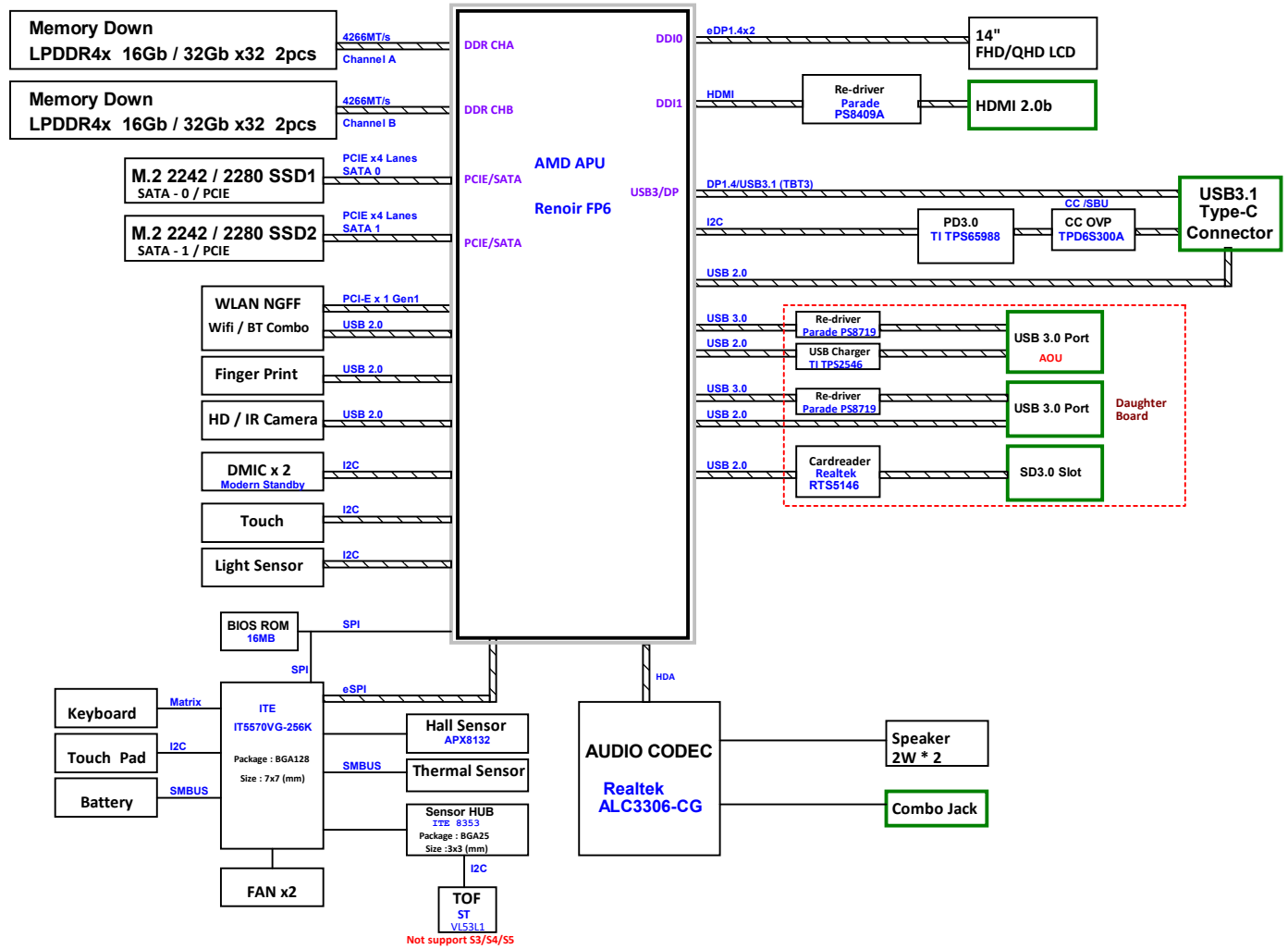
Aries 4B AMD Renoir FP6 Block Diagram



PCB 8L STACK UP

LAYER 1 : TOP
LAYER 2 : SVCC
LAYER 3 : IN1
LAYER 4 : IN2(High)
LAYER 5 : SGND
LAYER 6 : IN3
LAYER 7 : SGND
LAYER 8 : BOT

PROJECT : LS3
Quanta Computer Inc.

Power Diagram

02

Custom	PROJECT : LS3	
BU2	Quanta Computer Inc.	
Size	Document Number	Rev
	Power Map	1A
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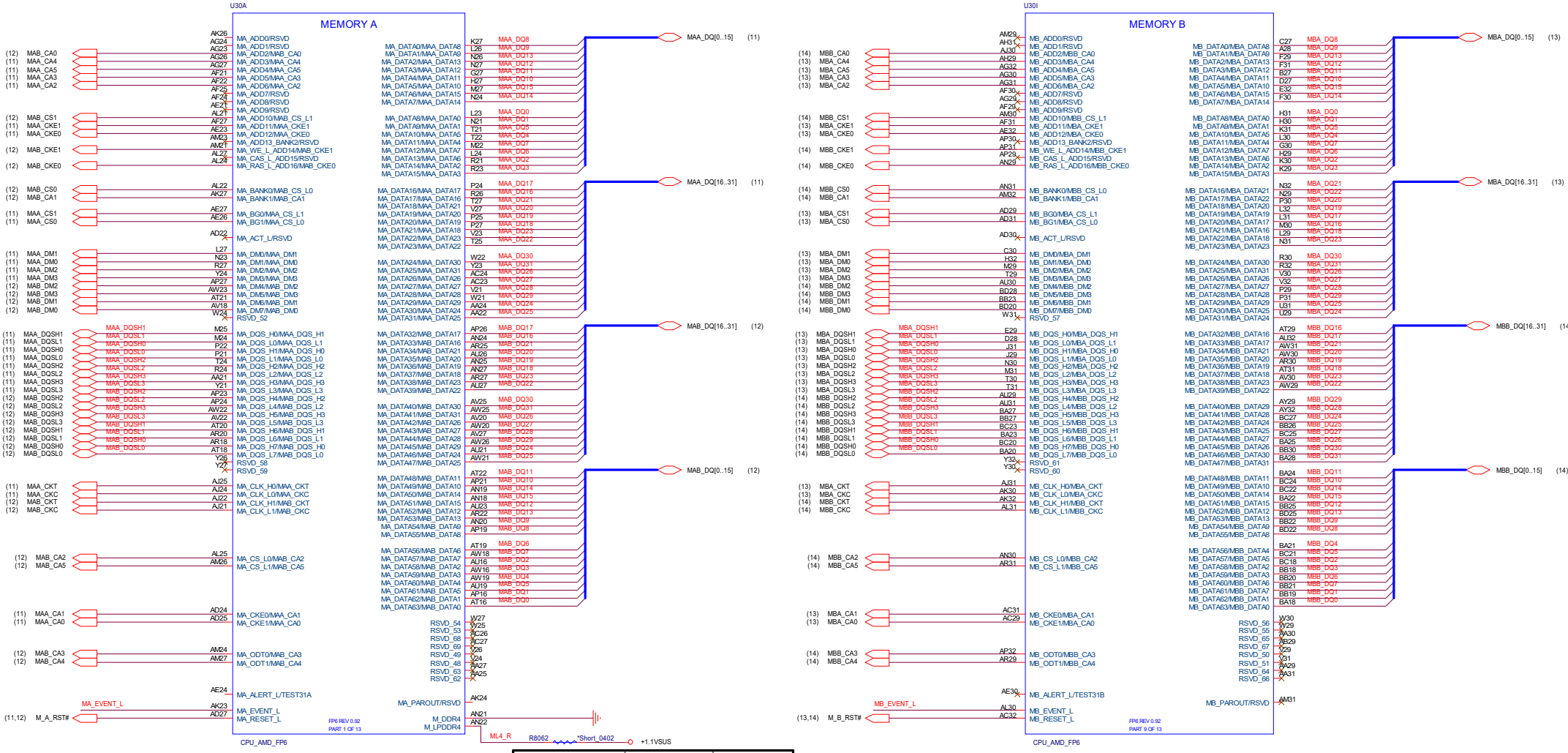

STRAPS	M_DDR4	M_LPDDR4
DDR4 ENABLE	H	L
LPDDR4 ENABLE	L	H

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	Quanta Computer Inc.
BU2	
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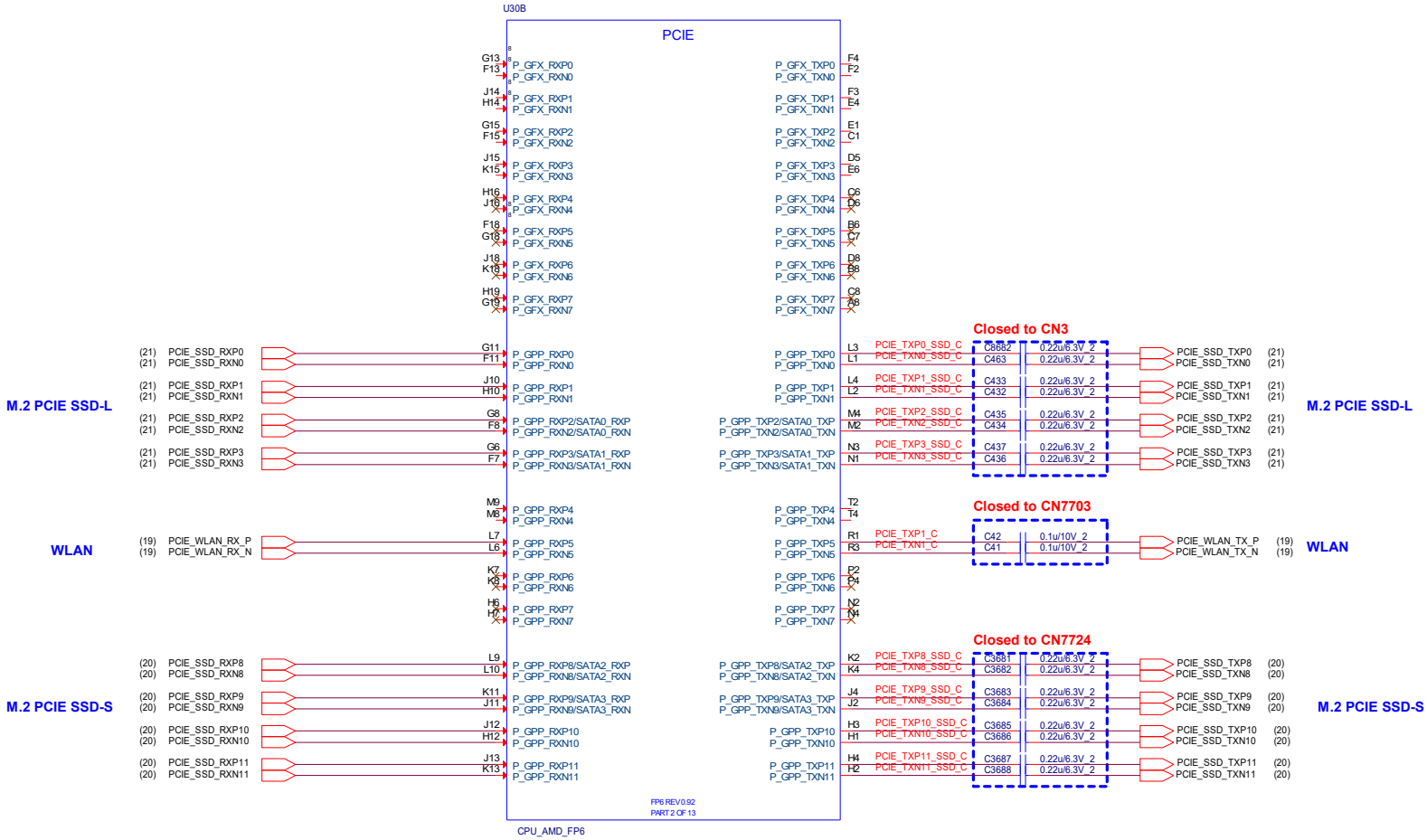

BU2

PROJECT : LS3

Quanta Computer Inc.

Size	Document Number	Rev
	eDP/DDI/MISC	1A

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APU DISPLAY and MISC

05

(9,23,24,47,48) +1.8V
(6,9,16,17,19,23,24,25,27,29,30,31,32,41,47) +3V
(9,23,44,48) +VDDP
(6,9,18,23,24,32,40,41,47,48) +1.8V_S5

+1.8V_S5
R78 4.7K_1% _2 APU_RST#
R79 4.7K_1% _2 APU_PWRGD
+3V
R7867 1K_5% _2 APU_ALERT#
R34 1K_5% _2 APU_THERMTRIP#
R7871 1K_5% _2 APU_SIC
R7872 1K_5% _2 APU_SID

EC-EVT-E14

Table 72. Connections for DisplayPort to HDMI™ Interface

Processor Signal Name	DVI Connector	$C_{Coupling}$	D_{TSD}	R_{TMDS}	Q_{TMDS}	Other Components
DP0_TXP0	TMDS Data2+	$C_{Coupling}$	D_{TSD}	R_{TMDS}	Q_{TMDS}	–
DP0_TXN0	TMDS Data2-	$C_{Coupling}$	D_{TSD}	R_{TMDS}	Q_{TMDS}	–
DP0_TXP1	TMDS Data1+	$C_{Coupling}$	D_{TSD}	R_{TMDS}	Q_{TMDS}	–
DP0_TXN1	TMDS Data1-	$C_{Coupling}$	D_{TSD}	R_{TMDS}	Q_{TMDS}	–
DP0_TXP2	TMDS Data0+	$C_{Coupling}$	D_{TSD}	R_{TMDS}	Q_{TMDS}	–
DP0_TXN2	TMDS Data0-	$C_{Coupling}$	D_{TSD}	R_{TMDS}	Q_{TMDS}	–
DP0_TXP3	TMDS Clock+	$C_{Coupling}$	D_{TSD}	R_{TMDS}	Q_{TMDS}	–
DP0_TXN3	TMDS Clock-	$C_{Coupling}$	D_{TSD}	R_{TMDS}	Q_{TMDS}	–
DP0_AUXP	DDC Clock	–	D_{TSD}	–	–	R_{AUX}
DP0_AUXN	DDC Data	–	D_{TSD}	–	–	R_{AUX}
DP0_HPD	Hot Plug Detect	–	D_{TSD}	–	–	R_{HPD}

DDI0 output to FHD Panel

(16) APU_DP0_TXP0 → DP0_TXP0 D11
(16) APU_DP0_TXN0 → DP0_TXN0 B11
(16) APU_DP0_TXP1 → DP0_TXP1 C11
(16) APU_DP0_TXN1 → DP0_TXN1 A11
(16) APU_DP0_TXP2 → DP0_TXP2 D10
(16) APU_DP0_TXN2 → DP0_TXN2 B10
(16) APU_DP0_TXP3 → DP0_TXP3 D9
(16) APU_DP0_TXN3 → DP0_TXN3 B9

(17) INT_HDMITX2P → DP1_TXP0 G23
(17) INT_HDMITX2N → DP1_TXN0 H23
(17) INT_HDMITX1P → DP1_TXP1 F22
(17) INT_HDMITX1N → DP1_TXN1 G22
(17) INT_HDMITX0P → DP1_TXP2 G21
(17) INT_HDMITX0N → DP1_TXN2 H21
(17) INT_HDMICLK+ → DP1_TXP3 F20
(17) INT_HDMICLK- → DP1_TXN3 G20

DDI1 output to HDMI conn

(23) SMBCLK0_EC
(23) SMBDATA0_EC
Q6A 2N7002KDW
Q6B 2N7002KDW
APU_SIC
APU_SID

Connect to EC SMBUS

U30C

DISPLAY/SVI2/JTAG/TEST

DP_BLON A22 APU_DP_BLON → APU_DP_BLON (16)
DP_DIGON D23 APU_DP_DIGON → APU_DP_DIGON (16)
DP_VARY_BL C23 APU_VARY_BL → APU_VARY_BL (16)

eDP

DP0_AUXP D12
DP0_AUXN B12 EDP_AUXP (16) / EDP_AUXN (16)
DP0_HPD C12 EDP_HPD_Q → EDP_HPD_Q (16)

HDMI

DP1_AUXP J20
DP1_AUXN K20 HDMI_DDCCLK (17) / HDMI_DDCDAT (17)
DP1_HPD L21 INT_HDMI_HPD (17)

TYPE C DP

DP2_AUXP L19
DP2_AUXN M19
DP2_HPD M20

DP3_AUXP M14
DP3_AUXN L14 DP3_AUXN (31)
DP3_HPD L16 DP3_HPD_Q → DP3_HPD_Q (31,32)

DP_STEREOSYNC B23 DP_STEREOSYNC
R119 1K_1% _2 +1.8V
R7873 *1K_1% _2

EDP_HPD_Q R7866 100K_1% _2
DP3_HPD_Q R541 100K_1% _2
APU_DP_BLON R7869 100K_1% _2
APU_DP_BLON R7868 100K_1% _2
APU_VARY_BL R7870 100K_1% _2

+3V +1.8V
R120 *2.2K_5% _2
R121 *2.2K_5% _2
C59 *220p/25V_2
(16) VARY_BL
Q7 *BSS138
R488 *0_5% _4
APU_VARY_BL

EMI/ESD reserve
APU_TRST#
VD6428 TVL5VB1-DFN1006-2L

TEST4 BB6 APU_TEST4 → TP45
TEST5 BD5 APU_TEST5 → TP46
TEST6 AG12
TEST14 G25 APU_TEST14 → TP21
TEST15 K25 APU_TEST15 → TP19
TEST16 F25 APU_TEST16 → TP17
TEST17 F26 APU_TEST17 → TP20
TEST31 H26 APU_TEST31 → TP22
TEST41 AK9 APU_TEST41 → TP15
ANALOGIO_0 AK21 APU_TEST470 → TP48
ANALOGIO_1 AG21 APU_TEST471 → TP47

APU_TDI AP3 → TDI
APU_TDO AU1 → TDO
APU_TCK AR2 → TCK
APU_TMS AU3 → TMS
APU_TRST# AR4 → TRST_L
APU_DBREQ# AT2 → DBREQ_L

(23,32) APU_RST# → APU_RST# AW3 → RESET_L
APU_PWRGD AW4 → PWROK

APU_SIC B22 → SIC
APU_SID D22 → SID
APU_ALERT# C22 → ALERT_L
(23) APU_THERMTRIP# → APU_THERMTRIP# AN9 → THERMTRIP_L
H_PROCHOT_C B25 → PROCHOT_L

SVC_APU D25 → SVC0
SVD_APU C25 → SVD0
SVT_APU A25 → SVT0

FP6 REV 0.92
PART 3 OF 13

CPU_AMD_FP6

SMU_ZVDDP P3 SMU_ZVDDP
R7874 196_1% _4 +VDDP

VDDP_S5_SENSE AK7 VDDP_S5_SENSE → VDDP_S5_SENSE (44)
VDDP_SENSE AK12 VDDP_SENSE → VDDP_SENSE (44)
VDDCR_SOC_SENSE J23 APU_VDDNB_RUN_FB_H → APU_VDDNB_RUN_FB_H (41)
VDDCR_SENSE K22 APU_VDD_RUN_FB_H → APU_VDD_RUN_FB_H (41)
VDDIO_MEM_S3_SENSE J21 VDDQ_SENSE → VDDQ_SENSE (39)
J22 APU_VSS_SENSE
VSS_SENSE_A AJ12 → TP7742
VSS_SENSE_B → APU_VSS_SENSE (41)

VSS_sense_A for VDDCR and VDDCR_SOC

APU_VDDNB_RUN_FB_H → TP24
APU_VDD_RUN_FB_H → TP23
APU_VSS_SENSE → TP7730
VDDP_S5_SENSE → TP7743
VDDP_SENSE → TP7744

APU Serial VID

SVT_APU R112 *Short_0402 → APU_SVT (41)
SVC_APU R114 *Short_0402 → APU_SVC (41)
SVD_APU R113 *Short_0402 → APU_SVD (41)

Place near APU within 500mil
CRB: SVC & SVD 22 ohm follow check list 0 ohm.

APU_PWRGD R81 *Short_0402 → CPU_PWRGD_SVID_REG (41)

HDT+ Connector for Debug only

+1.8V_S5
R41 1K_1%_2
APU_TRST#
C13 PROTO@0.01u/50V_4

R40 PROTO@1K_1% _2
R39 PROTO@10K_1% _2
R7876 PROTO@10K_1% _2
R37 PROTO@10K_1% _2

CN7
HDT_TRST# DBRDY3 DBRDY2 DBRDY1
APU_TCK R76 1K_1% _2
APU_TMS R74 1K_1% _2
APU_TDI R75 1K_1% _2
APU_TDO
APU_PWROK_BUF
APU_RST_L_BUF
APU_DBREQ# R66 1K_1% _2

*PROTO@ASP-137098-05_Header

CN1
APU_DBREQ#
DBRDY1
DBRDY2
APU_RST_L_BUF
DBRDY3
APU_PWROK_BUF
HDT_TRST#
APU_TDO
APU_TDI
APU_TMS
APU_TCK
+1.8V_S5

50696-0200m-v02-20p-l
PROTO@HDT CONN

VR (41) VRHOT#
R126 *Short_0402
H_PROCHOT#
R122 *Short_0402
APU_PROCHOT#
R123 *Short_0402
Q9 *2N7002k
R7875 1K_5%_2
H_PROCHOT_C
+3V

EC (23,37) EC_PROCHOT
Q8 2N7002k
C62 220p/25V_2

C28 PROTO@0.1u/16V_4
R70 PROTO@1K_1%_2
R80 PROTO@1K_1%_2
+1.8V
U6421
APU_RST#
APU_PWRGD
APU_RST_L_BUF
APU_PWROK_BUF
PROTO@74LVC2G07GW

PROJECT :LS3
Quanta Computer Inc.
BU2
Size | Document Number: APU Display Interface | Rev: 1A
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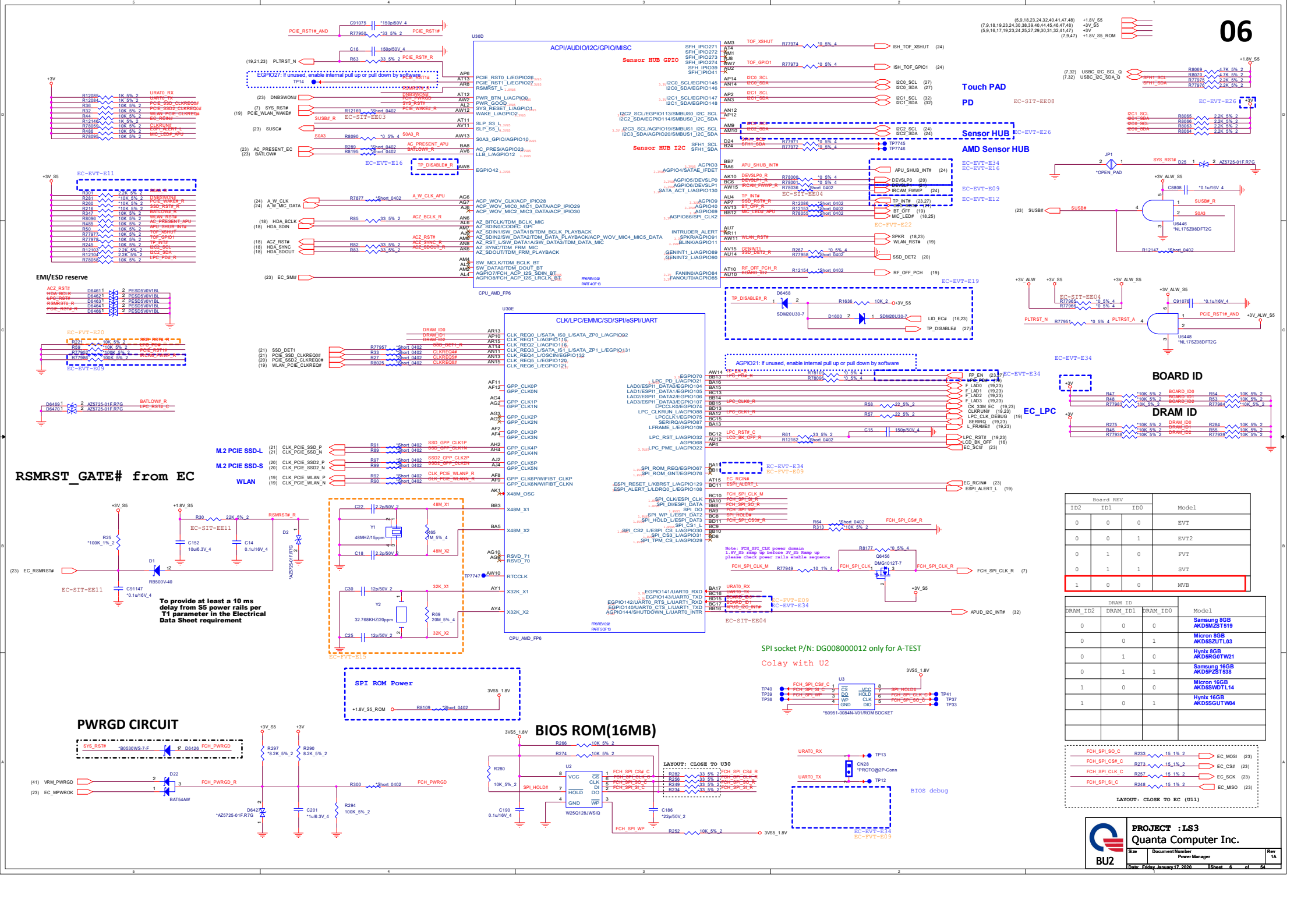
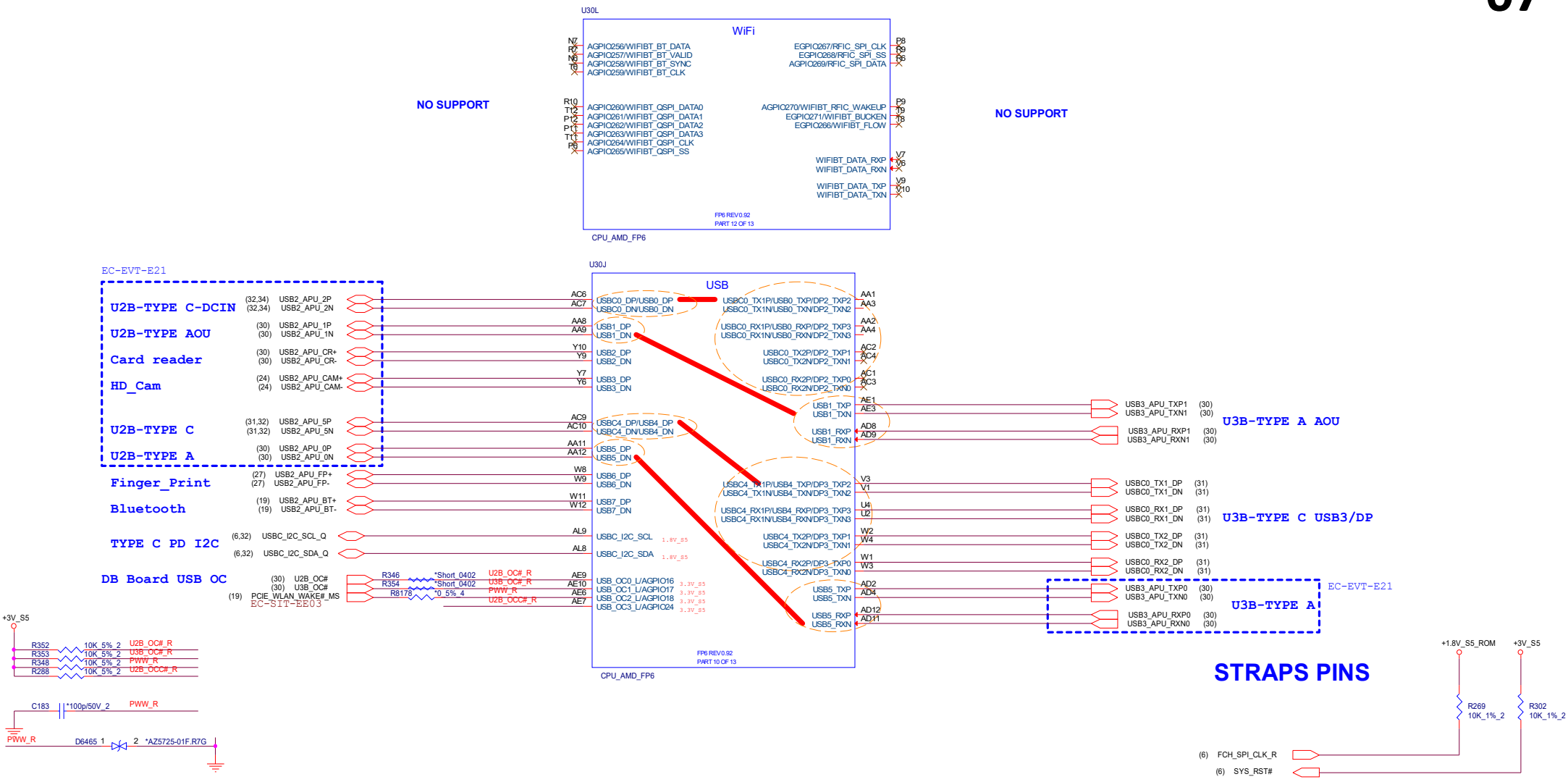


Board REV			
ID2	ID1	ID0	Model
0	0	0	EVT
0	0	1	EVT2
0	1	0	FVT
0	1	1	SVT
1	0	0	MVB

DRAM_ID			
DRAM_ID2	DRAM_ID1	DRAM_ID0	Model
0	0	0	Samsung 8GB AKD5MZS7519
0	0	1	Micron 8GB AKD5SZUTL03
0	1	0	Hynix 8GB AKD5RG0TW21
0	1	1	Samsung 16GB AKD5PZST538
1	0	0	Micron 16GB AKD5SWDTL14
1	0	1	Hynix 16GB AKD5SGUTW04

LAYOUT: CLOSE TO EC (U11)



REQUIRED STRAPS

	FCH_SPI_CLK_R	SYS_RST#
PULL HIGH	Use 48Mhz crystal clock and generate both internal and external clocks (pulled up VDD_18_S5) DEFAULT	normal reset mode (pulled up VDD_33_S5) DEFAULT

USB20_P0	USB20_P1	USB20_P2	USB20_P3	USB20_P4	USB20_P5	USB20_P6	USB20_P7
USB2.0 TYPEC DCIN	USB3.0 TYPEA	Card Reader	HD_CAM	USB2.0 TYPEC	USB3.0 TYPEA	FP	BT

USB30_P1	USB30_P4	USB30_P5
USB3.0 TYPEA	USB3.0 TYPEC	USB3.0 TYPEA

BU2

PROJECT : LS3
Quanta Computer Inc.

Size	Document Number	Rev
	CPU Decoupling 1	1A

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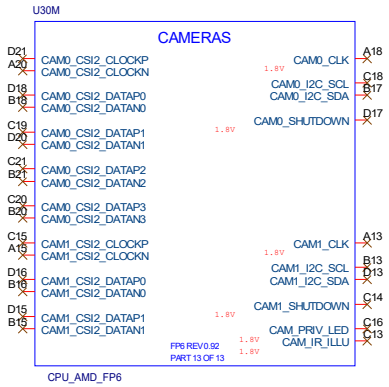

BU2

PROJECT : LS3

Quanta Computer Inc.

Size	Document Number	Rev
	CPU Decoupling 2	1A

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APU POWER

09

BOTTOM SIDE OUTSIDE OF APU

BOTTOM SIDE UNDER APU

+NB_CORE

C314 180p/50V_4 | C359 1u/6.3V_4 | C321 47U/6.3V_4 | C8684 22U/6.3V_6 | C342 47U/6.3V_6.3 | C354 47U/6.3V_6.3 | C348 47U/6.3V_6.3 | C361 47U/6.3V_4 | C343 47U/6.3V_4

EC-SVT-EE04

BOTTOM SIDE DECOUPLING UNDER APU

+1.1VSUS

C347 22u/6.3V_6 | C261 22u/6.3V_6 | C346 22u/6.3V_6 | C262 22u/6.3V_6 | C259 22u/6.3V_6 | C280 22u/6.3V_6 | C286 22u/6.3V_6 | C8685 1u/6.3V_4 | C340 1u/6.3V_4 | C338 180p/50V_4

C369 0.22u/25V_4 | C376 0.22u/25V_4 | C8688 0.22u/25V_4 | C274 0.22u/25V_4 | C370 180p/50V_4 | C362 180p/50V_4

If the VSS plane is cut to create a VDDIO_MEM_S3 plane, ceramic capacitors with NP0 or C0G dielectric are connected across the VDDIO_MEM_S3 and VSS plane split.

Background: VDDIO_VPH is a power supply pin on FP6 package used by certain phys within RN. The purpose of separating these phys is to allow better power efficiency and battery life in certain configurations. However AMD cannot guarantee the phys will meet compliance when 1.1V nominal source is used for VDDIO_VPH. This case is typically only for LPDDR4(x) based systems using the VDDIO_MEM_S3 1.1V source for VDDIO_VPH as previously recommended. A 1.2V or 1.8V nominal source will meet the phy requirements and is recommended. 1.2V is preferred for power savings if DP0 is implemented for eDP.

Fix: Use either 1.2V or 1.8V nominal source for VDDIO_VPH. Ensure the source meets the tolerance and ripple requirements defined in the FP6 IRM (PID# 56328)

+1.2V_VPH — R522 *0_5%_6 — +VDDIO_VPH

+1.8V — R494 0_5%_6

EC-SIT-EE02

EC-EVT-E11
EC-EVT-E31

+1.8V_S5 — R298 *Short_0603 — +APU_VDDIO_AZ

C230 1u/6.3V_4 | C203 22u/6.3V_6

BOTTOM SIDE OUTSIDE OF APU

+1.8V_S5_ROM — R287 *Short_0603 — +1.8V_S5_ROM_APU

C275 1u/6.3V_4 | C199 1u/6.3V_4 | C194 22u/6.3V_6

BOTTOM SIDE DECOUPLING UNDER APU

+3V — R285 *Short_0603 — +APU_VDD_33

C250 1u/6.3V_4 | C202 1u/6.3V_4 | C198 22u/6.3V_6

BOTTOM SIDE DECOUPLING UNDER APU

+1.8V

C270 1u/6.3V_4 | C227 1u/6.3V_4 | C215 22u/6.3V_6

BOTTOM SIDE DECOUPLING UNDER APU

U30F

POWER

+NB_CORE

VDDCR_SOC_1 N16
VDDCR_SOC_2 N18
VDDCR_SOC_3 N20
VDDCR_SOC_4 P17
VDDCR_SOC_5 P19
VDDCR_SOC_6 R18
VDDCR_SOC_7 R20
VDDCR_SOC_8 T19
VDDCR_SOC_9 U18
VDDCR_SOC_10 U20
VDDCR_SOC_11 V19
VDDCR_SOC_12 W18
VDDCR_SOC_13 W20
VDDCR_SOC_14 Y19

+1.1VSUS

VDDIO_MEM_S3_1 AC20
VDDIO_MEM_S3_2 AC28
VDDIO_MEM_S3_3 AD23
VDDIO_MEM_S3_4 AD26
VDDIO_MEM_S3_5 AD28
VDDIO_MEM_S3_6 AD32
VDDIO_MEM_S3_7 AE20
VDDIO_MEM_S3_8 AE22
VDDIO_MEM_S3_9 AE25
VDDIO_MEM_S3_10 AE28
VDDIO_MEM_S3_11 AF23
VDDIO_MEM_S3_12 AF26
VDDIO_MEM_S3_13 AF28
VDDIO_MEM_S3_14 AF32
VDDIO_MEM_S3_15 AG20
VDDIO_MEM_S3_16 AG22
VDDIO_MEM_S3_17 AG25
VDDIO_MEM_S3_18 AG28
VDDIO_MEM_S3_19 AJ20
VDDIO_MEM_S3_20 AJ23
VDDIO_MEM_S3_21 AJ26
VDDIO_MEM_S3_22 AJ28
VDDIO_MEM_S3_23 AJ32
VDDIO_MEM_S3_24 AK22
VDDIO_MEM_S3_25 AK25
VDDIO_MEM_S3_26 AK28
VDDIO_MEM_S3_27 AL23
VDDIO_MEM_S3_28 AL26
VDDIO_MEM_S3_29 AL28
VDDIO_MEM_S3_30 AL32
VDDIO_MEM_S3_31 AM22
VDDIO_MEM_S3_32 AM25
VDDIO_MEM_S3_33 AM28
VDDIO_MEM_S3_34 AN28
VDDIO_MEM_S3_35 AN32
VDDIO_MEM_S3_36 AP26
VDDIO_MEM_S3_37 AR32

+VDDIO_VPH

VDDIO_VPH_1 AC21
VDDIO_VPH_2 AD21

+APU_VDDIO_AZ

VDDIO_AUDIO AP9

+APU_VDD_33

VDD_33_1 AL18
VDD_33_2 AM17

+1.8V

VDD_18_1 AL20
VDD_18_2 AM19

+1.8V_S5_ROM_APU

VDD_18_S5_1 AL19
VDD_18_S5_2 AM18

+APU_VDD_33_S5

VDD_33_S5_1 AL17
VDD_33_S5_2 AM16

+VDDP_S5

VDDP_S5_1 AL11
VDDP_S5_2 AL12
VDDP_S5_3 AM12

+VDDP

VDDP_1 M15
VDDP_2 M16
VDDP_3 M18

1.5V_RTC_ALW_C

1.5V_RTC_ALW — R386 1K_1%_2 — 1.5V_RTC_ALW_C

4.5uA

C195 1u/6.3V_4 | C196 0.22u/25V_4

20MIL

VDDBT_RTC_G AJ11

FP6 REV 0.92
PART 6 OF 13

CPU_AMD_FP6

+CPU_CORE

VDDCR_1 G7
VDDCR_2 G10
VDDCR_3 G12
VDDCR_4 G14
VDDCR_5 H8
VDDCR_6 H11
VDDCR_7 H15
VDDCR_8 K6
VDDCR_9 K12
VDDCR_10 K14
VDDCR_11 L8
VDDCR_12 M7
VDDCR_13 M10
VDDCR_14 N14
VDDCR_15 P7
VDDCR_16 P10
VDDCR_17 P13
VDDCR_18 P15
VDDCR_19 R8
VDDCR_20 R14
VDDCR_21 R16
VDDCR_22 T7
VDDCR_23 T10
VDDCR_24 T13
VDDCR_25 T15
VDDCR_26 T17
VDDCR_27 U14
VDDCR_28 U16
VDDCR_29 V13
VDDCR_30 V15
VDDCR_31 V17
VDDCR_32 W7
VDDCR_33 W10
VDDCR_34 W14
VDDCR_35 W16
VDDCR_36 Y5
VDDCR_37 Y13
VDDCR_38 Y15
VDDCR_39 Y17
VDDCR_40 AA7
VDDCR_41 AA10
VDDCR_42 AA14
VDDCR_43 AA16
VDDCR_44 AA18
VDDCR_45 AB13
VDDCR_46 AB15
VDDCR_47 AB17
VDDCR_48 AB19
VDDCR_49 AC14
VDDCR_50 AC16
VDDCR_51 AC18
VDDCR_52 AD7
VDDCR_53 AD10
VDDCR_54 AD13
VDDCR_55 AD15
VDDCR_56 AD17
VDDCR_57 AD19
VDDCR_58 AE8
VDDCR_59 AE14
VDDCR_60 AE16
VDDCR_61 AE18
VDDCR_62 AF7
VDDCR_63 AF10
VDDCR_64 AF13
VDDCR_65 AF15
VDDCR_66 AF17
VDDCR_67 AF19
VDDCR_68 AG14
VDDCR_69 AG16
VDDCR_70 AG18
VDDCR_71 AH3
VDDCR_72 AH5
VDDCR_73 AH7
VDDCR_74 AH9
VDDCR_75 AJ7
VDDCR_76 AJ10
VDDCR_77 AJ14
VDDCR_78 AJ16
VDDCR_79 AJ18
VDDCR_80 AK13
VDDCR_81 AK15
VDDCR_82 AK17
VDDCR_83 AK19

+CPU_CORE

C291 47U/6.3V_6 | C287 22U/6.3V_6 | C281 22U/6.3V_6 | C324 22U/6.3V_6 | C312 22U/6.3V_6 | C305 22U/6.3V_6 | C292 47U/6.3V_6 | C288 22U/6.3V_6 | C282 22U/6.3V_6

EC-SVT-EE04 EC-SVT-EE04

C349 22U/6.3V_6 | C313 22U/6.3V_6 | C8686 22U/6.3V_6 | C8687 22U/6.3V_6 | C322 22U/6.3V_6 | C311 22U/6.3V_6 | C304 22U/6.3V_6 | C316 180p/50V_4

EC-EVT-E35

C91091 22U/6.3V_6 | C91092 22U/6.3V_6 | C91093 22U/6.3V_6 | C91094 *22U/6.3V_6

BOTTOM SIDE DECOUPLING UNDER APU

+VDDP

BOTTOM SIDE DECOUPLING UNDER APU

C249 1u/6.3V_4 | C272 180p/50V_4 | C257 1u/6.3V_4 | C224 1u/6.3V_4 | C229 1u/6.3V_4

C226 22u/6.3V_6 | C225 22u/6.3V_6 | C263 1u/6.3V_4 | C222 1u/6.3V_4 | C223 1u/6.3V_4 | C220 1u/6.3V_4

+VDDP_S5 1A

BOTTOM SIDE DECOUPLING UNDER APU

C217 22u/6.3V_6 | C245 1u/6.3V_4 | C258 1u/6.3V_4 | C277 1u/6.3V_4

+3V_S5 — R286 *Short_0603 — +APU_VDD_33_S5

C276 1u/6.3V_4 | C200 1u/6.3V_4 | C197 22u/6.3V_6

BOTTOM SIDE DECOUPLING UNDER APU

1.5V_RTC_ALW_C

20MIL

(23) EC_RTC_RST — 2 — Q25 DDTC144EUA-7-F

EC-EVT-E02

EC-EVT-E02

3VRTC_ALW — R77985 *Short_0603 — 20MIL — 1.5V_RTC_ALW

20MIL

U17 VOUT VIN GND

*AP2138N-1.5TRG1

C8689 1u/6.3V_4

BAT_RTC_ALW — 20MIL — R388 470_1%_4 — VCCRTC_2

+3V_ALW — 20MIL

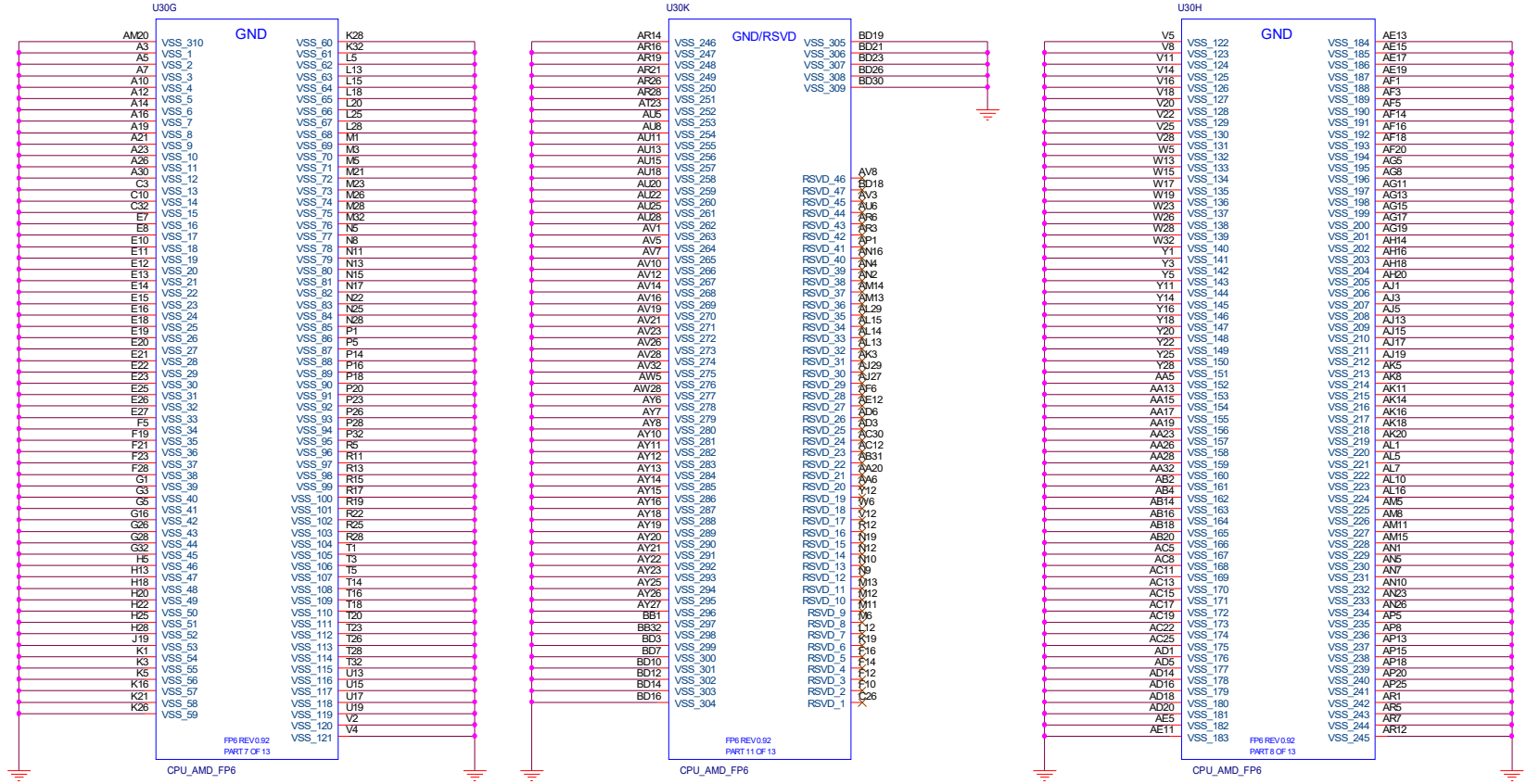
D27 BAT54CW-7-F

BU2

PROJECT : LS3
Quanta Computer Inc.

Size | Document Number: CPU Decoupling 3 | Rev: 1A

Date: Friday, March 13, 2020 | Sheet 9 of 54



BU2

PROJECT : LS3

Quanta Computer Inc.

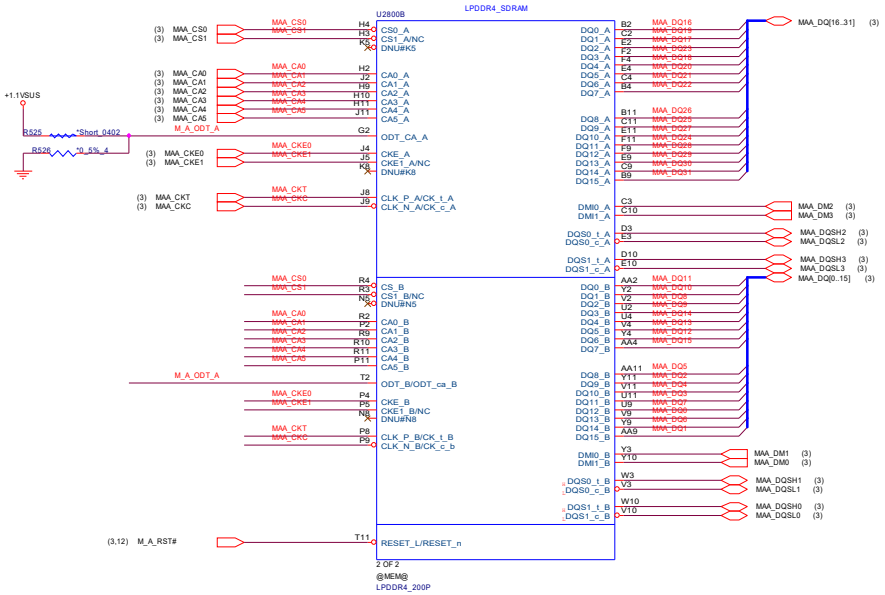
Size	Document Number	Rev
	GND	1A

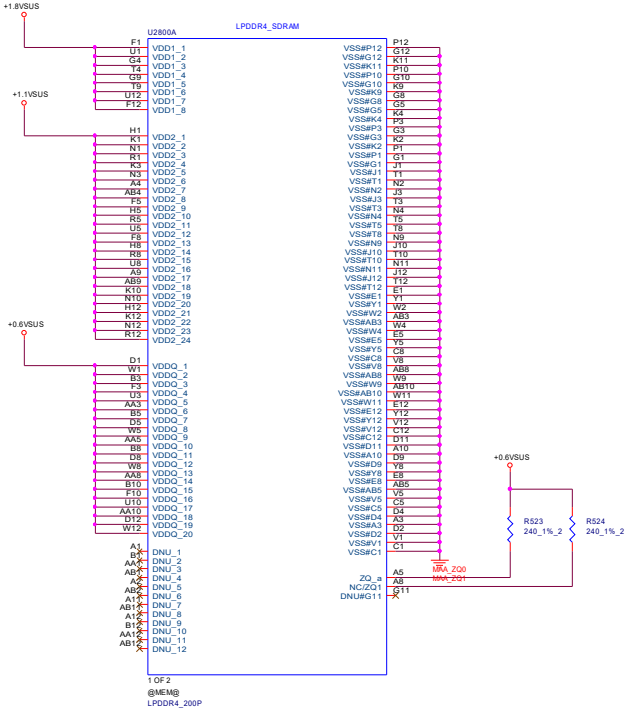
Date: Friday, January 17, 2020 | Sheet 10 of 54

(3,9,12,13,14,39,48) +1.1VSUS
(5,6,9,16,17,19,23,24,25,27,29,30,31,32,41,47) +3V

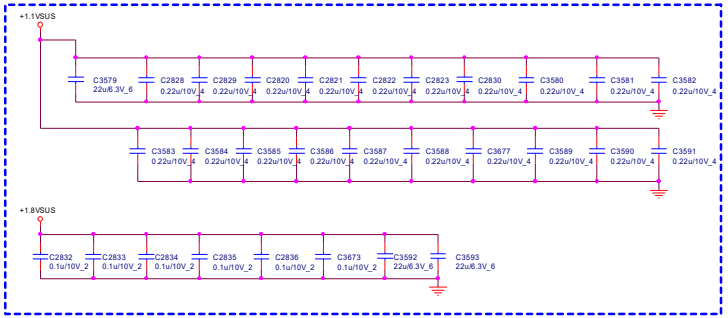
Non-NB Footprint:bga200-hynix-h9hcnnnbkmalhr-0_5s

LPDDR4 CH-MAA

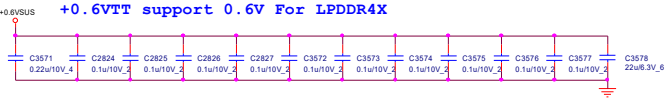




EC-EVT-E05



+0.6VSUS **+0.6VTT support 0.6V For LPDDR4X**



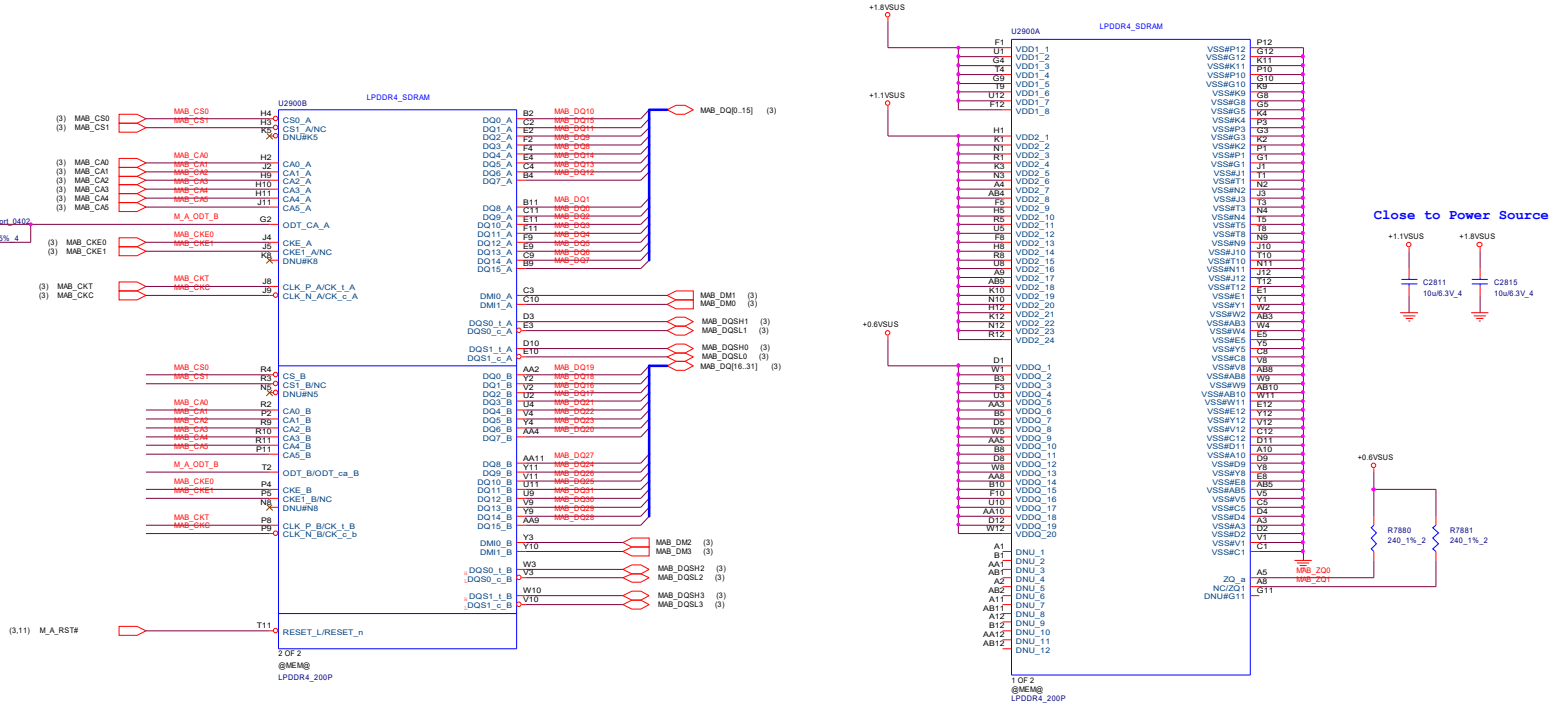
PROJECT : LS3
Quanta Computer Inc.
BU2

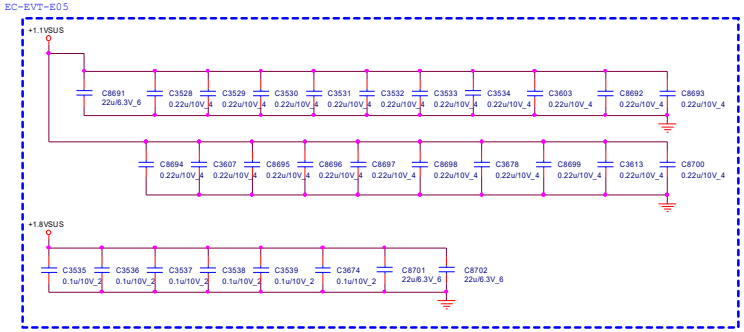
Size	Document Number	Rev
	LPDDR4_A Channel_Memory Down	1A

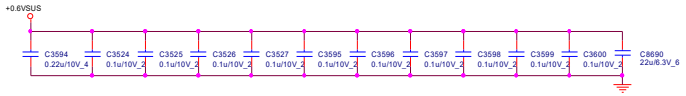
Date: Friday, January 17, 2020 Sheet 11 of 54

Non-NB Footprint:bga200-hynix-h9hcnnnbkmalhr-0_5s

LPDDR4 CH-MAB



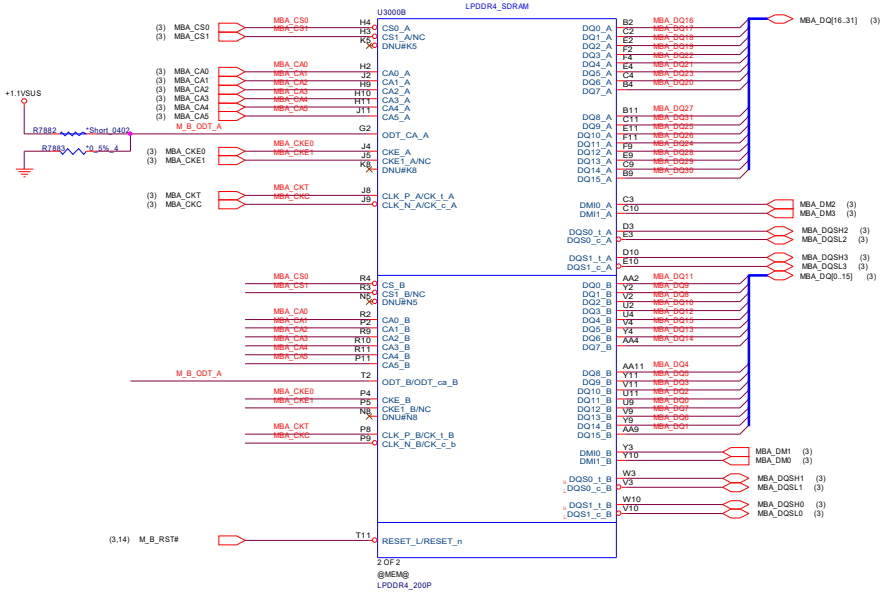


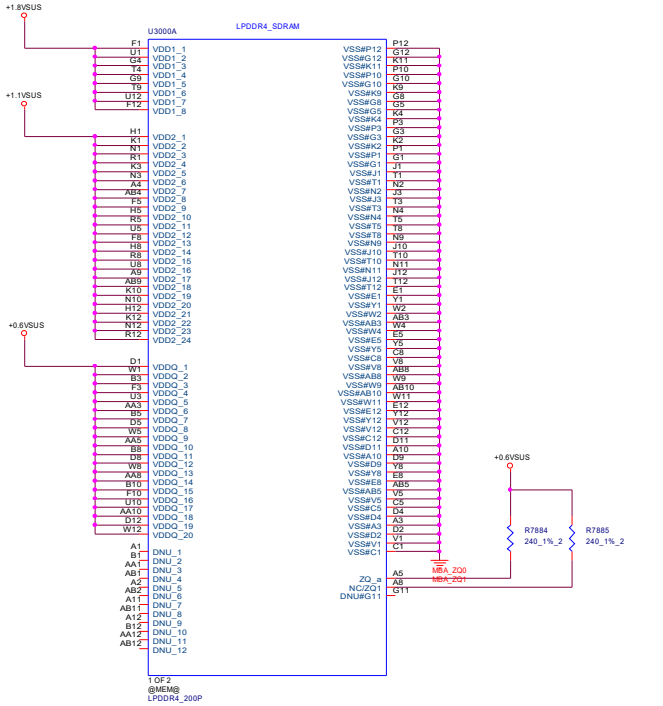


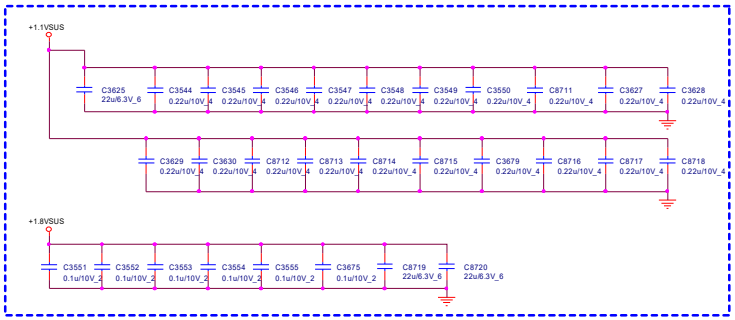
BU2	PROJECT : LS3 Quanta Computer Inc.	
Size	Document Number LPDDR4_A Channel_Memory Down	Rev 1A
Date: Friday, January 17, 2020	Sheet 12 of 54	

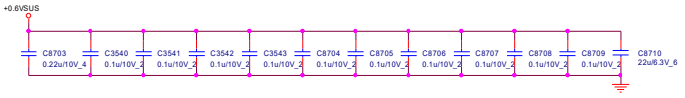
Non-NB Footprint:bga200-hynix-h9hcnnnbkmalhr-0_5s

LPDDR4 CH-MBA







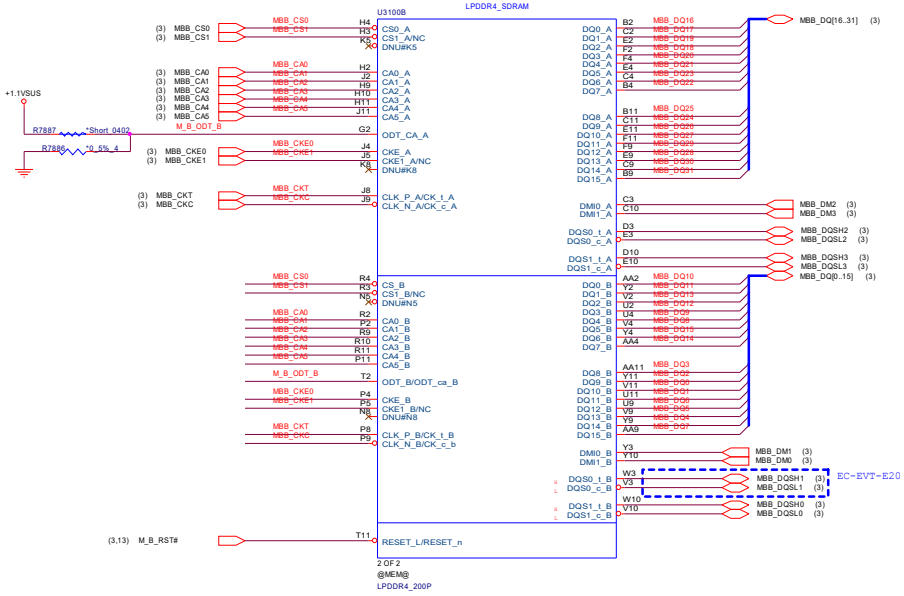


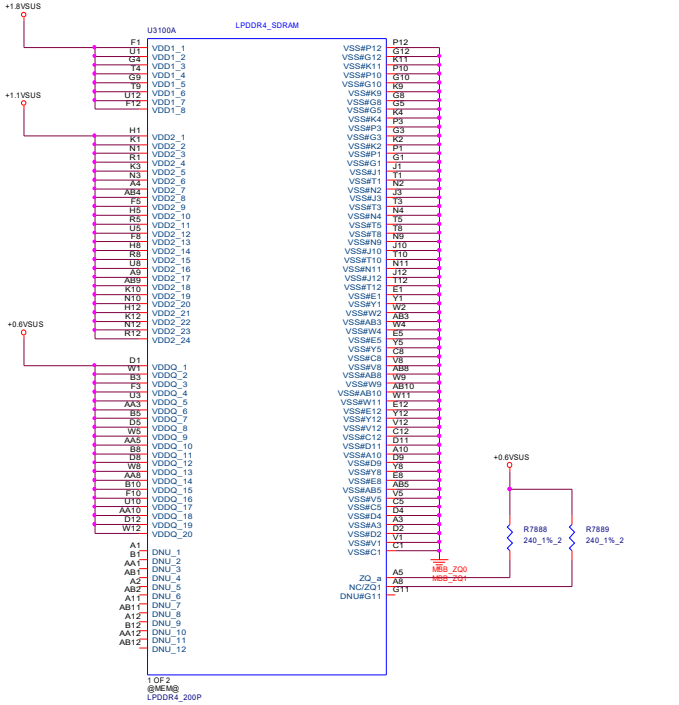
BU2	PROJECT : LS3 Quanta Computer Inc.	
Size	Document Number LPDDR4_8 Channel_Memory Down	Rev 1A
Date: Friday, January 17, 2020	Sheet 13 of 54	

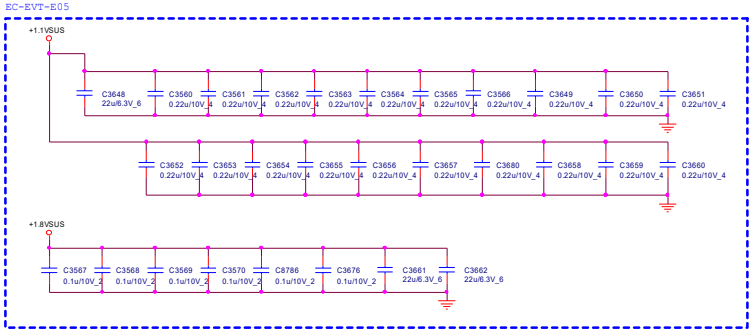
(3,9,11,12,13,39,48) +1.1VSUS
(5,6,9,16,17,19,23,24,25,27,29,30,31,32,41,47) +3V

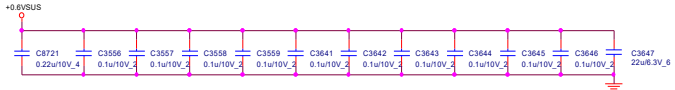
Non-NB Footprint:bga200-hynix-h9hcnnnbkmalhr-0_5s

LPDDR4 CH-MBB

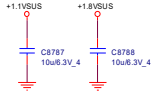








Close to Power Source

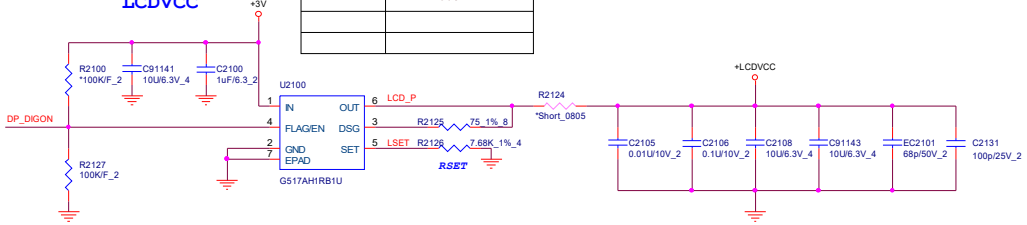


PROJECT :LS3
Quanta Computer Inc.
BU2
Size | Document Number: LPDDR4_B Channel_Memory Down | Rev: 1A
Date: Friday, January 17, 2020 | Sheet 14 of 54

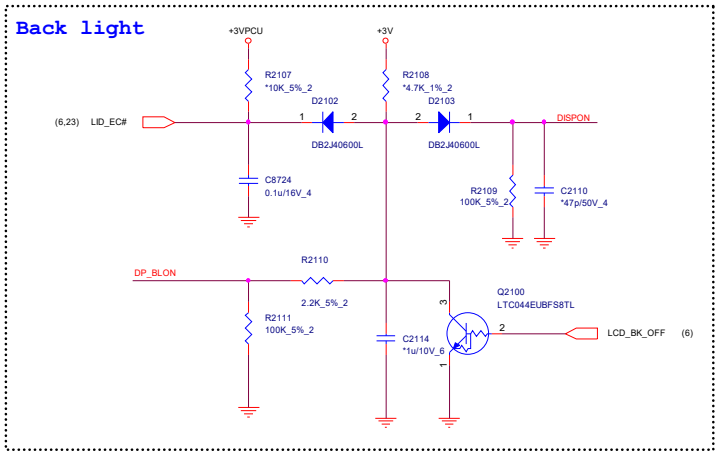
+3V (5,6,9,17,19,23,24,25,27,29,30,31,32,41,47)
+VIN (28,37,38,39,40,41,42,43,48,49)

G517AH	
RSET(KΩ)	Current Limit(A)
7.68	2.7
10.5	2
21	1
42	0.5

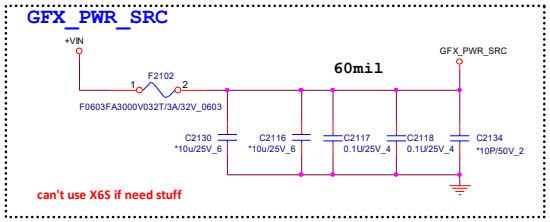
LCDVCC

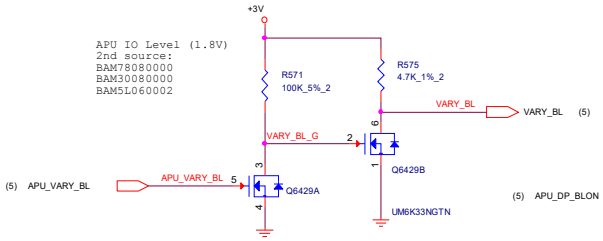


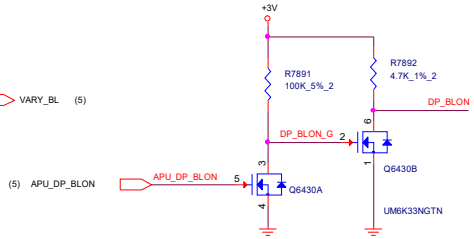
Back light

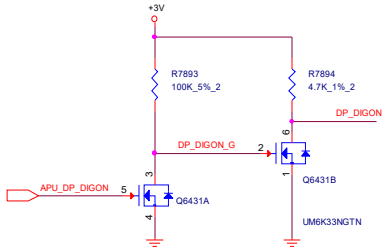


GFX_PWR_SRC

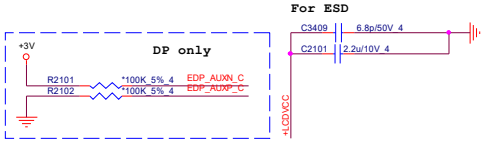




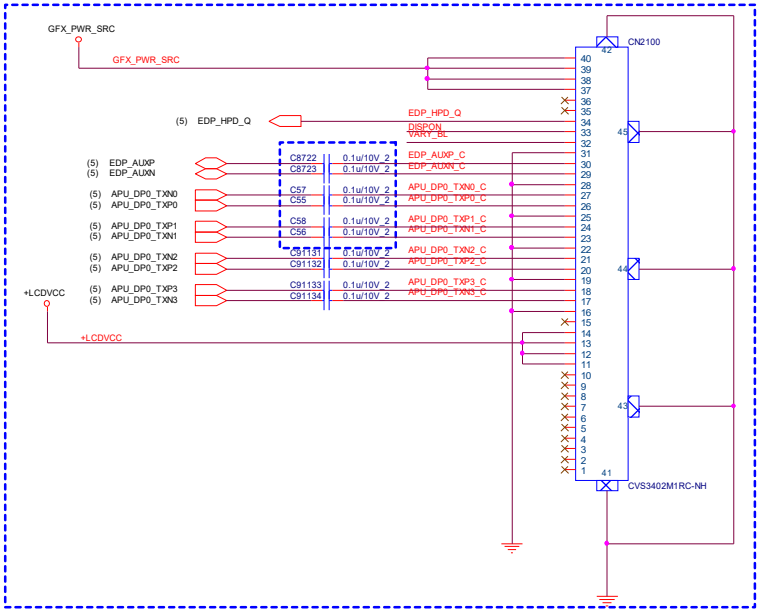




For ESD



EC-EVT-E23



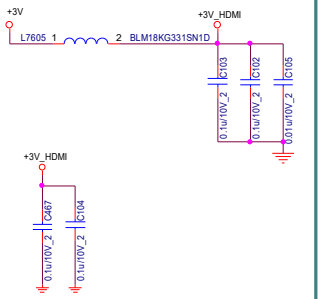
BU2

PROJECT : LS3
Quanta Computer Inc.

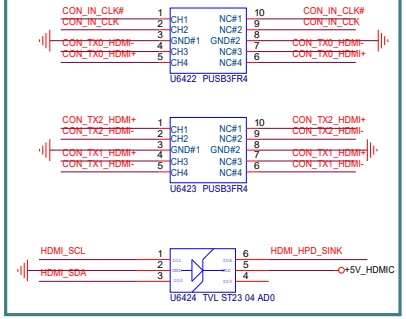
Size	Document Number	Rev
	eDP	1A
Date: Friday, January 17, 2020	Sheet 16 of 54	

HDMI with Parade 8409A

Close to Chip

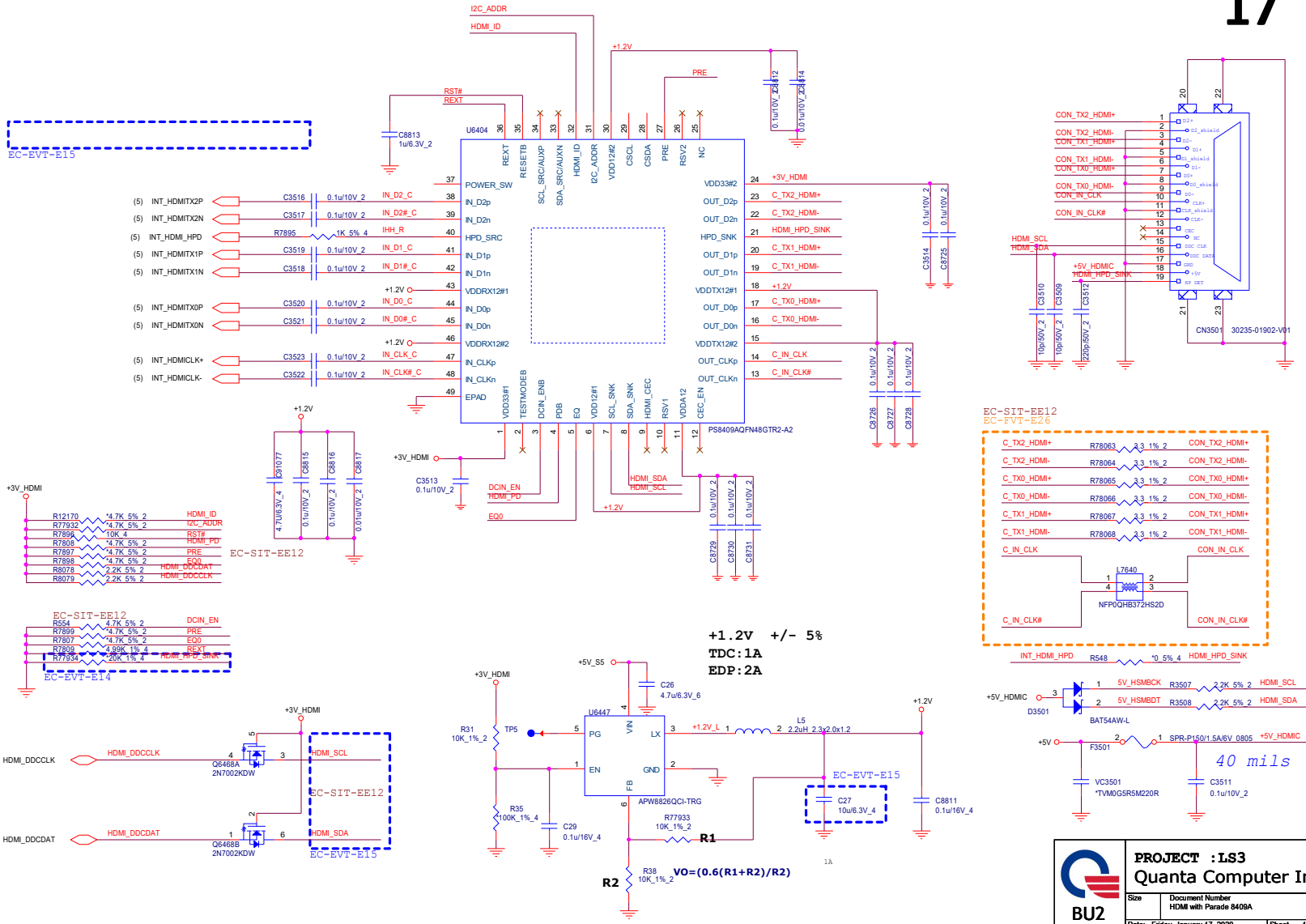


Close to HDMI connector



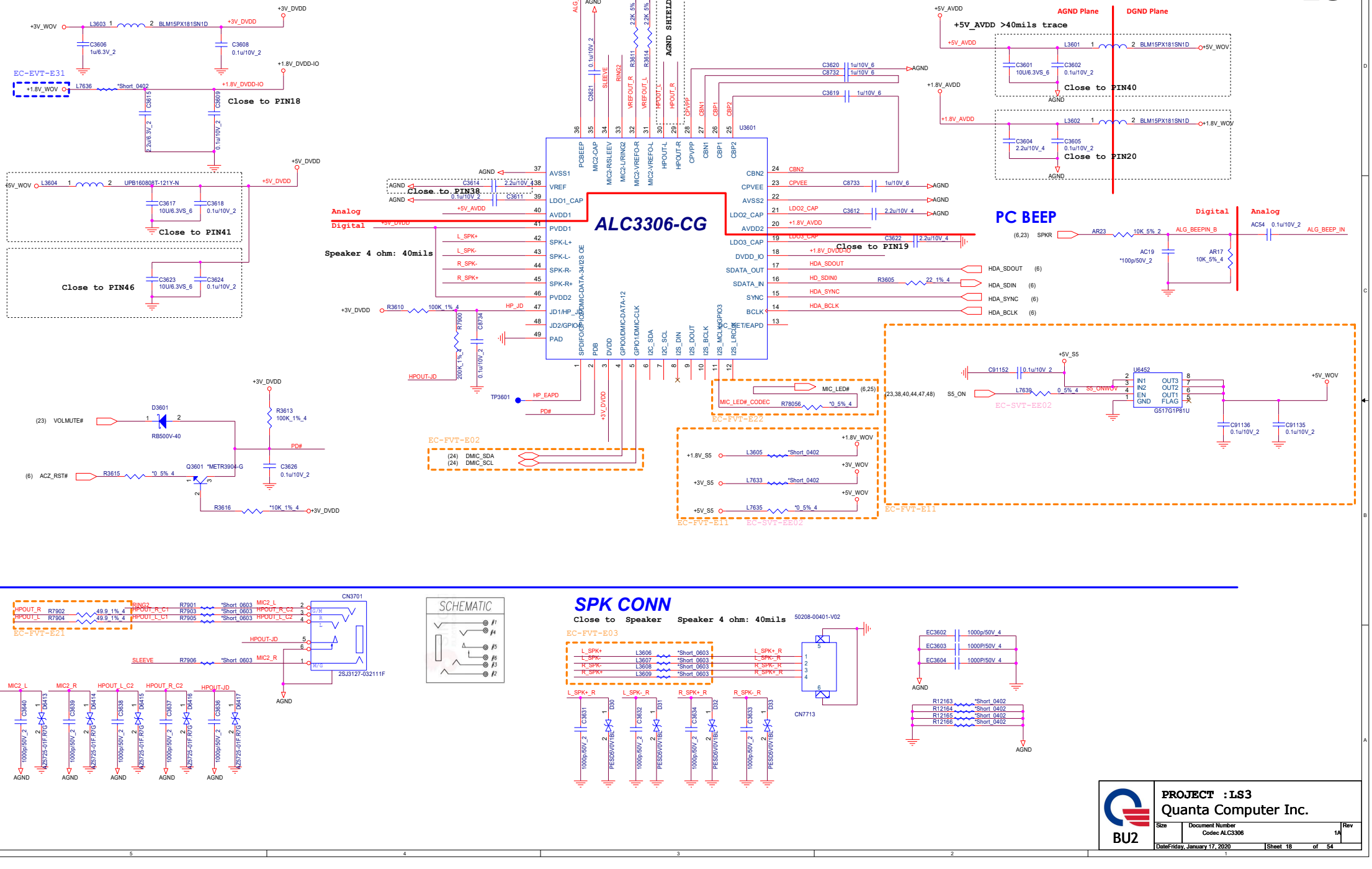
EC-EVT-E29

EC-EVT-E15



BU2	PROJECT : LS3 Quanta Computer Inc.		
	Size	Document Number HDMI with Parade 8409A	Rev 1A
	Date: Friday, January 17, 2020	Sheet 17 of 54	

ALC3306-CG


ALC3306-CG
AGND Plane
DGND Plane
+5V_AVDD >40mils trace
Close to PIN18
Close to PIN40
Close to PIN20
Close to PIN41
Close to PIN46
Close to PIN38
Close to PIN19
AGND SHIELD
Analog
Digital
Speaker 4 ohm: 40mils
PC BEEP
EC-EVT-E31
EC-FVT-E02
EC-FVT-E22
EC-FVT-E11
EC-SVT-EE02
EC-FVT-E21
EC-FVT-E03
SPK CONN
Close to Speaker
Speaker 4 ohm: 40mils
SCHEMATIC
PROJECT :LS3
Quanta Computer Inc.
BU2
Codec ALC3306
DateFriday, January 17, 2020
Sheet 18 of 54

WLAN

Mini Card
WLAN/BT(Option)

100mils

100mils

EC-FVT-E25

CN7726

*PROTO@ASP-137098-05_Header

U6444

NCT3522U

WLAN_PWR_EN SHOULD COME FROM EC
IN S3/S4/S5, EC TOGGLES LOW THIS SIGNAL
IN S03, EC KEEPS THIS SIGNAL HIGH

L7623 MCM2012B900GBE

Check pin define

CN7703

NGFF EKEY

APCI0076-P001A

EC-SIT-EE04

EC-SIT-EE03

EC-SVT-EE03

M2SSD_PWREN SHOULD COME FROM EC

NVMe (PCIe or M.2) devices should be powered by S0 rail to reduce power consumption in MS.

SATA SSD should be powered by S5 rail as SATA SSD has DEVSLP feature to reduce power consumption.

(5,6,9,16,17,19,23,24,25,27,29,30,31,32,41,47) +3V

20

+V3DX_SDD2

+3V_SSD — R8122 *Short_0805

C8737 SSD@10u/6.3V_4
C8740 SSD@0.1u/16V_4
C8743 SSD@0.01u/50V_4

NEAR PIN 2/4

+V3DX_SDD2

C8738 SSD@10u/6.3V_4
C8741 SSD@0.1u/16V_4
C8744 SSD@0.01u/50V_4

NEAR PIN 12/14/16/18

+V3DX_SDD2

C8739 SSD@10u/6.3V_4
C8742 SSD@0.1u/16V_4
C8745 SSD@0.01u/50V_4

NEAR PIN 70/72/74

DC Current rating: 2.1 A (MAX)

CN7724

NGFF- Key M

1	GND_PRESENCE_IND	3.3Vaux	2
3	GND	3.3Vaux1	4
5	PERn3	N/C	6
7	PERp3	N/C1	8
9	GND1	DAS/DSS/LED#1(OD)	10
11	PETn3	3.3Vaux2	12
13	PETp3	3.3Vaux3	14
15	GND2	3.3Vaux4	16
17	PERn2	3.3Vaux5	18
19	PERp2	N/C2	20
21	GND3	N/C3	22
23	PETn2	N/C4	24
25	PETp2	N/C5	26
27	GND4	N/C6	28
29	PERn1	N/C7	30
31	PERp1	N/C8	32
33	GND5	N/C9	34
35	PETn1	N/C10	36
37	PETp1	DEVSLP	38
39	GND6	N/C11	40
41	PERn0/SATA-R+	N/C12	42
43	PERp0/SATA-R-	N/C13	44
45	GND7	N/C14	46
47	PETn0/SATA-T-	N/C15	48
49	PETp0/SATA-T+	PERST#	50
51	GND8	CLKREQ#	52
53	REFCLKn	PEWAKE#	54
55	REFCLKp	NC16	56
57	GND9	NC17	58
77	77	76	76
79	79		78
67	N/C18	SUSCLK(32kHz)	68
69	PEDET_OC-PCIE/GND-SATA	3.3Vaux6	70
71	GND10	3.3Vaux7	72
73	GND11	3.3Vaux8	74
75	GND12		

SSD@2280 SSD_NGFF CONN

(4) PCIE_SSD_RXN11
(4) PCIE_SSD_RXP11
(4) PCIE_SSD_TXN11
(4) PCIE_SSD_TXP11
(4) PCIE_SSD_RXN10
(4) PCIE_SSD_RXP10
(4) PCIE_SSD_TXN10
(4) PCIE_SSD_TXP10
(4) PCIE_SSD_RXN9
(4) PCIE_SSD_RXP9
(4) PCIE_SSD_TXN9
(4) PCIE_SSD_TXP9

EC-EVT-E04

(4) PCIE_SSD_RXP8
(4) PCIE_SSD_RXN8
(4) PCIE_SSD_TXN8
(4) PCIE_SSD_TXP8
(6) CLK_PCIE_SSD2_N
(6) CLK_PCIE_SSD2_P

+V3DX_SDD2

EC-EVT-E04 R7908 100K_5%_2

SSD_DET2

(6) SSD_DET2

SSD_DET2:
SSD_PCIE IF => Low

+V3DX_SDD2

EC-EVT-E16

R77993 *10K_5%_2

DEVSLP0 (6)

DEVSLP[0] can be used for SATA Port 0 or 2.

SSD2_PLTRST_N

PCIE_SSD2_CLKREQ0# (6)

+V3DX_SDD2

SSD2_PLTRST_N — R12087 *Short_0402 — SSD_PLTRST_N (21)

BU2	PROJECT : LS3 Quanta Computer Inc.	
Size	Document Number NGFF SSD M Key	Rev 1A
Date: Friday, January 17, 2020	Sheet 20 of 54	

M2SSD_PWREN SHOULD COME FROM EC

NVMe (PCIe or M.2) devices should be powered by S0 rail to reduce power consumption in MS.

SATA SSD should be powered by S5 rail as SATA SSD has DEVSLP feature to reduce power consumption.

(5,6,9,16,17,19,23,24,25,27,29,30,31,32,41,47) +3V

21

+V3DX_SDD

+3V_SSD — R8121 *Short_0805

C3 SSD@10u/6.3V_4
C182 SSD@0.1u/16V_4
C127 SSD@0.01u/50V_4

NEAR PIN 2/4

+V3DX_SDD

C4 SSD@10u/6.3V_4
C176 SSD@0.1u/16V_4
C126 SSD@0.01u/50V_4

NEAR PIN 12/14/16/18

+V3DX_SDD

C5 SSD@10u/6.3V_4
C130 SSD@0.1u/16V_4
C129 SSD@0.01u/50V_4

NEAR PIN 70/72/74

DC Current rating: 2.1 A (MAX)

CN3

NGFF- Key M

1	GND_PRESENCE_IND	3.3Vaux	2
3	GND	3.3Vaux1	4
5	PERn3	N/C	6
7	PERp3	N/C1	8
9	GND1	DAS/DSS/LED#1(OD)	10
11	PETn3	3.3Vaux2	12
13	PETp3	3.3Vaux3	14
15	GND2	3.3Vaux4	16
17	PERn2	3.3Vaux5	18
19	PERp2	N/C2	20
21	GND3	N/C3	22
23	PETn2	N/C4	24
25	PETp2	N/C5	26
27	GND4	N/C6	28
29	PERn1	N/C7	30
31	PERp1	N/C8	32
33	GND5	N/C9	34
35	PETn1	N/C10	36
37	PETp1	DEVSLP	38
39	GND6	N/C11	40
41	PERn0/SATA-R+	N/C12	42
43	PERp0/SATA-R-	N/C13	44
45	GND7	N/C14	46
47	PETn0/SATA-T-	N/C15	48
49	PETp0/SATA-T+	PERST#	50
51	GND8	CLKREQ#	52
53	REFCLKn	PEWAKE#	54
55	REFCLKp	NC16	56
57	GND9	NC17	58
77	77	76	76
79	79		78
67	N/C18	SUSCLK(32kHz)	68
69	PEDET_OC-PCIE/GND-SATA	3.3Vaux6	70
71	GND10	3.3Vaux7	72
73	GND11	3.3Vaux8	74
75	GND12		

SSD@2280 SSD_NGFF CONN

(4) PCIE_SSD_RXN0
(4) PCIE_SSD_RXP0
(4) PCIE_SSD_TXN0
(4) PCIE_SSD_TXP0
(4) PCIE_SSD_RXN1
(4) PCIE_SSD_RXP1
(4) PCIE_SSD_TXN1
(4) PCIE_SSD_TXP1
(4) PCIE_SSD_RXN2
(4) PCIE_SSD_RXP2
(4) PCIE_SSD_TXN2
(4) PCIE_SSD_TXP2

EC-EVT-E04

(4) PCIE_SSD_RXP3
(4) PCIE_SSD_RXN3
(4) PCIE_SSD_TXN3
(4) PCIE_SSD_TXP3
(6) CLK_PCIE_SSD_N
(6) CLK_PCIE_SSD_P

+V3DX_SDD

EC-EVT-E04

R539 100K_5%_2

SSD_DET1

(6) SSD_DET1

SSD_DET1:
SSD_PCIE IF => Low

+V3DX_SDD

EC-EVT-E16

R77994 *10K_5%_2

DEVSLP1 (6)

DEVSLP[1] can be used for SATA Port 1 or 3

SSD_PLTRST_N

PCIE_SSD_CLKREQ0# (6)

+V3DX_SDD

R467 SSD@10K_5%_2 +V3DX_S0I3

+V3DX_SDD

C429 SSD@0.1u/16V_4

(20) SSD_PLTRST_N — SSD_PLTRST_N — R468 *SSD@100K_5%_2

U6425
NL17SZ08DFT2G

SSD_RST# (6)

+V3DX_S0I3 R78050 *0_5%_4 PLTRST_N (6,19,23)

R12149 *0_5%_4

EC-FVT-E20

PROJECT : LS3

Quanta Computer Inc.

BU2

Size	Document Number	Rev
	NGFF SSD M Key	1A

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PROJECT : LS3		
Quanta Computer Inc.		
Custom <Doc>	Size	Document Number
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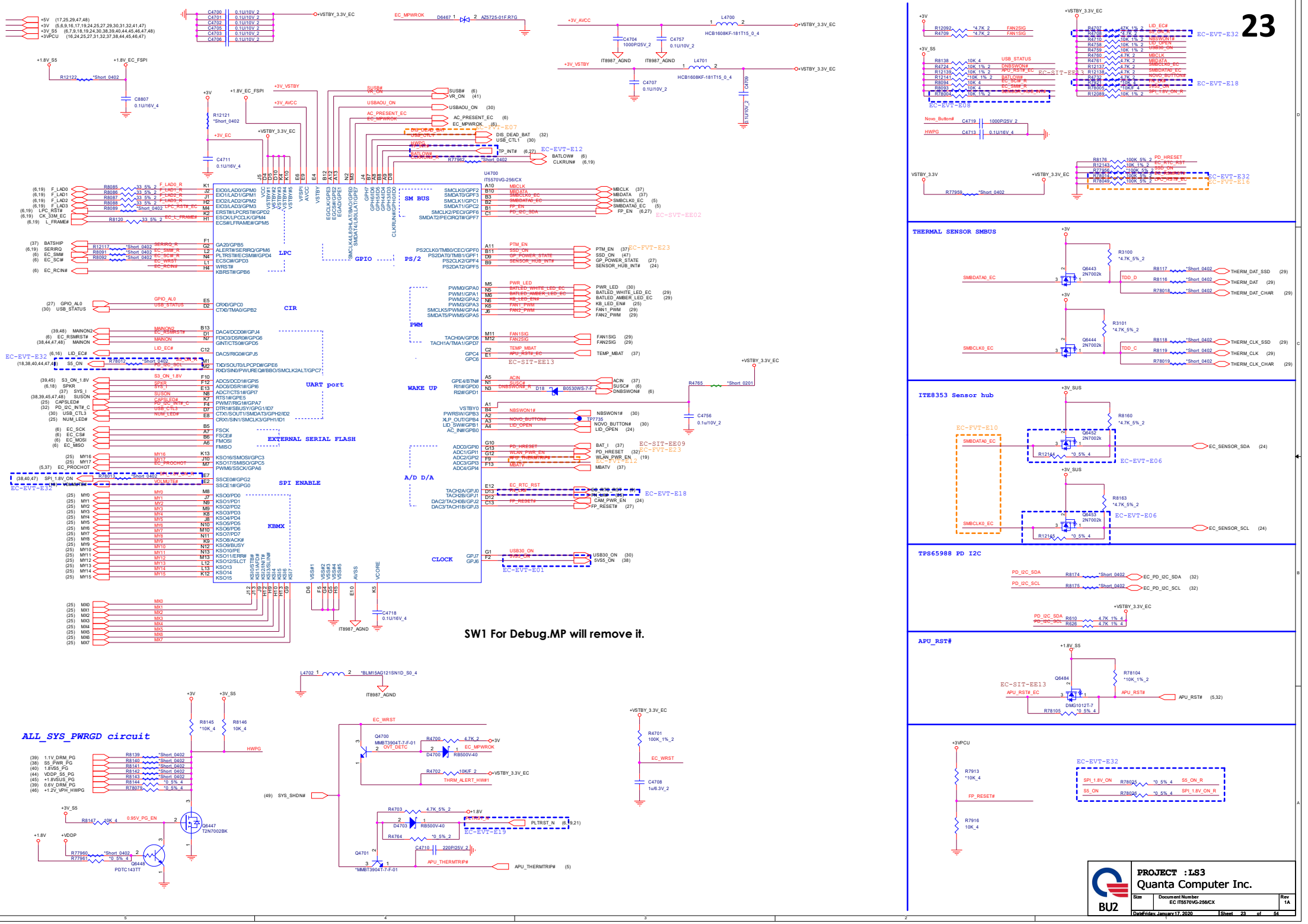
U4700
IT5570VG-256/CX
LPC
GPIO
SM BUS
PS/2
CIR
PWM
UART port
EXTERNAL SERIAL FLASH
WAKE UP
SPI ENABLE
A/D D/A
KBMX
CLOCK
SW1 For Debug.MP will remove it.
ALL_SYS_PWRGD circuit
THERMAL SENSOR SMBUS
ITE8353 Sensor hub
TPS65988 PD I2C
APU_RST#
PROJECT : LS3
Quanta Computer Inc.
BU2
Document Number
EC IT5570VG-256/CX
Rev 1A
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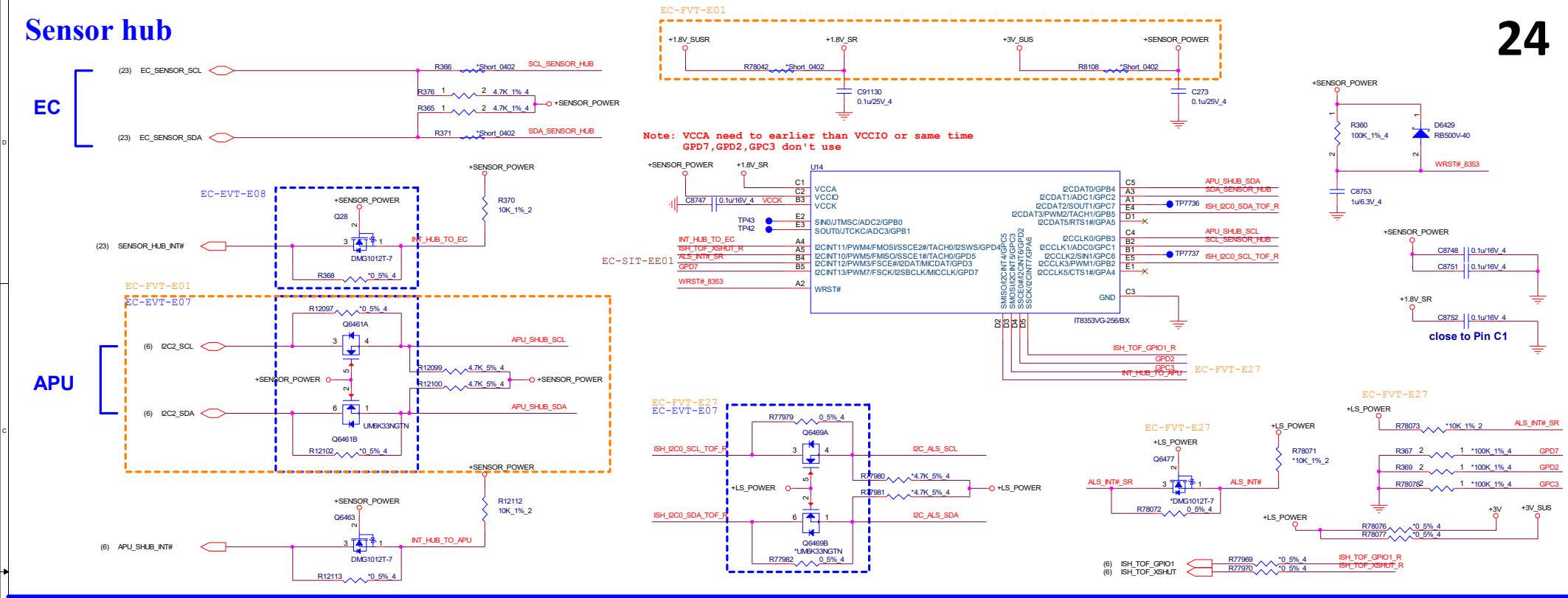
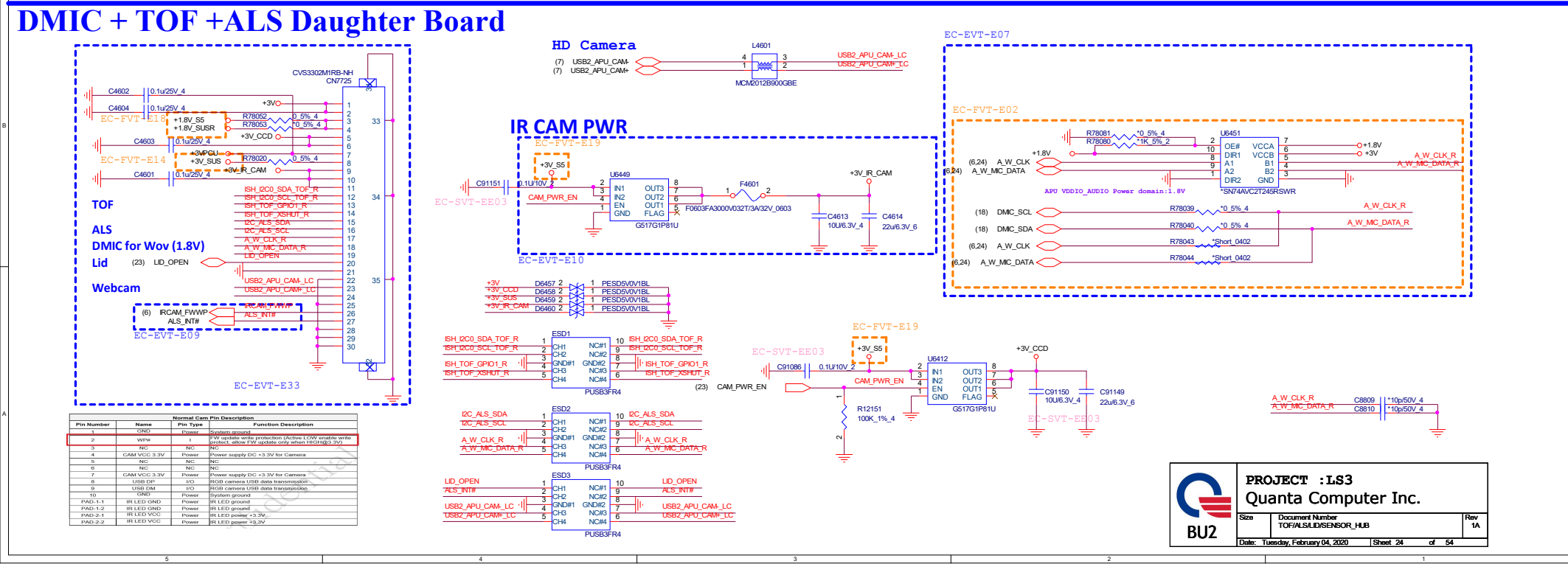
Sensor hub



DMIC + TOF +ALS Daughter Board

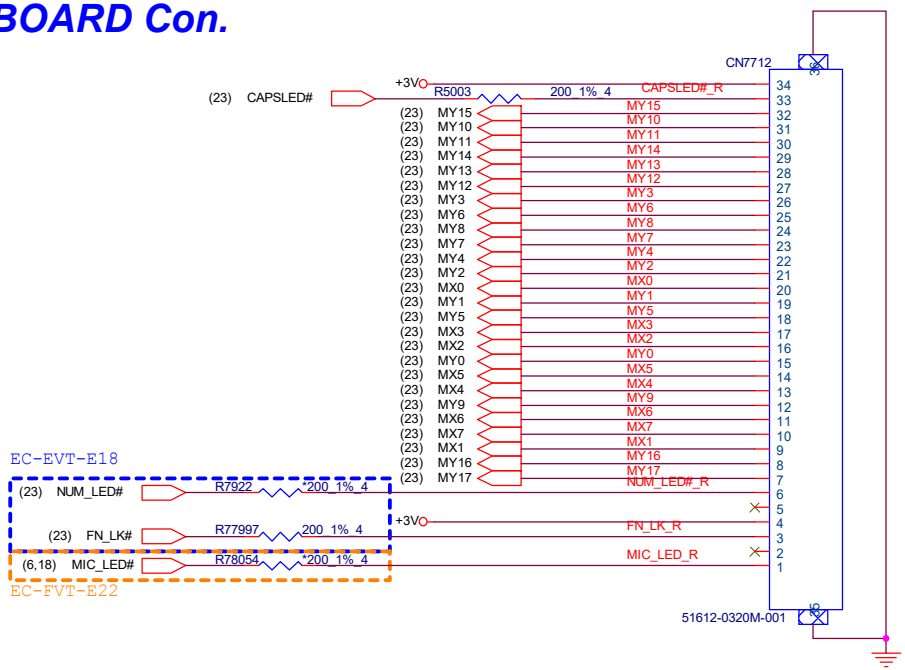


Normal Cam Pin Description			
Pin Number	Name	Pin Type	Function Description
1	GND	Power	System ground
2	WP#	I	FW update write protection (Active LOW enable write protect, allow F/W update only when HIGH@3.3V)
3	NC	NC	NC
4	CAM VCC 3.3V	Power	Power supply DC +3.3V for Camera
5	NC	NC	NC
6	NC	NC	NC
7	CAM VCC 3.3V	Power	Power supply DC +3.3V for Camera
8	USB DP	I/O	RGB camera USB data transmission
9	USB DM	I/O	RGB camera USB data transmission
10	GND	Power	System ground
PAD-1-1	IR LED GND	Power	IR LED ground
PAD-1-2	IR LED GND	Power	IR LED ground
PAD-2-1	IR LED VCC	Power	IR LED power +3.3V
PAD-2-2	IR LED VCC	Power	IR LED power +3.3V

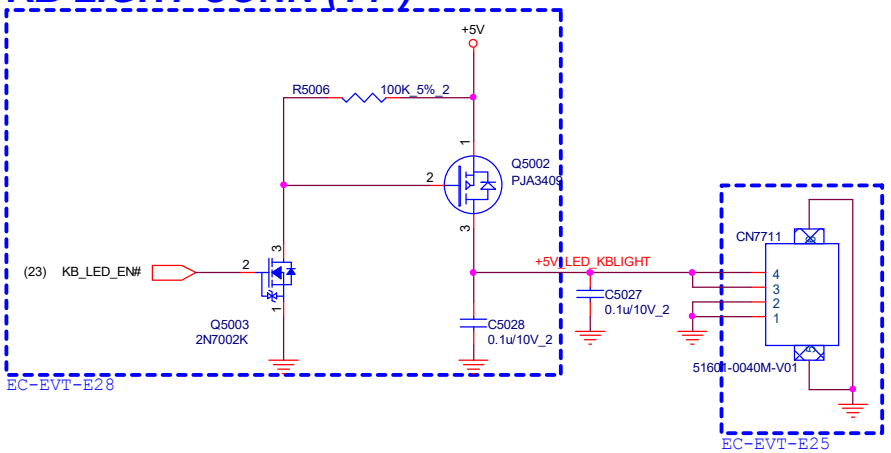
BU2	PROJECT : LS3 Quanta Computer Inc. Size: — Document Number: TOF/ALS/LID/SENSOR_HUB — Rev: 1A Date: Tuesday, February 04, 2020 — Sheet 24 of 54

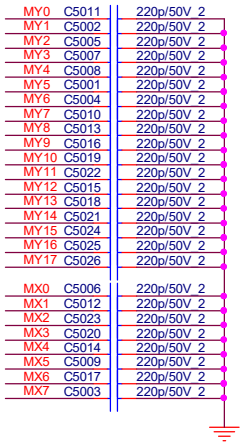
+3V_S5 (6,7,9,18,19,23,24,30,38,39,40,44,45,46,47,48)
+3V (5,6,9,16,17,19,23,24,27,29,30,31,32,41,47)
+5V_S5 (17,18,27,29,30,32,38,41,42,45,47)

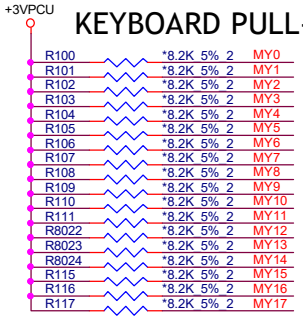
KEYBOARD Con.



KB LIGHT CONN (14")







BU2

PROJECT : LS3
Quanta Computer Inc.

Size	Document Number	Rev
	Kerboard/Keyboard Backlight	1A
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BU2	Size: Document Number: Discrete TPM	Rev: 1A
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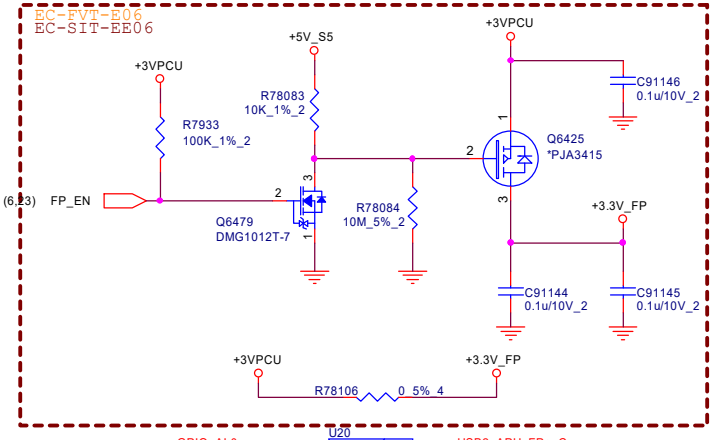
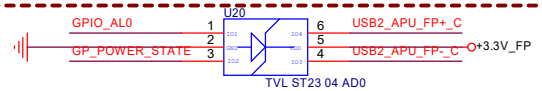
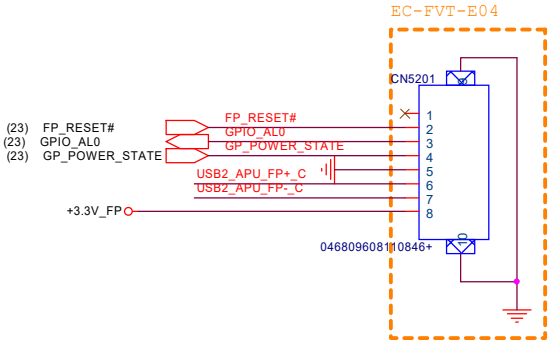
Finger print

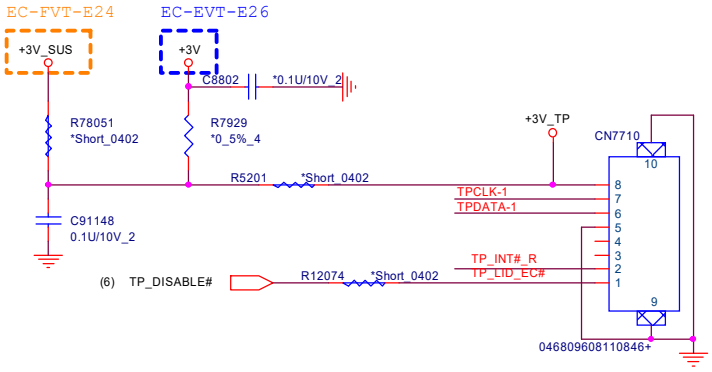


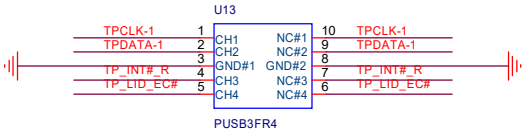


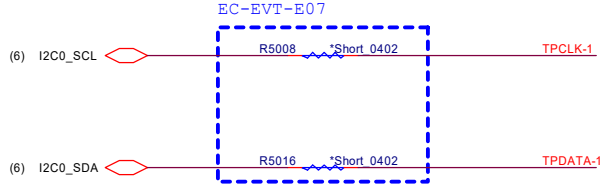


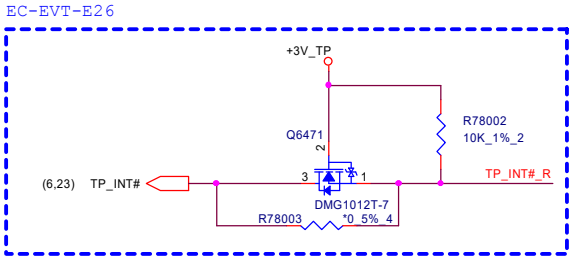
Pin No.	Symbol	Description
1	LED	LED SINGNAL
2	RESETN	MCU RESETN SINGAL
3	GPIO_AL0	POWER SHIELD
4	DELINK	POWER STATUS
5	DGND	GROUND
6	DP	USB DATA+
7	DM	USB DATA-
8	D3V3	POWER 3.3V

Touch Pad









Pin Number	Pin Name	Description
1	VDD	Power
2	I2C-CLK	I2C Clock
3	I2C-DAT	I2C Data
4	GND	Ground
5	NC	NC
6	NC	NC
7	ATTN	Attention
8	GPIO for LID CLOSE	LID Close

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BU2

PROJECT : LS3

Quanta Computer Inc.

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	Touch Pad/Fingerprint	1A

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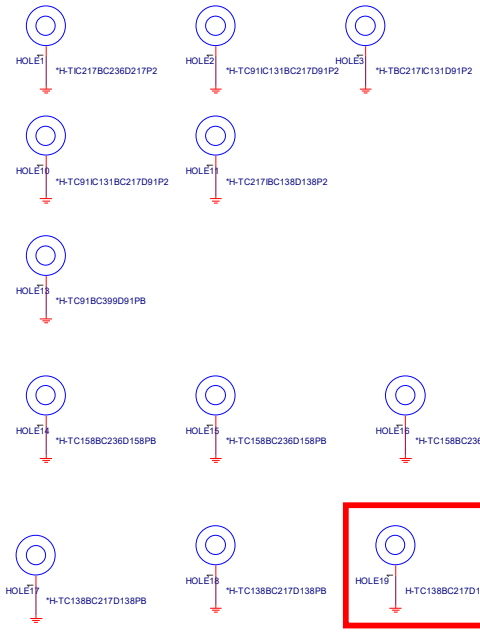
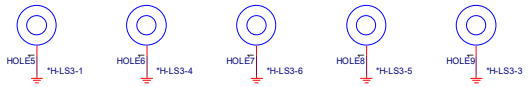
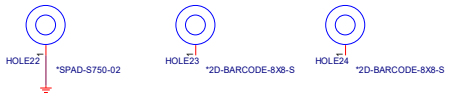
HOLE

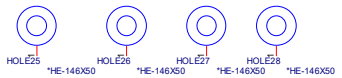


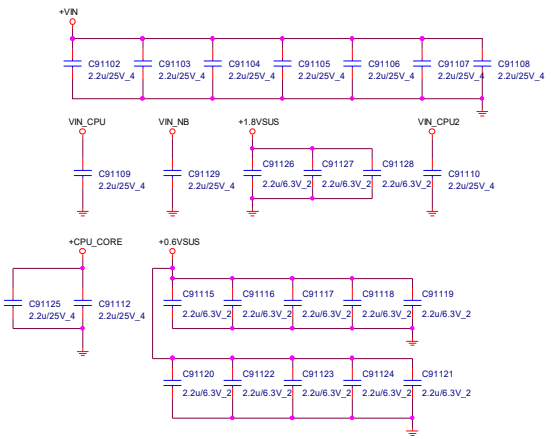
WLAN Nut

SSD Nut









Custom	PROJECT : LS3 Quanta Computer Inc.	
BU2	Size: HOLE	Document Number:	Rev: 1A
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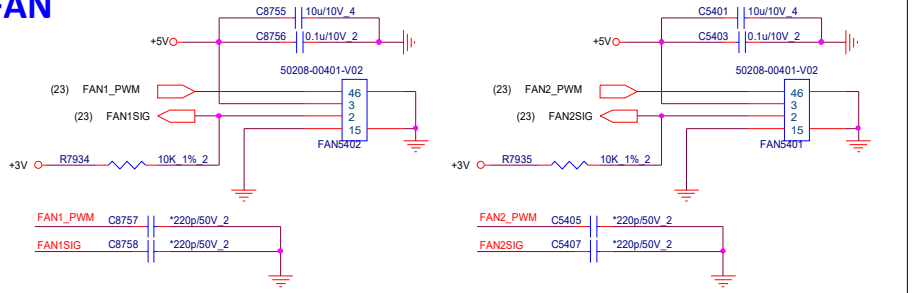
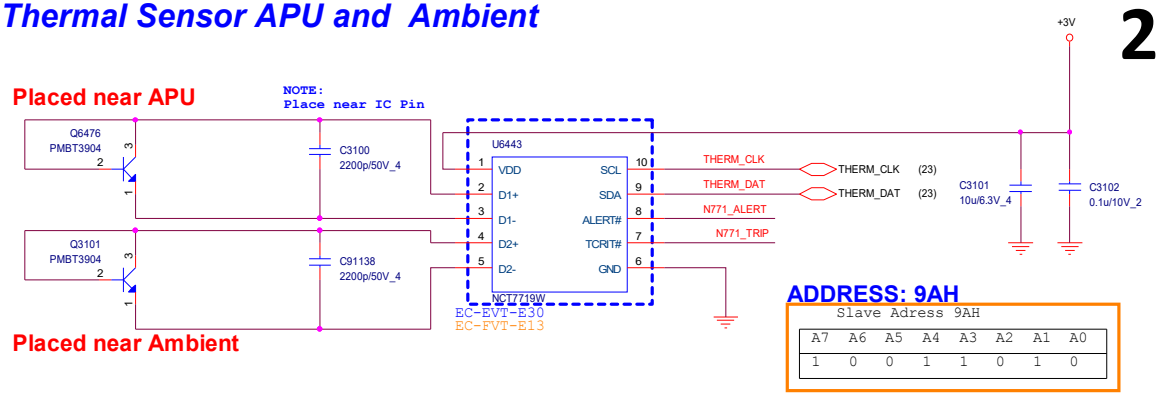
FAN



Thermal Sensor APU and Ambient

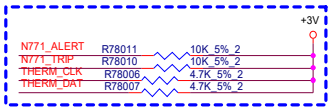


ADDRESS: 9AH

Slave Adress 9AH

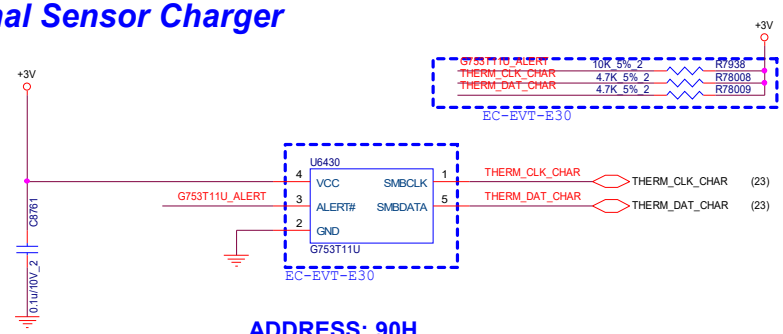
A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	1	1	0	1	0

EC-EVT-E30



GMT	G753T11U		90h	AL000753000
Nuvoton	NCT7719W	SMBus Address	9Ah	AL007719000
GMT	G751-2P8F	SMBus Address	92h	AL000751016
GMT	G781-1P8	SMBus Address	9Ah	AL000781039

Thermal Sensor Charger

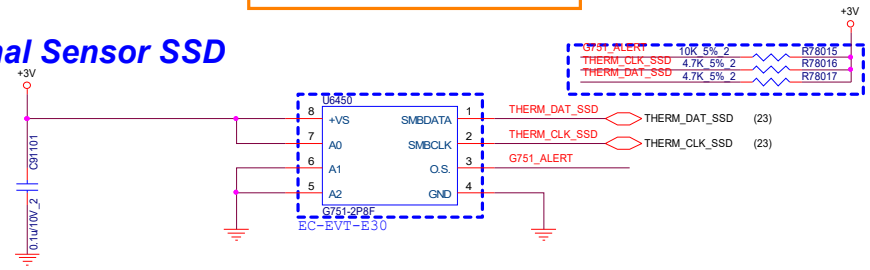


ADDRESS: 90H

Slave Adress 90H

A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	1	0	0	0	0

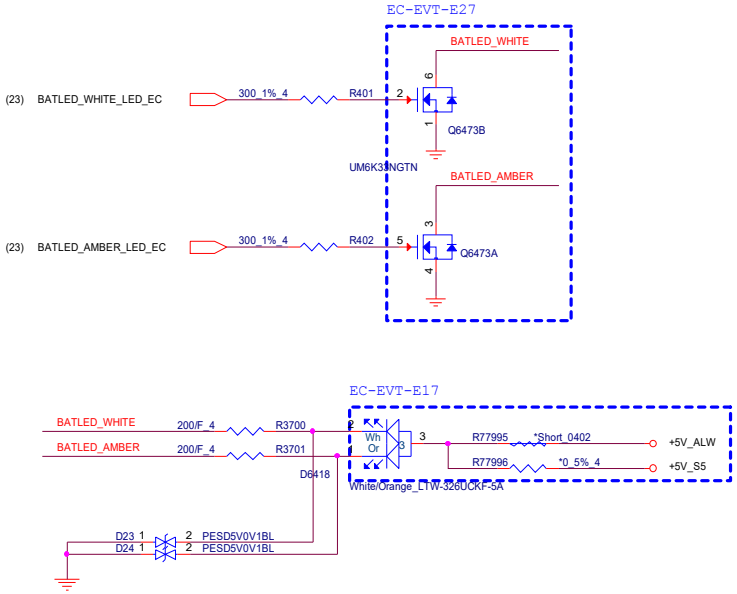
Thermal Sensor SSD



ADDRESS: 92H

Slave Adress 92H

						A1	A0
1	0	0	1	0	0	1	0



BU2

PROJECT : LS3

Quanta Computer Inc.

Size	Document Number	Rev
	FAN/Thermal Sensor	1A

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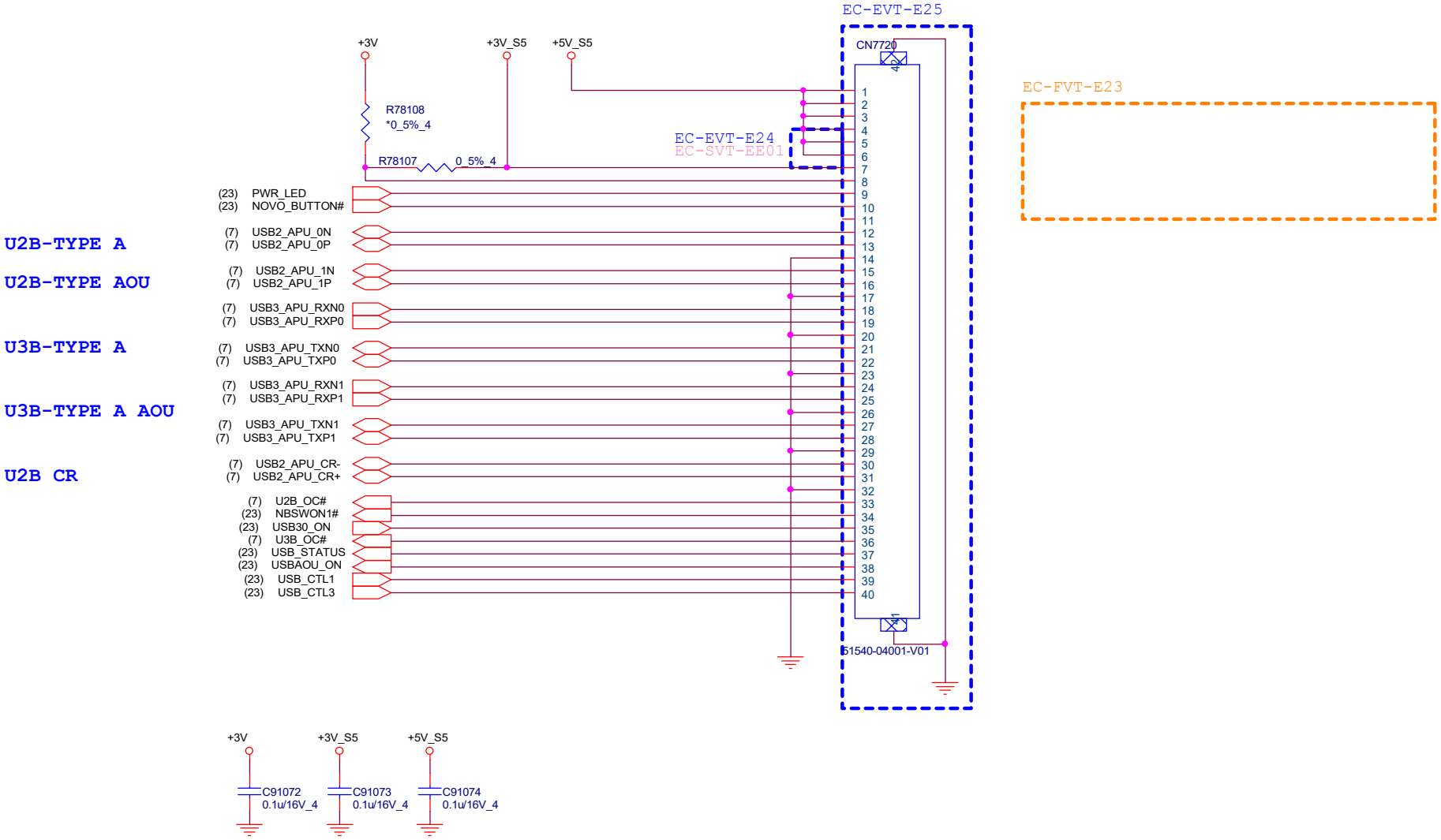
USB3+SD Daughter Board



Custom	PROJECT : LS3 Quanta Computer Inc.	
BU2	Size: Document Number: USB3+SD Daughter Board conn	Rev: 1A
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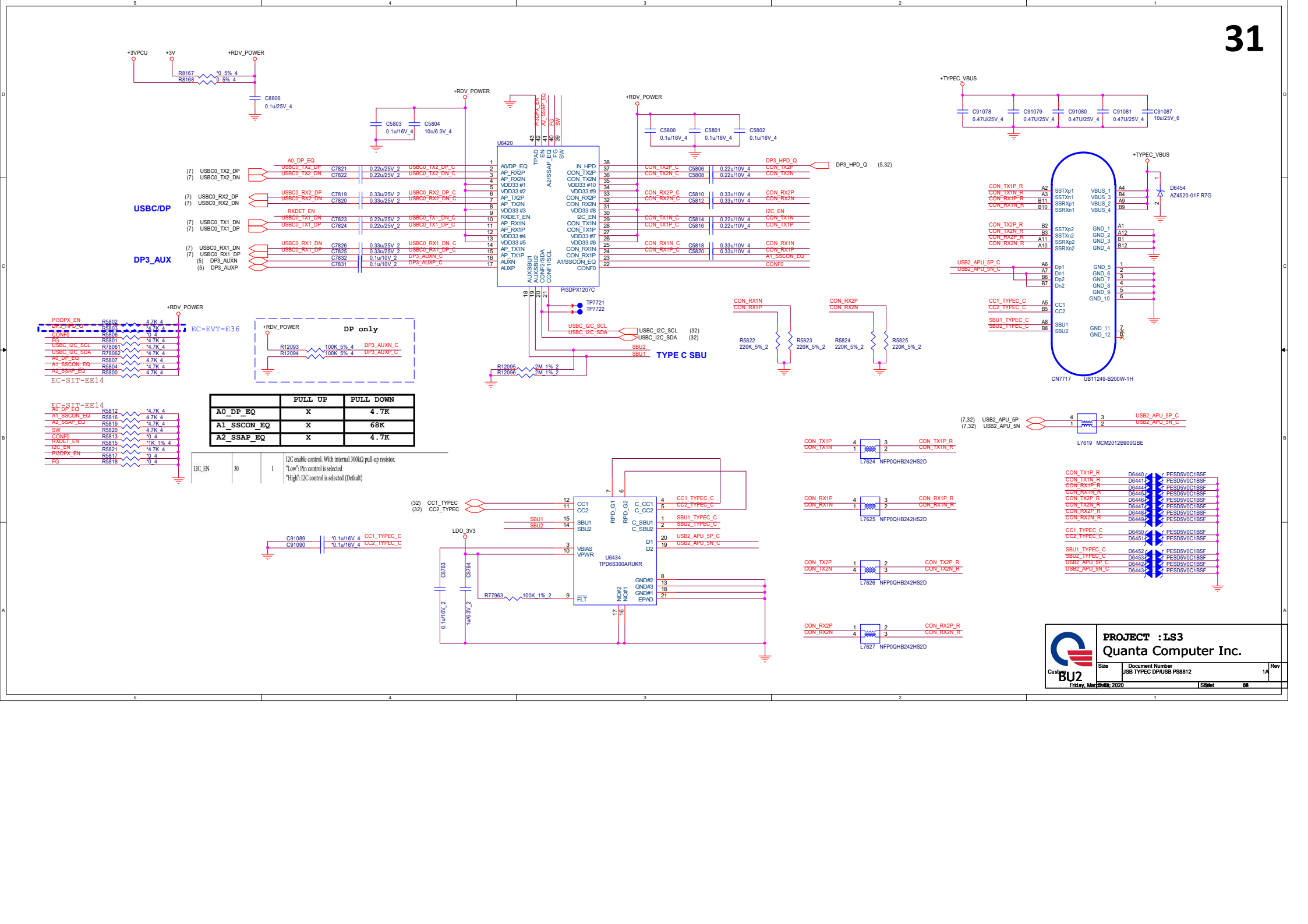
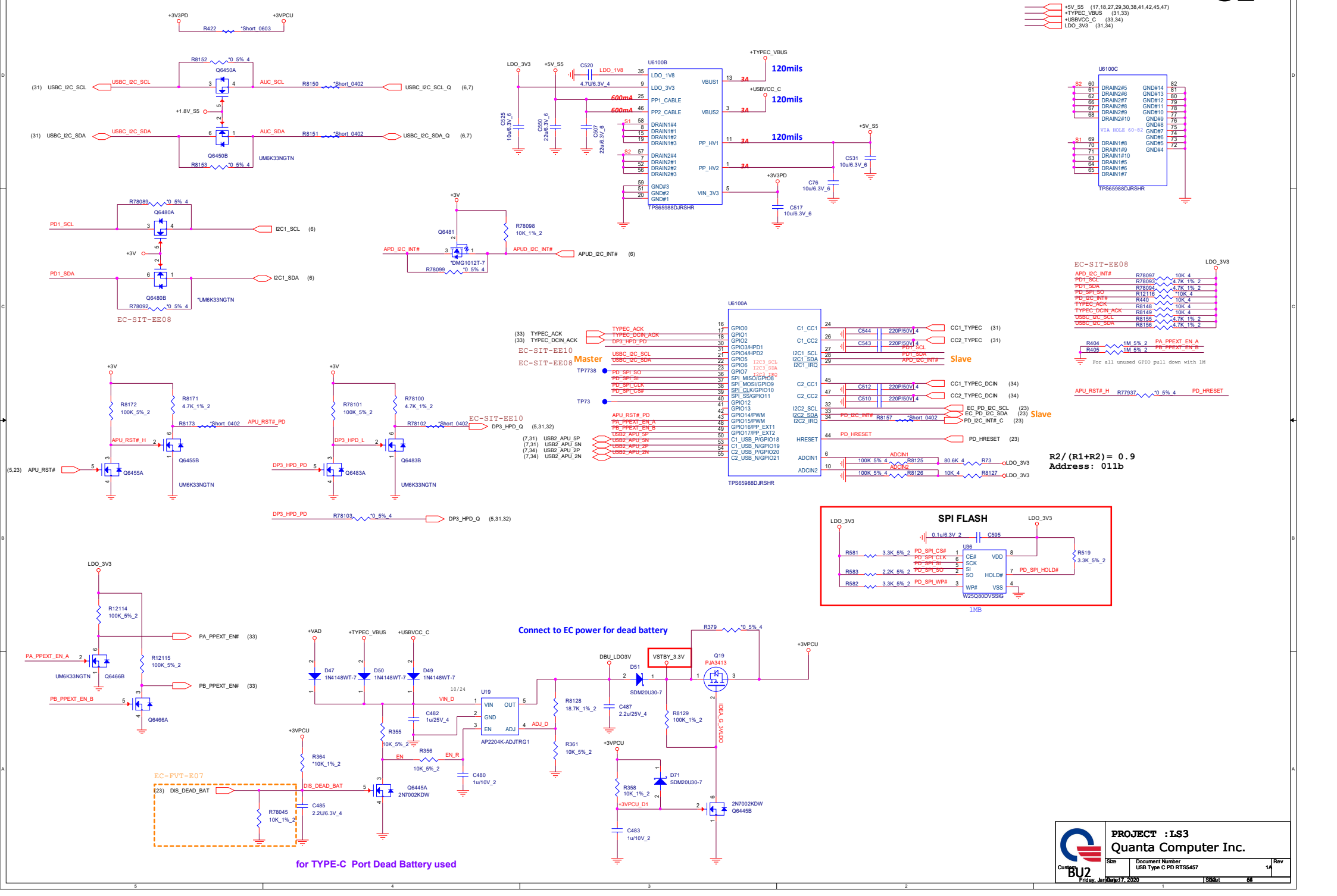


	PULL UP	PULL DOWN
A0_DP_EQ	X	4.7K
A1_SSCON_EQ	X	68K
A2_SSAP_EQ	X	4.7K

I2C_EN	30	I	I2C enable control. With internal 300kΩ pull-up resistor. "Low": Pin control is selected "High": I2C control is selected (Default)

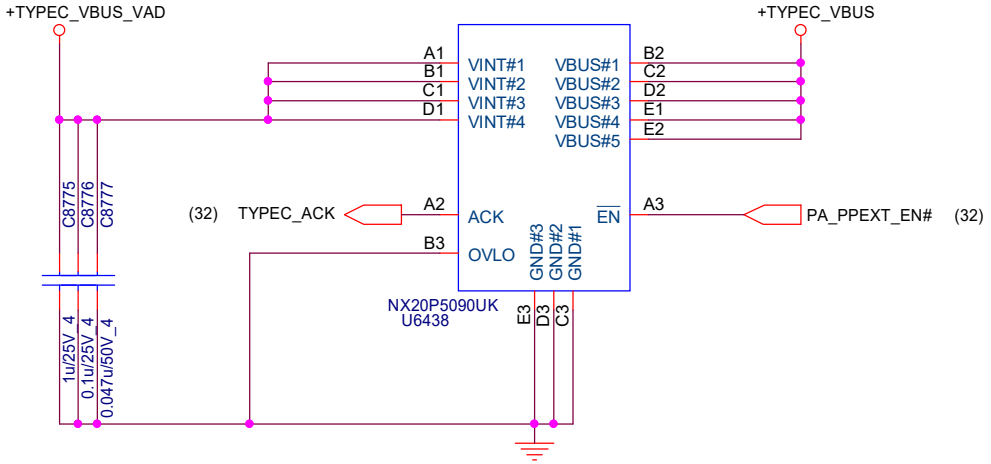
PROJECT :LS3
Quanta Computer Inc.
Custom BU2
Size: Document Number: USB TYPEC DP/USB PS8812 Rev: 1A
Date: Friday, March 13, 2020 Sheet 68

USB TYPEC PD



Quanta Computer Inc.	PROJECT : LS3		
Custom BU2	Size	Document Number USB Type C PD RTS5457	Rev 1A
Date: Friday, January 17, 2020	Sheet	of	

TYPE-C Load Switch



TYPE-C ADP Load Switch

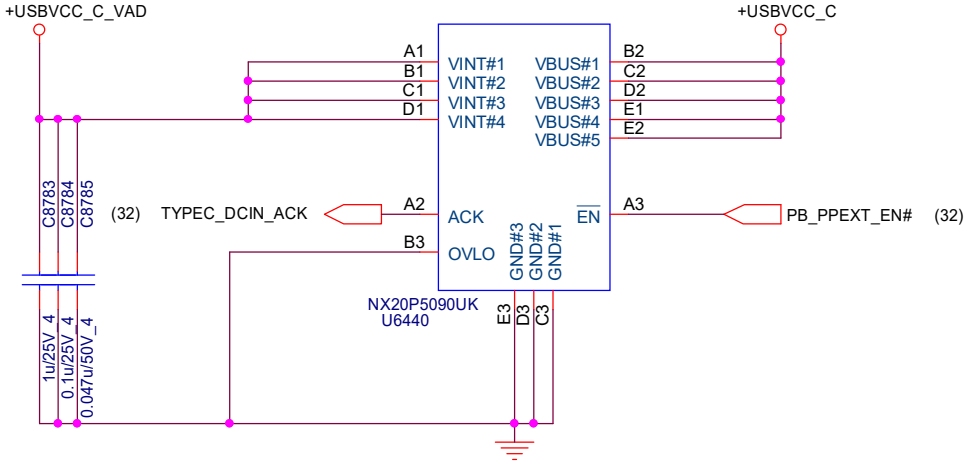


Table 4. Function table[1]

$\overline{EN}$	VBUS	VINT	ACK	Operation mode
L	< 2.5 V	X	Z	Under-voltage lockout; switch open
L	2.5 V < VBUS < V_{OVLO}	X	L	Enabled; switch closed; charging mode
L	X	X	Z	Over-temperature protection; switch open
L	> V_{OVLO}	X	Z	Over-voltage lockout; switch open
H	X	X	Z	Disable; switch open
X	X	VINT>VBUS	Z	Reverse Current Protection; Switch open

[1] H = HIGH voltage level; L = LOW voltage level, Z = high-impedance OFF-state.

8.5 ACK output

The ACK output is an open-drain output that requires an external pull-up resistor. ACK pin indicates the state of the power switch, when no fault is detected and power switch is conducting, ACK will output low, otherwise it will stay at high impedance. The pull up resistor value is recommend to be 10KΩ to 200KΩ.

BU2

PROJECT : LS3
Quanta Computer Inc.

Size	Document Number	Rev
	Load Switch for Power Delivery	1A
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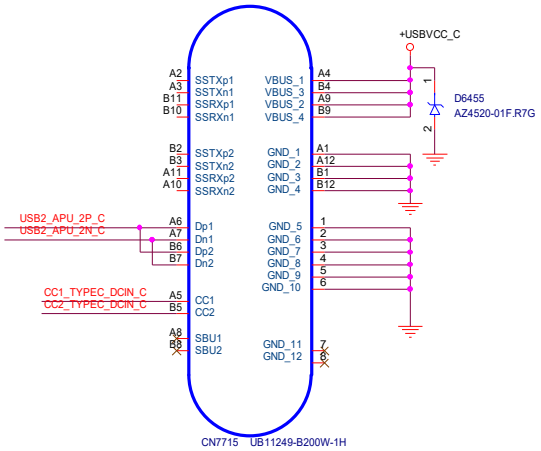
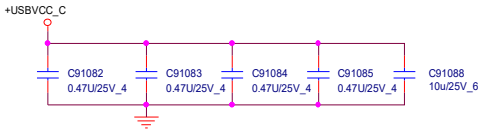
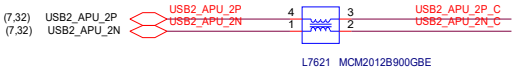
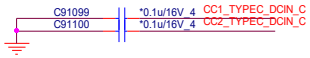
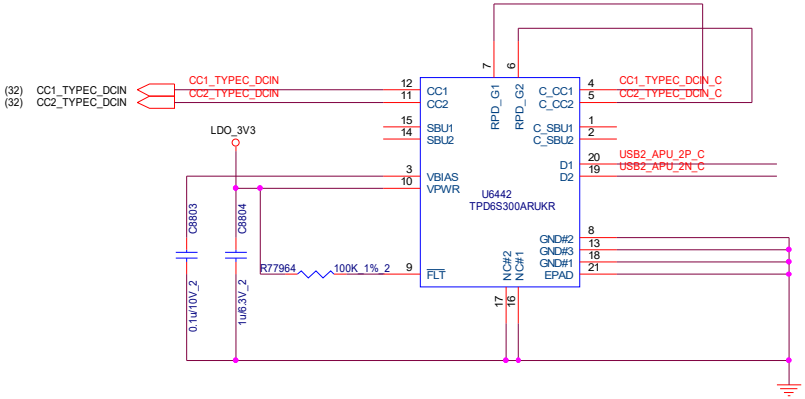
USB TYPEC PD-DCIN ONLY

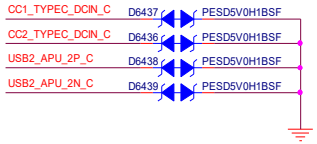












PROJECT : LS3

Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB Type C PD RTS5457	1A
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TYPE-C ADP Load Switch

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A	BU2	PROJECT : LS3 Quanta Computer Inc.
Size	Document Number TYPE-C ADP Load Switch	Rev 1A
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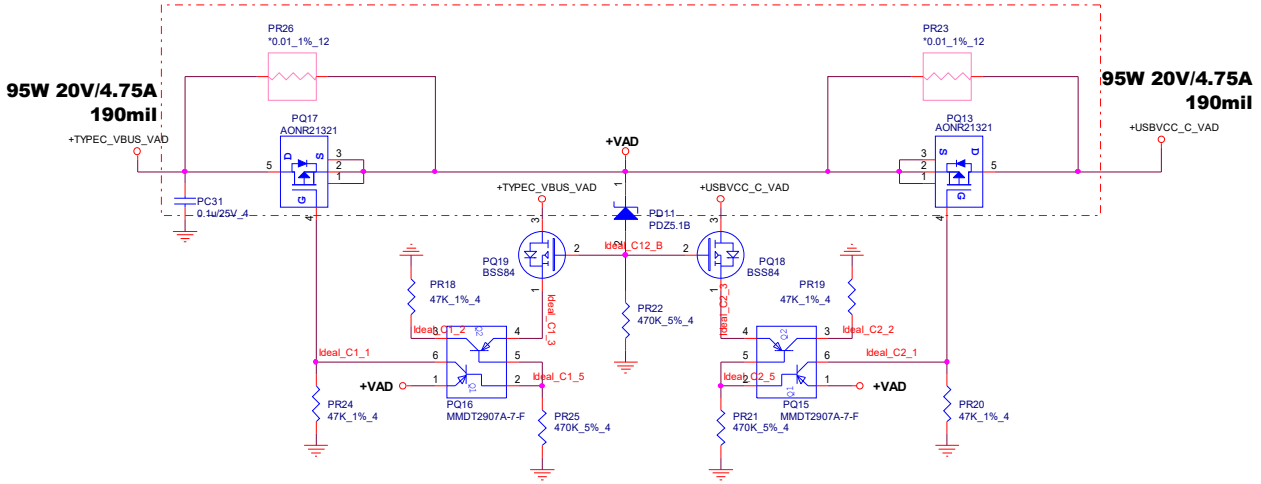

BU5

PROJECT : X36A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	TYPEC load switch MOSFET	1A
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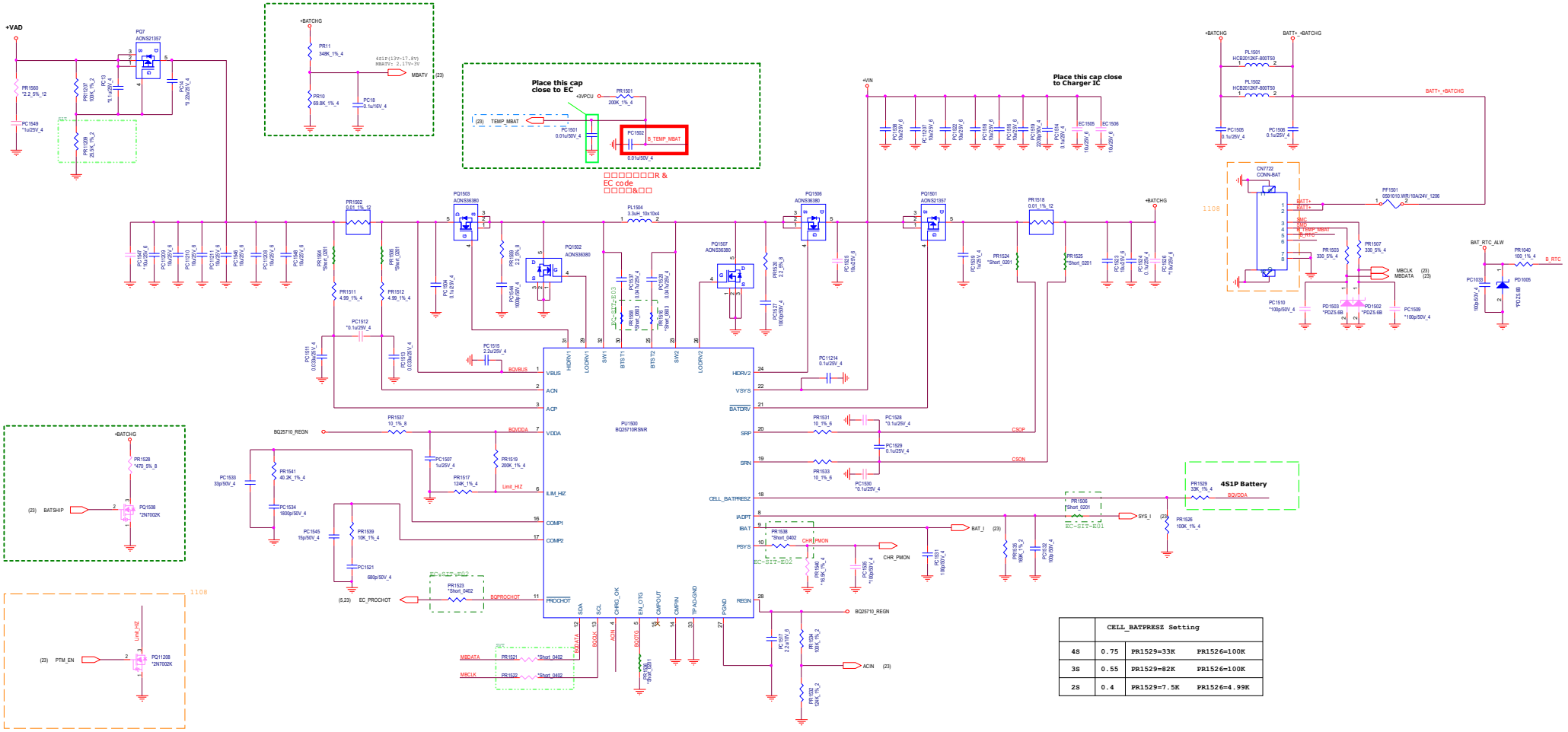

	CELL_BATPRESZ Setting	
4S	0.75	PR1529=33K PR1526=100K
3S	0.55	PR1529=82K PR1526=100K
2S	0.4	PR1529=7.5K PR1526=4.99K

PROJECT : LVC
Quanta Computer Inc.
Custom BU2
Size
Document Number Charger (BQ25710RSNR)
Rev 1A
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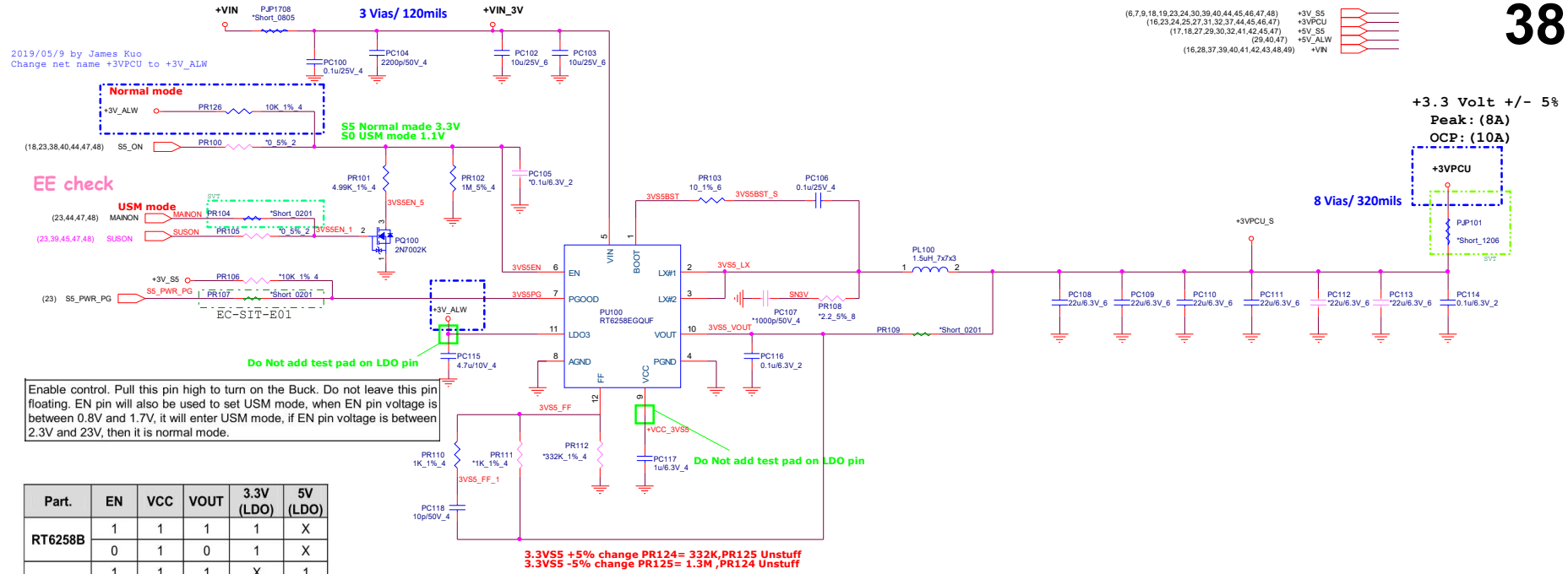
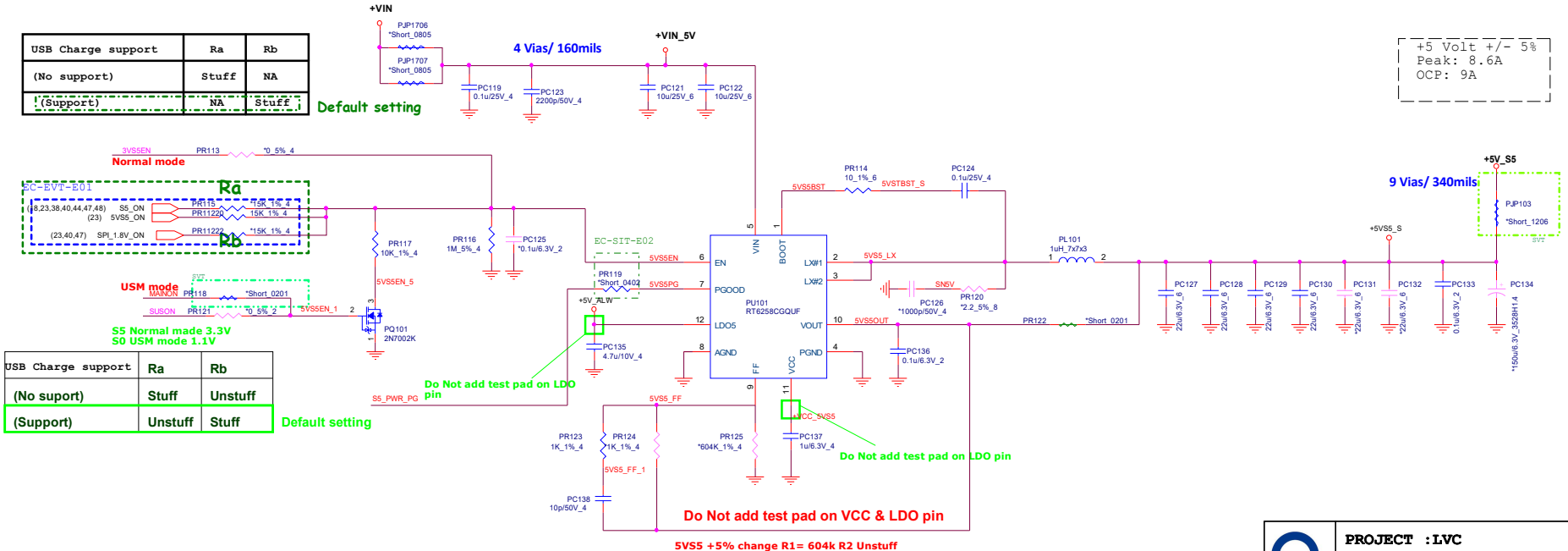


Enable control. Pull this pin high to turn on the Buck. Do not leave this pin floating. EN pin will also be used to set USM mode, when EN pin voltage is between 0.8V and 1.7V, it will enter USM mode, if EN pin voltage is between 2.3V and 23V, then it is normal mode.

Part.	EN	VCC	VOUT	3.3V (LDO)	5V (LDO)
RT6258B	1	1	1	1	X
	0	1	0	1	X
RT6258C	1	1	1	X	1
	0	1	0	X	1



USB Charge support	Ra	Rb
(No suport)	Stuff	Unstuff
(Support)	Unstuff	Stuff

Default setting

PROJECT :LVC
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+3/5VS5 (RT6256B/RT6258C)	1A
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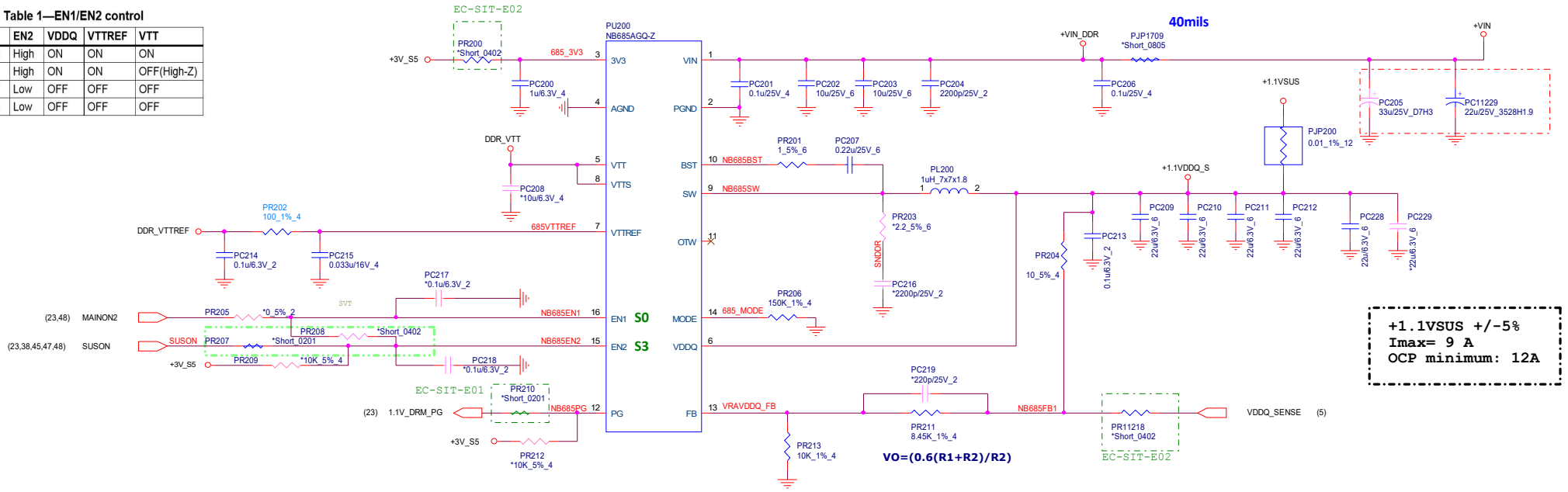
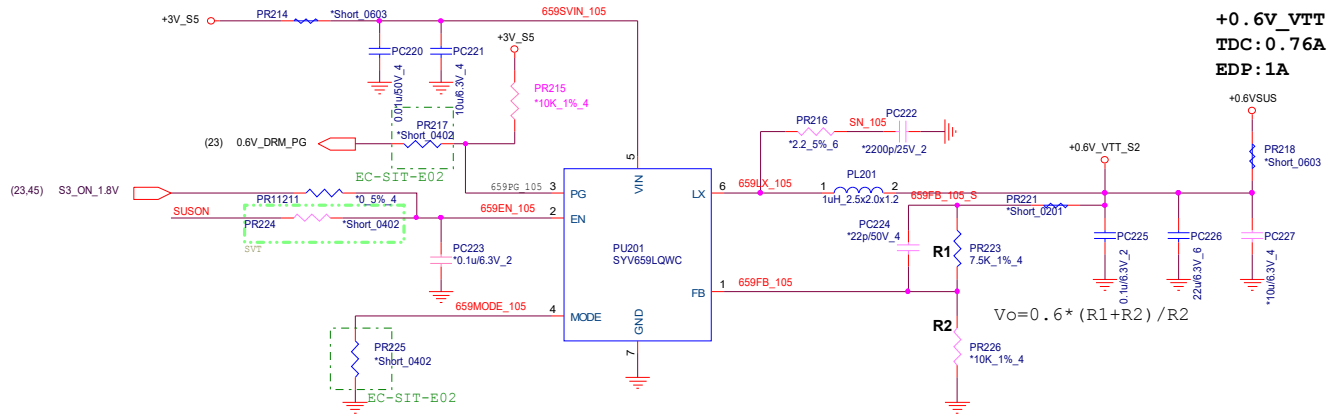
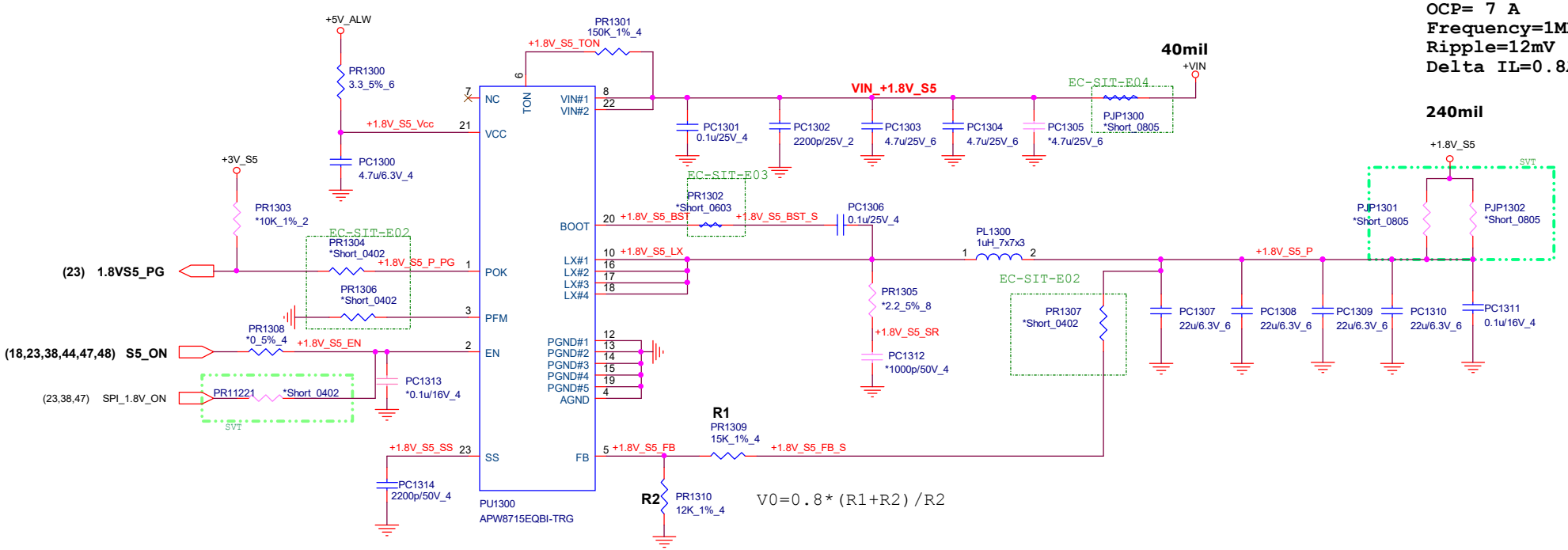
Table 1—EN1/EN2 control

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF





+1.8V_S5
Imax= 3.7A
OCP= 7 A
Frequency=1MHz
Ripple=12mV
Delta IL=0.8A



HP Restricted Secret

Quanta Computer Inc.
Project: HP-MONK-P/D

Title		
+1.8V_S5		
Size	Document Number	Rev
	--	A1A
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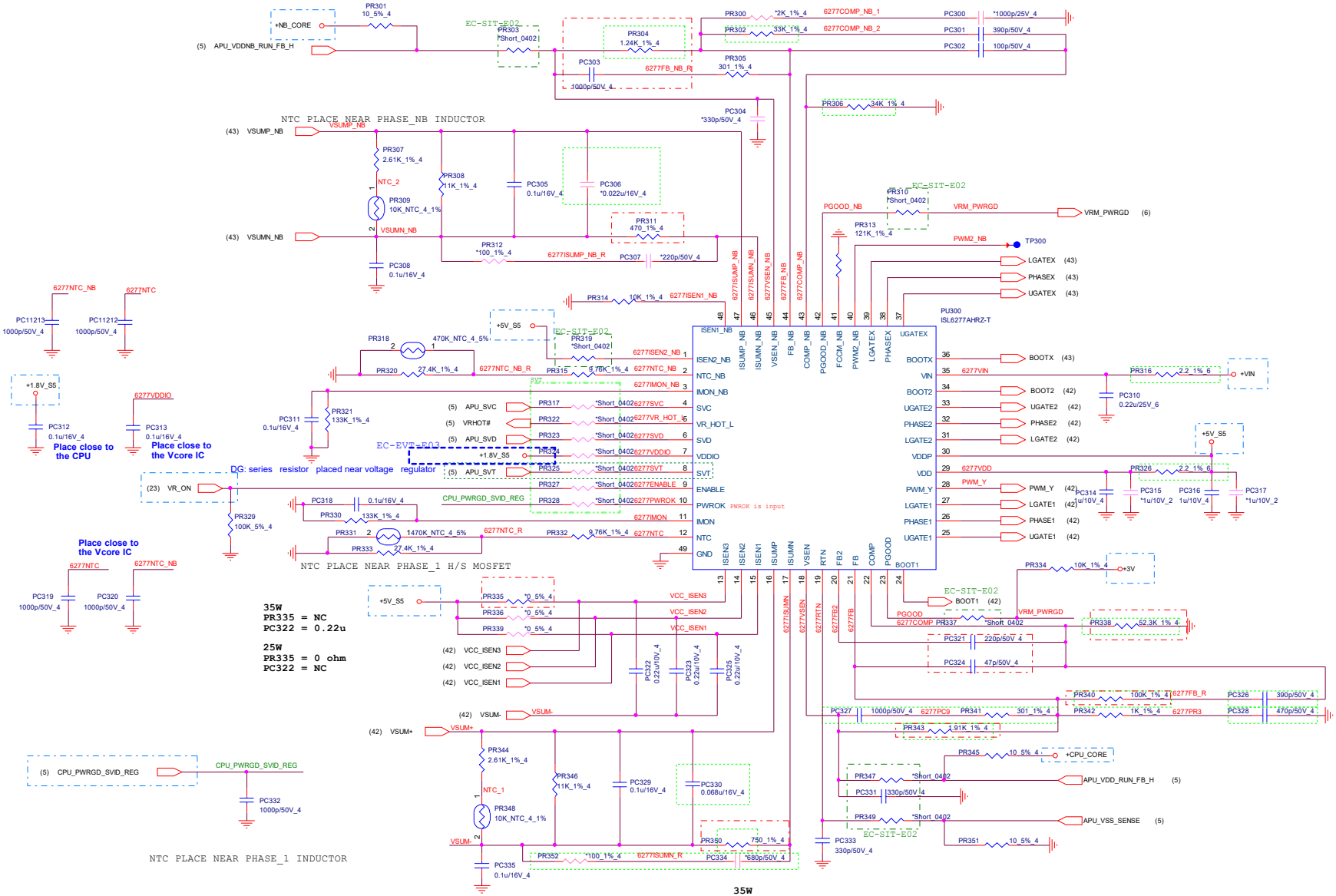
NOTE : □□□□□□□□□ , □□□□□□□ , □□□□□FAE□□□□□Low line & OCP & RC time constant
1. EN□□ & VID & VRHOT# & PG net name & pull high □EE□□□□□EE□□□□□
2. Pull high & Output name□□□□□EE□□

□□□□□□□□
□□□□□DB□□□□□□□

CPU_CORE
NB_CORE
(17,18,27,29,30,32,38,42,45,47) +5V_S5
(5,9,23,24,47,48) +1.8V
(5,6,9,16,17,19,23,24,25,27,29,30,31,32,47) +3V
(16,28,37,38,39,40,42,43,48,49) +VIN

VCORE/VDDNB (ISL6277AHRTZ-T and ISL6208CRZ-T)



Quanta Computer Inc.
Project:

Title		
CPU_CORE (ISL6277AHRZ-T)		
Size	Document Number	Rev
	--	A
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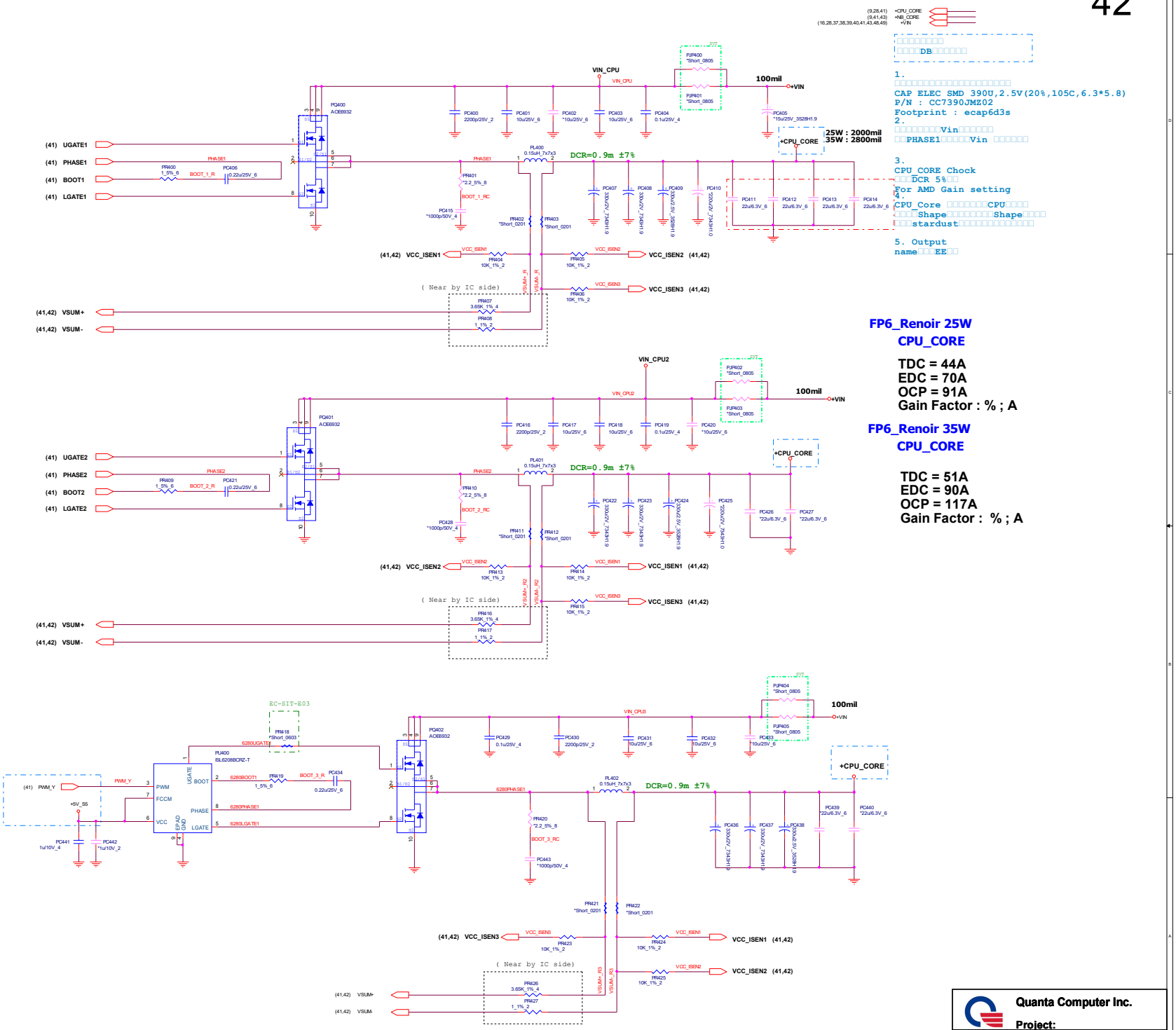

(9,28,41) +CPU_CORE
(9,41,43) +NB_CORE
(16,28,37,38,39,40,41,43,48,49) +VIN

1.
CAP ELEC SMD 390U,2.5V(20%,105C,6.3*5.8)
P/N : CC7390JMZ02
Footprint : ecap6d3s
2.
Vin
PHASE1 Vin
3.
CPU_CORE Chock
DCR 5%
For AMD Gain setting
4.
CPU_Core CPU
Shape Shape
stardust
5. Output
name EE

FP6_Renoir 25W
CPU_CORE

TDC = 44A
EDC = 70A
OCP = 91A
Gain Factor : % ; A

FP6_Renoir 35W
CPU_CORE

TDC = 51A
EDC = 90A
OCP = 117A
Gain Factor : % ; A

Quanta Computer Inc.	Project:		
Title: CPU core 3Phase			
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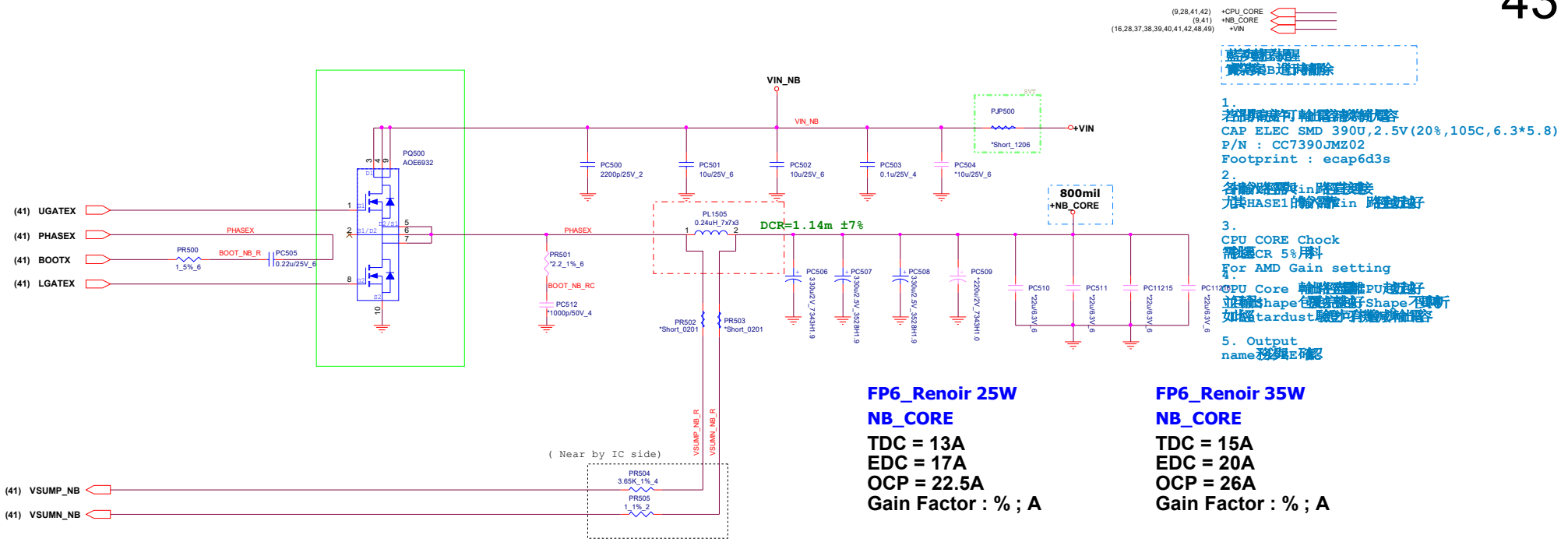

FP6_Renoir 25W

NB_CORE

TDC = 13A
EDC = 17A
OCP = 22.5A
Gain Factor : % ; A

FP6_Renoir 35W

NB_CORE

TDC = 15A
EDC = 20A
OCP = 26A
Gain Factor : % ; A

Quanta Computer Inc.

Project:

Title: NB core 1Phase

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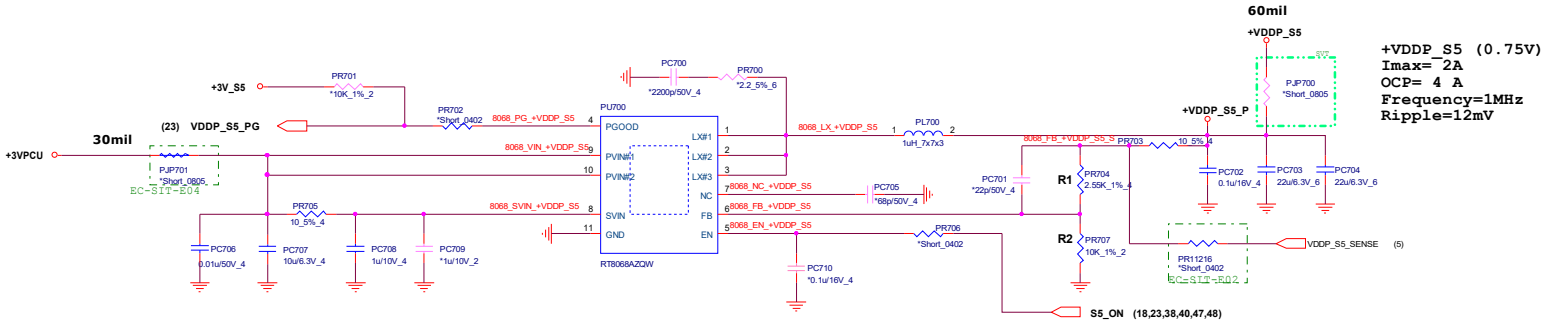
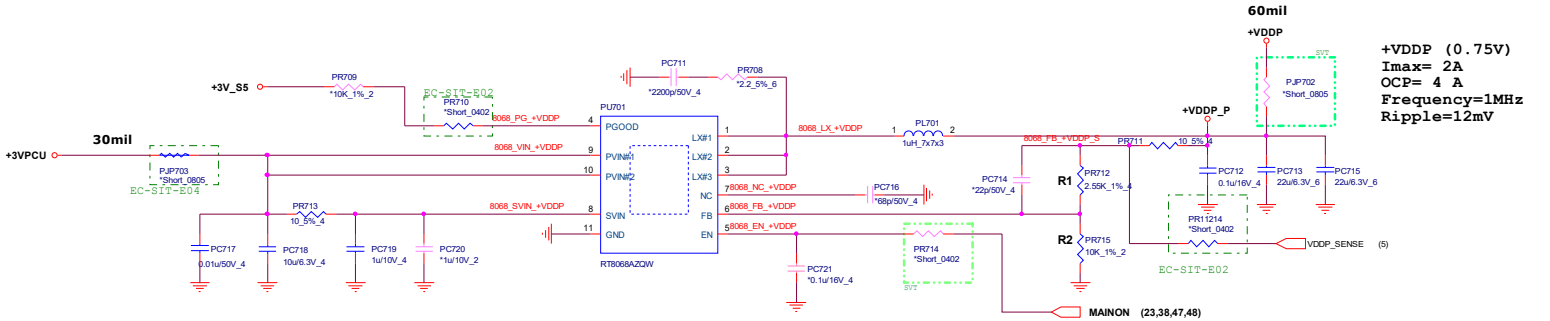
(6,7,9,18,19,23,24,30,38,39,40,45,46,47,48)
(17,18,27,29,30,32,38,41,42,45,47)
(16,28,37,38,39,40,41,42,43,48,49)
(9,48)
(5,9,23,48)

+3V_S5
+5V_S5
+VIN
+VDDP_S5
+VDDP



V0=0.6*(R1+R2)/R2



V0=0.6*(R1+R2)/R2

Quanta Computer Inc.
Project: HP-MONK-P/D

Title: **+VDDP (RT8068 & AOZ2261)**

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	--	A1A

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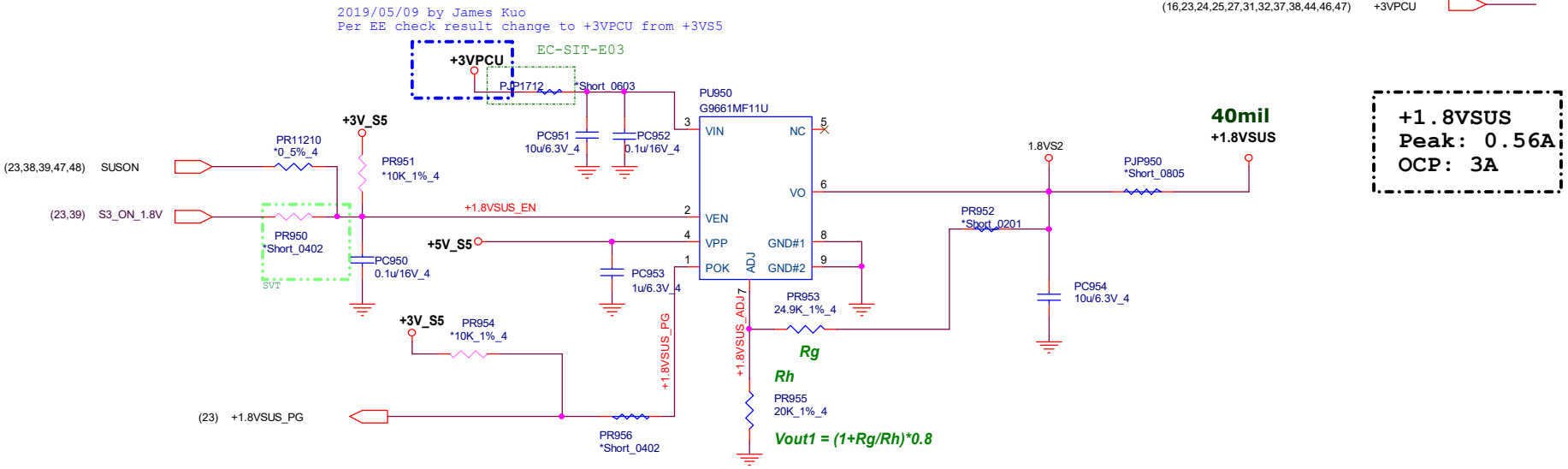
(11,12,13,14,28) +1.8VSUS
(17,18,27,29,30,32,38,41,42,47) +5V_S5
(6,7,9,18,19,23,24,30,38,39,40,44,46,47,48) +3V_S5
(16,23,24,25,27,31,32,37,38,44,46,47) +3VPCU



6.1. Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Core Power 1	VDD1	1.70	1.80	1.95	V	1,2
Core Power 2 & CA Power	VDD2	1.06	1.10	1.17	V	1,2,3
I/O Buffer Power	VDDQ	0.57	0.60	0.65	V	2,3

1. While applying power (after Ta), RESET_n is recommended to be LOW (≤0.2 x VDD2) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table "Voltage Ramp Conditions". VDD1 must ramp at the same time or earlier than VDD2. VDD2 must ramp at the same time or earlier than VDDQ.

Table - Voltage Ramp Conditions

After...	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2
	VDD2 must be greater than VDDQ - 200mV

PROJECT : LVC
Quanta Computer Inc.

Size	Document Number	Rev
B	+1.8V_GFX(RT8068)/+3V_GFX	1A

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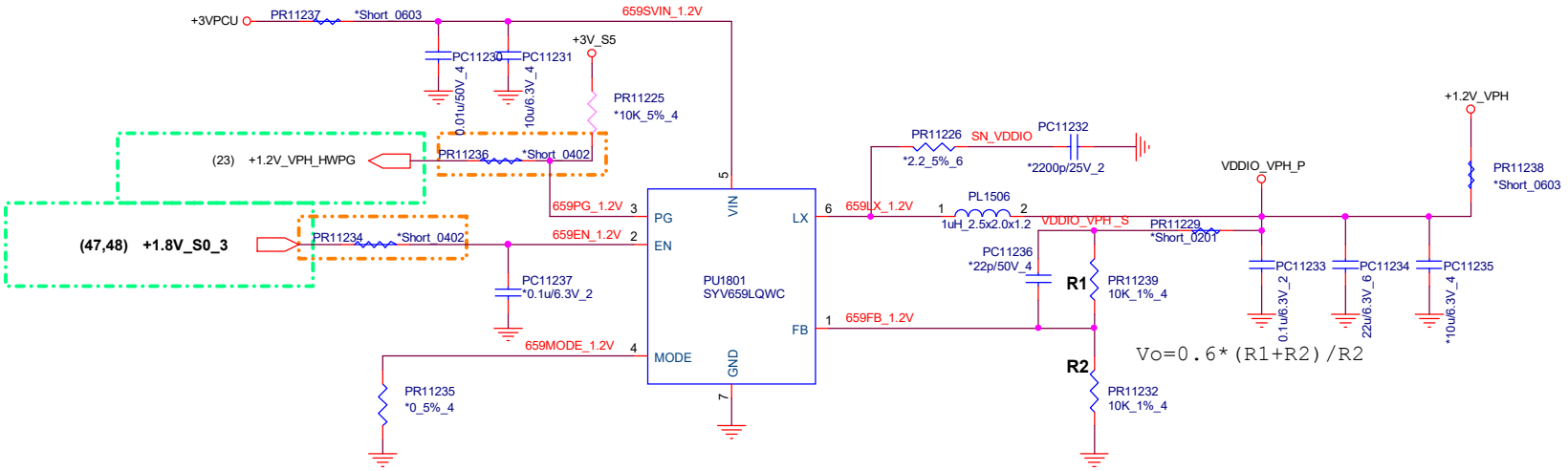
+1.2V_VDDIO_VPH
Peak:1A
OCP: 3A



Custom	**PROJECT : LVC** Quanta Computer Inc.	
BU2	Size: — Document Number: +1.8V_S5 (RT8068AZQW)	Rev: 1A
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(17,25,29,48) +5V
(5,6,9,16,17,19,23,24,25,27,29,30,31,32,41) +3V
(5,6,9,18,23,24,32,40,41,48) +1.8V_S5
(5,9,23,24,48) +1.8V
(6,7,9) +1.8V_S5_ROM
(17,18,27,29,30,32,38,41,42,45) +5V_S5
(6,7,9,18,19,23,24,30,38,39,40,44,45,46,48) +3V_S5
(16,23,24,25,27,31,32,37,38,44,45,46) +3VPCU
(20,21) +3V_SSD

2019/05/09 by James Kuo
Change +3VPCU from +3VS5

4A

+3V
PJP1208 *Short_0805
+3V_R
PC1244 *10u/6.3V_4
PC1250 0.1u/6.3V_2
+5V_ALW
PC1251 0.1u/6.3V_2
PC1253 0.1u/6.3V_2
PC1263 0.1u/6.3V_2
+3VPCU
+5V_S5
PU1204 TPS22976DPUR
VIN1#1 VIN1#2 VIN2#1 VIN2#2
VOUT1#1 VOUT1#2 OUT2#1 OUT2#2
VBIAS GND#1 GND#2 ON1 ON2 CT1 CT2
2.5A
PJP1202 *Short_0805 +5V
PC1211 0.1u/6.3V_2
PC1265 *10u/6.3V_4
(23,38,44,47,48) MAINON
MAINON
MAINON_R_3VEN
PR1231 *Short_0402 SVT
PC1255 *0.1u/6.3V_2
S0_ON1_D
S0_ON1_D (48)
PC1218 *0.1u/6.3V_2
3V_SS
3V_DEEP_SUS_SS
PC1256 1000p/25V_2
PC1220 1000p/25V_2

+1.8V_S5
+3VPCU
1.5A
+1.8V_SUSR
PJP1713 *Short_0805
+1.8V_SUSRR
PC11219 *10u/6.3V_4
PC11217 0.1u/6.3V_2
PC11218 0.1u/6.3V_2
PC11220 0.1u/6.3V_2
+5V_ALW
PC11223 0.1u/6.3V_2
SUSON
PC11224 *0.1u/6.3V_2
PU1501 TPS22976DPUR
VIN1#1 VIN1#2 VIN2#1 VIN2#2
VOUT1#1 VOUT1#2 VOUT2#1 VOUT2#2
BIAS GND#1 GND#2 EN1 EN2 SS1 SS2
+3V_SUS_R
PJP1714 *Short_0805
2.5A
+3V_SUS
PC11221 0.1u/6.3V_2
PC11222 *10u/6.3V_4
SUSON
SUSON (23,38,39,45,48)
PC11225 *0.1u/6.3V_2
+1.8V_SUSR_SS
+3V_SUS_SS
PC11226 1000p/25V_2
PC11227 1000p/25V_2

2019/05/09 by James Kuo
Change +3VPCU from +3VS5

5A
+3V_SSD
PJP1210 *Short_0805
+3V_SSD_R
PC1271 *10u/6.3V_4
PC1267 0.1u/6.3V_2
+5V_ALW
PC1269 0.1u/6.3V_2
PC1268 0.1u/6.3V_2
+3VPCU
PC1276 0.1u/6.3V_2
PU1203 TPS22976DPUR
VIN1#1 VIN1#2 VIN2#1 VIN2#2
VOUT1#1 VOUT1#2 OUT2#1 OUT2#2
VBIAS GND#1 GND#2 ON1 ON2 CT1 CT2
+3V_S5_F
PJP1211 *Short_0805
2A
+3V_S5
PC1274 0.1u/6.3V_2
PC1275 *10u/6.3V_4
PR1245 *Short_0402 SVT
3VS5ON
S5_ON (18,23,38,40,44,48)
(23,38,44,47,48) MAINON
MAINON
PR1244 *Short_0402 SVT
SSDON
(23) SSD_ON
PR1219 *0_5%_4
PC1270 *0.1u/6.3V_2
PC1273 *0.1u/6.3V_2
SSDSS
3V5_SS
PC1272 1000p/25V_2
PC1266 1000p/25V_2

2019/05/09 by James Kuo
Add +3VPCU switch to +3VS5

+1.8V_S5
+1.8V_S5
0.5A
+1.8V_S5_ROM
PJP1207 *Short_0805
+1.8V_ROM
PC1230 *10u/6.3V_4
PC1231 0.1u/6.3V_2
PC1223 0.1u/6.3V_2
PC1225 0.1u/6.3V_2
+5V_ALW
PC1255 0.1u/6.3V_2
PU1202 TPS22976DPUR
VIN1#1 VIN1#2 VIN2#1 VIN2#2
VOUT1#1 VOUT1#2 VOUT2#1 VOUT2#2
BIAS GND#1 GND#2 EN1 EN2 SS1 SS2
+1.8V_R
PJP1206 *Short_0805
2.5A
+1.8V
PC1232 0.1u/6.3V_2
PC1233 *10u/6.3V_4
(23,38,40) SPI_1.8V_ON
+1.8V_ROMEN_1
PR1228 *Short_0402 SVT
PC1238 *0.1u/6.3V_2
1.8V_EN_2
PC1239 *0.1u/6.3V_2
PR1229 *Short_0402 SVT
+1.8V_S0_3 (46,48)
+1.8V_ROM_SS
+1.8V_SS
PC1242 1000p/25V_2
PC1243 1000p/25V_2

Custom
BU2
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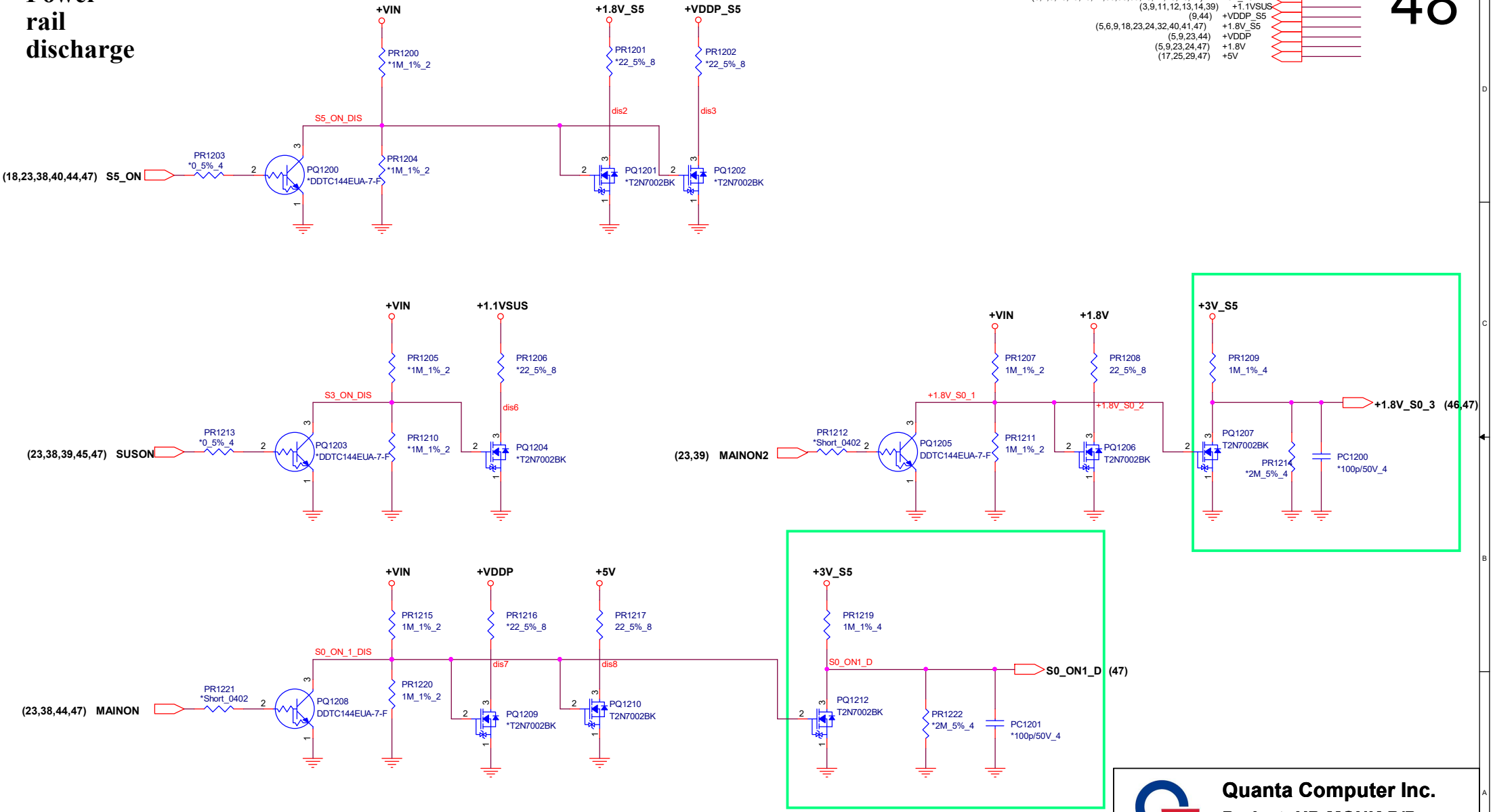
PROJECT : LS3
Quanta Computer Inc.

Size	Document Number	Rev
	Load switch IC (TPS22976)	1A

Date: Friday, January 17, 2020 Sheet 68

Power rail discharge

(16,28,37,38,39,40,41,42,43,49) +VIN
(6,7,9,18,19,23,24,30,38,39,40,44,45,46,47) +3V_S5
(3,9,11,12,13,14,39) +1.1VSUS
(9,44) +VDDP_S5
(5,6,9,18,23,24,32,40,41,47) +1.8V_S5
(5,9,23,44) +VDDP
(5,9,23,24,47) +1.8V
(17,25,29,47) +5V



Quanta Computer Inc.
Project: HP-MONK-P/D

Title		
Discharge		
Size	Document Number	Rev
	--	A1A
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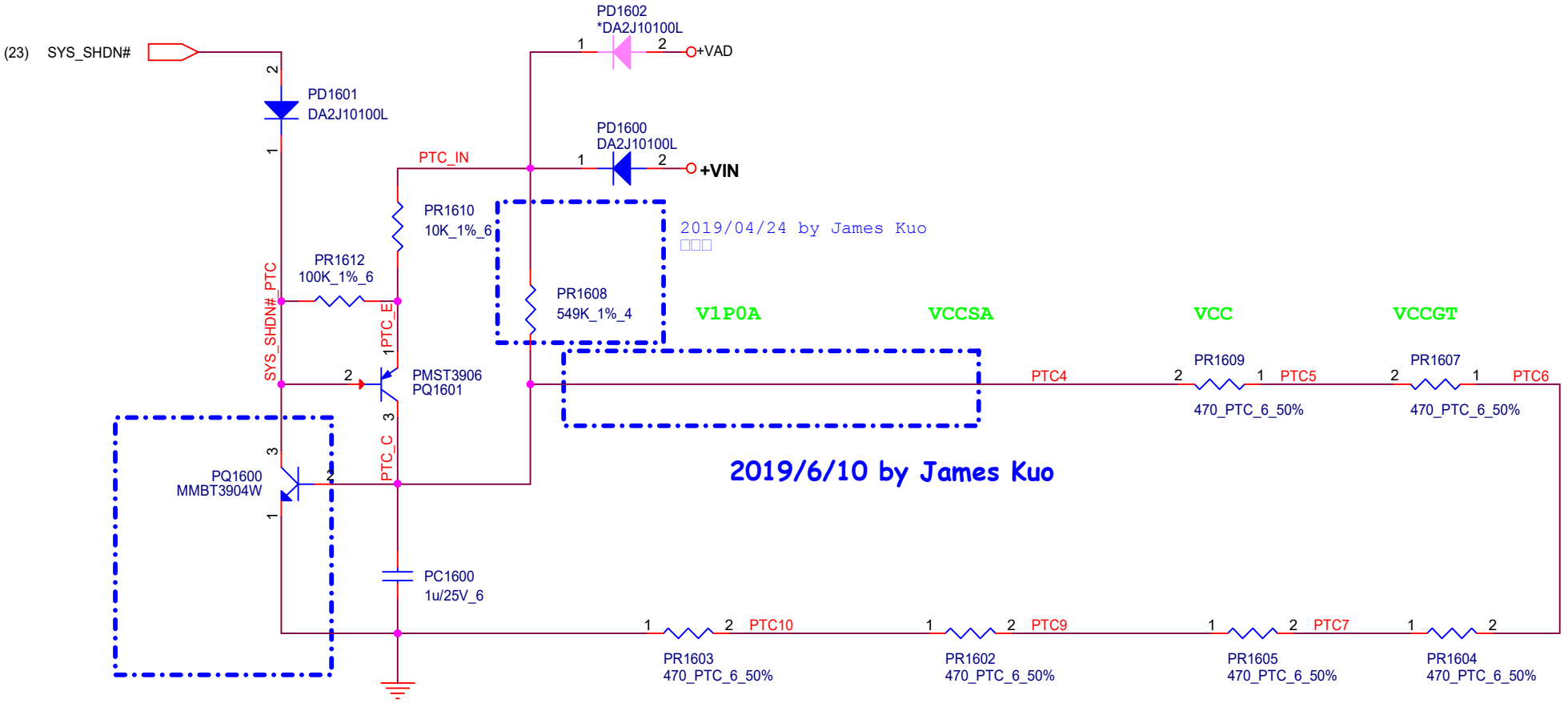

2019/04/23 by James Kuo
PQ1600 change to BA039040019 from BA0390400B1

Custom	PROJECT : LVC Quanta Computer Inc.	
Size: BU2	Document Number: PTC Circuit	Rev: 1A
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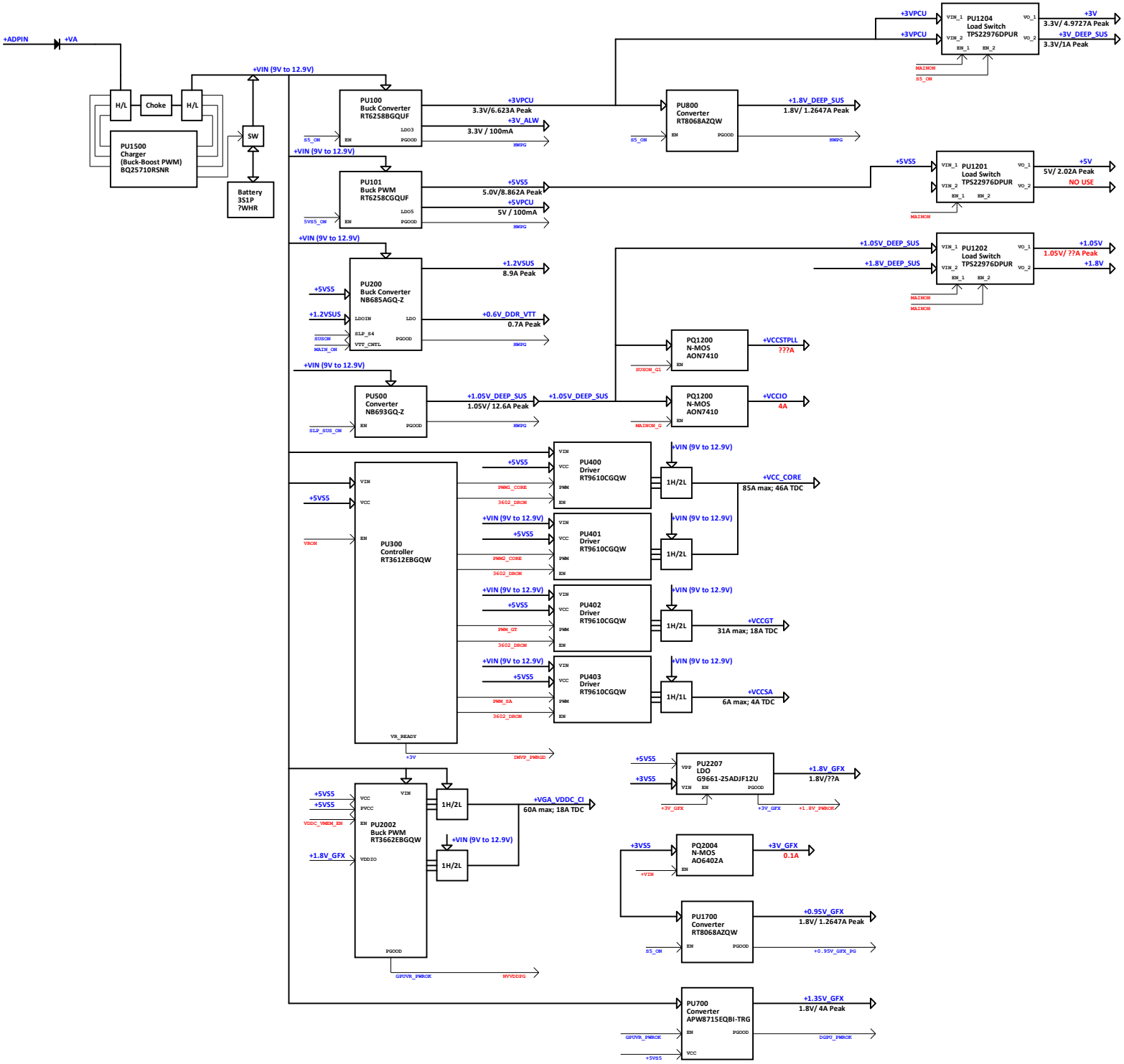
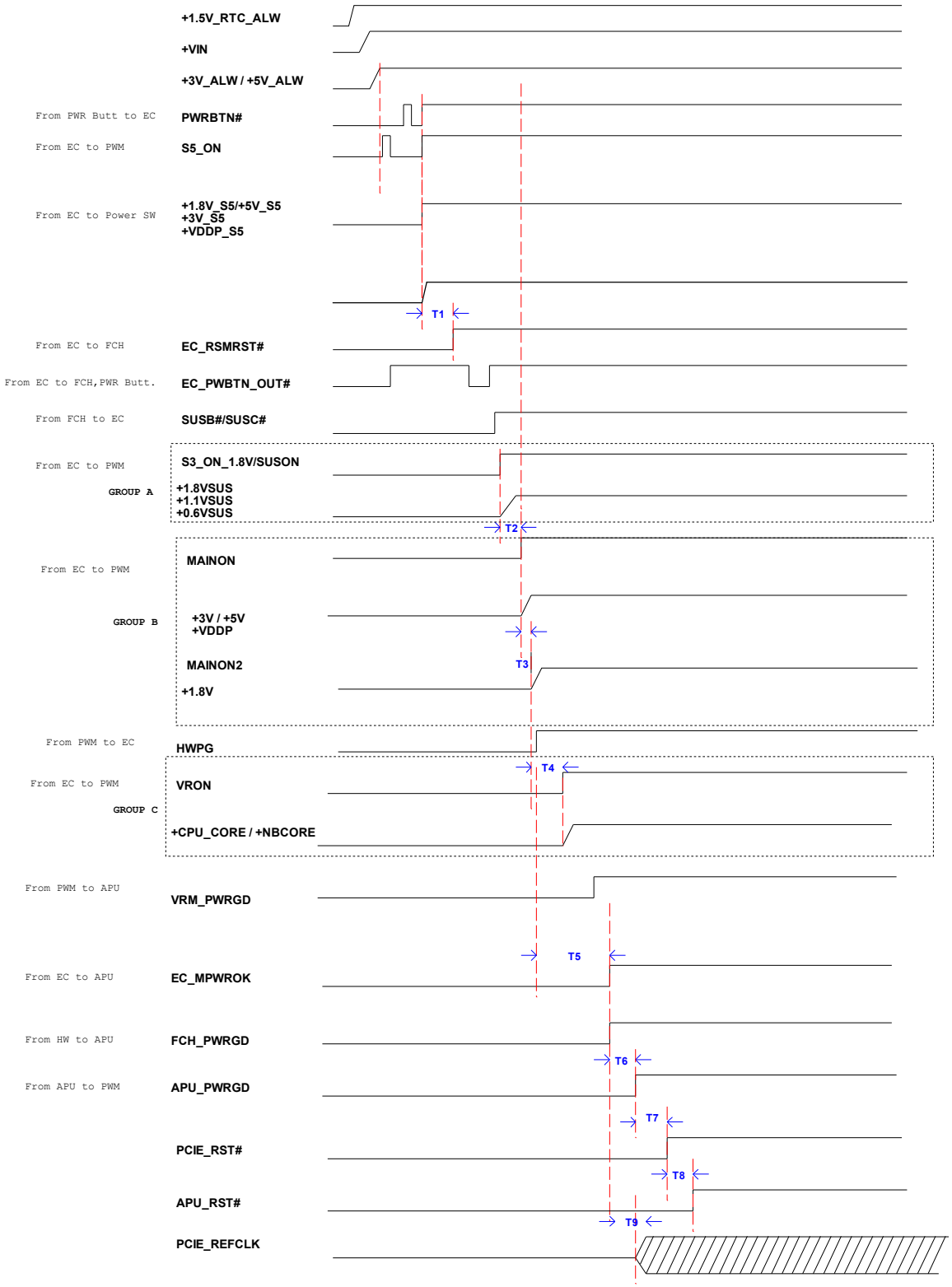
No.	Change details	Location/Description	Page	Remark
EC-EVT-E01	Change 5V_S5 power rails enable to S5_ON and 5VS5_ON	PR115	38	
EC-EVT-E02	Change APU RTC VCC to 3V_ALW,remove U17	U17,R77985	09	
EC-EVT-E03	Change APU SIV ID VDDIO to 1.8V_S5	PU300	13	
EC-EVT-E04	Change pin41 pin 43 pin define for support SATA	CN3,CN7724,R539,R7908	20,21	
EC-EVT-E05	Change LPDDR4 CAP part number to CH4222K9B04 0402 size		11,12,13,14	
EC-EVT-E06	Stuff Q6452 Q6453 for EC to sensor hub leakage	Q6452,Q6453		
EC-EVT-E07	Change dual mos polar for current leakage	Q6460,Q6467,Q6461,Q5000	24,27	
EC-EVT-E08	Add mos for prevent current leakage	Q28,Q6470	24,32	
EC-EVT-E09	Add IRCAM_FW for FW update	R77986	6,24	
EC-EVT-E10	Add U6449 for IRCAM power control	U6449	24	
EC-EVT-E11	Delete R260 for duplicate netname	R260	06	
EC-EVT-E12	Add TP_INT# for Lenovo reqoest of KB light off		23	
EC-EVT-E13	Add pull high MA,MB EVENT_L for follow AMD REF SCH	R77989,R77990	03	
EC-EVT-E14	Swap DDI1 signals for HDMI pin define		05	
EC-EVT-E15	Reserved re-driver CLK DAT path for debug use	R77991,R77992	17	
EC-EVT-E16	Change GPIO pin for AMD request and sata ssd		20,21	
EC-EVT-E17	Change battery LED power rails to 5V_S5	R77996	29	
EC-EVT-E18	change FN LED netname and add 200 ohm	R77997	25	
EC-EVT-E19	Add Diode to prevent leakage current	D6468	6,23	
EC-EVT-E20	change MBB_DQSH1,L1 order for layouthouse swap modify		14	
EC-EVT-E21	change USB3.0 USB 2.0 TYPEC order for AMD limitation		7	
			5	
EC-EVT-E23	Change CN2100 pin define for follow common design	CN2100	16	
EC-EVT-E24	add 5V_S5 one pin for increase current		25	
EC-EVT-E25	change CN7720,CN7711 footprint	CN7720,CN7711	25,30	
EC-EVT-E26	change I2C0,I2C1 power domain from 1.8V to 3.3V and remove level shifter		6,27	
EC-EVT-E27	change battery led control use mos instead of BJT reduce s5 power comsuption		29	
EC-EVT-E28	change KB light control	Q5003,Q5003	25	
EC-EVT-E29	change HDMI EMI resister	R3501,R3502,R73503,R3504	17	
EC-EVT-E30	change sensor smbus addresss add pull up resister for SMBUS	R78006,R78007,R78008,R78009	29	
EC-EVT-E31	change Audio DVDD-IO to 1.8V		18	
EC-EVT-E32	change S5_ON and SPI_1.8V_ON on EC pin order to avoid EC load code fail		23	
EC-EVT-E33	change CN7725 footprint		24	
EC-EVT-E34	Reserve UART interface for support WLAN 802.11ax card		6,19	
EC-EVT-E35	Add CPU CAP for stable CPU power		9	
EC-EVT-E36	unstuff R5803 for TPS65988 HPD is pushpull type		31	
EC-FVT-E01	Change sensor hub to SUS power rails to support wake on TOF	R78042,R8108,Q6461	24	
EC-FVT-E02	Reserve Aufio PDM level shifter for WoV feature		24	
EC-FVT-E03	Change Speaker bead to 0 ohm		18	
EC-FVT-E04	Change FP conn pin define	CN5201	27	
EC-FVT-E05				
EC-FVT-E06	Change FP power rails to 3VPCU to support SSO		27	
EC-FVT-E07	Add EC pin to control dead battery function		32	
EC-FVT-E08				
EC-FVT-E09	Remove GPIO67,76 for HW strip pin		6	
EC-FVT-E10	change sensor hub I2C interface location from EC		23	
EC-FVT-E11	Reserve S5 and S3 power rails for support Wov feature		18	
EC-FVT-E12	Add APU_THERMTRIP# to prevent restart issue		23	
EC-FVT-E13	Change thermal sensor NCT7719W for AMD STT2.0		29	
EC-FVT-E14	Change TOF sensor power rails same as sensor hub		24	
EC-FVT-E15	Change Y1 Y2 CAP value for EA test		6	
EC-FVT-E16	Add pull down GPD2 for ITE5570 HW issue		23	
EC-FVT-E17				
EC-FVT-E18	Change DMIC power rails same as APU AUDIO_VDDIO power rails		24	
EC-FVT-E19	Change camera power rails to S5 power for MS3 issue		24	
EC-FVT-E20	Add AND gate to meet PCIe specification		21	
EC-FVT-E21	Change head phone damp resister for EA test		18	
EC-FVT-E22	Add DMIC led control for Audio codec and APU		6,18,25	
EC-FVT-E23	Add FP LED for EC control		23,30	
EC-FVT-E24	Add SUS power for touch pad		27	
EC-FVT-E25	Add LPC header for MS3 debug		19	
EC-FVT-E26				
EC-FVT-E27				
EC-SIT-EE01	Change ALS interrupter pin define		19	
EC-SIT-EE02	Add 1.2V_VPH for EDP panel power saving		6	
EC-SIT-EE03	Keeping WLAN wake pin to oringnal location		6,7,19	
EC-SIT-EE04	Change WLAN,PD interrupt,s0i3 setting		6,19	
EC-SIT-EE06	Change FP power control for LVA suggest		27	
EC-SIT-EE08	Change PD I2C location for support PDFW update		6,32	
EC-SIT-EE09	ADD PD reset pin to EC		23	
EC-SIT-EE10	ADD PD HPD levle shifter for PD leakage issue		32	
EC-SIT-EE11	ADD cap for RSMRST#_R noise		6	
EC-SIT-EE12	Change HDMI SCL,SDA and damping resister		17	
EC-SIT-EE13	ADD mos for APU_RST# to EC notify		23	

POWER BLOCK DIAGRAM



PROJECT : LVC
Quanta Computer Inc.
BU2

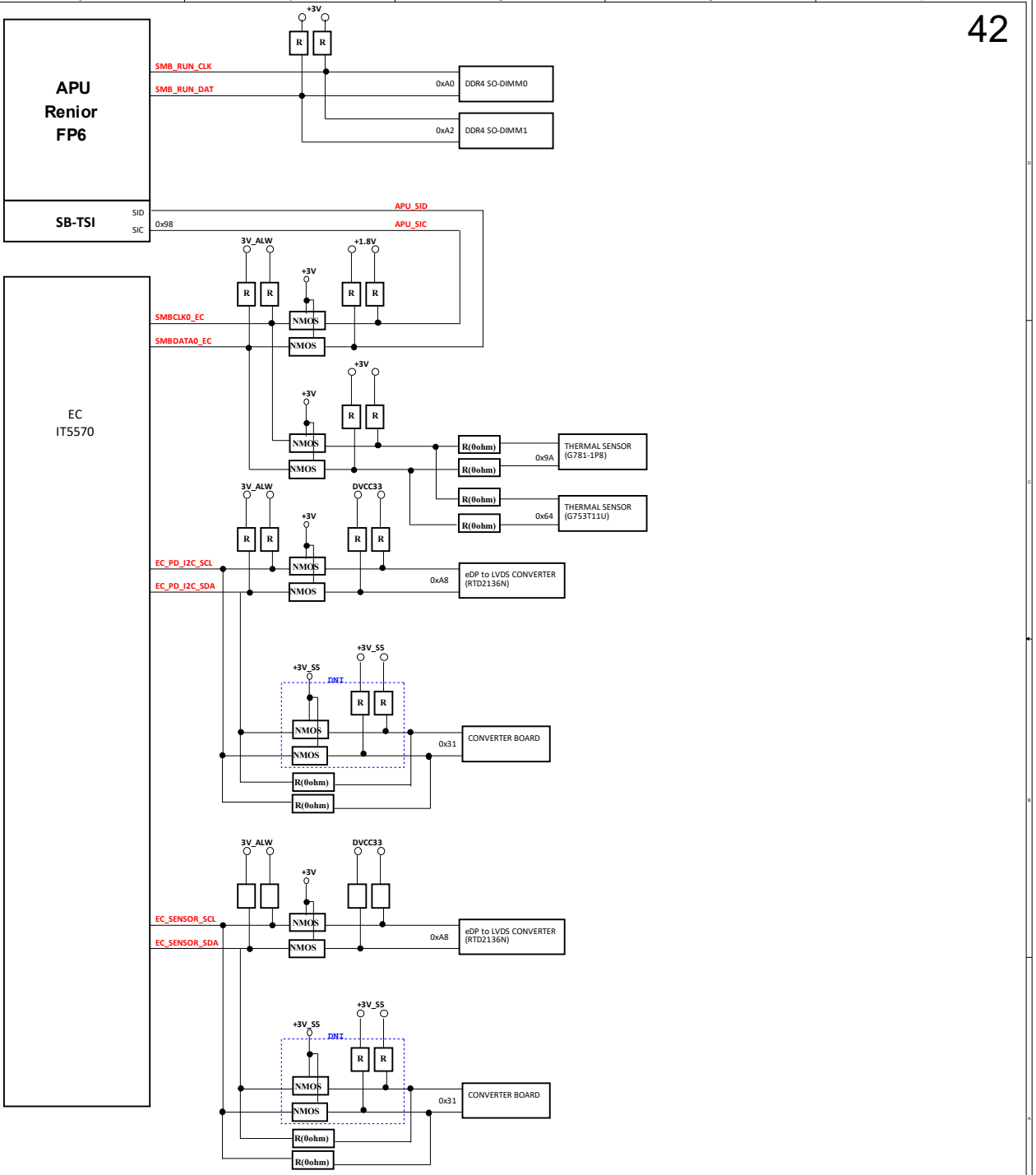


System Power Sequence

EC Control:
T1: S5_ON TO EC_RSMRST# = 20ms
T2: S3_ON TO MAIN_ON1=10ms
T3: MAIN_ON1 TO MAIN_ON2 = 1ms
T4: MAIN_ON2 TO VRON = 10ms
T5: HWPG TO MPWROK =99ms

Timing spec:
T1 Spec:10ms min
Power Up Spec:
Group A > Group B > Group C
T6: FCH_PWRGD TO APU_PWRGD = 108.6~118.6 ms
T7: APU_PWRGD TO PCIE_RST# = 114.2~124.2 ms
T8: PCIE_RST# TO APU_RST# = 111.9~121.9 ms
T9: FCH_PWRGD TO PCIE_REFCLK = 37.6~47.6 ms

PROJECT : LS3
Quanta Computer Inc.
BU2
Power Sequence
A1A
Friday, January 17, 2020



PROJECT : LS3
Quanta Computer Inc.
BU2
SMBUS
A1A
Friday, January 17, 2020
53
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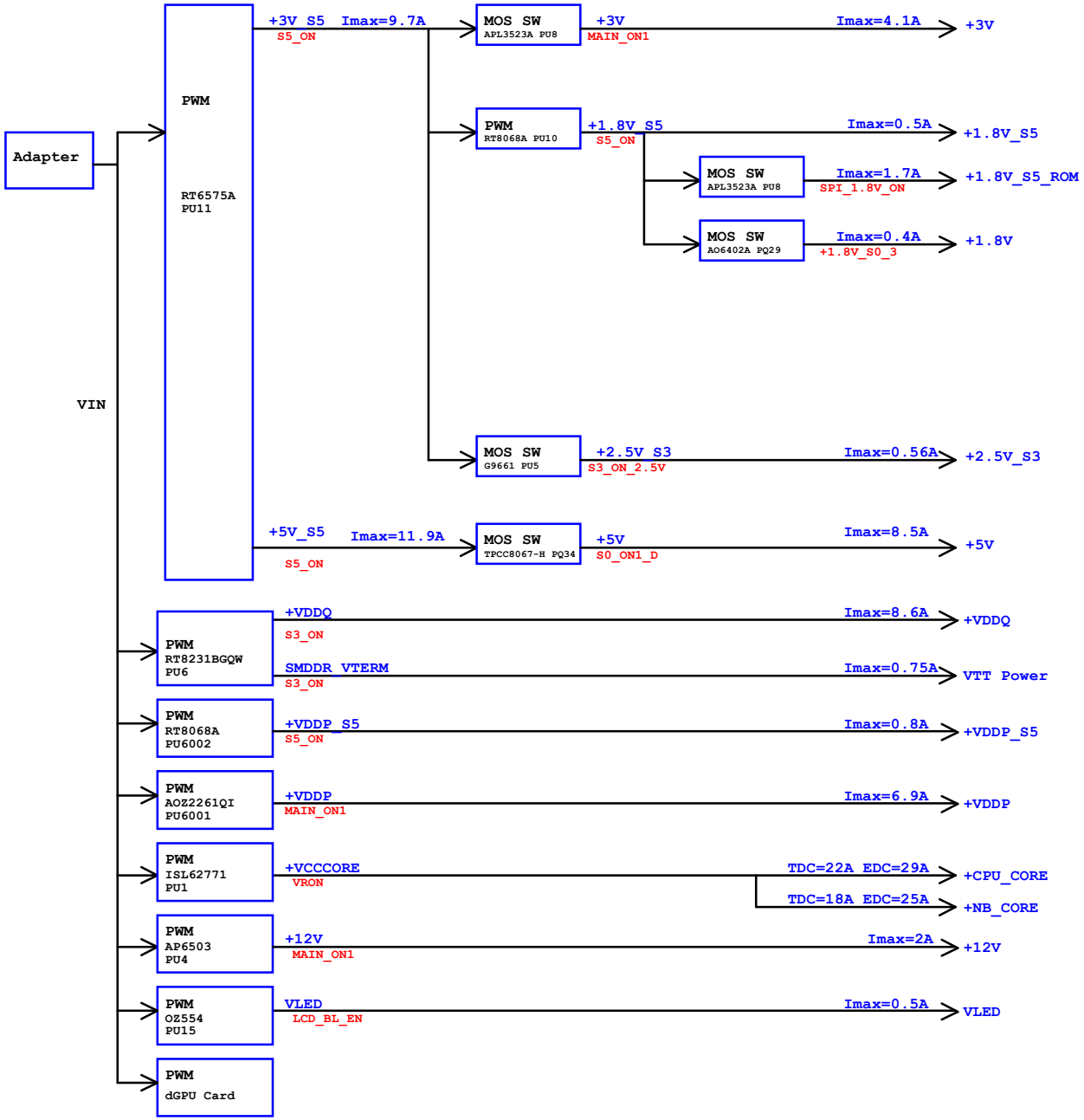
Power Delivery Map



HP Restricted Secret

BU2	PROJECT : LS3 Quanta Computer Inc. Size: -- | Document Number: Power Delivery Map | Rev: A1A Date: Friday, January 17, 2020 | Sheet 54 of 54