Vortex (I+N)
MVBuild

NB5

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Size	Document Number	Rev
Custom	VORTEX (I+N)	2A

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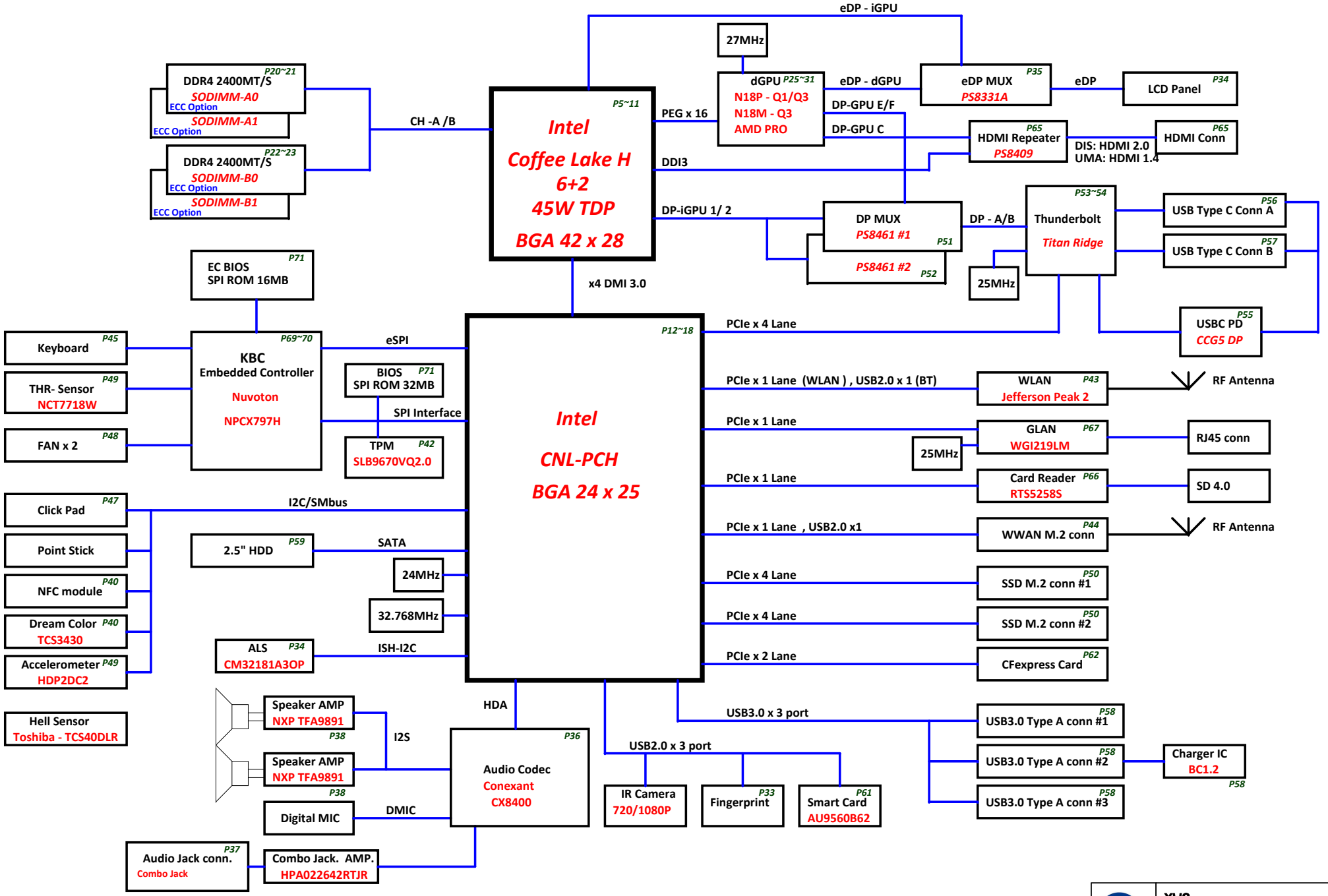

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Size	Document Number	Rev
Custom	Block Diagram	2A

NB5

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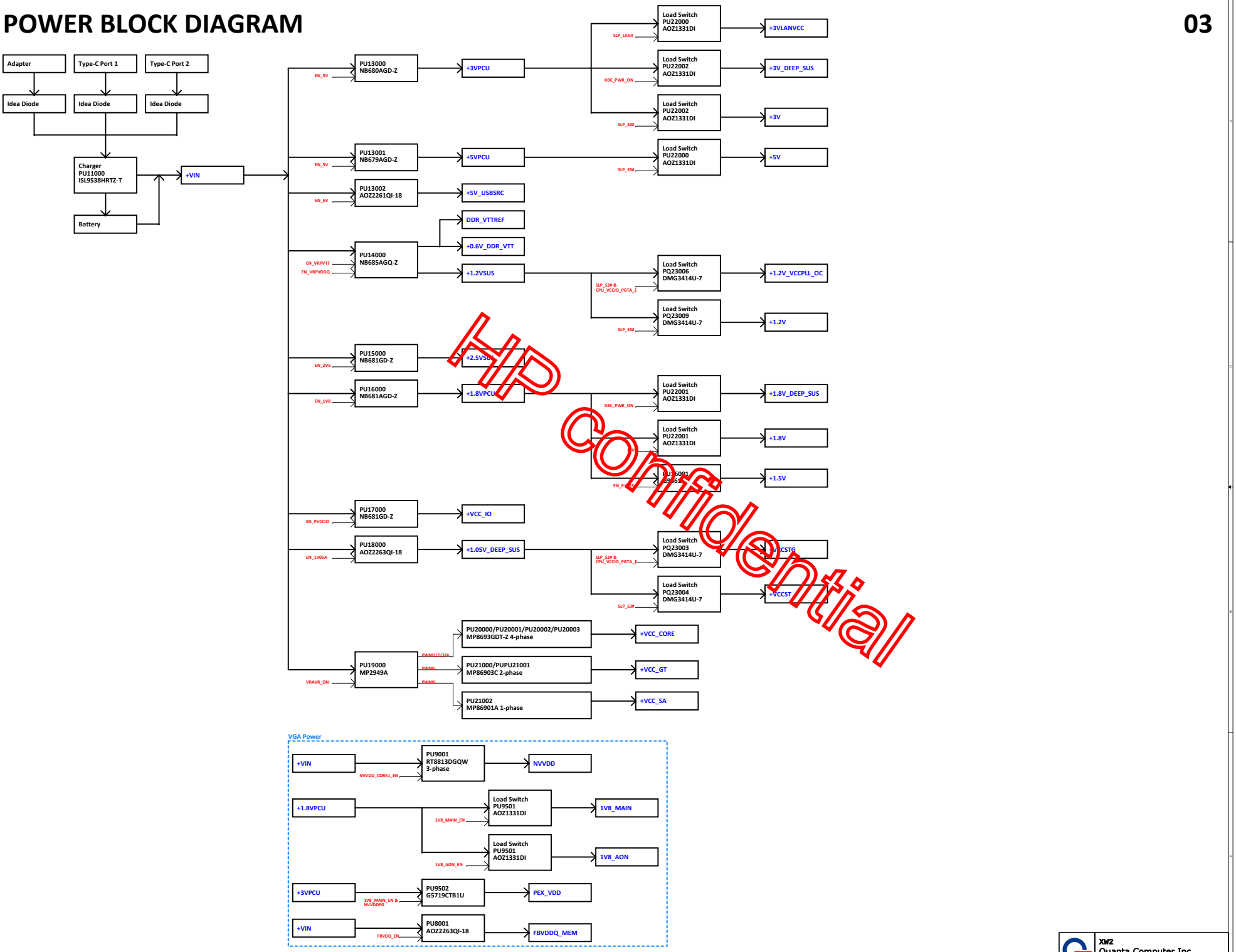
POWER BLOCK DIAGRAM



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Size: Custom
Document Number: 06 – Power Block Diagram
Rev: 2A
Date: Wednesday, May 30, 2018
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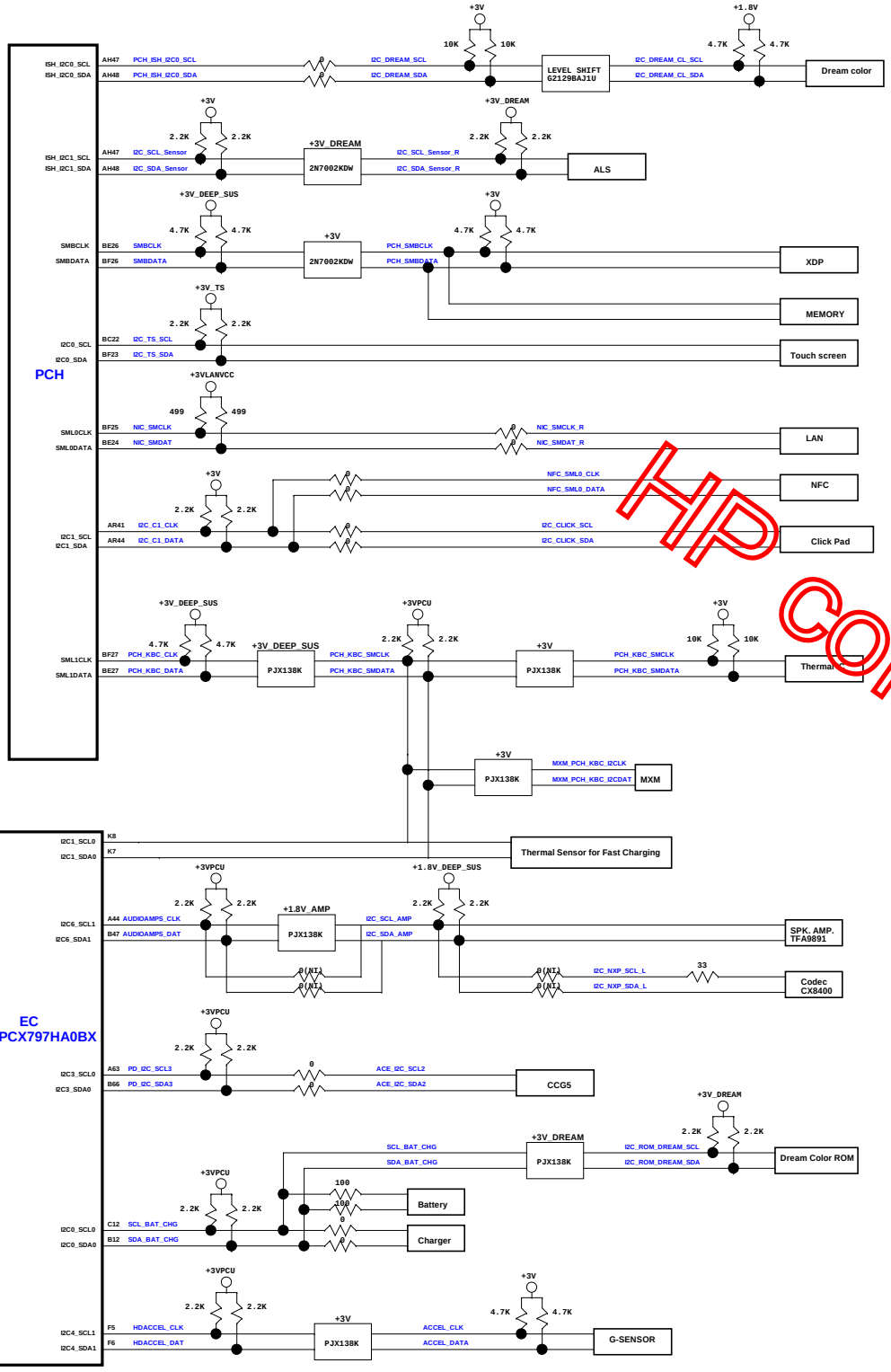

Multiplexed HSIO Lane	Port Assignment
USB3 #1	USB2.0/USB3.0 Combo Jack(Right side)
USB3 #2 / SSIC #1	NC
USB3 #3 / SSIC #2	USB2.0/USB3.0 Combo Jack(Light side-1)
USB3 #4	USB2.0/USB3.0 Combo Jack(Light side-2)
USB3 #5	NC
USB3 #6	NC
PCIE1 / USB3 #7	XQD
PCIE2 / USB3 #8	XQD
PCIE3 / USB3 #9	CARD READER
PCIE4 / USB3 #10	WWAN
PCIE5	Alpine Ridge
PCIE6	Alpine Ridge
PCIE7	Alpine Ridge
PCIE8	Alpine Ridge
PCIE9	SSD 1
PCIE10	SSD 1
PCIE11(SATA0A)	SSD 1(SATA0A)
PCIE12(SATA1)A	SSD 1(SATA1A)
PCIE13(SATA0B)	LAN
PCIE14(SATA1B)	WLAN
PCIE15(SATA2)	ODD
PCIE16(SATA3)	HDD
PCIE17(SATA4)	SSD 2(SATA4)
PCIE18(SATA5)	SSD 2(SATA5)
PCIE19(SATA6)	SSD 2(SATA6)
PCIE20(SATA7)	SSD 2(SATA7)
PCIE21	SSD 3
PCIE22	SSD 3
PCIE23	SSD 3
PCIE24	SSD 3

USB2.0	Port Assignment
USB2 #1	USB2.0/USB3.0 Combo Jack(Right side)
USB2 #2	WWAN
USB2 #3	NC
USB2 #4	USB2.0/USB3.0 Combo Jack(Left side-1)
USB2 #5	USB2.0/USB3.0 Combo Jack(Left side-2)
USB2 #6	NC
USB2 #7	Camera
USB2 #8	Finger Print
USB2 #9	Smart Card
USB2 #10	NC
USB2 #11	TI PD PORT A
USB2 #12	NC
USB2 #13	TI PD PORT B
USB2 #14	BT

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SMBUS & PORT ASSIGNMENT

CFL-H Processor (CLK,MISC,JTAG)

05

For debug only remove from MV

+3V R9301 *360_1%_6 LED9000 *White_19-113/T1D-CP2Q2HY/3T
+VCCST R9000 *49.9/F_4 R9002 *4.7K/F_4
CATERR# Q9001A *PJT138K Q9001B *PJT138K

U9001E

Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impendence 85 ohm

CLK_CPU_BCLKP B31 BCLKP
CLK_CPU_BCLKN A32 BCLKN
CPU_PCI_BCLKP D35 PCI_BCLKP
CPU_PCI_BCLKN C36 PCI_BCLKN
CLK_DPLL_NSCCLKP E31 CLK24P
CLK_DPLL_NSCCLKN D31 CLK24N

H_CPU_SVIDALRT# BH31 VIDALERT#
VR_SVID_CLK_R BH32 VIDSCK
H_CPU_SVIDDAT BH29 VIDSOUT
CPU_PROCHOT#_R BR30 PROCHOT#
DDR_PG_CNTL BT13 DDR_VTT_CNTL

CFG_0 BN25 CFG0 … CFG_18 BN22 CFG18
BPM#_0 BR27 XDP_BPM0 … BPM#_3 BT30 XDP_BPM3 TP9034 TP9035
PROC_TDO BT28 H_TDO
PROC_TDI BL32 H_TDI
PROC_TMS BP28 H_TMS
PROC_TCK BR28 H_TCK
PROC_TRST# BP30 H_TRST#
PROC_PREQ# BL30 H_PREQ#
PROC_PRDY# BP27 H_PRDY#
CFG_RCOMP BT25 CFG_RCOMP 49.9/F_4 R9310

VCCST_PWRGD H13
PROCPWRGD BT31
RESET# BP35
PM_SYNC BM34
PM_DOWN BP31
PECI BT34
THERMTRIP# J31
SKTOCC# BR33
PROC_SELECT# BN1
CATERR# BM30
ZVM# AT13 AW13
MSM# AU13 AY13
RSVD#AU13
RSVD#AY13
5 OF 13

*CPU_CFL-H_1440P

+3V_DEEP_SUS R9308 4.7K_1%_4 Q9002A PJX138K
+VCCST R9309 1K_1%_4 Q9002B PJX138K
PWR_GOOD_3 24,41,70,89,90
H_VCCST_PWRGD R9340 60.4_1%_4 VCCST_PWRGD
TP9002 PROCPWRGD CPU_PLTRST#R R9012 20_1%_4 H_PM_DOWN_R
TP9003 SKTOCC_N PROC_SEL#
TP9004 CATERR#
PECI 13_1%_4 R9017 PCH_PECI 14 PECI 70

PROCPWRGD (50ohm)
Trace Length: 1~11.25 inches
PM_SYNC (50ohm)
Trace Length: 1~11.25 inches
CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

Design Note(CFG_RCOMP):
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

Processor pull-up (CPU)

H_TDO R9302 100_1%_4 +VCCST
H_TMS R9303 51_5%_4
H_TDI R9304 51_5%_4
H_PREQ# R9305 *56.2_1%_4
H_TCK R9306 51_5%_4
H_TRST# R9307 *51_5%_4

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

CFG2 R9011 1K_1%_4
CFG4 R9013 1K_1%_4
CFG5 R9014 *1K_1%_4
CFG6 R9015 *1K_1%_4

Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.
Intel recommends placing test points on the board for CFG pins.
. CFG[0]:Stall reset sequence after PCU PLL lock until de-asserted:
-1=(Default) Normal Operation; No stall.
-0=Stall.
.CFG[1]:Reserved configuration lane.
.CFG[2]:PCI Express*Static x16 Lane Numbering Reversal.
-1=Normal operation
-0=Lane numbers reversed.
.CFG[3]:Reserved configuration lane.
.CFG[4]:eDP enable:
-1=Disabled.
-0=Enabled.
.CFG[6:5]:PCI Express* Bifurcation
-00=1x8,2x4 PCI Express*
-01=reserved
-10=2x8 PCI Express*
-11=1x16 PCI Express*
.CFG[7]:PEG Training:
-1=(default) PEG Train immediately following RESET# de assertion.
-0=PEG Wait for BIOS for assertion.
.CFG[19:8]:Reserved configuration lanes.

CPU CORE SVID

Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.

PLACE THE PU RESISTORS CLOSE TO VR PULL UP IS IN THE VR MODULE
+VCCST R9311 *54.9_1%_4 Close to CPU
SVID CLK
VR_SVID_CLK_R R9314 *0/S VR_SVID_CLK 84

CLOSE TO CPU PLACE THE PU RESISTORS
+VCCST R9318 56.2_1%_4 Close to CPU
SVID ALERT
H_CPU_SVIDALRT# R9030 220_1%_4 VR_SVID_ALERT# 84
C9002 *0.1u/16V_4

CLOSE TO CPU PLACE THE PU RESISTORS
+VCCST R9034 100_1%_4 Close to CPU
SVID DATA
H_CPU_SVIDDAT R9036 *0_5%_4 VR_SVID_DATA 84

THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches
+VCCST R9018 200_1%_4 R9019 1K_1%_4 Q9000 METR3904-G
14,20,21,22,23,27 PM_THRMTRIP# THRMTRIP#

Ra(R18) Not install in SKL-H
+VCCST Ra R9317 *10K_1%_4 PROC_SEL# R9319 *0_5%_4

Note: please keep plane is enough for VDDQ 2.8A
Placement close to CPU.
+1.2VSUS C9000 0.1u/16V_4 C9001 *0.1u/16V_4
+3V_DEEP_SUS R9313 10K_1%_4 R9028 100K_1%_4
+3V_DEEP_SUS R9312 10K_1%_4 Q9003 2N7002KTB R9315 *100K_1%_4 DDR_VTT_PG_CTRL 24,79
DDR_PG_CNTL R9316 10K_1%_4 METR3904-G

PROCHOT# (50ohm)
Trace Length <11 inches
Cb need placment near VR
+VCCSTG R9320 1K_1%_4
48,77,84 CPU_PROCHOT# R9321 499_1%_4 CPU_PROCHOT#_R
48,49 THERM_SC# R9033 *0_5%_4
Cb C9003 47p/50V_4

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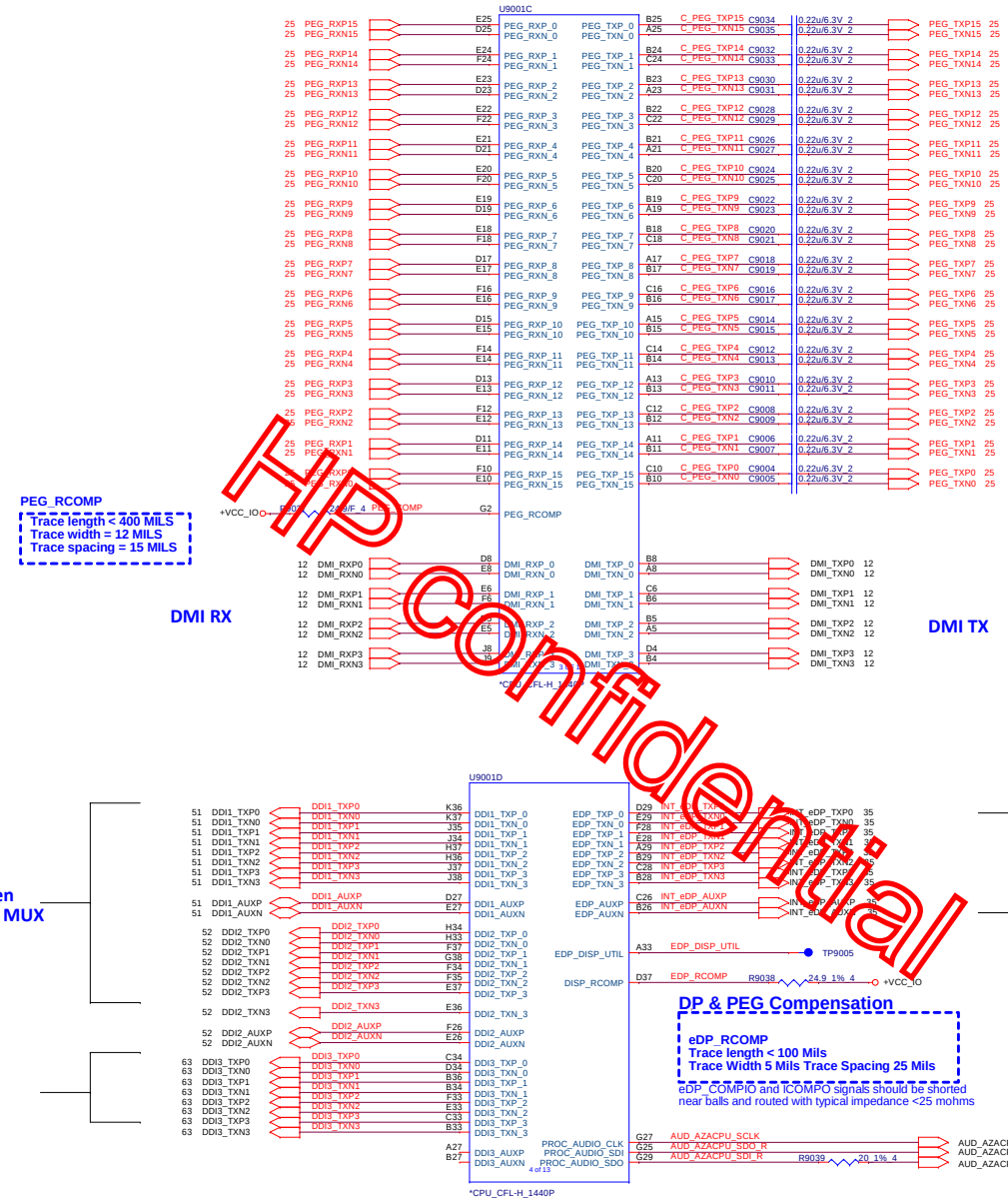
KBL Processor (DMI,PEG,FDI)



5,9,13,20,21,22,23,79,88 +1.2VSUS

5,12,13,14,16,20,21,22,23,27,28,33,34,35,36,40,41,42,43,44,45,47,48,49,50,51,54,59,63,65,66,68,69,73,77,84,87,90,93,94 +3V

NB5	XW2 Quanta Computer Inc.	
Size: Custom	Document Number: KBL 2/7 (DMI/EDP/PEG)	Rev: 2A
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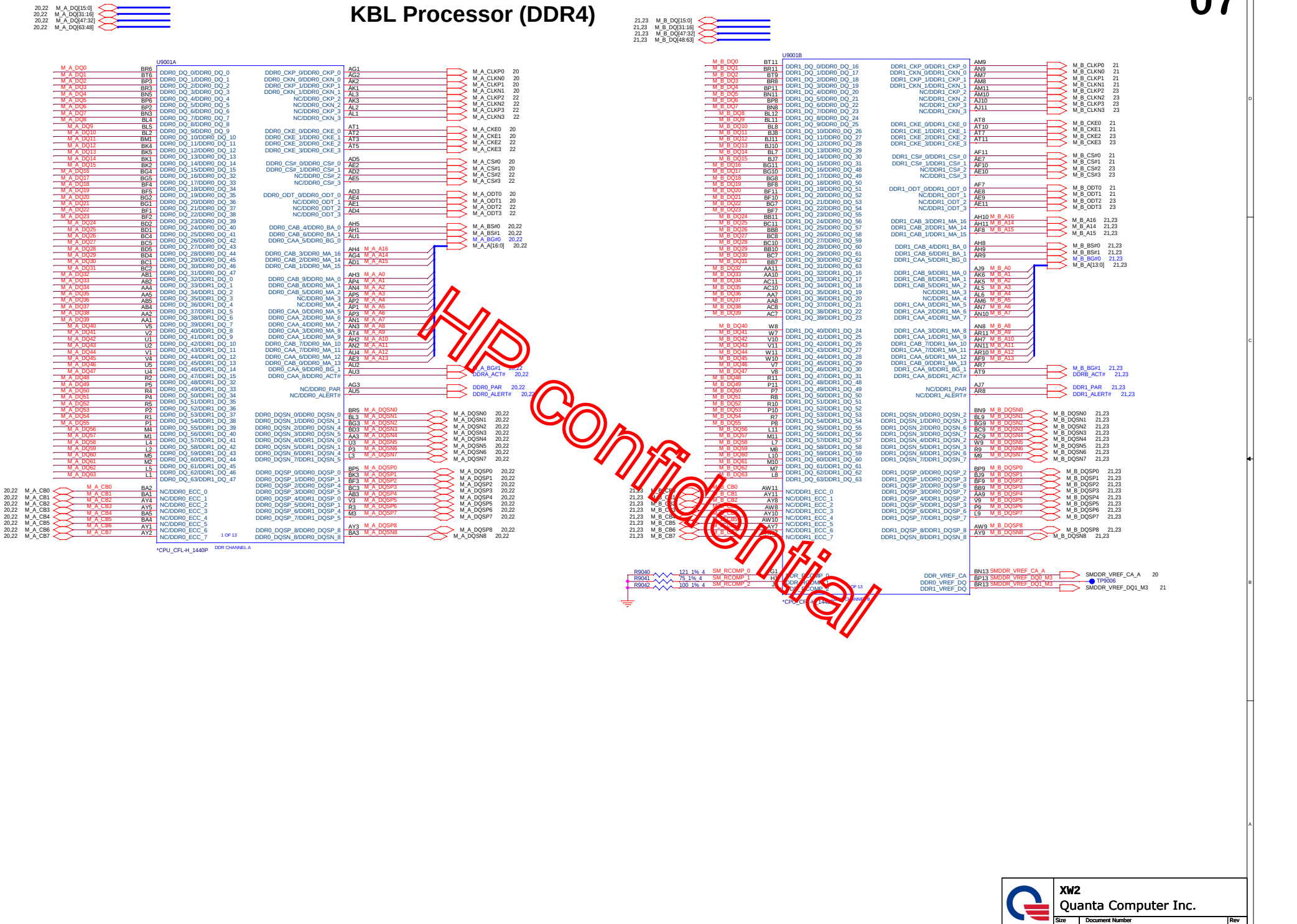
KBL Processor (DDR4)



XW2	Quanta Computer Inc.
NB5	Size C · Document Number KBL 3/7 (DDR4 I/F) · Rev 2A
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VCCGT

Edge cap
4x 47uF 0805
7x 22uF 0603

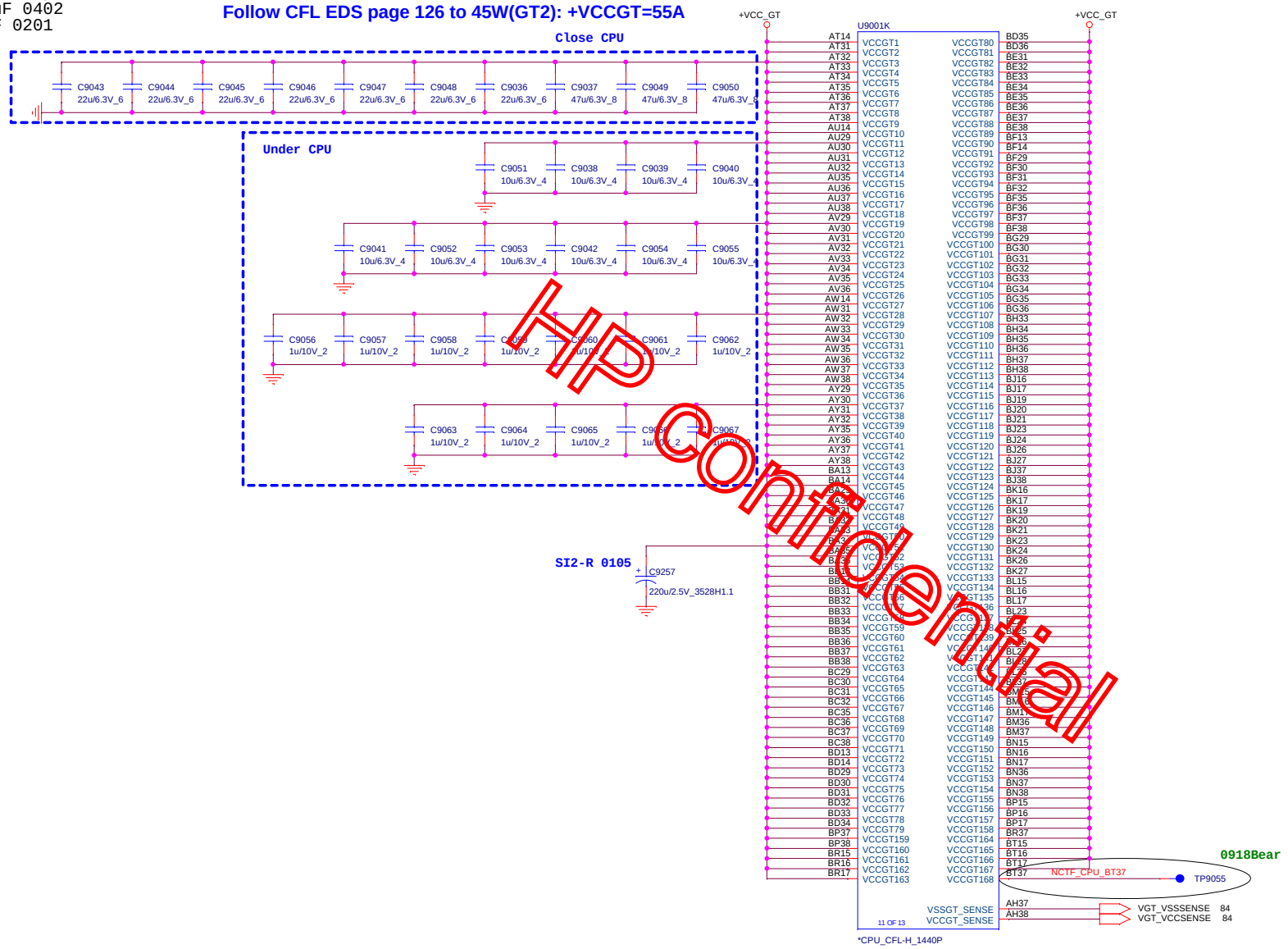
Backside cap
10x 10uF 0402
12x 1uF 0201

KBL Processor (POWER)

08

+VCC_GT 84,86

Follow CFL EDS page 126 to 45W(GT2): +VCCGT=55A



NB5	XW2 Quanta Computer Inc.	
Size: Custom	Document Number: KBL 4/7 (POWER)	Rev: 2A
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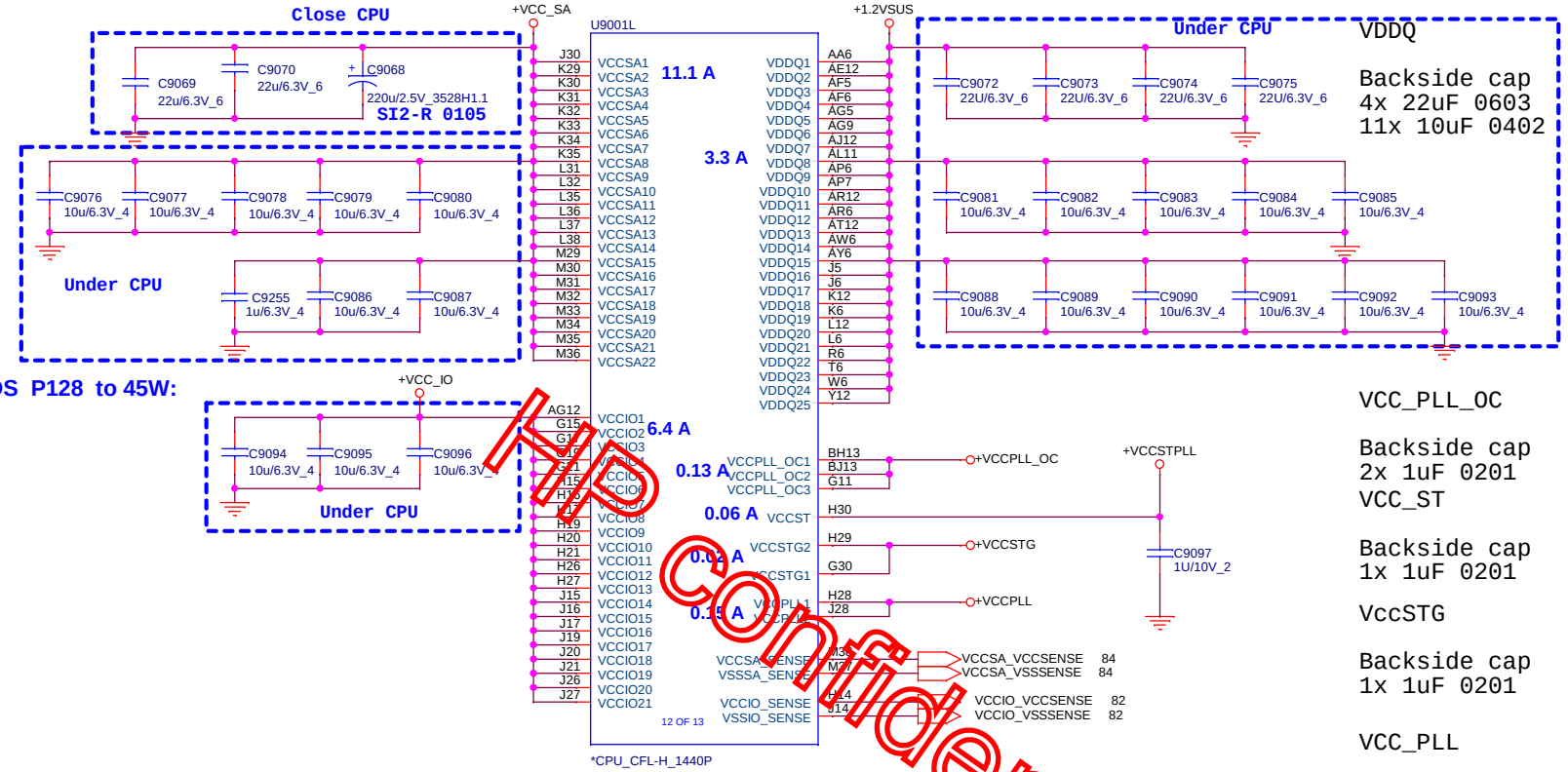
Follow CFL H EDS page 128 to 45W(GT2): VCCSA=11.1A

Follow CFL H EDS page 127 45W: VDDQ=3.3A (LPDDR4)

+VCC_SA

Edge cap
2x 47uF 0805
2x 22uF 0805

Backside cap
7x 10uF 0402



Follow CFL H EDS P128 to 45W:
VCCIO,
+VCCIO = 6.4A

+VCC_IO

Backside cap
3x 10uF 0402

VCC_PLL_OC

Backside cap
2x 1uF 0201
VCC_ST

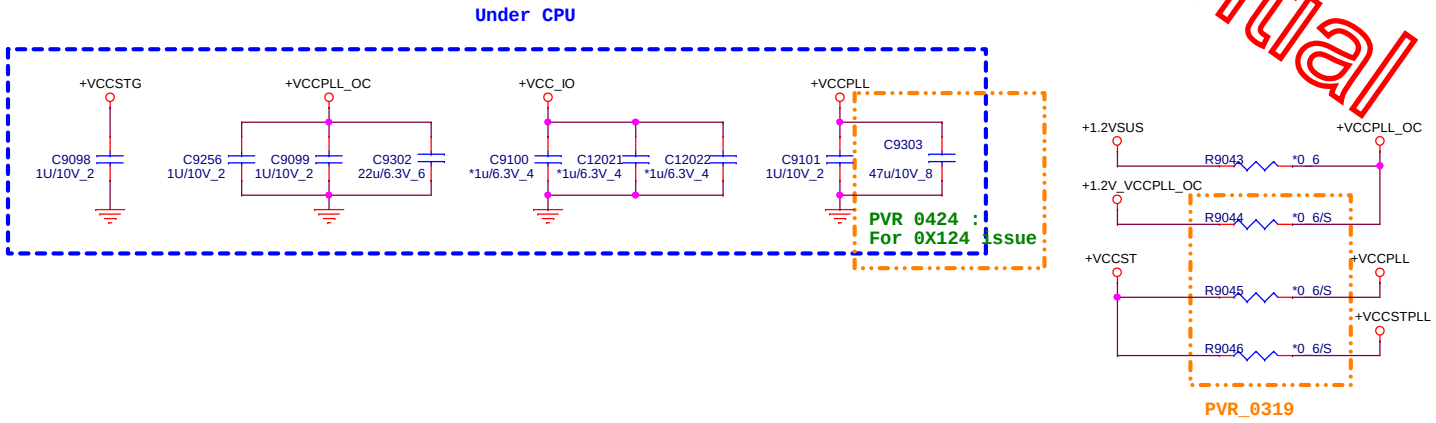
Backside cap
1x 1uF 0201

VccSTG

Backside cap
1x 1uF 0201

VCC_PLL

Backside cap
4x 22uF 0603
11x 10uF 0404



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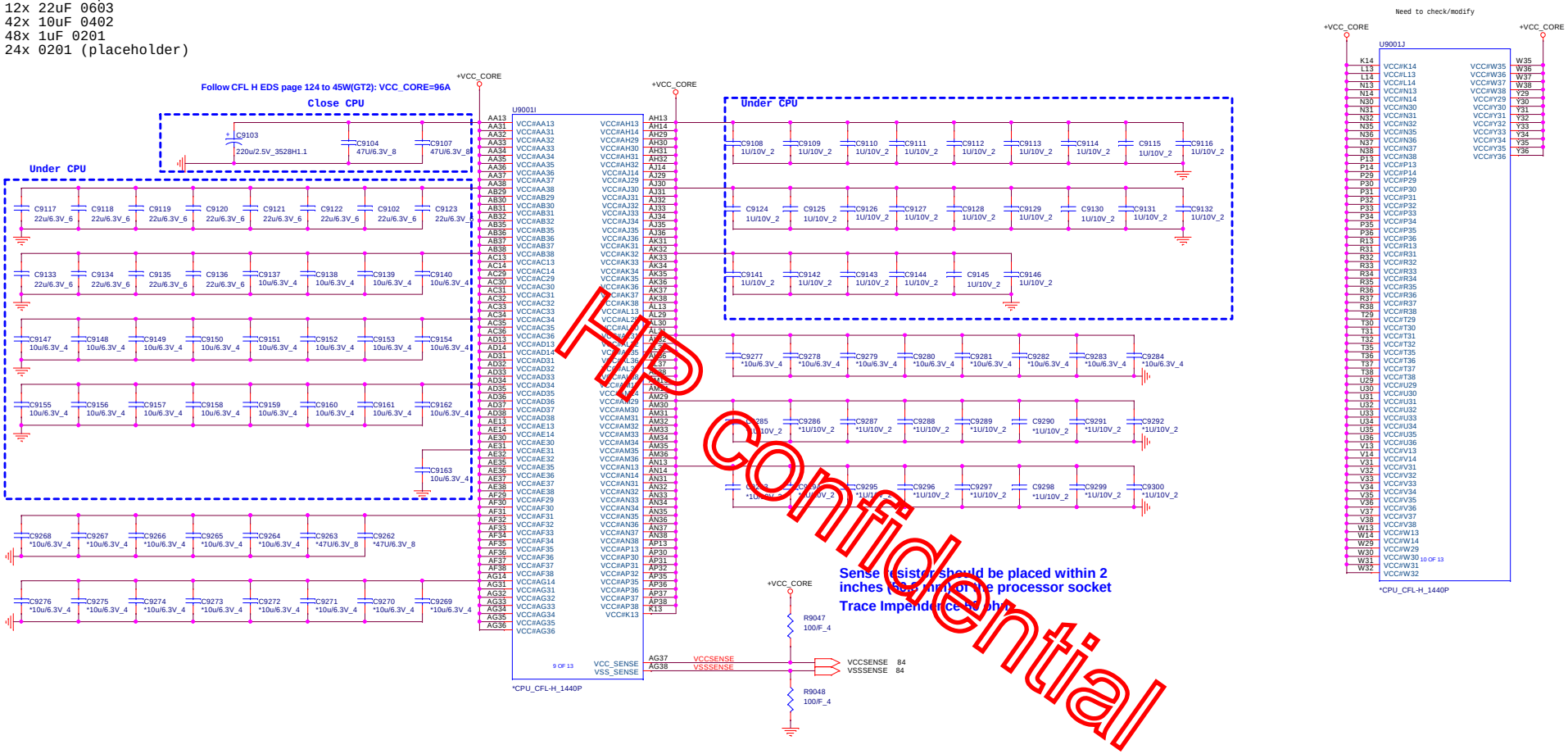
Vcc (VCC_CORE)

Edge cap
8 x 47uF 0805

Backside cap
12x 22uF 0603
42x 10uF 0402
48x 1uF 0201
24x 0201 (placeholder)



NB5	XW2 Quanta Computer Inc.	
Size: Custom	Document Number: KBL 6/7 (POWER&GND)	Rev: 2A
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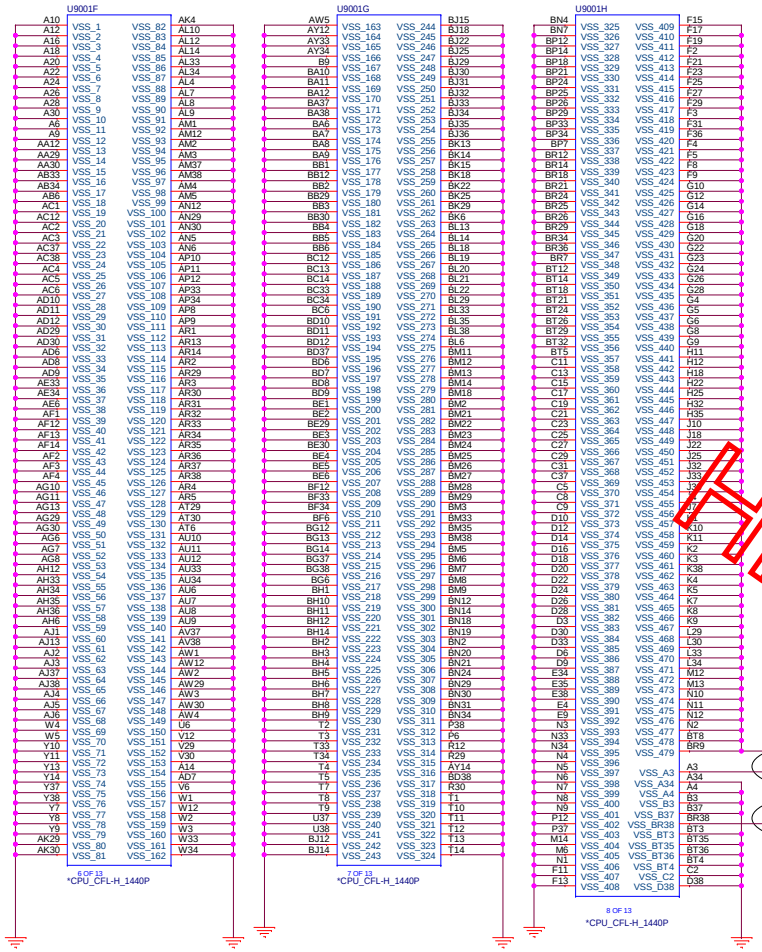
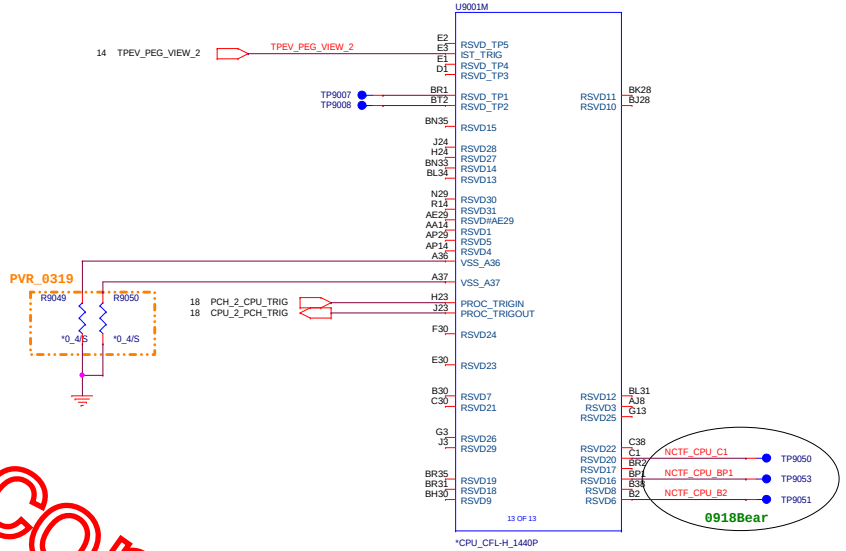
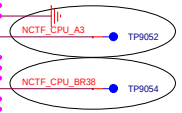
KBL-HProcessor (GND)



KBL-H Processor (RESERVED, CFG)





Configuration Signals:			
		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the older reference designs board might connect CFG[0] to HOOK[2]. This mode is not needed for a OxM board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asseted x0 = PEG wait for BIOS fro training	

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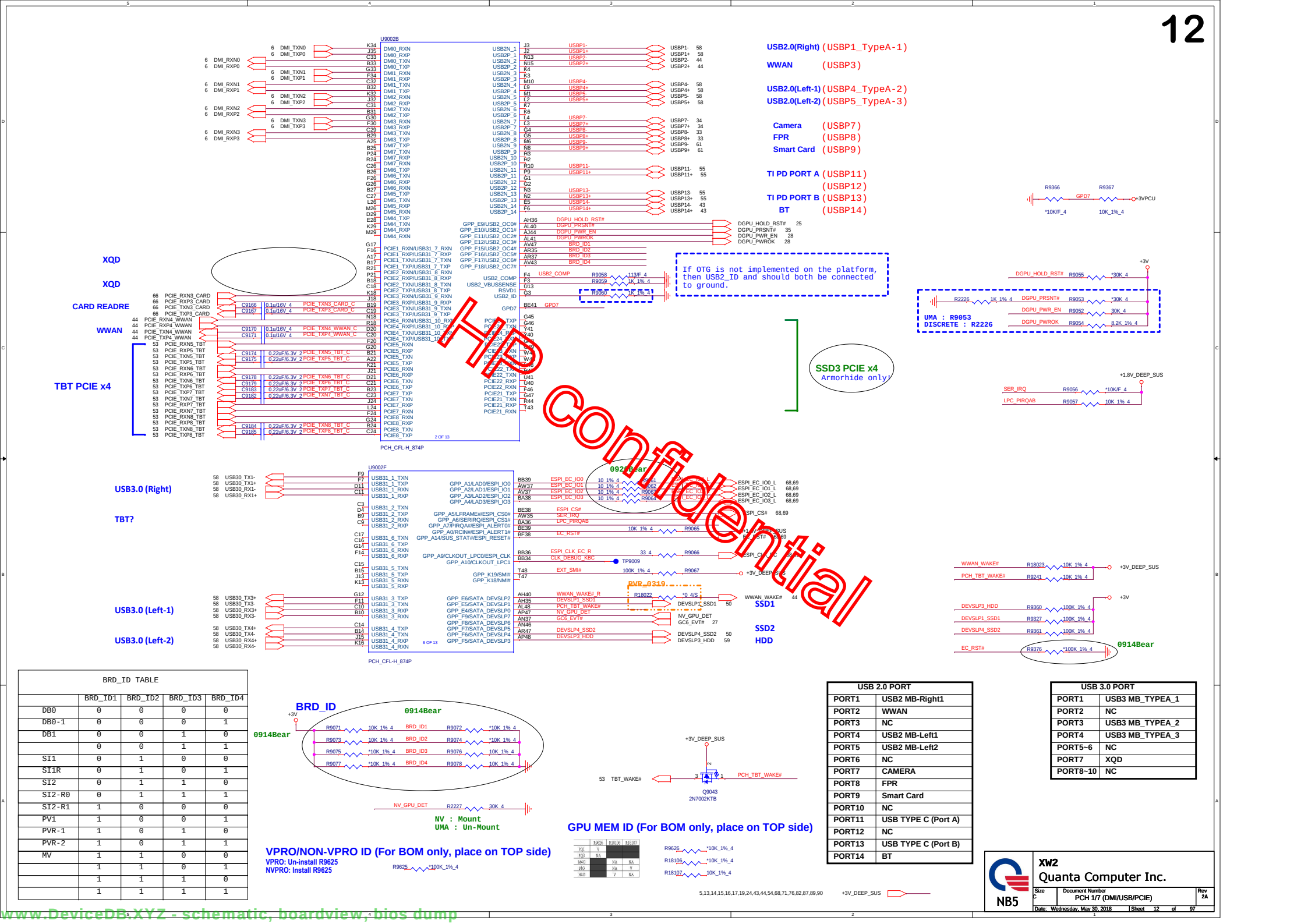

BRD_ID TABLE				
	BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4
DB0	0	0	0	0
DB0-1	0	0	0	1
DB1	0	0	1	0
	0	0	1	1
SI1	0	1	0	0
SI1R	0	1	0	1
SI2	0	1	1	0
SI2-R0	0	1	1	1
SI2-R1	1	0	0	0
PV1	1	0	0	1
PVR-1	1	0	1	0
PVR-2	1	0	1	1
MV	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1

USB 2.0 PORT	
PORT1	USB2 MB-Right1
PORT2	WWAN
PORT3	NC
PORT4	USB2 MB-Left1
PORT5	USB2 MB-Left2
PORT6	NC
PORT7	CAMERA
PORT8	FPR
PORT9	Smart Card
PORT10	NC
PORT11	USB TYPE C (Port A)
PORT12	NC
PORT13	USB TYPE C (Port B)
PORT14	BT

USB 3.0 PORT	
PORT1	USB3 MB_TYPEA_1
PORT2	NC
PORT3	USB3 MB_TYPEA_2
PORT4	USB3 MB_TYPEA_3
PORT5~6	NC
PORT7	XQD
PORT8~10	NC

XW2
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NB5
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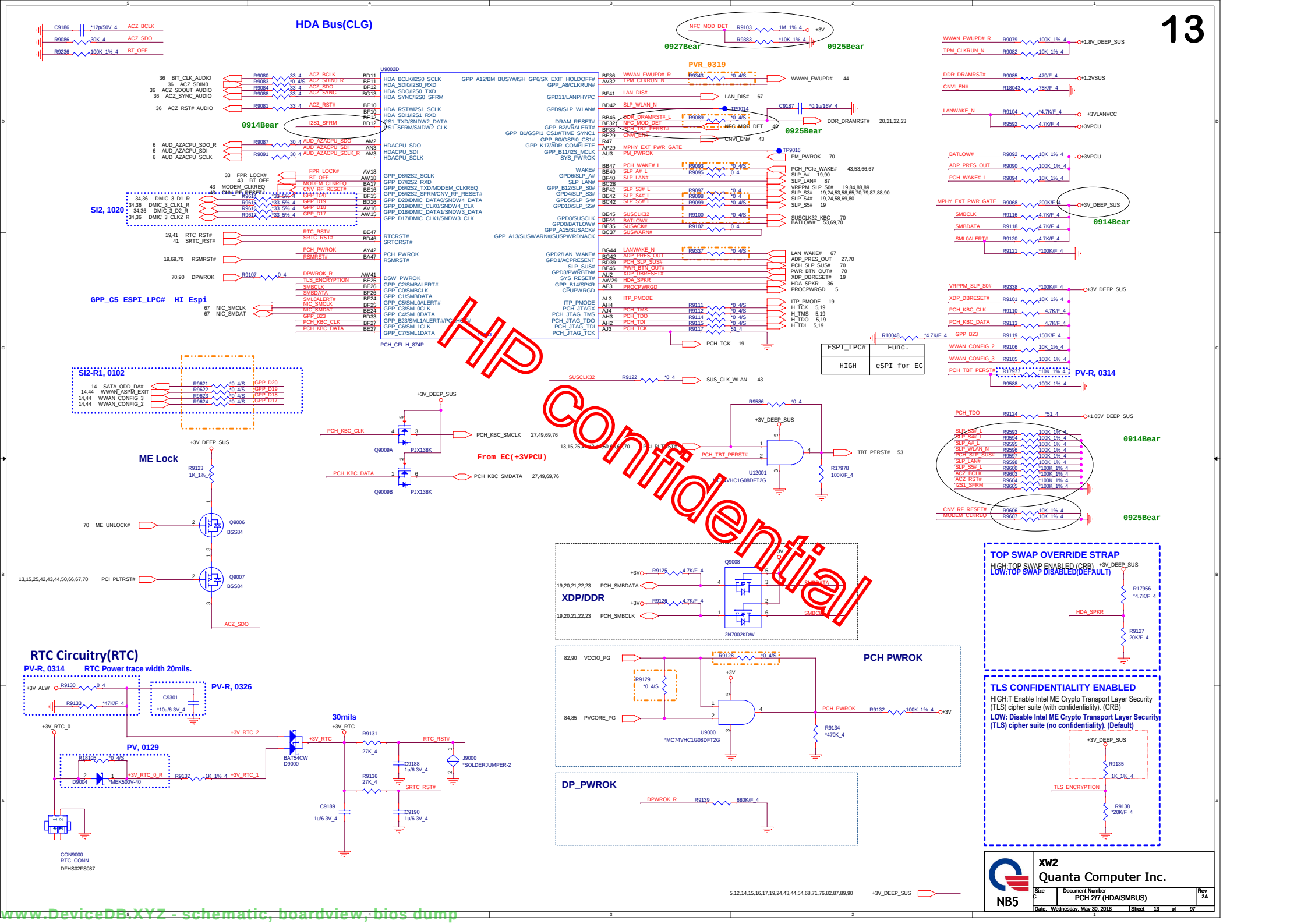

HSIO MUX PORT	
PCIE1	WLAN
PCIE2-4	NC
PCIE5-8	TITAN Ridge
PCIE9-12	SSD1 PCIE * 4
PCIE13-16	NC
PCIE17-20	SSD2 PCIE * 4

PLT_ID TABLE			
	PLT_ID0	PLT_ID1	PLT_ID2
Armorhide	0	1	1
Vortex	1	0	1
	0	1	0

SSD1 PCIE x4

WLAN

LAN PCIE

SSD1 PCIE x4

SSD2 PCIE x4

SSD1 PCIE x4

ODD SATA

HDD SATA

SSD2 PCIE x4

For SSD1 Det (SATA1A)

For SSD2 Det (SATA4)

SI2, 1121 SATA LED

For debug only remove from MV

24-MHz Crystal Specifications (Sheet 2 of 2)

Parameter	Symbol	Recommended Value
Temperature Stability	Df/f$_0$	±30ppm
Aging	Df/f$_0$	±5ppm
Crystal Loading	C$_{load}$	18-20pF

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-H needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-H.

Crystal Components with Surrounding 10 mil Wide GND Shield Trace Break Out:4-10 mil Wide GND Shield Trace

RTC Clock 32.768KHz

0914Bear

SI2-R1, 0102

SI2-R, 0112

SSD1

GFX

LAN

WLAN

Card reader

TBT

SSD2

XQD

WWAN

SSD3

0927Bear

0920Bear

PV 0123

GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
GPP_J9	1.8V VCCPSPI	Rising edge of RSMRST#	The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail Note: If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

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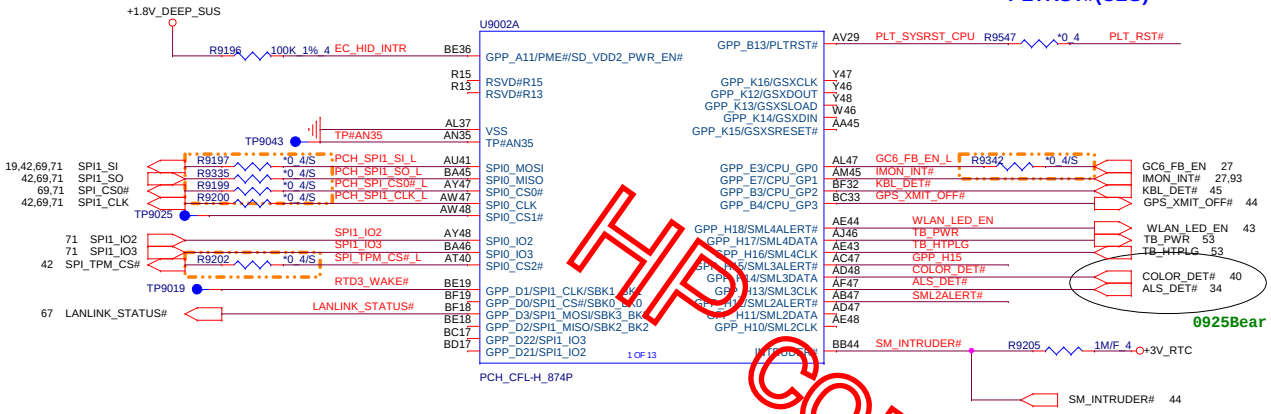
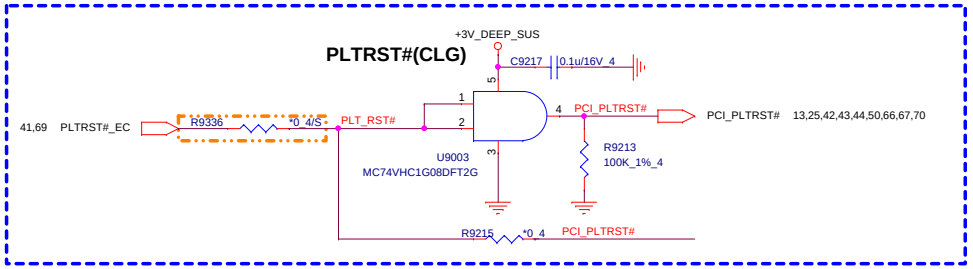
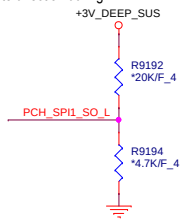
PCH Strap Pin





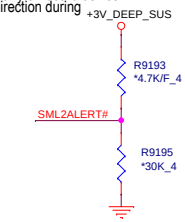
RESERVED

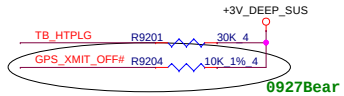
This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

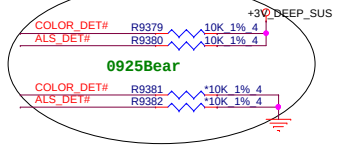


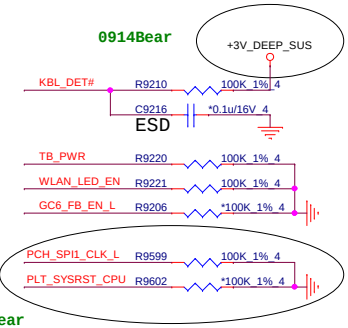
ESPI FLASH SHARING MODE

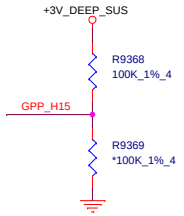
HIGH:SLAVE ATTACEHD FLASH SHARING
LOW: 0: MASTER ATTACHED FLASH SHARING
This strap should sample LOW.
There should NOT be any on-board device driving it to opposite direction during strap sampling.





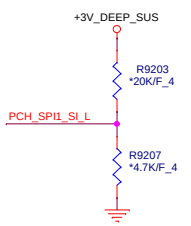






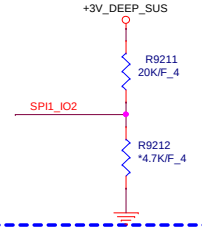
RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



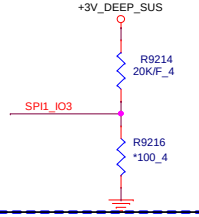
RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



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Boot BISO Destination: HIGH=LPC, LOW=SPI
GPP_B22 LOW

U9002K

PCH_CFL-H_874P

CLICKPAD/NFC/MCU Touch Screen

TBT

U9002E

PCH_CFL-H_874P

This signal has a weak internal pull-down.
0 = Port C and D is not detected.
1 = Port C and D is detected.

NO REBOOT IF SAMPLED HIGH
HIGH:TOP SWAP ENABLED (CRB)
LOW: Disable "No Reboot" mode. (Default)

GPP_B22 LOW

RESERVED
This strap should sample LOW.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

Intel ME STRAP

0914Bear

0914Bear

NB5	XW2 Quanta Computer Inc.	
Size Custom	Document Number PCH 5/7 (GPIO)	Rev 2A
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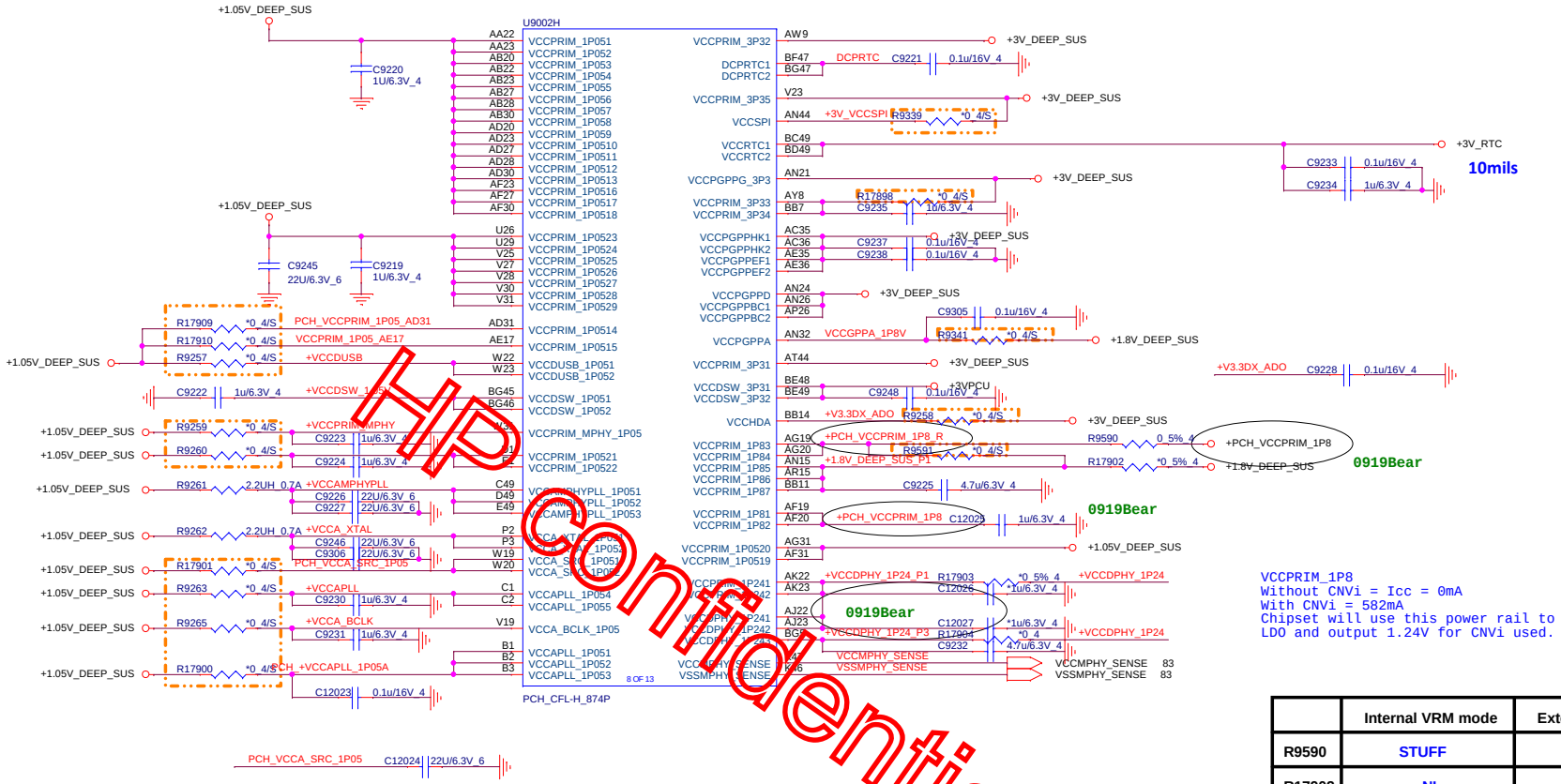

	Internal VRM mode	External VRM mode
R9590	STUFF	NI
R17902	NI	STUFF
R9591	STUFF	STUFF
C9225	STUFF 4.7u	STUFF 1u

5,12,13,14,15,16,19,24,43,44,54,68,71,76,82,87,89,90 +3V_DEEP_SUS

XW2
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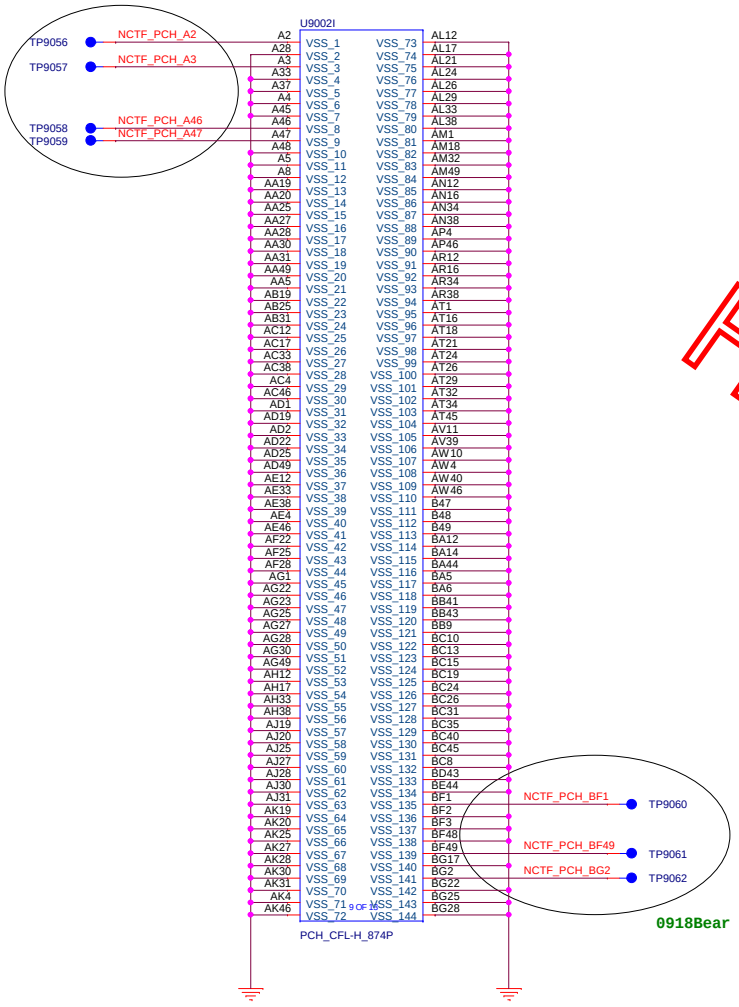
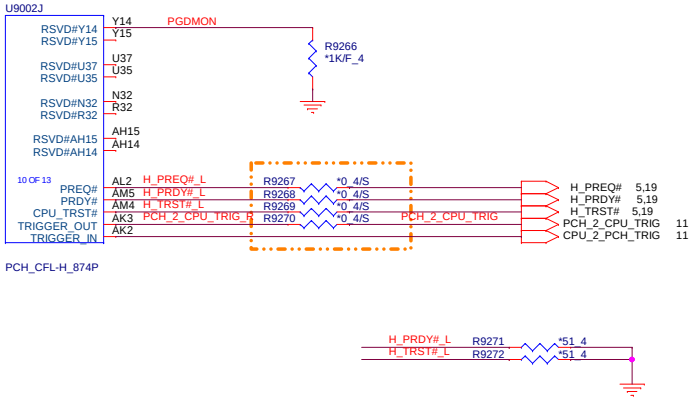
0918Bear





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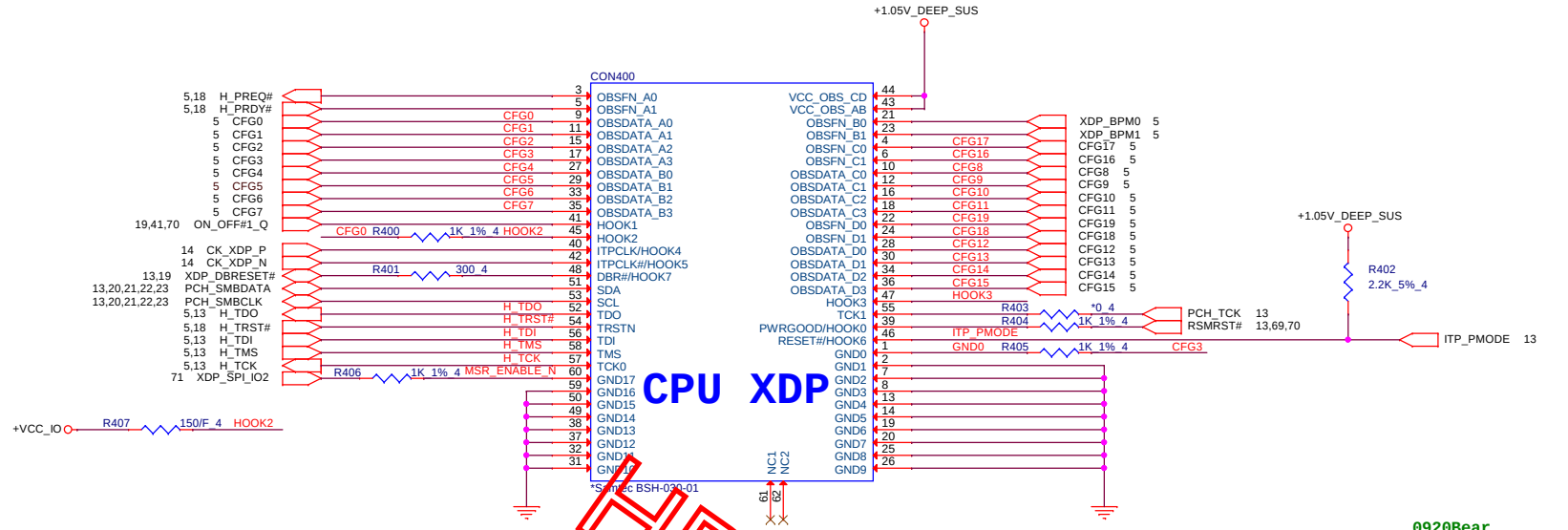

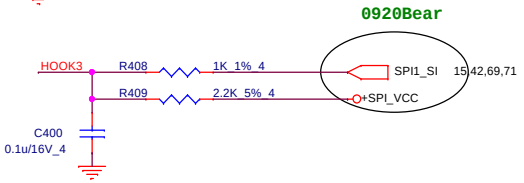

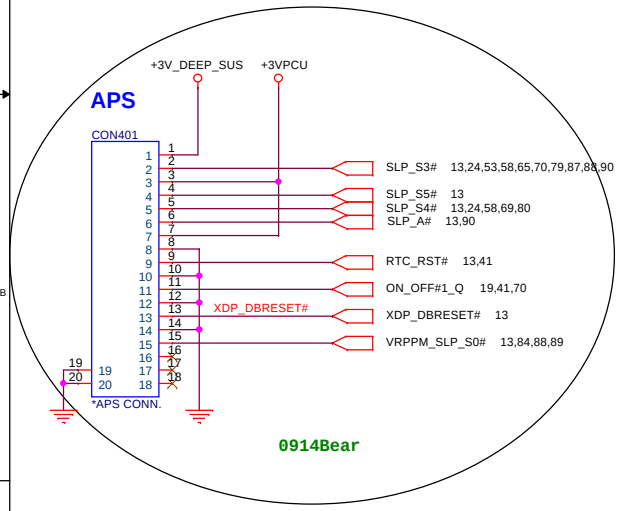

+3V_DEEP_SUS 5,12,13,14,15,16,17,24,43,44,54,68,71,76,82,87,89,90
+1.05V_DEEP_SUS 13,14,17,73,83,88,91
+VCC_IO 6,9,48,73,82
+3VPCU 12,13,17,24,34,41,43,44,45,47,49,54,55,68,69,70,71,75,76,77,78,79,80,81,82,84,85,86,87,88,89,90,91,94

NB5	XW2 Quanta Computer Inc.	
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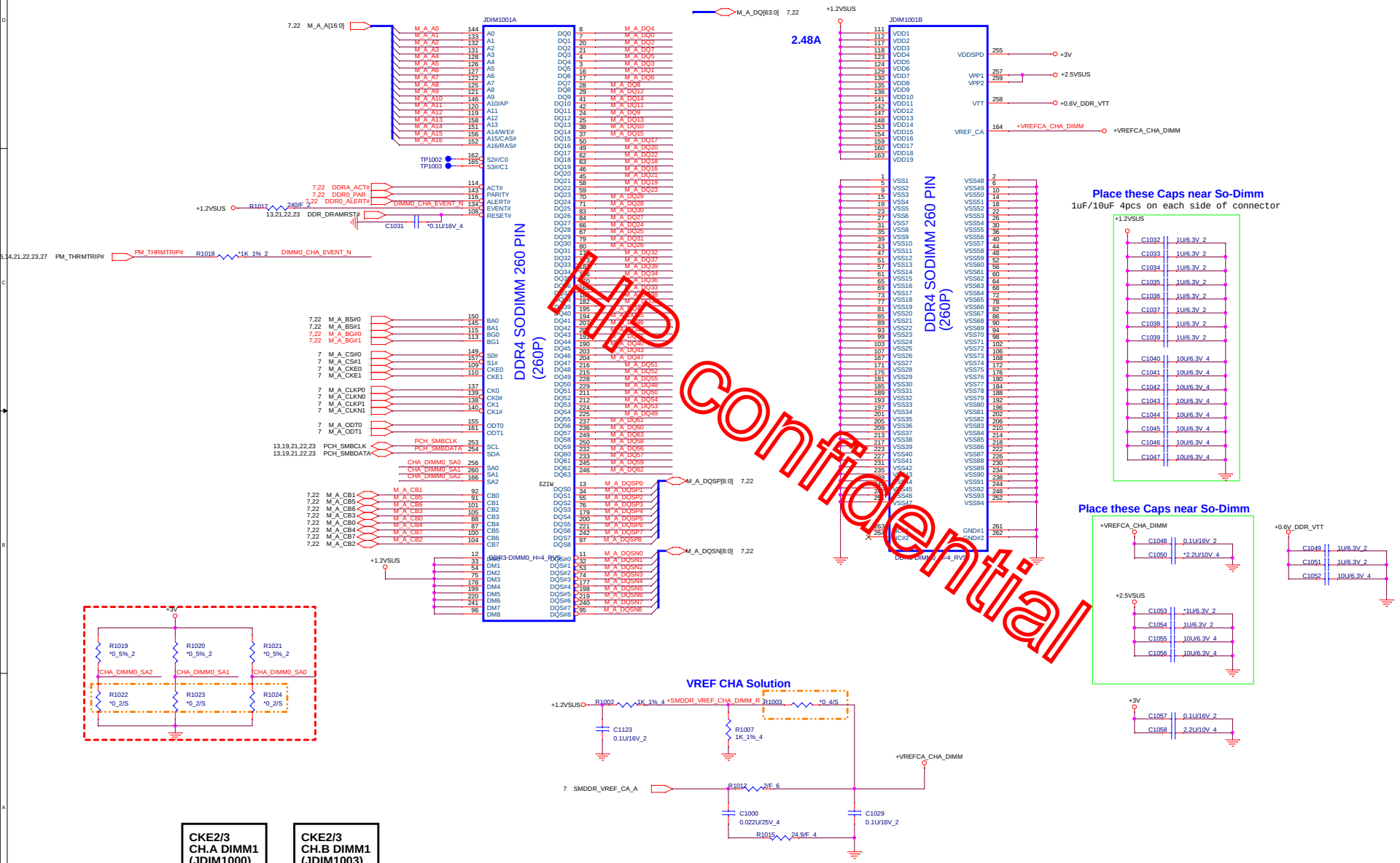

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Size: Custom	Document Number: DDR4 Memory Down (CH. A)
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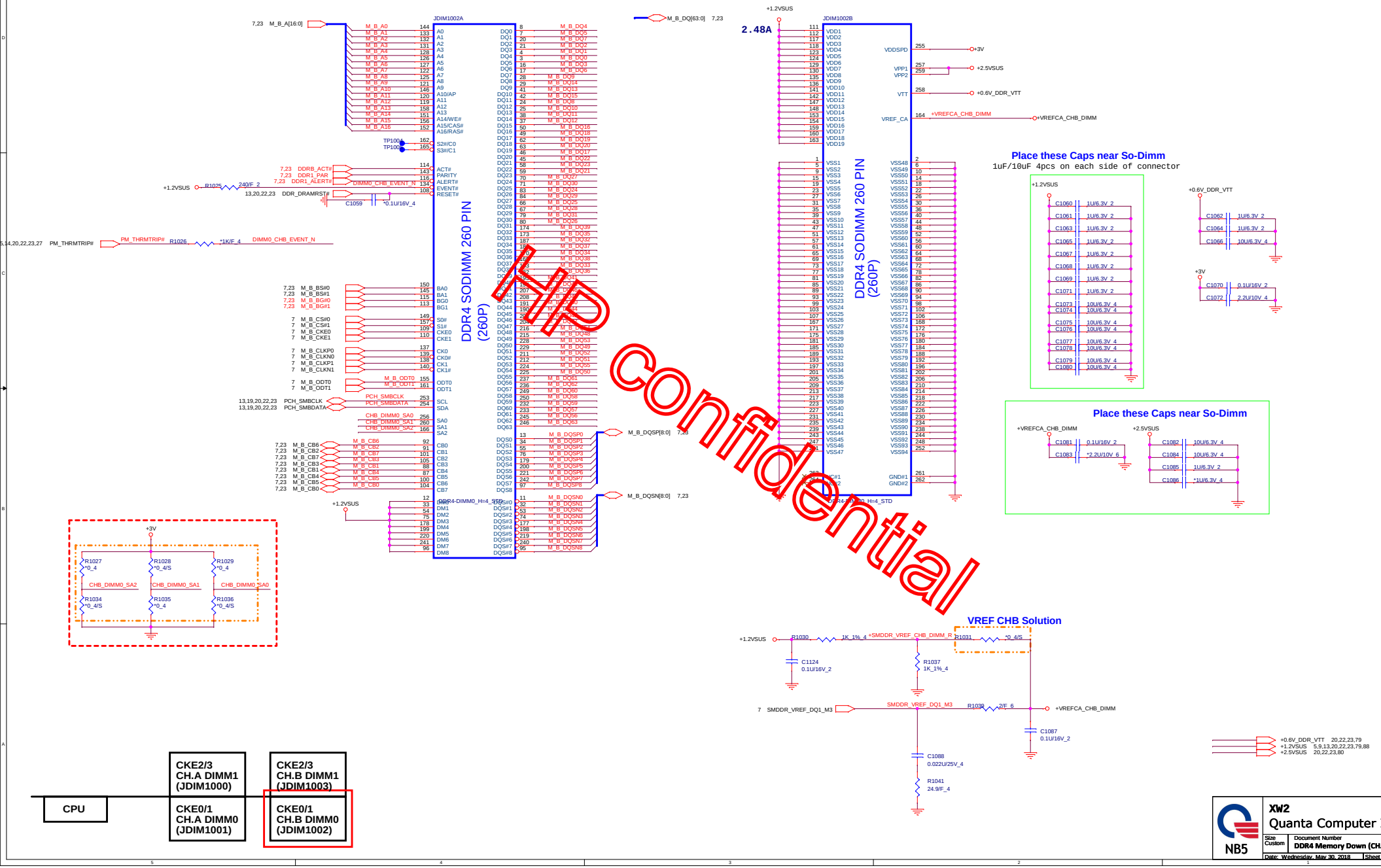
NB5



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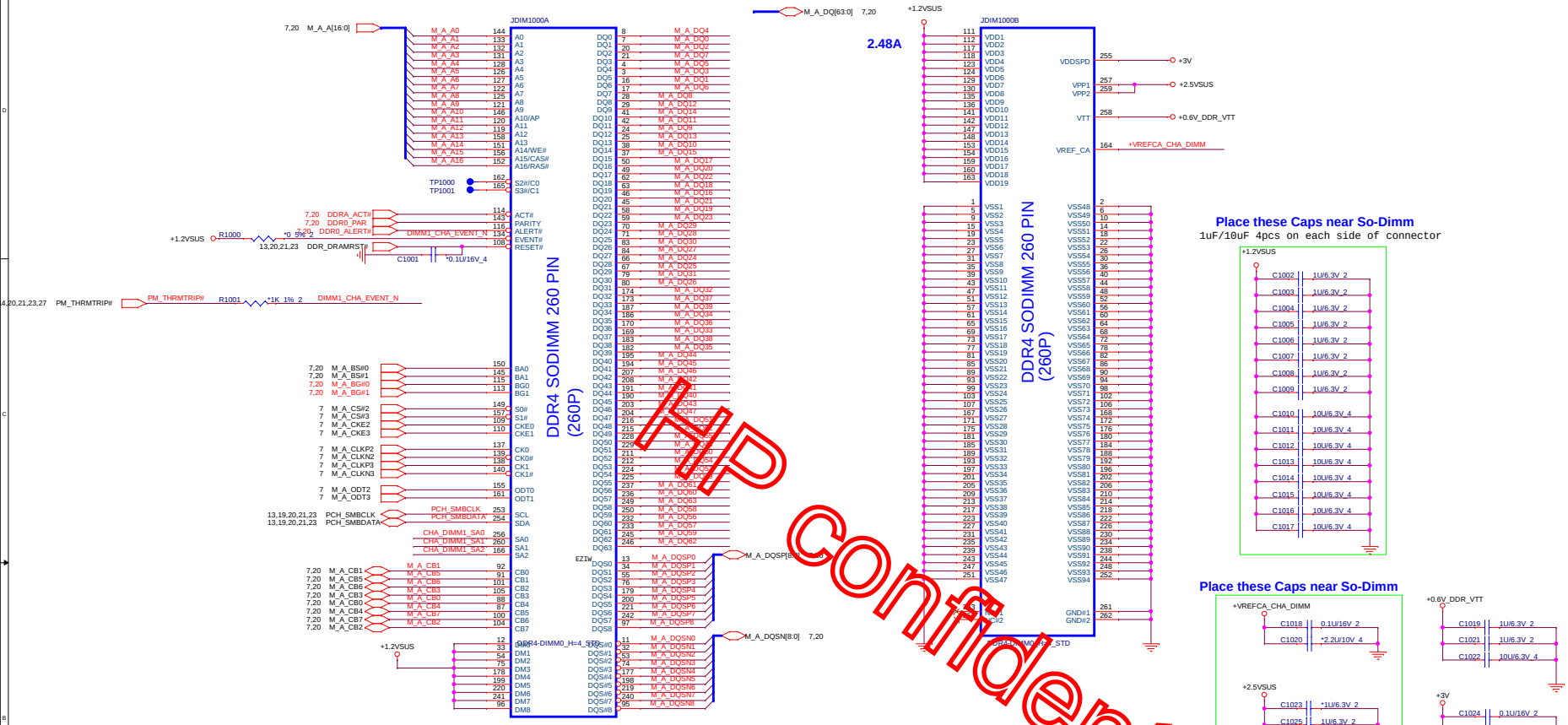
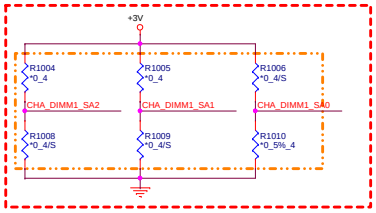


Place these Caps near So-Dimm
1uF/10uF 4pcs on each side of connector

Place these Caps near So-Dimm



CPU	CKE2/3 CH.A DIMM1 (JDIM1000)	CKE2/3 CH.B DIMM1 (JDIM1003)
	CKE0/1 CH.A DIMM0 (JDIM1001)	CKE0/1 CH.B DIMM0 (JDIM1002)

NB5	XW2 Quanta Computer Inc.	
	Size: Custom	Document Number: DDR4 Memory Down (CH. A)
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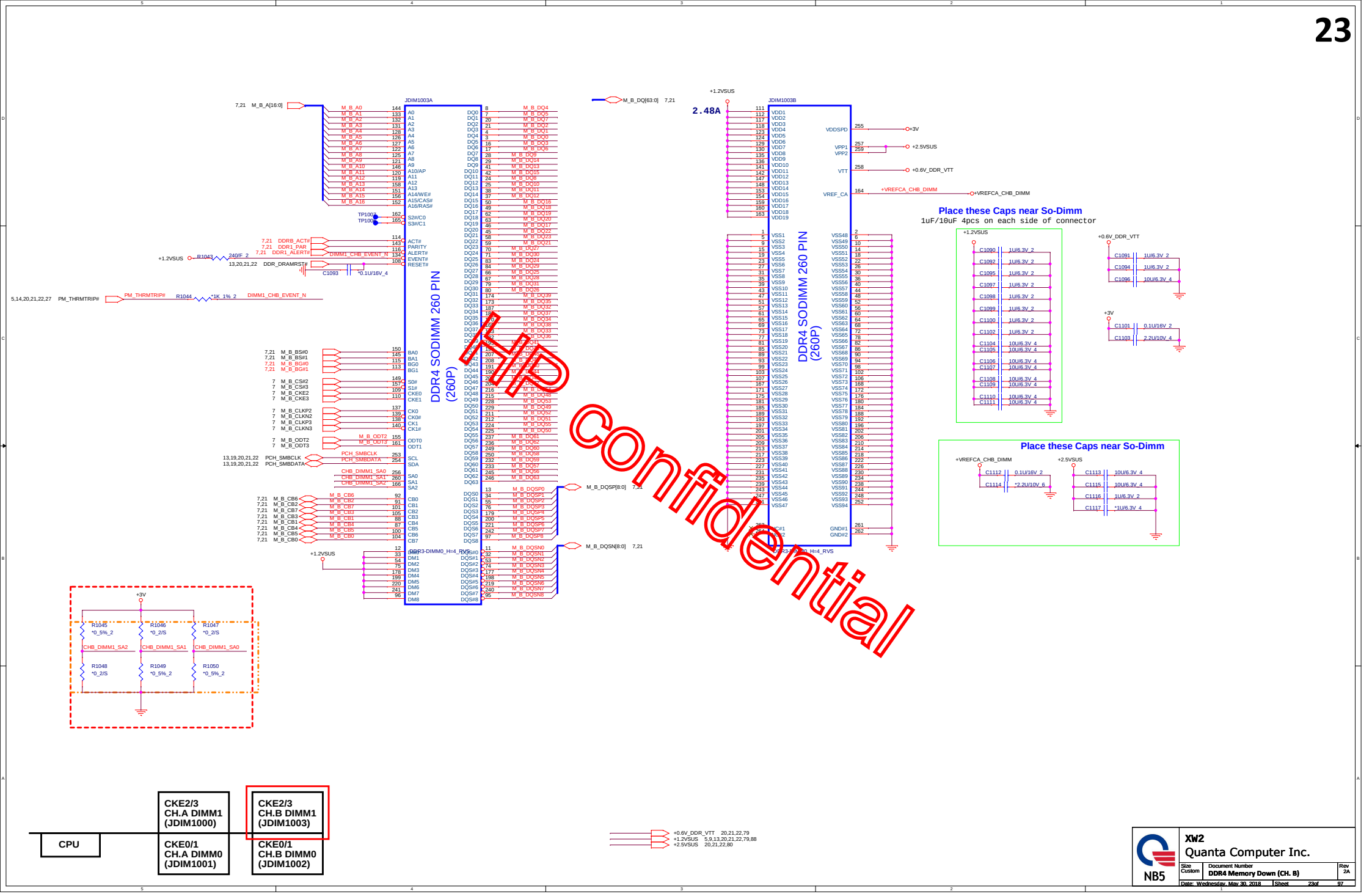

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NB5	Size: Custom; Document Number: DDR4 Memory Down (CH. B); Rev: 2A
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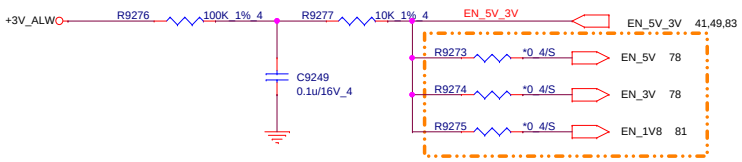

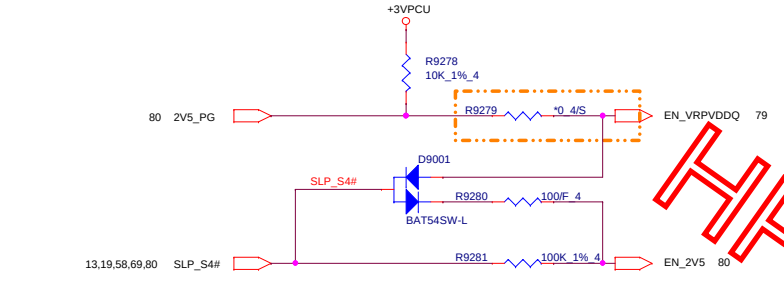

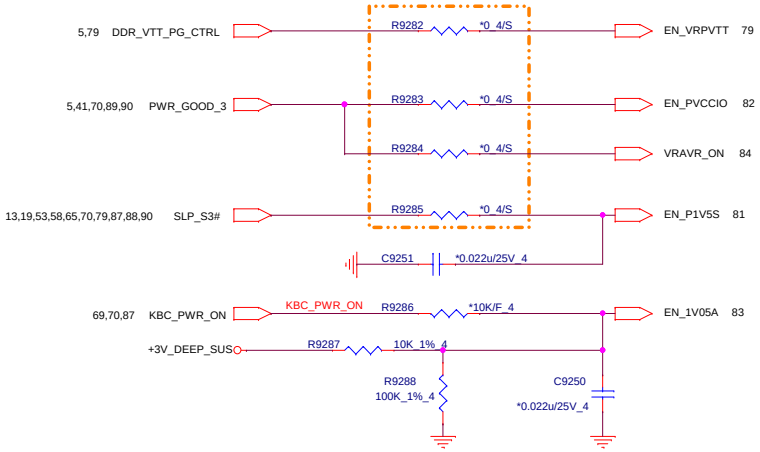

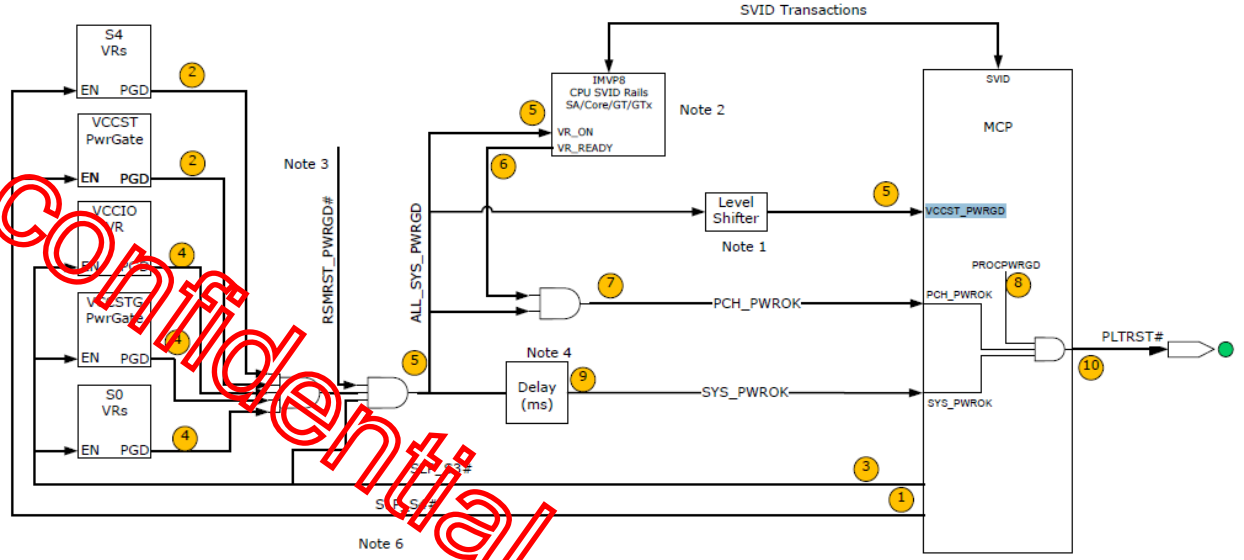

NB5	XW2 Quanta Computer Inc.	
Size Custom	Document Number Power enable	Rev 2A
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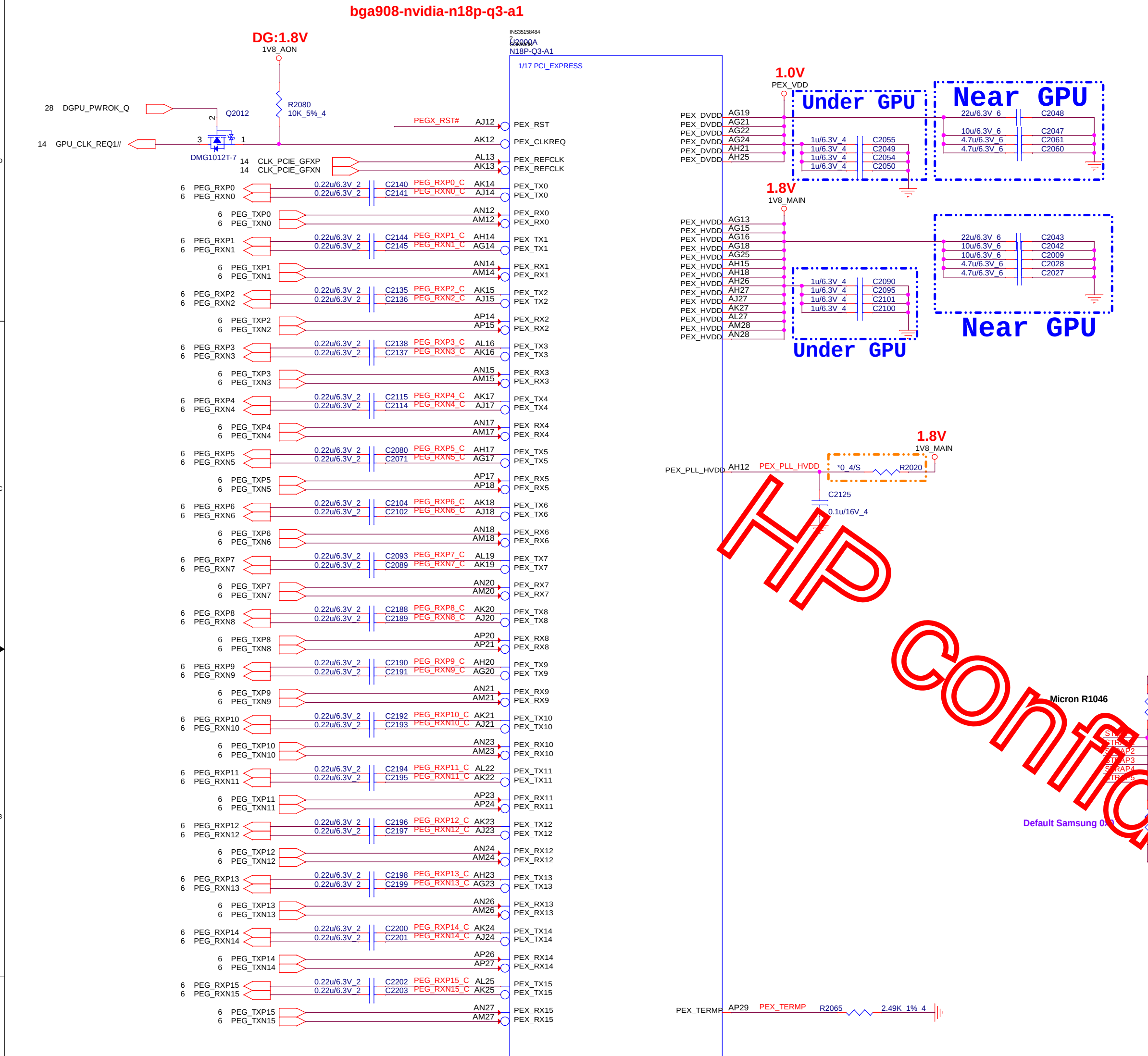
bga908-nvidia-n18p-q3-a1



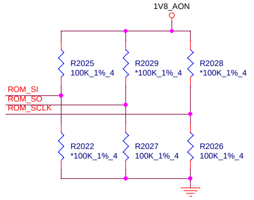


Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_ EXPOSED	SOR2_ EXPOSED	SOR1_ EXPOSED	SOR0_ EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

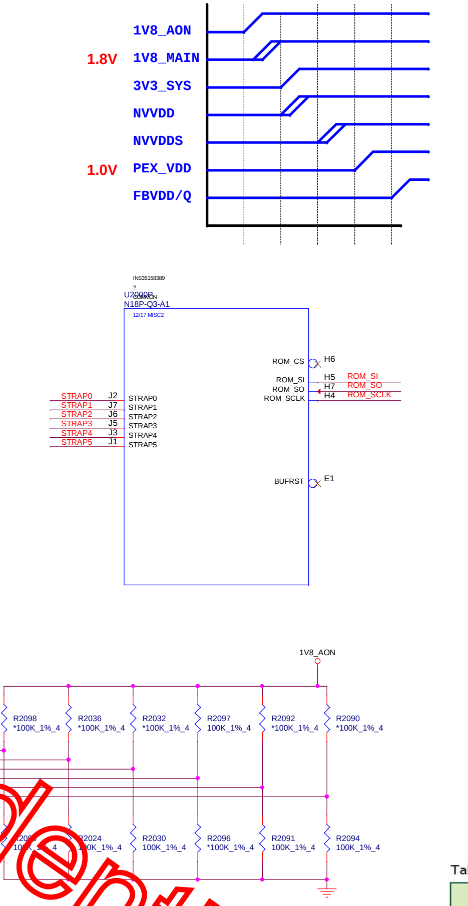


Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0

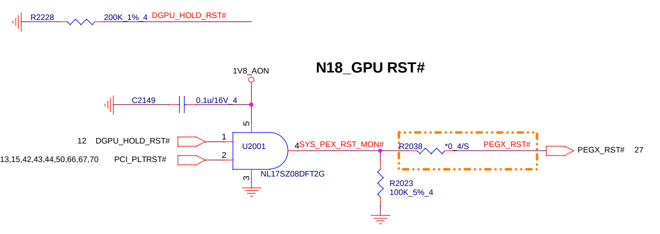
Display output from GPU

STRAP[2:0] VRAM Table for N18P-Q3/Q1 & N18M-Q3 GDDR5 Recommended Memories

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	QB P/N	
0x0	GDDR5 256Mx32 8 GHz	Samsung B die	K4G80325FB-HC25	AKD58WWT501	AKD58WWT502	
0x1	GDDR5 256Mx32 8 GHz	Micron A die	MT51J256M32HF-80:A	AKG5QGUTL01	AKG5QGUTL02	
0x2						

Default

N18_GPU RST#



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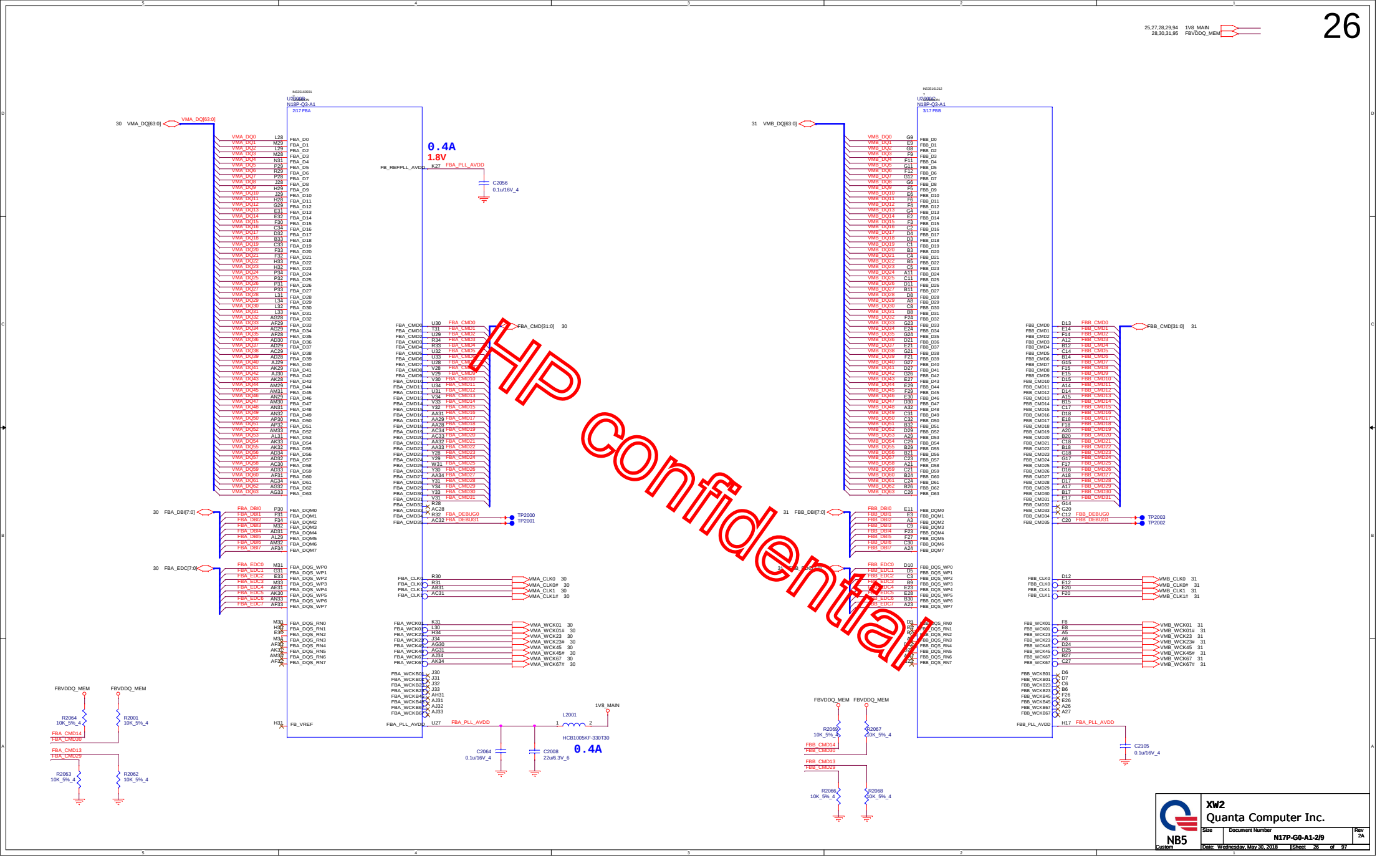

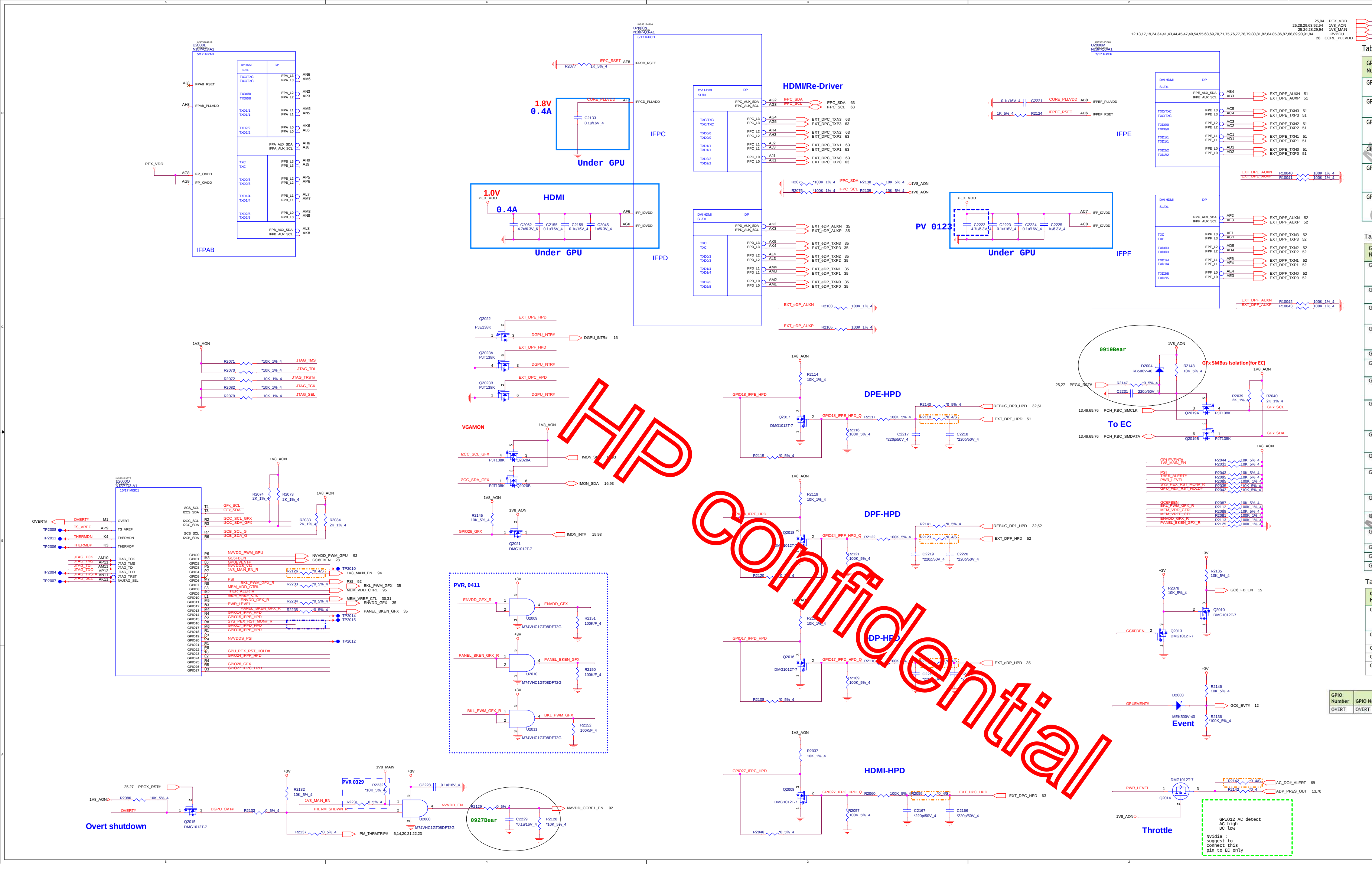

Table 14.2 GPIO Descriptions for GB4C-128 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	0 to1V8 PWM output
GPIO1	GC6M: GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source 10 KΩ pull-down
GPIO2	GC6M: GPU_EVENT#/ WAKE*	I	GPU wake signal for GC6 2.1	10KΩ pull-up to 1V8_AON, unless driven actively.
GPIO3	NVVDD_SRAM_PWM	O	PWM output to control the SRAM power supply	0 to 1V8 output
GPIO4	GC6M:1V8_MAIN_EN	O	GPU power sequencing for GC6 2.1	Open Drain 10KΩ pull-up to 1V8_AON
GPIO5	FRM_LCK	I	Active low Frame Lock	Open Drain 1V8 pull-up to 1V8AON

Table 14.2 GPIO Descriptions for GB4C-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO6	NVVDD_PSI	O	Phase Shedding (see Section 14.3.3)	10 kΩ pull-up to 1V8_AON to enable multiple phases
GPIO7	LCD_BL_PWM	O	Panel Backlight enable	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LCD_VDD Quadro:Power_Brake#	O	Panel Power enable	100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 kΩ pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	LCD Panel Backlight Enable	Panel Backlight Enable
GPIO14	HPD_IFPA	I	Hot Plug Detect for IFPA	Inverted input. See Figure 14.5
GPIO15	HPD_IFPB	I	Hot Plug Detect for IFPB	Inverted input. See Figure 14.5
GPIO16	GC6M: SYS_PEX_RST_MON#	O	System side PCIe reset monitor	10 kΩ pull-up to 1V8_AON unless actively driven
GPIO17	HPD_IFPD	I	Hot Plug Detect for IFPD	Inverted input. See Figure 14.5
GPIO18	HPD_IFPE	I	Hot Plug Detect for IFPE	Inverted input. See Figure 14.5
GPIO19	3D Vision	O	3D Vision L/R Signal	100 kΩ pull-down
GPIO20	GC5_MODE			
GPIO21	UNUSED	I/O		
GPIO22	UNUSED	I/O		

Table 14.2 GPIO Descriptions for GB4C-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO23	GC6M: GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	Open Drain 10 kΩ pull-up to a gated 3V3
GPIO24	HPD_IFPF	I	Hot plug detect for IFPF	Inverted input. See Figure 14.5
GPIO25	UNUSED			
GPIO26	UNUSED			
GPIO27	HPD_IFPC	I	Hot plug detect for IFPC	Inverted input. See Figure 14.5

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AON

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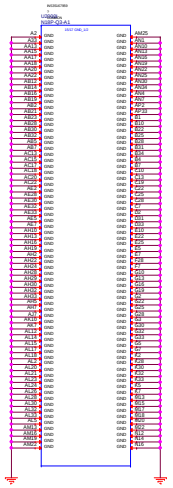

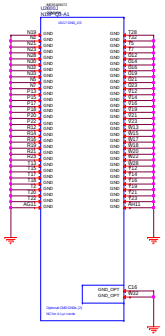

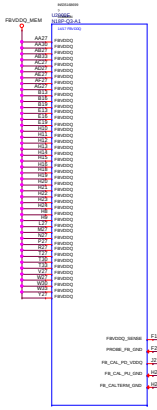

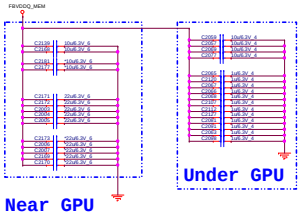

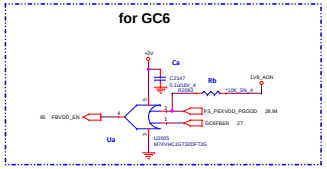

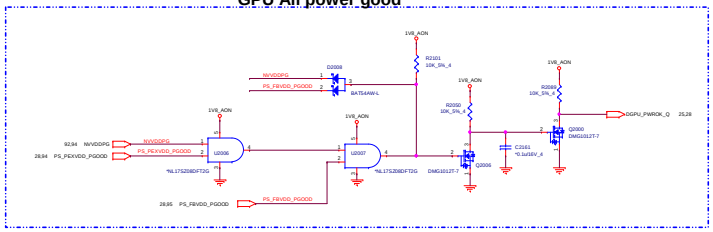

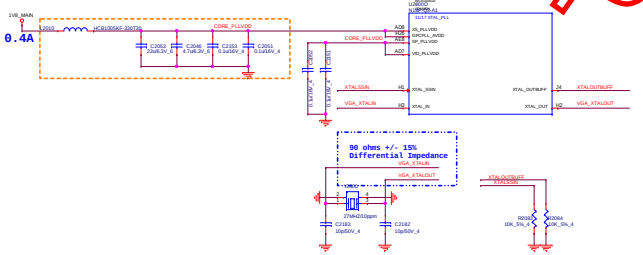

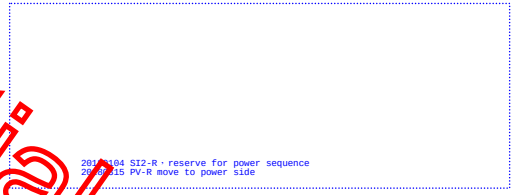

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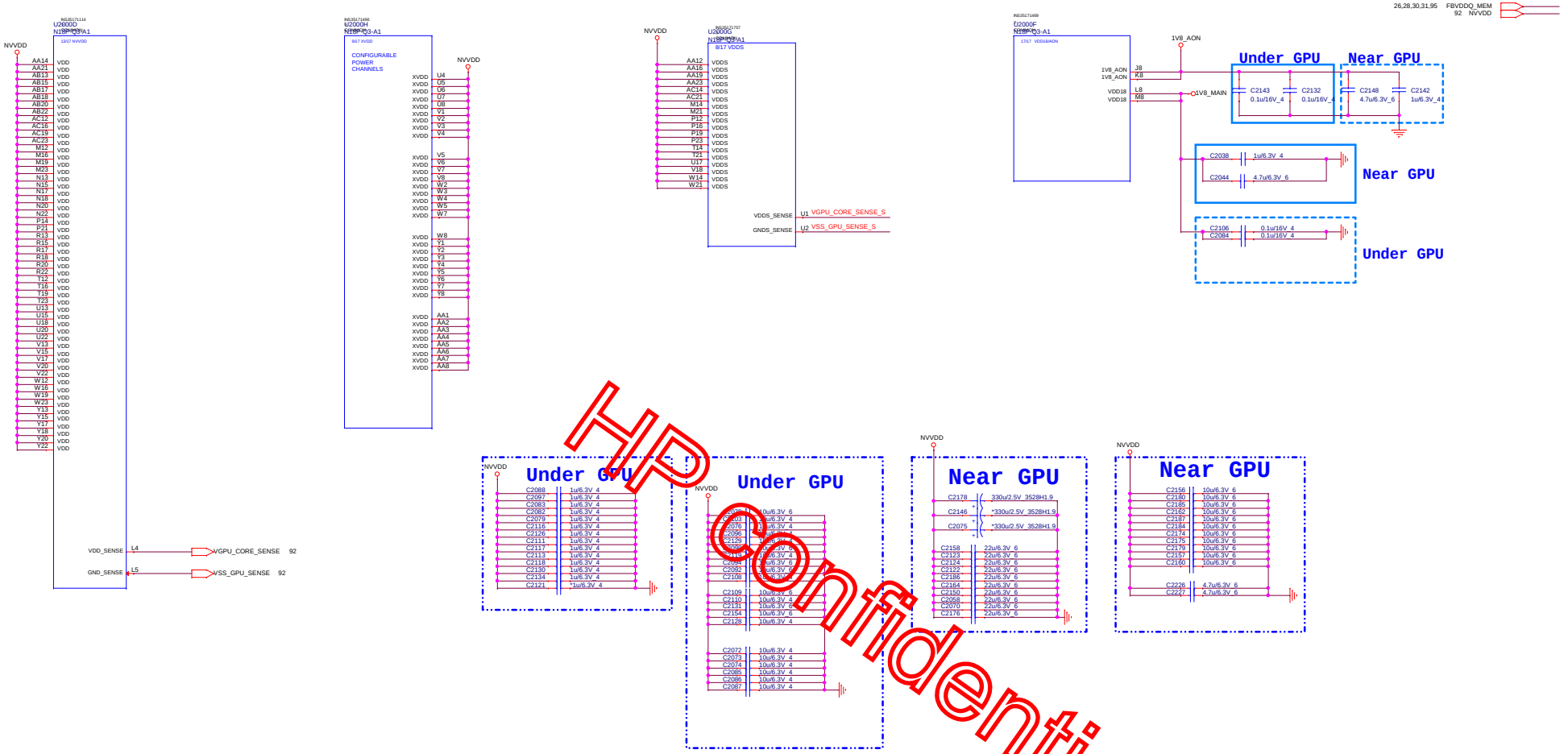

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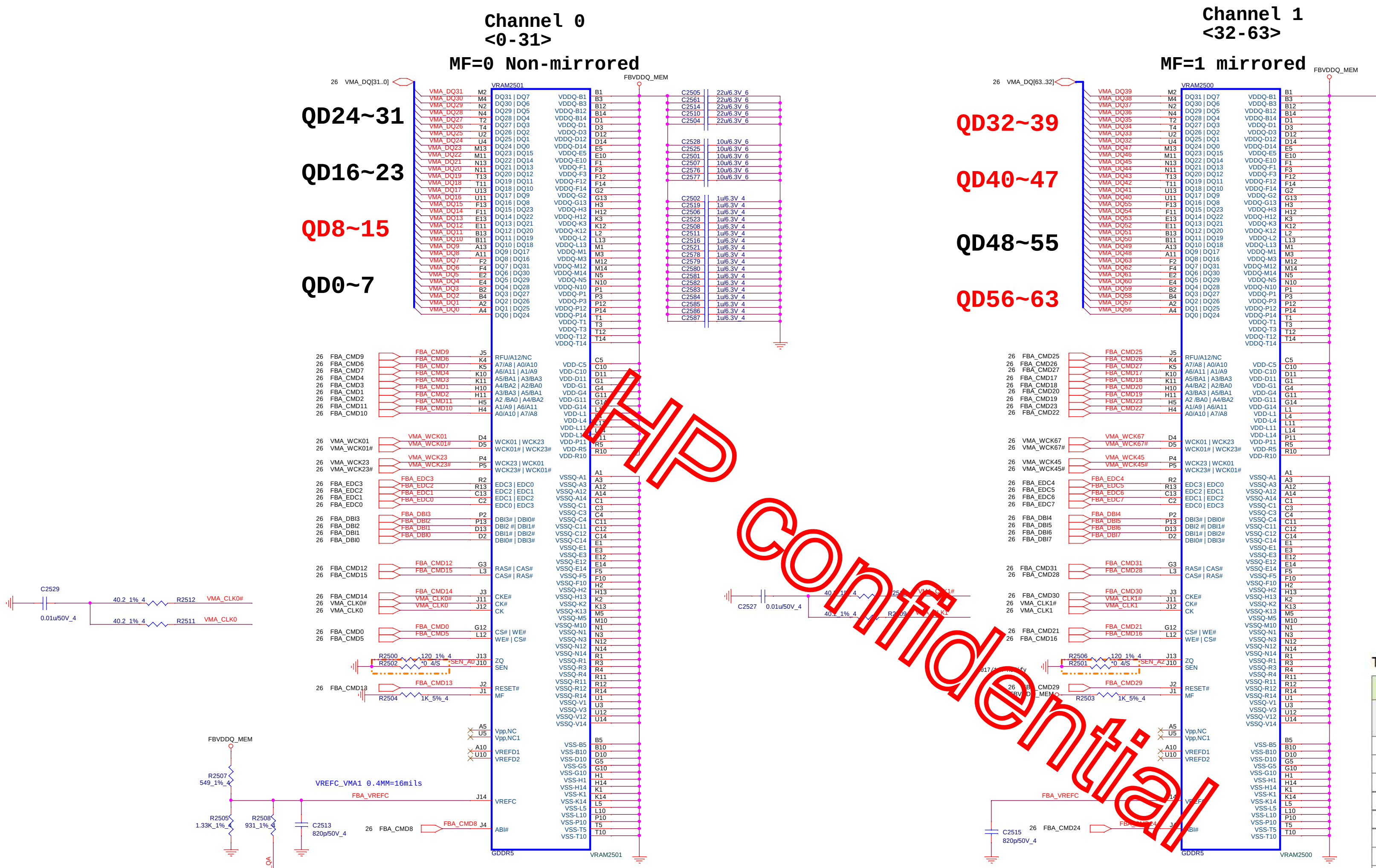
CHANNEL A: 2G/4G GDDR5



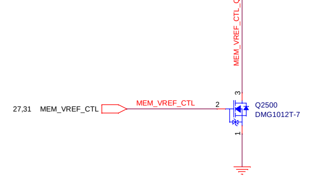


Table 9.19 DRAM-Side FBVDD/FBVDDQ Decoupling (Combined Rail)

Decoupling Capacitors		Recommended Quantity and Placement (per DRAM device)	
Capacitance	Type [Size]	Quantity	Placement (by DRAM Interface Mode)
Combined FBVDD-FBVDDQ Rail			
1.0 uF	X6S [0402]	10	For x32 DRAM: Under the DRAM FBVDD or FBVDDQ ball.
10 uF	X6S [0603]	4	For x16 DRAM in a "clamshell" PCB configuration: As close to DRAM periphery as possible. Ensure at least 2 GND vias and 2 power vias for each decoupling capacitor.
1.0 uF	X6S [0402]	8 additional	For x32 DRAM: Choose x32 interface to achieve max POR DRAM speeds. Add these additional decoupling caps under the DRAM FBVDD/Q ball; should share existing FBVDD/Q ball via if possible. See Figure 9.23 for an example.
10 uF	X6S [0603]	2	Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.
22 uF	X6S [0603]	5	For 4 GHz WCK (8 Gbps data rates): Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.

Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

CHANNEL B: 2G/4G GDDR5

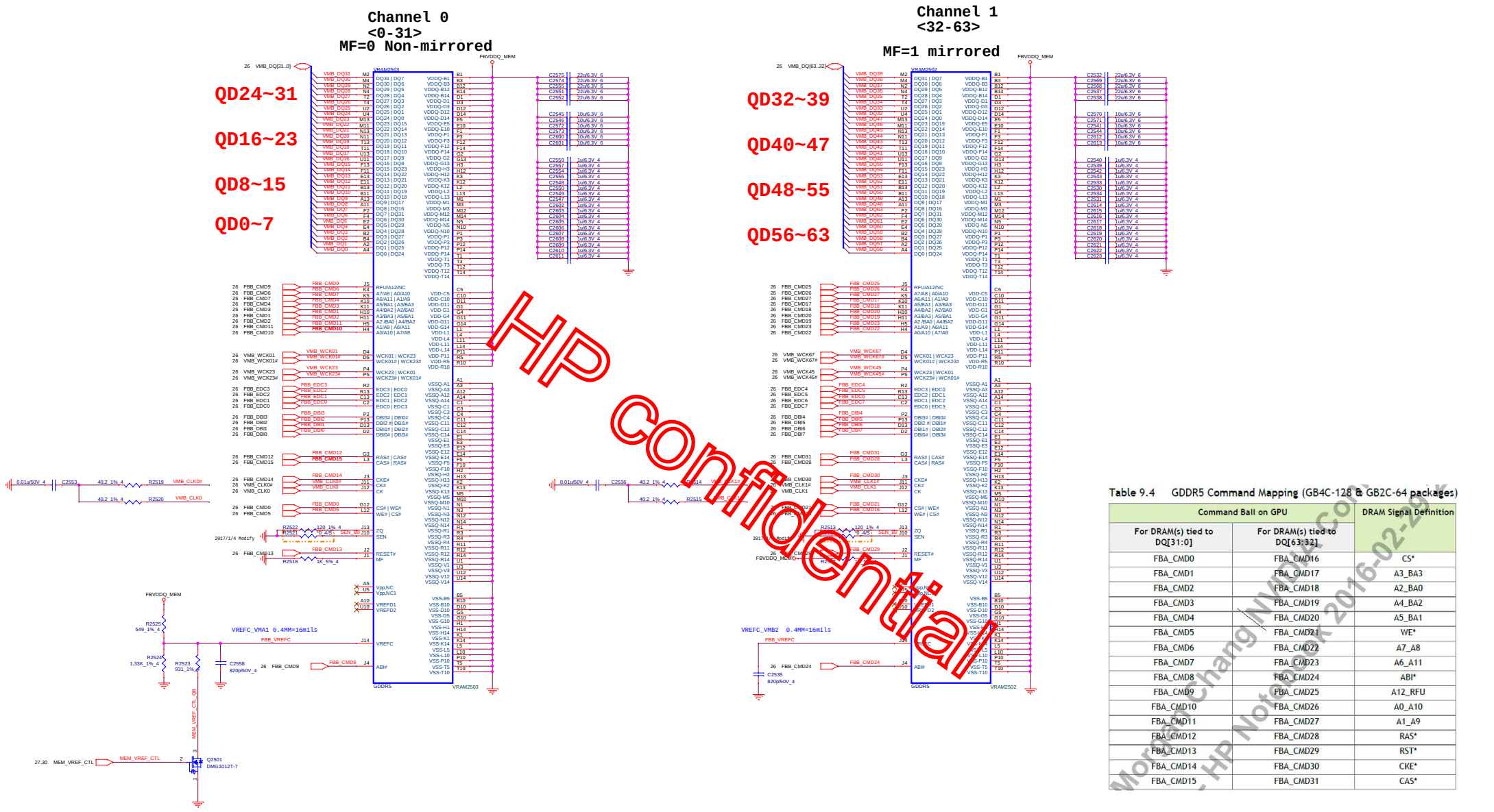


Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

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NB5 Custom
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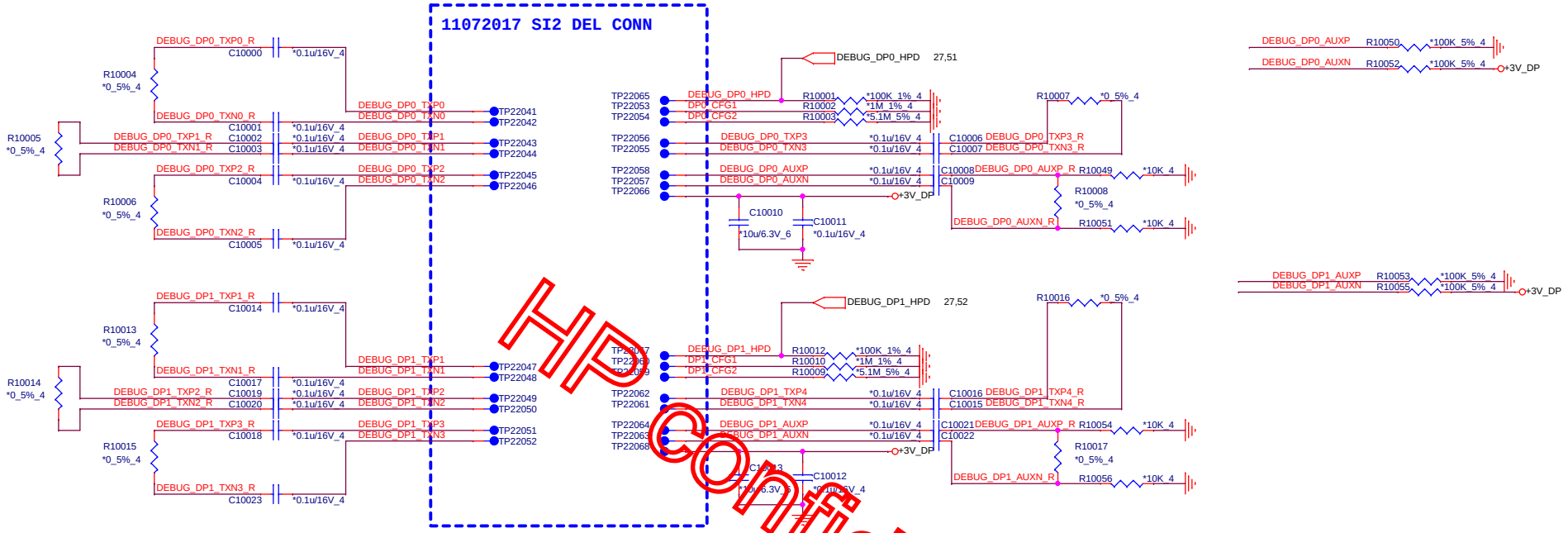
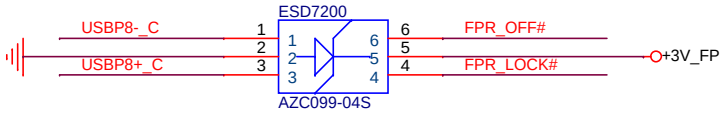
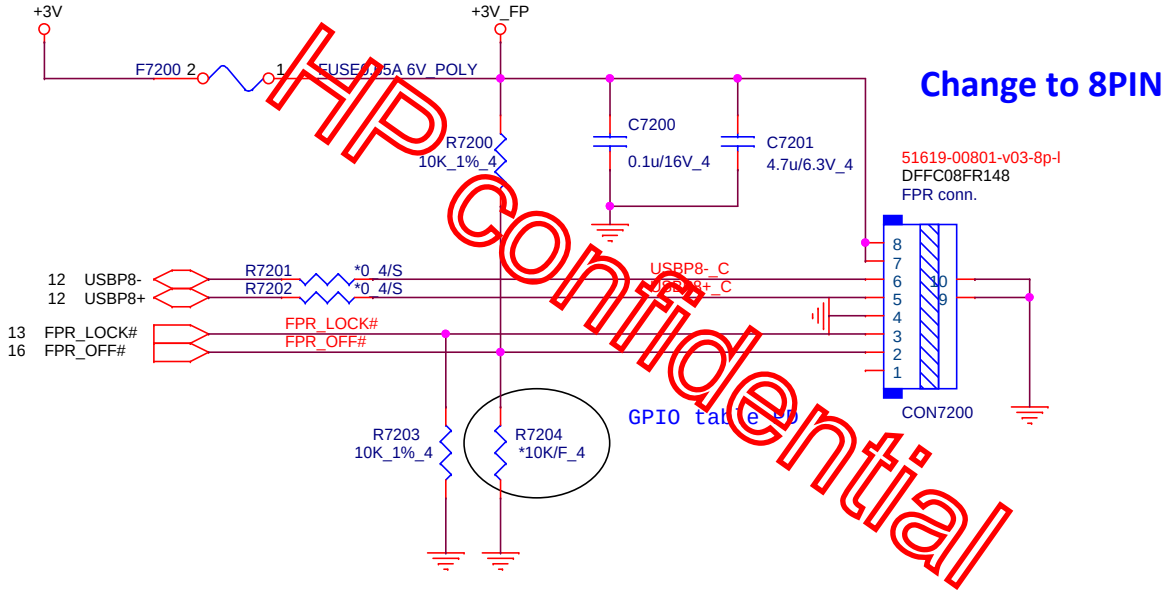


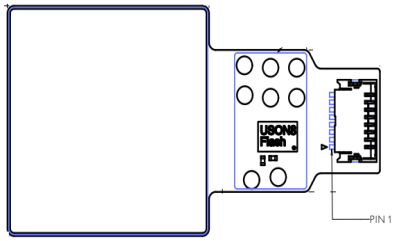
Table 2-1: Source-Side Mini DisplayPort Connector Pin Assignment

Top Row			Bottom Row		
Pin Number	Signal Type	Pin Name	Pin Number	Signal Type	Pin Name
1	GND	GND	2	In	Hot Plug Detect
3	Out	ML_Lane 0 (p)	4	CONFIG (see note 1)	CONFIG1
5	Out	ML_Lane 0 (n)	6	CONFIG (see note 1)	CONFIG2
7	GND	GND	8	GND	GND
9	Out	ML_Lane 1 (p)	10	Out	ML_Lane 3 (p)
11	Out	ML_Lane 1 (n)	12	Out	ML_Lane 3 (n)
13	GND	GND	14	GND	GND
15	Out	ML_Lane 2 (p)	16	I/O	AUX_CH (p)
17	Out	ML_Lane 2 (n)	18	I/O	AUX_CH (n)
19	GND	GND	20	PWR Out (see note 2)	DP_PWR

Fingerprint Conn







PIN	DEFINITION
1	3.3V
2	3.3V
3	D-
4	D+
5	GND
6	LOCK_N
7	FPR_OFF
8	N/C

NB5

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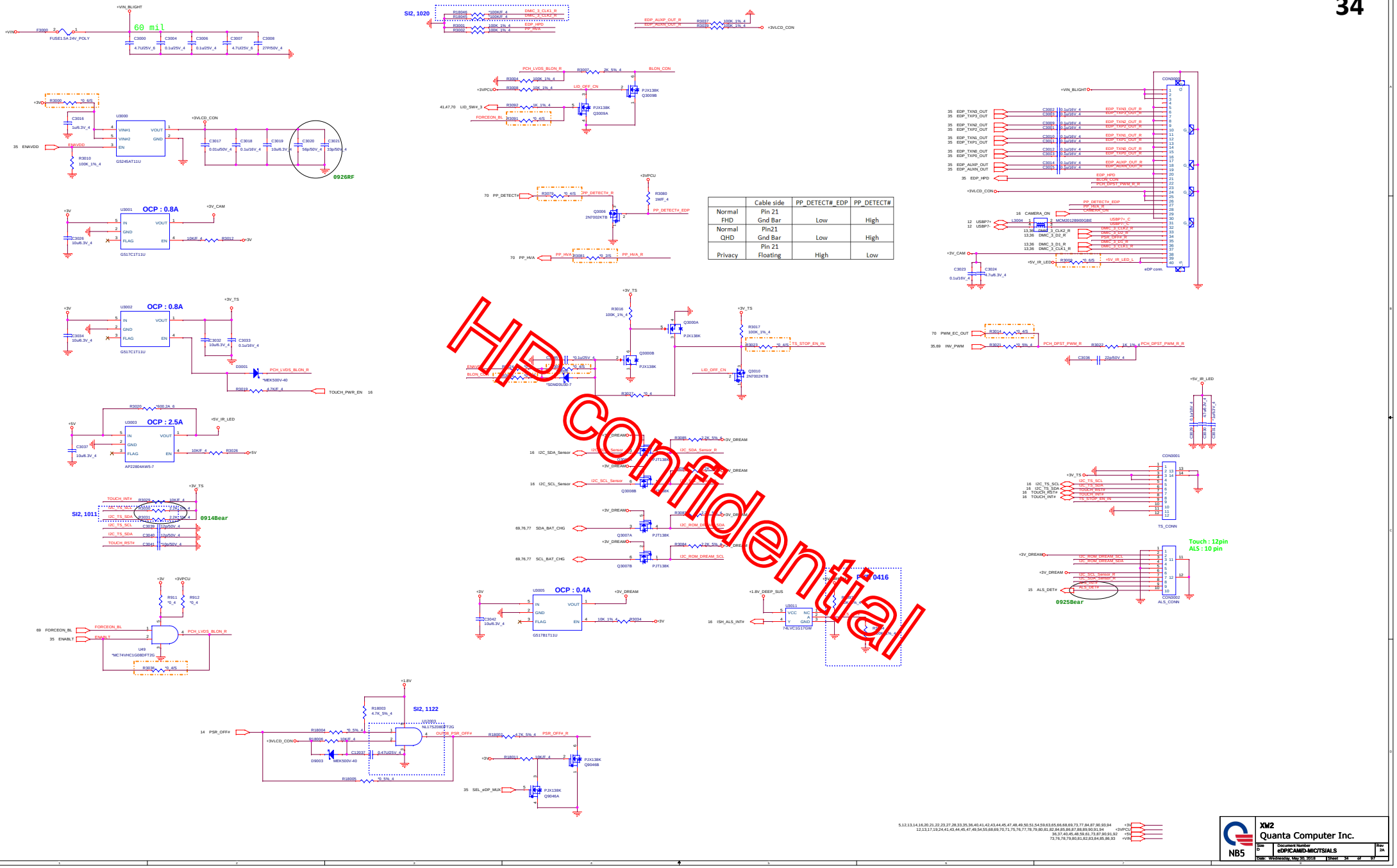
LID Switch



	Cable side	PP_DETECT#_EDP	PP_DETECT#
Normal FHD	Pin 21 Gnd Bar	Low	High
Normal QHD	Pin21 Gnd Bar	Low	High
Privacy	Pin 21 Floating	High	Low

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NB5
Size: D
Document Number: eDP/CAMID-MIC/TS/ALS
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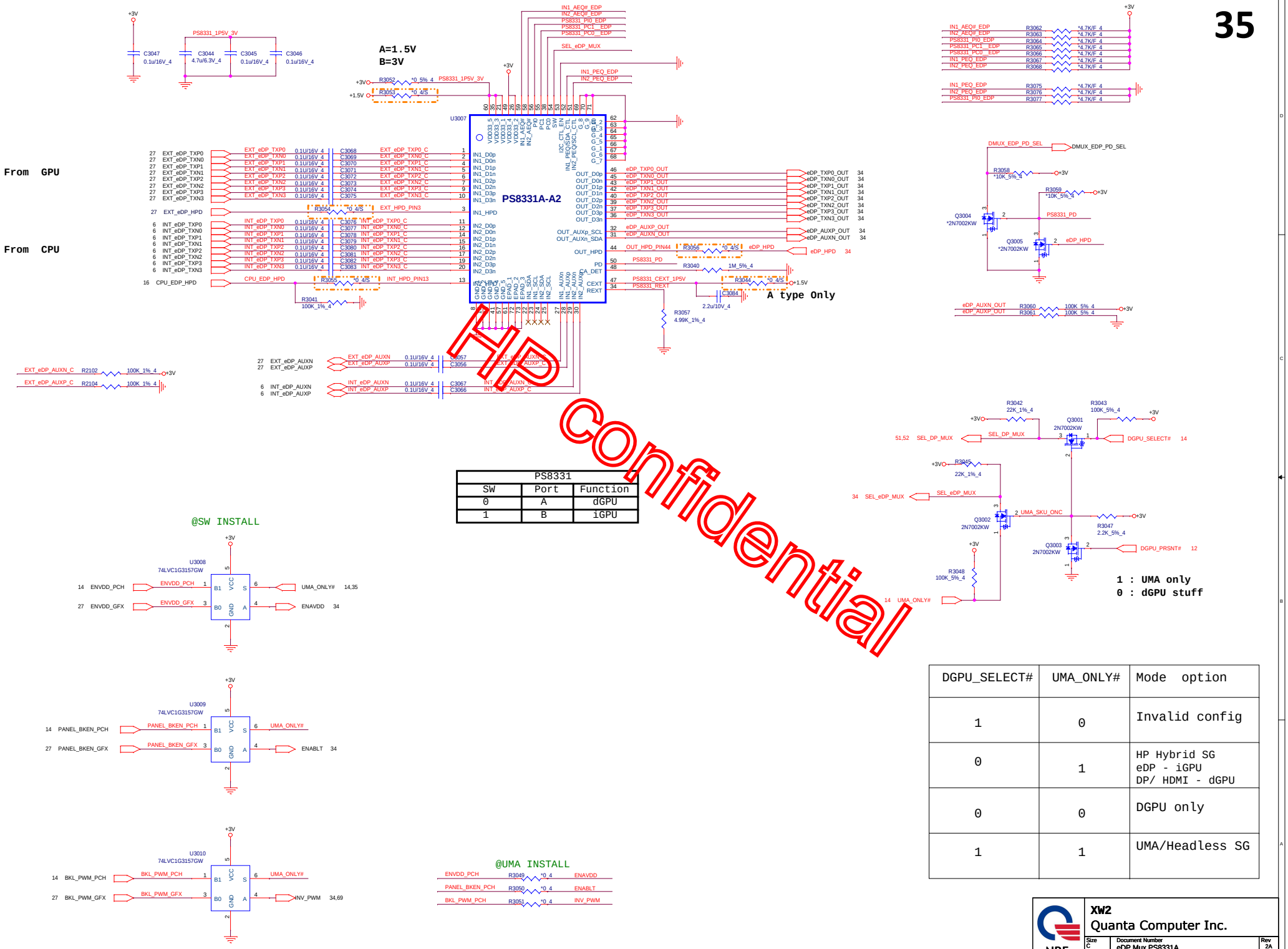

PS8331		
SW	Port	Function
0	A	dGPU
1	B	iGPU

DGPU_SELECT#	UMA_ONLY#	Mode option
1	0	Invalid config
0	1	HP Hybrid SG eDP - iGPU DP/ HDMI - dGPU
0	0	DGPU only
1	1	UMA/Headless SG

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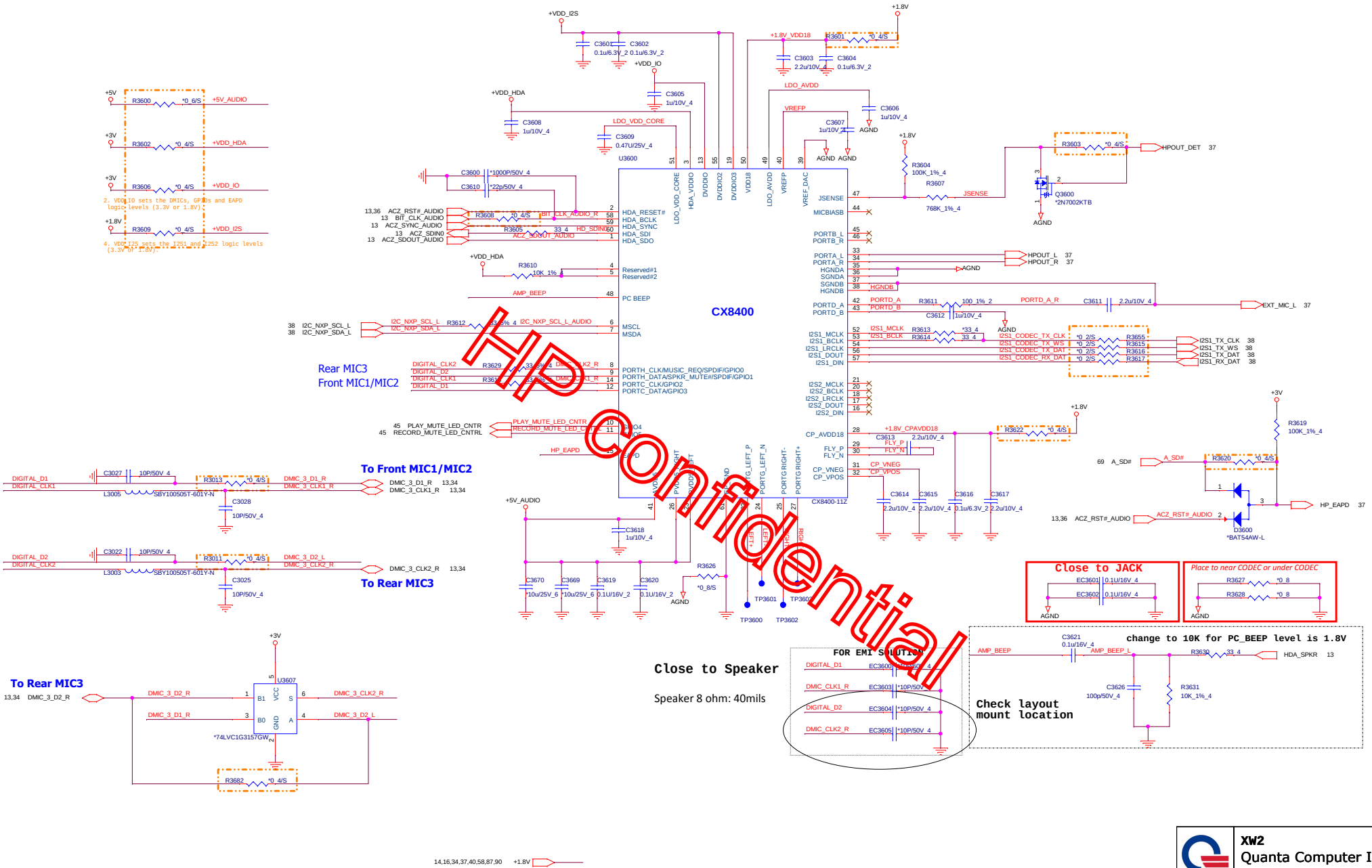
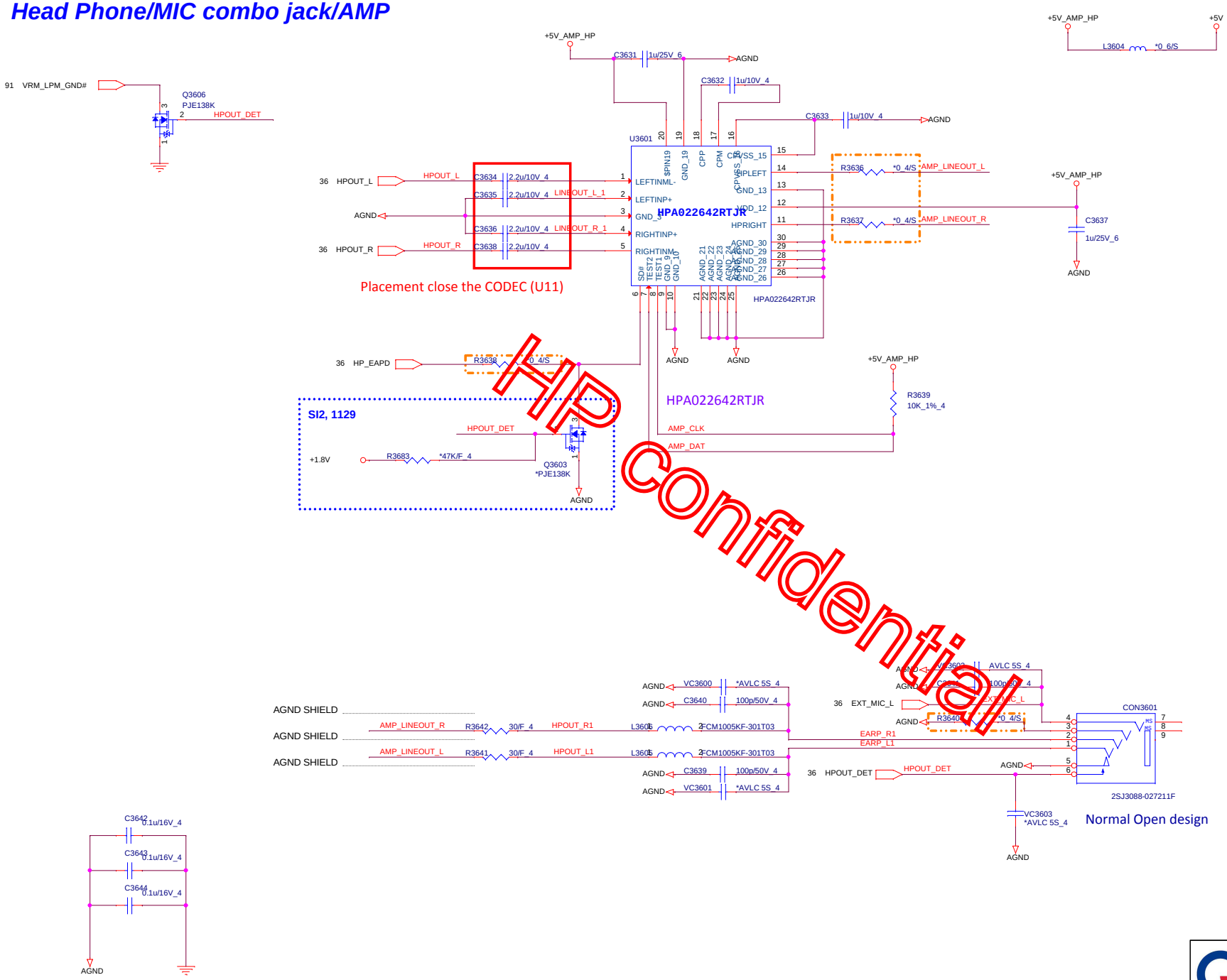
Audio Codec



Head Phone/MIC combo jack/AMP



NB5	XW2 Quanta Computer Inc.		
Size Custom	Document Number Combo jack Conn./AMP		Rev 2A
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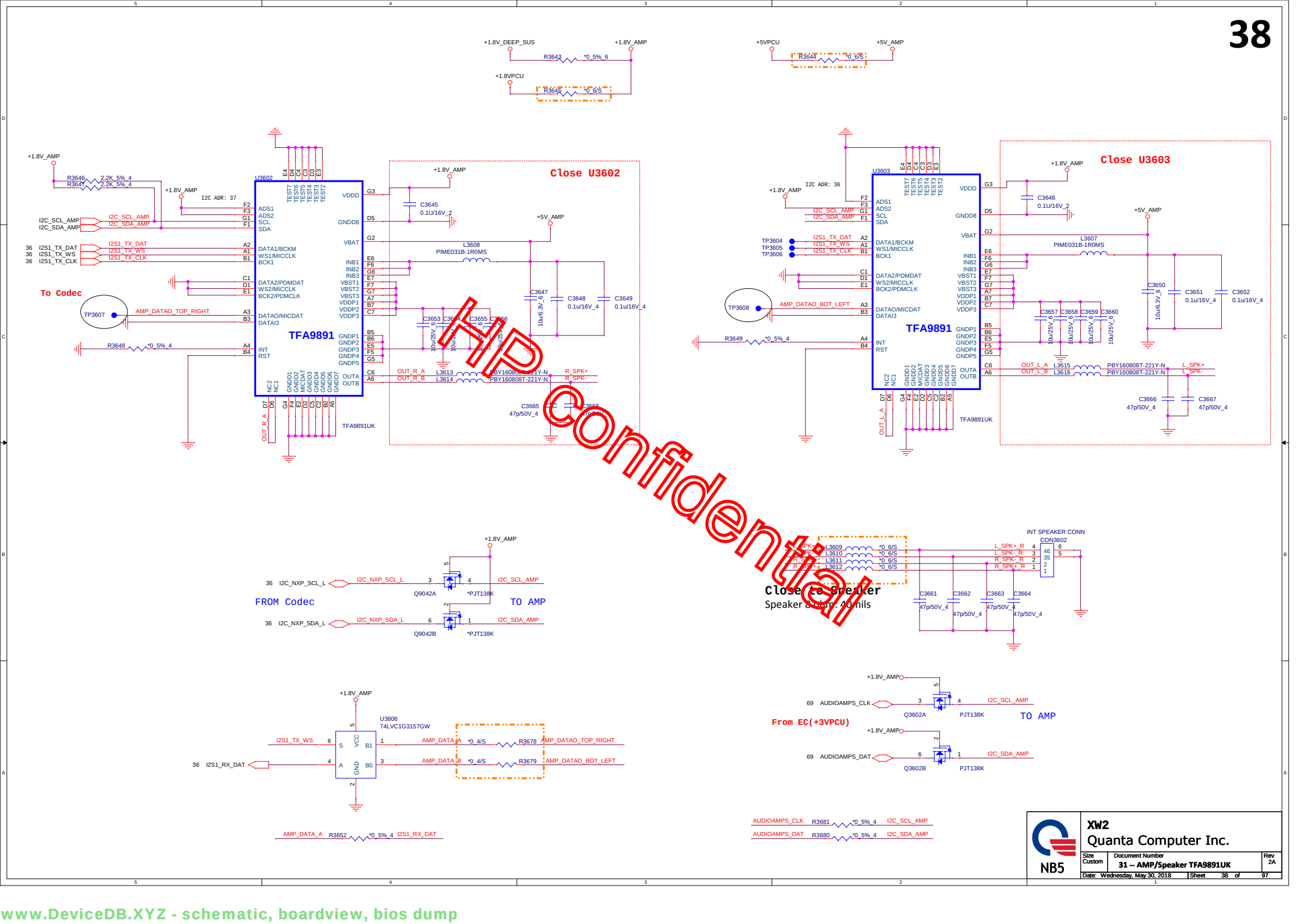

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NB5
Size: Custom | Document Number: 31 -- AMP/Speaker TFA9891UK | Rev: 2A
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HP has confirmed that MCU is only needed if there are 4 smart amps used.??
So please remove MCU from the schematic.

NB5

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Size	Document Number	Rev
Custom	NA	2A

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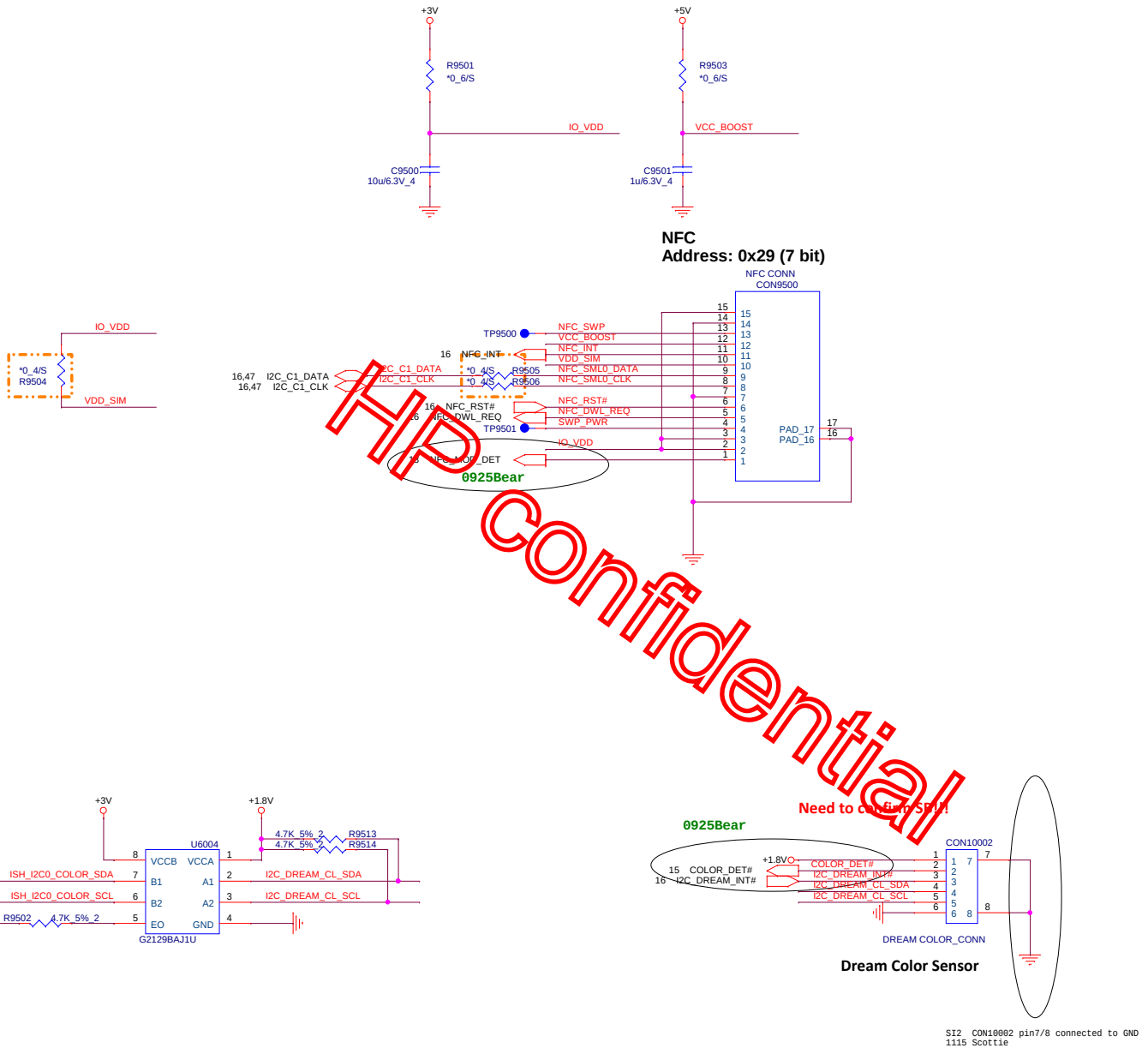

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Size	Document Number NFC / DREAM conn.	Rev 2A
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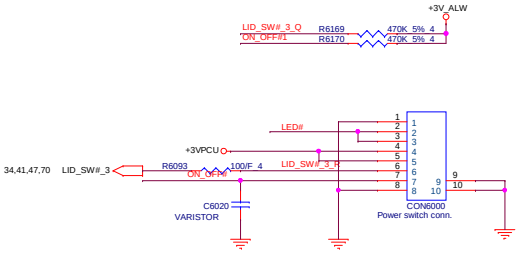
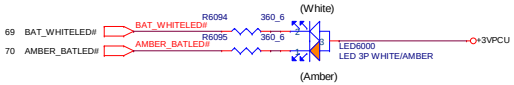
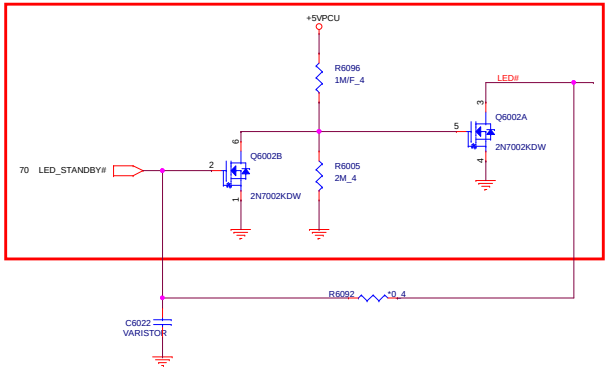
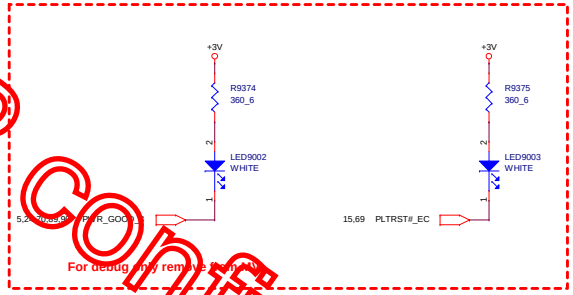


Battery LED

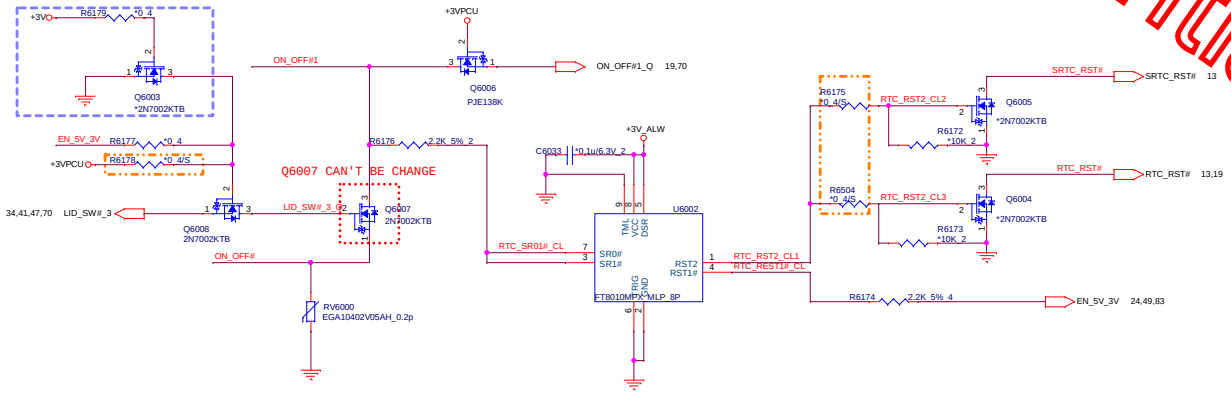


Dual LED control circuit





POWER BTN



NB5	XW2 Quanta Computer Inc.	
Size: Custom	Document Number: LED & Power Conn.	Rev: 2A
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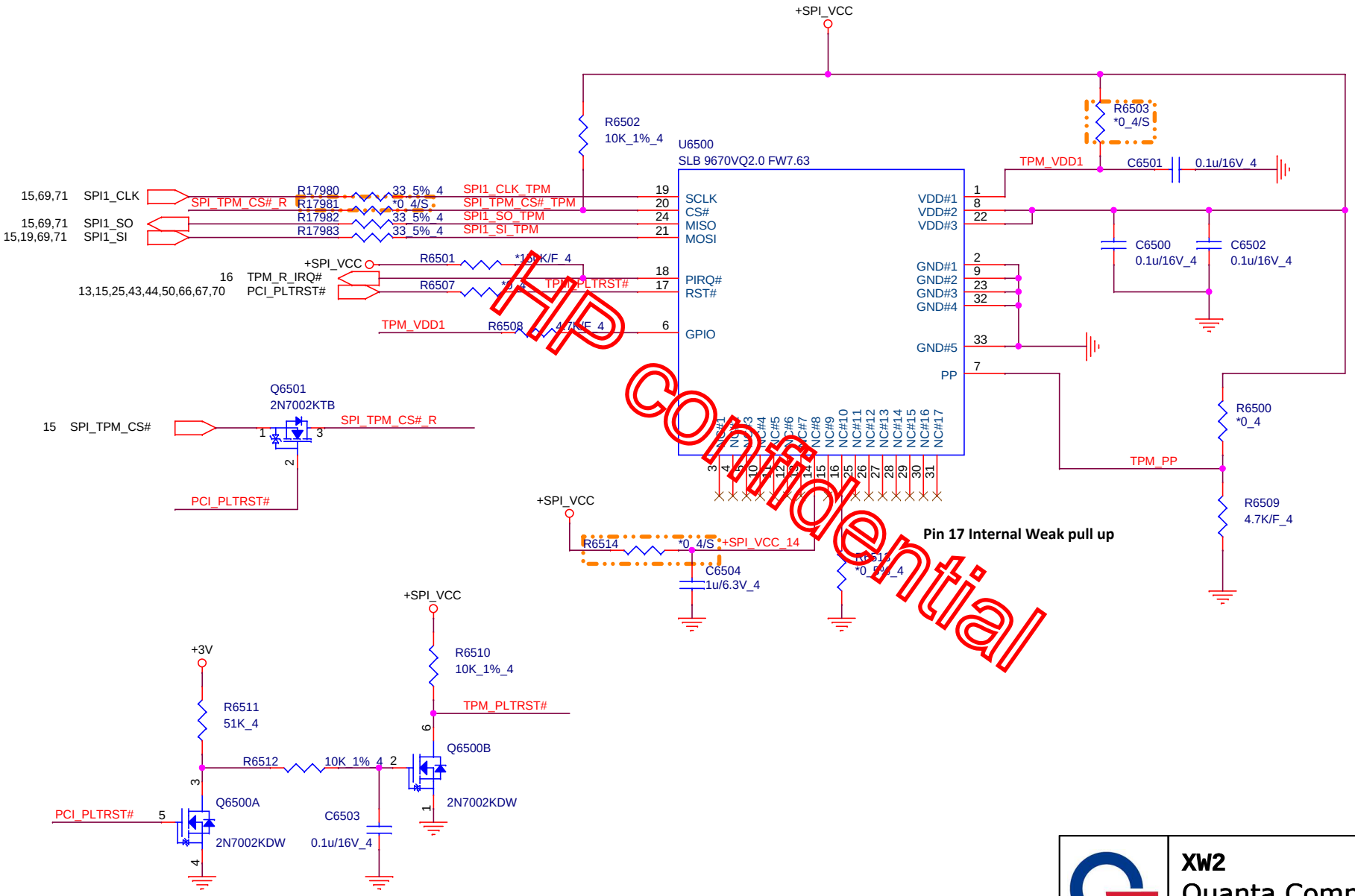
TPM 2.0



NB5	XW2 Quanta Computer Inc.	
Size Custom	Document Number TPM SLB9670_QFN	Rev 2A
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WIFI&BT

Max Load 2.5A for WLAN

SI2, 1124

SI2, 1129

If CNVi is present CNVi = Low, low switch will never turn off
If CNVi is not present CNVi = High, low switch EN pin will follow WLAN_DISABLE

PV, 0126

PV, 0123

0915Bear

0920Bear

0914Bear

0927Bear

Place close to WIFI module

Windstorm Peak & Jefferson Peak 2 M.2 1216 co-layout
Intel Dual Band Wireless-AC 8265
Intel Dual Band Wireless-AC 9560

XW2	Quanta Computer Inc.
NB5	Size C · Document Number WiFi +BT module · Rev 2A
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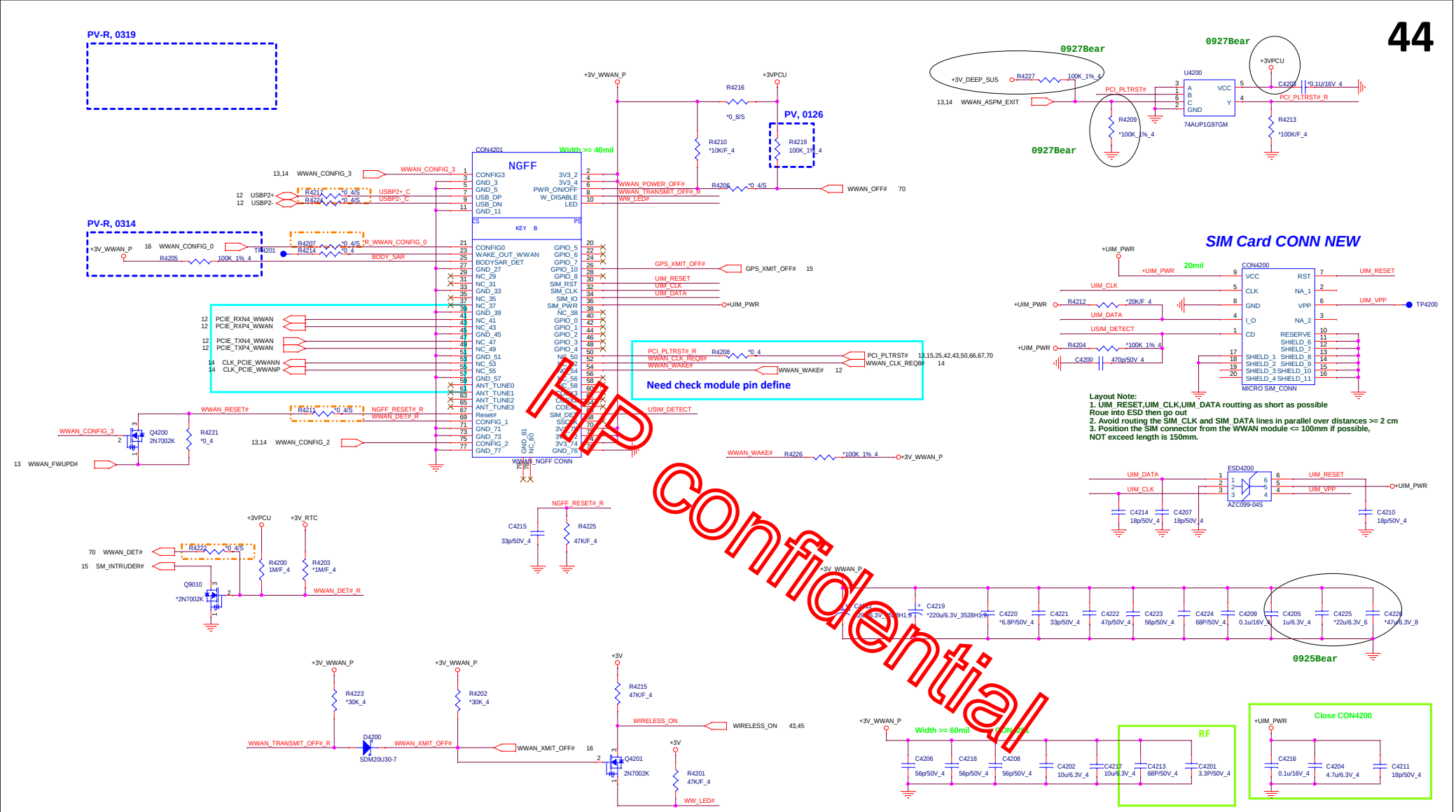


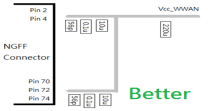
+VCC	Power_On/Off (Pin6)	W_Disable (Pin8)	GPS_Disable (Pin26)
S0 ON	High	High	High
S3 ON	High	Low	Low
S4 ON	Low	Low	Low
S5 ON	Low	Low	Low

Trace Length and Routing

- Special attention should be paid to SIM traces (UIM_CLK, UIM_DATA and UIM_RST) to minimize the trace lengths between the SIM slot and the WAN NGFF slot. **Minimizing the signal lengths and traces will reduce possibility of SIM signal integrity issues.** Recommended maximum length is 100mm. Not to exceed length is 150mm.
- Minimum distance between UIM_CLK and UIM_DATA should be 20 mils. Static signals such as UIM_RST can be routed between UIM_CLK and UIM_DATA to conserve space if needed.
- It is recommended that SIM traces be isolated from other high-speed switching signals, as noise can couple into the SIM signals. Keep a minimum distance of 20 mils between UIM_CLK, UIM_DATA and any other high-speed switching signals.
- Placing the SIM card on a daughter card is also not recommended as the interconnect may impact SIM signal integrity.

SIM Power

- The UIM_PWR trace width must be at least 20 mils. Sub-planar routing is recommended.
- Implement additional power filtering to SIM card power to ensure clean power is supplied to minimize any possible noise ripple effects. At a minimum, place a 0.1uF and a 4.7uF capacitor on the UIM_PWR supply and locate near the SIM connector.



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Quanta Computer Inc.
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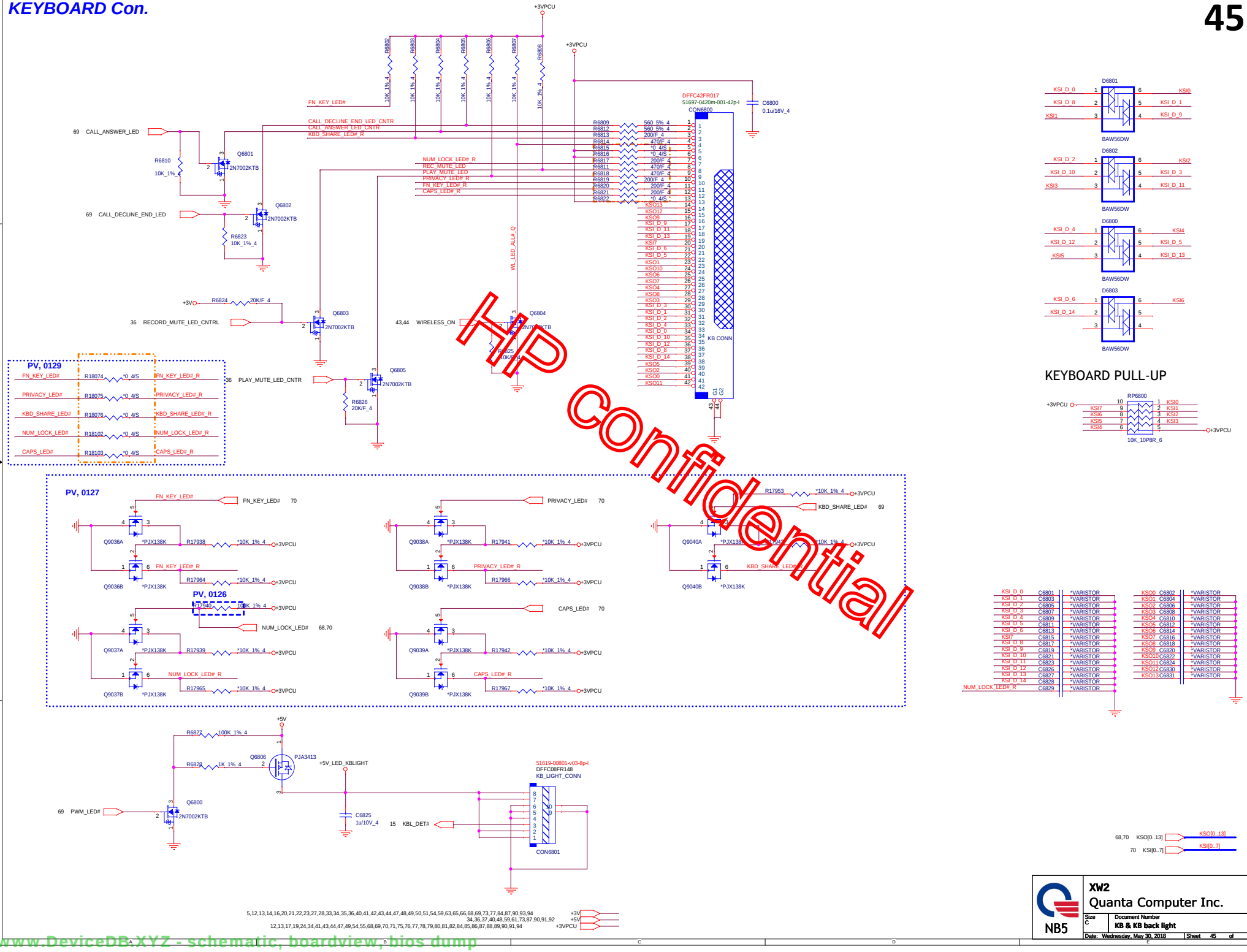
KEYBOARD Con.



KEYBOARD PULL-UP

68,70 KSO[0..13] KSO[0..13]
70 KSI[0..7] KSI[0..7]

NB5	XW2 Quanta Computer Inc.		
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NB5

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Quanta Computer Inc.

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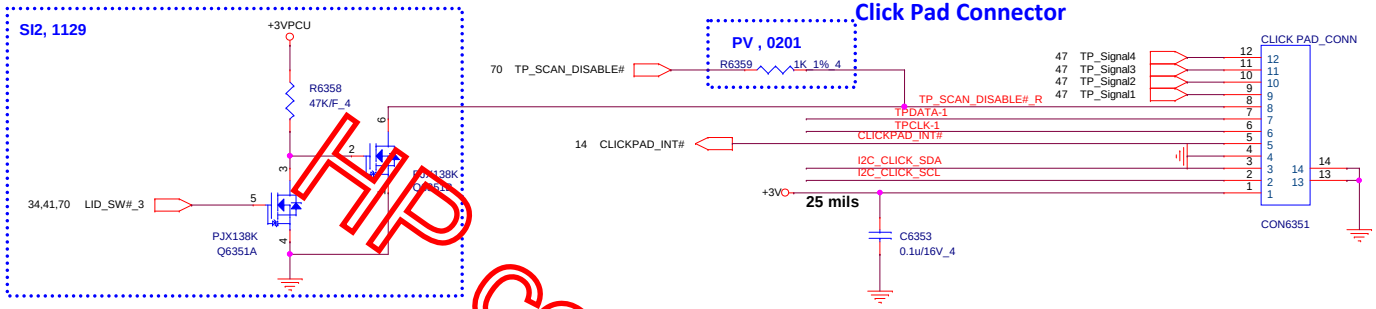
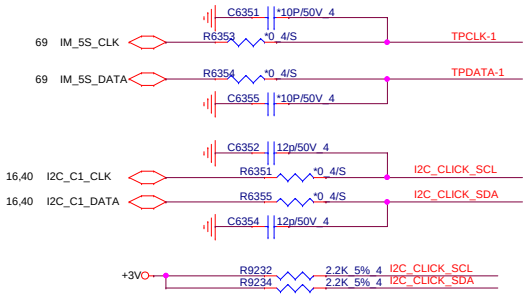


TP

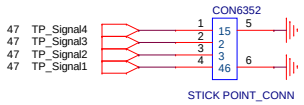
ピンアサイメント
PIN ASSIGNMENT

CN1

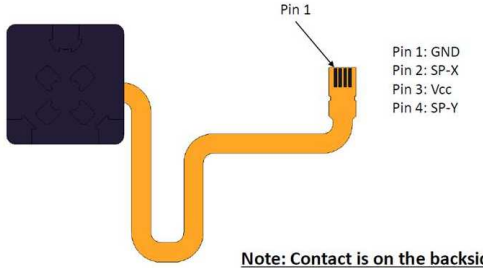
PIN NO.	SIGNAL
1	Vdd
2	SCL_I2C
3	SDA_I2C
4	GND
5	Int_I2C
6	CLK_PS2
7	DAT_PS2
8	TP_Disable#
9	PST signal1
10	PST signal2
11	PST signal3
12	PST signal4



CLICK PAD
Address: 0x2C(7 bit)



- View from the **backside**



Note: Contact is on the backside

5,12,13,14,16,20,21,22,23,27,28,33,34,35,36,40,41,42,43,44,45,48,49,50,51,54,59,63,65,66,68,69,73,77,84,87,90,93,94 +3V
14,16,34,36,37,40,58,87,90 +1.8V

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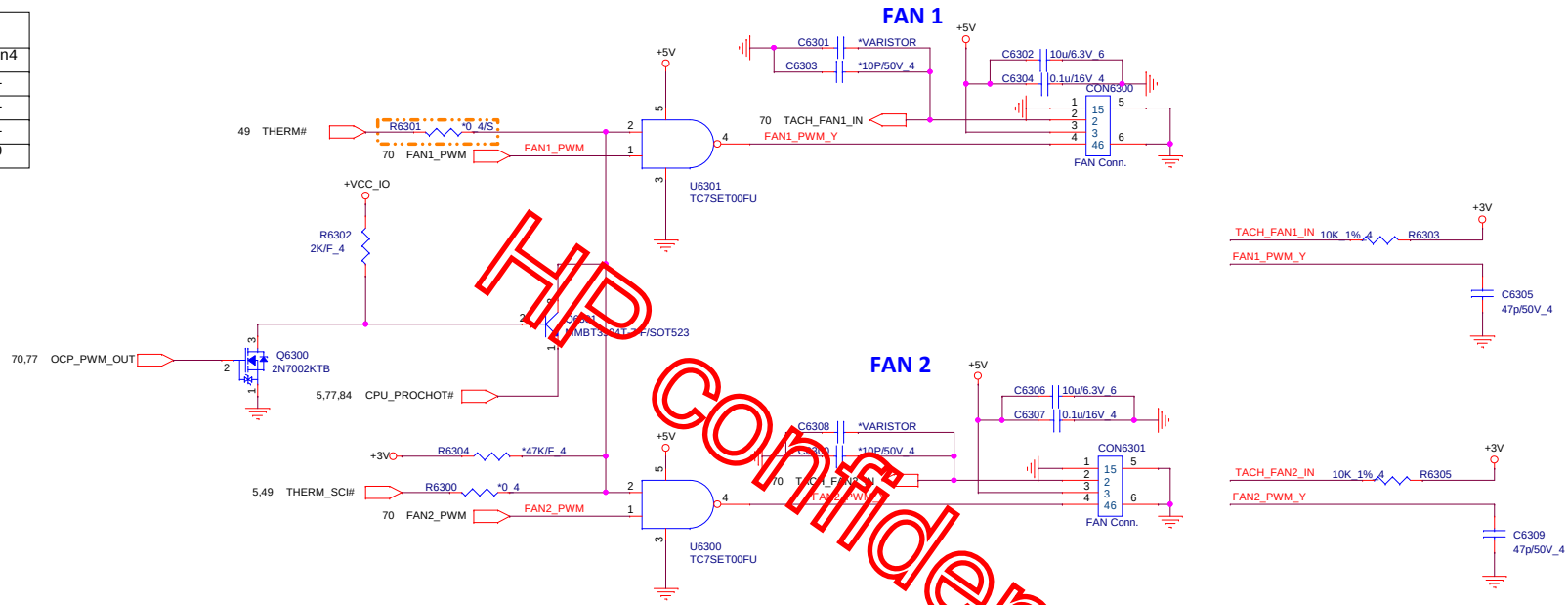
Truth table		
Pin1	Pin2	Pin4
0	0	1
0	1	1
1	0	1
1	1	0



5,12,13,14,16,20,21,22,23,27,28,33,34,35,36,40,41,42,43,44,45,47,49,50,51,54,59,63,65,66,68,69,73,77,84,87,90,93,94 +3V
34,36,37,40,45,59,61,73,87,90,91,92 +5V

NB5	XW2 Quanta Computer Inc.	
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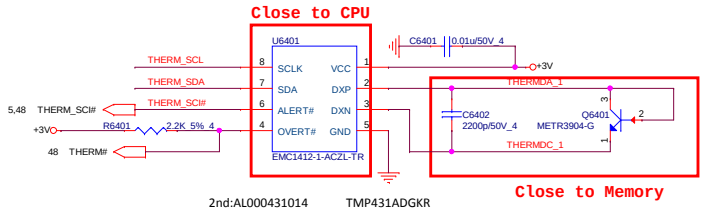
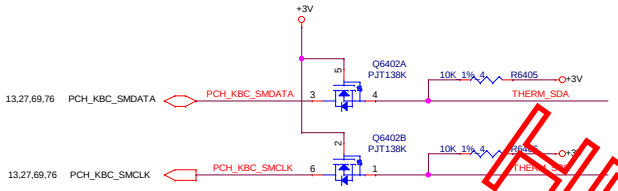
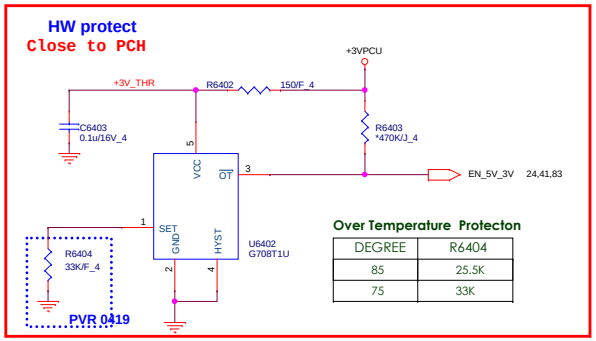


2nd:AL000431014 TMP431ADGKR
Main: AL000781012 G781P8(98h)

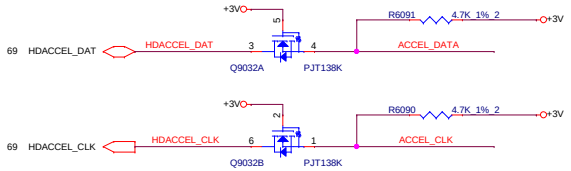


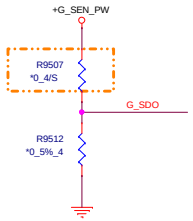


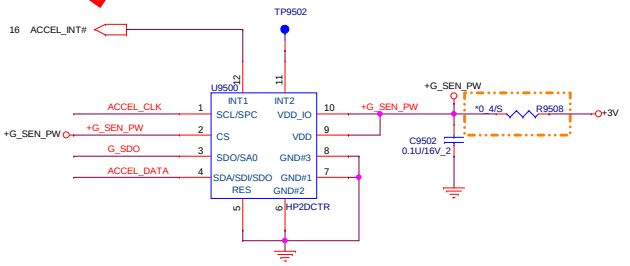
RSET (K OHM) = 0.0012T^2 - 0.9308T + 96.147

G-Sensor

copy from Bumblebee need check 5/10







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12,13,17,19,24,34,41,43,44,45,47,54,55,68,69,70,71,75,76,77,78,79,80,81,82,84,85,86,87,88,89,90,91,94
+3V
+3VPCU

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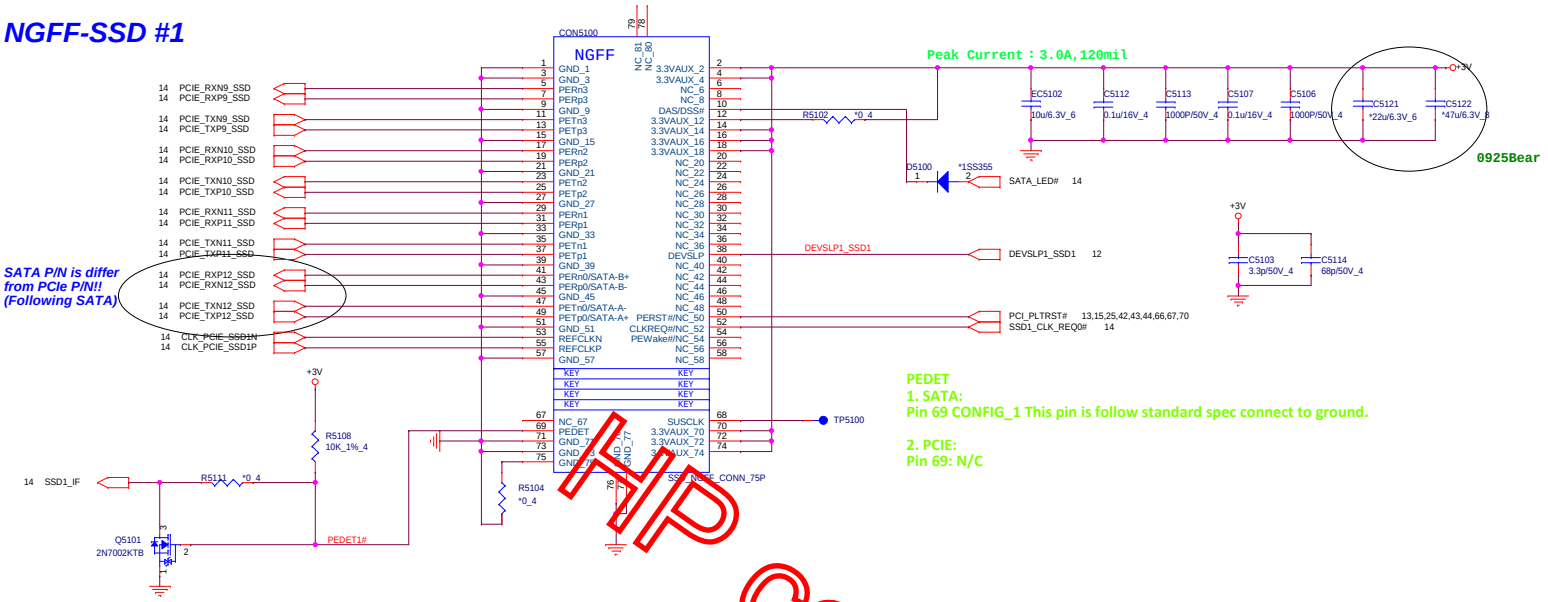
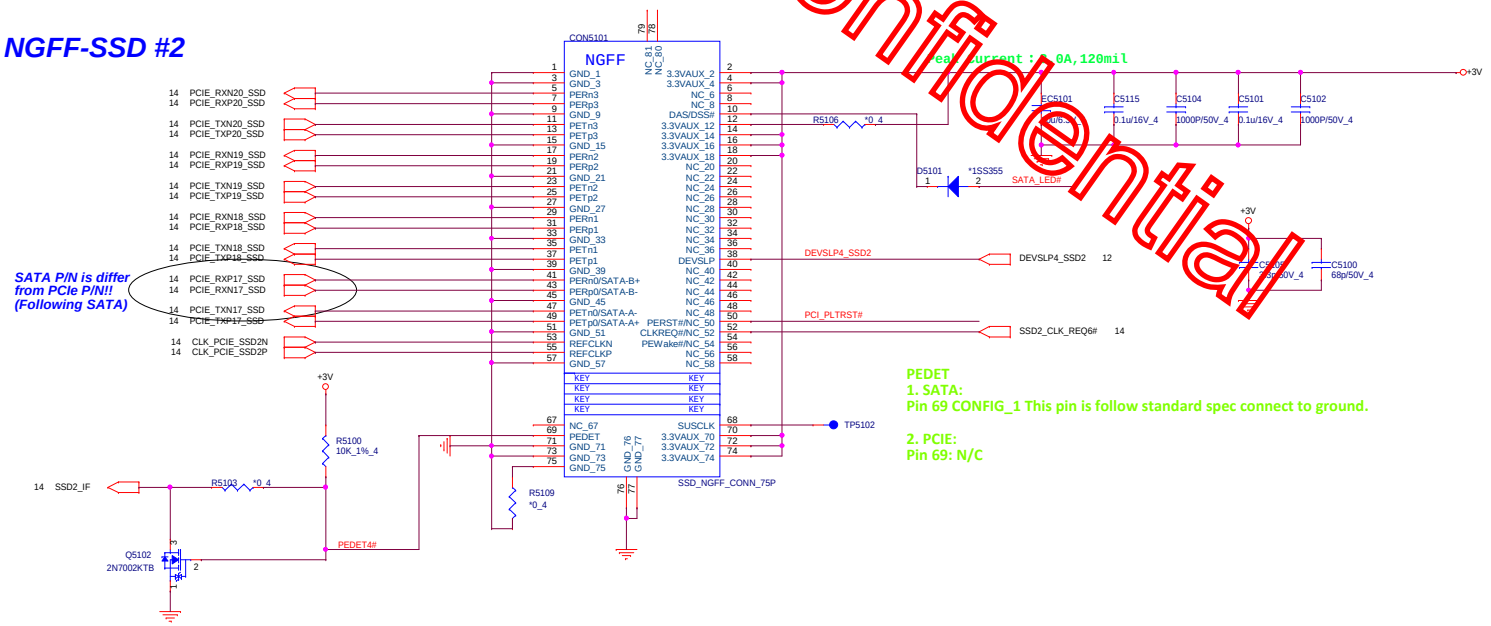
NGFF-SSD #1



PEDET
1. SATA:
Pin 69 CONFIG_1 This pin is follow standard spec connect to ground.

2. PCIE:
Pin 69: N/C

NGFF-SSD #2



PEDET
1. SATA:
Pin 69 CONFIG_1 This pin is follow standard spec connect to ground.

2. PCIE:
Pin 69: N/C

5,12,13,14,16,20,21,22,23,27,28,33,34,35,36,40,41,42,43,44,45,47,48,49,51,54,59,63,65,66,68,69,73,77,84,87,90,93,94 +3V

NB5	XW2 Quanta Computer Inc.	
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NB5	XW2 Quanta Computer Inc.	
Size	Document Number DP MUX PS8461(PortA)	Rev 2A
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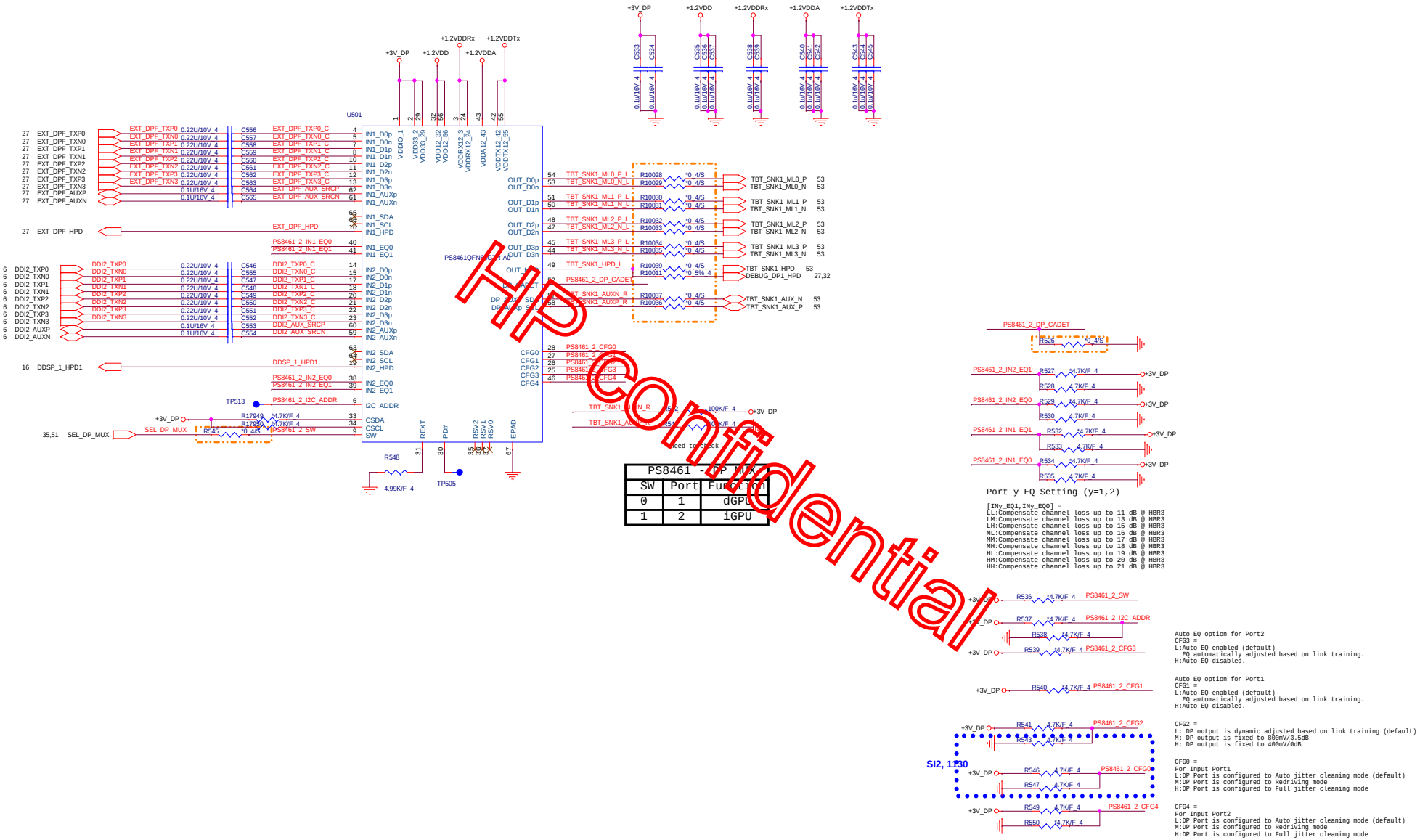
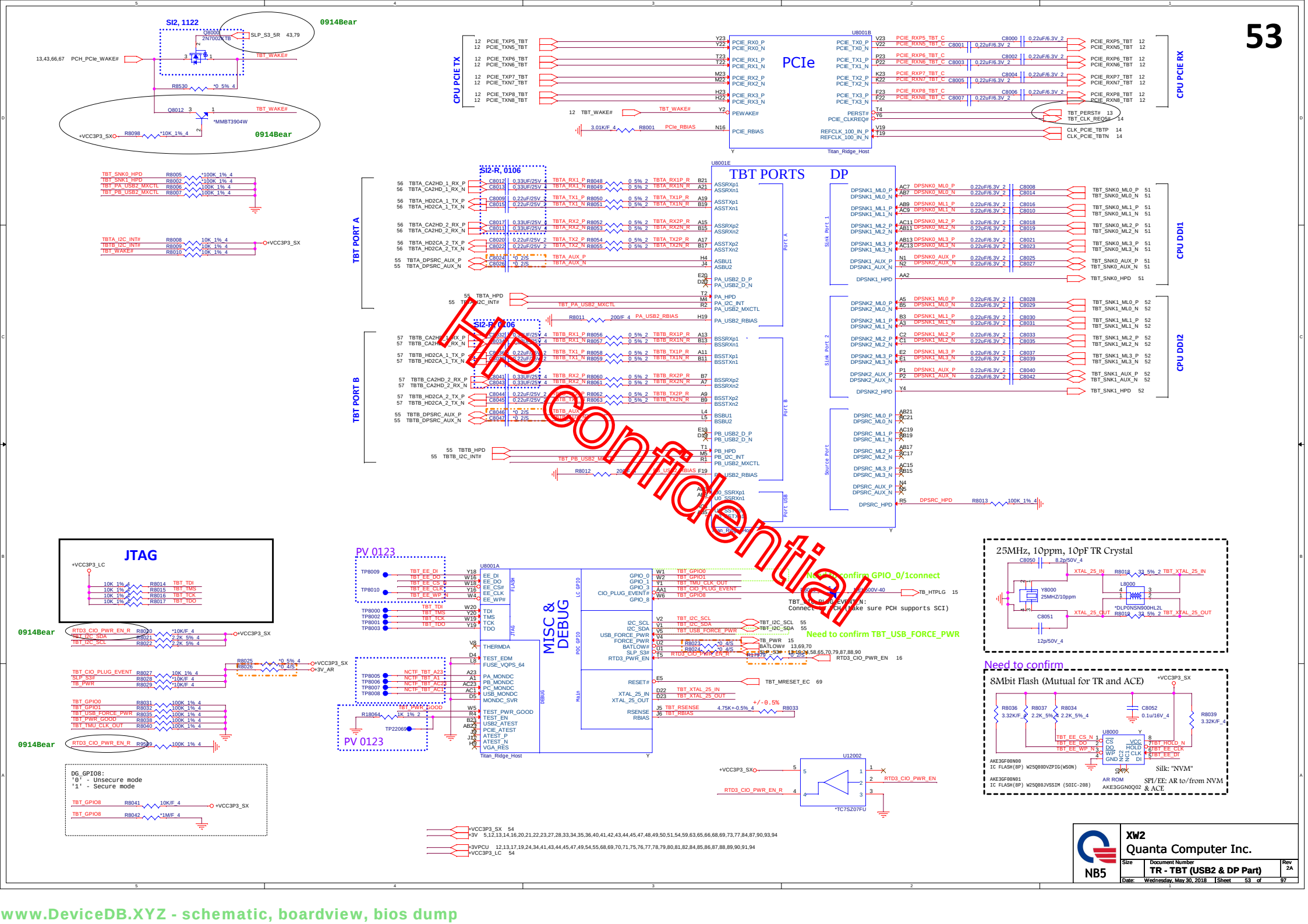


XW2	
Quanta Computer Inc.	
Size	Document Number: DP MUX PS8461(PortA)
Rev	2A
<Title>	
Date: Wednesday, May 30, 2018	Sheet 52 of 97
NB5	



XW2	
Quanta Computer Inc.	
NB5	
Size	Document Number: TR - TBT (USB2 & DP Part)
Rev	2A
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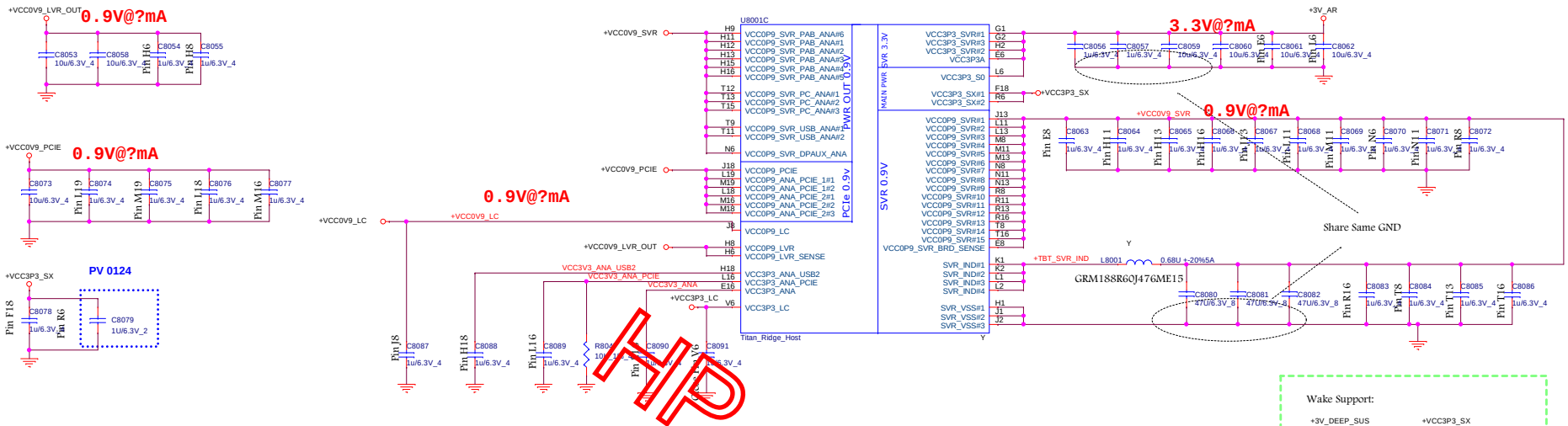
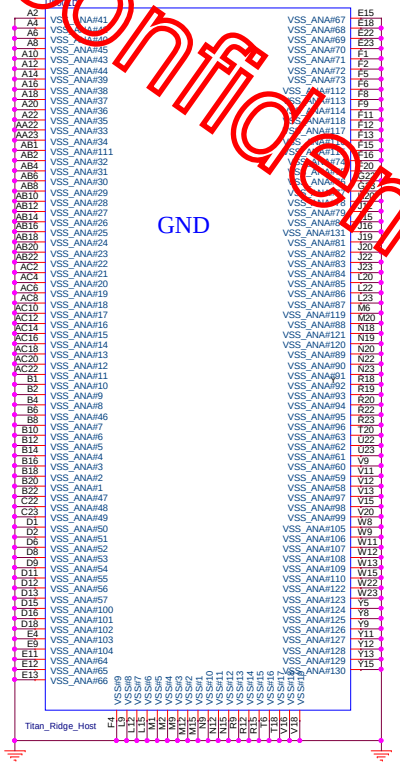
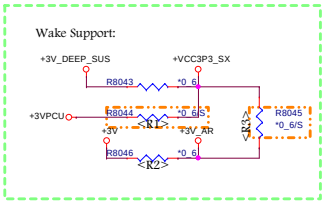


Titan Ridge DP - GND Symbol





Option 1 for wake support over TBT:
1. Connect 0Ohm to <R1> and <R3>. Keep <R2> empty.
2. Make sure VCC3v3_SX_SYS can support AR maximum power consumption.
3. Simple Bios implementation

No wake support at all from AR
1. Connect 0Ohm to <R2> and <R3>. Keep <R1> empty.

+VCC3P3_SX 53
+VCC3P3_LC 53
+3V 5,12,13,14,16,20,21,22,23,27,28,33,34,35,36,40,41,42,43,44,45,47,48,49,50,51,59,63,65,66,68,69,73,77,84,87,90,93,94
+3V_DEEP_SUS 5,12,13,14,15,16,17,19,24,43,44,68,71,76,82,87,89,90

NB5	XW2 Quanta Computer Inc.	
	Size Document Number TR - TBT (USB2 & DP Part)	Rev 2A
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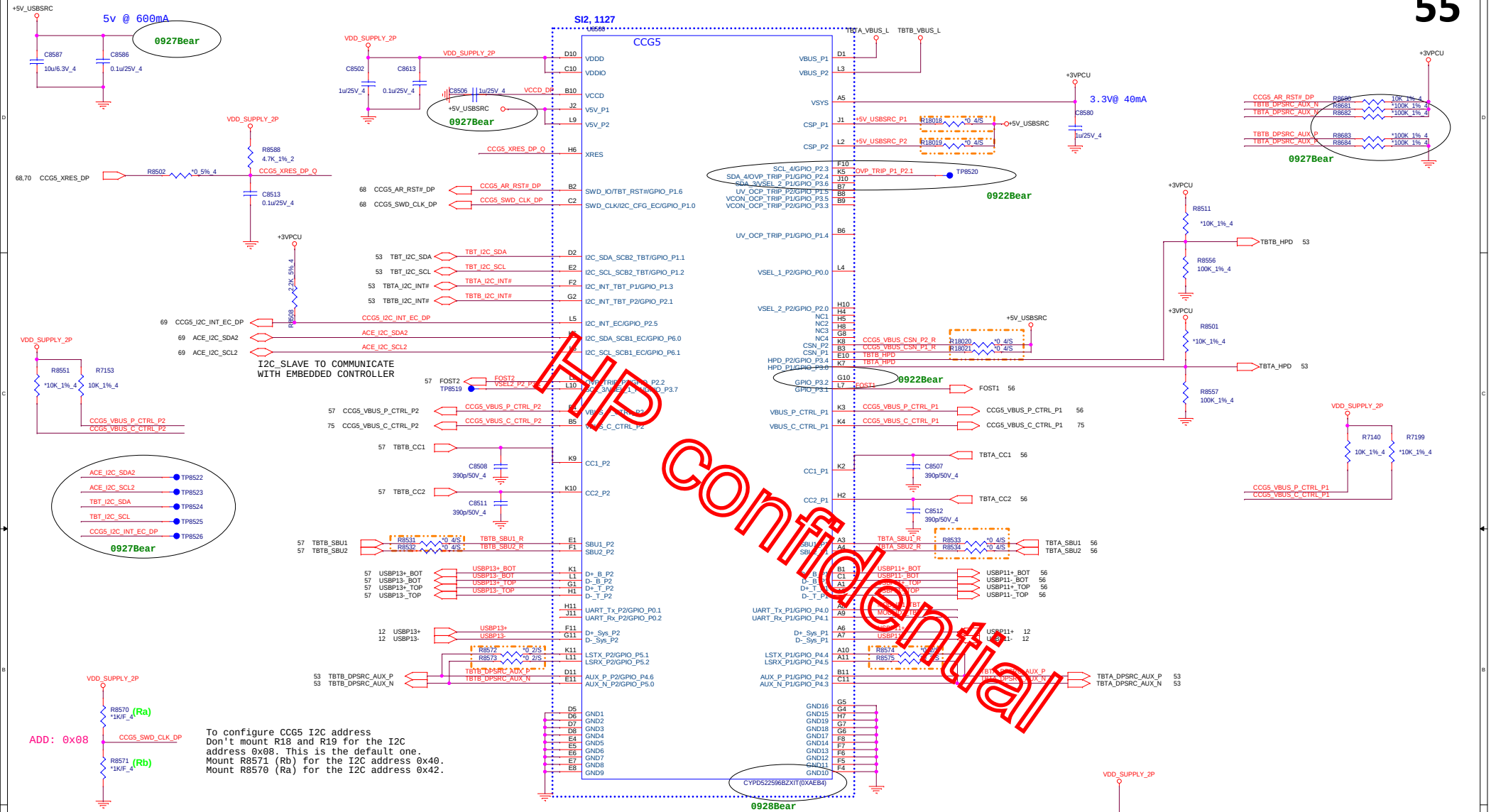

	Platform ID		CCG5 Dual Port
	MOD_ID1	MOD_ID2	Description (Dual port)
Notebooks	L7	L7	DRP+DP+ AR TBT on 2-ports
	L6	L7	DRP+DP on 2-ports
	L5	L7	DRP+DP on 2-ports with ANX MUX
	L4	L7	Malta
	L3	L7	DRP+DP+ TR TBT on 2-ports
	L2	L7	Reserved
	L1	L7	Reserved
	L0	L7	Reserved

L0 = 0V
L1 = VDDD/8
L2 = 2* VDDD/8
L3 = 3* VDDD/8
L4 = 4* VDDD/8
L5 = 5* VDDD/8
L6 = 6* VDDD/8
L7 = 7* VDDD/8
x = No Connect

MOD_ID	Pull high	Pull down
L0	None	10K
L1	71.5K	10K
L2	60.4K	22K
L3	49.9K	30K
L4	10K	10K
L5	30K	49.9K
L6	22K	60.4K
L7	10K	71.5K

XW2
Quanta Computer Inc.
NB5
Size C | Document Number CCG5 Connecton-A | Rev 2A
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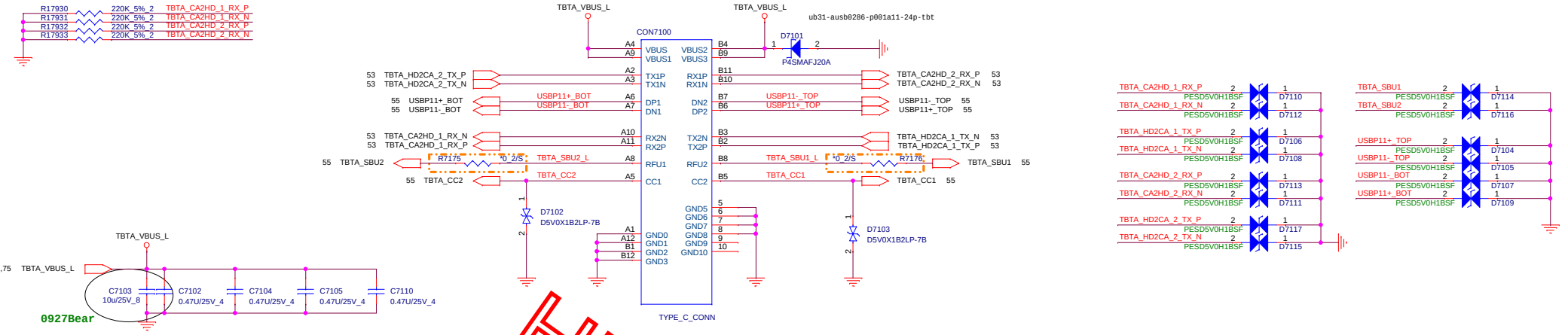
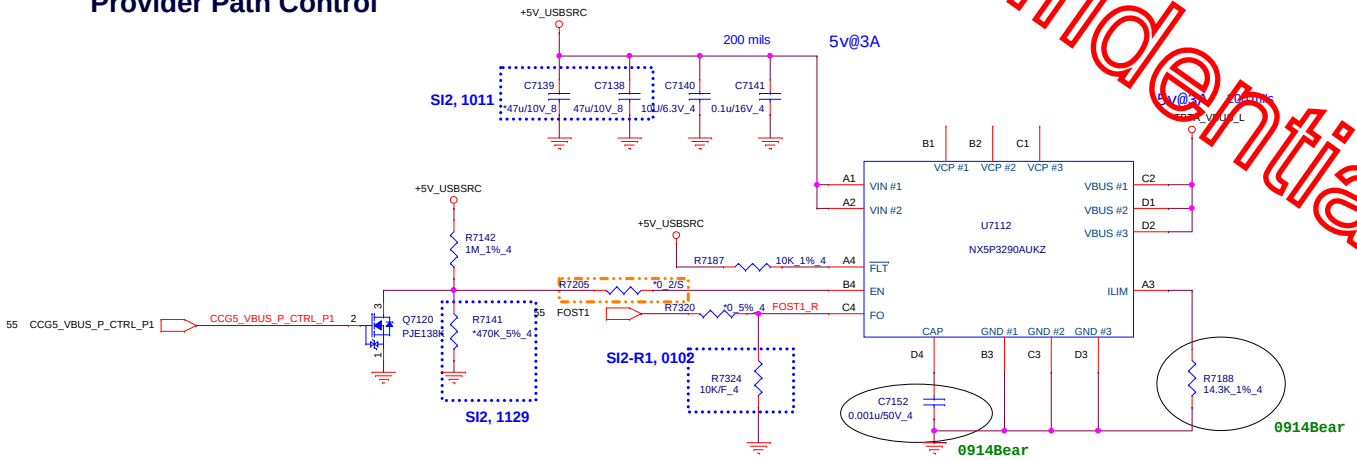
USB Type-C Port A

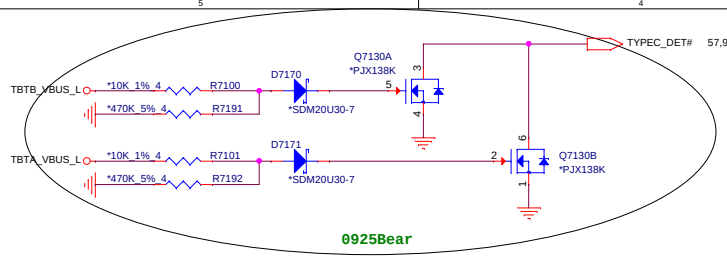


CCG5_VBUS_P_CTRL_P1= 0 (Provider Path ON)
CCG5_VBUS_P_CTRL_P1= 1 (Provider Path OFF)
ACTIVE LOW

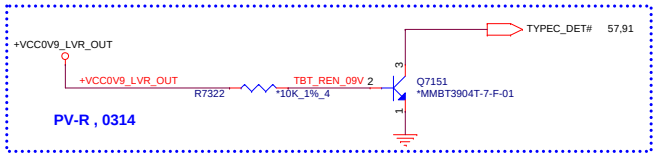
0914Bear

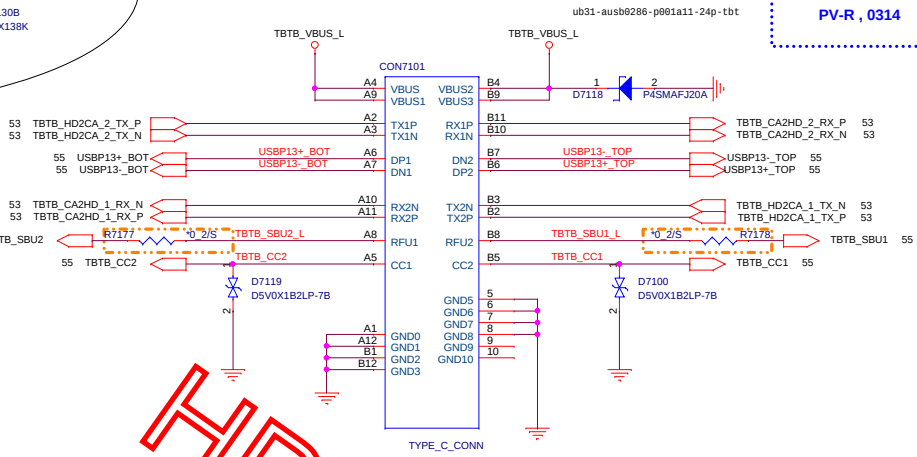
Provider Path Control

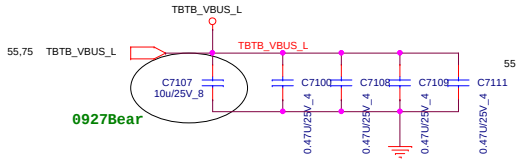


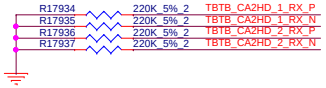


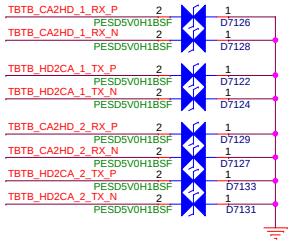
USB Type-C Port B

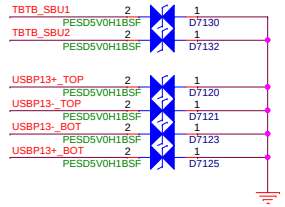








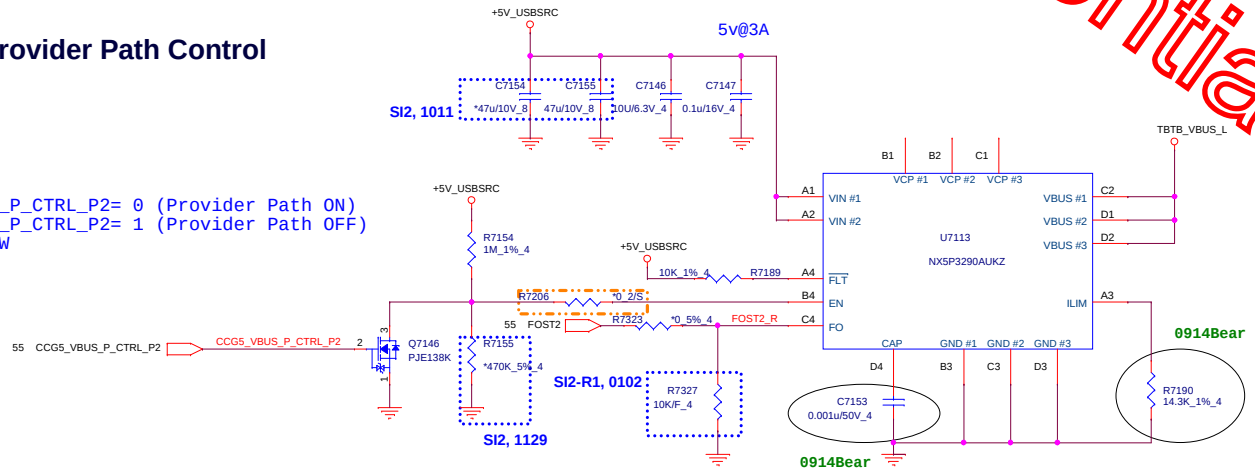




0914Bear

Provider Path Control

CCG5_VBUS_P_CTRL_P2= 0 (Provider Path ON)
CCG5_VBUS_P_CTRL_P2= 1 (Provider Path OFF)
ACTIVE LOW



NB5	XW2 Quanta Computer Inc.	
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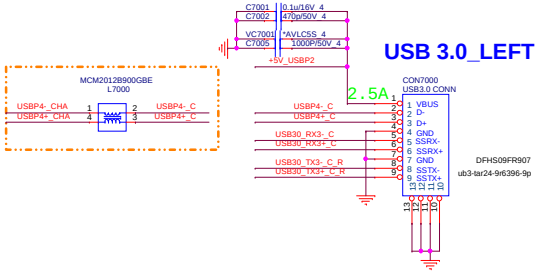
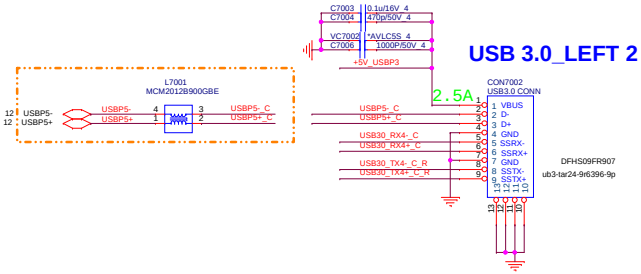
USB 2.0/3.0 Combo

USB 3.0_LEFT 1



USB 3.0_LEFT 2



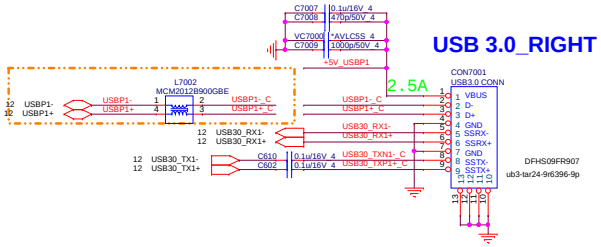
USB 3.0 ESD CHIP

P/N
BCSB3FR4Z00
BC001045Z02
BC000524Z01

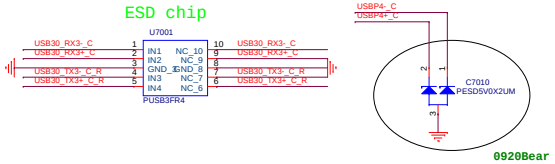
USB 2.0 ESD DIODE

P/N
BC5V0X2UZ00
BC005315Z00
BC10063LZ00

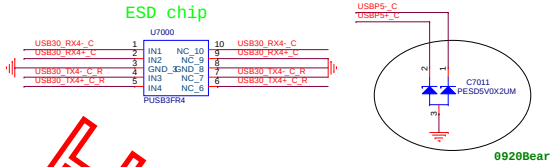
USB 3.0_RIGHT



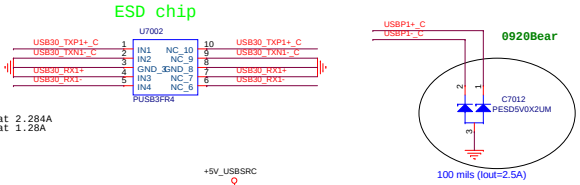
ESD chip



ESD chip



ESD chip

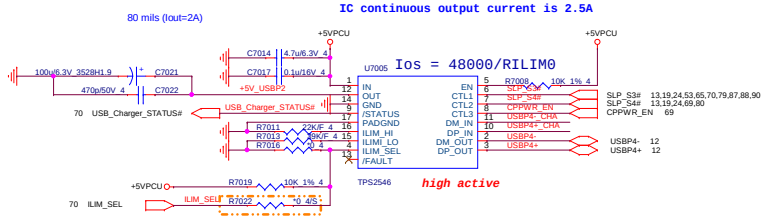


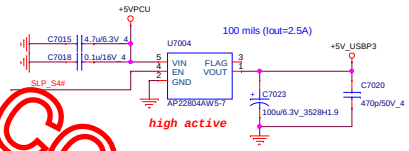
$$I_{OS\_typ}(mA) = \frac{50,250}{R_{ILIM\_XX}(k\Omega)}$$

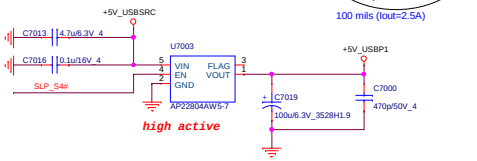
ILIM_HI = 22k, typical over current protection will be at 2.284A
ILIM_LO = 39k, typical over current protection will be at 1.28A

USB Charger

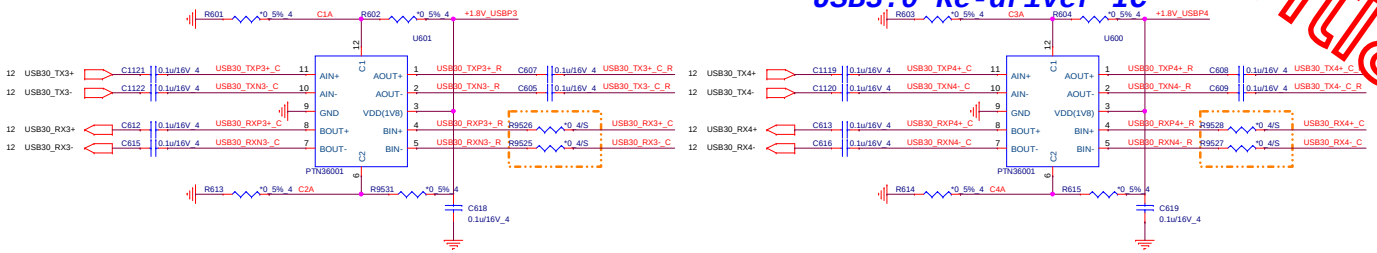
IC continuous output current is 2.5A

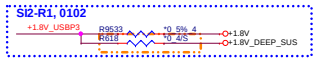


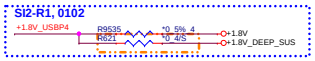




USB3.0 Re-driver IC







38,41,73,78,81,83,85,87,88,90,92,94,95 +5VPCU

Quanta Computer Inc.	XW2		
NB5	Size: Custom	Document Number: USB 3.0 & Re-Driver	Rev: 2A
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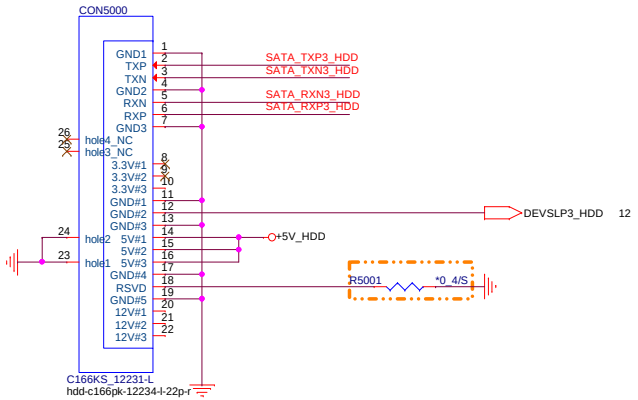
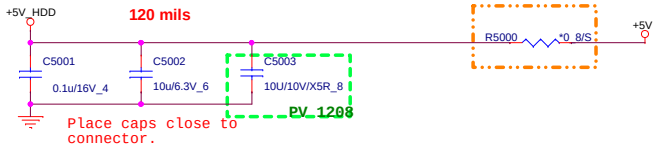
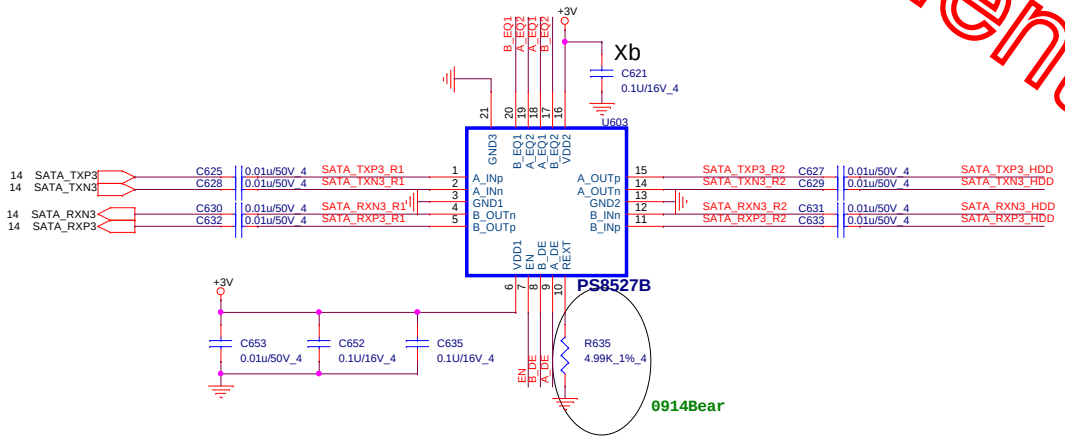
SATA-HDD



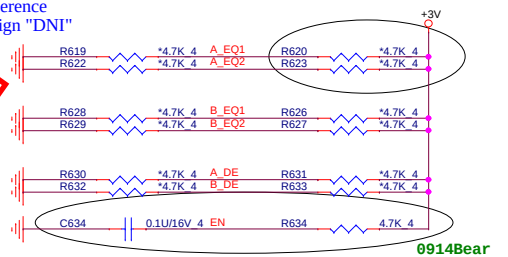




Equalization level setting for Channel x(x=A/B),internally tied to VDD/2 (default:12.2dB)
[x_EQ2, x_EQ1] ==
L/L: for channel loss up to 7.4dB
L/H: for channel loss up to 14.4dB
H/L: for channel loss up to 11.2dB
H/H: for channel loss up to 5dB

De-emphasis level setting for Channel x(x=A/B), internally tied to VDD/2(Default=-3.5dB)
[x_DE] ==
L: 0 dB
H: -6dB

Reference design "DNI"



NB5	XW2 Quanta Computer Inc.	
Size: Custom	Document Number: HDD & Re-Driver	Rev: 2A
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NB5

XW2

Quanta Computer Inc.

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<Title>	ODD	2A

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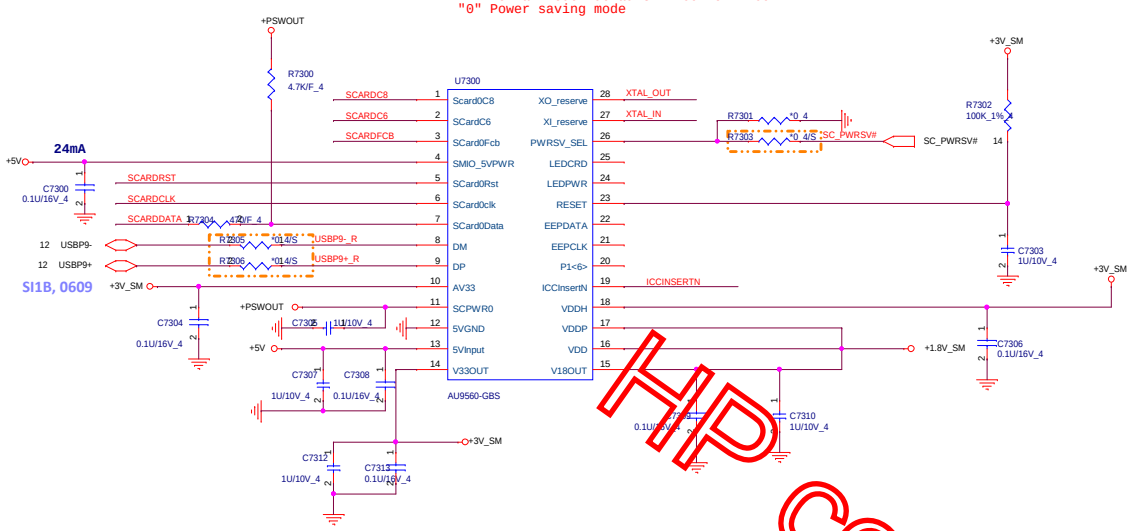
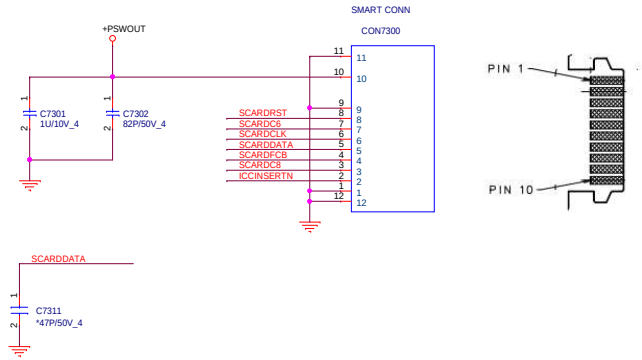
copy from BELLAGIO need check 5/10

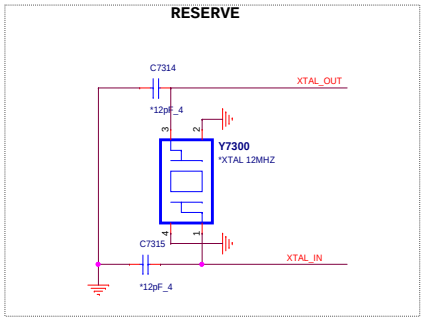
PWRSV_SEL
"1" Normal mode <default> 24C02 or 24C04
"0" Power saving mode





PIN NO.	ASSIGNMENT	PIN NO.	ASSIGNMENT
PIN 1 (C1)	VCC (Supply voltage)	PIN 2 (C5)	GND (Ground)
PIN 3 (C2)	RST (Reset signal)	PIN 4 (C6)	VPP (Programming Voltage)
PIN 5 (C3)	CLK (Clock signal)	PIN 6 (C7)	I/O (Data input/output)
PIN 7 (C4)	RESERVED TO ISO/IEC JTC 1 / SC 17 FOR FUTURE USE	PIN 8 (C8)	RESERVED TO ISO/IEC JTC 1 / SC 17 FOR FUTURE USE
PIN 9	SC_DET2	PIN 10	SC_DET1

RESERVE



XW2
Quanta Computer Inc.
NB5
Size
Document Number
Smart Card
Rev
2A
<Title>
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NB5

XW2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CFexpress Card	2A

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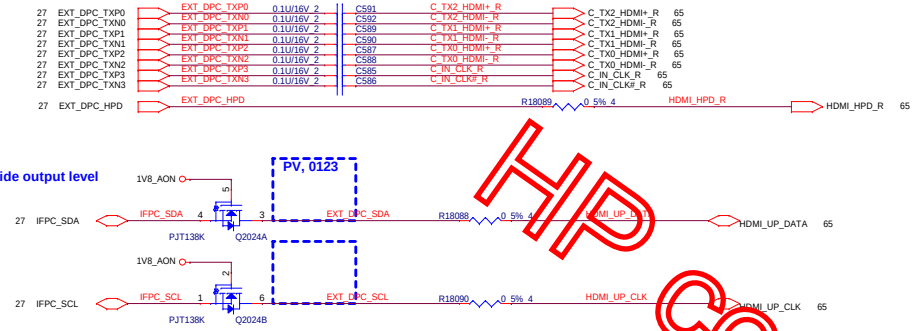
PV, 0126 , delete MUX , change to HW option

Mount these parts for HDMI , GPU sku only

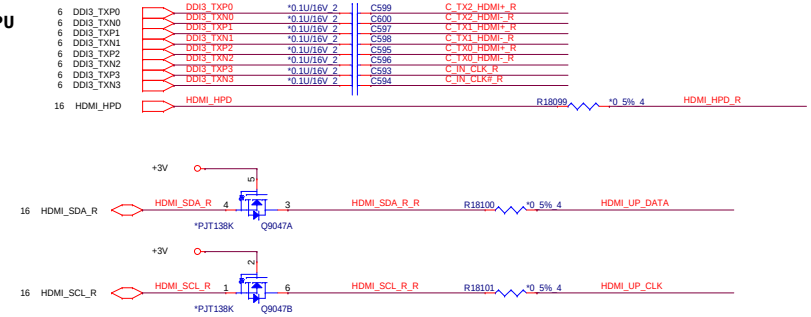
From GFX



Notice: check GPU side output level

Mount these parts for HDMI , UMA only

From CPU



NB5	XW2 Quanta Computer Inc.		
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NB5

XW2
Quanta Computer Inc.

Size	Document Number	Rev
<Title>	De-Mux PS8469	2A

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HDMI

+5V_HDMIC
C3205
*0.01U/50V_4
for EMI request

PV, 0123
EMI Solution
C_TX2_HDMI+_R_R R3204 *120_2 C_TX2_HDMI+_R
C_TX1_HDMI+_R_R R3205 *120_2 C_TX1_HDMI+_R
C_TX0_HDMI+_R_R R3206 *120_2 C_TX0_HDMI+_R
C_IN_CLK_R_R R3207 *120_2 C_IN_CLK#_R_R

PV 0127 delete
ESD chip, reserve

PV 0127 delete
ESD chip, reserve

+5V_USBSRC
C3201 1u/6.3V_4
R3201 *100K/F_4
13,19,24,53,58,70,79,87,88,90
SLP_S3#
R3202 *100K/F_4
U3201
VIN VOUT
OC# GND
EN
G524B1T11U
for eDP,stuff U2 & L8
for LVDS,stuff C29 & R23
+5V_HDMIC
C3202 0.01u/50V_4
C3203 0.1u/16V_4
C3204 10u/6.3V_4

CON3200
X_DP(PWR)
D2+
GND_2
D2-
D1+
GND_5
D1-
D0+ SHELL1
GND_8
D0-
CK+
GND_11
CK- SHELL2
CE Remote
NC
DDC CLK
DDC DATA
GND_DPAUX
+5V
HP DET
HD_DP_Option
HDMI CONN
C_TX2_HDMI+_R_R
C_TX2_HDMI-_R_R
C_TX1_HDMI+_R_R
C_TX1_HDMI-_R_R
C_TX0_HDMI+_R_R
C_TX0_HDMI-_R_R
C_IN_CLK_R_R
C_IN_CLK#_R_R
PVR 0329: RES value TBD
+5V_HDMIC
R3200 3.3K/F_4
R3203 3.3K/F_4
63 HDMI_UP_CLK
63 HDMI_UP_DATA
HDMI_UP_CLK
HDMI_UP_DATA
PV 0127 delete
+5V_HDMIC
PS8409_HDMI_HPD_R
VC3200 *TVM0G5R5M220R
C3207 220p/50V_4

HDMI Repeater

+3V
R18067 *0_4/S
+3V_8409
C12049 4.7u/6.3V_4
C12047 0.1u/16V_4
C12048 0.1u/16V_4
C12046 0.01u/50V_4
C12045 0.01u/50V_4

+1.2V
R18077 *0_4/S
+1.2V_8409

+1.2V_8409
C12054 4.7u/6.3V_4
C12051 0.1u/16V_4
C12052 0.1u/16V_4
C12055 0.01u/50V_4
close to U12006 PIN 43,46
VDDRX12: power ripple < 30mV

+1.2V_8409
C12058 0.1u/16V_4
C12057 0.1u/16V_4
C12060 0.01u/50V_4
close to U12006 PIN 6 & 11

+1.2V_8409
C12061 0.1u/16V_4
C12062 0.1u/16V_4
C12063 0.01u/50V_4
close to U12006 PIN 15 & 18

+1.2V_8409
C12065 0.1u/16V_4
C12066 0.01u/50V_4
close to U12006 PIN 29

+1.2V_8409
R18078 4.99K_1%_4
U12006
PS8409AQFN48GTR2-A2
REXT RESETB SCL_SRC/AUXP SDA_SRC/AUXN I2C_ADDR VDD12_2 CSCL CSDA PRE RSV2 NC
POWERSW IN_D2P IN_D2N HPD_SRC IN_D1P IN_D1N VDDRX12_1 IN_D0P IN_D0N VDDRX12_2 IN_CKP IN_CKN GND
VDD33_2 OUT_D2P OUT_D2N HPD_SNK OUT_D1P OUT_D1N VDDTX12_2 OUT_D0P OUT_D0N VDDTX12_1 OUT_CKP OUT_CKN
VDD33_1 TESTMODE DCIN_ENB PDB EQ_1 VDD12_1 SCL_SNK SDA_SNK SMA_CEC RSV1 VDDA12 CEC_EN
PS8409_RST# PS8409_HDMI_ID PS8409_I2C_ADDR PS8409_PRE
C12044 0.1u/16V_4
C12043 0.01u/50V_4
+3V_8409
C_TX2_HDMI+_R_R
C_TX2_HDMI-_R_R
PS8409_HDMI_HPD_R
C_TX1_HDMI+_R_R
C_TX1_HDMI-_R_R
C_TX0_HDMI+_R_R
C_TX0_HDMI-_R_R
C_IN_CLK_R_R
C_IN_CLK#_R_R
63 C_TX2_HDMI+_R
63 C_TX2_HDMI-_R
63 HDMI_HPD_R
63 C_TX1_HDMI+_R
63 C_TX1_HDMI-_R
63 C_TX0_HDMI+_R
63 C_TX0_HDMI-_R
63 C_IN_CLK_R
63 C_IN_CLK#_R
+1.2V_8409
C12056 0.1u/16V_4
+3V_8409
PS8409_DCIN_ENB
PS8409_EQ
HDMI_UP_CLK
HDMI_UP_DATA
+1.2V_8409
+1.2V_8409

+3V_8409
PS8409_I2C_ADDR R18072 *4.7K/F_4
PS8409_HDMI_ID R18073 *4.7K/F_4
PS8409_EQ R18069 *4.7K/F_4
R18070 *4.7K/F_4

I2C slave address selecion:
Internal pull down , 3.3V I/O
L:Default slave address: 0 X 10 - 0 X 2F
H:Alternative slave address: 0 X 90 - 0 X 9F , 0 X D0 - 0 X DF

HDMI_ID enable:
Internal pull down , 3.3V I/O.
L: Default, HDMI ID enable
H: HDMI ID disable

Receiver EQ setting: internal pull up 3.3V I/O
L: compensation for channel loss up to 13dB
H: default, compensation for channel loss up to 17dB
M: compensation for channel loss up to 11dB

PS8409_PRE R18071 *4.7K/F_4
PS8409_DCIN_ENB R18068 4.7K/F_4

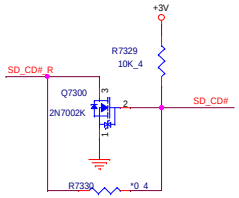
Output pre-emphasis setting: internal pull up 3.3V I/O
L: pre-emphasis = 2.5dB
H: default , no pre-emphasis

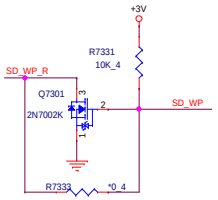
DC coupling enable: internal pull up 3.3V I/O
L: DC coupling input
H: default , AC coupling input

+3V_8409
PS8409_RST# R18079 10K_1%_4
C12064 1u/6.3V_4

XW2
Quanta Computer Inc.
NB5
Size: Custom
Document Number: HDMI repeater / CONN
Rev: 2A
Date: Wednesday, May 30, 2018
Sheet 65 of 97

CardReader - RTS5258S

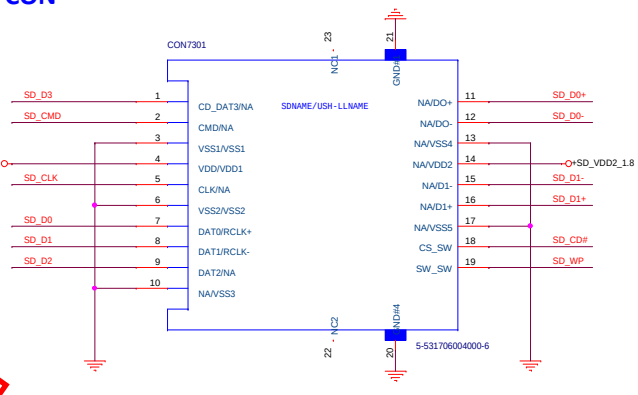


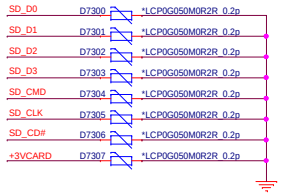


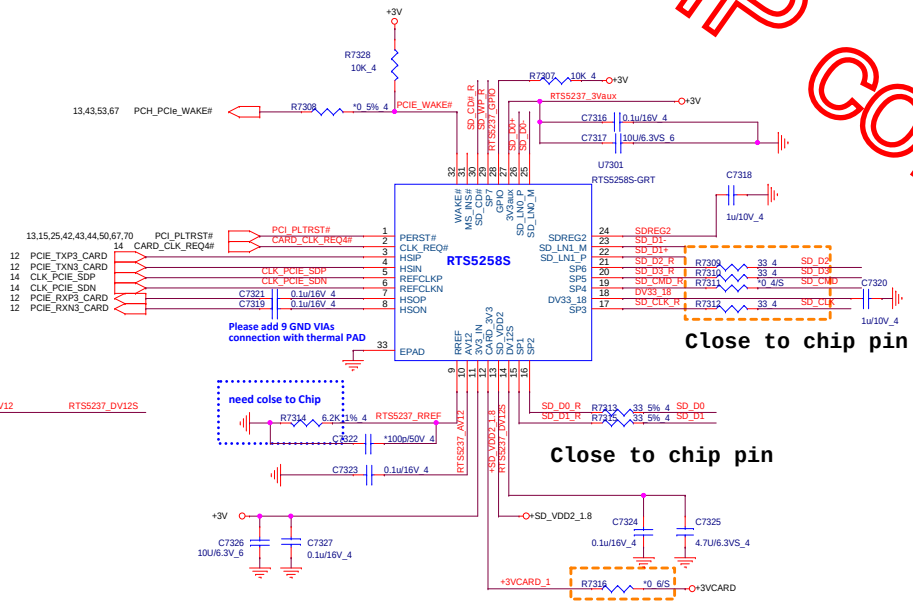
SP1	SD_WP	MS_D1
SP2	SD_D0	MS_D5
SP3	SD_D7	MS_D4
SP4	SD_D6	MS_D0
SP5	SD_CLK	MS_D2
SP6	SD_D5	MS_D6
SP7	SD_CMD	MS_D3
SP8	SD_D4	MS_D7
SP9	SD_D3	MS_CLK
SP10	SD_D2	MS_BS

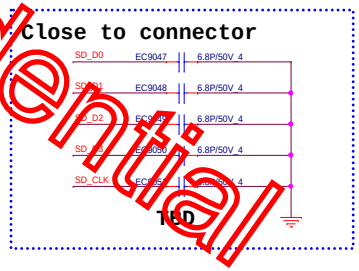
Share Pin

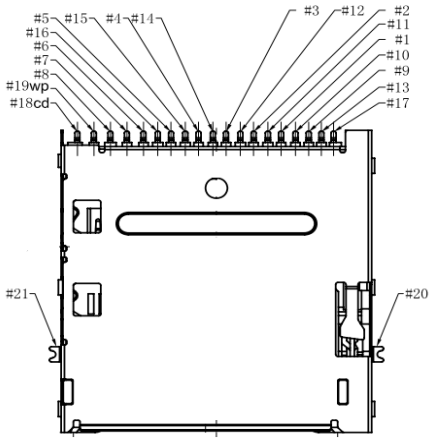
Card Reader CON







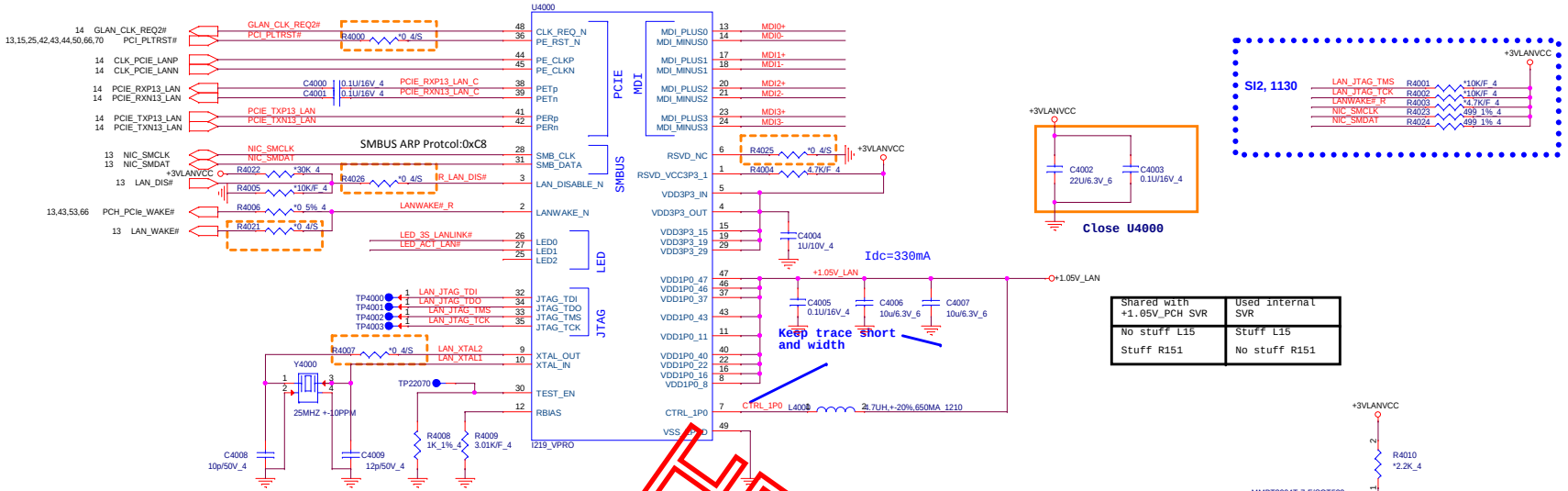




NO.	SD NAME	USH-LL NAME
1	CD/DAT3	
2	CMD	
3	VSS1	VSS1
4	VDD	VDD1
5	CLK	
6	VSS2	VSS2
7	DAT0	RCLK+
8	DAT1	RCLK-
9	DAT2	
10		VSS3
11		DO+
12		DO-
13		VSS4
14		VDD2
15		D1-
16		D1+
17		VSS5
18	CD SW	
19	WP SW	
20	GND SW	
21	GND SW	

XW2
Quanta Computer Inc.
NB5

Size	Document Number	Rev
	CardReader - RTS5258S	2A
<Title>		
Date: Wednesday, May 30, 2018	Sheet 66 of 97	



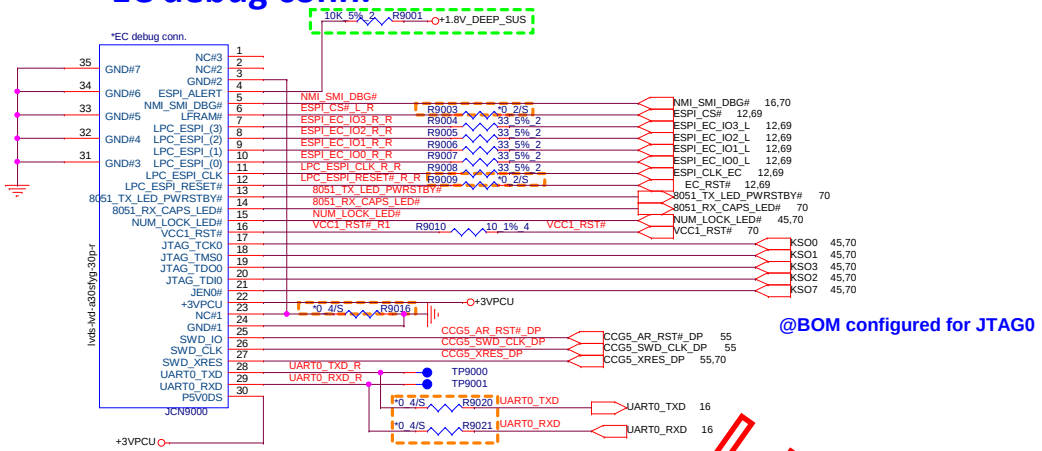
Shared with +1.05V_PCH SVR	Used internal SVR
No stuff L15	Stuff L15
Stuff R151	No stuff R151

Intel LAN "AL00QREF002"		
VPRO		
NON-VPRO		

Transformer for 10/100/1000

XW2
Quanta Computer Inc.
NB5
Size | Document Number: Intel WGI219LM | Rev: 2A
<Title>
Date: Wednesday, May 30, 2018 | Sheet 67 of 97

EC debug conn.



@BOM configured for JTAG0

+1.8V_DEEP_SUS 12,13,14,15,16,17,34,38,58,69,87,90

+3VPCU 12,13,17,19,24,34,41,43,44,45,47,49,54,55,69,70,71,75,76,77,78,79,80,81,82,84,85,86,87,88,89,90,91,94
+3V 5,12,13,14,16,20,21,22,23,27,28,33,34,35,36,40,41,42,43,44,45,47,48,49,50,51,54,59,63,65,66,69,73,77,84,87,90,93,94

XW2
Quanta Computer Inc.
NB5

Size	Document Number	Rev
Custom	EC & eSPI/UART debug connector	2A
Date: Wednesday, May 30, 2018	Sheet 68 of 97	

EC797 : +VHIF
ES Sample:staff R6097
QS Sample:staff R6098

CPU SKU	CFLH4	CFLH6
Ra	ADD	NC
Rb	NC	ADD

CHARGE ADD: 0x13/0x12
for Battery charge/charge
for Thermal IC/Speaker AMP

for PD1/PD2

0927Bear

NOTE:
Place a 1 uF capacitor as close to the CAP pin as possible.

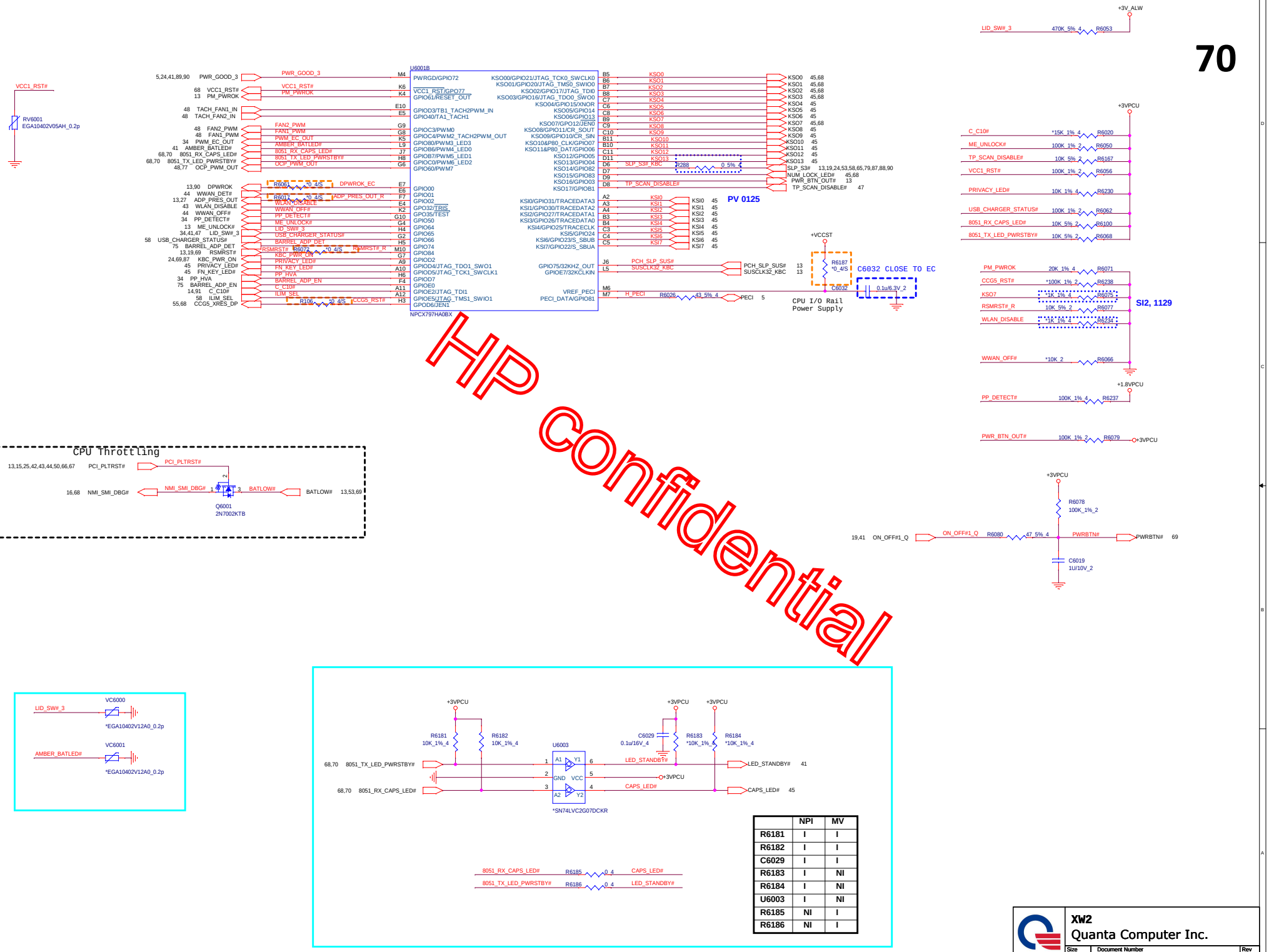
NOTE:
Connect GND and AGND planes via an 0R resistor or a one-point layout connection.

SI2R, 0108

SI2, 1124

PV, 0126

XW2
Quanta Computer Inc.
NB5
Size C | Document Number EC Nuvoton NPCE576H_1 | Rev 2A
Date: Wednesday, May 30, 2018 | Sheet 69 of 98

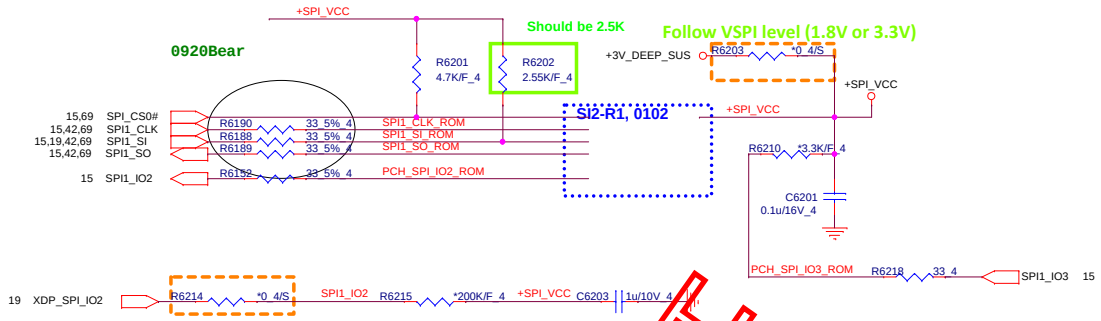


	NPI	MV
R6181	I	I
R6182	I	I
C6029	I	I
R6183	I	NI
R6184	I	NI
U6003	I	NI
R6185	NI	I
R6186	NI	I

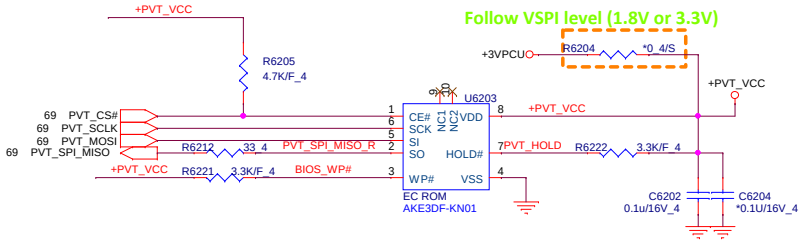
XW2
Quanta Computer Inc.
NB5
Size C | Document Number EC Nuvoton NPCE576H_2 | Rev 2A
Date: Wednesday, May 30, 2018 | Sheet 70 of 98

PCH SPI ROM(CLG)

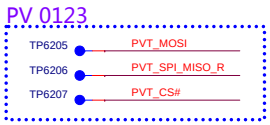
PCH 6*5mm WSON 32M
SPI ROM Socket



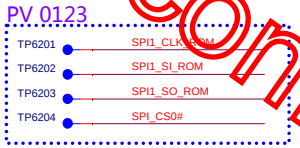
EC 6*5mm WSON 16M
SPI ROM Socket



PV 0123

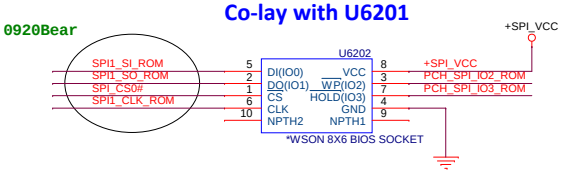


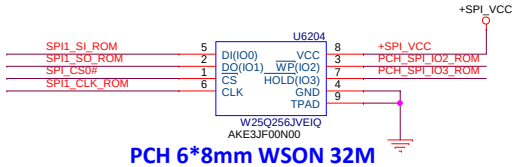
PV 0123



SPI ROM 32M 8x6 socket

SPI ROM 32M 8x6
Co-lay with U6201



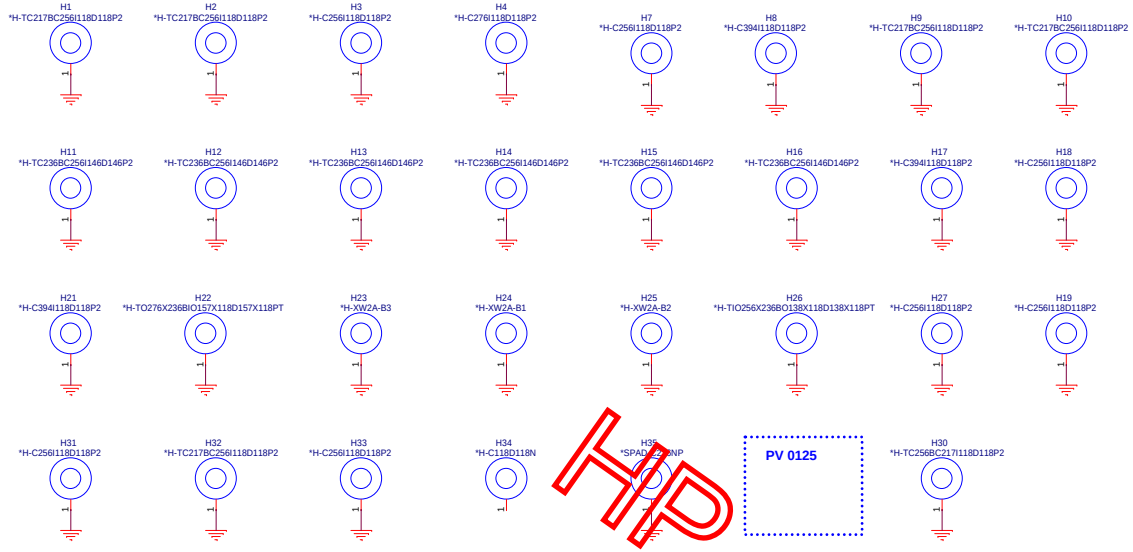


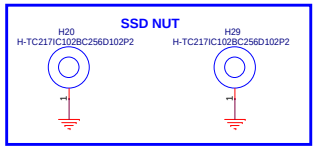
PCH 6*8mm WSON 32M

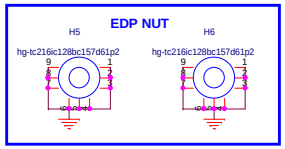
SPI ROM 32M 8x6 IC & 6x5 Socket & 8*6 Socket
(U6201/U6202/U6204)co-lay

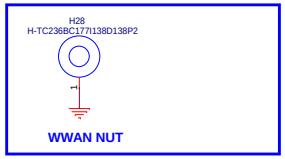
NB5	XW2 Quanta Computer Inc.	
Size: Custom	Document Number: Flash(KBC+PCH)	Rev: 2A
Date: Wednesday, May 30, 2018	Sheet: 71of 97	

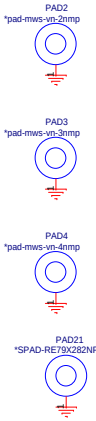
Screw Hole



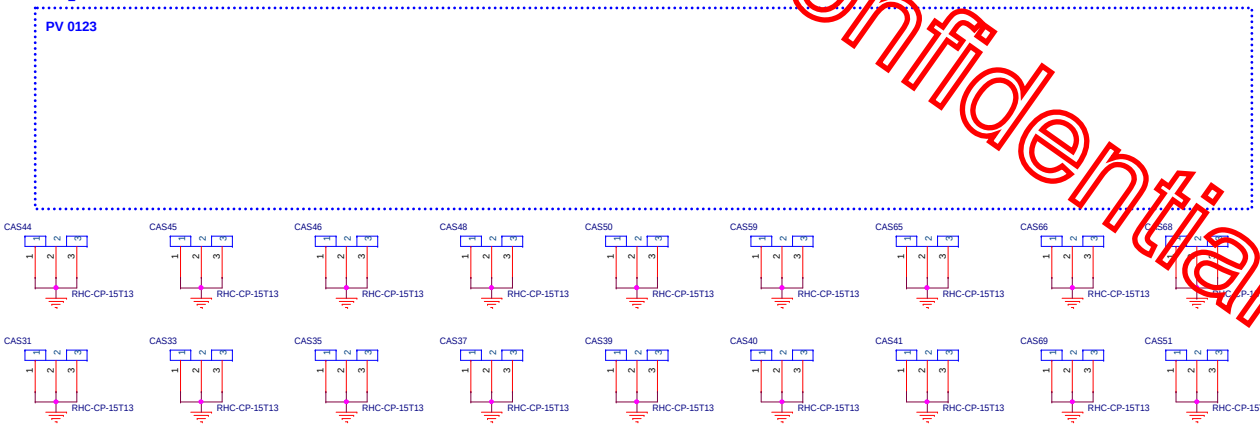






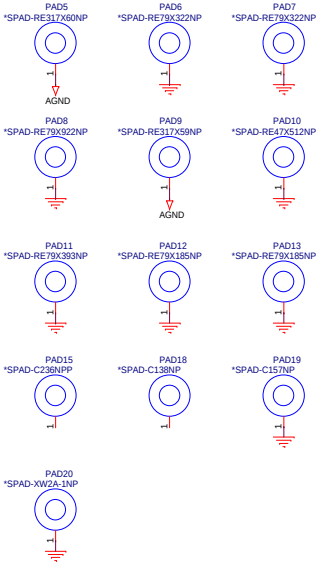


RAM Clip

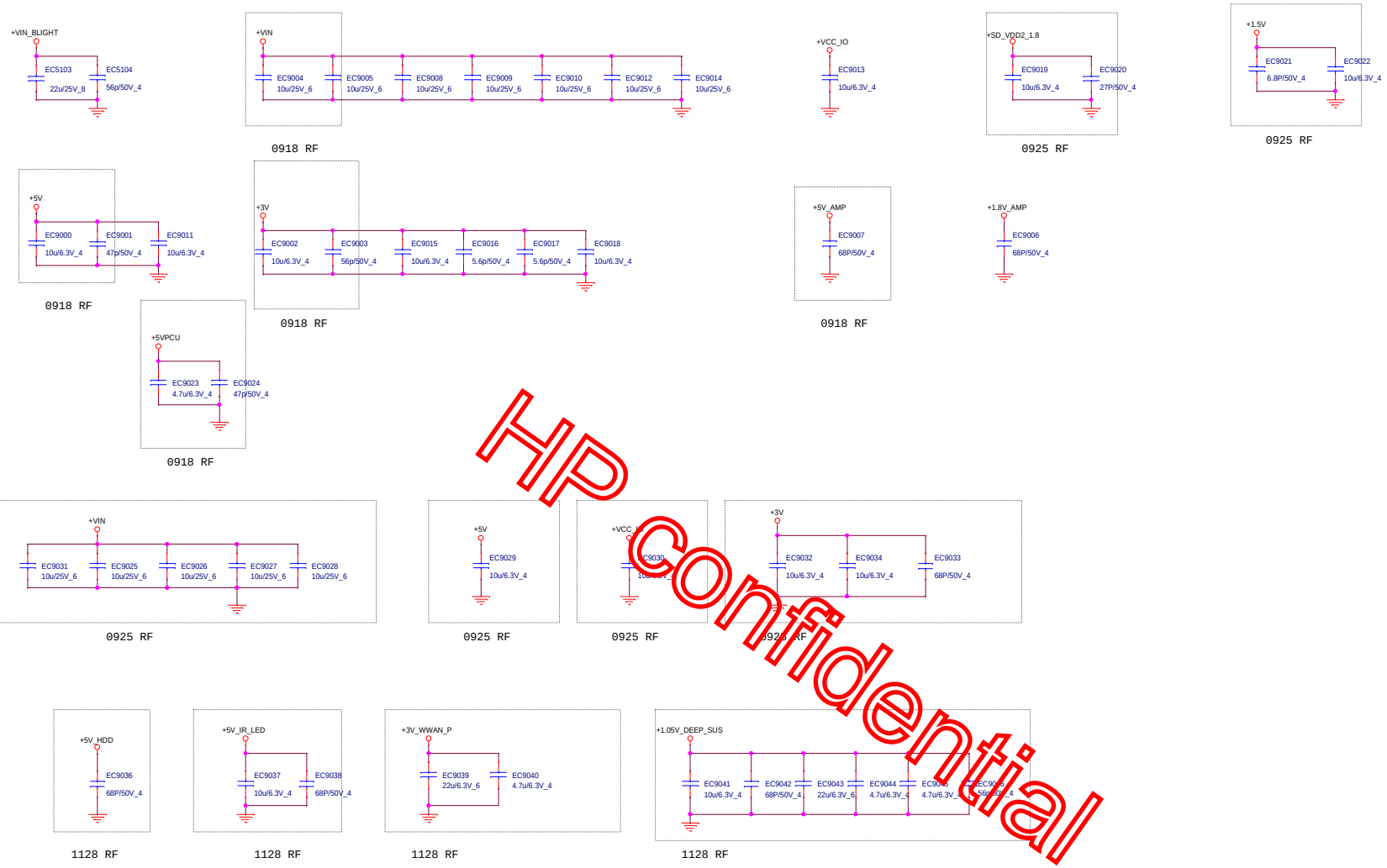


USBC Clip

PV 0202 delete



NB5	XW2 Quanta Computer Inc.	
	Size: <Title>	Document Number: Screw Hole
	Date: Wednesday, May 30, 2018	Sheet 72 of 97

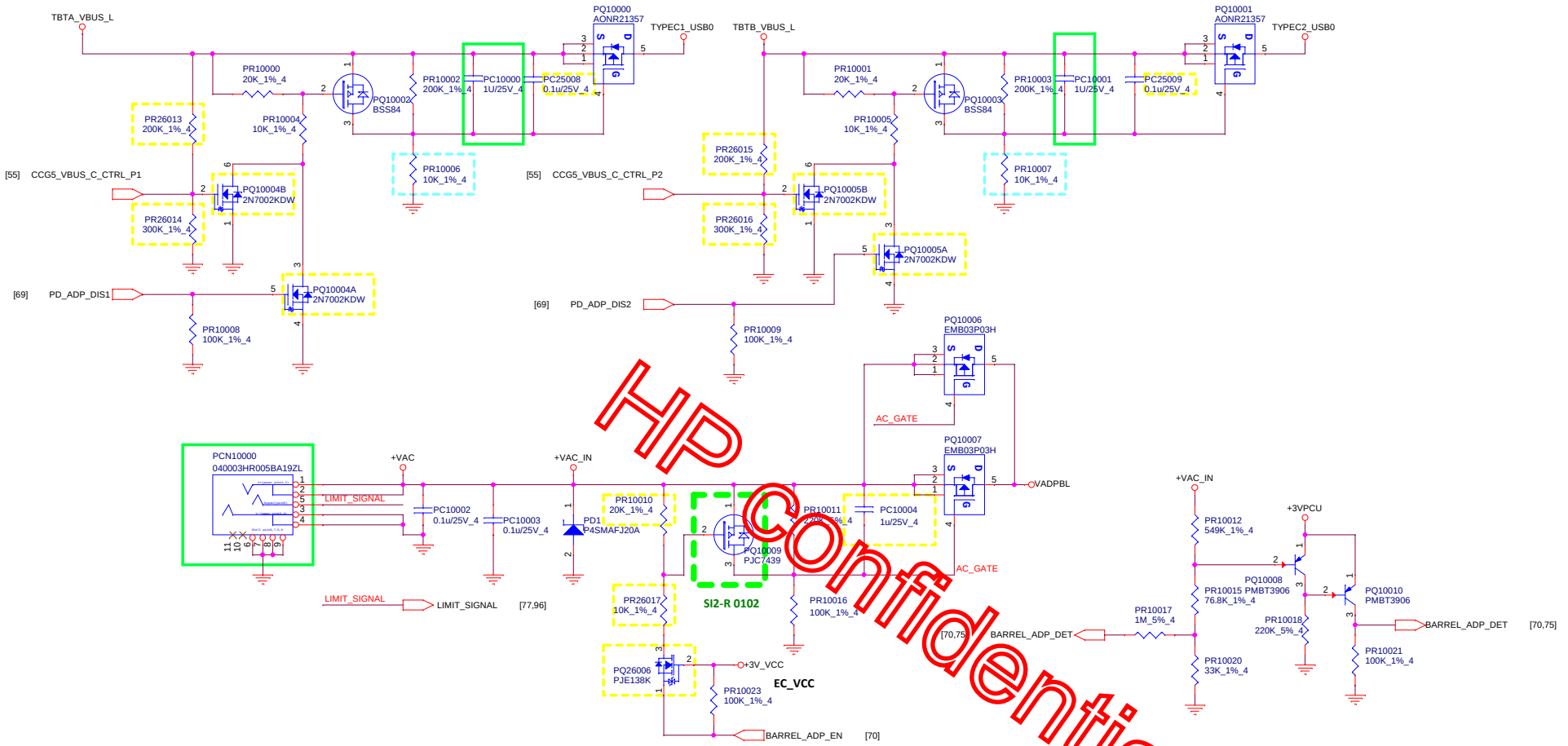


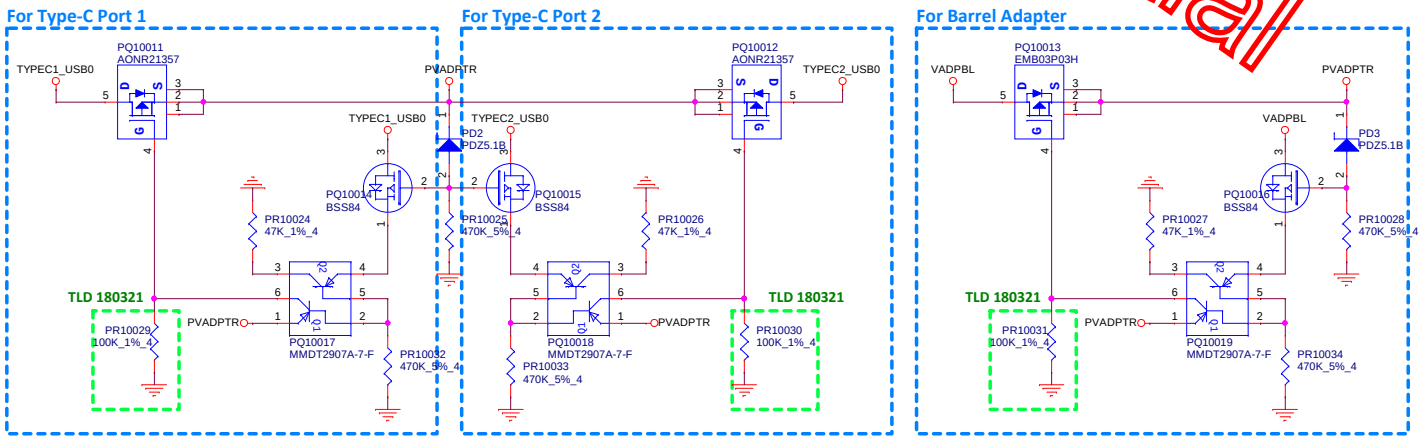
NB5	XW2 Quanta Computer Inc.
Size	Document Number: RF & EMI
Rev	2A
<Title>	
Date: Wednesday, May 30, 2018	Sheet 73 of 97

NB5

XW2
Quanta Computer Inc.

Size	Document Number	Rev
<Title>	NA	2A
Date: Wednesday, May 30, 2018	Sheet 74 of 97	





NB5	XW2 Quanta Computer Inc.	
Size: Custom	Document Number: 75 -- TYPE-C/Barrel switch	Rev: 1A
Date: Wednesday, May 30, 2018	Sheet 75 of 97	

When ACDET pin is above 0.6 V and VCC is above UVLO, REGN LDO is present, ACOK comparator, input current buffer (IADP), discharge current buffer (IDCHG), independent comparator, and power monitor buffer (PMON) can be enabled with SMBus. When ACDET is above 2.4V, and VCC is above SRN but below ACOV, ACOK goes HIGH.

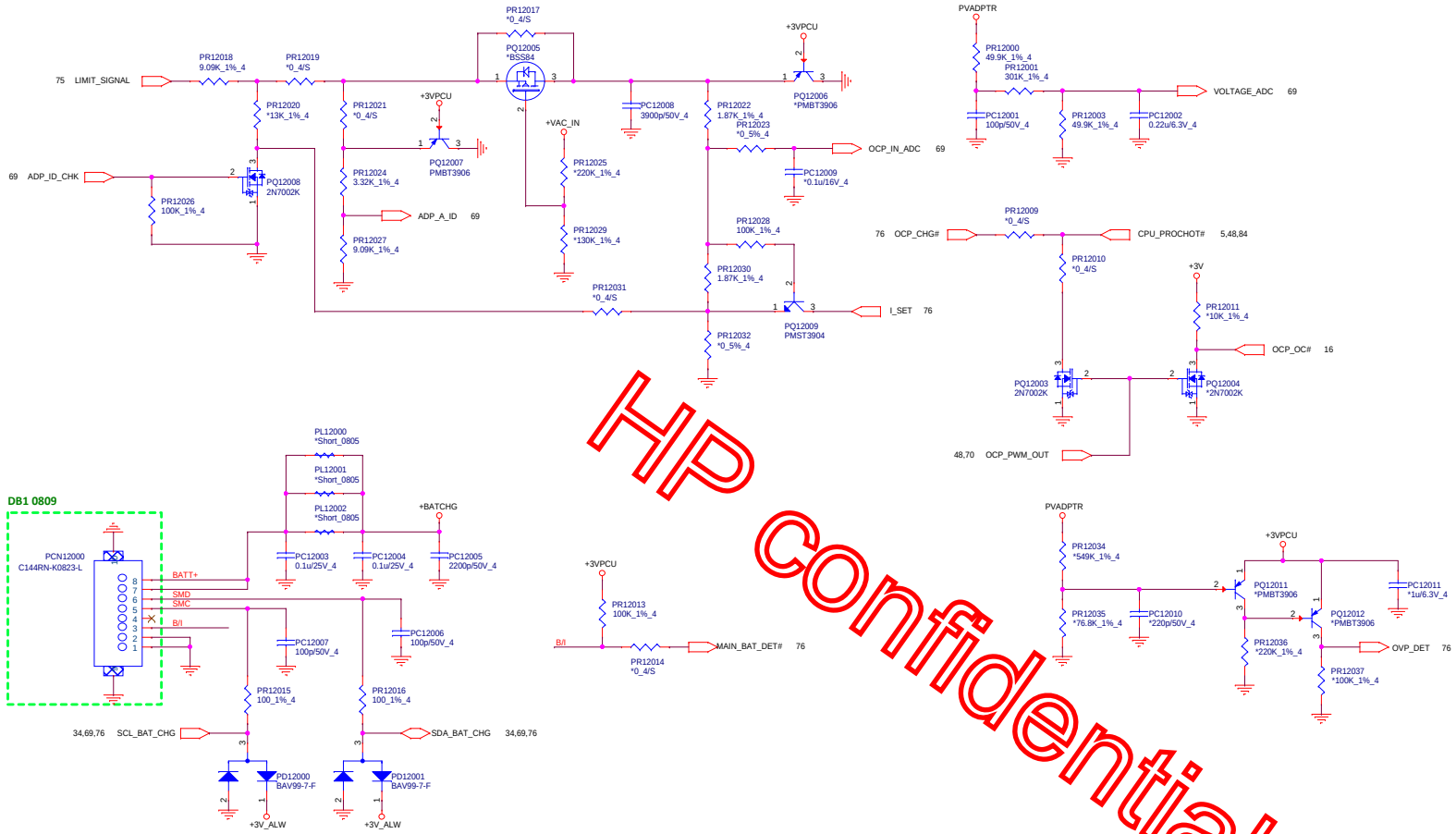
Place this TVS as close as possible to the furthest +VIN shape

DCR= 7 mohm (max.)

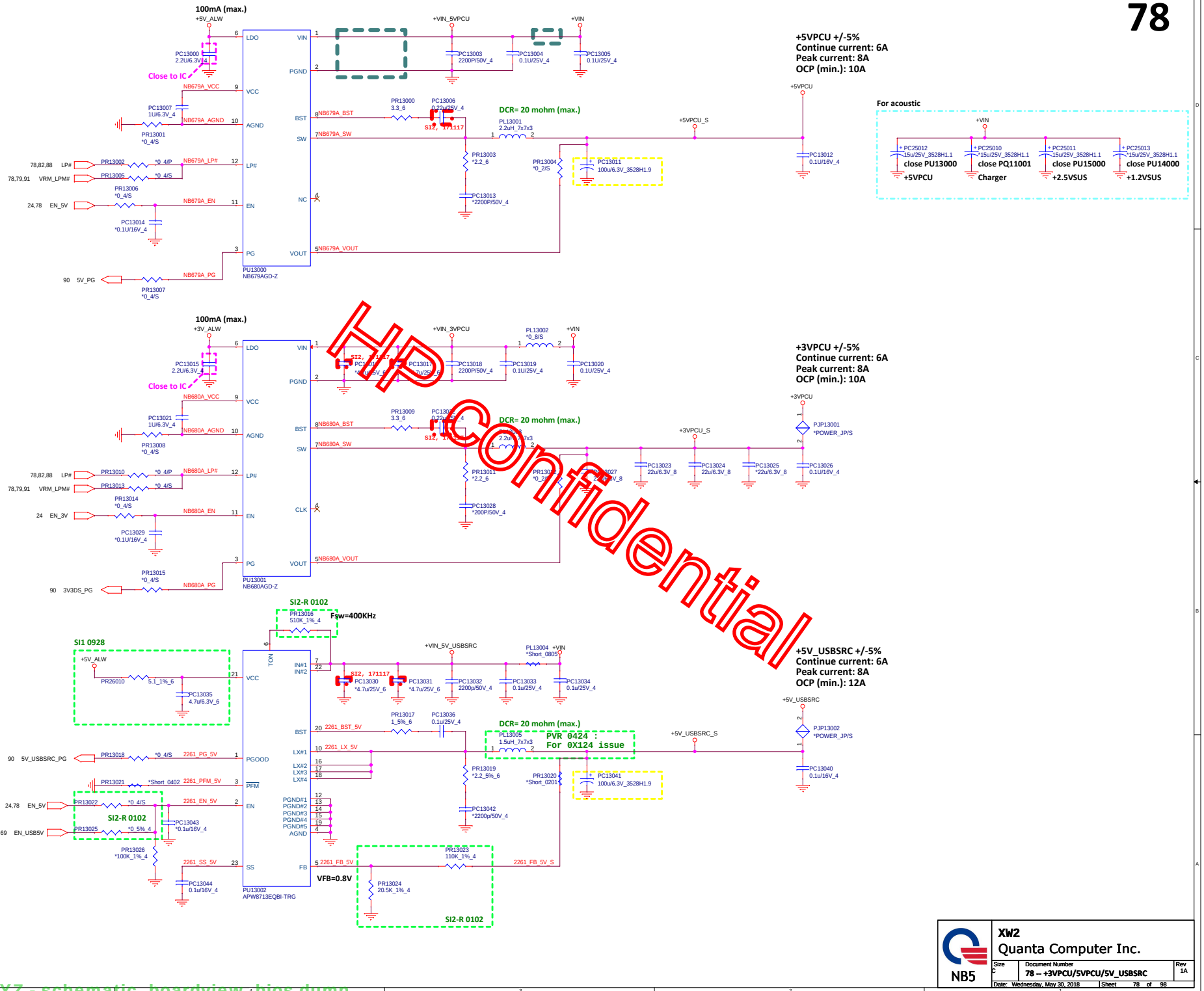
Thermal Sensor for Fast Charging

***Place close to charger IC pin

XW2	Quanta Computer Inc.
NB5	Size: Custom; Document Number: 76 -- Charger (BQ24780S); Rev: 2A
	Date: Wednesday, May 30, 2018; Sheet 76 of 98

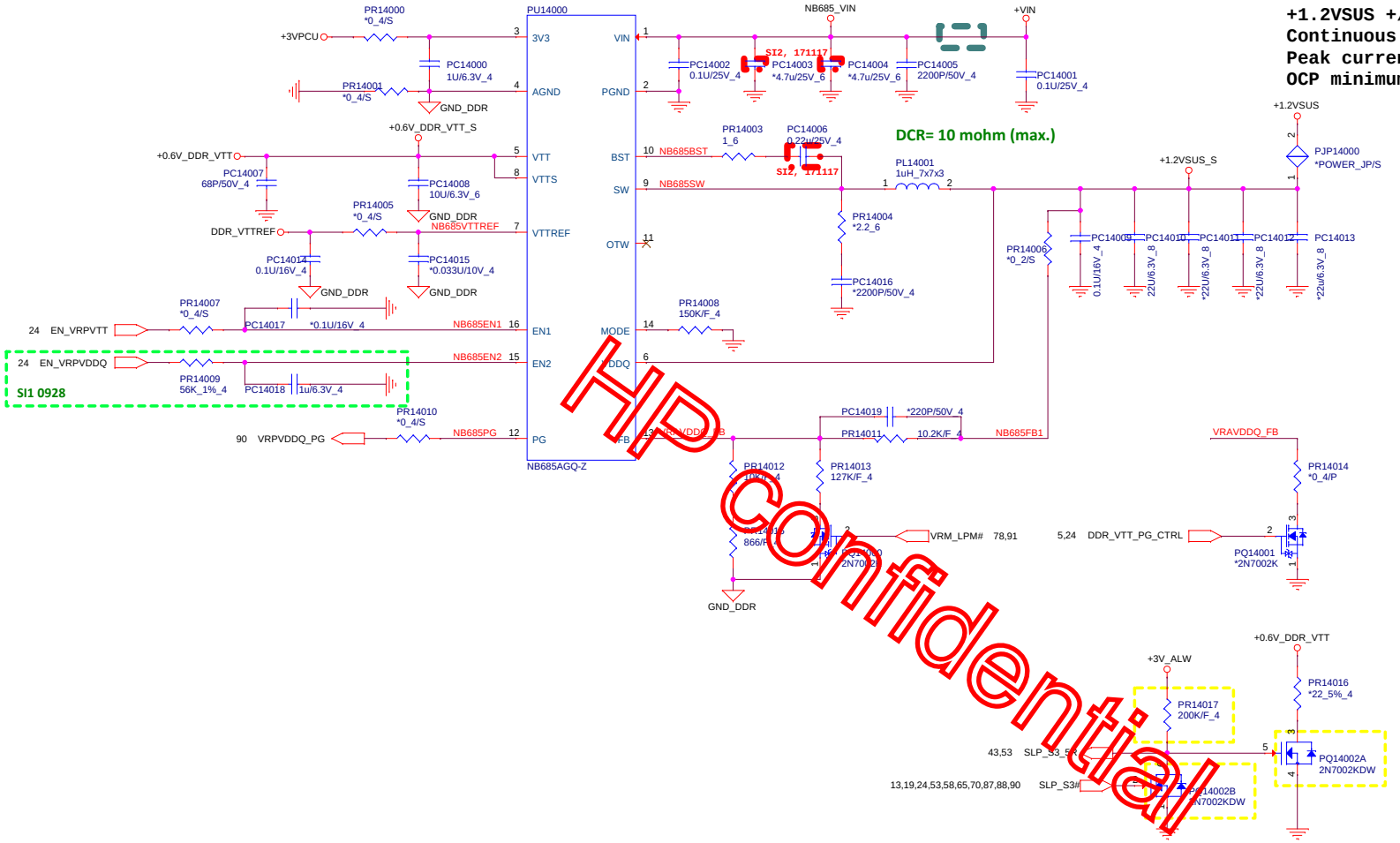


NB5	XW2 Quanta Computer Inc.	
Size	Document Number 77 -- Charger II	Rev 2A
Date: Wednesday, May 30, 2018	Sheet 77 of 98	

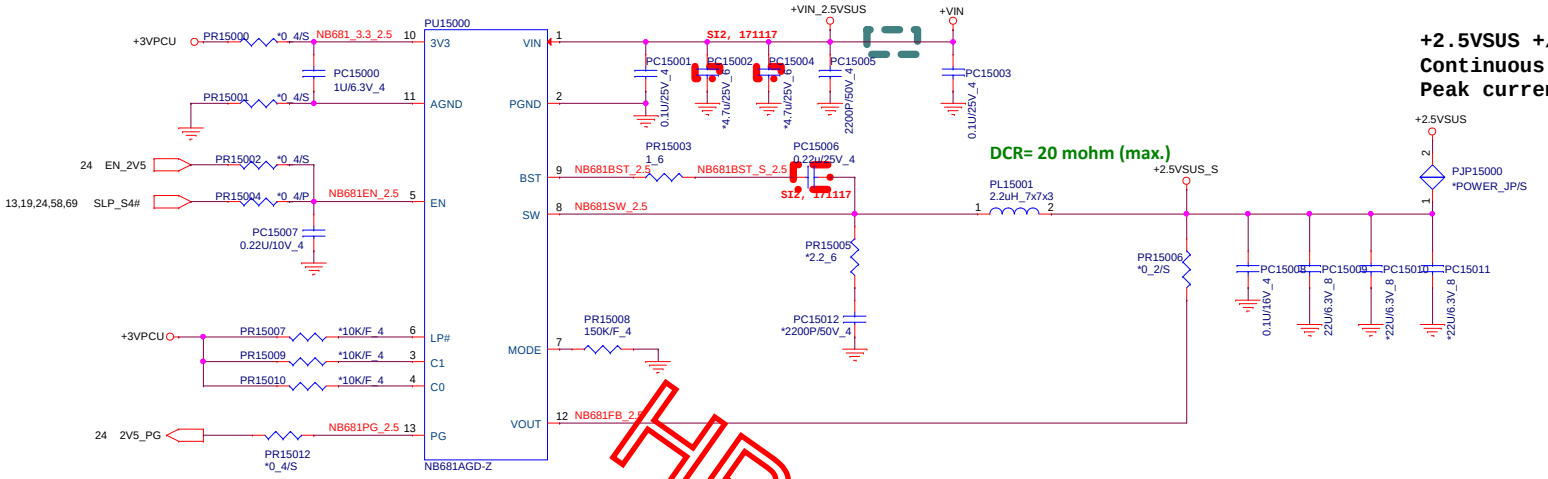


NB5	XW2 Quanta Computer Inc.		
	Size C	Document Number 78 -- +3VPCU/5VPCU/5V_USBSRC	Rev 1A
	Date: Wednesday, May 30, 2018	Sheet 78 of 98	

+1.2VSUS +/-5%
Continuous current: 8A
Peak current: 10A
OCP minimum: 12A



NB5	XW2 Quanta Computer Inc.	
Size	Document Number 79 -- DDR4 (NB685A)	Rev 1A
Date: Wednesday, May 30, 2018	Sheet 79 of 98	

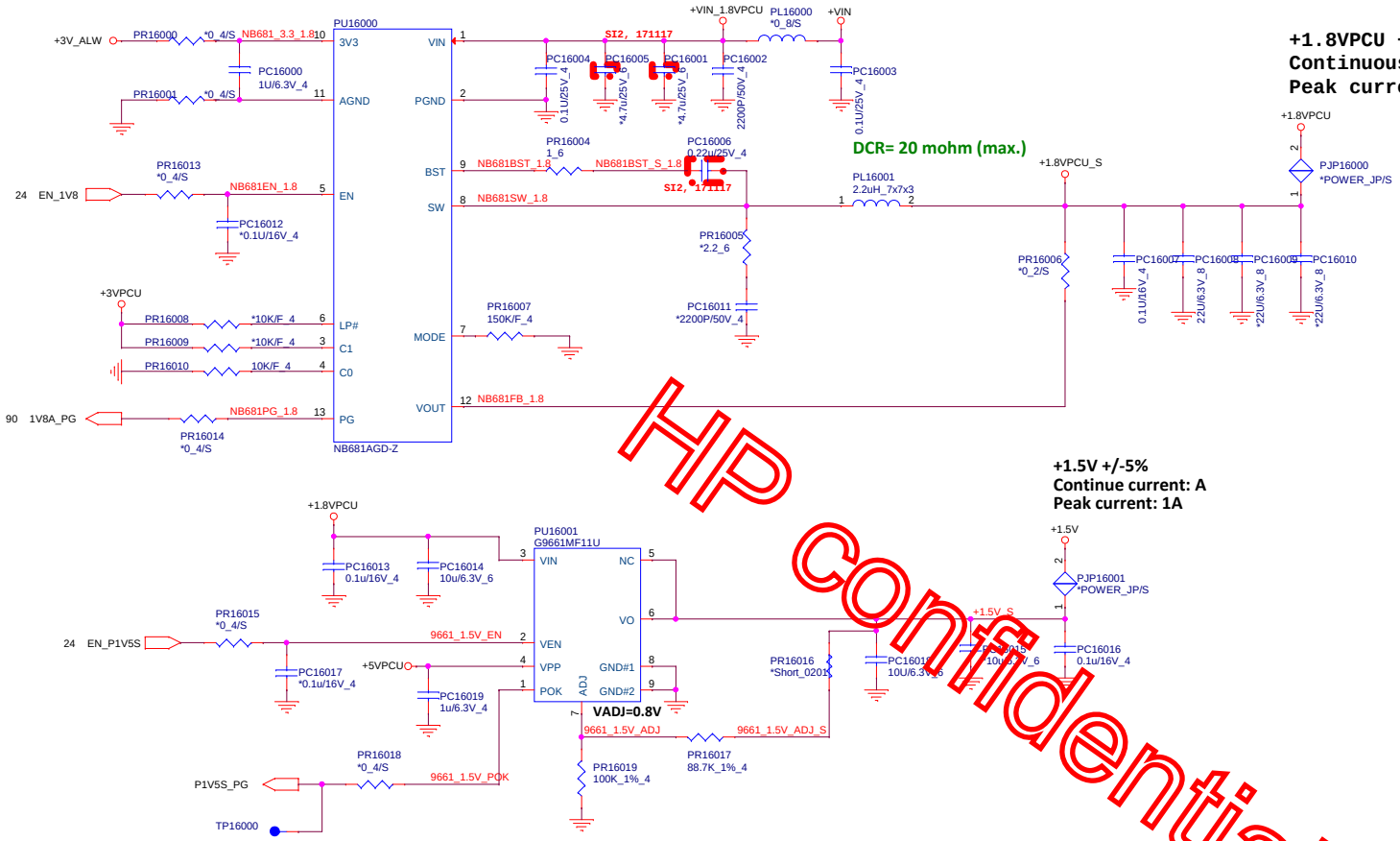


+2.5VSUS +/-5%
Continuous current: 2A
Peak current: 3A

DCR= 20 mohm (max.)

MODE	VR Rail	Resistor to GND (1% Accuracy)
M1	VCCIO	0
M2	PRIMCORE	Float or > 230K
M3	EDRAM/V1.0A/EOPIO	100K
M4	Others	150K

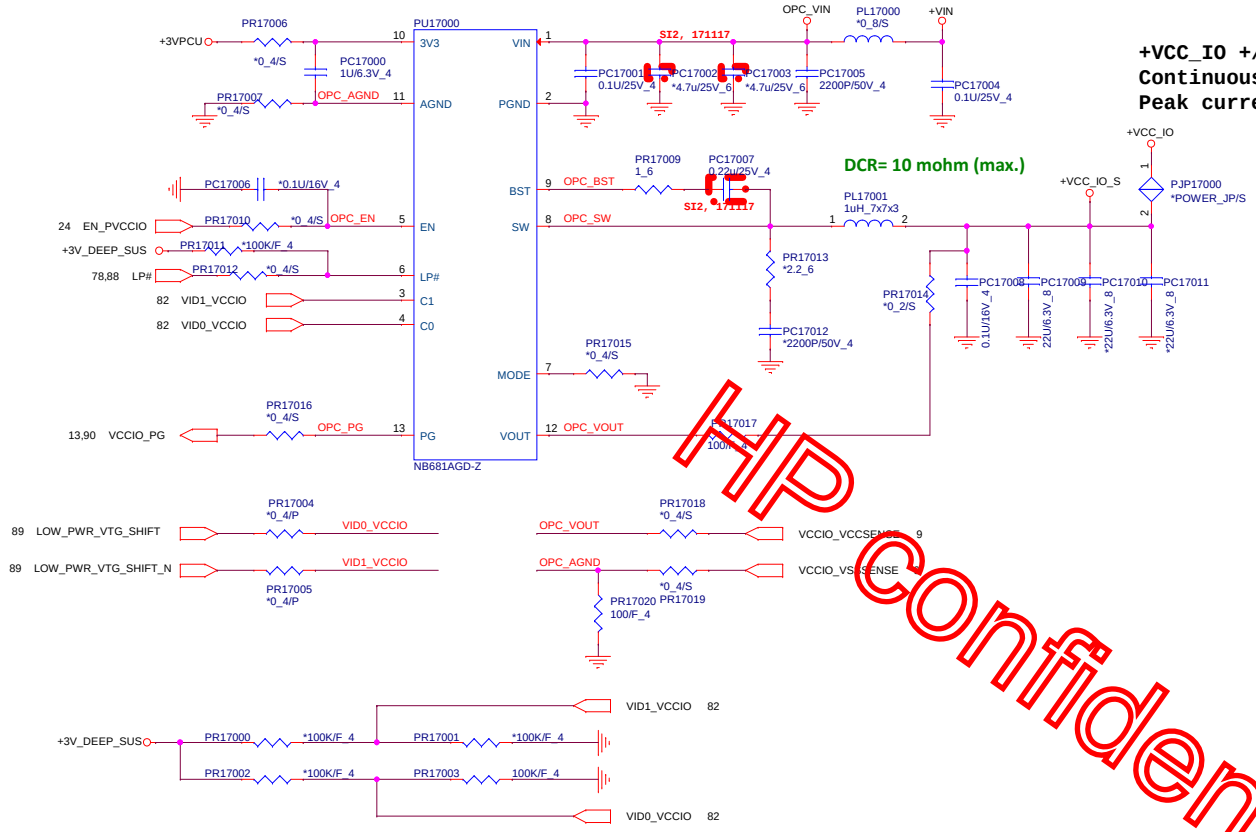
	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPRIM_CORE	0	X	X	0.7
	1	0	0	0.85
	1	0	1	0.9
	1	1	0	0.95
	1	1	1	1.00
EDRAM/ EOPIO/ V1.0A	0	X	X	0
	1	0	0	0.8 (MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others (Fixed design only, not allowed for changing on-the-fly)	0	0	0	1.59
	0	0	1	1.99
	0	1	0	2.38
	0	1	1	3.3
	1	0	0	1.2
	1	0	1	1.5
	1	1	0	1.8
	1	1	1	2.5



MODE	VR Rail	Resistor to GND (1% Accuracy)
M1	VCCIO	0
M2	PRIMCORE	Float or > 230K
M3	EDRAM/V1.0A/EOPIO	100K
M4	Others	150K

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPRIM_CORE	0	X	X	0.7
	1	0	0	0.85
	1	0	1	0.9
	1	1	0	0.95
	1	1	1	1.00
EDRAM/ EOPIO/ V1.0A	0	X	X	0
	1	0	0	0.8 (MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others (Fixed design only, not allowed for changing on-the-fly)	0	0	0	1.59
	0	0	1	1.99
	0	1	0	2.38
	0	1	1	3.3
	1	0	0	1.2
	1	0	1	1.5
	1	1	0	1.8
	1	1	1	2.5

XW2
Quanta Computer Inc.
NB5
Size: Custom | Document Number: 81 -- +1.8VPCU (NB681A) | Rev: 2A
Date: Wednesday, May 30, 2018 | Sheet 81 of 98



MODE	VR Rail	Resistor to GND (1% Accuracy)
M1	VCCIO	0
M2	PRIMCORE	Float or > 230K
M3	EDRAM/V1.0A/EOPIO	100K
M4	Others	150K

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPRIM_CORE	0	X	X	0.7
	1	0	0	0.85
	1	0	1	0.9
	1	1	0	0.95
	1	1	1	1.00
EDRAM/ EOPIO/ V1.0A	0	X	X	0
	1	0	0	0.8 (MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others (Fixed design only, not allowed for changing on-the-fly)	0	0	0	1.59
	0	0	1	1.99
	0	1	0	2.38
	0	1	1	3.3
	1	0	0	1.2
	1	0	1	1.5
	1	1	0	1.8
	1	1	1	2.5

NB5

XW2
Quanta Computer Inc.

Size	Document Number	Rev
	82 -- +VCC_IO (NB681A)	2A

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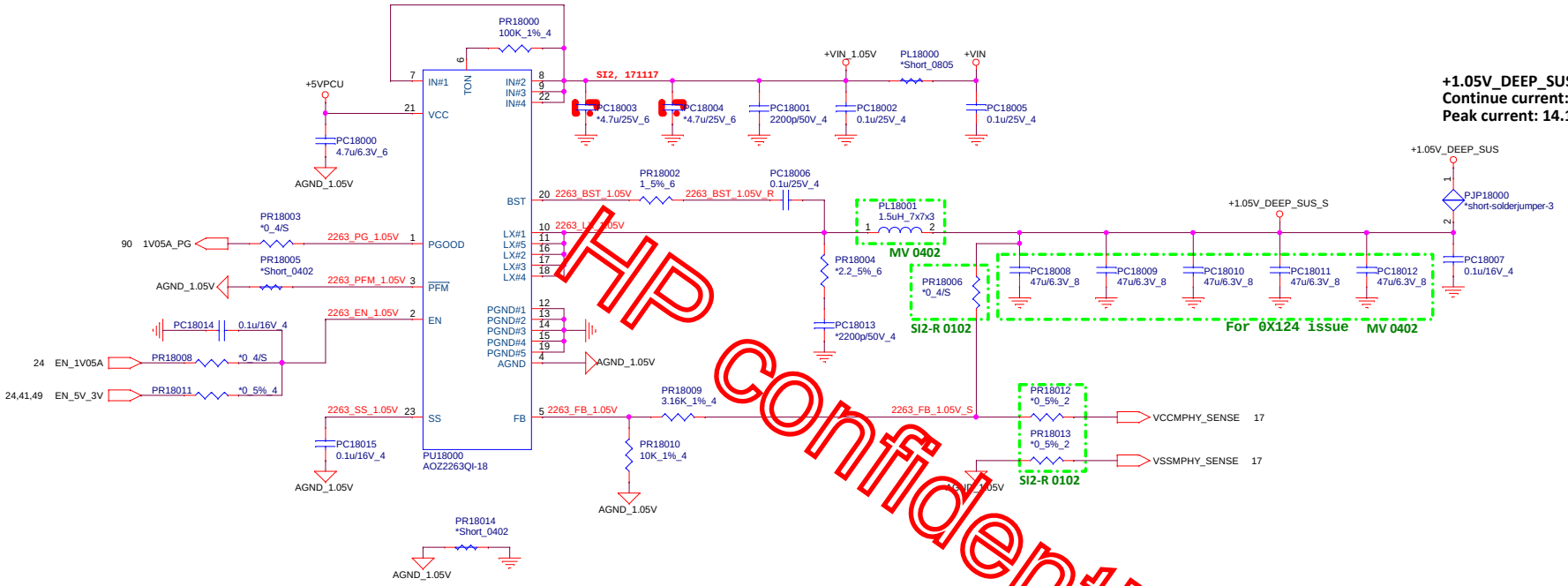
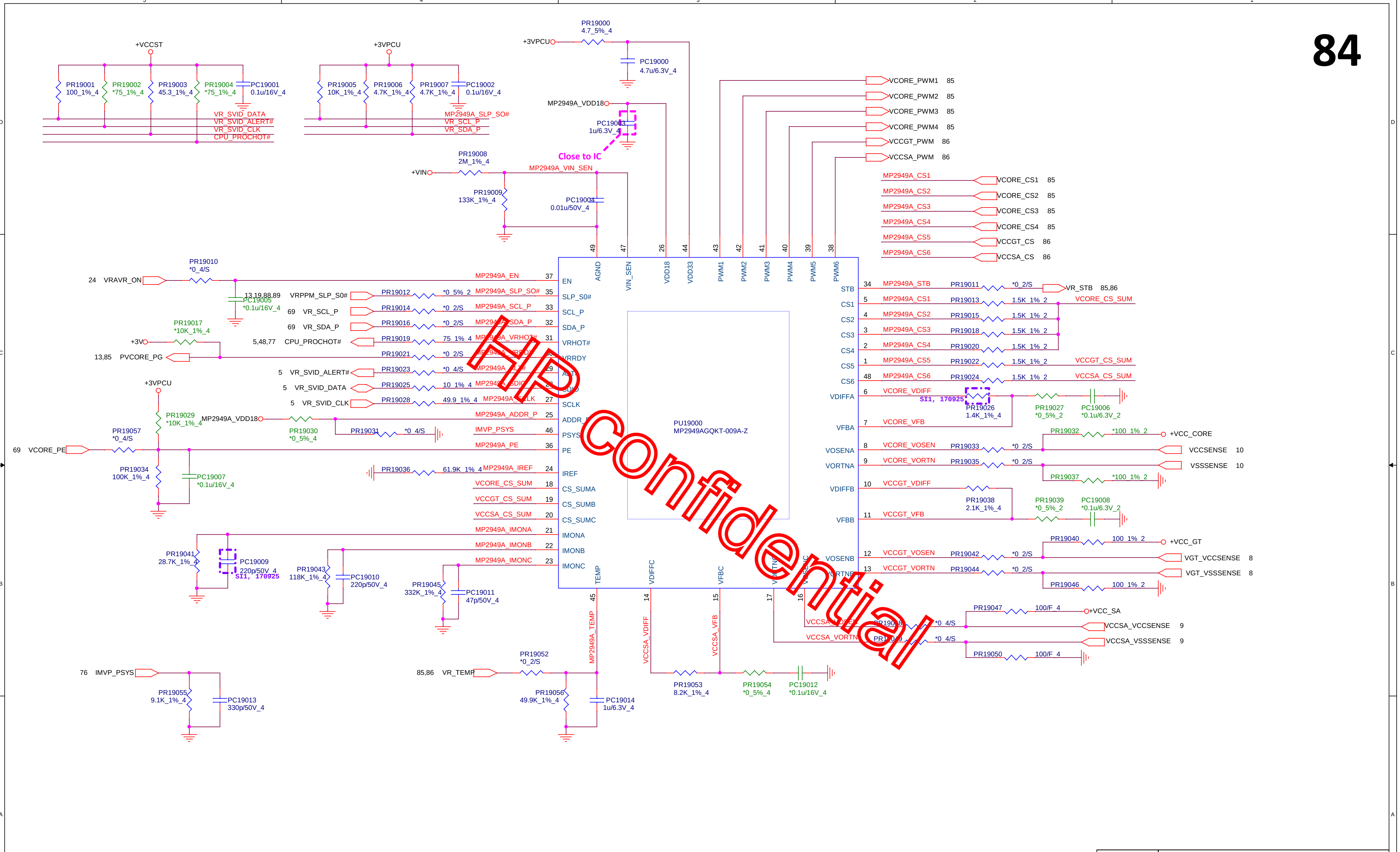


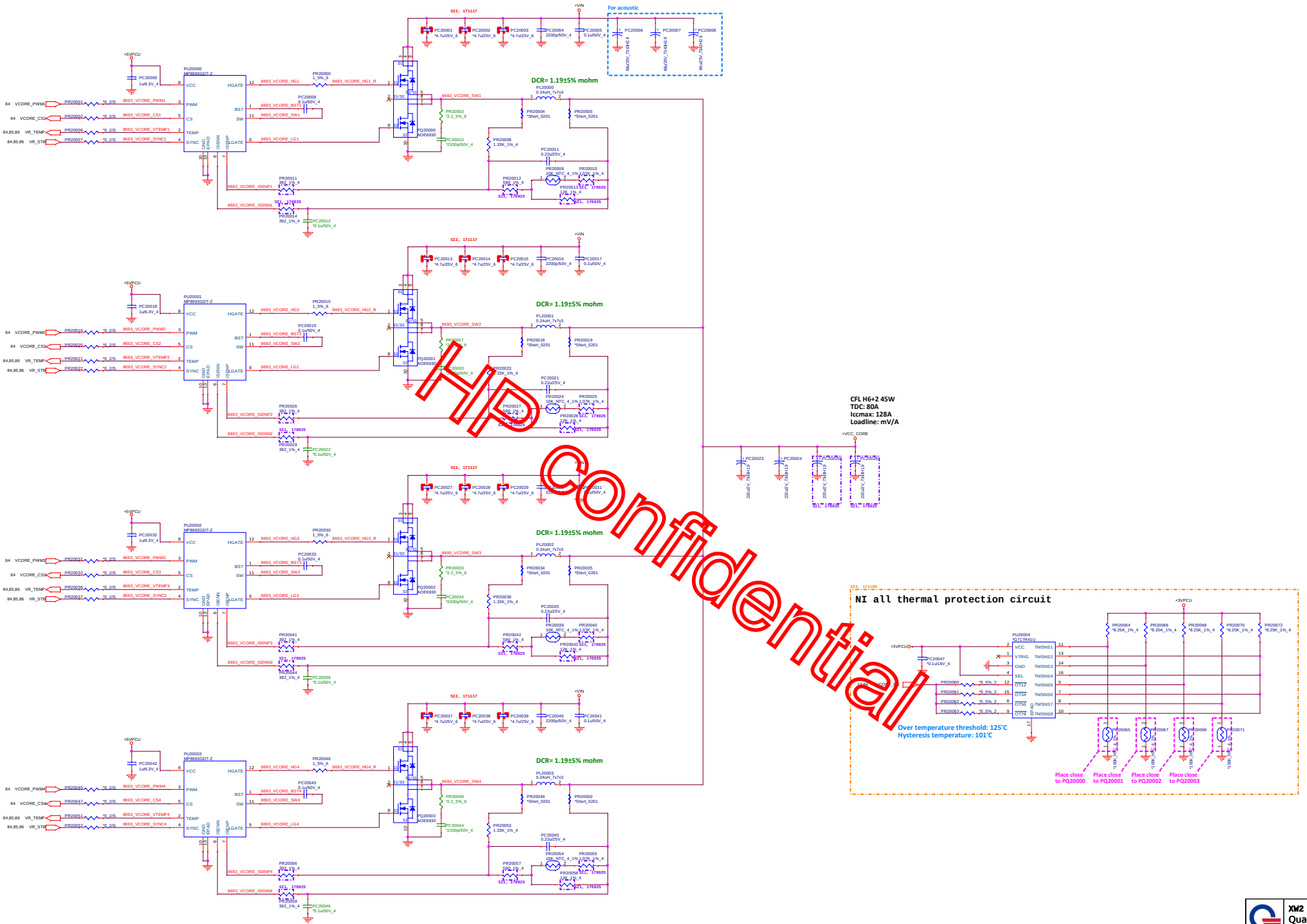
NB5	XW2 Quanta Computer Inc.	
	Size	Document Number 83 -- +1.05V_ DEEP_SUS(AOZ2263)
		Rev 2A
	Date: Wednesday, May 30, 2018	Sheet 83 of 98



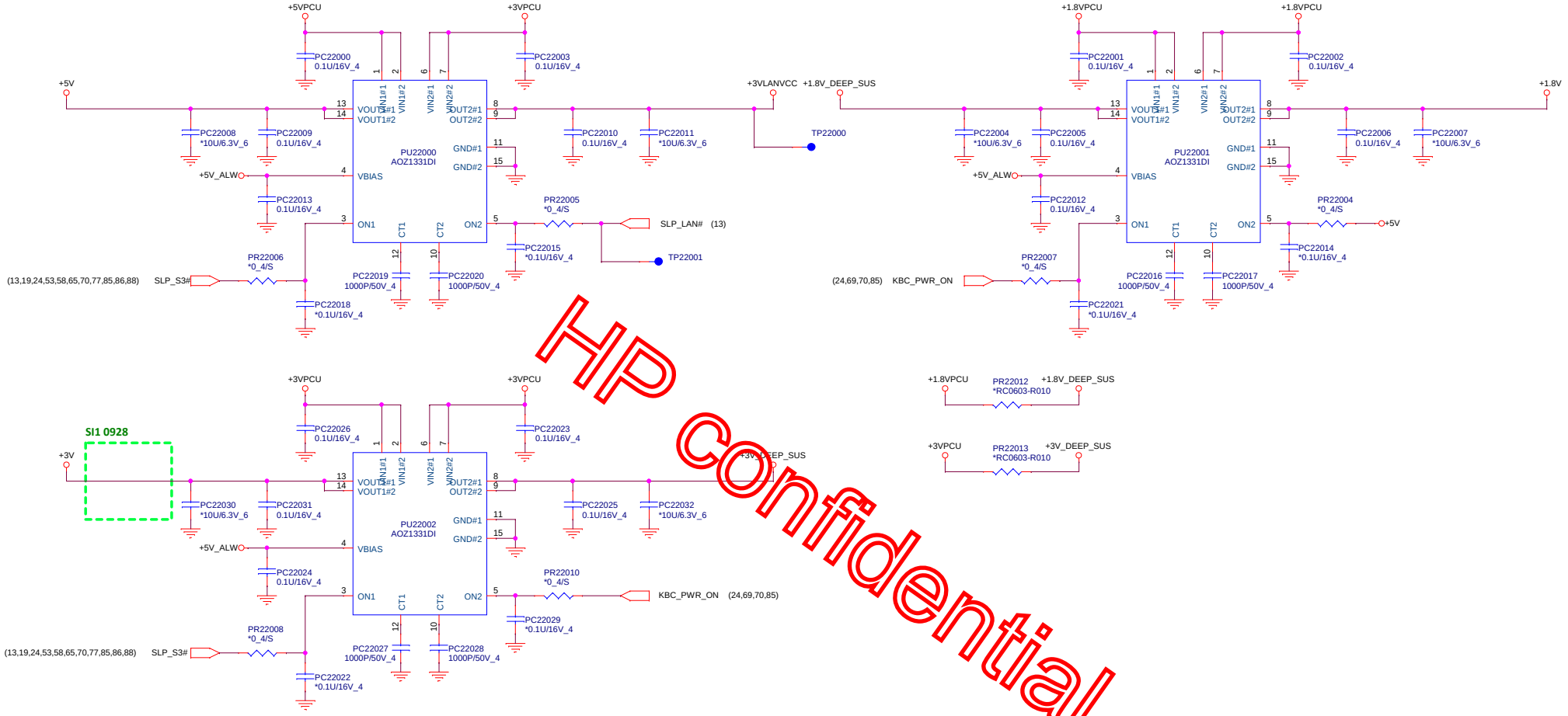
XW2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	84 -- CPU CORE VR (MP2949A)	2A

Date: Wednesday, May 30, 2018 | Sheet 84 of 98



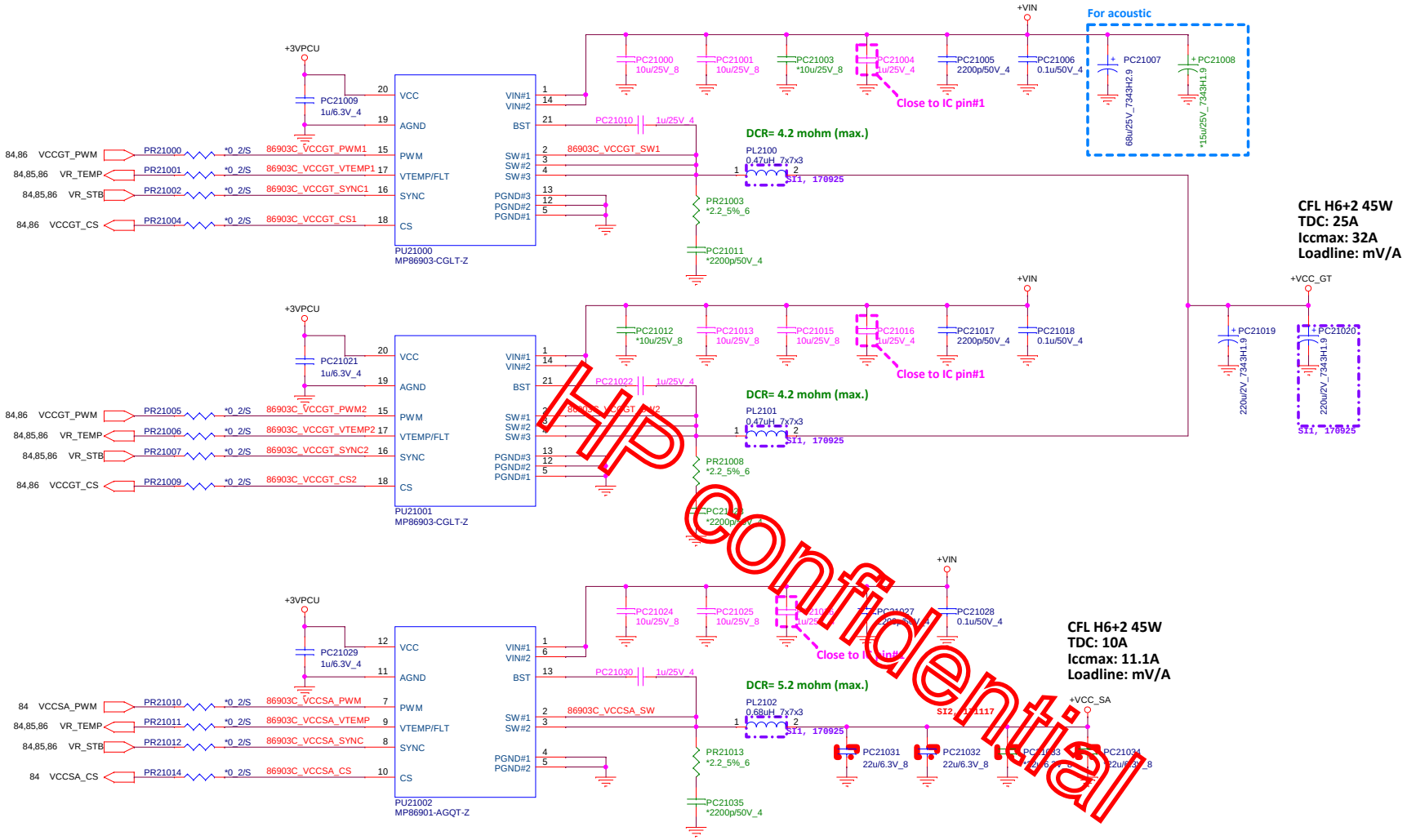
XW2	Quanta Computer Inc.
Size: D	Document Number: 85 -- +VCC_CORE (MP86903-C)
Date: Wednesday, May 30, 2018	Sheet 85 of 98



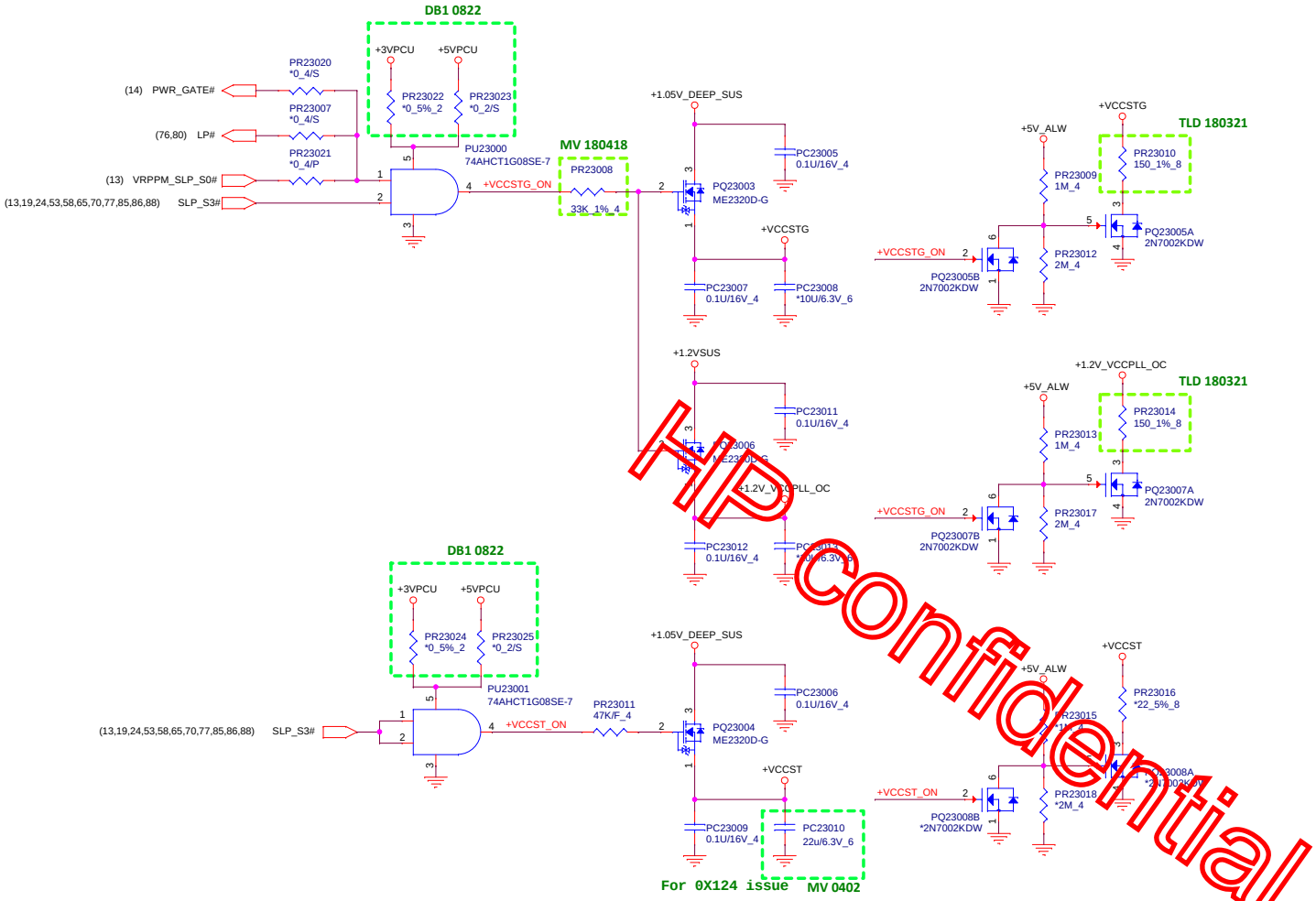
NB5

XW2
Quanta Computer Inc.

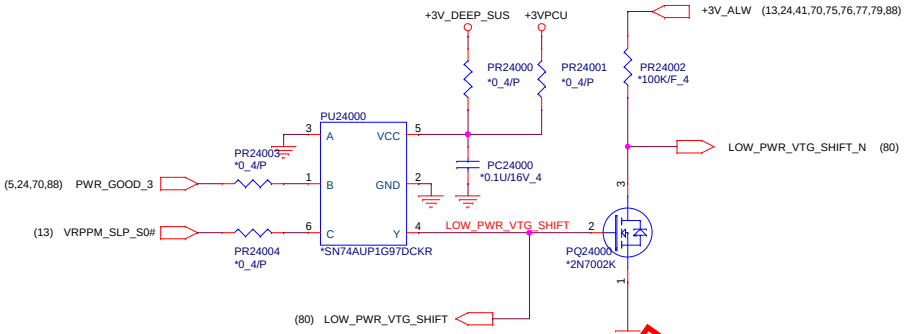
Size	Document Number	Rev
	87 -- Load switch I (AOZ1331DI)	1A
Date: Wednesday, May 30, 2018	Sheet 85 of 95	



NB5	XW2 Quanta Computer Inc.	
Size: Custom	Document Number: 86 -- +VCC_GT/+VCC_SA	Rev: 2A
Date: Wednesday, May 30, 2018	Sheet 86 of 98	



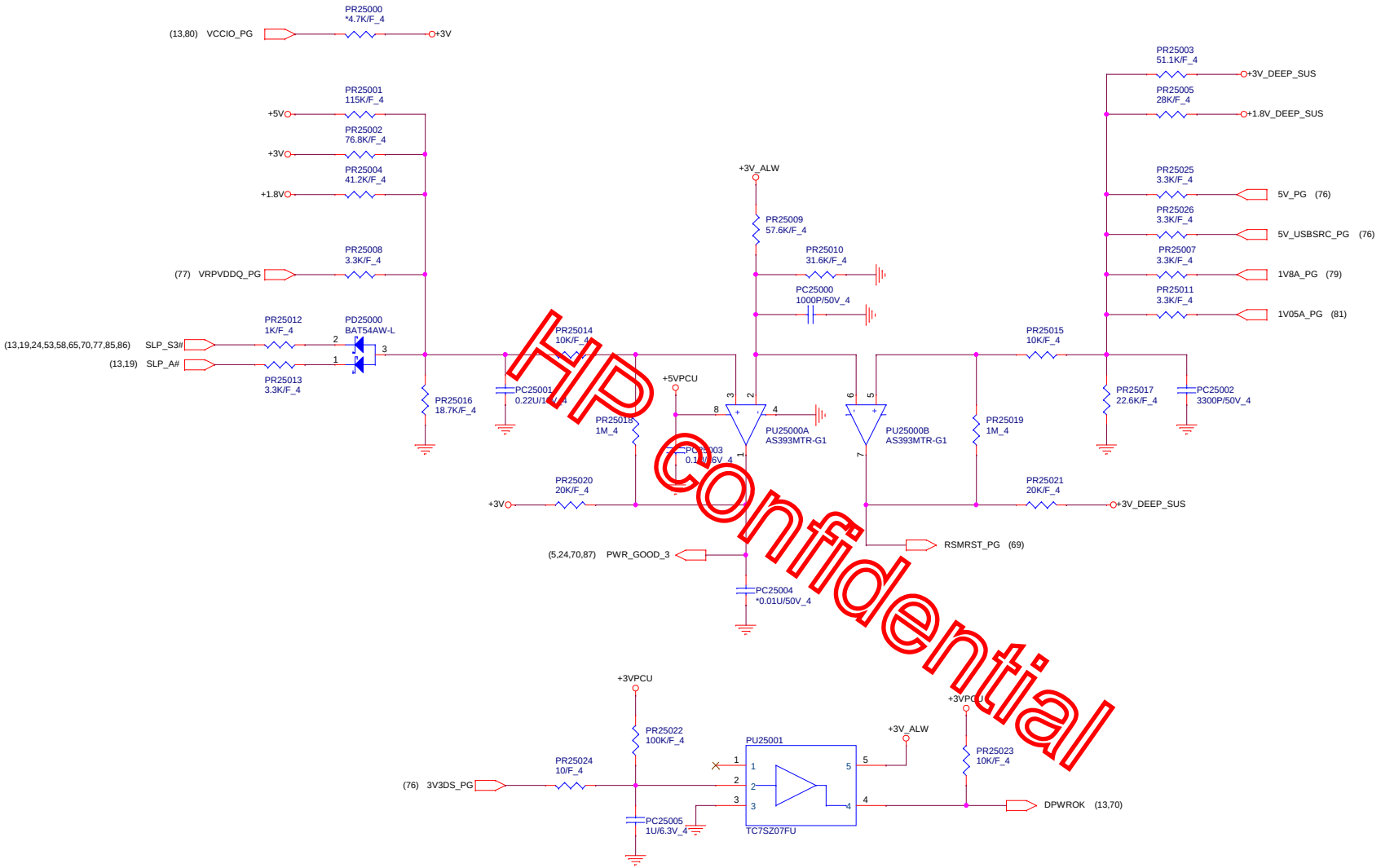
NB5	XW2 Quanta Computer Inc.	
Size	Document Number 88 -- Load switch II	Rev 1A
Date: Wednesday, May 30, 2018	Sheet 86 of 95	



NB5

XW2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	89 -- Low Power Voltage Shift	1A
Date: Wednesday, May 30, 2018	Sheet 87 of 95	



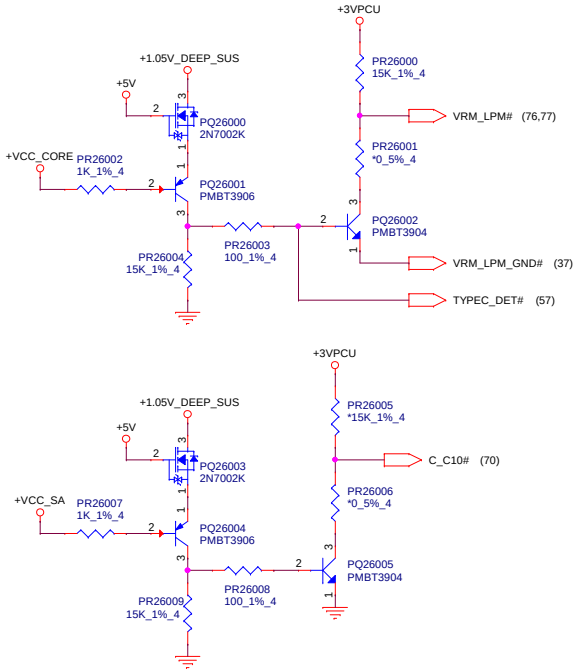
(5,12,13,14,15,16,20,21,22,23,27,33,34,35,36,40,41,42,43,44,45,47,48,49,50,51,54,59,62,63,66,69,75,82,85,94) +3V
(34,36,37,40,45,48,59,61,85,89,90) +5V
(13,24,41,70,75,76,77,79,87) +3V_ALW

NB5

XW2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	90 -- PWROK	1A

Date: Wednesday, May 30, 2018 Sheet 88 of 95

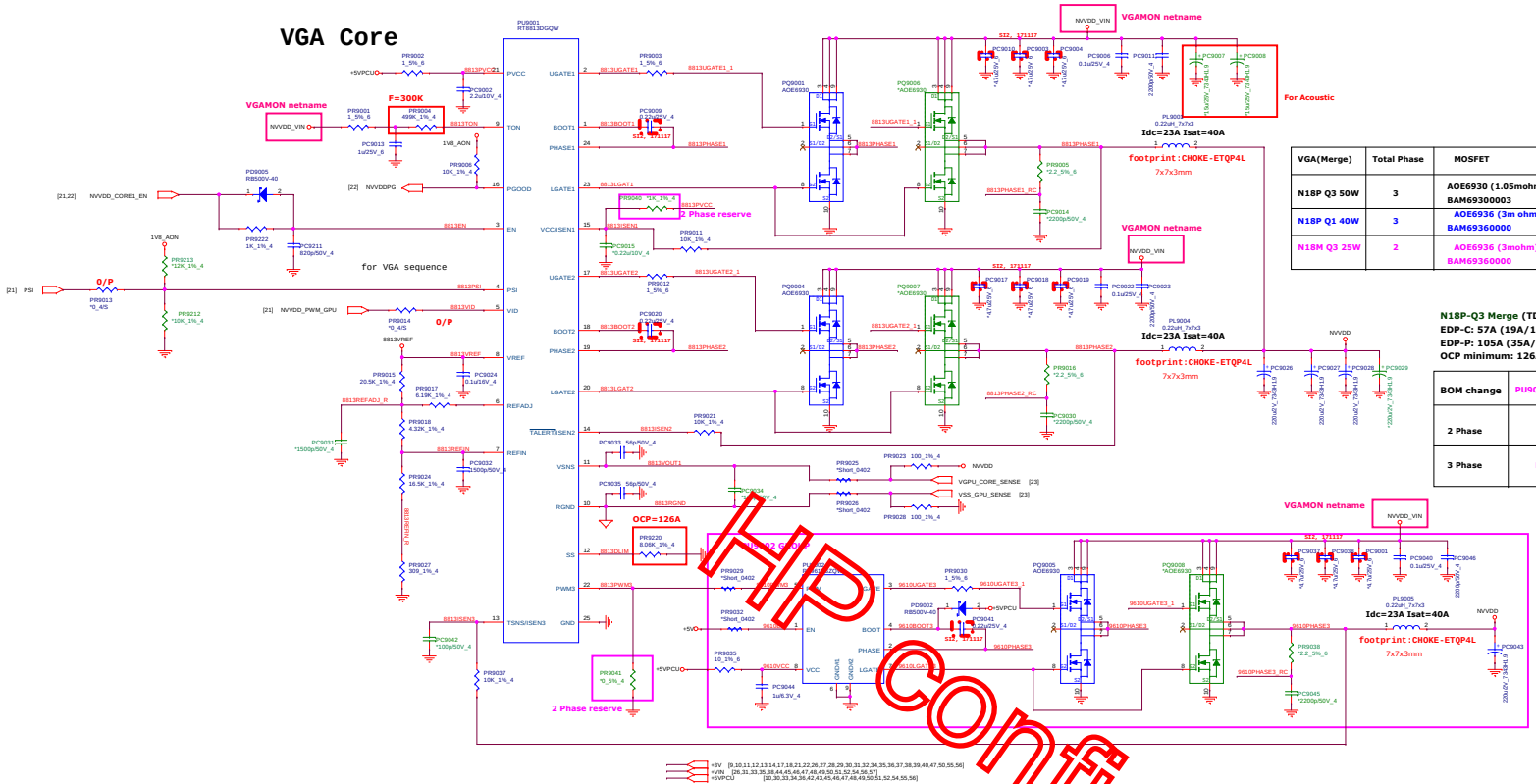


(5,12,13,14,15,16,20,21,22,23,27,33,34,35,36,40,41,42,43,44,45,47,48,49,50,51,54,59,62,63,66,69,75,82,85,88,94) +3V
(34,36,37,40,45,48,59,61,85,88,90) +5V
(13,24,41,70,75,76,77,79,87,88) +3V_ALW

NB5

XW2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	91 -- VRM_LPM#	1A
Date: Wednesday, May 30, 2018	Sheet 89 of 95	



VGA(Merge)	Total Phase	MOSFET	EDC SPEC	OCP setting	PR9220 OCP setting
N18P Q3 50W	3	AOE6930 (1.05mohm) BAM69300003	105A	126A	8.06K
N18P Q1 40W	3	AOE6936 (3m ohm) BAM69360000	81A	98A	12.7K
N18M Q3 25W	2	AOE6936 (3mohm) BAM69360000	64A	77A	14.7K

BOM change	PU9002 GROUP	PR9040	PR9011	PR9021	PR9037	PR9041
2 Phase	DNI	MOUNT	DNI	DNI	DNI	MOUNT
3 Phase	MOUNT	DNI	MOUNT	MOUNT	MOUNT	DNI

92

NVDDS

1. Ripple Current:
   Irip=14.35A
2. Ripple Voltage:
   ESR/3=9mohm/3=3 mohm
   Vrip=3m x 14.35A=43.05mV
3. MOSFET Spec:
   L-side MOSFET: FDPC5030
   Rds(ON)=3mohm (Vgs=4.5 V)
   I cont = 25A (T =25 ℃)
   I pulse=503A
4. Frequency:
   F=300KHz (PR9004=499k ohm)
5. OCP:
   N18P Q3 Merge
   Set = PR9220 to 8.06K
   Vrip= PR900P10uA-40mV=40.6mV
   Iocp=(Vtrip/Rdson) + Iripple/2
   = 38.67+7.17=45.8A(1 phase)
   Total OCP=42.8*3=137A (3 phase)

XW2
Quanta Computer Inc.
NB5
Size: D
Document Number: 92 -- NVVDD (RT8813D)
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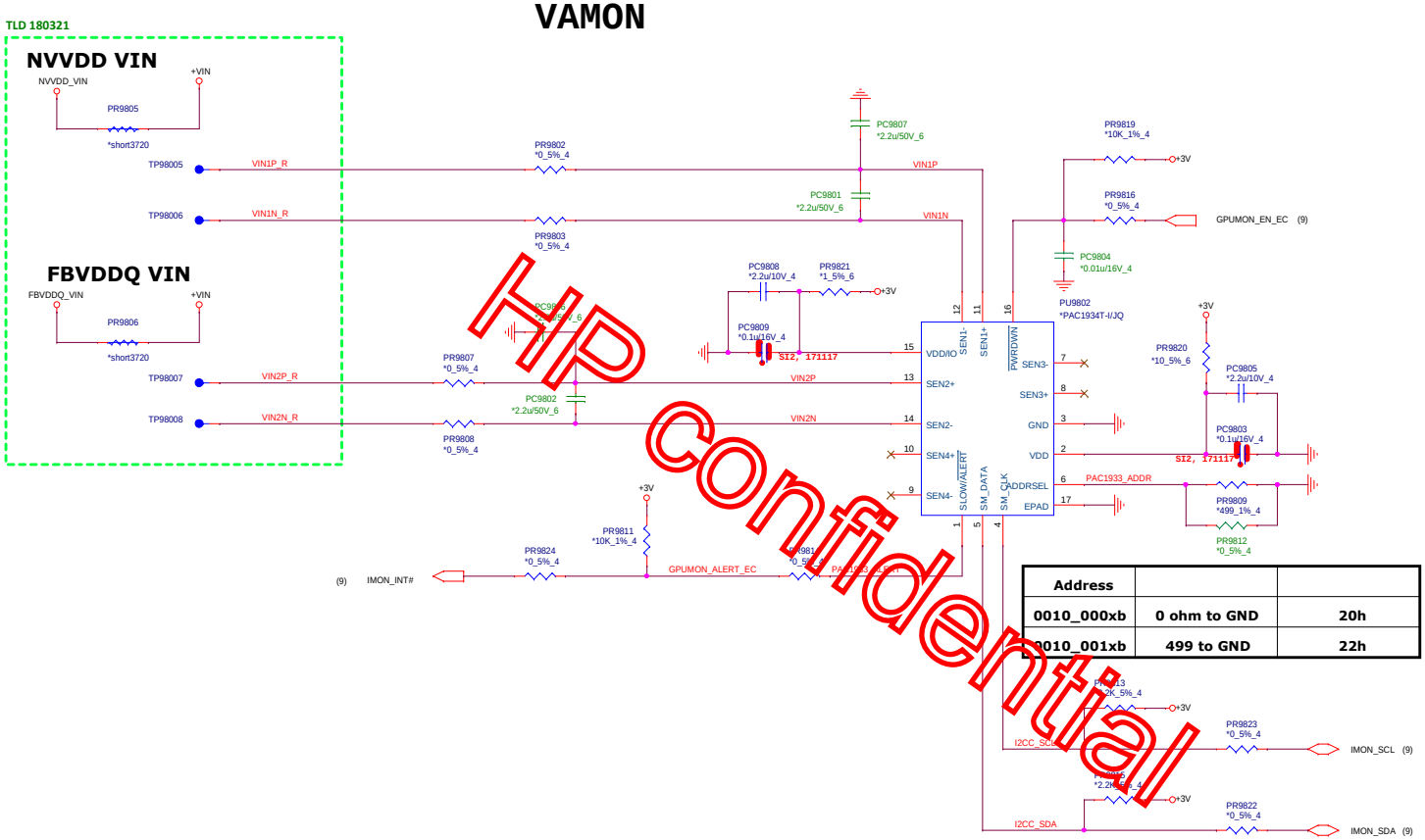
VAMON



Address		
0010_000xb	0 ohm to GND	20h
0010_001xb	499 to GND	22h

XW2
Quanta Computer Inc.
NB5

Size	Document Number	Rev
C	93 – VGAMON	1A

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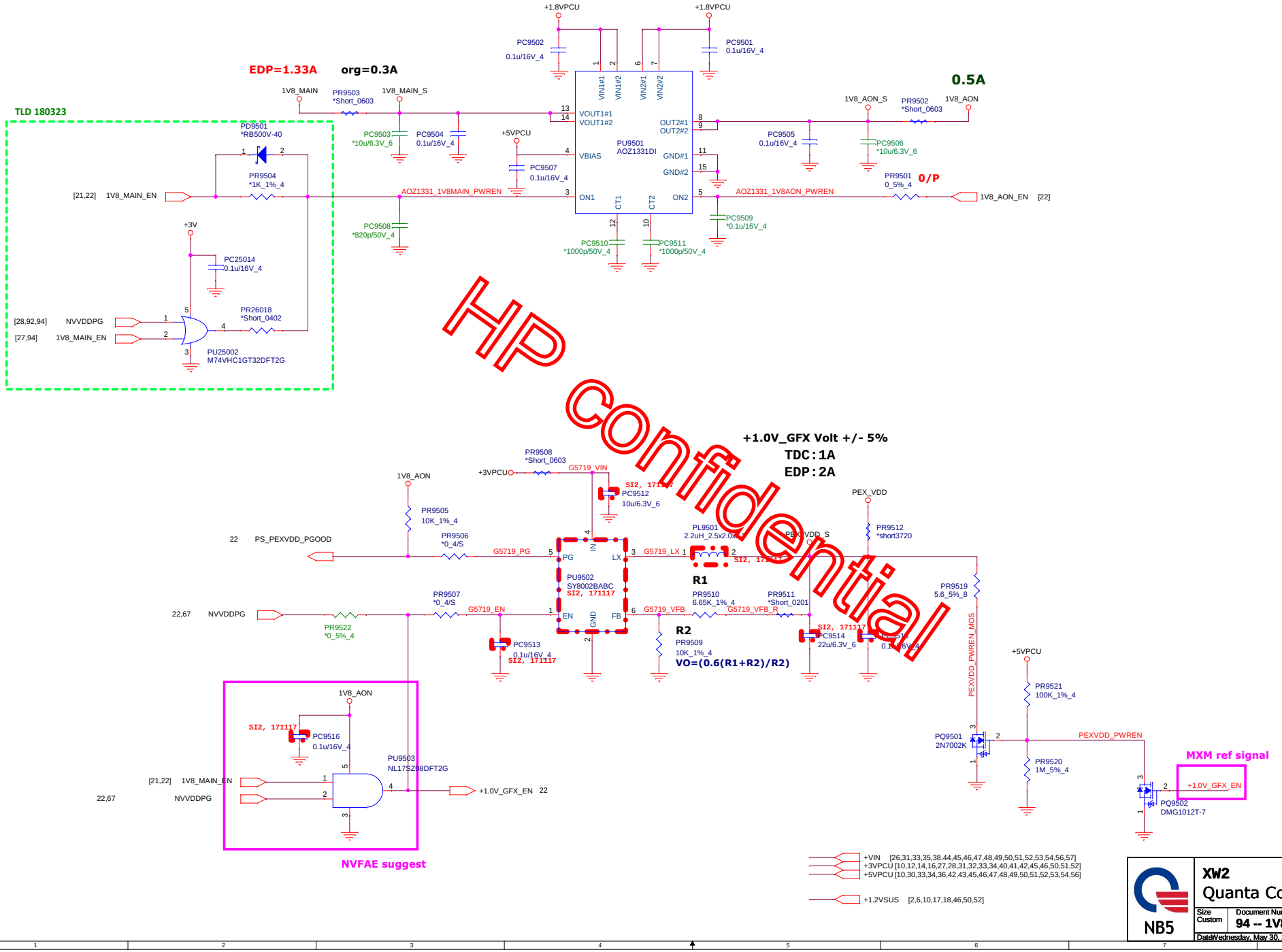
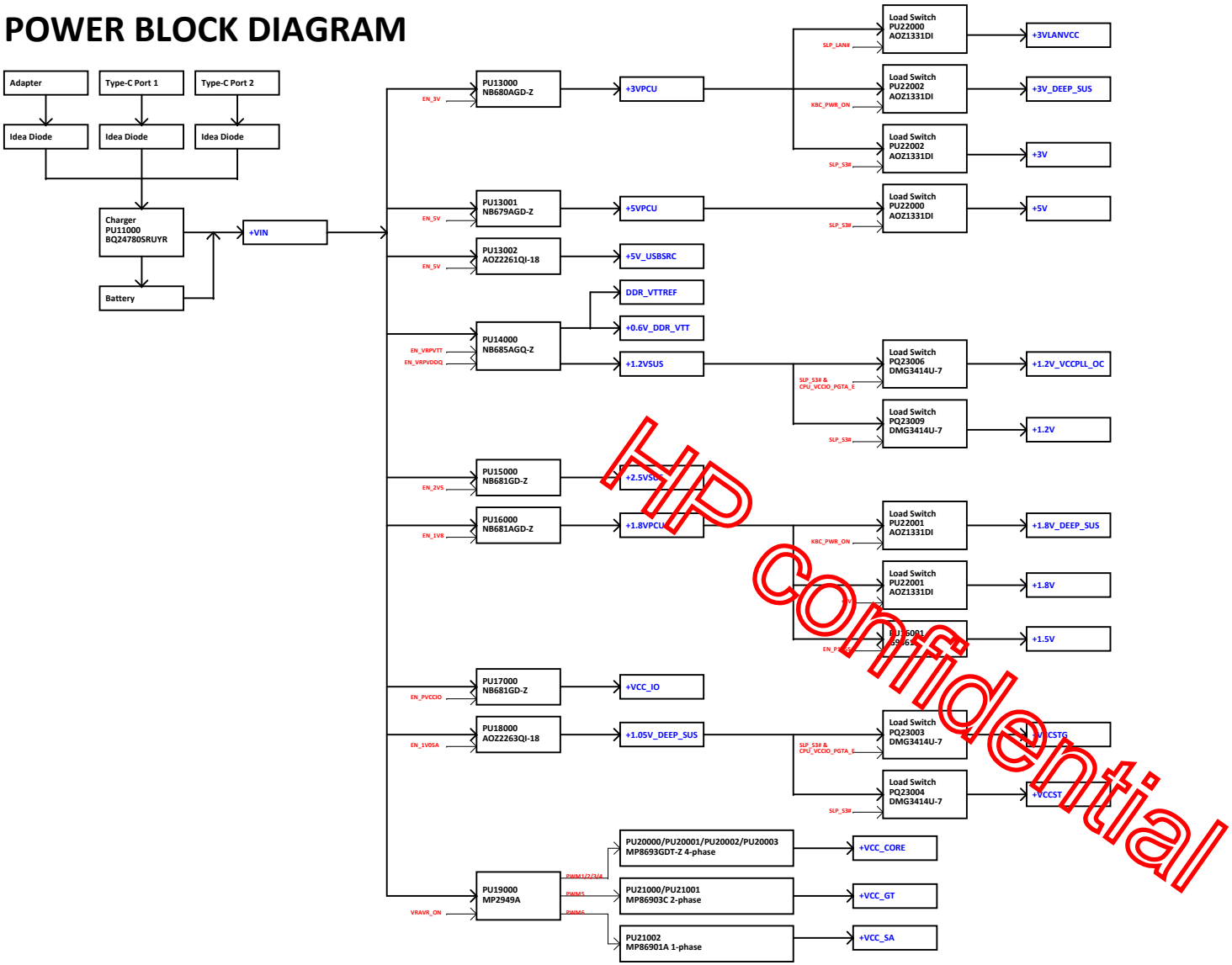
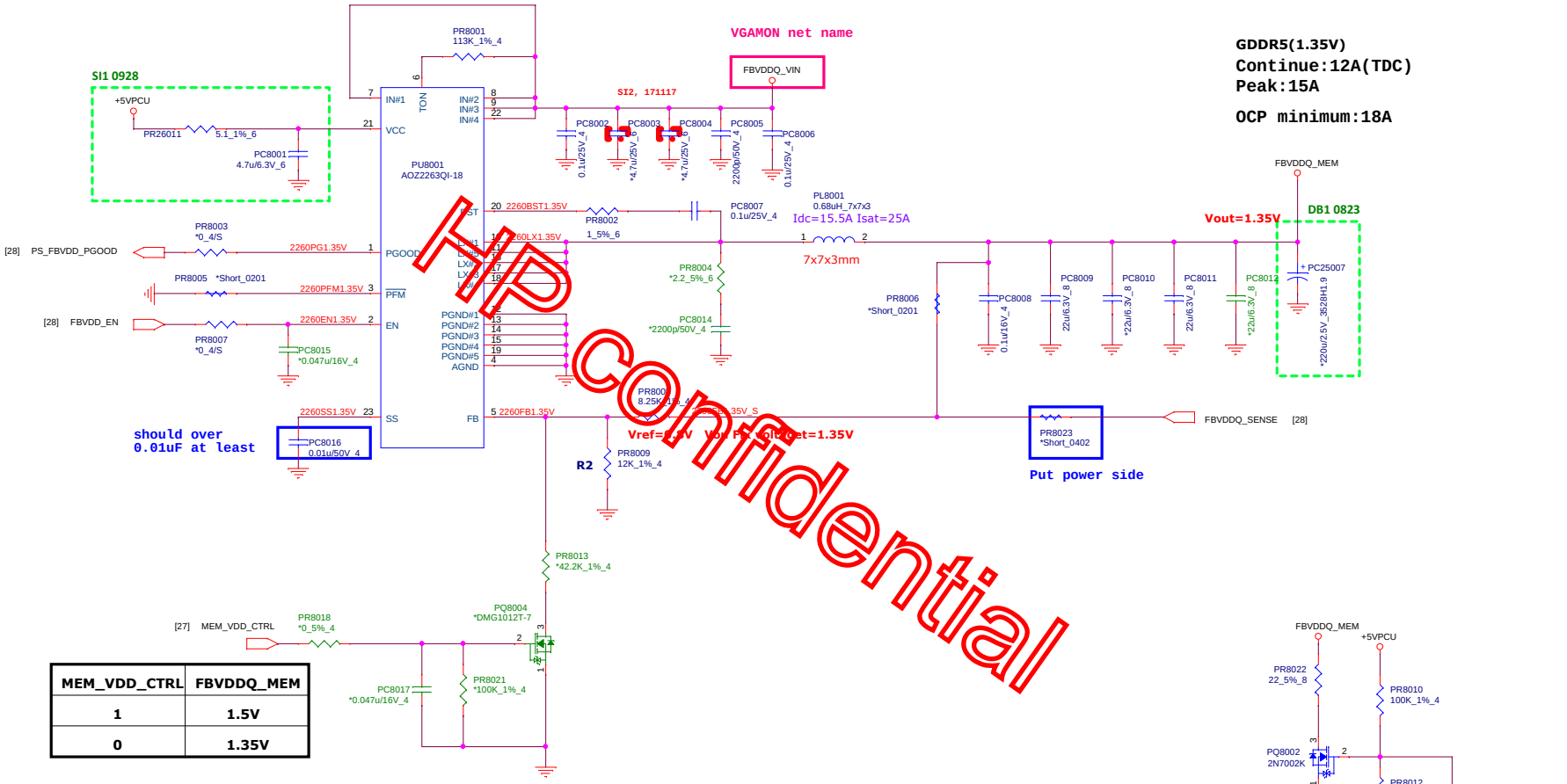


XW2		
Quanta Computer Inc.		
NB5	Size: Custom	Document Number: 94 -- 1V8_MAIN_AON/PEX_VDD
	Rev: 1A	
	Date: Wednesday, May 30, 2018	Sheet 94 of 96

POWER BLOCK DIAGRAM



XW2
Quanta Computer Inc.
NB5
Size: Custom | Document Number: 96 – Power Block Diagram | Rev: 1A
Date: Wednesday, May 30, 2018 | Sheet 94 of 96



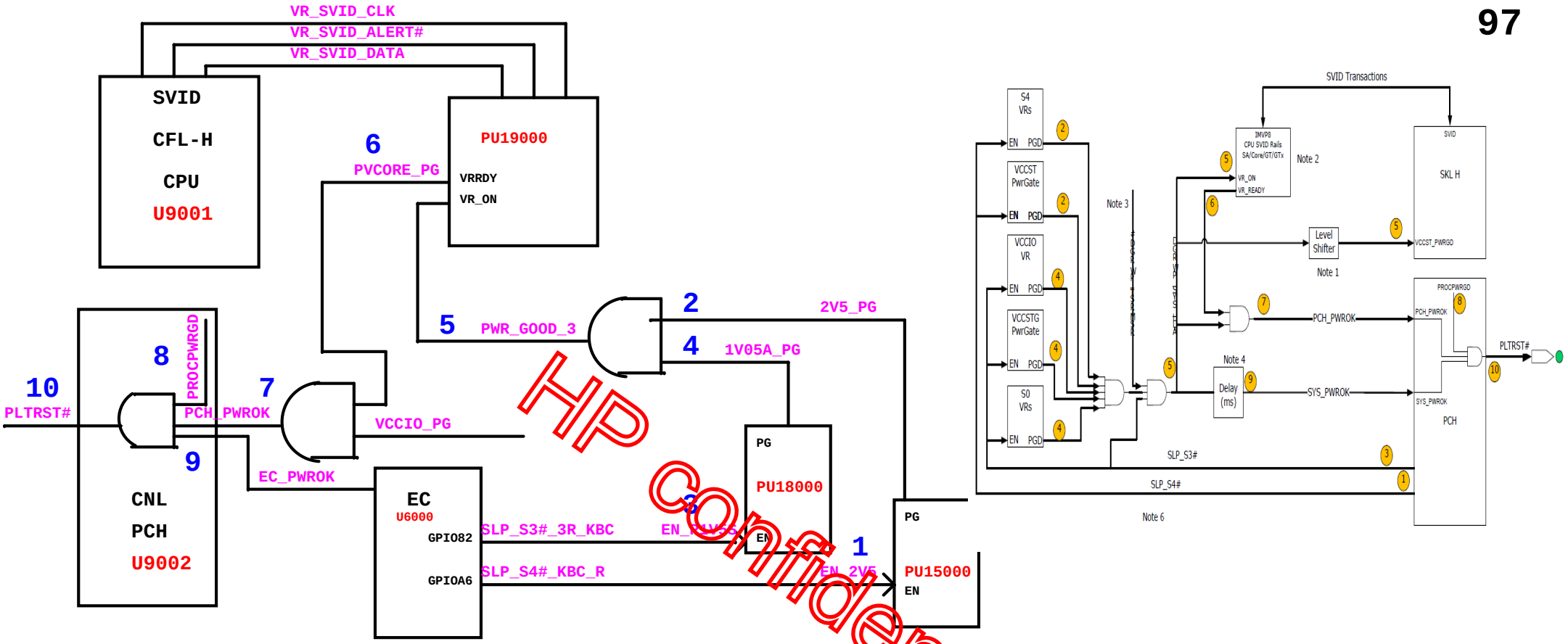
GDDR5(1.35V)
Continue:12A(TDC)
Peak:15A

OCP minimum:18A

MEM_VDD_CTRL	FBVDDQ_MEM
1	1.5V
0	1.35V

+5VPCU [38,41,58,78,81,83,85,87,88,90,92,94]
FBVDDQ_MEM [26,28,30,31]

XW2
Quanta Computer Inc.
NB5
Size: Custom
Document Number: 95 -- FBVDDQ_MEM(RT8816A)
Rev: 1A
Date: Wednesday, May 30, 2018
Sheet 95 of 97



NB5	XW2 Quanta Computer Inc.	
Size B	Document Number 97 -- Power Block Diagram	Rev 1A
Date: Wednesday, May 30, 2018	Sheet 95 of 95	