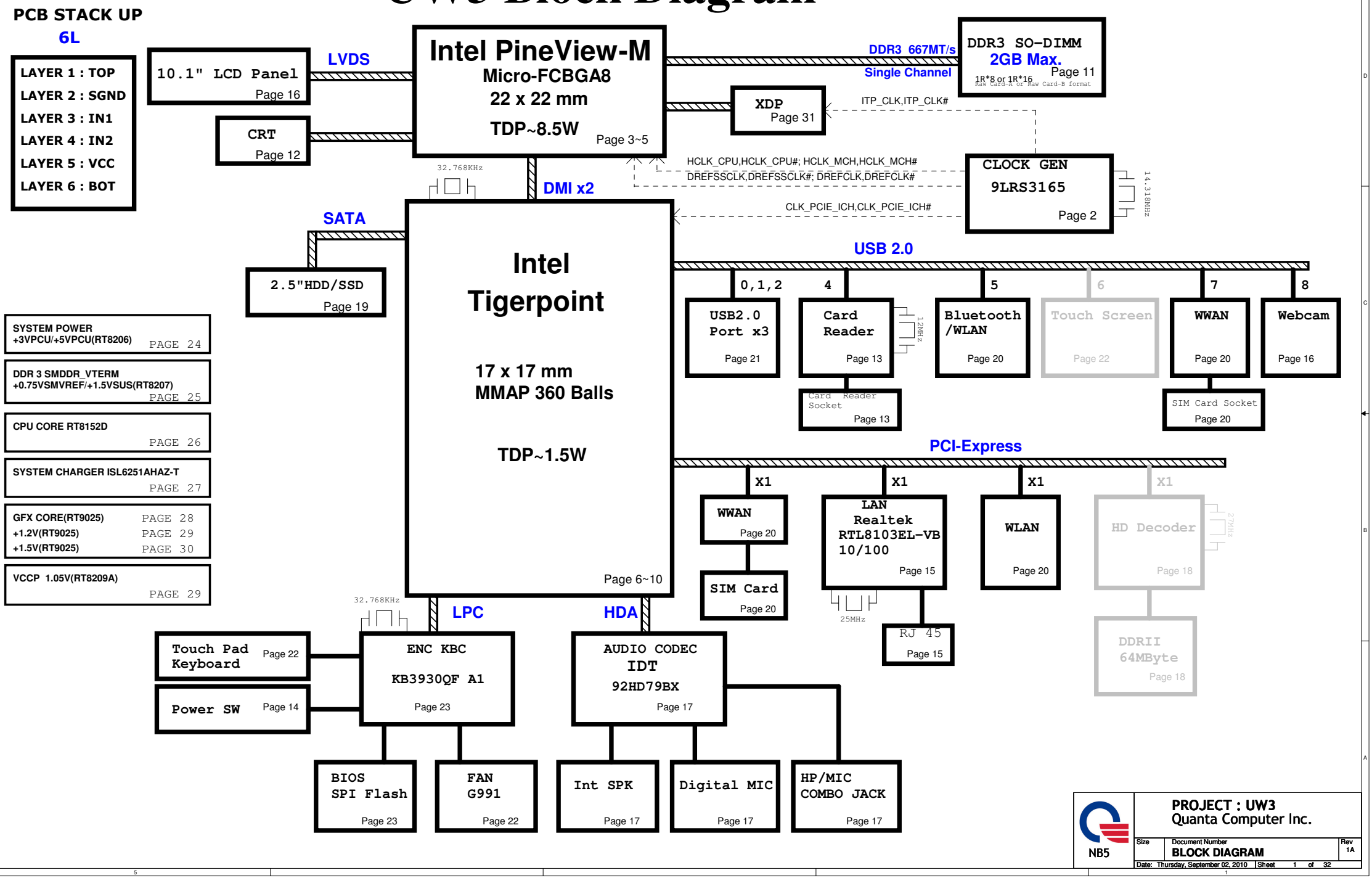
UW3 Block Diagram

01

PCB STACK UP

6L

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT



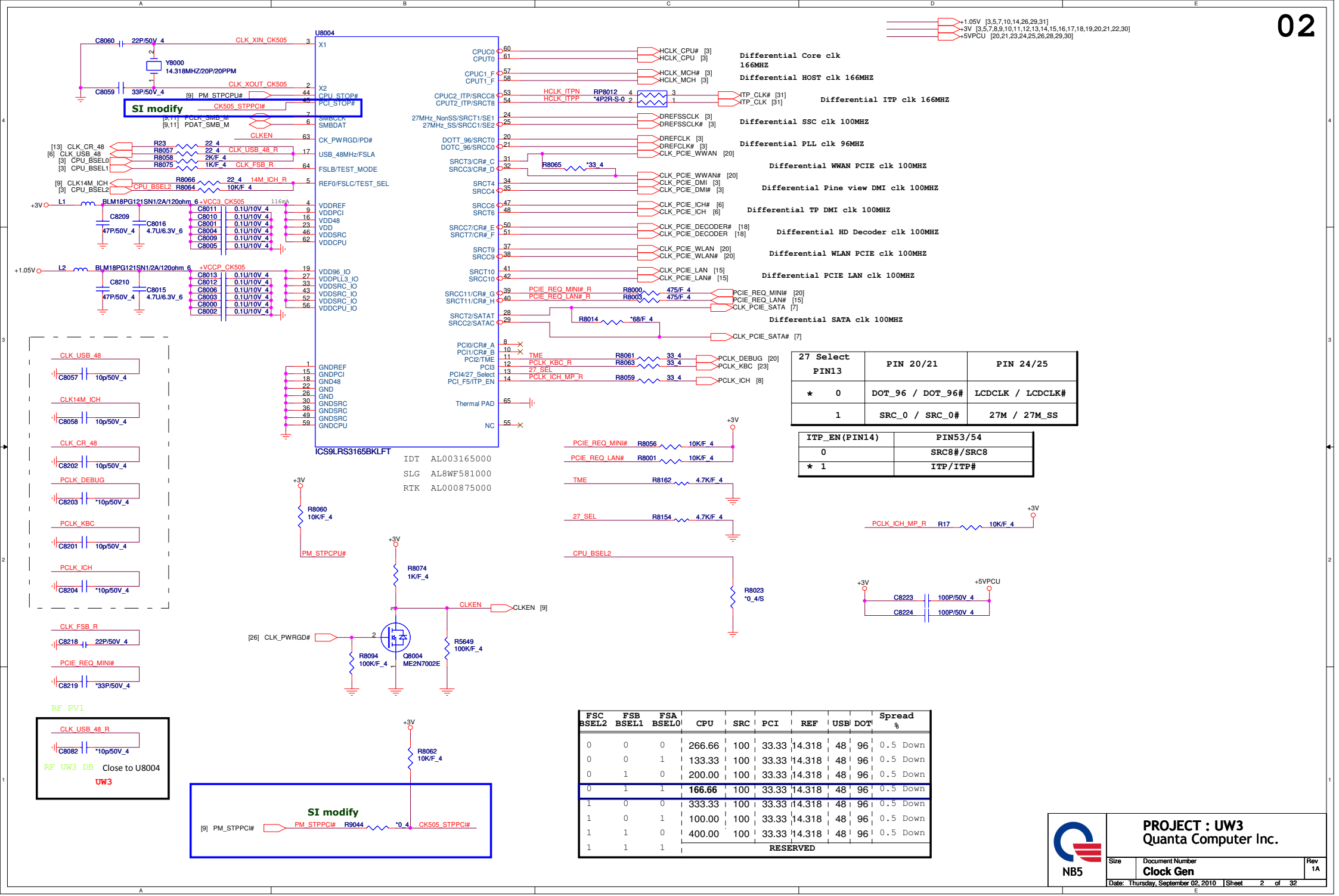
SYSTEM POWER +3VPCU/+5VPCU(RT8206)	PAGE 24
DDR 3 SMDDR_VTERM +0.75VSMVREF/+1.5VSUS(RT8207)	PAGE 25
CPU CORE RT8152D	PAGE 26
SYSTEM CHARGER ISL6251AHAZ-T	PAGE 27
GFX CORE(RT9025)	PAGE 28
+1.2V(RT9025)	PAGE 29
+1.5V(RT9025)	PAGE 30
VCCP 1.05V(RT8209A)	PAGE 29

NB5

PROJECT : UW3
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

Date: Thursday, September 02, 2010 | Sheet 1 of 32



27 Select PIN13	PIN 20/21	PIN 24/25
* 0	DOT_96 / DOT_96#	LCDCLK / LCDCLK#
1	SRC_0 / SRC_0#	27M / 27M_SS

ITP_EN(PIN14)	PIN53/54
0	SRC8#/SRC8
* 1	ITP/ITP#

FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB	DOT	Spread %
0	0	0	266.66	100	33.33	14.318	48	96	0.5 Down
0	0	1	133.33	100	33.33	14.318	48	96	0.5 Down
0	1	0	200.00	100	33.33	14.318	48	96	0.5 Down
0	1	1	166.66	100	33.33	14.318	48	96	0.5 Down
1	0	0	333.33	100	33.33	14.318	48	96	0.5 Down
1	0	1	100.00	100	33.33	14.318	48	96	0.5 Down
1	1	0	400.00	100	33.33	14.318	48	96	0.5 Down
1	1	1	RESERVED						

NB5

PROJECT : UW3
Quanta Computer Inc.

Size	Document Number	Rev
	Clock Gen	1A

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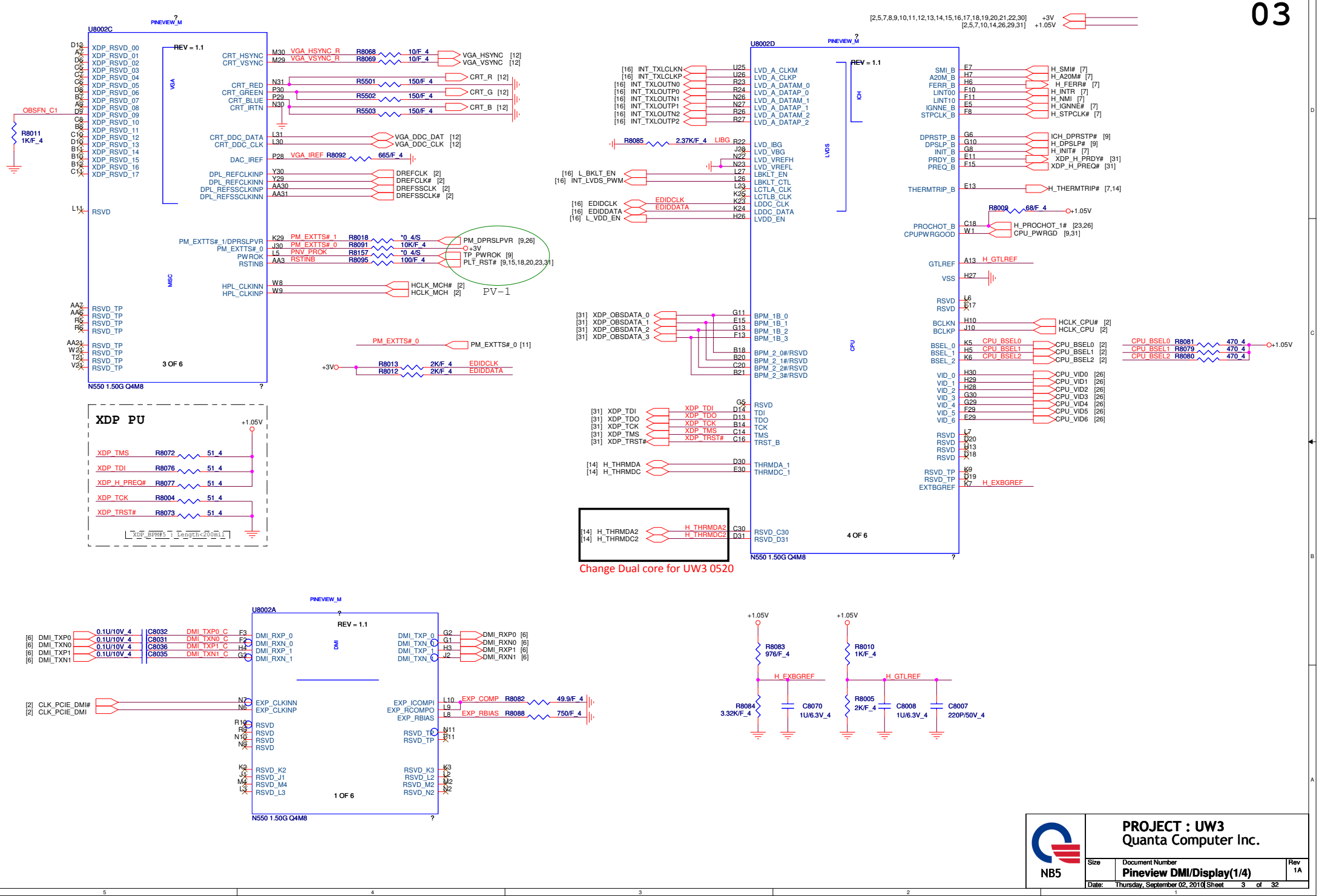

NB5	PROJECT : UW3 Quanta Computer Inc.	
	Size: Document Number: Pineview DMI/Display(1/4)	Rev: 1A
	Date: Thursday, September 02, 2010 Sheet 3 of 32	

+1.5VSUS [5,11,25,28,29,30]
+0.75VSMVREF [11,25]

U8002B
PINEVIEW_M
REV = 1.1

[11] M_A_A[14..0]
M_A_A0 AH19 DDR_A_MA_0
M_A_A1 AJ18 DDR_A_MA_1
M_A_A2 AK18 DDR_A_MA_2
M_A_A3 AK16 DDR_A_MA_3
M_A_A4 AJ14 DDR_A_MA_4
M_A_A5 AH14 DDR_A_MA_5
M_A_A6 AK14 DDR_A_MA_6
M_A_A7 AJ12 DDR_A_MA_7
M_A_A8 AH13 DDR_A_MA_8
M_A_A9 AK12 DDR_A_MA_9
M_A_A10 AK20 DDR_A_MA_10
M_A_A11 AH12 DDR_A_MA_11
M_A_A12 AJ11 DDR_A_MA_12
M_A_A13 AJ24 DDR_A_MA_13
M_A_A14 AJ10 DDR_A_MA_14

[11] M_A_WE#
[11] M_A_CAS#
[11] M_A_RAS#
M_A_WE# AK22 DDR_A_WEB
M_A_CAS# AJ22 DDR_A_CASB
M_A_RAS# AK21 DDR_A_RASB

[11] M_A_BS0
[11] M_A_BS1
[11] M_A_BS2
M_A_BS0 AJ20 DDR_A_BS_0
M_A_BS1 AH20 DDR_A_BS_1
M_A_BS2 AK11 DDR_A_BS_2

[11] M_CS#0
[11] M_CS#1
M_CS#0 AH22 DDR_A_CSB_0
M_CS#1 AK25 DDR_A_CSB_1
AJ21 DDR_A_CSB_2
AJ25 DDR_A_CSB_3

[11] M_CKE0
[11] M_CKE1
M_CKE0 AH10 DDR_A_CKE_0
M_CKE1 AH9 DDR_A_CKE_1
AK10 DDR_A_CKE_2
AJ8 DDR_A_CKE_3

[11] M_ODT0
[11] M_ODT1
M_ODT0 AK24 DDR_A_ODT_0
M_ODT1 AH26 DDR_A_ODT_1
AH24 DDR_A_ODT_2
AK23 DDR_A_ODT_3

[11] M_CLK0
[11] M_CLK#0
[11] M_CLK1
[11] M_CLK#1
M_CLK0 AG15 DDR_A_CK_0
M_CLK#0 AF15 DDR_A_CKB_0
M_CLK1 AD13 DDR_A_CK_1
M_CLK#1 AC13 DDR_A_CKB_1
AC15 DDR_A_CK_3
AD15 DDR_A_CKB_3
AF13 DDR_A_CK_4
AG13 DDR_A_CKB_4

AD17 RSVD_AD17
AC17 RSVD_AC17
AB15 RSVD_AB15
AB17 RSVD_AB17

[11] DDR3_DRAM_RST_N
DDR3_DRAM_RST_N AK8 DDR3_DRAMRSTB
DDR3_DRAM_PWROK AB4 DDR3_DRAM_PWROK

AB11 RSVD_TP
AB13 RSVD_TP
AL28 DDR_VREF
AK28 DDR_RPD
AJ26 DDR_RPU
AK29 RSVD

DDR_A_DQS_0 AD3 M_A_DQS0
DDR_A_DQSB_0 AD2 M_A_DQS#0
DDR_A_DM_0 AD4 M_A_DM0
DDR_A_DQ_0 AC4 M_A_DQ0
DDR_A_DQ_1 AC1 M_A_DQ1
DDR_A_DQ_2 AF4 M_A_DQ2
DDR_A_DQ_3 AG2 M_A_DQ3
DDR_A_DQ_4 AB2 M_A_DQ4
DDR_A_DQ_5 AB3 M_A_DQ5
DDR_A_DQ_6 AE2 M_A_DQ6
DDR_A_DQ_7 AE3 M_A_DQ7
DDR_A_DQS_1 AB8 M_A_DQS1
DDR_A_DQSB_1 AD7 M_A_DQS#1
DDR_A_DM_1 AA9 M_A_DM1
DDR_A_DQ_8 AB6 M_A_DQ8
DDR_A_DQ_9 AB7 M_A_DQ9
DDR_A_DQ_10 AE5 M_A_DQ10
DDR_A_DQ_11 AG5 M_A_DQ11
DDR_A_DQ_12 AA5 M_A_DQ12
DDR_A_DQ_13 AB5 M_A_DQ13
DDR_A_DQ_14 AB9 M_A_DQ14
DDR_A_DQ_15 AD6 M_A_DQ15
DDR_A_DQS_2 AD8 M_A_DQS2
DDR_A_DQSB_2 AD10 M_A_DQS#2
DDR_A_DM_2 AE8 M_A_DM2
DDR_A_DQ_16 AG8 M_A_DQ16
DDR_A_DQ_17 AG7 M_A_DQ17
DDR_A_DQ_18 AF10 M_A_DQ18
DDR_A_DQ_19 AG11 M_A_DQ19
DDR_A_DQ_20 AF7 M_A_DQ20
DDR_A_DQ_21 AF8 M_A_DQ21
DDR_A_DQ_22 AD11 M_A_DQ22
DDR_A_DQ_23 AE10 M_A_DQ23
DDR_A_DQS_3 AK5 M_A_DQS3
DDR_A_DQSB_3 AK3 M_A_DQS#3
DDR_A_DM_3 AJ3 M_A_DM3
DDR_A_DQ_24 AH1 M_A_DQ24
DDR_A_DQ_25 AJ2 M_A_DQ25
DDR_A_DQ_26 AK6 M_A_DQ26
DDR_A_DQ_27 AJ7 M_A_DQ27
DDR_A_DQ_28 AF3 M_A_DQ28
DDR_A_DQ_29 AH2 M_A_DQ29
DDR_A_DQ_30 AL5 M_A_DQ30
DDR_A_DQ_31 AJ6 M_A_DQ31
DDR_A_DQS_4 AG22 M_A_DQS4
DDR_A_DQSB_4 AG21 M_A_DQS#4
DDR_A_DM_4 AD19 M_A_DM4
DDR_A_DQ_32 AE19 M_A_DQ32
DDR_A_DQ_33 AG19 M_A_DQ33
DDR_A_DQ_34 AF22 M_A_DQ34
DDR_A_DQ_35 AD22 M_A_DQ35
DDR_A_DQ_36 AG17 M_A_DQ36
DDR_A_DQ_37 AF19 M_A_DQ37
DDR_A_DQ_38 AE21 M_A_DQ38
DDR_A_DQ_39 AD21 M_A_DQ39
DDR_A_DQS_5 AE26 M_A_DQS5
DDR_A_DQSB_5 AG27 M_A_DQS#5
DDR_A_DM_5 AJ27 M_A_DM5
DDR_A_DQ_40 AE24 M_A_DQ40
DDR_A_DQ_41 AG25 M_A_DQ41
DDR_A_DQ_42 AD25 M_A_DQ42
DDR_A_DQ_43 AD24 M_A_DQ43
DDR_A_DQ_44 AC22 M_A_DQ44
DDR_A_DQ_45 AG24 M_A_DQ45
DDR_A_DQ_46 AD27 M_A_DQ46
DDR_A_DQ_47 AE27 M_A_DQ47
DDR_A_DQS_6 AE30 M_A_DQS6
DDR_A_DQSB_6 AF29 M_A_DQS#6
DDR_A_DM_6 AF30 M_A_DM6
DDR_A_DQ_48 AG31 M_A_DQ48
DDR_A_DQ_49 AG30 M_A_DQ49
DDR_A_DQ_50 AD30 M_A_DQ50
DDR_A_DQ_51 AD29 M_A_DQ51
DDR_A_DQ_52 AJ30 M_A_DQ52
DDR_A_DQ_53 AJ29 M_A_DQ53
DDR_A_DQ_54 AE29 M_A_DQ54
DDR_A_DQ_55 AD28 M_A_DQ55
DDR_A_DQS_7 AB27 M_A_DQS7
DDR_A_DQSB_7 AA27 M_A_DQS#7
DDR_A_DM_7 AB26 M_A_DM7
DDR_A_DQ_56 AA24 M_A_DQ56
DDR_A_DQ_57 AB25 M_A_DQ57
DDR_A_DQ_58 W24 M_A_DQ58
DDR_A_DQ_59 W22 M_A_DQ59
DDR_A_DQ_60 AB24 M_A_DQ60
DDR_A_DQ_61 AB23 M_A_DQ61
DDR_A_DQ_62 AA23 M_A_DQ62
DDR_A_DQ_63 W27 M_A_DQ63

DDR_A
2 OF 6
N550 1.50G Q4M8

M_A_DQ[63..0] [11]
M_A_DM[7..0] [11]
M_A_DQS[7..0] [11]
M_A_DQS#[7..0] [11]

+1.5VSUS
R8039 1K/F_4
+0.75VSMVREF R8100 *0_4 +DDR_VREF
R8037 1K/F_4

+1.5VSUS
R8110 10K/F_4

C8033 0.01U/25V_4
+DDR_VREF
R8036 80.6/F_4 SM_RCOMP
R8040 80.6/F_4 SM_RCOMP#
+1.5VSUS
C8034 0.01U/25V_4

+5V_S5
+1.5VSUS
C8069 0.1U/10V_4
R8052 1K/F_4
R8050 1K/F_4
DDR3_DRAM_PWROK
R8051
DDR_PG
DDR_PG [25]
*0_4
MMBT3904 Q8008
DDR3_DRAM_PWROK
R8038 *0_4
[9,23] SUSC#
SUSC# R8053 1K/F_4
MMBT3904 Q8009
C436 1U/6.3V_4

Intel CRB

NB5
PROJECT : UW3
Quanta Computer Inc.
Size
Document Number
Pineview DDR(2/4)
Rev 1A
Date: Thursday, September 02, 2010
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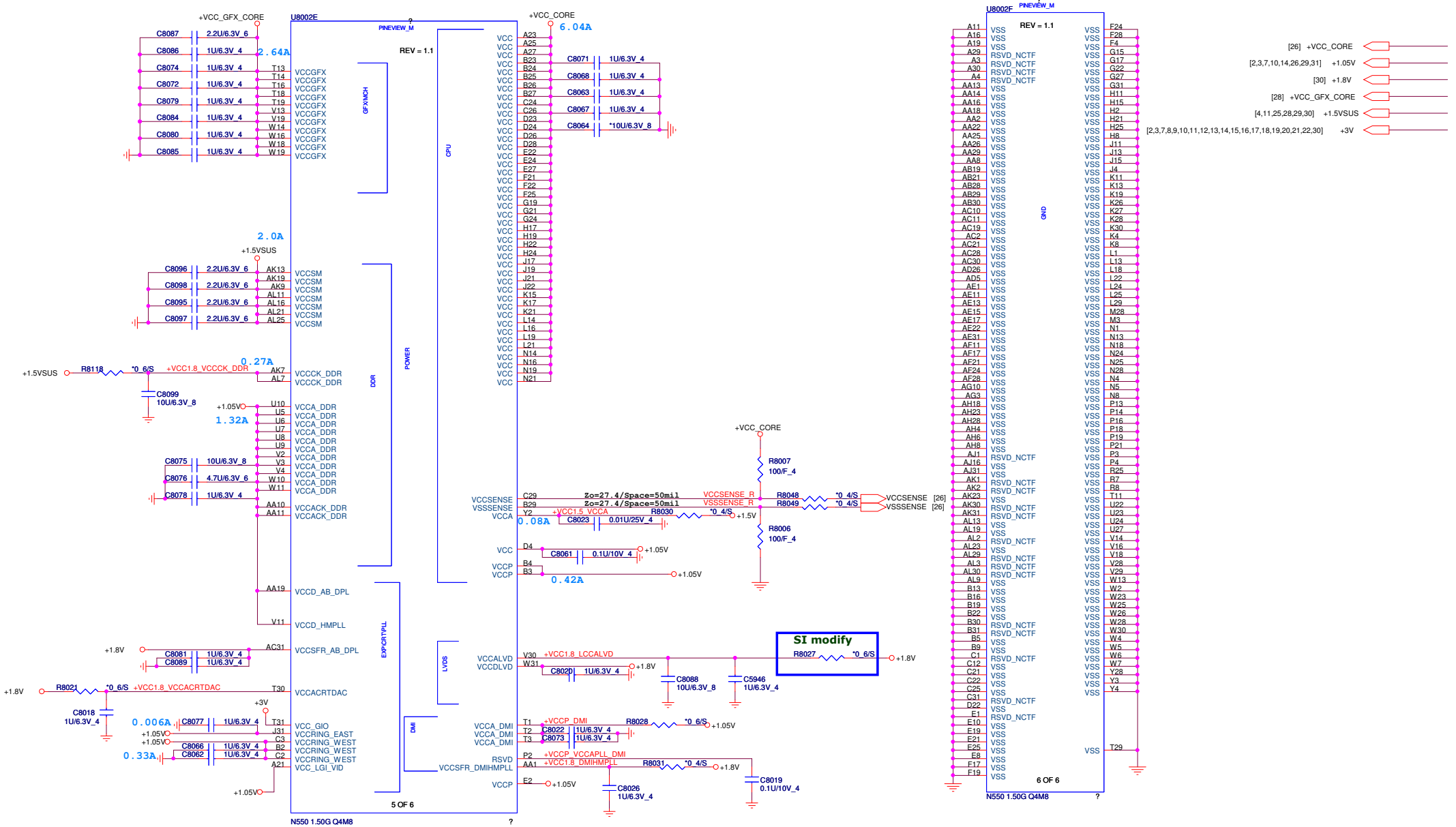
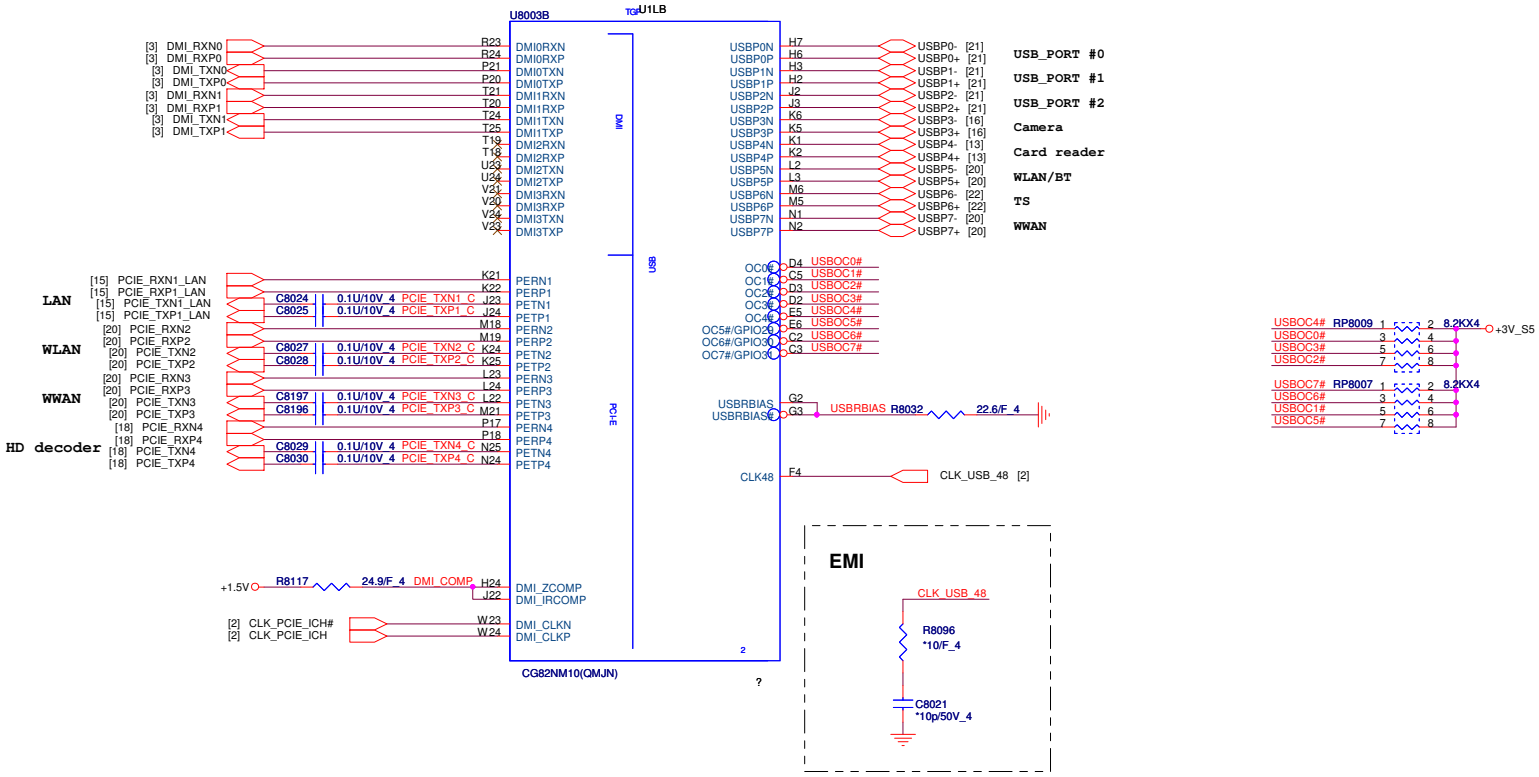


NB5	PROJECT : UW3 Quanta Computer Inc.	
Size	Document Number Pineview Power(3/4)	Rev 1A
Date: Thursday, September 02, 2010	Sheet 5 of 32	

[5,10,18,20,30] +1.5V

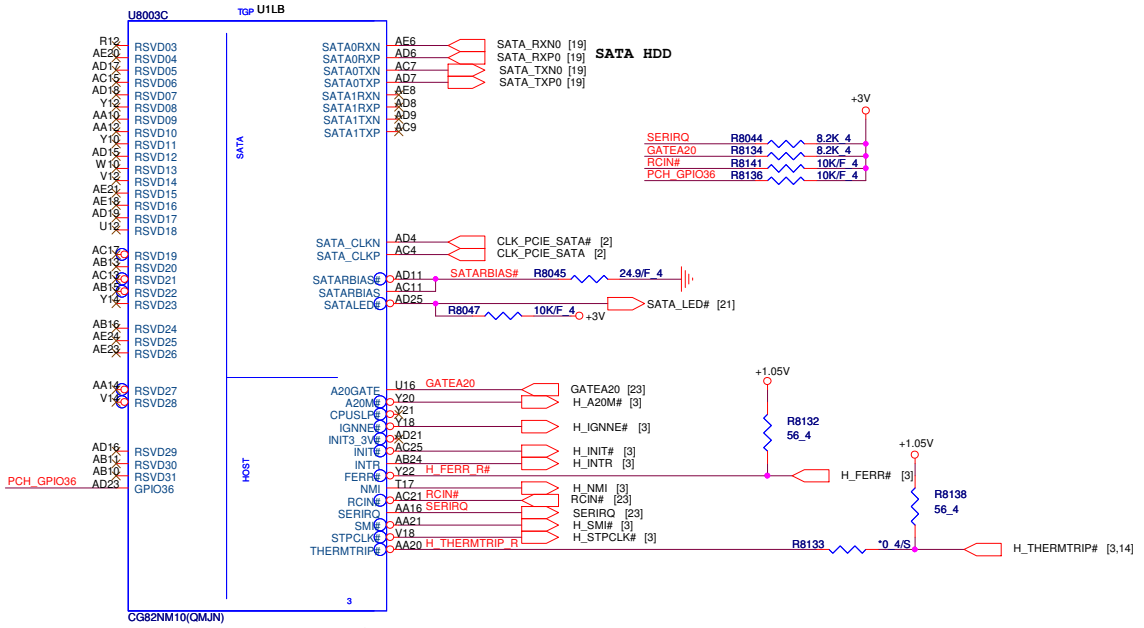
[9,10,30] +3V_S5



PROJECT : UW3	
Quanta Computer Inc.	
NB5	Size: — Document Number: TigerPoint DMI/PCIE(1/6) Rev: 1A
Date: Thursday, September 02, 2010	Sheet 6 of 32

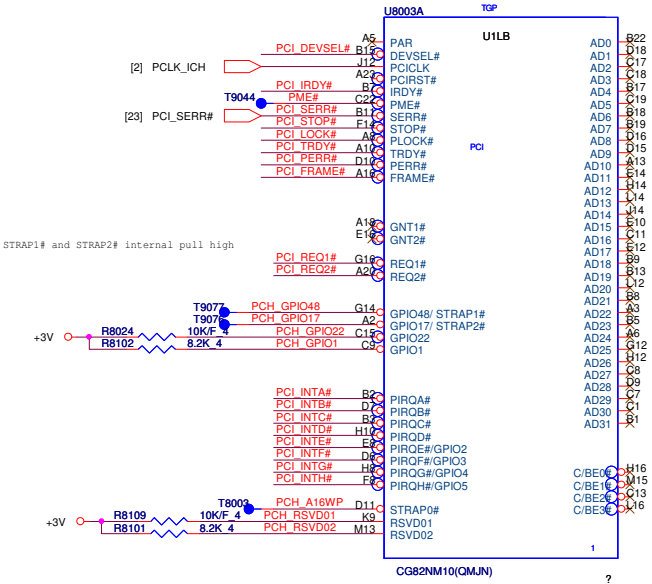
+3V [2,3,5,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,30]

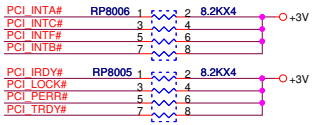
+1.05V [2,3,5,10,14,26,29,31]

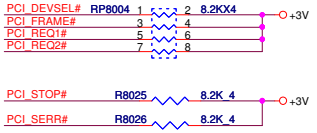


NB5	PROJECT : UW3 Quanta Computer Inc.	
	Size: — Document Number: TigerPoint Sata/Host(2/6)	Rev: 1A
	Date: Thursday, September 02, 2010 Sheet 7 of 32	

[2,3,5,7,9,10,11,12,13,14,15,16,17,18,19,20,21,22,30] +3V







ICH Boot BIOS select

PCH_GPIO17 (INT PU)	PCH_GPIO48 (INT PU)	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC (Default)

A16 SWAP Override strap

PCH_A16WP (INT PU)	**Low = A16 swap override enabled** **High = Default**

IRQ	Description
PIRQA	USB UHCI Controller #1, #4
PIRQB	AC'97 Codec; option for SMBUS
PIRQC	USB UH Controller #3; SATA/IDE Native Mode
PIRQD	USB UHCI Controller #2
PIRQE	Internal LAN; Option for SCI, TCO, HPET#0,1,2
PIRQF	Option for SCI, TCO, HPET#0,1,2
PIRQG	Option for SCI, TCO, HPET#0,1,2
PIRQH	USB EHCI Controller; Option for SCI, TCO, HPET#0,1,2

PCI_GNT#2	Internal PU Should not be PD

NB5

PROJECT : UW3
Quanta Computer Inc.

Size	Document Number	Rev
	TigerPoint PCI(3/6)	1A

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[14,16,20,21,22,23,24,26,27,30] +3VPCU
[2,3,5,7,8,10,11,12,13,14,15,16,17,18,19,20,21,22,30] +3V
[6,10,30] +3V_S5

EMI

CLK14M_ICH R8041 22_4 EMI-14M C8037 10P/50V_4

ACZ_SDOUT
ACZ_BITCLK
C8206 *10p/50V_4
C8205 10p/50V_4

ACZ_RST#
ACZ_SYNC
C8212 *10p/50V_4
C8213 *10p/50V_4

RTC

C8118 15p/50V_4
Y8999 32.768KHZ
C8113 15p/50V_4
R8129 10M_4

+VCCRTC
+3VPCU
D8999 RB500V-40
C8130 1U/6.3V_4
D8004 RB500V-40
R8151 20K/F_4
R8142 1K/F_4
R8150 1M_4
C8129 1U/6.3V_4
J8999 *SHORTPAD
SM_INTRUDER#

DB-8
BT8999 BAT_CONN

U8003D CG82NM10(QMJN)

T8999 LDRQ1#
T8017 LDRQ0#

[20,23] LAD0
[20,23] LAD1
[20,23] LAD2
[20,23] LAD3
[20,23] LFRAME#

[17] ACZ_BITCLK
[17] ACZ_RST#
[17] ACZ_SDIN0
R8125 33_4 ACZ_BITCLK_R
R8033 33_4 ACZ_RST#_R

[17] ACZ_SDOUT
[17] ACZ_SYNC
[2] CLK14M_ICH
R8035 33_4 ACZ_SDOUT_R
R8034 33_4 ACZ_SYNC_R
CLK14M_ICH

LAN_RST#

RTC_X1
RTC_X2
RTC_RST#

SMBALERT#
SMB0_CLK
SMB0_DATA
SMB_LINK_ALERT#
SMLINK0
SMLINK1

T8009 SPI_MISO
T8008 SPI_MISI
T8013 SPI_CS#
T8014 SPI_CLK
T8015 SPI_ARB

LDRQ1#/GPIO23
LAD0/FWH0
LAD1/FWH1
LAD2/FWH2
LAD3/FWH3
LDRQ0#
LFRAME#
LPC

HDA_BIT_CLK
HDA_RST#
HDA_SDI0
HDA_SDIN1
HDA_SDIN2
HDA_SDOUT
HDA_SYNC
CLK14
AUDIO

EE_CS
EE_DIN
EE_DOUT
EE_SHCLK
EPROM

LAN_CLK
LANR_STSYNC
LAN_RST#
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
LAN

RTCX1
RTCX2
RTCRST#
RTC

SMBALERT#/GPIO11
SMBCLK
SMBDATA
SMLALERT#
SMLINK0
SMLINK1
SMB

SPI_MISO
SPI_MOSI
SPI_CS#
SPI_CLK
SPI_ARB
SPI

U1LB

BM_BUSY#/GPIO0
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
DPRSLPVR
STP_PCI#
STP_CPU#
GPIO24
GPIO25
GPIO26
GPIO27
GPIO28
CLKRUN#
GPIO33
GPIO34
GPIO38
GPIO39
CPUPWRGD/GPIO49
THRMC
VRMPWRGD
MCH_SYNC#
PWRBTN#
RI#
SUS_STAT#/LPCPD#
SUSCLK
SYS_RESET#
PLTRST#
WAKE#
INTRUDER#
PWROK
RSMRST#
INTVRMEN
SPKR
SLP_S3#
SLP_S4#
SLP_S5#
BATLOW#
DPRSTP#
DPSLP#
RSVD31
MISC

BM_BUSY#
BOARD ID0
BOARD ID1
KBSMI# [23]
SCI# [23]
WWAN_OFF# [20]
PCH_GPIO12
PCH_GPIO13
PCH_GPIO14
PCH_GPIO15
PM_DPRSLPVR [3,26]
PM_STPPCI# [2]
PM_STPCPU# [2]
DMI_AC_ENABLE
CLKRUN# [23]
BOARD ID2
RF_OFF# [20]
PCIE_WWAN_DET# [20]
BT_COMBO_EN# [20]
1K/F_4 R9020
CPU_PWRGD [3,31]
TP_THRM# R8214 *0_4/S
VRMPWRGD R8218 *0_4/S
PM_THRM# [14]
CLKEN [2]
MCH_SYNC#
DNBSWON# [23]
ICH_RI#
SUS_STAT#
T8011 SUSCLK
T8016 SUSCLK
SYS_RST# [31]
PLTRSTB# [3,15,18,20,23,31]
PCIE_LAN_WAKE# [15,20]
SM_INTRUDER#
TP_PWROK
RSMRST# [23]
ICH_INTVRMEN
SPKR_L
SPKR [17]
SUSB# [23]
SUSC# [4,23]
PM_BATLOW#
ICH_DPRSTP# [3]
H_DPSLP# [3]

integrated pull-up of 18 k - 42 k .check list 0.7

+3V_S5
DNBSWON# R8111 *10K/F_4
KBSMI# R8123 8.2K_4
SYS_RST# R8112 10K/F_4
SMBALERT# R8122 10K/F_4
SMB_LINK_ALERT# R127 10K/F_4
PM_BATLOW# R8158 8.2K_4
PCIE_LAN_WAKE# R8159 10K/F_4
SMLINK1 R8043 10K/F_4
SMLINK0 R8098 10K/F_4
SMB0_CLK R8106 2K/F_4
SMB0_DATA R8105 2K/F_4
WWAN_OFF# R8119 10K/F_4
PCH_GPIO12 R9028 8.2K_4
PCH_GPIO13 R8160 8.2K_4
PCH_GPIO14 R8126 10K/F_4
PCH_GPIO15 R8161 8.2K_4
ICH_RI# R8135 10K/F_4
SCI# R9027 8.2K_4

+3V
CLKRUN# R8163 8.2K_4
TP_THRM# R8181 10K/F_4
MCH_SYNC# R8046 1K/F_4
BM_BUSY# R8182 10K/F_4

PLTRSTB# R8029 100K/F_4
LAN_RST# R8165 8.2K_4
TP_PWROK R8211 10K/F_4
RSMRST# R8212 10K/F_4
10-k pull-down to GND check list 0.7

INTVRMEN	
Enable (default)	1
Disable	0

ICH_INTVRMEN R8042 332K/F_4 +VCCRTC

[23] IMVP_PWRGD_EC R9037 *0_4
[23,26] IMVP_PWRGD
[14,16,23] ECPWROK
U8013 TC7SH08FU
TP_PWROK
TP_PWROK [3]
PV-1

SUSCLK SUSCLK [3]

+3V R8223 8.2K_4 BOARD ID0 R8224 *8.2K_4
R8225 8.2K_4 BOARD ID1 R8226 *8.2K_4
R8227 8.2K_4 BOARD ID2 R8228 *8.2K_4

Board ID	ID0	ID1	ID2
	0	0	0
	1	0	0
	0	1	0
	1	1	0

Q8005 ME2N7002E
SMB0_CLK
R8099 10K/F_4 +3V
PCLK_SMB_M [2,11]

Q9000 ME2N7002E
SMB0_DATA
R8097 10K/F_4 +3V
PDAT_SMB_M [2,11]

GPIO25 This signal has a weak internal pull-up.

If the signal is sampled high, the DMI interface is strapped to operate in DC coupled mode (No coupling capacitors are required on DMI differential pairs). If the signal is sampled low, the DMI interface is strapped to operate in AC coupled mode (Coupling capacitors are required on DMI differential pairs). NOTE: Board designer must ensure that DMI implementation matches the strap selection.

DMI_AC_ENABLE R8108 1K/F_4

ACZ_SDOUT (INT PD)	ACZ_SYNC (INT PD)	Description
0	0	★ 4 x 1s
1	0	Reserved
0	1	Reserved
1	1	1 x 4s(1 port/4 lanes)

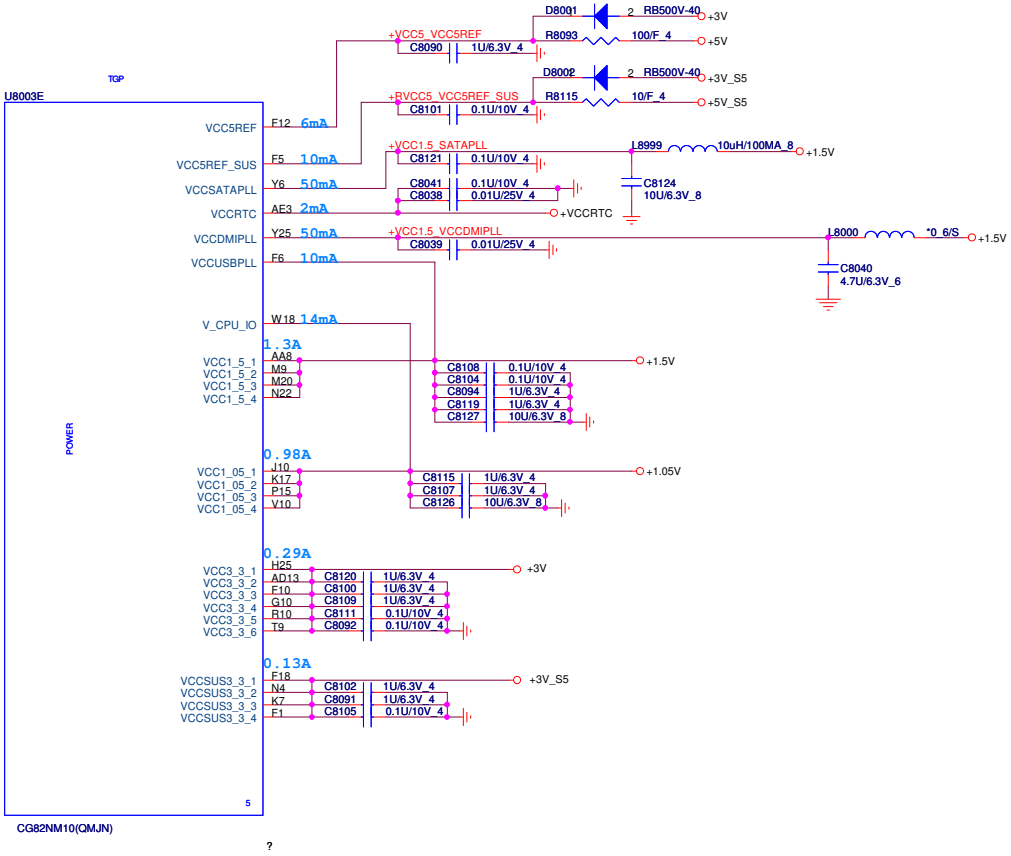
NB5

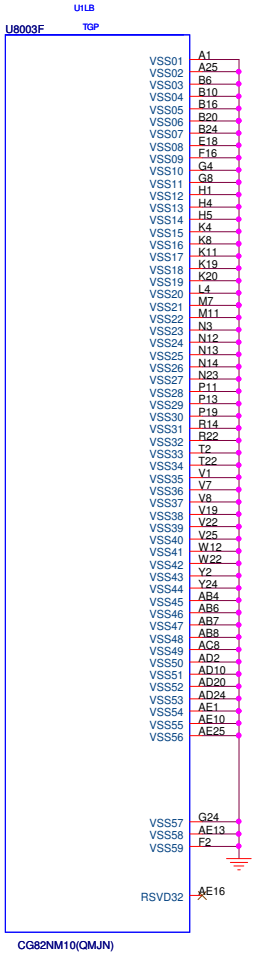
PROJECT : UW3
Quanta Computer Inc.

Size	Document Number	Rev
	TigerPoint GPIO(4/6)	1A

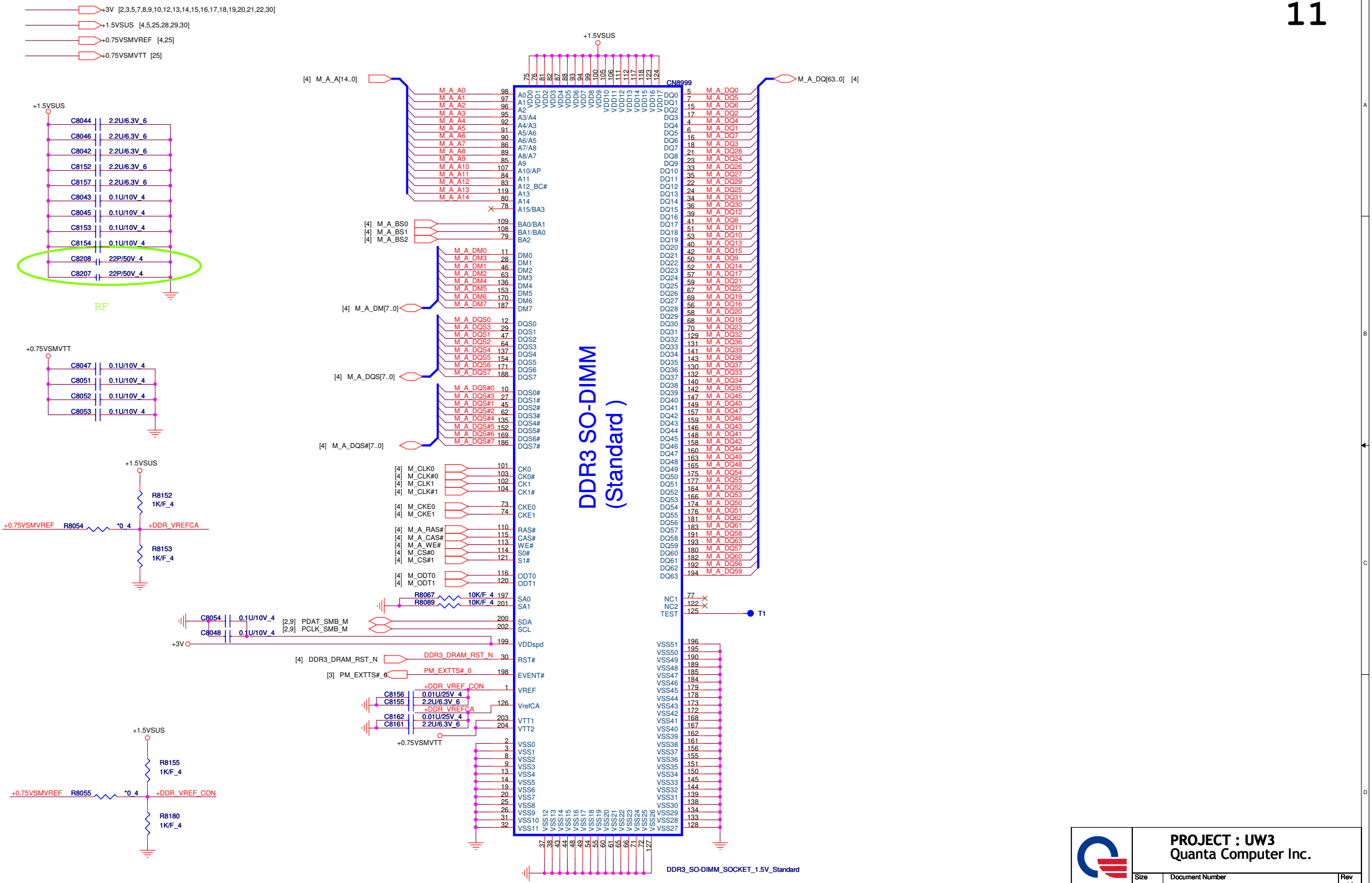
Date: Thursday, September 02, 2010 Sheet 9 of 32

[2,3,5,7,8,9,11,12,13,14,15,16,17,18,19,20,21,22,30] +3V
[12,16,17,19,20,22,30] +5V
[5,6,18,20,30] +1.5V
[2,3,5,7,14,26,29,31] +1.05V
[6,9,30] +3V_S5
[4,30] +5V_S5



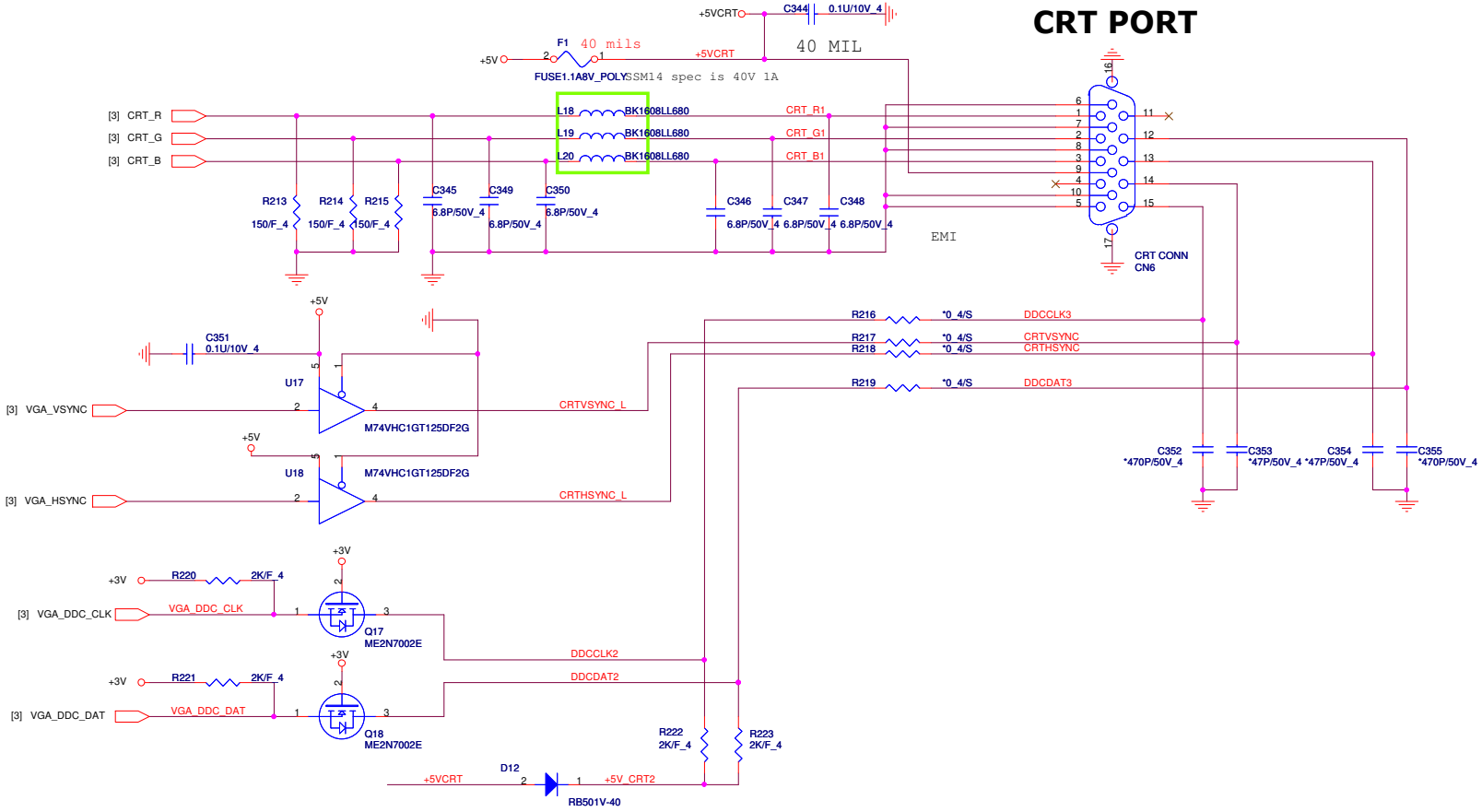


NB5	PROJECT : UW3 Quanta Computer Inc.	
Size	Document Number TigerPoint Power(5/6)	Rev 1A
Date: Thursday, September 02, 2010	Sheet 10 of 32	



[2,3,5,7,8,9,10,11,13,14,15,16,17,18,19,20,21,22,30] +3V

CRT PORT



NB5	PROJECT : UW3 Quanta Computer Inc.	
Size	Document Number CRT	Rev 1A
Date: Thursday, September 02, 2010	Sheet 12 of 32	

+3V [2,3,5,7,8,9,10,11,12,14,15,16,17,18,19,20,21,22,30]

PU for internal CLK input

Unstuff for external XTAL(12MHZ)

Note:

	SD/MMC	MS	XD
SP0			
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

U21

Realtek RTS5159

Close to Chipset

Without memory card 43mA
suspend current 350uA

Internal have pull Hi 200K

RTS5159 max output current for ..
XD card 250mA
SD/MMC 250mA
MS/MSPRO 250mA

G/F: DFHD39MR002

CN8001

CARD READER SOCKET

5 IN1 CARD-READER (PUSH-PUSH)

Support SD/SD PRO/MMC/MS/MS PRO/xD Cards

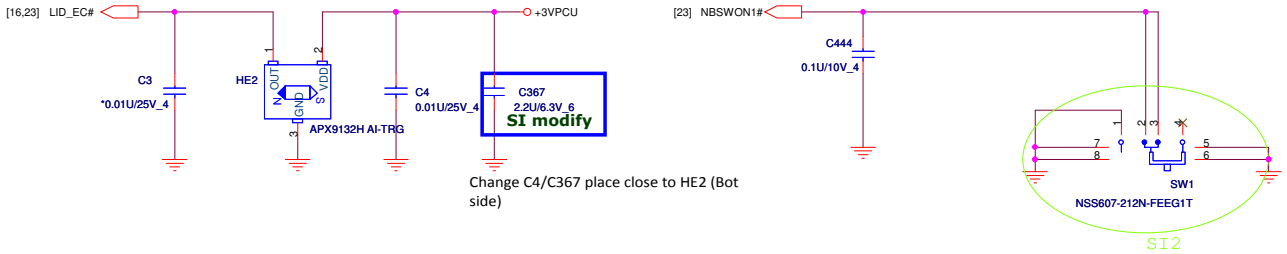
CLOSE to CONN

To Cardreader Connector

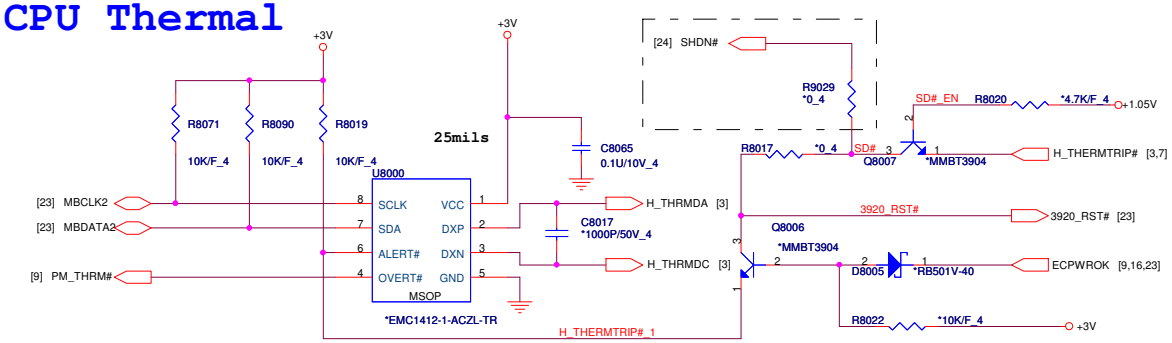
NB5	PROJECT : UW3 Quanta Computer Inc.
Size	Document Number: Realtek RTS5159 & Card Reader — Rev 1A
Date: Thursday, September 02, 2010	Sheet 13 of 32

+3VPCU [9,16,20,21,22,23,24,26,27,30]
+3V [2,3,5,7,8,9,10,11,12,13,15,16,17,18,19,20,21,22,30]
+1.05V [2,3,5,7,10,26,29,31]

LID Switch



CPU Thermal

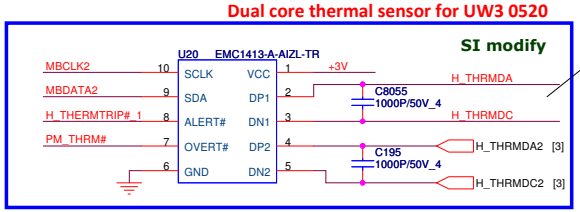


1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

SMSC
Single Code: **AL001412003** **EMC1412-1-ACZL-TR**
C8055 non-Staff, C8017 Staff

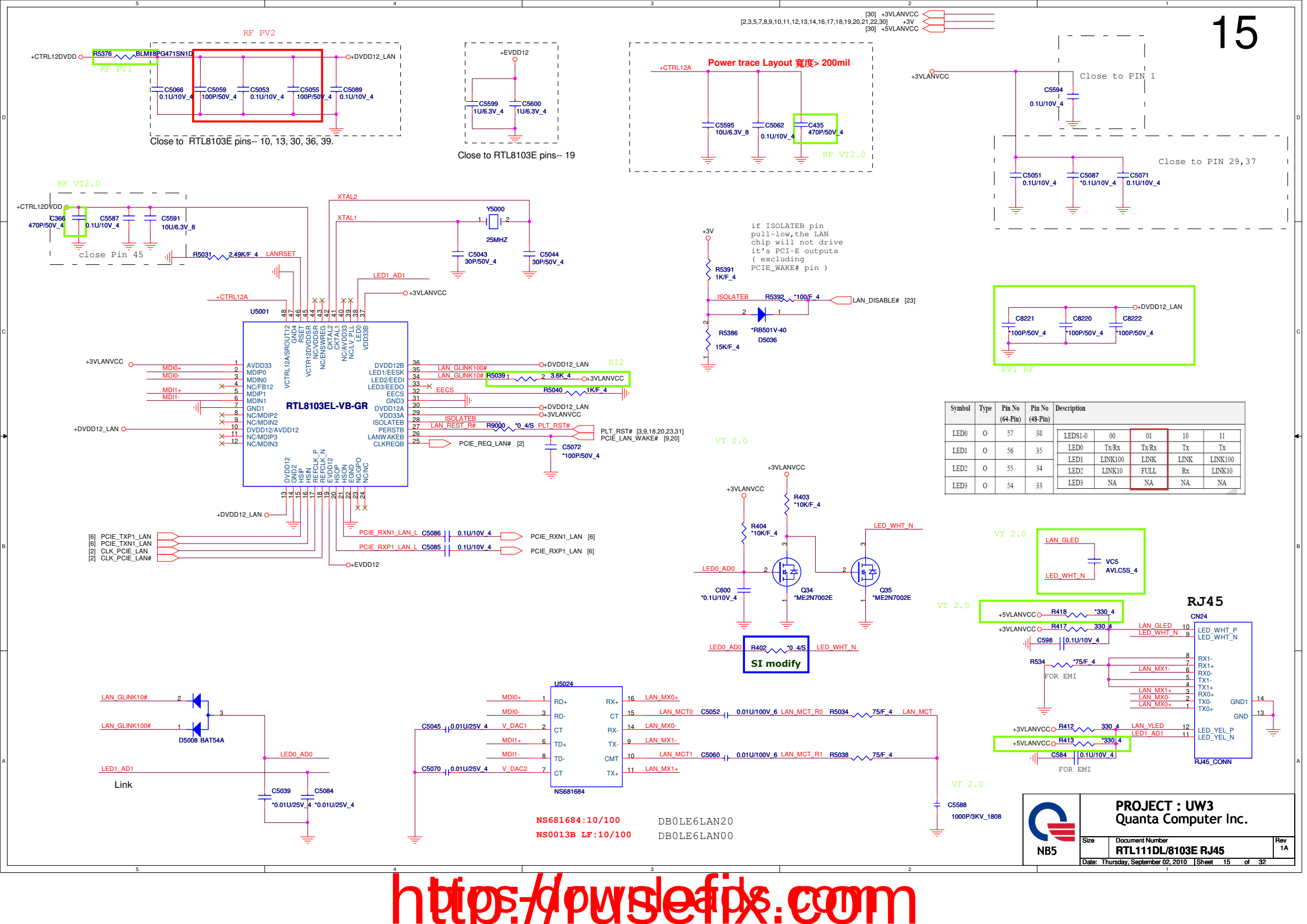
Dual Code: **AL001413002** **EMC1413-A-AIZL-TR**
C8055 staff, C8017 non-Staff

Dual core thermal sensor for UW3 0520



C8055 Place close to U20#2,3
SI modify

NB5
PROJECT : UW3
Quanta Computer Inc.
Size | Document Number: **Power Botton** | Rev: 1A
Date: Thursday, September 02, 2010 | Sheet 14 of 32

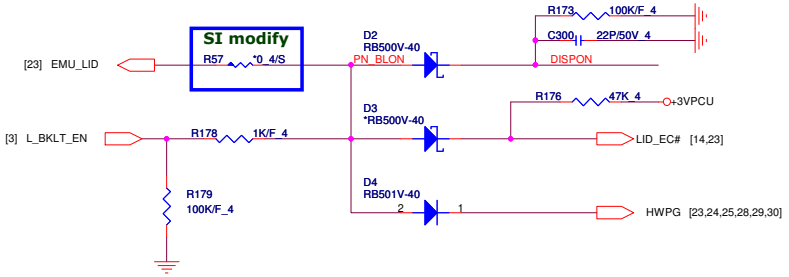


Symbol	Type	Pin No (64-Pin)	Pin No (48-Pin)	Description
LED0	O	57	38	
LED1	O	56	35	
LED2	O	55	34	
LED3	O	54	33	

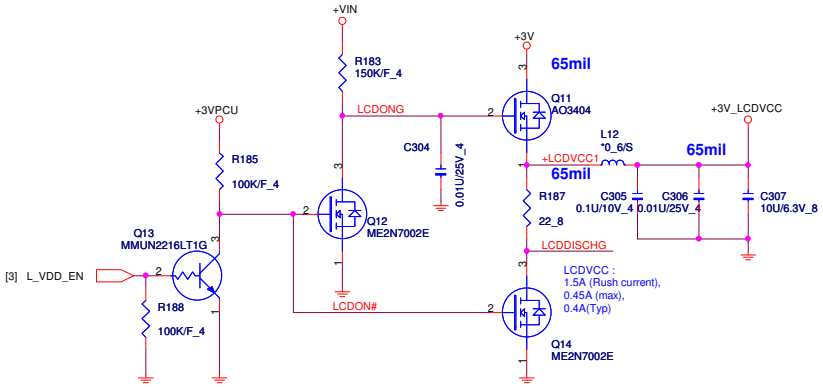
LEDS1-0	00	01	10	11
LED0	Tx/Rx	Tx/Rx	Tx	Tx
LED1	LINK100	LINK	LINK	LINK100
LED2	LINK10	FULL	Rx	LINK10
LED3	NA	NA	NA	NA

NB5	PROJECT : UW3 Quanta Computer Inc.		
	Size	Document Number RTL111DL/8103E RJ45	Rev 1A
	Date: Thursday, September 02, 2010	Sheet 15 of 32	

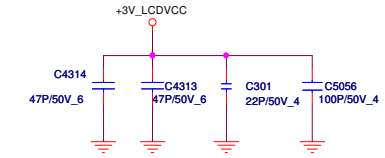
Backlight Control(LDS)

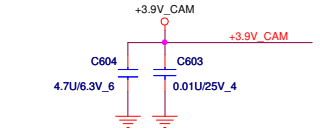


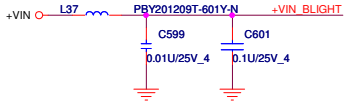
LCD POWER SWITCH



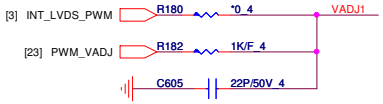
Request by HP RF(47Px2)



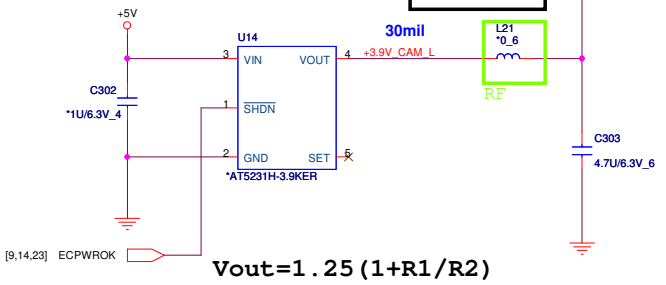




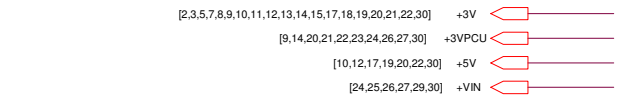
Close to LCD Connector



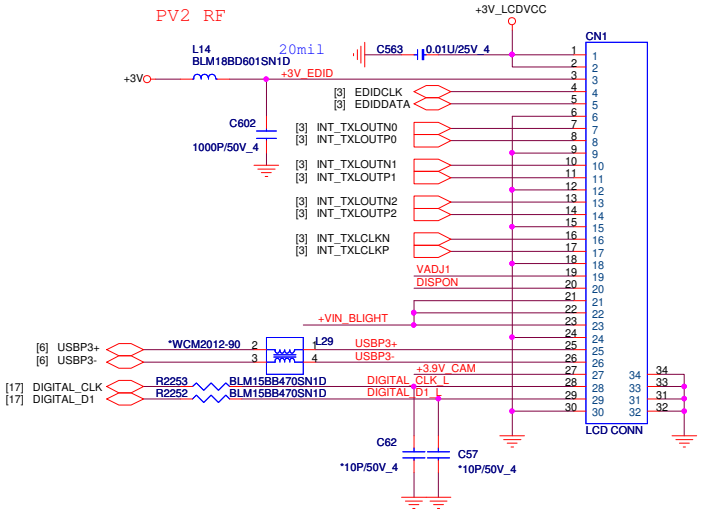
CAMERA POWER



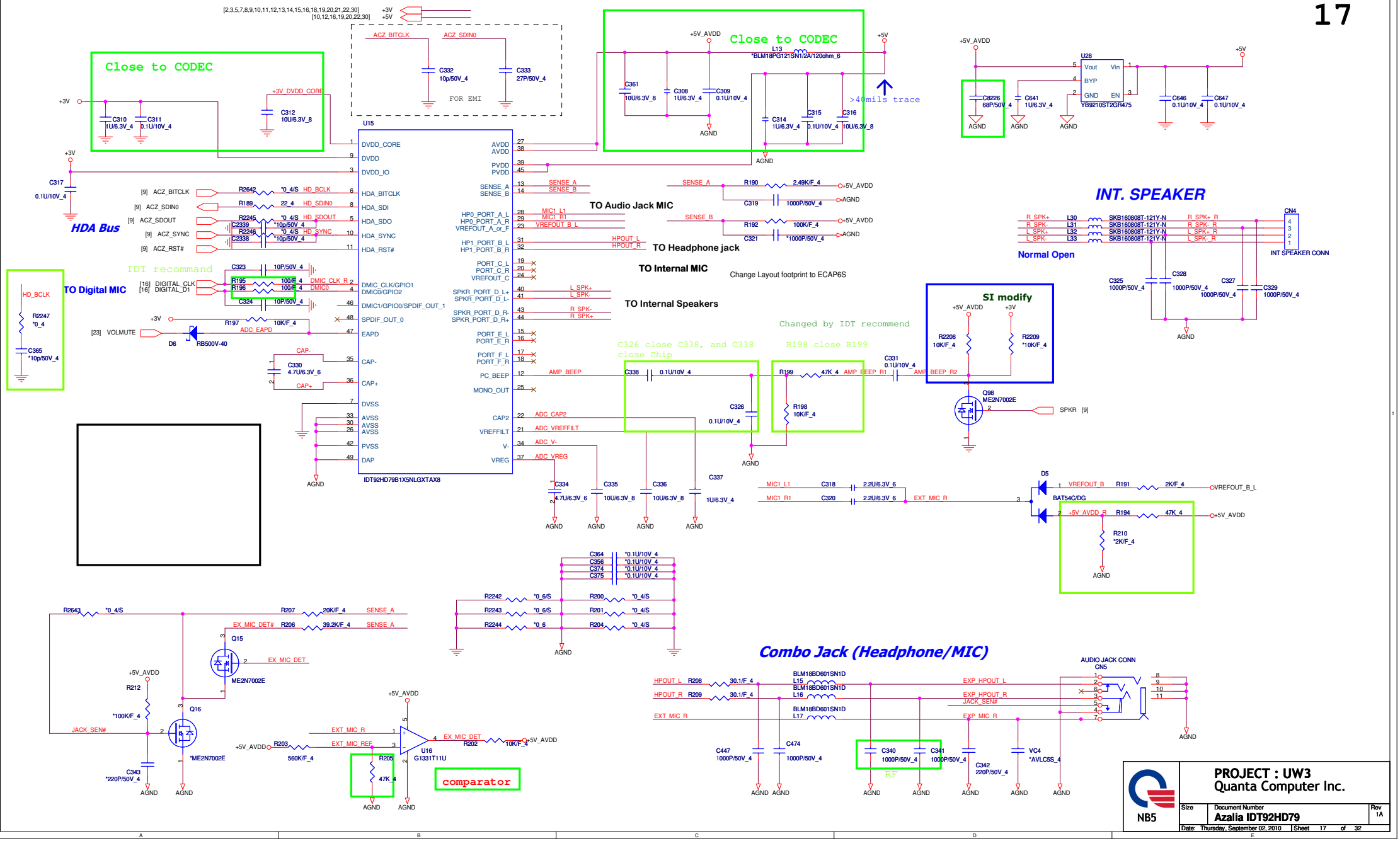
Vout=1.25(1+R1/R2)

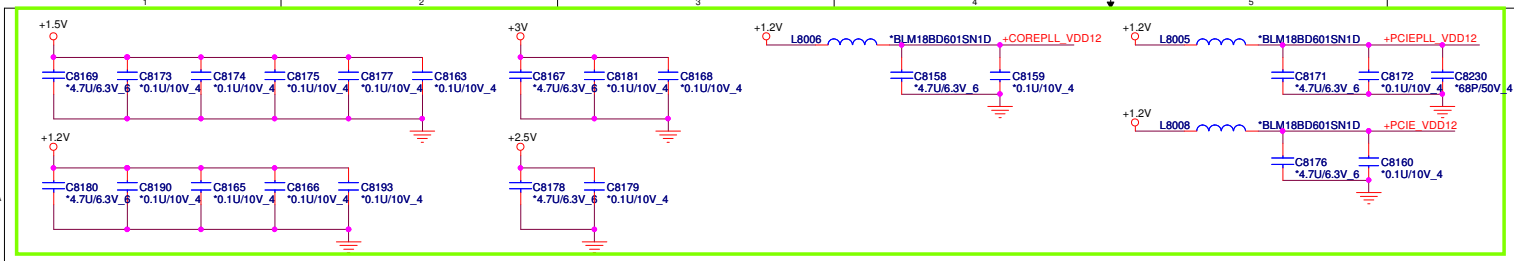


LED Panel(LDS)



NB5	PROJECT : UW3 Quanta Computer Inc.	
Size	Document Number LCD PANEL/CCD MODULE	Rev 1A
Date: Thursday, September 02, 2010	Sheet 16 of 32	

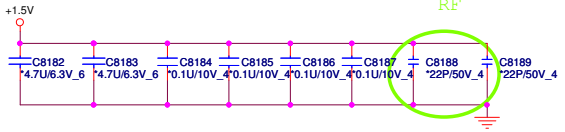




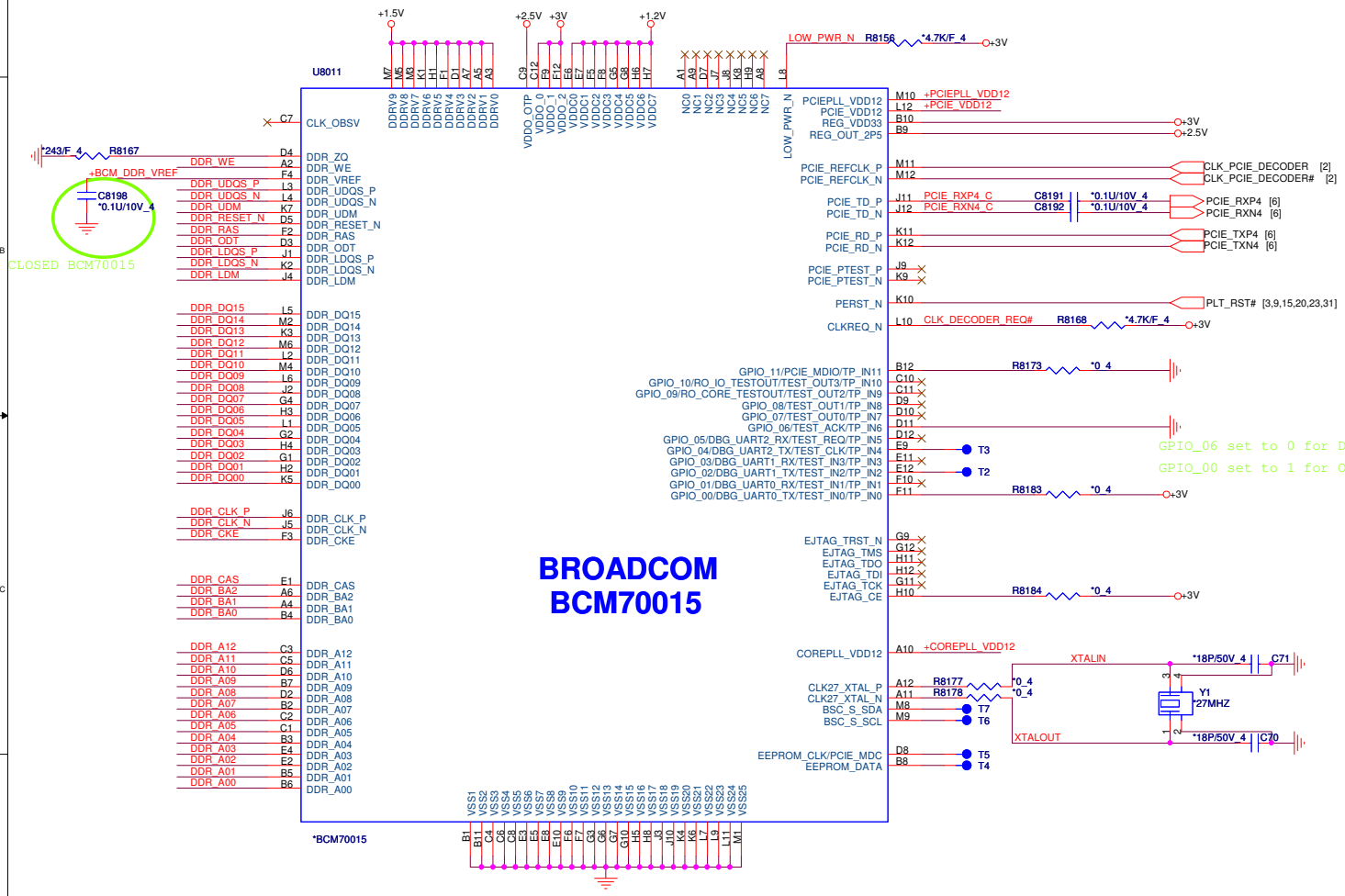
+1.2V [29]
+3V [2,3,5,7,8,9,10,11,12,13,14,15,16,17,19,20,21,22,30]
+1.5V [5,6,10,20,30]

CLOSED DDR3

RF



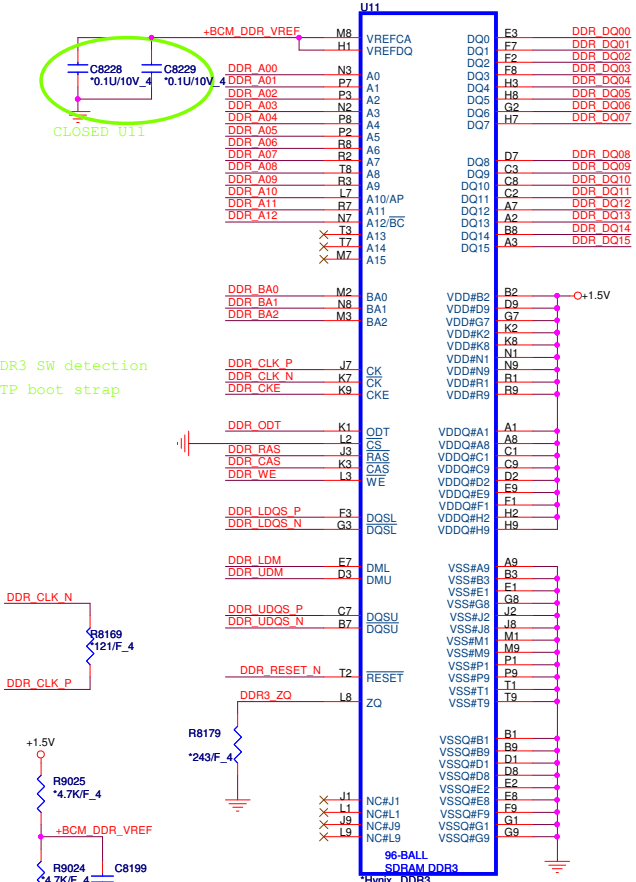
CLOSED BCM70015

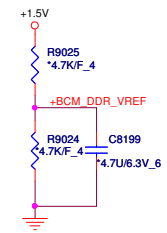


BROADCOM
BCM70015

GPIO_06 set to 0 for DDR3 SW detection

GPIO_00 set to 1 for OTP boot strap





DDR3 RAM Configuration Table

DESCRIPTION		Vendor	Vendor P/N	QCI P/N
DDR3 64Mx16, 128bit	800MHZ	HYNIX	H5TQ1G63BFR-12C	AKD5LZGTW00
DDR3 64Mx16, 128bit	800MHZ	SAMSUNG	K4W1G1646E-HC12	AKD5LGGT502

NB5

PROJECT : UW3
Quanta Computer Inc.

Size	Document Number	Rev
	BROADCOM BCM70015	1A

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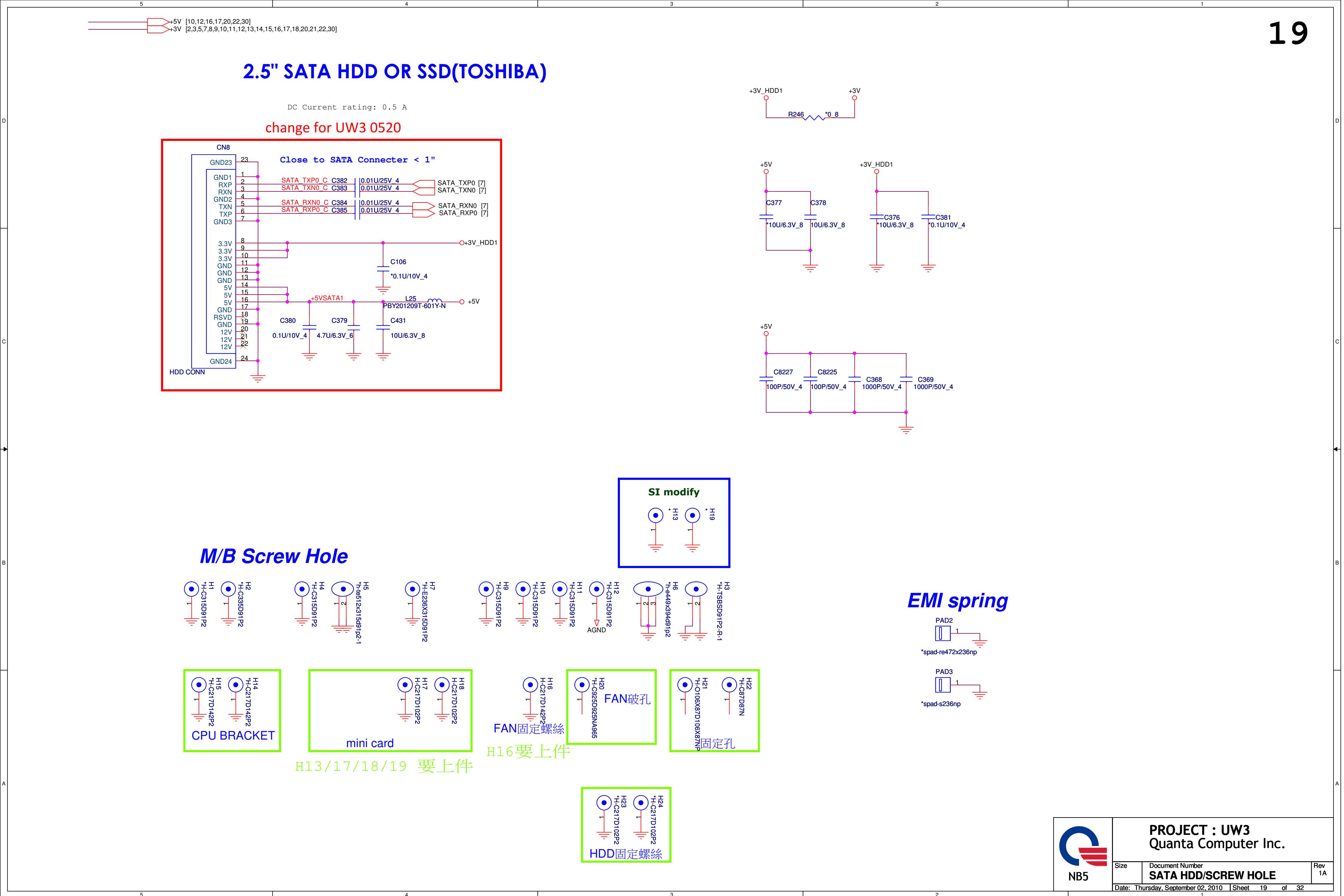

19
+5V [10,12,16,17,20,22,30]
+3V [2,3,5,7,8,9,10,11,12,13,14,15,16,17,18,20,21,22,30]
2.5" SATA HDD OR SSD(TOSHIBA)
DC Current rating: 0.5 A
change for UW3 0520
CN8
HDD CONN
Close to SATA Connecter < 1"
GND23 GND1 RXP RXN GND2 TXN TXP GND3 3.3V 3.3V 3.3V GND GND GND 5V 5V 5V GND RSVD GND 12V 12V 12V GND24
SATA_TXP0_C C382 0.01U/25V_4 SATA_TXP0 [7]
SATA_TXN0_C C383 0.01U/25V_4 SATA_TXN0 [7]
SATA_RXN0_C C384 0.01U/25V_4 SATA_RXN0 [7]
SATA_RXP0_C C385 0.01U/25V_4 SATA_RXP0 [7]
+3V_HDD1
C106 *0.1U/10V_4
+5VSATA1
L25 PBY201209T-601Y-N
+5V
C380 0.1U/10V_4
C379 4.7U/6.3V_6
C431 10U/6.3V_8
+3V_HDD1 +3V
R246 *0_8
C377 *10U/6.3V_8
C378 10U/6.3V_8
C376 *10U/6.3V_8
C381 *0.1U/10V_4
C8227 100P/50V_4
C8225 100P/50V_4
C368 1000P/50V_4
C369 1000P/50V_4
SI modify
H13 H19
M/B Screw Hole
H1 H-C315D91P2
H2 H-C335D91P2
H4 H-C315D91P2
H5 h-te512x315d91p2-1
H7 H-E236X315D91P2
H9 H-C315D91P2
H10 H-C315D91P2
H11 H-C315D91P2
H12 H-C315D91P2
AGND
H6 h-e449x394d91p2
H3 H-TSBSD91P2-R-1
EMI spring
PAD2 *spad-re472x236np
PAD3 *spad-s236np
H15 H-C217D142P2
H14 H-C217D142P2
CPU BRACKET
H17 H-C217D102P2
H18 H-C217D102P2
mini card
H13/17/18/19 要上件
H16 H-C217D142P2
FAN固定螺絲
H16要上件
H20 H-C925D925NA965
FAN破孔
H21 H-O106X87D106X87NP
H22 H-C87D87N
固定孔
H23 H-C217D102P2
H24 H-C217D102P2
HDD固定螺絲
PROJECT : UW3
Quanta Computer Inc.
NB5
Size
Document Number
SATA HDD/SCREW HOLE
Rev 1A
Date: Thursday, September 02, 2010
Sheet 19 of 32

+3VPCU [9,14,16,21,22,23,24,26,27,30]
+1.5V [5,6,10,18,30]
+3V [2,3,5,7,8,9,10,11,12,13,14,15,16,17,18,19,21,22,30]
+5V [10,12,16,17,19,22,30]

Request by HP RF

Mini PCI-E Card 1
Half Mini PCI-E WLAN

The value of the capacitor is suggest by Siemens HQ expert.
For against 900MHz RF interference. The value of capacitor is 27pF.
For against 1800MHz RF interference. The value of capacitor is 10pF.
1nF/10nF value capacitor use for against ESD purpose.

SI modify

No-Stuff

Combo LED

Full mini PCIE for WWAN
Mini PCI-E Card 2

WWAN LED

SIM CARD SIGNALS
ROUTE PARALLEL

Closed CN2

C513 close to CN3

Non-HF:
DFHS10FR381

SIM CARD

No Staff

C5912 close to CN17

C5913 close to CN3

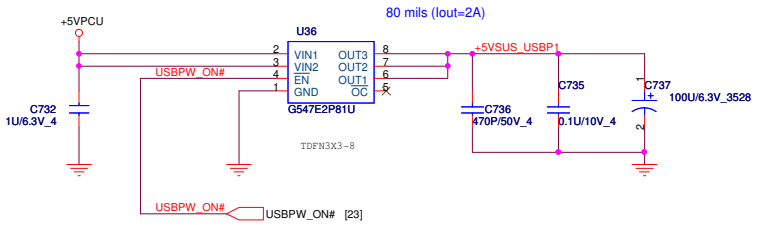
PROJECT : UW3
Quanta Computer Inc.

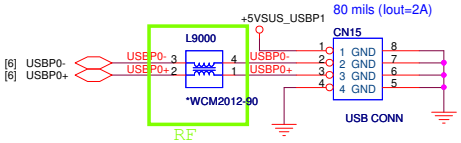
MINI PCIE(WLAN/WWAN)

Rev 1A

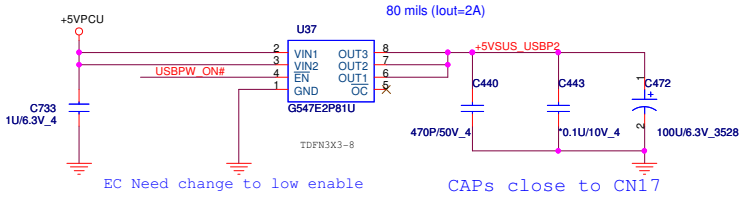
Date: Thursday, September 02, 2010 Sheet 20 of 32

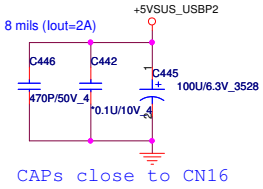
1x Left side USB port supports Keyed USB.

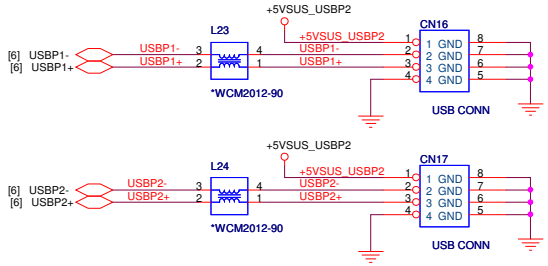




For Right 2xUSB Ports PWR

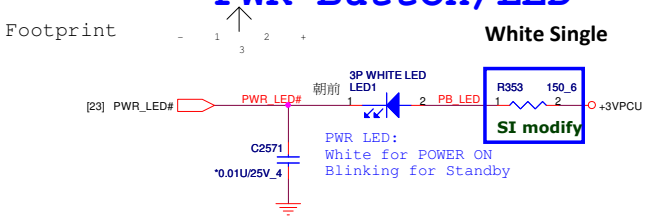






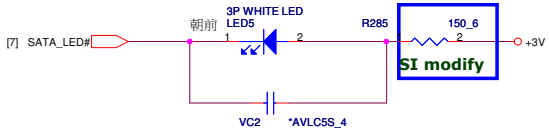
PWR Button/LED

Footprint



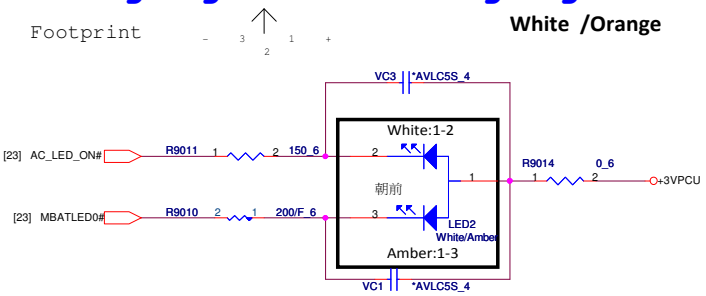
Change R285,R353 to 150 ohm

SATA/LED

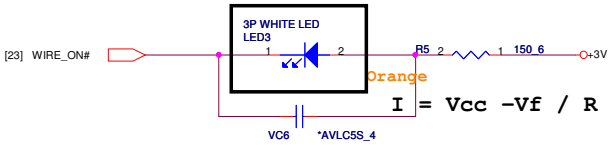


Charging & Discharging/LED

Footprint



WLAN/BLUETOOTH & WWAN LED



NB5	PROJECT : UW3 Quanta Computer Inc.	
Size	Document Number USB Conn/LED/PWR BT	Rev 1A
Date: Thursday, September 02, 2010	Sheet 21 of 32	

Keyboard (KBC)

+3VPCU [9,14,16,20,21,23,24,26,27,30]
+5V [10,12,16,17,19,20,30]
+3V [2,3,5,7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,30]

MY5 C448 220P/50V_4
MY6 C451 220P/50V_4
MY3 C454 220P/50V_4
MY7 C457 220P/50V_4
MY8 C460 220P/50V_4
MY9 C463 220P/50V_4
MY10 C466 220P/50V_4
MY11 C469 220P/50V_4

MY1 C449 220P/50V_4
MY2 C452 220P/50V_4
MY4 C455 220P/50V_4
MY0 C458 220P/50V_4
MX4 C461 220P/50V_4
MX6 C464 220P/50V_4
MX3 C467 220P/50V_4
MX2 C470 220P/50V_4

MX7 C450 220P/50V_4
MX0 C453 220P/50V_4
MX5 C456 220P/50V_4
MX1 C459 220P/50V_4
MY12 C462 220P/50V_4
MY13 C465 220P/50V_4
MY14 C468 220P/50V_4
MY15 C471 220P/50V_4

KEYBOARD PULL-UP

[23] MY[0..15] MY[0..15]
[23] MX[0..7] MX[0..7]

RP3
MY4 MY5 MY6 MY7 — MY3 MY2 MY1 MY0
+3VPCU
*10P8R-8.2K
RP4
MY12 MY13 MY14 MY15 — MY11 MY10 MY9 MY8
*10P8R-8.2K
SI modify

CN20
MX7 MX6 MX5 MY0 MY1 MY2 MX4 MY3 MY4 MY5 MY6 MY7 MY8 MX3 MY9 MX2 MX1 MY10 MY11 MX0 MY12 MY13 MY14 MY15
MX7 [23] MX6 [23] MX5 [23] MY0 [23] MY1 [23] MY2 [23] MX4 [23] MY3 [23] MY4 [23] MY5 [23] MY6 [23] MY7 [23] MY8 [23] MX3 [23] MY9 [23] MX2 [23] MX1 [23] MY10 [23] MY11 [23] MX0 [23] MY12 [23] MY13 [23] MY14 [23] MY15 [23]
25 26
KB CONN

Change fro UW3 0520

UW2/UW3 KB Matrix

TOUCH PAD CONNECTOR

Change CN25 Pin-define and footprint

[23] TPCLK TPCLK L35 BLM18BD601SN1D TPCLK-1
[23] TPDATA TPDATA L36 BLM18BD601SN1D TPDATA-1
TP_CONN
CN25
C574 10p/50V_4
C575 10p/50V_4
close conn
+5V R288 4.7K/F_4 TPCLK
R289 4.7K/F_4 TPDATA
By EMI request,
+5V 25 mils C572 0.1U/10V_4

Pin Number Pin Name Description
1 GND Ground Power
2 SWL Left Button
3 VDD Power Supply Voltage
4 DATA Data
5 CLK Clock
6 SWR Right Button

TOUCH SCREEN

CN23
USBP6- USBP6+ *WCM2012-90 L9001
USBP6- [6] USBP6+ [6]
*Touch screen Conn
+3V

CPU FAN

+3V
R292 4.7K/F_4
[23] FAN1SIG
+5V_FAN
CN22
FAN CONN
C478 2.2U/6.3V_6
C1479 *0.1U/10V_4
DFHD03MR008

FANPWR = 1.6*VSET
30 MIL
U25
+5V R293 10K/F_4 FAN_FON#
[23] VFAN R2667 *0_4/S FAN_VSET
VIN VO /FON GND VSET GND
+5V_FAN
G991PV11
C2482 *0.1U/10V_4
Request RC by HP RF

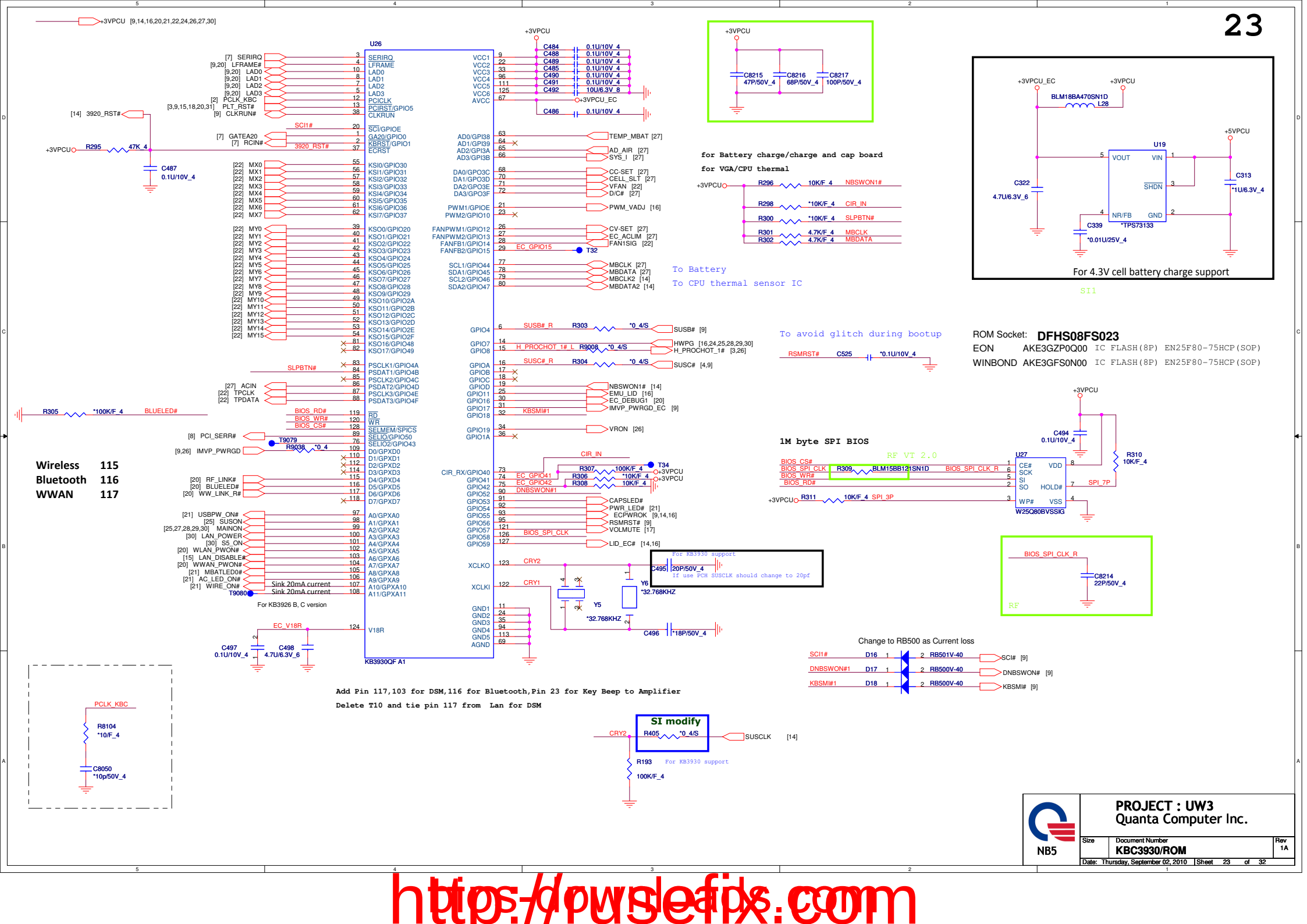
Gnd shape

NB5

PROJECT : UW3
Quanta Computer Inc.

Size	Document Number	Rev
	KB/TP/BT/CPU FAN/TP SCREEN	1A

Date: Thursday, September 02, 2010 Sheet 22 of 32



NB5

PROJECT : UW3
Quanta Computer Inc.

Size	Document Number	Rev
	KBC3930/ROM	1A

Date: Thursday, September 02, 2010 Sheet 23 of 32

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

SI2_RF

PC1032 47P/50V_4 PC1033 47P/50V_4 PC1034 47P/50V_4

PV1_RF

C370 1000P/50V_4 C371 1000P/50V_4 C372 1000P/50V_4

+5VPCU Volt +/- 5%
Countinue current:4A
Peak current:5.5A
OCP minimum 6A

SI2_RF

PC1027 47P/50V_4 PC1029 47P/50V_4 PC1030 47P/50V_4

PV1_RF

C387 1000P/50V_4 C373 1000P/50V_4 C386 1000P/50V_4

+3VPCU Volt +/- 5%
Countinue current:4A
Peak current:5.5A
OCP minimum 6A

Place these CAPs close to FETs

PC1002 *4.7U/25V_8 PC1026 4.7U/25V_8 PC1003 2200P/50V_4 PC1004 0.1U/25V_4 PC1008 0.1U/25V_4

PD1002 UDZ5V6B-7-F

PR1002 1K/F_4 PR1003 150K/F_4

8206ON_LDO

+5V_VCC1 PC1009 1U/6.3V_4

+5VALW PC1010 *0.1U/10V_4 PC1011 4.7U/6.3V_6 PC1012 0.1U/10V_4

PR1008 *0_4/S PR1009 205K/F_4

PU1001 RT8206B

BYP OUT1 FB1 ILIM1 PGOOD1 ON1 DH1 LX1 PAD PAD PAD PAD PAD BST1 DL1 VDD N.C AGND PGND DL2 BST2 PAD PAD

LDOREFIN LDO IN N.C ONLDO VCC TON REF

REFIN2 ILIM2 OUT2 SKIP PGOOD2 ON2 DH2 LX2

5V_FB1 PGOOD1 5V_DH 5V_LX 5V_BST1 5V_DL

3V_FB2 PGOOD2 3V_DH 3V_LX 3V_BST2 3V_DL

PR1006 182K/F_4

PQ1002 AO4496 PQ1005 AO4712

PL1003 2.5uH/7.5A

PR1011 2.2_8 PC1018 1500P/50V_4

SI2_RF

Rds(on) 20m ohm

PC1013 220U/6.3V_7343ESR25 PC1014 0.1U/10V_4 PR1007 *0_4 PR1013 *0_4/S

PC1019 0.1U/25V_4 PC1020 0.1U/25V_4

PR1015 2_6 PR1016 2_6

PD1003 BAV99 PD1004 BAV99 PD1009 1SS355

PC1021 0.01U/25V_4 PC1024 0.01U/25V_4 PC1023 0.1U/25V_4

PR1017 *0_4/S PR1018 *0_4 PR1021 100K/F_4

PC1263 2.2U/6.3V_6 PC1025 1U/25V_6

+10VALW +15VALW +5VALW

PC1022 1U/6.3V_4 PR1019 *0_4/S

R8070 *0_4 R8078 *0_4 R8086 *0_4

SI1 RF

[14] SHDN#

Place these CAPs close to FETs

PC1005 0.1U/25V_4 PC1006 2200P/50V_4 PC1007 *4.7U/25V_8 PC1028 4.7U/25V_8

PQ1003 AO4496 PQ1004 AO4712

PL1002 2.5uH_7.5A +3.3V_ALWP

PR1010 2.2_8 PC1015 1500P/50V_4

SI2_RF

PR1012 *0_4/S PR1014 *0_4

PC1016 0.1U/10V_4 PC1017 220U/6.3V_7343ESR25

+3VPCU

Rds(on) 20m ohm

SI2_RF

PC1031 47P/50V_4 PC1036 47P/50V_4

NM6 1.1 RF suggestion

PC38 68P/50V_4 PC39 68P/50V_4 PC40 68P/50V_4

PGOOD2 PGOOD1

PR1020 *0_4/S PR3256 10K/F_4

HWPG [16,23,25,28,29,30]

SI2_RF

PC1035 47P/50V_4

NB5	PROJECT : UW3 Quanta Computer Inc.	
Size	Document Number 3VPCU/5VPCU(RT8206)	Rev 1A
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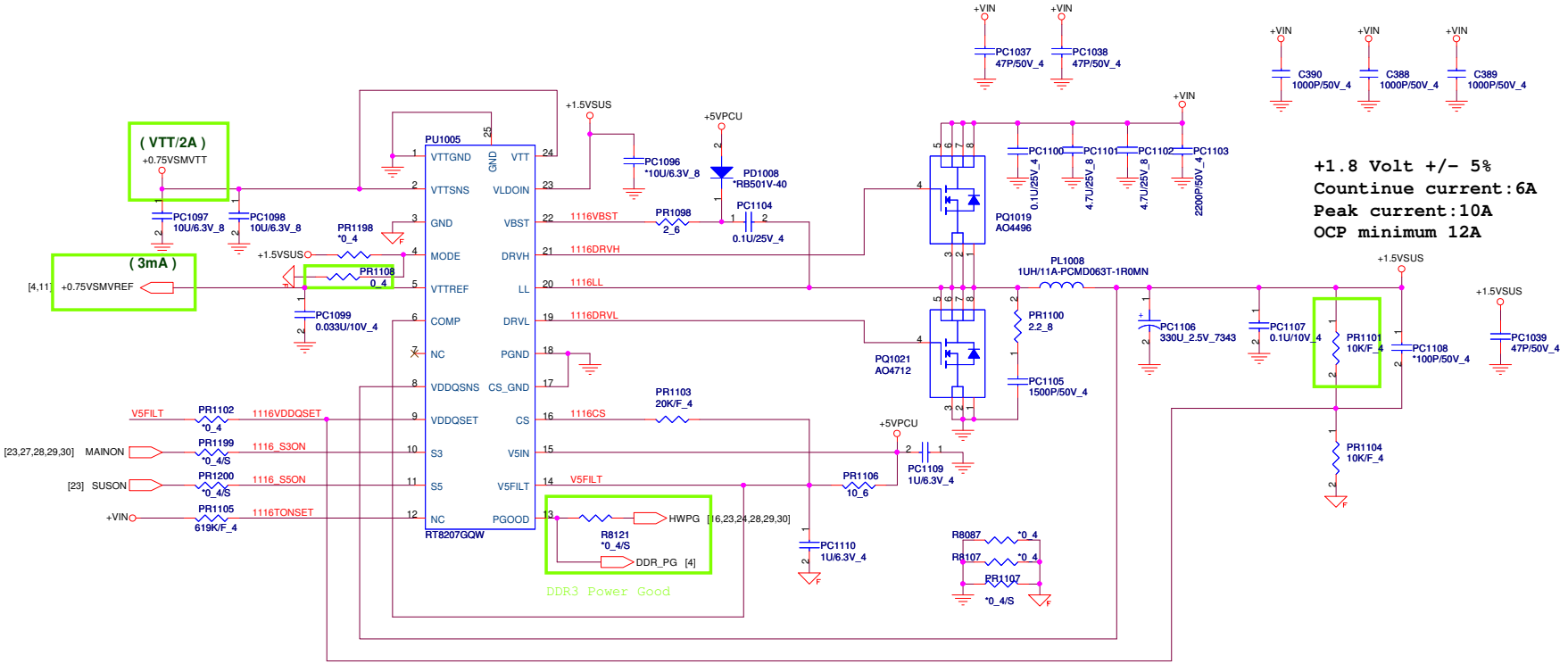
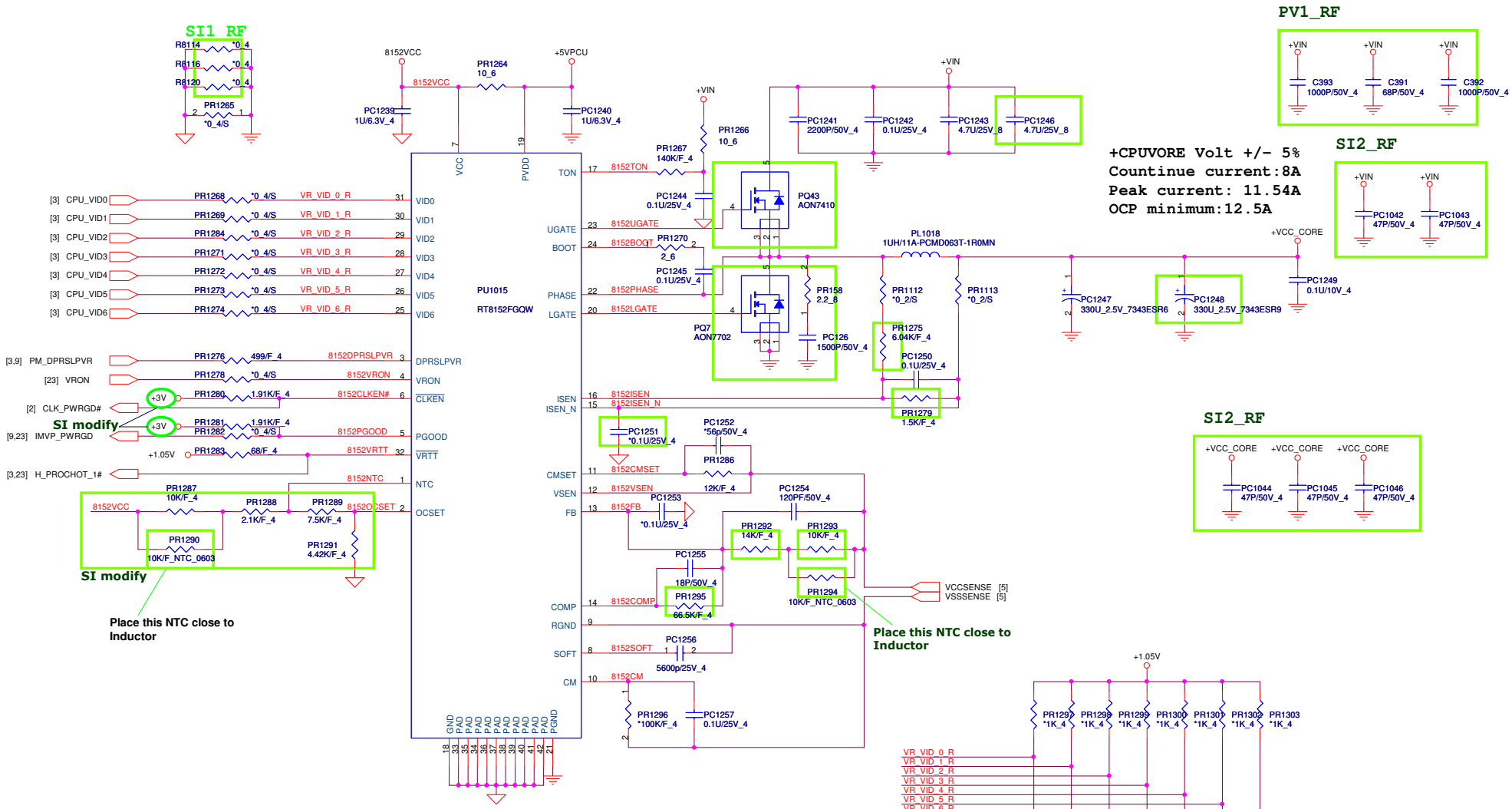
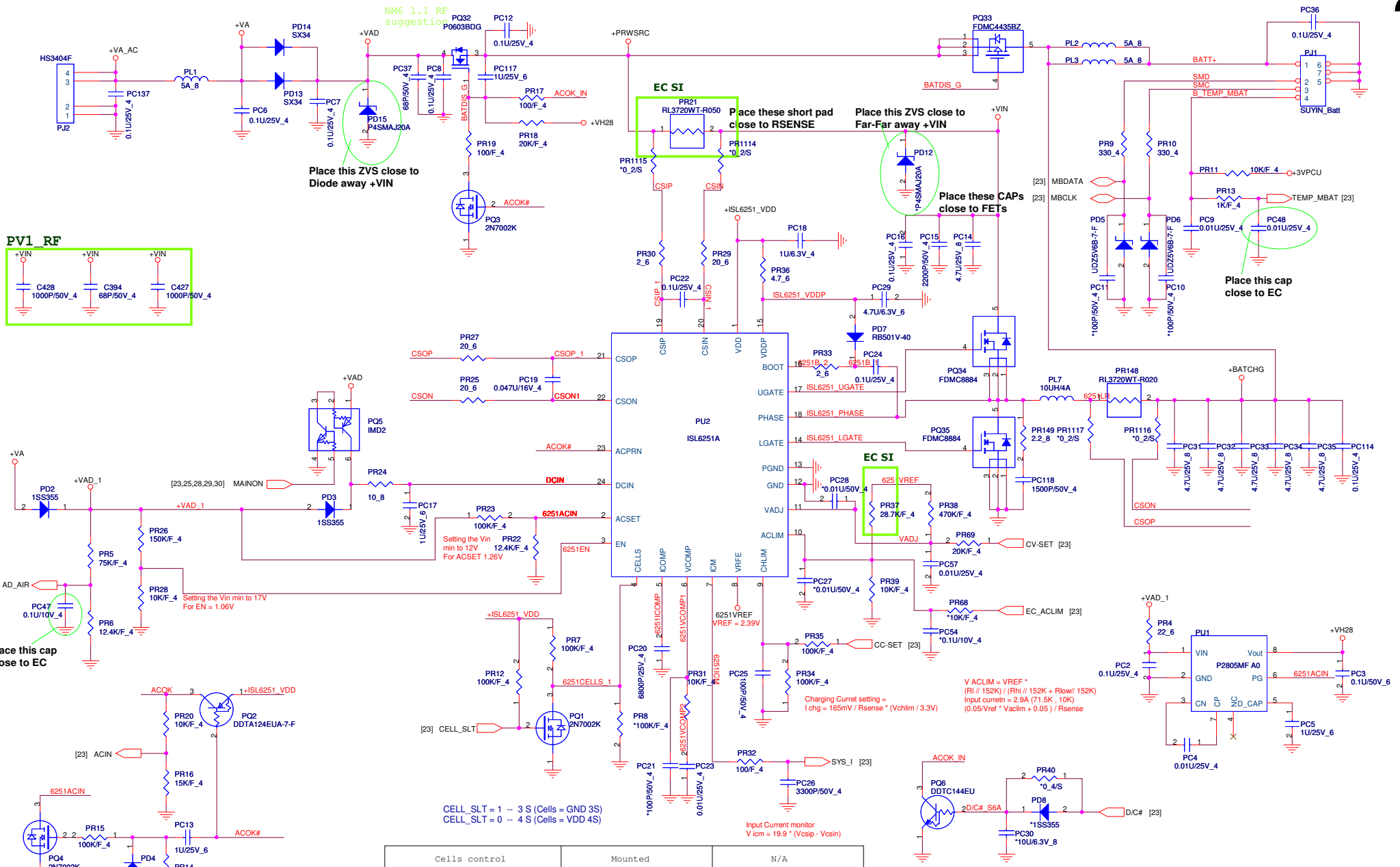


NB5	PROJECT : UW3 Quanta Computer Inc.	
Size	Document Number DDR2 +1.8VSUS/+0.89V	Rev 1A
Date: Thursday, September 02, 2010	Sheet 25 of 32	



PROJECT : UW3	
Quanta Computer Inc.	
NB5	Size: — Document Number: Vcore(RT8152B) Rev: 1A
Date: Thursday, September 02, 2010	Sheet 26 of 32



Cells control	Mounted	N/A
3cells only	PR8	PR7, PR12, PQ1
option for 3cells/4cells	PR7, PR12, PQ1	PR8

PROJECT : UW3
Quanta Computer Inc.

NB5

Size	Document Number	Rev
	CHARGER (ISL6251A)	1A

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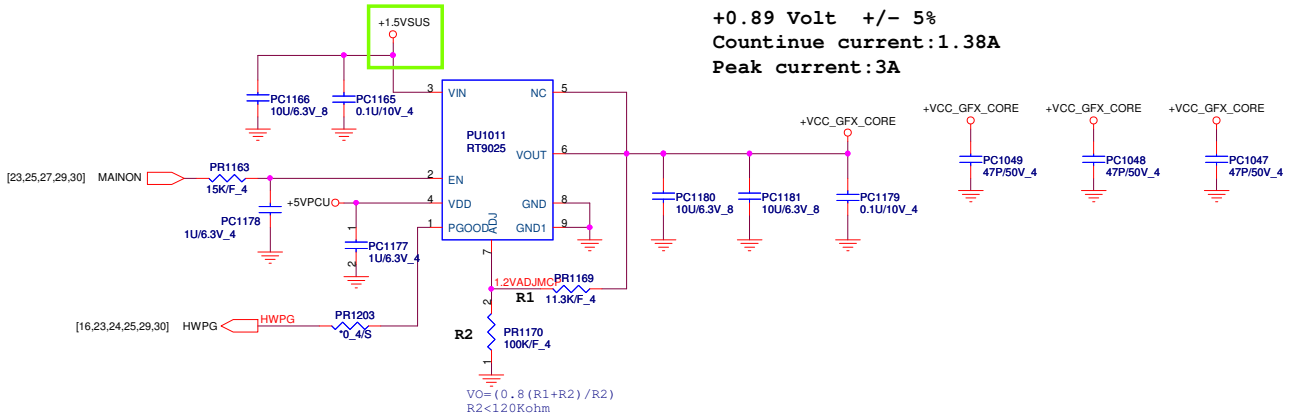
+VCC_GFX_CORE



+0.89 Volt +/- 5%
Countinue current:1.38A
Peak current:3A

NB5	PROJECT : UW3 Quanta Computer Inc.	
Size	Document Number +1.05V/+1.5V (RT8204)	Rev 1A
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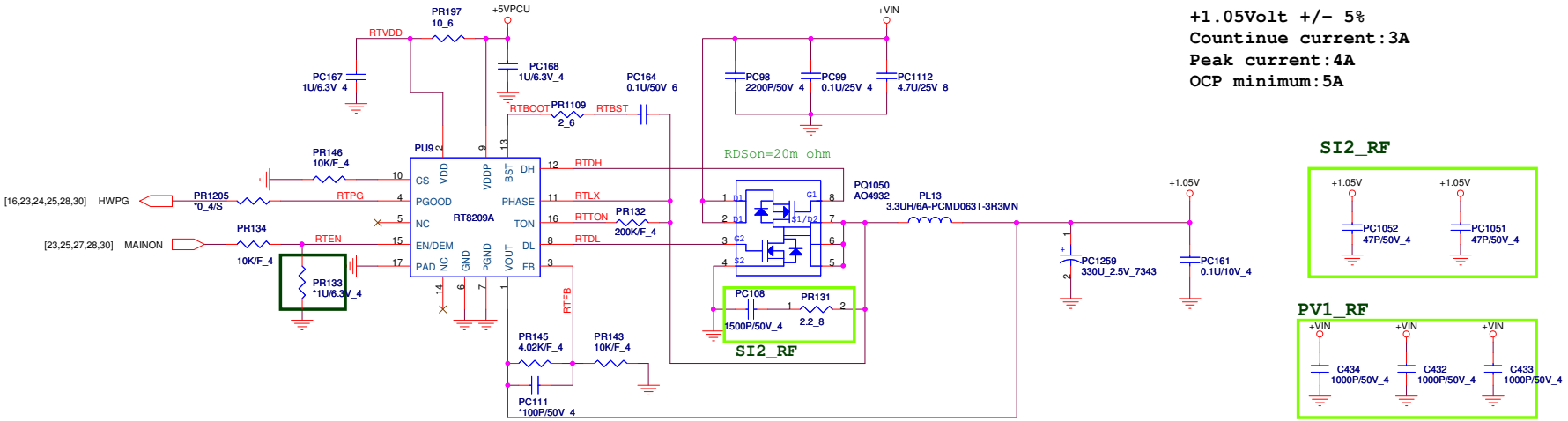
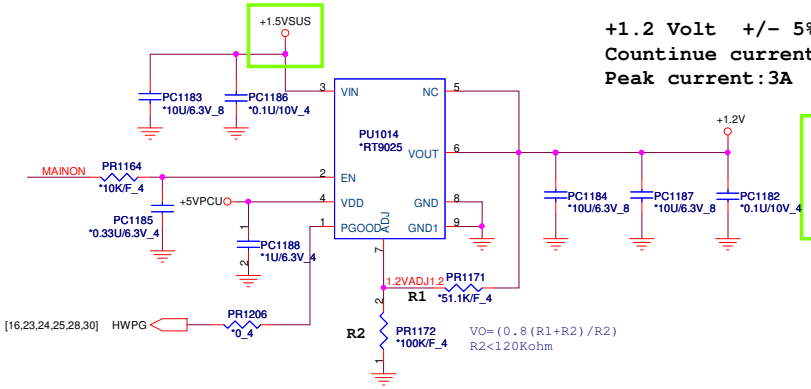
VCCP1.05V



+1.05Volt +/- 5%
Countinue current:3A
Peak current:4A
OCP minimum:5A

SI2_RF

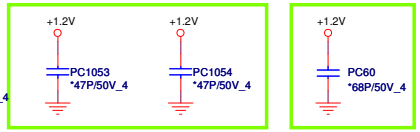
PV1_RF



+1.2 Volt +/- 5%
Countinue current:0.8A
Peak current:3A

SI2_RF

NM6 1.1 RF suggestion



NB5

PROJECT : UW3
Quanta Computer Inc.

Size	Document Number	Rev
	+1.05V (RT8209A)	1A

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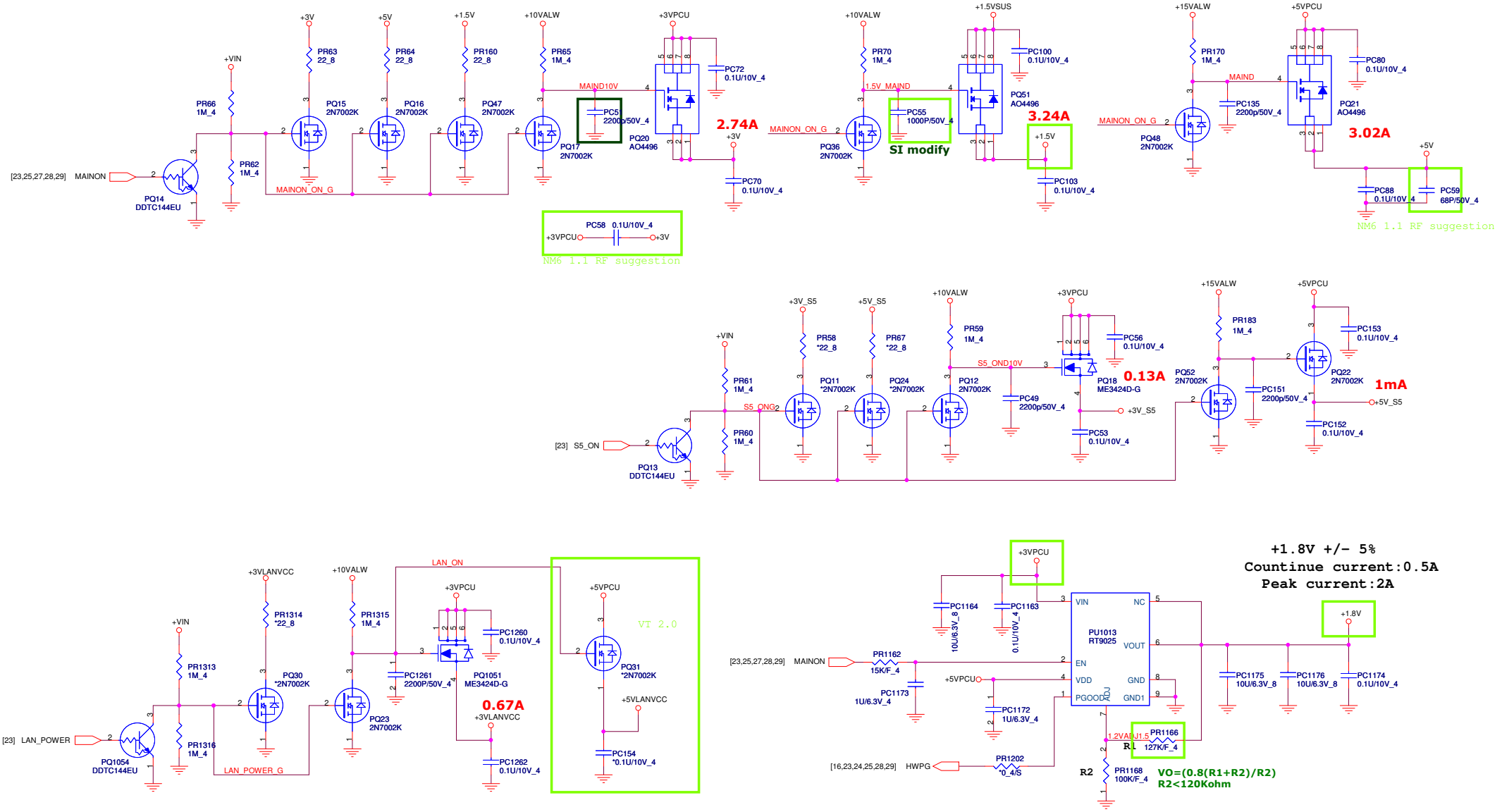
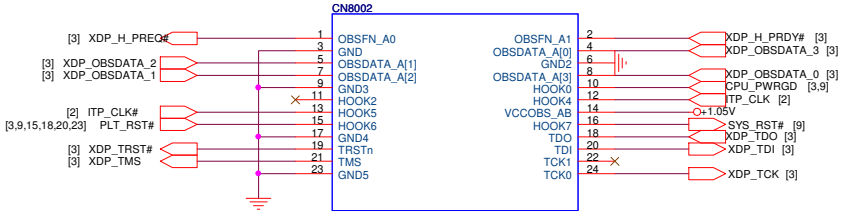


NB5	PROJECT : UW3 Quanta Computer Inc.	
Size	Document Number Discharge/LANVCC/+1.5V	Rev 1A
Date: Thursday, September 02, 2010	Sheet 30 of 32	

CPU XDP

[2,3,5,7,10,14,26,29] +1.05V

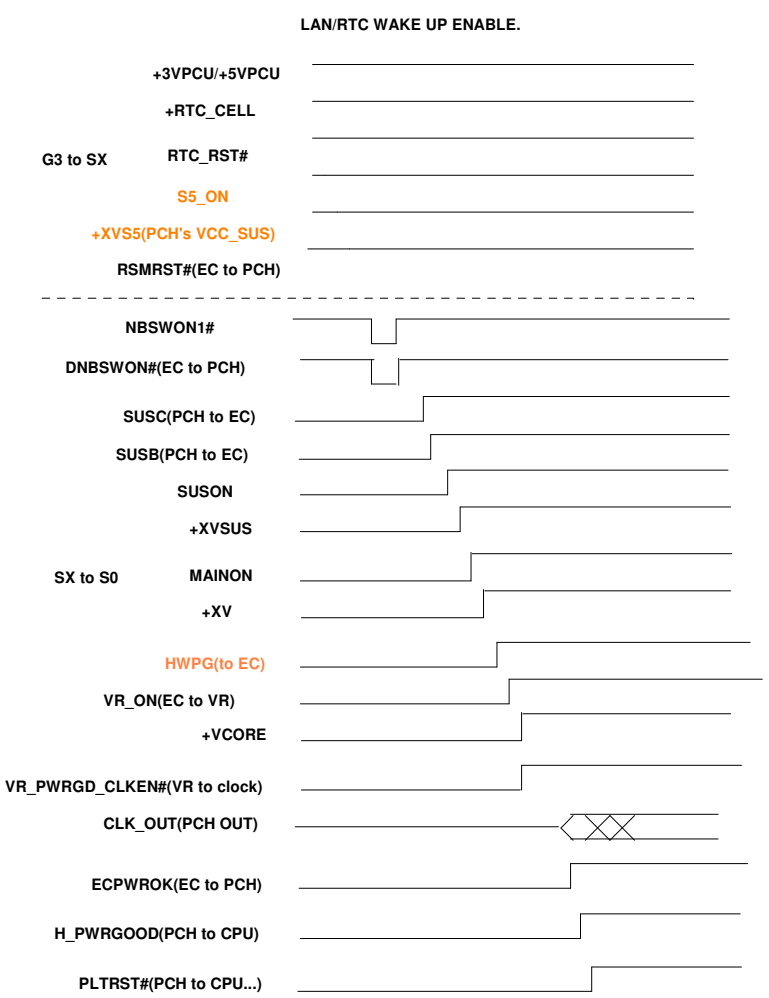


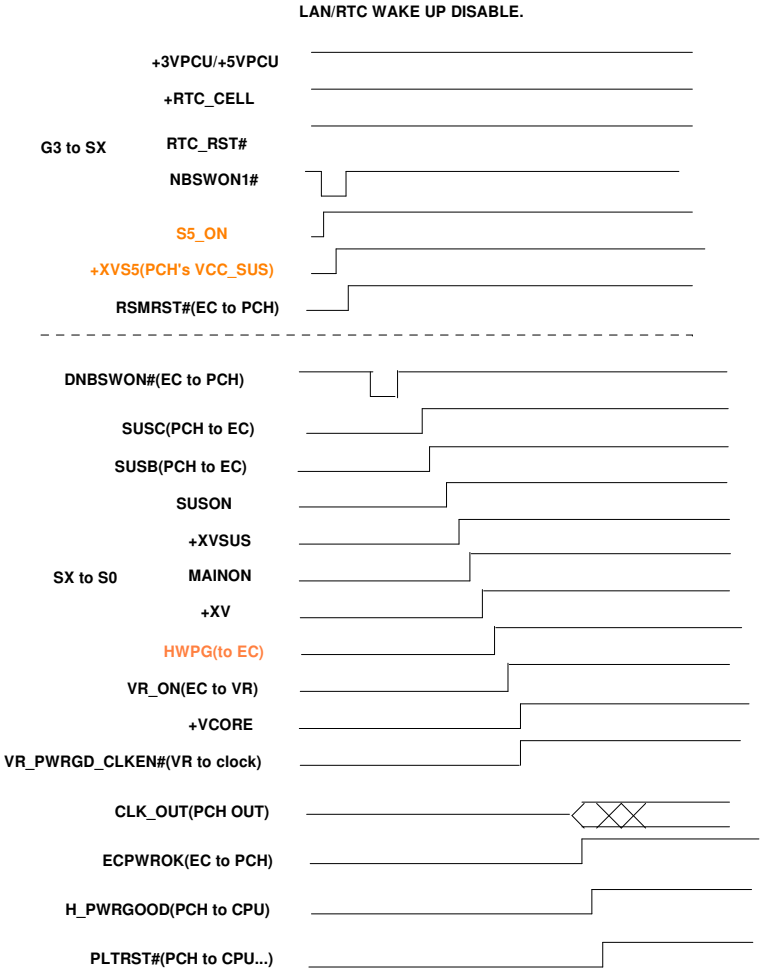
*196013-24011

CLOSE CN8002

NB5	PROJECT : UW3 Quanta Computer Inc.	
Size	Document Number XDP	Rev 1A
Date: Thursday, September 02, 2010	Sheet 31 of 32	

Power up sequence





NB5	PROJECT : UW3 Quanta Computer Inc.	
Size	Document Number Power Sequence	Rev 1A
Date: Thursday, September 02, 2010	Sheet 32 of 32	