Selek 15" CFL Schematic

CFL-H

2019/03/25

REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

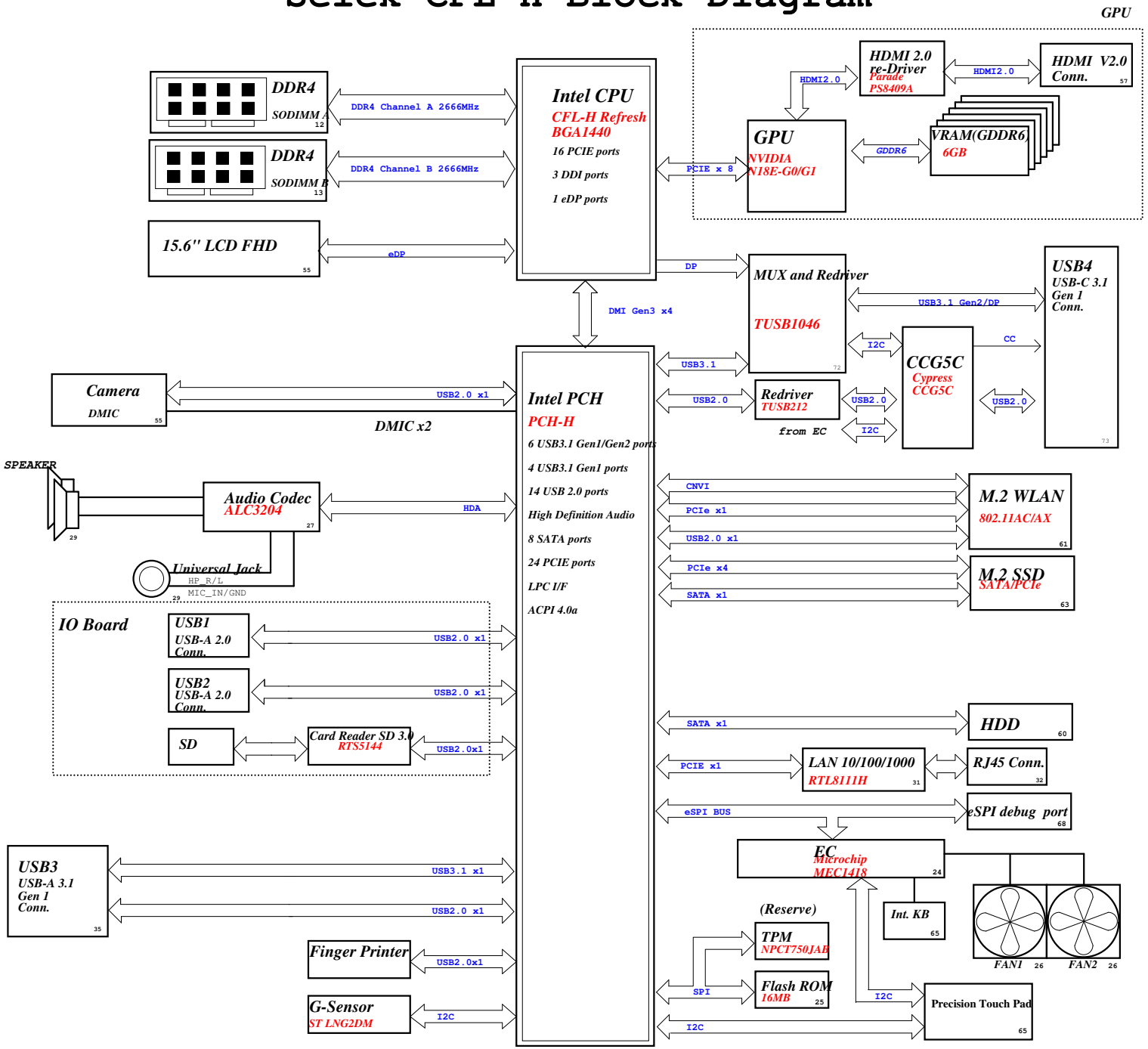
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page		
Size: A4	Document Number: Selek CFL-H	Rev: A00
Date: Thursday, April 11, 2019	Sheet 1 of 105	

Project Code : 4PD0H7010001
PCB P/N : 18812-SC
Revision : X02

Selek CFL-H Block Diagram



CHARGER ISL88739 44	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC TPS51225RUKR-GP 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_PWR 3D3V_S5 5V_PWR 5V_S5

CPU Core Power NCP81208MNTXG 46~50 NCP81382MNTXG x 2 NCP81382MNTXG (23e) NCP81253MNTBG	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DCBATOUT	+VCCGT
DCBATOUT	+VCCGT (23e)
DCBATOUT	+VCCSA

DDR4 SUS RT8231AGQW-GP APL5930KAI-TRG 51	
INPUTS	OUTPUTS
DCBATOUT 3D3V_S5	1D2V_S3 0D6V_S0 2D5V_S3

CPU VCCPRIM_CORE 1V 11	
INPUTS	OUTPUTS
1D0V_S5	+VCCPRIM_CORE

CPU DCDC-V1D00A AOZ2262QI-10-GP-U 53	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

LDO-V1D8V APL5930KAI-TRG 54	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

5V/3V S0 TPS22966DPUR-GP 40	
INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0

EOPIO/EDRAM (23e) TPS22961DNYT 40	
INPUTS	OUTPUTS
1D0V_S5 1D0V_S5	+V_EDRAM_VR +V_EOPIO_VR

3D3V VGA AO3419L 86	
INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0

VGA_CORE ISL62771HRTZ-GP-U 85	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

1D5V_VGA_S0 Y8288RAC-GP 86	
INPUTS	OUTPUTS
DCBATOUT	1D5V_VGA_S0

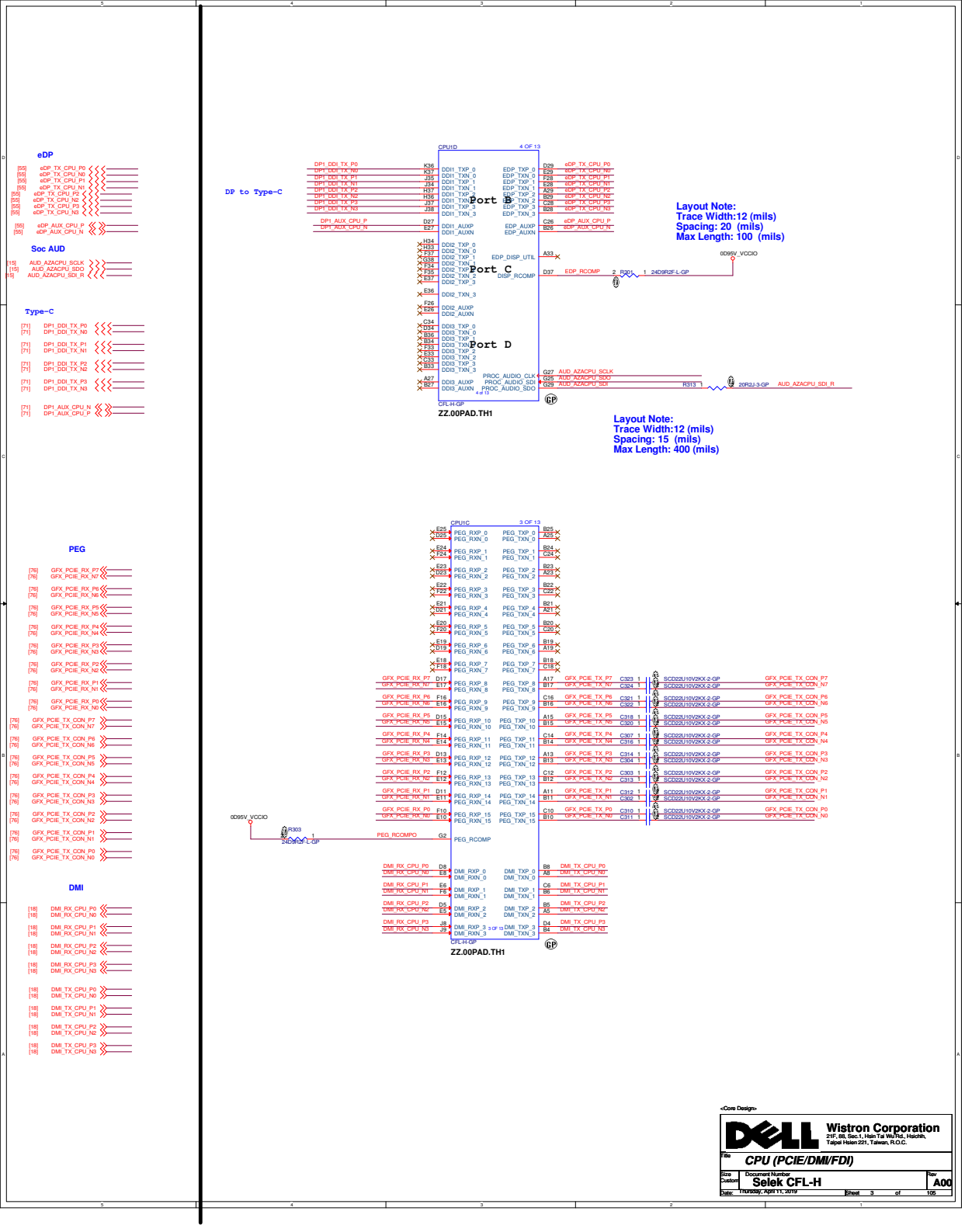
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

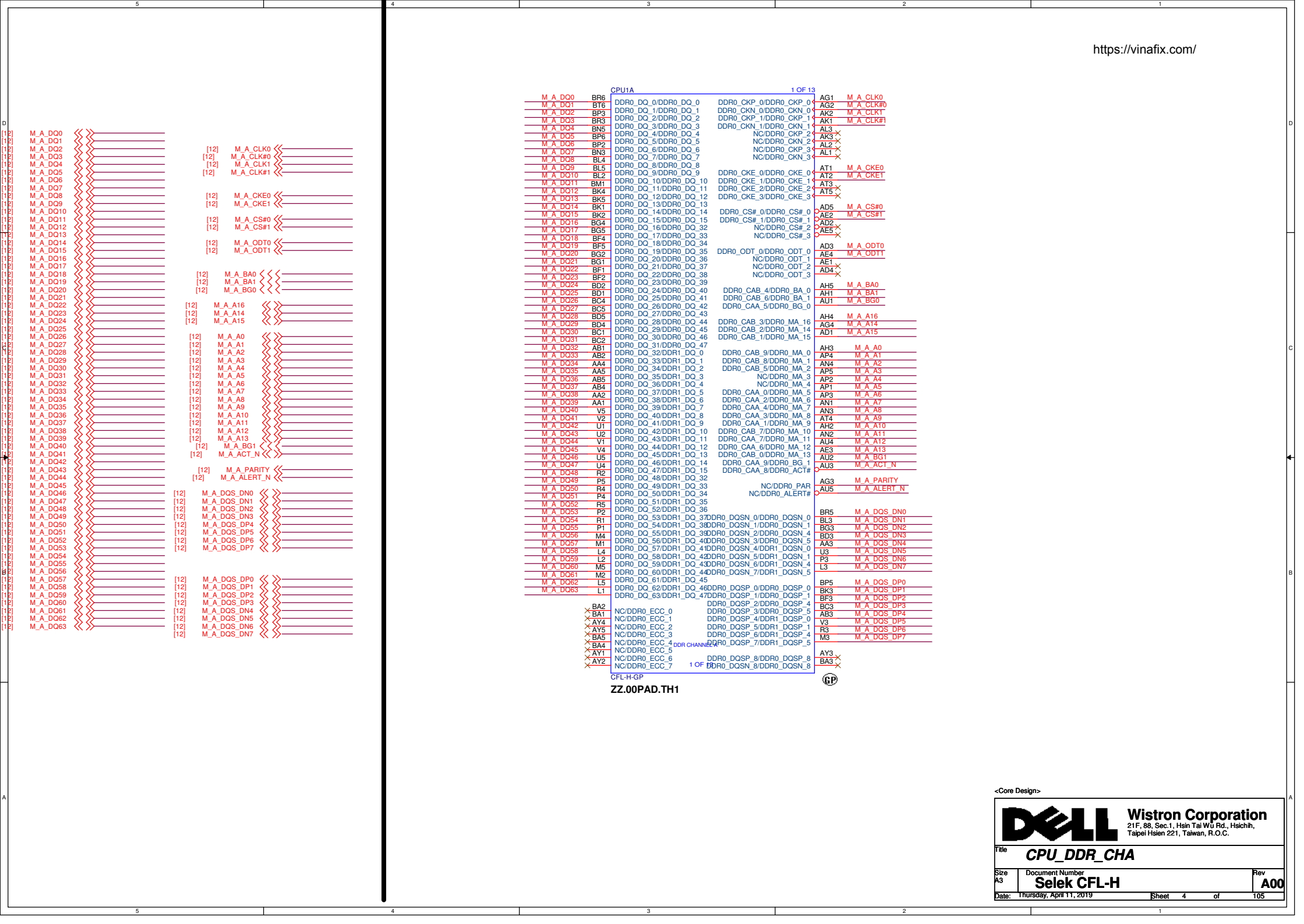
Size: Custom	Document Number: Selek CFL-H	Rev: A00

Date: Thursday, April 11, 2019 Sheet 2 of 105



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (PCIE/DMI/FDI)	
Size: Custom	Document Number: Selek CFL-H	Rev: A00
Date: Thursday, April 11, 2019	Sheet 3 of 105	

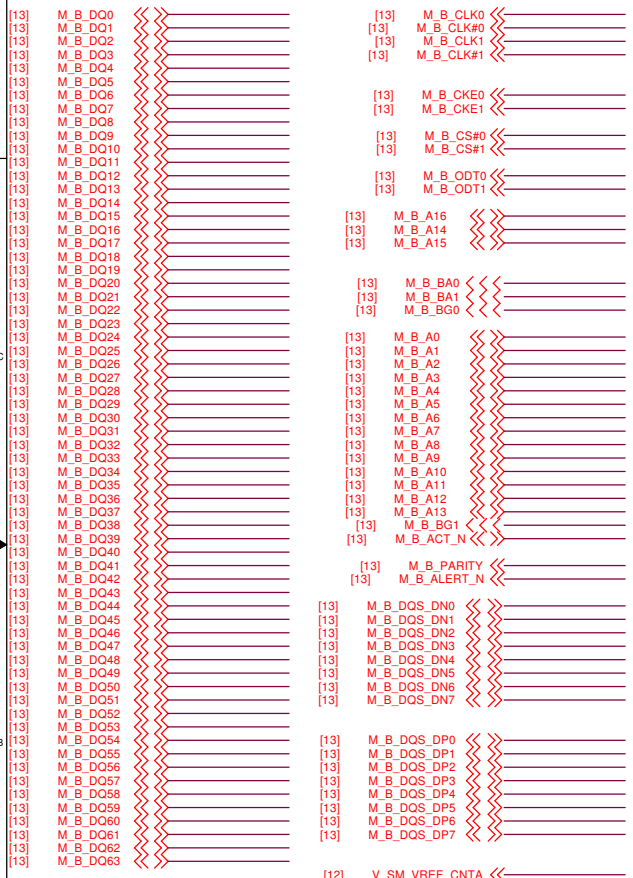


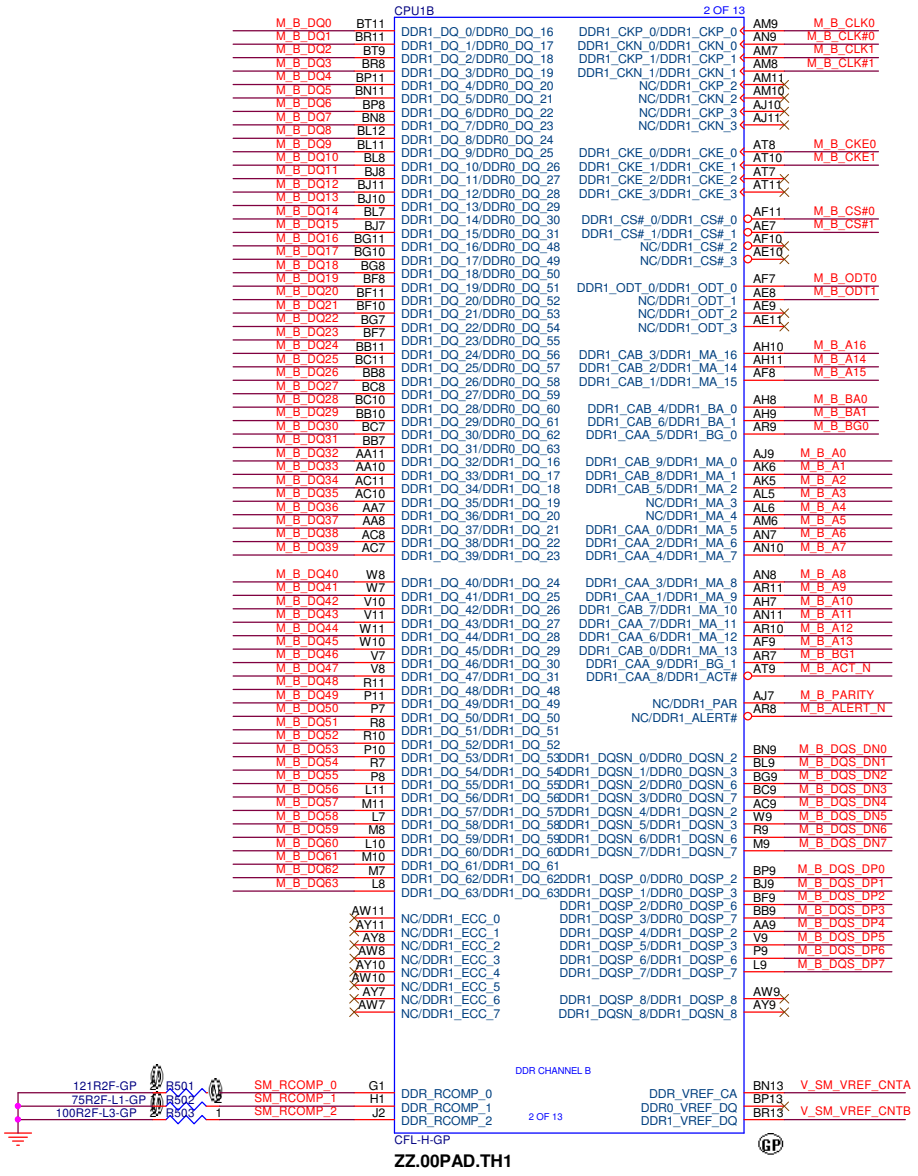
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_DDR_CHA	
Size A3	Document Number Selek CFL-H	Rev A00
Date: Thursday, April 11, 2019	Sheet 4 of 105	

SSID = CPU



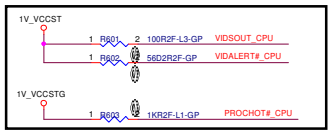


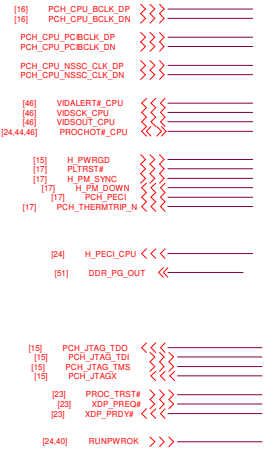
<Core Design>

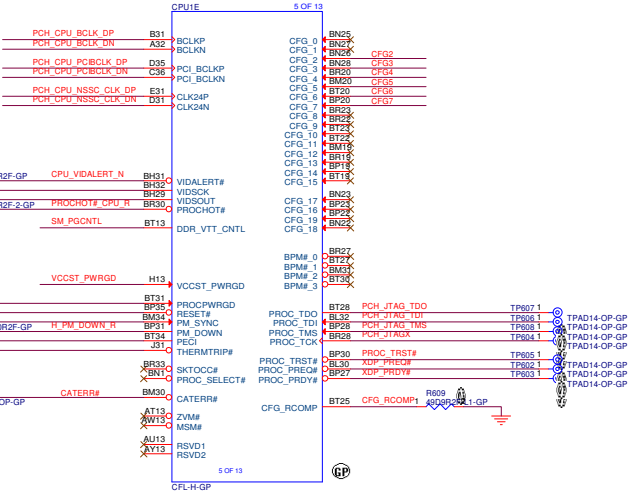
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*CPU_DDR_CHB*	
Size A3	Document Number **Selek CFL-H**	Rev **A00**
Date: Thursday, April 11, 2019	Sheet 5 of 105	

AROUND_CPU







https://vinafix.com/

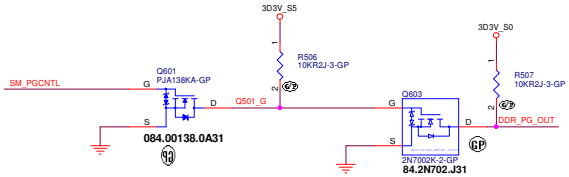
Table 6-8. Reset and Miscellaneous Signals

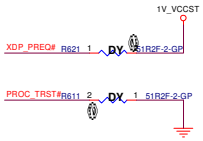
Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted: – 1 = (Default) Normal Operation; No stall. – 0 = Stall. • **CFG[1]:** Reserved configuration lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. – 1 = Normal operation – 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: – 1 = Disabled. – 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation – 00 = 1 x8, 2 x4 PCI Express* – 01 = reserved – 10 = 2 x8 PCI Express* – 11 = 1 x16 PCI Express* • **CFG[7]:** PEG Training: – 1 = (default) PEG Train immediately following RESET# de assertion. – 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

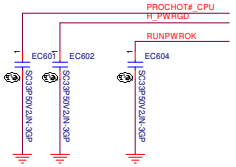
Table 13-14. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

Note: For additional information regarding SVID and power management refer to *"Power Architecture Guide"*.





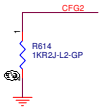


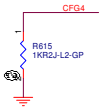
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition. 0:Lane Reversed

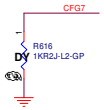
eDP Enable	
CFG4	1:Disable 0:Enable

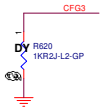
PEG Training	
CFG7	1:(default) PEG Train immediately following RESET# de assertion 0 = PEG Wait for BIOS for training.

Physical_Debug_Enabled (DFX privacy)	
CFG4	1:Disable 0:Enable (Set DXF enables bit in debug)









PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled

Processor Internal Pull-Up / Pull-Down Terminations

Processor Internal Pull-Up / Pull-Down Terminations

Signal Name	Pull Up/Pull Down	Rail	Value
BPM[3:0]	Pull Up	VCC_{IO}	16-60 Ω
PREQ# |	Pull Up	VCC_{ST}	3 kΩ
PROC_TDI	Pull Up	VCC_{STG}[1]	3 kΩ
PROC_TMS	Pull Up	VCC_{SGT}[1]	3 kΩ
CFG[19:0]	Pull Up	VCC_{IO}	3 kΩ

Note:
1. For SKL-S it should be VCC_{ST}

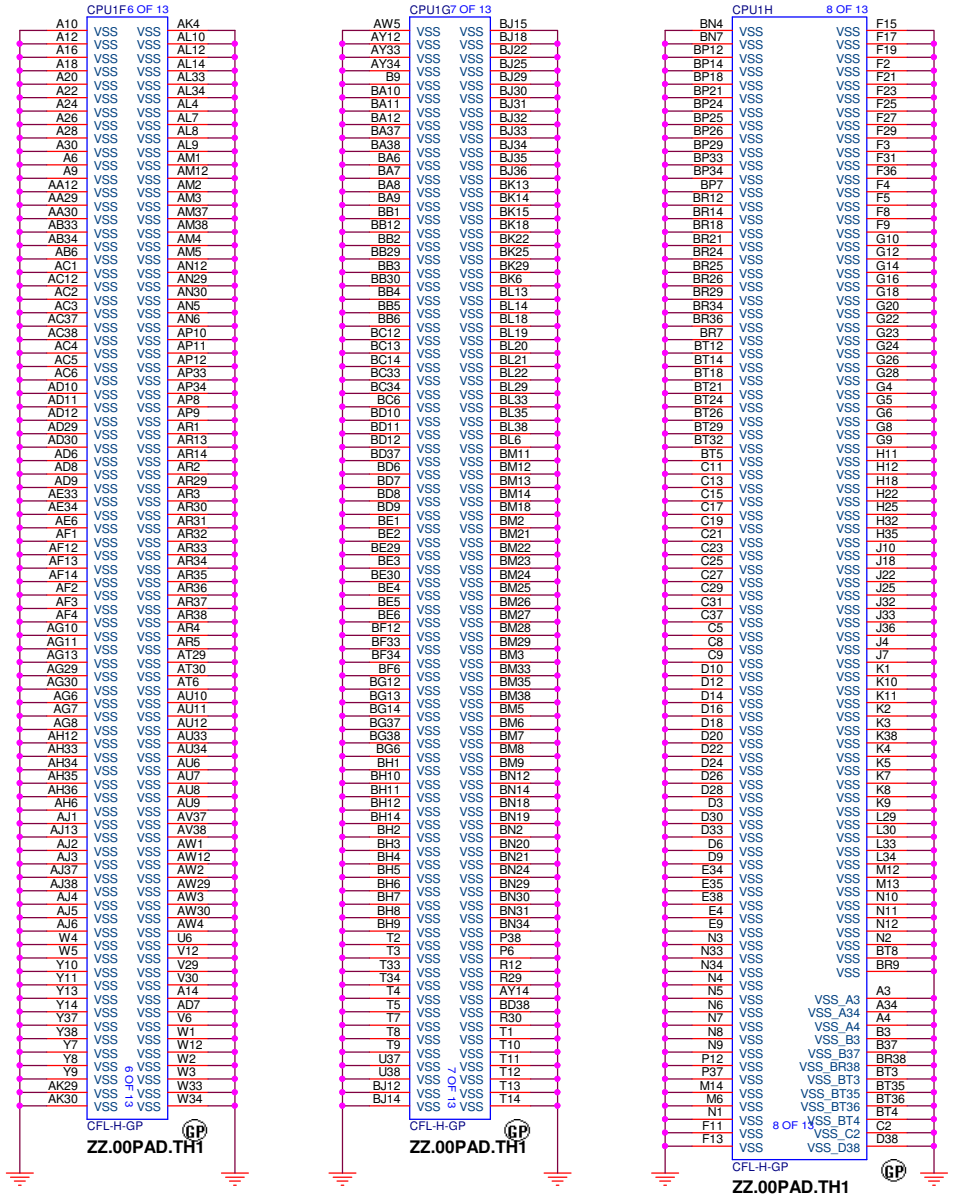
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_CFG_CFG STRAP

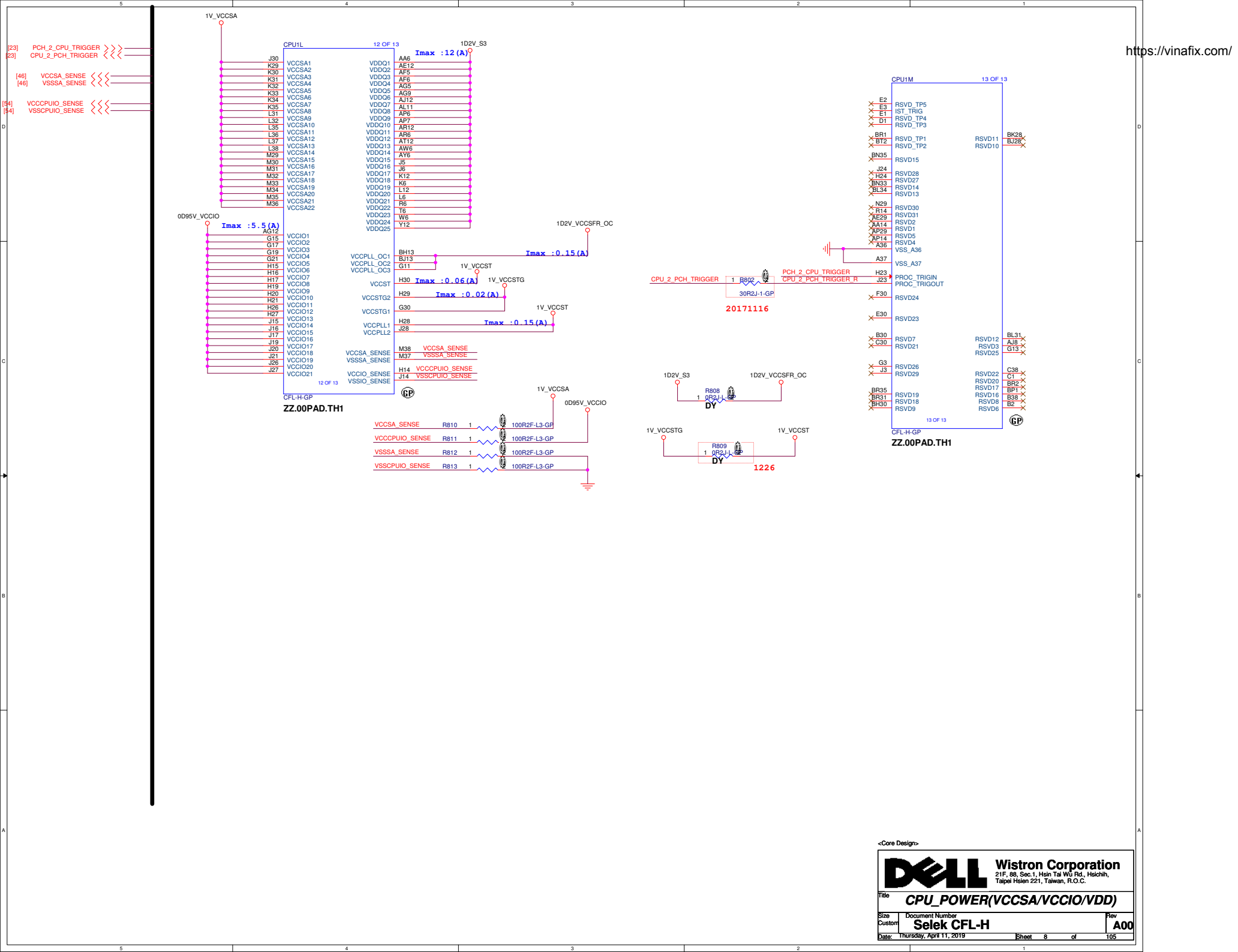
Size: A2 | Document Number: Selek CFL-H | Rev: A00

Date: Thursday, April 11, 2019 | Sheet 6 of 105



<Core Design>

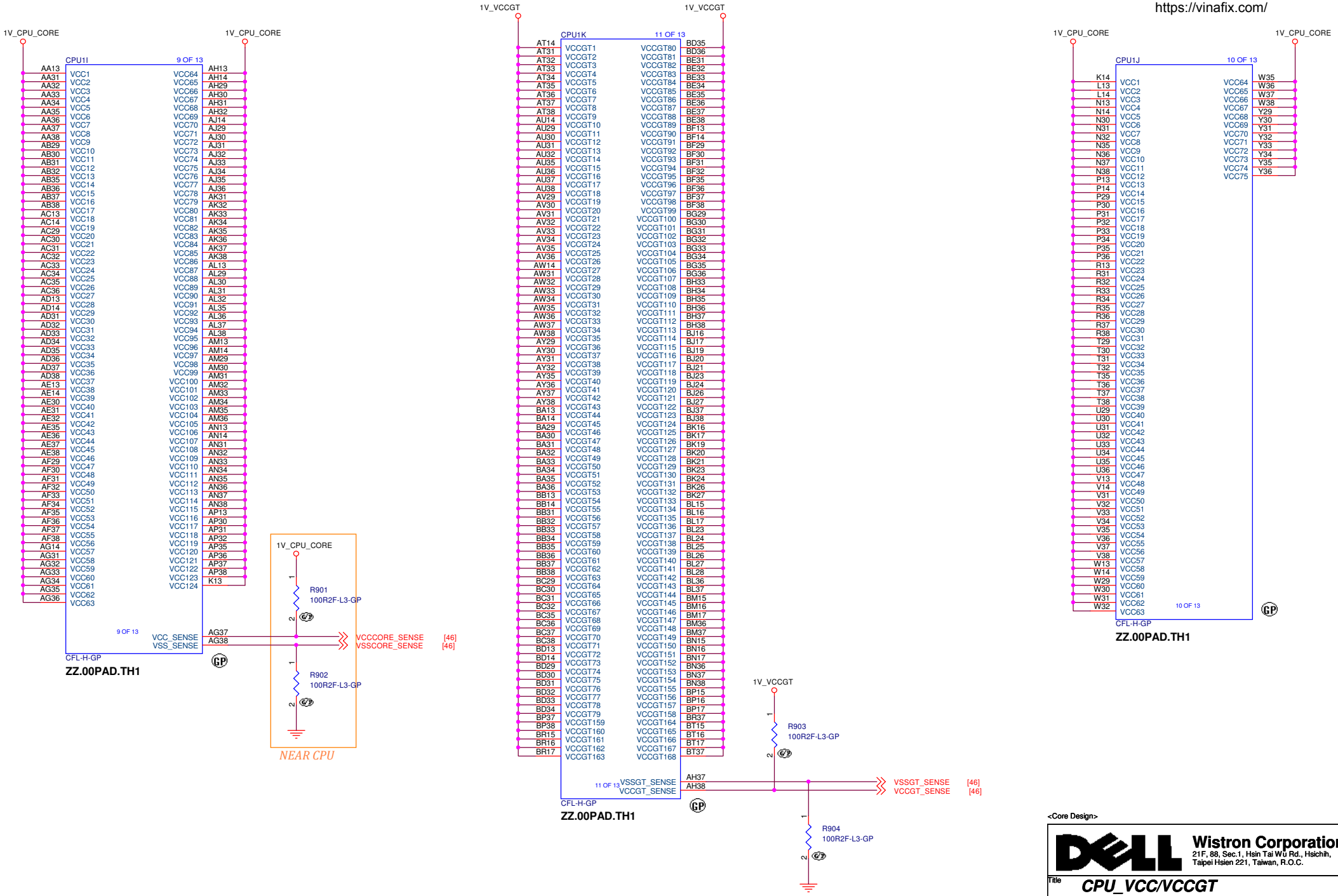
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU_GND		
Size: A3	Document Number: Selek CFL-H	Rev: A00
Date: Thursday, April 11, 2019	Sheet 7 of 105	



<Core Design>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *CPU_POWER(VCCSA/VCCIO/VDD)*		
Size: Custom	Document Number: Selek CFL-H	Rev: A00
Date: Thursday, April 11, 2019	Sheet 8 of 105	

SSID = CPU



<Core Design>

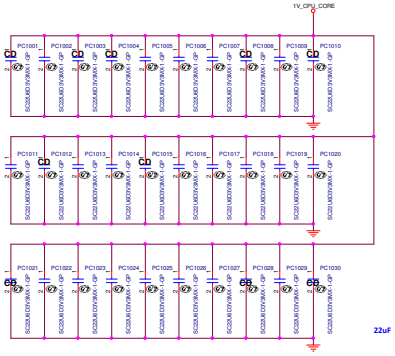
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *CPU_VCC/VCCGT*		
Size: A3	Document Number: **Selek CFL-H**	Rev: **A00**
Date: Thursday, April 11, 2019	Sheet 9 of 105	

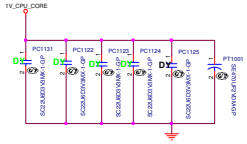
Main Func = CPU

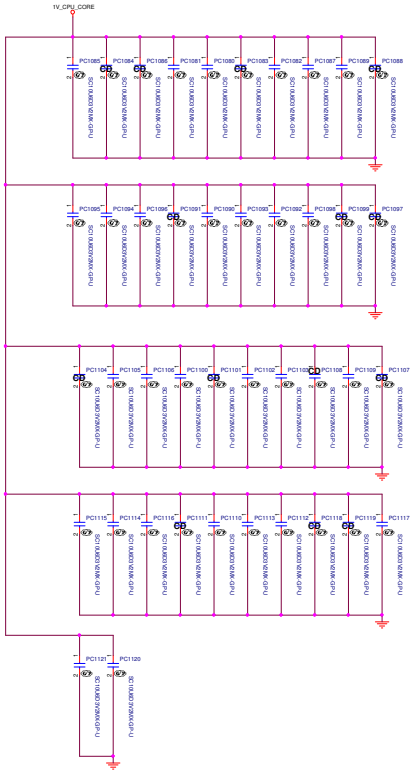
VCORE

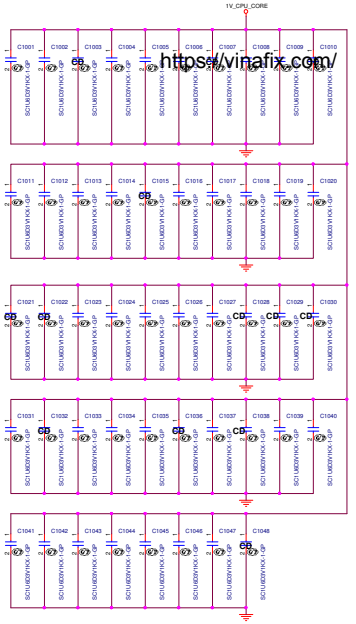
CFL-H_45W

H-line 45W
IccMax current-10ms max = 128A





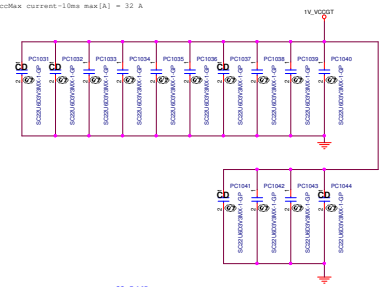


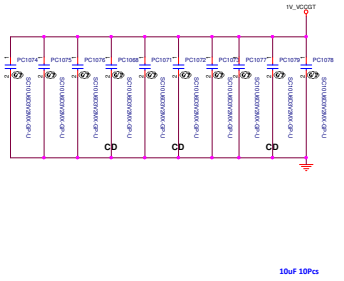


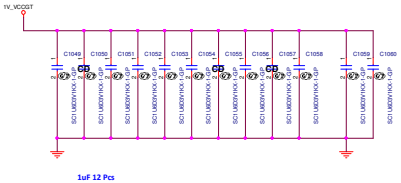
VCCGT

CFL-H_45W

IccMax current-10ms max[A] = 32 A



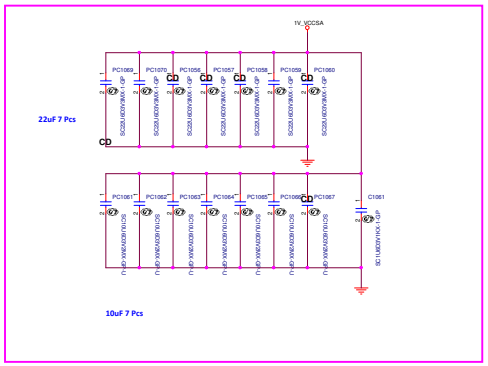


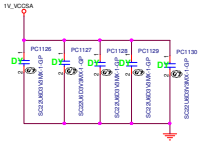


VCCSA

H-Line

IccMax current-10ms max[A] = 11.1 A





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CORE Power Cap1)

Size: A3 | Document Number: Selek CFL-H | Rev: A00

Date: Thursday, April 11, 2019 | Sheet 10 of 105

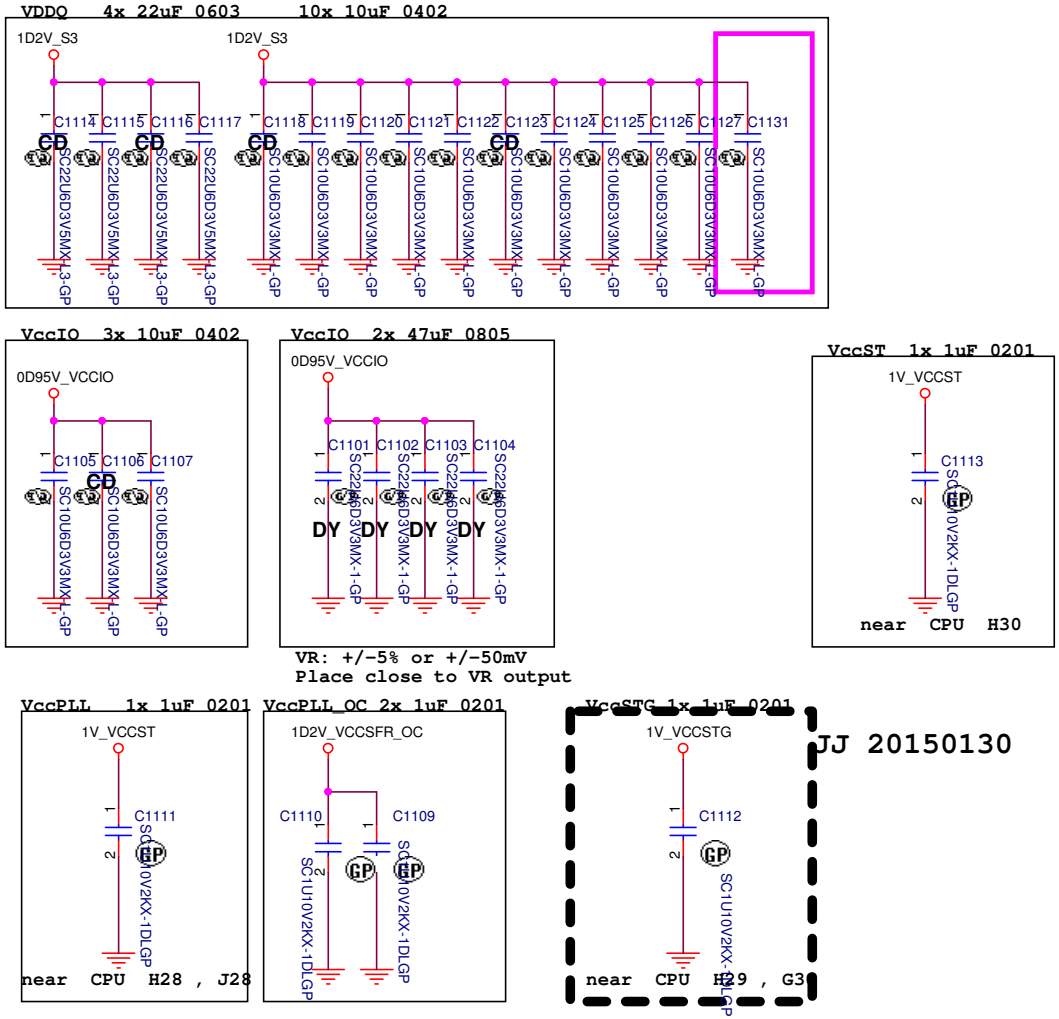


Table 50-5. Decoupling Requirements for CFL H 8+2 Processor (Sheet 1 of 2)

Domain	Board Edge cap	Backside cap	Notes
Vcc	2x 22uF 0603		
	8x 47uF 0805		
		48x 1uF 0201	
		42x 10uF 0402	
		10x 22uF 0603	
Vcc_{GT}	3x 47uF 0805		Place as close to the BGA as possible
	7x 22uF 0603		
		10x 10uF 0402	
		12x 1uF 0201	
Vcc_{SA}	2x 47uF 0805		
	2x 22uF 0603		
		7x 10uF 0402	
		1x 1uF 0201	
V_{DDQ}		4x 22uF 0603	
		11x 10uF 0402	
Vcc_{IO}		3x 10uF 0402	
		3x 0402 (placeholder)	Additional capacitors might be needed if the connectivity from BGAs to capacitors is not adequate.
Vcc_{ST}		1x 1uF 0201	Must be Ground referenced. Board routing resistance from BGA to Power gate should be less than 10mOhm. Do not route Vcc_{GT} closest adjacent layer over any power net other than ground.
Vcc_{STG}		1x 1uF 0201	Must be Ground referenced. Share with 1.0V PCH rail
Vcc_{PLL}		1x 1uF 0201	Must be Ground referenced. Share with 1.0V PCH rail. Board resistance from BGA to Power gate should be less than 130mOhm.
	1x 22uF/47uF 0805 (placeholder)		*Placeholder not stuffed. To be placed as close as possible to BGA (H28, J28) and be placed either at board edge or backside.

Domain	Board Edge cap	Backside cap	Notes
Vcc_{PLL_OC}		2x 1uF 0201	Must be Ground referenced. Share with V_{DDQ}. Board resistance from BGA to Power gate should be less than 86mOhm.

Note: High Current Rail assuming 600KHz for VR bandwidth. Higher VR bandwidth assumptions results in lower quantity of MLCC (0805/0603) to meet the same AC loadline.

Note: It is important to make sure that the noise on VCCPLL rail must be limited to the +/-5% VR specification below 150KHz - as this will potentially impact the PLL failing to phase lock. Where necessary, the 0805 placeholder can be stuffed with a 22uF or 47uF to assist noise reduction. While stuffing the 0805 cap may reduce noise coupling, one should still route the PLL rail carefully (i.e. to avoid noisy and high current rail) to mitigate any potential issue.

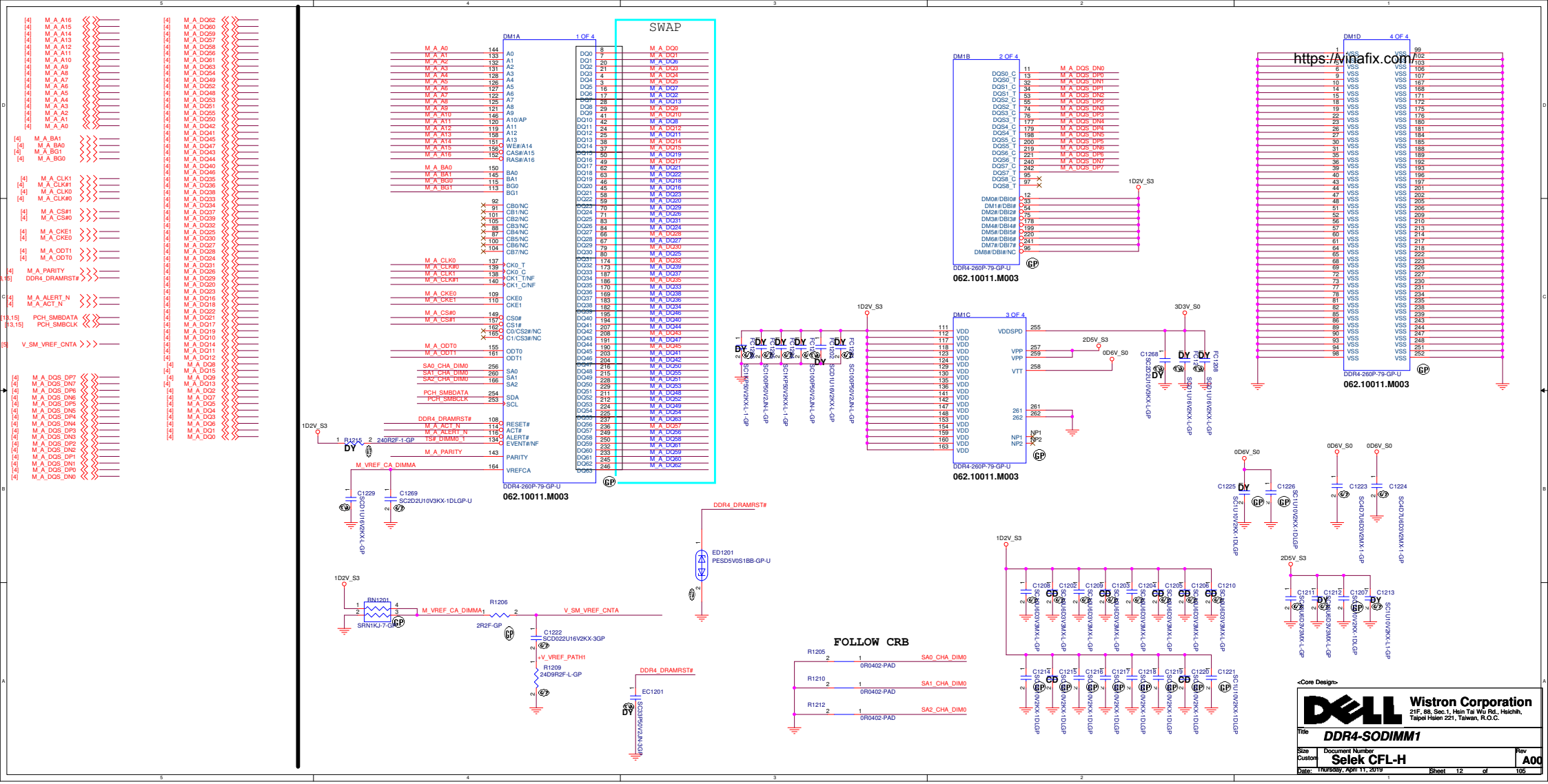
<Core Design>

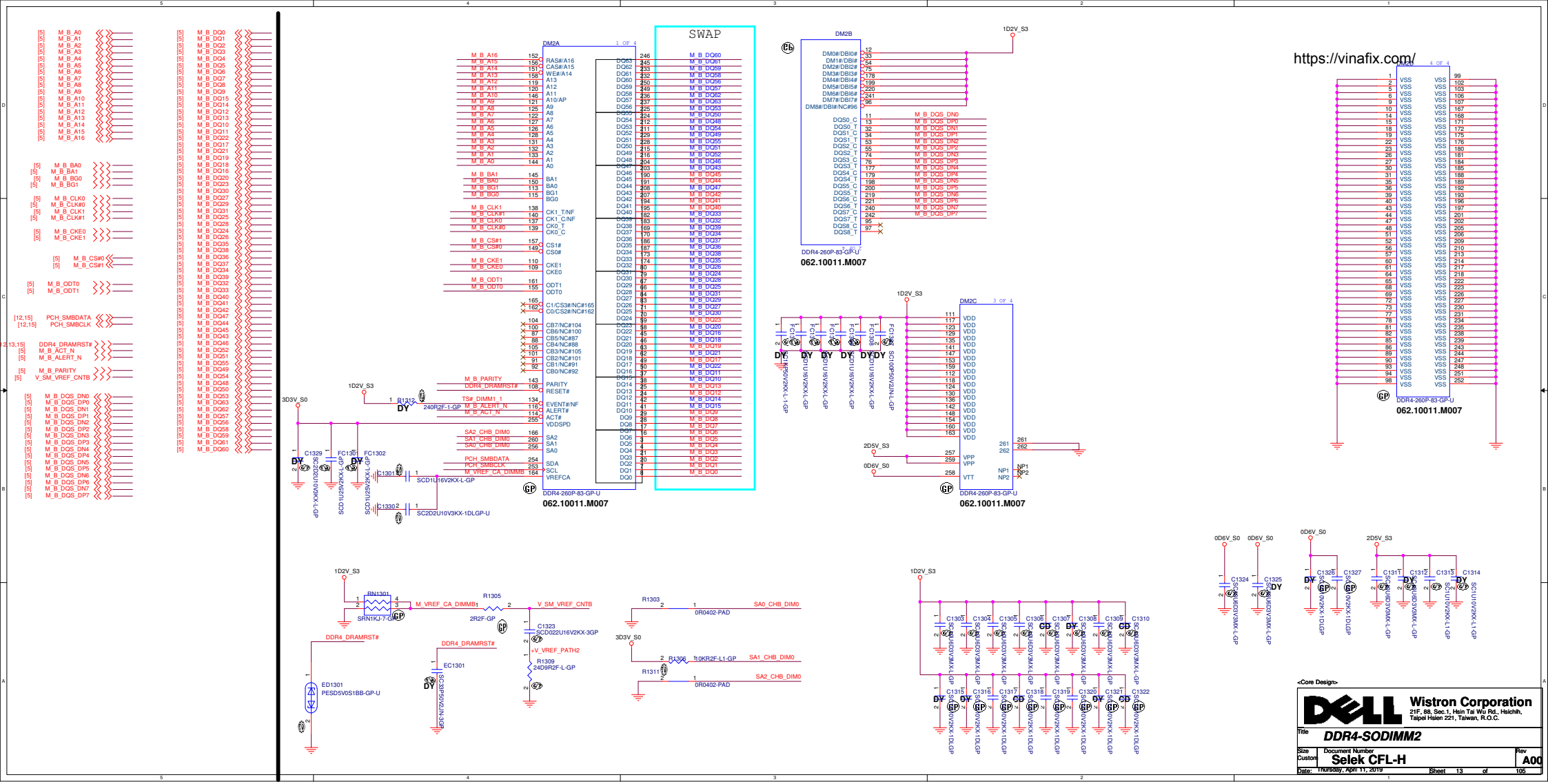
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU (Power CAP2)*

Size: Custom | Document Number: Selek CFL-H | Rev: A00

Date: Thursday, April 11, 2019 | Sheet 11 of 105




SWAP
DM2A
DM2B
DM2C
DDR4-260P-83-GP-U
062.10011.M007
https://vinafix.com/
M_B_A0
M_B_A1
M_B_A2
M_B_A3
M_B_A4
M_B_A5
M_B_A6
M_B_A7
M_B_A8
M_B_A9
M_B_A10
M_B_A11
M_B_A12
M_B_A13
M_B_A14
M_B_A15
M_B_A16
M_B_BA0
M_B_BA1
M_B_BG0
M_B_BG1
M_B_CLK0
M_B_CLK#0
M_B_CLK1
M_B_CLK#1
M_B_CKE0
M_B_CKE1
M_B_CS#0
M_B_CS#1
M_B_ODT0
M_B_ODT1
PCH_SMBDATA
PCH_SMBCLK
DDR4_DRAMRST#
M_B_ACT_N
M_B_ALERT_N
M_B_PARITY
V_SM_VREF_CNTB
M_B_DQS_DN0
M_B_DQS_DP0
M_B_DQS_DN1
M_B_DQS_DP1
M_B_DQS_DN2
M_B_DQS_DP2
M_B_DQS_DN3
M_B_DQS_DP3
M_B_DQS_DN4
M_B_DQS_DP4
M_B_DQS_DN5
M_B_DQS_DP5
M_B_DQS_DN6
M_B_DQS_DP6
M_B_DQS_DN7
M_B_DQS_DP7
M_B_DQ0
M_B_DQ1
M_B_DQ2
M_B_DQ3
M_B_DQ4
M_B_DQ5
M_B_DQ6
M_B_DQ7
M_B_DQ8
M_B_DQ9
M_B_DQ10
M_B_DQ11
M_B_DQ12
M_B_DQ13
M_B_DQ14
M_B_DQ15
M_B_DQ16
M_B_DQ17
M_B_DQ18
M_B_DQ19
M_B_DQ20
M_B_DQ21
M_B_DQ22
M_B_DQ23
M_B_DQ24
M_B_DQ25
M_B_DQ26
M_B_DQ27
M_B_DQ28
M_B_DQ29
M_B_DQ30
M_B_DQ31
M_B_DQ32
M_B_DQ33
M_B_DQ34
M_B_DQ35
M_B_DQ36
M_B_DQ37
M_B_DQ38
M_B_DQ39
M_B_DQ40
M_B_DQ41
M_B_DQ42
M_B_DQ43
M_B_DQ44
M_B_DQ45
M_B_DQ46
M_B_DQ47
M_B_DQ48
M_B_DQ49
M_B_DQ50
M_B_DQ51
M_B_DQ52
M_B_DQ53
M_B_DQ54
M_B_DQ55
M_B_DQ56
M_B_DQ57
M_B_DQ58
M_B_DQ59
M_B_DQ60
M_B_DQ61
M_B_DQ62
M_B_DQ63
M_B_DQS_DN0
M_B_DQS_DP0
M_B_DQS_DN1
M_B_DQS_DP1
M_B_DQS_DN2
M_B_DQS_DP2
M_B_DQS_DN3
M_B_DQS_DP3
M_B_DQS_DN4
M_B_DQS_DP4
M_B_DQS_DN5
M_B_DQS_DP5
M_B_DQS_DN6
M_B_DQS_DP6
M_B_DQS_DN7
M_B_DQS_DP7
1D2V_S3
3D3V_S0
0D6V_S0
2D5V_S3
R1312
240R2F-1-GP
DY
TS#_DIMM1_1
M_B_ALERT_N
M_B_PARITY
DDR4_DRAMRST#
SA2_CHB_DIM0
SA1_CHB_DIM0
SA0_CHB_DIM0
PCH_SMBDATA
PCH_SMBCLK
M_VREF_CA_DIMMB
C1329
C1330
C1301
C1302
SC2D2U10V3KX-1DLGP
SCD1U16V2KX-L-LGP
RN1301
SRN1KJ-7-GP
R1305
2R2F-GP
V_SM_VREF_CNTB
C1323
SCD022U16V2KX-3GP
+V_VREF_PATH2
R1309
24D9R2F-L-GP
DDR4_DRAMRST#
EC1301
SC33P50V2CN-3GP
ED1301
PESD5V0S1BB-GP-U
R1303
0R0402-PAD
SA0_CHB_DIM0
R1306
10KR2F-L1-GP
SA1_CHB_DIM0
R1311
0R0402-PAD
SA2_CHB_DIM0
C1303
C1304
C1305
C1306
C1307
C1308
C1309
C1310
C1315
C1316
C1317
C1318
C1319
C1320
C1321
C1322
SCD1U16V2KX-1DLGP
C1324
C1325
C1326
C1327
C1311
C1312
C1313
C1314
SC1U10V2KX-L-LGP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR4-SODIMM2
Size
Custom
Document Number
Selek CFL-H
Rev
A00
Date: Thursday, April 11, 2019
Sheet 13 of 105

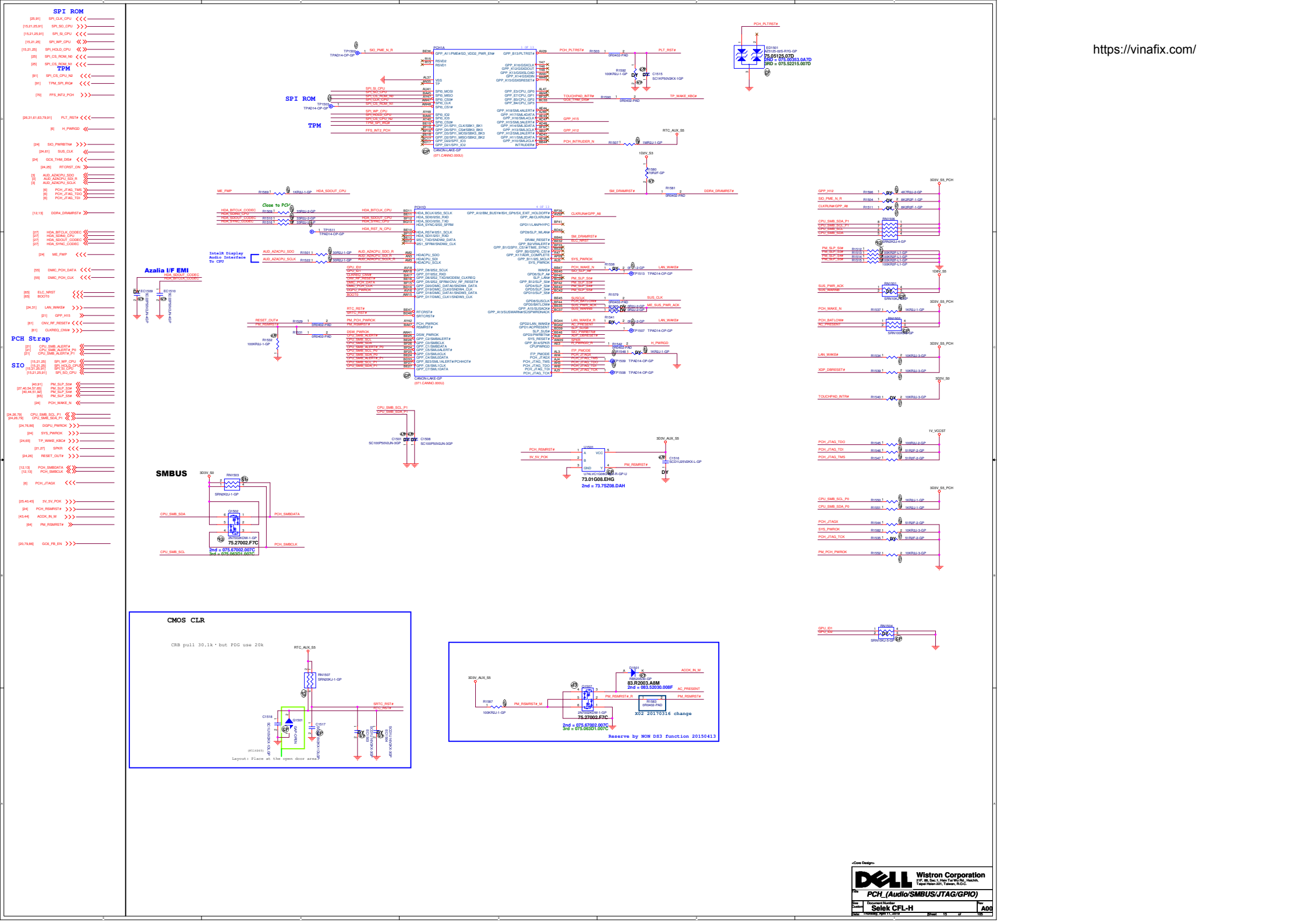
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
RESERVED

Size	Document Number	Rev
A4	**Selek CFL-H**	**A00**

Date: Thursday, April 11, 2019 Sheet 14 of 105

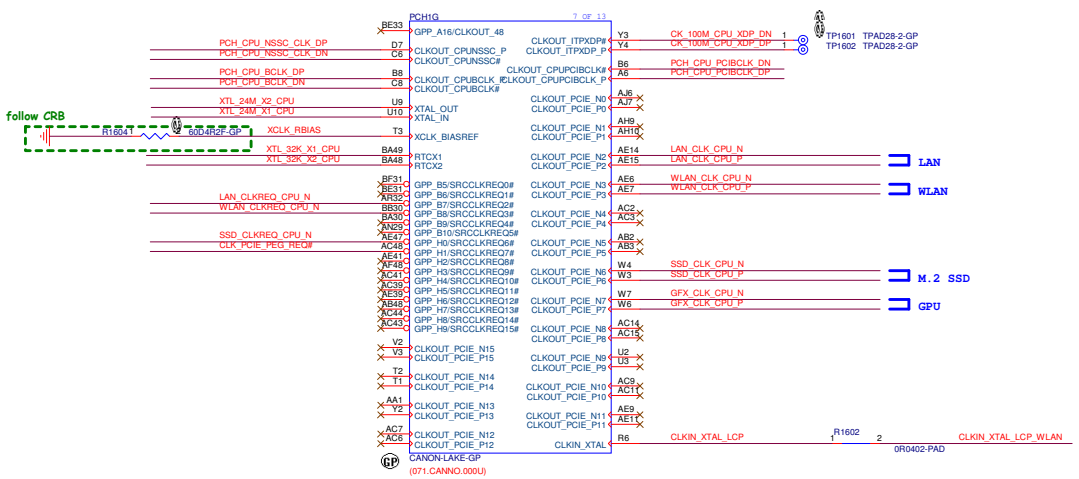


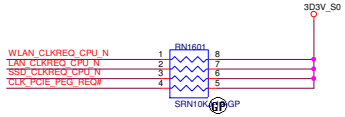
https://vinafix.com/

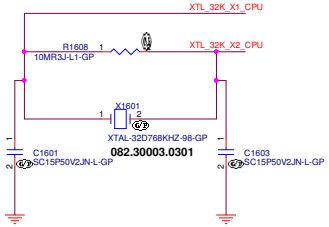
TO CPU CLOCK

[6] PCH_CPU_BCLK_DP
[6] PCH_CPU_BCLK_DN
[6] PCH_CPU_PCIBCLK_DP
[6] PCH_CPU_PCIBCLK_DN
[6] PCH_CPU_NSSC_CLK_DP
[6] PCH_CPU_NSSC_CLK_DN
[31] LAN_CLK_CPU_N
[31] LAN_CLK_CPU_P
[31] LAN_CLKREQ_CPU_N
[61] WLAN_CLK_CPU_N
[61] WLAN_CLK_CPU_P
[61] WLAN_CLKREQ_CPU_N
[63] SSD_CLK_CPU_N
[63] SSD_CLK_CPU_P
[63] SSD_CLKREQ_CPU_N
[76] GFX_CLK_CPU_N
[76] GFX_CLK_CPU_P
[76] CLK_PCIE_PEG_REQ#
[61] CLKIN_XTAL_LCP_WLAN

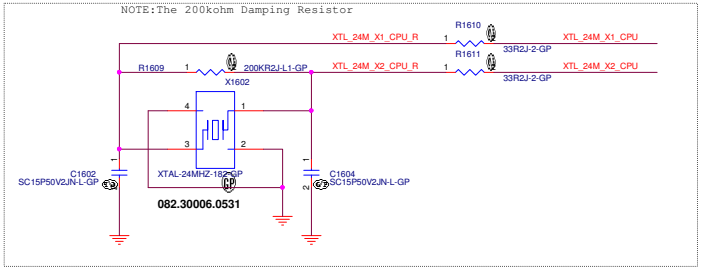
2. The SRCCLKREQ#[15:0] signals can be configured to map to any of the PCH-H PCI Express* Root Ports
3. SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements
   - SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs
   - SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs







follow PDG
Frequecy: 32.768KHz
ESR: 50kohm
CL: 12pF



follow PDG
Frequecy: 24MHz
Series Resistance :< 30ohm MAX
CL: 12pF

24 MHz Crystal Specifications (Sheet 1 of 2)

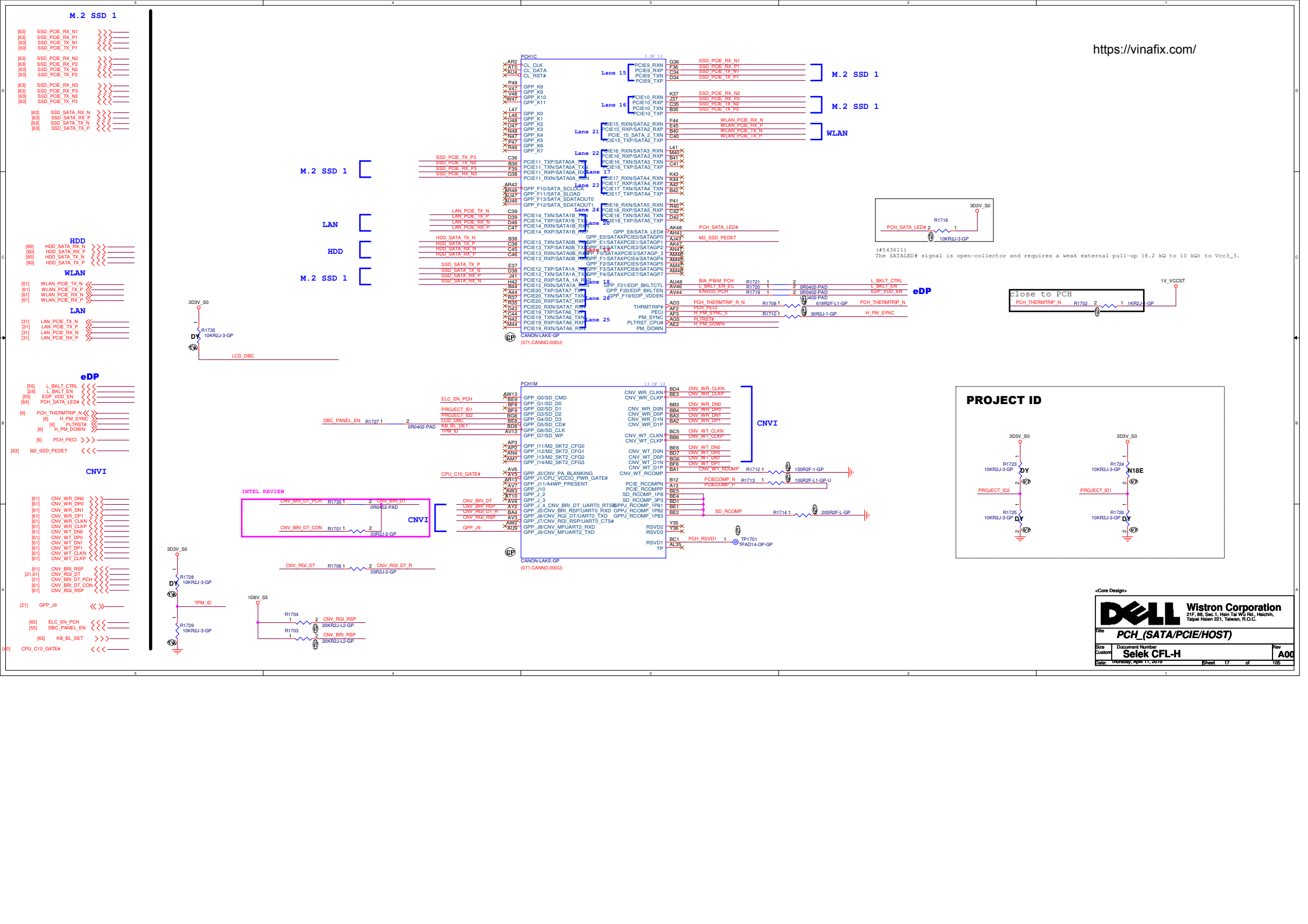
Parameter	Values	Units	Max/Min Range
Frequency	24	MHz	
Frequency Tolerance	≤ 100	PPM	
Duty Cycle Variation	+/- 5	%	
Pk to Pk jitter	≤ 150	pS	Includes cycle to cycle and period
Operating Temperature	-40 to 85	°C	

Parameter	Values	Units	Max/Min Range
Series Resistance	≤ 30	Ω	
Aging	±3	PPM	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (CLK)
Size: Custom
Document Number: Selek CFL-H
Rev: A00
Date: Thursday, April 11, 2019
Sheet 16 of 105



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_(SATA/PCIE/HOST)

Size: Custom | Document Number: Selek CFL-H | Rev: A00

Date: Thursday, April 11, 2019 | Sheet 17 of 105

[35] USB_OC0#
[35] USB_OC1#

[3] DMI_RX_CPU_P0
[3] DMI_RX_CPU_N0
[3] DMI_RX_CPU_P1
[3] DMI_RX_CPU_N1
[3] DMI_RX_CPU_P2
[3] DMI_RX_CPU_N2
[3] DMI_RX_CPU_P3
[3] DMI_RX_CPU_N3

[3] DMI_TX_CPU_P0
[3] DMI_TX_CPU_N0
[3] DMI_TX_CPU_P1
[3] DMI_TX_CPU_N1
[3] DMI_TX_CPU_P2
[3] DMI_TX_CPU_N2
[3] DMI_TX_CPU_P3
[3] DMI_TX_CPU_N3

[35] USB1_USB20_P
[35] USB1_USB20_N
[66] USB2_USB20_P
[66] USB2_USB20_N
[66] USB3_USB20_P
[66] USB3_USB20_N
[71,72] USB4_USB20_P
[71,72] USB4_USB20_N
[55] CCD_USB20_P
[55] CCD_USB20_N
[66] CARD1_USB20_P
[66] CARD1_USB20_N
[61] BT_USB20_P
[61] BT_USB20_N
[65] USB11_USB20_P
[65] USB11_USB20_N
[92] FP1_USB20_P
[92] FP1_USB20_N

[21] GPD_7

PCH1B — 2 OF 13

DMI_TX_CPU_N0 K34 DMI0_RXN
DMI_TX_CPU_P0 J35 DMI0_RXP
DMI_RX_CPU_N0 C33 DMI0_TXN
DMI_RX_CPU_P0 B33 DMI0_TXP
DMI_TX_CPU_N1 G33 DMI1_RXN
DMI_TX_CPU_P1 F34 DMI1_RXP
DMI_RX_CPU_N1 C32 DMI1_TXN
DMI_RX_CPU_P1 B32 DMI1_TXP
DMI_TX_CPU_N2 K32 DMI2_RXN
DMI_TX_CPU_P2 J32 DMI2_RXP
DMI_RX_CPU_N2 C31 DMI2_TXN
DMI_RX_CPU_P2 B31 DMI2_TXP
DMI_TX_CPU_N3 G30 DMI3_RXN
DMI_TX_CPU_P3 F30 DMI3_RXP
DMI_RX_CPU_N3 C29 DMI3_TXN
DMI_RX_CPU_P3 B29 DMI3_TXP
A25 DMI7_TXP
B25 DMI7_TXN
P24 DMI7_RXP
R24 DMI7_RXN
C26 DMI6_TXP
B26 DMI6_TXN
F26 DMI6_RXP
G26 DMI6_RXN
B27 DMI5_TXP
C27 DMI5_TXN
L26 DMI5_RXP
M26 DMI5_RXN
D29 DMI4_TXP
E28 DMI4_TXN
K29 DMI4_RXP
M29 DMI4_RXN

G17 PCIE1_RXP/USB31_7_RXN
F16 PCIE1_RXN/USB31_7_RXP
A17 PCIE1_TXP/USB31_7_TXN
B17 PCIE1_TXN/USB31_7_TXP
R21 PCIE2_RXP/USB31_8_RXN
P21 PCIE2_RXN/USB31_8_RXP
B18 PCIE2_TXP/USB31_8_TXN
C18 PCIE2_TXN/USB31_8_TXP
K18 PCIE3_RXP/USB31_9_RXN
J18 PCIE3_RXN/USB31_9_RXP
B19 PCIE3_TXP/USB31_9_TXN
C19 PCIE3_TXN/USB31_9_TXP
N18 PCIE4_RXP/USB31_10_RXN
R18 PCIE4_RXN/USB31_10_RXP
D20 PCIE4_TXP/USB31_10_TXN
C20 PCIE4_TXN/USB31_10_TXP
F20 PCIE5_RXP
G20 PCIE5_RXN
B21 PCIE5_TXP
A22 PCIE5_TXN
K21 PCIE6_RXP
J21 PCIE6_RXN
D21 PCIE6_TXP
C21 PCIE6_TXN
B23 PCIE7_RXP
C23 PCIE7_RXN
J24 PCIE7_TXP
L24 PCIE7_TXN
F24 PCIE8_RXP
G24 PCIE8_RXN
B24 PCIE8_TXP
C24 PCIE8_TXN

CANON-LAKE-GP
(071.CANNO.000U)

J3 USB1_USB20_N
J2 USB1_USB20_P
N13 USB2_USB20_N
N15 USB2_USB20_P
K4 USB3_USB20_N
K3 USB3_USB20_P
M10 USB4_USB20_N
L9 USB4_USB20_P
M1 CCD_USB20_N
L2 CCD_USB20_P
K7 CARD1_USB20_N
K6 CARD1_USB20_P
L4
L3
G4
G5
M6 FP1_USB20_N
N8 FP1_USB20_P
H3
H2
R10 USB11_USB20_N
P9 USB11_USB20_P
G1
G2
N3
N2
E5 BT_USB20_N
F6 BT_USB20_P

USB3.0 Type A
USB2.0 Type A IO Board
USB2.0 Type A IO Board
Type c
Camera
Cardreader
Finger Print
RGB Keyboard
BT

AH36 USB_OC0#
AL40 USB_OC1#
AJ44 USB_OC2#
AL41 USB_OC3#
AV47 USB_OC4#
AR35 USB_OC5#
AR37 USB_OC6#
AV43 USB_OC7#

GPP_E9/USB2_OC0#
GPP_E10/USB2_OC1#
GPP_E11/USB2_OC2#
GPP_E12/USB2_OC3#
GPP_F15/USB2_OC4#
GPP_F16/USB2_OC5#
GPP_F17/USB2_OC6#
GPP_F18/USB2_OC7#

F4 USB2_COMP
F3 USB2_VBUSSENSE
U13
G3 USB2_ID
BE41 GPD_7

USB2_COMP
USB2_VBUSSENSE
RSVD1
USB2_ID
GPD7

R1802 1 — 113R2F-GP

Lane 30 PCIE24_TXP G45
PCIE24_TXN G46
PCIE24_RXP Y41
PCIE24_RXN G48
Lane 29 PCIE23_TXP G49
PCIE23_TXN W44
PCIE23_RXP W43
PCIE23_RXN H48
Lane 28 PCIE22_TXP H47
PCIE22_TXN U41
PCIE22_RXP U40
PCIE22_RXN F46
Lane 27 PCIE21_TXP G47
PCIE21_TXN R44
PCIE21_RXP T43
PCIE21_RXN

Lane 11
Lane 12
Lane 13
Lane 14

3D3V_S5_PCH
RN1804
SRN10KJ-6-GP
USB_OC0#
USB_OC2#
USB_OC3#
USB_OC1#

3D3V_S5_PCH
RN1801
SRN10KJ-6-GP
USB_OC6#
USB_OC5#
USB_OC7#
USB_OC4#

RN1802
SRN1KJ-7-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_(DMI/USB2/USB3/PCIE)
Size: Custom
Document Number: Selek CFL-H
Rev: A00
Date: Thursday, April 11, 2019
Sheet 18 of 105

[19,60] HDD_DEVSLP
[71,72] CPU_DP_HPD_R
[55] EDP_HPD
[19,60] HDD_DEVSLP
[63] mSATA_DEVSLP
[24,68] ESPI_IO[3..0]
[35] USB1_USB30_TX_N
[35] USB1_USB30_TX_P
[35] USB1_USB30_RX_N
[35] USB1_USB30_RX_P
[71] USB4_USB30_TX_P
[71] USB4_USB30_TX_N
[71] USB4_USB30_RX_P
[71] USB4_USB30_RX_N
[24,68] ESPI_CS#
[24,68] ESPI_RESET#
[24,68] ESPI_CLK
[91] PIRQA#

3D3V_S0
CPU_DP_CTRL_CLK
CPU_DP_CTRL_DATA
RN1902
SRN2K2J-4-GP

Add RTC Gen 9 reset circuit_20170814
leakage issue

https://vinafix.com/

3D3V_S5_PCH
RTC_RST
R1906 10KR2J-3-GP
R1905 10KR2J-3-GP
Q1901
CPU_DDI1HPD
CPU_DP_HPD_R
CPU_DP_HPD_P
common part 2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C
R1907 100KR2J-1-GP
DY
SB_0403

CPU_DDI1HPD
R1902 100KR2J-1-GP

PCH1E
5 OF 13
CPU_DDI1HPD
EDP_HPD
GPP_I0/DDPB_HPD0/DISP_MISC0
GPP_I1/DDPC_HPD1/DISP_MISC1
GPP_I2/DPPD_HPD2/DISP_MISC2
GPP_I3/DPPE_HPD3/DISP_MISC3
GPP_I4/EDP_HPD/DISP_MISC4
GPP_I5/DDPB_CTRLCLK
GPP_I6/DDPB_CTRLDATA
GPP_I7/DDPC_CTRLCLK
GPP_I8/DDPC_CTRLDATA
GPP_I9/DDPD_CTRLCLK
GPP_I10/DDPD_CTRLDATA
GPP_F23/DDPF_CTRLDATA
GPP_F22/DDPF_CTRLCLK
GPP_F14/EXT_PWR_GATE#/PS_ON#
GPP_K23/IMGCLKOUT1
GPP_K22/IMGCLKOUT0
GPP_K21
GPP_K20
GPP_H23/TIME_SYNC0
CPU_DP_CTRL_CLK
CPU_DP_CTRL_DATA
PCIAUX_GATE
PROC_DETECT#
TP1901 TPAD28-2-GP
CANON-LAKE-GP
(071.CANNO.000U)

6.3.3 Embedded DisplayPort* Hot-Plug Detect Implementation

Hot-plug detect (HPD) is an output from eDP* sink device and it is a active high signal.

Note: When using eDP bifurcation for DP-VGA Topology, need to use HPD for DDIE (DDPE_HPD) for HPD connectivity.

For eSPI

ESPI_IO[3..0]
ESPI_IO0 R1921 15R2F-2-GP ESPI_IO0_R
ESPI_IO1 R1922 15R2F-2-GP ESPI_IO1_R
ESPI_IO2 R1923 15R2F-2-GP ESPI_IO2_R
ESPI_IO3 R1924 15R2F-2-GP ESPI_IO3_R

3D3V_S5_PCH
PROC_DETECT# R1920 20KR2J-L2-GP
3D3V_S0
PIRQA# R19111 10KR2J-3-GP
ESPI_RESET# R1919 DY 100KR2J-1-GP

USB3.0 Type A
USB3.1 Type c

PCH1F
6 OF 13
USB1_USB30_TX_N
USB1_USB30_TX_P
USB1_USB30_RX_N
USB1_USB30_RX_P
USB4_USB30_TX_P
USB4_USB30_TX_N
USB4_USB30_RX_P
USB4_USB30_RX_N
USB31_1_TXN
USB31_1_TXP
USB31_1_RXN
USB31_1_RXP
USB31_2_TXN
USB31_2_TXP
USB31_2_RXN
USB31_2_RXP
USB31_6_TXN
USB31_6_TXP
USB31_6_RXN
USB31_6_RXP
USB31_5_TXN
USB31_5_TXP
USB31_5_RXN
USB31_5_RXP
USB31_3_TXP
USB31_3_TXN
USB31_3_RXP
USB31_3_RXN
USB31_4_TXP
USB31_4_TXN
USB31_4_RXP
USB31_4_RXN
Lane 1
Lane 2
Lane 6
Lane 5
Lane 3
Lane 4
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS0#
GPP_A6/SERIRQ/ESPI_CS1#
GPP_A7/PIRQA#/ESPI_ALERT0#
GPP_A0/RCIN#/ESPI_ALERT1#
GPP_A14/SUS_STAT#/ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_K19/SMI#
GPP_K18/NMI#
GPP_E6/SATA_DEVSLP2
GPP_E5/SATA_DEVSLP1
GPP_E4/SATA_DEVSLP0
GPP_F9/SATA_DEVSLP7
GPP_F8/SATA_DEVSLP6
GPP_F7/SATA_DEVSLP5
GPP_F6/SATA_DEVSLP4
GPP_F5/SATA_DEVSLP3
ESPI_IO0_R
ESPI_IO1_R
ESPI_IO2_R
ESPI_IO3_R
ESPI_CS#
PIRQA#
ESPI_RESET#
ESPI_CLK_R
mSATA_DEVSLP
HDD_DEVSLP
CANON-LAKE-GP
(071.CANNO.000U)

ESPI_CLK_R R19141 33R2F-3-GP ESPI_CLK
DY
SCC1P50V2JN-4GP
ESC1P50

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_(DDI/USB3/GPIO)
Size: Custom
Document Number: Selek CFL-H
Rev: A00
Date: Thursday, April 11, 2019
Sheet 19 of 105

[79] GPU_EVENT#
[25] RTC_DET#_PCH
[24] SIO_EXT_WAKE#
[79,86] GC6_FB_EN
[79,86] GC6_FB_EN
[65] KB_DET#
[70] SKP_ID
[70] GSEN2_INT1_PCH
[70] GSEN2_INT2_PCH
[70] FFS_INT1
[65,68] UART_2_CTXD_DRXD
[65,68] UART_2_CRXD_DTXD
[61] BT_RADIO_DIS#

TOUCH PAD

[65,66] CPU_I2C_SCL_P1
[65,66] CPU_I2C_SDA_P1
[24] TABLE_MODE#
[79] DGPU_HOLD_RST#
[61] WLAN_WIGIG60GHZ_DIS#
[86] DGPU_PWR_EN
[61] CNV_DET#
[70] CPU_I2C_SCL_ISH
[70] CPU_I2C_SDA_ISH
[57,77] HDMI_HPD_GPU

PCH1K 11 OF 13

BBS_BIT0 BA26 GPP_B22/GSPI1_MOSI
BD30 GPP_B21/GSPI1_MISO
SIO_EXT_SCI# AU26 GPP_B20/GSPI1_CLK
FFS_INT1 AW26 GPP_B19/GSPI1_CS0#
NRB_BIT BE30 GPP_B18/GSPI0_MOSI
BD29 GPP_B17/GSPI0_MISO
GC6_FB_EN_MCP BP29 GPP_B16/GSPI0_CLK
GPU_EVENT# BB26 GPP_B15/GSPI0_CS0#
BB24 GPP_C9/UART0_TXD
SKP_ID BE23 GPP_C8/UART0_RXD
AP24 GPP_C11/UART0_CTS#
BT_RADIO_DIS# BA24 GPP_C10/UART0_RTS#
BD21 GPP_C15/UART1_CTS#/ISH_UART1_CTS#
HDMI_HPD_PCH AW24 GPP_C14/UART1_RTS#/ISH_UART1_RTS#
AP21 GPP_C13/UART1_TXD/ISH_UART1_TXD
AU24 GPP_C12/UART1_RXD/ISH_UART1_RXD
AV21 GPP_C23/UART2_CTS#
SIO_EXT_WAKE# AW21 GPP_C22/UART2_RTS#
UART_2_CTXD_DRXD BE20 GPP_C21/UART2_TXD
UART_2_CRXD_DTXD BD20 GPP_C20/UART2_RXD
BE21 GPP_C19/I2C1_SCL
CPU_I2C_SCL_P1 BF21 GPP_C18/I2C1_SDA
CPU_I2C_SDA_P1 BC22 GPP_C17/I2C0_SCL
BF23 GPP_C16/I2C0_SDA
BE15 GPP_D4/ISH_I2C2_SDA/I2C3_SDA/SBK4_BK4
BE14 GPP_D23/ISH_I2C2_SCL/I2C3_SCL

GPP_B22/GSPI1_MOSI BA20 GPP_D9/ISH_SPI_CS#/GSPI2_CS0#
GPP_B21/GSPI1_MISO BB20 GPP_D10/ISH_SPI_CLK/GSPI2_CLK
GPP_B20/GSPI1_CLK BB16 GPP_D11/ISH_SPI_MISO/GP_BSSB_CLK/GSPI2_MISO
GPP_B19/GSPI1_CS0# AN18 GPP_D12/ISH_SPI_MOSI/GP_BSSB_DI/GSPI2_MOSI
GPP_B18/GSPI0_MOSI BE14 GPP_D16/ISH_UART0_CTS#/CNV_WCEN
GPP_B17/GSPI0_MISO AR18 GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/CNV_WFEN
GPP_B16/GSPI0_CLK BF17 GPP_D14/ISH_UART0_TXD/I2C2_SCL
GPP_B15/GSPI0_CS0# BE17 GPP_D13/ISH_UART0_RXD/I2C2_SDA
GPP_C9/UART0_TXD
GPP_C8/UART0_RXD
GPP_C11/UART0_CTS#
GPP_C10/UART0_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS# AG45 GPP_H20/ISH_I2C0_SCL
GPP_C14/UART1_RTS#/ISH_UART1_RTS# AH46 GPP_H19/ISH_I2C0_SDA
GPP_C13/UART1_TXD/ISH_UART1_TXD AH47
GPP_C12/UART1_RXD/ISH_UART1_RXD AH48 GPP_H22/ISH_I2C1_SCL
GPP_H21/ISH_I2C1_SDA
GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C21/UART2_TXD AV34
GPP_C20/UART2_RXD AW32 GPP_A23/ISH_GP5
BA33 GPP_A22/ISH_GP4
GPP_C19/I2C1_SCL BE34 GPP_A21/ISH_GP3
GPP_C18/I2C1_SDA BD34 GPP_A20/ISH_GP2
GPP_C17/I2C0_SCL BF35 GPP_A19/ISH_GP1
GPP_C16/I2C0_SDA BD38 GPP_A18/ISH_GP0
GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7
GPP_D4/ISH_I2C2_SDA/I2C3_SDA/SBK4_BK4
GPP_D23/ISH_I2C2_SCL/I2C3_SCL

CANON-LAKE-GP
(071.CANNO.000U)

GC6_FB_EN R2046 1 2 0R0402-PAD
HDMI_HPD_GPU R2031 1 2 0R0402-PAD
CPU_I2C_SCL_ISH0 R2058 1 2 0R0402-PAD CPU_I2C_SCL_ISH
CPU_I2C_SDA_ISH0 R2059 1 2 0R0402-PAD CPU_I2C_SDA_ISH
TABLE_MODE#_PCH R2062 1 DY 2 0R2J-L-GP TABLE_MODE#
KB_DET# R2061 1 2 0R0402-PAD GSEN2_INT2_PCH
GSEN2_INT1_ISH R2060 1 2 0R0402-PAD GSEN2_INT1_PCH
DGPU_HOLD_RST# R2013 1 2 10KR2F-L1-GP
DGPU_PWR_EN R2014 1 2 10KR2F-L1-GP
R2057 1 2 10KR2F-L1-GP DY
BBS_BIT0 R2015 1 DY 2 10KR2F-L1-GP
CPU_I2C_SDA_ISH0 CPU_I2C_SCL_ISH0 RN2007 SRN1KJ-GP
KB_DET# R2045 2 1 10KR2J-3-GP
TABLE_MODE#_PCH R2063 2 DY 1 10KR2J-3-GP

TOUCH PAD

3D3V_S5_PCH
R2042 1 2 10KR2J-3-GP GPU_EVENT#
3D3V_S5_PCH
R2041 1 2 10KR2J-3-GP SIO_EXT_WAKE#
3D3V_S0
R2001 1 2 10KR2J-3-GP SIO_EXT_SCI#
RN2010 1 2 DY 4 3 CPU_I2C_SDA_P1 CPU_I2C_SCL_P1 SRN2K2J-1-GP
51KR2J-1-GP 1 DEBUG R2056 UART_2_CRXD_DTXD
51KR2J-1-GP 1 DEBUG R2055 UART_2_CTXD_DRXD

UART_2_CRXD_DTXD 1 R2030 2 DY 0R2J-L-GP CNV_DET#

Assign CNV_DET# for reserved

PHASE ID

3D3V_S0
R2050 10KR2J-3-GP DY BOARD_ID_2
R2049 10KR2J-3-GP DY
3D3V_S0
R2051 10KR2J-3-GP DY BOARD_ID_1
R2048 10KR2J-3-GP DY

1D8V_S0
R2002 10KR2F-L1-GP
1D8V_S0
Q2001 G S PJA138KA-GP D
3D3V_S0
R2003 10KR2F-L1-GP
TABLE_MODE#_PCH
TABLE_MODE#

3D3V_S5_PCH 1214
R2047 1KR2J-1-GP DY
NRB_BIT
R2019 1KR2J-1-GP DY

R2052 1 HDMI_HPD_PCH
100KR2J-1-GP

1D8V_S0
1D8V_S5

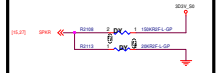
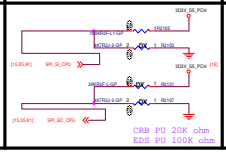
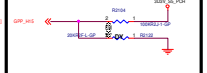
<Core Design>

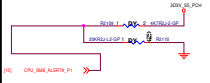
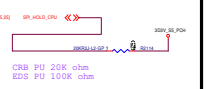
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

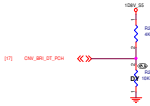
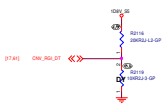
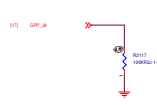
Title: PCH_(UART/GPIO/I2C)
Size: Custom
Document Number: Selek CFL-H
Rev: A00
Date: Thursday, April 11, 2019
Sheet 20 of 105

CNL_H_DDR4_4PH_VR_RVP_SCH_Rev1p0

CRB P.103 P.104

GPIO	GPP_B14 SPKR	GPP_B18 GSPIO_MOSI	GPP_C2 SMBALERT#	GPP_B22 GSPI1_MOSI	GPP_C5 SM0ALERT#	SPI0_MOSI SPI0_MISO	GPP_H15 SML3ALERT#
Schematic		default is internal pull down add TP at PCH side		default is internal pull down add TP at PCH side		 CRB PU 20K ohm EDS PU 100K ohm	

GPIO	GPP_B23 SML1ALERT# PCHHOT#	SPI0_IO2	SPI0_IO3	HDA_SDO I2S0_TXD	GPP_H12 SML2ALERT#	GPP_I6 DDPB_CTRLDATA	GPP_I8 DDPC_CTRLDATA
Schematic		 CRB PU 20K ohm EDS PU 100K ohm	 CRB PU 20K ohm EDS PU 100K ohm		GPP_H_12 add TP at PCH side	DDPB_CTRLDATA PU at Page.19	weak internal Pull-down.

GPIO	GPP_I10 DDPD_CTRLDATA	GPP_F23 DPPF_CTRLDATA	GPP_J4 CNV_BRI_DT UART0_RTS#	GPP_J6 CNV_RGI_DT UART0_TXD	GPP_J9	GPD7
Schematic	weak internal Pull-down.	weak internal pull-down.				

Signal	Usage	When Sampled	Comment
GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal Pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block (the opposite 64-KB block from the one it did invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap . **Notes:** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The state of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal Pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. **Notes:** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal Pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite confidentiality. (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite confidentiality. Must be pulled up to support Intel AMT with TLS. **Notes:** 1. The internal Pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

Signal	Usage	When Sampled	Comment
GPP_B23 / GSPI1_MOSI	Boot BIOS Strap Bit (BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function1, offset DCh, bit 6). **Bit 6 — Boot BIOS Destination** 0 — SPI (Default) 1 — LPC **Notes:** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected and descriptor in the SPI flash with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
GPP_C5 / SM1ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. **Warning: If this strap is configured to '0' (eSPI is disabled), the eSPI Flash Sharing Mode strap must be configured to '0' as well (SAFS is disabled)**
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_H15 / SML3ALERT#	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_B23 / SML1ALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down: 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

Signal	Usage	When Sampled	Comment
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external PU/D up in manufacturing/debug environments ONLY. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H12 / SML2ALERT#	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default). 1 = Slave Attached Flash Sharing (SAFS) enabled. **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. **Warning: This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC strap is configured to '0' (eSPI is disabled)**
GPP_I6 / DDPB_CTRLDATA	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_I8 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_I10 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_F23	Display Port F Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port F is not detected. (Default) 1 = Port F is detected. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.

Signal	Usage	When Sampled	Comment
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
GPP_J9	1.8V VCCSPI	Rising edge of RSMRST#	The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail **Note:** If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os
GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

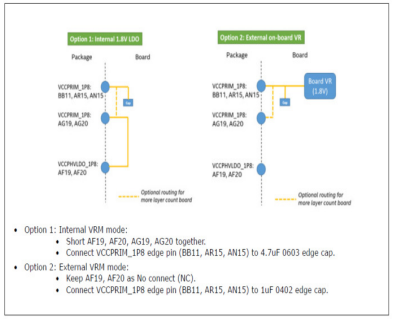
PCH_(Strap Pin)

Size: C | Document Number: Selek CFL-H | Rev: A00

Date: Thursday, April 11, 2019 | Sheet 35 of 38

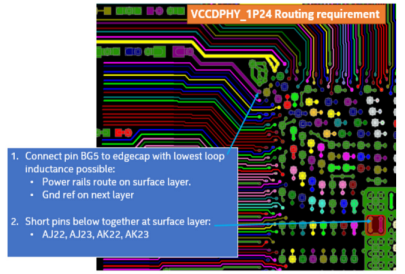
VCCDPHY_1P24	**1.24V for CNVi logic**. This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC. Refer to the Platform Design Guide for implementation details.

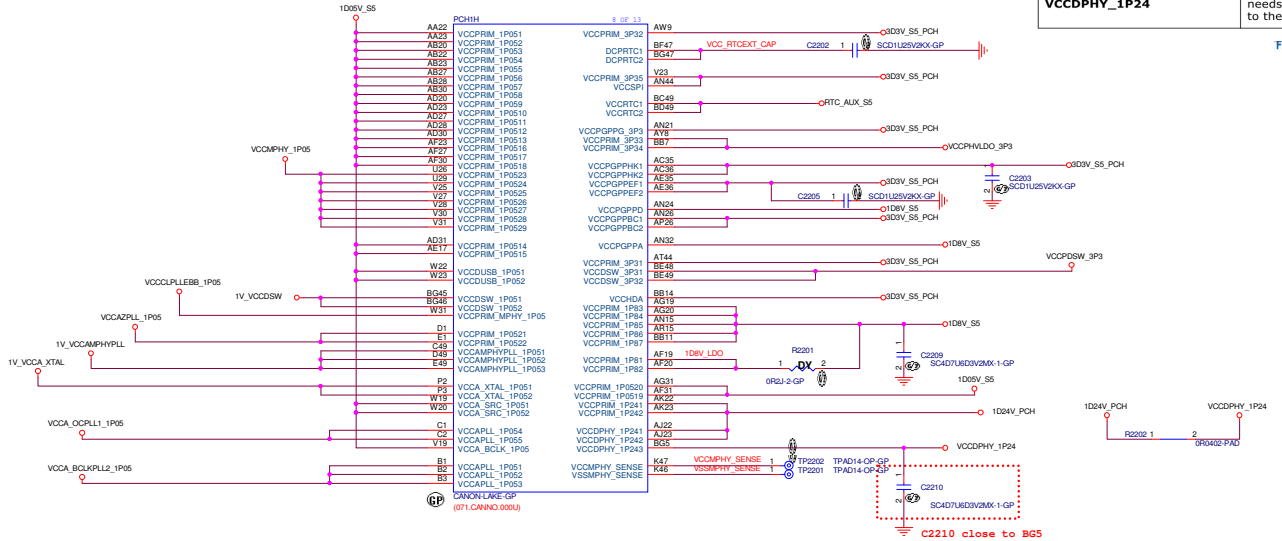
Figure 50-9. CFL PCH-H Power Rail VRM Recommendations

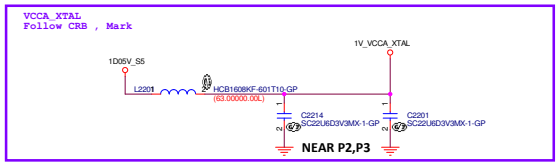


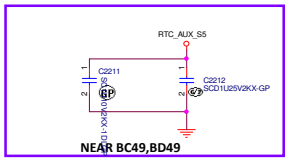
- Option 1: Internal VRM mode:
  - Short AF19, AF20, AG19, AG20 together.
  - Connect VCCPRIM_1P8 edge pin (BB11, AR15, AN15) to 4.7uF 0603 edge cap.
- Option 2: External VRM mode:
  - Keep AF19, AF20 as No connect (NC).
  - Connect VCCPRIM_1P8 edge pin (BB11, AR15, AN15) to 1uF 0402 edge cap.

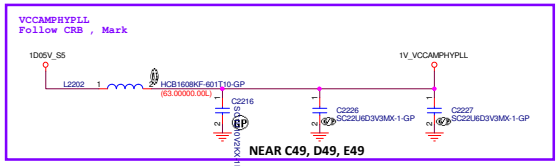
CFL PCH-H VCCDPHY_1P24 Routing

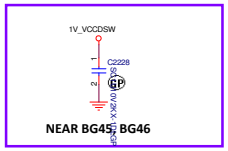


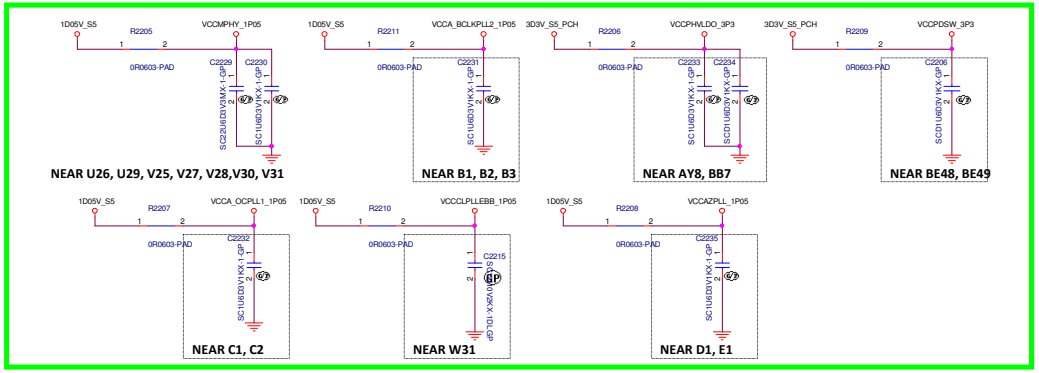






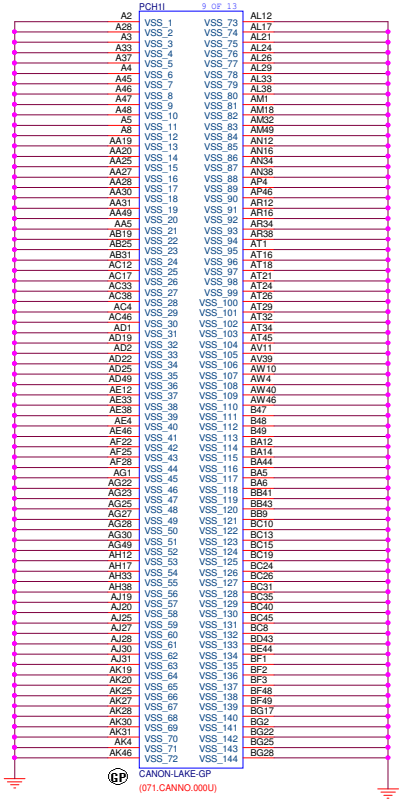


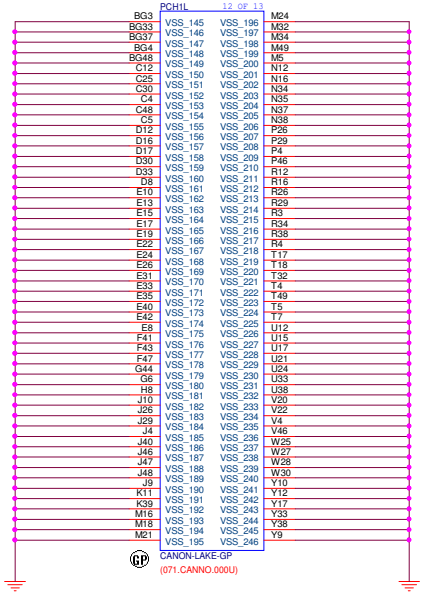


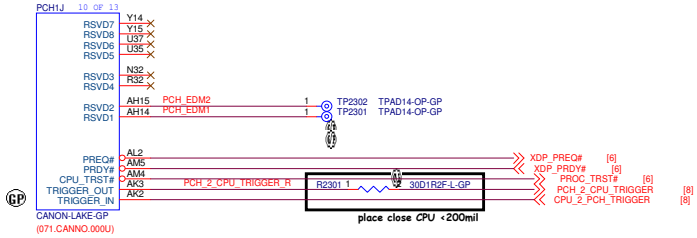


<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_POWER
Size: Custom | Document Number: Selek CFL-H | Rev: A00
Date: Thursday, April 11, 2019 | Sheet 22 of 105







<Core Design>

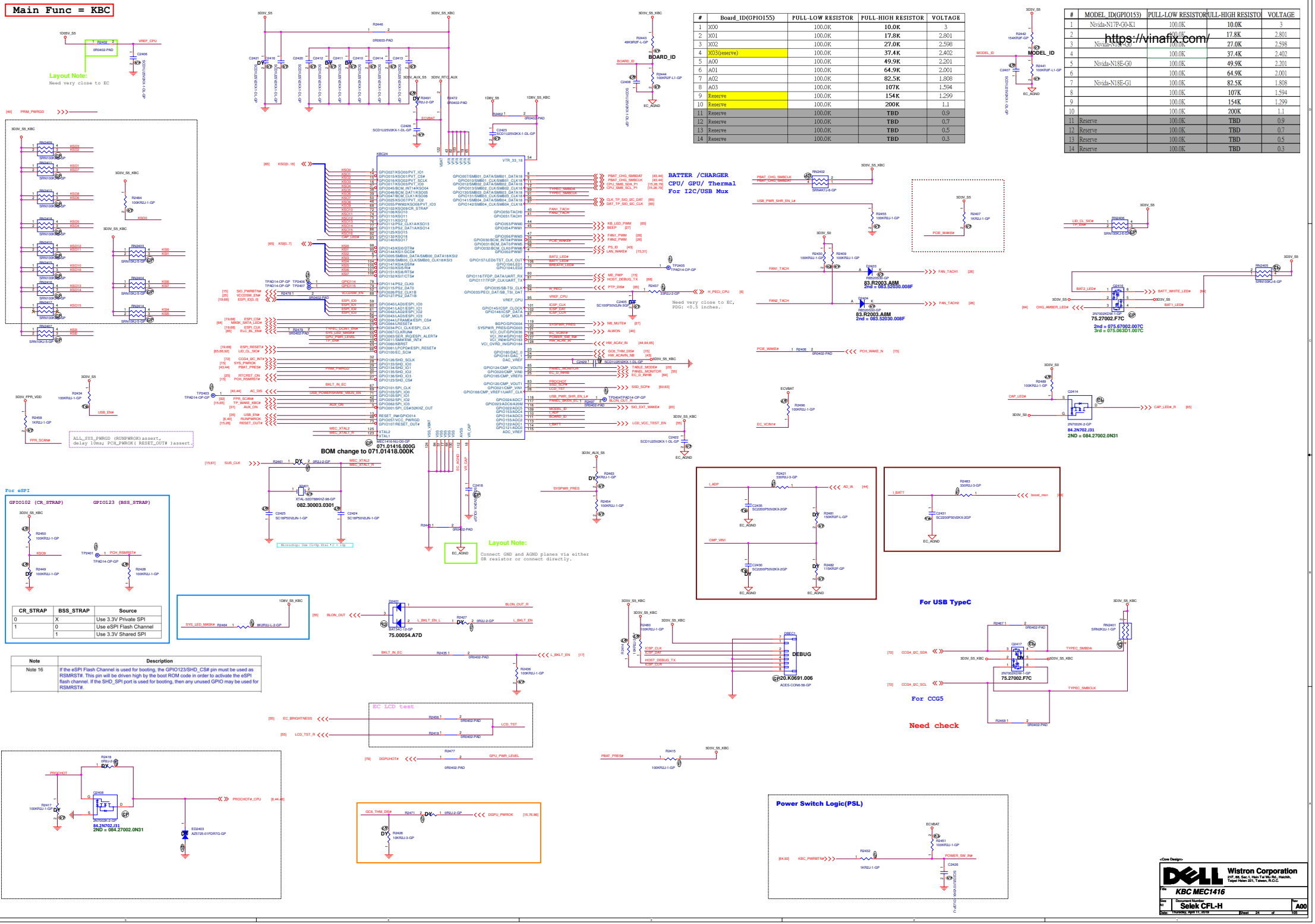
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_(VSS/GPIO)

Size	Document Number	Rev
Custom	Selek CFL-H	A00

Date: Thursday, April 11, 2019 Sheet 23 of 105

Main Func = KBC



#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	X00	100.0K	**10.0K**	3
2	X01	100.0K	**17.8K**	2.801
3	X02	100.0K	**27.0K**	2.598
4	X03(reserve)	100.0K	**37.4K**	2.402
5	A00	100.0K	**49.9K**	2.201
6	A01	100.0K	**64.9K**	2.001
7	A02	100.0K	**82.5K**	1.808
8	A03	100.0K	**107K**	1.594
9	Reserve	100.0K	**154K**	1.299
10	Reserve	100.0K	**200K**	1.1
11	Reserve	100.0K	**TBD**	0.9
12	Reserve	100.0K	**TBD**	0.7
13	Reserve	100.0K	**TBD**	0.5
14	Reserve	100.0K	**TBD**	0.3

#	MODEL_ID(GPIO153)	PULL-LOW RESISTOR	ULL-HIGH RESISTO	VOLTAGE
1	Nivida-N17P-G0-K1	100.0K	**10.0K**	3
2		100.0K	**17.8K**	2.801
3	Nivida-N18E-G0	100.0K	**27.0K**	2.598
4		100.0K	**37.4K**	2.402
5	Nivida-N18E-G0	100.0K	**49.9K**	2.201
6		100.0K	**64.9K**	2.001
7	Nivida-N18E-G1	100.0K	**82.5K**	1.808
8		100.0K	**107K**	1.594
9		100.0K	**154K**	1.299
10		100.0K	**200K**	1.1
11	Reserve	100.0K	**TBD**	0.9
12	Reserve	100.0K	**TBD**	0.7
13	Reserve	100.0K	**TBD**	0.5
14	Reserve	100.0K	**TBD**	0.3

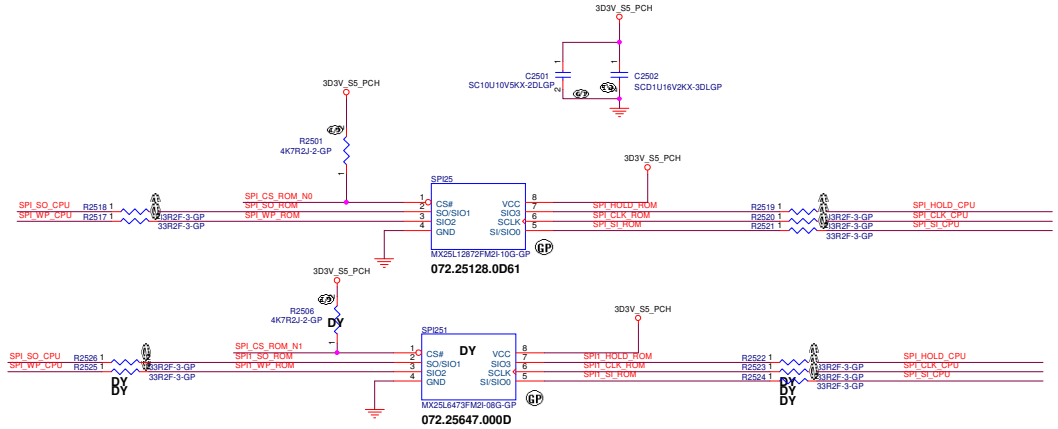
CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
	1	Use 3.3V Shared SPI

Note	Description
Note 16	If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
File: KBC MEC1416
Size: A1 | Document Number: Selek CFL-H | Rev: A00
Date: Thursday, April 11, 2019 | Sheet 24 of 105

SSID = Flash.ROM SPI FLASH ROM (32M byte) for PCH

[15] SPI_CS_ROM_N0
[15,21,91] SPI_SO_CPU
[15,21] SPI_WP_CPU
[15,21] SPI_HOLD_CPU
[15,91] SPI_CLK_CPU
[15,21,91] SPI_SI_CPU
[15] SPI_CS_ROM_N1



Main Func = RTC

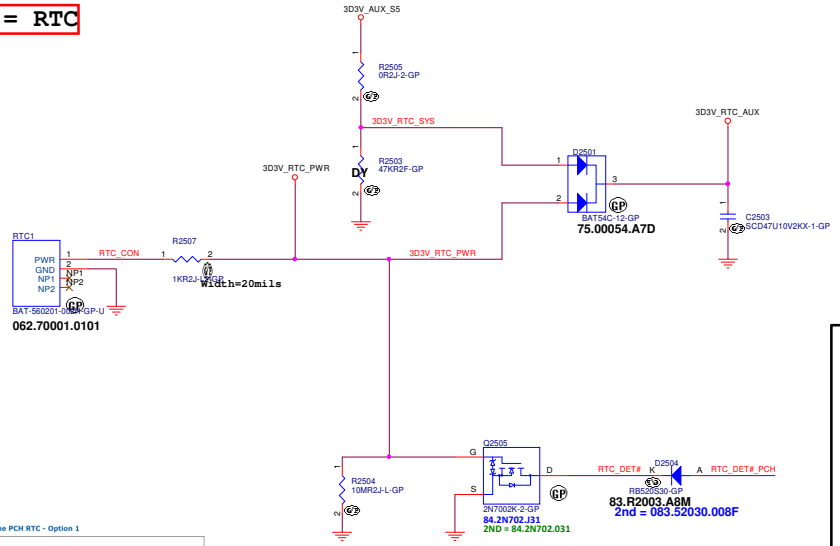
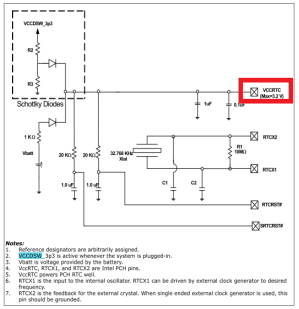
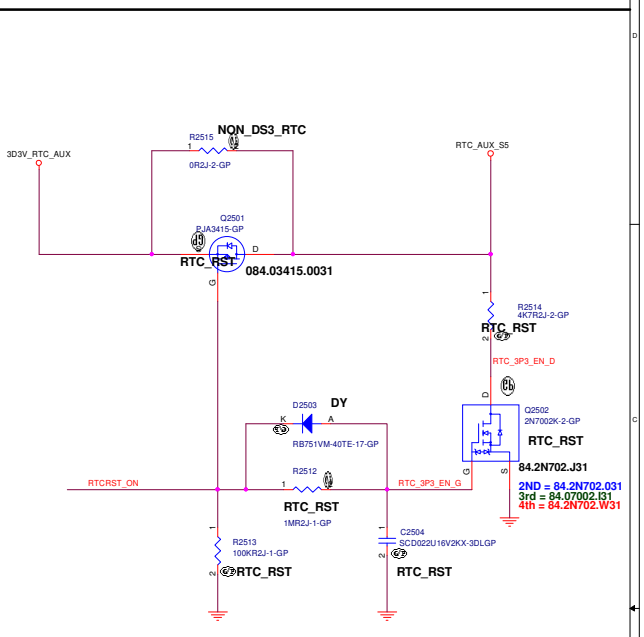
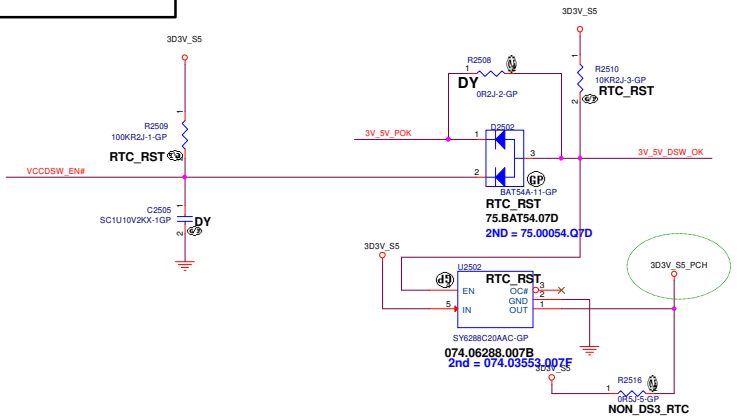


Figure 28-2. External Circuitry for the PCH RTC - Option 1





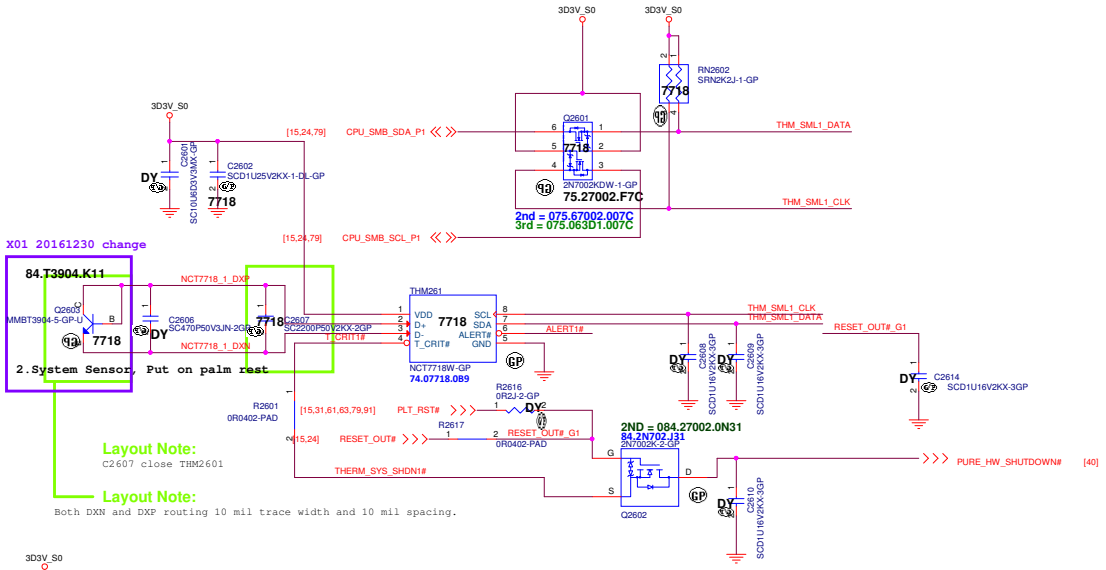


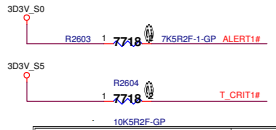
RTC GEN9

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	Flash(KBC+PCH)/RTC	
Size A2	Document Number Selek CFL-H	Rev A00
Date: Thursday, April 11, 2019	Sheet 25 of 105	

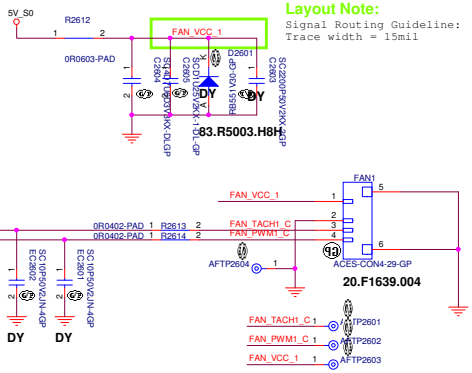
Main Func = Thermal Sensor



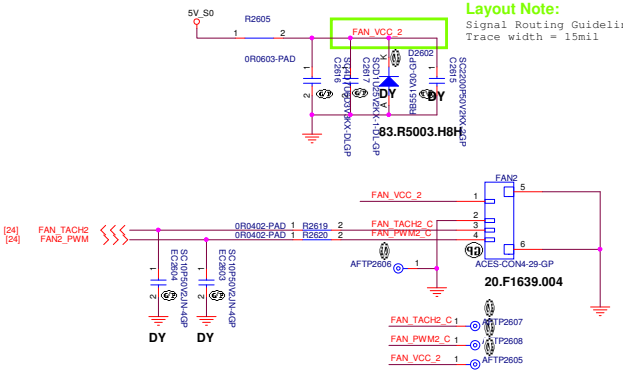


TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

PWM FAN1



PWM FAN2



https://vinafix.com/

<Core Design>

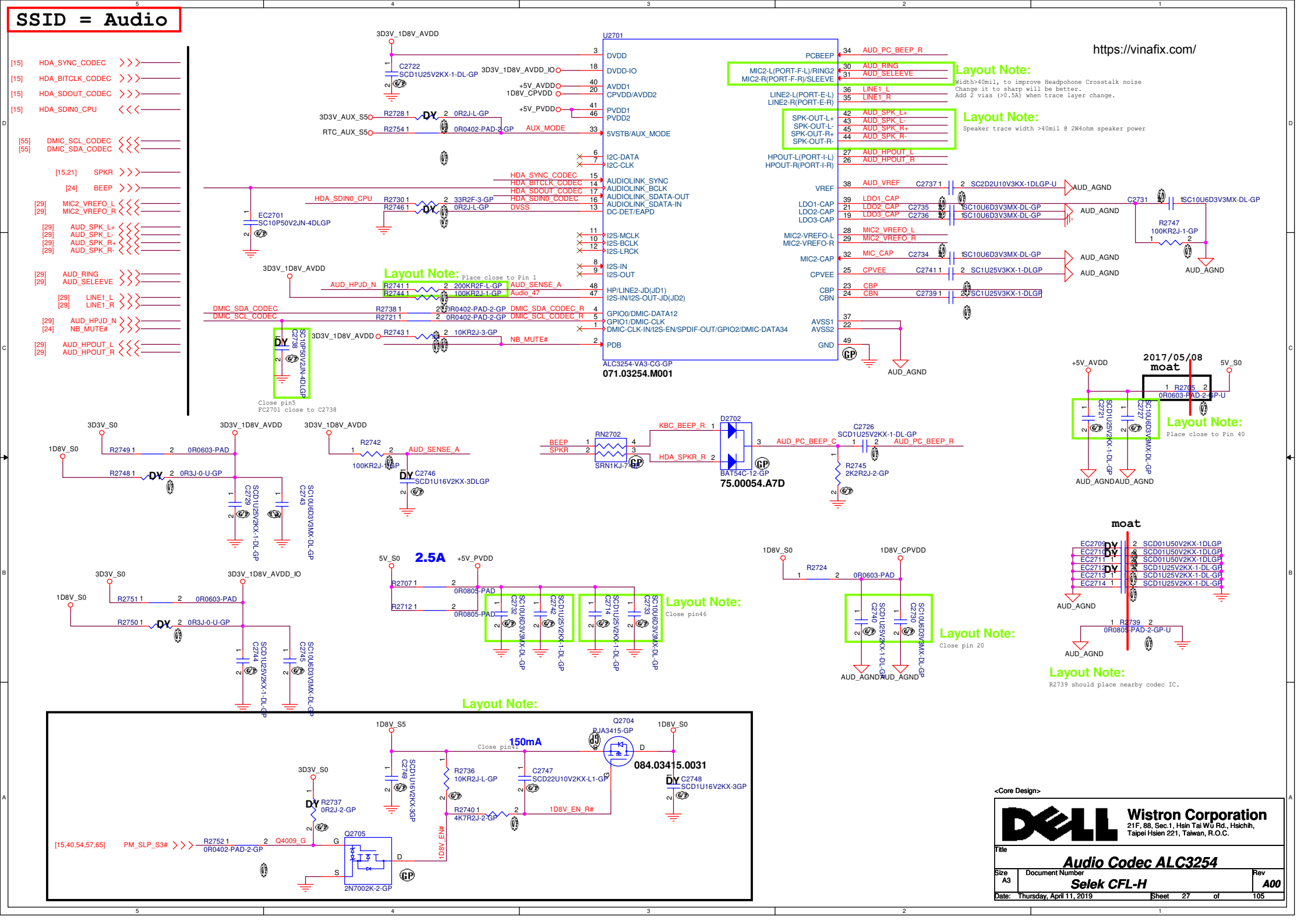
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan

Size: Custom | Document Number: Selek CFL-H | Rev: A00

Date: Thursday, April 11, 2019 | Sheet 26 of 105

SSID = Audio



<core_design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Codec ALC3254**

Size	Document Number	Rev
A3	Selek CFL-H	A00

Date: Thursday, April 11, 2019 Sheet 27 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
RESERVED

Size	Document Number	Rev
A4	Selek CFL-H	A00

Date: Thursday, April 11, 2019 Sheet 28 of 105

Main Func = Audio

https://vinafix.com/

[27] AUD_SPK_L+
[27] AUD_SPK_L-
[27] AUD_SPK_R+
[27] AUD_SPK_R-

[27] MIC2_VREFO_R
[27] MIC2_VREFO_L
[27] AUD_RING
[27] AUD_HPOUT_L
[27] LINE1_L
[27] AUD_HPOUT_R
[27] LINE1_R
[27] AUD_SELEEVE
[27] AUD_HPJD_N
[27] SKP_ID

Speaker

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

AUD_SPK_R+ — R2904 1 — 0R3J-0-U-GP — AUD_SPK_R+_C
AUD_SPK_R- — R2903 1 — 0R3J-0-U-GP — AUD_SPK_R-_C
AUD_SPK_L- — R2902 1 — 0R3J-0-U-GP — AUD_SPK_L-_C
AUD_SPK_L+ — R2901 1 — 0R3J-0-U-GP — AUD_SPK_L+_C
SKP_ID

SPK1
7 — 1 — 2 — 3 — 4 — 5 — 6 — 8
ACES-CON6-20-GP-U
20.F1639.006

CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

EC2901 SC1KP50V2KX-1DLGP
EC2902 SC1KP50V2KX-1DLGP
EC2903 SC1KP50V2KX-1DLGP
EC2904 SC1KP50V2KX-1DLGP

3D3V_S0
R2915 10KR2J-3-GP
SKP_ID

AUD_SPK_L-_C — AFTP2901
AUD_SPK_L+_C — AFTP2902
AUD_SPK_R-_C — AFTP2903
AUD_SPK_R+_C — AFTP2904

Universal Jack (Moved to I/O Board)

RN2901 SRN2K2J-1-GP
MIC2_VREFO_R
MIC2_VREFO_L

AUD_RING — R2908 1 — 2 0R0402-PAD — RING2_R — AUD_HP1_JACK_L1 — R2911 1 — 2 10R2F-L-GP — AUD_HP1_JACK_L1_R
AUD_HPOUT_L — R2906 1 — 2 0R0402-PAD
LINE1_L — C2907 1 — 2 LINE1-L_C — R2907 1 — 2 0R0402-PAD — SC10U6D3V3MX-DL-GP

AUD_HPOUT_R — R2909 1 — 2 0R0402-PAD — AUD_HP1_JACK_R1 — R2912 1 — 2 10R2F-L-GP — AUD_HP1_JACK_R1_R
LINE1_R — C2908 1 — 2 LINE1-L_R — R2913 1 — 2 0R0402-PAD — SC10U6D3V3MX-DL-GP

AUD_SELEEVE — R2910 1 — 2 0R0402-PAD — SLEEVE_R

JACK_PLUG_DET
10 mils
R2905 0R0402-PAD-2-GP
AUD_AGND

Layout Note:
EC2908 EC2907 should place nearby codec IC.

EC2908 SC680P50V2KX-2DLGP
EC2907 SC680P50V2KX-2DLGP
EC2906 SC680P50V2KX-2DLGP
EC2905 SC680P50V2KX-2DLGP

AUD_AGND
AUD_AGND

CLOSS TO HPMIC1
AUD_HP1_JACK_L1_R
RING2_R
JACK_PLUG
JACK_PLUG_DET
SLEEVE_R
AUD_HP1_JACK_R1_R

ED2901 AZ5125-02S-R7G-GP 75.05125.07D
ED2902 AZ5125-02S-R7G-GP 75.05125.07D
ED2903 AZ5125-02S-R7G-GP 75.05125.07D

JACK_PLUG — R2914 — 0R0603-PAD — AUD_HPJD_N
10 mils
10 mils
Delay circuit
(JACK_PLUG_DET: on IO Board)
DY C2909 SC10U6D3V3MX-DL-GP
AUD_AGND

HPMIC1
RING2_R
AUD_HP1_JACK_L1_R
JACK_PLUG
JACK_PLUG_DET
AUD_HP1_JACK_R1_R
SLEEVE_R
MS
AUDIO-JK440-GP
022.10002.0111
AUD_AGND

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio IO
Size: A3
Document Number: Selek CFL-H
Rev: A00
Date: Thursday, April 11, 2019
Sheet 29 of 105

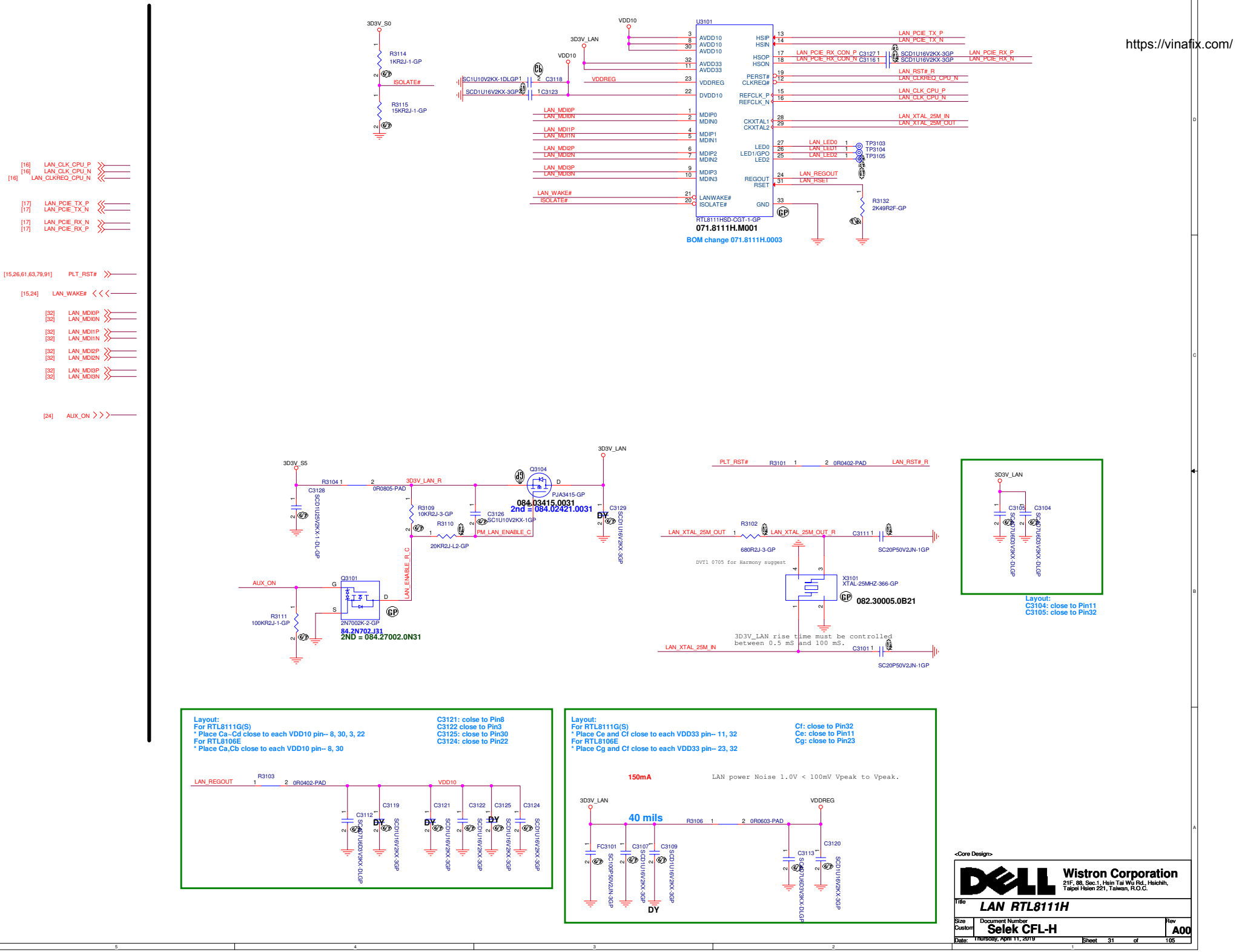
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Thursday, April 11, 2019 Sheet 30 of 105



[16] LAN_CLK_CPU_P
[16] LAN_CLK_CPU_N
[16] LAN_CLKREQ_CPU_N

[17] LAN_PCIE_TX_P
[17] LAN_PCIE_TX_N

[17] LAN_PCIE_RX_N
[17] LAN_PCIE_RX_P

[15,26,61,63,79,91] PLT_RST#

[15,24] LAN_WAKE#

[32] LAN_MDI0P
[32] LAN_MDI0N

[32] LAN_MDI1P
[32] LAN_MDI1N

[32] LAN_MDI2P
[32] LAN_MDI2N

[32] LAN_MDI3P
[32] LAN_MDI3N

[24] AUX_ON

<Core Design>

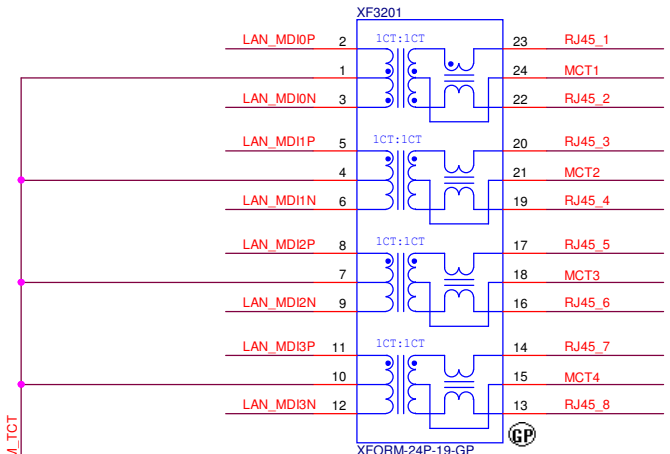
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

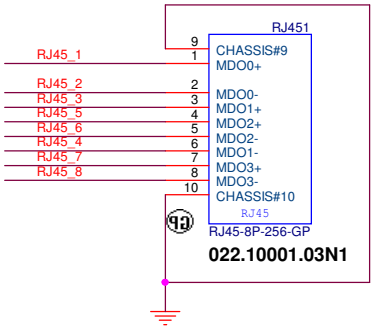
Title: LAN RTL8111H
Size: Custom
Document Number: Selek CFL-H
Rev: A00
Date: Thursday, April 11, 2019
Sheet 31 of 105

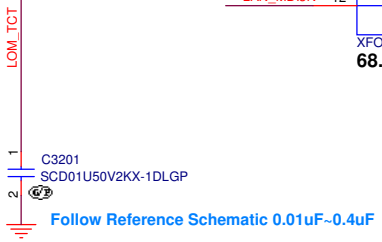
SSID = LAN

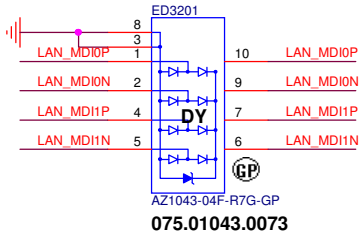
https://vinafix.com/

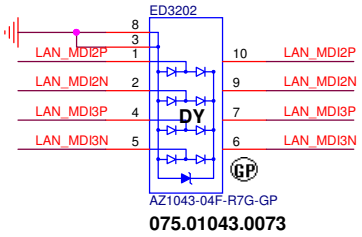
[31] LAN_MDI0P
[31] LAN_MDI0N
[31] LAN_MDI1P
[31] LAN_MDI1N
[31] LAN_MDI2P
[31] LAN_MDI2N
[31] LAN_MDI3P
[31] LAN_MDI3N

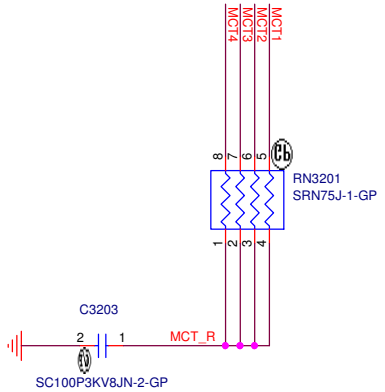












<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *RJ45+Transformer*		
Size: B	Document Number: Selek CFL-H	Rev: A00
Date: Thursday, April 11, 2019	Sheet 32 of 105	

SSID = Card Reader

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)

Size: A2 | Document Number: Selek CFL-H | Rev: A00

Date: Thursday, April 11, 2019 | Sheet 33 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Thursday, April 11, 2019 Sheet 34 of 105

USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

[19] USB1_USB30_RX_N
[19] USB1_USB30_RX_P
[19] USB1_USB30_TX_N
[19] USB1_USB30_TX_P
[18] USB1_USB20_P
[18] USB1_USB20_N

R3501 USB1_USB30_RX_N — USB1_USB30_RX_CON_N, 0R0402-PAD
R3502 USB1_USB30_RX_P — USB1_USB30_RX_CON_P, 0R0402-PAD
C3508 SCD1U25V2KX-1-DL-GP; R3503 USB1_USB30_TX_N — USB1_USB30_TX_CON_N, 0R0402-PAD
C3509 SCD1U25V2KX-1-DL-GP; R3504 USB1_USB30_TX_P — USB1_USB30_TX_CON_P, 0R0402-PAD

ED3501
USB1_USB30_RX_CON_N ↔ USB1_USB30_RX_CON_N
USB1_USB30_RX_CON_P ↔ USB1_USB30_RX_CON_P
USB1_USB30_TX_CON_N ↔ USB1_USB30_TX_CON_N
USB1_USB30_TX_CON_P ↔ USB1_USB30_TX_CON_P
L05ESDL5V0NA-4-GP
075.00550.0071

EL3501
USB1_USB20_P ↔ USB1_USB20_CON_P
USB1_USB20_N ↔ USB1_USB20_CON_N
FILTER-4P-213-GP
068.MCF86.2001

ED3502
I/O1, I/O4, GND, VDD, I/O2, I/O3
USB1_USB20_CON_N, USB1_USB20_CON_P, 5V_S5
AZC099-04S-2-GP
075.09904.0A7C
2nd = 75.08902.07C

USB30_VCCA
USB2
VBUS, D-, D+, SSRX-, SSRX+, SSTX-, SSTX+, PGND, GND, CHASSIS#10–#13
USB1_USB20_CON_N, USB1_USB20_CON_P
USB1_USB30_RX_CON_N, USB1_USB30_RX_CON_P
USB1_USB30_TX_CON_N, USB1_USB30_TX_CON_P
SKT-USB13-431-GP
022.10005.0FH1

USB30_VCCA
C3504 SC100U6D3V6MX-GP

[24,35] USB_EN#
[18] USB_OC0#

5V_S5, USB30_VCCA
EU3506 SY6288DAAC-GP (IN, EN# Active Low, OUT, GND, OC#)
074.06288.009B
2ND = 074.03553.007G
C3520 SC1U25V2KX-1DLGP
C3519 SCD1U16V2KX-L-GP
C3518 SC1U50V3KX-1-GP
USB_EN#, USB_OC0#

[24,35] USB_EN#
[18] USB_OC1#

5V_S5, USB30_VCCB
EU3508 SY6288DAAC-GP (IN, EN# Active Low, OUT, GND, OC#)
074.06288.009B
2ND = 074.03553.007G
C3524 SC1U25V2KX-1DLGP
C3523 SCD1U16V2KX-1-GP
C3522 SC1U50V3KX-1-GP
USB_EN#, USB_OC1#

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB3.0*2 CONN	
Size: Custom	Document Number: Selek CFL-H	Rev: A00
Date: Thursday, April 11, 2019	Sheet 35 of 105	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Charger*

Size	Document Number	Rev
B	Selek CFL-H	A00

Date: Thursday, April 11, 2019 Sheet 36 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Thursday, April 11, 2019 Sheet 37 of 105

SSID = USB3.0 Redriver

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB 3.0 Redriver*

Size	Document Number	Rev
A3	Selek CFL-H	A00

Date: Thursday, April 11, 2019 Sheet 38 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Thursday, April 11, 2019 Sheet 39 of 105

Power Sequence

[15,27,54,57,65] PM_SLP_S3#

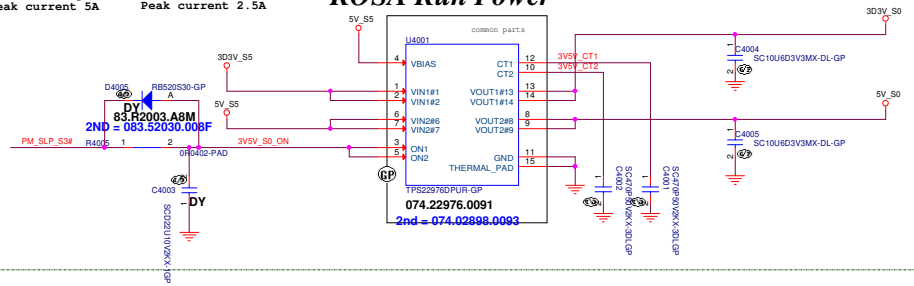
5V_S0

5V_S0 Comsumption
Peak current 5A

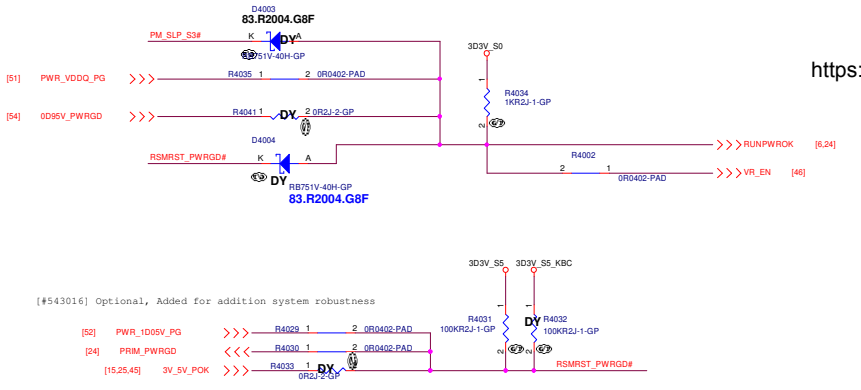
3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A

ROSA Run Power

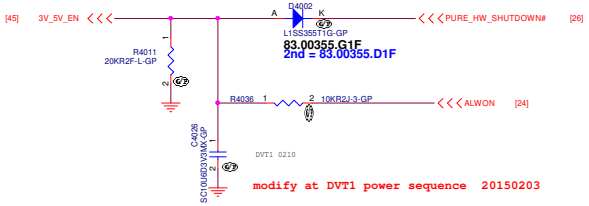


Power Good

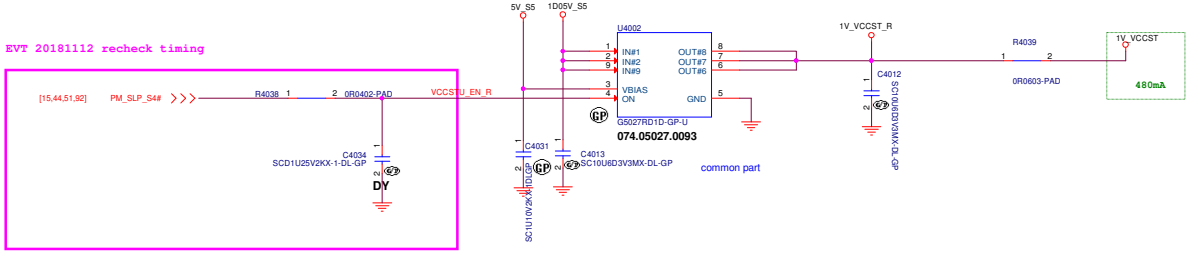


https://vinafix.com/

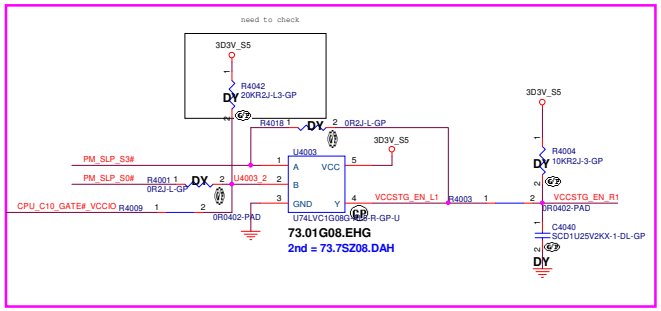
1V_VCCST



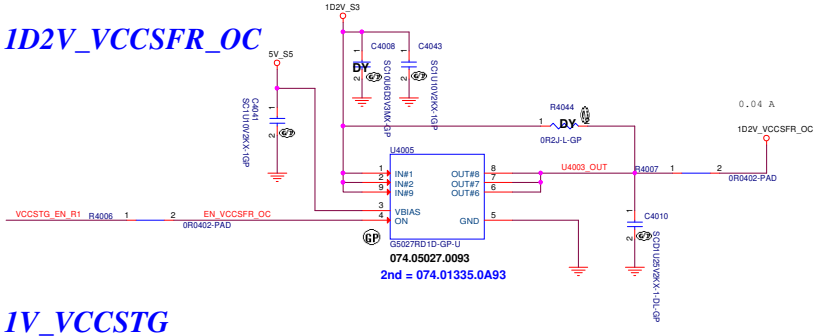
EVT 20181112 recheck timing



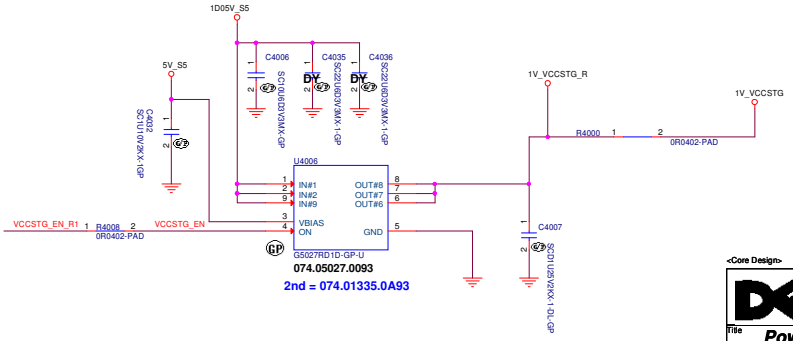
Sequence reserve

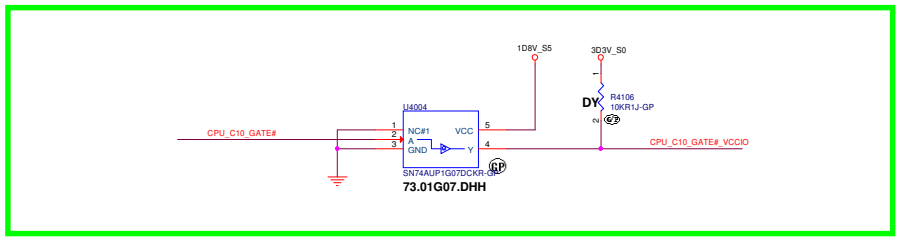


1D2V_VCCSFR_OC



1V_VCCSTG





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable & SEQUENCE

Size: A2 | Document Number: Selek CFL-H | Rev: A00

Date: Thursday, April 11, 2019 | Sheet 40 of 105

Main Func = Power & Sequence

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Connected_Standby(1/2)+DS3*

Size: A3 | Document Number: Selek CFL-H | Rev: A00

Date: Thursday, April 11, 2019 | Sheet 41 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Thursday, April 11, 2019 Sheet 42 of 105

Main Func = ADT Input

Layout Note:
PSID Layout width > 25mil

Pin Definition: TBD

60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA

EMI 20180515

X01 20161230B change

3rd = 75.00099.Q7D
4th = 75.00099.D7D

NON_TypeC

2ND = 83.R5003.T8F

Main Func = M-BAT Input

Batt Connecter

Placement: Close to Batt Connector

3rd = 75.00099.Q7D
4th = 75.00099.D7D

Barrel Adapter Piug-in Detect

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
DCIN		
Size: A2	Document Number: Selek CFL-H	Rev: A00
Date: Thursday, April 11, 2019	Sheet 43 of 105	

Main Func = Charger

ISL95522 Hybrid Charger

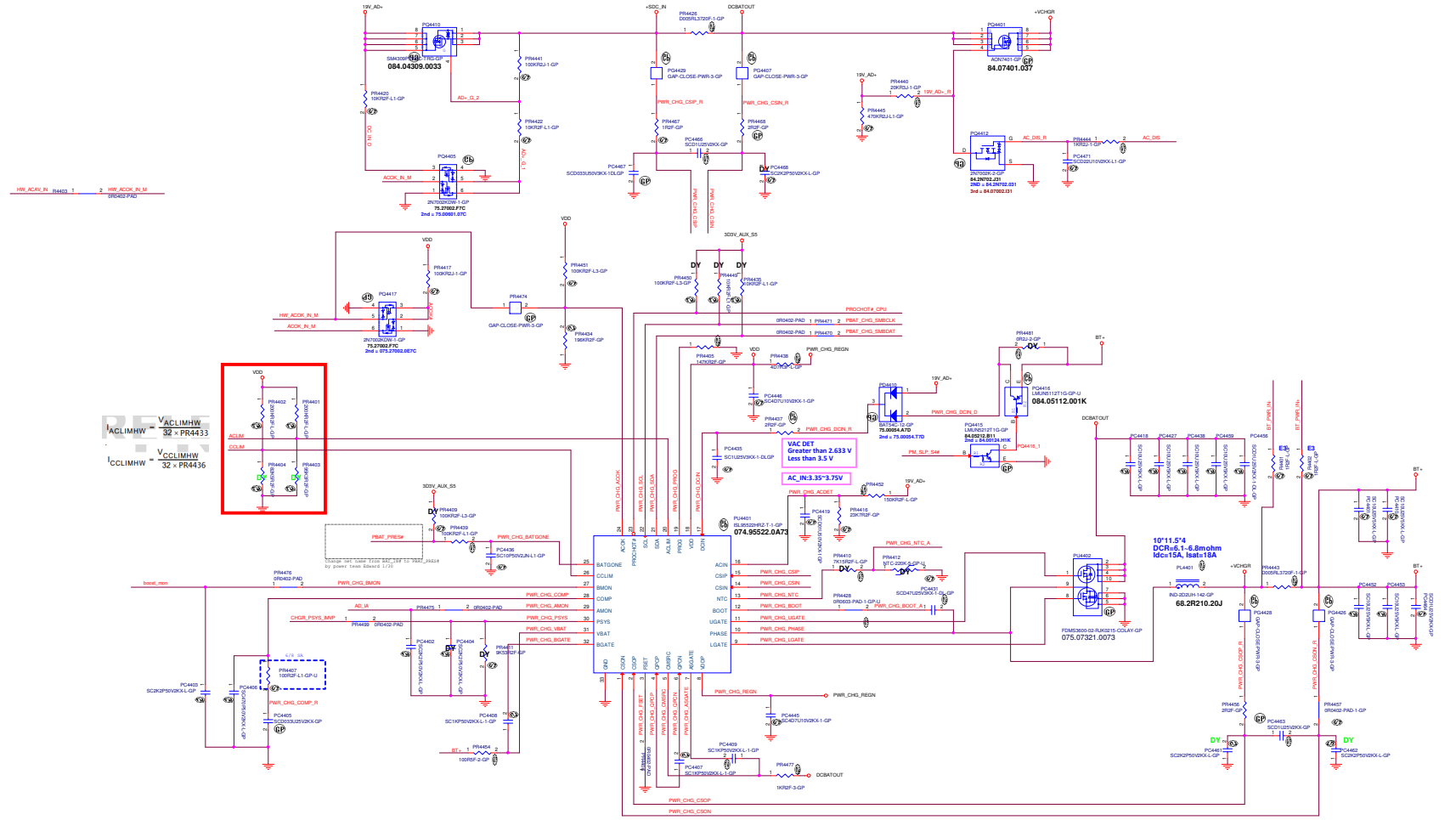
https://vinafix.com/

OFF PAGE

[24,64,65] HW_ACAV_IN
[24,43] AC_DIS
[15,40,51,92] PM_SLP_S4#
[15,43] ACOK_IN_M
[24,43] PBAT_CHG_SMBDAT
[24,43] PBAT_CHG_SMBCLK
[24,43] PBAT_PRES#
[6,24,46] PROCHOT#_CPU
[24] AD_IA
[46] CHGR_PSYS_IMVP
[24] boost_mon

E3

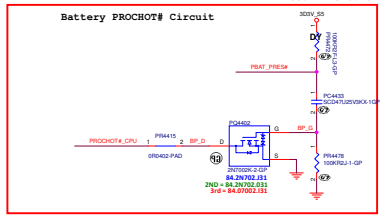
[66] BT_PWR_IN+
[66] BT_PWR_IN-



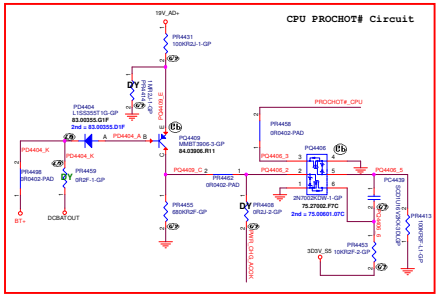
$$I_{ACLIMHW} = \frac{V_{ACLIMHW}}{32 \times PR4433}$$

$$I_{CCLIMHW} = \frac{V_{CCLIMHW}}{32 \times PR4436}$$

Need fine tune



PR4405	2 cell	3 cell	4 cell
NVDC	100k	66.5k	82.5k
HYBRID	165k	182k	147k

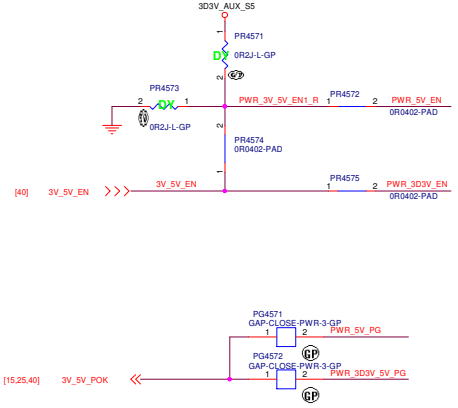


«Core Design»
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

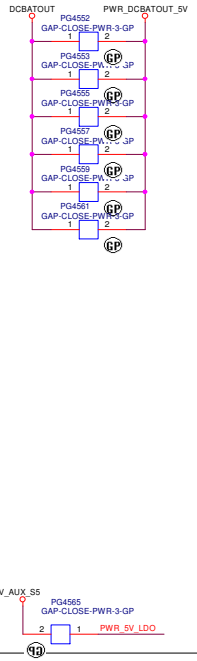
Title: Charger
Size: A1 | Document Number: Seiek CFL-H | Rev: A00
Date: Thursday, April 11, 2019 | Sheet 44 of 105

SSID = PWR.Plane.Regulator_5V

OFFPAGE-Signal

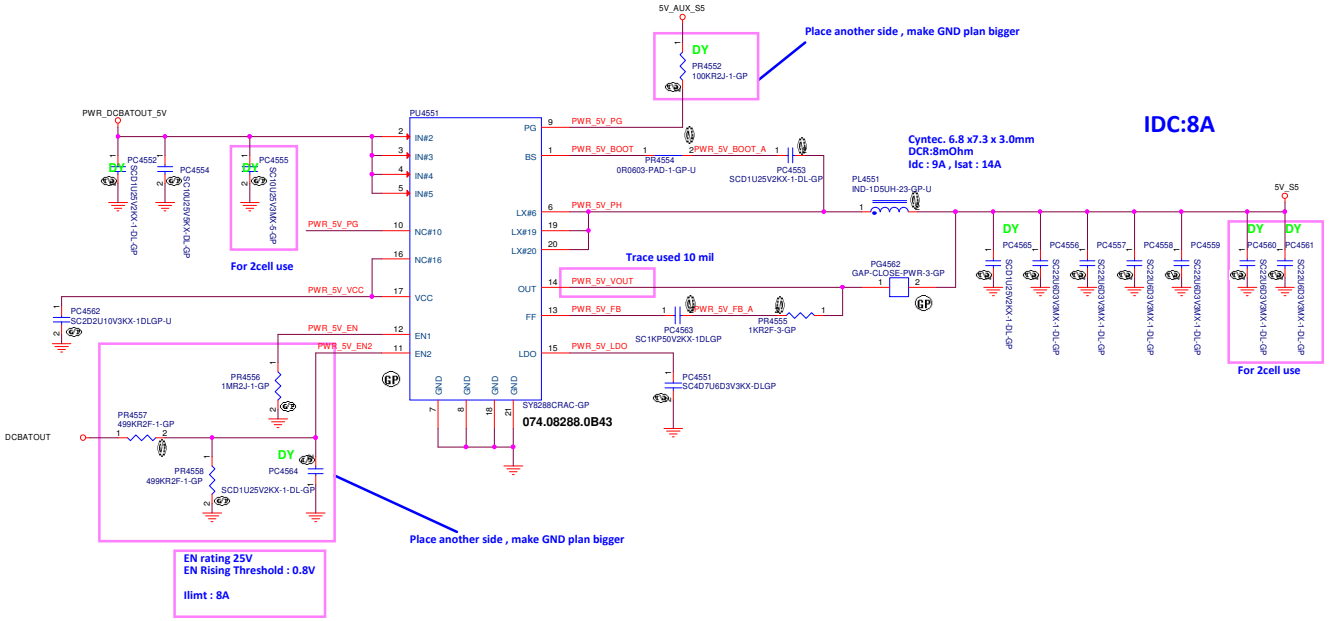


OFFPAGE-GAP



SY8288C For 5V

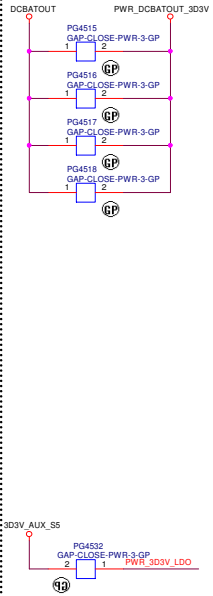
https://vinafix.com/



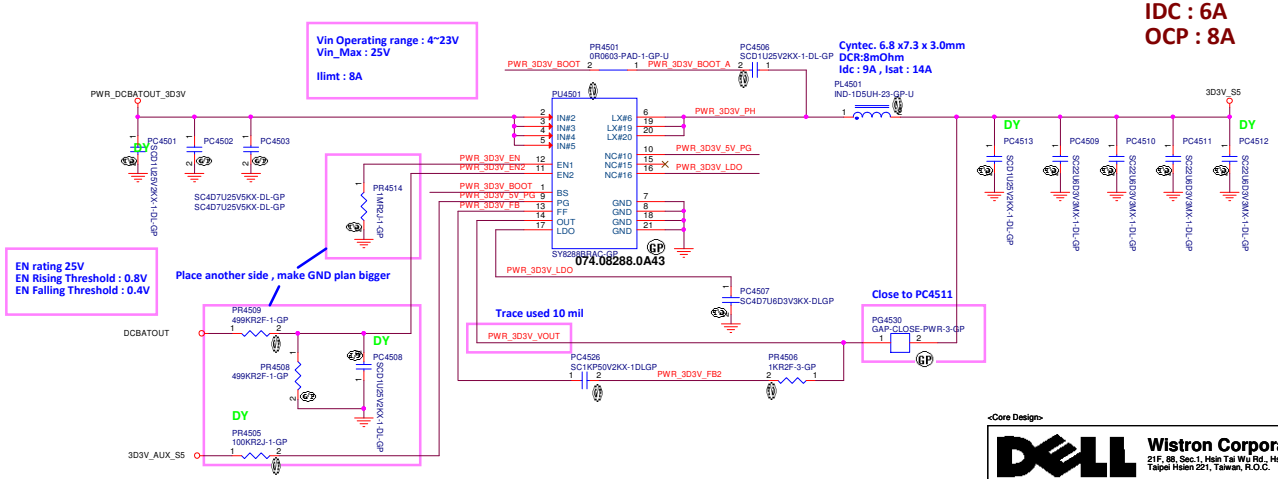
SSID = PWR.Plane.Regulator_3D3V

OFFPAGE-Signal

OFFPAGE-GAP



SY8286B For 3D3V



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (SY8288_5V/3D3V)

Size: A2 | Document Number: Selek CFL-H | Rev: A00

Date: Thursday, April 11, 2019 | Sheet 45 of 105

OFFPAGE

VCCSA SENSE

VCCCORE SENSE

VCCGT_I SENSE

Close to VCCSA Choke

Close to Vcore Choke

Close to GFX_I Choke

074.81215.0073

VBOOT Setting For Core/GT
24.9K ohm -> 0V
169K ohm -> 1.05V

VCCCORE Feedback

VCCGT Feedback

Close to VCORE Dr.MOS

Close to GFX_I Dr.MOS

Add : PWR GAP
change GND symbol on this page ALL GND

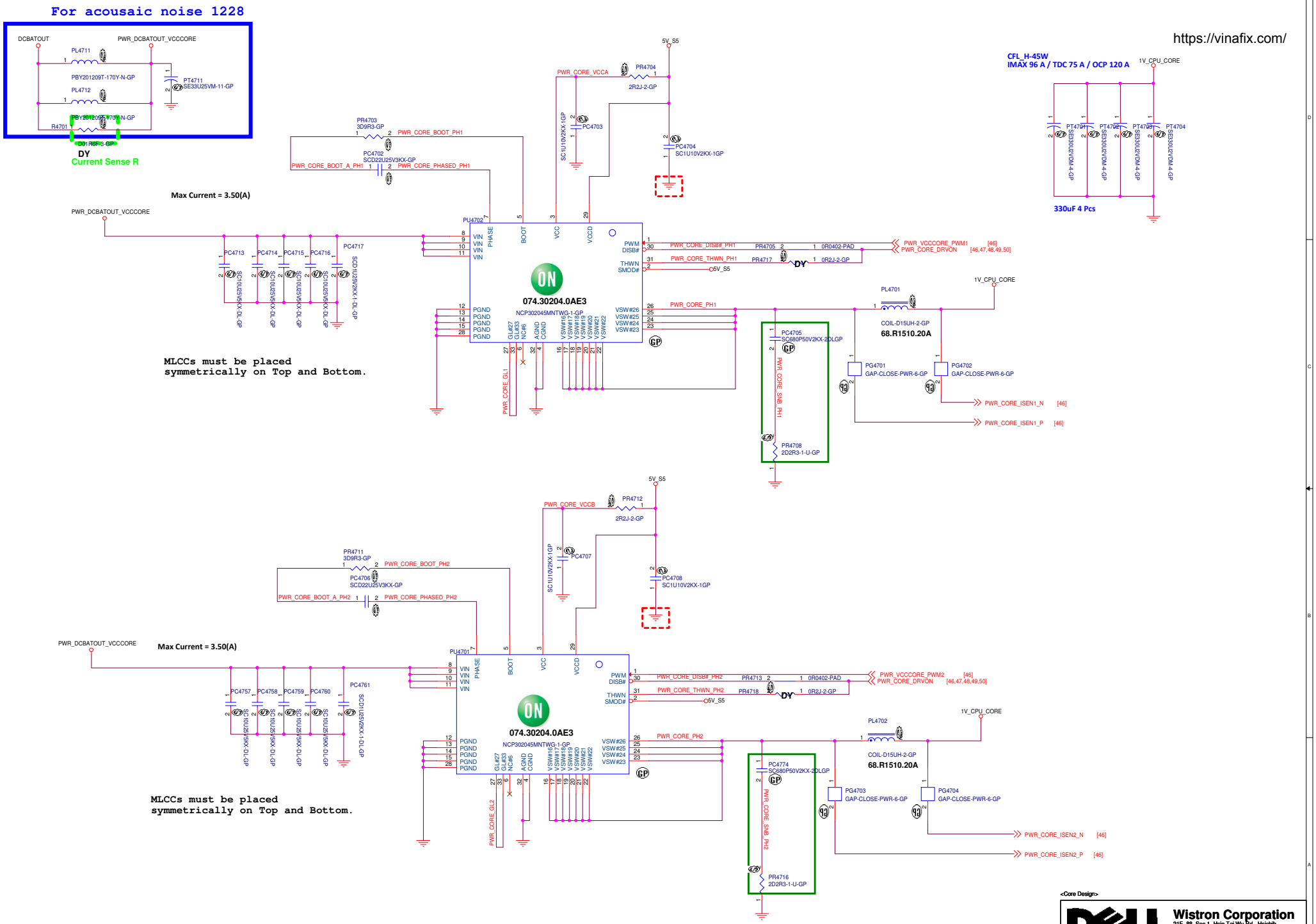
<Core Design>

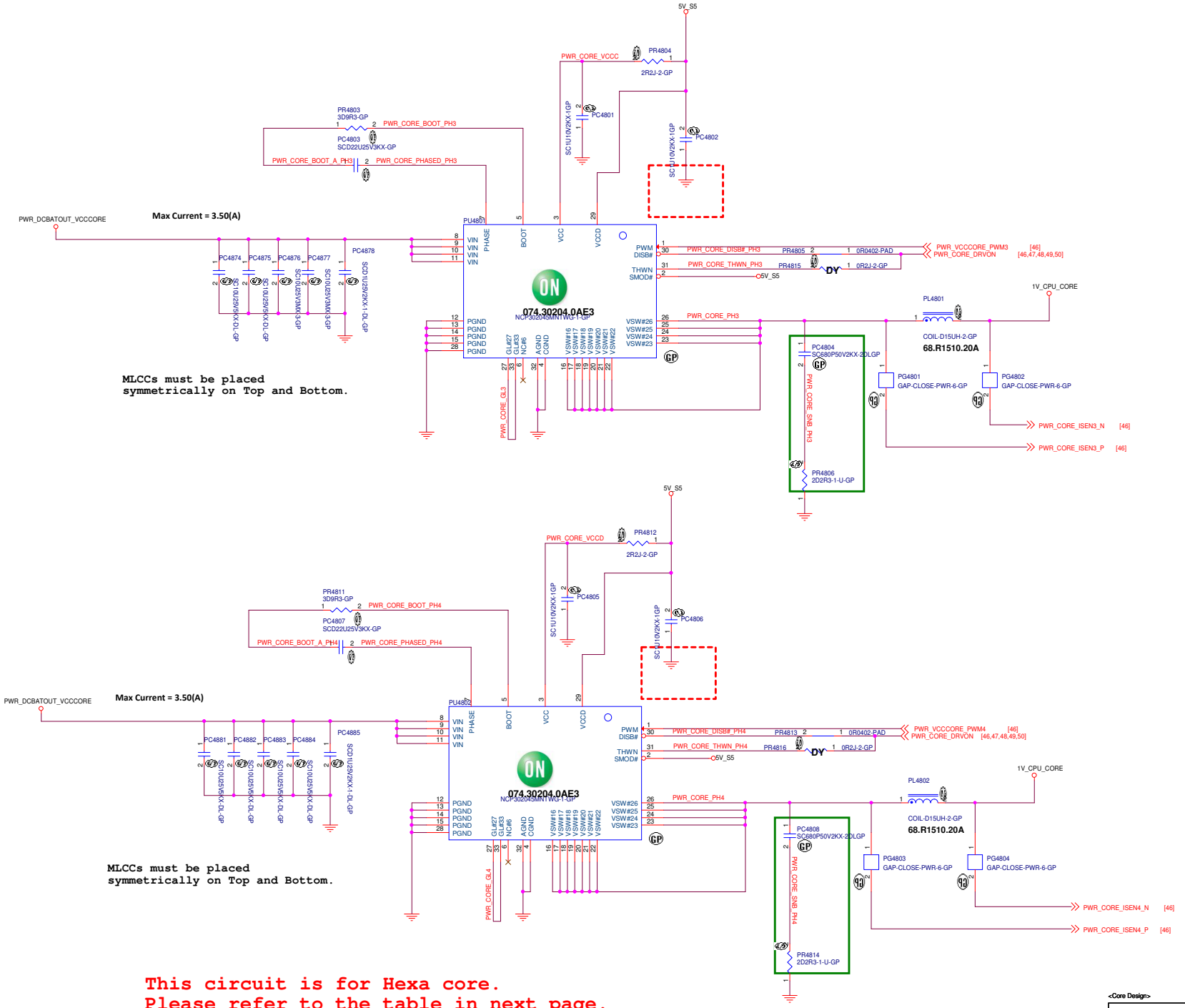
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC IMVP8

Size: Custom | Document Number: Selek CFL-H | Rev: A00

Date: Thursday, April 11, 2019 | Sheet 46 of 105


For acousaic noise 1228
DCBATOUT
PWR_DCBATOUT_VCCCORE
PL4711
PBY201209T-170Y-N-GP
PL4712
PBY201209T-170Y-N-GP
R4701
3D1R5-GP
PT4711
SE33U25VM-11-GP
DY
Current Sense R
https://vinafix.com/
CFL_H-45W
IMAX 96 A / TDC 75 A / OCP 120 A
1V_CPU_CORE
PT4704
SE330U2VDM-4-GP
330uF 4 Pcs
5V_S5
PWR_CORE_VCCA
PR4704
2R2J-2-GP
PC4703
SC1U10V2KX-1GP
PC4704
SC1U10V2KX-1GP
PR4703
3D9R3-GP
PWR_CORE_BOOT_PH1
PC4702
SCD22U25V3KX-GP
PWR_CORE_BOOT_A_PH1
PWR_CORE_PHASED_PH1
Max Current = 3.50(A)
PWR_DCBATOUT_VCCCORE
PU4702
PC4713
PC4714
PC4715
PC4716
PC4717
SCD10U25V5KX-1DL-GP
VIN
PHASE
BOOT
VCC
VCCD
PWM
DISB#
THWN
SMOD#
PWR_CORE_DISB#_PH1
PR4705
0R0402-PAD
PWR_VCCCORE_PWM1
PWR_CORE_DRVON
PWR_CORE_THWN_PH1
PR4717
0R2J-2-GP
5V_S5
ON
074.30204.0AE3
NCP302045MNTWG-1-GP
PGND
GL#27
GL#33
NC#6
AGND
CGND
VSW#16
VSW#17
VSW#18
VSW#19
VSW#20
VSW#21
VSW#22
VSW#26
VSW#25
VSW#24
VSW#23
PWR_CORE_PH1
PWR_CORE_GL1
PC4705
SC680P50V2KX-2DLGP
PWR_CORE_SNB_PH1
PR4708
2D2R3-1-U-GP
PL4701
COIL-D15UH-2-GP
68.R1510.20A
PG4701
GAP-CLOSE-PWR-6-GP
PG4702
GAP-CLOSE-PWR-6-GP
PWR_CORE_ISEN1_N
PWR_CORE_ISEN1_P
MLCCs must be placed
symmetrically on Top and Bottom.
PWR_CORE_VCCB
PR4712
2R2J-2-GP
PC4707
SC1U10V2KX-1GP
PC4708
SC1U10V2KX-1GP
PR4711
3D9R3-GP
PWR_CORE_BOOT_PH2
PC4706
SCD22U25V3KX-GP
PWR_CORE_BOOT_A_PH2
PWR_CORE_PHASED_PH2
PWR_DCBATOUT_VCCCORE
Max Current = 3.50(A)
PU4701
PC4757
PC4758
PC4759
PC4760
PC4761
SCD10U25V5KX-1DL-GP
PWR_CORE_DISB#_PH2
PR4713
0R0402-PAD
PWR_VCCCORE_PWM2
PWR_CORE_DRVON
PWR_CORE_THWN_PH2
PR4718
0R2J-2-GP
5V_S5
ON
074.30204.0AE3
NCP302045MNTWG-1-GP
PWR_CORE_PH2
PWR_CORE_GL2
PC4774
SC680P50V2KX-2DLGP
PWR_CORE_SNB_PH2
PR4716
2D2R3-1-U-GP
PL4702
COIL-D15UH-2-GP
68.R1510.20A
PG4703
GAP-CLOSE-PWR-6-GP
PG4704
GAP-CLOSE-PWR-6-GP
PWR_CORE_ISEN2_N
PWR_CORE_ISEN2_P
MLCCs must be placed
symmetrically on Top and Bottom.
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DC/DC VCCCPUCORE (1/2)
Size
C
Document Number
Selek CFL-H
Rev
A00
Date:
Thursday, April 11, 2019
Sheet
47
of
105



This circuit is for Hexa core.
Please refer to the table in next page.

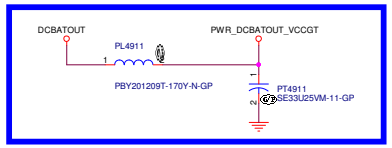
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

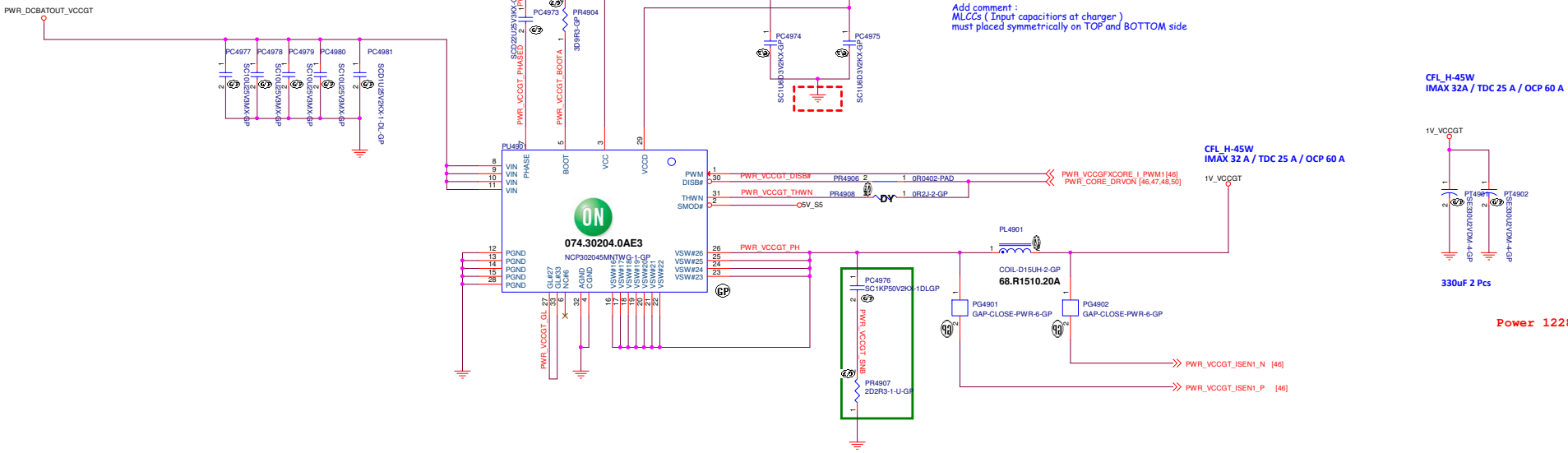
Title: DC/DC VCCCPUCORE (2/2)

Size	Document Number	Rev
C	Selek CFL-H	A00

Date: Thursday, April 11, 2019 Sheet 48 of 105



For acousaic noise 1228



CFL_H-45W
IMAX 32 A / TDC 25 A / OCP 60 A

CFL_H-45W
IMAX 32A / TDC 25 A / OCP 60 A

330uF 2 Pcs

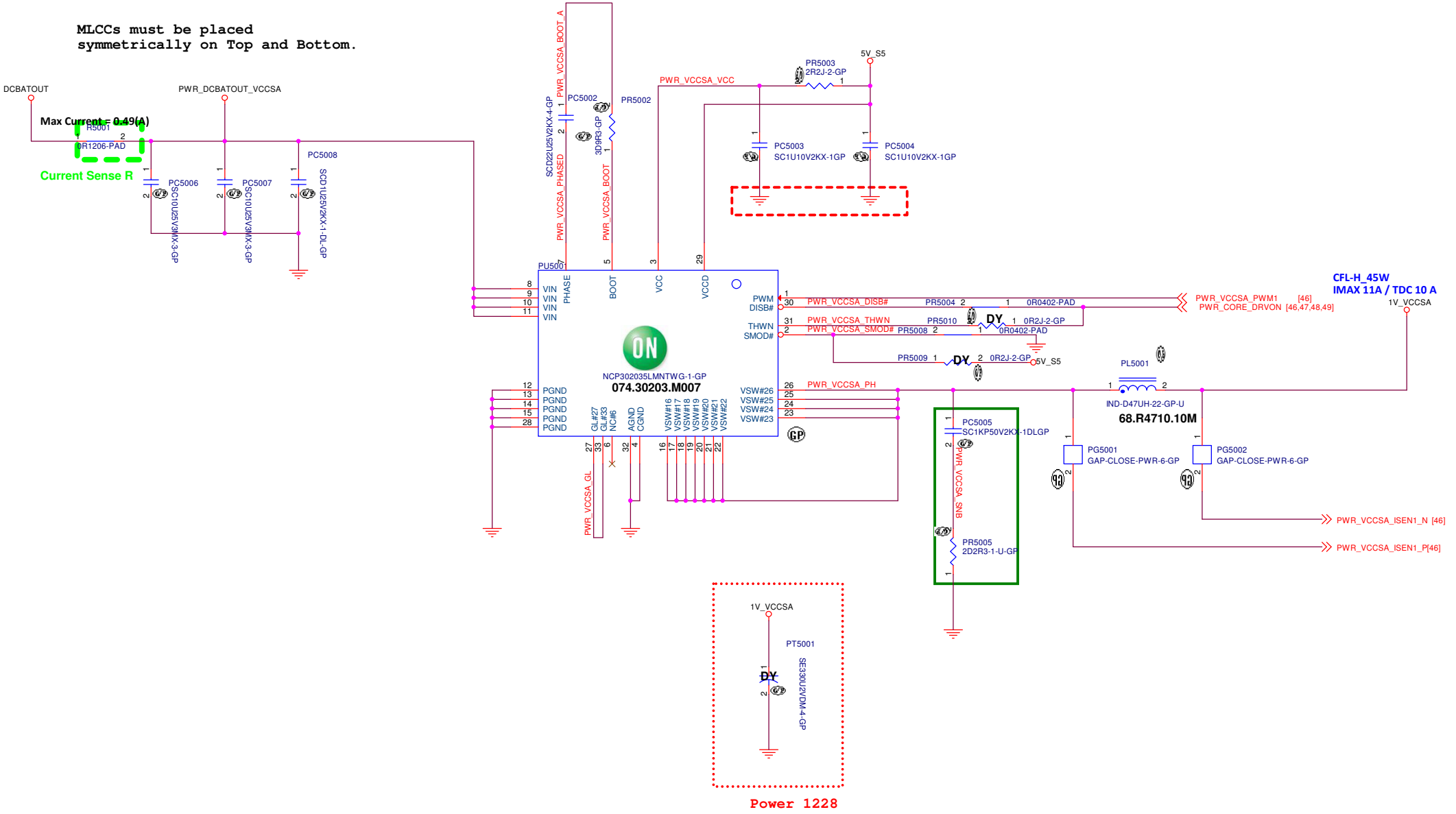
Power 1228

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DC/DC VCCGFXCORE_I(NCP302045)	
Size: Custom	Document Number: Selek CFL-H	Rev: A00
Date: Thursday, April 11, 2019	Sheet 49 of 105	

MLCCs must be placed
symmetrically on Top and Bottom.



<Core Design>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DC/DC VCCSA(NCP302035)		
Size: A3	Document Number: Selek CFL-H	Rev: A00
Date: Thursday, April 11, 2019	Sheet 50 of 105	

SSID = PWR.Plane.Regulator_1D2V/0D6V

OFFPAGE-Signal

S5

S3

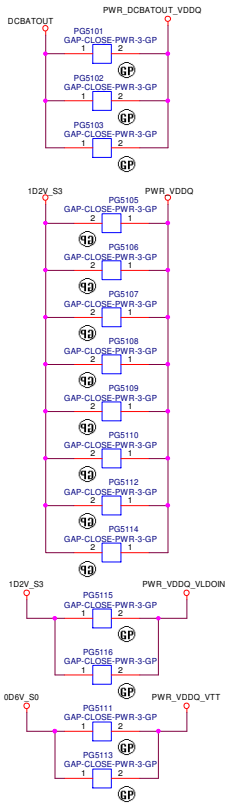
[8] DDR_PG_OUT >> DDR_PG_OUT

PH on EE Side

[40] PWR_VDDQ_PG <<< PWR_VDDQ_PG

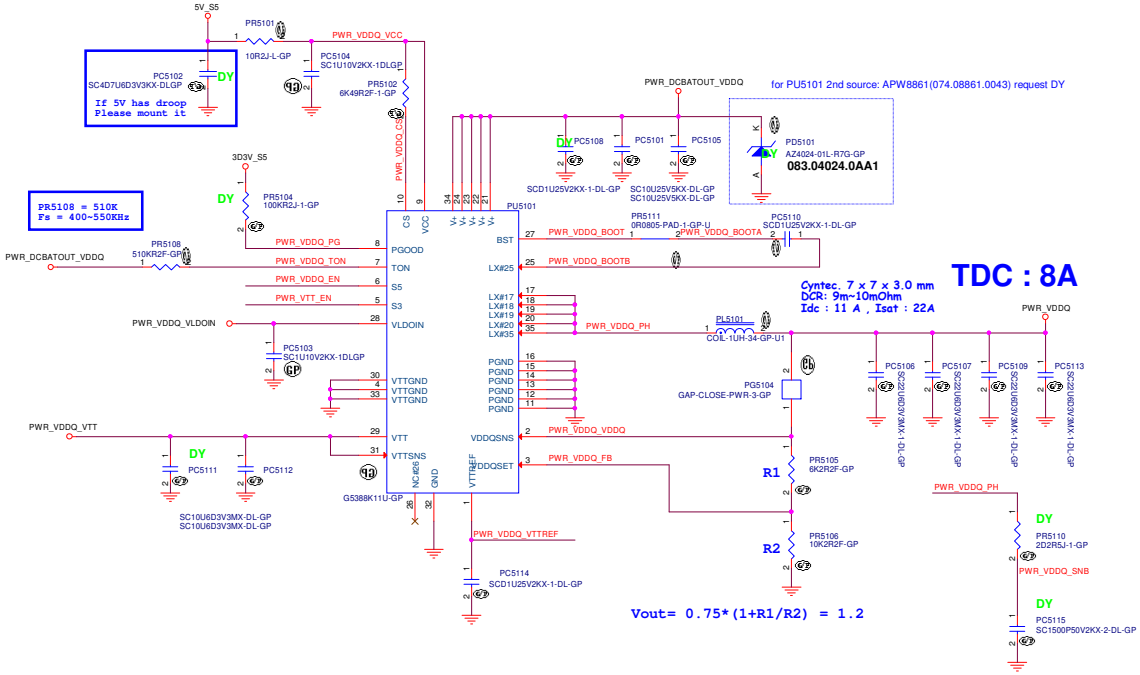
DDR_PG_OUT — R5102 0R0402-PAD — PWR_VTT_EN

OFFPAGE-GAP



G5388 For VDDQ/VTT

https://vinafix.com/



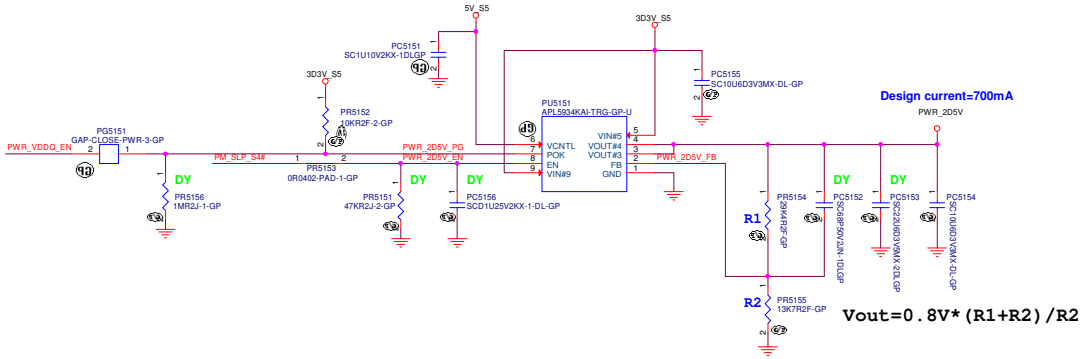
SSID = PWR.Plane.Regulator_2D5V

OFFPAGE-Signal

[15,40,44,92] PM_SLP_S4# >>>

OFFPAGE-GAP

APL5934 For 2D5V



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power (G5388_VDDQ_VTT_VPP)

Size	Document Number	Rev
A2	Selek CFL-H	A00

Date: Thursday, April 11, 2019 Sheet 51 of 105

SSID = PWR.Plane.Regulator_1D05V

OFFPAGE-Signal

PH on EE Side

[40] PWR_1D05V_PG

PWR_1D05V_PG

[53] PWR_1D8V_PG

OFFPAGE-GAP

DCBATOUT

PWR_DCBATOUT_1D05V

PG5201 GAP-CLOSE-PWR-3-GP

PG5202 GAP-CLOSE-PWR-3-GP

PG5203 GAP-CLOSE-PWR-3-GP

1D05V_S5

PWR_1D05V

PG5204 GAP-CLOSE-PWR-3-GP

PG5205 GAP-CLOSE-PWR-3-GP

PG5206 GAP-CLOSE-PWR-3-GP

PG5207 GAP-CLOSE-PWR-3-GP

PG5208 GAP-CLOSE-PWR-3-GP

PG5209 GAP-CLOSE-PWR-3-GP

PG5211 GAP-CLOSE-PWR-3-GP

PG5212 GAP-CLOSE-PWR-3-GP

PG5213 GAP-CLOSE-PWR-3-GP

PG5214 GAP-CLOSE-PWR-3-GP

IC / COM	AOZ2262(10A) 074.02262.0043	AOZ2261(8A) 074.02261.0A73	AOZ2260(6A) 074.02260.0043
Chock	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A
Output CAP	22uF/6.3V * 5pcs DY*1	22uF/6.3V * 4pcs DY*1	22uF/6.3V * 4pcs DY*1

AOZ2262 For 1D05V

Cyntec. 6.5mm x 6.9mm x 3.0mm
DCR: 9m~10mOhm
Idc : 11 A , Isat : 22A

TDC : 10A

5V_S5

PC5202 SC4D7U25V5KX-DL-GP

PU5201

VCC

IN#7 IN#8 IN#9

TON

PGOOD

EN

PFM#

SS

BST

FB

AGND

PGND

LX#18 LX#17 LX#16 LX#11 LX#10

AOZ2262QI-10-GP-U

PWR_DCBATOUT_1D05V

PC5208 DY SCD1U25V2KX-1-DL-GP

PC5209 SC10U25V5KX-DL-GP

PC5210 SC10U25V5KX-DL-GP

PR5201 88K7R2F-GP

PWR_1D05V_TON

PWR_1D05V_PG

PWR_1D05V_EN

PWR_1D05V_PFM

PWR_1D05V_SS

PC5214 SC1KP50V2KX-1DLGP

PR5203 100KR2F-L3-GP

PC5213 SCD01U50V2KX-1GP

PWR_1D05V_PH

PWR_1D05V_BT

PWR_1D05V_VFB

PL5201 COIL-1UH-34-GP-U1

PC5204 SCD1U25V2KX-1-DL-GP

PG5210 GAP-CLOSE-PWR-3-GP

PWR_1D05V_VFB_A

PR5202 3K16R2F-GP R1

PR5204 10KR2F-L1-GP R2

PC5212 SC220P50V2KX-3DLGP

PWR_1D05V

DY

PC5201 PC5203 PC5205 PC5207 PC5206

SC22U6D3V3MX-1-DL-GP

3D3V_S5

PR5208 100KR2J-1-GP DY

PWR_1D05V_PG

PWR_1D8V_PG R5202 1 2 PWR_1D05V_EN

0R0402-PAD

Vo=0.8x(1+R1/R2)
=0.8x(1+3.16/10)
=1.0528V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (AOZ2262_1D05V)

Size: A3 | Document Number: Selek CFL-H | Rev: A00

Date: Thursday, April 11, 2019 | Sheet 52 of 105

Main Func = 1D8V

OFFPAGE

[25] 3V_5V_DSW_OK

PH on EE Side

[52] PWR_1D8V_PG

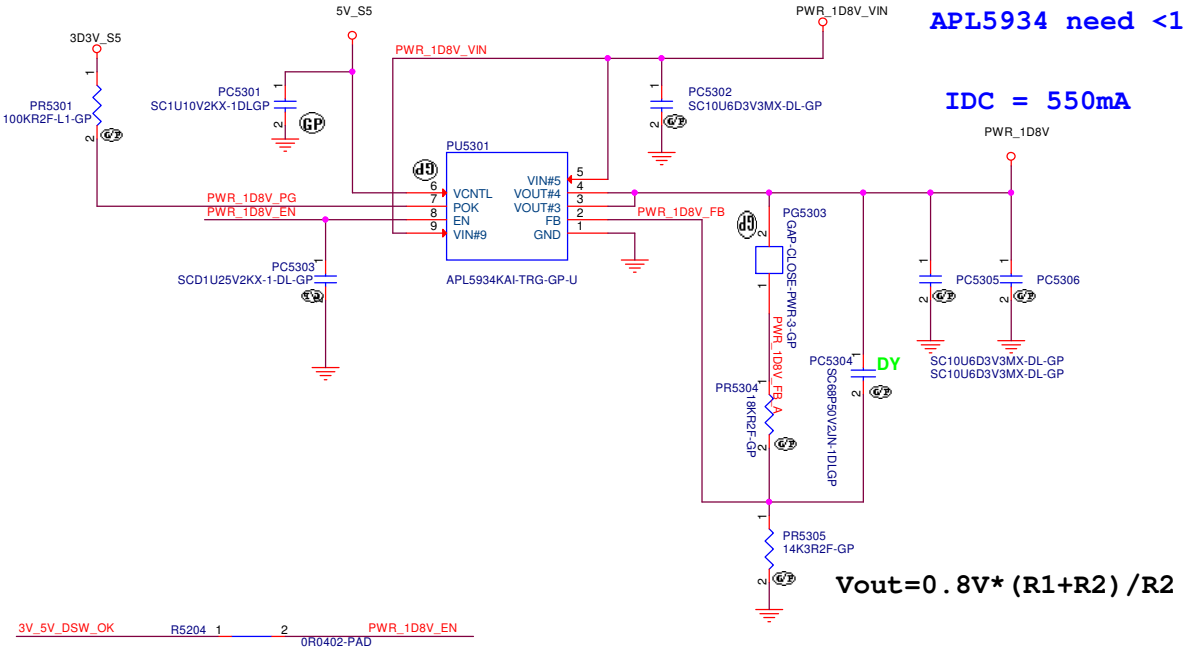
PWR_1D8V_PG

OFFPAGE_GAP

3D3V_S5 — PG5302 GAP-CLOSE-PWR-3-GP — PWR_1D8V_VIN

1D8V_S5 — PG5301 GAP-CLOSE-PWR-3-GP — PWR_1D8V

APL5934 for 1D8V



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	POWER (APL5934_1D8V)	
Size A3	Document Number Selek CFL-H	Rev A00
Date: Thursday, April 11, 2019	Sheet of	

NB694 for VCCIO

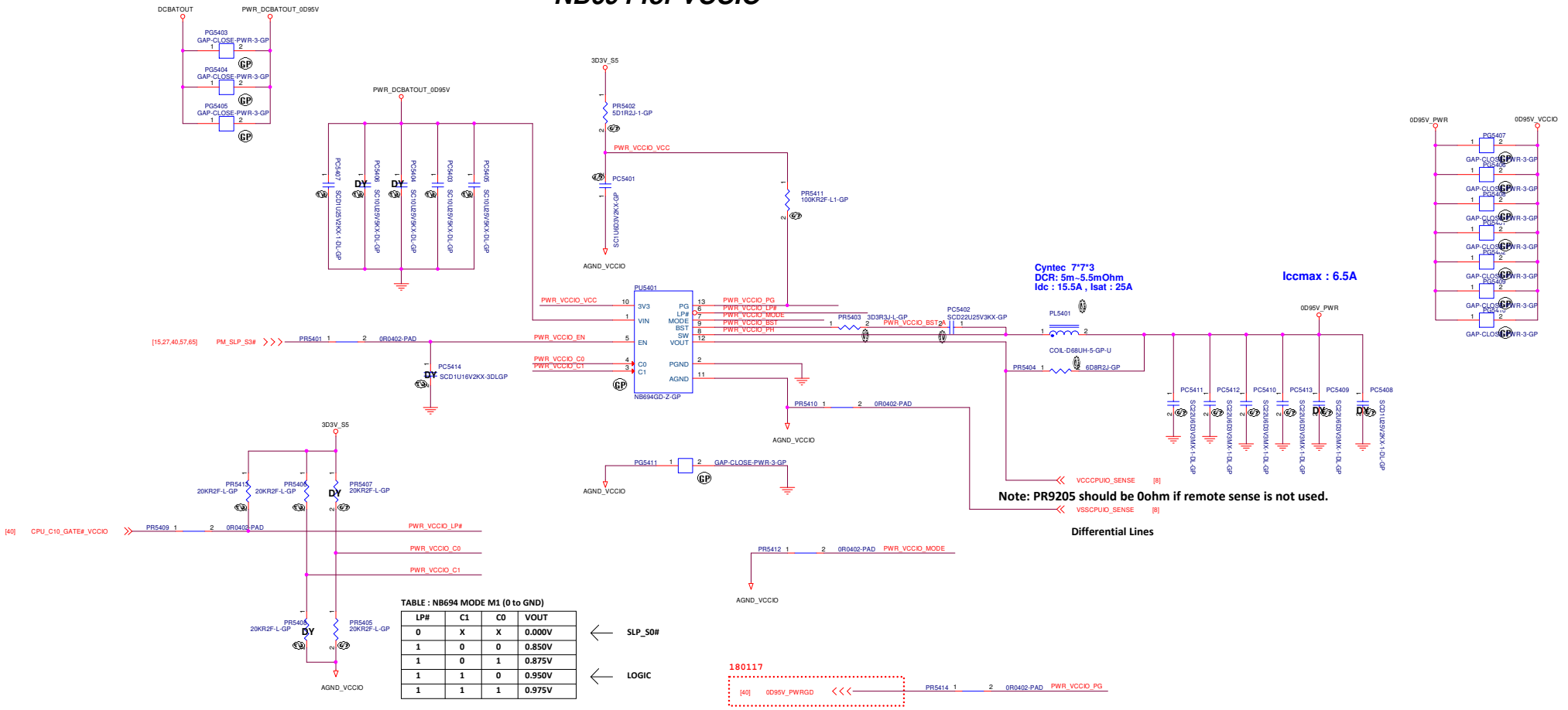
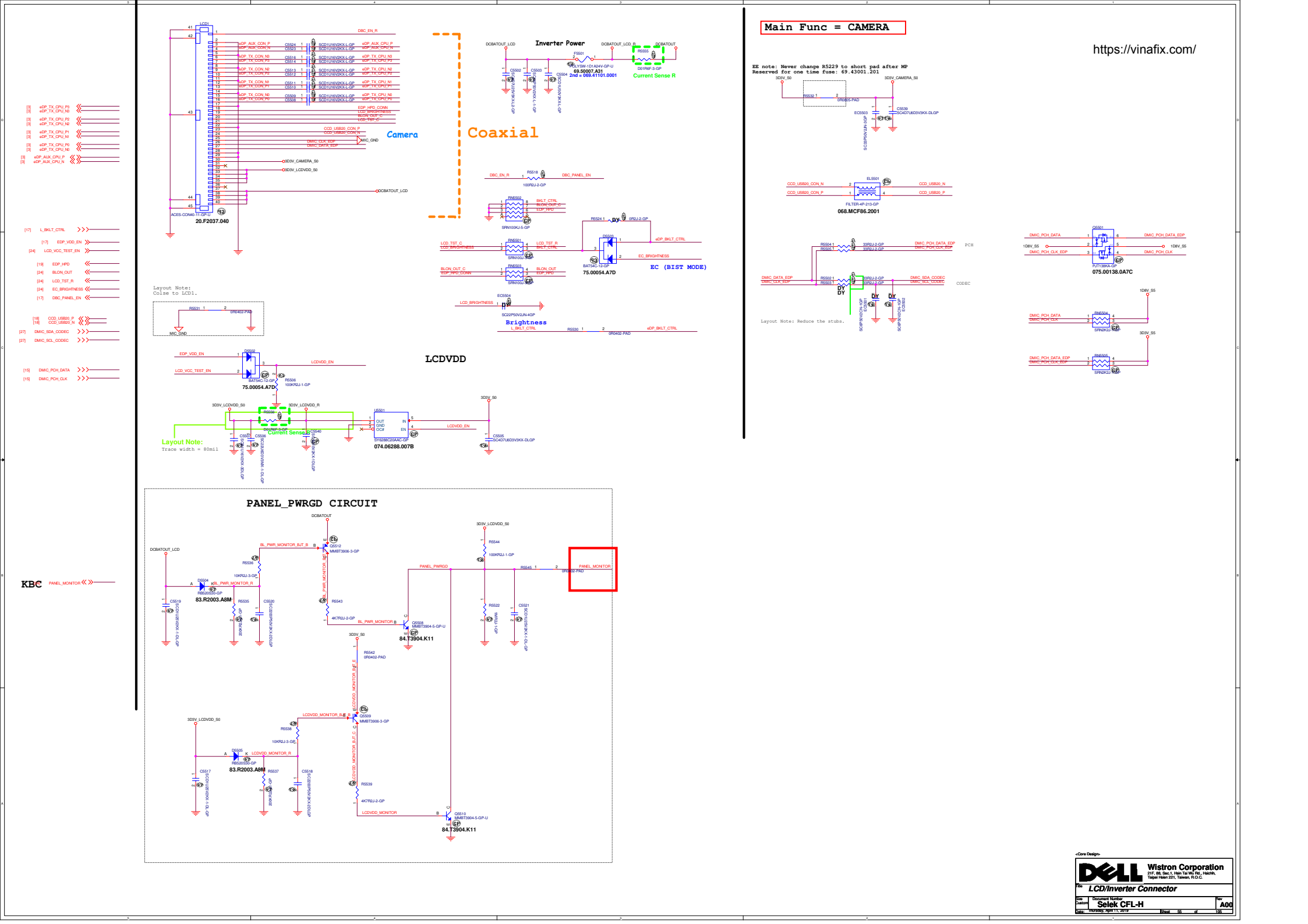


TABLE : NB694 MODE M1 (0 to GND)

LP#	C1	C0	VOUT	
0	X	X	0.000V	SLP_S0#
1	0	0	0.850V	
1	0	1	0.875V	
1	1	0	0.950V	LOGIC
1	1	1	0.975V	


Main Func = CAMERA
https://vinafix.com/
EE note: Never change R5229 to short pad after MP
Reserved for one time fuse: 69.43001.201
Camera
Coaxial
Inverter Power
Current Sense R
69.50007.A1
2nd = 069.41101.0001
Layout Note:
Colse to LCD1.
LCDVDD
Layout Note:
Trace width = 80mil
Current Sense
75.00054.A7D
74.06288.007B
EC (BIST MODE)
Brightness
75.00054.A7D
068.MCF86.2001
075.00138.0A7C
Layout Note: Reduce the stubs.
PANEL_PWRGD CIRCUIT
83.R2003.A8M
84.T3904.K11
KBC
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LCD/Inverter Connector
Selek CFL-H
A00

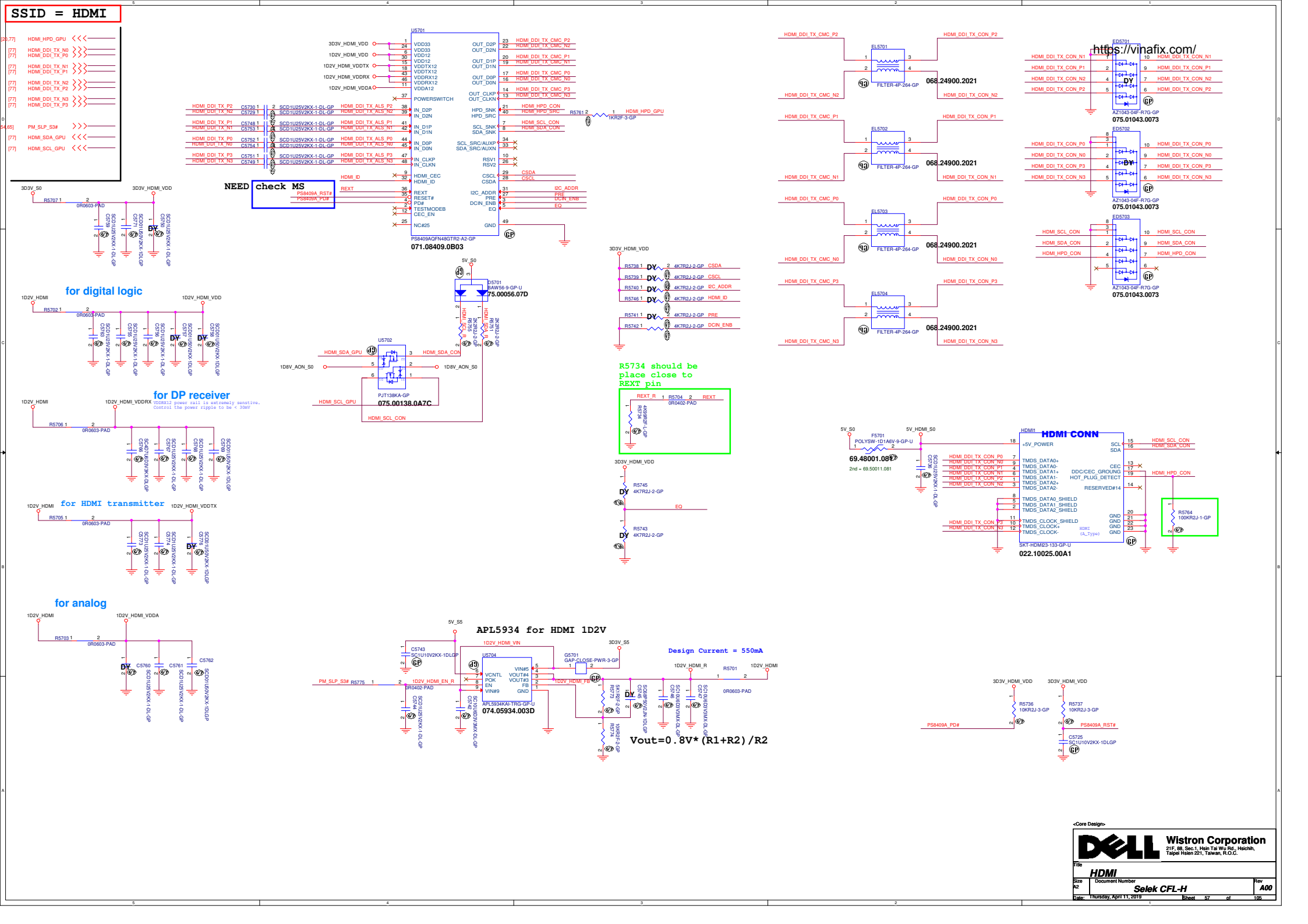
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LCD/Inverter Connector***

Size	Document Number	Rev
Custom	**Selek CFL-H**	**A00**

Date: Thursday, April 11, 2019 Sheet 56 of 105


SSID = HDMI
U5701
PS8409AQFN48GTR2-A2-GP
071.08409.0B03
NEED check MS
for digital logic
for DP receiver
for HDMI transmitter
for analog
U5702
PJT138KA-GP
075.00138.0A7C
D5701
BAW56-9-GP-U
075.00056.07D
R5734 should be place close to REXT pin
EL5701
EL5702
EL5703
EL5704
FILTER-4P-264-GP
068.24900.2021
ED5701
ED5702
ED5703
AZ1043-04F-R7G-GP
075.01043.0073
HDMI CONN
SKT-HDMI23-133-GP-U
022.10025.00A1
69.48001.08
APL5934 for HDMI 1D2V
U5704
APL5934KAI-TRG-GP-U
074.05934.003D
Design Current = 550mA
Vout=0.8V*(R1+R2)/R2
https://vinafix.com/
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
HDMI
Selek CFL-H
A00
Thursday, April 11, 2019
Sheet 57 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***(Reserved)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Thursday, April 11, 2019 Sheet 58 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

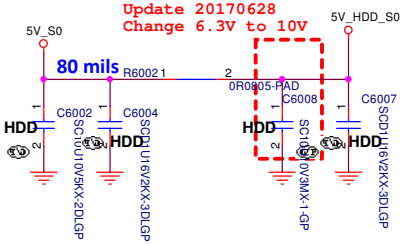
Date: Thursday, April 11, 2019 Sheet 59 of 105

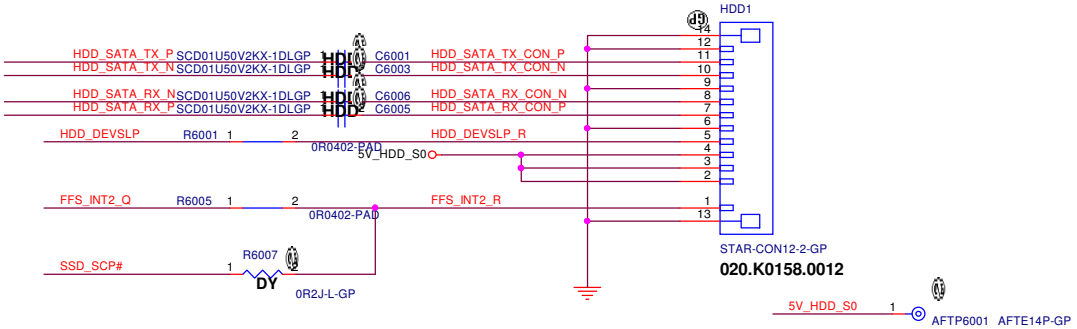
Main Func = HDD

SATA HDD Connector

[17] HDD_SATA_TX_P
[17] HDD_SATA_TX_N
[17] HDD_SATA_RX_N
[17] HDD_SATA_RX_P
[19] HDD_DEVSLP
[70] FFS_INT2_Q
[24,63] SSD_SCP#

Update 20170628
Change 6.3V to 10V





Layout Note:
Place near HDD1

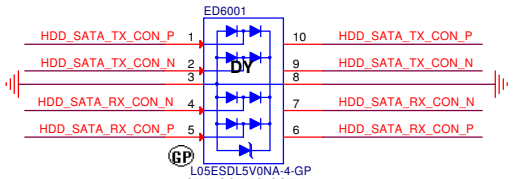


Table 16-5. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[1]	None[2]	None[3]

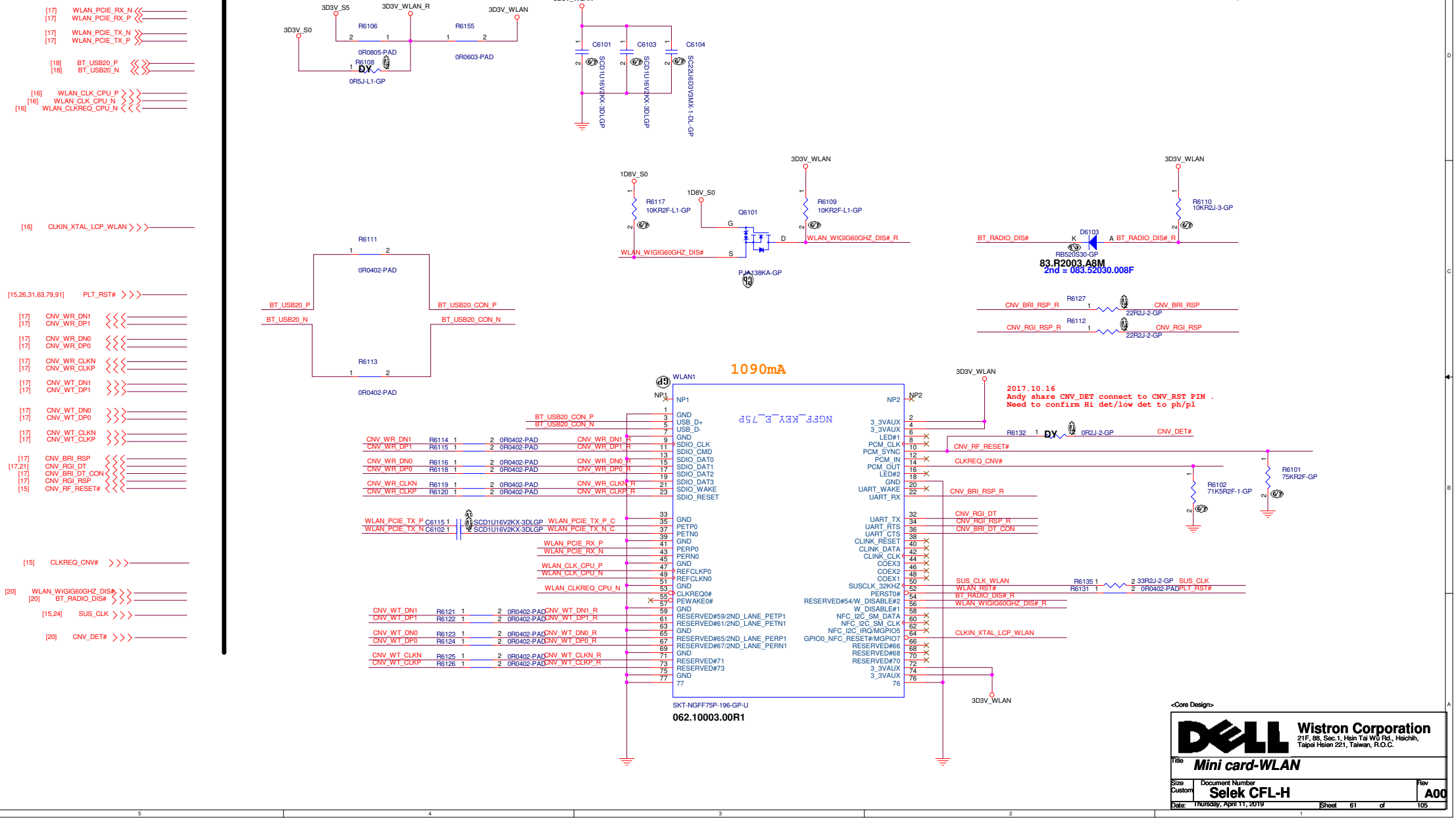
Notes:
1. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
2. For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
3. For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Use a non-interleaved breakout to isolate Tx and Rx.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SATA HDD
Size: Custom
Document Number: Selek CFL-H
Rev: A00
Date: Thursday, April 11, 2019
Sheet 60 of 105

Main Func = WLAN



SSID = Wireless

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)WWAN*

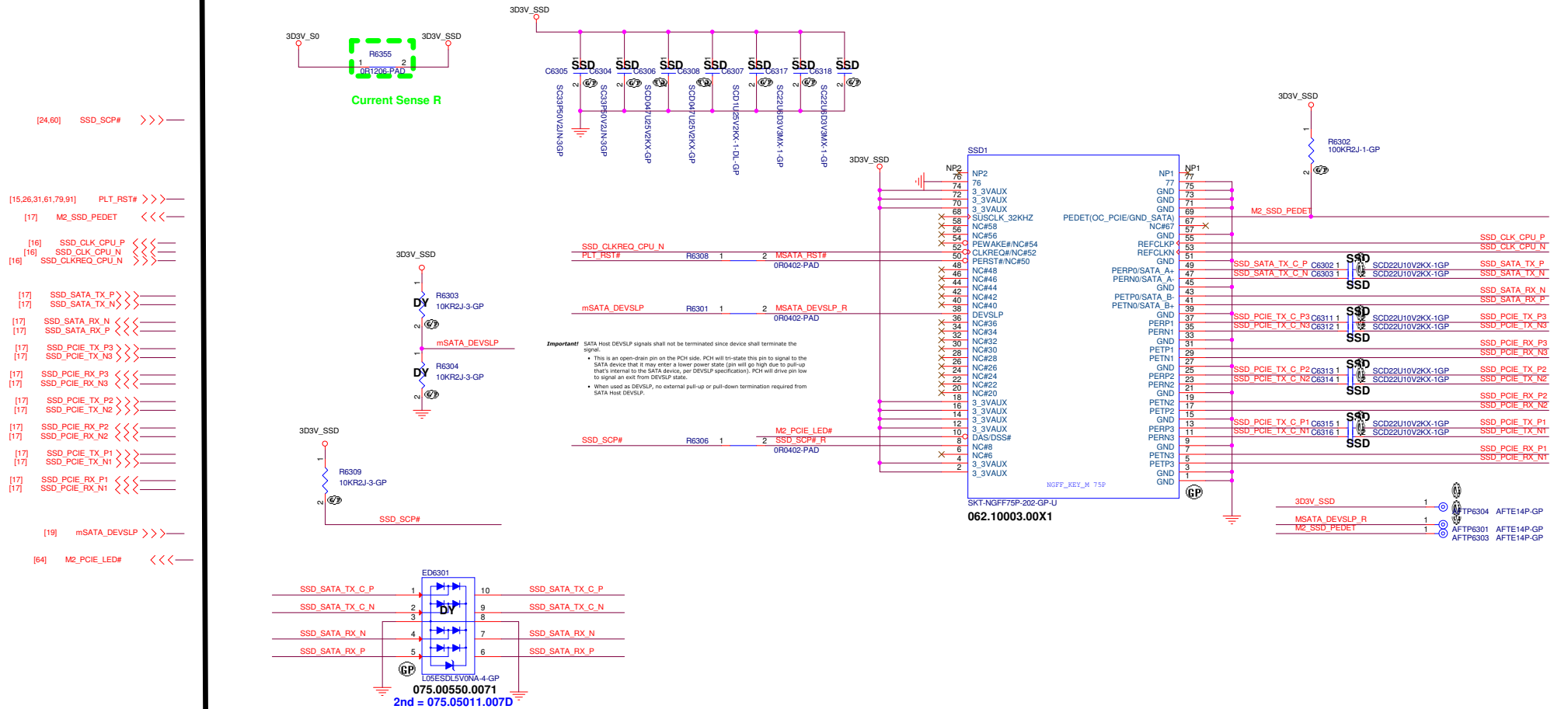
Size	Document Number	Rev
A	Selek CFL-H	A00

Date: Thursday, April 11, 2019 Sheet 62 of 105

Mini Card Connector (NGFF m-SATA)

SSID = m-SATA

https://vinafix.com/



[24,60] SSD_SCP#

[15,26,31,61,79,91] PLT_RST#

[17] M2_SSD_PEDET

[16] SSD_CLK_CPU_P

[16] SSD_CLK_CPU_N

[16] SSD_CLKREQ_CPU_N

[17] SSD_SATA_TX_P

[17] SSD_SATA_TX_N

[17] SSD_SATA_RX_N

[17] SSD_SATA_RX_P

[17] SSD_PCIE_TX_P3

[17] SSD_PCIE_TX_N3

[17] SSD_PCIE_RX_P3

[17] SSD_PCIE_RX_N3

[17] SSD_PCIE_TX_P2

[17] SSD_PCIE_TX_N2

[17] SSD_PCIE_RX_P2

[17] SSD_PCIE_RX_N2

[17] SSD_PCIE_TX_P1

[17] SSD_PCIE_TX_N1

[17] SSD_PCIE_RX_P1

[17] SSD_PCIE_RX_N1

[19] mSATA_DEVSLP

[64] M2_PCIE_LED#

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SSD-NGFF

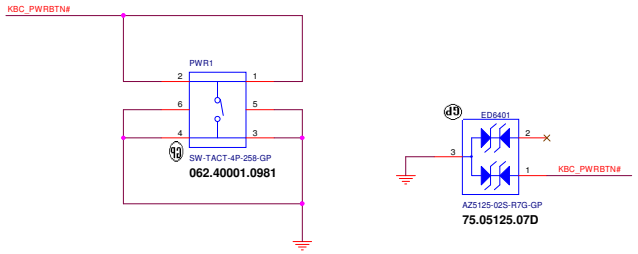
Size: Custom | Document Number: Selek CFL-H | Rev: A00

Date: Thursday, April 11, 2019 | Sheet 63 of 105

SSID = User.Interface

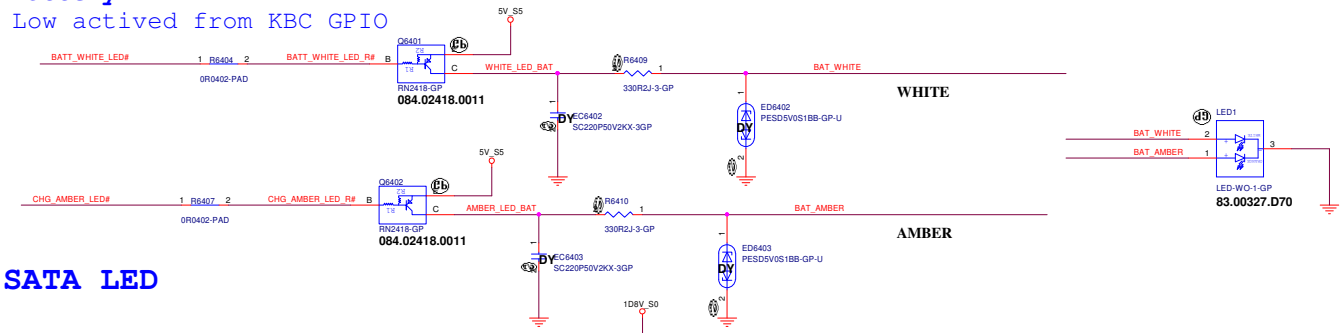
Power button

NONE FINGER PRINT 才會上件

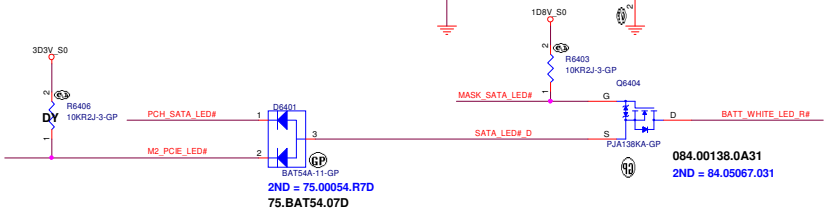


Battery LED1

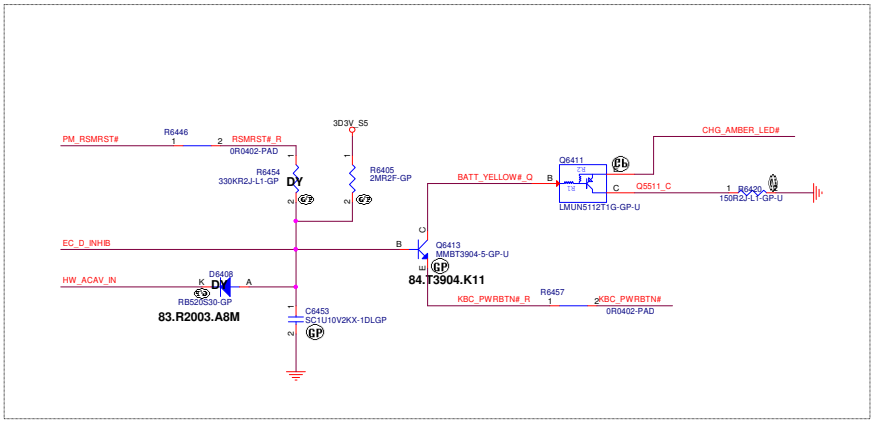
Low actived from KBC GPIO



SATA LED



M-BIST for G10 (Proposed schematic) follow bandon



Main Func = Keyboard

KB Backlight Power Consumption: 285mA max.

5V_S0 → R6501 POLYSW-1D1A6V-9-GP-U → +5V_KB_BL
69.48001.081
C6501 SCD1U25V2KX-1-GL-GP
KBBL1 STM-CON4-2-GP
020.K0311.0004
KB_LED_DET_C, KB_BL_CTRL#

KB1 STAR-CON60-2-GP
20.K0750.030
KSI[0..7], KSO[0..16], KB_DET#, CAP_LED

KB_BL_CTRL# → Q6501 AO3418L-GP
84.03418.A31
KBBL
KB_LED_PWM → R6509 100KR2J-1-GP
KB_BL_DET → R6507 51KR2J-1-GP, R6508 100KR2J-1-GP, Q6504

CAP LED Control
LOW actived from KBC GPIO

CAP_LED_R# → R6512 0R0402-PAD → Q6505 RN2418-GP
084.02418.0011
CAP_LED_Q → R6513 1KR2J-1-GP → CAP_LED
EC6507 SCP1P50U4LP

Main Func = TPAD

PS2
I2C

TP_VDD, TP_WAKE, NON TP_WAKE
DAT_TP_SIO_I2C_CLK, CLK_TP_SIO_I2C_DAT
CPU_I2C_SCL_P1, CPU_I2C_SDA_P1
I2CS_SCL_R, I2CS_SDA_R
TP_WAKE_KBC#, PTP_DIS#
TP1 PTWO-CON8-16-GP
020.K0255.0008
AFTP6540

Need to check if it is Active High or Active Low and check if there is PH on TPAD side.

X02 0415
R6511 10KR2J-3-GP → TP_WAKE_KBC#

Change pindefine SVT1 0210 1330

Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

AFTP6531, AFTP6534, AFTP6535, AFTP6536, AFTP6537

ACES-CON20-45-GP
020.K0400.0020
KBBL2
KB_LED_B4_DRV#, KB_LED_B3_DRV#, KB_LED_B2_DRV#, KB_LED_B1_DRV#, KB_LED_R4_DRV#, KB_LED_R3_DRV#, KB_LED_R2_DRV#, KB_LED_R1_DRV#, KB_BL_RGB_EN#

U6501 SY8288AAC-GP
074.06288.009B
2ND = 074.03553.007G
SC4D7U6D3V3KX-DL-GP, SC10U6D3V5MK-GP

L6501 BLM15AG121SN1-GP
SCD1U16V2KX-3GP, SCD01U16V2KX-3GP

U6502 STM32F070CBT6TA-GP
071.32070.000G
X6501 XTAL-12MHZ-115-GP
082.30000.0301
SC15P50V2JN-DL-GP

U6503 GD25Q80CSIGR-GP
072.25Q80.0E01
SPI_CLK, SPI_MOSI, SPI_MISO, SPI_CS#, SPI_HOLD#, SPI_SCLK, SPI_MOSI_C, SPI_WP#

BOOT0, ELC_NRST, BATT_LOW_LED, UART_2_CTXD_DRXD, UART_2_CRXD_DTXD
USB11_USB20_N, USB11_USB20_P, USART_RX, USART_TX, SPI_MOSI, SPI_MISO, SPI_SCK, SPI_CS#, SIO_SLP_S3, SIO_SLP_S5
PCIE_GEN1#_GEN2, LID_CL_SIO#_ELC, CAPLED_PWM1#, LOID_ON_ELC, PWM_I2C_DAT, TOBL_INT#, BATT_CHG_LED, HW_ACAV_IN_ELC

U6504 TLC59116IRHBR-QP
074.59116.0AE3
KB_LED_R1_DRV#, KB_LED_G1_DRV#, KB_LED_B1_DRV#, KB_LED_R2_DRV#, KB_LED_G2_DRV#, KB_LED_B2_DRV#, KB_LED_R3_DRV#, KB_LED_G3_DRV#, KB_LED_B3_DRV#, KB_LED_R4_DRV#, KB_LED_G4_DRV#, KB_LED_B4_DRV#
PWM_I2C_CLK, PWM_I2C_DAT, U6401_RESET#, U6401_REXT

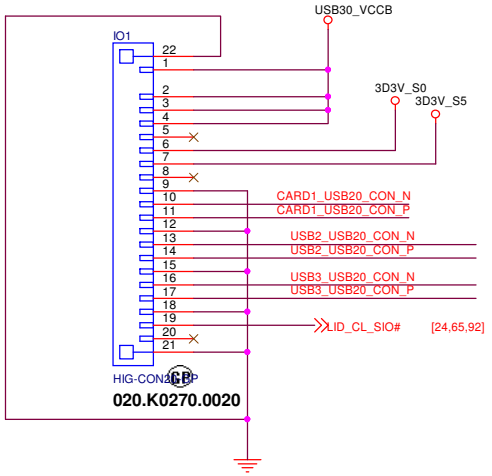
KB Backlight
AD0 0
AD1 1
AD2 0
AD3 0

Q6506 PJA138KA-GP
Q6507 PJA138KA-GP
SIO_SLP_S3, SIO_SLP_S5
[15,27,40,54,57] PM_SLP_S3#, [15,65] PM_SLP_S5#

D6507 BAW56-8-GP-U
75.00056.07D
LID_CL_SIO#_ELC, ELC_BL_EN#_ELC
Q6508 PJA138KA-GP
084.00138.0A31
ELC_BL_EN# [24]

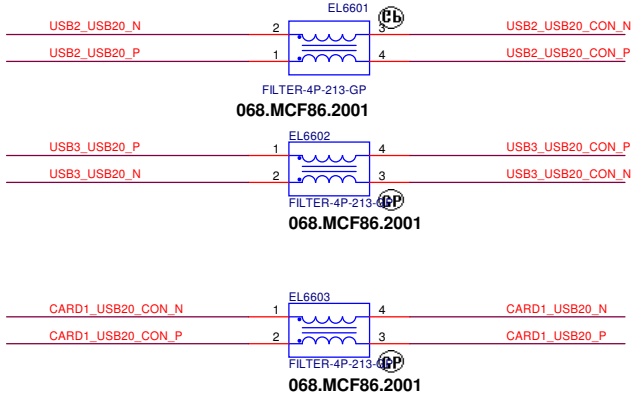
<Core Design>
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: Key Board&Touch Pad
Size: Custom | Document Number: Selek CFL-H | Rev: A00
Date: Thursday, April 11, 2019 | Sheet 65 of 105

[18] USB3_USB20_P
[18] USB3_USB20_N
[18] USB2_USB20_P
[18] USB2_USB20_N
[18] CARD1_USB20_P
[18] CARD1_USB20_N



Cardreader

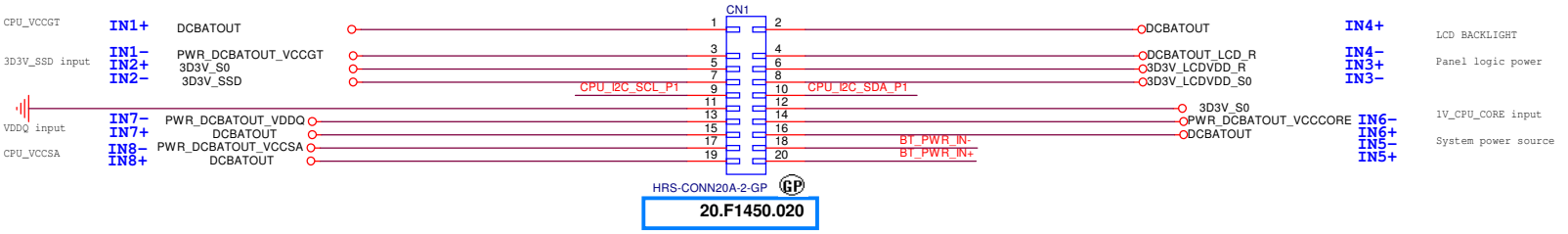
USB 2.0 Gen1 *2



[20,65] CPU_I2C_SCL_P1
[20,65] CPU_I2C_SDA_P1

[44] BT_PWR_IN+
[44] BT_PWR_IN-

E3 reserve



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
A3	Selek CFL-H	A00

Date: Thursday, April 11, 2019 Sheet 66 of 105

Main Func = Hall Sensor

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

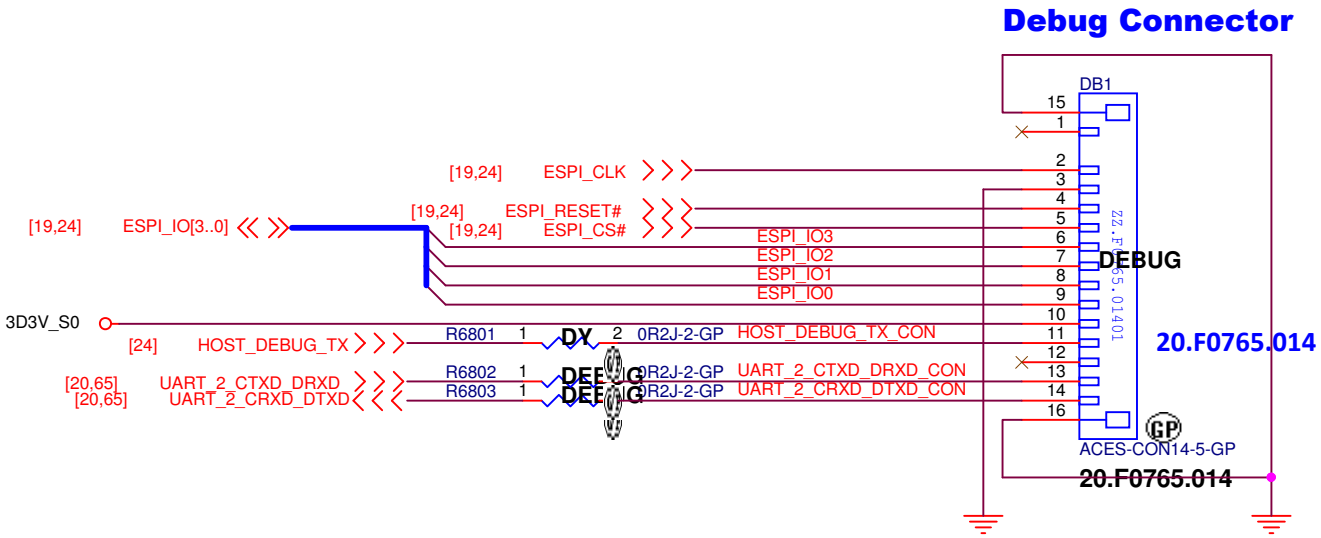
Title: *Hall Sensor*

Size	Document Number	Rev
A	Selek CFL-H	A00

Date: Thursday, April 11, 2019 Sheet 67 of 105

Main Func = Debug

https://vinafix.com/



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Dubug connector*		
Size: A4	Document Number: Selek CFL-H	Rev: A00
Date: Thursday, April 11, 2019	Sheet 68 of 105	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Selek CFL-H	A00

Date: Thursday, April 11, 2019 Sheet 69 of 105

SSID = Free Fall Sensor

https://vinafix.com/

[20] GSEN2_INT1_PCH
[20] GSEN2_INT2_PCH

[20] FFS_INT1
[15] FFS_INT2_PCH

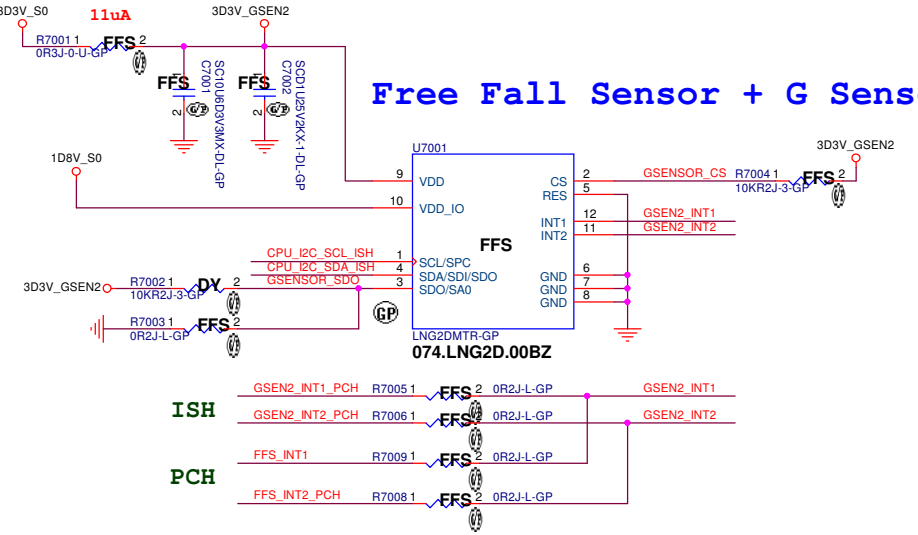
[20] CPU_I2C_SDA_ISH
[20] CPU_I2C_SCL_ISH

[24,65,66,92] LID_CL_SIO#

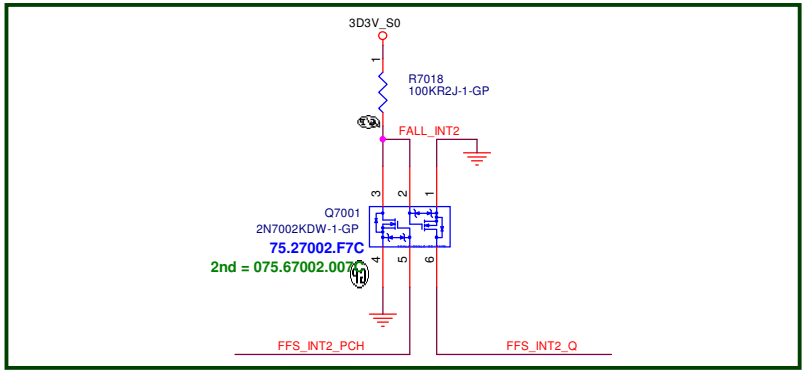
[60] FFS_INT2_Q

20180726 need DELL GPIO table

Free Fall Sensor + G Sensor



Please help to close with U6602



Note:

(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size: A3 | Document Number: *Selek CFL-H* | Rev: *A00*

Date: Thursday, April 11, 2019 | Sheet 70 of 105

Main Func = TYPEC MUX

From USB HOST

[19] USB4_USB30_RX_P
[19] USB4_USB30_RX_N
[19] USB4_USB30_TX_P
[19] USB4_USB30_TX_N

From CPU

[3] DP1_DDI_TX_P0
[3] DP1_DDI_TX_N0
[3] DP1_DDI_TX_P1
[3] DP1_DDI_TX_N1
[3] DP1_DDI_TX_P2
[3] DP1_DDI_TX_N2
[3] DP1_DDI_TX_P3
[3] DP1_DDI_TX_N3

[3] DP1_AUX_CPU_N
[3] DP1_AUX_CPU_P

From CCG4

[72] I2C_CLK_PD
[72] I2C_DATA_PD

From CCG5 to MUX

[19,72] CPU_DP_HPD_R

To Type-C CONNECTOR

[72] CCG5_SBU1
[72] CCG5_SBU2

[73] USB1_SSTX_CON_N1
[73] USB1_SSTX_CON_P1
[73] USB1_SSTX_CON_N2
[73] USB1_SSTX_CON_P2

[73] USB1_SSRX_CON_N1
[73] USB1_SSRX_CON_P1
[73] USB1_SSRX_CON_N2
[73] USB1_SSRX_CON_P2

From EC

[18,72] USB4_USB20_N
[18,72] USB4_USB20_P

Slave address : 0X38

USB HOST

CPU DP

Typec CONN

CPU

071.01046.0A03

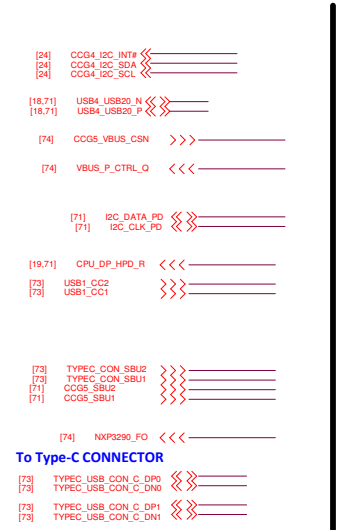
071.00212.0A03

Title: **RESERVED**

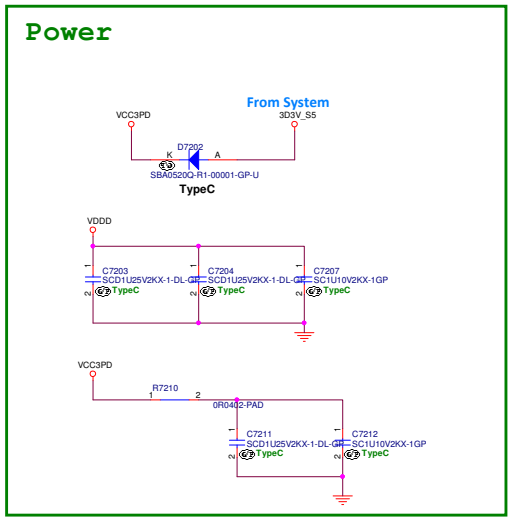
Size	Document Number	Rev
A1	Selek CFL-H	A00

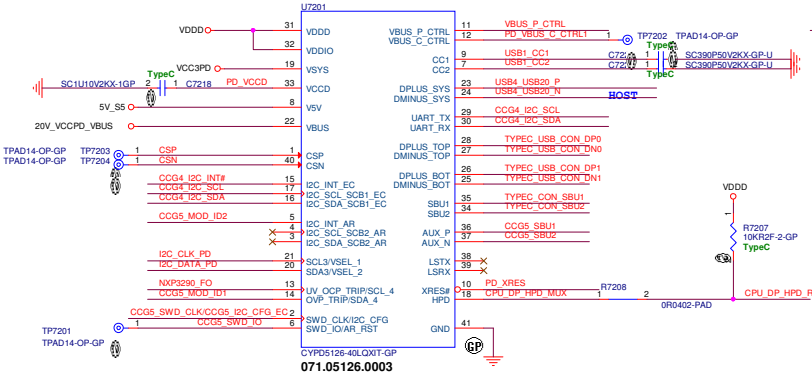
Date: Thursday, April 11, 2019 Sheet 71 of 105

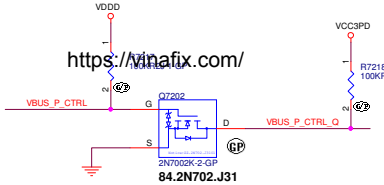
Main Func = TYPEC CONTROLLER

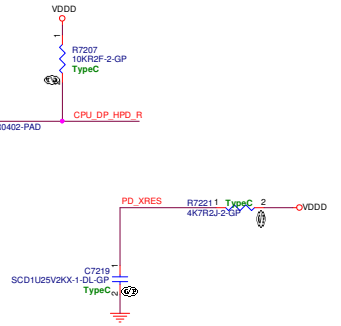


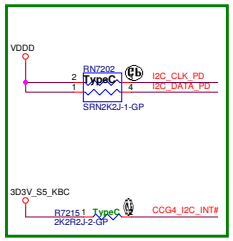
Power

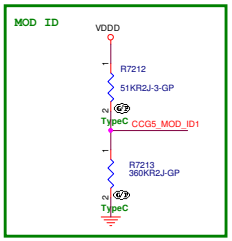


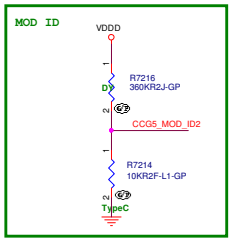


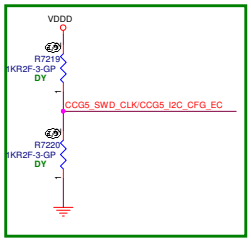


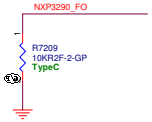


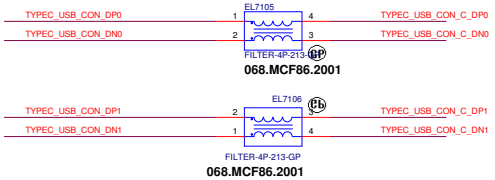












<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB3.0 PORT

Size	Document Number	Rev
Custom	Selek CFL-H	A00

Date: Thursday, April 11, 2019 Sheet 72 of 105

Main Func = TYPEC CONNECTOR

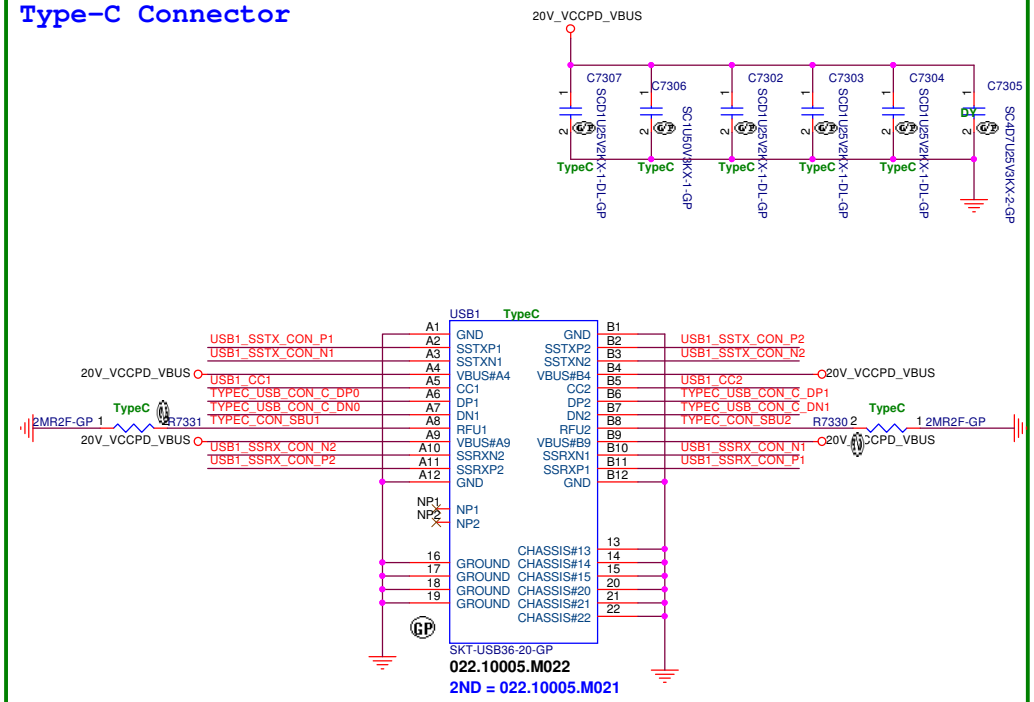
[71] USB1_SSRX_CON_N1
[71] USB1_SSRX_CON_P1
[71] USB1_SSRX_CON_N2
[71] USB1_SSRX_CON_P2
[71] USB1_SSTX_CON_N1
[71] USB1_SSTX_CON_P1
[71] USB1_SSTX_CON_N2
[71] USB1_SSTX_CON_P2

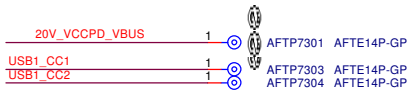
[72] TYPEC_CON_SBU1
[72] TYPEC_CON_SBU2
[72] USB1_CC1
[72] USB1_CC2

From USB2.0/ I2C Mux

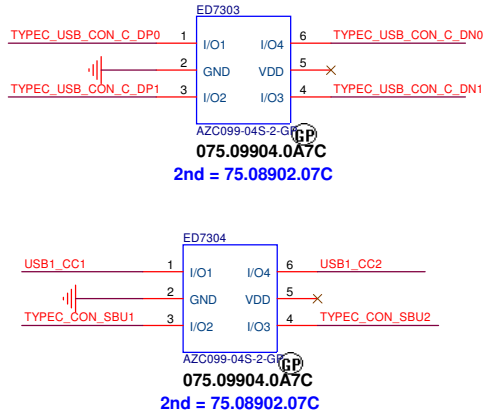
[72] TYPEC_USB_CON_C_DP0
[72] TYPEC_USB_CON_C_DN0
[72] TYPEC_USB_CON_C_DP1
[72] TYPEC_USB_CON_C_DN1

Type-C Connector

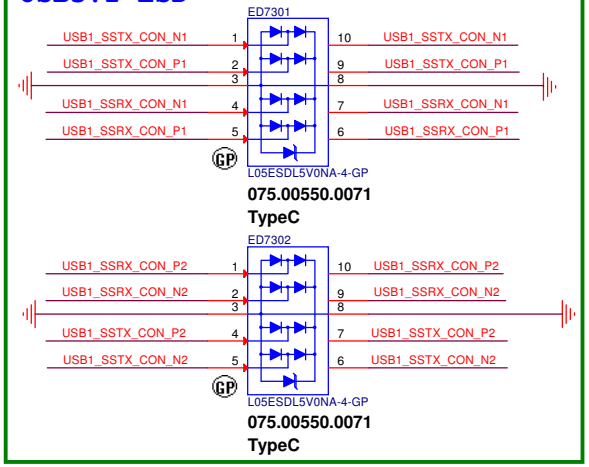




EMI



USB3.1 ESD



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TYPEC CONN**

Size: A3 | Document Number: **Selek CFL-H** | Rev: **A00**

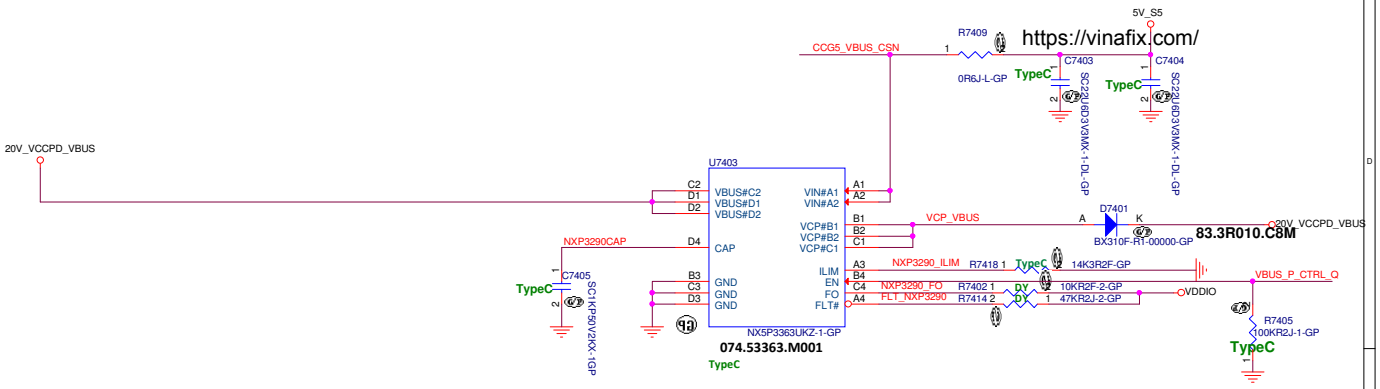
Date: Thursday, April 11, 2019 | Sheet 73 of 105

Main Func = LPS

[72] VBUS_P_CTRL_Q

[72] NXP3290_FO

[72] CCG5_VBUS_CSN



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LPS

Size: Custom | Document Number: Selek CFL-H | Rev: A00

Date: Thursday, April 11, 2019 | Sheet 74 of 105

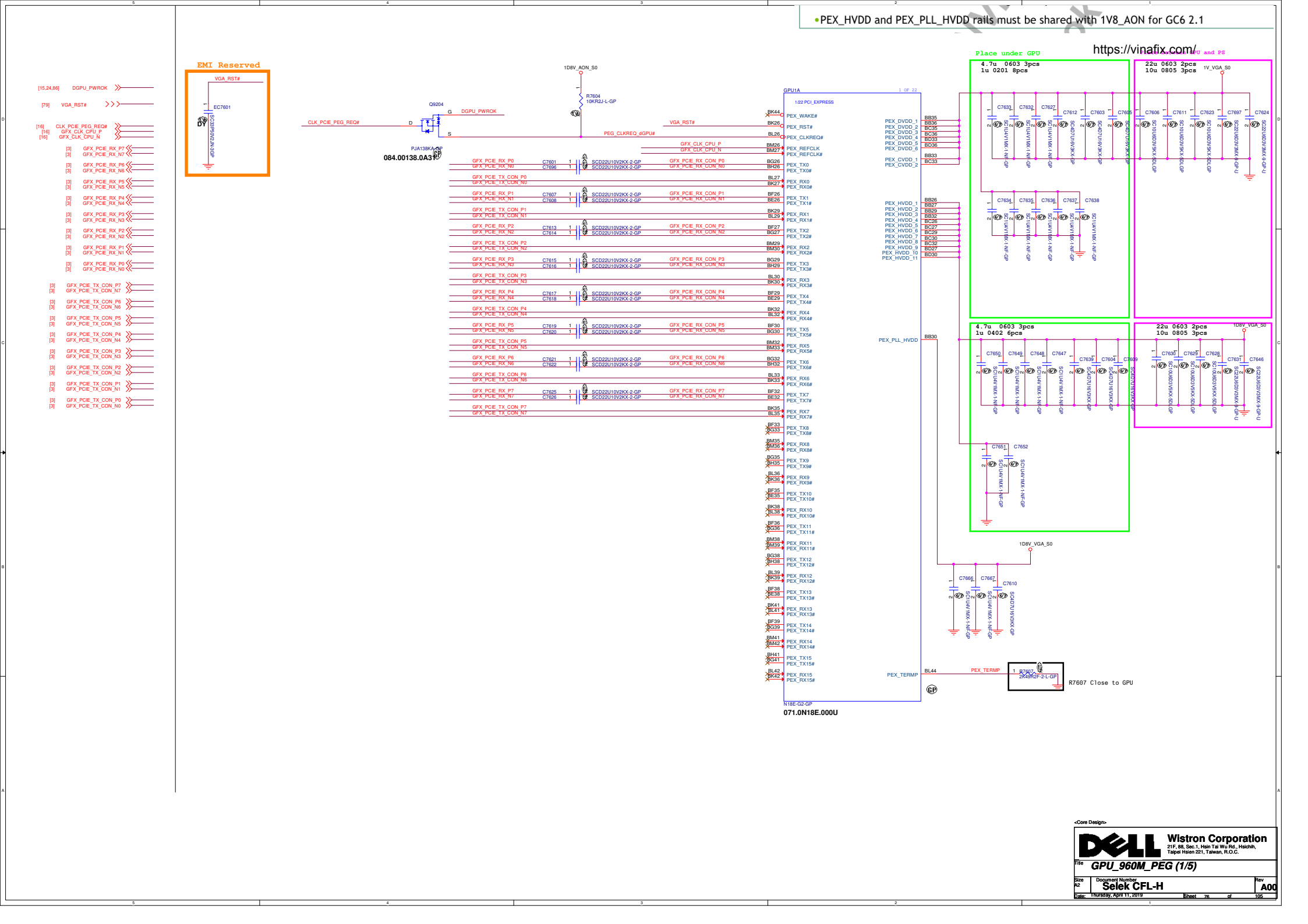
<Core Design>

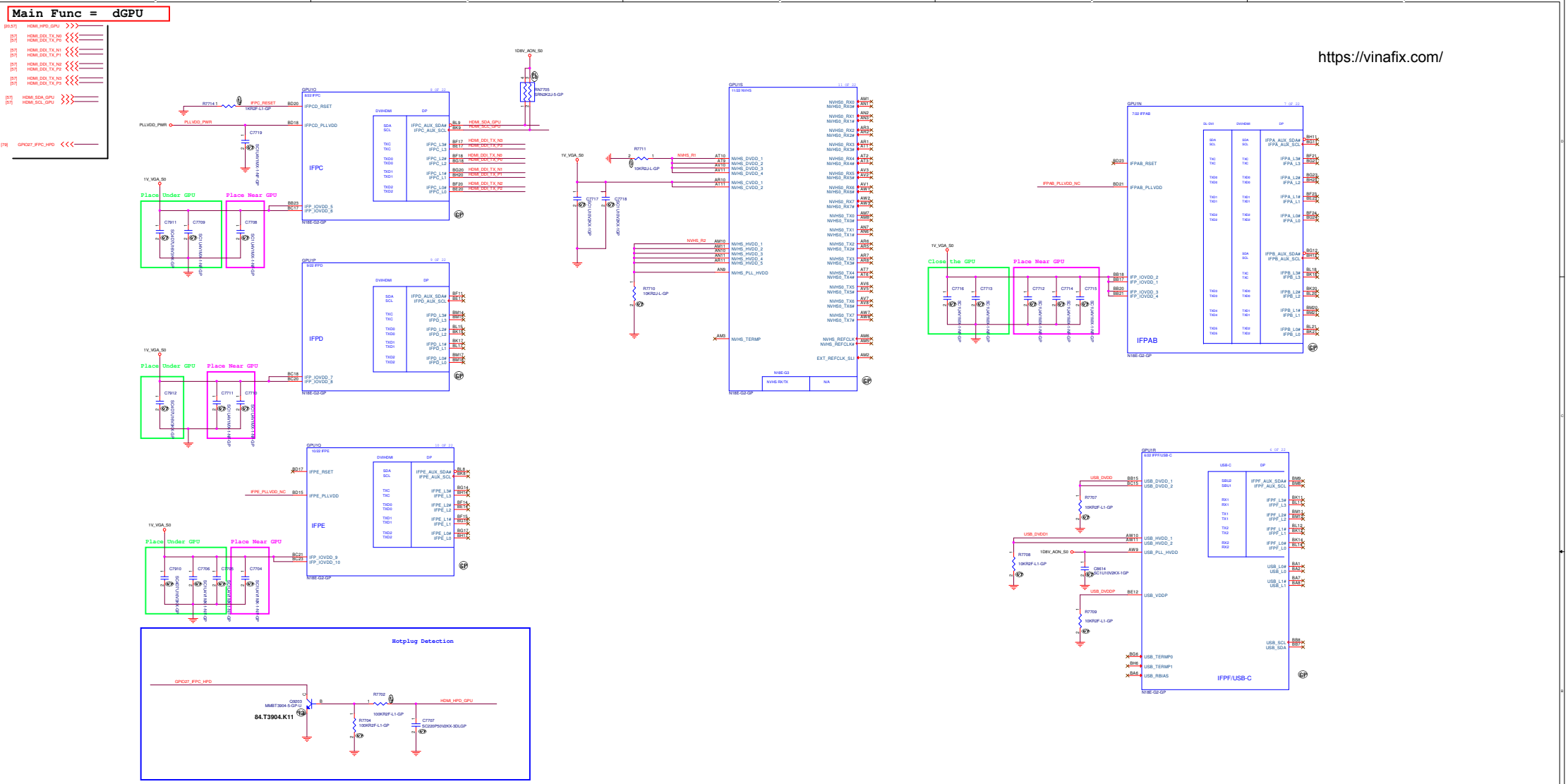
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)Thunderbolt (5/5)

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Thursday, April 11, 2019 Sheet 75 of 105


PEX_HVDD and PEX_PLL_HVDD rails must be shared with 1V8_AON for GC6 2.1
https://vinafix.com/
EMI Reserved
VGA_RST#
EC7601
SC682R5KN2-3GP
Place under GPU
4.7u 0603 3pcs
1u 0201 8pcs
22u 0603 2pcs
10u 0805 3pcs
1V_VGA_S0
4.7u 0603 3pcs
1u 0402 6pcs
22u 0603 2pcs
10u 0805 3pcs
1D8V_VGA_S0
1D8V_AON_S0
R7604
10KR2J-L-GP
Q9204
PJA138KA-GP
084.00138.0A31
DGPU_PWROK
CLK_PCIE_PEG_REQ#
VGA_RST#
PEG_CLKREQ_dGPU#
GPU1A
1_OF_22
1/22 PCI_EXPRESS
PEX_WAKE#
PEX_RST#
PEX_CLKREQ#
PEX_REFCLK
PEX_REFCLK#
PEX_TX0
PEX_TX0#
PEX_RX0
PEX_RX0#
PEX_TX1
PEX_TX1#
PEX_RX1
PEX_RX1#
PEX_TX2
PEX_TX2#
PEX_RX2
PEX_RX2#
PEX_TX3
PEX_TX3#
PEX_RX3
PEX_RX3#
PEX_TX4
PEX_TX4#
PEX_RX4
PEX_RX4#
PEX_TX5
PEX_TX5#
PEX_RX5
PEX_RX5#
PEX_TX6
PEX_TX6#
PEX_RX6
PEX_RX6#
PEX_TX7
PEX_TX7#
PEX_RX7
PEX_RX7#
PEX_TX8
PEX_TX8#
PEX_RX8
PEX_RX8#
PEX_TX9
PEX_TX9#
PEX_RX9
PEX_RX9#
PEX_TX10
PEX_TX10#
PEX_RX10
PEX_RX10#
PEX_TX11
PEX_TX11#
PEX_RX11
PEX_RX11#
PEX_TX12
PEX_TX12#
PEX_RX12
PEX_RX12#
PEX_TX13
PEX_TX13#
PEX_RX13
PEX_RX13#
PEX_TX14
PEX_TX14#
PEX_RX14
PEX_RX14#
PEX_TX15
PEX_TX15#
PEX_RX15
PEX_RX15#
PEX_DVDD_1
PEX_DVDD_2
PEX_DVDD_3
PEX_DVDD_4
PEX_DVDD_5
PEX_DVDD_6
PEX_CVDD_1
PEX_CVDD_2
PEX_HVDD_1
PEX_HVDD_2
PEX_HVDD_3
PEX_HVDD_4
PEX_HVDD_5
PEX_HVDD_6
PEX_HVDD_7
PEX_HVDD_8
PEX_HVDD_9
PEX_HVDD_10
PEX_HVDD_11
PEX_PLL_HVDD
PEX_TERMP
PEX_TERMP
R7607
2K49R2F-2-L-GP
R7607 Close to GPU
N18E-G2-GP
071.0N18E.000U
GFX_PCIE_RX_P0
GFX_PCIE_RX_N0
GFX_PCIE_TX_CON_P0
GFX_PCIE_TX_CON_N0
GFX_PCIE_RX_P1
GFX_PCIE_RX_N1
GFX_PCIE_TX_CON_P1
GFX_PCIE_TX_CON_N1
GFX_PCIE_RX_P2
GFX_PCIE_RX_N2
GFX_PCIE_TX_CON_P2
GFX_PCIE_TX_CON_N2
GFX_PCIE_RX_P3
GFX_PCIE_RX_N3
GFX_PCIE_TX_CON_P3
GFX_PCIE_TX_CON_N3
GFX_PCIE_RX_P4
GFX_PCIE_RX_N4
GFX_PCIE_TX_CON_P4
GFX_PCIE_TX_CON_N4
GFX_PCIE_RX_P5
GFX_PCIE_RX_N5
GFX_PCIE_TX_CON_P5
GFX_PCIE_TX_CON_N5
GFX_PCIE_RX_P6
GFX_PCIE_RX_N6
GFX_PCIE_TX_CON_P6
GFX_PCIE_TX_CON_N6
GFX_PCIE_RX_P7
GFX_PCIE_RX_N7
GFX_PCIE_TX_CON_P7
GFX_PCIE_TX_CON_N7
SCD22U10V2KX-2-GP
GFX_PCIE_RX_CON_P0
GFX_PCIE_RX_CON_N0
GFX_PCIE_RX_CON_P1
GFX_PCIE_RX_CON_N1
GFX_PCIE_RX_CON_P2
GFX_PCIE_RX_CON_N2
GFX_PCIE_RX_CON_P3
GFX_PCIE_RX_CON_N3
GFX_PCIE_RX_CON_P4
GFX_PCIE_RX_CON_N4
GFX_PCIE_RX_CON_P5
GFX_PCIE_RX_CON_N5
GFX_PCIE_RX_CON_P6
GFX_PCIE_RX_CON_N6
GFX_PCIE_RX_CON_P7
GFX_PCIE_RX_CON_N7
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GPU_960M_PEG (1/5)
Size
A2
Document Number
Selek CFL-H
Rev
A00
Date: Thursday, April 11, 2019
Sheet 76 of 105



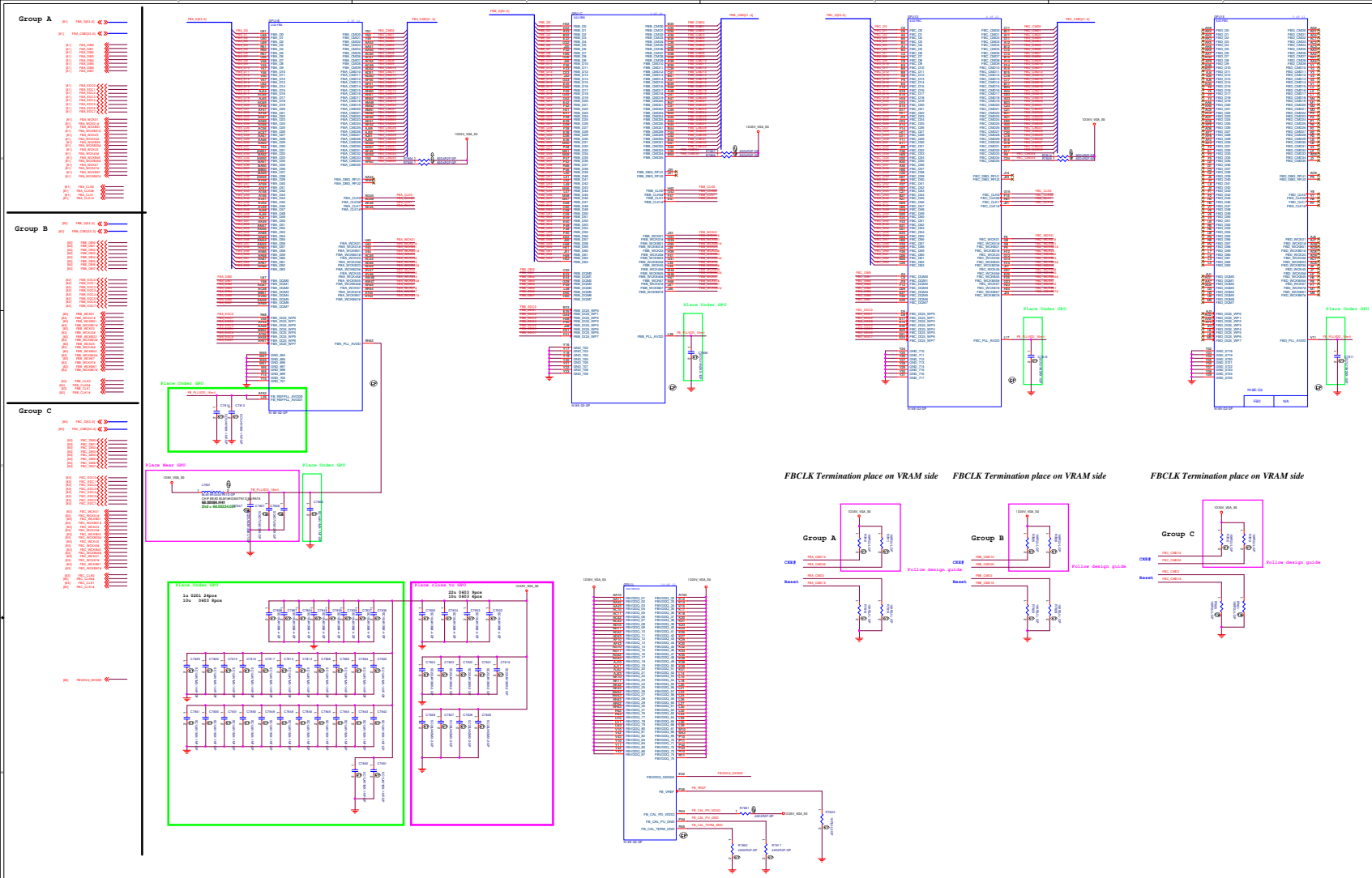
«Core Design»

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DIGITALOUT (2/5)

Size: Custom | Document Number: Selek CFL-H | Rev: A00

Date: Thursday, April 11, 2019 | Sheet 77 of 105



FBCLK Termination place on VRAM side

FBCLK Termination place on VRAM side

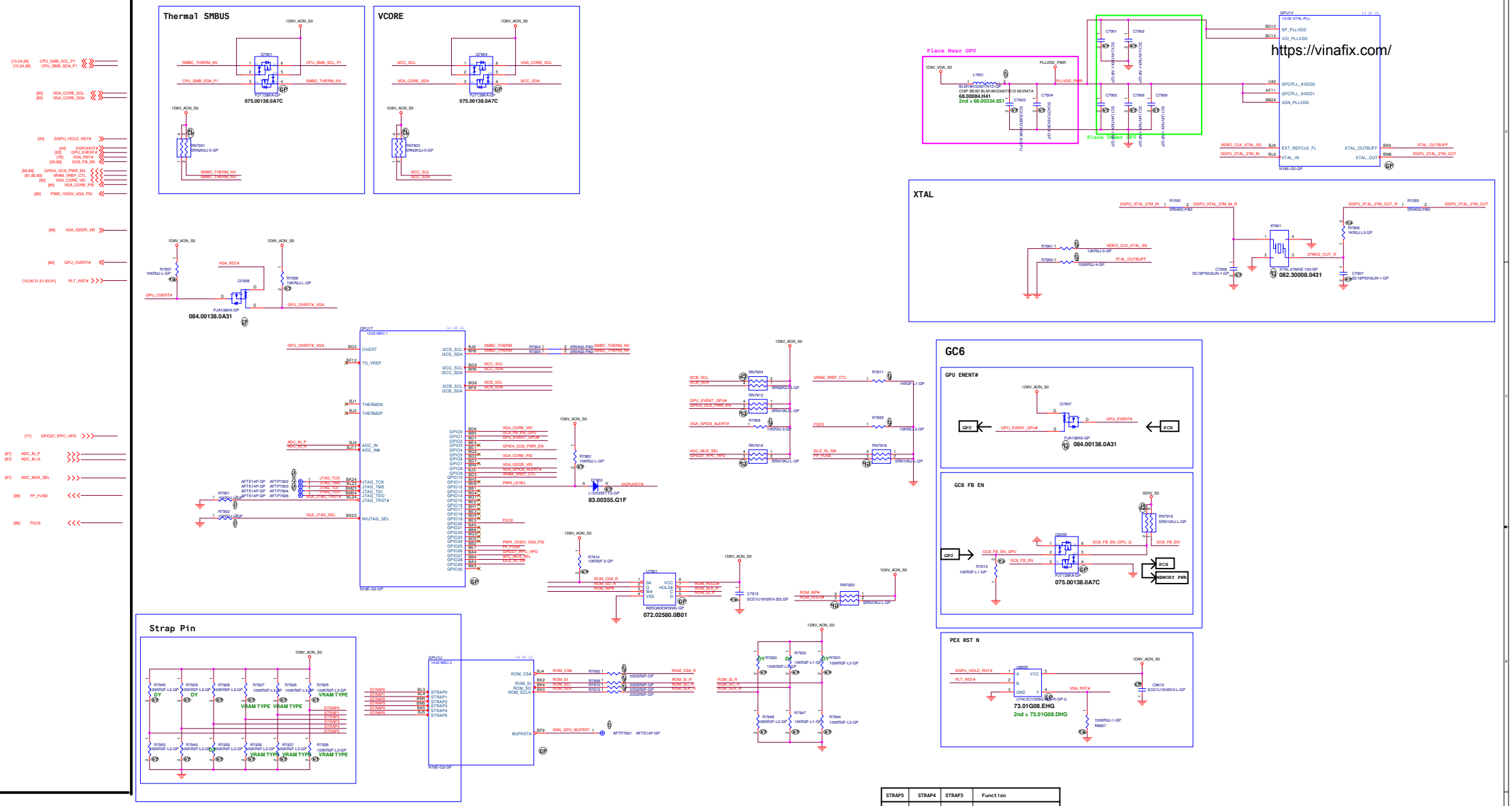
FBCLK Termination place on VRAM side

Wistron Corporation

GPU_VRAM I/F (3/5)

Selek CFL-H

A00



MEMORY STRAP

Table 12.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000) SAMSUNG
L	L	H	1 (0x0001) MICRON
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 2. N18E-G2/G1 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[2]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

Notes:
1. For N18E-G2/G1, the maximum allowable memory case temperature is 95 °C.
2. DVS is required. WCLK: TBD

Table 3. N18E-G0 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[2]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

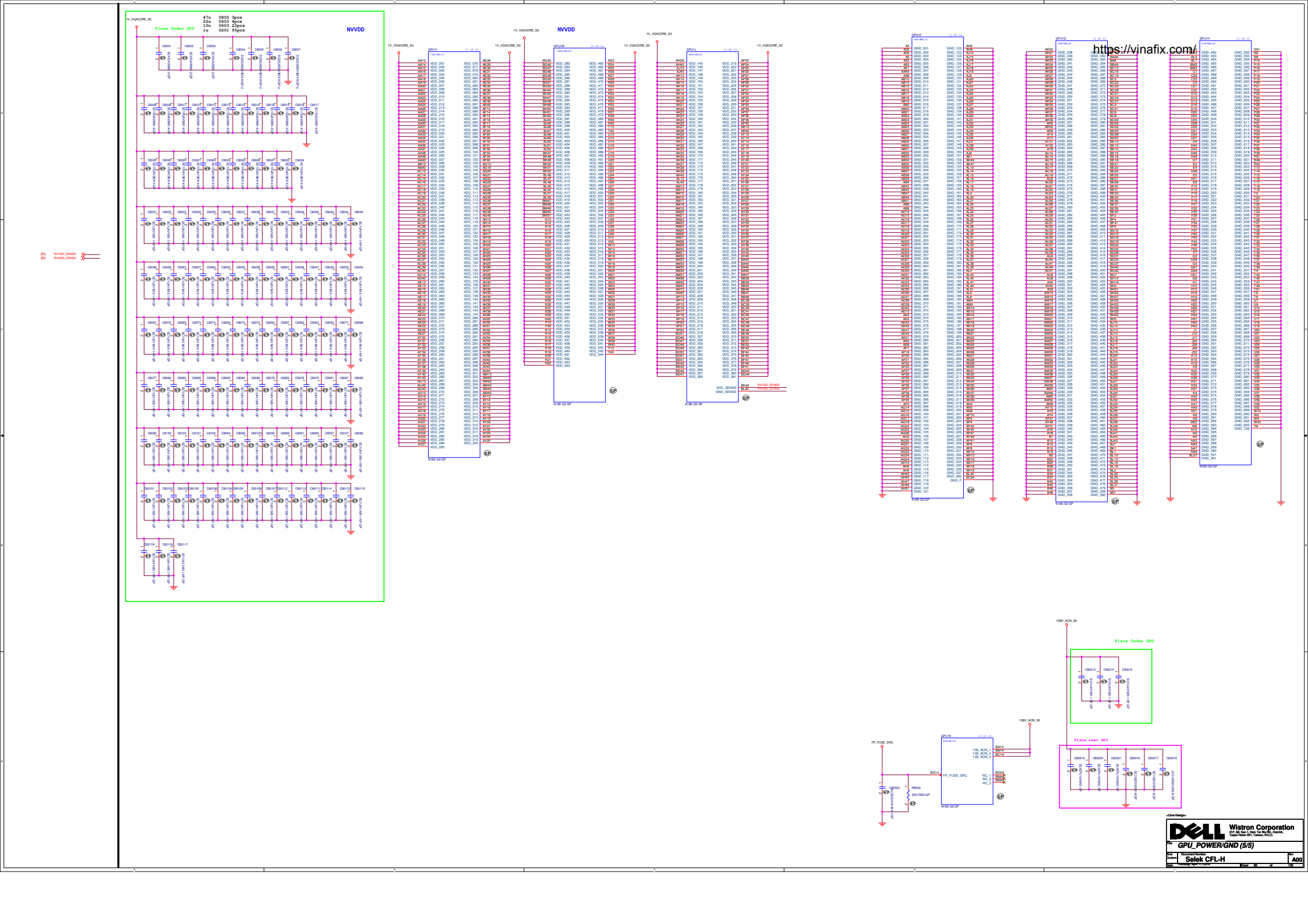
Notes:
1. For N18E-G0, the maximum allowable memory case temperature is 95 °C.
2. DVS is required. WCLK: TBD

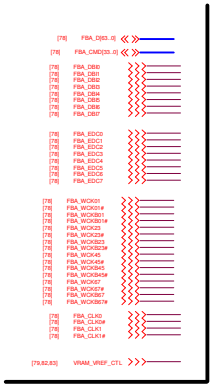
STRAP5	STRAP4	STRAP3	Function
L	L	H	as below picture

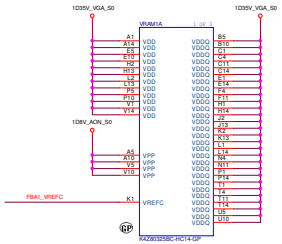
Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

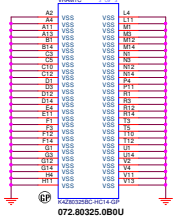
Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0

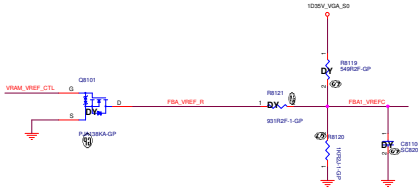
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
File: GPU_GPIO/STRAP
Size: A1 | Document Number: Selek CFL-H | Rev: A00
Date: Thursday, April 11, 2019 | Sheet 79 of 105

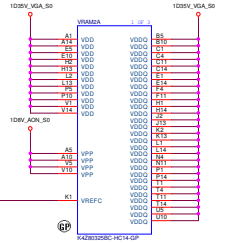


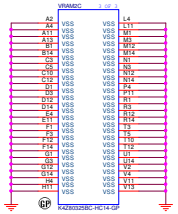




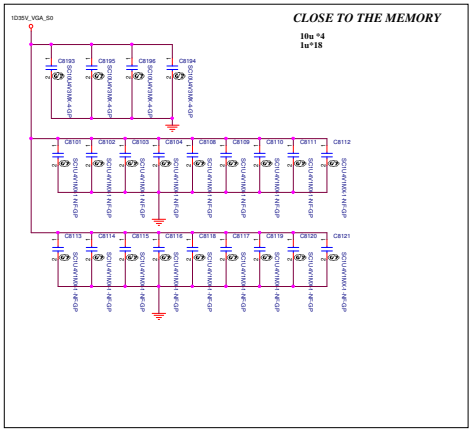




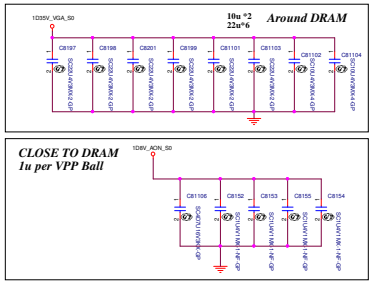




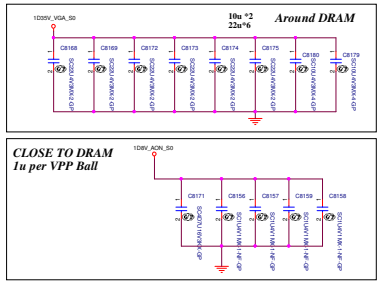
FOR VRAM1



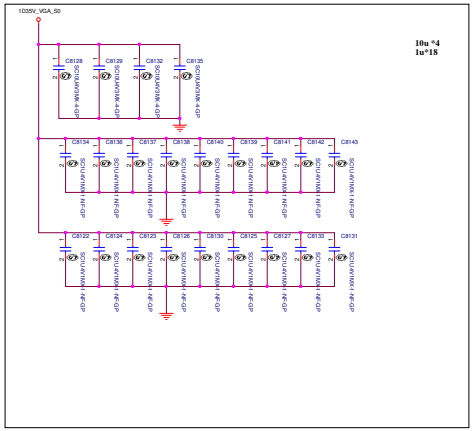
FOR VRAM1



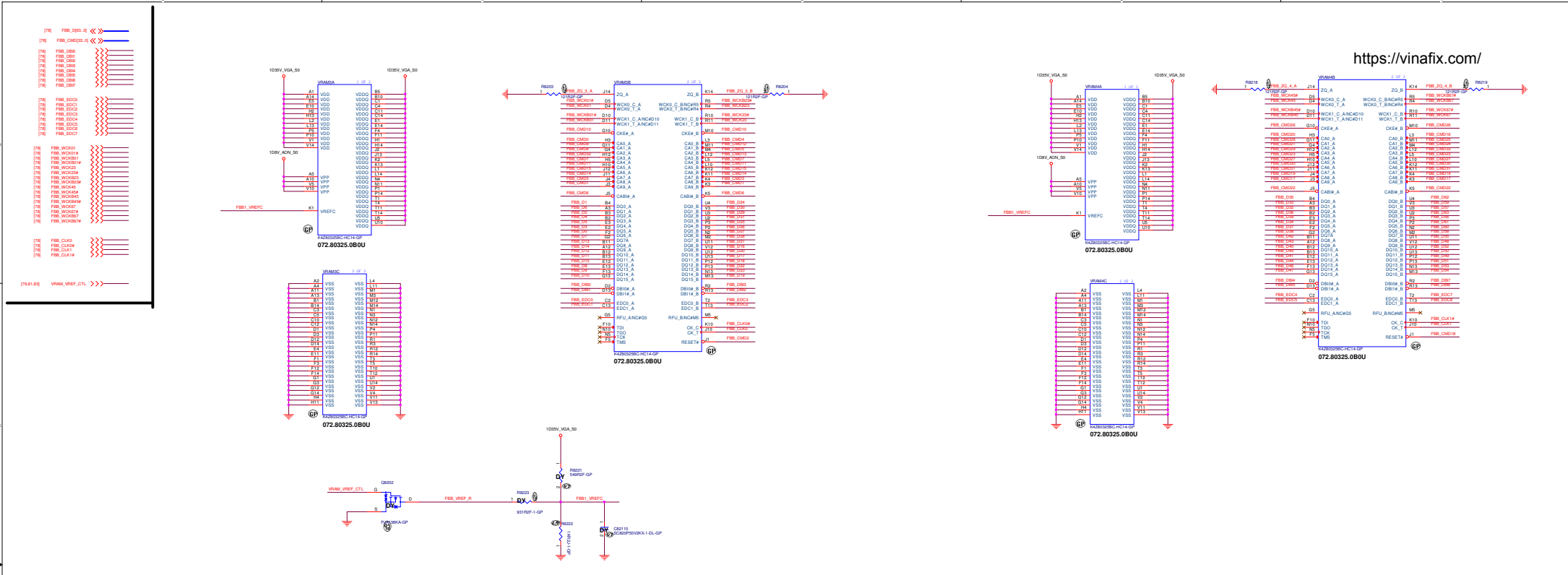
FOR VRAM2



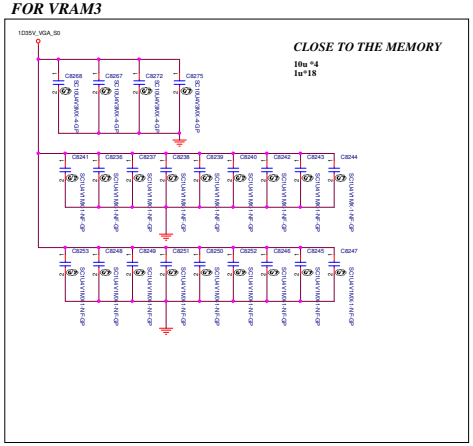
FOR VRAM2



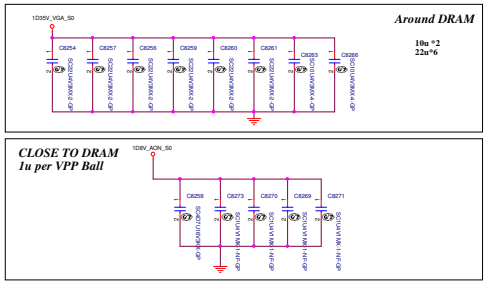
«Core Design»
DELL
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: VRAM 1,2 (1/4)
Size: A3
Document Number: Selek CFL-H
Rev: A00
Date: Thursday, April 11, 2019
Sheet 83 of 105



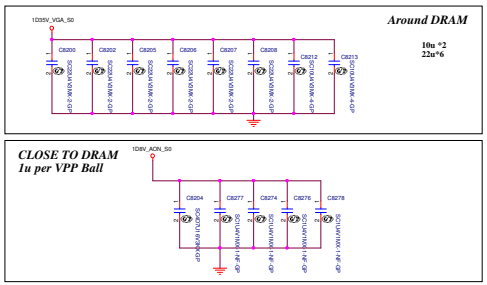
FOR VRAM3



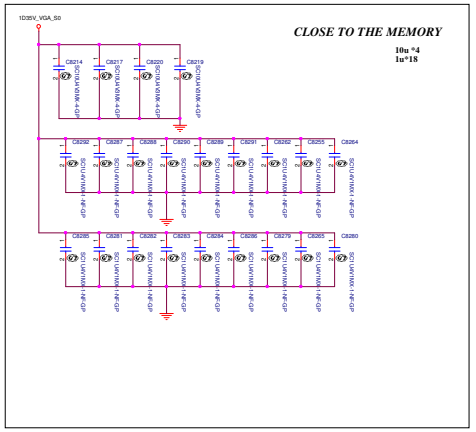
FOR VRAM3



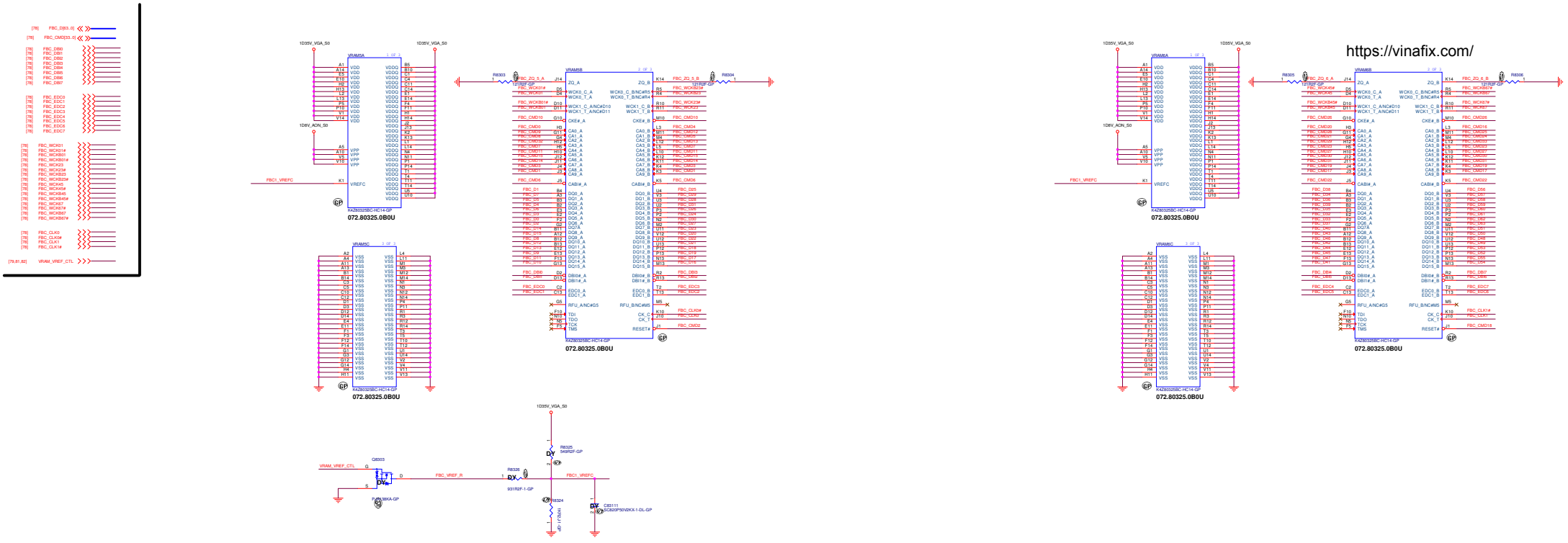
FOR VRAM4



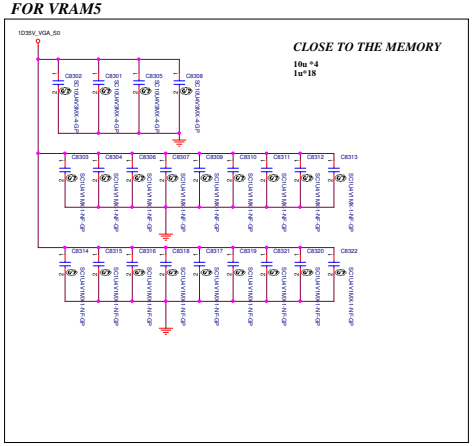
FOR VRAM4



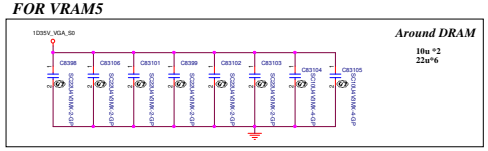
Wistron Corporation		
Title: VRAM 3,4 (2/4)		
Size: A3	Document Number: Selek CFL-H	Rev: A00
Date: Thursday, April 11, 2019	Sheet 82 of 105	

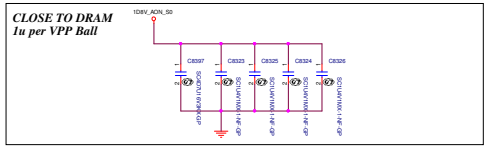


FOR VRAM5

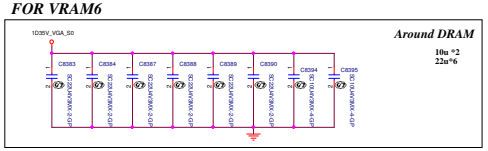


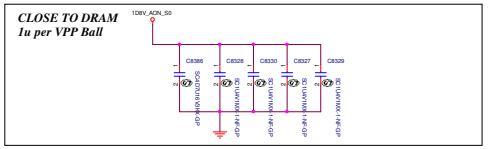
FOR VRAM5



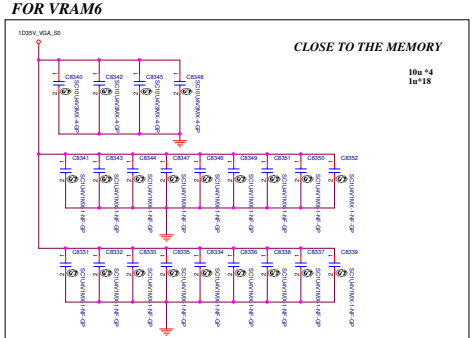


FOR VRAM6





FOR VRAM6



«Core Design»

Wistron Corporation
21F, 88, Sec.1, Nan Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: *VGA Power A*

Size	Document Number	Rev
A3	Selek CFL-H	A00

Date: Thursday, April 11, 2019 Sheet 83 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File: VGA Power B

Size	Document Number	Rev
A1	Selek CFL-H	A00

Date: Thursday, April 11, 2019 Sheet 84 of 105

OFFPAGE

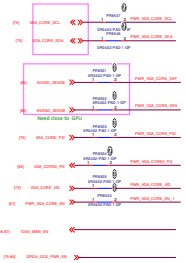


Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification		
	Unit	Config
Number of Voltage Levels til	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{OMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.249
C	nF	0.1

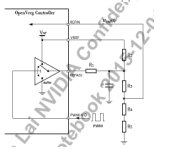
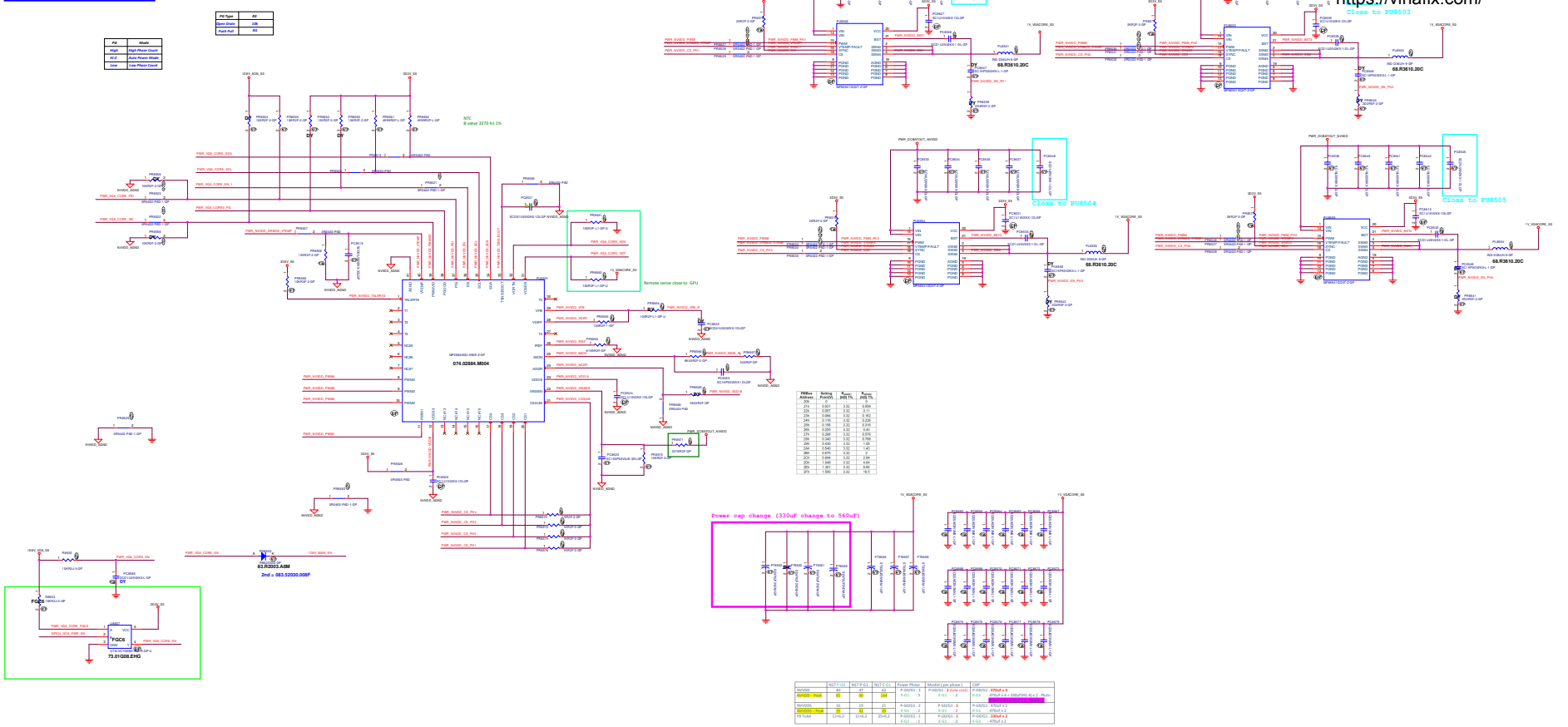


Table 7.9 PWM-VID Spec and Component Values

PWM-VID Specification		
		Config
Vmin	V	0.3
Vmax	V	1.3
Vboot	V	0.8
Voltage Step Vstep	mV	6.25
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{OMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.249
C	nF	0.1

Pin Type	Att
Open Drain	10k
Push Pull	No

Pin	Mode
High	High Phase Count
Hi-Z	Auto Power Mode
Low	Low Phase Count



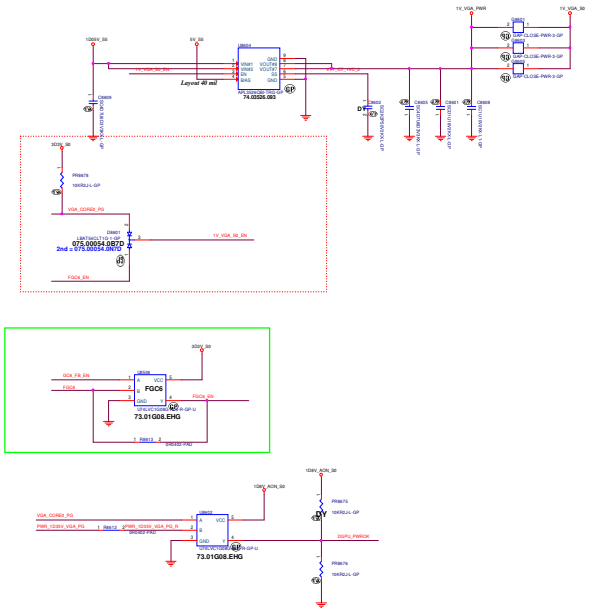
Wistron Corporation

GPU VCORE POWER

Selak CFL-H

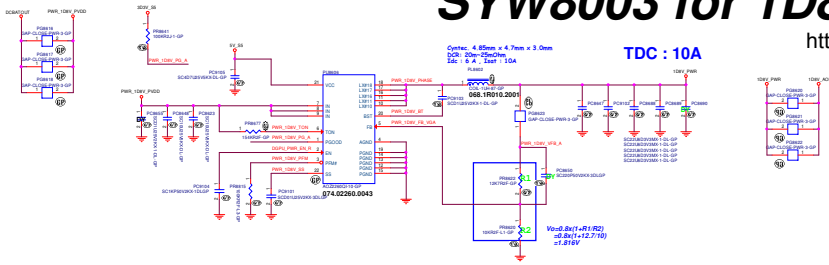
OFFPAGE

APL3526QB for 1V_VGA_S0

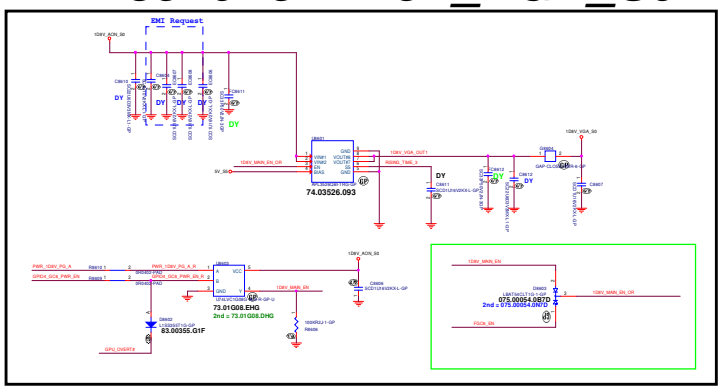


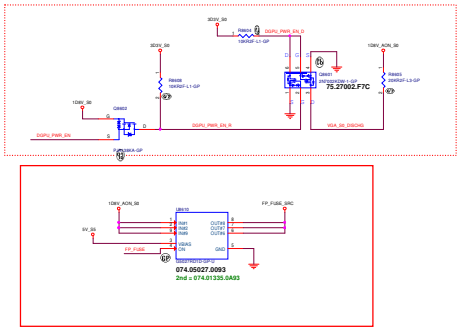
SYW8003 for 1D8V_AON

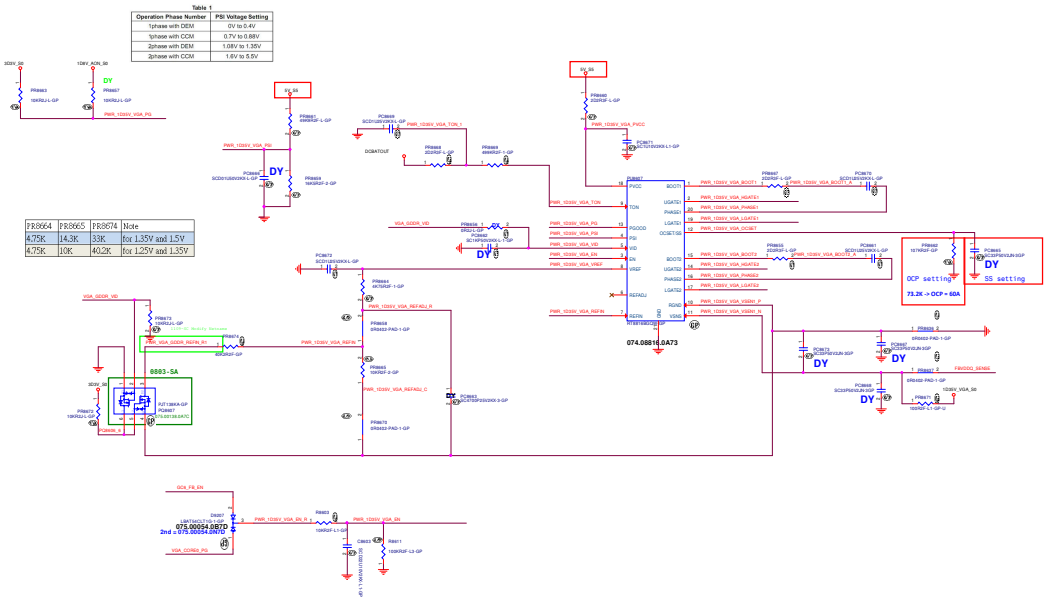
https://vinafix.com/

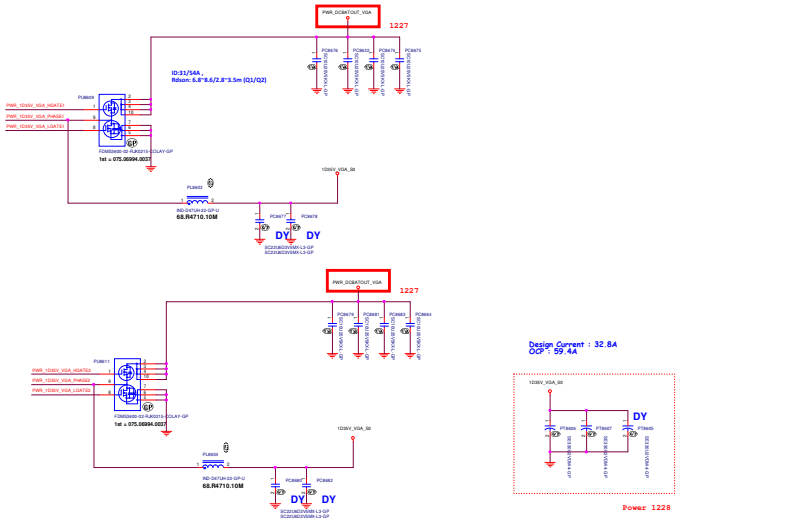


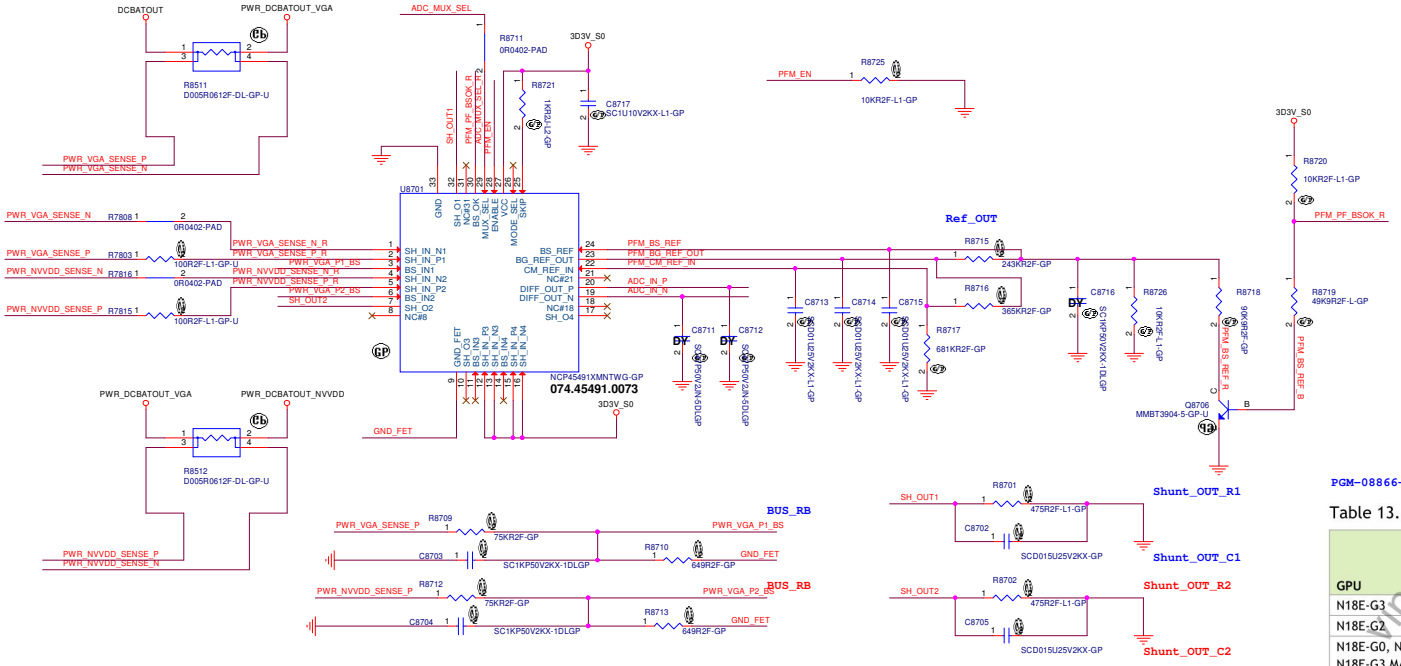
APL3526 for 1D8V_VGA_S0









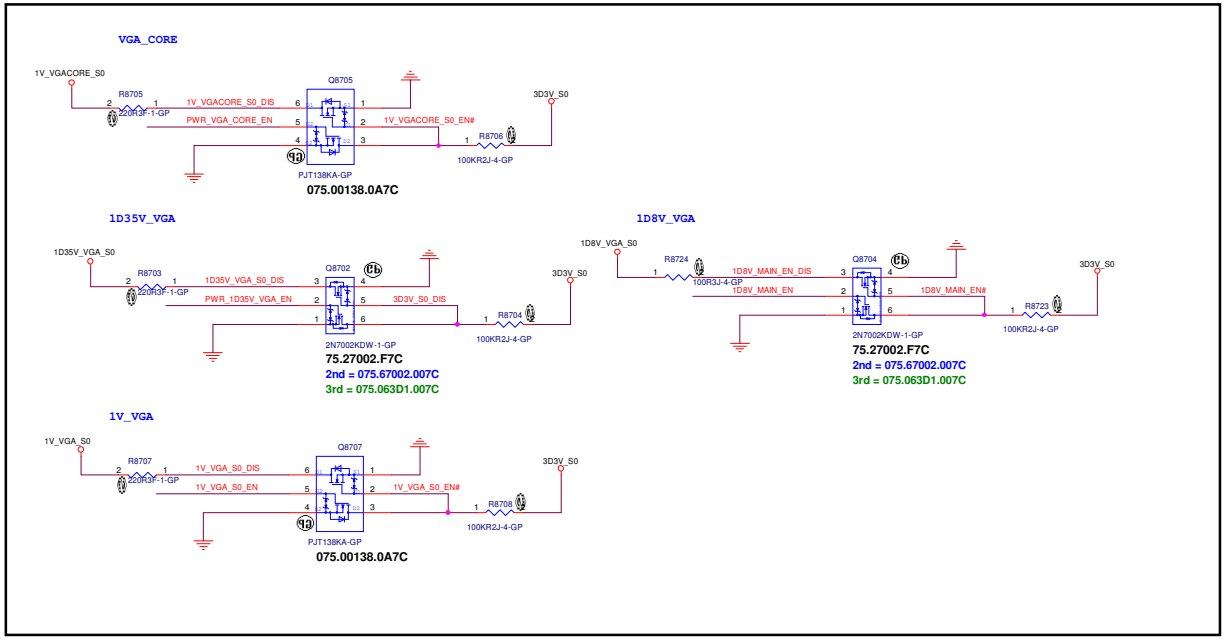


PGM-08866-001_V06

Table 13. Power Monitoring with OnSemi OVR-M

GPU	Component Values				
	R954, R924	R977, R923	R950	R953, R952	C841, C836
N18E-G3	649 Ω	169 Ω	243 kΩ	75 kΩ	1.0 nF
N18E-G2	649 Ω	191 Ω	243 kΩ	75 kΩ	1.0 nF
N18E-G0, N18E-G1 N18E-G3 MAX-Q N18E-G2 MAX-Q	649 Ω	287 Ω	243 kΩ	75 kΩ	1.0 nF
N18E-G1 MAX-Q N18E-G0 MAX-Q	649 Ω	475 Ω	243 kΩ	75 kΩ	1.0 nF

[85,87] PWR_VGA_CORE_EN
[85,87] PWR_1D35V_VGA_EN
[79] ADC_IN_P
[79] ADC_IN_N
[79] ADC_MUX_SEL
[85,87] [86] PWR_VGA_CORE_EN
[86] 1V_VGA_S0_EN
[85,86] 1D8V_MAIN_EN
[86,87] PWR_1D35V_VGA_EN



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Discharge

Size: A2 | Document Number: Selek CFL-H | Rev: A00

Date: Thursday, April 11, 2019 | Sheet 87 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title *(Reserved)*

Size	Document Number	Rev
A3	Selek CFL-H	A00

Date: Thursday, April 11, 2019 Sheet 88 of 105

https://vinafix.com/

HS1 STF236R128H101-3-GP — 34.4YG18.001
HS2 STF237R113H184-GP — 434.0H70B.0001
H15 HOLE233R154-GP — ZZ.SCREW.W91
H16 HOLE233R154-GP — ZZ.SCREW.W91
SPR1 SPRING-31-GP-U — 34.49U24.001 DY
SPR2 SPRING-43-GP-U — 34.15J03.001
SPR3 SPRING-43-GP-U — 34.15J03.001 DY
SPR4 SPRING-43-GP-U — 34.15J03.001 DY
H1 HOLE335R221-GP — ZZ.00PAD.YB1
H2 HOLE335R221-GP — ZZ.00PAD.YB1
H3 HOLE335R221-GP — ZZ.00PAD.YB1
H4 HOLE335R221-GP — ZZ.00PAD.YB1
H5 HOLE335R221-GP — ZZ.00PAD.YB1
H6 HOLE335R130-GP — ZZ.00PAD.XZ1
H9 HOLE233R154-GP — ZZ.SCREW.W91
H10 HOLE233R154-GP — ZZ.SCREW.W91
H11 HOLE233R154-GP — ZZ.SCREW.W91
H12 HOLE233R154-GP — ZZ.SCREW.W91
H13 HOLE233R154-GP — ZZ.SCREW.W91
H14 HOLE233R154-GP — ZZ.SCREW.W91

EMI Request

5V_S5
EC8938 SCD1U25V2KX-L-GP DY
EC8936 SCD1U25V2KX-L-GP
EC8937 SCD1U25V2KX-L-GP DY
EC8939 SCD1U25V2KX-L-GP
EC8940 SCD1U25V2KX-L-GP

5V_S0
EC8943 SCD1U25V2KX-L-GP
EC8941 SCD1U25V2KX-L-GP
EC8942 SCD1U25V2KX-L-GP DY
EC8944 SCD1U25V2KX-L-GP
EC8945 SCD1U25V2KX-L-GP DY

EMI Request

DCBATOUT
EC8901 EC8902 EC8903 EC8904 EC8905 EC8906 EC8907 EC8908 DY EC8909 EC8910 SCD1U25V2KX-L-GP
EC8917 EC8914 EC8912 EC8915 EC8916 EC8911 EC8913 SCD1U25V2KX-L-GP

EMI Request

1D2V_S3
EC8918 SCD1U25V2KX-L-GP
EC8919 SCD1U25V2KX-L-GP
EC8920 SCD1U25V2KX-L-GP
EC8921 SC100P50V2JN-L-GP
EC8922 SC1KP50V2KX-L-GP
EC8923 SC1KP50V2KX-L-GP DY
EC8924 SCD1U25V2KX-L-GP
EC8925 SCD1U25V2KX-L-GP

EMI Request

1D35V_VGA_S0
EC8932 SCD1U25V2KX-L-GP
EC8930 SC100P50V2JN-L-GP DY
EC8927 SCD1U25V2KX-L-GP
EC8931 SCD1U25V2KX-L-GP DY
EC8929 SC1KP50V2KX-L-GP
EC8933 SCD1U25V2KX-L-GP
EC8926 SCD1U25V2KX-L-GP
EC8928 SCD1U25V2KX-L-GP
EC8934 SC1KP50V2KX-L-GP
EC8935 SC100P50V2JN-L-GP DY

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors
Size: A3
Document Number: Selek CFL-H
Rev: A00
Date: Thursday, April 11, 2019
Sheet 89 of 105

<Core Design>

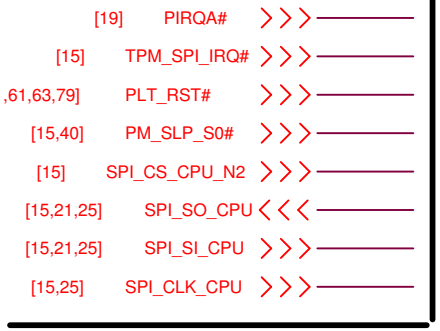
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Thursday, April 11, 2019 Sheet 90 of 105

SSID = TPM



reserve RTC Gen 9 reset circuit_20170814
leakage issue

3D3V_S5_PCH — R9148 TPM 10KR2J-3-GP
3D3V_TPM_VHIO — R9140 DY 10KR2J-3-GP

SPI_CS_CPU_N2 — R9130 TPM 0R2J-2-GP — SPI_CS2_TPM
SPI_SI_CPU — R9133 TPM 33R2J-2-GP — SPI_SI_TPM
SPI_SO_CPU — R9132 TPM 33R2J-2-GP — SPI_SO_TPM
SPI_CLK_CPU — R9138 TPM 33R2J-2-GP — SPI_CLK_TPM

3D3V_TPM_VHIO
If not used, it is ok to left it unconnected
R9149 DY 10KR2J-3-GP
SPI_IRQ#_TPM2 — R9139 DY 0R2J-2-GP — TPM_SPI_IRQ#

TP_TPM_GPIO1 — TP9103 TPAD14-OP-GP
TP_TPM_GPIO3 — TP9102 TPAD14-OP-GP
TPM_GPIO4 — TP9104 TPAD14-OP-GP
TP_TPM_PP — TP9101 TPAD14-OP-GP

3D3V_S0 — R9127 TPM 0R3J-0-U-GP
3D3V_S5 — R9126 DY 0R3J-0-U-GP
3D3V_TPM_VHIO
C9109 TPM SC10U6D3V3MX-DL-GP
C9112 TPM SCD1U16V2KX-3DLGP
C9113 TPM SCD1U16V2KX-3DLGP

3D3V_S5 — R9143 TPM 0R3J-0-U-GP — 3D3V_TPM_VSB
C9106 TPM SC10U6D3V3MX-DL-GP
C9108 TPM SCD1U16V2KX-3DLGP

reserve for modern standby

U9102

8	VHIO	SDA/GPIO0	29 — TPM_GPIO0 — R9141 DY 0R2J-2-GP — PM_SLP_S0#
22	VHIO	SCL/GPIO1	30 — TP_TPM_GPIO1
1	VSB	PIRQ#/GPIO2	18 — SPI_IRQ#_TPM2 — R9137 TPM 0R2J-2-GP — PIRQA#
		GPIO3	6 — TP_TPM_GPIO3
		GPIO4	13 — TPM_GPIO4
		PP/GPIO6	4 — TP_TPM_PP
21	SPI_SI_TPM	MOSI/GPIO7	
24	SPI_SO_TPM	MISO	
20	SPI_CS2_TPM	SCS#/GPIO5	
19	SPI_CLK_TPM	SCLK	
PLT_RST# — R9136 TPM 0R2J-2-GP — PLT_RST#_Q_TPM2	17	PLTRST#	
16	GND		
23	GND		
33	GND		
2	NC#2	NC#7	7
3	NC#3	NC#9	9
5	NC#5	NC#10	10
		NC#11	11
		NC#12	12
		NC#14	14
		NC#15	15
		NC#25	25
		NC#26	26
		NC#27	27
		NC#28	28
		NC#31	31
		NC#32	32

TPM
GP
NPCT750JAAYX-GP
071.00750.0003

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPM2.0**

Size	Document Number	Rev
A4	Selek CFL-H	A00

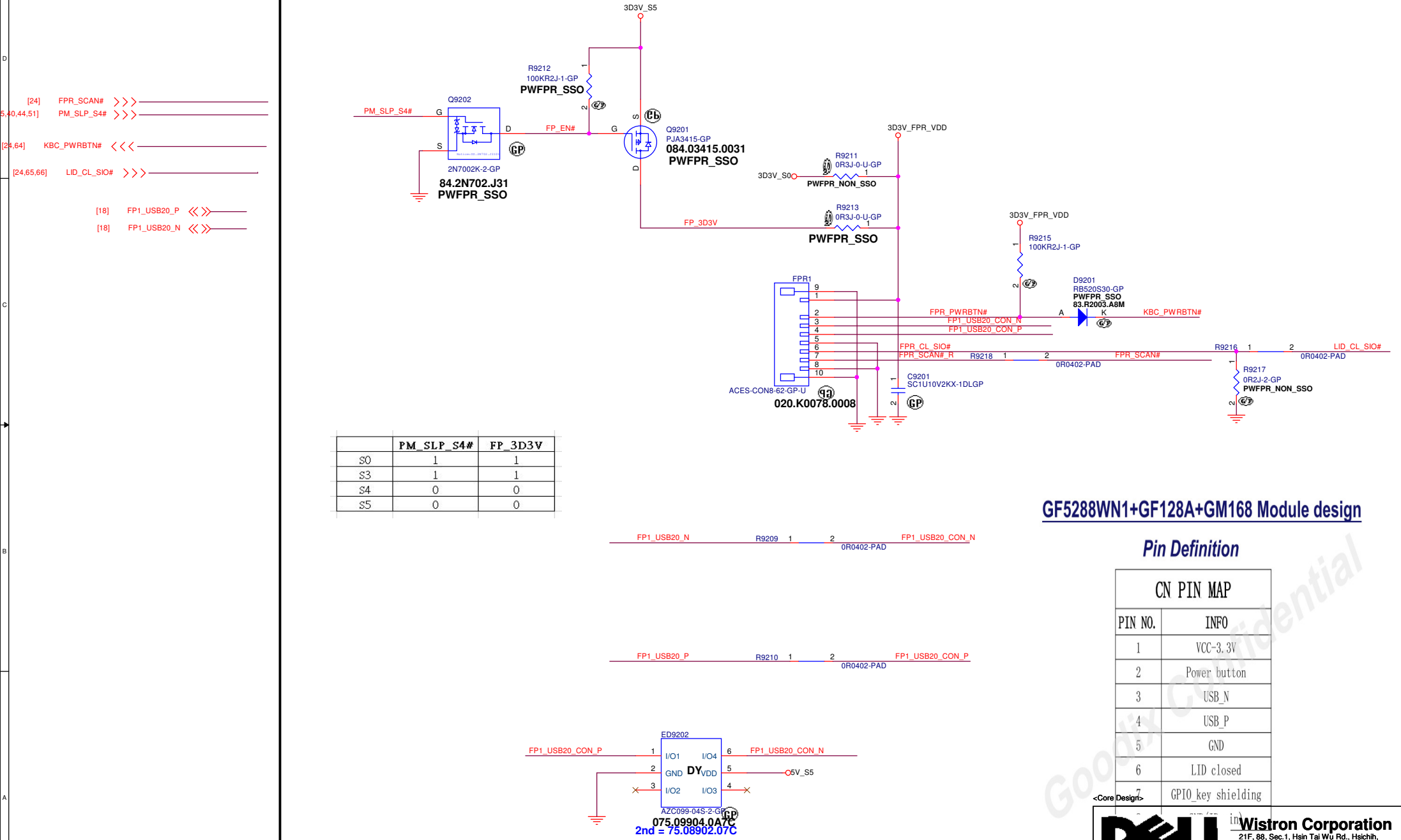
Date: Thursday, April 11, 2019 Sheet 91 of 106

Main Func = FPR

FBR(Botton side finger Print Sensor)

PWFPR_SSO: GOODIX module
PWFPR_NON_SSO: ELAN module(R9211 R9214 R9217)

https://vinafix.com/



	PM_SLP_S4#	FP_3D3V
S0	1	1
S3	1	1
S4	0	0
S5	0	0

GF5288WN1+GF128A+GM168 Module design

Pin Definition

CN PIN MAP	
PIN NO.	INFO
1	VCC-3.3V
2	Power button
3	USB_N
4	USB_P
5	GND
6	LID closed
7	GPIO_key shielding

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)Finger Print

Size: A3 | Document Number: Selek CFL-H | Rev: A00

Date: Thursday, April 11, 2019 | Sheet 92 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Thursday, April 11, 2019 Sheet 93 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A4	**Selek CFL-H**	**A00**

Date: Thursday, April 11, 2019 Sheet 94 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***(Reserved)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Thursday, April 11, 2019 Sheet 95 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***(Reserved)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Thursday, April 11, 2019 Sheet 96 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Thursday, April 11, 2019 Sheet 97 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***(Reserved)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Thursday, April 11, 2019 Sheet 98 of 105

Main Func = XDP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*CPU_XDP;PCH_XDP*	
Size A3	Document Number **Selek CFL-H**	Rev **A00**
Date: Thursday, April 11, 2019	Sheet 99 of 105	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***Table of Content***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Thursday, April 11, 2019 Sheet 100 of 105

<Core Design>

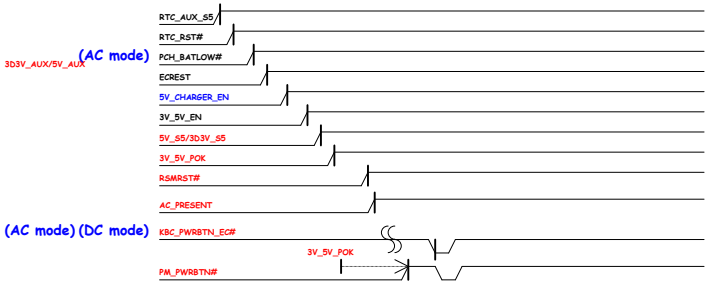
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

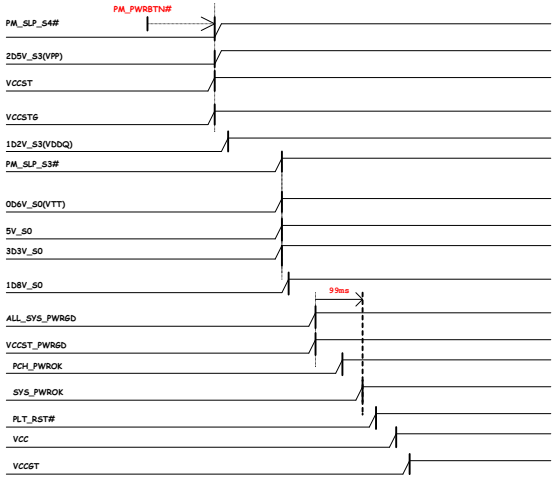
Title ***Change History***

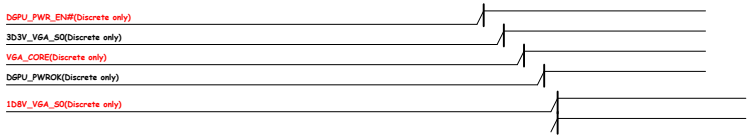
Size	Document Number	Rev
A	Selek CFL-H	A00

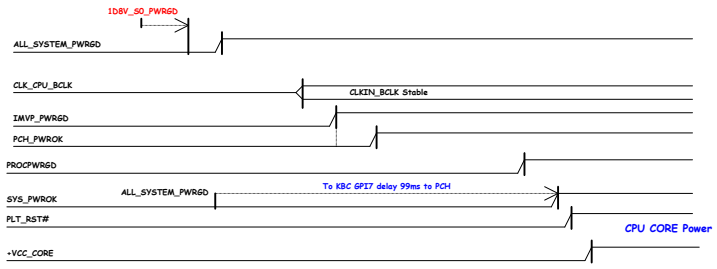
Date: Thursday, April 11, 2019 Sheet 101 of 105

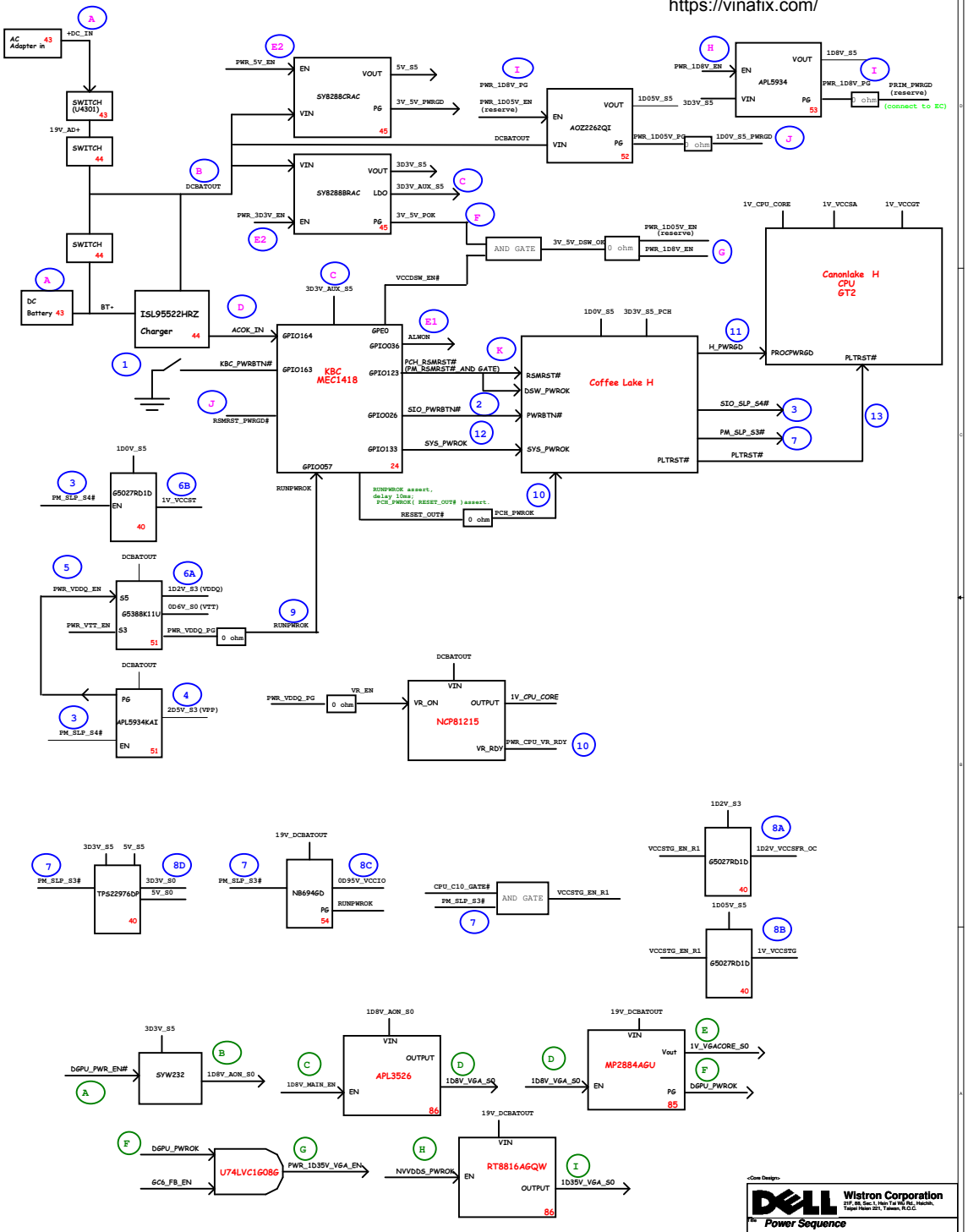
Intel-Power Up Sequence







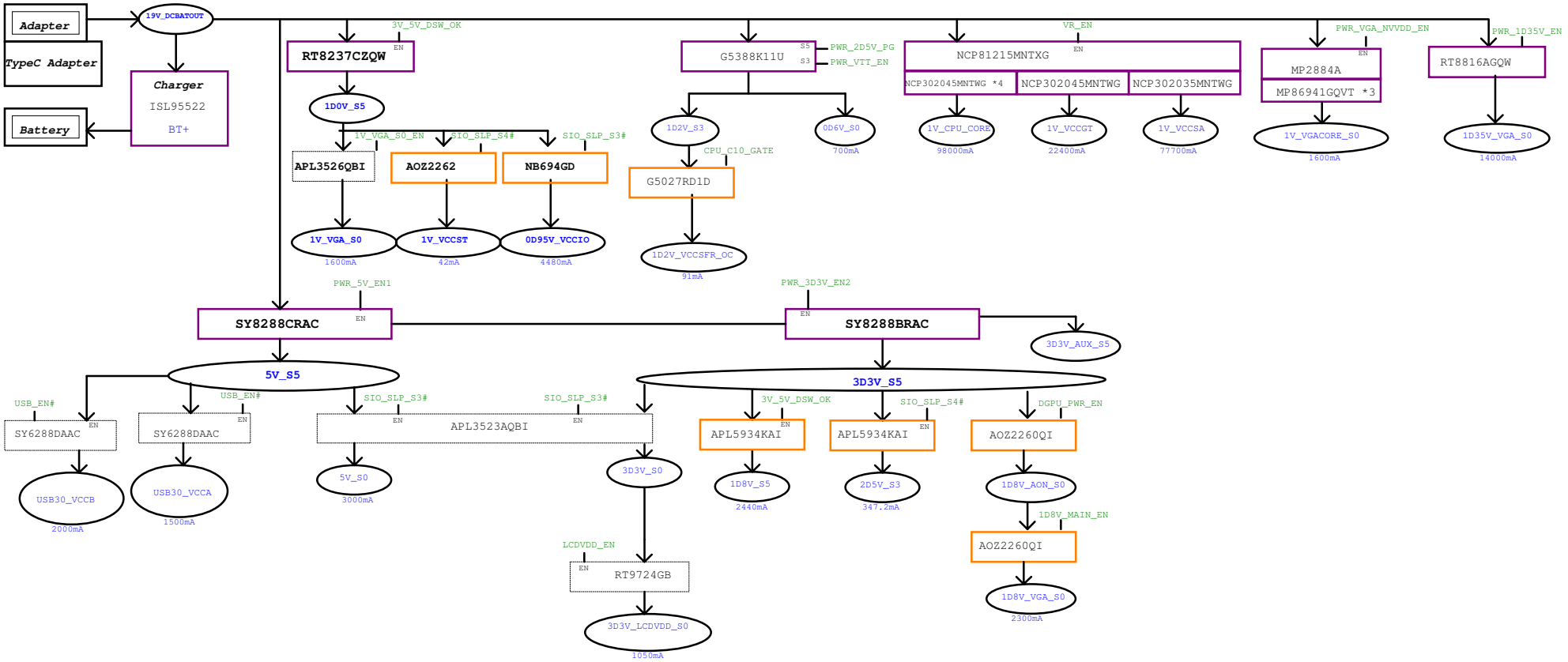




Title: Power Sequence

Size	Document Number	Rev
A3	Selek CFL-H	A00

Date: Thursday, April 11, 2019 Sheet 109 of 109



Power Shape

Regulator	LDO	Switch

<Core Design>

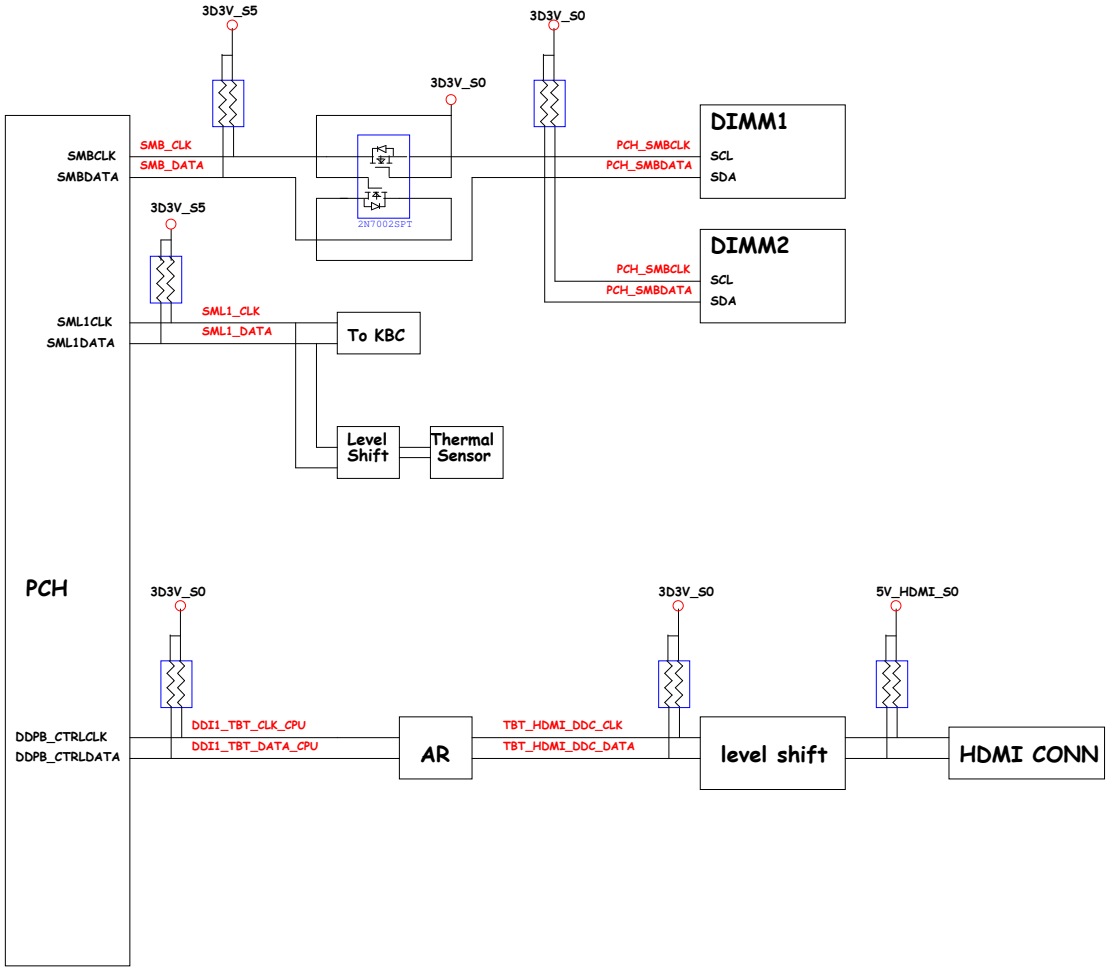
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

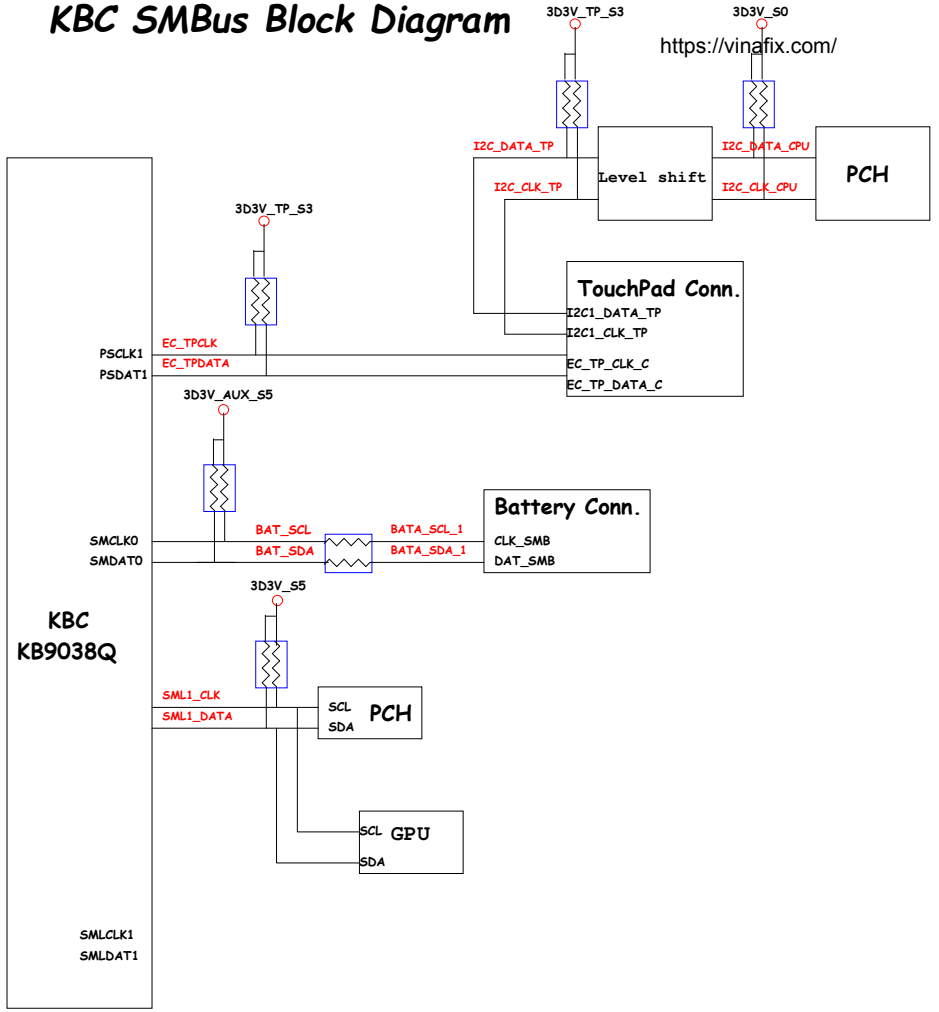
Size	Document Number	Rev
A2	Selek CFL-H	A00

Date: Thursday, April 11, 2019 Sheet 103 of 105

PCH SMBus Block Diagram



KBC SMBus Block Diagram



<Core Design>

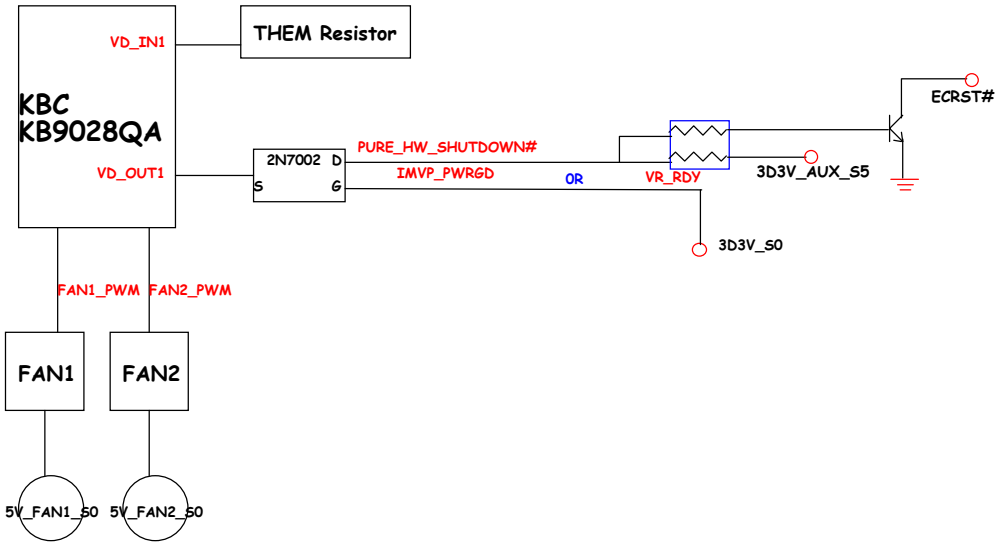
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS BLOCK DIAGRAM

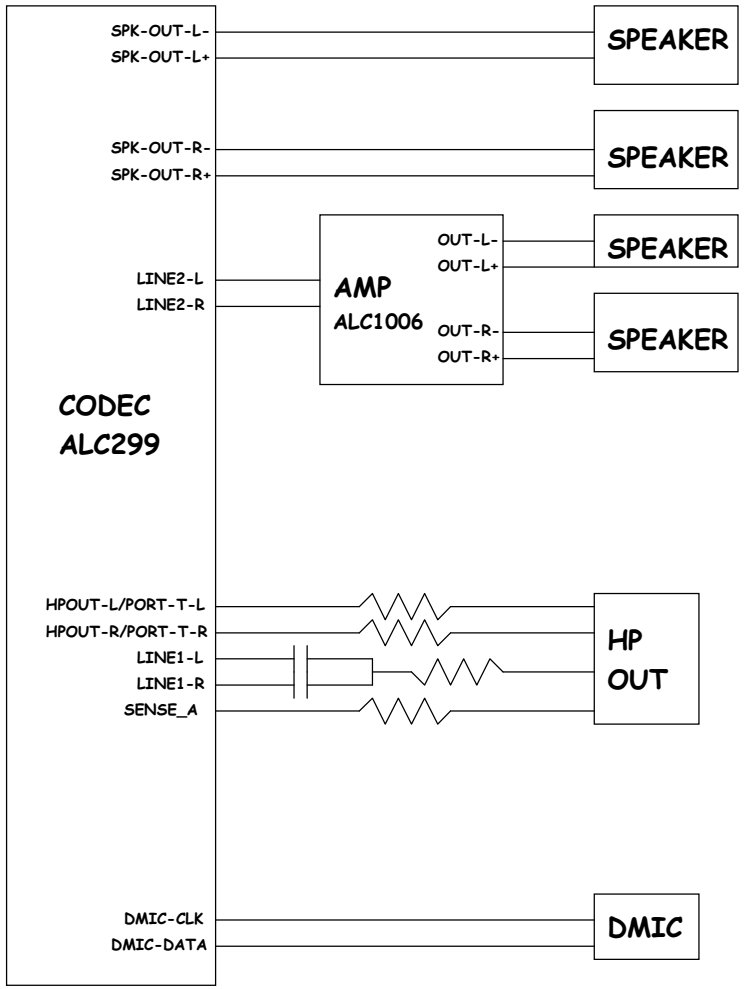
Size	Document Number	Rev
Custom	Selek CFL-H	A00

Date: Thursday, April 11, 2019 Sheet 104 of 105

Thermal Block Diagram



Audio Block Diagram



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal /AUDIO Block Diagram		
Size: Custom	Document Number: Selek CFL-H	Rev: A00
Date: Thursday, April 11, 2019	Sheet 105 of 105	