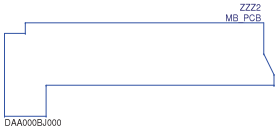
MODEL NAME : Celtic

PCB NO : LA-D312P

BOM P/N :



	R1	R3	R3	R3	R3
CPN	DAA000BJ000	DAA000BJ000	DAA000BJ000	DAA000BJ000	DAA000BJ000

Dell/Compal Confidential

Schematic Document

Celtic (Skylake Y)

2015-12-10

Rev: 1.0

AR Option

UV3 AR@

SA00008E75L

AR-B1_BGA337

CPU Option

UC1 SR2EG@ SA000092X3L
HE806620192287 6 SR2EG
S IC HE806620192287 6 SR2EG D1 1.1G A31!

UC1 SR2EH@ SA000092V3L
HE8066201922875 SR2EH
S IC HE8066201922875 SR2EH D1 1.2G A31!

UC1 SR2EM@ SA000092Z3L
HE8066201930524 SR2EM
S IC HE8066201930524 SR2EM D1 1.1G A31!

UC1 SR2EN@ SA000092Y3L
HE8066201930521 SR2EN
S IC HE8066201930521 SR2EN D1 0.9G A31!

Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

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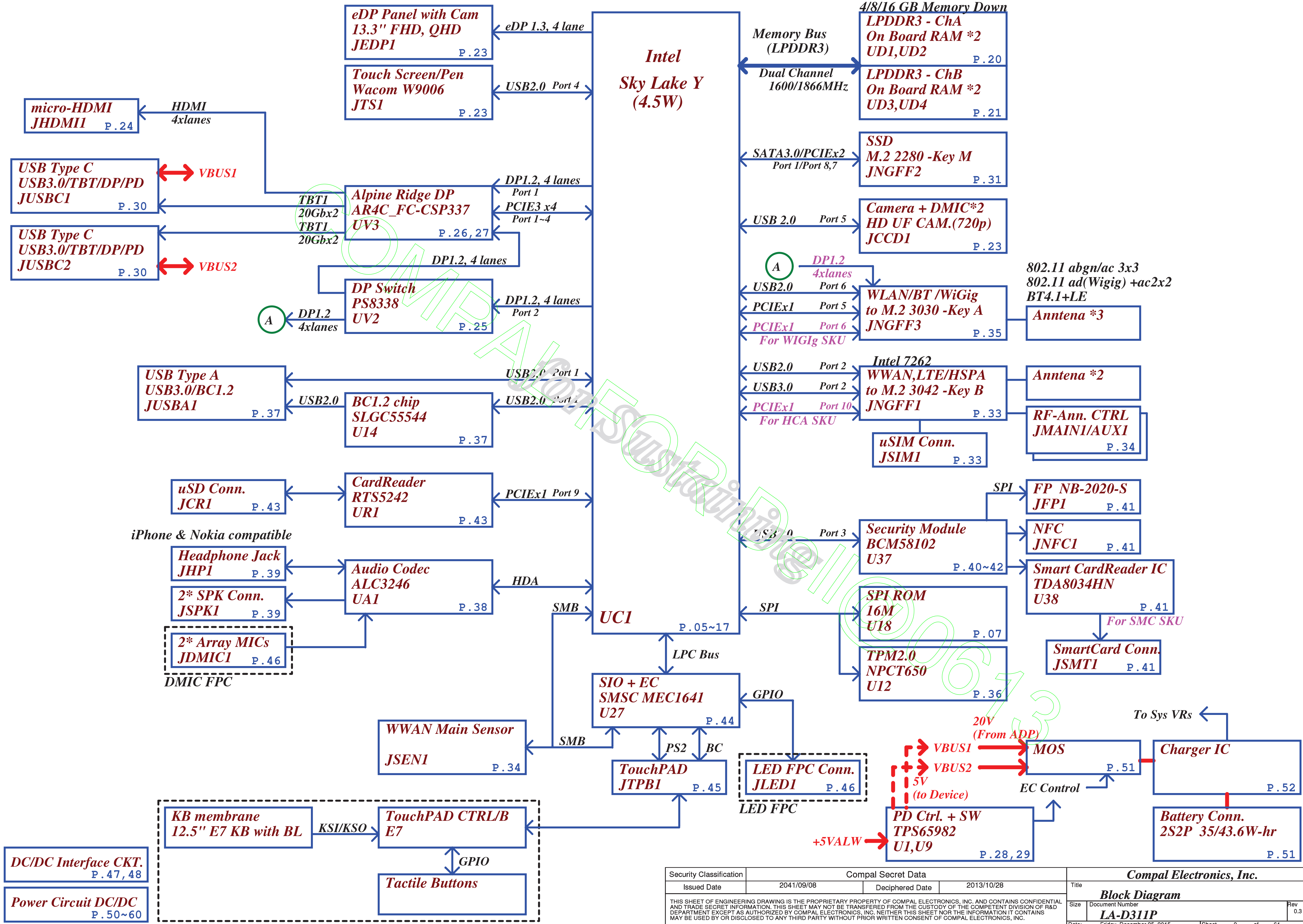
Title: *Cover Page*

Size	Document Number	Rev
	LA-D311P	0.3

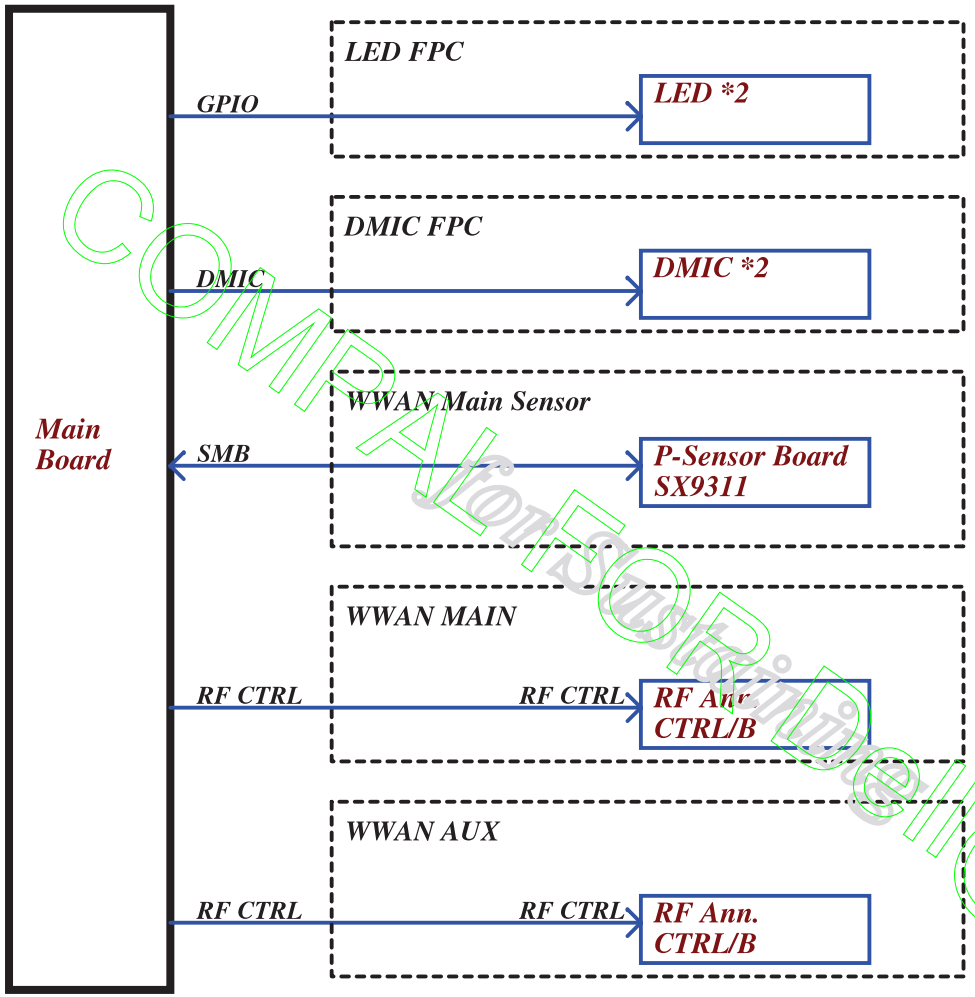
Date: Friday, December 25, 2015 Sheet 1 of 61



Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title	Block Diagram		
Size	Document Number: LA-D311P		Rev 0.3
Date: Friday, December 25, 2015	Sheet 2 of 61		



Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **DaughterB block diagram**

Size	Document Number	Rev
	LA-D311P	0.3

Date: Friday, December 25, 2015 Sheet 3 of 61

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ Power plane	+3VALW_DSW +5VALW +3VALW +1.8VALW +3VLP	+3V_PRIM +1.8V_PRIM +1.0V_PRIM +1.0VA_GATE +0.95V_PRIM	+1.2V_DDR +3.3V_CV2 +1.8V_MEM +1.0V_VCCST	+5VS +3VS +1.8VS +1.0V_VCCSTG +0.85VS_VCCIO +0.6VS_VTT +VCC_SA +VCC_GT +VCC_CORE
S0	ON	ON	ON	ON
S3 /AC	ON	ON	ON	OFF
DS3	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF

SMBUS Control Table

	SOURCE	BATT	Charger	XDP	USH	PD Controller -1	PD Controller -2	GPIO Expander	P-sensor
PCH_SML0CLK PCH_SML0DATA	PCH								
PCH_SML1CLK PCH_SML1DATA	PCH								
MEM_SMBCLK MEM_SMBDATA	PCH			V					
EC_SMB00_CLK EC_SMB00_DAT	MEC1641								
EC_SMB01_CLK EC_SMB01_DAT	MEC1641				V				V
EC_SMB03_CLK EC_SMB03_DAT	MEC1641	V							
EC_SMB04_CLK EC_SMB04_DAT	MEC1641		V						
EC_SMB05_CLK EC_SMB05_DAT	MEC1641					V			
EC_SMB07_CLK EC_SMB07_DAT	MEC1641						V		

Link

Board ID Table

Vcc	3.3V +/- 5%			
Board ID	R	C	PCB Revision	REV
0	240K +/- 5%	4700p	0.1	EVT1.0
1	130K +/- 5%	4700p	0.2	DVT1.0/DVT1.1
2	62K +/- 5%	4700p	0.3	DVT2.0/PreMP
3	33K +/- 5%	4700p		
4	8.2K +/- 5%	4700p		
5	4.3K +/- 5%	4700p		
6	2K +/- 5%	4700p		
7	NC			

SOC DDI Port Mapping	DDI PORT#	DESTINATION
	B	Alpine Ridge
	C	DP MUX

SOC PCIE Port Mapping	PCI EXPRESS	DESTINATION
	Lane 1	Alpine Ridge
	Lane 2	
	Lane 3	
	Lane 4	
	Lane 5	NGFF (WLAN)
	Lane 6	NGFF (WiGig)
	Lane 7	NGFF (SSD)
	Lane 8/ SATA 1	
	Lane 9	Cardreader
	Lane 10	~~HCA~~

Lane reversal

CLK	DIFFERENTIAL	DESTINATION
	CLKOUT_PCIE1	TBT
	CLKOUT_PCIE2	NGFF (WiGig) or (HCA)
	CLKOUT_PCIE3	Cardreader
	CLKOUT_PCIE4	NGFF (SSD)
	CLKOUT_PCIE5	NGFF (WLAN)

USB 3.0 PORT#	DESTINATION
1	Type A(Debug)
2	WWAN
3	
4	

USB 2.0 PORT#	DESTINATION
1	Type A(Debug)
5	WWAN
7	USH
3	Touch
9	CAM
2	BT

FLEX CLOCKS	DESTINATION
CLKOUT_LPC_0	EC LPC
CLKOUT_LPC_1	Debug

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	sm	0.50000
1	Top		Copper foil	0.33oz+plating	1.20000
			Prepreg	1086	2.65000
2	IN1(GND)		Copper foil	0.33oz+plating	1.10000
			Prepreg	106	1.80000
3	GND/PWR		Copper foil	0.33oz+plating	1.10000
			Prepreg	1080	2.56000
4	IN2		Copper foil	0.5oz	0.60000
			Core	3mil	3.00000
5	GND/PWR		Copper foil	0.5oz	0.60000
			Prepreg	106	1.63000
6	GND/PWR		Copper foil	0.5oz	0.60000
			Core	3mil	3.00000
7	IN3		Copper foil	0.5oz	0.60000
			Prepreg	1080	2.56000
8	GND/PWR		Copper foil	0.33oz+plating	1.10000
			Prepreg	106	1.80000
9	IN4(GND)		Copper foil	0.33oz+plating	1.10000
			Prepreg	1086	2.65000
10	Bottom		Copper foil	0.33oz+plating	1.20000
			SolderMask	sm	0.50000
Overall Thickness (0.8mm ± 10%)					31.85000
					0.80899

Symbol Note :

@ : means de-pop

: means Digital Ground

: means Analog Ground

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Compal Electronics, Inc.

Title: Notes List

Size: | Document Number: LA-D311P | Rev: 0.3

Date: Friday, December 25, 2015 | Sheet 4 of 61

Functional Strap Definitions

GPP_E19 (Internal Pull Down): DDPB_CTRLDATA

0 = Port B is not detected.

1 = Port B is detected.

GPP_E21 (Internal Pull Down): DDPC_CTRLDATA

0 = Port C is not detected.

1 = Port C is detected.

GPP_E23 (Internal Pull Down): DDPD_CTRLDATA

0 = Port D is not detected.

1 = Port D is detected.

PDG_Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

TBT1

DP MUX

SOC_DP1_CTRL_DATA(Internal Pull Down):
Display Port B Detected
0 = Port B is not detected.
1 = Port B is detected.
SOC_DP2_CTRL_DATA(Internal Pull Down):
Display Port C Detected
0 = Port C is not detected.
1 = Port C is detected.

RC4 Width 20 mils, Spacing 25 mils, Length < 100 mil

PS8338B internal pull doewn

PU/PD for CPU JTAG signals

PU/PD for PCH JTAG signals

Connect to XDP Conn. (Option w/ CPU JTAG)

<To CPU JTAG>

<To PCH JTAG>

Closed to CPU

<XDP Misc.>

<XDP_SMBUS> Link to PCH SMB

XDP CONN

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Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **SKL Y(1/13) DDI,MSIC,XDP**

Size	Document Number	Rev
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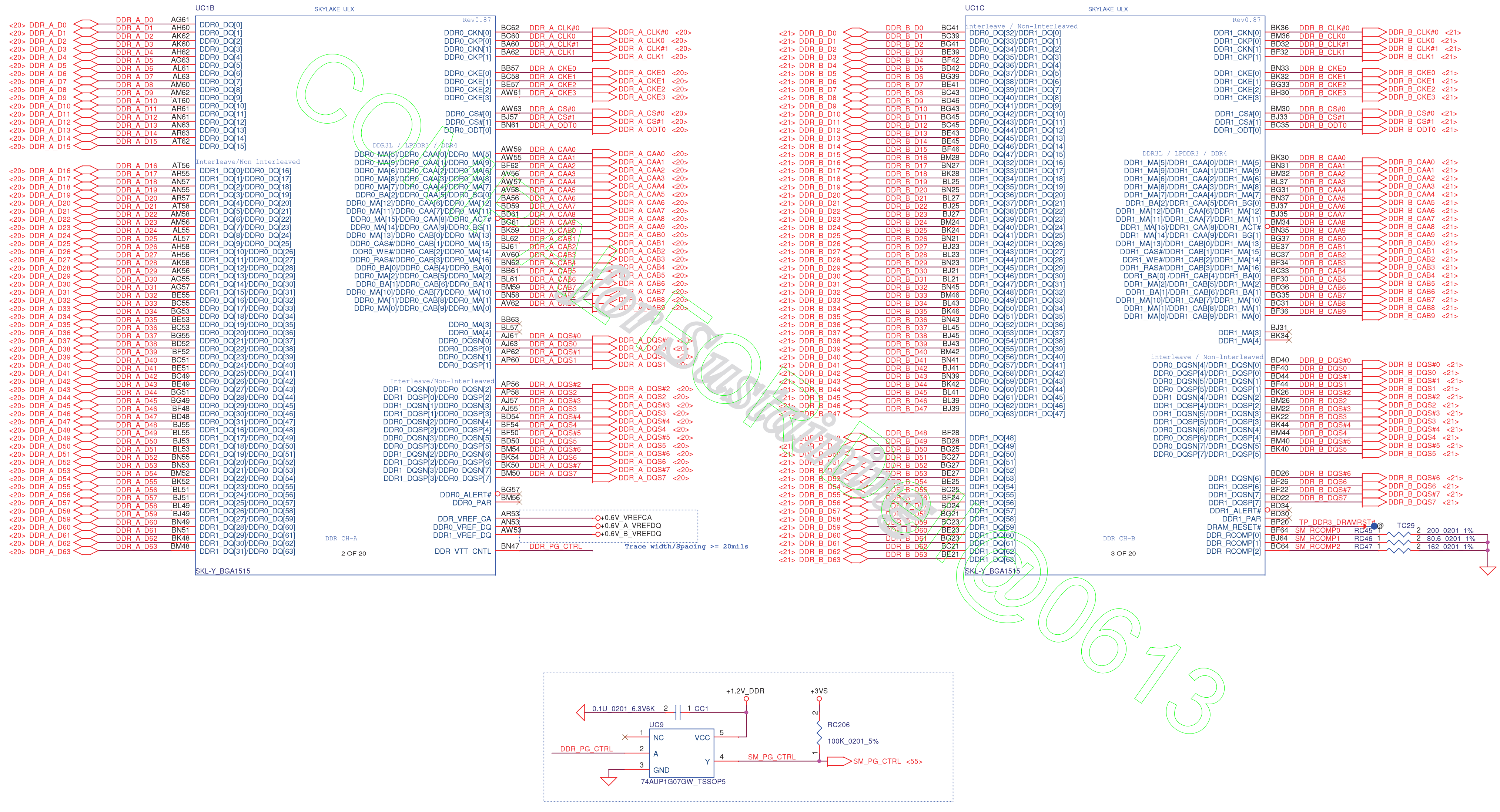
Non-Interleave Memory



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Issued Date	2041/09/08	Deciphered Date	2013/10/28

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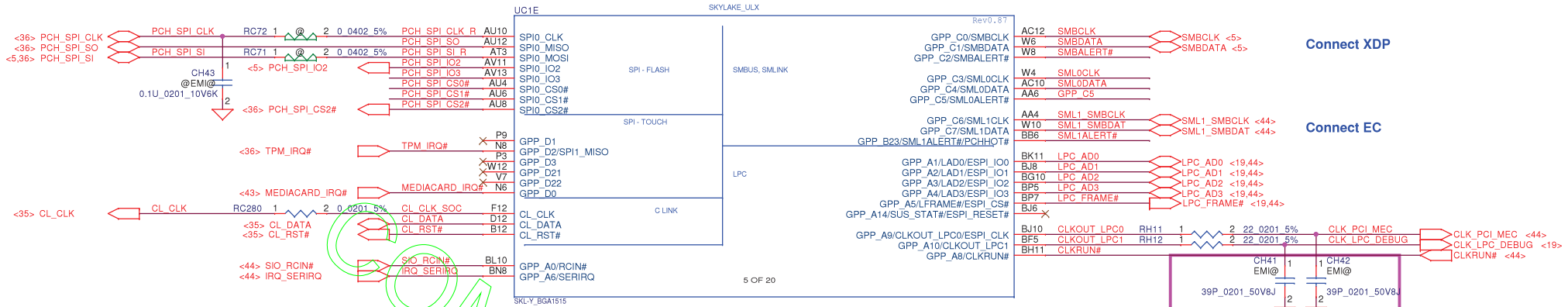
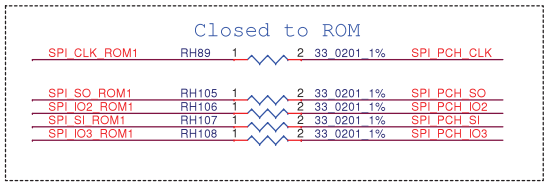
Compal Electronics, Inc.

Title: *SKL Y(2/13) DDRIII*

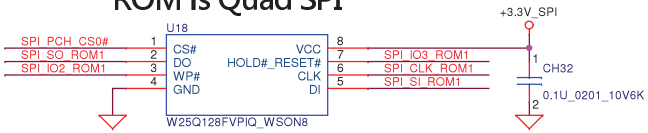
Size — Document Number: *LA-D311P* — Rev 0.3

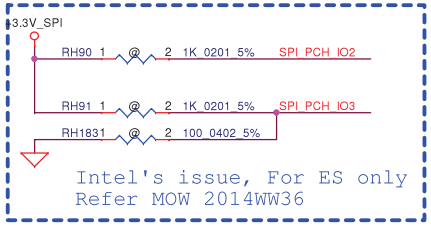
Date: Friday, December 25, 2015 — Sheet 6 of 61

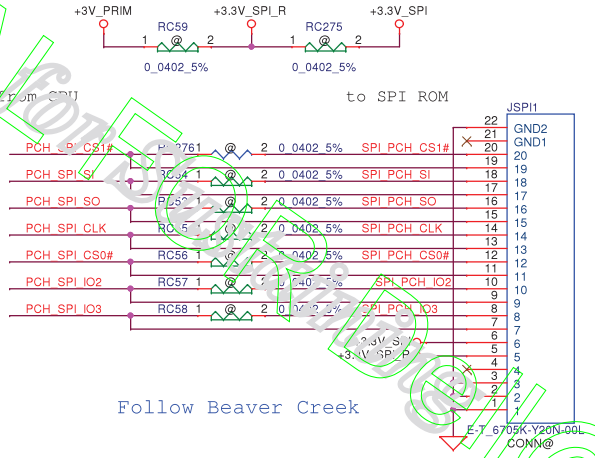


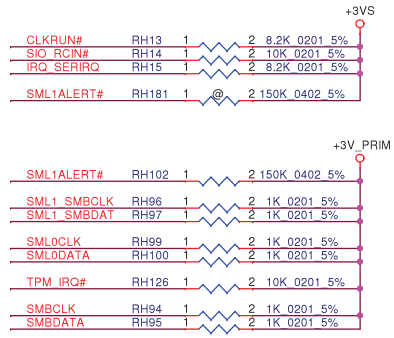


SPI ROM FOR ME (16MByte)
ROM is Quad SPI









Functional Strap Definitions

GPP_C2 (Internal Pull Down): SMBALERT#

0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).

1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

GPP_C5 (Internal Pull Down): SML0ALERT#

0 = LPC Is selected for EC.

1 = eSPI Is selected for EC.

Reserve SO8 footprint for BIOS debug conn (SA00005VV00_W25Q128FVSIG_SO8)

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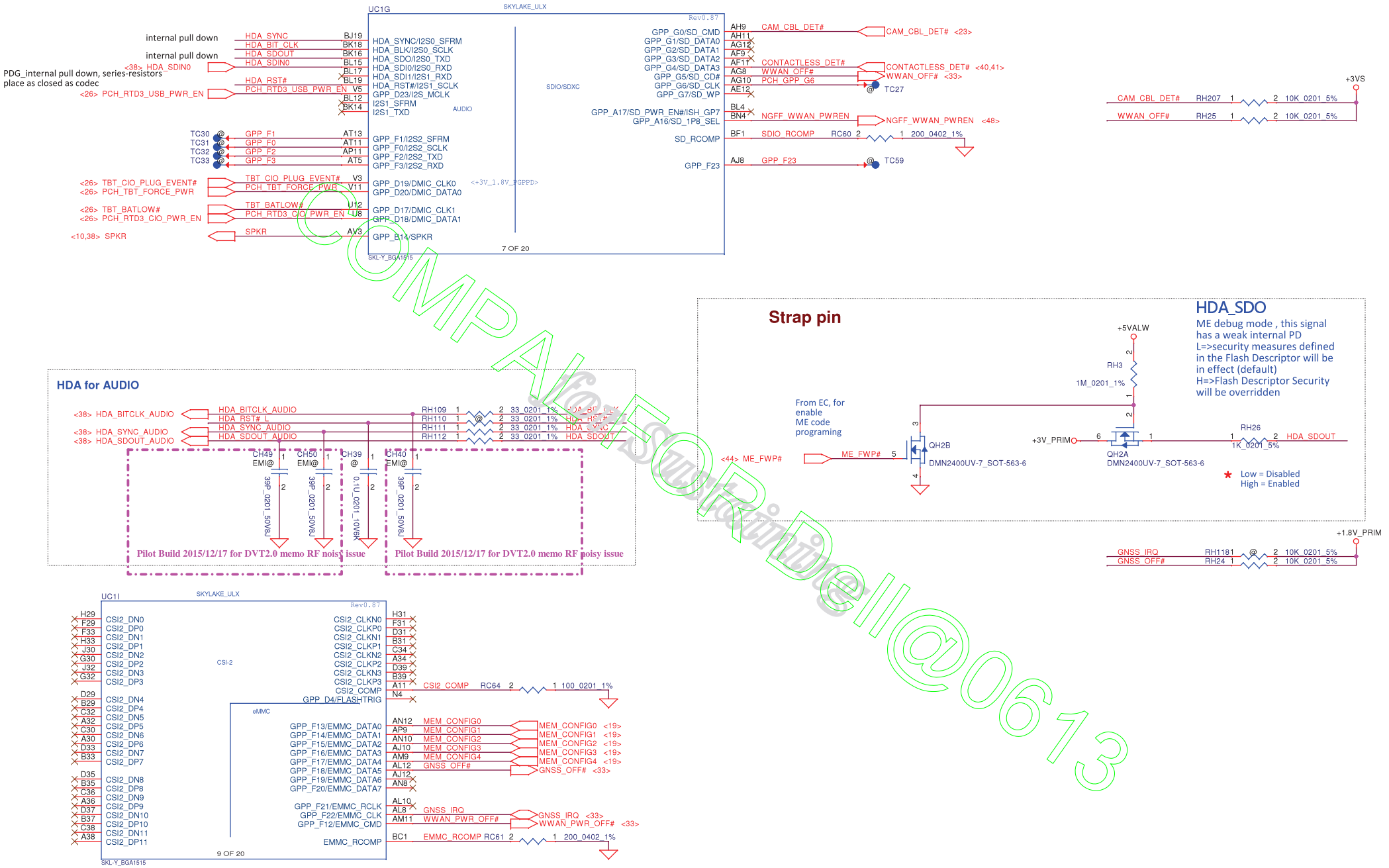
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: SKL Y(3/13) SPI,SMB			
Size	Document Number: LA-D311P		Rev: 0.3
Date: Friday, December 25, 2015	Sheet 7 of 61		



Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.	
Title	SKL Y(4/13) HDA,EMMC,SDIO
Size	Document Number: LA-D311P
Rev	0.3
Date:	Friday, December 25, 2015
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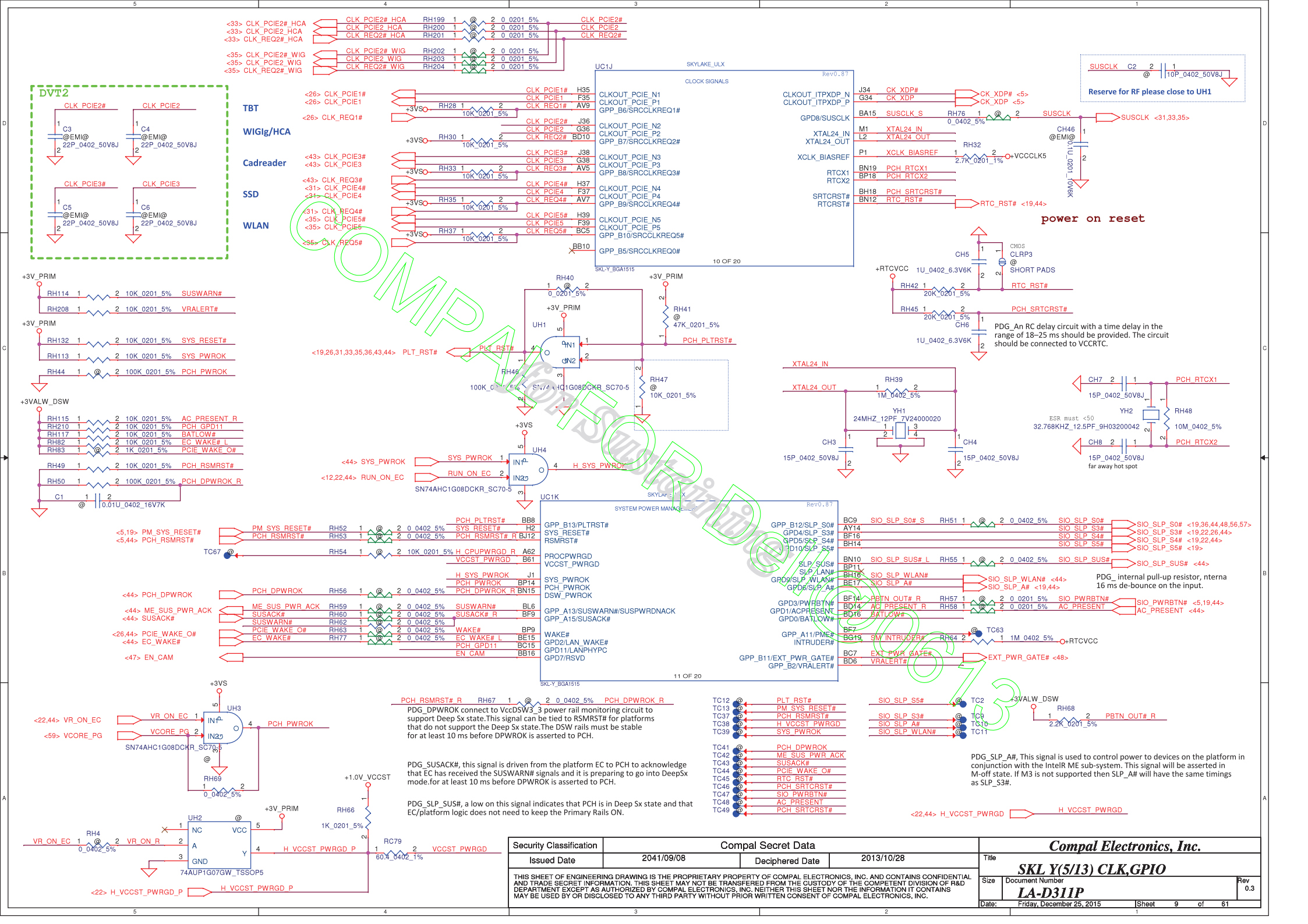
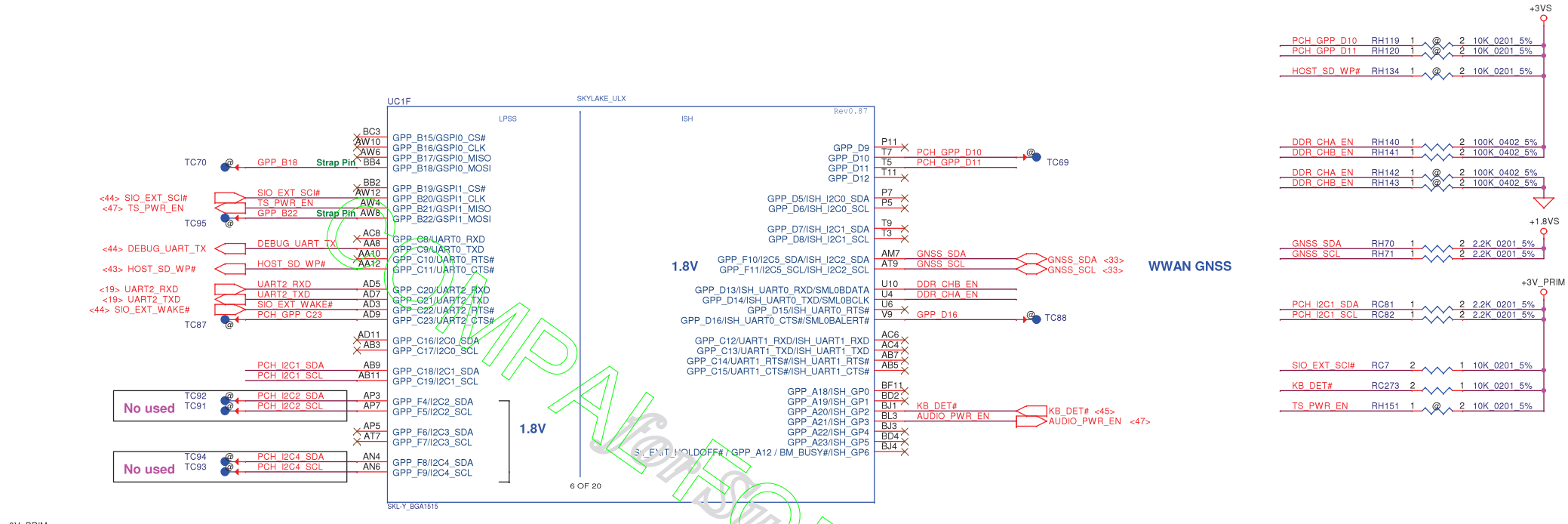
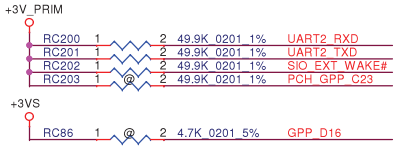




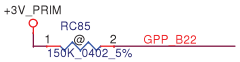


Functional Strap Definitions

GPP_B14 (Internal Pull Down): SPKR
TOP Swap Override
0 = Disable TOP Swap mode.----> AAU30 Use
1 = Enable TOP Swap Mode.

GPP_B18 (Internal Pull Down): GSSPIO_MOSI
No Reboot
0 = Disable No Reboot mode. --> AAU30 Use
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GPP_B22 (Internal Pull Down): GSSPI1_MOSI
Boot BIOS Strap Bit
0 = SPI Mode --> AAU30 Use
1 = LPC Mode



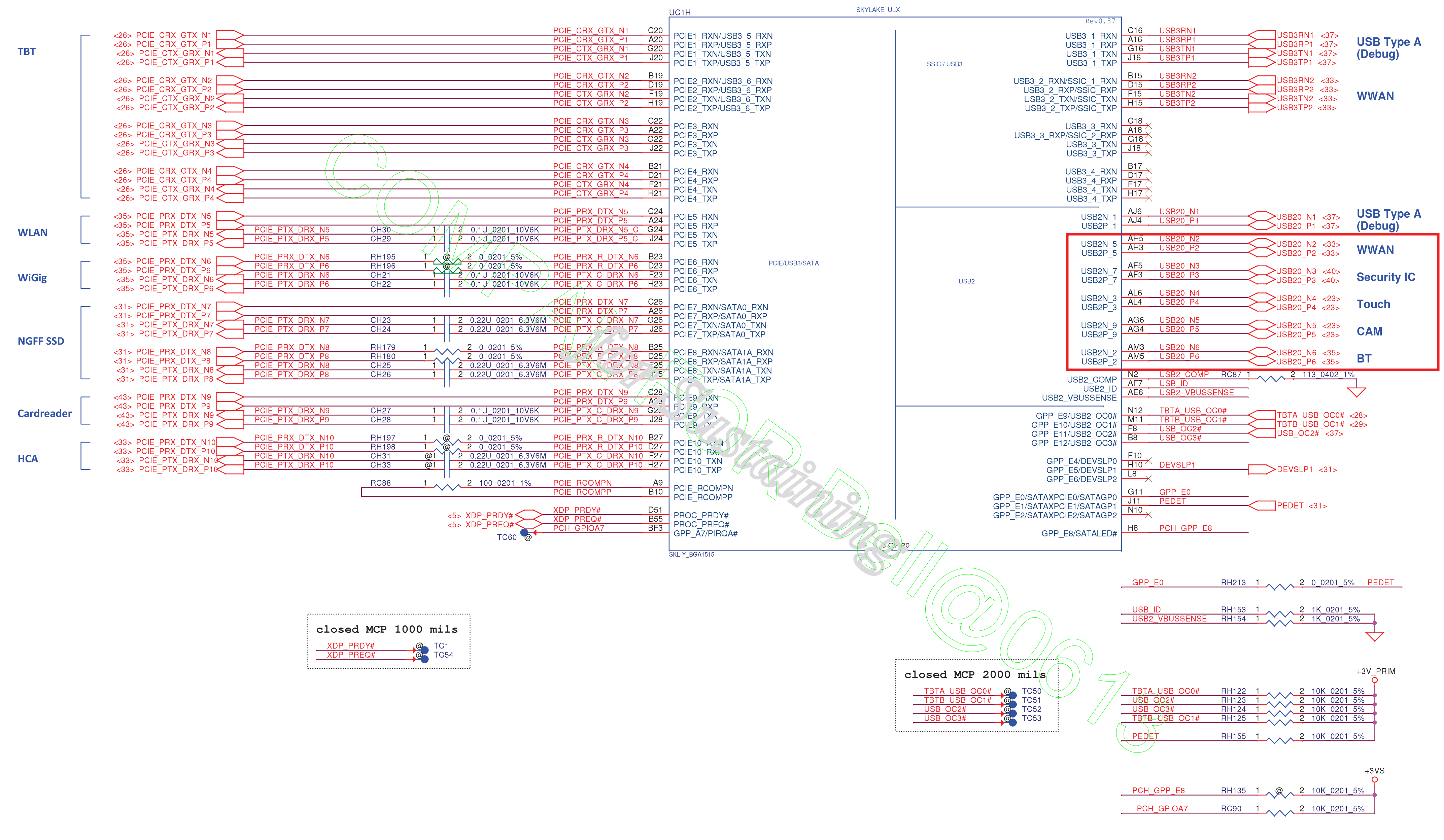
Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **SKL Y(6/13) GPIO,LPIO,I2C**

Size | Document Number: **LA-D311P** | Rev: 0.3

Date: Friday, December 25, 2015 | Sheet 10 of 61



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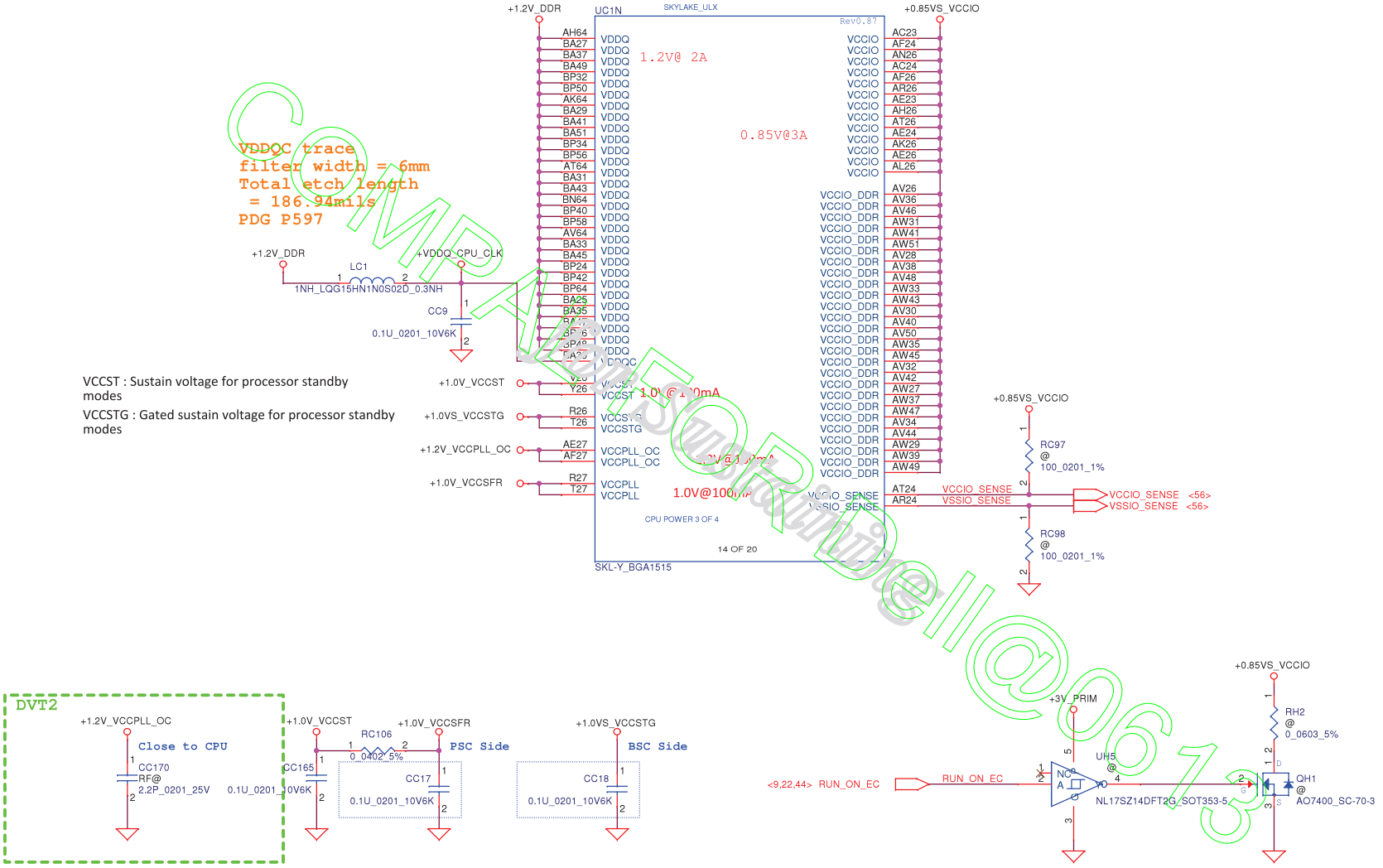
				Date: Friday, December 25, 2015 / Sheet 11 of 61



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Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **SKL Y(8/13) Power**

Size	Document Number	Rev
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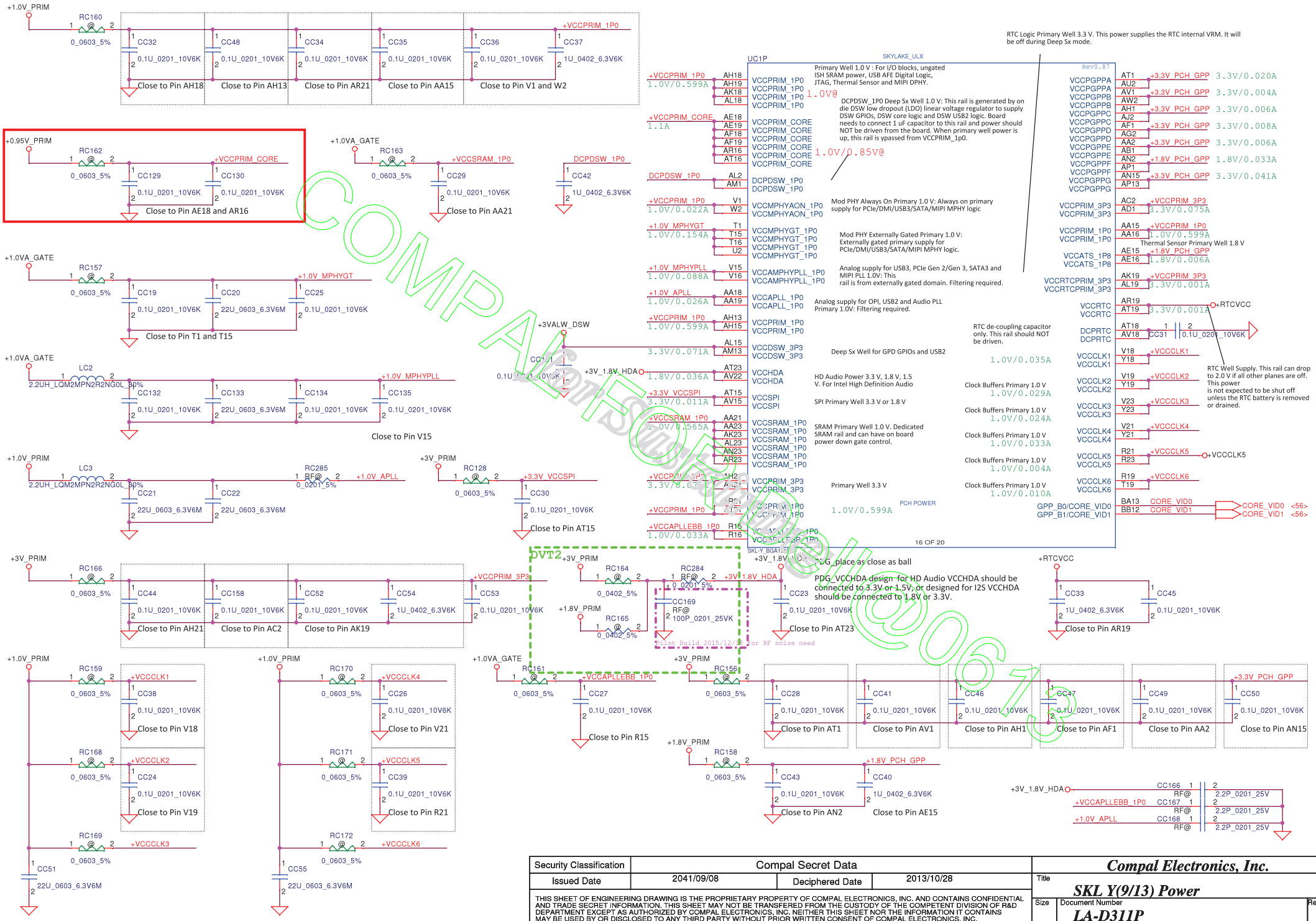
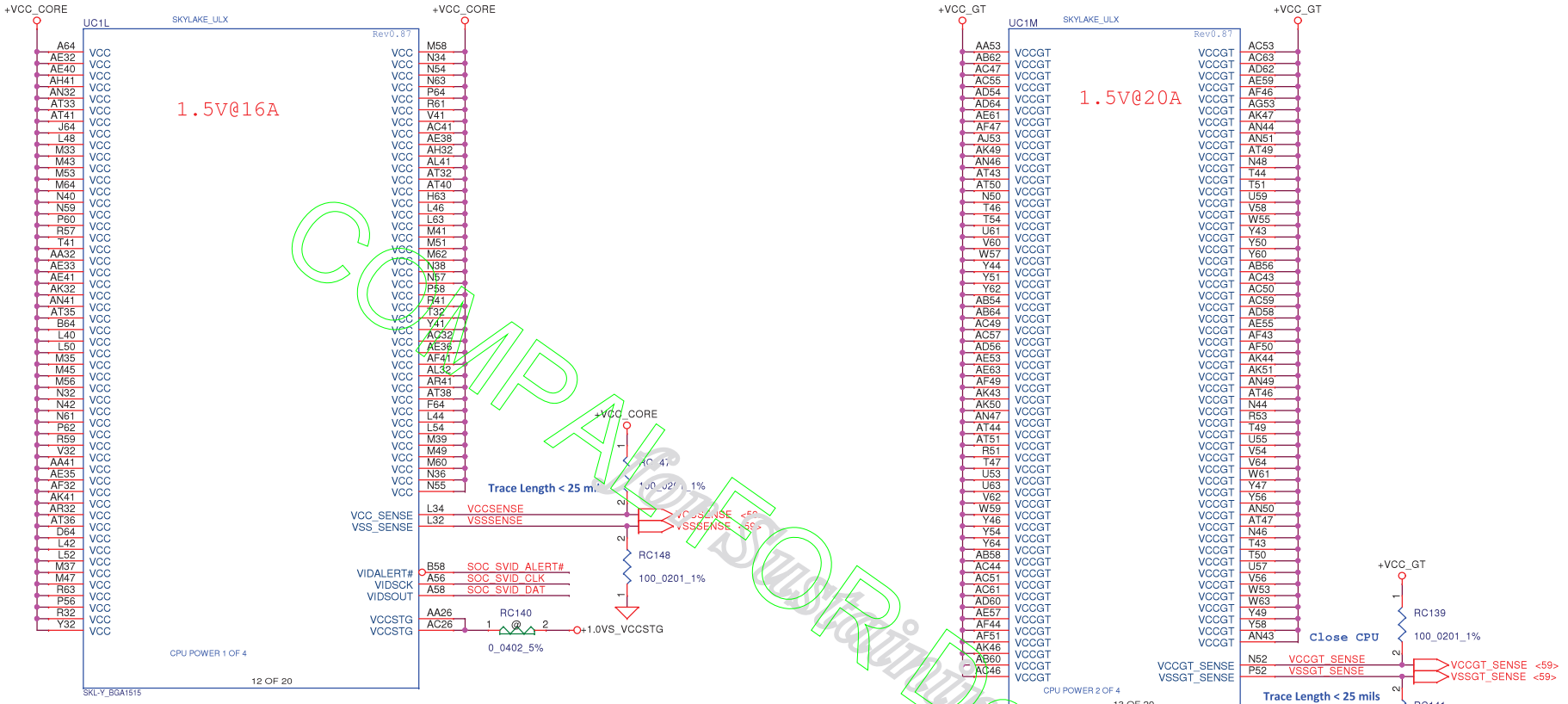
Date: Friday, December 25, 2015 | Sheet 12 of 61

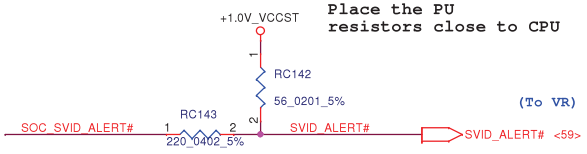


Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: SKL Y(9/13) Power			
Size	Document Number: LA-D311P		Rev: 0.3
Date: Friday, December 25, 2015	Sheet 13 of 61		



SVID ALERT



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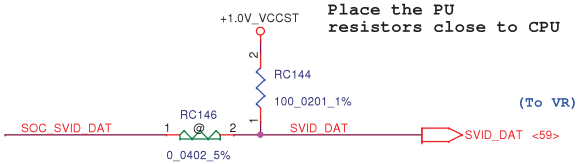
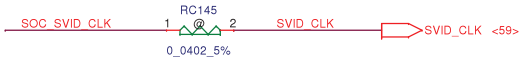


SVID CLK



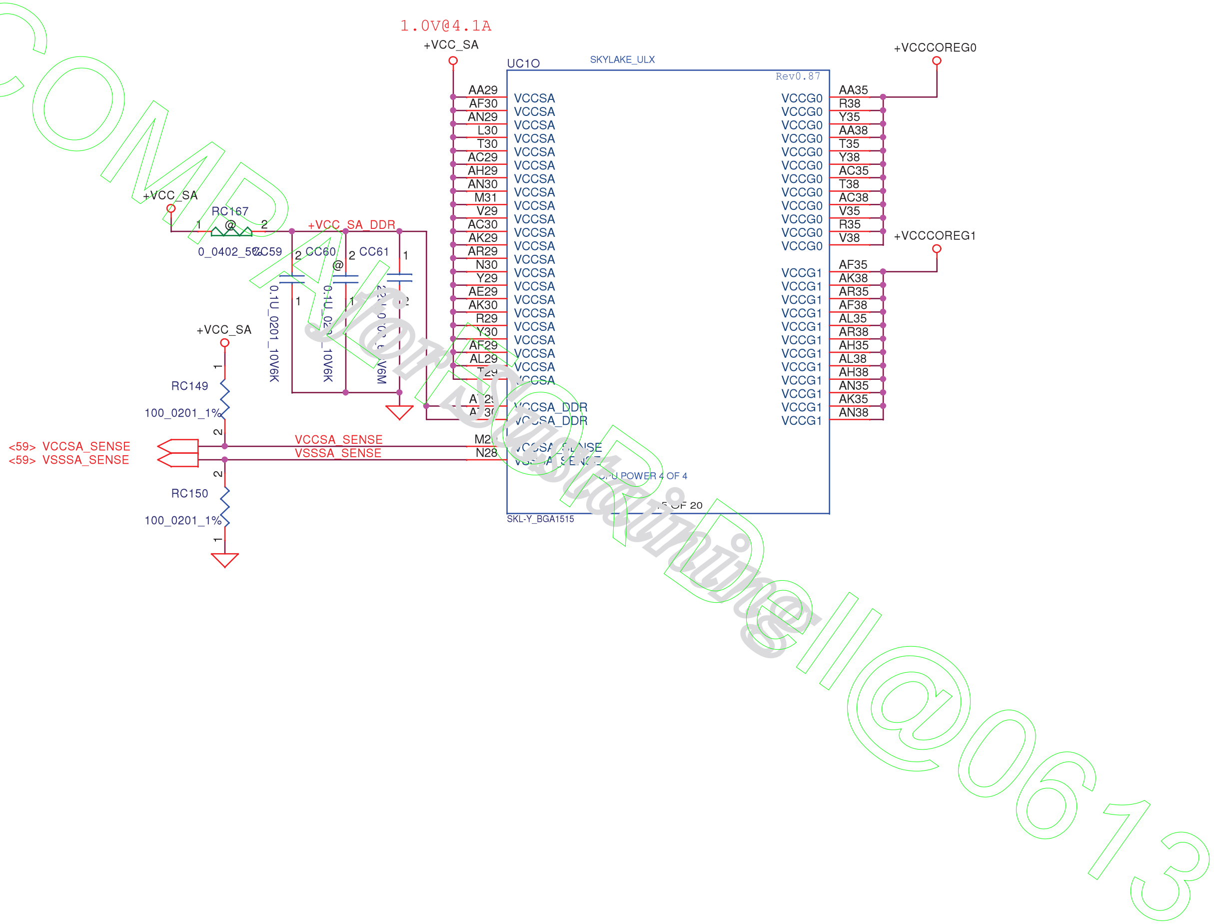
Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **SKL Y(10/13) Power**

Size	Document Number	Rev
	LA-D311P	0.3

Date: Friday, December 25, 2015 | Sheet 14 of 61



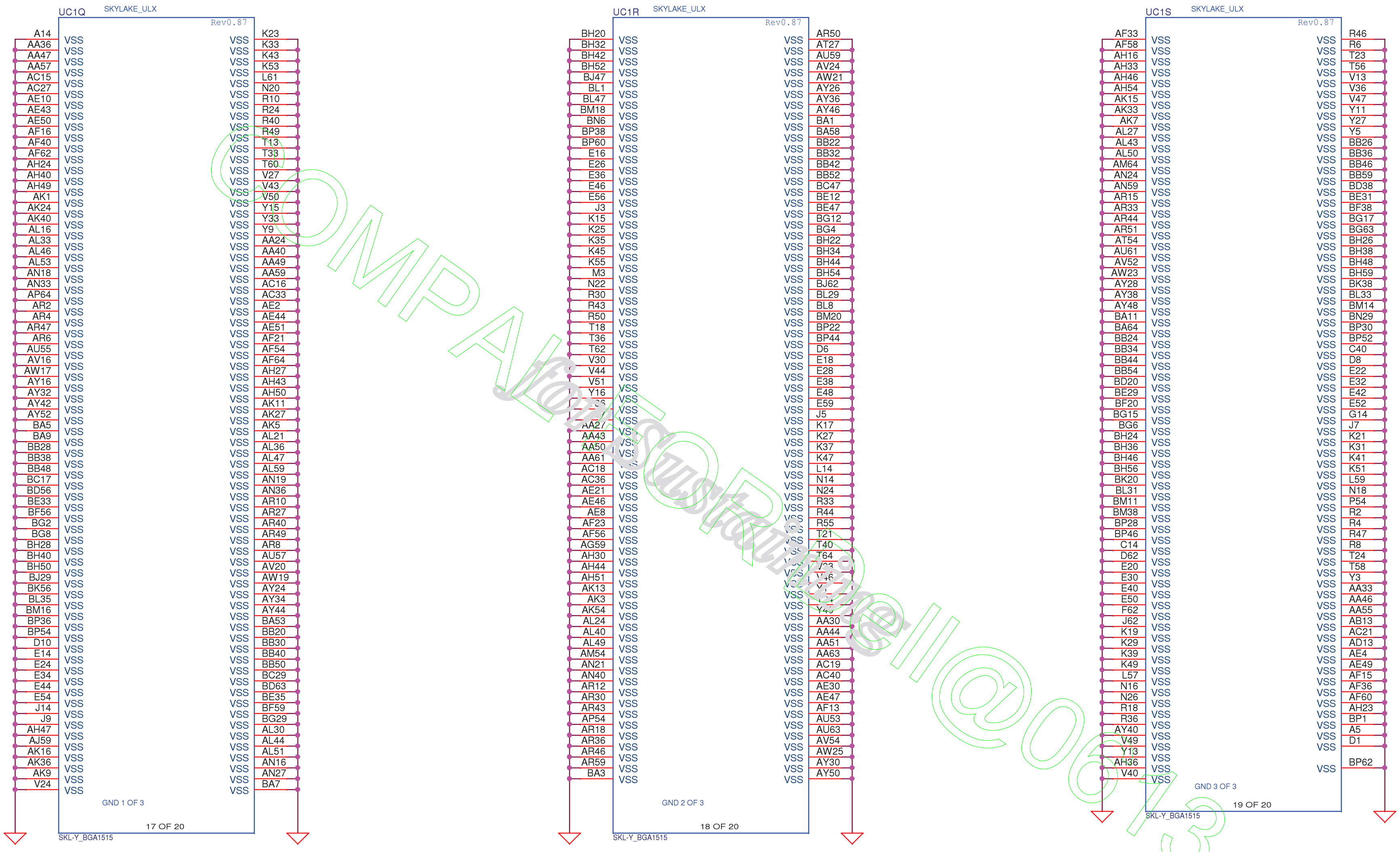
Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **SKL Y(11/13) Power**

Size | Document Number: **LA-D311P** | Rev 0.3

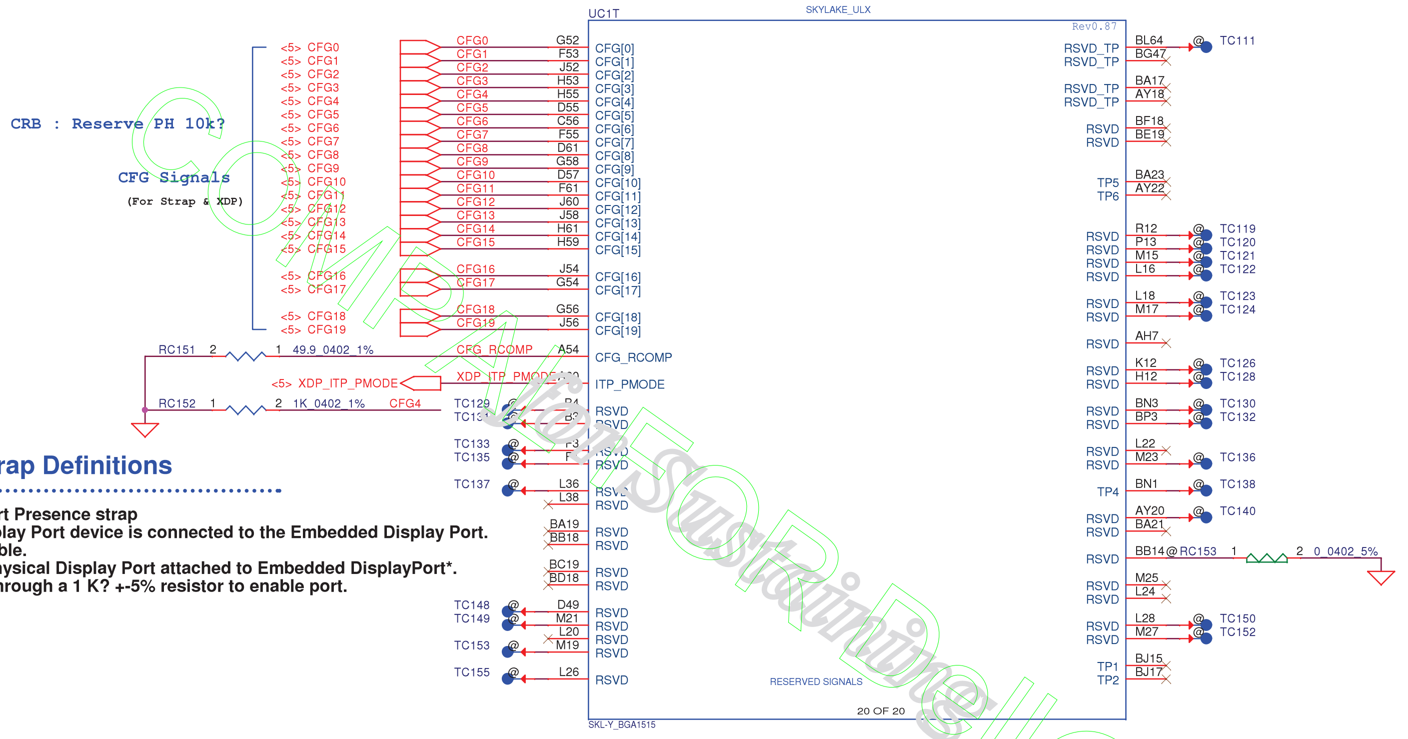
Date: Friday, December 25, 2015 |



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2041/09/08	Deciphered Date	2013/10/28	Title: SKL Y(12/13) GND

Size | Document Number: LA-D311P | Rev 0.3

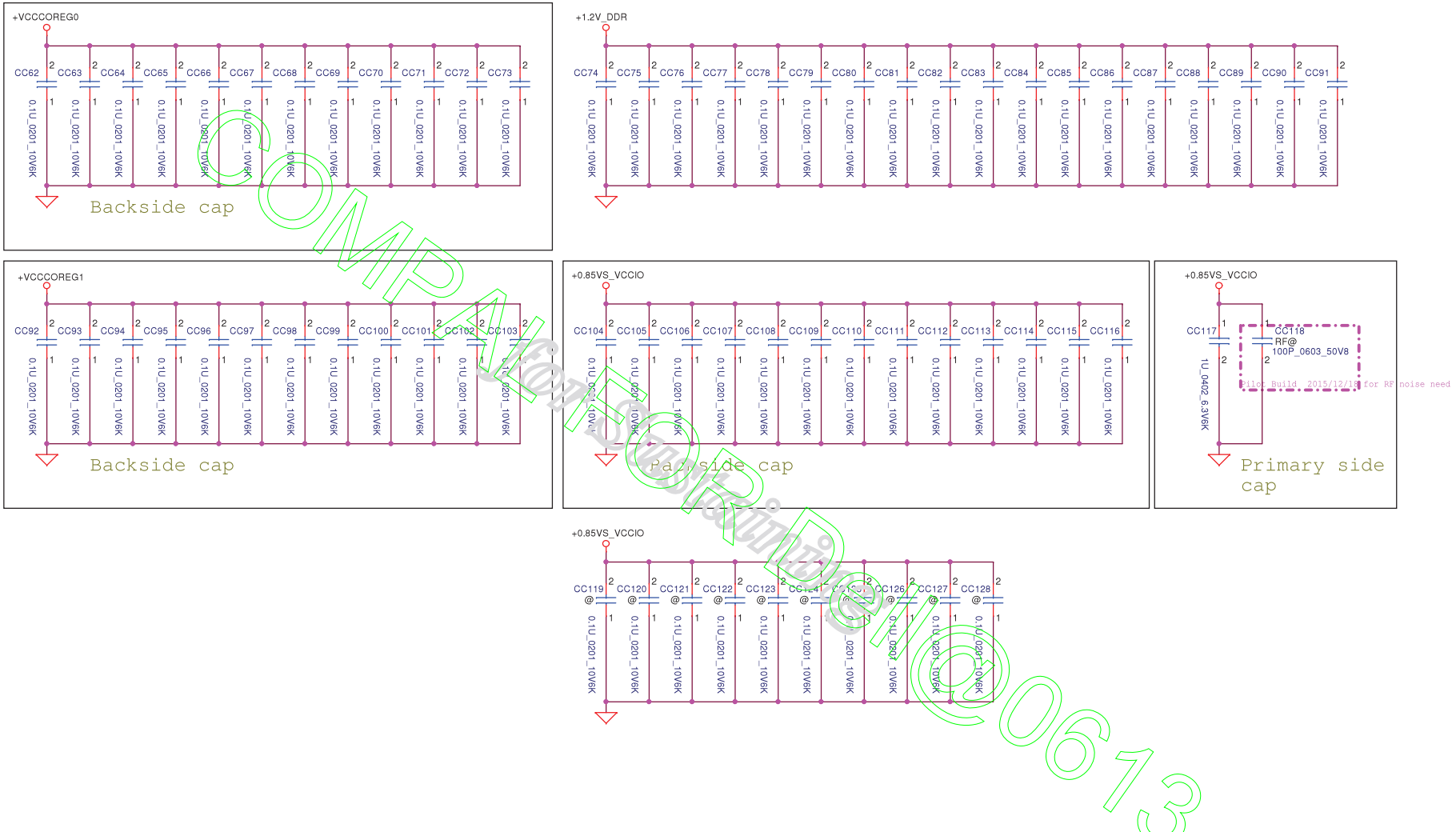
Date: Friday, December 25, 2015 | Sheet 16 of 61



Functional Strap Definitions

CFG[4] : Display Port Presence strap
0 = Enabled - A Display Port device is connected to the Embedded Display Port.
No connect for disable.
1 = Disabled - No Physical Display Port attached to Embedded DisplayPort*.
Pull-down to GND through a 1 K? +-5% resistor to enable port.

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2041/09/08	Deciphered Date	2013/10/28	Title: SKL Y(13/13) RSVD
				Size / Document Number: LA-D311P / Rev 0.3
				Date: Friday, December 25, 2015 / Sheet 17 of 61



Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **SKL Y -PROCESSOR DECOUPLING**

Size | Document Number: **LA-D311P** | Rev: 0.3

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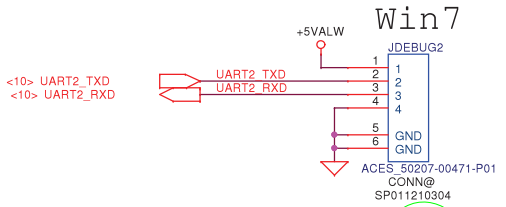
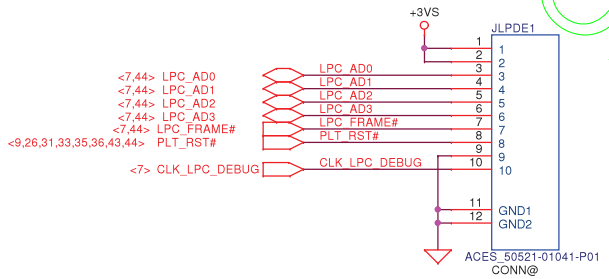
WIN debug

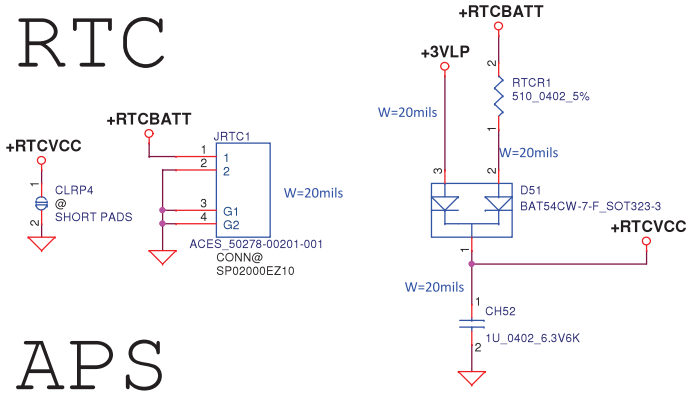
Win7



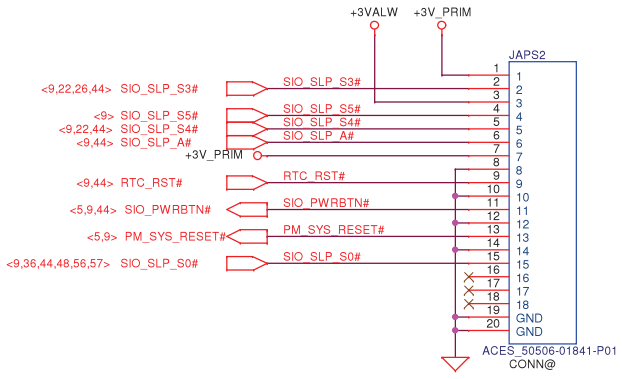
BIOS debug

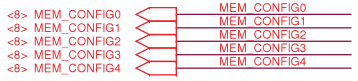


RTC

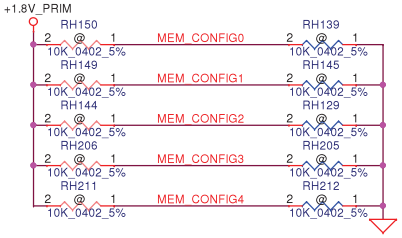


APS





DDR Memory Configuratino Type Strap pin



Pin Name	Micron 4GB SA00008PF0L	Micron 8GB SA00008Q10L	Micron 16GB SA00008QW0L	Hynix 4GB SA00008G60L	Hynix 8GB SA00008FJ0L	Hynix 16GB SA00008YT0L	Samsung 4GB SA00008PQ1L	Samsung 8GB SA00008QV1L	Samsung 16GB SA00008X11L
MEM_CONFIG0	0	1	0	1	0	1	0	1	0
MEM_CONFIG1	0	0	1	1	0	0	1	1	0
MEM_CONFIG2	0	0	0	0	1	1	1	1	0
MEM_CONFIG3	0	0	0	0	0	0	0	0	1
MEM_CONFIG4	0	0	0	0	0	0	0	0	0

DRAM Option	DRAM Config Option (MEM_CONFIG0 / MEM_CONFIG1 / MEM_CONFIG2 / MEM_CONFIG3 / MEM_CONFIG4)	X76
Micron 4G/1866	X76_M4G@ UD1 EDF8132A3MA-JD-F-R A31! SA00008PF1L; X76_M4G@ UD2 EDF8132A3MA-JD-F-R A31! SA00008PF1L; X76_M4G@ UD3 EDF8132A3MA-JD-F-R A31! SA00008PF1L; X76_M4G@ UD4 EDF8132A3MA-JD-F-R A31! SA00008PF1L	X76_M4G@ RH139 10K_0402_5% SD028100280; X76_M4G@ RH145 10K_0402_5% SD028100280; X76_M4G@ RH129 10K_0402_5% SD028100280; X76_M4G@ RH205 10K_0402_5% SD028100280; X76_M4G@ RH212 10K_0402_5% SD028100280	X7666031L03
Micron 8G/1866	X76_M8G@ UD1 EDFA232A2MA-JD-F-R A31! SA00008Q11L; X76_M8G@ UD2 EDFA232A2MA-JD-F-R A31! SA00008Q11L; X76_M8G@ UD3 EDFA232A2MA-JD-F-R A31! SA00008Q11L; X76_M8G@ UD4 EDFA232A2MA-JD-F-R A31! SA00008Q11L	X76_M8G@ RH150 10K_0402_5% SD028100280; X76_M8G@ RH145 10K_0402_5% SD028100280; X76_M8G@ RH129 10K_0402_5% SD028100280; X76_M8G@ RH205 10K_0402_5% SD028100280; X76_M8G@ RH212 10K_0402_5% SD028100280	X7666031L06
Micron 16G/1866	X76_M16G@ UD1 EDFB232A1MA-JD-F-R A31! SA00008QW1L; X76_M16G@ UD2 EDFB232A1MA-JD-F-R A31! SA00008QW1L; X76_M16G@ UD3 EDFB232A1MA-JD-F-R A31! SA00008QW1L; X76_M16G@ UD4 EDFB232A1MA-JD-F-R A31! SA00008QW1L	X76_M16G@ RH139 10K_0402_5% SD028100280; X76_M16G@ RH149 10K_0402_5% SD028100280; X76_M16G@ RH129 10K_0402_5% SD028100280; X76_M16G@ RH205 10K_0402_5% SD028100280; X76_M16G@ RH212 10K_0402_5% SD028100280	X7666031L09
Hynix 4G/1866	X76_H4G@ UD1 H9CCNNN8GTMLAR-NUD A31! SA00008G61L; X76_H4G@ UD2 H9CCNNN8GTMLAR-NUD A31! SA00008G61L; X76_H4G@ UD3 H9CCNNN8GTMLAR-NUD A31! SA00008G61L; X76_H4G@ UD4 H9CCNNN8GTMLAR-NUD A31! SA00008G61L	X76_H4G@ RH150 10K_0402_5% SD028100280; X76_H4G@ RH149 10K_0402_5% SD028100280; X76_H4G@ RH129 10K_0402_5% SD028100280; X76_H4G@ RH205 10K_0402_5% SD028100280; X76_H4G@ RH212 10K_0402_5% SD028100280	X7666031L01
Hynix 8G/1866	X76_H8G@ UD1 H9CCNNNBJTMLAR-NUD A31! SA00008FJ1L; X76_H8G@ UD2 H9CCNNNBJTMLAR-NUD A31! SA00008FJ1L; X76_H8G@ UD3 H9CCNNNBJTMLAR-NUD A31! SA00008FJ1L; X76_H8G@ UD4 H9CCNNNBJTMLAR-NUD A31! SA00008FJ1L	X76_H8G@ RH139 10K_0402_5% SD028100280; X76_H8G@ RH145 10K_0402_5% SD028100280; X76_H8G@ RH144 10K_0402_5% SD028100280; X76_H8G@ RH205 10K_0402_5% SD028100280; X76_H8G@ RH212 10K_0402_5% SD028100280	X7666031L04
Hynix 16G/1866	X76_H16G@ UD1 H9CCNNNCLTMLAR-NUD A31! SA00008YT1L; X76_H16G@ UD2 H9CCNNNCLTMLAR-NUD A31! SA00008YT1L; X76_H16G@ UD3 H9CCNNNCLTMLAR-NUD A31! SA00008YT1L; X76_H16G@ UD4 H9CCNNNCLTMLAR-NUD A31! SA00008YT1L	X76_H16G@ RH150 10K_0402_5% SD028100280; X76_H16G@ RH145 10K_0402_5% SD028100280; X76_H16G@ RH144 10K_0402_5% SD028100280; X76_H16G@ RH205 10K_0402_5% SD028100280; X76_H16G@ RH212 10K_0402_5% SD028100280	X7666031L07
Samsung 4G/1866	X76_S4G@ UD1 K4E8E304EE-EGCF A31! SA00008PQ1L; X76_S4G@ UD2 K4E8E304EE-EGCF A31! SA00008PQ1L; X76_S4G@ UD3 K4E8E304EE-EGCF A31! SA00008PQ1L; X76_S4G@ UD4 K4E8E304EE-EGCF A31! SA00008PQ1L	X76_S4G@ RH139 10K_0402_5% SD028100280; X76_S4G@ RH149 10K_0402_5% SD028100280; X76_S4G@ RH144 10K_0402_5% SD028100280; X76_S4G@ RH205 10K_0402_5% SD028100280; X76_S4G@ RH212 10K_0402_5% SD028100280	X7666031L02
Samsung 8G/1866	X76_S8G@ UD1 K4E6E304EE-EGCF A31! SA00008QV1L; X76_S8G@ UD2 K4E6E304EE-EGCF A31! SA00008QV1L; X76_S8G@ UD3 K4E6E304EE-EGCF A31! SA00008QV1L; X76_S8G@ UD4 K4E6E304EE-EGCF A31! SA00008QV1L	X76_S8G@ RH150 10K_0402_5% SD028100280; X76_S8G@ RH149 10K_0402_5% SD028100280; X76_S8G@ RH144 10K_0402_5% SD028100280; X76_S8G@ RH205 10K_0402_5% SD028100280; X76_S8G@ RH212 10K_0402_5% SD028100280	X7666031L05
Samsung 16G/1866	X76_S16G@ UD1 K4EBE304EB-EGCF A31! SA00008X11L; X76_S16G@ UD2 K4EBE304EB-EGCF A31! SA00008X11L; X76_S16G@ UD3 K4EBE304EB-EGCF A31! SA00008X11L; X76_S16G@ UD4 K4EBE304EB-EGCF A31! SA00008X11L	X76_S16G@ RH139 10K_0402_5% SD028100280; X76_S16G@ RH145 10K_0402_5% SD028100280; X76_S16G@ RH129 10K_0402_5% SD028100280; X76_S16G@ RH206 10K_0402_5% SD028100280; X76_S16G@ RH212 10K_0402_5% SD028100280	X7666031L08

Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: RTC,Debug, RAM setting

Size | Document Number: LA-D311P | Rev: 0.3

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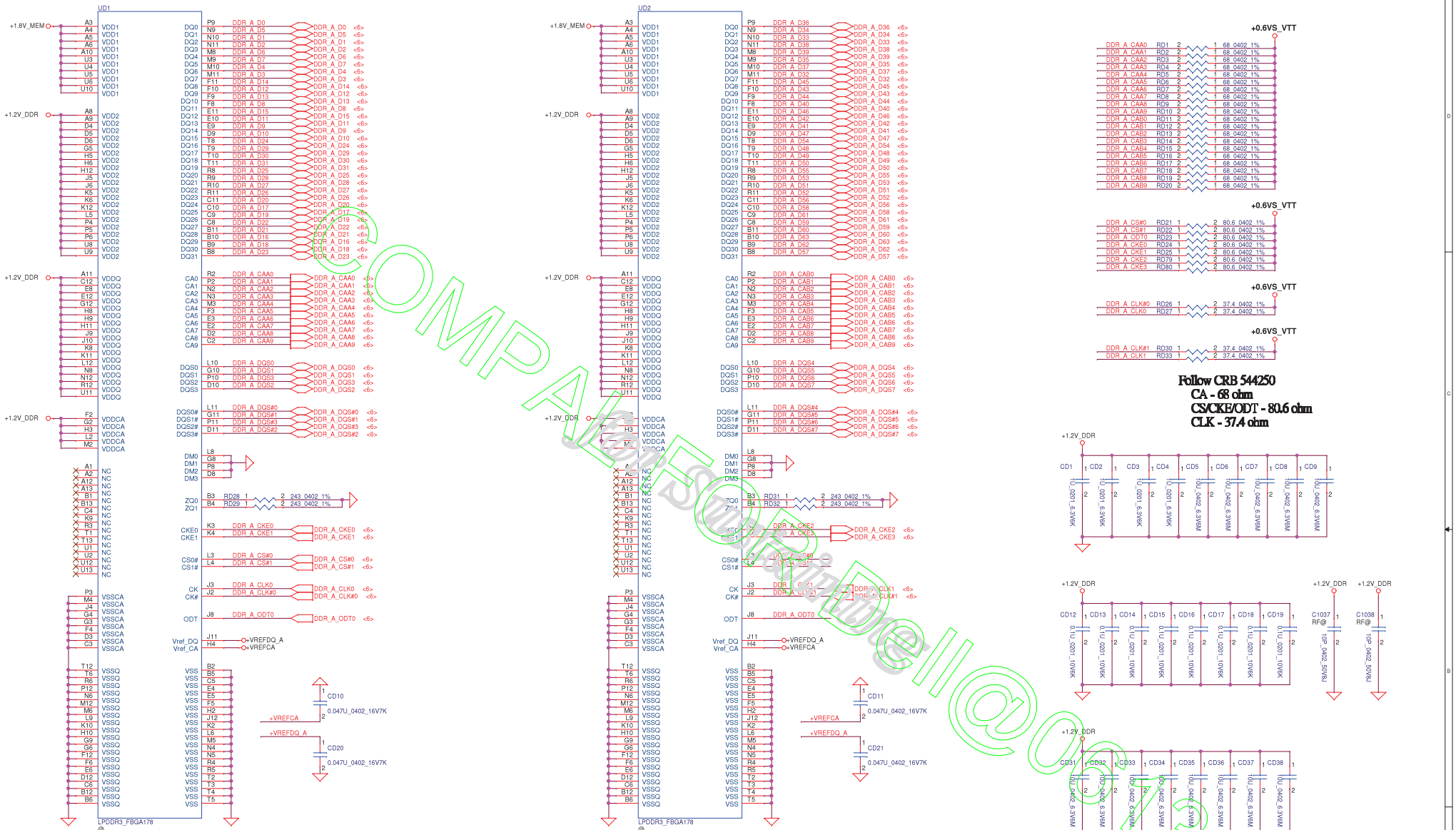
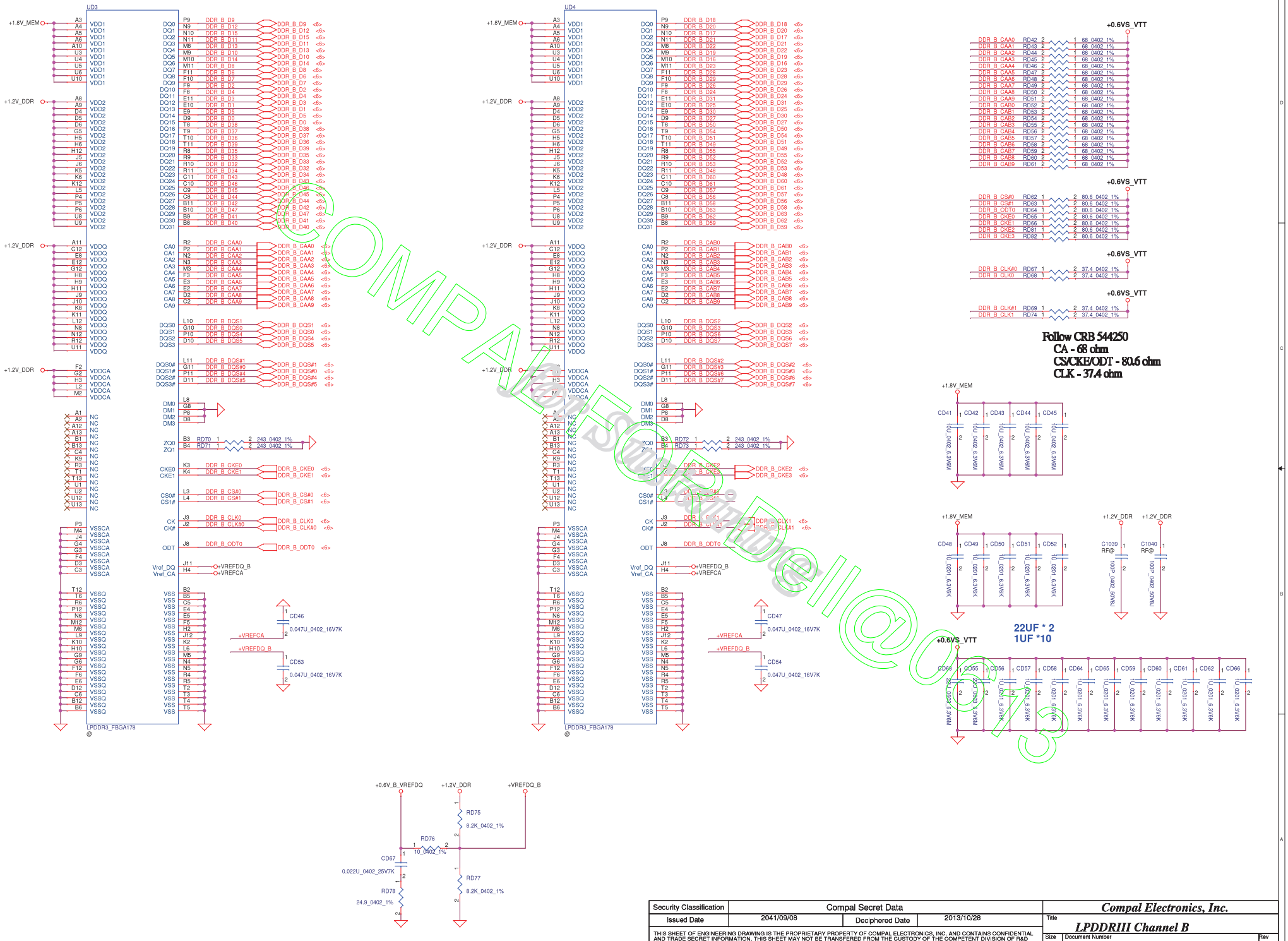


Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: LPDDRIII Channel A			
Size	Document Number: LA-D311P		Rev: 0.3
Date: Friday, December 25, 2015	Sheet 20 of 61		



Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title	LPDDRIII Channel B		
Size	Document Number		Rev
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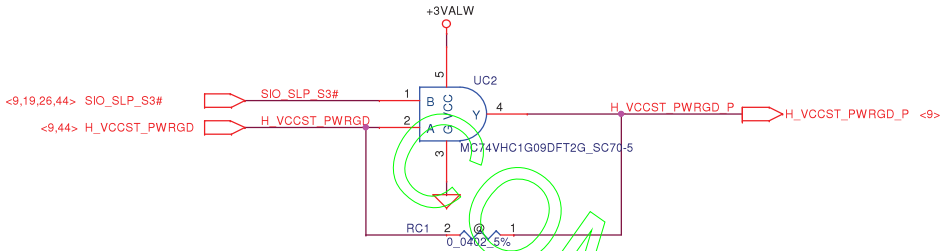
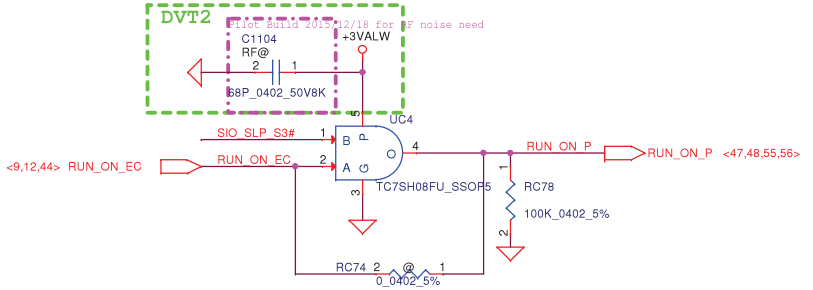
Date:	Friday, December 25, 2015	Sheet	21 of 61

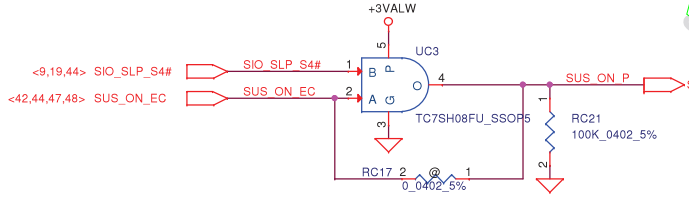


Change CPU VCCST_PWRGD enable from EC & PCH

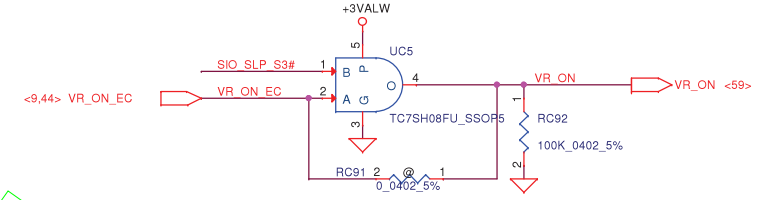
H_VCCST_PWRGD(3.3V), H_VCCST_PWRGD_P(1.0V)
If need to mount RC1, need to add level shift.



Change VCCIO & VCCSTG power enable from EC & PCH



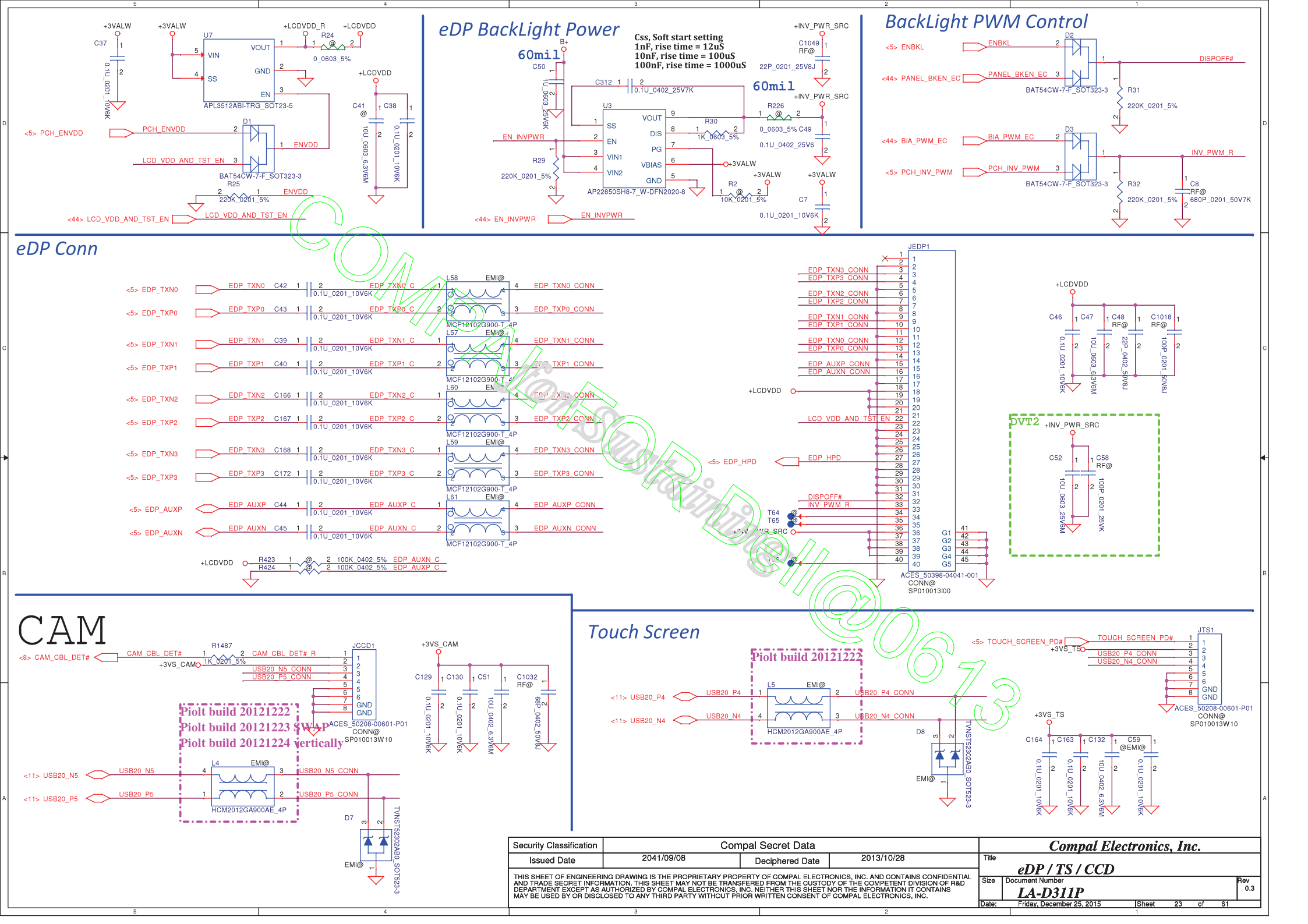
Change VCCST & 1.2_VR power enable from EC & PCH



Change VCORE power enable from EC & PCH

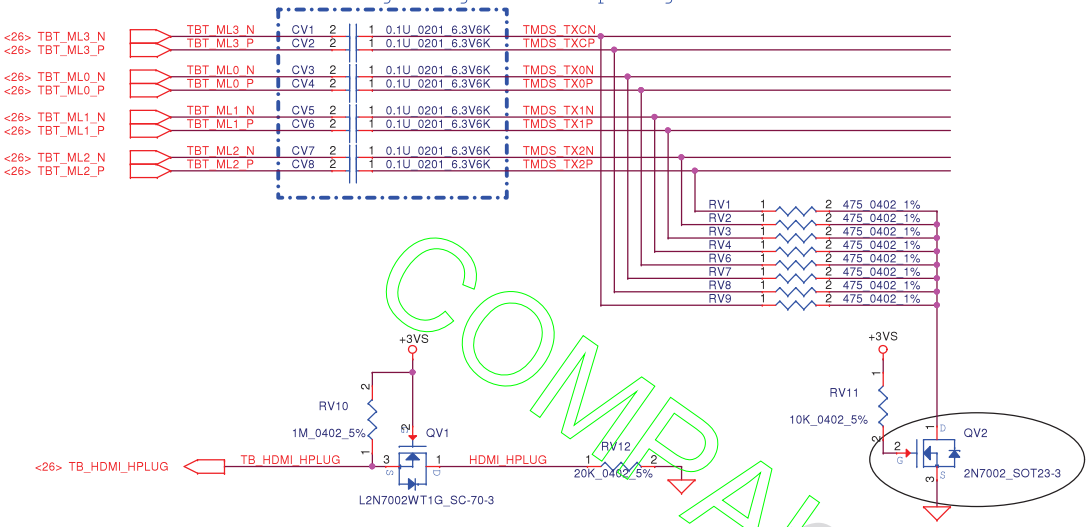
Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: Sequence Logic			
Size	Document Number: LA-D311P		Rev: 0.3
Date: Friday, December 25, 2015	Sheet 22 of 61		

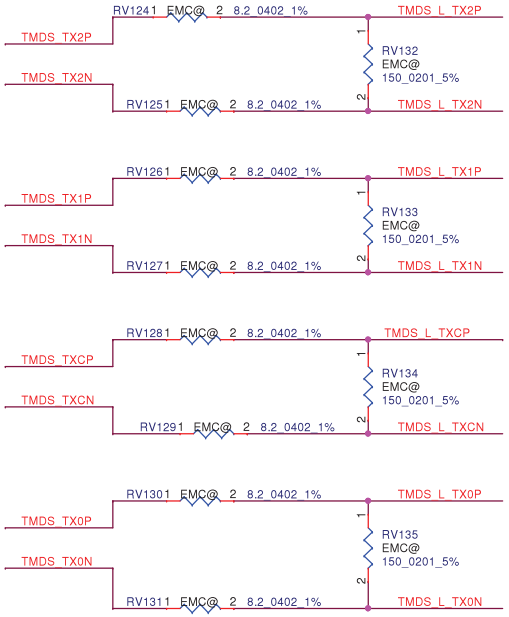

eDP BackLight Power
Css, Soft start setting
1nF, rise time = 12uS
10nF, rise time = 100uS
100nF, rise time = 1000uS
60mil
60mil
BackLight PWM Control
eDP Conn
CAM
Touch Screen
Piolt build 20121222
Piolt build 20121223 SWAP
Piolt build 20121224 vertically
Compal Confidential@0613
Compal Electronics, Inc.
eDP / TS / CCD
LA-D311P
Compal Secret Data
2041/09/08
2013/10/28
Friday, December 25, 2015

HDMI Active Level Shift(ALS type)

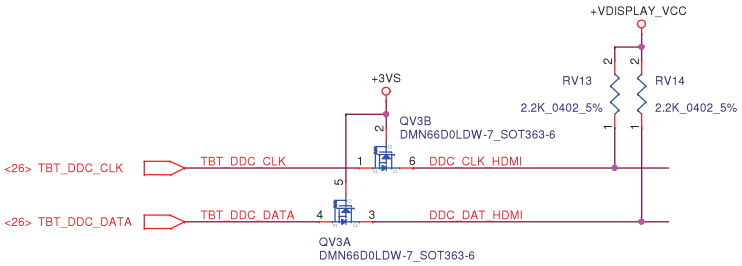
1014: Steg change to 0201 package.



Place close to JHDMI1 For EMI

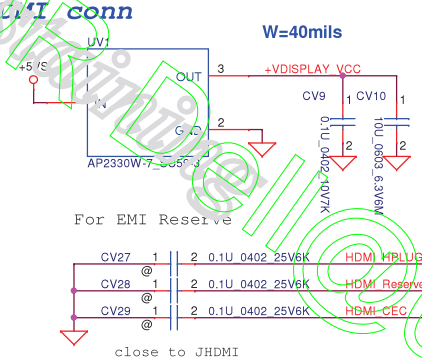


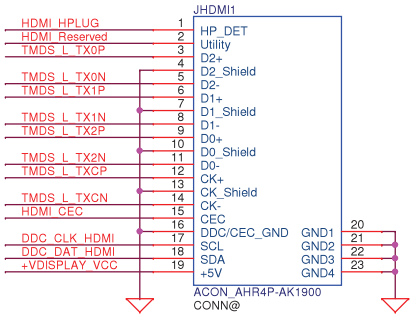
HDMI DDC

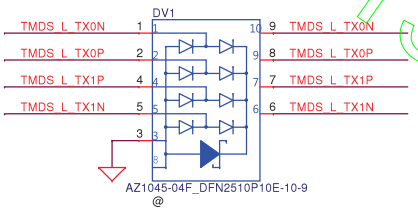


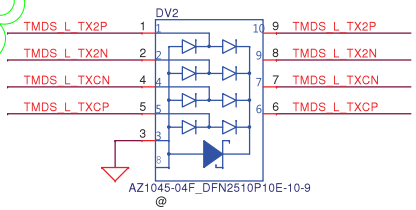
HDMI conn

W=40mils









Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: HDMI

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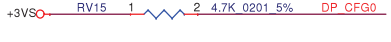
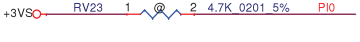


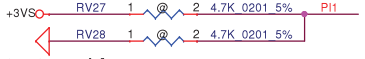
Chip operational mode configuration;
Internal pull down at ~150K?, 3.3V I/O.

L: Control switching mode (default)
H: Automatic switching mode

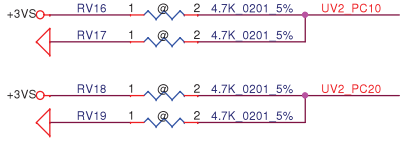


Automatic EQ disable;
Internal pull down at ~150K?, 3.3V IO

L: Automatic EQ enable (default)
H: Automatic EQ disable

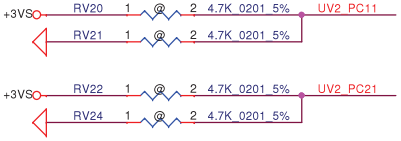


Auto test enable;
Internal pull down at ~150K?, 3.3V I/O.
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable



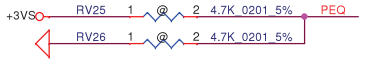
AUX interception disable for Port y (y=1,2)
Internal pull down at ~150K?, 3.3V I/O.

L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mv and 0dB
M: AUX interception disable, driver output with fixed 400mv and 0dB



Output swing adjusment for Port y (y=1,2).
Internal pull down at ~150K?, 3.3V I/O.

L:default
H: +20%
M: -26.7%

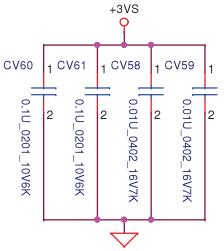


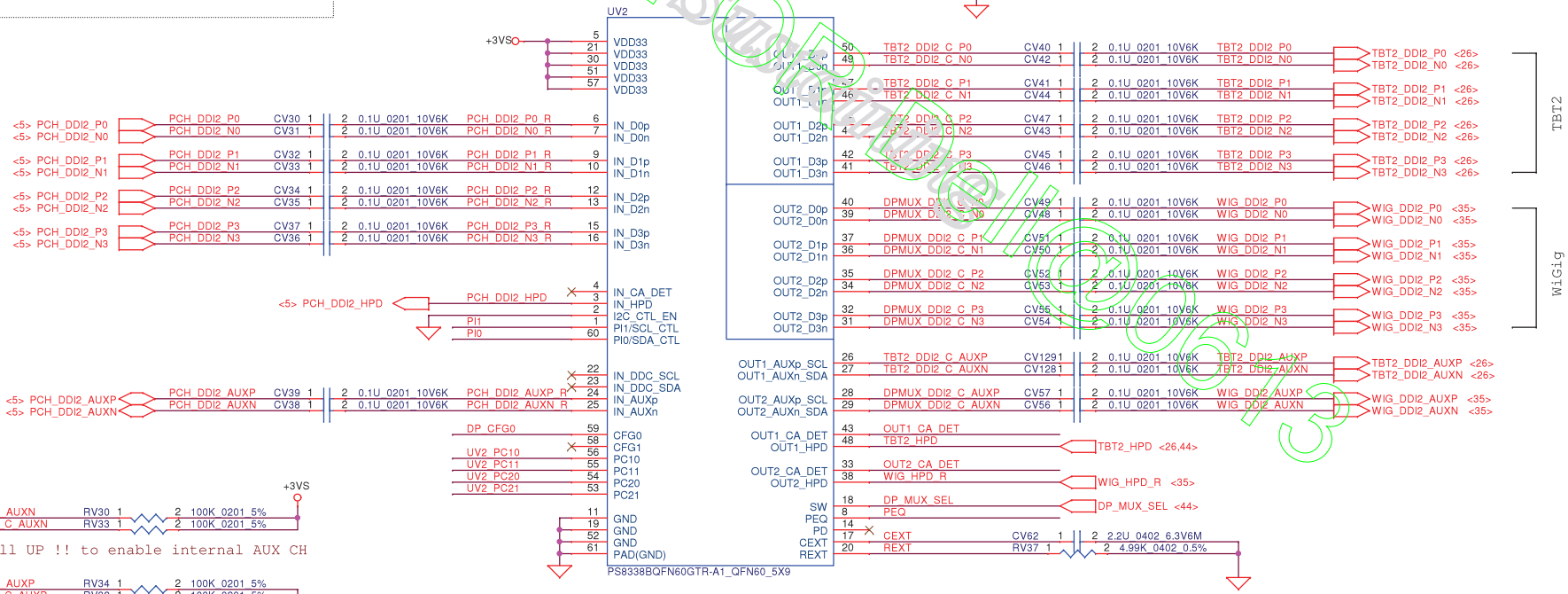
Programmable input equalization levels; Internal pull down at ~150K?, 3.3V I/O.

L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

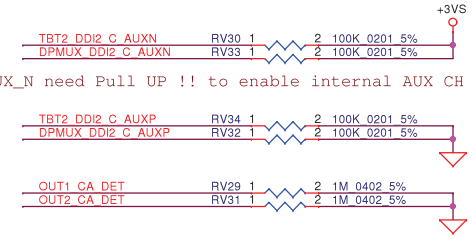
DP_MUX_SEL pin

Port switching control or priority configuration;
Internal pull down at ~150K?, 3.3V I/O.
L: Port1 is selected or with higher priority (default)
H: Port2 is selected or with higher priority





AUX_N need Pull UP !! to enable internal AUX CH



Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: DP MUX

Size | Document Number: LA-D311P | Rev: 0.3

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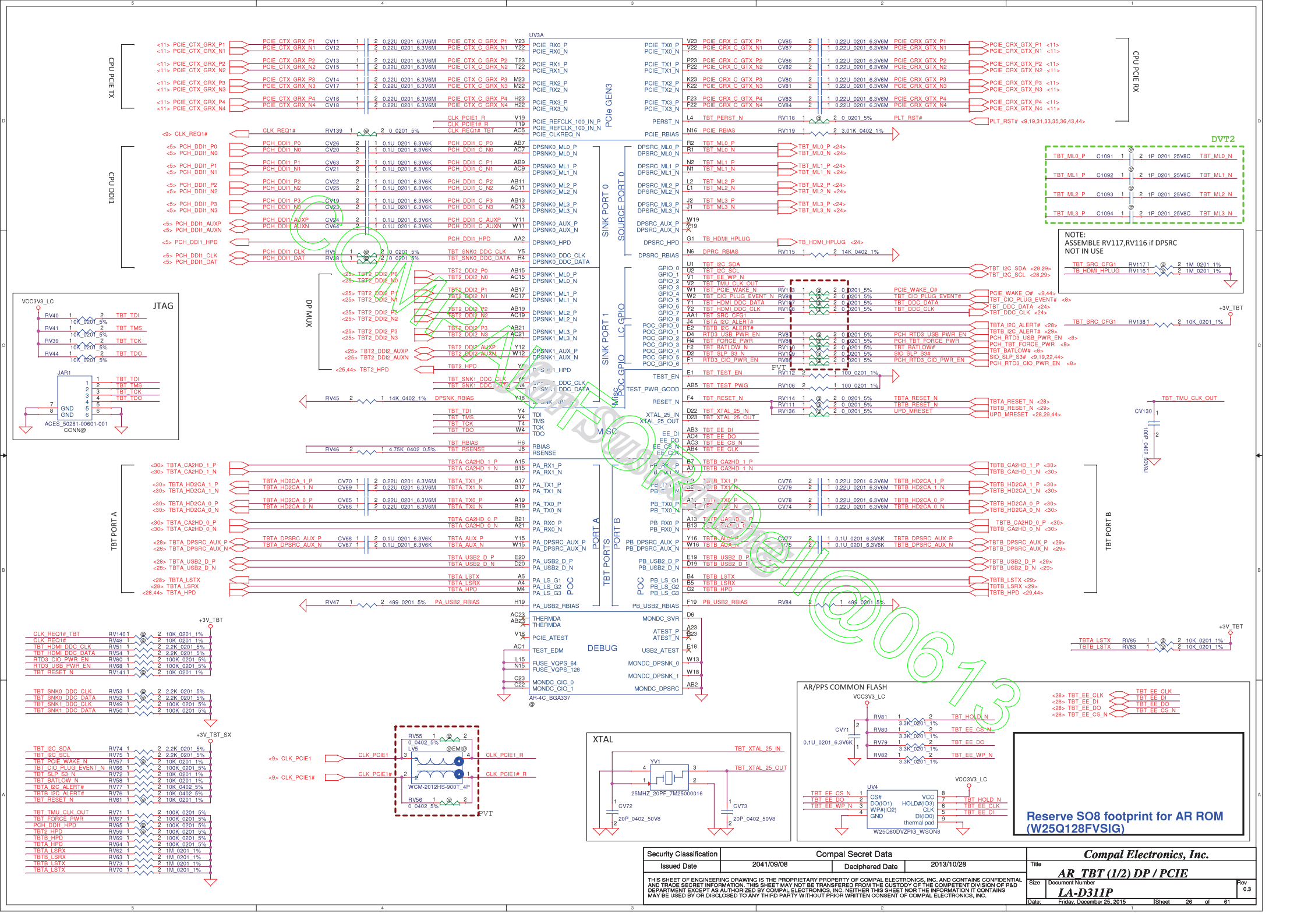


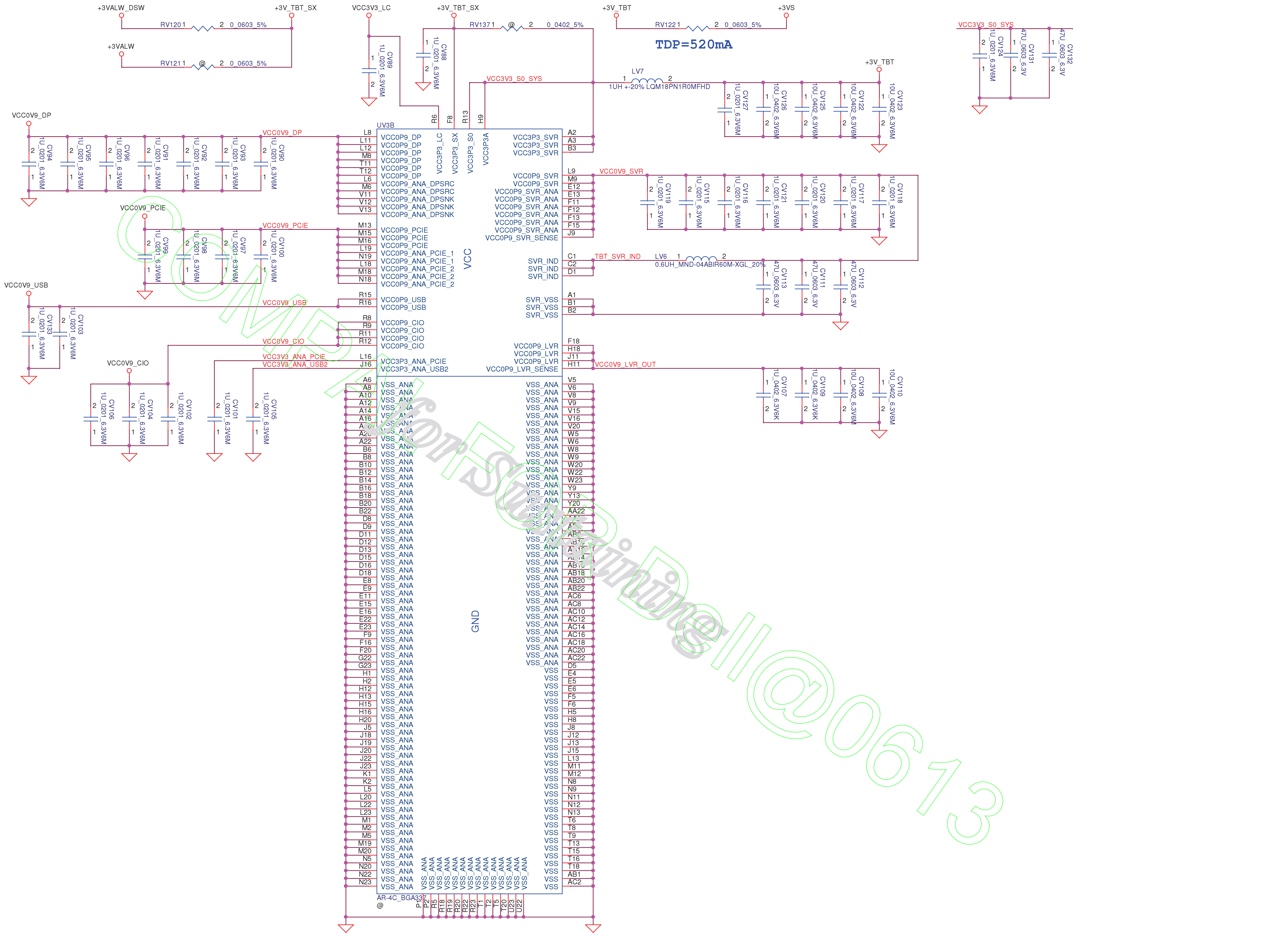
Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: AR_TBT (1/2) DP / PCIE

Size: — Document Number: LA-D311P — Rev: 0.3

Date: Friday, December 25, 2015 — Sheet 26 of 61



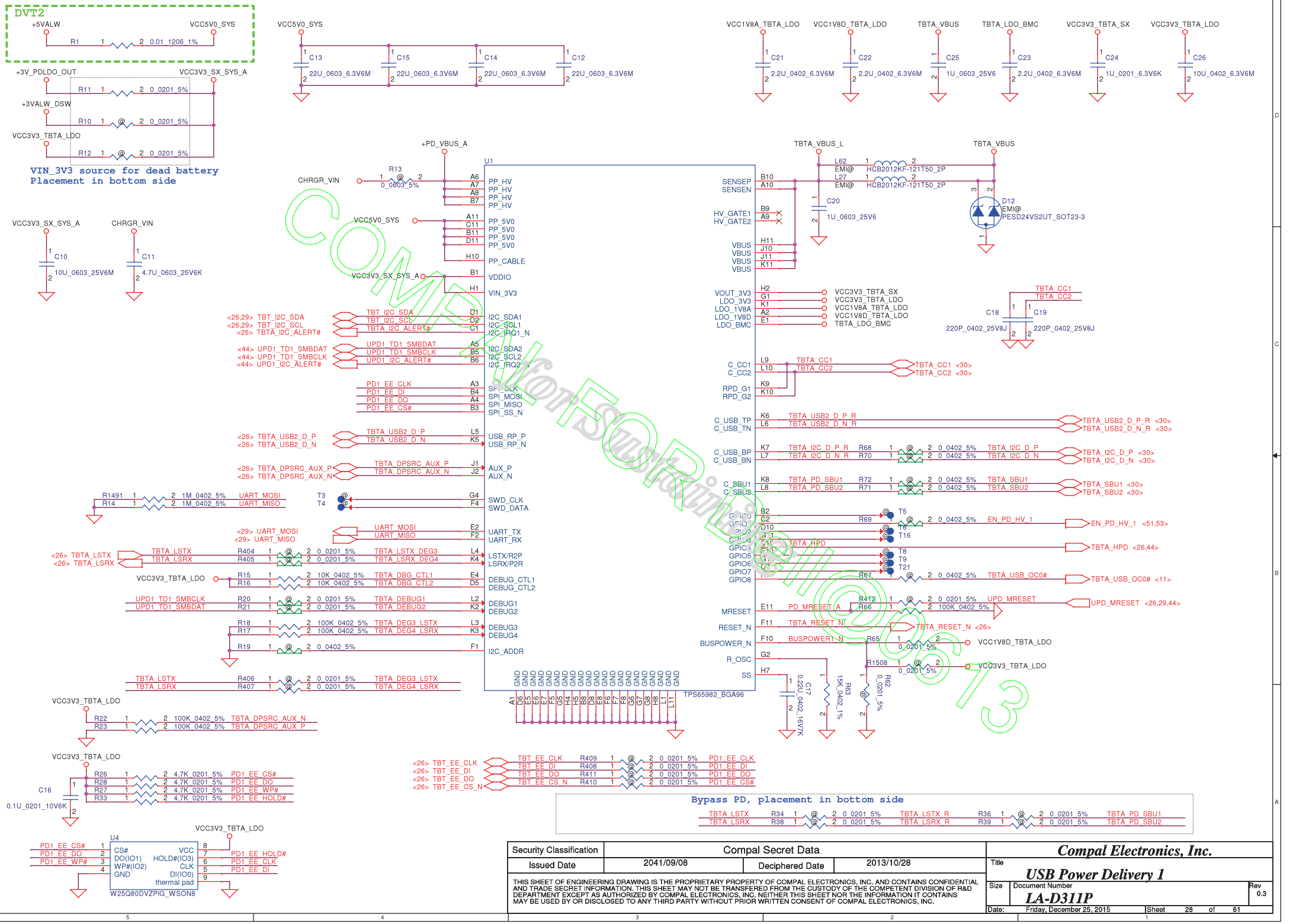
Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: AR_TBT (2/2) PWR / VSS

Size | Document Number: LA-D311P | Rev: 0.3

Date: Friday, December 25, 2015 | Sheet 27 of 61



Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **USB Power Delivery 1**

Size	Document Number	Rev
	LA-D311P	0.3

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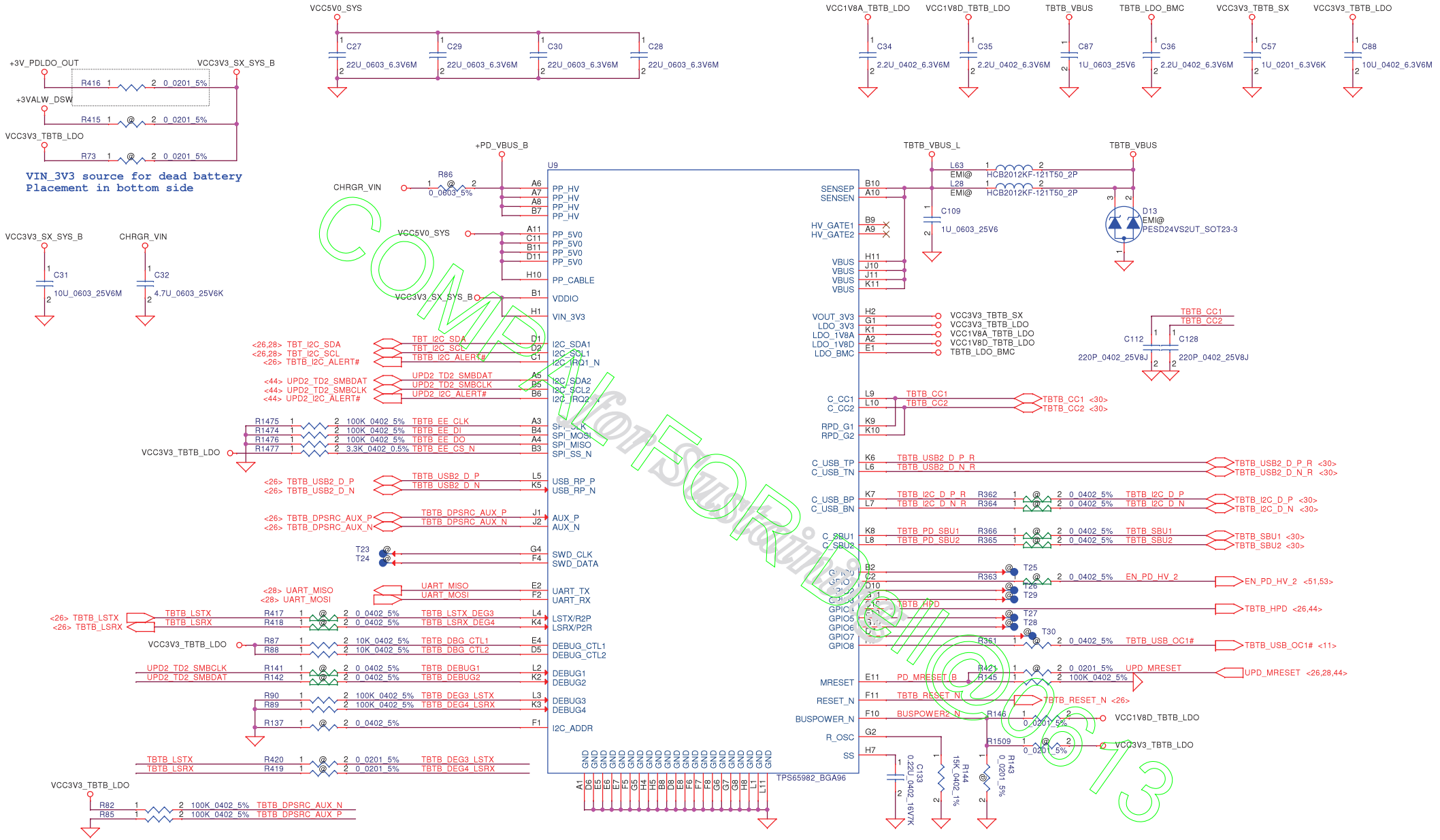


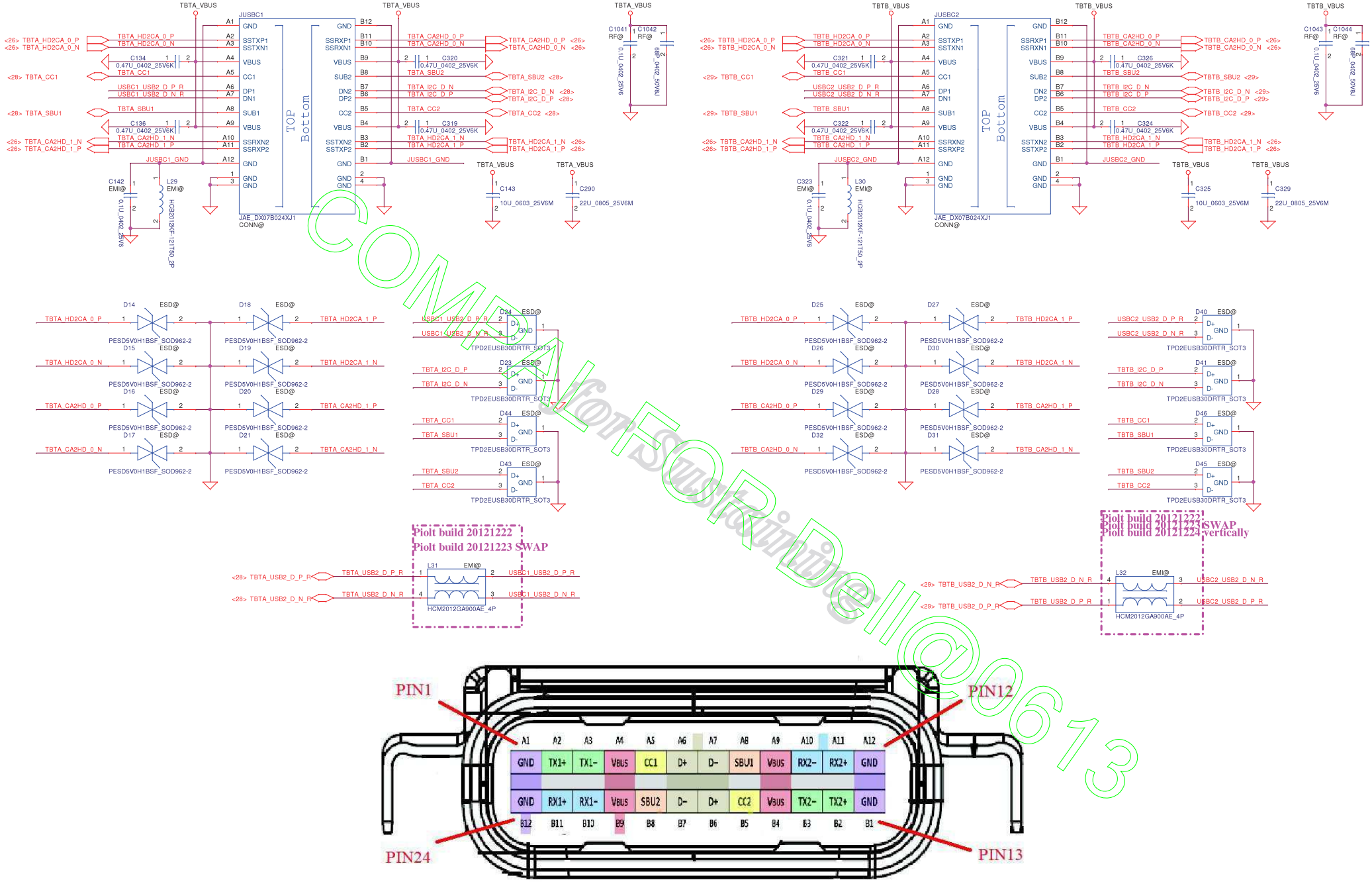
Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **USB Power Delivery 2**

Size	Document Number	Rev
	LA-D311P	0.3

Date: Friday, December 25, 2015 Sheet 29 of 61



Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

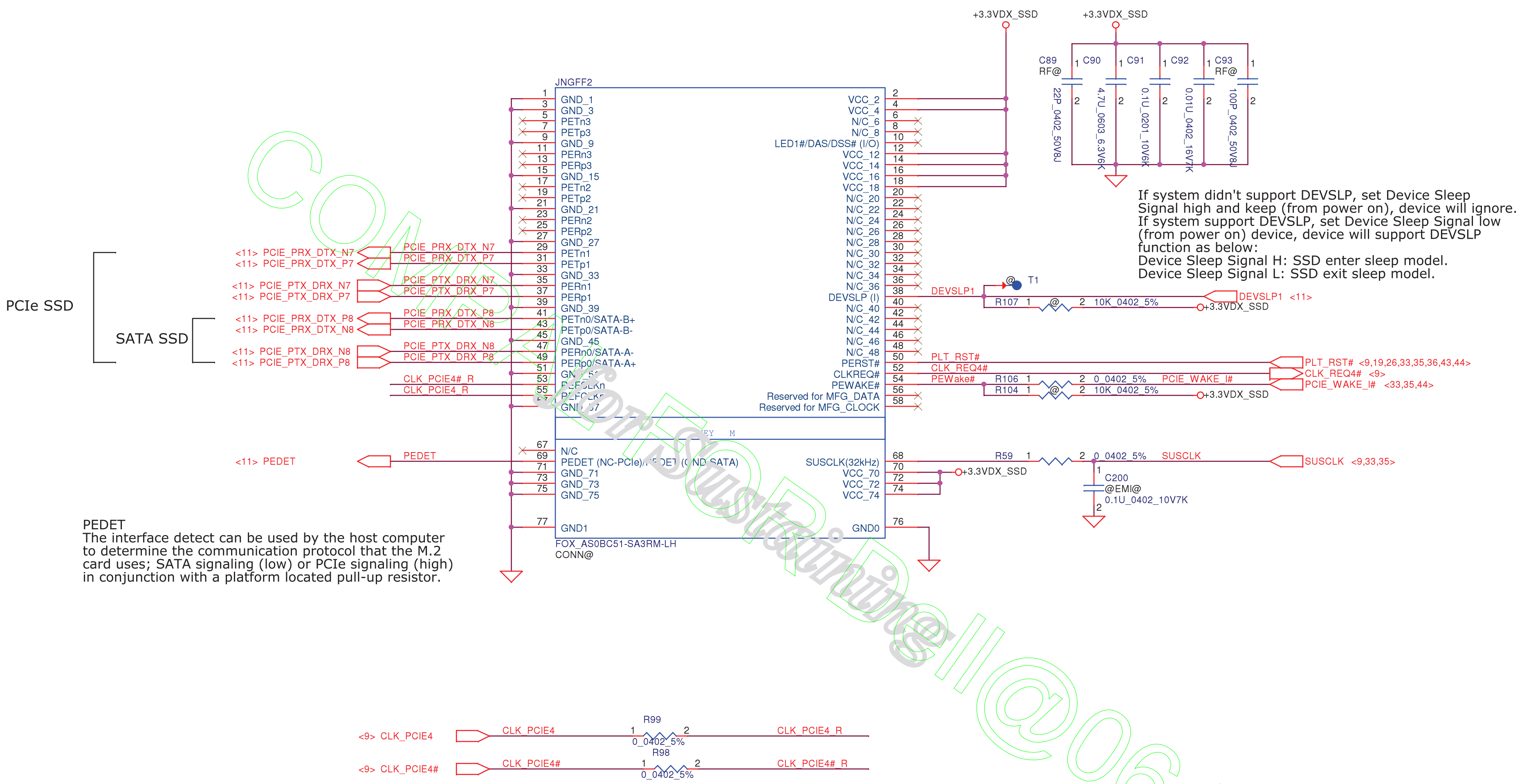
Compal Electronics, Inc.

Title: **USB Type C**

Size | Document Number: **LA-D311P** | Rev: 0.3

Date: Friday, December 25, 2015 | Sheet 30 of 61

NGFF(SATA)



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2041/09/08	Deciphered Date	2013/10/28	Title: SATA SSD

Size | Document Number: LA-D311P | Rev 0.3

Date: Friday, December 25, 2015 | Sheet 31 of 61

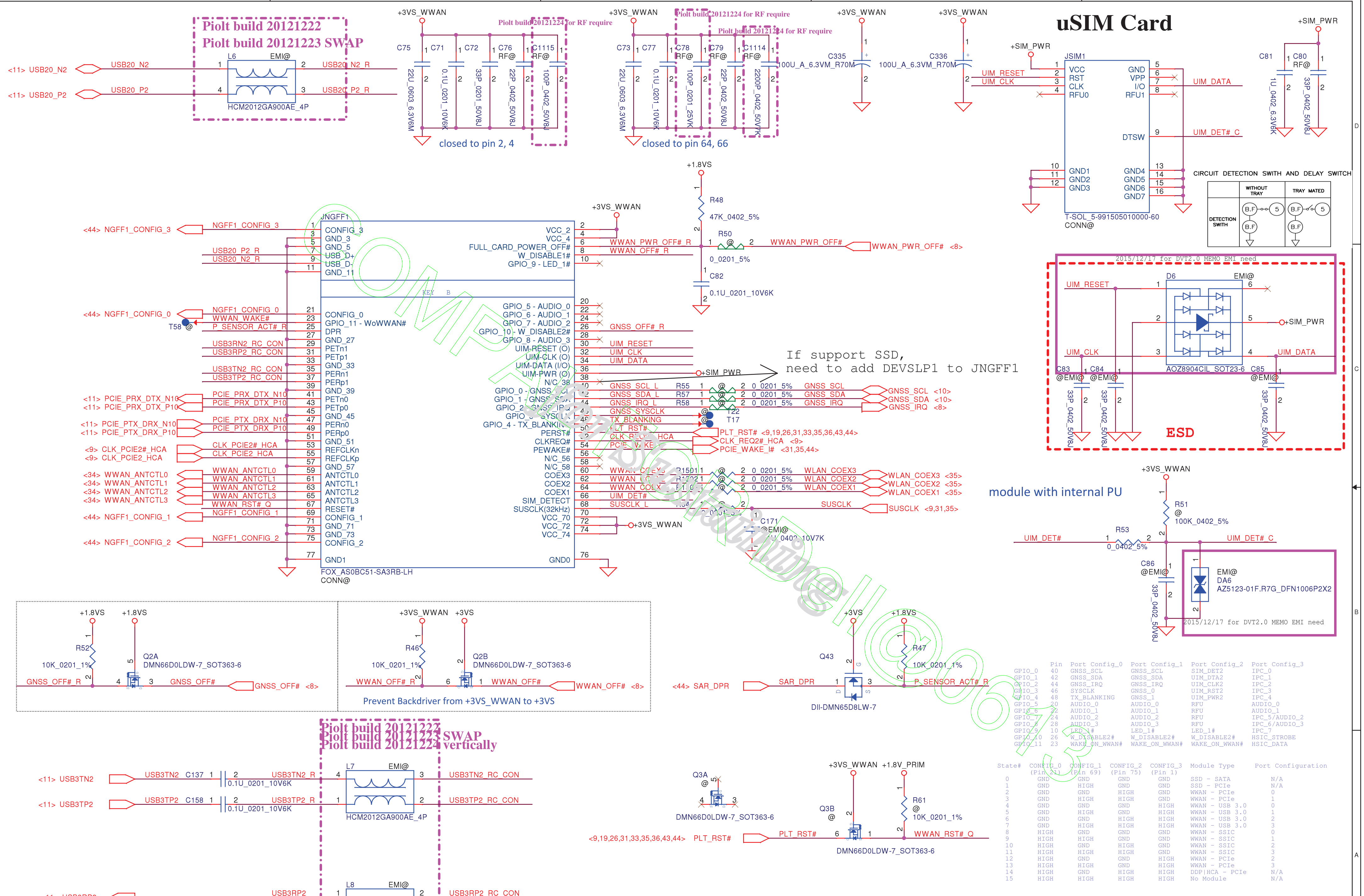
Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **Reserved**

Size	Document Number	Rev
	LA-D311P	0.3

Date: Friday, December 25, 2015 | Sheet 32 of 61



	Pin	Port Config_0	Port Config_1	Port Config_2	Port Config_3
GPIO_0	40	GNSS_SCL	GNSS_SCL	SIM_DET2	IPC_0
GPIO_1	42	GNSS_SDA	GNSS_SDA	UIM_DTA2	IPC_1
GPIO_2	44	GNSS_IRQ	GNSS_IRQ	UIM_CLK2	IPC_2
GPIO_3	46	SYSCLK	GNSS_0	UIM_RST2	IPC_3
GPIO_4	48	TX_BLANKING	GNSS_1	UIM_PWR2	IPC_4
GPIO_5	20	AUDIO_0	AUDIO_0	RFU	AUDIO_0
GPIO_6	22	AUDIO_1	AUDIO_1	RFU	AUDIO_1
GPIO_7	24	AUDIO_2	AUDIO_2	RFU	IPC_5/AUDIO_2
GPIO_8	28	AUDIO_3	AUDIO_3	RFU	IPC_6/AUDIO_3
GPIO_9	10	LED_1#	LED_1#	LED_1#	IPC_7
GPIO_10	26	W_DISABLE2#	W_DISABLE2#	W_DISABLE2#	HSIC_STROBE
GPIO_11	23	WAKE_ON_WWAN#	WAKE_ON_WWAN#	WAKE_ON_WWAN#	HSIC_DATA

State#	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type	Port Configuration
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	HIGH	GND	GND	SSD - PCIe	N/A
2	GND	GND	HIGH	GND	WWAN - PCIe	0
3	GND	HIGH	HIGH	GND	WWAN - PCIe	1
4	GND	GND	GND	HIGH	WWAN - USB 3.0	0
5	GND	HIGH	GND	HIGH	WWAN - USB 3.0	1
6	GND	GND	HIGH	HIGH	WWAN - USB 3.0	2
7	GND	HIGH	HIGH	HIGH	WWAN - USB 3.0	3
8	HIGH	GND	GND	GND	WWAN - SSIC	0
9	HIGH	HIGH	GND	GND	WWAN - SSIC	1
10	HIGH	GND	HIGH	GND	WWAN - SSIC	2
11	HIGH	HIGH	HIGH	GND	WWAN - SSIC	3
12	HIGH	GND	GND	HIGH	WWAN - PCIe	2
13	HIGH	HIGH	GND	HIGH	WWAN - PCIe	3
14	HIGH	GND	HIGH	HIGH	DDP|HCA - PCIe	N/A
15	HIGH	HIGH	HIGH	HIGH	No Module	N/A

Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

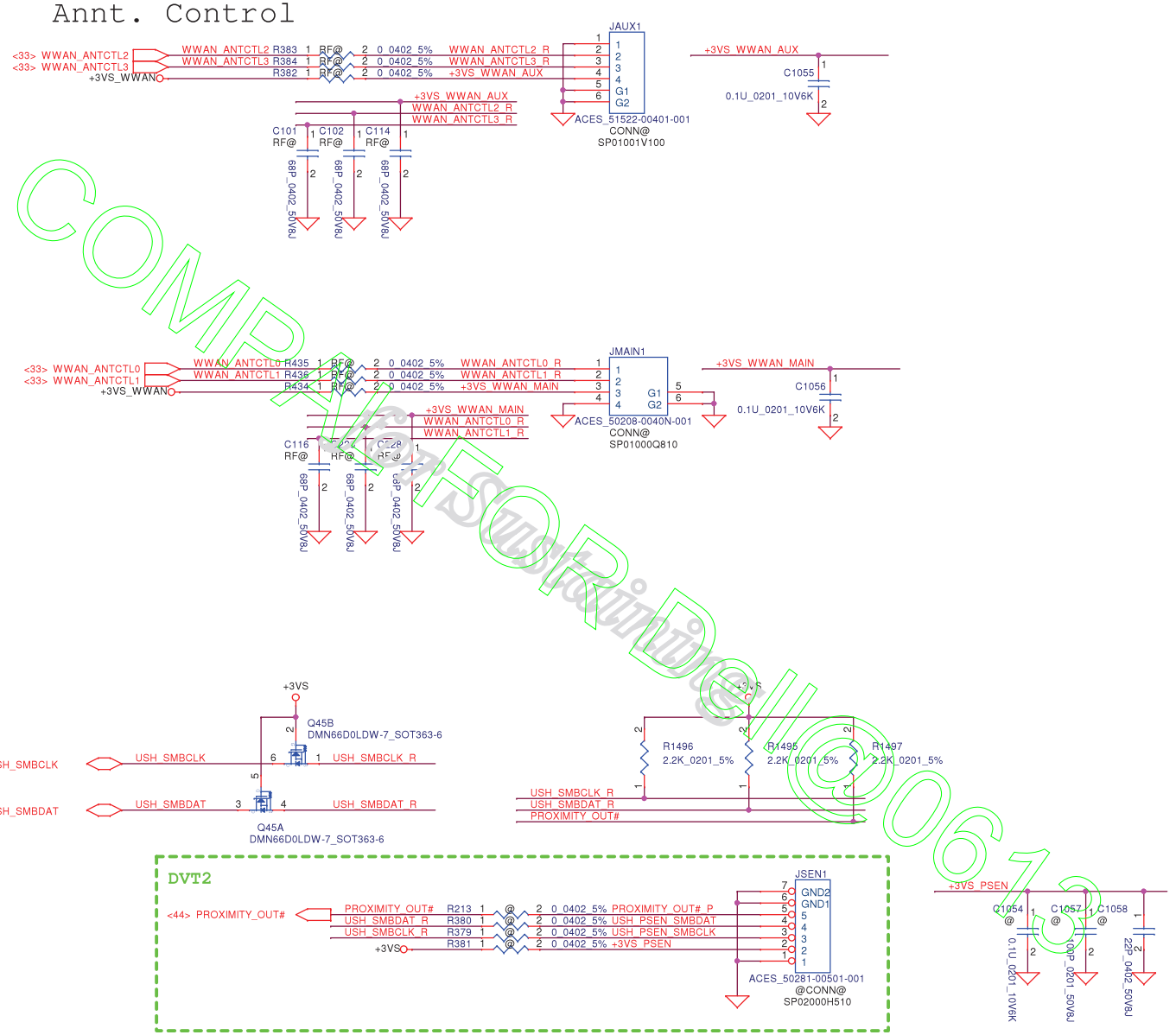
Compal Electronics, Inc.

Title: **P33-WWAN**

Size | Document Number: **LA-D311P** | Rev 0.3

Date: Friday, December 25, 2015 | Sheet 33 of 61

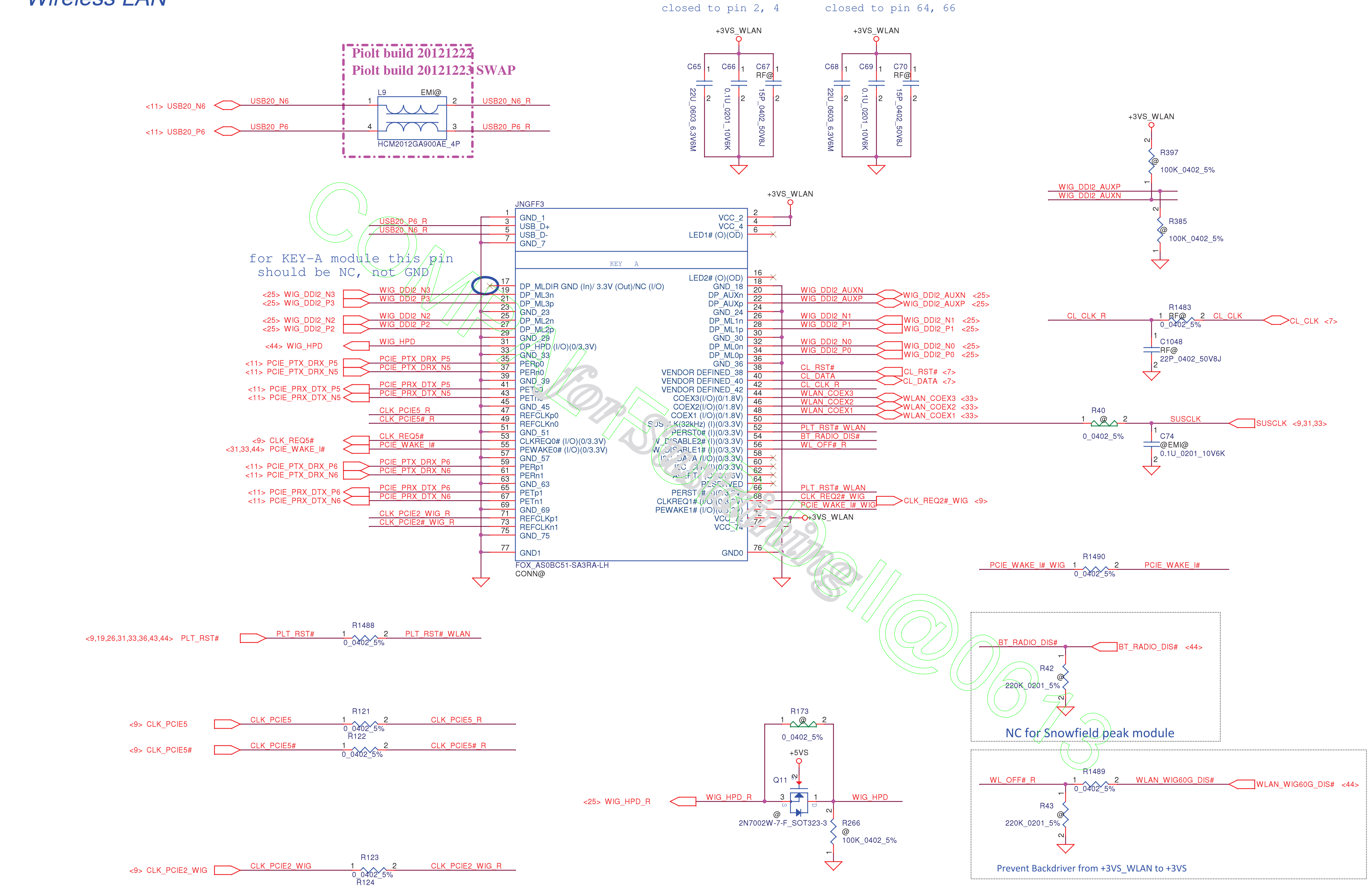
Annt. Control



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Title	RF Conn.		
Size	Document Number		Rev
	LA-D311P		0.3
Date:	Friday, December 25, 2015	Sheet 34 of 61	

Wireless LAN



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2041/09/08	Deciphered Date	2013/10/28	Title: WLAN / BT
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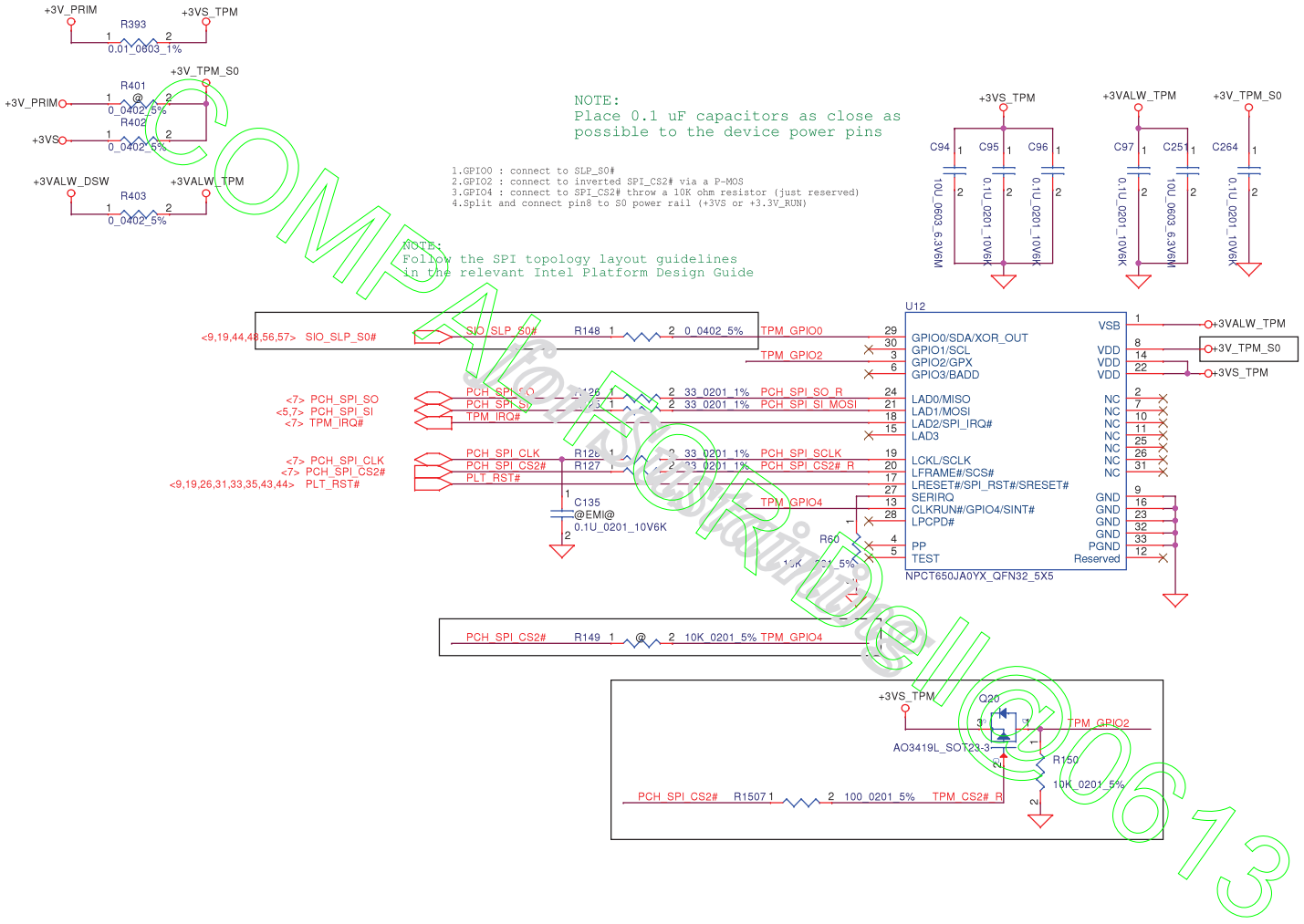
				Date: Friday, December 25, 2015 Sheet 35 of 61

TPM



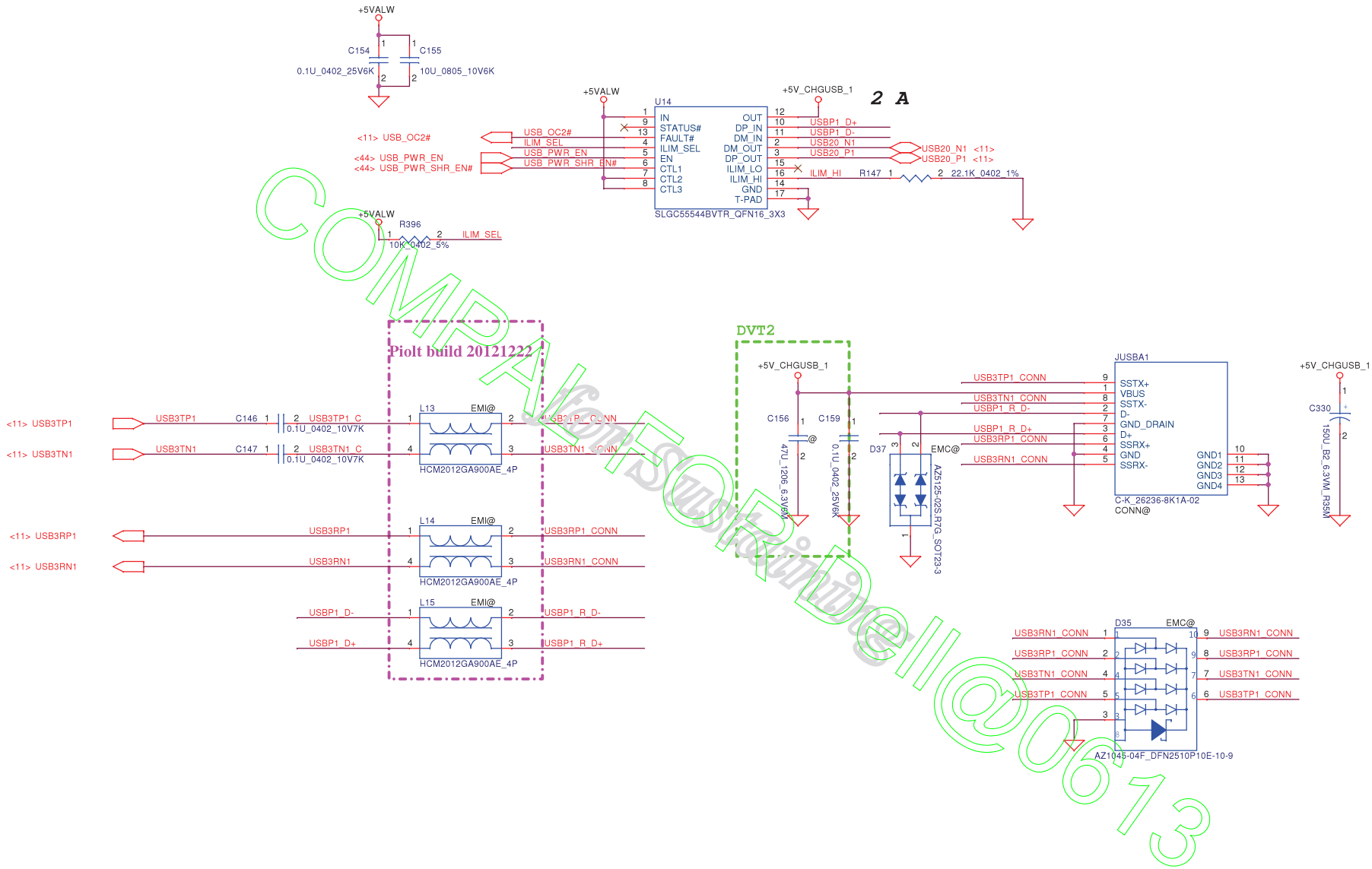
Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **TPM**

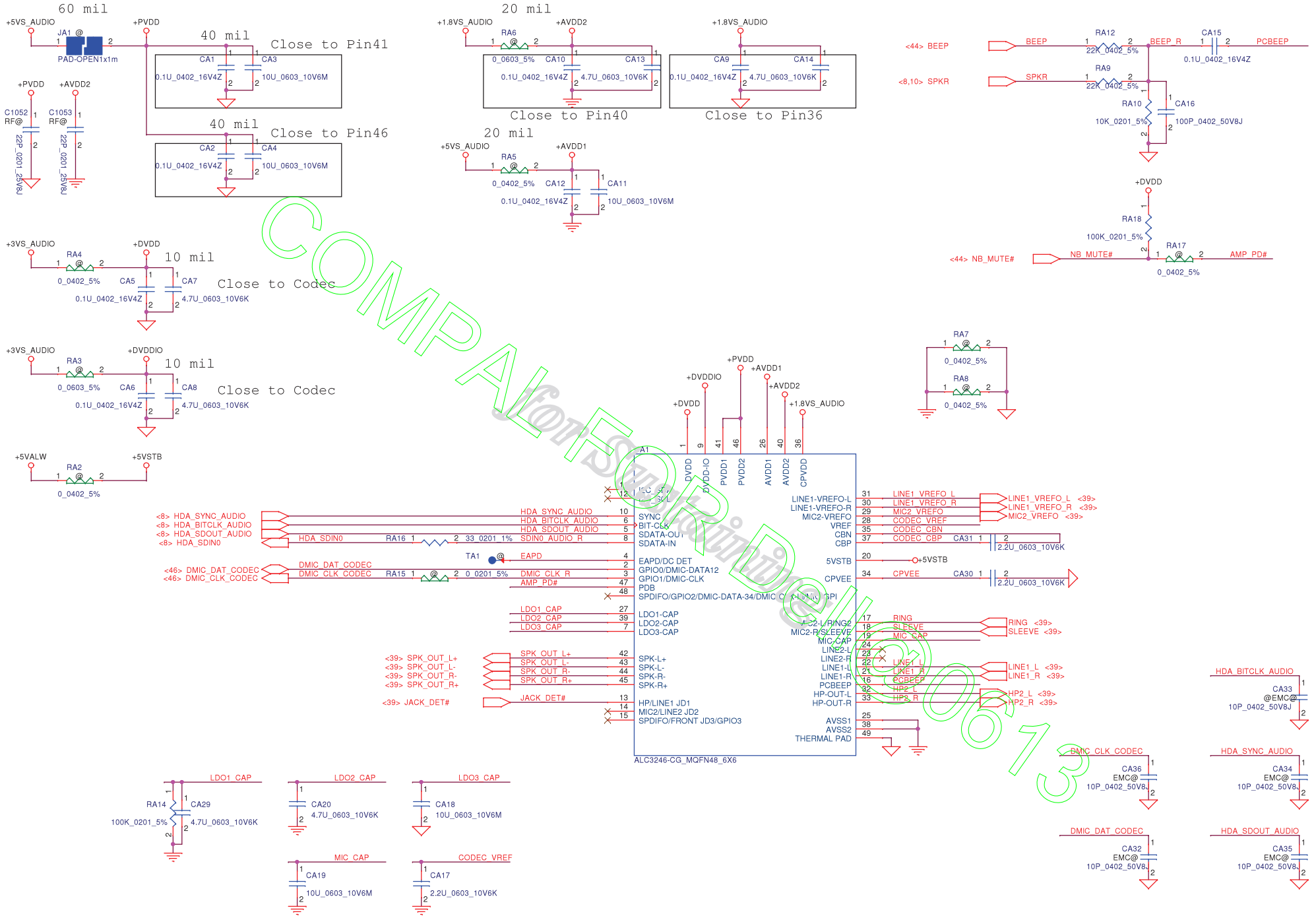
Size | Document Number: **LA-D311P** | Rev: 0.3

Date: Friday, December 25, 2015 | Sheet 36 of 61



Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: USB3.0 Type A			
Size	Document Number: LA-D311P		Rev: 0.3
Date: Friday, December 25, 2015	Sheet 37 of 61		



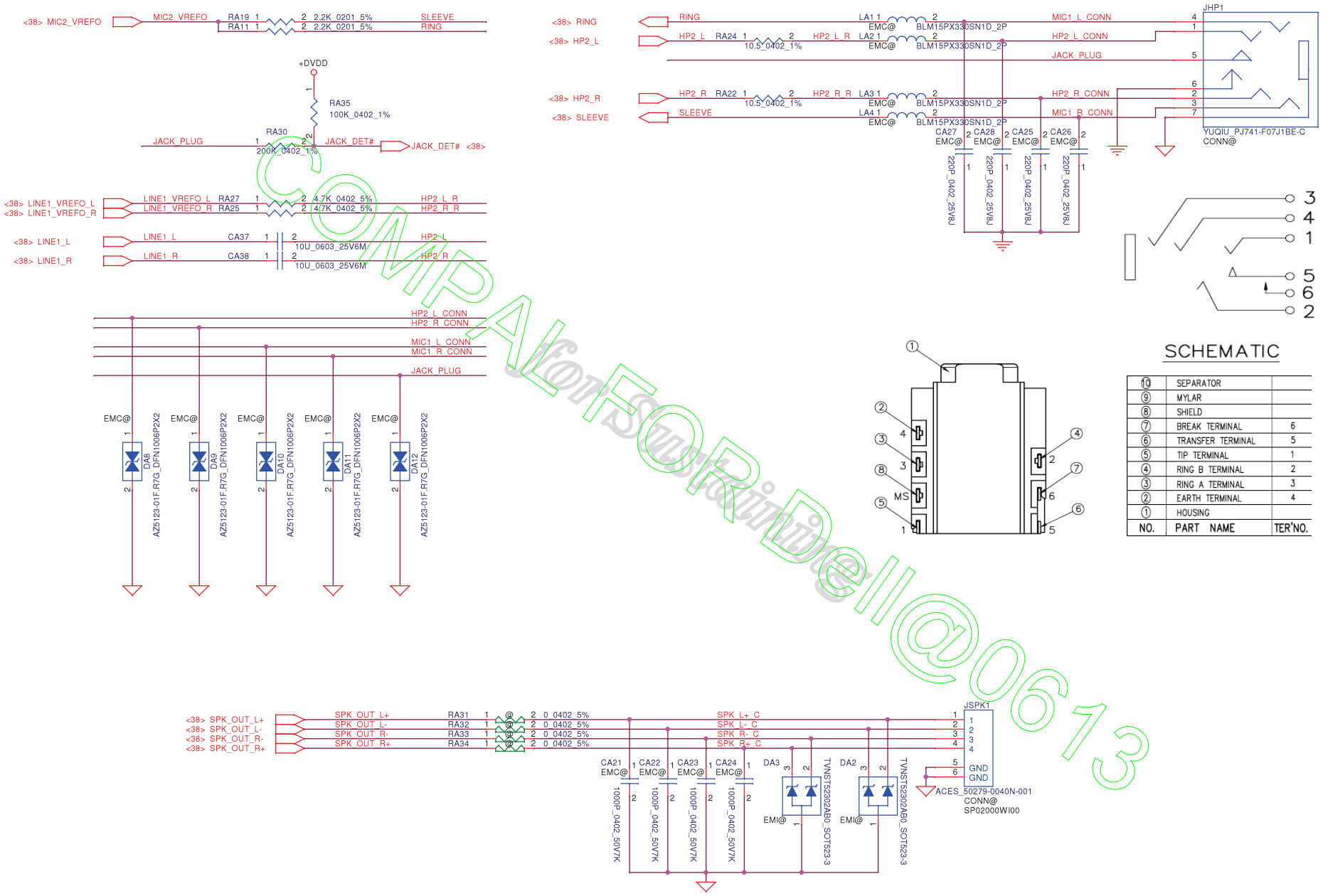
Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **Audio Codec3246**

Size | Document Number: **LA-D311P** | Rev: 0.3

Date: Friday, December 25, 2015 | Sheet 38 of 61



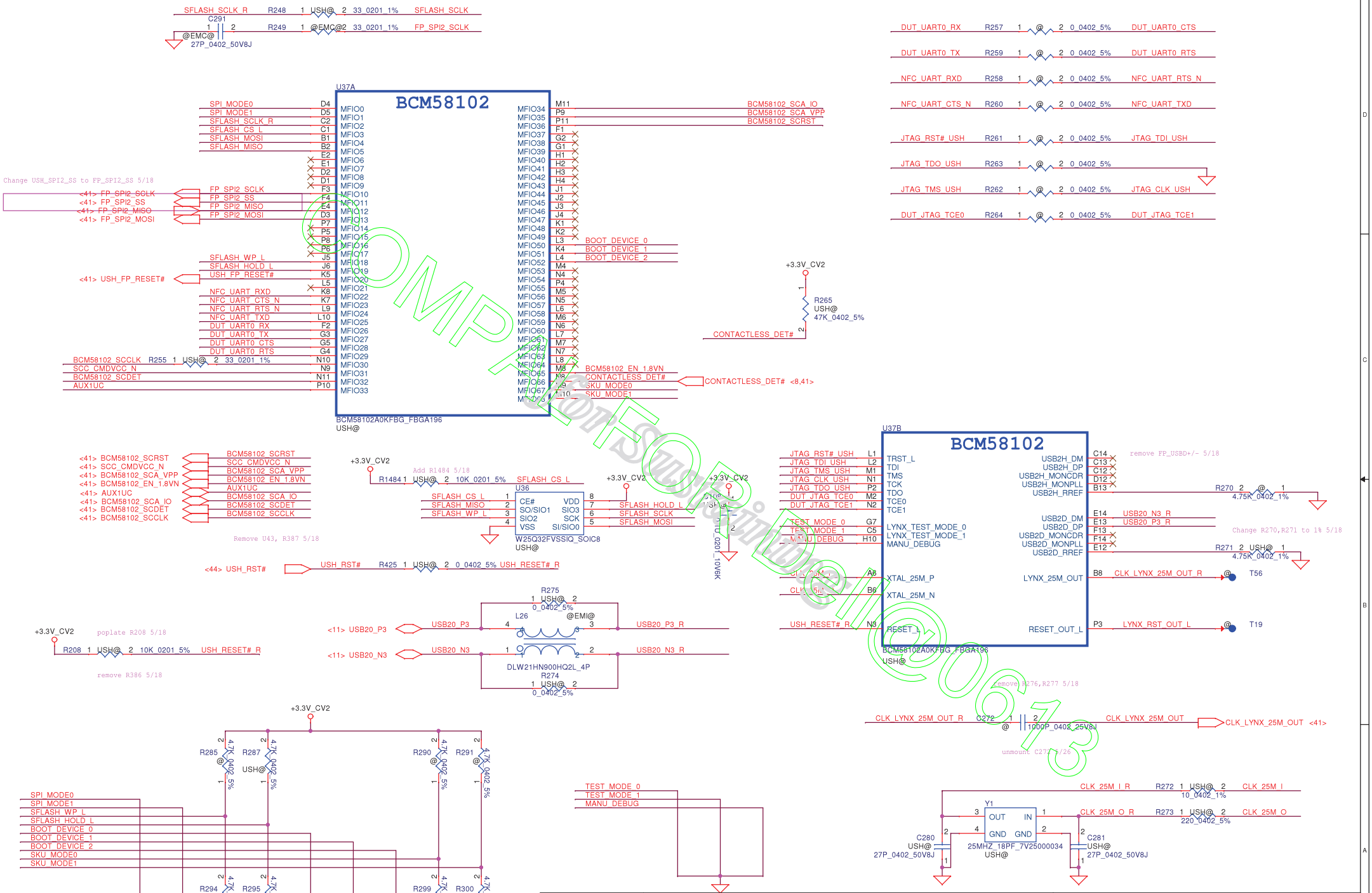
Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **Audio Jack/SPK**

Size | Document Number: **LA-D311P** | Rev: 0.3

Date: Friday, December 25, 2015 | Sheet 39 of 61



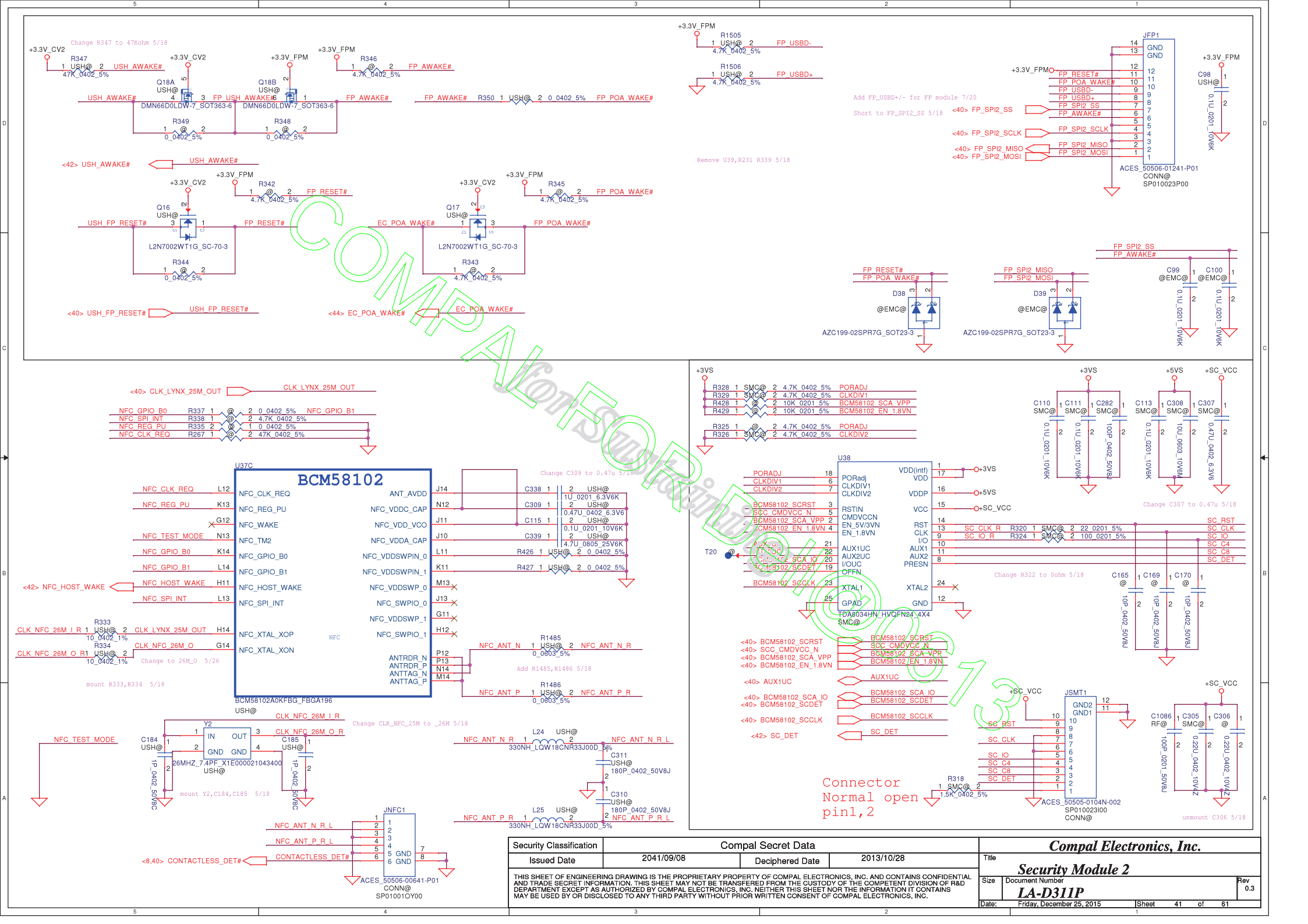
Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **Security Module 1**

Size	Document Number	Rev
	LA-D311P	0.3

Date: Friday, December 25, 2015 Sheet 40 of 61



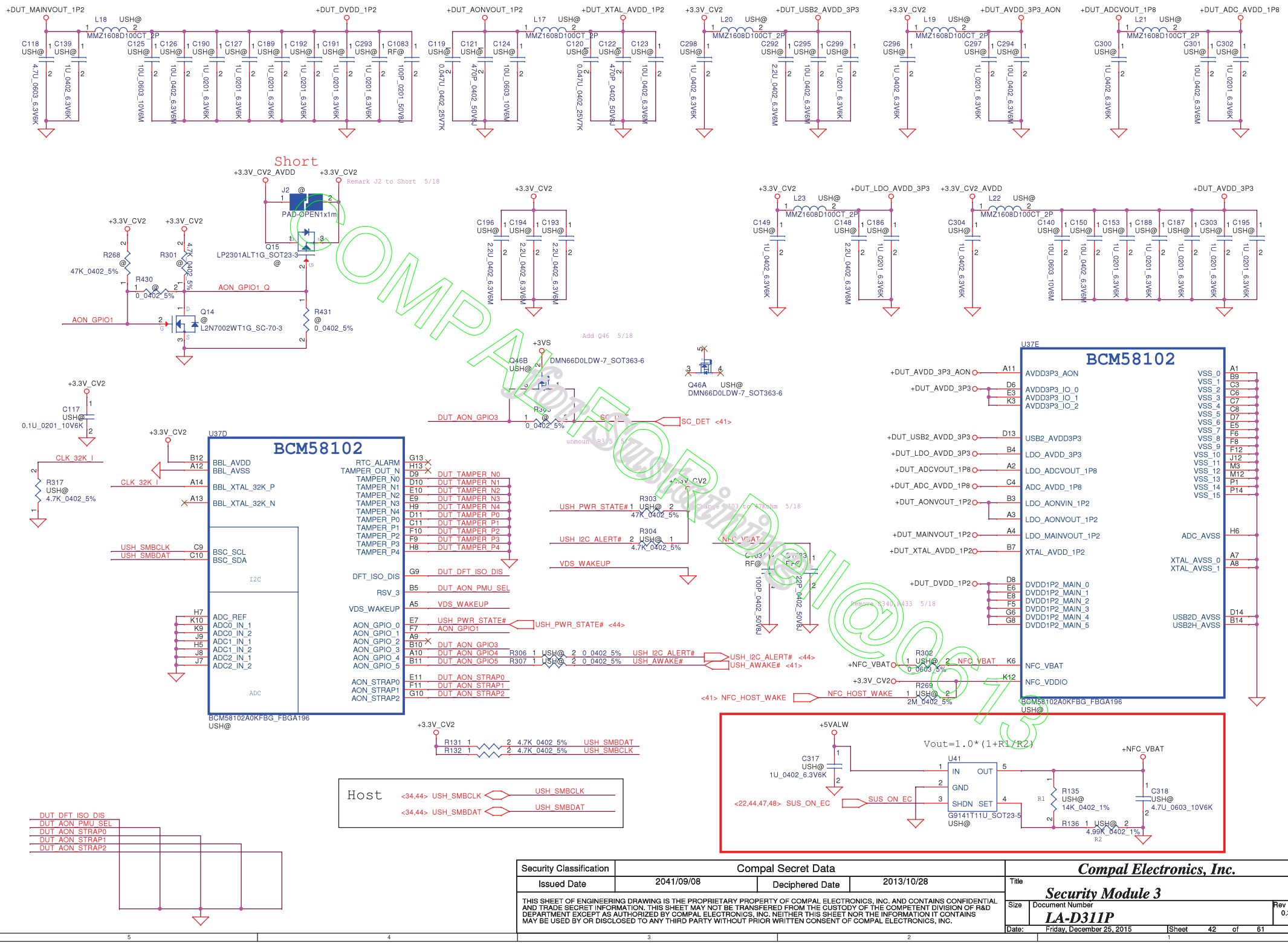
Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **Security Module 2**

Size	Document Number	Rev
	LA-D311P	0.3

Date: Friday, December 25, 2015 Sheet 41 of 61



Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

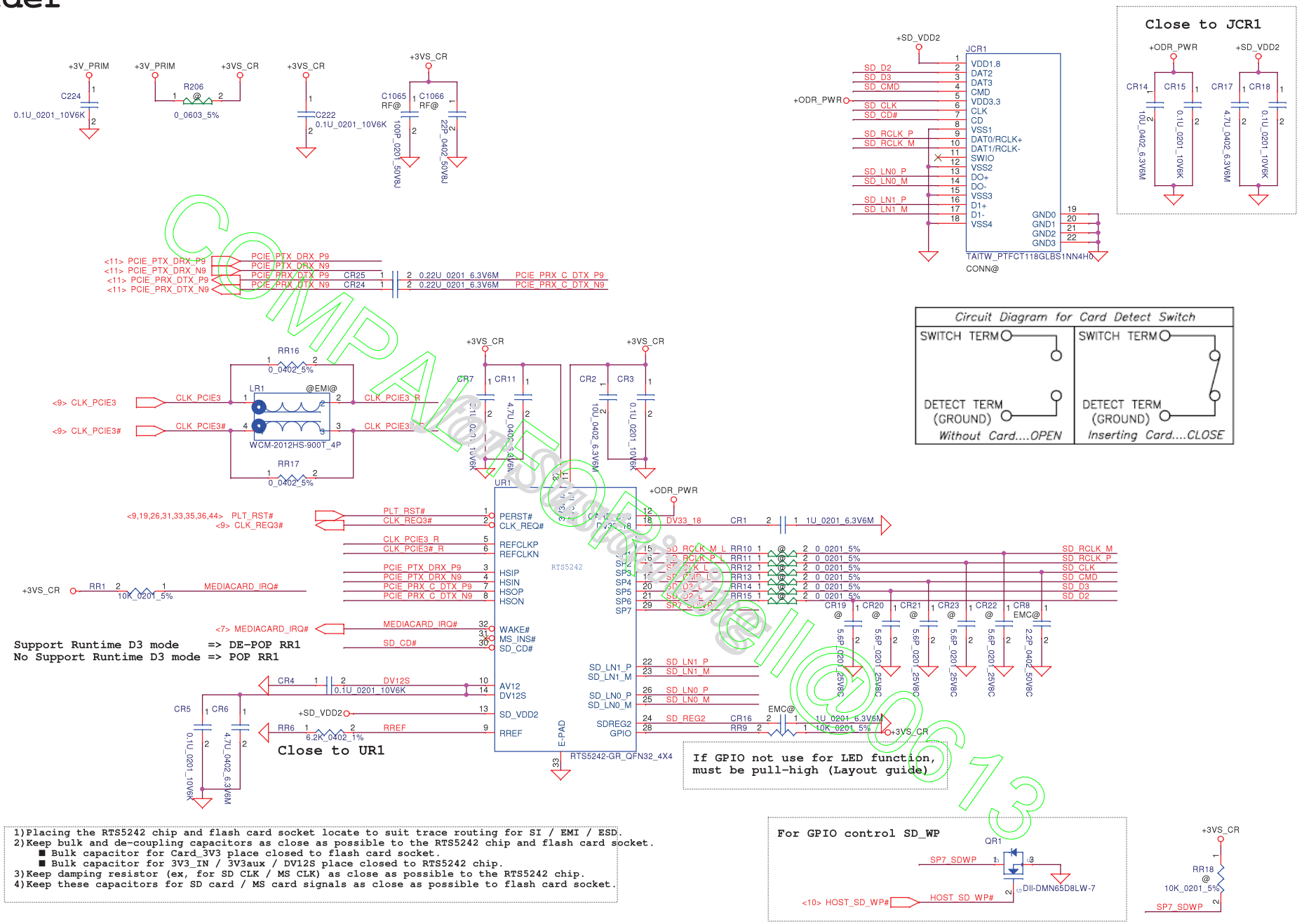
Compal Electronics, Inc.

Title: **Security Module 3**

Size | Document Number: **LA-D311P** | Rev: 0.3

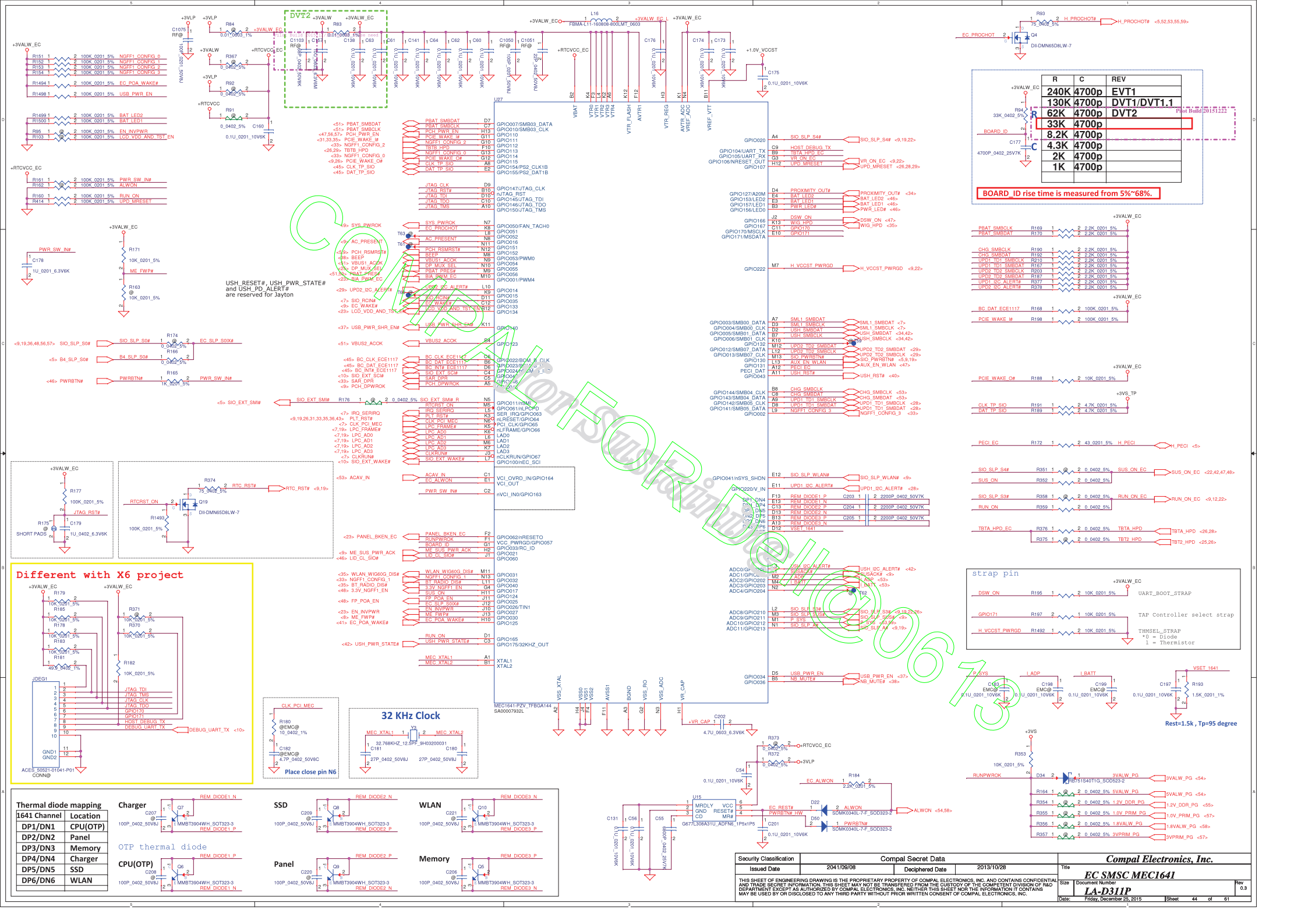
Date: Friday, December 25, 2015 | Sheet 42 of 61

Card Reader



Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.	
Title	Card Reader - RT5242
Size	Document Number: LA-D311P
Rev	0.3
Date:	Friday, December 25, 2015
Sheet	43 of 61



R	C	REV
240K	4700p	EVT1
130K	4700p	DVT1/DVT1.1
62K	4700p	DVT2
33K	4700p	
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

Thermal diode mapping	
1641 Channel	Location
DP1/DN1	CPU(OTP)
DP2/DN2	Panel
DP3/DN3	Memory
DP4/DN4	Charger
DP5/DN5	SSD
DP6/DN6	WLAN

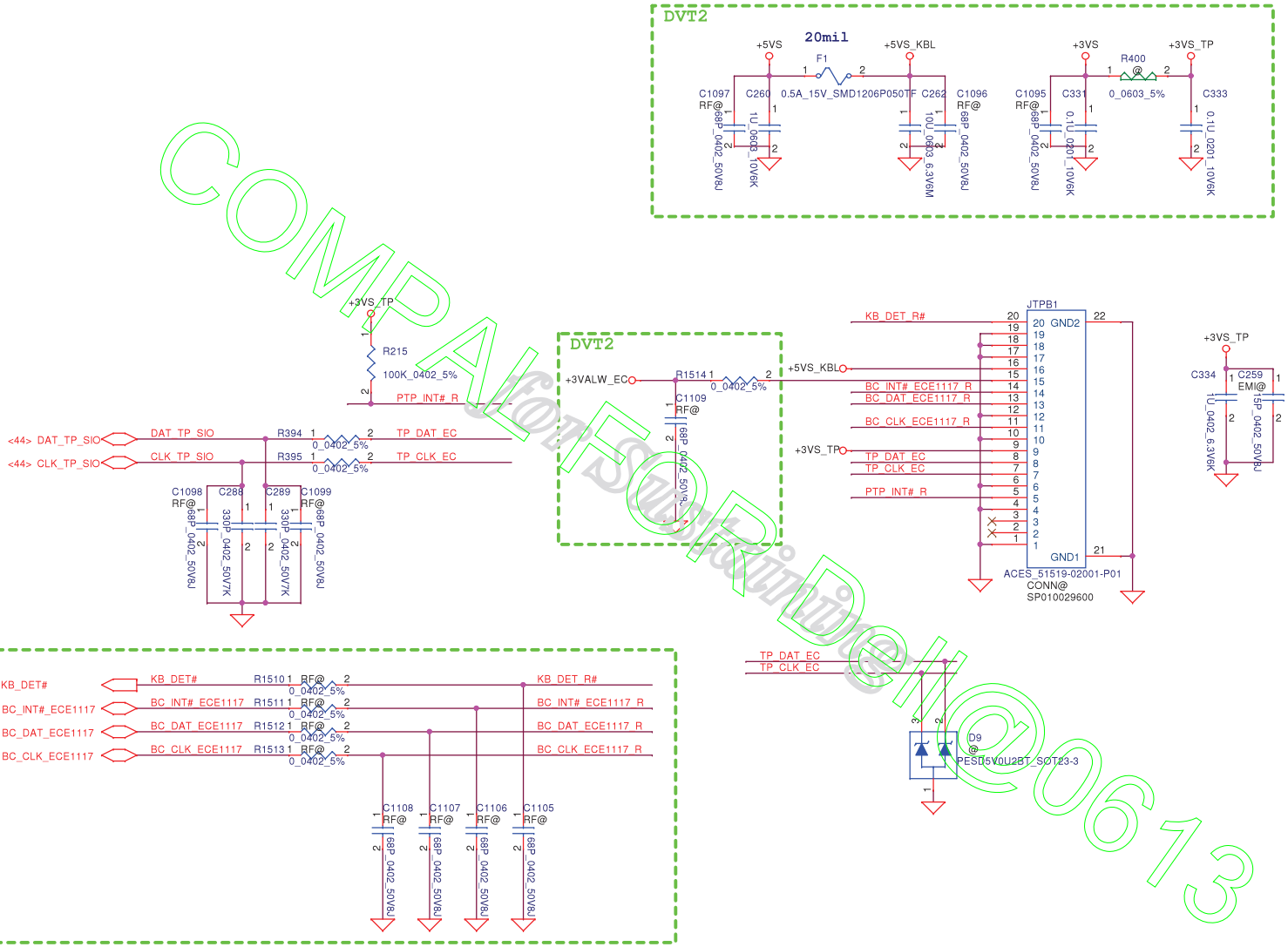
Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: EC SMSC MEC1641

Size: | Document Number: LA-D311P | Rev: 0.3

Date: Friday, December 25, 2015 | Sheet 44 of 61



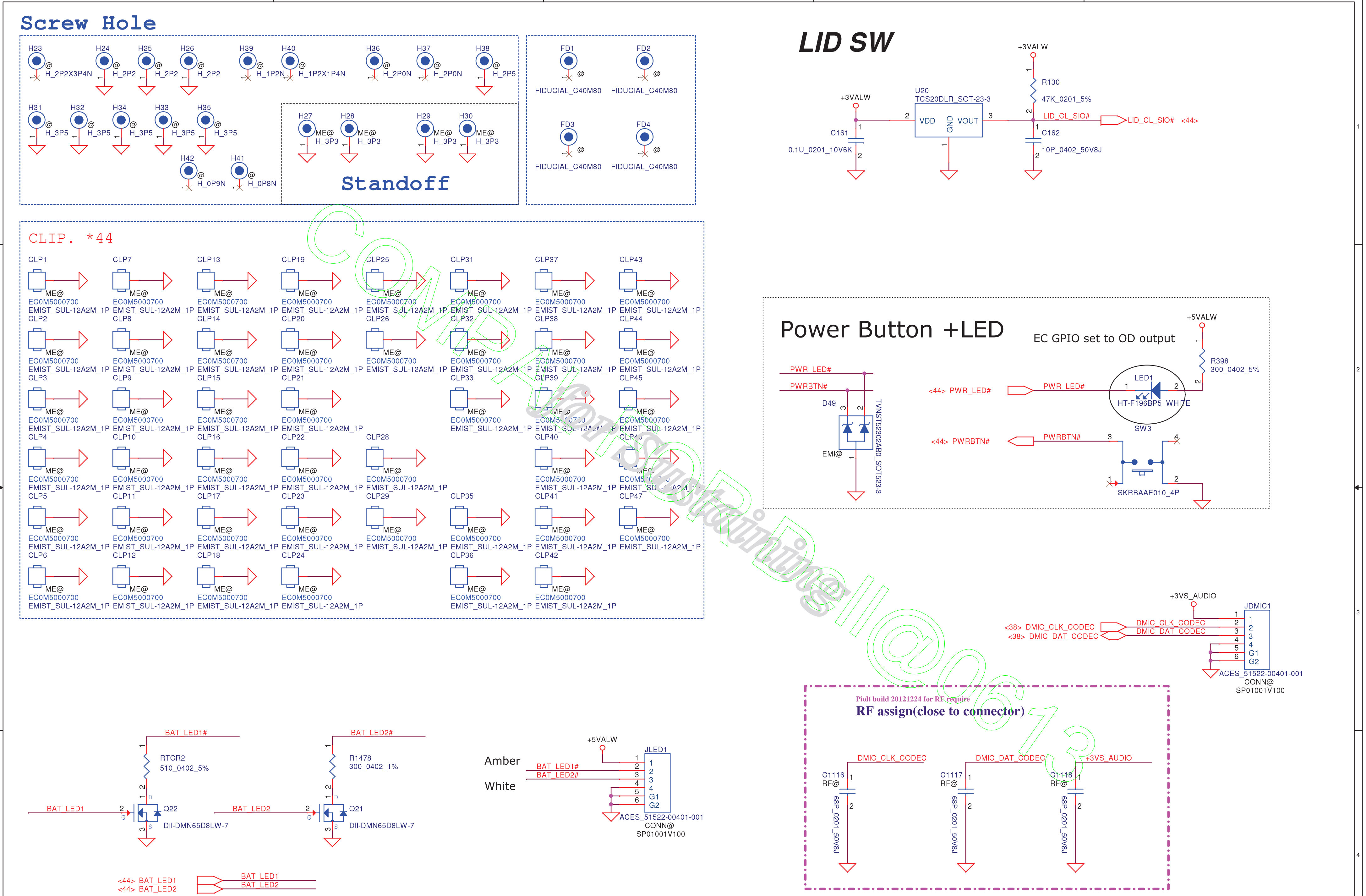
Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **TouchPAD**

Size | Document Number: **LA-D311P** | Rev: 0.3

Date: Friday, December 25, 2015 | Sheet 45 of 61


Screw Hole
H23 H_2P2X3P4N
H24 H_2P2
H25 H_2P2
H26 H_2P2
H39 H_1P2N
H40 H_1P2X1P4N
H36 H_2P0N
H37 H_2P0N
H38 H_2P5
H31 H_3P5
H32 H_3P5
H34 H_3P5
H33 H_3P5
H35 H_3P5
H42 H_0P9N
H41 H_0P8N
H27 ME@ H_3P3
H28 ME@ H_3P3
H29 ME@ H_3P3
H30 ME@ H_3P3
Standoff
FD1 FIDUCIAL_C40M80
FD2 FIDUCIAL_C40M80
FD3 FIDUCIAL_C40M80
FD4 FIDUCIAL_C40M80
LID SW
+3VALW
R130 47K_0201_5%
U20 TCS20DLR_SOT-23-3
VDD GND VOUT
C161 0.1U_0201_10V6K
C162 10P_0402_50V8J
LID_CL_SIO#
LID_CL_SIO# <44>
CLIP. *44
CLP1 CLP7 CLP13 CLP19 CLP25 CLP31 CLP37 CLP43
CLP2 CLP8 CLP14 CLP20 CLP26 CLP32 CLP38 CLP44
CLP3 CLP9 CLP15 CLP21 CLP33 CLP39 CLP45
CLP4 CLP10 CLP16 CLP22 CLP28 CLP40 CLP46
CLP5 CLP11 CLP17 CLP23 CLP29 CLP35 CLP41 CLP47
CLP6 CLP12 CLP18 CLP24 CLP36 CLP42
ME@
EC0M5000700
EMIST_SUL-12A2M_1P
Power Button +LED
EC GPIO set to OD output
+5VALW
R398 300_0402_5%
PWR_LED#
PWRBTN#
D49
EMI@
TVNST52302AB0_SOT523-3
<44> PWR_LED#
LED1 HT-F196BP5_WHITE
<44> PWRBTN#
SW3 SKRBAAE010_4P
+3VS_AUDIO
JDMIC1
<38> DMIC_CLK_CODEC
<38> DMIC_DAT_CODEC
DMIC_CLK_CODEC
DMIC_DAT_CODEC
1 2 3 4 5 6 G1 G2
ACES_51522-00401-001
CONN@
SP01001V100
Piolt build 20121224 for RF require
RF assign(close to connector)
DMIC_CLK_CODEC
DMIC_DAT_CODEC
+3VS_AUDIO
C1116 RF@ 68P_0201_50V8J
C1117 RF@ 68P_0201_50V8J
C1118 RF@ 68P_0201_50V8J
BAT_LED1#
RTCR2 510_0402_5%
BAT_LED1
Q22 DII-DMN65D8LW-7
BAT_LED2#
R1478 300_0402_1%
BAT_LED2
Q21 DII-DMN65D8LW-7
+5VALW
Amber
White
BAT_LED1#
BAT_LED2#
JLED1
ACES_51522-00401-001
CONN@
SP01001V100
<44> BAT_LED1
<44> BAT_LED2
BAT_LED1
BAT_LED2

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2041/09/08	Deciphered Date	2013/10/28	Title: LED/LID SW/SCREWH

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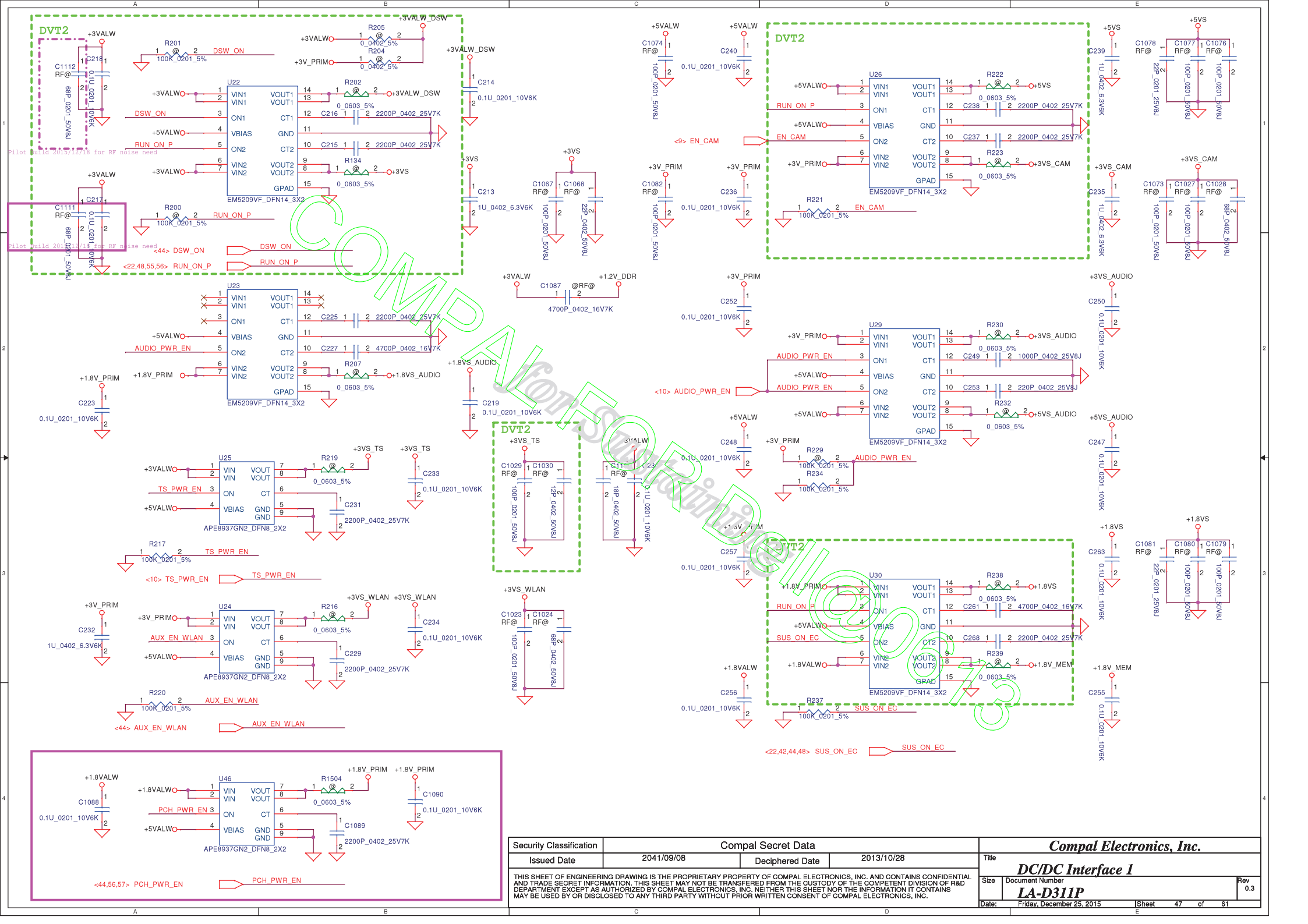
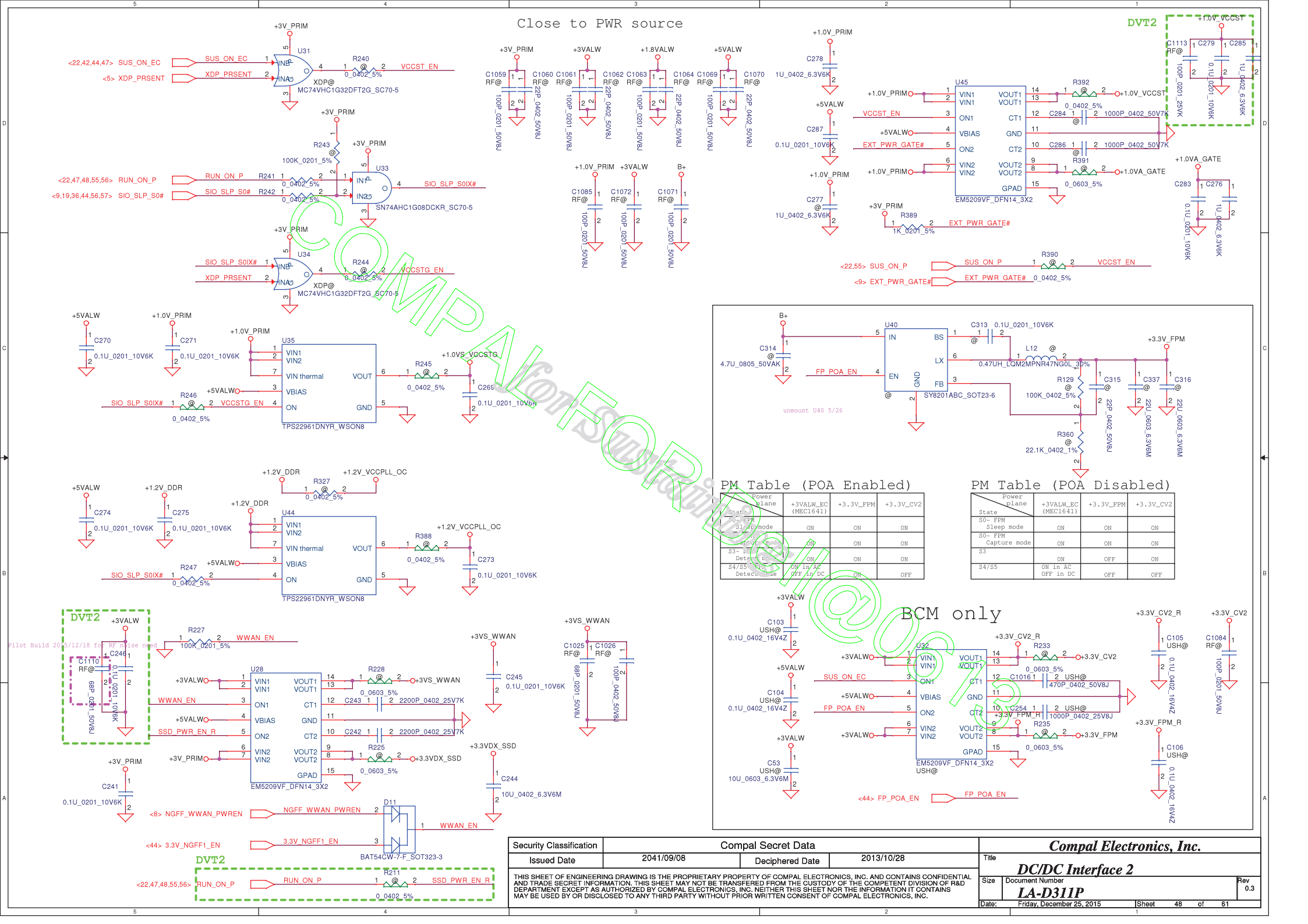
Date: Friday, December 25, 2015 | Sheet 46 of 61



Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: DC/DC Interface 1			
Size	Document Number: LA-D311P		Rev: 0.3
Date: Friday, December 25, 2015	Sheet 47 of 61		



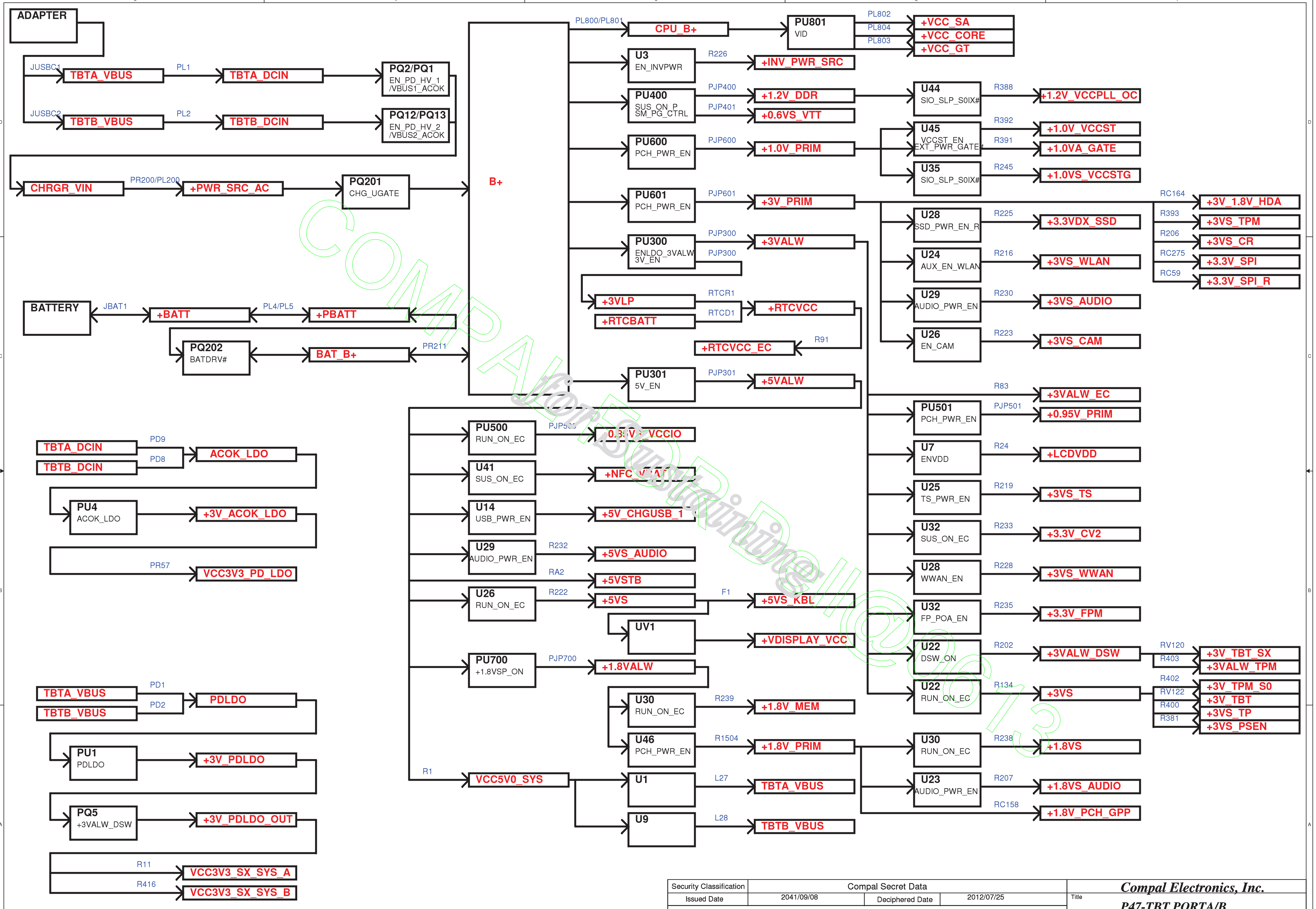
Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **DC/DC Interface 2**

Size: | Document Number: **LA-D311P** | Rev: 0.3

Date: Friday, December 25, 2015 | Sheet 48 of 61



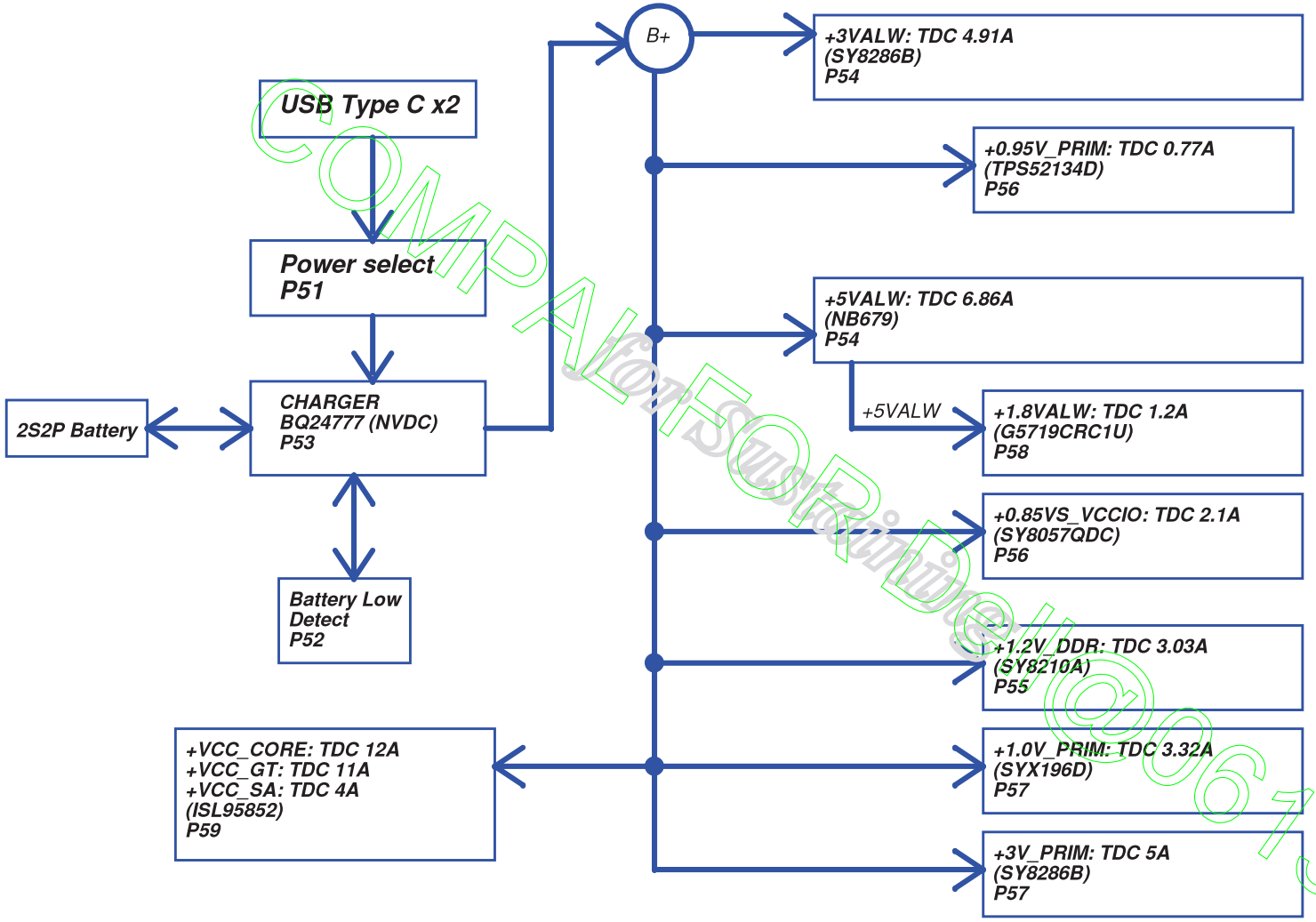
Security Classification	Compal Secret Data		
Issued Date	2041/09/08	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: ***P47-TBT PORTA/B***

Size: Custom | Document Number: *LA-D311P* | Rev: 0.3

Date: Friday, December 25, 2015 | Sheet 49 of 64



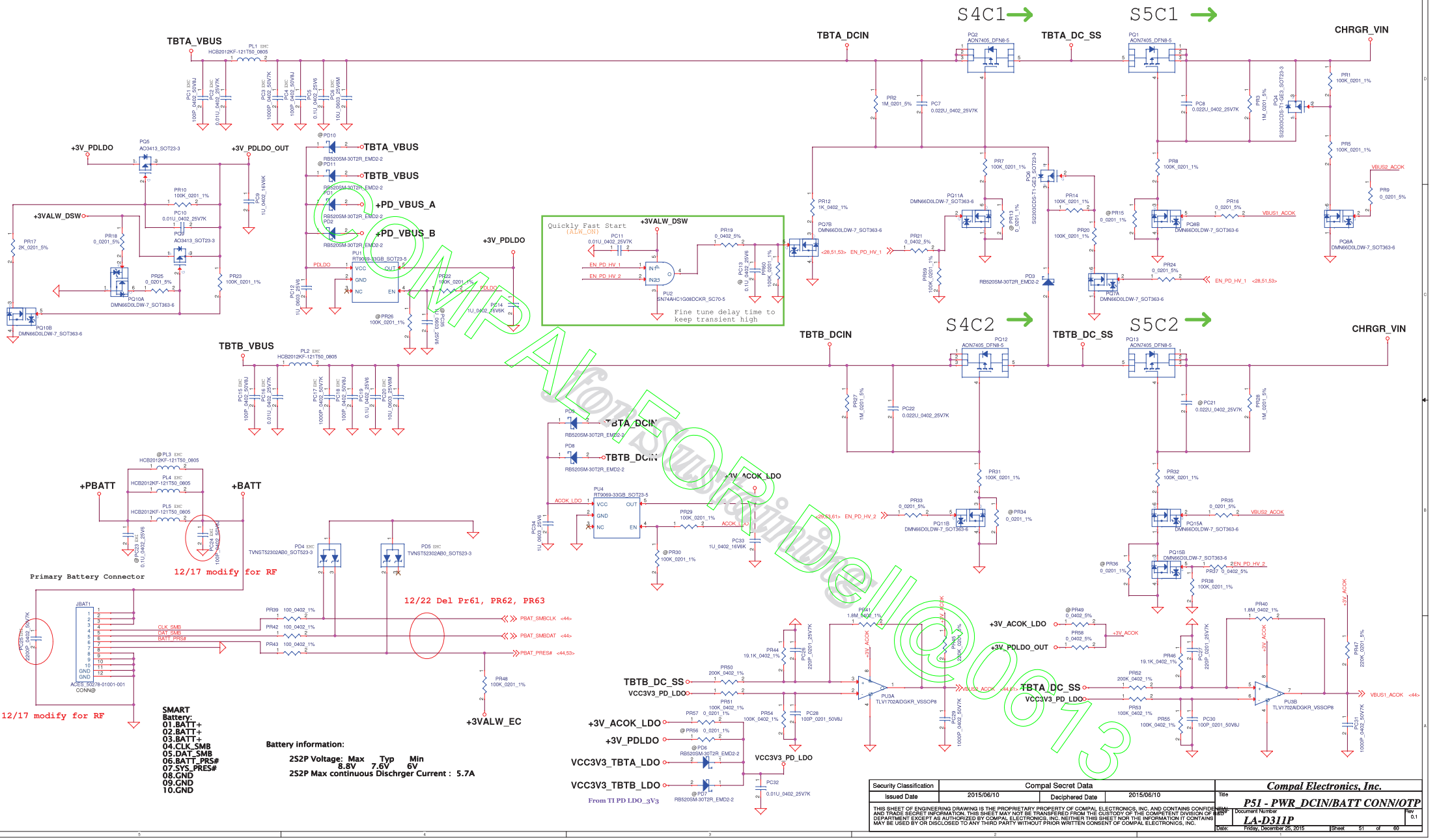
Security Classification	Compal Secret Data		
Issued Date	2015/06/10	Deciphered Date	2015/06/10

Compal Electronics, Inc.

Title: P50 - PWR_POWER BLOCK DIAGRAM

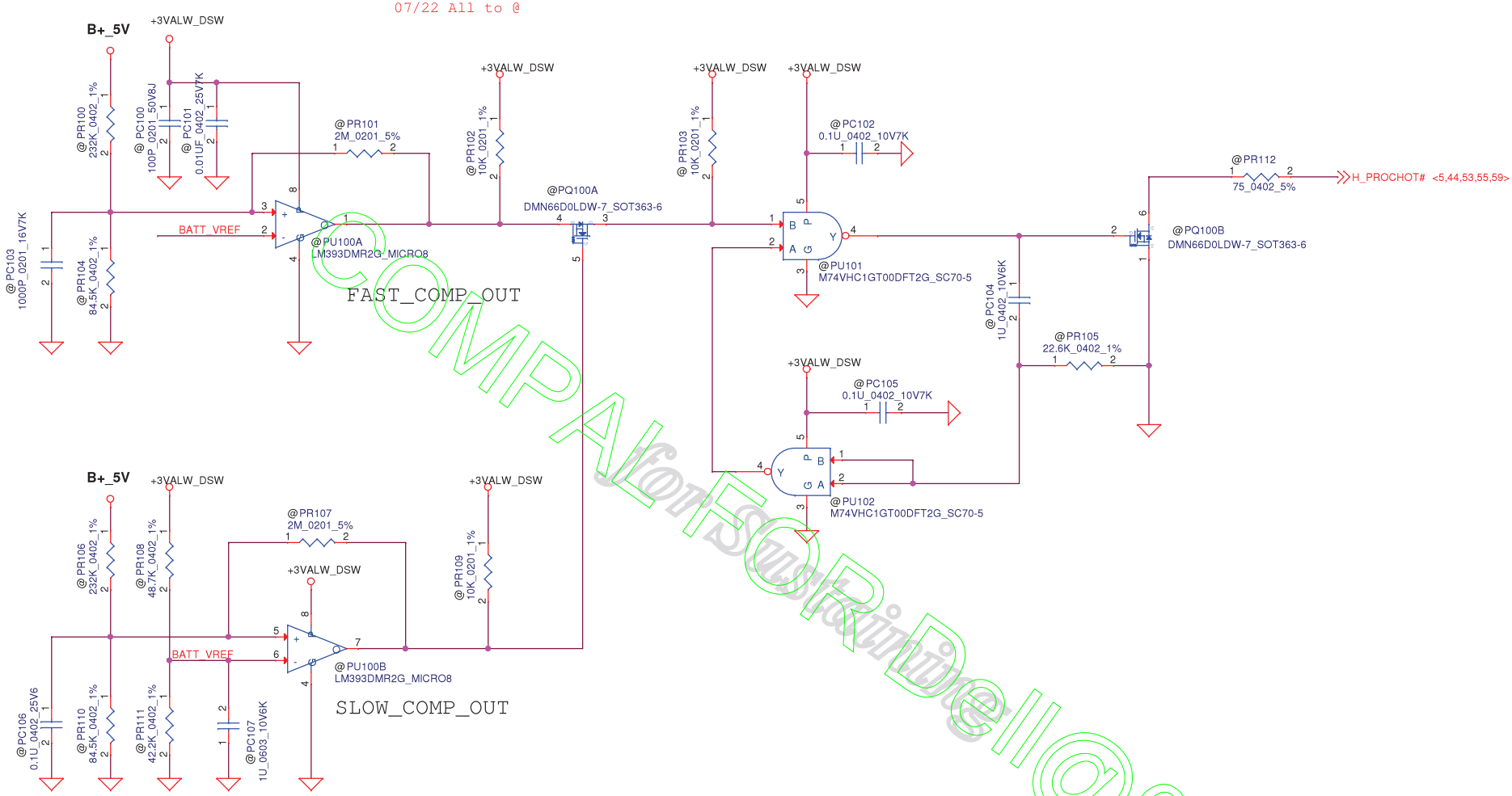
Size | Document Number: LA-D311P | Rev: 0.1

Date: Friday, December 25, 2015 | Sheet 50 of 60


S4C1
S5C1
S4C2
S5C2
TBTA_VBUS
TBTB_VBUS
TBTA_DCIN
TBTB_DCIN
TBTA_DC_SS
TBTB_DC_SS
CHRGR_VIN
+3V_PDLDO
+3V_PDLDO_OUT
+3VALW_DSW
+3VALW_EC
+PBATT
+BATT
+PD_VBUS_A
+PD_VBUS_B
+3V_ACOK_LDO
VCC3V3_PD_LDO
VCC3V3_TBTA_LDO
VCC3V3_TBTB_LDO
Quickly Fast Start
Fine tune delay time to keep transient high
Primary Battery Connector
12/17 modify for RF
12/22 Del Pr61, PR62, PR63
SMART Battery:
01.BATT+
02.BATT+
03.BATT+
04.CLK_SMB
05.DAT_SMB
06.BATT_PRS#
07.SYS_PRES#
08.GND
09.GND
10.GND
Battery information:
2S2P Voltage: Max Typ Min
8.8V 7.6V 6V
2S2P Max continuous Dischrger Current : 5.7A
From TI PD LDO_3V3
Security Classification
Compal Secret Data
Issued Date
2015/06/10
Deciphered Date
2015/06/10
Compal Electronics, Inc.
P51 - PWR_DCIN/BATT CONN/OTP
LA-D311P
Rev 0.1
Friday, December 25, 2015
Sheet 51 of 60

BATT low voltage detect

07/22 All to @



Security Classification	Compal Secret Data		
Issued Date	2015/06/10	Deciphered Date	2015/06/10

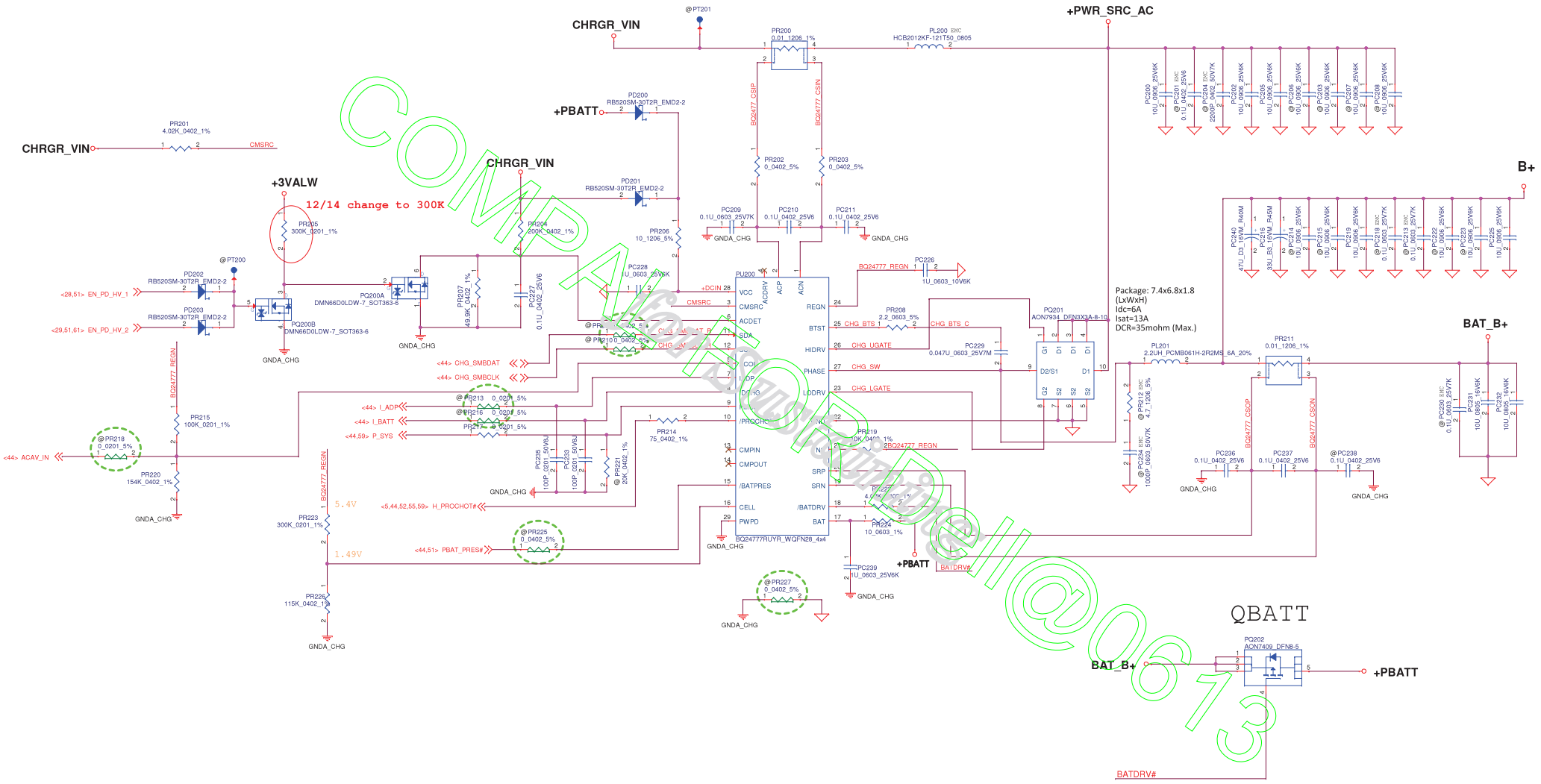
Compal Electronics, Inc.

Title: **P52 - PWR_DIS_BAT_PROCHOT#**

Size	Document Number	Rev
	LA-D311P	0.1

Date: Friday, December 25, 2015 | Sheet 52 of 60

Charger controller(40.1), Support component(40.2)



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/06/10	Deciphered Date 2015/06/10	Title: P53 - PWR_Charger_BQ24777
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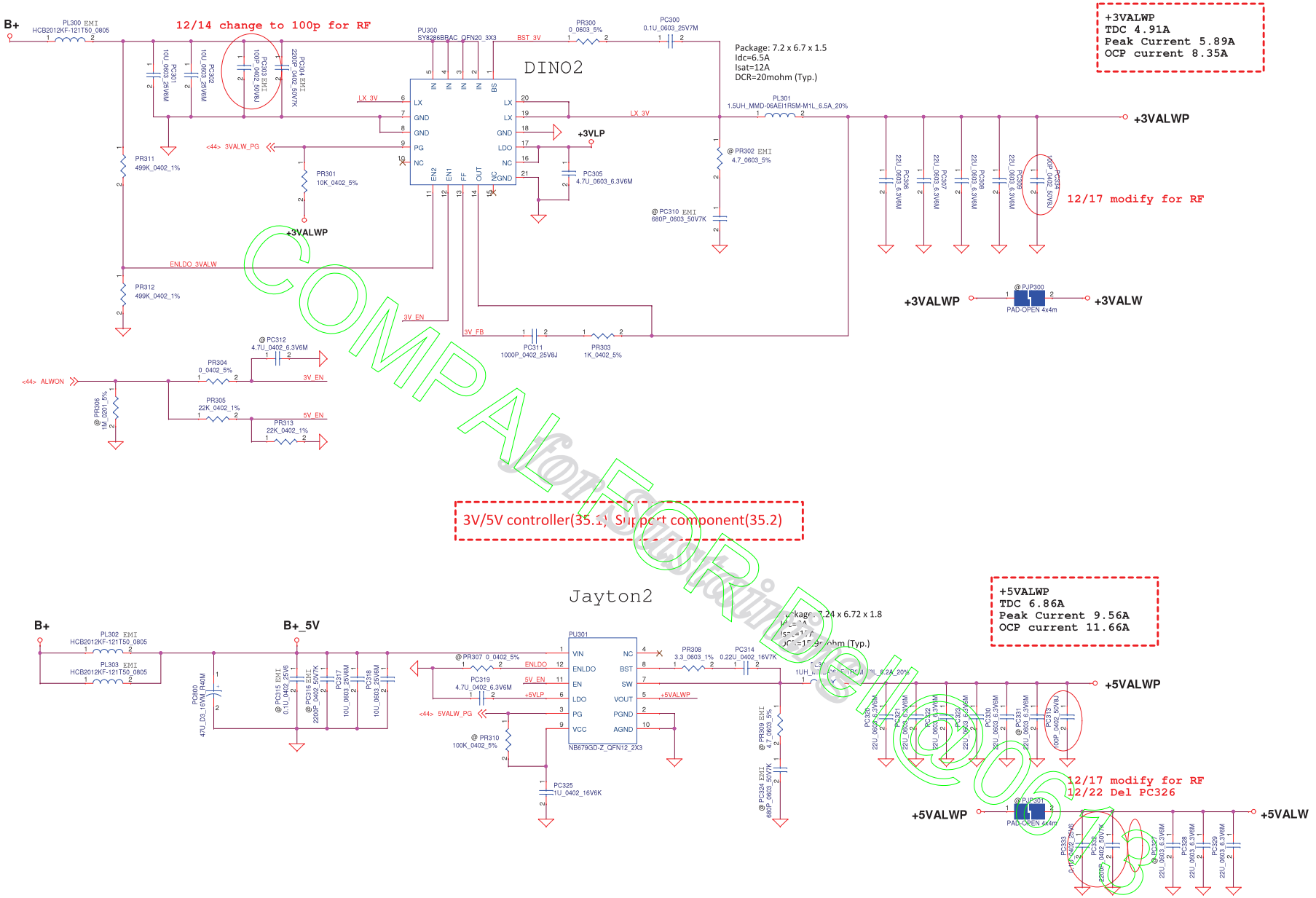
			Date: Friday, December 25, 2015 Sheet 53 of 60



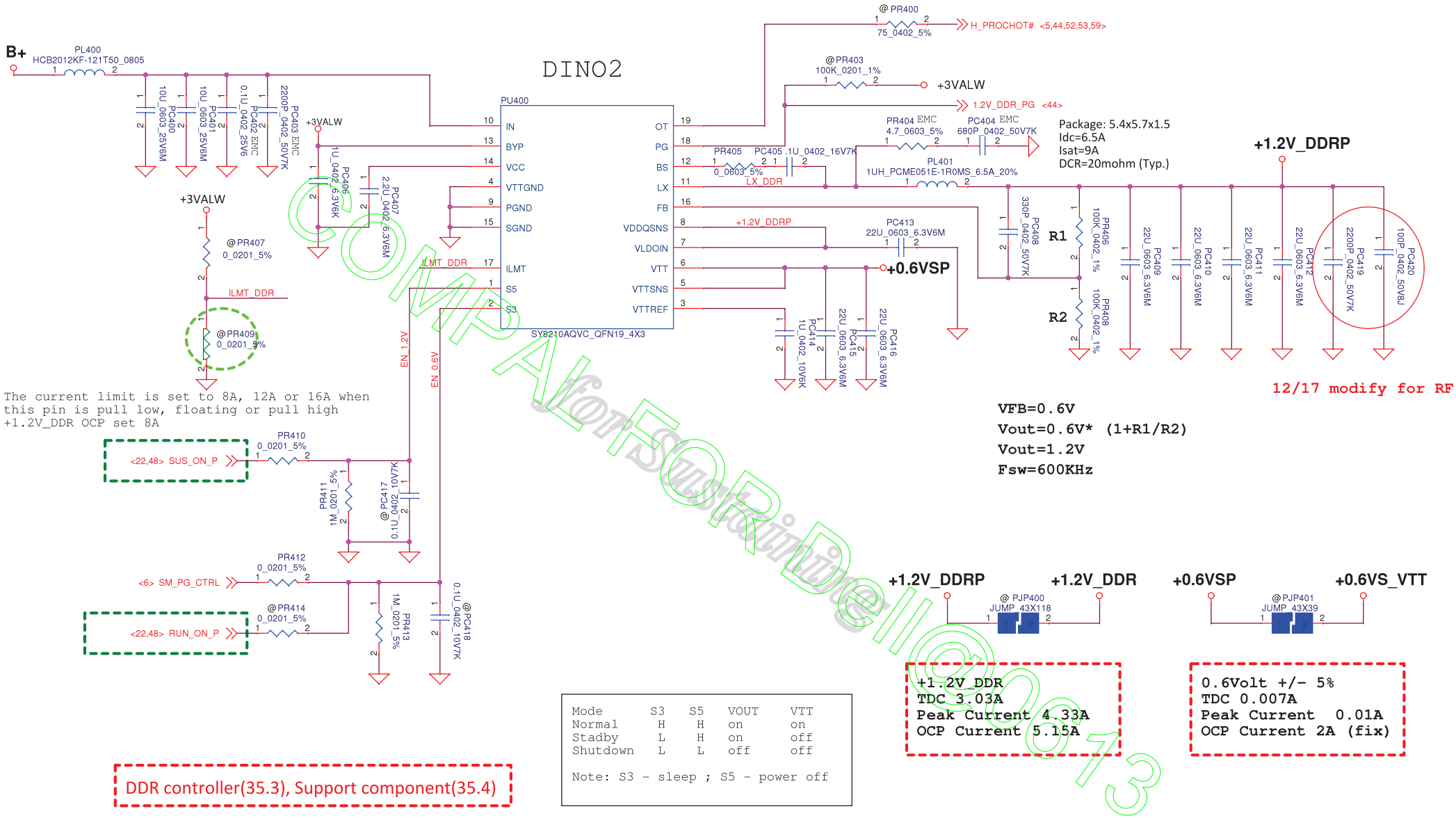
Security Classification	Compal Secret Data		
Issued Date	2015/06/10	Deciphered Date	2015/06/10

Compal Electronics, Inc.

Title: P54 - PWR-3VALWP/5VALWP

Size	Document Number	Rev
	LA-D311P	0.1

Date: Friday, December 25, 2015 | Sheet 54 of 60



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/06/10	Deciphered Date	2015/06/10

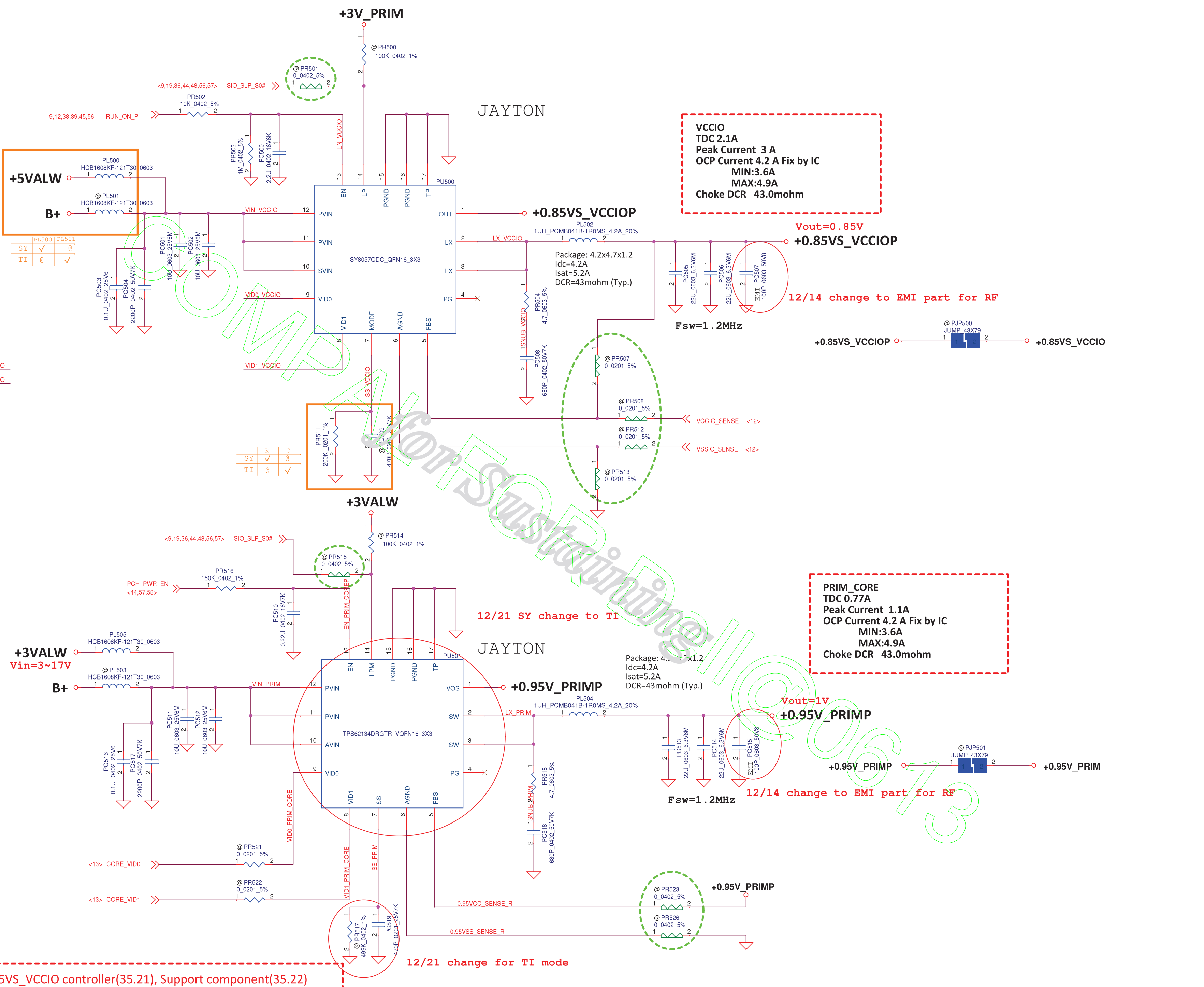
Title	P55 - PWR_+1.2V_DDR/0.6VS		
Size	Document Number		Rev
	LA-D311P		0.1
Date:	Friday, December 25, 2015	Sheet	55 of 60

SY8057 Rmode = 200k

LP	VID1	VID0	Vout(V)
0	X	X	0.000
1	0	0	0.850
1	0	1	0.875
1	1	0	0.950
1	1	1	0.975

TPS62134D

LP	VID1	VID0	Vout(V)
0	X	X	0.700
1	0	0	0.850
1	0	1	0.900
1	1	0	0.950
1	1	1	1.000



VCCIO
TDC 2.1A
Peak Current 3 A
OCP Current 4.2 A Fix by IC
MIN:3.6A
MAX:4.9A
Choke DCR 43.0mohm

PRIM_CORE
TDC 0.77A
Peak Current 1.1A
OCP Current 4.2 A Fix by IC
MIN:3.6A
MAX:4.9A
Choke DCR 43.0mohm

+0.85VS_VCCIO controller(35.21), Support component(35.22)
+0.95V_PRIM controller(35.23), Support component(35.24)

Security Classification	Compal Secret Data		
Issued Date	2015/06/10	Deciphered Date	2015/06/10

Compal Electronics, Inc.

Title: P56 - PWR_VCCIO/PRIM_CORE
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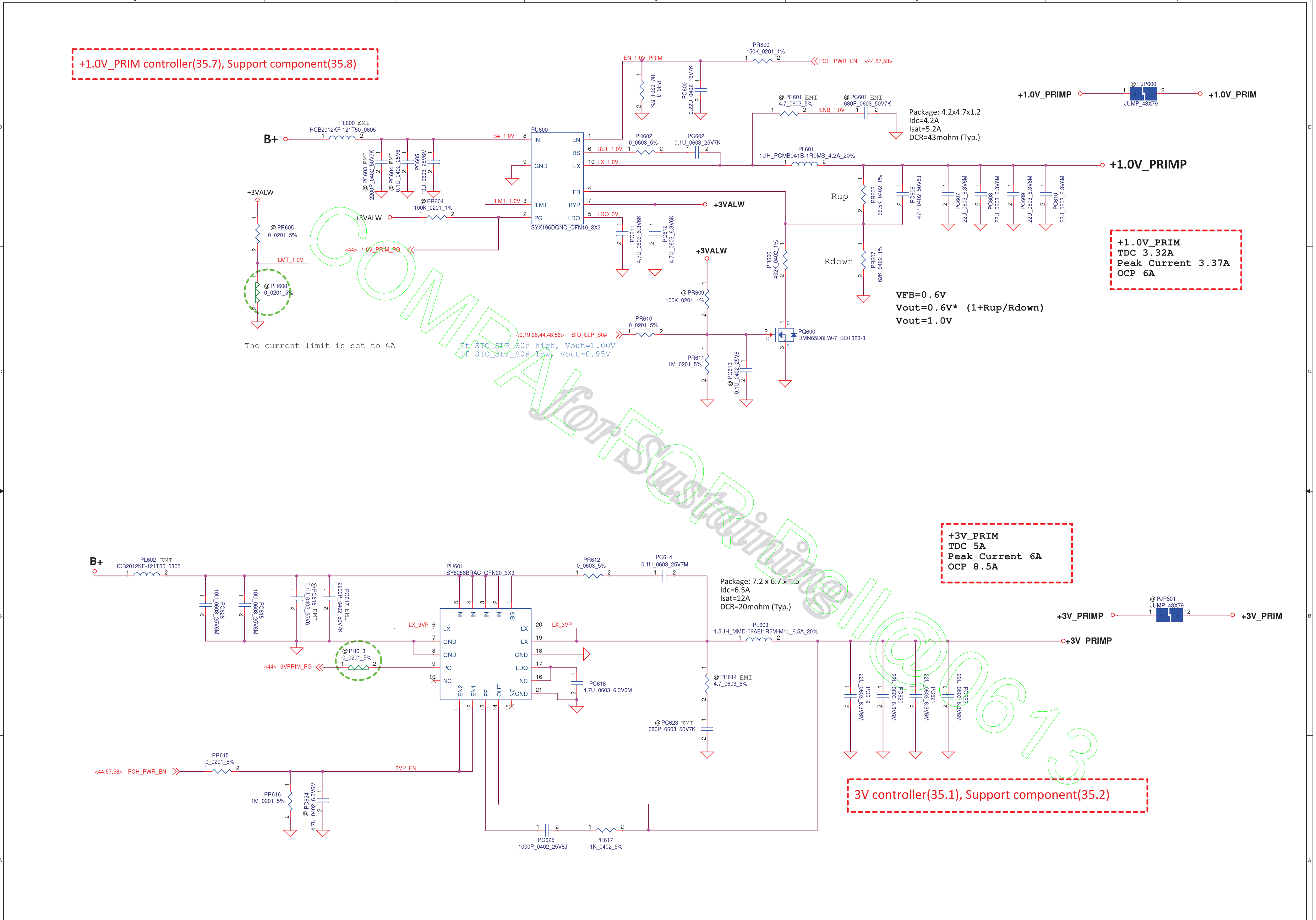


Security Classification	Compal Secret Data		
Issued Date	2015/06/10	Deciphered Date	2015/06/10

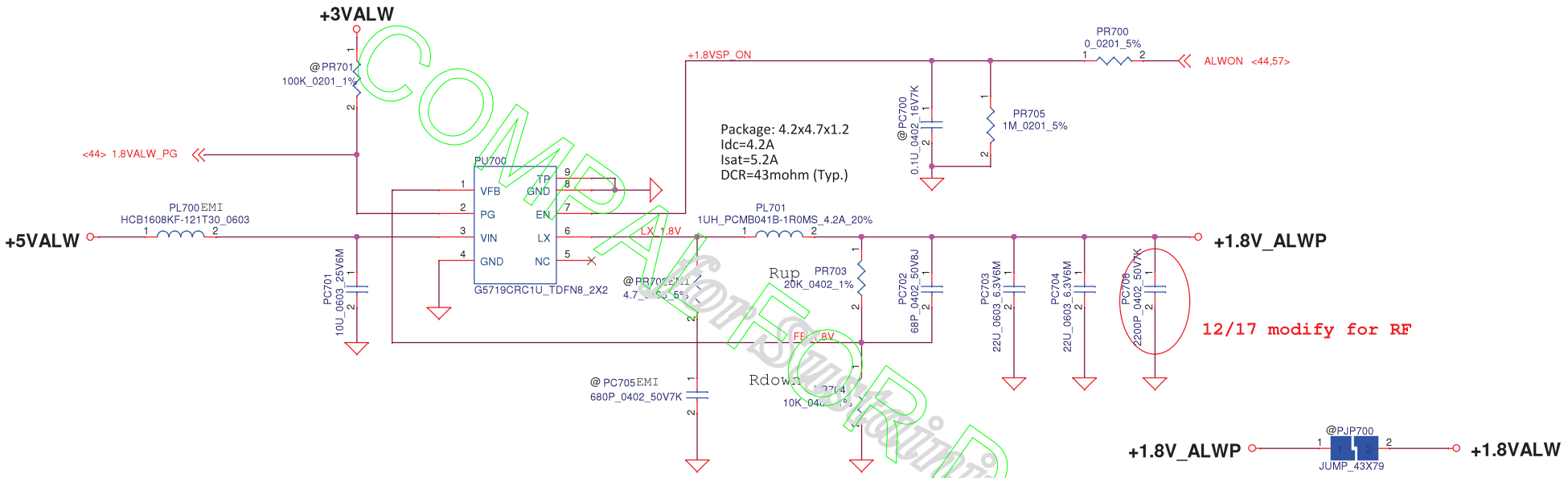
Compal Electronics, Inc.

Title: P57 - PWR_+1.0V_PRIM/+3V_PRIMP

Size | Document Number: LA-D311P | Rev 0.1

Date: Friday, December 25, 2015 |

1.8V controller(35.15), Support component(35.16)



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/06/10	Deciphered Date	2015/06/10

Title	P58 - PWR_+1.8V_ALW(SY8003)		
Size	Document Number		Rev
	LA-D311P		0.1
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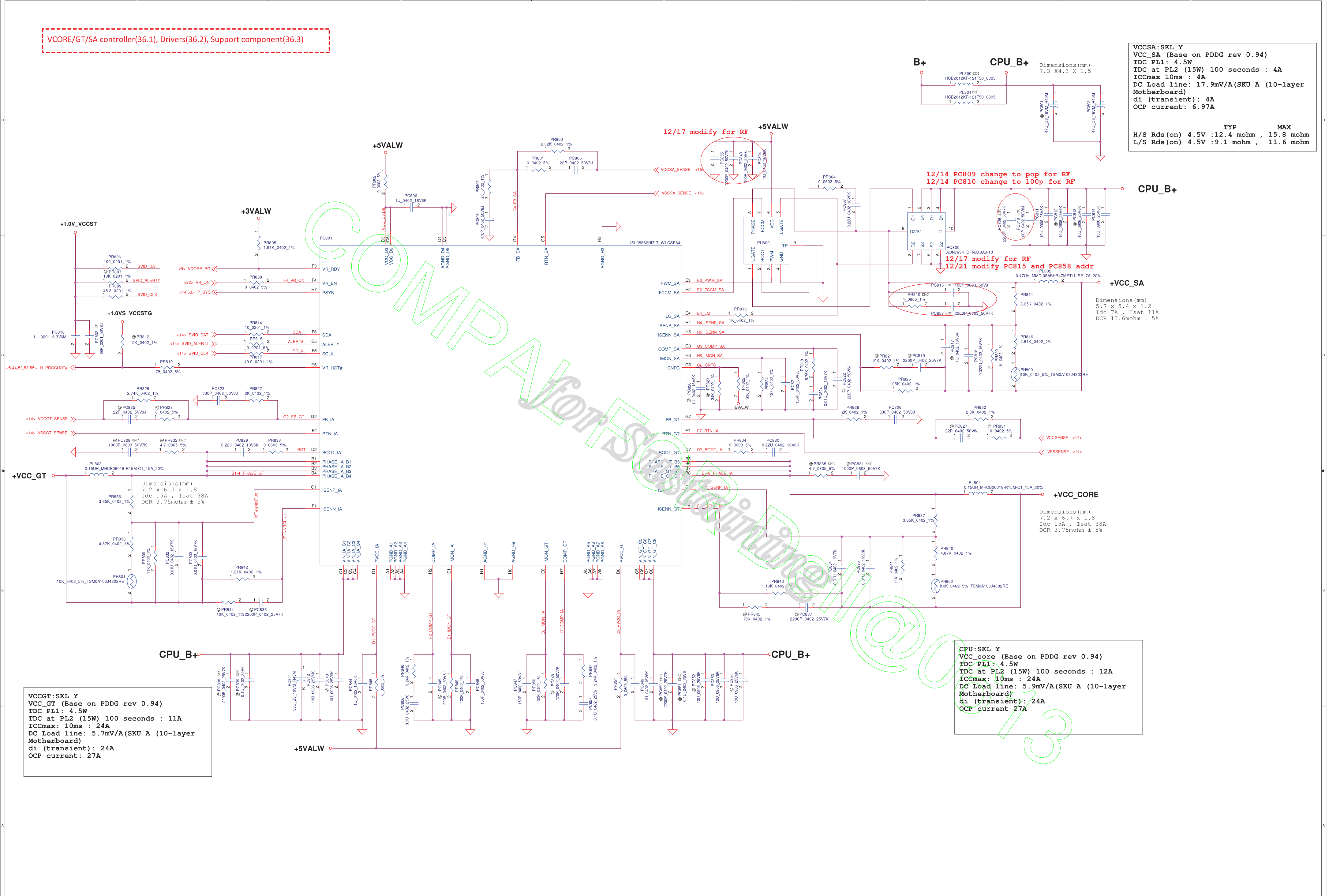

VCORE/GT/SA controller(36.1), Drivers(36.2), Support component(36.3)
VCCSA:SKL_Y
VCC_SA (Base on PDDG rev 0.94)
TDC PL1: 4.5W
TDC at PL2 (15W) 100 seconds : 4A
ICCmax 10ms : 4A
DC Load line: 17.9mV/A(SKU A (10-layer Motherboard)
di (transient): 4A
OCP current: 6.97A
TYP MAX
H/S Rds(on) 4.5V :12.4 mohm , 15.8 mohm
L/S Rds(on) 4.5V :9.1 mohm , 11.6 mohm
B+
CPU_B+
+5VALW
+3VALW
+1.0V_VCCST
+1.0VS_VCCSTG
12/17 modify for RF
12/14 PC809 change to pop for RF
12/14 PC810 change to 100p for RF
12/17 modify for RF
12/21 modify PC815 and PC858 addr
+VCC_SA
Dimensions(mm)
5.7 x 5.4 x 1.2
Idc 7A , Isat 11A
DCR 13.6mohm ± 5%
+VCC_GT
Dimensions(mm)
7.2 x 6.7 x 1.8
Idc 15A , Isat 38A
DCR 3.75mohm ± 5%
+VCC_CORE
Dimensions(mm)
7.2 x 6.7 x 1.8
Idc 15A , Isat 38A
DCR 3.75mohm ± 5%
ISL95852HIZ-T_WLCSP64
VCCGT:SKL_Y
VCC_GT (Base on PDDG rev 0.94)
TDC PL1: 4.5W
TDC at PL2 (15W) 100 seconds : 11A
ICCmax: 10ms : 24A
DC Load line: 5.7mV/A(SKU A (10-layer Motherboard)
di (transient): 24A
OCP current: 27A
CPU:SKL_Y
VCC_core (Base on PDDG rev 0.94)
TDC PL1: 4.5W
TDC at PL2 (15W) 100 seconds : 12A
ICCmax: 10ms : 24A
DC Load line: 5.9mV/A(SKU A (10-layer Motherboard)
di (transient): 24A
OCP current 27A

Security Classification	Compal Secret Data		
Issued Date	2015/06/10	Deciphered Date	2015/06/10

Compal Electronics, Inc.

Title: P59 - PWR_VCORE/SA/GT(ISL95852)

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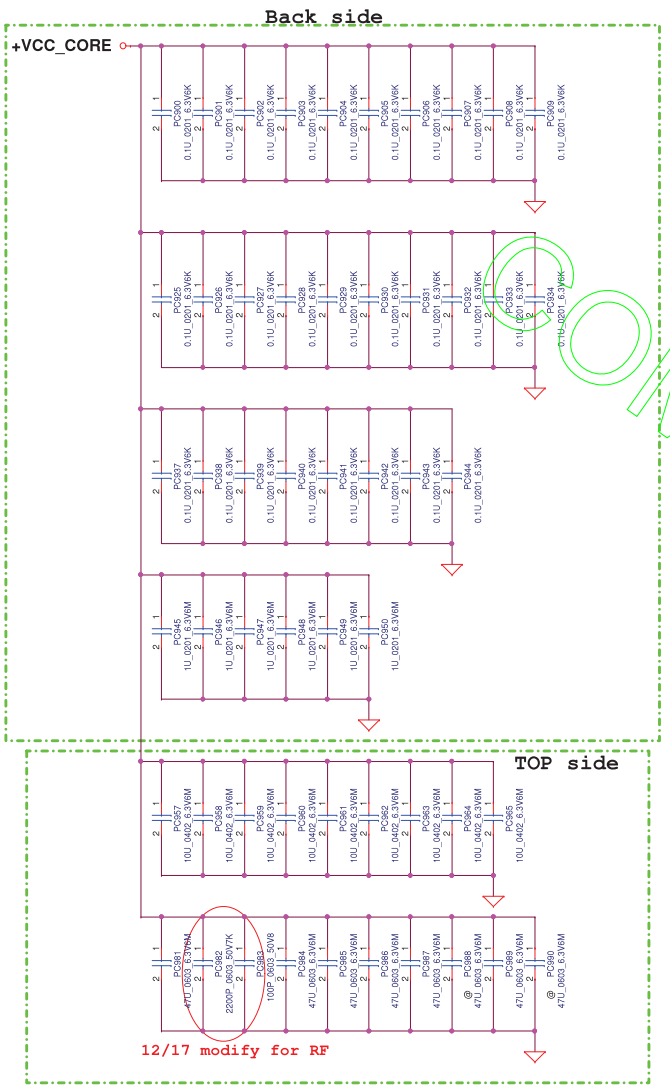
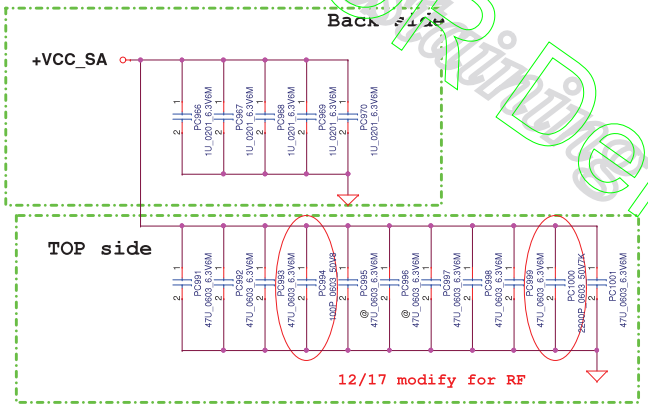
VCC_CORE
0.1U_0201 * 28 pcs +1U_0201*6 pcs+10U_0402*9pcs+47U_0603*10pcs



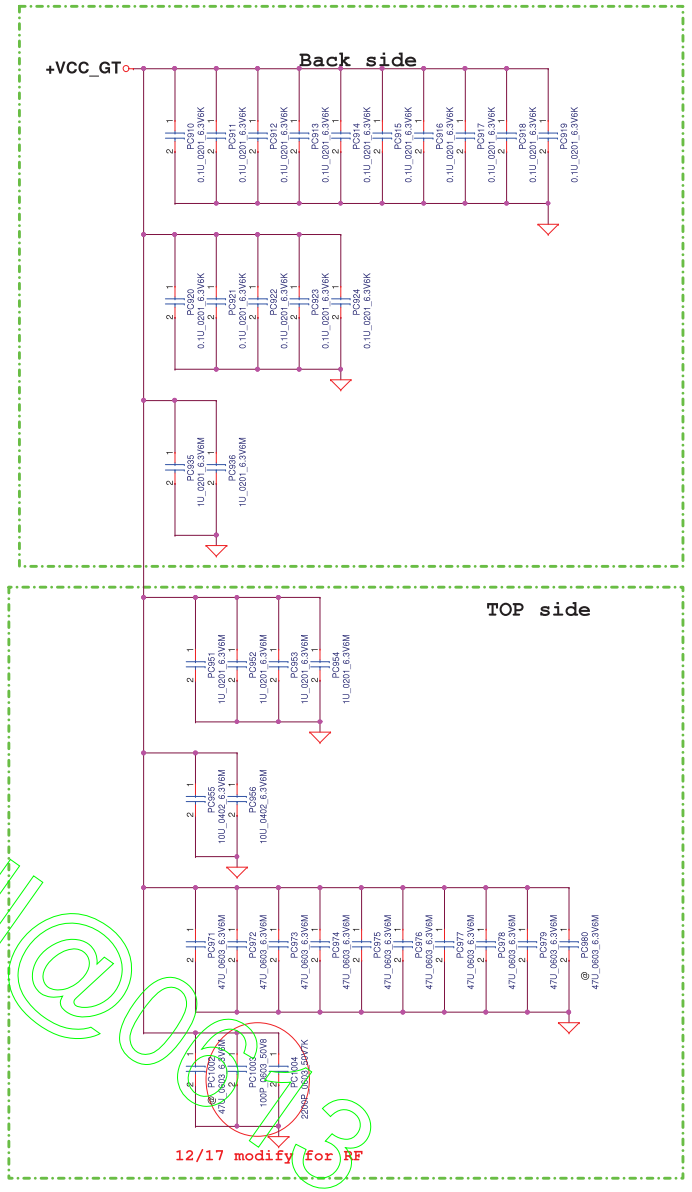
VCC_CORE output cap (36.4)

VCC_SA
1U_0201 * 5 pcs +47U_0603*1 pcs



VCC_SA output cap (36.6)

VCC_GT
0.1U_0201 * 15 pcs +1U_0201*6 pcs+1U_0402*4pcs+10U_0402*2pcs+47U_0603*13pcs



VCC_GT output cap (36.5)

Security Classification	Compal Secret Data		
Issued Date	2015/06/10	Deciphered Date	2015/06/10

Compal Electronics, Inc.

Title: P60 - Decoupling cap. for CPU power

Size	Document Number	Rev
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