G752VY Block Diagram

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Project Name	G752VY	Rev	2.0
Title :	Block Diagram		
Size	Custom	Dept.:	ASUSTeK COMPUTER INC.
Engineer:	Richard Liu		
Date:	Tuesday, July 21, 2015	Sheet	1 of 102

PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	RCIN#	Native	RC_IN#		PU 10K	+3VS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_KBCPCI_PCH_X1			
GPP_A10	CLKOUT_LPC1	Native	CLK_DEBUG_X1			
GPP_A11	PME#	Native	PCI_PME#			
GPP_A12	GPI	GPI	PCH_GPP_A12			
GPP_A13	SUSWANRN#	Native	ME_SusPwrDnAck		PU 10K	+3VSUS
GPP_A14	SUS_STAT#	Native	PCH_SUS_STAT#			
GPP_A15	SUS_ACK#	Native	PM_SUSACK#			
GPP_A16	Native/GPI	GPI	GPP_A16			
GPP_A17	GPI	GPI	PCH_GPP_A17			
GPP_A18	GPI	GPI	PCH_GPP_A18			
GPP_A19	GPI	GPI	PCH_GPP_A19			
GPP_A20	GPI	GPI	PCH_GPP_A20			
GPP_A21	GPI	GPI	PCH_GPP_A21			
GPP_A22	GPI	GPI	PCH_GPP_A22			
GPP_A23	GPI	GPI	PCH_GPP_A23			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	(N.C)			
GPP_B1	GPI	GPO	(N.C)			
GPP_B2	GPI	GPI	(N.C)			
GPP_B3	GPI	GPI	(N.C)			
GPP_B4	GPI	GPI	(N.C)			
GPP_B5	GPI	Native	CLK_PEGA_REQ0#_X1		PU 10K	+3VSUS
GPP_B6	GPI	Native	CLK_REQ1#		PU 10K	+3VSUS
GPP_B7	GPI	Native	CLK_REQ2#		PU 10K	+3VSUS
GPP_B8	GPI	Native	CLKREQ3_WLAN#_X1		PU 10K	+3VSUS
GPP_B9	GPI	Native	CLKREQ4_WLAN#_X1		PU 10K	+3VSUS
GPP_B10	GPI	Native	CLKREQ5_WLAN#_X1		PU 10K	+3VSUS
GPP_B11	GPO	GPO	MPHY_PWREN			+3VSUS
GPP_B12	SLP_S0#	Native	SLP_S0#			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPPB14	PD	PD 10K(@)	
GPP_B15	GPI		GSPI0_CS#			
GPP_B16	GPI		GSPI0_CLK			
GPP_B17	GPI		GSPI0_MISO			
GPP_B18	GPO	Strap	PCH_GPPB18	PD	PD 10K(@)	
GPP_B19	GPI	GPO	PCH_GPPB19/BT_ON_PCH			
GPP_B20	GPI	GPO	PCH_GPPB20/NV_GPU_EVENT#		PU 10K	+3VS
GPP_B21	GPI	GPI	PCH_GPPB21/DGPU_FB_CLAMP_FB_EN		PD 10K	
GPP_B22	GPO	Strap	PCH_GPPB22	PD		
GPP_B23	GPO	GPO	PCH_GPPB23/SML1ALERT#	PD	PU 150K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		PU 2.2K	+3VSUS
GPP_C2	GPO	Strap	CPAD_INT	PD	PU 10K(@)	+3VS
GPP_C3	SML0CLK	Native	SML0_CLK		PU 2.2K	+3VSUS
GPP_C4	SML0DATA	Native	SML0_DAT		PU 2.2K	+3VSUS
GPP_C5	GPO	Strap	PCH_GPPC5	PD		+3VSUS
GPP_C6	GPI	Native	SML1_CLK		PU 2.2K	+3VSUS
GPP_C7	GPI	Native	SML1_DAT		PU 2.2K	+3VSUS
GPP_C8	GPI	GPI	PCH_GPPC8			
GPP_C9	GPI	GPI	PCH_GPPC9			
GPP_C10	GPI	GPI	PCH_GPPC10			
GPP_C11	GPI	GPI	PCH_GPPC11			
GPP_C12	GPI	GPI	DIMM_SEL0		PD 10K	
GPP_C13	GPI	GPI	DIMM_SEL1		PD 10K	
GPP_C14	GPI	GPI	DIMM_SEL2		PD 10K	
GPP_C15	GPI	GPI	NFC_ID			
GPP_C16	GPI	GPO	AOAC_WLANLED		PU 10K(@)	+3VSUS
GPP_C17	GPI	GPO	PCH_GPPC17		PU 10K(@)	+3VS
GPP_C18	GPI	GPO	PCH_GPPC18/I2C1_SDA		PU 4.7K	+3VS
GPP_C19	GPI	GPO	PCH_GPPC19/I2C1_SCL		PU 4.7K	+3VS
GPP_C20	GPI	GPI	PCH_GPPC20/DGPU_PWROK		PU 2.2K	+3V3_AON
GPP_C21	GPI	GPO	PCH_GPPC21/GPU_RST#		PD 10K	
GPP_C22	GPI	GPO	PCH_GPPC22/DGPU_PWR_EN#		PU 10K	+3VS
GPP_C23	GPI	GPO	CPAD_INT#		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GPI	GPI	CIO_PLUG_EVENT		PU 10K	+VCC3V3_SX
GPP_D1	GPI	GPO	GPIO_3_FORCE_PWR		PD 100K	
GPP_D2	GPI	GPI	EXT_SMI#		PU 10K	+3VS
GPP_D3	GPI	GPI	EXT_SCI#		PU 10K	+3VS
GPP_D4	GPI	GPI	(N.C)			
GPP_D5	GPI	GPI	(N.C)			
GPP_D6	GPI	GPI	(N.C)			
GPP_D7	GPI	GPI	WLAN_ON#_X1/WLAN_ON#			
GPP_D8	GPI	GPI	(N.C)			
GPP_D9	GPI	Strap	PCB_ID0		PD 10K	+3VS
GPP_D10	GPI	Strap	PCB_ID1		PD 10K	+3VS
GPP_D11	GPI	Strap	TOUCHPAD_ID		PD 10K	+3VSUS
GPP_D12	GPI	Strap	TOUCH_PANEL_ID		PD 10K	+3VSUS
GPP_D13	GPI	GPI	PCH_GPP_D13/TOUCHPAD_INTR#		PU 10K	+3VSUS
GPP_D14	GPI	GPO	PCH_GPP_D14/WLAN_LED			
GPP_D15	GPI	GPO	PCH_GPP_D15/WLAN_BT_LED			
GPP_D16	GPI	GPI	(N.C)			
GPP_D17	GPI	GPI	(N.C)			
GPP_D18	GPI	GPI	(N.C)			
GPP_D19	GPI	GPI	(N.C)			
GPP_D20	GPI	GPI	(N.C)			
GPP_D21	GPI	GPO	LED_Record		PU 10K	+3VS
GPP_D22	GPI	GPI	(N.C)			
GPP_D23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	GPI	GPI	DIRECT_ESATA_DETECT#		PU 10K	+3VS
GPP_E1	GPI	GPI	SATA_ODD_PRSNT#		PU 10K	+3VS
GPP_E2	GPI	GPI	MSATA_MPCIE_DET#		PU 10K	+3VS
GPP_E3	GPI	GPI	(N.C)			
GPP_E4	GPI	GPI	SATA0_HDD_DEVSLP(N.C)			
GPP_E5	GPI	Native	NGFF1_DEVSLP		PU 10K(@)	+3VS
GPP_E6	GPI	Native	(N.C)		PU 10K(@)	+3VS
GPP_E7	GPI	GPI	(N.C)			
GPP_E8	GPI	Native	SATA_LED#		PU 10K	+3VS
GPP_E9	GPI	Native	USB_OC#0	PD	PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1	PD	PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2	PD	PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3	PD	PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	GPI	GPI	(N.C)			
GPP_F1	GPI	GPO	NGFF2_CONFIG_SEL		PU 10K	+3VS
GPP_F2	GPI	GPI	(N.C)			
GPP_F3	GPI	GPI	(N.C)			
GPP_F4	GPI	GPI	(N.C)			
GPP_F5	GPI	Native	(N.C)			
GPP_F6	GPI	Native	NGFF2_DEVSLP		PU 10K(@)	+3VS
GPP_F7	GPI	GPI	(N.C)			
GPP_F8	GPI	GPI	(N.C)			
GPP_F9	GPI	GPI	(N.C)			
GPP_F10	GPI	GPI	(N.C)			
GPP_F11	GPI	GPI	(N.C)			
GPP_F12	GPI	GPI	(N.C)			
GPP_F13	GPI	GPI	(N.C)			
GPP_F14	GPI	GPI	(N.C)			
GPP_F15	GPI	Native	USB_OC#4		PU 10K	+3VSUS
GPP_F16	GPI	Native	USB_OC#5		PU 10K	+3VSUS
GPP_F17	GPI	Native	USB_OC#6		PU 10K	+3VSUS
GPP_F18	GPI	Native	USB_OC#7		PU 10K	+3VSUS
GPP_F19	GPI	GPI	(N.C)			
GPP_F20	GPI	GPI	(N.C)			
GPP_F21	GPI	GPI	(N.C)			
GPP_F22	GPI	GPI	(N.C)			
GPP_F23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	GPI	GPI	CLKREQ6_NGFF1#_X1		PU 10K	+3VSUS
GPP_H1	GPI	GPI	CLKREQ7_NGFF2#_X1		PU 10K	+3VSUS
GPP_H2	GPI	GPI	CLK_REQ8#		PU 10K	+3VSUS
GPP_H3	GPI	GPI	CLK_REQ9#		PU 10K	+3VSUS
GPP_H4	GPI	GPI	CLK_REQ10#		PU 10K	+3VSUS
GPP_H5	GPI	GPI	CLK_REQ11#		PU 10K	+3VSUS
GPP_H6	GPI	GPI	CLK_REQ12#		PU 10K	+3VSUS
GPP_H7	GPI	GPI	CLK_REQ13#		PU 10K	+3VSUS
GPP_H8	GPI	GPI	CLK_REQ14#		PU 10K	+3VSUS
GPP_H9	GPI	GPI	CLK_REQ15#		PU 10K	+3VSUS
GPP_H10	GPI	GPI	(N.C)			
GPP_H11	GPI	GPI	(N.C)			
GPP_H12	GPO	GPO	(N.C)	PD		
GPP_H13	GPI	GPI	(N.C)			
GPP_H14	GPI	GPI	(N.C)			
GPP_H15	GPI	GPI	(N.C)			
GPP_H16	GPI	GPI	(N.C)			
GPP_H17	GPI	GPI	(N.C)			
GPP_H18	GPI	GPI	(N.C)			
GPP_H19	GPI	GPI	(N.C)			
GPP_H20	GPI	GPI	(N.C)			
GPP_H21	GPI	GPI	(N.C)			
GPP_H22	GPI	GPI	(N.C)			
GPP_H23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GPI	GPI	DDI1_DP_HPD0(N.C)			
GPP_I1	GPI	GPI	DDI2_HDMI_HPD1(N.C)			
GPP_I2	GPI	GPI	DDI3_TBT_HPD2(N.C)			
GPP_I3	GPI	GPI	DDIE_HPD(N.C)			
GPP_I4	GPI	GPI	EDP_HPD		PD 100K	
GPP_I5	GPI	GPI	DDPB_SCL_PCH(N.C)			
GPP_I6	GPO	Native	DDPB_SDA_PCH(N.C)	PD		
GPP_I7	GPI	Native	DDPC_SCL_PCH(N.C)			
GPP_I8	GPO	Native	DDPC_SDA_PCH(N.C)	PD		
GPP_I9	GPI	Native	DDPD_SCL_PCH(N.C)			
GPP_I10	GPO	Native	DDPD_SDA_PCH(N.C)	PD		

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	PM_BATLOW#		PU 8.2K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_X1		PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	PCH_GPD2#		PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#		PU 10K(@)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#		PD 100K	
GPD5	SLP_S4#	Native	SLP_S4#		PD 100K	
GPD6	SLP_A#	Native	SLP_A#			
GPD7	RSVD	GPO	(N.C)			
GPD8	SUSCLK	Native	SUS_CLK#			
GPD9	SLP_WLAN#	Native	SLP_WLAN#		PU 10K(@)	+3VA_DSW
GPD10	SLP_S5#	Native	SLP_S5#			
GPD11	LANPHYPC	Native	LAN_PWREN		PU 10K	+3VA_DSW

EC IT8585 GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	O	GPO	PWR_LED		
GPA1	OD	GPO	CHG_LED#	PU 10K (@)	+3VA_EC
GPA2	OD	GPO	CHG_FULL_LED#	PU 10K (@)	+3VA_EC
GPA3	Alt	PWM	FAN1_PWM		
GPA4	O	GPO	KB_LED_PWM2		
GPA5	Alt	PWM	FAN0_PWM		
GPA6	Alt	PWM	KB_LED_PWM		
GPA7	O	GPO	EC_GPA7		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_OC#	PU 10K	+3VA
GPB1	I	GPI	LID_SW#	PU 10K	+3VA
GPB2	OD	GPO	NUM_LED#		
GPB3	Alt	GPO	EC_GPB3/PWR_SW#	PU 10K	+3VA
GPB4	I	GPO	PS_ON		
GPB5	O	GPO	A20GATE	PU 10K (@)	+3VS
GPB6	OD	GPO	RC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	O	GPO	PM_EXTTS#0(NC)	PU 10K (@)	+3VA_EC
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	O	GPO	PM_PWRBTN#	PU 10K (@)	+3VSUS
GPC4	I	GPI	EC_GPC4	PU 10K(@)	+3V3_AON
GPC5	I	GPI	PM_SUSC#	PD 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PD 100K	
GPC7	O	GPO	EC_GPC7(NC)		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPI	EC_GPD0/Record_Key#		
GPD1	O	GPO	EC_GPD1/ME_AC_PRESENT		
GPD2	Alt	GPI	BUF_PLT_RST#	PD 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	O	GPO	EC_GPD5/OP_SD#		
GPD6	Alt	GPI	FAN0_TACH	PU 10K	+3VS
GPD7	Alt	GPI	EC_GPD7/FAN1_TACH	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PD 4.7K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PD 4.7K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO	LAN_WAKE#	PU 10K (@)	+3VA_EC
GPE4	O	GPO	USB_BC1.2_OFF#/CHG_CLT3		
GPE5	I	GPI	PM_SUSB#	PD 100K	
GPE6	OD	GPO	CAP_LED#		
GPE7	OD	GPO	THRO_CPU#	PU 10K (@)	+3VA_EC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	5VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF1	O	GPO	VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF2	Alt	SMBus	P_SMB0_CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB0_DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	PECI	EC_GPF6/PECI_EC		
GPF7	O	GPO	PCH_SPI_OV		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	O	GPO	PCH_SUSACK#		
GPG2	I	GPI	EC_GPG2/PWRLIMIT_EC#	PU 100K	+3VA_EC
GPG3	GPI		EC_SCE#/EC_SCE#_PCH	PD 10K (@)	
GPG4	GPI		EC_SI/EC_SI_PCH	PD 10K (@)	
GPG5	GPI		EC_SO/EC_SO_PCH	PD 10K (@)	
GPG6	O	GPO	USB30_5VBUS		
GPG7	GPI		EC_SCK_PCH	PD 10K (@)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB3_CLK	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB3_DAT	PU 4.7K	+3VA_EC
GPH3	O	GPO	PM_RSMRST#	PD 10K	
GPH4	O	GPO	DPWROK_EC	PD 10K	
GPH5	O	GPO	PM_PWROK	PD 10K	
GPH6	O	GPO	PM_SYSPWROK	PD 10K	
GPH7	O	GPO	LCD_BACKOFF#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_SUS#		
GPI1	I	GPI	3VSUS_PWRGD		
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3VS
GPI3	I	GPI	IMVP8_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#		
GPI6	Alt	AD	A/D_MAX_POWER	PD 0	+3VACC
GPI7	Alt	AD	MB_MAX_POWER	PU 100K&PD 93.1K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	O	GPI	EC_GPJ0		
GPJ1	O	GPO	3VADSW_ON	PU 100K	+3VA_EC
GPJ2	Alt	DA	PL_REF_EC		
GPJ3	O	GPO	EC_GPJ3 / PCH_SUS_STAT#		
GPJ4	Alt	DA	IBAT_REF_EC		
GPJ5	O	GPO	EC_GPJ5		
GPJ6	I	GPI	EC_GPJ6		
GPJ7	O	GPO	USB_CHARGE_ON#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/EIO0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/EIO1		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/EIO2		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/EIO3		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/ESCK		CLK_KBCPCI_PCH		
GPM5	LFRAME#/ECS#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

Design IP Source:

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	**SM-Bus Address**	
EC Master (SMB1)	**SM-Bus Address**	
SM-Bus Device		
DIMM TEMP.	9Ah	
CPU Thermal Sensor	90h	

Device Identification

CPU Thermal Senser		
1st	06G023123010	NCT7717U
2nd		

Memory Thermal Senser		
1st	06G023048020	
2nd		

Design IP Source:

G751VW Setting

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	**SM-Bus Address**	
SO-DIMM A(0)	A0h	
SO-DIMM B(0)	A4h	
SO-DIMM A(1)	A2h	
SO-DIMM B(1)	A6h	
EC Master (SMB1)	**SM-Bus Address**	
SM-Bus Device		
VGA Thermal Sensor	9Eh	
CPU Thermal Sensor	90h	

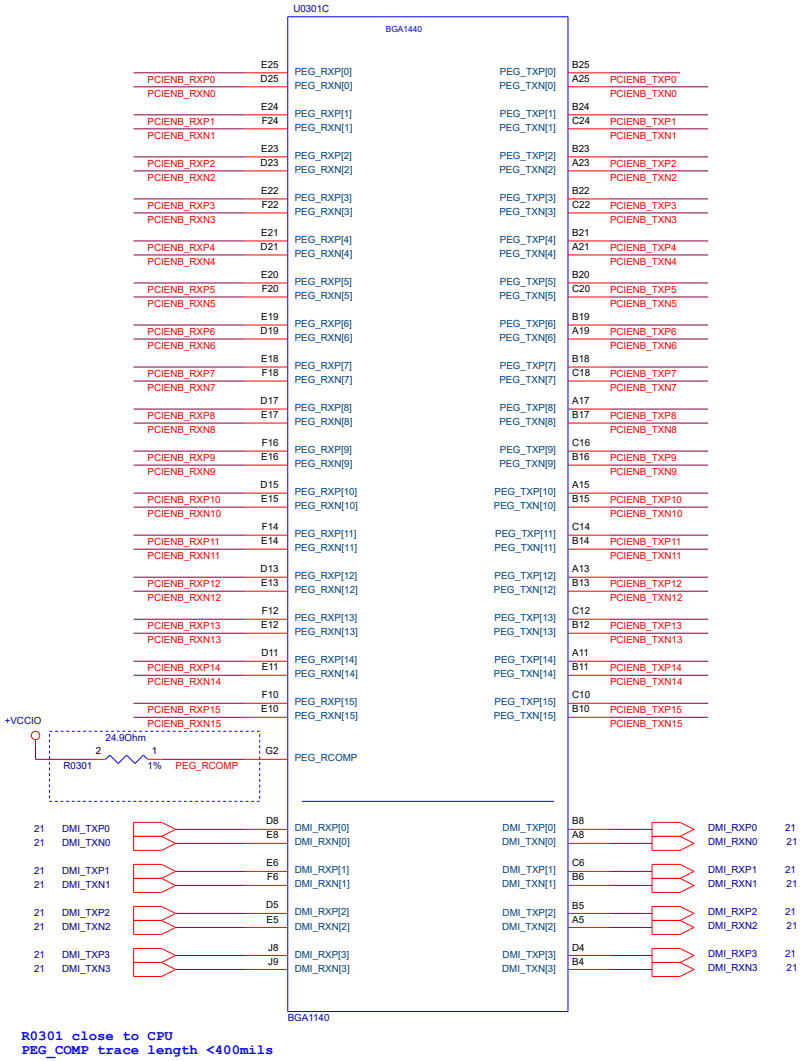
Device Identification

CPU Thermal Senser		
1st	06G023123010	NCT7717U
2nd		

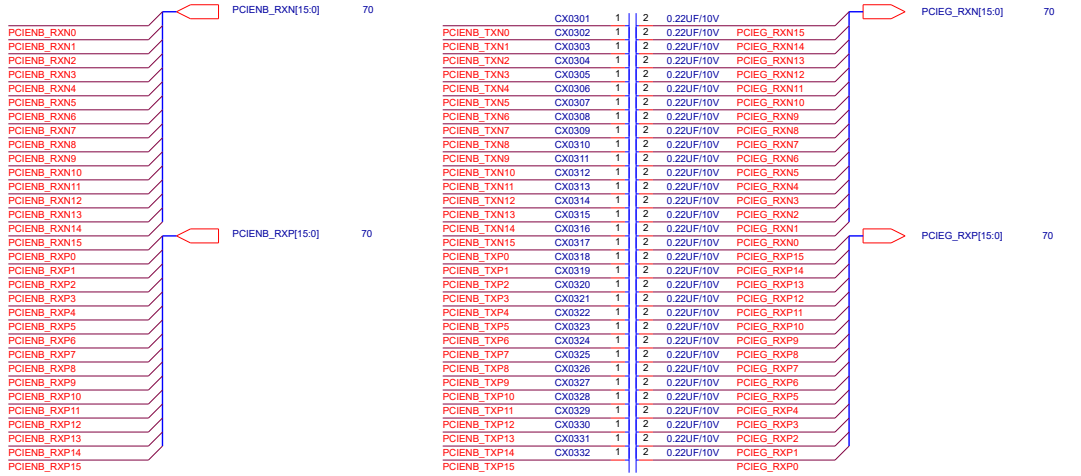
USB3.0/PCIE/SATA Setting		
1	USB3#1(OTG)	USB Port1 (Charge Port)
2	USB3#2	USB Port2
3	USB3#3	
4	USB3#4	
5	USB3#5	USB Port3(IO BD)
6	USB3#6	USB Port4(IO BD)
7	USB3#7	Card Reader
8	USB3#8	
9	PCIE#3	WLAN
10	PCIE#4	Giga LAN
11	PCIE#5	ThunderBolt Alpine-Ridge
12	PCIE#6	
13	PCIE#7	
14	PCIE#8	
15	PCIE#9	PCIE3.0 x 4 SSD
16	PCIE#10	
17	PCIE#11	
18	PCIE#12	
19	SATA#0	SATA HDD
20	SATA#1	SATA ODD
21	PCIE#15	
22	PCIE#16	
23	PCIE#17	PCIE3.0 x 4 SSD
24	PCIE#18	
25	PCIE#19	
26	PCIE#20	

USB2.0 Setting		
1	USB2#1	USB Port1
2	USB2#2	USB Port2
3	USB3#3	
4	USB3#4	CMOS Camera
5	USB3#5	USB Port3(IO BD)
6	USB3#6	USB Port4(IO BD)
7	USB3#7	Card Reader
8	USB3#8	Macro Key
9	USB3#9	BT
10	USB3#10	N- Key
11	USB3#11	
12	USB3#12	Touch Panel

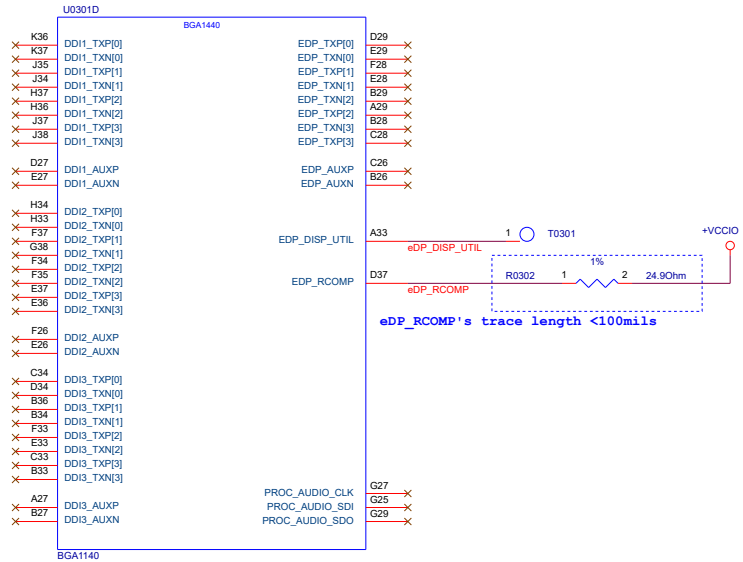
DMI & PCIEG



R0301 close to CPU
PEG_COMP trace length <400mils



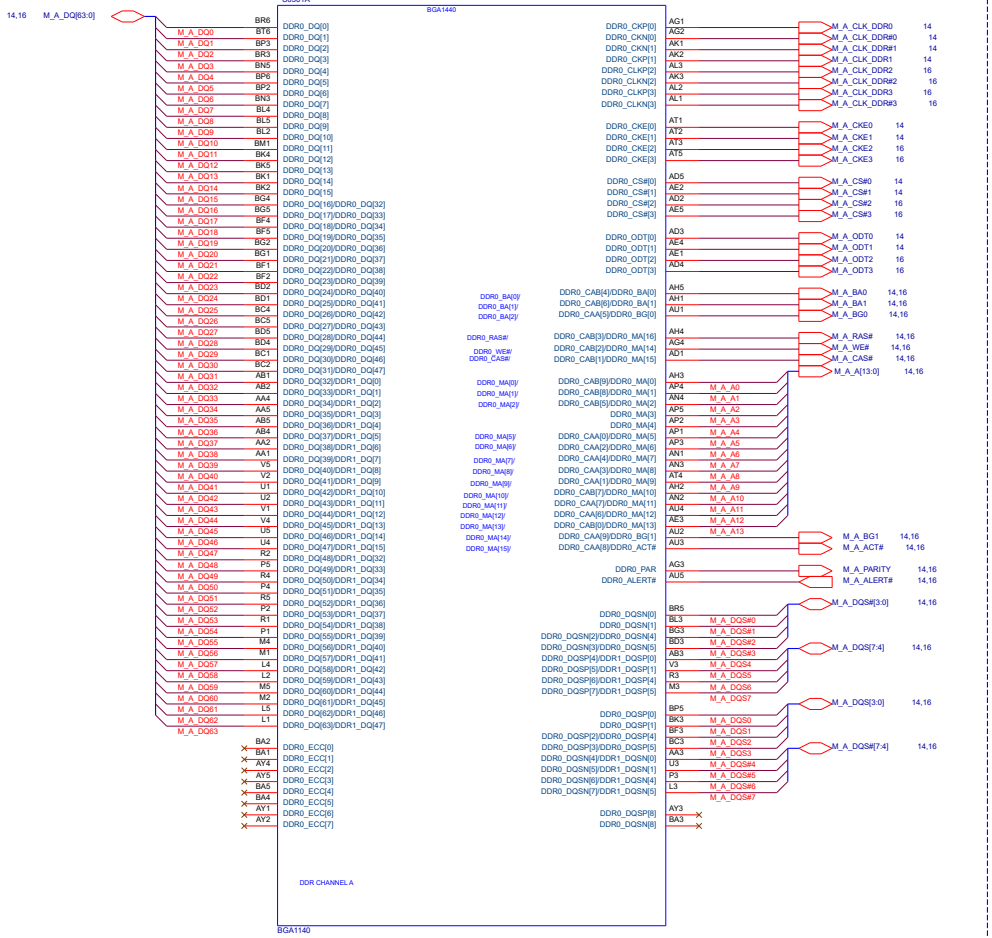
Display



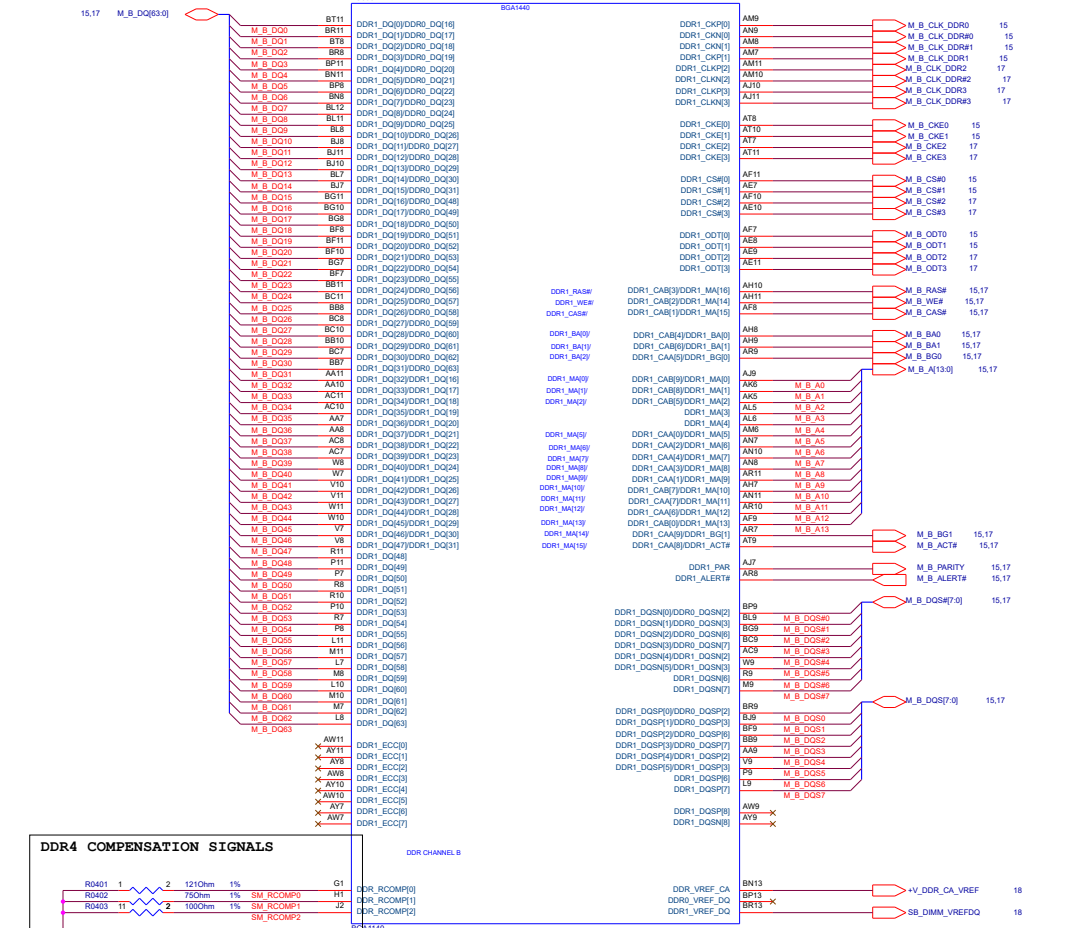
eDP_RCOMP's trace length <100mils

ASUS	Project Name: G752VY	Rev: 2.0
Title : CPU DMI/PCG/DISPY		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 3 of 102	

Memory Channel A

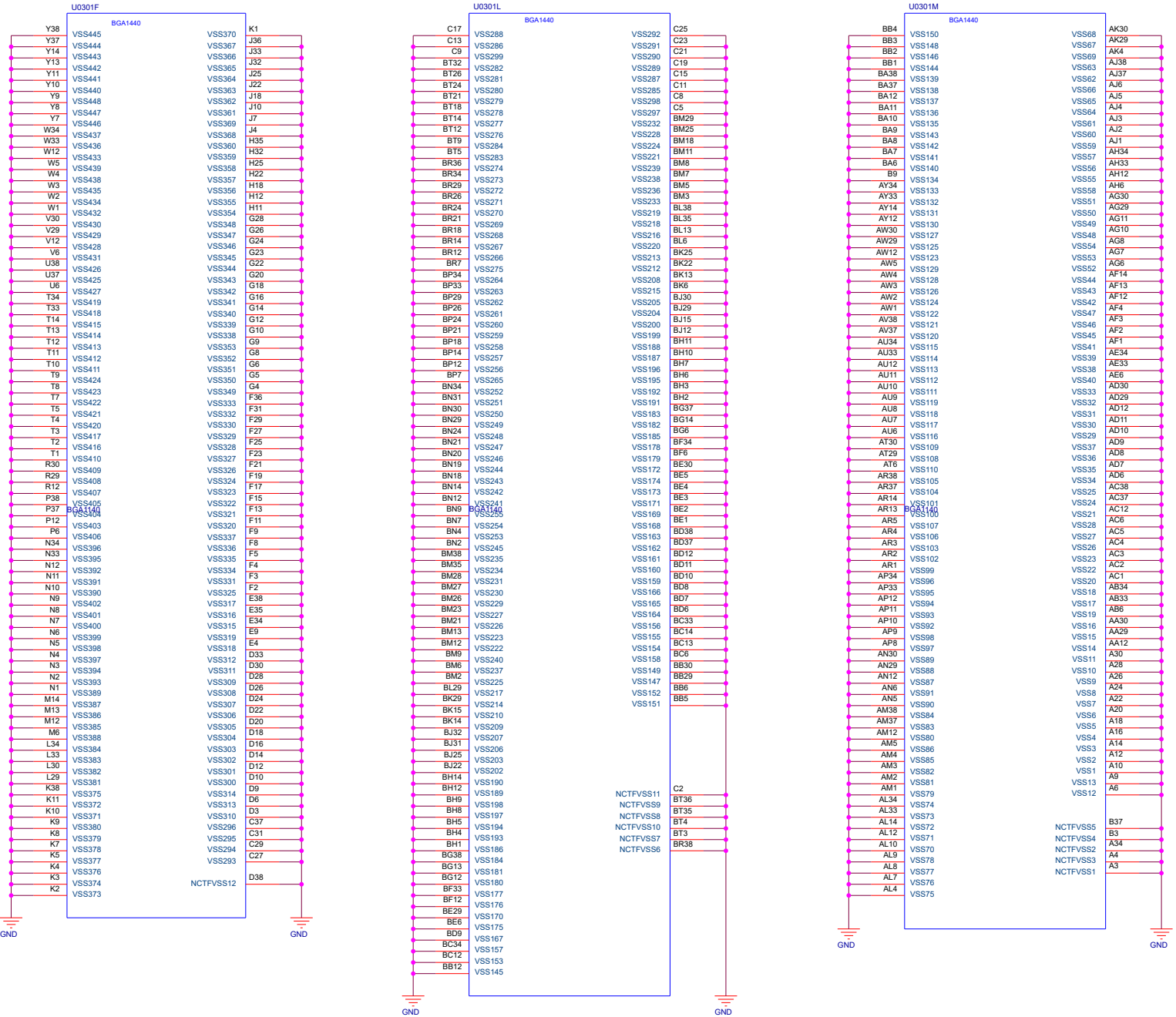


Memory Channel B



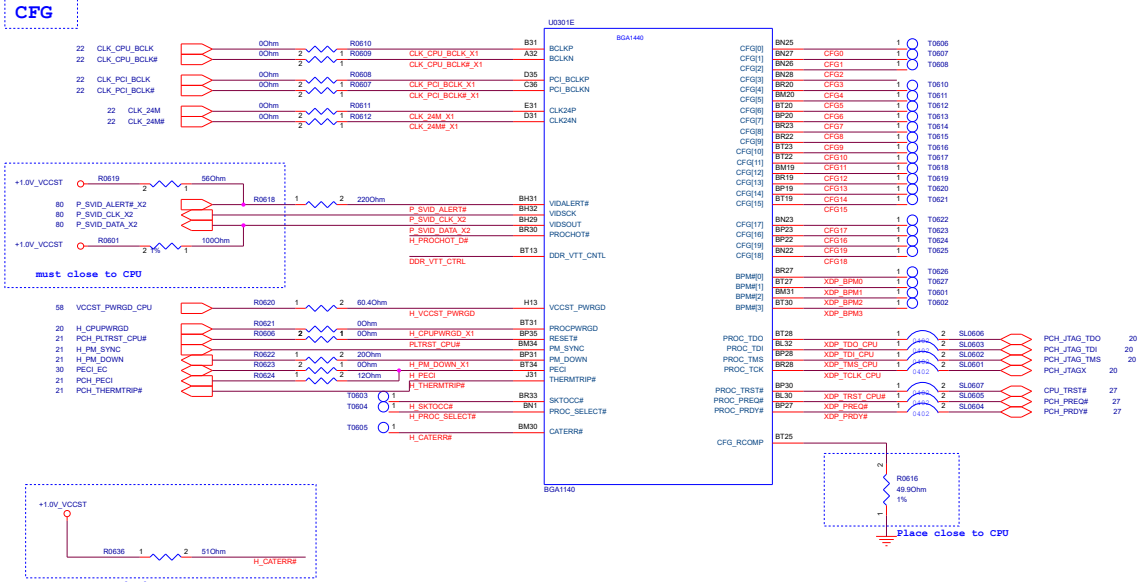
DDR4 COMPENSATION SIGNALS

ASUS	Project Name: G752VY		Rev: 2.0
Title : CPU DDR4			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Tuesday, July 21, 2015		Sheet 4 of 102	

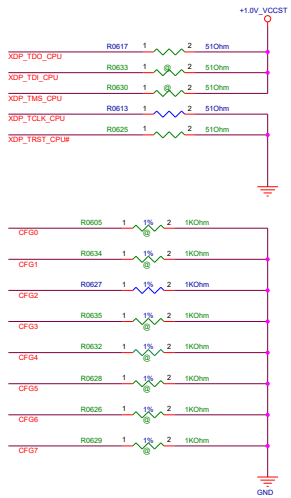


Project Name	G752VY
Rev	2.0
Title :	CPU GND
Size	B
Dept.:	ASUSTeK COMPUTER INC. (R
Engineer:	Richard Liu
Date:	Tuesday, July 21, 2015
Sheet	5 of 102

CFG



CFG Straps



CFG Straps for Processor

ref : Intel 544924_Skylake_EDS_Vol_1_Rev0.9 P.121

CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted

- 1 : (Default) Normal Operation; No stall
- 0 : Stall

CFG[1] : Reserved Configuration Lane

Reserved Configuration Lane

CFG[2] : PCI Express* Static x16 Lane Numbering Reversal

- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[3] : Reserved configuration lanes

Reserved Configuration Lane

CFG[4] : eDP Enable

- 1 : Disabled
- 0 : Enabled

CFG[6:5] : PCI Expres* Bifurcation

- 00 : 1 x8 , 2 x4 PCI Express*
- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

CFG[7] : PEG Training

- 1 : (Default) PEG Train Immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training

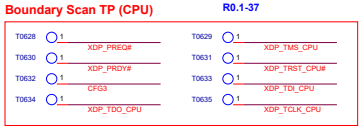
CFG[19:8] : Reserved Configuration Lanes

Reserved Configuration Lanes

Intel 544924_Skylake_EDS_Vol_1_Rev0.9 P.121
Richard 20141209

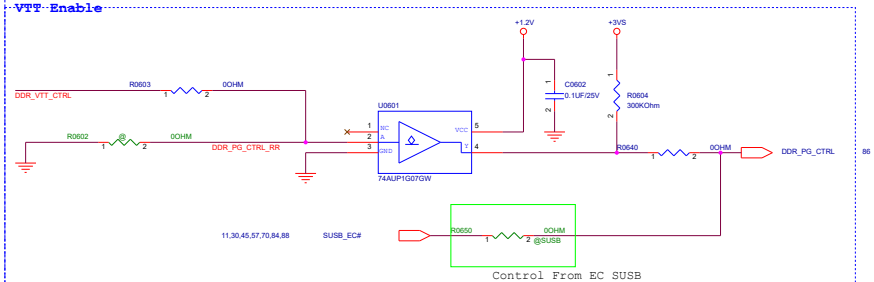
Boundary Scan TP (CPU)

R0.1-37

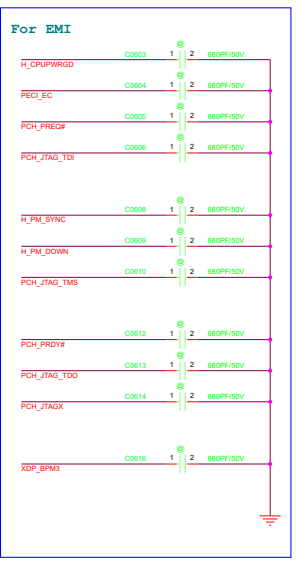


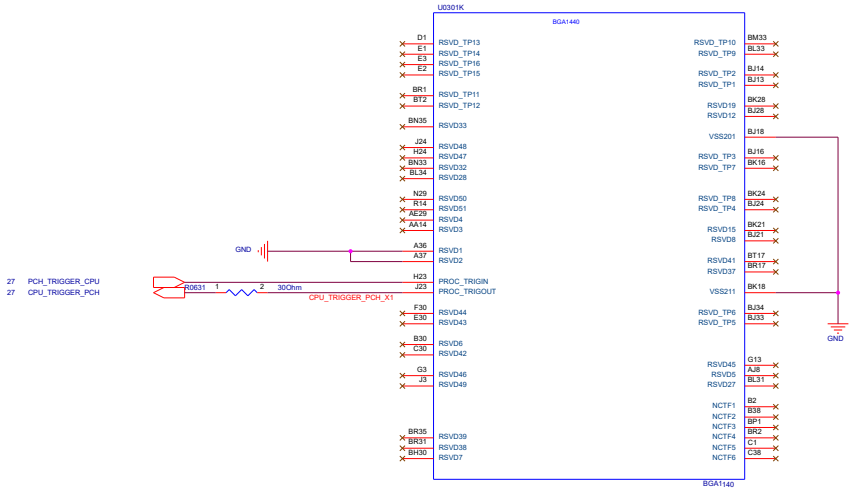
DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref:544924_544924_Skylake_EDS_Vol_1_Rev0.9.pdf P.120

VTT Enable

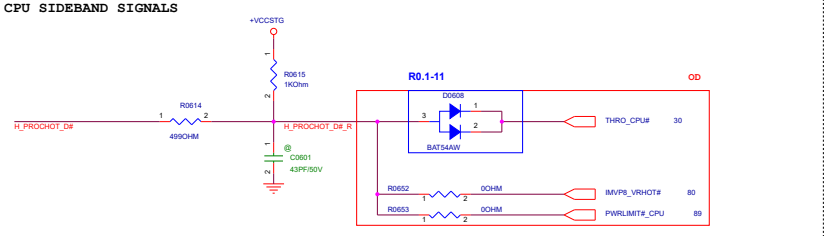


For EMI





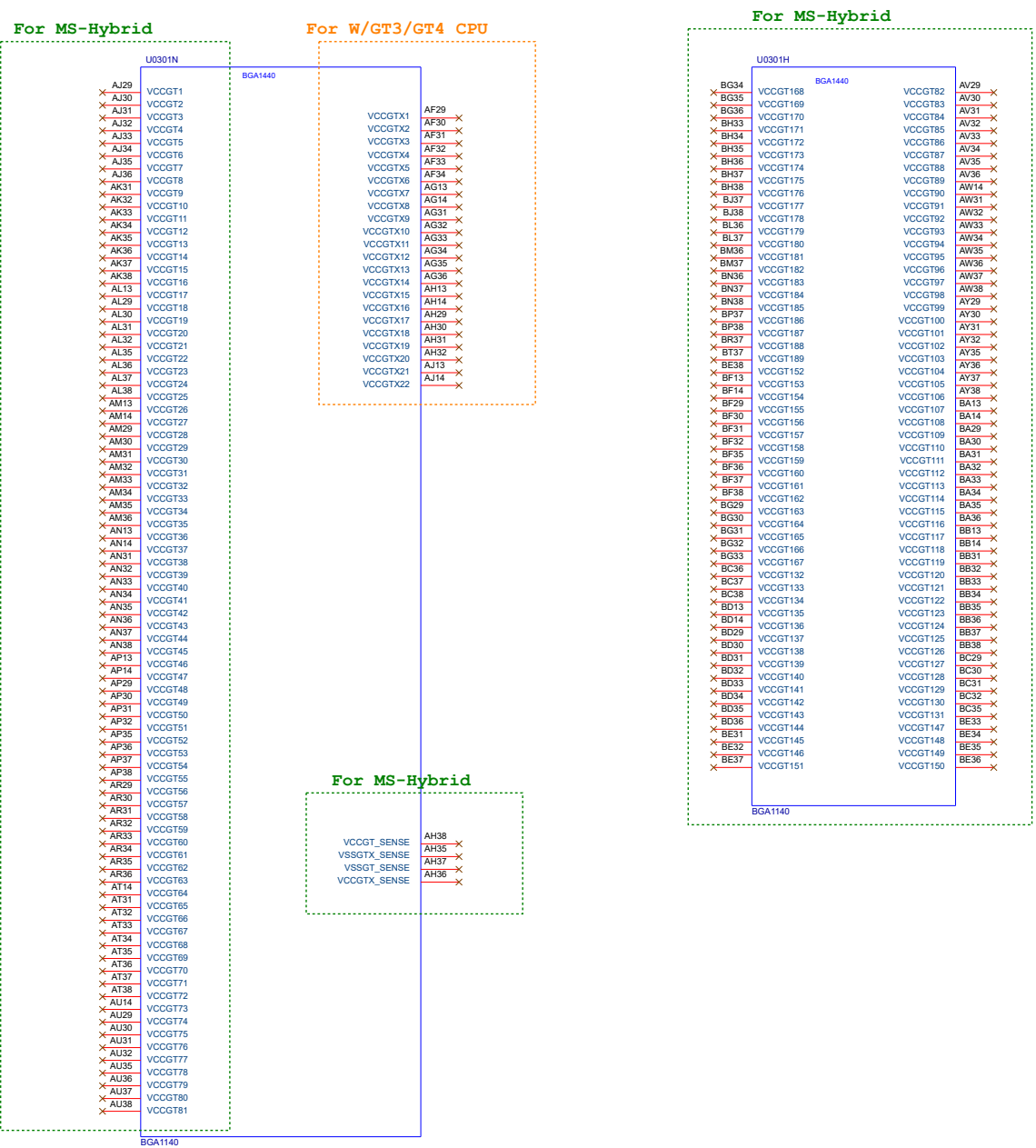
CPU SIDEBAND SIGNALS



ASUS	Project Name: G752VY		Rev: 2.0
Title : CPU CFG			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Tuesday, July 21, 2015	Sheet 6 of 102		

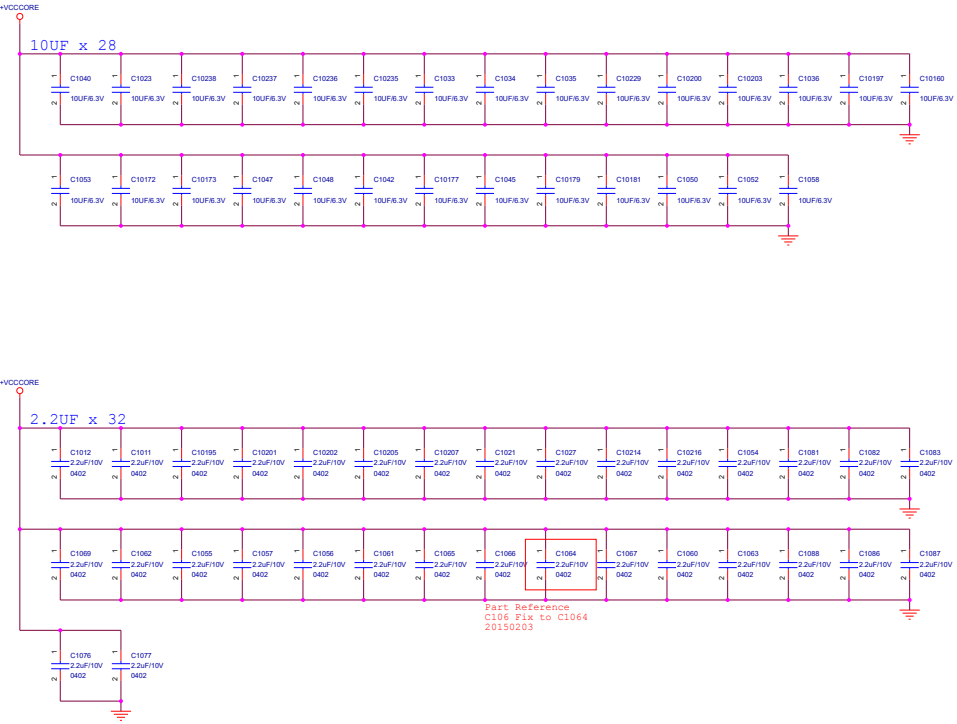
CPU XDP connector

Project Name: G752VY		Rev: 2.0
Title : CPU XDP		
Size: A	Dept.: ASUSTeK COMPUTER INC. (RD)	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 7 of 102	



Project Name: G752VY		Rev: 2.0
Title : CPU Power		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 9 of 102	

+VCCORE DECAPS Place Back Side (TOP)



+VCCGT DECAPS Place Back Side (TOP)

ASUS	Project Name: G752VY	Rev: 2.0
Title :	CPU Power Cap.	
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 10 of 102	

Main Board

NOTE:
For JTAG Debug

IF SOME OF GPIOs ARE NOT IN USE,
FOLLOW TABLE BELOW :

NOTE:
ASSEMBLE R1115, R1104 if DPSRC IS NOT IN USE

Alpine-Ridg Flash Memory

PCH_R2506 10Kohm Pull High +3Vs

To PCH GPIO that supports SCI

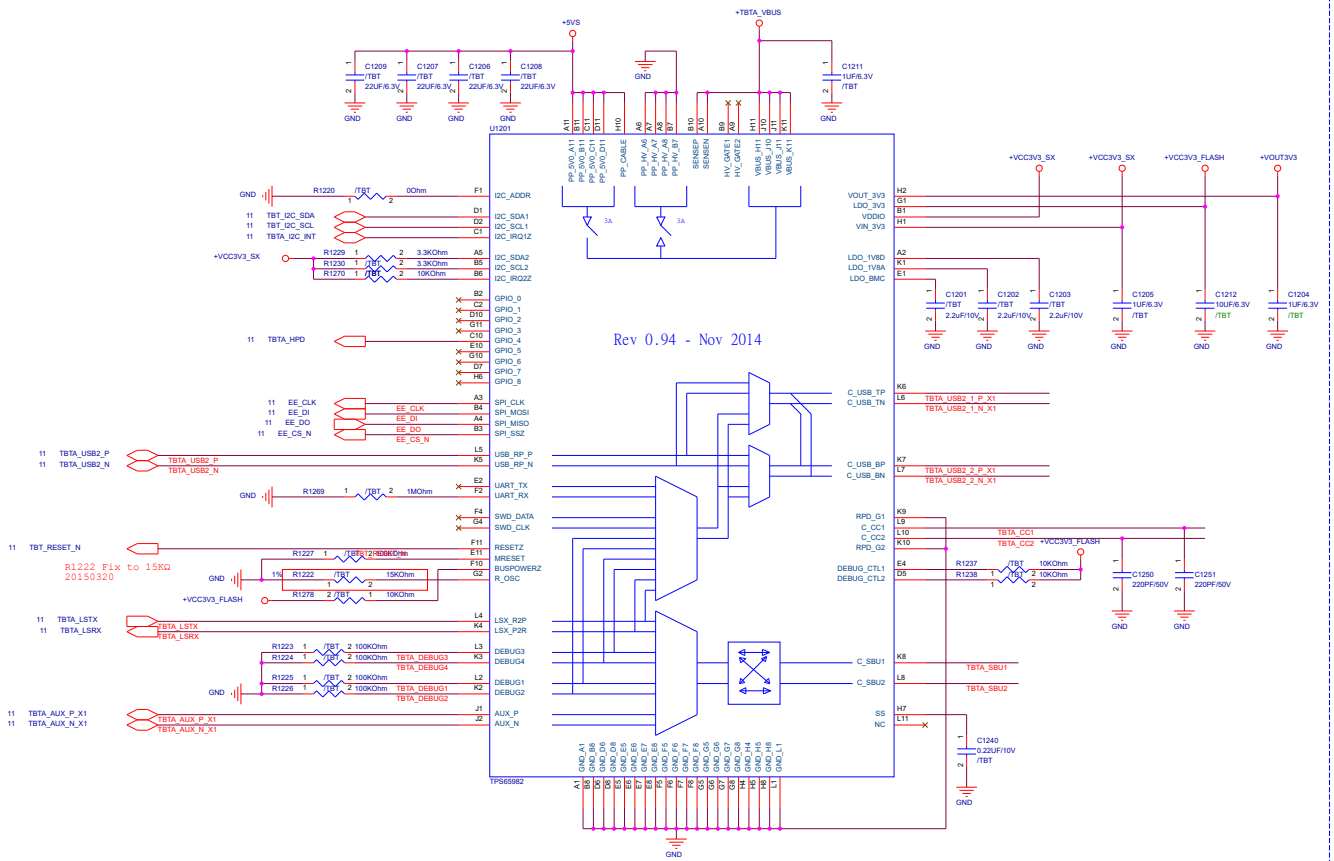
Low pulse

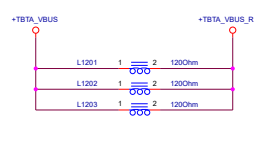
TBT SLP_S3#

TBT Force PWR

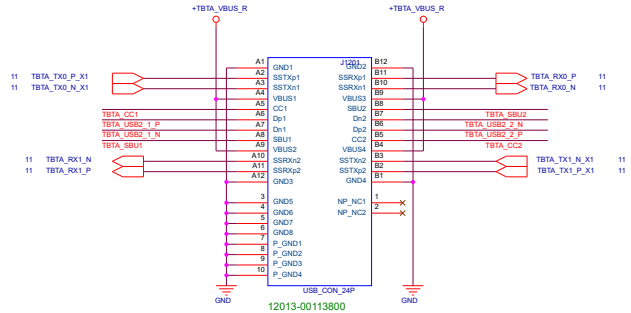
Debug Pin Not Use Setting:

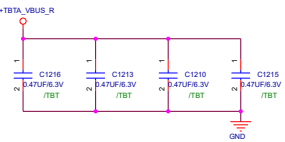
Project Name	G752VY
Rev	2.0
Title :	Intel Alpine-Ridge
Size	
Dwgt.:	ASUSTeK COMPUTER INC
Engineer:	Richard Liu
Date: Tuesday, July 21, 2015	Sheet 11 of 102



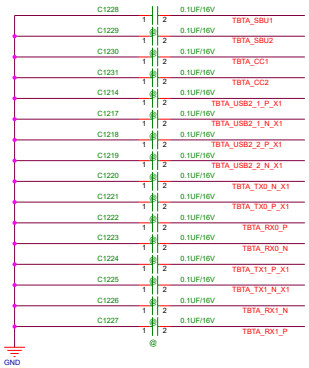


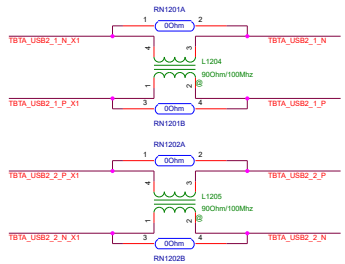
USB type C



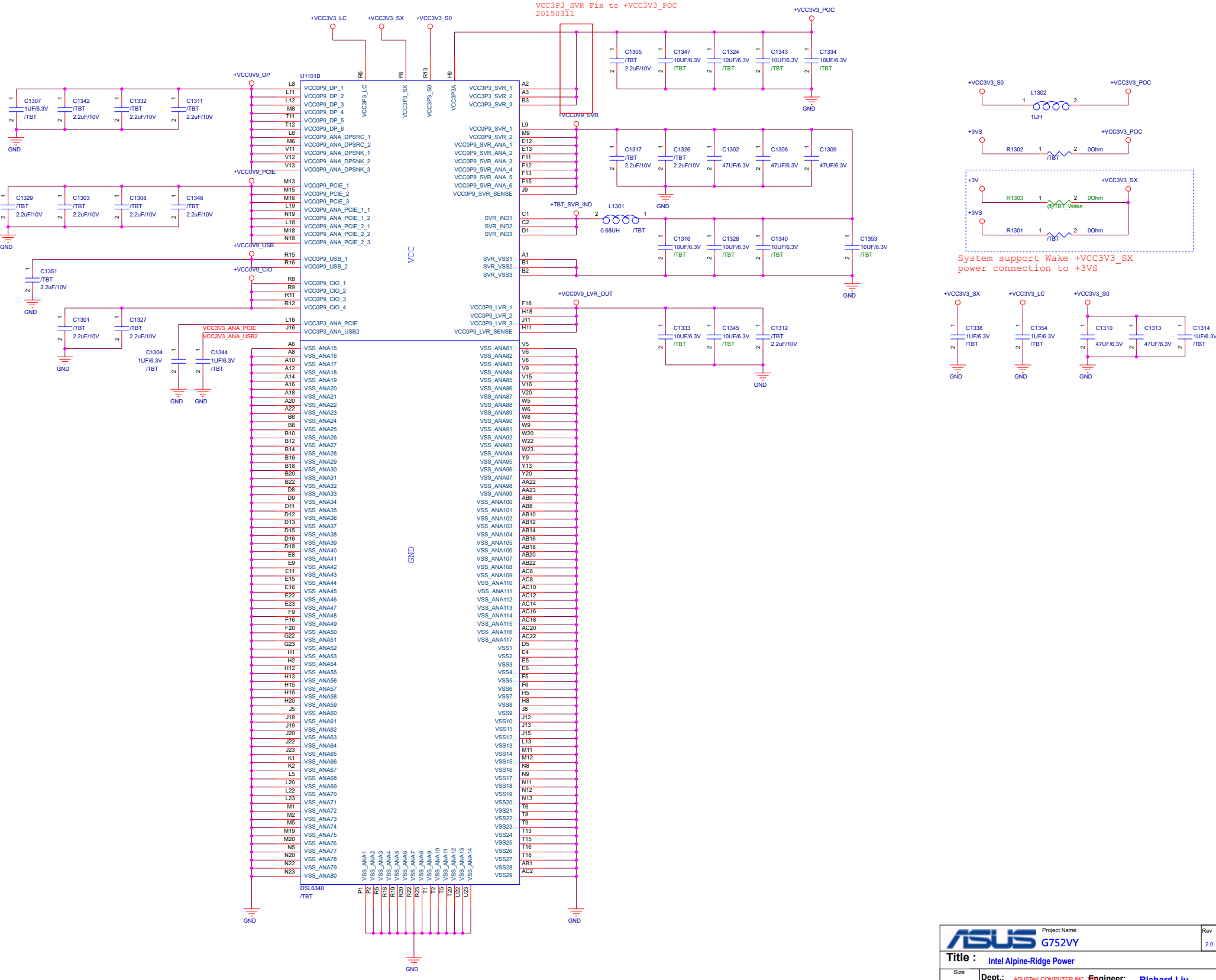


ESD-Protection





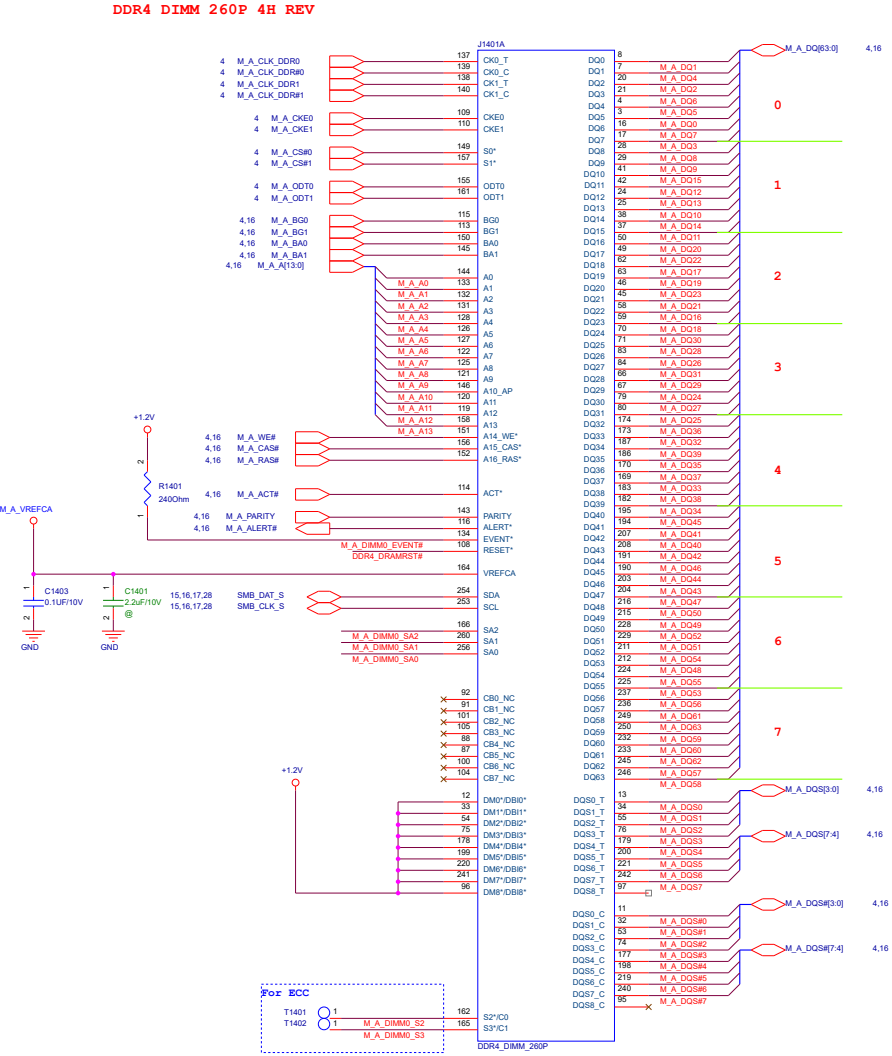
Project Name: G752VY			Rev: 2.0
Title: TPS65982 & USB 3.1 Type-C			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Wednesday, July 22, 2015	Sheet 12 of 102		

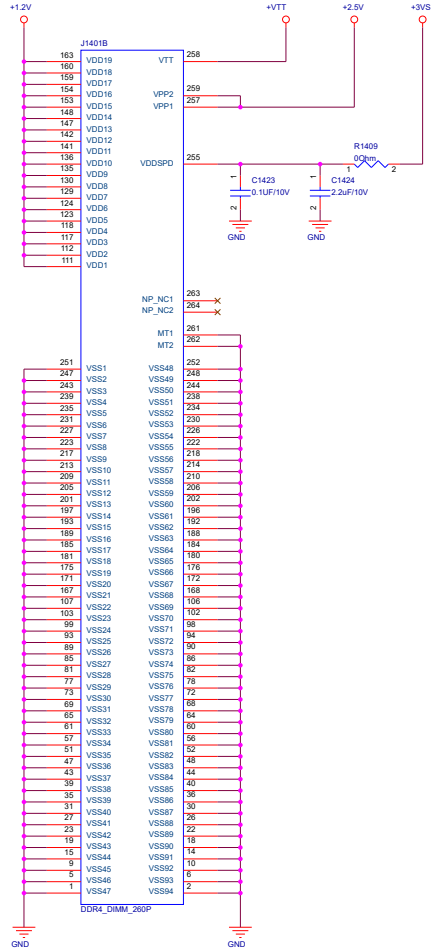


Project Name	G752VY
Rev	2.0
Title :	Intel Alpine-Ridge Power
Size	Custom
Dept.:	ASUSTeK COMPUTER INC.
Engineer:	Richard Liu
Date:	Tuesday, July 21, 2015
Sheet	13 of 102

SODIMM CHA-DIMM0
TOP H4.0mm REV (J1401)

12002-00080600
DDR4 DIMM 260P 4H REV

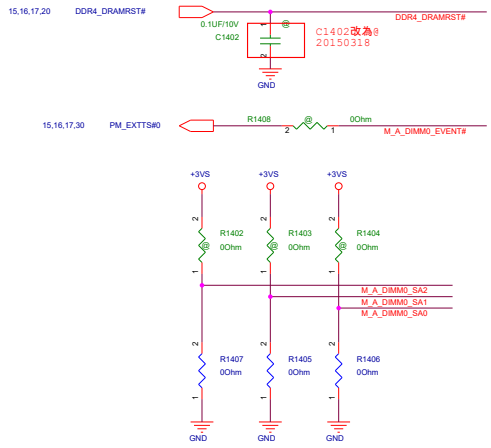


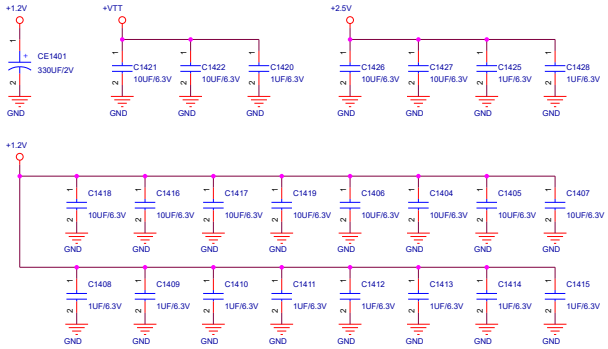


SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH

Main Board



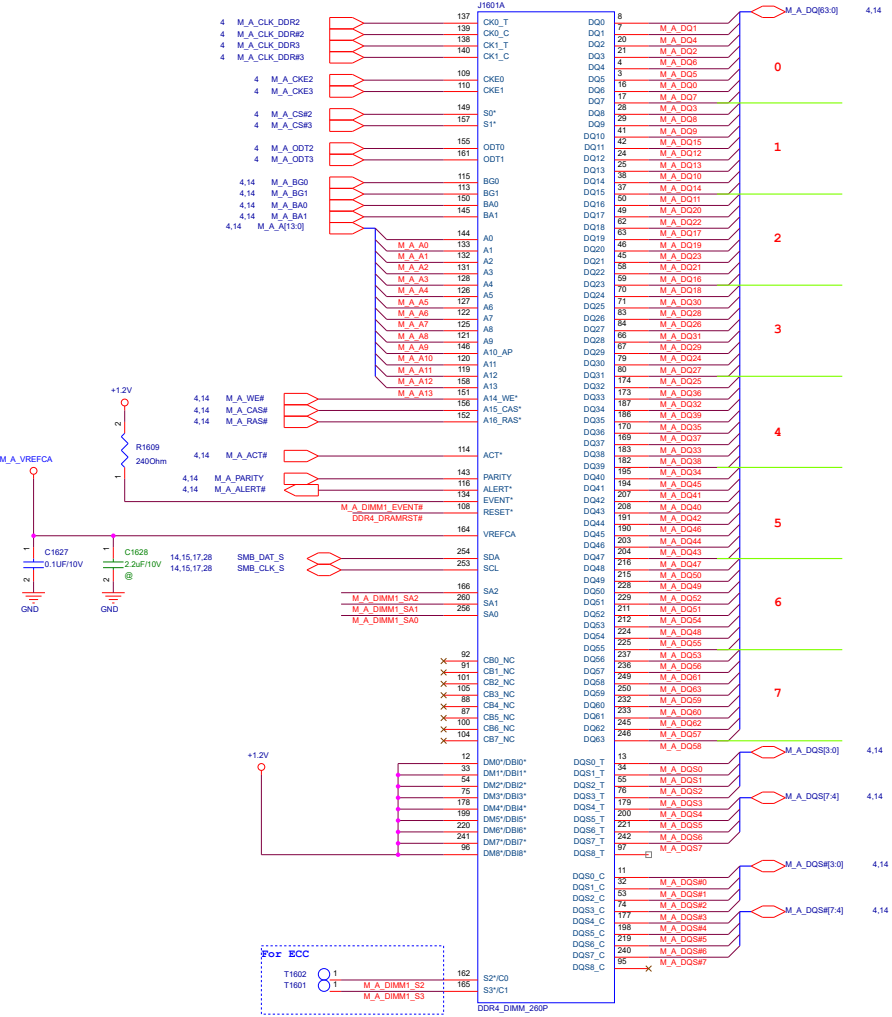


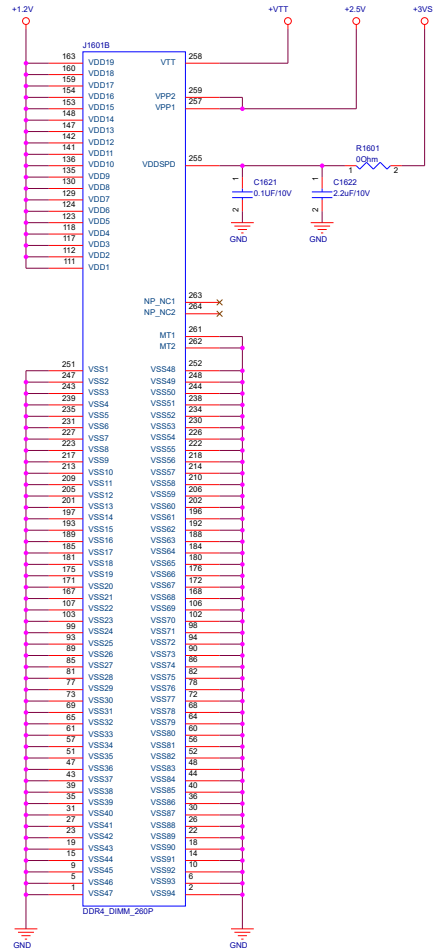
Main Source	1th PWR	2nd PWR
AC_BAT_SYS	+1.2V	+VTT (0.6V From PU8600)
		M_A_VREFCA (0.6V From +1.2V)
	+3VA_DSW	+3VS
		+2.5V

ASUS	Project Name: G752VY		Rev: 2.0
Title :	DIM_DDR4 SO-DIMM A1		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Tuesday, July 21, 2015		Sheet 14 of 102	

SODIMM CHA-DIMM1
BOT H4.0mm STD (J1601)

12002-00080700
DDR4 DIMM 260P 4H STD

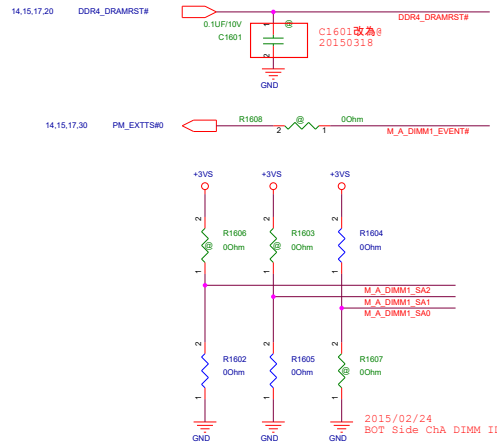


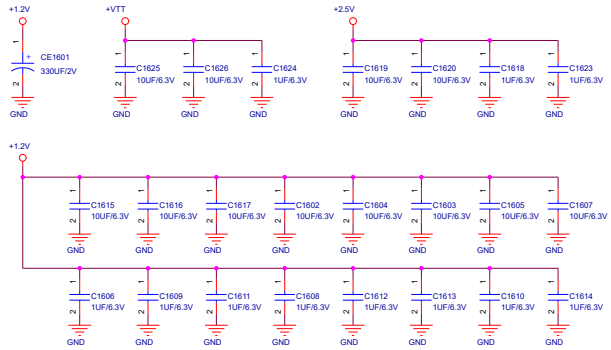


SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH

Main Board

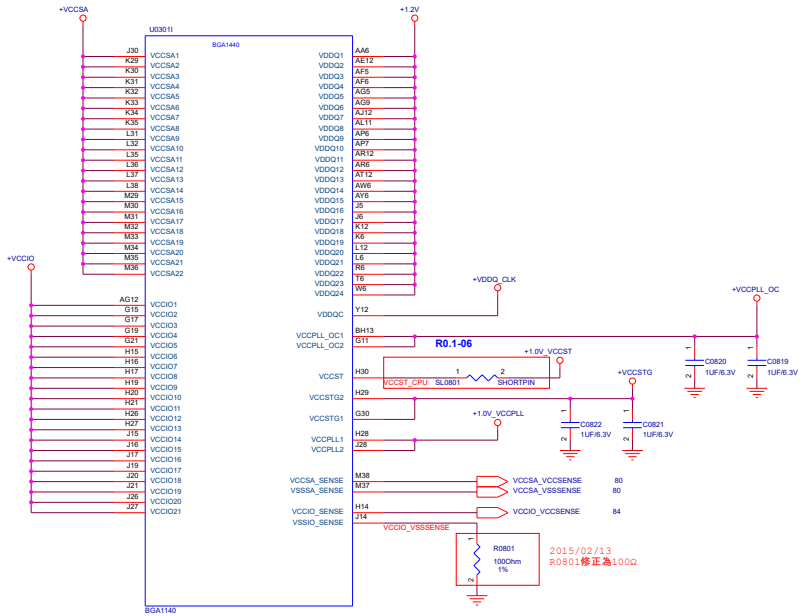


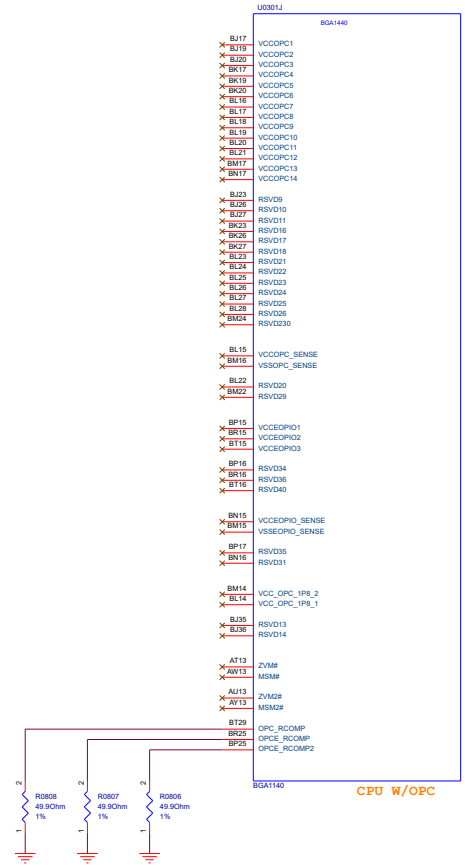


Main Source	1th PWR	2nd PWR
AC_BAT_SYS	+1.2V	+VTT (0.6V From PU8600)
		M_A_VREFCA (0.6V From +1.2V)
	+3VA_DSW	+3VS
		+2.5V

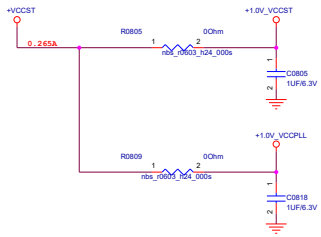
ASUS	Project Name: G752VY		Rev: 2.0
Title :	DIM_DDR4 SO-DIMM A0		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Tuesday, July 21, 2015	Sheet 16 of 102		

OPC Power Rails

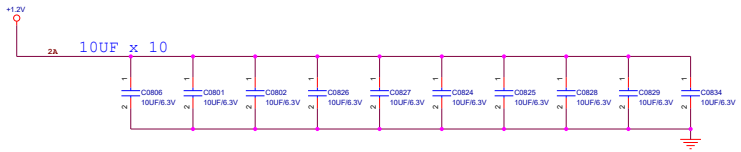




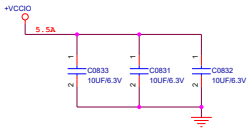
+1.0V_VCCST/+1.0V_VCCPLL DECAPS Place Back Side (TOP)



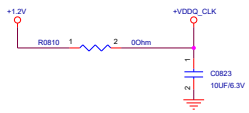
+VDDQ DECAPS Place Back Side (TOP)



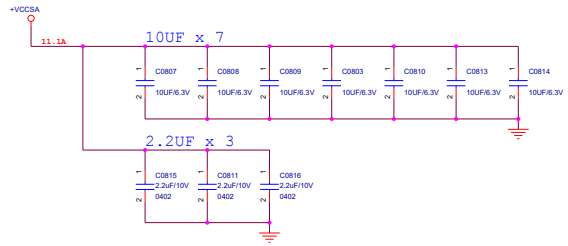
+VCCIO DECAPS Place Back Side (TOP)

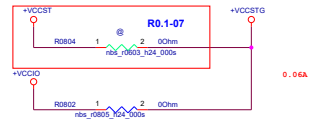


+VDDQ_CLK DECAPS Place Back Side (TOP)



+VCCSA DECAPS Place Back Side (TOP)



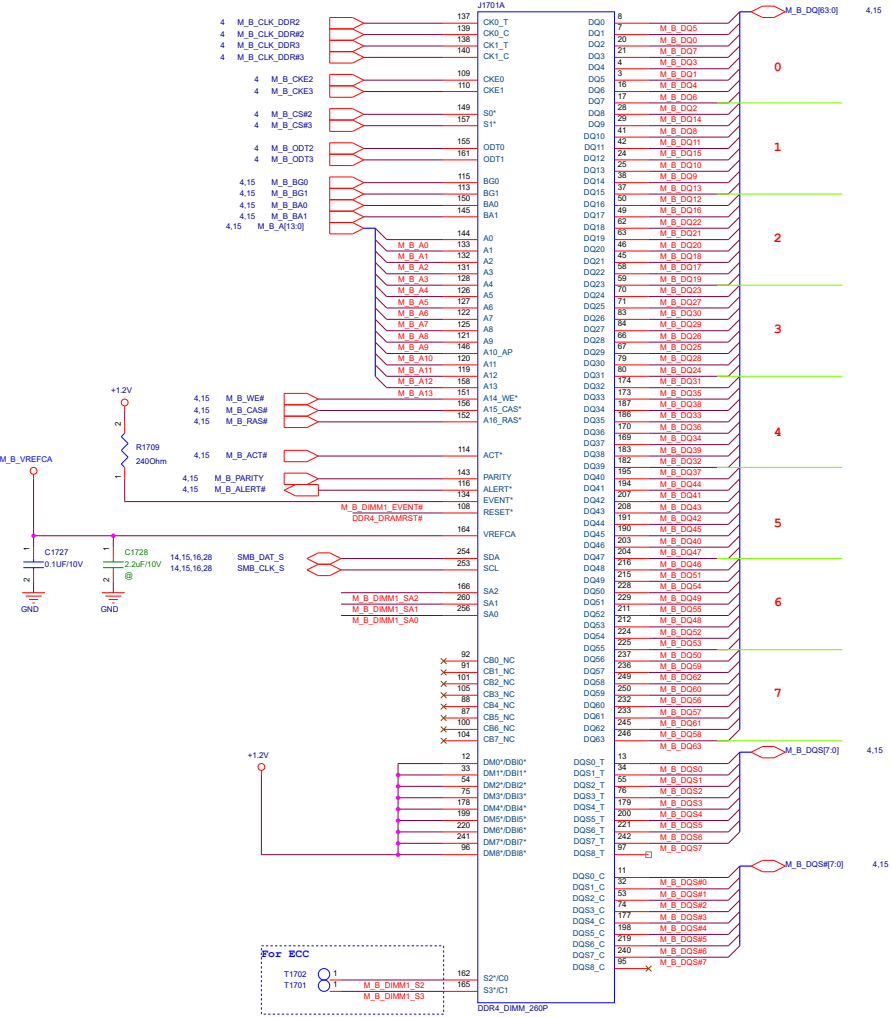


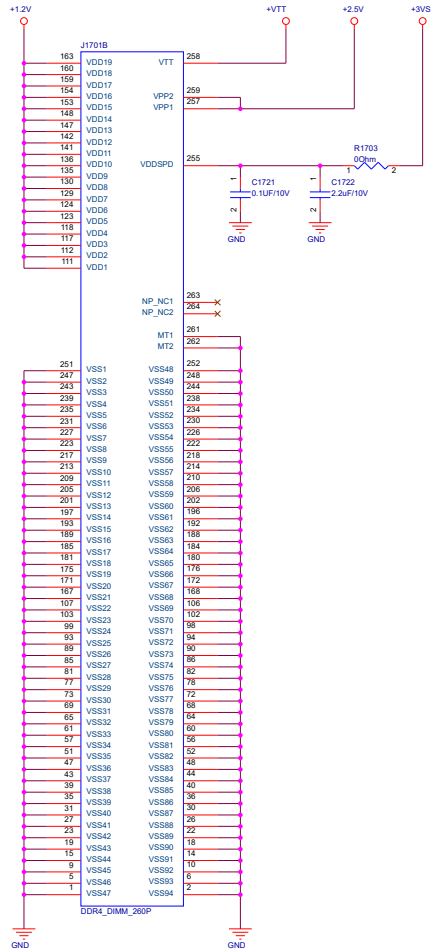
Volume Segment
+VCCIO is supplied +1.0VS (shared with +VCCSTG)

ASUS	Project Name: G752VY	Rev: 2.0
Title : CPU Power		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 8 of 102	

SODIMM CHB-DIMM1
BOT H8.0mm STD (J1701)

12002-00080500
DDR4 DIMM 260P 8H STD

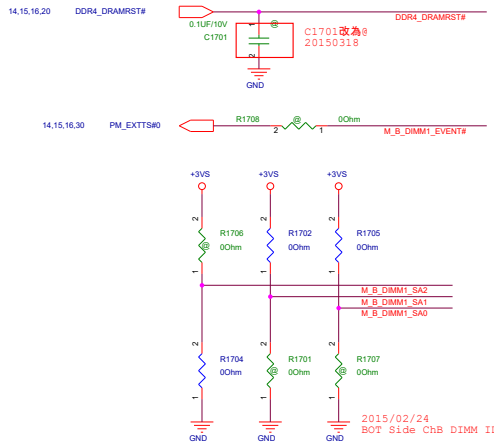


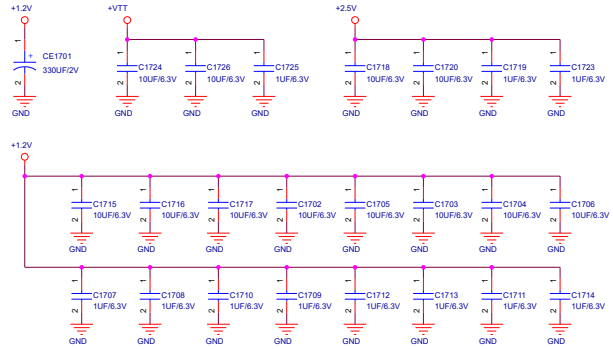


SO-DIMMs that do not support ECC (x64 only)
will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a
combined SPD/Thermal Sensor with EVENT# wired.

EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH

Main Board





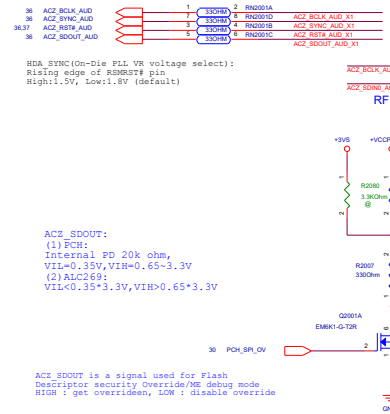
Main Source	1th PWR	2nd PWR
AC_BAT_SYS	+1.2V	+VTT (0.6V From PU8600)
		M_A_VREFCA (0.6V From +1.2V)
	+3VA_DSW	+3VS
		+2.5V

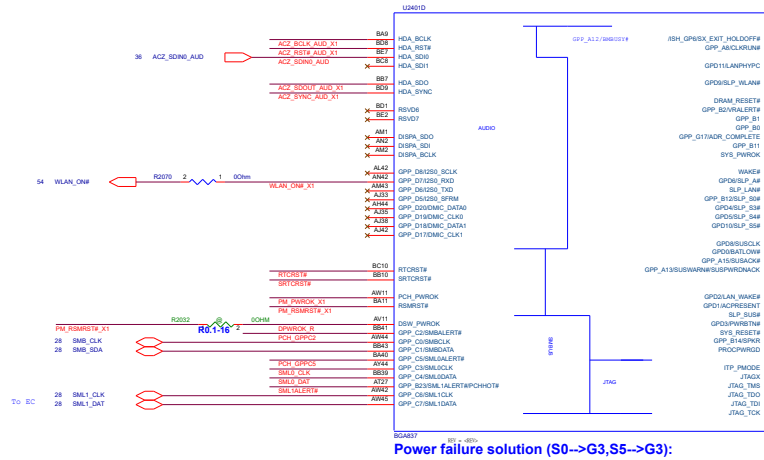
ASUS	Project Name: G752VY	Rev: 2.0
Title :	DIM_DDR4 SO-DIMM B0	
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 17 of 102	

Main Board

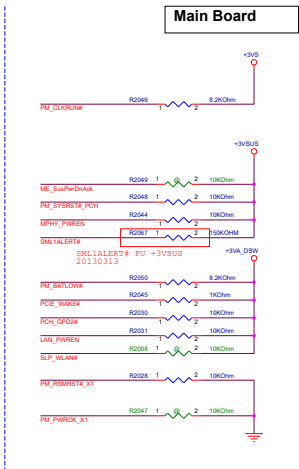
ASUS	Project Name: G752VY	Rev: 2.0
Title : NB*		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 10 of 102	

HD Audio



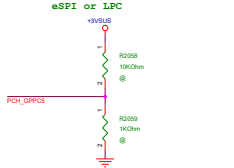


Power failure solution (S0-->G3,S5-->G3):



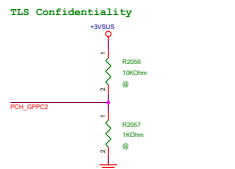
Main Source	1th PWR	2nd PWR	3rd PWR	4th
+RTCBAT	+RTC_BAT	+3VA_RTC		
AC_BAT_SYS	+1.0VSUS	+VCCST	+1.0V_VCCST	
	+1.2V			
	+3VAO	+3VA	+3VA_EC	
	+3VA_DSW	+3VSUS	+3VSUS_PCH	+VCCPAZIO
		+3VS		

eSPI or LPC



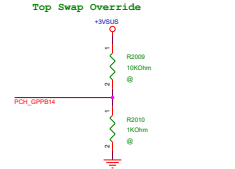
PCH_GPPC5: weak internal pull down	
PU	eSPI
PD	LPC (default)

TLS Confidentiality



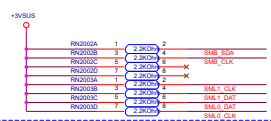
PCH_GPPC2: weak internal pull down	
PU	Enable
PD	Disable (default)

Top Swap Override



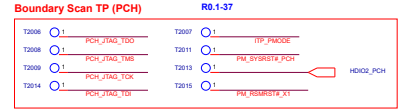
PCH_GPPB14: weak internal pull down	
PU	Enable
PD	Disable (default)

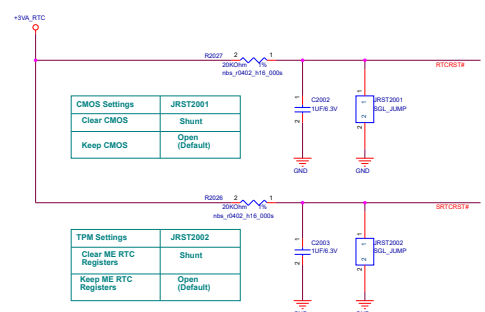
SMBUS

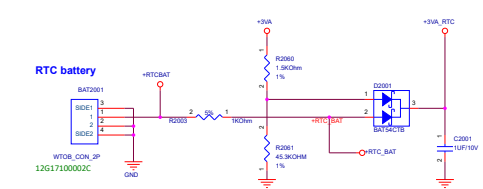


Boundary Scan TP (PCH)

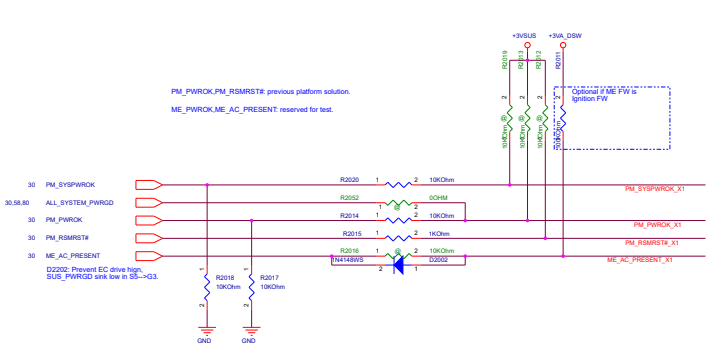
R0.1-37



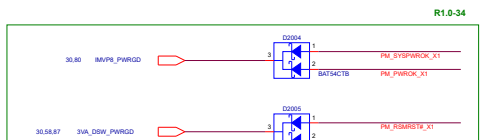




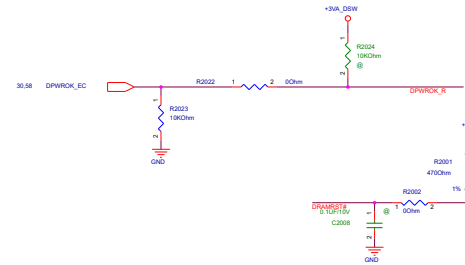
USE RTC Battery:
P/N: 0B100-00020300 BATT-LI CR2032 3V/220mAH
P/N: 0B100-00020400 BATT-LI CR2032 3V/220mAH



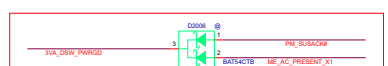
R1.0-34



Power failure solution (S0-->G3,S5-->G3)



R1.1-03



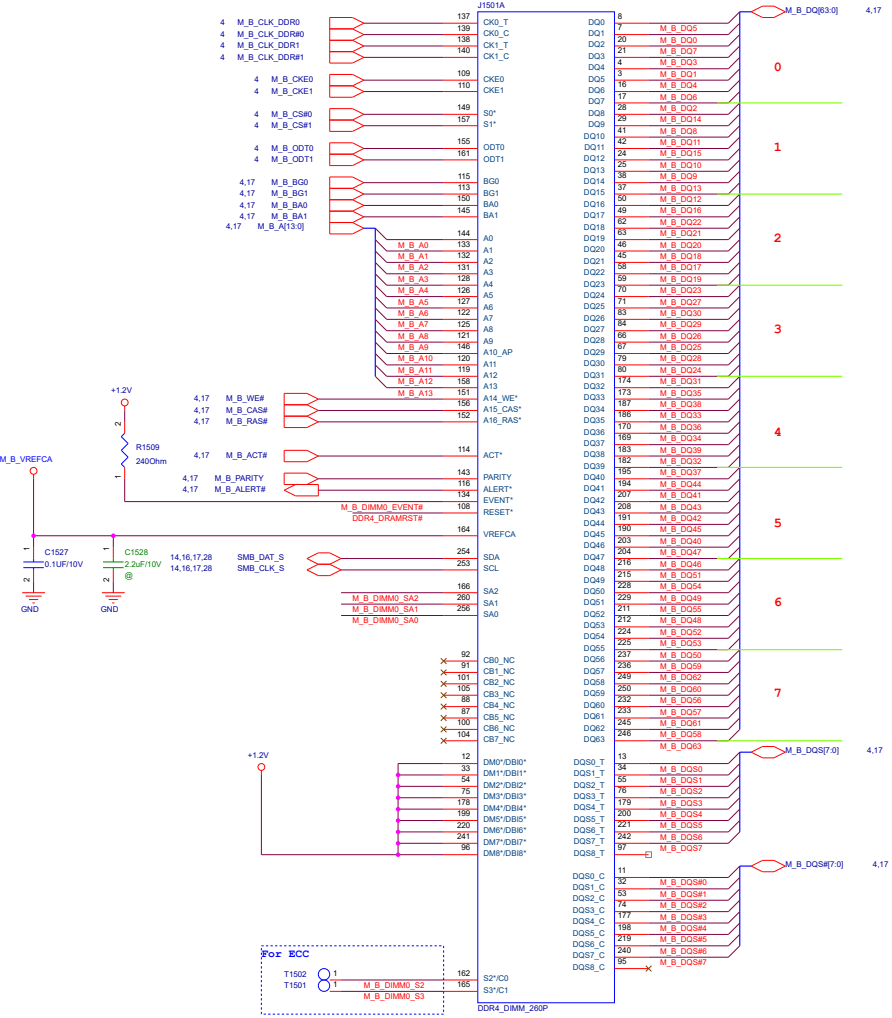
Change D2040 to 10Kohm if mount D2006

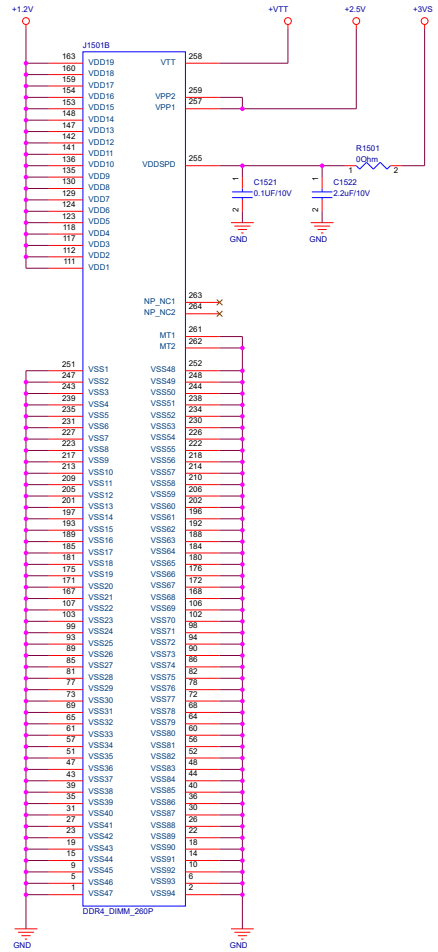
Deep SX discharge (S0-->DSX,S5-->DSX)

ASUS	Project Name: G752VY		Rev: 2.0
Title :	PCH-CPT(1)SATA,IHDA,RTC,JTAG		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Tuesday, July 21, 2015	Sheet 20 of 102		

SODIMM CHB-DIMM0
TOP H4.0mm STD (J1501)

12002-00080700
DDR4 DIMM 260P 4H STD

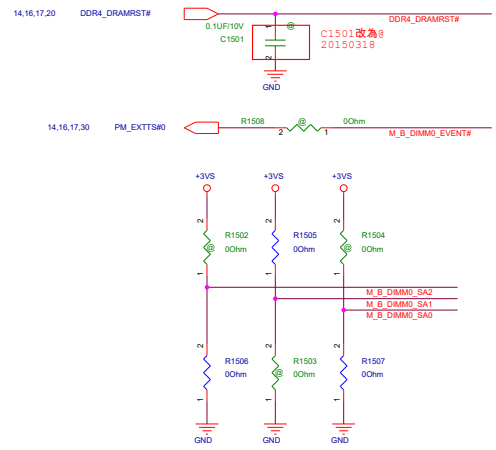


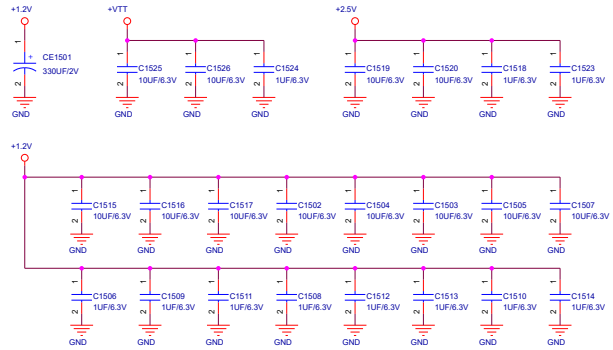


SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH

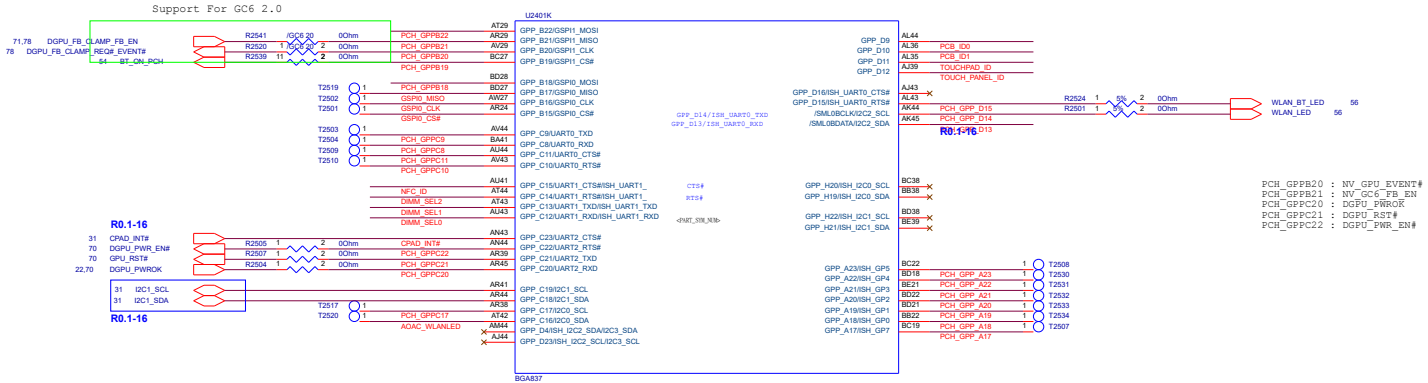
Main Board

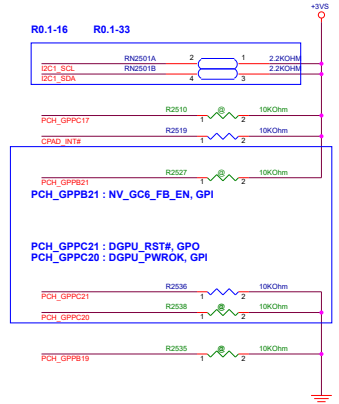


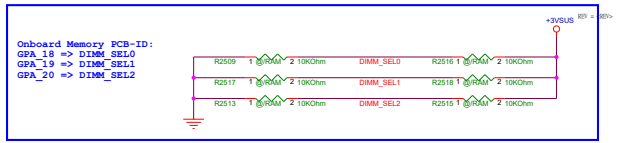


Main Source	1th PWR	2nd PWR
AC_BAT_SYS	+1.2V	+VTT (0.6V From PU8600)
		M_A_VREFCA (0.6V From +1.2V)
	+3VA_DSW	+3VS
		+2.5V

ASUS	Project Name: G752VY	Rev: 2.0
Title :	DIM_DDR4 SO-DIMM B1	
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 15 of 102	

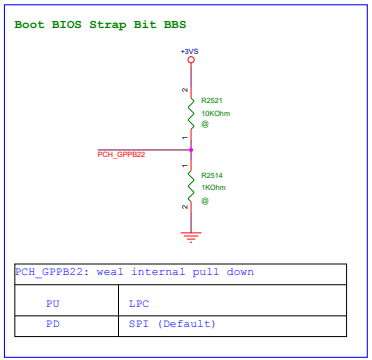


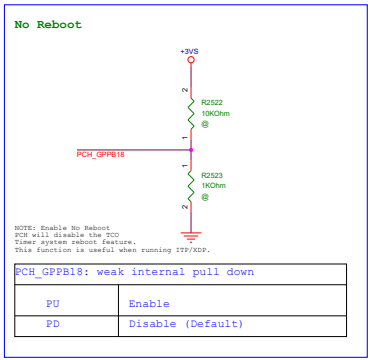


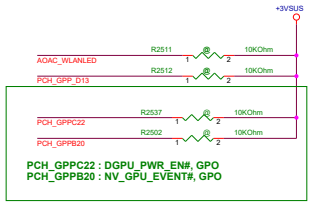


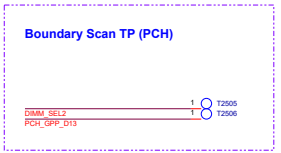
	Hynix(2Gb)	XXX (2Gb)	Micron(2Gb)	
DIMM_SEL0				
DIMM_SEL1				
DIMM_SEL2				

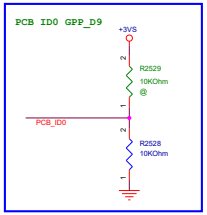
	HYNIX (4Gb) 03006-00011600 32Bit 1600 512M*8 1.35V HYNIX/H5TC4G83AFR-PBA	ELPIDA (4Gb)	Micron(4Gb) 03006-00011400 32Bit 1600 512M*8 1.35V MICRON/MT41K512M8RH-125:E	
DIMM_SEL0	L		L	
DIMM_SEL1	L		L	
DIMM_SEL2	H		L	

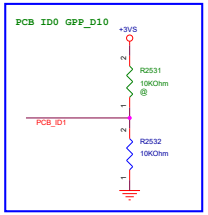


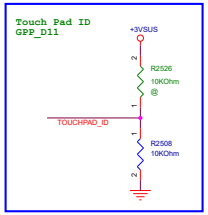


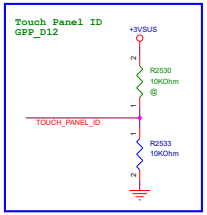


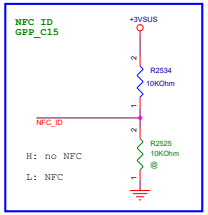




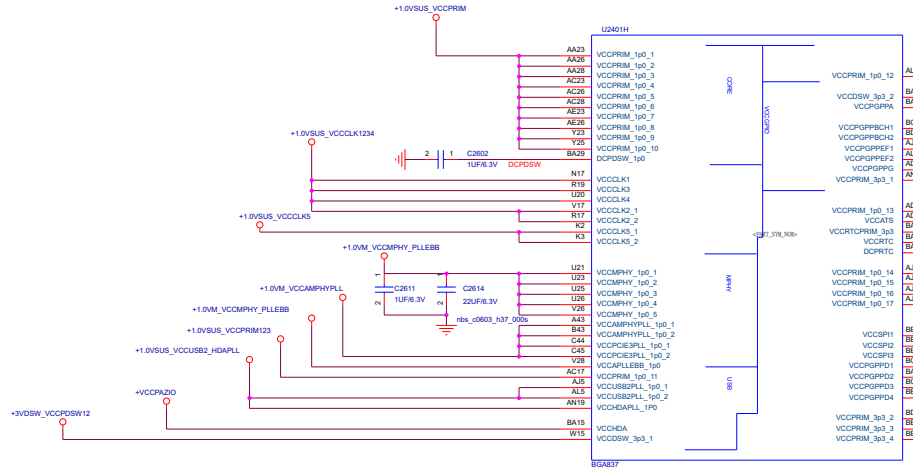


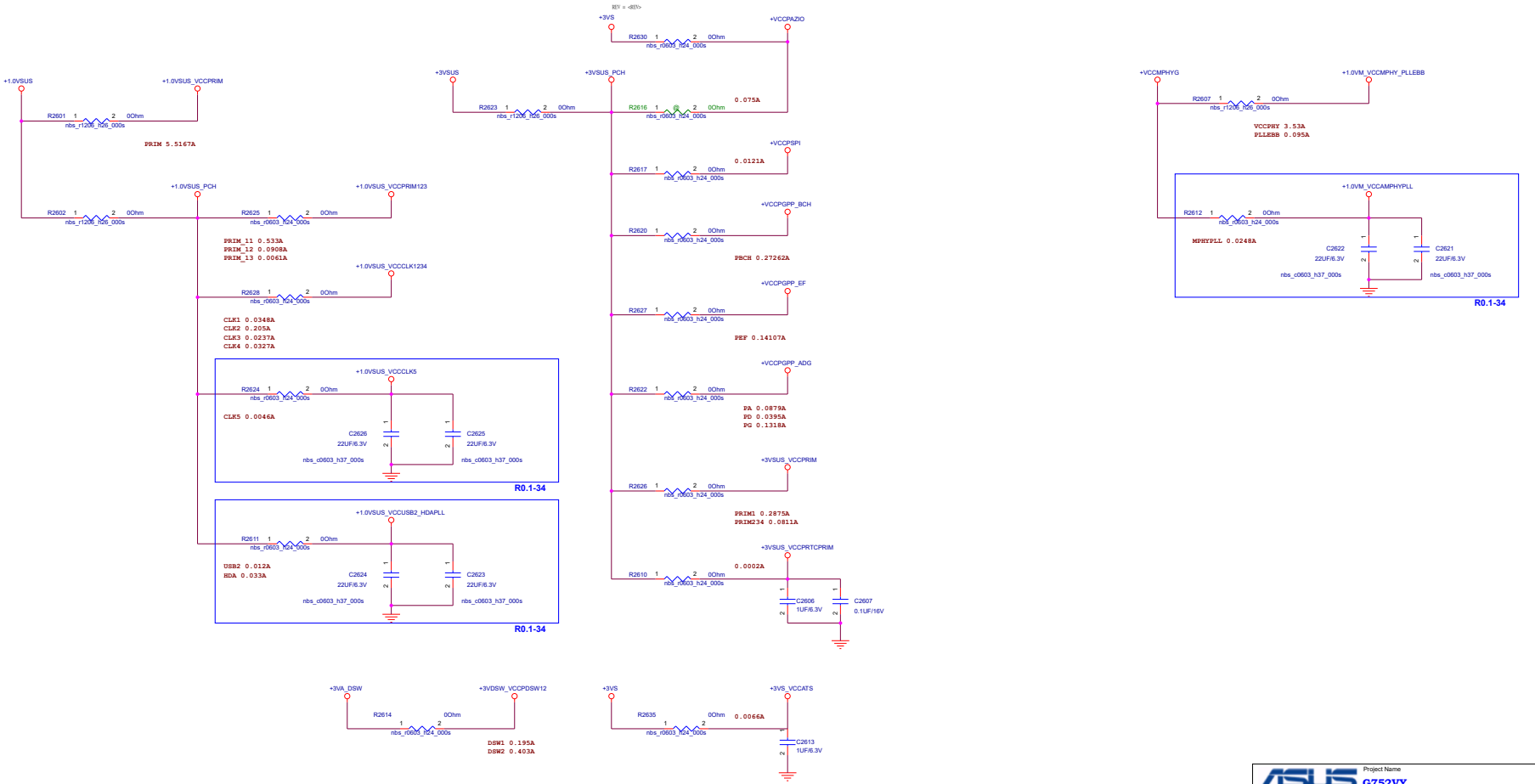






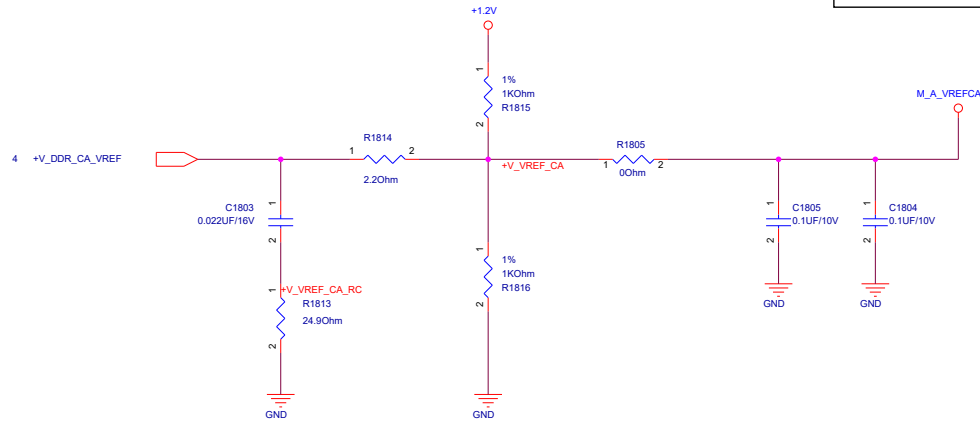
ASUS	Project Name: G752VY		Rev: 2.0
Title :	PCH-CPT(6)_GPIO,MISC		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Tuesday, July 21, 2015	Sheet 25 of 102		





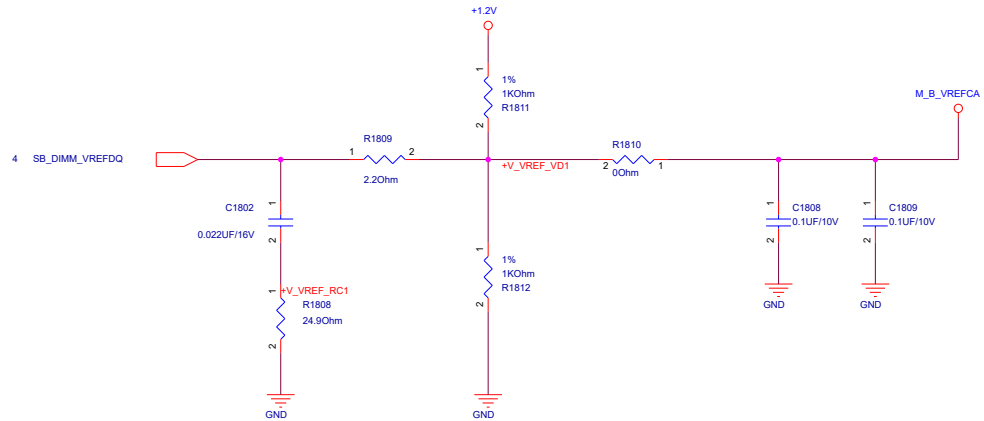
Project Name: G752VY		Rev: 2.0
Title: PCH-CPT(7)_POWER,GND		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Wendell_Lo
Date: Tuesday, July 21, 2015	Sheet 26 of 102	

SO-DIMM0 Vref

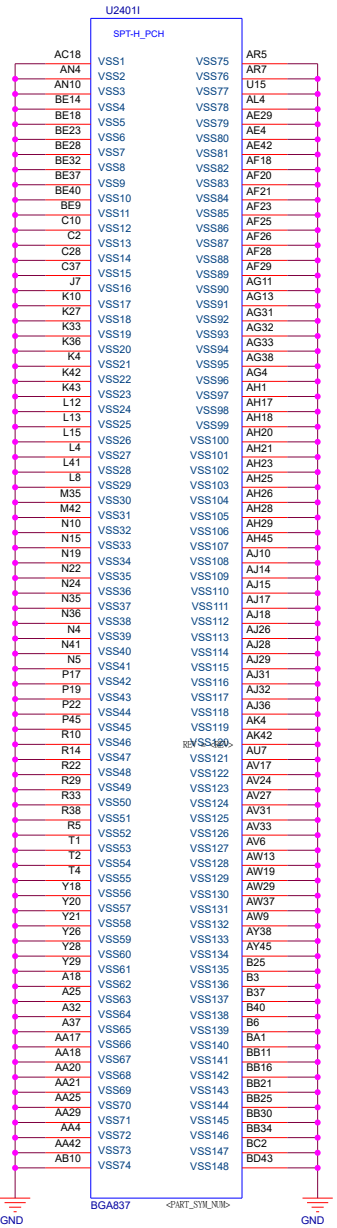


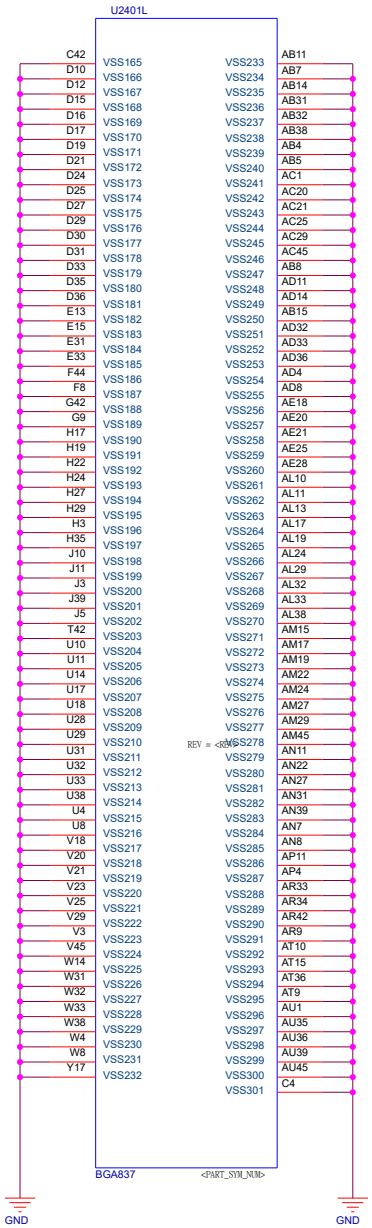
Main Source	1th PWR	2nd PWR
AC_BAT_SYS	+1.2V	M_A_VREFCA (0.6V From +1.2V)

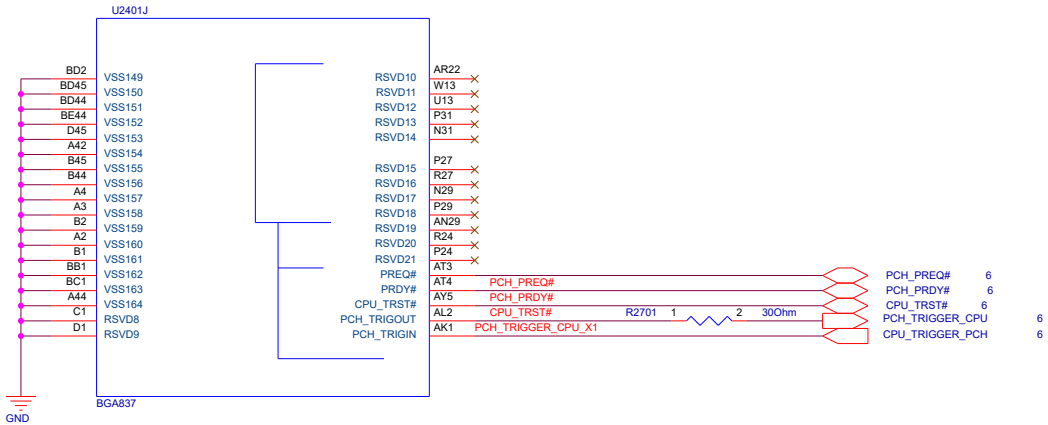
SO-DIMM1 Vref



ASUS	Project Name: G752VY		Rev: 2.0
Title : DIMM_CA/DQ Voltage			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Tuesday, July 21, 2015		Sheet 18 of 102	







REV = <REV>

REV = <REV>

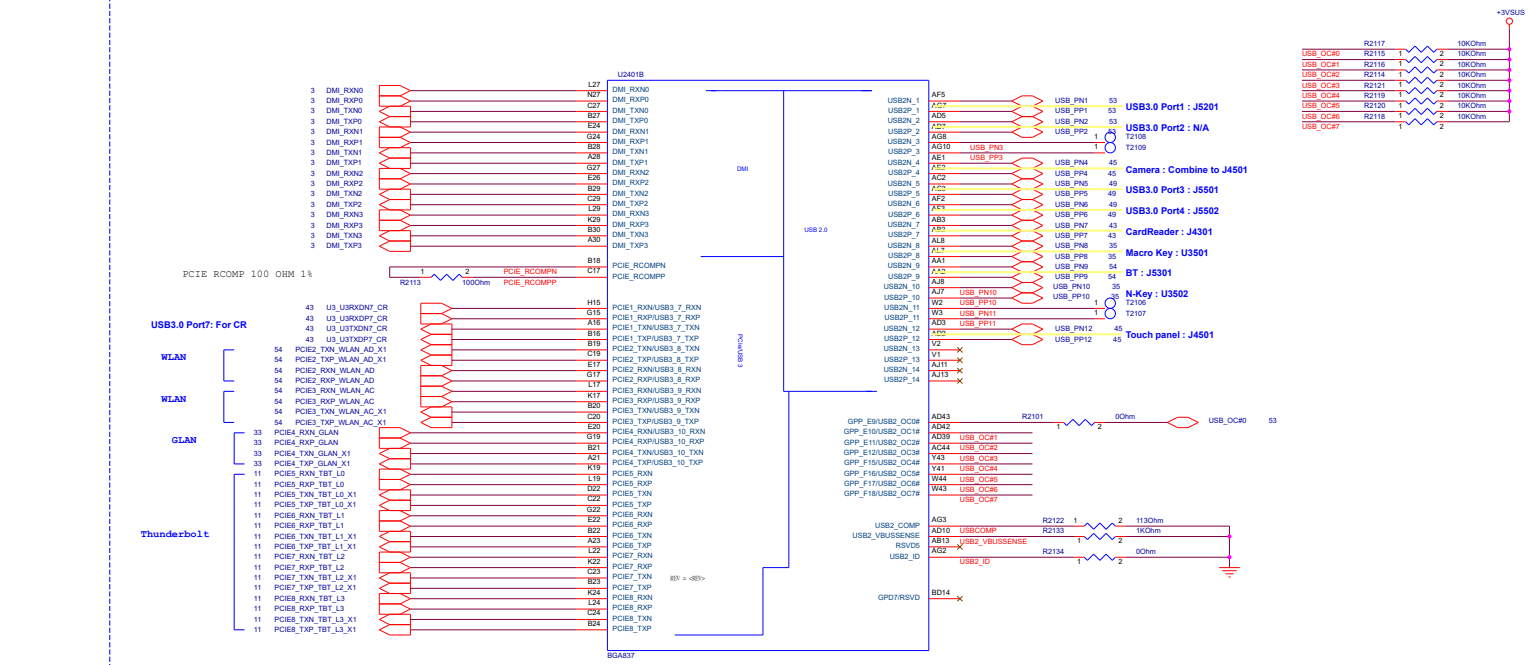
Project Name: G752VY			Rev: 2.0
Title : PCH-CPT(8)_POWER,GND			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Tuesday, July 21, 2015		Sheet 27 of 102	

Main Board

ASUS	Project Name: G752VY	Rev: 2.0
Title : PCH-XDP		
Size: B	Dept.: ASUSTeK COMPUTER INC. (I	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 29 of 102	

HSIO Setting

USB Setting



EC 8995

Only 3V Torlence

GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]

Can be adjusted to Open-Drain for port:

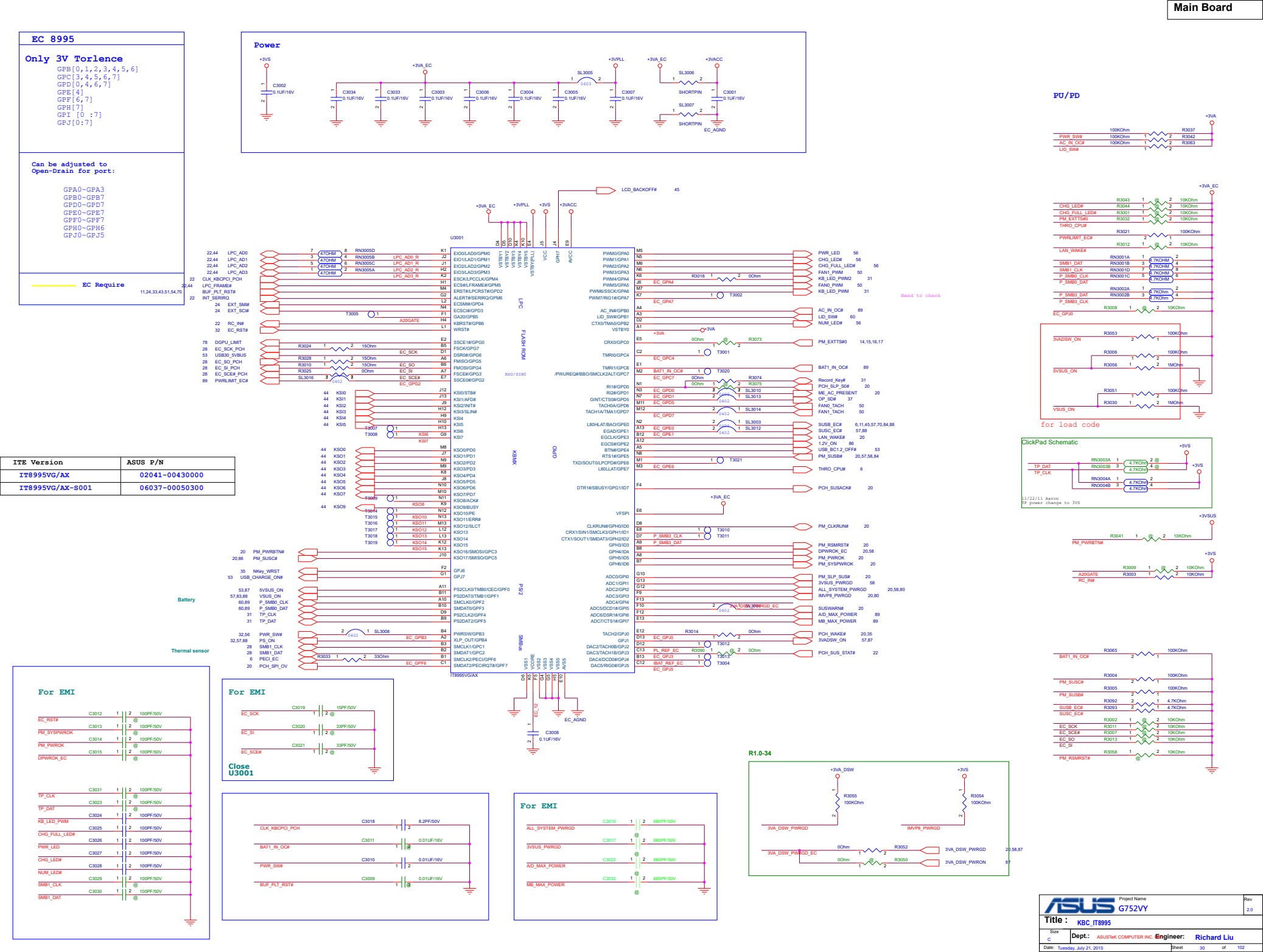
GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

EC Require

ITE Version	ASUS P/N
IT8995VG/AX	02041-00430000
IT8995VG/AX-S001	06037-00050300

Battery

Thermal sensor

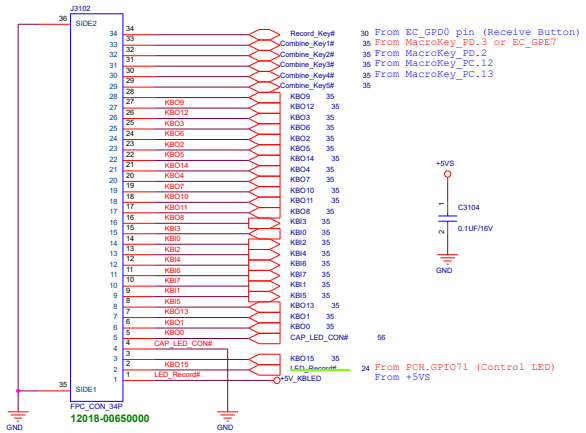


Project Name	G752VY	Rev	2.0
Title :	KBC_IT8995		
Size	C	Dept.:	ASUSTeK COMPUTER INC
Engineer:	Richard Liu		
Date:	Tuesday, July 21, 2015	Sheet	30 of 102

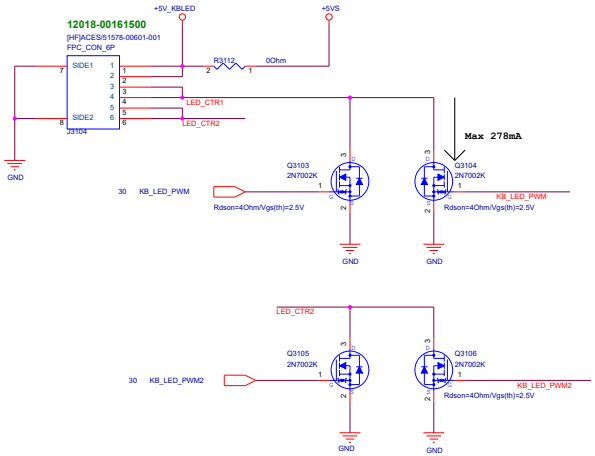
Main Board

Change Small KB Pin Define

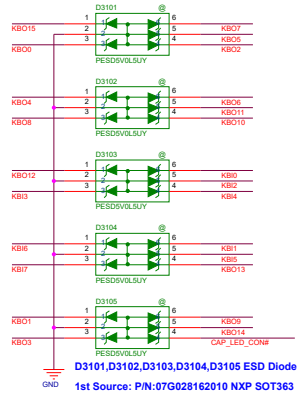
Keyboard Connector



Keyboard LED Connector



Reserved for EMI



D3101,D3102,D3103,D3104,D3105 ESD Diode

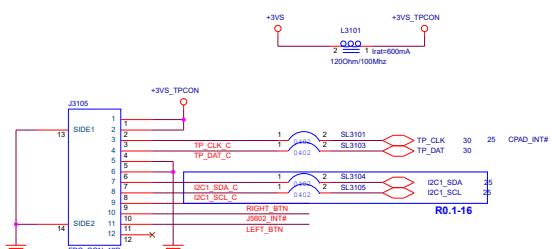
1st Source: P/N:07G028162010 NXP SOT363

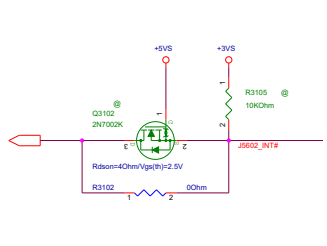
2nd Source: P/N: 07G028127010 AMAZING SC70-6L

Macro Key	KB Backlight	Macro Key LED Behavior
J3104.Pin6 LED_Combine	J3104.Pin4 KB_LED_PWM	Combine_Key[1,2,3,4]
No Set (0)	No Set (0)	LED OFF (0)
No Set (0)	Set (1)	LED OFF (0)
Set (1)	No Set (0)	Flash, then LED OFF(0)
Set (1)	No Set (0)	Flash, then LED ON(1)

To Touchpad

ClickPad Schematic

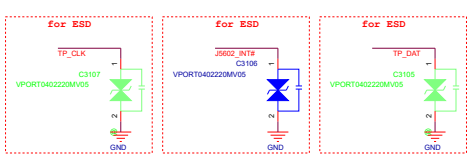




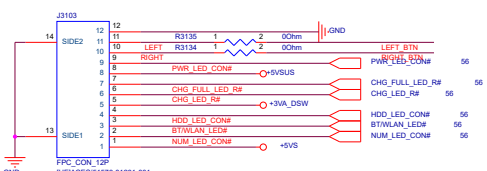
D3110 ESD Diode

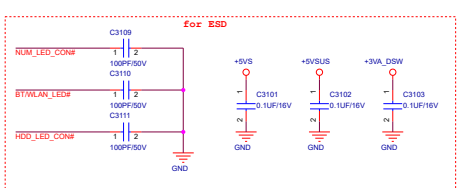
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

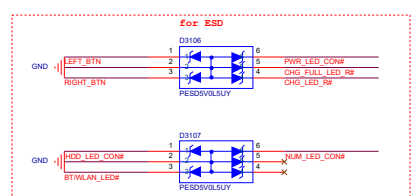
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D



To Touchpad Button







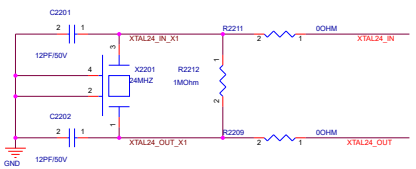
D3106,D3107 ESD Diode

1st Source: P/N:07G028162010 NXP SOT363

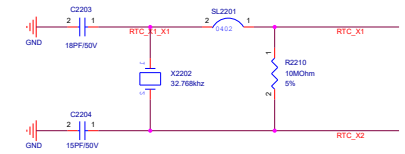
2nd Source: P/N: 07G028127010 AMAZING SC70-6L

ASUS	Project Name: G752VY	Rev: 2.0
Title : KBC_KB & TP		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 31 of 102	

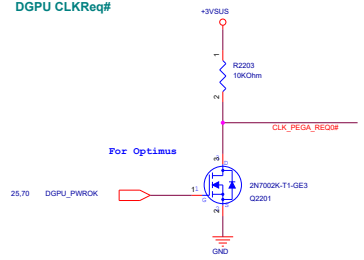
XTAL 24MHz



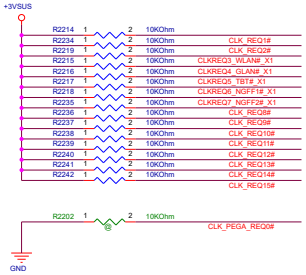
RTC CRYSTAL 32.768KHz

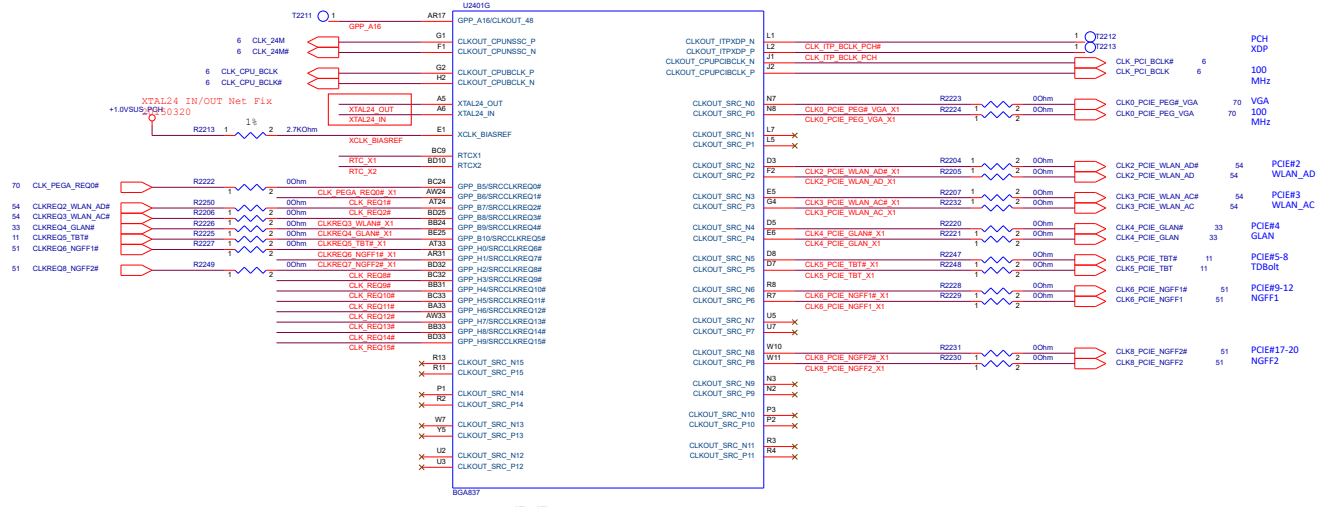


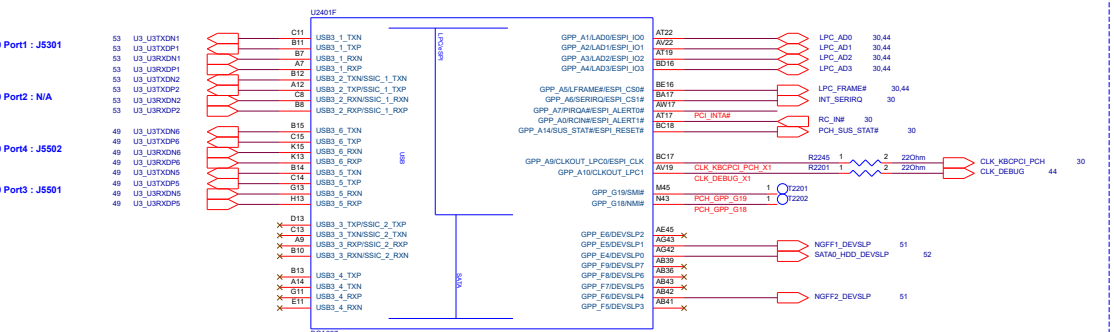
DGPU CLKReq#

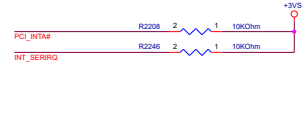


PCH CLKREQ Setting:



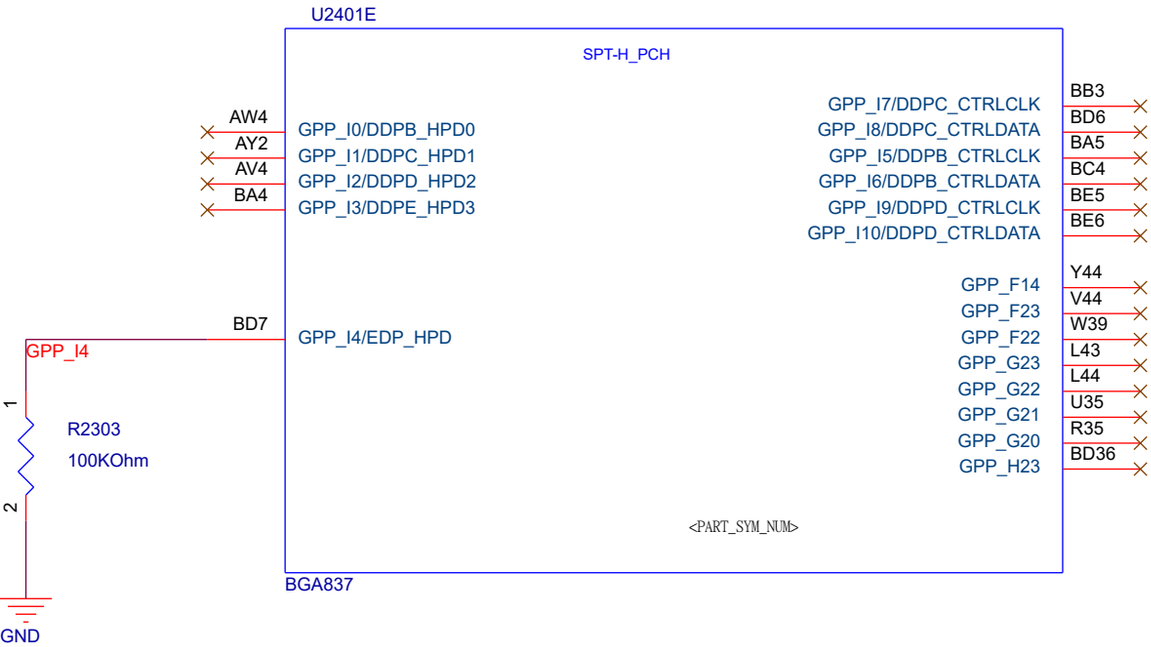






ASUS	Project Name: G752VY		Rev: 2.0
Title :	PCH-CPT(3)_FDI,DMI,SYS PWR		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Tuesday, July 21, 2015	Sheet 22 of 102		

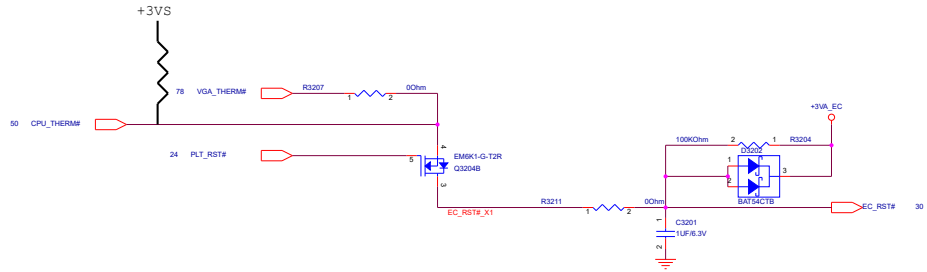
DDPD Strap Setting Update :
0 = Port D is not detected (Default)
1 = Port D is detected
20150309



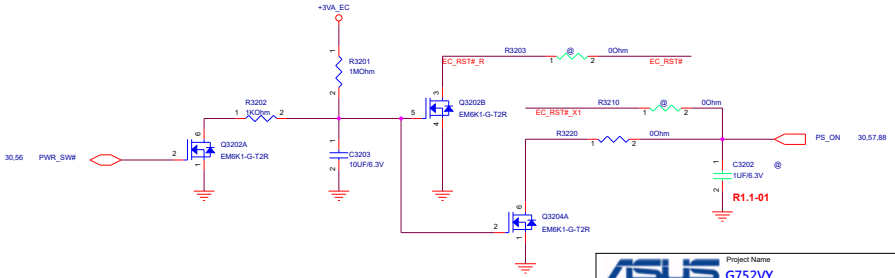
REV = <REV>

ASUS	Project Name: G752VY	Rev: 2.0
Title : PCH-CPT(4)_CRT,eDP,PCI,DP		
Size: A	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 23 of 102	

EC Reset Circuit



Embedded Battery Design_Reset Circuit



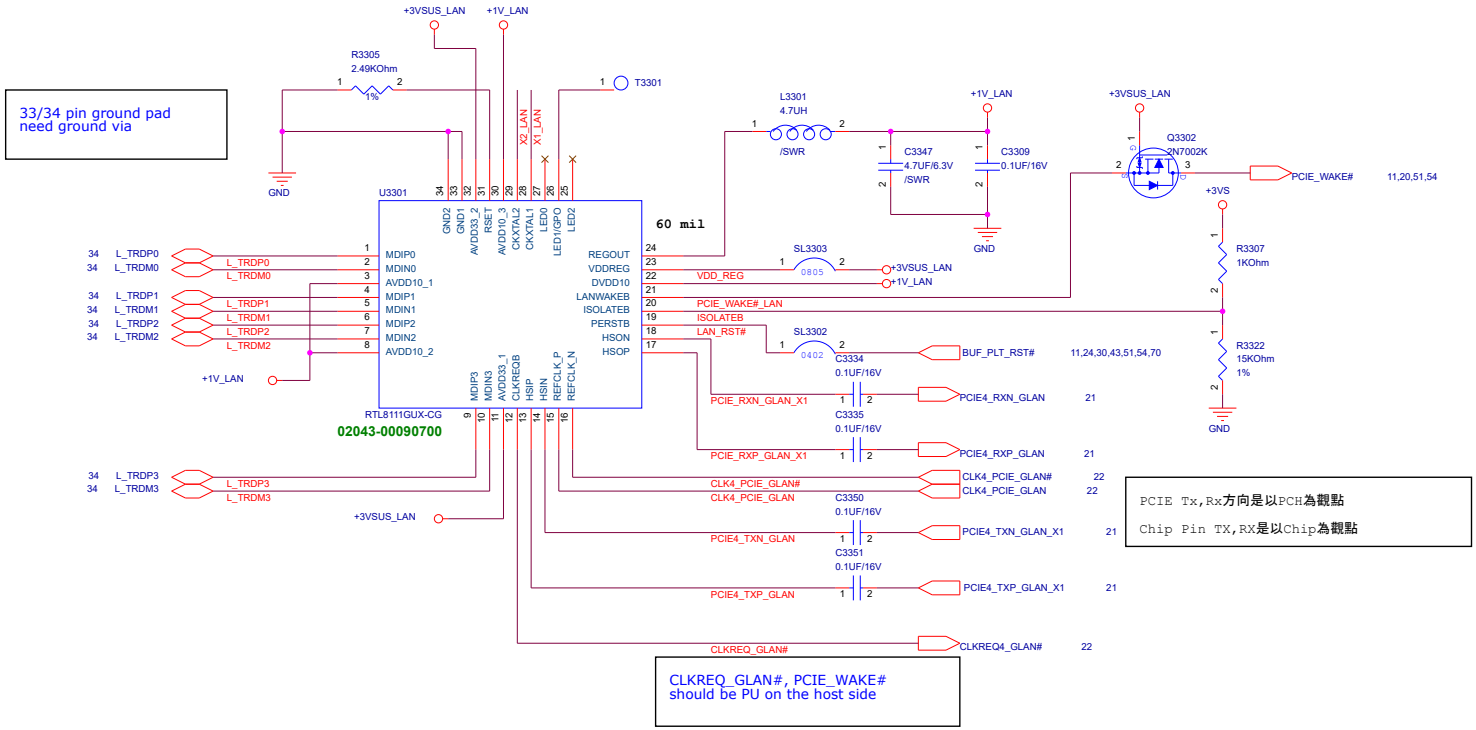
Project Name: G752VY		Rev: 2.0
Title : RST Reset Circuit		
Size: A	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 32 of 102	

Main Board

The distance from U3301.24 to L3301 within 200 mil.

The distance from L3301 to C3347 within 200 mil.

33/34 pin ground pad need ground via

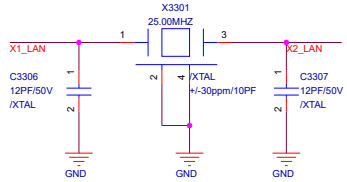


PCIE Tx,Rx方向是以PCH為觀點

Chip Pin TX,RX是以Chip為觀點

CLKREQ_GLAN#, PCIE_WAKE# should be PU on the host side

07G010272501

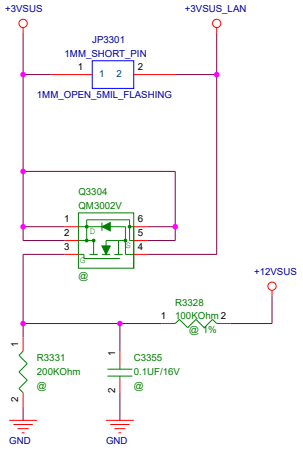


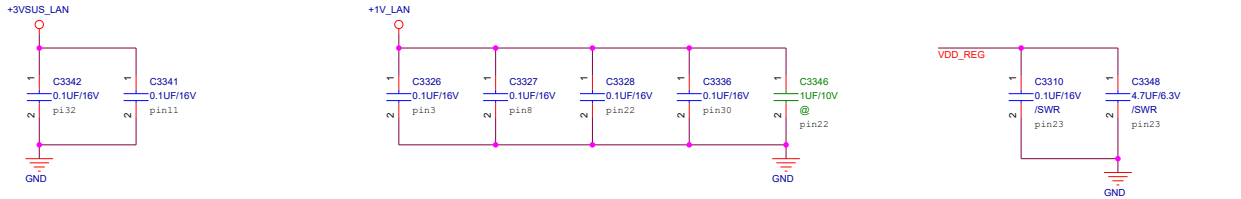
X3301: 25MHZ +/-30ppm/10pF (3225)

1st: P/N:07G010272501 TXC/7V25000011

2nd: P/N:07G010952500 HOSONIC/E3FB25

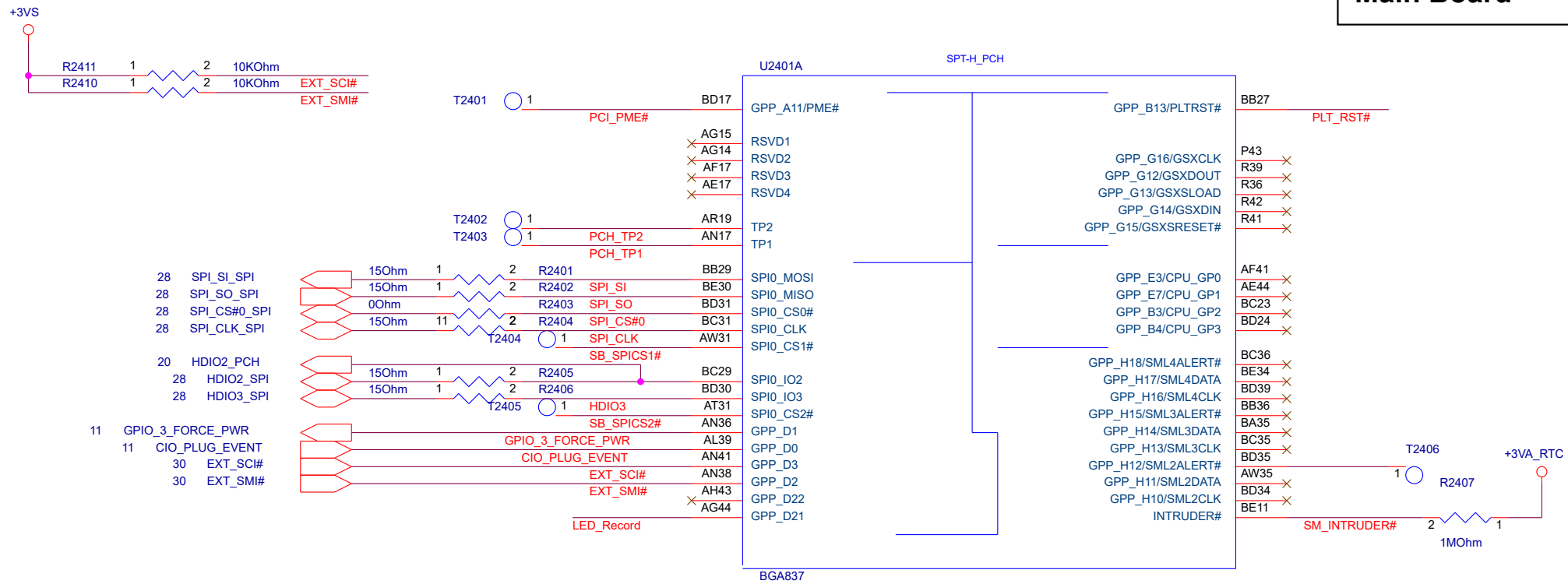
Realtek suggests 3V_LAN raise time >1ms





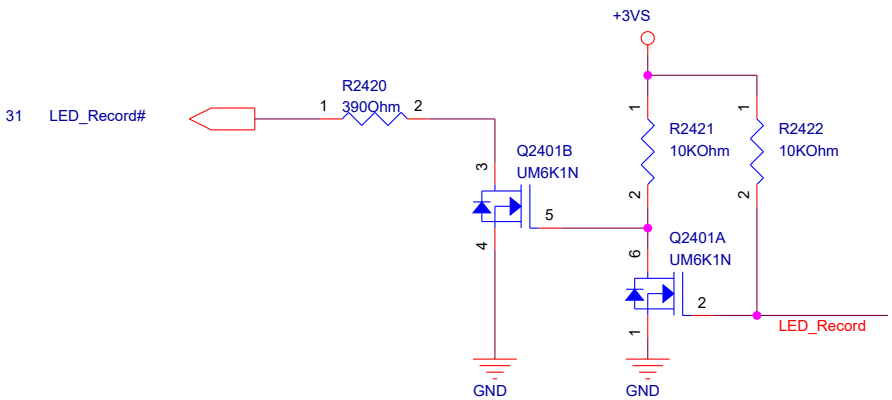
C3348, C3310 close to pin 23 reserved for SWR mode

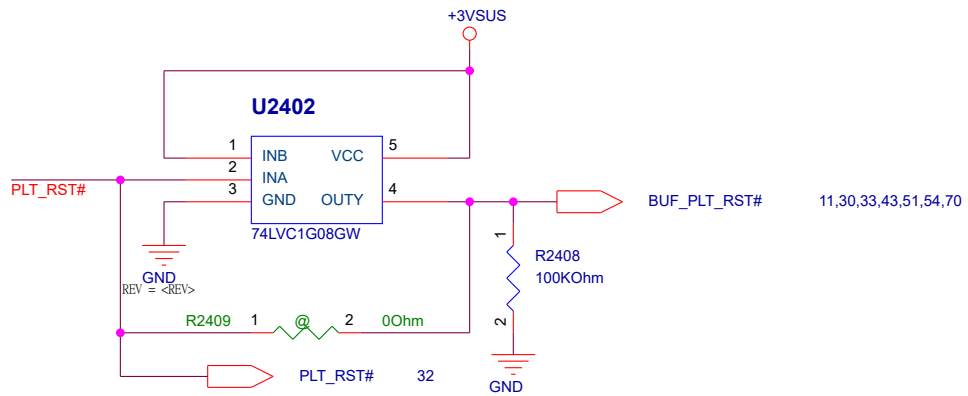
ASUS	Project Name: G752VY	Rev: 2.0
Title : LAN RTL8111GUX-CG		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 33 of 102	



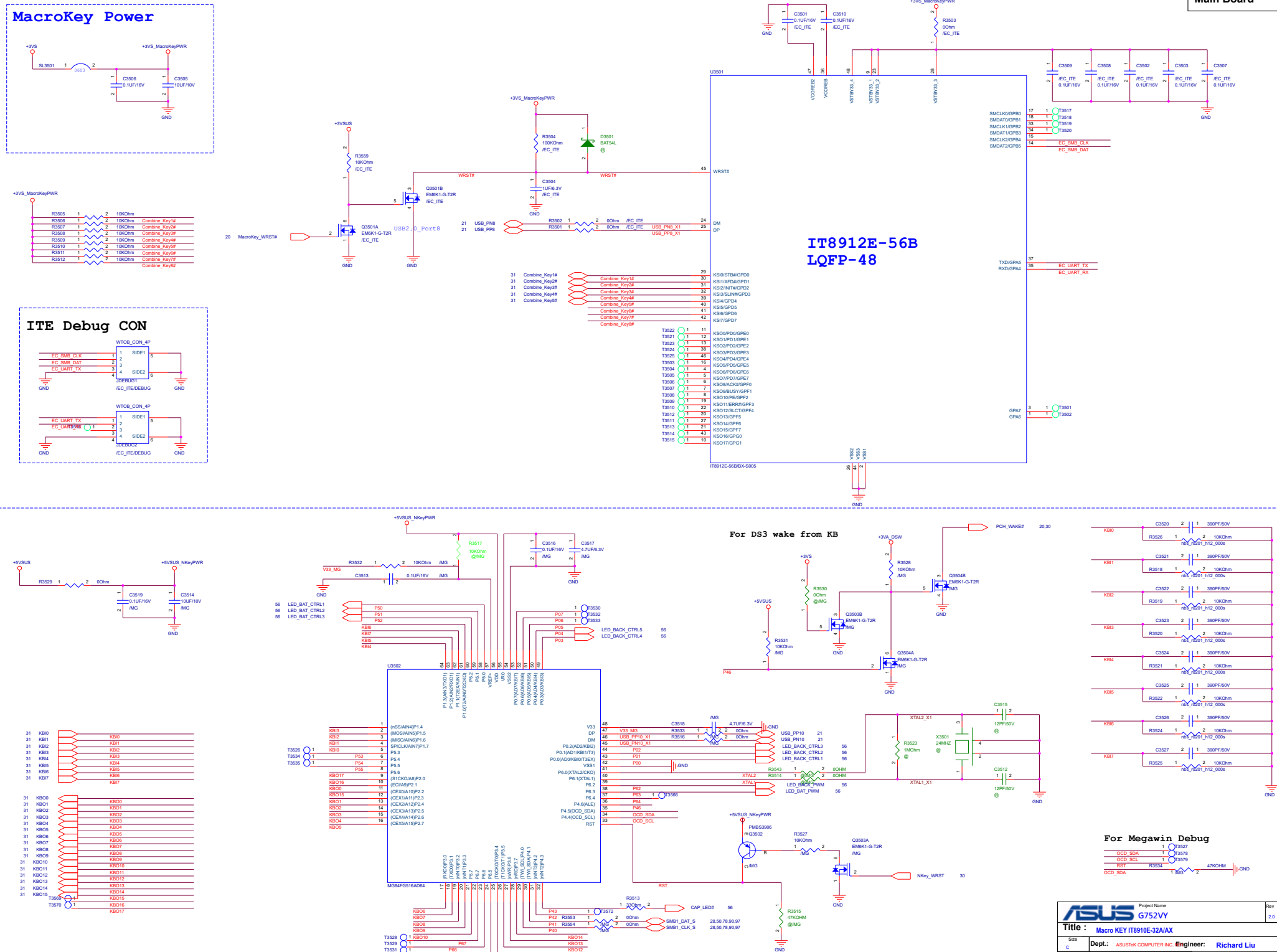
Record Key LED Control Circuit

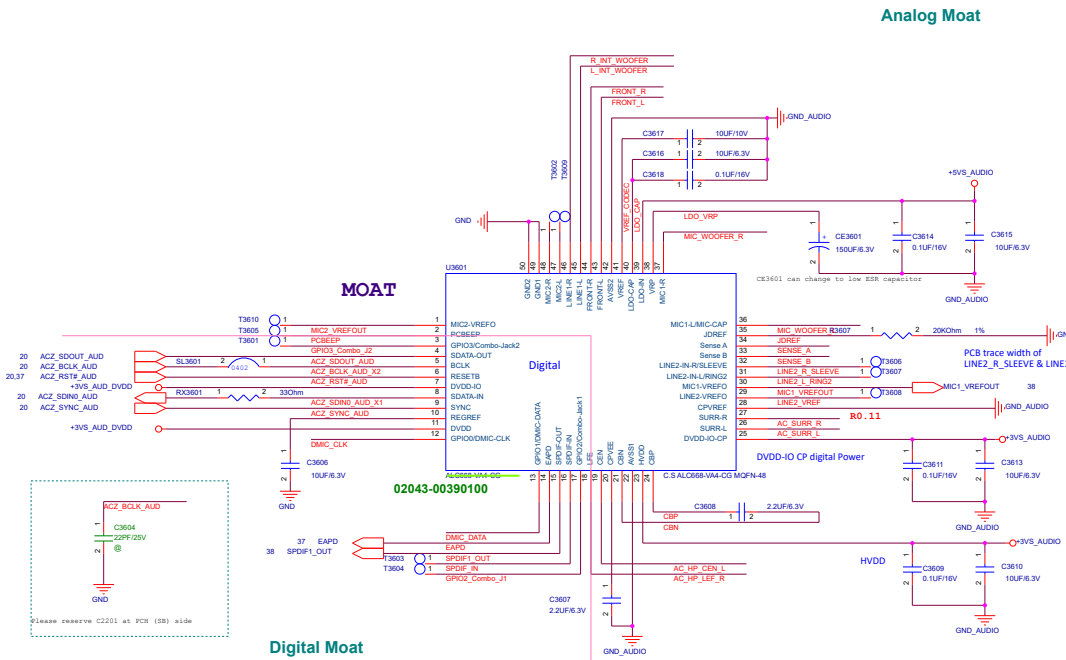
LED_Record# of Current :
(5-2.35) / 390 = 6.8mA

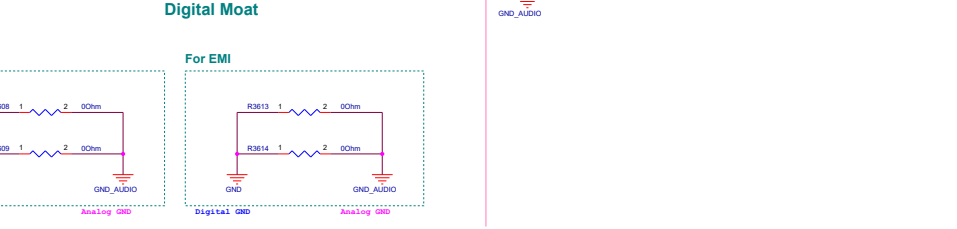


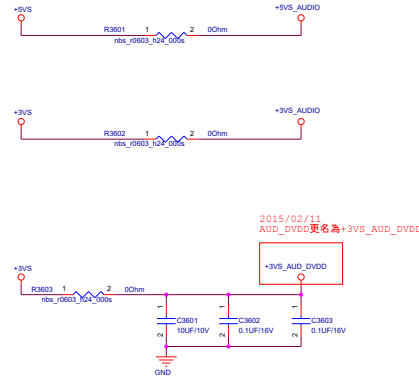


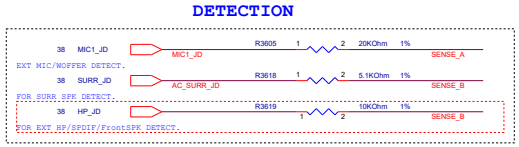
ASUS	Project Name: G752VY	Rev: 2.0
Title : PCH-CPT(5)_LPC,SPI,SMBUS		
Size: A	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 24 of 102	

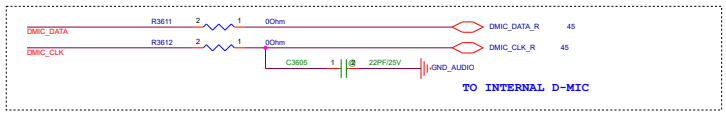

MacroKey Power
ITE Debug CON
IT8912E-56B
LQFP-48
IT8912E-56B/BX-S005
For DS3 wake from KB
For Megawin Debug
MG84FG516AD64
USB2.0_Port8
Project Name G752VY
Rev 2.0
Title : Macro KEY IT8910E-32A/AX
Size C
Dept.: ASUSTeK COMPUTER INC.
Engineer: Richard Liu
Date: Tuesday, July 21, 2015
Sheet 35 of 102

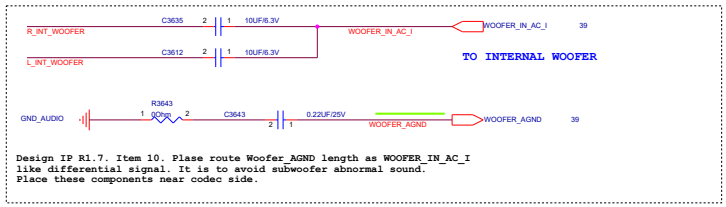






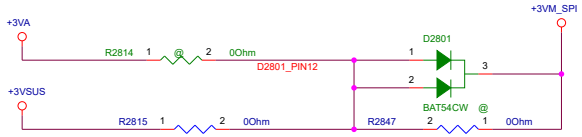






ASUS	Project Name: G752VY		Rev: 2.0
Title : AUD ALC668-CG			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Tuesday, July 21, 2015	Sheet 36 of 102		

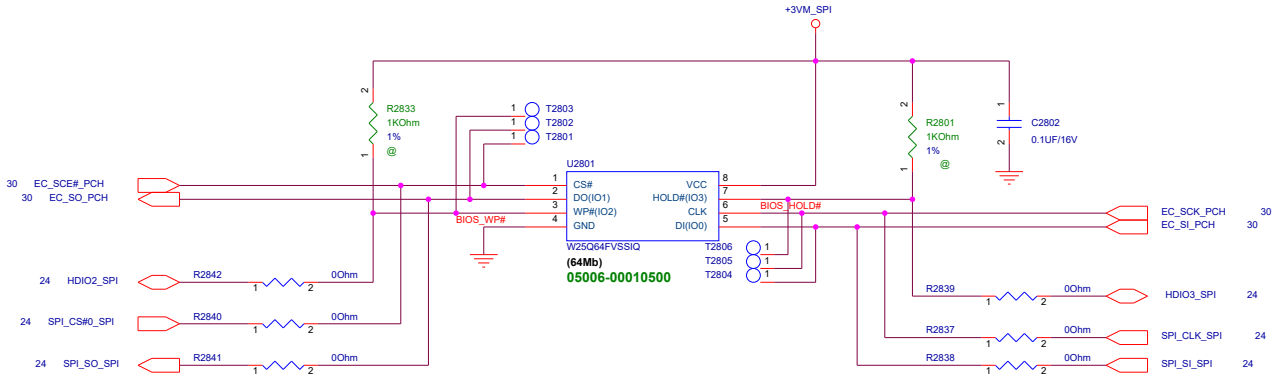
SPI Power



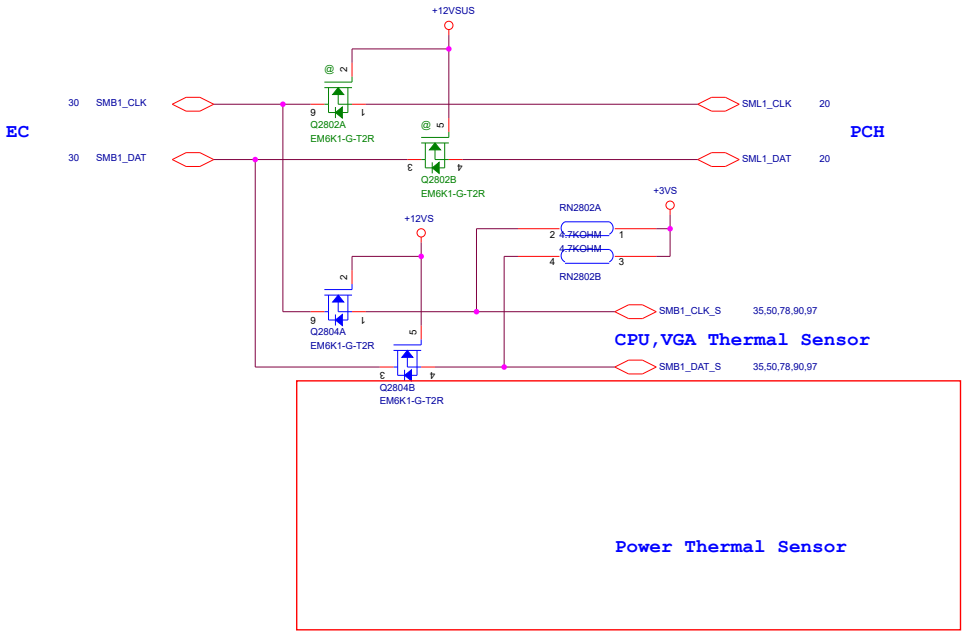
PCH_SPI_IO3 Signal Should PD 100Ω Before RSMRST# High
20150313

1st SPI ROM

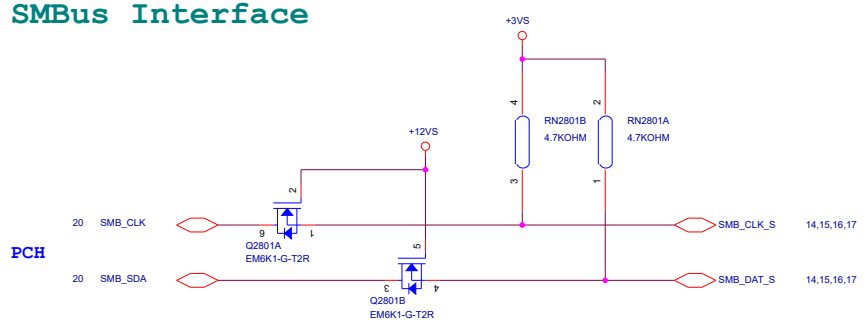
Main: 05006-00010500 (fixed quad bit)



System Management Interface



SMBus Interface



SMB1_CLK Level Shift Fix For PWR Thermal Sensor
Add Q2806, RN1804
20150320

Project Name: G752VY		Rev: 2.0
Title : PCH-SPI ROM,OTH		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 28 of 102	

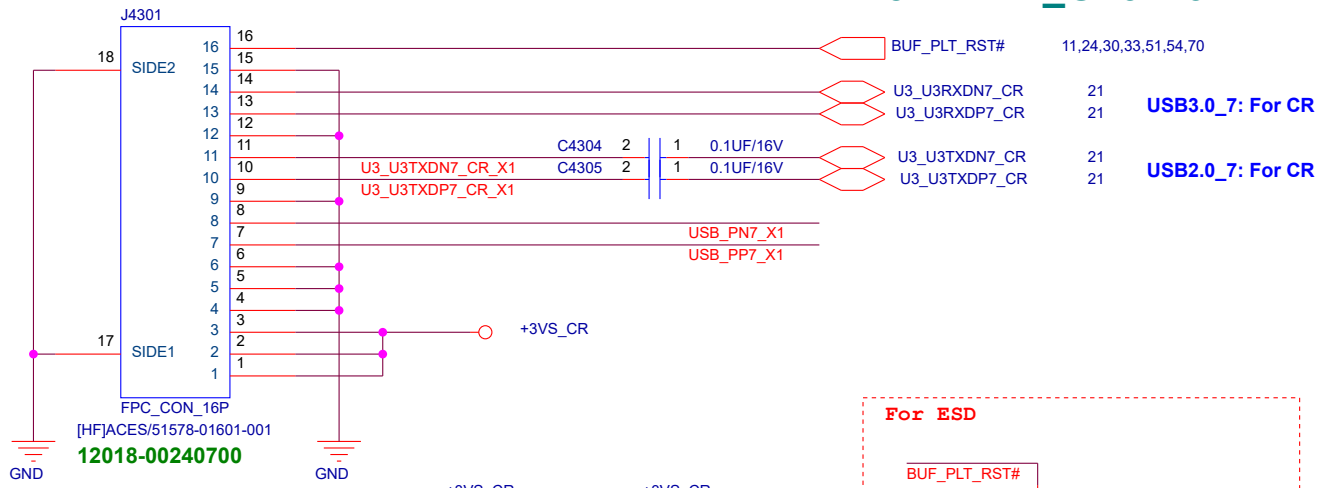
Main Board

ASUS	Project Name: G752VY	Rev: 2.0
Title : NB*		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 41 of 102	

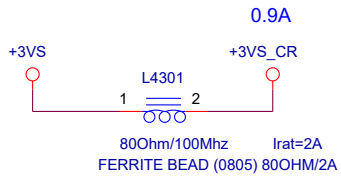
CR I/O Conn. (MB)

Main Board

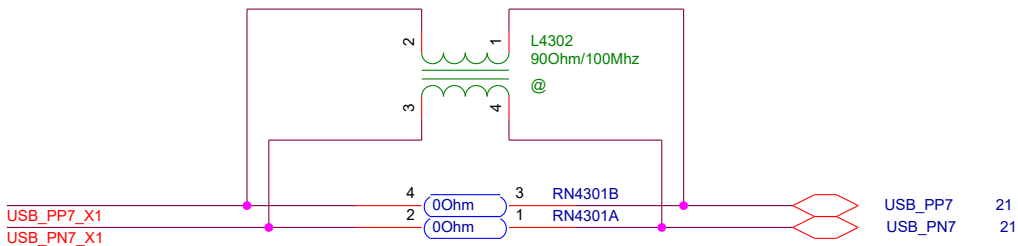
To CB BD_GL3213



CardReader PWR

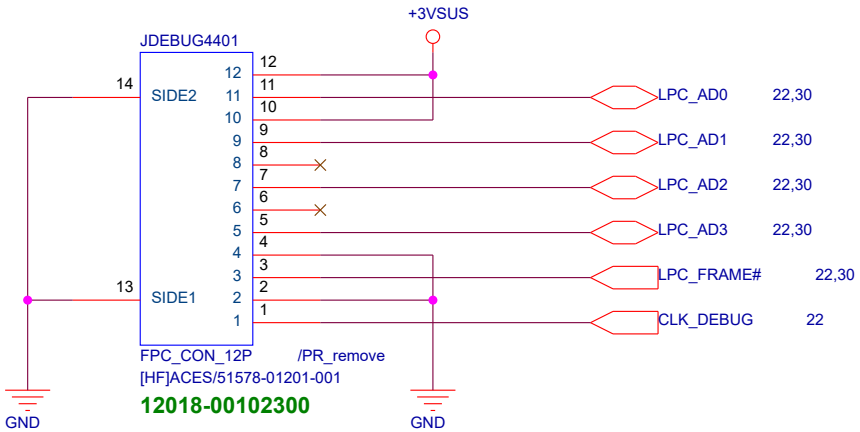


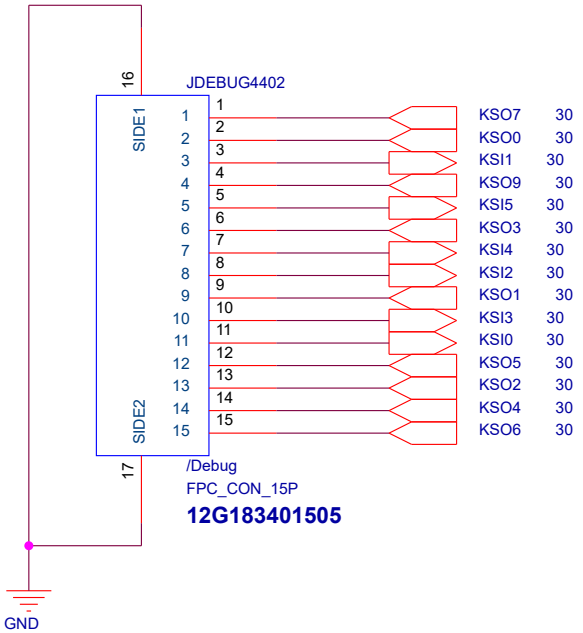
For EMI



Project Name: G752VY		Rev: 2.0
Title: CB IO CON		
Size: A	Dept.: ASUSTeK COMPUTER INC. (MB)	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 43 of 102	

LPC Debug Port



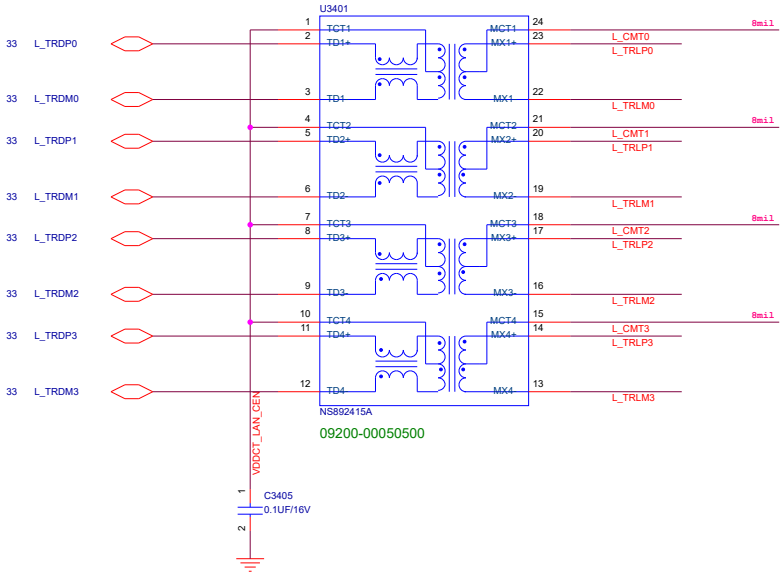


JDEBUG4401 Connector (MP USE)

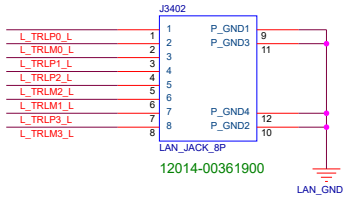
1st Source: P/N:12018-00102300 ACES/51578-01201-001

2nd Source: P/N:12018-00102100 ENTERY/6705K-Y12N-00L

ASUS	Project Name: G752VY	Rev: 2.0
Title : BUG NewCard & LPC		
Size: A	Dept.: ASUSTeK COMPUTER INC. NBBU	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 44 of 102	



LAN Connector

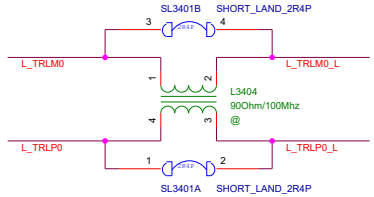


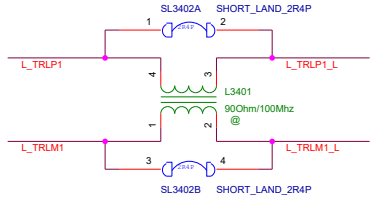
J3402 LAN Jack

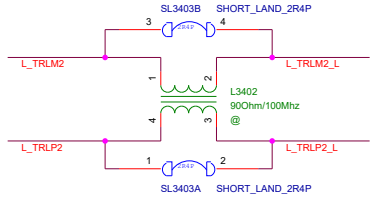
1st Source: P/N:12014-00161700 FOXCONN/JM3611-NS640003-7H

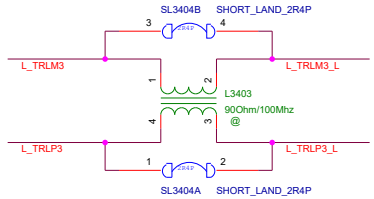
2nd Source: P/N:12014-00035500 SINGATRON/2RJ1648-000111F

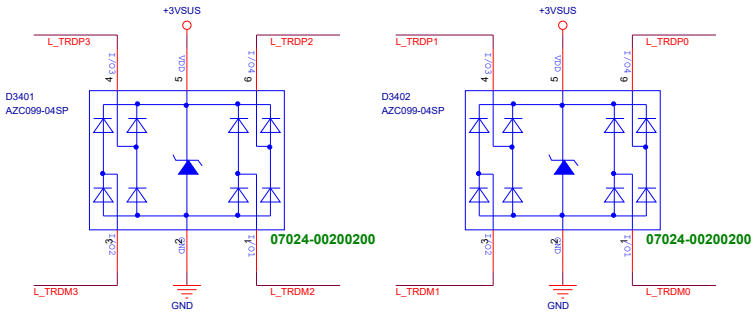
TEST POINT_LAN
Follow Factory ATS test







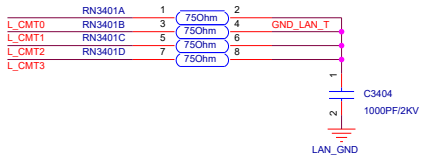




D3401,D3402 ESD Diode

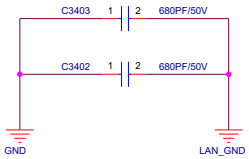
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D



GND_LAN_T 上禁止加任何零件

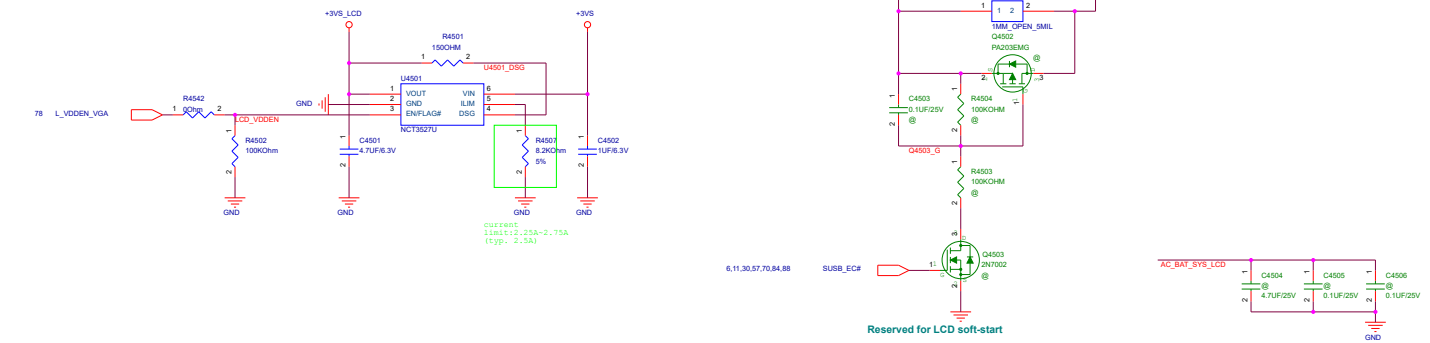
2012/2/16 EMI



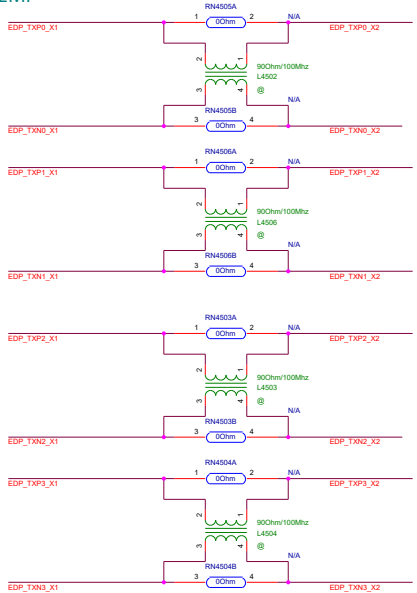
Place near chassis GND

ASUS	Project Name: G752VY	Rev: 2.0
Title : LAN RJ45 Conn.		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 34 of 102	

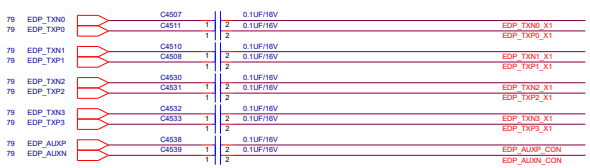
LCD Power switch



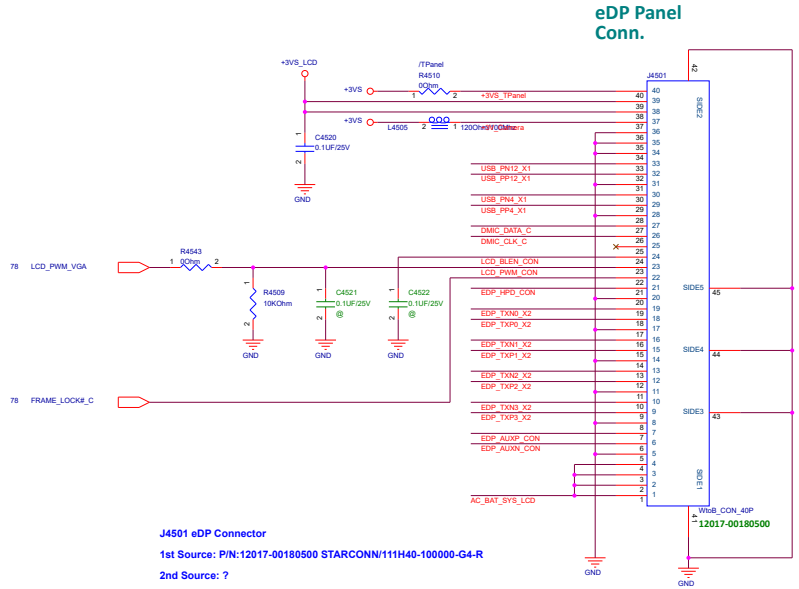
For EMI



eDP circuit



eDP Panel

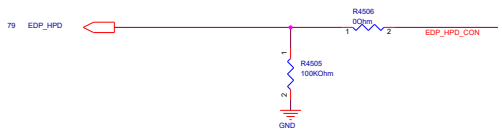


J4501 eDP Connector

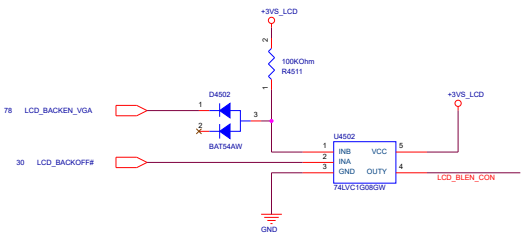
1st Source: P/N:12017-00180500 STARCONN/111H40-100000-G4-R

2nd Source: ?

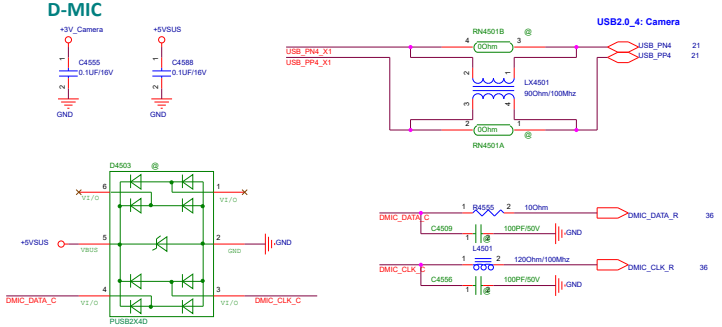
eDP_HPD



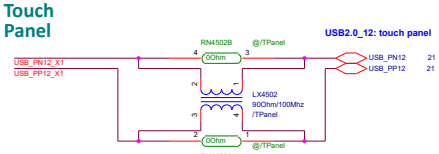
eDP_BL EN



Camera & D-MIC



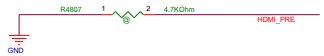
Touch Panel



Project Name: G752VY			Rev: 2.0
Title : eDP CON			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Tuesday, July 21, 2015	Sheet 45 of 102		

ASUS	Project Name: G752VY	Rev: 2.0
Title : CRT Conn.		
Size: A	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 46 of 102	

HDMI Active-Level Shift

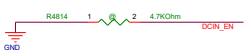


Output pre-emphasis setting; Internal pull up, 3.3V I/O.
L: Pre-emphasis =2.5dB
H: Default, No Pre-emphasis

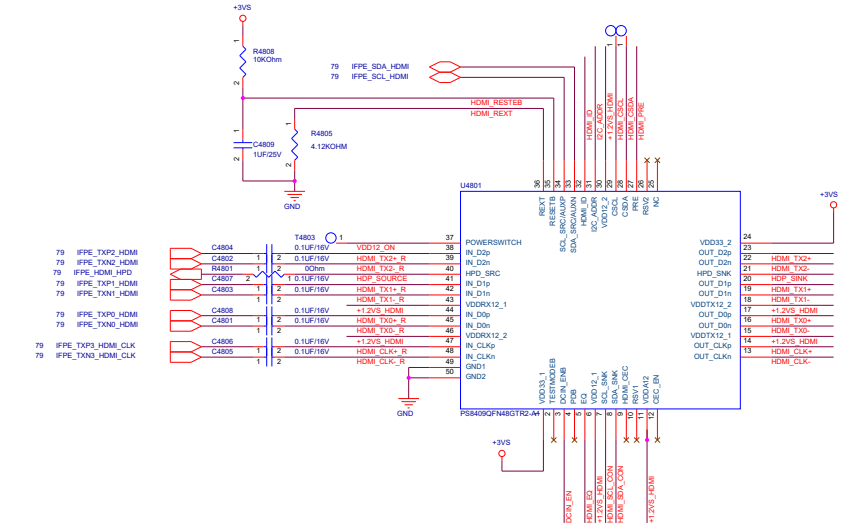
Receiver equalization setting; Internal pull up , 3.3V I/O.
L: Compensaton for channel loss up to 13dB
H: Default , Compensation for channel loss up to 17dB
M: Compensation for channel loss up to 11dB

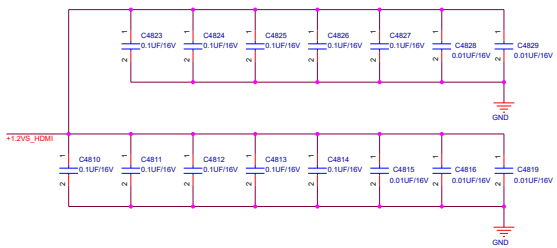
I2C Slave Address selection; Internal pull down, 3.3V I/O:
L: Default, Slave address 0x10-0x2F.
H: Alternative salve address 0x90-0x9F, 0xD0-0xDF.

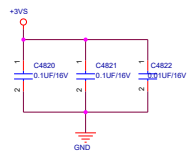
HDMI_ID enable ; Internal pull down , 3.3V I/O.
L: Default, HDMI ID enable
H: HDMI ID disable



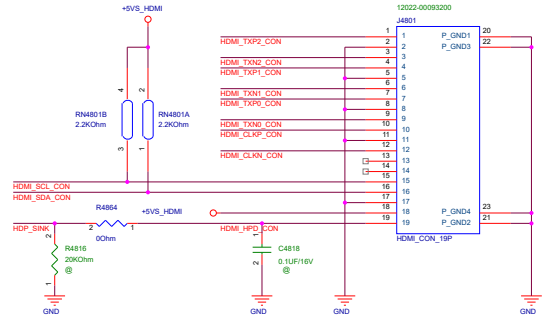
DC coupling enable; Internal pull up, 3.3V I/O.
L: DC coupling input
H: Default,AC coupling input



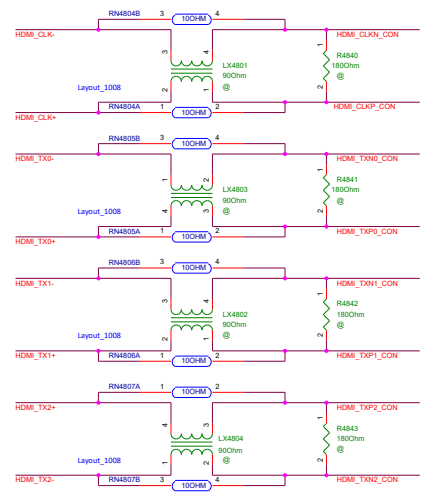




HDMI Conn.

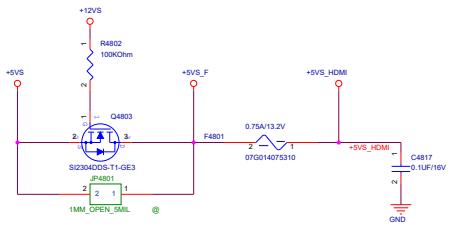


HDMI EMI



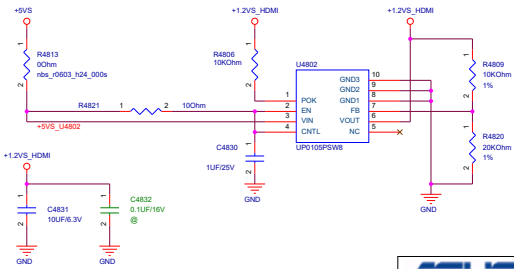
N56V C.M Choke : M 09G092090110

HDMI PWR_+5VS_HDMI



12/21/11
For HDMI Design IP R1.4
Del P4801
Add Q4803 07G005047212
F4801=>07G014075310
L4802=>09G013120802

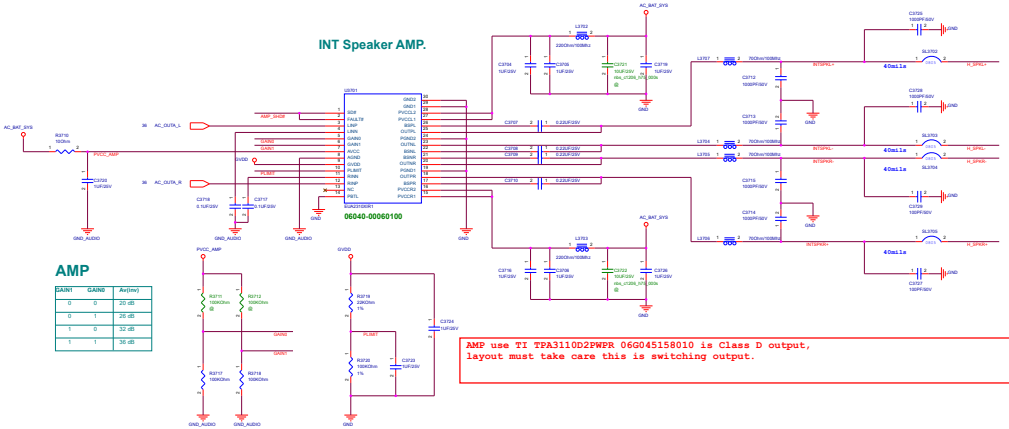
HDMI LDO 1.5VS



ASUS	Project Name G752VY		Rev 2.0
Title : HDMI Conn.			
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Tuesday, July 21, 2015	Sheet 48 of 102		

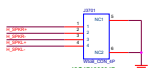
Main Board

INT Speaker AMP.



INT Left & Right Speakers

INTERNAL SPK Conn.

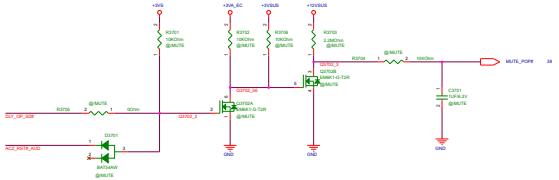


AMP

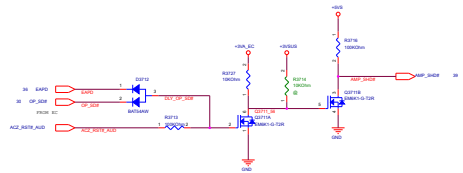
GAIN1	GAIN0	Av(inv)
0	0	20 dB
0	1	26 dB
1	0	32 dB
1	1	36 dB

AMP use TI TPA3110D2PWPR 06G045158010 is Class D output,
layout must take care this is switching output.

EXT JACK MUTE CONTROL



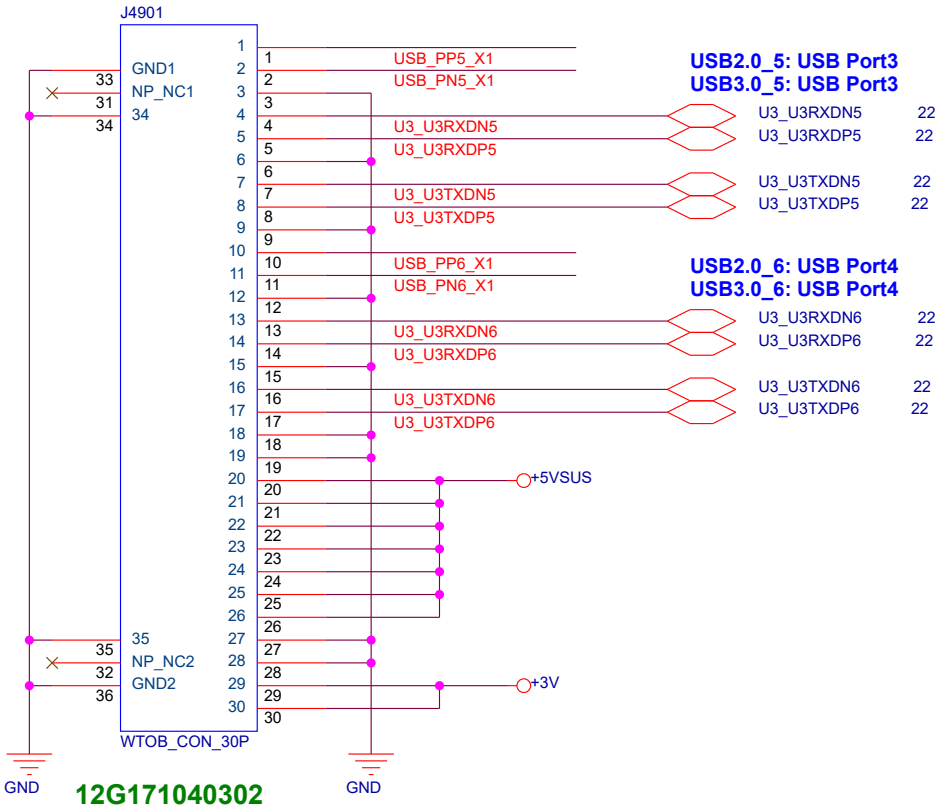
INT SPK MUTE CONTROL



ASUS	Project Name: G752VY		Rev: 3.0
Title : AUD INT SPK & MIC			
Size: A3	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Wednesday, July 23, 2014	Sheet: 37 of 100		

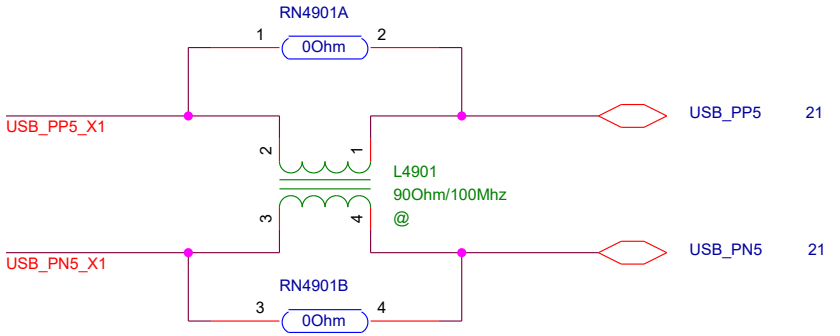
To USB3.0 IO BD on Page 55

To USB3.0 I/O Board (PAGE55)

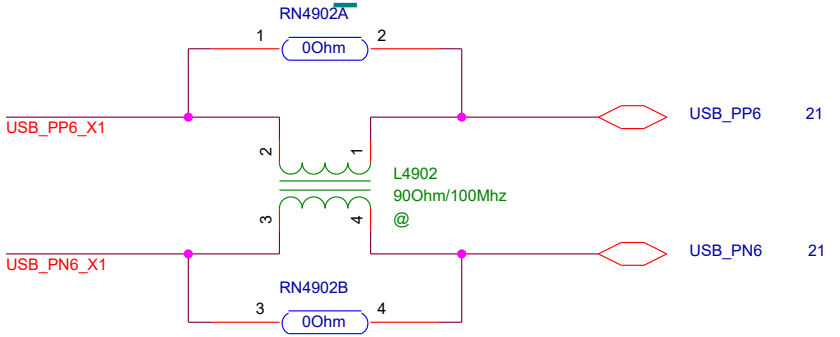


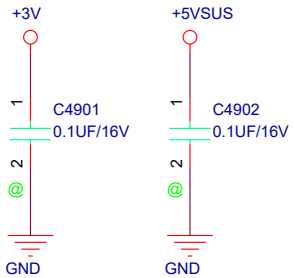
12G171040302

USB3.0 Port3_J5501



USB3.0 Port4_J5502

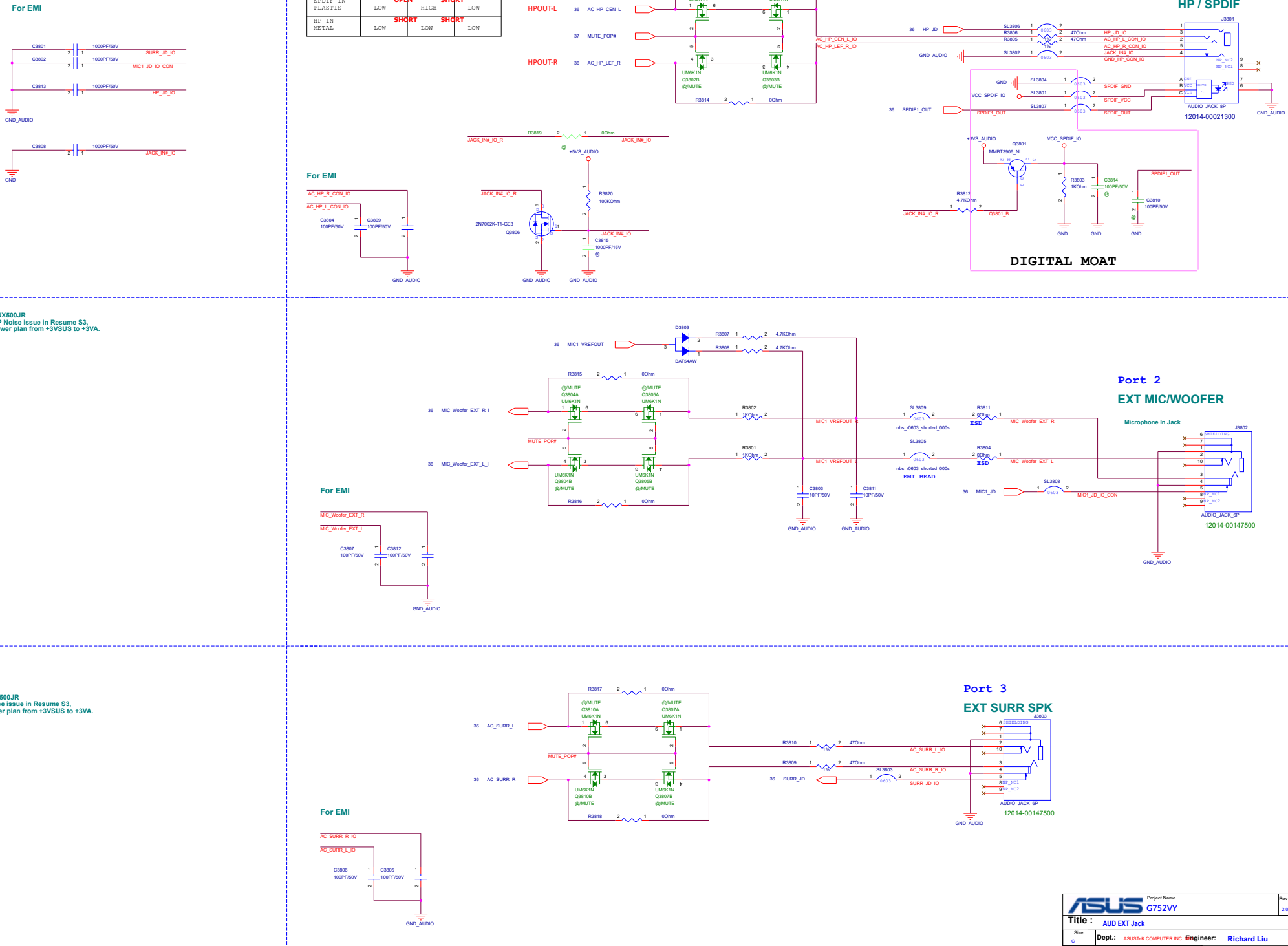




Project Name: G752VY			Rev: 2.0
Title : USB3.0 IO CON			
Size: A	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Tuesday, July 21, 2015	Sheet 49 of 102		

HP & SPDIF DETECT RULE.

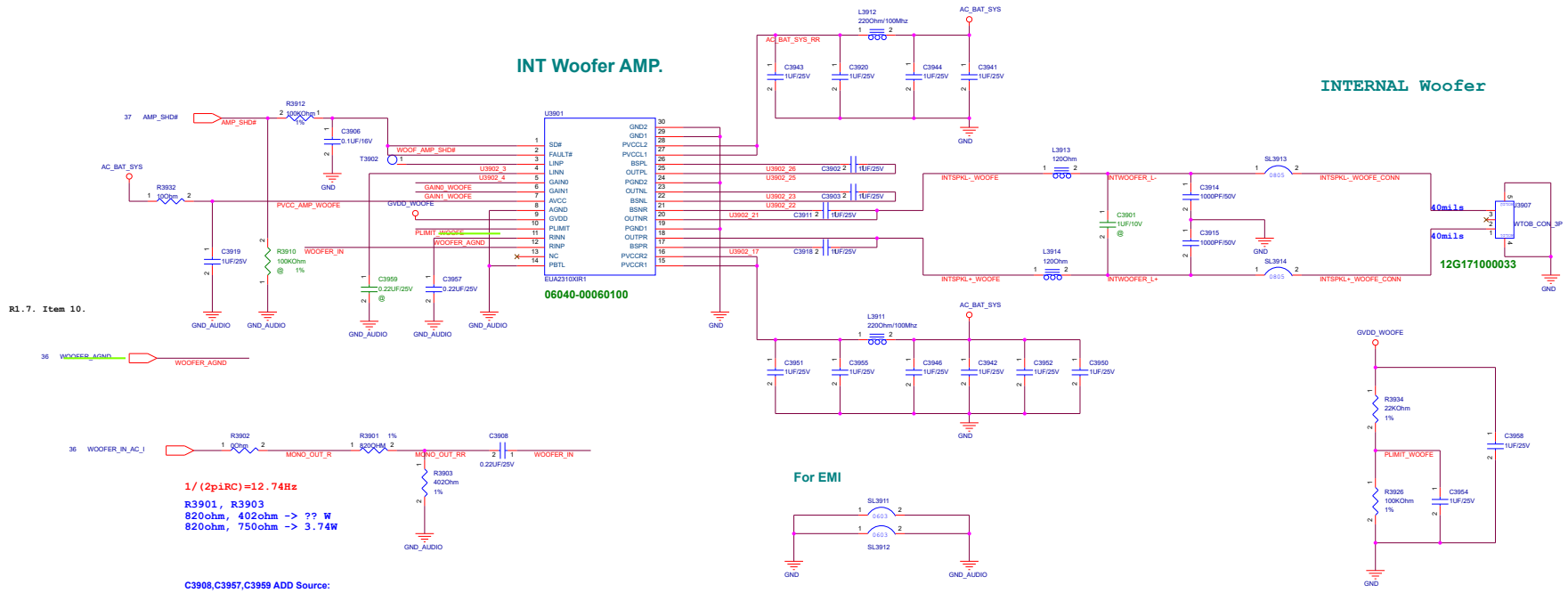
	M 5	M 6	M 7
SPDIF IN PLASTIS	OPEN LOW	SHORT HIGH	LOW
HP IN METAL	SHORT LOW	SHORT LOW	LOW

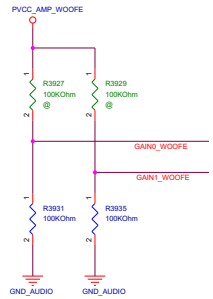


2013/6/18 NX500JR
Fix HP POP Noise issue in Resume S3,
Change Power plan from +3VSUS to +3VA.

2013/6/18 NX500JR
FIX POP Noise issue in Resume S3,
Change Power plan from +3VSUS to +3VA.

Project Name: G752VY			Rev: 2.0
Title: AUD EXT Jack			
Size: C	Dept.: ASUSTeK COMPUTER INC. (S	Engineer: Richard Liu	
Date: Tuesday, July 21, 2015		Sheet 38 of 102	



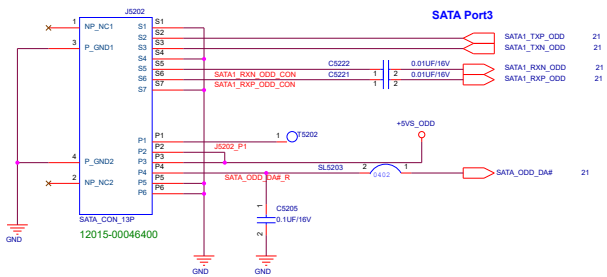


AMP

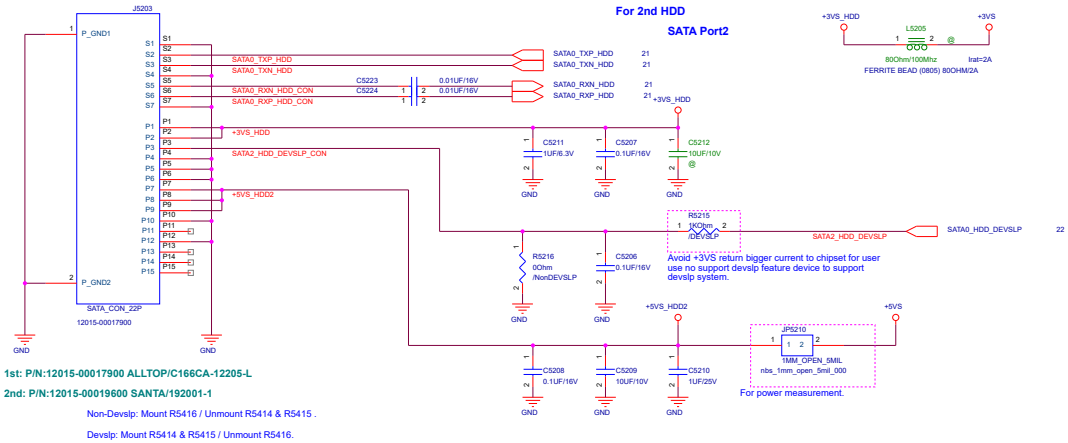
GAIN1	GAIN0	Av(inv)
0	0	20 dB
0	1	26 dB
1	0	32 dB
1	1	36 dB

ASUS	Project Name: G752VY	Rev: 2.0
Title : AUD INT WOOFER		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 39 of 102	

ODD



2nd HDD



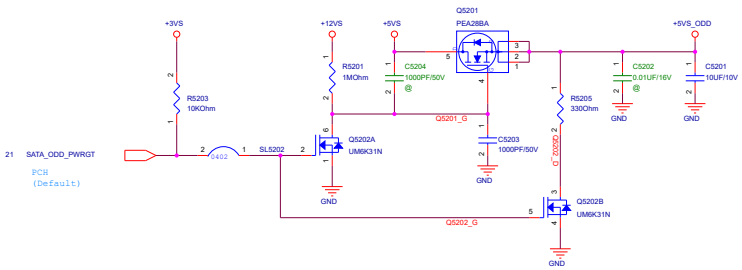
1st: P/N:12015-00017900 ALLTOP/C166CA-12205-L

2nd: P/N:12015-00019600 SANTA/192001-1

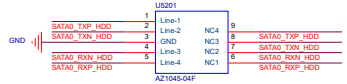
Non-Devslp: Mount R5416 / Unmount R5414 & R5415 .

Devslp: Mount R5414 & R5415 / Unmount R5416.

ODD Power



EMI Request

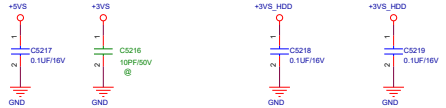


1st Source: P/N:07G028076030 ESD PROTECTION AZ1045-04F

2nd Source: P/N:07G028153010 ESD PROTECTION IP4284CZ10-TB

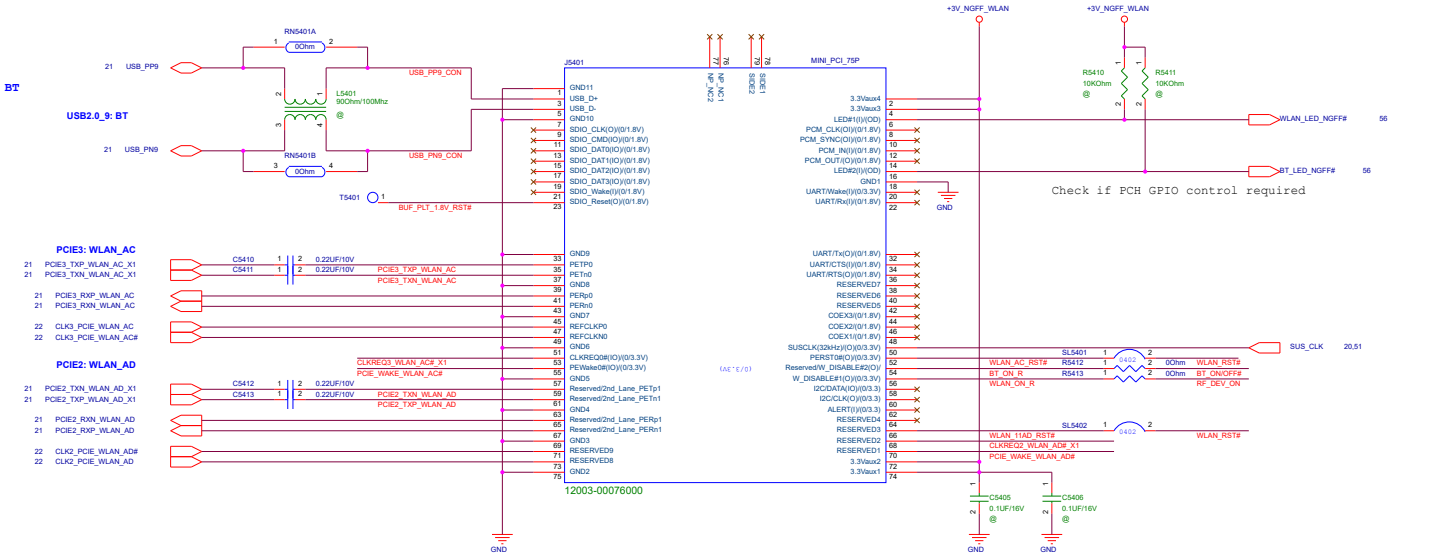
For RF requirement

EMI Request0820



ASUS	Project Name: G752VY		Rev: 2.0
Title : NGFF SDD/HDD/ODD Conn.			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Tuesday, July 21, 2015	Sheet 52 of 102		

NGFF M.2 TYPE_E-KEY WIFI



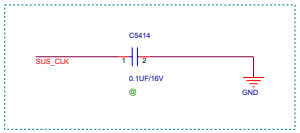
J5401_NGFF E-KEY WLAN Connector H=2.0mm

1st Source: P/N:12003-00071300 KYOCERA/206411067101894E

2nd Source: P/N:12003-00074900 ACES/51746-0670P-005

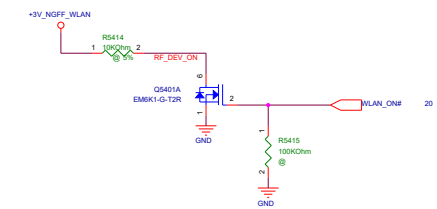
3rd Source: P/N:12003-00076000 ARGOSY/NASE0-S6701-TP20

4th Source: P/N:12003-00072100 JAE/SM3ZS067U215AE

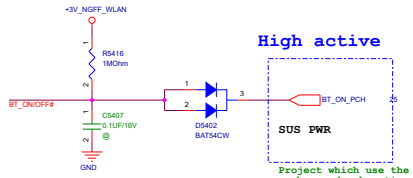


74	3.3Vaux	GND	75
72	3.3Vaux	RESERVED	73
70	RESERVED	RESERVED	71
68	RESERVED	GND	69
66	RESERVED	Reserved/2nd Lane PERn1	67
64	GPIO0 NFC Reset# (MGPIO7)(O)(0/3.3V)	Reserved/2nd Lane PERp1	65
62	NFC I2C IRQ (MGPIO5)(I)(0/3.3)	GND	63
60	NFC I2C SM CLK (O)(0/3.3)	Reserved/2nd Lane PETn1	61
58	NFC I2C SM DATA (IO)(0/3.3)	Reserved/2nd Lane PETp1	59
56	W_DISABLE#1 (O)(0/3.3V)	GND	57
54	Reserved/W_DISABLE#2 (O)(0/3.3V)	PEWake0# (IO)(0/3.3V)	55
52	PERST0# (O)(0/3.3V)	CLKREQ0# (IO)(0/3.3V)	53
50	SUSCLK(32kHz) (O)(0/3.3V)	GND	51
48	COEX1 (?)(0/1.8V)	REFCLKN0	49
46	COEX2(?)(0/1.8V)	REFCLKP0	47
44	COEX3(?)(0/1.8V)	GND	45
42	CLink CLK	PERn0	43
40	CLink DATA	PERp0	41
38	CLink RESET (O)(0/3.3V)	GND	39
36	UART CTS (O)(0/1.8V)	PETn0	37
34	UART RTS (I)(0/1.8V)	PETp0	35
32	UART Tx (O)(0/1.8V)	GND	33
	Key	Key	
	Key	Key	
	Key	Key	
	Key	Key	
22	UART Rx (I)(0/1.8V)	SDIO Reset(O)(0/1.8V)	23
20	UART Wake (I)(0/3.3V)	SDIO Wake(I)(0/1.8V)	21
18	GND	SDIO DAT3(IO)(0/1.8V)	19
16	LED#2 (I)(OD)	SDIO DAT2(IO)(0/1.8V)	17
14	PCM_OUT (I)(0/1.8V)	SDIO DAT1(IO)(0/1.8V)	15
12	PCM_IN (O)(0/1.8V)	SDIO DAT0(IO)(0/1.8V)	13
10	PCM_SYNC (O)(0/1.8V)	SDIO CMD(IO)(0/1.8V)	11
8	PCM_CLK (O)(0/1.8V)	SDIO CLK(O)(0/1.8V)	9
6	LED#1 (I)(OD)	GND	7
4	3.3Vaux	USB_D-	5
2	3.3Vaux	USB_D+	3
		GND	1

WLAN & BT ON



To match WHQL test.Due to BT wake up to spend much time if use +3VS.So,change to +3V,let BT can work quickly when S3 wake up.

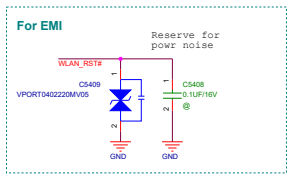


High active

Project which use the combo card schematic should make sure that BT_ON signal can't be High at S3/S4/S5 state to prevent leakage

WLAN NUT

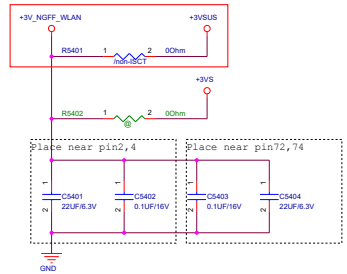
For EMI



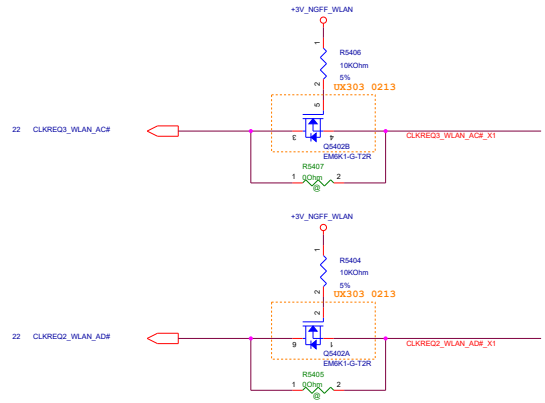
WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)

Support ASUS Open Cloud Computing (AOConnect)

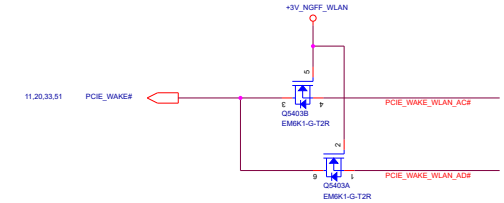
WLAN PWR to +3VSUS



WLAN CLKREQ#

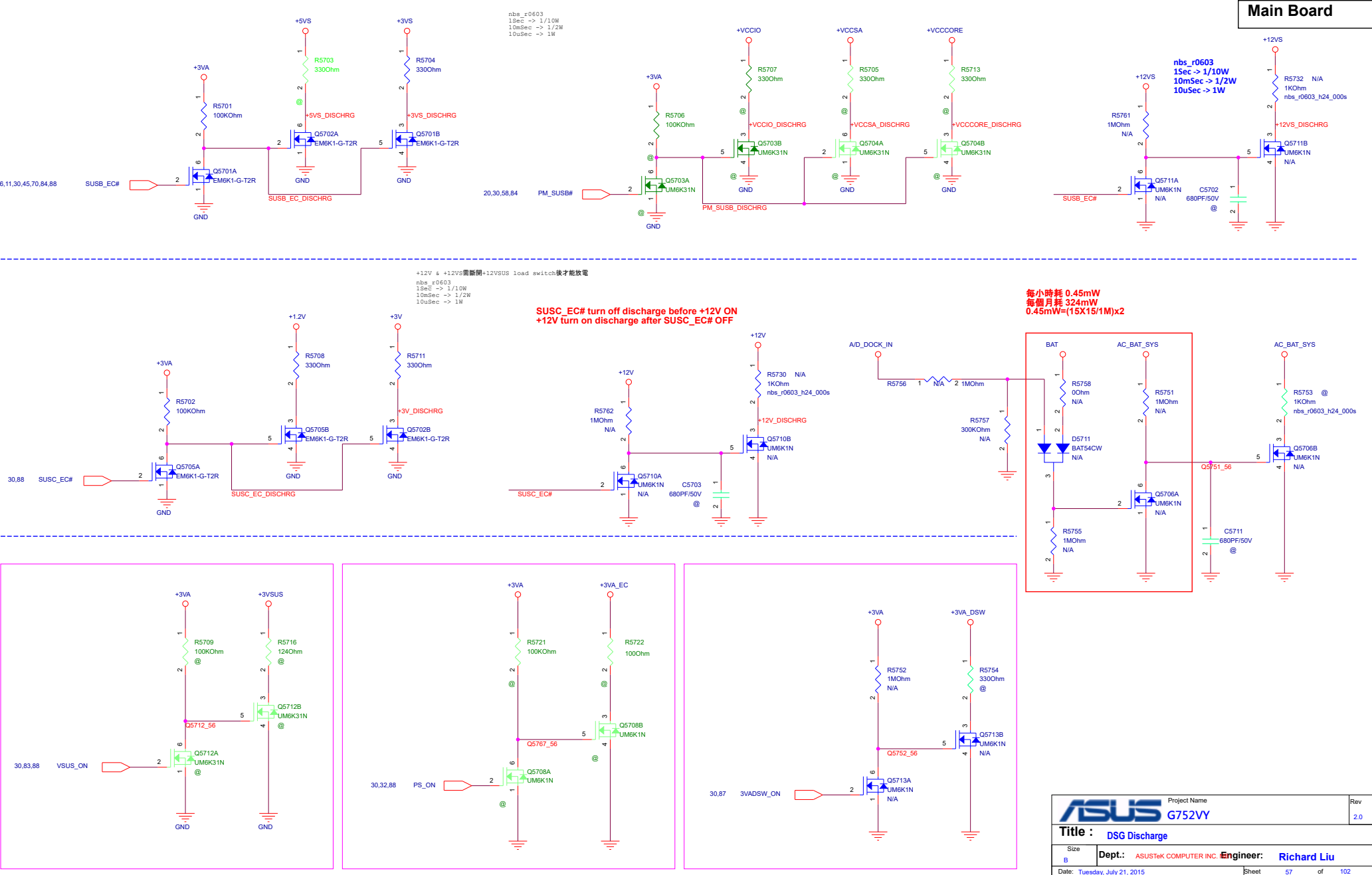


WLAN_Wake# Control



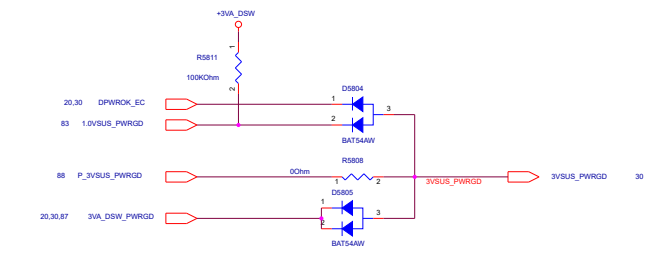
Project Name	G752VY	Rev 2.0
Title :	NGFF M.2 WLAN & BT	
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 54 of 102	

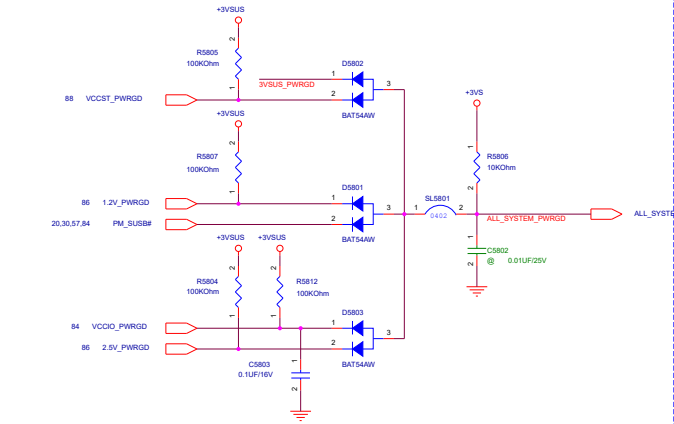
Main Board

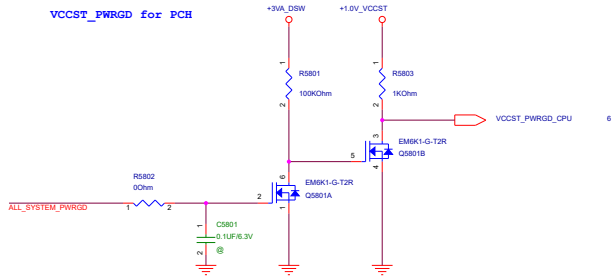


ASUS	Project Name: G752VY	Rev: 2.0
Title : DSG Discharge		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 57 of 102	

Main Board

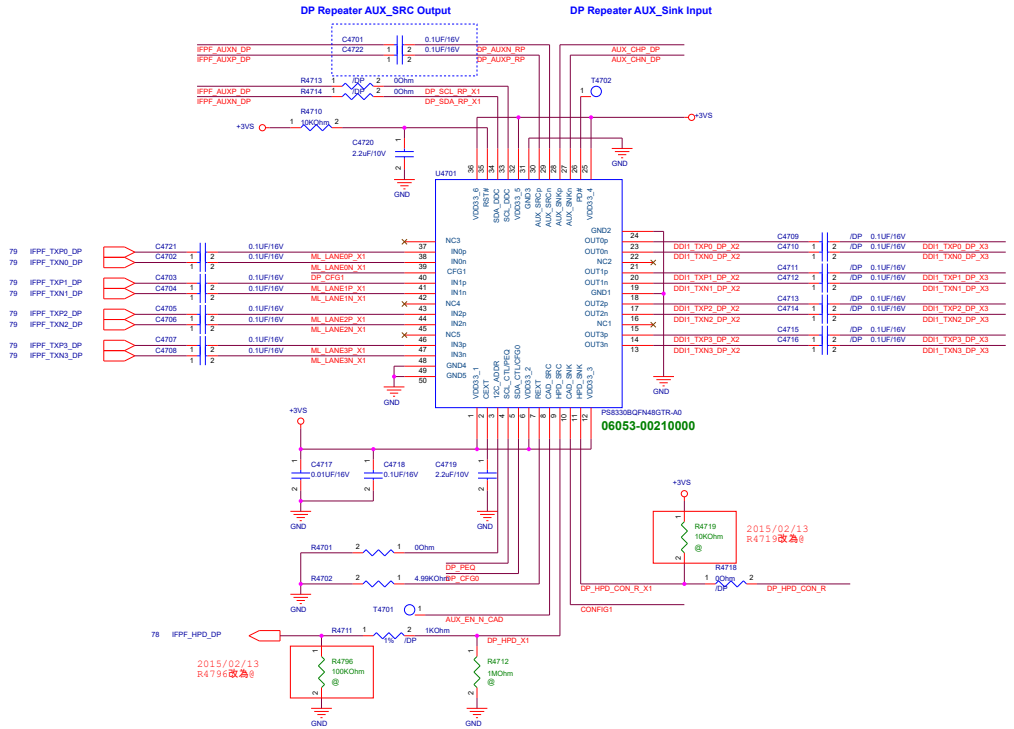


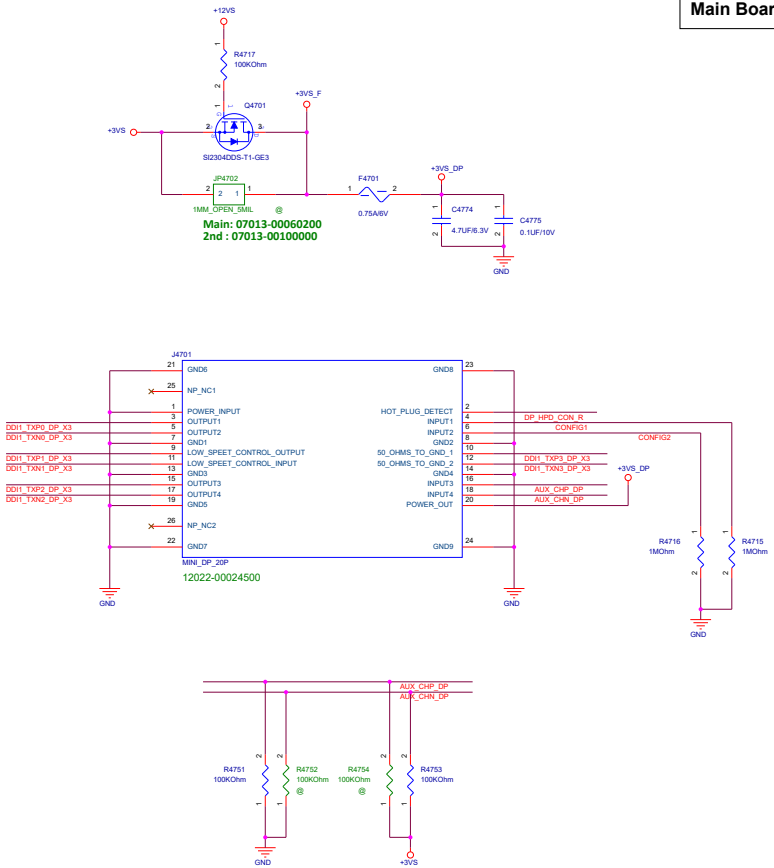


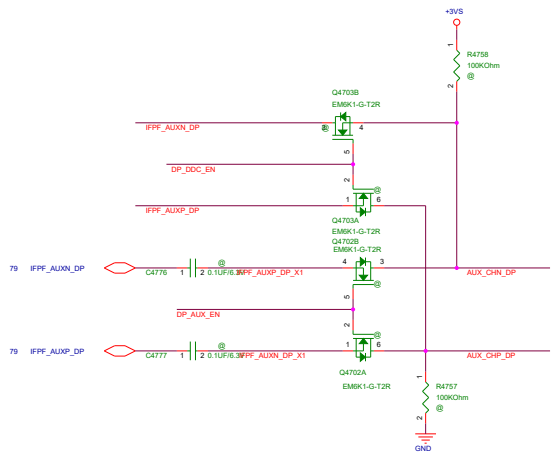


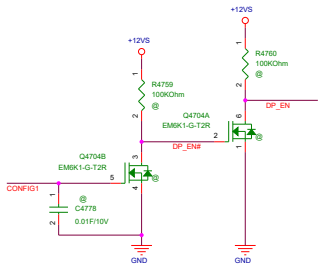
ASUS	Project Name: G752VY		Rev: 2.0
Title : PRO Protect			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Tuesday, July 21, 2015		Sheet 58 of 102	

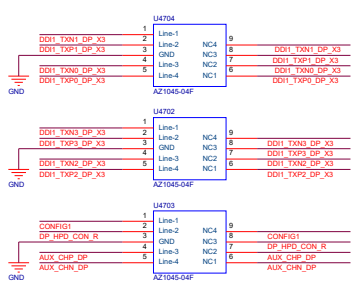
DP Repeater_PS8330B

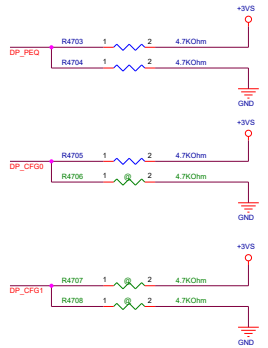






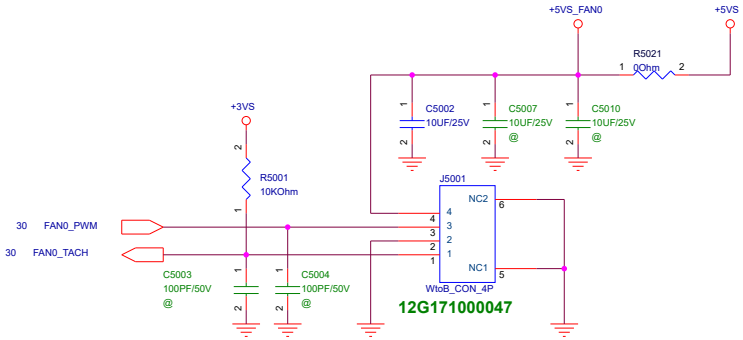




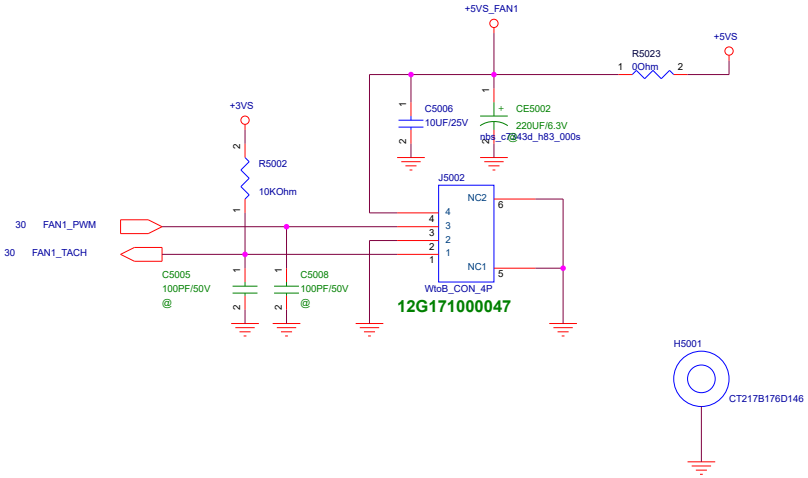


Project Name	G752VY
Rev	2.0
Title :	Display Port Conn.
Size	C
Dept.:	ASUSTeK COMPUTER INC.
Engineer:	Richard Liu
Date:	Tuesday, July 21, 2015
Sheet	47 of 102

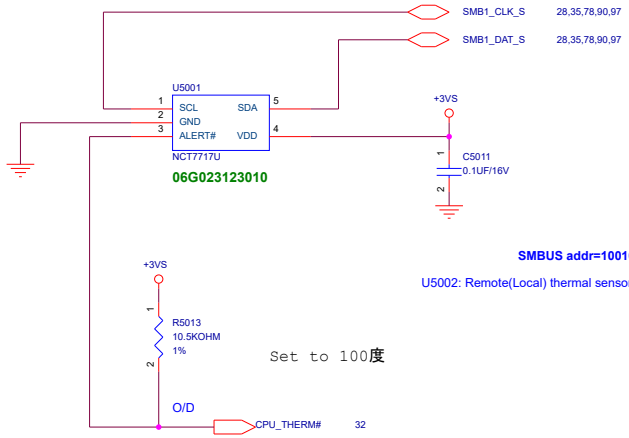
PWM CPU Fan



PWM VGA Fan



CPU Thermal Sensor



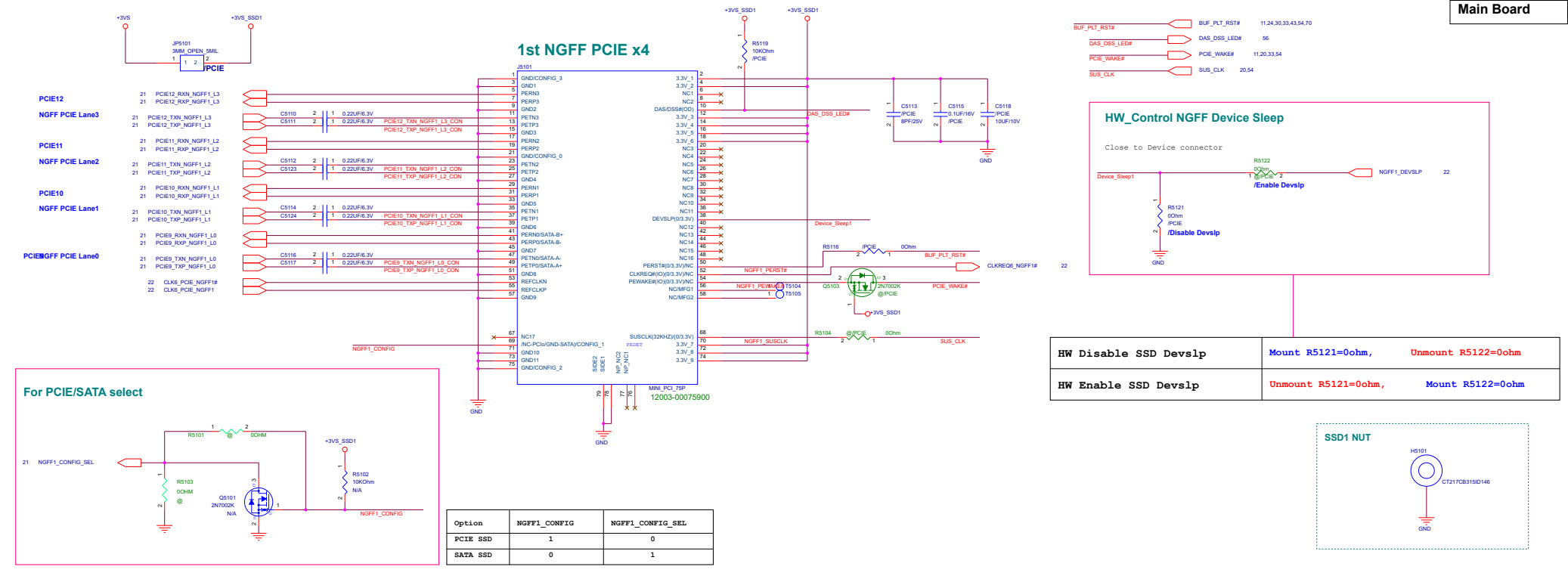
SMBUS addr=10010000 (90)

U5002: Remote(Local) thermal sensor,use remote mode.

ASUS	Project Name: G752VY		Rev: 2.0
Title : FAN_Fan & Sensor			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Tuesday, July 21, 2015		Sheet 50 of 102	

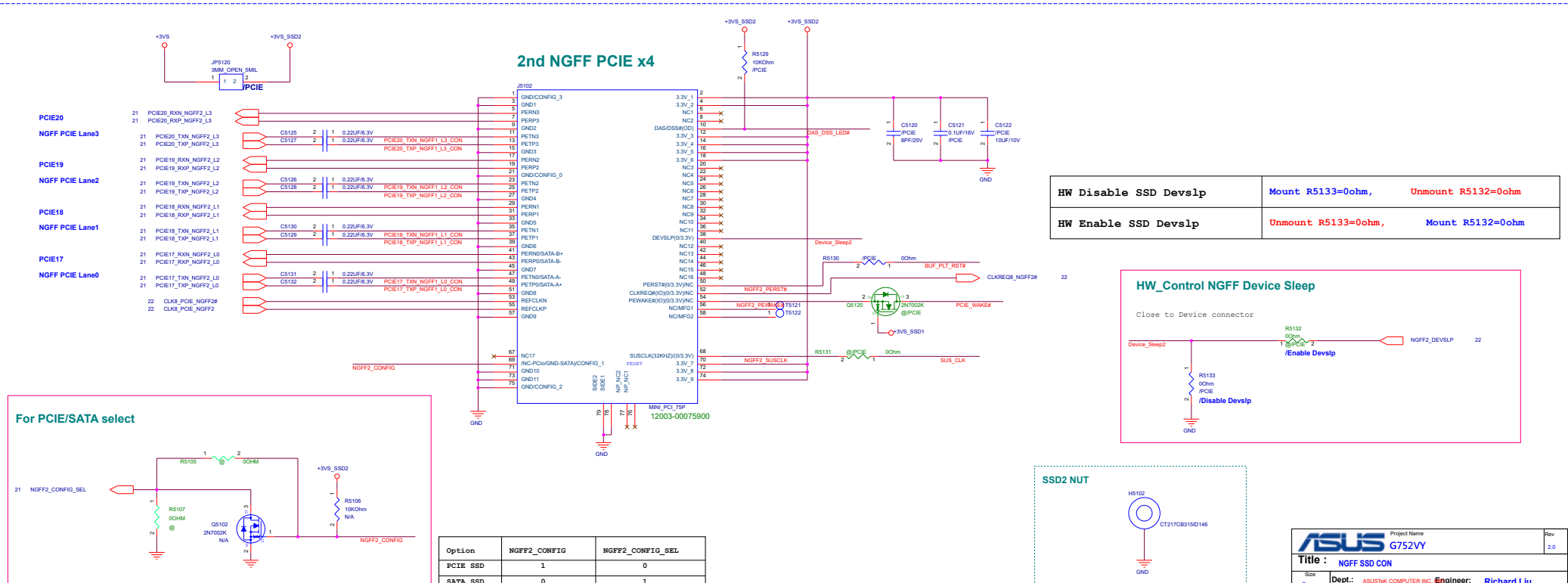
Main Board

Project Name: G752VY		Rev: 2.0
Title : NB*		
Size: A	Dept.: ASUSTeK COMPUTER INC. (NB)	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 64 of 102	



Option	NGFF1_CONFIG	NGFF1_CONFIG_SEL
PCIE SSD	1	0
SATA SSD	0	1

HW Disable SSD Devslp	Mount R5121=0ohm,	Unmount R5122=0ohm
HW Enable SSD Devslp	Unmount R5121=0ohm,	Mount R5122=0ohm

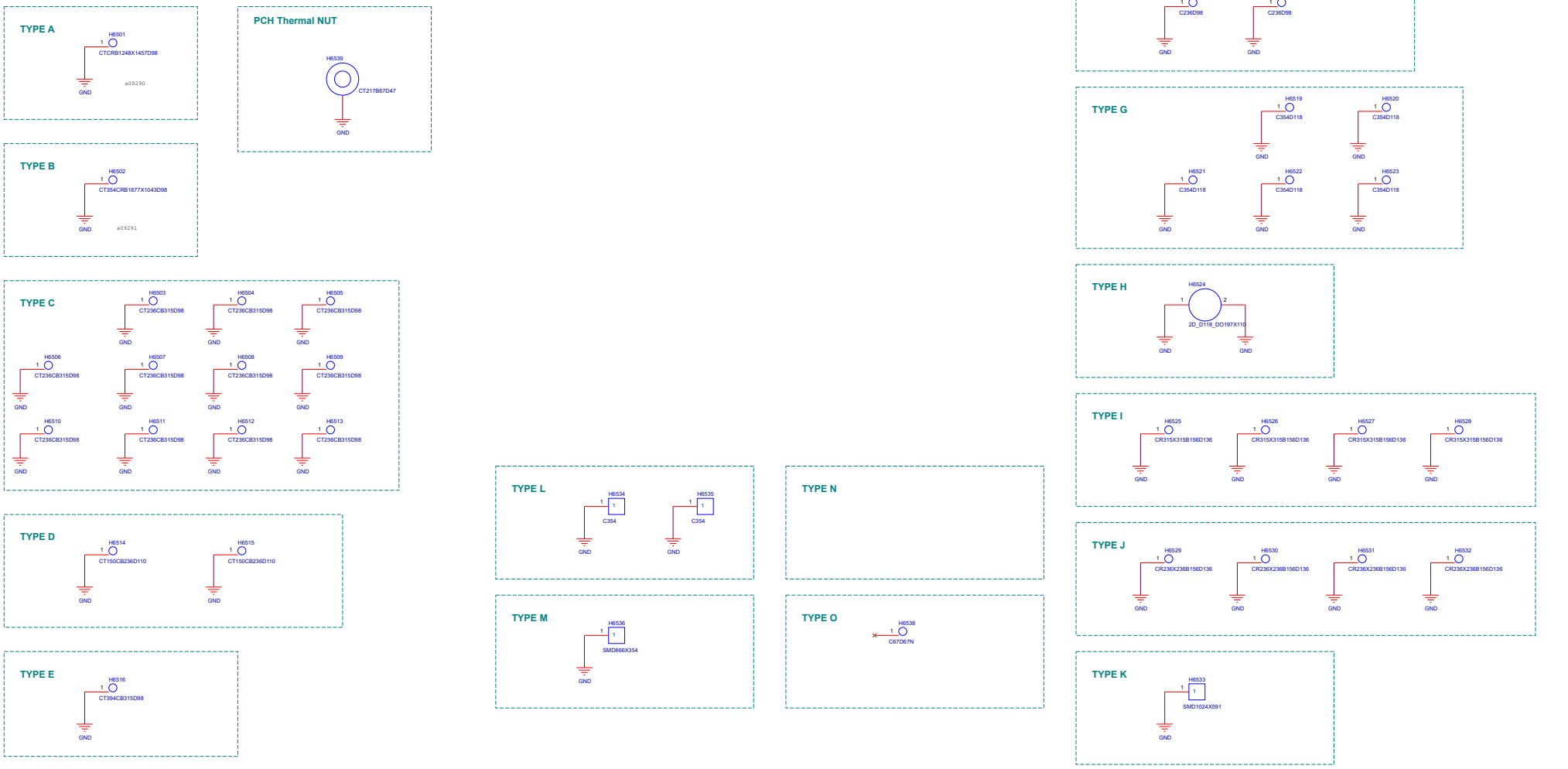


Option	NGFF2_CONFIG	NGFF2_CONFIG_SEL
PCIE SSD	1	0
SATA SSD	0	1

HW Disable SSD Devslp	Mount R5133=0ohm,	Unmount R5132=0ohm
HW Enable SSD Devslp	Unmount R5133=0ohm,	Mount R5132=0ohm

Project Name	G752VY	Rev 2.0
Title :	NGFF SSD CON	
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 51 of 102	

TOP Component



BOT Component

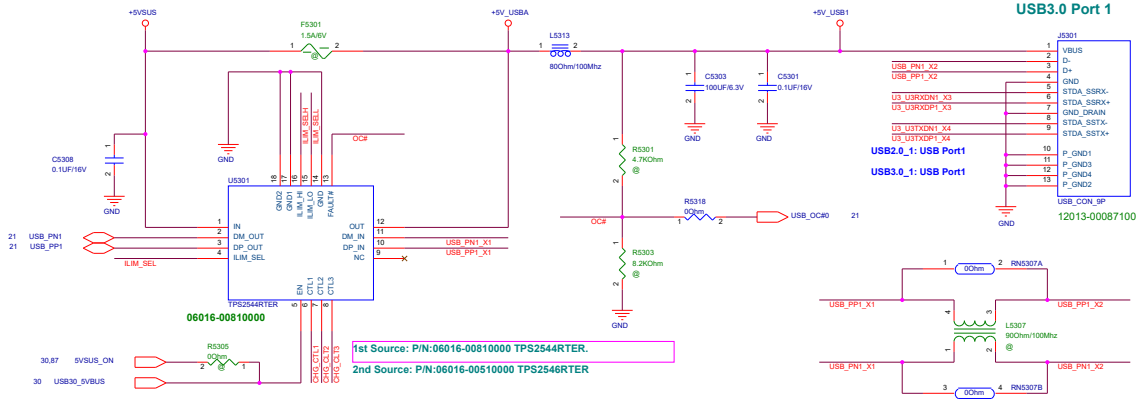
ASUS	Project Name: G752VY	Rev: 2.0
Title :	ME W2B Conn. & NUT	
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 65 of 102	

USB3.0_PORT1 (Support USB Charge Circuit)

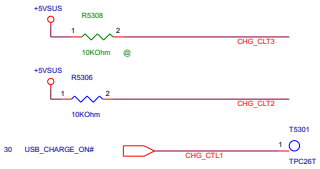
J5201 USB3.0 Connector

1st Source: P/N:12013-00018300 FOXCONN/UEA1111-N40AM2-7H

2nd Source: P/N:12013-00080400 SINGATRON/2UB4006-310101F



USB Charge Circuit (For PORT 1)

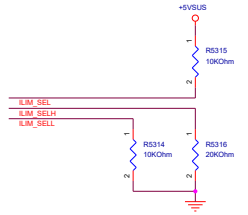


Cheif River Platform : Mount R5208

HSW, BDW Platform : Unmount R5208

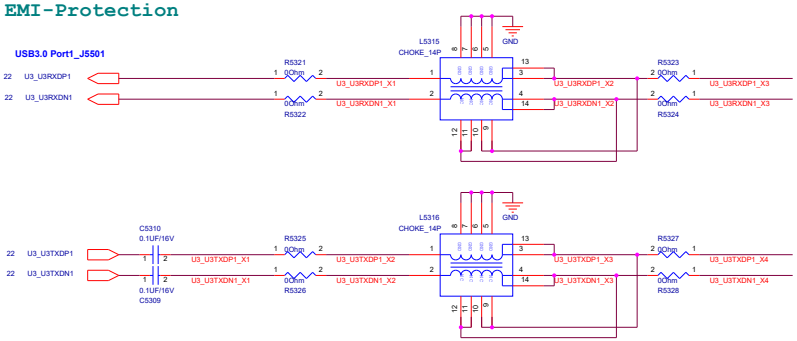
		TI 2544 / TI2546			
CHG_CTL		[1]	[2]	[3]	
USB_CHARGER_ON#	0	0	1	1	AUTO
	1	1	1	1	CDP
USB_CHARGE_DISABLE	0	1	1	0	SDP

Current Limit

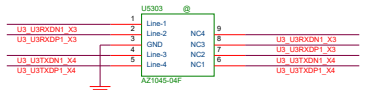


TI2544 / TI2546 Mount R5314(10kohm), R5316(20kohm), R5315(10kohm)

USB3.0 EMI-Protection



USB3.0 ESD-Protection

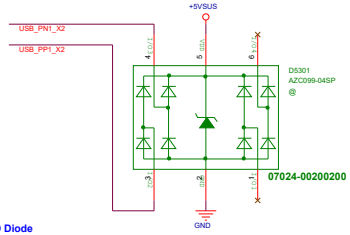


1st : 07G028076030
ESD PROTECTION AZ1045-04F

2nd : 07G028153010
ESD PROTECTION IP4284CZ10-TB

BC1.2 Charger Disable

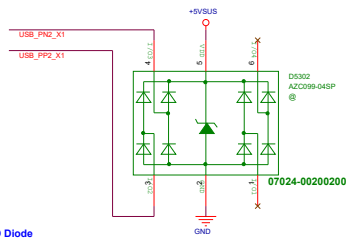
USB2.0 ESD-Protection



D5301 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

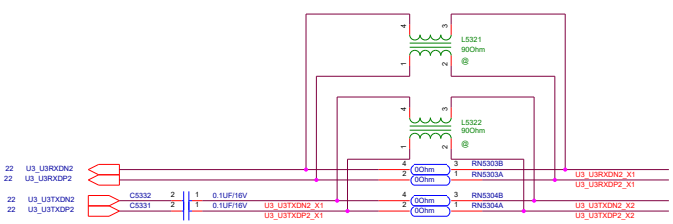


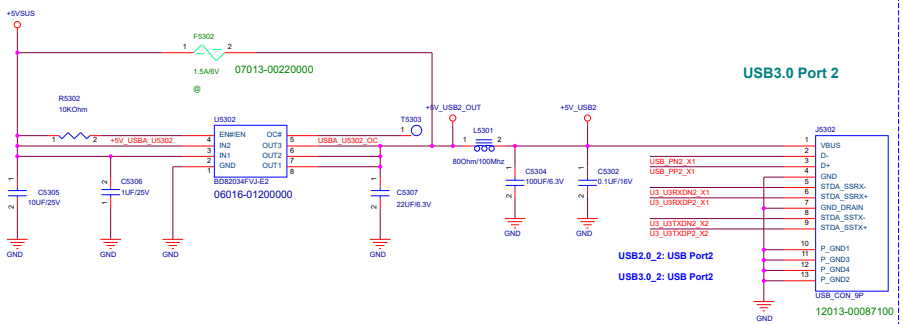
D5301 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

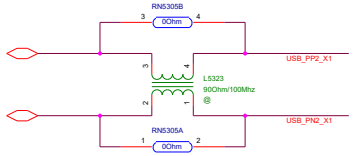
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

USB3.0_PORT2

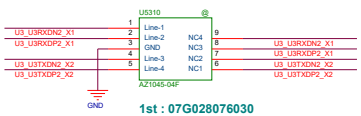




USB3.0 Port 2



USB3.0 ESD-Protection



1st : 07G028076030
ESD PROTECTION AZ1045-04F

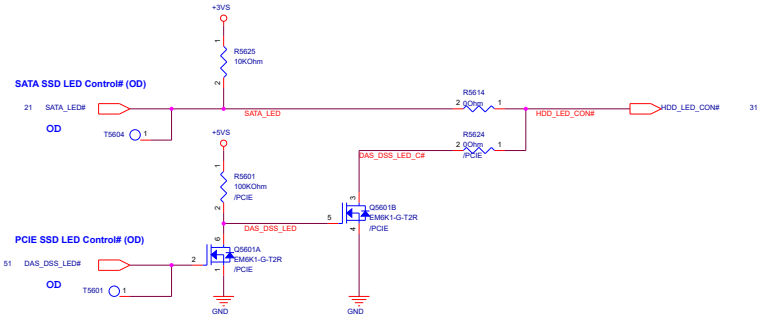
2nd : 07G028153010
ESD PROTECTION IP4284CZ10-TB

ASUS	Project Name: G752VY		Rev: 2.0
Title : USB 3.0 2 Ports			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Tuesday, July 21, 2015	Sheet: 53	of: 102	

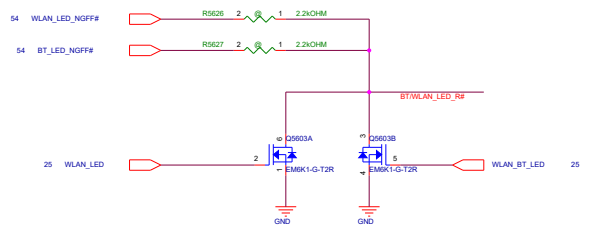
Main Board

ASUS	Project Name: G752VY	Rev: 2.0
Title : NB*		
Size: B	Dept.: ASUSTeK COMPUTER INC. (I	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 67 of 102	

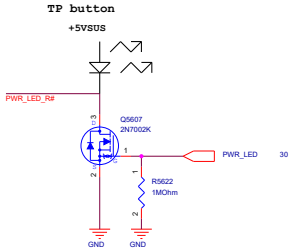
HDD LED & PCIE SSD LED



BT/WLAN LED Control



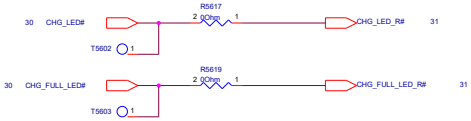
PWR LED Control



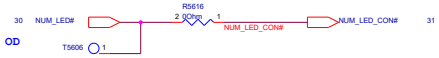
To TP Button CONN

PWR LED

Charger LED

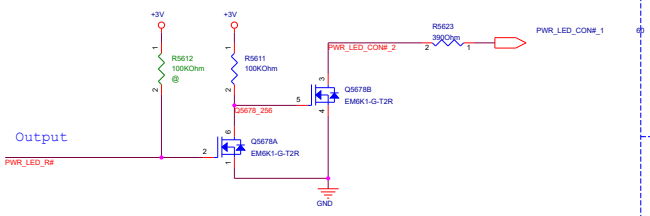


NumLock LED



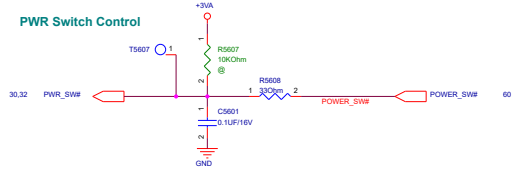
BT/WLAN LED

OS LED Control



To Power Button IO BD

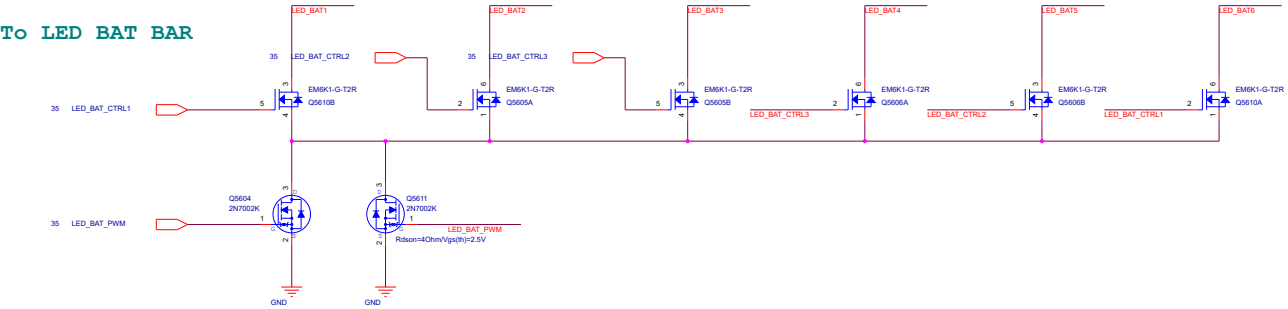
PWR Switch Control

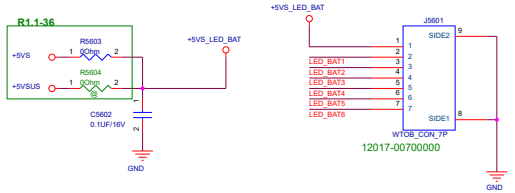


To KeyBoard CONN

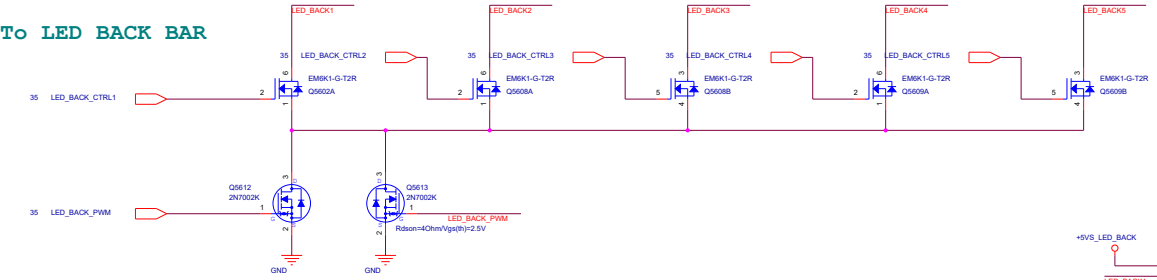
CapsLock LED

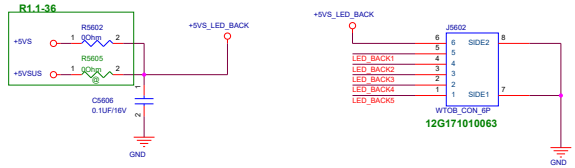
To LED BAT BAR

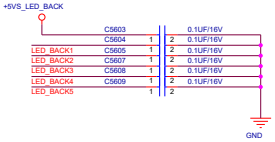




To LED BACK BAR







ASUS	Project Name: G752VY		Rev: 2.0
Title : LED Indicator			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Tuesday, July 21, 2015	Sheet 56 of 102		

PCI EXPRESS_Graphics

REVERSED Type PCIE X16

Reverse PCIEG x 16

PCIENB_RXN0	0.22UF/10V	2	1	CX7027		
PCIENB_RXP0	0.22UF/10V	2	1	CX7008	PCIEG_TXN15	PCIEG_TXP15
PCIENB_RXN1	0.22UF/10V	2	1	CX7004		
PCIENB_RXP1	0.22UF/10V	2	1	CX7013	PCIEG_TXN14	PCIEG_TXP14
PCIENB_RXN2	0.22UF/10V	2	1	CX7009		
PCIENB_RXP2	0.22UF/10V	2	1	CX7011	PCIEG_TXN13	PCIEG_TXP13
PCIENB_RXN3	0.22UF/10V	2	1	CX7010		
PCIENB_RXP3	0.22UF/10V	2	1	CX7016	PCIEG_TXN12	PCIEG_TXP12
PCIENB_RXN4	0.22UF/10V	2	1	CX7006		
PCIENB_RXP4	0.22UF/10V	2	1	CX7022	PCIEG_TXN11	PCIEG_TXP11
PCIENB_RXN5	0.22UF/10V	2	1	CX7030		
PCIENB_RXP5	0.22UF/10V	2	1	CX7024	PCIEG_TXN10	PCIEG_TXP10
PCIENB_RXN6	0.22UF/10V	2	1	CX7025		
PCIENB_RXP6	0.22UF/10V	2	1	CX7032	PCIEG_TXN9	PCIEG_TXP9
PCIENB_RXN7	0.22UF/10V	2	1	CX7021		
PCIENB_RXP7	0.22UF/10V	2	1	CX7015	PCIEG_TXN8	PCIEG_TXP8
PCIENB_RXN8	0.22UF/10V	2	1	CX7026		
PCIENB_RXP8	0.22UF/10V	2	1	CX7001	PCIEG_TXN7	PCIEG_TXP7
PCIENB_RXN9	0.22UF/10V	2	1	CX7029		
PCIENB_RXP9	0.22UF/10V	2	1	CX7002	PCIEG_TXN6	PCIEG_TXP6
PCIENB_RXN10	0.22UF/10V	2	1	CX7014		
PCIENB_RXP10	0.22UF/10V	2	1	CX7007	PCIEG_TXN5	PCIEG_TXP5
PCIENB_RXN11	0.22UF/10V	2	1	CX7020		
PCIENB_RXP11	0.22UF/10V	2	1	CX7023	PCIEG_TXN4	PCIEG_TXP4
PCIENB_RXN12	0.22UF/10V	2	1	CX7031		
PCIENB_RXP12	0.22UF/10V	2	1	CX7017	PCIEG_TXN3	PCIEG_TXP3
PCIENB_RXN13	0.22UF/10V	2	1	CX7003		
PCIENB_RXP13	0.22UF/10V	2	1	CX7019	PCIEG_TXN2	PCIEG_TXP2
PCIENB_RXN14	0.22UF/10V	2	1	CX7018		
PCIENB_RXP14	0.22UF/10V	2	1	CX7012	PCIEG_TXN1	PCIEG_TXP1
PCIENB_RXN15	0.22UF/10V	2	1	CX7005		
PCIENB_RXP15	0.22UF/10V	2	1	CX7028	PCIEG_TXN0	PCIEG_TXP0

Control Signal from PCH

PCH_GPIO17

22,25 DGPU_PWROK

+3V3_AON

R7004 10KOhm

D7002 BAT54AW

D7001 1N4148WS

R7007 10KOhm

C7026 0.022UF/16V

GND

71,91 PS_PGOOD_NV_FB

R7013 0Ohm

93 +FBVDDQ_PWRGD

R7010 0Ohm

92 +PEXVDD_PWRGD

R7015 0Ohm

PCH_GPIO54

25 DGPU_PWR_EN#

+3VS

R7021 10KOhm

0Ohm

R7019

SUSB# PWR_R

GPU_PWRON

U7005 74LVC1G08GW

+3VSUS

GPU_PWR_EN

GPU_PWR_EN 71

Q7001 2N7002K Rdson=4Ohm/Vgs(th)=2.5V

R7022 1KOhm

R7023 100KOhm

5,11,30,45,57,84,88 SUSB_EC#

R7016 0Ohm

11,24,30,33,43,51,54 BUF_PLT_RST#

2014/2/06 For EMI Request

C7029 100PF/50V

25 GPU_RST#

R7001 0Ohm

GPU_RST#_R

U7002 74LVC1G08GW

R7006 0Ohm /GC6 20

SYS_PEX_RST_MON#

SYS_PEX_RST_MON# 79

R7017 100KOhm

R1.4-04 R1.2-17

R1.4-02

PCH_GPIO50

R1.4-04 R1.4-02 R1.2-17

78 GPU_PEX_RST_HOLD#

U7003 74LVC1G08GW /GC6 20

DGPU_RST#

DGPU_RST# 78

R7008 10KOhm /GC6 20

+3V3_AON

R7014 100KOhm

R7005 0Ohm

DGPU_RST#

PEX_CLK_REQ0#_R

22 CLK_PEGA_REQ0#

22 CLK0_PCIE_PEG_VGA

22 CLK0_PCIE_PEG#_VGA

SL7002 SL7003 SL7001 SL7004 0402

PEX_RST#

PEX_CLK_REQ0#_C

PCIE_REFCLKP0_C

PCIE_REFCLKN0_C

3 PCIENB_RXN[15:0]

3 PCIENB_RXP[15:0]

3 PCIEG_RXN[15:0]

3 PCIEG_RXP[15:0]

EMI C7009 1UF/6.3V

U7001A 1/21 PCI_EXPRESS

PEX_WAKE_N

PEX_RST_N

PEX_CLKREQ_N

PEX_REFCLK

PEX_REFCLK_N

PEX_TX0 PEX_TX0_N

PEX_RX0 PEX_RX0_N

PEX_TX1 PEX_TX1_N

PEX_RX1 PEX_RX1_N

PEX_TX2 PEX_TX2_N

PEX_RX2 PEX_RX2_N

PEX_TX3 PEX_TX3_N

PEX_RX3 PEX_RX3_N

PEX_TX4 PEX_TX4_N

PEX_RX4 PEX_RX4_N

PEX_TX5 PEX_TX5_N

PEX_RX5 PEX_RX5_N

PEX_TX6 PEX_TX6_N

PEX_RX6 PEX_RX6_N

PEX_TX7 PEX_TX7_N

PEX_RX7 PEX_RX7_N

PEX_TX8 PEX_TX8_N

PEX_RX8 PEX_RX8_N

PEX_TX9 PEX_TX9_N

PEX_RX9 PEX_RX9_N

PEX_TX10 PEX_TX10_N

PEX_RX10 PEX_RX10_N

PEX_TX11 PEX_TX11_N

PEX_RX11 PEX_RX11_N

PEX_TX12 PEX_TX12_N

PEX_RX12 PEX_RX12_N

PEX_TX13 PEX_TX13_N

PEX_RX13 PEX_RX13_N

PEX_TX14 PEX_TX14_N

PEX_RX14 PEX_RX14_N

PEX_TX15 PEX_TX15_N

PEX_RX15 PEX_RX15_N

N16E-GS-KAB-A1

C7030 680PF/50V

DGPU_RST#

C7031 680PF/50V

GPU_RST#

+PEX_VDD

PLACE AT BALLS

PLACE OUTSIDE OF BGA

Max:2800mA

PEX_IOVDD1 PEX_IOVDD2 PEX_IOVDD3 PEX_IOVDD4 PEX_IOVDD5 PEX_IOVDD6 PEX_IOVDD7

AW33 AY32 AY33 AY35 BA33 BA35 BB33

C7023 1UF/6.3V C7014 1UF/6.3V

C7001 4.7UF/6.3V C7013 47UF/6.3V C7024 47UF/6.3V C7015 22UF/6.3V C7010 22UF/6.3V C7002 47UF/6.3V

PEX_IOVDDQ1 PEX_IOVDDQ2 PEX_IOVDDQ3 PEX_IOVDDQ4 PEX_IOVDDQ5 PEX_IOVDDQ6 PEX_IOVDDQ7 PEX_IOVDDQ8 PEX_IOVDDQ9 PEX_IOVDDQ10 PEX_IOVDDQ11 PEX_IOVDDQ12 PEX_IOVDDQ13 PEX_IOVDDQ14

AY24 AY26 AY27 AY29 AY30 BA24 BA26 BA27 BA29 BA30 BA32 BB24 BB27 BB30

C7019 1UF/6.3V C7020 1UF/6.3V

C7016 22UF/6.3V C7007 47UF/6.3V C7018 47UF/6.3V C7012 22UF/6.3V C7008 22UF/6.3V

PEX_PLL_HVDD

PEX_SVDD_3V3

Max:210mA

Max:210mA

AW30 AW32

C7011 0.1UF/10V C7006 0.1UF/10V

C7003 4.7UF/6.3V C7028 4.7UF/6.3V C7021 47UF/6.3V C7004 47UF/6.3V C7005 47UF/6.3V C7027 47UF/6.3V

+3V3_AON

VDD_SENSE AY23 NVDD_VCCSENSE 91

GND_SENSE AW23 NVDD_VSSSENSE 91

PLACE ON BOTTOM LAYER

PEX_TSTCLK_OUT PEX_TSTCLK_OUT_N

BH38 BG38

R7003 200Ohm

PEX_TSTCLK_OUT PEX_TSTCLK_OUTN

+PEX_PLLVDD +PEX_VDD

PEX_PLLVDD AW26

Max:150mA

R7009 0Ohm

C7025 0.1UF/10V C7022 1UF/6.3V C7017 4.7UF/6.3V

Under GPU PLACE OUTSIDE OF BGA

TESTMODE BA23

R7012 1% 10KOhm

GPU_TESTMODE

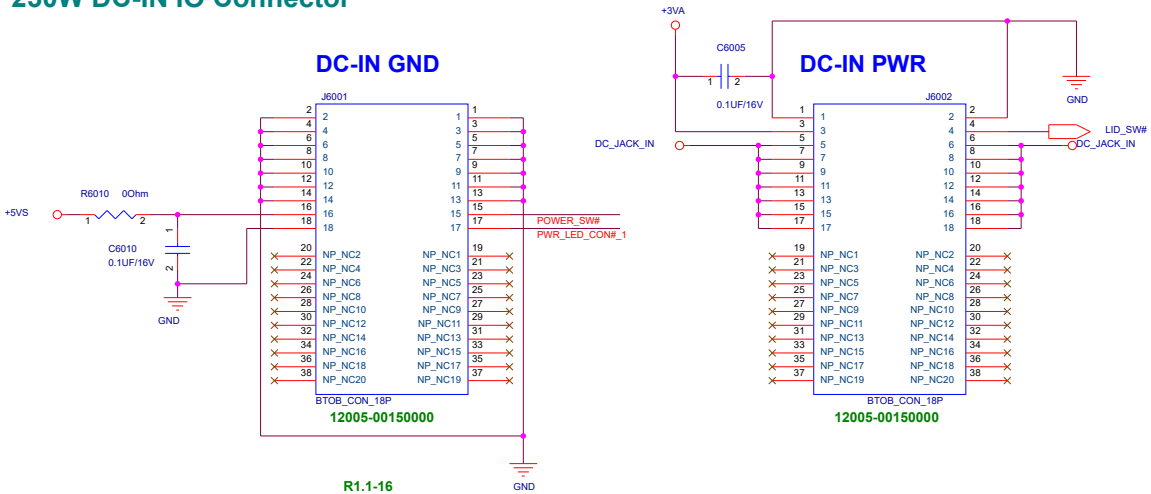
PEX_TERMP BJ38

R7002 1% 2.49KOhm

PEX_TERMP

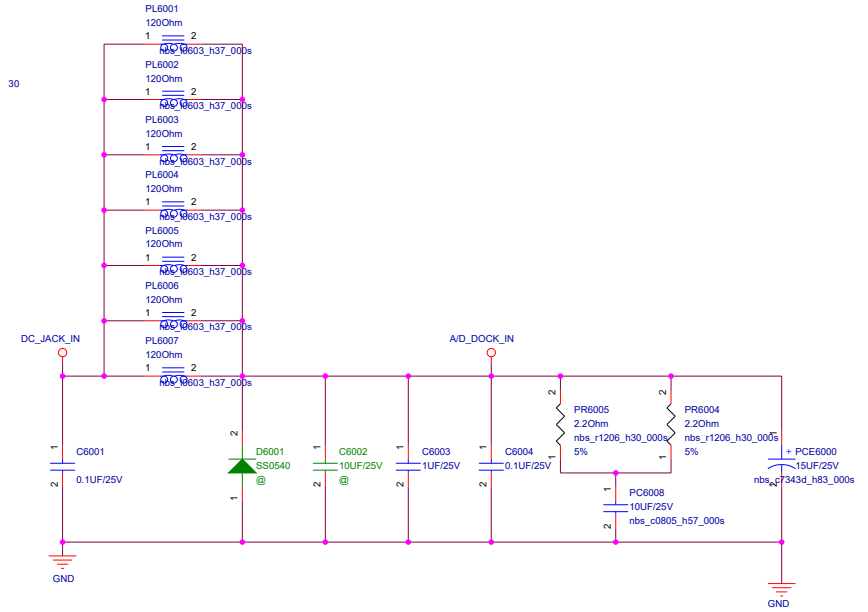
Project Name	G752VY
Rev	2.0
Title :	GPU_PCIE I/F
Size	C
Dept.:	ASUSTeK COMPUTER INC.
Engineer:	EE1_RD3
Date:	Tuesday, July 21, 2015
Sheet	70 of 102

230W DC-IN IO Connector

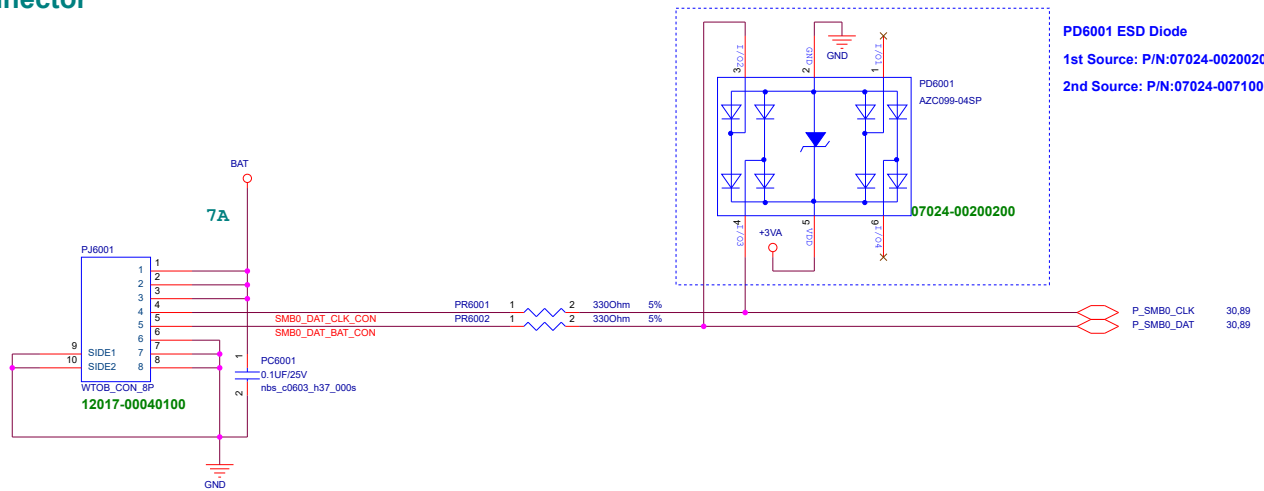


D6002 ESD Diode **1st Source: P/N:07G028162010 NXP SOT363**

2nd Source: P/N: 07G028127010 AMAZING SC70-6L



Battery Connector



PD6001 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

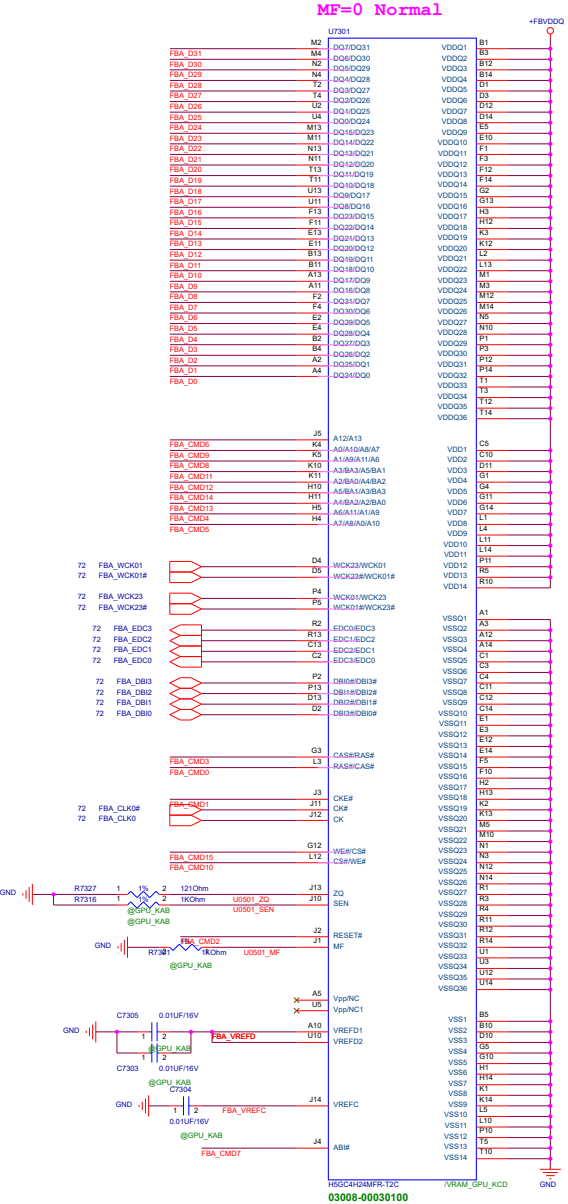
ASUS	Project Name: G752VY		Rev: 2.0
Title : DC & BAT IN			
Size: B	Dept.: NB Power team	Engineer: Benson Hsu	
Date: Tuesday, July 21, 2015		Sheet 60 of 102	

Main Board

Project Name: G752VY		Rev: 2.0
Title : NB*		
Size: A	Dept.: ASUSTeK COMPUTER INC. (RD)	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 62 of 102	

FBA Partition Memory (1 of 2)

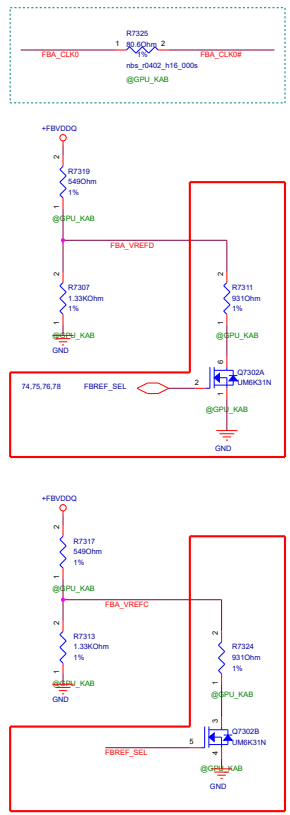
MF=0 Normal



GDD5 MODE SELECTION

MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

CK External Termination



R1.3-02 R1.2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)

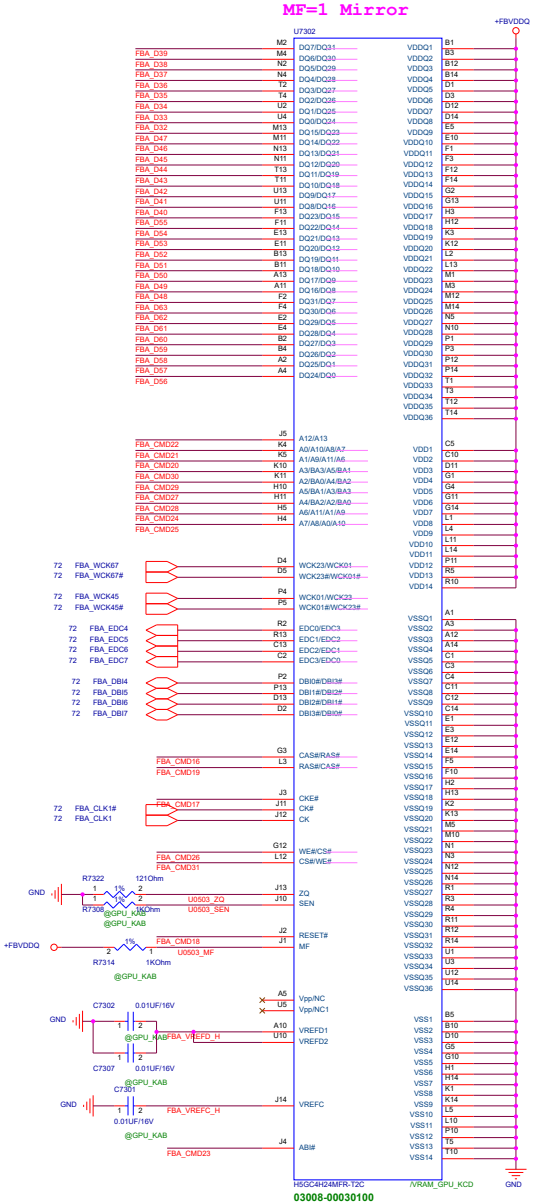
1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

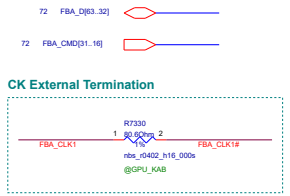
2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

3nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

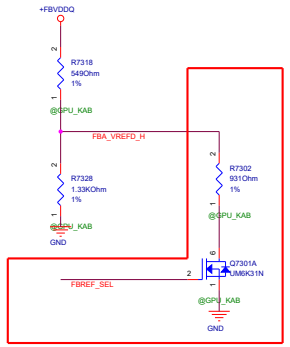
FBA Partition Memory (2 of 2)

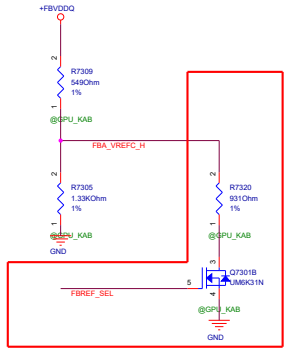
MF=1 Mirror





CK External Termination





R1.3-02 R1.2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)

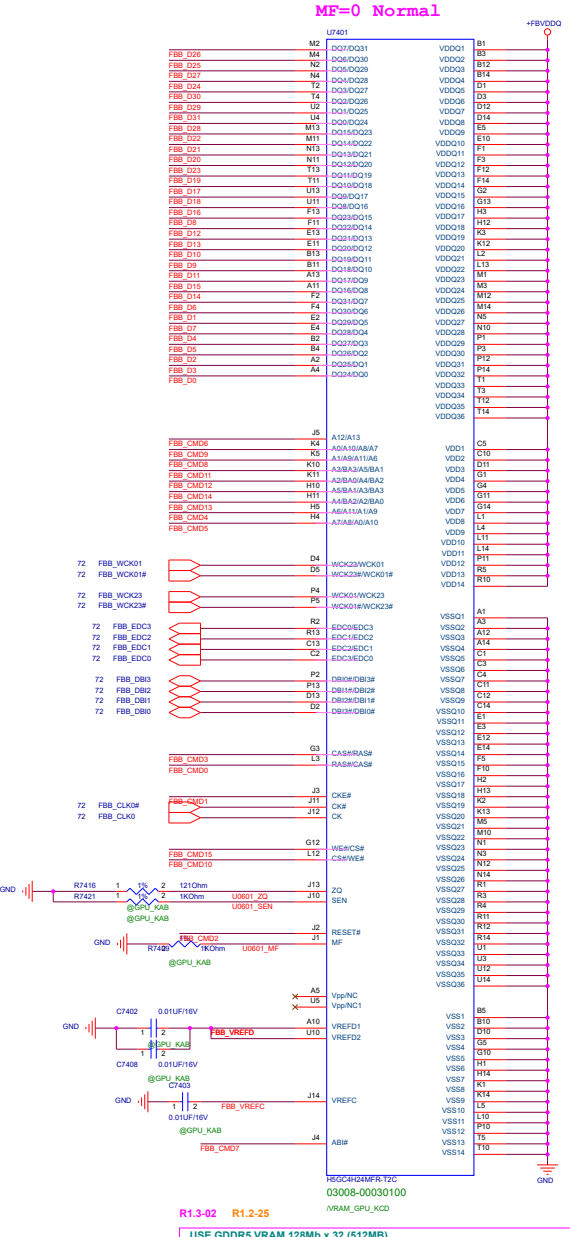
1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

3nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

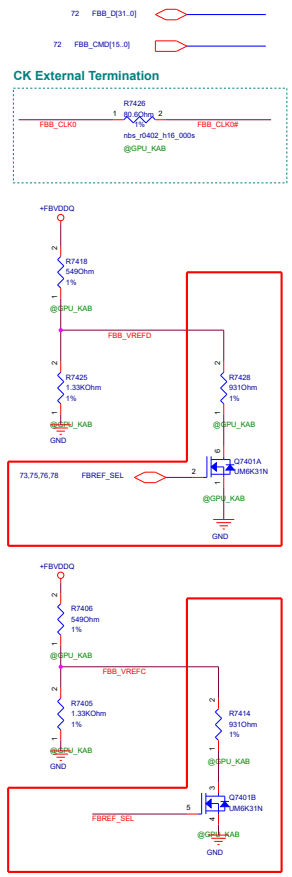
ASUSTeK COMPUTER INC. NB1	Title :	VRAM-CHANNEL A	
	Engineer:	Wenchi_Shen	
Size: C	Project Name: G752VY		Rev: 2.0
Date: Tuesday, July 21, 2015	Sheet 73 of 102		

FBB Partition Memory (1 of 2)



GDD5 MODE SELECTION

MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ



R1.3-02 R1.2-25

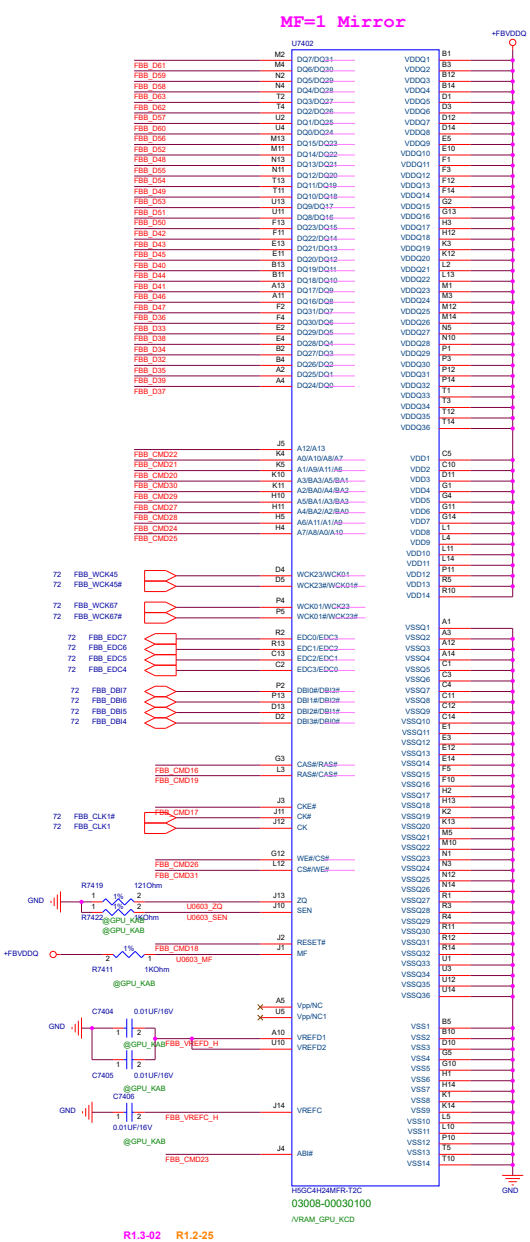
USE GDDR5 VRAM 128Mb x 32 (512MB)

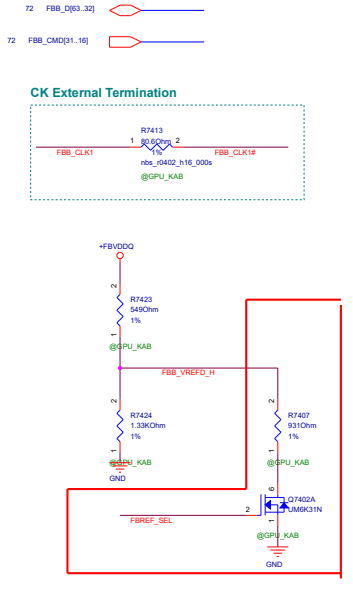
1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

3nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

FBB Partition Memory (2 of 2)





R1.3-02 R1.2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

3nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

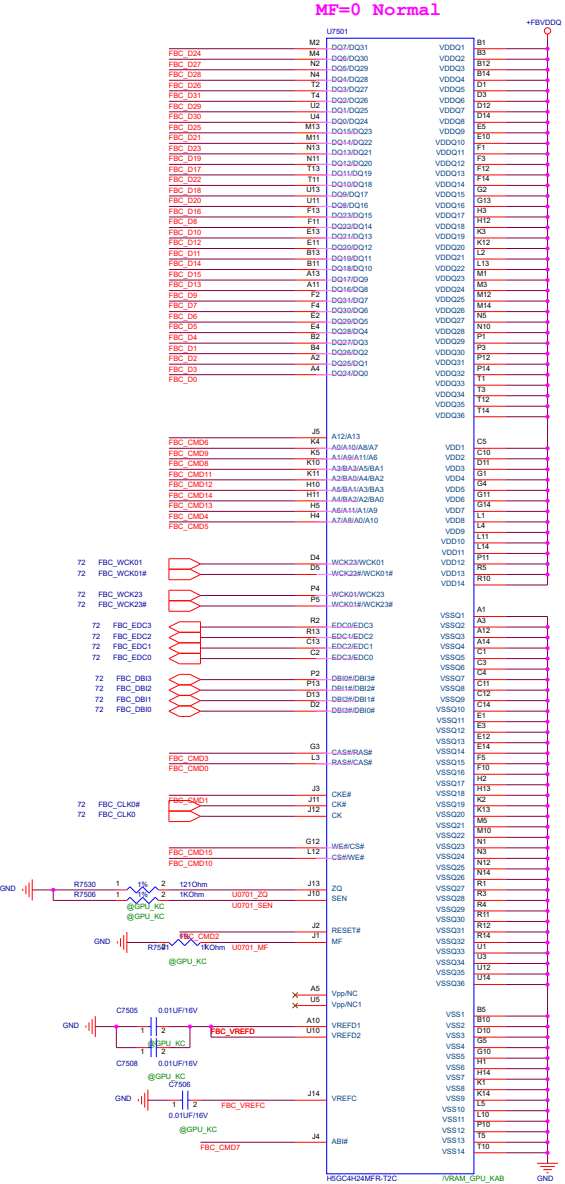
ASUSTeK COMPUTER INC. NB1	Title :	VRAM-CHANNEL B	
	Engineer:	Wenchi_Shen	
Size: C	Project Name: G752VY		Rev: 2.0
Date: Tuesday, July 21, 2015	Sheet 74 of 102		

Main Board

ASUS	Project Name: G752VY	Rev: 2.0
Title : NB*		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 66 of 102	

FBC Partition Memory (1 of 2)

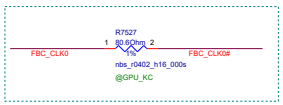
MF=0 Normal

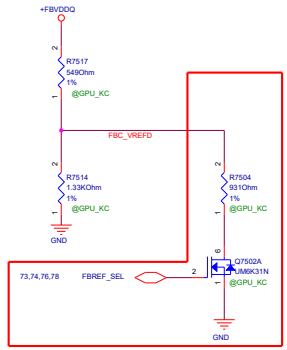


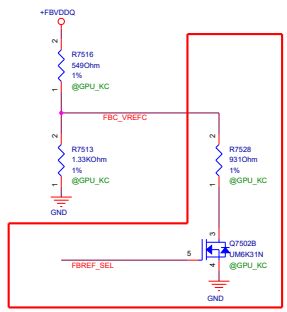
GDD5 MODE SELECTION

MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

CK External Termination







R1.3-02 R1.2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)

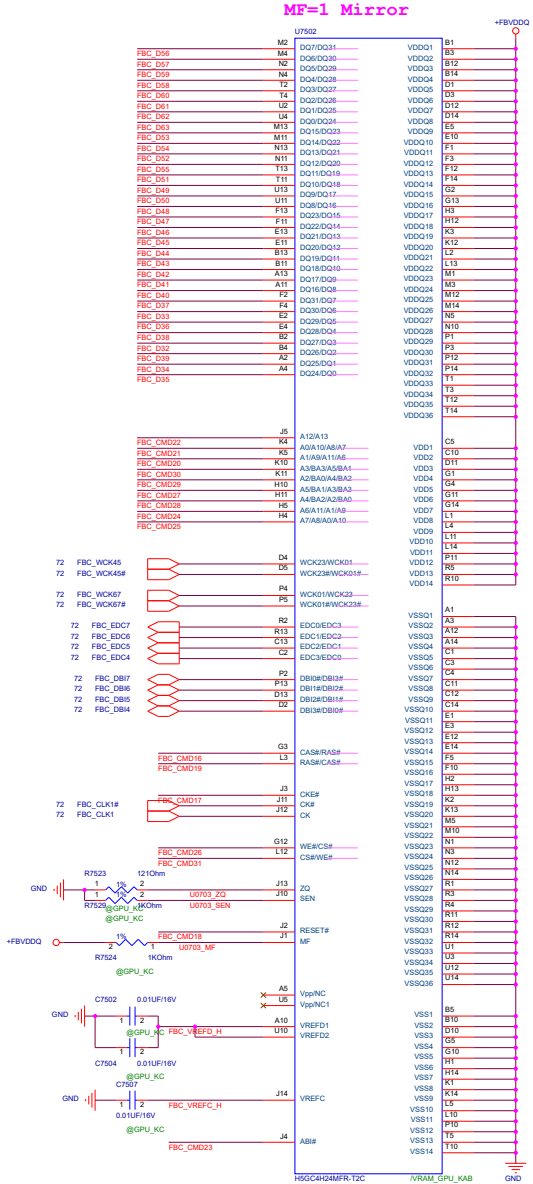
1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

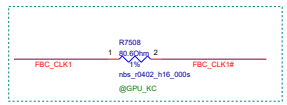
3nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

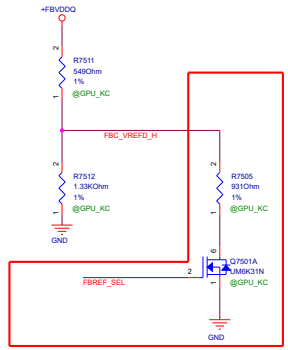
FBC Partition Memory (2 of 2)

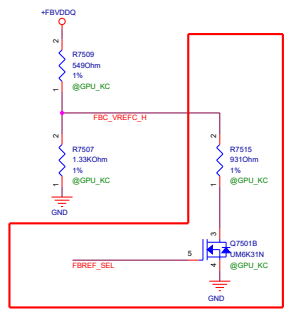
MF=1 Mirror



CK External Termination







R1.3-02 R1.2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

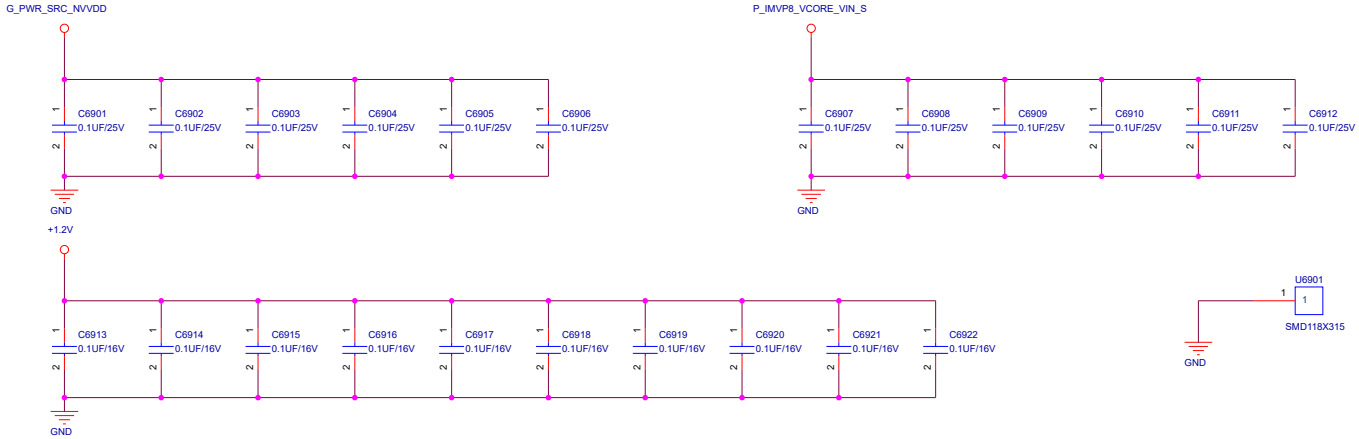
3nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

ASUS	Project Name: G752VY	Rev: 2.0
Title : VRAM-CHANNEL C		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE1_RD3
Date: Tuesday, July 21, 2015	Sheet 75 of 102	

Main Board

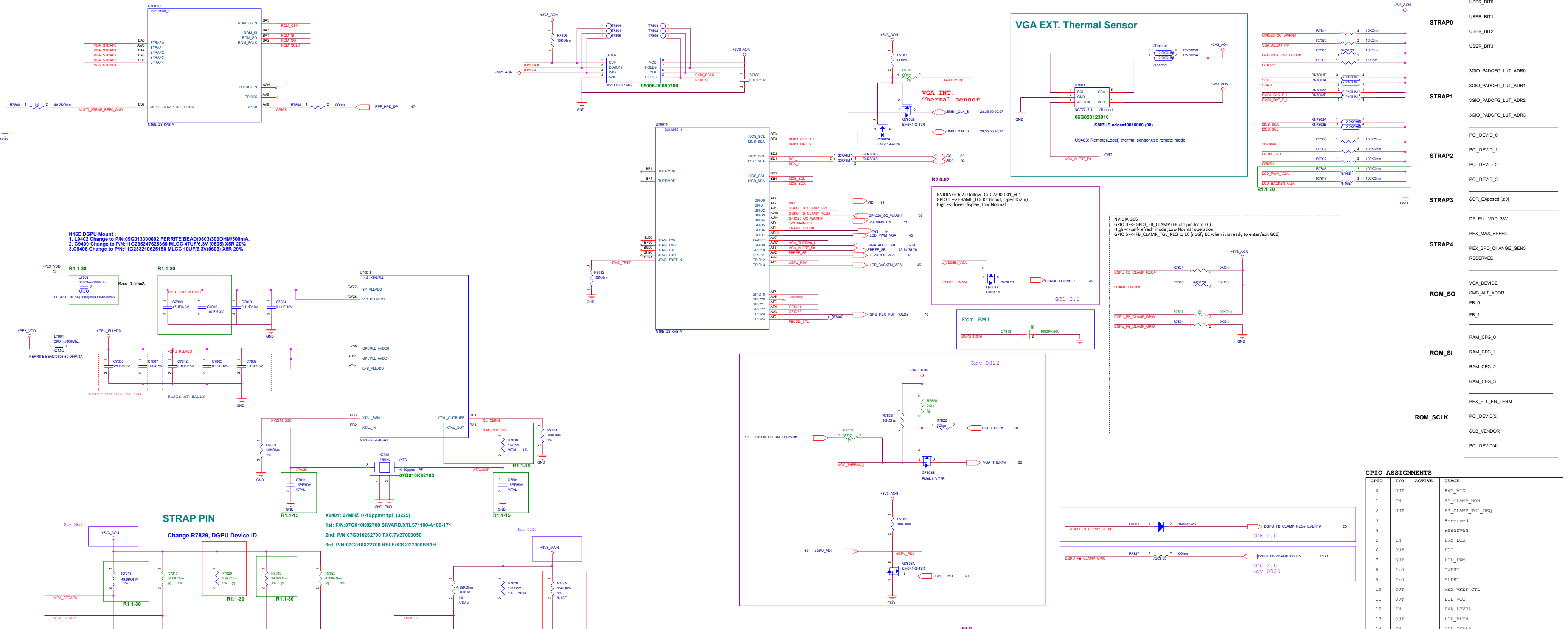
ASUS	Project Name: G752VY	Rev: 2.0
Title : OTH*		
Size: B	Dept.: ASUSTeK COMPUTER INC. I	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 68 of 102	

EMI



For RF requirement

ASUS	Project Name: G752VY	Rev: 2.0
Title : OTH EMI CAPS		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu
Date: Tuesday, July 21, 2015	Sheet 69 of 102	



VGA EXT. Thermal Sensor
VGA INT. Thermal sensor
SMBUS addr=10010000 (90)
U9403: Remote(Local) thermal sensor,use remote mode.
N16E DGPU Mount :
1. L9402 Change to P/N:09G013300602 FERRITE BEAD(0603)300OHM/500mA.
2. C9409 Change to P/N:11G235247625360 MLCC 47UF/6.3V (0805) X5R 20%
3.C9406 Change to P/N:11G233210625150 MLCC 10UF/6.3V(0603) X5R 20%
Max 150mA
PLACE OUTSIDE OF BGA
PLACE AT BALLS
NVIDIA GC6 2.0 follow DG-07290-001_v01
GPIO 5 --> FRAME_LOCK# (Input, Open Drain)
High -->driver display ,Low Normal
NVIDIA GC6
GPIO 0 --> GPIO_FB_CLAMP (FB ctrl pin from EC)
High --> self-refresh mode ,Low Normal operation
GPIO 6 --> FB_CLAMP_TGL_REQ (notify EC when it is ready to enter/exit GC6)
For EMI
Roy 0822
STRAP PIN
Change R7829, DGPU Device ID
X9401: 27MHZ +/-10ppm/11pF (3225)
1st: P/N:07G010K82700 SIWARD/XTL571100-A180-171
2nd: P/N:07G010262700 TXC/7V27000050
3rd: P/N:07G010X22700 HELE/X3G027000BB1H
Change R7809, For NV request
Change R7835, VRAM Vendor
STRAP0
USER_BIT0
USER_BIT1
USER_BIT2
USER_BIT3
3GIO_PADCFG_LUT_ADR0
3GIO_PADCFG_LUT_ADR1
STRAP1
3GIO_PADCFG_LUT_ADR2
3GIO_PADCFG_LUT_ADR3
PCI_DEVID_0
PCI_DEVID_1
STRAP2
PCI_DEVID_2
PCI_DEVID_3
STRAP3
SOR_EXposed [3:0]
DP_PLL_VDD_33V
PEX_MAX_SPEED
STRAP4
PEX_SPD_CHANGE_GEN3
RESERVED
VGA_DEVICE
ROM_SO
SMB_ALT_ADDR
FB_0
FB_1
RAM_CFG_0
ROM_SI
RAM_CFG_1
RAM_CFG_2
RAM_CFG_3
PEX_PLL_EN_TERM
ROM_SCLK
PCI_DEVID[5]
SUB_VENDOR
PCI_DEVID[4]

R1.0

N16E-GS-KAB-A1 P/N: 02004-00410600(PS)				
N16E-GS-KCD-A1 P/N: 02004-00410500(PS)				
DEVICE ID	0x13D9			
STRAP0	49.9K PU	ROM_SCLK		24.9K PH
STRAP1	No Stuffed	ROM_SI	128Mb x 32	Micron A-die: 24.9K PD
STRAP2	No Stuffed			
STRAP3	No Stuffed			Hynix M-die: 15K PD
STRAP4	No Stuffed			
		ROM_SO		10K PD

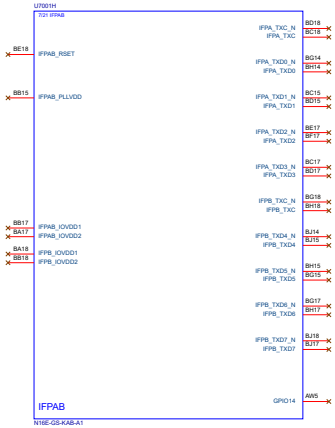
USE GDDR5 VRAM 128Mb x 32 (512MB)
1nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (A-die) ,Strap: 0x4
2nd: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2
Hynix strap 0x2 HYNIX/H5GC4H24MFR-T2C - 15Kohm
Micron strap 0x4 Micron/EDW4032BABG-60-F - 24.9Kohm

	3V3	GND
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111
	PU	PD

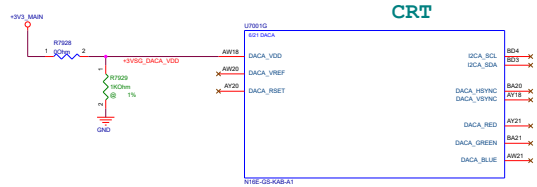
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	OUT		PWM_VID
1	IN		FB_CLAMP_MON
2	OUT		FB_CLAMP_TGL_REQ
3			Reserved
4			Reserved
5	IN		FRM_LCK
6	OUT		PSI
7	OUT		LCD_PWM
8	I/O		OVERT
9	I/O		ALERT
10	OUT		MEM_VREF_CTL
11	OUT		LCD_VCC
12	IN		PWR_LEVEL
13	OUT		LCD_BLEN
14	IN		HPD_IFPAB
15	IN		HPD_IFPC
16	IN		HPD_IFPF OR HPD_IFPD
17	IN		HPF_IFPD
18	IN		HPD_IFPE
19	OUT		3DVision
20			Reserved
21	I/O		RASTER_SYNC
22	IN		SWAP_RDY
23			Reserved
24	OUT		MEM_VDD_CTL

LVDS



CRT

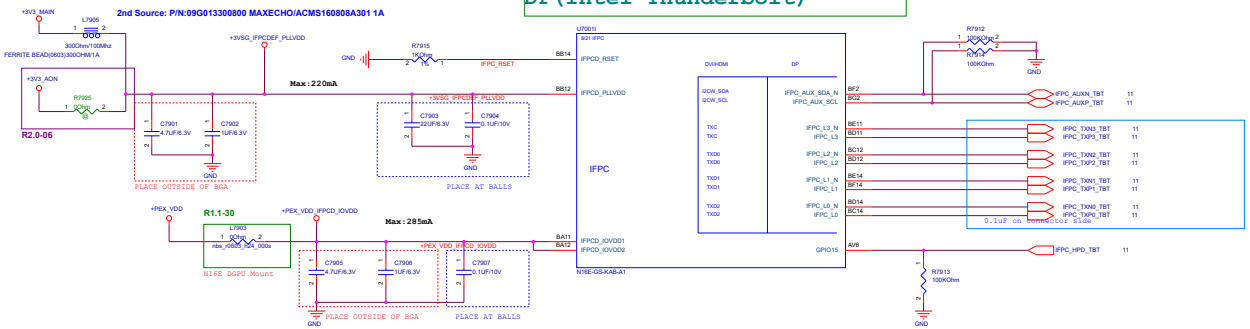


DP(Intel Thunderbolt)

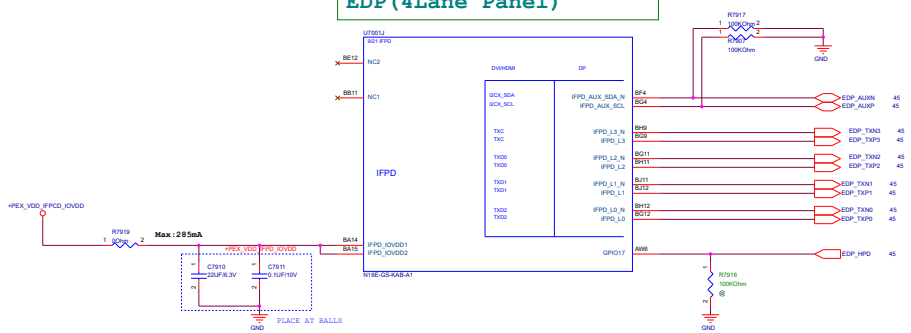
L7901 FERRITE BEAD(0603)300OHM/1A

1st Source: P/N:09G013300801 TAI-TECH/HCB1608KF-301T10

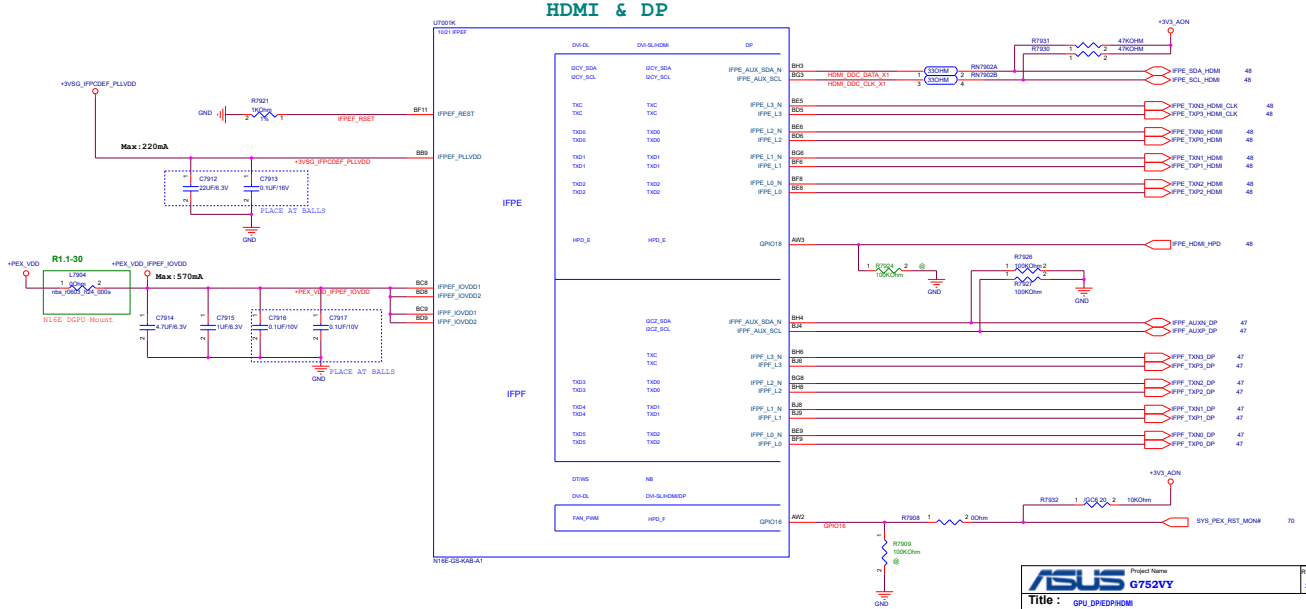
2nd Source: P/N:09G013300800 MAXECHO/ACMS1608080A301 1A



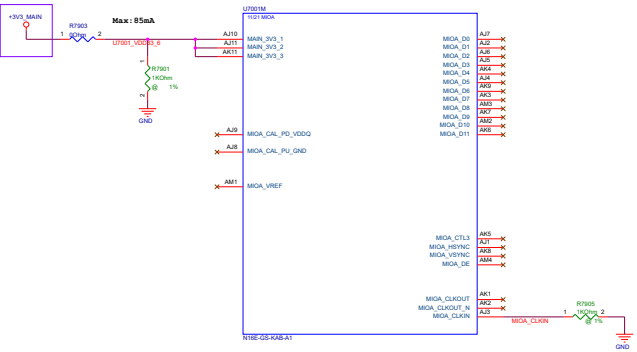
EDP(4Lane Panel)



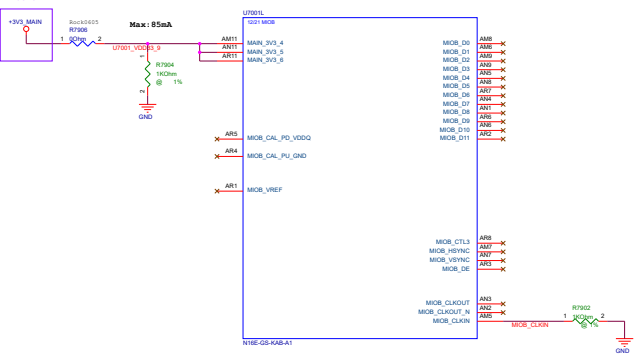
HDMI & DP



NV 0823

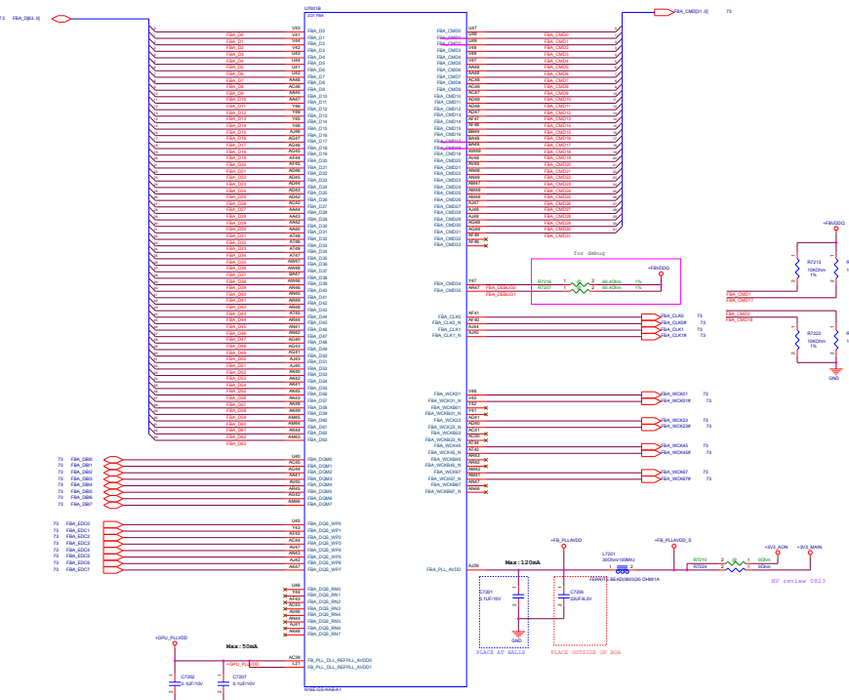


NV 0823

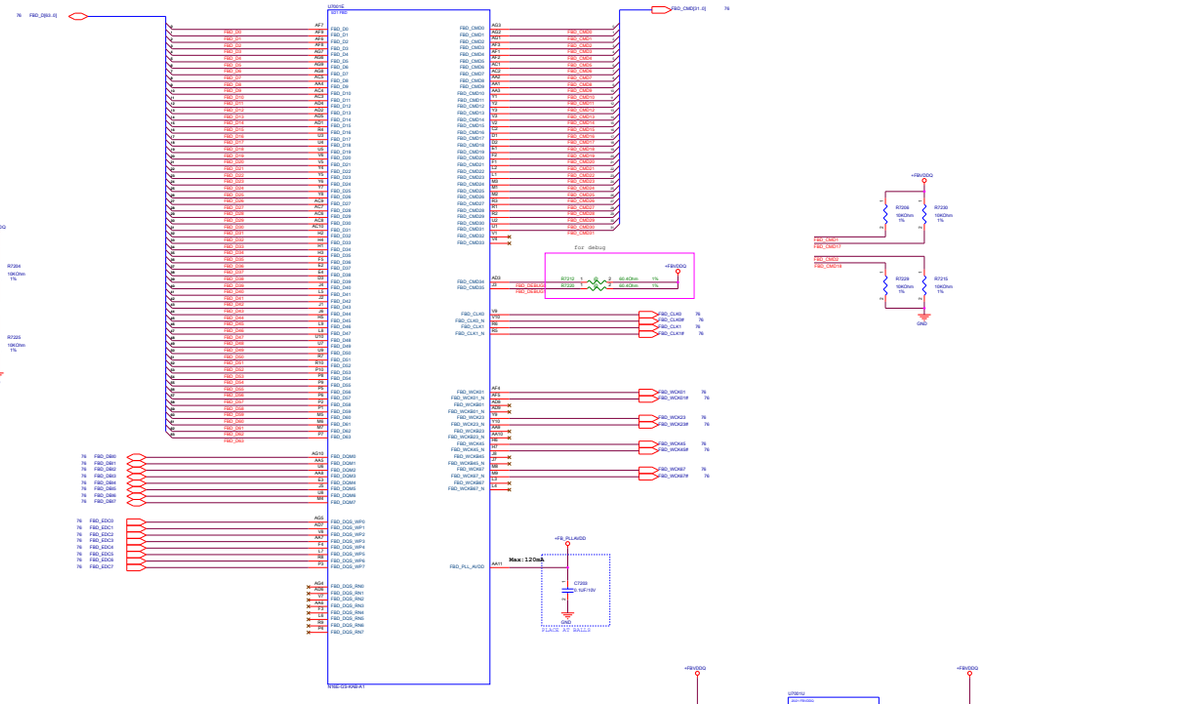


Project Name: G752VY			Rev: 2.0
Title: GPU_DP/EDP/HDMI			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE1_RD3	
Date: Tuesday, July 21, 2015	Sheet: 79	of: 102	

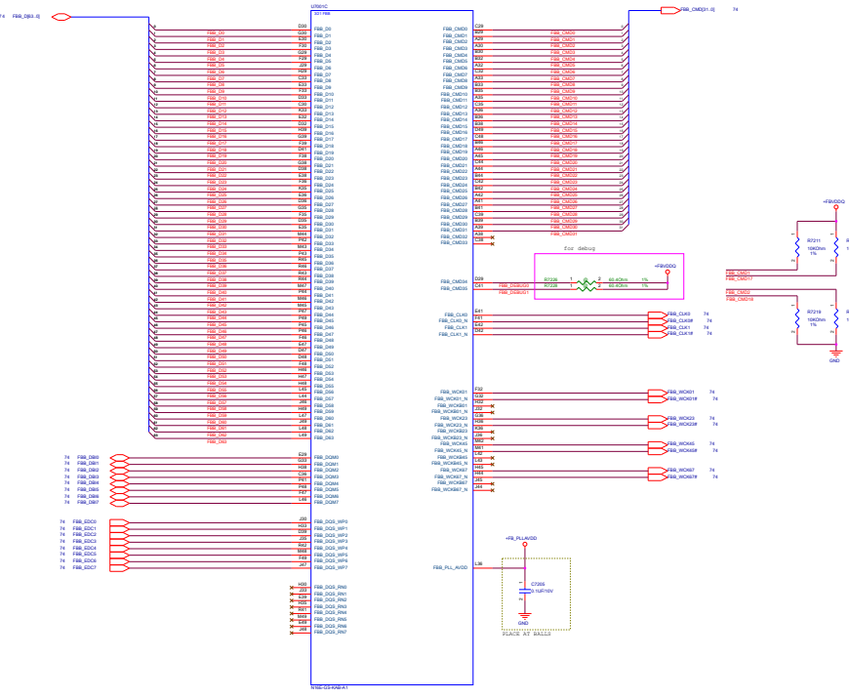
MEMORY: GPU FB Partition A



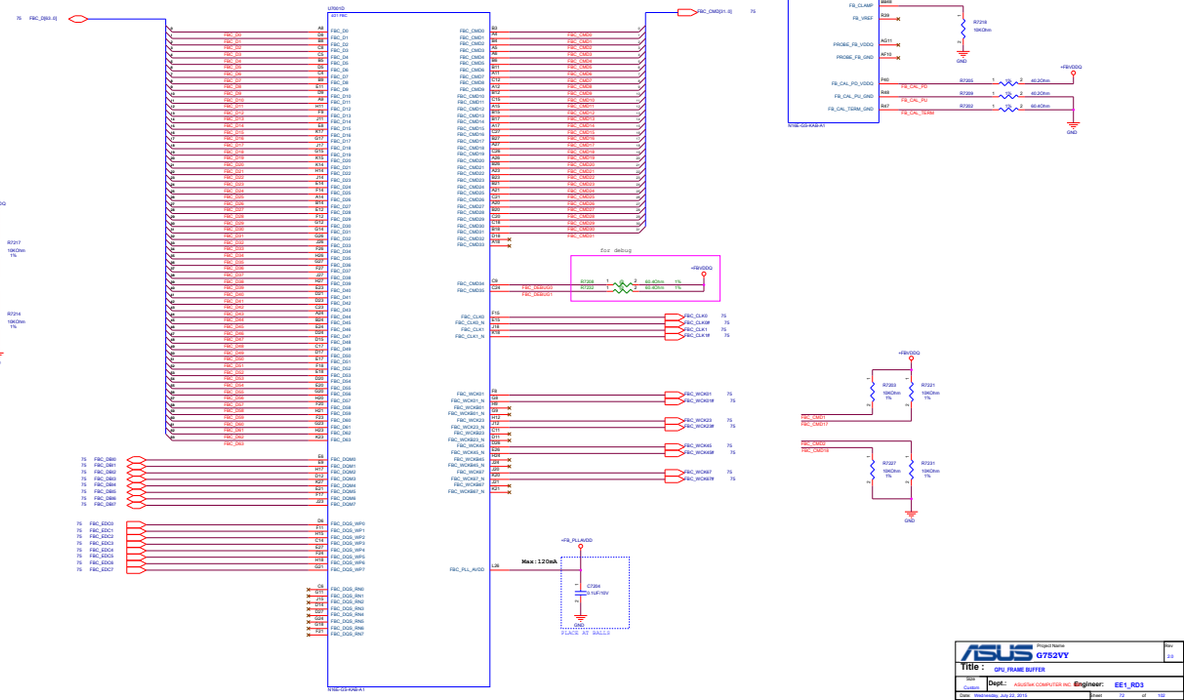
MEMORY: GPU FB Partition D



MEMORY: GPU FB Partition B

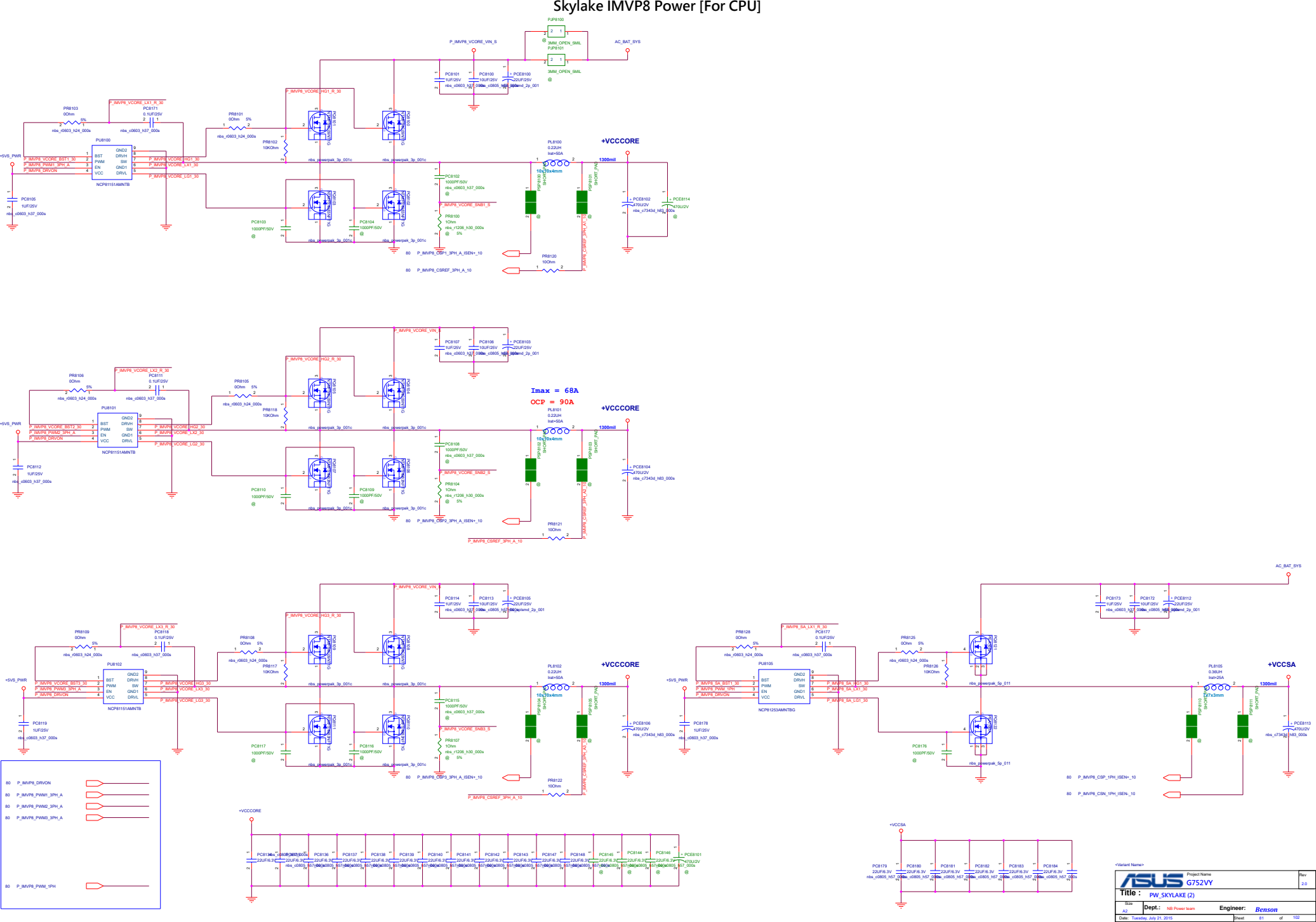


MEMORY: GPU FB Partition C



ASUS	Project Name: G752VY		Rev: 2.0
Title : GPU_FRAME BUFFER			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE1_RD3	
Date: Wednesday, July 02, 2015		Sheet 72 of 102	

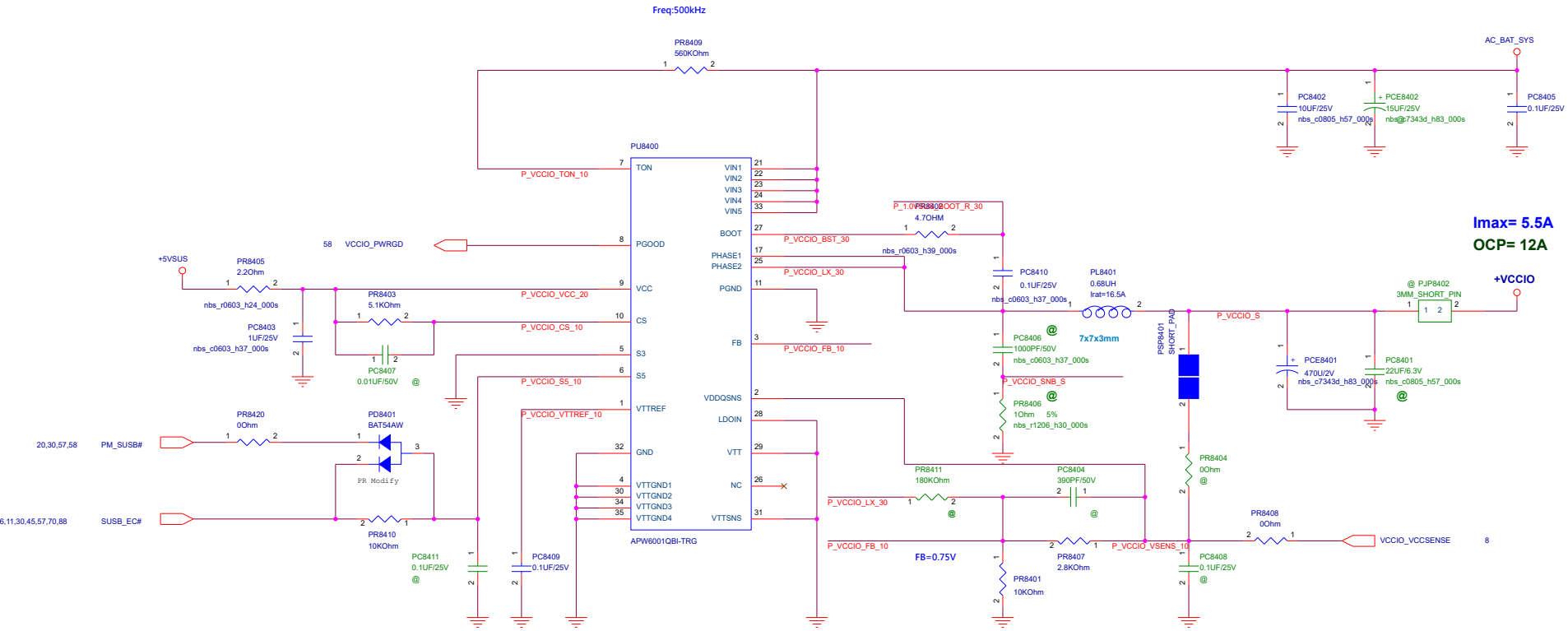
Skylake IMVP8 Power [For CPU]



<Variant Name>
ASUS Project Name G752VY Rev 2.0
Title : PW_SKYLAKE (2)
Size A2 Dept.: NB Power team Engineer: Benson
Date: Tuesday, July 21, 2015 Sheet 81 of 102

Project Name: G752VY		Rev: 2.0
Title : POWER_+VGFX_CORE		
Size: A	Dept.: NB Power team	Engineer: Benson Hsu
Date: Tuesday, July 21, 2015	Sheet 82 of 102	

+VCCIO [For CPU]

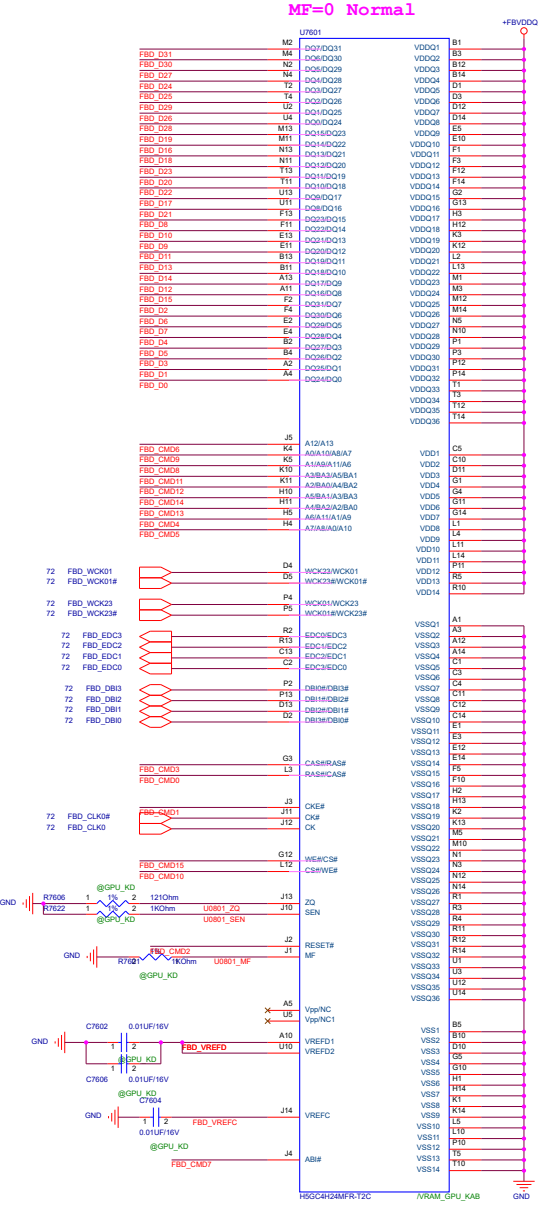


<Variant Name>

ASUS	Project Name: G752VY		Rev: 2.0
Title : PW_+VCCIO			
Size: A3	Dept.: NB Power Team	Engineer: Benson	
Date: Tuesday, July 21, 2015	Sheet 84 of 102		

FBD Partition Memory (1 of 2)

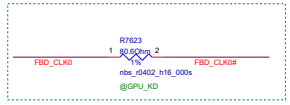
MF=0 Normal

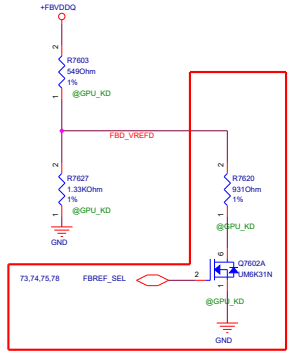


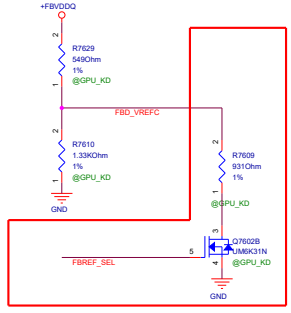
GDD5 MODE SELECTION

MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

CK External Termination







R1.3-02 R1.2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)

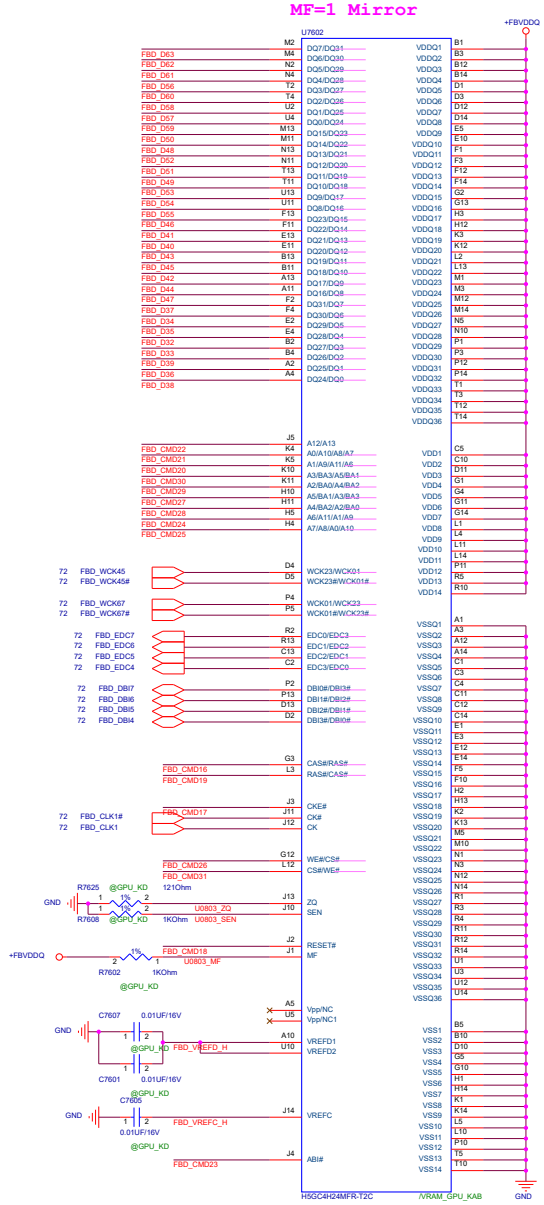
1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

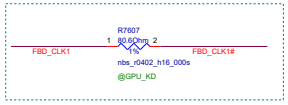
3nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

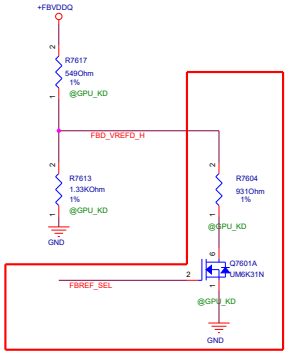
FBD Partition Memory (2 of 2)

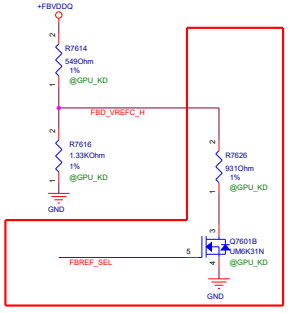
MF=1 Mirror



CK External Termination







R1.3-02 R1.2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)

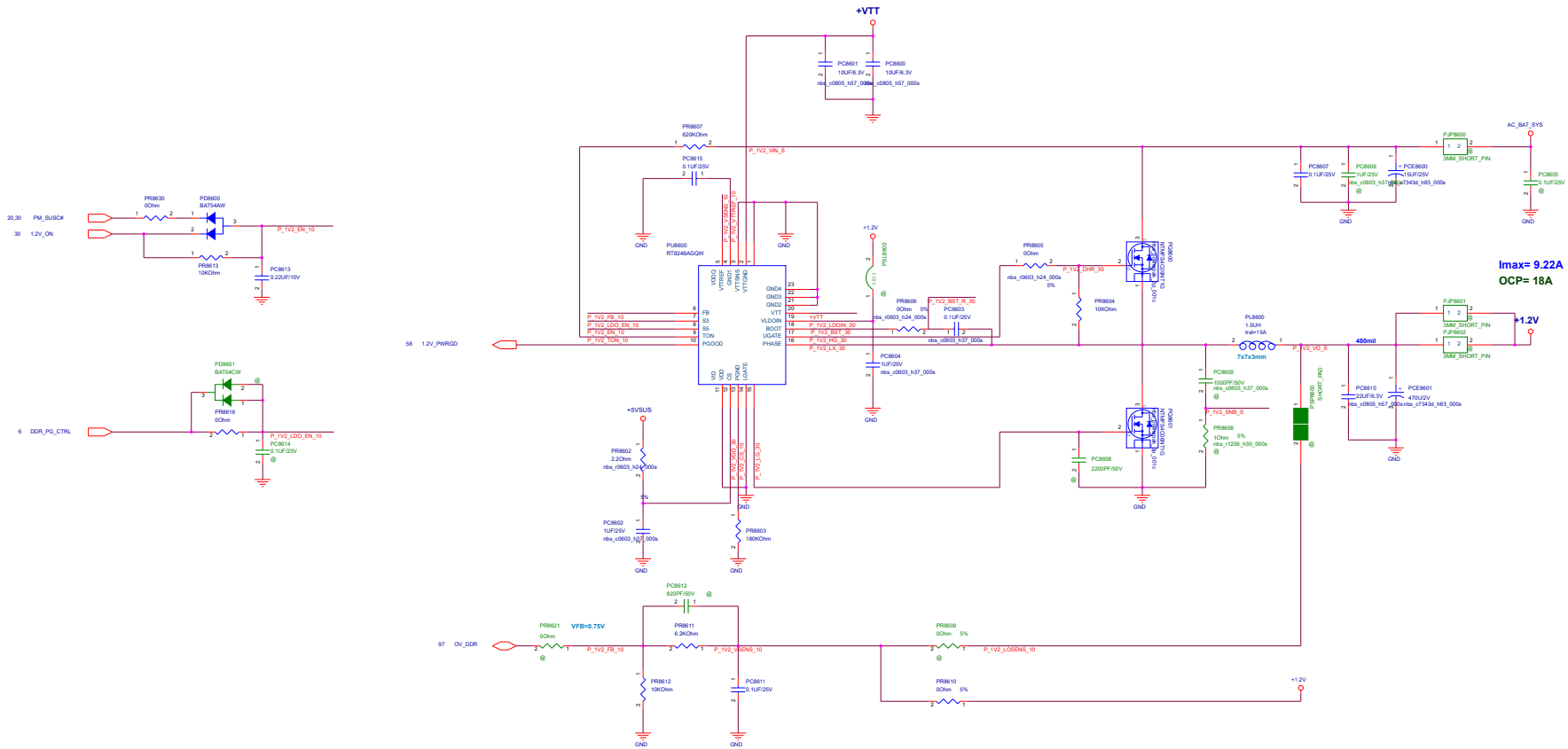
1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

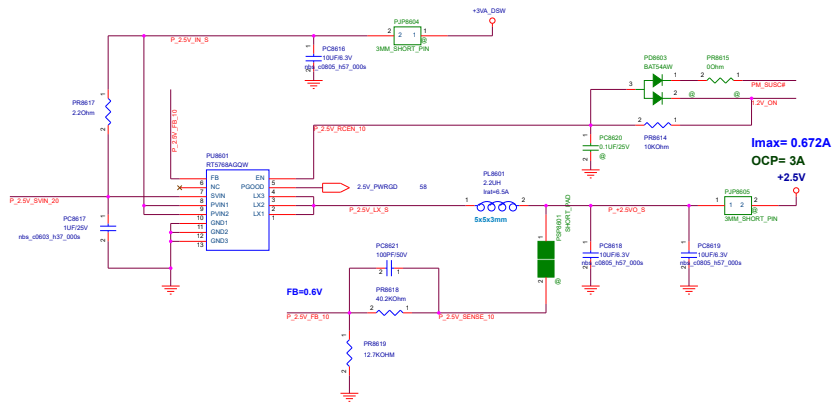
2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

3nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

ASUS	Project Name: G752VY	Rev: 2.0
Title : VRAM-CHANNEL D		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE1_RD3
Date: Tuesday, July 21, 2015	Sheet 76 of 102	

+1.2V / VTT / 2.5V[For Memory]

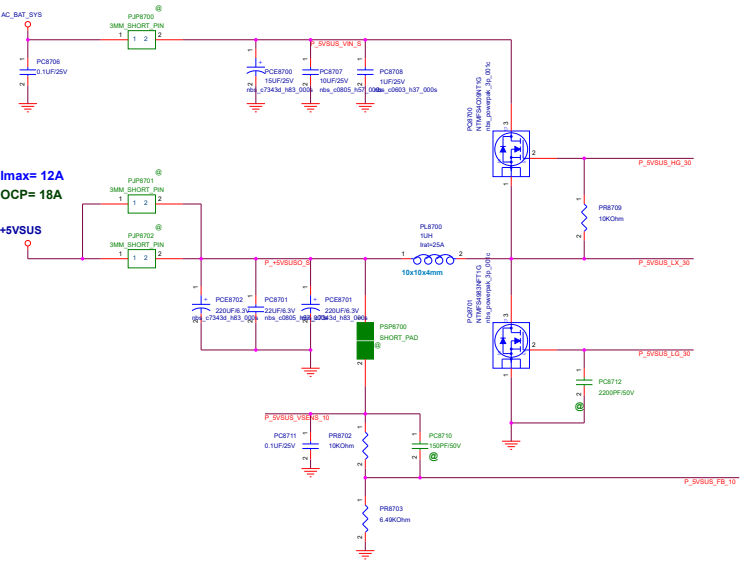


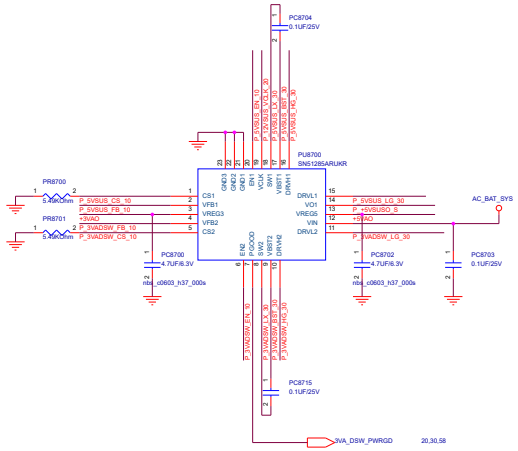


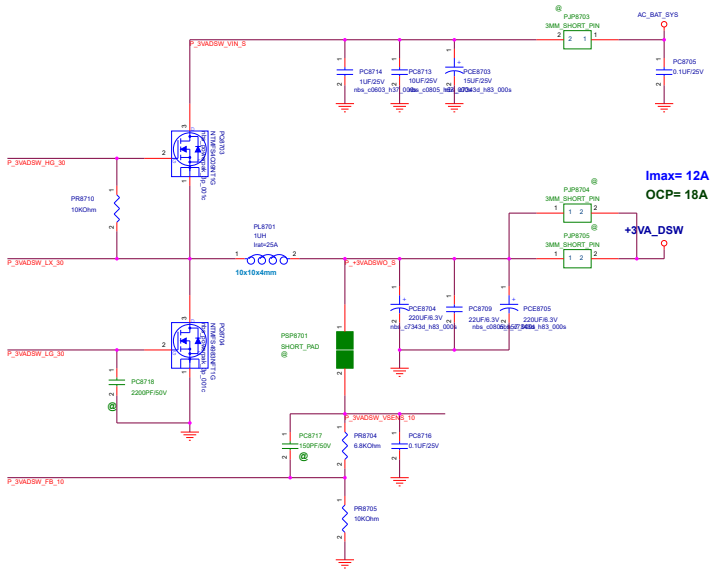
<Core Design>

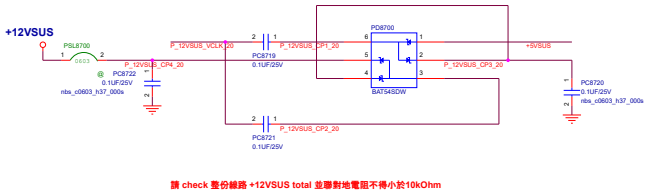
ASUS	Project Name: G752VY		Rev: 2.0
Title : PW_+1.2V/+VTT/+2.5V			
Size: A2	Dept.: NB Power team	Engineer: Benson	
Date: Tuesday, July 21, 2015	Sheet 86 of 102		

+3VA_DSW / +5VSUS [System Power]

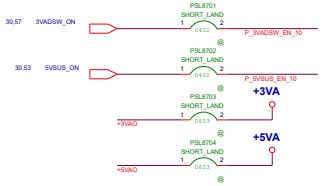


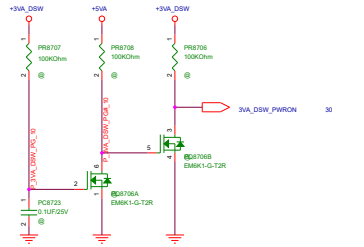






請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm



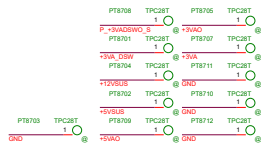


Adaptor Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	0	-	0
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP8)

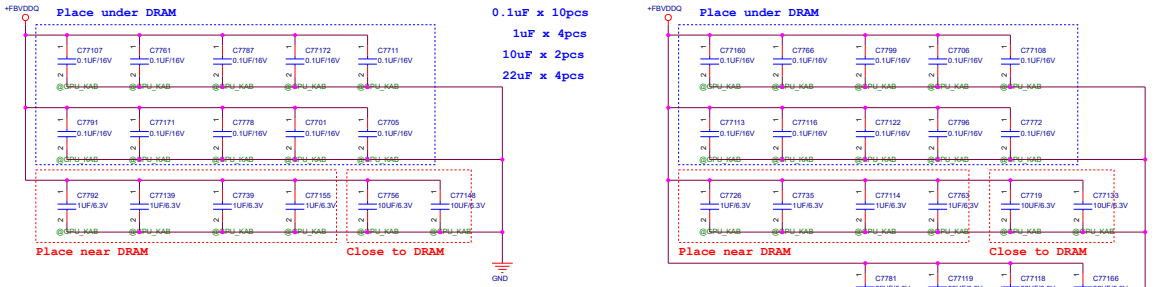
	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0



<variant_name>

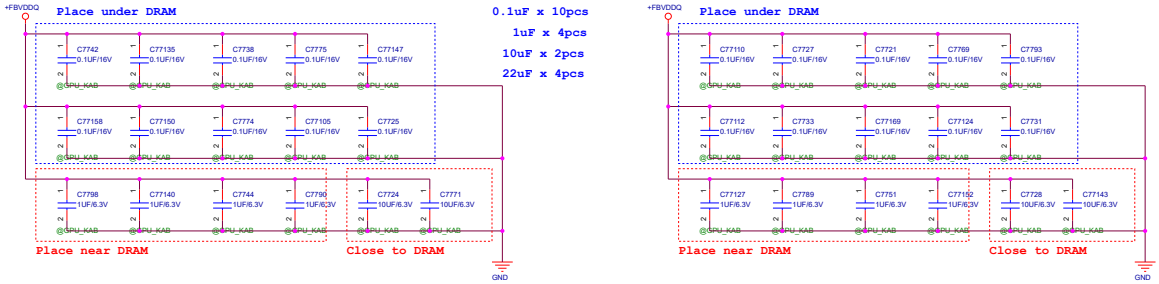
ASUS	Project Name: G752VY	Rev: 2.0
Title : PW_+3VA_DSW/+5VSUS		
Size: A2	Dept.: NB Power team	Engineer: Benson
Date: Tuesday, July 21, 2015	Sheet 87 of 102	

Chanel A



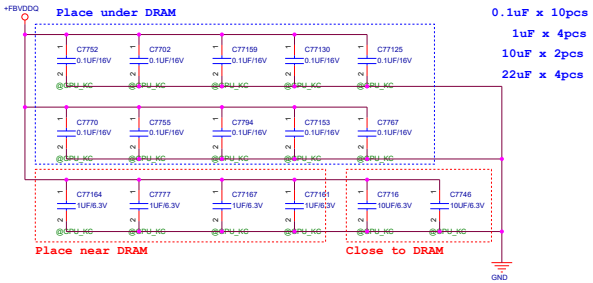
VRAM

Chanel B

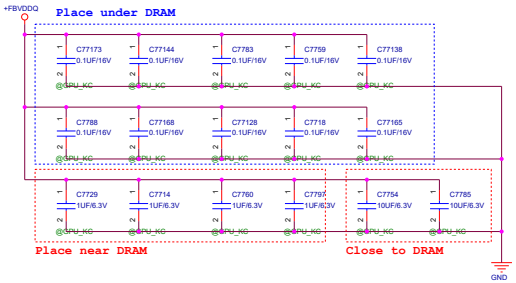


VRAM

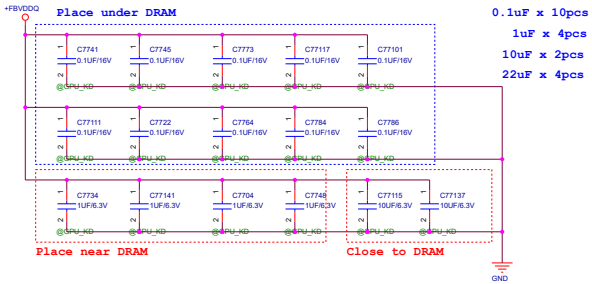
Chanel C



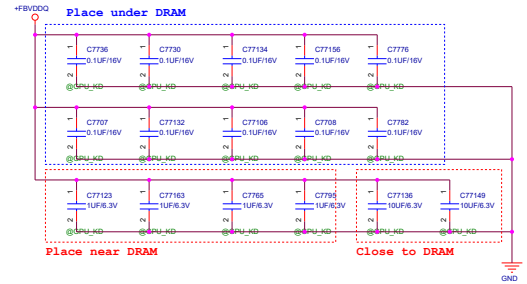
VRAM



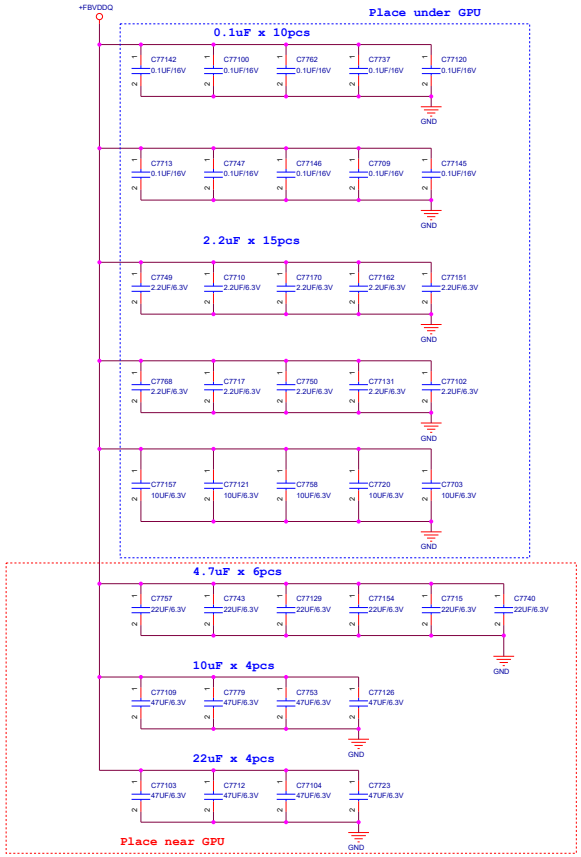
Chanel D



VRAM

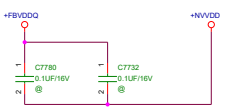


VRAM PWR_FBVDDQ

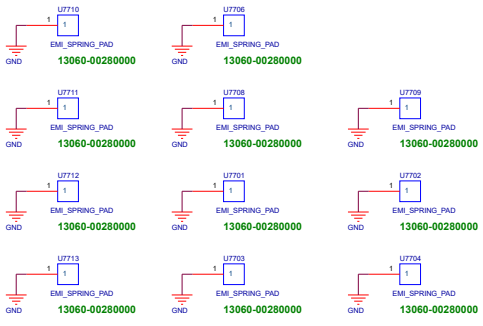


DGPU EMI GND Pad

EMI



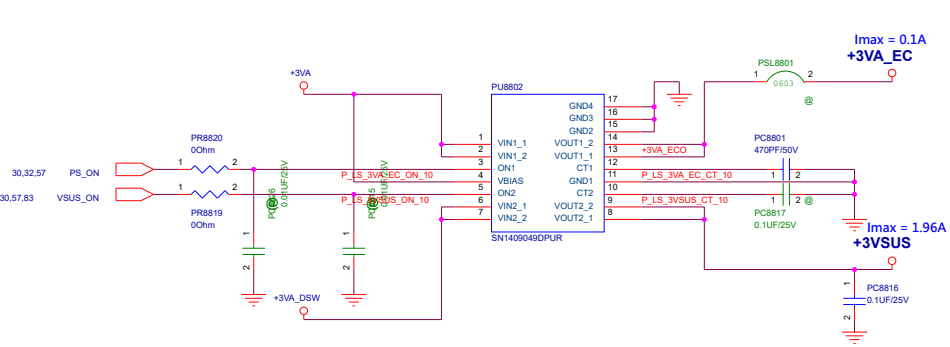
EMI DGPU Spring

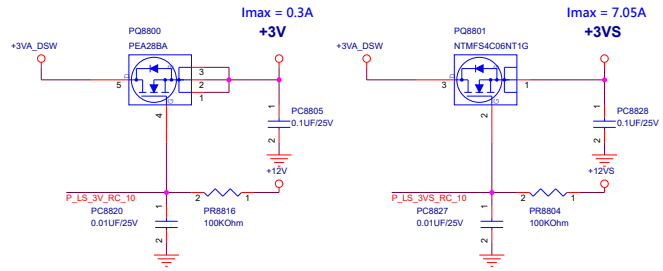


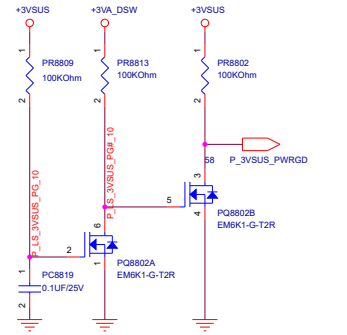
ASUSTeK COMPUTER INC. NB1	Title :	VRAM CAP.	
	Engineer:	Wenchi_Shen	
Size: C	Project Name: G752VY		Rev: 2.0
Date: Tuesday, July 21, 2015	Sheet 77 of 102		

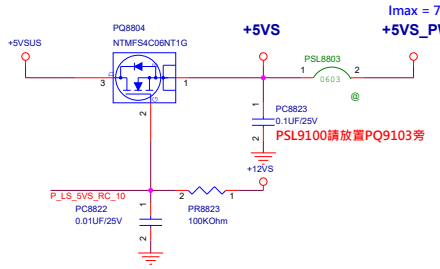
Load Switch

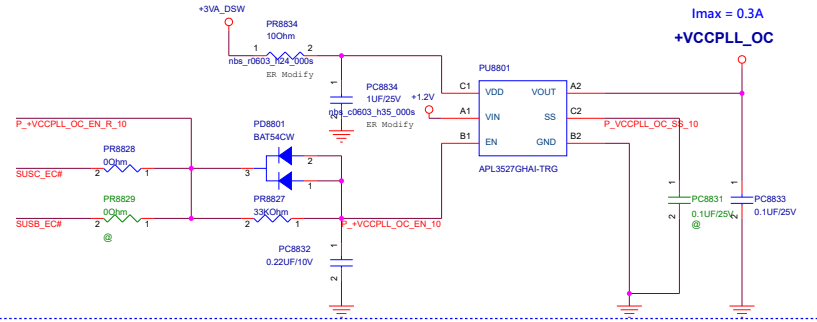
Main Board



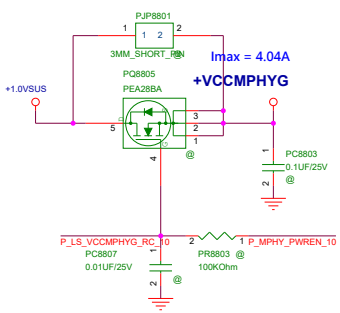


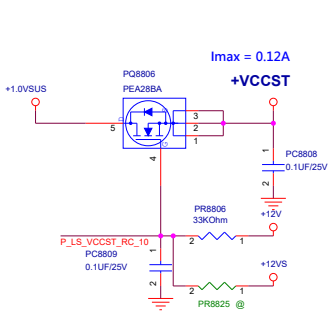


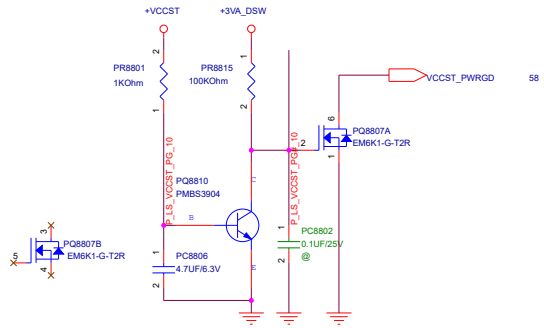


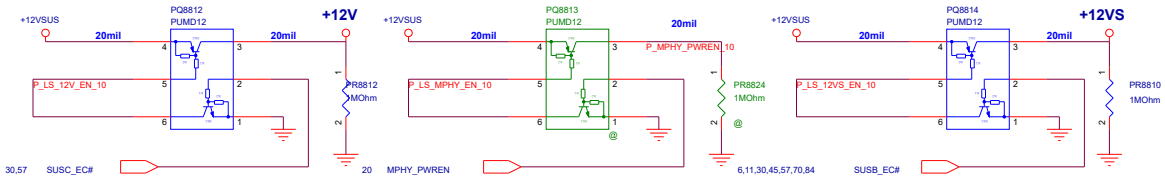


PJP8801 需開鋼板

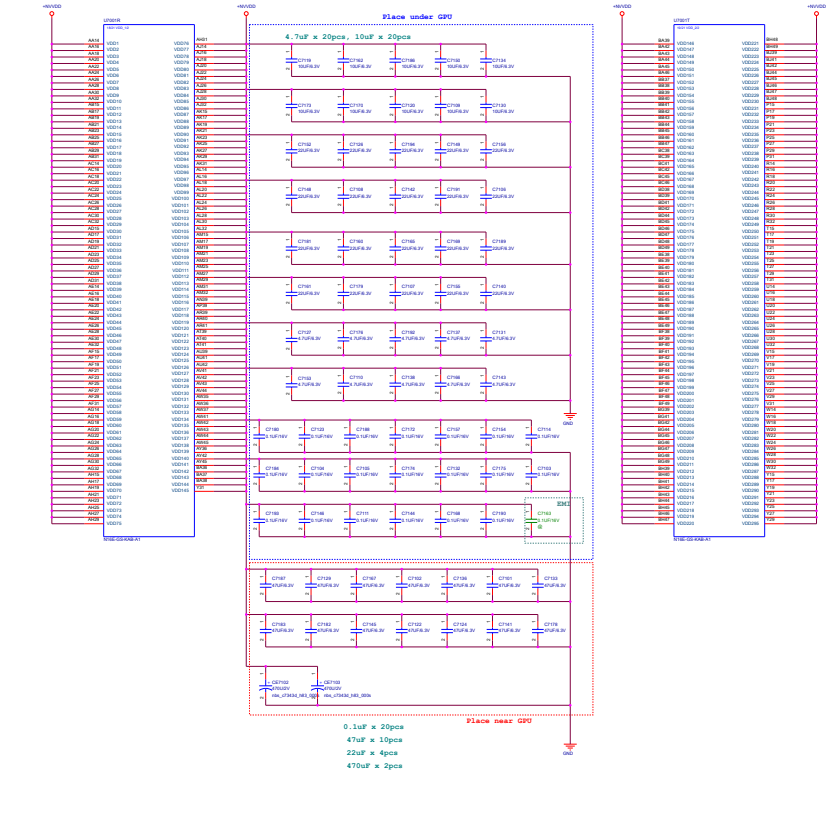


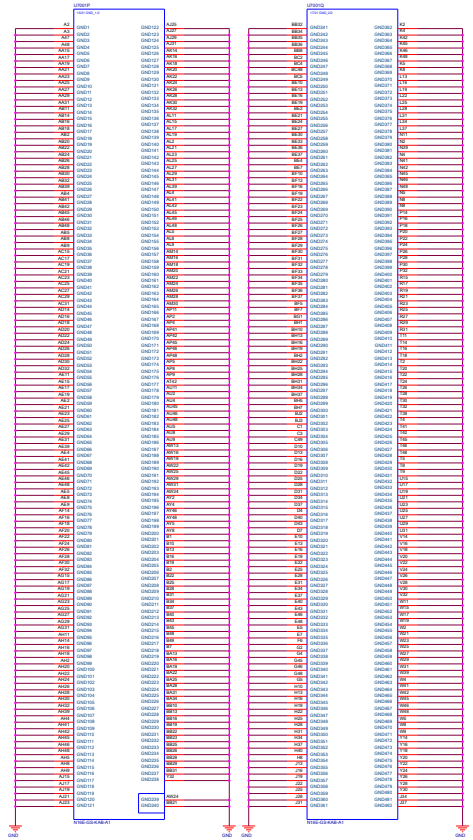


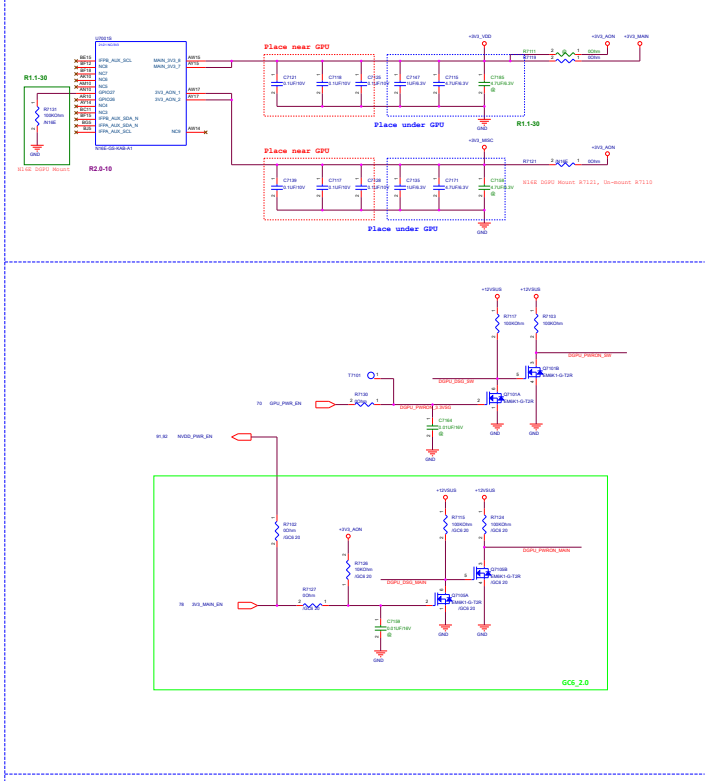


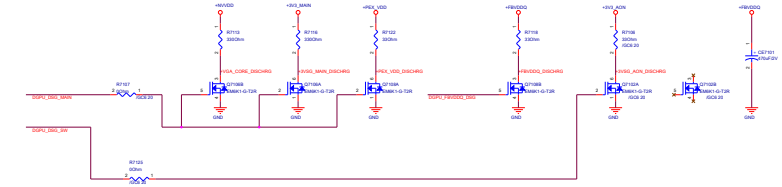


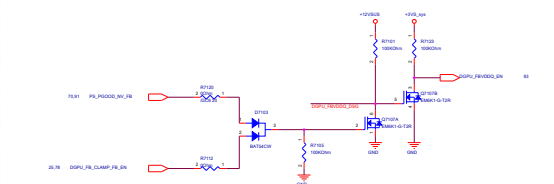
ASUS	Project Name: G752VY		Rev: 2.0
Title : PW_LOAD SWITCH			
Size: A3	Dept.: NB Power team	Engineer: Benson Hsu	
Date: Tuesday, July 21, 2015		Sheet 88 of 102	

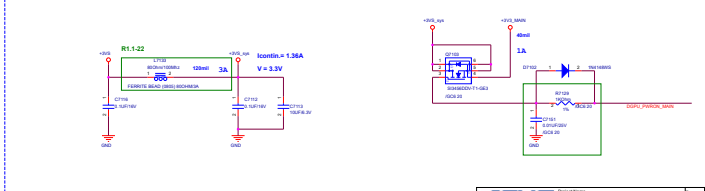




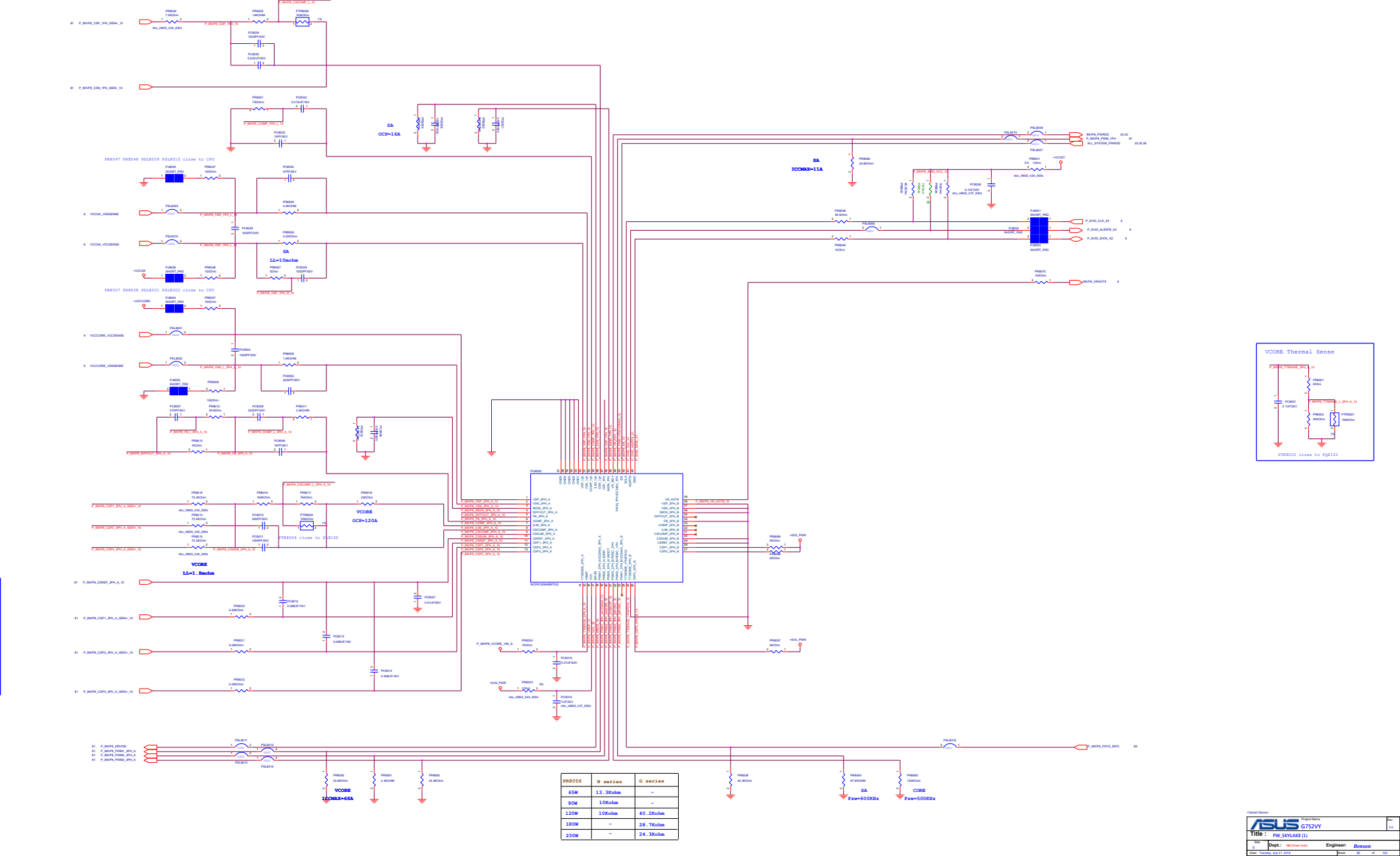








ASUS	Project Name: G752VY		Rev: 3.0
Title : GPU_POWER			
Size: D	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE1_RD3	
Date: Tuesday, July 21, 2015	Sheet: 71 of 102		



Project Name	G752VY	Rev
Title :	PW_SKYLAKE (1)	
Dept.:	NB Power team	Engineer: Benson
Date: Tuesday, July 21, 2015	Sheet 80 of 102	

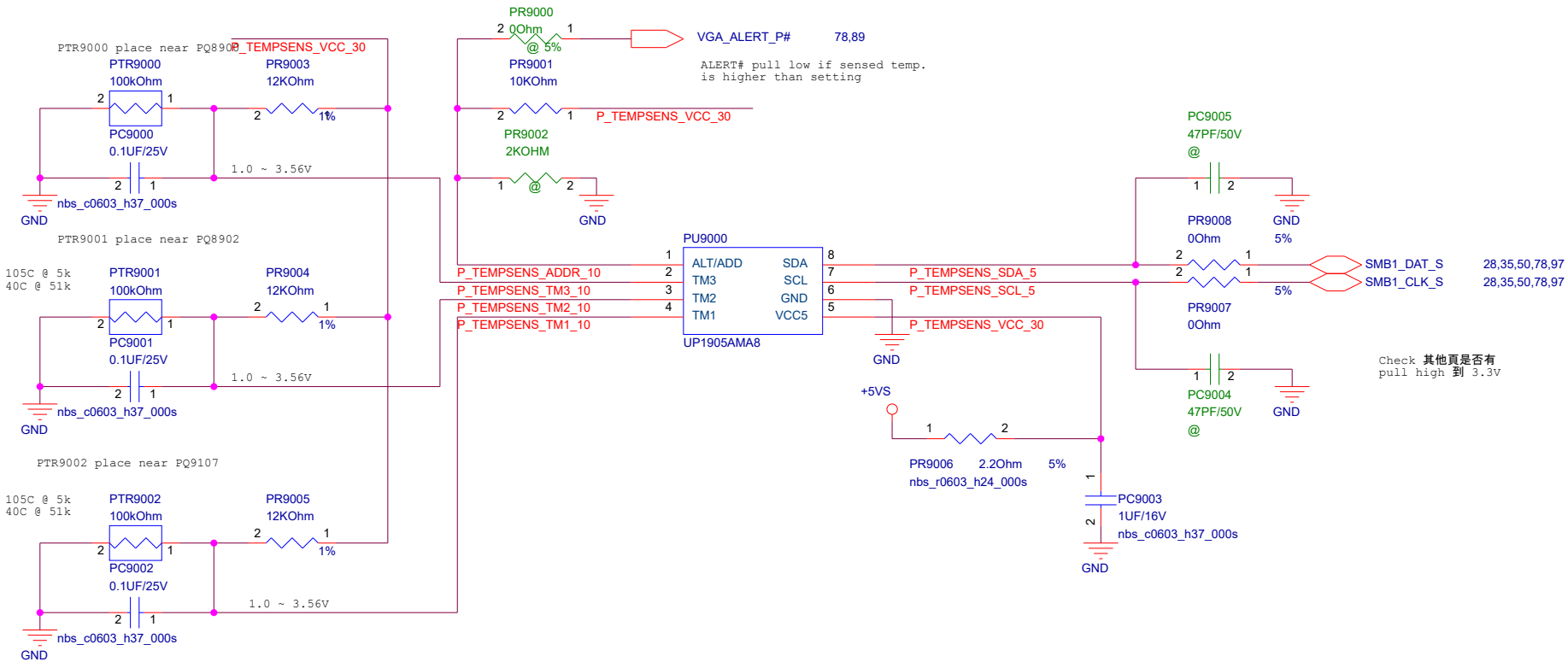
Main Board

Address Selection Table

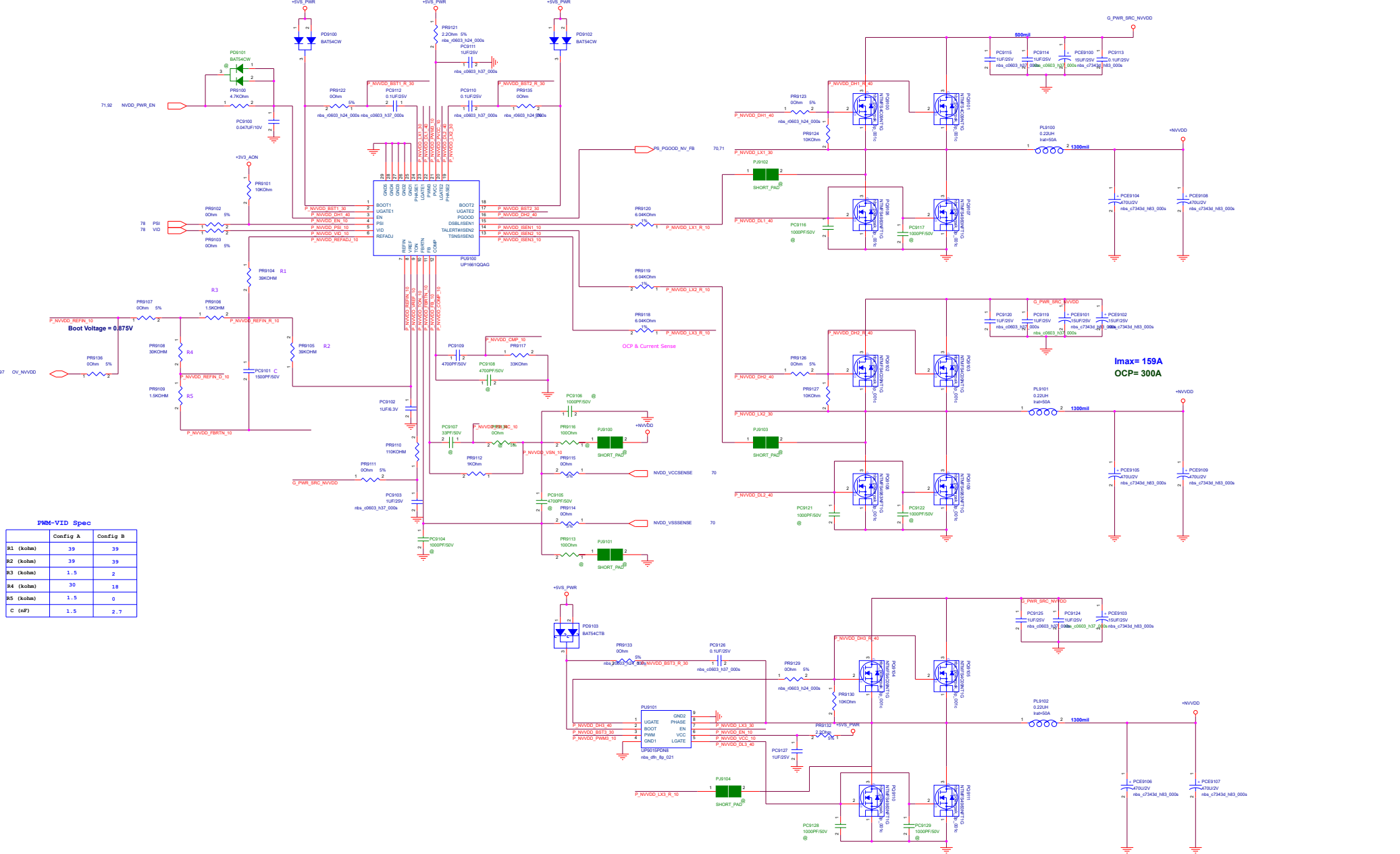
Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert



ASUS	Project Name: G752VY	Rev: 2.0
Title :	PW_PROTECTION	
Size: A4	Dept.: NB Power team	Engineer: Benson Hsu
Date: Tuesday, July 21, 2015	Sheet 90 of 102	



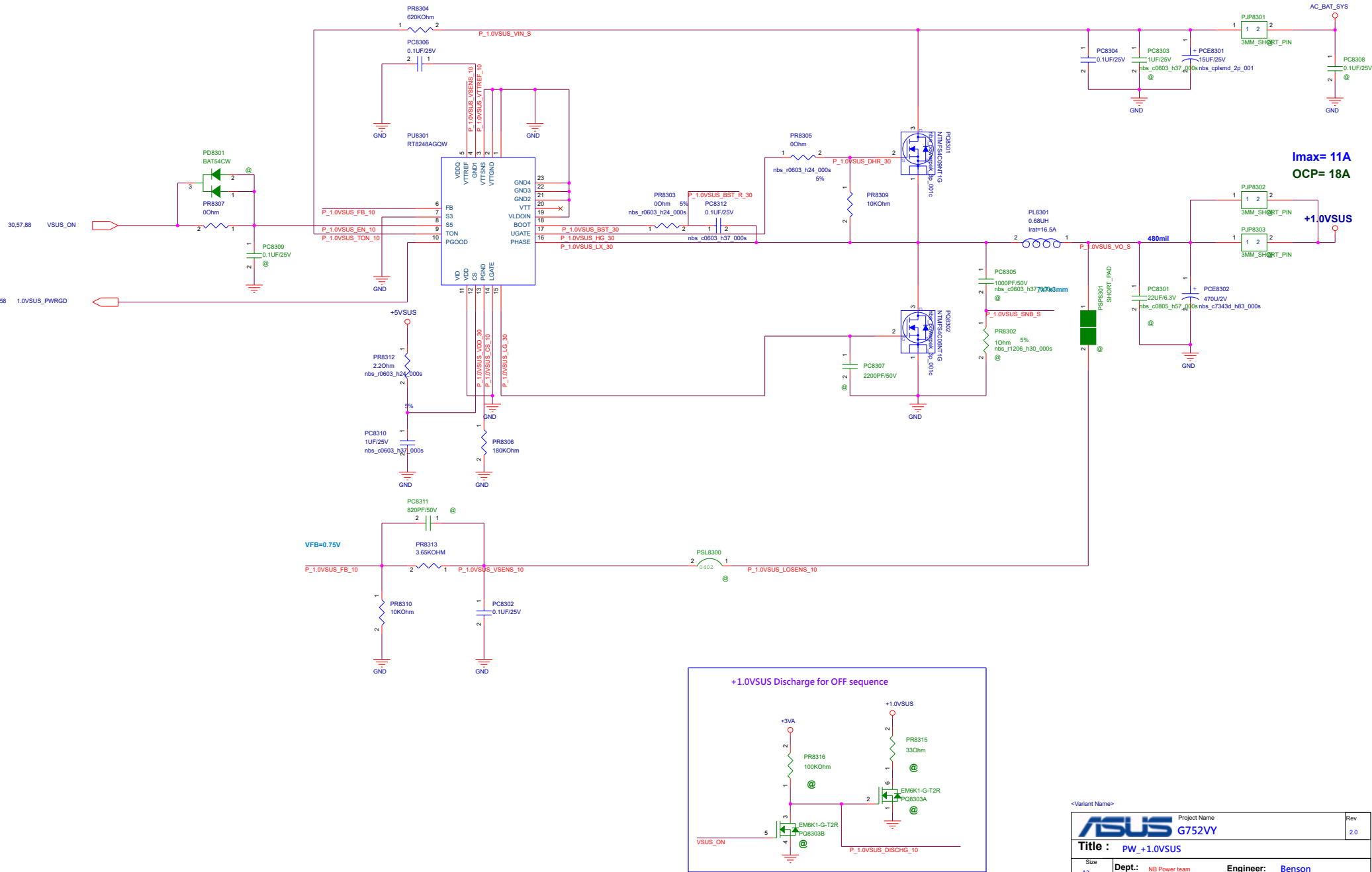
PWM-VID Spec

	Config A	Config B
R1 (kohm)	39	39
R2 (kohm)	39	39
R3 (kohm)	1.5	2
R4 (kohm)	30	18
R5 (kohm)	1.5	0
C (nF)	1.5	2.7

<Variant Name>

ASUS	Project Name: G752VY	Rev: 2.0
Title : PW_+NVVDD		
Size: A2	Dept.: NB Power Team	Engineer: Benson
Date: Tuesday, July 21, 2015	Sheet 91 of 102	

+1.0VSUS [For PCH]

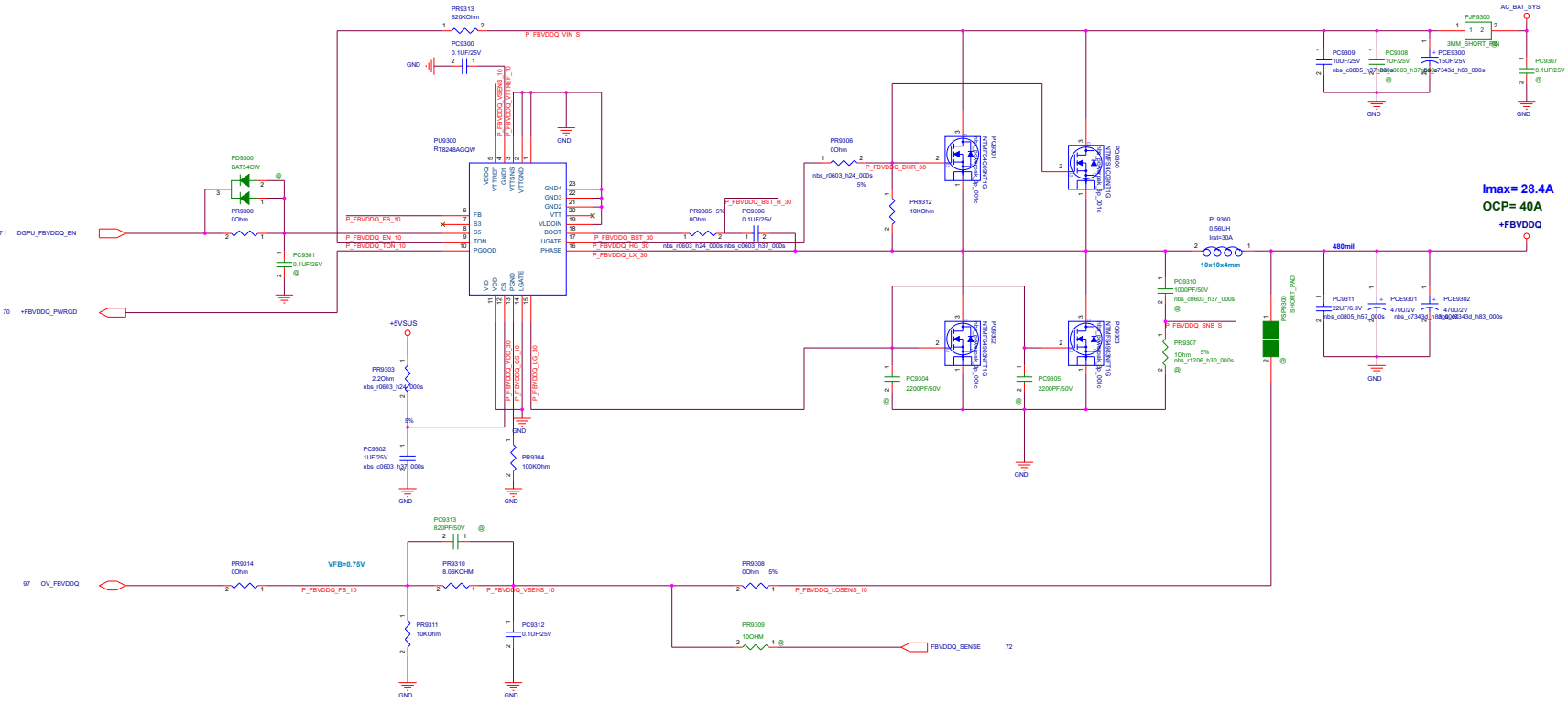


+1.0VSUS Discharge for OFF sequence

<Variant Name>

ASUS	Project Name: G752VY	Rev: 2.0
Title : PW_+1.0VSUS		
Size: A3	Dept.: NB Power team	Engineer: Benson
Date: Tuesday, July 21, 2015	Sheet 83 of 102	

+FBVDDQ [For FRAM]



Project Name

G752VY

Rev

2.0

Title : POWER_+VGFX_CORE

Size

A

Dept.: NB Power team

Engineer: Benson Hsu

Date: Tuesday, July 21, 2015

Sheet 85 of 102

Project Name

G752VY

Rev

2.0

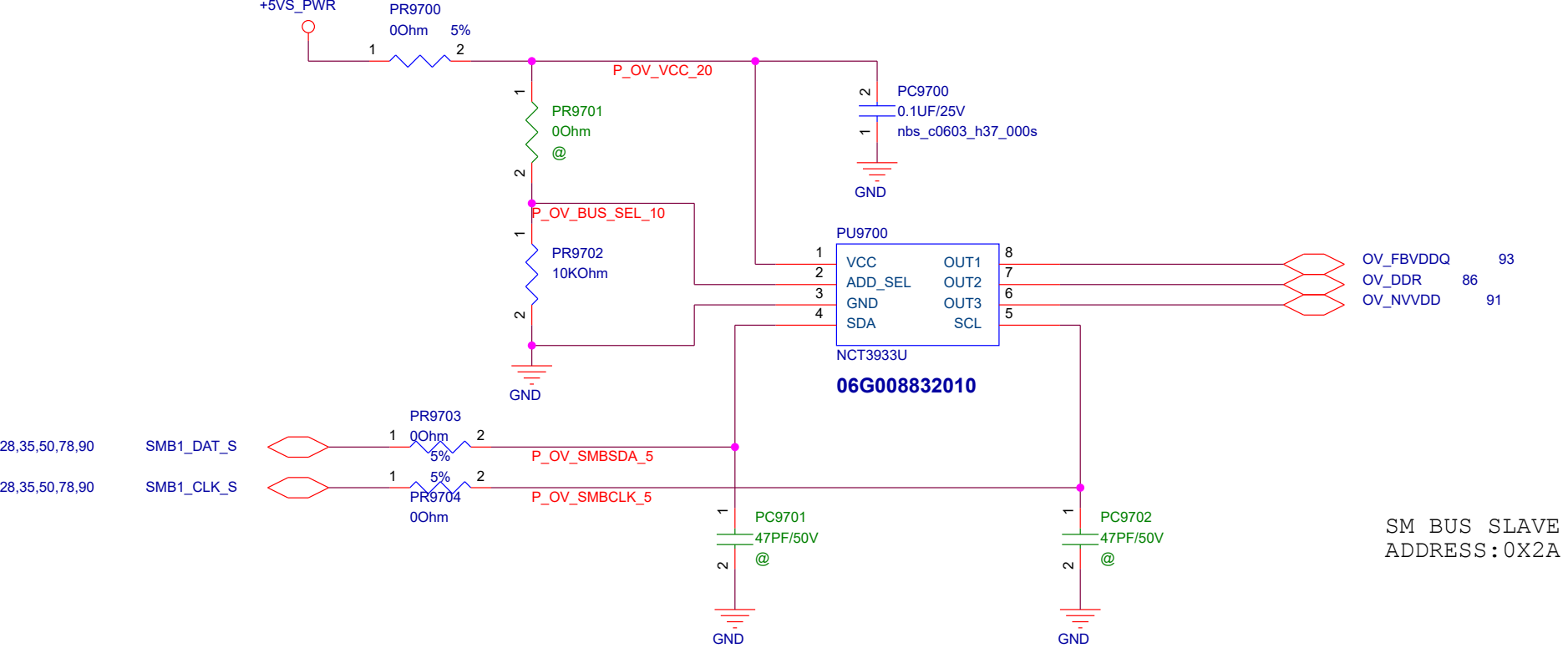
Title : INPUT SENSE

Size	Dept.:	Engineer:
Custom	ASUS PWR NB1	Joe

Date:	Sheet	of
Tuesday, July 21, 2015	94	102

Main Board

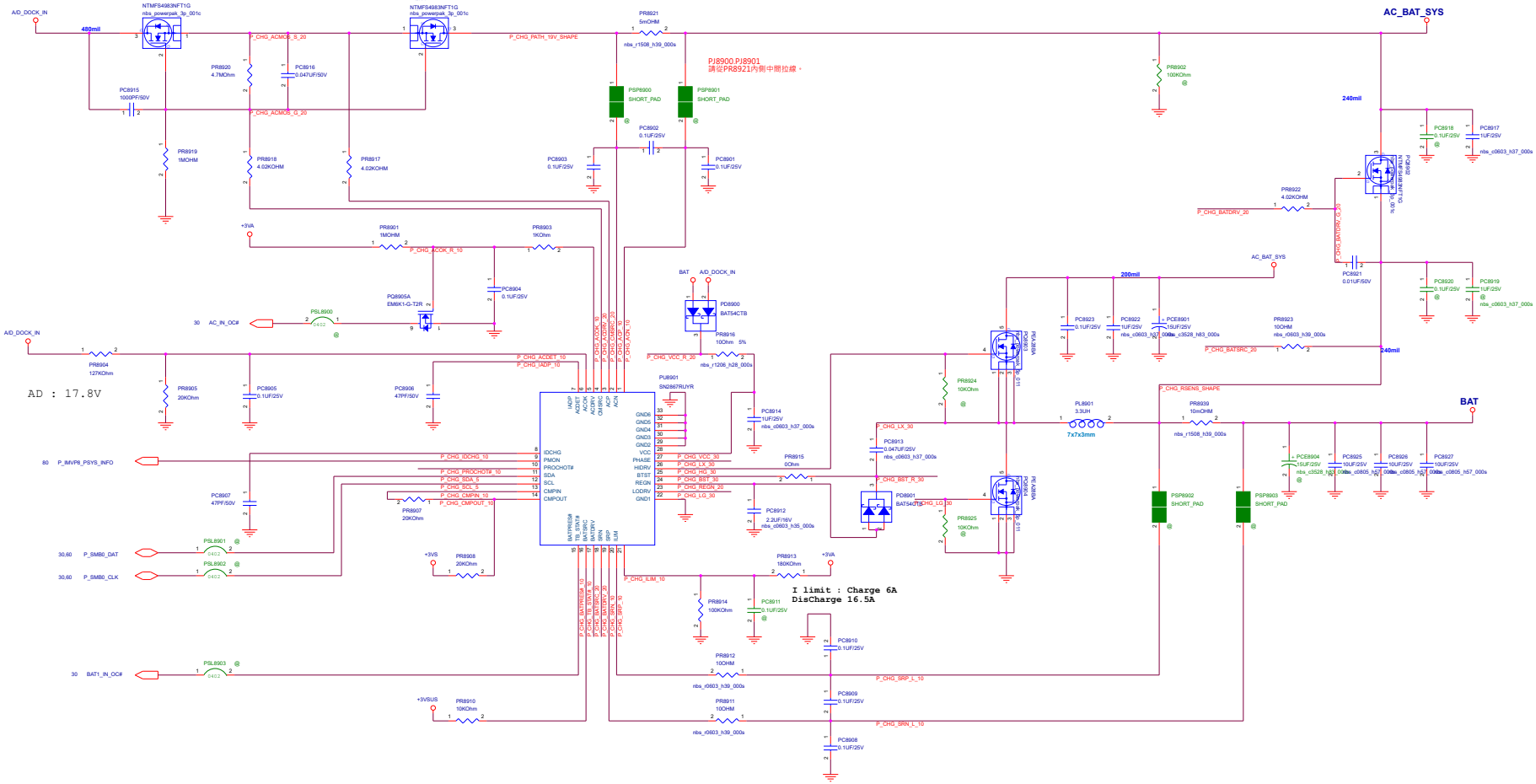
Project Name: G752VY		Rev: 2.0
Title : POWER_+VGFX_CORE		
Size: B	Dept.: NB Power team	Engineer: Benson Hsu
Date: Tuesday, July 21, 2015	Sheet 96 of 102	



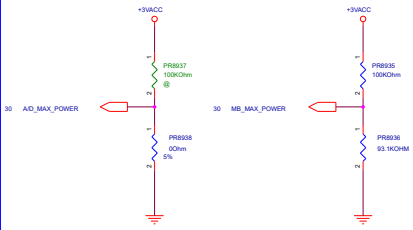
<Variant Name>

Project Name: G752VY		Rev: 2.0
Title : PW_OV		
Size: A	Dept.: NB Power team	Engineer: Benson
Date: Tuesday, July 21, 2015	Sheet 97 of 102	

	<=40W	<=120W	>=120W
PR8921	25m	10m	5m
	EPC	NB	G

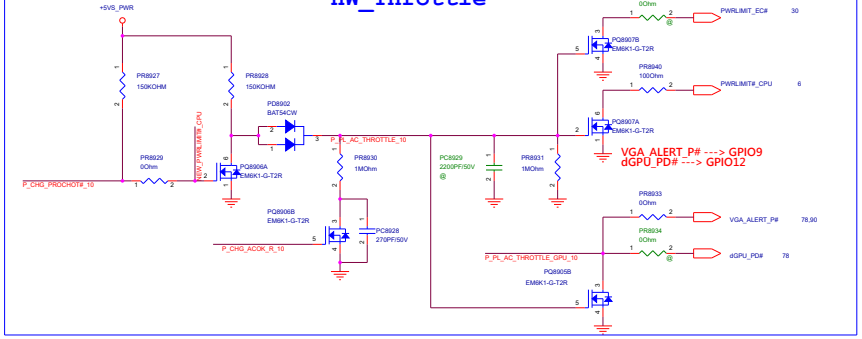


Adaptor select

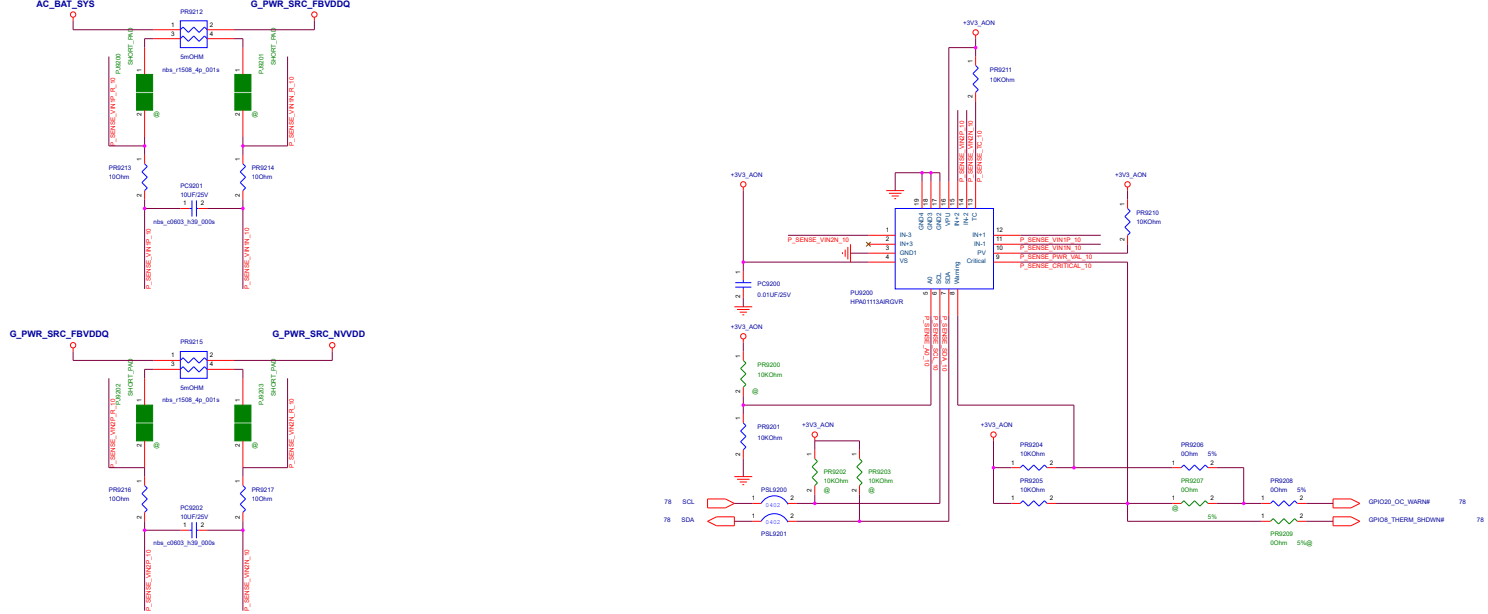


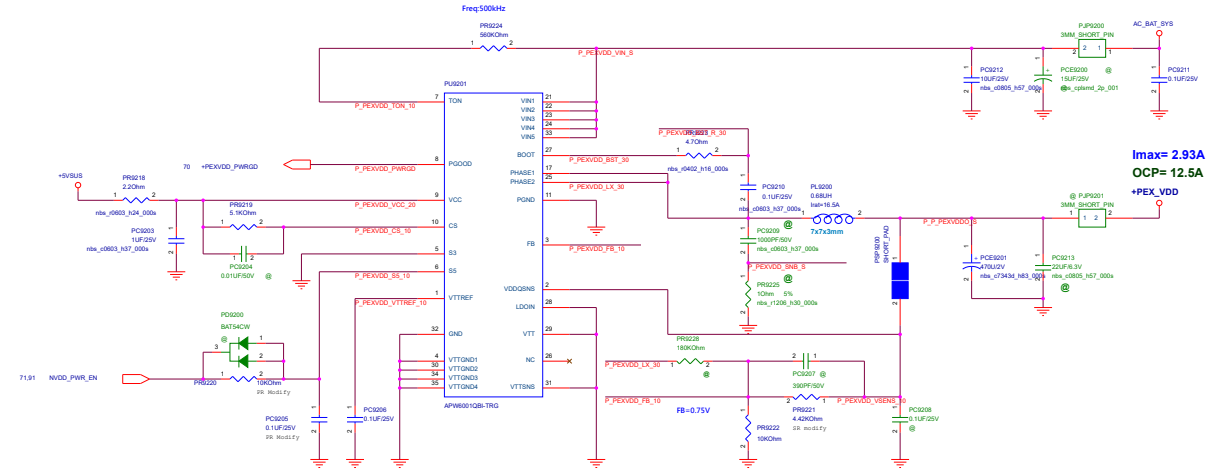
Adaptor select		N Series	G Series
PR8921		10m	5m
PR8936			
14K	0.4V	30W	120W
31.6K	0.8V	40W	150W
56K	1.2V	45W	180W
93.1K	1.6V	65W	230W
150K	2.0V	75W	300W
270K	2.4V	90W	330W
560K	2.8V	120W	400W

HW_Throttle



ASUS	Project Name: G752VY		Rev: 2.0
Title : PW_CHARGER			
Size: A2	Dept.: NB Power team	Engineer: Benson Hsu	
Date: Tuesday, July 21, 2015	Sheet: 89 of 102		





PR9221	UP1740Q_Vout
3.6kohm	1.0V
4.02kohm	1.05V
6.2kohm	1.2V
8.2kohm	1.35V
10.5kohm	1.5V

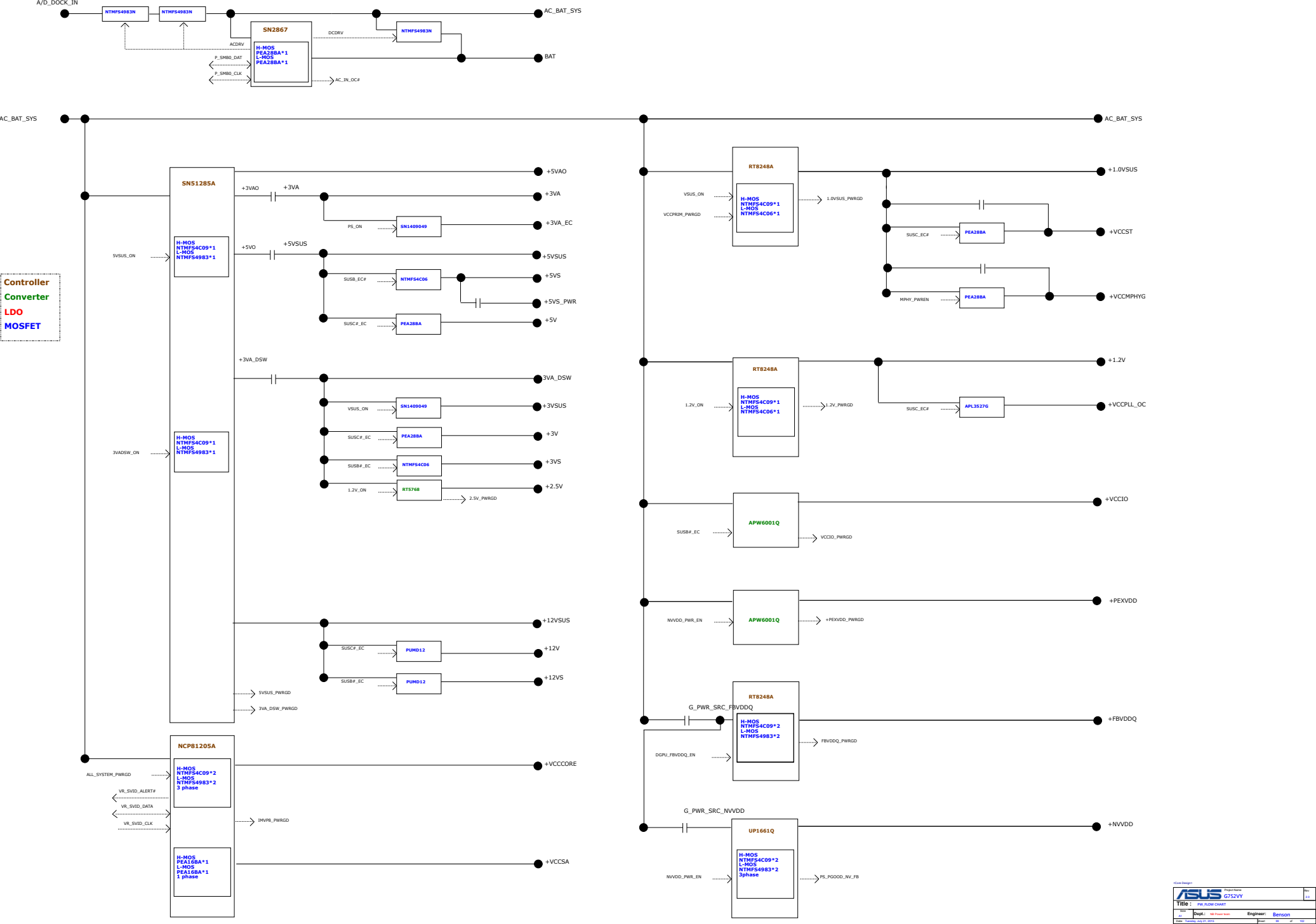
<Variant Name>

Project Name: G752VY		Rev: 2.0
Title : PW_PEX_VDD/IPC		
Size: A2	Dept.: NB Power Team	Engineer: Benson
Date: Tuesday, July 21, 2015	Sheet: 92 of 102	

Main Board

ASUS	Project Name: G752VY	Rev: 2.0
Title :	POWER_+VGFX_CORE	
Size: B	Dept.: NB Power team	Engineer: Benson Hsu
Date: Tuesday, July 21, 2015	Sheet 95 of 102	

ASUS	Project Name: G752VY	Rev: 2.0
Title :	POWER_+VGFX_CORE	
Size: Custom	Dept.: NB Power team	Engineer: Benson Hsu
Date: Tuesday, July 21, 2015	Sheet 98 of 102	

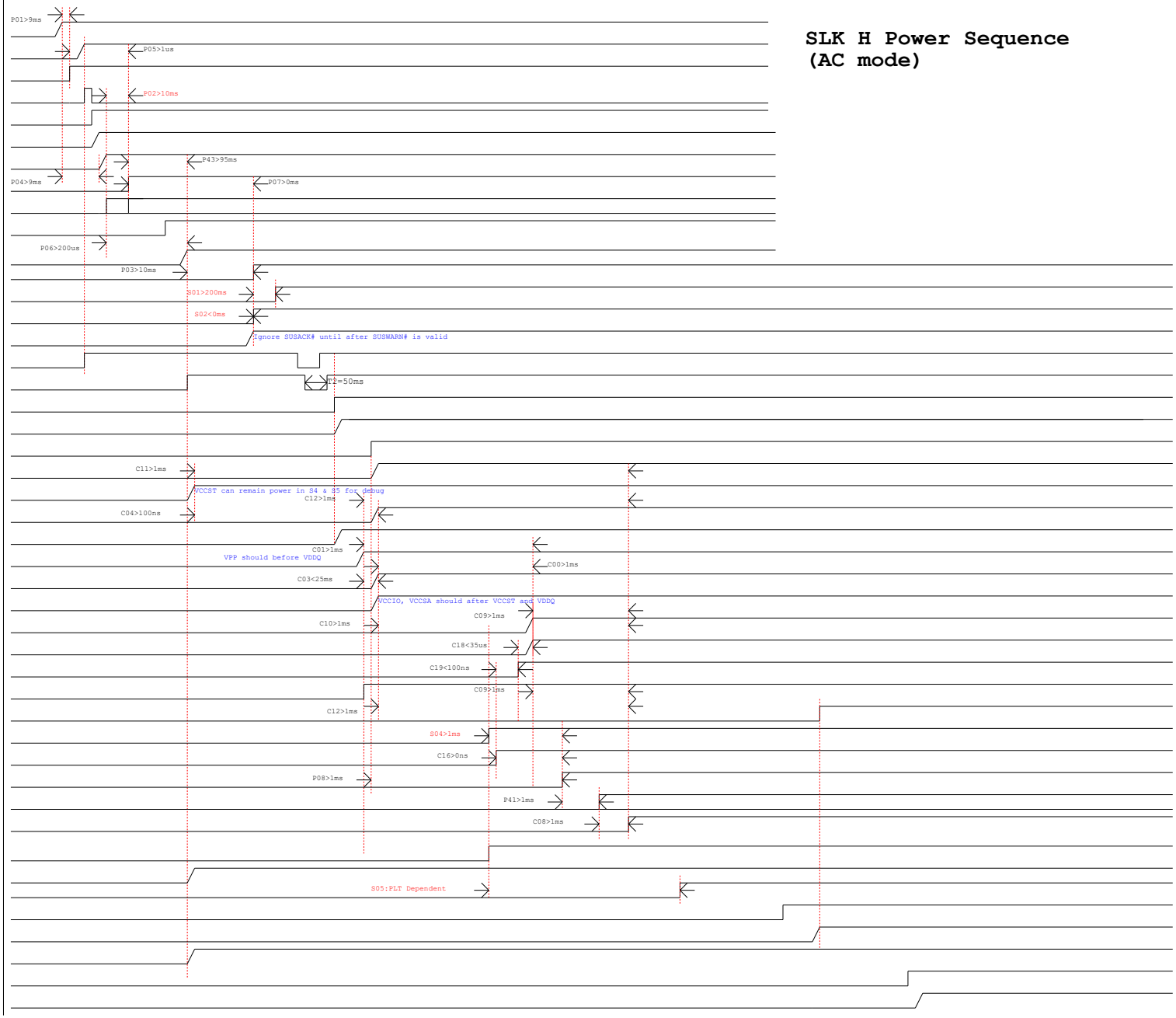

A/D_DOCK_IN
NTMFS4983N
NTMFS4983N
AC_BAT_SYS
SN2867
H-MOS
PEA28BA*1
L-MOS
PEA28BA*1
ACDRV
DCDRV
NTMFS4983N
BAT
P_SMB0_DAT
P_SMB0_CLK
AC_IN_OC#
AC_BAT_SYS
Controller
Converter
LDO
MOSFET
SN51285A
+5VAO
+3VAO
+3VA
+3VA
PS_ON
SN1409049
+3VA_EC
H-MOS
NTMFS4C09*1
L-MOS
NTMFS4983*1
5VSUS_ON
+5VO
+5VSUS
+5VSUS
SUSB_EC#
NTMFS4C06
+5VS
+5VS_PWR
SUSC#_EC
PEA28BA
+5V
+3VA_DSW
3VA_DSW
VSUS_ON
SN1409049
+3VSUS
SUSC#_EC
PEA28BA
+3V
3VADSW_ON
SUSB#_EC
NTMFS4C06
+3VS
1.2V_ON
RT5768
+2.5V
2.5V_PWRGD
+12VSUS
SUSC#_EC
PUMD12
+12V
SUSB#_EC
PUMD12
+12VS
5VSUS_PWRGD
3VA_DSW_PWRGD
NCP81205A
H-MOS
NTMFS4C09*2
L-MOS
NTMFS4983*2
3 phase
ALL_SYSTEM_PWRGD
VR_SVID_ALERT#
VR_SVID_DATA
VR_SVID_CLK
+VCCCORE
IMVP8_PWRGD
H-MOS
PEA168A*1
L-MOS
PEA168A*1
1 phase
+VCCSA
AC_BAT_SYS
RT8248A
H-MOS
NTMFS4C09*1
L-MOS
NTMFS4C06*1
VSUS_ON
VCCPRIM_PWRGD
1.0VSUS_PWRGD
+1.0VSUS
SUSC_EC#
PEA28BA
+VCCST
MPHY_PWREN
PEA28BA
+VCCMPHYG
RT8248A
H-MOS
NTMFS4C09*1
L-MOS
NTMFS4C06*1
1.2V_ON
1.2V_PWRGD
+1.2V
SUSC_EC#
APL3527G
+VCCPLL_OC
APW6001Q
SUSB#_EC
VCCIO_PWRGD
+VCCIO
APW6001Q
NVVDD_PWR_EN
+PEXVDD_PWRGD
+PEXVDD
RT8248A
H-MOS
NTMFS4C09*2
L-MOS
NTMFS4983*2
G_PWR_SRC_FBVDDQ
DGPU_FBVDDQ_EN
FBVDDQ_PWRGD
+FBVDDQ
G_PWR_SRC_NVVDD
UP1661Q
H-MOS
NTMFS4C09*2
L-MOS
NTMFS4983*2
3phase
NVVDD_PWR_EN
PS_PGOOD_NV_FB
+NVVDD
ASUS
Project Name
G752VY
Rev
2.0
Title :
PW_FLOW CHART
Size
A4
Dept.:
NB Power team
Engineer:
Benson
Date: Tuesday, July 21, 2015
Sheet
90
of
100

AC-IN Mode

SLK H Power Sequence (AC mode)

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#) +12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#) +12VS/+5VS/+3VS
(VSUS_ON) +1.0V_VCCST, VCCPLL (VCCST_PWRGD)
(+VCCIO) +VCCSTG
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
(+12VS) +VCCPLL_OC
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL) +0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT



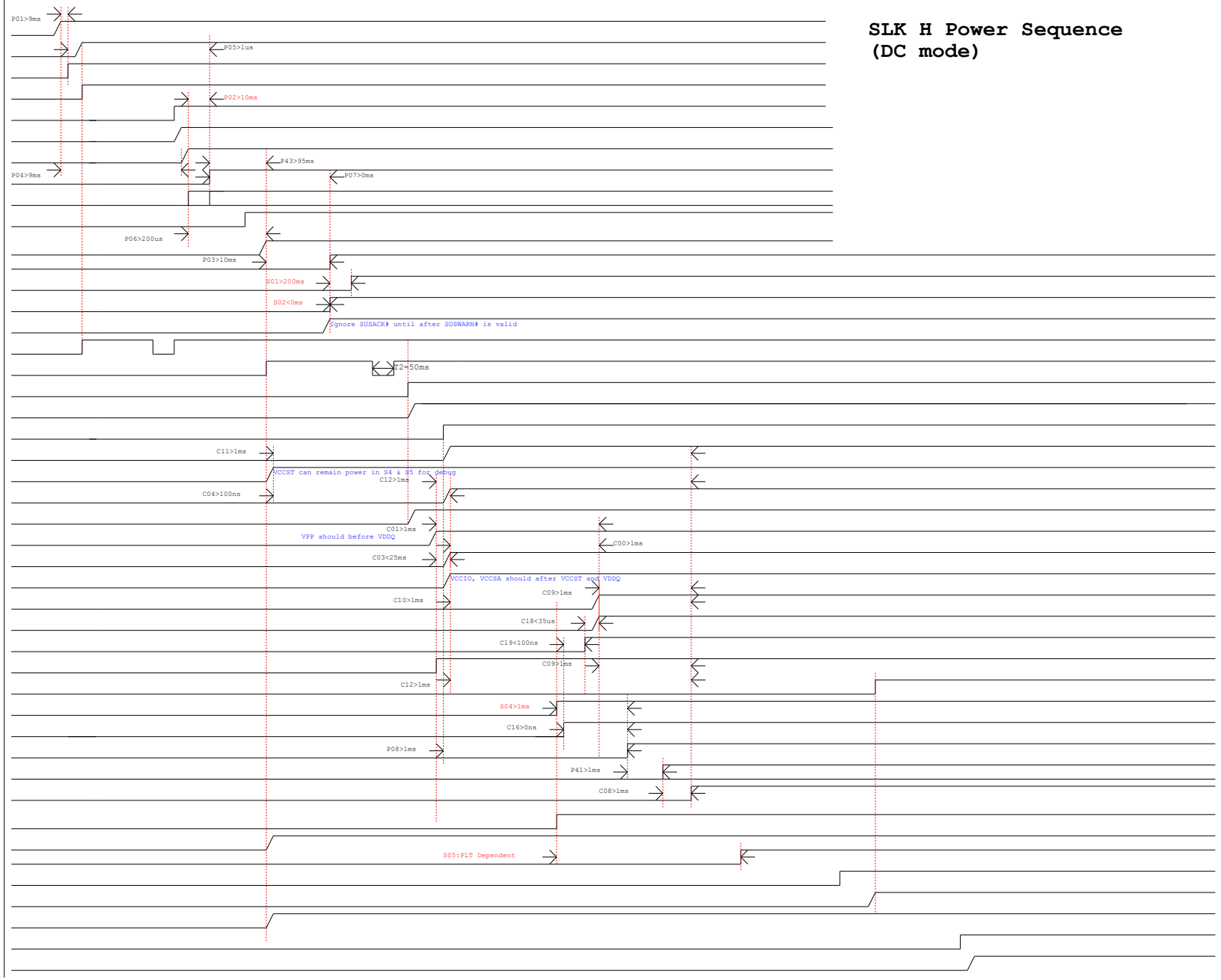
ASUS	Project Name: G752VY		Rev: 2.0
Title : AC Power On Timing			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Tuesday, July 21, 2015	Sheet 100 of 102		

SLK H Power Sequence (DC mode)

DC-IN Mode

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#) +12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#) +12VS/+5VS/+3VS
(VSUS_ON) +1.0V_VCCST,VCCPLL (VCCST_PWRGD)
(+VCCIO) +VCCSTG
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
(+12VS) +VCCPLL_OC
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL) +0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT



ASUS	Project Name: G752VY		Rev: 2.0
Title : POWER-ON SEQUENCE			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Richard Liu	
Date: Tuesday, July 21, 2015	Sheet 101 of 102		

Rev	Date	Description
R1.0	2015/03/24	Update G751VW R110_20150320