Project Name :PF4PN2F

Platform : AMD Picasso

M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

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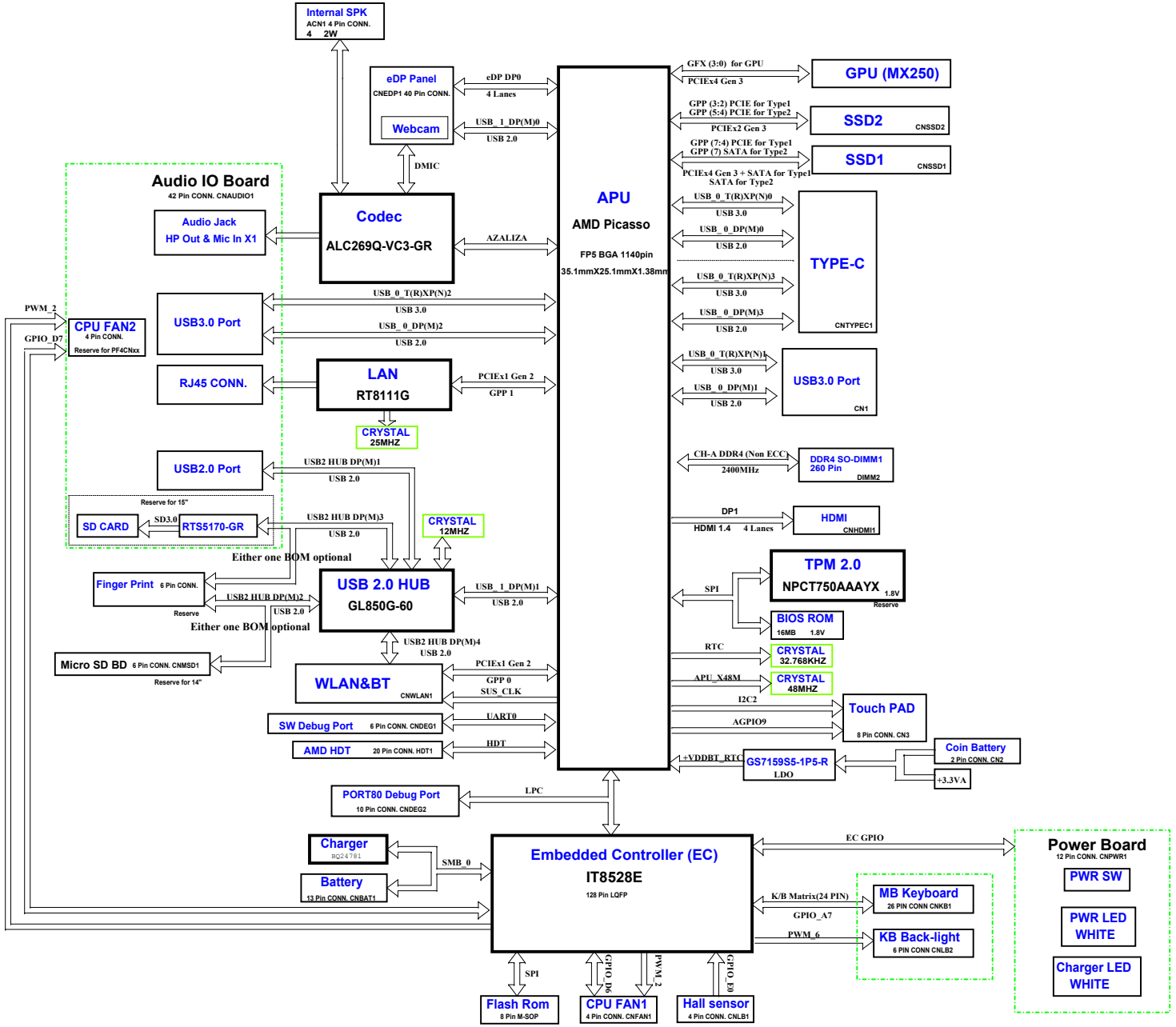
SYSTEM BLOCK DIAGRAM



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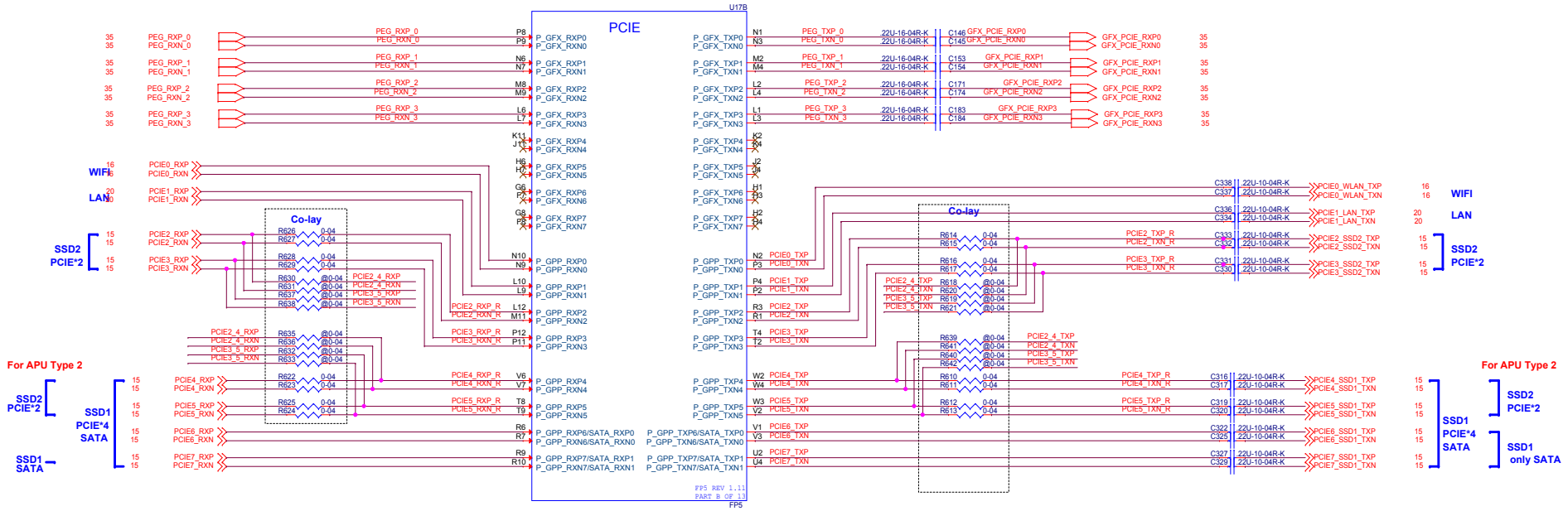

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MA_DM[0:7]
MA_MA[0:13]
MA_MD[0:63]
MA_DQS[0:7]
MA_DQS#[0:7]
U17A
MEMORY A
MA_MA0
MA_MA1
MA_MA2
MA_MA3
MA_MA4
MA_MA5
MA_MA6
MA_MA7
MA_MA8
MA_MA9
MA_MA10
MA_MA11
MA_MA12
MA_MA13
MA_WE#
MA_CAS#
MA_RAS#
MA_BA0
MA_BA1
MA_BG0
MA_BG1
MA_ACT#
MA_DM0
MA_DM1
MA_DM2
MA_DM3
MA_DM4
MA_DM5
MA_DM6
MA_DM7
MA_DQS0
MA_DQS#0
MA_DQS1
MA_DQS#1
MA_DQS2
MA_DQS#2
MA_DQS3
MA_DQS#3
MA_DQS4
MA_DQS#4
MA_DQS5
MA_DQS#5
MA_DQS6
MA_DQS#6
MA_DQS7
MA_DQS#7
MA_CLK0
MA_CLK#0
MA_CLK1
MA_CLK#1
MA_CS#0
MA_CS#1
MA_CKE0
MA_CKE1
MA_ODT0
MA_ODT1
MA_ALERT#
MA_EVENT#
MA_RESET#
MA_PAR
FP5 REV 1.11
PART A OF 13
FP5
U17I
MEMORY B
MB_CLK_H0/MBA_CKT
MB_CLK_L0/MBA_CKC
MB_CLK_H1/MBB_CKT
MB_CLK_L1/MBB_CKC
MB0_CKE0/MBA_CKE0
MB0_CKE1/MBA_CKE1
MB0_CS_L0/MBB_CS1
MB0_CS_L1/MBB_CS0
MB0_ODT0/RSVD
MB0_ODT1/RSVD
MB_ALERT_L/MB_TEST
MB_PAROUT/RSVD
MB_EVENT_L
MB_RESET_L
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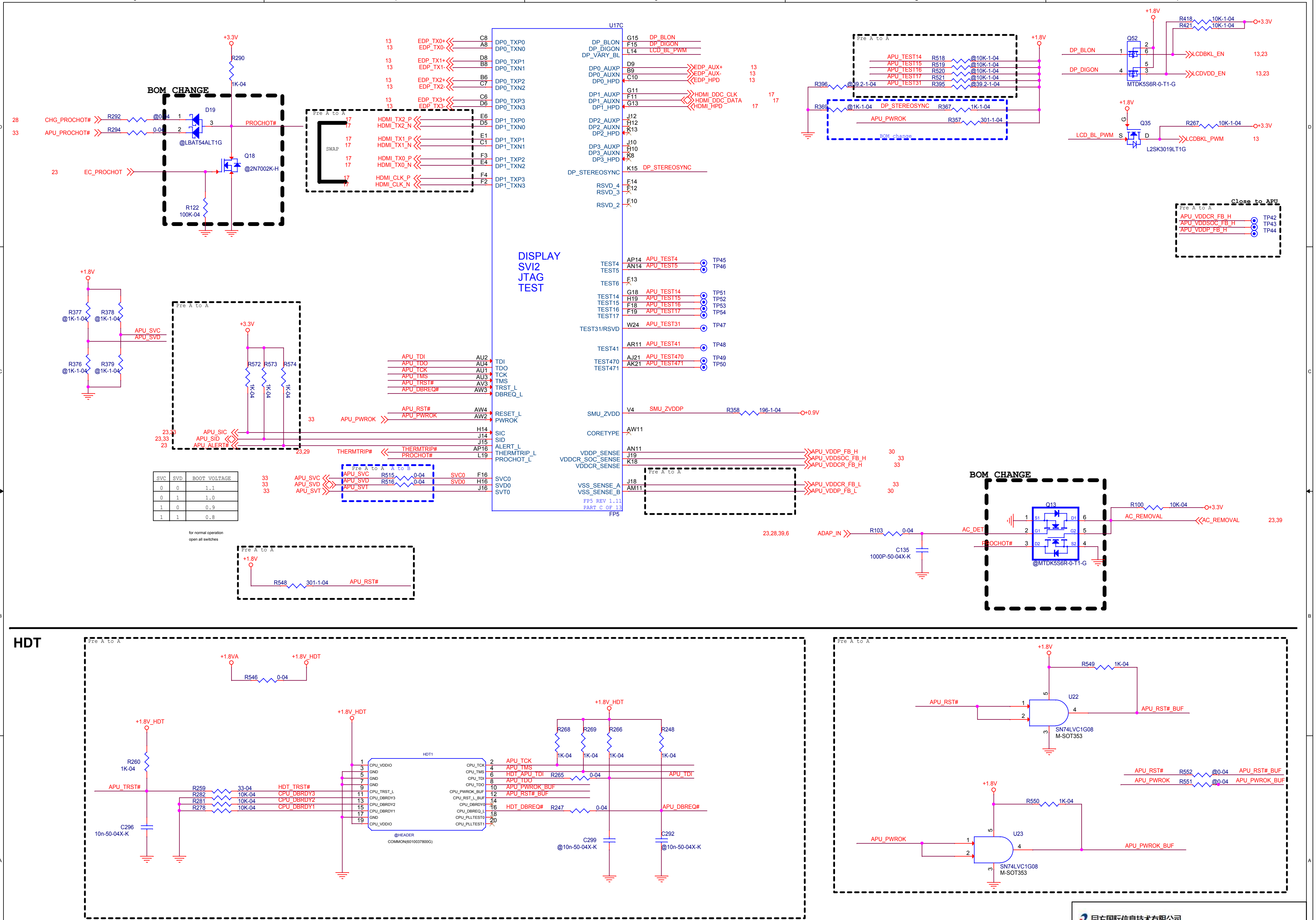

SVC	SVD	BOOT VOLTAGE
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

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Title: APU_eDP/DP/SVI2/JTAG

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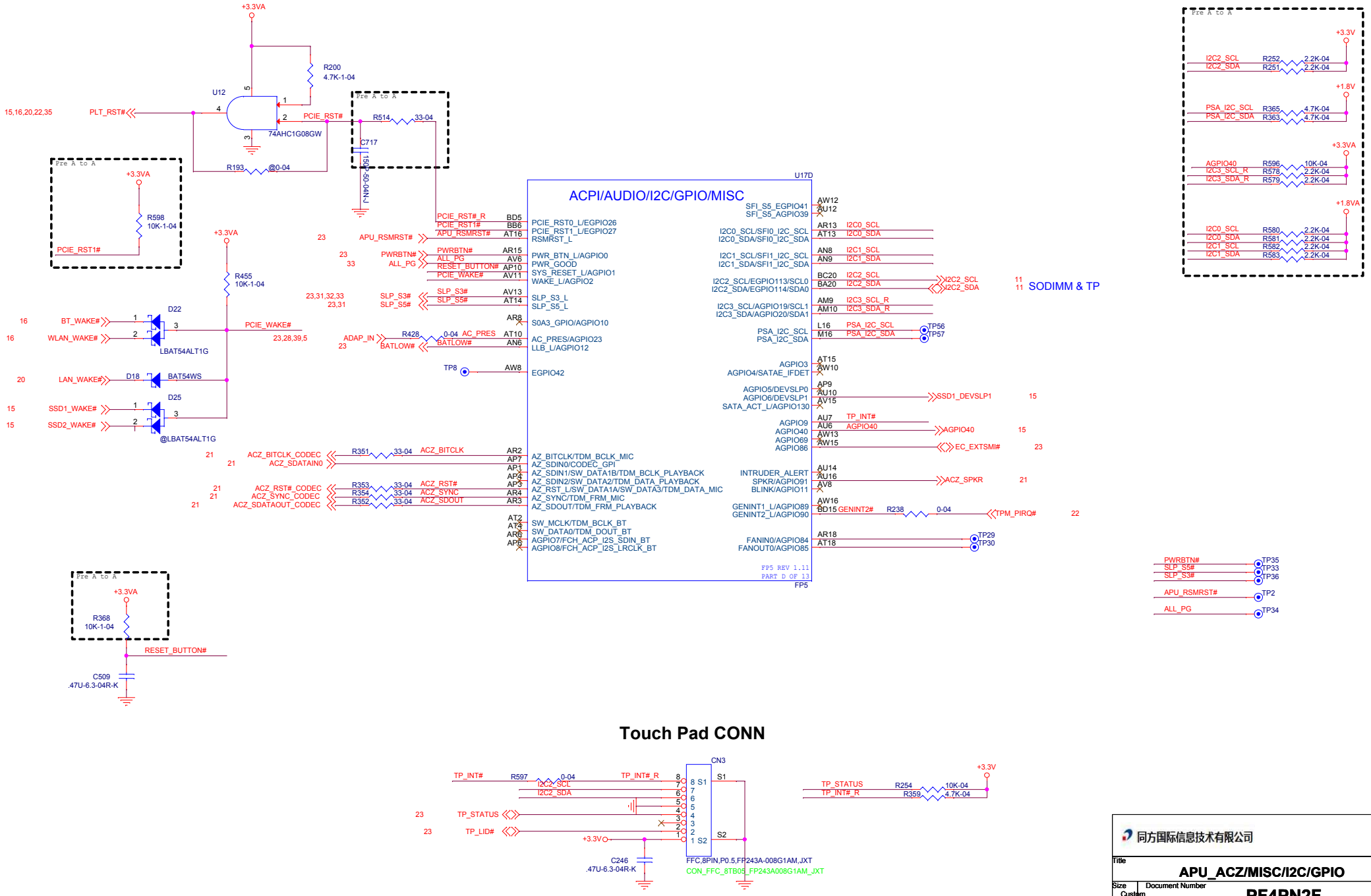

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Title	APU_ACZ/MISC/I2C/GPIO	
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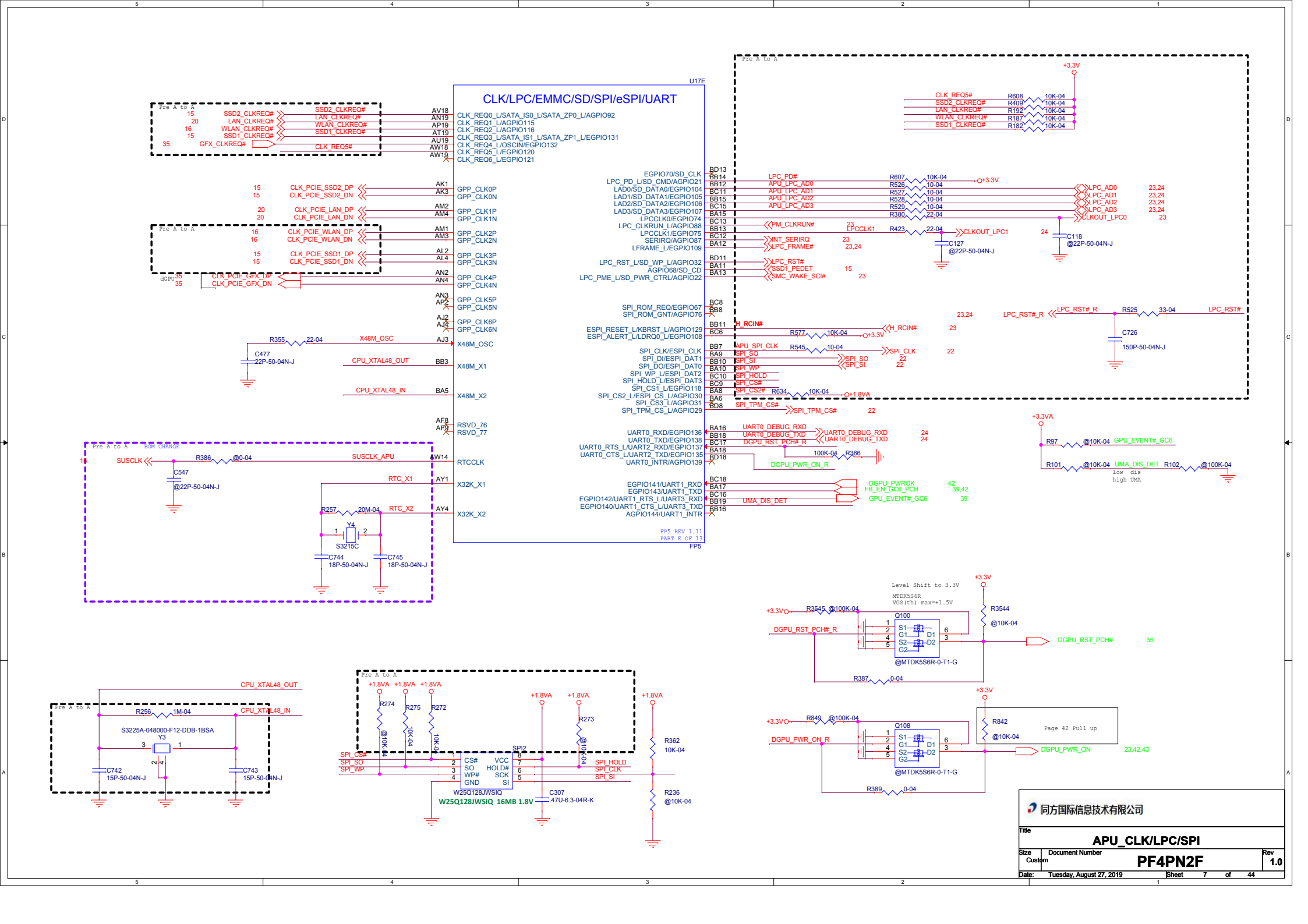
U17E
CLK/LPC/EMMC/SD/SPI/eSPI/UART
CLK_REQ0_L/SATA_IS0_L/SATA_ZP0_L/AGPIO92
CLK_REQ1_L/AGPIO115
CLK_REQ2_L/AGPIO116
CLK_REQ3_L/SATA_IS1_L/SATA_ZP1_L/EGPIO131
CLK_REQ4_L/OSCIN/EGPIO132
CLK_REQ5_L/EGPIO120
CLK_REQ6_L/EGPIO121
GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
GPP_CLK4P
GPP_CLK4N
GPP_CLK5P
GPP_CLK5N
GPP_CLK6P
GPP_CLK6N
X48M_OSC
X48M_X1
X48M_X2
RSVD_76
RSVD_77
RTCCLK
X32K_X1
X32K_X2
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FP5
SSD2_CLKREQ#
LAN_CLKREQ#
WLAN_CLKREQ#
SSD1_CLKREQ#
GFX_CLKREQ#
CLK_REQ5#
CLK_PCIE_SSD2_DP
CLK_PCIE_SSD2_DN
CLK_PCIE_LAN_DP
CLK_PCIE_LAN_DN
CLK_PCIE_WLAN_DP
CLK_PCIE_WLAN_DN
CLK_PCIE_SSD1_DP
CLK_PCIE_SSD1_DN
CLK_PCIE_GFX_DP
CLK_PCIE_GFX_DN
dGPU
SUSCLK
SUSCLK_APU
R386 @0-04
C547 @22P-50-04N-J
R355 22-04
C477 22P-50-04N-J
CPU_XTAL48_OUT
CPU_XTAL48_IN
RTC_X1
RTC_X2
R257 20M-04
Y4
S3215C
C744 18P-50-04N-J
C745 18P-50-04N-J
R256 1M-04
S3225A-048000-F12-DDB-1BSA
Y3
C742 15P-50-04N-J
C743 15P-50-04N-J
EGPIO70/SD_CLK
LPC_PD_L/SD_CMD/AGPIO21
LAD0/SD_DATA0/EGPIO104
LAD1/SD_DATA1/EGPIO105
LAD2/SD_DATA2/EGPIO106
LAD3/SD_DATA3/EGPIO107
LPCCLK0/EGPIO74
LPC_CLKRUN_L/AGPIO88
LPCCLK1/EGPIO75
SERIRQ/AGPIO87
LFRAME_L/EGPIO109
LPC_RST_L/SD_WP_L/AGPIO32
AGPIO68/SD_CD
LPC_PME_L/SD_PWR_CTRL/AGPIO22
SPI_ROM_REQ/EGPIO67
SPI_ROM_GNT/AGPIO76
ESPI_RESET_L/KBRST_L/AGPIO129
ESPI_ALERT_L/LDRQ0_L/EGPIO108
SPI_CLK/ESPI_CLK
SPI_DI/ESPI_DAT1
SPI_DO/ESPI_DAT0
SPI_WP_L/ESPI_DAT2
SPI_HOLD_L/ESPI_DAT3
SPI_CS1_L/EGPIO118
SPI_CS2_L/ESPI_CS_L/AGPIO30
SPI_CS3_L/AGPIO31
SPI_TPM_CS_L/AGPIO29
UART0_RXD/EGPIO136
UART0_TXD/EGPIO138
UART0_RTS_L/UART2_RXD/EGPIO137
UART0_CTS_L/UART2_TXD/EGPIO135
UART0_INTR/AGPIO139
EGPIO141/UART1_RXD
EGPIO143/UART1_TXD
EGPIO142/UART1_RTS_L/UART3_RXD
EGPIO140/UART1_CTS_L/UART3_TXD
AGPIO144/UART1_INTR
LPC_PD#
APU_LPC_AD0
APU_LPC_AD1
APU_LPC_AD2
APU_LPC_AD3
PM_CLKRUN#
INT_SERIRQ
LPC_FRAME#
LPC_RST#
SSD1_PEDET
SMC_WAKE_SCI#
H_RCIN#
APU_SPI_CLK
SPI_SO
SPI_SI
SPI_WP
SPI_HOLD
SPI_CS#
SPI_CS2#
SPI_TPM_CS#
UART0_DEBUG_RXD
UART0_DEBUG_TXD
DGPU_RST_PCH#_R
DGPU_PWR_ON_R
UMA_DIS_DET
DGPU_PWROK
FB_EN_GC6_PCH
GPU_EVENT#_GC6
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
CLKOUT_LPC0
CLKOUT_LPC1
LPC_RST#_R
C118 @22P-50-04N-J
C127 @22P-50-04N-J
C726 150P-50-04N-J
R607 10K-04
R526 10-04
R527 10-04
R528 10-04
R529 10-04
R380 22-04
R423 22-04
R577 10K-04
R545 10-04
R634 10K-04
R366 100K-04
R608 10K-04
R409 10K-04
R192 10K-04
R187 10K-04
R182 10K-04
R525 33-04
R97 @10K-04
R101 @10K-04
R102 @100K-04
+3.3V
+3.3VA
+1.8VA
Pre A to A
BOM CHANGE
Level Shift to 3.3V
MTDK5S6R
VGS(th) max=+1.5V
Q100
Q108
@MTDK5S6R-0-T1-G
R3545 @100K-04
R3544 @10K-04
R387 0-04
R849 @100K-04
R842 @10K-04
R389 0-04
DGPU_RST_PCH#
DGPU_PWR_ON
Page 42 Pull up
SPI2
W25Q128JWSIQ
W25Q128JWSIQ 16MB 1.8V
R274
R275
R272
R273
C307 .47U-6.3-04R-K
R362 10K-04
R236 @10K-04
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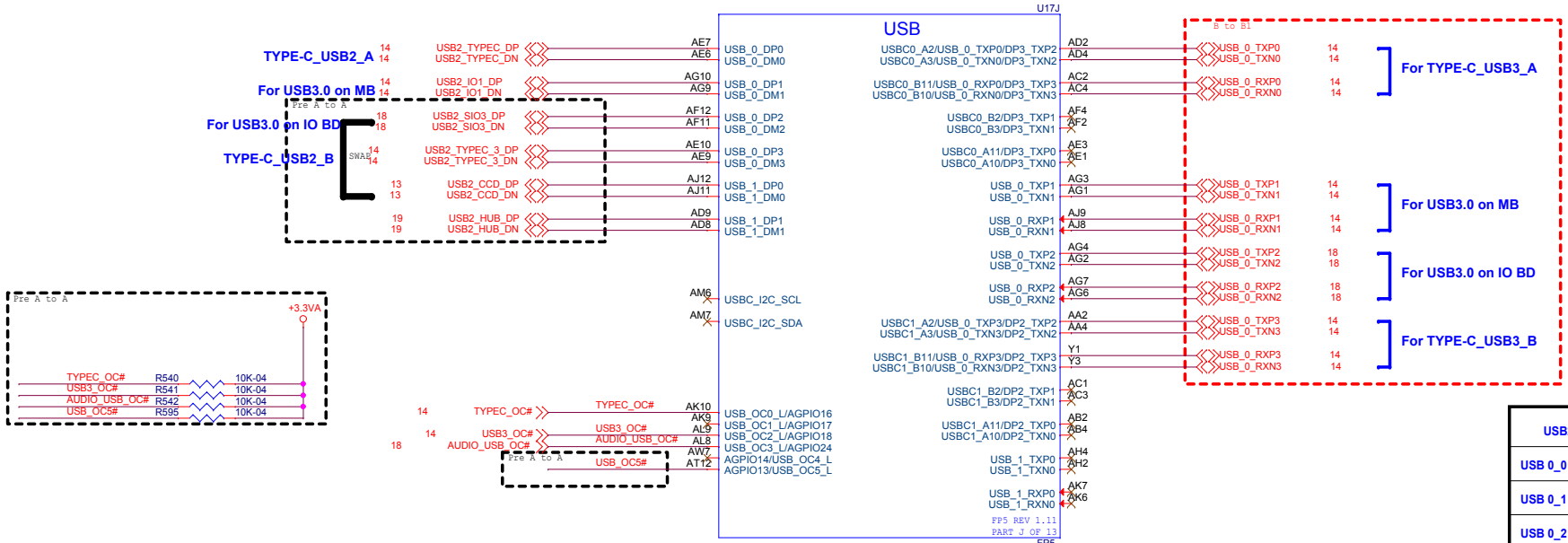
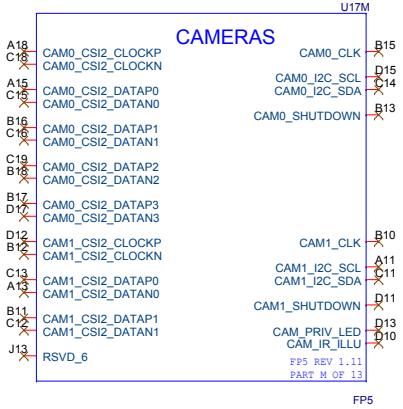
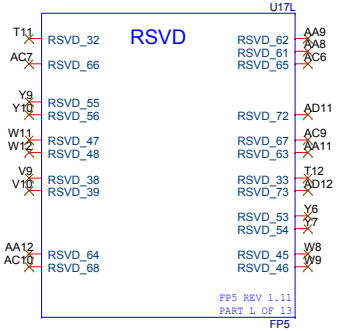


USB2.0 Configuration Table		
USB 0_0	TYPE-C Port	
USB 0_1	USB3.0 Port	
USB 0_2	USB3.0 Port on IO DB	
USB 0_3	TYPE-C Port	
USB 1_0	Web Camera	
USB 1_1	USB 2.0 HUB	
HUB 0	USB 1_1	
HUB 1	USB2.0 PORT on IO DB	
HUB 2	14" CardReader / Finger Printer	Switch by resistor
HUB 3	15" CardReader / Finger Printer	Switch by resistor
HUB 4	Bluetooth	





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Title: APU_USB2/USB3/CAM

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VDDCR

Under the APU

22uF*16 180PF*1 change to 22uF*12 180PF*1

+APU_VDDCORE

C503 C517 C520 C341 C510 C539 C490 C522 C511 C483 C518 C548 C365 C498 C540 C538 C505 C562 C525 C414 C514 C552 C491 C526 C519 C484 C535 C556 C413 C499 C553 C554 C500 C563 C564 C569 C521

10U-6.3-04R / @10U-6.3-04R / C_180P_50_04N_J

VDDIO_MEM_S3

Under the APU

22uF*9 1uF*2 180PF*1 change to 22uF*5 2.2uF*1 180PF*1

+1.2VS_DDR

C620 C607 C608 C603 C622 C621 C587 C623 C609 C624 C615 C626 C627 C629 C631 C588 C628 C630 C632 C633 C586 C573 C610

10U-6.3-04R / @10U-6.3-04R / 2.2U-6.3-04R / @1U-10-04R-K / C_180P_50_04N_J

VDDCR_SOC

Under the APU

+APU_VDDSOC

22uF*7 1uF*1 180PF*1 change to 22uF*5 0.47uF*1 180PF*1

+1.2VS_DDR Split 0.22uF*4 180PF*2 change to 0.47uF*1 0.22uF*1 330PF*1

C366 C374 C377 C373 C367 C368 C369 C420 C421 C431 C438 C417 C418 C419 C442 C570 C530 C572

C574 C618 C617 C592 C616 C619

10U-6.3-04R / @10U-6.3-04R / 0.47U-6.3-04R-K / @2.2U-10-04R-K / C_180P_50_04N_J

VDDP

Under the APU

1uF*4 180PF*1 change to 2.2uF*1 180PF*1

+0.9V

C502 C488 C497 C482 C469

2.2U-6.3-04R / @1U-10-04R-K / C_180P_50_04N_J

Bottom, Outside of the APU

22uF*2 1uF*4 change to 22uF*1 10uF*1 2.2uF*1

+0.9V

C496 C523 C575 C576 C504 C513 C473 C487

10U-6.3-04R / 2.2U-6.3-04R / @1U-10-04R-K / @1U-10-04R-K

VDDP_S5

Under the APU 1uF*2 change to 2.2uF*1

Bottom, Outside of the APU

+0.9VA

C527 C528 C524 C529

2.2U-6.3-04R / @1U-10-04R-K / 10U-6.3-04R / 47U-6.3-04R-K

VDDIO_AUDIO

+1.8VA

Under the APU 1uF*1 change to 0.47uF*1

Bottom, Outside of the APU 22uF*1 change to 10uF*1

10uF*1 0.47uF*1

C531 47U-6.3-04R-K

C532 10U-6.3-04R

+3.3V VDD_33_1 VDD_33_2

+1.8V VDD_18_1 VDD_18_2

+1.8VA VDD_18_S5_1 VDD_18_S5_2

VDD_33_S5

+3.3VA

Under the APU 1uF*1 change to 0.47uF*1

Bottom, Outside of the APU 22uF*1 1uF*1 change to 10uF*1 0.47uF*1

C544 47U-6.3-04R-K

C541 10U-6.3-04R

C545 47U-6.3-04R-K

VDD_33_S5_1 VDD_33_S5_2

+0.9VA VDDP_S5_1 VDDP_S5_2 VDDP_S5_3

+0.9V VDDP_1 VDDP_2 VDDP_3 VDDP_4 VDDP_5

Under the APU +VDDBT_RTC

C506 22U-10-04R-K

C512 @1U-10-04R-K

22uF*1 1uF*1 change to 2.2uF*1

VDDBT_RTC_G

VDD_18

Under the APU 1uF*1 change to 0.47uF*1

+1.8V

C579 47U-6.3-04R-K

Bottom, Outside of the APU 22uF*1 1uF*1 change to 10uF*1 0.47uF*1

+1.8V

C582 10U-6.3-04R

C571 47U-6.3-04R-K

VDD_18_S5

Under the APU 1uF*1 change to 0.47uF*1

+1.8VA

C416 47U-6.3-04R-K

Bottom, Outside of the APU 22uF*1 1uF*1 change to 10uF*1 0.47uF*1

+1.8VA

C286 10U-6.3-04R

C423 47U-6.3-04R-K

VDD_33

Under the APU 1uF*1 change to 0.47uF*1

+3.3V

C543 47U-6.3-04R-K

Bottom, Outside of the APU 22uF*1 1uF*1 change to

+3.3V

C546 10U-6.3-04R

C542 47U-6.3-04R-K

VDDBT_RTC_G

Pin A to A

+3.3VA

R119 0-04

D10 LBAT54CLT1G

CN2 WB,2P,SMT,P1.25,W-00-1025-0200,JCTC

R40 1K-04

+3.3VA_RTC

R364 1.5K-1-04

C494 47U-6.3-04R-K

U21 GS7159S5-1P5-R

VIN VOUT GND NC EN

31 to 1_0 Pin A to A

+VDDBT_RTC

TP_RTC

23 EC_RTC_RST

Q32 2N7002K-H

BOM change A to B

POWER

U17F

M15	VDDCR_SOC_1	VDDCR_1	G7
M18	VDDCR_SOC_2	VDDCR_2	G10
M19	VDDCR_SOC_3	VDDCR_3	G12
N16	VDDCR_SOC_4	VDDCR_4	G14
N18	VDDCR_SOC_5	VDDCR_5	H8
N20	VDDCR_SOC_6	VDDCR_6	H11
P17	VDDCR_SOC_7	VDDCR_7	H15
P19	VDDCR_SOC_8	VDDCR_8	K7
R18	VDDCR_SOC_9	VDDCR_9	K12
R20	VDDCR_SOC_10	VDDCR_10	K14
T19	VDDCR_SOC_11	VDDCR_11	L8
U18	VDDCR_SOC_12	VDDCR_12	M7
U20	VDDCR_SOC_13	VDDCR_13	M10
V19	VDDCR_SOC_14	VDDCR_14	N14
W18	VDDCR_SOC_15	VDDCR_15	P7
W20	VDDCR_SOC_16	VDDCR_16	P10
Y19	VDDCR_SOC_17	VDDCR_17	P13
		VDDCR_18	P15
		VDDCR_19	R8
T32	VDDIO_MEM_S3_1	VDDCR_20	R14
V28	VDDIO_MEM_S3_2	VDDCR_21	R16
W28	VDDIO_MEM_S3_3	VDDCR_22	T7
W32	VDDIO_MEM_S3_4	VDDCR_23	T10
Y32	VDDIO_MEM_S3_5	VDDCR_24	T13
Y25	VDDIO_MEM_S3_6	VDDCR_25	T15
Y28	VDDIO_MEM_S3_7	VDDCR_26	T17
AA20	VDDIO_MEM_S3_8	VDDCR_27	U14
AA23	VDDIO_MEM_S3_9	VDDCR_28	U16
AA26	VDDIO_MEM_S3_10	VDDCR_29	V13
AA28	VDDIO_MEM_S3_11	VDDCR_30	V15
AA32	VDDIO_MEM_S3_12	VDDCR_31	V17
AC20	VDDIO_MEM_S3_13	VDDCR_32	W7
AC22	VDDIO_MEM_S3_14	VDDCR_33	W10
AC25	VDDIO_MEM_S3_15	VDDCR_34	W14
AC28	VDDIO_MEM_S3_16	VDDCR_35	W16
AD23	VDDIO_MEM_S3_17	VDDCR_36	Y8
AD26	VDDIO_MEM_S3_18	VDDCR_37	Y13
AD28	VDDIO_MEM_S3_19	VDDCR_38	Y15
AD32	VDDIO_MEM_S3_20	VDDCR_39	Y17
AE20	VDDIO_MEM_S3_21	VDDCR_40	AA7
AE22	VDDIO_MEM_S3_22	VDDCR_41	AA10
AE25	VDDIO_MEM_S3_23	VDDCR_42	AA14
AE28	VDDIO_MEM_S3_24	VDDCR_43	AA16
AF23	VDDIO_MEM_S3_25	VDDCR_44	AA18
AF26	VDDIO_MEM_S3_26	VDDCR_45	AB13
AF28	VDDIO_MEM_S3_27	VDDCR_46	AB15
AF32	VDDIO_MEM_S3_28	VDDCR_47	AB17
AG20	VDDIO_MEM_S3_29	VDDCR_48	AB19
AG22	VDDIO_MEM_S3_30	VDDCR_49	AC14
AG25	VDDIO_MEM_S3_31	VDDCR_50	AC16
AG28	VDDIO_MEM_S3_32	VDDCR_51	AC18
AJ20	VDDIO_MEM_S3_33	VDDCR_52	AD7
AJ23	VDDIO_MEM_S3_34	VDDCR_53	AD10
AJ26	VDDIO_MEM_S3_35	VDDCR_54	AD13
AJ28	VDDIO_MEM_S3_36	VDDCR_55	AD15
AJ32	VDDIO_MEM_S3_37	VDDCR_56	AD17
AK28	VDDIO_MEM_S3_38	VDDCR_57	AD19
AL28	VDDIO_MEM_S3_39	VDDCR_58	AE8
AL32	VDDIO_MEM_S3_40	VDDCR_59	AE14
AP12	VDDIO_AUDIO	VDDCR_60	AE16
		VDDCR_61	AE18
AL18	VDD_33_1	VDDCR_62	AF7
AM17	VDD_33_2	VDDCR_63	AF10
AL20	VDD_18_1	VDDCR_64	AF13
AM19	VDD_18_2	VDDCR_65	AF15
AL19	VDD_18_S5_1	VDDCR_66	AF17
AM18	VDD_18_S5_2	VDDCR_67	AF19
AL17	VDD_33_S5_1	VDDCR_68	AG14
AM16	VDD_33_S5_2	VDDCR_69	AG16
AL14	VDDP_S5_1	VDDCR_70	AG18
AL15	VDDP_S5_2	VDDCR_71	AH13
AM14	VDDP_S5_3	VDDCR_72	AH15
AL13	VDDP_1	VDDCR_73	AH17
AM12	VDDP_2	VDDCR_74	AH19
AM13	VDDP_3	VDDCR_75	AJ7
AN12	VDDP_4	VDDCR_76	AJ10
AN13	VDDP_5	VDDCR_77	AJ14
		VDDCR_78	AJ16
AT11	VDDBT_RTC_G	VDDCR_79	AJ18
		VDDCR_80	AK13
		VDDCR_81	AK15
		VDDCR_82	AK17
		VDDCR_83	AK19

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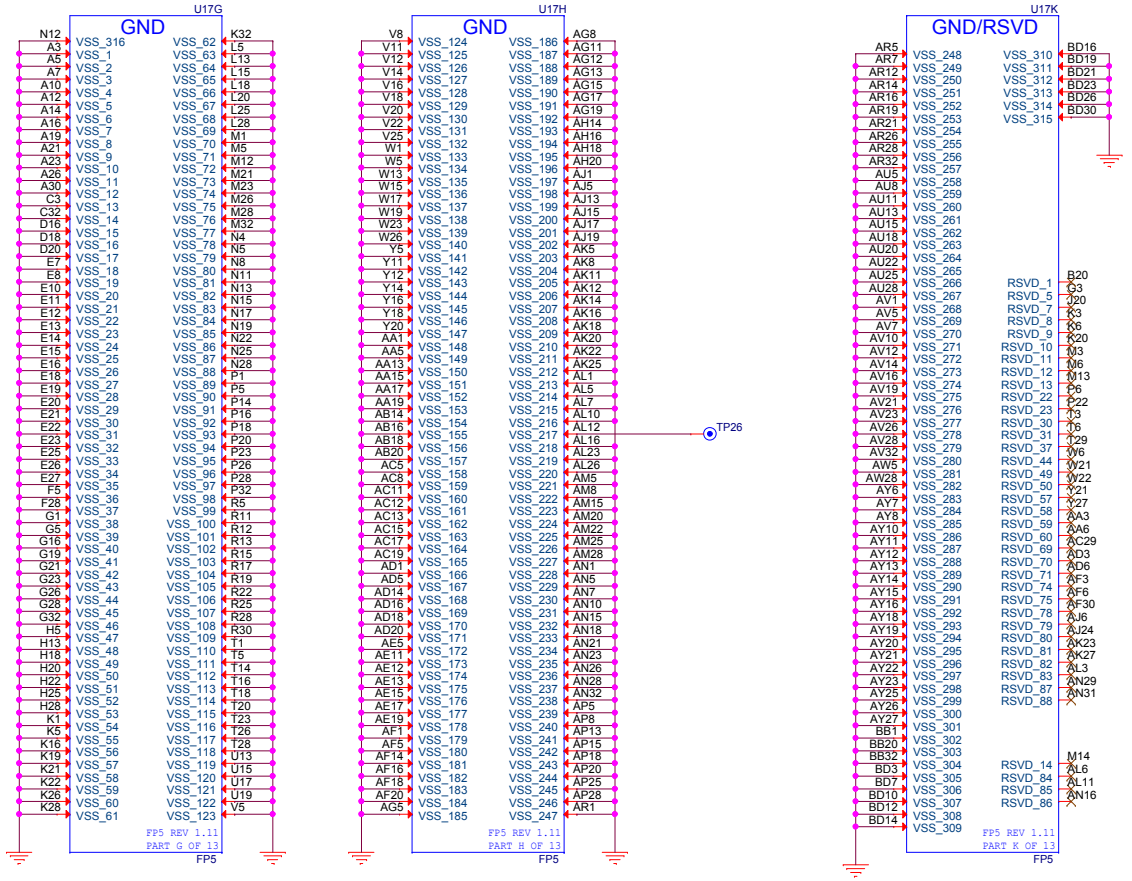
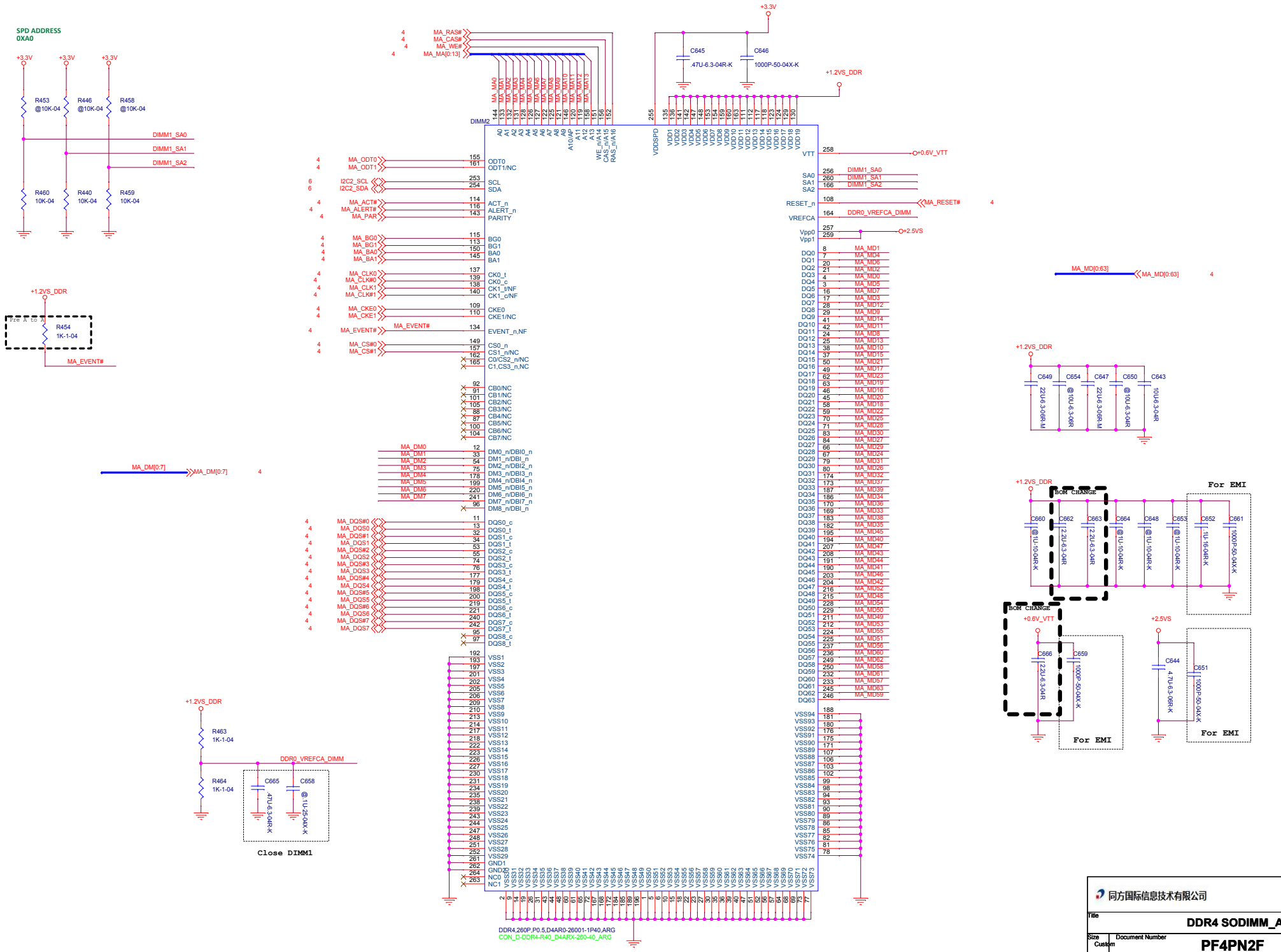


同方国际信息技术有限公司

Title	APU_GND	
Size: Custom	Document Number: PF4PN2F	Rev: 1.0
Date: Tuesday, August 27, 2019	Sheet 10 of 44	



同方国际信息技术有限公司

Title	DDR4 SODIMM_A	
Size: Custom	Document Number: PF4PN2F	Rev: 1.0
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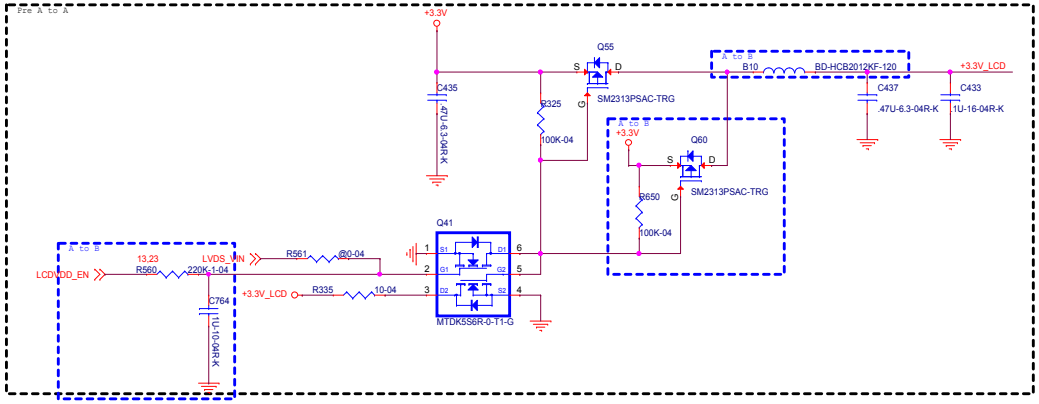
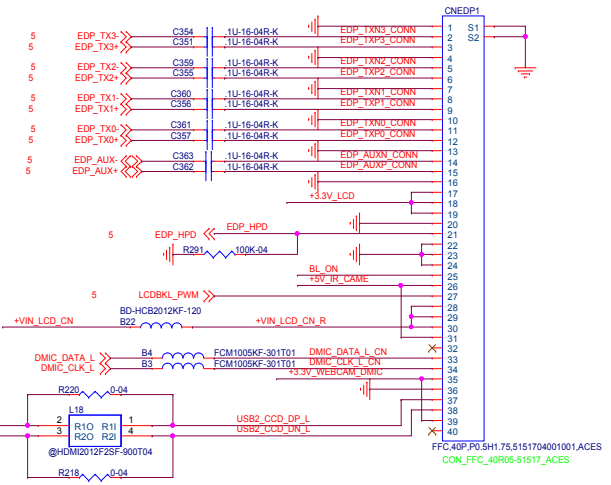
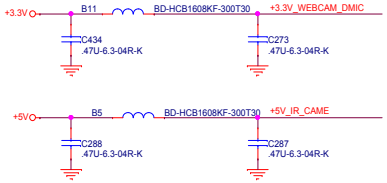
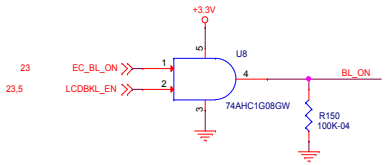
同方国际信息技术有限公司

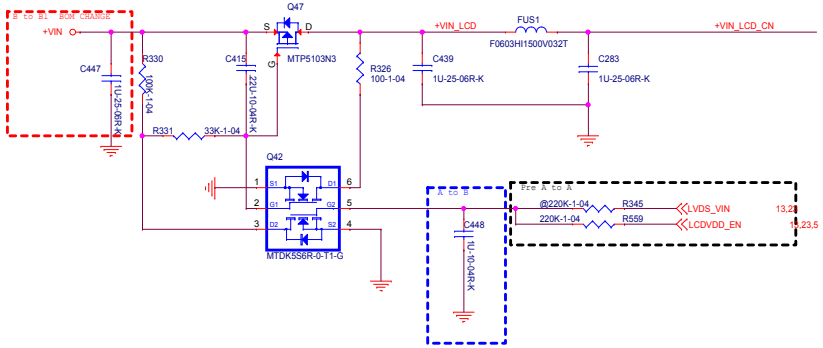
Title	RESERVED	
Size: Custom	Document Number: PF4PN2F	Rev: 1.0
Date: Tuesday, August 27, 2019	Sheet 12 of 44	

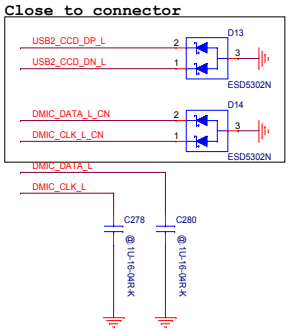








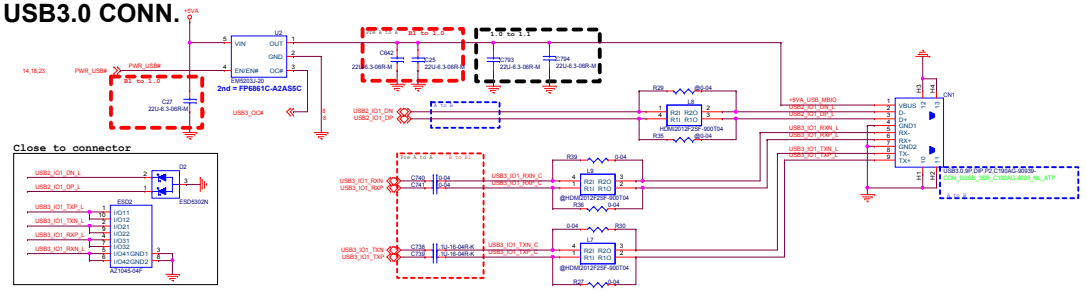




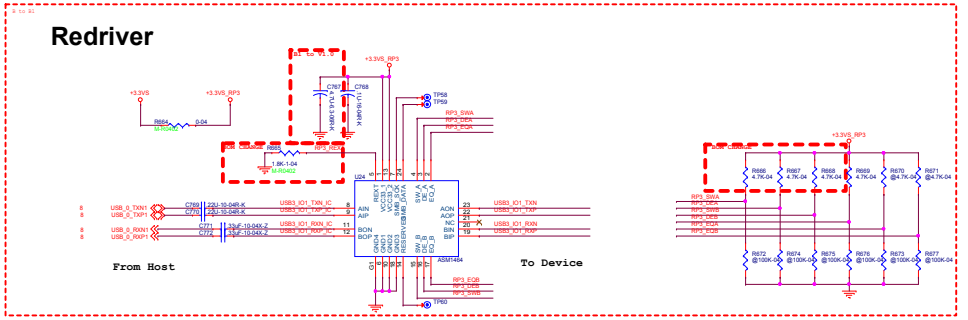
同方国际信息技术有限公司

Title	eDP Pannel/CAMERA		
Size C	Document Number PF4PN2F		Rev 1.0
Date: Tuesday, August 27, 2019		Sheet 13 of 44	

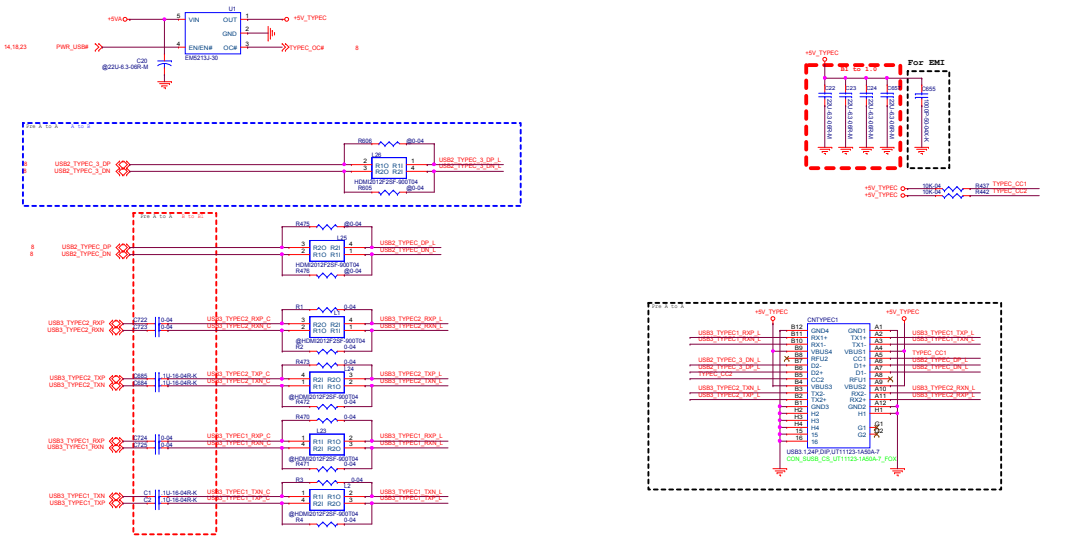
USB3.0 CONN.



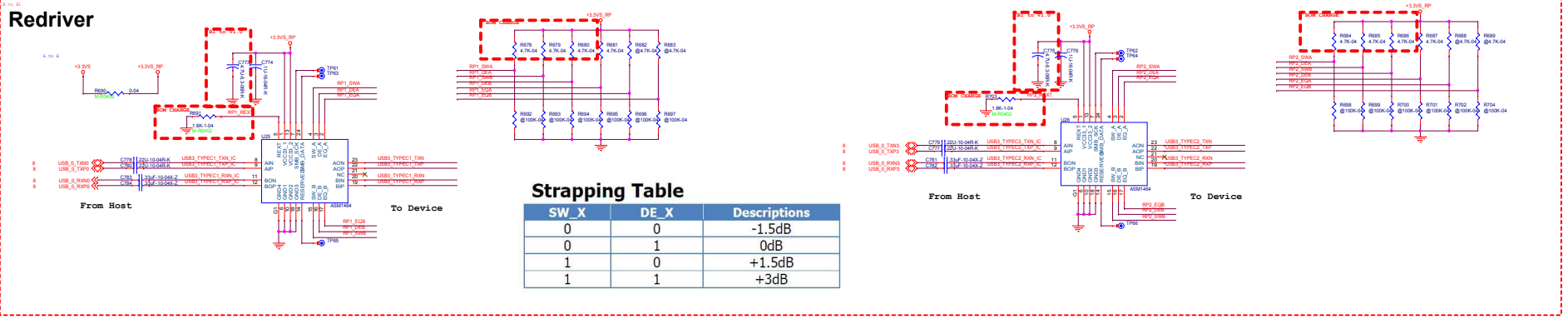
Redriver



USB3.0 TYPE-C



Redriver



Strapping Table

SW_X	DE_X	Descriptions
0	0	-1.5dB
0	1	0dB
1	0	+1.5dB
1	1	+3dB

同方国际信息技术有限公司

File	USB3.1/TYPE-C	
Size: D	Document Number: PF4PN2F	Rev: 1.0
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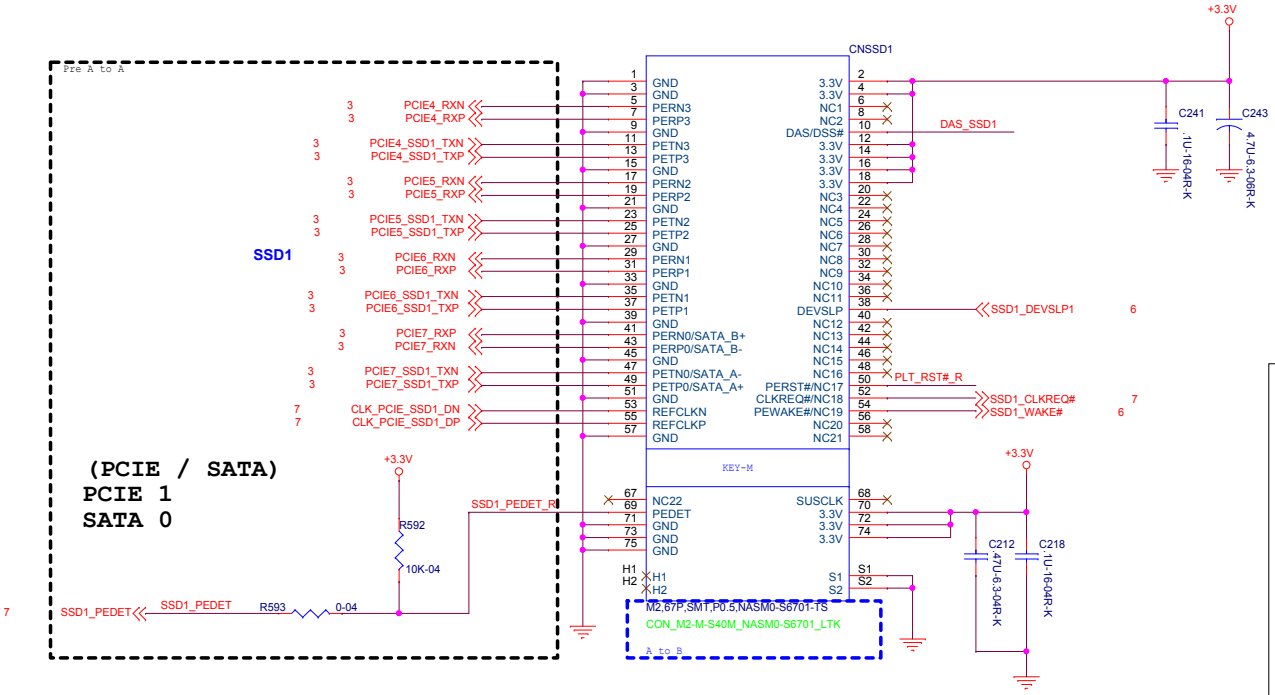
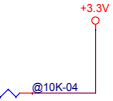
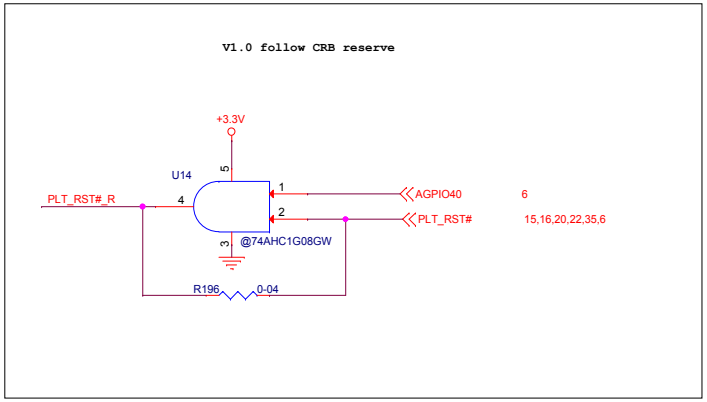
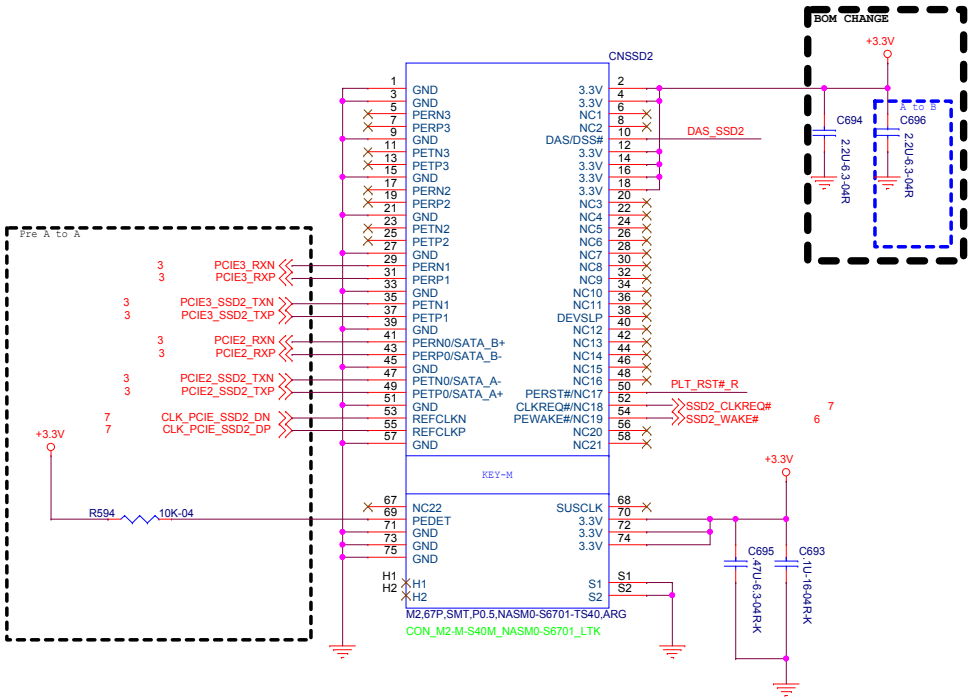
SSD1

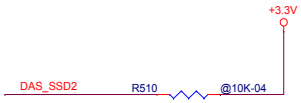






SSD2



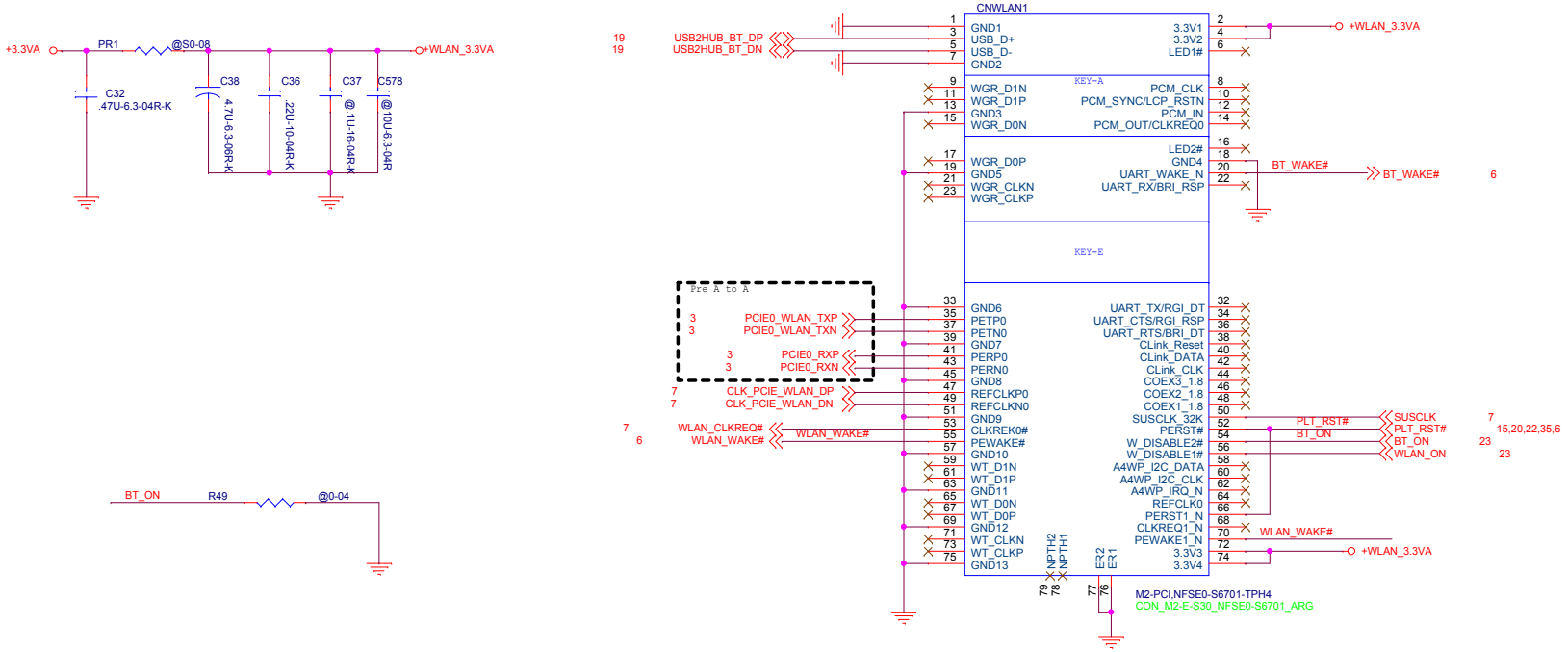


(only PCIE)

同方国际信息技术有限公司

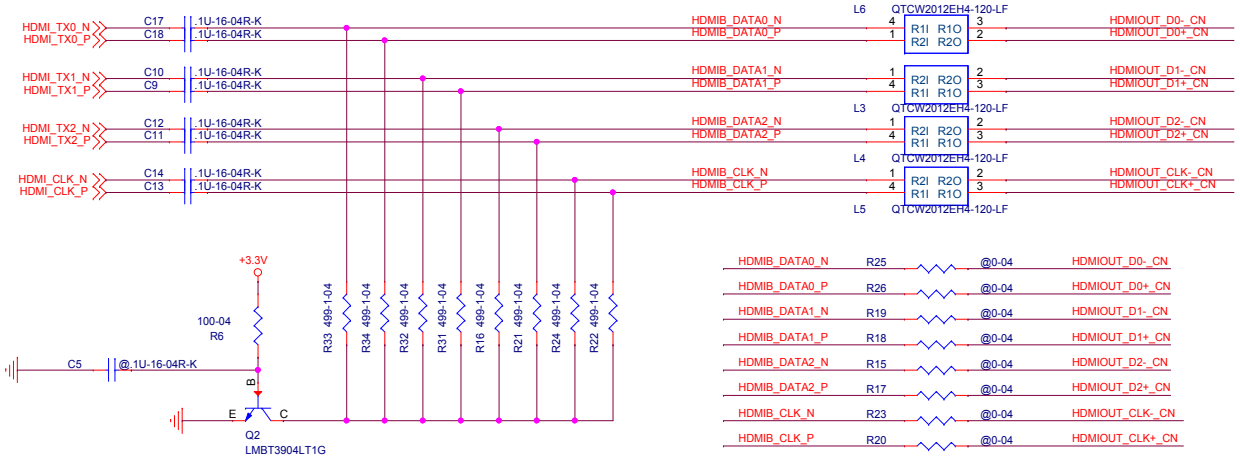
Title	M.2_SSD	
Size: Custom	Document Number: PF4PN2F	Rev: 1.0
Date: Wednesday, August 28, 2019	Sheet 15 of 44	

WLAN CONN



同方国际信息技术有限公司

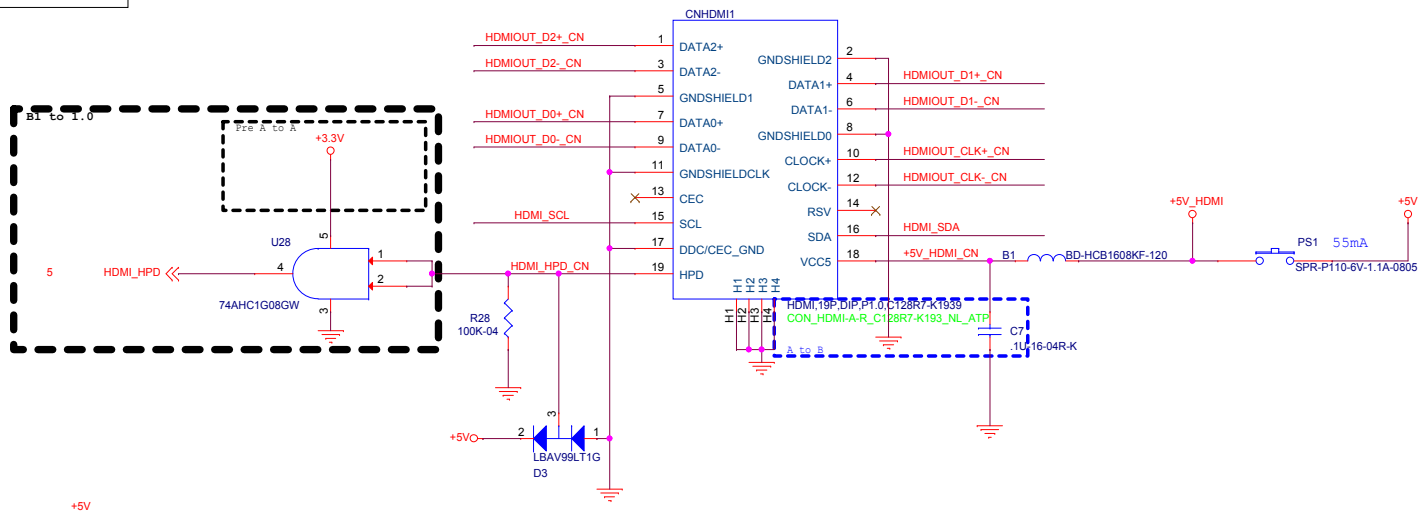
Title	M.2_WLAN	
Size: Custom	Document Number: PF4PN2F	Rev: 1.0
Date: Tuesday, August 27, 2019	Sheet 16 of 44	

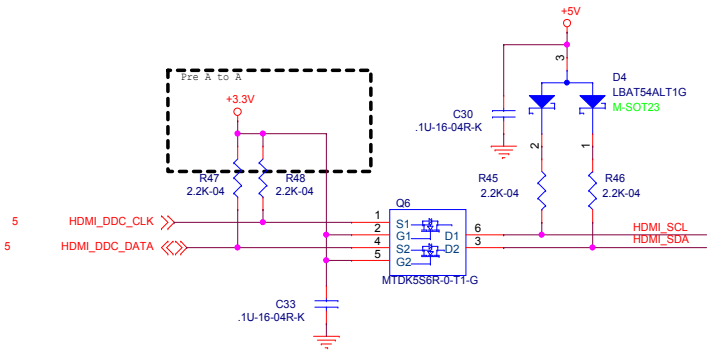


HDMI 2.0 Max =18Gbps, 4K resolution at 60HZ

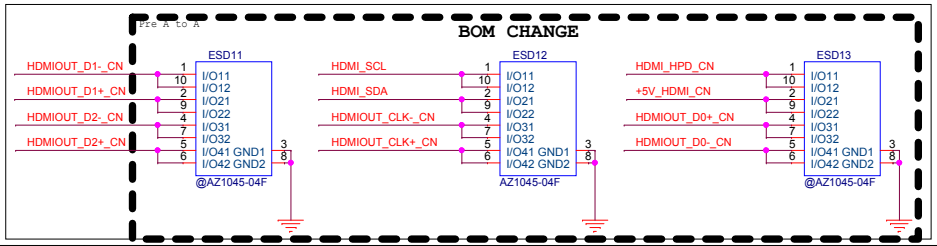
HDMI R2.0 670MHz NV Supported
HDMI R1.4 340MHz Intel Supported

HDMI CONN





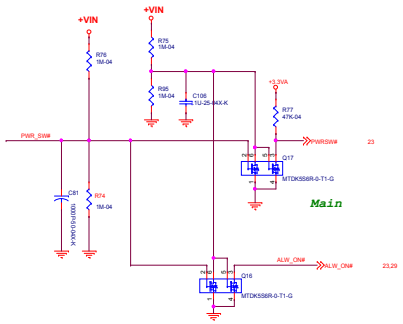
Close to connector



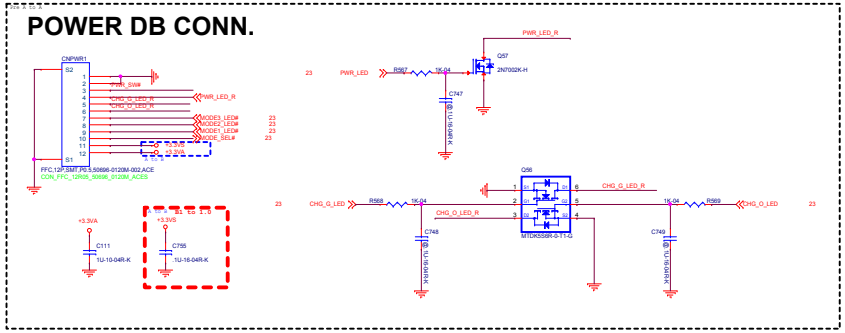
同方国际信息技术有限公司

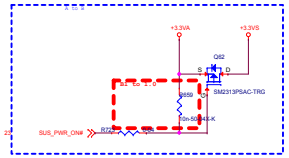
Title	HDMI	
Size: Custom	Document Number: PF4PN2F	Rev: 1.0
Date: Tuesday, August 27, 2019	Sheet 17 of 44	

POWER SW

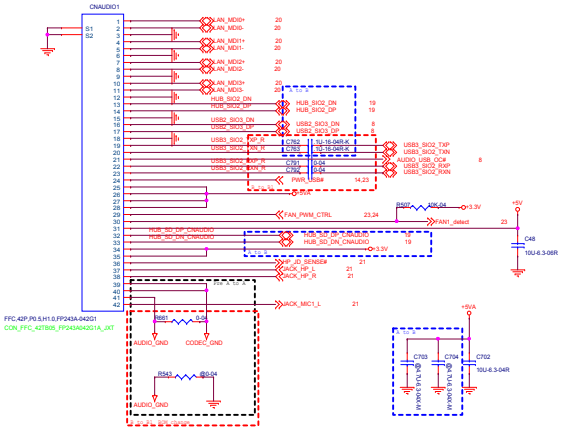


POWER DB CONN.

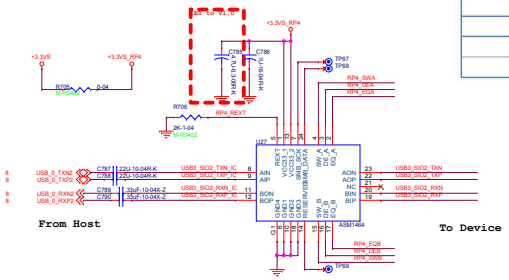




Audio&LAN DB CONN.

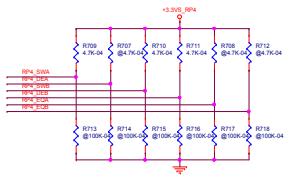


Redriver



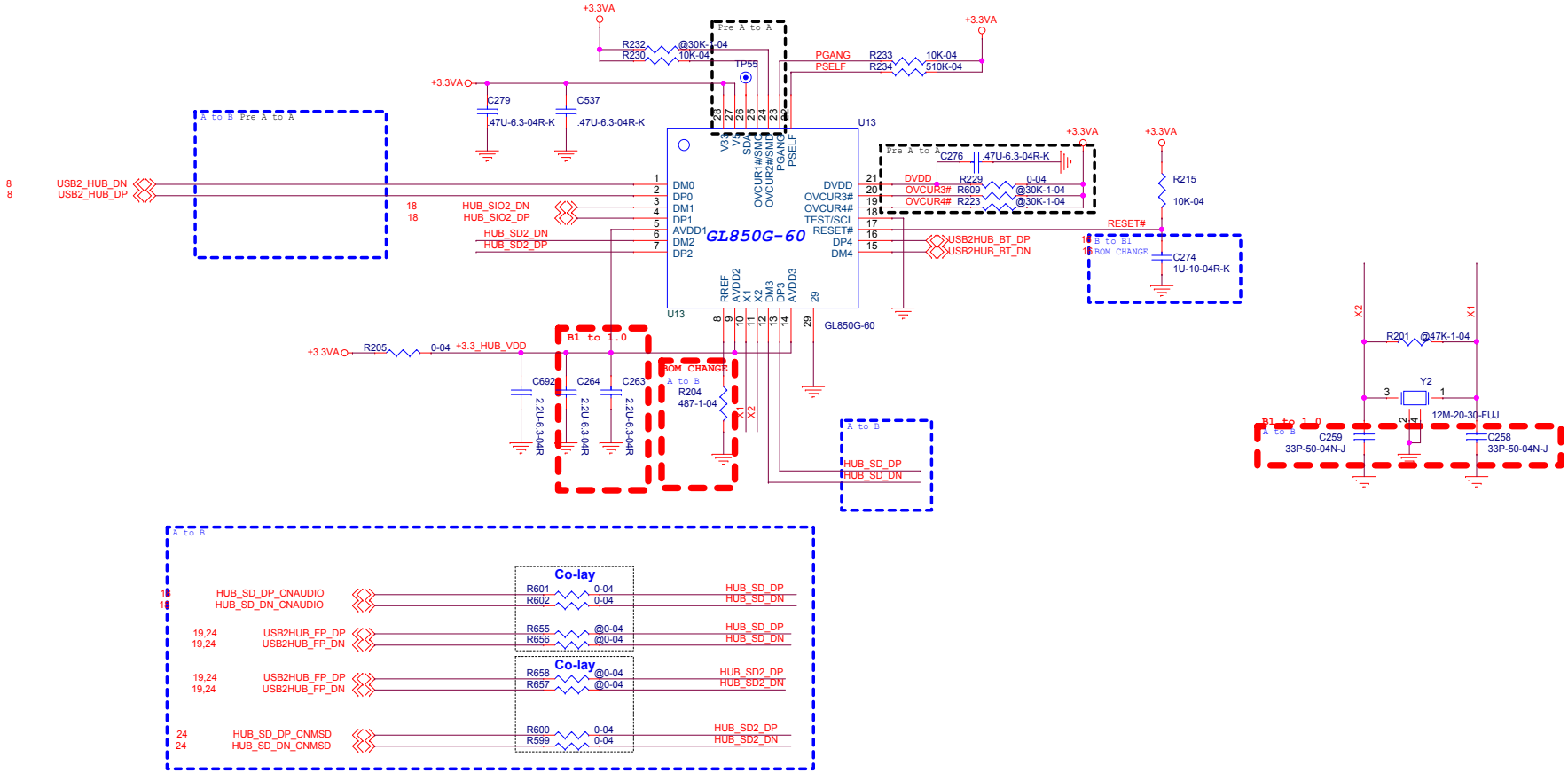
Strapping Table

SW_X	DE_X	Descriptions
0	0	-1.5dB
0	1	0dB
1	0	+1.5dB
1	1	+3dB



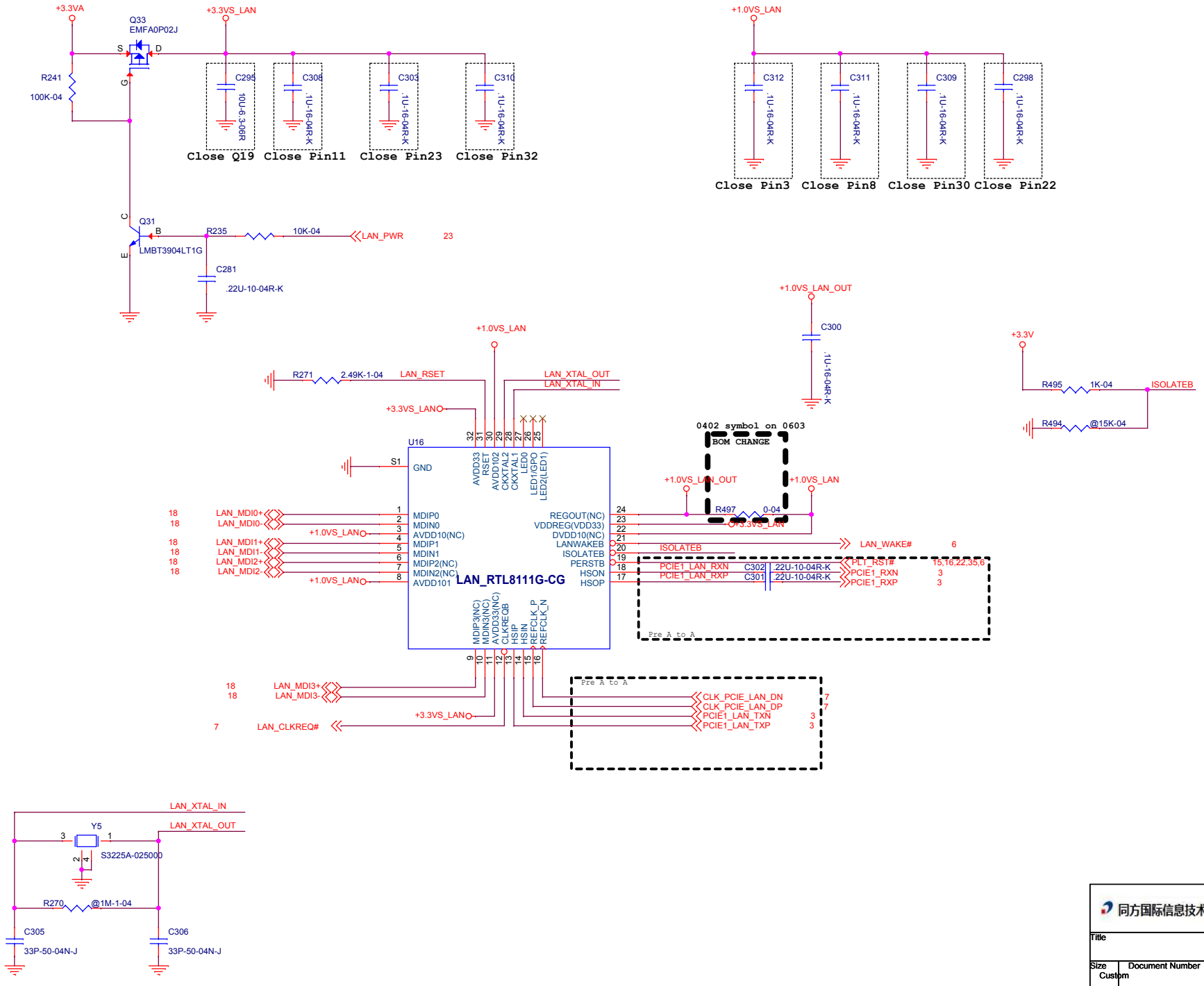
同方国际信息技术有限公司

Title	PWR_DB/Audio_DB CONN	
Size D	Document Number PF4PN2F	Rev 1.0
Date: Tuesday, August 27, 2019	Sheet 18 of 44	



同方国际信息技术有限公司

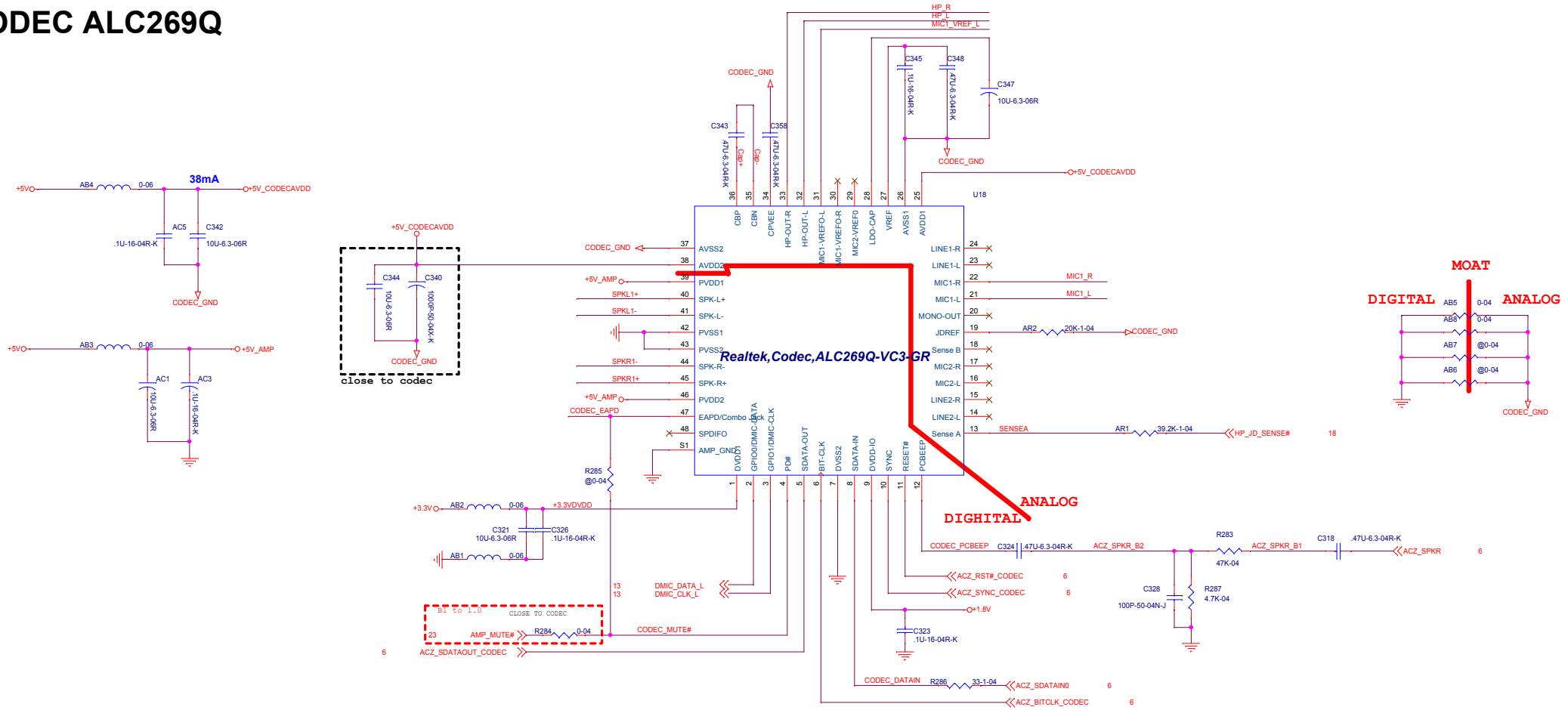
Title	USB HUB	
Size: Custom	Document Number: PF4PN2F	Rev: 1.0
Date: Tuesday, August 27, 2019	Sheet 19 of 44	



同方国际信息技术有限公司

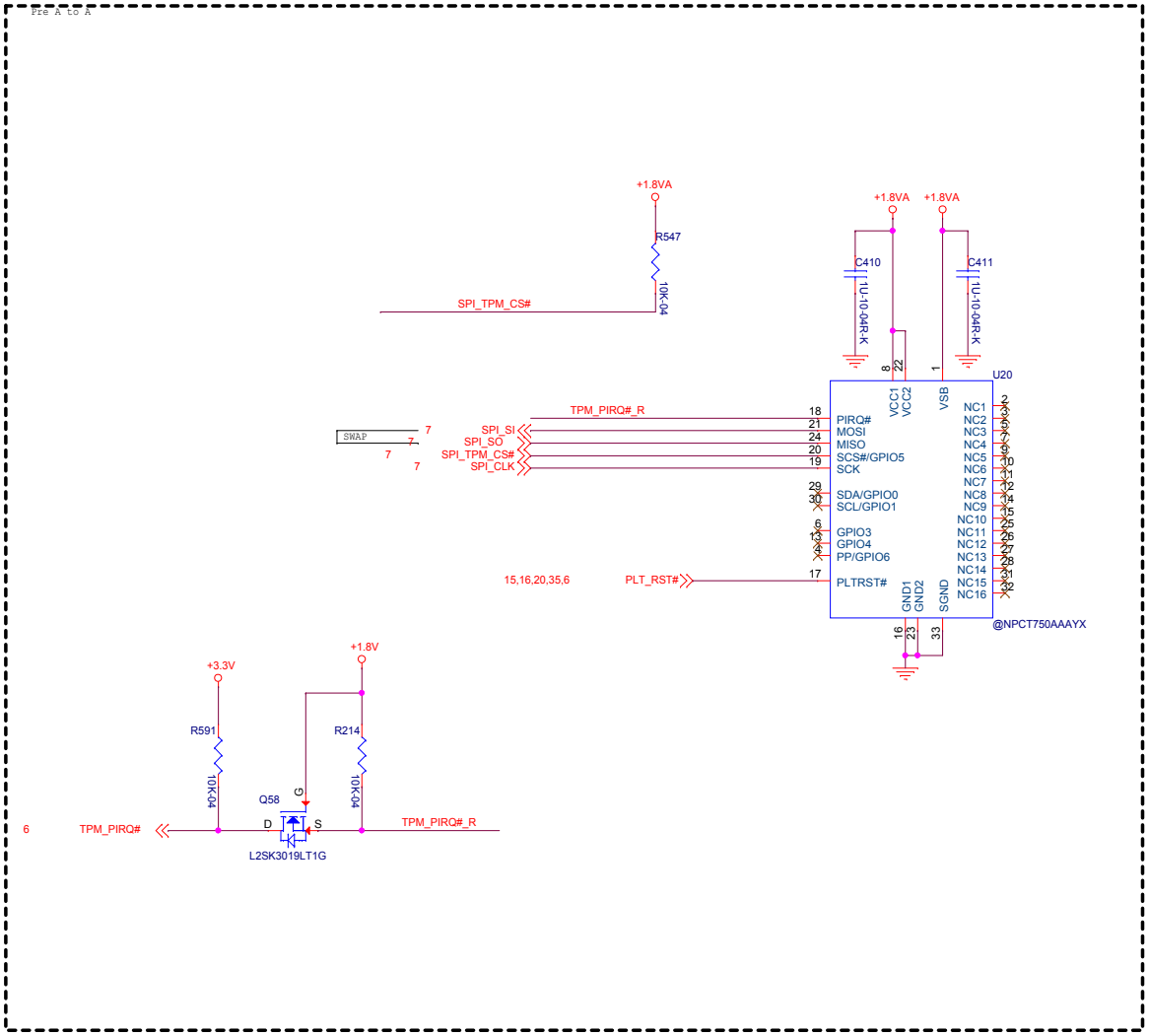
Title	LAN(RTL8111G-CG)	
Size: Custom	Document Number: PF4PN2F	Rev: 1.0
Date: Tuesday, August 27, 2019	Sheet 20 of 44	

CODEC ALC269Q



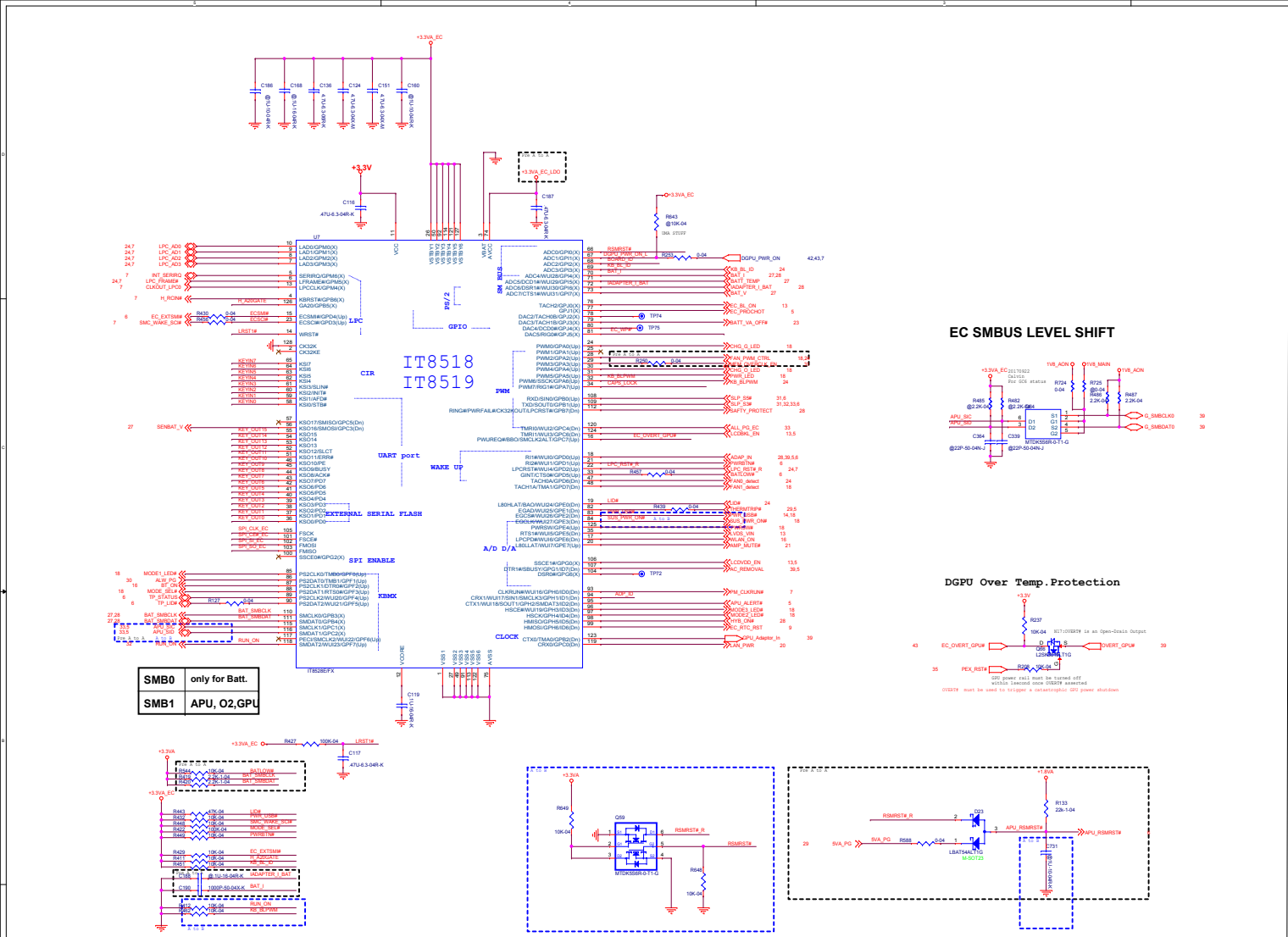
同方国际信息技术有限公司

Title	AUDIO(ALC269Q)/SPK	
Size: Custom	Document Number: PF4PN2F	Rev: 1.0
Date: Tuesday, August 27, 2019	Sheet 21 of 44	

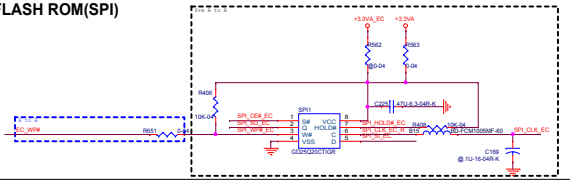


同方国际信息技术有限公司

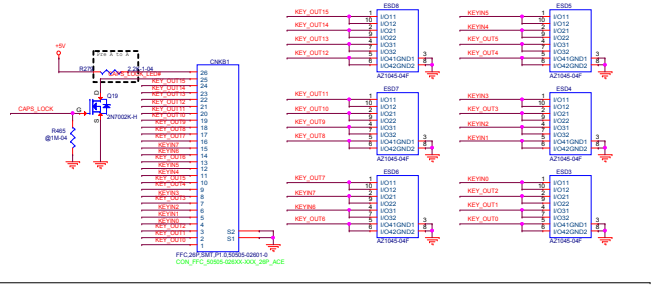
Title	TPM	
Size: Custom	Document Number: PF4PN2F	Rev: 1.0
Date: Tuesday, August 27, 2019	Sheet 22 of 44	

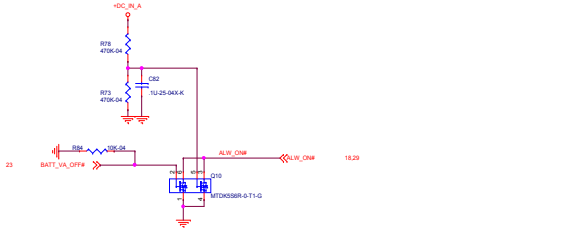


EC FLASH ROM(SPI)

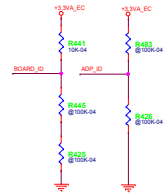


KEYBOARD





Platform ID



No.	Keyboard_ID	Description	R1	R2	MEMO
1	(3.3V)				
2	(2.8V)		56K-1-04	0-04	
3	(2.6V)		36K-1-04	1.24K-1-04	
4	(2.4V)		26.7K-1-04	0-04	
5			15.4K-1-04	0-04	
6	(2.0V)		12K-1-04	0-04	
7	(1.65V)				
8	(1.2V)		5.62K-1-04	100-1-04	
9	(0.8V)		3.24K-1-04	0-04	
10	(0.4V)		1.33K-1-04	75-1-04	
11	(0.0V)		0-04	0-04	

同方国际信息技术有限公司

Title	EC(IT8528E)/BIOS/KB CONN	
Size: D	Document Number: PF4PN2F	Rev: 1.0
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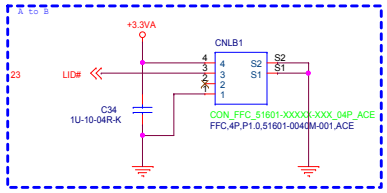
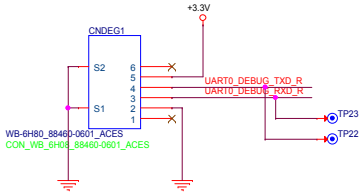
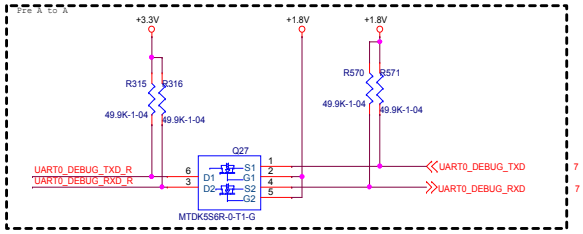
LID Switch CONN

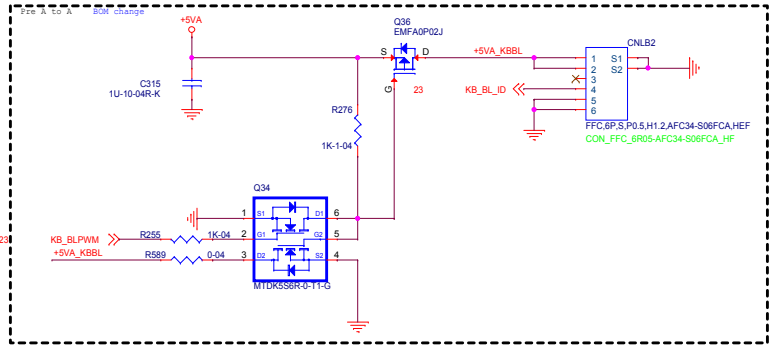


UART debug port

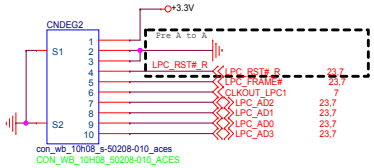




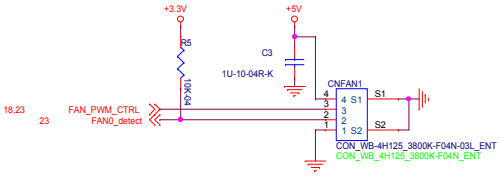
KB Back-Light CONN



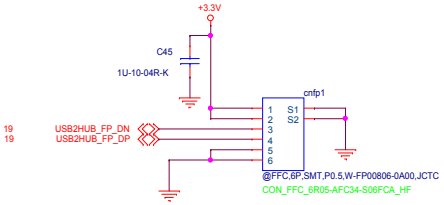
LPC debug port



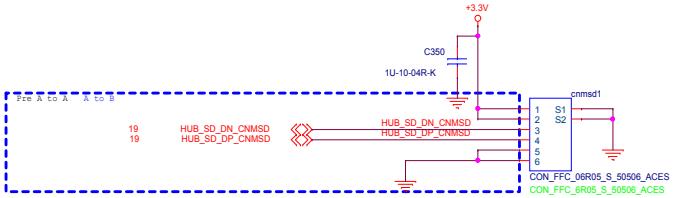
FAN CONTROLLER CONN



FINGER PRINTER CONN

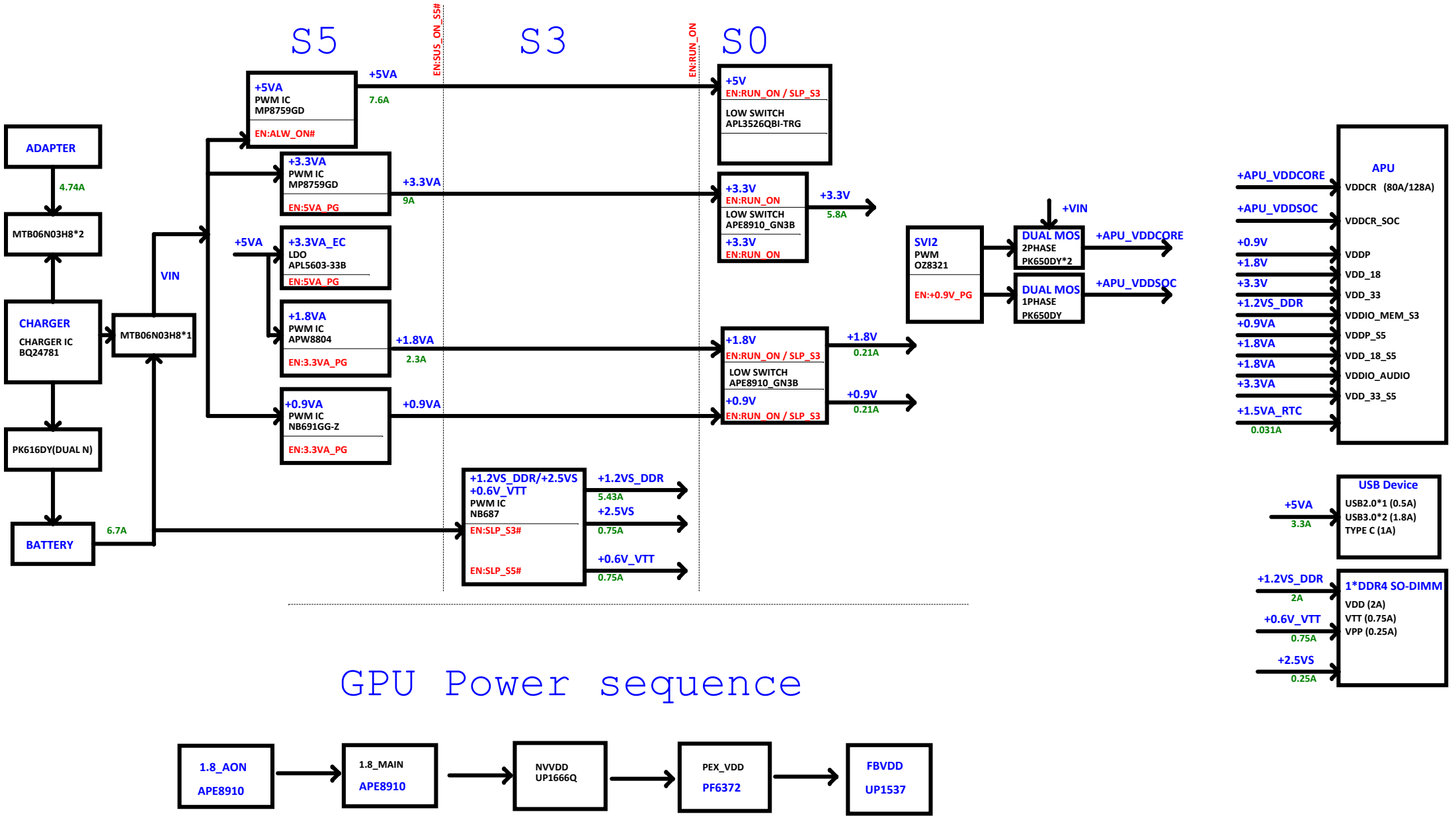


Micro SD2 CONN



同方国际信息技术有限公司

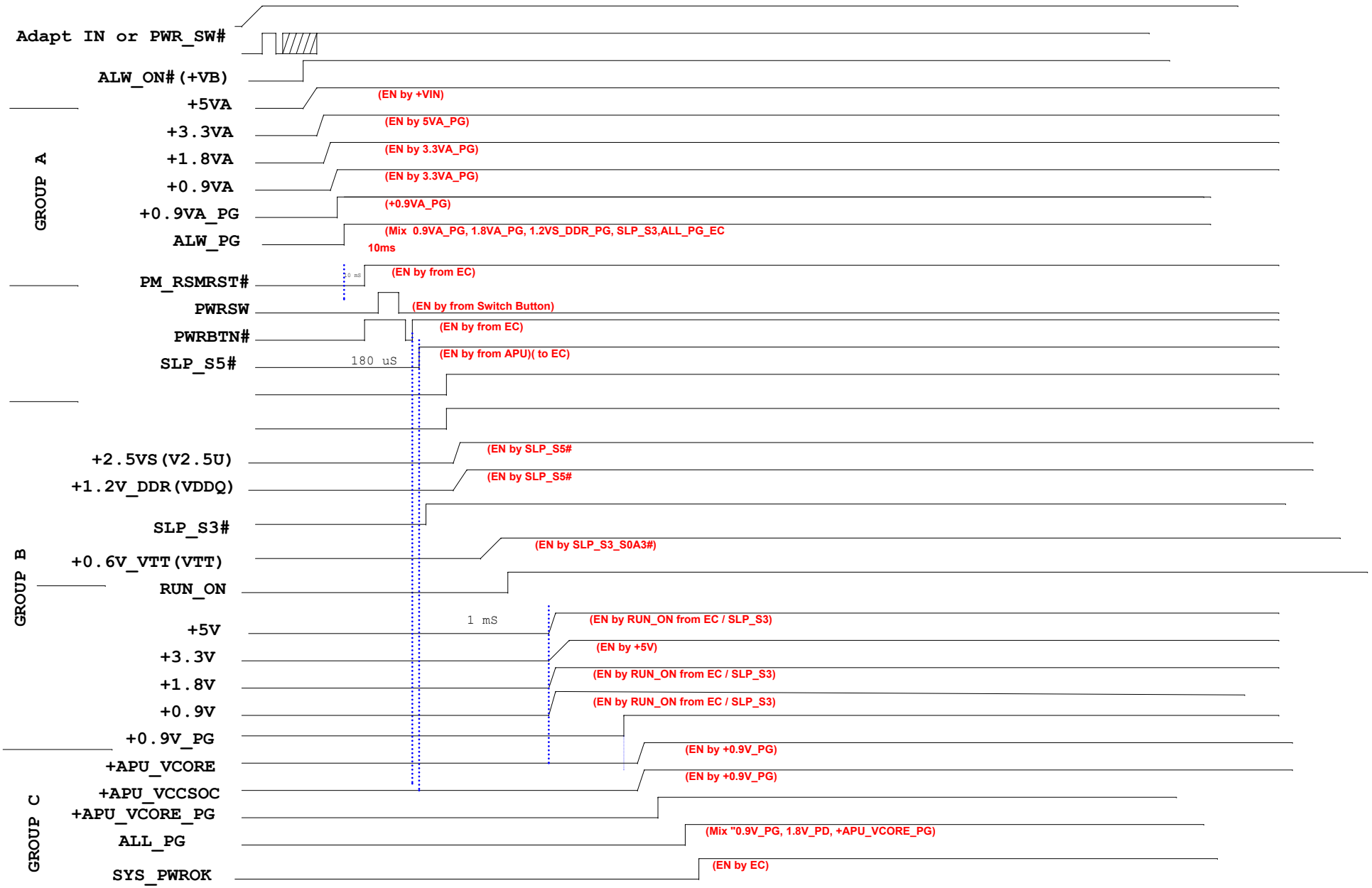
Title	LID/KBBL/FAN/DEBUG/FP/SD2	
Size C	Document Number PF4PN2F	Rev 1.0
Date: Tuesday, August 27, 2019	Sheet 24 of 44	



GPU Power sequence

同方国际信息技术有限公司

Title	POWER MAP	
Size: Custom	Document Number: PF4PN2F	Rev: 1.0
Date: Tuesday, August 27, 2019	Sheet 25 of 44	



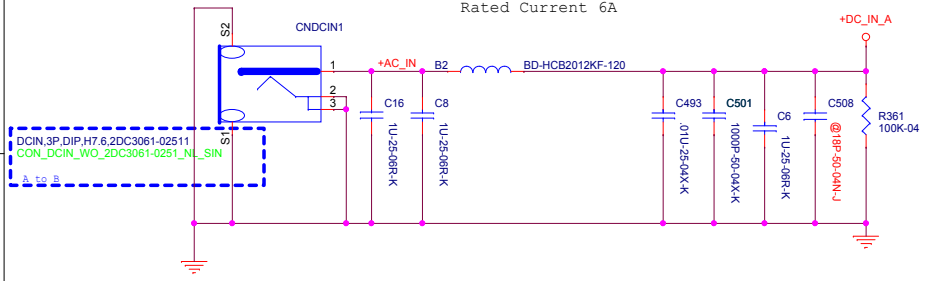
POWER ON SEQUENCE

同方国际信息技术有限公司

Title	POWER SEQUENCE	
Size: Custom	Document Number: PF4PN2F	Rev: 1.0
Date: Tuesday, August 27, 2019	Sheet 26 of 44	

+DC_IN

```
EMB20NP3V
ID=-13A  TC=100 deg
Ipulse=-72A
Avalanche=-10A
9watt 1ms
15Watt  0.1ms
```



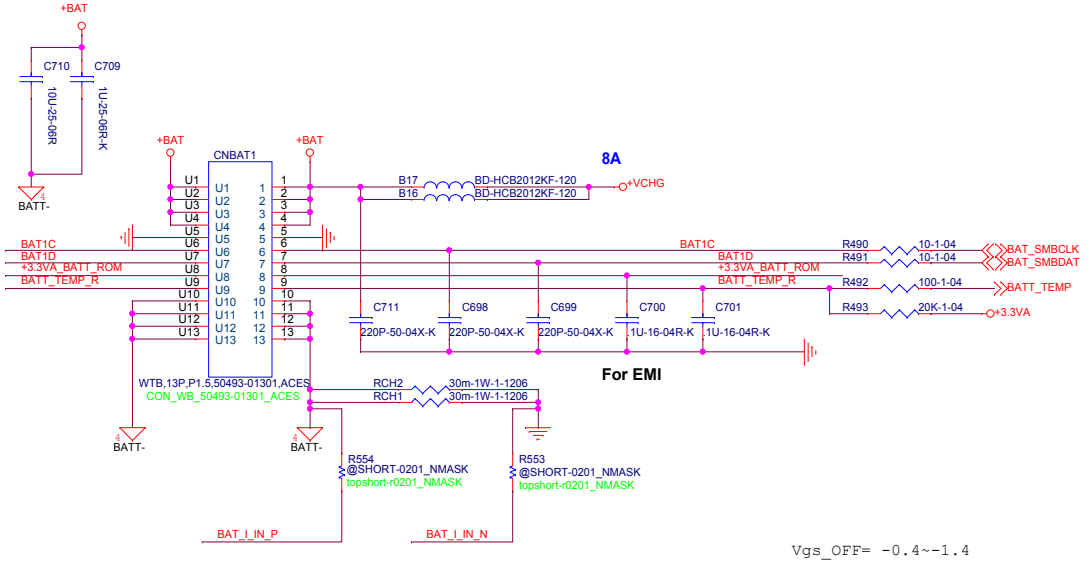
Battery Current Detect

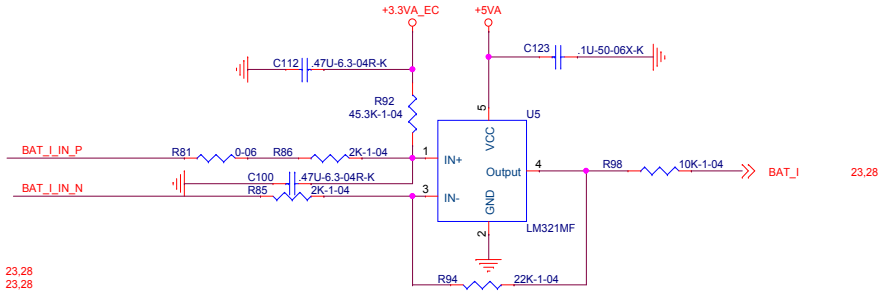
RCH1 //RCH2 =7.5mohm

BAT_I	ICHG (0.0862V/1A)
2.0192V	4A
1.8468V	2A
1.7606V	1A
1.6744V	0A
1.5882V	-1A
1.5020V	-2A
1.3296V	-4A
1.1572V	-6A
0.9848V	-8A
0.8124V	-10A

RCH1 //RCH2 =15mohm

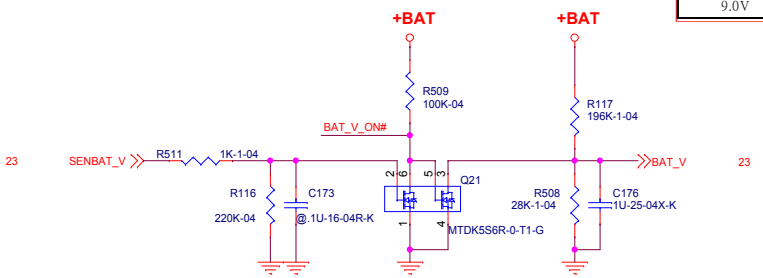
BAT_I	ICHG (0.1724V/1A)
2.3640V	4A
2.0192V	2A
1.8468V	1A
1.6744V	0A
1.5020V	-1A
1.3296V	-2A
0.9848V	-4A
0.6400V	-6A
0.2952V	-8A
0.1228V	-9A

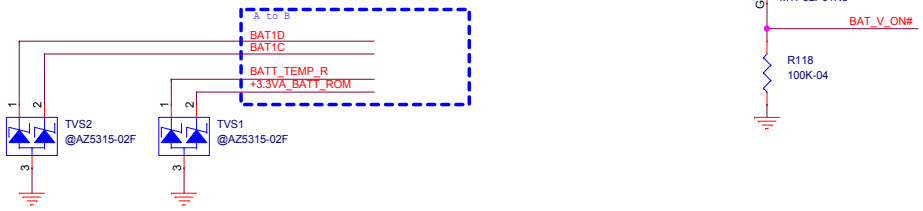


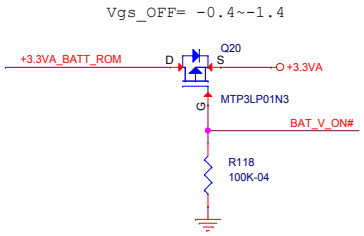


BAT_Voltage	BAT_V
17.6V	2.2V
16.8V	2.1V
13.2V	1.65V
12.6V	1.575V
9.0V	1.125V

Battery Voltage Detect







同方国际信息技术有限公司

Title	DC IN/BAT_IN	
Size: Custom	Document Number: PF4PN2F	Rev: 1.0
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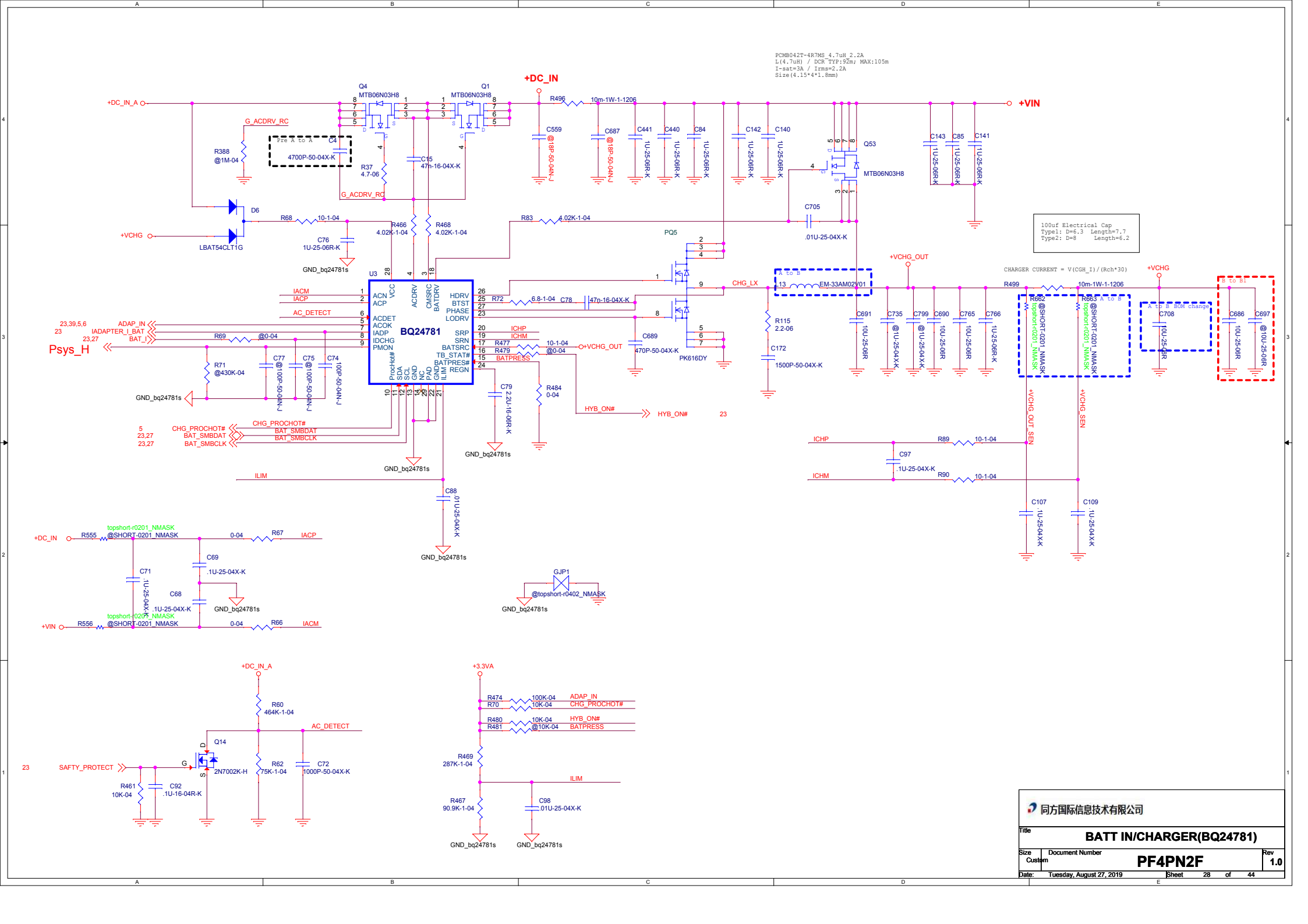
PCMB042T-4R7MS_4.7uH_2.2A
L(4.7uH) / DCR TYP:92m; MAX:105m
I-sat=3A / Irms=2.2A
Size(4.15*4*1.8mm)
+DC_IN
+VIN
+DC_IN_A
Q4 MTB06N03H8
Q1 MTB06N03H8
Q53 MTB06N03H8
R496 10m-1W-1-1206
C559 @18P-50-04N-J
C687 @18P-50-04N-J
C441 1U-25-06R-K
C440 1U-25-06R-K
C84 1U-25-06R-K
C142 1U-25-06R-K
C140 1U-25-06R-K
C143 1U-25-06R-K
C85 1U-25-06R-K
C141 1U-25-06R-K
G_ACDRV_RC
R388 @1M-04
C4 4700P-50-04X-K
R37 4.7-06
C15 47n-16-04X-K
D6
LBAT54CLT1G
+VCHG
R68 10-1-04
C76 1U-25-06R-K
GND_bq24781s
R466 4.02K-1-04
R468 4.02K-1-04
R83 4.02K-1-04
C705 .01U-25-04X-K
PQ5
PK616DY
CHG_LX
EM-33AM02V01
+VCHG_OUT
R499 10m-1W-1-1206
R662 @SHORT-0201_NMASK
R663 @SHORT-0201_NMASK
C708 10U-25-06R
C686 10U-25-06R
C697 @10U-25-06R
C691 10U-25-06R
C735 @1U-25-04X-K
C799 @1U-25-04X-K
C690 10U-25-06R
C765 10U-25-06R
C766 1U-25-06R-K
R115 2.2-06
C172 1500P-50-04X-K
C689 470P-50-04X-K
R72 6.8-1-04
C78 47n-16-04X-K
U3
BQ24781
ACN VCC ACDRV CMSRC BATDRV HDRV BTST PHASE LODRV
ACP SRP SRN BATSRC TB_STAT# BATPRES# REGN
ACDET ACOK IADP IDCHG PMON ProchOt# SDA SCL GND NC PAD GNDS ILIM
IACM
IACP
AC_DETECT
ADAP_IN
IADAPTER_I_BAT
BAT_I
Psys_H
R69 @0-04
R71 @430K-04
C77 @100P-50-04N-J
C75 @100P-50-04N-J
C74 100P-50-04N-J
ICHP
ICHM
R477 10-1-04
R479 @0-04
BATPRESS
+VCHG_OUT
R484 0-04
C79 2.2U-16-06R-K
HYB_ON#
CHG_PROCHOT#
BAT_SMBDAT
BAT_SMBCLK
ILIM
C88 .01U-25-04X-K
CHARGER CURRENT = V(CGH_I)/(Rch*30)
100uf Electrical Cap
Type1: D=6.3 Length=7.7
Type2: D=8 Length=6.2
A to B
B to B1
A to B BOM change
+VCHG_OUT_SEN
+VCHG_SEN
R89 10-1-04
C97 .1U-25-04X-K
R90 10-1-04
C107 .1U-25-04X-K
C109 .1U-25-04X-K
R555 @SHORT-0201_NMASK
R556 @SHORT-0201_NMASK
R67 0-04
R66 0-04
C69 .1U-25-04X-K
C71 .1U-25-04X-K
C68 .1U-25-04X-K
GJP1
@topshort-r0402_NMASK
+DC_IN_A
R60 464K-1-04
Q14
2N7002K-H
SAFTY_PROTECT
R461 10K-04
C92 .1U-16-04R-K
R62 75K-1-04
C72 1000P-50-04X-K
+3.3VA
R474 100K-04
R70 10K-04
R480 10K-04
R481 @10K-04
R469 287K-1-04
R467 90.9K-1-04
C98 .01U-25-04X-K
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BATT IN/CHARGER(BQ24781)
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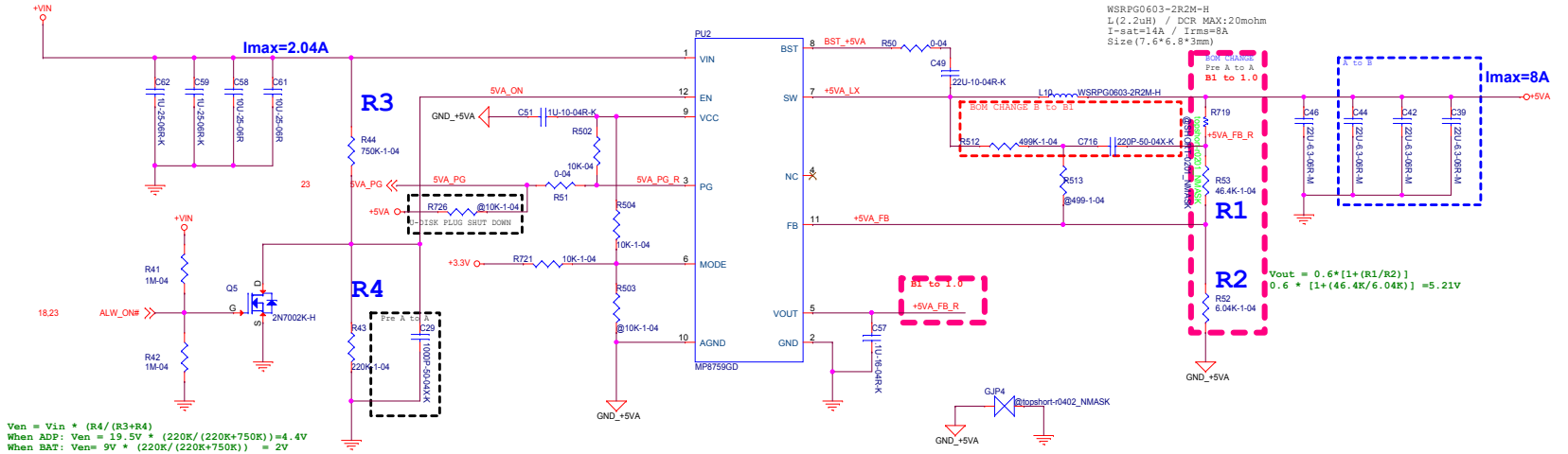
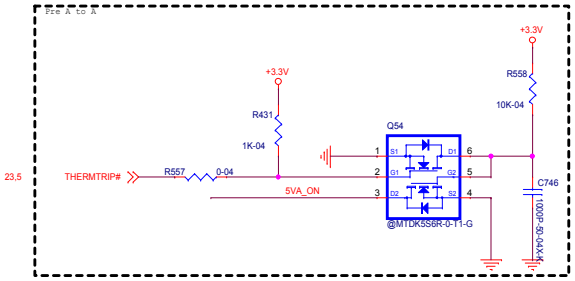
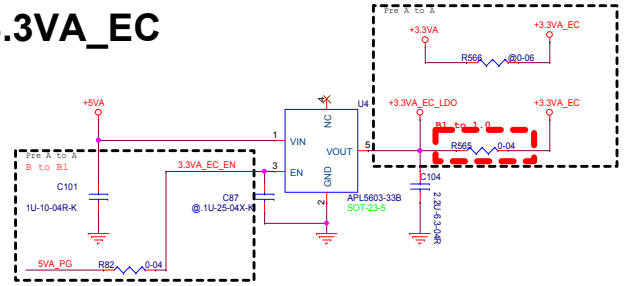
+5VA

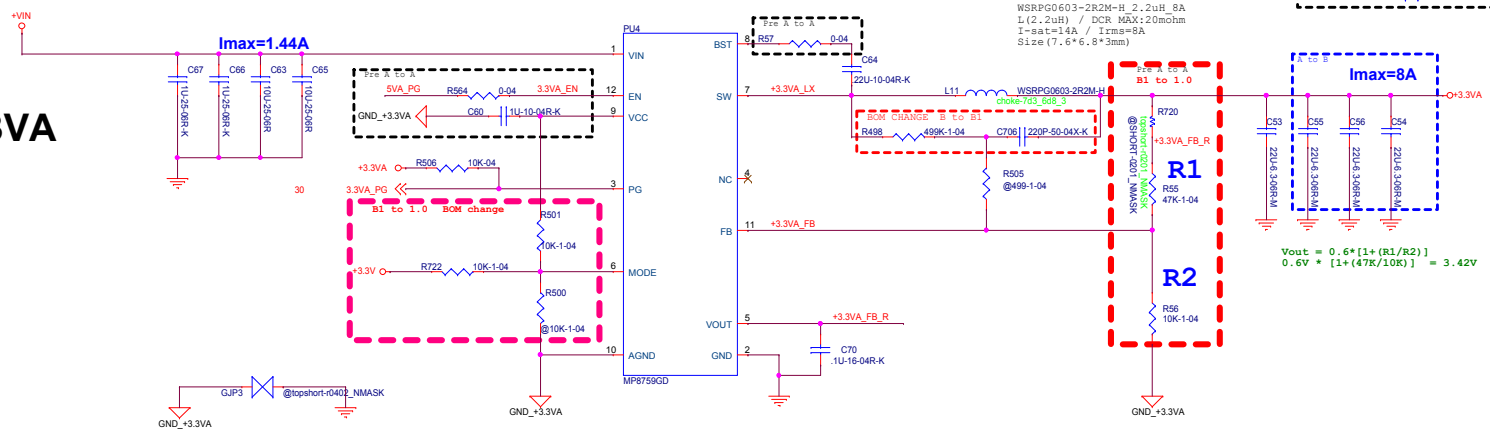




+3.3VA_EC



+3.3VA



同方国际信息技术有限公司			
Title	POWER +5VA/+3.3VA/+3.3VA_EC		
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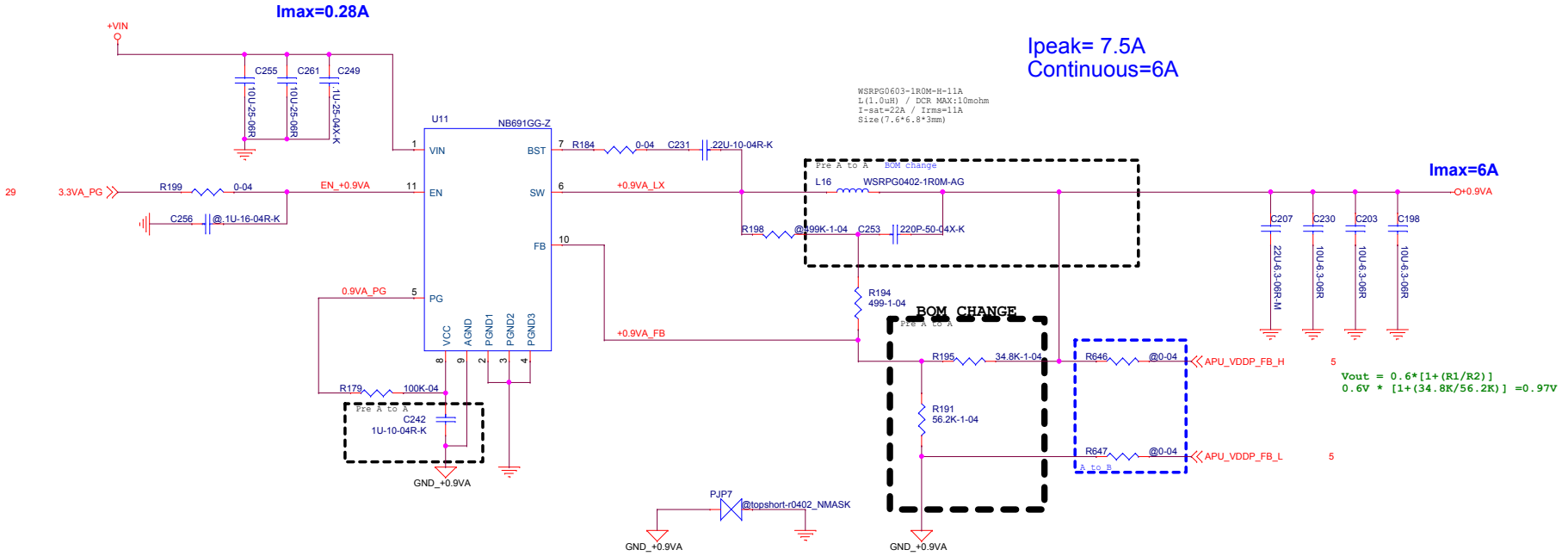
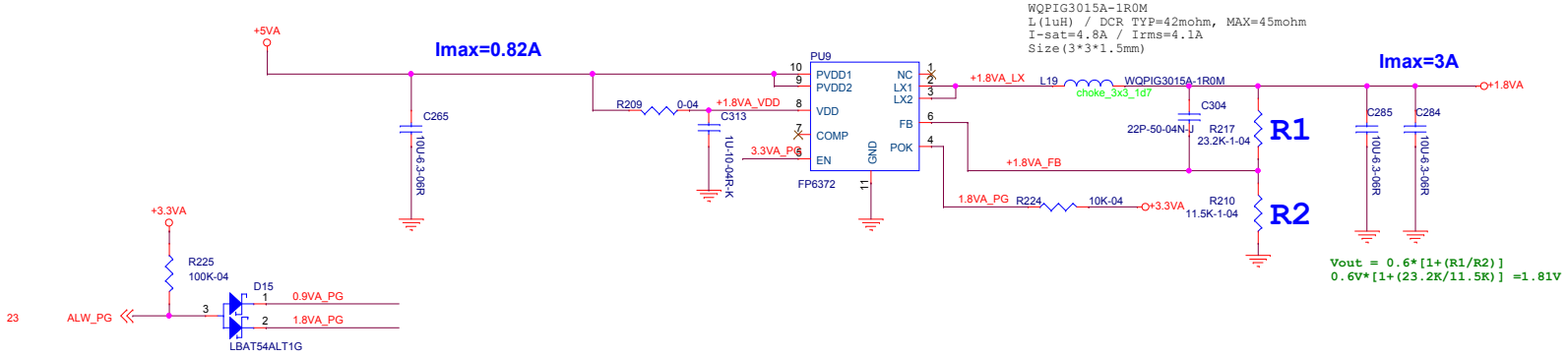
+0.9VA



+1.8VA



同方国际信息技术有限公司

Title	POWER_0.9VA/+1.8VA	
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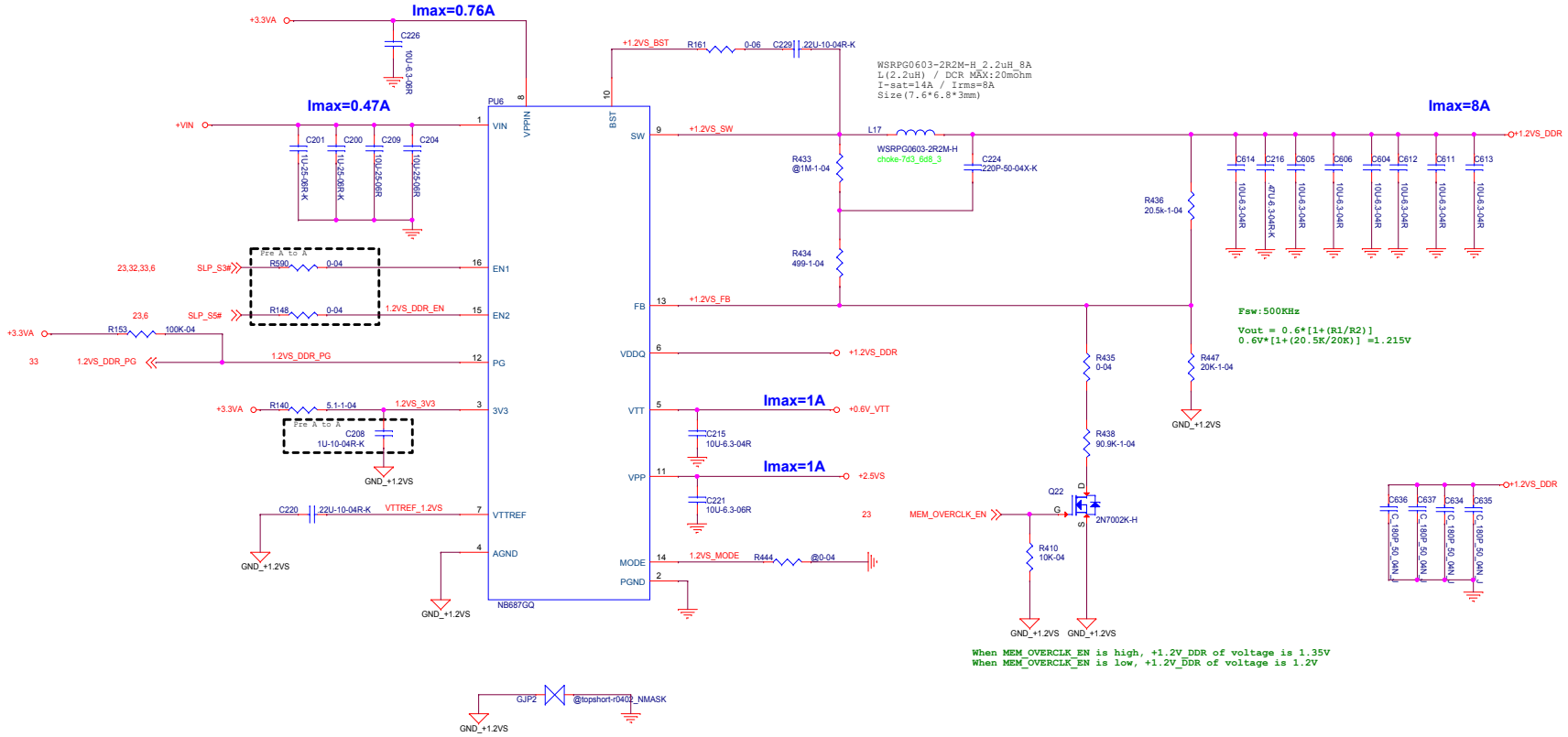
+1.2VS_DDR/+2.5VS/+0.6V_VTT



同方国际信息技术有限公司

Title	POWER +1.2VS/2.5VS/VTT	
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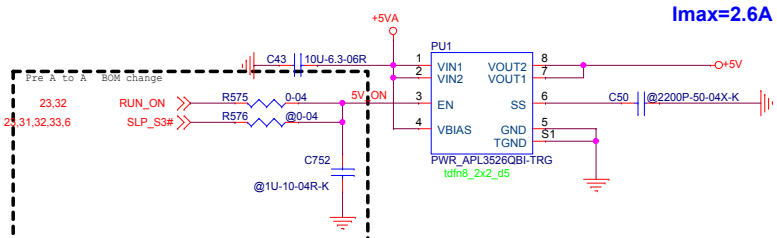
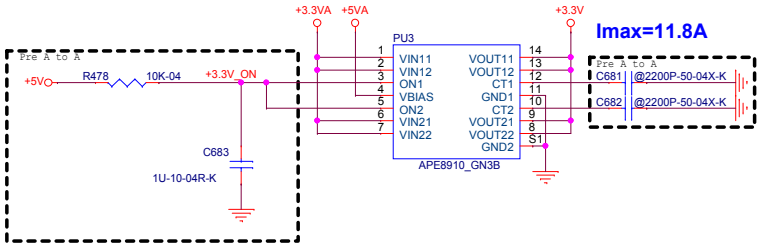
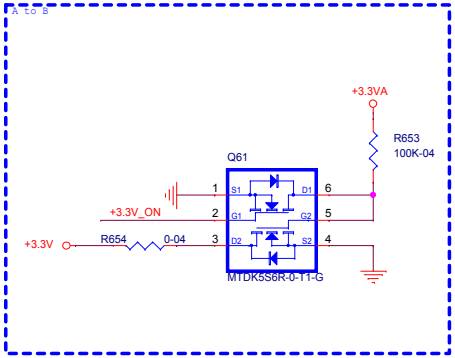
+5V



+3.3V



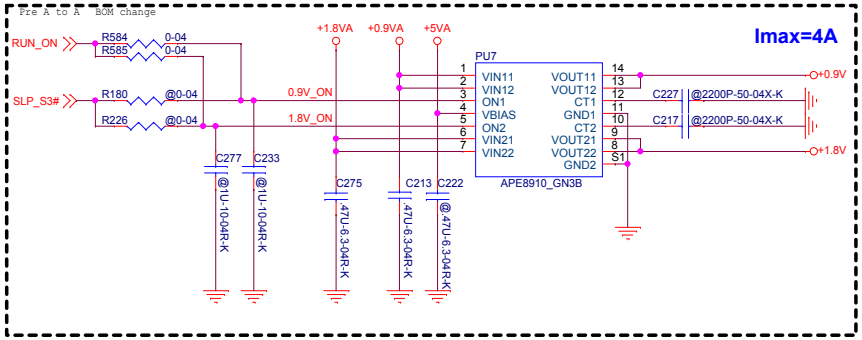


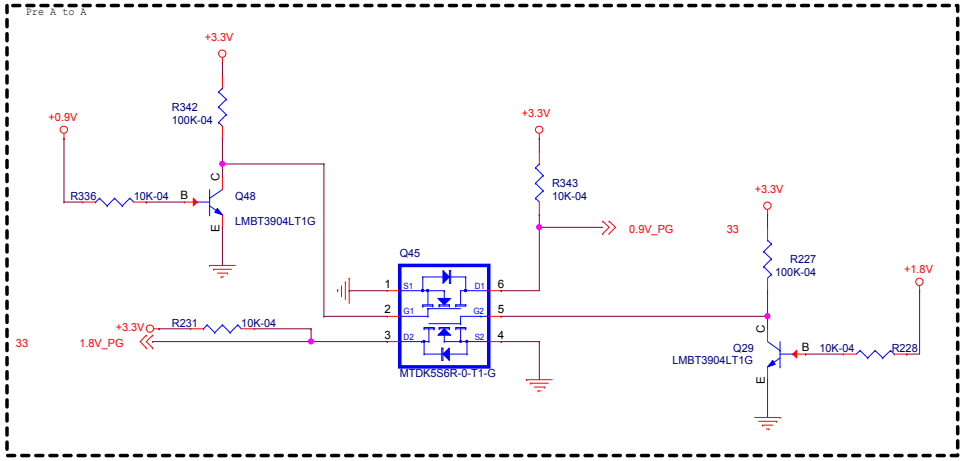
+0.9V

23,32

+1.8V

23,31,32,33,6





同方国际信息技术有限公司

Title	+5V/+3.3V/+1.8V/+0.9V	
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1 L32=L33=0.36uH/2.2mohm, 953-1-04 PN
2 L34=0.68uH/5.5mohm,, 1.21k-1-04 PN

Load line & OCP setting:
Load Line :R304 R305
OCP : R306 R307

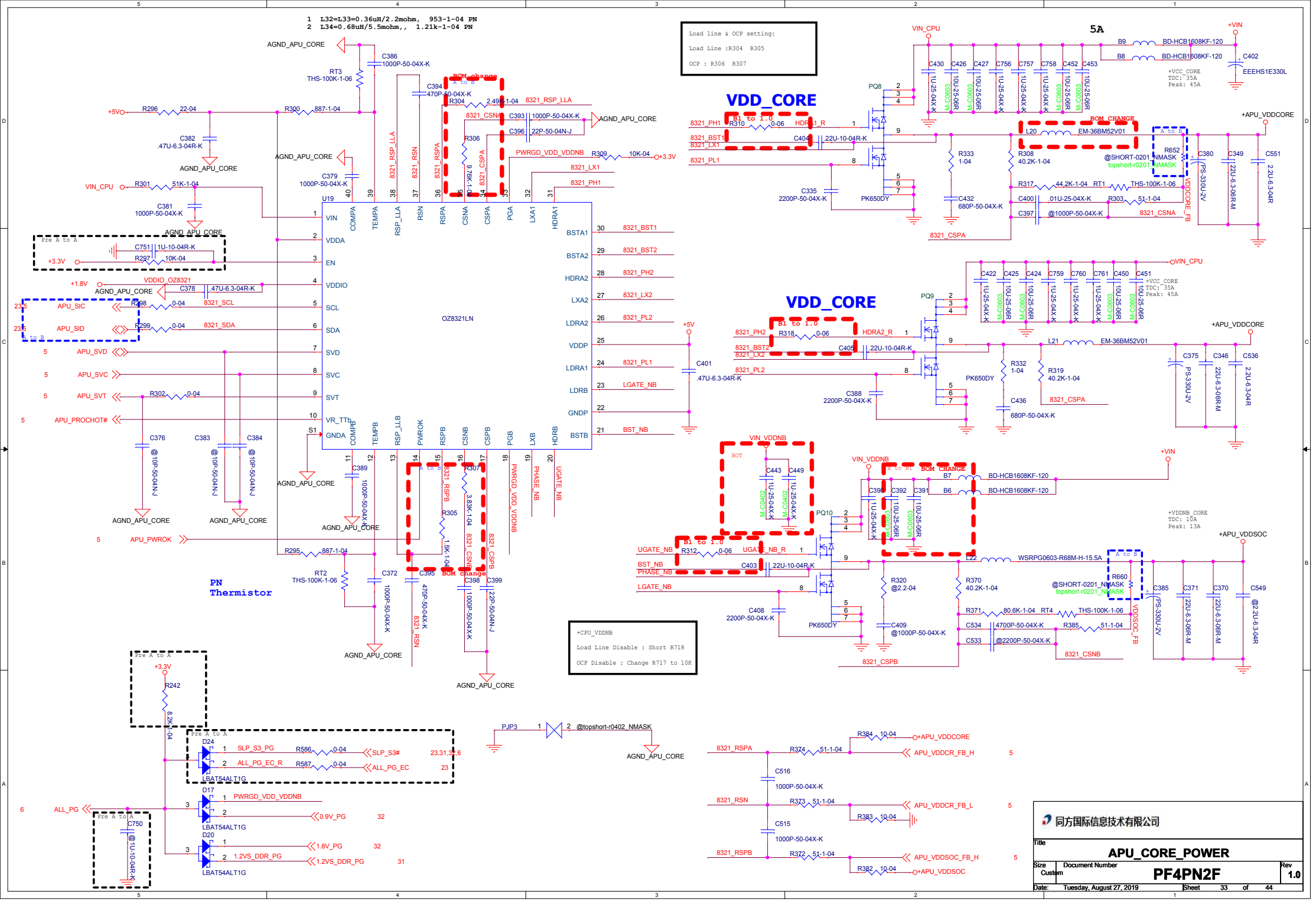
VDD_CORE

5A

VDD_CORE

PN Thermistor

+CPU_VDDNB
Load Line Disable : Short R718
OCP Disable : Change R717 to 10K



同方国际信息技术有限公司

Title	APU_CORE_POWER	
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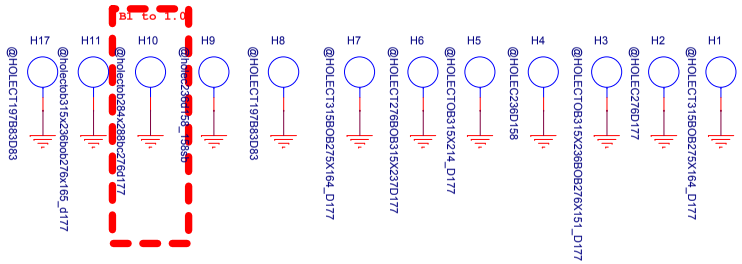
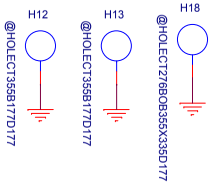
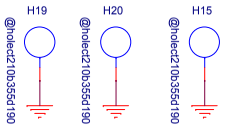
A to B

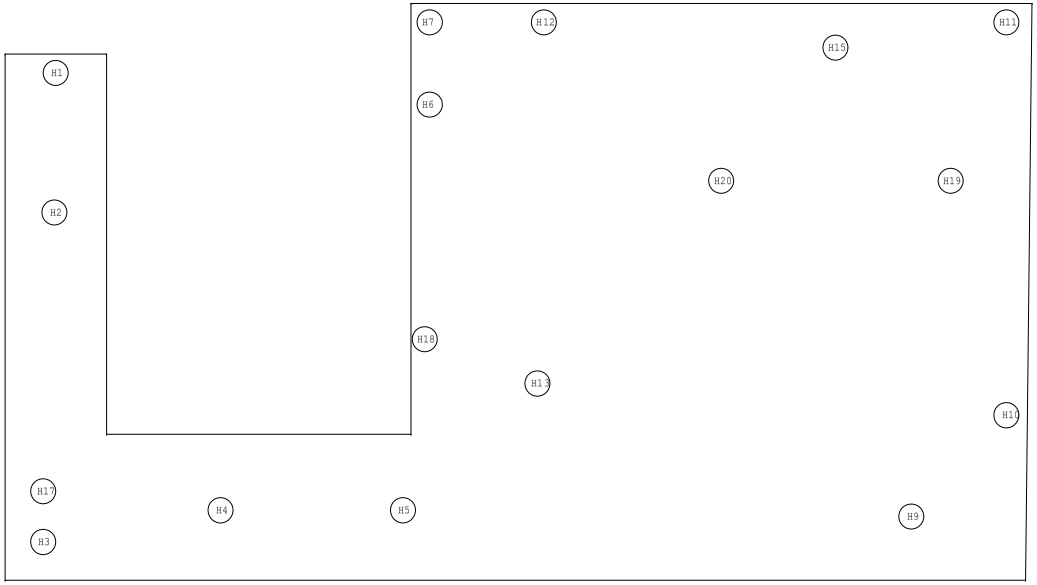
PCB HOLE



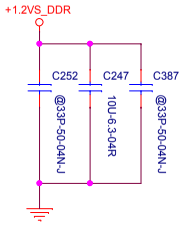
THERMAL HOLE

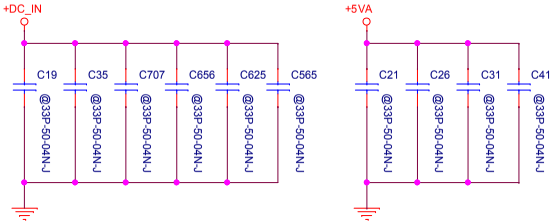


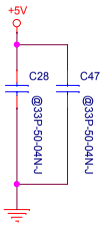


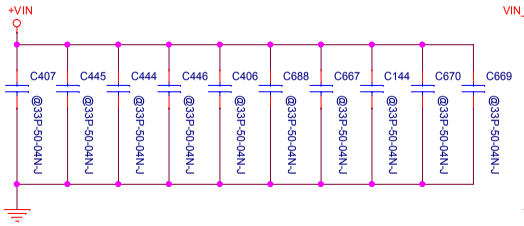


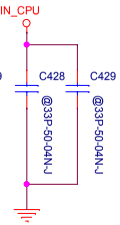
For RF

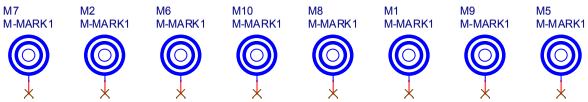












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Title	Other/SCREW	
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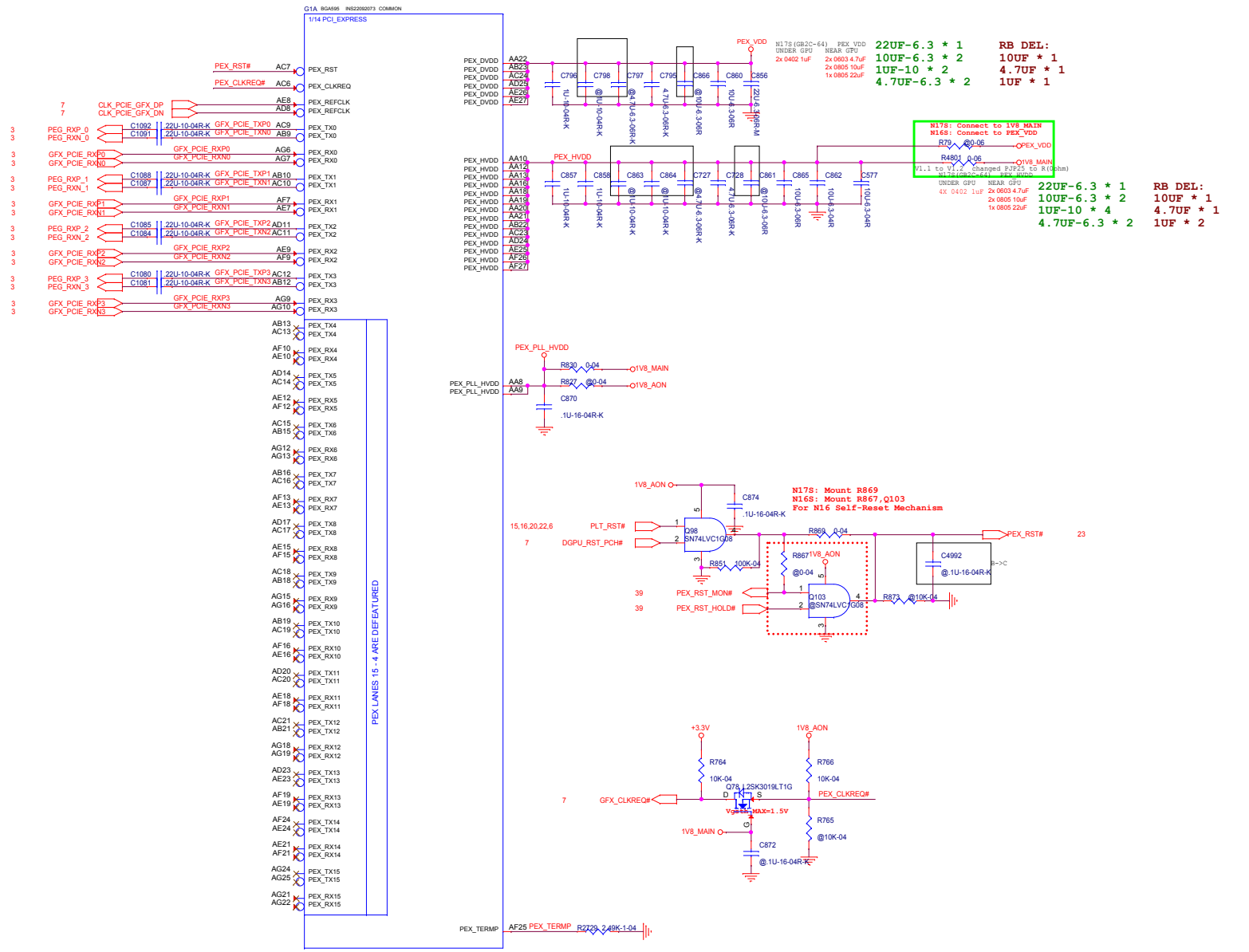

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Title	NV-PCIE		
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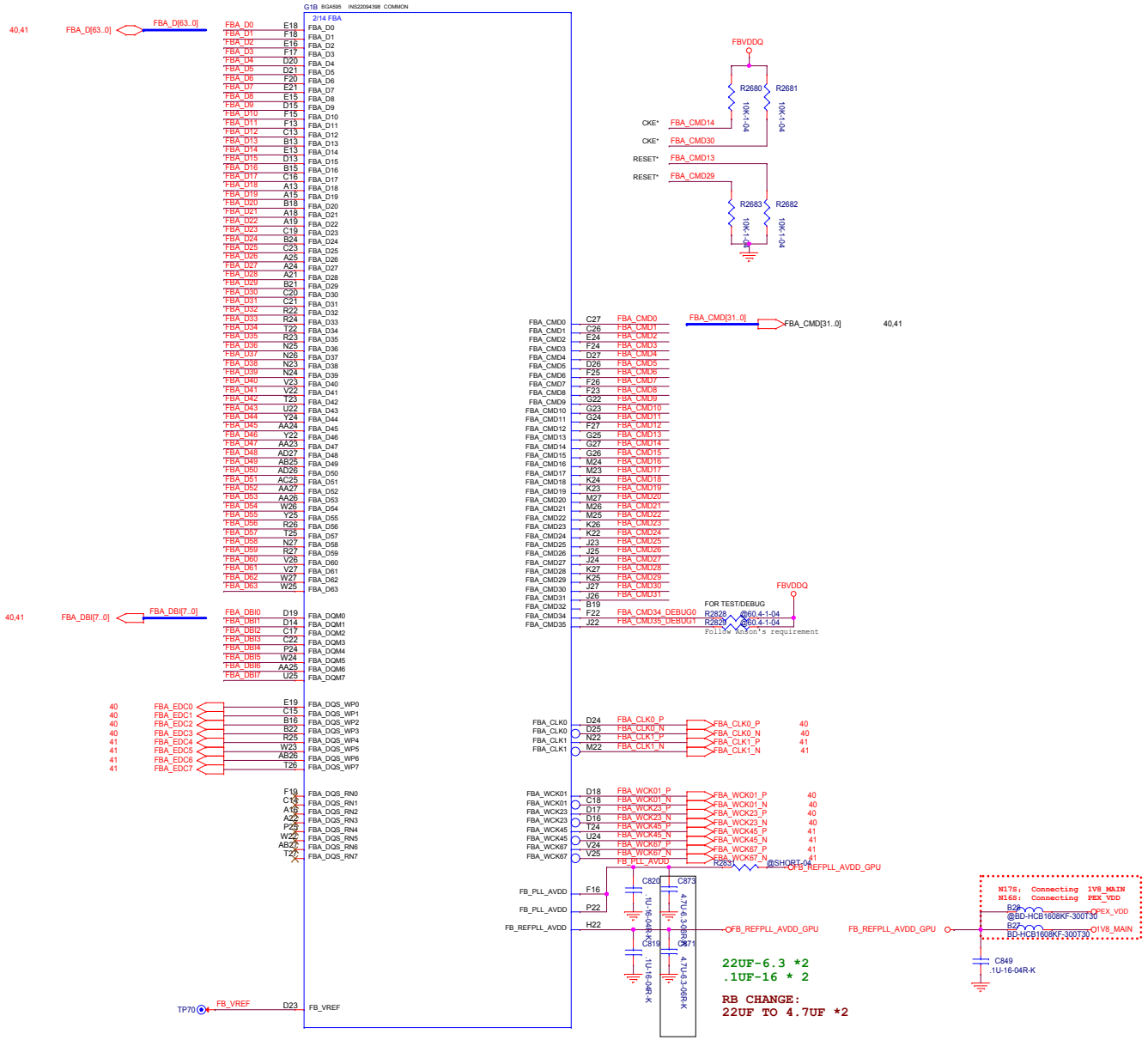

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Title	FRAME BUFFER	
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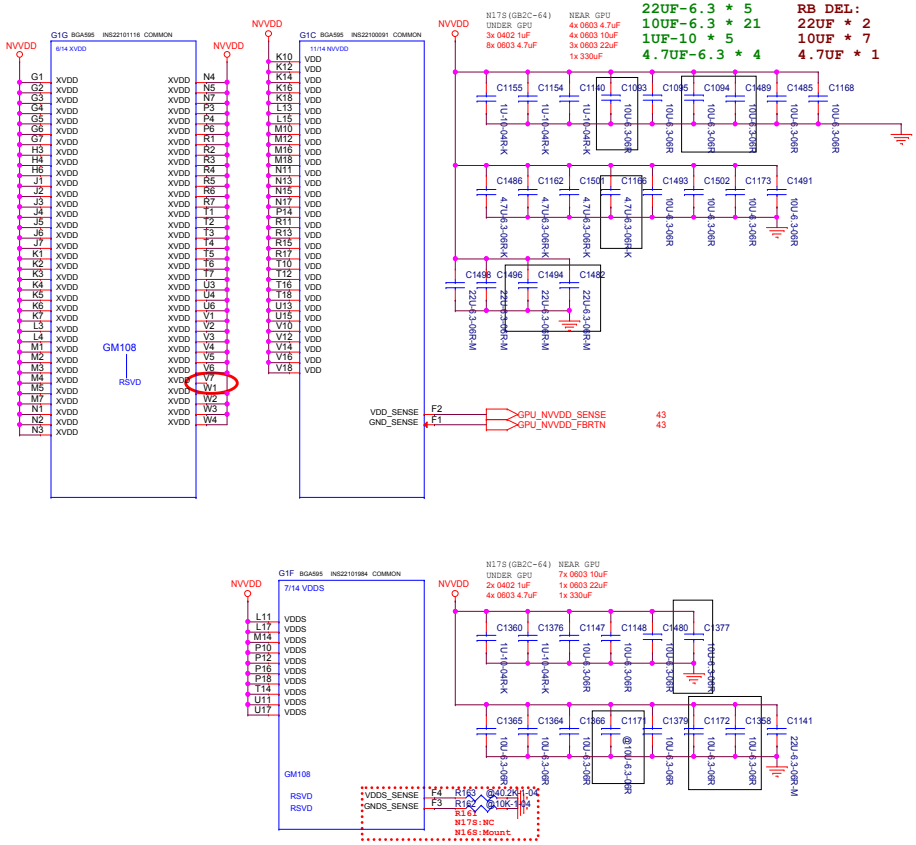
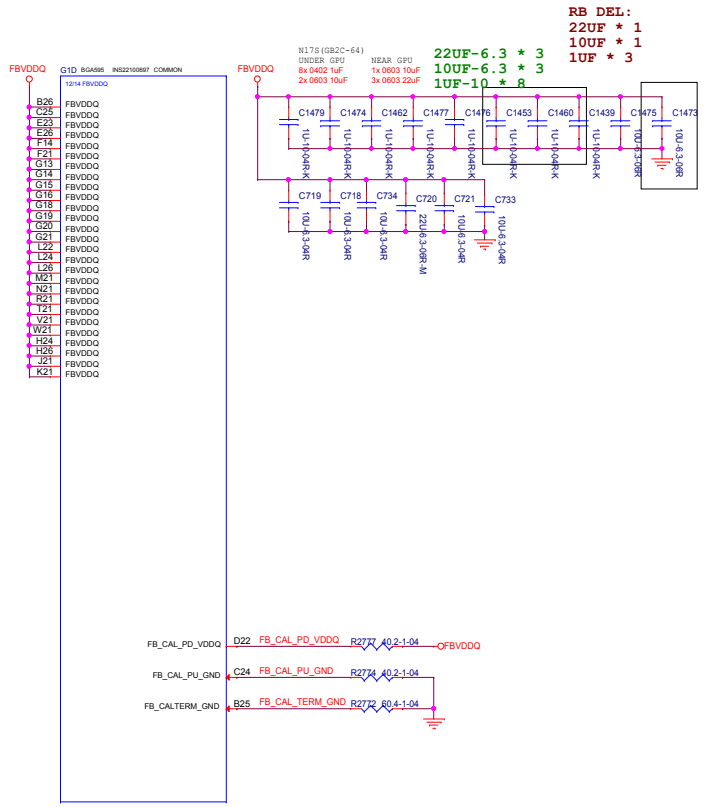
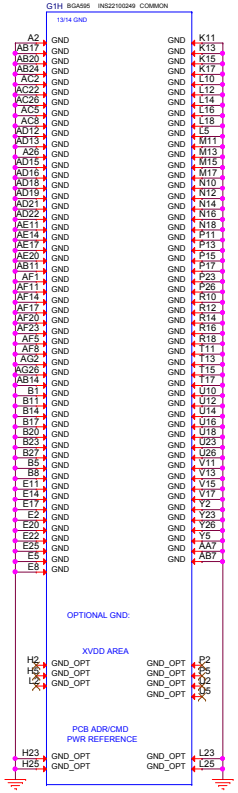
NVVDD



FBVDDQ

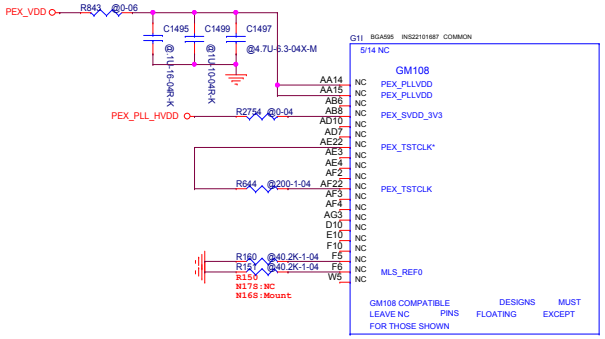


GND

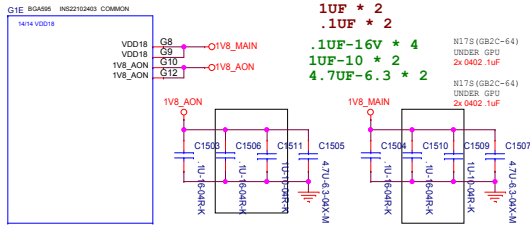


PEX_PLLVDD

N17S: NC
N16S: Mount



1V8_AON/1V8_MAIN



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Title	DECOUPLING CAP	
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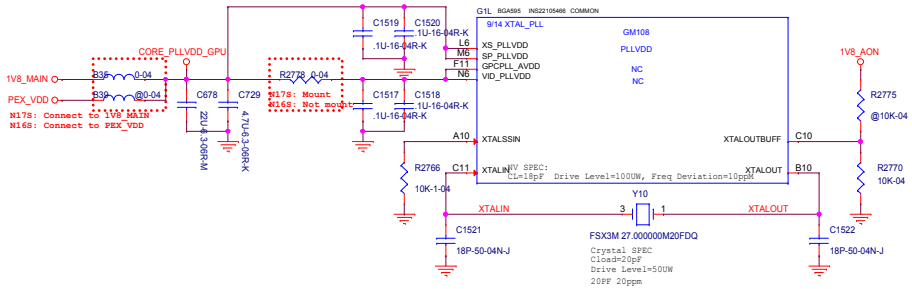


STRAP PIN	Strap 5	Strap 4	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	STRAP5
N17S HIGH	100K	100K	100K	Optional	Optional	Optional	NA	NA	NA
N17S LOW	NA	NA	100K				100K	100K	100K
N16S HIGH	NA	Optional	NA	49.9K	NA	NA	NA	NA	NA
N16S LOW	4.99K		4.99K	NA	NA	NA	NA	NA	NA

GDDR5 3.0G							
Density	Vendor	Part Number	Die	Strap	Strap2	Strap1	Strap0
8GB	Samsung	K4G80325FC-HC25	C-die	0X3	L	H	H
8GB	Micron	MT51J256M32HF-80	B-die	0X4	H	L	L
8GB	Hynix	H5GC8H24AJR-R2C	A-die	0X5	H	L	H

	Voltage(V)		
LEVEL	Min	Normal	Max
H	1.5	1.8	1.854
M	0.5	0.9	1.3
L	0	0	0.3
Invalid	1.3V<pin voltage<1.5V		
	0.3V<pin voltage<0.5V		

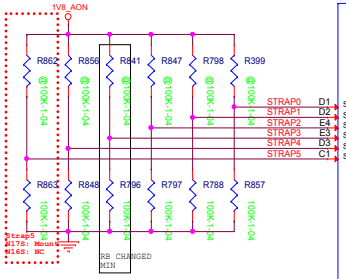
Strap5,4,3 LLH

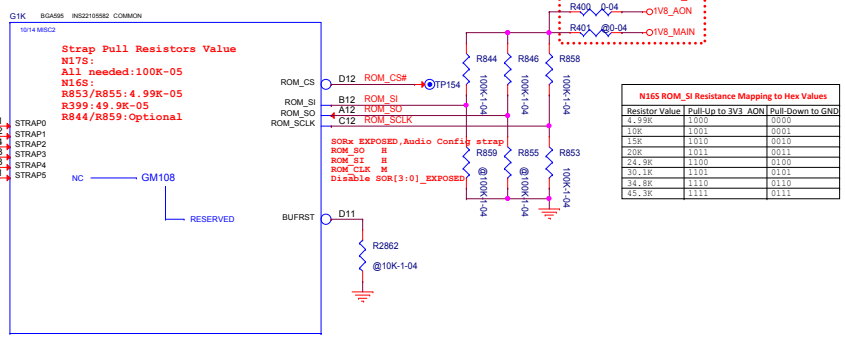
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE(Select)

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL(Select)

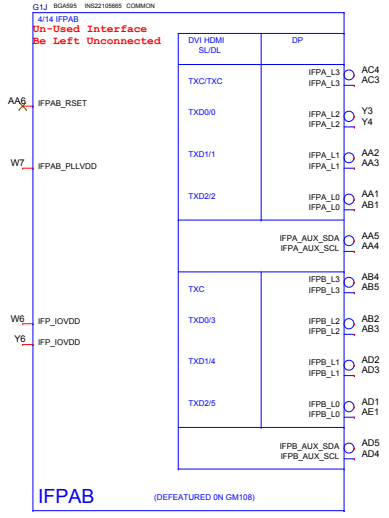
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER(Select)

1:VGA_DEVICE ENABLE(Select)
0:VGA_DEVICE DISABLE





N16S ROM_SI Resistance Mapping to Hex Values		
Resistor Value	Pull-Up to 3V3_AON	Pull-Down to GND
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111



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Title	XTAL/STRAP/ROM/IPFAB		
Size C	Document Number PF4PN2F		Rev 1.0
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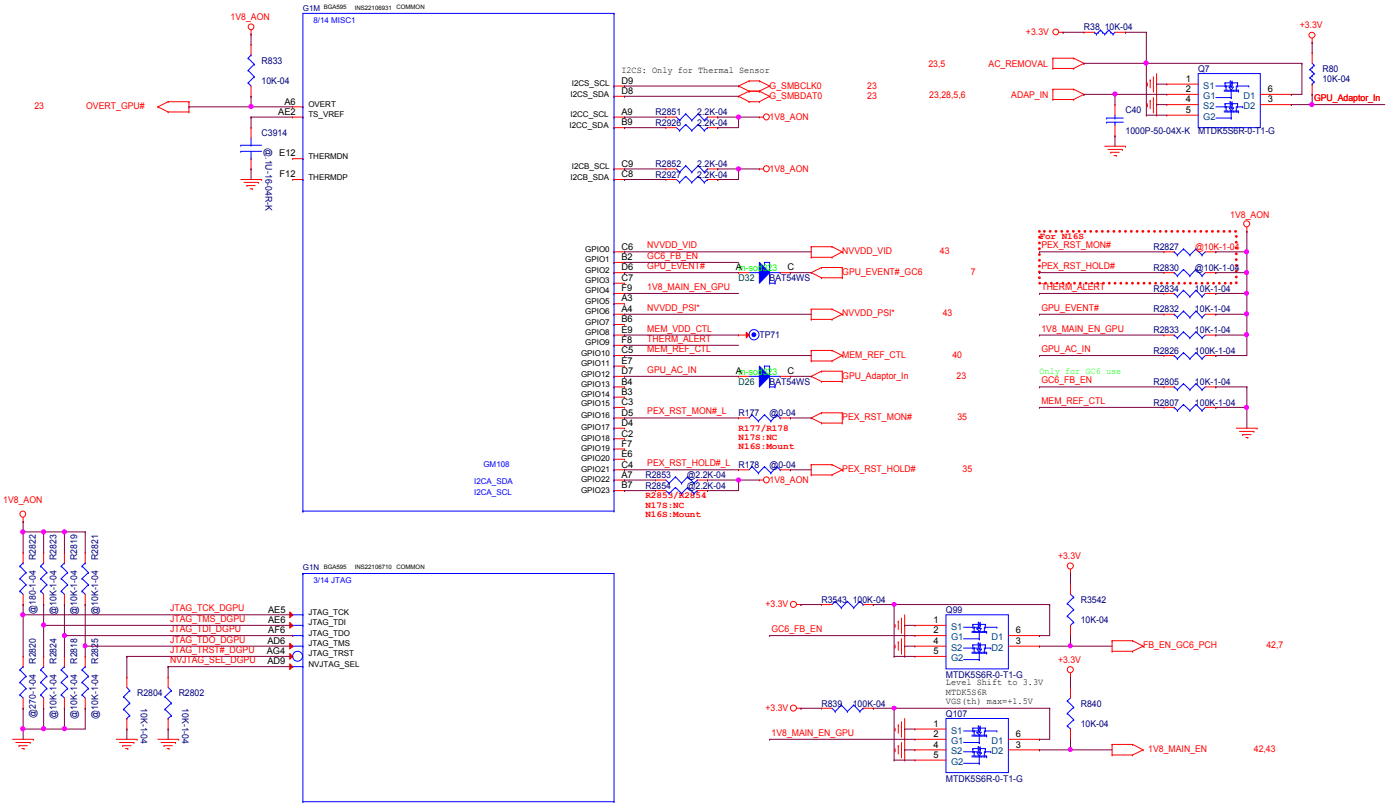
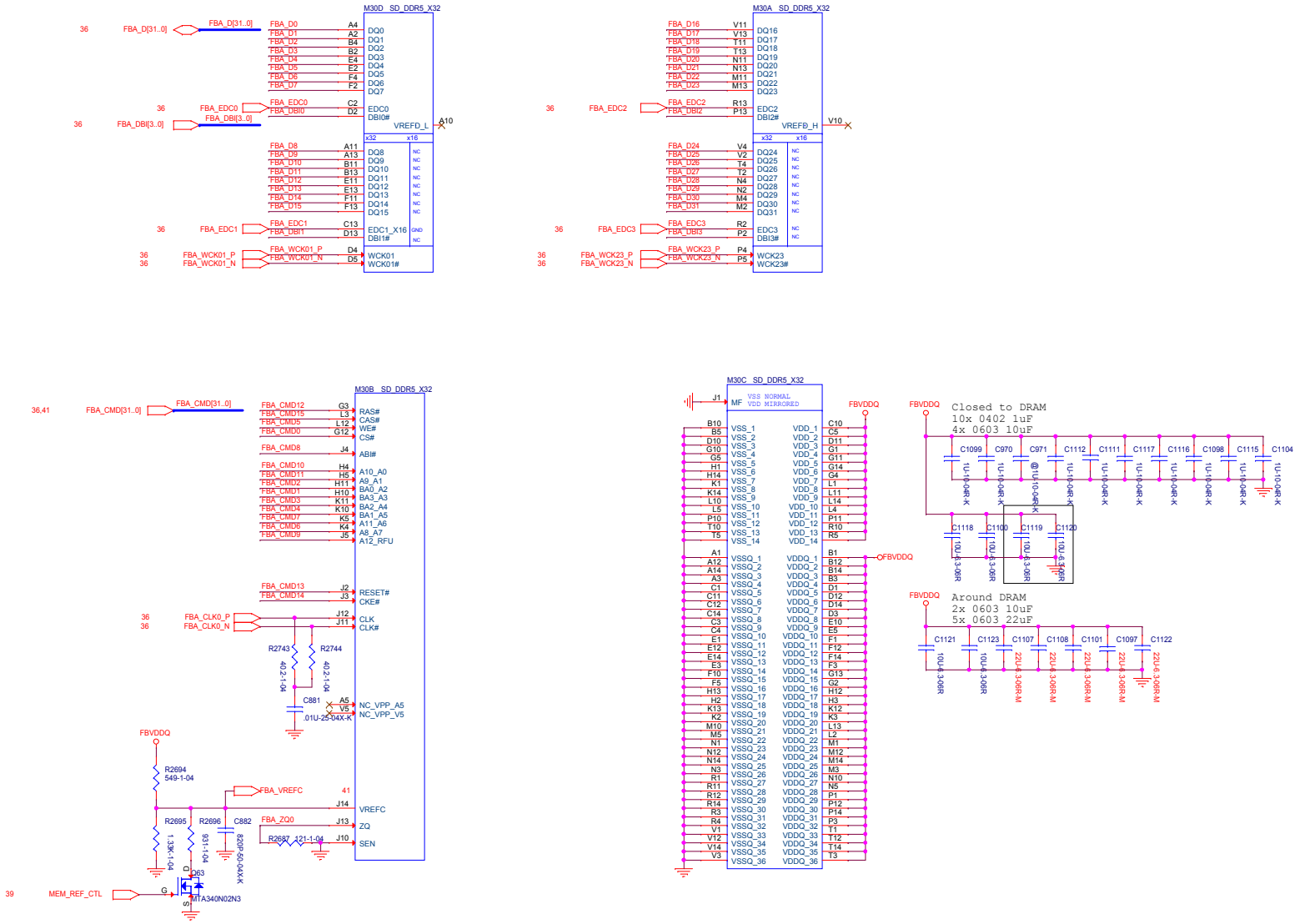


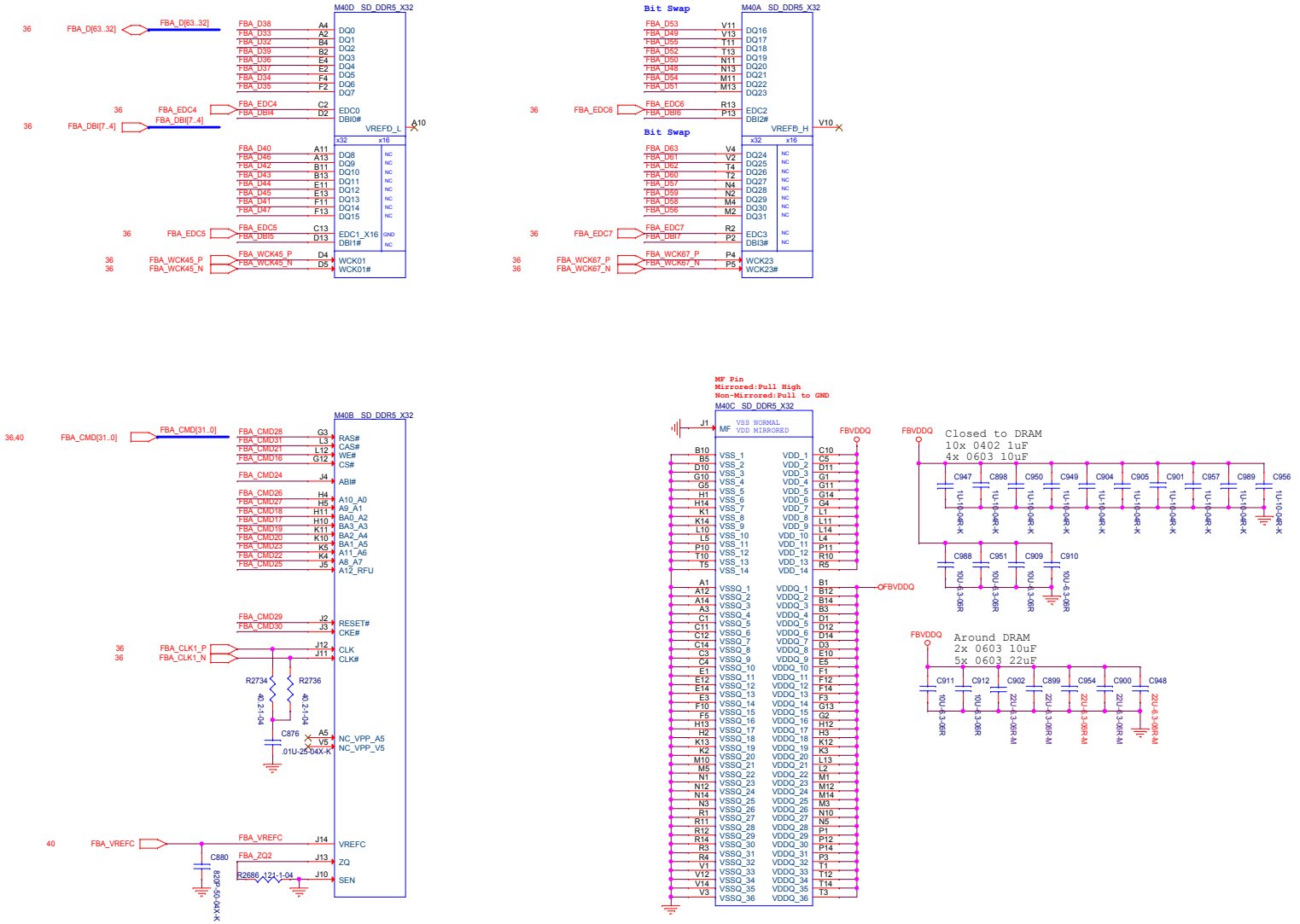
同方国际信息技术有限公司

Title	GPIO/I2C/JTAG	
Size C	Document Number PF4PN2F	Rev 1.0
Date: Tuesday, August 27, 2019	Sheet 39 of 44	



同方国际信息技术有限公司

Title	VRAM1-FRAME BUFFER		
Size C	Document Number PF4PN2F		Rev 1.0
Date: Tuesday, August 27, 2019	Sheet 40 of 44		



同方国际信息技术有限公司			
Title	VRAM2-FRAME BUFFER		
Size C	Document Number PF4PN2F		Rev 1.0
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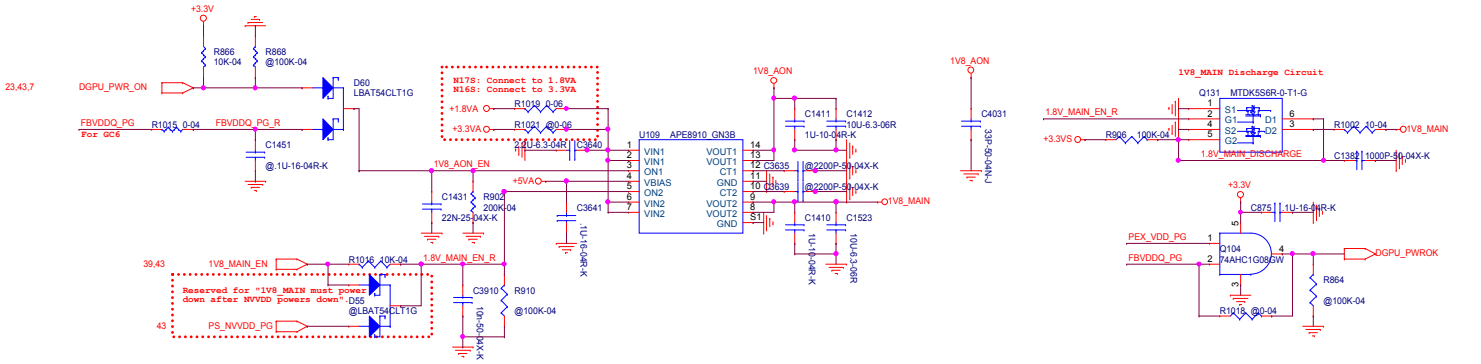
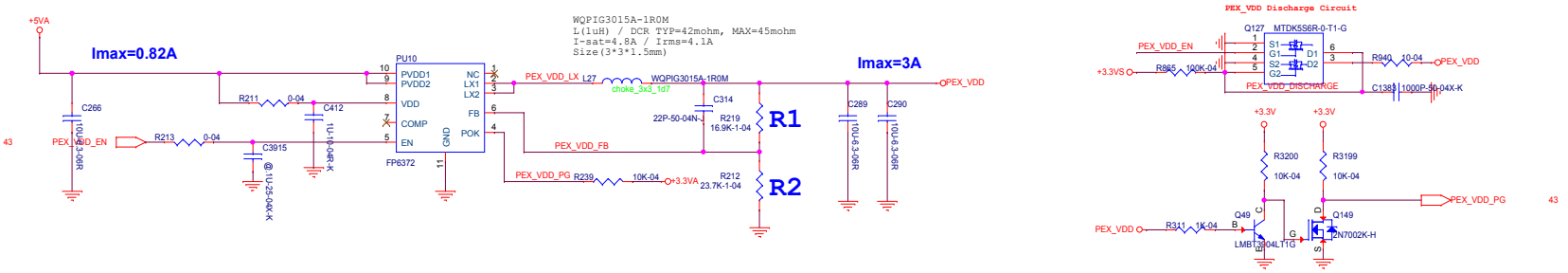
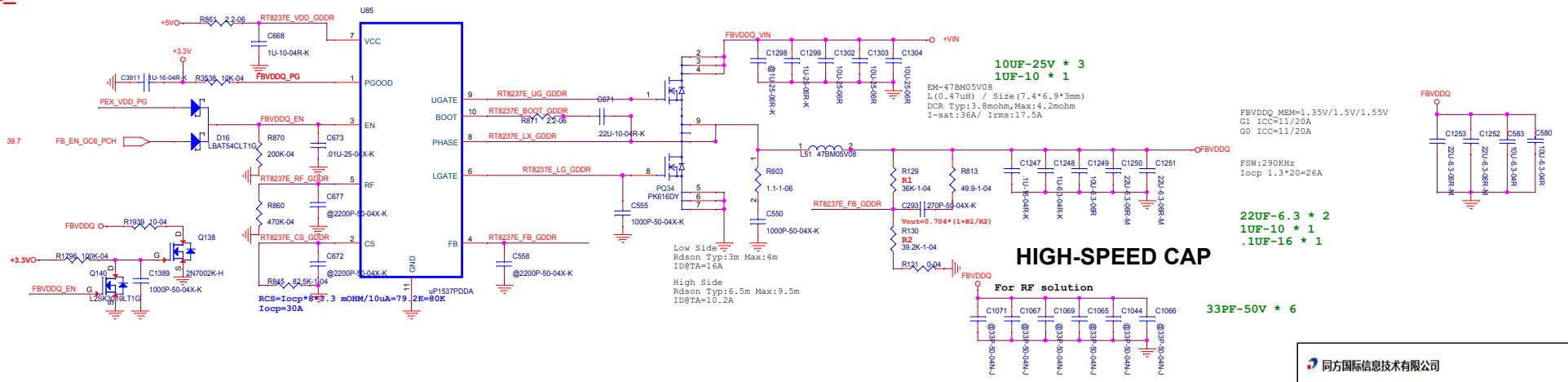
1V8_AON/1V8_MAIN



PEX_VDD



FBVDDQ_MEM



同方国际信息技术有限公司

Title	1V8/PEX_VDD/FBVDDQ	
Size C	Document Number PF4PN2F	Rev 1.0
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UPI 1666 PSI 1.8V 2 Phase CCM mode 1.2V 2 Phase DCM mode 0.6V 1 Phase CCM mode 0V 1 Phase DCM mode	N17S_G1 : 25W + 1.9W N17S_LG: 10W + 1.6W N17S_G1 : NVDD 30A/ 60.1A VRAM: 9.6A /10.3A 1.0V: 0.1A /0.2A 1.8V: 0.3A N17S_LG : NVDD 15.4A /48.3A VRAM: 7.5A/8.6A 1.0V: 0.1A/0.2A 1.8V: 0.2A

High side
Rds(on) TYP:10m MAX:14m
ID@TA=8A

WSRPG0603A-R22M-AG
L(0.22uH) / DCR TYP:2.5mohm, MAX:2.75mohm / I-sat(40A) / Irms(23A)
Size(7.6*6.8*3mm)

Low side
Rds(on) TYP:2.1m MAX:3.8m
ID@TA=17A

10UF-25V * 5
1UF-25 *2

TDC : 30A/60.1A
Vol step:6.25mv
Boot vol:0.8v

22UF-6.3 * 3
10UF-6.3 * 1
.1UF-16 * 1
1UF-6.3 * 2
330UF PS * 2

5/29 added for 1.8main &1.8_AON sequence

同方国际信息技术有限公司			
Title	NVVDD		
Size C	Document Number PF4PN2F		Rev 1.0
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Pre A to A

1. Modify value of R279 to 2.2K-1-04 due to CAPS LOCK LED brightness too strong
2. Modify value of R53 from 560K to 47K and R52 from 73.2K to 6.04K to meet MP8759GD SPEC (+5VA)
3. Del R64/R65/Q9/R63/C73 , and modify value of R55 from 715K to 47K and R56 from 165K to 10K to meet MP8759GD SPEC (+3.3VA)
4. Del PCIE_CLK TP, delete TP1/TP37/TP38/TP39/TP15/TP16/TP21/TP24/TP27/TP28
5. Modify value of Y3 to S3225A-048000-F12-DDB-1BSA for 48MHz
6. Modify value of R454 from 240 to 1K to meet AMD request
7. Del R190 (10K PU PCIE_RST) to meet AMD request
8. Add R514(33) / C717(150P) for PCIE_RST# to meet AMD request
9. Add TP42/TP43/TP44/TP45/TP46/TP47/TP48/TP49/TP50/TP51/TP52/TP53/TP54/TP55/TP56/TP57/TP58 for AMD request
10.Add R515/R516/R517 (0 ohm) for SVC0/SVD0/SVT0 to meet AMD request
11.Modify value of R368 from 1K to 10K for RESET_BUTTON# to meet AMD request
12.Del CNHDD1/C454/C460/C452/R346, due to SPEC changed, and PCIE(7:6) change to PCIE*2+SATA for SSD1
13.Modify value of C327/C329 from 10n to .22u to meet AMD request
14.Del Net SSD2_DEVSLP1 and R522
15.Modify value of R251/R252 from 1K to 2.2K to meet AMD request
16.Del D1 and add ESD11/ESD12/ESD13 to meet AMD request
17.Add R523/R524/C720/C721/C722/C723/C724/C725 for Type-C to meet AMD request
18.Modify value of C1/C2/C684/C685 from .1uF to .22uF for Type-C to meet AMD request
~~19.Modify value of R440 from 10K-04 to @10K-04 to meet AMD request~~
20.Add R525/C726 for LPC_RST# to meet AMD request
21.Add R526/R527/R528/R529 for LPC_ADx to meet AMD request
22.Add R530/R531/C727/C728/C738/C739/C740/C741 for USB3.0 to meet AMD request
23.For SPI changed
    A.Add R545 for SPI_CLK
    B.Swap SPI_SO/SPI_SI, and PU SPI_SO with R275
    C.Unmount R273/R274
24.For EDP changed
    A.Add R559 for LCDVDD_EN and unmount R345 for VIN_LCD_CN enable
    B.Add R560/R561/Q55 for +3.3V_LCD control
    C.Add PS2(SPR-P110-6V-1.1A-0805) for eDP +VIN_LCD_CN by Safety request
25.Add R532/R533/C729/C730 for CCD USB to meet AMD request
26.Add R534/R535/R536/R537/C732/C733/C734/C735 for Audio board USB to meet AMD request
27.Add R538/R539/C736/C737 for USB_HUB USB to meet AMD request
28.Add R540/R541/R542 PU resistor to +3.3VA for USB_OC#
29.Add AR9/AC6 and mount AR5 for CODEC_EAPD
30.Modify value of B18/B19/B20/B21 from BD-HCB2012KF-120 to MBKK2012T4R7M for Audio issue
31.Add R543 between AUDIO_GND and GND_POWER for Audio issue
32.Modify value of R242 from 10K to 8.2K to meet AMD request
33.Add R544 for BATLOW# PU resistor, PU source is +3.3VA to meet AMD request
34.Modify value of R119 from 1.5K to 0 for RTC circuit to meet AMD request
35.Del GPU / H11/H15/H16 and add HDT connector, and Change HDT power source from +1.8V to +1.8VA
36.Add Net name APU_VDDCR_VSS_SENSE for VSS_SENSE_A / APU_VDDP_VSS_SENSE for VSS_SENSE_B
37.Del DIMM1 function
38.For Sequence
    A.Unmount C681/C682
    B.Modify value of R180 from 10K to 4.7K and C233 from @.47uF to 1uF for sequence
    C.Reserve C750 for ALL_PG
    D.Del R293 and add R297/C751 for APU CORE POWER enable, and change enable source from 1.0V_PG to +3.3V
    E.Modify value of R575 from 0-04 to @0-04 and add PU1 enable source SLP_S3# via R576(0-04), and reserve C752
    F.Modify value of R226 from 10K-04 to 0-04 and change PU7 enable source to SLP_S3# via R226 or source to RUN_ON via R585 for 1.8V
    G.Modify value of R180 from 4.7K-04 to 0-04 and unmount C233 and change PU7 enable source to SLP_S3# or source to RUN_ON via R584 for 0.9V
    H.Modify value of R478 from 0-04 to 10K-04 and mount C683
    I.Del U14 and 1.8V change to PU7
    J.Reserve ALL_PG_EC(EC) / SLP_S3# to control ALL_PG via D24/R586/R587
    K.Modify value of R133 from 10K to 22K , and PU to +1.8VA, and add C731/D23/R588 for RSMRST# for sequence
39.Del NET SYS_PWROK and remove Q23/R350/R424
40.Del R7-R14 to meet AMD SPEC
41.For TPM
    A.Let pin 29 floating, VSS/VCC change to +1.8VA
    B.SPI_TPM_CS# PU +1.8VA via R547
    C.TPM_PIRQ# PU to +1.8V
    D.SWAP SI & SO for TPM
    E.Add Q58/R214/R591 for TPM_PIRQ# level shift
42.Del R245/R246 replace C742/C743 ; del R243/R244 replace C744/C745 for symbol error
43.Modify value of R257 from 10M to 20M for X32 to meet AMD request
44.Modify value of R256 from 200K to 1M for X48 to meet AMD request
45.Modify value of R386 from 22 to 0, and unmount C547
46.Net APU_RST PU+1.8V via R548
47.Del R263/R264/R289/R211/R366/R262 for HDT to mee AMD request
48.Modify value of R365/R363 from 2.2K to 4.7K to meet AMD request
49.Move the JP1 to U21 output to meet AMD request
50.Modify value of R195 from 22K to 33K / R191 from 32.4K to 63.4K / R196 & R189 from @0 to 10 for Output 0.9VA
51.Swap SSD1 & WLAN CLK/CLK_REQ fo meet AMD request
52.ADD U22/U23/R549/R550/R551/R552 for APU_RST/APU_PWROK buffer to meet AMD request
53.Modify C642 of value from @PS-330U-2V to @10U-6.3-06R for layout spacing
54.Add R553/554/R555/R556 for Charger sense
55.Add Q54/R558/C746/R431/R557 for THERMTRIP HW control
56.For EC changed
    A.Change the AVCC pin to +3.3VA_EC_LDO
    B.Add R562/R563 for SPI power and PU power source selection(+3.3VA_EC/+3.3VA)
    C.Add R564 for 3.3VA_EN
    D.Change 5VA_PG for 3.3VA_EC enable via R82
    E.Add R565 0-06 between +3.3VA_EC_LDO and +3.3VA_EC
    F.Add R566 @0-06 between +3.3VA and +3.3VA_EC
57.Add Q57/R567/C747/Q56/R568/C748/R569/C749 for Power board LED used
58.Add Q27/R570/R571 for UART debug level shift.
59.For SIC/SID/ALERT_L
    A.Del R212/R213/R221/R222, add TP59/TP60 for I2C3
    B.Connect SIC to EC pin115 / SID to EC pin116 / ALERT_L to EC pin95
    C.Add R572/R573/R574(1K) for SIC/SID/ALERT_L PU to +3.3V
60.Change EC_ROM Net from SPI_HOLD# to SPI_HOLD#_EC & from SPI_WP# to SPI_WP#_EC
61.Modify value of C4 from 10n to 4700P
62.Del PEX_VDD and PEX_VDD_PG and discharge circuit, move 1.8V_PG to Q45
63.Del R375 to meet AMD request
64.Change HDMI CLK/DATA/HPD level shift power source from +1.8V to +3.3V
65.Del Q7/D5/R58/C52/R51/R59/R61/Q8/Q37/R288/R277 due to no discharge request.
66.Add R577 for ESPI_ALERT_L PU to +3.3V to meet AMD request
67.Modify value of R423 from 0 to 22, and unmount C118
68. For USB
    A. SWAP USB 2.0 port between USB2_CCD and USB2_SIO2
    B.USB HUB port 2 change to connected to CNMSD1 & CNAUDIO1 for SD function, switch by R599/R600 & R601/R602
    C.USB HUB port 1 change to connected to ANAUDIO1 for USB2.0 function.
    D.USB_0_DP(M)3 connected to TypeC, and addC753/C754/R604/R603/L26/R606/R605
    E.Modify ESD10 value from ESD5302N to AZ1045-04F and connected to USB2_TYPEC_3_DP_L & USB2_TYPEC_3_DN_L
69.For I2C
    A.Del TP55/TP56/TP57/TP58/TP59/TP60
    B.Add R578/R579 for I2C3 PU +3.3VA
    C.Add R580/R581/R582/R583 for I2C(1:0) PU to +1.8VA
70.For +1.0VA
    A.Mount C253 to meet low output power SPEC
    B.Modify value of C242 from .47u to 1u
71.For +1.2VS_DDR/+2.5VS/+0.6V_VTT
    A.Reserve R590(0) for EN1
    B.Modify value of C208 from .47u to 1u
    C.Del D12, and remove EC_SUS_ON and SUS_ON_S5#
    D.Modify value of R148 from 100K to 0
72.Del C314/R280, and add R589, modify value of R276 from 100K to 1K , and change Q34 from 2N7002 to MTDK5S6R-0-T1-G for KB BL PWM feature.
73.For +5VA
    A.Modify value of C51 from .47u to 1u
    B.5VA_PG PH power source change from +5VA to PU2 pin VCC
    C.Modify value of C29 from @.1u to 1000P
    D.Unmount C716
74.For +3.3VA
    A.Modify value of R57 from 3.9 to 0
    B.Modify value of C60 from .47u to 1u
75.Add R592/R593 and SSD1 PEDET PU +3.3V via R592 to +3.3V and connected to AGPIO68 via R593 for SSD1
76.Reserve R594 and SSD2 PEDET PU +3.3V via R594 for SSD2
77.SWAP HDMI between 0 and 2
78.Net MEM_OVERCLK_EN and R250 move from APU pin BD18 to EC pin 29
79.Change NET TP_INT# from APU pin AP6 to AP9, and reserve R597
80.APU USB_OC5_L PU +3.3VA via R595
81.AGPIO40 PU +3.3VA via R596 and del TP40
82.PCIE_RST1# PU +3.3VA via R598(10K) and del TP41 to meet AMD request
83.Unmount C188
84.For LAN
    A.SWAP PCIE3_LAN_TXP / PCIE3_LAN_TXN
    B.Modify value of C301/C302 from .1U to .22U
85.SSD1_DEVSLP0 change to SSD1_DEVSLP1 and connected to APU DEVSLP1
86.LPC_PD# PU +3.3V via R607(10K)
87.CLK_REQ5# PU +3.3V via R608(10K)
88. Add TP55 for U13 pin26, and reserve PU R609 to +3.3VA for U13 pin20
89.Modify value of Y2 from S3225A to 12M-20-30-FUJ
90.For PCIE SPEC change
    A.WIFI PCIE change to GPP0
    B.LAN PCIE change to GPP1
    C.SSD2 PCIE change to GPP2/3 colay GPP4/5
    D.Add R610-R633 for Colay optional
91.Del PJP4 / PJP6
92.Reserve D25 and add SSD1_WAKE#/SSD2_WAKE# for PCIE_WAKE#
93.SPI_CS2# PU R634(10K) to +1.8VA
94.Add C755 for PWR board +3.3V
95.Del R390/R360 due to have another resistor on PWM side.
96.Add C756/C757/C758/C759/C760/C761 for VIN_CPU
97.Add R643 to PU +3.3VA_EC for GDPU_PWR_ON always high
98.Modify H2/H9/H12/H13/H1/H8 footprint to meet DXF
99.Modify value of C190 from .47U to 1000P
100.BOM change for sequence: Unmount R566,R576,R180,R226 ; Mount R575,R584,R585,Q32
101.BOM change for USB2: Unmount C732/C733 and modify value of R534/R535 from 15 to 0
102.BOM change for speaker: Modify value of B18/B19/B20/B21 from MBKK2012T4R7M to MBKK2012T1R0M
103. BOM change for +5VA/+3.3VA mode selection: Mount R500/R503
104.BOM change for speaker: Modify value of B18/B19/B20/B21 from MBKK2012T1R0M to MBKK2012T4R7M due to sourcer request

A to B

1. Del R517 due to PWR control IC have reserve 0 ohm
2. Let APU SIC/APU_SID connect to O2 PWR controller, and reserve TP56/TP57 for PSA I2C
3. Reserve R646/R647 for +0.9VA APU_VDDP_FB_H/L, and del R196/R189 to fix +0.9VA leakage
4. Modify value of L13 from 47AM47V01 to EM-33AM02V01 due to charger current change to 3.5A
5. Q32 change plancement to +VDDBT_RTC (U21 output) to reach EC reset RTC feature
6. Add Q59/R649/R648 for RSMRST# sequence
7. Reverse CNLB1 pindefine to fix Hall Sensor issue
8. Add C762/C763 for USB3_SIO2_TX
9. Modify screws to mapping PF4WN, and add 2 screw H19/H20 for PF4PU CPU used
10.Del H14/H16 due to CPU screws no follow WN
11.Modify C696/C703/C704 package from 0604 to 0402 due to layout spacing.
12.Del C736/C737/R538/R539/C732/C733/R534/R535/C734/C735/R536/R537/C727/C728/R531/R530/C753/C754/R603/R604/C720/C721/R523/R524/C729/C730/R532/R533 due to USB2.0 no need to meet AMD SPEC (AMD conform)
13.Tvs1/Tvs2 swap pin due to layout request
14.Modify value of CNSSD1 from M2,67P,SMT,P0.5,NASM0-S6701-TS40,ARG to M2,67P,SMT,P0.5,NASM0-S6701-TS due to MCJ request
15.Jumper change to shortpad
16.Modify value of R304 from 953-1-04 to 3.01K-1-04 / R306 from 2.32K-1-04 to 8.87K-1-04 / R305 from 1.21K-1-04 to 1.74K-1-04 / R307 from 2.87K-1-04 to 3.83K-1-04 for APU Power performance
17.Modify value of C258/C259 from 15P to 33P due to the crystal vender suggestion
18.Modify footprint of CNDCIN1 from CON_DCIN_WO_2DC3061-025111F_SIN to CON_DCIN_WO_2DC3061-0251_NL_SIN
19.Modify footprint of CNHDMI1 from CON_HDMI-A-R_C128R7-X19XX_ATP to CON_HDMI-A-R_C128R7-K193_NL_ATP
20.Modify footprint of CN1 from CON_SUSB_3SR_C190AG-90939-L_ATP to CON_SUSB_3SR_C190AG-9093_NL_ATP
21.Unmount C731 due to sequence
~~22.Unmount CNDEG2 fro B phase Ass'y~~
23.For 144MHz LCD
    A. Modify value of B10 from BD-HCB1608KF-300T30 to BD-HCB2012KF-120
    B. Add Q60/R650 to reduce RDS on
24.EC pin81(EC_WP#) connect to SPI_WP#_EC via R651 (0-04)
25.Modify value of C39/C42/C44/C54/C55/C56 from 10uF to 22uF for +3.3VA & +5VA output
26.Modify value of R204 from 680 to 620 to fix USB2.0 SI test result
27.For LCD sequence
    A.Modify value of R560 from 0-04 to 220K
    B.Add C764
    C.Modify value of C448 from .47uF to 1uF
28.Add R652 shortpad for VDDCORE FB
29.Add Q61/R653/R654 for +3.3V discharge
30.Modify value of B18/B21 from MBKK2012T4R7M to MBKK2012T1R0M
31.For USB HUB
    A. Add R655/R656 for co-lay CNAUDIO1 card reader and Finger Printer
    B. Add R657/R658 for co-lay CNMSD1 car reader and Finger Printer
    C. Change Page 8 USB2.0 table and Block Diagram
32.Add Q62/R659/Net SUS_PWR_ON# for +3.3VS function
33.C755 change power source from +3.3V to +3.3VS
34.Net KB_BLPWN PU change to PD by R462
35.Modify value of C691/C686/C690 from 1U-25-06R-K to 10U-50 , and add C765, another C766 for reserve
36.Modify footprint of H15/H19/H20 from @holect355b177d177 to @holect210b355d190 due to PF5 ME request
37.Add R660 shortpad for VDDSOC FB
38.Reserve R661 between Codec GND and AUDIO GND
39.Add R662/R663 for +VCHG_OUT_SEN and +VCHG_SEN due to layout request
40.For charge battery waveform unstable issue
    A.Unmount C697/C686
    B Modify value of C691/C690/C765 from 10u to 1u
    C.Mount C766 (1uF)
    D.Modify value of C708 from 1uF to 10uF
41.Unmount R369 and mount R367 for HDMI audio output issue
42.Modify value of R306 from 8.87K to 13K due to APU power setting
43.Unmount R386 due to WLAN SPEC no need SUSCLK
44.Modify value of R53 from 47K to 46.4K for reduece +5VA from 5.27V to 5.21V

B to B1

1. Change C697/C686 power source from +VCHG_OUT to +VCHG to fix charge wave unstable issue
2. Add U25/ U26 and others symbols for CNTYPEC1 re-driver
3. Add U24 and others symbols for CN1 re-driver
4. Add U27 and others symbols for CNAUDIO1 USB3.0 re-driver
5. Add C791/C792 for USB 3.0 IO RX uesd
6. Mount R661 and unmount R543 to fix audio signal issue
7. Modify value of C722/C723/C724/C725/C740/C741/C791/C792 from .33uF to 0-04 for re-driver output RX
8. Modify value of C1/C2/C684/C685/C738/C739/C762/C763 from .22uF to .1uF for re-driver output TX
9. Modify value of C391/C392/C424/C425/C426/C427/C447 from 10uF to 1uF to fix High fequence noise issue
10.Modify value of R306 from 13K to 9.76K for APU setting
11. For +5VA / +3.3VA stable
    a.Mount R498 / C706
    b.Modify value of R512 from 51.1K to 499K
    c.Modify value of C716 from 2200pF to 220pF
~~12. For APU power controller setting~~
    ~~a.Modify value of R304 from 3.01K-1-04 to 1.1K-1-04~~
    ~~b.Modify value of R305 from 1.74K-1-04 to 2.1K-1-04~~
    ~~c.Modify value of R307 from 3.83K-1-04 to 5.49K-1-04~~
13.Modify value of C274 from .47uF to 1uF for USB HUB sequence
14.Modify value of R284 from 10K to 0-04
15.Modify value of C101 from .47uF to 1uF

B1 to 1.0

1. Modify value/footprint of H10 from HOLECTOB284X288BOB276X196_D177 to holectob284x288bc276d177 for layout issue
2. Remove JP1 and Add TP_RTC for SMT request
3. Add R719 / R720 for +5VA_FB_R / +3.3VA_FB_R layout request
4. Add R721 / R722 for +5VA/+3.3VA mode change
5. Modify value/footprint of R565 from 0-06 to 0-04 due to spacing risk
6. Modify valuie of C101 from .47uF to 1uF due to S3 become S5 when DC mode
7. Del R38/Q3 and add U28 for HDMI HPD issue
8. Unmount Q54 to fix S3 become S5 when DC mode
9. For APU power controller IC setting
    A. Del R311/R313/R314
    B. Modify value of R310/R318 from 2.2-06 to 0-06
    C. Modify value of R304 from 3.01K to 2.49K-1-04
    D. Modify value of R305 from 1.74K to 1.5K-1-04
10. Modify value of C259 from 15P to 33P due to fix 12MHz crystal SPEC
11. Modify value of C391/C392/C424/C425/C426/C427 from 1uF to 10uF for APU power stable
12.For AC mode high frequence noise issue
    A.Modify value of R721/R722 from 0-04 to 10K-1-04
    B.Mount R504/R501 (10K-1-04)
    C.Unmount R503/R500
13.Unmount R54 to fix meet Safety request
14.Unmount CNDEG1/CNDEG2/CNFP1
15.Modify value of B19/B20 from MBKK2012T4R7M to MBKK2012T1R0M due to sourcer request
16.Reduce +3.3VS pulse
    ~~A.Modify value of C767/C773/C775/C785 from 4.7u to .1U-50-06X-K~~
    B.Modify value of C755 from 1U-10-04R-K to .1U-16-04R-K
    C.Modify value of R659 from 100K to 10n
17.Modify value of C24/C25/C27 from 10uF to 22uF
18.Mount C22/C642/C657 for 22uF
19.Mount C263/C264 for 0.1uF
20.For USB HUB
    A.Modify value of R204 from 620 to 487-1-04
    B.Modify value of C263/C264 from .1uF to 2.2uF
21.Modify value of R665/R691/R703 from 2K to 1.8K-1-04 to improve rederiver driving strength
22.Mount R667/R679/R685 to set the redriver TX +3dB
23.Unmount Q13/Q18/D19 to disable prochot function
24.For symbol damage risk
    A.Modify value of C662 / C666 / C696 from 4.7u to 2.2u
    B.Mount C663 for 2.2u
    C.Modify value of C694 from .1u to 2.2u
    D.Modify R497 from 0-06 to 0-04
25.Modify value of PS2 from SPR-P110-6V-1.1A-0805 to SPR-P260T
26.Mount ESD12 for HDMI issue
27.Modify value of R195 from 33K to 34.8K-1-04 and R191 from 63.4K to 56.2K-1-04 for +0.9VA change to +0.97VA
28.Modify value of L20/L21 from WSRPG0603-R36M-BG to EM-36BM52V01 for change source

1.0 to 1.1

1. Add R723 for SUS_PWR_ON#
2. Add C793 / C794 for +5VA_USB_MBIO