GA-78LMT-S2PT

Revision : 3.1

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Model Name:GA-78LMT-S2PT

Component value change history

Version: 3.1

P-Code: U11120-0

Date	Change Item		Reason
2011.10.25	3.1A E_BOM Release.	PCB: 3.1	Modify from 78LMT-S2P 4.0, Remove DVI, Add LPT,IDE, COM PH 改 CONN to back panel
2011.12.28	3.1B P_BOM Release.	PCB: 3.1	ACN1~2 , PCN1~4 , PC2 180p Cap for HCL requirements

Circuit or PCB layout change for next version

Date	Version	Change Item
2011.10.25	3.1 Gerber out	Modify from 78LMT-S2P 4.0. Remove DVI, Add LPT,IDE, COM PH 改 CONN to back, (RS760=RS780L) ~~SIO/LAN /F_PANEL /F_USB/VGA~~ relocate

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Title	BOM & PCB HISTORY	
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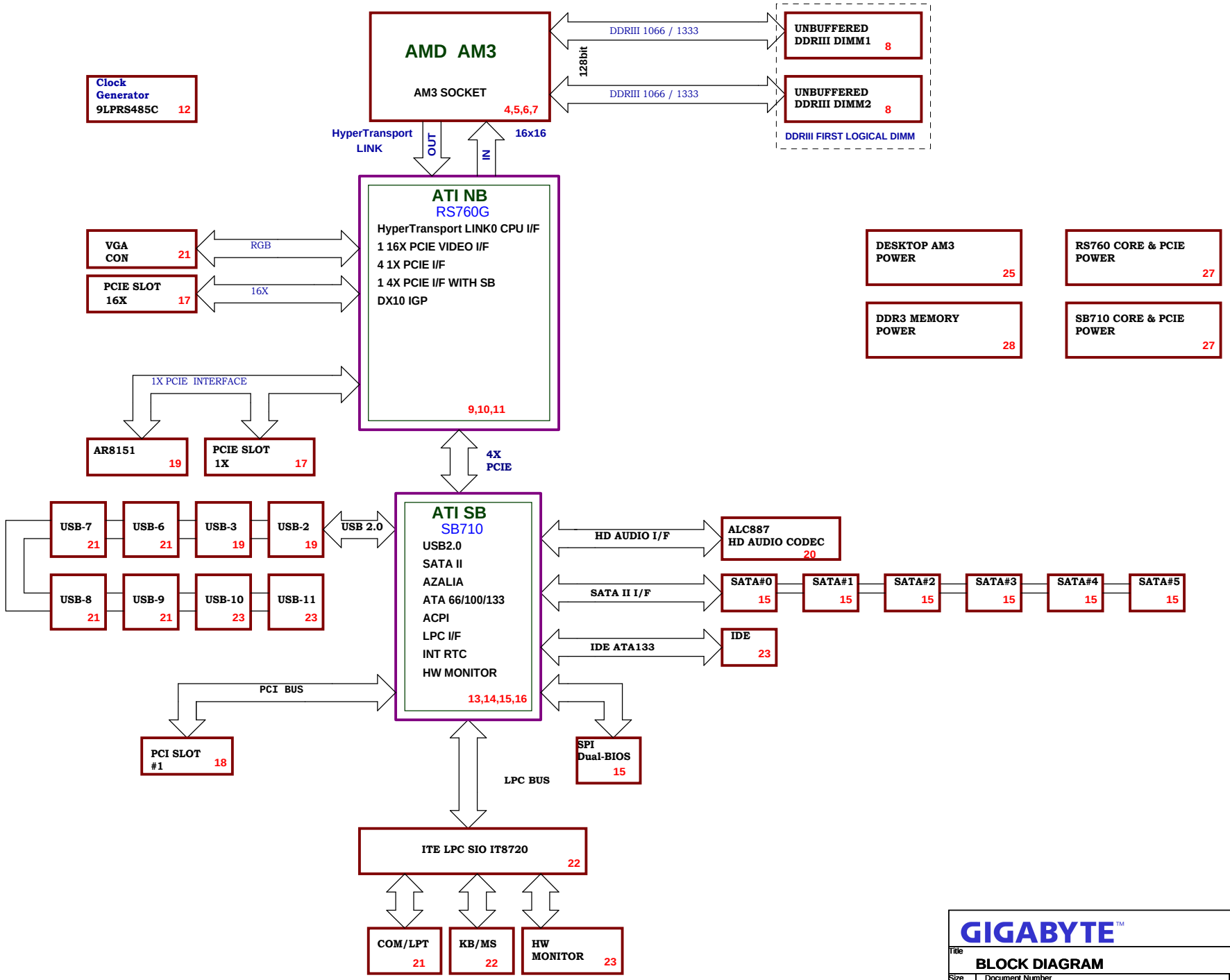
RS780L CUSTOMER DESKTOP DESIGN



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Title: BLOCK DIAGRAM		
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L0_CADIN_L[0..15] L0_CADIN_L[0..15] <9>
L0_CADIN_H[0..15] L0_CADIN_H[0..15] <9>

L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] <9>
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] <9>

M2CPUA

HYPERTRANSPORT

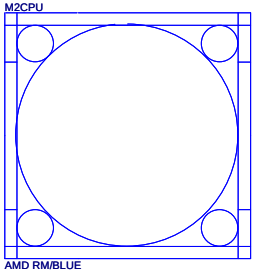
<9> L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1 <9>
<9> L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1 <9>
<9> L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0 <9>
<9> L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0 <9>
<9> L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1 <9>
<9> L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1 <9>
<9> L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0 <9>
<9> L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0 <9>
	L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15	
	L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15	
	L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14	
	L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14	
	L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13	
	L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13	
	L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12	
	L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12	
	L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AF6	L0_CADOUT_H11	
	L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11	
	L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AE5	L0_CADOUT_H10	
	L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10	
	L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9	
	L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9	
	L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8	
	L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8	
	L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7	
	L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7	
	L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6	
	L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6	
	L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5	
	L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5	
	L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4	
	L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4	
	L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3	
	L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3	
	L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2	
	L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2	
	L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1	
	L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1	
	L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0	
	L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0	

CPU-SK/941AM3/S/15u/[10SC1-A01942-01R_10SC1-A01942-02R]

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPU



AMD RM/BLUE

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Title	CPU HYPER TRANSPORT	
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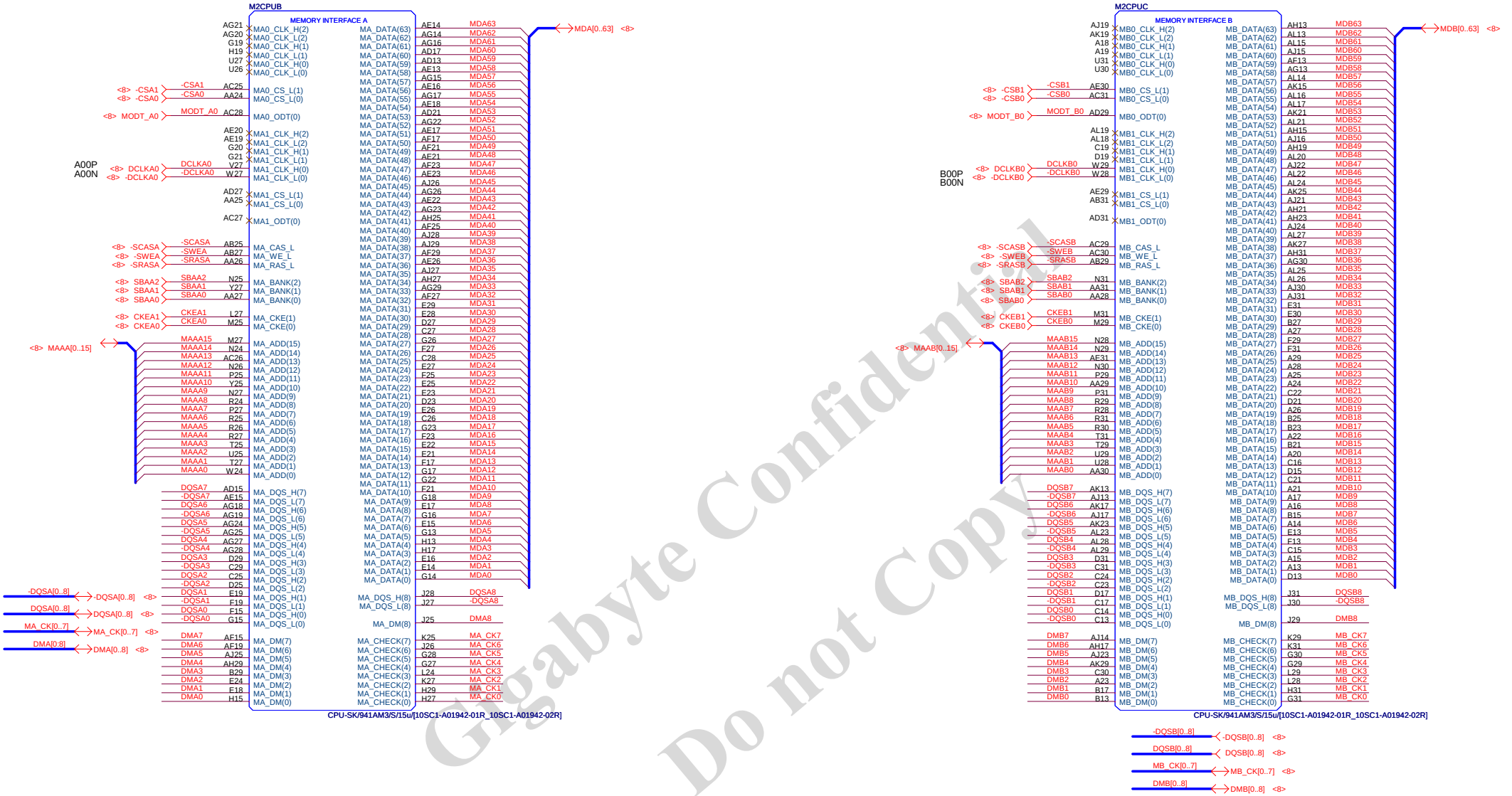

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Title	CPU DDRII MEMORY	
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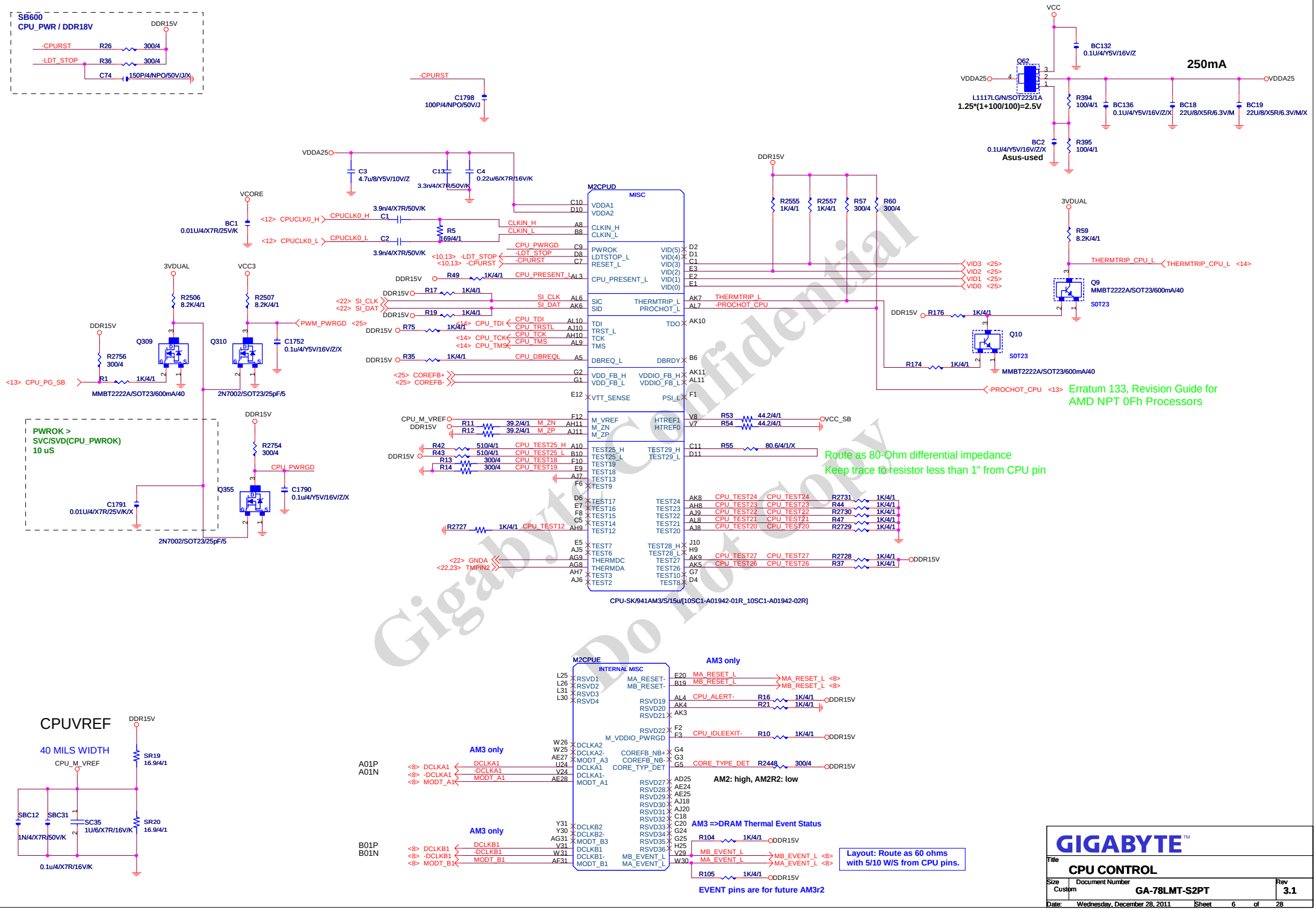
SB600
CPU_PWR / DDR18V
DDR15V
-CPURST
R26
300/4
-LDT_STOP
R36
300/4
C74
150P/4/NPO/50V/J/X
-CPURST
C1798
100P4/NPO/50V/J
VCC
BC132
0.1U/4/Y5V/16V/Z
Q62
250mA
VDDA25
L1117LG/N/SOT223/1A
1.25*(1+100/100)=2.5V
R394
100/4/1
BC136
0.1U/4/Y5V/16V/Z/X
BC18
22U/8/X5R/6.3V/M
BC19
22U/8/X5R/6.3V/M/X
BC2
0.1U/4/Y5V/16V/Z/X
Asus-used
R395
100/4/1
VDDA25
C3
4.7u/8/Y5V/10V/Z
C13
3.3n/4/X7R/50V/K
C4
0.22u/6/X7R/16V/K
VCORE
BC1
0.01U/4/X7R/25V/K
3.9n/4/X7R/50V/K
C1
C2
3.9n/4/X7R/50V/K
R5
169/4/1
<12> CPUCLK0_H
CPUCLK0_H
<12> CPUCLK0_L
CPUCLK0_L
M2CPUD
MISC
C10
D10
VDDA1
VDDA2
CLKIN_H
CLKIN_L
A8
B8
CPU_PWRGD
-LDT_STOP
-CPURST
PWROK
LDTSTOP_L
RESET_L
<10,13> -LDT_STOP
<10,13> -CPURST
C9
D8
C7
DDR15V
R49
1K/4/1
CPU_PRESENT_L
AL3
CPU_PRESENT_L
R17
1K/4/1
SI_CLK
SI_DAT
<22> SI_CLK
<22> SI_DAT
AL6
AK6
SIC
SID
R19
1K/4/1
THERMTRIP_L
PROCHOT_L
AK7
AL7
THERMTRIP_L
-PROCHOT_CPU
R75
1K/4/1
CPU_TDI
CPU_TRSTL
CPU_TCK
CPU_TMS
<14> CPU_TDI
<14> CPU_TCK
<14> CPU_TMS
AL10
AJ10
AH10
AL9
TDI
TRST_L
TCK
TMS
TDO
AK10
R35
1K/4/1
CPU_DBREQL
A5
DBREQ_L
DBRDY
B6
<25> COREFB+
<25> COREFB-
G2
G1
VDD_FB_H
VDD_FB_L
VDDIO_FB_H
VDDIO_FB_L
AK11
AL11
E12
VTT_SENSE
PSI_L
F1
CPU_M_VREF
R11
39.2/4/1
M_ZN
R12
39.2/4/1
M_ZP
F12
AH11
AJ11
M_VREF
M_ZN
M_ZP
HTREF1
HTREF0
V8
V7
R53
44.2/4/1
R54
44.2/4/1
VCC_SB
R42
510/4/1
CPU_TEST25_H
R43
510/4/1
CPU_TEST25_L
R13
300/4
CPU_TEST18
R14
300/4
CPU_TEST19
A10
B10
F10
E9
AJ7
F6
TEST25_H
TEST25_L
TEST19
TEST18
TEST13
TEST9
TEST29_H
TEST29_L
C11
D11
R55
80.6/4/1/X
Route as 80-Ohm differential impedance
Keep trace to resistor less than 1" from CPU pin
R2727
1K/4/1
CPU_TEST12
AH9
TEST12
D6
E7
F8
C5
AH9
TEST17
TEST16
TEST15
TEST14
TEST12
TEST24
TEST23
TEST22
TEST21
TEST20
AK8
AH8
AJ9
AL8
AJ8
CPU_TEST24
CPU_TEST23
CPU_TEST22
CPU_TEST21
CPU_TEST20
R2731
R44
R2730
R47
R2729
1K/4/1
E5
AJ5
AG9
AG8
AH7
AJ6
TEST7
TEST6
THERMDC
THERMDA
TEST3
TEST2
TEST28_H
TEST28_L
TEST27
TEST26
TEST10
TEST8
J10
H9
G7
D4
AK9
AK5
CPU_TEST27
CPU_TEST26
R2728
R37
<22> GNDA
<22,23> TMPIN2
DDR15V
CPU-SK/941AM3/S/15u/[10SC1-A01942-01R_10SC1-A01942-02R]
R2555
1K/4/1
R2557
1K/4/1
R57
300/4
R60
300/4
VID(5)
VID(4)
VID(3)
VID(2)
VID(1)
VID(0)
D2
D1
C1
E3
E2
E1
VID3 <25>
VID2 <25>
VID1 <25>
VID0 <25>
3VDUAL
R59
8.2K/4/1
THERMTRIP_CPU_L
THERMTRIP_CPU_L <14>
Q9
MMBT2222A/SOT23/600mA/40
SOT23
DDR15V
R176
1K/4/1
Q10
SOT23
R174
1K/4/1
MMBT2222A/SOT23/600mA/40
-PROCHOT_CPU <13>
Erratum 133, Revision Guide for
AMD NPT 0Fh Processors
3VDUAL
VCC3
R2506
8.2K/4/1
R2507
8.2K/4/1
PWM_PWRGD <25>
DDR15V
R2756
300/4
<13> CPU_PG_SB
R1
1K/4/1
Q309
Q310
C1752
0.1u/4/Y5V/16V/Z/X
MMBT2222A/SOT23/600mA/40
2N7002/SOT23/25pF/5
PWROK >
SVC/SVD(CPU_PWROK)
10 uS
DDR15V
R2754
300/4
CPU_PWRGD
Q355
C1790
0.1u/4/Y5V/16V/Z/X
C1791
0.01U/4/X7R/25V/K/X
2N7002/SOT23/25pF/5
M2CPUE
INTERNAL MISC
AM3 only
L25
L26
L31
L30
RSVD1
RSVD2
RSVD3
RSVD4
MA_RESET-
MB_RESET-
E20
B19
MA_RESET_L
MB_RESET_L
MA_RESET_L <8>
MB_RESET_L <8>
RSVD19
RSVD20
RSVD21
AL4
AK4
AK3
CPU_ALERT-
R16
1K/4/1
R21
1K/4/1
DDR15V
RSVD22
M_VDDIO_PWRGD
F2
F3
CPU_IDLEEXIT-
R10
1K/4/1
DDR15V
W26
W25
AE27
V24
AE28
DCLKA2
DCLKA2-
MODT_A3
DCLKA1
DCLKA1-
MODT_A1
COREFB_NB+
COREFB_NB-
CORE_TYP_DET
G4
G3
G5
CORE_TYPE_DET
R2448
300/4
DDR15V
A01P
A01N
AM3 only
<8> DCLKA1
<8> -DCLKA1
<8> MODT_A1
DCLKA1
-DCLKA1
MODT_A1
AM2: high, AM2R2: low
RSVD27
RSVD28
RSVD29
RSVD30
RSVD31
RSVD32
RSVD33
RSVD34
RSVD35
RSVD36
AD25
AE24
AE25
AJ18
AJ20
C18
C20
G24
G25
H25
V29
W30
AM3 =>DRAM Thermal Event Status
R104
1K/4/1
DDR15V
MB_EVENT_L
MA_EVENT_L
MB_EVENT_L <8>
MA_EVENT_L <8>
R105
1K/4/1
DDR15V
Layout: Route as 60 ohms
with 5/10 W/S from CPU pins.
EVENT pins are for future AM3r2
Y31
Y30
AG31
V31
W31
AE31
DCLKB2
DCLKB2-
MODT_B3
DCLKB1
DCLKB1-
MODT_B1
MB_EVENT_L
MA_EVENT_L
B01P
B01N
AM3 only
<8> DCLKB1
<8> -DCLKB1
<8> MODT_B1
DCLKB1
-DCLKB1
MODT_B1
CPUVREF
DDR15V
40 MILS WIDTH
CPU_M_VREF
SR19
16.9/4/1
SBC12
1N/4/X7R/50V/K
SBC31
SC35
1U/6/X7R/16V/K
SR20
16.9/4/1
0.1u/4/X7R/16V/K
GIGABYTE
Title
CPU CONTROL
Size
Custom
Document Number
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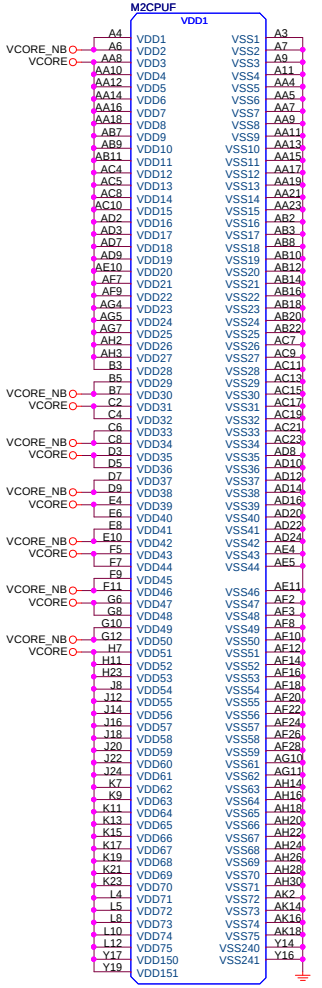
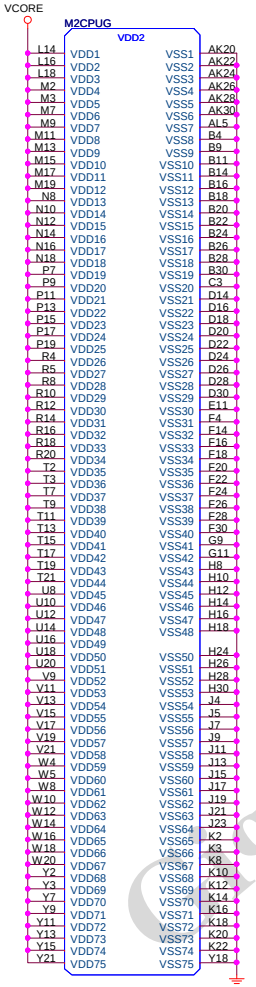
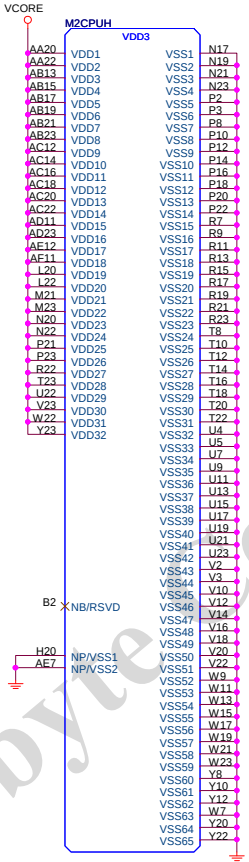
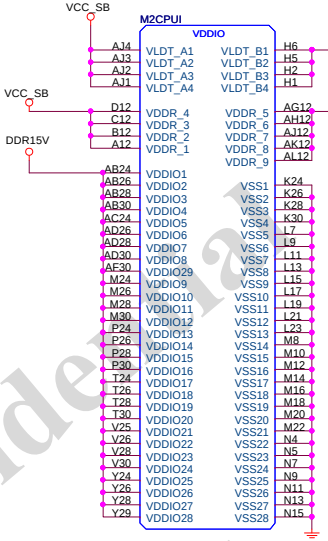
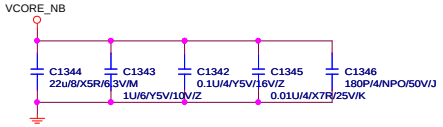
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

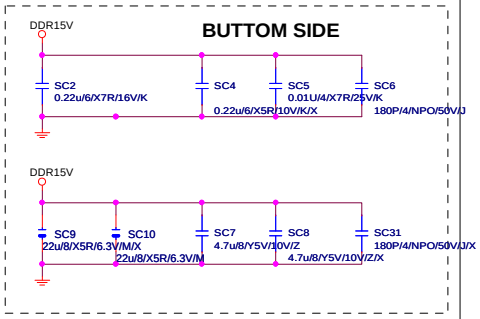


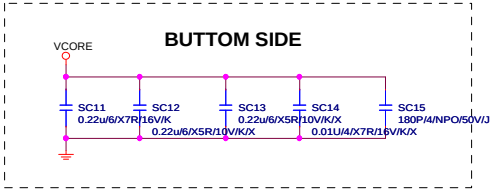


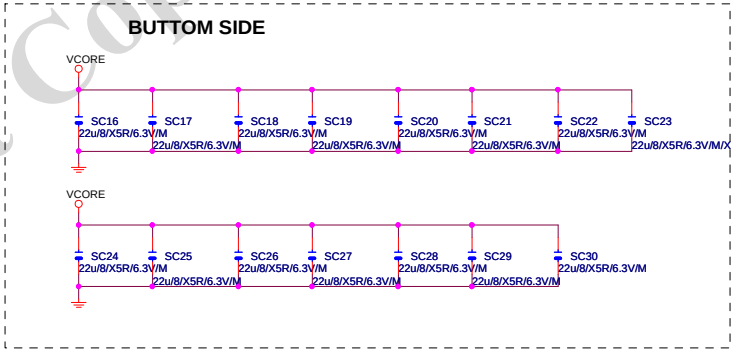


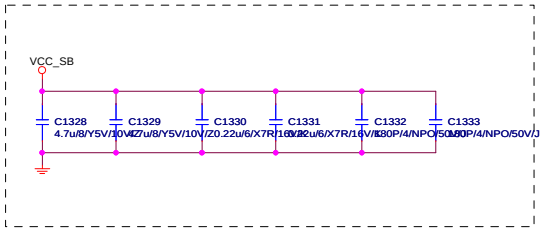


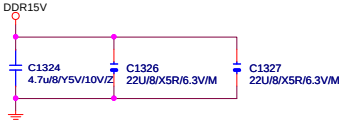


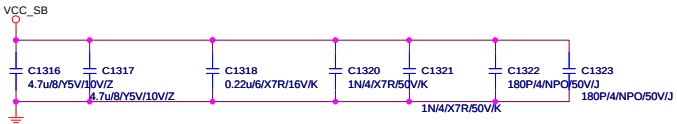


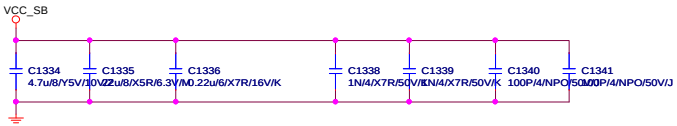


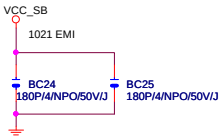












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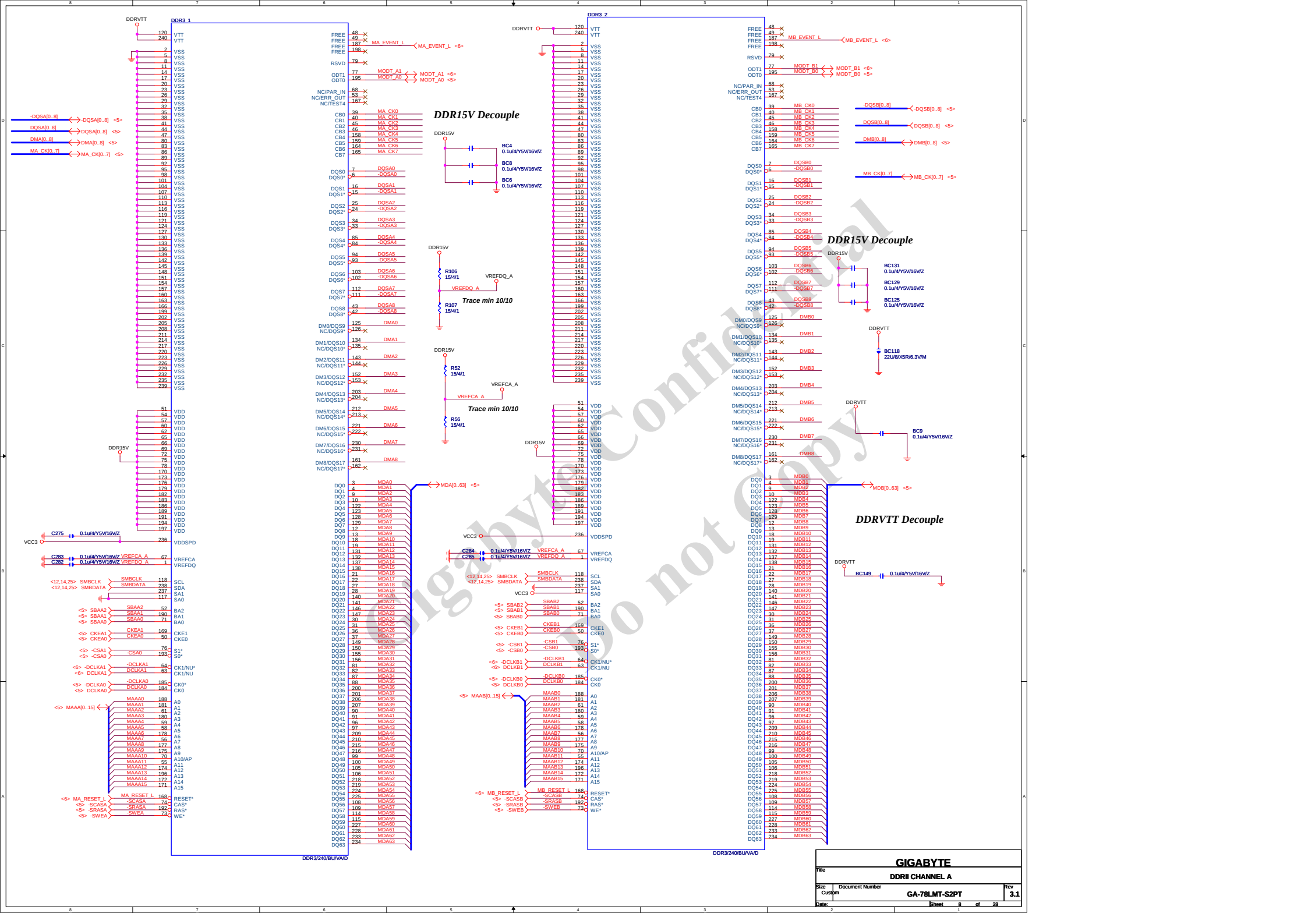
Title: CPU POWER & GND

Size	Document Number	Rev
Custom	GA-78LMT-S2PT	3.1

Date: Wednesday, December 28, 2011 Sheet 7 of 28



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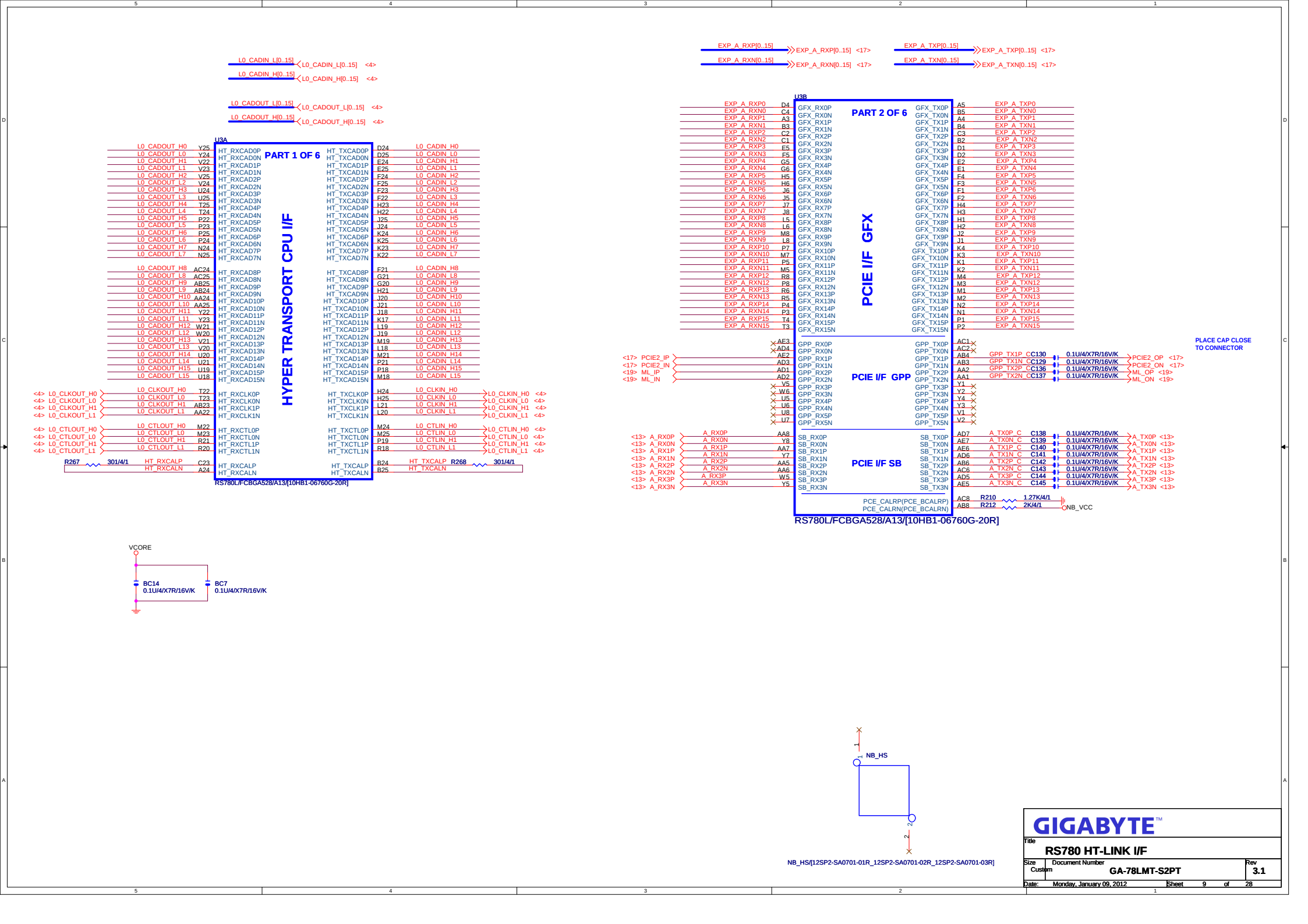
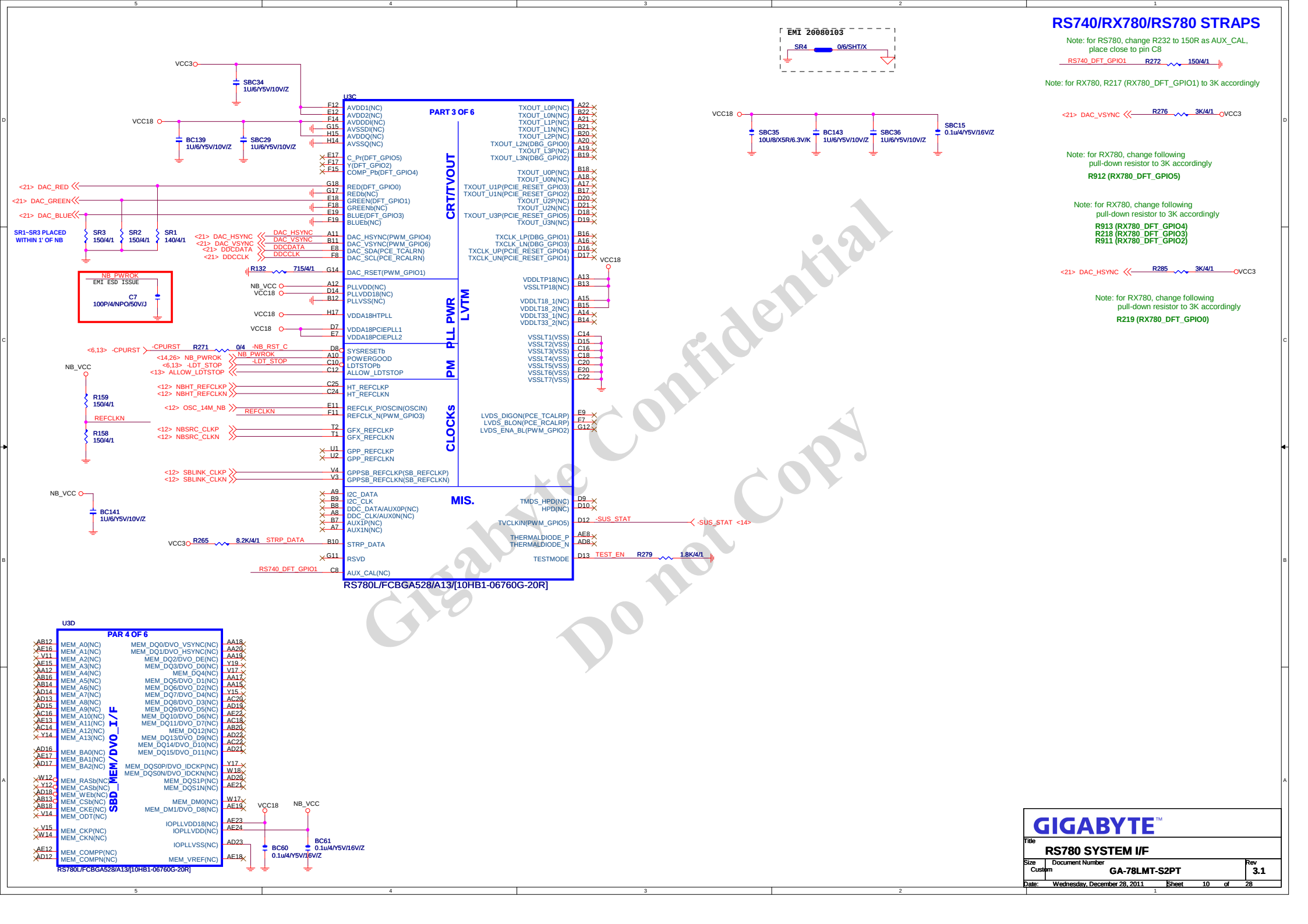
GIGABYTE		
Title: DDRII CHANNEL A		
Size: Custom	Document Number: GA-78LMT-S2PT	Rev: 3.1
Date:	Sheet 8 of 28	


L0_CADIN_L[0..15]
L0_CADIN_L[0..15] <4>
L0_CADIN_H[0..15]
L0_CADIN_H[0..15] <4>
L0_CADOUT_L[0..15]
L0_CADOUT_L[0..15] <4>
L0_CADOUT_H[0..15]
L0_CADOUT_H[0..15] <4>
U3A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
HT_RXCAD0P HT_RXCAD0N HT_RXCAD1P HT_RXCAD1N HT_RXCAD2P HT_RXCAD2N HT_RXCAD3P HT_RXCAD3N HT_RXCAD4P HT_RXCAD4N HT_RXCAD5P HT_RXCAD5N HT_RXCAD6P HT_RXCAD6N HT_RXCAD7P HT_RXCAD7N
HT_RXCAD8P HT_RXCAD8N HT_RXCAD9P HT_RXCAD9N HT_RXCAD10P HT_RXCAD10N HT_RXCAD11P HT_RXCAD11N HT_RXCAD12P HT_RXCAD12N HT_RXCAD13P HT_RXCAD13N HT_RXCAD14P HT_RXCAD14N HT_RXCAD15P HT_RXCAD15N
HT_RXCLK0P HT_RXCLK0N HT_RXCLK1P HT_RXCLK1N
HT_RXCTL0P HT_RXCTL0N HT_RXCTL1P HT_RXCTL1N
HT_RXCALP HT_RXCALN
HT_TXCAD0P HT_TXCAD0N HT_TXCAD1P HT_TXCAD1N HT_TXCAD2P HT_TXCAD2N HT_TXCAD3P HT_TXCAD3N HT_TXCAD4P HT_TXCAD4N HT_TXCAD5P HT_TXCAD5N HT_TXCAD6P HT_TXCAD6N HT_TXCAD7P HT_TXCAD7N
HT_TXCAD8P HT_TXCAD8N HT_TXCAD9P HT_TXCAD9N HT_TXCAD10P HT_TXCAD10N HT_TXCAD11P HT_TXCAD11N HT_TXCAD12P HT_TXCAD12N HT_TXCAD13P HT_TXCAD13N HT_TXCAD14P HT_TXCAD14N HT_TXCAD15P HT_TXCAD15N
HT_TXCLK0P HT_TXCLK0N HT_TXCLK1P HT_TXCLK1N
HT_TXCTL0P HT_TXCTL0N HT_TXCTL1P HT_TXCTL1N
HT_TXCALP HT_TXCALN
L0_CADOUT_H0 L0_CADOUT_L0 L0_CADOUT_H1 L0_CADOUT_L1 L0_CADOUT_H2 L0_CADOUT_L2 L0_CADOUT_H3 L0_CADOUT_L3 L0_CADOUT_H4 L0_CADOUT_L4 L0_CADOUT_H5 L0_CADOUT_L5 L0_CADOUT_H6 L0_CADOUT_L6 L0_CADOUT_H7 L0_CADOUT_L7
L0_CADOUT_H8 L0_CADOUT_L8 L0_CADOUT_H9 L0_CADOUT_L9 L0_CADOUT_H10 L0_CADOUT_L10 L0_CADOUT_H11 L0_CADOUT_L11 L0_CADOUT_H12 L0_CADOUT_L12 L0_CADOUT_H13 L0_CADOUT_L13 L0_CADOUT_H14 L0_CADOUT_L14 L0_CADOUT_H15 L0_CADOUT_L15
L0_CLKOUT_H0 L0_CLKOUT_L0 L0_CLKOUT_H1 L0_CLKOUT_L1
L0_CTLOUT_H0 L0_CTLOUT_L0 L0_CTLOUT_H1 L0_CTLOUT_L1
L0_CADIN_H0 L0_CADIN_L0 L0_CADIN_H1 L0_CADIN_L1 L0_CADIN_H2 L0_CADIN_L2 L0_CADIN_H3 L0_CADIN_L3 L0_CADIN_H4 L0_CADIN_L4 L0_CADIN_H5 L0_CADIN_L5 L0_CADIN_H6 L0_CADIN_L6 L0_CADIN_H7 L0_CADIN_L7
L0_CADIN_H8 L0_CADIN_L8 L0_CADIN_H9 L0_CADIN_L9 L0_CADIN_H10 L0_CADIN_L10 L0_CADIN_H11 L0_CADIN_L11 L0_CADIN_H12 L0_CADIN_L12 L0_CADIN_H13 L0_CADIN_L13 L0_CADIN_H14 L0_CADIN_L14 L0_CADIN_H15 L0_CADIN_L15
L0_CLKIN_H0 L0_CLKIN_L0 L0_CLKIN_H1 L0_CLKIN_L1
L0_CTLIN_H0 L0_CTLIN_L0 L0_CTLIN_H1 L0_CTLIN_L1
R267 301/4/1 HT_RXCALP HT_RXCALN
R268 301/4/1
RS780L/FCBGA528/A13/[10HB1-06760G-20R]
VCORE
BC14 0.1U/4/X7R/16V/K
BC7 0.1U/4/X7R/16V/K
EXP_A_RXP[0..15]
EXP_A_RXP[0..15] <17>
EXP_A_RXN[0..15]
EXP_A_RXN[0..15] <17>
EXP_A_TXP[0..15]
EXP_A_TXP[0..15] <17>
EXP_A_TXN[0..15]
EXP_A_TXN[0..15] <17>
U3B
PART 2 OF 6
PCIE I/F GFX
GFX_RX0P GFX_RX0N GFX_RX1P GFX_RX1N GFX_RX2P GFX_RX2N GFX_RX3P GFX_RX3N GFX_RX4P GFX_RX4N GFX_RX5P GFX_RX5N GFX_RX6P GFX_RX6N GFX_RX7P GFX_RX7N GFX_RX8P GFX_RX8N GFX_RX9P GFX_RX9N GFX_RX10P GFX_RX10N GFX_RX11P GFX_RX11N GFX_RX12P GFX_RX12N GFX_RX13P GFX_RX13N GFX_RX14P GFX_RX14N GFX_RX15P GFX_RX15N
GFX_TX0P GFX_TX0N GFX_TX1P GFX_TX1N GFX_TX2P GFX_TX2N GFX_TX3P GFX_TX3N GFX_TX4P GFX_TX4N GFX_TX5P GFX_TX5N GFX_TX6P GFX_TX6N GFX_TX7P GFX_TX7N GFX_TX8P GFX_TX8N GFX_TX9P GFX_TX9N GFX_TX10P GFX_TX10N GFX_TX11P GFX_TX11N GFX_TX12P GFX_TX12N GFX_TX13P GFX_TX13N GFX_TX14P GFX_TX14N GFX_TX15P GFX_TX15N
EXP_A_RXP0 EXP_A_RXN0 EXP_A_RXP1 EXP_A_RXN1 EXP_A_RXP2 EXP_A_RXN2 EXP_A_RXP3 EXP_A_RXN3 EXP_A_RXP4 EXP_A_RXN4 EXP_A_RXP5 EXP_A_RXN5 EXP_A_RXP6 EXP_A_RXN6 EXP_A_RXP7 EXP_A_RXN7 EXP_A_RXP8 EXP_A_RXN8 EXP_A_RXP9 EXP_A_RXN9 EXP_A_RXP10 EXP_A_RXN10 EXP_A_RXP11 EXP_A_RXN11 EXP_A_RXP12 EXP_A_RXN12 EXP_A_RXP13 EXP_A_RXN13 EXP_A_RXP14 EXP_A_RXN14 EXP_A_RXP15 EXP_A_RXN15
EXP_A_TXP0 EXP_A_TXN0 EXP_A_TXP1 EXP_A_TXN1 EXP_A_TXP2 EXP_A_TXN2 EXP_A_TXP3 EXP_A_TXN3 EXP_A_TXP4 EXP_A_TXN4 EXP_A_TXP5 EXP_A_TXN5 EXP_A_TXP6 EXP_A_TXN6 EXP_A_TXP7 EXP_A_TXN7 EXP_A_TXP8 EXP_A_TXN8 EXP_A_TXP9 EXP_A_TXN9 EXP_A_TXP10 EXP_A_TXN10 EXP_A_TXP11 EXP_A_TXN11 EXP_A_TXP12 EXP_A_TXN12 EXP_A_TXP13 EXP_A_TXN13 EXP_A_TXP14 EXP_A_TXN14 EXP_A_TXP15 EXP_A_TXN15
PCIE I/F GPP
GPP_RX0P GPP_RX0N GPP_RX1P GPP_RX1N GPP_RX2P GPP_RX2N GPP_RX3P GPP_RX3N GPP_RX4P GPP_RX4N GPP_RX5P GPP_RX5N
GPP_TX0P GPP_TX0N GPP_TX1P GPP_TX1N GPP_TX2P GPP_TX2N GPP_TX3P GPP_TX3N GPP_TX4P GPP_TX4N GPP_TX5P GPP_TX5N
<17> PCIE2_IP <17> PCIE2_IN <19> ML_IP <19> ML_IN
GPP_TX1P_C C130 0.1U/4/X7R/16V/K PCIE2_OP <17>
GPP_TX1N_C C129 0.1U/4/X7R/16V/K PCIE2_ON <17>
GPP_TX2P_C C136 0.1U/4/X7R/16V/K ML_OP <19>
GPP_TX2N_C C137 0.1U/4/X7R/16V/K ML_ON <19>
PLACE CAP CLOSE TO CONNECTOR
PCIE I/F SB
SB_RX0P SB_RX0N SB_RX1P SB_RX1N SB_RX2P SB_RX2N SB_RX3P SB_RX3N
SB_TX0P SB_TX0N SB_TX1P SB_TX1N SB_TX2P SB_TX2N SB_TX3P SB_TX3N
<13> A_RX0P <13> A_RX0N <13> A_RX1P <13> A_RX1N <13> A_RX2P <13> A_RX2N <13> A_RX3P <13> A_RX3N
A_TX0P_C C138 0.1U/4/X7R/16V/K A_TX0P <13>
A_TX0N_C C139 0.1U/4/X7R/16V/K A_TX0N <13>
A_TX1P_C C140 0.1U/4/X7R/16V/K A_TX1P <13>
A_TX1N_C C141 0.1U/4/X7R/16V/K A_TX1N <13>
A_TX2P_C C142 0.1U/4/X7R/16V/K A_TX2P <13>
A_TX2N_C C143 0.1U/4/X7R/16V/K A_TX2N <13>
A_TX3P_C C144 0.1U/4/X7R/16V/K A_TX3P <13>
A_TX3N_C C145 0.1U/4/X7R/16V/K A_TX3N <13>
PCE_CALRP(PCE_BCALRP)
PCE_CALRN(PCE_BCALRN)
R210 1.27K/4/1
R212 2K/4/1
NB_VCC
RS780L/FCBGA528/A13/[10HB1-06760G-20R]
NB_HS
NB_HS/[12SP2-SA0701-01R_12SP2-SA0701-02R_12SP2-SA0701-03R]
GIGABYTE
Title
RS780 HT-LINK I/F
Size Custom
Document Number GA-78LMT-S2PT
Rev 3.1
Date: Monday, January 09, 2012
Sheet 9 of 28


RS740/RX780/RS780 STRAPS
Note: for RS780, change R232 to 150R as AUX_CAL, place close to pin C8
RS740_DFT_GPIO1 R272 150/4/1
Note: for RX780, R217 (RX780_DFT_GPIO1) to 3K accordingly
<21> DAC_VSYNC R276 3K/4/1 VCC3
Note: for RX780, change following pull-down resistor to 3K accordingly
R912 (RX780_DFT_GPIO5)
Note: for RX780, change following pull-down resistor to 3K accordingly
R913 (RX780_DFT_GPIO4)
R218 (RX780_DFT_GPIO3)
R911 (RX780_DFT_GPIO2)
<21> DAC_HSYNC R285 3K/4/1 VCC3
Note: for RX780, change following pull-down resistor to 3K accordingly
R219 (RX780_DFT_GPIO0)
EMI 20080103
SR4 0/6/SHT/X
VCC3
SBC34 1U/6/Y5V/10V/Z
VCC18
BC139 1U/6/Y5V/10V/Z
SBC29 1U/6/Y5V/10V/Z
U3C
PART 3 OF 6
CRT/TVOUT
PLL PWR
LVTM
PM
CLOCKs
MIS.
AVDD1(NC)
AVDD2(NC)
AVDDDI(NC)
AVSSDI(NC)
AVDDQ(NC)
AVSSQ(NC)
C_Pr(DFT_GPIO5)
Y(DFT_GPIO2)
COMP_Pb(DFT_GPIO4)
RED(DFT_GPIO0)
REDb(NC)
GREEN(DFT_GPIO1)
GREENb(NC)
BLUE(DFT_GPIO3)
BLUEb(NC)
DAC_HSYNC(PWM_GPIO4)
DAC_VSYNC(PWM_GPIO6)
DAC_SDA(PCE_TCALRN)
DAC_SCL(PCE_RCALRN)
DAC_RSET(PWM_GPIO1)
PLLVDD(NC)
PLLVDD18(NC)
PLLVSS(NC)
VDDA18HTPLL
VDDA18PCIEPLL1
VDDA18PCIEPLL2
SYSRESETb
POWERGOOD
LDTSTOPb
ALLOW_LDTSTOP
HT_REFCLKP
HT_REFCLKN
REFCLK_P/OSCIN(OSCIN)
REFCLK_N(PWM_GPIO3)
GFX_REFCLKP
GFX_REFCLKN
GPP_REFCLKP
GPP_REFCLKN
GPPSB_REFCLKP(SB_REFCLKP)
GPPSB_REFCLKN(SB_REFCLKN)
I2C_DATA
I2C_CLK
DDC_DATA/AUX0P(NC)
DDC_CLK/AUX0N(NC)
AUX1P(NC)
AUX1N(NC)
STRP_DATA
RSVD
AUX_CAL(NC)
TXOUT_L0P(NC)
TXOUT_L0N(NC)
TXOUT_L1P(NC)
TXOUT_L1N(NC)
TXOUT_L2P(NC)
TXOUT_L2N(DBG_GPIO0)
TXOUT_L3P(NC)
TXOUT_L3N(DBG_GPIO2)
TXOUT_U0P(NC)
TXOUT_U0N(NC)
TXOUT_U1P(PCIE_RESET_GPIO3)
TXOUT_U1N(PCIE_RESET_GPIO2)
TXOUT_U2P(NC)
TXOUT_U2N(NC)
TXOUT_U3P(PCIE_RESET_GPIO5)
TXOUT_U3N(NC)
TXCLK_LP(DBG_GPIO1)
TXCLK_LN(DBG_GPIO3)
TXCLK_UP(PCIE_RESET_GPIO4)
TXCLK_UN(PCIE_RESET_GPIO1)
VDDLTP18(NC)
VSSLTP18(NC)
VDDLT18_1(NC)
VDDLT18_2(NC)
VDDLT33_1(NC)
VDDLT33_2(NC)
VSSLT1(VSS)
VSSLT2(VSS)
VSSLT3(VSS)
VSSLT4(VSS)
VSSLT5(VSS)
VSSLT6(VSS)
VSSLT7(VSS)
LVDS_DIGON(PCE_TCALRP)
LVDS_BLON(PCE_RCALRP)
LVDS_ENA_BL(PWM_GPIO2)
TMDS_HPD(NC)
HPD(NC)
TVCLKIN(PWM_GPIO5)
THERMALDIODE_P
THERMALDIODE_N
TESTMODE
RS780L/FCBGA528/A13/[10HB1-06760G-20R]
SR1~SR3 PLACED WITHIN 1' OF NB
SR3 150/4/1
SR2 150/4/1
SR1 140/4/1
<21> DAC_RED
<21> DAC_GREEN
<21> DAC_BLUE
<21> DAC_HSYNC
<21> DAC_VSYNC
<21> DDCDATA
<21> DDCCLK
R132 715/4/1
NB_PWROK
EMI ESD ISSUE
C7 100P/4/NPO/50V/J
NB_VCC
VCC18
<6,13> -CPURST
R271 0/4
-NB_RST_C
<14,26> NB_PWROK
<6,13> -LDT_STOP
<13> ALLOW_LDTSTOP
R159 150/4/1
R158 150/4/1
REFCLKN
<12> NBHT_REFCLKP
<12> NBHT_REFCLKN
<12> OSC_14M_NB
REFCLKN
<12> NBSRC_CLKP
<12> NBSRC_CLKN
<12> SBLINK_CLKP
<12> SBLINK_CLKN
BC141 1U/6/Y5V/10V/Z
R265 8.2K/4/1
STRP_DATA
RS740_DFT_GPIO1
-SUS_STAT
-SUS_STAT <14>
TEST_EN
R279 1.8K/4/1
SBC35 10U/8/X5R/6.3V/K
BC143 1U/6/Y5V/10V/Z
SBC36 1U/6/Y5V/10V/Z
SBC15 0.1u/4/Y5V/16V/Z
U3D
PAR 4 OF 6
SBD_MEM/DVO_I/F
MEM_A0(NC)
MEM_A1(NC)
MEM_A2(NC)
MEM_A3(NC)
MEM_A4(NC)
MEM_A5(NC)
MEM_A6(NC)
MEM_A7(NC)
MEM_A8(NC)
MEM_A9(NC)
MEM_A10(NC)
MEM_A11(NC)
MEM_A12(NC)
MEM_A13(NC)
MEM_BA0(NC)
MEM_BA1(NC)
MEM_BA2(NC)
MEM_RASb(NC)
MEM_CASb(NC)
MEM_WEb(NC)
MEM_CSb(NC)
MEM_CKE(NC)
MEM_ODT(NC)
MEM_CKP(NC)
MEM_CKN(NC)
MEM_COMPP(NC)
MEM_COMPN(NC)
MEM_DQ0/DVO_VSYNC(NC)
MEM_DQ1/DVO_HSYNC(NC)
MEM_DQ2/DVO_DE(NC)
MEM_DQ3/DVO_D0(NC)
MEM_DQ4(NC)
MEM_DQ5/DVO_D1(NC)
MEM_DQ6/DVO_D2(NC)
MEM_DQ7/DVO_D4(NC)
MEM_DQ8/DVO_D3(NC)
MEM_DQ9/DVO_D5(NC)
MEM_DQ10/DVO_D6(NC)
MEM_DQ11/DVO_D7(NC)
MEM_DQ12(NC)
MEM_DQ13/DVO_D9(NC)
MEM_DQ14/DVO_D10(NC)
MEM_DQ15/DVO_D11(NC)
MEM_DQS0P/DVO_IDCKP(NC)
MEM_DQS0N/DVO_IDCKN(NC)
MEM_DQS1P(NC)
MEM_DQS1N(NC)
MEM_DM0(NC)
MEM_DM1/DVO_D8(NC)
IOPLLVDD18(NC)
IOPLLVDD(NC)
IOPLLVSS(NC)
MEM_VREF(NC)
RS780L/FCBGA528/A13/[10HB1-06760G-20R]
BC60 0.1u/4/Y5V/16V/Z
BC61 0.1u/4/Y5V/16V/Z
GIGABYTE
Title
RS780 SYSTEM I/F
Size Custom
Document Number GA-78LMT-S2PT
Rev 3.1
Date: Wednesday, December 28, 2011
Sheet 10 of 28
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RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC

U3F — PART 6/6 — GROUND

RS780L/FCBGA528/A13/[10HB1-06760G-20R]

Please use 1mm pad size, place all ELT test pads on bottom side only

U3E — PART 5/6 — POWER

RS780L/FCBGA528/A13/[10HB1-06760G-20R]

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Title	RS780 POWER & GND
Size	Custom
Document Number	GA-78LMT-S2PT
Rev	3.1
Date:	Wednesday, December 28, 2011
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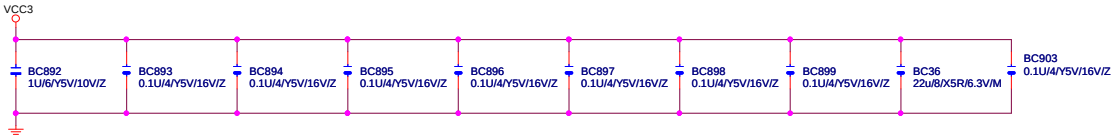


1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE

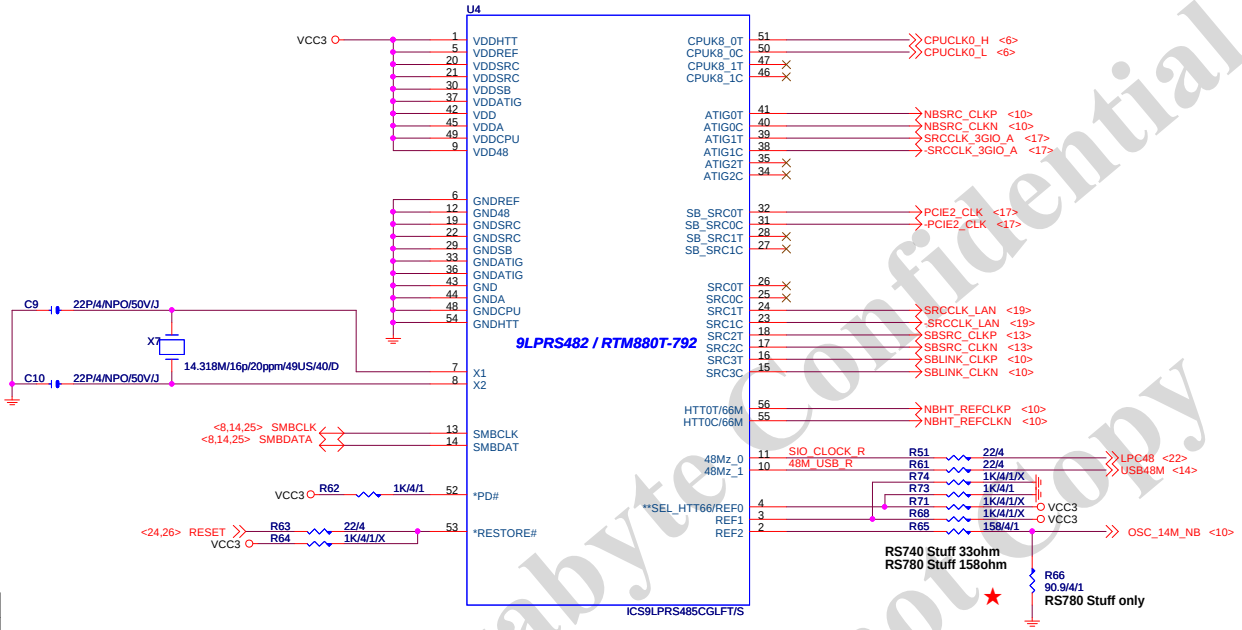
2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



watch dog --
RESTORE# 接 RESET

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

**SEL_HTT66/REF0		OUT 3.3V 14.318MHz REF output.
IN	Low	100MHz differential HT clock, (Internal 120KΩ pull-down)
	High	66MHz 3.3V single ended HT clock.

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PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600

S.B HEATSINK

SB_HS

SB_HS/[12SP2-030005-41R_12SP2-030005-42R_12SP2-030005-43R]

U2A

SB700

Part 1 of 5

SB710/FCBGA528/A14/[10HB1-06B710-11R]

PCI EXPRESS INTERFACE

PCI CLKS

PCI INTERFACE

CLOCK GENERATOR

RTC XTAL

LPC

CPU

RTC

Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

X4 32.768K/12.5p/20ppm/TF38/35K/D

SHW/D0.64*5.08*6.74

	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT

BIOS after boot setting
EC AOD-ACC

	LPC_CLK0	LPC_CLK1
PULL HIGH	IMC ENABLED AOD Extreme	CLKGEN ENABLED
PULL LOW	IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT

20mil 20mil 20mil

BAT54C/SOT23/200mA

BATTERY CR2032

CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

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Title: ATI SB710 PCIE/PCI/CPU/LPC

Size: Custom | Document Number: GA-78LMT-S2PT | Rev: 3.1

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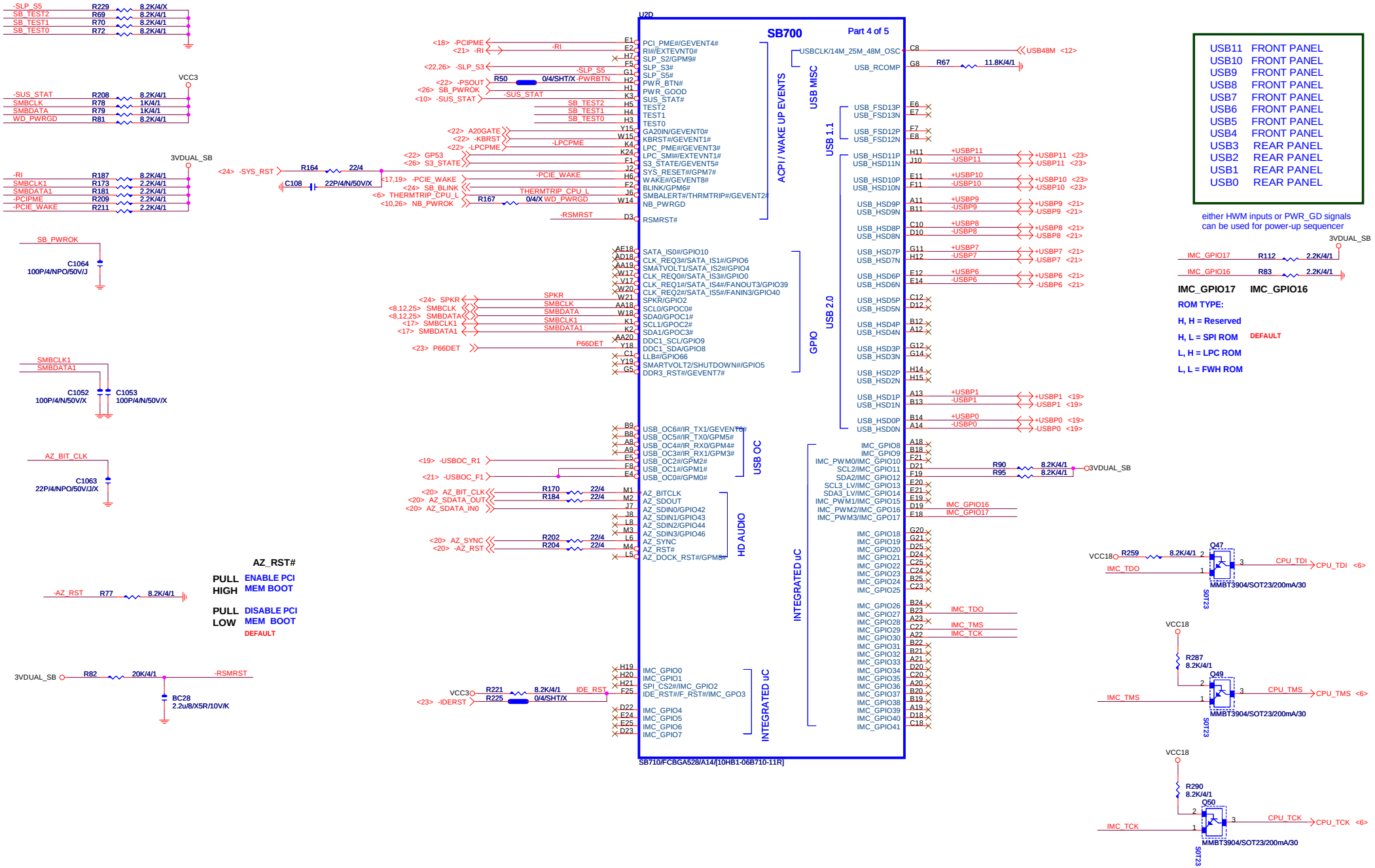
U2D
SB700
Part 4 of 5
SB710/FCBGA528/A14/[10HB1-06B710-11R]
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#
ACPI / WAKE UP EVENTS
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB MISC
USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB 1.1
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
USB 2.0
SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMATVOLT1/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SMARTVOLT2/SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#
GPIO
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
USB OC
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#
HD AUDIO
IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7
INTEGRATED uC
IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPIO16
IMC_PWM3/IMC_GPIO17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41
INTEGRATED uC
-SLP_S5 R229 8.2K/4/X
SB_TEST2 R69 8.2K/4/1
SB_TEST1 R70 8.2K/4/1
SB_TEST0 R72 8.2K/4/1
VCC3
-SUS_STAT R208 8.2K/4/1
SMBCLK R78 1K/4/1
SMBDATA R79 1K/4/1
WD_PWRGD R81 8.2K/4/1
3VDUAL_SB
-RI R187 8.2K/4/1
SMBCLK1 R173 2.2K/4/1
SMBDATA1 R181 2.2K/4/1
-PCIPME R209 2.2K/4/1
-PCIE_WAKE R211 2.2K/4/1
<24> -SYS_RST
R164 22/4
C108 22P/4/N/50V/X
SB_PWROK
C1064 100P/4/NPO/50V/J
SMBCLK1
SMBDATA1
C1052 100P/4/N/50V/X
C1053 100P/4/N/50V/X
AZ_BIT_CLK
C1063 22P/4/NPO/50V/J/X
-AZ_RST R77 8.2K/4/1
AZ_RST#
PULL HIGH ENABLE PCI MEM BOOT
PULL LOW DISABLE PCI MEM BOOT
DEFAULT
3VDUAL_SB R82 20K/4/1 -RSMRST
BC28 2.2u/8/X5R/10V/K
<18> -PCIPME
<21> -RI
-RI
<22,26> -SLP_S3
-SLP_S5
R50 0/4/SHT/X -PWRBTN
<22> -PSOUT
<26> SB_PWROK
<10> -SUS_STAT
-SUS_STAT
SB_TEST2
SB_TEST1
SB_TEST0
<22> A20GATE
<22> -KBRST
-LPCPME
<22> -LPCPME
<22> GP53
<26> S3_STATE
<17,19> -PCIE_WAKE
-PCIE_WAKE
<24> SB_BLINK
<6> THERMTRIP_CPU_L
THERMTRIP_CPU_L
<10,26> NB_PWROK
R167 0/4/X WD_PWRGD
-RSMRST
<24> SPKR
<8,12,25> SMBCLK
<8,12,25> SMBDATA
<17> SMBCLK1
<17> SMBDATA1
SPKR
SMBCLK
SMBDATA
SMBCLK1
SMBDATA1
<23> P66DET
P66DET
<19> -USBOC_R1
<21> -USBOC_F1
<20> AZ_BIT_CLK
<20> AZ_SDATA_OUT
<20> AZ_SDATA_IN0
R170 22/4
R184 22/4
<20> AZ_SYNC
<20> AZ_RST
R202 22/4
R204 22/4
VCC3
R221 8.2K/4/1
R225 0/4/SHT/X
IDE_RST
<23> -IDERST
C8 USB48M <12>
G8 R67 11.8K/4/1
+USBP11 -USBP11 <23>
+USBP10 -USBP10 <23>
+USBP9 -USBP9 <21>
+USBP8 -USBP8 <21>
+USBP7 -USBP7 <21>
+USBP6 -USBP6 <21>
+USBP1 -USBP1 <19>
+USBP0 -USBP0 <19>
R90 8.2K/4/1
R95 8.2K/4/1
3VDUAL_SB
IMC_TDO
IMC_TMS
IMC_TCK
USB11 FRONT PANEL
USB10 FRONT PANEL
USB9 FRONT PANEL
USB8 FRONT PANEL
USB7 FRONT PANEL
USB6 FRONT PANEL
USB5 FRONT PANEL
USB4 FRONT PANEL
USB3 REAR PANEL
USB2 REAR PANEL
USB1 REAR PANEL
USB0 REAR PANEL
either HWM inputs or PWR_GD signals can be used for power-up sequencer
3VDUAL_SB
IMC_GPIO17 R112 2.2K/4/1
IMC_GPIO16 R83 2.2K/4/1
IMC_GPIO17 IMC_GPIO16
ROM TYPE:
H, H = Reserved
H, L = SPI ROM DEFAULT
L, H = LPC ROM
L, L = FWH ROM
VCC18
R259 8.2K/4/1
Q47
IMC_TDO
CPU_TDI
CPU_TDI <6>
MMBT3904/SOT23/200mA/30
SOT23
R287 8.2K/4/1
Q49
IMC_TMS
CPU_TMS
CPU_TMS <6>
R290 8.2K/4/1
Q50
IMC_TCK
CPU_TCK
CPU_TCK <6>
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Title
ATI SB710 ACPI/USB/GPIO/AUDIO
Size Custom
Document Number GA-78LMT-S2PT
Rev 3.1
Date: Wednesday, December 28, 2011
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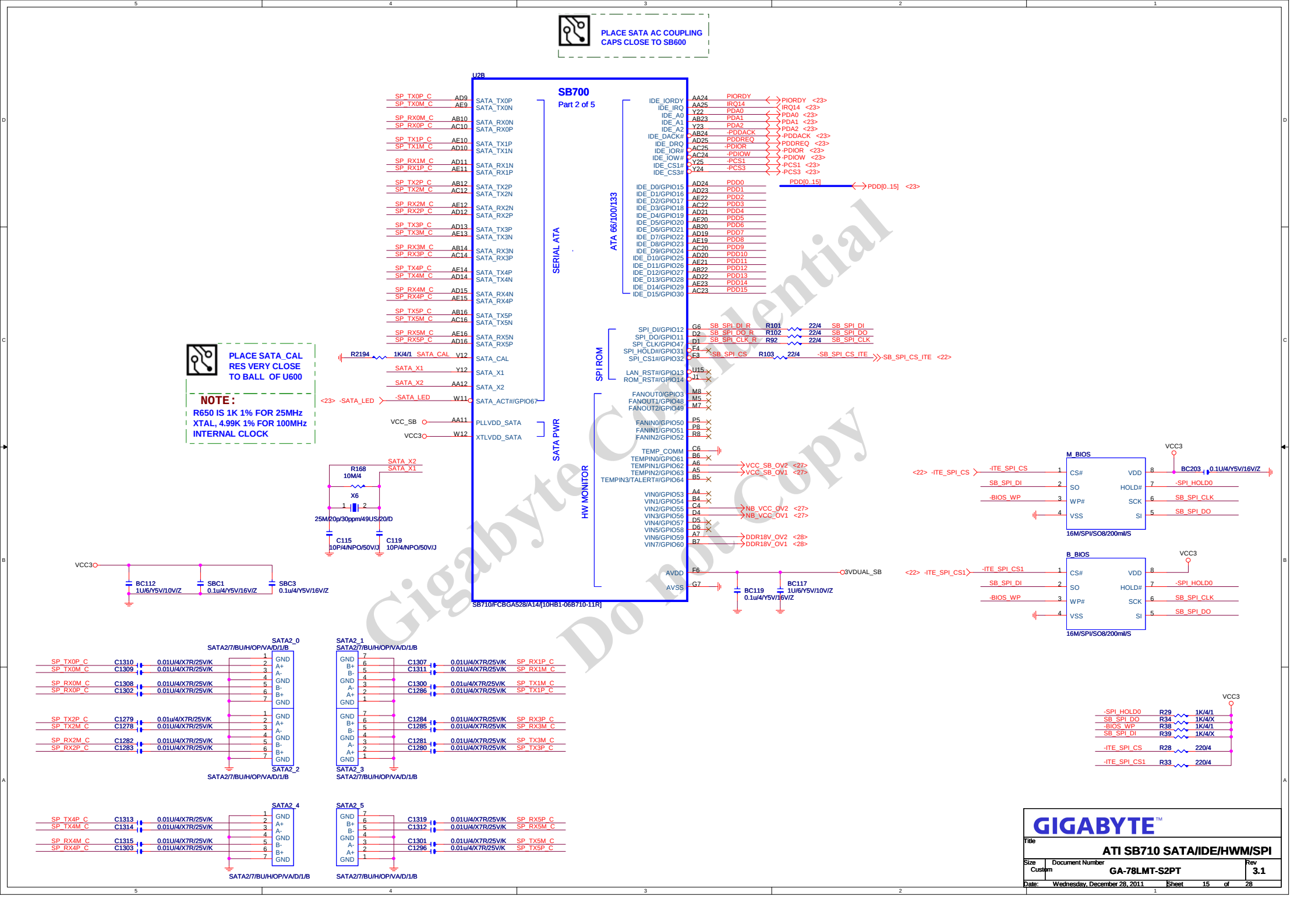

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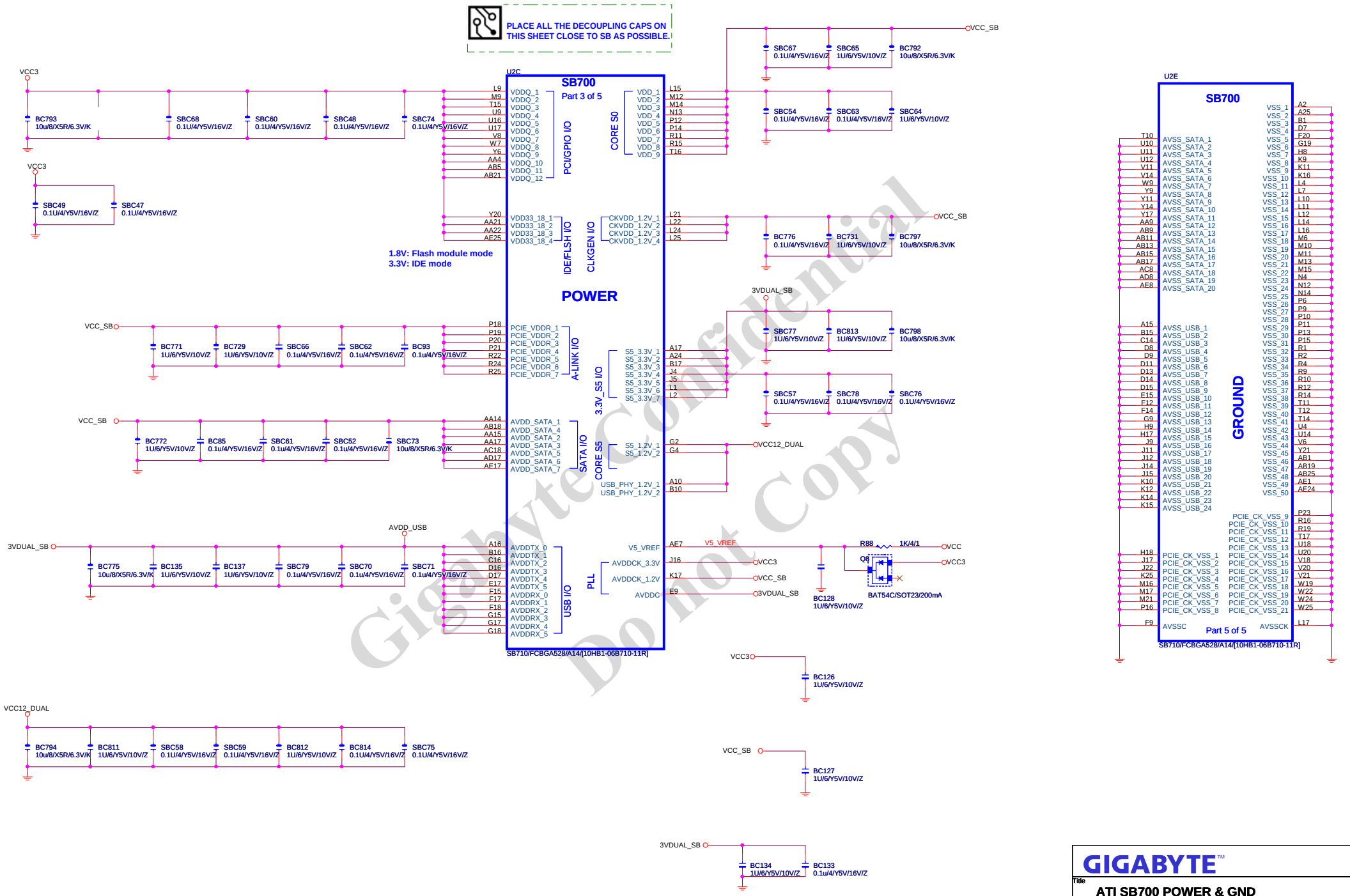

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Title: ATI SB700 POWER & GND

Size	Document Number	Rev
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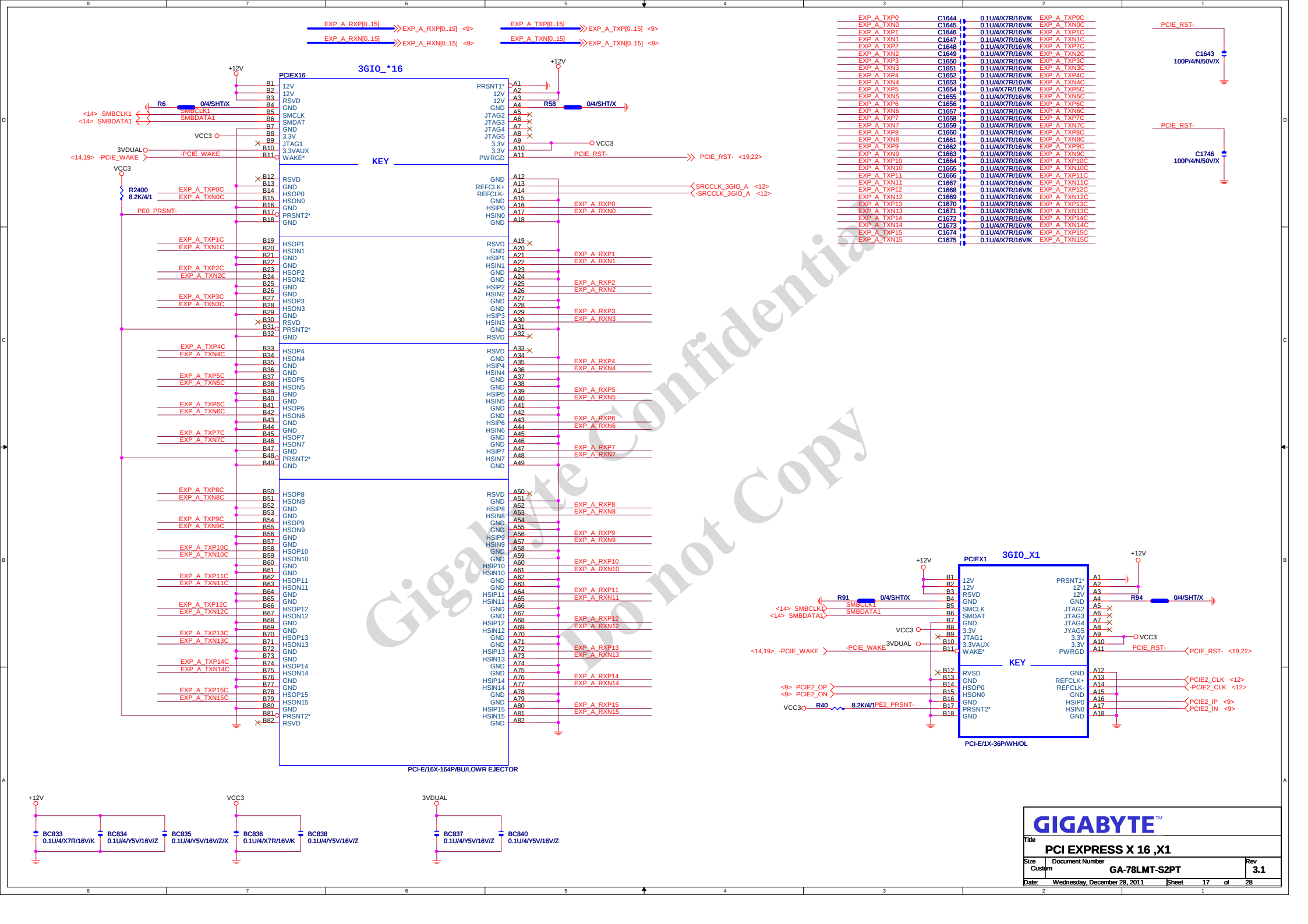
EXP_A_RXP[0..15]
EXP_A_RXN[0..15]
EXP_A_TXP[0..15]
EXP_A_TXN[0..15]
3GIO_*16
PCIEX16
KEY
PCI-E/16X-164P/BU/LOWR EJECTOR
3GIO_X1
PCIEX1
PCI-E/1X-36P/WH/OL
PCIE_RST-
C1643
100P/4/N/50V/X
C1746
100P/4/N/50V/X
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PCI EXPRESS X 16 ,X1
GA-78LMT-S2PT
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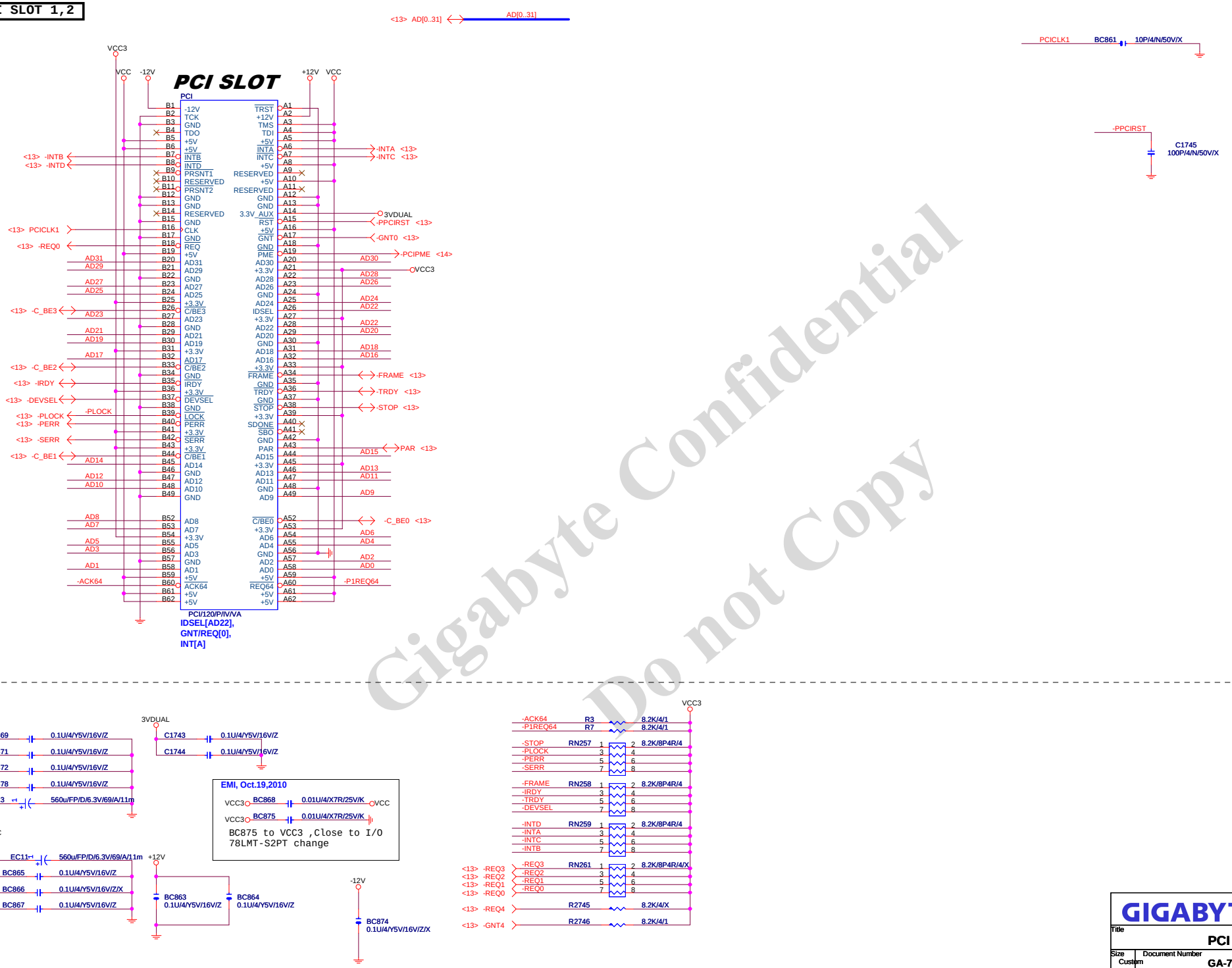
PCI SLOT 1,2



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Title	PCI SLOT 1,2	
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LAN:AR8151/AR8161

離IC近越好

LA_ ML-->80歐姆:[15/5/5/5/15]

SRCCLK-->50歐姆:[18/4/10/4/18]

<12> -SRCCLK_LAN
<12> SRCCLK_LAN
<9> ML_OP
<9> ML_ON

LABC5 0.1u/4/X7R/16V/K
LABC4 1u/4/X5R/6.3V/K
LABC3 0.1u/4/X7R/16V/K
LABC6 0.1u/4/X7R/16V/K
AR8161-->N/A (LABC6)

LA_AVDDVCO
LABC7 0.1u/4/X7R/16V/K/X
LABC8 4.7u/6/X5R/6.3V/K/X
AR8161-->(O)

3VDUAL
LABC9 10u/8/X5R/6.3V/K
LABC10 1u/4/X5R/6.3V/K
LABC11 0.1u/4/X7R/16V/K

LAU1

LA_ ML-->80歐姆:[15/5/5/5/15]

離IC近越好

LA_ML_IP_C LAC12 0.1u/4/X7R/16V/K
LA_ML_IN_C LAC13 0.1u/4/X7R/16V/K
ML_IP <9>
ML_IN <9>

3VDUAL
LAC33 100p/4/NPO/50V/J/X
LAR6 8.2K/4/1
<17,22> PCIE_RST-
<14,17> -PCIE_WAKE

AR8161-->N/A (LABC12)

LABC12 1u/4/X5R/6.3V/K
LABC15 1u/4/X5R/6.3V/K
LABC16 0.1u/4/X7R/16V/K
LABC18 1u/4/X5R/6.3V/K
LABC19 0.1u/4/X7R/16V/K
LAR10 2.37K/4/1

Atheros
AR8151/AR8161
AR8151-BL1A-R/S

LA_VDD33
LA_-CLKREQ
LA_VDDCT
LA_AVDDL
LA_XTALO
LA_XTALI
LA_AVDDH
LA_RBIAS
LA_PPS
LA_LED_LINK1000
LA_MDI3-

LAR9 0/4
LABC14 0.1u/4/X7R/16V/K
LA_DVDDL
AR8161-->N/A (LAR9,LAC18)
LABC17 0.1u/4/X7R/16V/K

LAX1 25M/20p/30ppm/49US/20/D
LA_XTALI
LA_XTALO
LAC31 27p/4/NPO/50V/J
LAC32 27p/4/NPO/50V/J

LABC20 0.1u/4/X7R/16V/K
AR8161-->N/A (LABC20)
LABC21 0.1u/4/X7R/16V/K

LAR19 0/4/X
LAR20 0/4
3VDUAL
LA_AVDDH
AR8151:LA_AVDDH(LAR20)
AR8161:3VDUAL(LAR19)
LABC22 1u/4/X5R/6.3V/K

SCH BOM OPT:(二擇一使用)
-->(LAC30):M/B有CLK GEN 25M
-->(LAX1,LAC31,LAC32):M/B無CLK GEN 25M

LAN POWER

NEW DESIGN ONLY FOR INTERNAL SWR
AR8151:LAR3(0),LAR5(X)
AR8161:LAR5(0),LAR3/LAR4(X)

EMI Request
Put on LAR4

LA_LX_OUT
LAESD2
AZ2225-01L/SOD323/X

LAL1 4.7uH/1A/[10LC4-5A470B-01R_10LI5-12470B-01R]
LA_LX_OUT
LA_LX
CLOSE
LA_LX 200mil
LABC1 10u/8/X5R/6.3V/K
LABC2 0.1u/4/X7R/16V/K

LA_VDDCT
LAR3 0/4
AR8161-->N/A (LAR3,LAR4)
AR8151 POWER
LA_AVDD_CEN
LAR4 0/4

LA_DVDDL
LA_AVDDL
LA_AVDDVCO
LAR5 0/6/X
AR8161-->(O)
LAFB2 0/6/X
AR8161-->BEAD
AR8151-->N/A
LAFB3 0/6
AR8161-->BEAD
AR8151-->0/6
AR8161 POWER

AR8161-->(O)
LA_AVDDH
LAR7 8.2K/4/X
LA_LED_ACT_TXRX
LA_LED_LINK100
LAR8 8.2K/4/X

AR8161-->(O)
VCC3
LAR1 30K/4/X
LAR2 0/4/X
LA_VDDCT
N_ISOLATEB <22>

Power domain chart

	AR8151	AR8161
AVDD33	N/A	3.3V
VDD33	3.3V	3.3V
AVDDH	2.7V	2.7V
AVDDL/DVDDL	1.1V	1.1V
VDDCT	1.7V	

MDI : AR8161-->N/A

LA_MDI0+ LA_MDI0-
LAR11 49.9/4/1
LAR12 49.9/4/1
LAR13 49.9/4/1
LA_MDI_RC0
LAC26 0.1u/4/X7R/16V/K

LA_MDI1+ LA_MDI1-
LAR14 49.9/4/1
LAR15 49.9/4/1
LA_MDI_RC1
LAC27 0.1u/4/X7R/16V/K

LA_MDI2+ LA_MDI2-
LAR16 49.9/4/1
LAR17 49.9/4/1
LA_MDI_RC2
LAC28 0.1u/4/X7R/16V/K

LA_MDI3+ LA_MDI3-
LAR18 49.9/4/1
LA_MDI_RC3
LAC29 0.1u/4/X7R/16V/K

CLOSE LAN CHIP

USB_LAN CONNECTOR

3VDUAL
LFB4 0/6/SHT/X

LABC23 0.1u/4/X7R/16V/K
LA_AVDD_CEN
USB_LAN
LA_MDI0+
LA_MDI0-
LA_MDI1+
LA_MDI1-
LA_MDI2+
LA_MDI2-
LA_MDI3+
LA_MDI3-
GND_L10
LABC25 0/4/SHT/M/X

UP
DOWN

D1 LA_LED_ACT_TXRX
D2 LA_LED_D2 LR13 150/4/1 LAN_3VDUAL_LED
D3 LA_LED_LINK100 LR21 150/4/1
D4 LA_LED_LINK1000 LR22 150/4/1
LBC33 0.1U/4/Y5V/25V/Z/X

U1 FUSEVCC
U2 -USBP0 -USBP0 <14>
U3 +USBP0 +USBP0 <14>
U4
U5 FUSEVCC
U6 -USBP1 -USBP1 <14>
U7 +USBP1 +USBP1 <14>
U8
LBC26 0.1U/4/Y5V/25V/Z/X
LBC29 0.1U/4/Y5V/25V/Z/X

USB+LAN/1G/GO,Y/OS/RA/D/8C/[11NR6-702009-0ER]

LAESD1
LA_LED_LINK100
LA_LED_LINK1000
LA_LED_ACT_TXRX
LAN_3VDUAL_LED
LA_LED_D2
AOZ8902CIL/SOT23-6

FUSEVCC
LEC4 560u/FP/D/6.3V/69/A/11m
EC要靠近USB_PORT的FUSEVCC

USB_LAN
EMI
LR28 0/6/SHT/X

SU1
-USBP0
+USBP0
-USBP1
FUSEVCC
+USBP1
AOZ8902CIL/SOT23-6

5VDUAL F6 SMD1812P260/6V FUSEVCC
FUSEVCC R3161 150K/4 -USBOC_R1 <14>
R3162 270K/4

GIGABYTE

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Size	Custom
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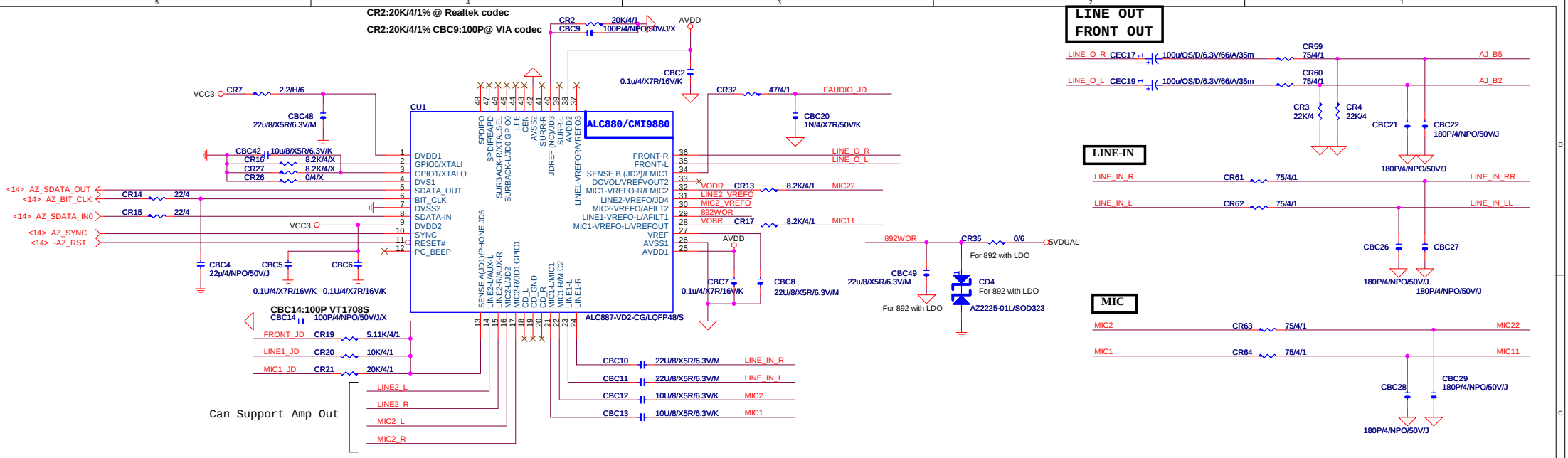
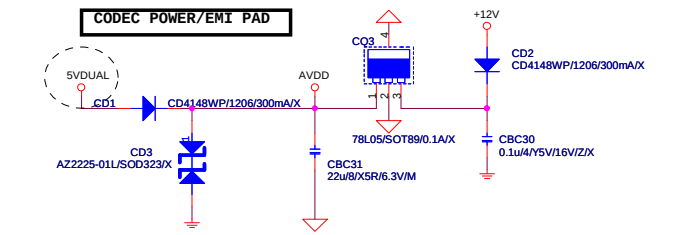
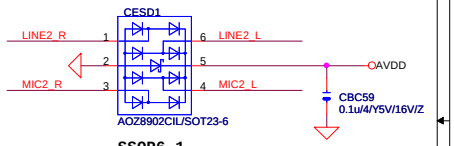
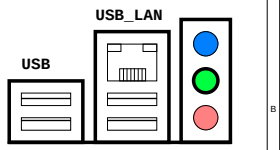


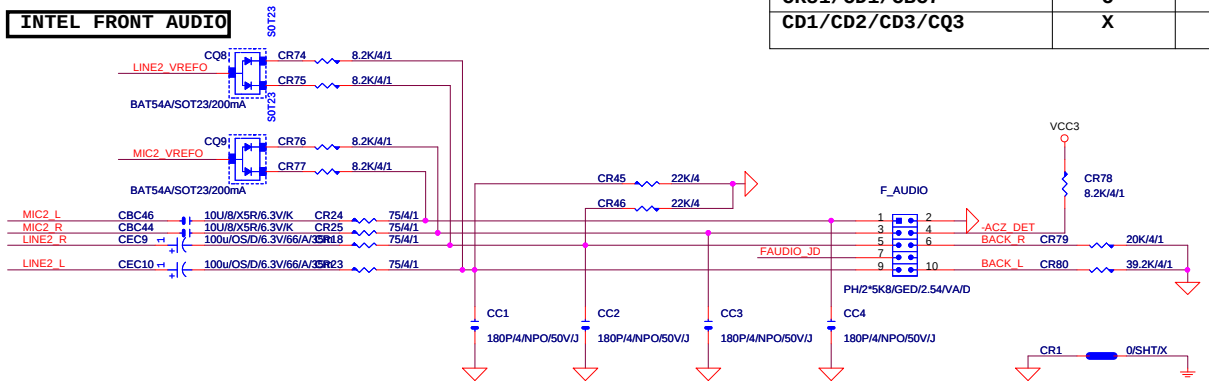
AZALIA CODEC — ALC887-VD2/ALC889/VT1708S/VT1708SCE Colay

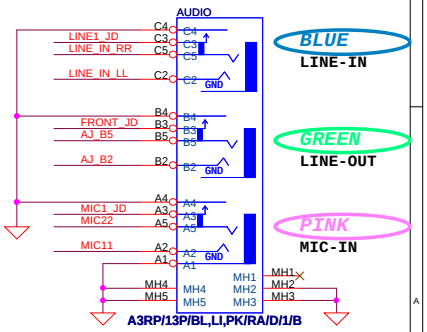
	ALC662	ALC887-VD2	ALC889	VT1708S	VT1708SCE
CR26	X	X	0	0	X
CR27	X	X	X	X	0.1u/4
CBC42	0	0	X	X	0
CR32/CBC20	47ohm+1nF	47ohm+1nF	47ohm+1nF	22ohm+100P	22ohm+100P
CR31	X	0	0	0	0
CR30	0	X	X	X	X
CR19	5.11K/4/1	5.11K/4/1	5.11K/4/1	5.1K/4/1	5.1K/4/1
CR2	20K/4/1	20K/4/1	20K/4/1	5.1K/4/1	20K/4/1
CBC9/CBC14	N/A	N/A	N/A	100P/4	100P/4
CR6/CR7/CR54/CR58	22K/4	22K/4	22K/4	10K/4	10K/4
CR59/CR60/CR61/ CR62/CR63/CR64	62 ohm	62 ohm	62 ohm	75 ohm	75 ohm
CR51/CD1/CBC7	0	0	X	X	0
CD1/CD2/CD3/CQ3	X	X	0	0	X











Fix AP issue
0713 realtek fix 0 ohm

Realtek recommand for AP
Put on Codec Bottom side

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Title	ALC888B CODEC		
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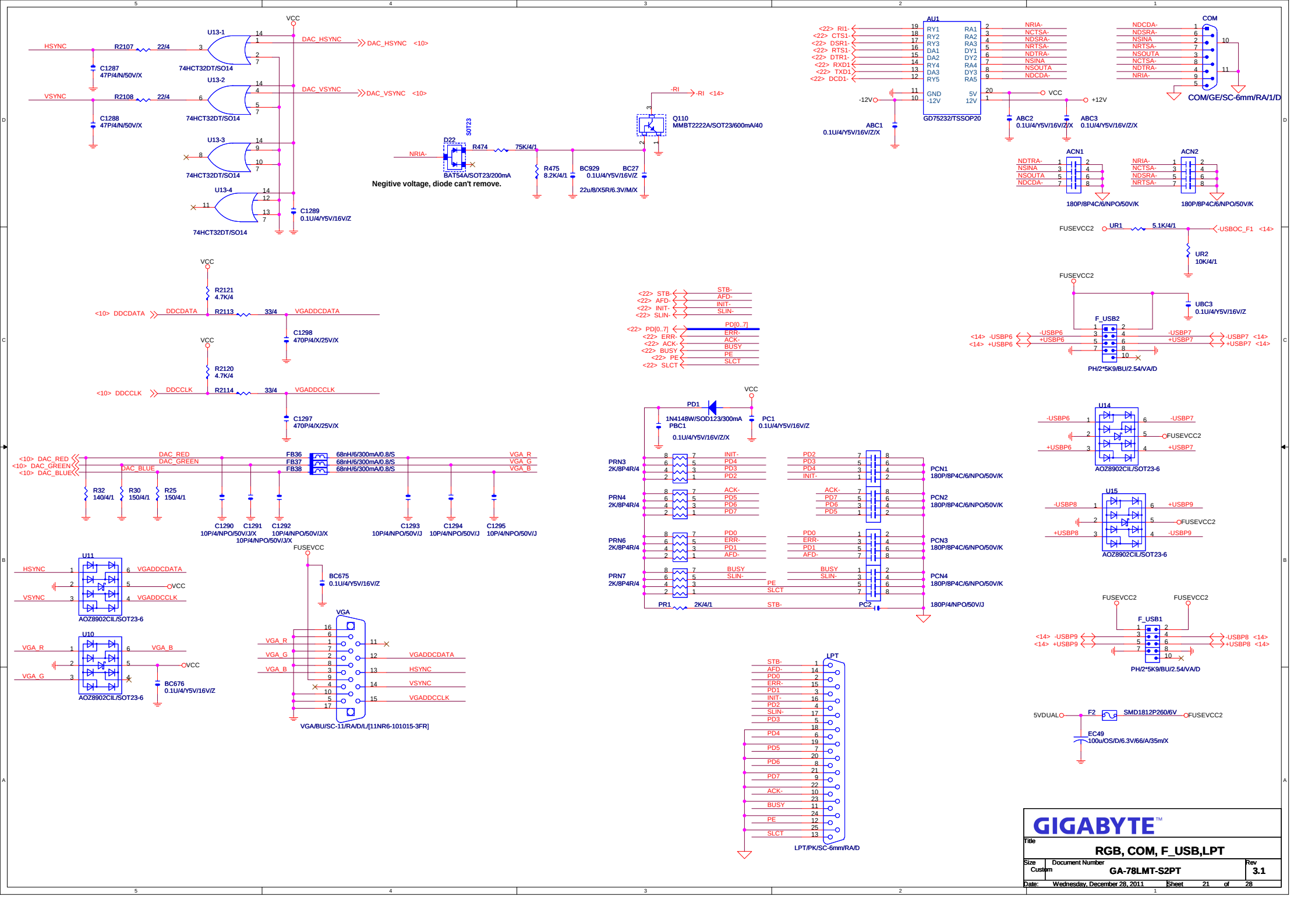

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Title	RGB, COM, F_USB,LPT	
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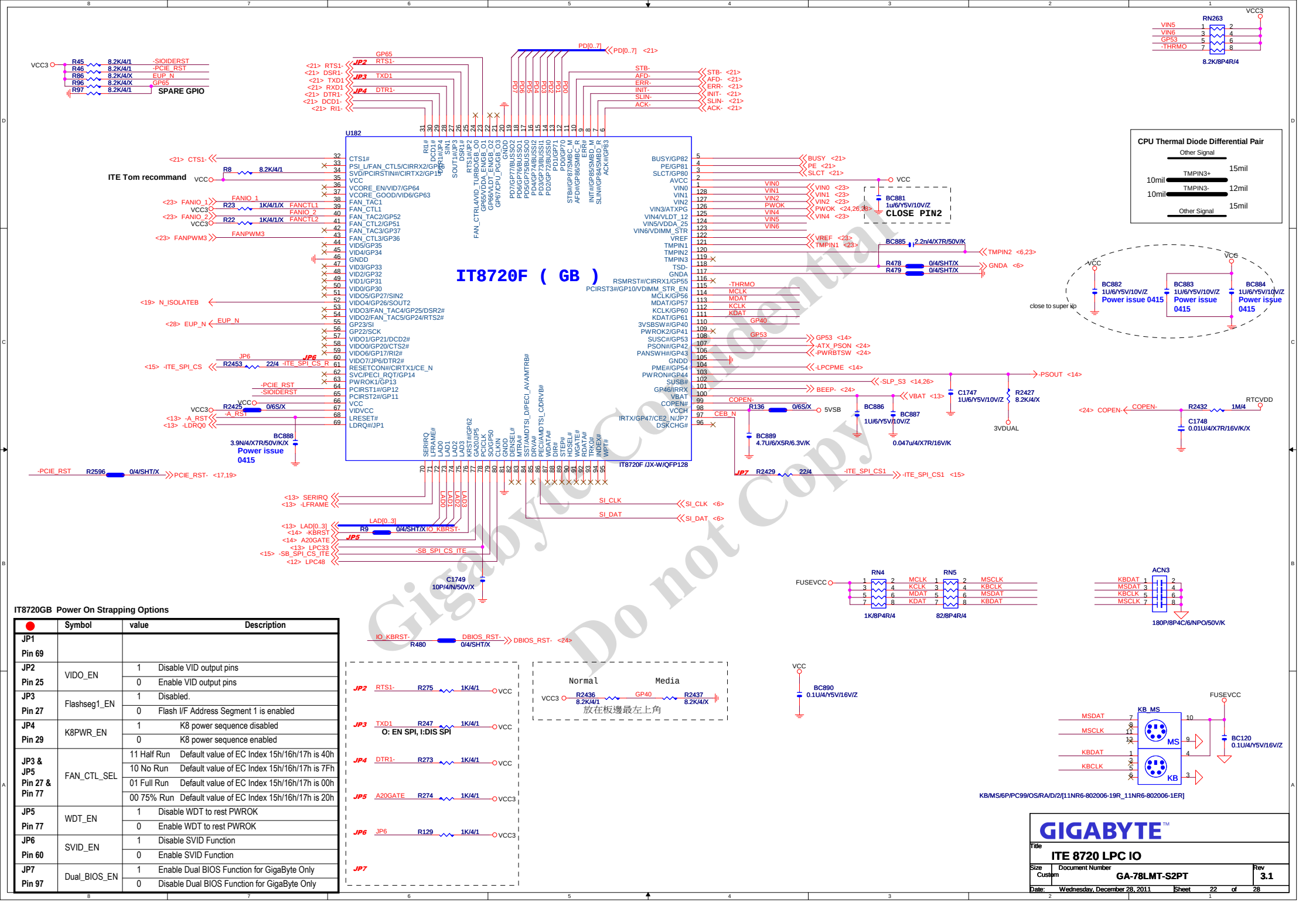

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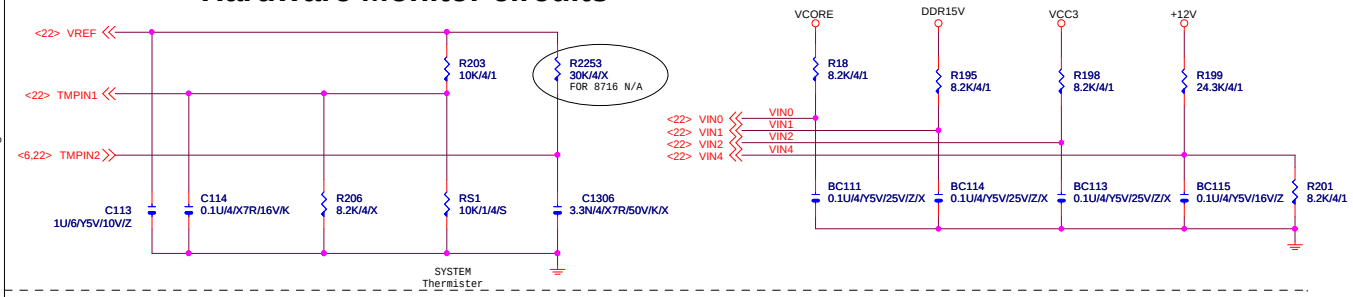
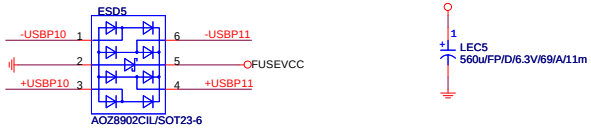
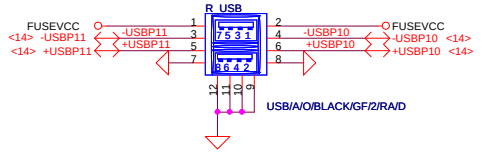
IT8720GB Power On Strapping Options

	Symbol	value	Description
JP1 Pin 69			
JP2 Pin 25	VIDO_EN	1	Disable VID output pins
		0	Enable VID output pins
JP3 Pin 27	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 is enabled
JP4 Pin 29	K8PWR_EN	1	K8 power sequence disabled
		0	K8 power sequence enabled
JP3 & JP5 Pin 27 & Pin 77	FAN_CTL_SEL	11 Half Run	Default value of EC Index 15h/16h/17h is 40h
		10 No Run	Default value of EC Index 15h/16h/17h is 7Fh
		01 Full Run	Default value of EC Index 15h/16h/17h is 00h
		00 75% Run	Default value of EC Index 15h/16h/17h is 20h
JP5 Pin 77	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK
JP6 Pin 60	SVID_EN	1	Disable SVID Function
		0	Enable SVID Function
JP7 Pin 97	Dual_BIOS_EN	1	Enable Dual BIOS Function for GigaByte Only
		0	Disable Dual BIOS Function for GigaByte Only

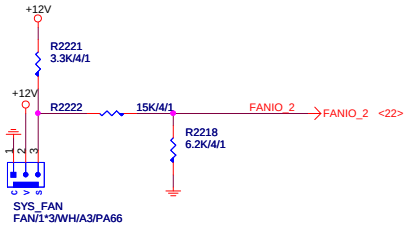
Hardware Monitor circuits

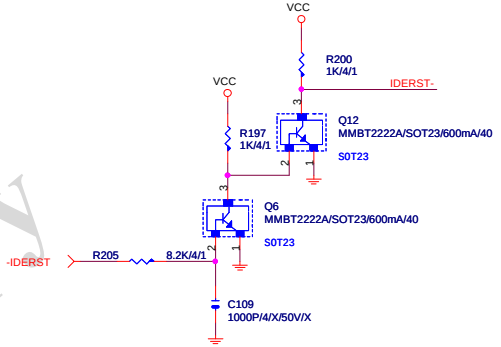




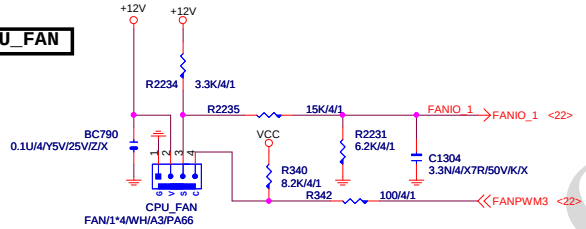


SYSTEM FAN

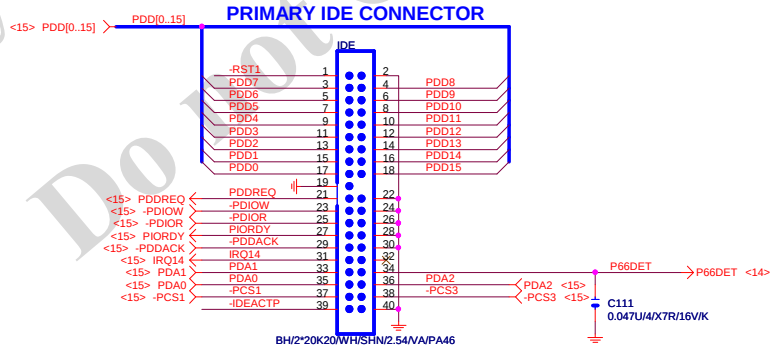




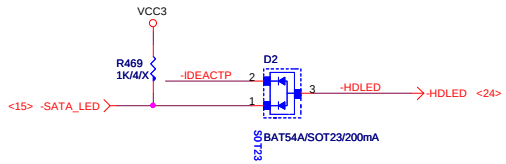
CPU_FAN



PRIMARY IDE CONNECTOR



Close to connector



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Title: FAN/HWMO, USB,IDE		
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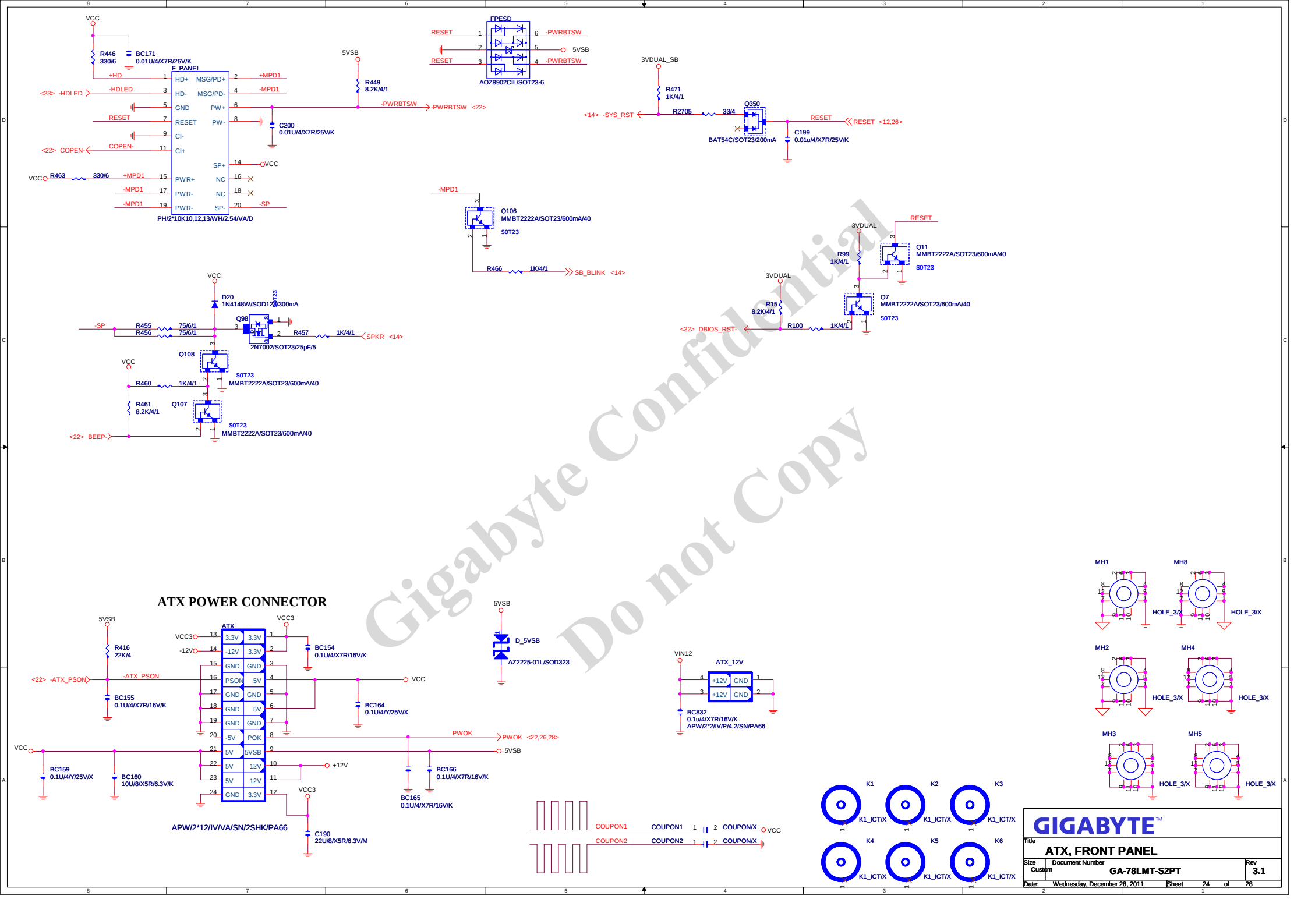

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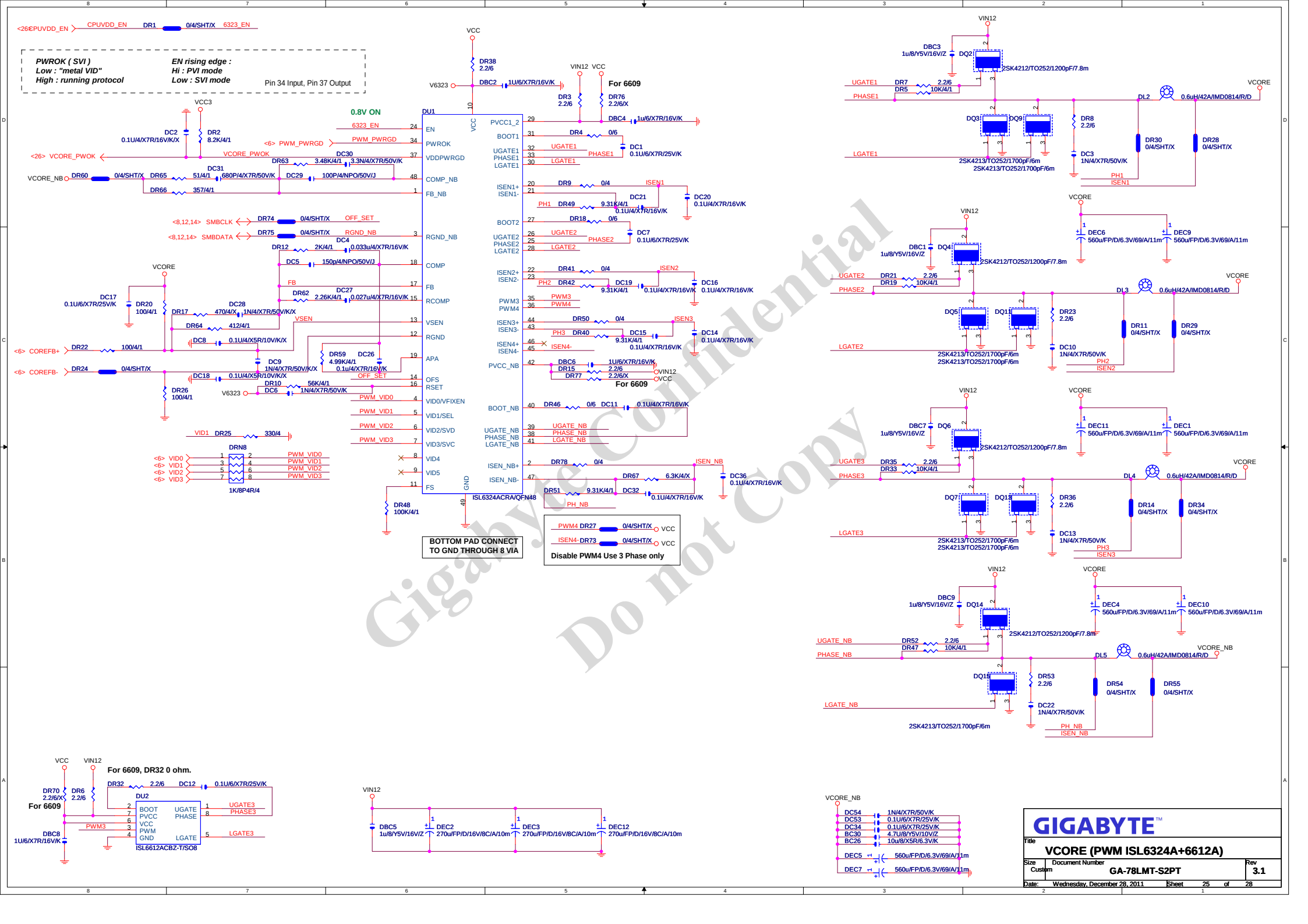
PWROK (SVI)
Low : "metal VID"
High : running protocol
EN rising edge :
Hi : PVI mode
Low : SVI mode
Pin 34 Input, Pin 37 Output
0.8V ON
DU1
ISL6324ACRA/QFN48
For 6609
BOTTOM PAD CONNECT TO GND THROUGH 8 VIA
Disable PWM4 Use 3 Phase only
DU2
ISL6612ACBZ-T/SO8
For 6609, DR32 0 ohm.
VCORE (PWM ISL6324A+6612A)
GA-78LMT-S2PT
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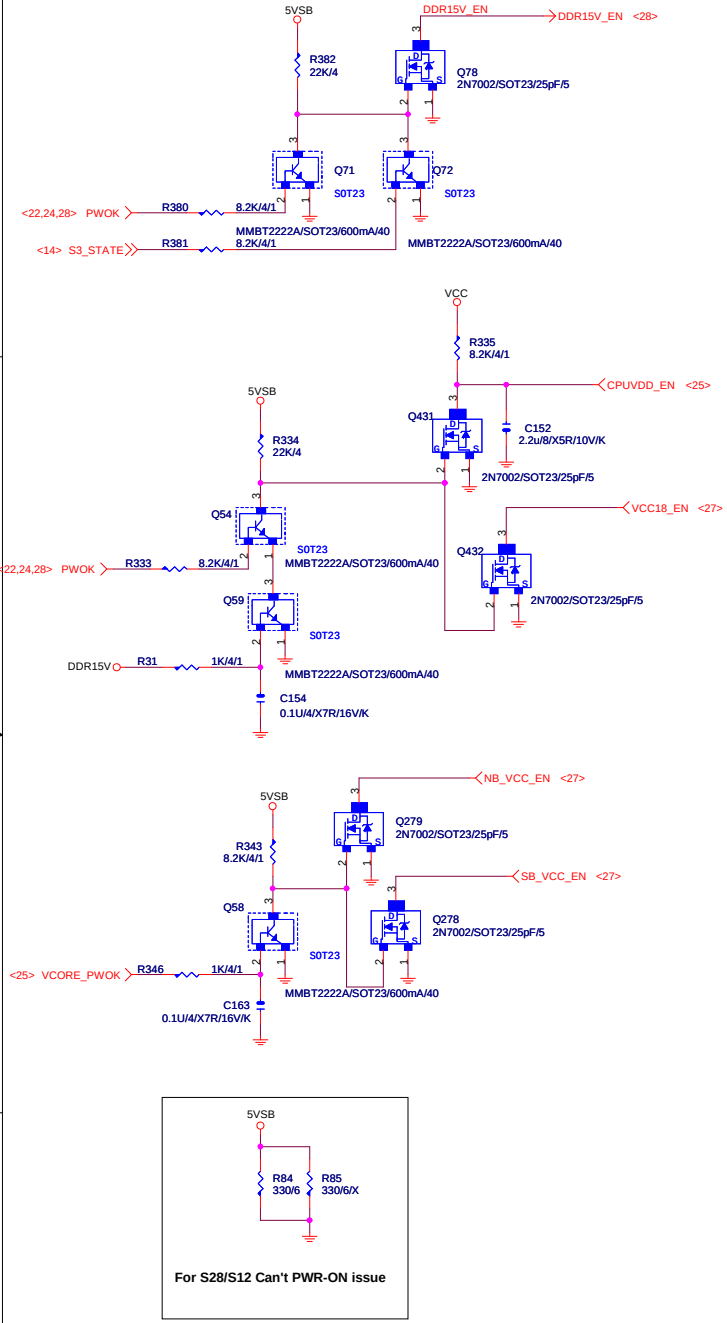

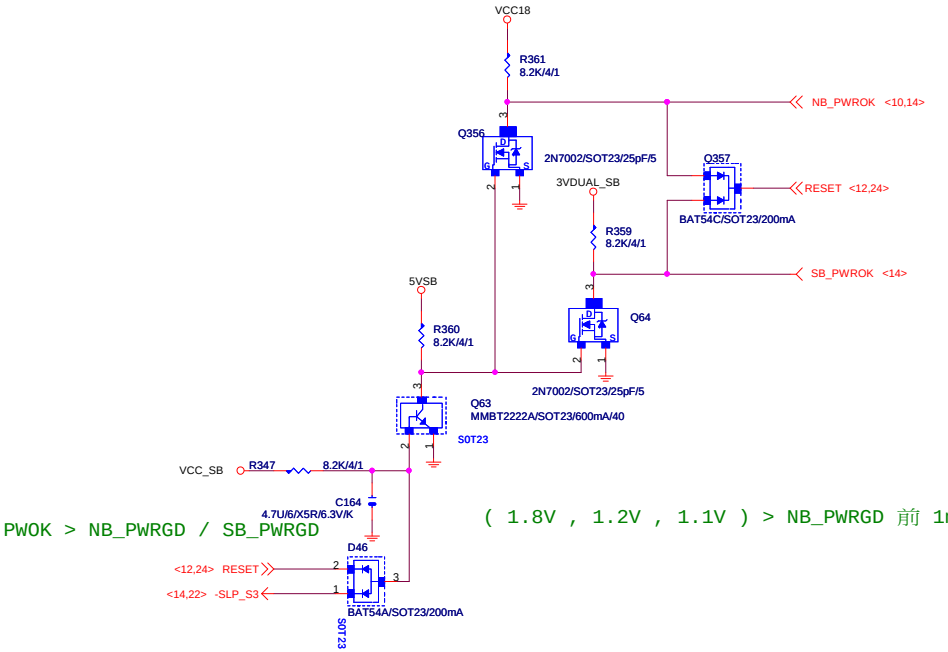

PWOK > NB_PWRGD / SB_PWRGD

(1.8V , 1.2V , 1.1V) > NB_PWRGD 前 1ms

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Title: POWER SEQUENCE		
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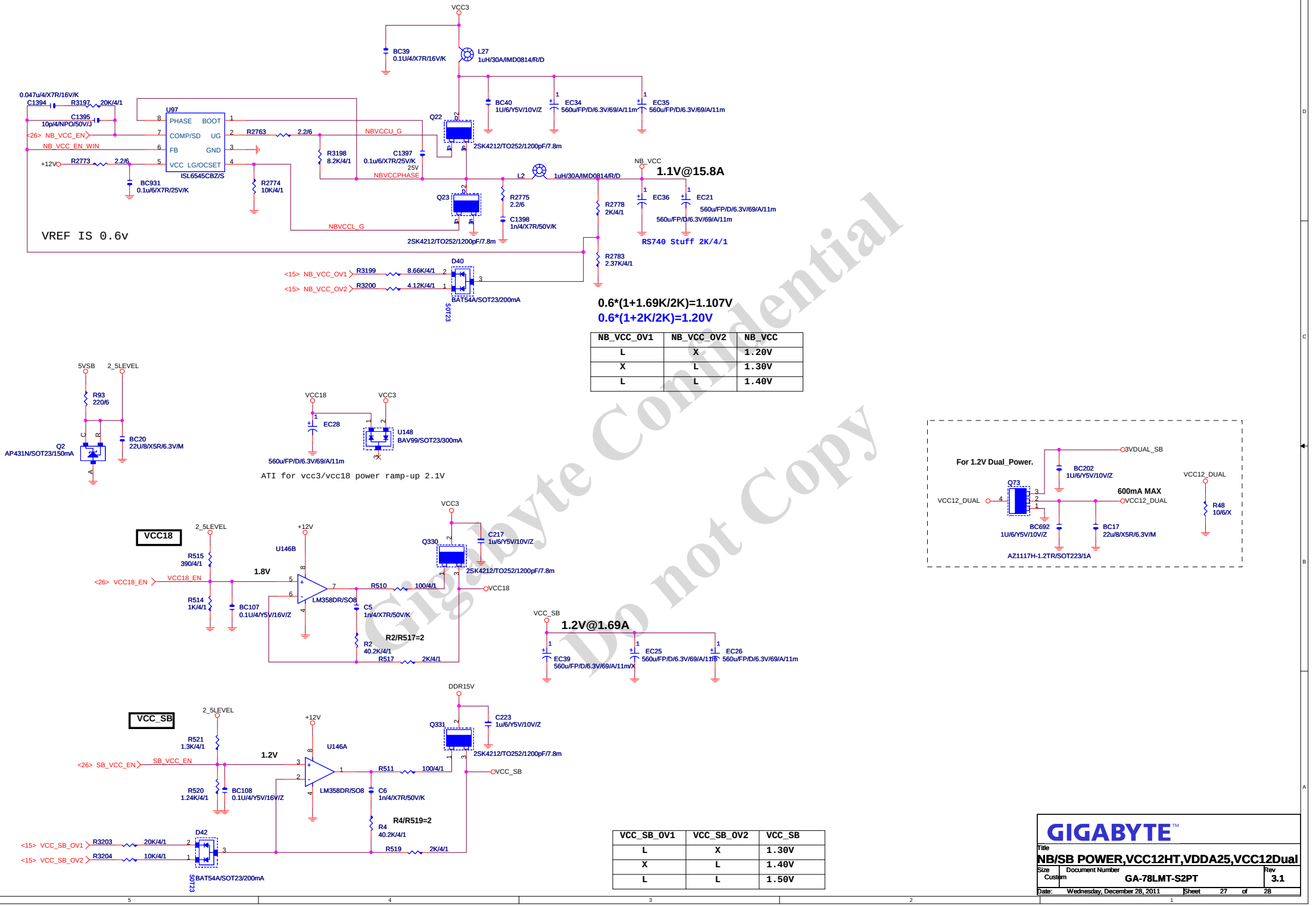

NB_VCC_OV1	NB_VCC_OV2	NB_VCC
L	X	1.20V
X	L	1.30V
L	L	1.40V

ATI for vcc3/vcc18 power ramp-up 2.1V

VCC_SB_OV1	VCC_SB_OV2	VCC_SB
L	X	1.30V
X	L	1.40V
L	L	1.50V

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Title	NB/SB POWER,VCC12HT,VDDA25,VCC12Dual	
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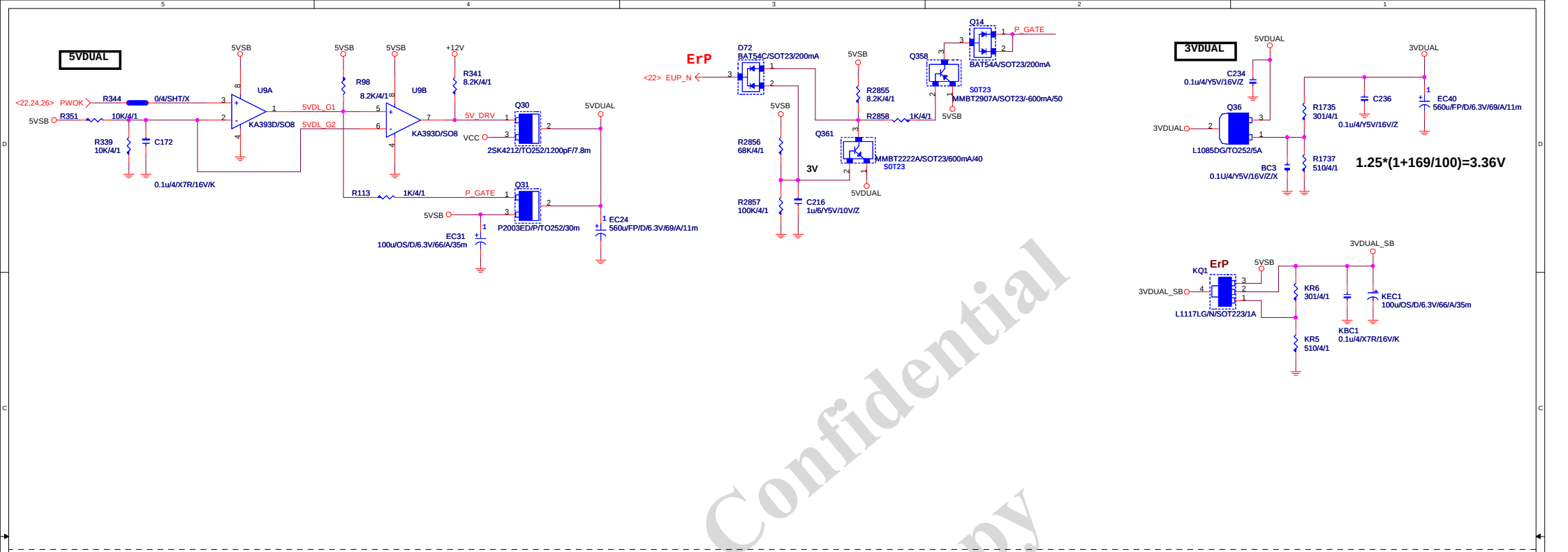

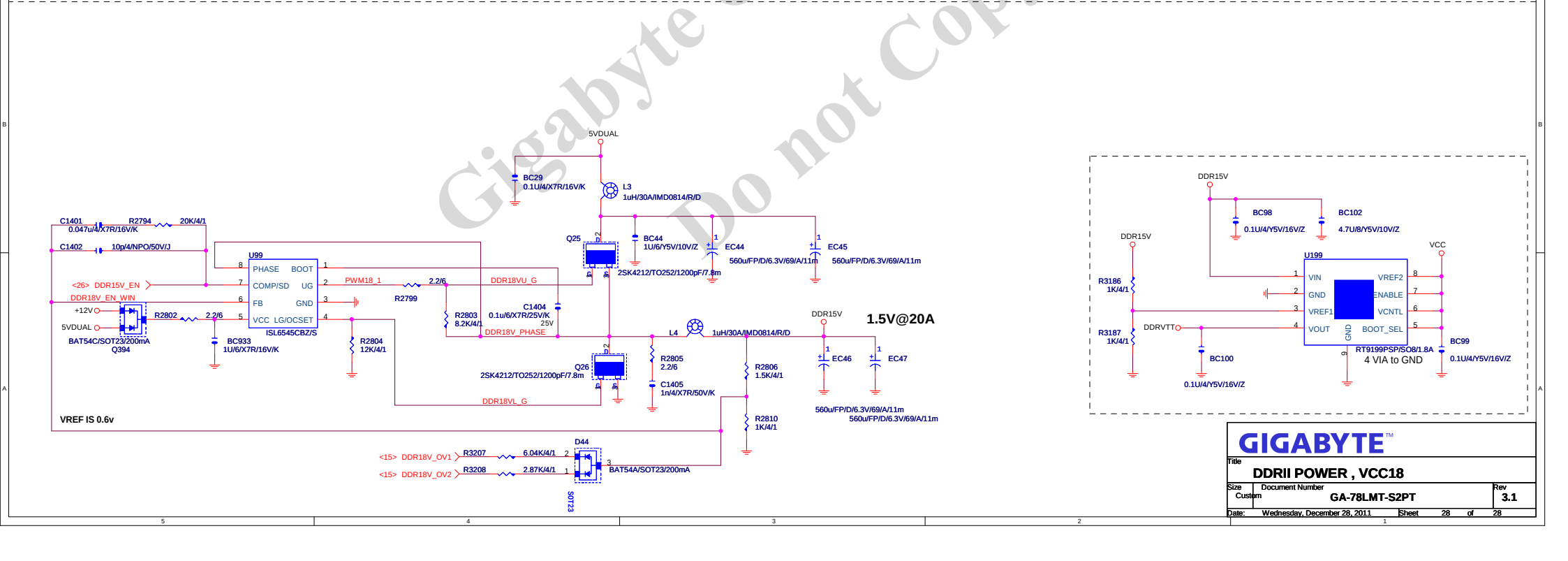

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Title: DDRII POWER , VCC18

Size	Document Number	Rev
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