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MS-7C13

ATX:226mm*185mm

Ver: 10

intel -CoffeeLake-S plamform

CPU:

LGA1151

*CPU POWER PAK *4Phase*

*GT POWER PAK *2 Phase*

System Chipset:

Kaby Lake H310C

Onboard Chip:

SIO: NCT5567D

HD Audio Codec: ALC887

LAN: RTL8111H

Flash ROM: SPI 128Mb/16 MB

DP to VGA: IT6516

PWM:

VCORE - RT3607

DDR - RT8231

DDR VPP25- MP2143

PCH(1.05V) - RT8125E

VCCSA - RT8125E

VCCIO - SY8288

Main Memory:

*DDR4 * 2 (Dual Channel)*

ACPI:

5VDAUL:uP7501

5VDIMM:uP7501

3VSB:MP2147

3VDSW: GS7133

VCCSTPLL:GS7133

Expansion Slots:

*PCI Express (X16) Slot * 1*

*PCI Express (X1) Slot * 2*

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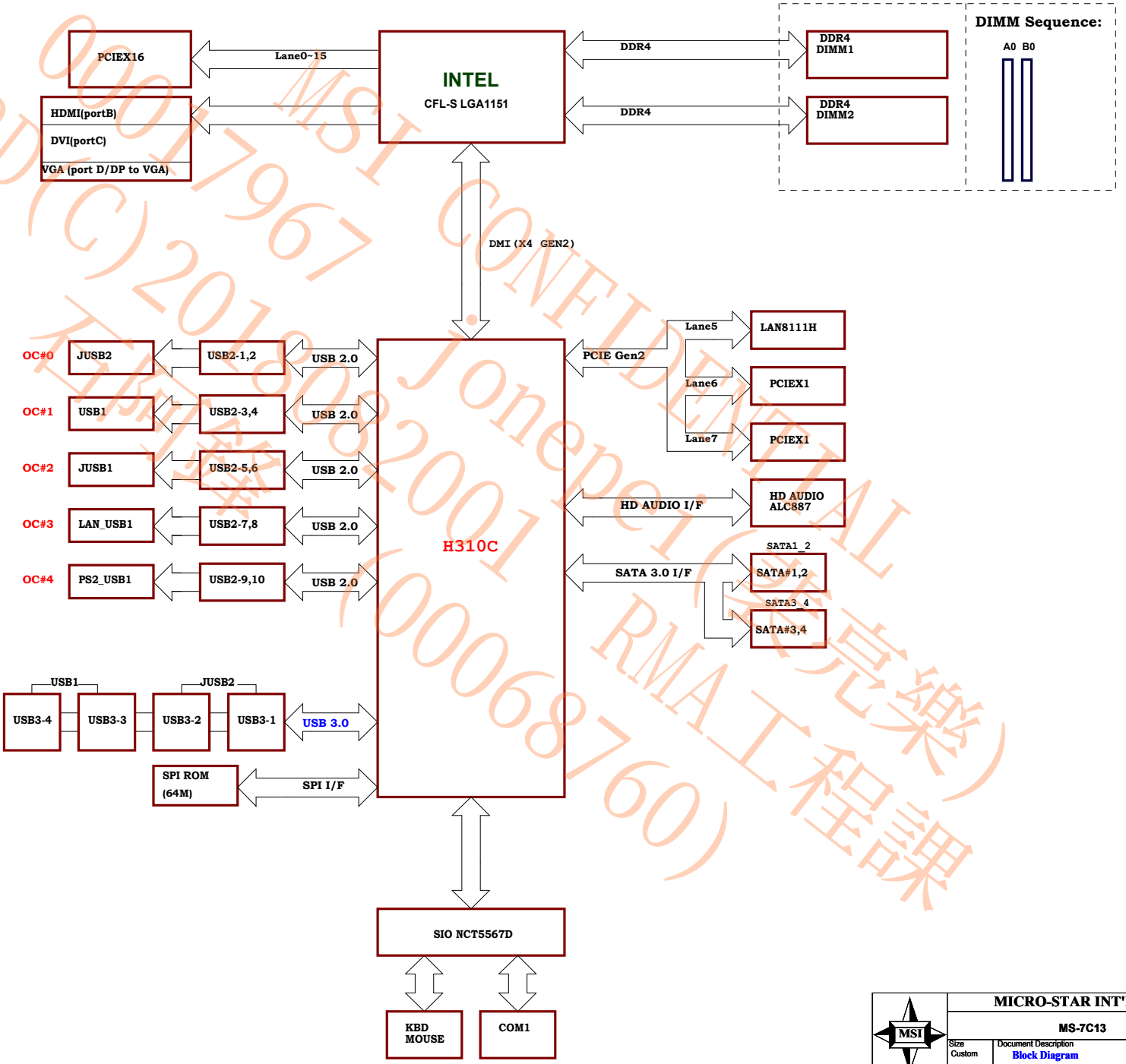
MS-7C13 Block Diagram



Slot Sequence:

PCIE X16	(By CPU GEN3)
PCIE X1	(By PCH GEN2)
PCIE X1	(By PCH GEN2)

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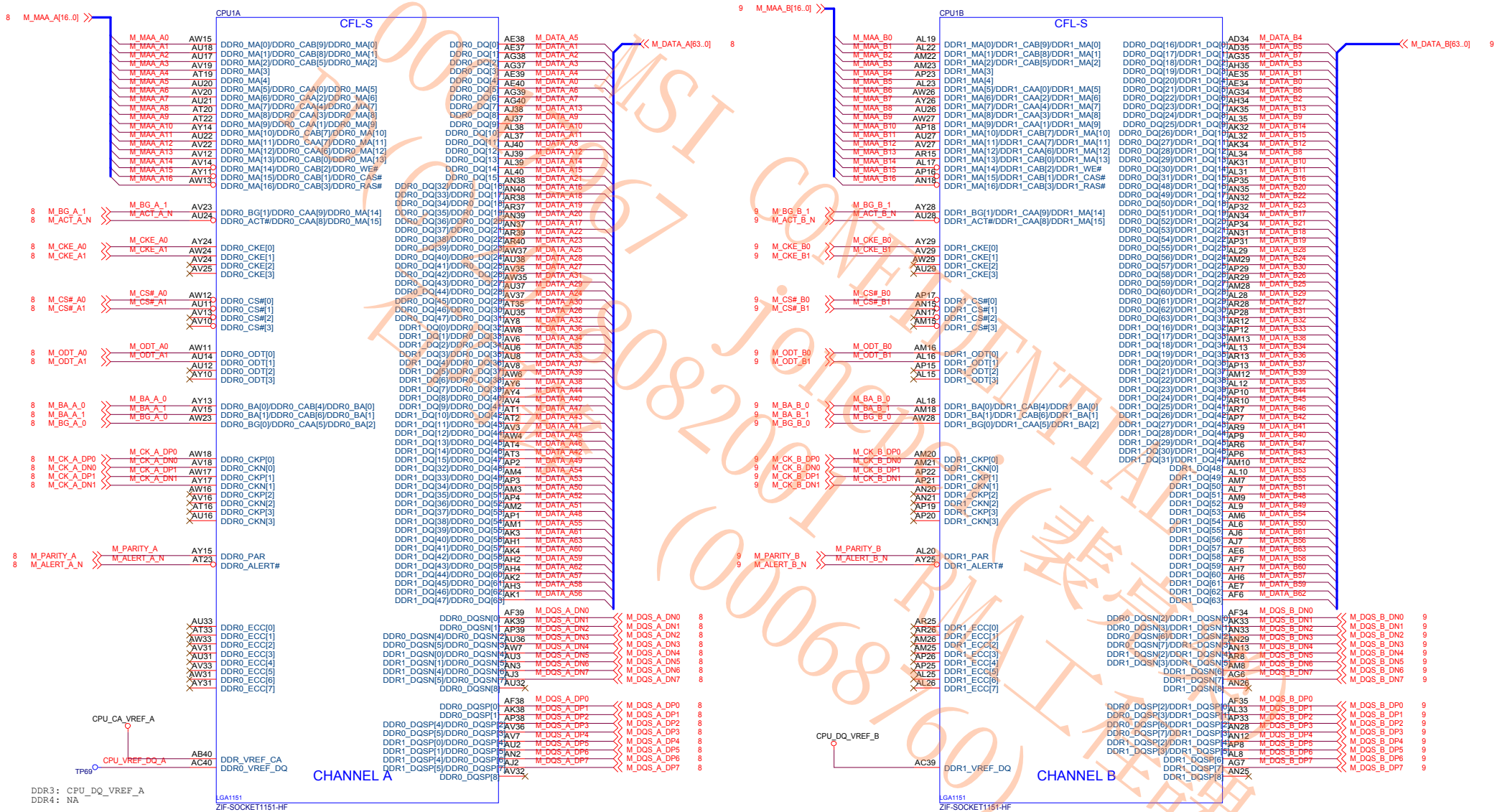

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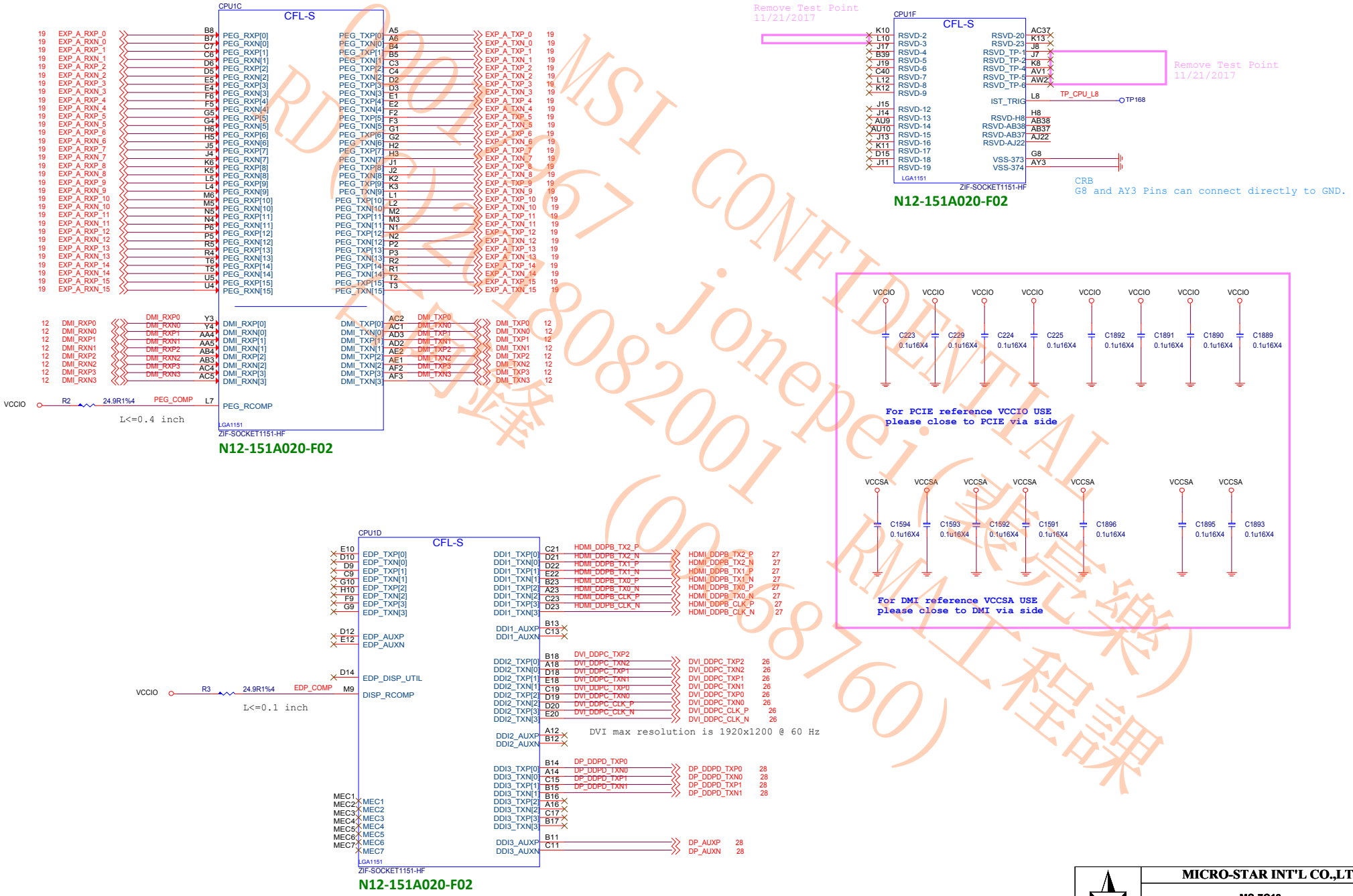
CPU1C
CFL-S
PEG_RXP[0]
PEG_RXN[0]
PEG_RXP[1]
PEG_RXN[1]
PEG_RXP[2]
PEG_RXN[2]
PEG_RXP[3]
PEG_RXN[3]
PEG_RXP[4]
PEG_RXN[4]
PEG_RXP[5]
PEG_RXN[5]
PEG_RXP[6]
PEG_RXN[6]
PEG_RXP[7]
PEG_RXN[7]
PEG_RXP[8]
PEG_RXN[8]
PEG_RXP[9]
PEG_RXN[9]
PEG_RXP[10]
PEG_RXN[10]
PEG_RXP[11]
PEG_RXN[11]
PEG_RXP[12]
PEG_RXN[12]
PEG_RXP[13]
PEG_RXN[13]
PEG_RXP[14]
PEG_RXN[14]
PEG_RXP[15]
PEG_RXN[15]
PEG_TXP[0]
PEG_TXN[0]
PEG_TXP[1]
PEG_TXN[1]
PEG_TXP[2]
PEG_TXN[2]
PEG_TXP[3]
PEG_TXN[3]
PEG_TXP[4]
PEG_TXN[4]
PEG_TXP[5]
PEG_TXN[5]
PEG_TXP[6]
PEG_TXN[6]
PEG_TXP[7]
PEG_TXN[7]
PEG_TXP[8]
PEG_TXN[8]
PEG_TXP[9]
PEG_TXN[9]
PEG_TXP[10]
PEG_TXN[10]
PEG_TXP[11]
PEG_TXN[11]
PEG_TXP[12]
PEG_TXN[12]
PEG_TXP[13]
PEG_TXN[13]
PEG_TXP[14]
PEG_TXN[14]
PEG_TXP[15]
PEG_TXN[15]
EXP_A_RXP_0
EXP_A_RXN_0
EXP_A_RXP_1
EXP_A_RXN_1
EXP_A_RXP_2
EXP_A_RXN_2
EXP_A_RXP_3
EXP_A_RXN_3
EXP_A_RXP_4
EXP_A_RXN_4
EXP_A_RXP_5
EXP_A_RXN_5
EXP_A_RXP_6
EXP_A_RXN_6
EXP_A_RXP_7
EXP_A_RXN_7
EXP_A_RXP_8
EXP_A_RXN_8
EXP_A_RXP_9
EXP_A_RXN_9
EXP_A_RXP_10
EXP_A_RXN_10
EXP_A_RXP_11
EXP_A_RXN_11
EXP_A_RXP_12
EXP_A_RXN_12
EXP_A_RXP_13
EXP_A_RXN_13
EXP_A_RXP_14
EXP_A_RXN_14
EXP_A_RXP_15
EXP_A_RXN_15
EXP_A_TXP_0
EXP_A_TXN_0
EXP_A_TXP_1
EXP_A_TXN_1
EXP_A_TXP_2
EXP_A_TXN_2
EXP_A_TXP_3
EXP_A_TXN_3
EXP_A_TXP_4
EXP_A_TXN_4
EXP_A_TXP_5
EXP_A_TXN_5
EXP_A_TXP_6
EXP_A_TXN_6
EXP_A_TXP_7
EXP_A_TXN_7
EXP_A_TXP_8
EXP_A_TXN_8
EXP_A_TXP_9
EXP_A_TXN_9
EXP_A_TXP_10
EXP_A_TXN_10
EXP_A_TXP_11
EXP_A_TXN_11
EXP_A_TXP_12
EXP_A_TXN_12
EXP_A_TXP_13
EXP_A_TXN_13
EXP_A_TXP_14
EXP_A_TXN_14
EXP_A_TXP_15
EXP_A_TXN_15
DMI_RXP0
DMI_RXN0
DMI_RXP1
DMI_RXN1
DMI_RXP2
DMI_RXN2
DMI_RXP3
DMI_RXN3
DMI_RXP[0]
DMI_RXN[0]
DMI_RXP[1]
DMI_RXN[1]
DMI_RXP[2]
DMI_RXN[2]
DMI_RXP[3]
DMI_RXN[3]
DMI_TXP[0]
DMI_TXN[0]
DMI_TXP[1]
DMI_TXN[1]
DMI_TXP[2]
DMI_TXN[2]
DMI_TXP[3]
DMI_TXN[3]
DMI_TXP0
DMI_TXN0
DMI_TXP1
DMI_TXN1
DMI_TXP2
DMI_TXN2
DMI_TXP3
DMI_TXN3
VCCIO
R2
24.9R1%4
PEG_COMP
L7
PEG_RCOMP
L<=0.4 inch
LGA1151
ZIF-SOCKET1151-HF
N12-151A020-F02
CPU1D
CFL-S
EDP_TXP[0]
EDP_TXN[0]
EDP_TXP[1]
EDP_TXN[1]
EDP_TXP[2]
EDP_TXN[2]
EDP_TXP[3]
EDP_TXN[3]
EDP_AUXP
EDP_AUXN
EDP_DISP_UTIL
EDP_COMP
DISP_RCOMP
R3
24.9R1%4
L<=0.1 inch
MEC1
MEC2
MEC3
MEC4
MEC5
MEC6
MEC7
DDI1_TXP[0]
DDI1_TXN[0]
DDI1_TXP[1]
DDI1_TXN[1]
DDI1_TXP[2]
DDI1_TXN[2]
DDI1_TXP[3]
DDI1_TXN[3]
DDI1_AUXP
DDI1_AUXN
DDI2_TXP[0]
DDI2_TXN[0]
DDI2_TXP[1]
DDI2_TXN[1]
DDI2_TXP[2]
DDI2_TXN[2]
DDI2_TXP[3]
DDI2_TXN[3]
DDI2_AUXP
DDI2_AUXN
DDI3_TXP[0]
DDI3_TXN[0]
DDI3_TXP[1]
DDI3_TXN[1]
DDI3_TXP[2]
DDI3_TXN[2]
DDI3_TXP[3]
DDI3_TXN[3]
DDI3_AUXP
DDI3_AUXN
HDMI_DDPB_TX2_P
HDMI_DDPB_TX2_N
HDMI_DDPB_TX1_P
HDMI_DDPB_TX1_N
HDMI_DDPB_TX0_P
HDMI_DDPB_TX0_N
HDMI_DDPB_CLK_P
HDMI_DDPB_CLK_N
DVI_DDPC_TXP2
DVI_DDPC_TXN2
DVI_DDPC_TXP1
DVI_DDPC_TXN1
DVI_DDPC_TXP0
DVI_DDPC_TXN0
DVI_DDPC_CLK_P
DVI_DDPC_CLK_N
DVI max resolution is 1920x1200 @ 60 Hz
DP_DDPD_TXP0
DP_DDPD_TXN0
DP_DDPD_TXP1
DP_DDPD_TXN1
DP_AUXP
DP_AUXN
LGA1151
ZIF-SOCKET1151-HF
N12-151A020-F02
Remove Test Point
11/21/2017
CPU1F
CFL-S
RSVD-2
RSVD-3
RSVD-4
RSVD-5
RSVD-6
RSVD-7
RSVD-8
RSVD-9
RSVD-12
RSVD-13
RSVD-14
RSVD-15
RSVD-16
RSVD-17
RSVD-18
RSVD-19
RSVD-20
RSVD-23
RSVD_TP-1
RSVD_TP-2
RSVD_TP-4
RSVD_TP-5
RSVD_TP-6
IST_TRIG
RSVD-H8
RSVD-AB38
RSVD-AB37
RSVD-AJ22
VSS-373
VSS-374
TP_CPU_L8
TP168
LGA1151
ZIF-SOCKET1151-HF
N12-151A020-F02
Remove Test Point
11/21/2017
CRB
G8 and AY3 Pins can connect directly to GND.
VCCIO
C223 0.1u16X4
C229 0.1u16X4
C224 0.1u16X4
C225 0.1u16X4
C1892 0.1u16X4
C1891 0.1u16X4
C1890 0.1u16X4
C1889 0.1u16X4
For PCIE reference VCCIO USE
please close to PCIE via side
VCCSA
C1594 0.1u16X4
C1593 0.1u16X4
C1592 0.1u16X4
C1591 0.1u16X4
C1896 0.1u16X4
C1895 0.1u16X4
C1893 0.1u16X4
For DMI reference VCCSA USE
please close to DMI via side
MICRO-STAR INT'L CO.,LTD
MS-7C13
Size
Custom
Document Description
CPU-PEG/Display
Rev
10
Date: Monday, June 25, 2018
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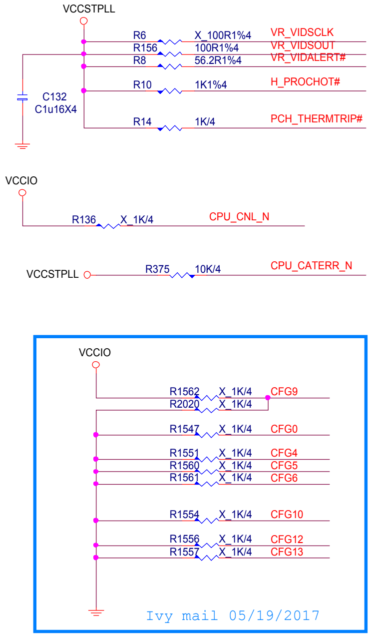

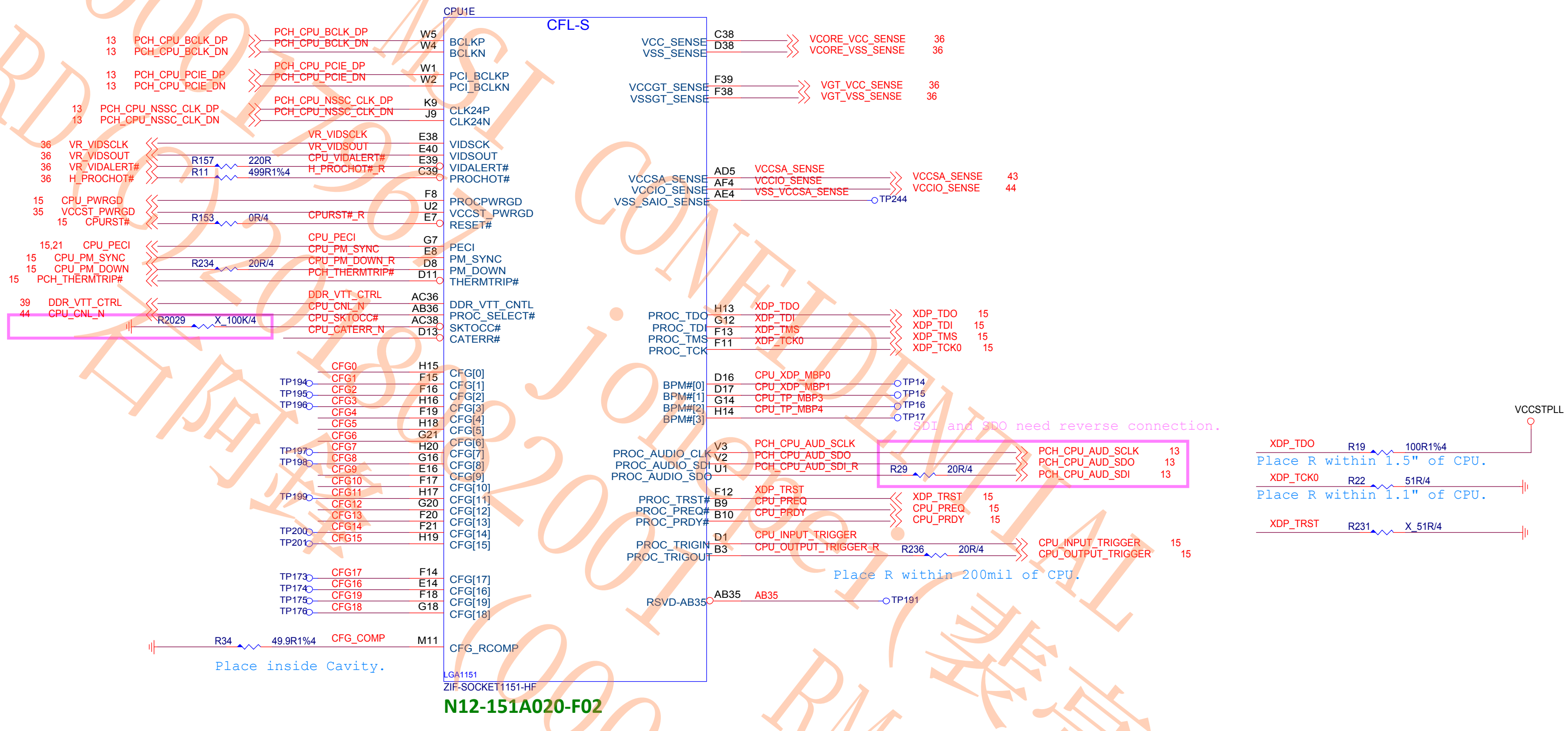

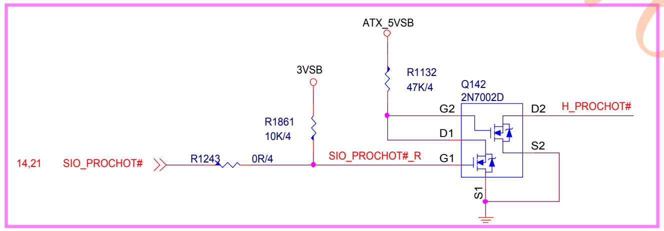

	CFG Table		
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG_DEFER_TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		

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MS-7C13

Size	Document Description	Rev
Custom	CPU-Power	10

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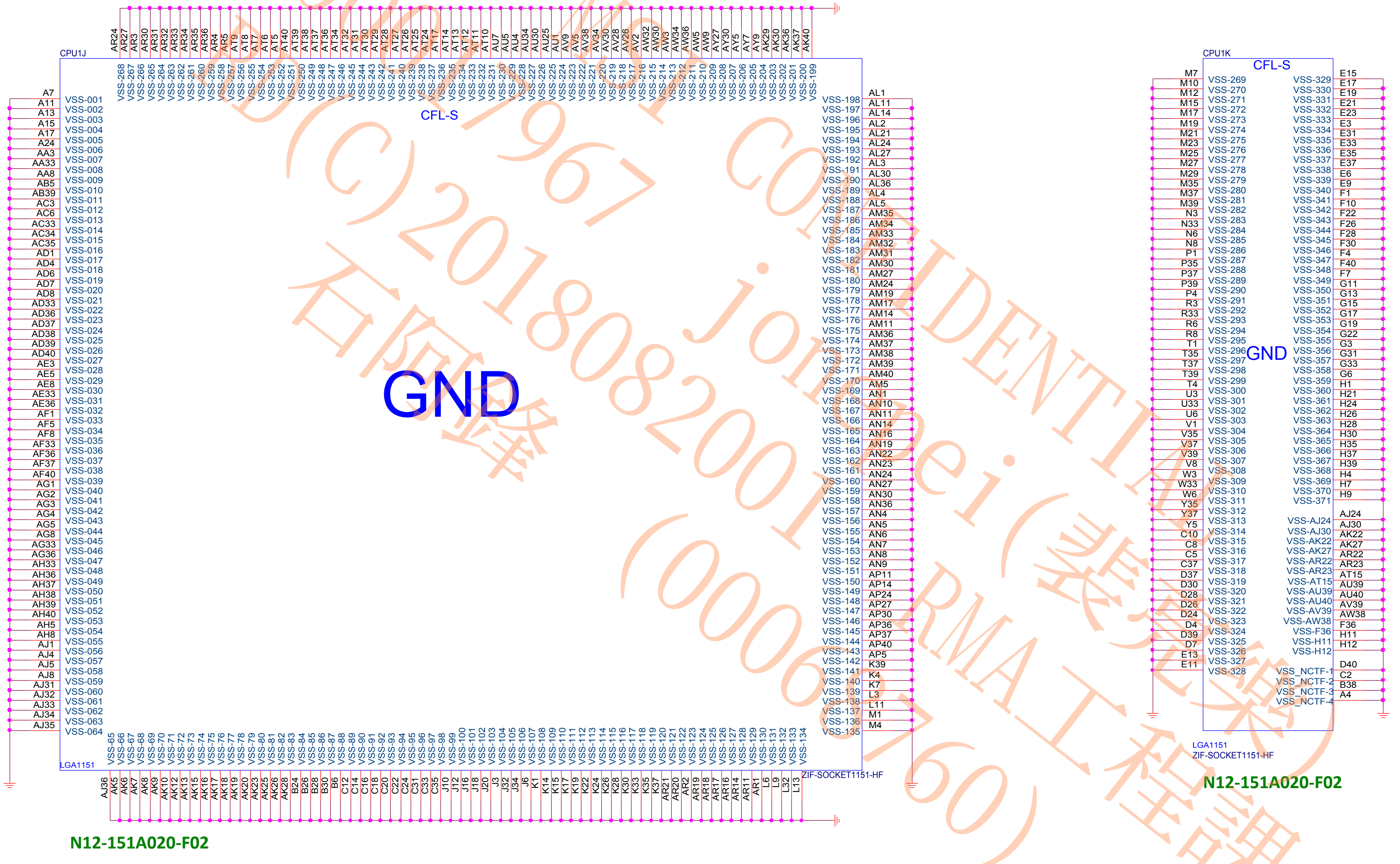
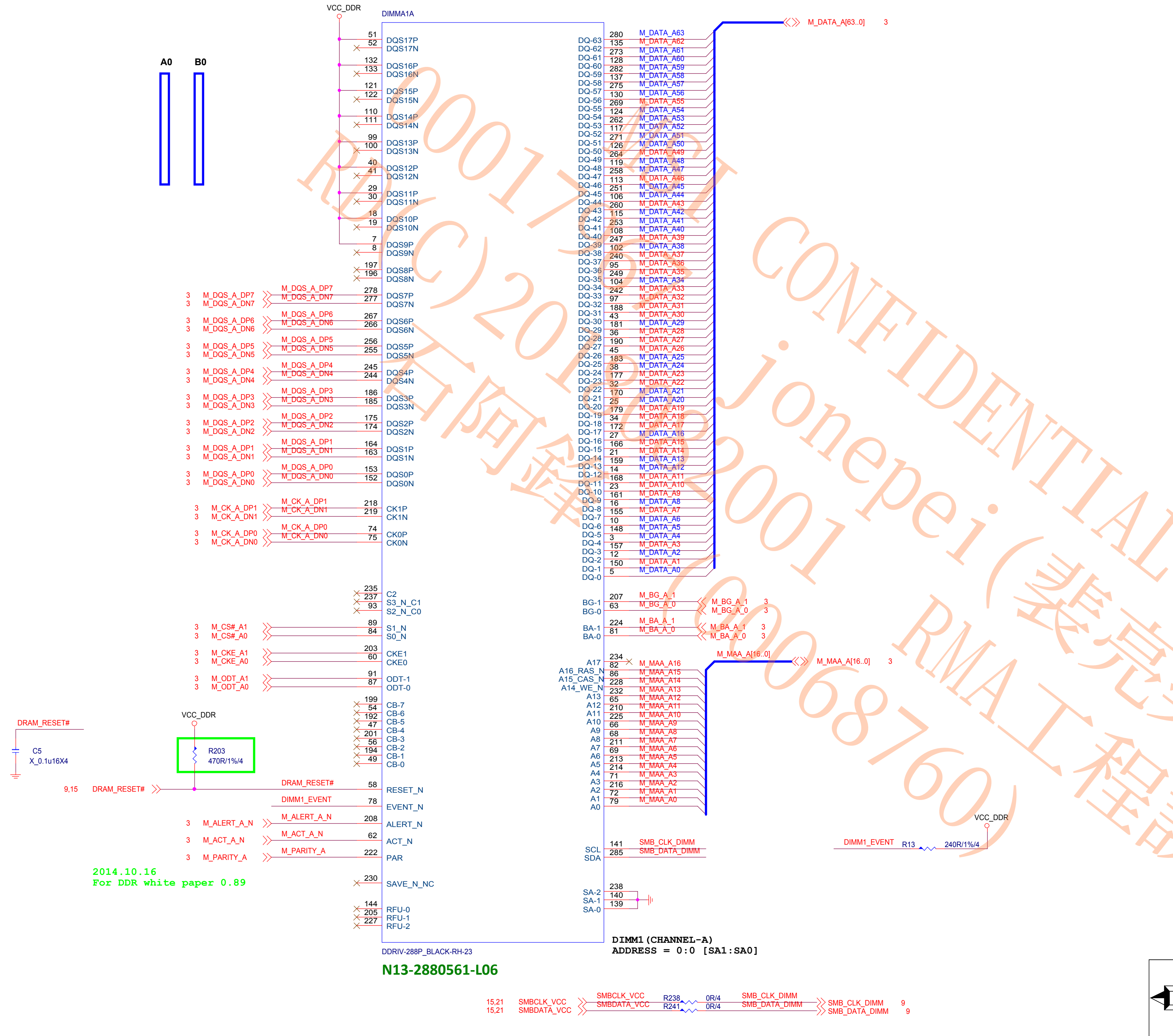
RD(C)2018082001 石向鋒
(00068760) RMA工程課 Jonepei(裴亮樂)



MSI CONFIDENTIAL
00007967 johnpei(裴覺榮)
(C)201808200(000617960)
RMA工程課
石福隆

MICRO-STAR INT'L CO.,LTD		
MS-7C13		
Size: Custom	Document Description: CPU-GND	Rev: 10
Date: Monday, June 25, 2018	Sheet 7 of 53	



00017 MSI CONFIDENTIAL
RD (C) 2018/02/2001 Jonepei(裴亮樂) (00068760) RMA工程課
石向鋒

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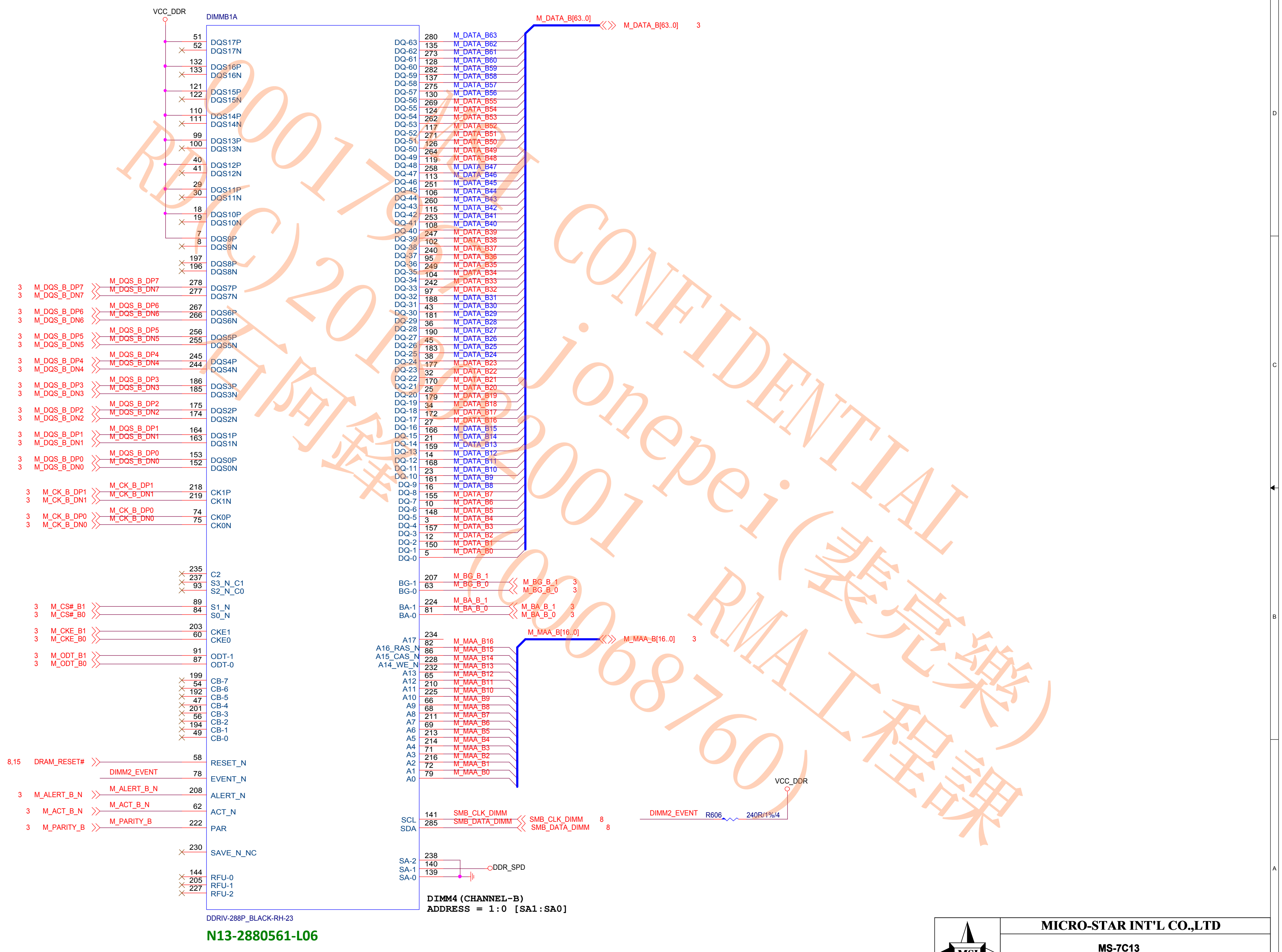
MS-7C13		
Size: Custom	Document Description: DDR4 DIMM 1	Rev: 10
Date: Monday, June 25, 2018	Sheet 8 of 53	



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MS-7C13

Size	Document Description	Rev
Custom	DDR4 DIMM 2	10

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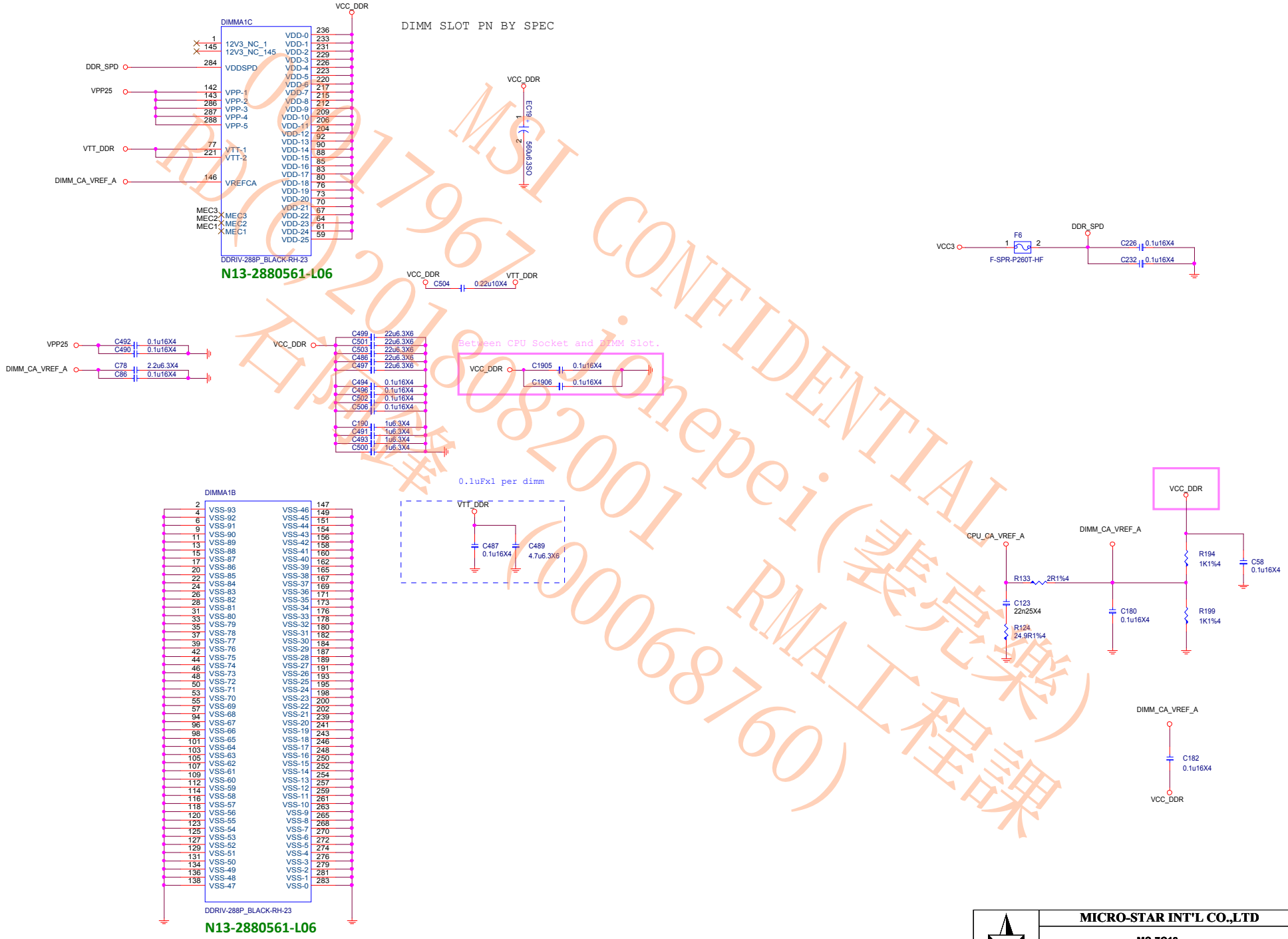
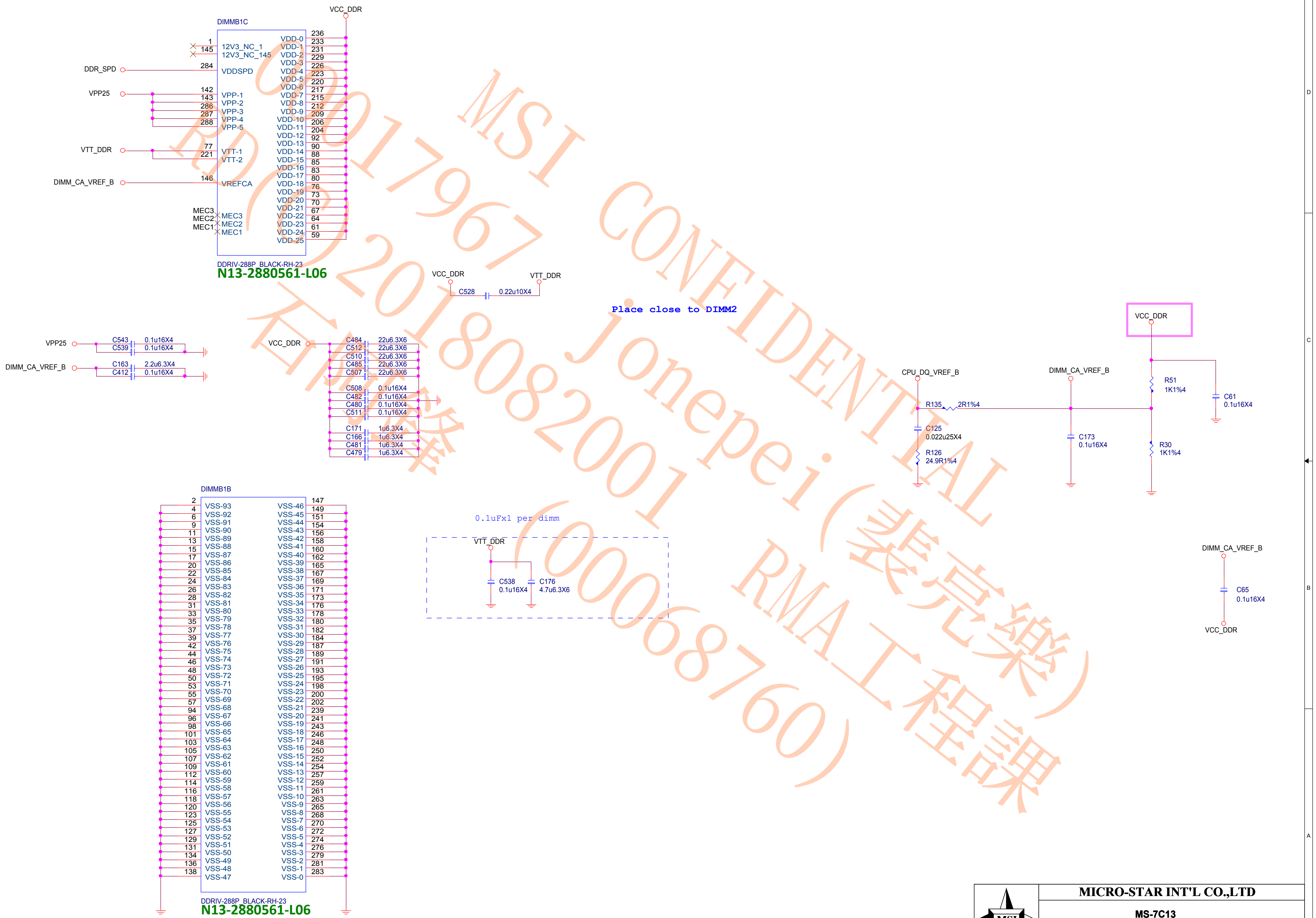


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C13	
Size: Custom	Document Description: DDR4-POWER/GND-1	Rev: 10
Date: Monday, June 25, 2018	Sheet 10 of 53	



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Jonepei(裴亮樂) RMA工程課 (00068760)
(00017967) 2018082001
RD(石)

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MS-7C13

Size	Document Description	Rev
Custom	DDR4-POWER/GND-2	10

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H310C Note:Polarity inversion and lane reversal on DMI link is not allowed.
2018/5/30 modify.

DMI

PCH1B

4 DMI_TXP0 → N27 DMI_RXP0
4 DMI_TXN0 → L27 DMI_RXN0
4 DMI_TXP1 → G24 DMI_RXP1
4 DMI_TXN1 → E24 DMI_RXN1
4 DMI_TXP2 → E26 DMI_RXP2
4 DMI_TXN2 → G27 DMI_RXN2
4 DMI_TXP3 → K29 DMI_RXP3
4 DMI_TXN3 → L29 DMI_RXN3

C27 DMI_TXP0 → D27 DMI_RXN0 → 4 DMI_RXP0 4
D27 DMI_TXN0 → A28 DMI_RXP0 → 4 DMI_RXN0 4
A28 DMI_TXP1 → B27 DMI_RXN1 → 4 DMI_RXP1 4
B27 DMI_TXN1 → C28 DMI_RXP1 → 4 DMI_RXN1 4
C28 DMI_TXP2 → B28 DMI_RXN2 → 4 DMI_RXP2 4
B28 DMI_TXN2 → B29 DMI_RXP2 → 4 DMI_RXN2 4
B29 DMI_TXP3 → C29 DMI_RXN3 → 4 DMI_RXP3 4
C29 DMI_TXN3 → 4 DMI_RXN3 4

PCIE

H310C don't support PCIe port 1~4

E15 PCIE1_RXP / USB3_7_RXP
G15 PCIE1_RXN / USB3_7_RXN
G17 PCIE2_RXP / USB3_8_RXP
E17 PCIE2_RXN / USB3_8_RXN
K17 PCIE3_RXP / USB3_9_RXP
L17 PCIE3_RXN / USB3_9_RXN
G19 PCIE4_RXP / USB3_10_RXP
E19 PCIE4_RXN / USB3_10_RXN

B18 PCIE1_TXP / USB3_7_TXP
A18 PCIE1_TXN / USB3_7_TXN
C19 PCIE2_TXP / USB3_8_TXP
B19 PCIE2_TXN / USB3_8_TXN
C20 PCIE3_TXP / USB3_9_TXP
B20 PCIE3_TXN / USB3_9_TXN
A21 PCIE4_TXP / USB3_10_TXP
B21 PCIE4_TXN / USB3_10_TXN

H310C don't support PCIe port 1~4

25 PE5_LAN_RX → L19 PCIE5_RXP
25 PE5_LAN_RX# → K19 PCIE5_RXN
20 PE6_X1_RX → E22 PCIE6_RXP
20 PE6_X1_RX# → G22 PCIE6_RXN
20 PE7_X1_RX → K22 PCIE7_RXP
20 PE7_X1_RX# → L22 PCIE7_RXN
L24 PCIE8_RXP
K24 PCIE8_RXN

C22 PCIE5_TXP → D22 PCIE5_TXN → PE5_LAN_TX 25
A23 PCIE6_TXP → B22 PCIE6_TXN → PE5_LAN_TX# 25
B23 PCIE7_TXP → C23 PCIE7_TXN → PE6_X1_TX 20
B24 PCIE8_TXP → C24 PCIE8_TXN → PE6_X1_TX# 20
PE7_X1_TX 20
PE7_X1_TX# 20

H310C port 9 only support intel LAN
H310C don't support PCIe port 10

H31 PCIE9_RXP / SATA0A_RXP
G31 PCIE9_RXN / SATA0A_RXN
E29 PCIE10_RXP / SATA1A_RXP
G29 PCIE10_RXN / SATA1A_RXN
K31 PCIE11_RXP
L31 PCIE11_RXN
G33 PCIE12_RXP
E33 PCIE12_RXN

C31 PCIE9_TXP / SATA0A_TXP
D31 PCIE9_TXN / SATA0A_TXN
A32 PCIE10_TXP / SATA1A_TXP
B31 PCIE10_TXN / SATA1A_TXN
B32 PCIE11_TXP
C32 PCIE11_TXN
B33 PCIE12_TXP
C33 PCIE12_TXN

H310C port 9 only support intel LAN
H310C don't support PCIe port 10

31 SATA0_RX → E35 PCIE13_RXP / SATA0B_RXP
31 SATA0_RX# → G35 PCIE13_RXN / SATA0B_RXN
31 SATA1_RX → G37 PCIE14_RXP / SATA1B_RXP
31 SATA1_RX# → E37 PCIE14_RXN / SATA1B_RXN
31 SATA2_RX → C42 PCIE15_RXP / SATA2_RXP
31 SATA2_RX# → E41 PCIE15_RXN / SATA2_RXN
31 SATA3_RX → E43 PCIE16_RXP / SATA3_RXP
31 SATA3_RX# → D42 PCIE16_RXN / SATA3_RXN

H310C only SATA

B36 PCIE13_TXP / SATA0B_TXP → SATA0_TX 31
C36 PCIE13_TXN / SATA0B_TXN → SATA0_TX# 31
B37 PCIE14_TXP / SATA1B_TXP → SATA1_TX 31
A37 PCIE14_TXN / SATA1B_TXN → SATA1_TX# 31
B38 PCIE15_TXP / SATA2_TXP → SATA2_TX 31
C38 PCIE15_TXN / SATA2_TXN → SATA2_TX# 31
A39 PCIE16_TXP / SATA3_TXP → SATA3_TX 31
B39 PCIE16_TXN / SATA3_TXN → SATA3_TX# 31

H310C only SATA

K39 PCIE17_RXP / SATA4_RXP
J41 PCIE17_RXN / SATA4_RXN
M41 PCIE18_RXP / SATA5_RXP
M39 PCIE18_RXN / SATA5_RXN
P41 PCIE19_RXP
P39 PCIE19_RXN
P36 PCIE20_RXP
P38 PCIE20_RXN

F45 PCIE17_TXP / SATA4_TXP
E45 PCIE17_TXN / SATA4_TXN
Y44 PCIE18_TXP / SATA5_TXP
G45 PCIE18_TXN / SATA5_TXN
H45 PCIE19_TXP
H44 PCIE19_TXN
J44 PCIE20_TXP
J43 PCIE20_TXN

H310C don't support PCIe port 17~24

T41 PCIE_21_RXP
T36 PCIE_21_RXN
V36 PCIE_22_RXP
V35 PCIE_22_RXN
V41 PCIE_23_RXP
V39 PCIE_23_RXN
Y41 PCIE_24_RXP
Y39 PCIE_24_RXN

K44 PCIE_21_TXP
K43 PCIE_21_TXN
L44 PCIE_22_TXP
L43 PCIE_22_TXN
N45 PCIE_23_TXP
N44 PCIE_23_TXN
P44 PCIE_24_TXP
P43 PCIE_24_TXN

C10 PCIE_RCOMPP
B10 PCIE_RCOMPN
PCIECOMP_P
PCIECOMP_N
R285 100R1%4

PCIECOMP_P
PCIECOMP_N
Length Match < 5mil

TP246 GPP_E4 AL44 GPP_E4 / DEVSLP0
TP247 GPP_E5 AL45 GPP_E5 / DEVSLP1
TP228 GPP_E6 AK44 GPP_E6 / DEVSLP2
TP70 GPP_F5 AF44 GPP_F5 / DEVSLP3
TP73 GPP_F6 AG41 GPP_F6 / DEVSLP4
TP72 GPP_F7 AH39 GPP_F7 / DEVSLP5
GPP_F8 AH36 GPP_F8 / DEVSLP6
GPP_F9 AF45 GPP_F9 / DEVSLP7

GFX_CRB_DETECT AE43 GPP_F13 / SDATAOUT0
SV_ADVANCE AE44 GPP_F12 / SDATAOUT1
PCH_RSVD AH35 GPP_F11 / SLOAD
PCH_CONFIG AE30 GPP_F10 / SCLOCK

GPP_E8 / SATALED# AJ44 PCH_SATA_LED# → PCH_SATA_LED# 45
SMI Pin
R489 10K/4 VCC3

AM36 GPP_E0 / SATAXPCIE0 / SATAGP0 GPP_E0
AM35 GPP_E1 / SATAXPCIE1 / SATAGP1 GPP_E1
AM38 GPP_E2 / SATAXPCIE2 / SATAGP2 GPP_E2
AK36 GPP_F0 / SATAXPCIE3 / SATAGP3 GPP_F0
AK33 GPP_F1 / SATAXPCIE4 / SATAGP4 GPP_F1
AK38 GPP_F2 / SATAXPCIE5 / SATAGP5 GPP_F2
AH43 GPP_F3 / SATAXPCIE6 / SATAGP6
AE42 GPP_F4 / SATAXPCIE7 / SATAGP7

PCH_H310C

OB1-7C10001-I06

USB3

PCH1C

30 MB_USB30_RX1+ → A7 USB3_1_RXP
30 MB_USB30_RX1- → B7 USB3_1_RXN
30 MB_USB30_RX2+ → B8 USB3_2_SSIC_1_RXP
30 MB_USB30_RX2- → C8 USB3_2_SSIC_1_RXN
30 MB_USB30_RX3+ → A9 USB3_3_SSIC_2_RXP
30 MB_USB30_RX3- → B9 USB3_3_SSIC_2_RXN
30 MB_USB30_RX4+ → G11 USB3_4_RXP
30 MB_USB30_RX4- → E11 USB3_4_RXN
G13 USB3_5_RXP
E13 USB3_5_RXN
K15 USB3_6_RXP
H15 USB3_6_RXN

H310C don't support USB3.0 5~6

C13 USB3_1_TXP → D13 USB3_1_TXN → A14 USB3_2_SSIC_1_TXP → B13 USB3_2_SSIC_1_TXN → C14 USB3_3_SSIC_2_TXP → B14 USB3_3_SSIC_2_TXN → C15 USB3_4_TXP → B15 USB3_4_TXN → B16 USB3_5_TXP → A16 USB3_5_TXN → D17 USB3_6_TXP → C17 USB3_6_TXN

MB_USB30_TX1+ 30
MB_USB30_TX1- 30
MB_USB30_TX2+ 30
MB_USB30_TX2- 30
MB_USB30_TX3+ 30
MB_USB30_TX3- 30
MB_USB30_TX4+ 30
MB_USB30_TX4- 30

JUSB2
USB1

H310C don't support USB3.0 5~6

USB2

29 OC#0 → AJ43 OC#0 → GPP_E9 / USB_OC0#
29 OC#1 → AH44 OC#1 → GPP_E10 / USB_OC1#
29 OC#2 → AM39 OC#2 → GPP_E11 / USB_OC2#
29 OC#3 → AK42 OC#3 → GPP_E12 / USB_OC3#
29 OC#4 → AD43 OC#4 → GPP_F15 / USB_OCB4#
AC44 OC#5 → GPP_F16 / USB_OCB5#
AH42 OC#6 → GPP_F17 / USB_OC6#
AC43 OC#7 → GPP_F18 / USB_OC7#

AH7 USB2P_1 → MB_USB_1D+ 30
AH5 USB2N_1 → MB_USB_1D- 30
AE7 USB2P_2 → MB_USB_2D+ 30
AE5 USB2N_2 → MB_USB_2D- 30
AH10 USB2P_3 → MB_USB_3D+ 30
AH8 USB2N_3 → MB_USB_3D- 30
AE3 USB2P_4 → MB_USB_4D+ 30
AE2 USB2N_4 → MB_USB_4D- 30

AC3 USB2P_5 → MB_USB_5D+ 29
AC2 USB2N_5 → MB_USB_5D- 29
AF1 USB2P_6 → MB_USB_6D+ 29
AF2 USB2N_6 → MB_USB_6D- 29
AB1 USB2P_7 → MB_USB_7D+ 29
AB2 USB2N_7 → MB_USB_7D- 29
AM7 USB2P_8 → MB_USB_8D+ 29
AM8 USB2N_8 → MB_USB_8D- 29

Y2 USB2P_9 → MB_USB_9D+ 29
Y3 USB2N_9 → MB_USB_9D- 29
AK7 USB2P_10 → MB_USB_10D+ 29
AK8 USB2N_10 → MB_USB_10D- 29
W1 USB2P_11
W2 USB2N_11
AD2 USB2P_12
AD3 USB2N_12
V2 USB2P_13
V3 USB2N_13
AK13 USB2P_14
AK11 USB2N_14

JUSB2
USB1
LAN_USB1
PS2_USB1

H310C don't support USB2.0 11~14

R284 0R0402 USB2_ID → AG2 USB2_ID
R283 10KR0402 USB2_VBUSSENSE → AE10 USB2_VBUSSENSE
R286 113R1% USB2_COMP → AG3 USB2_COMP

USB2_COMP <1000 mil

PCH_H310C

OB1-7C10001-I06

3VSB
R1842 10K/4 OC#5
R27 10K/4 OC#6
R33 10K/4 OC#7

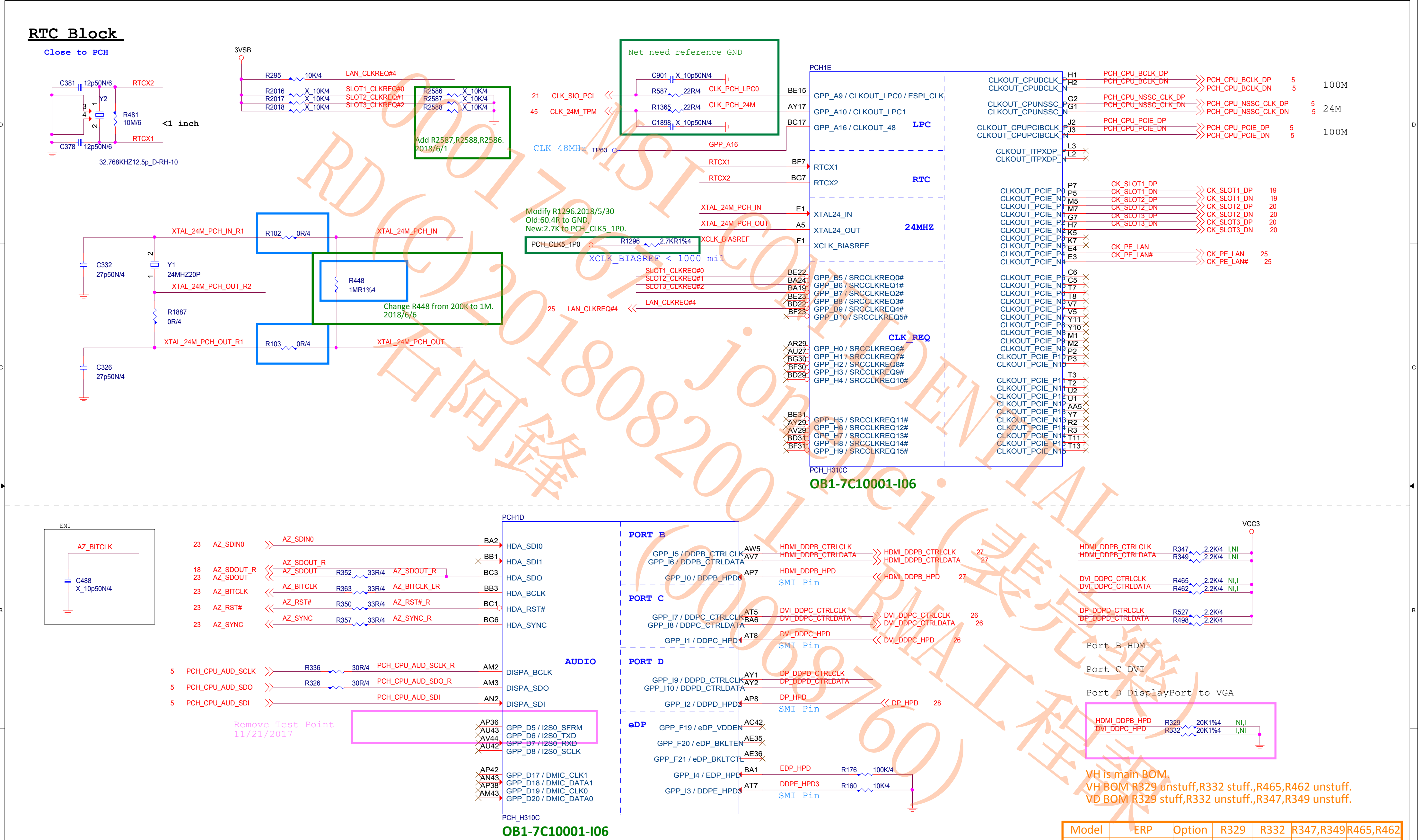
3VSB
GPP_E0 R1396 10K/4 SMI Pin
GPP_E1 R1400 10K/4 SMI Pin
GPP_E2 R1393 10K/4 SMI Pin
GPP_F0 R1405 10K/4
GPP_F1 R1408 10K/4
GPP_F2 R1402 10K/4

SATAXPCIE0-PE9
SATAXPCIE1-PE10
SATAXPCIE2-PE15
SATAXPCIE3-PE16
SATAXPCIE4-PE17
SATAXPCIE5-PE18
0--PCIE
1--SATA

VCC3 R1223 X_10K/4 GPP_F8
R1221 X_10K/4 GPP_F9
R792 1K/4 R662 10K/4 PCH_CONFIG
R249 X_10K/4 R255 10K/4 PCH_RSVD
R211 20K/4 R2019 X_10K/4 SV_ADVANCE
R245 X_10K/4 R242 10K/4 GFX_CRB_DETECT

MSI CONFIDENTIAL
0609-7967 (Inspur)
KDC(Suzhou)2018082001 (000760)
KDC(蘇州)(完樂)
MA工程課

MICRO-STAR INT'L CO.,LTD
MS-7C13
Size: Custom
Document Description: PCH-USB/PCIE/DMI/SATA
Rev: 10
Date: Monday, June 25, 2018
Sheet 12 of 53



VH is main BOM.
VH BOM R329 unstuff,R332 stuff.,R465,R462 unstuff.
VD BOM R329 stuff,R332 unstuff.,R347,R349 unstuff.

Model	ERP	Option	R329	R332	R347,R349	R465,R462
7C13-VH	7C31-0**	STD	unstuff	stuff	stuff	unstuff
7C13-VD	7C31-0**	A	stuff	unstuff	unstuff	stuff

MICRO-STAR INT'L CO.,LTD

MS-7C13

Size: Custom | Document Description: PCH-Audio/Display/Clock | Rev 10

Date: Monday, June 25, 2018 | Sheet 13 of 53

MSI CONFIDENTIAL
001796/jonpei(裴亮鑫) RD(C)20180820017(0008760) RD工程課 石向鋒

GPIO(SMI/NMI):
GPP_B14,GPP_B20,GPP_B23
GPP_C[23:22]
GPP_D[4:0]
GPP_E[8:0]
GPP_I[3:0]
GPP_G[7:0](Support SMI# only)

Model	ERP	Option	GPP_G21	GPP_G22	GPP_G23
7C13-VH	7C31-0**	STD	0	0	0
7C13-VD	7C31-0**	A	0	0	1

MSI CONFIDENTIAL

MICRO-STAR INT'L CO.,LTD

MS-7C13

Size: Custom | Document Description: PCH-GPIO/USBOC#/SATASTRAP | Rev: 10

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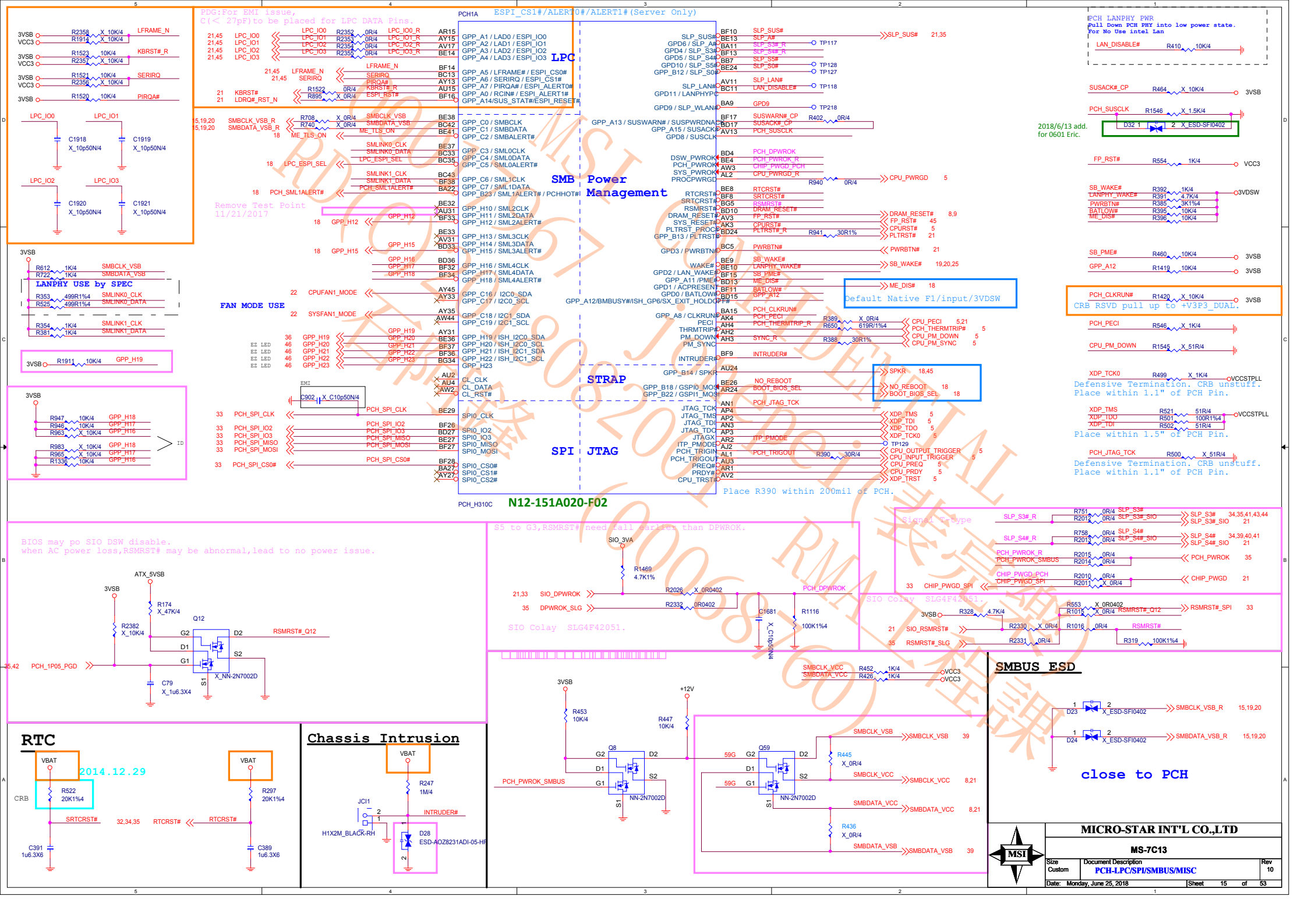
PDG:For EMI issue, C(< 27pF)to be placed for LPC DATA Pins.
PCH1A
ESPI_CS1#/ALERT0#/ALERT1#(Server Only)
LPC
SMB
Power Management
STRAP
SPI
JTAG
FAN MODE USE
LANPHY USE by SPEC
Remove Test Point 11/21/2017
Default Native F1/input/3VDSW
CRB RSVD pull up to +V3P3_DUAL.
Defensive Termination. CRB unstuff. Place within 1.1" of PCH Pin.
Defensive Termination. CRB unstuff. Place within 1.5" of PCH Pin.
Place R390 within 200mil of PCH.
PCH LANPHY PWR
Pull Down PCH PHY into low power state.
For No Use intel Lan
2018/6/13 add. for 0601 Eric.
BIOS may po SIO DSW disable.
when AC power loss,RSMRST# may be abnormal,lead to no power issue.
S5 to G3,RSMRST# need fall earlier than DPWROK.
SIO Colay SLG4F42051.
RTC
2014.12.29
Chassis Intrusion
SMBUS ESD
close to PCH
PCH_H310C
N12-151A020-F02
MICRO-STAR INT'L CO.,LTD
MS-7C13
PCH-LPC/SPI/SMBUS/MISC
Rev 10
Date: Monday, June 25, 2018
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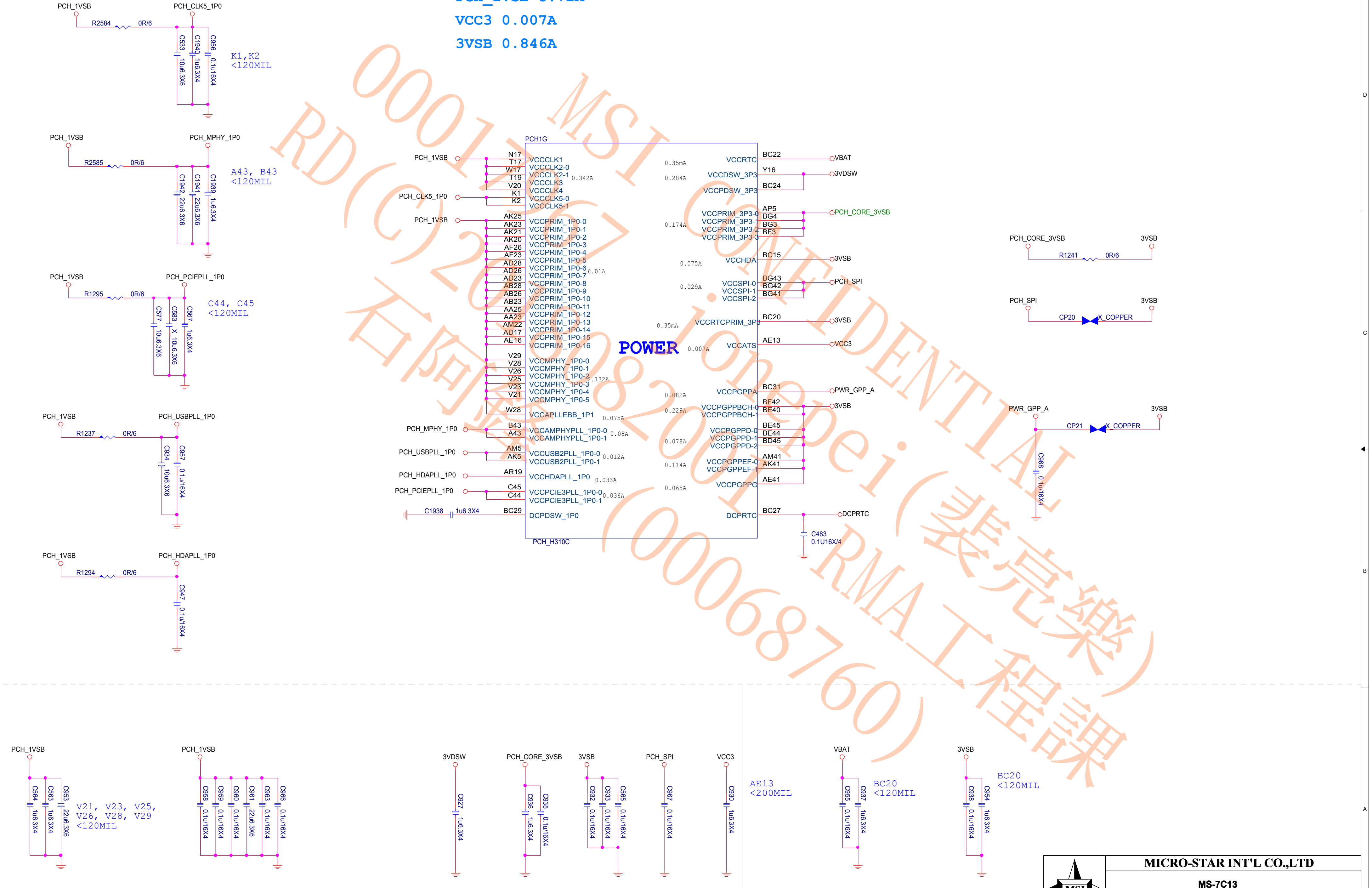
PCH_1VSB 8.72A

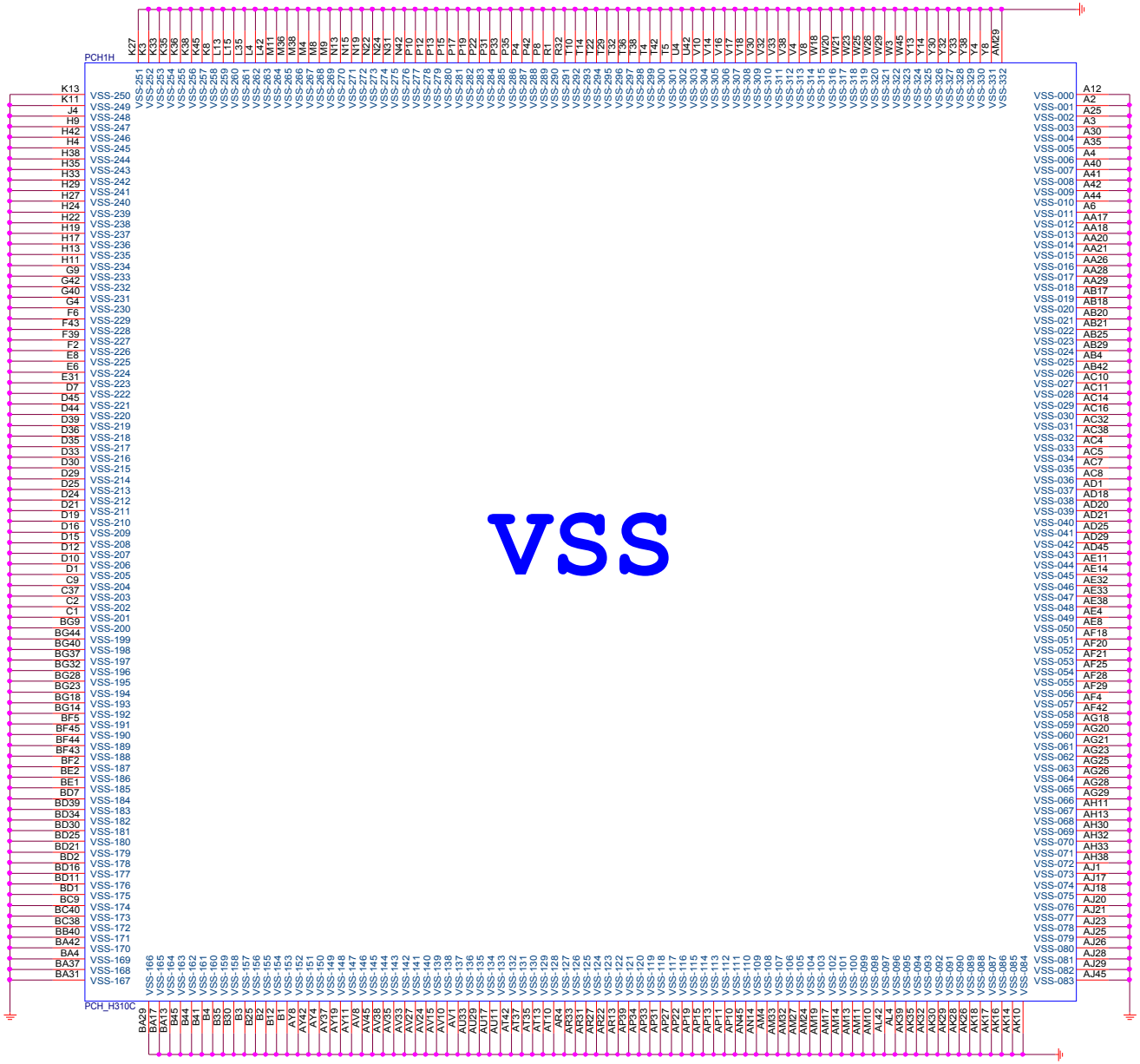
VCC3 0.007A

3VSB 0.846A



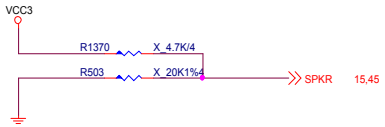
MICRO-STAR INT'L CO.,LTD			
MS-7C13			
Size: Custom	Document Description: PCH-Power		Rev: 10
Date: Monday, June 25, 2018		Sheet 16 of 53	

MSI CONFIDENTIAL
0001MS(C)2018-06-28 RD 石詢錦 jonepei (裴亮樂) (00068760) RMA工程課



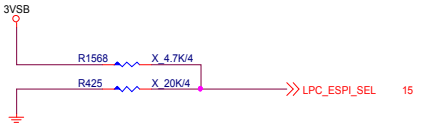
MICRO-STAR INT'L CO.,LTD	
MS-7C13	
Size: Custom	Document Description: PCH-GND
Rev: 10	
Date: Monday, June 25, 2018	Sheet 17 of 53

TOP Swap



Internal pull-down 20K is disabled after PLTRST#

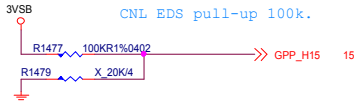
LPC eSPI Mode



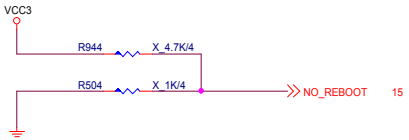
0 : LPC
1 : eSPI

Internal pull-down 20K is disabled after RSMRST

Reserved



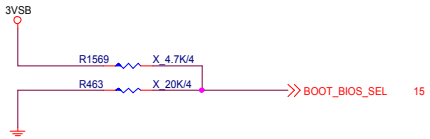
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

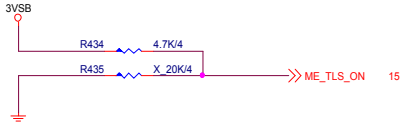
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down 20K is disabled after PLTRST

AMT and SBA with confidentiality

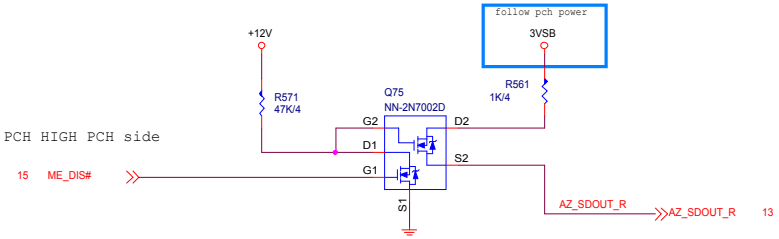


0 : DISABLE
1 : ENABLE (Default)

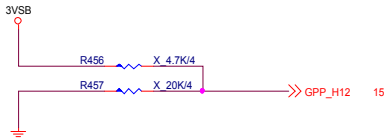
Internal pull-down 20K is disabled after RSMRST

HDA_SDO

ME flash by GPIO



ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down 20K is disabled after RSMRST

Reserved

MICRO-STAR INT'L CO.,LTD

MS-7C13

Size	Document Description	Rev
Custom	PCH-Strap	10

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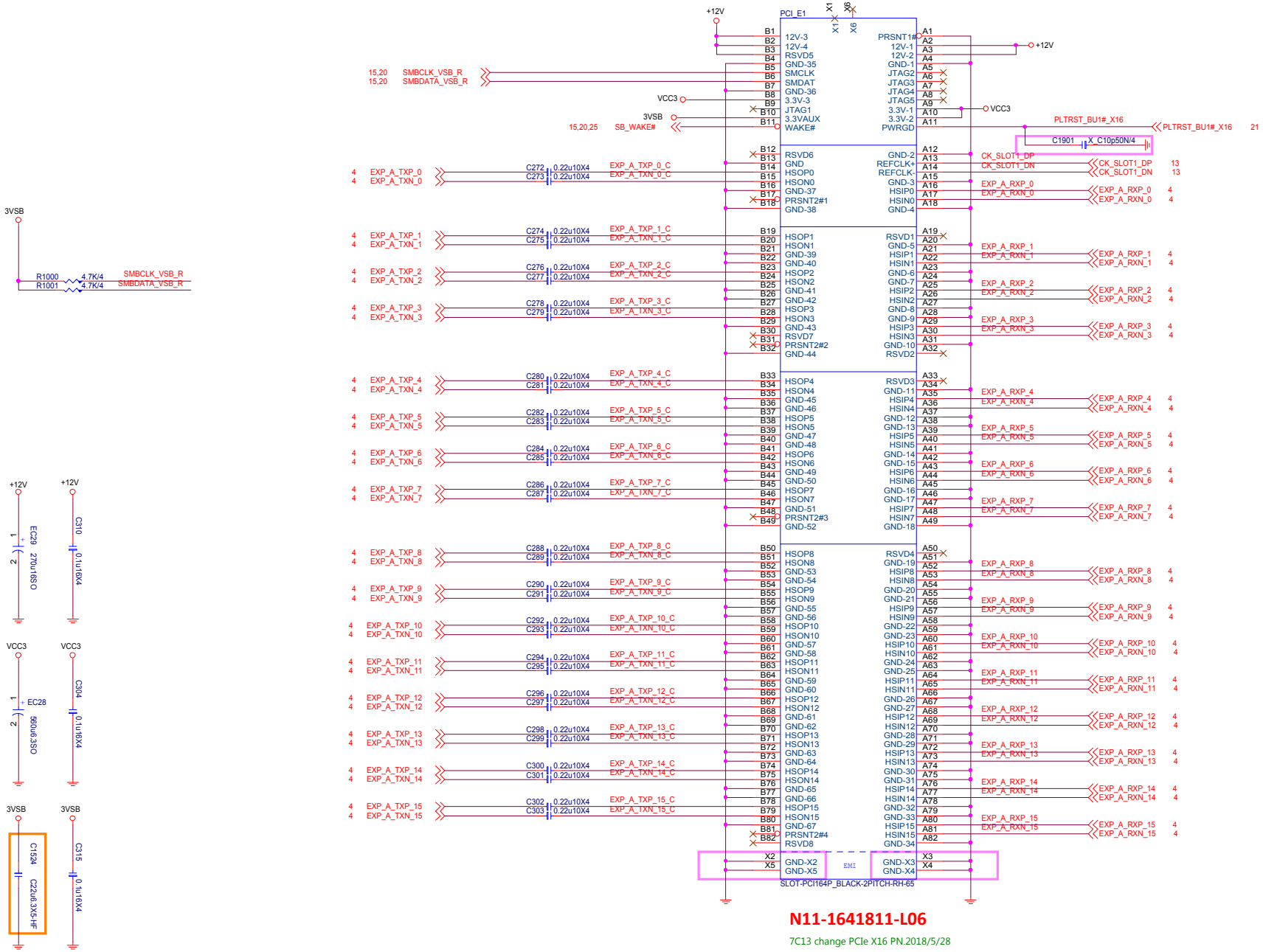
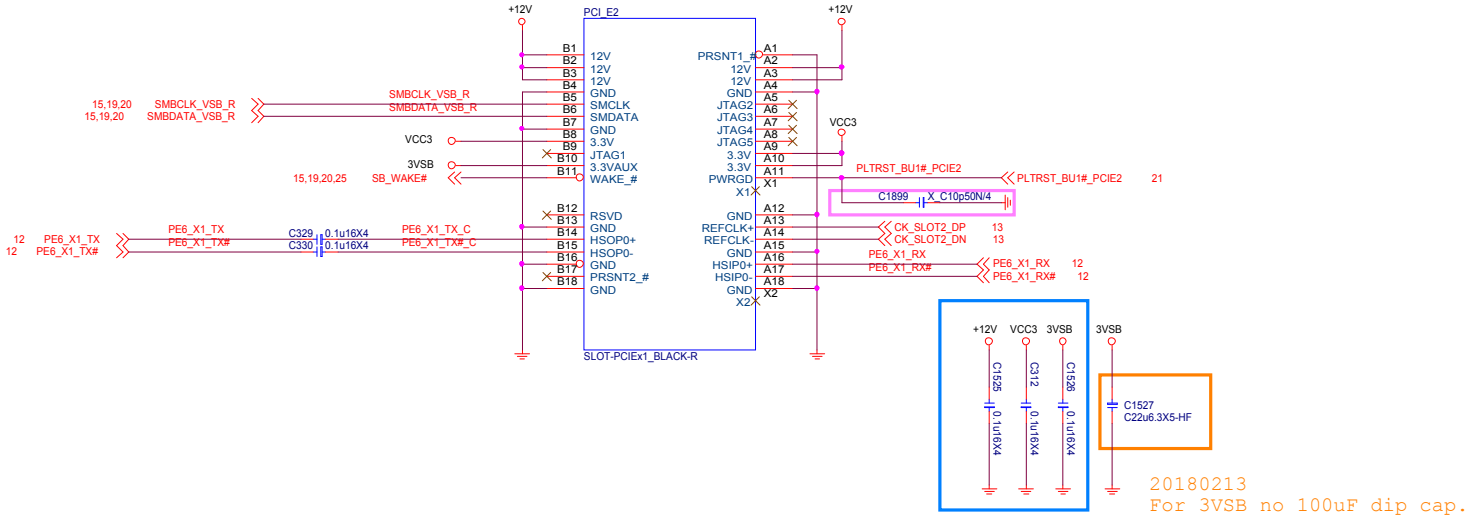


N11-1641811-L06

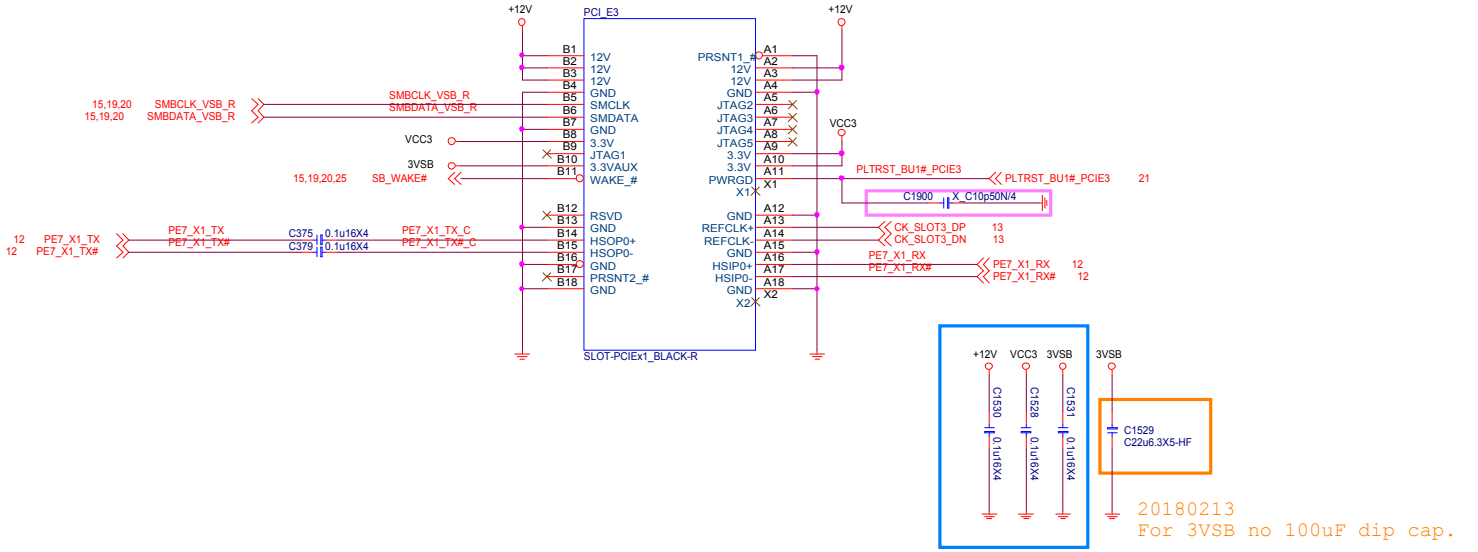
7C13 change PCIe X16 PN.2018/5/28

20180213
For 3VSB no 100uF dip cap.

MICRO-STAR INT'L CO.,LTD	
MS-7C13	
Size: Custom	Document Description: PCIE SLOT-CPU(X16)
Rev: 10	
Date: Monday, June 25, 2018	Sheet 19 of 53



20180213
For 3VSB no 100uF dip cap.



20180213
For 3VSB no 100uF dip cap.

MICRO-STAR INT'L CO.,LTD		
MS-7C13		
Size: Custom	Document Description: PCIE SLOT-PCH(X1)	Rev: 10
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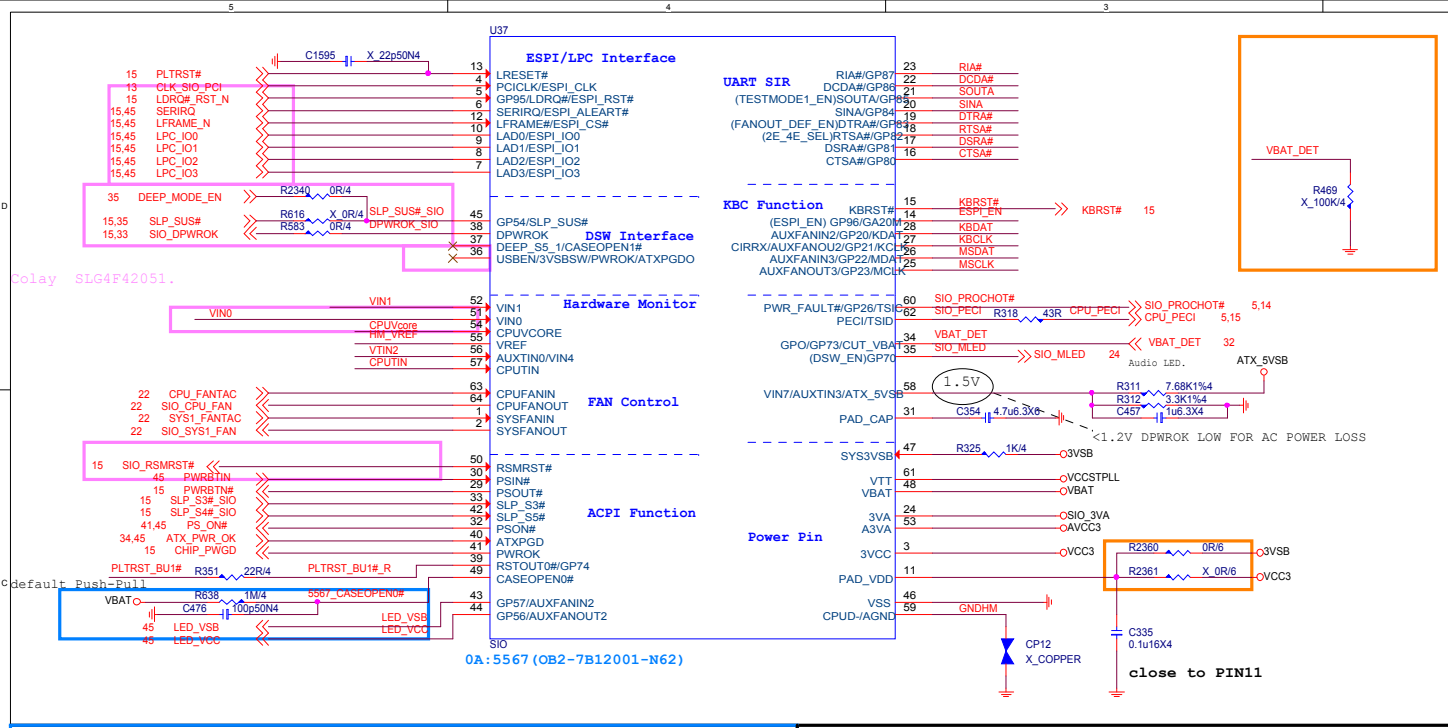
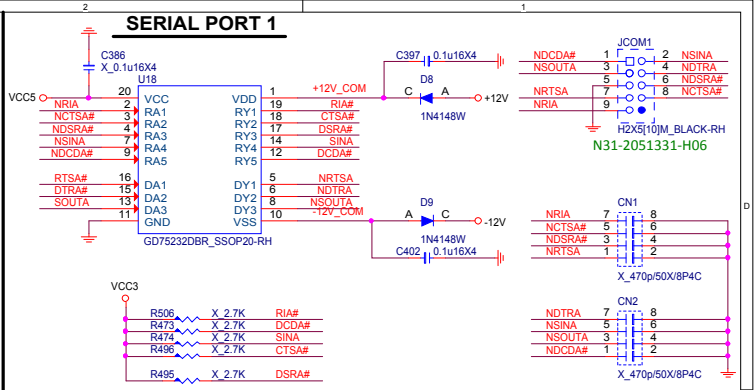
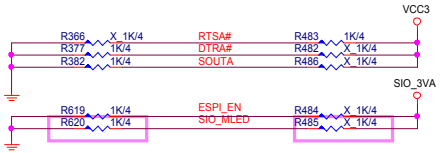
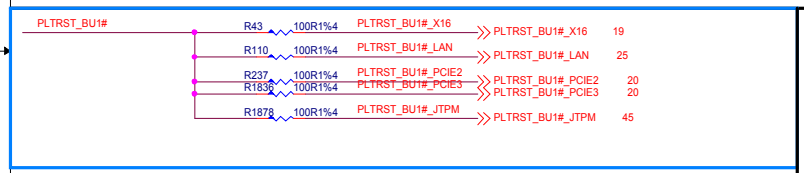


SERIAL PORT 1

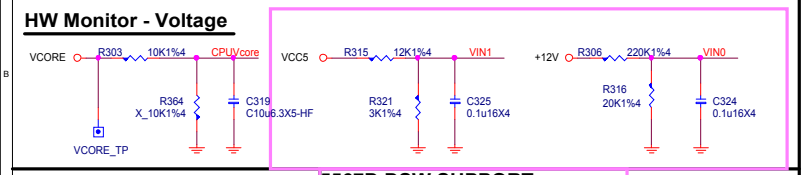


PIN	5567D NAME	Circuit NAME	0	1
18	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E
19	FANOUT_DEF_EN	DTRA#	CPU FANOUT default RPM 50%.	CPU FANOUT default RPM 100%
21	TESTMODE1_EN	SOUTA	DISABLE TEST1MODE	ENABLE TEST1MODE
14	ESPI_EN	ESPI_EN	ENABLE LPC	ENABLE ESPI
35	DSW_EN	SIO_MLED	DISABLE	ENABLE DSW_EN

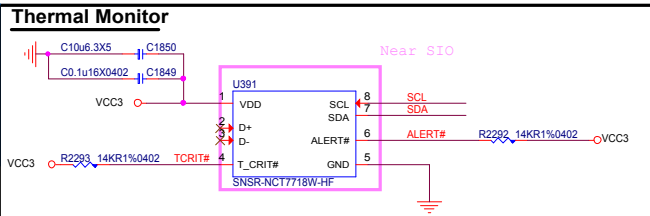




HW Monitor - Voltage

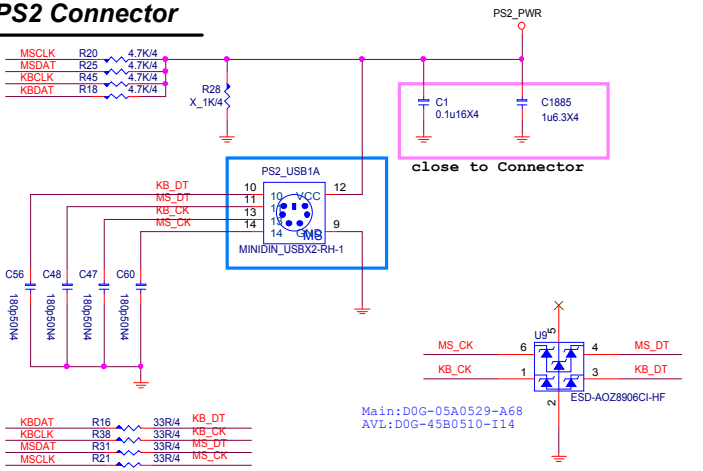


Thermal Monitor

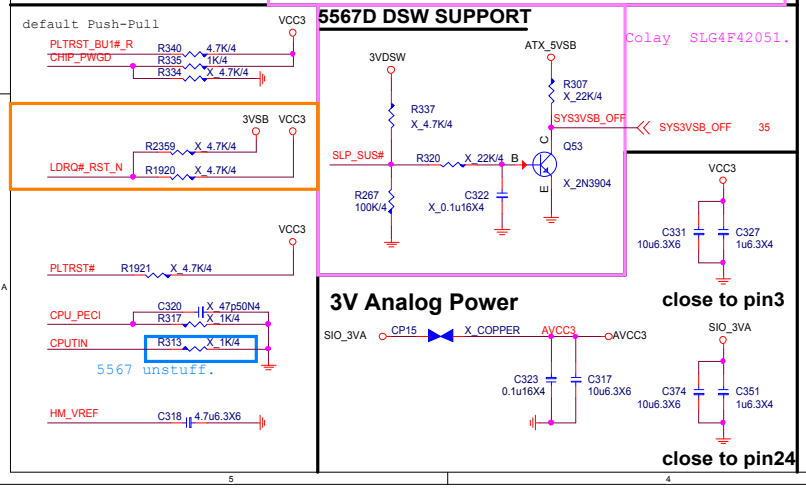


TEMPERATURE (℃)		T_CRIT# 2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

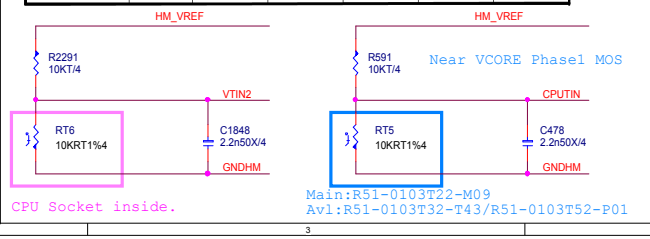
PS2 Connector

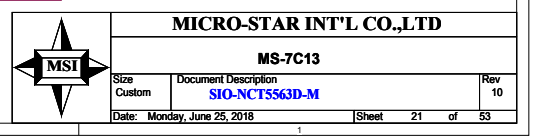


5567D DSW SUPPORT



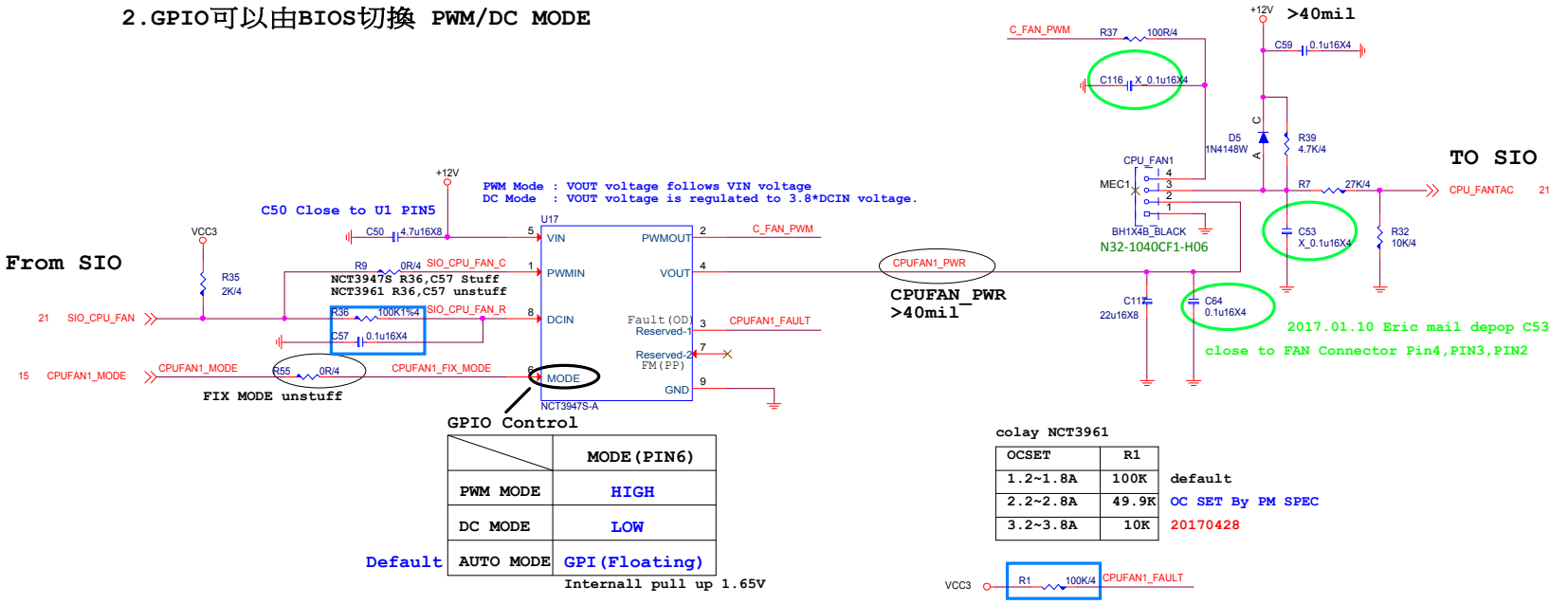
3V Analog Power





TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

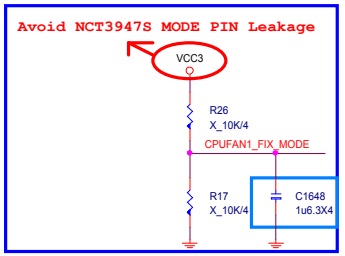
2.GPIO可以由BIOS切換 PWM/DC MODE



	MODE(PIN6)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

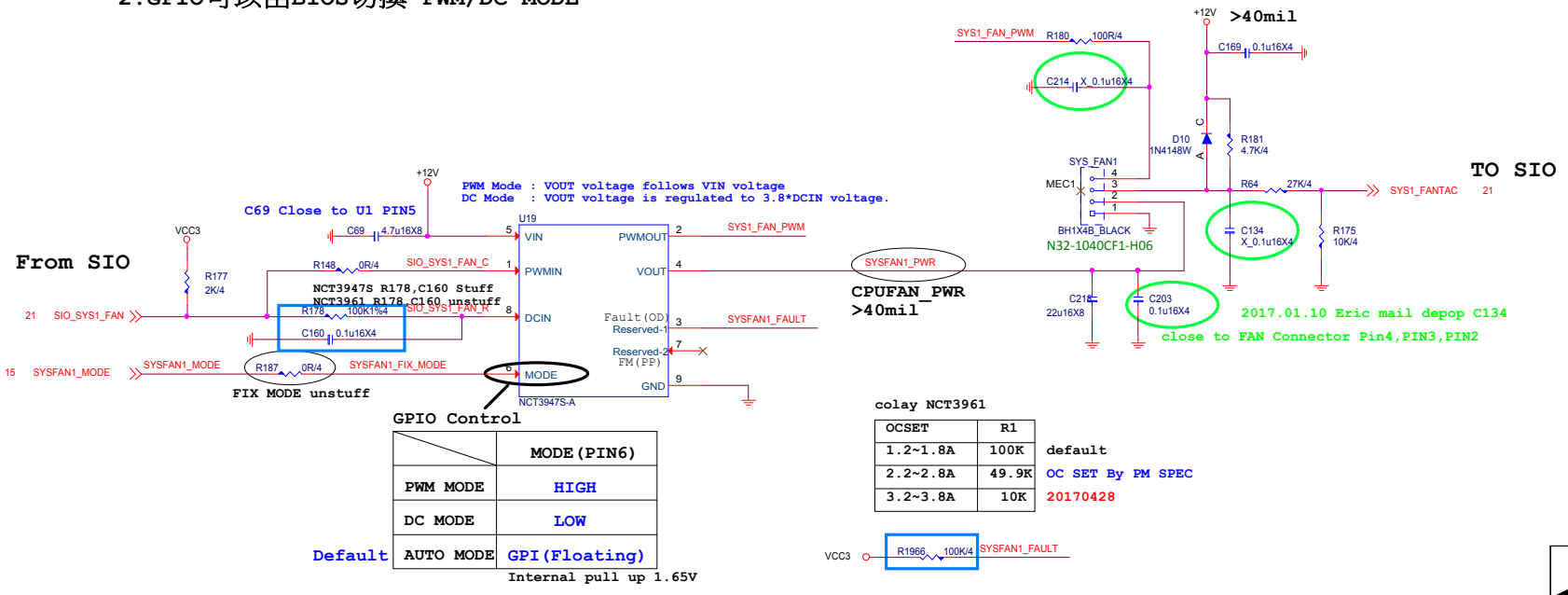
colay NCT3961

OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	OC SET By PM SPEC
3.2~3.8A	10K	20170428



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

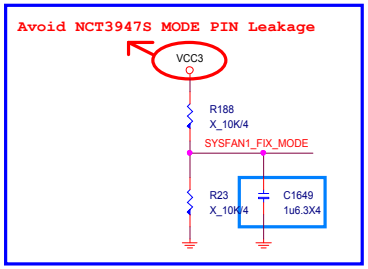
2.GPIO可以由BIOS切換 PWM/DC MODE



	MODE(PIN6)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

colay NCT3961

OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	OC SET By PM SPEC
3.2~3.8A	10K	20170428



MICRO-STAR INT'L CO.,LTD

MS-7C13

Size: Custom | Document Description: FAN CONTROLLOR | Rev: 10

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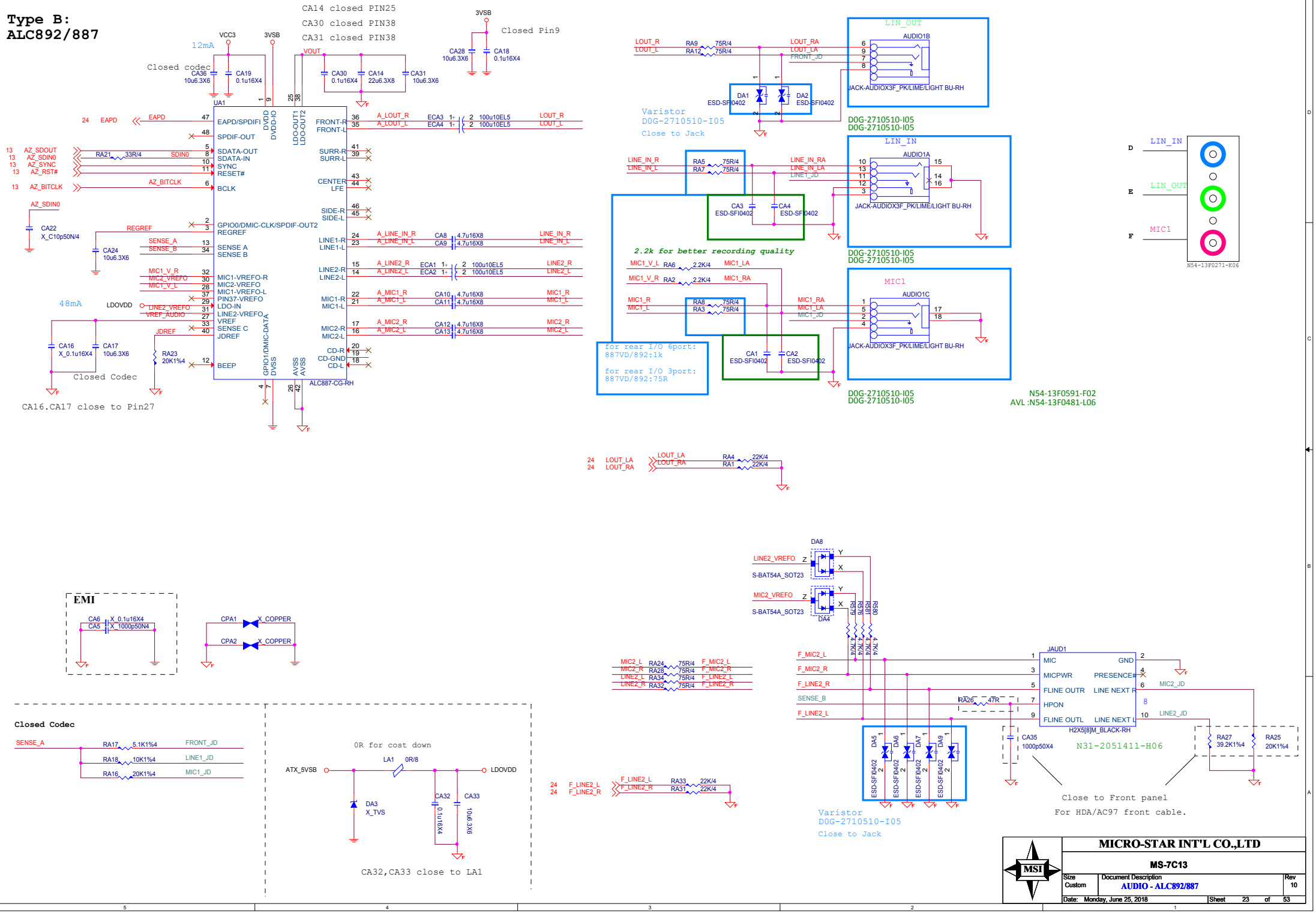
Type B:
ALC892/887



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MS-7C13	
Size: Custom	Document Description: AUDIO - ALC892/887
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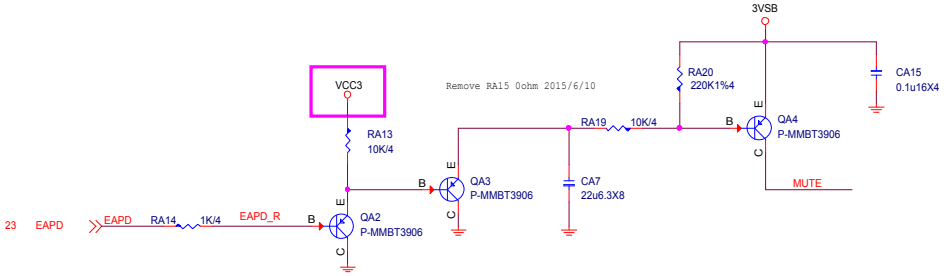
Rear Line OUT De-POP circuit

History:

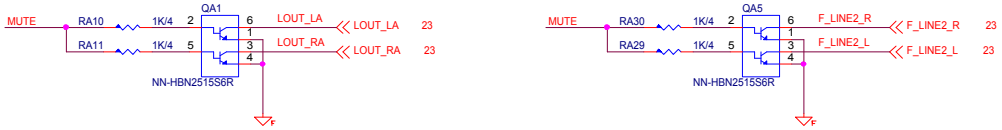
2014/02/13: stuff de-pop circuit of Line out & HP out.

De-pop circuit for Rear Line out & Front Headphone out)



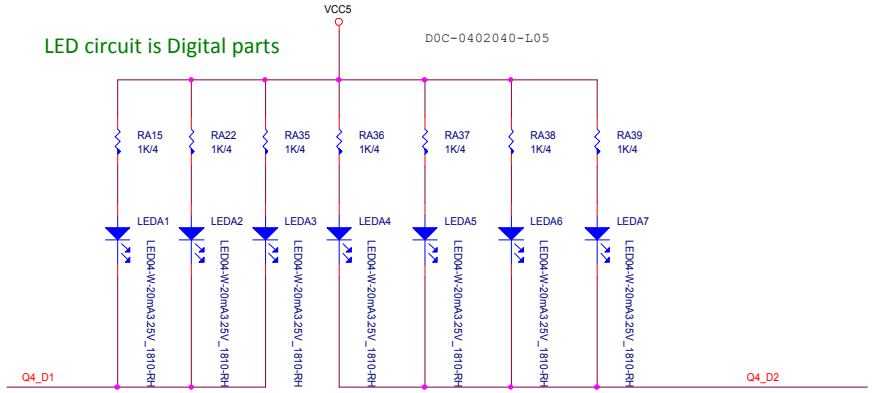
Digital

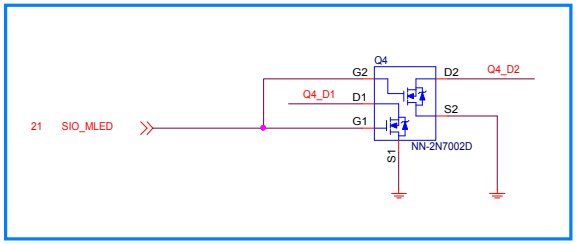
Analog



Audio LED

LED circuit is Digital parts





2016.01.12:Modify Q4 to Dual 7002 & Remove 0R

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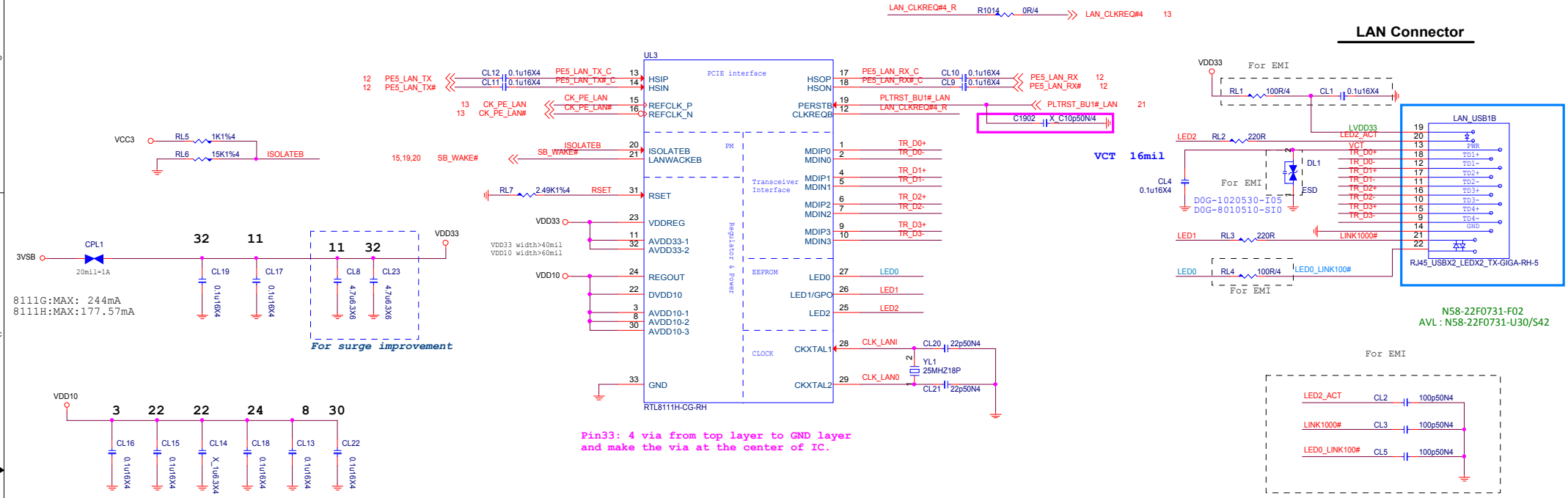
RTL8111G/RTL8111H Giga LAN

8111H:B06-08111CC-R09
8111G:B06-08116C-R09



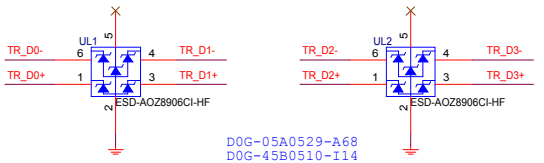
LAN Connector

VCT 16mil

N58-22F0731-F02
AVL : N58-22F0731-U30/S42

ESD Protect

UL1 & UL2 close to connector



8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

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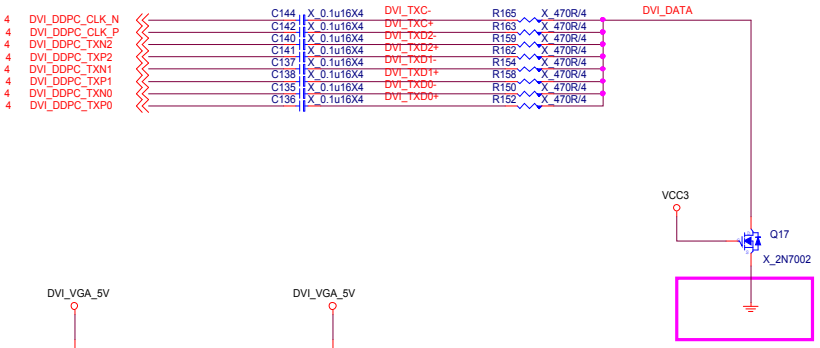
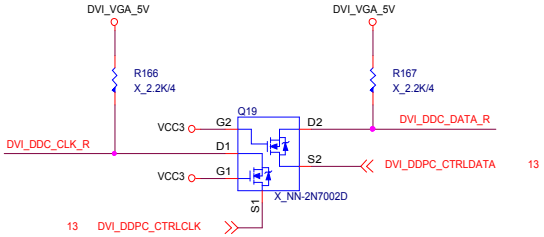
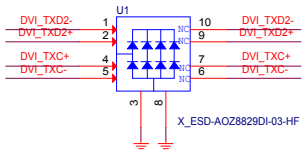
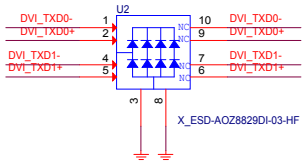
DVI level shifter

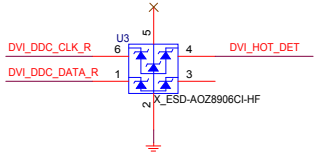
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

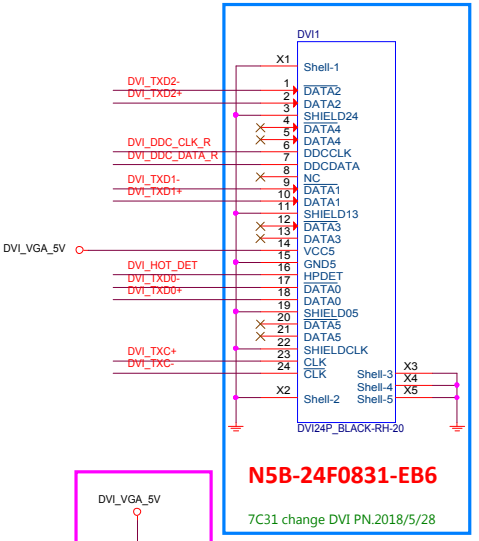


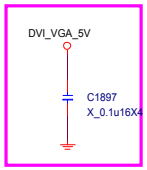


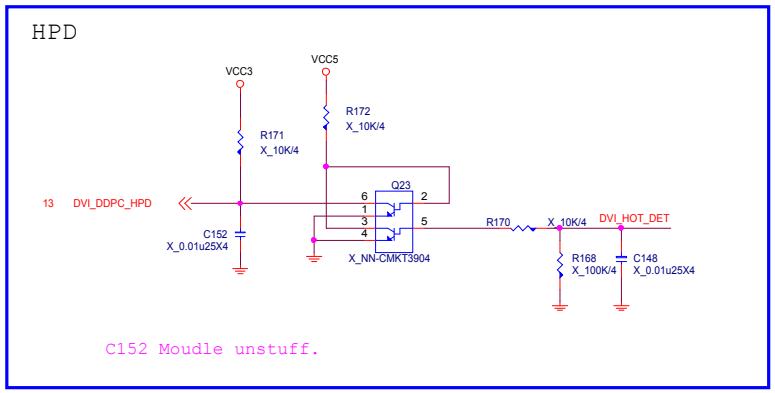


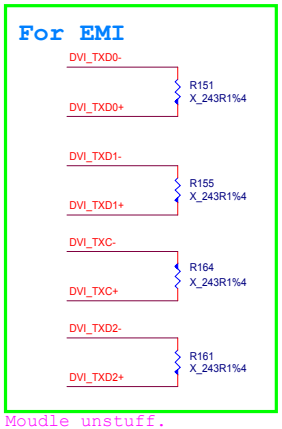


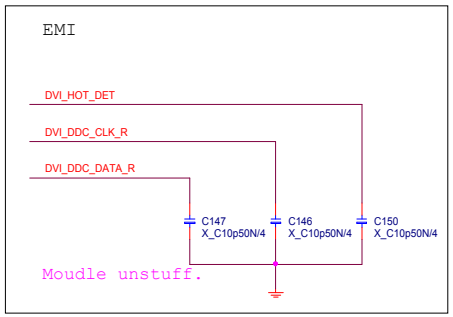












Moudle unstuff.

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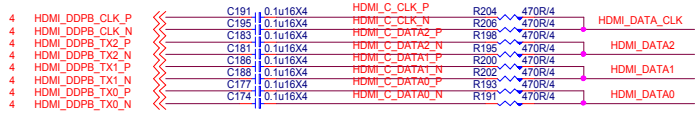
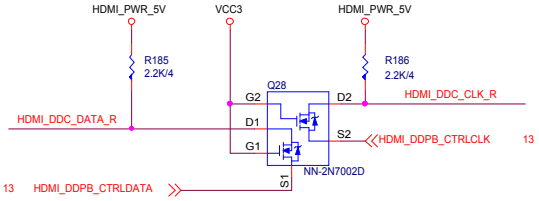
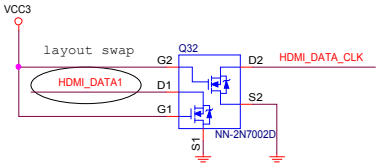
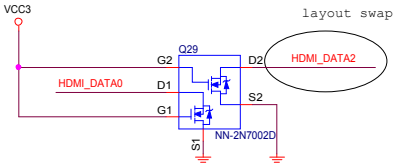
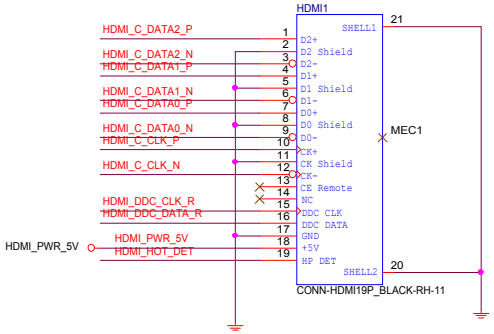
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

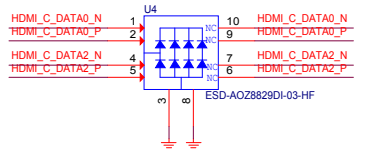


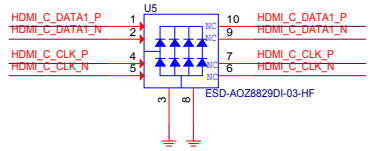


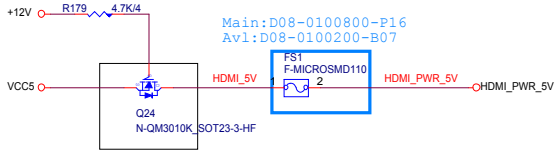




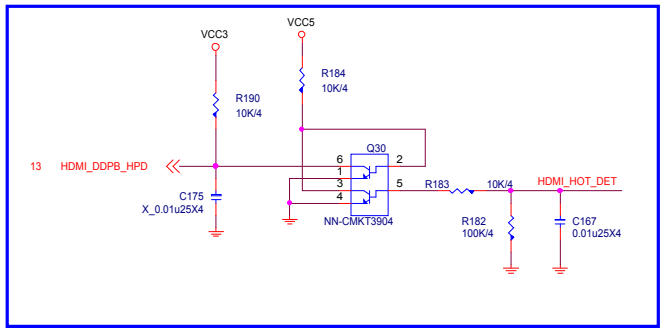


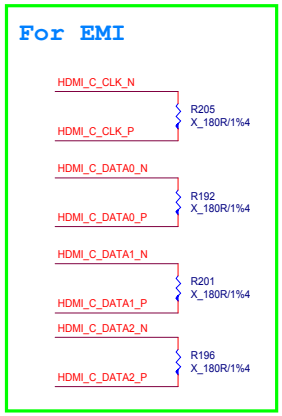


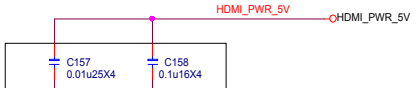


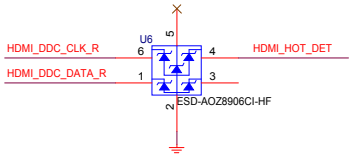


HPD









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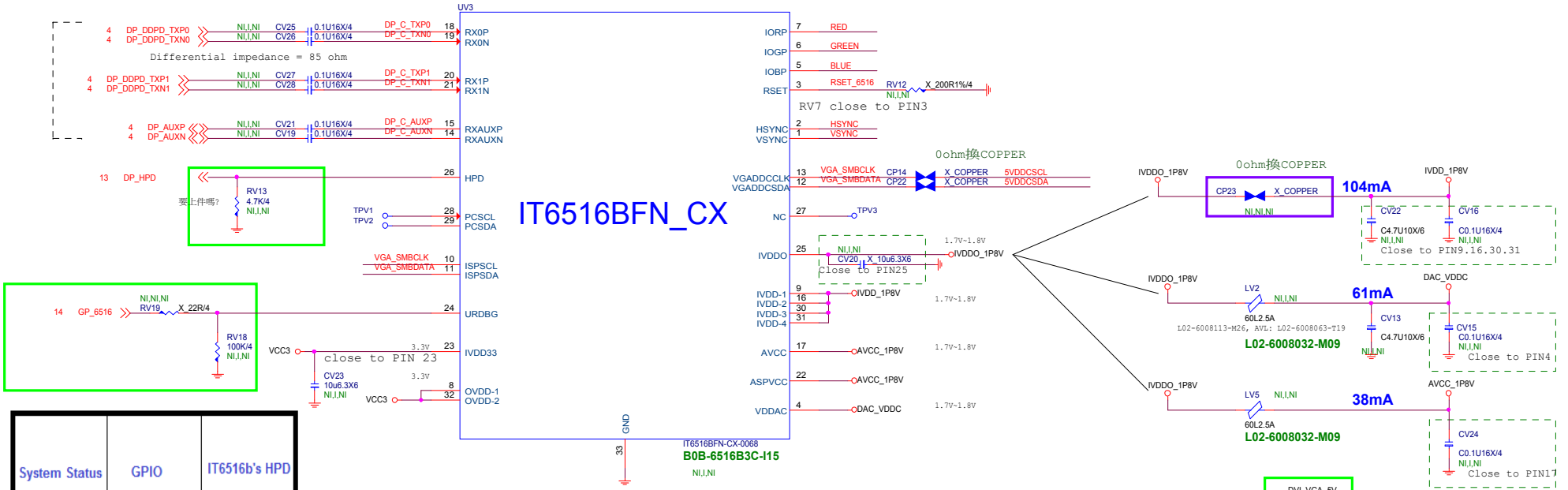
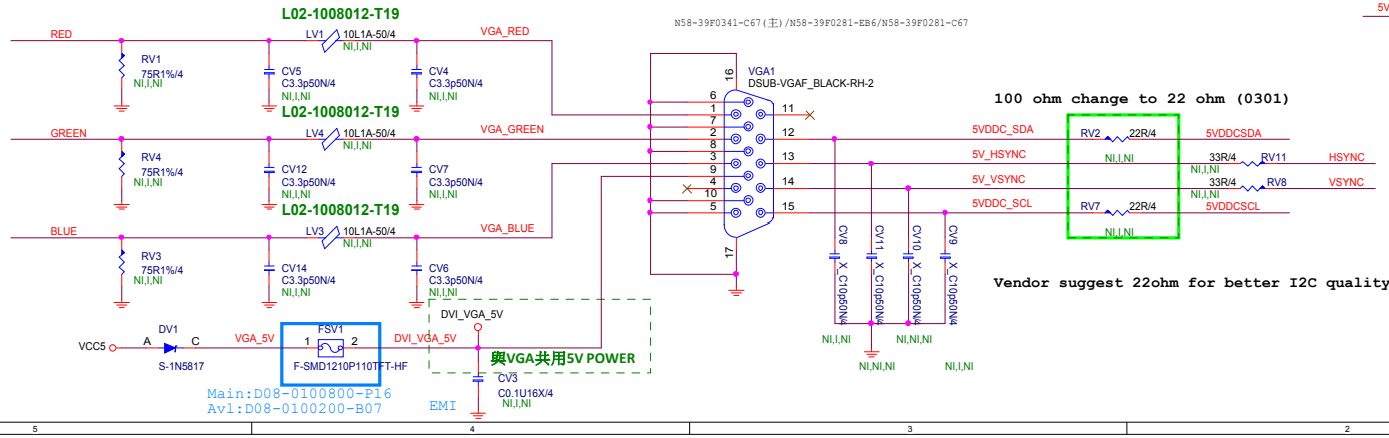
Note:

If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



System Status	GPIO	IT6516b's HPD
Legacy Mode (VBIOS) /DOS MOde	HIGH	Force HIGH
Windows /UEFI Mode (GOP)	LOW	Depend on VGA device's plug/unplug

If have VSIS1.2 SPEC requset,can change bead to L02-2208012-M09 use, It test pass.



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Size: Custom	Document Description: VGA - ITE6516	Rev: 10
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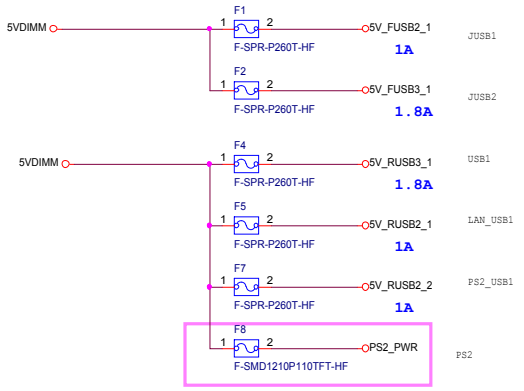
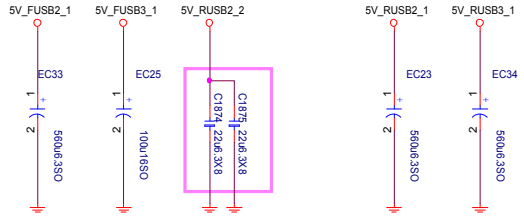
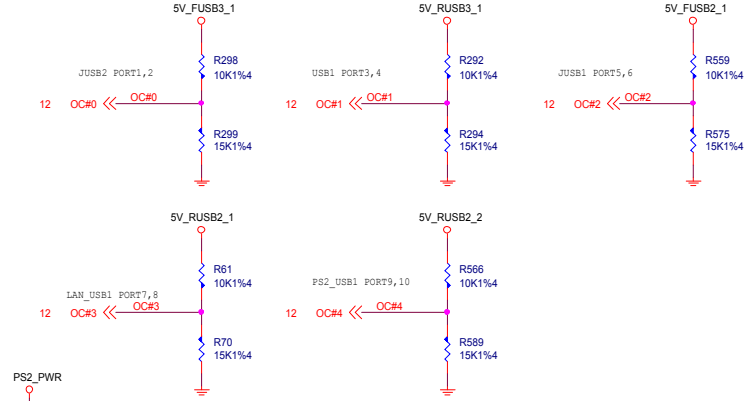
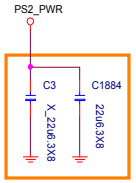




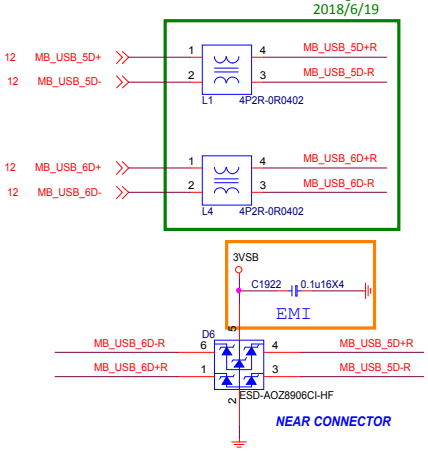


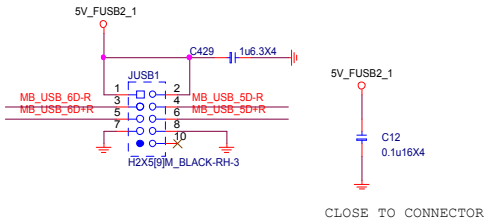


USB CONN	USB POWER	PCH PORT	OC# SIGNAL
JUSB1	5V_FUSB2_1	Port5,6	OC#2
PS2_USB1	5V_RUSB2_2	Port9,14	OC#4
JUSB3	5V_FUSB3_1	Port1,2	OC#0
USB1	5V_RUSB3_1	Port3,4	OC#1
LAN_USB1	5V_RUSB2_1	Port7,8	OC#3

FRONT JUSB2 PORT 5,6

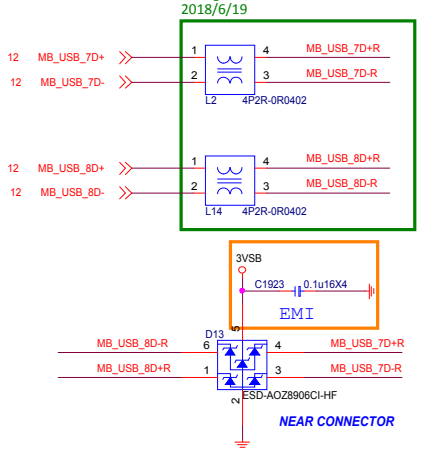
Change L1,L4 from NI to I 0ohm.
2018/6/19

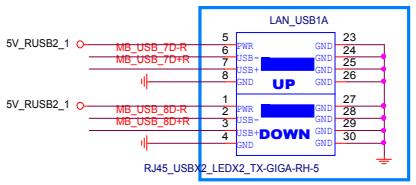


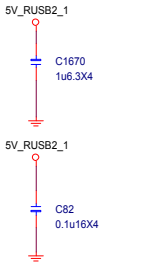


USB1 PORT 7,8

Change L2,L14 from NI to I 0ohm.
2018/6/19



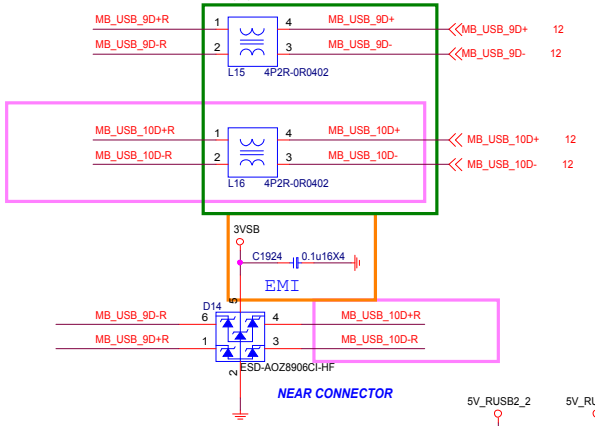


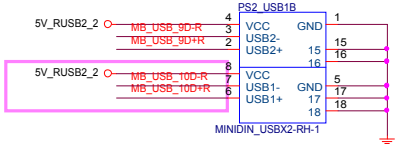


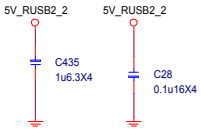
N58-22F0731-F02
AVL : N58-22F0731-U30/S42

FRONT PS2_USB1 PORT 9,10

Change L15,L16 from NI to I 0ohm.
2018/6/19







USB2.0 Port10 change to Port14.
H310C : USB2.0 Port14 change to Port10.

N58-14M0081-L06
AVL : N58-14M0221-H06

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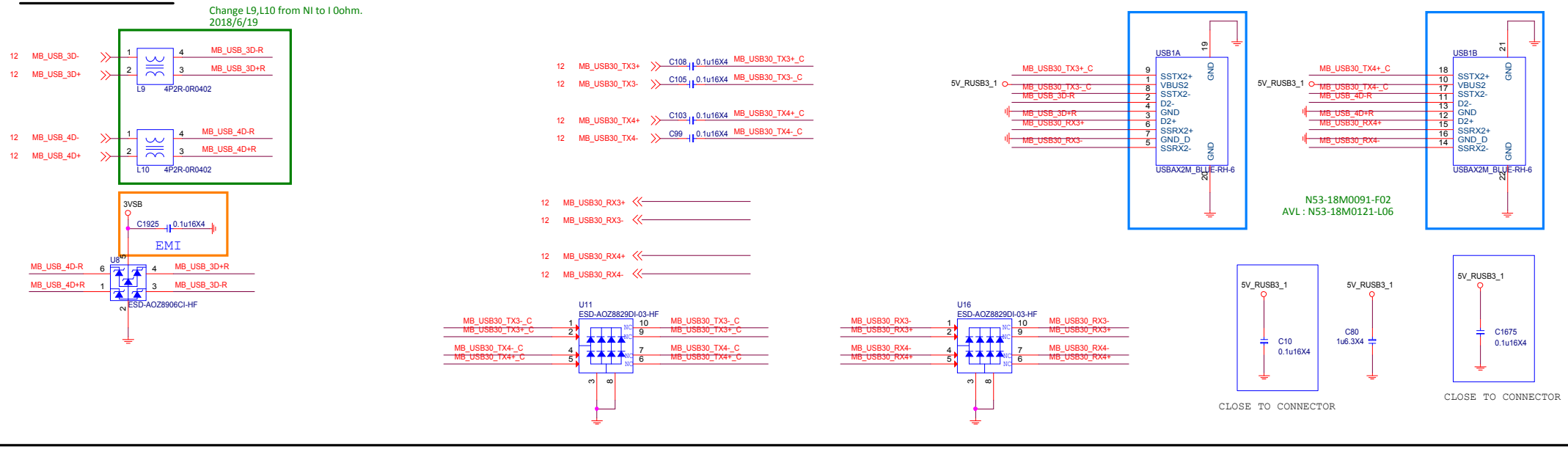
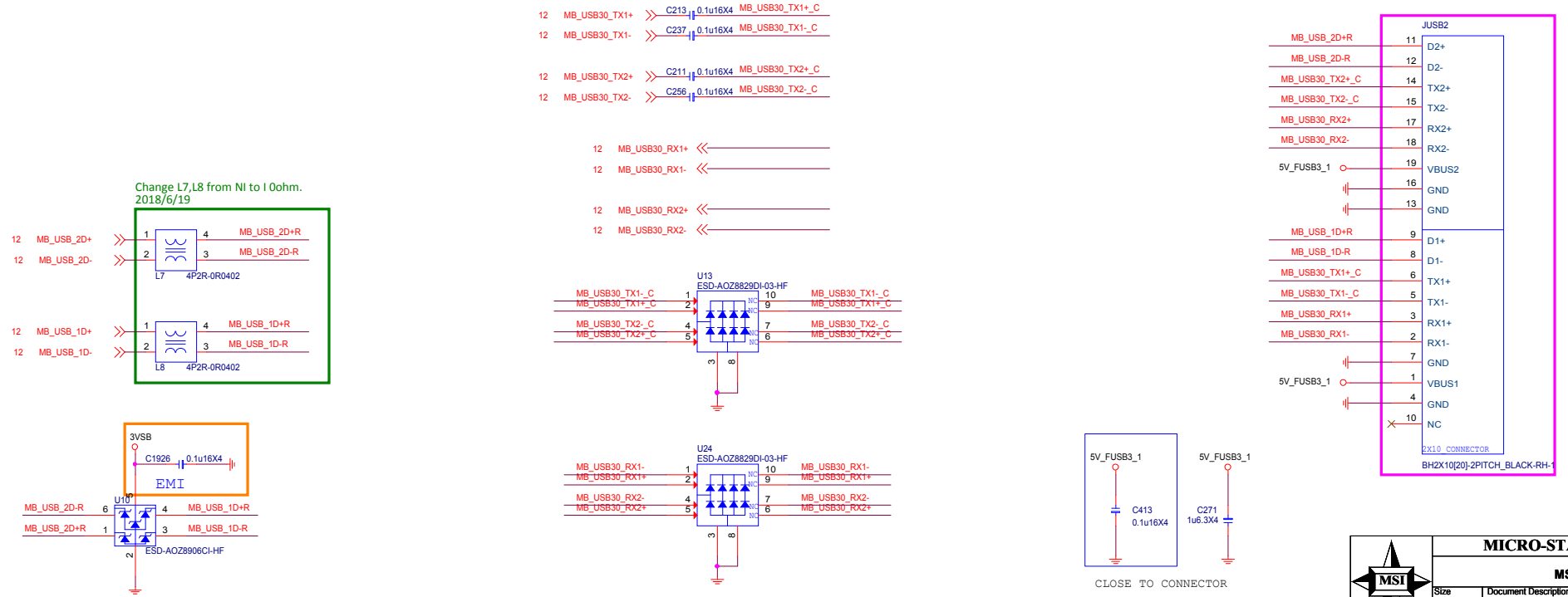
Rear USB1 port 9,10



Front JUSB3 port 1,2



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Size: Custom	Document Description: Rear USB3 & Front Connector	Rev: 10
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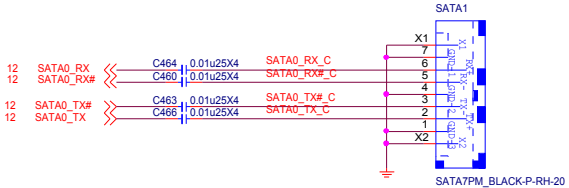

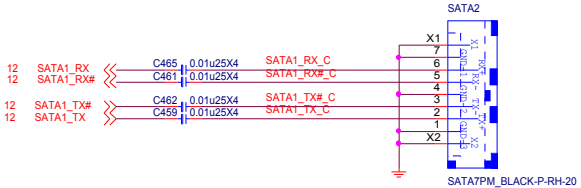

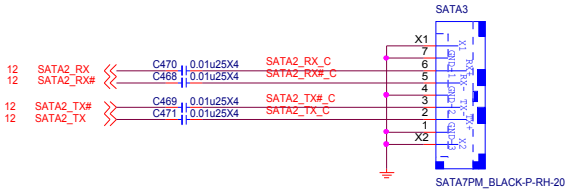

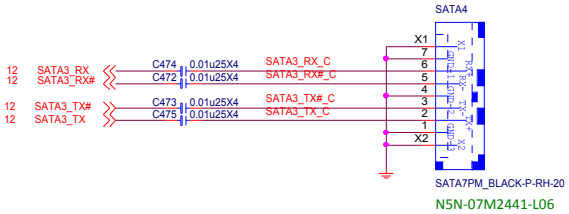

MICRO-STAR INT'L CO.,LTD		
MS-7C13		
Size: Custom	Document Description: SATA connector	Rev: 10
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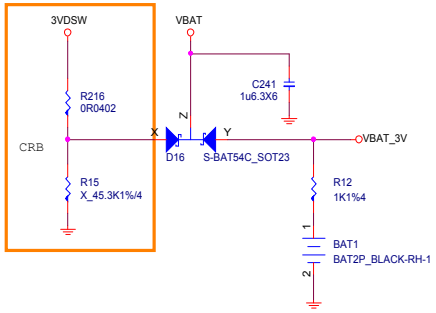
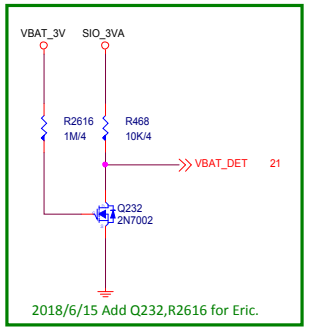
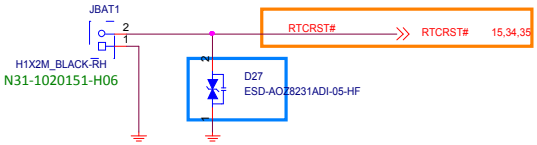
VBAT





For Factory VBAT test use.
Connector to SIO 5567 GP73.
BIOS request form need programing to GPI.
LOW:VBAT OK.
HIGH : VBAT LOSS



By Ivy's word document.
Main:D0G-130050C-A68
Av1:D0G-3000600-L07/D0G-1200520-I05

MICRO-STAR INT'L CO.,LTD		
MS-7C13		
Size: Custom	Document Description: CUT VBAT circuit	Rev: 10
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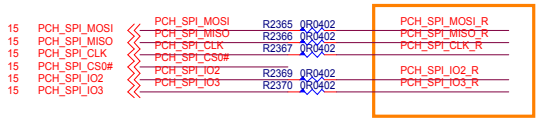
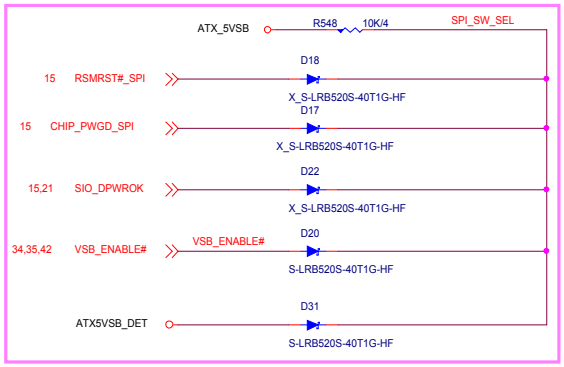
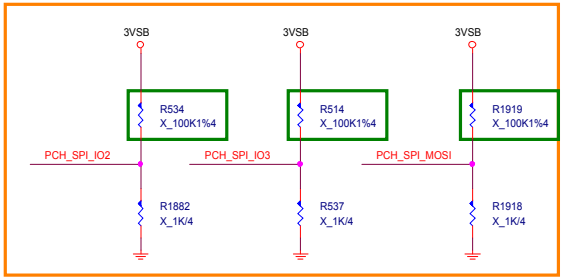


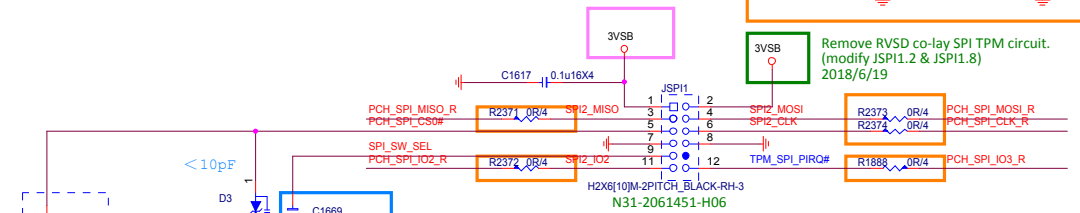


Main:D01-5204000-LA9
Avl:D01-BAS4030-P15

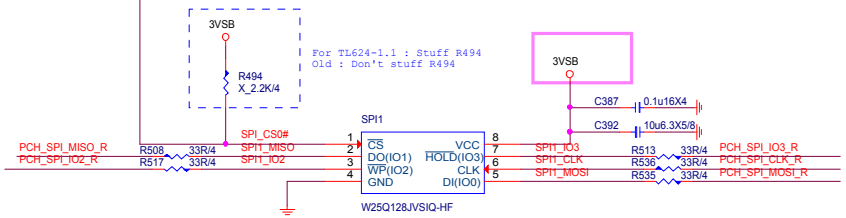


Remove RVSD co-lay SPI TPM circuit.
(modify JSPI1.2 & JSPI1.8)
2018/6/19

Change R534,R514,R1919 From I to NI
2018/6/20



1.CNL EDS
During reset,PCH_GPP_K21 via 20k pull up to 3.3V.
2.PCH_SPI_IO3 colay TPM_PIRQ#(1.8V or 3.3V,OD)
3.TPM_PIRQ#
Interrupt request signal to the host.
No internal pull up resistor.Active low.
4.TL624-2.2 support SPI Standard Mode.



M31-2512893-W03
AVL : M31-2512832-M24

MICRO-STAR INT'L CO.,LTD

MS-7C13

Size	Document Description	Rev
Custom	BIOS ROM	10

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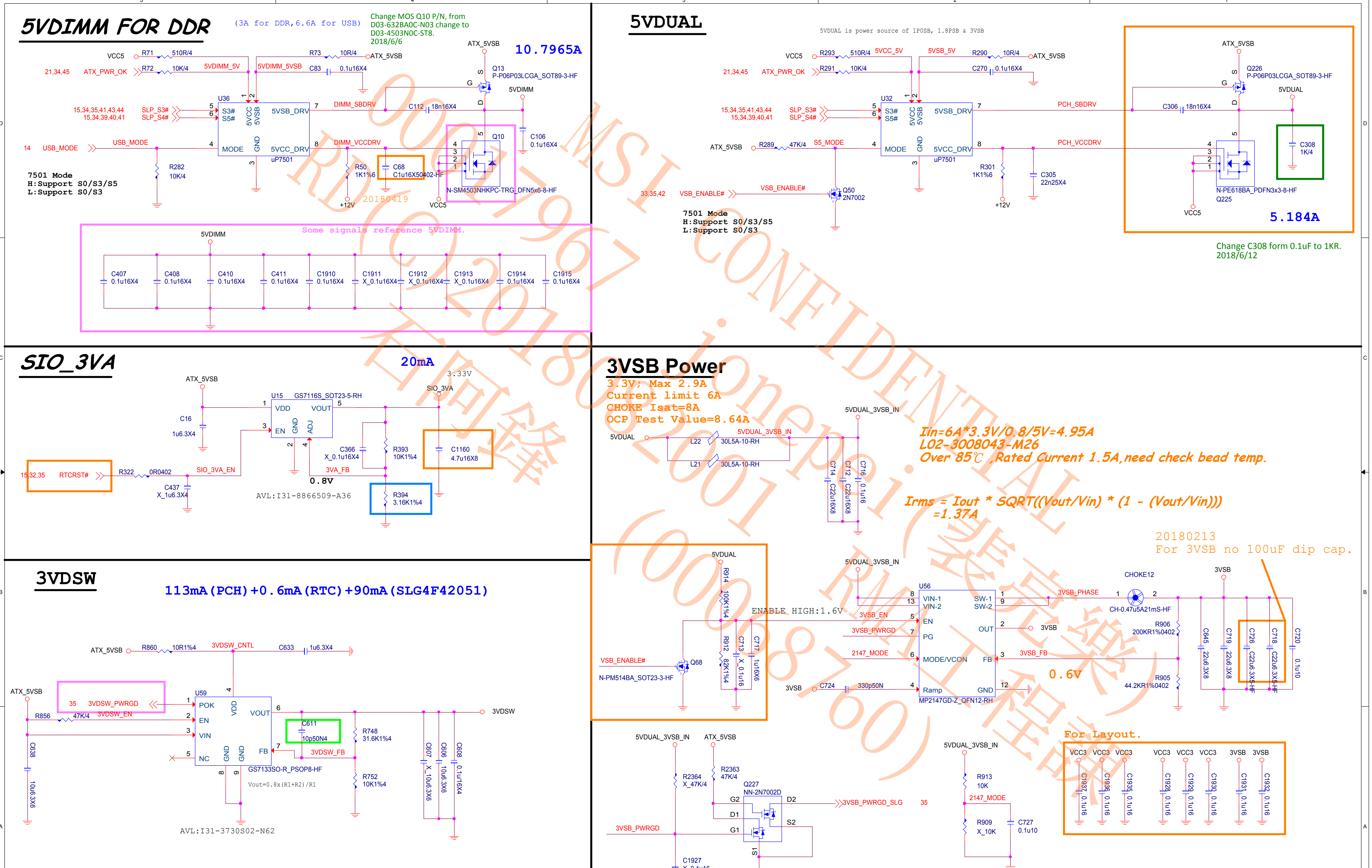

5VDIMM FOR DDR
(3A for DDR,6.6A for USB)
Change MOS Q10 P/N, from D03-632BA0C-N03 change to D03-4503N0C-ST8. 2018/6/6
10.7965A
ATX_5VSB
VCC5
R71 510R/4
R73 10R/4
21,34,45 ATX_PWR_OK
R72 10K/4
5VDIMM_5V
5VDIMM_5VSB
C83 0.1u16X4
Q13 P-P06P03LCGA_SOT89-3-HF
5VDIMM
U36
15,34,35,41,43,44 SLP_S3#
15,34,39,40,41 SLP_S4#
5VSB_DRV
DIMM_SBDRV
C112 18n16X4
14 USB_MODE
MODE
5VCC_DRV
DIMM_VCCDRV
uP7501
Q10
C106 0.1u16X4
R282 10K/4
R50 1K1%6
C68 C1u16X50402-HF
20180419
N-SM4503NHKPC-TRG_DFN5x6-8-HF
+12V
VCC5
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3
Some signals reference 5VDIMM.
5VDIMM
C407 0.1u16X4
C408 0.1u16X4
C410 0.1u16X4
C411 0.1u16X4
C1910 0.1u16X4
C1911 X_0.1u16X4
C1912 X_0.1u16X4
C1913 X_0.1u16X4
C1914 0.1u16X4
C1915 0.1u16X4
5VDUAL
5VDUAL is power source of 1P05B, 1.8PSB & 3VSB
R293 510R/4
5VCC_5V
5VSB_5V
R290 10R/4
R291 10K/4
C270 0.1u16X4
U32
PCH_SBDRV
C306 18n16X4
Q226 P-P06P03LCGA_SOT89-3-HF
5VDUAL
R289 47K/4
S5_MODE
PCH_VCCDRV
R301 1K1%6
C305 22n25X4
C308 1K/4
N-PE618BA_PDFN3x3-8-HF
Q225
33,35,42 VSB_ENABLE#
Q50 2N7002
5.184A
Change C308 form 0.1uF to 1KR. 2018/6/12
SIO_3VA
20mA
3.33V
U15 GS7116S_SOT23-5-RH
VDD
VOUT
EN
ADJ
C16 1u6.3X4
15,32,35 RTCRST#
R322 0R0402
SIO_3VA_EN
C437 X_1u6.3X4
C366 X_0.1u16X4
R393 10K1%4
3VA_FB
0.8V
C1160 4.7u16X8
R394 3.16K1%4
AVL:I31-8866509-A36
3VSB Power
3.3V; Max 2.9A
Current limit 6A
CHOKE Isat=8A
OCP Test Value=8.64A
5VDUAL_3VSB_IN
L22 30L5A-10-RH
L21 30L5A-10-RH
C714 C22u16X8
C712 C22u16X8
C716 0.1u16
Iin=6A*3.3V/0.8/5V=4.95A
L02-3008043-M26
Over 85℃ ,Rated Current 1.5A,need check bead temp.
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
=1.37A
20180213
For 3VSB no 100uF dip cap.
R914 100K1%4
R912 82K1%4
C713 X_0.1u16
C717 1u16X6
ENABLE HIGH:1.6V
VSB_ENABLE#
Q68 N-PM514BA_SOT23-3-HF
U56
VIN-1
VIN-2
SW-1
SW-2
3VSB_PHASE
CHOKE12 CH-0.47u5A21mS-HF
3VSB_EN
3VSB_PWRGD
PG
OUT
2147_MODE
MODE/VCON
FB
3VSB_FB
0.6V
R906 200KR1%0402
R905 44.2KR1%0402
C724 330p50N
Ramp
GND
MP2147GD-Z_QFN12-RH
C645 22u6.3X8
C719 22u6.3X8
C726 C22u6.3X5-HF
C718 C22u6.3X5-HF
C720 0.1u10
3VDSW
113mA(PCH)+0.6mA(RTC)+90mA(SLG4F42051)
R860 10R1%4
3VDSW_CNTL
C633 1u6.3X4
35 3VDSW_PWRGD
U59
POK
R856 47K/4 3VDSW_EN
VIN
NC
C611 10p50N4
R748 31.6K1%4
3VDSW_FB
R752 10K1%4
GS7133SO-R_PSOP8-HF
Vout=0.8x(R1+R2)/R1
C638 10u6.3X6
C607 X_10u6.3X6
C606 10u6.3X6
C608 0.1u16X4
AVL:I31-3730S02-N62
R2364 X_47K/4
R2363 47K/4
Q227 NN-2N7002D
3VSB_PWRGD_SLG 35
C1927 X_0.1u16
R913 10K
R909 X_10K
C727 0.1u10
For Layout.
C1937 0.1u16
C1936 0.1u16
C1935 0.1u16
C1928 0.1u16
C1929 0.1u16
C1930 0.1u16
C1931 0.1u16
C1932 0.1u16

MICRO-STAR INT'L CO.,LTD		
MS-7C13		
Size: Custom	Document Description: ACPI CONTROLLER	Rev: 10
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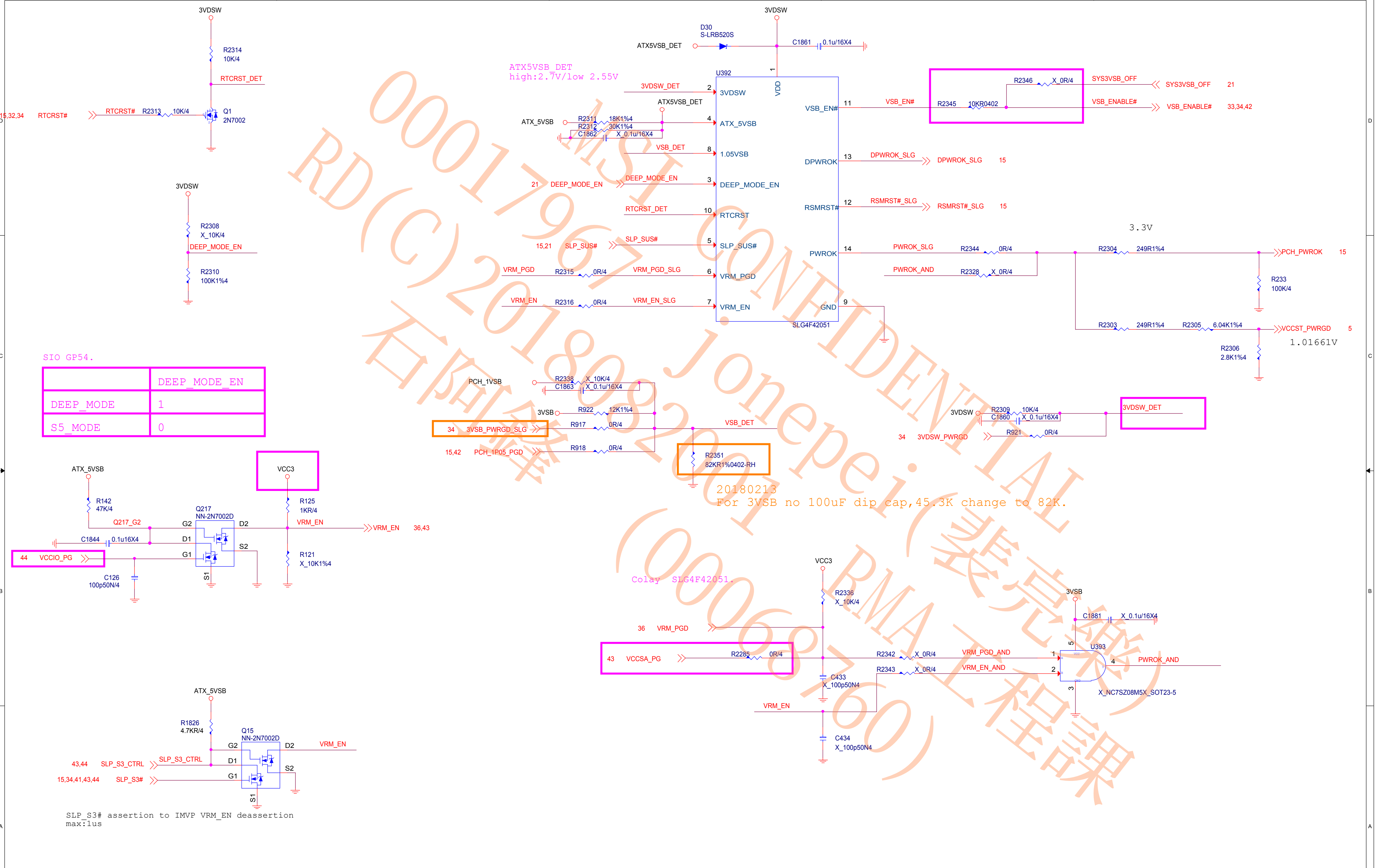

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00017967 Jonepei(裴亮乘)
RD(C)20180620 BA工程課
石南德
(00068760)

MICRO-STAR INT'L CO.,LTD

MS-7C13

Size	Document Description	Rev
Custom	M.2-SLOT1	10

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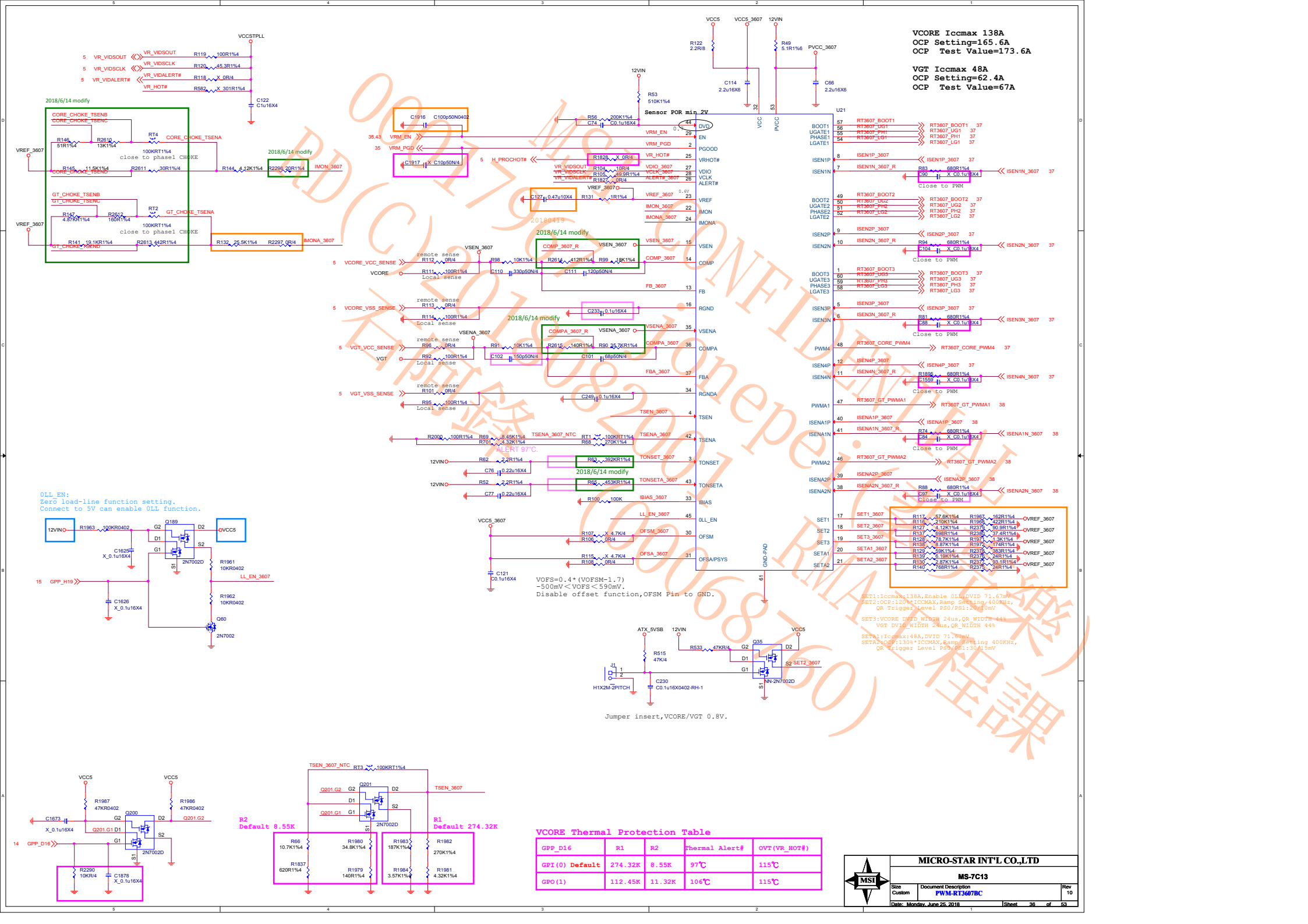
VCORE Iccmax 138A
OCP Setting=165.6A
OCP Test Value=173.6A
VGT Iccmax 48A
OCP Setting=62.4A
OCP Test Value=67A
U21
RT3607_CORE_PWM4
RT3607_GT_PWMA1
RT3607_GT_PWMA2
0LL_EN:
Zero load-line function setting.
Connect to 5V can enable 0LL function.
VOFS=0.4*(VOFSM-1.7)
-500mV<VOFS<590mV.
Disable offset function,OFSM Pin to GND.
Jumper insert,VCORE/VGT 0.8V.
R2
Default 8.55K
R1
Default 274.32K
VCORE Thermal Protection Table
GPP_D16 | R1 | R2 | Thermal Alert# | OVT(VR_HOT#)
GPI(0) Default | 274.32K | 8.55K | 97℃ | 115℃
GPO(1) | 112.45K | 11.32K | 106℃ | 115℃
MICRO-STAR INT'L CO.,LTD
MS-7C13
Size Custom
Document Description PWM-RT3607BC
Rev 10
Date: Monday, June 25, 2018
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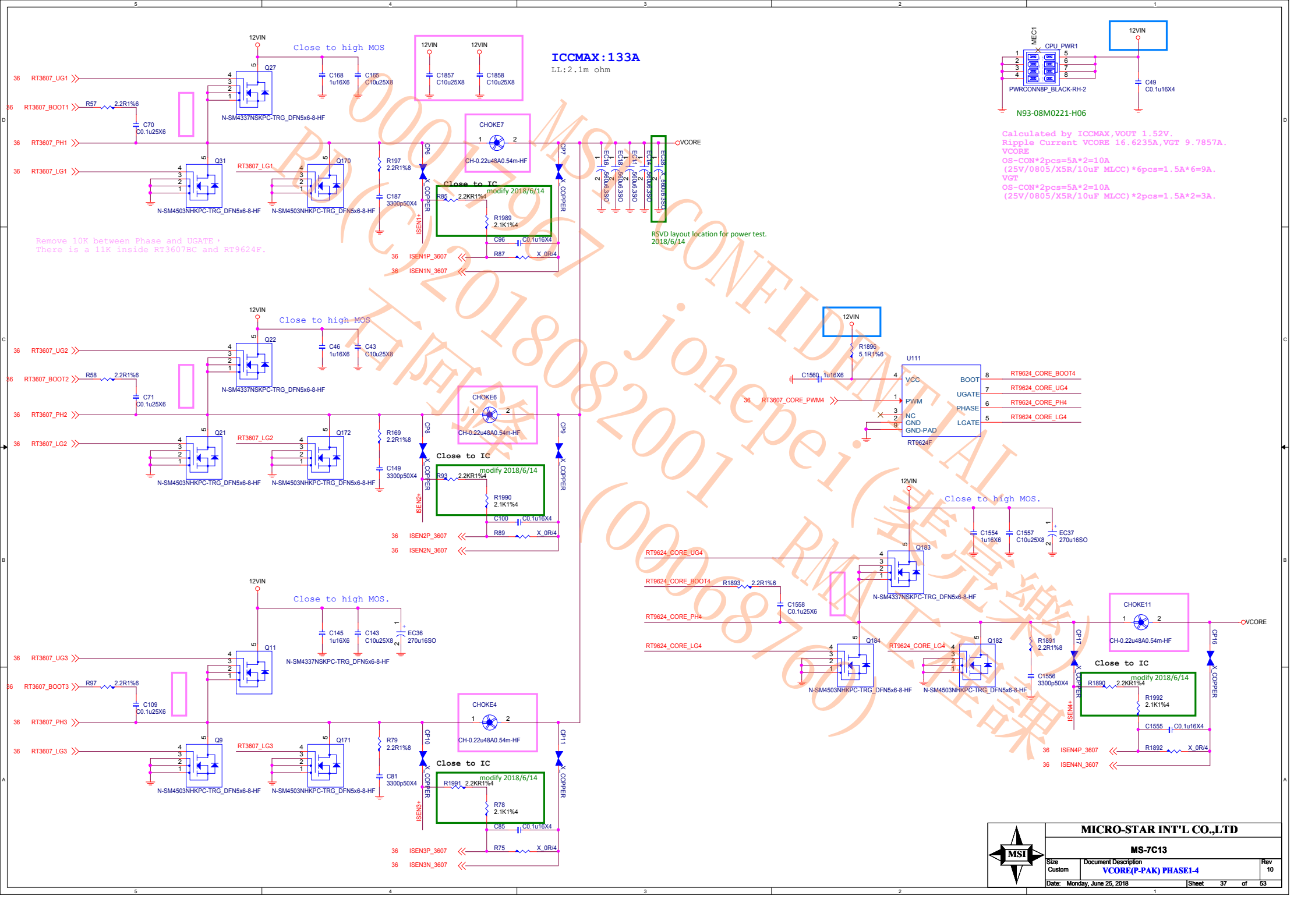
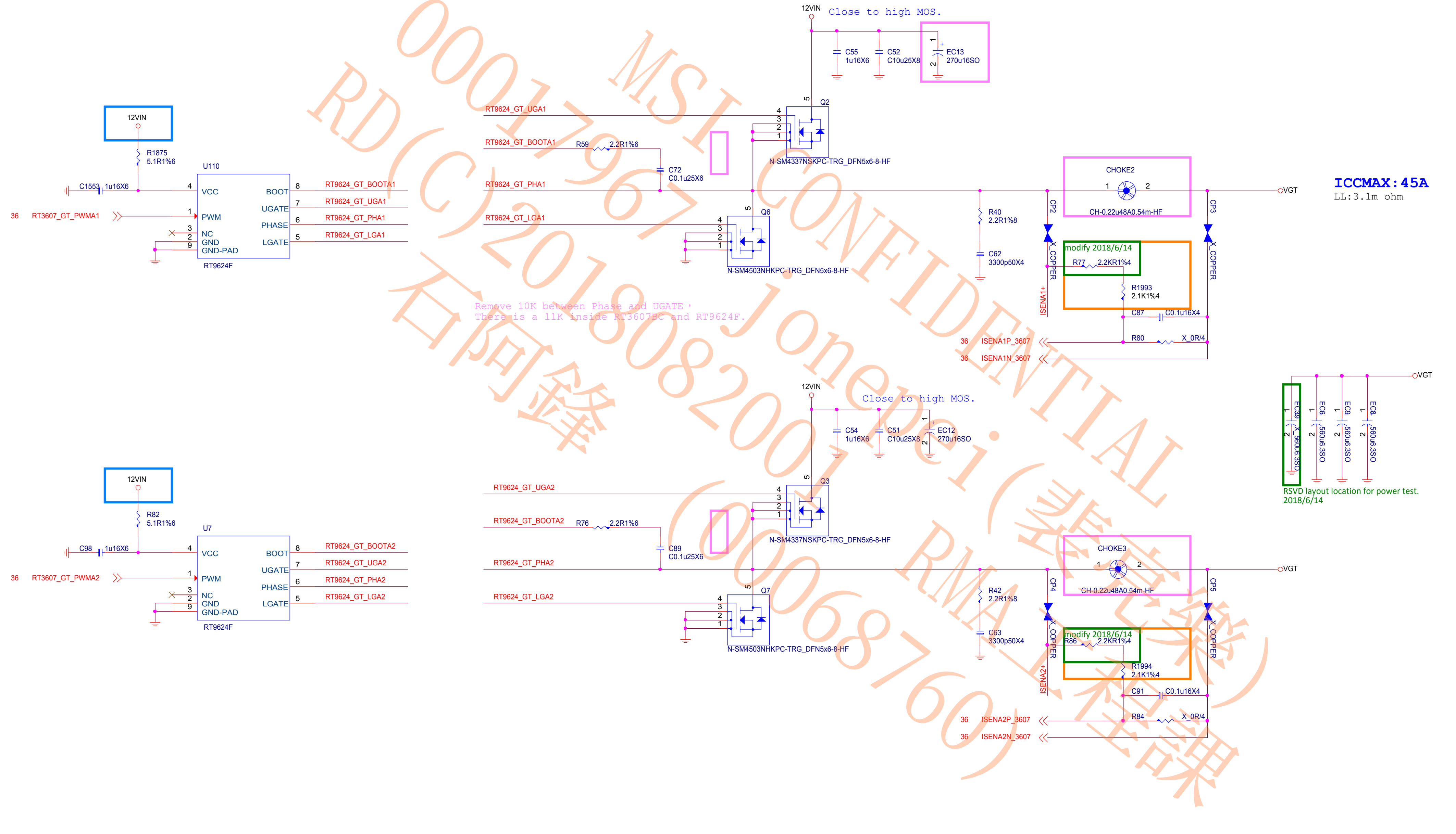


MICRO-STAR INT'L CO.,LTD	
MS-7C13	
Size: Custom	Document Description: VCORE(P-PAK) PHASE1-4
Rev: 10	
Date: Monday, June 25, 2018	Sheet 37 of 53



MSI CONFIDENTIAL
000179675
RD(C)20180820017 Jonepei(裴宗樂)
石阿鋒
(00068760) RMA工程課

MICRO-STAR INT'L CO.,LTD		
MS-7C13		
Size: Custom	Document Description: VGT(P-PAK) PHASE1-2	Rev: 10
Date: Monday, June 25, 2018	Sheet 38 of 53	

DDR4_1.2V 3.3A+ 7.85A+0.35A+0.13A=11.63A

3.3A FOR CPU
7.85A FOR 2DIMM DDR4
0.35A FOR VTT_DDR
0.13A FOR VCCPLL_OC

D03-632BA0C-N03 3~4.6mohm/4.5V
Current limit= 140K*5uA/4.6mohm)= 15.217A
Current limit= 140K*5uA/3mohm)=23.333A
Output Choke Isat=32A

OCP Test Value=20.32A

Vcs=140K*5uA=0.7V(Spec:0.4V~3V)

Vout=0.75V/1.65K*(1.65K+1K)=1.204V

NCT3933 source 10uA
Vout=[VREF*(1+R173/R1056)]+10uA*R173
=0.75V*(1+1K/3.16K)+10uA*1K=1.204V+0.010V=1.214V

NCT3933 sink 10uA
Vout=[VREF*(1+R173/R1056)]-10uA*R173
=0.75V*(1+1K/3.16K)-10uA*1K=1.204V-0.010V=1.194V

Iin=IOCP*Vout/0.8/Vin
Iin:4.565A~6.9999A
L02-3008043-M26
Over 85℃ ,Rated Current 1.5A,need check bead temp.

VID Pin	VREF (V)
H	0.675
L	0.75

Irms = Iout * SQRT((Vout/Vin) * (1-(Vout/Vin)))
=9.525 * 0.427
= 4.06797A

f:426.57KHz(Spec:320KHz to 480KHz)
tON:636.4456ns (Spec:100ns to 3us)

Current Limit 2.6A

0.1uFx1 per dimm

Change MOS P/N.
hi: D03-616BA0C-N03 change to D03-4337N0C-ST8.
lo: D03-632BA0C-N03 change to D03-4503N0C-ST8.
2018/6/6

Main:L04-82B7181-T15
AVL:L04-82B7211-L65

MAX:9.525A

1.2V

L=tON*(VIN-VDDQ)/(LIR*ILOAD(MAX))
tON=636.4456ns
LIR:20%~40%
L:0.63uH~1.27uH.

SLP_S4# de-assertion to VDDQ ramp down start

VPP ramp down after VDDQ ramp down

MS-7981 Add. Package C-states above C8 function

UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K

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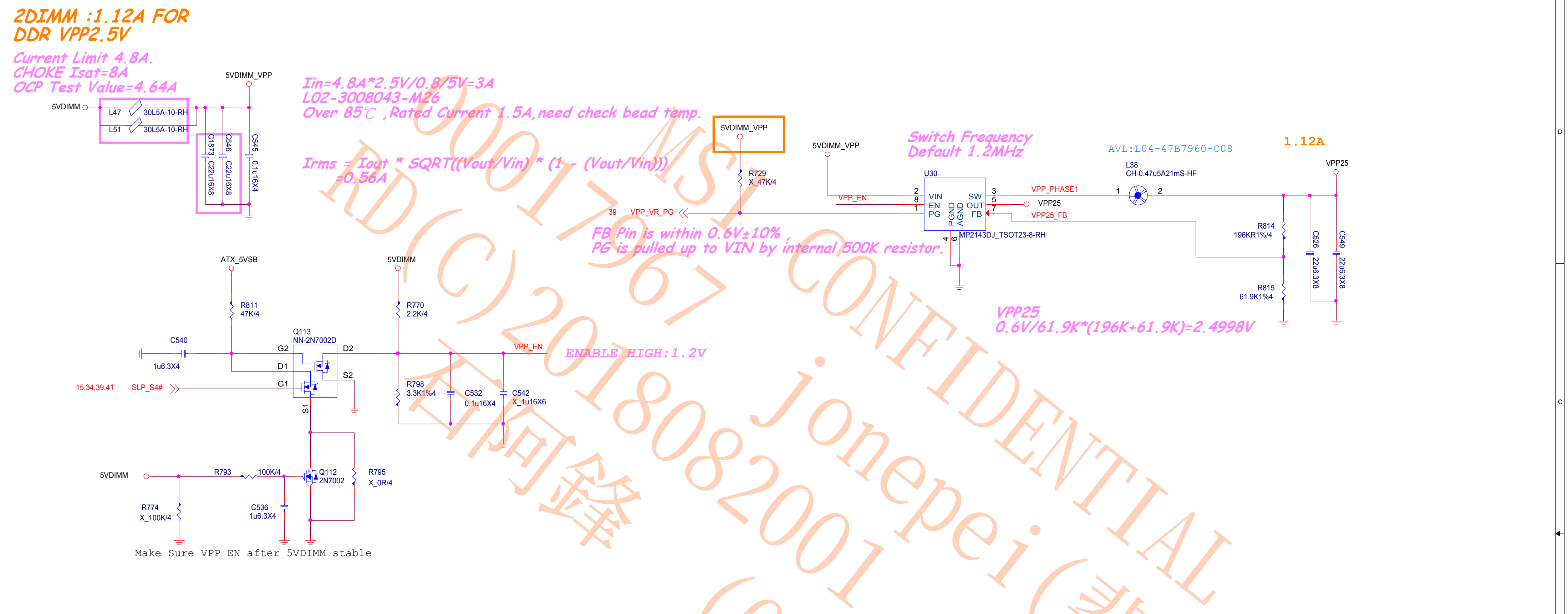
RD(C)2018/6/1 joinepc1(吴建荣)
(0006876) RMA(不提供)

MICRO-STAR INT'L CO.,LTD	
MS-7C13	
Size: Custom	Document Description: DDR-RT8231
Rev: 10	
Date: Monday, June 25, 2018	Sheet 39 of 53



000179967 MSI CONFIDENTIAL
RD(C)20180820001 jonepei(裴亮樂) 石向鋒 (00068760) RMA工程課

MICRO-STAR INT'L CO.,LTD

MS-7C13

Size	Document Description	Rev
Custom	DDR-MP2143-VPP25	10

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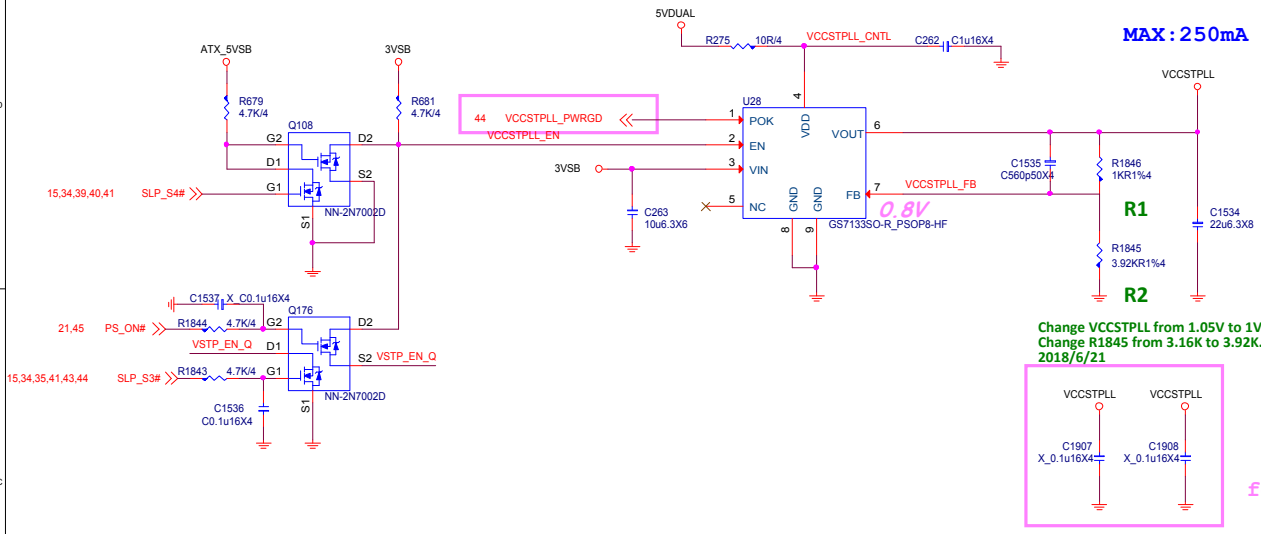
VCCSTPLL

1.05V; 250mA



Change VCCSTPLL from 1.05V to 1V for spec.
Change R1845 from 3.16K to 3.92K.
2018/6/21

for Layout.

VCCSTPLL
Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(1K/3.92K))
= 1.004V

Current limit 3.8A.

PD(MAX)=1.33W

Vout 0.8V~1.6V:C1535 470pF~1nF,R1846 0~10KOhm

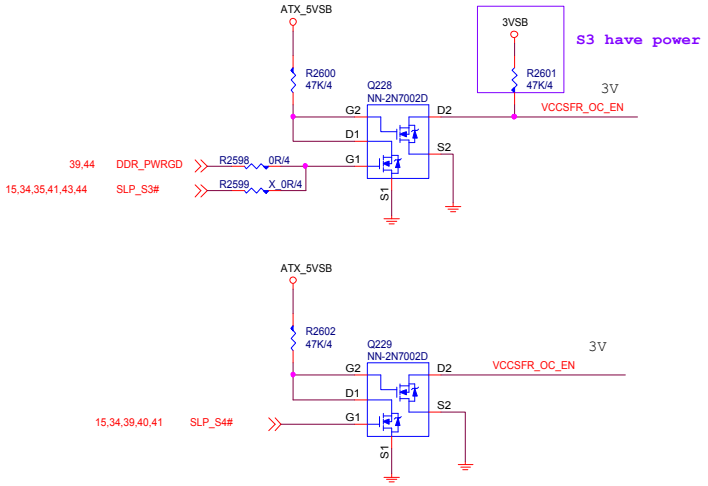
VDD 3.0V~5.5V,POR 2.4V~3.0V.
VIN 1.0V~5.5V,POR 0.55V~0.95V.

EN Vih:1.4V Vil:0.6V

POK:As Vout arrives 92% of normal output voltage, then output the POK pin high to indicate the output is OK.

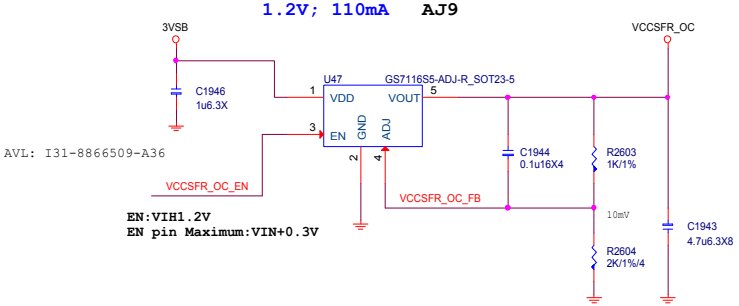
VCCPLL_OC

2018/6/12 add.



from NCT3933

1.2V; 110mA AJ9



AVL: I31-8866509-A36

EN:VIH1.2V
EN pin Maximum:VIN+0.3V

MICRO-STAR INT'L CO.,LTD
MS-7C13
Size: Custom
Document Description: CPU PWR_ST/PLL
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PCH_1VSB

1.0V; MAX:11.043A

Current limit= 6.65K*10uA/3.9mohm)=17.05A
Current limit= 6.65K*10uA/5.1mohm)=13.04A
CHOKE Isat=18A
From CHOKE I-L Curve,when I=25A, L=0.6uH.

4503 Rdson
10V 2.5~3mohm
4.5V 3.9~5.1mohm

Default Vout=1V

NCT3933 sink 10uA
VREFIN =VREFOUT-10uA*R406=796mV-8mV=788mV
Vout=[VREFOUT*(1+R434/R435)]+△Vout/2
=0.788V*(1+1K/3.92K)+17.18mV/2=0.997V

NCT3933 source 10uA
VREFIN =VREFOUT+10uA*R407=796mV+8mV=804mV
Vout=[VREFOUT*(1+R434/R435)]+△Vout/2
=0.804V*(1+1K/3.92K)+17.18mV/2=1.0177V

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
=8.72 * 0.276
=2.407A

Iin=IOCP*Vout/08/Vin
=17.05A*1.V/0.8/5V=4.2625A
L02-3008043-M26
Over 85℃ ,Rated Current 1.5A.

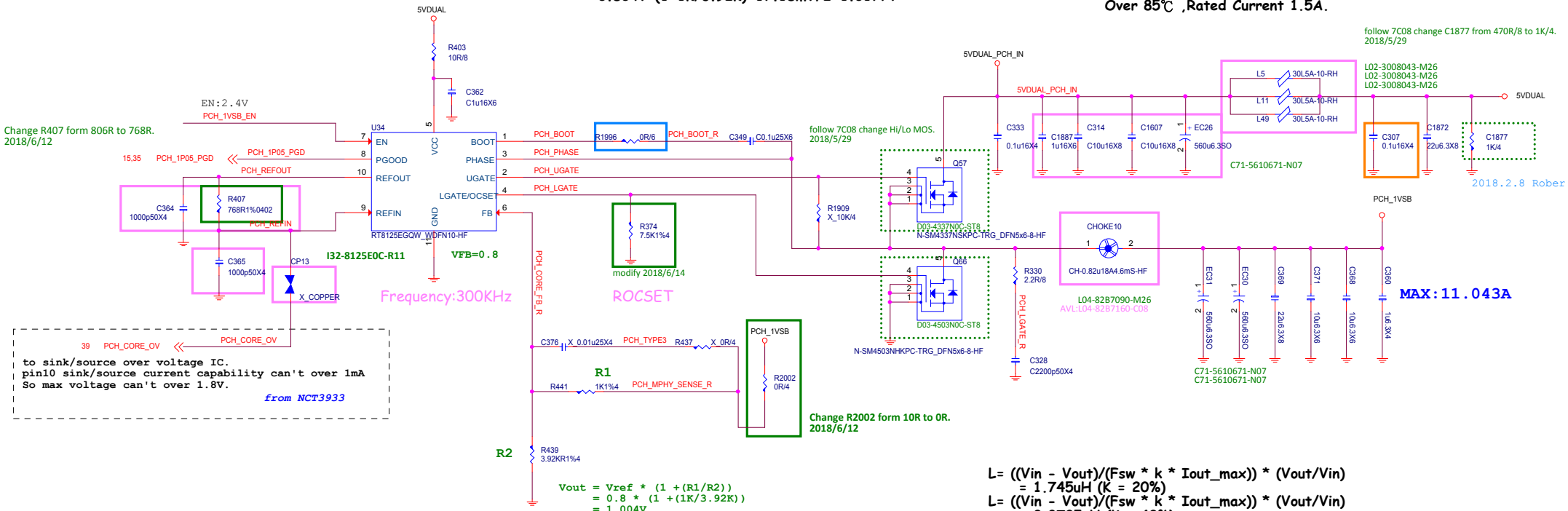
follow 7C08 change C1877 from 470R/8 to 1K/4. 2018/5/29

Change R407 form 806R to 768R. 2018/6/12

follow 7C08 change Hi/Lo MOS. 2018/5/29

modify 2018/6/14

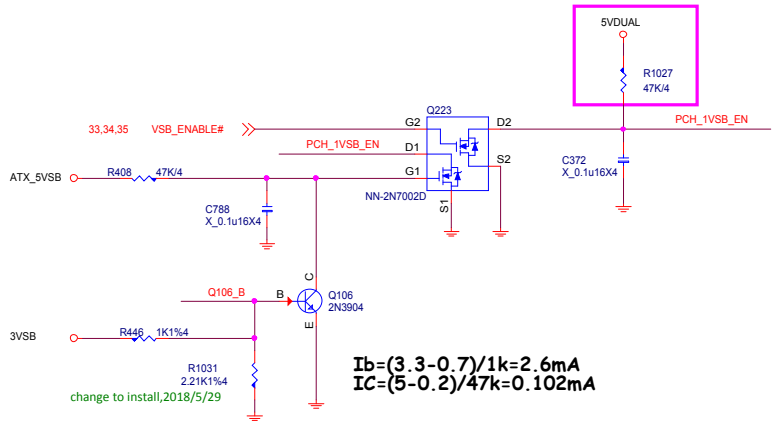
2018.2.8 Rober



L= ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 1.745uH (K = 20%)
L= ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.8725uH (K = 40%)
K is the ratio between inductor ripple current and rated output current.
20%<k<40%

Vout=[VREFOUT*(1+R434/R435)]+△Vout/2
=0.796V*(1+1K/3.92K)+17.18mV/2=1.007V
VREFOUT=0.796V

△Vout_ESR = △IL*ESR =40%*8.72A*4mOhm=13.952mV
△Vout_C = △IL*1/(8*Cout*fSW) =40%*8.72A /(8*560uF*2*300KHz)=1.3mV
Vout_SAG=ESR*△ Iout=4mOhm*10.743A=34.88mV



Ib=(3.3-0.7)/1k=2.6mA
IC=(5-0.2)/47k=0.102mA

MICRO-STAR INT'L CO.,LTD
MS-7C13
Size: Custom
Document Description: PCH Core power
Rev: 10
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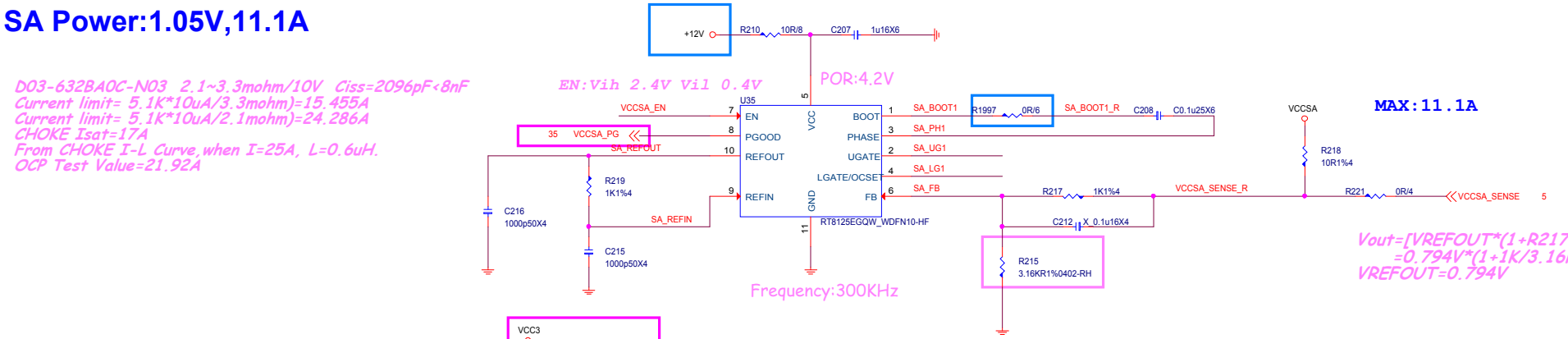
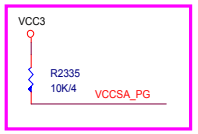
SA Power:1.05V,11.1A

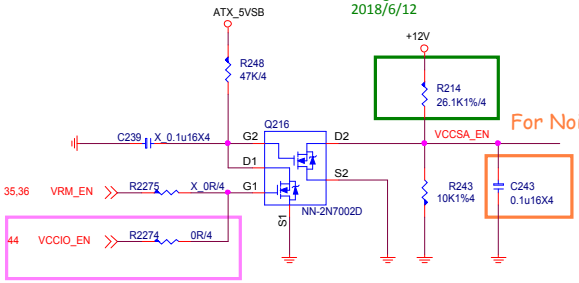
D03-632BA0C-N03 2.1~3.3mohm/10V Ciss=2096pF<8nF
Current limit= 5.1K*10uA/3.3mohm)=15.455A
Current limit= 5.1K*10uA/2.1mohm)=24.286A
CHOKE Isat=17A
From CHOKE I-L Curve,when I=25A, L=0.6uH.
OCP Test Value=21.92A



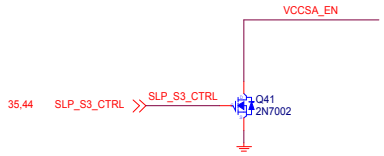
Vout=[VREFOUT*(1+R217/R215)]+△Vout/2
=0.794V*(1+1K/3.16K)+17.76mV/2=1.053V
VREFOUT=0.794V



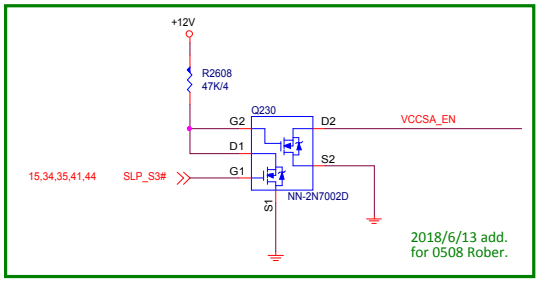
Change R214 from 21.5K to 26.1K.
2018/6/12



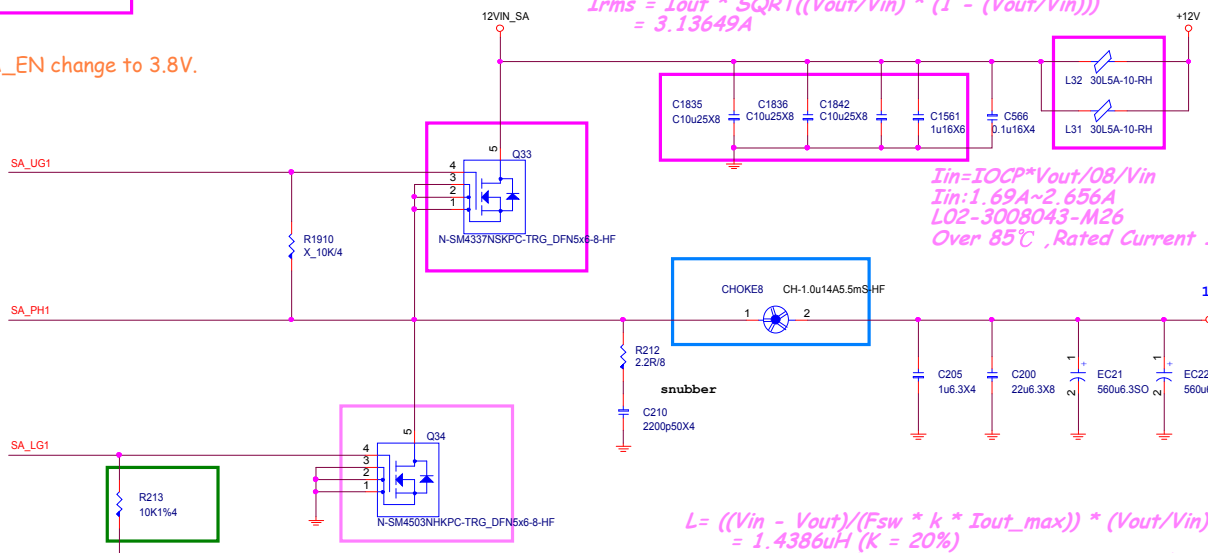
For Noise,VCCSA_EN change to 3.8V.



SLP_S3# assertion to VR disabled
max:1us



Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 3.13649A

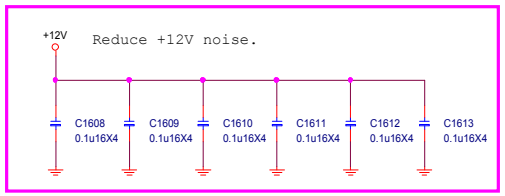


Iin=IOCP*Vout/08/Vin
Iin:1.69A~2.656A
L02-3008043-M26
Over 85℃ ,Rated Current 1.5A,need check bead temp.

Change MOS P/N.
hi: D03-616BA0C-N03 change to D03-4337N0C-ST8.
lo: D03-632BA0C-N03 change to D03-4503N0C-ST8.
2018/6/6

L= ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 1.4386uH (k = 20%)
L= ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.7193uH (k = 40%)
K is the ratio between inductor ripple current and rated output current.
20%<k<40%

△Vout_ESR = △IL*ESR =40%*11.1A*4mOhm=17.76mV
△Vout_C = △IL*1/(8*Cout*fSW) =40%*11.1A /(8*560uF*2*300KHz)=1.65mV
Vout_SAG=ESR*△Iout=4mOhm*11.1A=44.4mV



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VCCIO

0.95V; 6.4A

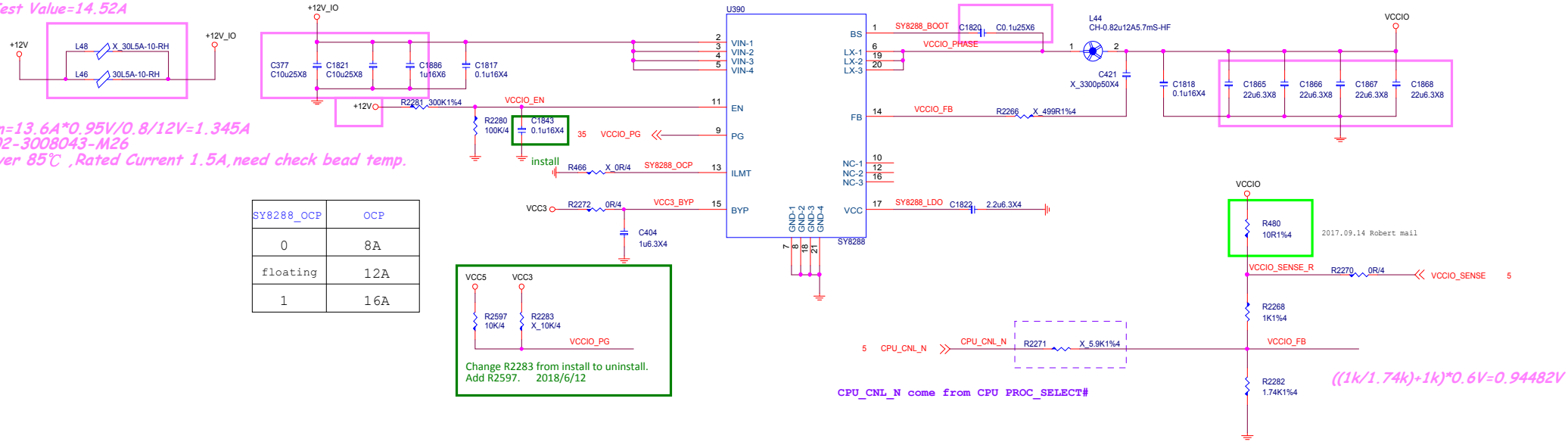
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
=1.72799A

IMAX 8A
ILIMIT=12A
IOC=ILIMIT+40%*IMAX/2=13.6A.
CHOKE Isat=15A
OCP Test Value=14.52A

L=Vout*(1-Vout/Vin)/(Fsw*Iout*40%)
=0.95V*(1-0.95V/12V)/(500KHz*6.4A*40%)=0.68uH.

MAX:6.4A

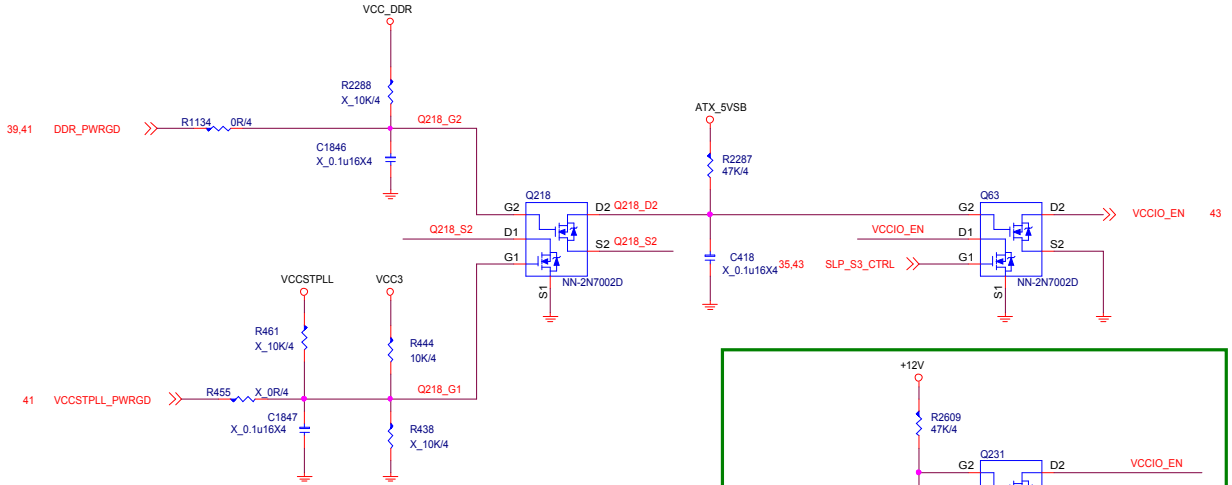
Iin=13.6A*0.95V/0.8/12V=1.345A
L02-3008043-M26
Over 85℃ ,Rated Current 1.5A,need check bead temp.



SY8288_OCP	OCP
0	8A
floating	12A
1	16A

CPU_CNL_N come from CPU PROC_SELECT#

((1k/1.74k)+1k)*0.6V=0.94482V



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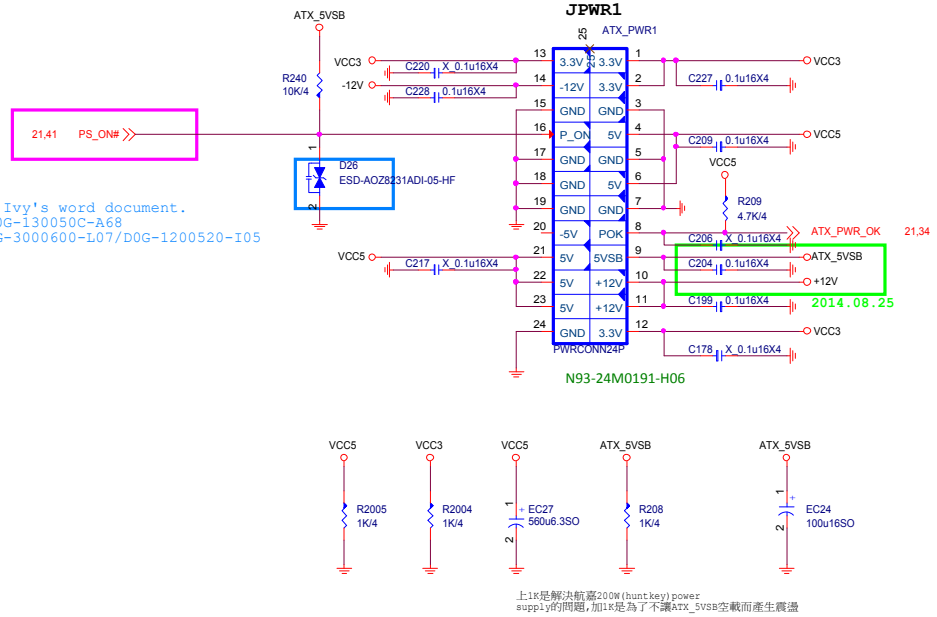
ATX POWER CONNECTOR

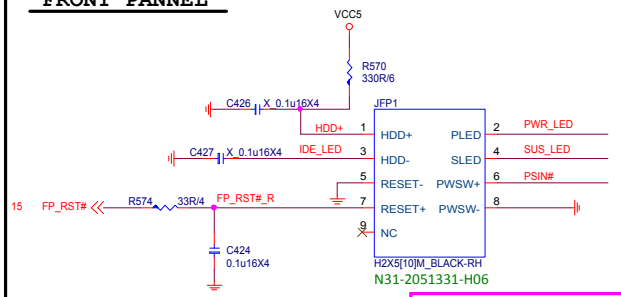
D26:By Ivy's word document.
Main:D0G-130050C-A68
Avl:D0G-3000600-L07/D0G-1200520-I05

7C08:
D26:By Ivy's word document.
Main:D0G-130050C-A68
Avl:D0G-3000600-L07/D0G-1200520-I05

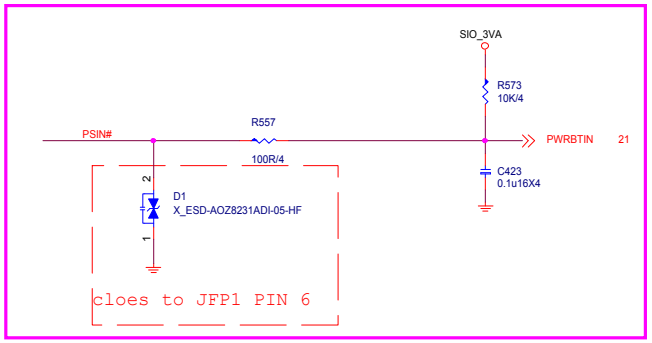


上1K是解決航嘉200W(huntkey)power supply的問題,加1K是為了不讓ATX_5VSB空載而產生震盪

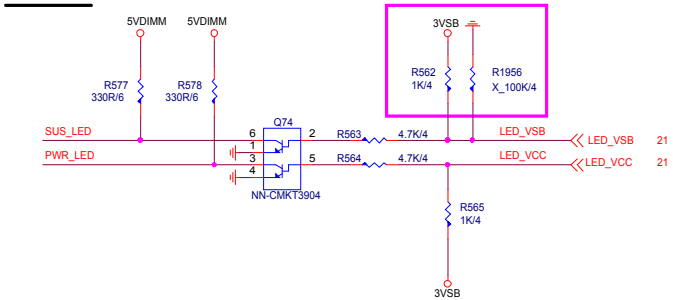
FRONT PANNEL

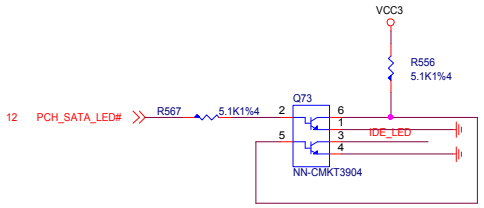


close to SIO

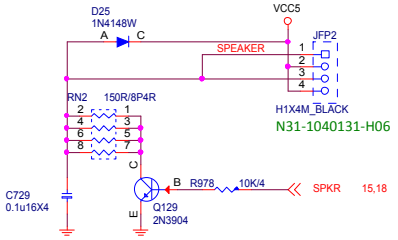


LED



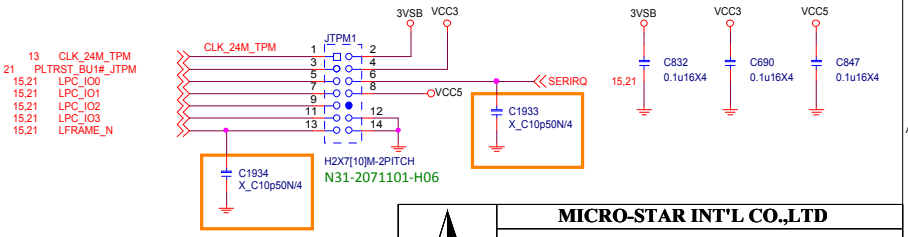


Speaker Pin Header



TPM

Don't colay espi debug.



MSI	MICRO-STAR INT'L CO.,LTD	
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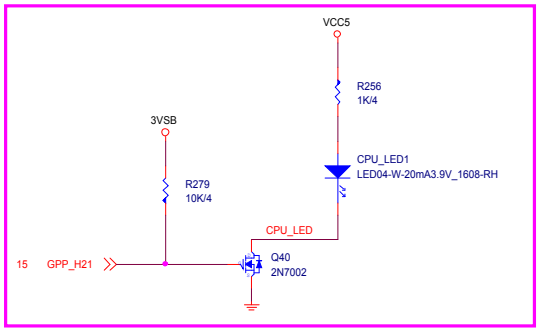
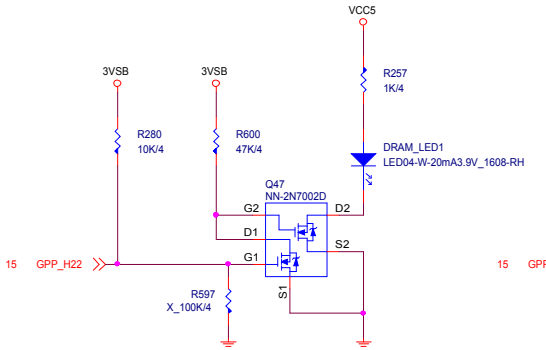
DEBUG LED

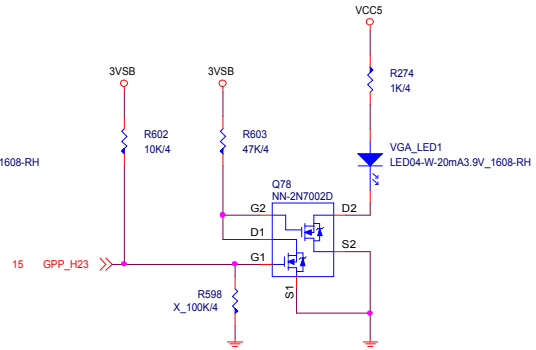
CPU



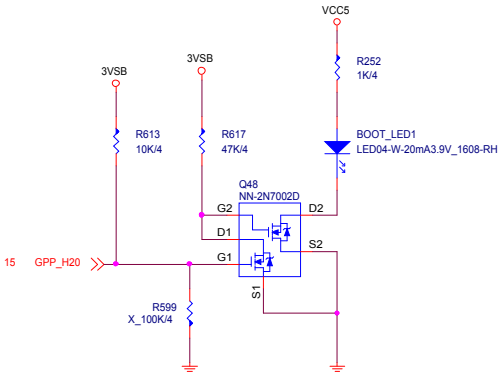
DRAM



VGA



DEVICE



LED	GPP_H21	GPP_H22	GPP_H23	GPP_H20
亮	GPO HIGH	GPO LOW	GPO LOW	GPO LOW
滅	GPO LOW (default LOW)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

LED
RED:D0C-040P100-H91
AVL:D0C-040S500-E07

WHI:D0C-040T200-H91
AVL:D0C-040S200-E07

關機斷電狀態下，3個LED先維持default全暗，開機通電後：

1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
4. 因此最後正常順利開機後，三個LED燈都是滅掉的。（系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

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EMI CAP

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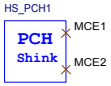
HS_PCH1



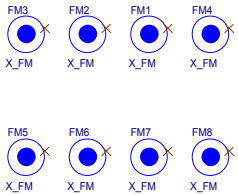
HS-0409430-RH

MSI Heatsink

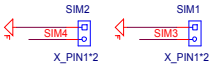
MSI_HS_PCH

X_HS

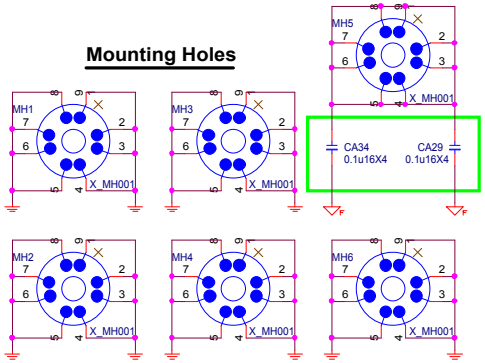
Optical Fiducial Marks-120

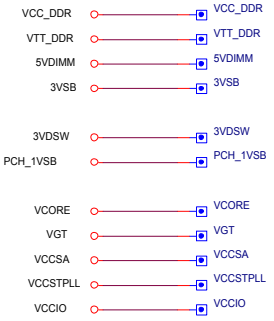


Simulation



Mounting Holes





BAT1_X1

BAT-BCR2032P-RH

CPU_H1

CPU_H1

E21-7557050-L06
AVL:E21-7557060-F02

PCB1

7C13_10

PK0-07C1310-G37

BIOS_LA1

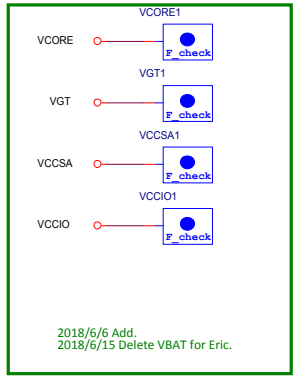
AMI

G51-M1SPXXA-A09

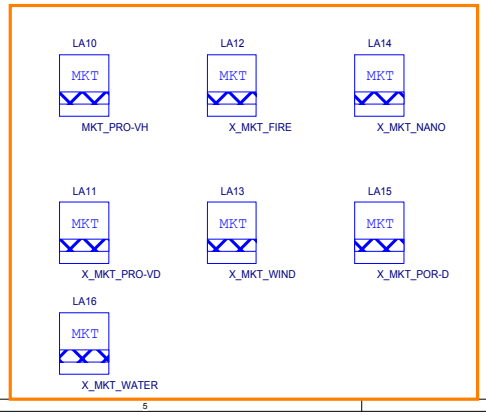
HDMI_LA1

HDMI LABEL

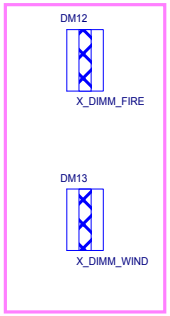
Y01-RHDMI03-000



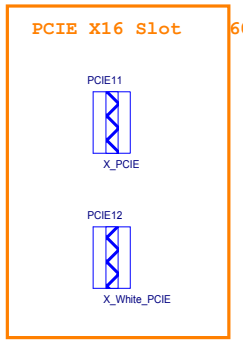
Marketing Name



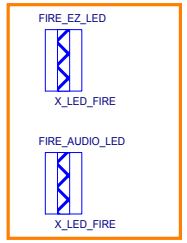
DIMM Slot



PCIE X16 Slot



601-7B33-10S LED



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