PCB NO : DAB00089000

BOM P/N :

Compal Confidemntial

FP6 BCEZANNE-H MB SCHERMATIC DOCUMENT

GDL56 LA-K453P

2021-02-05 REV 1.0 (A00)

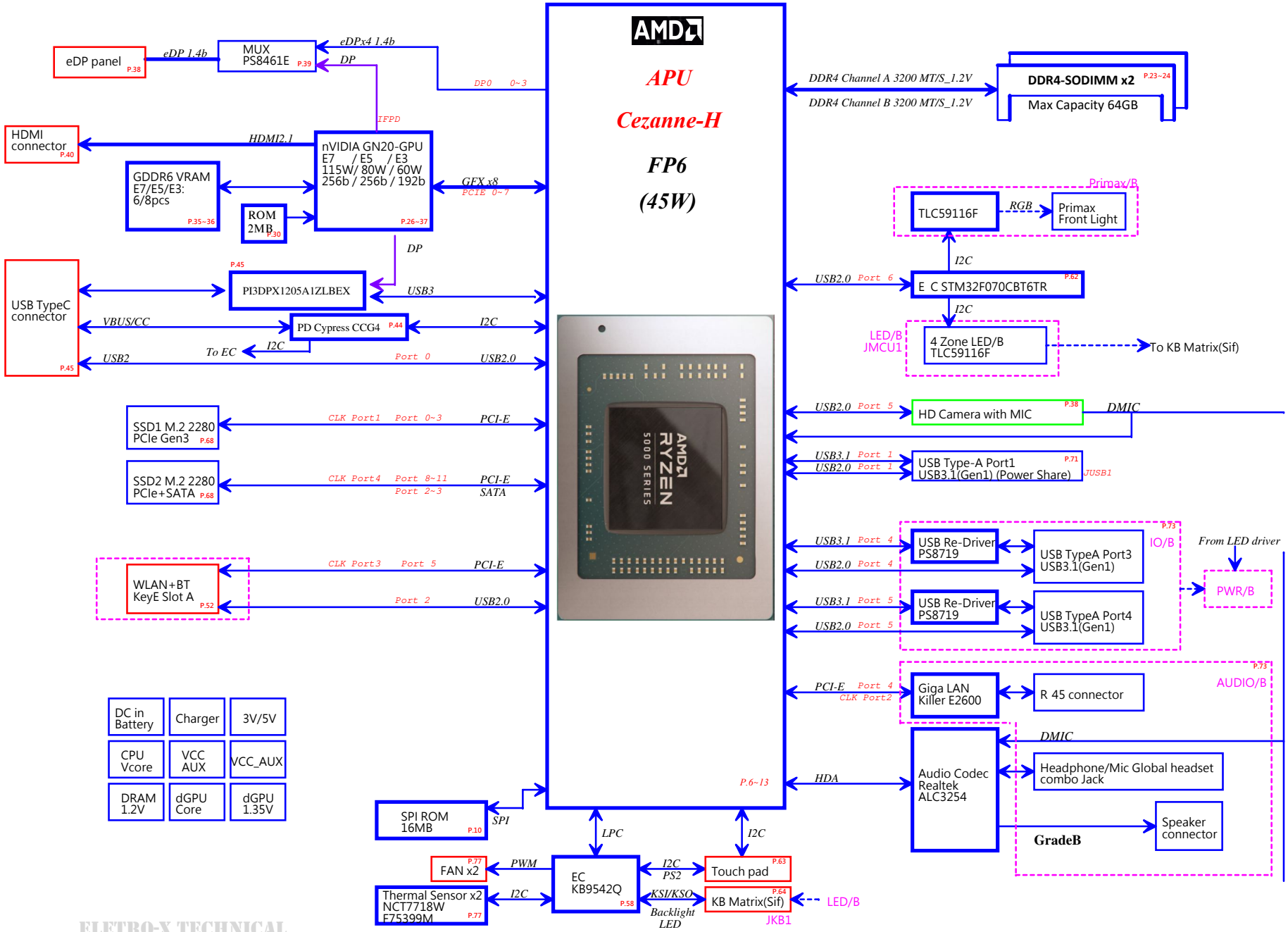
@ : Un-pop Component

EMI@/ESD@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component
CONN@ : Connector Component
DDS@: DDS function

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2021/12/31

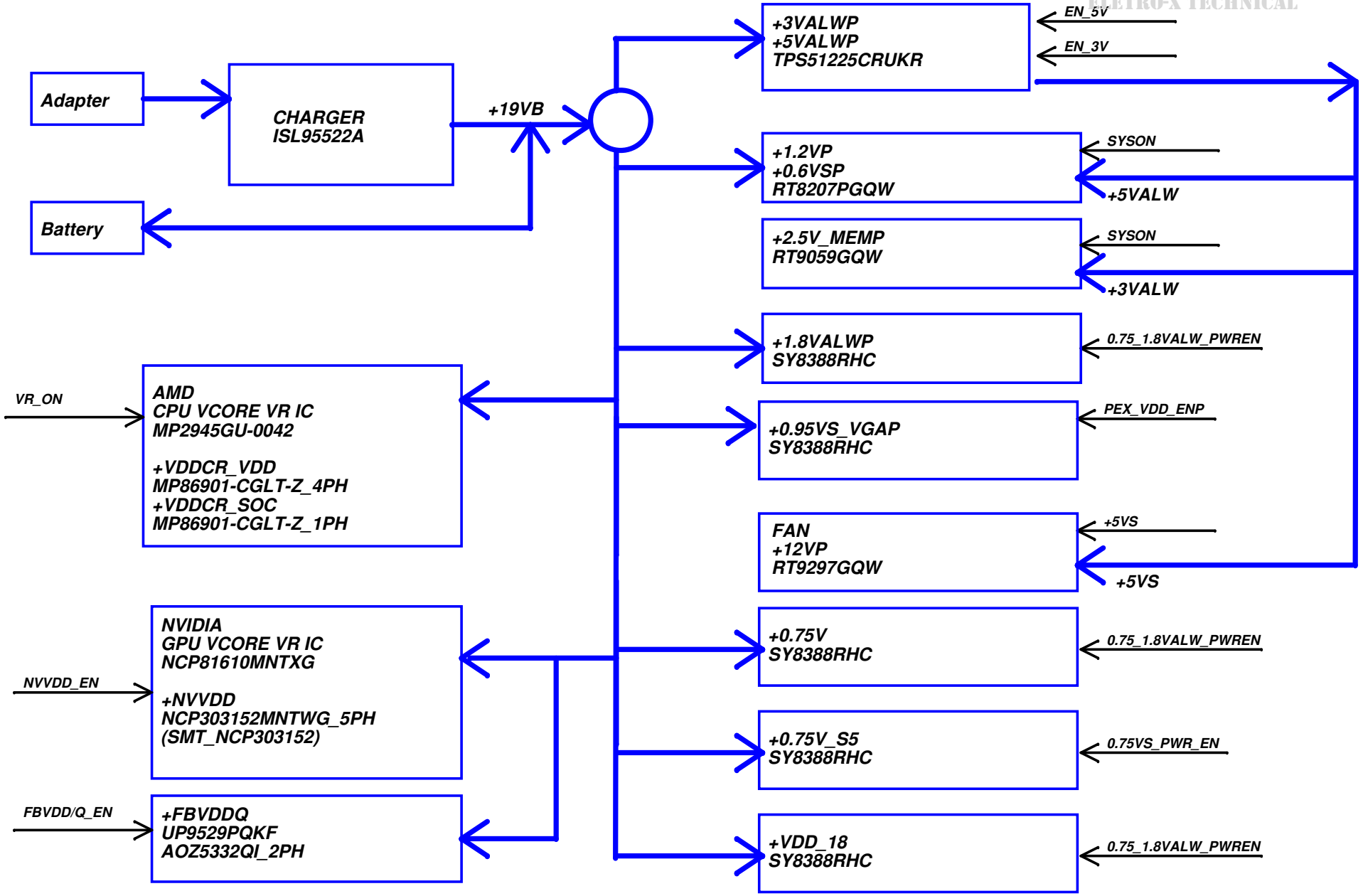
Compal Electronics, Inc.		
Title: Cover Sheet		
Size: Custom	Document Number: LA-K453P	Rev: 0.1
Date: Friday, February 05, 2021	Sheet 1 of 121	

Block Diagram

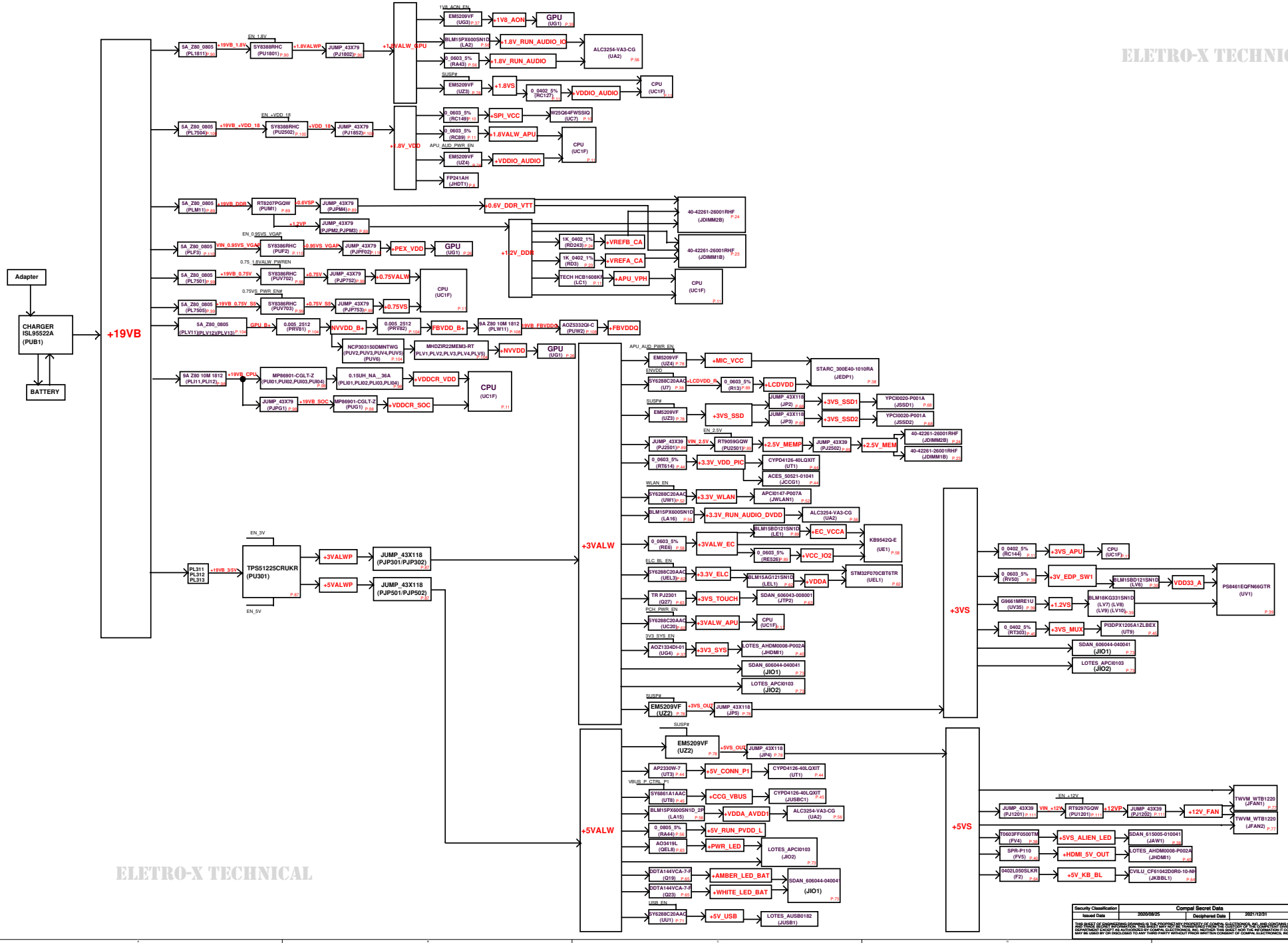


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2018/02/05	Title: Block Diagram
			Document Number: LA-K453P
			Rev: 0.1
Date: Friday, February 05, 2021		Sheet 2 of 121	

Power block



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2021/08/01	Title: PWR_POWER BLOCK DIAGRAM
			Size: B29 Document Number: LA-K453P Rev: 0.1
			Date: Friday, February 05, 2021 Sheet 81 of 121



Security Classification	Compal Secret Data		
Issued Date	2020/08/25	Deciphered Date	2021/12/31

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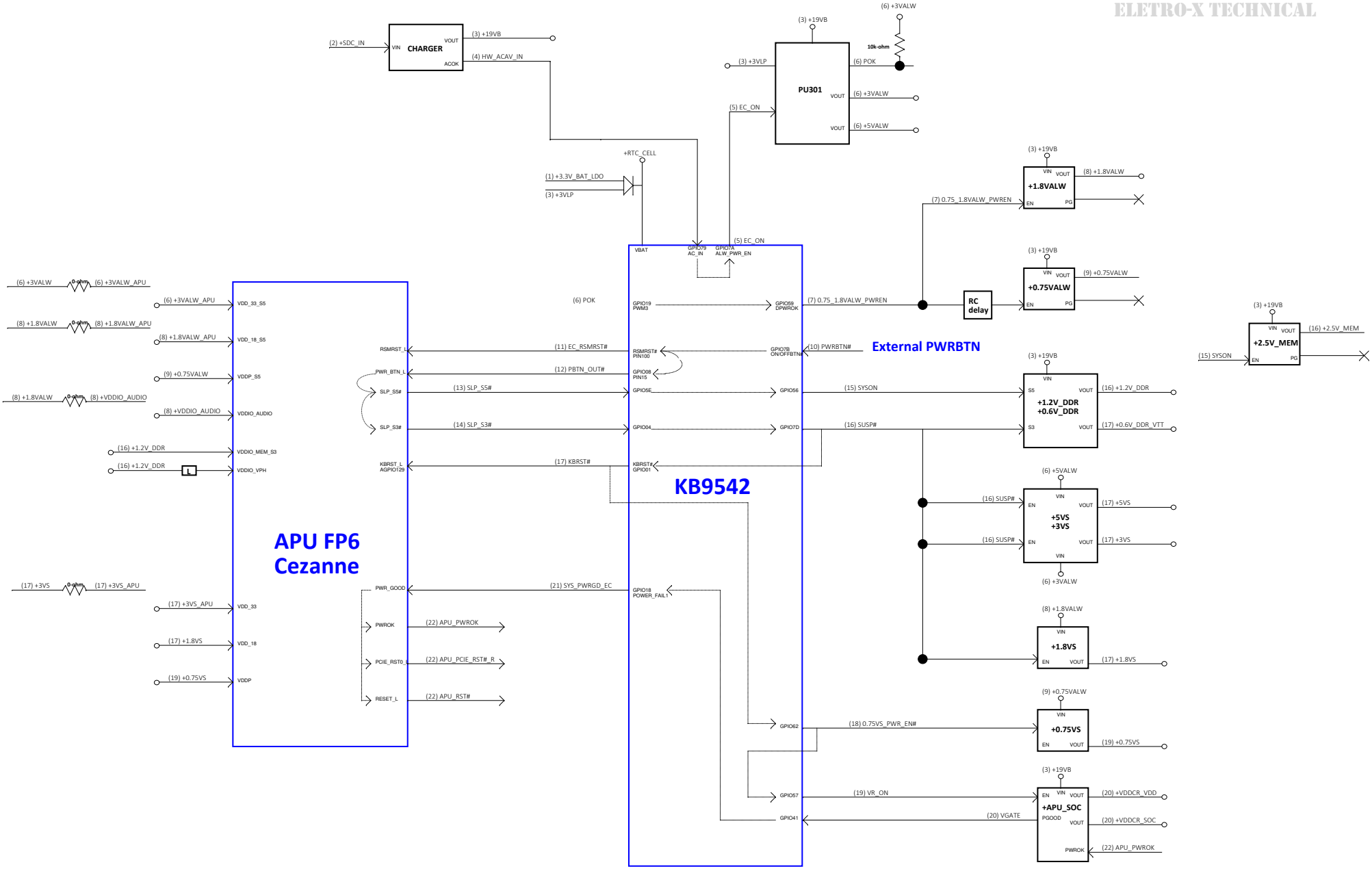
Compal Electronics, Inc.

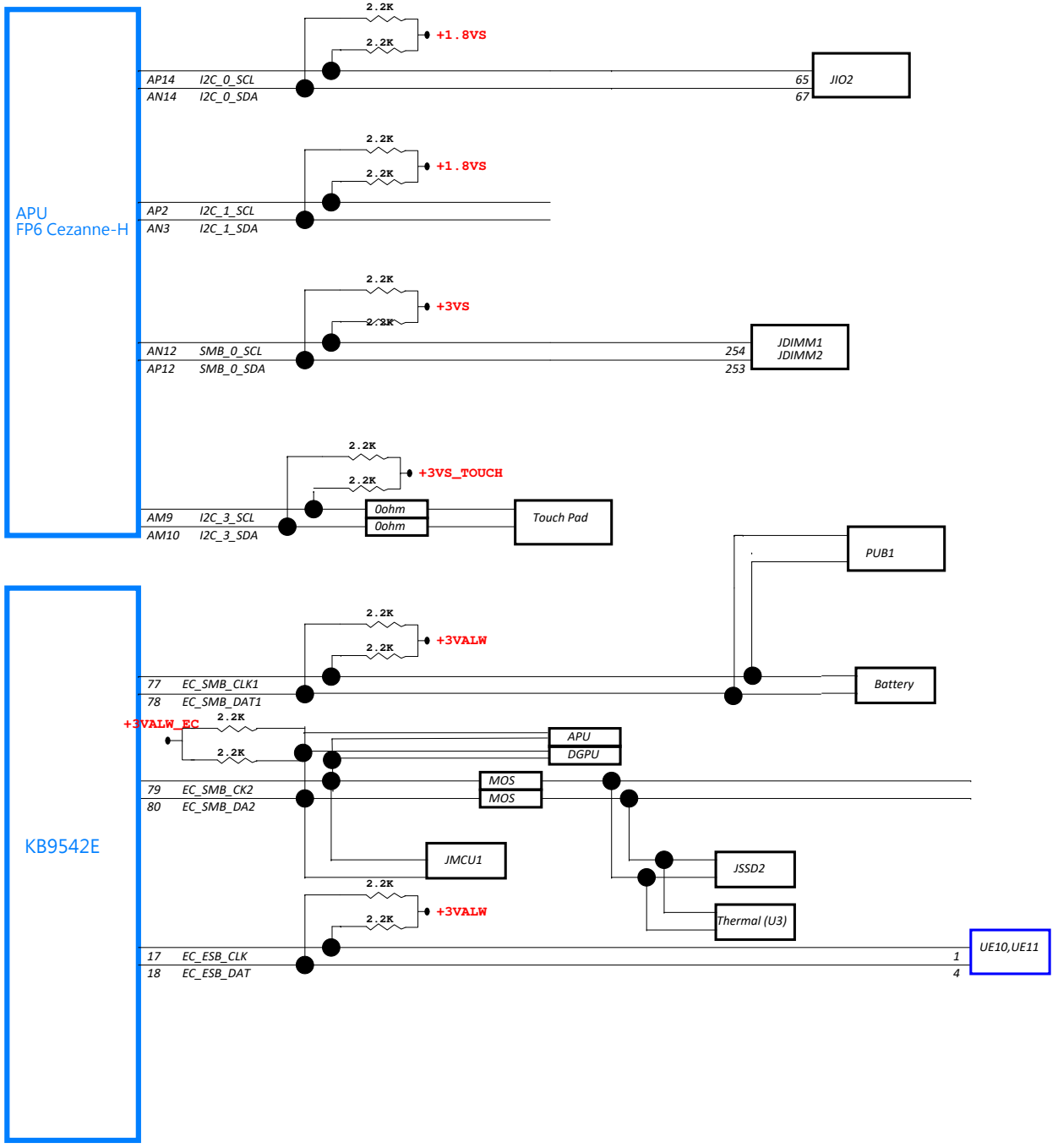
Title: Power Map

Size: C | Document Number: LA-K453P | Rev: 0.1

Date: Friday, February 05, 2021 | Sheet 4 of 182



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/04/01	Deciphered Date 2019/04/01	Title: Power Sequence Diagram
Document Number: LA-K661P			Rev: 0.1
Date: Friday, February 05, 2021	Sheet 75 of 101		



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/02/05

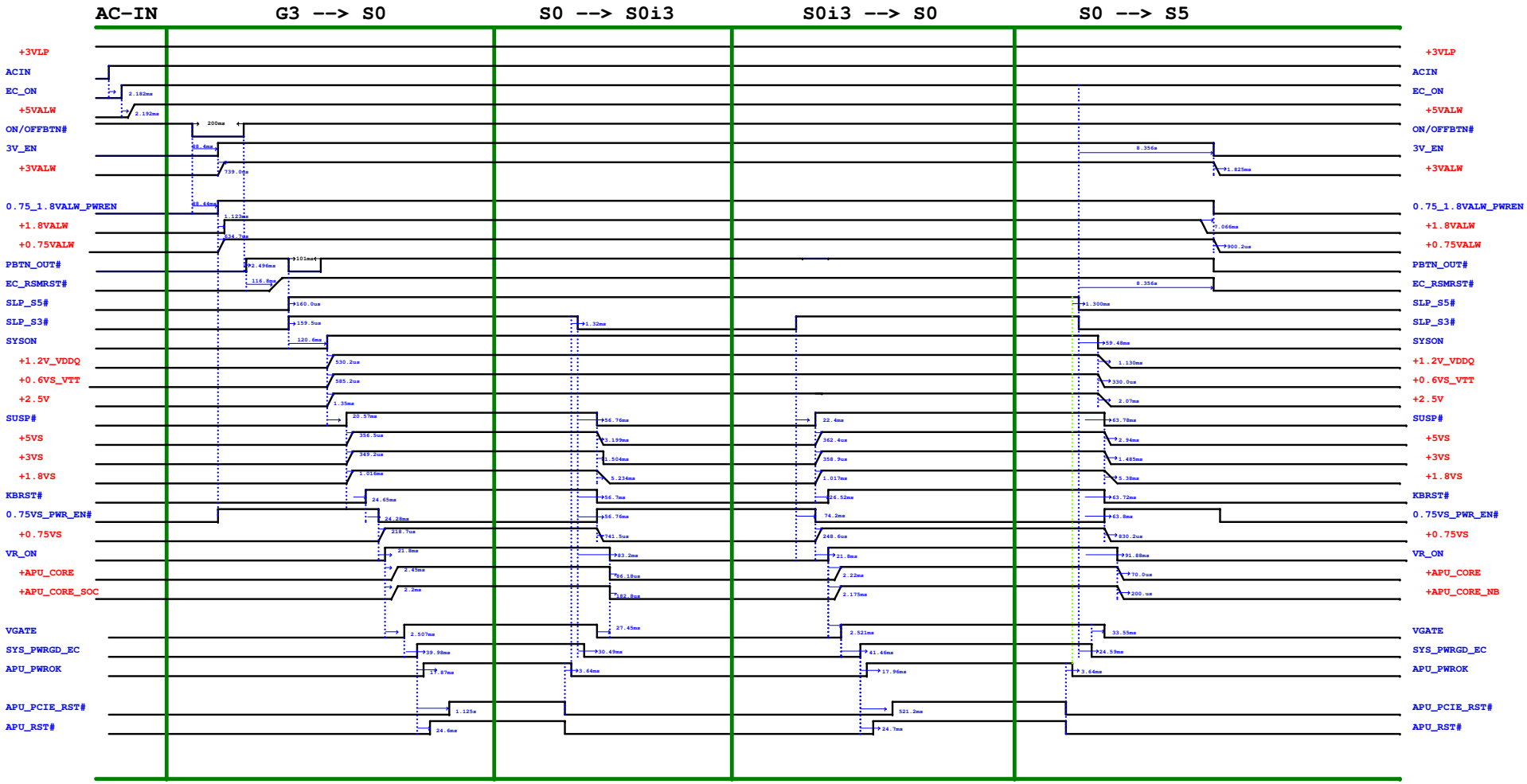
Compal Electronics, Inc.

Title: SMBus Block Diagram

Size: B | Document Number: LA-K453P | Rev: 0.1

Date: Friday, February 05, 2021 | Sheet 61 of 121

Renoir Ridge Platform Power Sequence



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2019/08/26	Deciphered Date	2020/08/26	Title: POWER SEQUENCE
Size: D	Document Number: LA-K453P			Rev: 1.0
Date: Friday, February 05, 2021	Sheet 5 of 121			

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

PCH SMBUS Address Table

PCH_SMBUS Port	Power Rail	Device	Address
PCH_SMBCLK PCH_SMBDATA	+3VALW_PCH	JDIMM1	
		JDIMM2	

Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xF0
19	NC	3.000V	3.300V	3.300V	0xF1 - 0xFF

BOARD ID Table

Board ID	
0	EVT@
1	DVT1@
2	DVT2@
3	PVT@
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	

GPU ID Table

GPU ID	
0	GN20E3@
1	GN20E4@
2	GN20E5@
3	GN20E7@
4	GN20P0@
5	GN20P1@
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address
GPU_THM_SMBCLK GPU_THM_SMBDAT	+3VS		
		Thermal 1 Thermal 2	0x98h 0x9Ah
		GPU (GN20E)	0x9E
PBAT_CHG_SMBCLK PBAT_CHG_SMBDAT	+3VALW_EC	BAT	TBD
		CHGR	TBD
DAT_TP_SIO_I2C_CLK CLK_TP_SIO_I2C_DAT	+TP_VDD	Touch Pad	TBD
UPD1_SMBCLK UPD1_SMBDAT	+3V_VSYS	CCG5C	0x08

HSIO

USB2.0	
Controller0_Port0	TYPE-C
Controller0_Port1	TYPE-A MB
Controller0_Port2	WLAN/BT
Controller0_Port3	Camera
Controller1_Port4	TYPE-A I/O
Controller1_Port5	TYPE-A I/O
Controller1_Port6	ELC
Controller1_Port7	MCU
USB3.0	
Controller0_Port1	TYPE-A MB
Controller1_Port4	TYPE-A I/O
Controller1_Port5	TYPE-A I/O
PCI EXPRESS(GPP)	
Lane0	NVME SSD
Lane1	NVME SSD
Lane2	NVME SSD
Lane3	NVME SSD
Lane4	LAN
Lane5	WLAN
Lane8	NVME SSD
Lane9	NVME SSD
Lane10	NVME SSD
Lane11	NVME SSD

Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5	DS3
+19V_VIN						
+12.6V_BATT+						
+19VB						
+VCC_CORE						
+VCCGT						
+VCCSA						
+VCCIO						
+3.3V_BAT_LDO						
+RTC_CELL						
+5VALW						
+3VALW						
+3VALW_PCH						
+3VALW_DSW						
+1.8V_PRIM						
+1VALW						
+1.2V_DDR						
+0.6V_DDR_VTT						
+2.5V_MEM						
+VCCST						
+VCCSTG						
+5VS						
+3VS						
+1.8VS						

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

ZZZ DAB00089010 PCB@ PCB 36M LA-K453P REV1 MB AMD GN20

ZZZ DAB00089011 PCB@ PCB 36M LA-K453P REV1 MB AMD GN20 GOLD A31

ZZZ DAB00089012 PCB@ PCB 36M LA-K453P REV1 MBAMDGN20 TRIPA31

ZZZ DAB00089013 PCB@ PCB 36M LA-K453P REV1 MB AMDGN20HANNA31

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2021/12/31

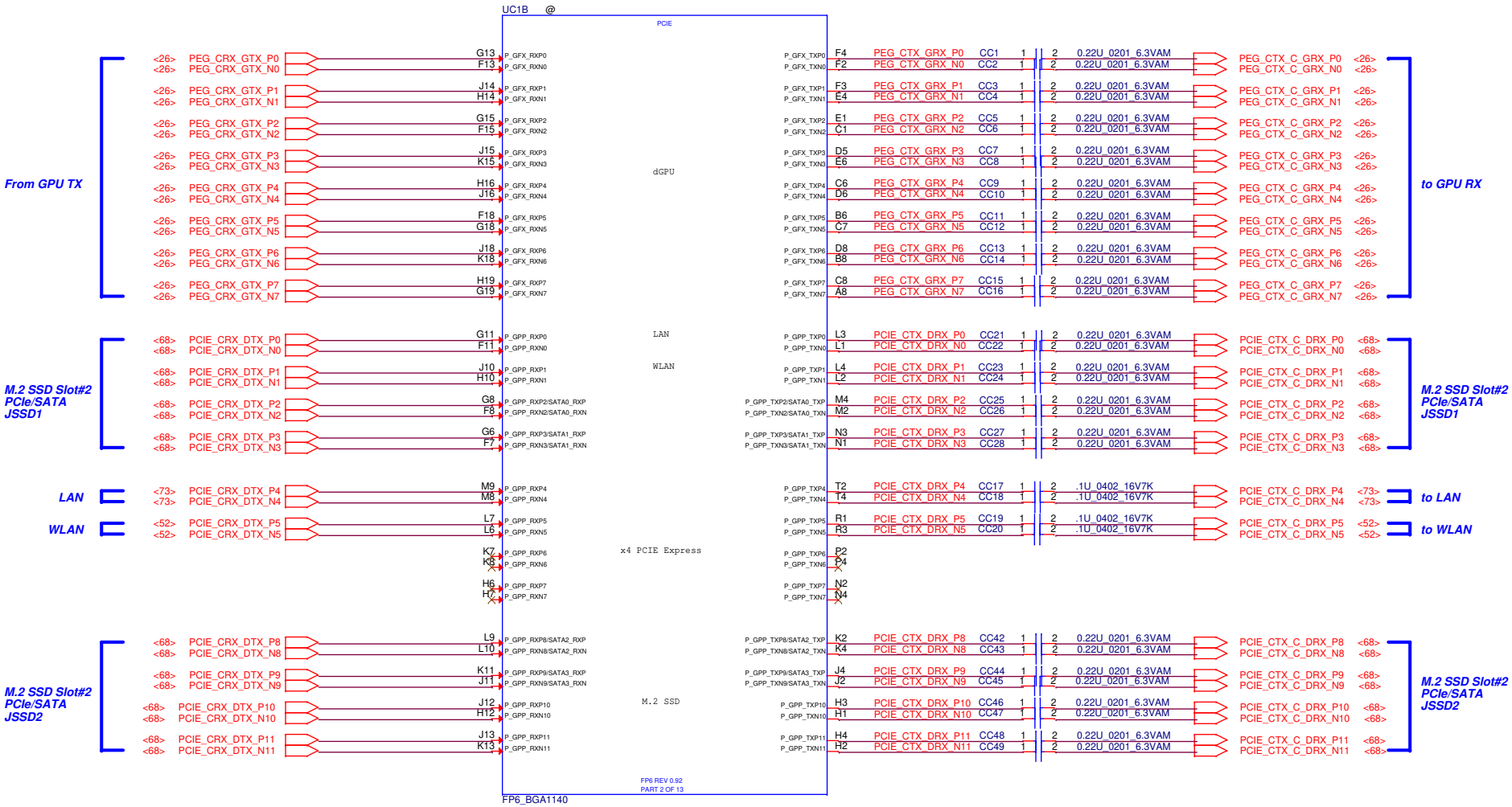
Compal Electronics, Inc.

Title: Notes List

Size: Custom | Document Number: LA-K453P | Rev: 0.1

Date: Friday, February 05, 2021 | Sheet 3 of 121

Main Func = CPU



APU PN Table

UC1

Cezanne R7
R7PC@
SA0000E1P3L

UC1

Cezanne R9
R9PR@
SA0000E1N3L

Security Classification	Compal Secret Data		
Issued Date	2019/08/26	Deciphered Date	2020/08/26

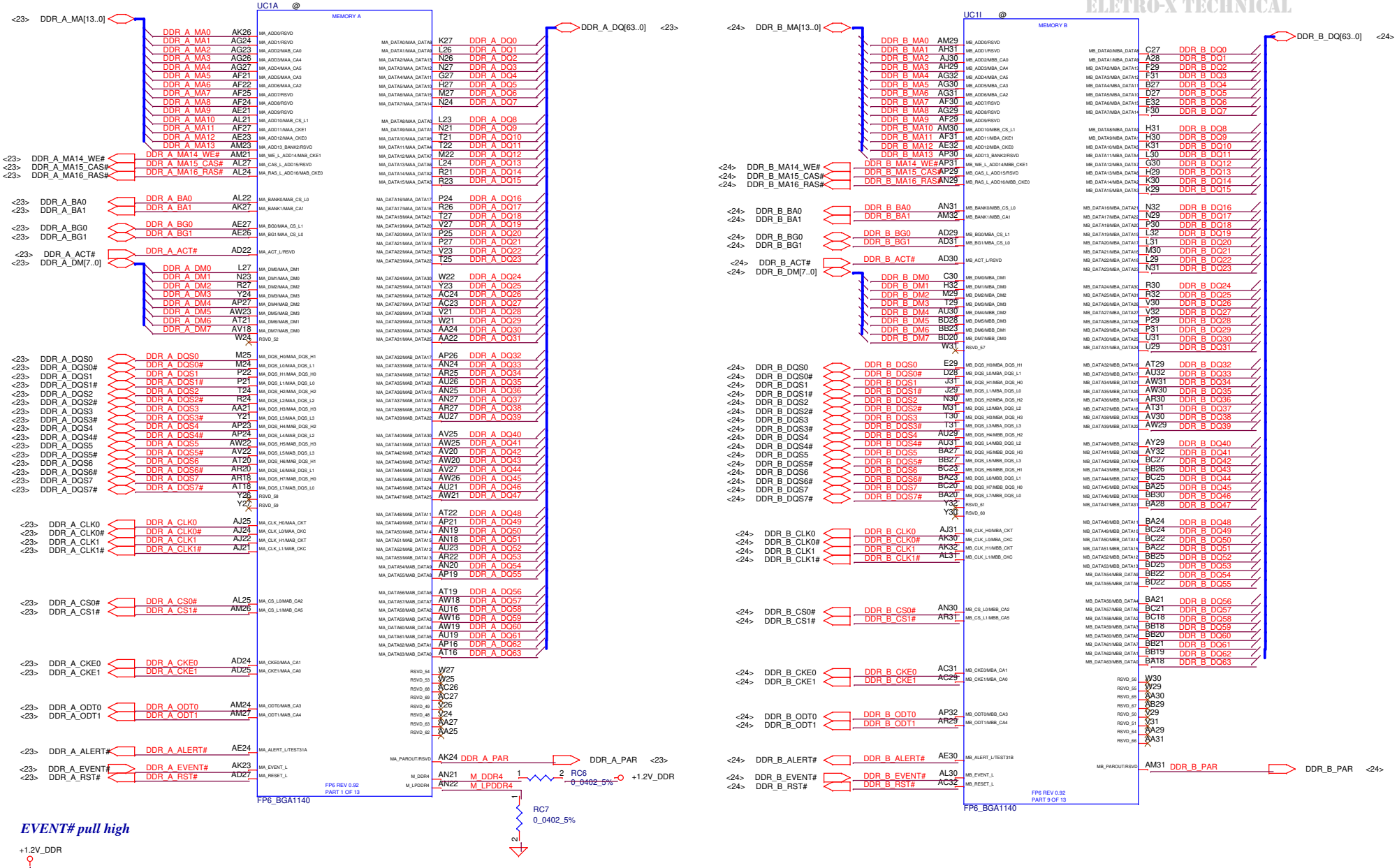
Compal Electronics, Inc.

Title: FP6_(1/7)_PEG/PCIE/SATA

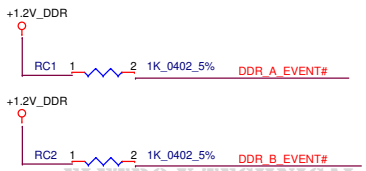
Size: Document Number: LA-K453P Rev: 1.0

Date: Friday, February 05, 2021 Sheet 6 of 121

Main Func = CPU



EVENT# pull high



Security Classification	Compal Secret Data		
Issued Date	2019/04/30	Deciphered Date	2020/04/30

Compal Electronics, Inc.

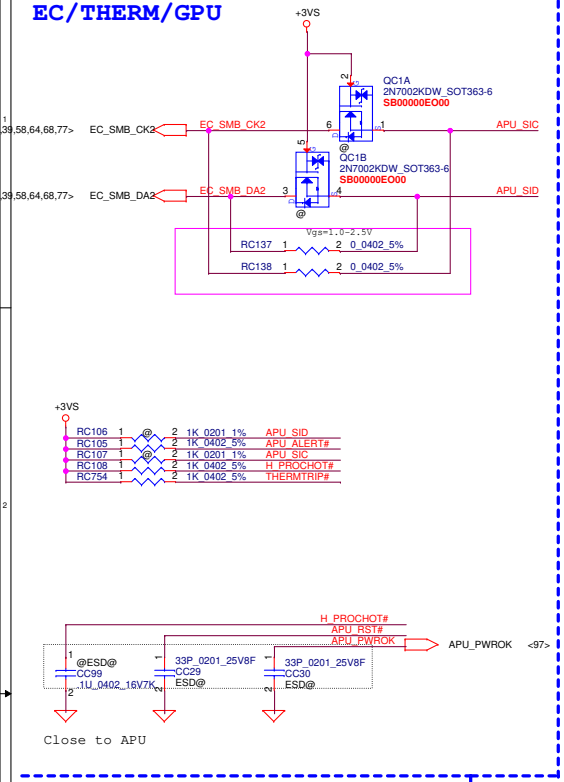
Title: FP6_(2/7)_DDR4

Size: B | Document Number: LA-K453P | Rev: 1.0

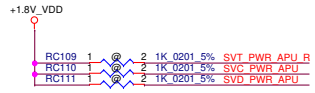
Date: Friday, February 05, 2021 | Sheet 7 of 121

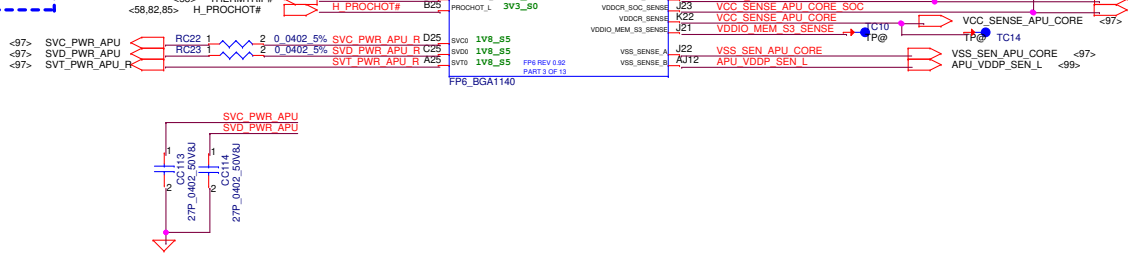
Main Func = CPU

EC/THERM/GPU

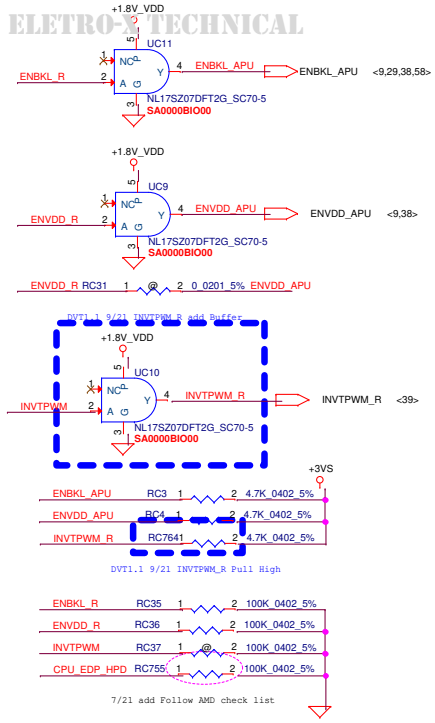


SVID

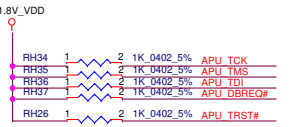


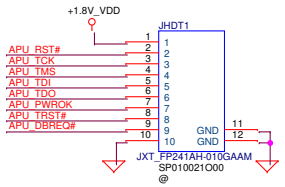


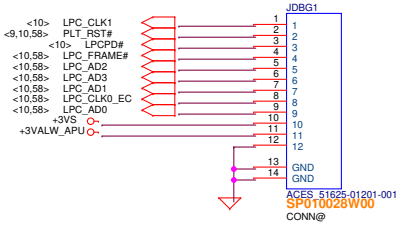
DISP



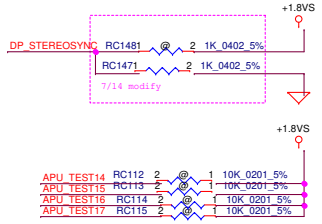
AMD DEBUG





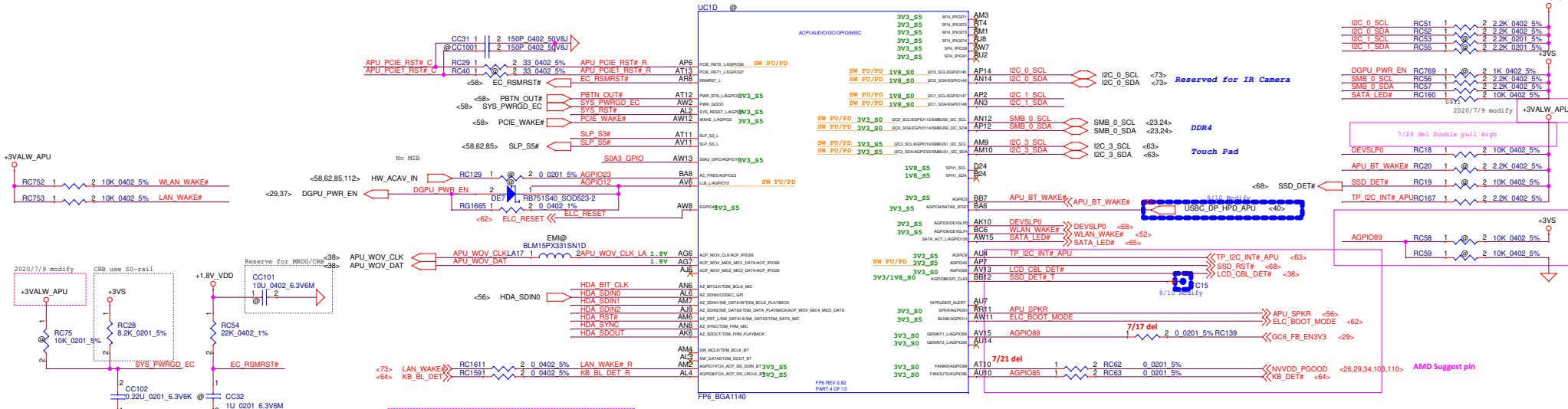


TESTPOINT

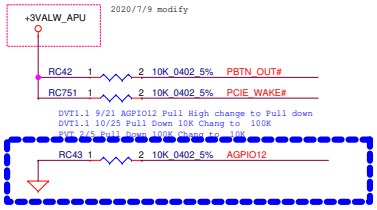


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2019/08/26	Deciphered Date 2020/08/26	Title: FP6_(3/7)_DISP/MISC/HDT
			Document Number: LA-K453P Rev: 1.0
			Date: Friday, February 05, 2021 Sheet 8 of 121

Main Func = CPU



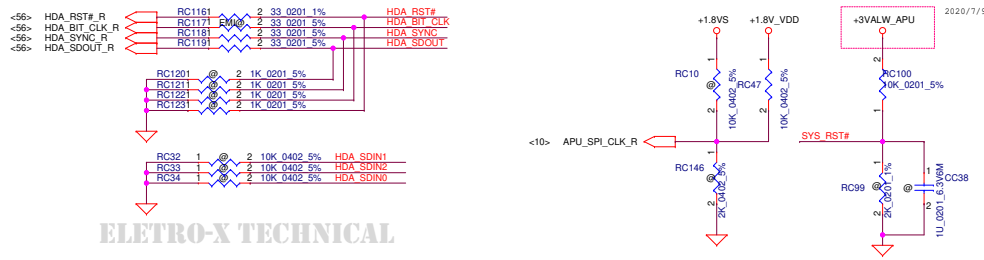
ACPI

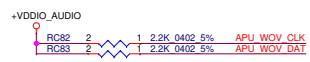


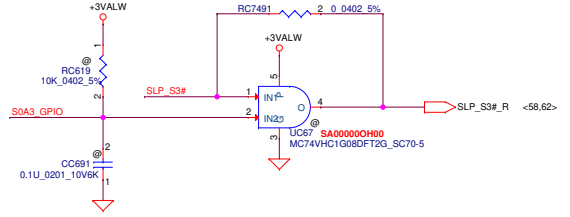
Strap Pin

	APU_SPI_CLK_R	SYS_RST#
H	USE 48MHZ CRYSTAL CLOCK (Default)	NORMAL RESET MODE (Default)
L	USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK	SHORT RESET MODE

HDA



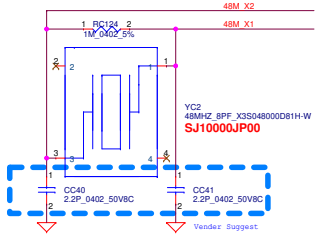




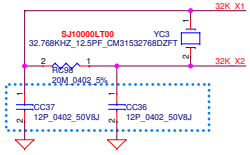
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2019/08/26	Deciphered Date	2020/08/26
Title	FP6_(4/7)_GPIO/HDA/STRAP		
Document Number	LA-K453P		Rev 1.0
Date:	Friday, February 05, 2021	Sheet	9 of 121

Main Func = CPU

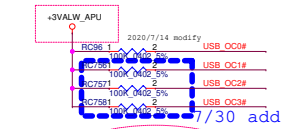
48MHz CRYSTAL



32.768KHz CRYSTAL

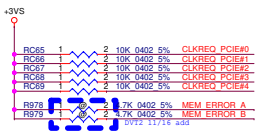


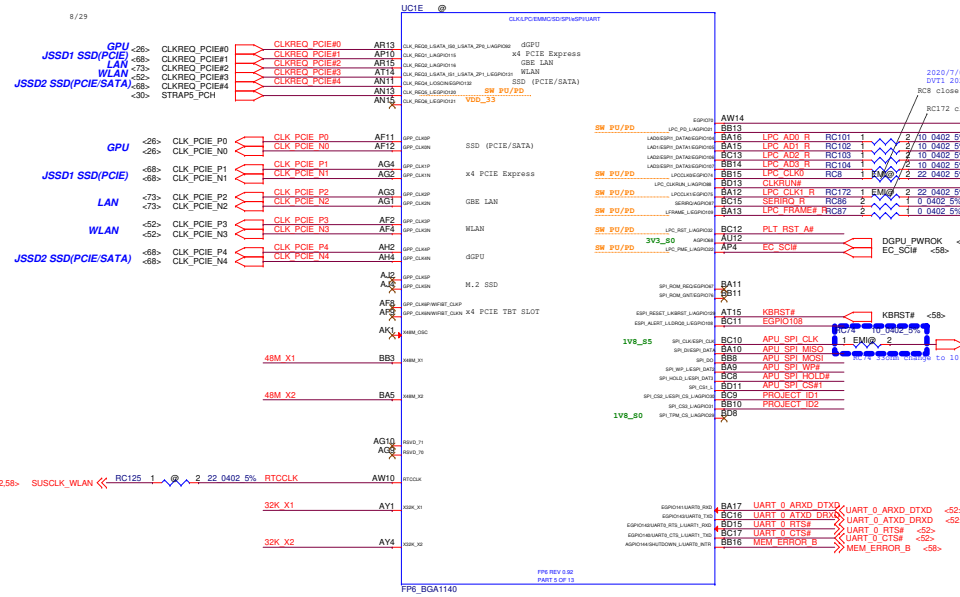
USB Function

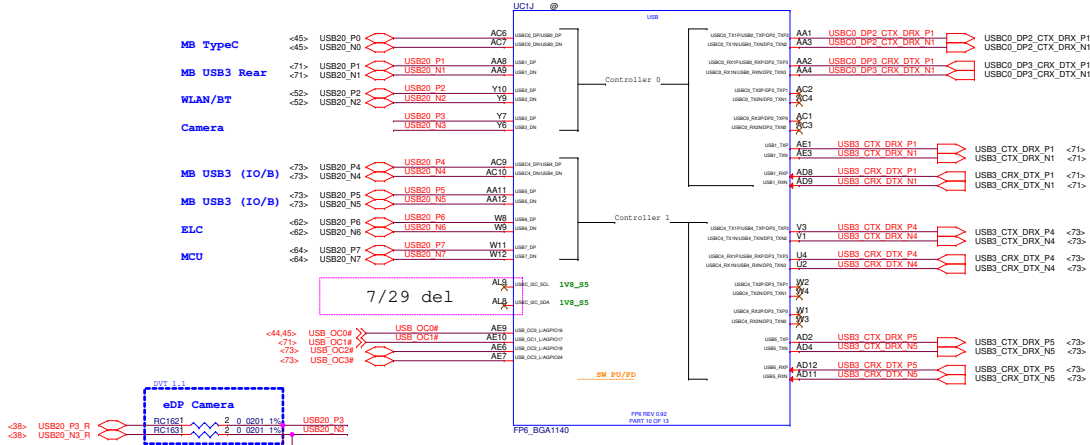


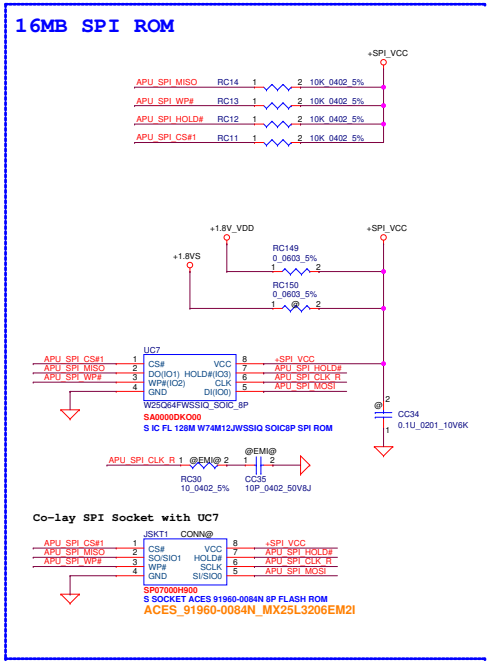
7/17 DEL

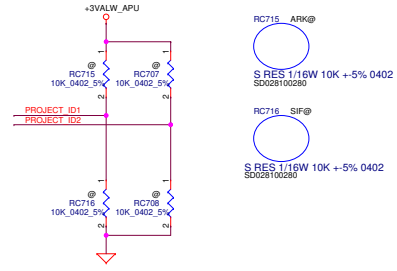
ELETRO-X TECHNICAL











Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2019/08/26	Deciphered Date 2020/08/26	Title FP6_(5/7)_CLK/USB/SPI/LPC
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			Date: Saturday, February 20, 2021 Sheet 10 of 121

Main Func = CPU

+APU_CORE_SOC Cap
place at Power Side

SCL/MBDG:
7*22uF (BU)
1*1uF (BU)
1*180pF (BU)

SCL/MBDG:
7*22uF (BU)
2*1uF (BU)
4*0.22uF
1*180pF (BU)
2*180pF

SM01000JX00
3000ma 33ohm@100mhz DCR 0.04

+1.2V_DDR
TAI-TECH HCB1608KF-330T30
LC1
+1.8VS
LC3
+APU_VPH

All BU(on bottom side under SOC)**ACROSS VDDIO AND VSS SPLIT**

+1.8V_VDD
+VDDIO_AUDIO
RC126 0_0402_5%
RC127 0_0402_5%
+VDDIO_AUDIO connect to +1.8V_VDD
No support voice on voice

+3VS
+3VS_APU
RC144 0_0402_5%

+1.8VS
+1.8VALW_APU
RC89 0_0603_5%
+3VALW_APU

control by P.66

+0.75VS
+0.75VALW

SCL/MBDG:
2*22uF (BO)
8*1uF (BOx4+BUx4)
1*180pF (BU)

SCL/MBDG:
1*22uF (BO)
3*1uF (BOx1+BUx2)

+VDDCR_VDD
+VDDCR_SOC
CC115 180P_0402_50V8J
CC116 180P_0402_50V8J
CC117 1U_0402_6.3V7K

UC1F @
POWER
FP6_BGA1140
FP6 REV 0.92
PART 6 OF 13

+VDDCR_SOC	TDC: 15A EDC: 20A	N16 N18 N20 P17 P19 R18 R20 T19 U18 U20 V19 W18 W20 Y19
+1.2V_DDR	TDC: 6A	AC20 AC28 AD23 AD26 AD28 AD32 AE20 AE22 AE25 AE28 AF23 AF26 AF28 AF32 AG20 AG22 AG25 AG28 AJ20 AJ23 AJ26 AJ29 AJ32 AK22 AK25 AK28 AL23 AL26 AL29 AL32 AM22 AM25 AM28 AN28 AN32 AP28 AR32
+APU_VPH	TDC: 1A	AC21 AD21
+VDDIO_AUDIO	TDC: 0.2A	AP9
+3VS_APU	TDC: 0.25A	AL18 AM17
+1.8VS	TDC: 2.5A	AL20 AM19
+1.8VALW_APU	TDC: 1A	AL19 AM18
+3VALW_APU	TDC: 0.25A	AL17 AM16
+0.75VALW	TDC: 2A	AL11 AL12 AM12
+0.75VS	TDC: 2A	M15 M16 M18
+RTC_APU_R	TDC: 4.5uA	AJ11
+VDDCR_VDD	TDC: 51A EDC: 90A	G7 G10 G12 G14 H8 H11 H15 K6 K12 K14 L8 M7 M10 N14 P7 P10 P13 P15 R8 R14 R16 T7 T10 T13 T15 T17 U14 U16 V13 V15 V17 W7 W10 W14 W16 Y8 Y13 Y15 Y17 AA7 AA10 AA14 AA16 AA18 AB13 AB15 AB17 AB19 AC14 AC16 AC18 AD7 AD10 AD13 AD15 AD17 AD19 AE8 AE14 AE16 AE18 AF7 AF10 AF13 AF15 AF17 AF19 AG14 AG16 AG18 AH13 AH15 AH17 AH19 AJ7 AJ10 AJ14 AJ16 AJ18 AK13 AK15 AK17 AK19

SCL/MBDG:
16*22uF (BU)
1*180pF (BU)

+APU_CORE Cap place at Power Side

Stitching Cap.

+VDDCR_VDD
CC104 0.01U_0402_16V7K
CC105 0.01U_0402_16V7K
CC106 0.01U_0402_16V7K
CC108 0.01U_0402_16V7K

RTC OF APU

from BAT_LDO

+RTC_APU_R
SCL/MBDG: 1*1uF 1*0.22uF
close to UC1
W=20mils
CC103 0.22U_0402_16V7K
CC50 1U_0201_6.3V6M
CLRP1 SHORT PADS
CC107 0.1U_0201_10V6K
RC73 1K_0402_5%
+RTC_APU
RC79 1 2 0_0402_5%
+RTC_CELL
CC108 680P_0402_50V7K

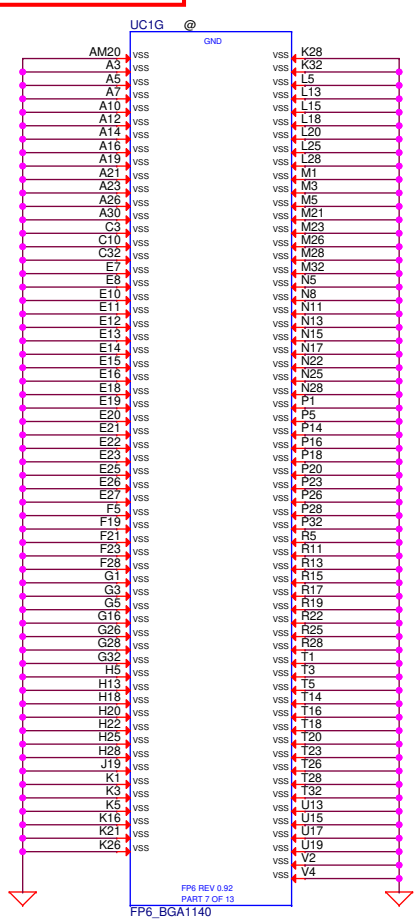
for Clear CMOS

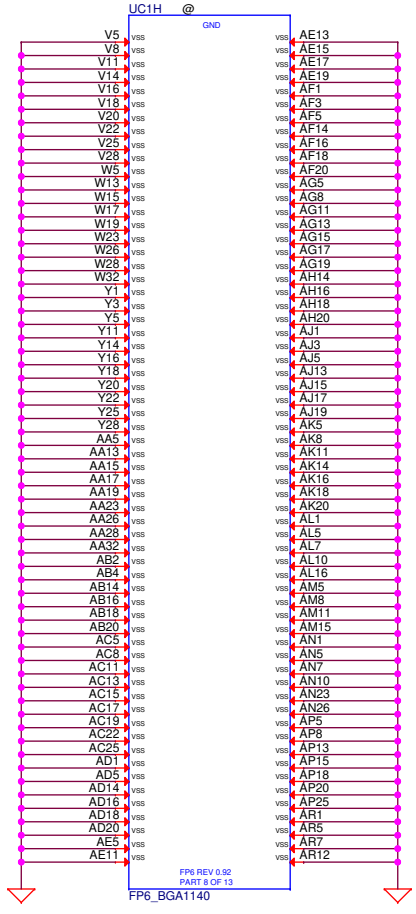
Security Classification	Compal Secret Data		
Issued Date	2019/08/26	Deciphered Date	2020/08/26

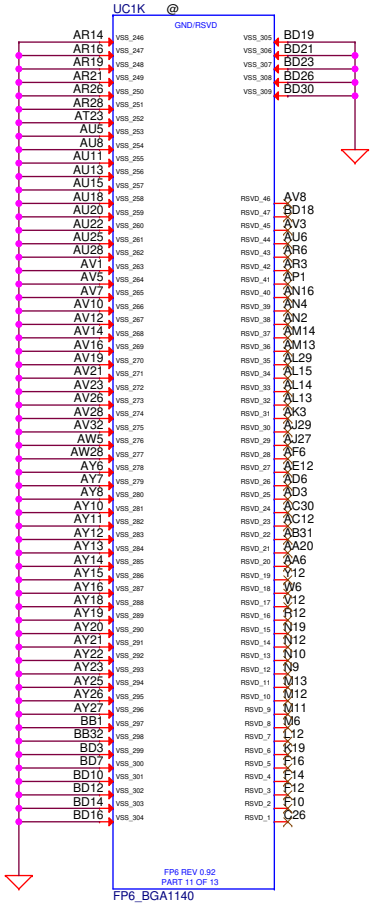
Compal Electronics, Inc.

Title: FP6_(6/7)_PWR
Size: C
Document Number: LA-K453P
Rev: 1.0
Date: Friday, February 05, 2021
Sheet 11 of 121

Main Func = CPU







ELETRO-X TECHNICAL

Project ID

+3VALW_APU

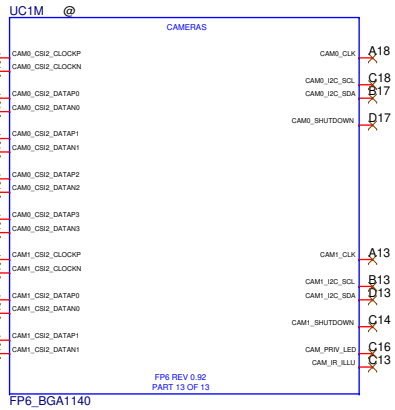
GPUID 100K_0201_5% 2 N20E@ 1 RC169

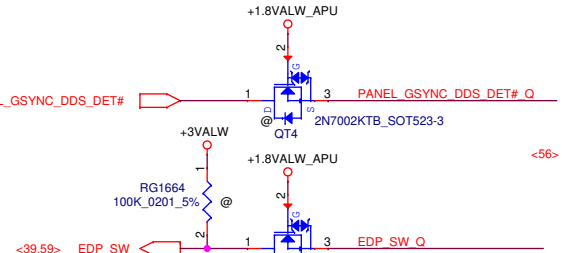
GPUID 100K_0201_5% 1 N20P@ 2 RC171

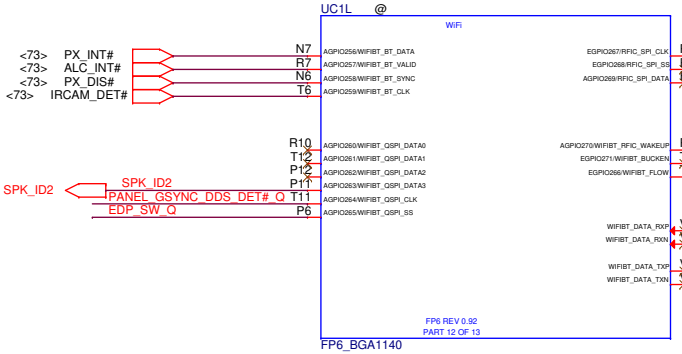
Pin Name	SIF / ARK	
SIF	*LOW*	*SIF*
ARK	*HIGH*	*ARK*

N20E / N20P

GPUID	*NV - GN20P*	*LOW*	*N20P@*
	NV - GN20E	*HIGH*	*N20E@*







+1.8V_VDD

DVT1 9/16 +1.8VALW_APU change to +1.8V_VDD

10K_0201_5% 2 RC763 1 SPK_ID2

ELETRO-X TECHNICAL

Security Classification	Compal Secret Data		
Issued Date	2019/08/26	Deciphered Date	2020/08/26

Compal Electronics, Inc.

Title: FP6_(7/7)_GND/RSVD/CSI

Size: B | Document Number: LA-K453P | Rev: 1.0

Date: Friday, February 05, 2021 | Sheet 12 of 121

Main Func = DDR

Interleaved Memory

ELETRO-X TECHNICAL

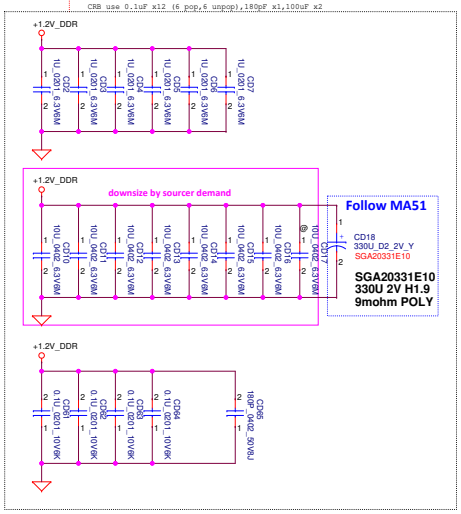
REVERSE TYPE (4 mm)

Layout Note:
Place near JDIMM1

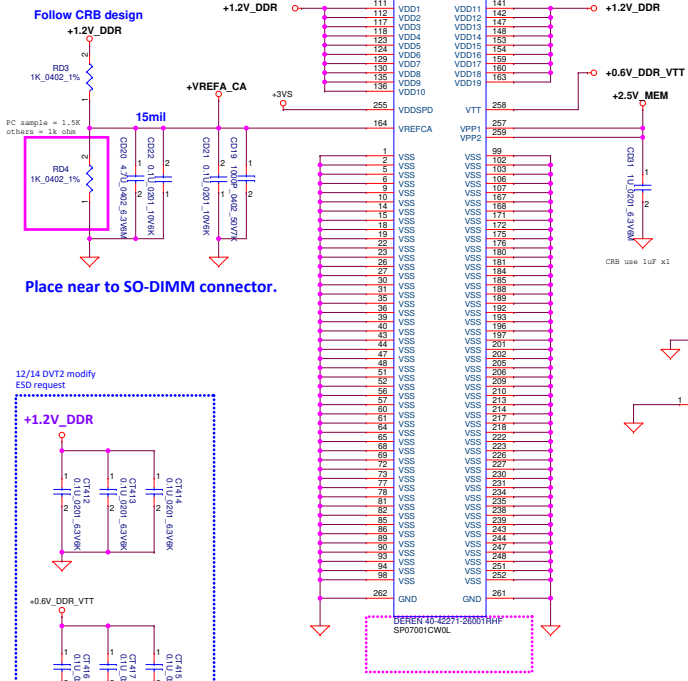
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

DDR4 support Even Parity check in DRAMs.

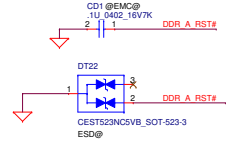
CRB use 0.1uF x12 (6 pop,6 unpop),180pF x1,100uF x2

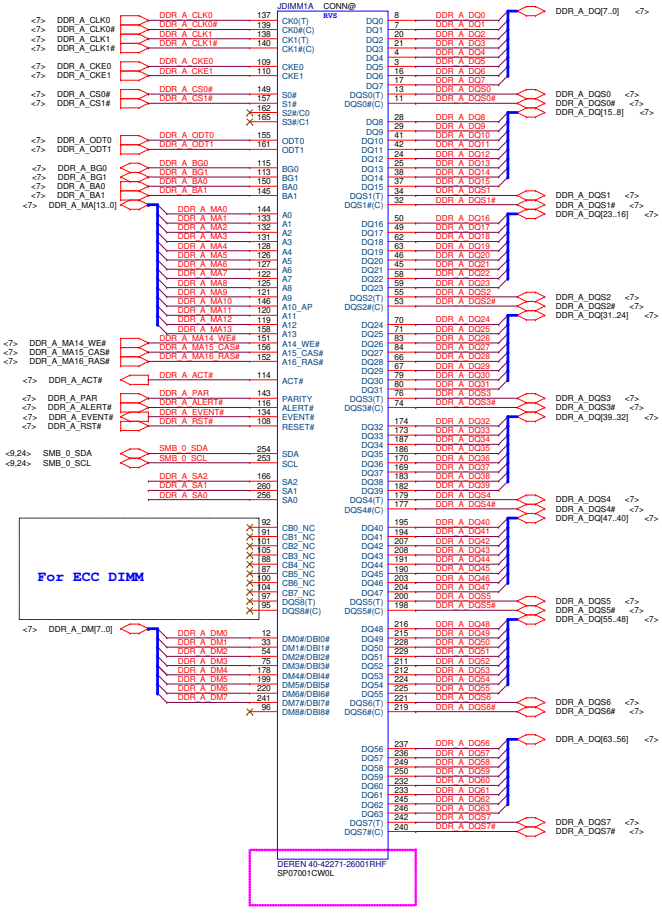


Follow CRB design

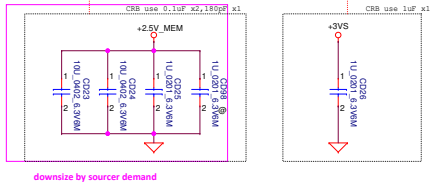


Part Number: SP07001CW0L
Part Value: S SOCKET DEREN 40-42271-26001RHF DDR A31





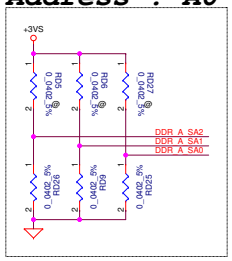
Layout Note:
Place near JDIMM1.257,259



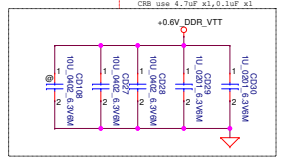
Layout Note:
Place near JDIMM1.255

12/14 DVT2 modify
ESD request

Address : A0



Layout Note:
Place near JDIMM1.258



ELETRO-X TECHNICAL

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2017/01/06	Title DDR4 DIMMA_RVS
			Size Document Number LA-K453P Rev 0.1
			Date: Friday, February 05, 2021 Sheet 23 of 121

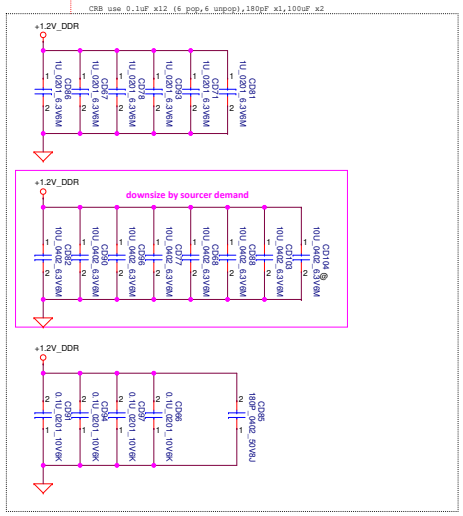
Main Func = DDR

Layout Note:
Place near JDIMM2

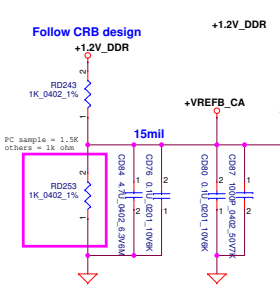
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

Interleaved Memory

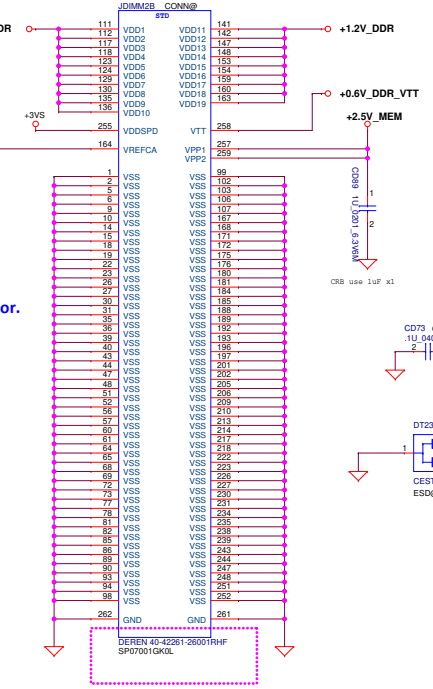
STD (4 mm)



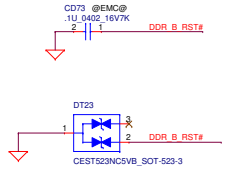
Follow CRB design

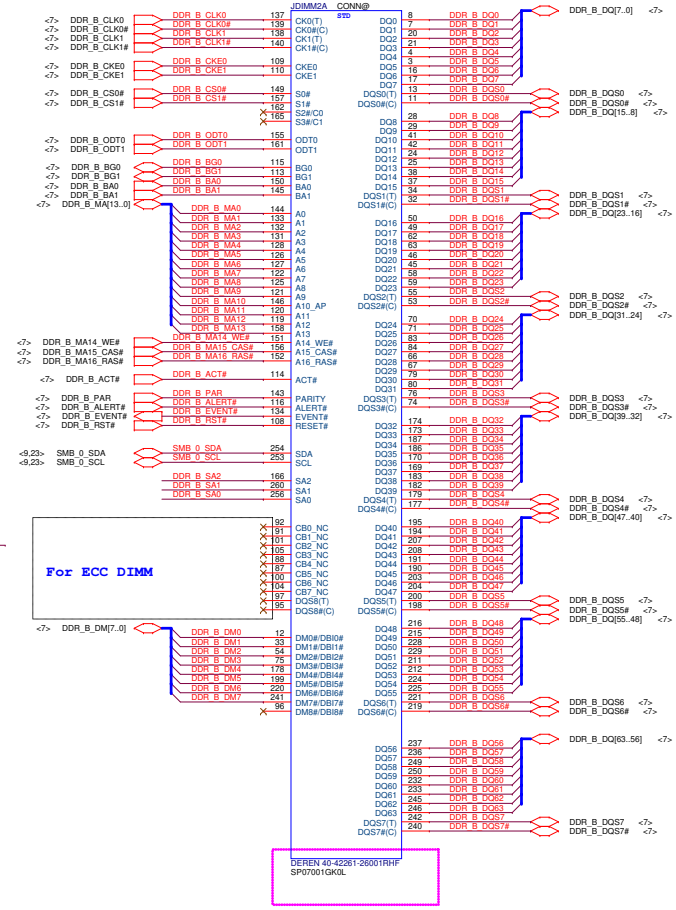


Place near to SO-DIMM connector.

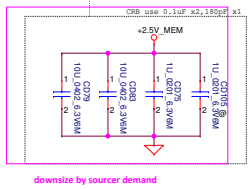


Part Number: SP07001GK0L
Part Value: S SOCKET DEREN 40-42261-26001RHF A31

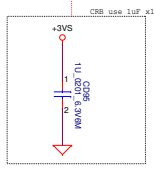




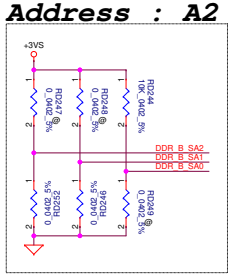
Layout Note:
Place near JDIMM2.257,259



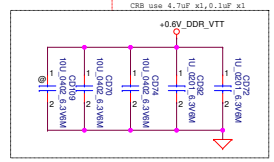
Layout Note:
Place near JDIMM2.255



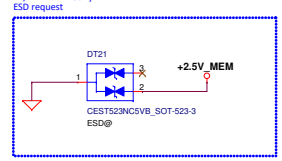
Address : A2



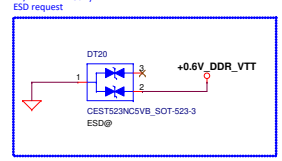
Layout Note:
Place near JDIMM2.258



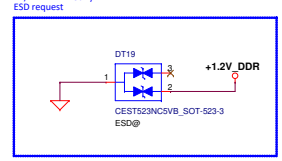
12/14 DVT2 modify
ESD request



12/14 DVT2 modify
ESD request

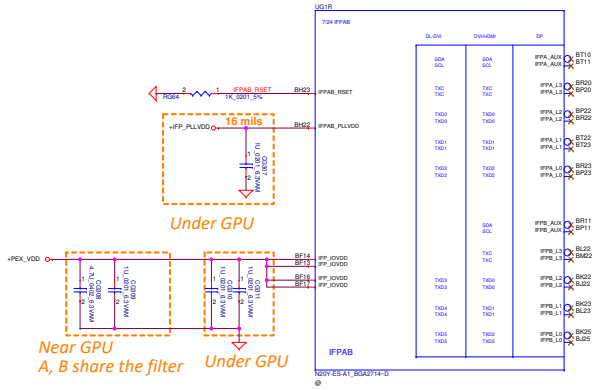


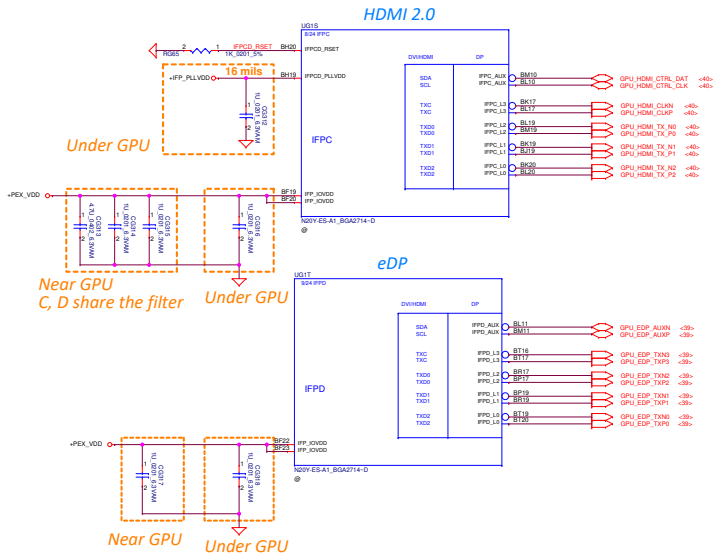
12/14 DVT2 modify
ESD request

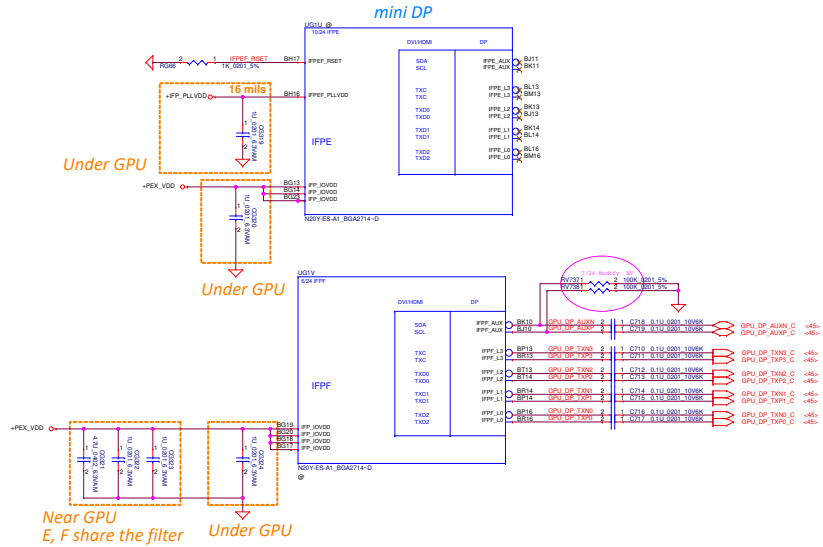


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2017/01/06	Title: DDR4 DIMMB_STD
Size	Document Number: LA-K453P		Rev: 0.1
Date: Friday, February 05, 2021	Sheet 24 of 121		

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/08/07	Deciphered Date 2019/08/07	Title: NV(1/8) PCI EXPRESS
Document Number	LA-K453P		Rev 0.1
Date: Friday, February 05, 2021	Sheet 25 of 121		







Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/08/07	Deciphered Date 2019/08/07	Title: NV(2/8) IFP ABCDEF
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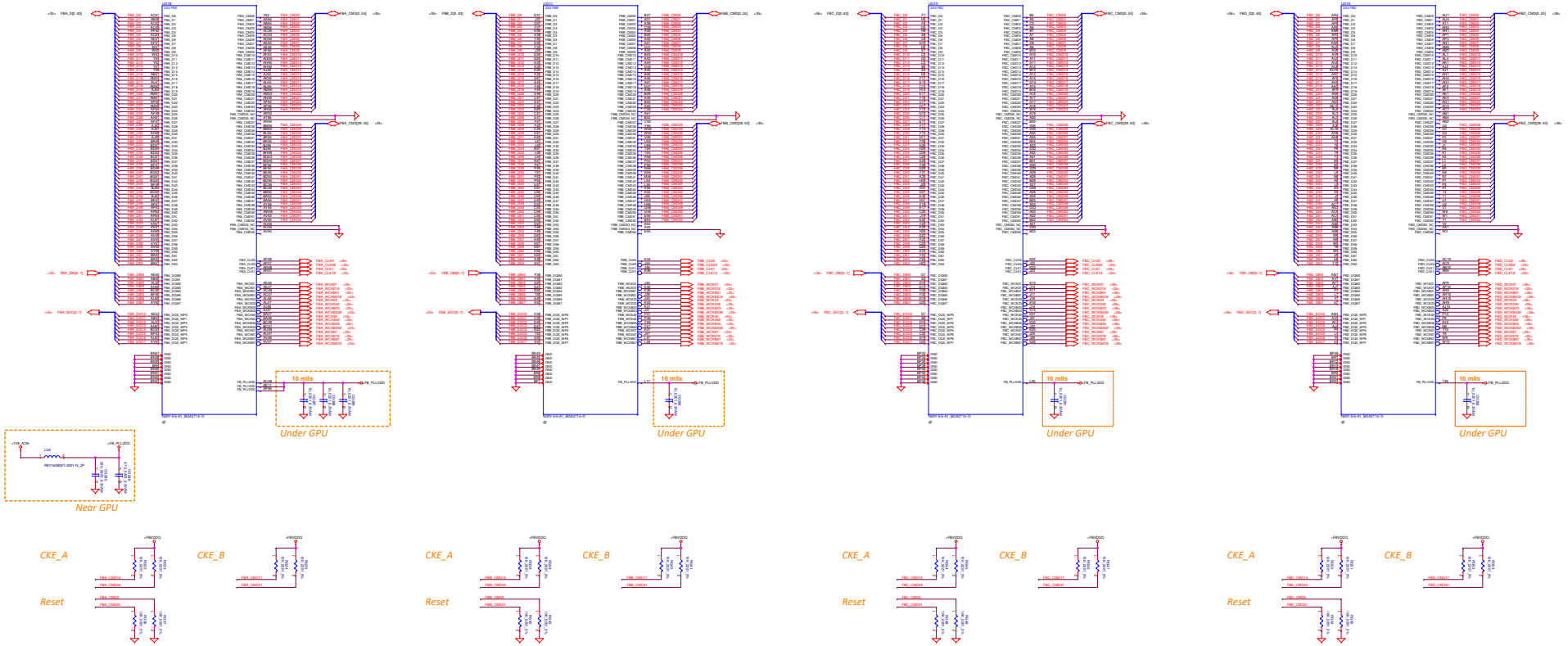
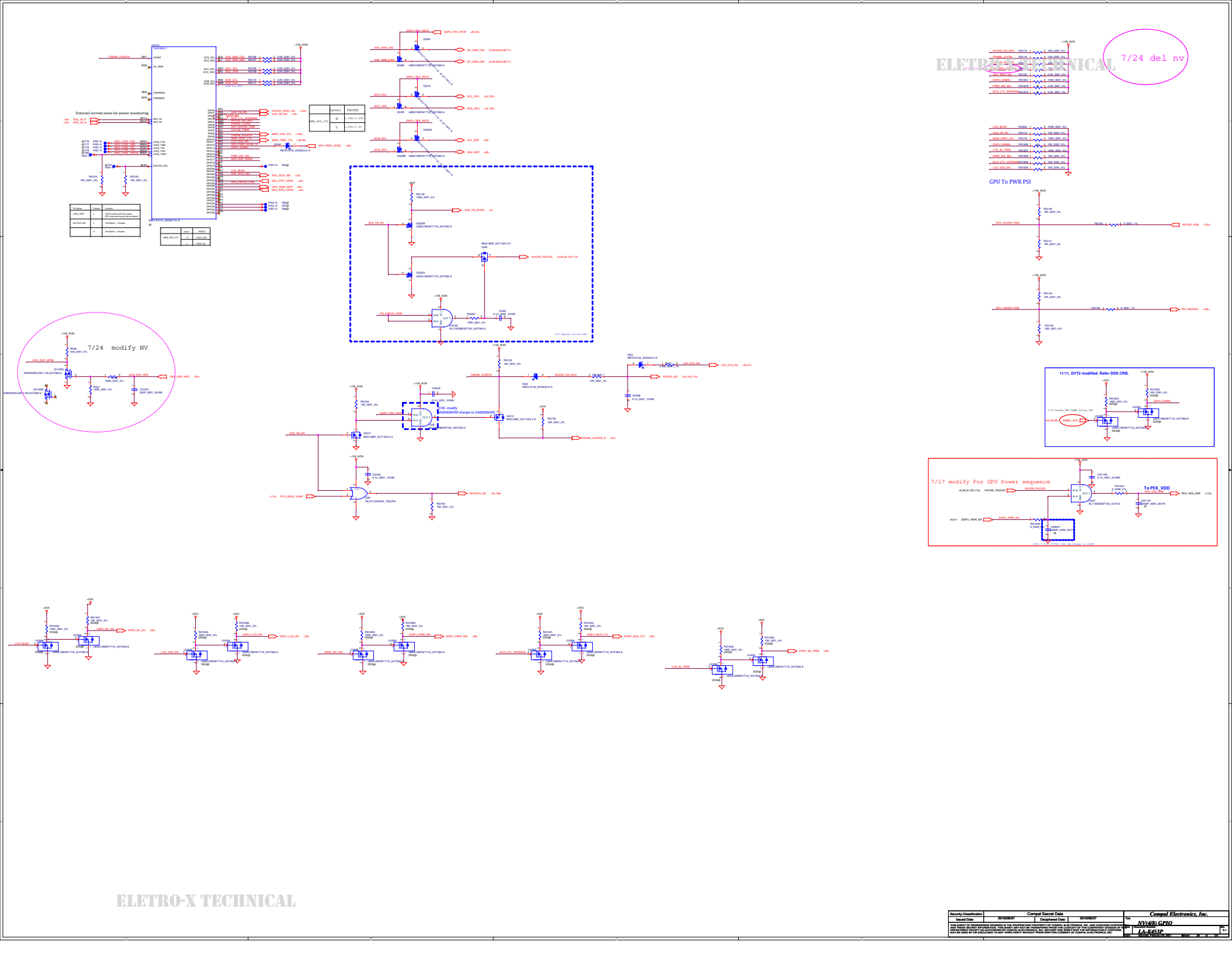
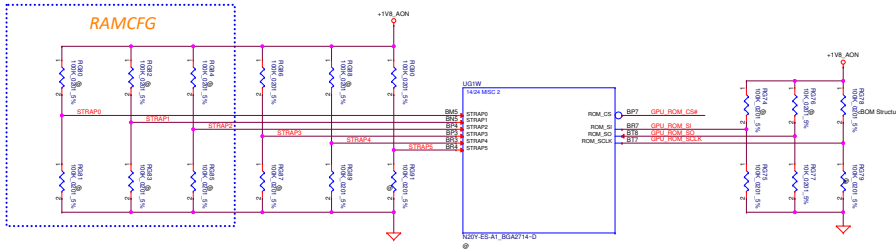
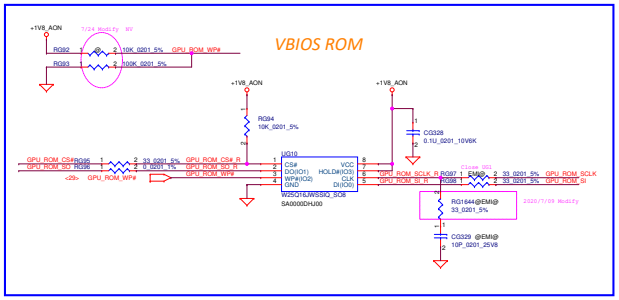
			Date: Friday, February 05, 2021 Sheet 27 of 121



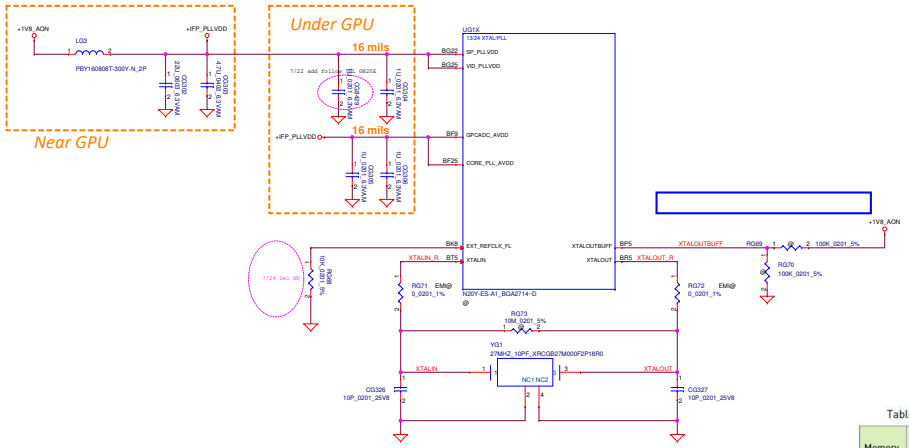
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/08/07	Deciphered Date	2016/08/07	Title
			NV(3/8) MEMORY_FB_ABCD
			Document Number Rev 0.1
			LA-K453P
			Date: Thursday, May 11, 2017 Sheet 39 of 53

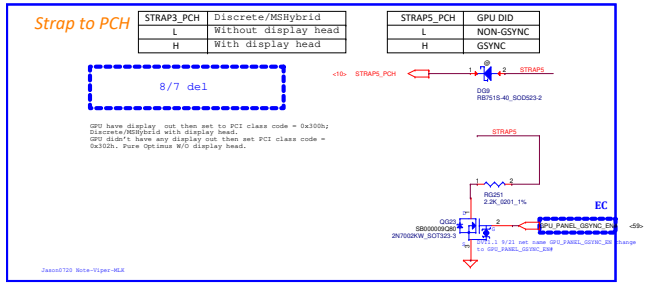

7/24 del nv
GPU To PWR PSI
7/24 modify NV
11/11, DVT2 modified. Refer DDS CRB.
7/17 modify For GPU Power sequence
To PEX_VDD
ELETRO-X TECHNICAL





Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)





STRAP3_PCH	Discrete/MSHybrid
L	Without display head
H	With display head

STRAP5_PCH	GPU DID
L	NON-GSYNC
H	GSYNC

GPU have display out then set to PCI class code = 0x300h; Discrete/MSHybrid with display head.
GPU didn't have any display out then set PCI class code = 0x302h. Pure Optimus W/O display head.

Table 9.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Table 2. GN20-E5/E4 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2021[3]	Full	Production candidate
			Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate
			Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940[3]	Full	Production candidate

Notes:
[1] Refer to GN20-E GeForce Product Spec for memory voltages and clocks.
[2] Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Samsung memory is identified by "SFL" letters inserted before the seven digits in its lot ID.
[3] Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Micron memory will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
For GN20-E5/E4, the maximum allowable memory case temperature is 95 °C.

Table 3. GN20-E3 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2021[3]	Full	Production candidate
			Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate
			Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940[3]	Full	Production candidate

Notes:
[1] Refer to GN20-E GeForce Product Spec for memory voltages and clocks.
[2] Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Samsung memory is identified by "SFL" letters inserted before the seven digits in its lot ID.
[3] Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Micron memory will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
For GN20-E3, the maximum allowable memory case temperature is 95 °C.

Table 1. GN20-E7 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
16 Gb	2Chx512Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4ZAF325BM-HC14	M-die	0x9	14 Gbps	2020[3]	Full	Production candidate
			Micron	TBD	TBD	0xA	14 Gbps	N/A	Full	Production candidate
			Hynix	TBD	TBD	0xB	14 Gbps	N/A	Full	Production candidate
8 Gb	2Chx256Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001[3]	Full	Production candidate
			Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate
			Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940[3]	Full	Production candidate

Notes:
[1] Refer to GN20-E GeForce Product Spec for memory voltages and clocks.
[2] Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Samsung memory is identified by "SFL" letters inserted before the seven digits in its lot ID.
[3] Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Micron memory will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
For GN20-E7, the maximum allowable memory case temperature is 95 °C.

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Issued Date	2020/03/05	Deciphered Date	2021/12/31
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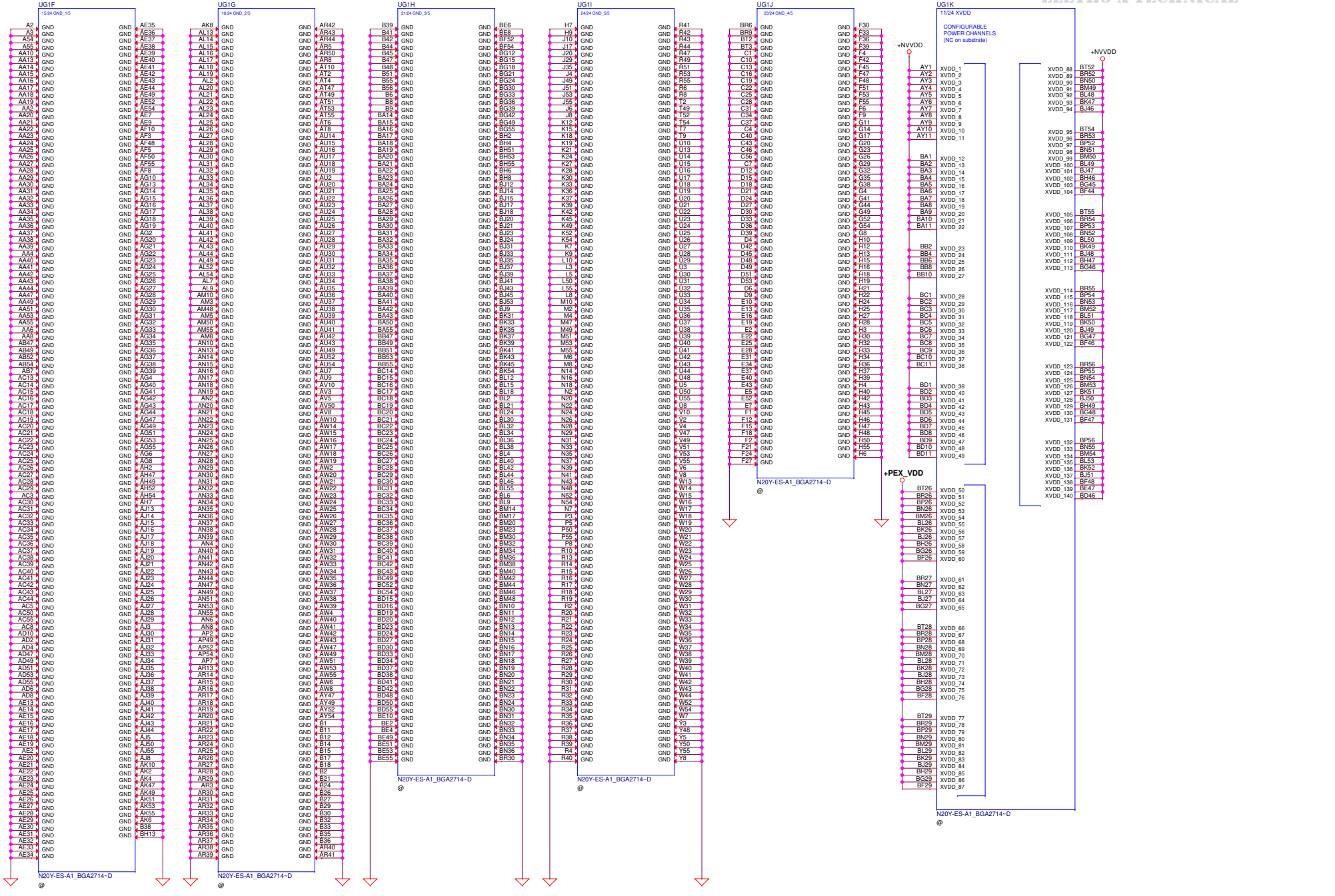
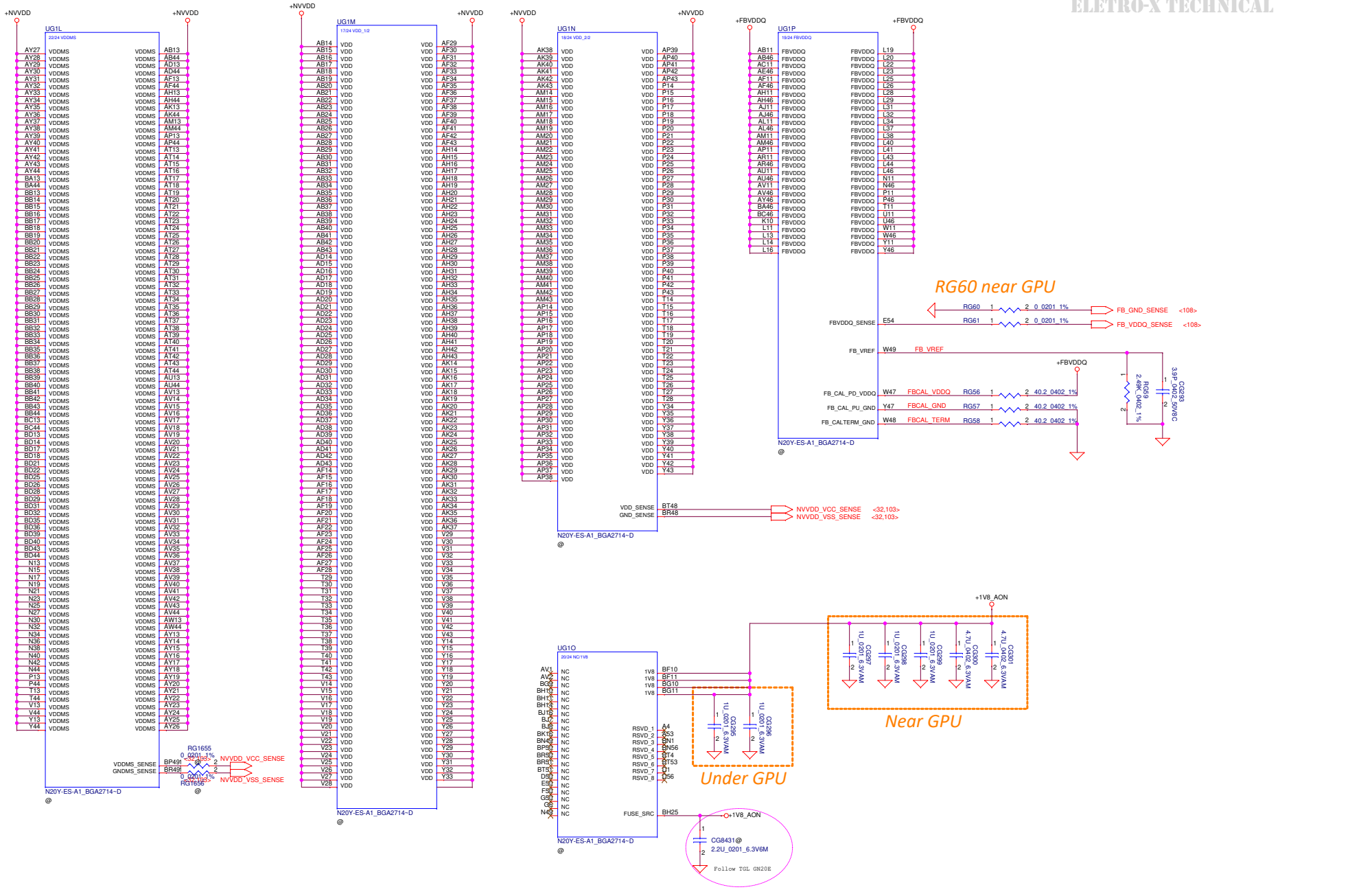


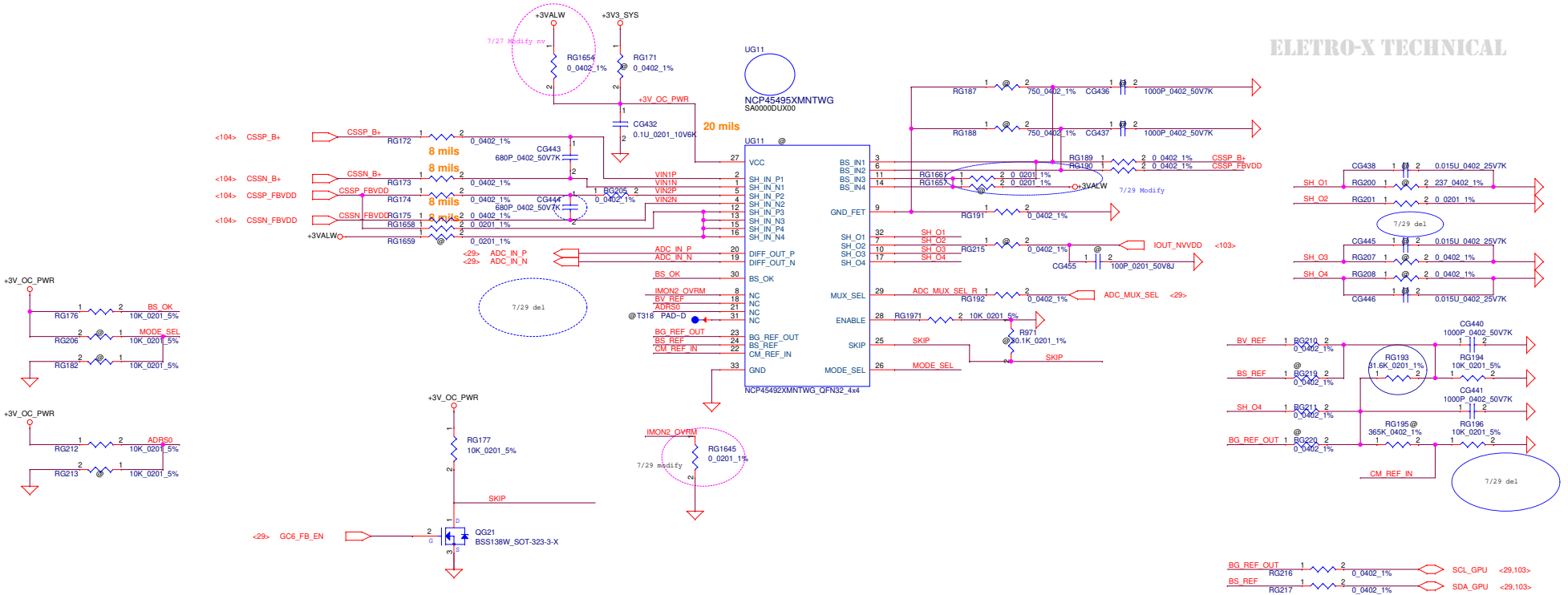
Security Classification	Compal Secret Data		
Issued Date	2018/08/07	Deciphered Date	2019/08/07

Compal Electronics, Inc.	
Title	NV(6/8) GND, RFUs
Size	Document Number: LA-K453P
Rev	0.1
Date: Friday, February 05, 2021	Sheet 31 of 121



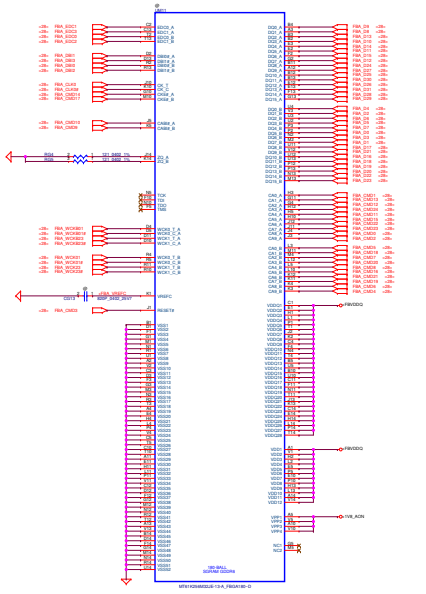
Security Classification	Compal Secret Data		
Issued Date	2018/08/07	Deciphered Date	2019/08/07

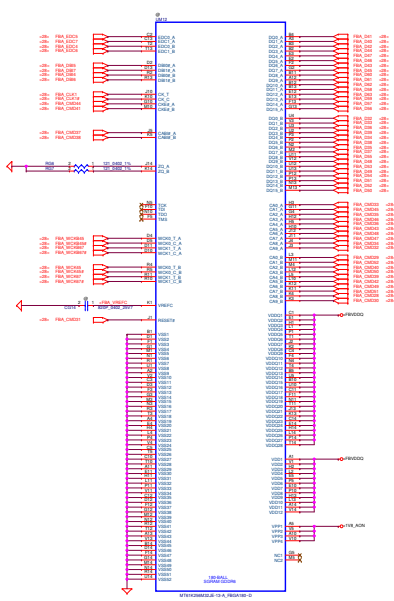
Compal Electronics, Inc.	
Title	NV(7/8) POWERS
Size	Document Number LA-K453P
Rev	0.1
Date: Friday, February 05, 2021	Sheet 32 of 121

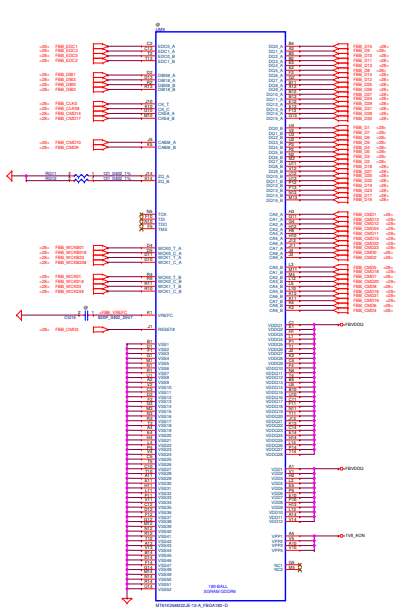


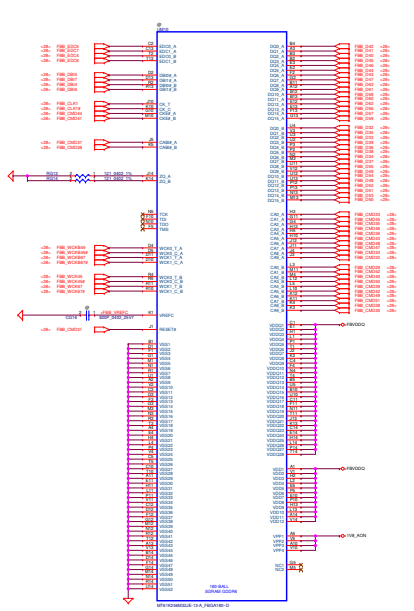
Security Classification	Compal Secret Data		
Issued Date	2018/08/07	Deciphered Date	2019/08/07

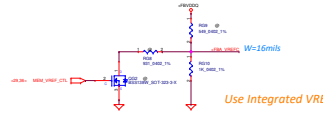
Compal Electronics, Inc.			
Title	OC, Discharging		
Size	Document Number		Rev
	LA-K453P		0.2
Date:	Friday, February 05, 2021	Sheet	34 of 121



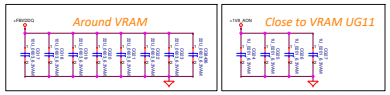


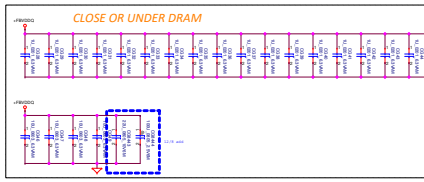




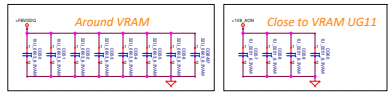


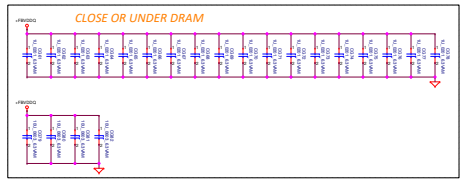
UM11



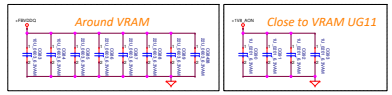


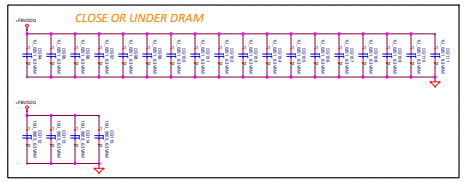
UM12



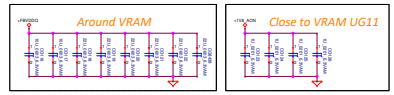


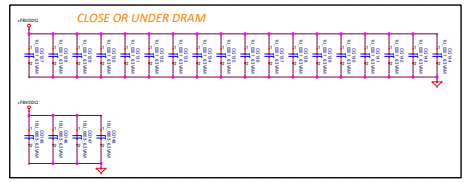
UM9





UM10





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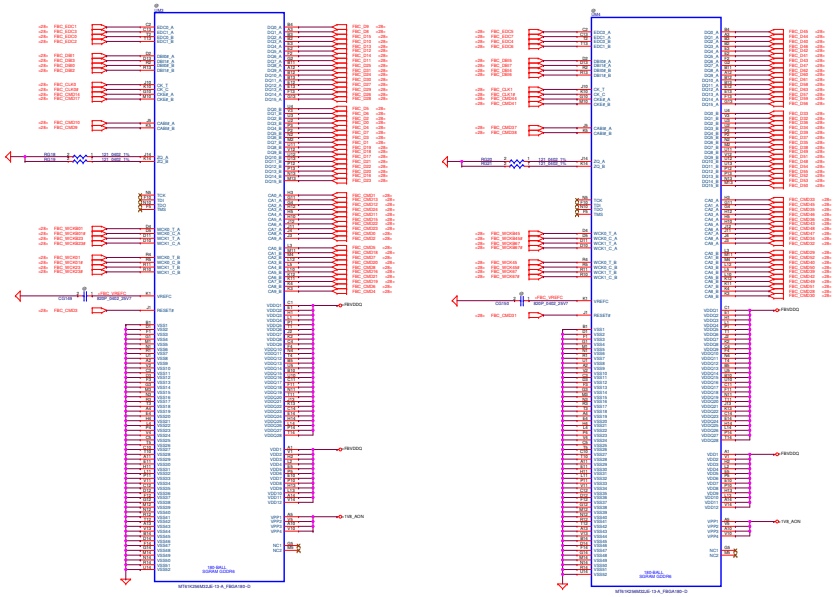
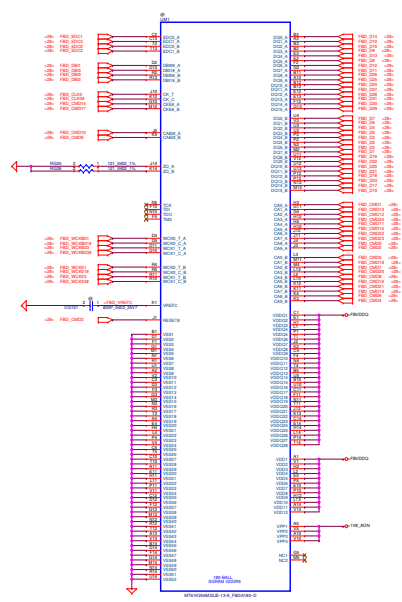
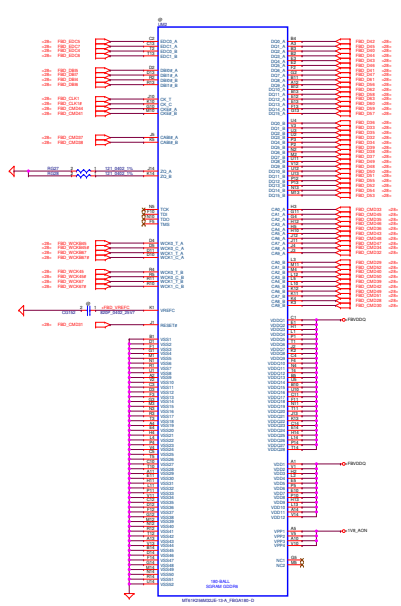
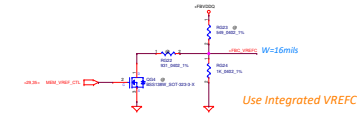
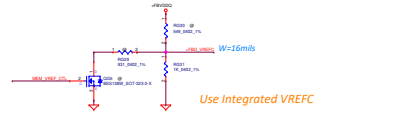
Issued Date	2016/08/07	Deciphered Date	2016/08/07	Title
			VRAM_GDDR5_AB
			Document Number	Rev
			LA-K453P	0.1
			Date: Wednesday, October 19, 2016	Sheet 36 of 50



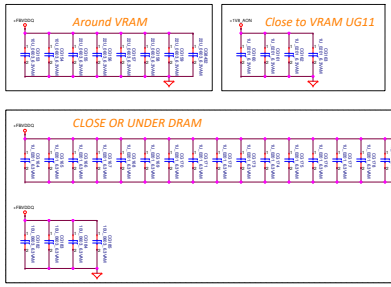




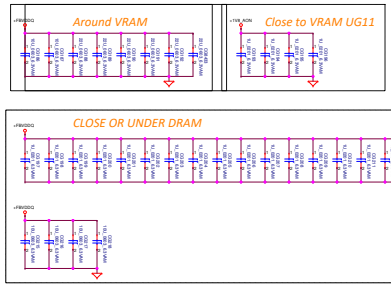




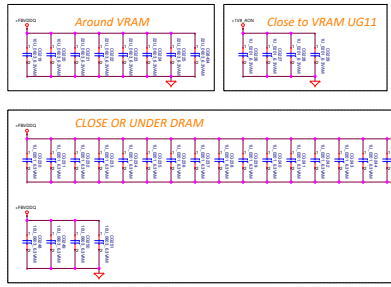
UM3



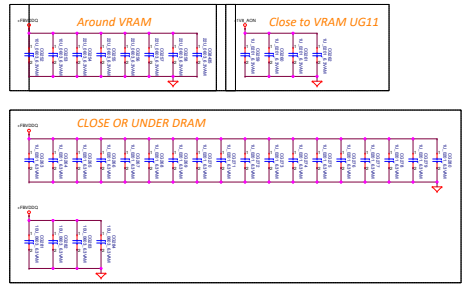
UM4



UM1



UM2



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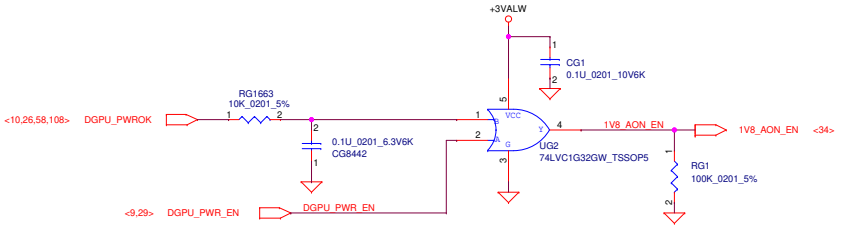
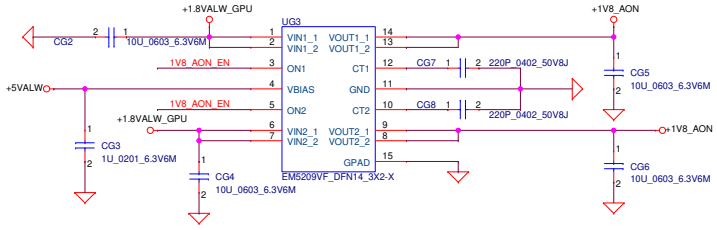
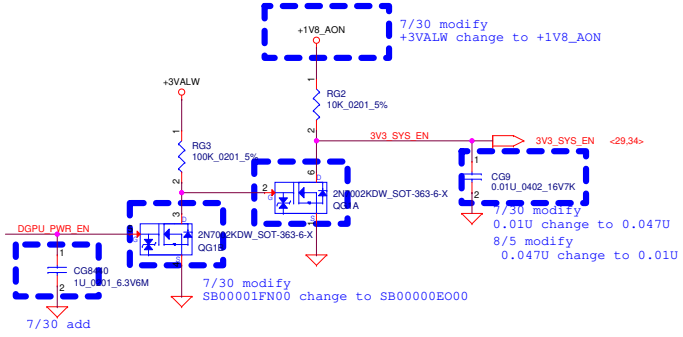
Issued Date	2016/08/07	Deciphered Date	2016/08/07	Title
			VRAM_GDDR6_CD
			Size / Document Number / Rev
			LA-K452P / 0.1
			Date: Thursday, July 28, 2022 / Sheet 36 of 50

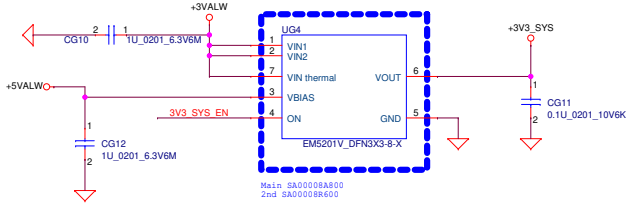
+1V8_AON / +1V8_MAIN(PLL)







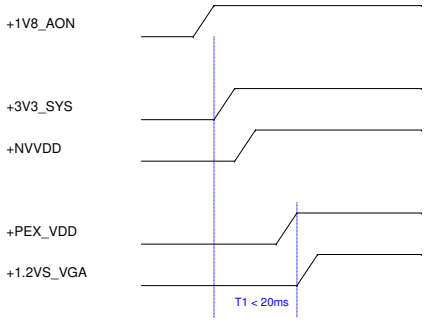
NV_3V3(For Sequence)



FUSE_SRC

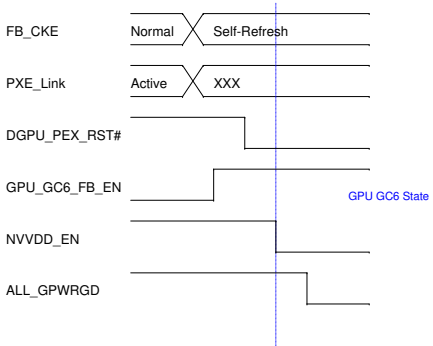
Follow TGL GN20E

GPU Power Up Sequence



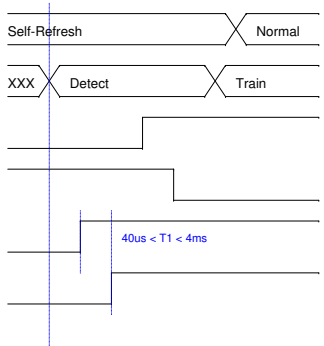
The ramp time for any rail must be more than 40us and less than 2ms.

GPU GC6 Entry Sequence

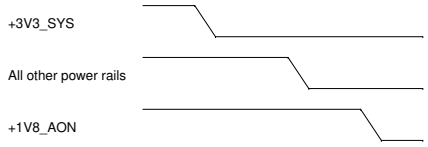


The entire entry/exit sequence must complete within 200 ms.

GPU GC6 Exit Sequence



GPU Power Down Sequence



Security Classification	Compal Secret Data		
Issued Date	2018/08/07	Deciphered Date	2019/08/07

Compal Electronics, Inc.

Title: DGPU_DC/DC Interface

Size: B | Document Number: LA-K453P | Rev: 0.1

Date: Friday, February 05, 2021 | Sheet 37 of 121

Main Func = LCD

Brightness_EN

APU <9,29,58> ENBKL_APU
GPU <29> DGPU_BL_EN
R957 1 DDS@ 2 0 0201 1%
DV5 BAT54C_SOT23-3-D
DDS_BL_EN
DDS
R951 1 DDS@ 2 100K_0201_5%

+19VB
FV1 3A_32V_F0603FA3000V032T-X
+DCBAT_LCD

<39> SW_EDP_TXP0 / SW_EDP_TXN0 0.22U_0201_6.3V6K
<39> SW_EDP_TXP1 / SW_EDP_TXN1 0.22U_0201_6.3V6K
<39> SW_EDP_TXP2 / SW_EDP_TXN2 0.22U_0201_6.3V6K
<39> SW_EDP_TXP3 / SW_EDP_TXN3 0.22U_0201_6.3V6K
<39> SW_EDP_AUXP / SW_EDP_AUXN
CV1 SW_EDP_TXP0_C / CV2 SW_EDP_TXN0_C
CV3 SW_EDP_TXP1_C / CV4 SW_EDP_TXN1_C
CV5 SW_EDP_TXP2_C / CV6 SW_EDP_TXN2_C
CV7 SW_EDP_TXP3_C / CV8 SW_EDP_TXN3_C
SW_EDP_AUXP / SW_EDP_AUXN
JEDP1 CONN@

USB20_N3_EDP / USB20_P3_EDP

<39> EDP_HPD → ENBKL
<39> EDP_PWM → EDP_PWM
LCD_TST_C
DMIC_DATA_EDP / DMIC_CLK_EDP

EC-DDS
EC-BKOFF
+3VALW
<59> DDS_PANEL_BKEN_EC
DDS_BL_EN
ENBKL_D
UG57 NL17SZ08DFT2G_SC70-5 DDS@

+LCDVDD
RV41 1 @ 2 10K_0201_5%
<12> OD_EN_R
R144 2 1 0_0402_5%
OD_EN
<9> LCD_CBL_DET#
8/6 add DE5
RB751S-40_SOD523-2-X
DE5
C726 10P_0201_25V8
OD_EN_D
Pin 30
RSV for NV/non-NV
R6 100K_0201_5%
R7 100K_0201_5%
EDP_PWM
ENBKL
+CAM_VCC
+MIC_VCC
W=60 mils
+LCDVDD
RF@C727 10P_0201_25V8
W=60 mils
+DCBAT_LCD
1.5A
RF@ CV17 10P_0201_25V8

STARC_300E40-1010RA-G3 SP010022J00

EC (BIST MODE)
<58> BKOFF#
DV13 BAT54C_SOT23-3-D
ENBKL_D
ENBKL

<39,58> LCD_TST
LCD_TST R962 1 2 100_0402_1% LCD_TST_C

+5VS
FV4 ARK@ 0.5A_65V_T0603FF0500TM-X
+5VS_ALIEN_LED

+5VS_ALIEN_LED
<63> ALIEN_LED_R_DRV#
<63> ALIEN_LED_G_DRV#
<63> ALIEN_LED_B_DRV#
<12,39,58> DDS_CBL_DET#
<29> SCL_EDP
<29> SDA_EDP
JAW1 SDAN_615005-010041 SP01002S500 CONN@

<10> USB20_P3_R
<10> USB20_N3_R
LV1 EMI@ DLM0NSN900HY2D_4P-X
USB20_P3_EDP
USB20_N3_EDP
DV2 AZC199-02S.R7G_SOT23-3-X ESD@

+LCDVDD
RV730 27_0402_1%
+5VALW
RV731 10K_0402_5%
QV10A DMN66D0LDW-7_SOT363-6
QV10B DMN66D0LDW-7_SOT363-6
ENVDD

OD_EN_D_R RV732 0_0201_1% OD_EN_D
0112 : Add EV41 reserve for debug
<39> DDS_EDP_SW
DDS_EDP_SW2
2N7002KW_SOT323-3 QV103
0114 : Reserve for G-sync control

2020/07/17 modify,
for LCDVDD discharge follow TGL

+LCDVDD
RV717 1 2 2.2K_0201_5% SCL_EDP
RV716 1 2 2.2K_0201_5% SDA_EDP

Main Func = DMIC

From ARK module (JIO2)
<53> DMIC_DATA_R
<53> DMIC_CLK_R
R446 2 0_0201_1%
R448 2 0_0201_1%
DMIC_DATA
DMIC_CLK
R120 1 2 0_0201_1% APU_WOV_DAT_L
R121 1 2 0_0201_1% APU_WOV_CLK_L
RA31 1 2 0_0201_1% DMIC_DATA_CODEC <56>
RA32 1 2 0_0201_1% DMIC_CLK_CODEC <56>
To PCH
To Codec

From SIF module (eDP)
DMIC_DATA_EDP
DMIC_CLK_EDP
RA41 1 2 0_0201_1% DMIC_DATA
RA42 1 2 0_0201_1% DMIC_CLK
DV1 ESD@ AZ5125-02S.R7G_SOT23-3-X

+3VS_CAM
+MIC_VCC
FV3 @ 0.5A_65V_T0603F0500TM-X
+3VALW_APU
RC84 2 1 2.2K_0402_5% APU_WOV_CLK_L
RC85 2 1 2.2K_0402_5% APU_WOV_DAT_L
+3VALW
Q2 AO3419L_SOT23-3
+3VS_CAM
+CAM_VCC
FV2 0.5A_65V_T0603F0500TM-X
C1 4.7U_0402_6.3V6M
C2 0.01U_0201_6.3V6K
C3 @ 10U_0402_6.3V6M
+3VALW
R8 @ 100K_0201_5%
R9 10K_0201_5%
SUSP# Change to PCH_PWR_EN for Modern Standy
<58,90,99,100> 0.75_1.8VALW_PWREN
R10 1 2 0_0201_1%
Q1 AO3416L_SOT-23-3-X
R132 @ 100K_0201_5%
High Active

LCD_EN

PCH <8,9> ENVDD_APU
GPU <29> DGPU_LCD_EN
R958 1 DDS@ 2 0_0201_1%
DV14 BAT54C_SOT23-3-D
Non-DDS
R963 1 @ 2 100_0402_1% ENVDD_D
DDS
DDS_EN_LCDVCC
R959 1 DDS@ 2 100K_0201_5%
9/12 2014 ECR change to 100K

EC-DDS
Panel RST
EC <59> EC_EDP_RESET
+3VALW
UG58 NL17SZ08DFT2G_SC70-5 DDS@
DDS_EN_LCDVCC
ENVDD_D

EC (BIST MODE)
<59> LCD_VCC_TEST_EN
DV15 BAT54C_SOT23-3-D
ENVDD_D
ENVDD

APU WOV 1.8V to module 3.3V

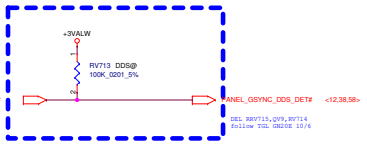
+VDDIO_AUDIO
DMIC 1.8V POWER
CA1 0.1U_0201_10V6K
@RA120 2.2K_0201_1%
+3VS_CAM
DMIC 3.3V POWER
CA2 0.1U_0201_10V6K
UA1 SA0000ANI00
VCCA VCCB GND DIR A B
74LVC1T45GW_SC-88
<9> APU_WOV_CLK
APU_WOV_CLK
UFC_OE
RA1 1 2 0_0201_1%
RE548 2 1 0_0402_5% APU_WOV_CLK_L
RA124 1 @ 2 2.2K_0201_1%
+3VS_CAM
To PCH
From Module
+VDDIO_AUDIO
DMIC 1.8V POWER
@RA122 2.2K_0201_1%
+3VS_CAM
DMIC 3.3V POWER
RA123 @ 2.2K_0201_1%
UA3 SA00001NQ00
VCC NC A GND Y
74LVC1G17GW_TSSOP_5P
<9> APU_WOV_DAT
APU_WOV_DAT
APU_WOV_DAT_L
DATA OUTPUT
DATA INPUT

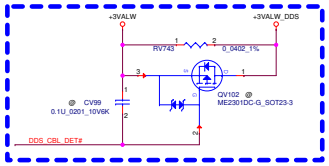
+LCDVDD_R
C5 0.01U_0201_10V6K
C728 47U_0603_6.3V6M
+3VALW
+LCDVDD_R
+LCDVDD
C4 10U_0402_6.3V6M
U7 SY6288C20AAC_SOT23-5-X
IN OUT GND EN OC
R13 0_0603_5%
ENVDD
R12 100K_0201_5%
9/30 Del Unuse OC
High Active

Main Func = LCDVDD monitor

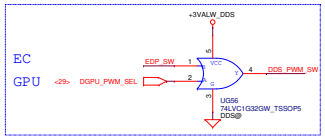
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2018/02/05	Title: eDP/Camera
Document Number: LA-K453P			Rev: 0.1
Date: Friday, February 05, 2021	Sheet 38 of 121		

Main Func = DDS

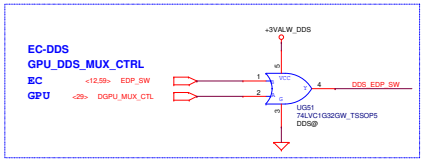


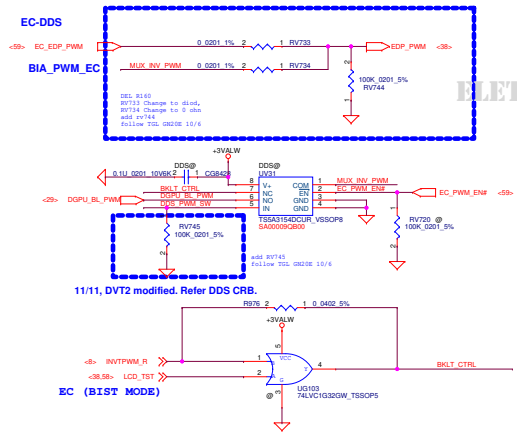


To PWM Switch



To MUX Switch

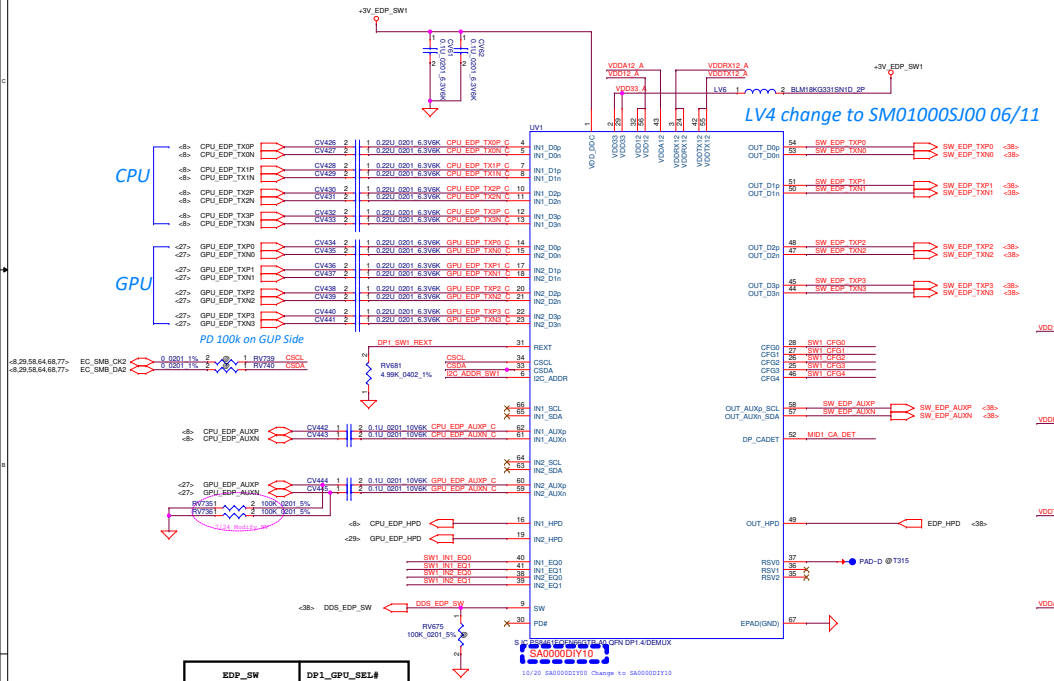




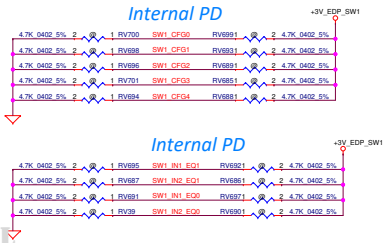
ELETRO-X TECHNICAL

EN#	IN	NC to COM COM to NC	NO to COM COM to NO	Function
L	L	ON	OFF	IGPU
L	H	OFF	ON	DGPU
H	X	OFF	OFF	X

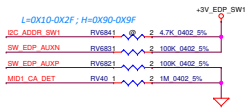
Main Func = eDP MUX

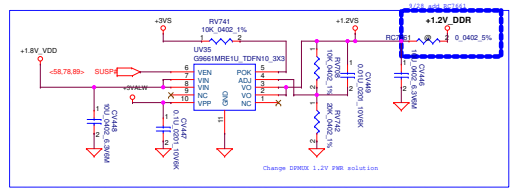


EDP_SW	DP1_GPU_SEL#
0 (Default)	CPU Input Port1
1	GPU Input Port2



EQ0, EQ1	LEVEL
LL	Compensate 11 dB @ HBR3
LM	Compensate 13 dB @ HBR3
LH	Compensate 15 dB @ HBR3
ML	Compensate 16 dB @ HBR3
MM	Compensate 17 dB @ HBR3
MH	Compensate 18 dB @ HBR3
HL	Compensate 19 dB @ HBR3
HM	Compensate 20 dB @ HBR3
HH	Compensate 21 dB @ HBR3





+1.2V_RUN power ripple need <30mV

ELETRO-X TECHNICAL

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2019/04/01

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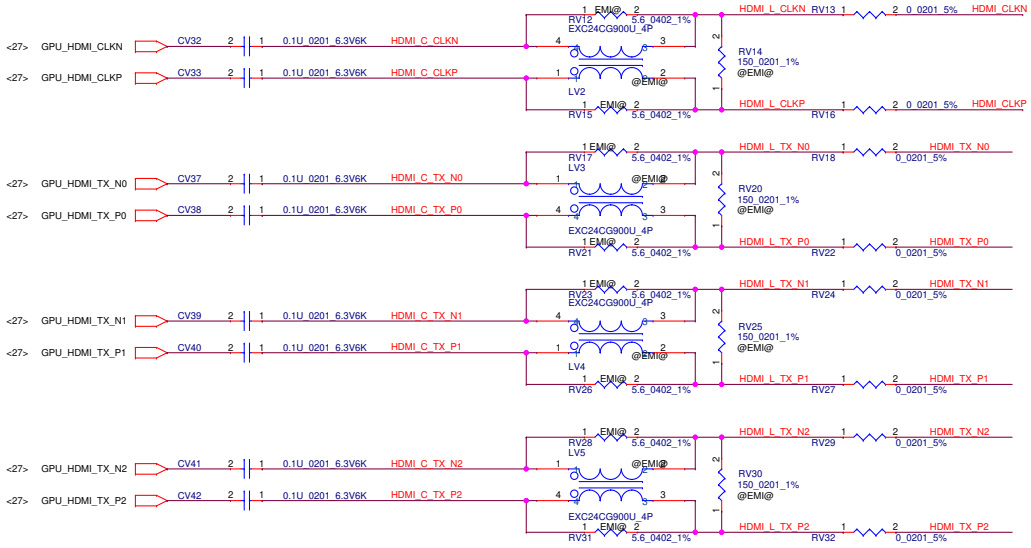
Compal Electronics, Inc.

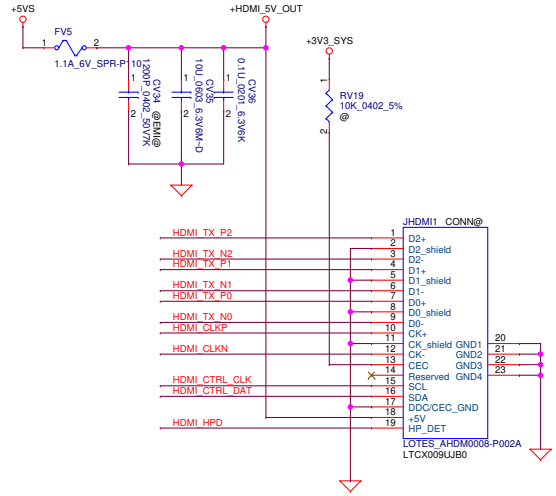
Title: eDP MUX/DDS

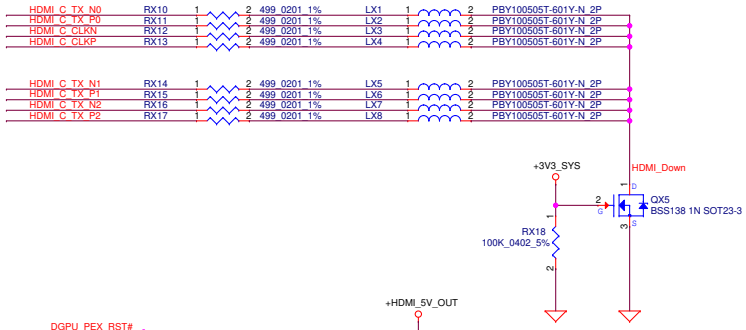
Document Number: LA-K453P

Rev: 0.1

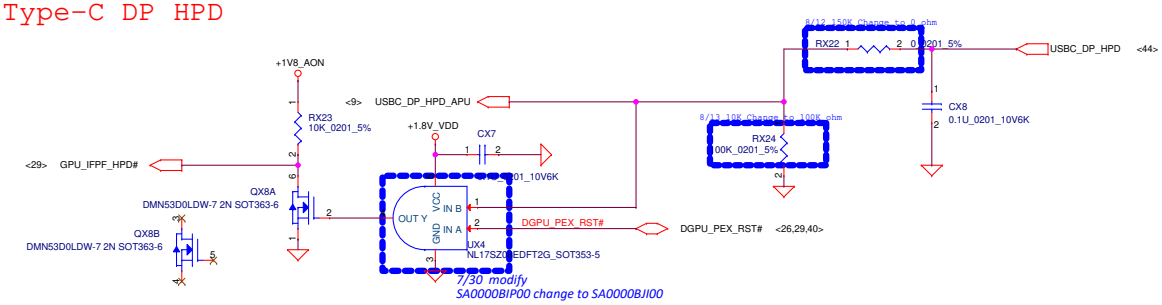
Date: Friday, February 05, 2021 Sheet 39 of 121



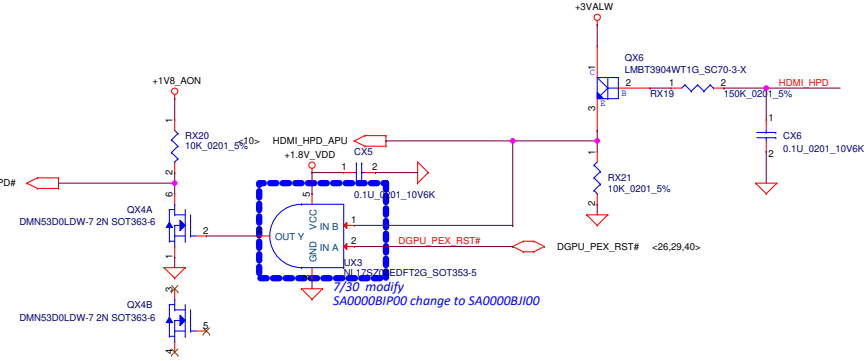


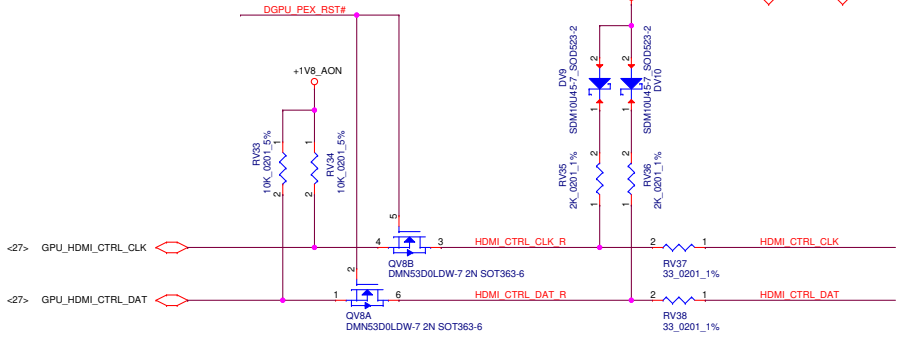


Type-C DP HPD



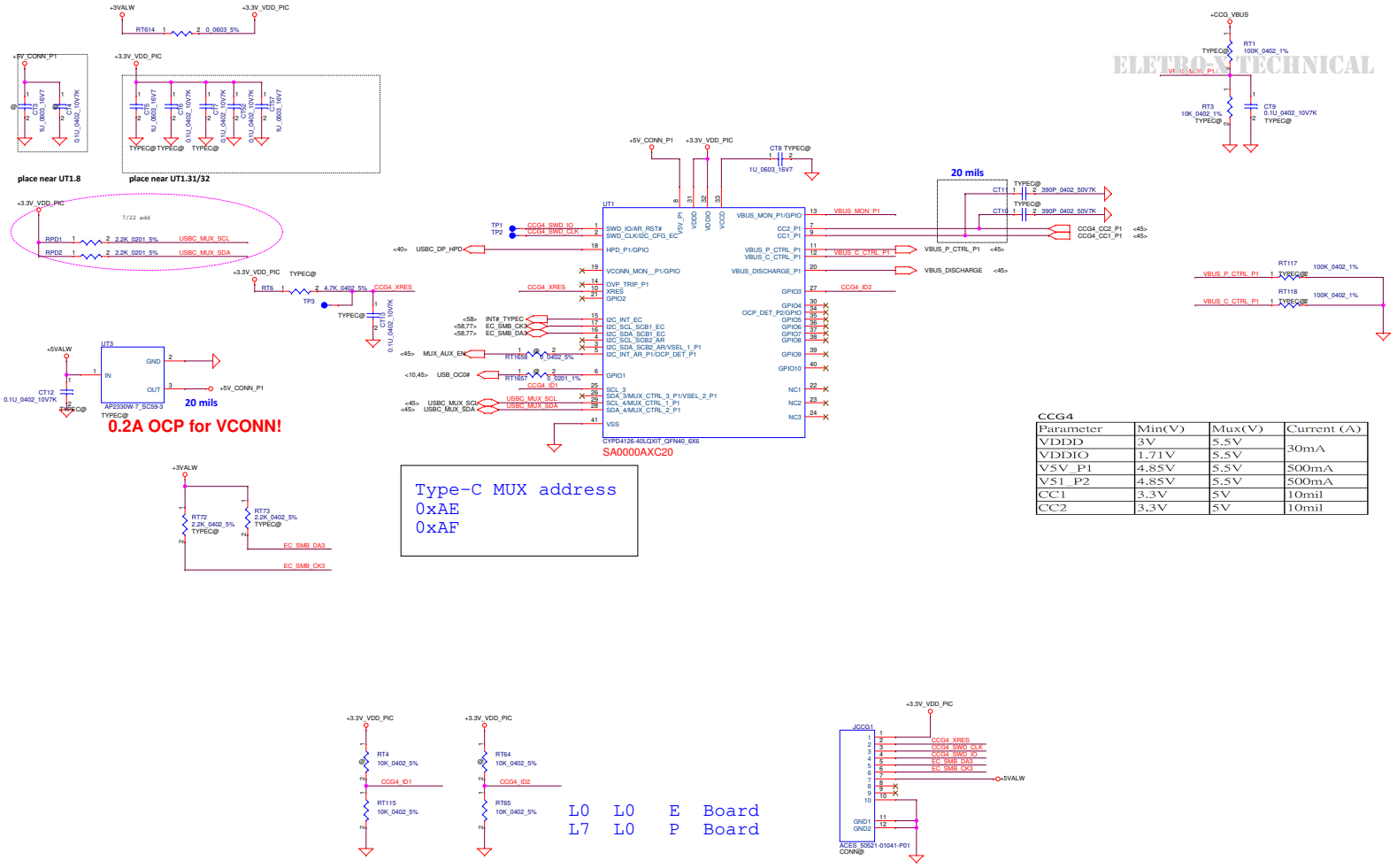
7/15 add





Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/02/05

Compal Electronics, Inc.			
Title	HDMI		
Size	Document Number	LA-K453P	Rev 0.1
Date:	Friday, February 05, 2021	Sheet 40 of 121	



CCG4

Parameter	Min(V)	Mux(V)	Current (A)
VDDD	3V	5.5V	30mA
VDDIO	1.71V	5.5V	
V5V_P1	4.85V	5.5V	500mA
V51_P2	4.85V	5.5V	500mA
CC1	3.3V	5V	10mil
CC2	3.3V	5V	10mil

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

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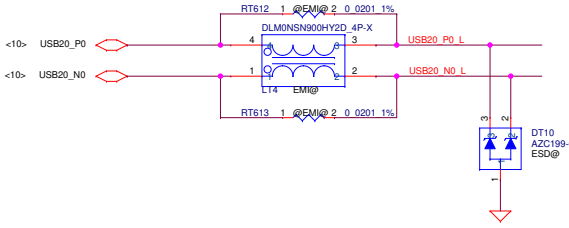
Compal Electronics, Inc.

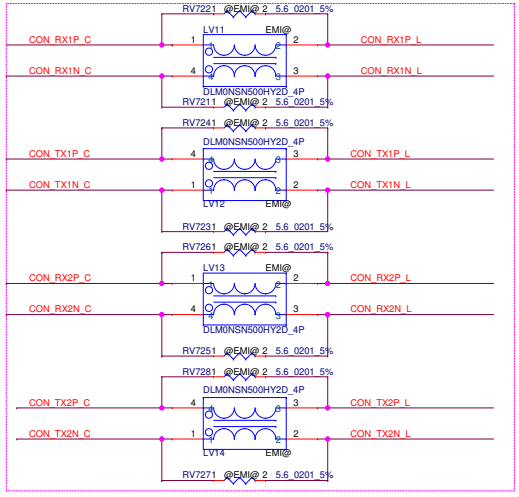
Title: Cypress PD Control

Size: Custom | Document Number: LA-K453P | Rev: 0.3(002)

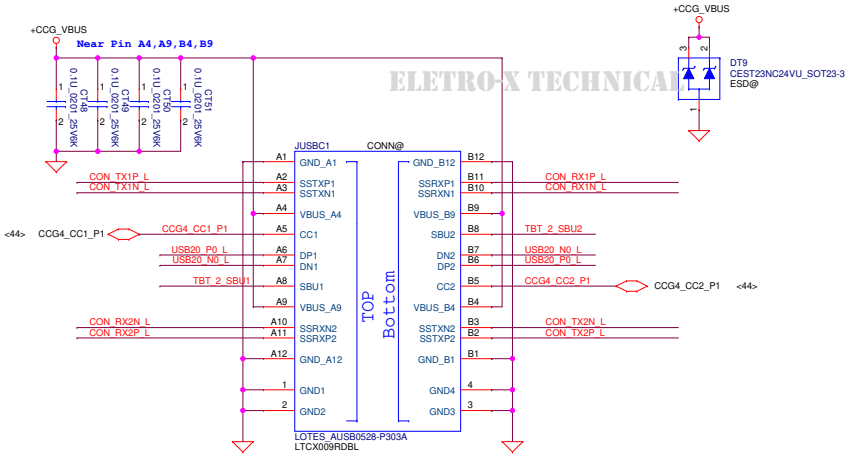
Date: Friday, February 05, 2021 | Sheet 44 of 121

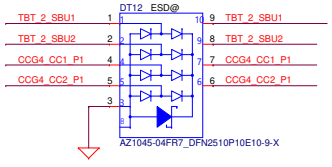
Main Function:



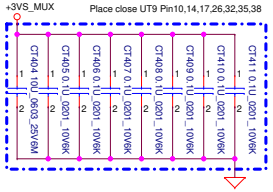


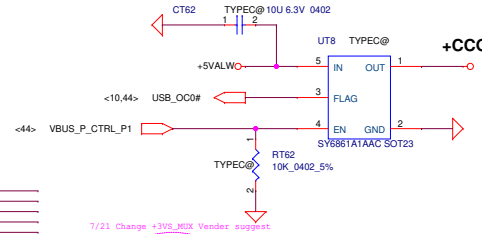
2020/7/20 Modify

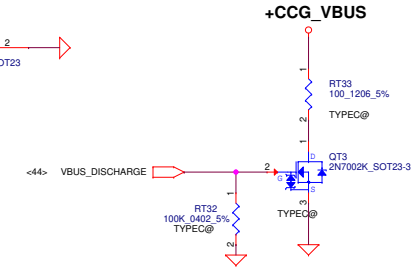


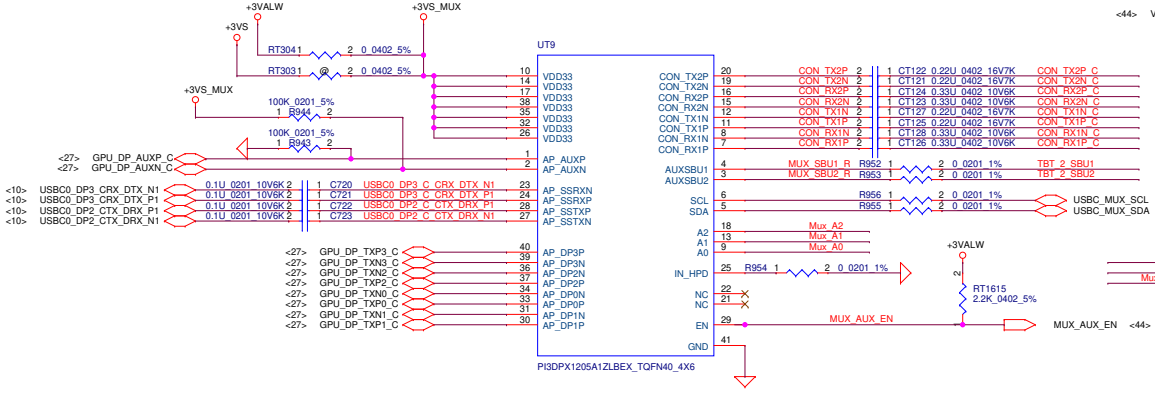


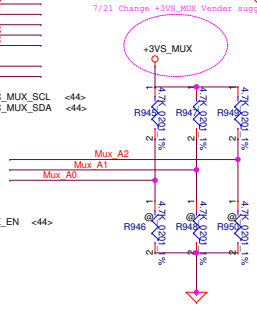
5V@3A



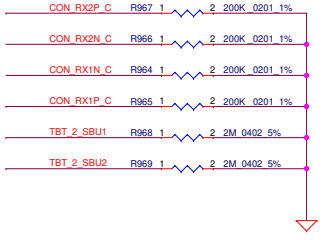


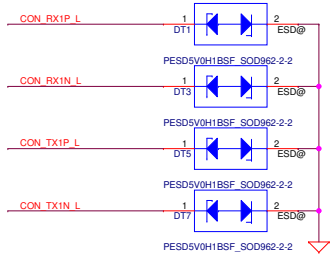


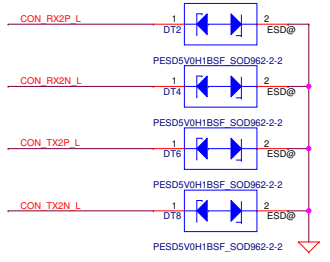




Type-C 5V Provide Path Control







ELETRO-X TECHNICAL

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

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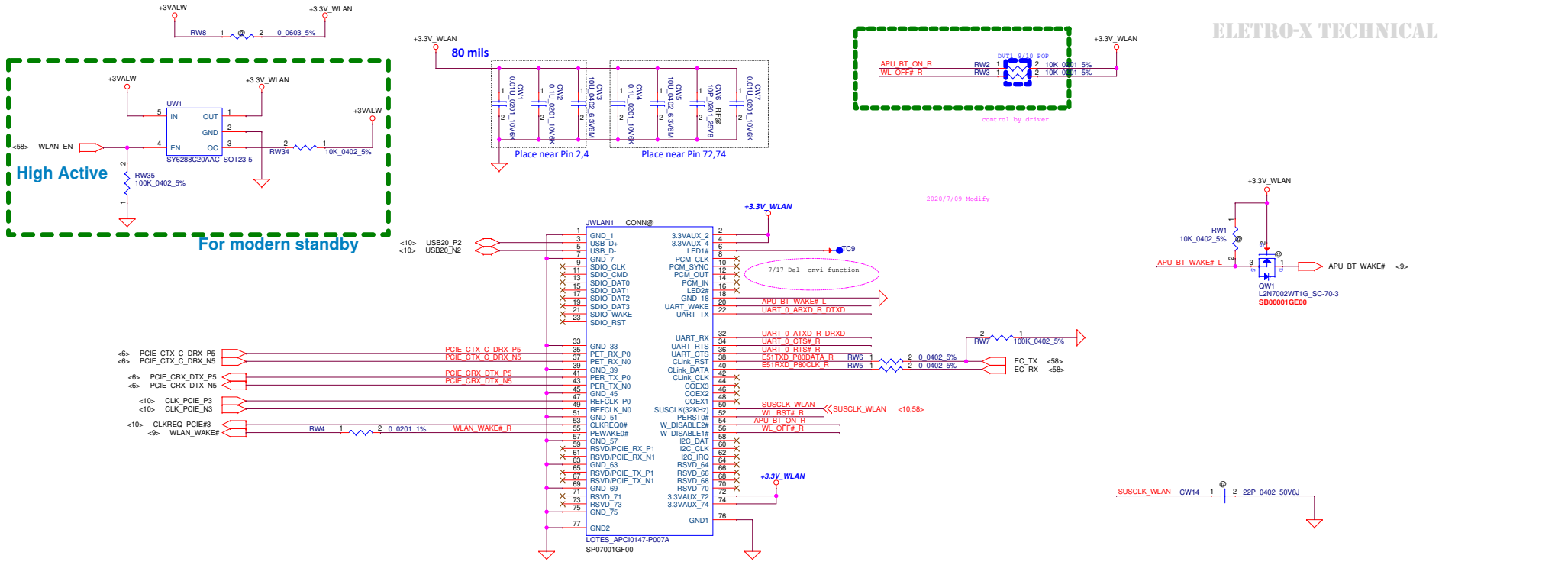
Compal Electronics, Inc.

Title: TypeC CONN

Size: B | Document Number: LA-K453P | Rev: 0.1

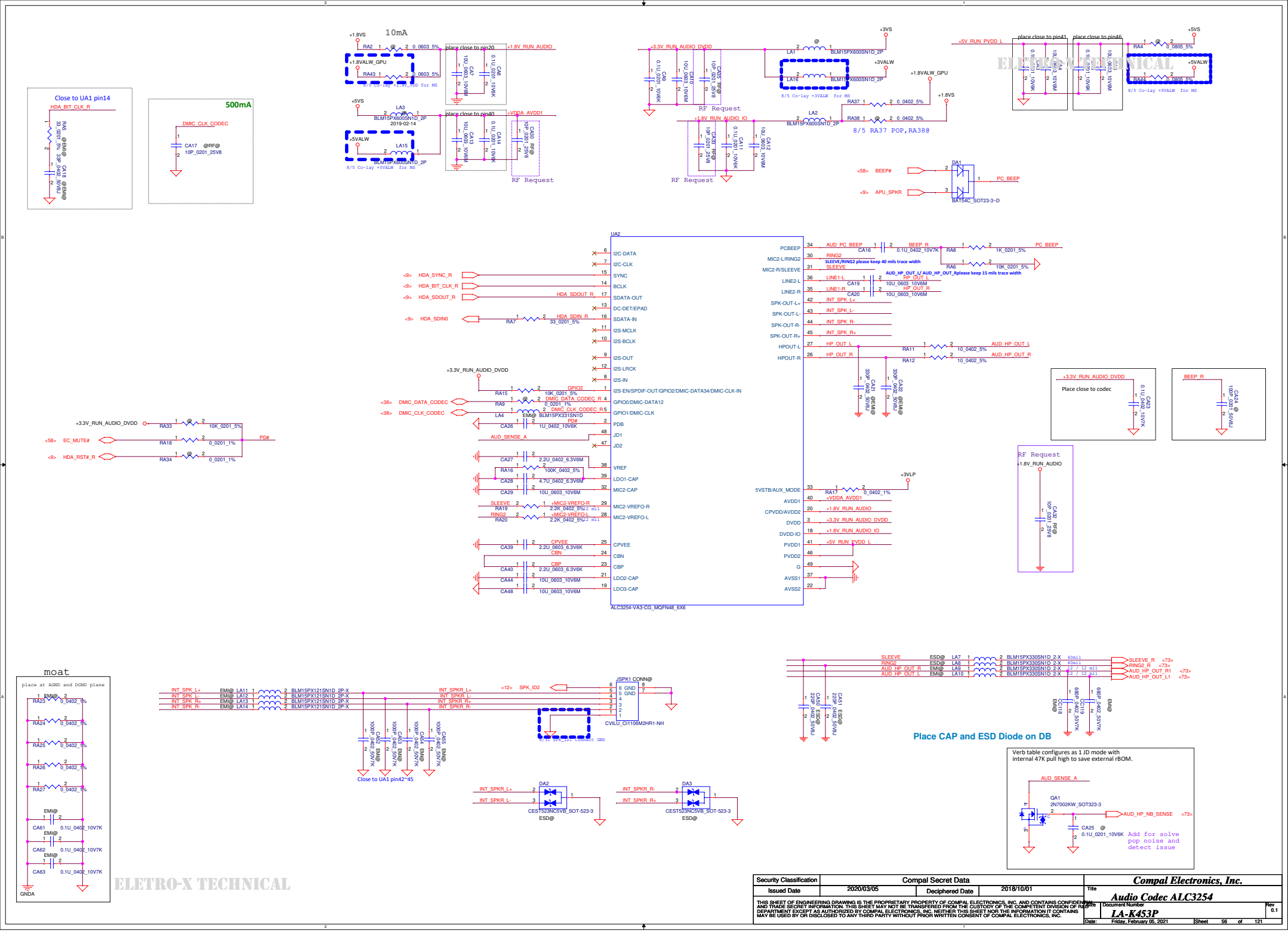
Date: Friday, February 05, 2021 | Sheet 45 of 121

Main Func = WLAN M.2



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/10/01

Compal Electronics, Inc.		
Title	WLAN/BT (w/ CNVi) M.2	
Size	Document Number LA-K453P	Rev 0.1
Date: Friday, February 05, 2021	Sheet 52 of 121	



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2018/10/01	Title: Audio Codec ALC3254
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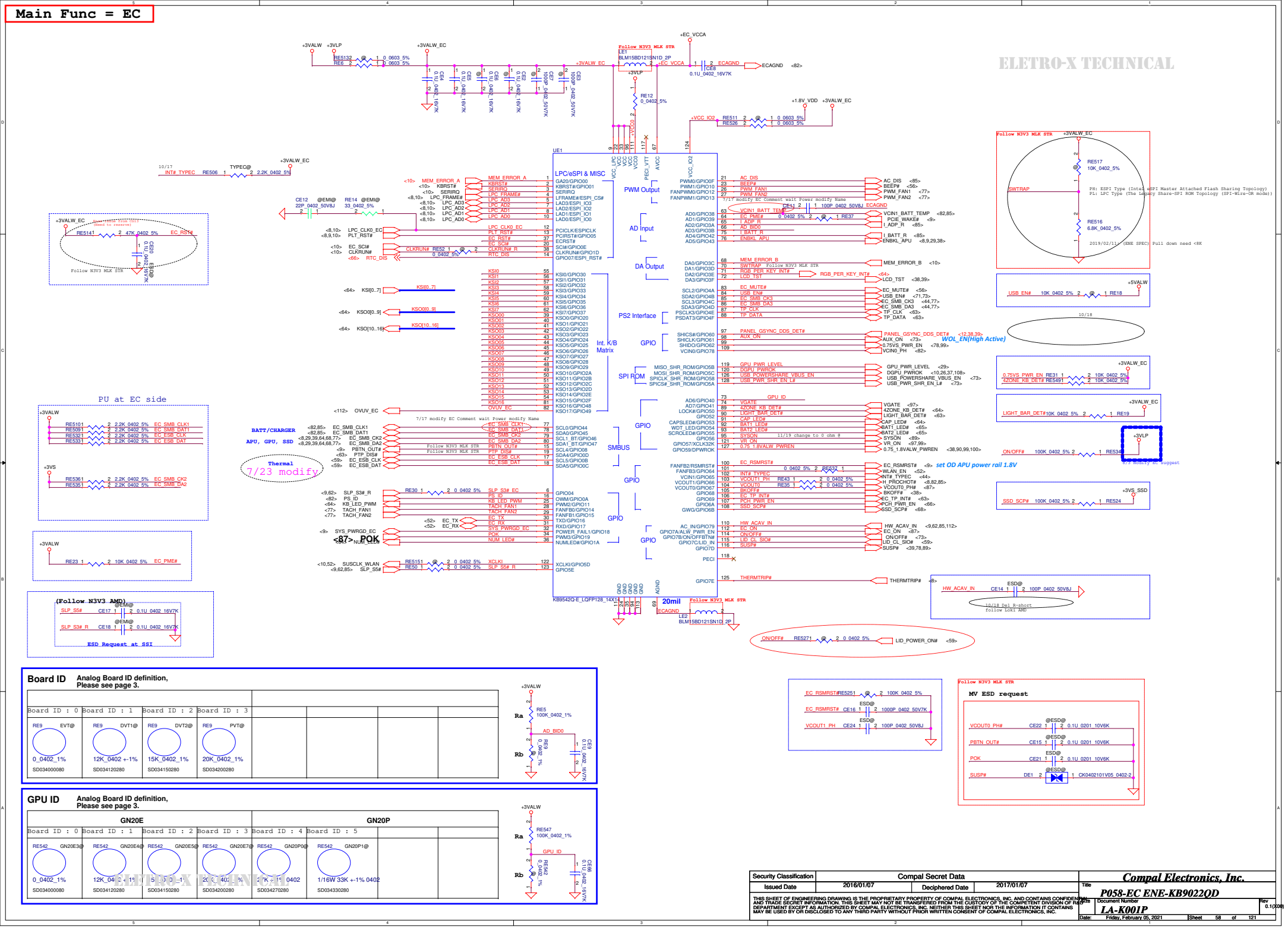
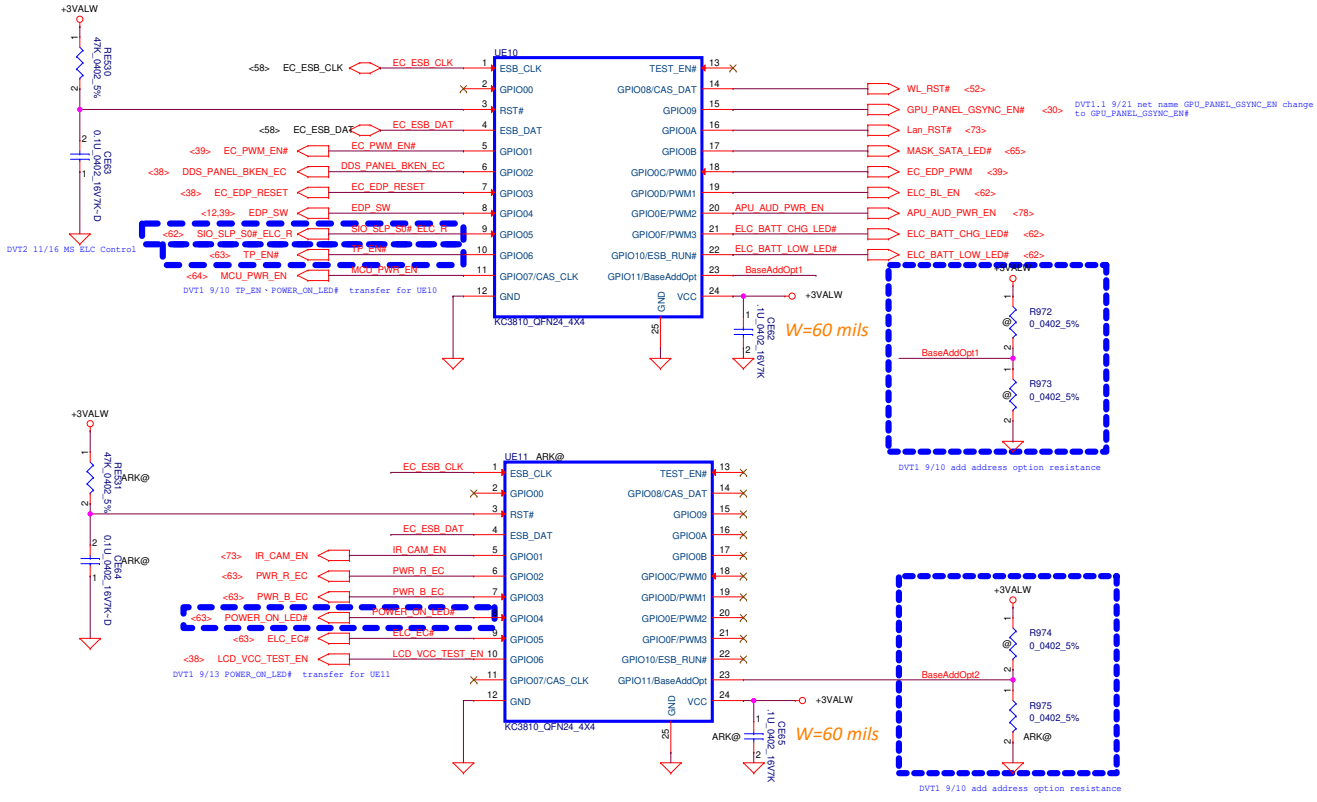
			Date: Friday, February 05, 2021 Sheet 56 of 121

Main Func = EC


UE1
LPC/eSPI & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI ROM
SMBUS
GPIO
KB9542Q-E_LQFP128_14X14
PU at EC side
Board ID
Analog Board ID definition,
Please see page 3.
Board ID : 0
Board ID : 1
Board ID : 2
Board ID : 3
0_0402_1%
12K_0402 +-1%
15K_0402_1%
20K_0402_1%
GPU ID
GN20E
GN20P
Board ID : 4
Board ID : 5
1/16W 33K +-1% 0402
ELETRO-X TECHNICAL
Compal Secret Data
Compal Electronics, Inc.
P058-EC ENE-KB9022QD
LA-K001P

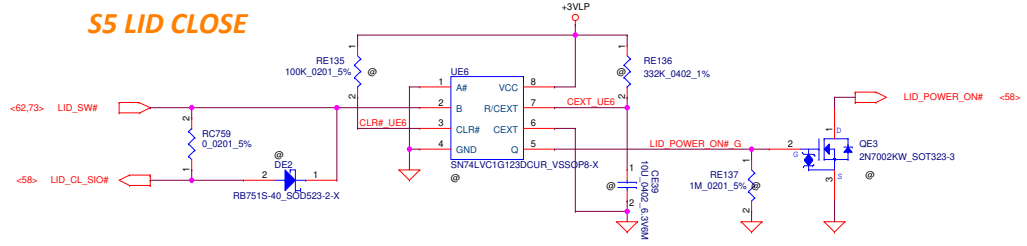
Main Func = GPIO Expander



FUNCTION TABLE

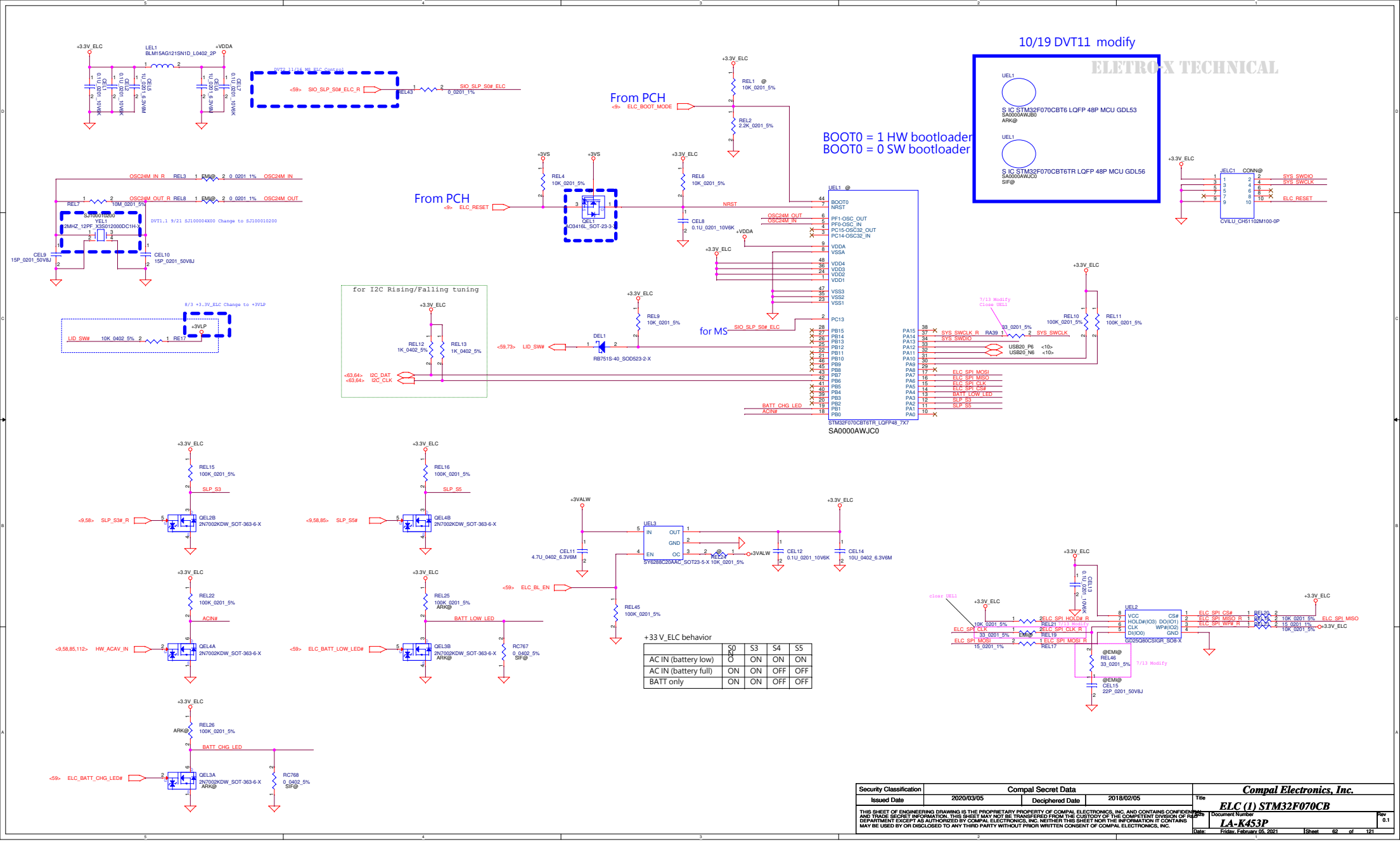
INPUTS			OUTPUTS
$\overline{CLR}$	$\overline{A}$	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	↑	⎍
H	↓	H	⎍
↑	L	H	⎍

S5 LID CLOSE

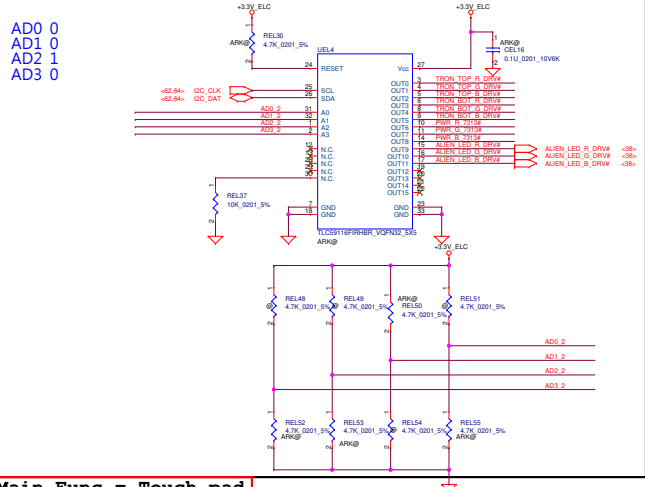


Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/10/01

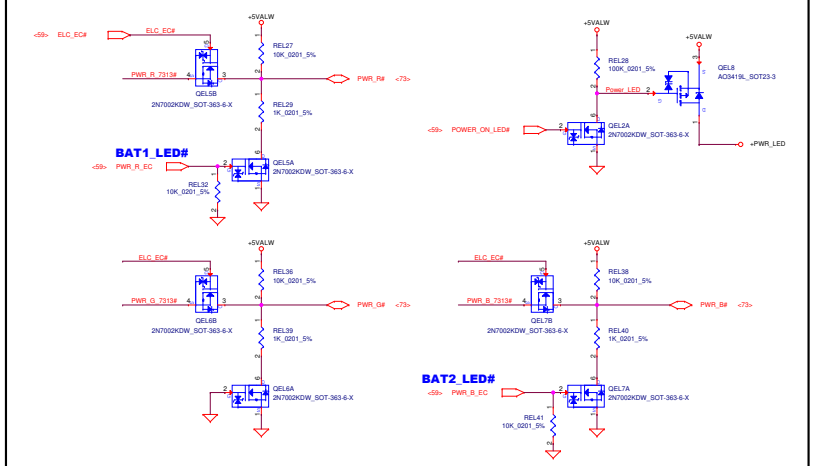
Compal Electronics, Inc.	
Title	GPIO Expander/WDT/S5 LID
Size	Document Number: LA-K453P
Rev	0.1
Date: Friday, February 05, 2021	Sheet 59 of 121


10/19 DVT11 modify
ELETRO-X TECHNICAL
From PCH
<9> ELC_BOOT_MODE
BOOT0 = 1 HW bootloader
BOOT0 = 0 SW bootloader
From PCH
<9> ELC_RESET
for I2C Rising/Falling tuning
for MS
SIO_SLP_S0#_ELC
LID_SW#
BATT_CHG_LED
ACIN#
SYS_SWCLK
SYS_SWDIO
ELC_RESET
ELC_SPI_MOSI
ELC_SPI_MISO
ELC_SPI_CLK
ELC_SPI_CS#
BATT_LOW_LED
SLP_S3
SLP_S5
STM32F070CBT6TR_LQFP48_7X7
SA0000AWJC0
+33 V_ELC behavior
S0
S3
S4
S5
AC IN (battery low)
ON
ON
ON
AC IN (battery full)
ON
ON
OFF
OFF
BATT only
ON
ON
OFF
OFF
Compal Secret Data
2020/03/05
2018/02/05
Compal Electronics, Inc.
ELC (1) STM32F070CB
LA-K453P
Rev 0.1
Friday, February 05, 2021
Sheet 62 of 121

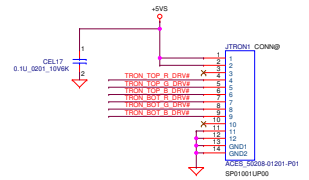
Main Func = ELC



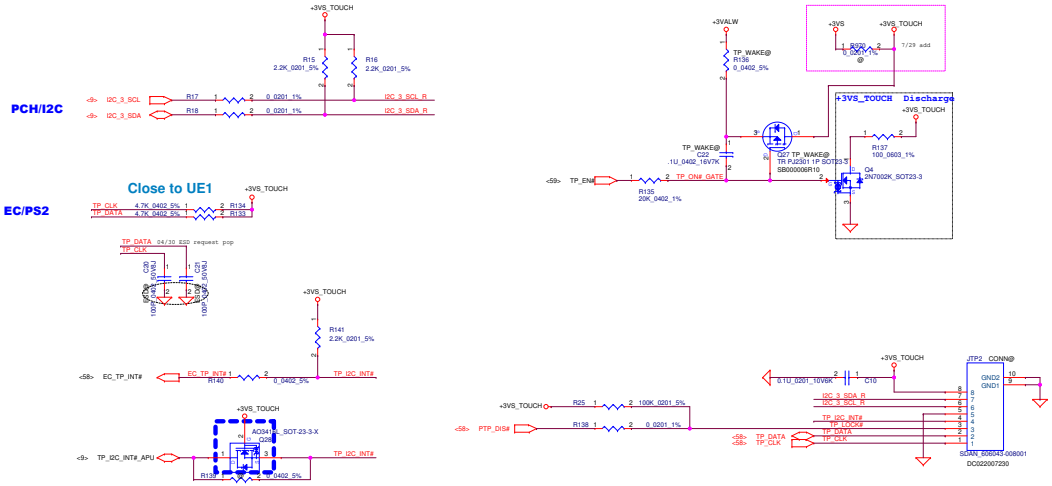
Main Func = Power LED



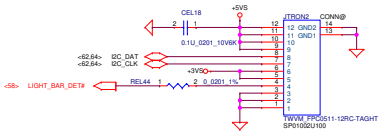
Main Func = ON/OFF TRON



Main Func = Touch pad

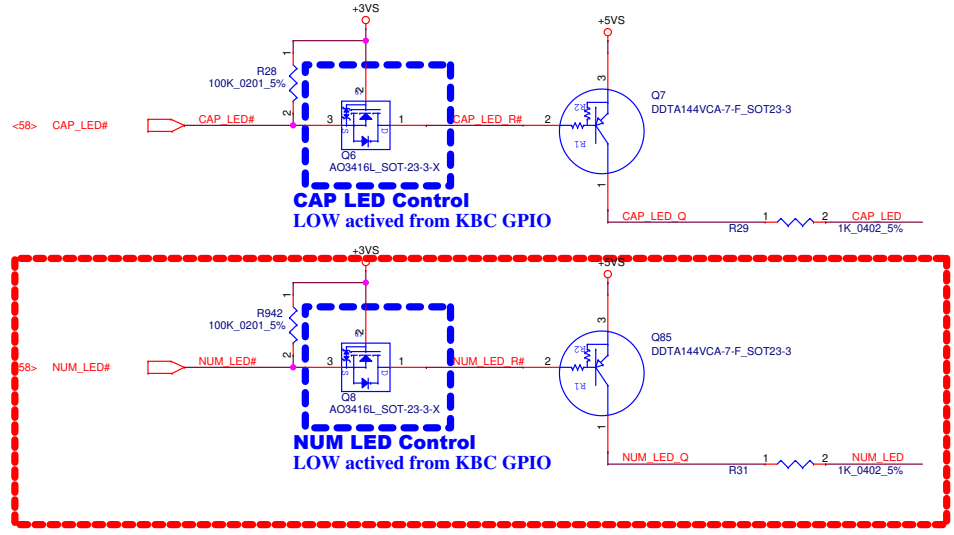


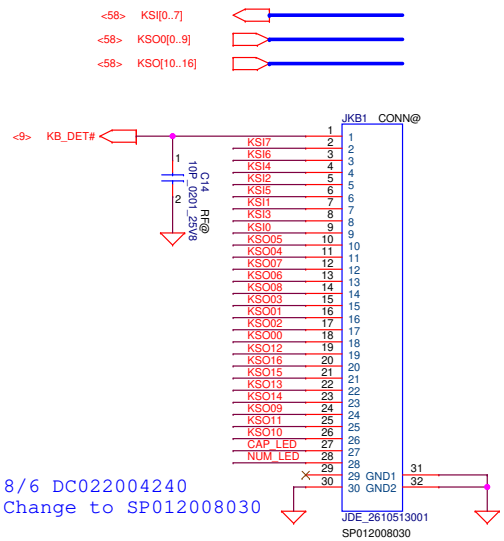
Main Func = Primax Front Lighting

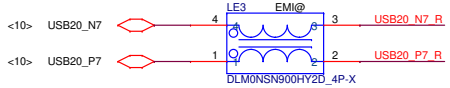


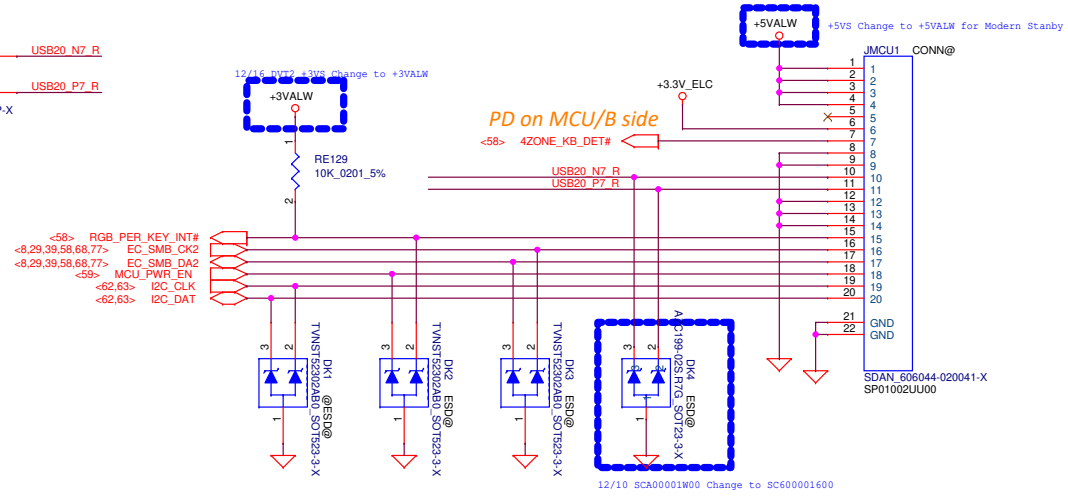
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2018/02/05	Title: ELC (2) TP/PWR/TRON
Document Number: LA-K453P			Rev: 0.1
Date: Friday, February 05, 2021	Sheet 53 of 121		

Main Func = KB/KBBL



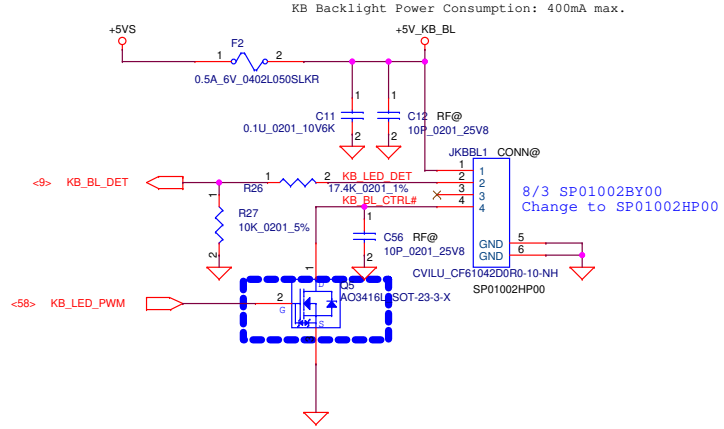






SIF only

Keyboard Backlight



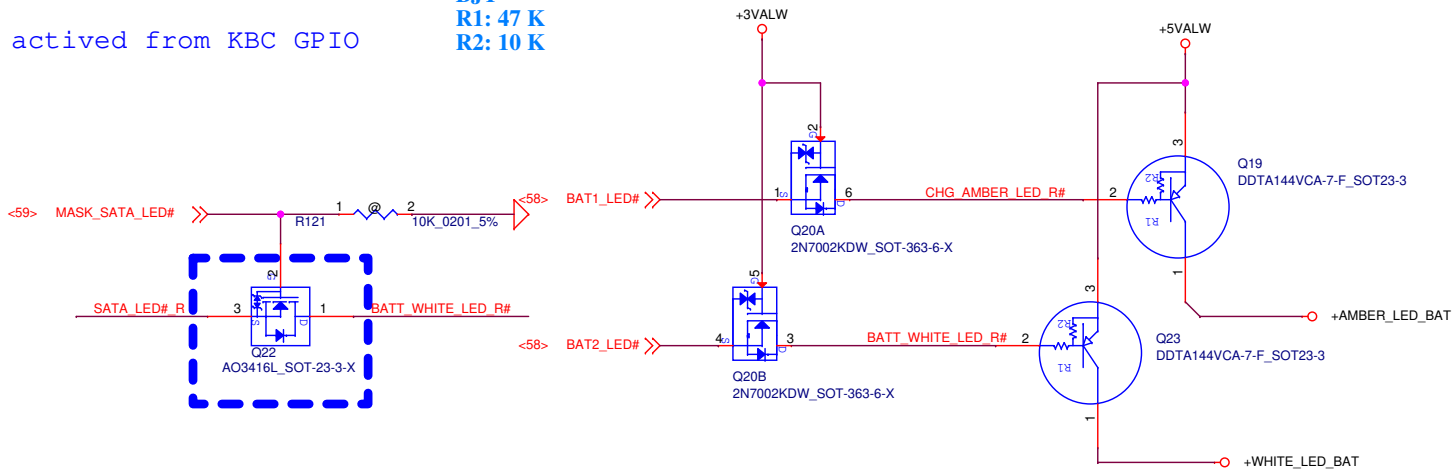
Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/02/05

Compal Electronics, Inc.			
Title	MCU Per Key/4 Zone KB		
Size	Document Number	LA-K453P	Rev 0.1
Date:	Friday, February 05, 2021	Sheet	64 of 121

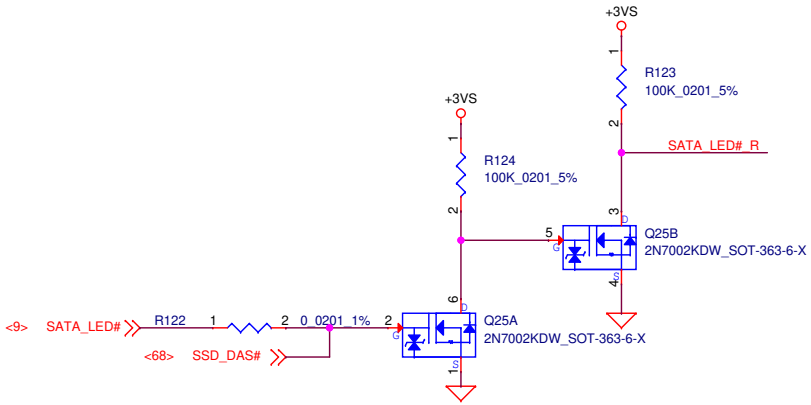
Main Func = Battery LED

Low actived from KBC GPIO

BJT
R1: 47 K
R2: 10 K



Main Func = M_BIST



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2019/04/01

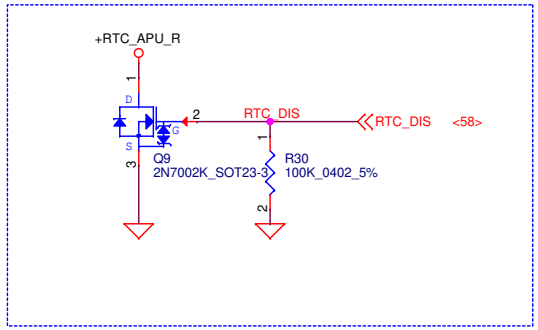
Compal Electronics, Inc.

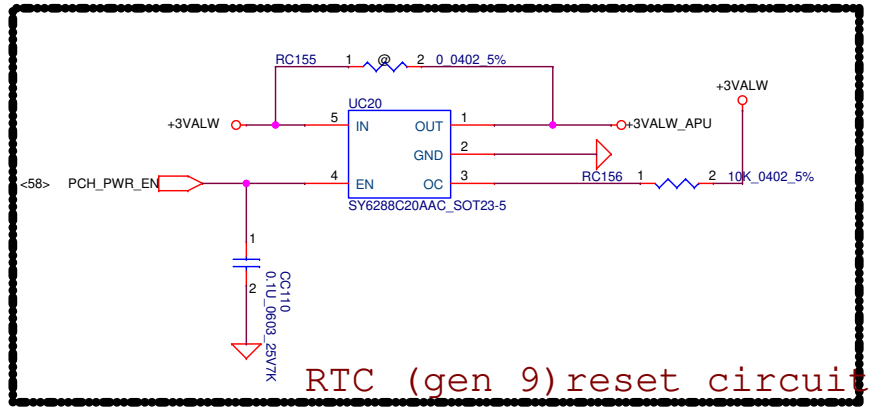
Title: LED (SIF)

Size: B26 | Document Number: LA-K453P | Rev: 0.1

Date: Friday, February 05, 2021 | Sheet 65 of 121

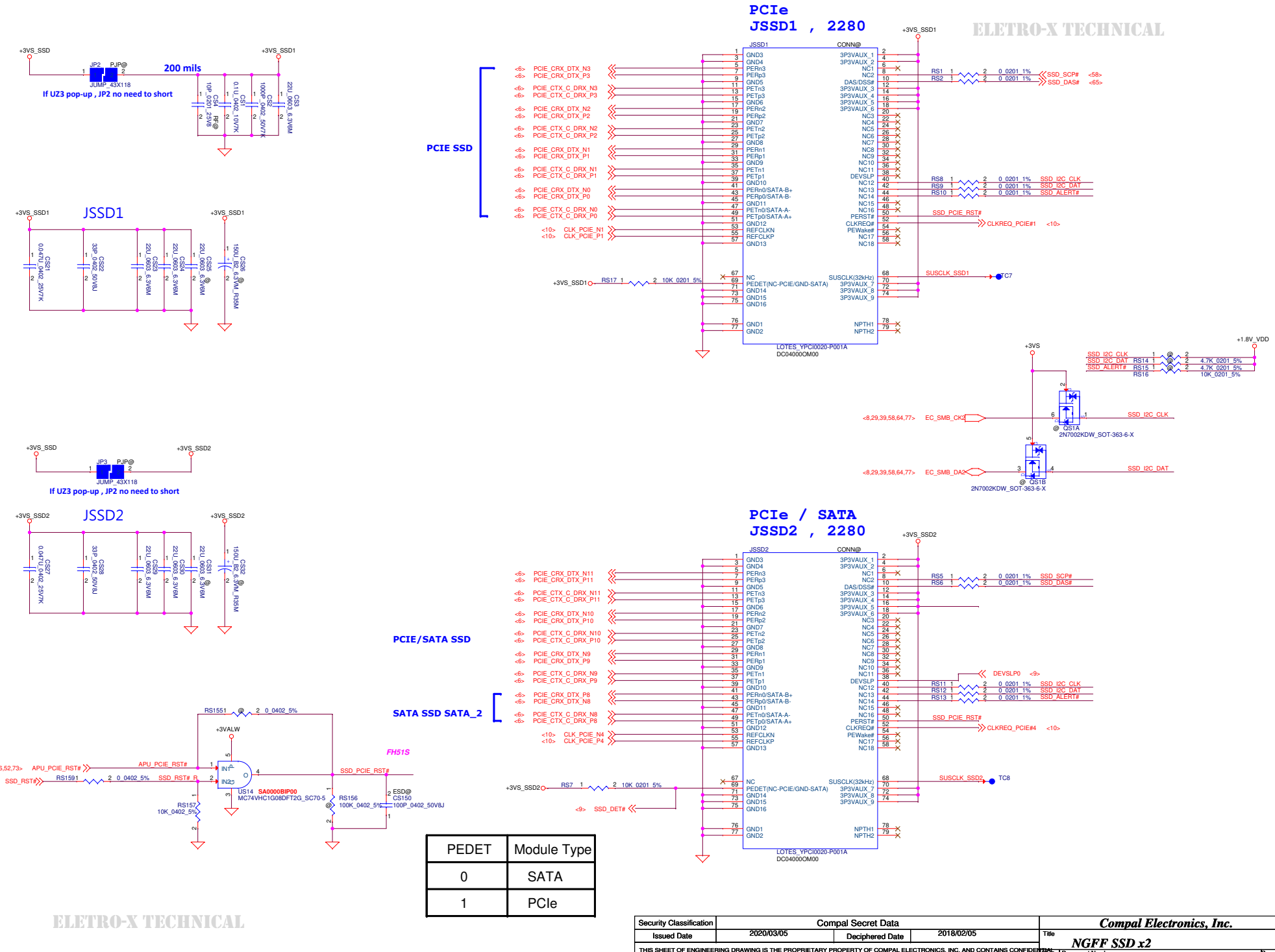
Main Func = RTC Gen9





Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title: RTC Gen9			
Size: B	Document Number: LA-K453P		Rev: 0.1
Date: Friday, February 05, 2021	Sheet 66 of 121		



PEDET	Module Type
0	SATA
1	PCIe

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/02/05

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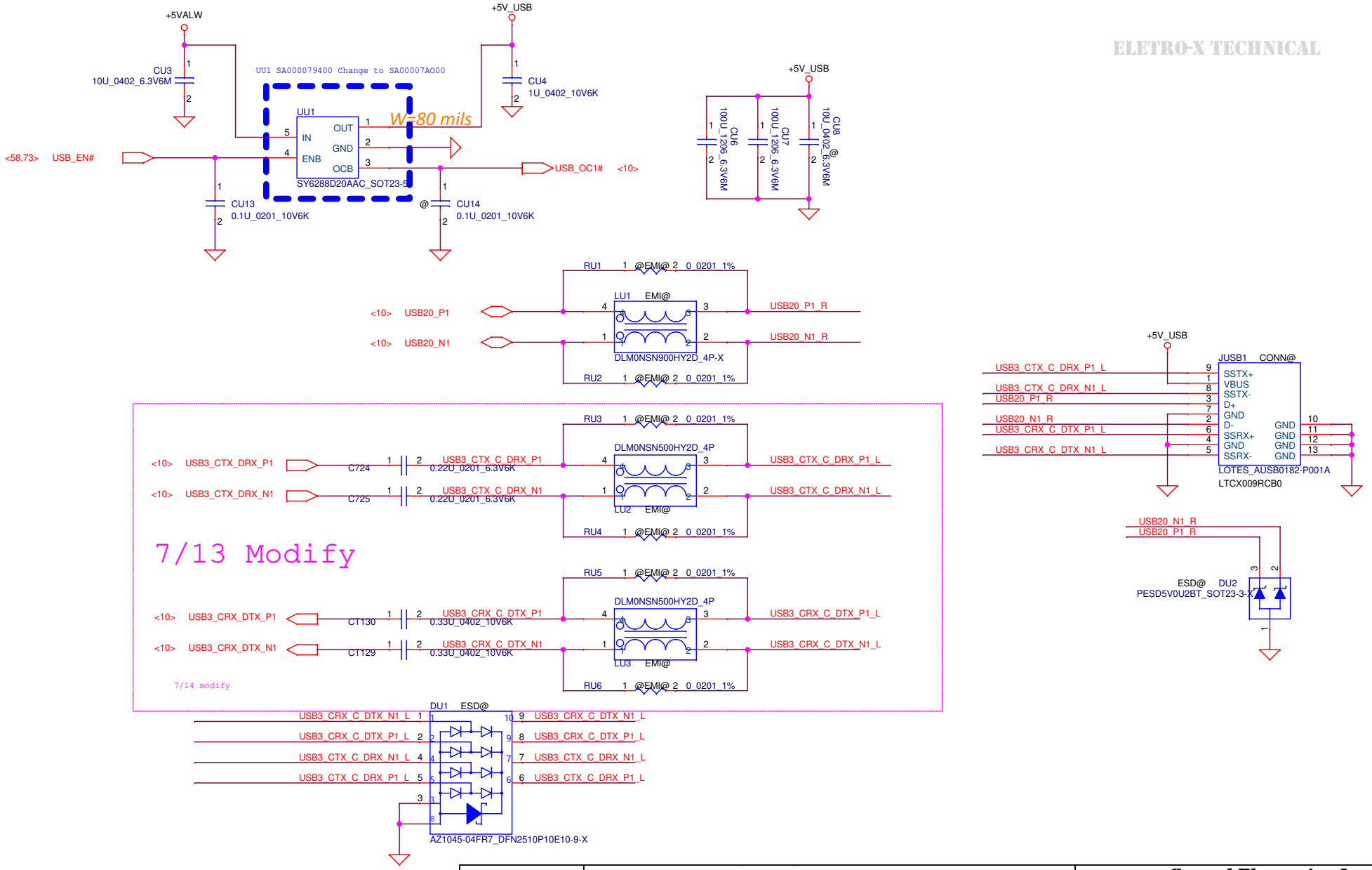
Compal Electronics, Inc.

Title: NGFF SSD x2

Document Number: LA-K453P

Rev: 0.1

Date: Friday, February 05, 2021 | Sheet 68 of 121



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

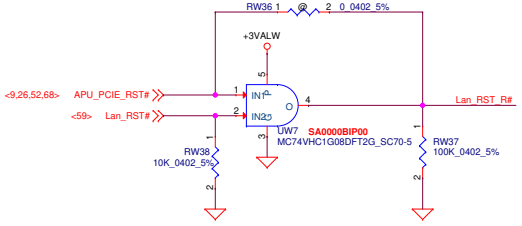
Compal Electronics, Inc.

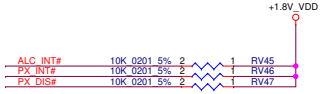
Title: **USB3.1 TypeA Gen1**

Document Number: **LA-K453P**

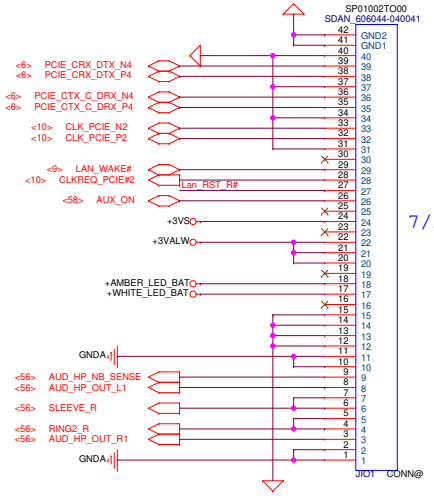
Rev: 0.1

Date: Friday, February 05, 2021 Sheet 71 of 121





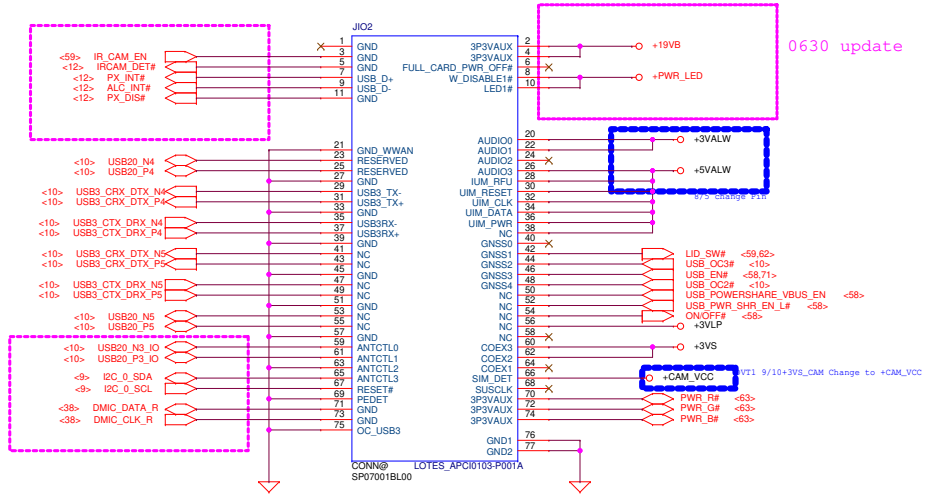
to LAN



7/28 JIO1反接 Connecter 反向

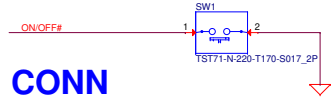
B Key CONN

0630 update



0630 update

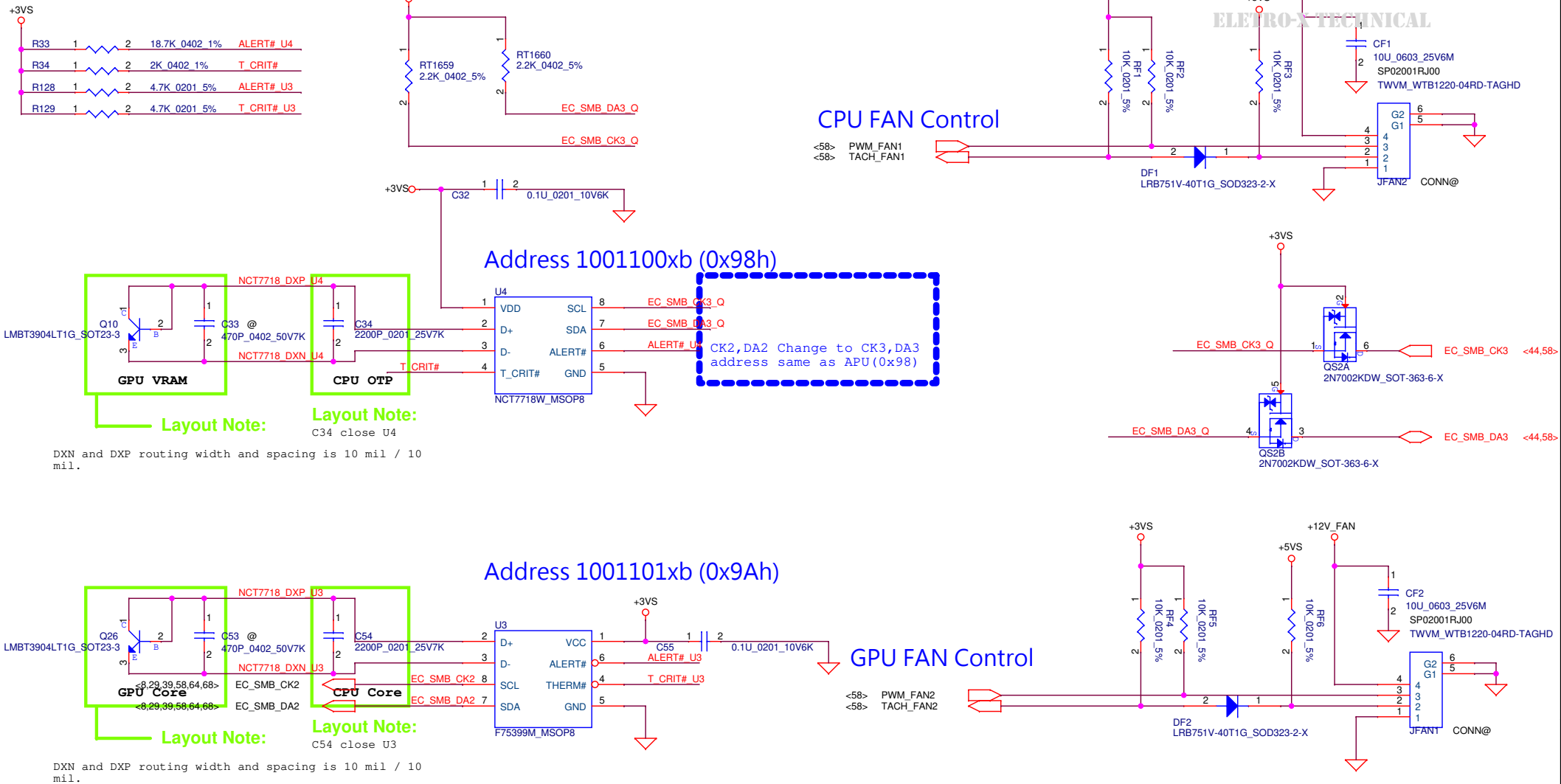
0630 update



For LAN DB CONN

For USB DB CONN

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2018/02/05	Title: IO Board CONN
Document Number	LA-K453P		Rev 0.1
Date: Friday, February 05, 2021	Sheet 73 of 121		



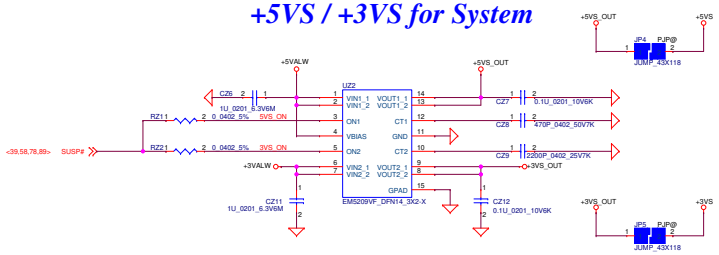
TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/02/05

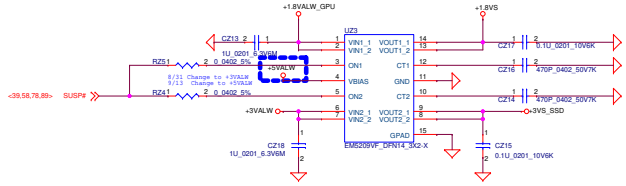
Compal Electronics, Inc.			
Title: FAN/Thermal			
Size: D	Document Number: LA-K453P		Rev: 0.1
Date: Friday, February 05, 2021	Sheet 77 of 121		

Main Func = DC/DC

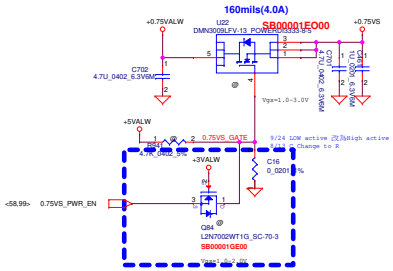
+5VS / +3VS for System

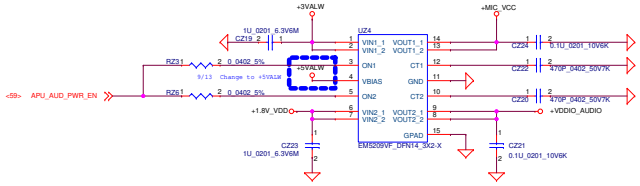


+1.8VS/+3V_SSD for System



+0.75VS for System





Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2019/04/01	Title: DC/DC Interface
			Size: Document Number: LA-K453P Rev: 0.1
			Date: Friday, February 05, 2021 Sheet 78 of 121

Main Func = DCIN CONN

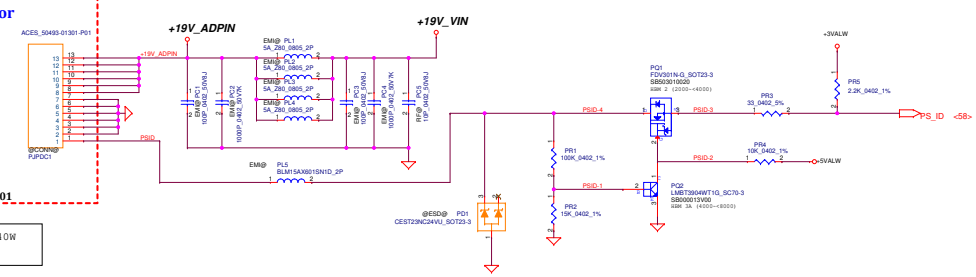
Adapter Connector

Adapter Bot Side

PIN1 ADPIN
PIN2 GND
PIN3 GND
PIN4 GND
PIN5 GND
PIN6 GND
PIN7 GND
PIN8 ADPIN
PIN9 ADPIN
PIN10 ADPIN
PIN11 ADPIN
PIN12 ADPIN
PIN13 ADPIN
ACES_50493-01301-P01

1176 PWR modify

Adapter 180W / 240W
240W/19V=12.63A

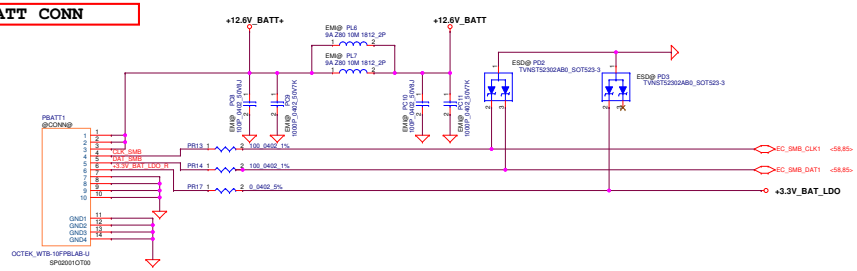


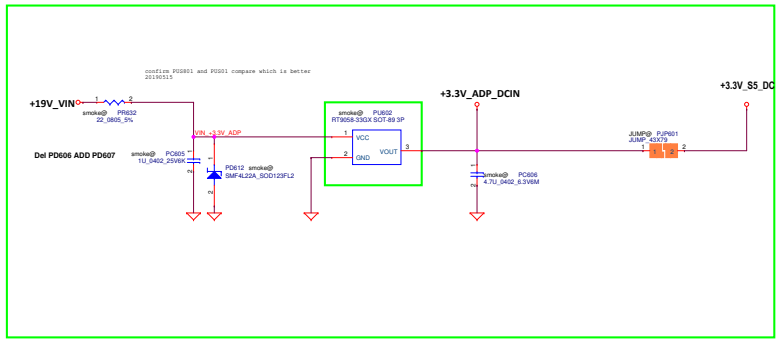
Main Func = BATT CONN

Battery Connector

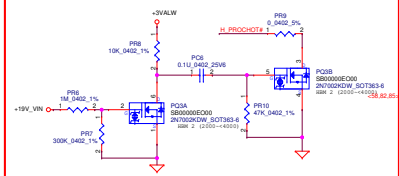
Battery Bot Side
Before - ->Aftre
PIN1 GND- ->PIN 10
PIN2 GND- ->PIN0 9
PIN3 GND- ->PIN0 8
PIN4 SYS_PRES#- ->PIN0 7
PIN5 BATT_PRS#- ->PIN0 6
PIN6 DAT_SMB#- ->PIN0 5
PIN7 CLK_SMB#- ->PIN0 4
PIN8 BATT+- ->PIN0 3
PIN9 BATT+- ->PIN0 2
PIN10 BATT+- ->PIN0 1
SP07001R500

Battery 56W
56W/11.4V=4.91A
Battery 86W
86W/11.4V=7.54A

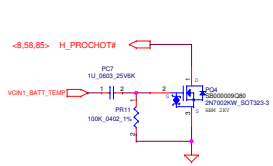


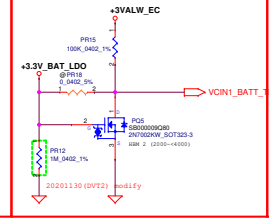


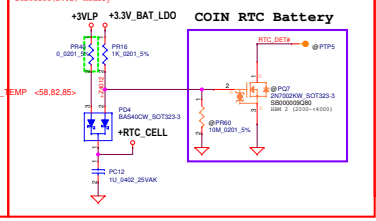
Adapter protection:



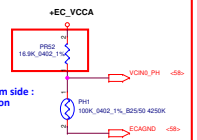
Battery protection:







APU OTP



PH1 under CPU bottem side :
CPU thermal protection
at 92 +/- 3 degree C

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

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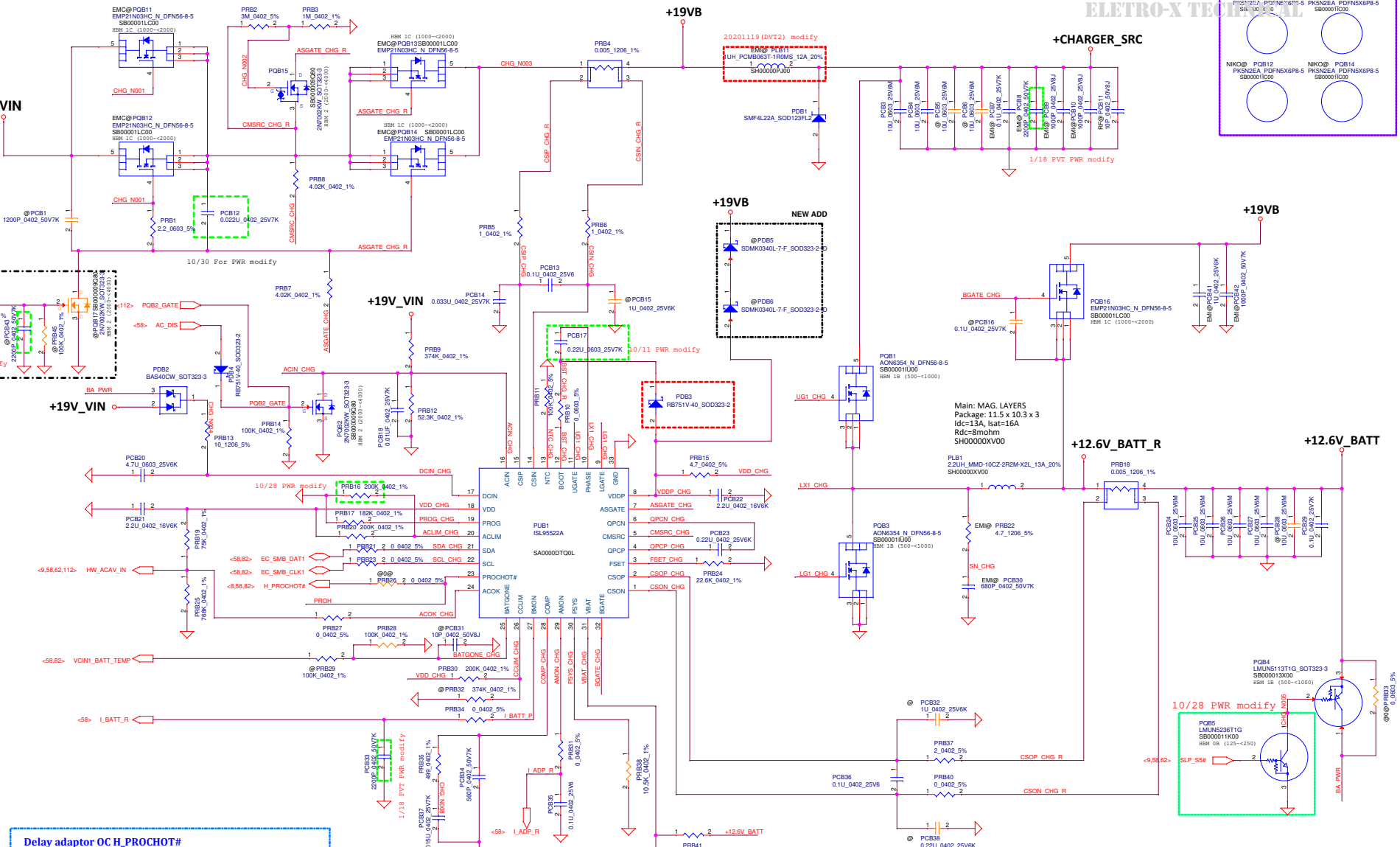
Compal Electronics, Inc.			
Title	PWR-DCIN / OTP / BATT CONN / RTC		
Size	Document Number		Rev
	LA-K453P		0.1
Date:	Friday, February 05, 2021	Sheet	82 of 121

Main Func = CHARGER



	CPN	Value	Effective capacitance	Renesas recommend
DCIN	SE000013880	4.7uF_0603_25V	0.4uF	0.4uF
VDD	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
VDDP	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
CBOOT	SE00000WA00	0.47uF_0402_25V	0.22uF	0.2uF

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2017/01/06	Title: PWR_CHARGER
			Size: Document Number: LA-K453P Rev: 0.1
			Date: Friday, February 05, 2021 Sheet 85 of 121

Main Func = 3VALWP / 5VALWP

3VALW
Vout=3.4V
TDC 9.3A
Peak Current 13A
OCP current 15.3A
OVP=3.824V~3.994V(112.5%~117.5%)
UVP=1.869V~2.209V(55%~65%)
FSW=355kHz

MOS (VGS = 4.5V)

	TYP	MAX
H/S Rds(on) :	6.7mohm	8.5mohm
L/S Rds(on) :	4.1mohm	5.2mohm

5VALW
Vout= 5.16V
TDC 14A
Peak Current 20A
OCP current 21.3A
OVP=5.805V~6.063V(112.5%~117.5%)
UVP=2.838V~3.354V(55%~65%)
FSW=300kHz

MOS (VGS = 4.5V)

	TYP	MAX
H/S Rds(on) :	6.7mohm	8.5mohm
L/S Rds(on) :	4.1mohm	5.2mohm

Input Current: 14.06A
3.4V*9.97A/0.85/9V=4.43A
5.16V*14.28A/0.85/9V=9.63A

POK need pull high, it will pull high on VS transfer circuit

Output capacitor ESR need follow below equation to make sure feed back loop stability
ESR=20mV*L*fsw/2V

20201119 (DVT2) modify
Main: TAI
Package: 10 x 10 x 3
Idc=16A, Isat=20A
Rdc=6.5mohm
SH00001TW00

Main: MAG. LAYERS
Package: 6.95 x 6.6 x 3
Idc=10A, Isat=13A
Rdc=12mohm
SH00001KN00

ESR = 25mohm

2020/07/06 HW control

10/7 EE Add

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: PWR_+3.3VALWP/+5VALWP

Size: C | Document Number: LA-K453P | Rev: 0.1

Date: Friday, February 05, 2021 | Sheet 87 of 121

Main Func = 1.2VP / 0.6VSP / 2.5V_MEMP

Input Current: 1.012A

1.203V*5.92A/0.85/9V=0.93A

0.6V*1.05A/0.85/9V=0.082A

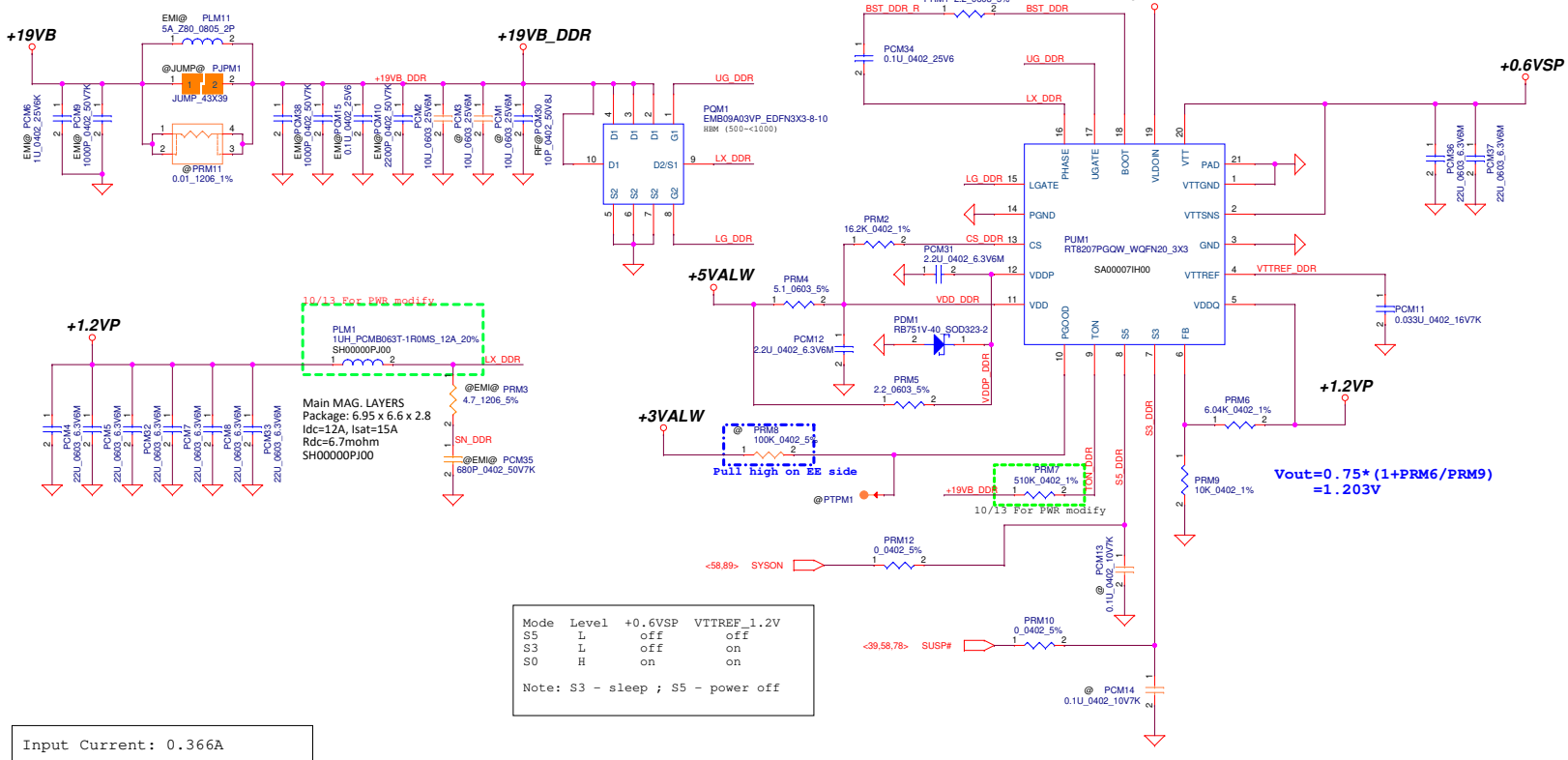
Pin19 need pull separate from +1.2VP.
If you have +1.2V and +0.6V sequence question,
you can change from +1.2VP to +1.2VS.

+1.2V_DDR
Vout= 1.203V
TDC 8A
Peak Current 10.2A
OCP current 13.44A
OVP=1.36V~1.44V(113%~120%)
UVP=0.72V~0.96V(60%~80%)
FSW= ~538KHz

MOS (VGS = 4.5V)

	TYP	MAX
H/S Rds(on) :	11mohm	13mohm
L/S Rds(on) :	11mohm	13mohm

+0.6V_DDR_VTT
Vout= 1.203V
TDC 1.05A
Peak Current 1.5A



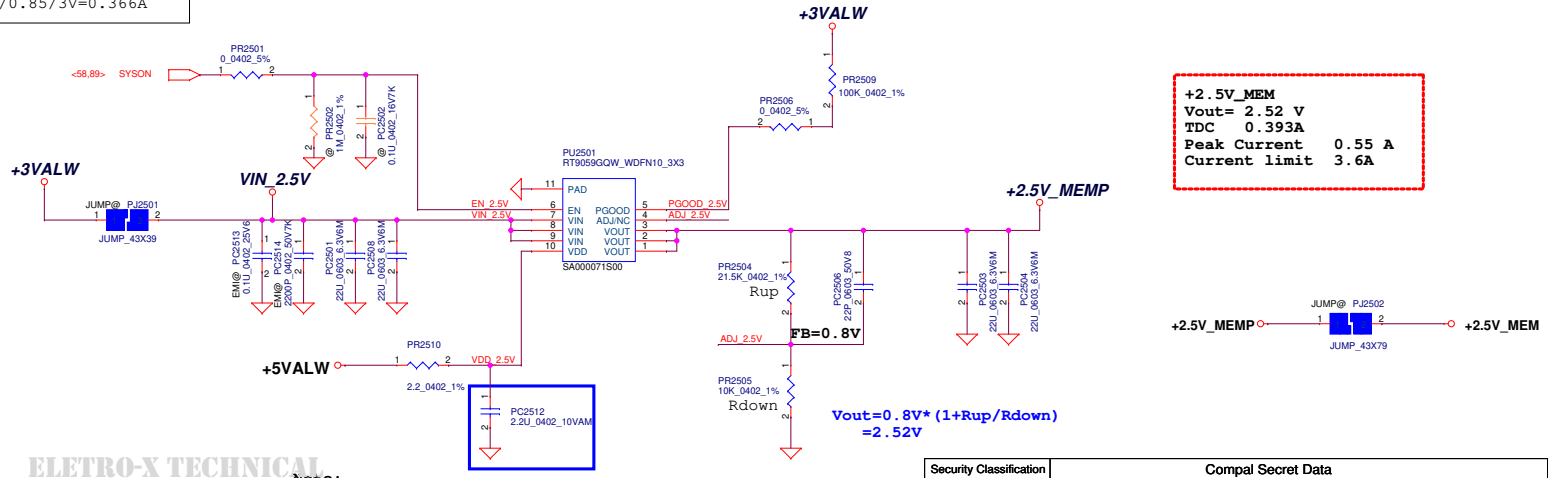
Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Input Current: 0.366A

2.52V*0.37A/0.85/3V=0.366A

+2.5V_MEM
Vout= 2.52 V
TDC 0.393A
Peak Current 0.55 A
Current limit 3.6A



Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: PWR_1.2VP/0.6VSP/+2.5V

Size: A3 | Document Number: LA-K453P | Rev: 0.1

Date: Friday, February 05, 2021 | Sheet 89 of 121

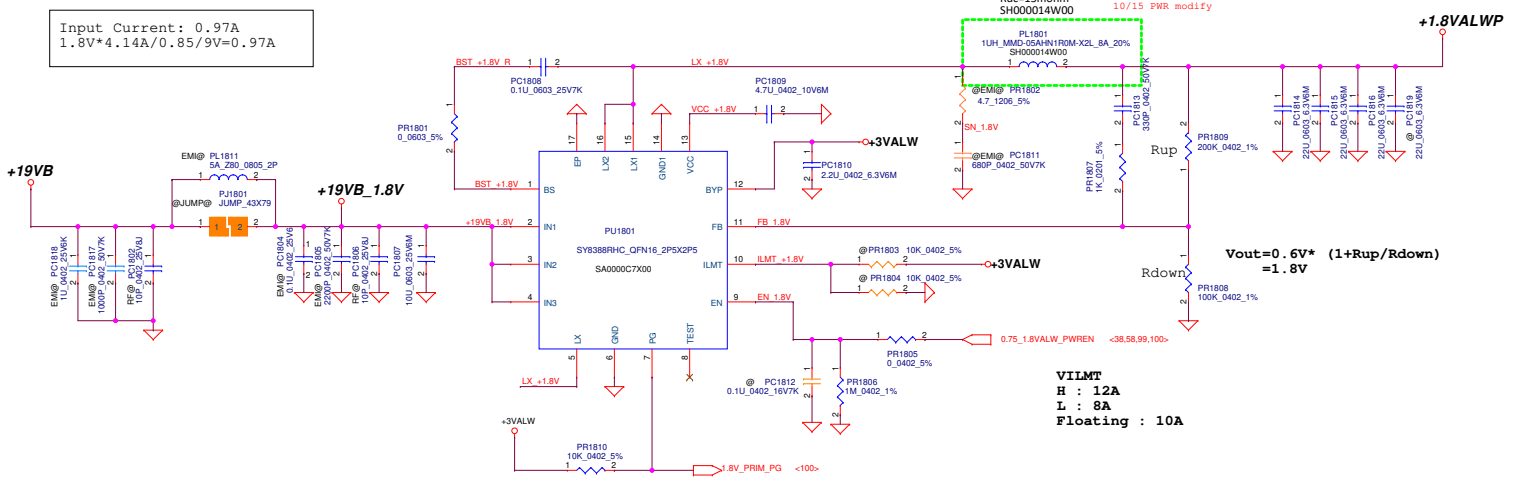
Main Func = 1.8VALWP

Input Current: 0.97A
1.8V*4.14A/0.85/9V=0.97A

Main MAG. LAYERS
Package: 5.49 x 5.18 x 2
Idc=8A, Isat=9A
Rdc=15mohm
SH000014W00

10/15 PWR modify

+1.8VALW_GPU
IDC 7.1A
Peak Current 8.1A
Current limit 10A
OVP=2.106V~2.214V(117%~123%)
UVP=0.99V~1.17V(55%~65%)
FSW= 500K Hz



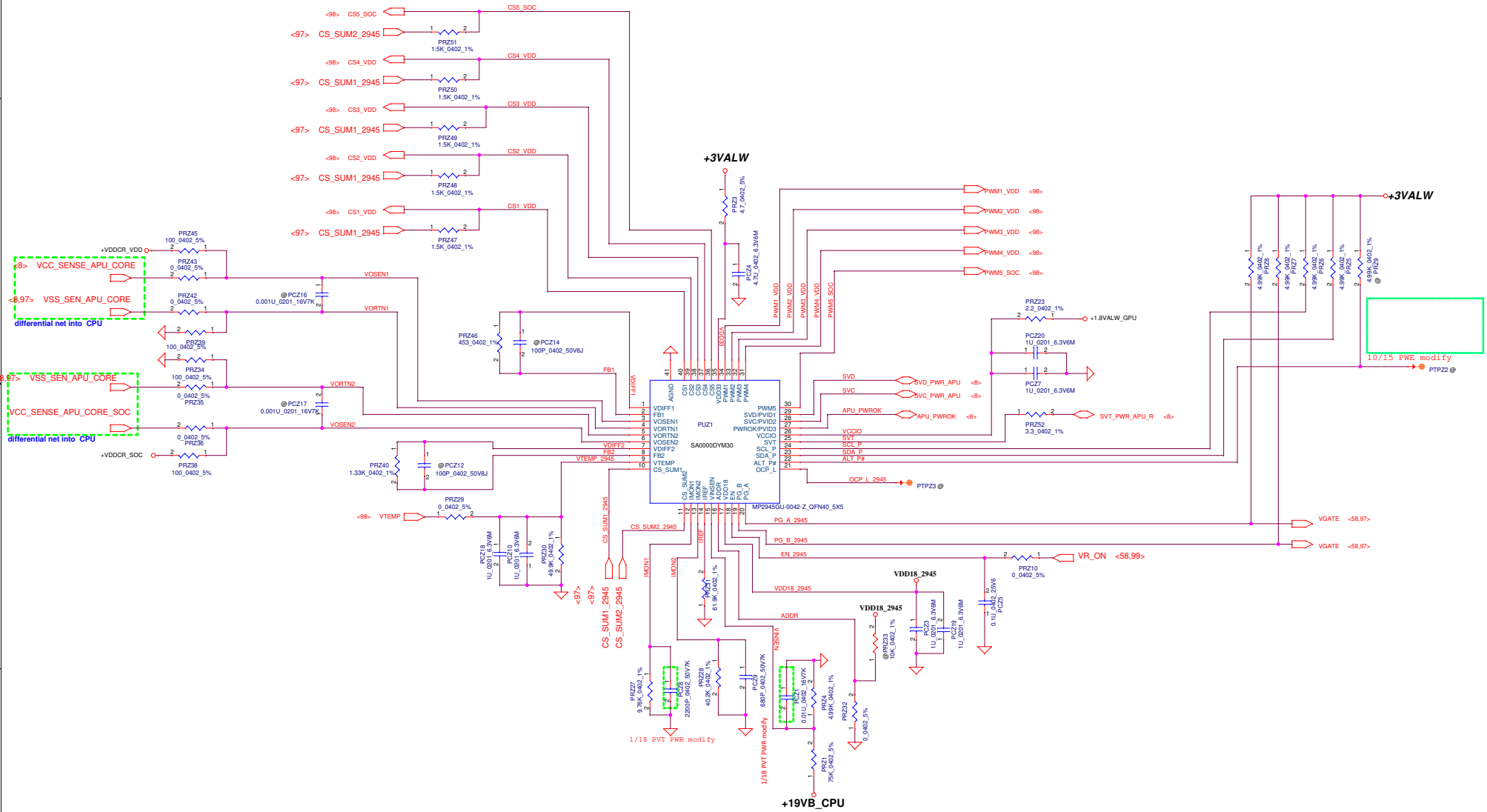
VILMT
H : 12A
L : 8A
Floating : 10A

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2021/08/01	Title: PWR-+1.8V
			Size / Document Number: LA-K453P
			Rev: 0.1
			Date: Friday, February 05, 2021 Sheet 90 of 121

Main Func = VDDCR_VDD / VDDCR_SOC

VDDCR_VDD
Fsw = 750kHz
TDC=58A
EDP(Iccmax) = 110A
OCP = 153A

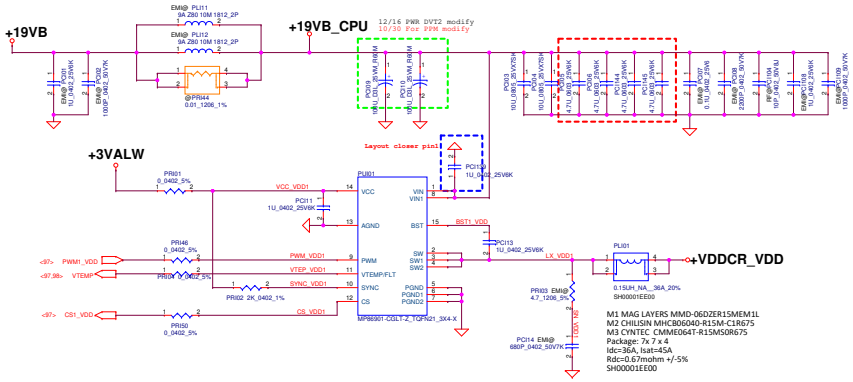
VDDCR_SOC
Fsw = 750kHz
TDC= 15A
EDP(Iccmax) = 20A
OCP = 38A

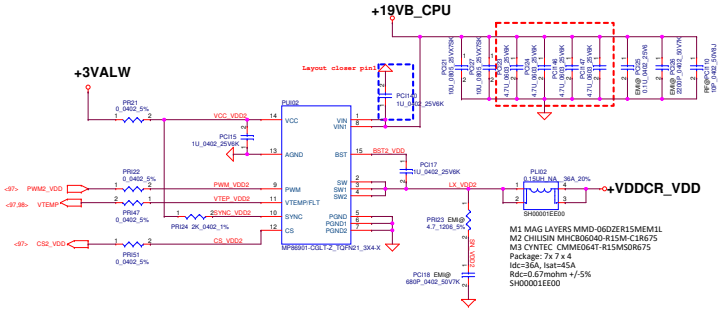


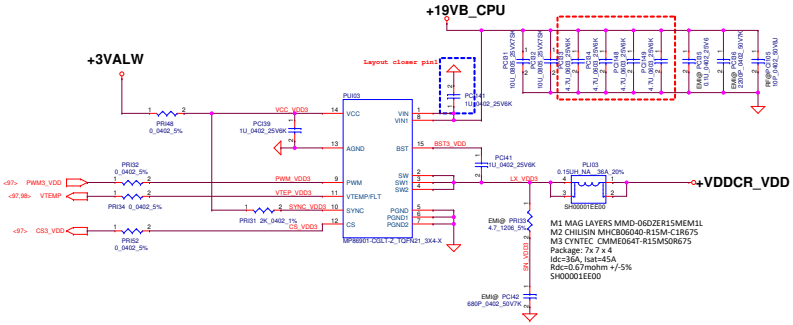
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2017/01/06	Title +VCORE_MP2945
Size	Document Number LA-K453P		Rev 1.1
Date: Friday, February 05, 2021	Sheet 97 of 121		

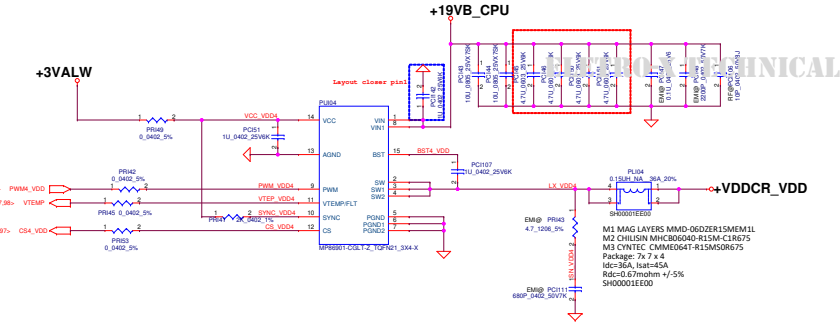
Main Func = CPU_CORE_SW

+VDDCR_VDD
TDC= 58A
EDP= Peak Current 110A

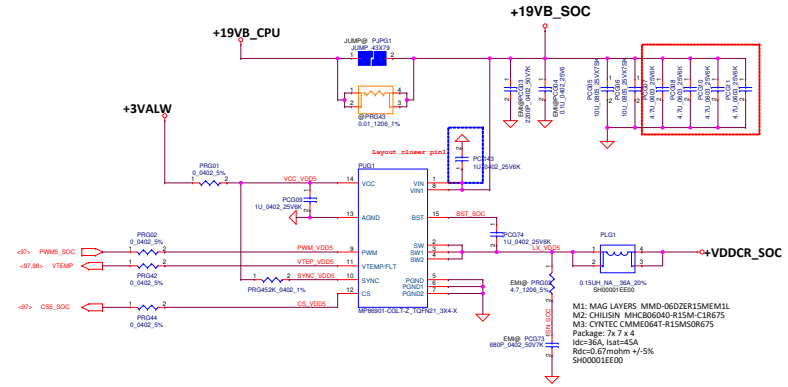








+VDDCR_SOC
TDC= 15 A
EDP= Peak Current 20 A



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date	2017/01/06
Title	PWR +VCC_CORE		
Size	Document Number		Rev
	LA-K453P		0.1
Date:	Friday, February 05, 2021	Sheet	95 of 121

Main Func = CPU_+0.75V_VDDP

Input Current : 0.49A
Input Peak Current : 1.2A

[AMD]:
+VDDCR_VDD
22uF_0603 X 2

[SGY]
+VDDP
470uF_ D2 x1
22uF_0603 X 6
0.1uF_0201 x1

+0.75VALW
Vout = 0.753V
TDC = 2A

OCP current = 6A
OVP = 0.904V (120% Type)
UVP = 0.452V (60% Type)
Fsw = 500KHz
Delta IL = 1.44A

+0.75V — JUMP@ PJP752 JUMP_43X39 — +0.75VALW

COILFORCE
Package: 5.4 x 5.2 x 2.2
Idc=9A, Isat=13.2A
Rdc=12mohm
SH000021700

+19VB — +19VB_0.75V — +0.75V — +3VALW — +3VS

PUV702 SY8388RHC_QFN16_2P5X2P5 SA0000C7X00

VILMT
H : 12A
L : 8A
Floating : 10A

Vout=0.6V* (1+Rup/Rdown)
=0.753V

<58,97,99> VR_ON

Sensing nets uses differential mode to connect

APU_VDDP_SEN_H <8>
APU_VDDP_SEN_L <8,99>

10/9 PWR modify

[AMD]:
+VDDCR_VDD
22uF_0603 X 2

[SGY]
+VDDP
470uF_ D2 x1
22uF_0603 X 6
0.1uF_0201 x1

+0.75VS
Vout = 0.753V
TDC = 2A

OCP current = 6A
OVP = 0.904V (120% Type)
UVP = 0.452V (60% Type)
Fsw = 500KHz
Delta IL = 1.44A

+0.75V_S5 — JUMP@ PJP753 JUMP_43X39 — +0.75VS

COILFORCE
Package: 5.4 x 5.2 x 2.2
Idc=9A, Isat=13.2A
Rdc=12mohm
SH000021700

+19VB — +19VB_0.75V_S5 — +0.75V_S5 — +3VALW

PUV703 SY8388RHC_QFN16_2P5X2P5 SA0000C7X00

VILMT
H : 12A
L : 8A
Floating : 10A

Vout=0.6V* (1+Rup/Rdown)
=0.753V

<58,97,99> VR_ON

Sensing nets uses differential mode to connect

VDDP_SENSE <8>
APU_VDDP_SEN_L <8,99>

10/9 PWR modify

<58,76> 0.75VS_PWR_EN

9/21 EE modify

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date	2017/01/06
Title	PWR +0.75V PRIM		
Size	Document Number		Rev
	LA-K453P		0.1
Date:	Friday, February 05, 2021	Sheet	99 of 121

Main Func = CPU_VDD_18

[AMD]
+VDDCR_VDD
22uF_0603 X 4

[SGY]
+VDD_18
470uF_ D2 x1
22uF_0603 X 5
0.1uF_ 0201x1

+1.8V_VDD
TDC 1A
Current limit 8A
OVP=2.106V~2.214V(117%~123%)
UVP=0.99V~1.17V(55%~65%)
FSW= 500K Hz

+VDD_18 — JUMP@ PJ1852 — +1.8V_VDD
JUMP_43X118

Input Current: 0.97A
1.8V*4.14A/0.85/9V=0.97A

Main MAG. LAYERS
Package: 5.49 x 5.18 x 2
Idc=7A, Isat=13.7A
Rdc=18.9mohm
SH00001YU00

+19VB
+19VB_+VDD_18
+VDD_18

EMI@ PL7504 5A_Z80_0805_2P
@JUMP@ PJ1851
JUMP_43X79

PC1858 0.1U_0603_25V7K
PR1851 0_0603_5%
BST_+VDD_18_R
BST_+VDD_18
LX_+VDD_18
PL1851 1UH_MMD-05AHN1R0M-X2L_8A_20%
SH00001YU00
10/9 PWR modify

PC1859 4.7U_0402_10V6M
VCC_+VDD_18
PC1860 2.2U_0402_6.3V6M
+3VALW

@EMI@ PR1852 4.7_0603_5%
SN_+VDD_18
@EMI@ PC1861 680P_0402_50V7K
PC1863 330P_0402_50V7K
PR1857 1K_0201_5%

PU2502
SY8388RHC_QFN16_2P5X2P5
SA0000C7X00
BS, IN1, IN2, IN3, EP, LX2, LX1, GND1, VCC, BYP, FB, ILMT, EN, LX, GND, PG, TEST

FB_+VDD_18
ILMT_+VDD_18
EN_+VDD_18

@PR1853 10K_0402_5%
PR1854 10K_0402_5%

Rup PR1859 200K_0402_1%
Rdown PR1858 100K_0402_1%

Vout=0.6V* (1+Rup/Rdown)
=1.8V

VILMT
H : 12A
L : 8A
Floating : 10A

PR1855 120K_0402_1%
0.75_1.8VALW_PWREN <38,58,90,99>

PC1862 0.1U_0402_16V7K
PR1856 1M_0402_1%

9/21 EE modify

VILMT
H : 12A
L : 8A
Floating : 10A

PR1860 10K_0402_5%
1.8V_PRIM_PG <90>

EMI@ PC1874 1U_0402_25V6K
EMI@ PC1875 1000P_0402_50V7K
RF@ PC1852 10P_0402_25V8J
EMI@ PC1854 0.1U_0402_25V6
PC1855 2200P_0402_50V7K
RF@ PC1856 10P_0402_25V8J
PC1857 10U_0603_25V6M

PC1864 @ 22U_0603_6.3V6M
PC1865 22U_0603_6.3V6M
PC1866 22U_0603_6.3V6M
PC1873 0.1U_0201_10V6K
PC1868 22U_0603_6.3V6M
PC1867 @ 22U_0603_6.3V6M

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: PWR_+VPP

Document Number: LA-K453P

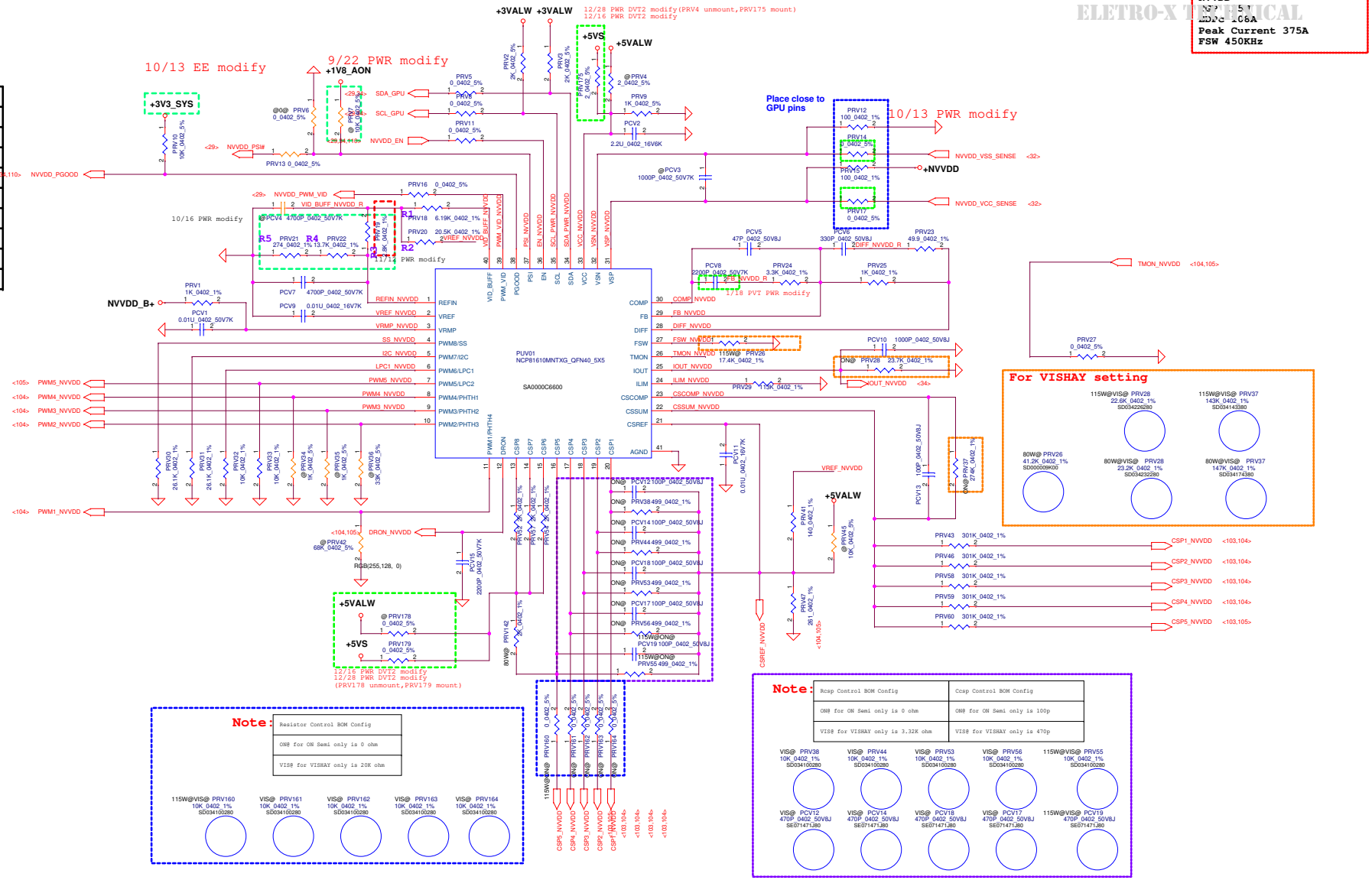
Rev: 0.1

Date: Friday, February 05, 2021 Sheet 100 of 121

Main Func = VGA CORE

Config	GN20
Vmin	0.597
Vmax	0.843
Vboot	0.75
R1	6.19K
R2	20.5K
R3	2.8K
R4	13.7K
R5	274
C	4.7n

NVVDD
[illegible] 5V
DDRC 106A
Peak Current 375A
FSW 450KHz



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2020/04/19

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Compal Electronics, Inc.

Title: PWR_VGA_NCP81610MNTXG

Size: C | Document Number: LA-K453P | Rev: 0.1

Date: Friday, February 05, 2021 | Sheet 103 of 121

Main Func = GPU_CORE SW(1-4PH)

20201016 Modify

Note:

MOS Control BOM Config
ON@ for ON Semi MOS only
VISHAY@ for VISHAY MOS only

VIS@ PUV2 SIC850EED SA000050Z00 | VIS@ PUV3 SIC850EED SA000050Z00 | VIS@ PUV4 SIC850EED SA000050Z00 | VIS@ PUV5 SIC850EED SA000050Z00

+19VB — EMI@ PLV11 5A_Z90_0805_2P | EMI@ PLV12 5A_Z90_0805_2P | EMI@ PLV13 5A_Z90_0805_2P → GPU_B+

PRV81 0.005_2512_1% → NVVDD_B+

PRV82 0.005_2512_1% → FBVDD_B+

PRV88 10_0402_1%

Close to controller (PUV1) pin3

NVVDD
TGP 115W
EDPc 108A
Peak Current 375A

Use 0805 size

Main: MAG LAYERS
Package: 13.1 x 8.1 x 4
Idc=45A, Isat=77A
Rdc=0.48mohm +/-5%
SH00001QL00

1/28 PWR PVT modify

10/13 For PWR modify

10/30 For PPM modify

12/16 PWR DVT2 modify

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2020/04/19

Compal Electronics, Inc.

Title: PWR_VGA_NCP30315

Size: Document Number: LA-K453P — Rev: 0.1

Date: Friday, February 05, 2021 — Sheet 104 of 121

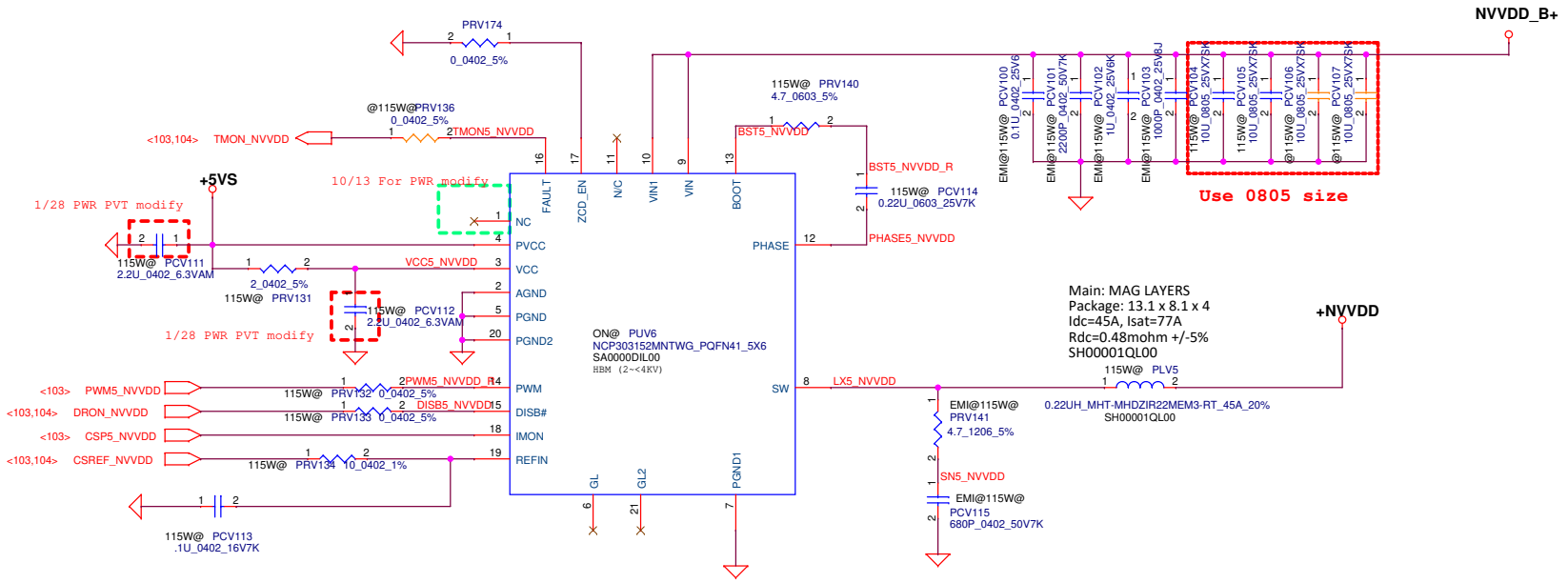
Main Func = GPU_CORE SW(5PH)

20201016 Modify

Note:

MOS Control BOM Config
ON@ for ON Semi MOS only
AOS@ for AOS MOS only

115W@VIS@
PUV6
SCI830ED
SA0000E0Z00



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.

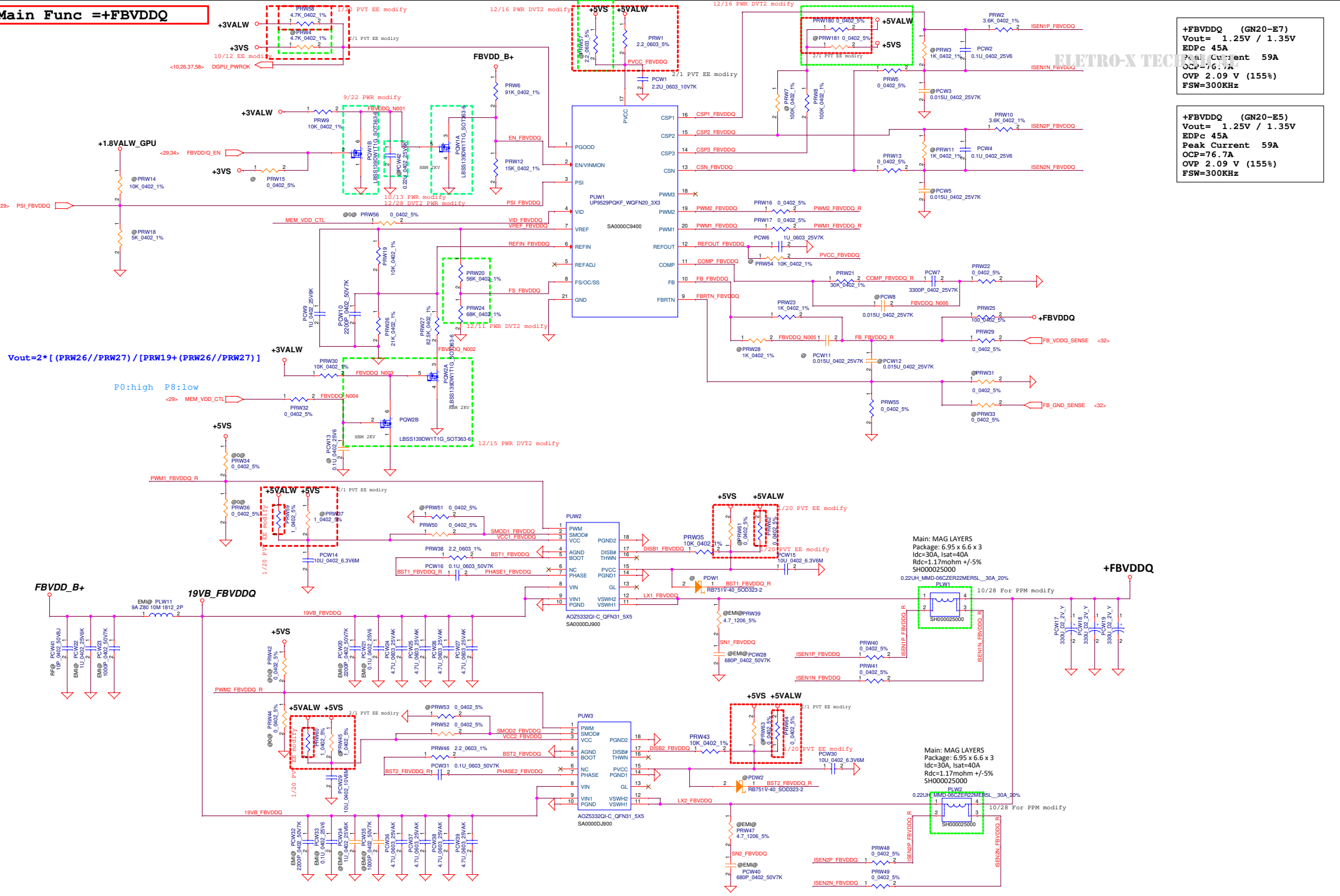
Title: PWR- Reserve for PWR

Document Number: LA-K453P

Rev: 0.1

Date: Friday, February 05, 2021 Sheet 105 of 121

Main Func =+FBVDDQ



BOM config	GPU type	VRAM memory	VRAM vender	RVL	PRW30	PRW31
	GN20			1.25V	16.9K	
				1.2V	16.9K	133K

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2020/04/19

Compal Electronics, Inc.

Title: **PWR +1.35VRAM**

Size: Document Number: **LA-K453P** Rev: 0.1

Date: Friday, February 05, 2021 Sheet 108 of 121

Main Func =+0.95VS_VGAP

Input Current: 0.974A
0.954V*2.604A/0.85/3V=0.974A

+PEX_VDD
TDC 3.85A
Peak Current 5.5A
OCP Current 8A
Fsw = 500KHz

JUMP@ PJPF02
+0.95VS_VGAP — 1 — 2 — +PEX_VDD
JUMP_43X79

Main MAG. LAYERS
Package: 5.49 x 5.18 x 2
Idc=7A, Isat=13.7A
Rdc=18.9mohm
SH00001YU00

PLF1
1UH_MMD-05BZ-1R0M-M2L_7A_20%
SH00001YU00

9/21 PWR modify

+0.95VS_VGAP

10/9 PWR ADD

+19VB

EMI@ PLF3
5A_Z80_0805_2P

@JUMP@ PJPF01
JUMP_43X39

VIN_0.95VS_VGAP

PCF14
0.1U_0603_25V7K

BS2_0.95VS_VGAP

LX_0.95VS_VGAP

PRF1
0_0603_5%

BS_0.95VS_VGAP

VIN_0.95VS_VGAP

PCF15
4.7U_0402_10V6M

VCC_0.95VS_VGAP

+3VALW

PCF16
2.2U_0402_6.3V6M

PUF2
SY8388RHC_QFN16_2P5X2P5
SA0000C7X00

BS
IN1
IN2
IN3
EP
LX2
LX1
GND1
VCC
BYP
FB
ILMT
EN
LX
GND
PG
TEST

FB_0.95VS_VGAP

ILIM_0.95VS_VGAP

@EMI@ PRF5
4.7_0603_5%

SN_0.95VS_VGAP

@EMI@ PCF5
680P_0402_50V7K

PCF6
330P_0402_50V7K

PRF8
1K_0201_5%

PRF6
42.2K_0201_1%

Rup

PRF7
71.5K_0201_1%

Rdown

Vout=0.6V* (1+Rup/Rdown)=0.954V

@PRF12 10K_0402_5%

PRF13 10K_0402_5%

+3VALW

VILMT
H : 12A
L : 8A
Floating : 10A

PCF2 22U_0603_6.3V6M
PCF3 22U_0603_6.3V6M
PCF7 22U_0603_6.3V6M
PCF17 22U_0603_6.3V6M

RF@ PCF8 10P_0402_25V8J
EMI@ PCF9 1000P_0402_50V7K
EMI@PCF10 1U_0402_25VAK

EMI@ PCF11 0.1U_0402_25V7K
EMI@ PCF12 220P_0402_50V7K
PCF13 10P_0402_25V8J
RF@ PCF1 10U_0603_25V6M

9/21 PWR modify

LX_0.95VS_VGAP

PG_0.95VS_VGAP

9/21EE modify

+1V8_AON

PRF9
100K_0402_1%

<29> PG_0.95VS_VGAP

EN_0.95VS_VGAP

0.1U_0402_16V7K
@ PCF4
1M_0402_1%
PRF4

PRF10
0_0402_5%

PEX_VDD_ENP <29>

@0@ PRF2
0_0402_5%

NVVDD_EN <29,34,103>

@PRF3
0_0402_5%

NVVDD_PGOOD <9,26,29,34,103>

10/13 EE modify

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2021/08/01

Compal Electronics, Inc.

Title: PWR-+1.0VS_VGAP

Size: B | Document Number: LA-K453P | Rev: 0.1

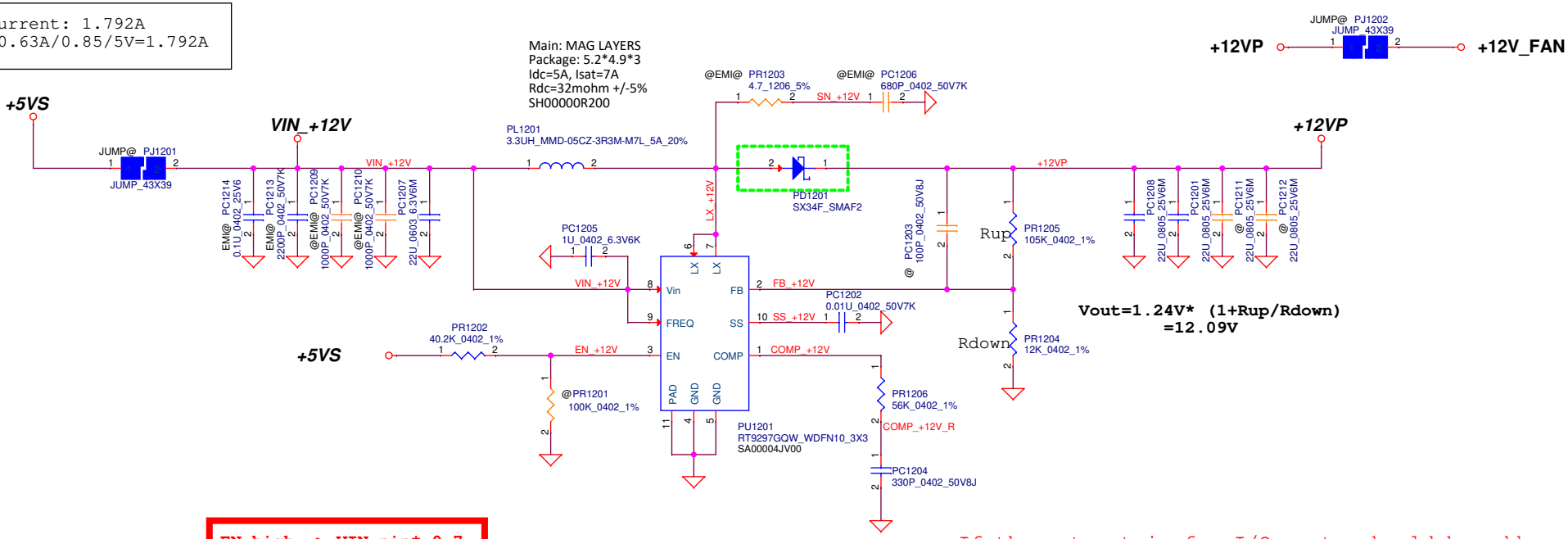
Date: Friday, February 05, 2021 | Sheet 110 of 121

Main Func =+12VP_FAN

+12V_FAN
Vout = 12.09 V
IDC 0.63A
Peak Current 0.9A
Input Current limit 3A
FSW=1.24MHz

Add a switch circuit to turn off the +12V_VIN if need.

Input Current: 1.792A
12.09V*0.63A/0.85/5V=1.792A



EN high: > VIN pin* 0.7
EN Low: < VIN pin* 0.3

FREQ high : Frequency = 1.2MHz
FREQ low : Frequency = 640KHz

If the out put is for I/O port, should be add protection circuit for I/O short protection.

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/12/31

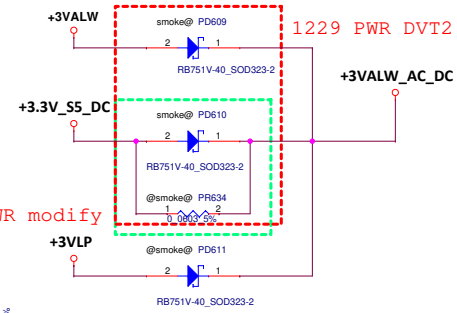
Compal Electronics, Inc.

Title: PWR_+12VP_FAN

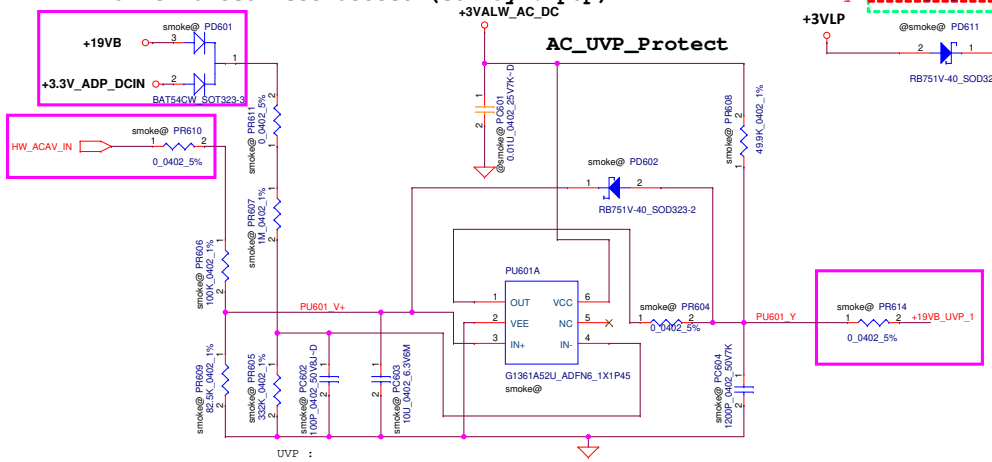
Size | Document Number: LA-K453P | Rev: 0.1

Date: Friday, February 05, 2021 | Sheet 111 of 121

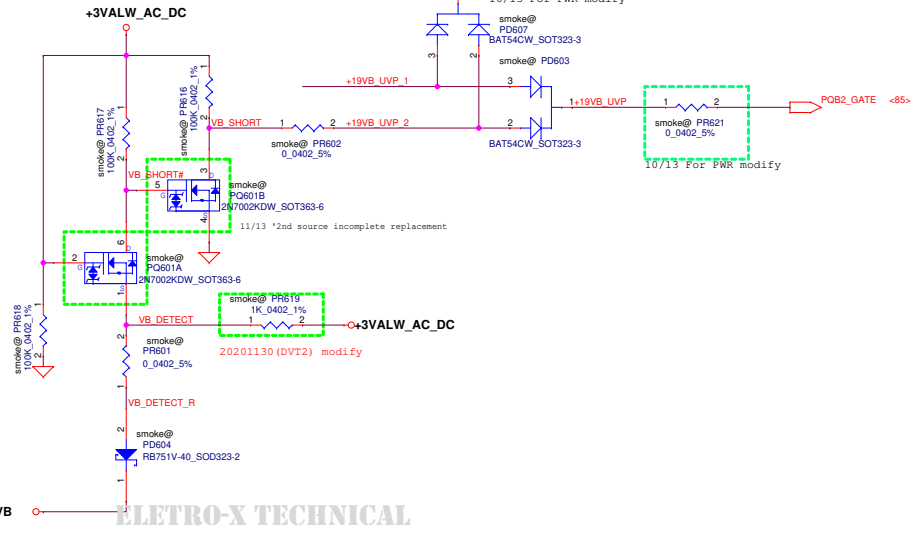
Main Func = Smokeless UVP

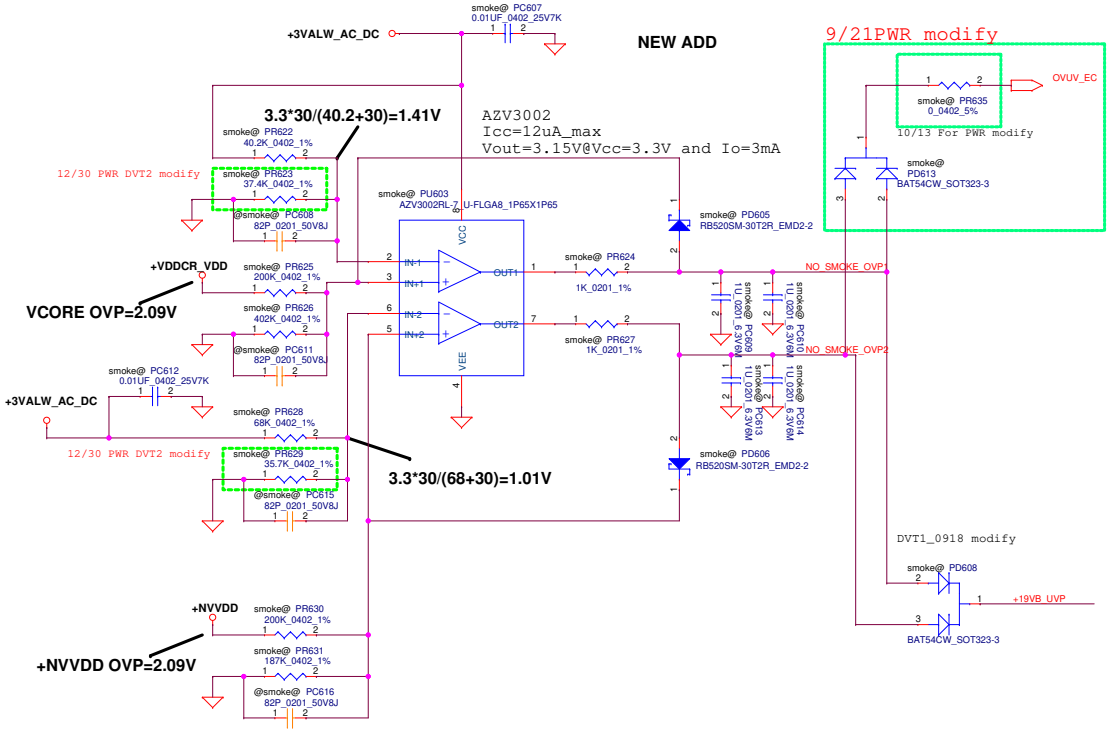


AC_UVP_Protect
Barrel disconncet detect (co-lay unpop)



UVP :
PR606 100K
PR609 82.5K
PR607 1M
PR605 332K
PC602 100P
PC603 220P
PR603 1M(depop)
PR604 0
PR608 49.9K
PC604 1200P
V+ :1.5V
V- :<1.5V when V<6V
latch V+ :1.87V
latch V- : 0.87V





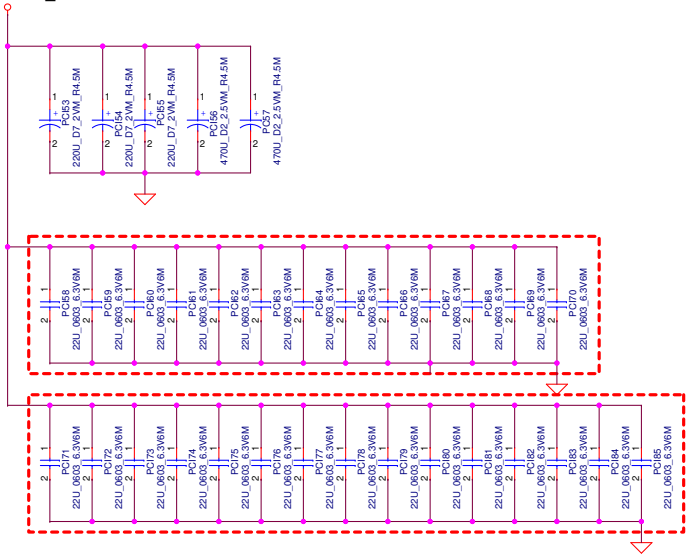
Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.			
Title: PWR- Smokeless UVP/OVP			
Size: B	Document Number: LA-K453P		Rev: 0.1
Date: Friday, February 05, 2021	Sheet 112 of 121		

[AMD]:
+VDDCR_VDD
22uF_0603 X 16

[MPS]
+VDDCR_VDD
470u_D7 x2
220uF_D2 x3
22uF_0603 X 28

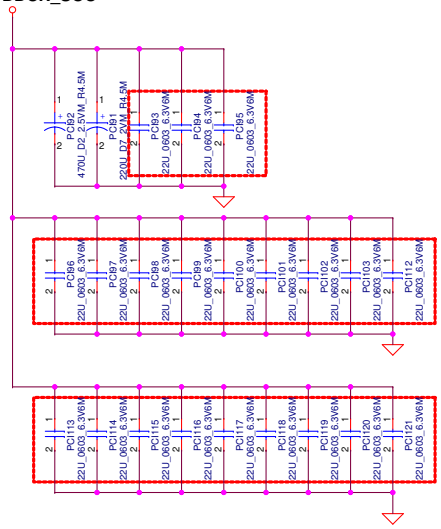
+VDDCR_VDD



[AMD]:
+VDDCR_VDD
22uF_0603 X 7

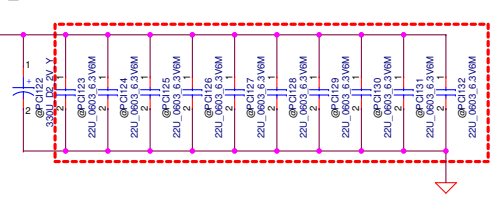
[MPS]
+VDDCR_SOC
470uF_D2 x1
220uF_D2 x1
22uF_0603 X 21

+VDDCR_SOC



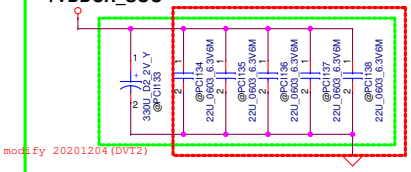
reserve:
+VDDCR_VDD
330uF_D2 x1
22uF_0603 X 10

+VDDCR_VDD



reserve:
+VDDCR_SOC
330uF_D2 x1
22uF_0603 X 5

+VDDCR_SOC



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2018/12/31	Title: PWR_CPU DECOUPLING
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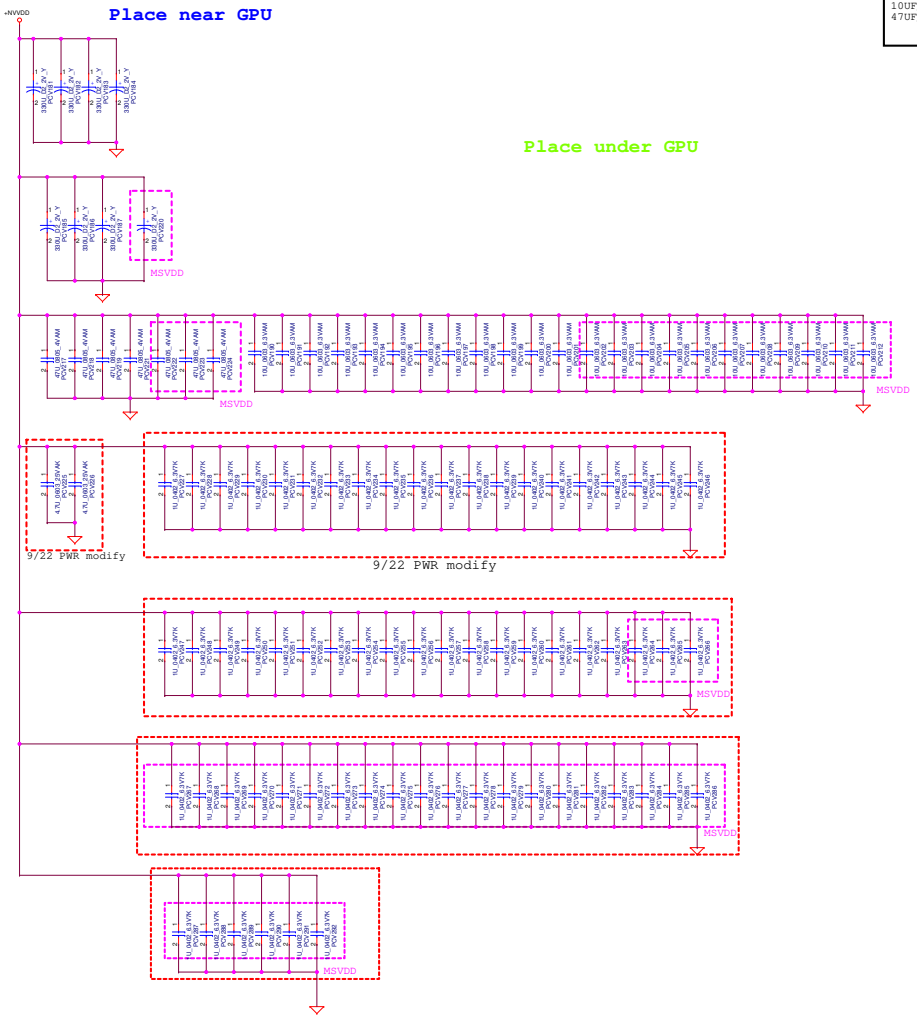
			Date: Friday, February 05, 2021 Sheet 101 of 121

Main Func = VGA CORE DECOUPLING

+NVVDD / +MSVDD
330UF X 8
1UF_0402 X 66
4.7UF_0603 X 2
10UF_0603 X 23
47UF_0805 X7

DG-09845-001_v01
+NVVDD
330UF X 3
1UF_0402 X 37
4.7UF_0603 X 2
10UF_0603 X 12
47UF_0805 X 4

+MSVDD
330UF X 1
1UF_0402 X 29
10UF_0603 X 11
47UF_0805 X 2



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2020/04/19	Title: PWR_NVVDD DECOUPLING
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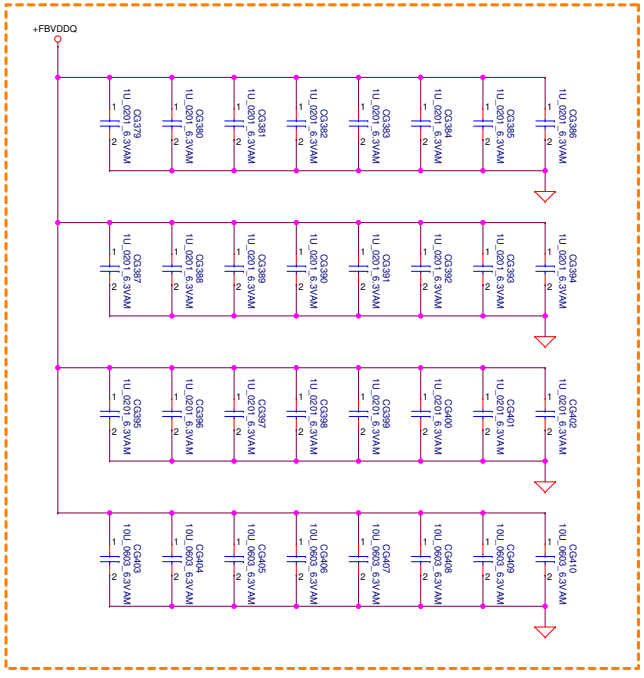
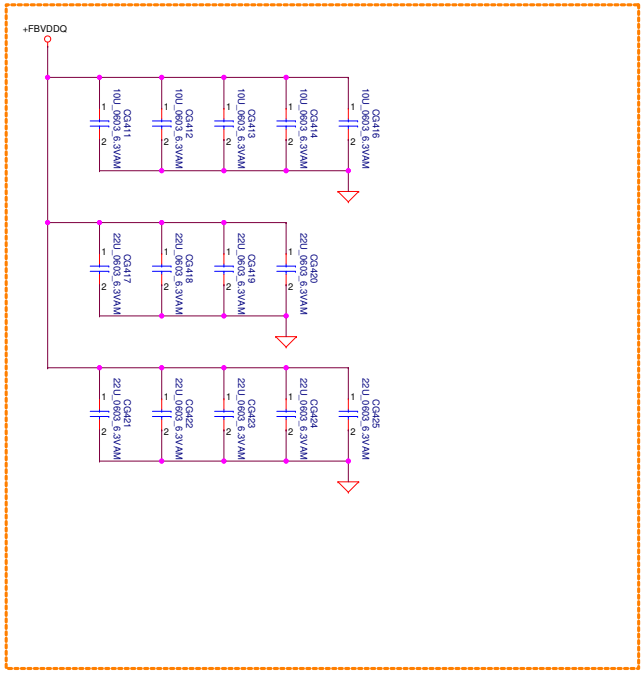
FBVDDQ_GPU

Under GPU



Near GPU



ELETRO-X TECHNICAL

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title: NV(8/8) GPU DECOUPLING			
Size: B	Document Number: LA-K453P		Rev: 0.1
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Main Function:

VRAM X76:

ZZ21 X765BG@
ALT_GROUP PARTS VRAM 6G SAM GDP53
X7691031L51

ZZ21 X76M6G@
ALT_GROUP PARTS VRAM 6G MIC GDP53
X7691031L52

ZZ21 X76H6G@
ALT_GROUP PARTS VRAM 6G HYN GDP53
X7691031L53

ZZ21 X765BG@
ALT_GROUP PARTS VRAM 8G SAM GDP53
X7691031L54

ZZ21 X76M8G@
ALT_GROUP PARTS VRAM 8G MIC GDP53
X7691031L55

ZZ21 X76H8G@
ALT_GROUP PARTS VRAM 8G HYN GDP53
X7691031L56

6G bit GDDR6

Micron 6GB SKU		Samsung 6GB SKU		Hynix 6GB SKU	
R1	R3	R1	R3	R1	R3
	UM1 VM6GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM9 VM6GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM2 VM6GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM10 VM6GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM3 VM6GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM11 VM6GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM4 VM6GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM12 VM6GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L		UM1 VS6GR3@ K4Z80325BC-HC14 1.2V SA0000C626L UM9 VS6GR3@ K4Z80325BC-HC14 1.2V SA0000C626L UM2 VS6GR3@ K4Z80325BC-HC14 1.2V SA0000C626L UM10 VS6GR3@ K4Z80325BC-HC14 1.2V SA0000C626L UM3 VS6GR3@ K4Z80325BC-HC14 1.2V SA0000C626L UM11 VS6GR3@ K4Z80325BC-HC14 1.2V SA0000C626L UM4 VS6GR3@ K4Z80325BC-HC14 1.2V SA0000C626L UM12 VS6GR3@ K4Z80325BC-HC14 1.2V SA0000C626L		UM1 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L UM9 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L UM2 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L UM10 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L UM3 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L UM11 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L UM4 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L UM12 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L

8G bit GDDR6

Micron 8GB SKU		Samsung 8GB SKU		Hynix 8GB SKU	
R1	R3	R1	R3	R1	R3
	UM1 VM8GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM9 VM8GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM2 VM8GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM10 VM8GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM3 VM8GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM11 VM8GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM4 VM8GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L UM12 VM8GR3@ MT61K256M32JE-14:A1.2V SA0000BND7L		UM1 VS8GR3@ K4Z80325BC-HC14 1.2V SA0000C626L UM9 VS8GR3@ K4Z80325BC-HC14 1.2V SA0000C626L UM2 VS8GR3@ K4Z80325BC-HC14 1.2V SA0000C626L UM10 VS8GR3@ K4Z80325BC-HC14 1.2V SA0000C626L UM3 VS8GR3@ K4Z80325BC-HC14 1.2V SA0000C626L UM11 VS8GR3@ K4Z80325BC-HC14 1.2V SA0000C626L UM4 VS8GR3@ K4Z80325BC-HC14 1.2V SA0000C626L UM12 VS8GR3@ K4Z80325BC-HC14 1.2V SA0000C626L		UM1 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L UM9 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L UM2 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L UM10 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L UM3 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L UM11 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L UM4 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L UM12 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L		UM1 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L UM9 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L UM2 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L UM10 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L UM3 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L UM11 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L UM4 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L UM12 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L

RG80 VM@ 100K +-5% 0201 SD043100380
RG83 VM@ 100K +-5% 0201 SD043100380
RG85 VM@ 100K +-5% 0201 SD043100380

RG81 VS@ 100K +-5% 0201 SD043100380
RG83 VS@ 100K +-5% 0201 SD043100380
RG85 VS@ 100K +-5% 0201 SD043100380

RG81 VH@ 100K +-5% 0201 SD043100380
RG82 VH@ 100K +-5% 0201 SD043100380
RG85 VH@ 100K +-5% 0201 SD043100380

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Issued Date	2020/03/05	Deciphered Date 2019/04/01	Title RSV
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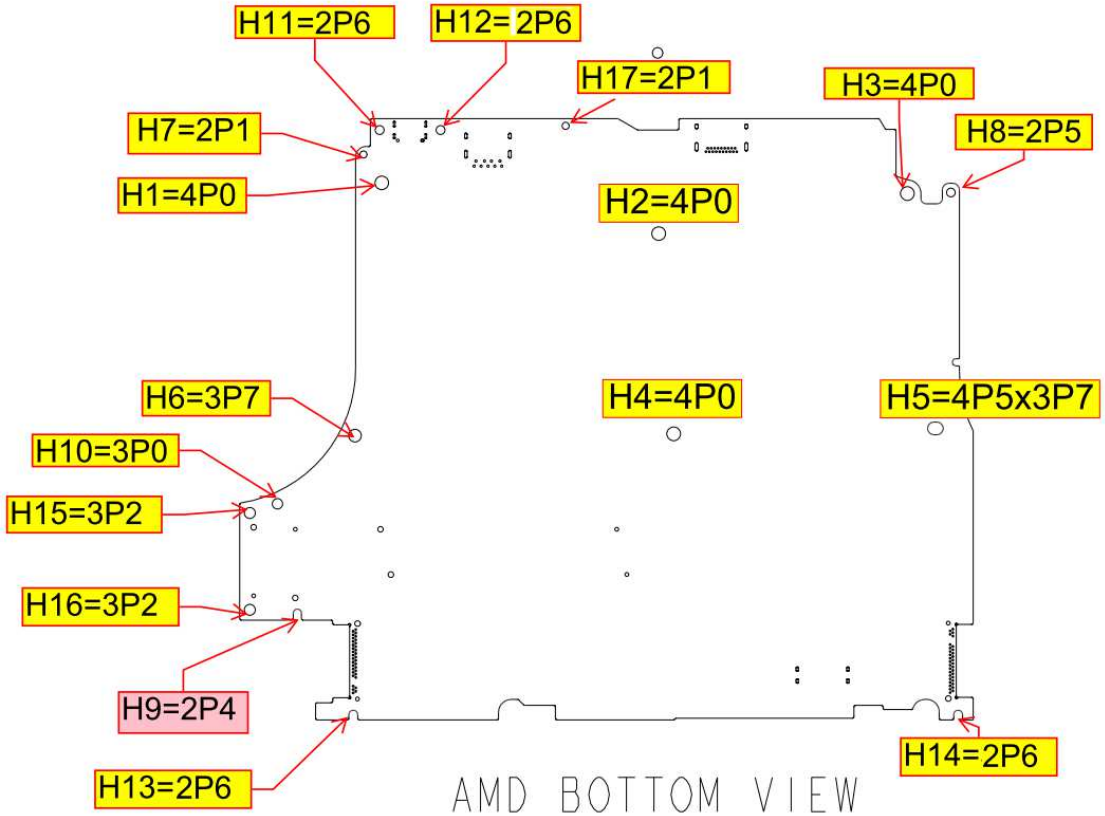

CPU & GPU

12/14 DVT2 add H17

H1 H_4P0-G
H2 H_4P0-G
H3 H_4P0-G
H4 H_4P0-G
H17 H_2P1N
H5 H_4P5X3P7-G
H6 H_3P7-G

PTH

H7 H_2P1-G
H8 H_2P5-G
H9 H_2P4-G
H10 H_3P0-G
H11 H_2P6-G
H12 H_2P6-G
H13 H_2P6-G
H14 H_2P6-G

Stand-off

H15 H_3P3-G
H16 H_3P3-G

Fiducial Mark

FD1 @FIDUCIAL
FD2 @FIDUCIAL
FD3 @FIDUCIAL
FD4 @FIDUCIAL
FD5 @FIDUCIAL
FD6 @FIDUCIAL
FD7 @FIDUCIAL

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date	2018/02/05	Title: Screw Hole
				Document Number: LA-K453P
				Rev: 0.1
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
29	103	PWR_GPU_CORE IC	10/16	PWR	1.GPU +NVVDD VBOOT setting	1.PRV19 change SD00000J280 to SD034280280 2.PRV22 change SD034165280 to SD034137280. 2.PRV21 change SD000017700 to SD034274080.	X01
30	103	PWR_GPU_CORE IC	10/16	PWR	1.GPU +NVVDD Dr.MOS 2nd source Bom control setting	1.PUV2,PUV3,PUV4,PUV5,PUV6	X01
31	82	PWR_DCIN / BATT CONN / OTP	10/17	EE	1.EE request 'Sequence modify'	1.Net:+3.3V_ADP_DCIN change to +3VLP	X01
32	108	PWR_GPU_VRAM	10/28	PWR	1.meet thremal module high	1.PLW1,PLW2 change from SH00001G400 to SH000025000.	X01
33	85	PWR_CHARGER(ISL95522A)	10/28	PWR	1.2nd source incomplete replacement	1.PDB2 SCS00008E00 change to SCS00001200	X01
34	112	PWR_Smokeless UVP/OVP	10/28	PWR	1.2nd source incomplete replacement	1.PQ601 SB00000PV00 change to SB00000EO00	X01
35	85	PWR_CHARGER(ISL95522A)	10/28	PWR	1.Adaptor CP setting	1.PRB16 change from 75K change to 200K	X01
36	85	PWR_CHARGER(ISL95522A)	10/30	PWR	1.PPM inform main source (SB00001PI00) shortage_ 2nd source change to main	1.PQB5 SB00001PI00 change to SB000011K00	X01
37	98,104	PWR_CPU_CORE_SW PWR_GPU_CORE SW(NCP303152)	10/30	PWR	1.material shortage	1.PCI09,PCI10,PCV43,PCV43,PCV55 SGA0000C300 change toSGA0000EP00	X01
38	85	PWR_CHARGER(ISL95522A)	10/30	PWR	1.reduce inrush	1.PCB12 0.1U change to 0.022U and pop.	X01
39	82	PWR_DCIN / BATT CONN / OTP	11/6	PWR	1.ME requirements	1.PJPDC1 swap.	X02
40	85	PWR_CHARGER(ISL95522A)	11/19	PWR	1.Corrosion issues	1.PLB11 change from SH00000YE00 to SH00000PJ00	X02
41	87	PWR_+3VALWP/+5VALWP	11/19	PWR	1.Corrosion issues	1.PL501 change from SH00001ST00 to SH00001TW00	X02
42	103	PWR_GPU_CORE IC	11/19	PWR	1.GPU +NVVDD VBOOT setting	1.PRV19 change SD00000J280 to SD034280180 2.PRV22 change SD034165280 to SD034137280. 2.PRV21 change SD000017700 to SD034274080.	X02
43	82	PWR_DCIN / BATT CONN / OTP	11/30	PWR	1.Flashing yellow light issue	1.PR12 SD000011M00 change to SD034100480 PR40 SD043100180 change to SD043000080	X02
44	112	PWR_Smokeless UVP/OVP	11/30	PWR	1.pre charge time	1.PR619 SD034100280 change to SD034100180	X02
45	108	PWR_GPU_VRAM	12/11	PWR	1.Run NV diag fail	NV change VRAM Spec EDPc from 26A to 45A EDPp from 41A to 59A need change the resistor setting	X02
46	108	PWR_GPU_VRAM	12/15	PWR	1.Materials EOL	PQW2 change from SB00000EO00 to SB00001FN00	X02
47	108	PWR_GPU_VRAM	12/16	PWR	1.預留Pull high to +5VS power consumption	resever PRW57,PRW180,PRW181	X02
48	103	PWR_GPU_CORE IC	12/16	PWR	1.預留Pull high to +5VS power consumption	resever PRV175,PRW179,PRV179	X02
49	103	PWR_CPU_CORE_SW PWR_GPU_CORE SW(NCP303152)	12/16	PWR	1.material shortage	1.PCI09,PCI10,PCV42,PCV43,PCV55 change from SGA0000EP00 to SGA0000C300	X02
50	85	PWR_CHARGER(ISL95522A)	12/21	PWR	1.Bom change	1.PRB29、PCB31 unmount. PRB28 mount.	X02
51	108	PWR_GPU_VRAM	12/28	PWR	廠商分析有加此電容放電時較慢介於0.1-0.4之間, PWM會再打有機會造成risk	PCW42 unmount	X02
52	85	NVVDD	12/28	PWR	vendor suggest IC, Dr.MOS the same power net	PRV176,PRV178 mount, PRV4,PRV177 unmount	X02
53	85	PWR_CPU_CORE_SW PWR_GPU_CORE SW(NCP303152)	12/28	PWR	material shortage	PPM inform SGA0000EP00 shortage_change main/2nd/3rd change SGA0000C300 / SGA0000E000/SGA0000EP00	X02
54	112	PWR_Smokeless UVP/OVP	12/29	PWR	auto shutsown when run AC power cycling with battery	PD609,PD610 unmount, PR633 mount PR623 change SD034300280 to SD034374280 PR629 change SD034300280 to SD000007D00	X02

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	99	PWR_CPU_+0.75V_VDDP	9/21	EE	1.EE request 'naming rule'	1.0.75VS_PWR_EN# change to 0.75VS_PWR_EN	X01
2	100	PWR_CPU_VDD_18	9/21	EE	1.EE request 'Sequence modify'	1. PR1855 change to 120K ohm ,PC1862 Not loaded	X01
3	103	PWR_GPU_CORE IC	9/21	EE	1.EE request 'Sequence modify'	1.PRV7 Not loaded	X01
4	108	PWR_GPU_VRAM	9/21	PWR	1.Material shortage	1.PQW1 SB00000EO00 change to SB00001FN00	X01
5	110	PWR_+0.95VS_VGAP	9/21	PWR	1.EE request 'Sequence modify'	1.Net +3VALW# change to +1V8_AON	X01
6	110	PWR_+0.95VS_VGAP	9/21	PWR	1.Solution modify	1.PUF2 SA0000C7S00 change to SA0000C7X00	X01
7	112	PWR_Smokeless UVP/OVP	9/21	PWR	1.Counterpart request 2.Reservation software notification behavior	1.PD610 Not laoded Add PR634 0_0603 ohm(SD013000080) 2.Add PD613 BAT54CW_SOT323-3(SCS00006400) Add PR635 0 ohm(SD028000080)	X01
8	97	PWR_CPU CORE IC	9/22	PWR	1.Vender suggestion is not suitable for additional test points	1.PRZ53,PRZ54 Delete	X01
9	107	PWR_GPU_CORE DECOUPLING	9/22	PWR	1.Material shortage	1.4.7U 6.3V change SE00000G300 to SE00001CJ00 1U 6.3V change SE00000WV00 to SE00001EP00	X01
10	104.105	PWR_GPU_CORE SW(NCP303152) PWR_GPU_CORE SW(5PH)	9/22	PWR	1.BOM change	1.PUV2~PUV6 NCP303150D change to NCP303152	X01
11	82	PWR_DCIN / BATT CONN / OTP	9/29	PWR	1.For Adaptor PROCHOT action speed	1.PR7 1M change to 300K PR10 100K change to 47K	X01
12	82	PWR_DCIN / BATT CONN / OTP	11/6	PWR	1.Stencil Memo modify	1.PJP601 pop	X01
13	87	PWR_+3VALWP/+5VALWP	10/7	EE	1.EE request 'Sequence modify'	1.Add PR508(SD028000080),Net:THERM_OVERT#_R	X01
14	100	PWR_CPU_VDD_18	10/9	PWR	1.Solution modify	1.PU2502 SA0000C7S00 change to SA0000C7X00	X01
15	99	PWR_+VCC_CORE	10/9	PWR	1.Solution modify	1.PUV702,PUV703 change SA0000C7S00 to SA0000C7X00	X01
16	110	PWR_+0.95VS_VGAP	10/9	PWR	1.Solution modify:Follow SY8388 solution	1.Add PCF17(SE00000M000)	X01
17	85	PWR_CHARGER(ISL95522A)	10/11	PWR	1.Vendor suggestion	1.PCB17 0.47U change to 0.22U(SE000005Z80)	X01
18	85	PWR_CHARGER(ISL95522A)	10/11	PWR	1.Vendor suggestion	1.PCB17 0.47U change to 0.22U(SE000005Z80)	X01
19	85	PWR_CHARGER(ISL95522A)	10/12	PWR	1.Charger B2B MOS 2nd source Bom control setting	1.PQB11, PQB12, PQB13, PQB14	X01
20	103	PWR_GPU_CORE IC	10/12	PWR	1.GPU 2nd source Bom control setting	1.PRV28,PRV37 2.PRV160,PRV161, PRV162, PRV163, PRV164, PCV12,PCV14, PCV17, PCV18,PCV19, PRV38, PRV44, PRV53, PRV56,PRV55	X01
21	108	PWR_GPU_VRAM	10/12	EE	1.EE request 'Sequence modify'	1.PRW4 100K change to 4.7K	X01
22	108	PWR_GPU_VRAM	10/13	PWR	1.Material shortage	1.PDB2 SCS00008E00 change to SCS00001200	X01
23	89	PWR_+1.2VP/+0.6VSP/+2.5V	10/13	PWR	1.2nd source incomplete replacement	1.PLM1 SH0000OM00 change to SH00000PJ00	X01
24	104.105	PWR_GPU_CORE SW(NCP303152) PWR_GPU_CORE SW(5PH)	10/13	PWR	1.Vendor suggestion	1.PUV2~PUV6 NC	X01
25	89	PWR_+1.2VP/+0.6VSP/+2.5V	10/13	PWR	1.Vender suggestion Change lower FW	1.PRM7 470K change to 510K	X01
26	112	PWR_Smokeless UVP/OVP	10/13	PWR	1.Reservation software notification behavior	1.PR633,PR621,PR635 POP	X01
27	90	PWR_+1.8VALWP	10/15	PWR	1.TDC modify	1.PL1801 SH00001YU00 change to SH000014W00	X01
28	103	PWR_GPU_CORE IC	10/15	PWR	1.Increase accuracy		X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
55	108	PWR_GPU_VRAM	12/30	PWR	vendor suggest IC, Dr.MOS the same power net	PRW57,PRW181 mount, PRW1,PRW180 unmount	X02
51	97,85	APU,CHARGER	01/18	PWR	Modify PCZ1,PUB1 For Dell專用料號	PCZ1(SE00001R4X0 change SE076103K80), PUB1(SA0000DTQ10 change SA0000DTQ0L)	A00
52	108	+FBVDDQ	01/21	EE	modern stanby issue	DGPU_PWROK Co-lay +3VALW PUW2 +5VS Co-lay +5VALW PRW61 mount,PRW62 unmount	A00
53	85 103 97	CHARGER GPU APU	01/19	PWR	COS (Avoid material shortage)	PCB8,PCB33,PCV8,PCZ8 change from SE075222K80 to SE074222K80.	A00
54	98	CPU_CORE_SW	01/27	PWR	material shortage	PCI05,PCI06.PCI144.PCI145,PCI23,PCI24,PCI46,PCI47,PCI33,PCI34, PCI48,PCI49,PCI45,PCI46,PCI50,PCI51 PCG08,PCG09,PCG10,PCG11(SE00001CJ00 change to SE000013880)	A00
55	101	+VCORE DECOUPLING	01/27	PWR	material shortage	PCI58-85,PCI123-132 PCI93-103,PCI112-121, PCI134-138(SE00001CA00 change to SE00000M000)	A00
56	108	GPU_VRAM	2/1	EE	modern stanby issue	+3VS change +3VALW(PRW4 unmunt,PRW58 munt) +5VS change +5VALW (PRW57,181,37,45,61,63 unmunt,PRW1,180,59,60,62,64 munt)	A00

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