SYSTEM PAGE REF.

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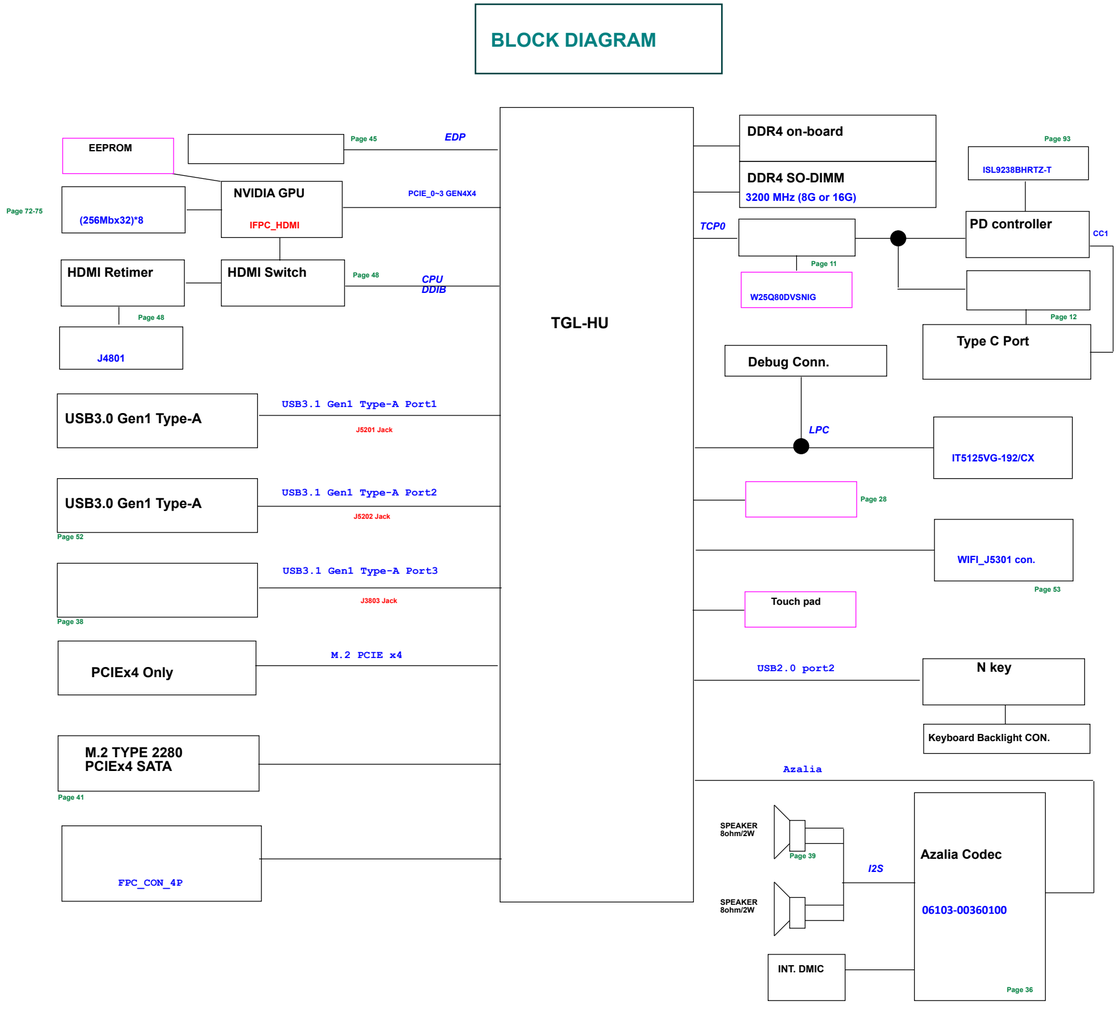
1	Block Diagram
2	System Setting
3	CPU_DMI,PEG,eDP,DDI
	CPU_DDR
5	CPU_GND
6	CPU_CFG,RSVD
7	CPU_ESPI,SPI,SMB,CLINK
	CPU_PCH_CSI2,EMMC,CNV
9	CPU_POWER
10	CPU_POWER_CAP
11	TBT_Titan Ridge SP
12	TBT_TPS65994ADType C
13	TBT
14	DIM_DDR4_ON-BOARD_A(1)
15	DIM
16	DIM_DDR4 SO-DIMM B(0) TOP
17	DIM_
18	DIM_CA/DQ Voltage
19	DDR4_TERMINATION*
20	PCH_HDA,SMBUS,SYS PWR
21	PCH-CPT(2)_PCIE,USB2,MISC
22	PCH-CPT(3)_CLK,LPC,USB3
23	
24	PCH-CPT(5)_SPI
25	PCH-CPT(6)_GPIO
26	PCH-CPT(7)_POWER,GND
27	PCH-CPT(8)_POWER,GND
28	PCH-SPI ROM,OTH
30	KBC_IT8995
31	EC_KB_TP
36	AUD-ALC3288
38	Audio_Jack
39	
40	Card Reader AU6465
44	BUG_Debug
45	CRT_LCD Panel_CMOS_DMIC
48	HDMI
51	NGFF_SSD
52	USB Port
53	USB 3.0 MB Type-C
54	G-sensor
56	LED_Indicator
57	DSG_Discharge
58	PRO_PROTECT
60	DC_DC BAT Conn.
62	ME_Conn Skew Hole
63	EMI_RF Reserve
64	U3_B2B CONN
66	WLANBT SIP
67	LID_Switch / FAN_connector
71	GPU MEMORY Interface
72	Frame Buffer
74	GPU STRAP
75	GPU GPIO
76	GPU VDD/GND
77	GPU PWG Decopling
78	GPU Power

80_PW_IMVP8 (1)
81_PW_IMVP8 (2)
83_PW_+1.0VSUS / +1.8VSUS
86_PW_1.2V/+0.6VS
87_PW_+3VADSW/+5VSUS
88_PW_LOAD SWITCH
89_PW_CHARGER(BQ24780)
90_PW_PROTECTION

94_PW_VRAM

BLOCK DIAGRAM



PW_IMVP9

+3VADSW/+5VSUS
Page 87

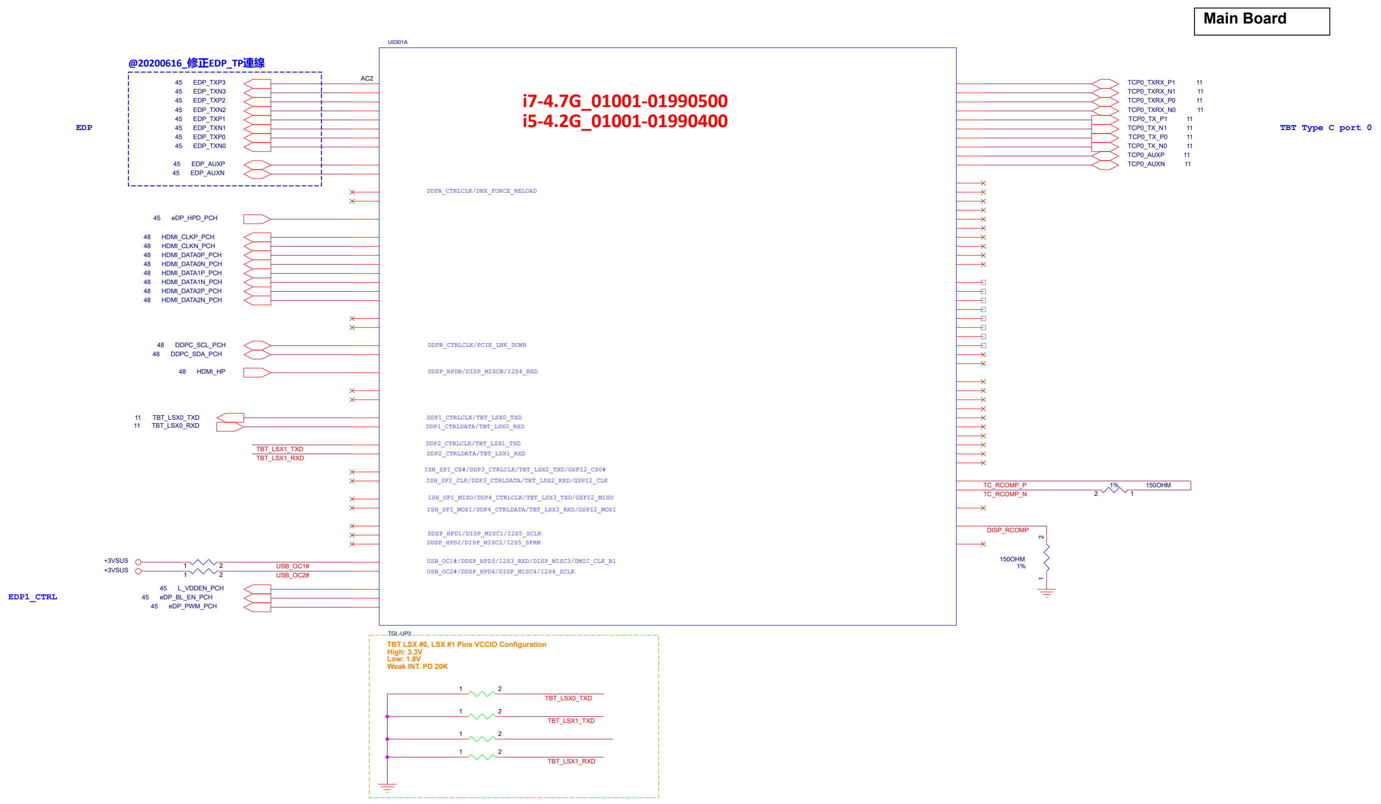
+1.8VSUS

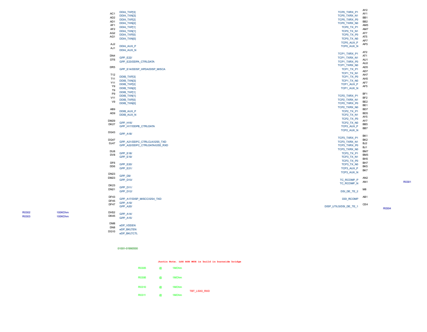
+1.1V

Page 94

Charger

Load Switch
Page 88


Main Board
U0301A
@20200616_修正EDP_TP連線
EDP
45 EDP_TXP3
45 EDP_TXN3
45 EDP_TXP2
45 EDP_TXN2
45 EDP_TXP1
45 EDP_TXN1
45 EDP_TXP0
45 EDP_TXN0
45 EDP_AUXP
45 EDP_AUXN
AC2
i7-4.7G_01001-01990500
i5-4.2G_01001-01990400
TCP0_TXRX_P1 11
TCP0_TXRX_N1 11
TCP0_TXRX_P0 11
TCP0_TXRX_N0 11
TCP0_TX_P1 11
TCP0_TX_N1 11
TCP0_TX_P0 11
TCP0_TX_N0 11
TCP0_AUXP 11
TCP0_AUXN 11
TBT Type C port 0
DDPA_CTRLCLK/DNX_FORCE_RELOAD
45 eDP_HPD_PCH
48 HDMI_CLKP_PCH
48 HDMI_CLKN_PCH
48 HDMI_DATA0P_PCH
48 HDMI_DATA0N_PCH
48 HDMI_DATA1P_PCH
48 HDMI_DATA1N_PCH
48 HDMI_DATA2P_PCH
48 HDMI_DATA2N_PCH
48 DDPC_SCL_PCH
48 DDPC_SDA_PCH
DDPB_CTRLCLK/PCIE_LNK_DOWN
48 HDMI_HP
DDSP_HPDB/DISP_MISCB/I2S4_RXD
11 TBT_LSX0_TXD
11 TBT_LSX0_RXD
DDP1_CTRLCLK/TBT_LSX0_TXD
DDP1_CTRLDATA/TBT_LSX0_RXD
TBT_LSX1_TXD
TBT_LSX1_RXD
DDP2_CTRLCLK/TBT_LSX1_TXD
DDP2_CTRLDATA/TBT_LSX1_RXD
ISH_SPI_CS#/DDP3_CTRLCLK/TBT_LSX2_TXD/GSPI2_CS0#
ISH_SPI_CLK/DDP3_CTRLDATA/TBT_LSX2_RXD/GSPI2_CLK
ISH_SPI_MISO/DDP4_CTRLCLK/TBT_LSX3_TXD/GSPI2_MISO
ISH_SPI_MOSI/DDP4_CTRLDATA/TBT_LSX3_RXD/GSPI2_MOSI
DDSP_HPD1/DISP_MISC1/I2S5_SCLK
DDSP_HPD2/DISP_MISC2/I2S5_SFRM
USB_OC1#/DDSP_HPD3/I2S3_RXD/DISP_MISC3/DMIC_CLK_B1
USB_OC2#/DDSP_HPD4/DISP_MISC4/I2S4_SCLK
TC_RCOMP_P
TC_RCOMP_N
1%
150OHM
DISP_RCOMP
150OHM
1%
+3VSUS
+3VSUS
USB_OC1#
USB_OC2#
EDP1_CTRL
45 L_VDDEN_PCH
45 eDP_BL_EN_PCH
45 eDP_PWM_PCH
TGL-UP3
TBT LSX #0, LSX #1 Pins VCCIO Configuration
High: 3.3V
Low: 1.8V
Weak INT. PD 20K
TBT_LSX0_TXD
TBT_LSX1_TXD
TBT_LSX1_RXD



MA/B_
I/O-IOMEM-S/D VDDIO_MEM_S3 (S0_1.2)_FP6 (FDS)

On board 只接一組
(Follow FP6 MPDG P53 GA502)

0_VREF_CA需在確認

Follow SCH VDD2_MEM: 1.2V

LPDDR4X COMPENSATION SIGNALS

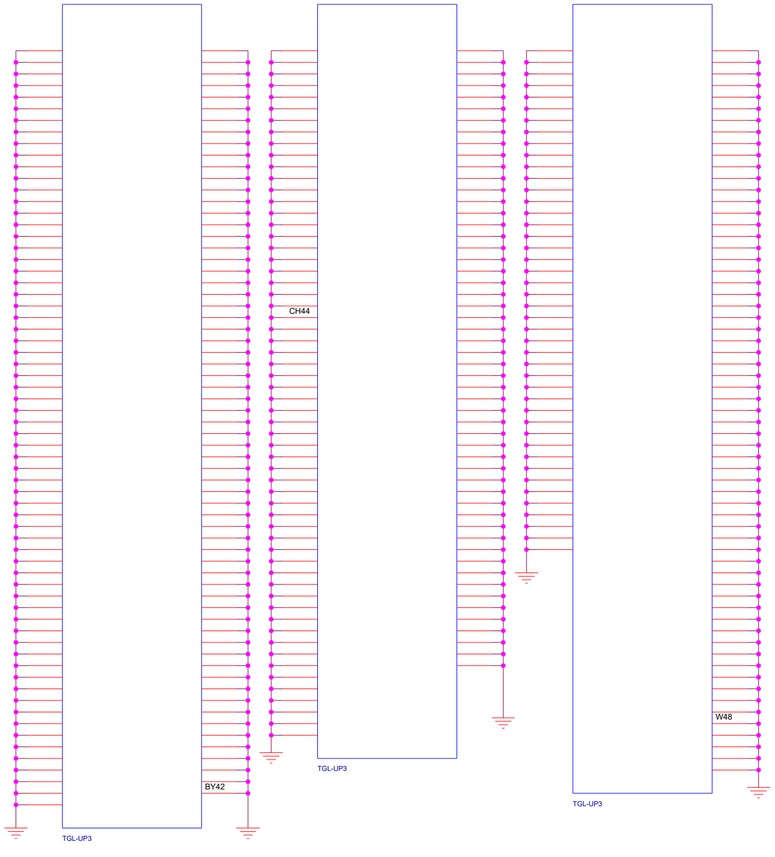
Main Board

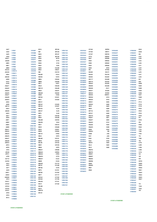
SO-DIMM DDR4

1_VREF_CA需在確認

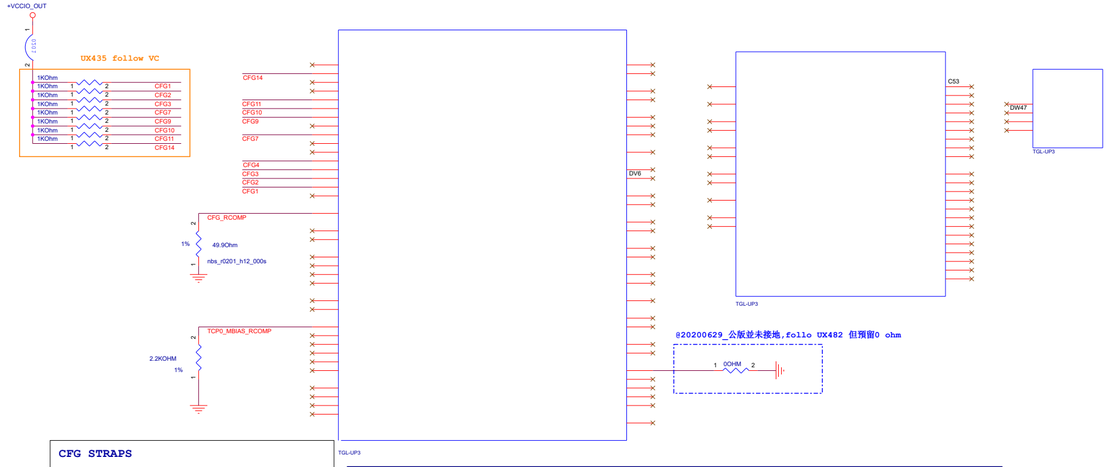
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref: Intel 570805_Coffelake_EDS_Vol_1_Rev1.5 P.116

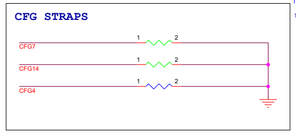
[建議用料]
1st. : LOGIC U74AUP1G07G-AL5-R 06004-00620000
2nd. : LOGIC 74AUP1G07SE-7 SOT353 06004-00051800





Main Board

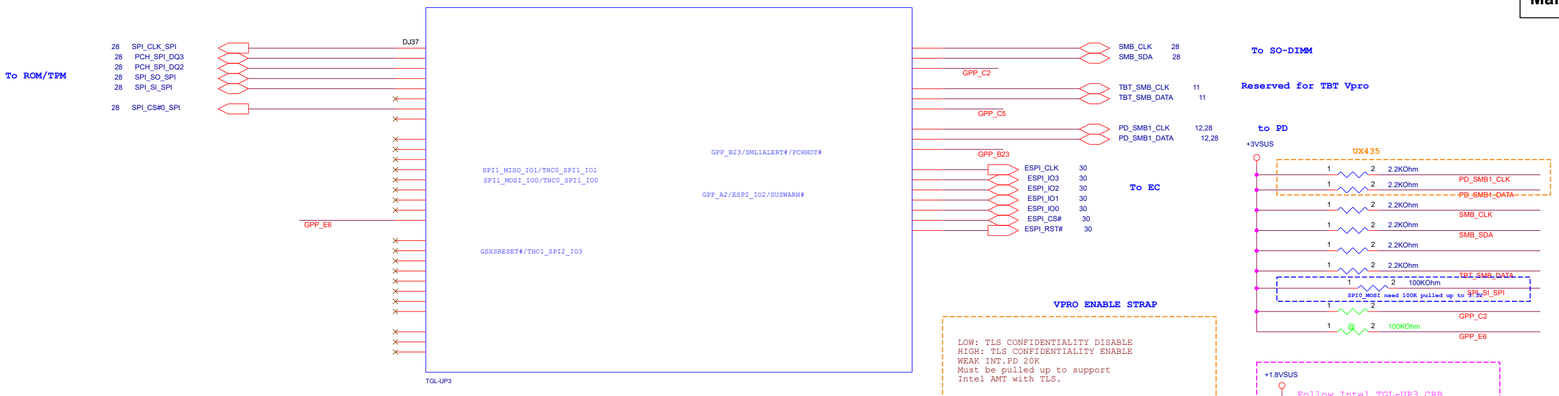




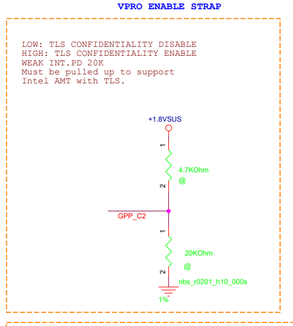
	1	0	NOTE
	DISABLE	ENABLE	eDP ENABLE

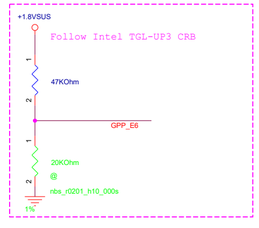
CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training - 1 = (Default) PEG Train immediately following RESET# - 0 = PEG Wait for BIOS for training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

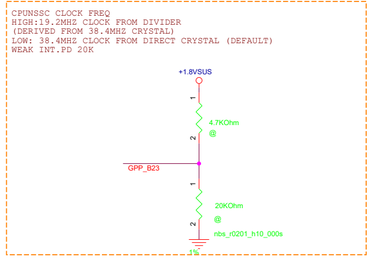
Main Board

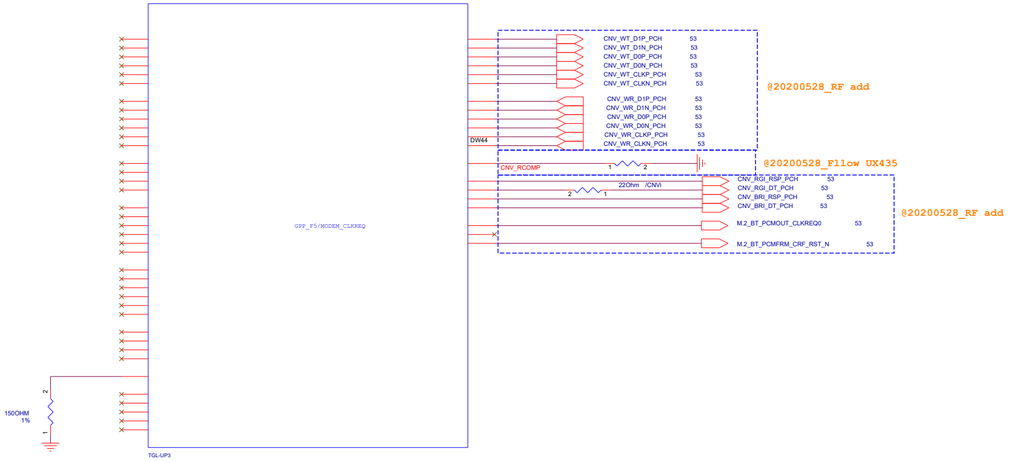


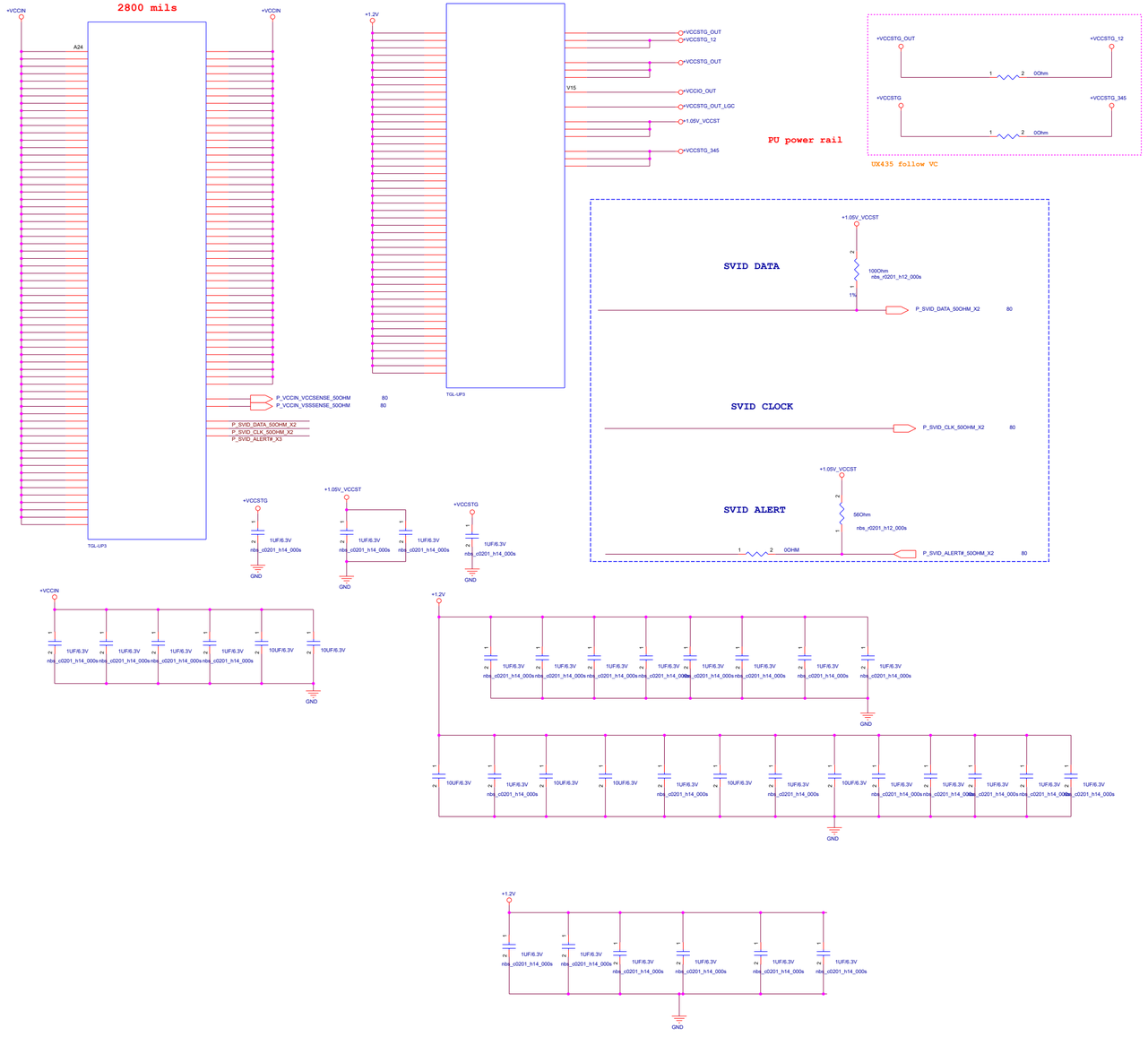
Vinafix.com

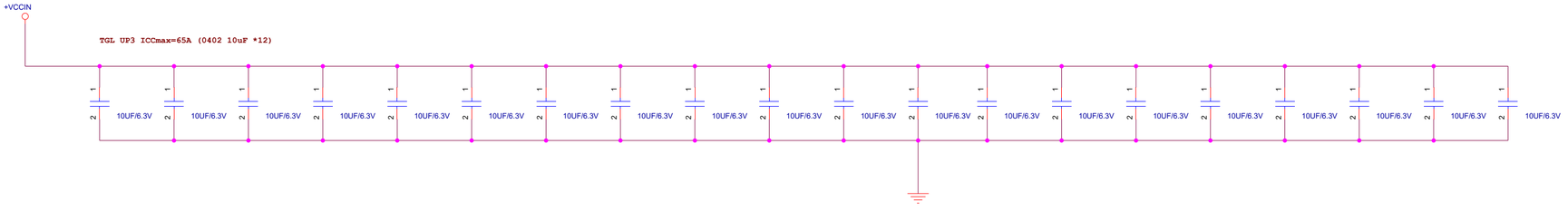




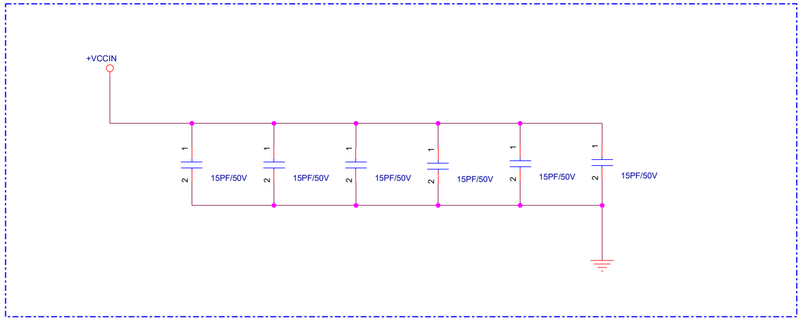



GPP_F5/MODEM_CLKREQ
150OHM
1%
TGL-UP3
CNV_WT_D1P_PCH 53
CNV_WT_D1N_PCH 53
CNV_WT_D0P_PCH 53
CNV_WT_D0N_PCH 53
CNV_WT_CLKP_PCH 53
CNV_WT_CLKN_PCH 53
CNV_WR_D1P_PCH 53
CNV_WR_D1N_PCH 53
CNV_WR_D0P_PCH 53
CNV_WR_D0N_PCH 53
CNV_WR_CLKP_PCH 53
CNV_WR_CLKN_PCH 53
DW44
@20200528_RF add
CNV_RCOMP
22Ohm /CNVi
@20200528_Fllow UX435
CNV_RGI_RSP_PCH 53
CNV_RGI_DT_PCH 53
CNV_BRI_RSP_PCH 53
CNV_BRI_DT_PCH 53
M.2_BT_PCMOUT_CLKREQ0 53
M.2_BT_PCMFRM_CRF_RST_N 53
@20200528_RF add

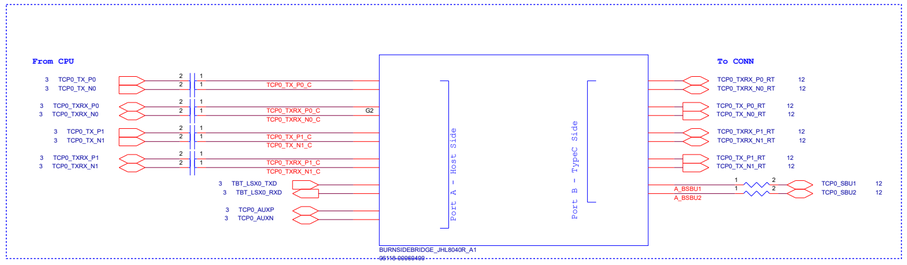

2800 mils
+VCCIN
+VCCIN
A24
TGL-UP3
P_VCCIN_VCCSENSE_50OHM
P_VCCIN_VSSSENSE_50OHM
P_SVID_DATA_50OHM_X2
P_SVID_CLK_50OHM_X2
P_SVID_ALERT#_X3
+1.2V
TGL-UP3
+VCCSTG_OUT
+VCCSTG_12
+VCCSTG_OUT
V15
+VCCIO_OUT
+VCCSTG_OUT_LGC
+1.05V_VCCST
+VCCSTG_345
PU power rail
+VCCSTG_OUT
+VCCSTG_12
0Ohm
+VCCSTG
+VCCSTG_345
0Ohm
UX435 follow VC
SVID DATA
+1.05V_VCCST
100Ohm
nbs_r0201_h12_000s
1%
P_SVID_DATA_50OHM_X2
80
SVID CLOCK
P_SVID_CLK_50OHM_X2
80
SVID ALERT
+1.05V_VCCST
56Ohm
nbs_r0201_h12_000s
0OHM
P_SVID_ALERT#_50OHM_X2
80
+VCCSTG
+1.05V_VCCST
+VCCSTG
1UF/6.3V
nbs_c0201_h14_000s
GND
+VCCIN
10UF/6.3V
+1.2V
GND
+1.2V
GND

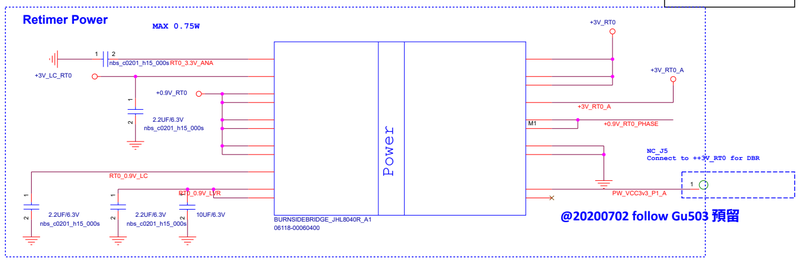


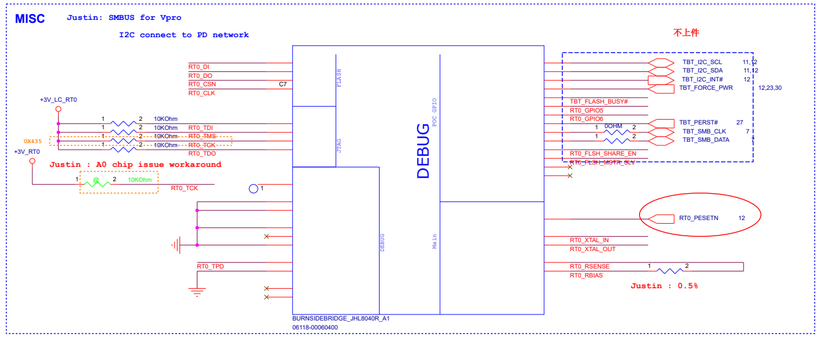
@20200616_add C1031~36: 15PF for EMI/RF

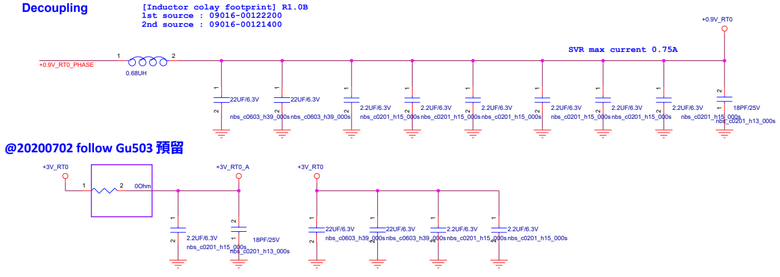


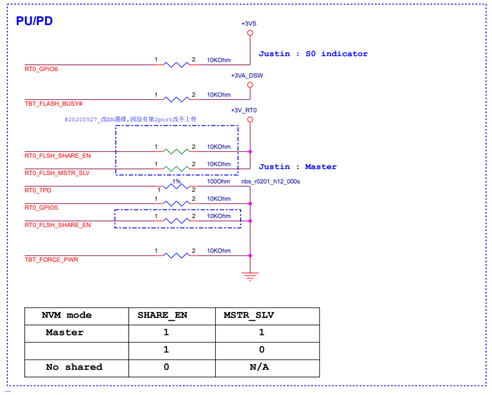
Main Board



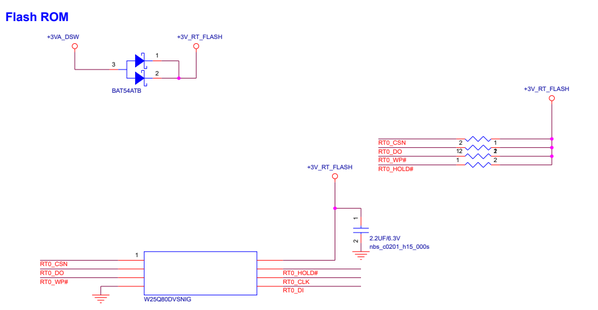


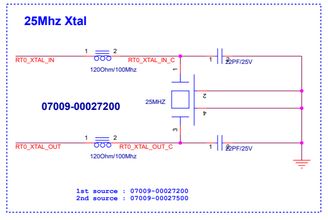




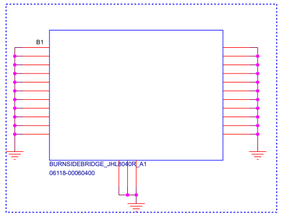


NVM mode	SHARE_EN	MSTR_SLV
Master	1	1
	1	0
No shared	0	N/A



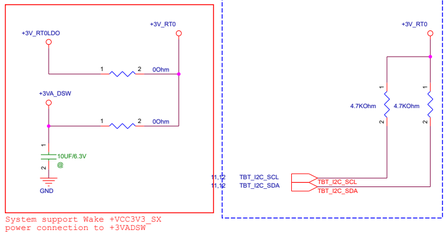


將18PF改22PCF



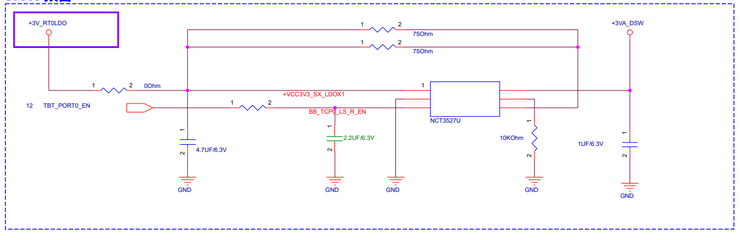
8202083l_TBT_I2C_SCL/TBT_I2C_SDA PU +3V_RT0

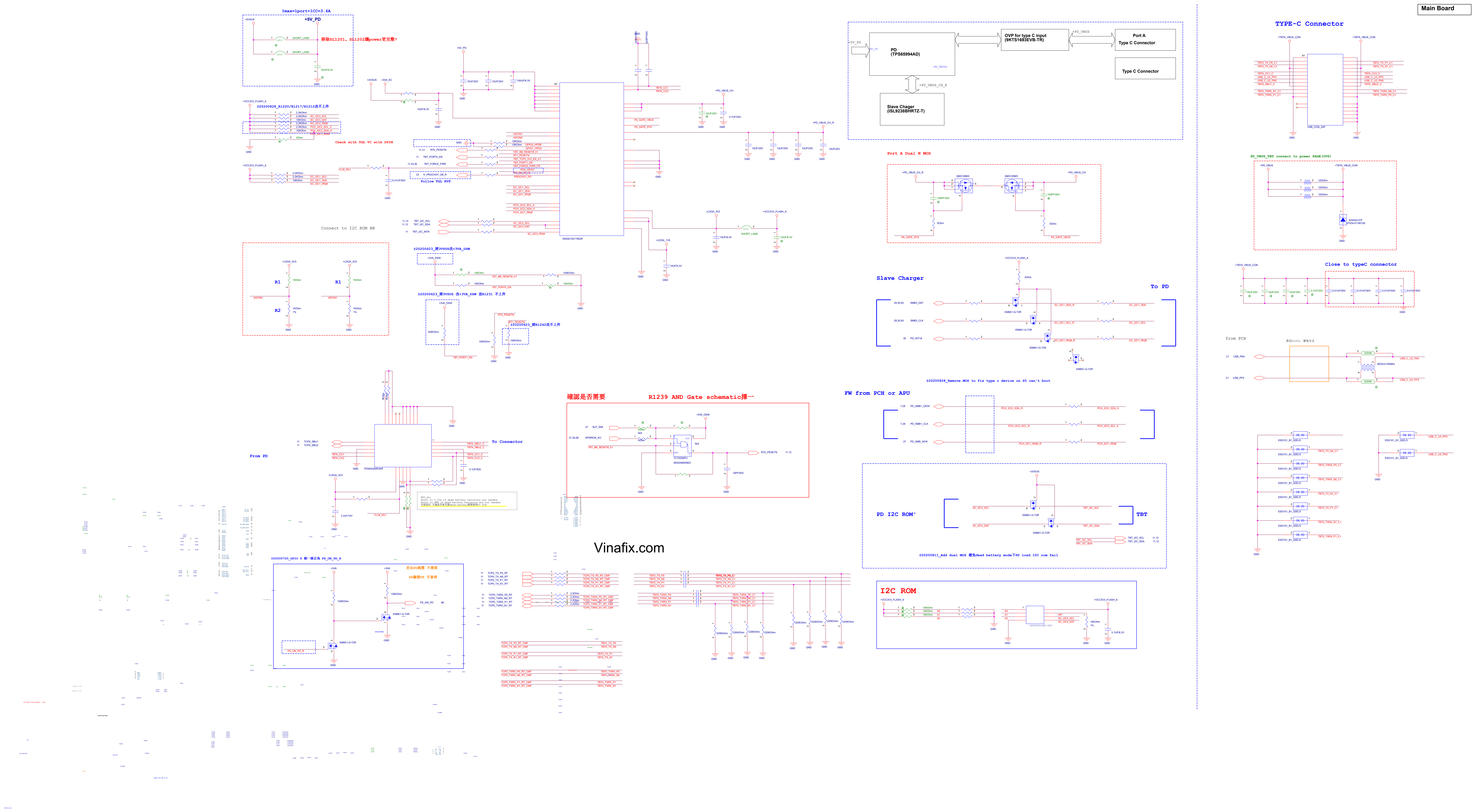
@20200702 follow Gu503 預留



Check which power solution should be used

@20200702 follow Gu503 預留

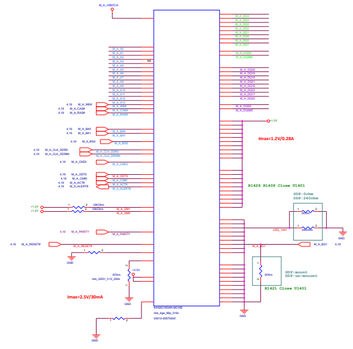


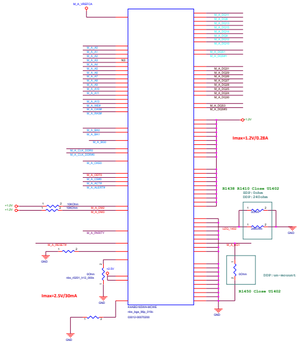

Main Board
TYPE-C Connector
Imax=1port+1CC=3.6A
+5V_PD
Check with TGL VC with DPIN
Connect to I2C ROM BB
PD (TPS65994AD)
OVP for type C input (SKTS1693EVB-TR)
Port A Type C Connector
Type C Connector
Slave Chager (ISL9238BHRTZ-T)
Port A Dual N MOS
Slave Charger
To PD
Close to typeC connector
From PD
To Connector
確認是否需要
R1239 AND Gate schematic
FW from PCH or APU
PD I2C ROM'
TBT
I2C ROM

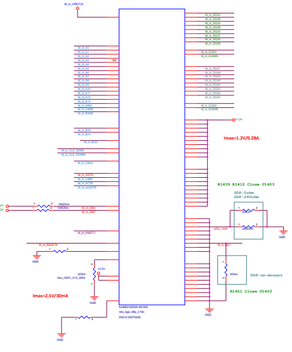
8Gb_Micron: 03012-00030900
8Gb_Samsung: 03012-00031000

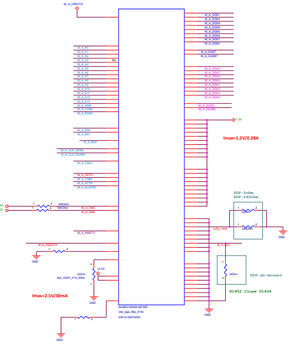
1Gx8(IO)
Total: 1Gx8ea = 8G

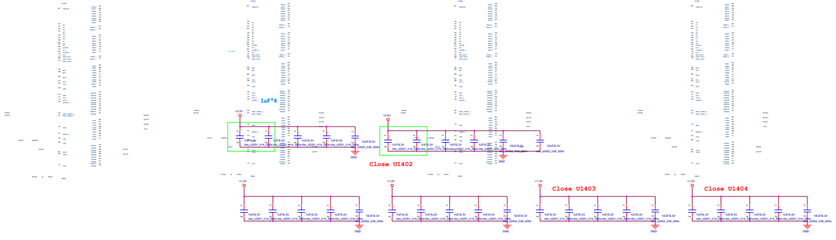
DDR4 3200 2048MP8 1.2V = 16G
8Gb_Micron: 03012-00060400 (此次更换_0409
8Gb_Samsung: 03012-00060500



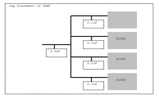


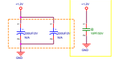




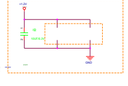


DIM Thermal Sensor





CE1402, CE1401 (220uf) change to CE1601 (330uf)
@20190626A



Add C1401 C1402 C1458
請設置未裝
@20150713A

Delete C1402 C1458
C1401 0805 -- 0603
請設置未裝
@20150715E

Table 4-25. DDR4 Memory Down Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 Memory Down x8- 8 Devices per Channel	VDDQ/VDD (shelled)	4 als near each x8 DRAM device as possible	64x 1µF (0402) [min of 48 stuffed]	
		Distributed around the DRAM devices	30x 10uF (0603) [min of 12 stuffed]	
	VPP	2 as near each x8 DRAM device as possible	32x 1µF (0402)	
		Distributed around the DRAM devices	10x 10uF (0603)	
	VTT	Distributed along termination resistors	32x 1µF (0402)	
		Distributed evenly across domain	8x 10µF (0603)	

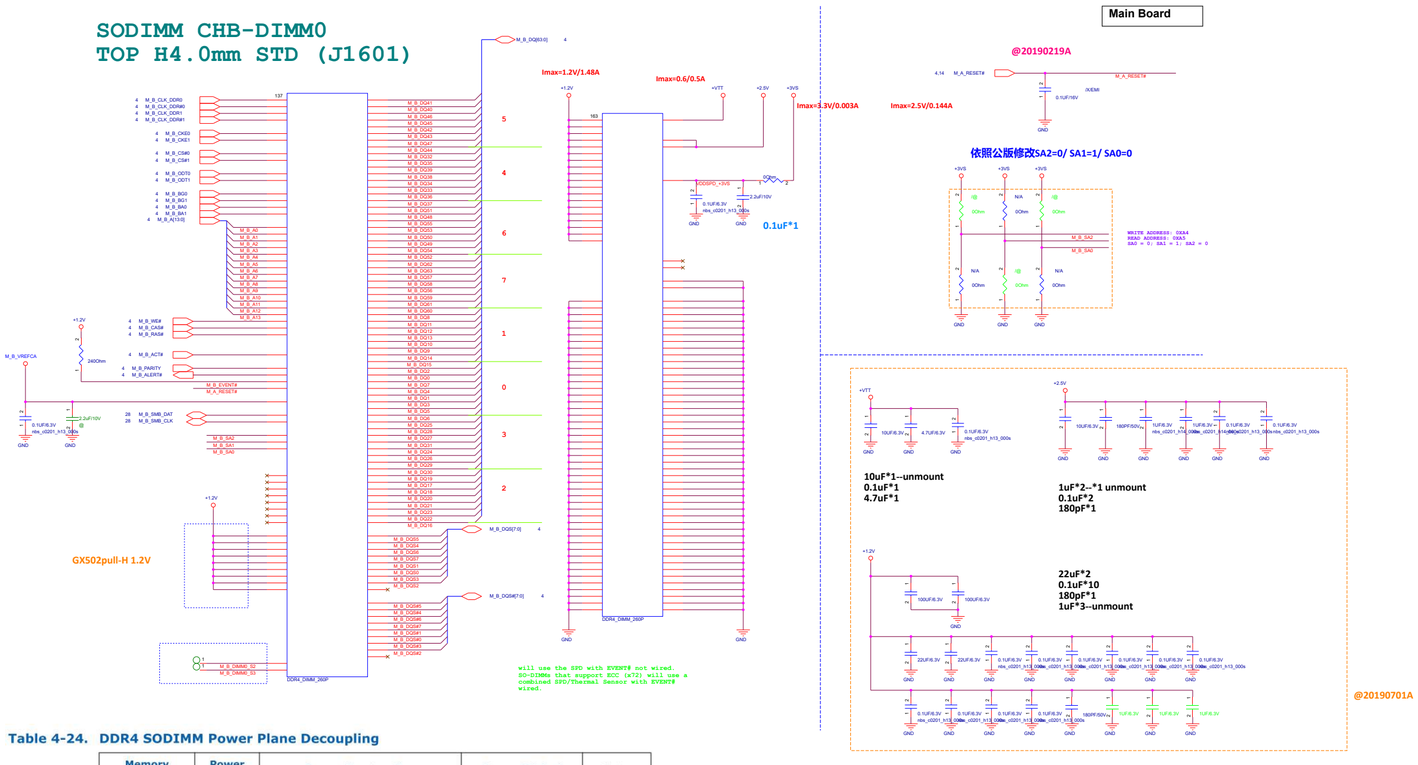


Table 4-24. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM **1DPC**	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Placed on VTT plane close to DIMM, 1 cap stuffed, 1 placeholder	2x 10µF (0603)	
		Placed on VTT plane close to DIMM	4x 1µF (0402)	
	VPP	DIMM Pin side, 1 per DIMM	2x 10µF (0603)	
		DIMM Pin side, 1 per DIMM	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	2x 0.1µF (0402)	
		Place close to DIMM	2x 2.2µF (0402)	

Figure 4-24. CFL-H DDR4 x8 Memory Down V_{REF-CA} Overview

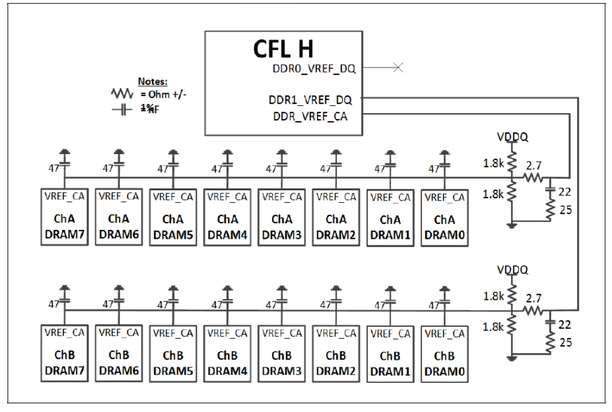
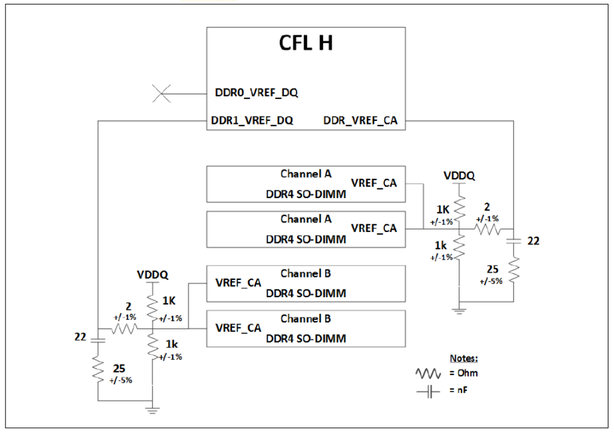
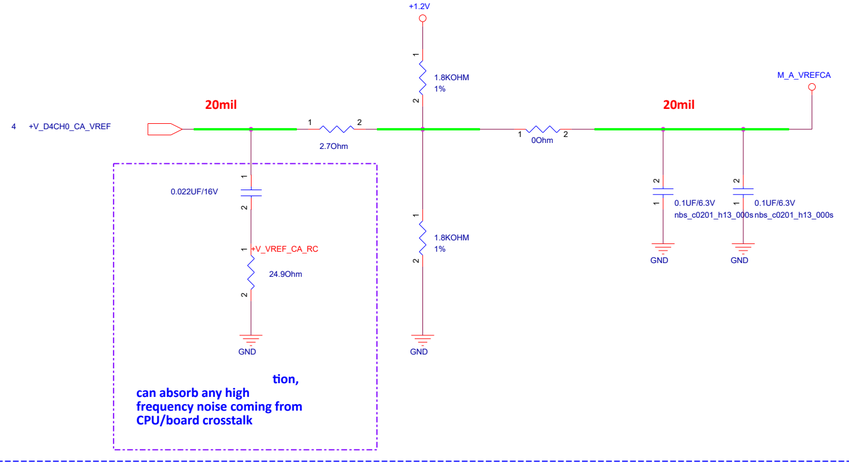


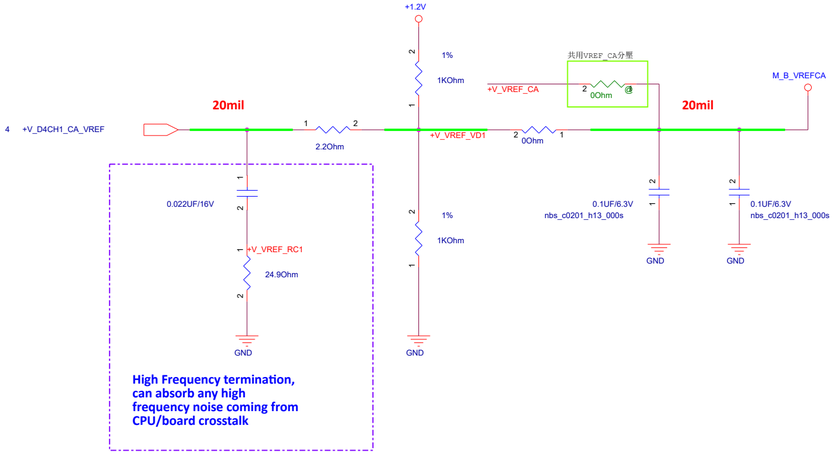
Figure 4-22. CFL-H DDR4 SO-DIMM V_{REF-CA} Overview

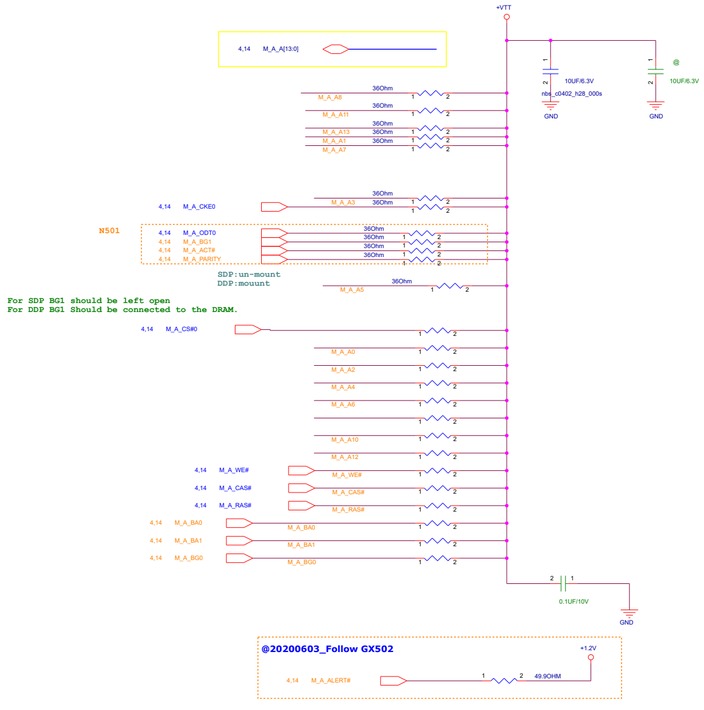


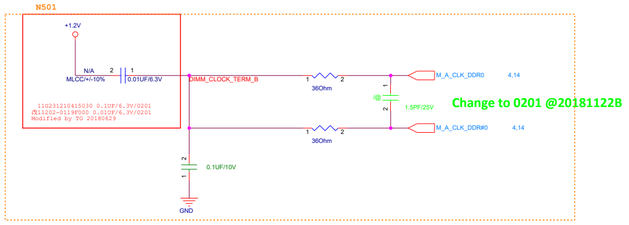
Memory Down Vref

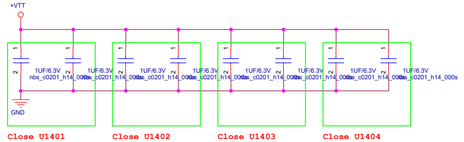


SO-DIMM1 Vref









1uF*16

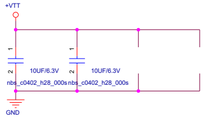
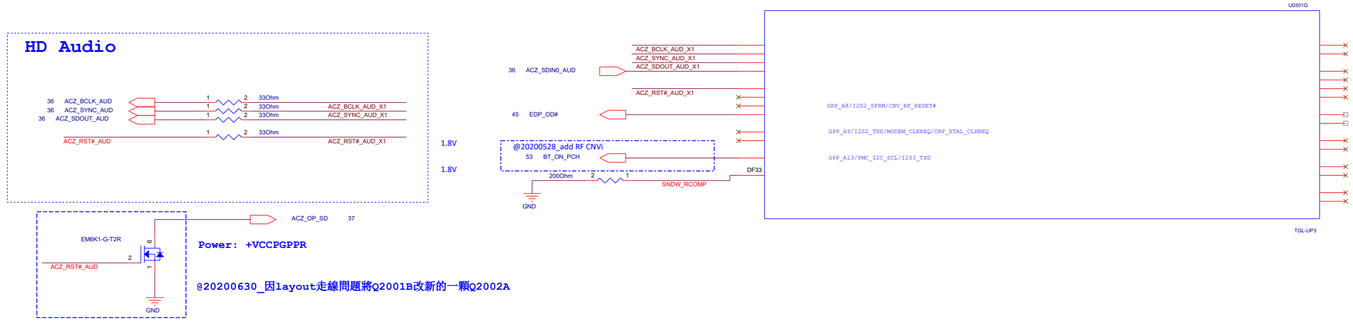
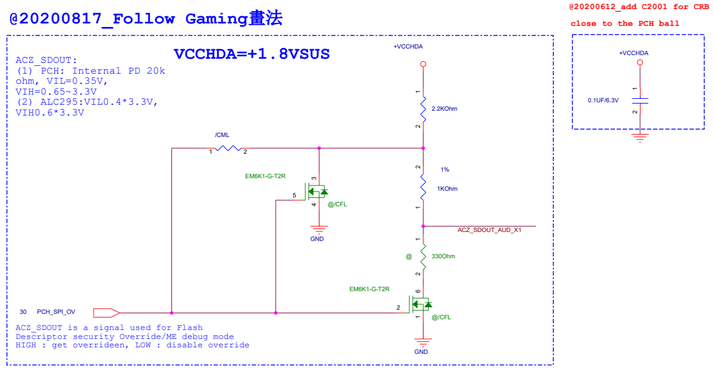


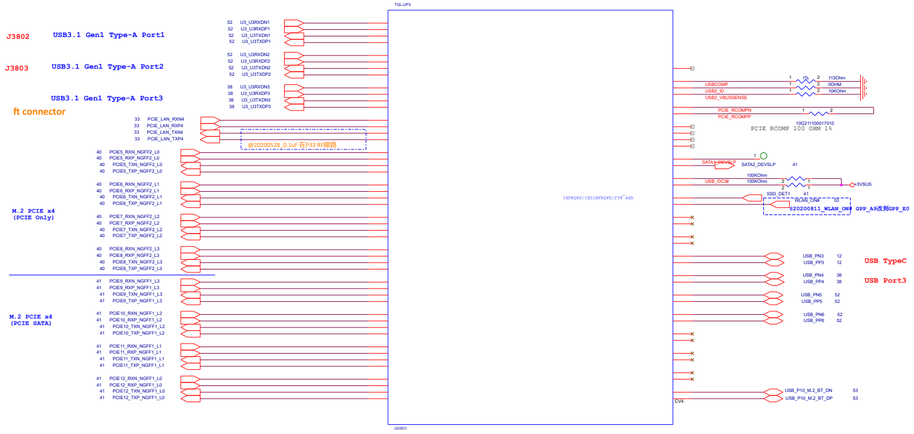
Table 4-25. DDR4 Memory Down Power Plane Decoupling

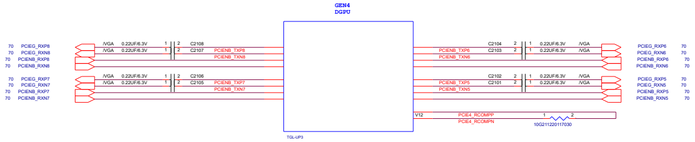
Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 Memory Down x8- 8 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x8 DRAM device as possible	64x 1µF (0402) (min of 48 stuffed)	
		Distributed around the DRAM devices	20x 10µF (0603) (min of 12 stuffed)	
	VPP	2 as near each x8 DRAM device as possible	32x 1µF (0402)	
		Distributed around the DRAM devices	10x 10µF (0603)	
	VTT	Distributed along termination resistors	32x 1µF (0402)	
		Distributed evenly across domain	8x 10µF (0603)	

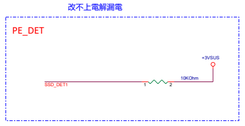

HD Audio
36 ACZ_BCLK_AUD
36 ACZ_SYNC_AUD
36 ACZ_SDOUT_AUD
ACZ_RST#_AUD
33Ohm
ACZ_BCLK_AUD_X1
ACZ_SYNC_AUD_X1
ACZ_RST#_AUD_X1
36 ACZ_SDIN0_AUD
45 EDP_OD#
1.8V
1.8V
@20200528_add RF CNVi
53 BT_ON_PCH
200Ohm
GND
DF33
SNDW_RCOMP
U0301G
GPP_A8/I2S2_SFRM/CNV_RF_RESET#
GPP_A9/I2S2_TXD/MODEM_CLKREQ/CRF_XTAL_CLKREQ
GPP_A13/PMC_I2C_SCL/I2S3_TXD
TGL-UP3
EM6K1-G-T2R
ACZ_OP_SD 37
Power: +VCCPGPPR
@20200630_因layout走線問題將Q2001B改新的一顆Q2002A


@20200817_Follow Gaming畫法
VCCHDA=+1.8VSUS
ACZ_SDOUT:
(1) PCH: Internal PD 20k ohm, VIL=0.35V, VIH=0.65~3.3V
(2) ALC295:VIL0.4*3.3V, VIH0.6*3.3V
+VCCHDA
2.2KOhm
/CML
EM6K1-G-T2R
@/CFL
1%
1KOhm
ACZ_SDOUT_AUD_X1
@
330Ohm
30 PCH_SPI_OV
ACZ_SDOUT is a signal used for Flash Descriptor security Override/ME debug mode
HIGH : get overrideen, LOW : disable override
GND

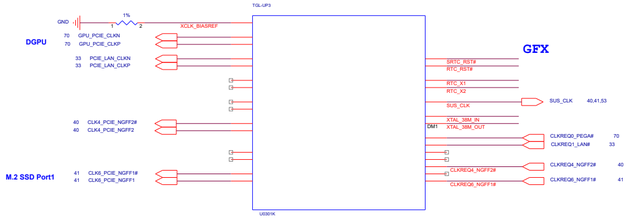
@20200612_add C2001 for CRB close to the PCH ball
+VCCHDA
0.1UF/6.3V







PCI-E* X1	PCIE USAGE DEFAULT/OPTION	Co-lay	Clock
PCIE 1	N/A		
PCIE 2	N/A		
PCIE 3	N/A		
PCIE 4	N/A		
PCIE 5	N/A		
PCIE 6	N/A		
PCIE 7/SATA 0	N/A		
PCIE 8/SATA 1A	N/A		
PCIE 9	N/A		
PCIE 10	N/A		
PCIE 11/SATA 0	N/A		
PCIE 12/SATA 1A	PCIE SSD		
PCIE 13	PCIE SSD		
PCIE 14	PCIE SSD		
PCIE 15/SATA 1B	PCIE SSD		
PCIE 16/SATA 2	SATA SSD		

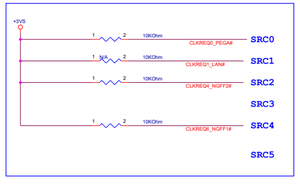


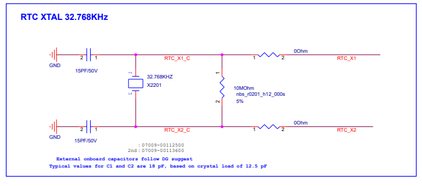
CLKOUT_PCIE_P/N [6:4, 2:1] = Support up to PCIe Gen3
CLKOUT_PCIE_P/N [3, 0] = Support up to PCIe Gen4

- CLKOUT_PCIE_P/N [3, 0] = Must be used for PCIe* Gen4 support

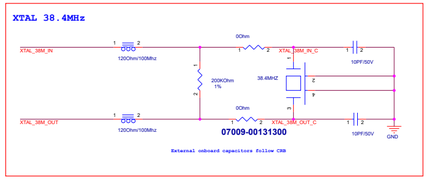
Any un-used CLKOUT_PCIE_P/N differential pair not being routed on a platform should be configured as "Disabled" through the Intel® Flash Image Tool (FIT) tool. The CLKOUT_PCIE_P/N differential pairs are called out as CLKOUT_SRC differential outputs in FIT as discussed in the SPI Programming Guide.

@20200630_XTAL change 07009-00111800 15PF for UX482

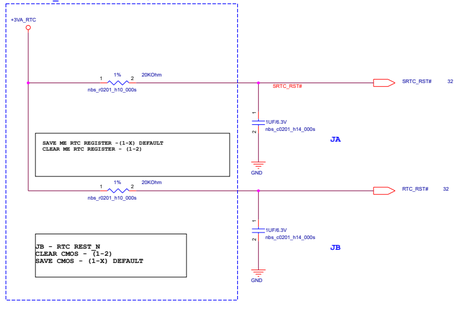


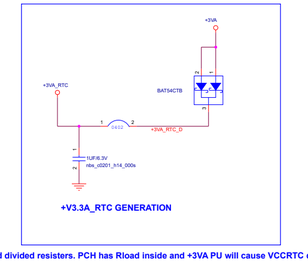


@20200630_將C2201 C2202 Change 10PF for UX482 R1.1



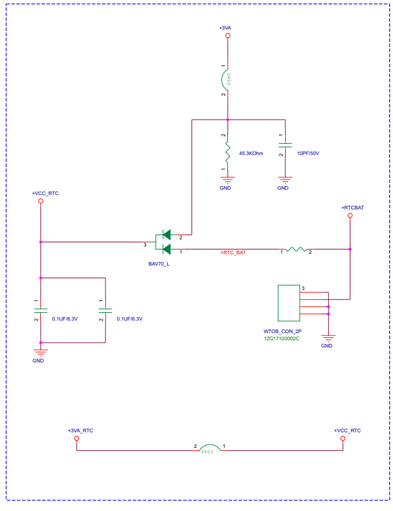
@20200611_R2209 R2210 由27K改20K for CRB



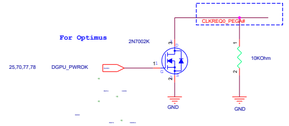


Justin : No used divided resisters. PCH has Rload inside and +3VA PU will cause VCCRTC drop to 2.7V in S0
VCCRTC must not exceed 3.3V and sustained operation at voltages below 3.0V is not recommended
Intel suggested to use diode circuit for long life relibility

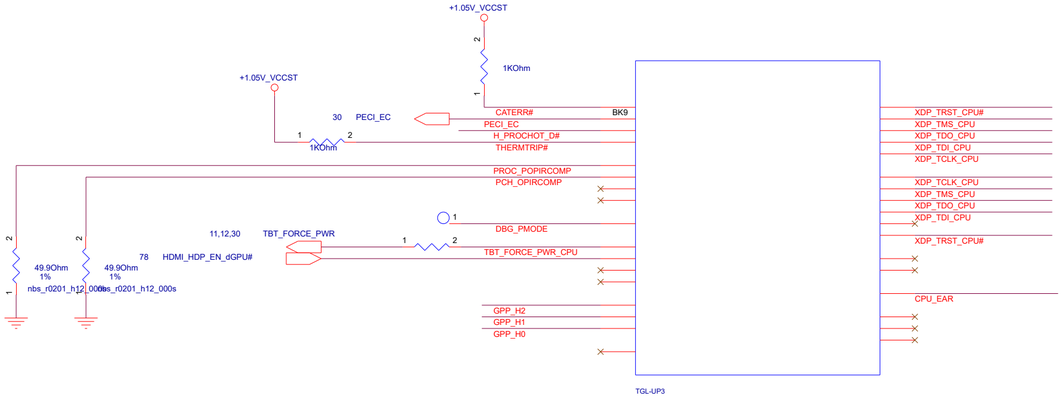
@20200702_add RTC battery

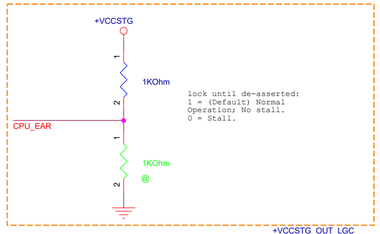


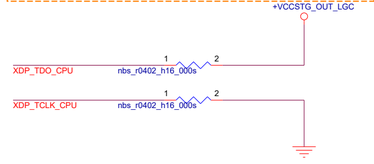
@20200630_change name CLKREQ0_PEGA#

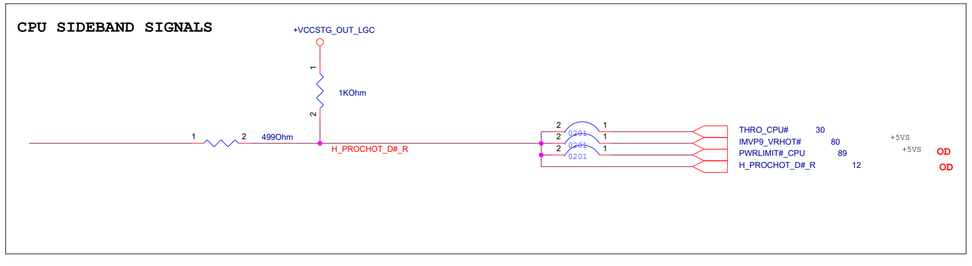


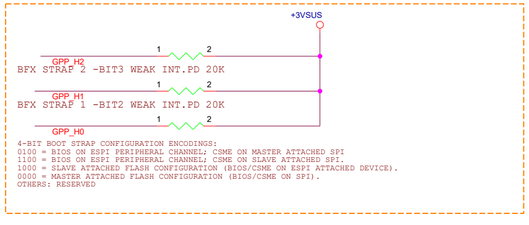
Main Board

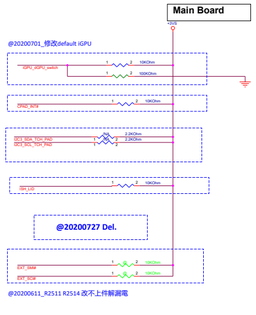

+1.05V_VCCST
1KOhm
+1.05V_VCCST
30 PECI_EC
CATERR# BK9
PECI_EC
H_PROCHOT_D#
THERMTRIP#
1KOhm
PROC_POPIRCOMP
PCH_OPIRCOMP
11,12,30 TBT_FORCE_PWR
DBG_PMODE
78 HDMI_HDP_EN_dGPU#
TBT_FORCE_PWR_CPU
49.9Ohm 1%
nbs_r0201_h12_000s
49.9Ohm 1%
nbs_r0201_h12_000s
GPP_H2
GPP_H1
GPP_H0
XDP_TRST_CPU#
XDP_TMS_CPU
XDP_TDO_CPU
XDP_TDI_CPU
XDP_TCLK_CPU
XDP_TCLK_CPU
XDP_TMS_CPU
XDP_TDO_CPU
XDP_TDI_CPU
XDP_TRST_CPU#
CPU_EAR
TGL-UP3

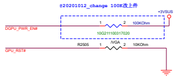

+VCCSTG
1KOhm
lock until de-asserted:
1 = (Default) Normal
Operation; No stall.
0 = Stall.
CPU_EAR
1KOhm
@

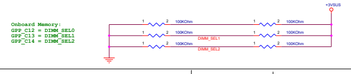

+VCCSTG_OUT_LGC
XDP_TDO_CPU
nbs_r0402_h16_000s
XDP_TCLK_CPU
nbs_r0402_h16_000s


CPU SIDEBAND SIGNALS
+VCCSTG_OUT_LGC
1KOhm
499Ohm
H_PROCHOT_D#_R
THRO_CPU# 30
IMVP9_VRHOT# 80
PWRLIMIT#_CPU 89
H_PROCHOT_D#_R 12
+5VS
+5VS
OD
OD

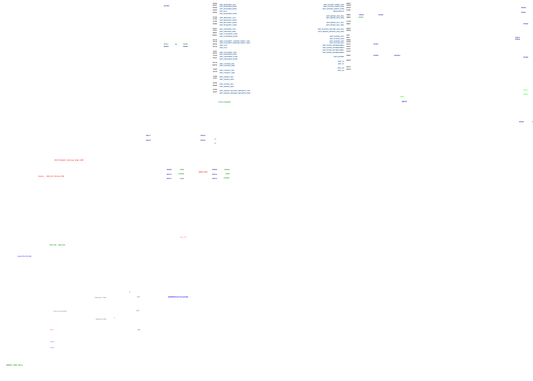

+3VSUS
GPP_H2
BFX STRAP 2 -BIT3 WEAK INT.PD 20K
GPP_H1
BFX STRAP 1 -BIT2 WEAK INT.PD 20K
GPP_H0
4-BIT BOOT STRAP CONFIGURATION ENCODINGS:
0100 = BIOS ON ESPI PERIPHERAL CHANNEL; CSME ON MASTER ATTACHED SPI
1100 = BIOS ON ESPI PERIPHERAL CHANNEL; CSME ON SLAVE ATTACHED SPI.
1000 = SLAVE ATTACHED FLASH CONFIGURATION (BIOS/CSME ON ESPI ATTACHED DEVICE).
0000 = MASTER ATTACHED FLASH CONFIGURATION (BIOS/CSME ON SPI).
OTHERS: RESERVED

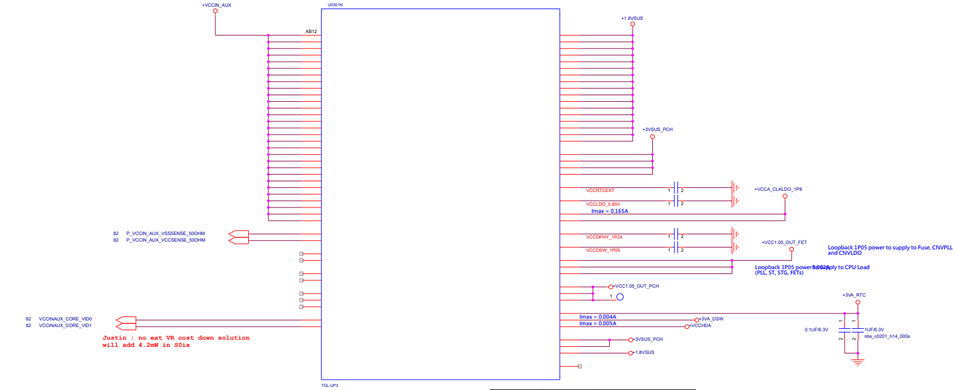




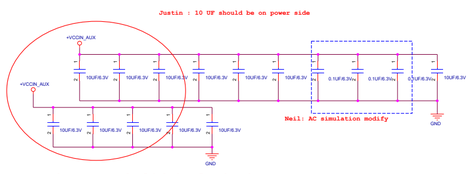


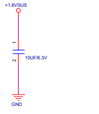
			DIMM_SEL#			Key Part List
			GPP_C14	GPP_C13		
			2	1		
03012-00070200	目前線路		0	0	0	上 R2508 / R2512 / R2513 不上件: R2509 / R2512 / R2515
			0	0	1	
		MICRO 8Gb	0	1	0	上 R2508 / R2512 / R2513 不上件: R2509 / R2510 / R2515
03012-00040700				1	1	主件: R2509 / R2512 / R2513 不上件: R2508 / R2510 / R2515
			1	0	0	
03012-00070300	SKU1	Hynix 16Gb	1	0	1	上 R2509 / R2510 / R2515 不上件: R2508 / R2512 / R2513
			1	1	1	

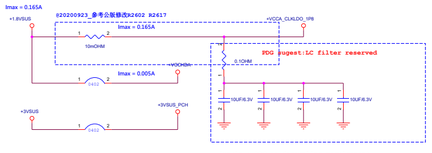


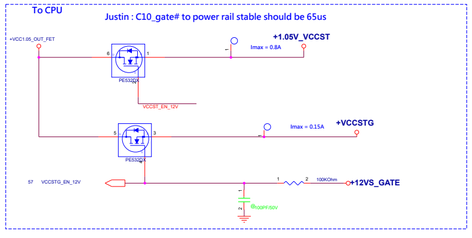


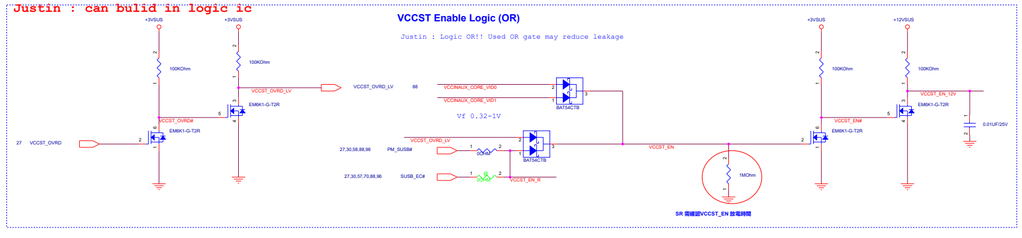
VID1	VID0	VCCIN_AUX
	0	0V
0	1	1.1V
1	0	1.65V
1	1	1.8V

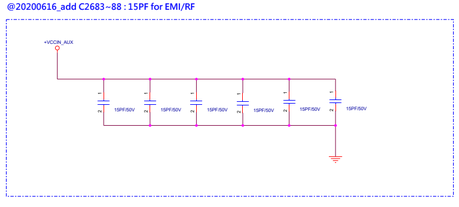


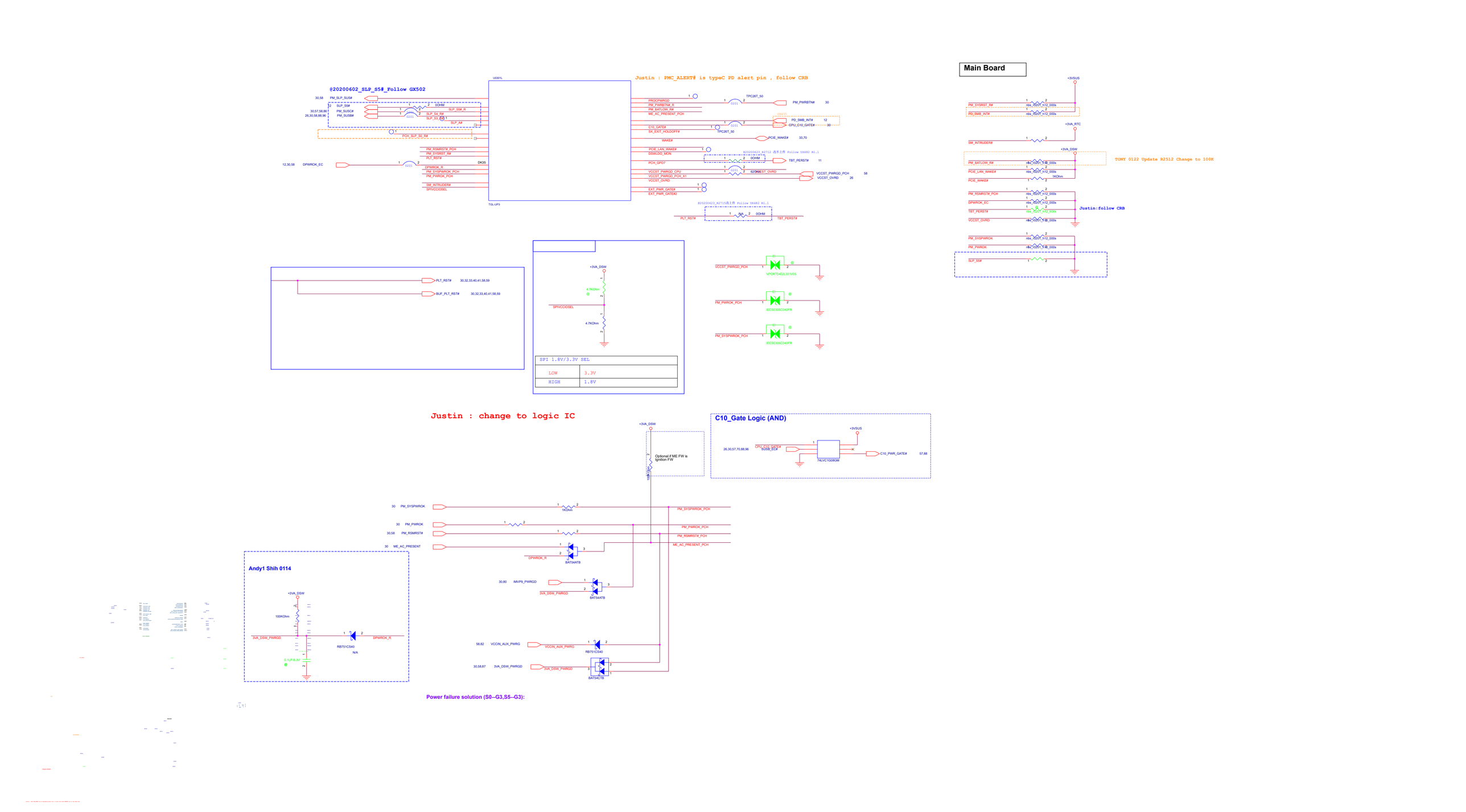




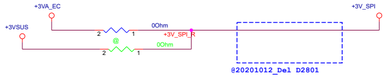







@20200602_SLP_S5#_Follow GX502
Justin : PMC_ALERT# is typeC PD alert pin , follow CRB
U3301L
TGL-UP3
30,58 PM_SLP_SUS#
SLP_S5#
30,57,58,86 PM_SUSC#
26,30,58,88,96 PM_SUSB#
SLP_S5#_R
SLP_S4_R#
SLP_3/5_R#
SLP_A#
PCH_SLP_S0_R#
PM_RSMRST#_PCH
PM_SYSRST_R#
PLT_RST#
12,30,58 DPWROK_EC
DPWROK_R
PM_SYSPWROK_PCH
PM_PWROK_PCH
SM_INTRUDER#
SPIVCCOSEL
DK35
PROCPWRGD
PM_PWRBTN#_R
PM_BATLOW_R#
ME_AC_PRESENT_PCH
C10_GATE#
SX_EXIT_HOLDOFF#
WAKE#
PCIE_LAN_WAKE#
DSWLDO_MON
PCH_GPD7
VCCST_PWRGD_CPU
VCCST_PWRGD_PCH_X1
VCCST_OVRD
EXT_PWR_GATE#
EXT_PWR_GATE#2
TPC26T_50
PM_PWRBTN# 30
PD_SMB_INT# 12
GPU_C10_GATE# 80
PCIE_WAKE# 33,70
TBT_PERST# 11
62OHM
VCCST_PWRGD_PCH 58
VCCST_OVRD 26
PLT_RST#
TBT_PERST#
Main Board
+3VSUS
+3VA_RTC
+3VA_DSW
TONY 0122 Update R2512 Change to 100K
Justin:follow CRB
PLT_RST# 30,32,33,40,41,58,59
BUF_PLT_RST# 30,32,33,40,41,58,59
SPI 1.8V/3.3V SEL
LOW 3.3V
HIGH 1.8V
VPORT0402L331V05
IEC0030SC040FR
Justin : change to logic IC
C10_Gate Logic (AND)
Optional if ME FW is Ignition FW
74LVC1G08GM
C10_PWR_GATE# 57,88
30 PM_SYSPWROK
30 PM_PWROK
30,58 PM_RSMRST#
30 ME_AC_PRESENT
30,80 IMVP9_PWRGD
58,82 VCCIN_AUX_PWRG
30,58,87 3VA_DSW_PWRGD
Andy1 Shih 0114
100KOhm
0.1UF/6.3V
RB751CS40
N/A
Power failure solution (S0--G3,S5--G3):

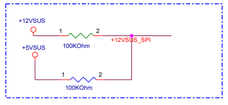
Justin : for PD platform using +3VA_EC to avoid dead battery issue.



EC G3 flash sharing with Wire-OR Topology
Justin :Follow DG 6.12.3.2

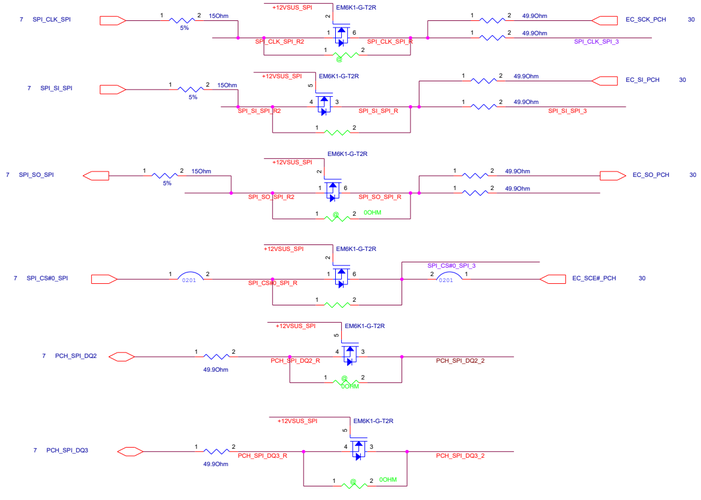
R2 75 ohm
R3 22 ohm
R4 X

tion aviod SPI leakage



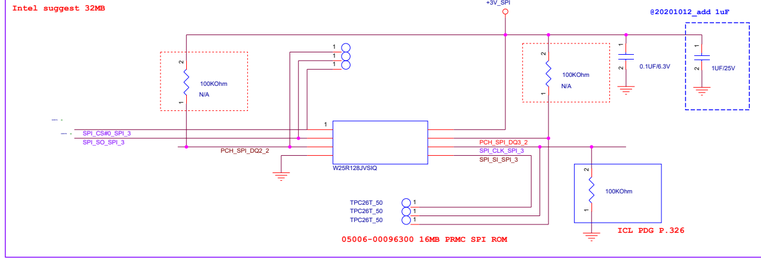
@20200611_新增R2810 Pull 5VSUS
並將R2815改不上件,解漏電

EC,SPI ROM Side



@20200709_modify 05006-00096300 16MB PRMC SPI ROM

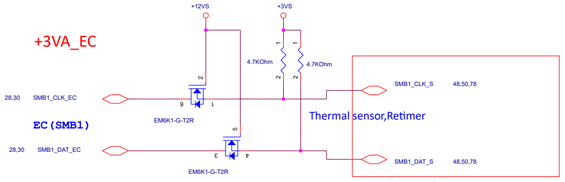
Intel suggest 32MB



05006-00096300 16MB PRMC SPI ROM

ICL PDG P.326

+3VA_EC

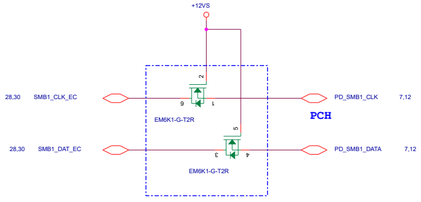


EC(SMB1)

ADDR 0x7E

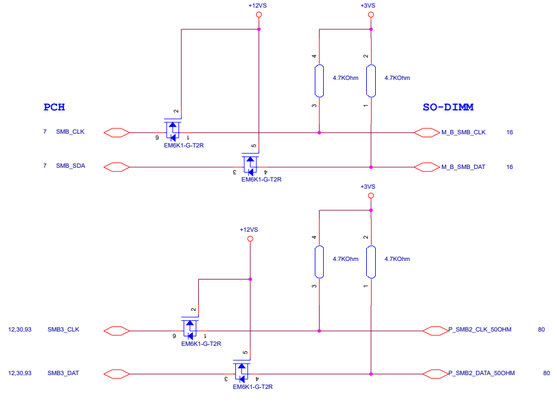
CPU Thermal sensor

VRAM Thermal sensor



@20200707_改不上件

@20200602 Remove SMB_CLK to AMP NVVDD CLK Switck



EC 8585

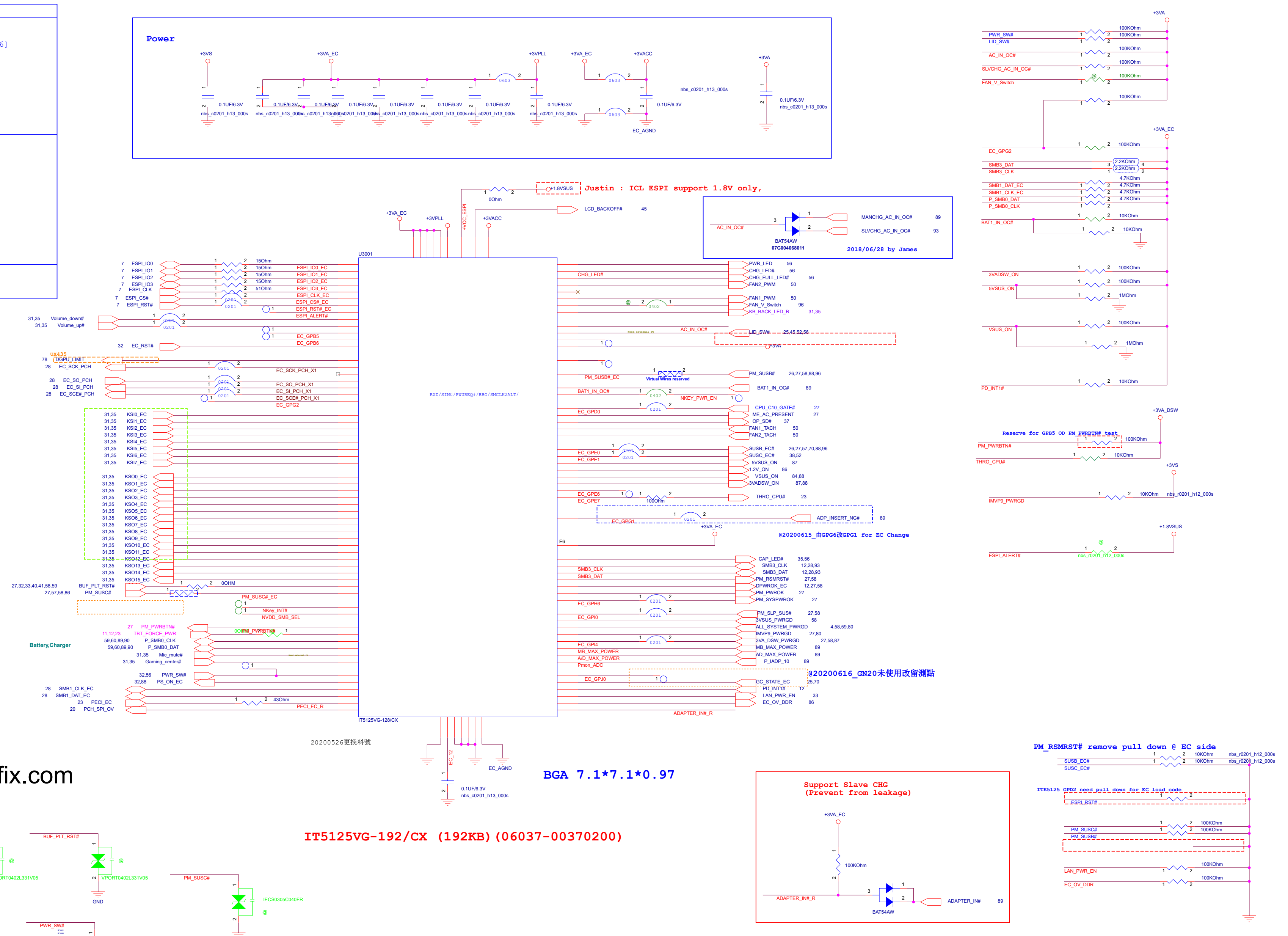
Only 3V Torlence

GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]

Can be adjusted to Open-Drain for port:

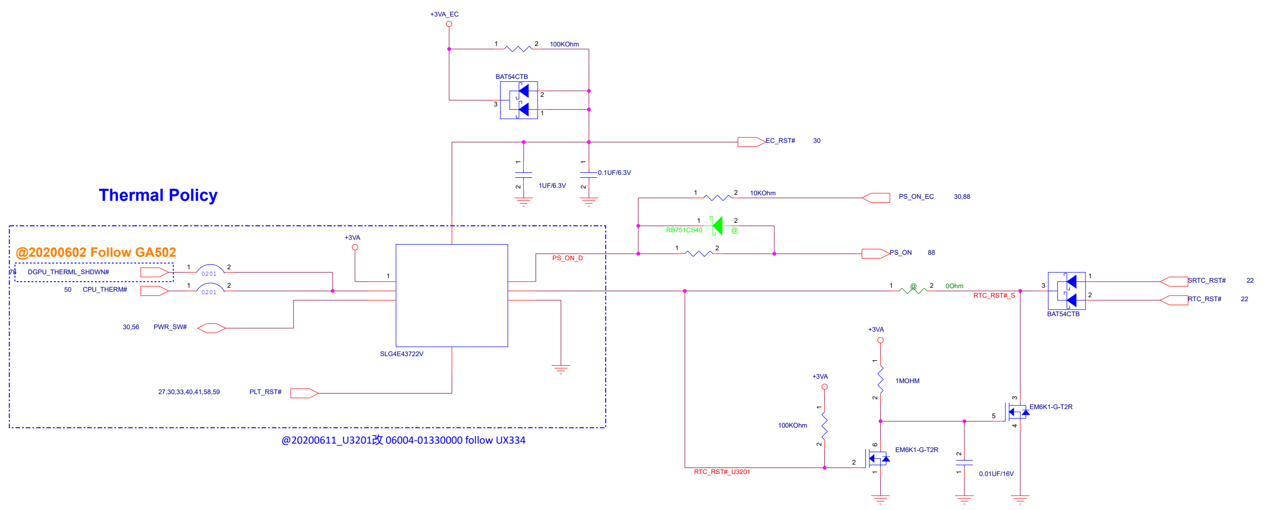
GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

EC Require



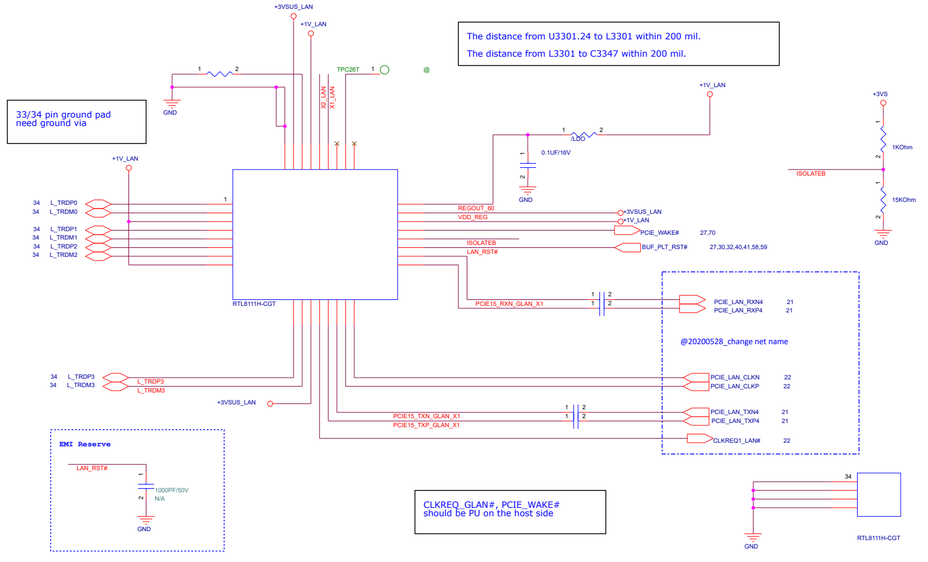
Vinafix.com

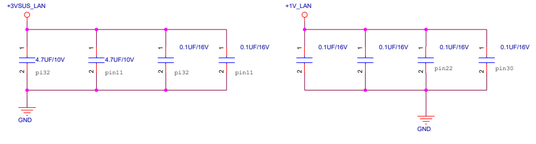
IT5125VG-192/CX (192KB)(06037-00370200)



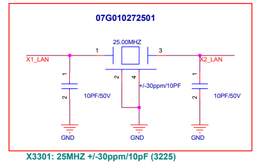
Thermal Policy
@20200602 Follow GA502
+3VA_EC
100KOhm
BAT54CTB
1UF/6.3V
0.1UF/6.3V
EC_RST# 30
10KOhm
PS_ON_EC 30,88
RB751CS40
PS_ON_D
PS_ON 88
+3VA
78 DGPU_THERML_SHDWN#
50 CPU_THERM#
0201
30,56 PWR_SW#
SLG4E43722V
27,30,33,40,41,58,59 PLT_RST#
0Ohm
RTC_RST#_S
SRTC_RST# 22
RTC_RST# 22
BAT54CTB
1MOHM
100KOhm
EM6K1-G-T2R
0.01UF/16V
RTC_RST#_U3201
@20200611_U3201改 06004-01330000 follow UX334

Main Board





@20200615_換回較常用XTAL 但體積較大 for GA502 GX502

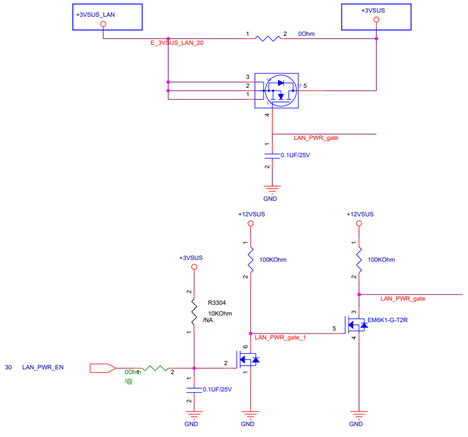


X3301: 25MHZ +/-30ppm/10pF (3225)

1st: P/N:07G010272501 TXC/7V25000011

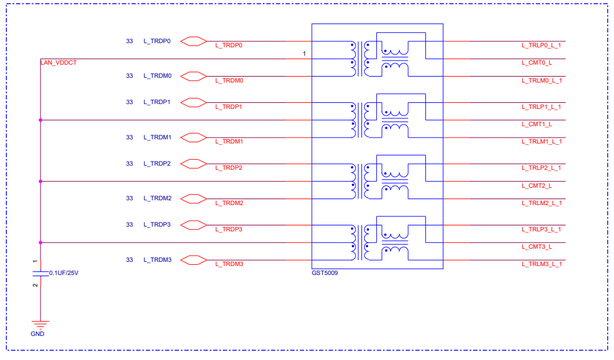
2nd: P/N:07G010952500 HOSONIC/E3FB25

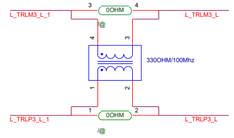
Realtek suggests 3V_LAN raise time 1ms

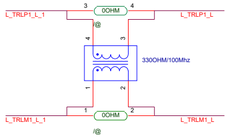


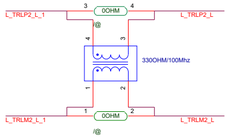
Main Board

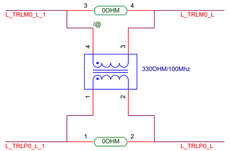
@20200702_RF要求修改連線順序

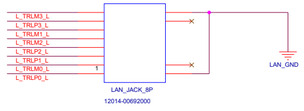


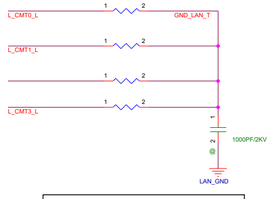


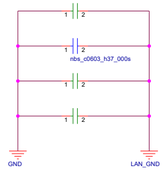








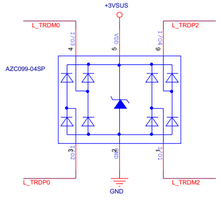




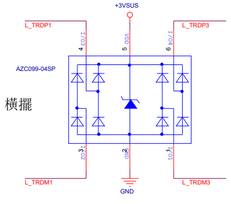
GND_LAN_T 上禁止加任何零件

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D



橫擺

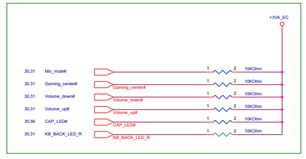


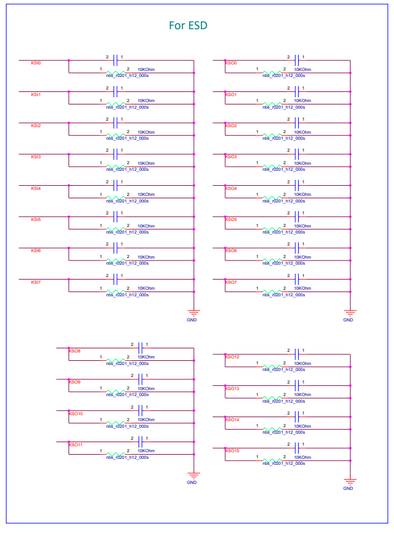
D3401,D3402 ESD Diode

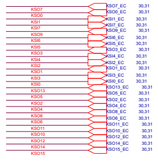
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

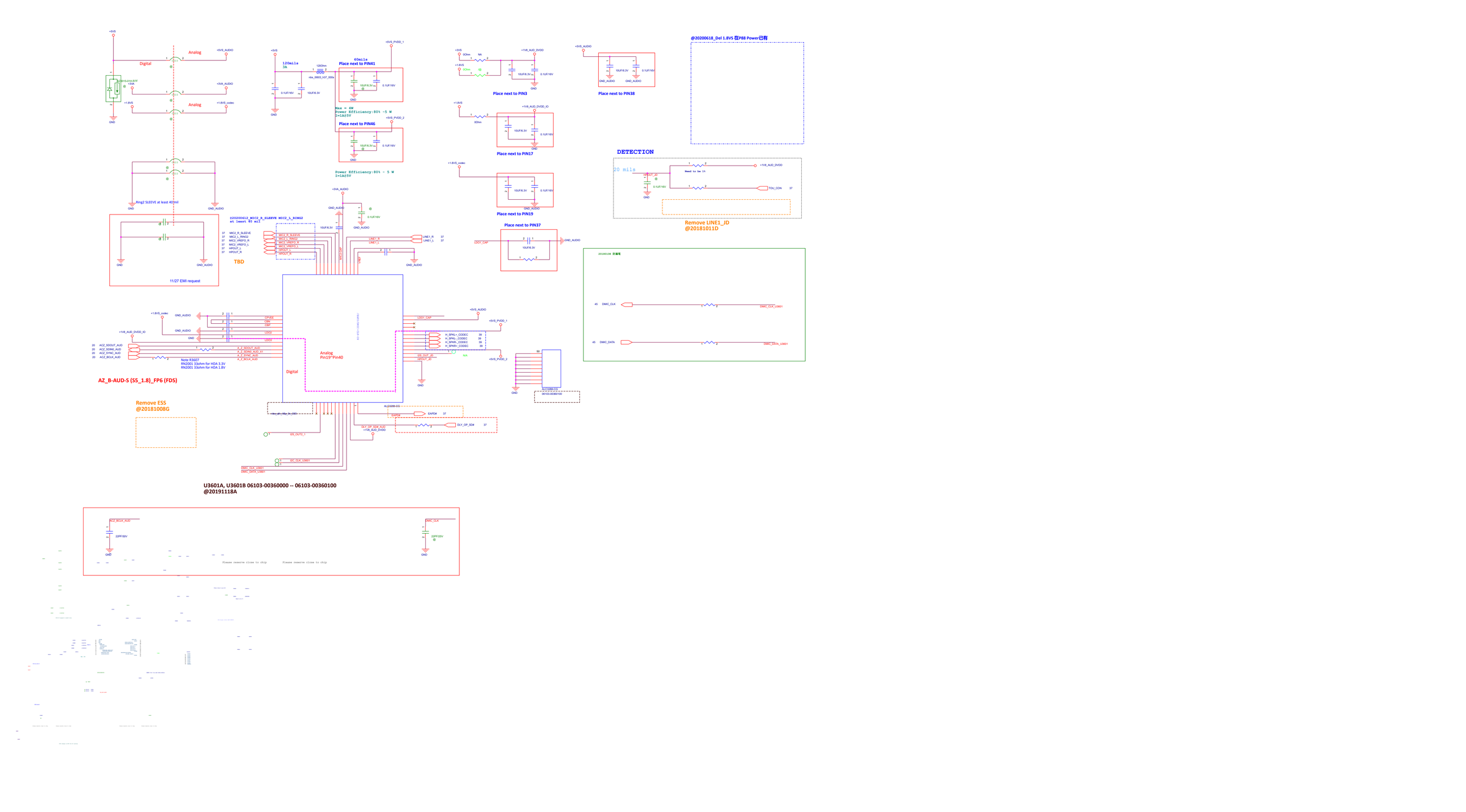
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

Pull up


+3VA_EC
30,31 Mic_mute#
30,31 Gaming_center#
30,31 Volume_down#
30,31 Volume_up#
30,56 CAP_LED#
30,31 KB_BACK_LED_R
10KOhm
Gaming_center#
Volume_down#
Volume_up#
CAP_LED#
KB_BACK_LED_R

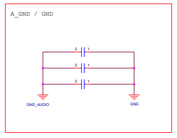

For ESD
KSO0
KSO1
KSO2
KSO3
KSO4
KSO5
KSO6
KSO7
KSO8
KSO9
KSO10
KSO11
KSO12
KSO13
KSO14
KSO15
10KOhm
nsk_dz01_tr12_000x
GND

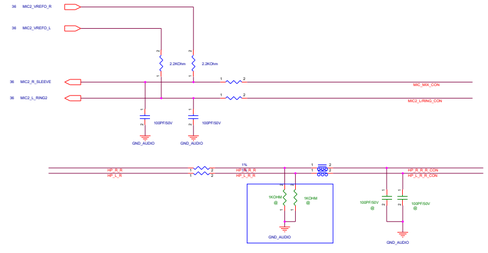

KSO7
KSO0
KSO1
KSO7
KSO6
KSO5
KSO4
KSO3
KSO2
KSO1
KSO0
KSO15
KSO14
KSO13
KSO12
KSO11
KSO10
KSO9
KSO8
KSI7_EC 30,31
KSI6_EC 30,31
KSI1_EC 30,31
KSI7_EC 30,31
KSI06_EC 30,31
KSI5_EC 30,31
KSI5_EC 30,31
KSI03_EC 30,31
KSI4_EC 30,31
KSI2_EC 30,31
KSI7_EC 30,31
KSI3_EC 30,31
KSI5_EC 30,31
KSO15_EC 30,31
KSO6_EC 30,31
KSO2_EC 30,31
KSO4_EC 30,31
KSO6_EC 30,31
KSO8_EC 30,31
KSO11_EC 30,31
KSO10_EC 30,31
KSO12_EC 30,31
KSO14_EC 30,31
KSO15_EC 30,31


Analog
Digital
Analog
Ring2 SLEEVE at least 40mil
11/27 EMI request
TBD
120mils
3A
60mils
Place next to PIN41
Max = 4W
Power Efficiency:80% ~5 W
I=1A@5V
Place next to PIN46
Power Efficiency:80% ~ 5 W
I=1A@5V
Place next to PIN3
Place next to PIN17
Place next to PIN19
Place next to PIN37
Place next to PIN38
@20200618_Del 1.8VS 在P88 Power已有
DETECTION
20 mils
Need to be 1%
Remove LINE1_JD
@20181011D
@20200612_MIC2_R_SLEEVE MIC2_L_RING2
at least 8o mil
Analog
Pin19~Pin40
Digital
AZ_B-AUD-S (S5_1.8)_FP6 (FDS)
Note R3607
RN2001 33ohm for HDA 3.3V
RN2001 33ohm for HDA 1.8V
Remove ESS
@20181008G
U3601A, U3601B 06103-00360000 -- 06103-00360100
@20191118A
Please reserve close to chip.
Please reserve close to chip

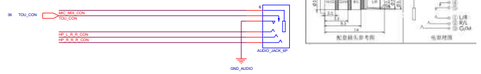
Main Board

A_GND / GND



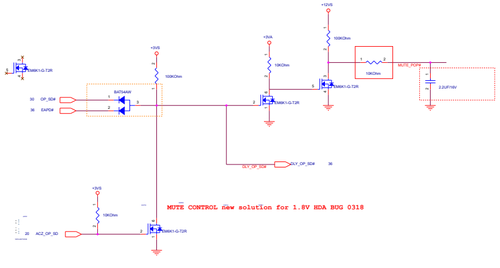


HP MIC Connector



MUTE

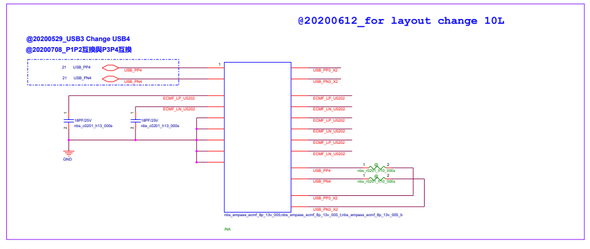
2016.09.06 Add DEPOP solution



MUTE CONTROL new solution for 1.8V HDA BOG 0318

USB3.1_Port3

USB2.0 EMI-Protection With ECMF(PCB 1.05mm_10Layer)

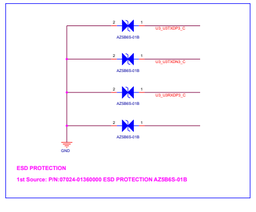


Note :

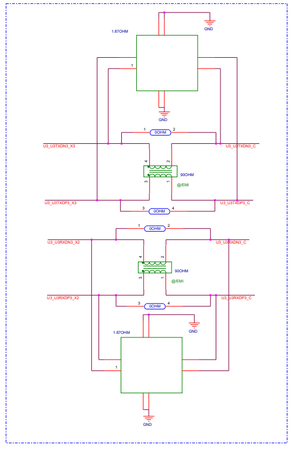
Please check your project must matching the thickness , DF and DK value of PCB every layer

3. Pin7 Pin8 Pin11 Pin12 must be connected to system ground

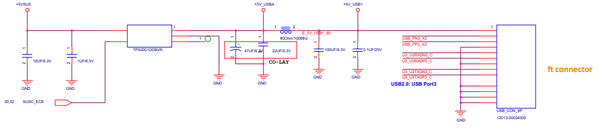
USB3.0 ESD-Protection



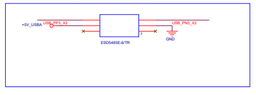
@20200615_新增L3801 L3802 L3811 L3812 for EMI

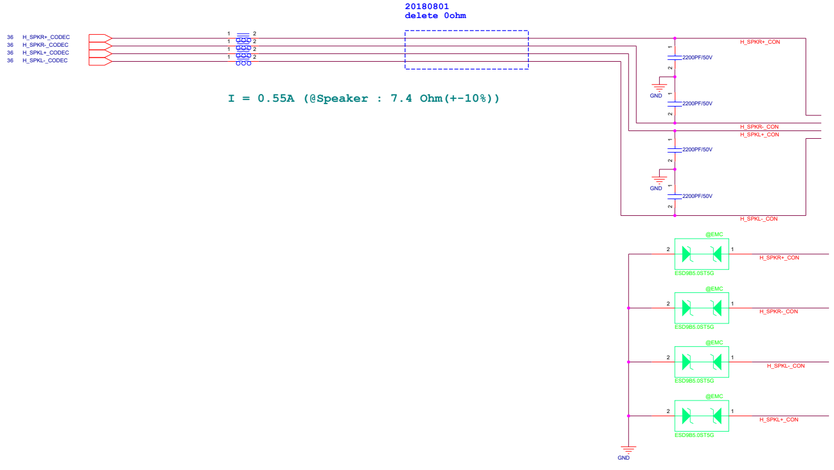


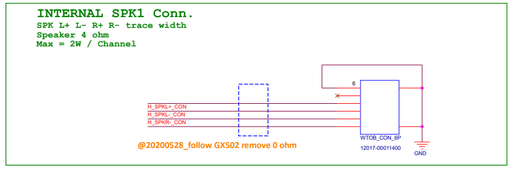
Main source: 09016-00030100



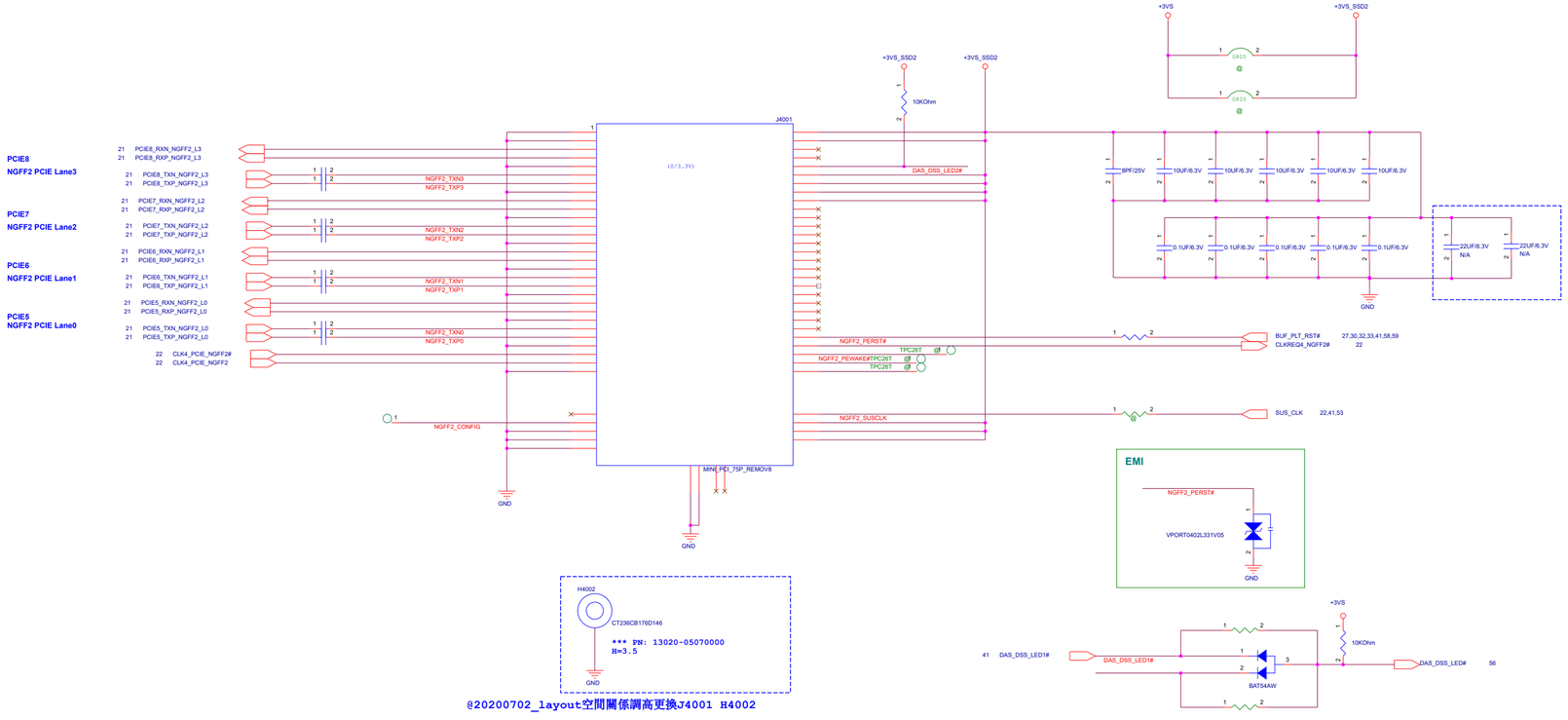
USB2.0 ESD-Protection



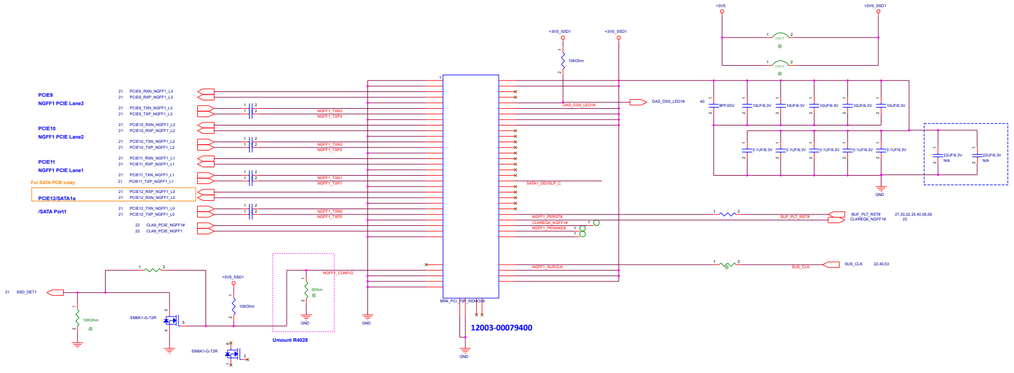

20180801
delete 0ohm
36 H_SPKR+_CODEC
36 H_SPKR-_CODEC
36 H_SPKL+_CODEC
36 H_SPKL-_CODEC
I = 0.55A (@Speaker : 7.4 Ohm(+-10%))
2200PF/50V
GND
H_SPKR+_CON
H_SPKR-_CON
H_SPKL+_CON
H_SPKL-_CON
@EMC
ESD985.0ST5G


INTERNAL SPK1 Conn.
SPK L+ L- R+ R- trace width
Speaker 4 ohm
Max = 2W / Channel
H_SPKL+_CON
H_SPKL-_CON
H_SPKR-_CON
WTOB_CON_6P
12017-2001140G
GND
@20200528_follow GX502 remove 0 ohm

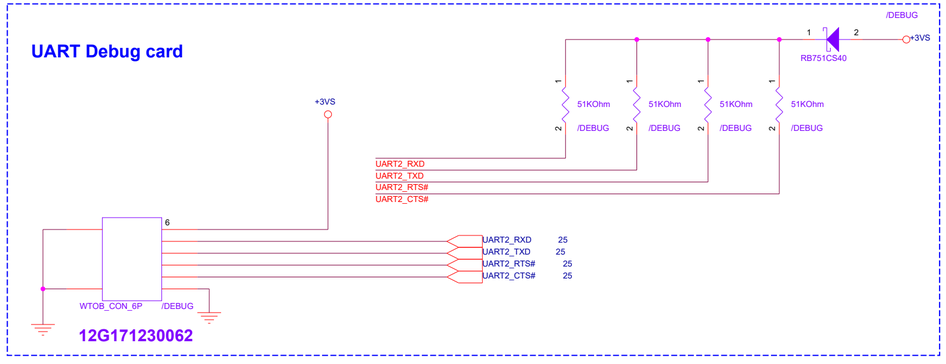
2 nd NGFF PCIE x4 (PCIE only)



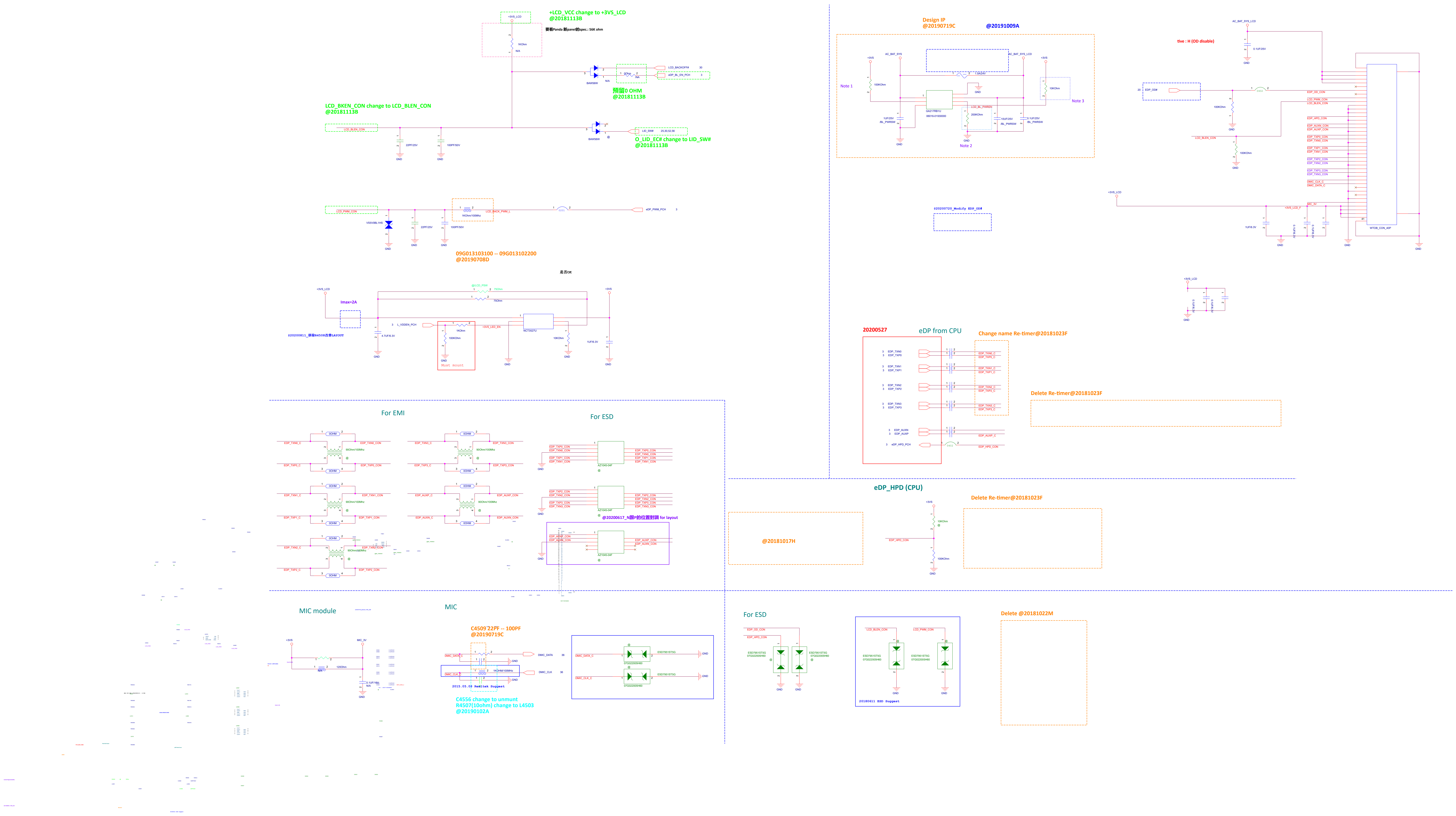
@20200702_layout空間關係調高更換J4001 H4002



Option	NGFF1_CONFIG	SSD_DET1
PCIE SSD	1	0
SATA SSD	0	1



Jigboard4 debug guide
DIP SW to 0000 : BIOS Flash
DIP SW to 0010 : Keyboard CONN Port80
DIP SW to 1000 : SMBUS CONN Port80 BIOS DUMP(by Postcode monitor)


+LCD_VCC change to +3VS_LCD
@20181113B
LCD_BKEN_CON change to LCD_BLEN_CON
@20181113B
預留0 OHM
@20181113B
O_LID_EC# change to LID_SW#
@20181113B
09G013103100 -- 09G013102200
@20190708D
Imax=2A
For EMI
For ESD
MIC module
MIC
C4509 22PF -- 100PF
@20190719C
C4556 change to unmount
R4507(10ohm) change to L4503
@20190102A
Design IP
@20190719C
@20191009A
Note 1
Note 2
Note 3
20200527
eDP from CPU
Change name Re-timer@20181023F
Delete Re-timer@20181023F
eDP_HPD (CPU)
Delete Re-timer@20181023F
@20181017H
For ESD
Delete @20181022M

Main Board

HDMI Active-Level Shift

From HDMI Switch

+1V8_AON -- 3VS
@20190722A

Q4801只用07G005107010 Vth 1.5V Ciss 13pF與07G005905021 Vth 1.5V Ciss 7.8pF

Add
@20190829C

D4801/4802 change to 07024-00880000
@20190705C

Delete C4820 C4828
@20190626E

HDMI PWR_+5VS_HDMI

HDMI Conn.

12022-00130800

HDMI EMI

Add Co-lay device
@20190626E

HDMI HPD

D0	CH1	CH2	FUNCTION
L	-	-	Switch Disabled, All Channel Hi-Z.
H	L	L	Channel 0 Enabled. Channel 1 Hi-Z.
H	L	H	Channel 0 Hi-Z. Channel 1 Enabled.
H	H	L	Channel 0 Enabled. Channel 1 Enabled.

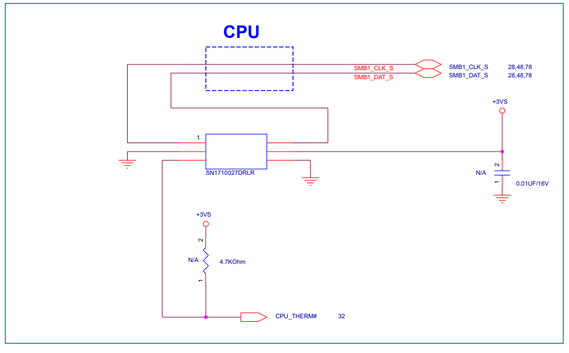
eDP0	eDP1
0	1

Main Board

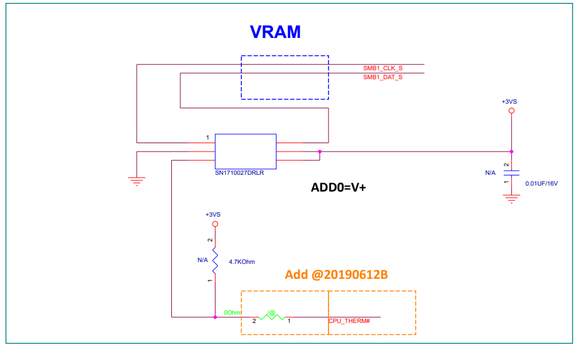
Thermal Sensor : SN170027

Pin function Supply voltage.: 1.62 V to 3.6 V

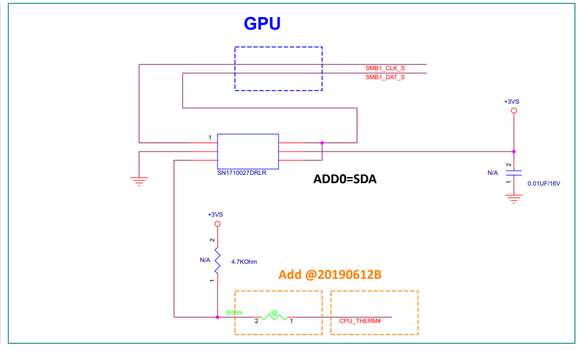
@20200728_Modify thermal Del. 0 ohm



SMBUS addr=10010000 (90)



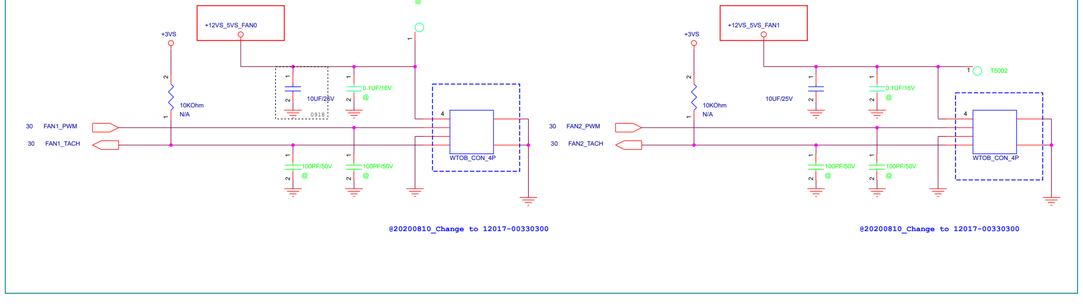
Near VRAM



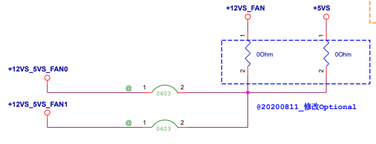
Near GPU

SMBUS addr=10010010 (92)

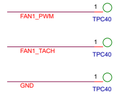
CPUGPU FAN

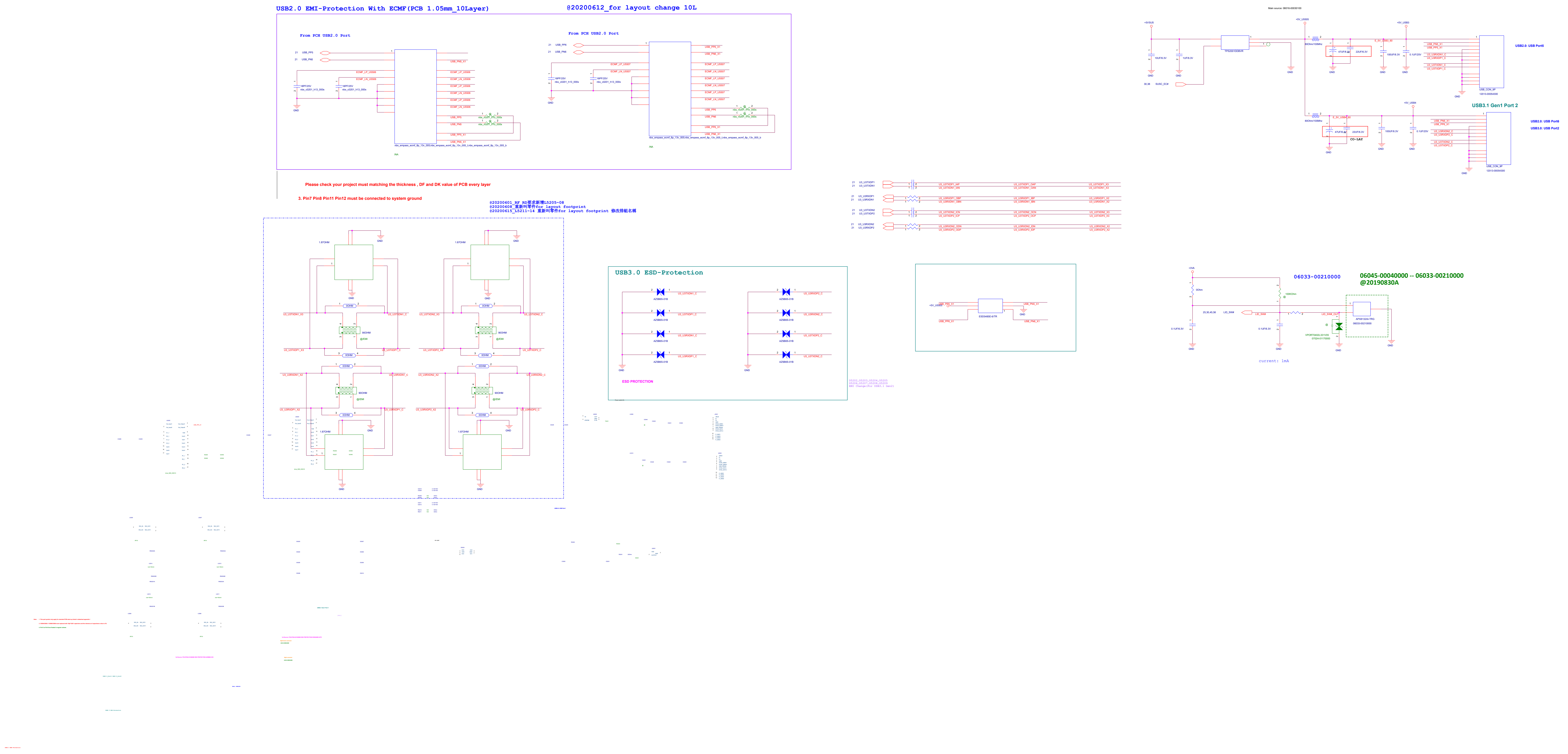


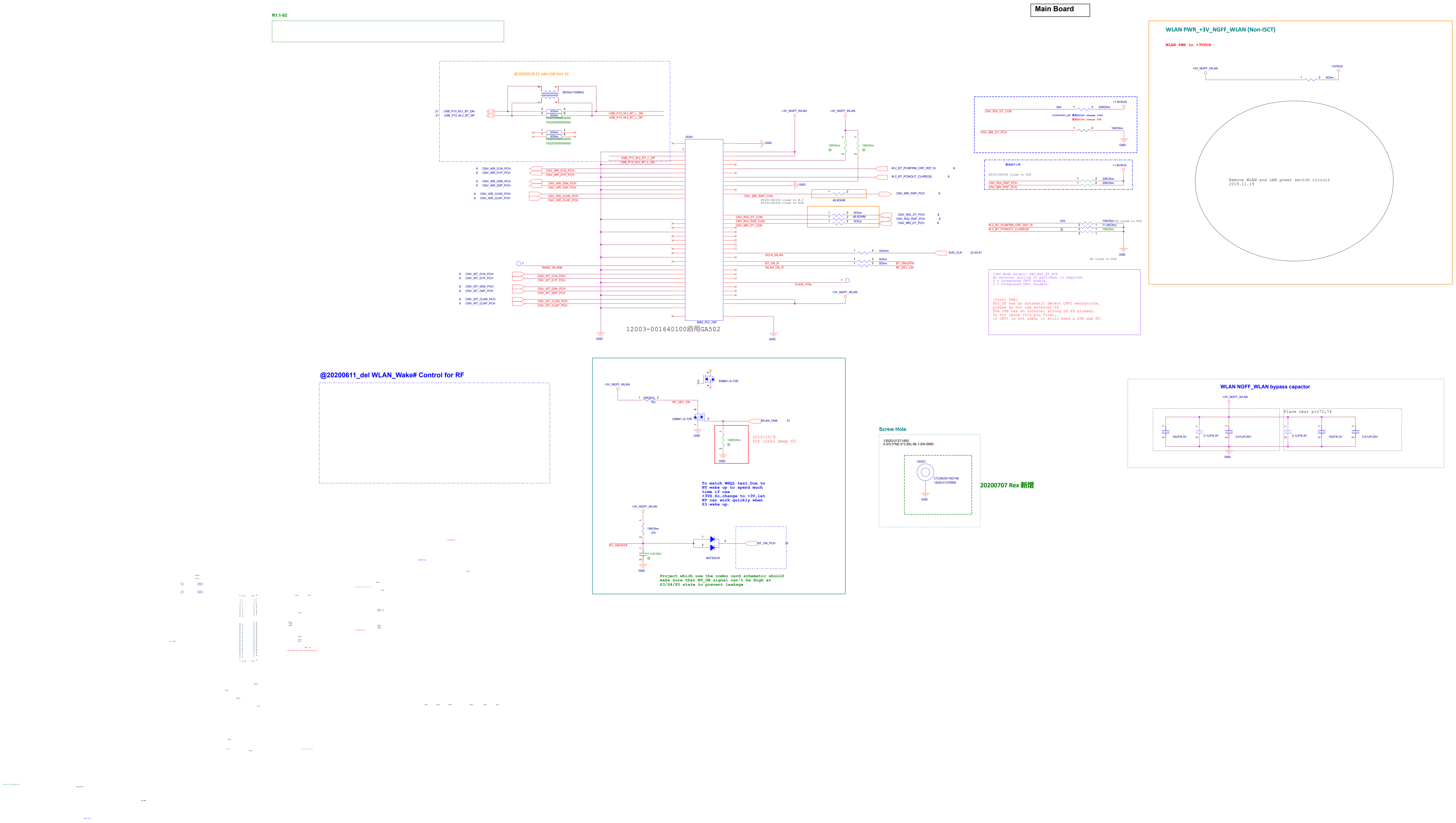
DEVICE TWO-WIRE ADDRESS		ADD0 PIN CONNECTION	Output
1001000	90	Ground	CPU
1001001	91	V+	VRAM
1001010	92	SDA	GPU
1001011	93	SCL	

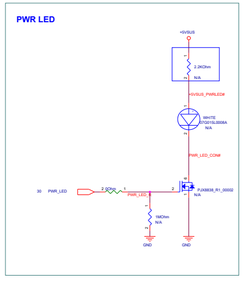


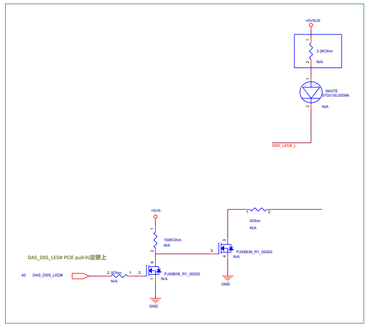
Delete TP5001 @20190619A

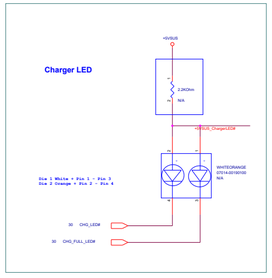


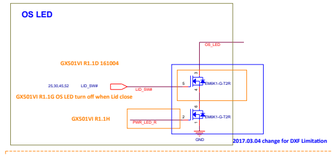

USB2.0 EMI-Protection With ECMF(PCB 1.05mm_10Layer)
@20200612_for layout change 10L
From PCH USB2.0 Port
From PCH USB2.0 Port
Please check your project must matching the thickness , DF and DK value of PCB every layer
3. Pin7 Pin8 Pin11 Pin12 must be connected to system ground
USB3.0 ESD-Protection
ESD PROTECTION
USB3.1 Gen1 Port 2
USB2.0 USB Port6
06033-00210000
06045-00040000 -- 06033-00210000
@20190830A
current: 1mA

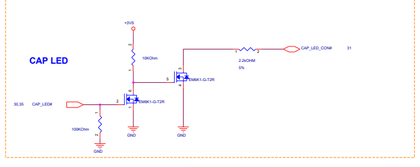

Main Board
R1.1-02
@20200528 EE add USB Port 10
WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)
WLAN PWR to +3VSUS
Remove WLAN and LAN power switch circuit
2019.11.19
12003-001640100沿用GA502
@20200611_del WLAN_Wake# Control for RF
WLAN NGFF_WLAN bypass capacitor
Screw Hole
20200707 Rex 新增
2012/10/9
for intel deep S3
To match WHQL test.Due to
BT wake up to spend much
time if use
+3VS.So,change to +3V,let
BT can work quickly when
S3 wake up.
Project which use the combo card schematic should
make sure that BT_ON signal can't be High at
S3/S4/S5 state to prevent leakage

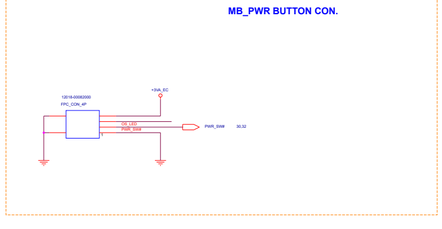










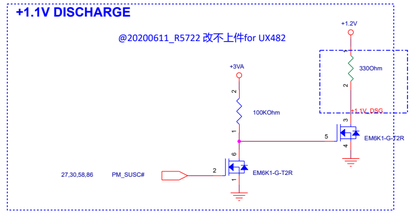


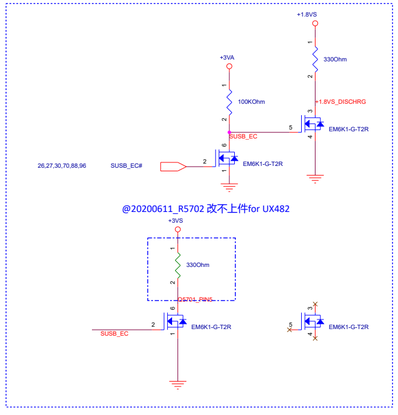
@20190731C

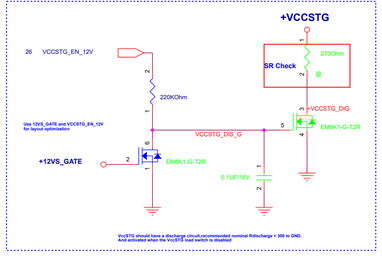
FP No	GA502 FP Pwrbtn	GA502 小板	GA502 小板 pin No
10	LED+	LED+	4
9	LED-	LED-	3
8	PWRBTN	PWRBTN	2
7	GND	GND	1
6	USB_D-	-	-
5	USB_D+	-	-
4	GND	-	-
3	SSO	-	-
2	ATC	-	-
1	RESETn	-	-

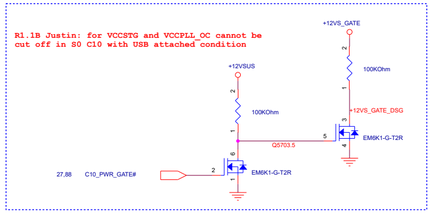
Main Board

Justin : Removed no used Discharge circuit
1.8V ,VCCIO,+5VS load switch already build in 180~260 ohm discharge function



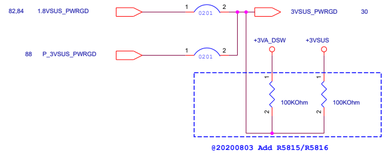




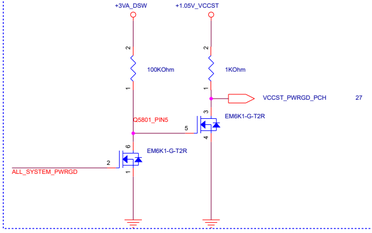


Main Board

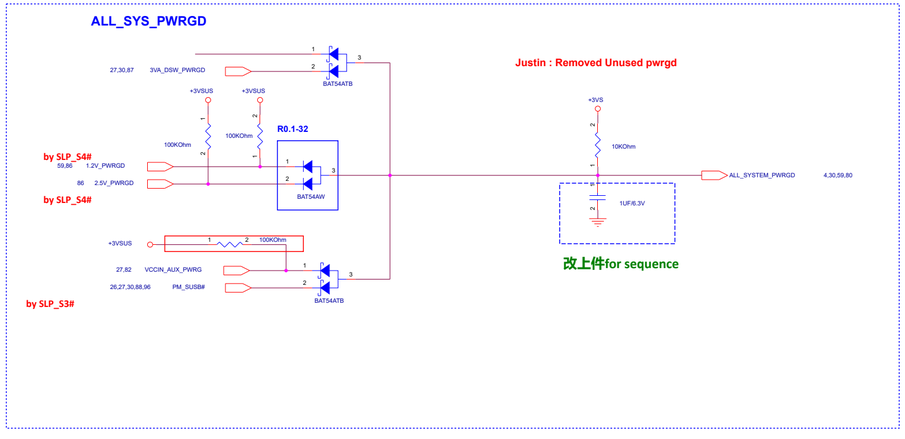
3VSUS_PWRGD

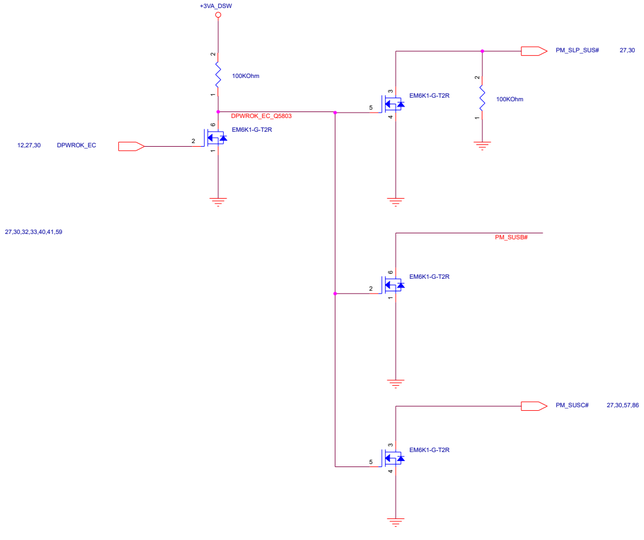


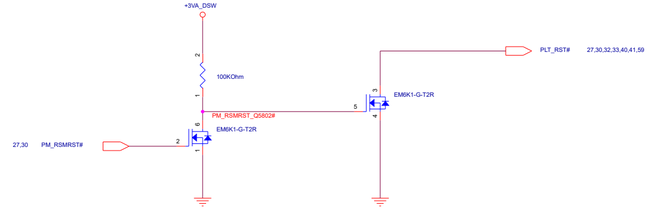
VCCST_PWRGD



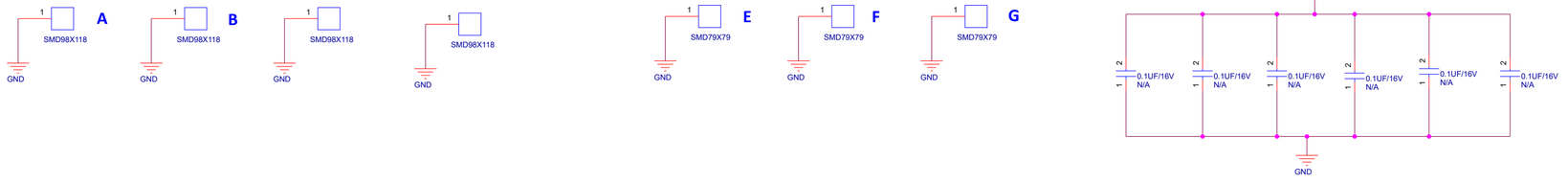
ALL_SYS_PWRGD



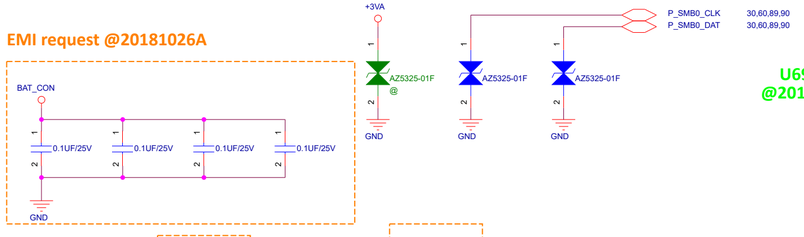




SMT EMI GASKET 2*1.5*2 13040-00850100



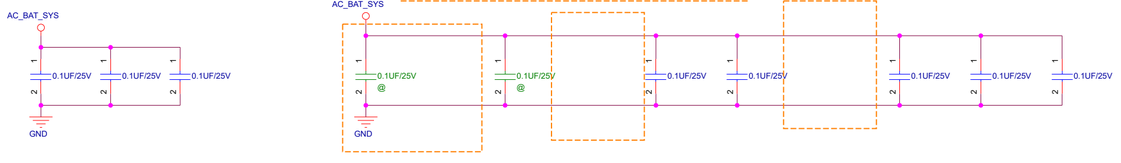
EMI request @20181026A



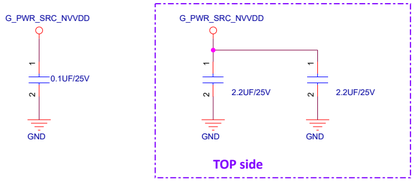
P_SMB0_CLK 30,60,89,90
P_SMB0_DAT 30,60,89,90

U6904, U6908(改裸銅), U6905(改裸銅) 移除
@20181122C

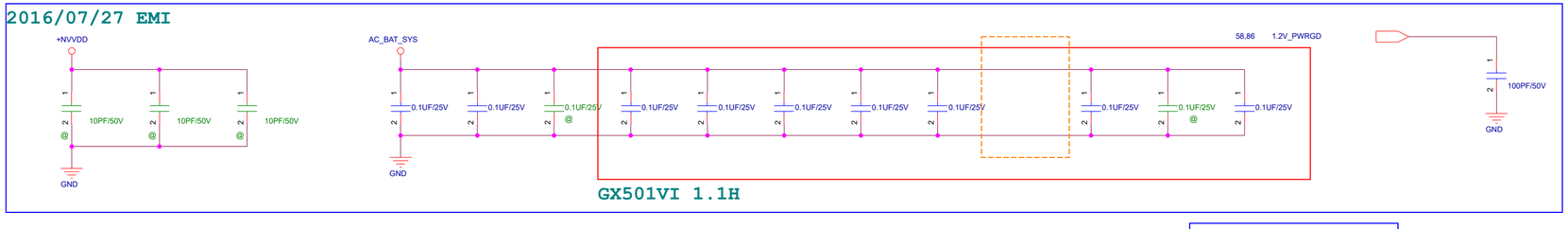
2017/04/05 EMI

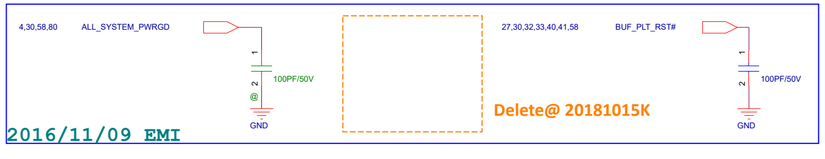


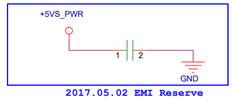
4/2 for EMI



2016/07/27 EMI

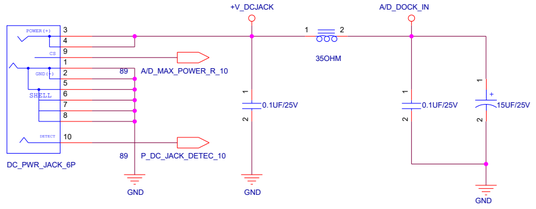






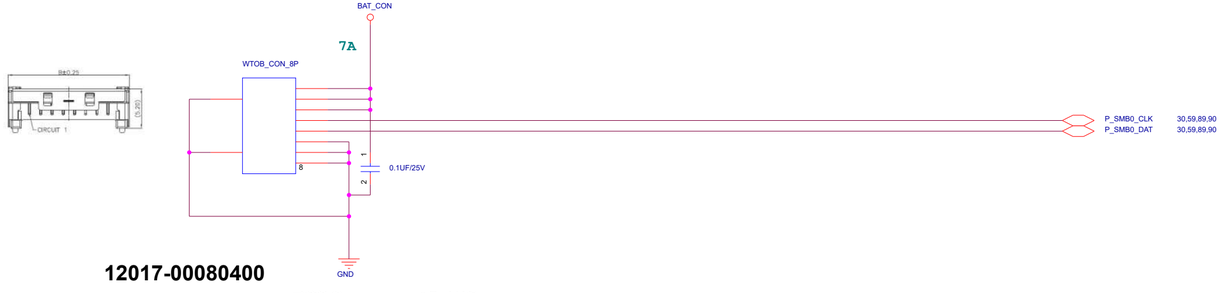
DC-IN Connector

使用請詢用River_Hsu



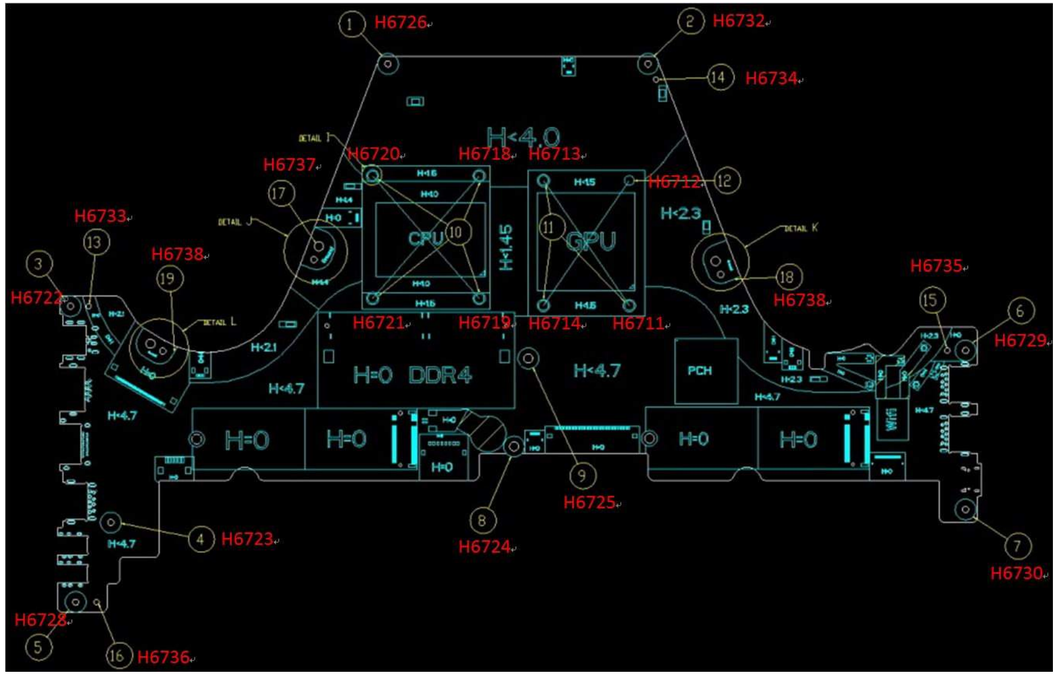
	3.4CH	1.55CH
J6001		

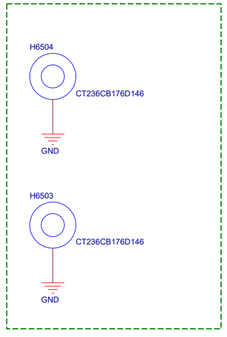
Battery Connector

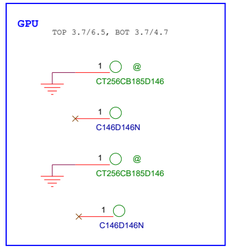


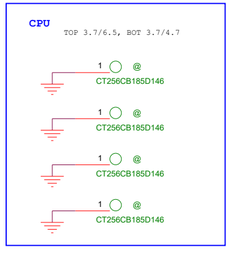
12017-00080400

正確性與BAT1_IN_OC#是否預留!

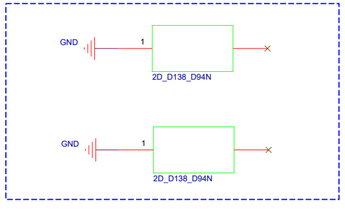


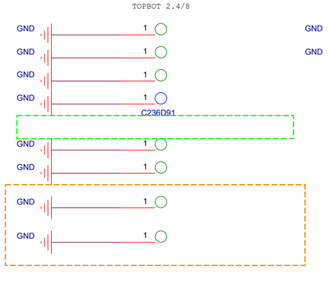




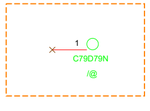


@20200707_Modify H6533H6535





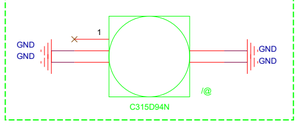
Add @20181029C

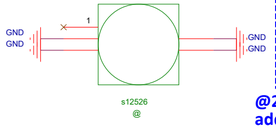


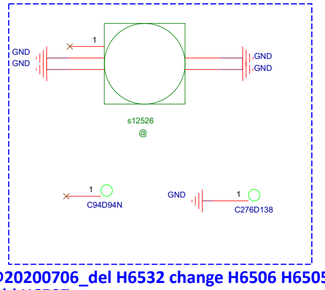
Change @20181023F

NC @20181030B

Change @20181023F

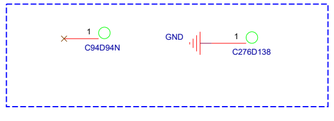






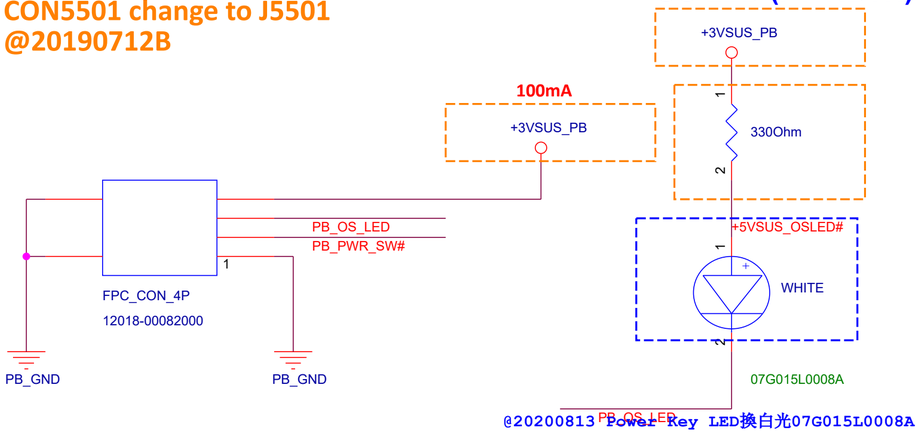
@20200706_del H6532 change H6506 H6505
add H6507

change H6501 H6502



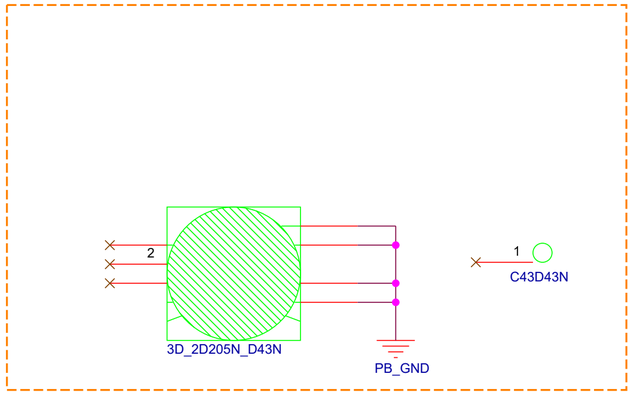
CON5501 change to J5501
@20190712B

OS LED (PWRBTN)



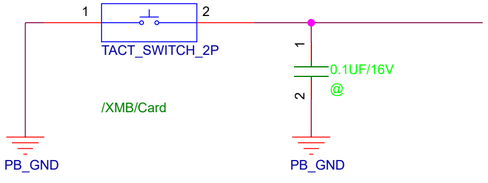
~~@20200813 Power Key LED換白光07G015L0008A~~

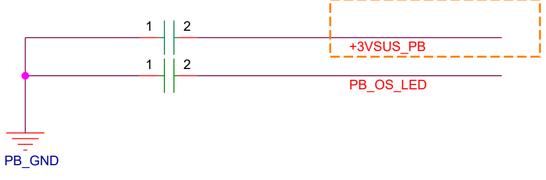
+5VSUS_PB -- +3VSUS_PB
R5510 750 OHM -- 330 OHM
@20190708A

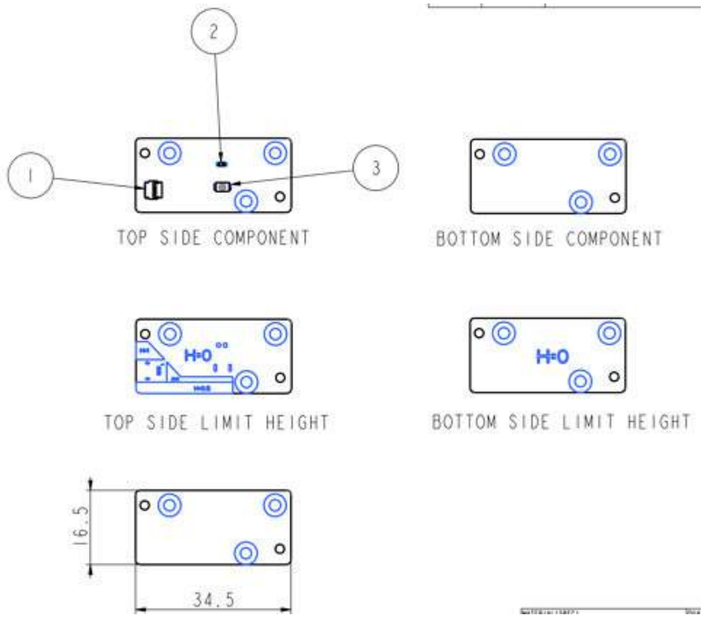


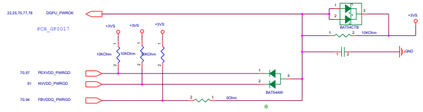
Vinafix.com

POWER button

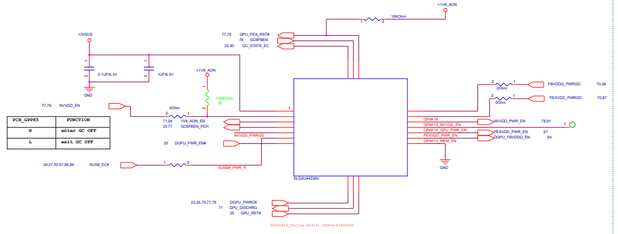


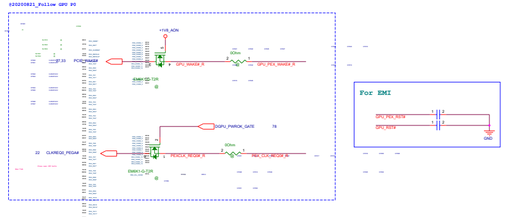


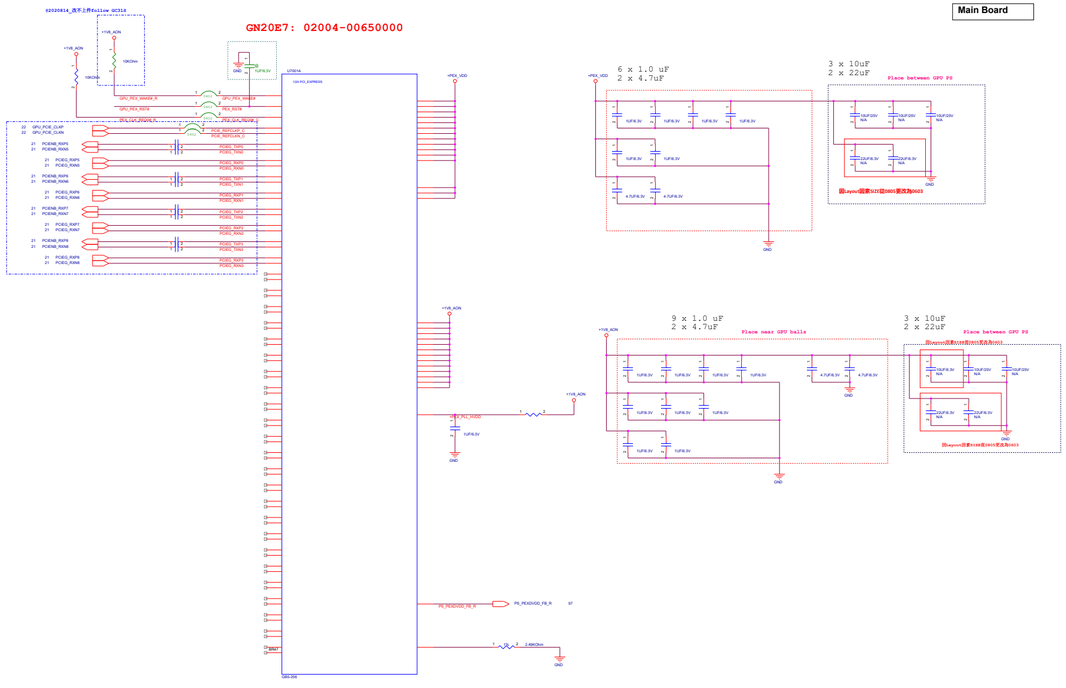


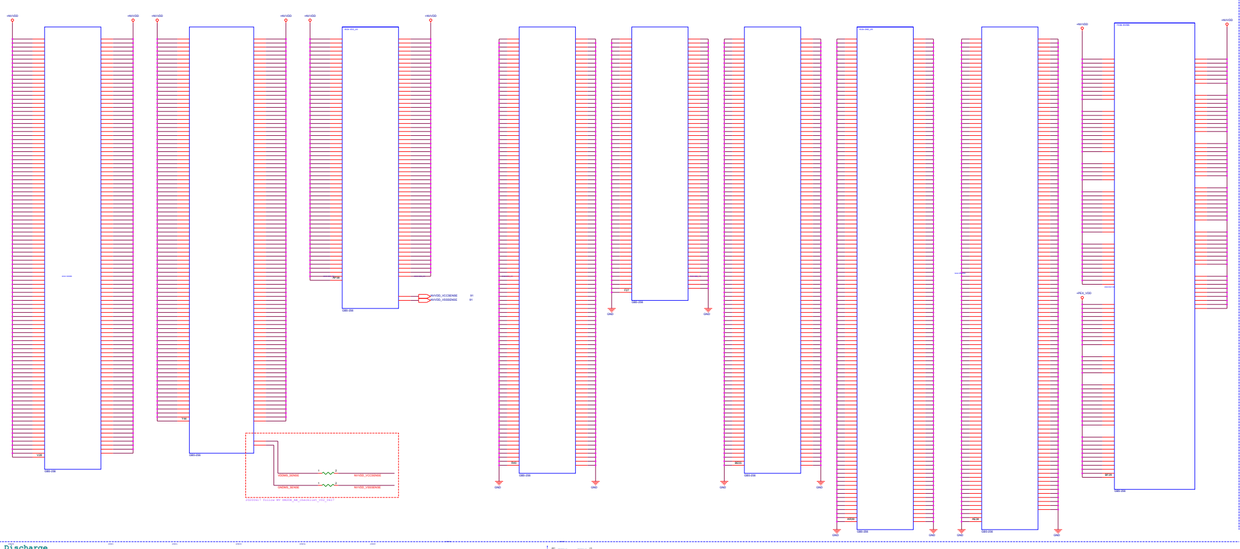


GPU POWER SEQUENCE CONTROL

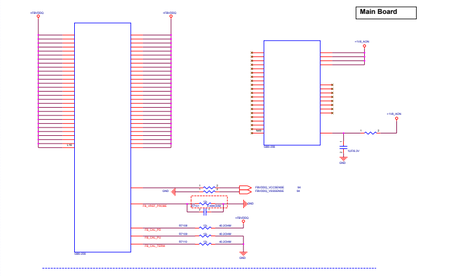




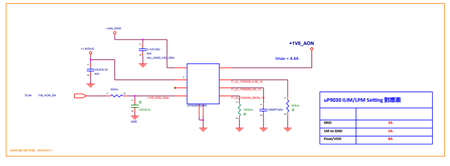




Main Board

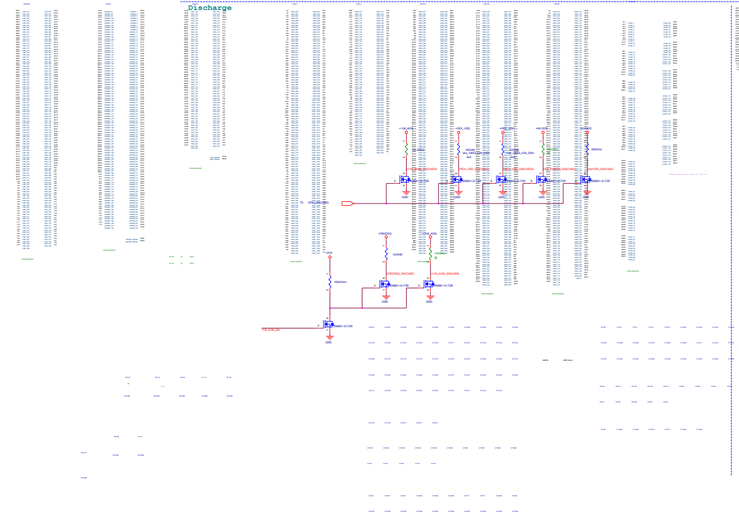


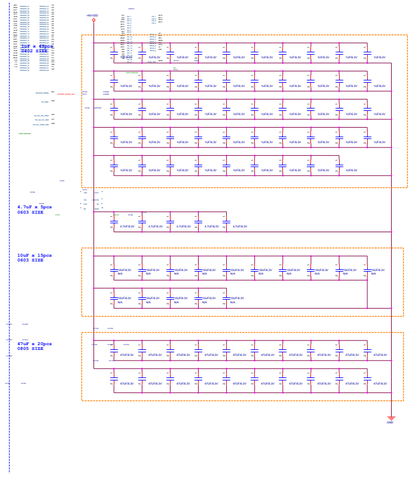
1V8 Power Control



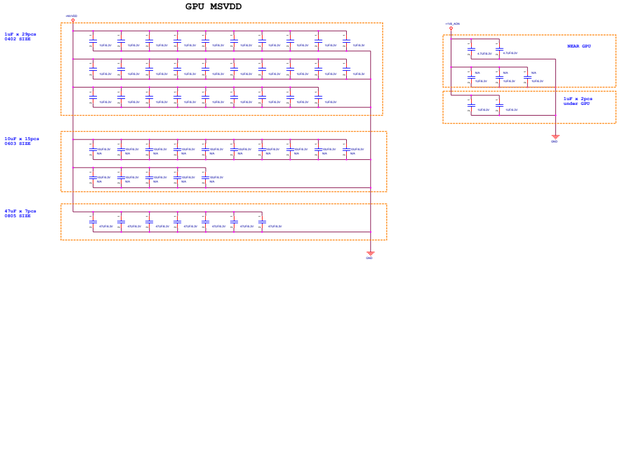
GND	NA
5K to GND	NA
Floating	NA

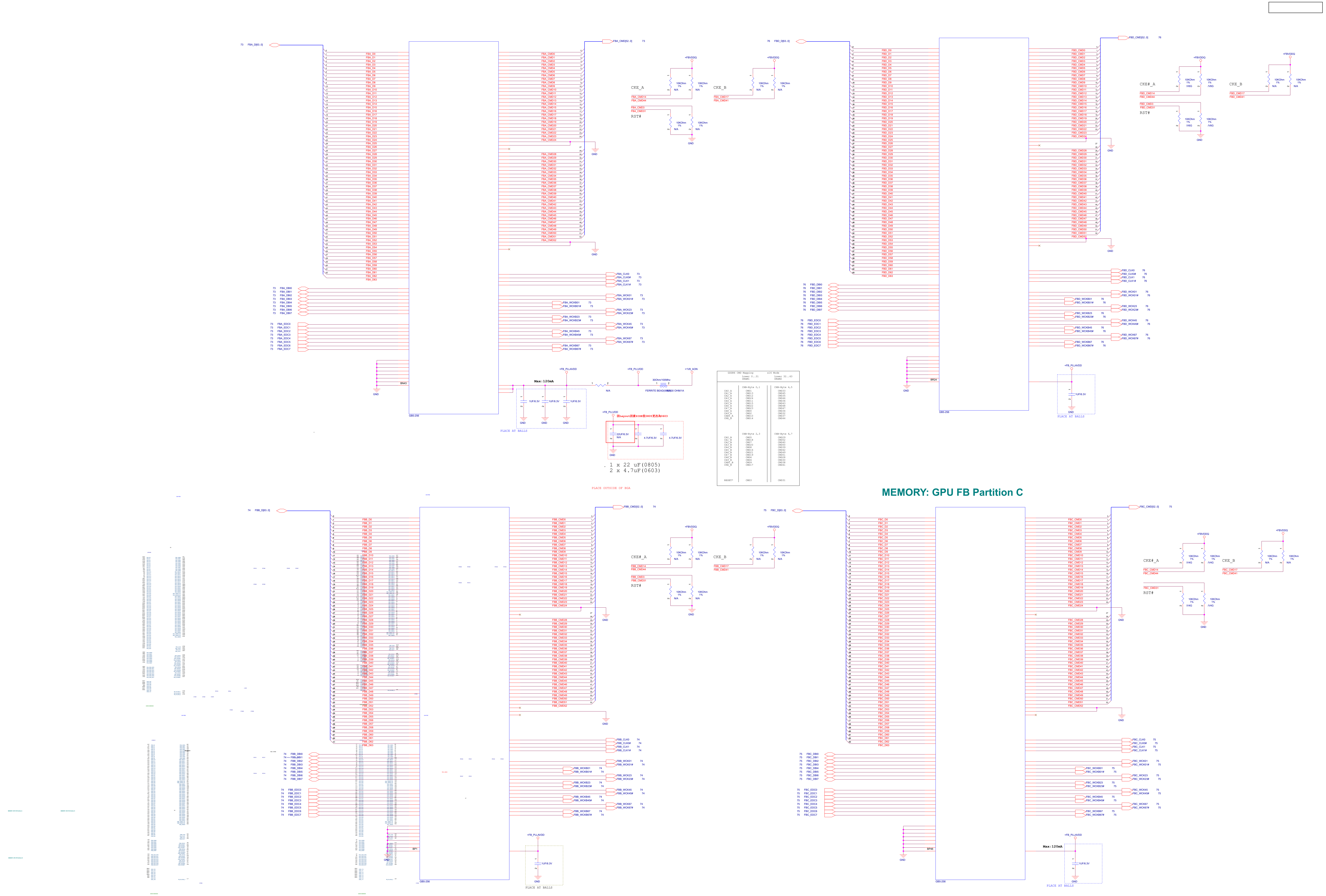
Discharge





GPU MSVDD





MEMORY: GPU FB Partition C

Samsung_256*32_K4Z80325BC : 03014-00010600(目前
Micron_256M*32_MT61K256M32JE: 03014-00010500

40 OHm_NET
FBA Partition 31..0
MF=1 Mirror

72 FBA_D[31..0]
72 FBA_CMD[52..0]

+FBVDDQ

FBA_D9
FBA_D8
FBA_D13
FBA_D10
FBA_D14
FBA_D11
FBA_D15
FBA_D12
FBA_D24
FBA_D27
FBA_D25
FBA_D30
FBA_D26
FBA_D28
FBA_D29

FBA_CMD1
FBA_CMD13
FBA_CMD12
FBA_CMD24
FBA_CMD11
FBA_CMD15
FBA_CMD22
FBA_CMD23
FBA_CMD0
FBA_CMD2
FBA_CMD10
FBA_CMD14

72 FBA_DBI1
72 FBA_DBI3
72 FBA_WCKB01
72 FBA_WCKB01#
72 FBA_EDC1
72 FBA_EDC3

MEM_VPP

FBA_D4
FBA_D2
FBA_D6
FBA_D5
FBA_D7
FBA_D0
FBA_D3
FBA_D1
FBA_D17
FBA_D21
FBA_D16
FBA_D18
FBA_D19
FBA_D20
FBA_D22
FBA_D23

FBA_CMD5
FBA_CMD18
FBA_CMD7
FBA_CMD20
FBA_CMD8
FBA_CMD16
FBA_CMD21
FBA_CMD19
FBA_CMD6
FBA_CMD4
FBA_CMD9
FBA_CMD17

72 FBA_DBI0
72 FBA_DBI2
72 FBA_WCK23
72 FBA_WCK23#
72 FBA_EDC0
72 FBA_EDC2
72 FBA_CLK0#
72 FBA_CLK0
K10
FBA_CMD3

GND
FBA_WCKB23 72
FBA_WCKB23# 72
FBA_WCK01 72
FBA_WCK01# 72

121Ohm 2 1% 1 /GPU_KA FBA_ZQ_1A GND
121Ohm 2 1% 1 /GPU_KA FBA_ZQ_1B GND

FBA_VREFC_L
1KOhm 1% /GPU_KA
GND

MT61K256M32JE-14:A
/VRAM

40 OHm_NET
FBA Partition 64..32
MF=0 Normal

72 FBA_D[63..32]

+FBVDDQ

FBA_D41
FBA_D40
FBA_D42
FBA_D44
FBA_D47
FBA_D46
FBA_D43
FBA_D45
FBA_D60
FBA_D61
FBA_D62
FBA_D58
FBA_D63
FBA_D59
FBA_D57
FBA_D56

FBA_CMD33
FBA_CMD45
FBA_CMD35
FBA_CMD46
FBA_CMD36
FBA_CMD43
FBA_CMD48
FBA_CMD47
FBA_CMD34
FBA_CMD32
FBA_CMD37
FBA_CMD44

72 FBA_DBI5
72 FBA_DBI7
72 FBA_WCKB45
72 FBA_WCKB45#
72 FBA_EDC5
72 FBA_EDC7

MEM_VPP

FBA_D32
FBA_D33
FBA_D36
FBA_D39
FBA_D34
FBA_D38
FBA_D35
FBA_D37
FBA_D55
FBA_D48
FBA_D53
FBA_D49
FBA_D54
FBA_D51
FBA_D52
FBA_D50

FBA_CMD29
FBA_CMD52
FBA_CMD40
FBA_CMD50
FBA_CMD39
FBA_CMD42
FBA_CMD49
FBA_CMD51
FBA_CMD28
FBA_CMD30
FBA_CMD38
FBA_CMD41

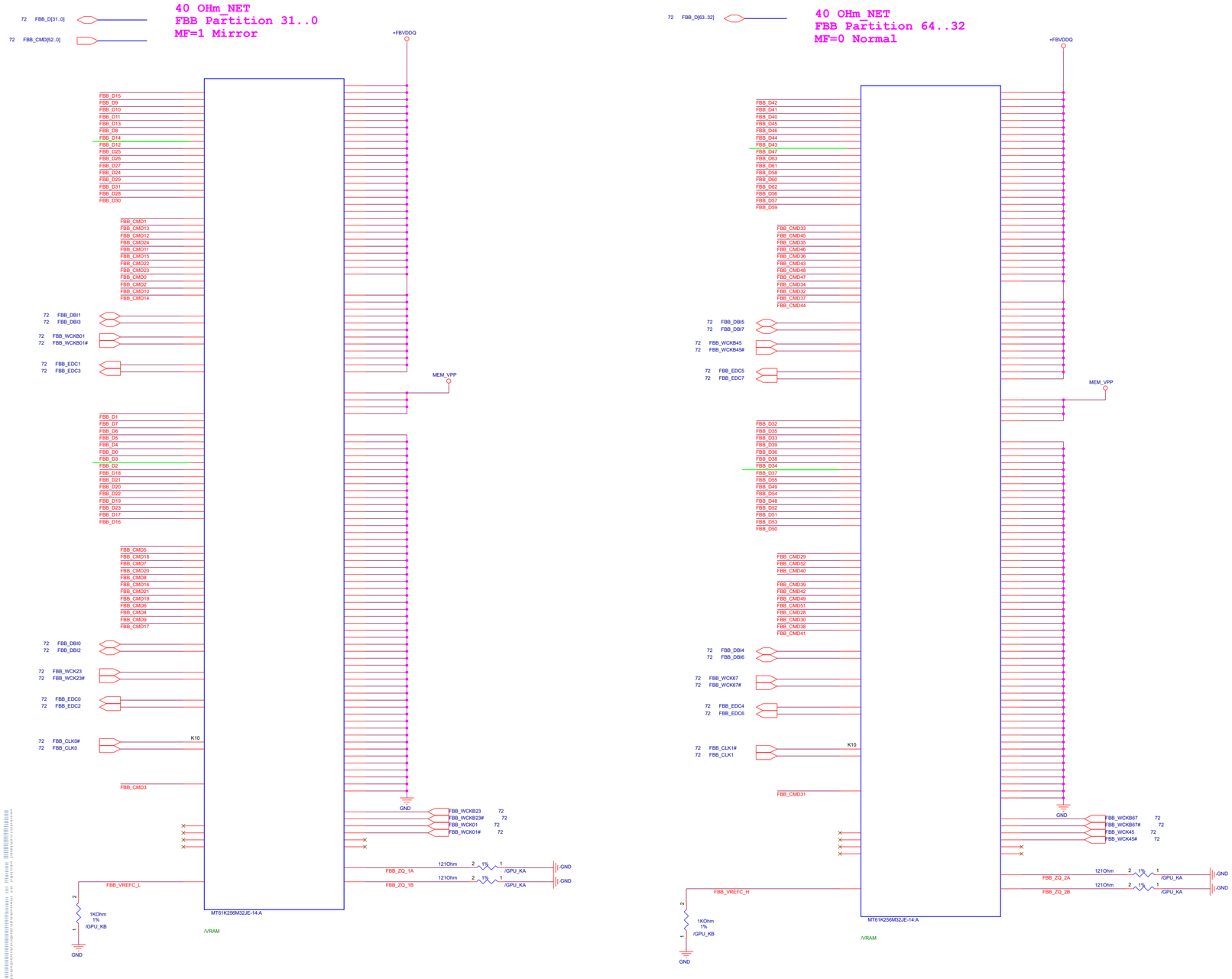
72 FBA_DBI4
72 FBA_DBI6
72 FBA_WCK67
72 FBA_WCK67#
72 FBA_EDC4
72 FBA_EDC6
72 FBA_CLK1#
72 FBA_CLK1
K10
FBA_CMD31

GND
FBA_WCKB67 72
FBA_WCKB67# 72
FBA_WCK45 72
FBA_WCK45# 72

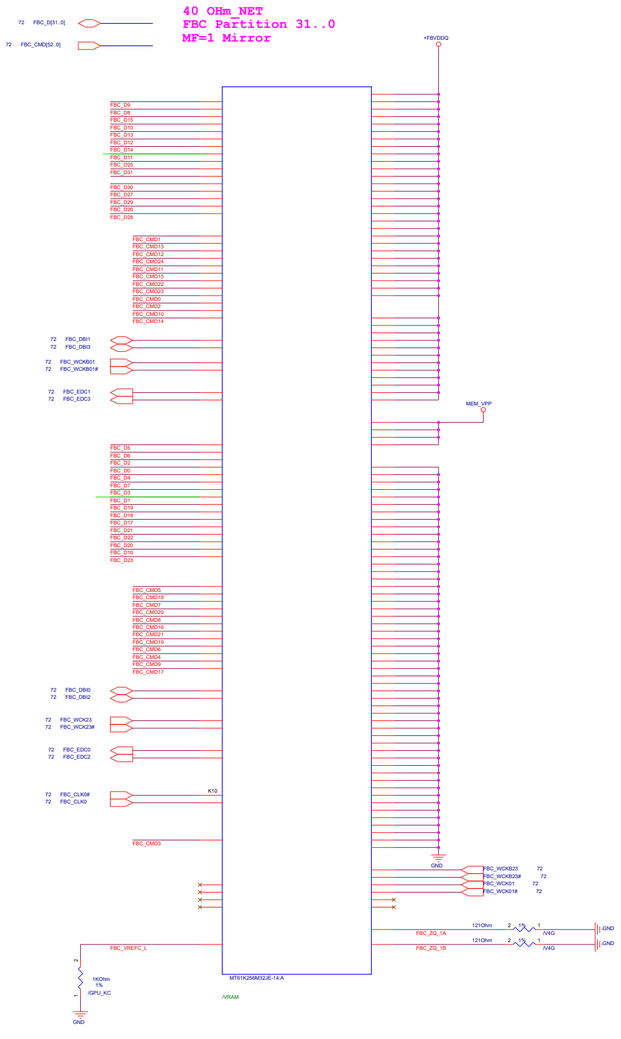
121Ohm 2 1% 1 /GPU_KA FBA_ZQ_2A GND
121Ohm 2 1% 1 /GPU_KA FBA_ZQ_2B GND

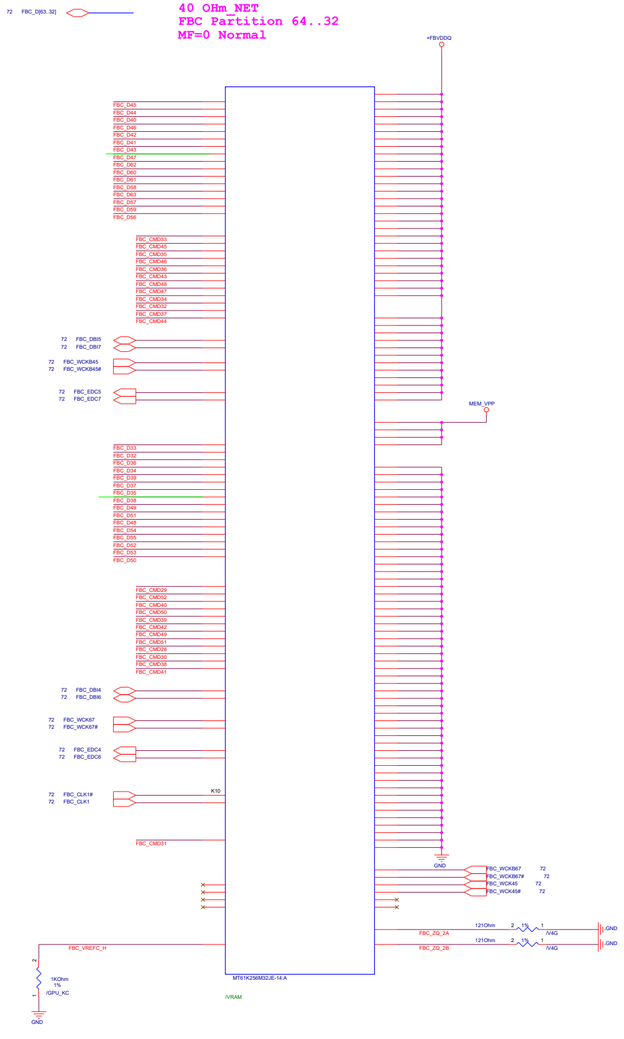
FBA_VREFC_H
1KOhm 1% /GPU_KA
GND

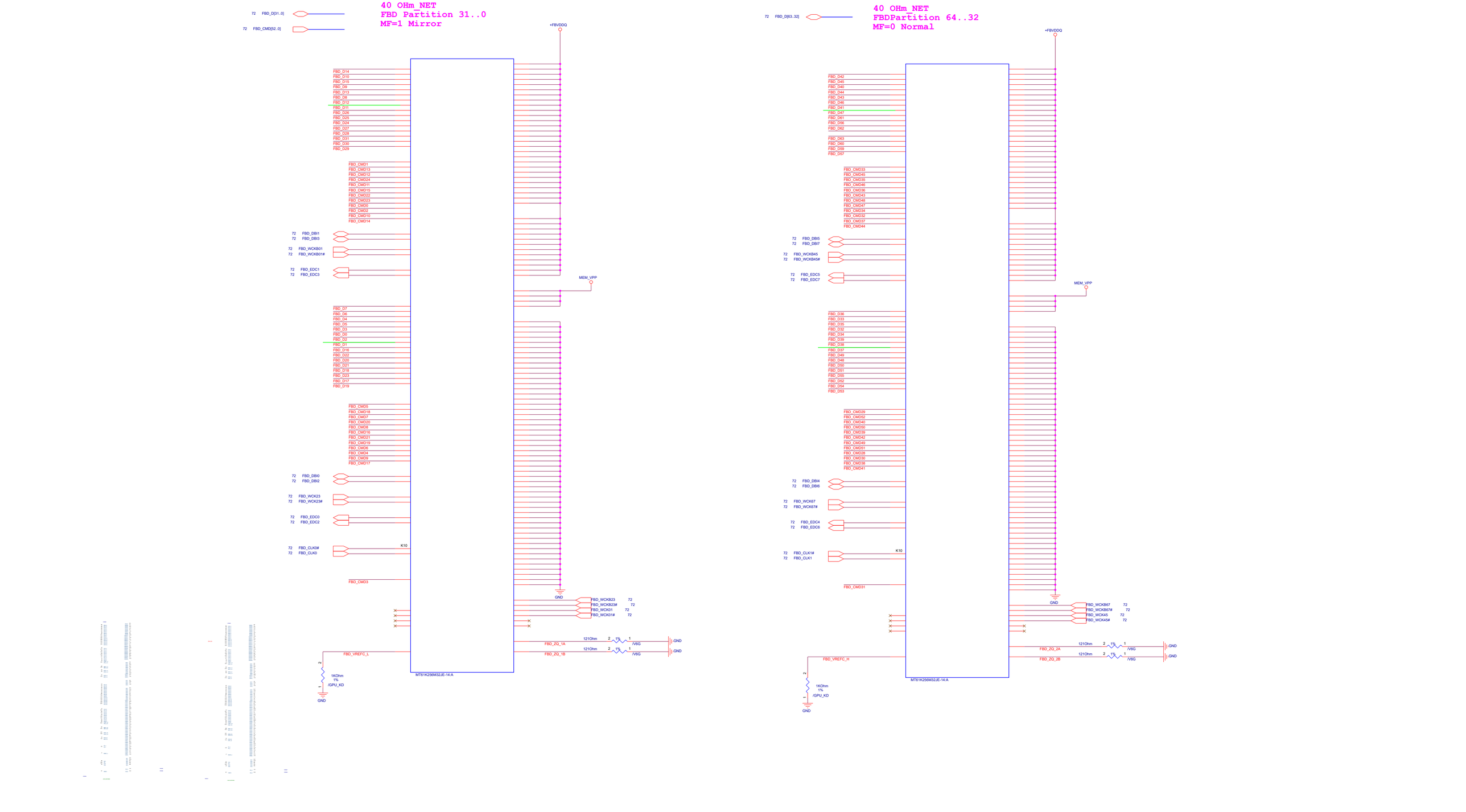
MT61K256M32JE-14:A
/VRAM


40 OHm_NET
FBB Partition 31..0
MF=1 Mirror
72 FBB_D[31..0]
72 FBB_CMD[52..0]
+FBVDDQ
MEM_VPP
GND
K10
MT61K256M32JE-14:A
/VRAM
FBB_VREFC_L
1KOhm
1%
/GPU_KB
121Ohm
/GPU_KA
FBB_ZQ_1A
FBB_ZQ_1B
40 OHm_NET
FBB Partition 64..32
MF=0 Normal
72 FBB_D[63..32]
FBB_VREFC_H
FBB_ZQ_2A
FBB_ZQ_2B

Samsung_256*32_K4Z80325BC : 03014-00010600(目前
Micron_256M*32_MT61K256M32JE: 03014-00010500






40 OHm_NET
FBD Partition 31..0
MF=1 Mirror
72 FBD_D[31..0]
72 FBD_CMD[52..0]
+FBVDDQ
MEM_VPP
GND
K10
MT61K256M32JE-14:A
FBD_VREFC_L
1KOhm
1%
/GPU_KD
FBD_ZQ_1A
FBD_ZQ_1B
121Ohm
/V6G
40 OHm_NET
FBDPartition 64..32
MF=0 Normal
72 FBD_D[63..32]
FBD_VREFC_H
FBD_ZQ_2A
FBD_ZQ_2B

FBVDDQ
VRAM side

GPU side

Channel A

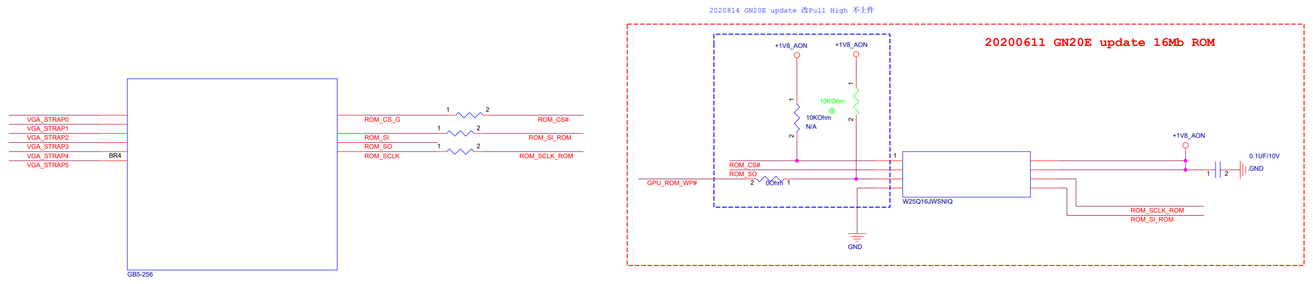
Channel C

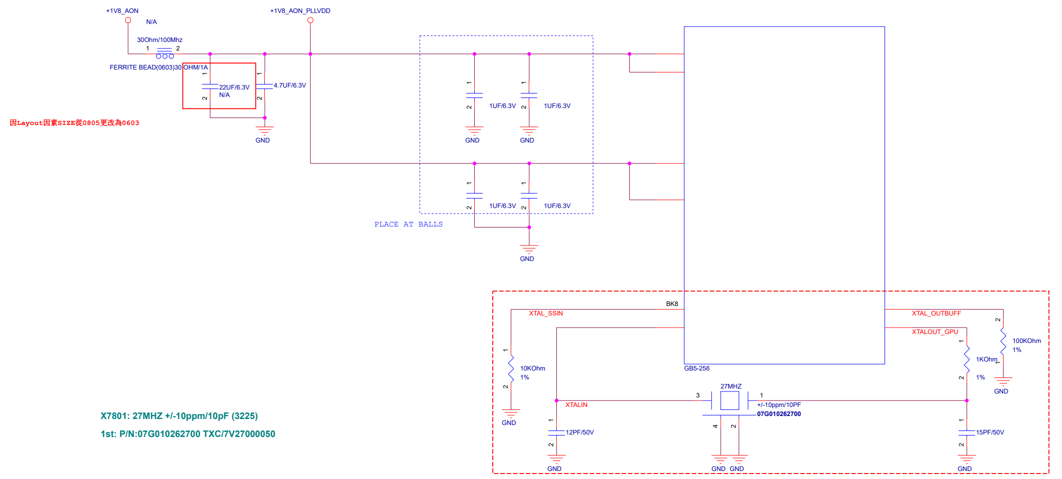
Channel D

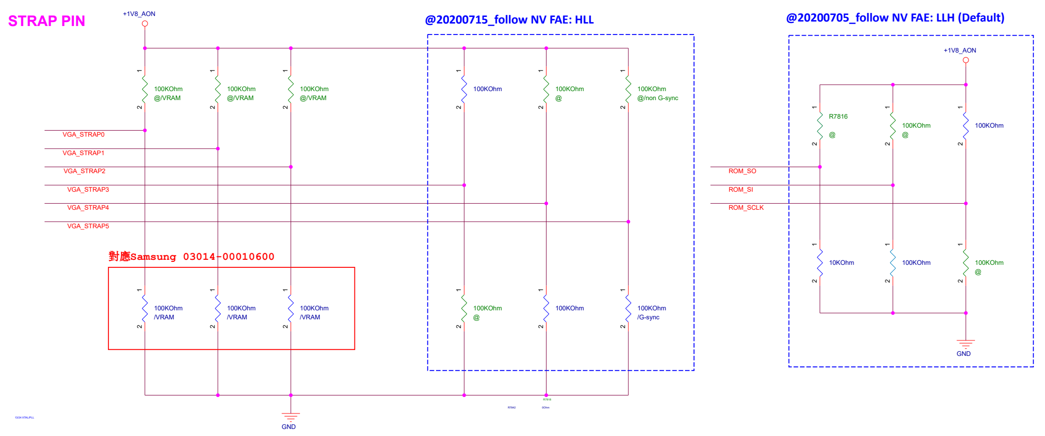
Close to DRAM

Around DRAM

For power sequence measurement





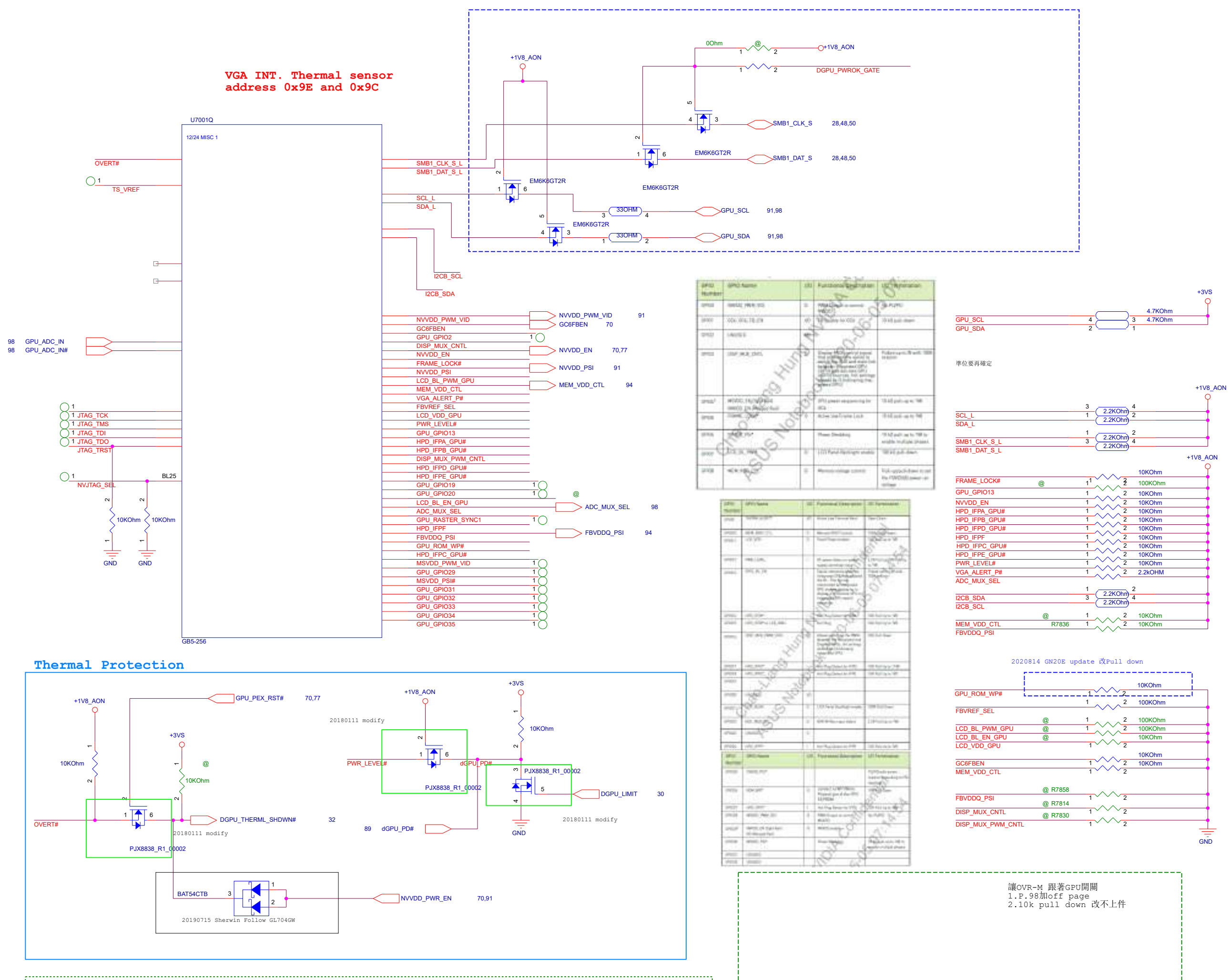


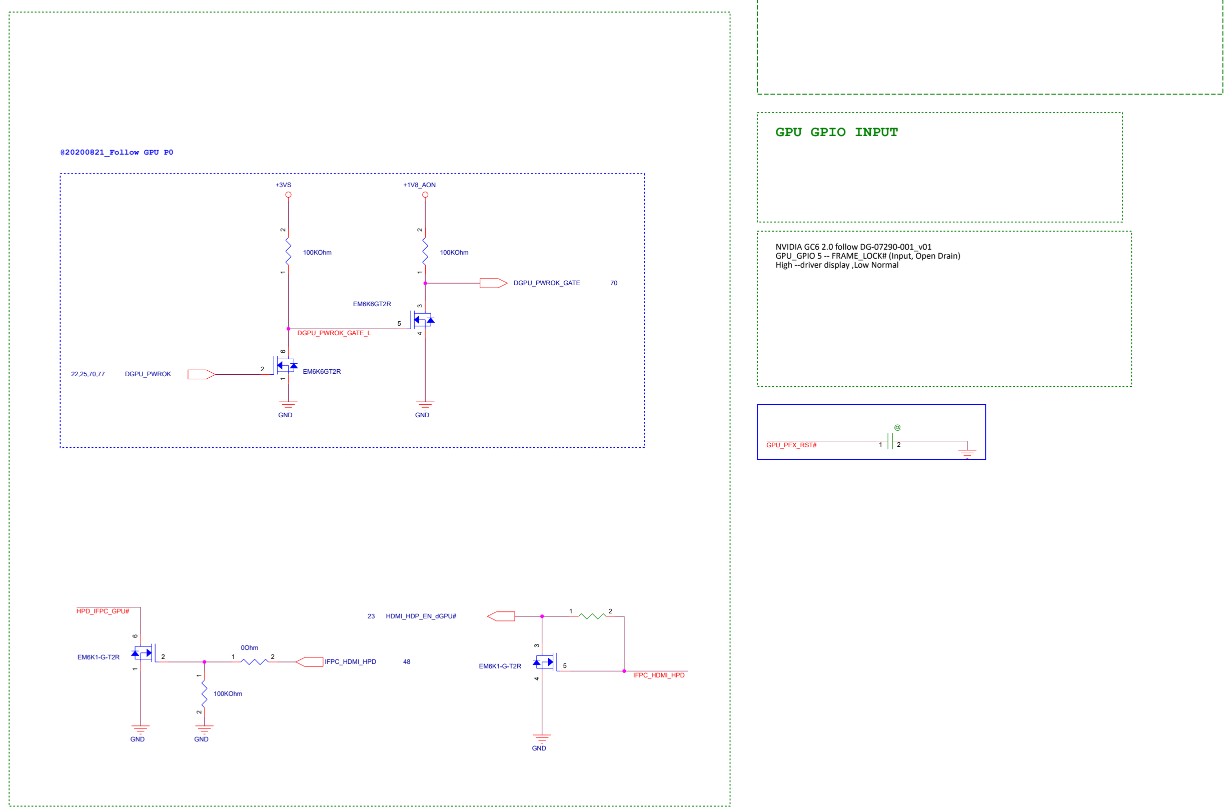
	Physical Configuration	
Level Option	Pull-Up to 1.8V via resistor (see Note 1). (Notebook designs also see Note 2.)	Pull-Down to GND via resistor Note 1
1.8V ("HIGH") Level	Populate	No Stuff
0.9V ("MIDDLE") Level	Populate	Populate
GND ("LOW") Level	No Stuff	Populate

Note 1: Resistor should be 100K Ohms. 5% tolerance is acceptable.
Note 2: Notebook graphics circuit designs should pull up to the 1V8_AON rail rather than to 1V8_MAIN.

Strap Pins see Note			FS_OVERT* Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function ENABLED
L	L	H	FS_OVERT* function DISABLED (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

DEFULT : L L L





Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

Assorted Configuration Straps

1. SMB_ALT_ADDR Enable: "0" signal GPU setting I2CS address 0x9E, "1" Dual GPU setting I2CS address add 0x9C, used when a second GPU
2. DEVID_SEL: G-sync function→"0" normal GPU ID, "1" support G-sync GPU ID
3. PCIE_CFG: PCIE Swing→"0" PCIE Swing default, "1" PCEI swing reduce
4. VGA_DEVICE: Graphics circuit→"0" MS-Hybrid, "1" Discrete

0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND

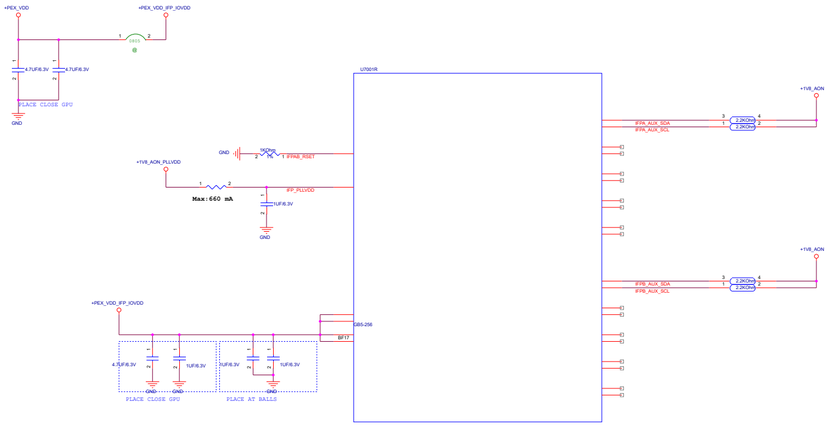
0:DEVID_SEL ORIGNAL

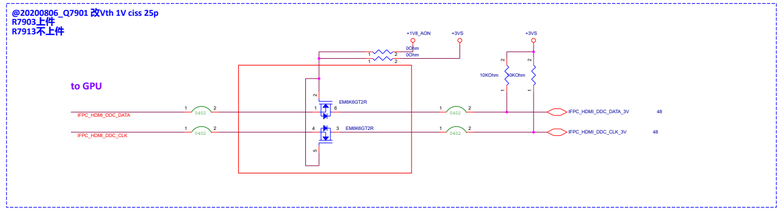
1:PCIE_CFG LOW POWER

0:PCIE_CFG HIGH POWER

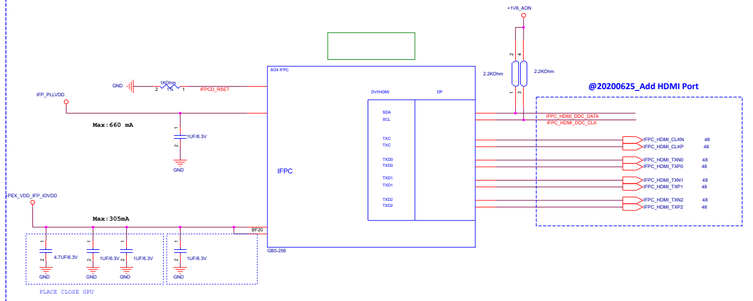
1:VGA_DEVICE ENABLE

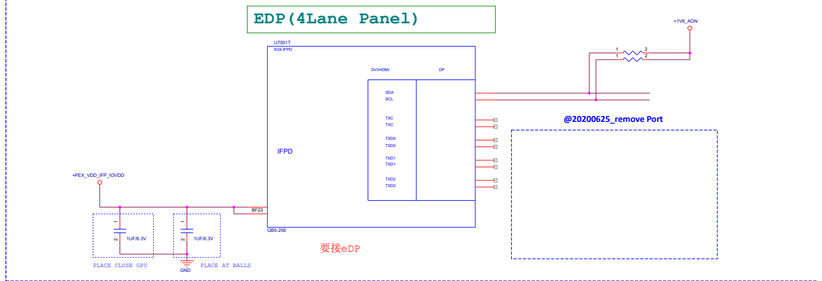
0:VGA_DEVICE DISABLE

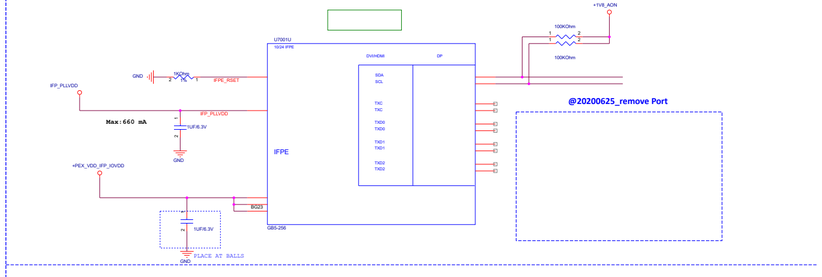

+PEX_VDD
+PEX_VDD_IFP_IOVDD
4.7UF/6.3V
4.7UF/6.3V
PLACE CLOSE GPU
GND
U7001R
+1V8_AON
IFPA_AUX_SDA
IFPA_AUX_SCL
2.2KOHM
2.2KOHM
+1V8_AON_PLLVDD
10KOhm
IFPA8_RSET
IFP_PLLVDD
Max:660 mA
1UF/6.3V
+1V8_AON
IFPB_AUX_SDA
IFPB_AUX_SCL
+PEX_VDD_IFP_IOVDD
GB5-256
BF17
4.7UF/6.3V
1UF/6.3V
1UF/6.3V
PLACE CLOSE GPU
PLACE AT BALLS

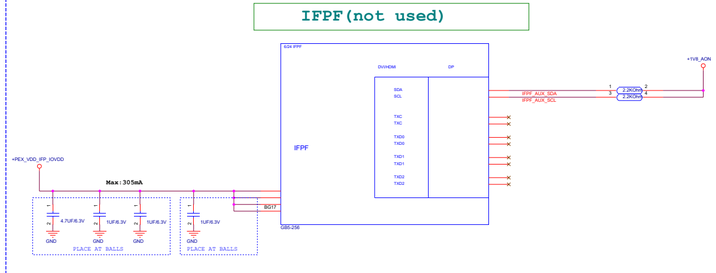

@20200806_Q7901 改Vth 1V ciss 25p
R7903上件
R7913不上件
to GPU
+1V8_AON
+3V3
0Ohm
0Ohm
10KOhm
10KOhm
EMI6K6GT2R
IFPC_HDMI_DDC_DATA
IFPC_HDMI_DDC_CLK
IFPC_HDMI_DDC_DATA_3V
IFPC_HDMI_DDC_CLK_3V
48
48

Main Board

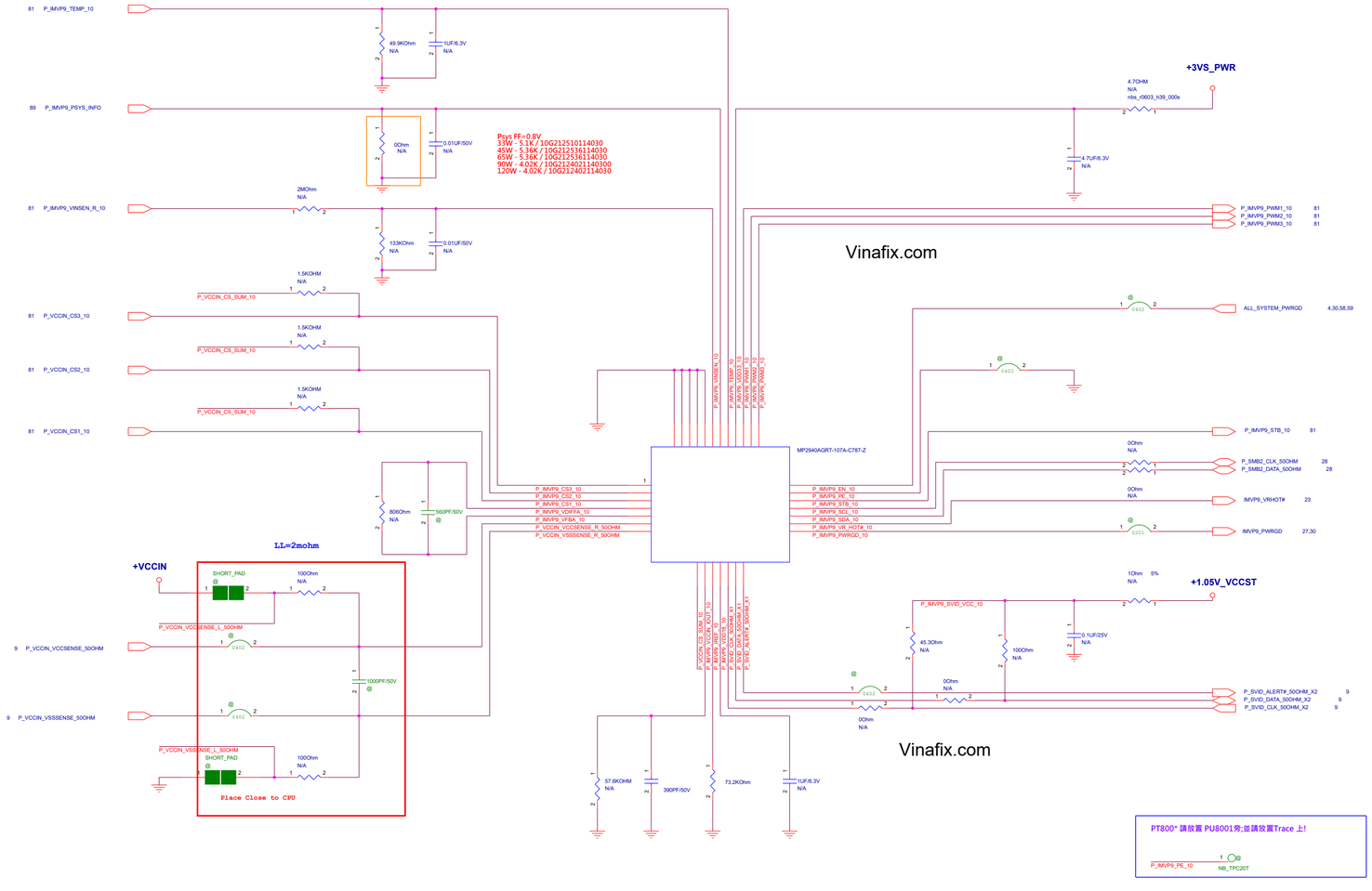

+1V8_AON
GND
10KOhm
IFPC8_RSET
IFP_PLLVDD
Max:660 mA
1UF/6.3V
2.2KOhm
2.2KOhm
@20200625_Add HDMI Port
IFPC
8G4 IFPC
DVI/HDMI
DP
SDA
SCL
TXC
TXC
TXD0
TXD0
TXD1
TXD1
TXD2
TXD2
IFPC_HDMI_DDC_DATA
IFPC_HDMI_DDC_CLK
IFPC_HDMI_CLKN
IFPC_HDMI_CLKP
IFPC_HDMI_TXN0
IFPC_HDMI_TXP0
IFPC_HDMI_TXN1
IFPC_HDMI_TXP1
IFPC_HDMI_TXN2
IFPC_HDMI_TXP2
48
+PEX_VDD_IFP_IOVDD
Max:305mA
BF20
4.7UF/6.3V
1UF/6.3V
1UF/6.3V
1UF/6.3V
GB5-256
PLACE CLOSE GPU

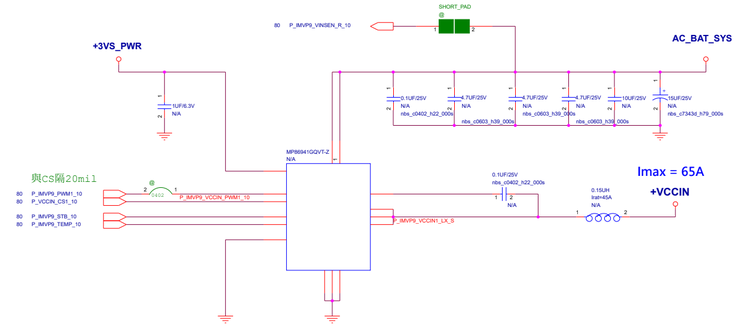

EDP(4Lane Panel)
U7001T
8G4 IFPD
DVI/HDMI
DP
IFPD
SDA
SCL
TXC
TXC
TXD0
TXD0
TXD1
TXD1
TXD2
TXD2
+1V8_AON
@20200625_remove Port
+PEX_VDD_IFP_IOVDD
BF23
1UF/6.3V
1UF/6.3V
GB5-256
PLACE CLOSE GPU
PLACE AT BALLS
要接eDP

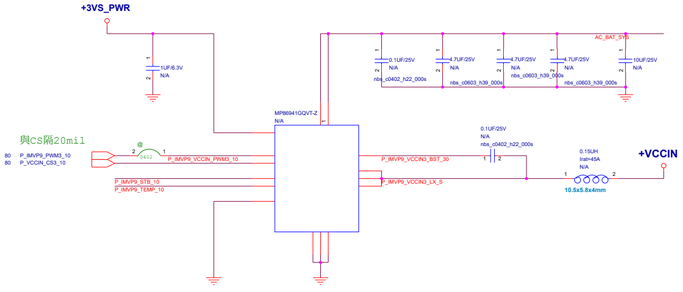

U7001U
10CK IFPE
DVI/HDMI
DP
+1V8_AON
100KOhm
100KOhm
@20200625_remove Port
GND
10KOhm
IFPE8_RSET
IFP_PLLVDD
Max:660 mA
1UF/6.3V
IFPE
+PEX_VDD_IFP_IOVDD
BG23
1UF/6.3V
GB5-256
PLACE AT BALLS

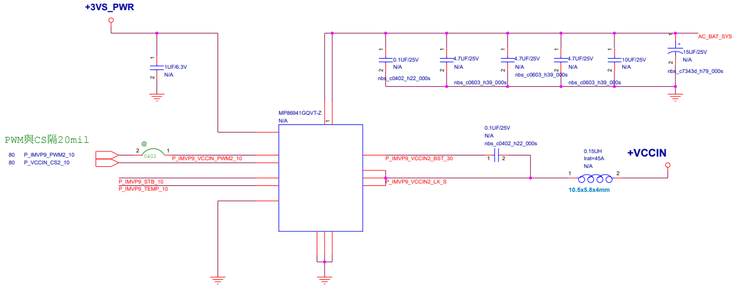

IFPF(not used)
8G4 IFPF
DVI/HDMI
DP
+1V8_AON
IFPF_AUX_SDA
IFPF_AUX_SCL
2.2KOhm
2.2KOhm
IFPF
+PEX_VDD_IFP_IOVDD
Max:305mA
BG17
4.7UF/6.3V
1UF/6.3V
1UF/6.3V
1UF/6.3V
GB5-256
PLACE AT BALLS
PLACE AT BALLS

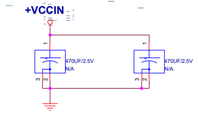
TGL IMVP9 (1) Power [For CPU]



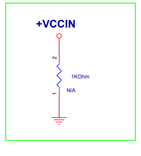


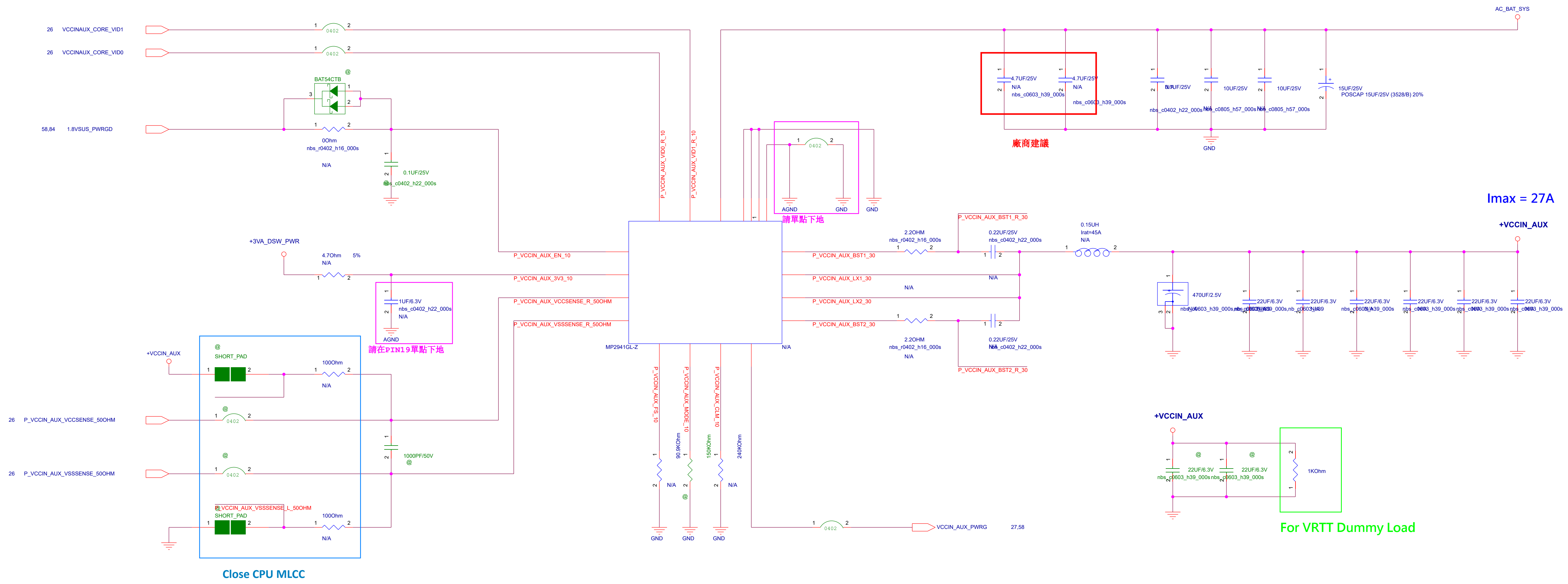






For VRTT Dummy Load

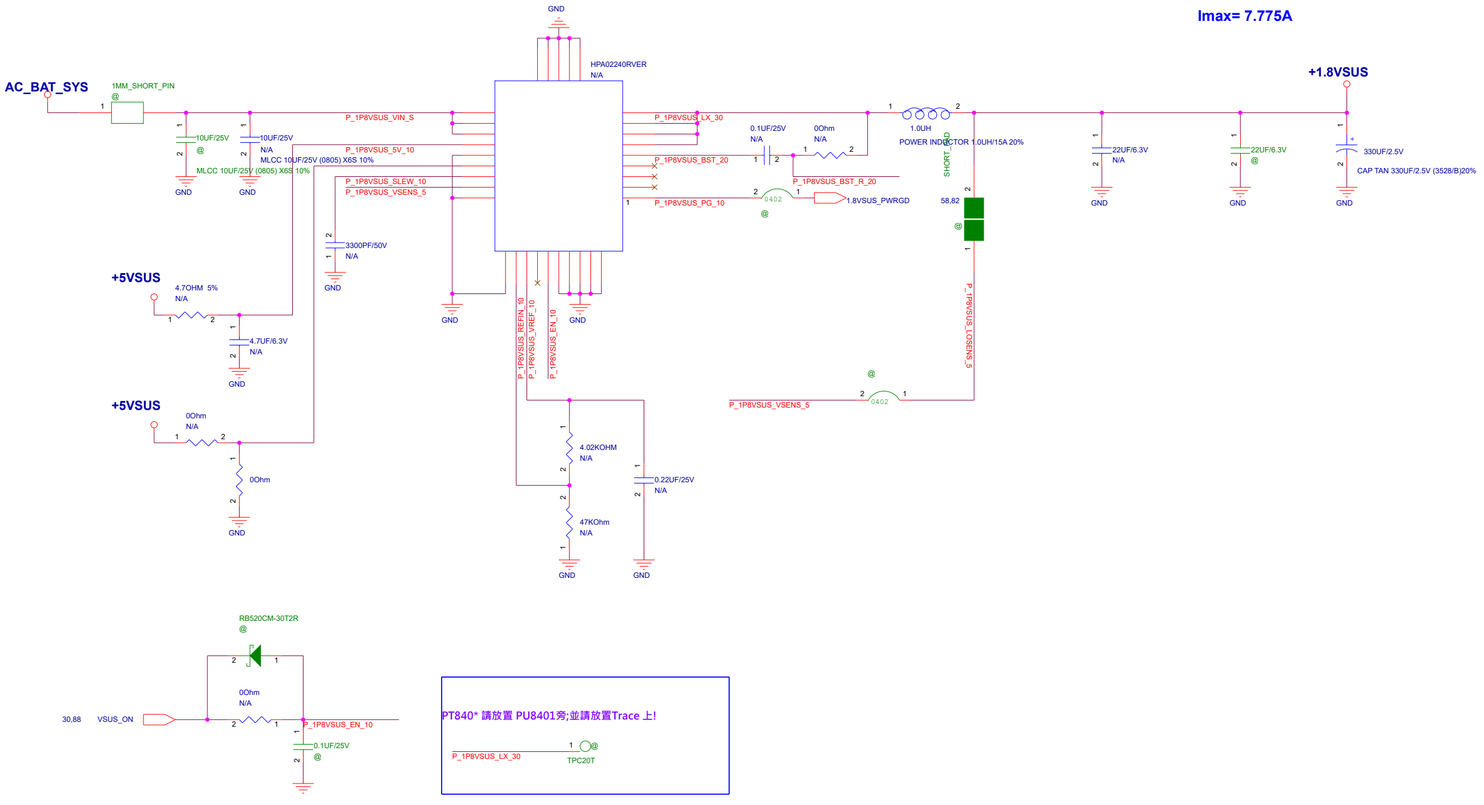


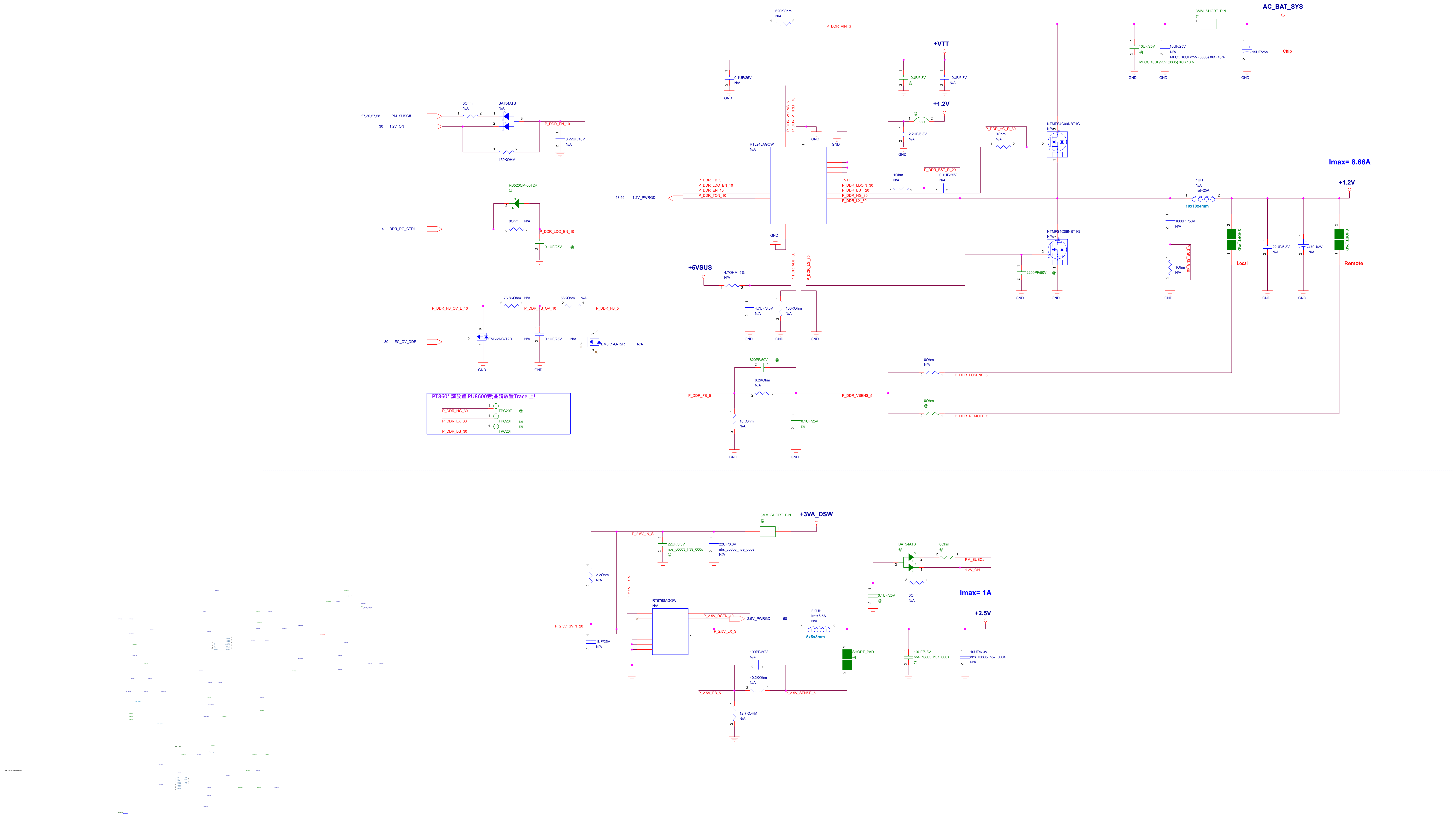


VCCINAUX_CORE_VID1
VCCINAUX_CORE_VID0
1.8VSUS_PWRGD
BAT54CTB
0Ohm
0.1UF/25V
+3VA_DSW_PWR
4.7Ohm 5%
1UF/6.3V
請在PIN19單點下地
AGND
+VCCIN_AUX
SHORT_PAD
100Ohm
P_VCCIN_AUX_VCCSENSE_50OHM
P_VCCIN_AUX_VSSSENSE_50OHM
1000PF/50V
Close CPU MLCC
P_VCCIN_AUX_EN_10
P_VCCIN_AUX_3V3_10
P_VCCIN_AUX_VCCSENSE_R_50OHM
P_VCCIN_AUX_VSSSENSE_R_50OHM
MP2941GL-Z
請單點下地
AC_BAT_SYS
4.7UF/25V
10UF/25V
15UF/25V POSCAP 15UF/25V (3528/B) 20%
廠商建議
GND
P_VCCIN_AUX_BST1_30
P_VCCIN_AUX_LX1_30
P_VCCIN_AUX_LX2_30
P_VCCIN_AUX_BST2_30
2.2OHM
0.22UF/25V
0.15UH Irat=45A
Imax = 27A
+VCCIN_AUX
470UF/2.5V
22UF/6.3V
90.9KOhm
150KOhm
240KOhm
VCCIN_AUX_PWRG
1KOhm
For VRTT Dummy Load

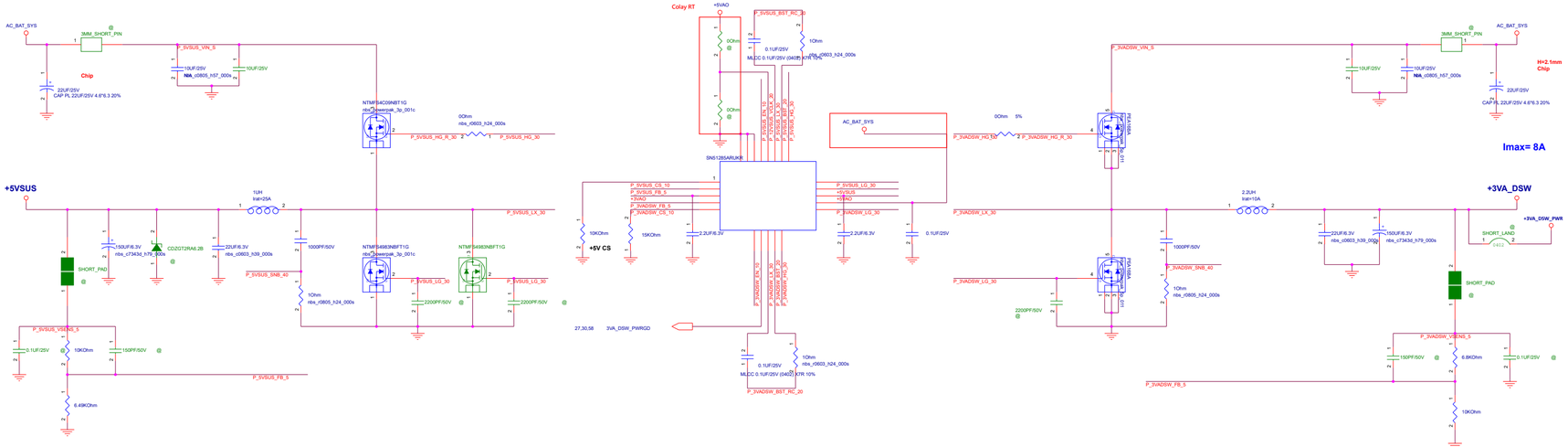
+1.8VSUS [For PCH]

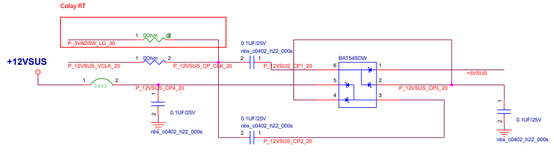
Imax= 7.775A

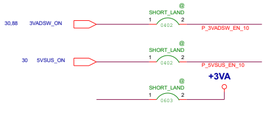




AC_BAT_SYS
3MM_SHORT_PIN
Chip
+VTT
+1.2V
RT8248AGQW
NTMFS4C08NBT1G
NTMFS4C06NBT1G
Imax= 8.66A
+1.2V
1UH
Isat=25A
10x10x4mm
Local
Remote
+5VSUS
PM_SUSC#
1.2V_ON
DDR_PG_CTRL
1.2V_PWRGD
EC_OV_DDR
BAT54ATB
RB520CM-30T2R
EM6K1-G-T2R
PT860° 請放置 PU8600旁;並請放置Trace 上!
P_DDR_HG_30
P_DDR_LX_30
P_DDR_LG_30
TPC20T
+3VA_DSW
RT5768AGQW
2.5V_PWRGD
Imax= 1A
+2.5V
2.2UH
Isat=6.5A
5x5x3mm
SHORT_PAD







請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm

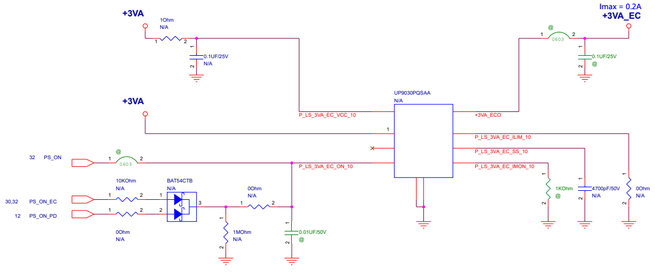
Battery Mode (IMVP8)

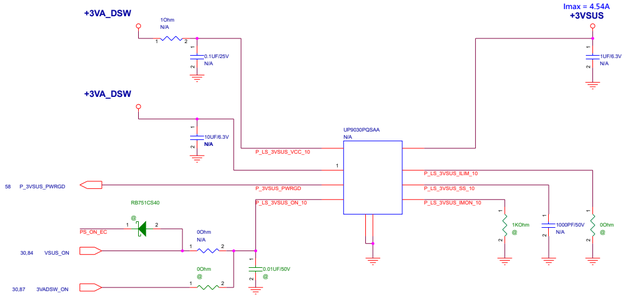
	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-		-	1
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0

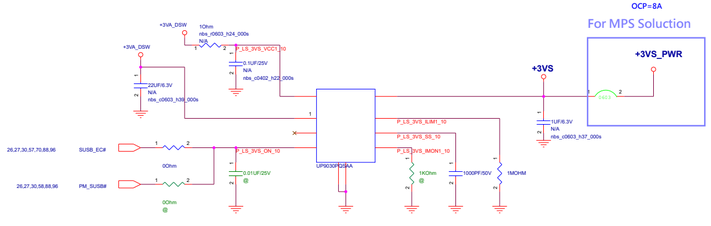
PT870* 請放置 PU8700旁;並請放置Trace 上!

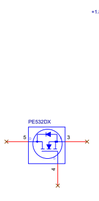
Load Switch

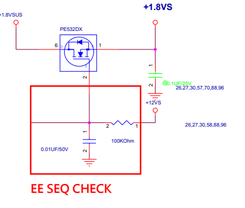


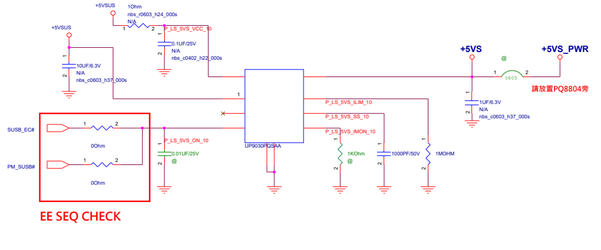


uP9030 ILIM/LPM Setting 對應表		
	LPM (C10)	
GND	Off	3A
1M to GND	Off	5A
Float/VDD	On	8A

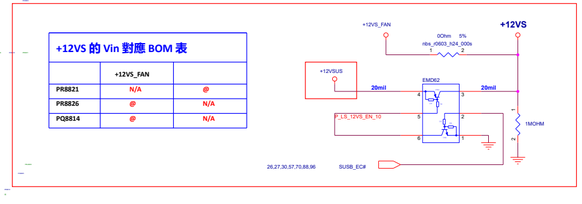


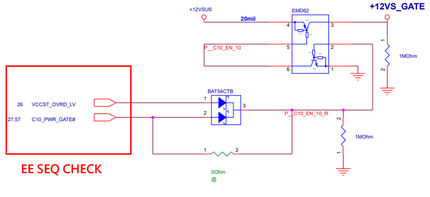






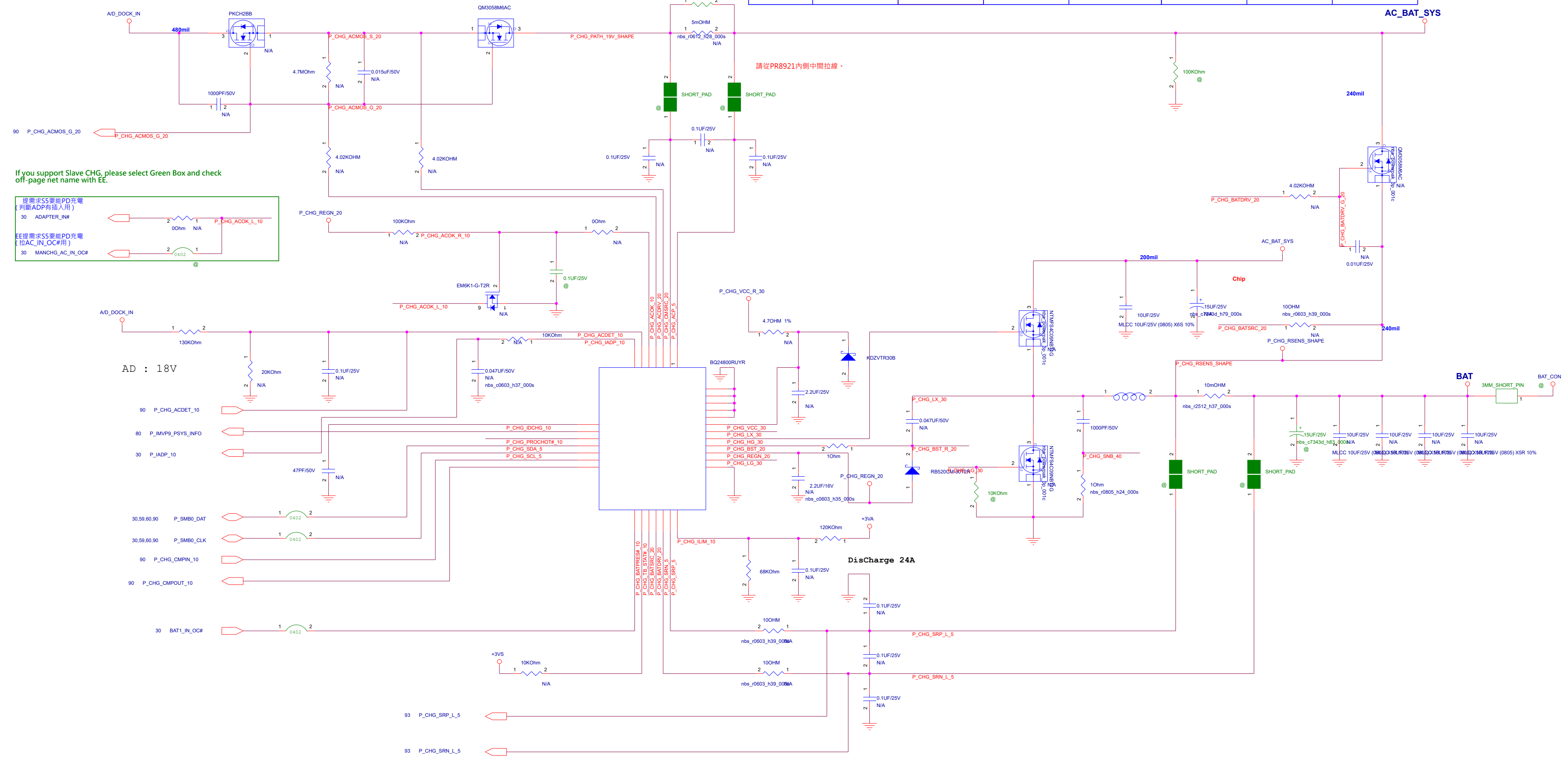
+12VS 的 Vin 對應 BOM 表		
	+12VS_FAN	
PR8821	N/A	@
PR8826	@	N/A
PQ8814	@	N/A

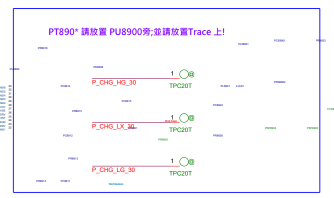




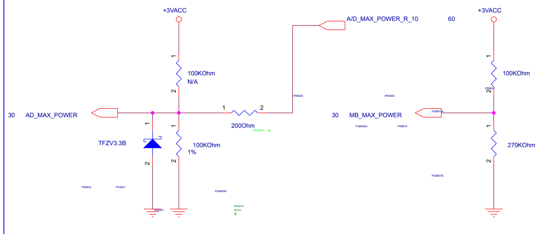
PRS8901	ADP120W	ADP=230W	ADP230W	ADP330W
	TBD		5m	2m
		10125-0008B100		10108-0008B000

PRS8903	ADP=120W	ADP=150W	ADP=180W	ADP=230W	ADP=240W	ADP=280W	ADP=330W
	200m		X	X			560m
			x	x		x	



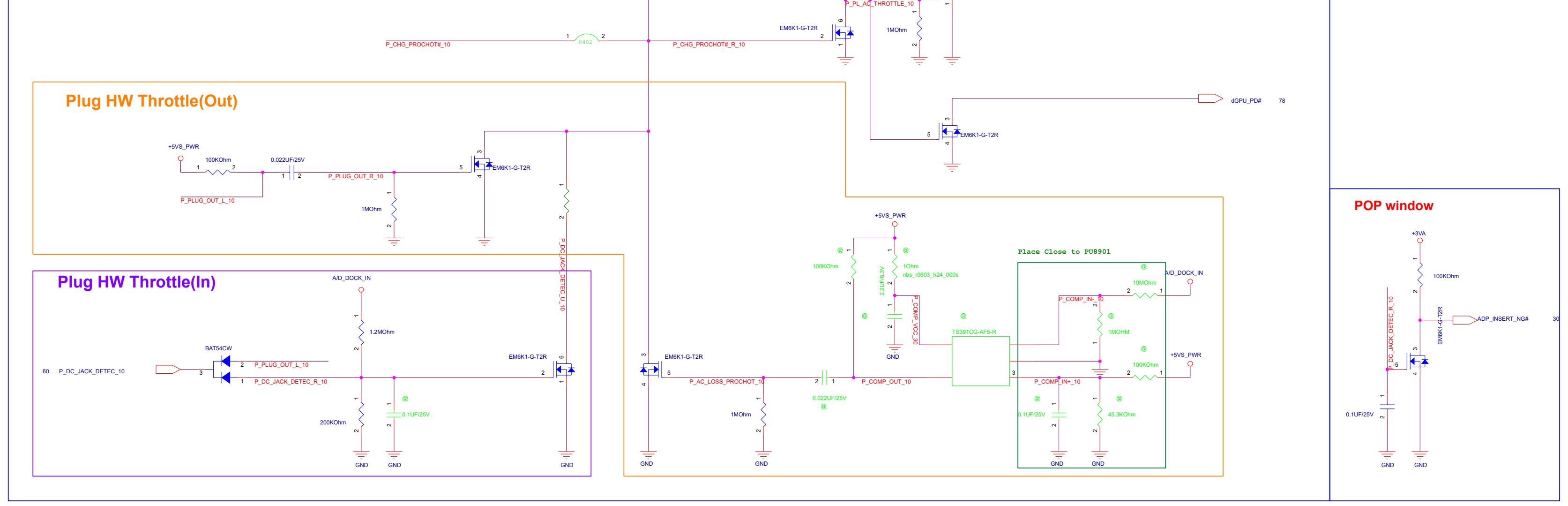


Adaptor select
total power = 90% ADP



	N Series	
PRS8901	10m	5m
PR8936		
14K	0.4V		120W
31.6K 10G212316214030	0.8V	150W	150W
56K 10G212560214030	1.2V	180W	180W
93.1K 10G212931214031	1.6V	65W	230W
150K 10G212150314031	2.0V	NA	280W
270K 10G212270314030	2.4V	90W	200W
560K 10G212560314030	2.8V	120W	240W

Bat limit = byte 7 x 1.7



P90_PROTECTION

Address Selection Table

ADDR0	0	0	0	0	1	1	1	1
ADDR1	0	0	1	1	0	0	1	1
ADDR2	0	1	0	1	0	1	0	1

Register Address

Address	R/W	CMD	DATA	DATA	DATA	DATA
7'h9	W	0	0	0	0	0
Function		Fast_Write Enhanced Setting		Reset time, 0ms		Slave 0 0 0 Slave 0 0 1 Slave 0 1 0 Slave 0 1 1

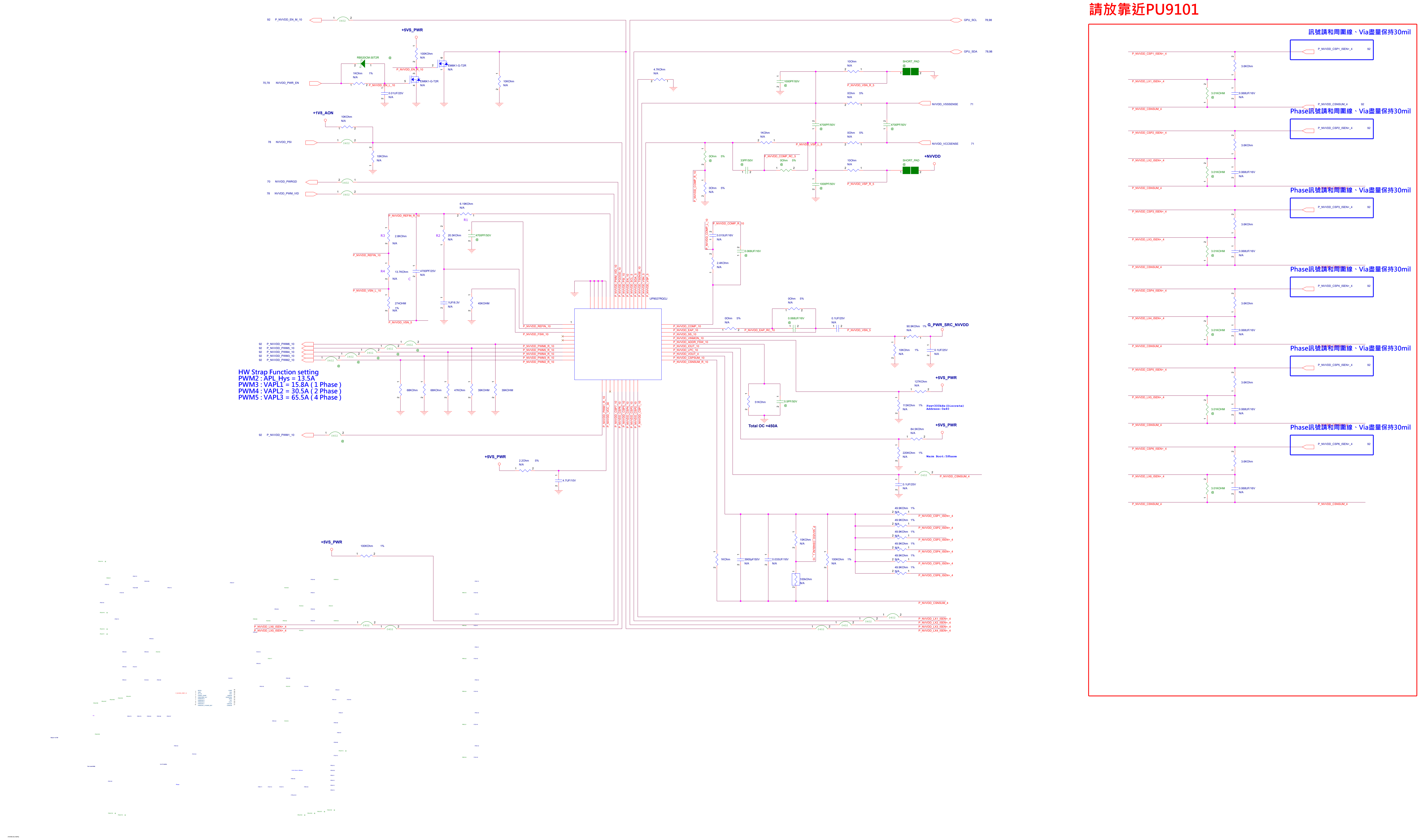
VCC pin OVP Protection circuit
24V

IPCXXXXX

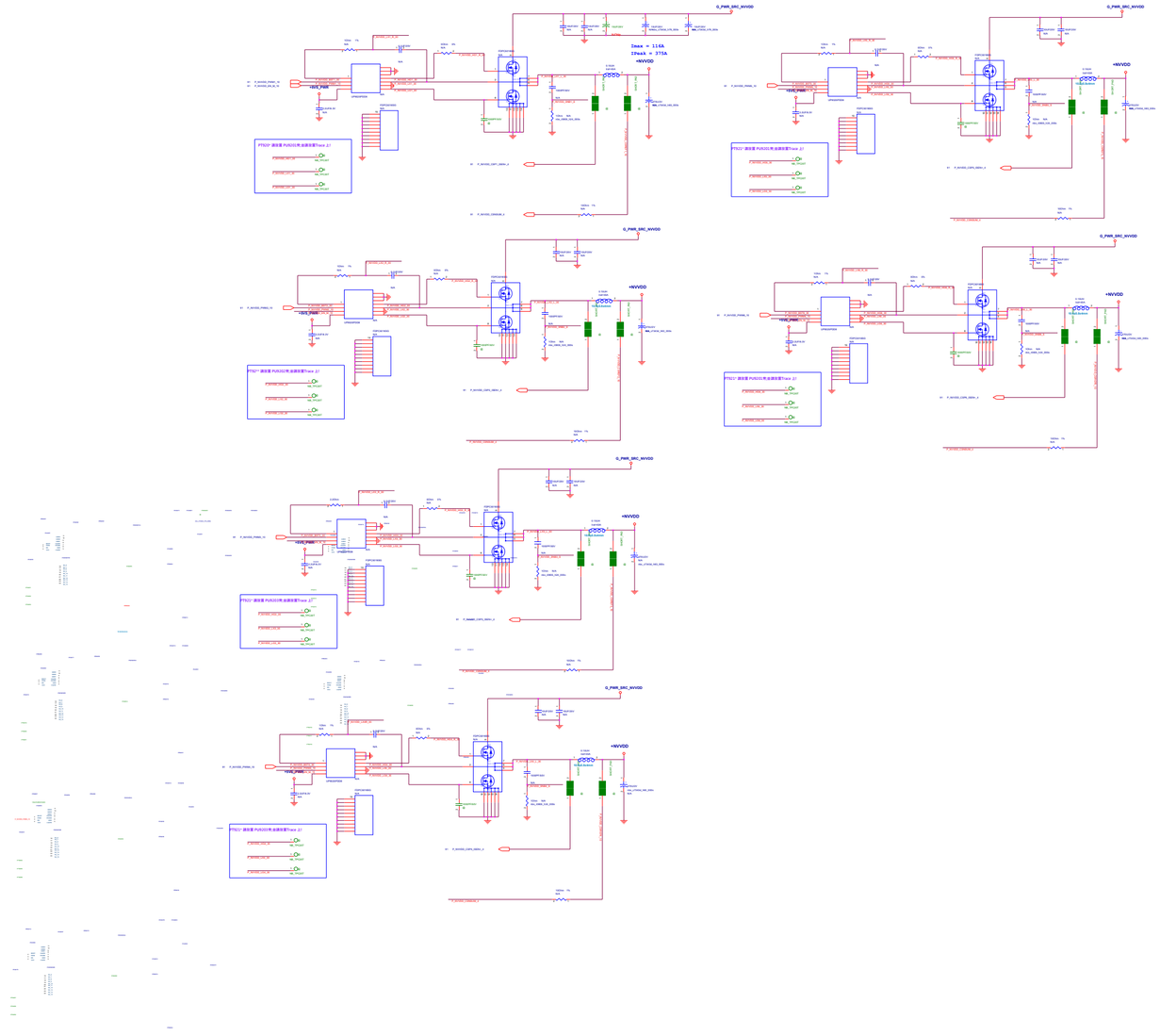
DC JACK Protection

OVP Protection circuit
24V==Cost down

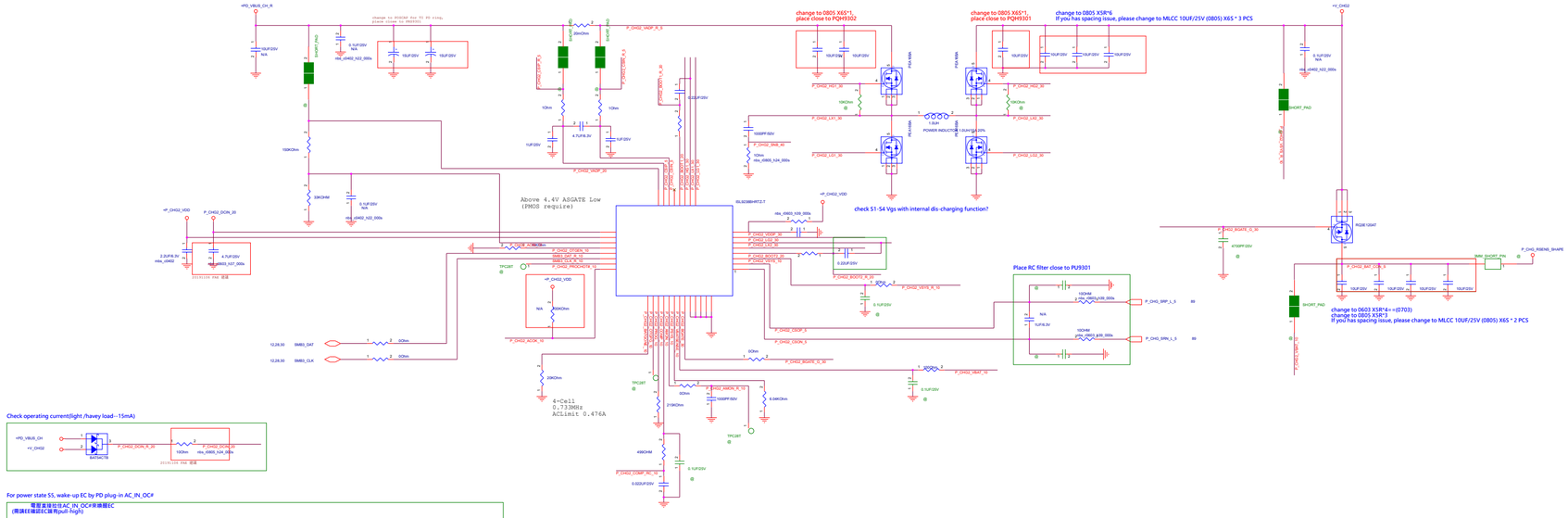
OVP for type C input
(Slave Charger)


請放靠近PU9101
訊號請和周圍線，Via盡量保持30mil
Phase訊號請和周圍線，Via盡量保持30mil
Phase訊號請和周圍線，Via盡量保持30mil
Phase訊號請和周圍線，Via盡量保持30mil
Phase訊號請和周圍線，Via盡量保持30mil
Phase訊號請和周圍線，Via盡量保持30mil
HW Strap Function setting
PWM2 : APL_Hys = 13.5A
PWM3 : VAPL1 = 15.8A (1 Phase)
PWM4 : VAPL2 = 30.5A (2 Phase)
PWM5 : VAPL3 = 65.5A (4 Phase)
+5VS_PWR
+1V8_AON
+NVVDD
G_PWR_SRC_NVVDD
Total OC =450A
92 P_NVVDD_PWM6_10
92 P_NVVDD_PWM5_10
92 P_NVVDD_PWM4_10
92 P_NVVDD_PWM3_10
92 P_NVVDD_PWM2_10
92 P_NVVDD_PWM1_10

+NVVDD [For DGPU]

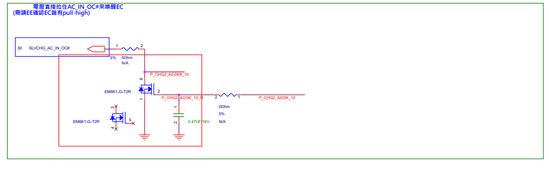


Charger ISL9238 (NVDC)



Check operating current(light /havey load--15mA)

For power state S5, wake-up EC by PD plug-in AC_IN_OC#

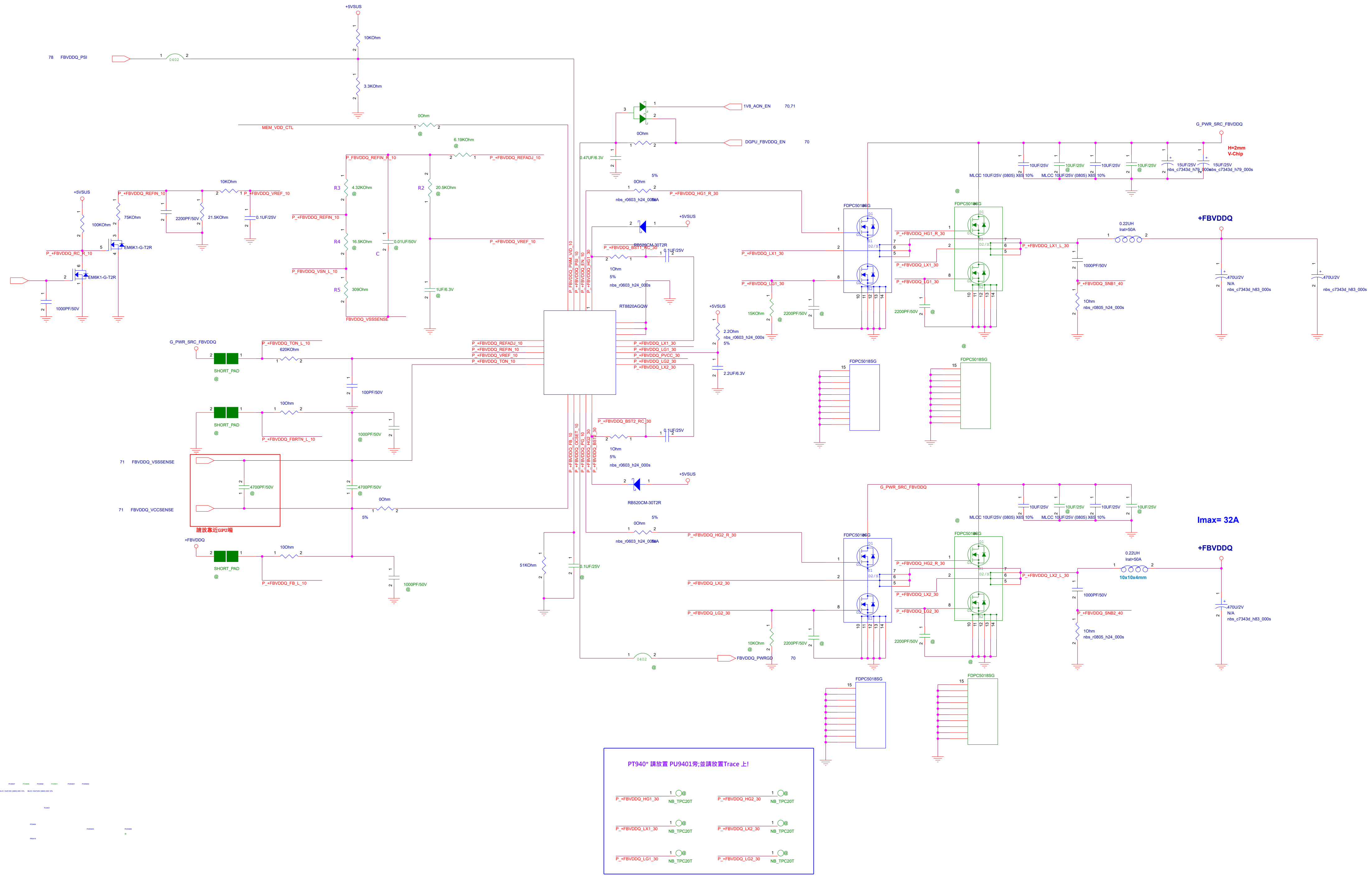


		L
Voltage	1.35V	
PR9409		
PR9423		

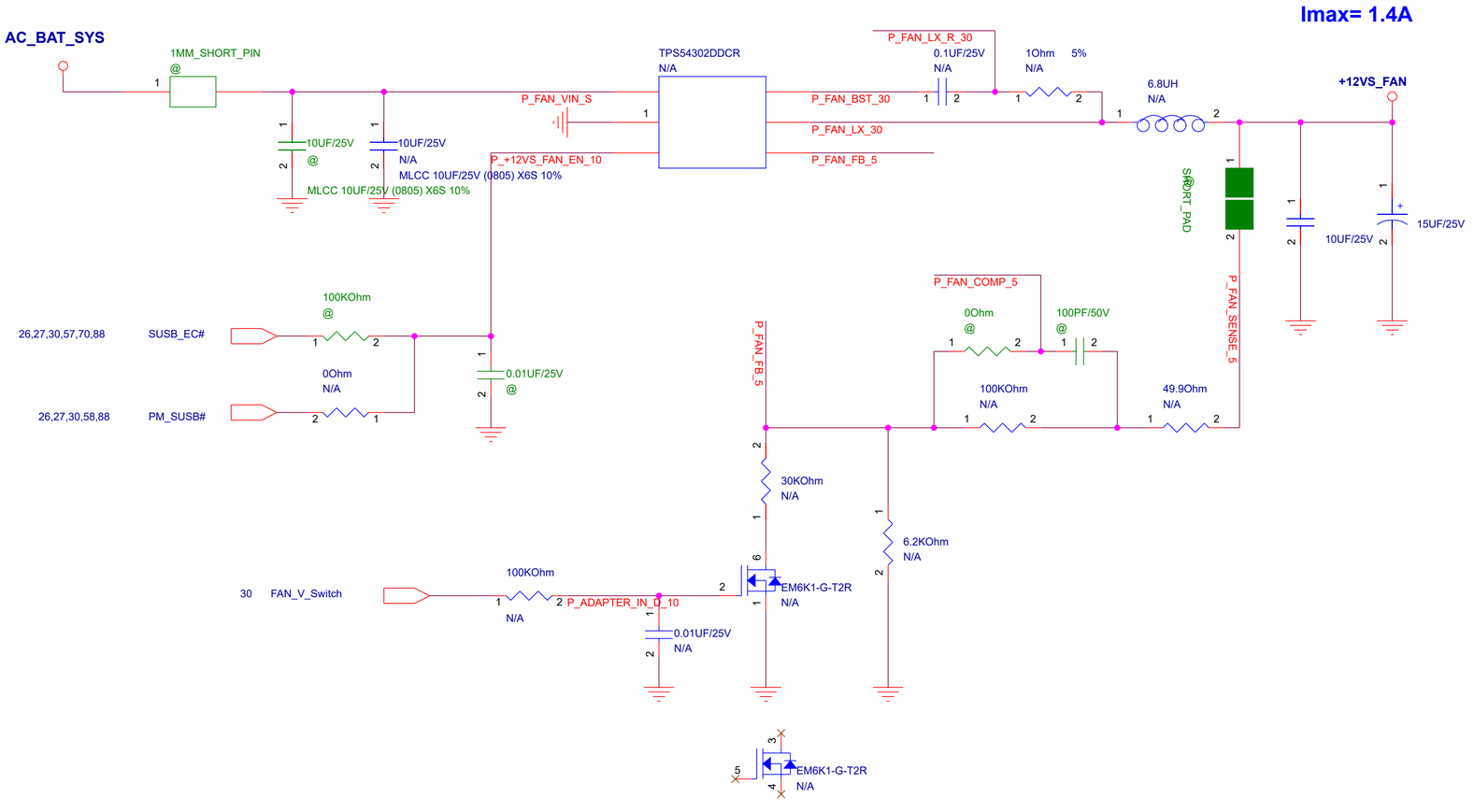
MEM_VDD_CTL		L
Voltage	1.35V	
PR9409		
PR9423		

DVS Setting		
	H	
Voltage		1.2V
PR9404		
PR9409		
	140KOhm	

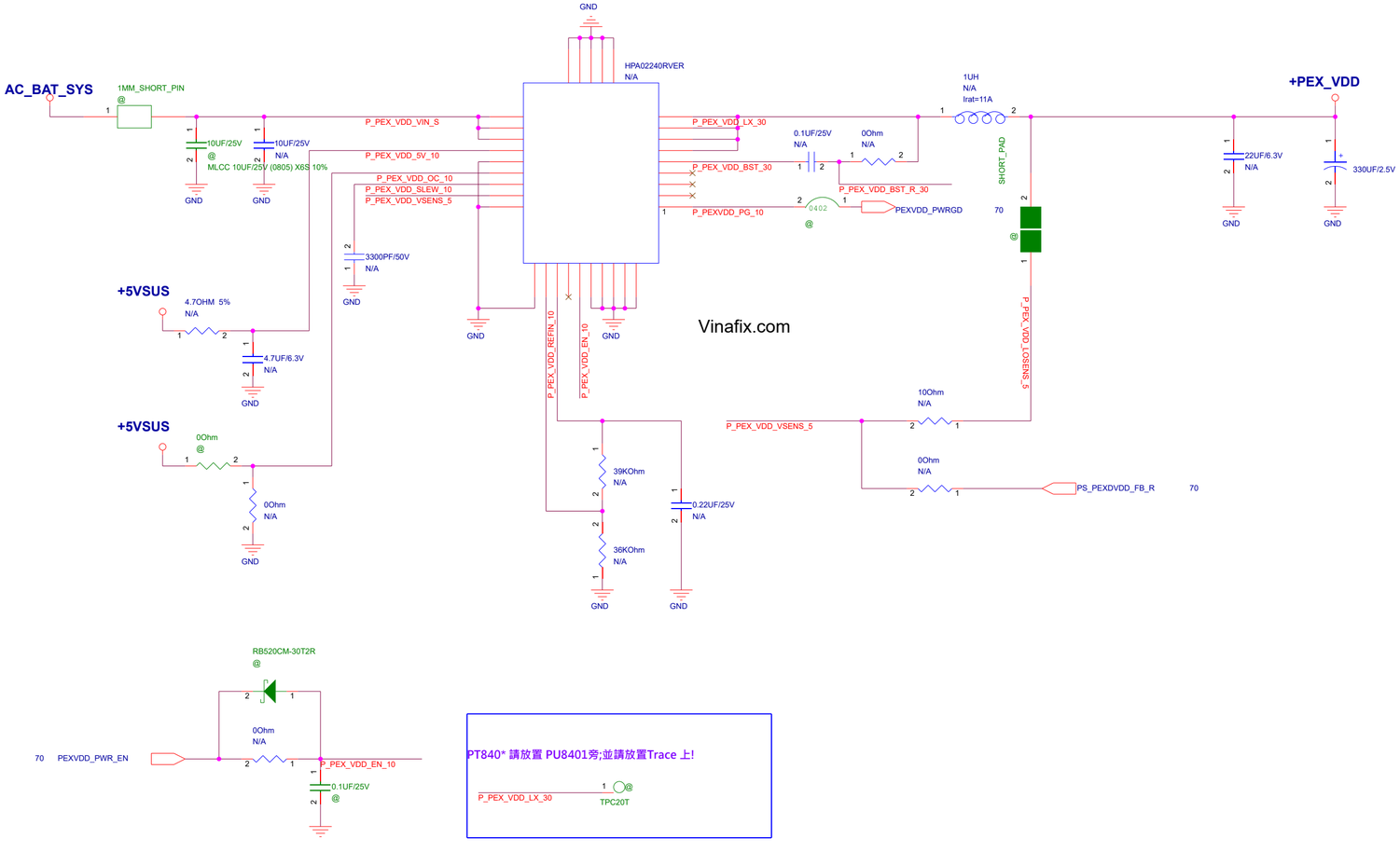
Fixed Vout		
	PC9403/PR9423/PQ9401 PR9402/PR9414	
Voltage		1.2V
PR9404		
PR9409		



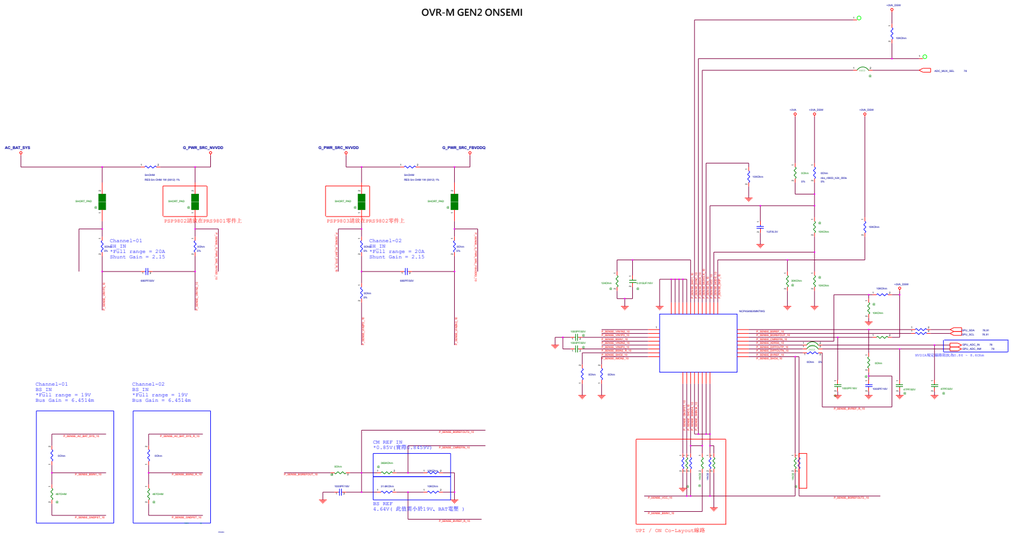
78 MEM_VDD_CTL
78 FBVDDQ_PSI
+5VSUS
MEM_VDD_CTL
1V8_AON_EN
DGPU_FBVDDQ_EN
G_PWR_SRC_FBVDDQ
H=2mm
V-Chip
+FBVDDQ
Imax= 32A
0.22UH
10x10x4mm
SHORT_PAD
FBVDDQ_VSSSENSE
FBVDDQ_VCCSENSE
FBVDDQ_PWRGD
FDPC5018SG
RB520CM-30T2R
PT940* 請放置 PU9401旁;並請放置Trace 上!
P_+FBVDDQ_HG1_30
NB_TPC20T
P_+FBVDDQ_HG2_30
NB_TPC20T
P_+FBVDDQ_LX1_30
NB_TPC20T
P_+FBVDDQ_LX2_30
NB_TPC20T
P_+FBVDDQ_LG1_30
NB_TPC20T
P_+FBVDDQ_LG2_30
NB_TPC20T


Imax= 1.4A
AC_BAT_SYS
1MM_SHORT_PIN
@
TPS54302DDCR
N/A
P_FAN_LX_R_30
0.1UF/25V
N/A
1Ohm 5%
N/A
6.8UH
N/A
+12VS_FAN
P_FAN_VIN_S
P_FAN_BST_30
P_FAN_LX_30
P_FAN_FB_5
P_+12VS_FAN_EN_10
10UF/25V
@
MLCC 10UF/25V (0805) X6S 10%
10UF/25V
N/A
MLCC 10UF/25V (0805) X6S 10%
SHORT_PAD
10UF/25V
15UF/25V
P_FAN_SENSE_5
P_FAN_COMP_5
0Ohm
@
100PF/50V
@
100KOhm
N/A
49.9Ohm
N/A
100KOhm
@
26,27,30,57,70,88 SUSB_EC#
0Ohm
N/A
26,27,30,58,88 PM_SUSB#
0.01UF/25V
@
P_FAN_FB_5
30KOhm
N/A
6.2KOhm
N/A
100KOhm
30 FAN_V_Switch
N/A
P_ADAPTER_IN_D_10
EM6K1-G-T2R
N/A
0.01UF/25V
N/A
EM6K1-G-T2R
N/A

PEX_VDD [For GPU]



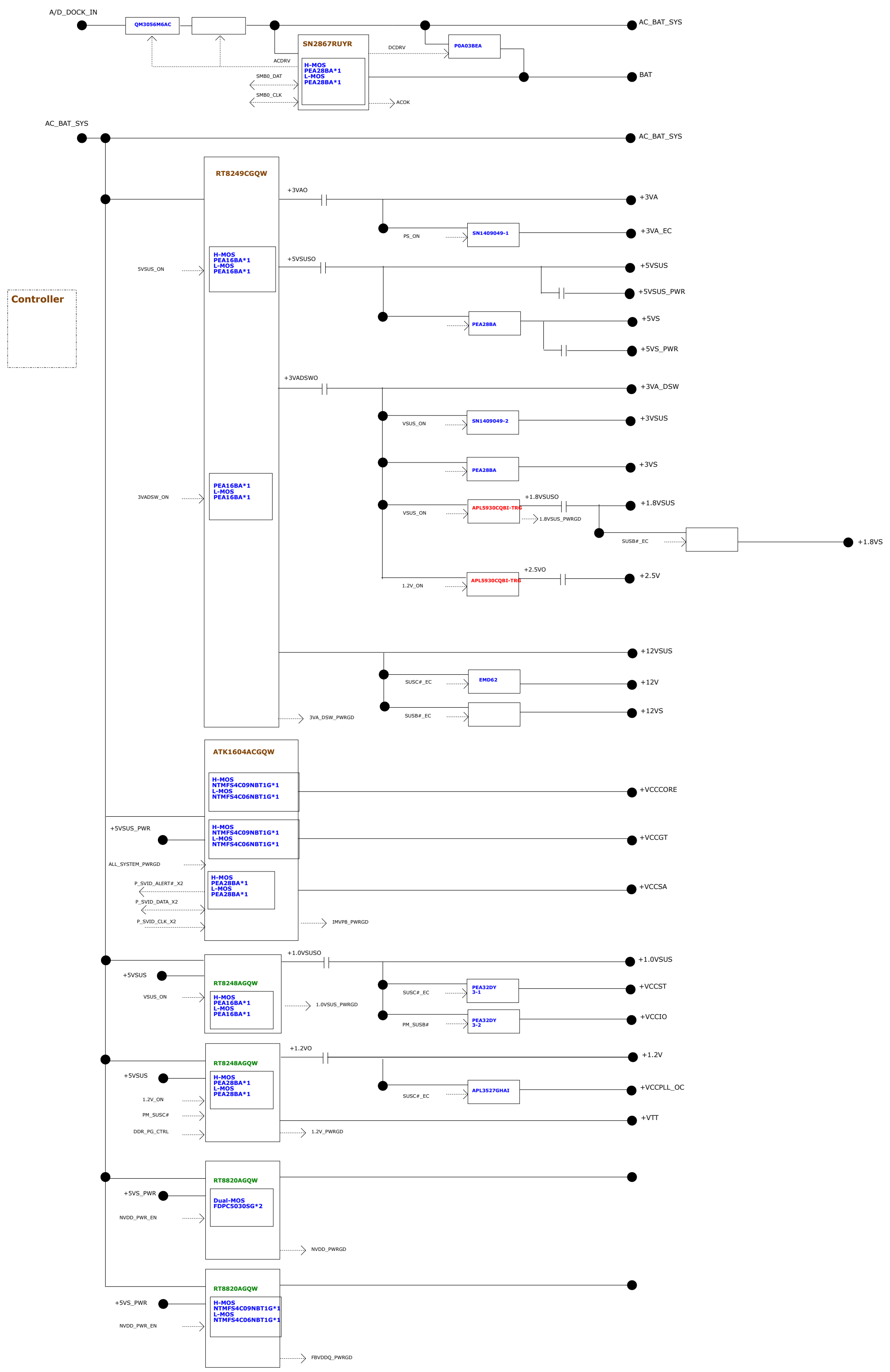
OVR-M GEN2 ONSEMI



	PD9801	PR9805	PR9807	PC9803	PC9804	PC9805	PR9814	PR9855	PR9822
GN2O	06129-00220000	0 Ohm 10G212000004030	0 Ohm 10G212000004030	0	0	0	0 Ohm 10G212000004030	0 Ohm 10G212000004030	0 Ohm 10G212000004030
	06129-00110100	10G212750214010	75KOhm 10G212750214010	1000PF/50V 11G232110214321	1000PF/50V 11G232110214321	0.015OF/16V 11G232115311360	357Ohm 10G212357014010	0	49.9Ohm 10G212499N914010

	PC9810	PR9860	PR9809	PR9810	PR9834				
GN2O	0	0	0	10KOhm 10G212100214010	51.6KOhm 10G212316214010	10G212000004030	10G212000004030		
	1000PF/16V 11G232110211030	0 Ohm 10G212000004030	360KOhm 10G212364004010	68KOhm 10G212680314010	324Kohm 10G212324314010	0	0	0.015OF/16V 11G232115311360	487Ohm 10G212487014010

GN2O		10G212000004030		10G212100214010	10G212000004030	10G212000004030		10G212000004030	
N18P-G1	487Ohm 10G212487014010	0	00hm 10G212000004030	0	100Ohm 10G212100014010	49.9Ohm 10G212499N914010	357Ohm 10G212357014010		10G212000004030

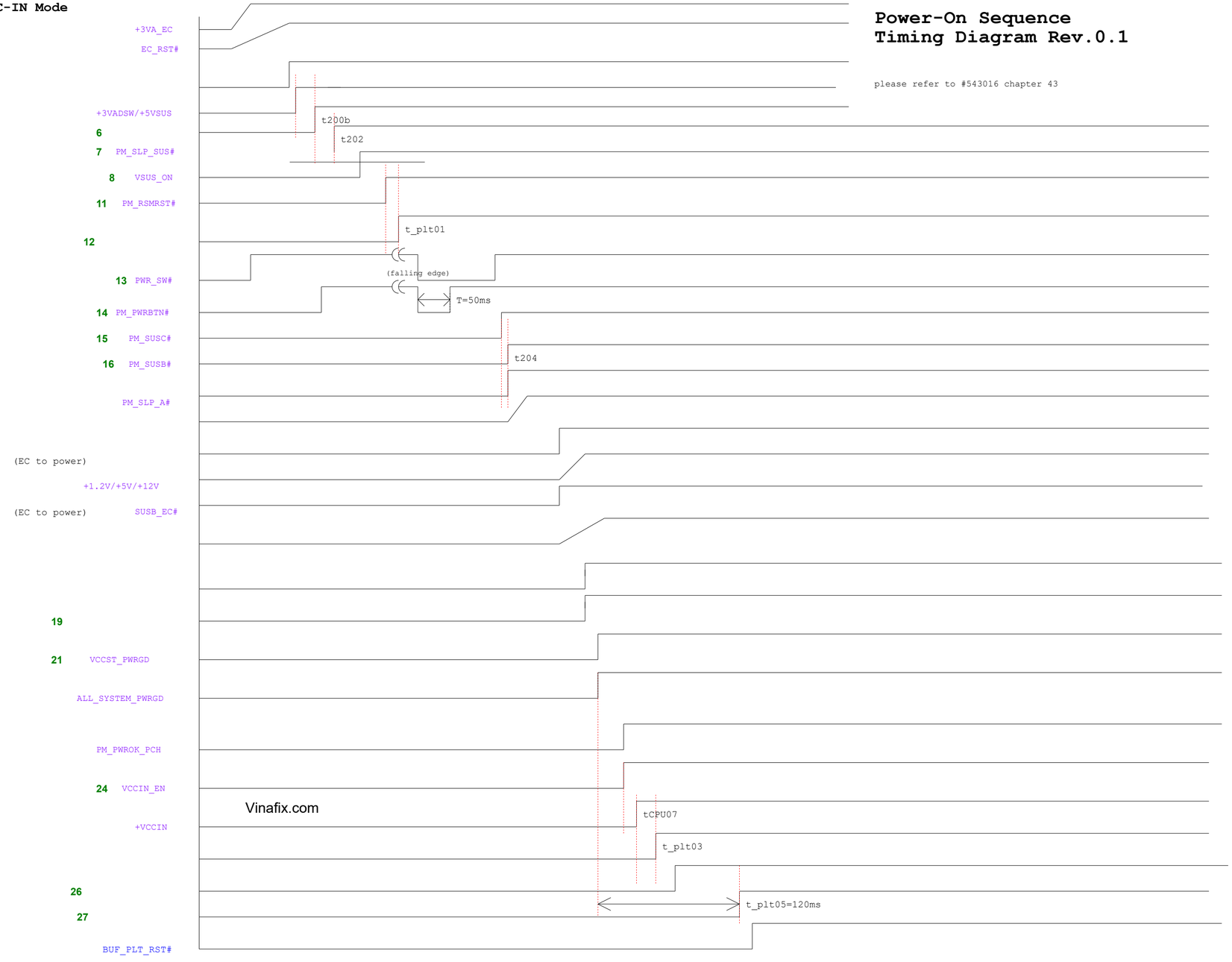


A/D_DOCK_IN
QM3056M6AC
AC_BAT_SYS
SN2867RUYR
DCDRV
P0A03BEA
ACDRV
H-MOS
PEA28BA*1
L-MOS
PEA28BA*1
SMB0_DAT
SMB0_CLK
ACOK
BAT
AC_BAT_SYS
AC_BAT_SYS
RT8249CGQW
+3VAO
+3VA
PS_ON
SN1409049-1
+3VA_EC
5VSUS_ON
H-MOS
PEA16BA*1
L-MOS
PEA16BA*1
+5VSUSO
+5VSUS
+5VSUS_PWR
Controller
PEA28BA
+5VS
+5VS_PWR
+3VADSWO
+3VA_DSW
VSUS_ON
SN1409049-2
+3VSUS
PEA28BA
+3VS
3VADSW_ON
PEA16BA*1
L-MOS
PEA16BA*1
VSUS_ON
APL5930CQBI-TRG
+1.8VSUSO
+1.8VSUS
1.8VSUS_PWRGD
SUSB#_EC
+1.8VS
1.2V_ON
APL5930CQBI-TRG
+2.5VO
+2.5V
+12VSUS
SUSC#_EC
EMD62
+12V
SUSB#_EC
+12VS
3VA_DSW_PWRGD
ATK1604ACGQW
H-MOS
NTMFS4C09NBT1G*1
L-MOS
NTMFS4C06NBT1G*1
+VCCCORE
+5VSUS_PWR
H-MOS
NTMFS4C09NBT1G*1
L-MOS
NTMFS4C06NBT1G*1
+VCCGT
ALL_SYSTEM_PWRGD
P_SVID_ALERT#_X2
P_SVID_DATA_X2
P_SVID_CLK_X2
H-MOS
PEA28BA*1
L-MOS
PEA28BA*1
+VCCSA
IMVP8_PWRGD
+1.0VSUSO
+1.0VSUS
+5VSUS
RT8248AGQW
VSUS_ON
H-MOS
PEA16BA*1
L-MOS
PEA16BA*1
1.0VSUS_PWRGD
SUSC#_EC
PEA32DY
3-1
+VCCST
PM_SUSB#
PEA32DY
3-2
+VCCIO
+1.2VO
+1.2V
RT8248AGQW
+5VSUS
H-MOS
PEA28BA*1
L-MOS
PEA28BA*1
1.2V_ON
PM_SUSC#
DDR_PG_CTRL
SUSC#_EC
APL3527GHAI
+VCCPLL_OC
+VTT
1.2V_PWRGD
RT8820AGQW
+5VS_PWR
Dual-MOS
FDPC5030SG*2
NVDD_PWR_EN
NVDD_PWRGD
RT8820AGQW
+5VS_PWR
H-MOS
NTMFS4C09NBT1G*1
L-MOS
NTMFS4C06NBT1G*1
NVDD_PWR_EN
FBVDDQ_PWRGD

AC-IN Mode

Power-On Sequence Timing Diagram Rev.0.1

please refer to #543016 chapter 43



AC-IN Mode

Power On Sequence Diagram Rev.2.0