MS-7C58 Ver:10

CPU:
AMD AM4

System Chipset:
Promontory A320 / B450
(Value DIY or System Builder)

Main Memory:
DDR IV * 2 MAX:64 GB

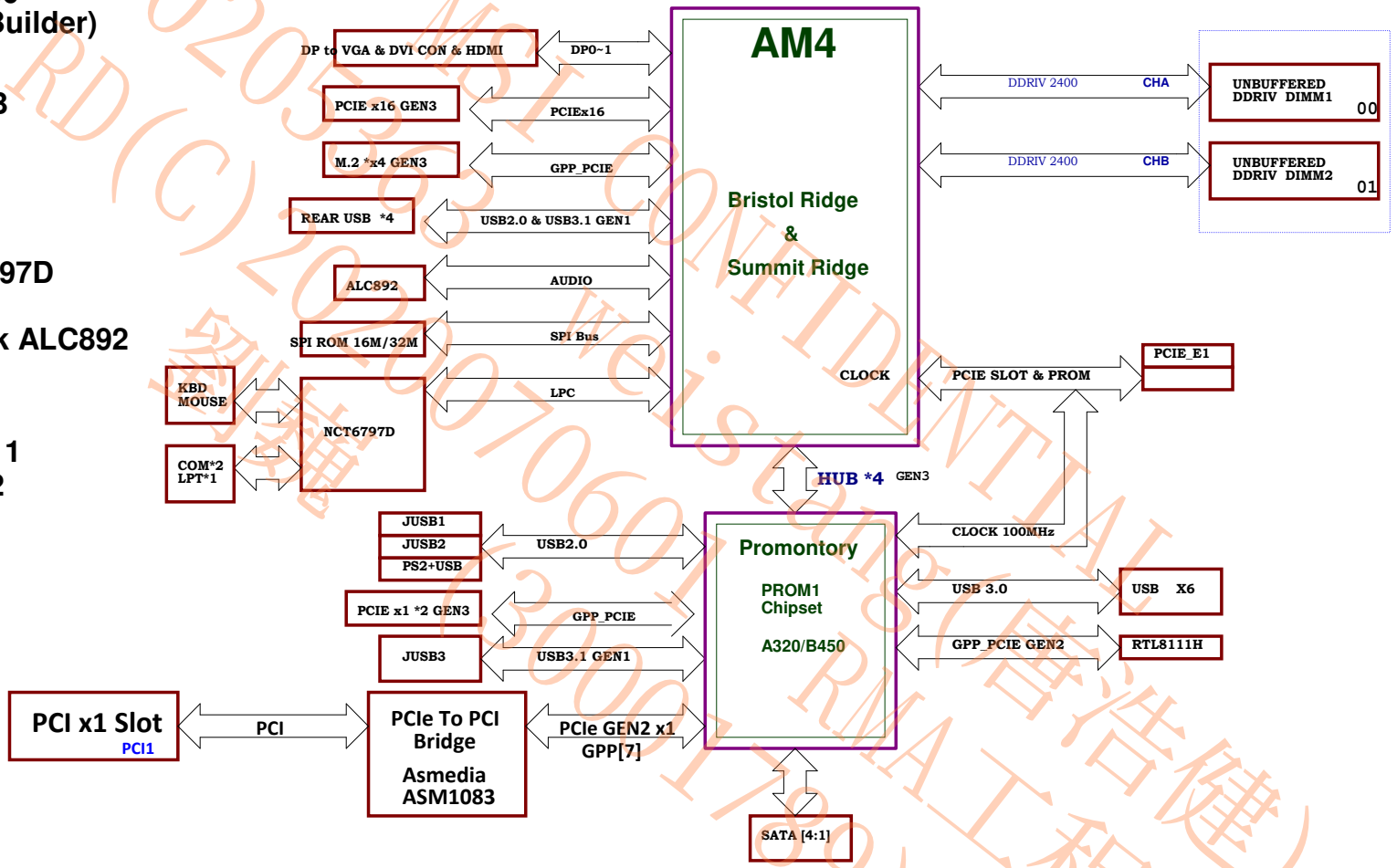
VRM
RT8894 3+2

On Board Chipset:
LPC Super I/O --NCT6797D
LAN RTL8111H
Azalia CODEC - Realtek ALC892

Expansion Slots:
From CPU
PCI Express X16 Slot * 1
PCI Express X1 Slot * 2
PCI Slot * 1
M.2 Slot * 1

OCP IC:
UP6273

FUSION BLOCK DIAGRAM



MICRO-STAR INT'L CO.,LTD.

Title: Block Diagram

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AMD
AM4

MICRO-STAR INT'L CO.,LTD.

Title: COVER SHEET

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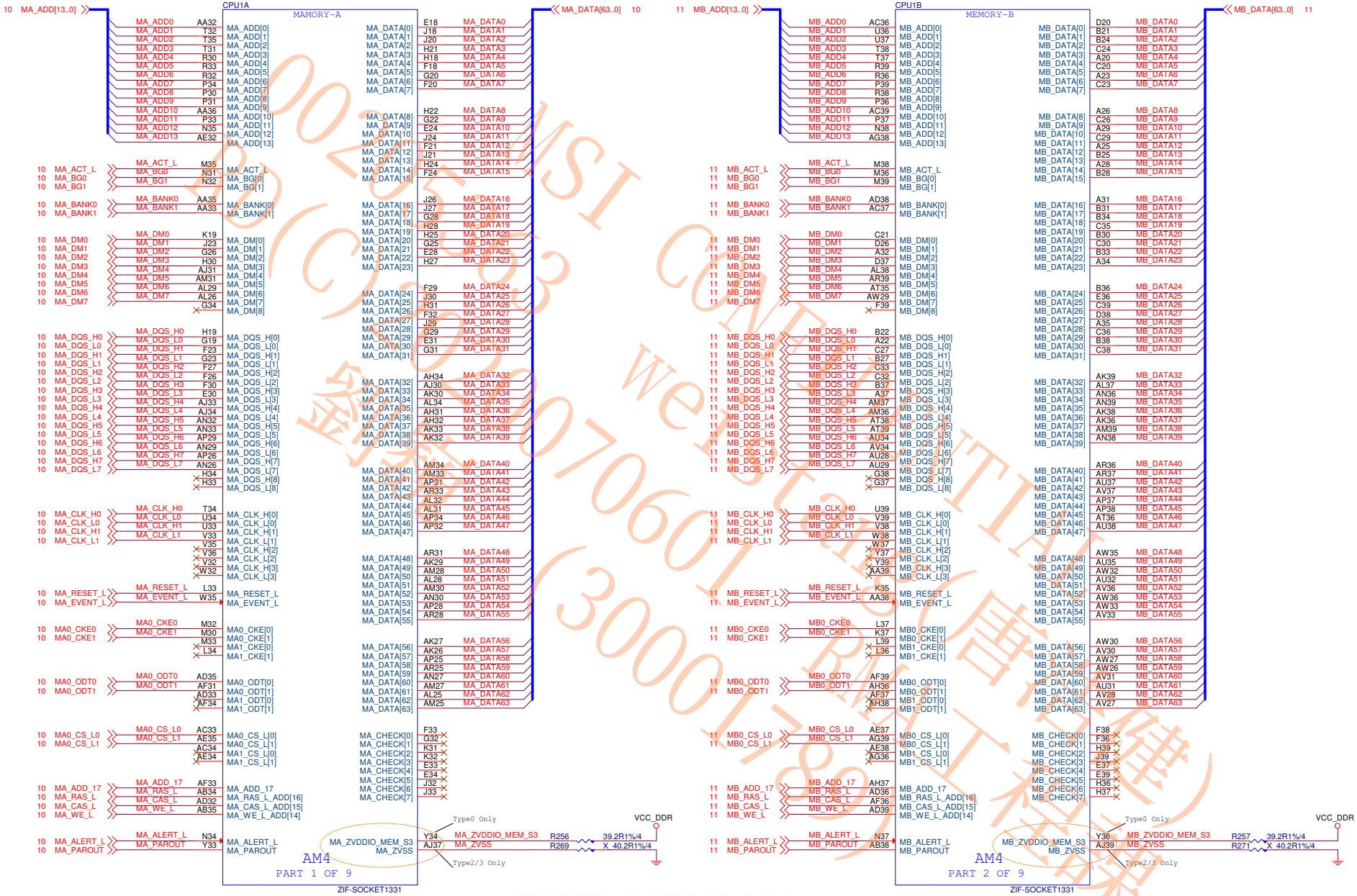

Table 6. DRAM Memory Interface Pin Descriptions (Continued)

Signal Name	Type	Description	Processor Types				
			0	1	2	3	4
MA_ZVDDIO_MEM_S3, MB_ZVDDIO_MEM_S3	A	Compensation Resistor to VDDIO_MEM_S	X				
MA_ZVSS, MB_ZVSS	A	DRAM Compensation Resistor to VSS		X	X	X	X

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Title: AM4 DDR4 I/F			
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CPU1C
PCIE
From FCH
To FCH
No fuction for Type1
From M2_1
To M2_1
No fuction for Type0/1
From PCI_E2
To PCI_E2
No fuction for Type0/1/3
SATA Express
P_HUB_RXP[0] P_HUB_RXN[0] P_HUB_RXP[1] P_HUB_RXN[1] P_HUB_RXP[2] P_HUB_RXN[2] P_HUB_RXP[3] P_HUB_RXN[3]
P_HUB_TXP[0] P_HUB_TXN[0] P_HUB_TXP[1] P_HUB_TXN[1] P_HUB_TXP[2] P_HUB_TXN[2] P_HUB_TXP[3] P_HUB_TXN[3]
P_GPP_RXP[0] P_GPP_RXN[0] P_GPP_RXP[1] P_GPP_RXN[1]
P_GPP_RXP[2]/SATA_RX0P P_GPP_RXN[2]/SATA_RX0N P_GPP_RXP[3]/SATA_RX1P P_GPP_RXN[3]/SATA_RX1N
P_GPP_TXP[0] P_GPP_TXN[0] P_GPP_TXP[1] P_GPP_TXN[1]
P_GPP_TXP[2]/SATA_TX0P P_GPP_TXN[2]/SATA_TX0N P_GPP_TXP[3]/SATA_TX1P P_GPP_TXN[3]/SATA_TX1N
P_GFX_RXP[0]–P_GFX_RXP[15] P_GFX_RXN[0]–P_GFX_RXN[15]
P_GFX_TXP[0]–P_GFX_TXP[15] P_GFX_TXN[0]–P_GFX_TXN[15]
C0.22u16X5/4
CPU_VDDP
R258 196R1%/4 APU_P_ZVDDP W8
R304 1K1%/4 APU_SATA_ZVDDP AV7
Within 1500 mils from APU
Within 1000 mils from APU
P_ZVDDP
SATA_ZVDDP
Type0 Only
Type2 Only
P_ZVSS
P0A_ZVSS
P0B_ZVSS
SATA_ZVSS
APU_P_ZVSS APU_P0A_ZVSS APU_P0B_ZVSS APU_SATA_ZVSS
R222 196R1%/4
R253 X_200R/4
R325 X_200R/4
R309 1K1%/4
AM4
PART 3 OF 9
ZIF-SOCKET1331

Table 3. PCI Express® Interface Pin Descriptions

Signal Name	Type	Description	Processor Types 0	1	2	3	4
P_GFX_RXP[3:0], P_GFX_RXN[3:0]	I-PCIe-D	External Graphics PCIe® Receive Data Differential Pairs	X	X	X	X	X
P_GFX_RXP[7:4], P_GFX_RXN[7:4]	I-PCIe-D	External Graphics PCIe® Receive Data Differential Pairs	X		X	X	X
P_GFX_TXP[3:0], P_GFX_TXN[3:0]	O-PCIe-D	External Graphics PCIe® Transmit Data Differential Pairs	X	X	X	X	X
P_GFX_TXP[7:4], P_GFX_TXN[7:4]	O-PCIe-D	External Graphics PCIe® Transmit Data Differential Pairs	X		X	X	X
P_GFX_RXP[15:8], P_GFX_RXN[15:8]	I-PCIe-D	External Graphics PCIe® Receive Data Differential Pairs			X		X
P_GFX_TXP[15:8], P_GFX_TXN[15:8]	O-PCIe-D	External Graphics PCIe® Transmit Data Differential Pairs			X		X
P_GPP_RXP[1:0], P_GPP_RXN[1:0]	I-PCIe-D	General Purpose External PCIe® Receive Data Differential Pairs	X	X	X	X	X
P_GPP_TXP[1:0], P_GPP_TXN[1:0]	O-PCIe-D	General Purpose External PCIe® Transmit Data Differential Pairs	X	X	X	X	X
P_GPP_RXP[2]/SATA_RX0P, P_GPP_RXN[2]/SATA_RX0N	I-PCIe-D	General Purpose External PCIe® Receive Data Differential Pairs			X	X	X
P_GPP_TXP[2]/SATA_TX0P, P_GPP_TXN[2]/SATA_TX0N	O-PCIe-D	General Purpose External PCIe® Transmit Data Differential Pairs			X	X	X
P_GPP_RXP[3]/SATA_RX1P, P_GPP_RXN[3]/SATA_RX1N	I-PCIe-D	General Purpose External PCIe® Receive Data Differential Pairs			X	X	X
P_GPP_TXP[3]/SATA_TX1P, P_GPP_TXN[3]/SATA_TX1N	O-PCIe-D	General Purpose External PCIe® Transmit Data Differential Pairs			X	X	X
P_HUB_RXP[1:0], P_HUB_RXN[1:0]	I-PCIe-D	General Purpose External PCIe® Receive Data Differential Pairs	X	X	X	X	X
P_HUB_RXP[3:2], P_HUB_RXN[3:2]	I-PCIe-D	General Purpose External PCIe® Receive Data Differential Pairs	X		X	X	X
P_HUB_TXP[1:0], P_HUB_TXN[1:0]	O-PCIe-D	General Purpose External PCIe® Transmit Data Differential Pairs	X	X	X	X	X
P_HUB_TXP[3:2], P_HUB_TXN[3:2]	O-PCIe-D	General Purpose External PCIe® Transmit Data Differential Pairs	X		X	X	X
PCIE_RST_L/EGPIO26	O-IO33S5-S	PCI Host Bus Reset. Asserted during transition to S3/S5.	X	X	X	X	X

Table 3. PCI Express® Interface Pin Descriptions (Continued)

Signal Name	Type	Description	Processor Types 0	1	2	3	4
P0A_ZVSS	A	Compensation Resistor to VSS / PCIe® Calibration Positive			X		X
P0B_ZVSS	A	Compensation Resistor to VSS / PCIe® Calibration Positive			X		X
P_ZVDDP	A	Compensation Resistor to VDDP	X				
P_ZVSS	A	Compensation Resistor to VSS / PCIe® Calibration Positive	X				

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Title: AM4 PCIE/SATAE

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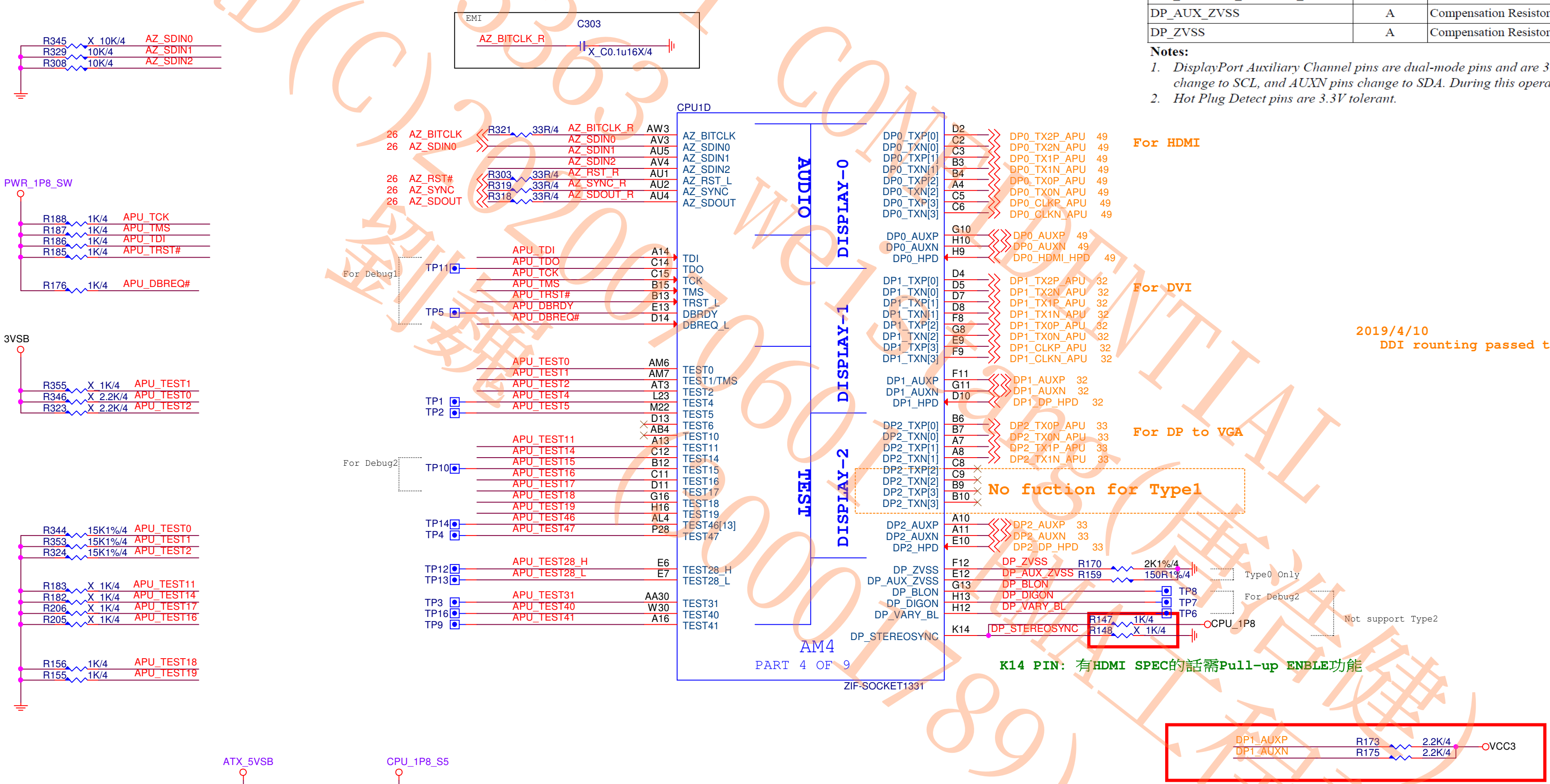
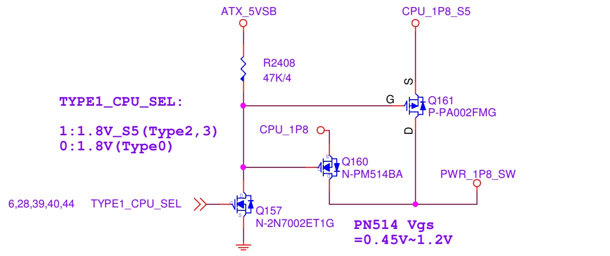


Table 4. Digital Display Interface (DDI) Pin Descriptions

Signal Name	Type	Description	Processor Types 0	1	2	3	4
DP0_TXP[3:0], DP0_TXN[3:0] DP1_TXP[3:0], DP1_TXN[3:0] DP2_TXP[1:0], DP2_TXN[1:0]	O-PCIe-D	DisplayPort Differential Transmitter	X	X		X	
DP2_TXP[3:2], DP2_TXN[3:2]	O-PCIe-D	DisplayPort Differential Transmitter	X			X	
DP0_AUXP, DP0_AUXN DP1_AUXP, DP1_AUXN DP2_AUXP, DP2_AUXN[1]	B-IO18-D	DisplayPort Auxiliary Channel	X	X		X	
DP0_HPD, DP1_HPD, DP2_HPD[2]	I-IO18-S	DisplayPort Hot Plug Detect	X	X		X	
DP_AUX_ZVSS	A	Compensation Resistor to VSS	X				
DP_ZVSS	A	Compensation Resistor to VSS	X				

Notes:

1. *DisplayPort Auxiliary Channel pins are dual-mode pins and are 3.3V tolerant. In I2C mode AUXP pins change to SCL, and AUXN pins change to SDA. During this operation the pin type is B-IO33-OD.*
2. *Hot Plug Detect pins are 3.3V tolerant.*



TYPE1_CPU_SEL:

1:1.8V_S5(Type2,3)
0:1.8V(Type0)

PN514 Vgs =0.45V~1.2V

2019/7/19 (1.1 only)
R2408, Q157, Q160, Q161 are added by Ryan's comment(2019/6/13)

Table 5. LCD Power Interface Pin Descriptions

Signal Name	Type	Description	Processor Types 0	1	2	3	4
DP_BLON	O-IO18-S	Display Panel Backlight Enable	X	X		X	
DP_DIGON	O-IO18-S	Display Panel Power Enable	X	X		X	
DP_STEREOSYNC	B-IO18-S	Signal used to drive active shutter glasses for stereoscopic 3D viewing on 120-Hz panels.	X	X		X	
DP_VARY_BL	O-IO18S	Display Backlight Brightness Control	X	X		X	

MICRO-STAR INT'L CO.,LTD.

Title: AM4 Display/Audio

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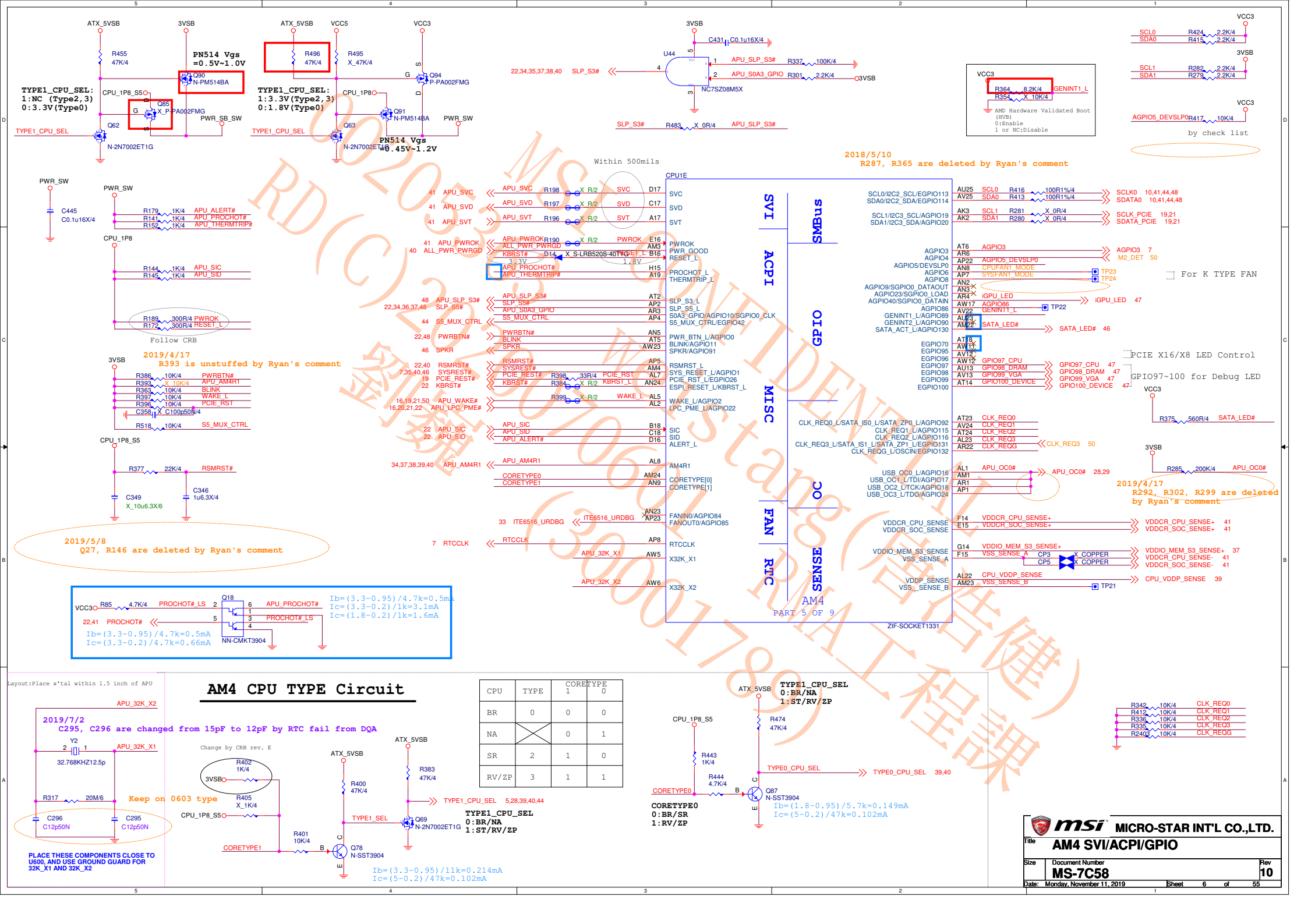
ATX_5VSB
3VSB
VCC5
VCC3
R455 47K/4
R496 47K/4
R495 X_47K/4
PN514 Vgs =0.5V~1.0V
PN514 Vgs =0.45V~1.2V
TYPE1_CPU_SEL: 1:NC (Type2,3) 0:3.3V(Type0)
TYPE1_CPU_SEL: 1:3.3V(Type2,3) 0:1.8V(Type0)
Q90 N-PM514BA
Q85 X_P-PA002FMG
Q62 N-2N7002ET1G
Q94 P-PA002FMG
Q91 N-PM514BA
Q63 N-2N7002ET1G
CPU_1P8_S5
CPU_1P8
PWR_SB_SW
PWR_SW
TYPE1_CPU_SEL
U44
NC7SZ08M5X
C431 C0.1u16X/4
APU_SLP_S3#
APU_S0A3_GPIO
R337 100K/4
R301 2.2K/4
22,34,35,37,38,40 SLP_S3#
SLP_S3#
R483 X_0R/4
APU_SLP_S3#
VCC3
R364 8.2K/4
R354 X_10K/4
GENINT1_L
AMD Hardware Validated Boot (HVB)
0:Enable
1 or NC:Disable
SCL0 R424 2.2K/4
SDA0 R415 2.2K/4
SCL1 R282 2.2K/4
SDA1 R279 2.2K/4
AGPIO5_DEVSLP0 R417 10K/4
by check list
C445 C0.1u16X/4
R179 1K/4 APU_ALERT#
R141 1K/4 APU_PROCHOT#
R152 1K/4 APU_THERMTRIP#
R144 1K/4 APU_SIC
R145 1K/4 APU_SID
R189 300R/4 PWROK
R172 300R/4 RESET_L
Follow CRB
2019/4/17
R393 is unstuffed by Ryan's comment
R386 10K/4 PWRBTN#
R393 X_10K/4 APU_AM4R1
R363 10K/4 BLINK
R397 10K/4 WAKE_L
R396 10K/4 PCIE_RST
C358 X_C100p50N/4
R518 10K/4 S5_MUX_CTRL
R377 22K/4 RSMRST#
C349 X_10u6.3X/6
C346 1u6.3X/4
2019/5/8
Q27, R146 are deleted by Ryan's comment
Within 500mils
CPU1E
SVI
ACPI
MISC
FAN
RTC
GPIO
SMBus
OC
SENSE
AM4
PART 5 OF 9
ZIF-SOCKET1331
APU_SVC R198 X_R/2 SVC D17
APU_SVD R197 X_R/2 SVD C17
APU_SVT R196 X_R/2 SVT A17
APU_PWROK R190 X_R/2 PWROK E16
ALL_PWR_PWRGD AM3
KBRST# D14 X_S-LRB520S-40TVG
APU_PROCHOT# H15
APU_THERMTRIP# A19
APU_SLP_S3# AT2
SLP_S5# AP2
APU_S0A3_GPIO AR3
S5_MUX_CTRL AP4
PWRBTN# AN5
BLINK AT5
SPKR AW23
RSMRST# AP5
SYSRESET# AM4
PCIE_RST# AL7
KBRST# AN24
R399 X_R/2 WAKE_L AL5
APU_WAKE#
APU_LPC_PME# AL2
APU_SIC B18
APU_SID C18
APU_ALERT# D16
APU_AM4R1 AL8
CORETYPE0 AM24
CORETYPE1 AN9
ITE6516_URDBG AN23 AP23
RTCCLK AP8
APU_32K_X1 AW5
APU_32K_X2 AW6
2018/5/10
R287, R365 are deleted by Ryan's comment
SCL0/I2C2_SCL/EGPIO113 AU25 SCL0 R416 100R1%/4 SCLK0 10,41,44,48
SDA0/I2C2_SDA/EGPIO114 AV25 SDA0 R413 100R1%/4 SDATA0 10,41,44,48
SCL1/I2C3_SCL/AGPIO19 AK3 SCL1 R281 X_0R/4 SCLK_PCIE 19,21
SDA1/I2C3_SDA/AGPIO20 AK2 SDA1 R280 X_0R/4 SDATA_PCIE 19,21
AGPIO3 AT6 AGPIO3 AGPIO3 7
AGPIO4 AR6 M2_DET 50
AGPIO5/DEVSLP0 AP22 AGPIO5_DEVSLP0
AGPIO6 AN8 CPUFAN1_MODE
AGPIO8 AP7 SYSFAN1_MODE TP23
AN2 TP24
AGPIO9/SGPIO0_DATAOUT AN3
AGPIO23/SGPIO0_LOAD AR4 iGPU_LED
AGPIO40/SGPIO0_DATAIN AW17 AGPIO86 iGPU_LED 47
AGPIO86 AV22 GENINT1_L TP22
GENINT1_L/AGPIO89 AL23
GENINT2_L/AGPIO90 AM22 SATA_LED# SATA_LED# 46
SATA_ACT_L/AGPIO130 AT18
EGPIO70 AW11
EGPIO95 AV13
EGPIO96 AW12 GPIO97_CPU GPIO97_CPU 47
EGPIO97 AU13 GPIO98_DRAM GPIO98_DRAM 47
EGPIO98 AV13 GPIO99_VGA GPIO99_VGA 47
EGPIO99 AT14 GPIO100_DEVICE GPIO100_DEVICE 47
EGPIO100
For K TYPE FAN
PCIE X16/X8 LED Control
GPIO97~100 for Debug LED
VCC3
R375 560R/4 SATA_LED#
CLK_REQ0_L/SATA_IS0_L/SATA_ZP0_L/AGPIO92 AT23 CLK_REQ0
CLK_REQ1_L/AGPIO115 AV24 CLK_REQ1
CLK_REQ2_L/AGPIO116 AT24 CLK_REQ2
CLK_REQ3_L/SATA_IS1_L/SATA_ZP1_L/EGPIO131 AL23 CLK_REQ3 CLK_REQ3 50
CLK_REQG_L/OSCIN/EGPIO132 AR22 CLK_REQG
USB_OC0_L/AGPIO16 AL1 APU_OC0# APU_OC0# 28,29
USB_OC1_L/TDI/AGPIO17 AM1
USB_OC2_L/TCK/AGPIO18 AR1
USB_OC3_L/TDO/AGPIO24 AP1
3VSB
R285 200K/4 APU_OC0#
2019/4/17
R292, R302, R299 are deleted by Ryan's comment
VDDCR_CPU_SENSE AF14 VDDCR_CPU_SENSE+ VDDCR_CPU_SENSE+ 41
VDDCR_SOC_SENSE AE15 VDDCR_SOC_SENSE+ VDDCR_SOC_SENSE+ 41
VDDIO_MEM_S3_SENSE G14 VDDIO_MEM_S3_SENSE+ VDDIO_MEM_S3_SENSE+ 37
VSS_SENSE_A F15 VDDCR_CPU_SENSE- VDDCR_CPU_SENSE- 41
CP3 X_COPPER
CP5 X_COPPER
VDDP_SENSE AL22 CPU_VDDP_SENSE CPU_VDDP_SENSE 39
VSS_SENSE_B AM23 TP21
R342 10K/4 CLK_REQ0
R412 10K/4 CLK_REQ1
R336 10K/4 CLK_REQ2
R335 10K/4 CLK_REQ3
R2403 10K/4 CLK_REQG
Q18 NN-CMKT3904
VCC3 R85 4.7K/4 PROCHOT#_LS APU_PROCHOT#
22,41 PROCHOT# PROCHOT#_LS
Ib=(3.3-0.95)/4.7k=0.5mA
Ic=(3.3-0.2)/4.7k=0.66mA
Ib=(3.3-0.95)/4.7k=0.5mA
Ic=(3.3-0.2)/1k=3.1mA
Ic=(1.8-0.2)/1k=1.6mA
AM4 CPU TYPE Circuit
Layout:Place x'tal within 1.5 inch of APU
APU_32K_X2
2019/7/2
C295, C296 are changed from 15pF to 12pF by RTC fail from DQA
Y2 32.768KHZ12.5p
APU_32K_X1
R317 20M/6
Keep on 0603 type
C296 C12p50N
C295 C12p50N
PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2
Change by CRB rev. E
3VSB R402 1K/4
R405 X_1K/4
CPU_1P8_S5
CORETYPE1
R401 10K/4
Q78 N-SST3904
ATX_5VSB
R400 47K/4
R383 47K/4
TYPE1_SEL
Q69 N-2N7002ET1G
TYPE1_CPU_SEL 5,28,39,40,44
TYPE1_CPU_SEL
0:BR/NA
1:ST/RV/ZP
Ib=(3.3-0.95)/11k=0.214mA
Ic=(5-0.2)/47k=0.102mA
CPU_1P8_S5
R443 1K/4
R444 4.7K/4
CORETYPE0
R474 47K/4
TYPE0_CPU_SEL
TYPE0_CPU_SEL 39,40
Q87 N-SST3904
CORETYPE0
0:BR/SR
1:RV/ZP
Ib=(1.8-0.2)/5.7k=0.149mA
Ic=(5-0.2)/47k=0.102mA
CPU TYPE CORETYPE 1 0
BR 0 0 0
NA X 0 1
SR 2 1 0
RV/ZP 3 1 1
MICRO-STAR INT'L CO.,LTD.
Title
AM4 SVI/ACPI/GPIO
Size
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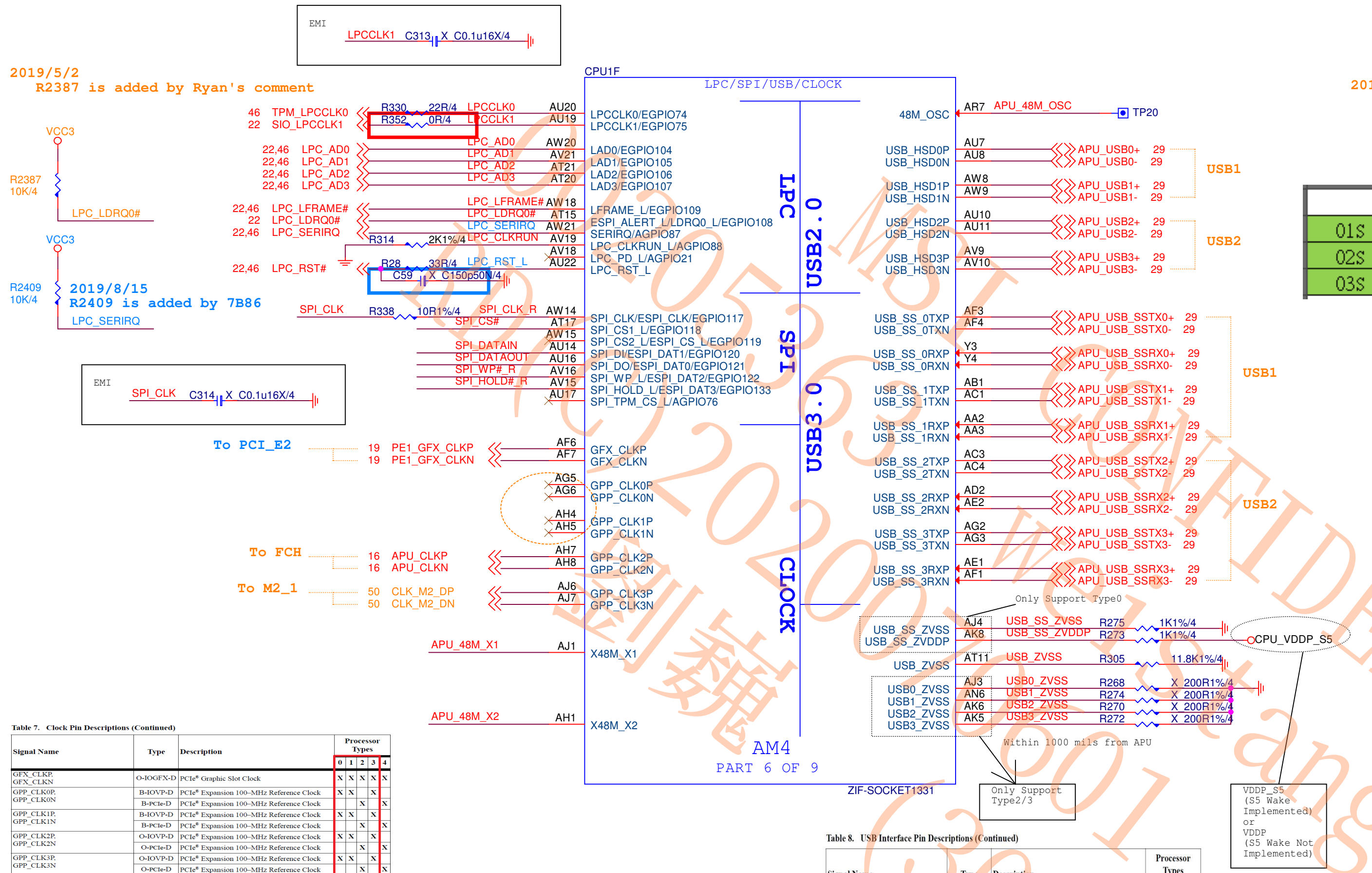


EMI
LPCCLK1 C313 X_C0.1u16X/4
2019/5/2
R2387 is added by Ryan's comment
CPU1F
LPC/SPI/USB/CLOCK
46 TPM_LPCCLK0
22 SIO_LPCCLK1
R330 22R/4 LPCCLK0 AU20 LPCCLK0/EGPIO74
R352 0R/4 LPCCLK1 AU19 LPCCLK1/EGPIO75
VCC3
R2387 10K/4
LPC_LDRQ0#
22,46 LPC_AD0
22,46 LPC_AD1
22,46 LPC_AD2
22,46 LPC_AD3
AW20 LAD0/EGPIO104
AV21 LAD1/EGPIO105
AT21 LAD2/EGPIO106
AT20 LAD3/EGPIO107
22,46 LPC_LFRAME#
22 LPC_LDRQ0#
22,46 LPC_SERIRQ
AW18 LFRAME_L/EGPIO109
AT15 ESPI_ALERT_L/LDRQ0_L/EGPIO108
AW21 SERIRQ/AGPIO87
R314 2K1%/4 LPC_CLKRUN AV19 LPC_CLKRUN_L/AGPIO88
AV18 LPC_PD_L/AGPIO21
22,46 LPC_RST#
R28 33R/4 LPC_RST_L AU22 LPC_RST_L
C59 X_C150p50N/4
R2409 10K/4
2019/8/15
R2409 is added by 7B86
LPC_SERIRQ
SPI_CLK R338 10R1%/4 SPI_CLK_R AW14 SPI_CLK/ESPI_CLK/EGPIO117
SPI_CS# AT17 SPI_CS1_L/EGPIO118
AW15 SPI_CS2_L/ESPI_CS_L/EGPIO119
SPI_DATAIN AU14 SPI_DI/ESPI_DAT1/EGPIO120
SPI_DATAOUT AU16 SPI_DO/ESPI_DAT0/EGPIO121
SPI_WP#_R AV16 SPI_WP_L/ESPI_DAT2/EGPIO122
SPI_HOLD#_R AV15 SPI_HOLD_L/ESPI_DAT3/EGPIO133
AU17 SPI_TPM_CS_L/AGPIO76
EMI
SPI_CLK C314 X_C0.1u16X/4
To PCI_E2
19 PE1_GFX_CLKP AF6 GFX_CLKP
19 PE1_GFX_CLKN AF7 GFX_CLKN
AG5 GPP_CLK0P
AG6 GPP_CLK0N
AH4 GPP_CLK1P
AH5 GPP_CLK1N
To FCH
16 APU_CLKP AH7 GPP_CLK2P
16 APU_CLKN AH8 GPP_CLK2N
To M2_1
50 CLK_M2_DP AJ6 GPP_CLK3P
50 CLK_M2_DN AJ7 GPP_CLK3N
APU_48M_X1 AJ1 X48M_X1
APU_48M_X2 AH1 X48M_X2
LPC
USB2.0
SPI
USB3.0
CLOCK
AM4
PART 6 OF 9
ZIF-SOCKET1331
48M_OSC AR7 APU_48M_OSC TP20
USB_HSD0P AU7 APU_USB0+ 29
USB_HSD0N AU8 APU_USB0- 29
USB_HSD1P AW8 APU_USB1+ 29
USB_HSD1N AW9 APU_USB1- 29
USB1
USB_HSD2P AU10 APU_USB2+ 29
USB_HSD2N AU11 APU_USB2- 29
USB_HSD3P AV9 APU_USB3+ 29
USB_HSD3N AV10 APU_USB3- 29
USB2
USB_SS_0TXP AF3 APU_USB_SSTX0+ 29
USB_SS_0TXN AF4 APU_USB_SSTX0- 29
USB_SS_0RXP Y3 APU_USB_SSRX0+ 29
USB_SS_0RXN Y4 APU_USB_SSRX0- 29
USB_SS_1TXP AB1 APU_USB_SSTX1+ 29
USB_SS_1TXN AC1 APU_USB_SSTX1- 29
USB_SS_1RXP AA2 APU_USB_SSRX1+ 29
USB_SS_1RXN AA3 APU_USB_SSRX1- 29
USB1
USB_SS_2TXP AC3 APU_USB_SSTX2+ 29
USB_SS_2TXN AC4 APU_USB_SSTX2- 29
USB_SS_2RXP AD2 APU_USB_SSRX2+ 29
USB_SS_2RXN AE2 APU_USB_SSRX2- 29
USB_SS_3TXP AG2 APU_USB_SSTX3+ 29
USB_SS_3TXN AG3 APU_USB_SSTX3- 29
USB_SS_3RXP AE1 APU_USB_SSRX3+ 29
USB_SS_3RXN AF1 APU_USB_SSRX3- 29
USB2
Only Support Type0
USB_SS_ZVSS AJ4 USB_SS_ZVSS R275 1K1%/4
USB_SS_ZVDDP AK8 USB_SS_ZVDDP R273 1K1%/4
CPU_VDDP_S5
USB_ZVSS AT11 USB_ZVSS R305 11.8K1%/4
USB0_ZVSS AJ3 USB0_ZVSS R268 X_200R1%/4
USB1_ZVSS AN6 USB1_ZVSS R274 X_200R1%/4
USB2_ZVSS AK6 USB2_ZVSS R270 X_200R1%/4
USB3_ZVSS AK5 USB3_ZVSS R272 X_200R1%/4
Within 1000 mils from APU
Only Support Type2/3
VDDP_S5 (S5 Wake Implemented) or VDDP (S5 Wake Not Implemented)

Table 7. Clock Pin Descriptions (Continued)

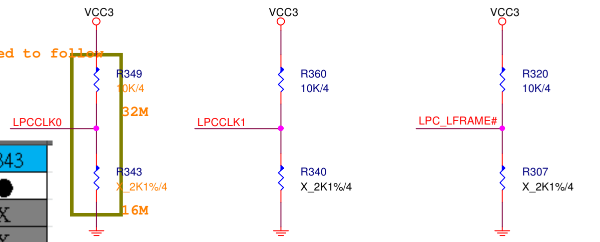
Signal Name	Type	Description	Processor Types 0	1	2	3	4
GFX_CLKP, GFX_CLKN	O-IOGFX-D	PCIe® Graphic Slot Clock	X	X	X	X	X
GPP_CLK0P, GPP_CLK0N	B-IOVP-D	PCIe® Expansion 100–MHz Reference Clock	X	X		X	
	B-PCIe-D	PCIe® Expansion 100–MHz Reference Clock			X		X
GPP_CLK1P, GPP_CLK1N	B-IOVP-D	PCIe® Expansion 100–MHz Reference Clock	X	X		X	
	B-PCIe-D	PCIe® Expansion 100–MHz Reference Clock			X		X
GPP_CLK2P, GPP_CLK2N	O-IOVP-D	PCIe® Expansion 100–MHz Reference Clock	X	X		X	
	O-PCIe-D	PCIe® Expansion 100–MHz Reference Clock			X		X
GPP_CLK3P, GPP_CLK3N	O-IOVP-D	PCIe® Expansion 100–MHz Reference Clock	X	X		X	
	O-PCIe-D	PCIe® Expansion 100–MHz Reference Clock			X		X
X48M_X1	I-IOVPS5-S	48–MHz Crystal Clock 1 **Note:** *Power rail may be tied to S0-S5 or S0-S3.*	X	X	X	X	X
X48M_X2	I-IOVPS5-S	48–MHz Crystal Clock 2 **Note:** *Power rail may be tied to S0-S5 or S0-S3.*	X	X	X	X	X
X32K_X1	I-RTC-S	32–kHz Real Time Clock Crystal Oscillator Input 1 **Note:** *Input must be active at all times.*	X	X	X	X	X
X32K_X2	I-RTC-S	32–kHz Real Time Clock Crystal Oscillator Input 2 **Note:** *Input must be active at all times.*	X	X	X	X	X
RTCCLK	O-IO33S5-S	Real Time Clock 32–kHz Output	X				
	O-IO18S5-S	Real Time Clock 32–kHz Output		X	X	X	X

Table 8. USB Interface Pin Descriptions (Continued)

Signal Name	Type	Description	Processor Types 0	1	2	3	4
48M_OSC	B-IO33S5-S	48–MHz USB Clock	X				
	B-IO18S5-S	48–MHz USB Clock		X	X	X	X
USB_ZVSS,	A	USB Compensating Resistor to VSS	X				
USB[3:0]_ZVSS,	A	USB Compensating Resistor to VSS		X	X	X	
USB_SS_ZVSS	A	USB SS Compensation Resistor to VSS	X				
USB_SS_ZVDDP	A	Compensation Resistor to USB SS Power Supply	X				

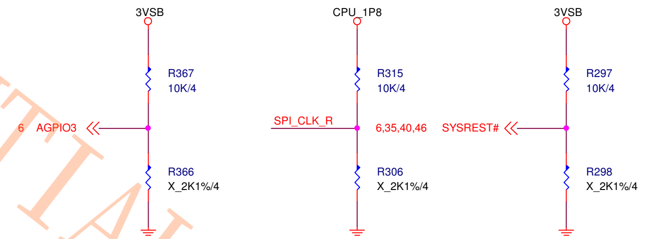
Strapping Options

2019/5/14
R349 & R343 passed to follow up PM's spec



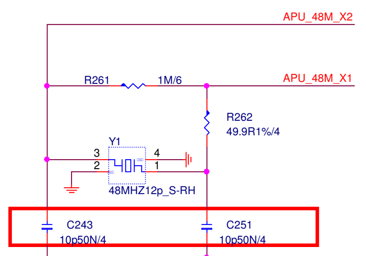
	R349	R343
01S	X	●
02S	●	X
03S	●	X

	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled	Configured for Internal clock generator (Default)	SPI ROM (Default)
PULL LOW	LPC device Boot Fail Timer Disabled (Default)	Configured for External clock generator ?????	LPC ROM



	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode

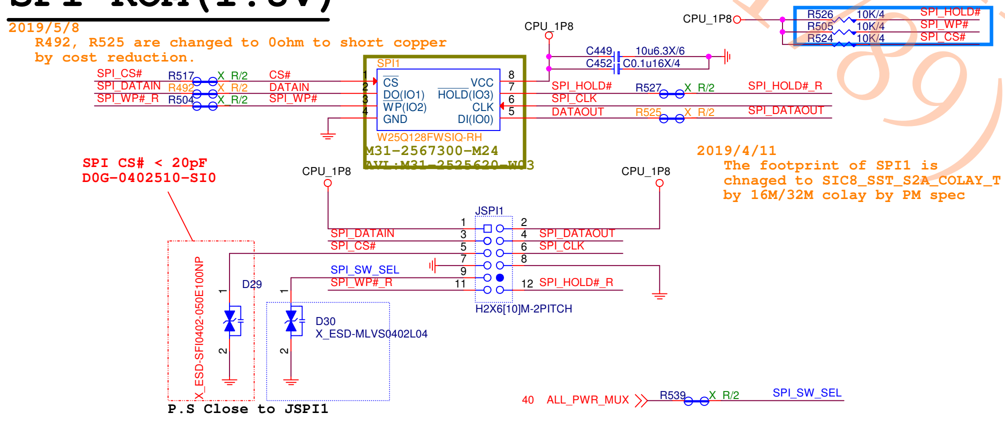
Layout:Place x'tal within 1.5 inch of APU



PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR48M_X1 AND 48M_X2

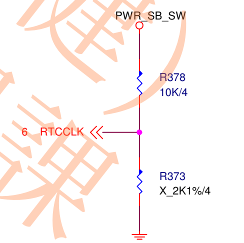
SPI ROM(1.8V)

2019/5/8
R492, R525 are changed to 0ohm to short copper by cost reduction.

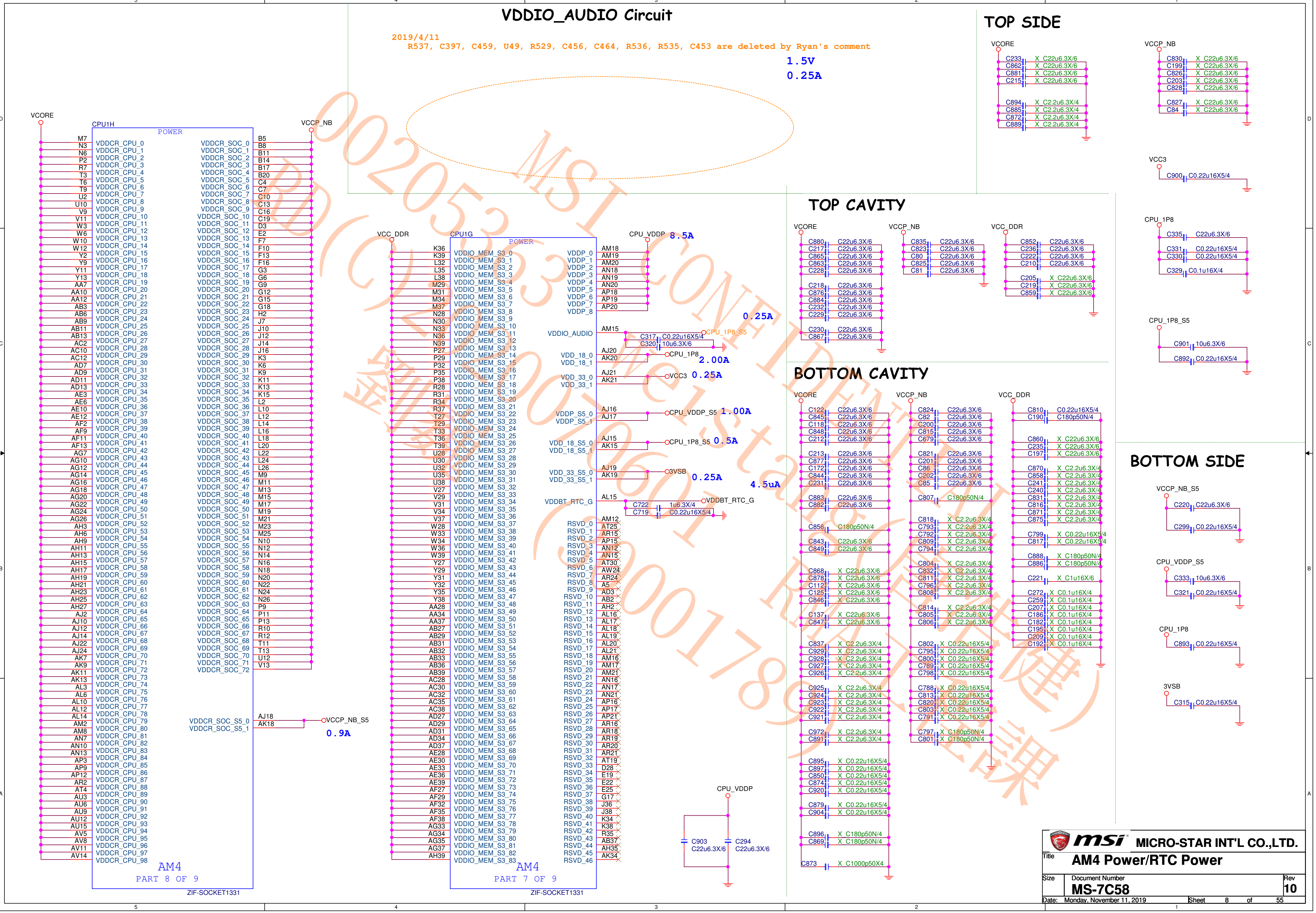


CPU_1P8
C449 10u6.3X/6
C452 C0.1u16X/4
CPU_1P8
R526 10K/4 SPI_HOLD#
R505 10K/4 SPI_WP#
R524 10K/4 SPI_CS#
SPI1
SPI_CS# R517 X_R/2 CS#
SPI_DATAIN R492 X_R/2 DATAIN
SPI_WP#_R R504 X_R/2 SPI_WP#
CS VCC
DO(IO1) HOLD(IO3)
WP(IO2) CLK
GND DI(IO0)
SPI_HOLD# R527 X_R/2 SPI_HOLD#_R
SPI_CLK
DATAOUT R525 X_R/2 SPI_DATAOUT
W25Q128FWSIQ-RH
M31-2567300-M24
AVL:M31-2525620-W03
SPI CS# < 20pF
D0G-0402510-SI0
CPU_1P8
CPU_1P8
JSPI1
SPI_DATAIN
SPI_CS#
SPI_SW_SEL
SPI_WP#_R
SPI_DATAOUT
SPI_CLK
SPI_HOLD#_R
H2X6[10]M-2PITCH
D29
X_ESD-SFI0402-050E100NP
D30
X_ESD-MLVS0402L04
P.S Close to JSPI1
40 ALL_PWR_MUX R539 X_R/2 SPI_SW_SEL

2019/4/11
The footprint of SPI1 is chnaged to SIC8_SST_S2A_COLAY_T by 16M/32M colay by PM spec



	RTCCLK
PULL HIGH	RTC Coin Battery is on board (Default)
PULL LOW	RTC Coin Battery is not on board



VDDIO_AUDIO Circuit
2019/4/11
R537, C397, C459, U49, R529, C456, C464, R536, R535, C453 are deleted by Ryan's comment
1.5V
0.25A
TOP SIDE
TOP CAVITY
BOTTOM CAVITY
BOTTOM SIDE
VCORE
VCCP_NB
VCC_DDR
VCC3
CPU_1P8
CPU_1P8_S5
VCCP_NB_S5
CPU_VDDP_S5
3VSB
CPU_VDDP
CPU1H
POWER
AM4
PART 8 OF 9
ZIF-SOCKET1331
CPU1G
AM4
PART 7 OF 9
ZIF-SOCKET1331
VDDIO_AUDIO
VDDBT_RTC_G
8.5A
0.25A
2.00A
0.25A
1.00A
0.5A
0.25A
4.5uA
0.9A
MICRO-STAR INT'L CO.,LTD.
Title
AM4 Power/RTC Power
Size
Document Number
MS-7C58
Rev
10
Date: Monday, November 11, 2019
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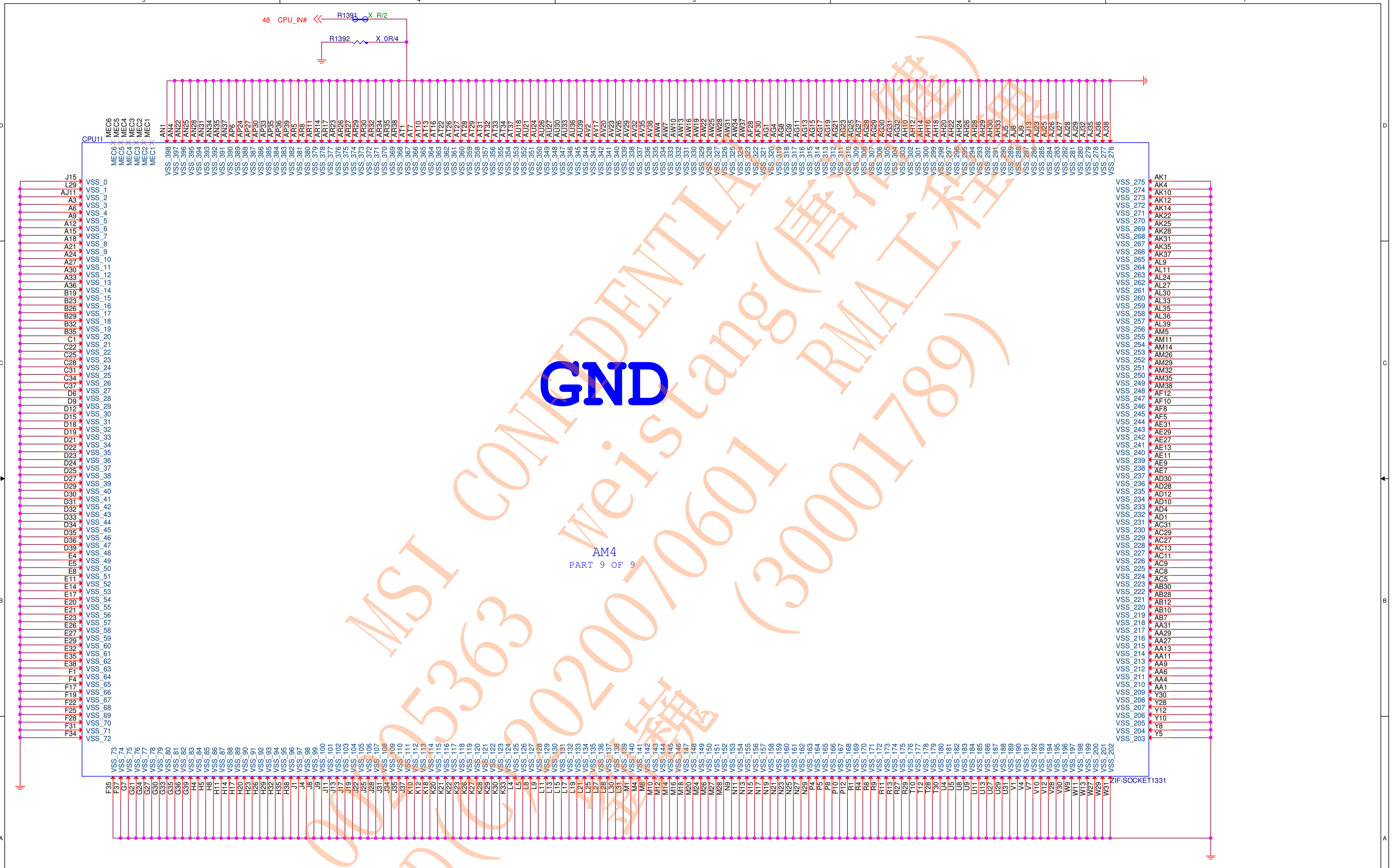

MICRO-STAR INT'L CO.,LTD.
Title: AM4 GND
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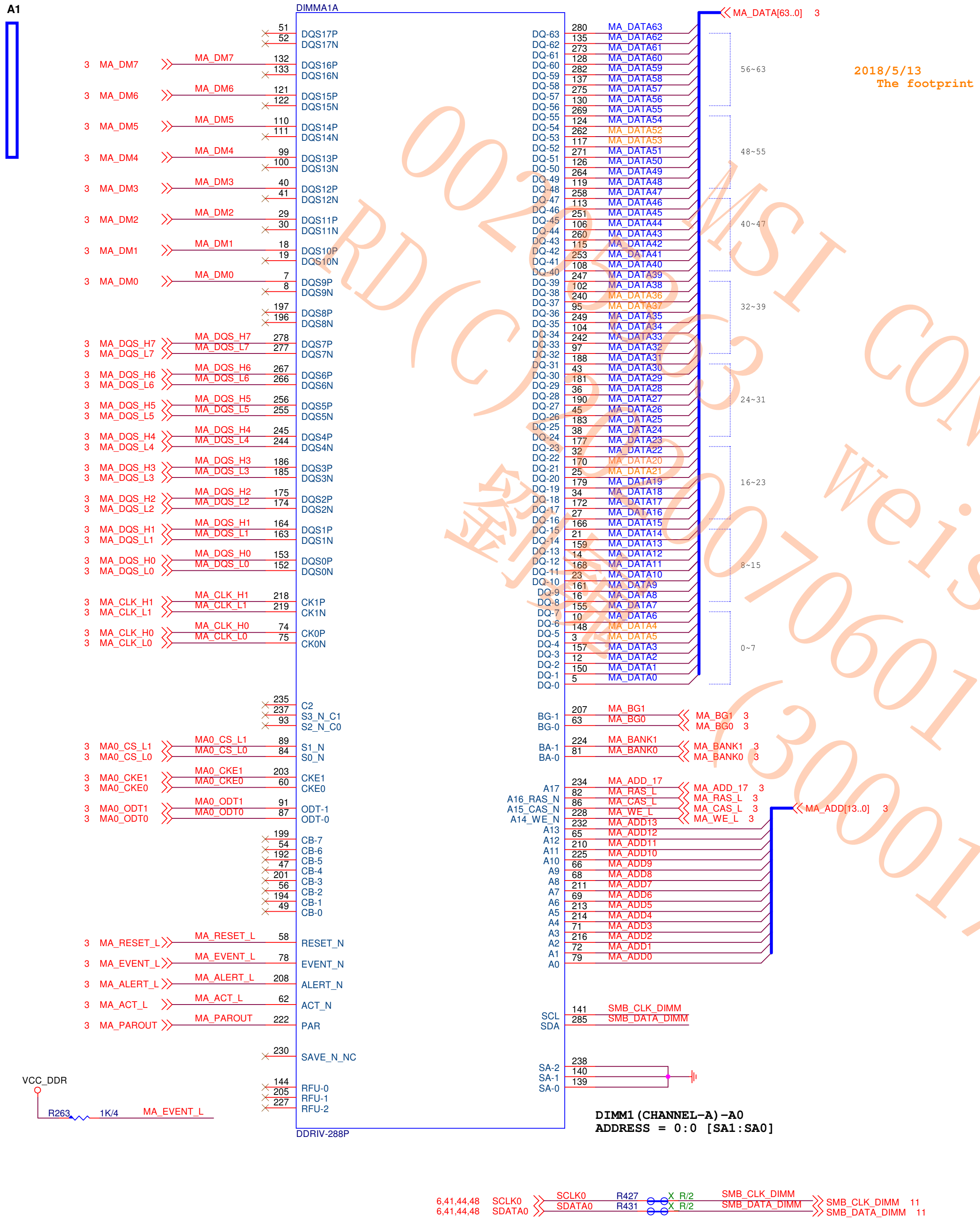
A1
DIMMA1A
DDRIV-288P
MA_DATA[63..0] 3
56~63
48~55
40~47
32~39
24~31
16~23
8~15
0~7
MA_DM7 … MA_DM0
MA_DQS_H7 … MA_DQS_H0
MA_DQS_L7 … MA_DQS_L0
MA_CLK_H1 MA_CLK_L1 MA_CLK_H0 MA_CLK_L0
MA0_CS_L1 MA0_CS_L0
MA0_CKE1 MA0_CKE0
MA0_ODT1 MA0_ODT0
MA_RESET_L MA_EVENT_L MA_ALERT_L MA_ACT_L MA_PAROUT
DQS17P DQS17N … DQS0P DQS0N
CK1P CK1N CK0P CK0N
C2 S3_N_C1 S2_N_C0 S1_N S0_N CKE1 CKE0 ODT-1 ODT-0
CB-7 … CB-0
RESET_N EVENT_N ALERT_N ACT_N PAR SAVE_N_NC RFU-0 RFU-1 RFU-2
DQ-63 … DQ-0
MA_DATA63 … MA_DATA0
BG-1 BG-0 MA_BG1 3 MA_BG0 3
BA-1 BA-0 MA_BANK1 3 MA_BANK0 3
A17 A16_RAS_N A15_CAS_N A14_WE_N A13 … A0
MA_ADD_17 3 MA_RAS_L 3 MA_CAS_L 3 MA_WE_L 3
MA_ADD[13..0] 3
MA_ADD13 … MA_ADD0
SCL SDA SMB_CLK_DIMM SMB_DATA_DIMM
SA-2 SA-1 SA-0
VCC_DDR
R263 1K/4 MA_EVENT_L
DIMM1(CHANNEL-A)-A0
ADDRESS = 0:0 [SA1:SA0]
6,41,44,48 SCLK0 SCLK0 R427 X R/2 SMB_CLK_DIMM SMB_CLK_DIMM 11
6,41,44,48 SDATA0 SDATA0 R431 X R/2 SMB_DATA_DIMM SMB_DATA_DIMM 11

2018/5/13
The footprint of DIMMA1 is changed to DDRIV_D288_1_T_7A17 by the latest result from Ryan's comment

MICRO-STAR INT'L CO.,LTD.

Title: DDR4 DIMM CH-A

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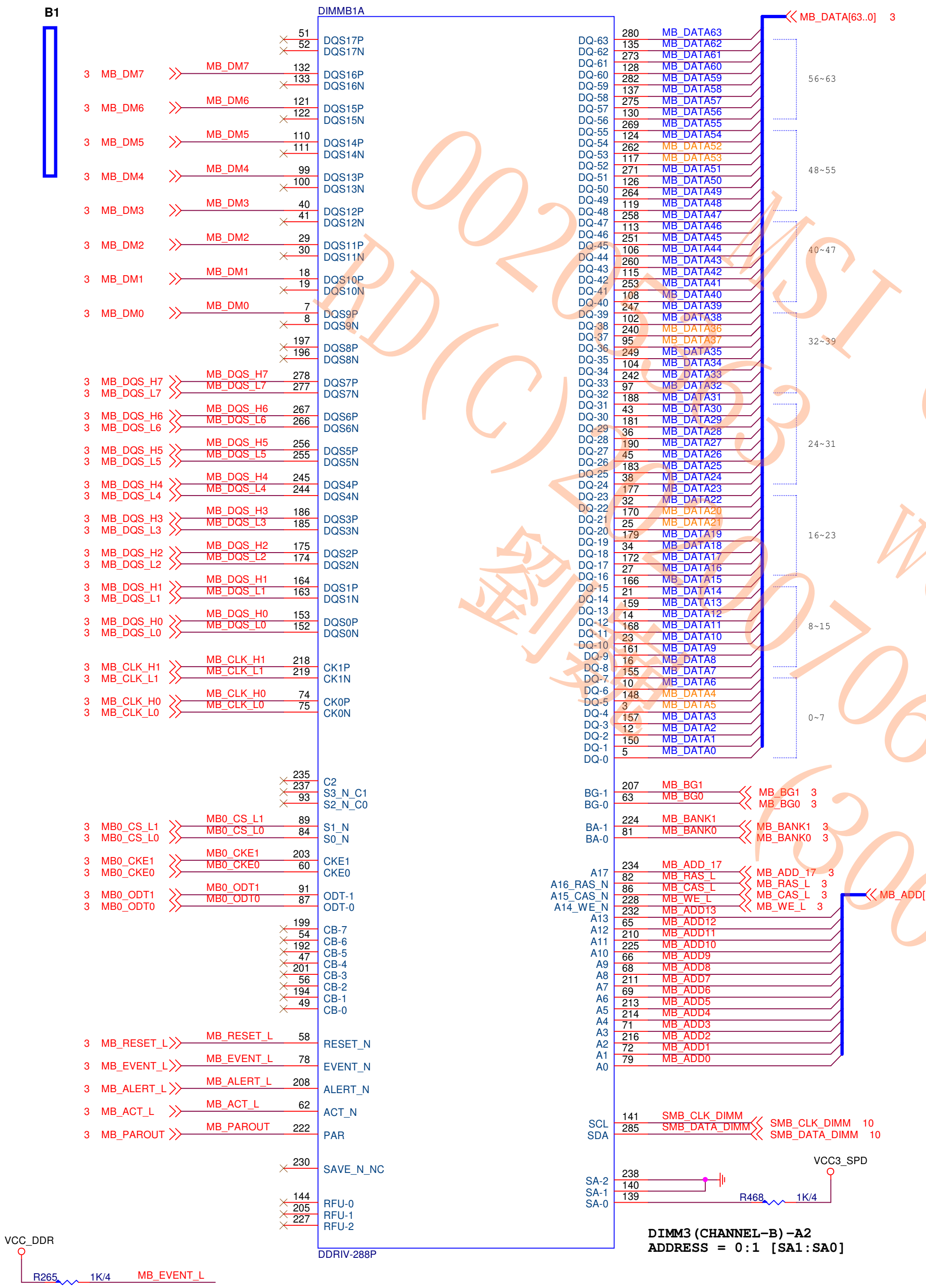
B1
DIMMB1A
DDRIV-288P
3 MB_DM7 / MB_DM7 132 DQS16P, 133 DQS16N
3 MB_DM6 / MB_DM6 121 DQS15P, 122 DQS15N
3 MB_DM5 / MB_DM5 110 DQS14P, 111 DQS14N
3 MB_DM4 / MB_DM4 99 DQS13P, 100 DQS13N
3 MB_DM3 / MB_DM3 40 DQS12P, 41 DQS12N
3 MB_DM2 / MB_DM2 29 DQS11P, 30 DQS11N
3 MB_DM1 / MB_DM1 18 DQS10P, 19 DQS10N
3 MB_DM0 / MB_DM0 7 DQS9P, 8 DQS9N
51 DQS17P, 52 DQS17N
197 DQS8P, 196 DQS8N
3 MB_DQS_H7 278 DQS7P / 3 MB_DQS_L7 277 DQS7N
3 MB_DQS_H6 267 DQS6P / 3 MB_DQS_L6 266 DQS6N
3 MB_DQS_H5 256 DQS5P / 3 MB_DQS_L5 255 DQS5N
3 MB_DQS_H4 245 DQS4P / 3 MB_DQS_L4 244 DQS4N
3 MB_DQS_H3 186 DQS3P / 3 MB_DQS_L3 185 DQS3N
3 MB_DQS_H2 175 DQS2P / 3 MB_DQS_L2 174 DQS2N
3 MB_DQS_H1 164 DQS1P / 3 MB_DQS_L1 163 DQS1N
3 MB_DQS_H0 153 DQS0P / 3 MB_DQS_L0 152 DQS0N
3 MB_CLK_H1 218 CK1P / 3 MB_CLK_L1 219 CK1N
3 MB_CLK_H0 74 CK0P / 3 MB_CLK_L0 75 CK0N
235 C2, 237 S3_N_C1, 93 S2_N_C0
3 MB0_CS_L1 89 S1_N / 3 MB0_CS_L0 84 S0_N
3 MB0_CKE1 203 CKE1 / 3 MB0_CKE0 60 CKE0
3 MB0_ODT1 91 ODT-1 / 3 MB0_ODT0 87 ODT-0
199 CB-7, 54 CB-6, 192 CB-5, 47 CB-4, 201 CB-3, 56 CB-2, 194 CB-1, 49 CB-0
3 MB_RESET_L 58 RESET_N
3 MB_EVENT_L 78 EVENT_N
3 MB_ALERT_L 208 ALERT_N
3 MB_ACT_L 62 ACT_N
3 MB_PAROUT 222 PAR
230 SAVE_N_NC
144 RFU-0, 205 RFU-1, 227 RFU-2
VCC_DDR R265 1K/4 MB_EVENT_L
MB_DATA[63..0] 3
DQ-63 280 MB_DATA63; DQ-62 135 MB_DATA62; DQ-61 273 MB_DATA61; DQ-60 128 MB_DATA60; DQ-59 282 MB_DATA59; DQ-58 137 MB_DATA58; DQ-57 275 MB_DATA57; DQ-56 130 MB_DATA56
DQ-55 269 MB_DATA55; DQ-54 124 MB_DATA54; DQ-53 262 MB_DATA52; DQ-52 117 MB_DATA53; DQ-51 271 MB_DATA51; DQ-50 126 MB_DATA50; DQ-49 264 MB_DATA49; DQ-48 119 MB_DATA48
DQ-47 258 MB_DATA47; DQ-46 113 MB_DATA46; DQ-45 251 MB_DATA45; DQ-44 106 MB_DATA44; DQ-43 260 MB_DATA43; DQ-42 115 MB_DATA42; DQ-41 253 MB_DATA41; DQ-40 108 MB_DATA40
DQ-39 247 MB_DATA39; DQ-38 102 MB_DATA38; DQ-37 240 MB_DATA36; DQ-36 95 MB_DATA37; DQ-35 249 MB_DATA35; DQ-34 104 MB_DATA34; DQ-33 242 MB_DATA33; DQ-32 97 MB_DATA32
DQ-31 188 MB_DATA31; DQ-30 43 MB_DATA30; DQ-29 181 MB_DATA29; DQ-28 36 MB_DATA28; DQ-27 190 MB_DATA27; DQ-26 45 MB_DATA26; DQ-25 183 MB_DATA25; DQ-24 38 MB_DATA24
DQ-23 177 MB_DATA23; DQ-22 32 MB_DATA22; DQ-21 170 MB_DATA20; DQ-20 25 MB_DATA21; DQ-19 179 MB_DATA19; DQ-18 34 MB_DATA18; DQ-17 172 MB_DATA17; DQ-16 27 MB_DATA16
DQ-15 166 MB_DATA15; DQ-14 21 MB_DATA14; DQ-13 159 MB_DATA13; DQ-12 14 MB_DATA12; DQ-11 168 MB_DATA11; DQ-10 23 MB_DATA10; DQ-9 161 MB_DATA9; DQ-8 16 MB_DATA8
DQ-7 155 MB_DATA7; DQ-6 10 MB_DATA6; DQ-5 148 MB_DATA4; DQ-4 3 MB_DATA5; DQ-3 157 MB_DATA3; DQ-2 12 MB_DATA2; DQ-1 150 MB_DATA1; DQ-0 5 MB_DATA0
56~63
48~55
40~47
32~39
24~31
16~23
8~15
0~7
BG-1 207 MB_BG1 — MB_BG1 3; BG-0 63 MB_BG0 — MB_BG0 3
BA-1 224 MB_BANK1 — MB_BANK1 3; BA-0 81 MB_BANK0 — MB_BANK0 3
A17 234 MB_ADD_17 — MB_ADD_17 3
A16_RAS_N 82 MB_RAS_L — MB_RAS_L 3
A15_CAS_N 86 MB_CAS_L — MB_CAS_L 3
A14_WE_N 228 MB_WE_L — MB_WE_L 3
MB_ADD[13..0] 3
A13 232 MB_ADD13; A12 65 MB_ADD12; A11 210 MB_ADD11; A10 225 MB_ADD10; A9 66 MB_ADD9; A8 68 MB_ADD8; A7 211 MB_ADD7; A6 69 MB_ADD6; A5 213 MB_ADD5; A4 214 MB_ADD4; A3 71 MB_ADD3; A2 216 MB_ADD2; A1 72 MB_ADD1; A0 79 MB_ADD0
SCL 141 SMB_CLK_DIMM — SMB_CLK_DIMM 10
SDA 285 SMB_DATA_DIMM — SMB_DATA_DIMM 10
SA-2 238, SA-1 140, SA-0 139
VCC3_SPD R468 1K/4
DIMM3(CHANNEL-B)-A2
ADDRESS = 0:1 [SA1:SA0]

2018/5/13
The footprint of DIMMB1 is changed to DDRIV_D288_1_T_7A17 by the latest result from Ryan's comment

MICRO-STAR INT'L CO.,LTD.			
Title	DDR4 DIMM CH-B		
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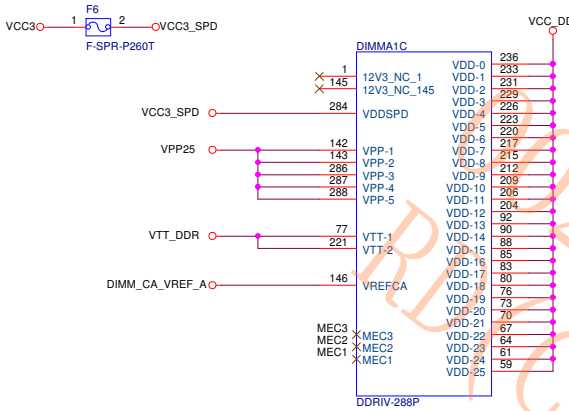
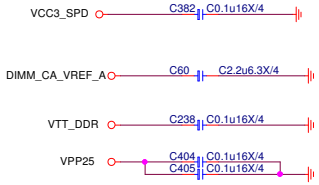
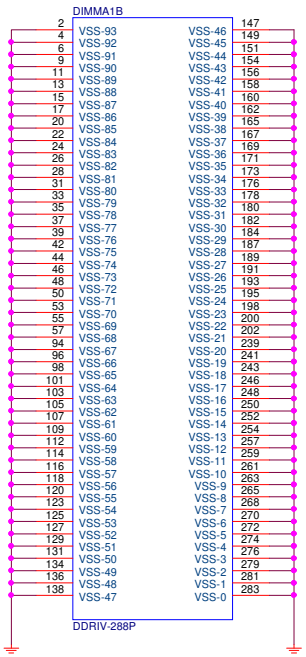


2018/5/13
The footprint of DIMMA1 is changed to DDRIV_D288_1_T_7A17 by the latest result from Ryan's comment

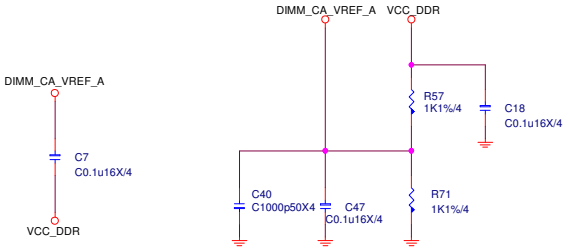




2018/5/13
The footprint of DIMMA1 is changed to DDRIV_D288_1_T_7A17 by the latest result from Ryan's comment

DDR VREF

(place resistors close to DIMMs)



MICRO-STAR INT'L CO.,LTD.

Title: DDR4-POWER/GND-1

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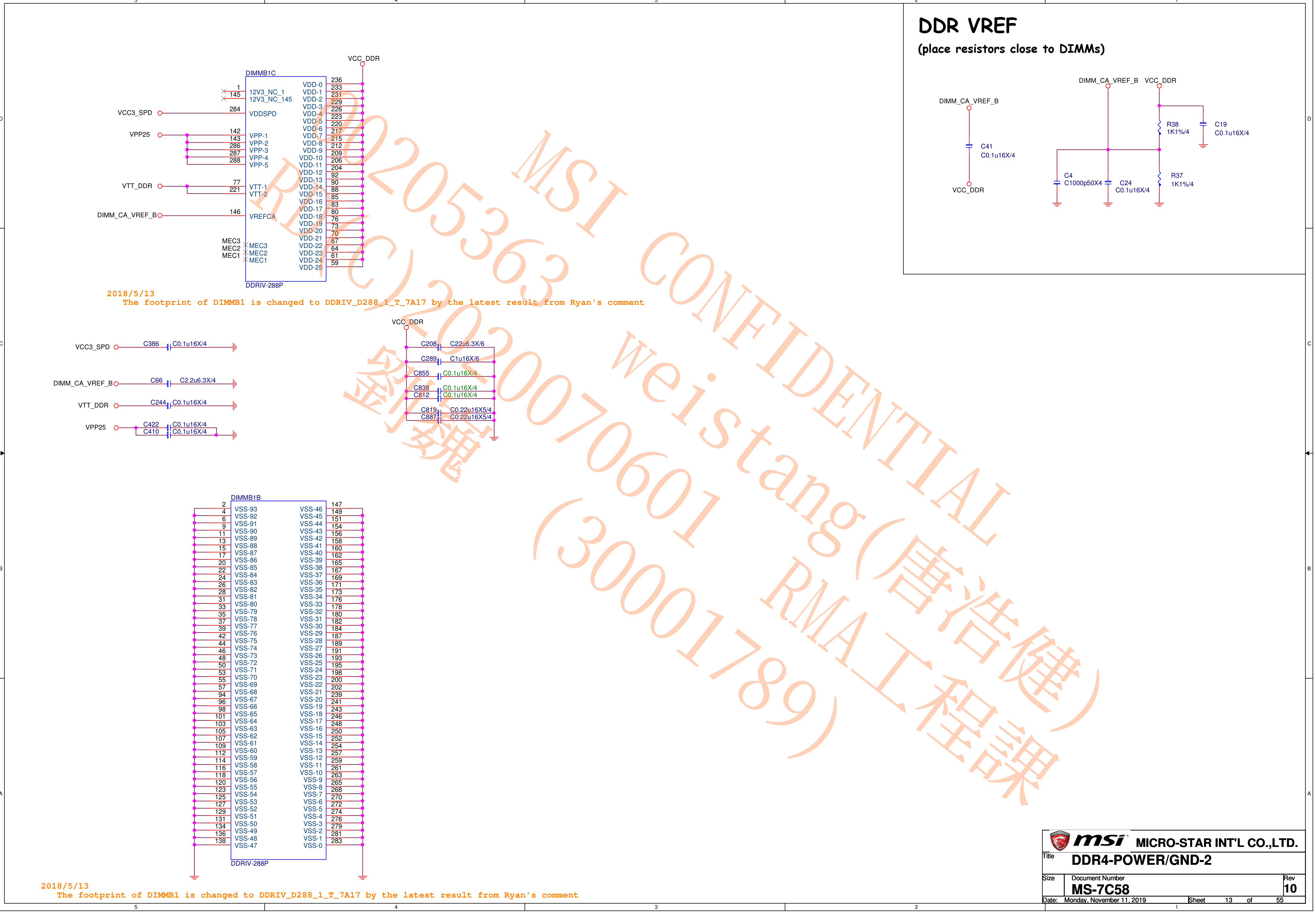
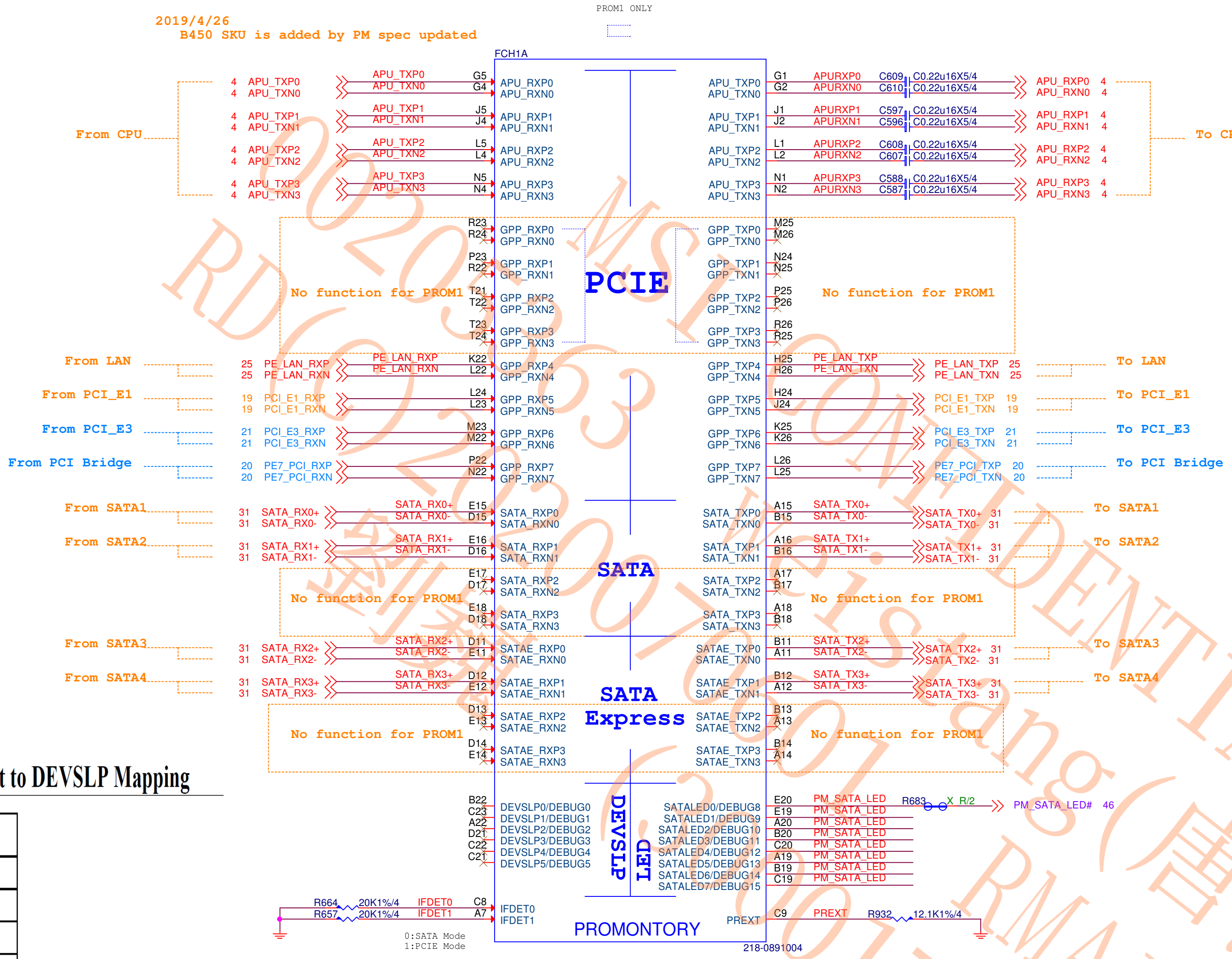

DDR VREF
(place resistors close to DIMMs)
DIMM_CA_VREF_B
C41 C0.1u16X/4
VCC_DDR
DIMM_CA_VREF_B VCC_DDR
R38 1K1%/4
C19 C0.1u16X/4
C4 C1000p50X4
C24 C0.1u16X/4
R37 1K1%/4
DIMMB1C
DDRIV-288P
12V3_NC_1
12V3_NC_145
VDDSPD
VPP-1
VPP-2
VPP-3
VPP-4
VPP-5
VTT-1
VTT-2
VREFCA
MEC3
MEC2
MEC1
VDD-0 … VDD-25
VCC3_SPD
VPP25
VTT_DDR
DIMM_CA_VREF_B
C386 C0.1u16X/4
C66 C2.2u6.3X/4
C244 C0.1u16X/4
C422 C0.1u16X/4
C410 C0.1u16X/4
C208 C22u6.3X/6
C289 C1u16X/6
C855 C0.1u16X/4
C838 C0.1u16X/4
C812 C0.1u16X/4
C819 C0.22u16X5/4
C887 C0.22u16X5/4
DIMMB1B
DDRIV-288P
VSS-0 … VSS-93
2018/5/13
The footprint of DIMMB1 is changed to DDRIV_D288_1_T_7A17 by the latest result from Ryan's comment
2018/5/13
The footprint of DIMMB1 is changed to DDRIV_D288_1_T_7A17 by the latest result from Ryan's comment
msi MICRO-STAR INT'L CO.,LTD.
Title DDR4-POWER/GND-2
Size Document Number MS-7C58 Rev 10
Date: Monday, November 11, 2019 Sheet 13 of 55

2019/4/26
B450 SKU is added by PM spec updated



AMD 300-Series Chipsets, "Promontory" Sub-Family Data Sheet 55553 Rev. 1.10 May 2018

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM3	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM3	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

Appendix G SATA Port to DEVSLP Mapping

SATA port	DEVSLP signal
SATA_TX/RXP/N[0]	DEVSLP0
SATA_TX/RXP/N[1]	DEVSLP1
SATA_TX/RXP/N[2]	DEVSLP2
SATA_TX/RXP/N[3]	DEVSLP3
SATAE_TX/RXP/N[0]	SATAE_CLKREQ0N
SATAE_TX/RXP/N[1]	DEVSLP4
SATAE_TX/RXP/N[2]	SATAE_CLKREQ1N
SATAE_TX/RXP/N[3]	DEVSLP5

Appendix F SATA Port to SATA LED Mapping

SATA port	SATA LED
SATA_TX/RXP/N[0]	SATALED0
SATA_TX/RXP/N[1]	SATALED1
SATA_TX/RXP/N[2]	SATALED2
SATA_TX/RXP/N[3]	SATALED3
SATAE_TX/RXP/N[0]	SATALED4
SATAE_TX/RXP/N[1]	SATALED5
SATAE_TX/RXP/N[2]	SATALED6
SATAE_TX/RXP/N[3]	SATALED7

2019/7/18 (1.1 only)
The name of net is changed from SATA_LED# to PM_SATA_LED# by SATA_ACT_L function fails with Matisse

msi	MICRO-STAR INT'L CO.,LTD.
Title	Promontory-PCIE/SATA/SATAE
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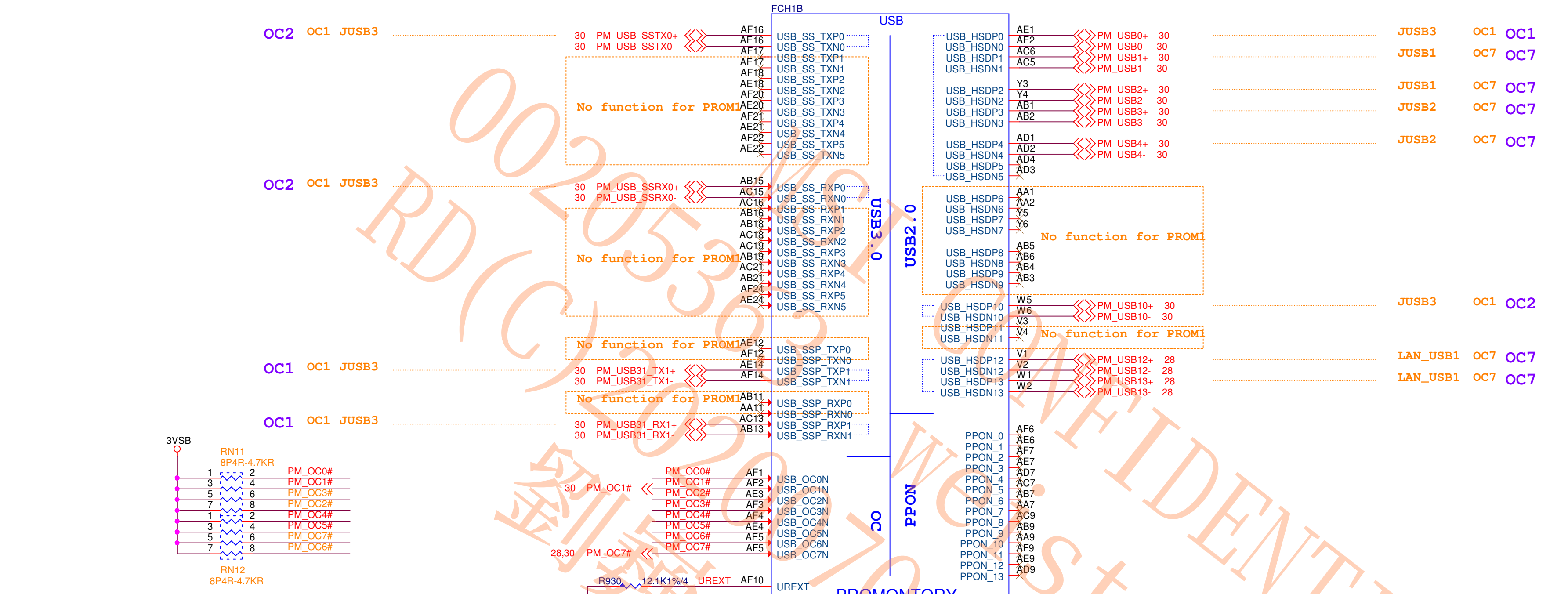
2019/4/30
B450 SKU is added by PM spec updated



2018/5/9
R635, R634, R633, R916 are deleted and then RN11 is added by cost reduction.
2018/5/9
R917, R632, R918, R631 are deleted and then RN12 is added by cost reduction.

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Appendix D USB Port to OC Pin Mapping

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N

USB3.0	USB2.0	USB_OC
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

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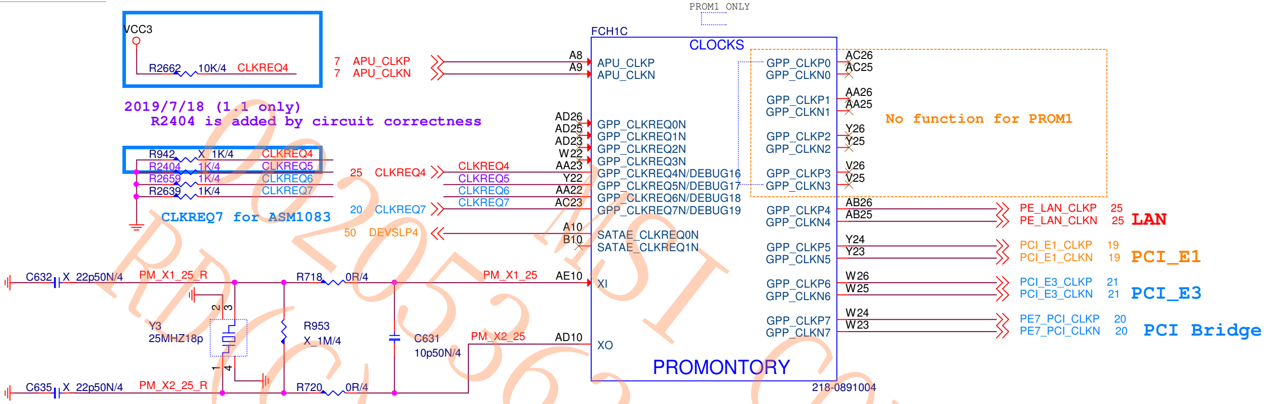
Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM3	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM3	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

Appendix E GPP Port to GPP_CLK*N Pin Mapping

GPP Clock	CLKREQ#
GPP_CLKP/N[0]	GPP_CLKREQ0N
GPP_CLKP/N[1]	GPP_CLKREQ1N
GPP_CLKP/N[2]	GPP_CLKREQ2N
GPP_CLKP/N[3]	GPP_CLKREQ3N
GPP_CLKP/N[4]	GPP_CLKREQ4N
GPP_CLKP/N[5]	GPP_CLKREQ5N
GPP_CLKP/N[6]	GPP_CLKREQ6N
GPP_CLKP/N[7]	GPP_CLKREQ7N



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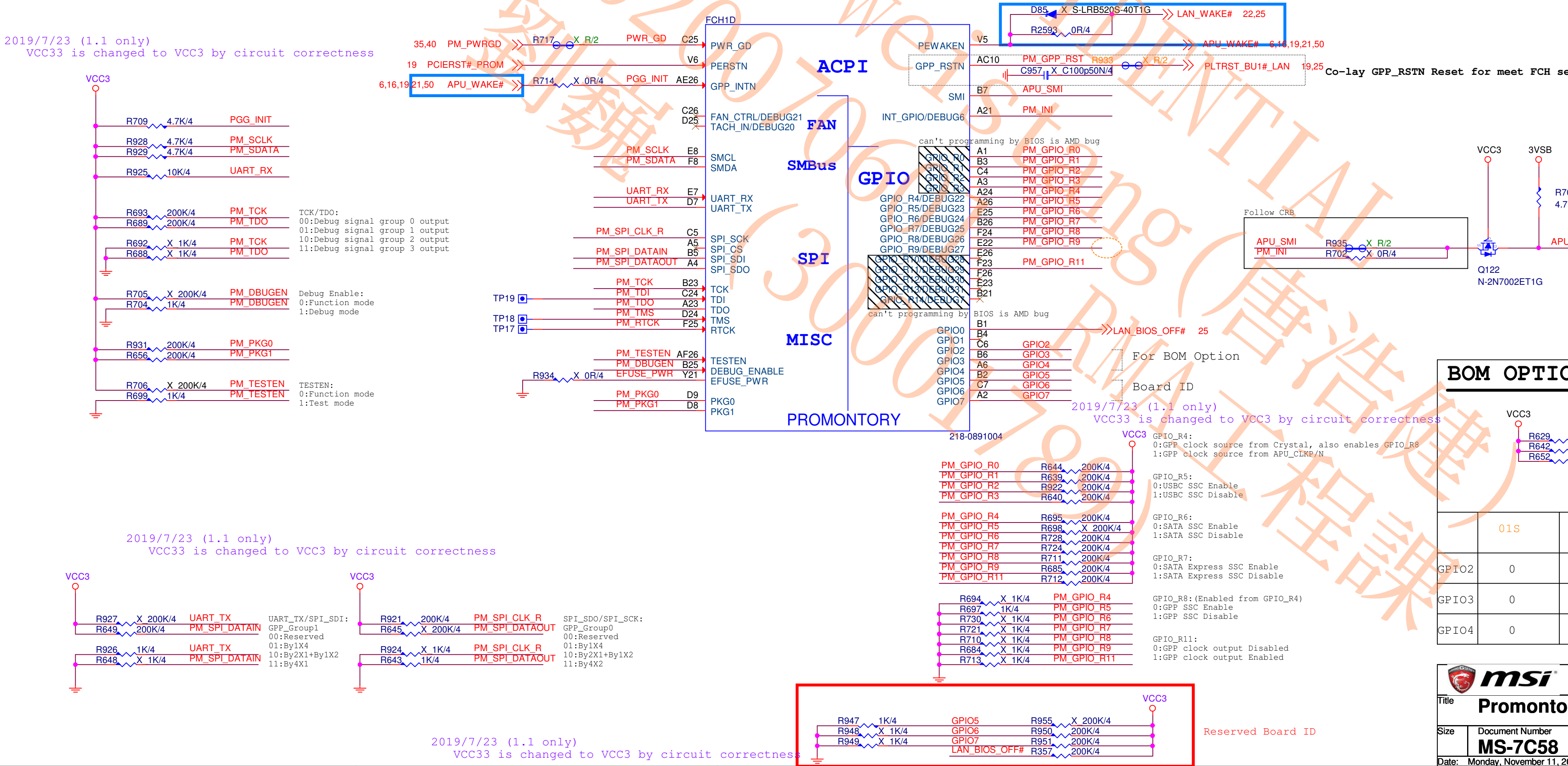
Appendix C Port Mapping for Different Bus Models

BUS Model	USB 3.1 Gen2 10 Gbps	USB 3.1 Gen1 5 Gbps	USB 2.0	USB Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM3	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM3	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7



2019/4/30
B450 SKU is added by PM spec updated
2019/5/8
R933 is changed to 0ohm to short copper by cost reduction.
2019/7/23 (1.1 only)
VCC33 is changed to VCC3 by circuit correctness
Co-lay GPP_RSTN Reset for meet FCH sequence. See 55553.
ACPI
FAN
SMBus
GPIO
SPI
MISC
PROMONTORY
218-0891004
can't programming by BIOS is AMD bug
TCK/TDO:
00:Debug signal group 0 output
01:Debug signal group 1 output
10:Debug signal group 2 output
11:Debug signal group 3 output
Debug Enable:
0:Function mode
1:Debug mode
TESTEN:
0:Function mode
1:Test mode
Follow CRB
For BOM Option
Board ID
GPIO_R4:
0:GPP clock source from Crystal, also enables GPIO_R8
1:GPP clock source from APU_CLKP/N
GPIO_R5:
0:USBC SSC Enable
1:USBC SSC Disable
GPIO_R6:
0:SATA SSC Enable
1:SATA SSC Disable
GPIO_R7:
0:SATA Express SSC Enable
1:SATA Express SSC Disable
GPIO_R8:(Enabled from GPIO_R4)
0:GPP SSC Enable
1:GPP SSC Disable
GPIO_R11:
0:GPP clock output Disabled
1:GPP clock output Enabled
UART_TX/SPI_SDI:
GPP_Group1
00:Reserved
01:By1X4
10:By2X1+By1X2
11:By4X1
SPI_SDO/SPI_SCK:
GPP_Group0
00:Reserved
01:By1X4
10:By2X1+By1X2
11:By4X2
Reserved Board ID

BOM OPTION

	01S	02S	03S	
GPIO2	0	1	0	1
GPIO3	0	0	1	1
GPIO4	0	0	0	0

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Title: Promontory-CLK/ACPI/GPIO

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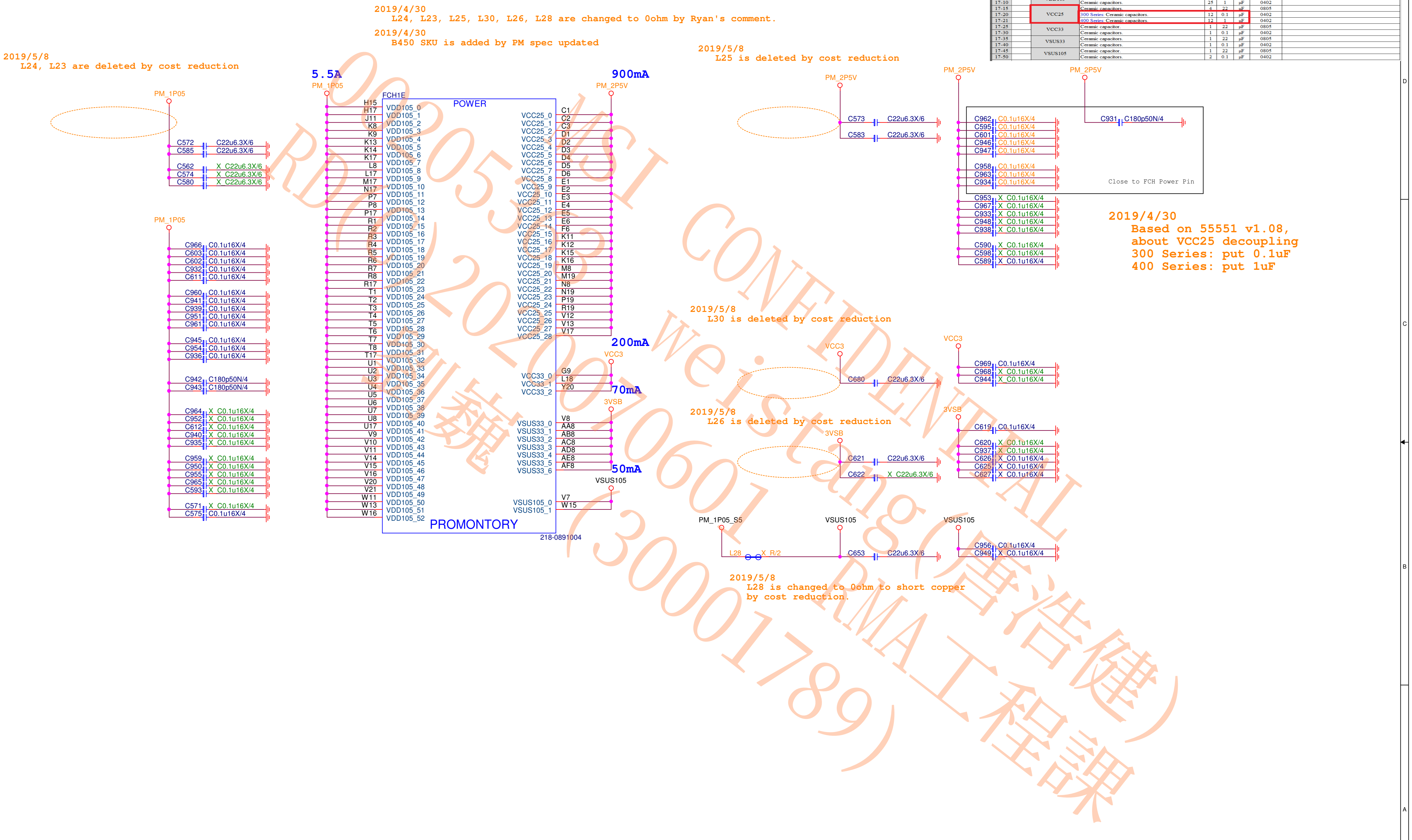
Chapter 17 Power and Decoupling Requirements

Note: Unless otherwise specified, recommended capacitor dielectric material is X5R, X6S, X7R, or X7S ceramic. Designers may replace a larger capacitor body size with a smaller body size. Transposed body sizes are acceptable and preferred.

No.	Y/N/V	Group	Explanation	Qty	Value	Units	Size/Tol	Comments
17-5		VDD105	Ceramic capacitors.	6	22	µF	0805	
17-10			Ceramic capacitors.	25	1	µF	0402	
17-15		VCC25	Ceramic capacitors.	4	22	µF	0805	
17-20			300 Series: Ceramic capacitors.	12	0.1	µF	0402	
17-21			400 Series: Ceramic capacitors.	12	1	µF	0402	
17-25		VCC33	Ceramic capacitor.	1	22	µF	0805	
17-30			Ceramic capacitors.	1	0.1	µF	0402	
17-35		VSUS33	Ceramic capacitors.	1	22	µF	0805	
17-40			Ceramic capacitors.	1	0.1	µF	0402	
17-45		VSUS105	Ceramic capacitor.	1	22	µF	0805	
17-50			Ceramic capacitors.	2	0.1	µF	0402	



2019/4/30
L24, L23, L25, L30, L26, L28 are changed to 0ohm by Ryan's comment.
2019/4/30
B450 SKU is added by PM spec updated
2019/5/8
L24, L23 are deleted by cost reduction
2019/5/8
L25 is deleted by cost reduction
5.5A
900mA
PM_1P05
PM_2P5V
FCH1E
POWER
PROMONTORY
218-0891004
200mA
VCC3
70mA
3VSB
50mA
VSUS105
Close to FCH Power Pin
2019/4/30
Based on 55551 v1.08,
about VCC25 decoupling
300 Series: put 0.1uF
400 Series: put 1uF
2019/5/8
L30 is deleted by cost reduction
2019/5/8
L26 is deleted by cost reduction
PM_1P05_S5
2019/5/8
L28 is changed to 0ohm to short copper
by cost reduction.

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Title: Promontory-Power

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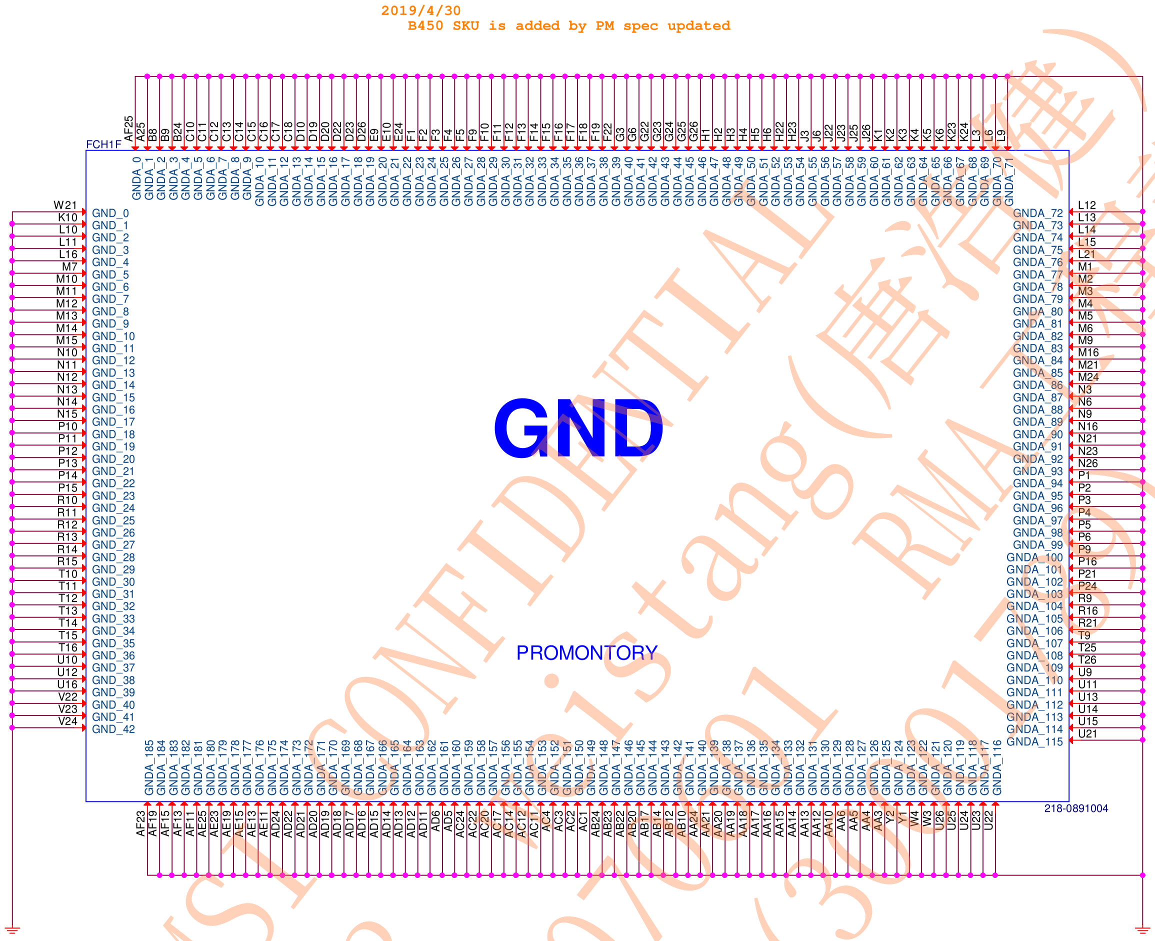

MICRO-STAR INT'L CO.,LTD.
Title: Promontory-GND
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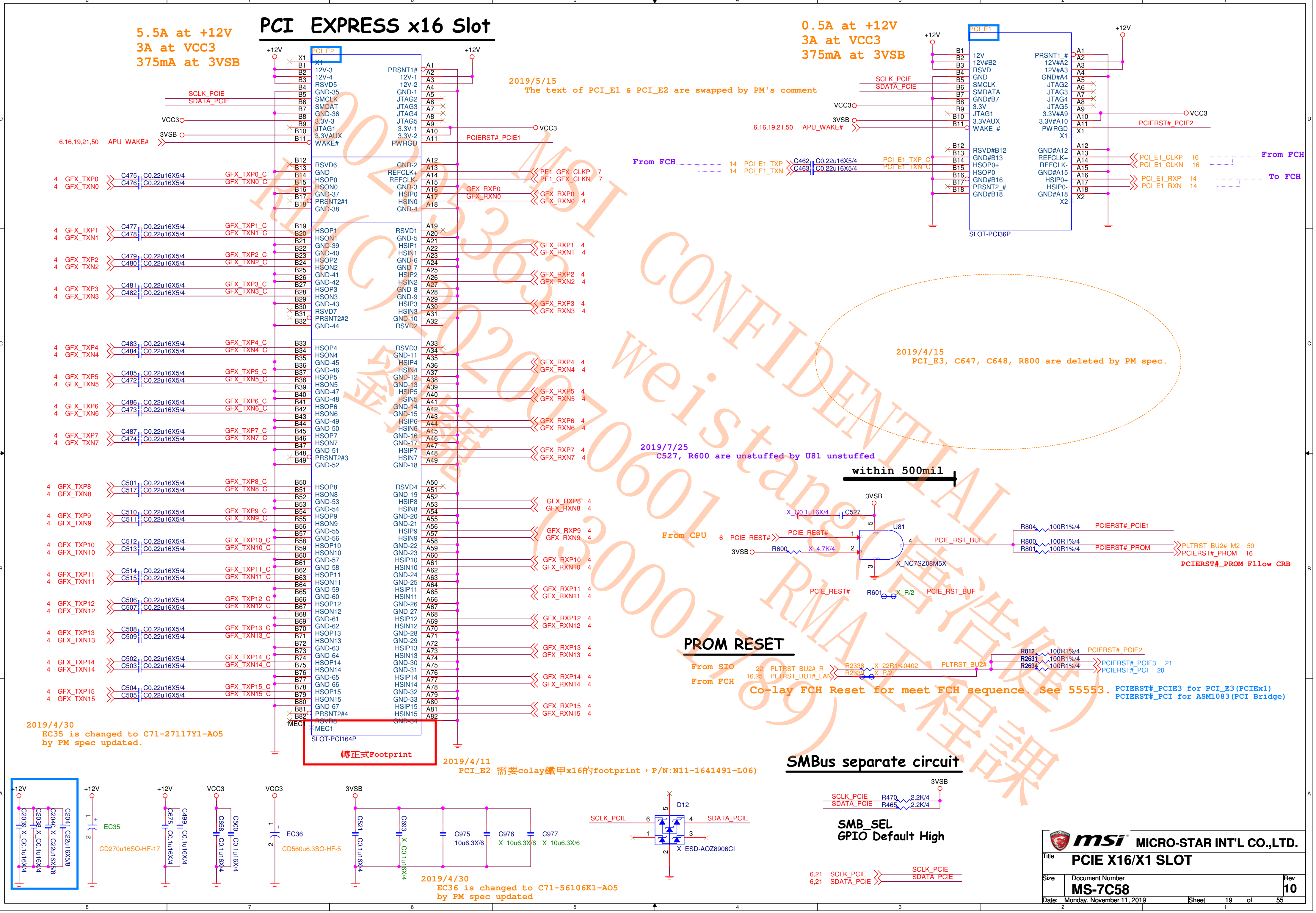

PCI EXPRESS x16 Slot
5.5A at +12V
3A at VCC3
375mA at 3VSB
0.5A at +12V
3A at VCC3
375mA at 3VSB
PCI_E2
SLOT-PCI164P
PCI_E1
SLOT-PCI36P
2019/5/15
The text of PCI_E1 & PCI_E2 are swapped by PM's comment
From FCH
To FCH
2019/4/15
PCI_E3, C647, C648, R800 are deleted by PM spec.
2019/7/25
C527, R600 are unstuffed by U81 unstuffed
within 500mil
From CPU
U81
X_NC7SZ08M5X
PCIERST#_PROM Fllow CRB
PROM RESET
From SIO
From FCH
Co-lay FCH Reset for meet FCH sequence. See 55553.
PCIERST#_PCIE3 for PCI_E3(PCIEx1)
PCIERST#_PCI for ASM1083(PCI Bridge)
2019/4/30
EC35 is changed to C71-27117Y1-A05
by PM spec updated.
轉正式Footprint
2019/4/11
PCI_E2 需要colay鐵甲x16的footprint，P/N:N11-1641491-L06)
SMBus separate circuit
SMB_SEL
GPIO Default High
D12
X_ESD-AOZ8906CI
2019/4/30
EC36 is changed to C71-56106K1-A05
by PM spec updated
EC35
CD270u16SO-HF-17
EC36
CD560u6.3SO-HF-5

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Title: PCIE X16/X1 SLOT

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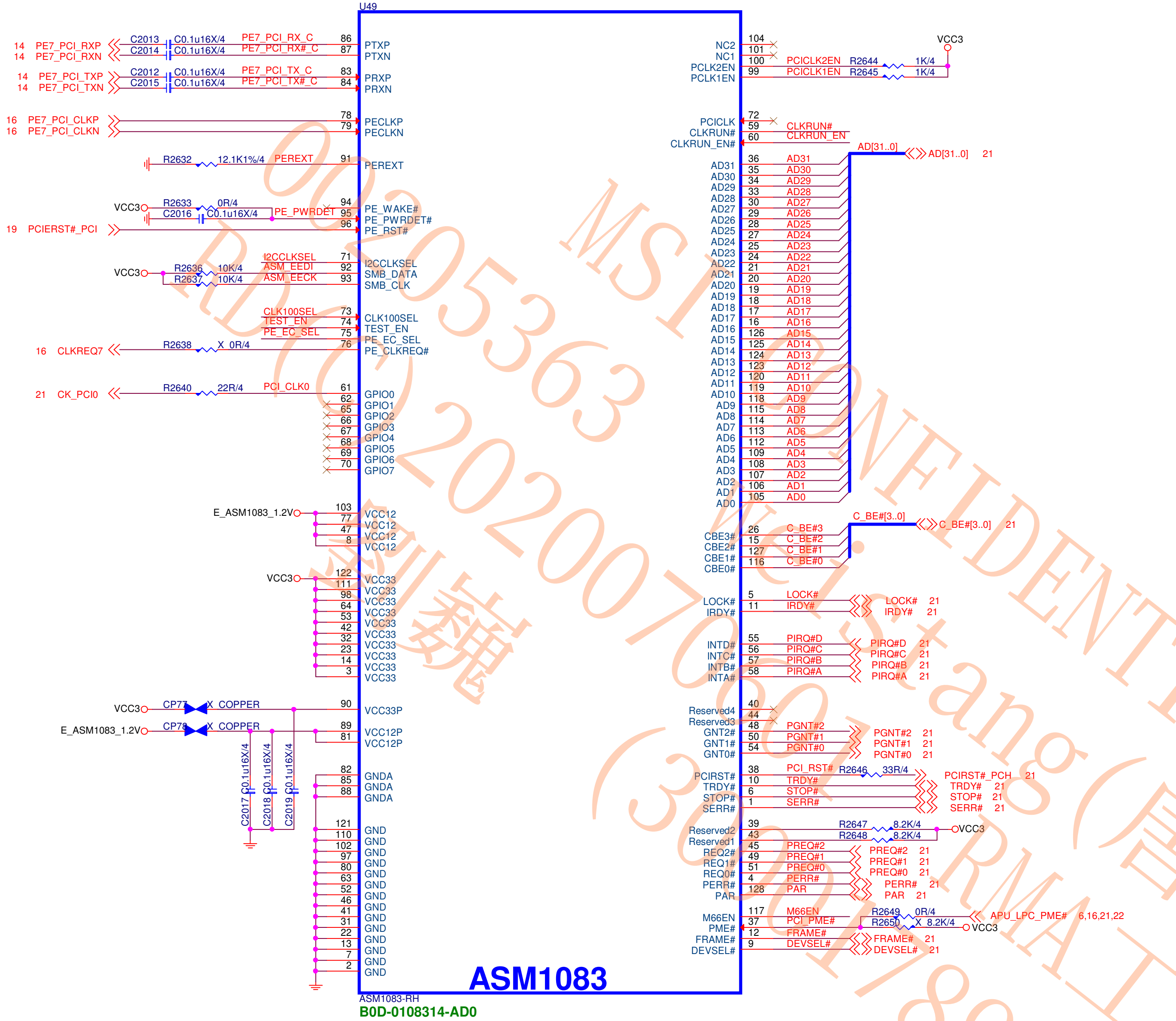
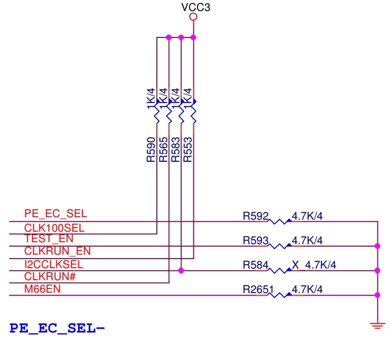

U49
ASM1083
ASM1083-RH
B0D-0108314-AD0
PE7_PCI_RXP
PE7_PCI_RXN
PE7_PCI_TXP
PE7_PCI_TXN
PE7_PCI_CLKP
PE7_PCI_CLKN
PCIERST#_PCI
CLKREQ7
CK_PCI0
E_ASM1083_1.2V
VCC3
PTXP
PTXN
PRXP
PRXN
PECLKP
PECLKN
PEREXT
PE_WAKE#
PE_PWRDET#
PE_RST#
I2CCLKSEL
SMB_DATA
SMB_CLK
CLK100SEL
TEST_EN
PE_EC_SEL
PE_CLKREQ#
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
VCC12
VCC33
VCC33P
VCC12P
GNDA
GND
NC2
NC1
PCLK2EN
PCLK1EN
PCICLK
CLKRUN#
CLKRUN_EN#
AD[31..0]
C_BE#[3..0]
CBE3#
CBE2#
CBE1#
CBE0#
LOCK#
IRDY#
INTD#
INTC#
INTB#
INTA#
Reserved4
Reserved3
GNT2#
GNT1#
GNT0#
PCIRST#
TRDY#
STOP#
SERR#
Reserved2
Reserved1
REQ2#
REQ1#
REQ0#
PERR#
PAR
M66EN
PME#
FRAME#
DEVSEL#
PCIRST#_PCH
APU_LPC_PME#

H/W Strapping



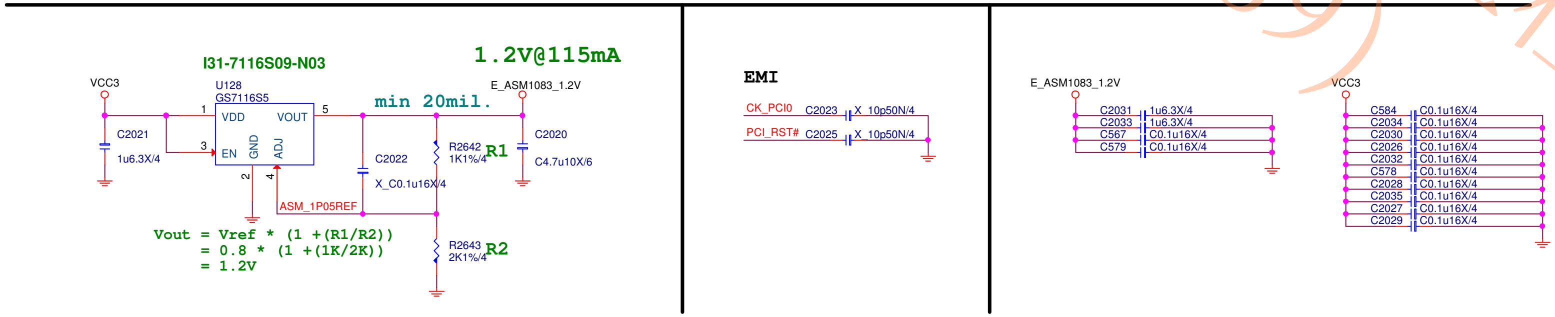
PE_EC_SEL-
"H" for Express Card mode
"L" for PCIe Riser Card mode

CLK100SEL-
"H" for PECLK input only
"L" for PECLK & PCICLK input

TEST_EN-
"H" for Test Mode Enable
"L" for Test Mode Disable

CLKRUN_EN-
"H" for CLKRUN Mode Disable
"L" for CLKRUN Mode Enable

I2CCLKSEL-
"H" is 135KHz I2CCLK
"L" is 67.5KHz I2CCLK


I31-7116S09-N03
1.2V@115mA
min 20mil.
U128
GS7116S5
VDD
VOUT
EN
GND
ADJ
C2021 1u6.3X/4
C2022 X_C0.1u16X/4
R2642 1K1%/4 R1
R2643 2K1%/4 R2
C2020 C4.7u10X/6
ASM_1P05REF
Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(1K/2K))
= 1.2V
EMI
CK_PCI0 C2023 X_10p50N/4
PCI_RST# C2025 X_10p50N/4
E_ASM1083_1.2V
VCC3

msi	MICRO-STAR INT'L CO.,LTD.
Title	ASM1083 PCI Bri.
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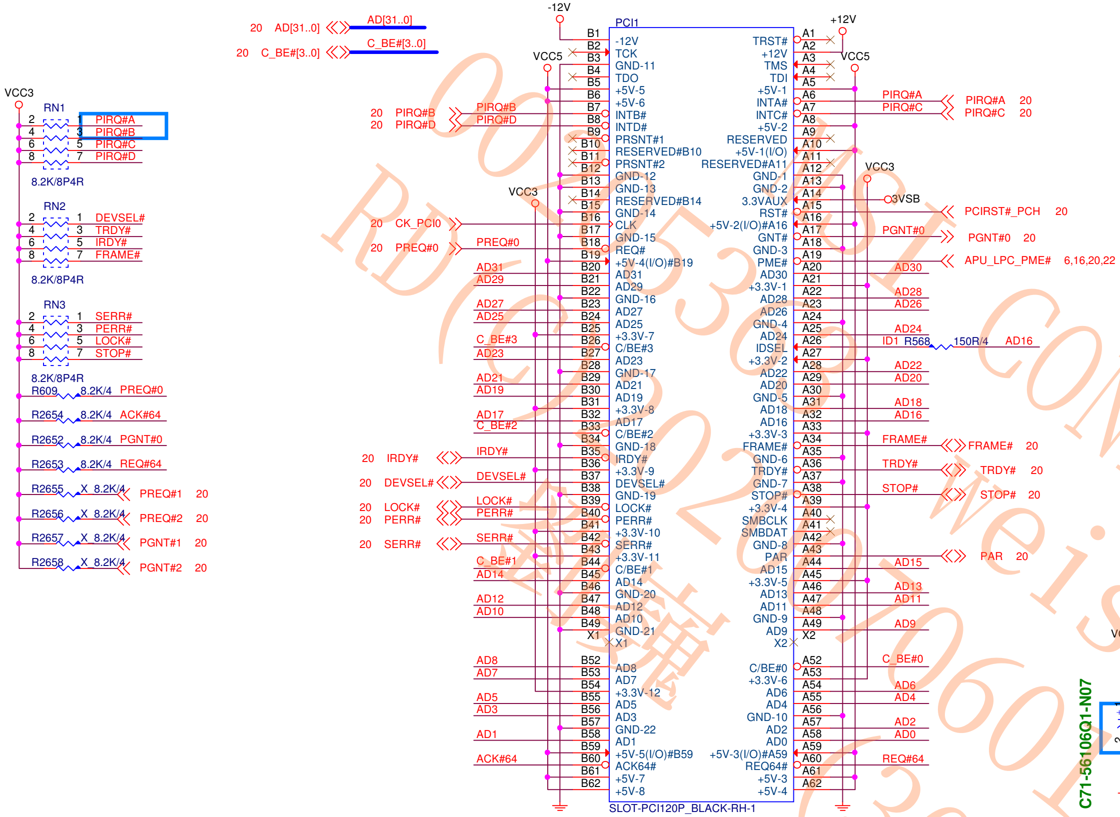
PCI Slot

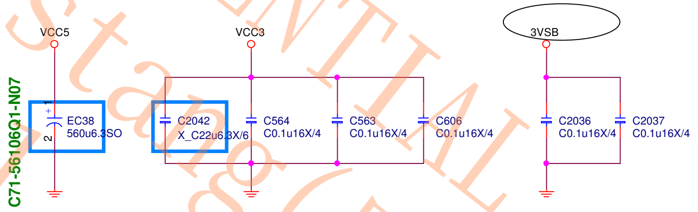


PCI1
SLOT-PCI120P_BLACK-RH-1
-12V
+12V
VCC5
VCC3
3VSB
RN1
RN2
RN3
8.2K/8P4R
PIRQ#A
PIRQ#B
PIRQ#C
PIRQ#D
DEVSEL#
TRDY#
IRDY#
FRAME#
SERR#
PERR#
LOCK#
STOP#
R609 8.2K/4 PREQ#0
R2654 8.2K/4 ACK#64
R2652 8.2K/4 PGNT#0
R2653 8.2K/4 REQ#64
R2655 X_8.2K/4 PREQ#1 20
R2656 X_8.2K/4 PREQ#2 20
R2657 X_8.2K/4 PGNT#1 20
R2658 X_8.2K/4 PGNT#2 20
20 AD[31..0]
20 C_BE#[3..0]
20 CK_PCI0
20 PREQ#0
20 IRDY#
20 DEVSEL#
20 LOCK#
20 PERR#
20 SERR#
PIRQ#A 20
PIRQ#C 20
PCIRST#_PCH 20
PGNT#0 20
APU_LPC_PME# 6,16,20,22
R568 150R/4 AD16
FRAME# 20
TRDY# 20
STOP# 20
PAR 20

N11-1200541-C67

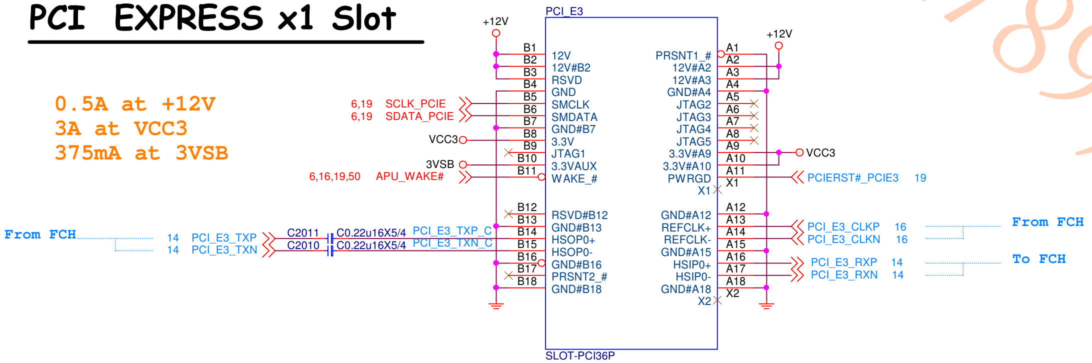
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI Slot		
+12V		- 0.5 A
+VCC3		- 7.6A
+VCC5		- 5A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA



PCI EXPRESS x1 Slot

0.5A at +12V
3A at VCC3
375mA at 3VSB



PCI_E3
SLOT-PCI36P
+12V
6,19 SCLK_PCIE
6,19 SDATA_PCIE
VCC3
3VSB
6,16,19,50 APU_WAKE#
From FCH
14 PCI_E3_TXP
14 PCI_E3_TXN
C2011 C0.22u16X5/4
C2010 C0.22u16X5/4
PCI_E3_TXP_C
PCI_E3_TXN_C
PCIERST#_PCIE3 19
PCI_E3_CLKP 16
PCI_E3_CLKN 16
PCI_E3_RXP 14
PCI_E3_RXN 14
From FCH
To FCH

msi MICRO-STAR INT'L CO.,LTD.

Title	PCI Slot/PCIE X1 Slot
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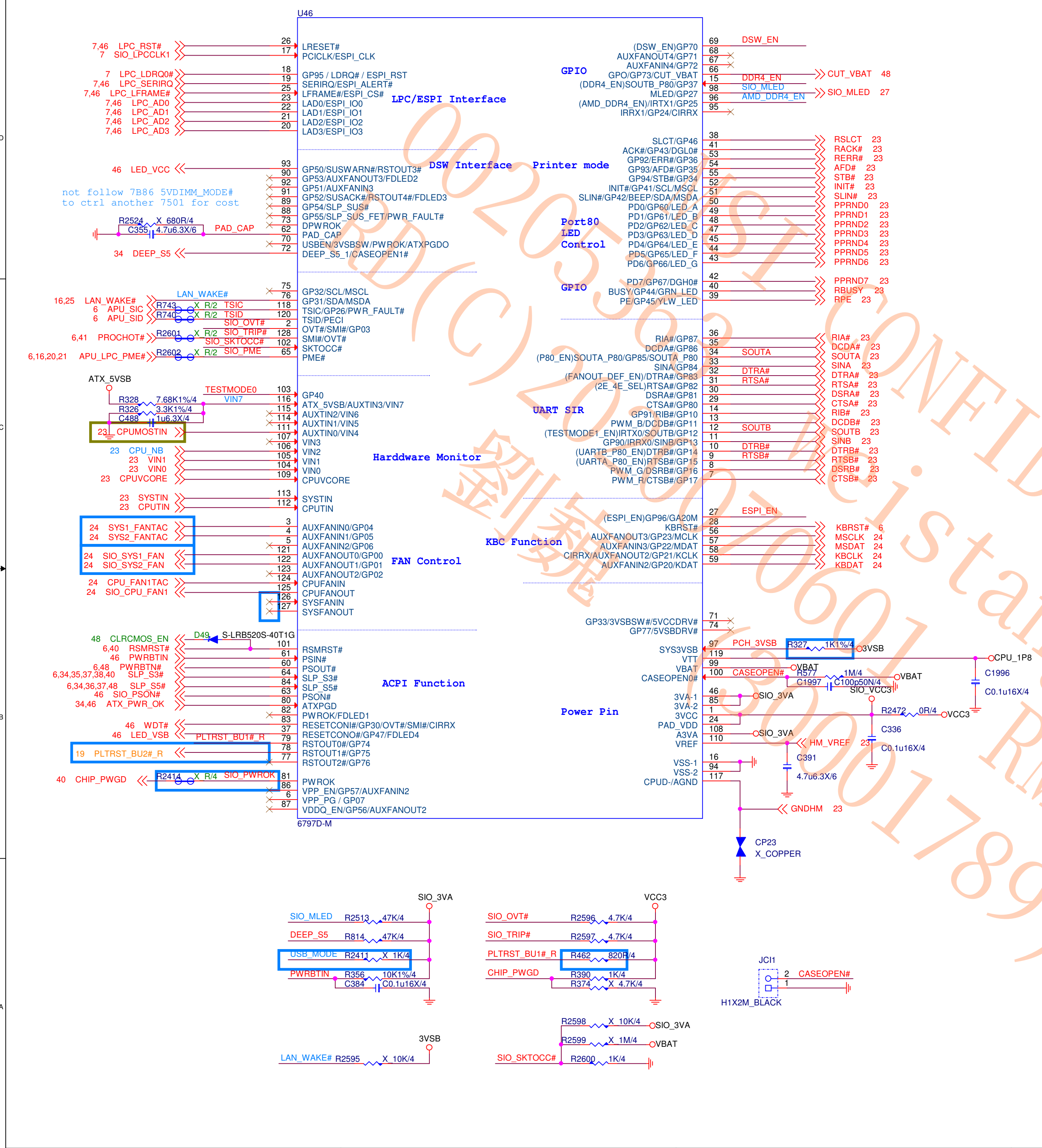
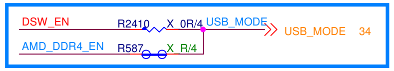
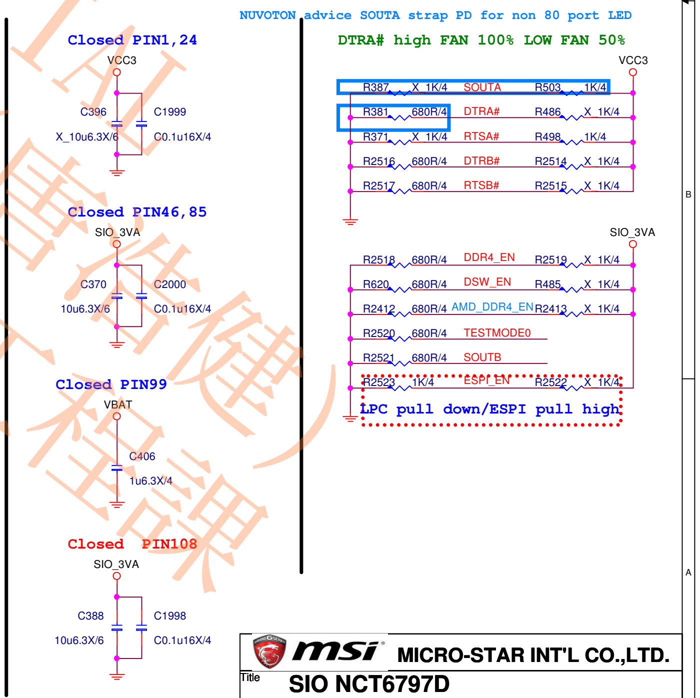




POWER ON STRAPPING PIN FOR NCT6797/6795

PIN	6797/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TESTMODE1_EN	SOUTB	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	DDR4_EN	DDR4_EN	Disable	Enable	
27	ESPI_EN	ESPI_EN	LPC	ESPI	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	FANOUT_DEF_EN	DTRA#	default 50%	default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	6795 TESTMODE_EN 6797 GP40	TESTMODE0	6795 DISABLE TESTMODE	6795 ENABLE TESTMODE	INTERNAL RSMRST

Note: If PIN34 strapping low,BIOS must programming LPT or GPIO



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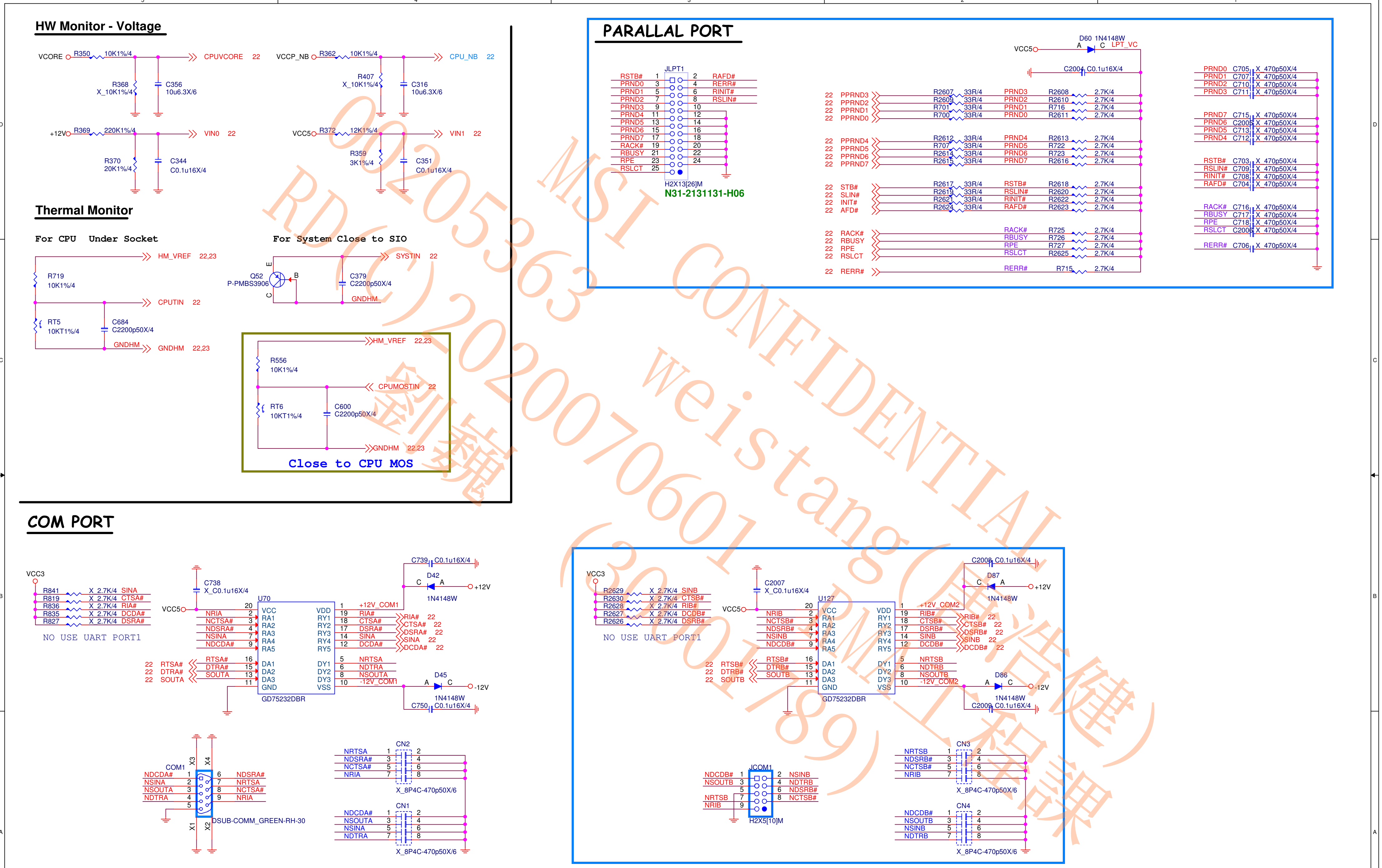

MICRO-STAR INT'L CO.,LTD.

Title: SIO COM/LPT/HWM

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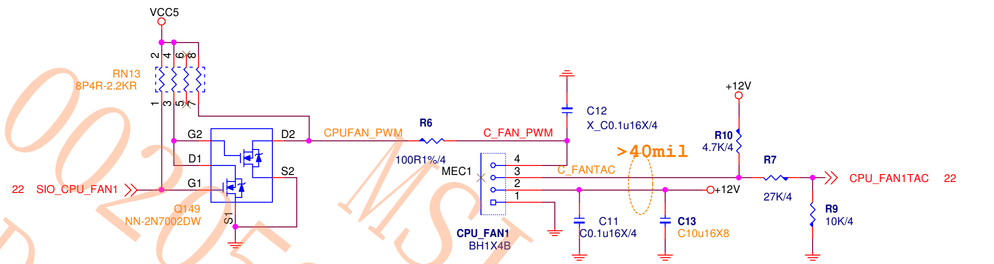
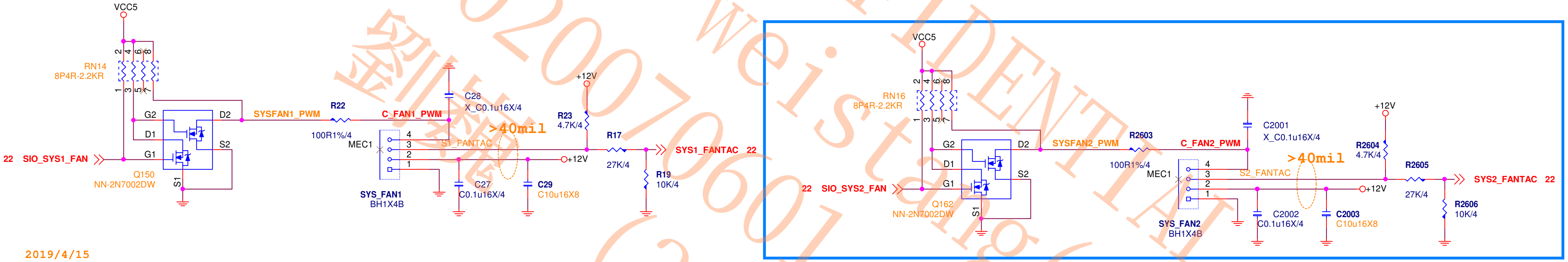
FAN(direct PWM mode)



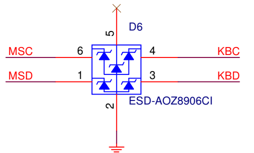
2019/4/15
U2, C5, R8, C9, C23 are deleted; R1517, R1518, Q149 are added; R4 is changed to 2.2Kohm by PM spec.
2019/4/15
C13 is changed from 22uF to 10uF; D5, C10, C6 are deleted by the latest module circuit
2018/5/9
R1517, R1518, R4 are deleted and then RN13 is added by cost reduction.


VCC5
RN14
8P4R-2.2KR
22 SIO_SYS1_FAN
Q150
NN-2N7002DW
SYSFAN1_PWM
R22
100R1%/4
C_FAN1_PWM
MEC1
S1_FANTAC
SYS_FAN1
BH1X4B
C28
X_C0.1u16X/4
>40mil
+12V
R23
4.7K/4
R17
27K/4
SYS1_FANTAC 22
R19
10K/4
C27
C0.1u16X/4
C29
C10u16X8
VCC5
RN16
8P4R-2.2KR
22 SIO_SYS2_FAN
Q162
NN-2N7002DW
SYSFAN2_PWM
R2603
100R1%/4
C_FAN2_PWM
MEC1
S2_FANTAC
SYS_FAN2
BH1X4B
C2001
X_C0.1u16X/4
>40mil
+12V
R2604
4.7K/4
R2605
27K/4
SYS2_FANTAC 22
R2606
10K/4
C2002
C0.1u16X/4
C2003
C10u16X8

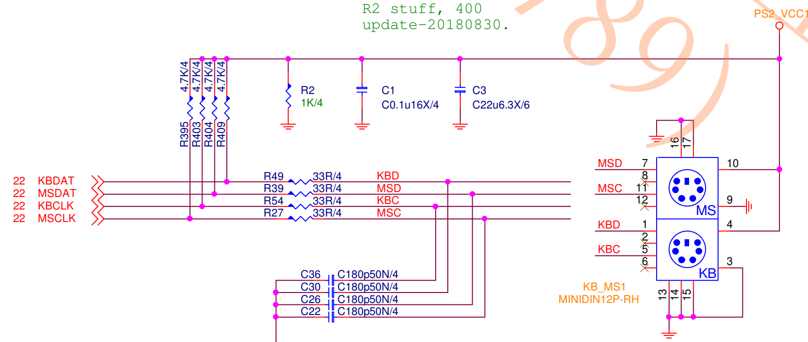
2019/4/15
U3, C14, R21, C20, C32 are deleted; Q150, R1520, R1519 are added; R20 is changed to 2.2Kohm by PM spec
2019/4/15
C29 is changed from 22uF to 10uF; D8, C21, C15 are deleted by the latest module circuit
2018/5/9
R1520, R1519, R20 are deleted and then RN14 is added by cost reduction.

PS2

TVS P/N:
D0G-45B0510-I14



20181026:
R2 stuff, 400
update-20180830.

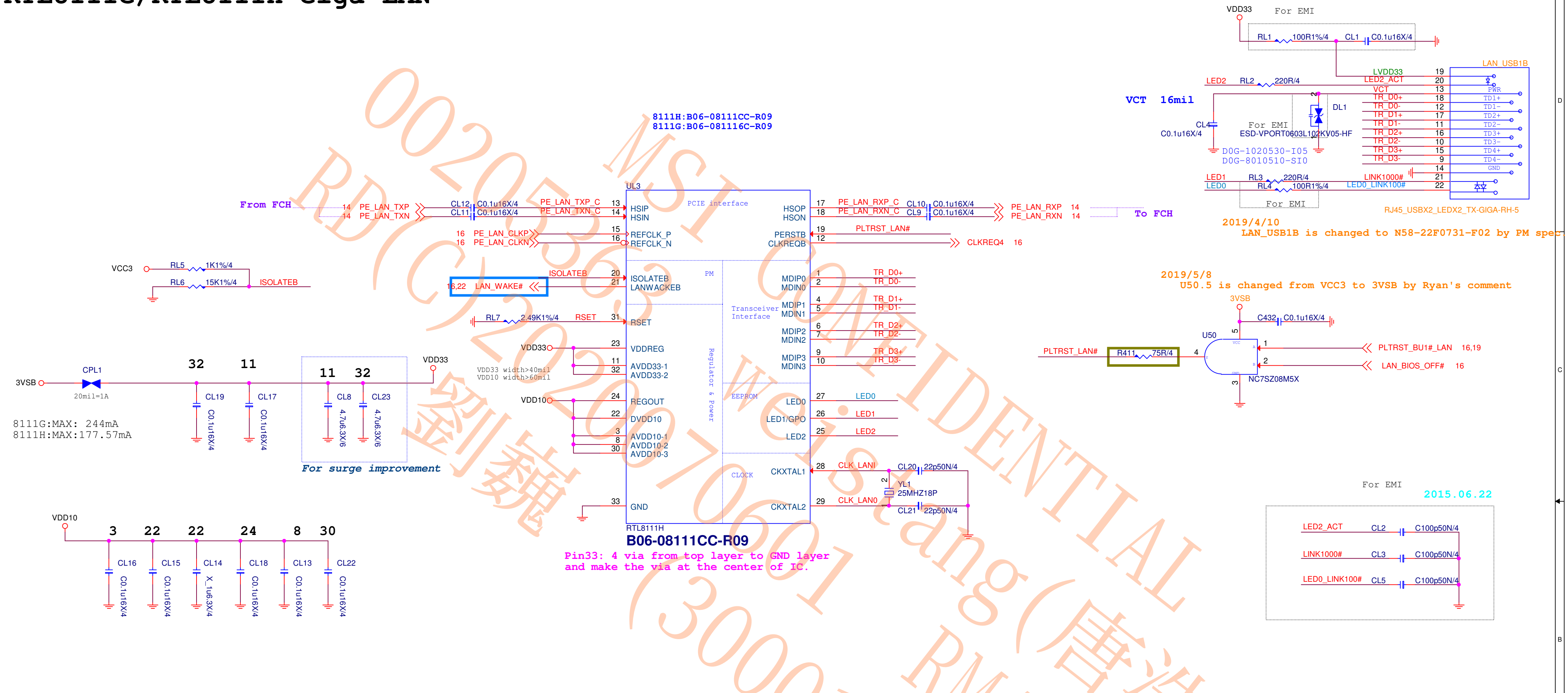


layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch

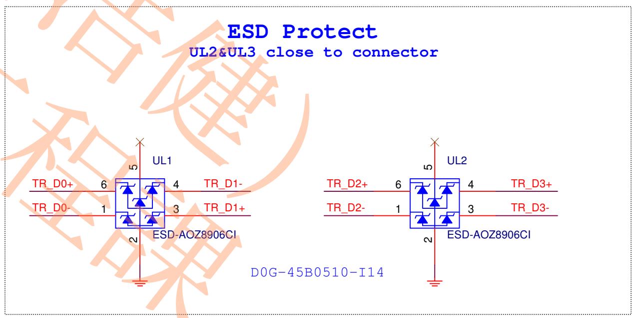
2019/4/10
About PS2 circuit move from the page 25

2019/4/10
KB_MS1 is changed to N56-12F0151-H06 by PM spec.

RTL8111G/RTL8111H Giga LAN



LAN Connector
VDD33
For EMI
RL1 100R1%/4
CL1 C0.1u16X/4
LAN_USB1B
LVDD33
LED2_ACT
LED2 RL2 220R/4
VCT
VCT 16mil
TR_D0+
TR_D0-
TR_D1+
TR_D1-
TR_D2+
TR_D2-
TR_D3+
TR_D3-
DL1
CL4 C0.1u16X/4
ESD-VPORT0603L102KV05-HF
D0G-1020530-I05
D0G-8010510-SI0
LED1 RL3 220R/4 LINK1000#
LED0 RL4 100R1%/4 LED0_LINK100#
RJ45_USBX2_LEDX2_TX-GIGA-RH-5
2019/4/10
LAN_USB1B is changed to N58-22F0731-F02 by PM spec
8111H:B06-08111CC-R09
8111G:B06-081116C-R09
From FCH
PE_LAN_TXP
PE_LAN_TXN
CL12 C0.1u16X/4 PE_LAN_TXP_C
CL11 C0.1u16X/4 PE_LAN_TXN_C
PE_LAN_CLKP
PE_LAN_CLKN
UL3
PCIE interface
HSIP
HSIN
REFCLK_P
REFCLK_N
HSOP
HSON
PERSTB
CLKREQB
PE_LAN_RXP_C CL10 C0.1u16X/4 PE_LAN_RXP
PE_LAN_RXN_C CL9 C0.1u16X/4 PE_LAN_RXN
To FCH
PLTRST_LAN#
CLKREQ4
VCC3
RL5 1K1%/4
RL6 15K1%/4
ISOLATEB
LAN_WAKE#
ISOLATEB
LANWAKEB
PM
RL7 2.49K1%/4 RSET
RSET
Transceiver Interface
MDIP0
MDIN0
MDIP1
MDIN1
MDIP2
MDIN2
MDIP3
MDIN3
VDD33
VDDREG
AVDD33-1
AVDD33-2
VDD33 width>40mil
VDD10 width>60mil
Regulator & Power
VDD10
REGOUT
DVDD10
AVDD10-1
AVDD10-2
AVDD10-3
EEPROM
LED0
LED1/GPO
LED2
CLOCK
CKXTAL1
CKXTAL2
CLK_LANI
CLK_LANO
CL20 22p50N/4
CL21 22p50N/4
YL1 25MHZ18P
GND
RTL8111H
B06-08111CC-R09
Pin33: 4 via from top layer to GND layer
and make the via at the center of IC.
3VSB
CPL1
20mil=1A
8111G:MAX: 244mA
8111H:MAX:177.57mA
CL19 C0.1u16X/4
CL17 C0.1u16X/4
CL8 4.7u6.3X/6
CL23 4.7u6.3X/6
For surge improvement
2019/5/8
U50.5 is changed from VCC3 to 3VSB by Ryan's comment
3VSB
C432 C0.1u16X/4
U50
PLTRST_LAN# R411 75R/4
PLTRST_BU1#_LAN
LAN_BIOS_OFF#
NC7SZ08M5X
For EMI
2015.06.22
LED2_ACT CL2 C100p50N/4
LINK1000# CL3 C100p50N/4
LED0_LINK100# CL5 C100p50N/4
VDD10
CL16 C0.1u16X/4
CL15 C0.1u16X/4
CL14 X_1u6.3X/4
CL18 C0.1u16X/4
CL13 C0.1u16X/4
CL22 C0.1u16X/4

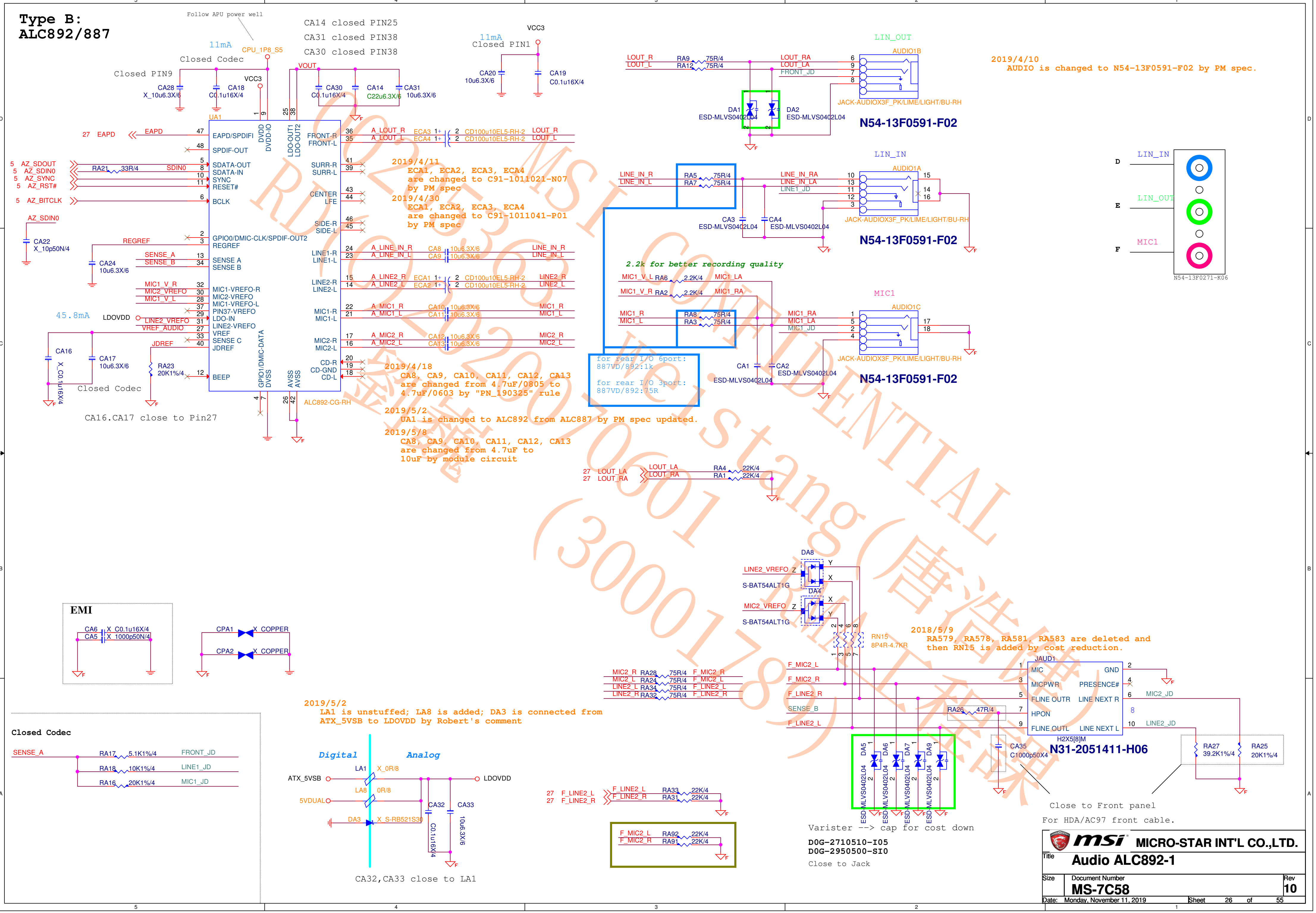


8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15



Type B:
ALC892/887
Follow APU power well
CA14 closed PIN25
CA31 closed PIN38
CA30 closed PIN38
11mA
Closed Codec
Closed PIN9
11mA
Closed PIN1
VCC3
LIN_OUT
AUDIO1B
JACK-AUDIOX3F_PK/LIME/LIGHT/BU-RH
N54-13F0591-F02
2019/4/10
AUDIO is changed to N54-13F0591-F02 by PM spec.
EAPD/SPDIFI
SPDIF-OUT
SDATA-OUT
SDATA-IN
SYNC
RESET#
BCLK
GPIO0/DMIC-CLK/SPDIF-OUT2
REGREF
SENSE A
SENSE B
MIC1-VREFO-R
MIC2-VREFO
MIC1-VREFO-L
PIN37-VREFO
LDO-IN
LINE2-VREFO
VREF
SENSE C
JDREF
BEEP
FRONT-R
FRONT-L
SURR-R
SURR-L
CENTER
LFE
SIDE-R
SIDE-L
LINE1-R
LINE1-L
LINE2-R
LINE2-L
MIC1-R
MIC1-L
MIC2-R
MIC2-L
CD-R
CD-GND
CD-L
ALC892-CG-RH
2019/4/11
ECA1, ECA2, ECA3, ECA4
are changed to C91-1011021-N07
by PM spec
2019/4/30
ECA1, ECA2, ECA3, ECA4
are changed to C91-1011041-P01
by PM spec
45.8mA
LDOVDD
Closed Codec
CA16.CA17 close to Pin27
2019/4/18
CA8, CA9, CA10, CA11, CA12, CA13
are changed from 4.7uF/0805 to
4.7uF/0603 by "PN_190325" rule
2019/5/2
UA1 is changed to ALC892 from ALC887 by PM spec updated.
2019/5/8
CA8, CA9, CA10, CA11, CA12, CA13
are changed from 4.7uF to
10uF by module circuit
LIN_IN
AUDIO1A
N54-13F0591-F02
2.2k for better recording quality
MIC1
AUDIO1C
N54-13F0591-F02
for rear I/O 6port:
887VD/892:1k
for rear I/O 3port:
887VD/892:75R
N54-13F0271-K06
EMI
2018/5/9
RA579, RA578, RA581, RA583 are deleted and
then RN15 is added by cost reduction.
JAUD1
MIC
GND
MICPWR
PRESENCE#
FLINE OUTR
LINE NEXT R
HPON
FLINE OUTL
LINE NEXT L
H2X5[8]M
N31-2051411-H06
Close to Front panel
For HDA/AC97 front cable.
2019/5/2
LA1 is unstuffed; LA8 is added; DA3 is connected from
ATX_5VSB to LDOVDD by Robert's comment
Digital
Analog
ATX_5VSB
5VDUAL
LDOVDD
CA32,CA33 close to LA1
Varister --> cap for cost down
D0G-2710510-I05
D0G-2950500-SI0
Close to Jack
Closed Codec
SENSE_A
FRONT_JD
LINE1_JD
MIC1_JD
MICRO-STAR INT'L CO.,LTD.
Title
Audio ALC892-1
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Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)

2019/5/8
RA13 pull up to VCC3 by module circuit

2019/5/23
RA15 is changed from 1Kohm to 0ohm by module circuit

Digital

Analog

2019/7/25
RA14, RA13, QA2, QA3, RA15, CA7, RA19, RA20, QA7, CA15, RA10, RA11, QA1, RA30, RA29, QA6 are unstuffed by PM request(2019/7/24)

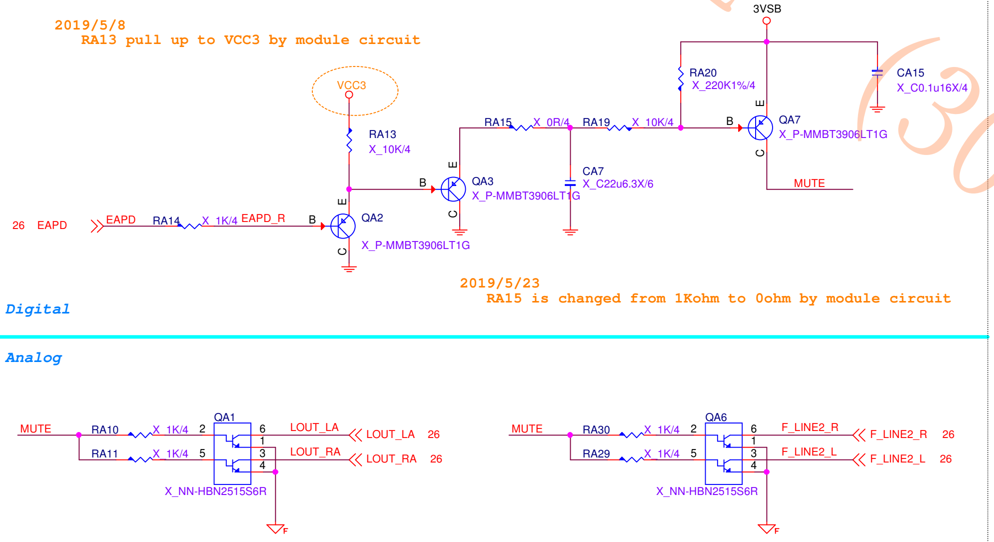
20181203
Remove Audio LED,
RA73、RA71、RA72、RA74、RA75、RA76、LEDA4、LEDA2、LEDA3、LEDA6、LEDA5、LEDA7、QA4、QA5 unstuff.

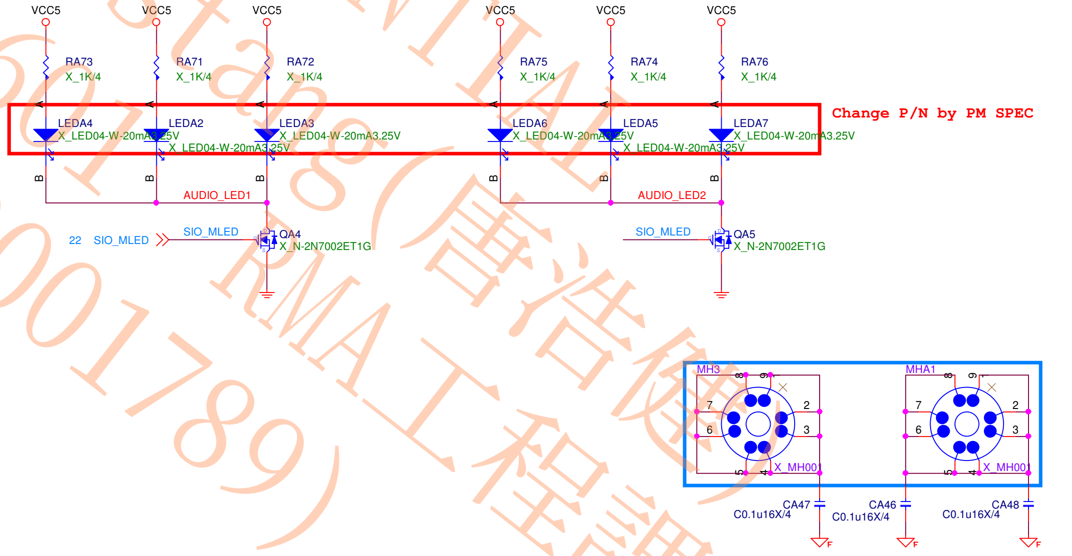
使用測光LED

Change P/N by PM SPEC

2019/4/26
The pin1 of MH3, MHA1 are changed to GND by CND rule

2019/7/19 (1.1 only)
The pootprint of MH3, MHA1 are changed from HOLES_4S to Holes_4s_CND by Eric's comment(2019/7/17)


3VSB
VCC3
RA13
X_10K/4
RA20
X_220K1%/4
CA15
X_C0.1u16X/4
RA15
X_0R/4
RA19
X_10K/4
QA7
X_P-MMBT3906LT1G
QA3
X_P-MMBT3906LT1G
CA7
X_C22u6.3X/6
MUTE
26 EAPD
EAPD
RA14
X_1K/4
EAPD_R
QA2
X_P-MMBT3906LT1G
MUTE
RA10
X_1K/4
RA11
X_1K/4
QA1
LOUT_LA
LOUT_RA
LOUT_LA 26
LOUT_RA 26
X_NN-HBN2515S6R
MUTE
RA30
X_1K/4
RA29
X_1K/4
QA6
F_LINE2_R
F_LINE2_L
F_LINE2_R 26
F_LINE2_L 26
X_NN-HBN2515S6R


VCC5
RA73
X_1K/4
RA71
X_1K/4
RA72
X_1K/4
RA75
X_1K/4
RA74
X_1K/4
RA76
X_1K/4
LEDA4
X_LED04-W-20mA3.25V
LEDA2
X_LED04-W-20mA3.25V
LEDA3
X_LED04-W-20mA3.25V
LEDA6
X_LED04-W-20mA3.25V
LEDA5
X_LED04-W-20mA3.25V
LEDA7
X_LED04-W-20mA3.25V
AUDIO_LED1
AUDIO_LED2
22 SIO_MLED
SIO_MLED
QA4
X_N-2N7002ET1G
QA5
X_N-2N7002ET1G
MH3
X_MH001
MHA1
X_MH001
CA47
C0.1u16X/4
CA46
C0.1u16X/4
CA48
C0.1u16X/4

msi	MICRO-STAR INT'L CO.,LTD.
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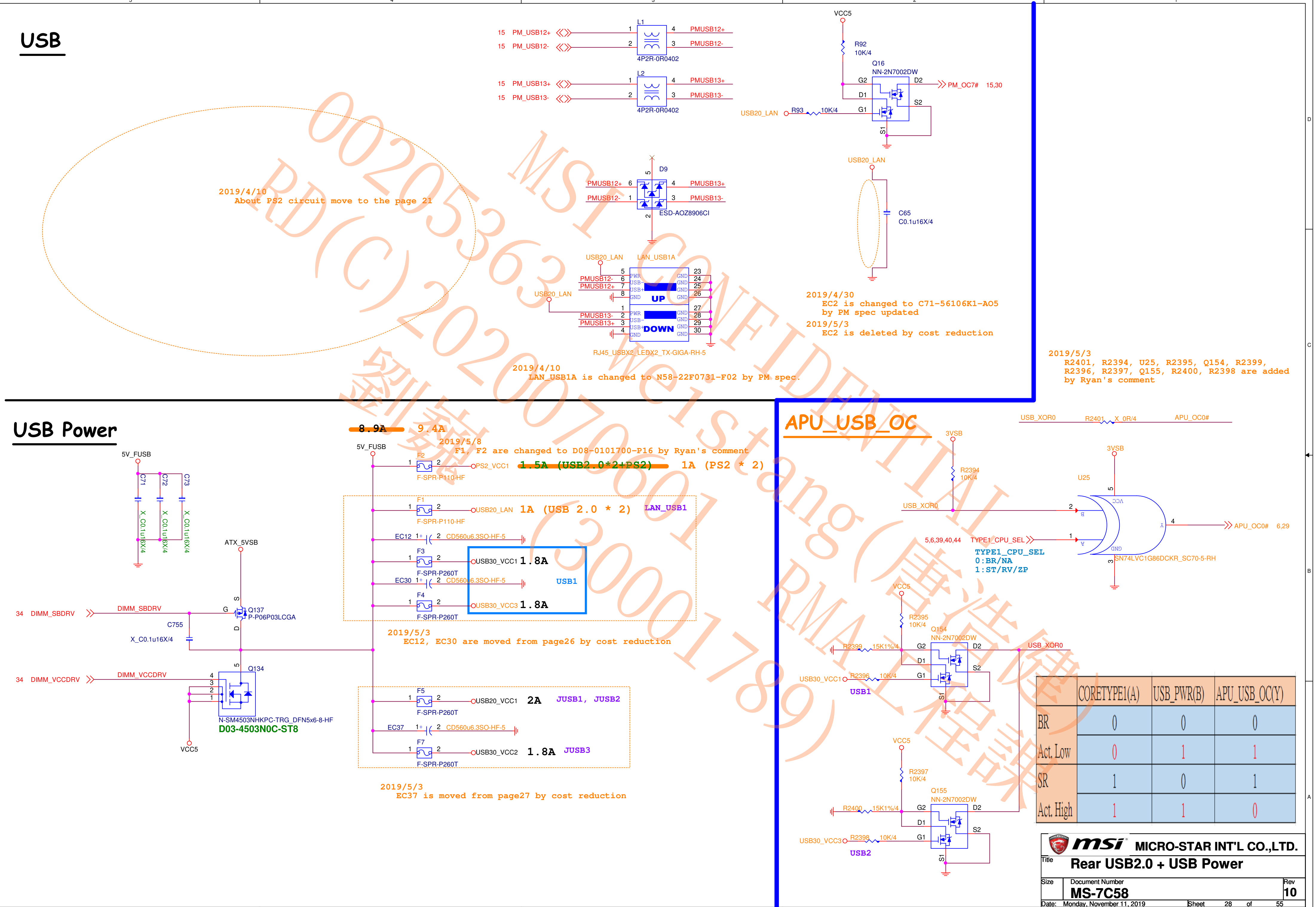
USB



15 PM_USB12+
15 PM_USB12-
L1
4P2R-0R0402
PMUSB12+
PMUSB12-
15 PM_USB13+
15 PM_USB13-
L2
4P2R-0R0402
PMUSB13+
PMUSB13-
VCC5
R92
10K/4
Q16
NN-2N7002DW
G2
D2
D1
G1
S2
S1
PM_OC7# 15,30
USB20_LAN
R93
10K/4
D9
PMUSB12+
PMUSB12-
PMUSB13+
PMUSB13-
ESD-AOZ8906CI
C65
C0.1u16X/4
USB20_LAN
LAN_USB1A
PMUSB12-
PMUSB12+
PMUSB13-
PMUSB13+
UP
DOWN
RJ45_USBX2_LEDX2_TX-GIGA-RH-5
5V_FUSB
C71
C72
C73
X_C0.1u16X/4
ATX_5VSB
34 DIMM_SBDRV
DIMM_SBDRV
Q137
P-P06P03LCGA
C755
X_C0.1u16X/4
34 DIMM_VCCDRV
DIMM_VCCDRV
Q134
N-SM4503NHKPC-TRG_DFN5x6-8-HF
D03-4503N0C-ST8
VCC5
8.9A
9.4A
5V_FUSB
F2
F-SPR-P110-HF
PS2_VCC1
1.5A (USB2.0*2+PS2)
1A (PS2 * 2)
F1
F-SPR-P110-HF
USB20_LAN
1A (USB 2.0 * 2)
LAN_USB1
EC12
CD560u6.3SO-HF-5
F3
F-SPR-P260T
USB30_VCC1
1.8A
EC30
CD560u6.3SO-HF-5
USB1
F4
F-SPR-P260T
USB30_VCC3
1.8A
F5
F-SPR-P260T
USB20_VCC1
2A
JUSB1, JUSB2
EC37
CD560u6.3SO-HF-5
F7
F-SPR-P260T
USB30_VCC2
1.8A
JUSB3
APU_USB_OC
USB_XOR0
R2401
X_0R/4
APU_OC0#
3VSB
R2394
10K/4
3VSB
U25
USB_XOR0
5,6,39,40,44
TYPE1_CPU_SEL
APU_OC0# 6,29
SN74LVC1G86DCKR_SC70-5-RH
TYPE1_CPU_SEL
0:BR/NA
1:ST/RV/ZP
VCC5
R2395
10K/4
Q154
NN-2N7002DW
R2399
15K1%/4
USB_XOR0
USB30_VCC1
R2396
10K/4
USB1
VCC5
R2397
10K/4
Q155
NN-2N7002DW
R2400
15K1%/4
USB30_VCC3
R2398
10K/4
USB2

2019/4/10
About PS2 circuit move to the page 21

2019/4/30
EC2 is changed to C71-56106K1-A05
by PM spec updated

2019/5/3
EC2 is deleted by cost reduction

2019/4/10
LAN_USB1A is changed to N58-22F0731-F02 by PM spec.

2019/5/3
R2401, R2394, U25, R2395, Q154, R2399,
R2396, R2397, Q155, R2400, R2398 are added
by Ryan's comment

USB Power

2019/5/8
F1, F2 are changed to D08-0101700-P16 by Ryan's comment

2019/5/3
EC12, EC30 are moved from page26 by cost reduction

2019/5/3
EC37 is moved from page27 by cost reduction

APU_USB_OC

	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

MICRO-STAR INT'L CO.,LTD.
Title: Rear USB2.0 + USB Power
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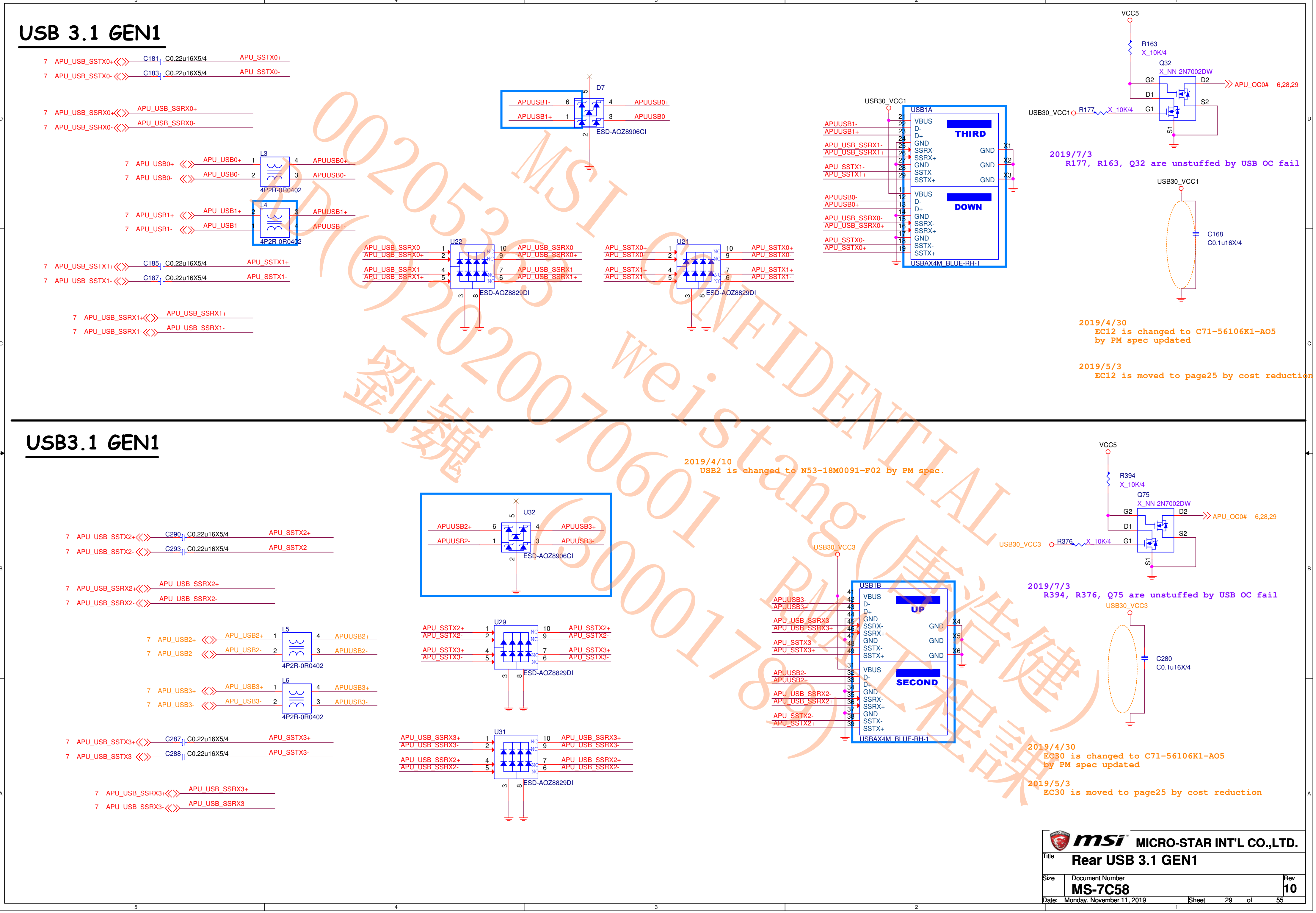
USB 3.1 GEN1
APU_USB_SSTX0+
APU_USB_SSTX0-
C181 C0.22u16X5/4
C183 C0.22u16X5/4
APU_SSTX0+
APU_SSTX0-
APU_USB_SSRX0+
APU_USB_SSRX0-
APU_USB0+
APU_USB0-
L3
4P2R-0R0402
APUUSB0+
APUUSB0-
APU_USB1+
APU_USB1-
L4
APUUSB1+
APUUSB1-
APU_USB_SSTX1+
APU_USB_SSTX1-
C185 C0.22u16X5/4
C187 C0.22u16X5/4
APU_SSTX1+
APU_SSTX1-
APU_USB_SSRX1+
APU_USB_SSRX1-
D7
ESD-AOZ8906CI
U22
ESD-AOZ8829DI
U21
USB30_VCC1
USB1A
VBUS
D-
D+
GND
SSRX-
SSRX+
SSTX-
SSTX+
THIRD
DOWN
USBAX4M_BLUE-RH-1
VCC5
R163
X_10K/4
Q32
X_NN-2N7002DW
APU_OC0# 6,28,29
R177
2019/7/3
R177, R163, Q32 are unstuffed by USB OC fail
C168
C0.1u16X/4
2019/4/30
EC12 is changed to C71-56106K1-AO5
by PM spec updated
2019/5/3
EC12 is moved to page25 by cost reduction
USB3.1 GEN1
2019/4/10
USB2 is changed to N53-18M0091-F02 by PM spec.
U32
ESD-AOZ8906CI
APUUSB2+
APUUSB2-
APUUSB3+
APUUSB3-
APU_USB_SSTX2+
APU_USB_SSTX2-
C290 C0.22u16X5/4
C293 C0.22u16X5/4
APU_SSTX2+
APU_SSTX2-
APU_USB_SSRX2+
APU_USB_SSRX2-
APU_USB2+
APU_USB2-
L5
APU_USB3+
APU_USB3-
L6
APU_USB_SSTX3+
APU_USB_SSTX3-
C287 C0.22u16X5/4
C288 C0.22u16X5/4
APU_SSTX3+
APU_SSTX3-
APU_USB_SSRX3+
APU_USB_SSRX3-
U29
U31
USB30_VCC3
USB1B
UP
SECOND
R394
X_10K/4
Q75
R376
2019/7/3
R394, R376, Q75 are unstuffed by USB OC fail
C280
C0.1u16X/4
2019/4/30
EC30 is changed to C71-56106K1-AO5
by PM spec updated
2019/5/3
EC30 is moved to page25 by cost reduction
MICRO-STAR INT'L CO.,LTD.
Title
Rear USB 3.1 GEN1
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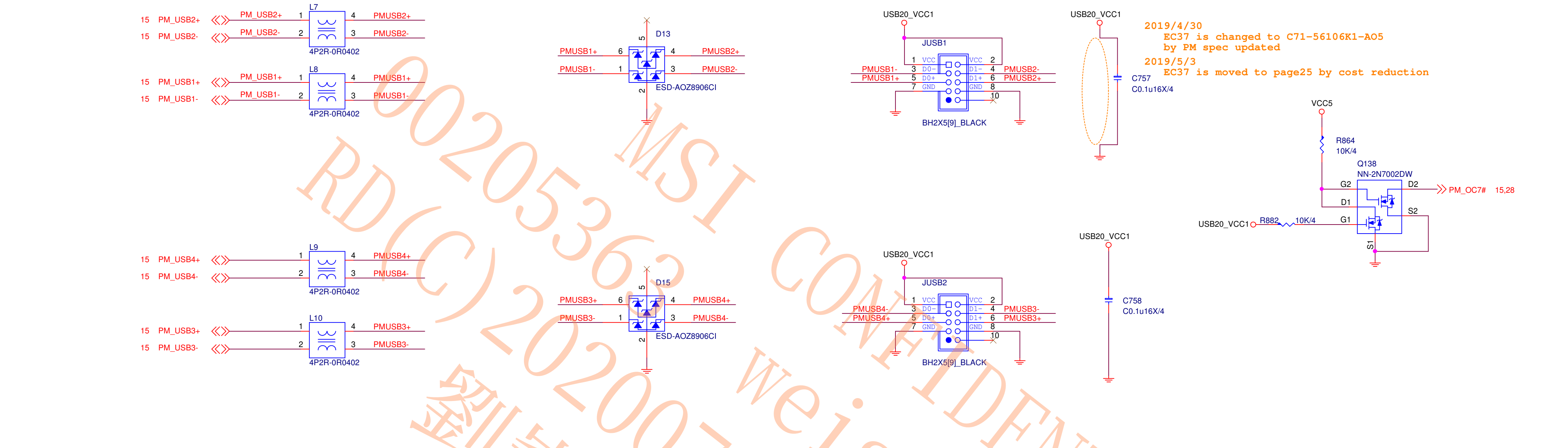
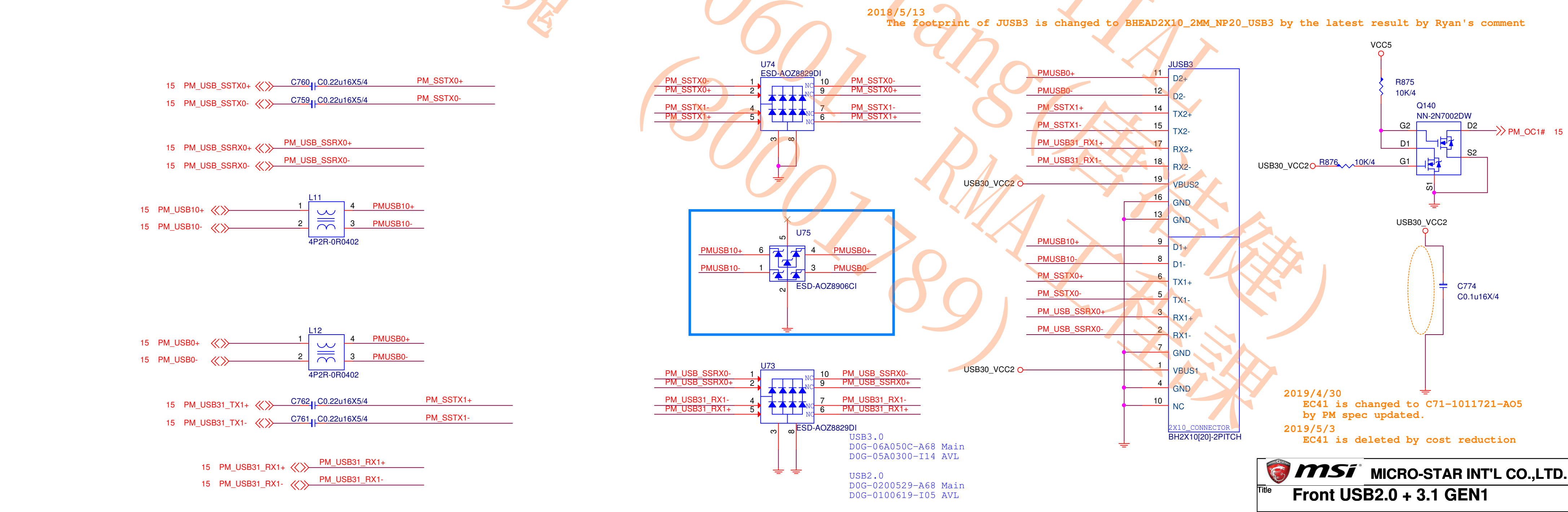
Front USB2.0



PM_USB2+
PM_USB2-
PM_USB1+
PM_USB1-
PM_USB4+
PM_USB4-
PM_USB3+
PM_USB3-
L7
L8
L9
L10
4P2R-0R0402
PMUSB2+
PMUSB2-
PMUSB1+
PMUSB1-
PMUSB4+
PMUSB4-
PMUSB3+
PMUSB3-
D13
D15
ESD-AOZ8906CI
USB20_VCC1
JUSB1
JUSB2
BH2X5[9]_BLACK
C757
C0.1u16X/4
C758
C0.1u16X/4
2019/4/30
EC37 is changed to C71-56106K1-A05
by PM spec updated
2019/5/3
EC37 is moved to page25 by cost reduction
VCC5
R864
10K/4
Q138
NN-2N7002DW
PM_OC7# 15,28
R882 10K/4

Front USB3.1 GEN1



2018/5/13
The footprint of JUSB3 is changed to BHEAD2X10_2MM_NP20_USB3 by the latest result by Ryan's comment
PM_USB_SSTX0+
PM_USB_SSTX0-
C760 C0.22u16X5/4
C759 C0.22u16X5/4
PM_SSTX0+
PM_SSTX0-
PM_USB_SSRX0+
PM_USB_SSRX0-
PM_USB10+
PM_USB10-
L11
L12
4P2R-0R0402
PMUSB10+
PMUSB10-
PM_USB0+
PM_USB0-
PMUSB0+
PMUSB0-
PM_USB31_TX1+
PM_USB31_TX1-
C762 C0.22u16X5/4
C761 C0.22u16X5/4
PM_SSTX1+
PM_SSTX1-
PM_USB31_RX1+
PM_USB31_RX1-
U74
ESD-AOZ8829DI
U75
ESD-AOZ8906CI
U73
ESD-AOZ8829DI
USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL
USB2.0
D0G-0200529-A68 Main
D0G-0100619-I05 AVL
USB30_VCC2
JUSB3
D2+
D2-
TX2+
TX2-
RX2+
RX2-
VBUS2
GND
D1+
D1-
TX1+
TX1-
RX1+
RX1-
VBUS1
NC
2X10_CONNECTOR
BH2X10[20]-2PITCH
VCC5
R875
10K/4
Q140
NN-2N7002DW
PM_OC1# 15
R876 10K/4
C774
C0.1u16X/4
2019/4/30
EC41 is changed to C71-1011721-A05
by PM spec updated.
2019/5/3
EC41 is deleted by cost reduction

MICRO-STAR INT'L CO.,LTD.

Title: Front USB2.0 + 3.1 GEN1

Size	Document Number	Rev
	MS-7C58	10

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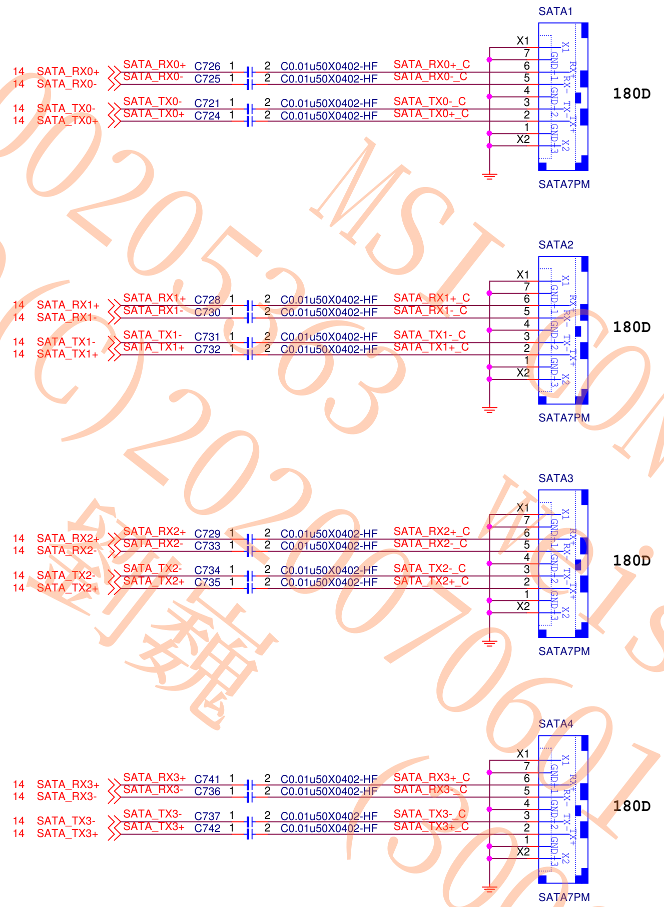
SATA Connector



SATA1
SATA7PM
180D
14 SATA_RX0+
14 SATA_RX0-
14 SATA_TX0-
14 SATA_TX0+
C726 C0.01u50X0402-HF SATA_RX0+_C
C725 C0.01u50X0402-HF SATA_RX0-_C
C721 C0.01u50X0402-HF SATA_TX0-_C
C724 C0.01u50X0402-HF SATA_TX0+_C
SATA2
SATA7PM
180D
14 SATA_RX1+
14 SATA_RX1-
14 SATA_TX1-
14 SATA_TX1+
C728 C0.01u50X0402-HF SATA_RX1+_C
C730 C0.01u50X0402-HF SATA_RX1-_C
C731 C0.01u50X0402-HF SATA_TX1-_C
C732 C0.01u50X0402-HF SATA_TX1+_C
SATA3
SATA7PM
180D
14 SATA_RX2+
14 SATA_RX2-
14 SATA_TX2-
14 SATA_TX2+
C729 C0.01u50X0402-HF SATA_RX2+_C
C733 C0.01u50X0402-HF SATA_RX2-_C
C734 C0.01u50X0402-HF SATA_TX2-_C
C735 C0.01u50X0402-HF SATA_TX2+_C
SATA4
SATA7PM
180D
14 SATA_RX3+
14 SATA_RX3-
14 SATA_TX3-
14 SATA_TX3+
C741 C0.01u50X0402-HF SATA_RX3+_C
C736 C0.01u50X0402-HF SATA_RX3-_C
C737 C0.01u50X0402-HF SATA_TX3-_C
C742 C0.01u50X0402-HF SATA_TX3+_C
X1 7 6 5 4 3 2 1 X2

MICRO-STAR INT'L CO.,LTD.

Title	SATA Connector	
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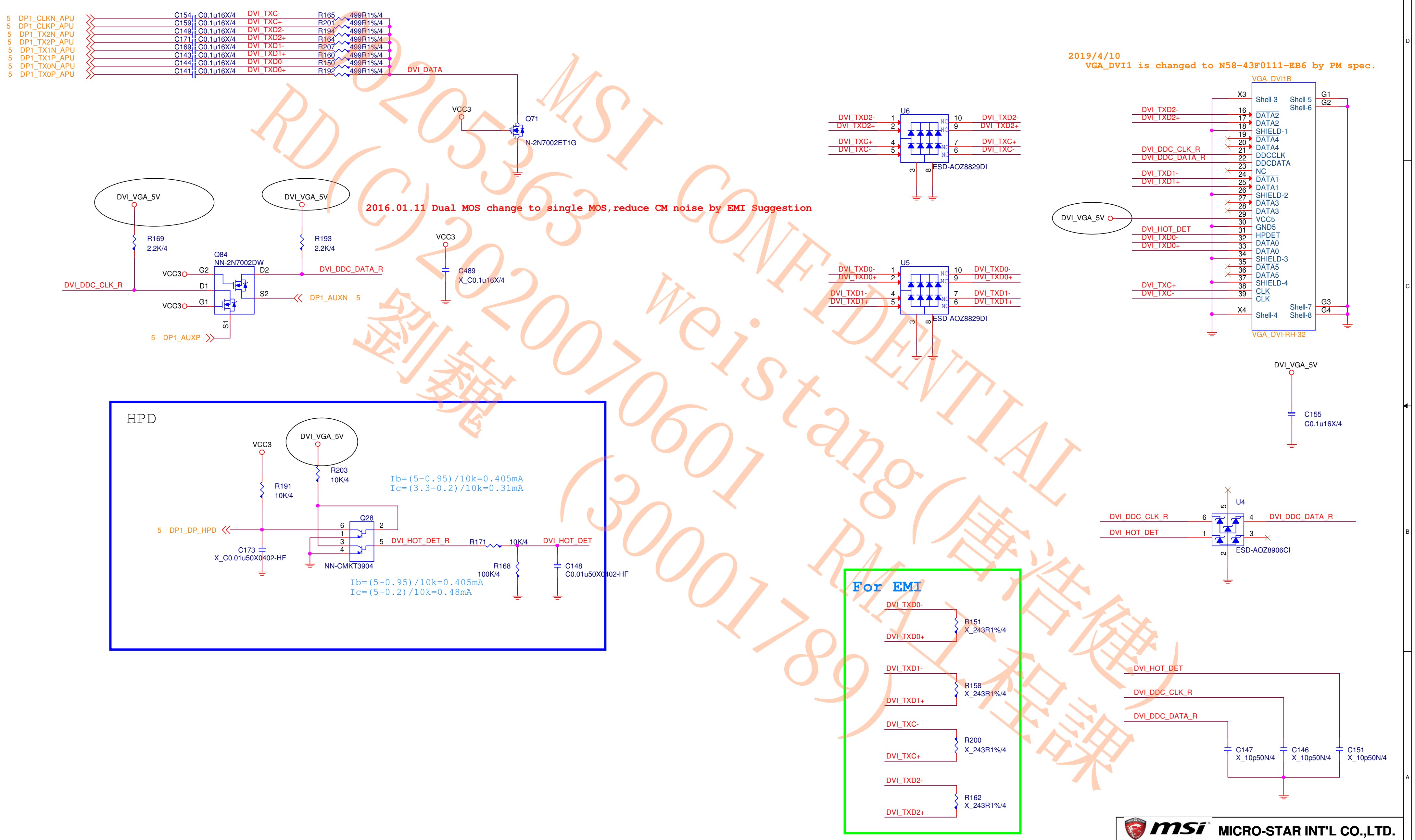
DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



5 DP1_CLKN_APU
5 DP1_CLKP_APU
5 DP1_TX2N_APU
5 DP1_TX2P_APU
5 DP1_TX1N_APU
5 DP1_TX1P_APU
5 DP1_TX0N_APU
5 DP1_TX0P_APU
C154 C0.1u16X/4 DVI_TXC- R165 499R1%/4
C159 C0.1u16X/4 DVI_TXC+ R201 499R1%/4
C149 C0.1u16X/4 DVI_TXD2- R194 499R1%/4
C171 C0.1u16X/4 DVI_TXD2+ R164 499R1%/4
C169 C0.1u16X/4 DVI_TXD1- R207 499R1%/4
C143 C0.1u16X/4 DVI_TXD1+ R160 499R1%/4
C144 C0.1u16X/4 DVI_TXD0- R150 499R1%/4
C141 C0.1u16X/4 DVI_TXD0+ R192 499R1%/4
DVI_DATA
VCC3
Q71
N-2N7002ET1G
2016.01.11 Dual MOS change to single MOS,reduce CM noise by EMI Suggestion
DVI_VGA_5V
R169 2.2K/4
DVI_VGA_5V
R193 2.2K/4
Q84 NN-2N7002DW
VCC3 G2 D2 DVI_DDC_DATA_R
DVI_DDC_CLK_R D1 S2 DP1_AUXN 5
VCC3 G1 S1
5 DP1_AUXP
VCC3
C489 X_C0.1u16X/4
U6
DVI_TXD2- 1 10 DVI_TXD2-
DVI_TXD2+ 2 9 DVI_TXD2+
DVI_TXC+ 4 7 DVI_TXC+
DVI_TXC- 5 6 DVI_TXC-
ESD-AOZ8829DI
U5
DVI_TXD0- 1 10 DVI_TXD0-
DVI_TXD0+ 2 9 DVI_TXD0+
DVI_TXD1- 4 7 DVI_TXD1-
DVI_TXD1+ 5 6 DVI_TXD1+
ESD-AOZ8829DI
2019/4/10
VGA_DVI1 is changed to N58-43F0111-EB6 by PM spec.
VGA_DVI1B
Shell-3 Shell-5 Shell-6 G1 G2
DVI_TXD2- 16 DATA2
DVI_TXD2+ 17 DATA2
18 SHIELD-1
19 DATA4
20 DATA4
DVI_DDC_CLK_R 21 DDCCLK
DVI_DDC_DATA_R 22 DDCDATA
23 NC
DVI_TXD1- 24 DATA1
DVI_TXD1+ 25 DATA1
26 SHIELD-2
27 DATA3
28 DATA3
DVI_VGA_5V 29 VCC5
30 GND5
DVI_HOT_DET 31 HPDET
DVI_TXD0- 32 DATA0
DVI_TXD0+ 33 DATA0
34 SHIELD-3
35 DATA5
36 DATA5
37 SHIELD-4
DVI_TXC+ 38 CLK
DVI_TXC- 39 CLK
X4 Shell-4 Shell-7 Shell-8 G3 G4
VGA_DVI-RH-32
DVI_VGA_5V
C155 C0.1u16X/4
HPD
VCC3
DVI_VGA_5V
R203 10K/4
R191 10K/4
Ib=(5-0.95)/10k=0.405mA
Ic=(3.3-0.2)/10k=0.31mA
5 DP1_DP_HPD
Q28
C173 X_C0.01u50X0402-HF
NN-CMKT3904
DVI_HOT_DET_R R171 10K/4 DVI_HOT_DET
R168 100K/4
C148 C0.01u50X0402-HF
Ib=(5-0.95)/10k=0.405mA
Ic=(5-0.2)/10k=0.48mA
U4
DVI_DDC_CLK_R 6 4 DVI_DDC_DATA_R
DVI_HOT_DET 1 3
ESD-AOZ8906CI
For EMI
DVI_TXD0- R151 X_243R1%/4 DVI_TXD0+
DVI_TXD1- R158 X_243R1%/4 DVI_TXD1+
DVI_TXC- R200 X_243R1%/4 DVI_TXC+
DVI_TXD2- R162 X_243R1%/4 DVI_TXD2+
DVI_HOT_DET
DVI_DDC_CLK_R
DVI_DDC_DATA_R
C147 X_10p50N/4
C146 X_10p50N/4
C151 X_10p50N/4

MICRO-STAR INT'L CO.,LTD.

Title	DVI Connector	
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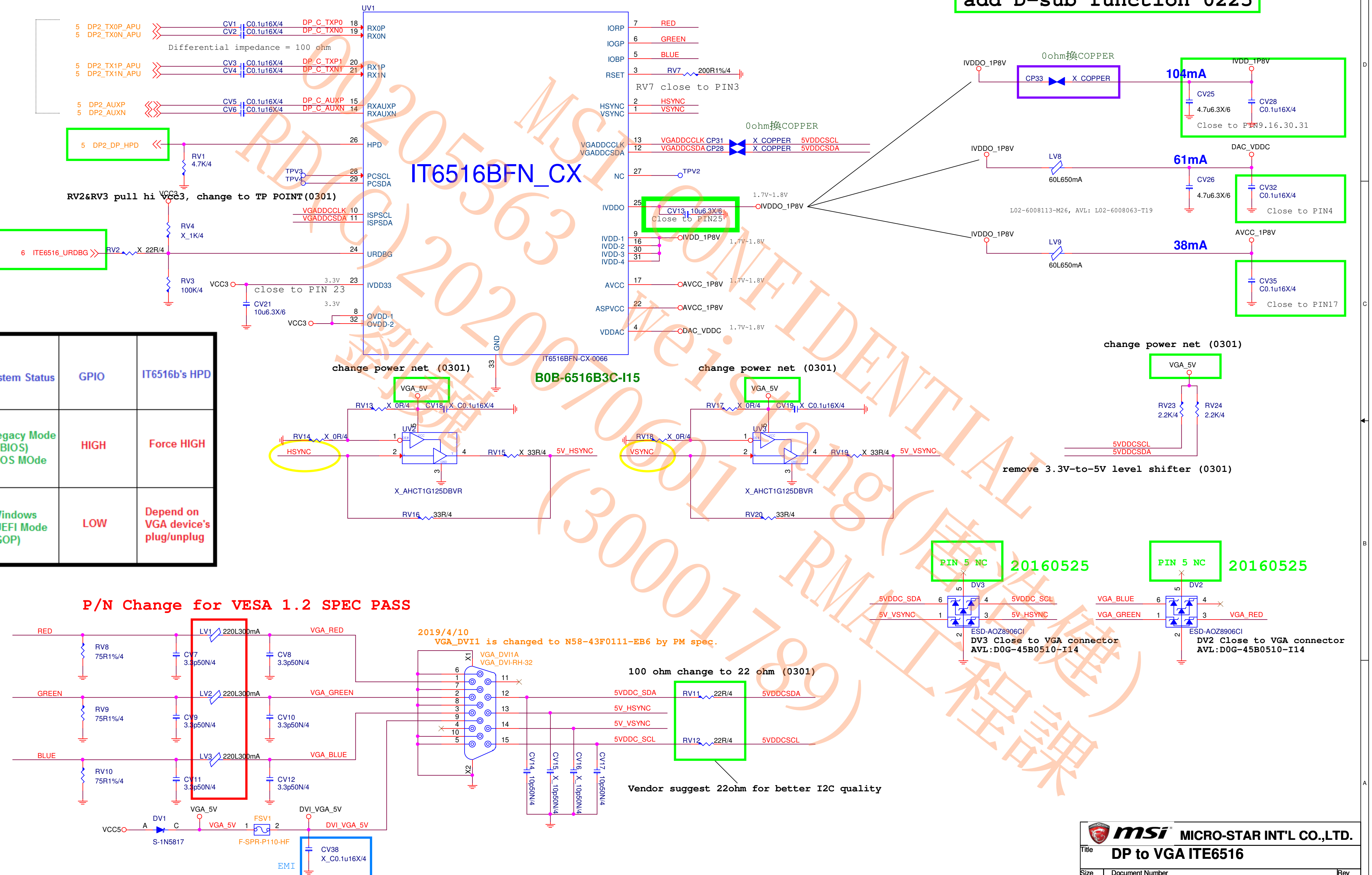
2019/5/8

Note: 7C52-02S are all no unstuff expect for DV1, FSV1, CV38, VGA_DVI1

20181203:
UV1 change to B0B-6516B3C-I15, FW改善省電.

If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

add D-sub function 0225



UV1
DP2_TX0P_APU
DP2_TX0N_APU
Differential impedance = 100 ohm
DP2_TX1P_APU
DP2_TX1N_APU
DP2_AUXP
DP2_AUXN
DP2_DP_HPD
RV1 4.7K/4
RV2&RV3 pull hi VCC3, change to TP POINT(0301)
RV4 X_1K/4
ITE6516_URDBG
RV2 X_22R/4
RV3 100K/4
VCC3
close to PIN 23
CV21 10u6.3X/6
IT6516BFN_CX
IT6516BFN-CX-0066
B0B-6516B3C-I15
RX0P
RX0N
RX1P
RX1N
RXAUXP
RXAUXN
HPD
PCSCL
PCSDA
ISPSCL
ISPSDA
URDBG
IVDD33
OVDD-1
OVDD-2
GND
IORP
IOGP
IOBP
RSET
HSYNC
VSYNC
VGADDCCLK
VGADDCSDA
NC
IVDDO
IVDD-1
IVDD-2
IVDD-3
IVDD-4
AVCC
ASPVCC
VDDAC
RED
GREEN
BLUE
RV7 200R1%/4
RV7 close to PIN3
0ohm換COPPER
CP31 X_COPPER
CP28 X_COPPER
5VDDCSCL
5VDDCSDA
TPV2
CV13 10u6.3X/6
Close to PIN25
IVDDO_1P8V
IVDD_1P8V
AVCC_1P8V
DAC_VDDC
1.7V~1.8V
CP33 X_COPPER
104mA
CV25 4.7u6.3X/6
CV28 C0.1u16X/4
Close to PIN9.16.30.31
LV8 60L650mA
61mA
CV26 4.7u6.3X/6
CV32 C0.1u16X/4
Close to PIN4
L02-6008113-M26, AVL: L02-6008063-T19
LV9 60L650mA
38mA
CV35 C0.1u16X/4
Close to PIN17
change power net (0301)
VGA_5V
RV23 2.2K/4
RV24 2.2K/4
remove 3.3V-to-5V level shifter (0301)
RV13 X_0R/4
CV18 X_C0.1u16X/4
RV14 X_0R/4
UV2
X_AHCT1G125DBVR
RV15 X_33R/4
5V_HSYNC
RV16 33R/4
RV17 X_0R/4
CV19 X_C0.1u16X/4
RV18 X_0R/4
UV3
RV19 X_33R/4
5V_VSYNC
RV20 33R/4
PIN 5 NC
20160525
DV3
ESD-AOZ8906CI
DV3 Close to VGA connector
AVL:D0G-45B0510-I14
DV2
DV2 Close to VGA connector
AVL:D0G-45B0510-I14
5VDDC_SDA
5VDDC_SCL
5V_VSYNC
5V_HSYNC
VGA_BLUE
VGA_GREEN
VGA_RED
P/N Change for VESA 1.2 SPEC PASS
RV8 75R1%/4
CV7 3.3p50N/4
LV1 220L300mA
CV8 3.3p50N/4
RV9 75R1%/4
CV9 3.3p50N/4
LV2 220L300mA
CV10 3.3p50N/4
RV10 75R1%/4
CV11 3.3p50N/4
LV3 220L300mA
CV12 3.3p50N/4
2019/4/10
VGA_DVI1 is changed to N58-43F0111-EB6 by PM spec.
VGA_DVI1A
VGA_DVI-RH-32
100 ohm change to 22 ohm (0301)
RV11 22R/4
RV12 22R/4
Vendor suggest 22ohm for better I2C quality
CV14 10p50N/4
CV15 X_10p50N/4
CV16 X_10p50N/4
CV17 10p50N/4
VCC5
DV1
S-1N5817
FSV1
F-SPR-P110-HF
DVI_VGA_5V
CV38 X_C0.1u16X/4
EMI

System Status	GPIO	IT6516b's HPD
Legacy Mode (VBIOS) /DOS MOde	HIGH	Force HIGH
Windows /UEFI Mode (GOP)	LOW	Depend on VGA device's plug/unplug

2019/5/6
FSV1 is changed to D08-0101700-P16 by Ivy's comment

MICRO-STAR INT'L CO.,LTD.

Title	DP to VGA ITE6516		
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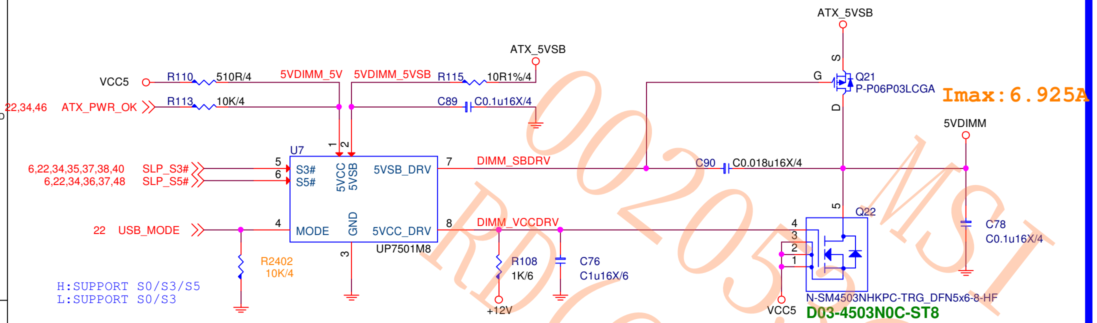
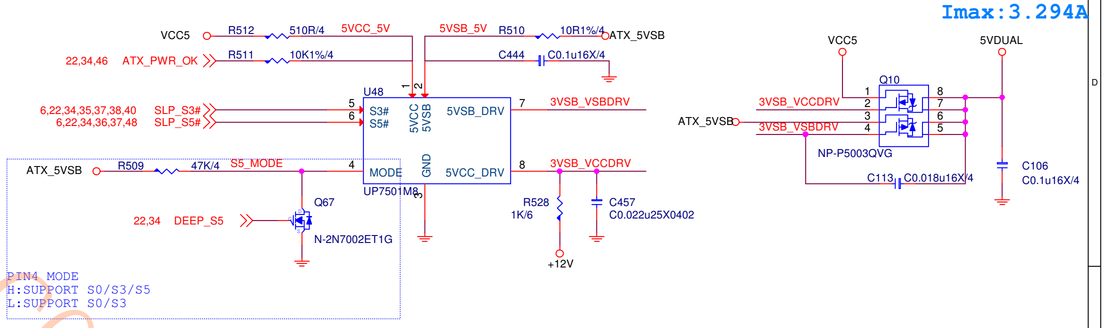
5VDIMM FOR DDR


ATX_5VSB
VCC5
R110 510R/4
5VDIMM_5V
5VDIMM_5VSB
R115 10R1%/4
22,34,46 ATX_PWR_OK
R113 10K/4
C89 C0.1u16X/4
G
S
D
Q21
P-P06P03LCGA
Imax:6.925A
5VDIMM
U7
6,22,34,35,37,38,40 SLP_S3#
6,22,34,36,37,48 SLP_S5#
S3#
S5#
5VCC
5VSB
5VSB_DRV
DIMM_SBDRV
C90 C0.018u16X/4
22 USB_MODE
MODE
GND
5VCC_DRV
DIMM_VCCDRV
UP7501M8
R2402 10K/4
R108 1K/6
C76 C1u16X/6
+12V
Q22
C78 C0.1u16X/4
VCC5
N-SM4503NHKPC-TRG_DFN5x6-8-HF
D03-4503N0C-ST8
H:SUPPORT S0/S3/S5
L:SUPPORT S0/S3

2019/5/8
R2402 is added by Ryan's comment

28 DIMM_VCCDRV — DIMM_VCCDRV
28 DIMM_SBDRV — DIMM_SBDRV

5VDUAL For 3VSB、CPU 1.8V 、 VDDP

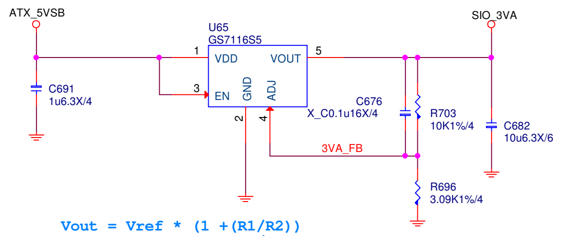

Imax:3.294A
VCC5
R512 510R/4
5VCC_5V
5VSB_5V
R510 10R1%/4
ATX_5VSB
22,34,46 ATX_PWR_OK
R511 10K1%/4
C444 C0.1u16X/4
U48
6,22,34,35,37,38,40 SLP_S3#
6,22,34,36,37,48 SLP_S5#
S3#
S5#
5VCC
5VSB
5VSB_DRV
3VSB_VSBDRV
ATX_5VSB
R509 47K/4
S5_MODE
MODE
GND
5VCC_DRV
3VSB_VCCDRV
UP7501M8
Q67
22,34 DEEP_S5
N-2N7002ET1G
R528 1K/6
C457 C0.022u25X0402
+12V
PIN4 MODE
H:SUPPORT S0/S3/S5
L:SUPPORT S0/S3
VCC5
5VDUAL
Q10
3VSB_VCCDRV
3VSB_VSBDRV
ATX_5VSB
NP-P5003QVG
C113 C0.018u16X/4
C106 C0.1u16X/4

For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

2019/4/17
R60, C79, Q9, R55, C67 are deleted by Ryan's comment

SIO_3VA

Imax=0.02A

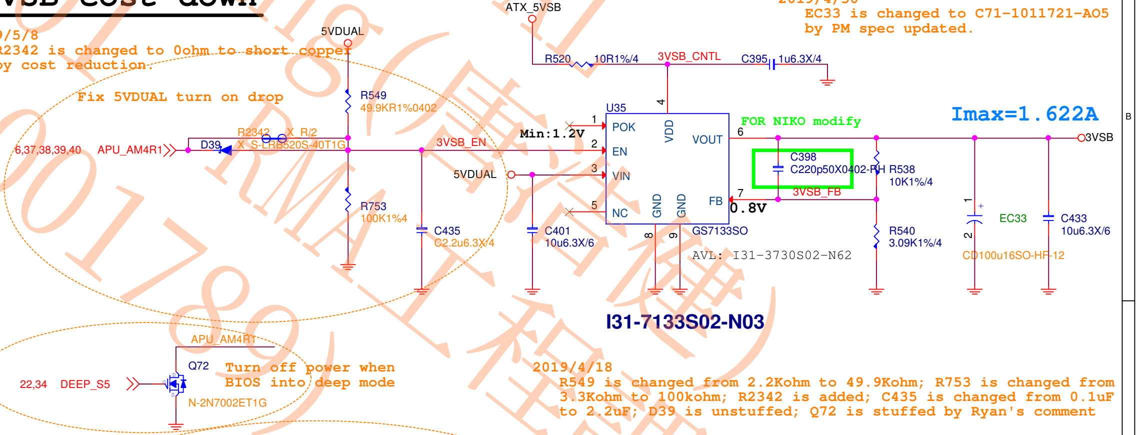


Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.09K))
= 3.38V

3VSB cost down

2019/5/8
R2342 is changed to 0ohm to short copper
by cost reduction.

2019/4/30
EC33 is changed to C71-1011721-A05
by PM spec updated.


Fix 5VDUAL turn on drop
5VDUAL
ATX_5VSB
R520 10R1%/4
3VSB_CNTL
C395 1u6.3X/4
R549 49.9KR1%0402
U35
POK
EN
VIN
NC
VDD
VOUT
GND
FB
Min:1.2V
FOR NIKO modify
Imax=1.622A
3VSB
6,37,38,39,40 APU_AM4R1
D39
R2342 X_R/2
X_S-LRB520S-40T1G
3VSB_EN
5VDUAL
R753 100K1%/4
C435 C2.2u6.3X/4
C401 10u6.3X/6
C398 C220p50X0402-RH
R538 10K1%/4
3VSB_FB
0.8V
GS7133SO
AVL: I31-3730S02-N62
R540 3.09K1%/4
EC33 C0100u16SO-HF-12
C433 10u6.3X/6
I31-7133S02-N03
APU_AM4R1
Q72
22,34 DEEP_S5
N-2N7002ET1G
Turn off power when
BIOS into deep mode

2019/4/18
R549 is changed from 2.2Kohm to 49.9Kohm; R753 is changed from 3.3Kohm to 100kohm; R2342 is added; C435 is changed from 0.1uF to 2.2uF; D39 is unstuffed; Q72 is stuffed by Ryan's comment

2019/4/18
R59, Q2, R62, Q81, R114 are deleted
by Ryan's comment

MSI	MICRO-STAR INT'L CO.,LTD.
Title	ACPI uPI-5VDIMM&3VSB
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Promontory 1.05V_S0

1.05V
S0:5.5A
S5:0.05A

2019/4/12
U58 is changed to SY8288; CHOKE15 is changed to 1R0; L22, L39 are deleted; CHOKE24, C1975, CP71, C605, C1977, C1512, R610 are added; R573 is changed to 39kohm; C519 is changed to 0.1uF;
R582 is changed to 1.33Kohm; R781, R791, C1974 are reserved by Ryan's comment
2019/4/12
U58 is changed to SY8286; R2345, R2343, R2344 are added by Ryan's comment

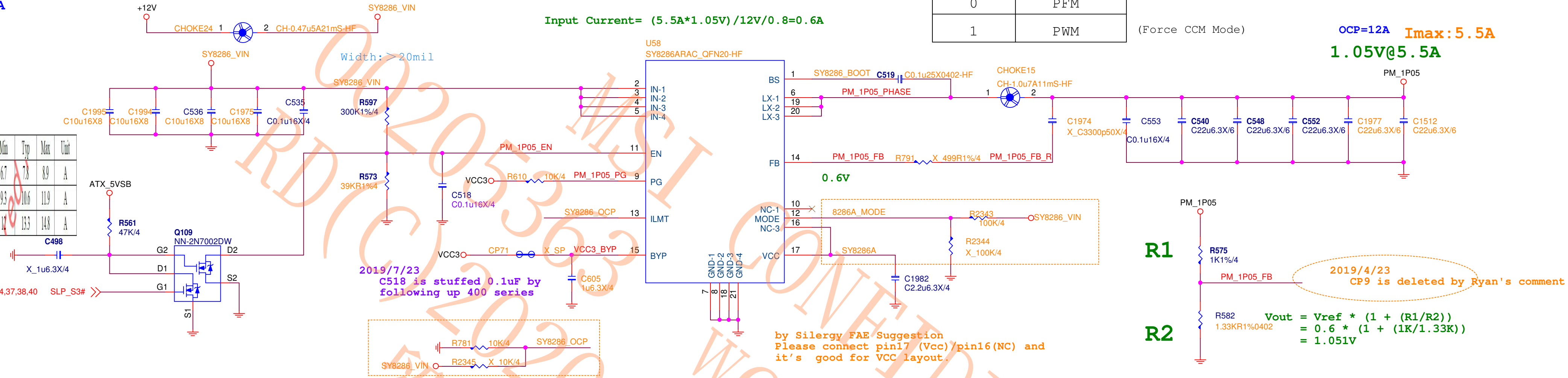
8286A_MODE	Operating mode
0	PFM
1	PWM

(Force CCM Mode)

Input Current= (5.5A*1.05V)/12V/0.8=0.6A

OCP=12A Imax:5.5A
1.05V@5.5A

Test Conditions	Min	Typ	Max	Unit
ILMT=Low	6.7	7.8	8.9	A
ILMT=Floating	9.5	10.6	11.9	A
ILMT=High	12	13.3	14.8	A



+12V
CHOKE24
CH-0.47u5A21mS-HF
SY8286_VIN
Width: >20mil
C1995 C10u16X8
C1994 C10u16X8
C536 C10u16X8
C1975 C10u16X8
C535 C0.1u16X/4
R597 300K1%/4
PM_1P05_EN
R573 39KR1%/4
C518 C0.1u16X/4
VCC3 R610 10K/4 PM_1P05_PG
SY8286_OCP
VCC3 CP71 X_SP VCC3_BYP
C605 1u6.3X/4
ATX_5VSB
R561 47K/4
C498 X_1u6.3X/4
Q109 NN-2N7002DW
6,22,34,37,38,40 SLP_S3#
U58 SY8286ARAC_QFN20-HF
IN-1 IN-2 IN-3 IN-4 EN PG ILMT BYP BS LX-1 LX-2 LX-3 FB NC-1 MODE NC-3 VCC GND-1 GND-2 GND-3 GND-4
SY8286_BOOT C519 C0.1u25X0402-HF
PM_1P05_PHASE
CHOKE15 CH-1.0u7A11mS-HF
PM_1P05
C1974 X_C3300p50X/4
C553 C0.1u16X/4
C540 C22u6.3X/6
C548 C22u6.3X/6
C552 C22u6.3X/6
C1977 C22u6.3X/6
C1512 C22u6.3X/6
PM_1P05_FB R791 X_499R1%/4 PM_1P05_FB_R
0.6V
8286A_MODE R2343 100K/4 SY8286_VIN
R2344 X_100K/4
SY8286A
C1982 C2.2u6.3X/4
R781 10K/4 SY8286_OCP
SY8286_VIN R2345 X_10K/4
R1 R575 1K1%/4
PM_1P05_FB
R2 R582 1.33KR1%0402

2019/7/23
C518 is stuffed 0.1uF by following up 400 series

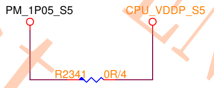
by Silergy FAE Suggestion
Please connect pin17 (Vcc)/pin16(NC) and it's good for VCC layout.

2019/4/23
CP9 is deleted by Ryan's comment

Vout = Vref * (1 + (R1/R2))
= 0.6 * (1 + (1K/1.33K))
= 1.051V

FOR Promontory 1.05V_S5

0.05A



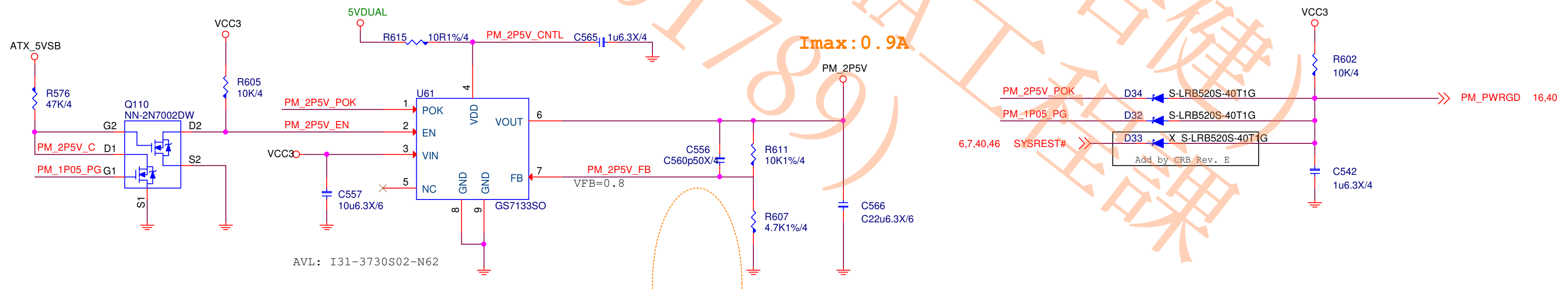
2019/4/16
R2341 is added; R663, C636, C629, U63, R675, R672, C645 are unstuffed by Ryan's comment

2019/4/25
R663, C636, C629, Q73, U63, C646, R675, R672, C645 are deleted by Ryan's comment

Promontory-2.5V

2.5V; 900mA

Imax:0.9A



ATX_5VSB
R576 47K/4
Q110 NN-2N7002DW
PM_2P5V_C
PM_1P05_PG
VCC3
R605 10K/4
5VDUAL
R615 10R1%/4 PM_2P5V_CNTL C565 1u6.3X/4
PM_2P5V_POK
PM_2P5V_EN
VCC3
C557 10u6.3X/6
U61
POK EN VIN NC VDD VOUT FB GND GND
GS7133SO
PM_2P5V_FB
VFB=0.8
C556 C560p50X/4
R611 10K1%/4
R607 4.7K1%/4
PM_2P5V
C566 C22u6.3X/6
VCC3
R602 10K/4
PM_2P5V_POK D34 S-LRB520S-40T1G
PM_1P05_PG D32 S-LRB520S-40T1G
6,7,40,46 SYSREST# D33 X_S-LRB520S-40T1G
Add by CRB Rev. E
PM_PWRGD 16,40
C542 1u6.3X/4

AVL: I31-3730S02-N62

2019/4/23
CP10 is deleted by Ryan's comment

MICRO-STAR INT'L CO.,LTD.
Title: Promontory-1.05V/GS7133-2.5V
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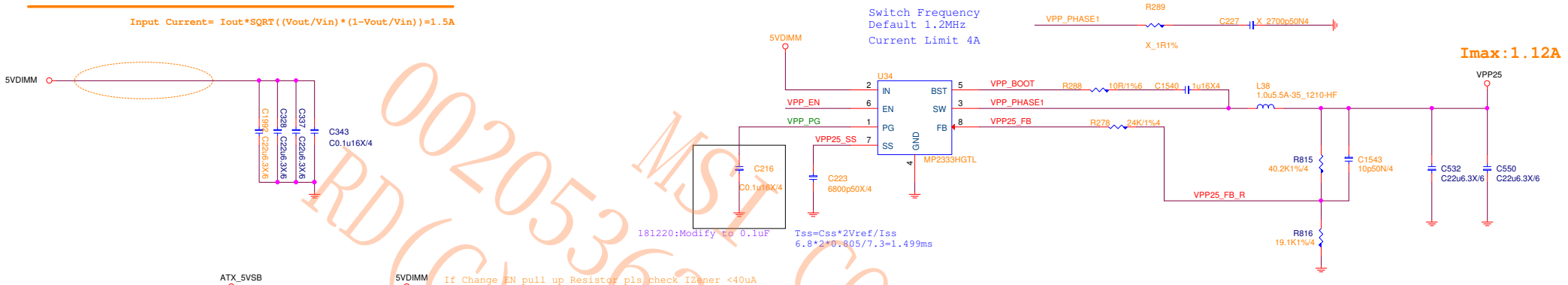
2DIMM :1.12A FOR DDR VPP2.5V

2019/4/12
U34 is changed from MP2143 to MP2333; L29, C443 are deleted and C1992 is added by Ryan's comment

Input Current= Iout*SQRT((Vout/Vin)*(1-Vout/Vin))=1.5A

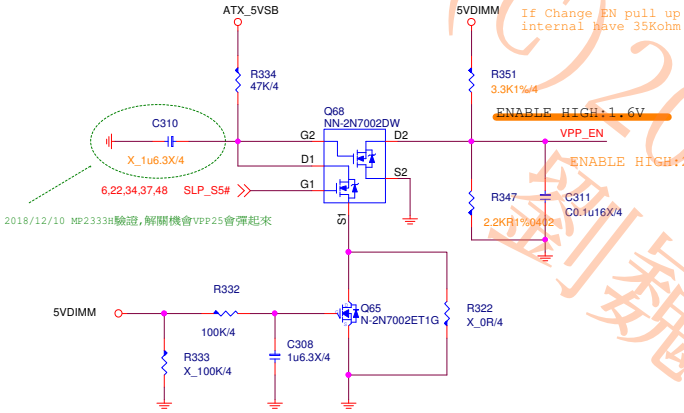
Switch Frequency
Default 1.2MHz
Current Limit 4A

Imax:1.12A



181220:Modify to 0.1uF

Tss=Css*2Vref/Iss
6.8*2*0.805/7.3=1.499ms



2019/4/12
R351 is changed from 2.2Kohm to 100Kohm; R347 is changed from 3.3Kohm to 82kohm; C310 is unstuffed by MP2333 solution

2019/5/7
R351 is changed from 100kohm to 3.3Kohm; R347 is changed from 82Kohm to 2.2Kohm by Ryan's comment

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. EN is clamped internally using a 2.8V series Zener diode (see Figure 2). Connecting the EN input through a pull-up resistor to V_{IN} limits the EN input current below 40µA to prevent damage to the Zener diode. For example, when connecting a 604kΩ pull-up resistor to 12V VIN, I_{Zener} = (12V - 2.8V) / (604kΩ + 35kΩ) = 14µA.

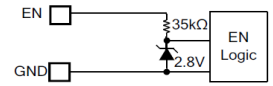
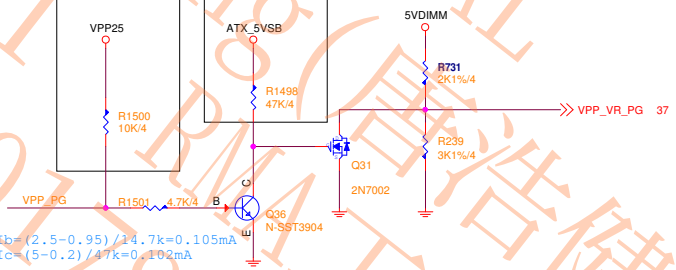


Figure 2: Zener Diode between EN and GND

181220:Modify to 47K

181220:Modify to 10K



2019/4/12
R1500, R1501, R1498, Q36, Q31, R731, R239 are added by MP2333 solution

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Title: DDR PWR VPP25		
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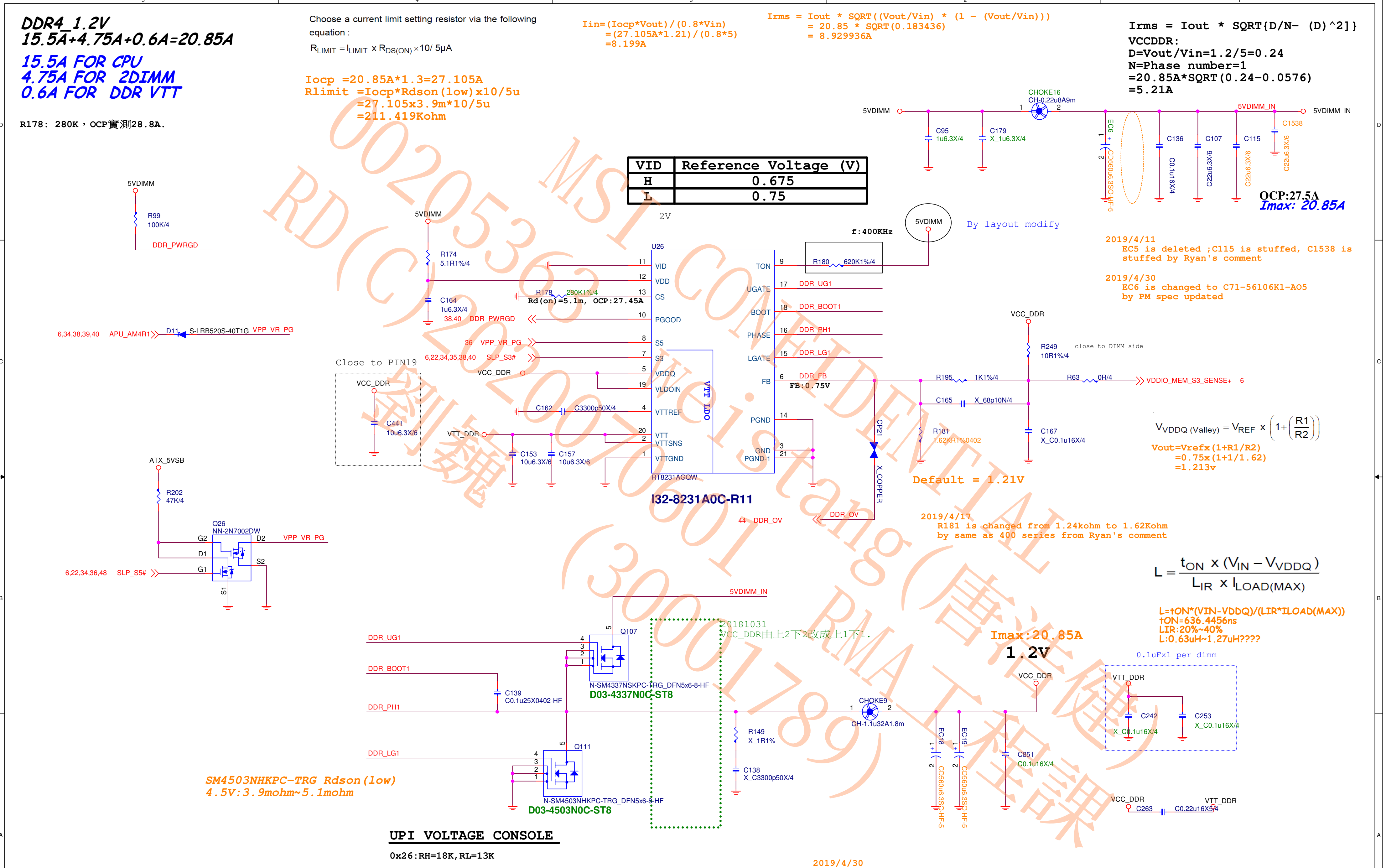
DDR4_1.2V
15.5A+4.75A+0.6A=20.85A
15.5A FOR CPU
4.75A FOR 2DIMM
0.6A FOR DDR VTT
R178: 280K，OCP實測28.8A.
Choose a current limit setting resistor via the following equation :
RLIMIT = ILIMIT x RDS(ON) x10/ 5μA
Iocp =20.85A*1.3=27.105A
Rlimit =Iocp*Rdson(low)x10/5u
=27.105x3.9m*10/5u
=211.419Kohm
Iin=(Iocp*Vout)/(0.8*Vin)
=(27.105A*1.21)/(0.8*5)
=8.199A
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 20.85 * SQRT(0.183436)
= 8.929936A
Irms = Iout * SQRT{D/N- (D)^2]}
VCCDDR:
D=Vout/Vin=1.2/5=0.24
N=Phase number=1
=20.85A*SQRT(0.24-0.0576)
=5.21A
VID | Reference Voltage (V)
H | 0.675
L | 0.75
OCP:27.5A
Imax: 20.85A
By layout modify
f:400KHz
2019/4/11
EC5 is deleted ;C115 is stuffed, C1538 is stuffed by Ryan's comment
2019/4/30
EC6 is changed to C71-56106K1-A05 by PM spec updated
Rd(on)=5.1m, OCP:27.45A
Close to PIN19
FB:0.75V
close to DIMM side
VVDDQ (Valley) = VREF x (1+(R1/R2))
Vout=Vrefx(1+R1/R2)
=0.75x(1+1/1.62)
=1.213v
Default = 1.21V
2019/4/17
R181 is changed from 1.24kohm to 1.62Kohm by same as 400 series from Ryan's comment
I32-8231A0C-R11
L = tON x (VIN – VVDDQ) / (LIR x ILOAD(MAX))
L=tON*(VIN-VDDQ)/(LIR*ILOAD(MAX))
tON=636.4456ns
LIR:20%~40%
L:0.63uH~1.27uH????
0.1uFx1 per dimm
Imax:20.85A
1.2V
20181031
VCC_DDR由上2下2改成上1下1.
D03-4337N0C-ST8
D03-4503N0C-ST8
SM4503NHKPC-TRG Rdson(low)
4.5V:3.9mohm~5.1mohm
UPI VOLTAGE CONSOLE
0x26:RH=18K,RL=13K
2019/4/30
EC18, EC19 are changed to C71-56106K1-A05 by PM spec updated.

MICRO-STAR INT'L CO.,LTD.

Title: DDR Power-RT8231AGQW

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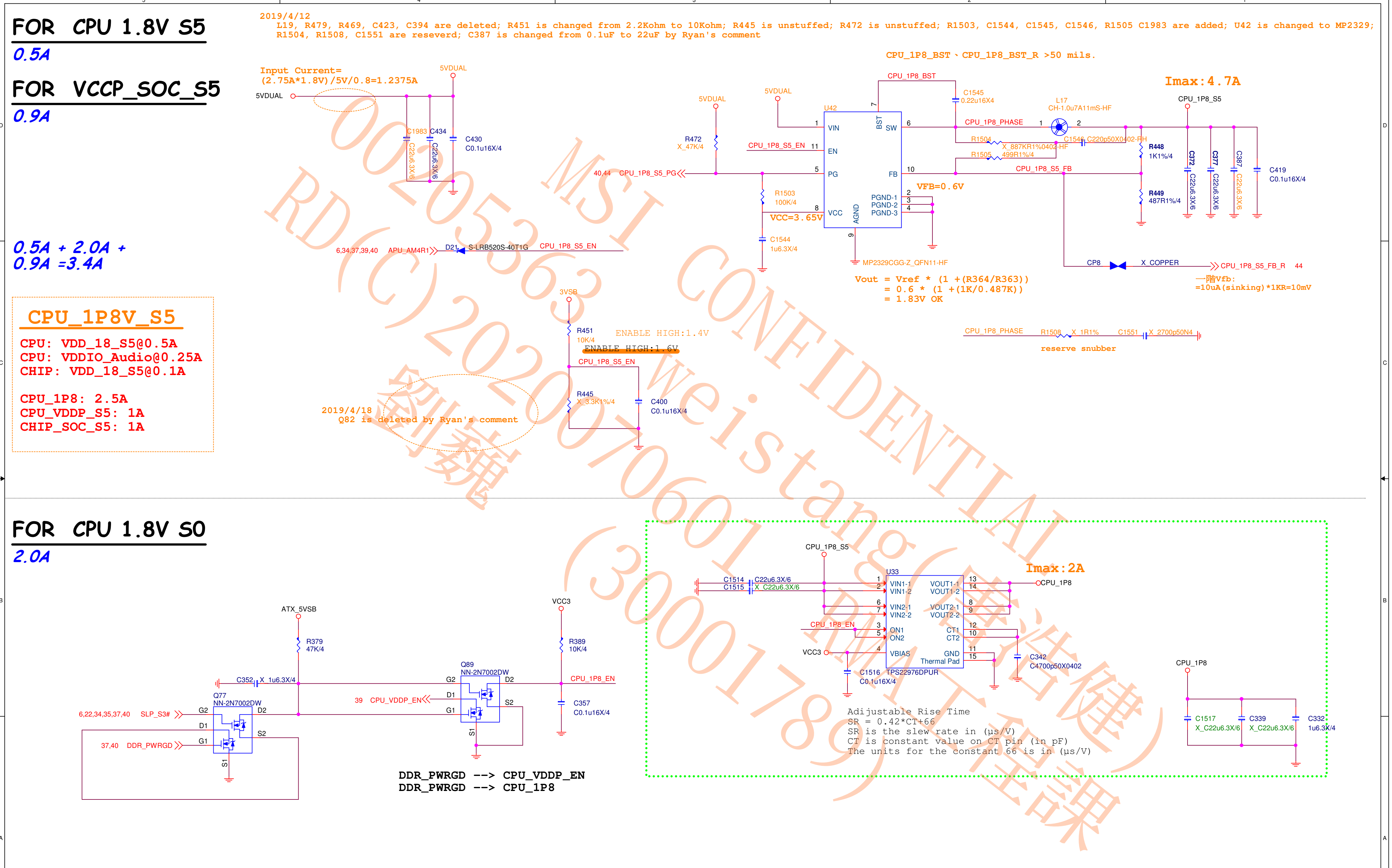

FOR CPU 1.8V S5
0.5A
FOR VCCP_SOC_S5
0.9A
0.5A + 2.0A +
0.9A =3.4A
CPU_1P8V_S5
CPU: VDD_18_S5@0.5A
CPU: VDDIO_Audio@0.25A
CHIP: VDD_18_S5@0.1A
CPU_1P8: 2.5A
CPU_VDDP_S5: 1A
CHIP_SOC_S5: 1A
2019/4/12
L19, R479, R469, C423, C394 are deleted; R451 is changed from 2.2Kohm to 10Kohm; R445 is unstuffed; R472 is unstuffed; R1503, C1544, C1545, C1546, R1505 C1983 are added; U42 is changed to MP2329;
R1504, R1508, C1551 are reseverd; C387 is changed from 0.1uF to 22uF by Ryan's comment
CPU_1P8_BST、CPU_1P8_BST_R >50 mils.
Input Current=
(2.75A*1.8V)/5V/0.8=1.2375A
5VDUAL
C1983 C22u6.3X/6
C434 C22u6.3X/6
C430 C0.1u16X/4
R472 X_47K/4
CPU_1P8_S5_EN
40,44 CPU_1P8_S5_PG
R1503 100K/4
C1544 1u6.3X/4
VCC=3.65V
U42
VIN
EN
PG
VCC
AGND
BST
SW
FB
PGND-1
PGND-2
PGND-3
MP2329CGG-Z_QFN11-HF
CPU_1P8_BST
C1545 0.22u16X4
L17 CH-1.0u7A11mS-HF
CPU_1P8_PHASE
R1504 X_887KR1%0402-HF
C1546 C220p50X0402-HF
R1505 499R1%/4
CPU_1P8_S5_FB
VFB=0.6V
Imax:4.7A
CPU_1P8_S5
R448 1K1%/4
R449 487R1%/4
C372 C22u6.3X/6
C377 C22u6.3X/6
C387 C22u6.3X/6
C419 C0.1u16X/4
CP8 X_COPPER
CPU_1P8_S5_FB_R 44
一階Vfb:
=10uA(sinking)*1KR=10mV
Vout = Vref * (1 +(R364/R363))
= 0.6 * (1 +(1K/0.487K))
= 1.83V OK
6,34,37,39,40 APU_AM4R1
D21 S-LRB520S-40T1G
3VSB
R451 10K/4
ENABLE HIGH:1.4V
ENABLE HIGH:1.6V
R445 X_3.3K1%/4
C400 C0.1u16X/4
2019/4/18
Q82 is deleted by Ryan's comment
CPU_1P8_PHASE R1508 X_1R1% C1551 X_2700p50N4
reserve snubber
FOR CPU 1.8V S0
2.0A
ATX_5VSB
R379 47K/4
C352 X_1u6.3X/4
Q77 NN-2N7002DW
6,22,34,35,37,40 SLP_S3#
37,40 DDR_PWRGD
VCC3
R389 10K/4
Q89 NN-2N7002DW
39 CPU_VDDP_EN
CPU_1P8_EN
C357 C0.1u16X/4
DDR_PWRGD --> CPU_VDDP_EN
DDR_PWRGD --> CPU_1P8
CPU_1P8_S5
C1514 C22u6.3X/6
C1515 X_C22u6.3X/6
U33
VIN1-1
VIN1-2
VIN2-1
VIN2-2
ON1
ON2
VBIAS
VOUT1-1
VOUT1-2
VOUT2-1
VOUT2-2
CT1
CT2
GND
Thermal Pad
TPS22976DPUR
Imax:2A
CPU_1P8
C342 C4700p50X0402
C1516 C0.1u16X/4
Adjustable Rise Time
SR = 0.42*CT+66
SR is the slew rate in (μs/V)
CT is constant value on CT pin (in pF)
The units for the constant 66 is in (μs/V)
C1517 X_C22u6.3X/6
C339 X_C22u6.3X/6
C332 1u6.3X/4

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Title: CPU Power 1P8_S0/S5

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CPU_VDDP

CPU: VDDP@8.5A

Input Current = (8.5A*0.9V)/12V/0.8 = 0.8A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=13*SQRT((0.9/12)*(1-(0.9/12))) = 3.42A
Choke Irms =5 A

L = (Vout/(Fsw*Iripple))*(1-(Vout/Vin))
0.9/(700K*8.5*0.3)*(1-(0.9/12)) = 0.47uH
0.9/(700K*8.5*0.5)*(1-(0.9/12)) = 0.28uH

Isat: 22A

0.9V@8.5A
OCP=13A Imax:8.5A

CPU_VDDP need to confirm 1.05V

+12V, +12V_VDDP, CHOKE14, CH-0.47u5A21mS-HF, C1520 C10u16X8, C348 C10u16X8, C1519 C10u16X8, C1518 C0.1u16X/4

L04-47B7930-M26

CPU_VDDP_SW, R1494 X_1R1% C1532 X_C3300p50X/4
reserve snubber

U41 NB503GQ_QFN16-HF
VIN, BST, SW, EN, 3V3, FB, PG, CLM, MODE1, MODE2, PGND, GND-1, GND-2, GND-3, GND-4, NC-1

CPU_VDDP_EN, CPU_VDDP_BST, CPU_VDDP_SW, CPU_VDDP_3V3, CPU_VDDP_FB, CPU_VDDP_PG, CPU_VDDP_CLM, CPU_VDDP_MODE1, CPU_VDDP_MODE2

C440 0.22u16X4

CHOKE13 CH-0.68u15A5mS-HF-1

R1492 1MR1%0402, C1524 C220p50X0402-RH, R1493 499R1%/4

R823、R344、C822 stuff for stability

C1531 C1525 C1526 C1527 C1528 C1529 C22u6.3X6

C1530 C0.1u16X/4

CPU_VDDP

Internal 3.3V Input

R437 100K/4, C1521 1u6.3X/4, C1522 C0.1u16X/4

R1488 150KR0402 Current limit:13A
R1489 X_R/2 MODE1=0, Vo<3V, DCM 700K
R1491 X_R/2 MODE2=0, Internal 3V3

VFB=0.6V

2019/4/25
CHOKE13 is changed to L04-68B7350-T15
by Ryan's comment

20180822
fix PG glitch when VCC3 ramp up, C386 stuff.

TYPE0_CPU_SEL: 1:TYPE 0 0:TYPE 2
TYPE1_CPU_SEL: 1:TYPE 0 0:TYPE 2
CPU_VDDP_EN: 0:TYPE 2 1:TYPE 0

Q92 NN-2N7002DW
6,40 TYPE0_CPU_SEL, 5,6,28,39,40,44 TYPE1_CPU_SEL, VDDP_SEL, CPU_VDDP_EN → CPU_VDDP_EN 38

CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

CPU_VDDP
R420 6.8R1%0402-HE
CPU_VDDP_SENSE_R, CP35 X_COPPER → CPU_VDDP_SENSE 6
R438 1K1%/4
CPU_VDDP_FB, CP25 X_COPPER → CPU_VDDP_OV 44
R450 1.33KR1%0402

一路VFb:
=10uA(sinking)*1KR=10mV

+12V_VDDP, R406 100K1%/4, 6,34,37,38,39,40 APU_AM4R1, D20 S-LRB520S-40T1G, CPU_VDDP_EN, R418 39K/4, C389 C0.1u16X/4

EN: 1.12-1.32V

Vout=Vref*{1/[R450*(1/R438+1/R1492)]+1}
=0.6*{1/[1.33k*(1/1k+1/1m)]+1}
=1.0506v

CPU_VDDP_S5

CPU: VDDP_S5@1A

2019/7/19
D28 is unstuffed by 7B86 v4.0 refered

6,34,37,38,39,40 APU_AM4R1, D28 X_S-LRB520S-40T1G, VDDP_VSB_EN, C390 X_C0.1u16X/4

2019/4/18
Q98 is deleted by Ryan's comment

5VDUAL, R1496 10R/4, VDDP_VSB_CNTL, C439 1u6.3X/4

3VSB, R502 10K/4, CPU_1P8_S5, C1537 10u6.3X/6, C1536 1u6.3X/4, R501 47K/4, VDDP_VSB_PG

U45 GS7133TD-R_TDFN10
VIN1 VIN2 VIN3 VDD VOUT1 VOUT2 VOUT3 EN FB POK GND

I31-S71330C-N03

0.9W

VDDP_VSB_EN, VDDP_VSB_PG, VDDP_VSB_FB

C1534 C560p50X/4, R1, R489 1K1%/4, R2, R488 3.16KR1%0402-RH, C412 C22u6.3X/6

CPU_VDDP_S5

Vout = Vref * (1+R489/R488)
= 0.8 * (1+1K/3.16K)
= 1.053v

2019/4/16
R490, C436, Q95, R464 are unstuffed by Ryan's comment

Imax:1A
0.9V@1A

VDDP_VSB_FB
ATX_5VSB, R490 X_47K/4, C436 X_C0.1u16X/4
Q95 X_NN-2N7002DW
5,6,28,39,40,44 TYPE1_CPU_SEL
AM4_CPU_SEL
0:Type 0/1
1:Type 2/3
R464 X_3.83K1%/4

R488///R464=1.3139K, Vout=1.056V
R488=8.06K, Vout=0.9V

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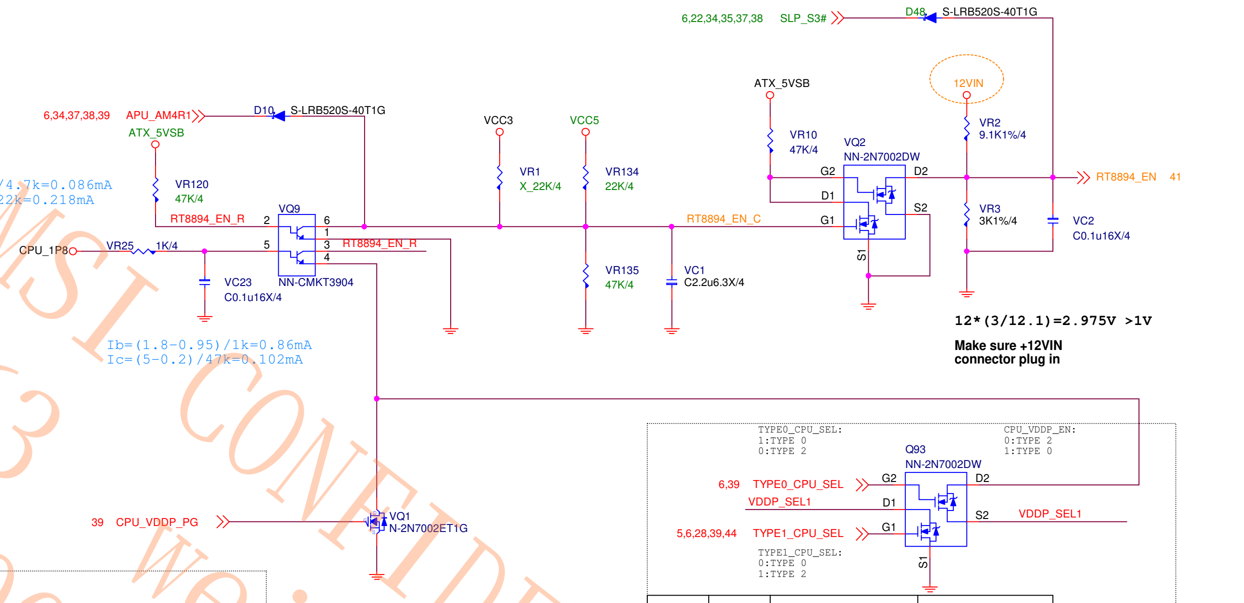
VRM_Enable circuit



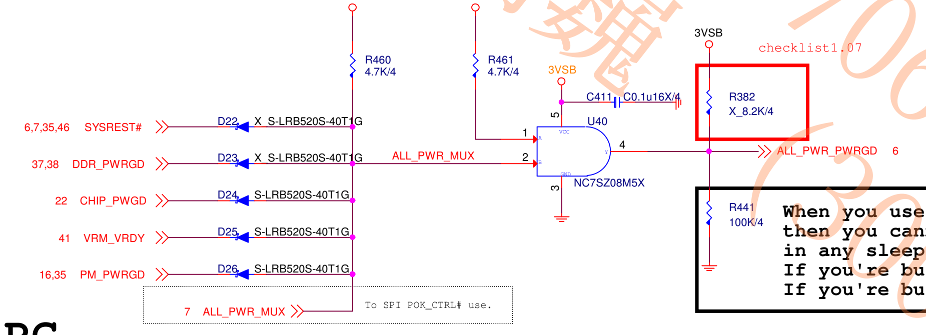
6,22,34,35,37,38 SLP_S3#
D48 S-LRB520S-40T1G
ATX_5VSB
12VIN
6,34,37,38,39 APU_AM4R1
D10 S-LRB520S-40T1G
ATX_5VSB
VCC3
VCC5
VR10 47K/4
VQ2 NN-2N7002DW
VR2 9.1K1%/4
Ib=(5-0.95)/4.7k=0.086mA
Ic=(5-0.2)/22k=0.218mA
VR120 47K/4
VR1 X_22K/4
VR134 22K/4
RT8894_EN 41
RT8894_EN_R
VQ9
RT8894_EN_C
VR3 3K1%/4
VC2 C0.1u16X/4
CPU_1P8
VR25 1K/4
RT8894_EN_R
VC23 C0.1u16X/4
NN-CMKT3904
VR135 47K/4
VC1 C2.2u6.3X/4
12*(3/12.1)=2.975V >1V
Make sure +12VIN connector plug in
Ib=(1.8-0.95)/1k=0.86mA
Ic=(5-0.2)/47k=0.102mA
TYPE0_CPU_SEL: 1:TYPE 0 0:TYPE 2
CPU_VDDP_EN: 0:TYPE 2 1:TYPE 0
Q93 NN-2N7002DW
6,39 TYPE0_CPU_SEL
VDDP_SEL1
5,6,28,39,44 TYPE1_CPU_SEL
VDDP_SEL1
TYPE1_CPU_SEL: 0:TYPE 0 1:TYPE 2
39 CPU_VDDP_PG
VQ1 N-2N7002ET1G

CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

ALL POWER GOOD MUX

2019/4/9
U40.5 is changed to 3VSB from VCC3 by same as X570.

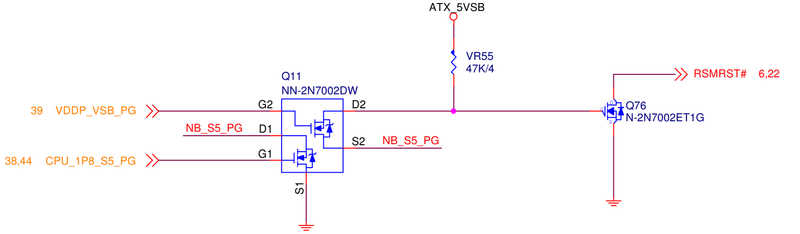


VCC3
VCC3
3VSB
R460 4.7K/4
R461 4.7K/4
3VSB
C411 C0.1u16X/4
checklist1.07
R382 X_8.2K/4
6,7,35,46 SYSREST#
D22 X_S-LRB520S-40T1G
U40
37,38 DDR_PWRGD
D23 X_S-LRB520S-40T1G
ALL_PWR_MUX
ALL_PWR_PWRGD 6
22 CHIP_PWGD
D24 S-LRB520S-40T1G
NC7SZ08M5X
R441 100K/4
41 VRM_VRDY
D25 S-LRB520S-40T1G
16,35 PM_PWRGD
D26 S-LRB520S-40T1G
7 ALL_PWR_MUX
To SPI POK_CTRL# use.

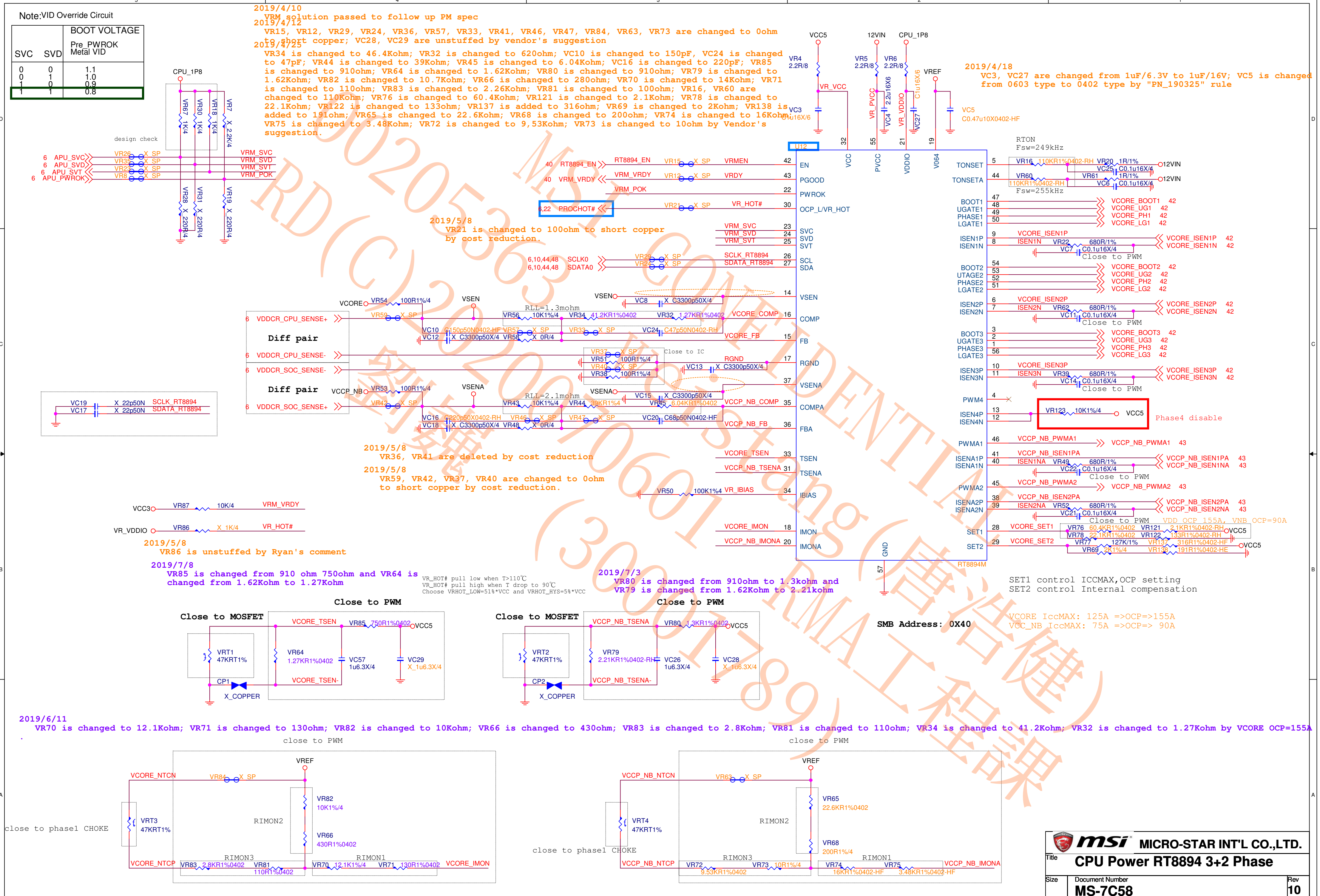
When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

S0 PG

S5 PG



2019/5/20
Q11.G2 and Q11.G1 are swapped by Ryan's comment



2019/4/10
VRM solution passed to follow up PM spec

2019/4/12
VR15, VR12, VR29, VR24, VR36, VR57, VR33, VR41, VR46, VR47, VR84, VR63, VR73 are changed to 0ohm to short copper; VC28, VC29 are unstuffed by vendor's suggestion

2019/4/25
VR34 is changed to 46.4Kohm; VR32 is changed to 620ohm; VC10 is changed to 150pF, VC24 is changed to 47pF; VR44 is changed to 39Kohm; VR45 is changed to 6.04Kohm; VC16 is changed to 220pF; VR85 is changed to 910ohm; VR64 is changed to 1.62Kohm; VR80 is changed to 910ohm; VR79 is changed to 1.62Kohm; VR82 is changed to 280ohm; VR70 is changed to 14Kohm; VR71 is changed to 110ohm; VR83 is changed to 2.26Kohm; VR81 is changed to 100ohm; VR16, VR60 are changed to 110Kohm; VR76 is changed to 60.4Kohm; VR121 is changed to 2.1Kohm; VR78 is changed to 22.1Kohm; VR122 is changed to 133ohm; VR137 is added to 316ohm; VR69 is changed to 2Kohm; VR138 is added to 191ohm; VR65 is changed to 22.6Kohm; VR68 is changed to 200ohm; VR74 is changed to 16Kohm; VR75 is changed to 3.48Kohm; VR72 is changed to 9,53Kohm; VR73 is changed to 10ohm by Vendor's suggestion.

2019/4/18
VC3, VC27 are changed from 1uF/6.3V to 1uF/16V; VC5 is changed from 0603 type to 0402 type by "PN_190325" rule

2019/5/8
VR21 is changed to 100ohm to short copper by cost reduction.

2019/5/8
VR36, VR41 are deleted by cost reduction

2019/5/8
VR59, VR42, VR37, VR40 are changed to 0ohm to short copper by cost reduction.

2019/5/8
VR86 is unstuffed by Ryan's comment

2019/7/8
VR85 is changed from 910 ohm 750ohm and VR64 is changed from 1.62Kohm to 1.27Kohm

2019/7/3
VR80 is changed from 910ohm to 1.3kohm and VR79 is changed from 1.62Kohm to 2.21kohm

2019/6/11
VR70 is changed to 12.1Kohm; VR71 is changed to 130ohm; VR82 is changed to 10Kohm; VR66 is changed to 430ohm; VR83 is changed to 2.8Kohm; VR81 is changed to 110ohm; VR34 is changed to 41.2Kohm; VR32 is changed to 1.27Kohm by VCORE OCP=155A

msi	MICRO-STAR INT'L CO.,LTD.
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VCORE 95W TDC:80A EDC:125A
VCORE 65W TDC:65A EDC:95A

2019/4/10
VRM passed to follow up PM spec

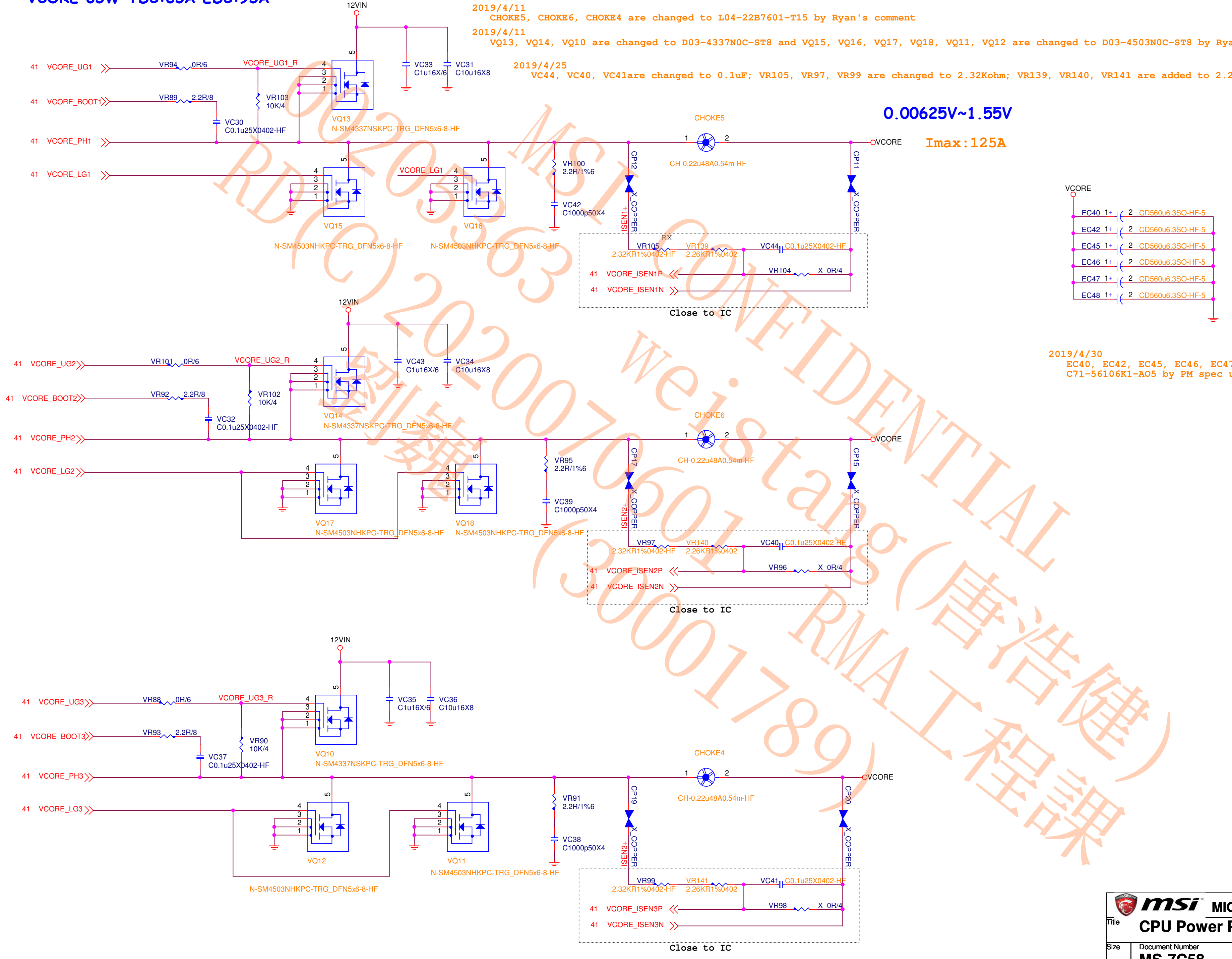
2019/4/11
CHOKE5, CHOKE6, CHOKE4 are changed to L04-22B7601-T15 by Ryan's comment

2019/4/11
VQ13, VQ14, VQ10 are changed to D03-4337N0C-ST8 and VQ15, VQ16, VQ17, VQ18, VQ11, VQ12 are changed to D03-4503N0C-ST8 by Ryan's comment(same as 7A36-3.0)

2019/4/25
VC44, VC40, VC41are changed to 0.1uF; VR105, VR97, VR99 are changed to 2.32Kohm; VR139, VR140, VR141 are added to 2.26Kohm by vendor's suggestion

0.00625V~1.55V

Imax:125A



2019/4/30
EC40, EC42, EC45, EC46, EC47, EC48 are changed to C71-56106K1-AO5 by PM spec updated

msi	MICRO-STAR INT'L CO.,LTD.
Title	CPU Power Phase 1-3
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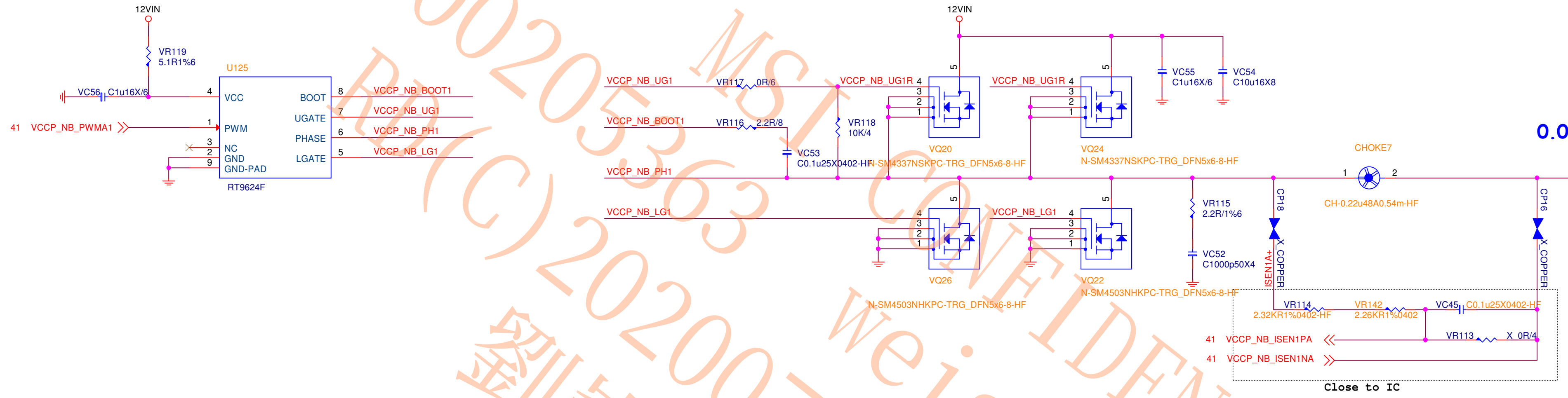
VCCP_NB 95W TDC:50A EDC:75A
VCCP_NB 65W TDC:50A EDC:75A

2019/4/10
VRM passed to follow up PM spec

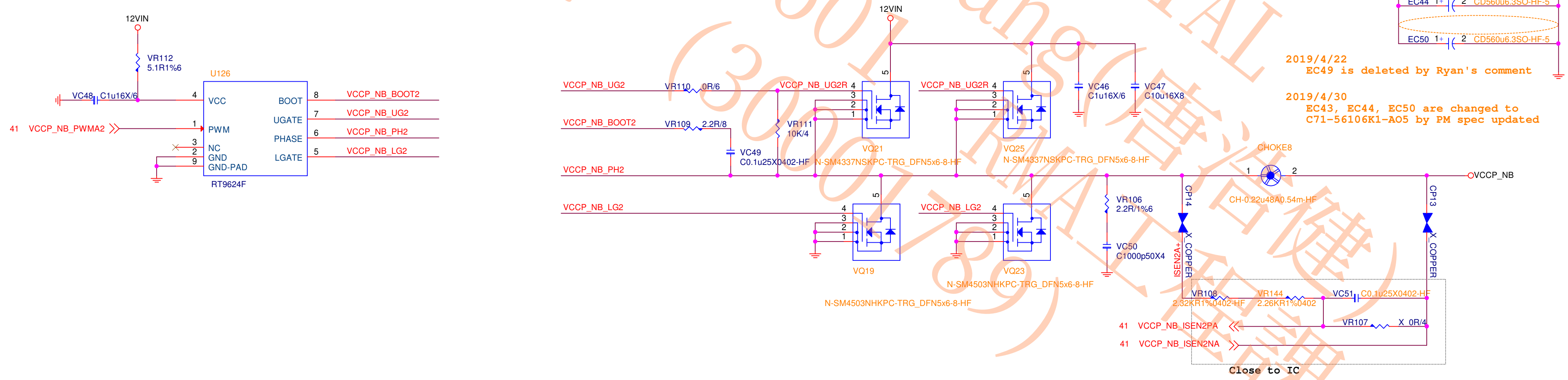
2019/4/11
CHOKE7, CHOKE8 are changed to L04-22B7601-T15 by Ryan's comment

2019/4/11
VQ20, VQ24, VQ21, VQ25 are changed to D03-4337N0C-ST8 and VQ22, VQ26, VQ19, VQ23 are changed to D03-4503N0C-ST8 by Ryan's comment(same as 7A36-3.0)



12VIN
VR119 5.1R1%6
U125
VC56 C1u16X/6
VCC
BOOT
UGATE
PHASE
LGATE
PWM
NC
GND
GND-PAD
RT9624F
41 VCCP_NB_PWMA1
VCCP_NB_BOOT1
VCCP_NB_UG1
VCCP_NB_PH1
VCCP_NB_LG1
VR117 0R/6
VR116 2.2R/8
VR118 10K/4
VC53 C0.1u25X0402-HF
VCCP_NB_UG1R
12VIN
VC55 C1u16X/6
VC54 C10u16X8
VQ20 N-SM4337NSKPC-TRG_DFN5x6-8-HF
VQ24 N-SM4337NSKPC-TRG_DFN5x6-8-HF
VQ26 N-SM4503NHKPC-TRG_DFN5x6-8-HF
VQ22 N-SM4503NHKPC-TRG_DFN5x6-8-HF
VR115 2.2R/1%6
VC52 C1000p50X4
0.00625V~1.55V
Imax:75A
CHOKE7
CH-0.22u48A0.54m-HF
VCCP_NB
CP18
CP16
X_COPPER
ISEN1A+
VR114 2.32KR1%0402-HF
VR142 2.26KR1%0402
VC45 C0.1u25X0402-HF
VR113 X 0R/4
41 VCCP_NB_ISEN1PA
41 VCCP_NB_ISEN1NA
Close to IC

2019/4/25
VC45, VC51 are changed to 0.1uF; VR114, VR108 are changed to 2.32Kohm; VR142, VR144 are added to 2.26Kohm by vendor's suggestion



12VIN
VR112 5.1R1%6
U126
VC48 C1u16X/6
VCC
BOOT
UGATE
PHASE
LGATE
PWM
NC
GND
GND-PAD
RT9624F
41 VCCP_NB_PWMA2
VCCP_NB_BOOT2
VCCP_NB_UG2
VCCP_NB_PH2
VCCP_NB_LG2
VR110 0R/6
VR109 2.2R/8
VR111 10K/4
VC49 C0.1u25X0402-HF
VCCP_NB_UG2R
12VIN
VC46 C1u16X/6
VC47 C10u16X8
VQ21 N-SM4337NSKPC-TRG_DFN5x6-8-HF
VQ25 N-SM4337NSKPC-TRG_DFN5x6-8-HF
VQ19 N-SM4503NHKPC-TRG_DFN5x6-8-HF
VQ23 N-SM4503NHKPC-TRG_DFN5x6-8-HF
VR106 2.2R/1%6
VC50 C1000p50X4
CHOKE8
CH-0.22u48A0.54m-HF
VCCP_NB
CP14
CP13
X_COPPER
ISEN2A+
VR108 2.32KR1%0402-HF
VR144 2.26KR1%0402
VC51 C0.1u25X0402-HF
VR107 X 0R/4
41 VCCP_NB_ISEN2PA
41 VCCP_NB_ISEN2NA
Close to IC
VCCP_NB
EC43 CD560u6.3SO-HF-5
EC44 CD560u6.3SO-HF-5
EC50 CD560u6.3SO-HF-5

2019/4/22
EC49 is deleted by Ryan's comment

2019/4/30
EC43, EC44, EC50 are changed to C71-56106K1-A05 by PM spec updated

MSI MICRO-STAR INT'L CO.,LTD.

Title	CPU Power NB Phase 1-2	
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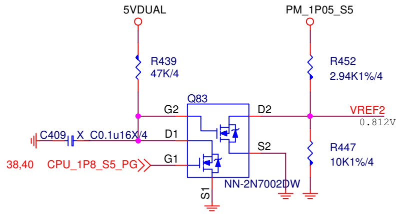
FOR VCCP_SOC_s5
0.9A

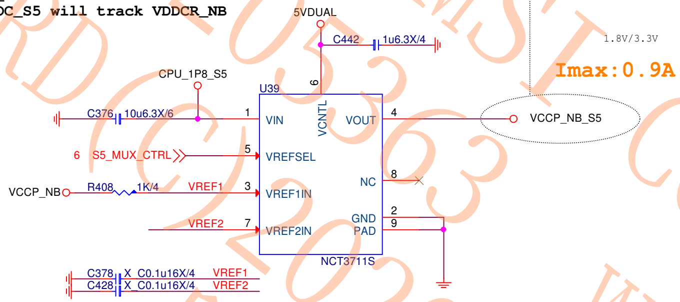
TYPE0 Only

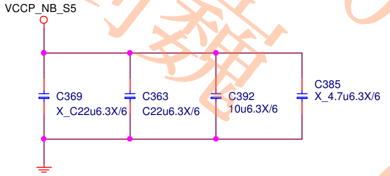
S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

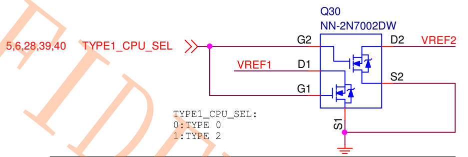
H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors) Bristol Ridge TYPE0









CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VCCP_NB_S5 ONLY SUPPORT TYPE0

Over Voltage Control IC

2019/4/23
U62, R616, R614 are deleted by Ryan's comment

除非超壓對功能有任何幫助,否則不上NCT3933與開超壓選項

2019/4/11
U64, C570, R618, R621 are deleted by Ryan's comment

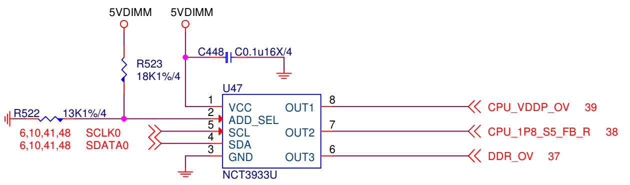
0x26:RH=18K,RL=13K

0x20:RH=10K,RL=OPEN

0x2A:RH=OPEN,RL=10K

UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



MICRO-STAR INT'L CO.,LTD.
Title: CPU Power NB Switch/NCT3933
Size | Document Number: MS-7C58 | Rev 10
Date: Monday, November 11, 2019 | Sheet 44 of 55

uP6273 CURRENT SENSE

20181107
cost down-remove 12VIN OCP

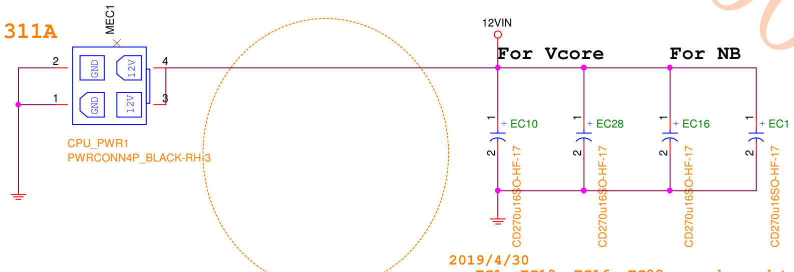
2019/4/11
R1083, R1080, C973, R1079, U101, C914, C915, R1060, C919, C916, R1071, R1072, C917, C918, R1066, R43, Q6, Q12, R61 are deleted by Ryan's comment

VCORE EDC MAC 125A
NB EDC MAX75A

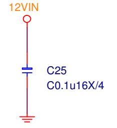
CPU POWER CONNECTOR

2019/4/11
CPU_PWR1 is changed to N93-04M0441-H06 by PM spec.
2019/4/11
CHOKE1, SP1, SP2 are deleted by Ryan's comment

Imax:27.311A



2019/4/30
EC1, EC10, EC16, EC28 are changed to C71-27117Y1-A05 by PM spec updated.



Irms = Iout * SQRT{D/N- (D)^2]}

CORE:
D=Vout/Vin=1.4/12=0.1166
N=Phase number=3
=125A*SQRT(0.0388-0.0136)
=19.8A

NB:
D=Vout/Vin=1.4/12=0.1166
N=Phase number=2
=75A*SQRT(0.0583-0.0136)
=15.8A

D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.5	> output Vcore
D	=	0.125	

I o = Icore(max)*0.8			
I core(max)	=	125	> Vcore current
I avg.	=	100	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	3	phase
I ripple	=	11.02396	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COETEMP	=	1	
Input Cap.	=	3	pcs.

For Vcore

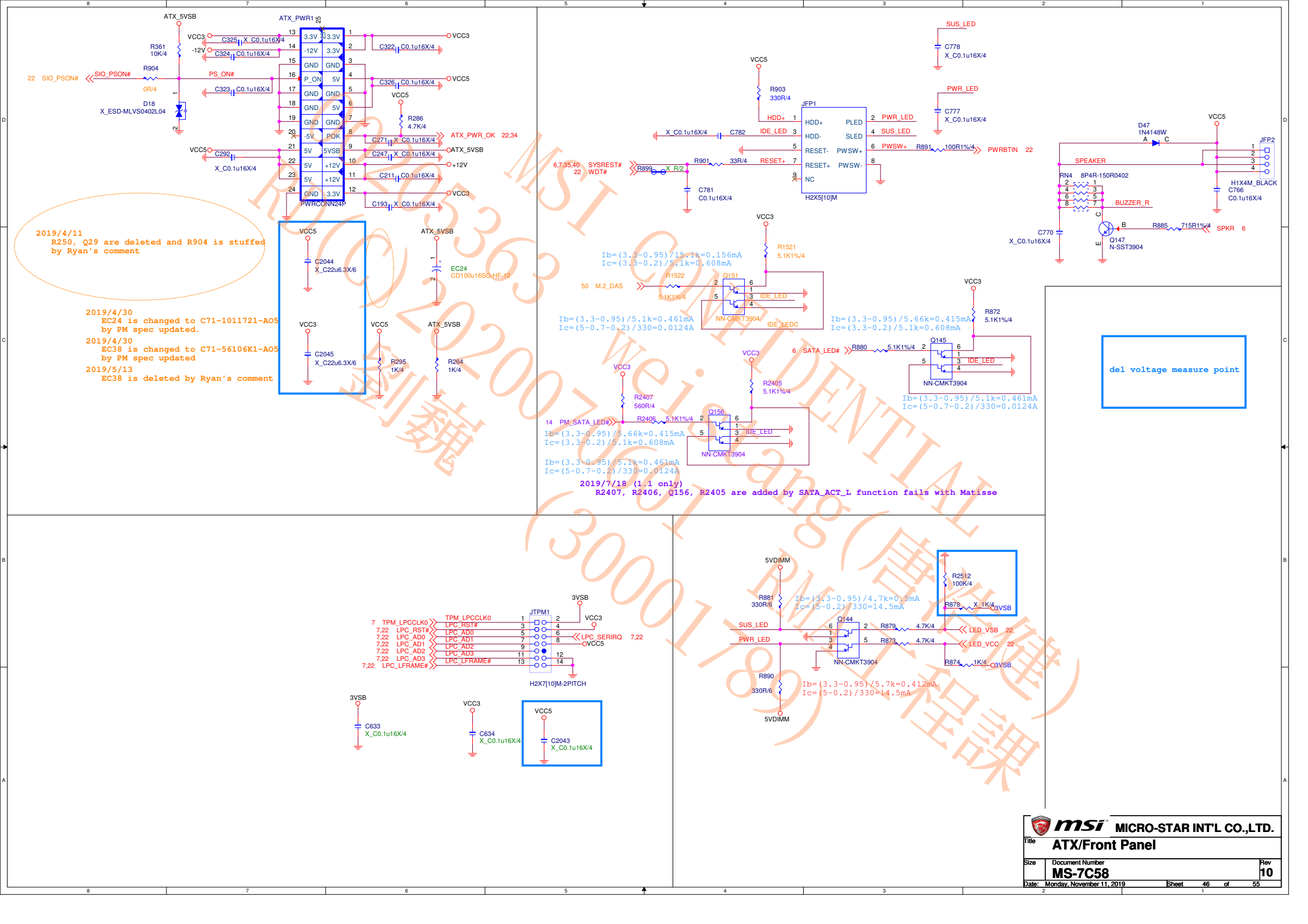
D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.2	> output Vcore
D	=	0.1	

I o = Icore(max)*0.8			
I core(max)	=	75	> Vcore current
I avg.	=	60	A

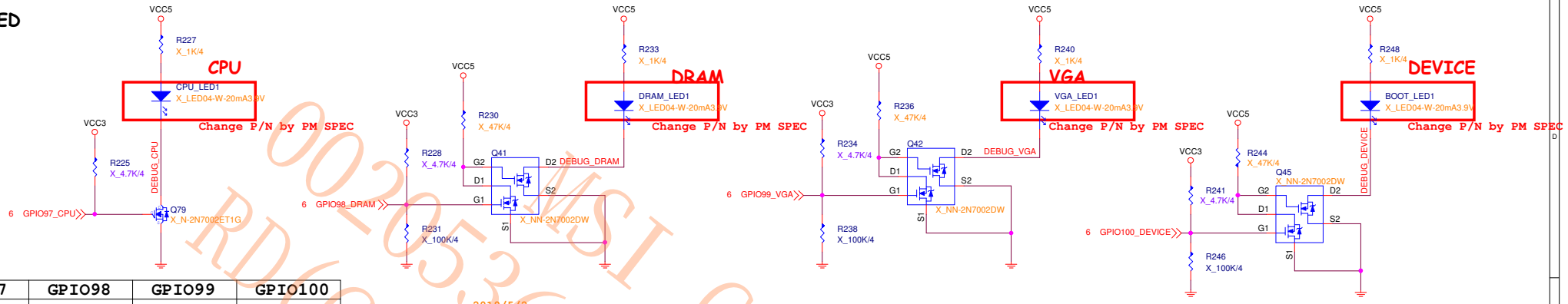
I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	2	phase
I ripple	=	9	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COETEMP	=	1	
Input Cap.	=	2	pcs.

For NB


ATX_PWR1
PWRCONN24P
SIO_PSON#
PS_ON#
ATX_PWR_OK 22,34
ATX_5VSB
+12V
2019/4/11
R250, Q29 are deleted and R904 is stuffed by Ryan's comment
2019/4/30
EC24 is changed to C71-1011721-A05 by PM spec updated.
2019/4/30
EC38 is changed to C71-56106K1-A05 by PM spec updated
2019/5/13
EC38 is deleted by Ryan's comment
JFP1
H2X5[10]M
JFP2
H1X4M_BLACK
SPEAKER
BUZZER_R
SYSREST# 6,7,35,40
WDT# 22
PWRBTIN 22
SUS_LED
PWR_LED
IDE_LED
IDE_LEDC
M.2_DAS 50
SATA_LED# 6
PM_SATA_LED# 14
2019/7/18 (1.1 only)
R2407, R2406, Q156, R2405 are added by SATA_ACT_L function fails with Matisse
del voltage measure point
JTPM1
H2X7[10]M-2PITCH
TPM_LPCCLK0
LPC_RST#
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_LFRAME#
LPC_SERIRQ
5VDIMM
LED_VSB 22
LED_VCC 22
MICRO-STAR INT'L CO.,LTD.
ATX/Front Panel
MS-7C58
Monday, November 11, 2019

EZ Debug LED



LED \ GPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

2019/5/2
R227, CPU_LED1, Q79, R223, DRAM_LED1, Q41, R230, R240, VGA_LED1, Q42, R236, R248, BOOT_LED1, Q45, R244 are unstuffed by PM spec updated.

2019/6/21
R225, R228, R234, R241 are unstuffed by PM request

LED Control by SIO

1.0 SPEC Removed

DDR LED

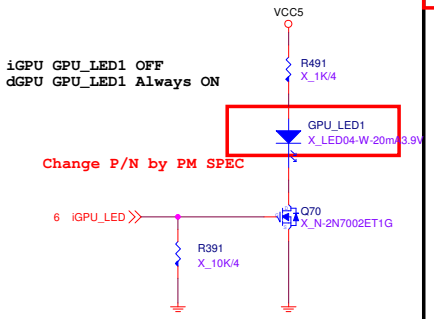
Removed P/N by PM SPEC

PCI Express LED Control

Removed P/N by PM SPEC

2019/6/21
R491, GPU_LED1, Q70, R391 are unstuffed by PM request

AM4 APU Detect LED Circuit



Bottom LED

Removed P/N by PM SPEC

LED	x16	x8	x4
PCIE2	Red	White	White

LED \ GPIO	EGPIO95	EGPIO96
亮	GPO PO HIGH	GPO PO HIGH
滅	GPI (default LOW)	GPI (default LOW)

MICRO-STAR INT'L CO.,LTD.

Title: ALL LED Control

Size: | Document Number: MS-7C58 | Rev: 10

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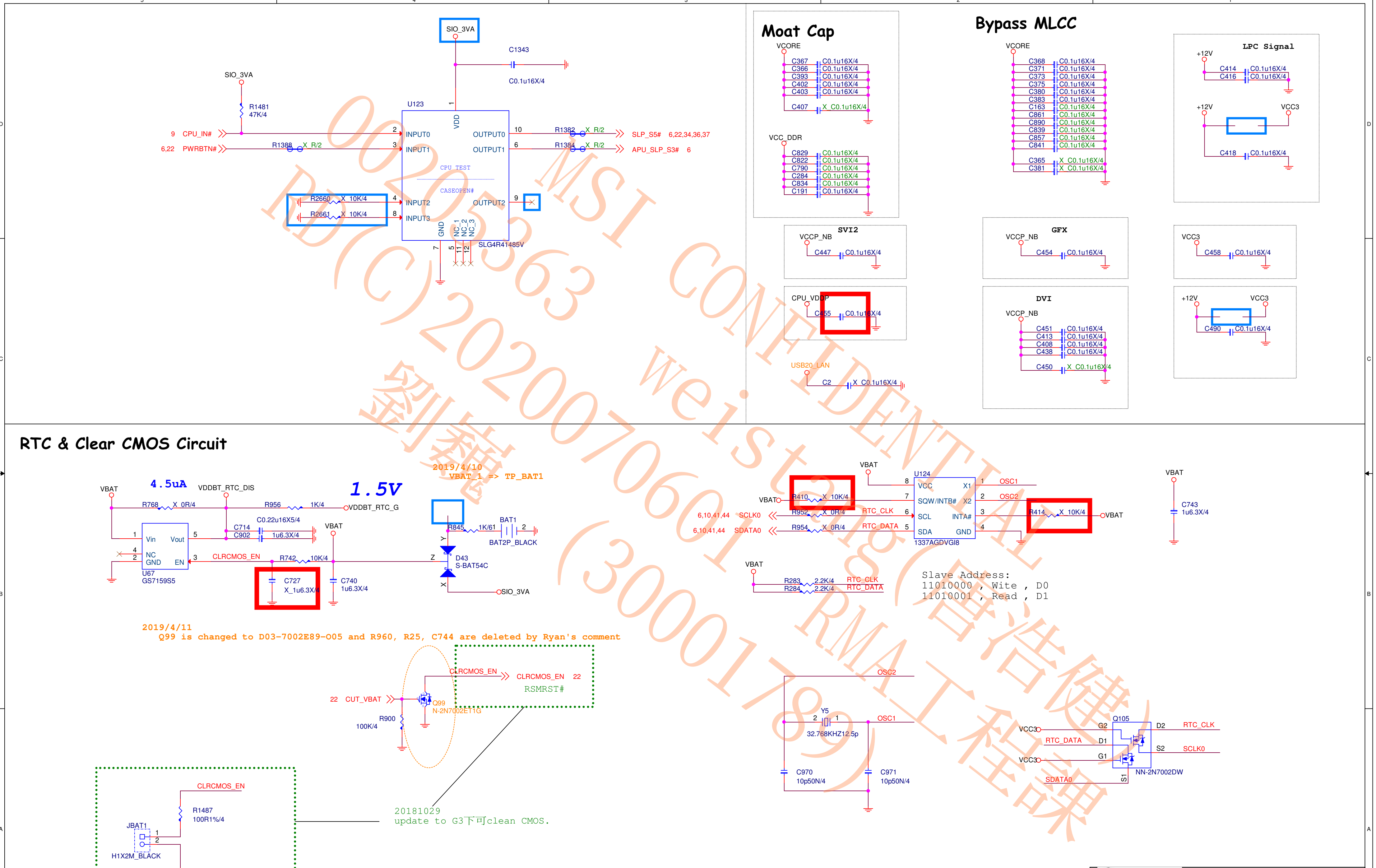
Moat Cap
Bypass MLCC
LPC Signal
SVI2
GFX
DVI
RTC & Clear CMOS Circuit
U123
SLG4R41485V
SIO_3VA
CPU_IN#
PWRBTN#
SLP_S5#
APU_SLP_S3#
4.5uA
1.5V
VDDBT_RTC_DIS
VDDBT_RTC_G
U67
GS7159S5
CLRCMOS_EN
BAT1
BAT2P_BLACK
D43
S-BAT54C
2019/4/10
VBAT_1 => TP_BAT1
2019/4/11
Q99 is changed to D03-7002E89-005 and R960, R25, C744 are deleted by Ryan's comment
U124
1337AGDVGI8
Slave Address:
11010000 , Wite , D0
11010001 , Read , D1
Q99
N-2N7002ETIG
CUT_VBAT
RSMRST#
Y5
32.768KHZ12.5p
Q105
NN-2N7002DW
JBAT1
H1X2M_BLACK
R1487
100R1%/4
20181029
update to G3下可clean CMOS.

MICRO-STAR INT'L CO.,LTD.

Title: RTC Circuit / Moat Cap

Document Number: MS-7C58 | Rev 10

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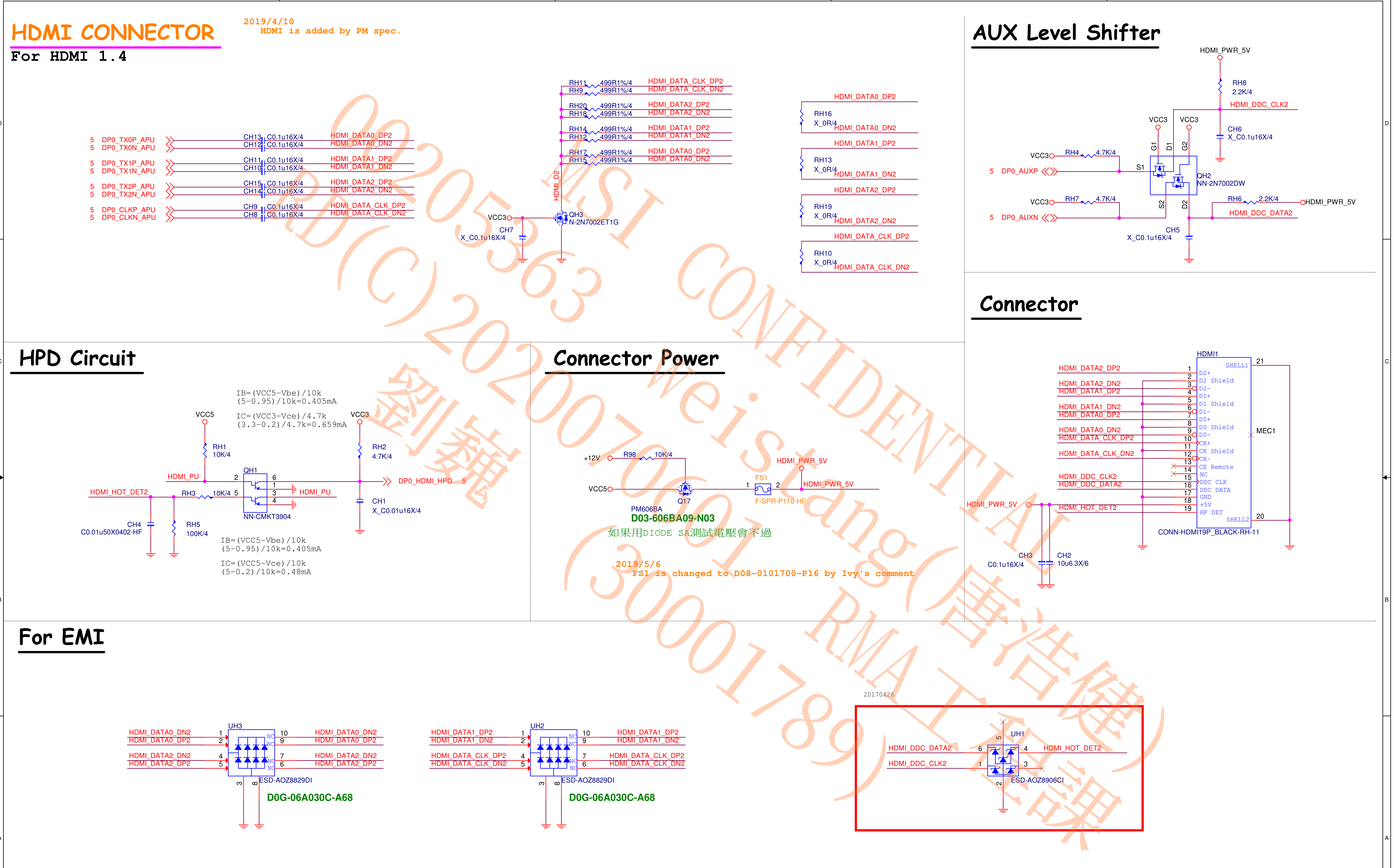

HDMI CONNECTOR
For HDMI 1.4
2019/4/10
HDMI is added by PM spec.
AUX Level Shifter
HDMI_PWR_5V
RH8
2.2K/4
HDMI_DDC_CLK2
VCC3
CH6
X_C0.1u16X/4
RH4 4.7K/4
5 DP0_AUXP
QH2
NN-2N7002DW
RH7 4.7K/4
5 DP0_AUXN
RH6 2.2K/4
HDMI_DDC_DATA2
CH5
X_C0.1u16X/4
5 DP0_TX0P_APU
5 DP0_TX0N_APU
5 DP0_TX1P_APU
5 DP0_TX1N_APU
5 DP0_TX2P_APU
5 DP0_TX2N_APU
5 DP0_CLKP_APU
5 DP0_CLKN_APU
CH13 C0.1u16X/4
CH12 C0.1u16X/4
CH11 C0.1u16X/4
CH10 C0.1u16X/4
CH15 C0.1u16X/4
CH14 C0.1u16X/4
CH9 C0.1u16X/4
CH8 C0.1u16X/4
HDMI_DATA0_DP2
HDMI_DATA0_DN2
HDMI_DATA1_DP2
HDMI_DATA1_DN2
HDMI_DATA2_DP2
HDMI_DATA2_DN2
HDMI_DATA_CLK_DP2
HDMI_DATA_CLK_DN2
RH11 499R1%/4
RH9 499R1%/4
RH20 499R1%/4
RH18 499R1%/4
RH14 499R1%/4
RH12 499R1%/4
RH17 499R1%/4
RH15 499R1%/4
HDMI_D2
VCC3
QH3
N-2N7002ET1G
CH7
X_C0.1u16X/4
RH16 X_0R/4
RH13 X_0R/4
RH19 X_0R/4
RH10 X_0R/4
Connector
HDMI1
SHELL1
D2+
D2 Shield
D2-
D1+
D1 Shield
D1-
D0+
D0 Shield
D0-
CK+
CK Shield
CK-
CE Remote
NC
DDC CLK
DDC DATA
GND
+5V
HP DET
SHELL2
MEC1
HDMI_DDC_CLK2
HDMI_DDC_DATA2
HDMI_PWR_5V
HDMI_HOT_DET2
CH3
C0.1u16X/4
CH2
10u6.3X/6
CONN-HDMI19P_BLACK-RH-11
HPD Circuit
IB=(VCC5-Vbe)/10k
(5-0.95)/10k=0.405mA
IC=(VCC3-Vce)/4.7k
(3.3-0.2)/4.7k=0.659mA
VCC5
RH1
10K/4
VCC3
RH2
4.7K/4
HDMI_PU
QH1
HDMI_HOT_DET2
RH3 10K/4
DP0_HDMI_HPD 5
CH1
X_C0.01u16X/4
NN-CMKT3904
CH4
C0.01u50X0402-HF
RH5
100K/4
IB=(VCC5-Vbe)/10k
(5-0.95)/10k=0.405mA
IC=(VCC5-Vce)/10k
(5-0.2)/10k=0.48mA
Connector Power
+12V
R98 10K/4
HDMI_PWR_5V
VCC5
Q17
FS1
F-SPR-P110-HF
PM606BA
D03-606BA09-N03
如果用DIODE SA測試電壓會不過
2019/5/6
FS1 is changed to D08-0101700-P16 by Ivy's comment
For EMI
UH3
ESD-AOZ8829DI
D0G-06A030C-A68
UH2
ESD-AOZ8829DI
D0G-06A030C-A68
20170426
UH1
ESD-AOZ8906CI

MICRO-STAR INT'L CO.,LTD.

Title: HDMI Connector

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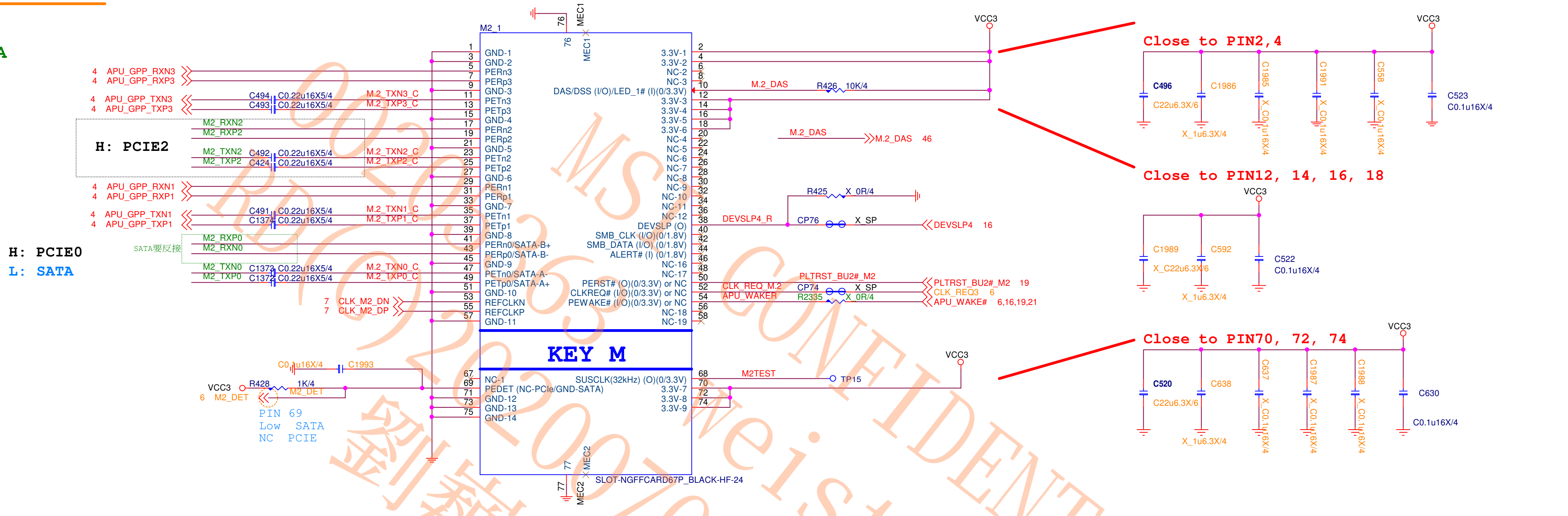
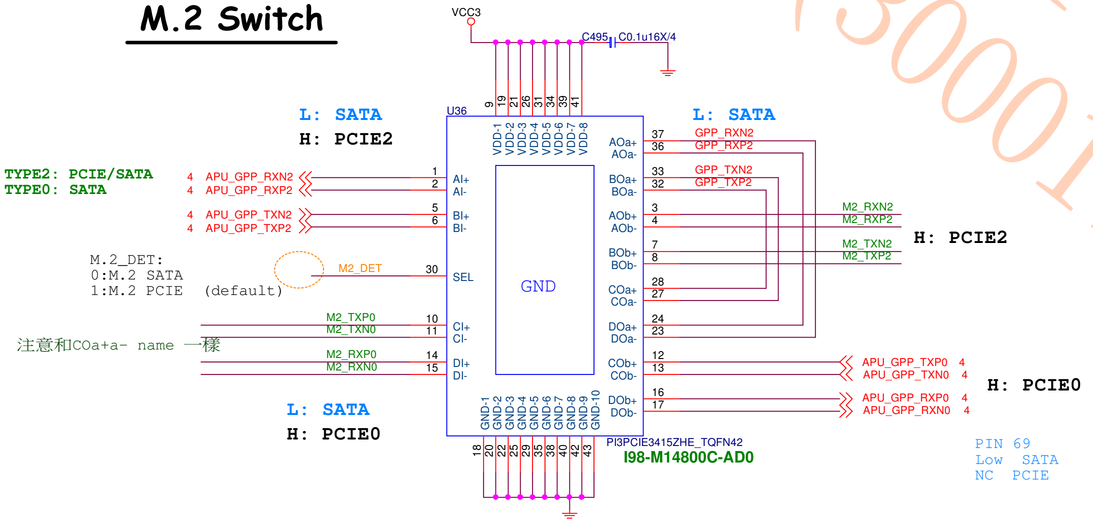
M.2 Connector

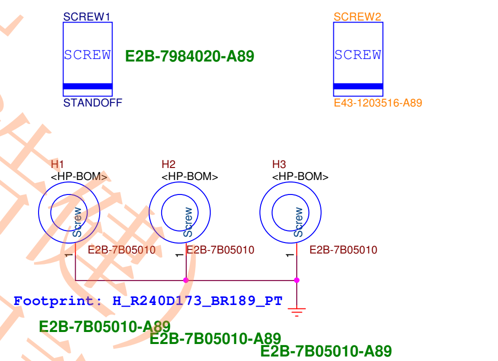
3.3V@2.5A



2019/5/21
SCREW2 is add by PM request

M.2 Switch





MICRO-STAR INT'L CO.,LTD.

Title	M2	
Size	Document Number MS-7C58	Rev 10
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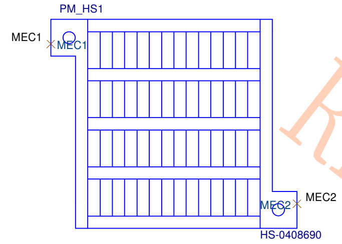
HEAT SINK

2019/7/19 (1.1 MP only)
PM_HS1_Silver 導入 05S/06S 的 MP BOM by PM request

OK



2019/4/30
B450 SKU is added by PM spec updated

CPU Socket

CPU2
E95-0000022-A91
E95-0000022-A91

Simulation

X_JS3
SIM1
X_PIN1*2
X_JS4
SIM2
X_PIN1*2

2019/5/8
SPI_32 is added by PM spec updated

SPI_32
X_MX25U25673GZ4I40
M31-2567300-M24
AVL:M31-2525620-W03

2019/5/8
DVI1 is added by PM spec updated

MANUAL PART

OK
UEFI1
G51-M1SPXXA-A09

BAT1_X1
BAT-BCR2032P

2019/5/21
MKT1, MKT2, MKT3 are modified by PM updated

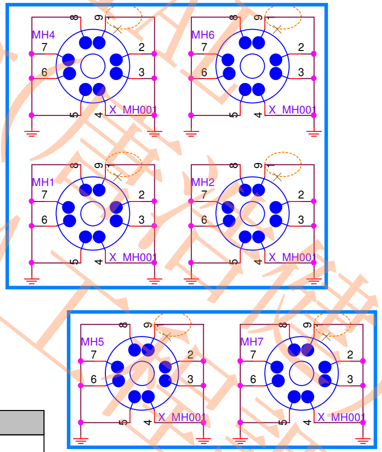
MKT1
A320M PRO-C
G51-M1SPP76-Q13

PCB1

PK0-07C5810-G37
PK0-07C5810-G37, 精成
AVL PK0-07C5810-E48, 競華

2019/4/26
The pin1 of MH4, MH6, MH1, MH2 are changed to GND by CND rule
2019/7/19 (1.1 only)
The pootprint of MH4, MH6, MH1, MH2 are changed from HOLES_4S to Holes_4s_CND by Eric' s comment(2019/7/17)

Optics Orientation Holes



5010

FM3 FM2 FM8 FM6
X_FM120 X_FM120 X_FM120 X_FM120

5020

FM1 FM4 FM7 FM5
X_FM120 X_FM120 X_FM120 X_FM120

OPT	Configure	BOM	Function