Project Name :GK5MP6Y

Platform : CMFL_H+N18E-G0

PAGE CONTENT

M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

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Title: INDEX

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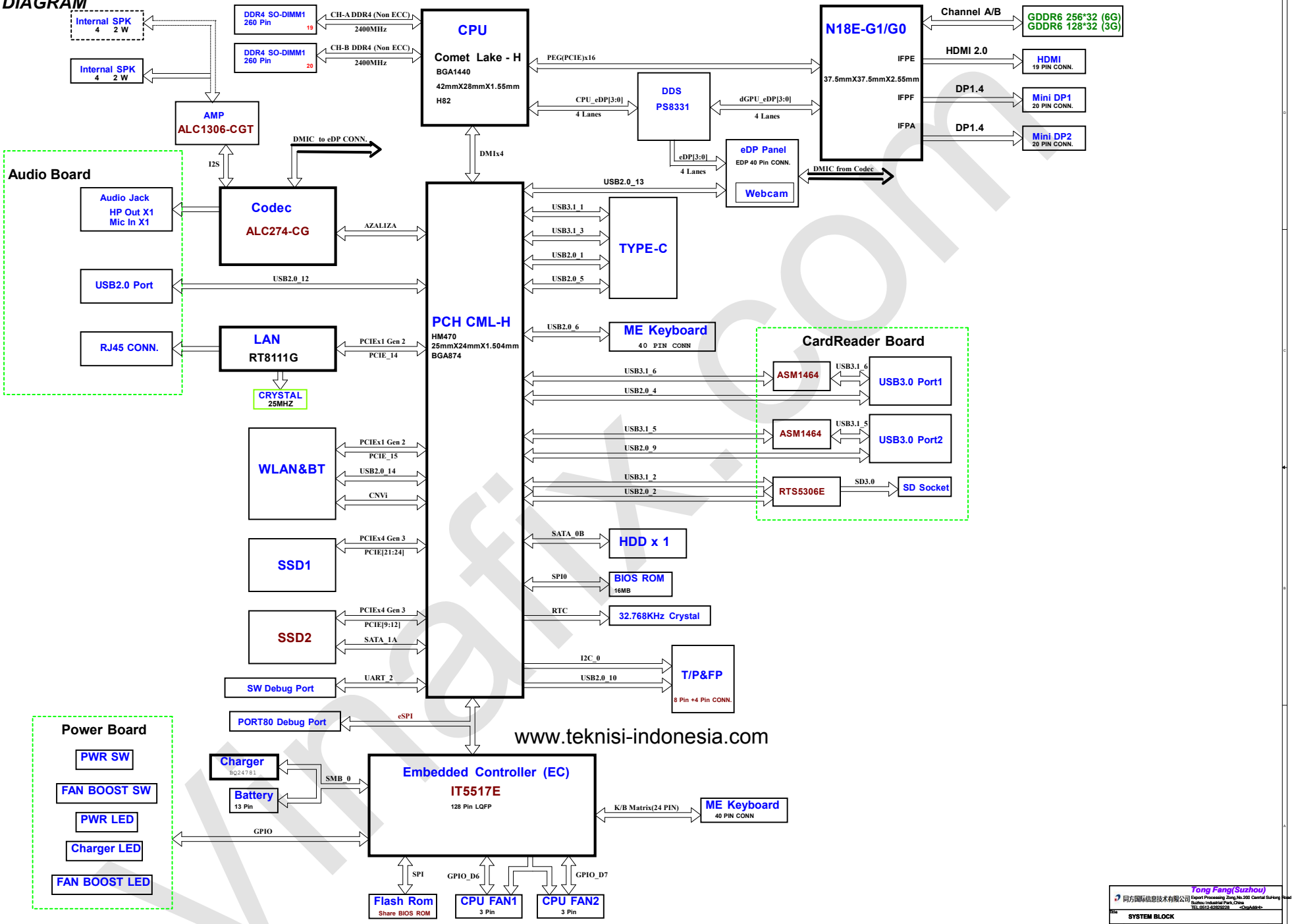
SYSTEM BLOCK DIAGRAM



Title	SYSTEM BLOCK		
Size	Document Number		Rev
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POWER ON SEQUENCE

Title: POWER DIAGRAM & SEQUENCE

Size	Document Number	Rev
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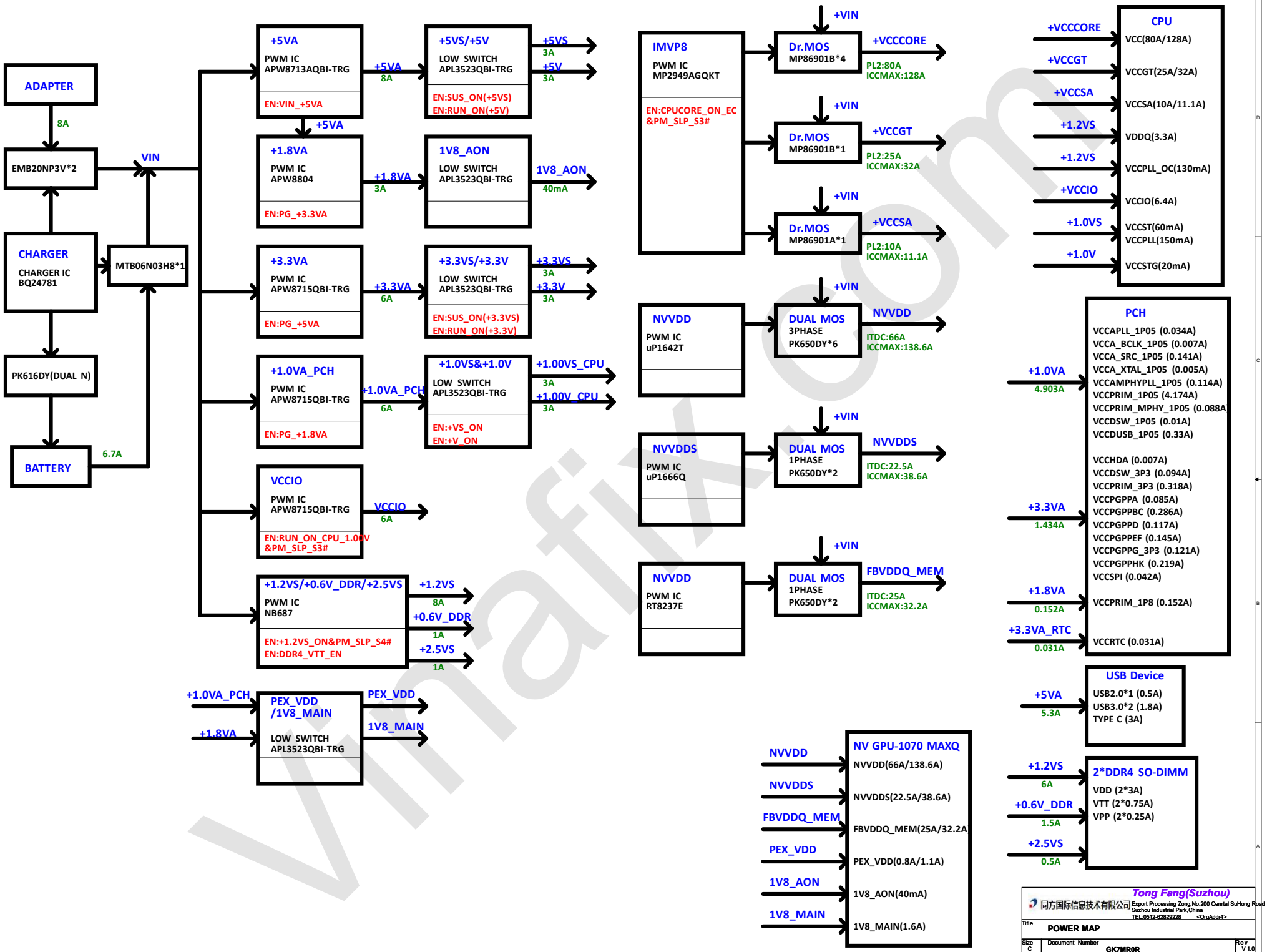

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Title	POWER MAP		
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GPP_F21	PCH_BL_PWM	DEL
GPP_F20	T/P LED_PWM	
GPP_F19	PWM_KB BLUE	
GPA3	PWM_KB RED	
GPA4	PID_1 CHG_R_LED	
GPA5	PID_2 PWR_LED	
GPA6	ME_KB_LED	
GPA7	Board ID	

GH5KN

ITE8528 GPIO		Default Pull/Mode
GPA0	PWM_KB GREEN	UP / GPO
GPA1	T/P LED_PWM	UP / GPO
GPA2	PWM_KB BLUE	UP / GPO
GPA3	PWM_KB RED	UP / GPO
GPA4	PID_1 CHG_R_LED	UP / GPO
GPA5	PID_2 PWR_LED	UP / GPO
GPA6	ME_KB_LED	UP / GPO
GPA7	Board ID	UP / GPO
GPB0	PM_SLP_S4#	UP / GPI
GPB1	PM_SLP_S3#	UP / GPI
GPB2	GPU_Adaptor in	Dn / GPI
GPB3	BAT_SMBCLK	Z / GPI
GPB4	BAT_SMBDAT	Z / GPI
GPB5	H_A20GATE	Z / GPO
GPB6	H_RCIN#	UP / GPI
GPB7	SAFTY_PROTECT	Dn / GPI
GPC0	LAN_PWR	Dn / GPI
GPC1	SMBCLK_EC	Z / GPI
GPC2	SMBDAT_EC	Z / GPI
GPC3	SENBAT_V	Dn / GPO
GPC4	FAN_enable0	Dn / GPO
GPC5	SYS_PWROK	Dn / GPO
GPC6	Boost FAN_EN1	Dn / GPO
GPC7	+2.5VS_ON	UP / GPO
GPD0	ADAP_IN	UP / GPI
GPD1	PWRBTN#	UP / GPO
GPD2	PLT_RST#	UP / GPI
GPD3	HDMI_HPD	UP / GPI
GPD4	EC_EXTSMI#	UP / GPI
GPD5	ME_WE#	UP / GPO
GPD6	FAN0_detect	Dn / GPO
GPD7	FAN1_detect	Dn / GPO
GPE0	LID#	Dn / GPI
GPE1	EG_DA	
GPE2	EG_Cycle start	
GPE3	EG_CLK	
GPE4	PWRSW	UP / GPI
GPE5	LVDS_VIN	Dn / GPO
GPE6	WLAN_ON	Dn / GPO
GPE7	AMP_MUTE#	UP / GPO
GPF0	PANEL_VCC	UP / GPO
GPF1	PCH_PWROK	UP / GPI
GPF2	BT_ON	UP / GPO
GPF3	Q_key1	UP / GPI
GPF4	TP_CLK	UP / GPI
GPF5	TP_DATA	UP / GPI
GPF6	EC_PECI	UP / GPI
GPF7	RUN_ON	UP / GPI
GPG0	PANEL_3.3V_ON	Z/ GPO
GPG1	Reserved for AC remo	Dn/GPO/ID7
GPG2	CPUCORE_ON	Z/ GPO
GPG6	WEBCAM_ON	Z/ GPO
GPH0	PM_CLKRUN#	Dn/GPI/ID0
GPH1	PCH_BL_EN	Dn/GPO/ID1
GPH2	ID_DET	Dn/GPI/ID2
GPH3		Dn/GPI/ID3
GPH4		Dn/GPI/ID4
GPH5	HYB_ON#	Dn/GPI/ID5
GPH6		Dn/GPI/ID6
GPI0	Boost FAN_EN	/GPI/Z
GPI1	PANEL_DETECT	/GPI/Z
GPI2	PCIE_WAKE#	/GPI/Z
GPI3	FAN_enable1	/GPI/Z
GPI4	BAT_I	/GPI/Z
GPI5	BATT_TEMP	/GPI/Z
GPI6	Iadapter_I bat	/GPI/Z
GPI7	BAT_V	/GPI/Z
GPJ0	EC_BL_ON	/GPO/Z
GPJ1	EC_PROCHOT	/GPOI/Z
GPJ2	FAN_CTRL0	/GPO/Z
GPJ3	BATT_VA_OFF#	/GPO/Z
GPJ4	FAN_CTRL1	/GPO/Z
GPJ5	CHG_REF	/GPO/Z
GPM0	LPC_AD0	/GPI/Z
GPM1	LPC_AD1	/GPI/Z
GPM2	LPC_AD2	/GPI/Z
GPM3	LPC_AD3	/GPI/Z
GPM4	CLK_EC_LPC	/GPI/Z
GPM5	LPC_FRAME#	/GPI/Z
GPM6	INT_SERIRQ	/GPI/Z

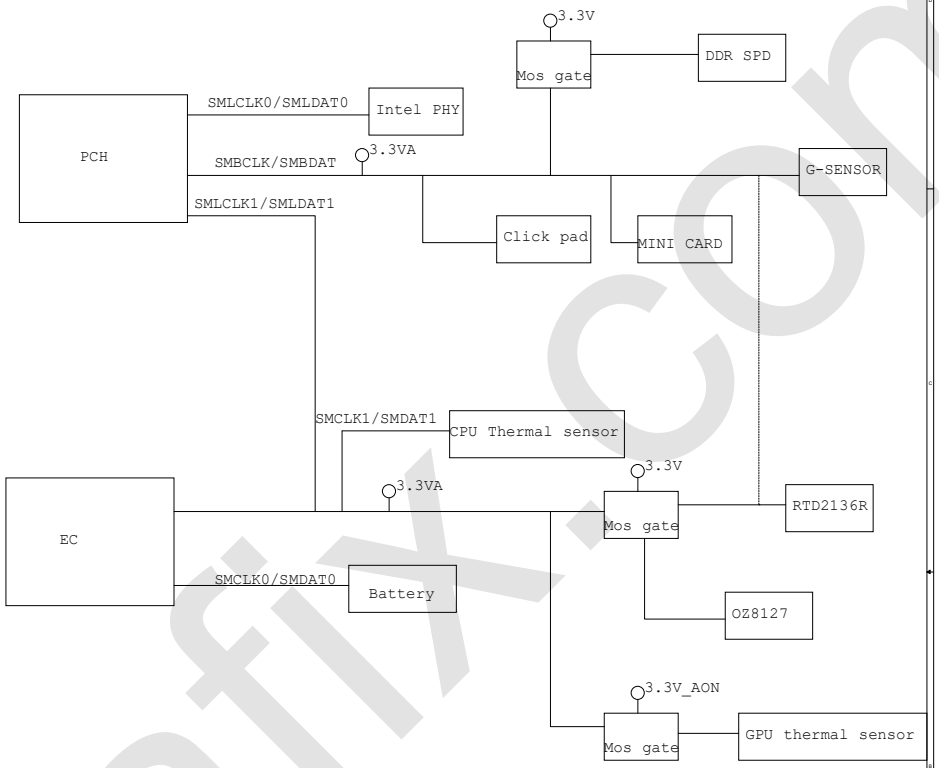
GI5KN

ITE8528 GPIO		Default Pull/Mode
GPA0	PWM_KB GREEN	UP / GPO
GPA1	T/P LED_PWM	UP / GPO
GPA2	PWM_KB BLUE	UP / GPO
GPA3	PWM_KB RED	UP / GPO
GPA4	PID_1 CHG_R_LED	UP / GPO
GPA5	PID_2 PWR_LED	UP / GPO
GPA6	PM_RSMRST#	UP / GPO
GPA7	Board ID	UP / GPO
GPB0	PM_SLP_S4#	UP / GPI
GPB1	PM_SLP_S3#	UP / GPI
GPB2	GPU_Adaptor in	Dn / GPI
GPB3	BAT_SMBCLK	Z / GPI
GPB4	BAT_SMBDAT	Z / GPI
GPB5	H_A20GATE	Z / GPO
GPB6	H_RCIN#	UP / GPI
GPB7	SAFTY_PROTECT	Dn / GPI
GPC0	LAN_PWR	Dn / GPI
GPC1	SMBCLK_EC	Z / GPI
GPC2	SMBDAT_EC	Z / GPI
GPC3	SENBAT_V	Dn / GPO
GPC4	FAN_enable0	Dn / GPO
GPC5	SYS_PWROK	Dn / GPO
GPC6	Boost FAN_EN1	Dn / GPO
GPC7	+2.5VS_ON	UP / GPO
GPD0	ADAP_IN	UP / GPI
GPD1	PWRBTN#	UP / GPO
GPD2	PLT_RST#	UP / GPI
GPD3	HDMI_HPD	UP / GPI
GPD4	EC_EXTSMI#	UP / GPI
GPD5	ME_WE#	UP / GPO
GPD6	FAN0_detect	Dn / GPO
GPD7	FAN1_detect	Dn / GPO
GPE0	LID#	Dn / GPI
GPE1	+1.2VS_ON	Dn / GPI
GPE2	PWR_USB#	Dn / GPO
GPE3	EXT_WIFI_ON	Dn / GPO
GPE4	PWRSW	UP / GPI
GPE5	LVDS_VIN	Dn / GPO
GPE6	WLAN_ON	Dn / GPO
GPE7	AMP_MUTE#	UP / GPO
GPF0	DGPU_EN_EC	UP / GPO
GPF1	PCH_PWROK	UP / GPI
GPF2	BT_ON	UP / GPO
GPF3	Q_key1	UP / GPI
GPF4	TP_CLK	UP / GPI
GPF5	TP_DATA	UP / GPI
GPF6	EC_PECI	UP / GPI
GPF7	RUN_ON	UP / GPI
GPG0	PANEL_3.3V_ON	Z/ GPO
GPG1	Reserved for AC remo	Dn/GPO/ID7
GPG2	CPUCORE_ON	Z/ GPO
GPG6	WEBCAM_ON/SUS_ON	Z/ GPO
GPH0	PM_CLKRUN#	Dn/GPI/ID0
GPH1	PCH_BL_EN	Dn/GPO/ID1
GPH2	ID_DET	Dn/GPI/ID2
GPH3	DGPU_EN_EC_Keep	Dn/GPI/ID3
GPH4	Dgpu_RST_EC#	Dn/GPI/ID4
GPH5	HYB_ON#	Dn/GPI/ID5
GPH6	Clear CMOS	Dn/GPI/ID6
GPI0	Boost FAN_EN	/GPI/Z
GPI1	EC_OVERT_NVVDD#	/GPI/Z
GPI2	PCIE_WAKE#/Dgpu_RST_EC#_keep	/GPI/Z
GPI3	FAN_enable1	/GPI/Z
GPI4	BAT_I	/GPI/Z
GPI5	BATT_TEMP	/GPI/Z
GPI6	Iadapter_I bat	/GPI/Z
GPI7	BAT_V	/GPI/Z
GPJ0	EC_BL_ON	/GPO/Z
GPJ1	EC_PROCHOT	/GPOI/Z
GPJ2	FAN_CTRL0	/GPO/Z
GPJ3	BATT_VA_OFF#	/GPO/Z
GPJ4	FAN_CTRL1	/GPO/Z
GPJ5	CHG_REF	/GPO/Z
GPM0	LPC_AD0	/GPI/Z
GPM1	LPC_AD1	/GPI/Z
GPM2	LPC_AD2	/GPI/Z
GPM3	LPC_AD3	/GPI/Z
GPM4	CLK_EC_LPC	/GPI/Z
GPM5	LPC_FRAME#	/GPI/Z
GPM6	INT_SERIRQ	/GPI/Z

EXT EC

ITE8302 GPIO		Default Pull/Mode
GPIO4	EXT_WIFI_ON	UP / GPO
GPIO5	EC_OVERT_NVVDD#	UP / GPO
GPIO7	Dgpu_RST_EC#_keep	UP / GPO
GPIO9	SUS_ON	UP / GPO
GPIO11	CTL3	UP / GPO
GPIO13	CTL2	UP / GPO
GPIO18	EXT_Q_key0	UP / GPO
GPIO20	EXT_Q_key1	UP / GPO
GPIO22	PWR_USB#	UP / GPI
GPIO24	+1.2VS_ON	UP / GPI
GPIO26	LID1#	Dn / GPI
GPIO27	Dgpu_RST_EC#	Z / GPI
GPIO29	PM_RSMRST#	Z / GPI
GPIO31	DGPU_EN_EC_Keep	Z / GPO
GPIO33	DGPU_EN_EC	UP / GPI
GPIO35	Clear CMOS	Dn / GPI

SMBUS BLOCK



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GPIO & SMBUS Block

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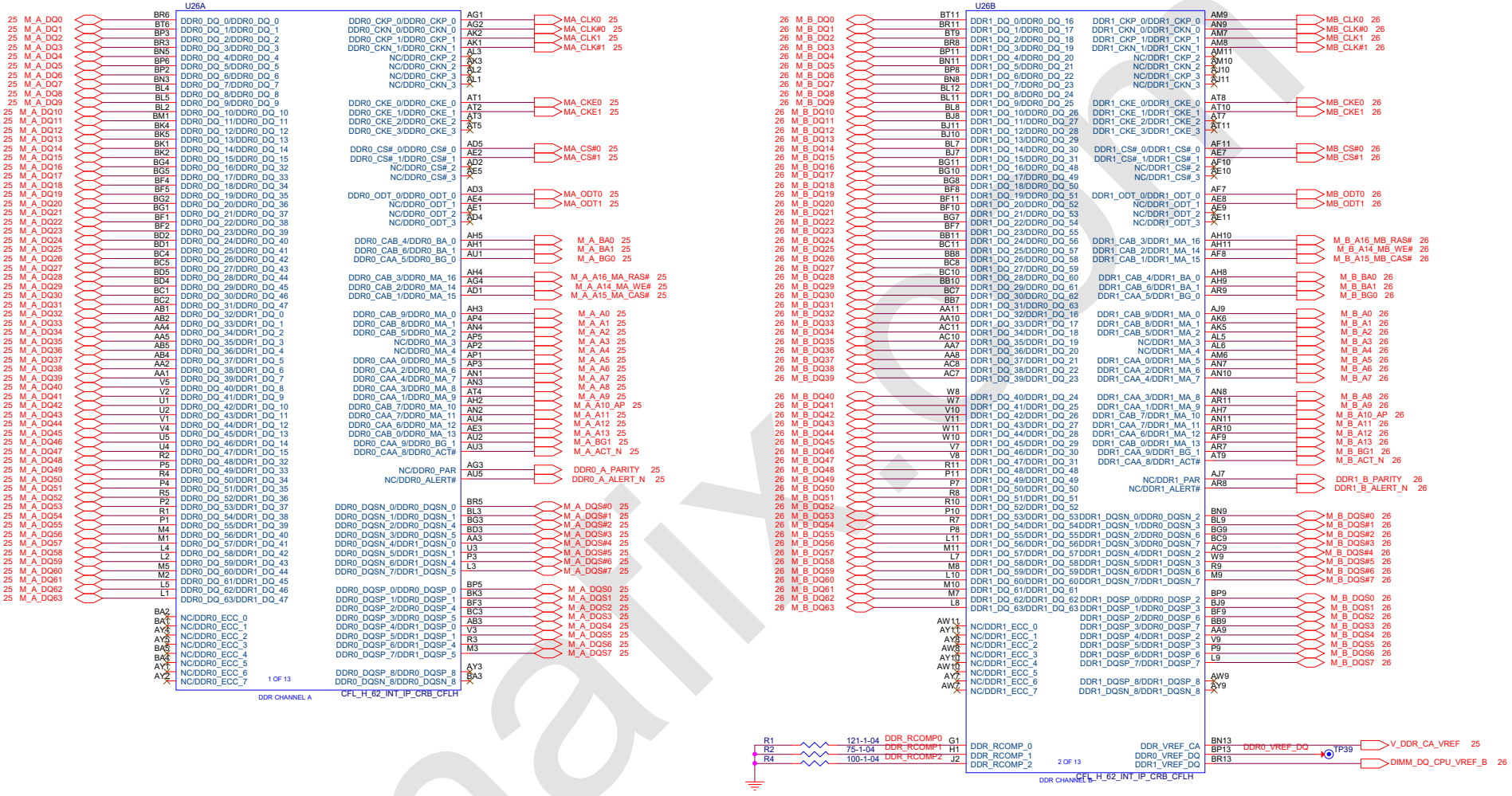

Title: CPU CFL-H : DDR4 CH-A/CH-B

Size	Document Number	Rev
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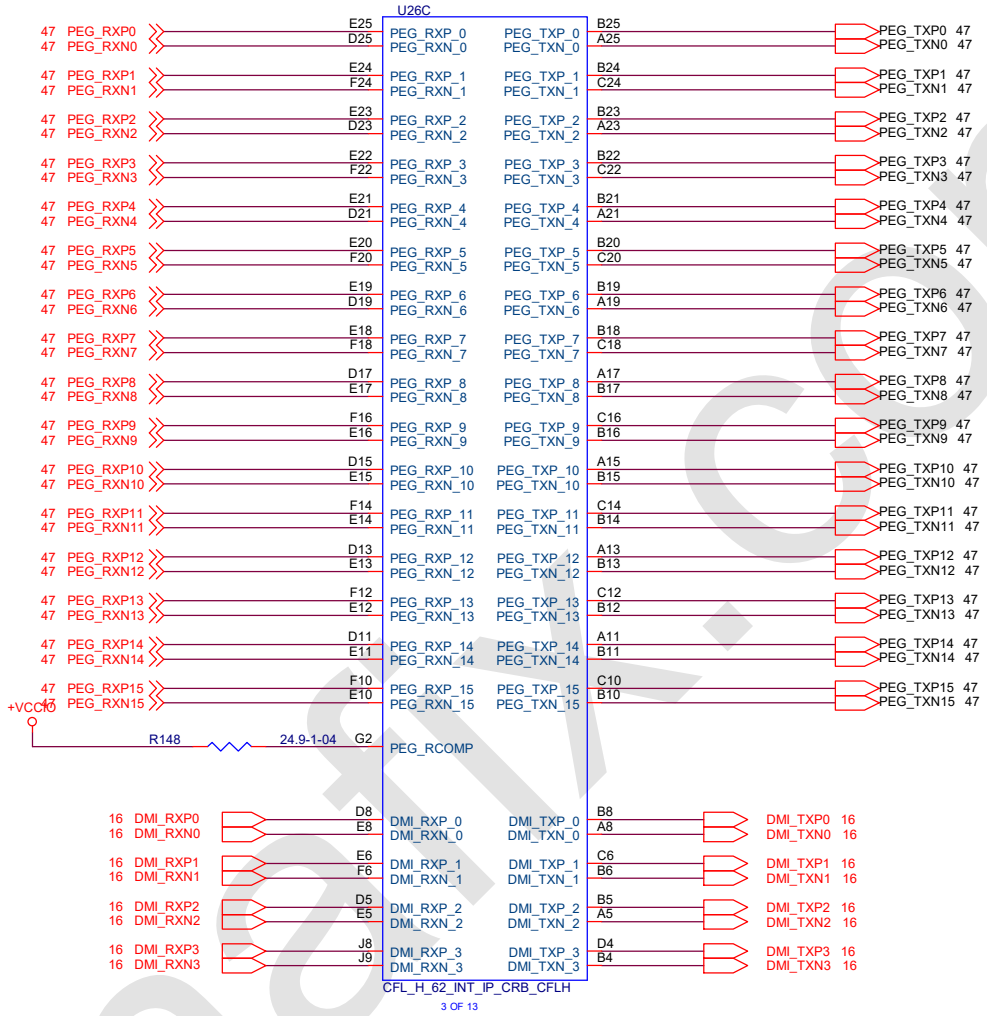

Table 2-13. PCI Express* Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width			CFG Signals			Lanes													
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 Reversed	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2x8 Reversed	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 Reversed	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

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Title	CPU CFL-H : PEG/DMI		
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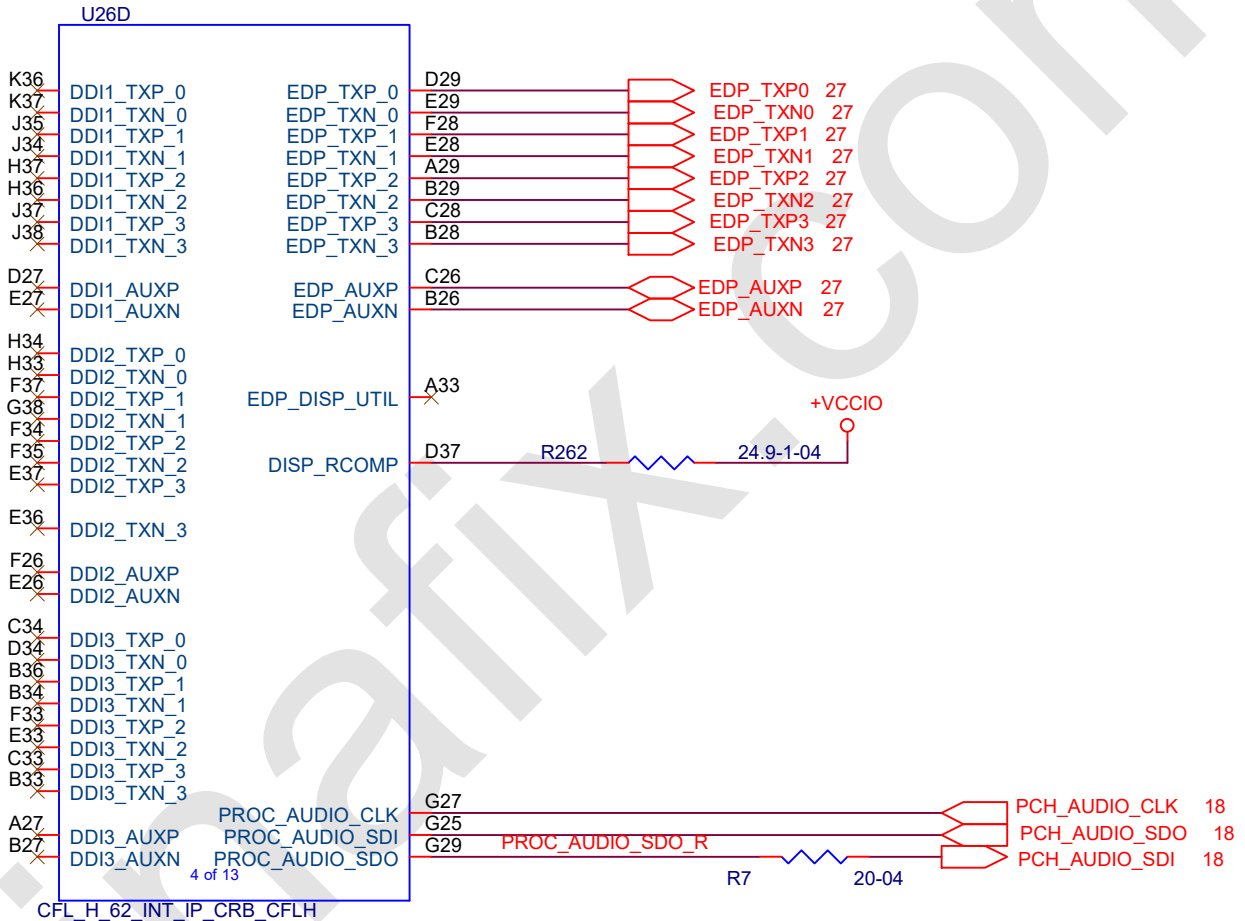

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Title
CPU CFL-H : DDI/EDP

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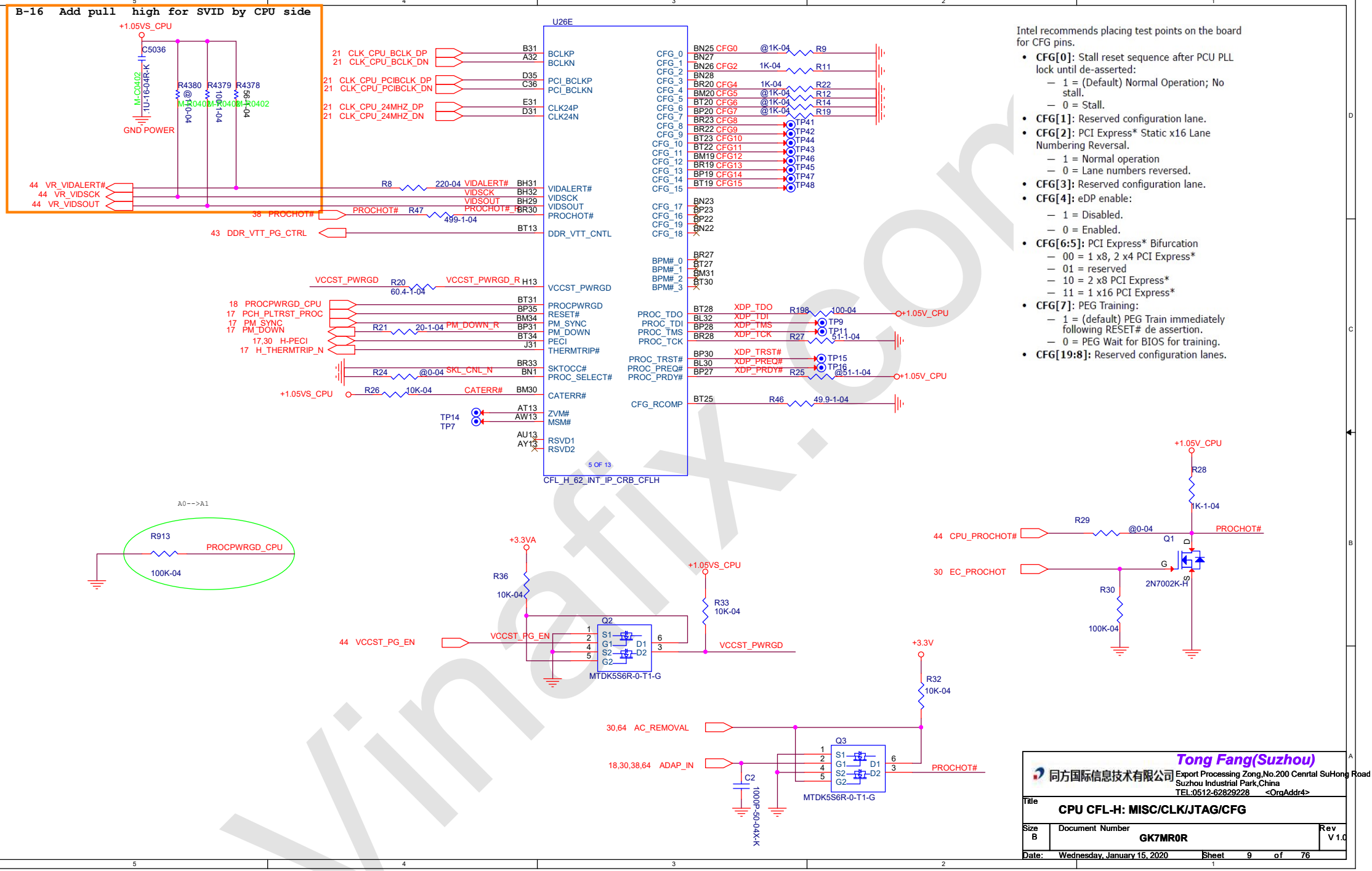
B-16 Add pull high for SVID by CPU side
+1.05VS_CPU
C5036
1U-16-04R-K
M-C0402
R4380 @ 0-0-04
R4379 10-1-04
R4378 56-1-04
M-R0402
GND POWER
U26E
CLK_CPU_BCLK_DP
CLK_CPU_BCLK_DN
CLK_CPU_PCIBCLK_DP
CLK_CPU_PCIBCLK_DN
CLK_CPU_24MHZ_DP
CLK_CPU_24MHZ_DN
BCLKP
BCLKN
PCI_BCLKP
PCI_BCLKN
CLK24P
CLK24N
VR_VIDALERT#
VR_VIDSCK
VR_VIDSOUT
R8 220-04
VIDALERT#
VIDSCK
VIDSOUT
PROCHOT#
R47 499-1-04
DDR_VTT_PG_CTRL
DDR_VTT_CNTL
VCCST_PWRGD
R20 60.4-1-04
VCCST_PWRGD_R
PROCPWRGD_CPU
PCH_PLTRST_PROC
PM_SYNC
PM_DOWN
H-PECI
H_THERMTRIP_N
R21 20-1-04
PM_DOWN_R
PROCPWRGD
RESET#
PECI
THERMTRIP#
R24 @0-04
SKL_CNL_N
SKTOCC#
PROC_SELECT#
R26 10K-04
CATERR#
ZVM#
MSM#
RSVD1
RSVD2
5 OF 13
CFL_H_62_INT_IP_CRB_CFLH
CFG_0
CFG_1
CFG_2
CFG_3
CFG_4
CFG_5
CFG_6
CFG_7
CFG_8
CFG_9
CFG_10
CFG_11
CFG_12
CFG_13
CFG_14
CFG_15
CFG_16
CFG_17
CFG_18
CFG_19
R9 @1K-04
R11 1K-04
R22 1K-04
R12 @1K-04
R14 @1K-04
R19 @1K-04
TP41
TP42
TP44
TP43
TP46
TP45
TP47
TP48
BPM#_0
BPM#_1
BPM#_2
BPM#_3
PROC_TDO
PROC_TDI
PROC_TMS
PROC_TCK
PROC_TRST#
PROC_PREQ#
PROC_PRDY#
XDP_TDO
XDP_TDI
XDP_TMS
XDP_TCK
XDP_TRST#
XDP_PREQ#
XDP_PRDY#
R198 100-04
+1.05V_CPU
TP9
TP11
R27 51-1-04
TP15
TP16
R25 @51-1-04
CFG_RCOMP
R46 49.9-1-04
TP14
TP7
Intel recommends placing test points on the board for CFG pins.
CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted:
1 = (Default) Normal Operation; No stall.
0 = Stall.
CFG[1]: Reserved configuration lane.
CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
1 = Normal operation
0 = Lane numbers reversed.
CFG[3]: Reserved configuration lane.
CFG[4]: eDP enable:
1 = Disabled.
0 = Enabled.
CFG[6:5]: PCI Express* Bifurcation
00 = 1 x8, 2 x4 PCI Express*
01 = reserved
10 = 2 x8 PCI Express*
11 = 1 x16 PCI Express*
CFG[7]: PEG Training:
1 = (default) PEG Train immediately following RESET# de assertion.
0 = PEG Wait for BIOS for training.
CFG[19:8]: Reserved configuration lanes.
A0-->A1
R913
PROCPWRGD_CPU
100K-04
+3.3VA
R36 10K-04
+1.05VS_CPU
R33 10K-04
44 VCCST_PG_EN
VCCST_PG_EN
Q2
MTDK5S6R-0-T1-G
VCCST_PWRGD
+3.3V
R32 10K-04
30,64 AC_REMOVAL
18,30,38,64 ADAP_IN
C2 100P-50-04X-K
Q3
MTDK5S6R-0-T1-G
PROCHOT#
+1.05V_CPU
R28 1K-1-04
R29 @0-04
44 CPU_PROCHOT#
30 EC_PROCHOT
Q1
2N7002K-H
R30 100K-04
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Title
CPU CFL-H: MISC/CLK/JTAG/CFG
Size B
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Title: CPU CFL-H : GND

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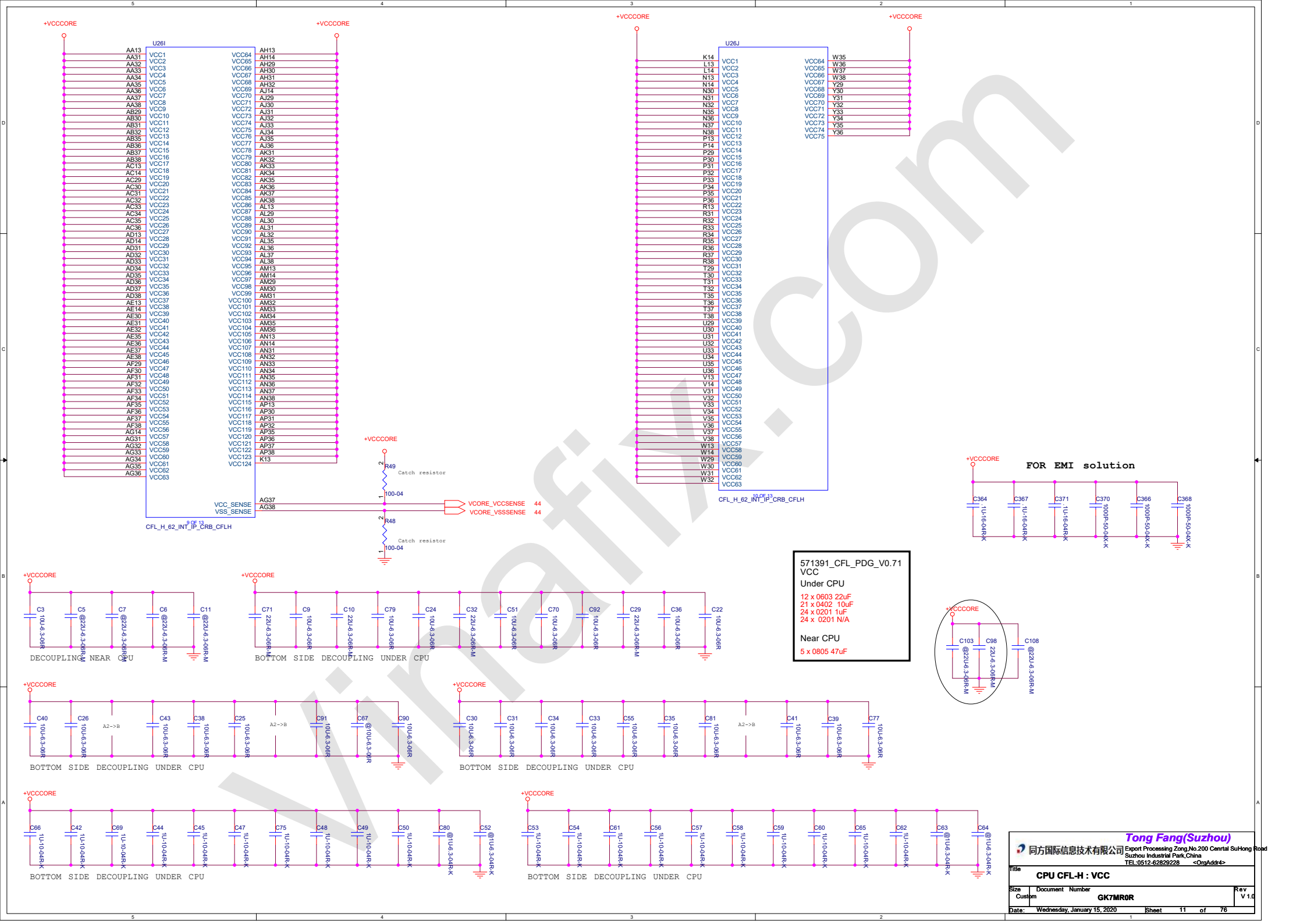
+VCCCORE
U26I
CFL_H_62_INT_IP_CRB_CFLH
9 OF 13
VCC_SENSE
VSS_SENSE
VCORE_VCCSENSE 44
VCORE_VSSSENSE 44
R49
R48
Catch resistor
100-04
U26J
CFL_H_62_INT_IP_CRB_CFLH
10 OF 13
FOR EMI solution
C364 1U-16-04R-K
C367 1U-16-04R-K
C371 1U-16-04R-K
C370 1000P-50-04X-K
C366 1000P-50-04X-K
C368 1000P-50-04X-K
571391_CFL_PDG_V0.71
VCC
Under CPU
12 x 0603 22uF
21 x 0402 10uF
24 x 0201 1uF
24 x 0201 N/A
Near CPU
5 x 0805 47uF
DECOUPLING NEAR CPU
BOTTOM SIDE DECOUPLING UNDER CPU
BOTTOM SIDE DECOUPLING UNDER CPU
BOTTOM SIDE DECOUPLING UNDER CPU
BOTTOM SIDE DECOUPLING UNDER CPU
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Title
CPU CFL-H : VCC
Size Custom
Document Number GK7MR0R
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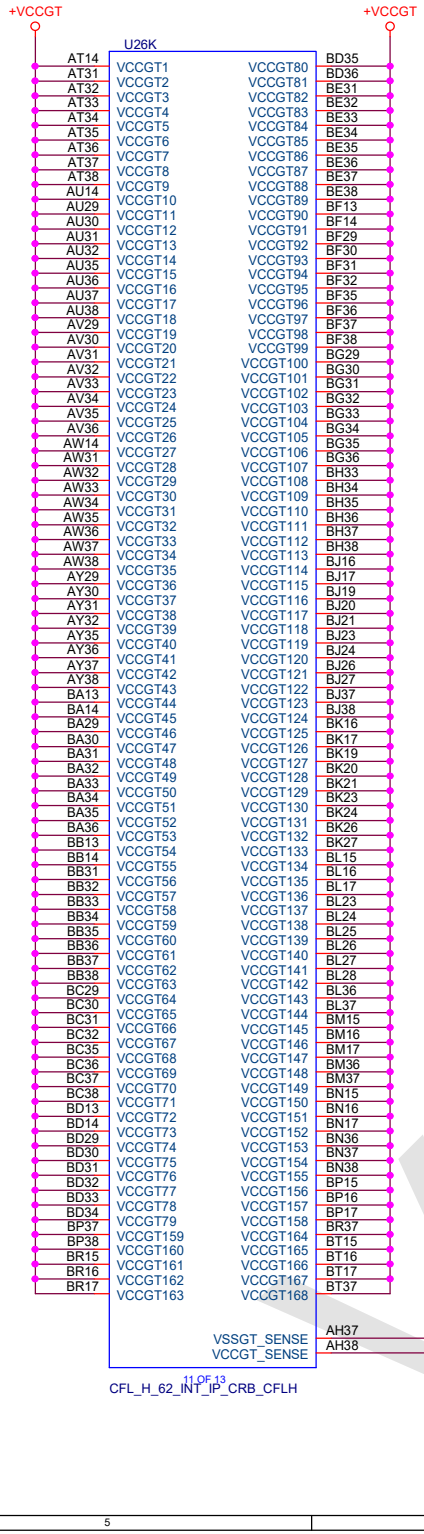
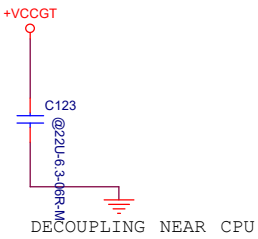
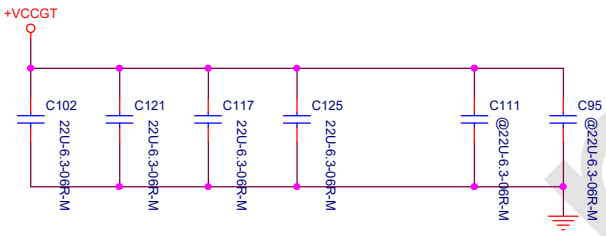
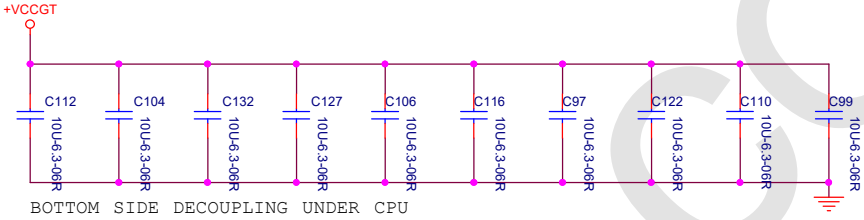


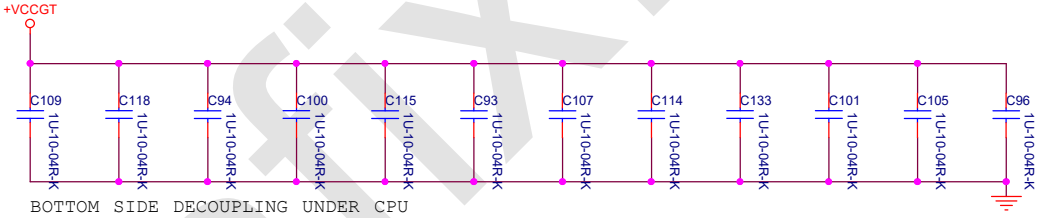




DECOUPLING NEAR CPU

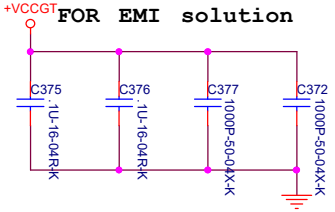


BOTTOM SIDE DECOUPLING UNDER CPU



BOTTOM SIDE DECOUPLING UNDER CPU

571391_CFL_PDG_V0.71
VCCGT
Under CPU
10 x 0402 10uF
12 x 0201 1uF
Near CPU
3 x 0805 47uF
7 x 0603 22uF



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Title	CPU CFL-H : VCCGT	
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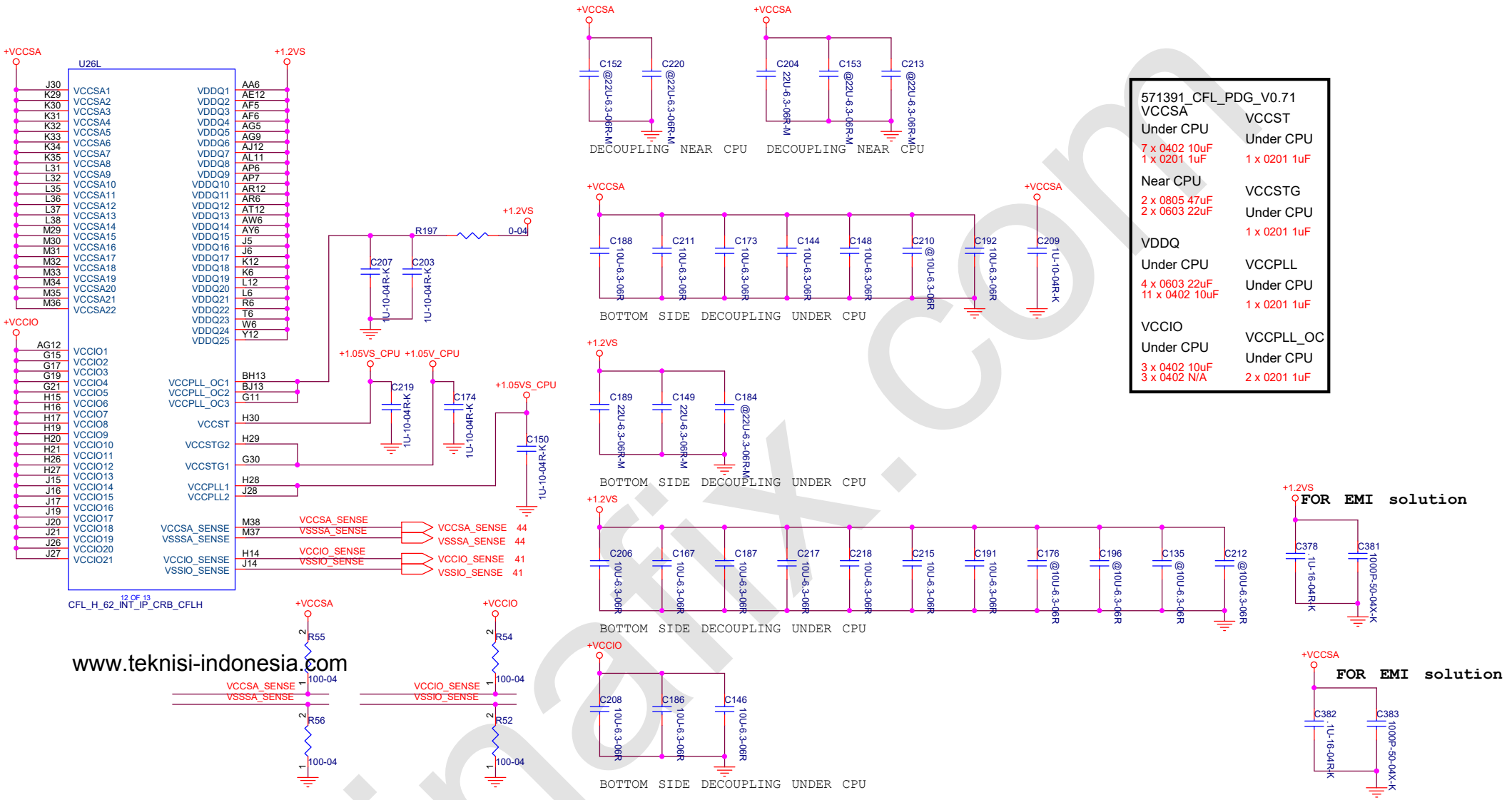
U26L
+VCCSA
+1.2VS
+VCCIO
VCCSA1
VCCSA2
VCCSA3
VCCSA4
VCCSA5
VCCSA6
VCCSA7
VCCSA8
VCCSA9
VCCSA10
VCCSA11
VCCSA12
VCCSA13
VCCSA14
VCCSA15
VCCSA16
VCCSA17
VCCSA18
VCCSA19
VCCSA20
VCCSA21
VCCSA22
VCCIO1
VCCIO2
VCCIO3
VCCIO4
VCCIO5
VCCIO6
VCCIO7
VCCIO8
VCCIO9
VCCIO10
VCCIO11
VCCIO12
VCCIO13
VCCIO14
VCCIO15
VCCIO16
VCCIO17
VCCIO18
VCCIO19
VCCIO20
VCCIO21
VDDQ1
VDDQ2
VDDQ3
VDDQ4
VDDQ5
VDDQ6
VDDQ7
VDDQ8
VDDQ9
VDDQ10
VDDQ11
VDDQ12
VDDQ13
VDDQ14
VDDQ15
VDDQ16
VDDQ17
VDDQ18
VDDQ19
VDDQ20
VDDQ21
VDDQ22
VDDQ23
VDDQ24
VDDQ25
VCCPLL_OC1
VCCPLL_OC2
VCCPLL_OC3
VCCST
VCCSTG2
VCCSTG1
VCCPLL1
VCCPLL2
VCCSA_SENSE
VSSSA_SENSE
VCCIO_SENSE
VSSIO_SENSE
12 OF 13
CFL_H_62_INT_IP_CRB_CFLH
R197
0-04
C207
C203
1U-10-04R-K
+1.05VS_CPU
+1.05V_CPU
C219
C174
C150
VCCSA_SENSE 44
VSSSA_SENSE 44
VCCIO_SENSE 41
VSSIO_SENSE 41
R55
R56
R54
R52
100-04
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C152
C220
C204
C153
C213
@22U-6.3-06R-M
22U-6.3-06R-M
DECOUPLING NEAR CPU
C188
C211
C173
C144
C148
C210
C192
C209
10U-6.3-06R
@10U-6.3-06R
1U-10-04R-K
BOTTOM SIDE DECOUPLING UNDER CPU
C189
C149
C184
22U-6.3-06R-M
@22U-6.3-06R-M
C206
C167
C187
C217
C218
C215
C191
C176
C196
C135
C212
C208
C186
C146
FOR EMI solution
C378
C381
C382
C383
1U-16-04R-K
1000P-50-04X-K
571391_CFL_PDG_V0.71
VCCSA
Under CPU
7 x 0402 10uF
1 x 0201 1uF
Near CPU
2 x 0805 47uF
2 x 0603 22uF
VDDQ
Under CPU
4 x 0603 22uF
11 x 0402 10uF
VCCIO
Under CPU
3 x 0402 10uF
3 x 0402 N/A
VCCST
Under CPU
1 x 0201 1uF
VCCSTG
Under CPU
1 x 0201 1uF
VCCPLL
Under CPU
1 x 0201 1uF
VCCPLL_OC
Under CPU
2 x 0201 1uF
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Title
CPU CFL-H : VCCSA/VCCIO/VDDQ
Size
B
Document Number
GK7MR0R
Rev
V 1.0
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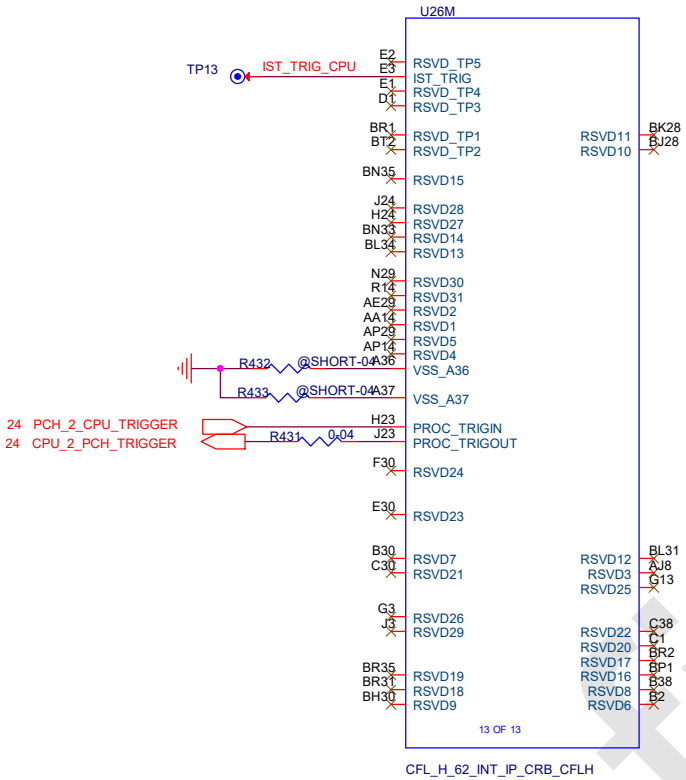
76



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Title: CPU CFL-H : TRIG/RSVD

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BBS_BIT0 - BIOS BOOT STRAP BIT 0

BOOT BIOS STRAP		
BBS_BIT1	BBS_BIT0	BOOT BIOS LOCATION
0	0	LPC
0	1	RESERVED(NAND)
1	0	----
1	1	SPI

U28A

TP18 GPP_A11 BE36 GPP_A11/PME#/SD_VDD2_PWR_EN#

GPP_B13/PLTRST# AV29 → PLT_RST# 32,33,36,47

R67 @1K-1-04

R15 RSVD2
R13 RSVD1

GPP_K16/GSXCLK Y47
GPP_K12/GSXDOUT Y46
GPP_K13/GSXSLOAD Y48
GPP_K14/GSXDIN W46
GPP_K15/GSXSRESET# AA45

+3.3VA

TP24 VSS_AL37 AL37 VSS
AN35 TP

R72 1K-04

PCH_SPI_SI R75 1 2 33-04 PCH_SPI0_SI_R AU41 SPI0_MOSI
PCH_SPI_SO R57 short_0402 2 33-04 PCH_SPI0_SO_R BA45 SPI0_MISO
PCH_SPI_CS#0 R4286 @S0-04 PCH_SPI0_CS#0_R AY47 SPI0_CS0#
PCH_SPI_CLK R71 1 2 33-04 PCH_SPI0_CLK_R AW47 SPI0_CLK
TP19 SPI0_CS1# AW48 SPI0_CS1#

GPP_E3/CPU_GP0 AL47 → EC_EXTSMI# 30
GPP_E7/CPU_GP1 AM45 → TP_INT# 37
GPP_B3/CPU_GP2 BF32
GPP_B4/CPU_GP3 BC33

PCH_SPI_WP R58 1 2 33-04 PCH_SPI0_IO2 AY48 SPI0_IO2
PCH_SPI_HOLD# R74 1 2 33-04 PCH_SPI0_IO3 BA46 SPI0_IO3
TP25 SPI0_CS2# AT40 SPI0_CS2#

GPP_H18/SML4ALERT# AE44
GPP_H17/SML4DATA AJ46
GPP_H16/SML4CLK AE43
GPP_H15/SML3ALERT# AC47 GPP_H15 R73 100K-04 +3.3VA
GPP_H14/SML3DATA AD48
GPP_H13/SML3CLK AF47
GPP_H12/SML2ALERT# AB47 GPP_H12 R76 @4.7K-04 +3.3VA
GPP_H11/SML2DATA AD47
GPP_H10/SML2CLK AE48

GPP_H15 External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

GPP_H12 eSPI Flash Sharing Mode
0:Master Attached Flash Sharing(MAFS) enabled(internal pull down)
1:Slave Attached Flash Sharing(SAFS) enabled

BE19 GPP_D1/SPI1_CLK/SBK1_BK1
BF19 GPP_D0/SPI1_CS#/SBK0_BK0
BF18 GPP_D3/SPI1_MOSI/SBK3_BK3
BE18 GPP_D2/SPI1_MISO/SBK2_BK2
BC17 GPP_D22/SPI1_IO3
BD17 GPP_D21/SPI1_IO2

INTRUDER# BB44 → SM_INTRUDER# 18

1 OF 13
CNP_H_IP_CFL

A-17
Modify

SPI0_MOSI:
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K ifpulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

to eSPI EC

PCH_SPI_CLK → PCH_SPI_CLK 30
PCH_SPI_CS#0 → PCH_SPI_CS#0 30
PCH_SPI_SI → PCH_SPI_SI 30
PCH_SPI_SO → PCH_SPI_SO 30

+3.3VA

R60 1K-04
R59 1K-04

U20

PCH_SPI_CS#0 1 CS#
PCH_SPI_SO 2 SO
PCH_SPI_WP 3 WP/IO2
4 GND
8 VCC
7 HOLD/IO3
6 SCK
5 SI

PCH_SPI_HOLD#
PCH_SPI_CLK
PCH_SPI_SI

W25Q128JVSIQT

C221 4.7U-6.3-06R-K

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Title: PCH CFL-H : SPI

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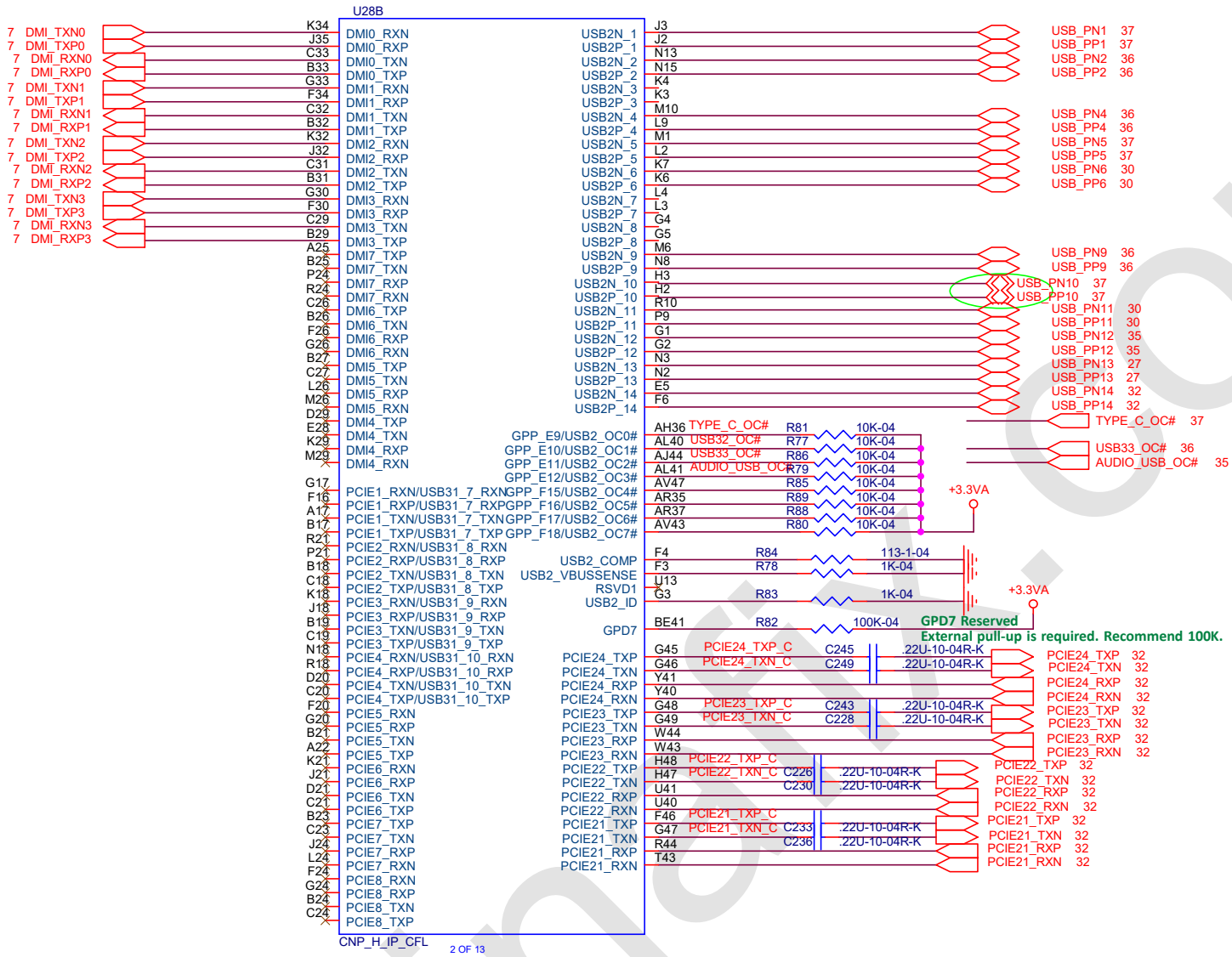

USB2.0 Configuration Table	
USB1	TYPE-C Port
USB2	CardReader on USB3.0 DB
USB3	N/A
USB4	USB3.0 Port1 on USB3.0 DB
USB5	TYPE-C Port
USB6	ME Keyboard CONN
USB7	N/A
USB8	N/A
USB9	USB3.0 Port2 on USB3.0 DB
USB10	N/A
USB11	USB3.0 Port1 on USB3.0 DB
USB12	USB2.0 PORT on Audio DB
USB13	Web Camera
USB14	Bluetooth

USB OC Configuration Table	
OC0	TYPE_C_OC#
OC1	N/A
OC2	USB3.0 DB
OC3	AUDIO_USB DB
OC4	N/A
OC5	N/A
OC6	N/A
OC7	N/A

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Title: PCH CFL-H : DMI/USB2.0

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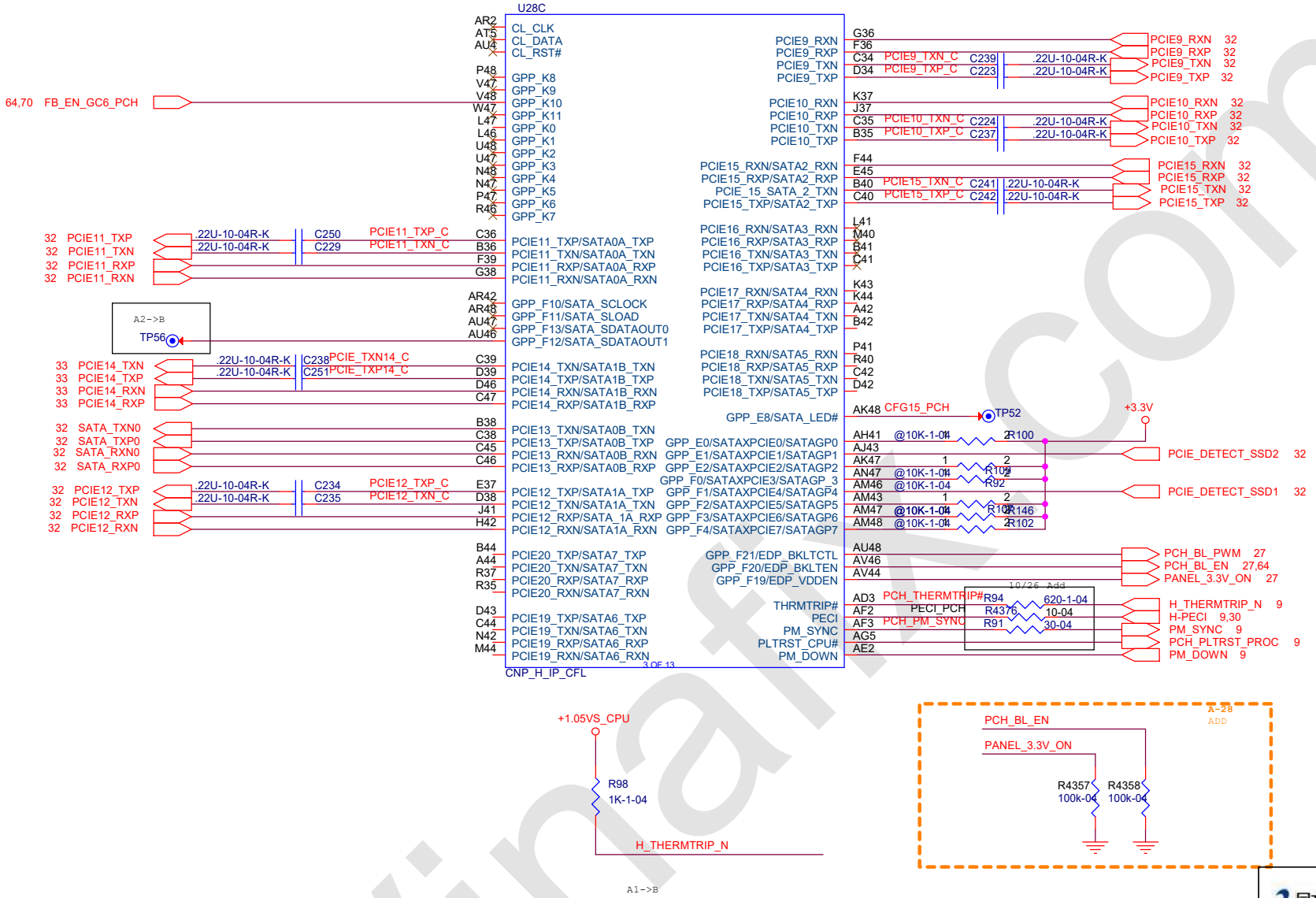

PCIE Configuration Table			
PCIE1	No function	PCIE13	SATA HDD
PCIE2	No function	PCIE14	LAN
PCIE3	No function	PCIE15	WLAN
PCIE4	No function	PCIE16	N/A
PCIE5	N/A	PCIE17	PCIE SSD1
PCIE6	N/A	PCIE18	PCIE SSD1
PCIE7	No function	PCIE19	PCIE SSD1
PCIE8	No function	PCIE20	PCIE SSD1
PCIE9	PCIE SSD2	PCIE21	N/A
PCIE10	PCIE SSD2	PCIE22	N/A
PCIE11	PCIE SSD2	PCIE23	N/A
PCIE12	PCIE SSD2	PCIE24	N/A

SATA Configuration Table	
SATA0	SATA HDD
SATA1	SATA SSD2
SATA2	No Function
SATA3	No Function
SATA4	SATA SSD1
SATA5	N/A
SATA6	No Function
SATA7	No Function

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Title: PCH CFL-H : SATA/PCIE

Size: Custom | Document Number: GK7MR0R | Rev: V 1.0

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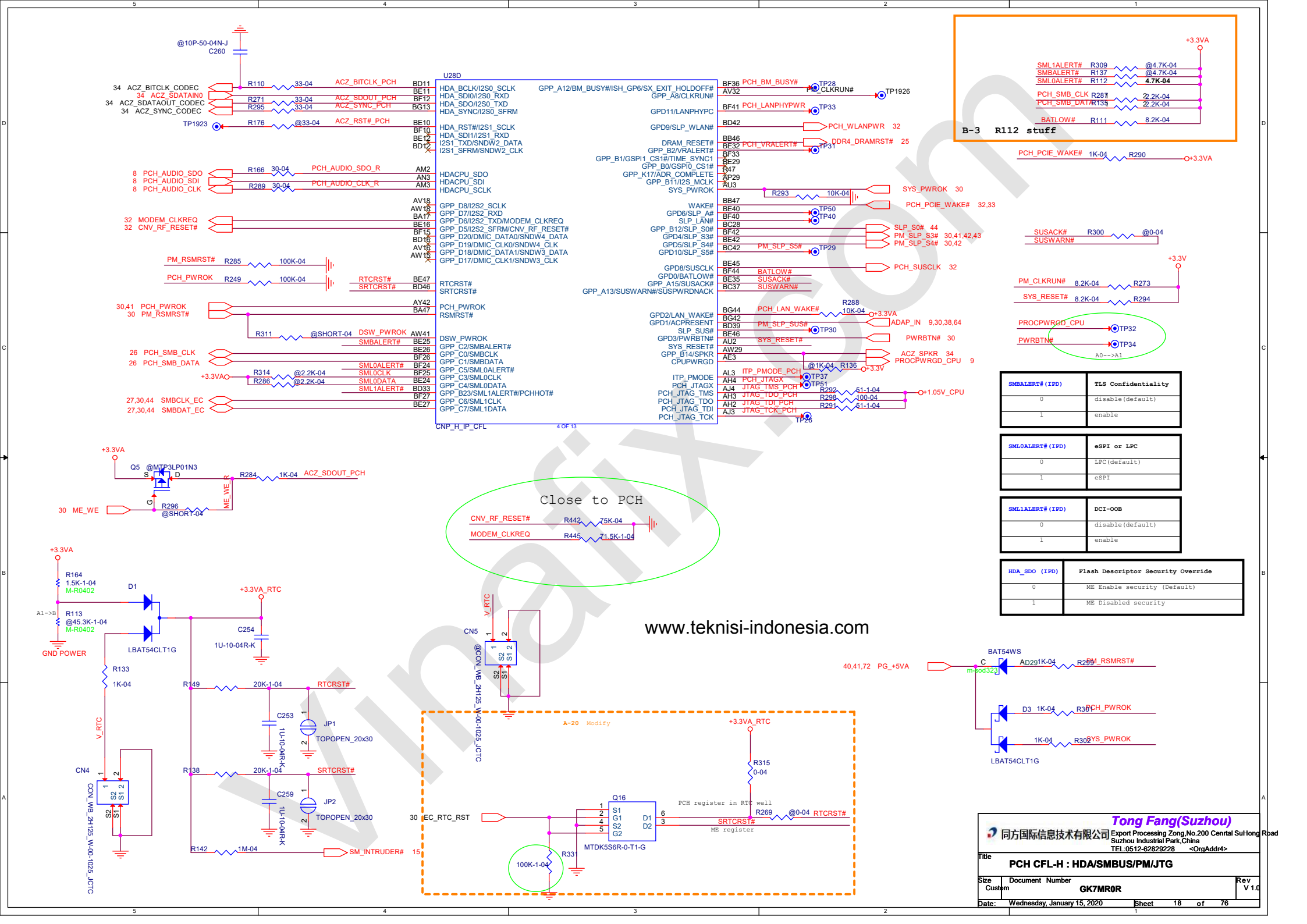
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CNP_H_IP_CFL
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PCH CFL-H : HDA/SMBUS/PM/JTG
GK7MR0R
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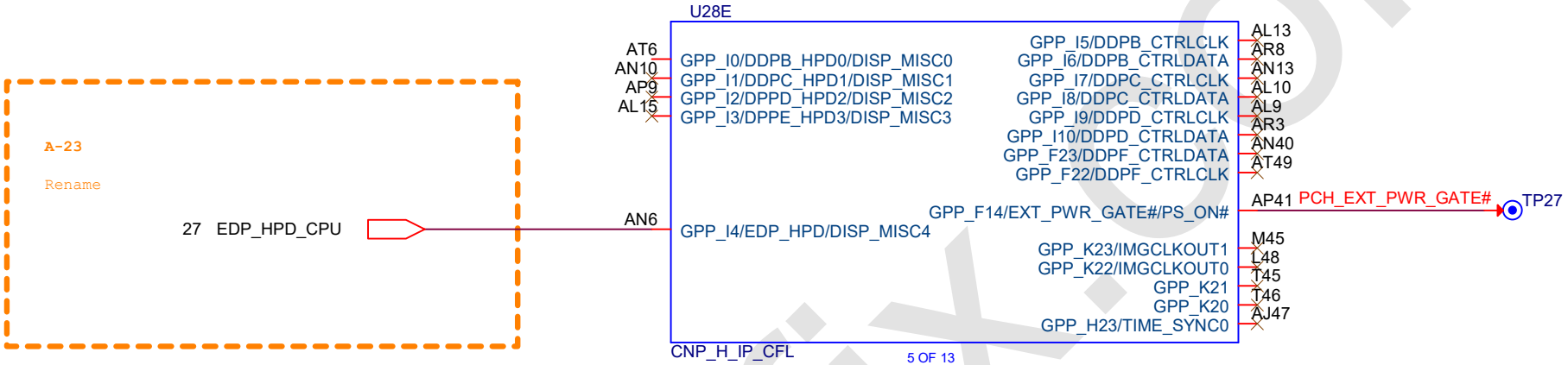

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Title
PCH CFL-H : DDI CONTROL

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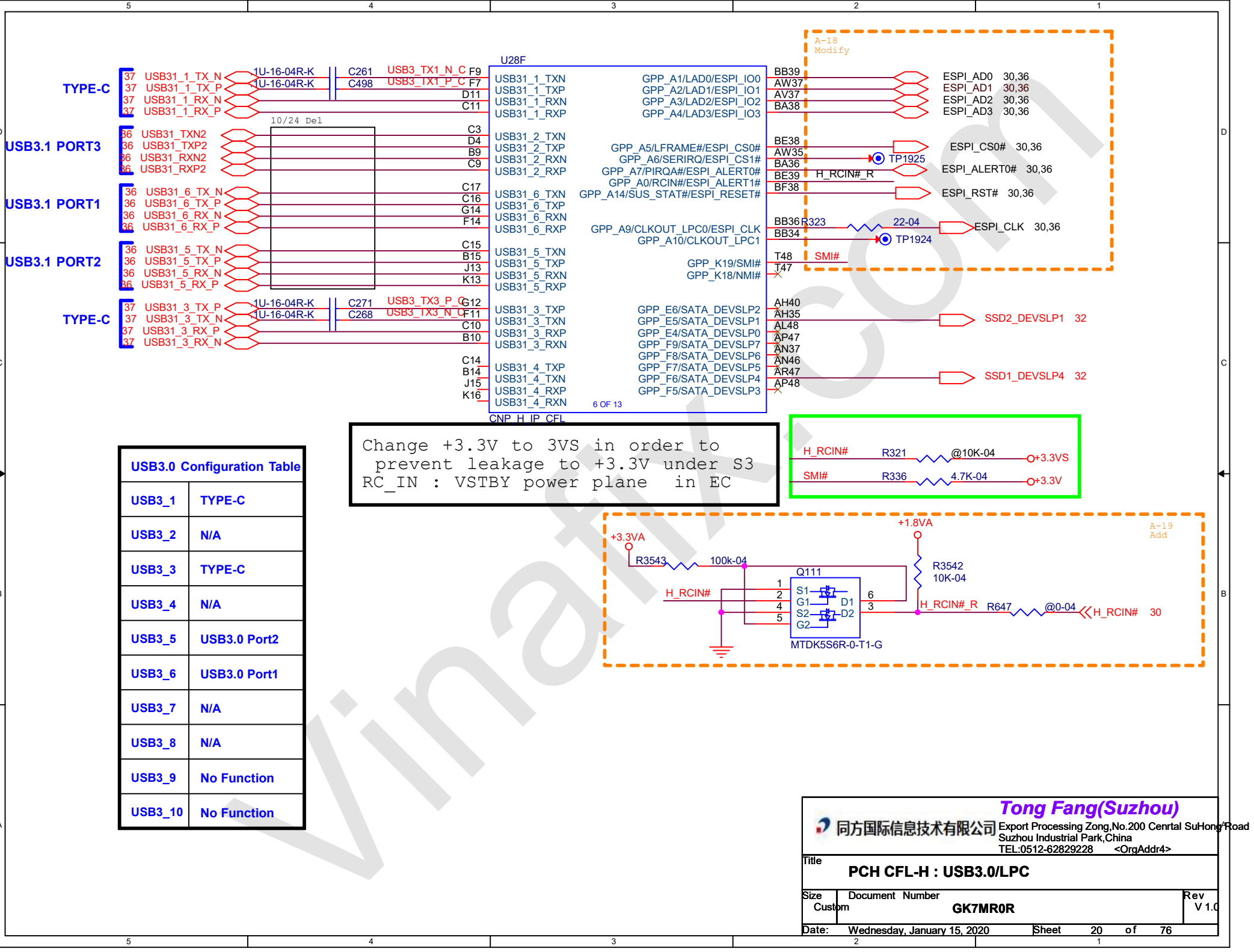

USB3.0 Configuration Table	
USB3_1	TYPE-C
USB3_2	N/A
USB3_3	TYPE-C
USB3_4	N/A
USB3_5	USB3.0 Port2
USB3_6	USB3.0 Port1
USB3_7	N/A
USB3_8	N/A
USB3_9	No Function
USB3_10	No Function

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Title: PCH CFL-H : USB3.0/LPC

Size: Custom | Document Number: GK7MR0R | Rev: V 1.0

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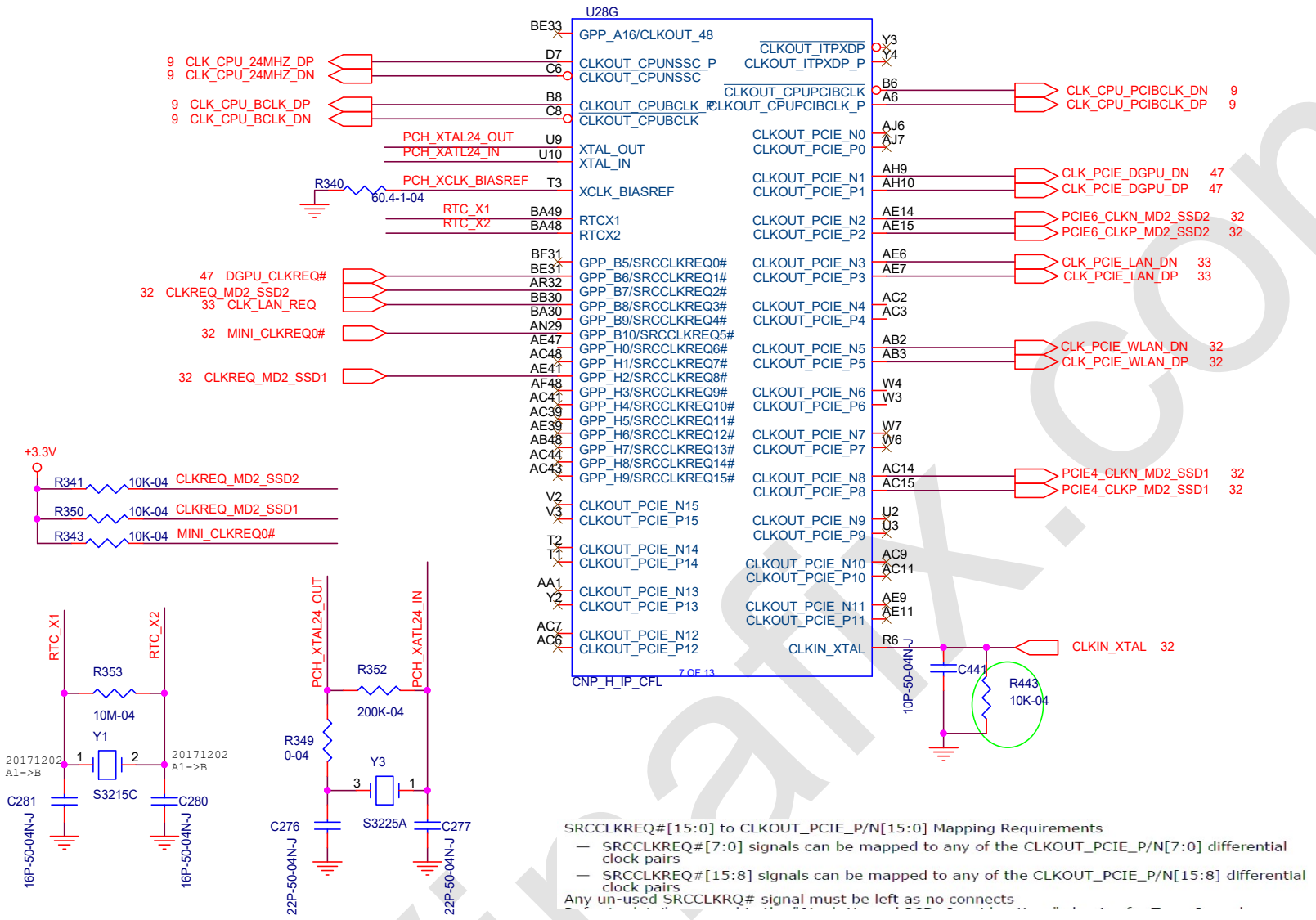

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Title	PCH CFL-H : CLK	
Size: Custom	Document Number: GK7MR0R	Rev: V 1.0
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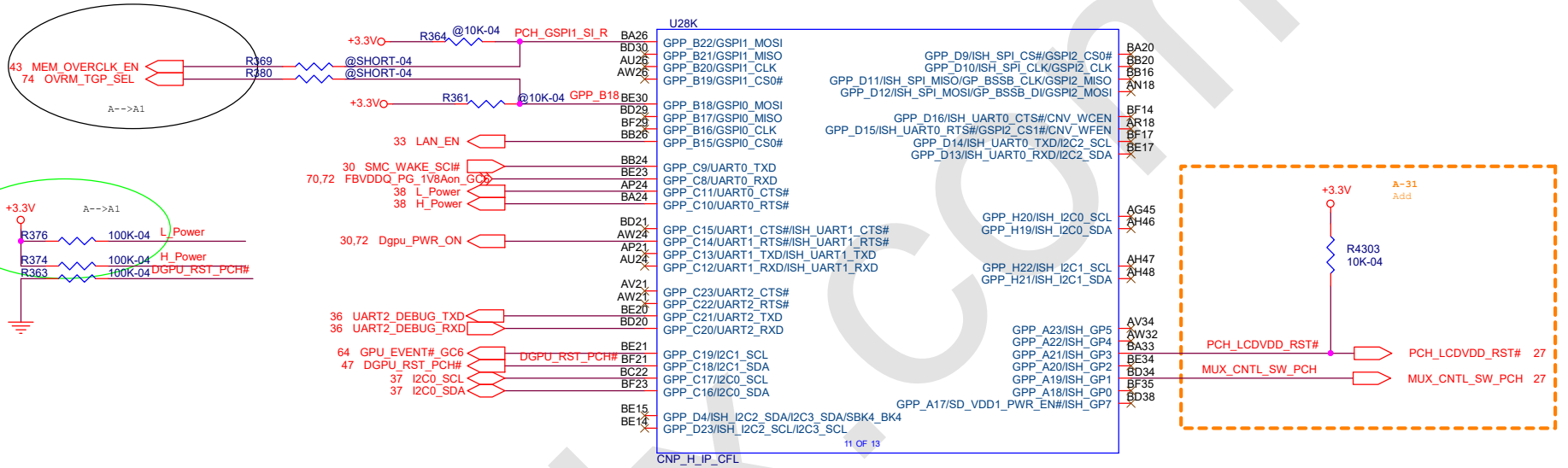
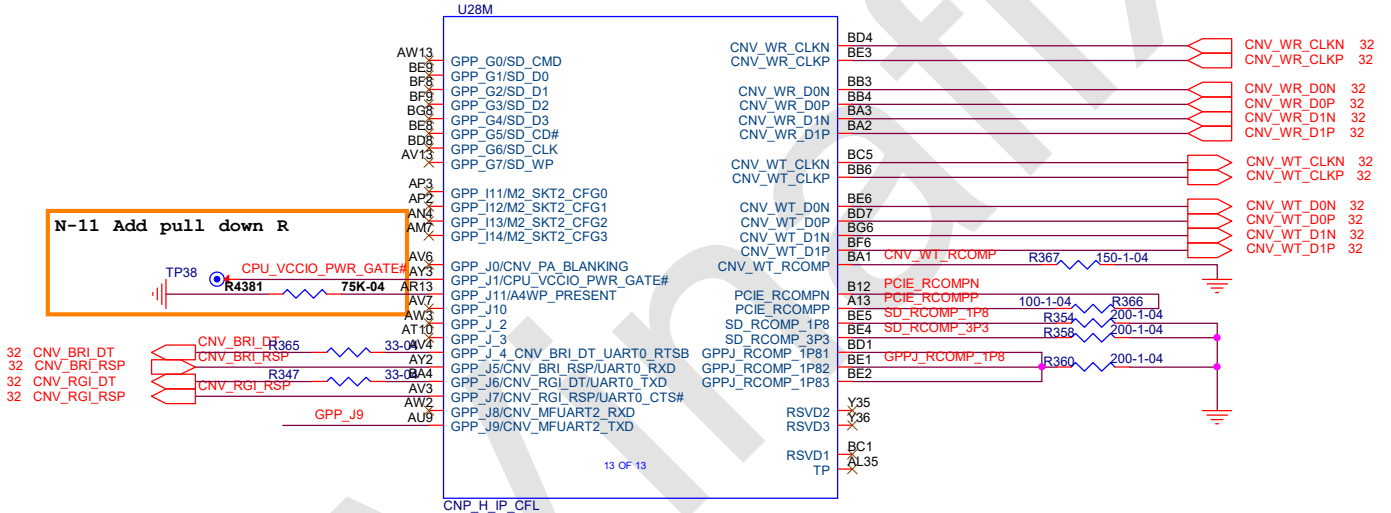
GPP_B22/GSPI1_MOSI(IPD)	Boot BIOS Strap Bit
0(weak internal pull down)	SPI
1	LPC

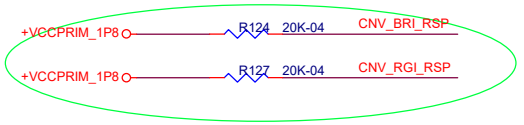
GPP_B18/GSPI0_MOSI(IPD)	No Reboot
0	Disable "No Reboot" mode (Default)
1	Enable "No Reboot" mode





XTAL
0:38.4MHz (weak internal pull down)
1:24MHz

CNVi
0:CNVi enable
1:CNVi disable



VCCSPI
0:VCCSPI 3.3V (weak internal pull down)
1:VCCSPI 1.8V

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Title: PCH CFL-H:GSPI/UART/I2C/CNVi

Size	Document Number	Rev
B	GK7MR0R	V 1.0

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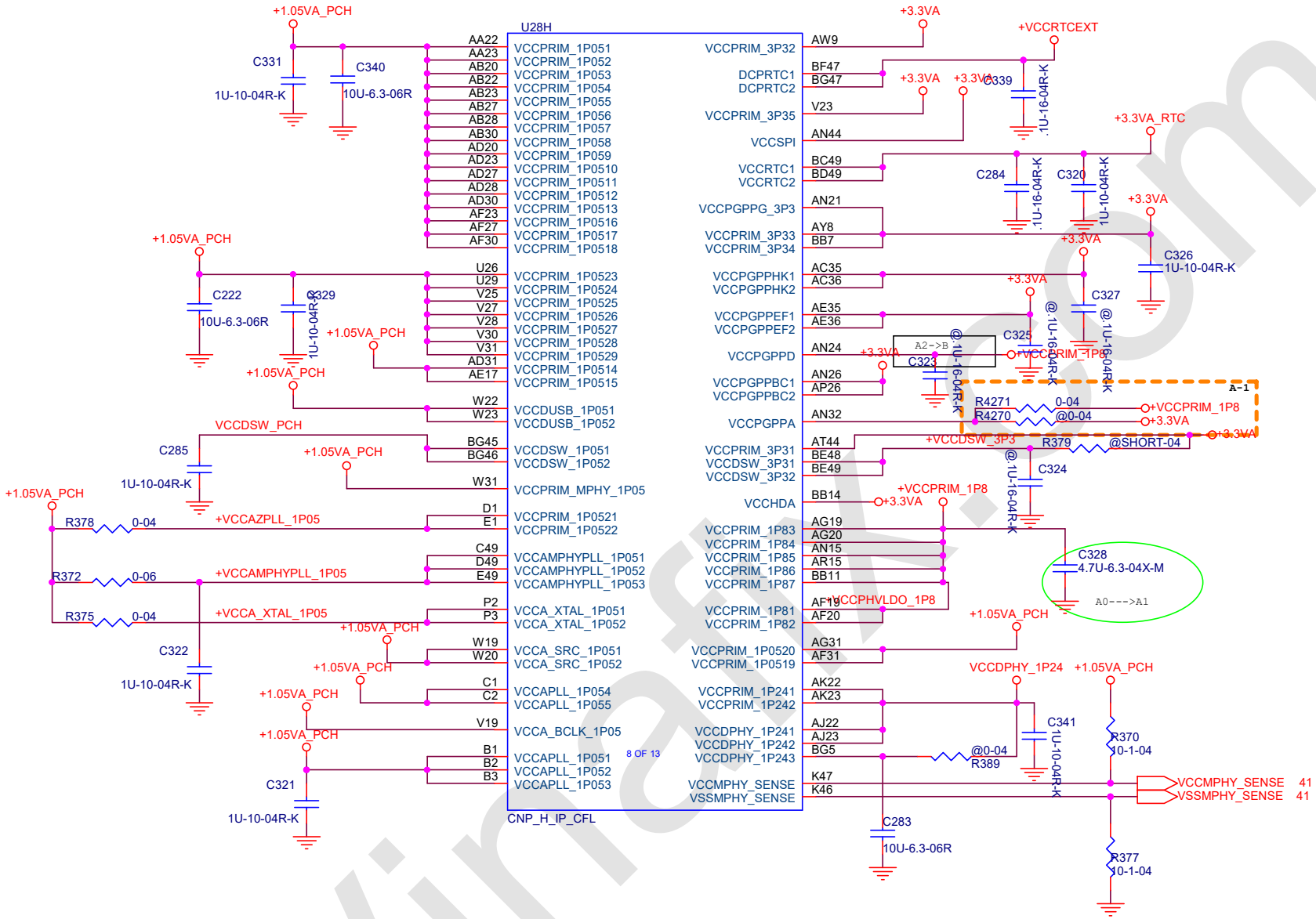
U28H
CNP_H_IP_CFL
8 OF 13
+1.05VA_PCH
+3.3VA
+VCCRTCEXT
+3.3VA_RTC
+VCCPRIM_1P8
+VCCDSW_3P3
+VCCPHVLDO_1P8
VCCDPHY_1P24
VCCDSW_PCH
VCCMPHY_SENSE 41
VSSMPHY_SENSE 41
A-1
A2->B
A0--->A1
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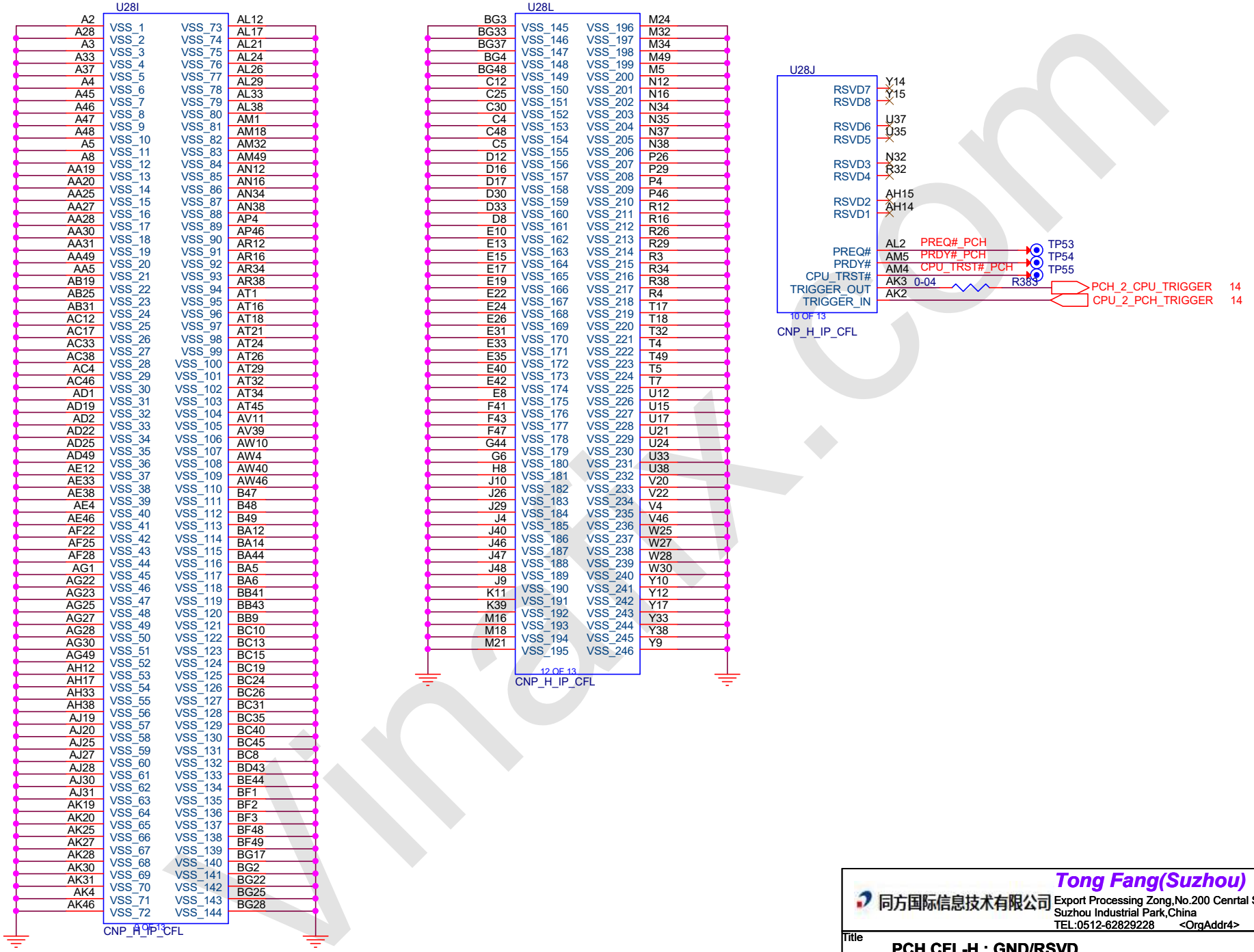
TEL:0512-62829228 <OrgAddr4>
Title
PCH CFL-H : POWER
Size
Custom
Document Number
GK7MR0R
Rev
V 1.0
Date: Wednesday, January 15, 2020
Sheet 23 of 76



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Title: PCH CFL-H : GND/RSVD

Size	Document Number	Rev
Custom	GK7MR0R	V 1.0

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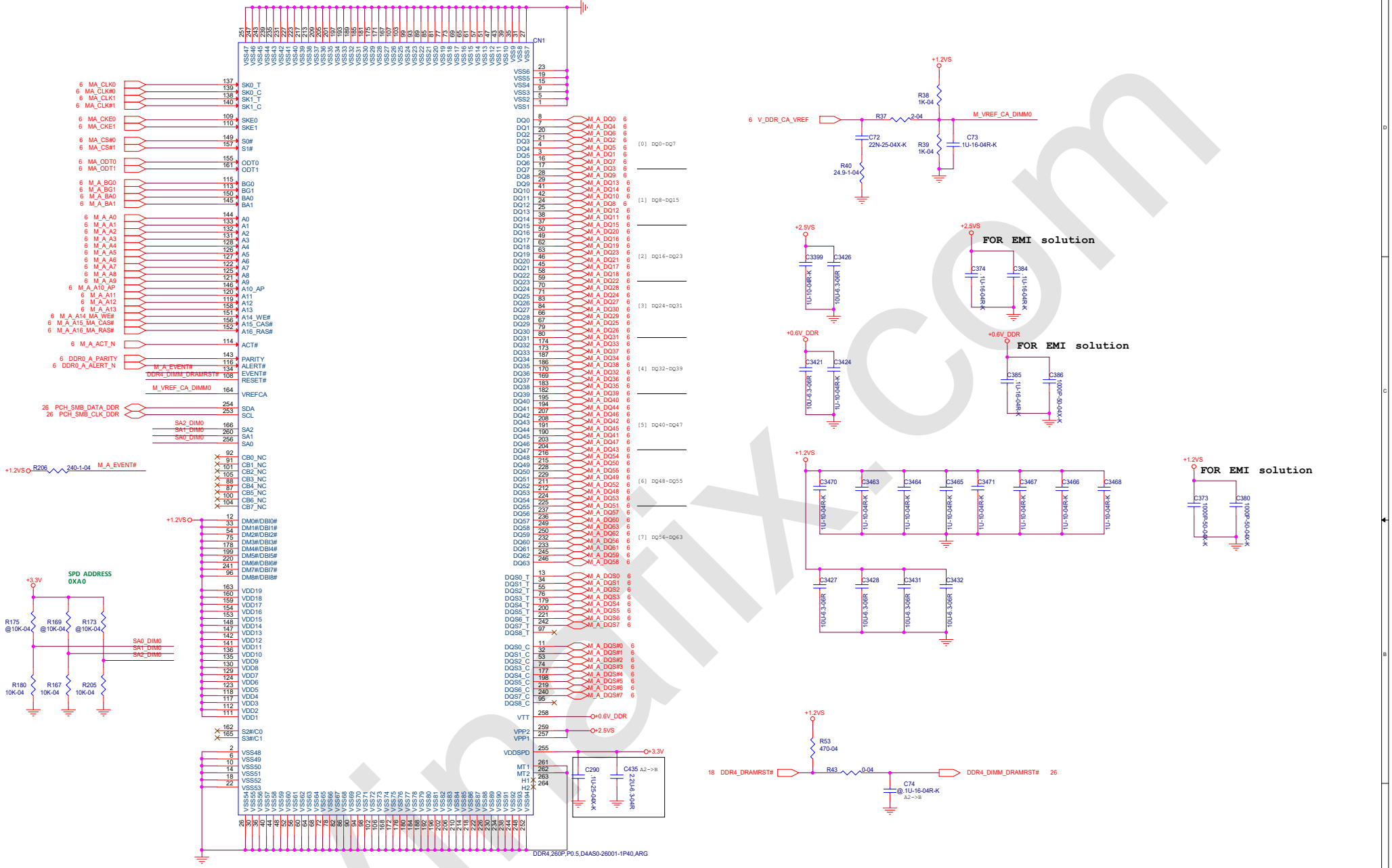
CN1
DDR4_260P.P0.5,D4AS0-26001-1P40,ARG
SPD ADDRESS
0XA0
FOR EMI solution
FOR EMI solution
FOR EMI solution
M_VREF_CA_DIMM0
DDR4_DIMM_DRAMRST#
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DDR4 SODIMMA
GK7MR0R
Wednesday, January 15, 2020
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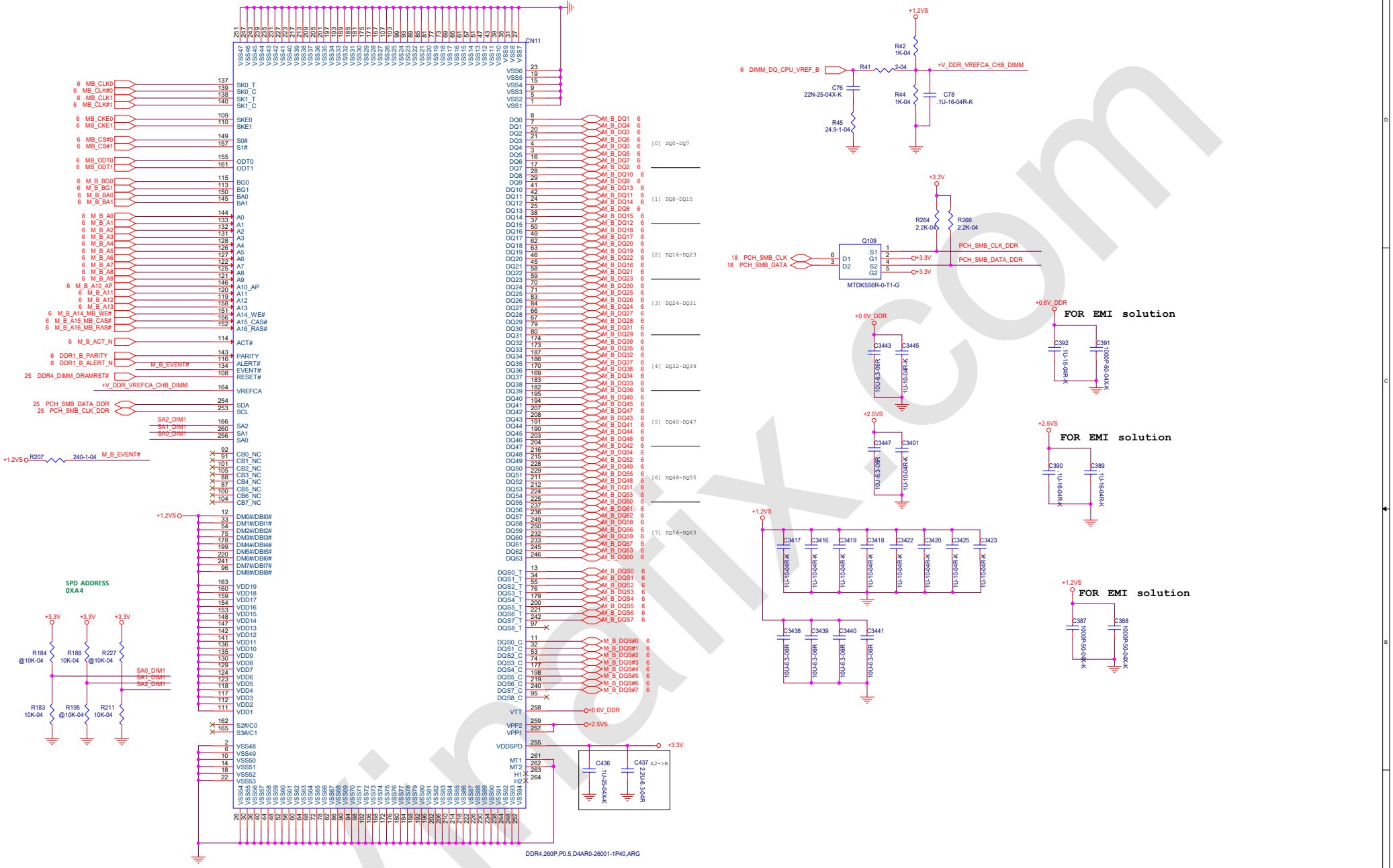
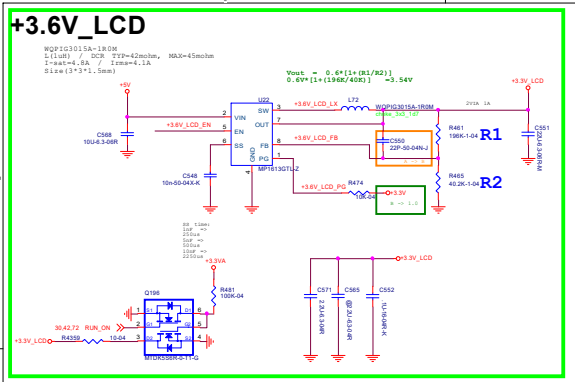
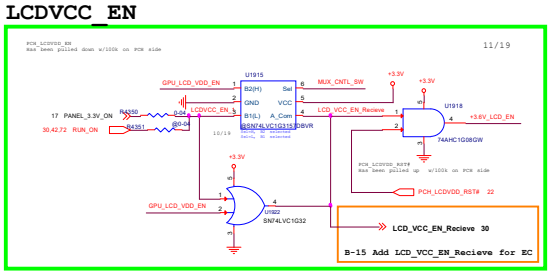
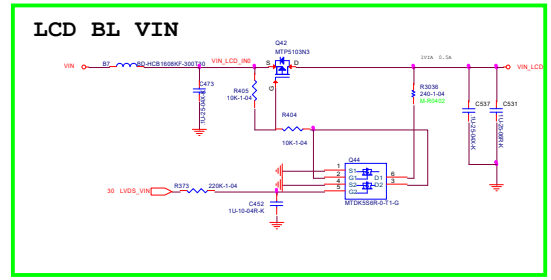
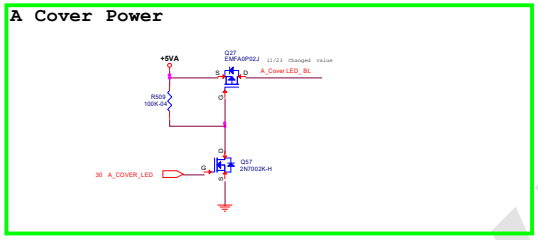


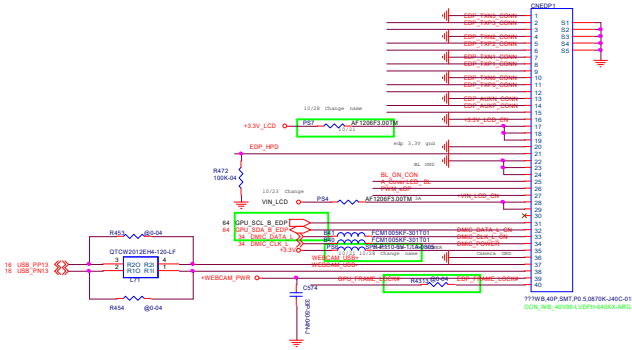
Title	DDR4 SODIMMB	
Size C	Document Number GK7MR0R	Rev V 1.0
Date: Wednesday, January 15, 2020	Sheet 26 of 76	

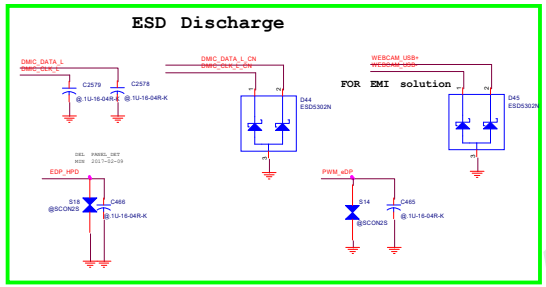


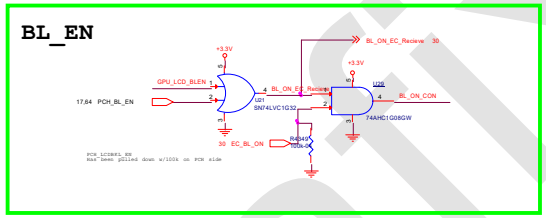


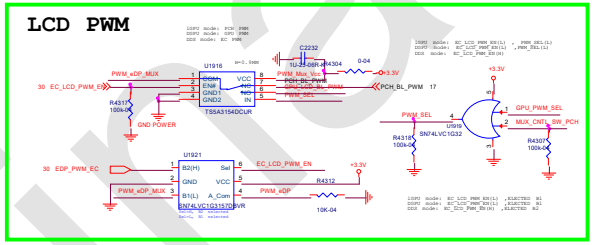


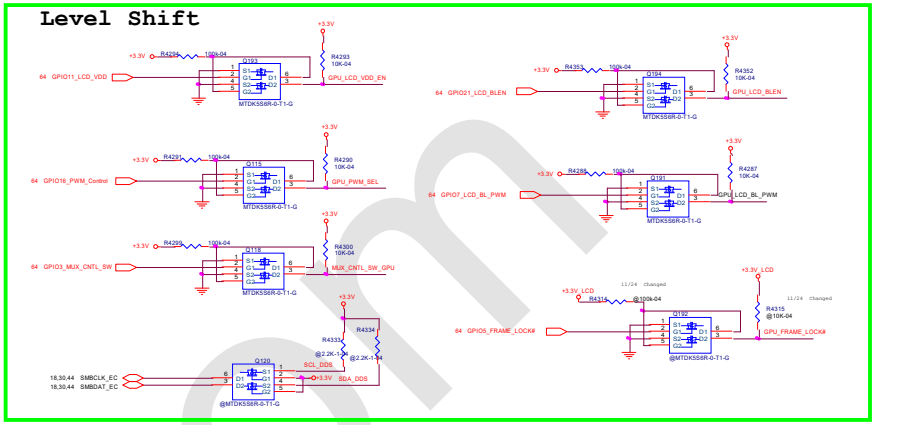


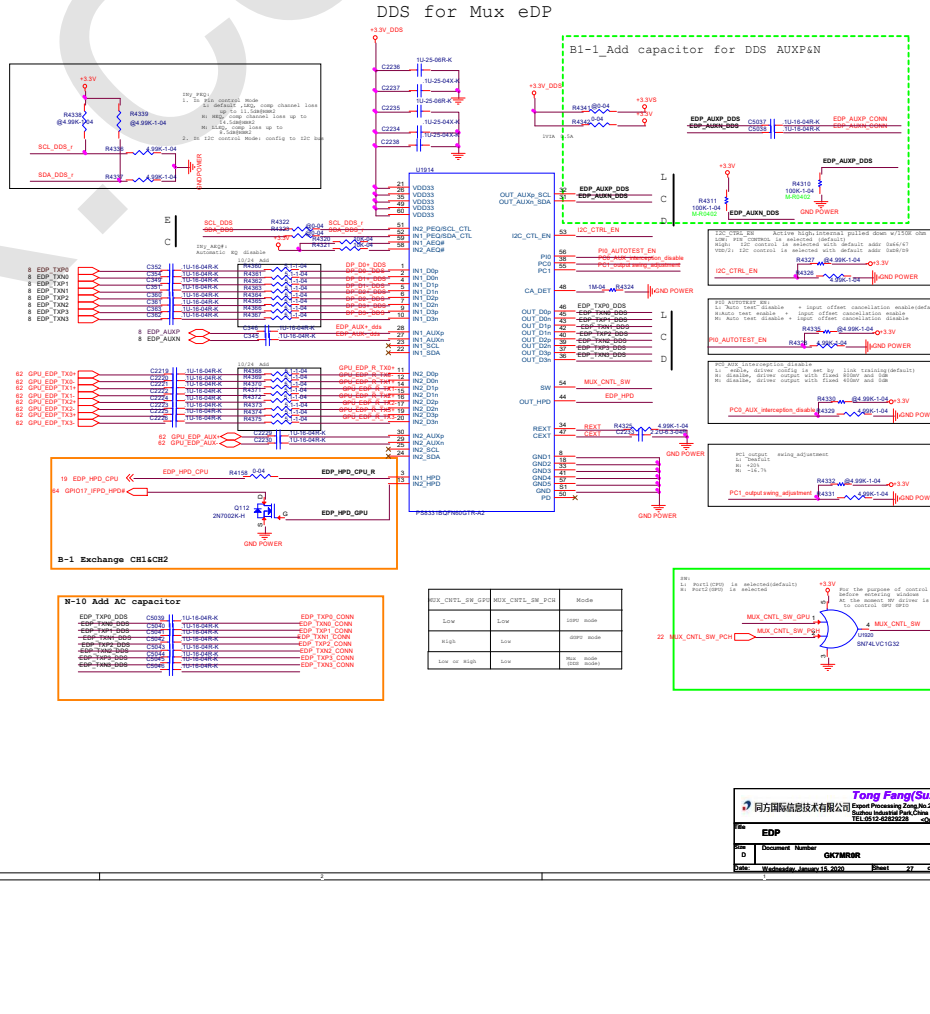












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Title	EDP	
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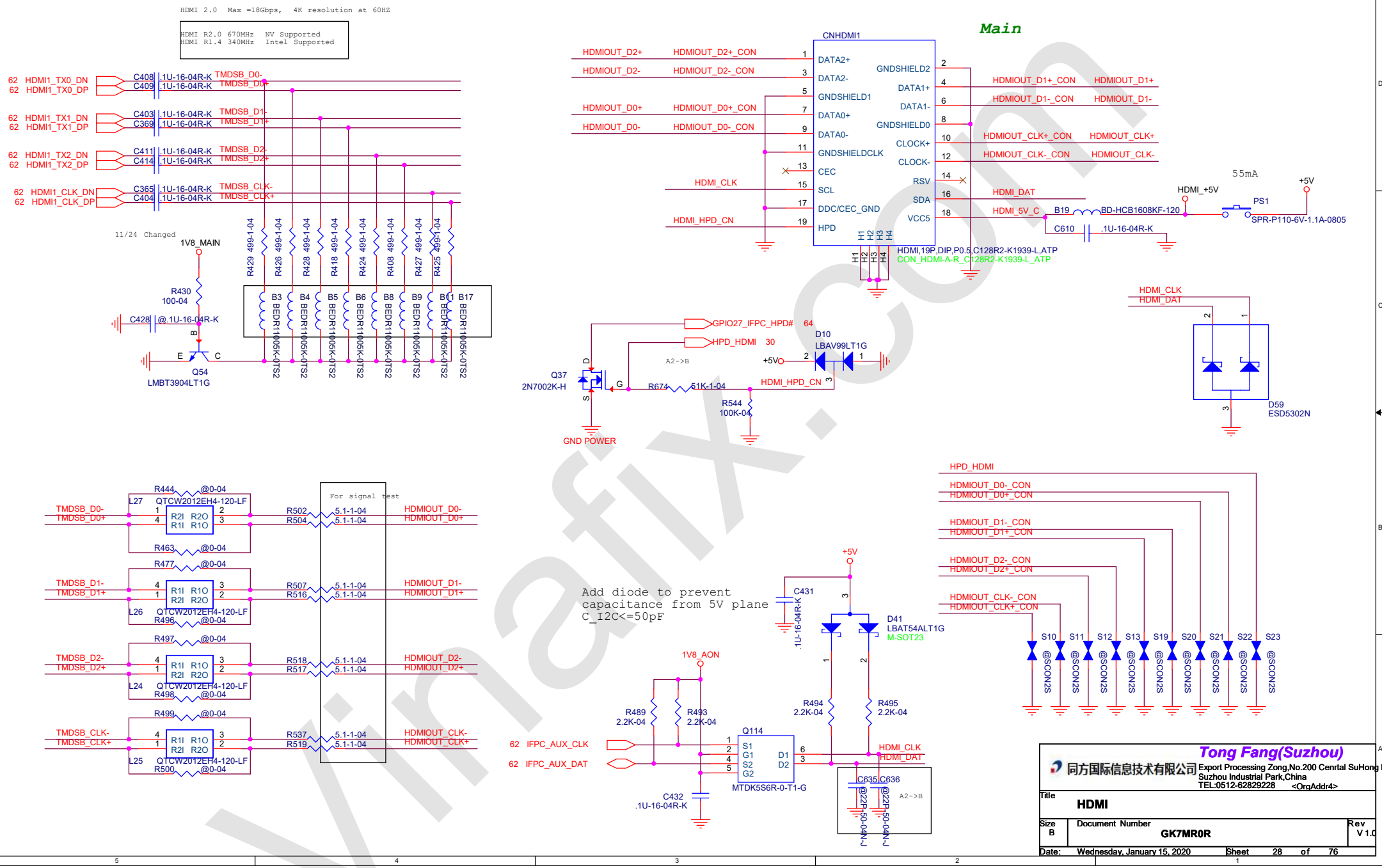
HDMI CONN



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Title	HDMI	
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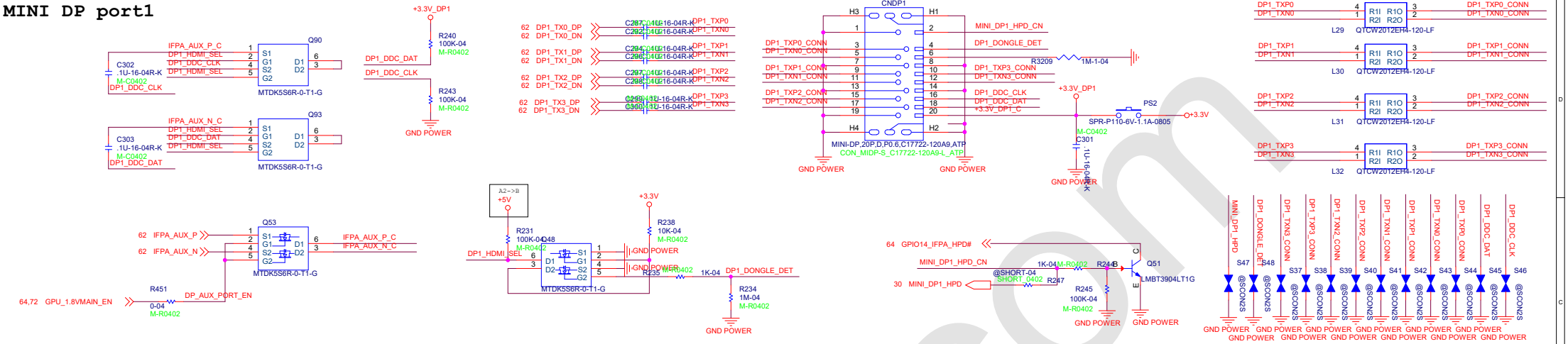
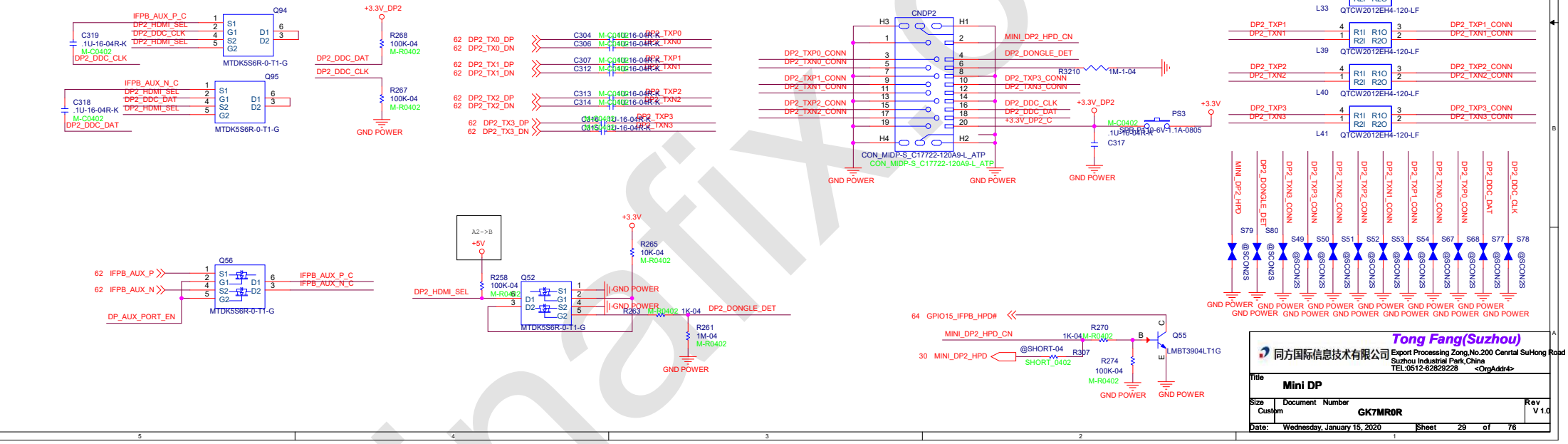
MINI DP port1



MINI DP port2



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Title	Mini DP		
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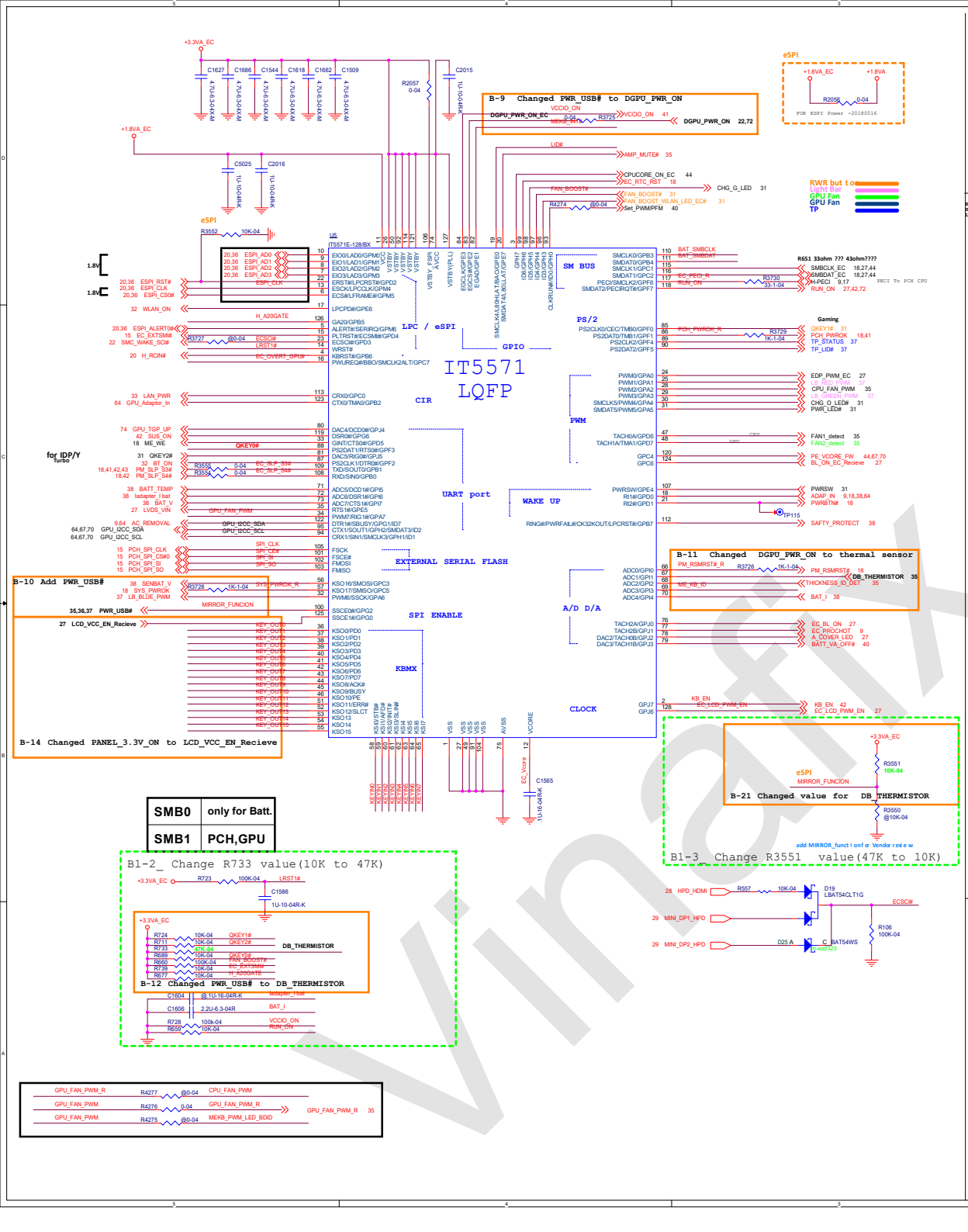

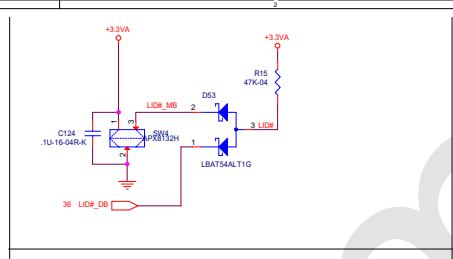

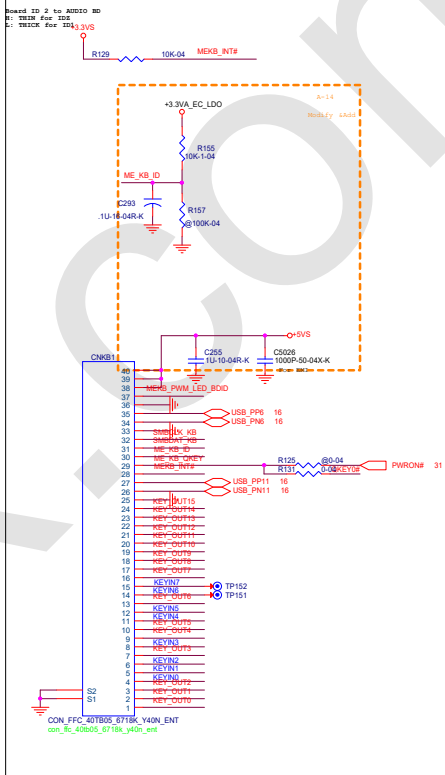

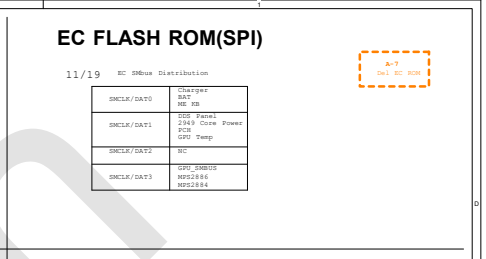

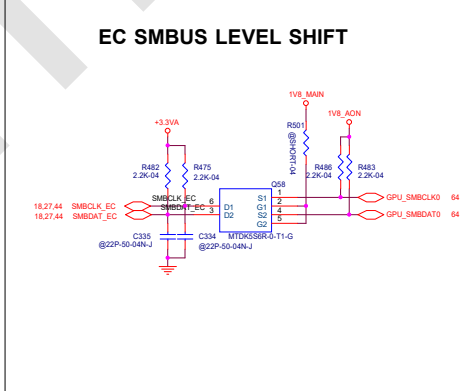

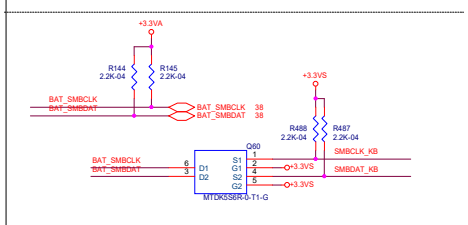

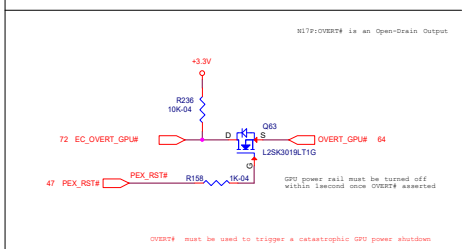

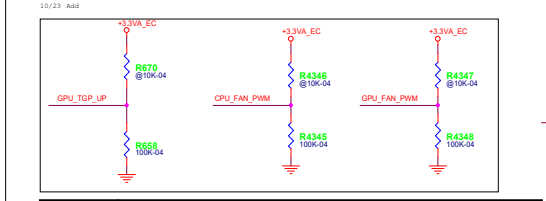

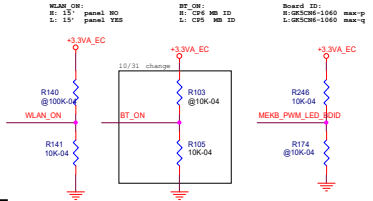

NET / Level	CPU_FAN_PWM GPA2	GPU_FAN_PWM GPA7	WLAN_ON GPE6	BT_ON GPF2	GPU_TGP_UP GPJ4
N18E-G0	LOW	LOW	LOW	LOW	LOW
N18E-G1-B	LOW	LOW	LOW	LOW	HIGH
N18P-G62	LOW	LOW	LOW	HIGH	LOW
N/A	LOW	LOW	LOW	HIGH	HIGH

eSPI version

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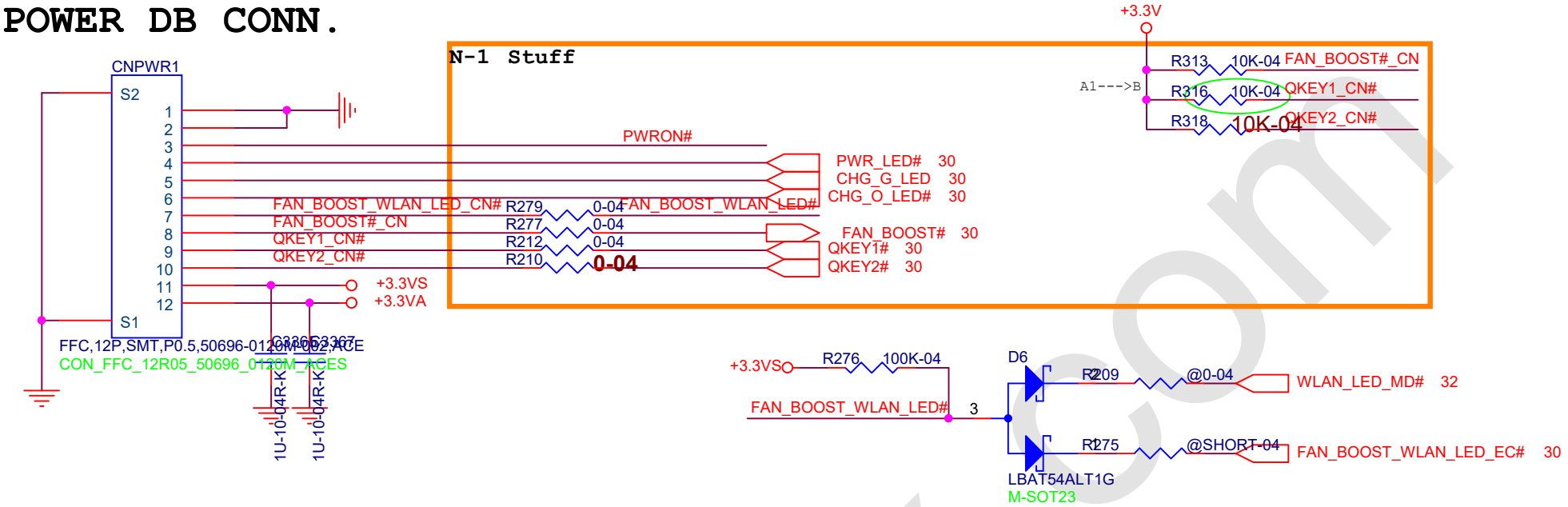
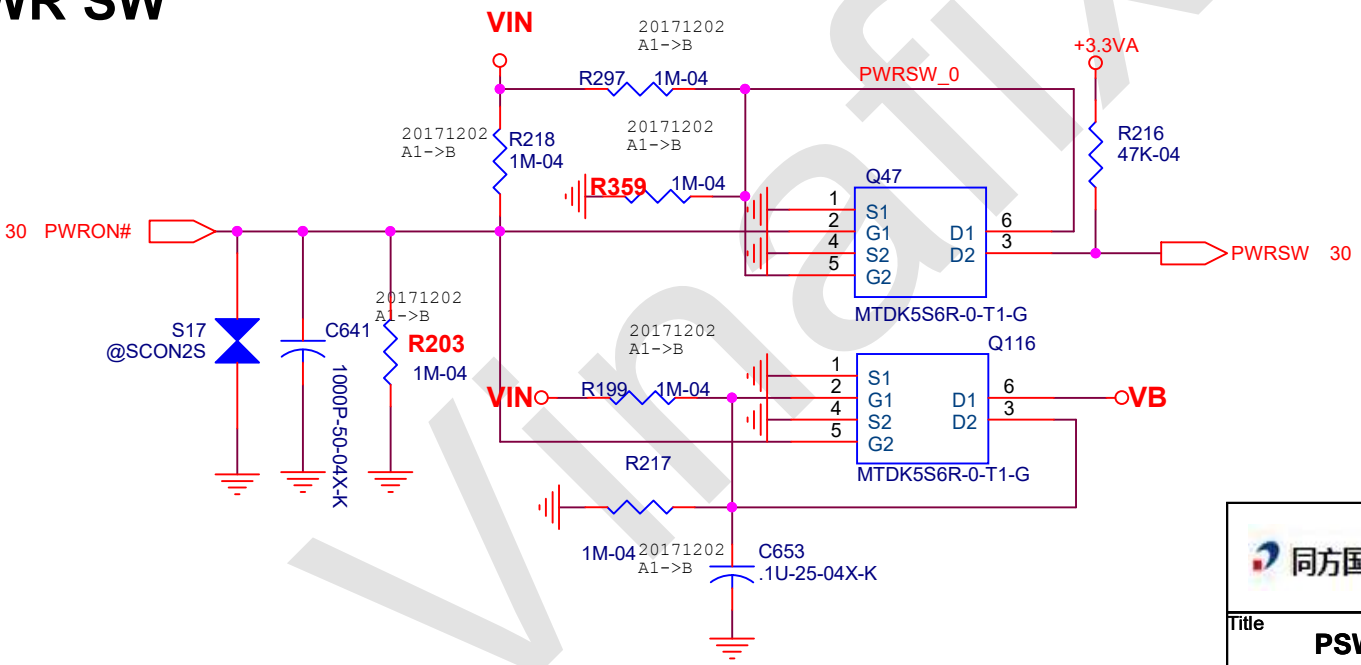
POWER DB CONN.



PWR SW



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Title	PSW/PWR DB CON	
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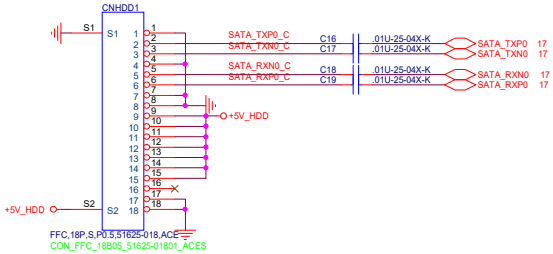
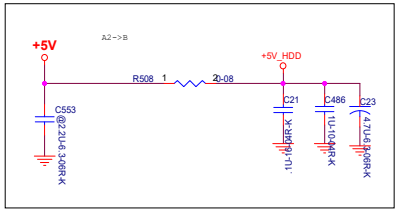
SATA-HDD





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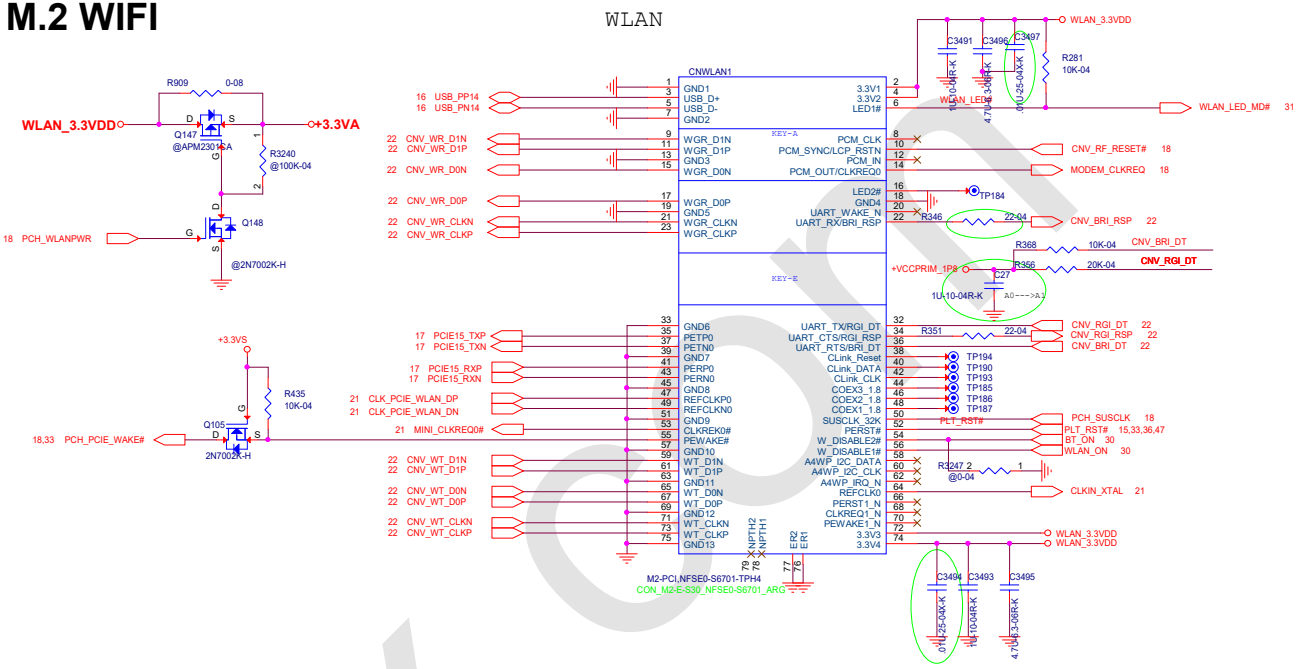
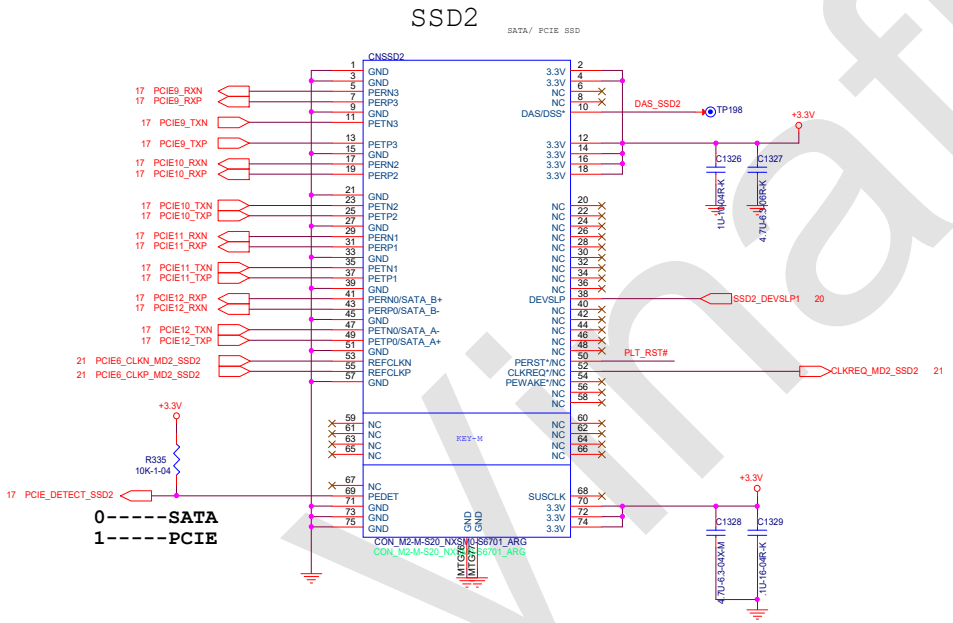
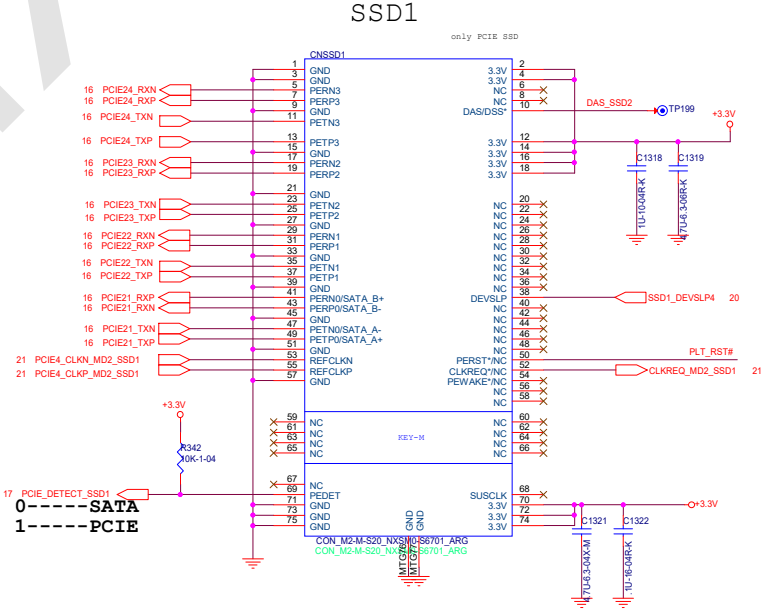


M.2 SSD





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Title	LAN RTL8111	
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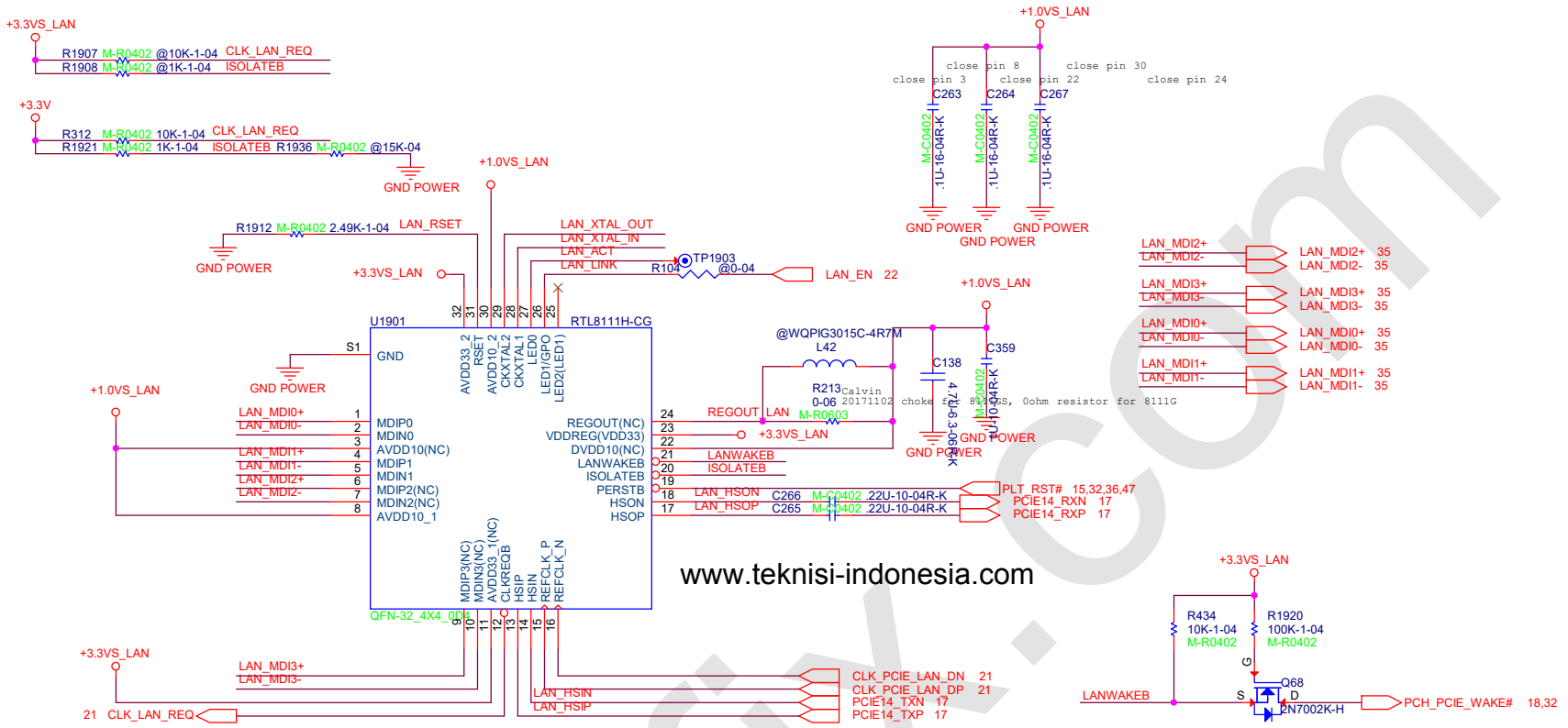

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Title	HDD/M.2/UART debug	
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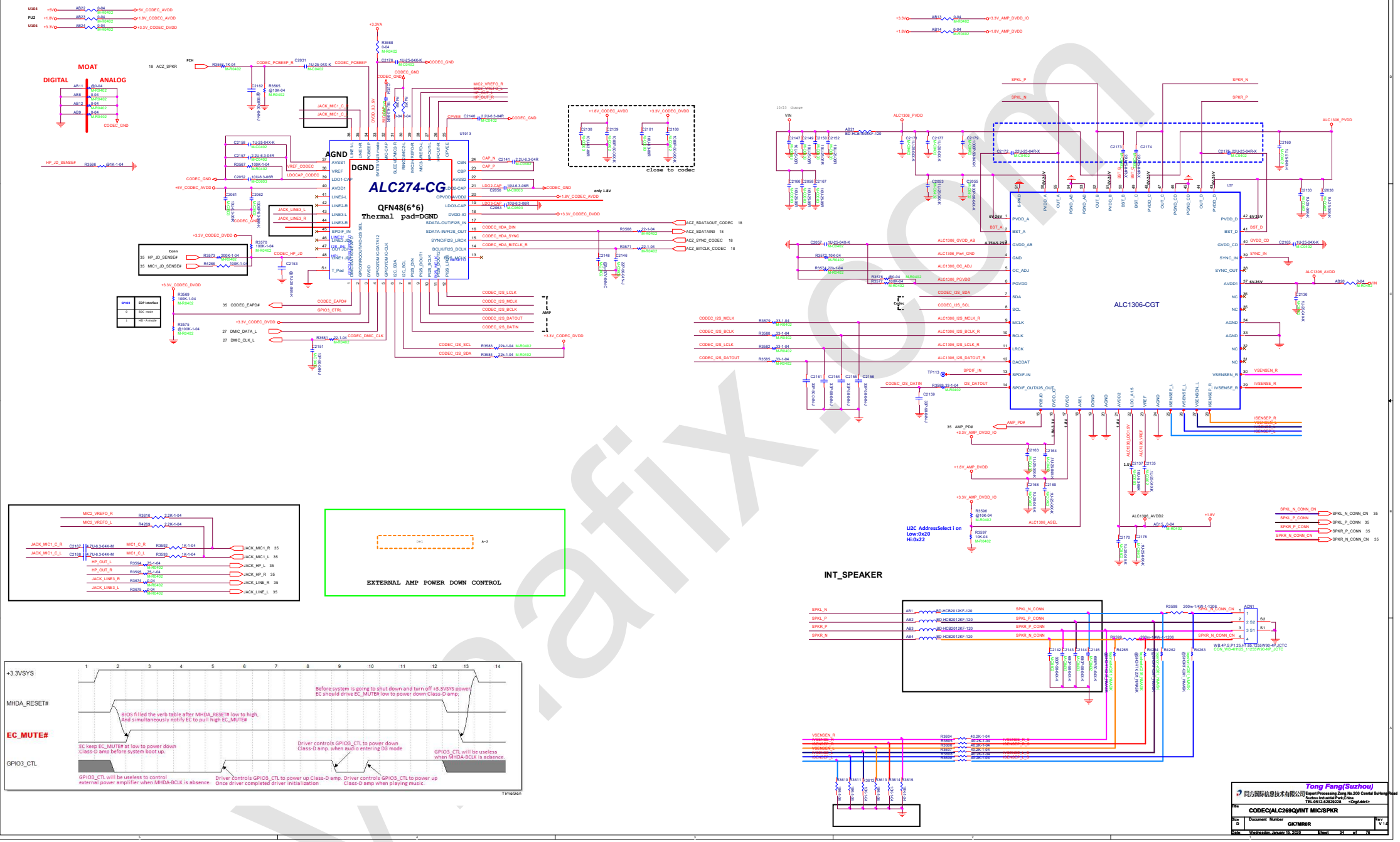
CODEC-ALC274

AMP-ALC1306



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Title	CODEC(ALC269Q)/INT MIC/SPKR		
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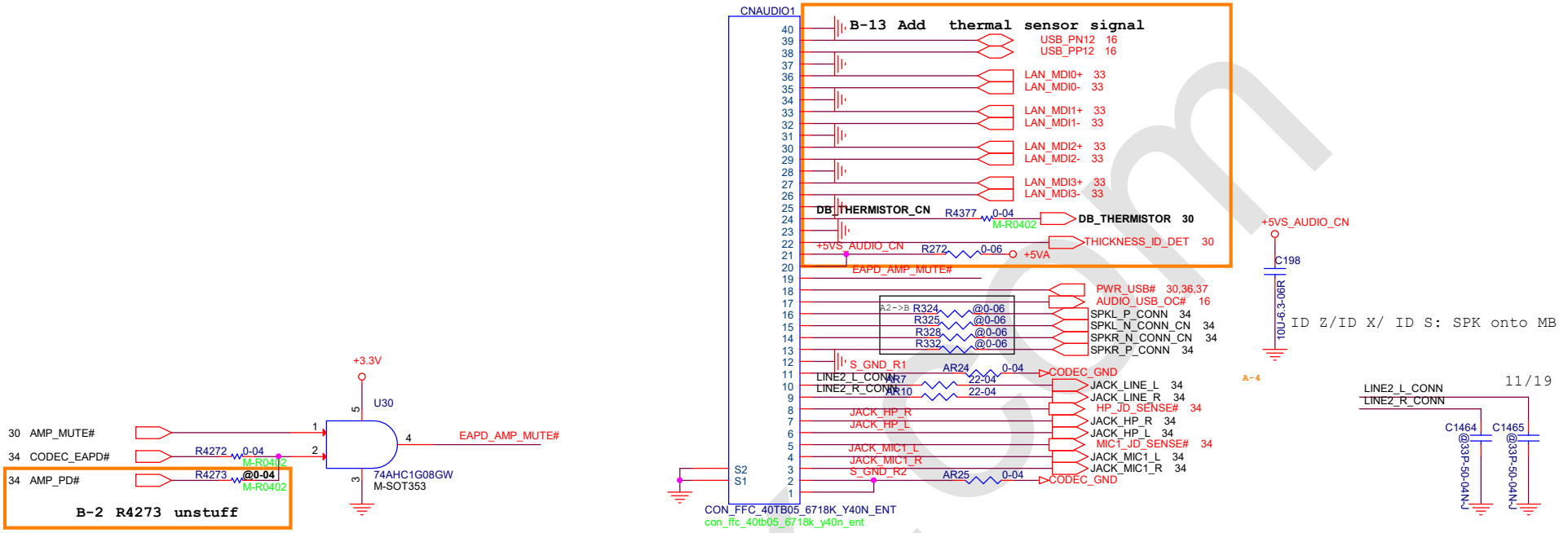
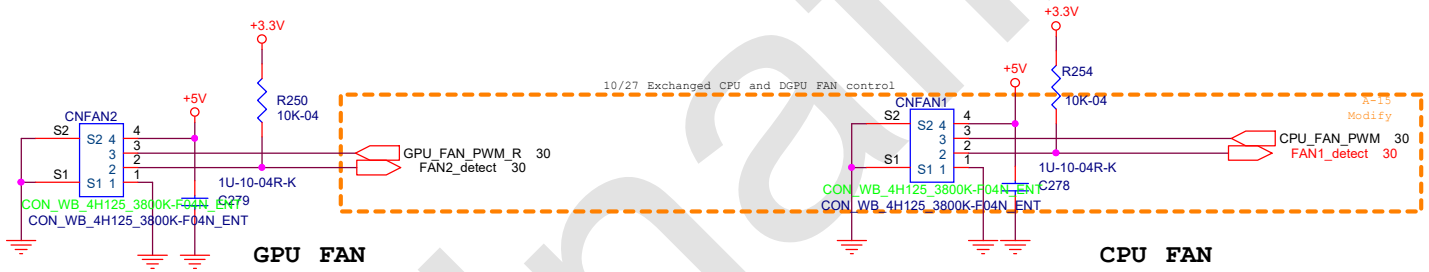
EXT MIC / EXT LINE IN / EXT USB JACK



FAN CONTROLLER 0

FAN CONTROLLER 1



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Title	EXT_AUDIO/EXT_USB/FAN	
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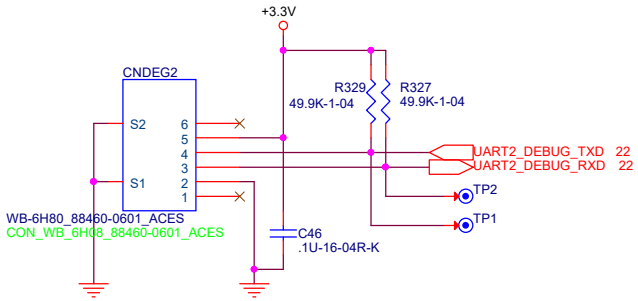
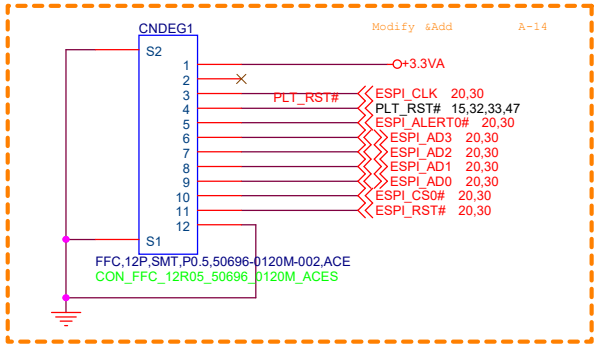
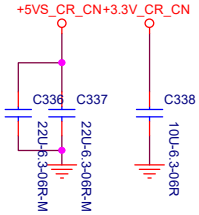
UART debug port

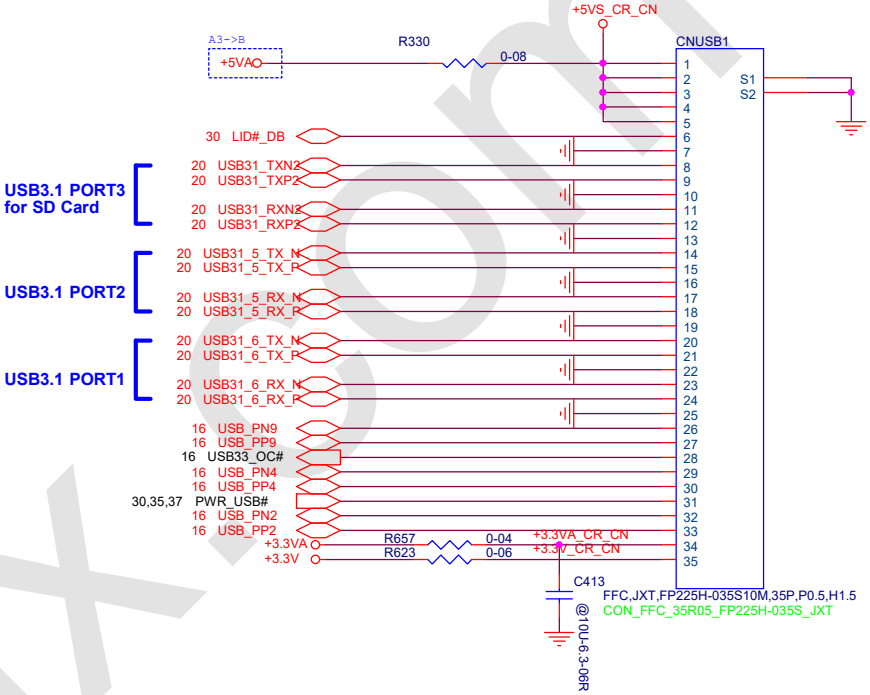


ESPI debug port



USB3.0 DB CONN.





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Title	EXT USB3.0	
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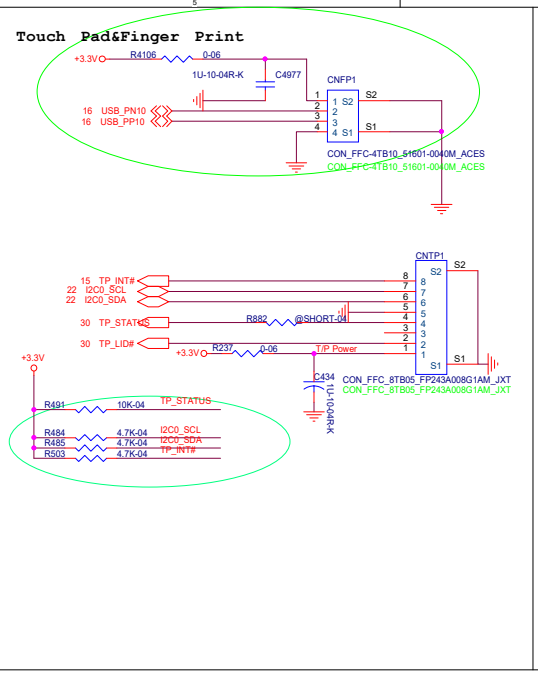
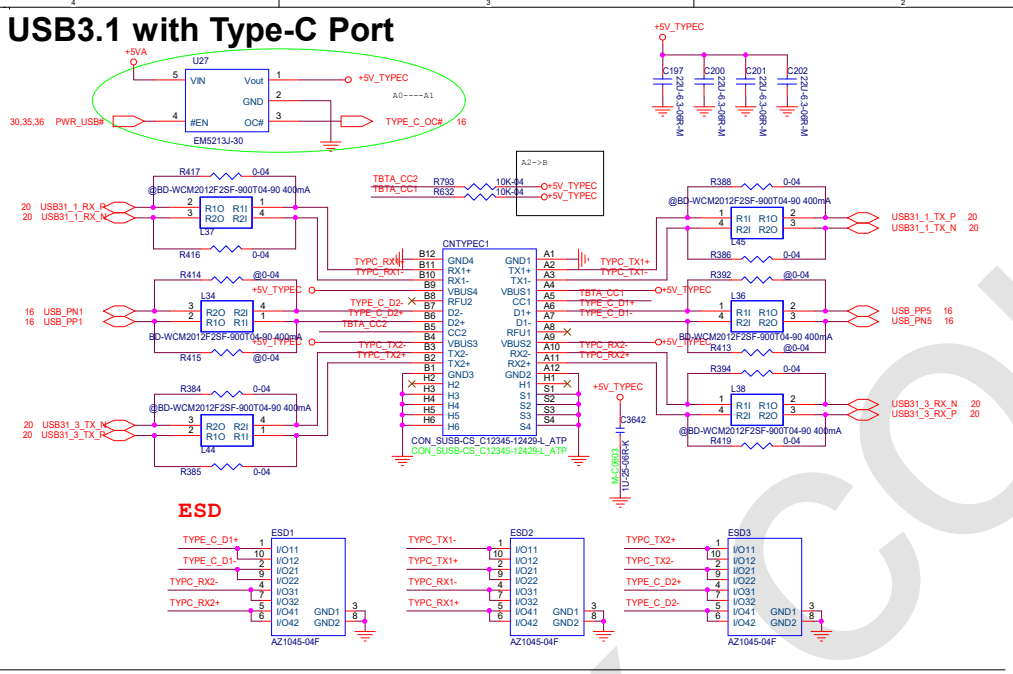
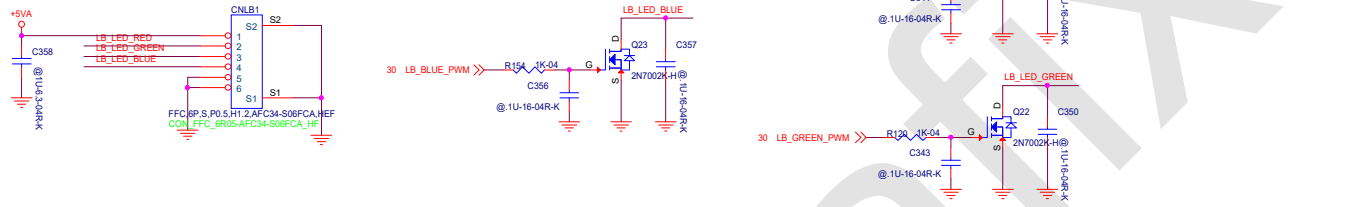


USB3.1 with Type-C Port



ESD

Light bar Control



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Title: TP/USB/TYPEC

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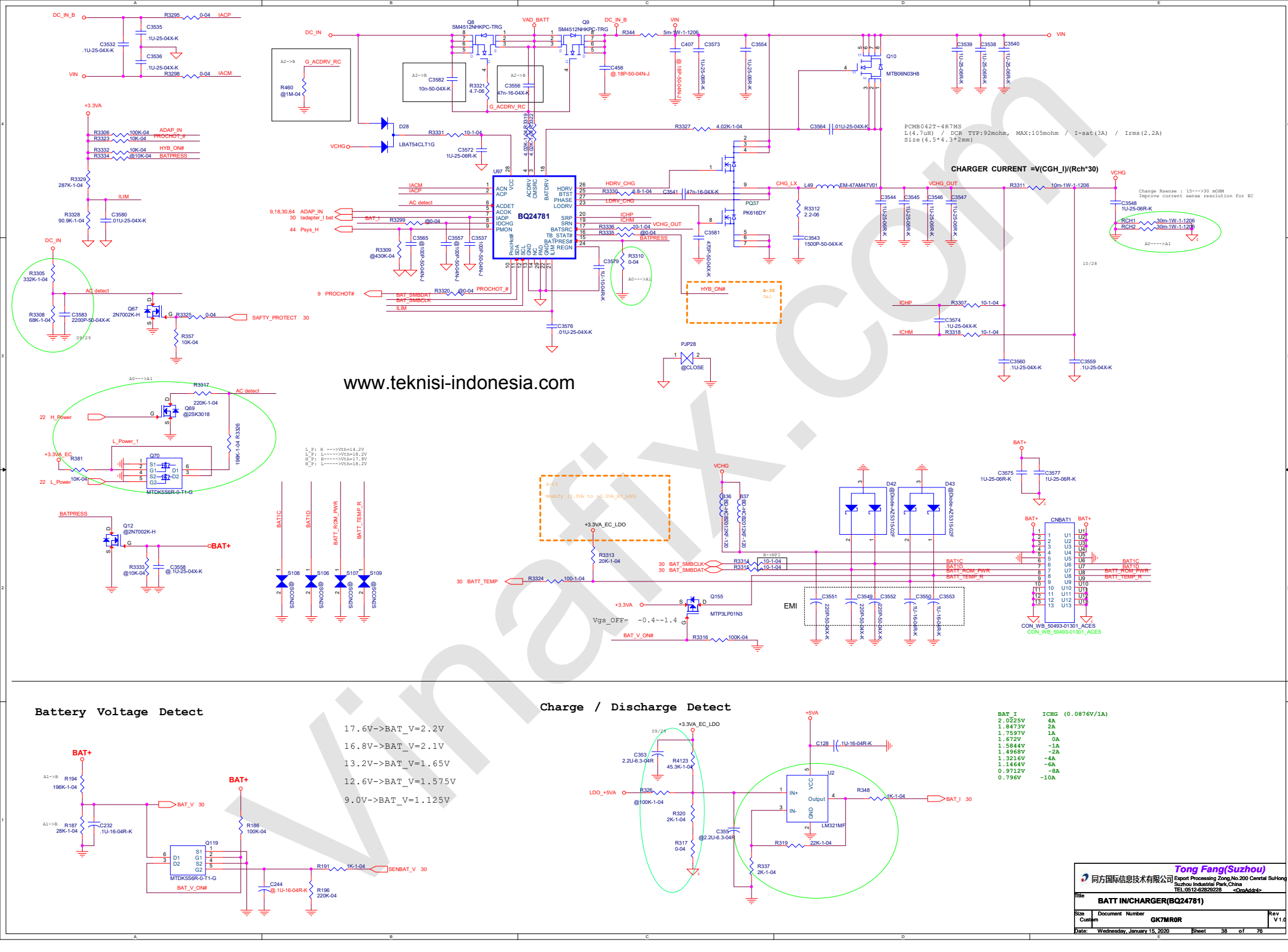
BQ24781
CHARGER CURRENT =V(CGH_I)/(Rch*30)
PCMB042T-4R7MS
L(4.7uH) / DCR TYP:92mohm, MAX:105mohm / I-sat(3A) / Irms(2.2A)
Size(4.5*4.3*2mm)
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Battery Voltage Detect
17.6V->BAT_V=2.2V
16.8V->BAT_V=2.1V
13.2V->BAT_V=1.65V
12.6V->BAT_V=1.575V
9.0V->BAT_V=1.125V
Charge / Discharge Detect
BAT_I ICHG (0.0876V/1A)
2.0225V 4A
1.8473V 2A
1.7597V 1A
1.672V 0A
1.5844V -1A
1.4968V -2A
1.3216V -4A
1.1464V -6A
0.9712V -8A
0.796V -10A
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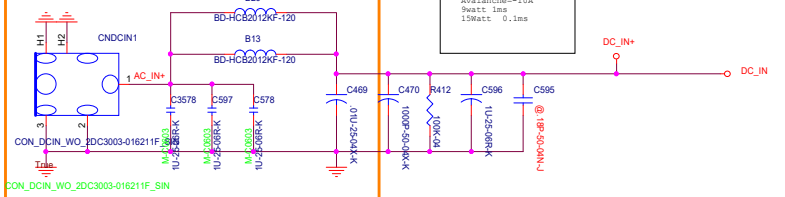
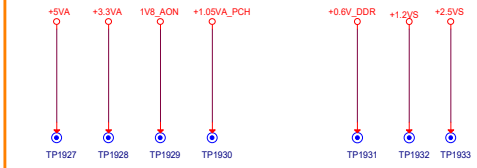
BATT IN/CHARGER(BQ24781)
GK7MR0R
Wednesday, January 15, 2020

DC IN

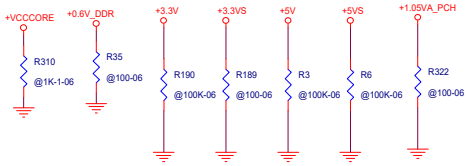


B-18 Changed PCB footprint for hole size and update symbol

N-9 Add test point

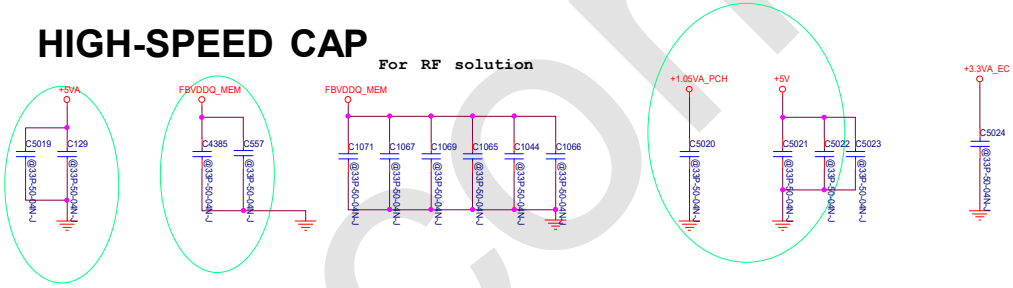


Discharge Resistor

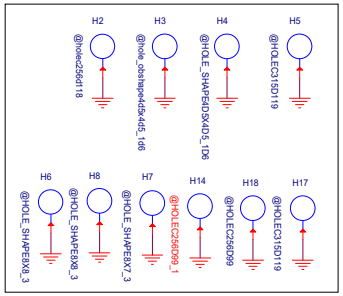


HIGH-SPEED CAP

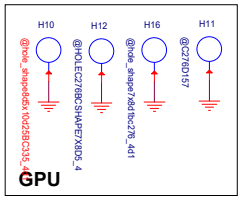
For RF solution

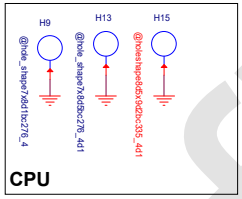


PCB HOLE



THERMAL HOLE





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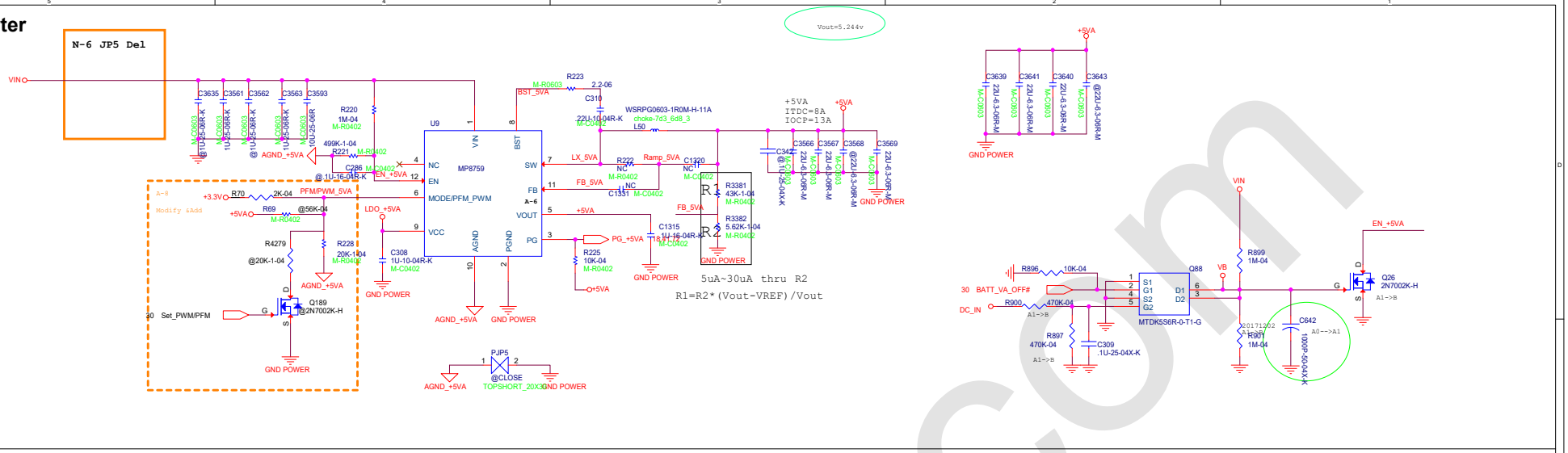
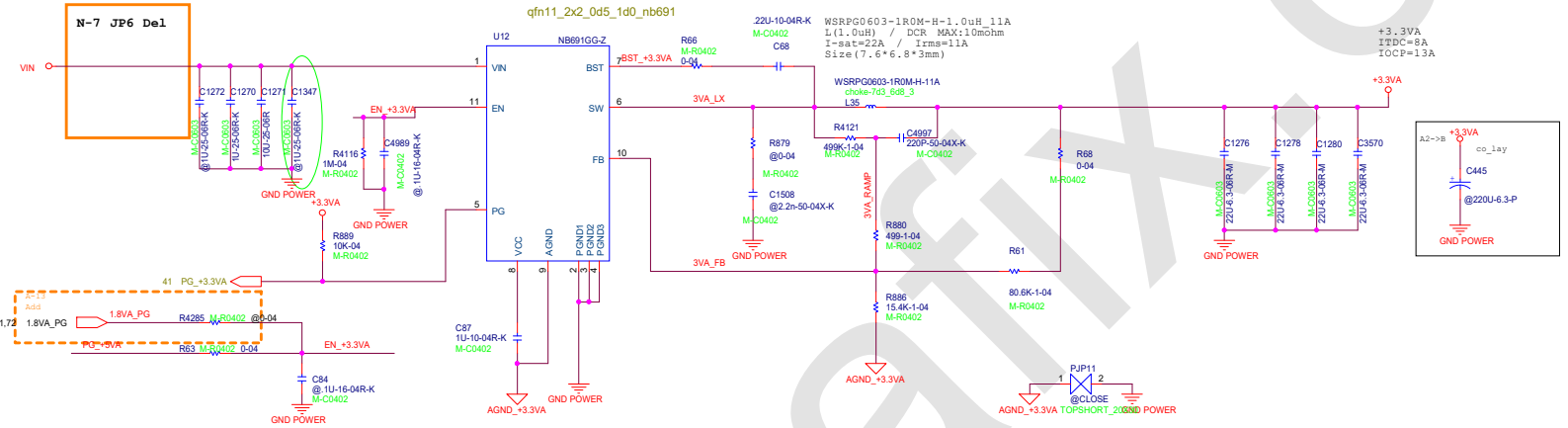
5VA Converter



3.3VA Converter



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Title	+5VA/+3.3VA		
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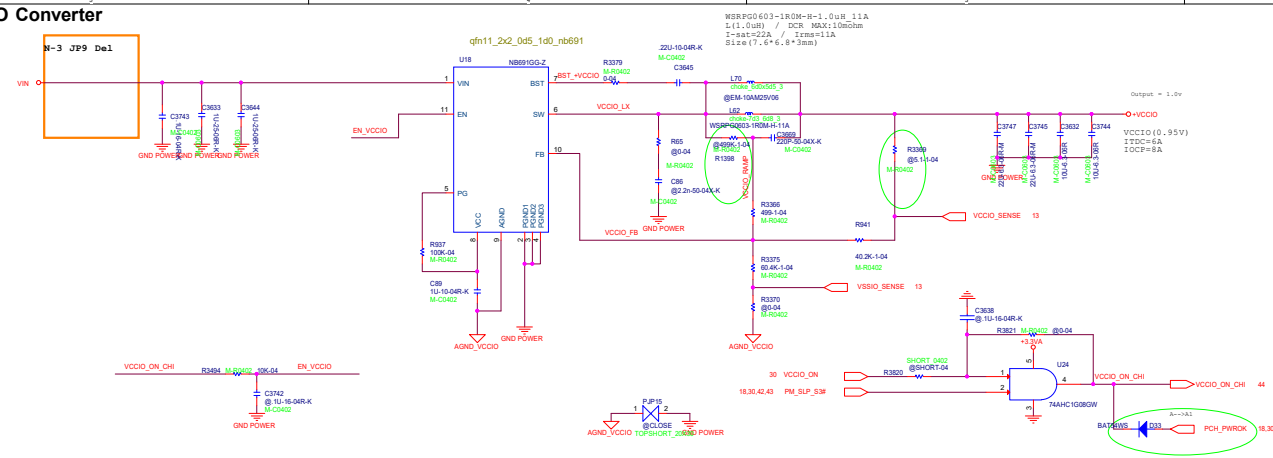
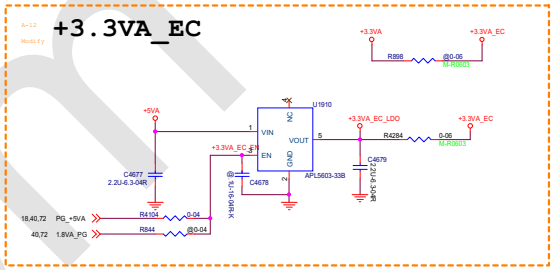
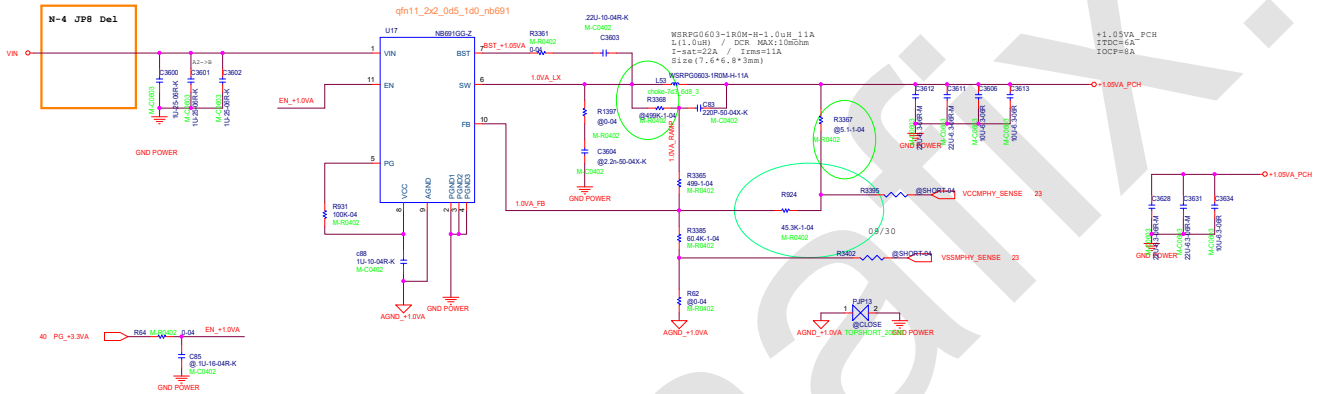
VCCIO Converter

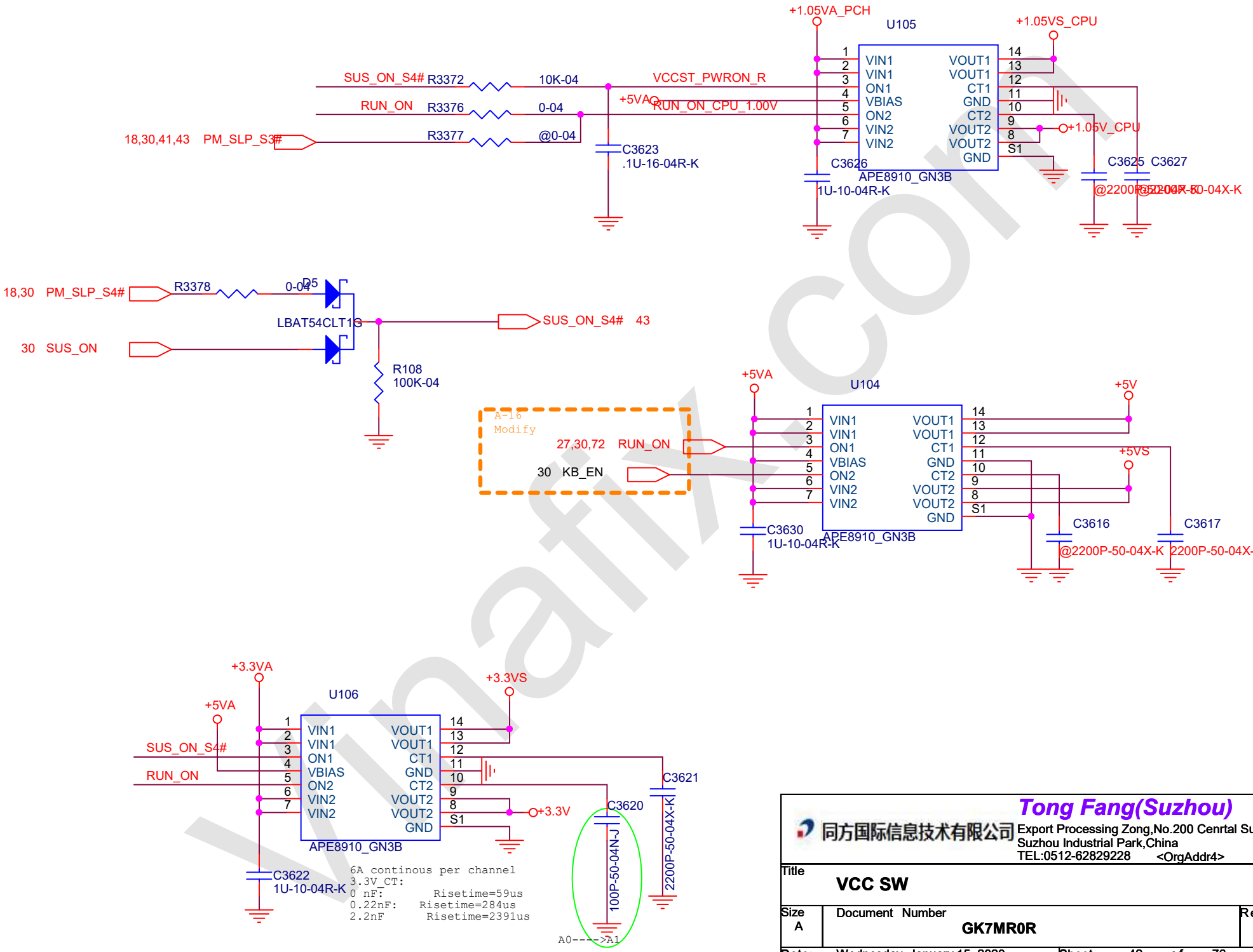


+3.3VA_EC



1.05VA Converter





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Title	VCC SW	
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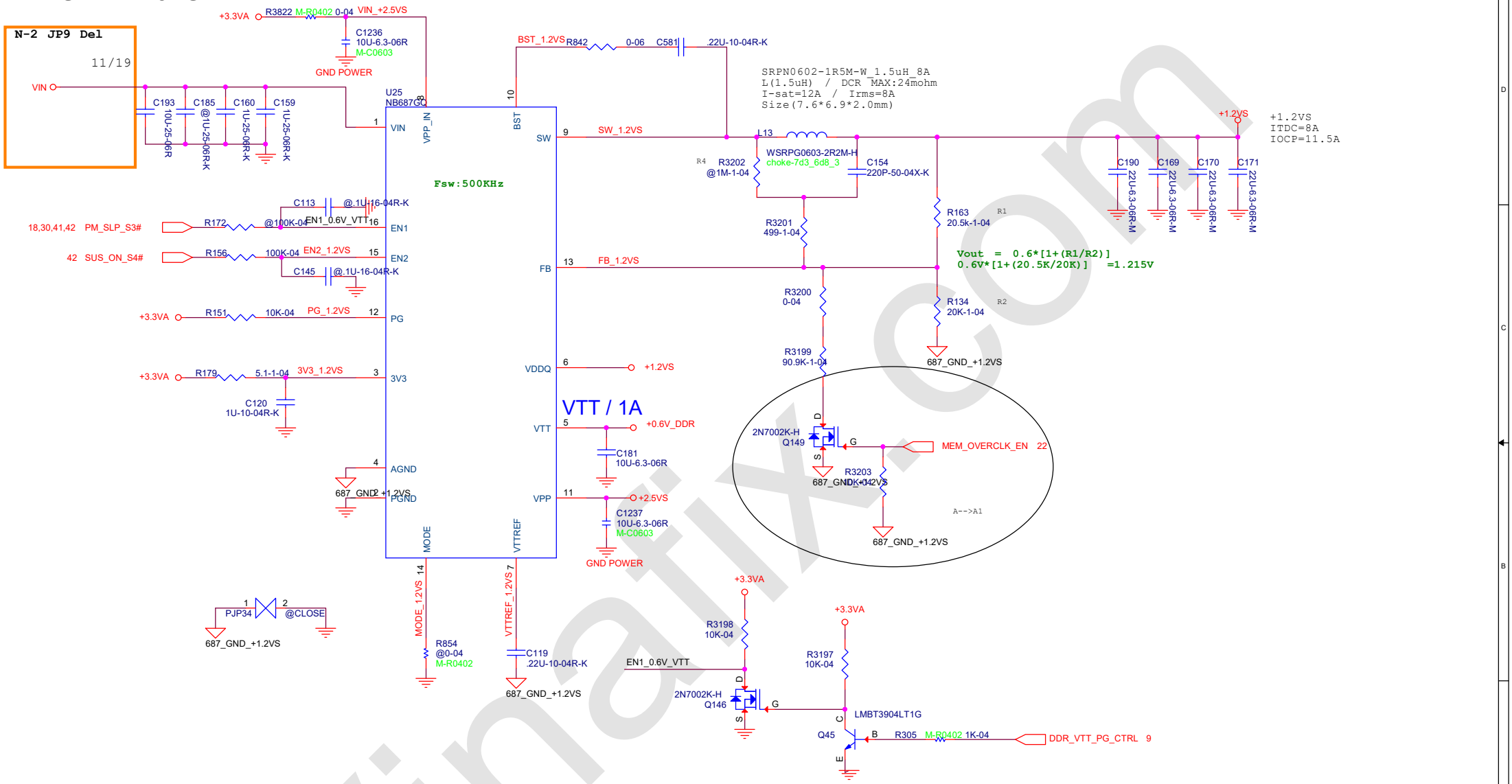
1.2VS/VTT/2.5VS



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Title: +1.2VS/+2.5VS		
Size: B	Document Number: GK7MR0R	Rev: V 1.0
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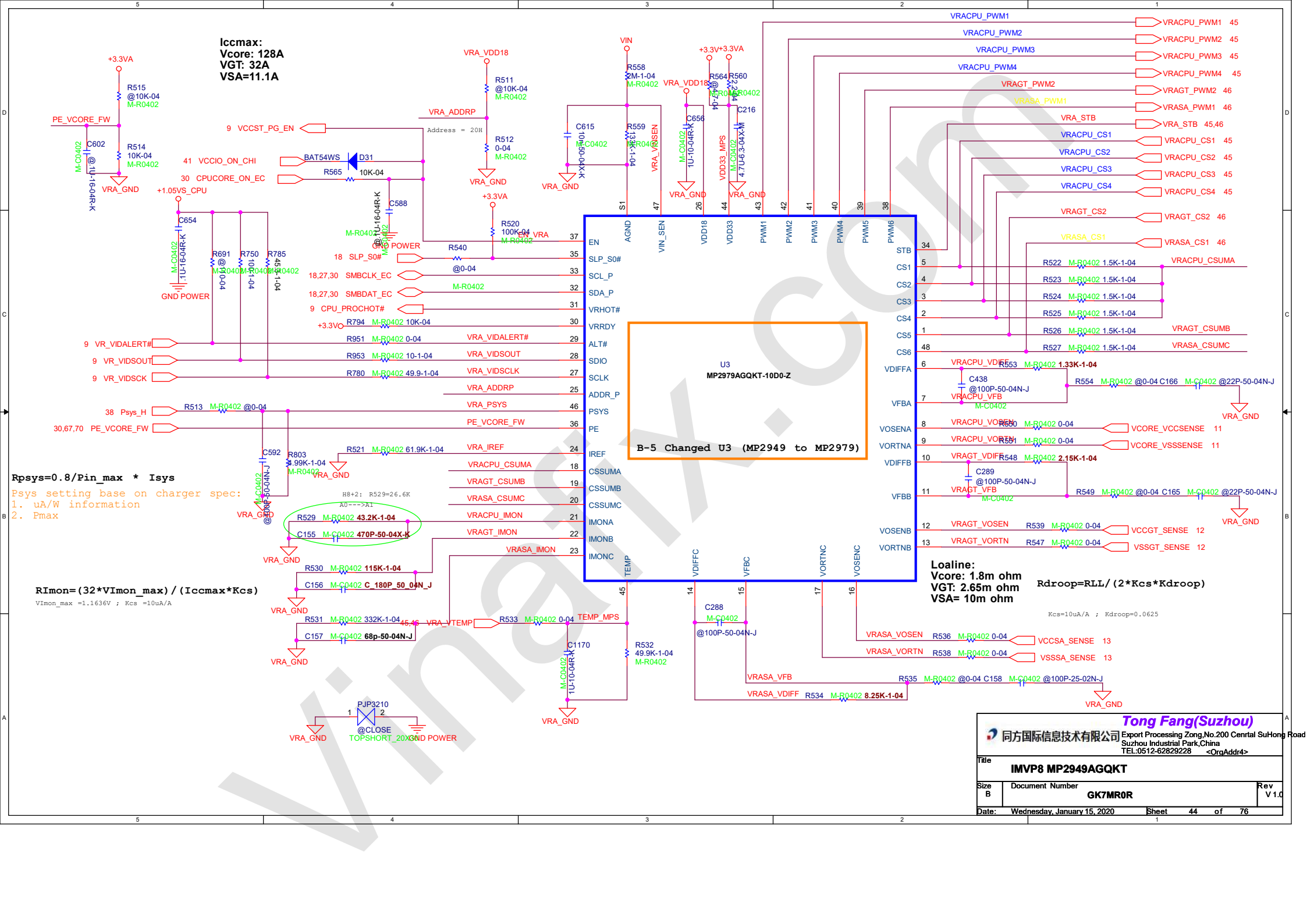
Iccmax:
Vcore: 128A
VGT: 32A
VSA=11.1A
U3
MP2979AGQKT-10D0-Z
B-5 Changed U3 (MP2949 to MP2979)
Rpsys=0.8/Pin_max * Isys
Psys setting base on charger spec:
1. uA/W information
2. Pmax
RImon=(32*VImon_max)/(Iccmax*Kcs)
VImon_max =1.1636V ; Kcs =10uA/A
Loaline:
Vcore: 1.8m ohm
VGT: 2.65m ohm
VSA= 10m ohm
Rdroop=RLL/(2*Kcs*Kdroop)
Kcs=10uA/A ; Kdroop=0.0625
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<OrgAddr4>
Title
IMVP8 MP2949AGQKT
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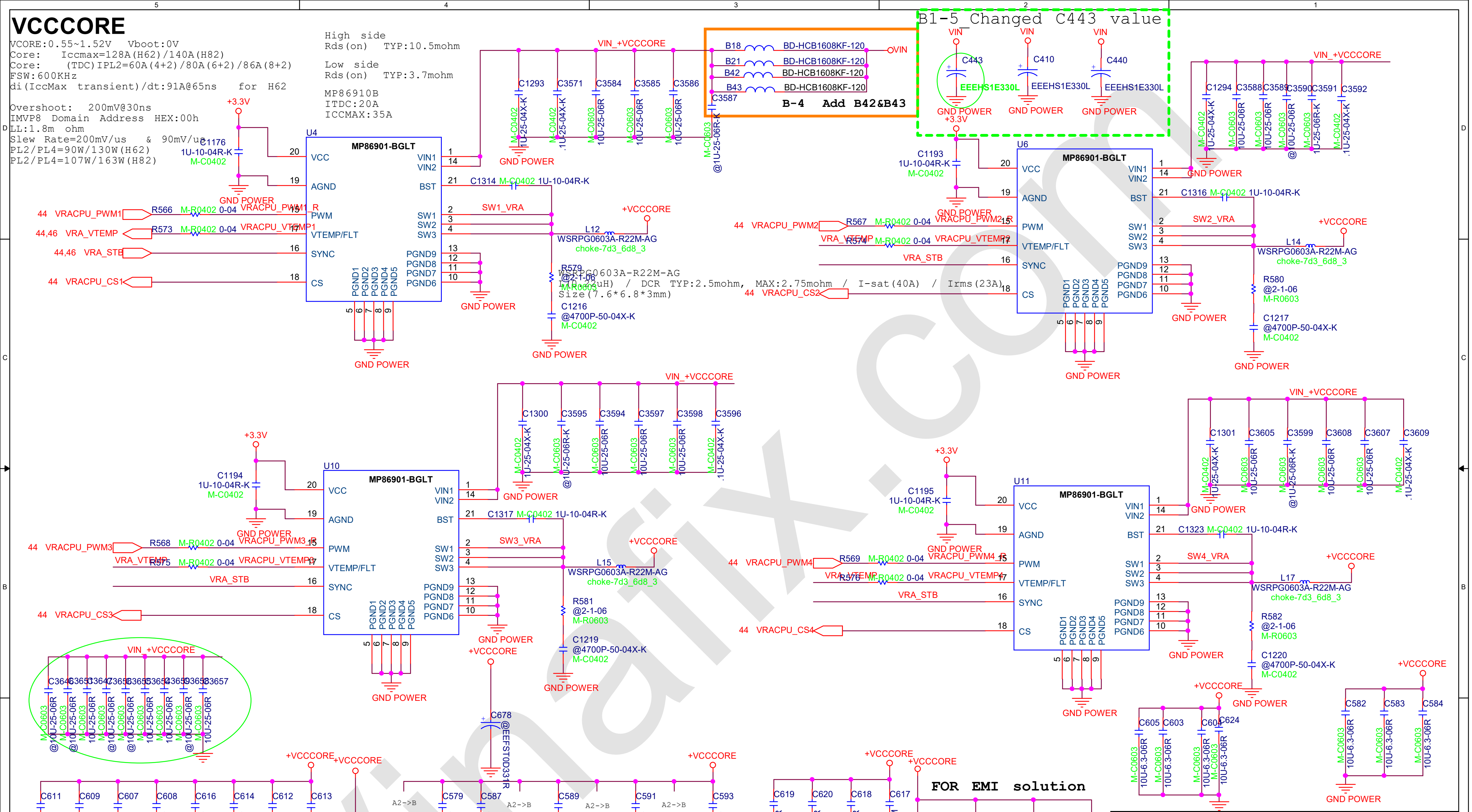
VCCCORE



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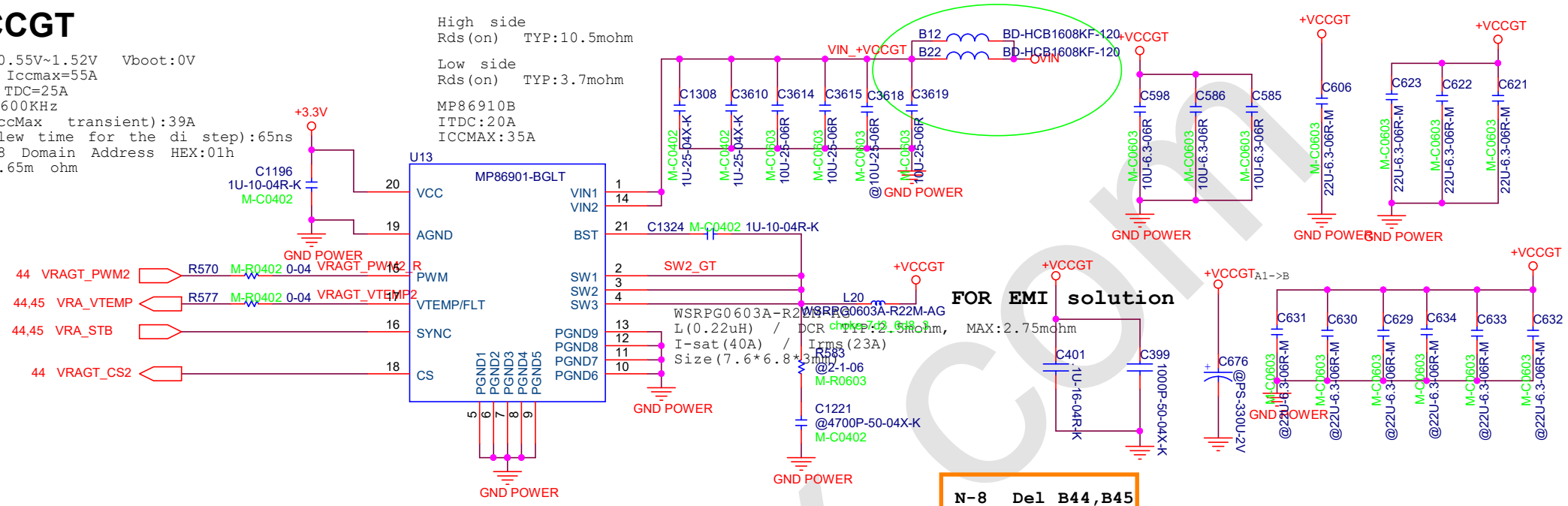
VCCGT

VGT:0.55V~1.52V Vboot:0V
GT: Iccmax=55A
GT: TDC=25A
FSW:600KHz
di(IccMax transient):39A
dt(Slew time for the di step):65ns
IMVP8 Domain Address HEX:01h
LL:2.65m ohm

High side
Rds(on) TYP:10.5mohm

Low side
Rds(on) TYP:3.7mohm

MP86910B
ITDC:20A
ICCMAX:35A



N-8 Del B44,B45

B-20 Add B44&B45 for VIN_VCCSA

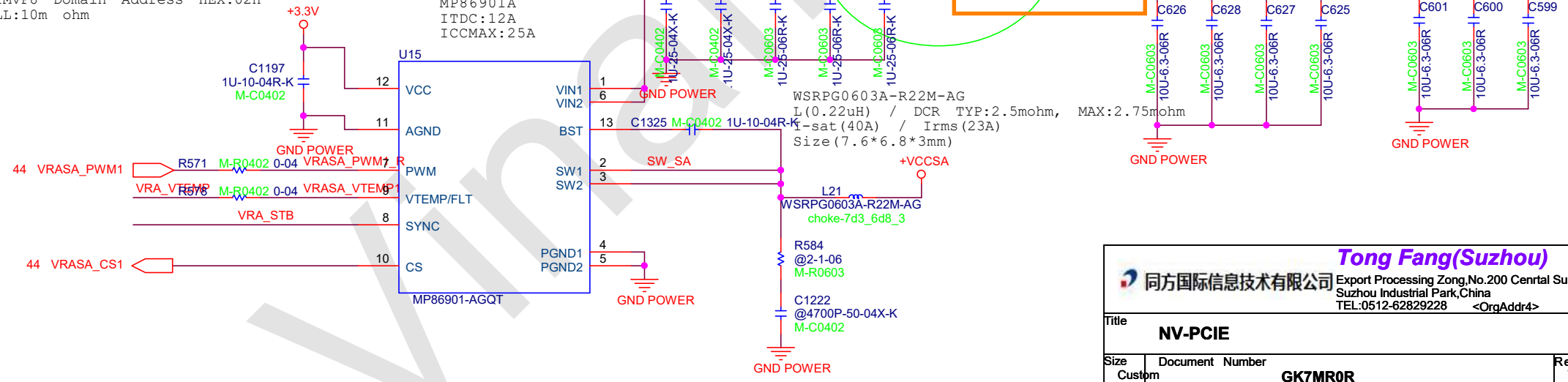
VCCSA

VCCSA:0.55~1.52V Vboot:1.05V
VCCSA: Iccmax=11.1A
VCCSA: TDC=10A
FSW:600KHz
di(IccMax transient):3A
dt(Slew time for the di step):200ns
IMVP8 Domain Address HEX:02h
LL:10m ohm

High side
Rds(on) TYP:19.5mohm

Low side
Rds(on) TYP:7.9mohm

MP86901A
ITDC:12A
ICCMAX:25A



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Title: NV-PCIE		
Size: Custom	Document Number: GK7MR0R	Rev: V 1.0
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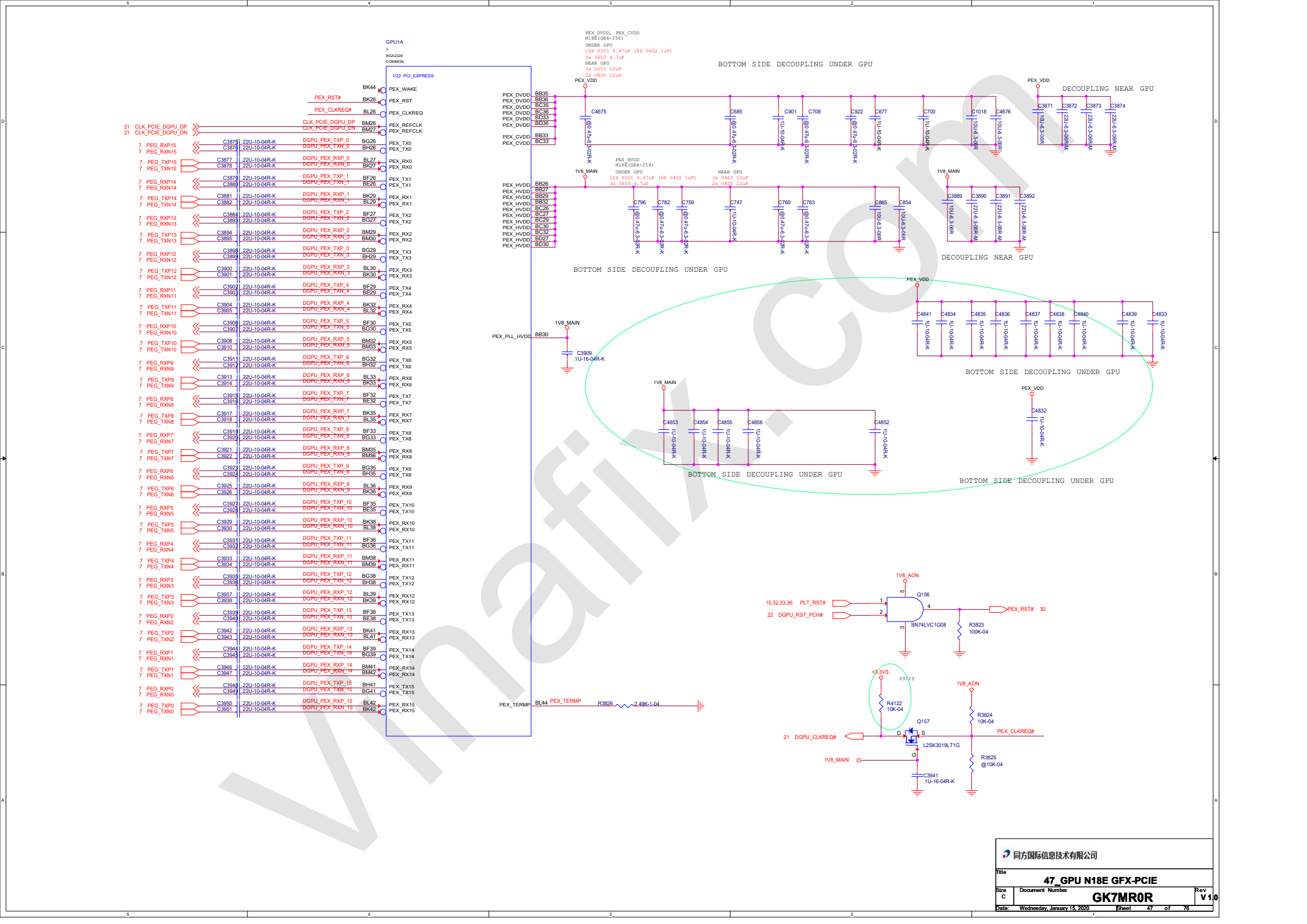

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Size C	Document Number GK7MR0R	Rev V1.0
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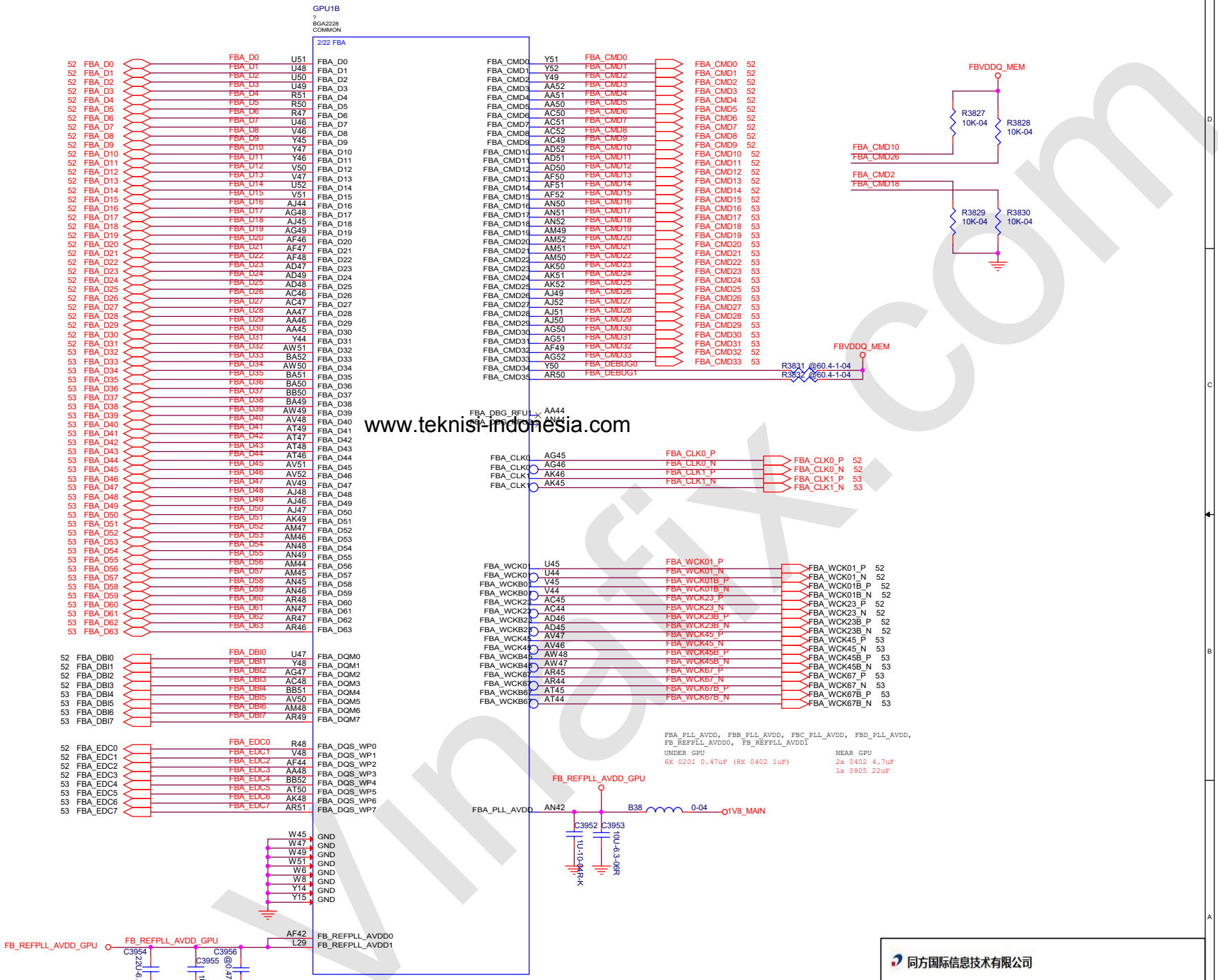
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BGA2228
COMMON
2/22 FBA
FBA_D0 U51
FBA_D1 U48
FBA_D2 U50
FBA_D3 U49
FBA_D4 R51
FBA_D5 R50
FBA_D6 R47
FBA_D7 U46
FBA_D8 V46
FBA_D9 Y45
FBA_D10 Y47
FBA_D11 Y46
FBA_D12 V50
FBA_D13 V47
FBA_D14 U52
FBA_D15 V51
FBA_D16 AJ44
FBA_D17 AG48
FBA_D18 AJ45
FBA_D19 AG49
FBA_D20 AF46
FBA_D21 AF47
FBA_D22 AF48
FBA_D23 AD47
FBA_D24 AD49
FBA_D25 AD48
FBA_D26 AC46
FBA_D27 AC47
FBA_D28 AA47
FBA_D29 AA46
FBA_D30 AA45
FBA_D31 Y44
FBA_D32 AW51
FBA_D33 BA52
FBA_D34 AW50
FBA_D35 BA51
FBA_D36 BA50
FBA_D37 BB50
FBA_D38 BA49
FBA_D39 AW49
FBA_D40 AV48
FBA_D41 AT49
FBA_D42 AT47
FBA_D43 AT48
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FBA_D46 AV52
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FBA_D50 AJ47
FBA_D51 AK49
FBA_D52 AM47
FBA_D53 AM46
FBA_D54 AN48
FBA_D55 AN49
FBA_D56 AM44
FBA_D57 AM45
FBA_D58 AN45
FBA_D59 AN46
FBA_D60 AR48
FBA_D61 AN47
FBA_D62 AR47
FBA_D63 AR46
FBA_DBI0 U47
FBA_DBI1 Y48
FBA_DBI2 AG47
FBA_DBI3 AC48
FBA_DBI4 BB51
FBA_DBI5 AV50
FBA_DBI6 AM48
FBA_DBI7 AR49
FBA_EDC0 R48
FBA_EDC1 V48
FBA_EDC2 AF44
FBA_EDC3 AA48
FBA_EDC4 BB52
FBA_EDC5 AT50
FBA_EDC6 AK48
FBA_EDC7 AR51
W45 GND
W47 GND
W49 GND
W51 GND
W6 GND
W8 GND
Y14 GND
Y15 GND
AF42 FB_REFPLL_AVDD0
L29 FB_REFPLL_AVDD1
FB_REFPLL_AVDD_GPU
C3954 22U-6.3-06R-M
C3955 1U-10-04R-K
C3956 @0.47u-6.3-02R-K
FBA_CMD0 Y51
FBA_CMD1 Y52
FBA_CMD2 Y49
FBA_CMD3 AA52
FBA_CMD4 AA51
FBA_CMD5 AA50
FBA_CMD6 AC50
FBA_CMD7 AC51
FBA_CMD8 AC52
FBA_CMD9 AC49
FBA_CMD10 AD52
FBA_CMD11 AD51
FBA_CMD12 AD50
FBA_CMD13 AF50
FBA_CMD14 AF51
FBA_CMD15 AF52
FBA_CMD16 AN50
FBA_CMD17 AN51
FBA_CMD18 AN52
FBA_CMD19 AM49
FBA_CMD20 AM52
FBA_CMD21 AM51
FBA_CMD22 AM50
FBA_CMD23 AK50
FBA_CMD24 AK51
FBA_CMD25 AK52
FBA_CMD26 AJ49
FBA_CMD27 AJ52
FBA_CMD28 AJ51
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FBA_CMD30 AG50
FBA_CMD31 AG51
FBA_CMD32 AF49
FBA_CMD33 AG52
FBA_DEBUG0 Y50
FBA_DEBUG1 AR50
FBVDDQ_MEM
R3827 10K-04
R3828 10K-04
R3829 10K-04
R3830 10K-04
R3831 @60.4-1-04
R3832 @60.4-1-04
FBA_DBG_RFU1 AA44
FBA_DBG_RFU2 AM43
FBA_CLK0 AG45
FBA_CLK0 AG46
FBA_CLK1 AK46
FBA_CLK1 AK45
FBA_CLK0_P
FBA_CLK0_N
FBA_CLK1_P
FBA_CLK1_N
FBA_WCK01 U45
FBA_WCK0 U44
FBA_WCKB01 V45
FBA_WCKB0 V44
FBA_WCK23 AC45
FBA_WCK2 AC44
FBA_WCKB23 AD46
FBA_WCKB2 AD45
FBA_WCK45 AV47
FBA_WCK4 AV46
FBA_WCKB45 AW48
FBA_WCKB4 AW47
FBA_WCK67 AR45
FBA_WCK6 AR44
FBA_WCKB67 AT45
FBA_WCKB6 AT44
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FBA_WCK01_N
FBA_WCK01B_P
FBA_WCK01B_N
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FBA_WCK23B_P
FBA_WCK23B_N
FBA_WCK45_P
FBA_WCK45_N
FBA_WCK45B_P
FBA_WCK45B_N
FBA_WCK67_P
FBA_WCK67_N
FBA_WCK67B_P
FBA_WCK67B_N
FBA_PLL_AVDD, FBB_PLL_AVDD, FBC_PLL_AVDD, FBD_PLL_AVDD,
FB_REFPLL_AVDD0, FB_REFPLL_AVDD1
UNDER GPU
6X 0201 0.47uF (8X 0402 1uF)
NEAR GPU
2x 0402 4.7uF
1x 0805 22uF
FB_REFPLL_AVDD_GPU
FBA_PLL_AVDD AN42
B38 0-04
1V8_MAIN
C3952 1U-10-04R-K
C3953 10U-6.3-06R
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Title
48_GPU N18E FrameBuffer A
Size Custom
Document Number GK7MR0R
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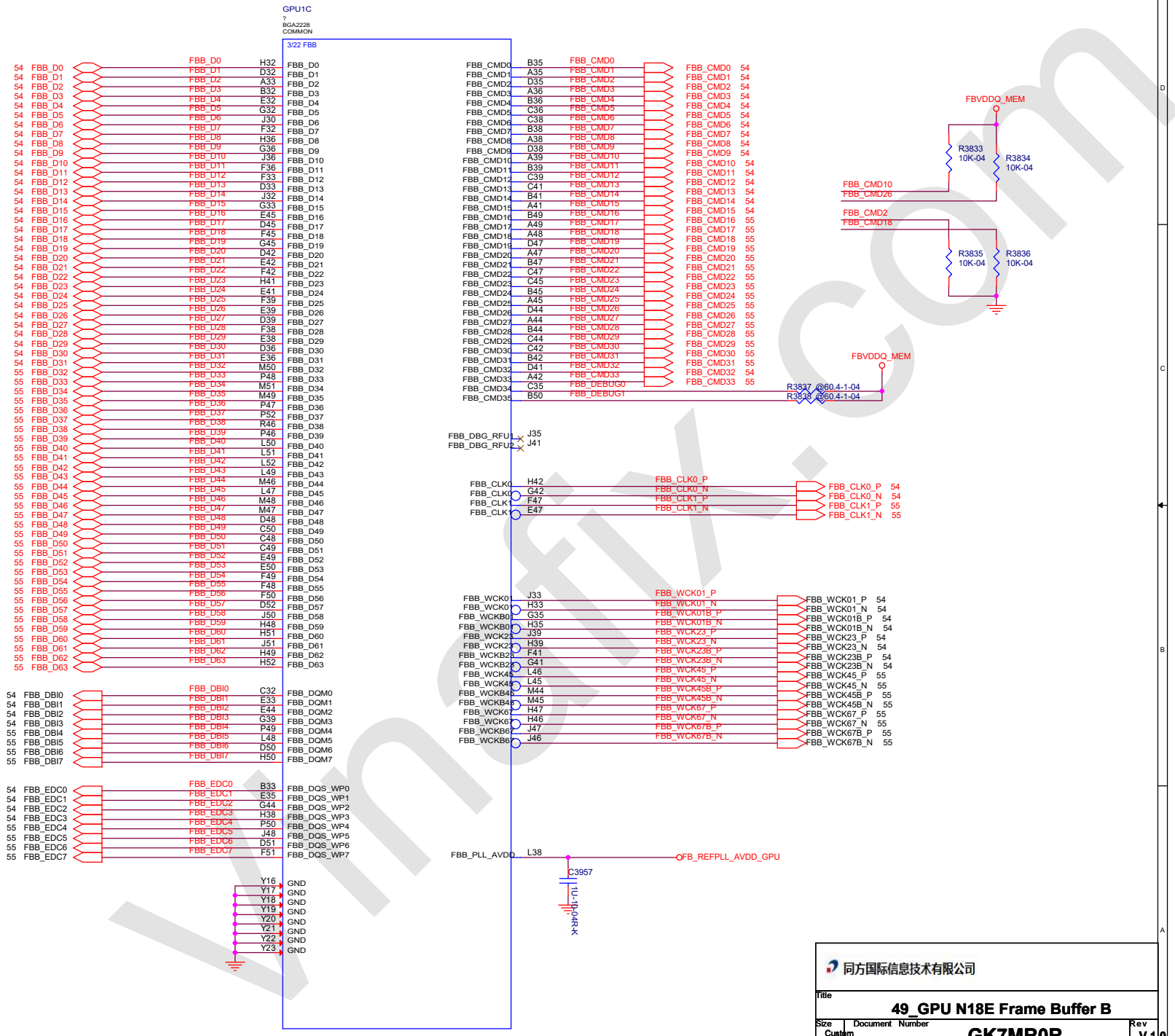
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FBB_D2 A33 FBB_D2
FBB_D3 B32 FBB_D3
FBB_D4 E32 FBB_D4
FBB_D5 G32 FBB_D5
FBB_D6 J30 FBB_D6
FBB_D7 F32 FBB_D7
FBB_D8 H36 FBB_D8
FBB_D9 G36 FBB_D9
FBB_D10 J36 FBB_D10
FBB_D11 F36 FBB_D11
FBB_D12 F33 FBB_D12
FBB_D13 D33 FBB_D13
FBB_D14 J32 FBB_D14
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FBB_D35 M49 FBB_D35
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FBB_D38 R46 FBB_D38
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FBB_D42 L52 FBB_D42
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FBB_D58 J50 FBB_D58
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FBB_D63 H52 FBB_D63
FBB_DBI0 C32 FBB_DQM0
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FBB_DBI2 E44 FBB_DQM2
FBB_DBI3 G39 FBB_DQM3
FBB_DBI4 P49 FBB_DQM4
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FBB_DBI6 D50 FBB_DQM6
FBB_DBI7 H50 FBB_DQM7
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FBB_EDC2 G44 FBB_DQS_WP2
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FBB_EDC6 D51 FBB_DQS_WP6
FBB_EDC7 F51 FBB_DQS_WP7
Y16 GND
Y17 GND
Y18 GND
Y19 GND
Y20 GND
Y21 GND
Y22 GND
Y23 GND
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FBB_CMD1 A35 FBB_CMD1
FBB_CMD2 D35 FBB_CMD2
FBB_CMD3 A36 FBB_CMD3
FBB_CMD4 B36 FBB_CMD4
FBB_CMD5 C36 FBB_CMD5
FBB_CMD6 C38 FBB_CMD6
FBB_CMD7 B38 FBB_CMD7
FBB_CMD8 A38 FBB_CMD8
FBB_CMD9 D38 FBB_CMD9
FBB_CMD10 A39 FBB_CMD10
FBB_CMD11 B39 FBB_CMD11
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FBB_CMD13 C41 FBB_CMD13
FBB_CMD14 B41 FBB_CMD14
FBB_CMD15 A41 FBB_CMD15
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FBB_CMD18 A48 FBB_CMD18
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FBB_CMD26 D44 FBB_CMD26
FBB_CMD27 A44 FBB_CMD27
FBB_CMD28 B44 FBB_CMD28
FBB_CMD29 C44 FBB_CMD29
FBB_CMD30 C42 FBB_CMD30
FBB_CMD31 B42 FBB_CMD31
FBB_CMD32 D41 FBB_CMD32
FBB_CMD33 A42 FBB_CMD33
FBB_CMD34 C35 FBB_DEBUG0
FBB_CMD35 B50 FBB_DEBUG1
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FBB_CMD1 54
FBB_CMD2 54
FBB_CMD3 54
FBB_CMD4 54
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FBB_CMD6 54
FBB_CMD7 54
FBB_CMD8 54
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FBB_CMD14 54
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FBB_CMD27 55
FBB_CMD28 55
FBB_CMD29 55
FBB_CMD30 55
FBB_CMD31 55
FBB_CMD32 54
FBB_CMD33 55
FBVDDQ_MEM
R3833 10K-04
R3834 10K-04
FBB_CMD10
FBB_CMD26
FBB_CMD2
FBB_CMD18
R3835 10K-04
R3836 10K-04
FBVDDQ_MEM
R3837 @60.4-1-04
R3838 @60.4-1-04
FBB_DBG_RFU1 J35
FBB_DBG_RFU2 J41
FBB_CLK0 H42 FBB_CLK0_P
FBB_CLK0 G42 FBB_CLK0_N
FBB_CLK1 F47 FBB_CLK1_P
FBB_CLK1 E47 FBB_CLK1_N
FBB_CLK0_P 54
FBB_CLK0_N 54
FBB_CLK1_P 55
FBB_CLK1_N 55
FBB_WCK01 J33 FBB_WCK01_P
FBB_WCK01 H33 FBB_WCK01_N
FBB_WCKB01 G35 FBB_WCK01B_P
FBB_WCKB01 H35 FBB_WCK01B_N
FBB_WCK23 J39 FBB_WCK23_P
FBB_WCK23 H39 FBB_WCK23_N
FBB_WCKB23 F41 FBB_WCK23B_P
FBB_WCKB23 G41 FBB_WCK23B_N
FBB_WCK45 L46 FBB_WCK45_P
FBB_WCK45 L45 FBB_WCK45_N
FBB_WCKB45 M44 FBB_WCK45B_P
FBB_WCKB45 M45 FBB_WCK45B_N
FBB_WCK67 H47 FBB_WCK67_P
FBB_WCK67 H46 FBB_WCK67_N
FBB_WCKB67 J47 FBB_WCK67B_P
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FBB_WCK01_P 54
FBB_WCK01_N 54
FBB_WCK01B_P 54
FBB_WCK01B_N 54
FBB_WCK23_P 54
FBB_WCK23_N 54
FBB_WCK23B_P 54
FBB_WCK23B_N 54
FBB_WCK45_P 55
FBB_WCK45_N 55
FBB_WCK45B_P 55
FBB_WCK45B_N 55
FBB_WCK67_P 55
FBB_WCK67_N 55
FBB_WCK67B_P 55
FBB_WCK67B_N 55
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FB_REFPLL_AVDD_GPU
C3957
1U-10n-04R-K
同方国际信息技术有限公司
Title
49_GPU N18E Frame Buffer B
Size Custom
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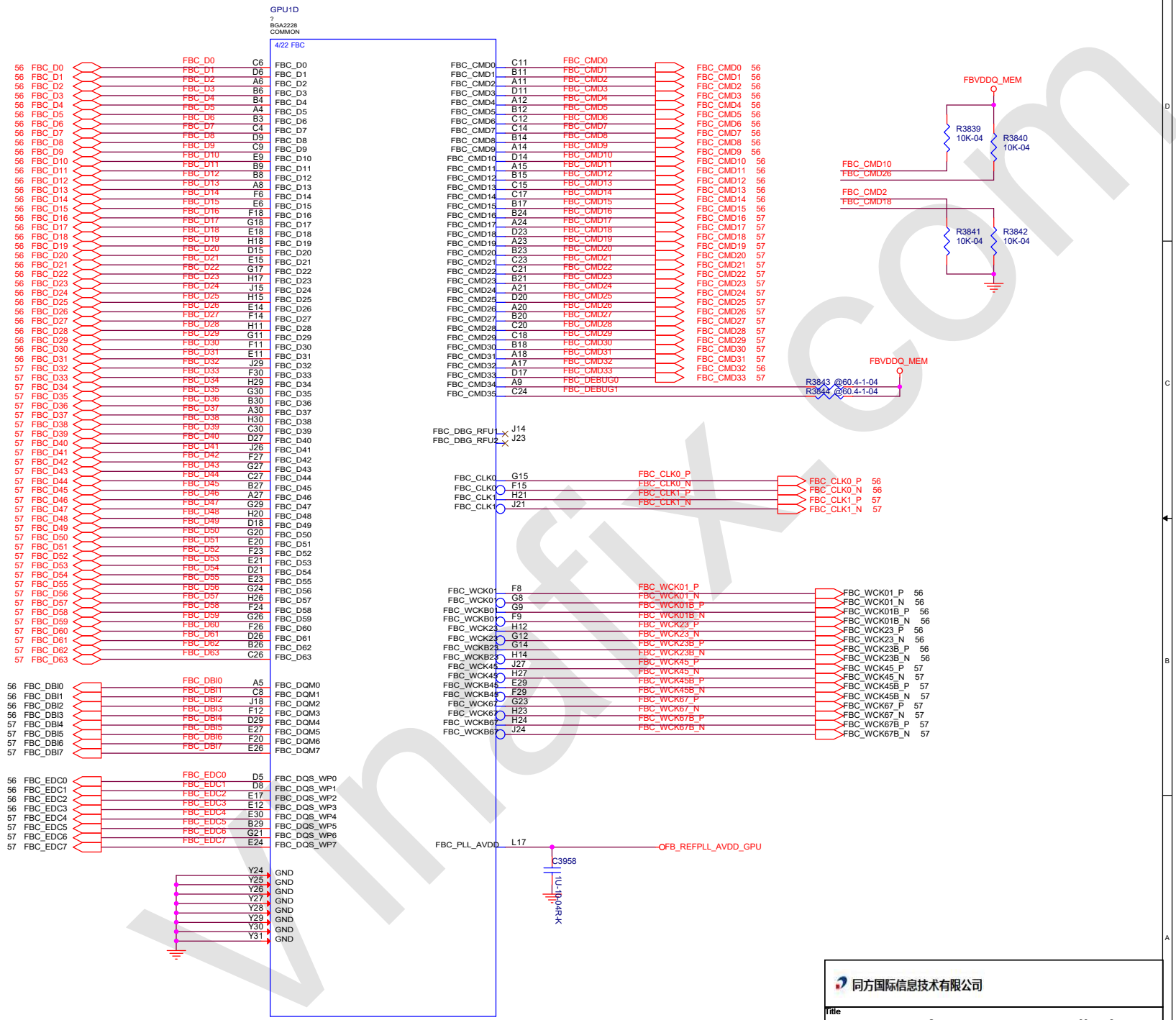

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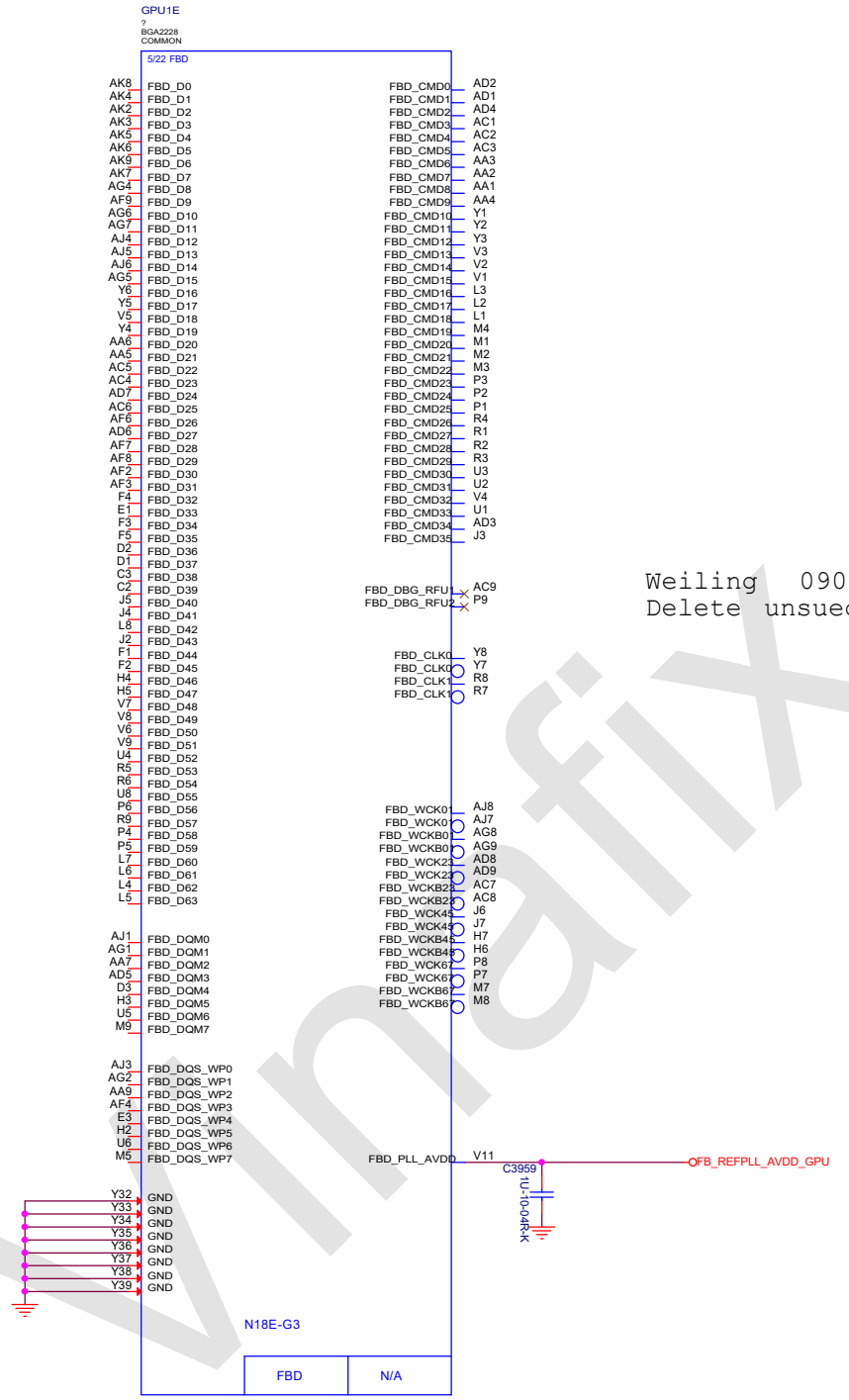
Title: 50_GPU N18E Frame Buffer C

Size: Custom | Document Number: GK7MR0R | Rev: V 1.0

Date: Wednesday, January 15, 2020 | Sheet 50 of 76



Weiling 0904
Delete unsued FBD partition

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Title: 51_GPU N18E Frame Buffer D

Size: Custom | Document Number: GK7MR0R | Rev: V 1.0

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MEM_FBA[31_0]

GDDR6: Maximum allowable case temp =95 degree

VRAM1A
VRAM1B
VRAM1C
VRAM1D

B-7 Changed C3961&C3962 value

BOTTOM SIDE DECOUPLING UNDER VRAM

DECOUPLING NEAR VRAM

Title	52_VRAM Frame Buffer A0
Size	C
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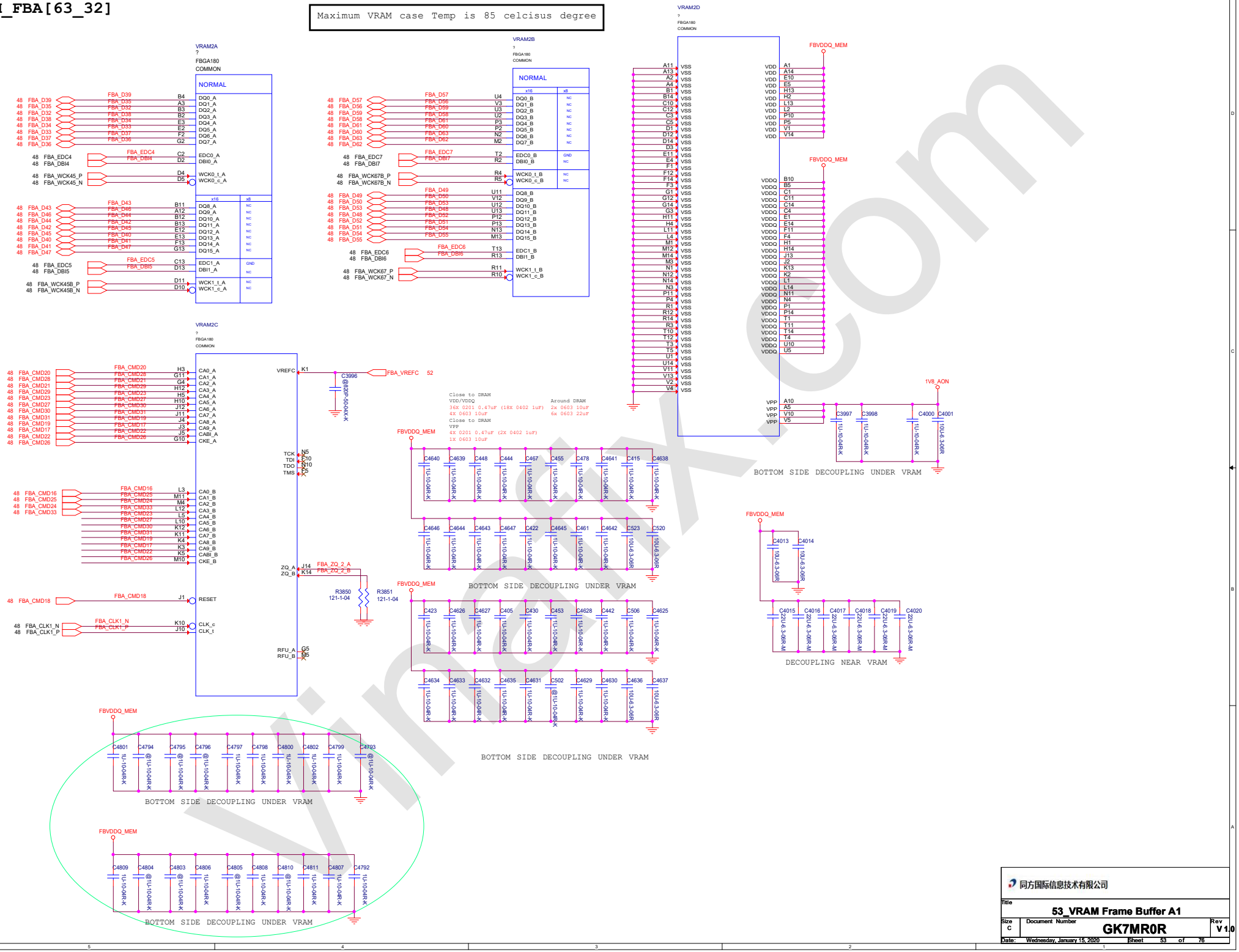
MEM_FBA[63_32]

Maximum VRAM case Temp is 85 celcisus degree



同方国际信息技术有限公司

Title	53_VRAM Frame Buffer A1	
Size C	Document Number GK7MR0R	Rev V1.0
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MEM_FBB[31_0]

Maximum VRAM case Temp is 85 celcisus degree

VRAM3A — NORMAL

VRAM3B — NORMAL

VRAM3C

VRAM3D

FBGA180 COMMON

FBVDDQ_MEM

B-6 Changed C4034&C4035 Value

1V8_AON

BOTTOM SIDE DECOUPLING UNDER VRAM

DECOUPLING NEAR VRAM

Close to DRAM
VDD/VDDQ
36X 0201 0.47uF (18X 0402 1uF)
4X 0603 10uF
Close to DRAM
VPP
4X 0201 0.47uF (2X 0402 1uF)
1X 0603 10uF

Around DRAM
2x 0603 10uF
6x 0603 22uF

同方国际信息技术有限公司	
Title	54_VRAM Frame Buffer B0
Size C	Document Number GK7MR0R
Rev	V 1.0
Date:	Wednesday, January 15, 2020
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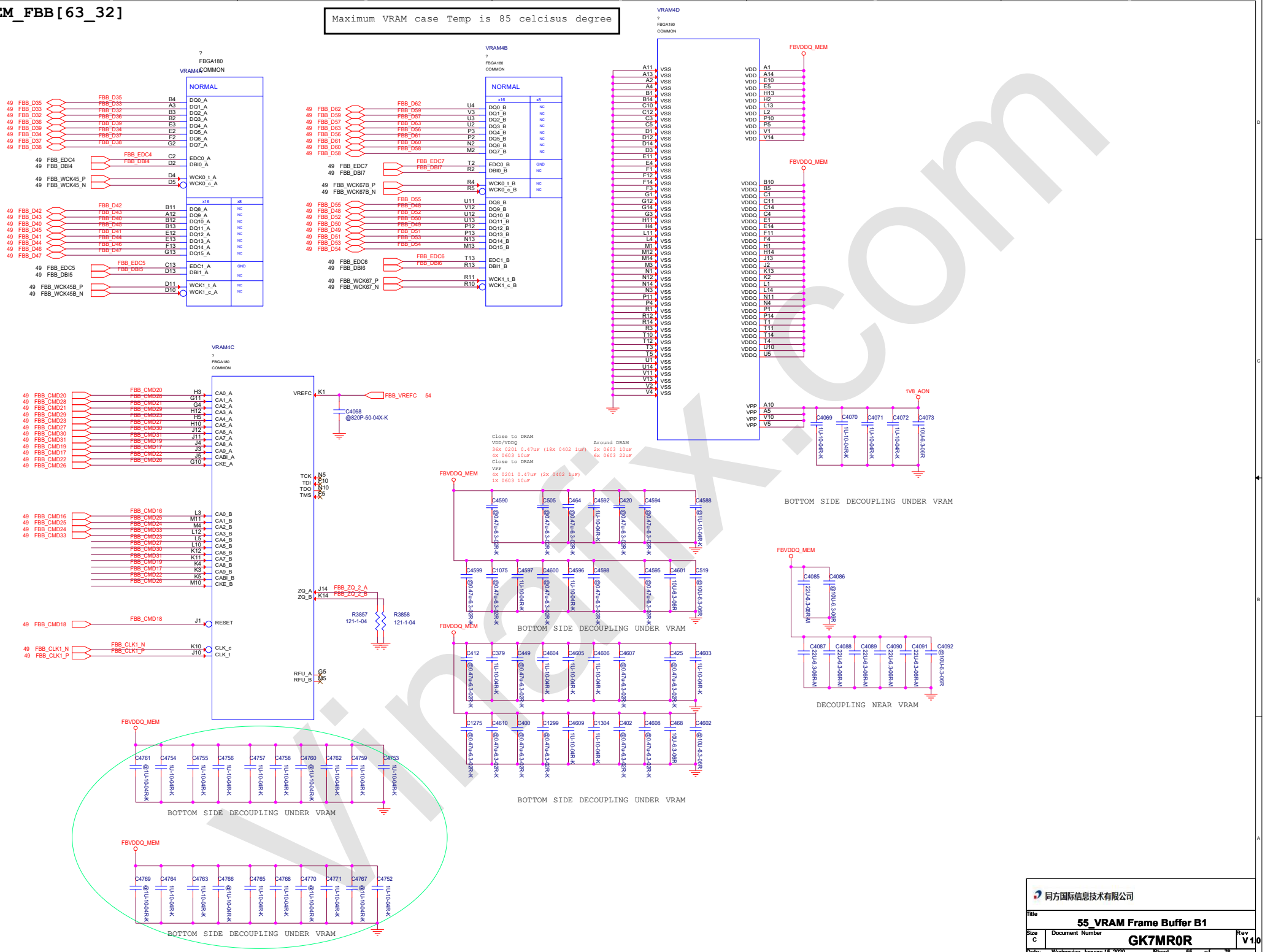
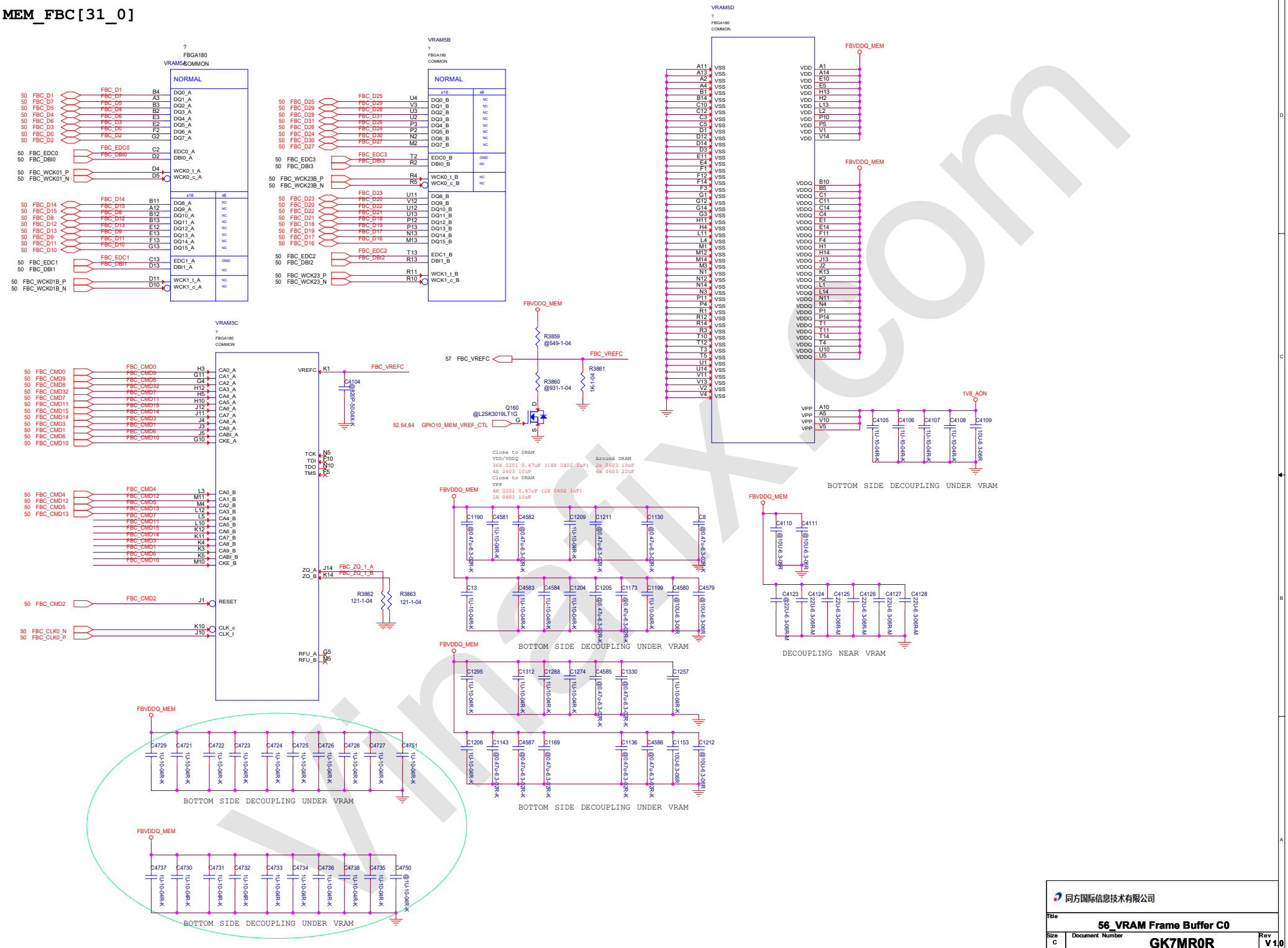
MEM_FBB[63_32]

Maximum VRAM case Temp is 85 celcisus degree



同方国际信息技术有限公司			
Title	55_VRAM Frame Buffer B1		
Size C	Document Number GK7MR0R		Rev V1.0
Date: Wednesday, January 15, 2020	Sheet 55 of 76		

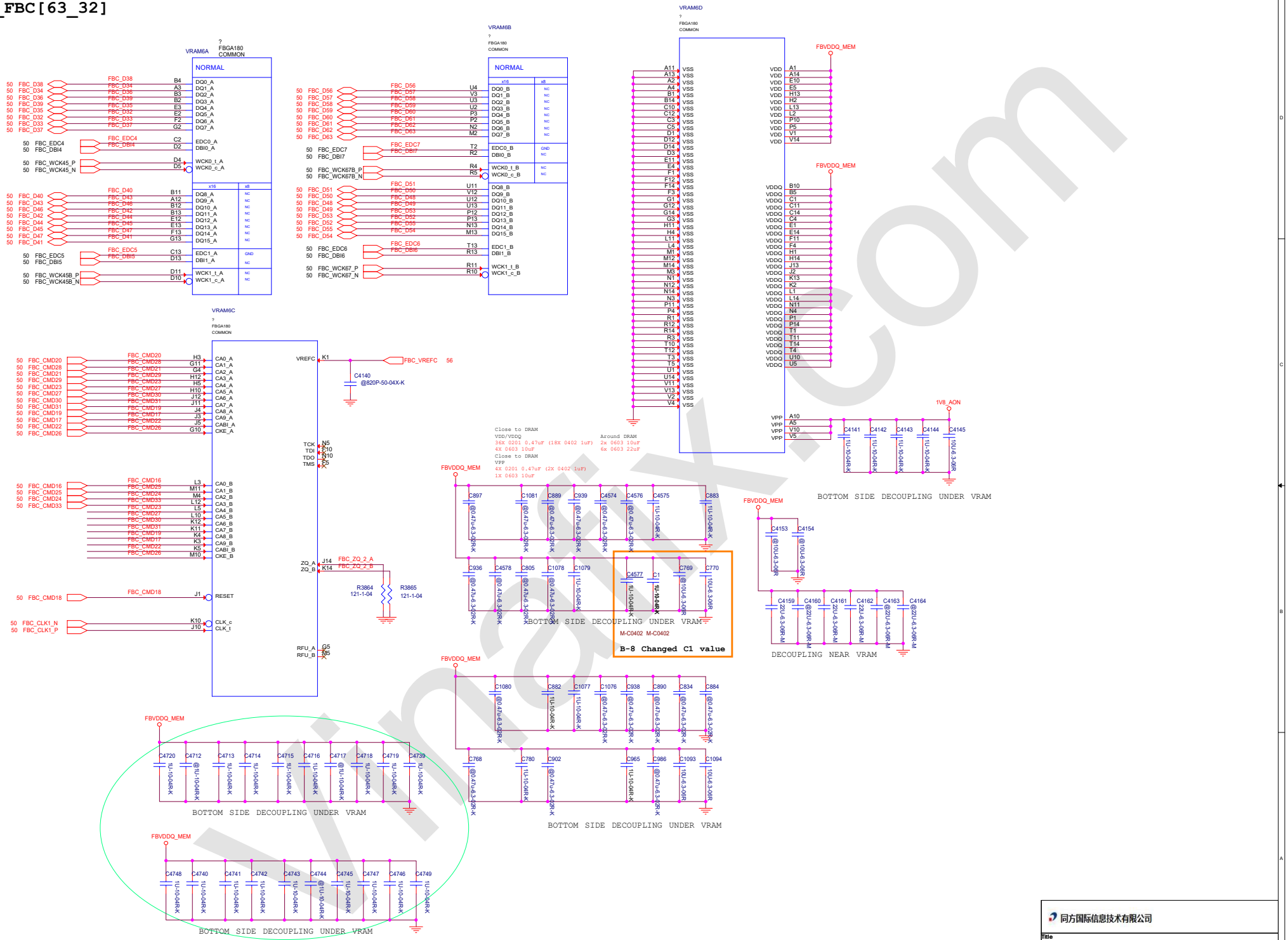
MEM_FBC[31_0]



同方国际信息技术有限公司

Title	56_VRAM Frame Buffer C0	
Size C	Document Number GK7MR0R	Rev V 1.0
Date: Wednesday, January 15, 2020	Sheet 56 of 76	

MEM_FBC[63_32]



同方国际信息技术有限公司

Title	57_VRAM Frame Buffer C1	
Size C	Document Number GK7MR0R	Rev V1.0
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MEM_FBD[31_0]

Weiling 0904
Delete VRAM due to G1
 only supporting 192bits

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Title: 58_VRAM Frame Buffer D0

Size: Custom | Document Number: GK7MR0R | Rev: V1.0

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MEM_FBC[63_32]

Weiling 0904
Delete VRAM due to G1
 only supporting 192bits

同方国际信息技术有限公司

Title: 59_VRAM Frame Buffer D1

Size: Custom | Document Number: GK7MR0R | Rev: V1.0

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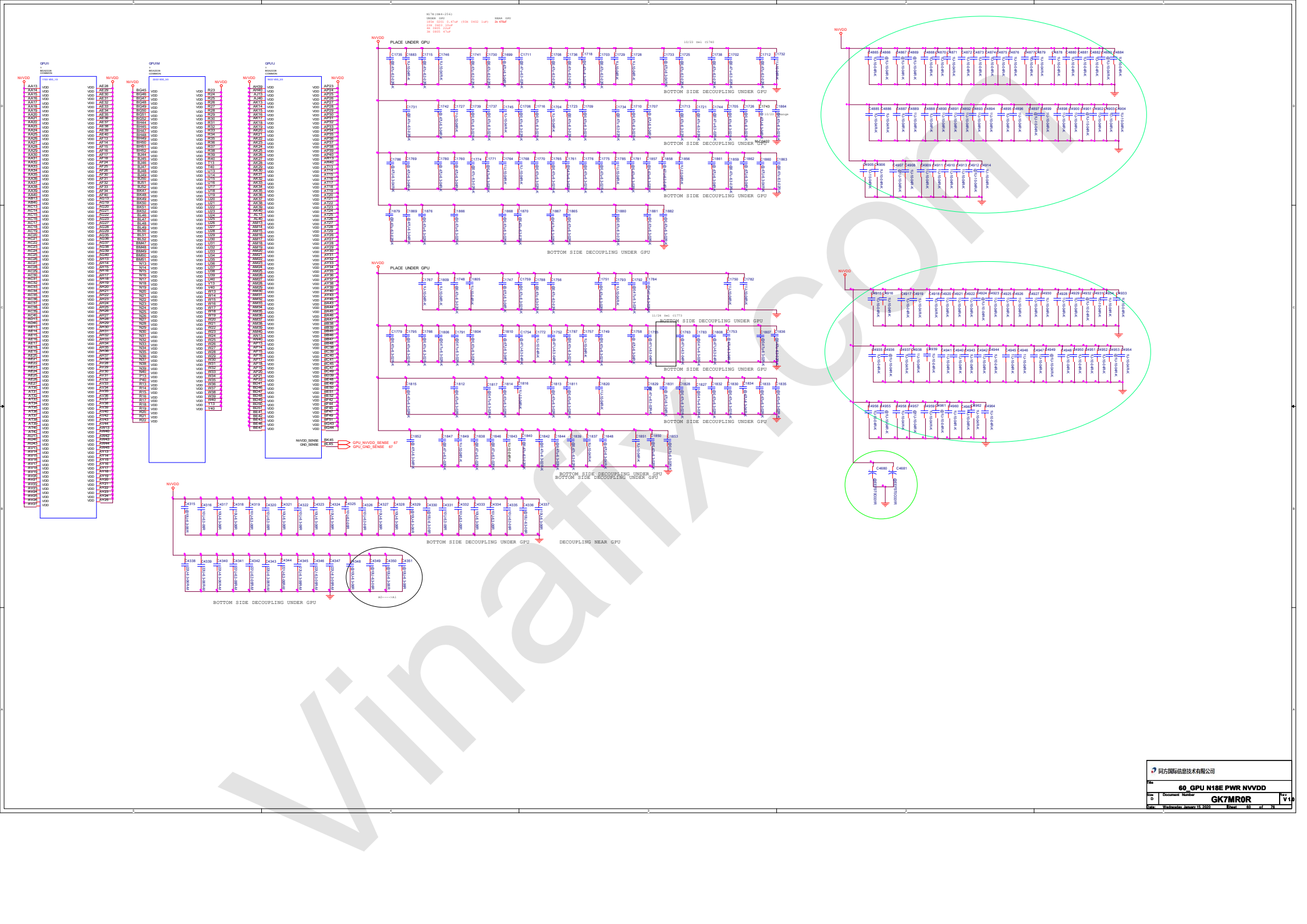

同方国际信息技术有限公司

File	60_GPU N18E PWR NVVDD	
Size D	Document Number GK7MR0R	Rev V1.0
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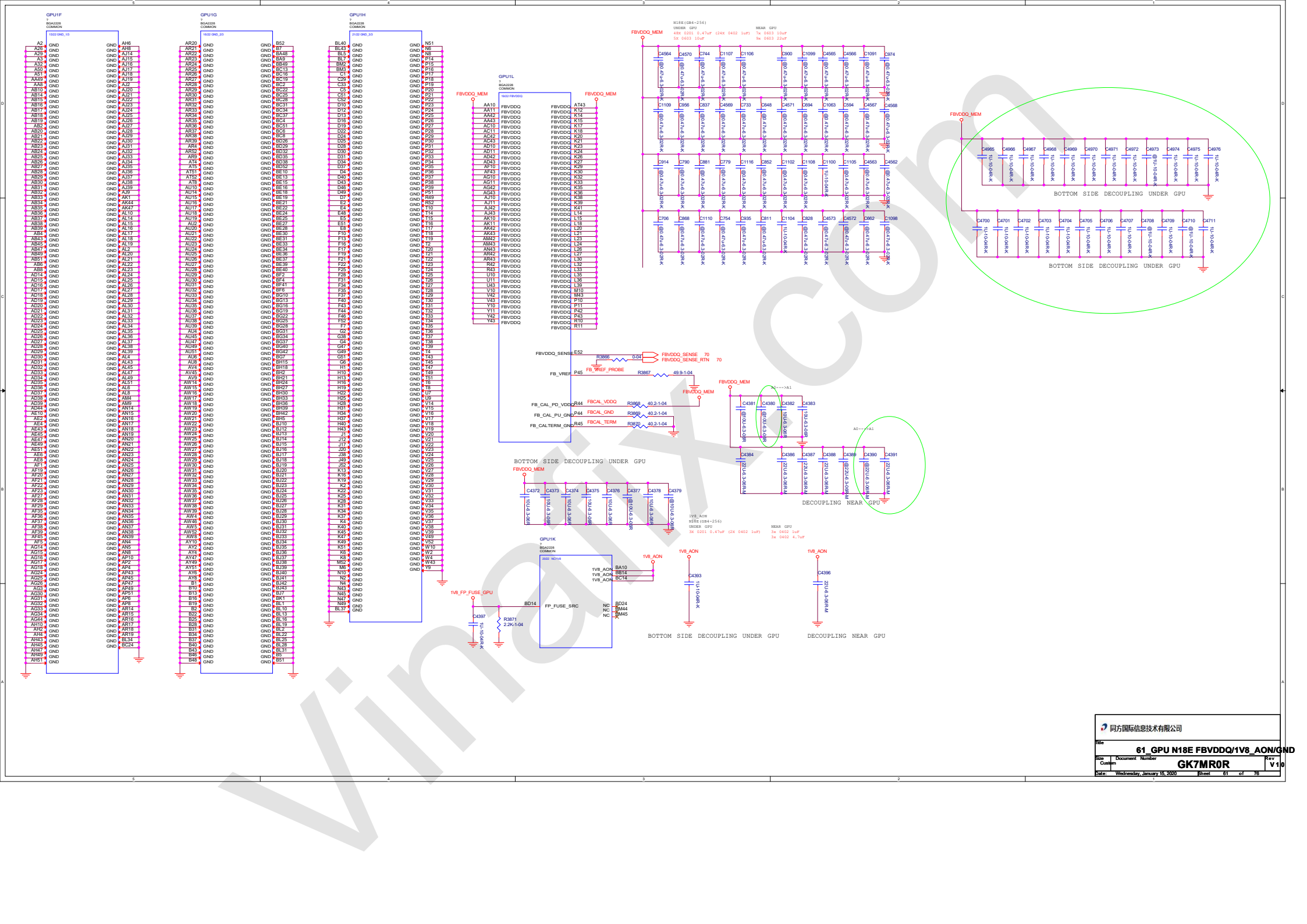

同方国际信息技术有限公司

Title	61_GPU N18E FBVDDQ/1V8_AON/GND		
Size: Custom	Document Number: GK7MR0R		Rev: V 1.0
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Hardware Design Guide Page282:
For IFPA/B/C/D/E/F
If an IFP link is not used, it should be NC
including power rail and signal and references
associated with LINKX

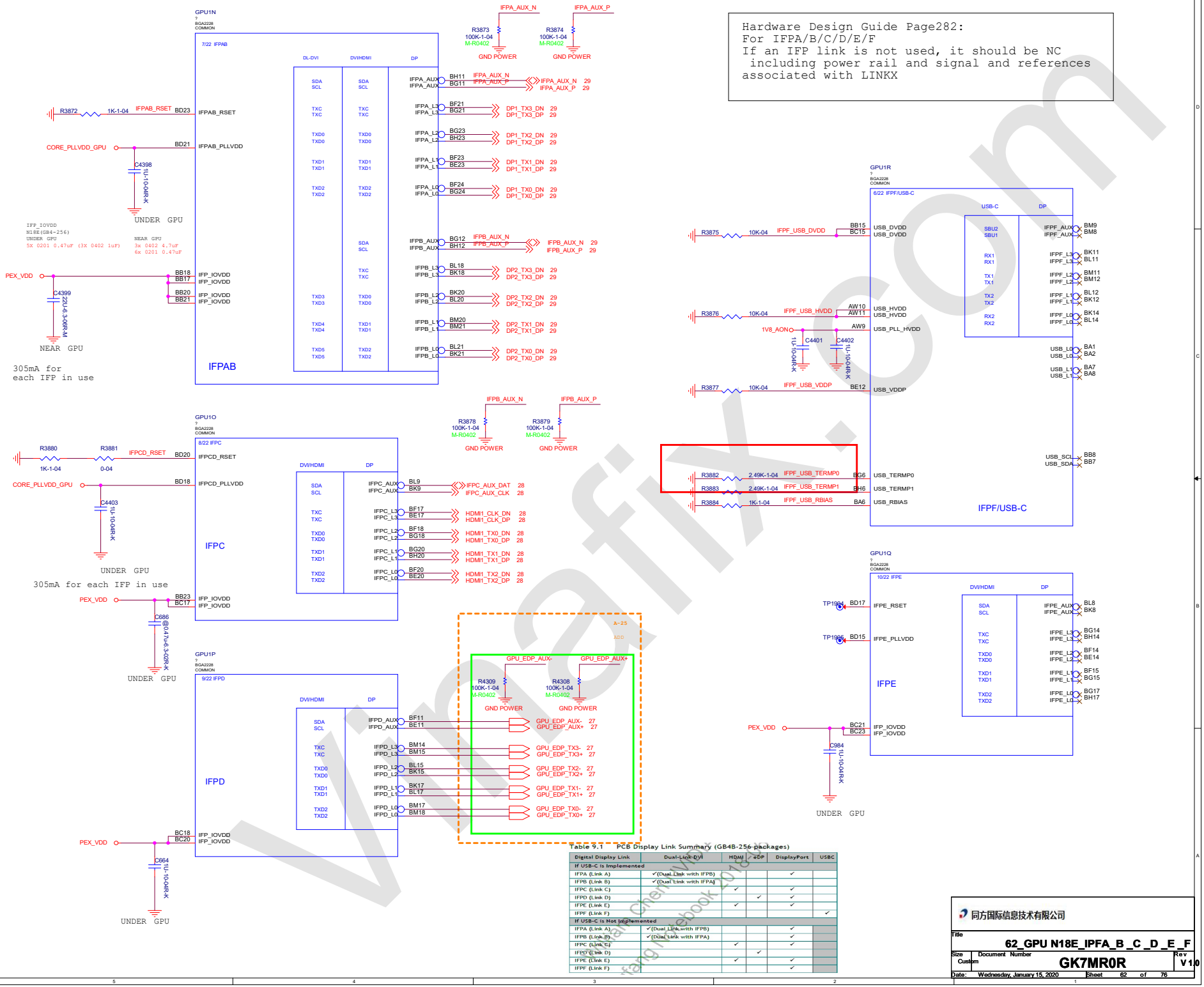

Table 9.1 PCB Display Link Summary (GB4B-256 packages)

Digital Display Link	Dual-Link DVI	HDMI	eDP	DisplayPort	USBC
If USB-C is Implemented					
IFPA (Link A)	✓(Dual Link with IFPB)			✓	
IFPB (Link B)	✓(Dual Link with IFPA)				
IFPC (Link C)		✓		✓	
IFPD (Link D)			✓	✓	
IFPE (Link E)		✓		✓	
IFPF (Link F)					✓
If USB-C is Not Implemented					
IFPA (Link A)	✓(Dual Link with IFPB)			✓	
IFPB (Link B)	✓(Dual Link with IFPA)			✓	
IFPC (Link C)		✓		✓	
IFPD (Link D)			✓		
IFPE (Link E)		✓		✓	
IFPF (Link F)				✓	

同方国际信息技术有限公司

Title	62_GPU N18E_IPFA_B_C_D_E_F	
Size: Custom	Document Number: GK7MR0R	Rev: V1.0
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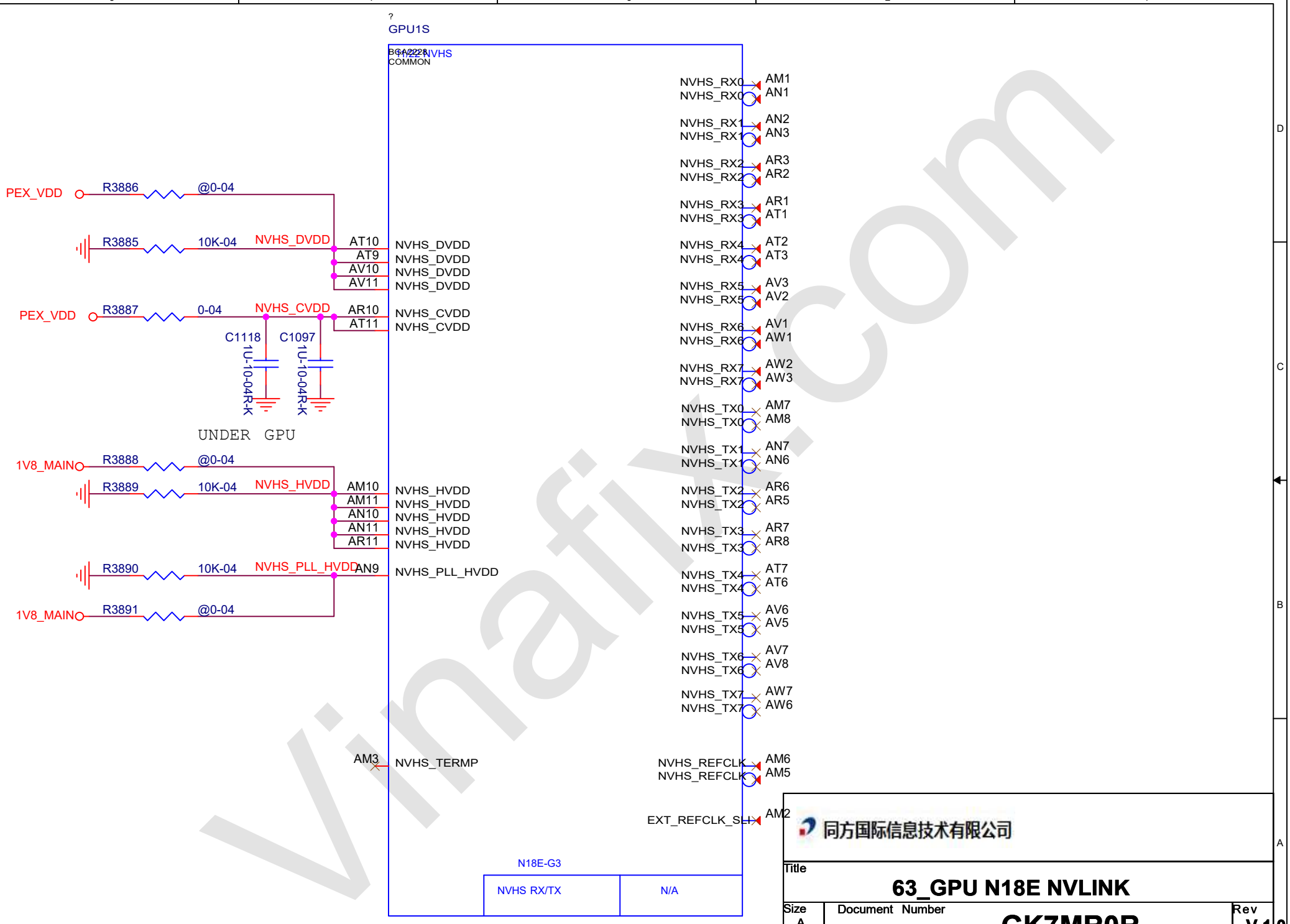

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Title: 63_GPU N18E NVLINK

Size	Document Number	Rev
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B1-4_Changed power plane 1V8_AON to +3.3V_LCD

B-19 R4354, R4355 unstuff

I2CS: Slave
I2CC: Master and NV Use only
I2CB: Master and for Partner use

GPU1T
BGA2228
COMMON

12/22 MISC 1

11/24 Changed

11/19

A-27
ADD

MTDK5S6R
VGS(th) max=+1.5V

Title	64_GPU N18E GPIO/Thermal/I2C
Size	Custom
Document Number	GK7MR0R
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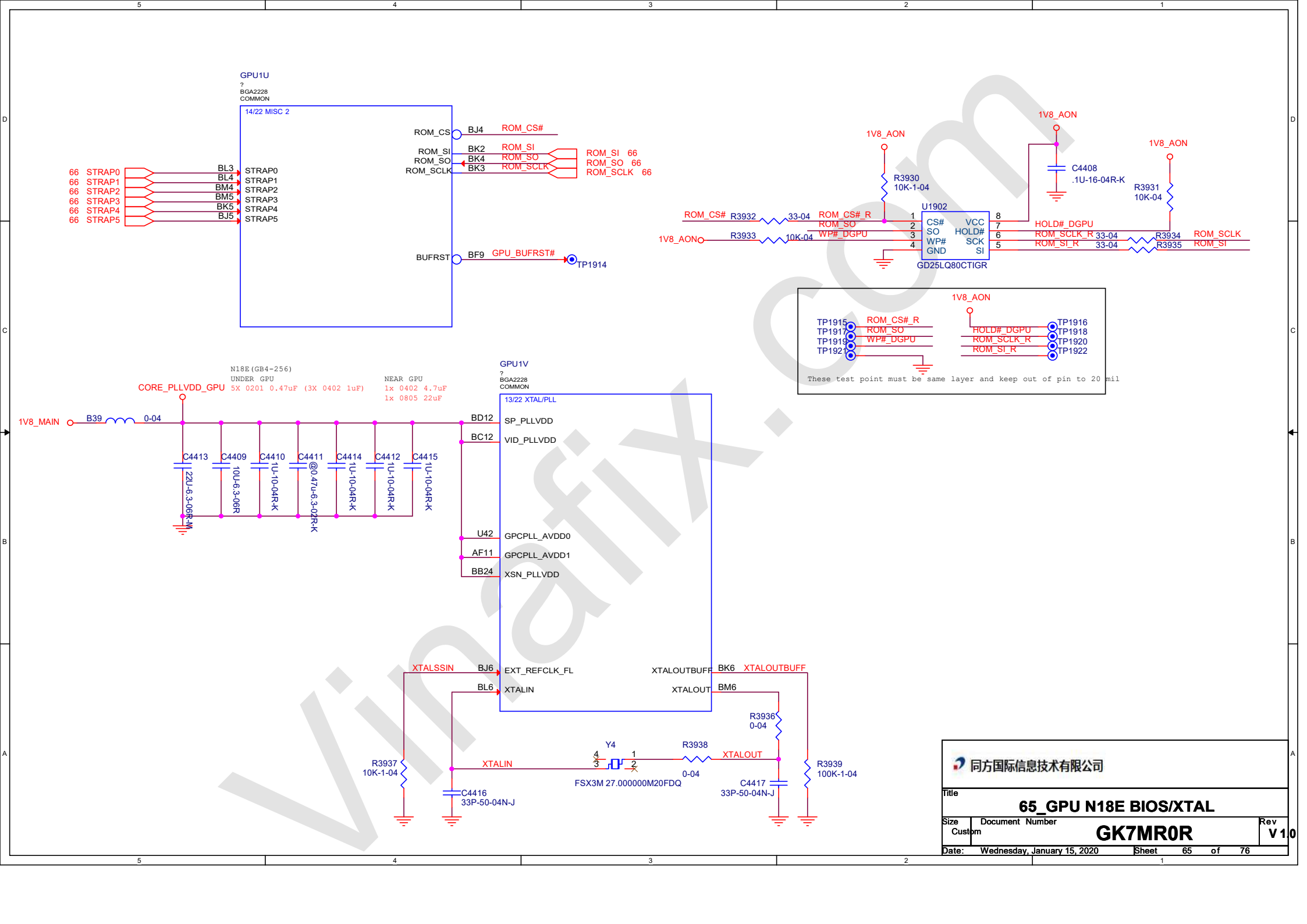

同方国际信息技术有限公司

Title: 65_GPU N18E BIOS/XTAL

Size: Custom | Document Number: GK7MR0R | Rev: V 1.0

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Voltage (V)			
LEVEL	Min	Normal	Max
H	1.5	1.8	1.854
M	0.5	0.9	1.3
L	0	0	0.3
Invalid	1.3V<pin voltage<1.5V		
	0.3V<pin voltage<0.5V		

Table 11.4 FS_OVERT* Strap Enablement

Strap Pins see Note			FS_OVERT* Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function ENABLED
L	L	H	FS_OVERT* function DISABLED (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Note that configurations other than the two listed in Table 11.4 must be avoided, as otherwise damage to strap inputs may result.

For N18x GPUs the hardware (on-PCB) SOR_EXPOSED straps are redacted; ROM_SO, ROM_SI and ROM_SCLK straps are no longer provided. The register-based method for configuring audio for display links is the only method provided. This method is implemented in VBIOS settings.

Based on RVL_07916_001_V10 JUNE 2017

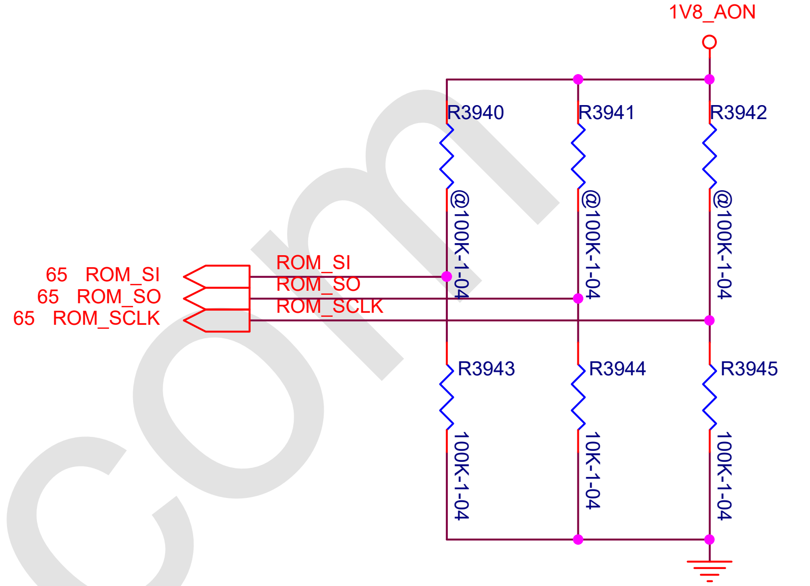
GDDR5						
Density	Vendor	Part Number	Strap	Strap 2	Strap 1	Strap 0
8Gb	Samsung	K4Z80325BC-HC14 C-die	0X0	L	L	L
8Gb	Micron	MT61K256M32JE-14:A A-die	0X1	L	L	H
8Gb	Hynix	H56C8H24MJR-S4C M-die	0X2	L	H	L
4Gb	Samsung		0X7	H	H	H
4Gb	Hynix		0X6	H	H	L
4Gb	Micron					

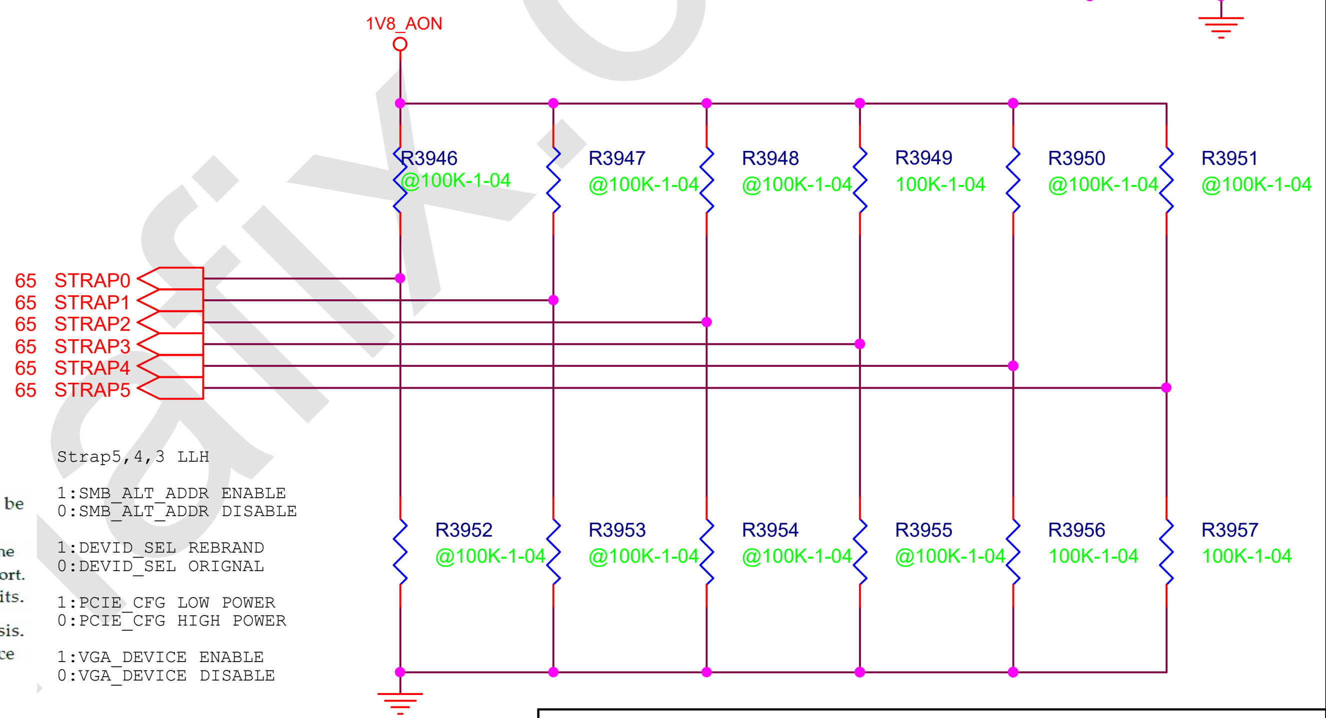
POWER

1.25V/1.35V

1.25V/1.35V

1.25V/1.35V N18E-G2 only





Strap5,4,3 LLH

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

- **SMB_ALT_ADDR Enable:** This strap function allows an alternate SMBus address to be configured, so that graphics circuits with multiple GPUs can have separate SMBus connections for each GPU. In dual GPU configurations, use of the alternate address on one GPU (by setting this function to ‘1’) avoids conflicts between the two GPUs on an SMBUS port. The “SMB_ALT_ADDR disabled” setting (‘0’) is correct for single-GPU graphics circuits.
- **DEVID_SEL:** NVIDIA defines an original and a re-brand Device ID on a per-GPU basis. This Device ID Select strap function allows selection between the original PCIe Device ID defined for the GPU (via a function setting of ‘0’), and the alternate “re-brand” Device ID defined for the GPU (via a function setting of ‘1’).
- **PCIE_CFG:** This function sets electrical characteristics of PCIe lanes, in particular signal amplitude (swing). A setting of ‘0’ selects normal (full) signal swing. N18x graphics circuits should strap for this setting. (A setting of ‘1’ designates reduced signal amplitude, available if special concerns require. Consult NVIDIA for guidance.)
- **VGA_DEVICE:** This strap function is used to report the graphics circuit either as a 3D device (class code 302, designated by a setting of ‘0’ for this strap) or as a VGA device (class code 300, designated by a setting of ‘1’) to the host system. The 3D Device (class code 302, strap=‘0’) setting is correct for most MS-Hybrid notebook GeForce graphics circuits (consult NVIDIA for details on proper bit setting for MS-Hybrid solutions).

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Title	66_GPU N18E STRAP
Size A	Document Number GK7MR0R
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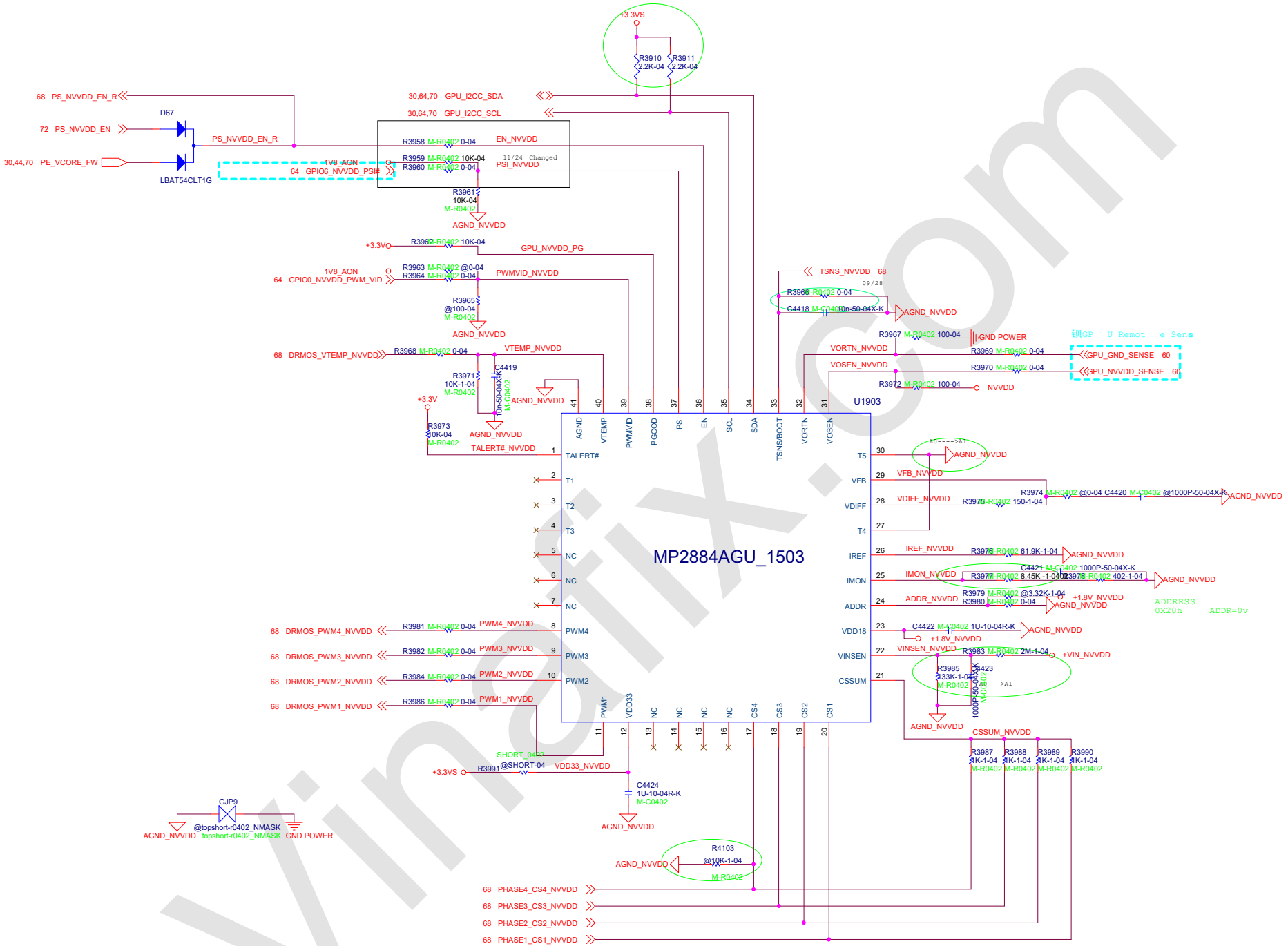

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Title: 67_POWER N18E NVVDD CONTROLLER

Size: Custom | Document Number: GK7MR0R | Rev: V 1.0

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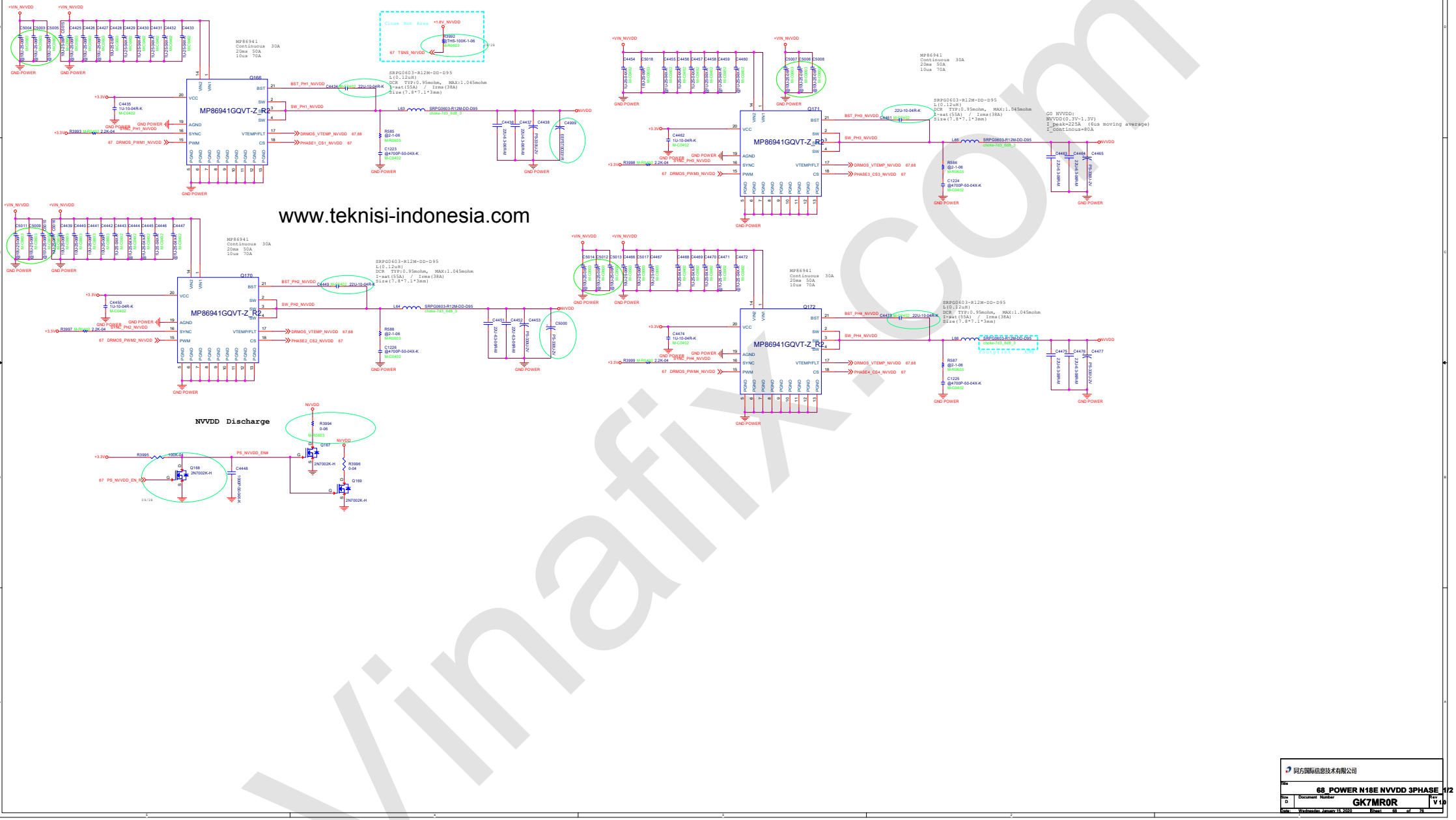

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Title	68_POWER N18E NVVDD 3PHASE_1/2		
Size: D	Document Number: GK7MR0R		Rev: V1.0
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Del Q16, Q21

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Title: 69_POWER N18E NVVDD 3PHASE_2/2

Size	Document Number	Rev
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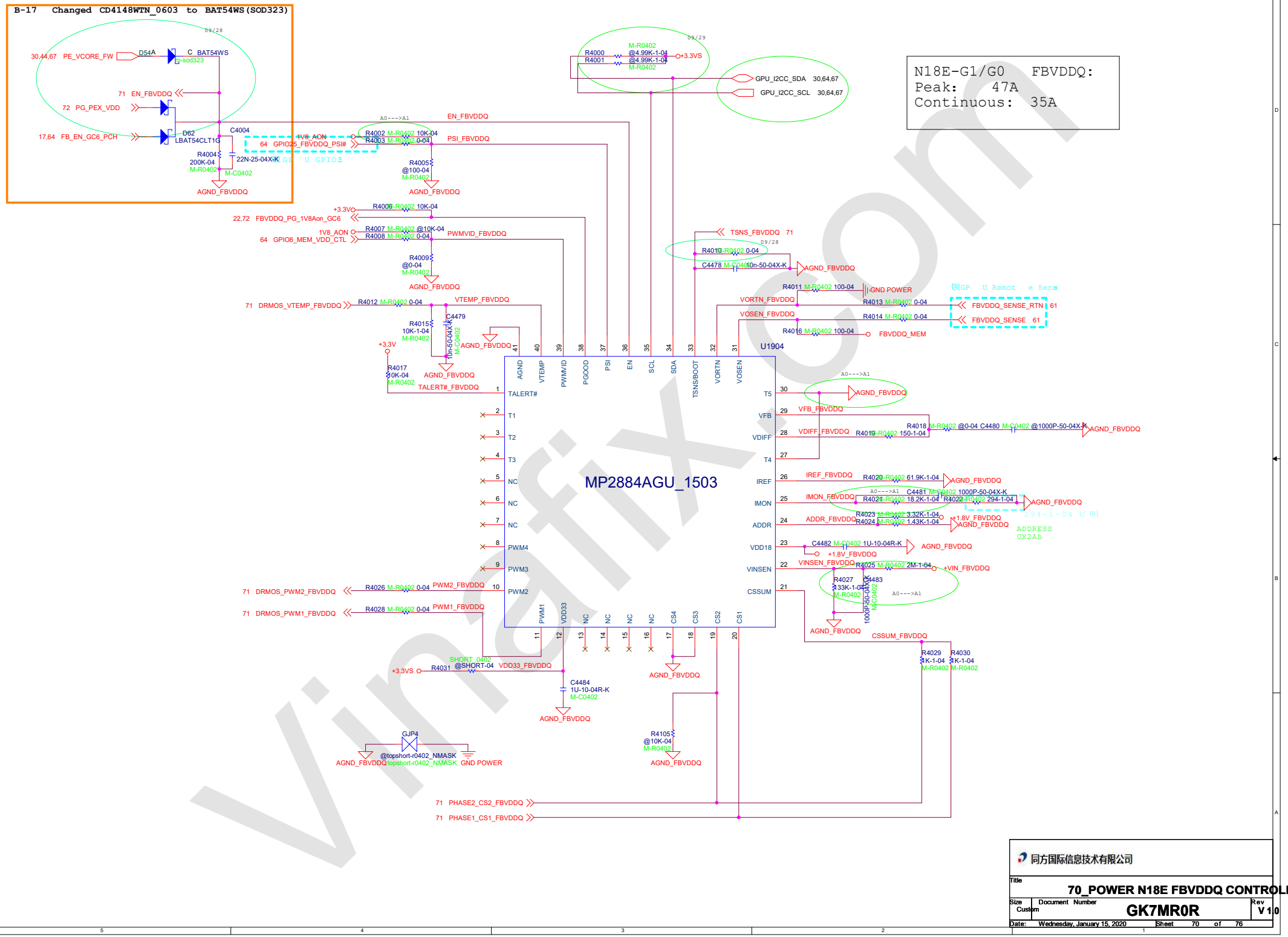
B-17 Changed CD4148WTN_0603 to BAT54WS(SOD323)
N18E-G1/G0 FBVDDQ:
Peak: 47A
Continuous: 35A
MP2884AGU_1503
U1904
TALERT#
T1
T2
T3
NC
NC
NC
PWM4
PWM3
PWM2
PWM1
VDD33
NC
NC
NC
NC
CS4
CS3
CS2
CS1
T5
VFB
VDIFF
T4
IREF
IMON
ADDR
VDD18
VINSEN
CSSUM
AGND
VTEMP
PWMVID
PGOOD
PSI
EN
SCL
SDA
TSNS/BOOT
VORTN
VOSEN
EN_FBVDDQ
PSI_FBVDDQ
PWMVID_FBVDDQ
VTEMP_FBVDDQ
TALERT#_FBVDDQ
PWM2_FBVDDQ
PWM1_FBVDDQ
VFB_FBVDDQ
VDIFF_FBVDDQ
IREF_FBVDDQ
IMON_FBVDDQ
ADDR_FBVDDQ
VINSEN_FBVDDQ
CSSUM_FBVDDQ
TSNS_FBVDDQ
VORTN_FBVDDQ
VOSEN_FBVDDQ
FBVDDQ_MEM
FBVDDQ_SENSE
FBVDDQ_SENSE_RTN
AGND_FBVDDQ
GND POWER
+3.3VS
+3.3V
+1.8V_FBVDDQ
+VIN_FBVDDQ
GPU_I2CC_SDA
GPU_I2CC_SCL
PHASE2_CS2_FBVDDQ
PHASE1_CS1_FBVDDQ
GJP4
@topshort-r0402_NMASK
ADDRESS 0X2Ah
同方国际信息技术有限公司
70_POWER N18E FBVDDQ CONTROLLER
GK7MR0R
V 1.0
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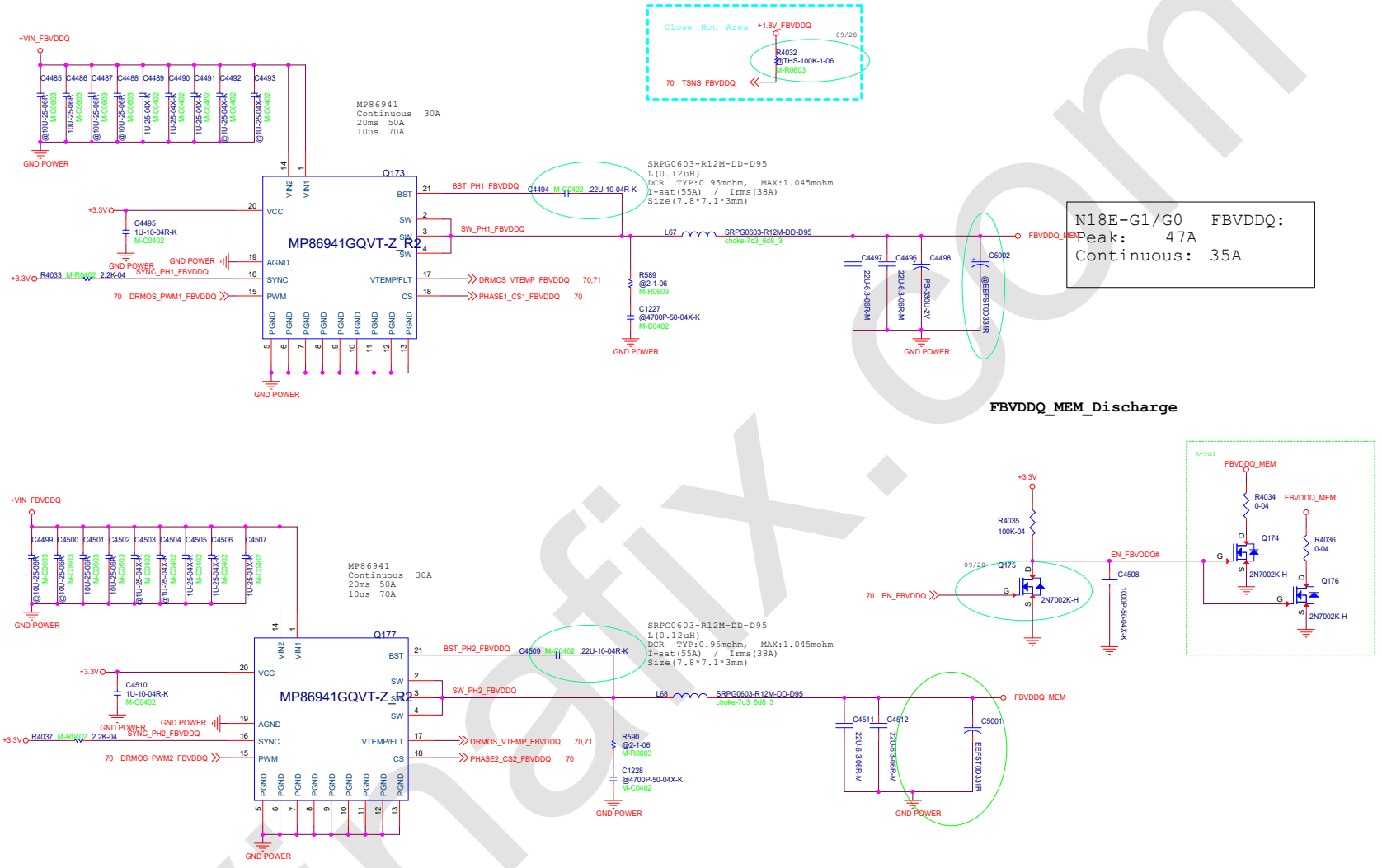

同方国际信息技术有限公司

Title	71_POWER N18E FBVDDQ 2PHASE	
Size C	Document Number GK7MR0R	Rev V1.0
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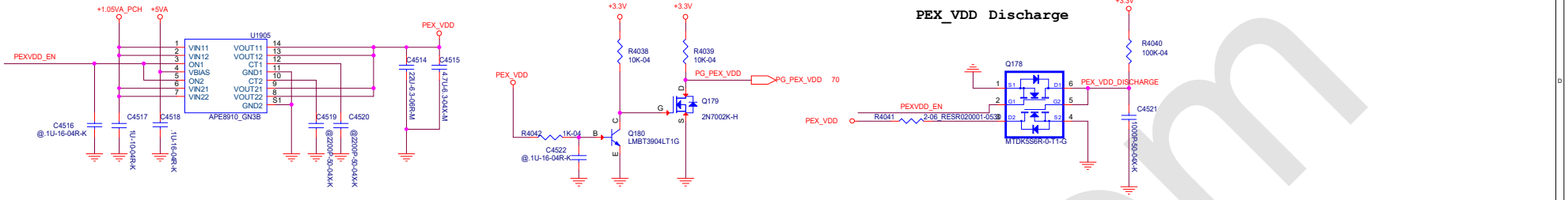
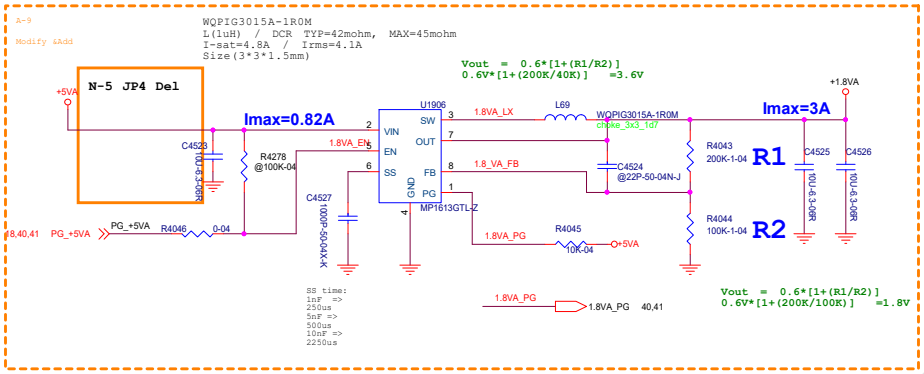
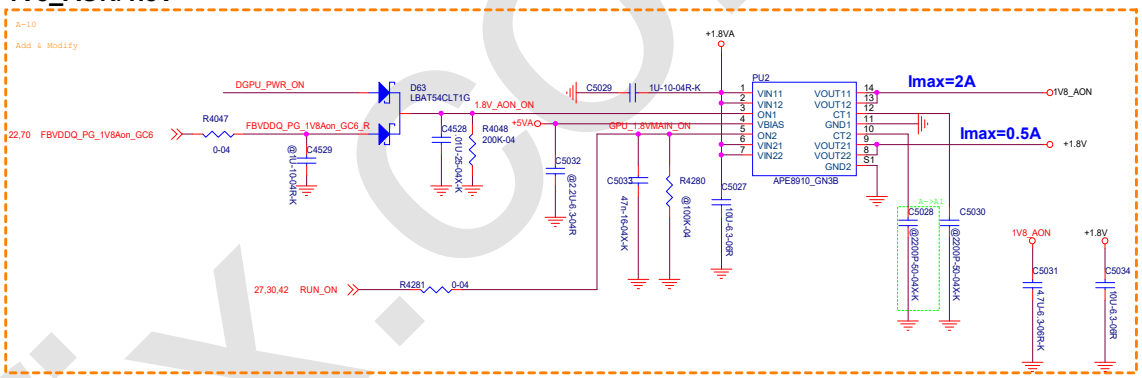
PEX_VDD SW



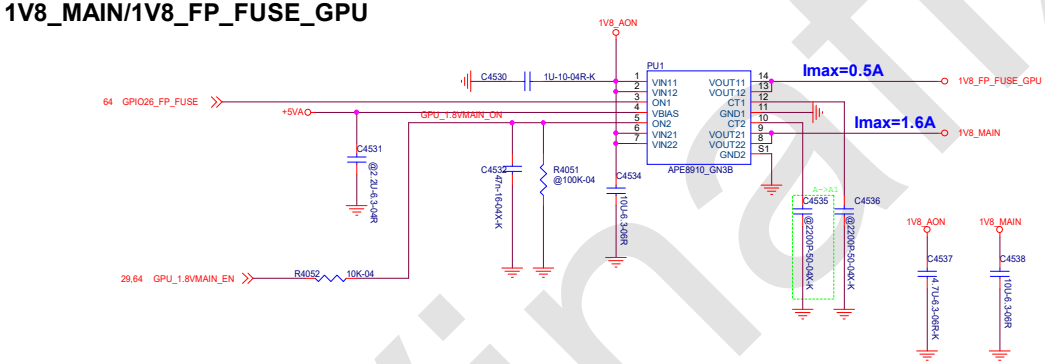
1.8VA

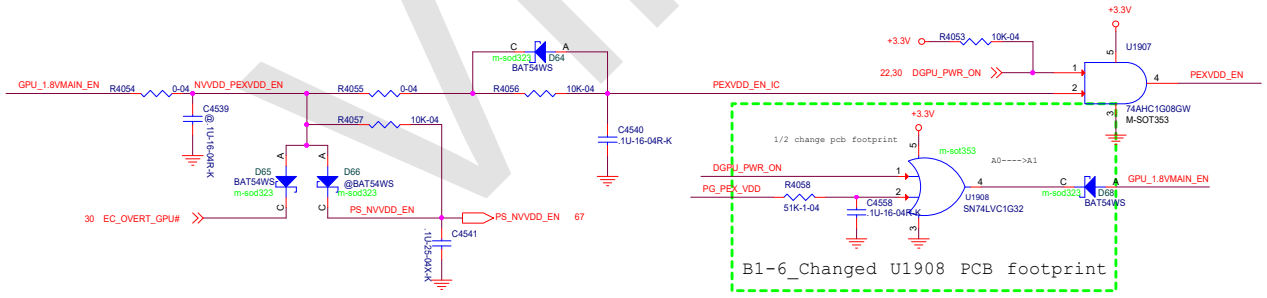


1V8_AON/1.8V

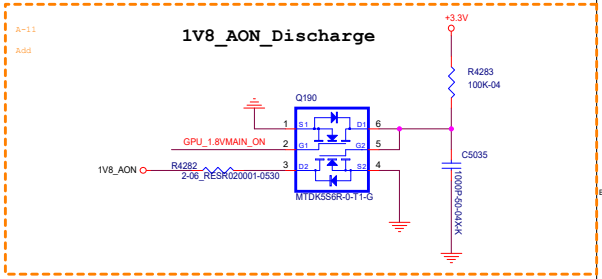


1V8_MAIN/1V8_FP_FUSE_GPU

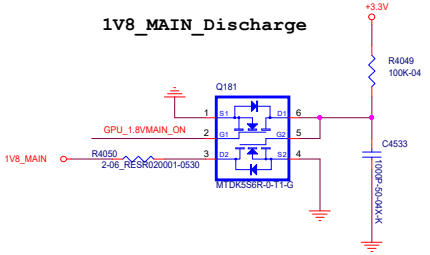




1V8_AON_Discharge



1V8_MAIN_Discharge



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Title: 72_POWER N18E PEX_VDD/1V8_AON

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C	GK7MR0R	V1.0

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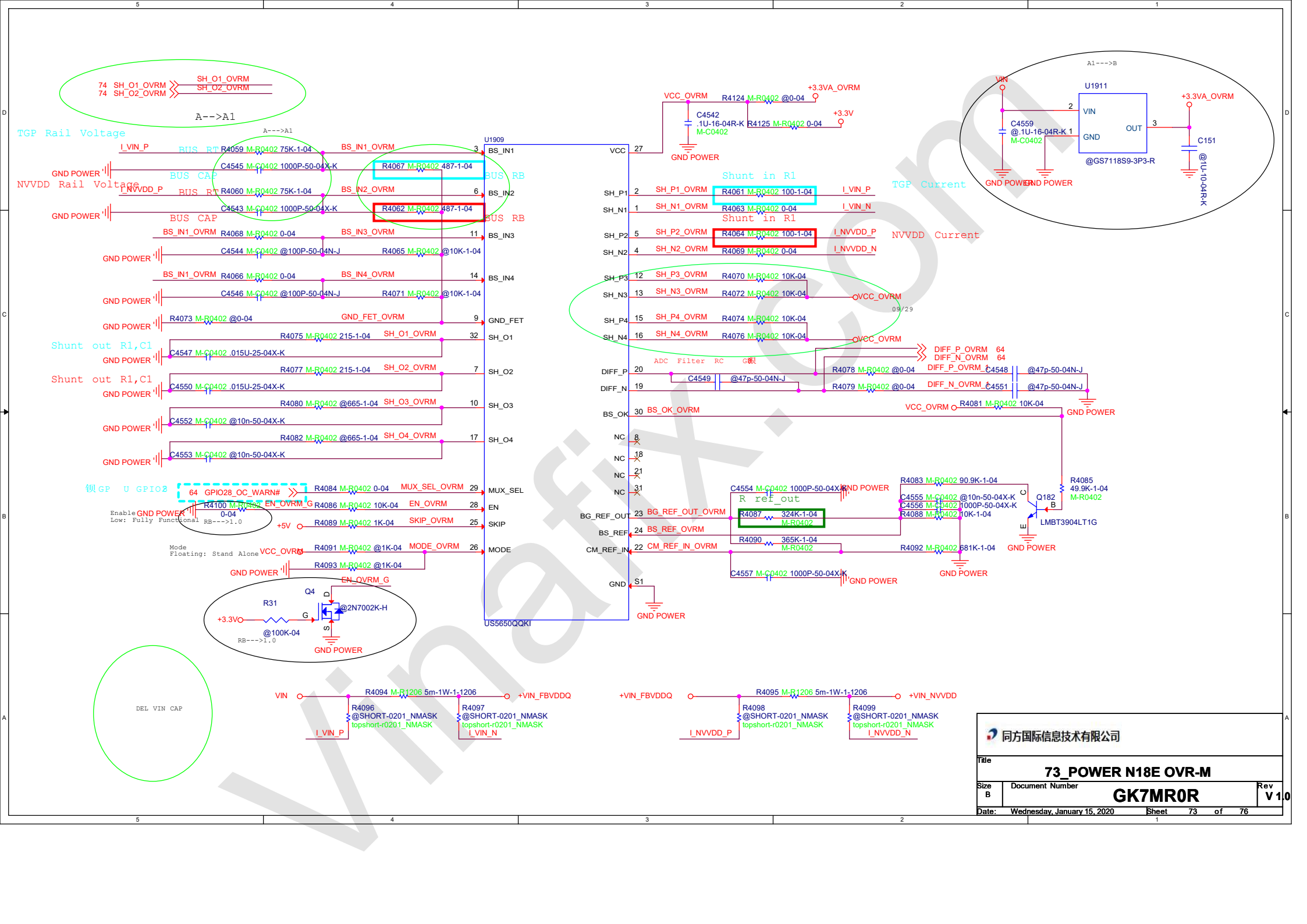
74 SH_O1_OVRM
74 SH_O2_OVRM
SH_O1_OVRM
SH_O2_OVRM
A-->A1
TGP Rail Voltage
NVVDD Rail Voltage
BUS RT
BUS CAP
BUS RB
I_VIN_P
I_NVVDD_P
GND POWER
R4059 M-R0402 75K-1-04
C4545 M-C0402 1000P-50-04X-K
R4067 M-R0402 487-1-04
R4060 M-R0402 75K-1-04
C4543 M-C0402 1000P-50-04X-K
R4062 M-R0402 487-1-04
BS_IN1_OVRM
BS_IN2_OVRM
U1909
BS_IN1
BS_IN2
R4068 M-R0402 0-04
C4544 M-C0402 @100P-50-04N-J
R4065 M-R0402 @10K-1-04
BS_IN3_OVRM
BS_IN3
R4066 M-R0402 0-04
C4546 M-C0402 @100P-50-04N-J
R4071 M-R0402 @10K-1-04
BS_IN4_OVRM
BS_IN4
R4073 M-R0402 @0-04
GND_FET_OVRM
GND_FET
Shunt out R1,C1
R4075 M-R0402 215-1-04
C4547 M-C0402 .015U-25-04X-K
SH_O1_OVRM
SH_O1
R4077 M-R0402 215-1-04
C4550 M-C0402 .015U-25-04X-K
SH_O2_OVRM
SH_O2
R4080 M-R0402 @665-1-04
C4552 M-C0402 @10n-50-04X-K
SH_O3_OVRM
SH_O3
R4082 M-R0402 @665-1-04
C4553 M-C0402 @10n-50-04X-K
SH_O4_OVRM
SH_O4
GPIO28_OC_WARN#
R4084 M-R0402 0-04
MUX_SEL_OVRM
MUX_SEL
R4086 M-R0402 10K-04
EN_OVRM
EN
R4089 M-R0402 1K-04
SKIP_OVRM
SKIP
R4091 M-R0402 @1K-04
MODE_OVRM
MODE
R4093 M-R0402 @1K-04
EN_OVRM_G
Enable
Low: Fully Functional
Mode
Floating: Stand Alone
+5V
VCC_OVRM
Q4
@2N7002K-H
R31
+3.3V
@100K-04
US5650QQKI
VCC_OVRM
R4124 M-R0402 @0-04
+3.3VA_OVRM
C4542
.1U-16-04R-K
R4125 M-R0402 0-04
+3.3V
M-C0402
Shunt in R1
TGP Current
NVVDD Current
SH_P1_OVRM
SH_N1_OVRM
R4061 M-R0402 100-1-04
R4063 M-R0402 0-04
I_VIN_P
I_VIN_N
SH_P2_OVRM
SH_N2_OVRM
R4064 M-R0402 100-1-04
R4069 M-R0402 0-04
I_NVVDD_P
I_NVVDD_N
SH_P3_OVRM
SH_N3_OVRM
R4070 M-R0402 10K-04
R4072 M-R0402 10K-04
SH_P4_OVRM
SH_N4_OVRM
R4074 M-R0402 10K-04
R4076 M-R0402 10K-04
09/29
ADC Filter RC GBR
DIFF_P_OVRM 64
DIFF_N_OVRM 64
DIFF_P_OVRM_C
DIFF_N_OVRM_C
C4549 @47p-50-04N-J
R4078 M-R0402 @0-04
R4079 M-R0402 @0-04
C4548 @47p-50-04N-J
C4551 @47p-50-04N-J
R4081 M-R0402 10K-04
BS_OK_OVRM
R ref_out
C4554 M-C0402 1000P-50-04X-K
R4087 324K-1-04 M-R0402
R4090 365K-1-04 M-R0402
C4557 M-C0402 1000P-50-04X-K
R4083 M-R0402 90.9K-1-04
C4555 M-C0402 @10n-50-04X-K
C4556 M-C0402 1000P-50-04X-K
R4088 M-R0402 10K-1-04
R4092 M-R0402 681K-1-04
Q182
LMBT3904LT1G
R4085
49.9K-1-04
M-R0402
U1911
@GS7118S9-3P3-R
C4559
@.1U-16-04R-K
M-C0402
C151
@1U-10-04R-K
A1--->B
DEL VIN CAP
R4094 M-R1206 5m-1W-1-1206
R4096
@SHORT-0201_NMASK
topshort-r0201_NMASK
R4097
@SHORT-0201_NMASK
topshort-r0201_NMASK
+VIN_FBVDDQ
R4095 M-R1206 5m-1W-1-1206
R4098
@SHORT-0201_NMASK
topshort-r0201_NMASK
R4099
@SHORT-0201_NMASK
topshort-r0201_NMASK
+VIN_NVVDD
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Title
73_POWER N18E OVR-M
Size B
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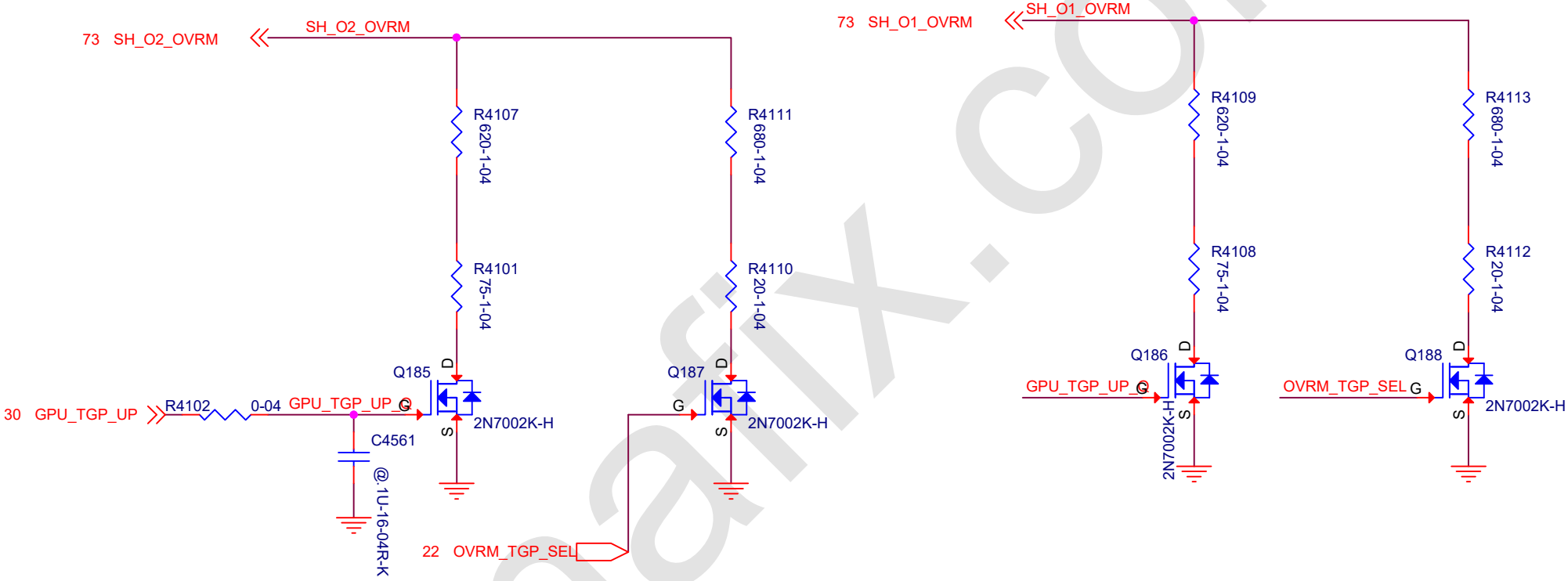

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Title	74_POWER N18E TGP SENSE	
Size A	Document Number GK7MR0R	Rev V 1.0
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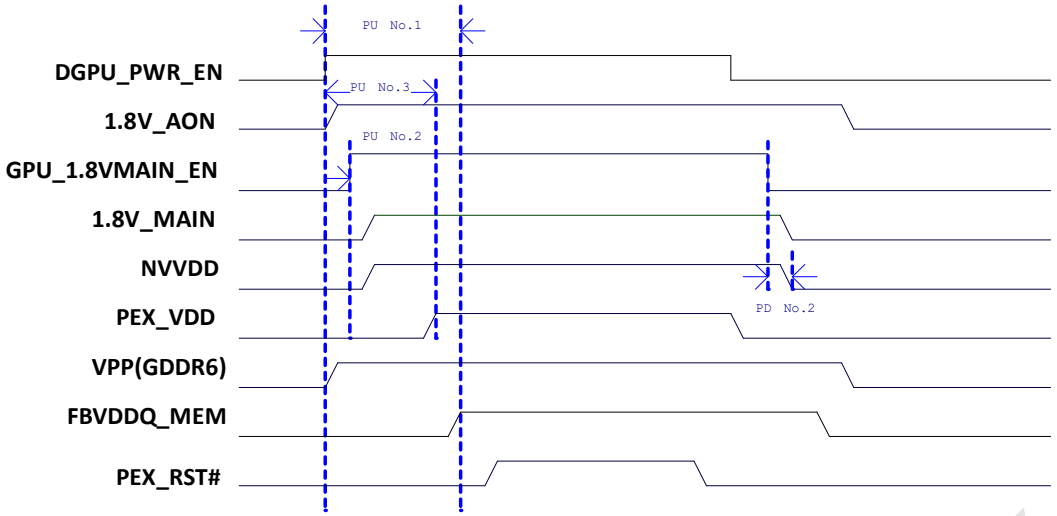
DGPU POWER SEQUENCE



POWER UP sequence is required:1.8V_AON->1.8V_MAIN->NVVDD->/PEX_DVDD->FBVDDQ_MEM
1.The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.
2.Delay From GPU_1.8VMAIN_EN to PEX_DVDD/PG_PEX_VDD) must NOT exceed 4ms.
3.Delay From 1.8V_AON to PEX_DVDD/PG_PEX_VDD) must NOT exceed 20ms.
4.The ramp-up overshoot should not exceed the silicon reliability limit voltage
5.Power up NVVDD must be 90% before PEX_DVDD and NVVDDS can start ramp up.
6.Power up 1.8V_AON must be 90% before NV 3.3V ramp up.
7.All 3.3V devices that connect to the GPU must be powered after 1.8V_AON ; GPU can't have any 3.3V leakage path before 1.8V_AON present.
8.FBVDDQ.USB_VPP and 1.8_AON don't need power cycle for GC6

POWER DOWN sequence is required
1.PEX_DVDD must ramp down before NVVDD.
2.The propagation delay between GPU_1.8VMAIN_EN and the NVVDD_EN pin needs to be less than 1ms during both power down.
3.For GDDR6,VPP must be equal to or higher than FBVDDQ at all time ; use gate logic and discharge circuit as needed.
4.All 3.3V devices that connect to the GPU must be ramp down before +1.8V_AON; GPU can't have any 3.3V leakage path after +1.8V_AON and +1.8V_MAIN power down.
5.Power down PEX_DVDD must be less than 10% before NVVDD can start ramp down.
6.Power down NV 3.3V must be less than 10% before +1.8V_AON can start ramp down.

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Title	75_GPU POWER SEQUENCE	
Size: Custom	Document Number: GK7MR0R	Rev: V 1.0
Date: Wednesday, January 15, 2020	Sheet 75 of 76	

Revision History

VA TO VB Date: 2019/11/25

PCB Version: B PCB P/N XXXX

No.	Modify Item	Modify Details	Schematic/Layout/BOM Change	Page
1	B1-Exchanged HPD of DDS IC CH1&CH2 for iGPU&dGPU	U1914 Pin3&Pin13	Schematic&Layout	27
2	B2-SPEAKER no sound	R4273 unstuff	Schematic&BOM	35
3	B3- eSPI&LPC strapping pin	R112 stuff	Schematic&BOM	18
4	B4- Revised Vcore_VIN	Add B42,B43	Schematic&BOM	45
5	B5- Changed U3 for new material	U3 value (MP2949 to MP2979)	Schematic&BOM	44
6	B-6 Changed value	C4034,C4035 value	Schematic&BOM	54
7	B-7 Changed value	C3961,C3962 value	Schematic&BOM	52
8	B-8 Changed value	C1 value	Schematic&BOM	57
9	B-9 Changed PWR_USB# to DGPU_PWR_ON for DB_THERMISTOR	Layout	Schematic&Layout	44
10	B-10 Moved PWR_USB# to EC GPG2 pin for DB_THERMISTOR	Layout	Schematic&Layout	30
11	B-11 Changed DGPU_PWR_ON to DB_THERMISTOR	Layout	Schematic&Layout	30
12	B-12 Changed PWR_USB# pull up to DB_THERMISTOR pull up	Layout	Schematic&Layout	30
13	B-13 Add DB_THERMISTOR signal	Add R4337	Schematic&Layout&BOM	35
14	B-14 Changed PANEL_3.3V_ON to LCD_VCC_EN_Recieve	Layout	Schematic&Layout	30
15	B-15 Add LCD_VCC_EN_Recieve for EC	Layout	Schematic&Layout	27
16	B-16 Add pull high for SVID by CPU side	Add R4378,R4379,R4380，C5036	Schematic&Layout&BOM	9
17	B-17 Changed CD4148WTN_0603 to BAT54WS(SOD323)	D54	Schematic&Layout&BOM	70
18	B-18 Changed pcb footprint and update symbol	CNDCIN1	Schematic&Layout	39
19	B-19 Unstuff	R4354, R4355 unstuff	BOM	70
20	B-20 Add JP for VIN_VCCSA	Add B44,B45	Schematic&Layout	46
21	B-21 Changed value for DB_THERMISTOR	Changed R3551	BOM	30
22	B-22 Revised R &C for MP2979	Changed R529,C155,R530,C156,C157,R534,R548,R553	BOM	44
23	B-23 Changed value	Changed C157 (56pF to 68pF)	BOM	44

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Title: 76_History

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Revision History

VB TO VB1 Date: 2019/12/26

PCB Version: B1 PCB P/N XXXX

No.	Modify Item	Modify Details	Schematic/Layout/BOM Change	Page
1	B1-1_Add capacitor for DDS AUXP&N solved non-DDS LG panel no display	C5037,C5038	Schematic&BOM&Layout	27
2	B1-2_ Change R733 value for DB thermistor	R733(10K to 47K)	Schematic&BOM	30
3	B1-3_ Change R3551 value	R3551(47K to 10K)	Schematic&BOM	30
4	B1-4_Changed power plane 1V8_AON to +3.3V_LCD for pull up	R4354,R4355	Layout	64
5	B1-5_Changed C443 value for ME interference	C433(to EEEHS1E330L)	BOM	45
6	B1-6_Changed U1908 PCB footprint	U1908	Schematic&Layout	72

VB1 TO V1.0 Date: 2020/01/08

PCB Version: 1.0 PCB P/N XXXX

No.	Modify Item	Modify Details	Schematic/Layout/BOM Change	Page
1	N-1_ Stuff for Turbo LED lighter	R210,R318 stuff	Schematic&BOM	31
2	N-2_ Cancel Jumper	JP9 cancel	Schematic&Layout	43
14	N-3_ Cancel Jumper	JP7 cancel	Schematic&Layout	41
15	N-4_ Cancel Jumper	JP8 cancel	Schematic&Layout	41
16	N-5_ Cancel Jumper	JP4 cancel	Schematic&Layout	72
17	N-6_ Cancel Jumper	JP5 cancel	Schematic&Layout	40
18	N-7_ Cancel Jumper	JP6 cancel	Schematic&Layout	40
19	N-8_ Removed B44&B45	B44,B45 cancel	Schematic&Layout&BOM	46
20	N-9_ Add TestPoint	Add TP1927 ... TP1933 on the TOP size	Schematic&Layout	39
21	N-10_ Add Capacitor for DDS edp output	Add C5039..... C5046	Schematic&Layout&BOM	27
22	N-11_ Add pull down R for PCH GPIO	Add R4381	Schematic&Layout&BOM	22
23				

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Title: 77_History

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