PEGATRON CORPORATION

INTEL SKYLAKE-H CUP INTEL SKL PCH-H (HM-170)
GPU NVIDIA/N16E-GX GB3B-256

MU5DC/CH7DC
2020-10-12
(REV 2.0)

<Variiant Name>

PEGATRON Title : I2C MAP

Pegatron Corp. Engineer: Leon_Lu

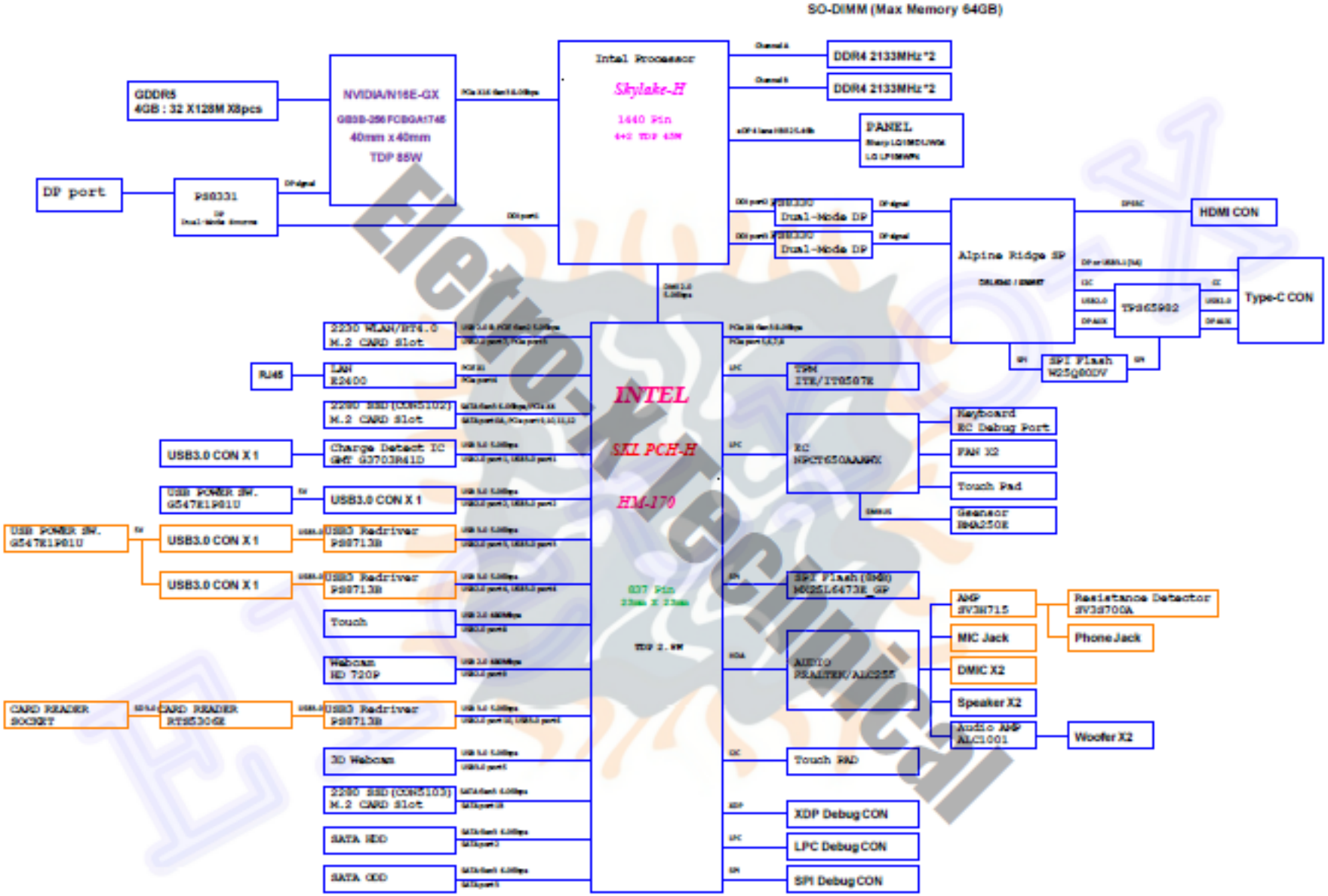
Size	Project Name	Rev
A3	MU5DC/CH7DC MAIN	A00

Date: Monday, September 07, 2020 Sheet 2 of A02

BOARD

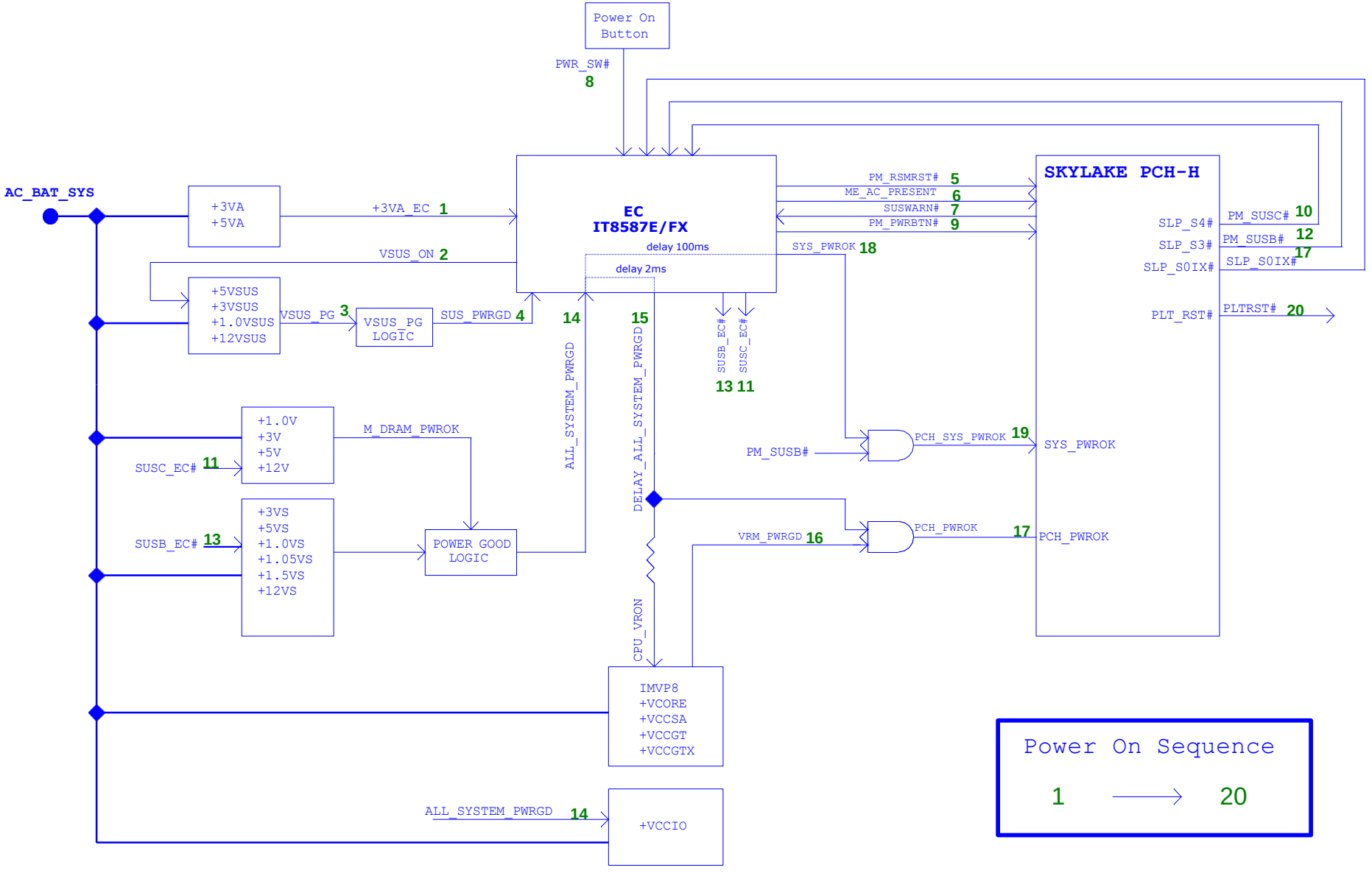
Gaming (Skylake-H)

Revision_1.00_2015/03/10

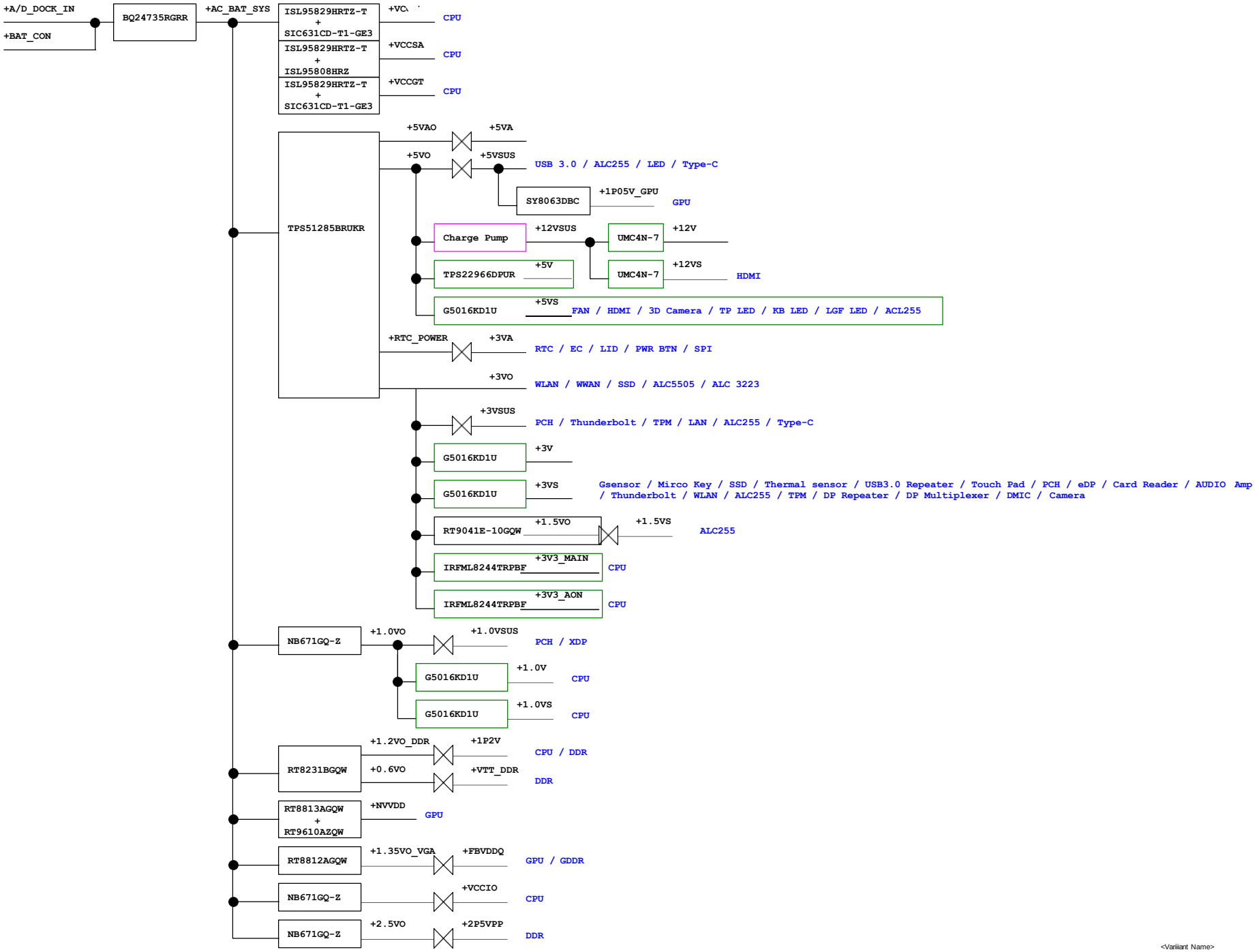


PEGATRON Title :

Power On Sequence Diagram G3-S0 R0.1(non-Deep Sx)



Size C	Document Number MUSDC//CH7DC MAIN BOARD	Rev A00
Date: Monday,, Septtember 07,, 2015	Sheet 99 of 108	



<Variiant Name>

PEGATRON

Title : POWER TREE

PEGATRON CORPORATION

Engineer: Leon_Lu

Size	Project Name	Rev
A3	MU5DC/CH7DC MAIN	A00

Date: Monday, September 07, 2015 Sheet 108 of A04

BOARD

..ntel SharkBay and DSW supported

LANRTL8151GD-CG
RESET#

Mini Express x 1 (Half Card)
PERST#

Mini Express x 1 (Full Card)
PERST#

CARDER READER RTS5209-GR
RESET#

RESET_SWITCH
SYS_RESET#

POWER_SWITCH
PWRBTN

<5> PWRBTN#

Fintek SIO F71808AU
PSIN#
PSON#
PCIRST2#
PCIRST1#
LRESET#
KBRST#
RSMRST#
PSOUT#
S3#
S4#
SUS_WARN#
SUS_ACK#
DPWROK
PWROK

<23> PCIE_RST#
<22> PLTRST#
RST_KB#
<8> RSMRST#
<5> SB_PWRBTN#
<13> SLP_S3#
<11> SLP_S4#
<9> SUS_WARN#
<10> SUS_ACK#
<4> PCH_DPWROK
<16> PWROK
<6> SLP_SUS#

<14> PSON#

MAIN POWER
<15> +19V
+5V
+3P3V
+1P5V
+1P2V
+1P05V

LYNXPOINT PCH
HDA_RST#
SYS_RESET#
PLTRST#
RCIN#
RSMRST#
PWRBTN#
SLP_S3#
SLP_S4#
SLP_A#
SLP_LAN#
SUS_WARN#
SUS_ACK#
DPWROK
PWROK
APWROK
SLP_SUS#
SYS_PWROK
DRAMPWROK
PROCPWRGD
PLTRST_PROC#
RTCRST#

AZ_RST#
AUDIO ALC3661-CG
RESET#

SYS_RESET#
<17> PM_DRAM_PWRGD
<18> H_CPUPWRGD
<22> PLTRST_CPU#
<1> RTCRST#
BATTERY

HASWELL PROCESSOR
DBR#
SM_DRAMPWROK
PWRGOOD
PLTRSTIN#
VIDSOUT/VIDSCLK
VCORE

<16~18> SVIDs
<19> LOAD SVIDs

Vcore Controller
VDIO/VCLK
VCORE
VR_RDY
EN
TPS51631RSM

<20> +VCORE
<21> VRM_PWRGD
<15> +3P3V

MAIN POWER
+3P3V

DUAL POWER
<12> +5V_DUAL
+1P35V_DUAL

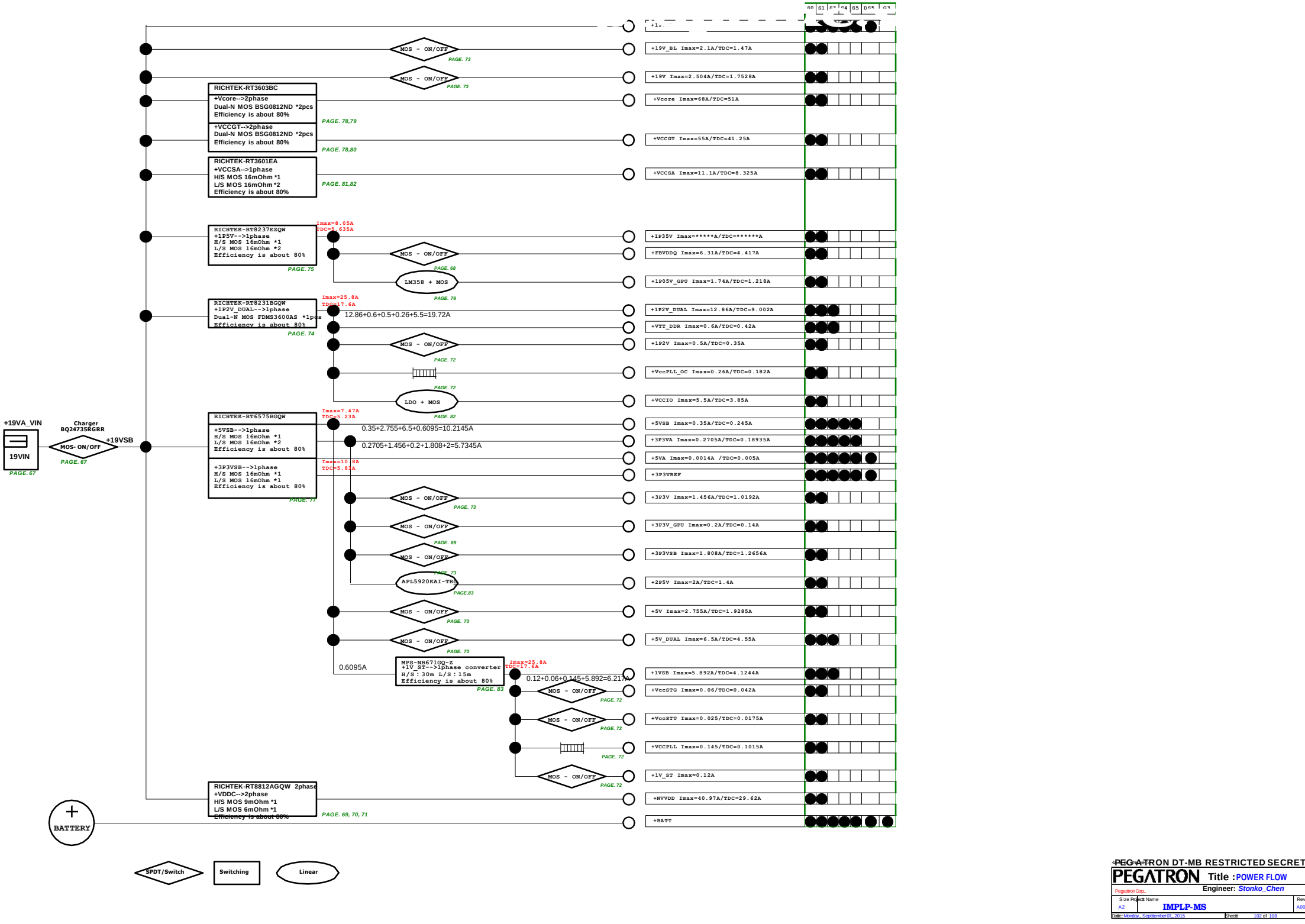
ALWAYS POWER
<3> +5VA
+3VA

STANDBY POWER
<7> +5VSB
+3VSB

<2> +19VA
+19V Adapter PSU

ONBOARD POWER
CHIP
SOCKET or SLOT

PEGATRON Title : POWER ON CHART
Pegatron Corp. Engineer: Stonko_Chen
Size A3 | Project Name IMPLP-MS | Rev A00
Date: Monday, September 07, 2015 | Sheet 100 of 108



PEGATRON Title : POWER FLOW

PegatronCorp. Engineer: Stonko_Chen

Size	Project Name	Rev
A2	IMPLP-MS	A00

Date: Monday, September 07, 2015 Sheet 102 of 108

GAMING

I2C_Port	Module	DEVICE	7-bit addr
I2C_0	TOUCH PAD		0X2C
I2C_1	TOUCH PANEL		
SMBUS	DDR Channel A(CON1600)		
	DDR Channel A(CON1601)		
	DDR Channel B(CON1700)		
	DDR Channel B(CON1701)		
	Resistance Detector	SV3S700A	0X73
SMBUS0 (EC)	BATTERY		0X0B
	CHARGE IC	BQ24735RGRR	0X09
SMBUS1 (EC)	G-SENSOR	BMA250E	0X1D
	THERMAL-SENSOR	G781P8F	0X4C
	LED DRIVER	TLC59116IPWR	0X68
	GPU	N16E-GX	0X4B

Note:
Default component footprint is
SMD 0402, Y5V, 5% type.
Difference footprint show on schematics. Property: BOM
I = Installed Part.
(I) = Not Installed Part.
PAOTO = PROTO Phase Only.VP = Virtual Part. NOBOM = Symbol only. VP = Virtual Part.

+AC_BAT_SYS → +AC_BAT_SYS 45,80,81,82,83,87,88,94,95,96

+BAT_CON → +BAT_CON 60,88

+5VA → +5VA 53,56,81

+3VA → +3VA 26,30,31,44,45,56,57,60,81,88

+5VO → +5VO 81,83,84,88,91

+3VO → +3VO 81,82,84,91,94

+1.5VO → +1.5VO 84

+5VSUS → +5VSUS 12,36,37,45,52,55,56,67,81

+3VSUS → +3VSUS 7,11,12,21,22,23,24,26,31,33,36,44,52,53,62,81,92

+3V → +3V 91

+5VS → +5VS 31,36,37,43,45,48,50,51,56,80,87,89,91

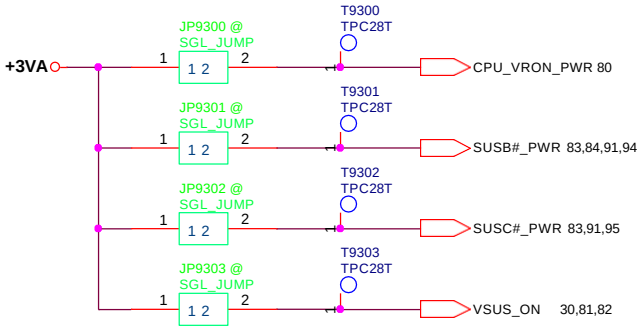
+3VS → +3VS 3,7,11,12,13,14,16,17,21,22,23,24,26,30,31,36,43,44,45,46,48,50,51,53,56,58,61,62,67,70,91,92

+1.5VS → +1.5VS 36,51,84

+VCORE → +VCORE 9,80

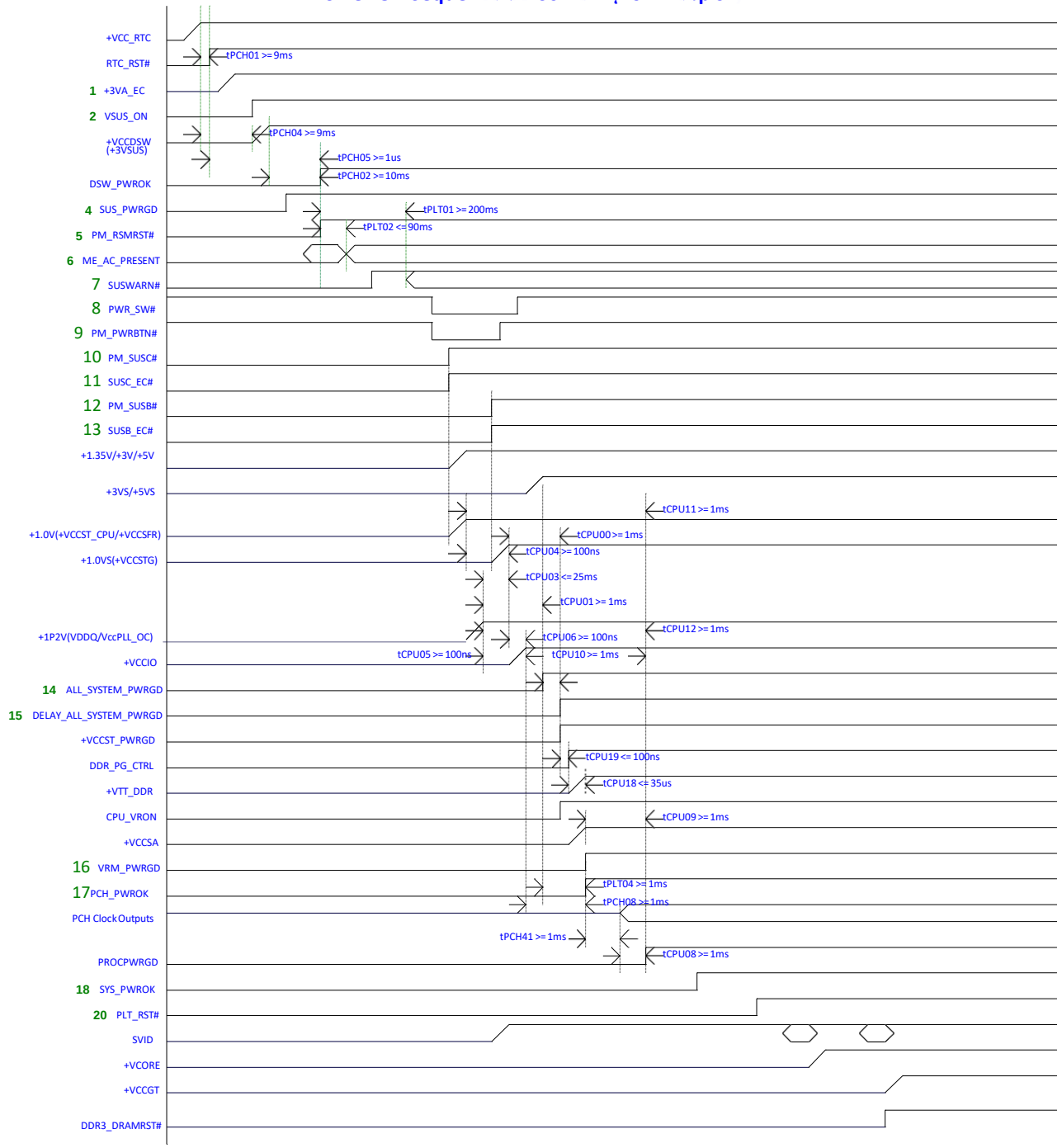
+VCCIO → +VCCIO 3,6,7,10,44,94

FOR POWER TEST



PEGATRON	Title : USB CHARGE IC	
Pegatron Corp.	Engineer: Shrek_Tseng	
Size: Custom	Project Name: IPPSL-CD	Rev: A00
Date: Monday, September 07, 2015	Sheet 93 of 108	

Power On Sequen[illegible] Sx



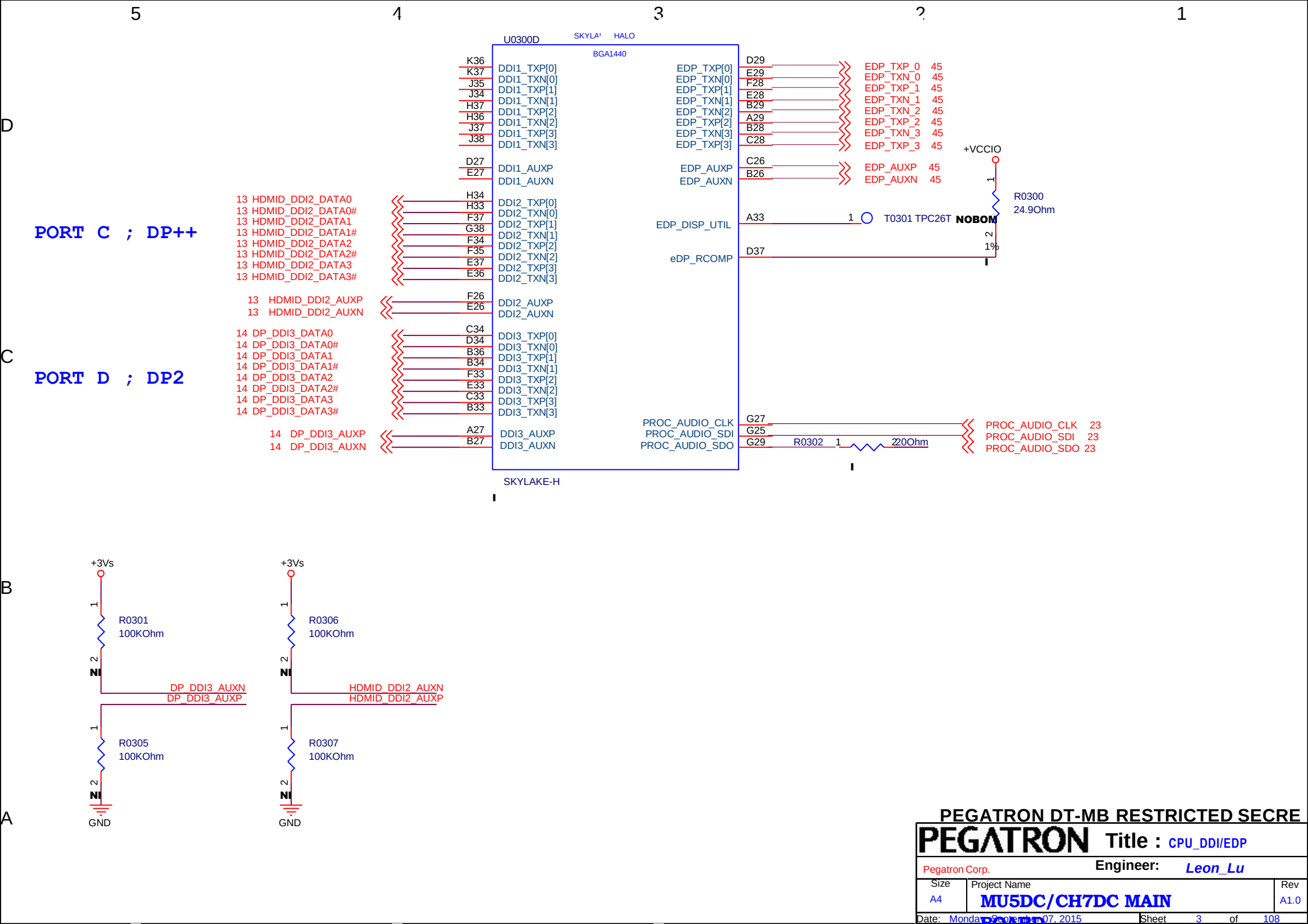
<Variantt Name>

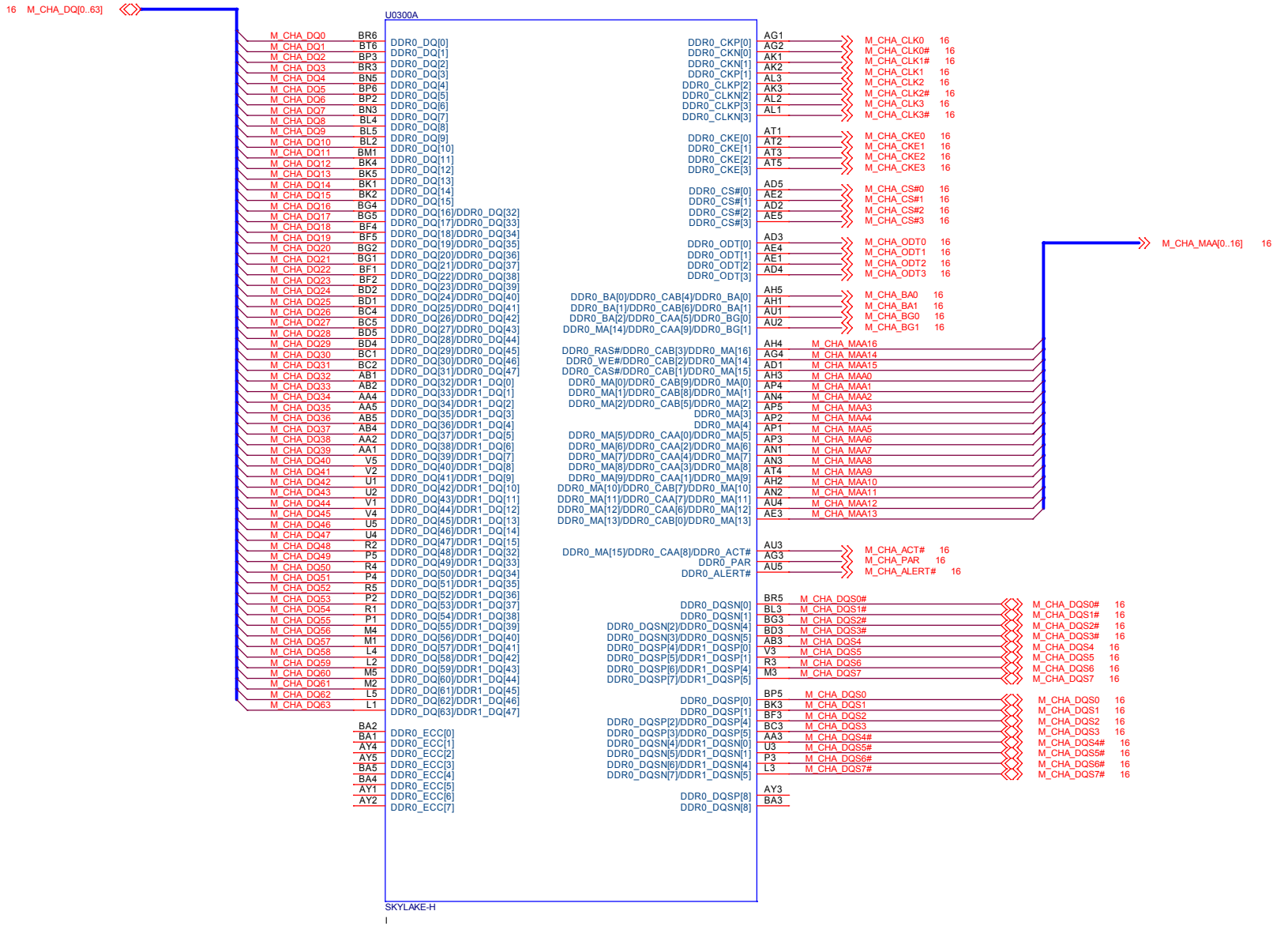
PEGATRON Title : POWER SEQUENCE Timing

Pegatitron Corp.. Engineer: Leon_Lu

Size	Projectt Name	Rev
C	MU5DC/CH7DC MAIN BOARD	A00

Date: Monday, Septe... Sheett 108 of A03


5
4
3
2
1
D
C
B
A
U0300D
SKYLAKE_HALO
BGA1440
SKYLAKE-H
PORT C ; DP++
PORT D ; DP2
DDI1_TXP[0]
DDI1_TXN[0]
DDI1_TXP[1]
DDI1_TXN[1]
DDI1_TXP[2]
DDI1_TXN[2]
DDI1_TXP[3]
DDI1_TXN[3]
DDI1_AUXP
DDI1_AUXN
DDI2_TXP[0]
DDI2_TXN[0]
DDI2_TXP[1]
DDI2_TXN[1]
DDI2_TXP[2]
DDI2_TXN[2]
DDI2_TXP[3]
DDI2_TXN[3]
DDI2_AUXP
DDI2_AUXN
DDI3_TXP[0]
DDI3_TXN[0]
DDI3_TXP[1]
DDI3_TXN[1]
DDI3_TXP[2]
DDI3_TXN[2]
DDI3_TXP[3]
DDI3_TXN[3]
DDI3_AUXP
DDI3_AUXN
EDP_TXP[0]
EDP_TXN[0]
EDP_TXP[1]
EDP_TXN[1]
EDP_TXP[2]
EDP_TXN[2]
EDP_TXP[3]
EDP_TXN[3]
EDP_AUXP
EDP_AUXN
EDP_DISP_UTIL
eDP_RCOMP
PROC_AUDIO_CLK
PROC_AUDIO_SDI
PROC_AUDIO_SDO
EDP_TXP_0 45
EDP_TXN_0 45
EDP_TXP_1 45
EDP_TXN_1 45
EDP_TXN_2 45
EDP_TXP_2 45
EDP_TXN_3 45
EDP_TXP_3 45
EDP_AUXP 45
EDP_AUXN 45
+VCCIO
R0300
24.9Ohm
1%
T0301 TPC26T
NOBOM
R0302
220Ohm
PROC_AUDIO_CLK 23
PROC_AUDIO_SDI 23
PROC_AUDIO_SDO 23
13 HDMID_DDI2_DATA0
13 HDMID_DDI2_DATA0#
13 HDMID_DDI2_DATA1
13 HDMID_DDI2_DATA1#
13 HDMID_DDI2_DATA2
13 HDMID_DDI2_DATA2#
13 HDMID_DDI2_DATA3
13 HDMID_DDI2_DATA3#
13 HDMID_DDI2_AUXP
13 HDMID_DDI2_AUXN
14 DP_DDI3_DATA0
14 DP_DDI3_DATA0#
14 DP_DDI3_DATA1
14 DP_DDI3_DATA1#
14 DP_DDI3_DATA2
14 DP_DDI3_DATA2#
14 DP_DDI3_DATA3
14 DP_DDI3_DATA3#
14 DP_DDI3_AUXP
14 DP_DDI3_AUXN
+3Vs
R0301
100KOhm
R0305
100KOhm
DP_DDI3_AUXN
DP_DDI3_AUXP
R0306
100KOhm
R0307
100KOhm
HDMID_DDI2_AUXN
HDMID_DDI2_AUXP
GND
PEGATRON DT-MB RESTRICTED SECRE
PEGATRON
Title : CPU_DDI/EDP
Pegatron Corp.
Engineer: Leon_Lu
Size A4
Project Name MU5DC/CH7DC MAIN
Rev A1.0
Date: Monday, September 07, 2015
Sheet 3 of 108



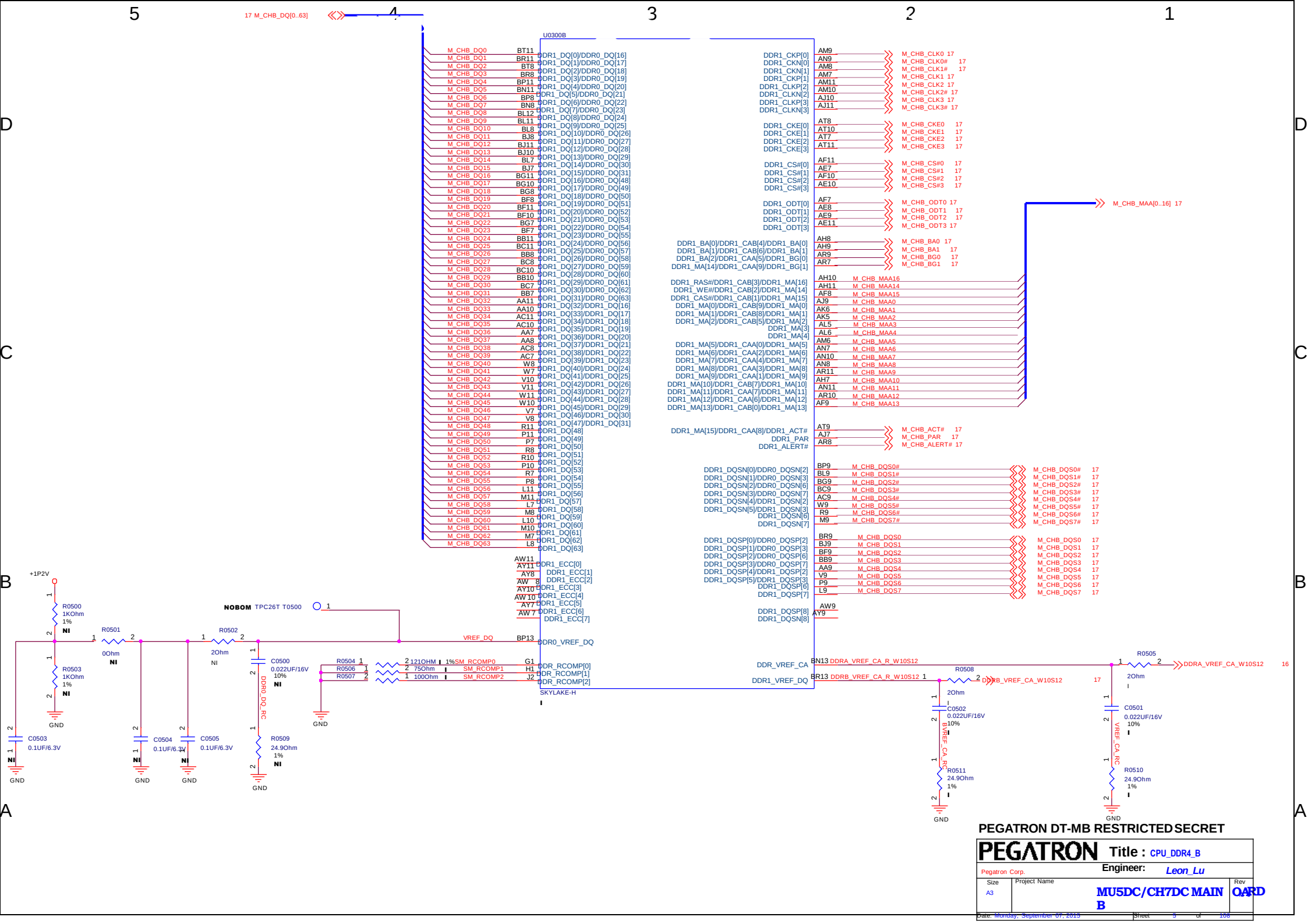
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU_DDR4_A

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A3	MU5DC/CH7DC MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 4 of 108



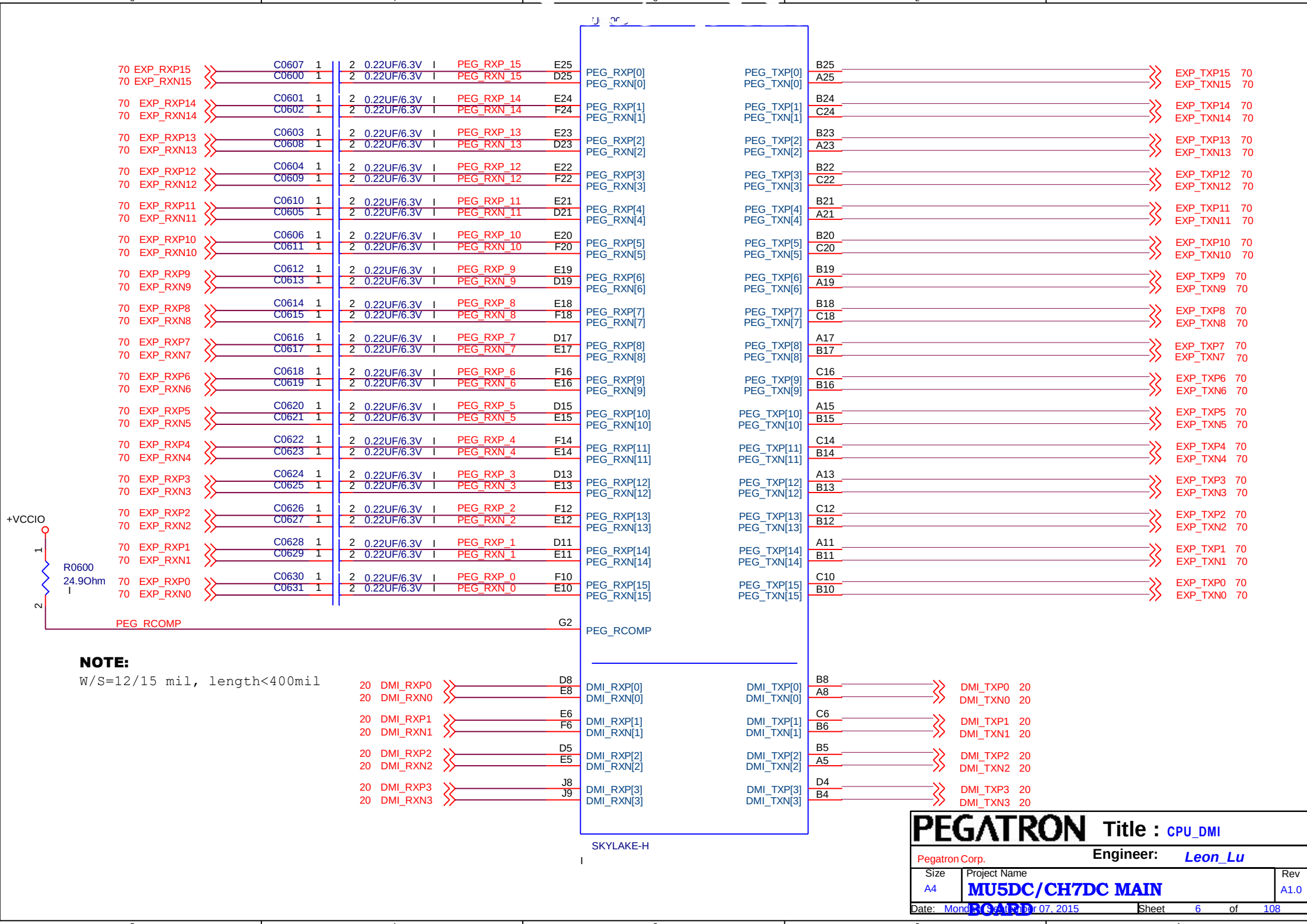
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU_DDR4_B

Pegatron Corp. Engineer: Leon_Lu

Size A3 | Project Name MU5DC/CH7DC MAIN BOARD | Rev A1

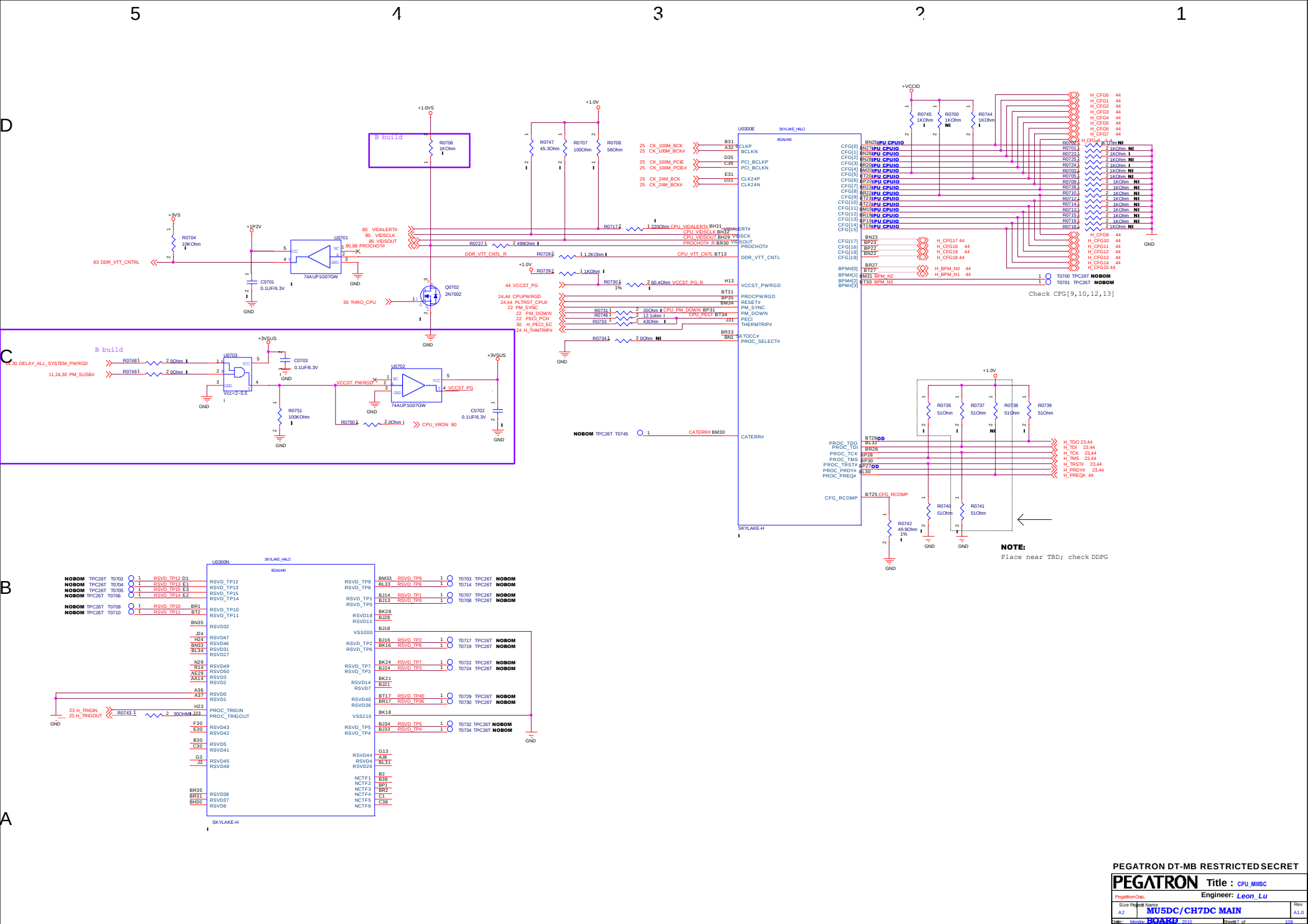
Date: Monday, September 07, 2015 | Sheet 5 of 106

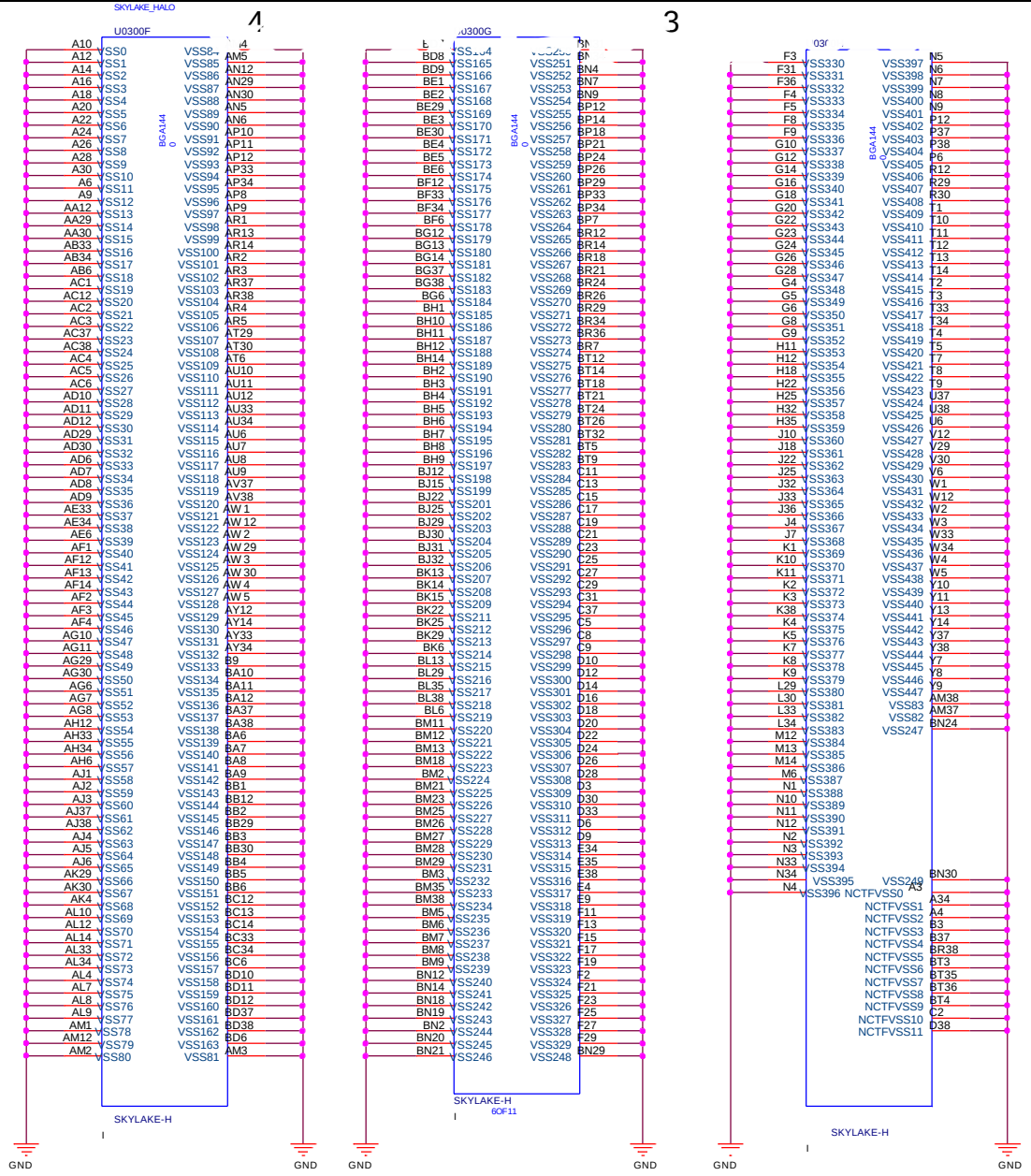


NOTE:

W/S=12/15 mil, length<400mil

PEGATRON	Title : CPU_DMI		
Pegatron Corp.	Engineer: Leon_Lu		
Size: A4	Project Name: MU5DC/CH7DC MAIN BOARD		Rev: A1.0
Date: Monday, September 07, 2015	Sheet 6 of 108		


5
4
3
2
1
D
C
B
A
B build
U0300E
SKYLAKE_HALO
BGA1440
SKYLAKE-H
U0300N
U0701
U0702
U0703
74AUP1G07GW
Q0702
2N7002
Check CFG[9,10,12,13]
NOTE:
Place near TBD; check DDPG
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : CPU_MIISC
Engineer: Leon_Lu
Size
Project Name
MU5DC/CH7DC MAIN BOARD
Rev
A1.0
Date: Monday, 2015
Sheet 7 of 108



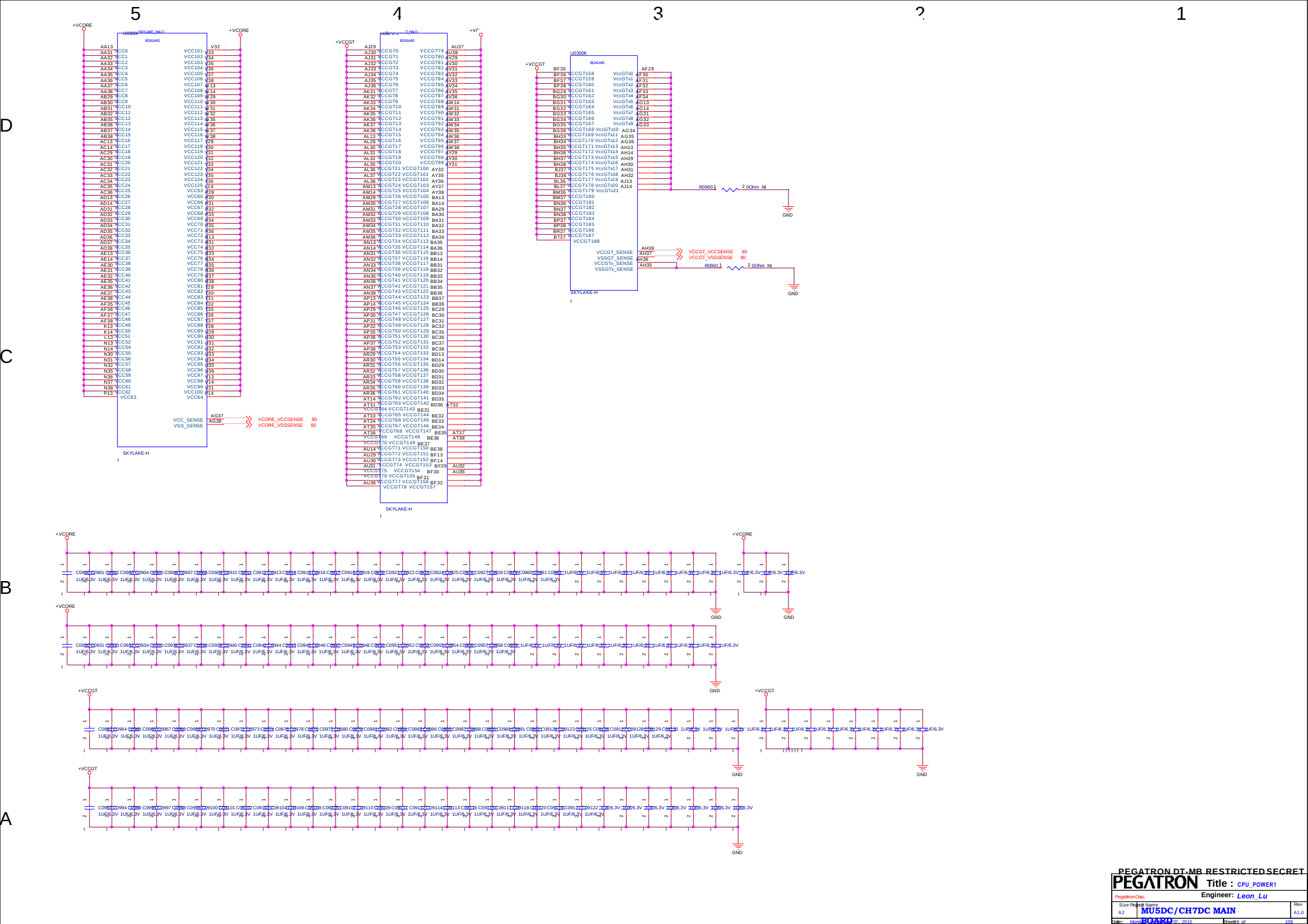
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU_VSS

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A3	MU5DC/CH7DC MAIN BOARD	A1.0

Date: Monday, January 26, 2015 Sheet 8 of 108



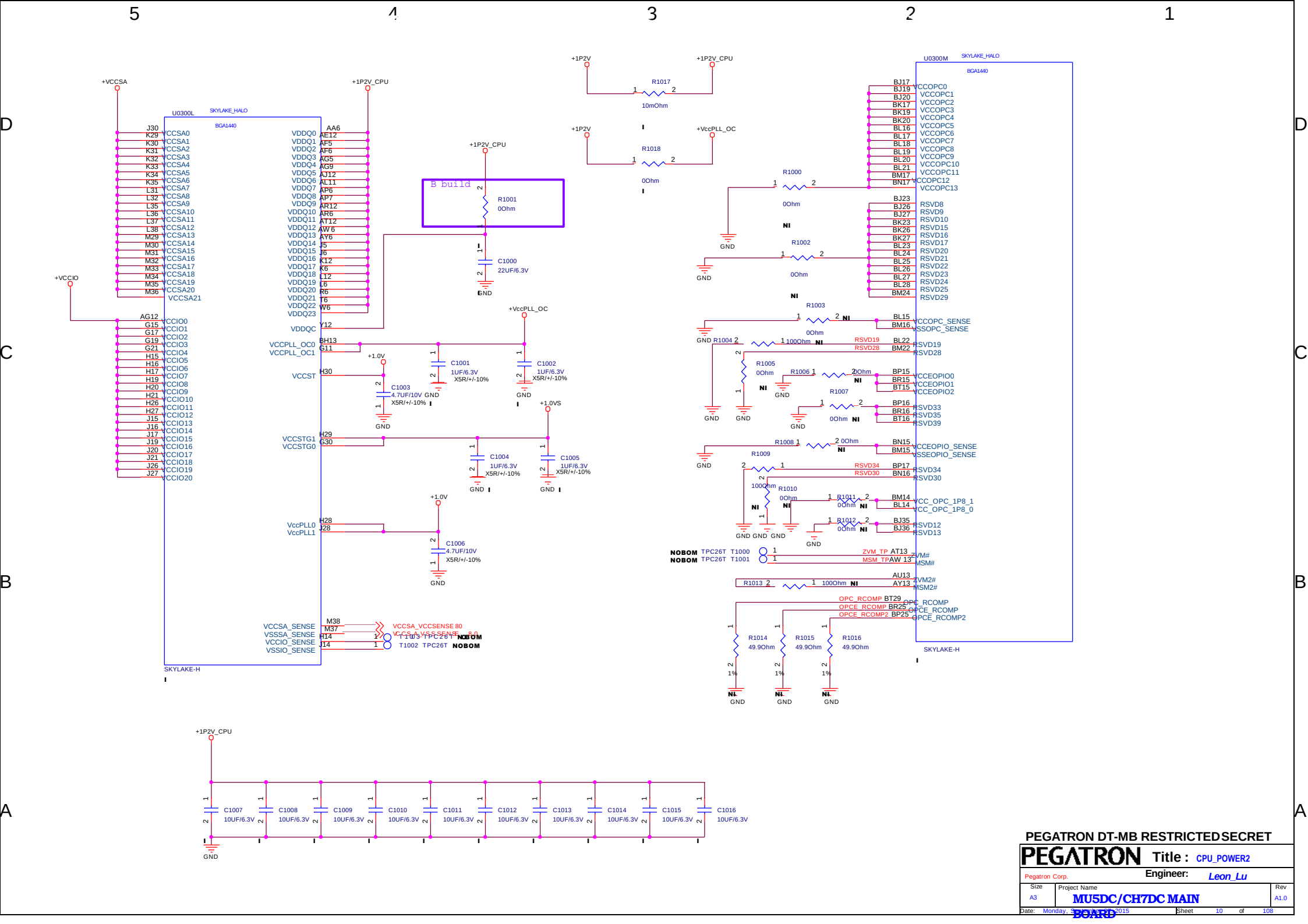
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU_POWER1

PegatronCorp. Engineer: Leon_Lu

Size	Project Name	Rev
A2	MU5DC/CH7DC MAIN BOARD	A1.0

Date: Monday, July 27, 2015 Sheet 9 of 108



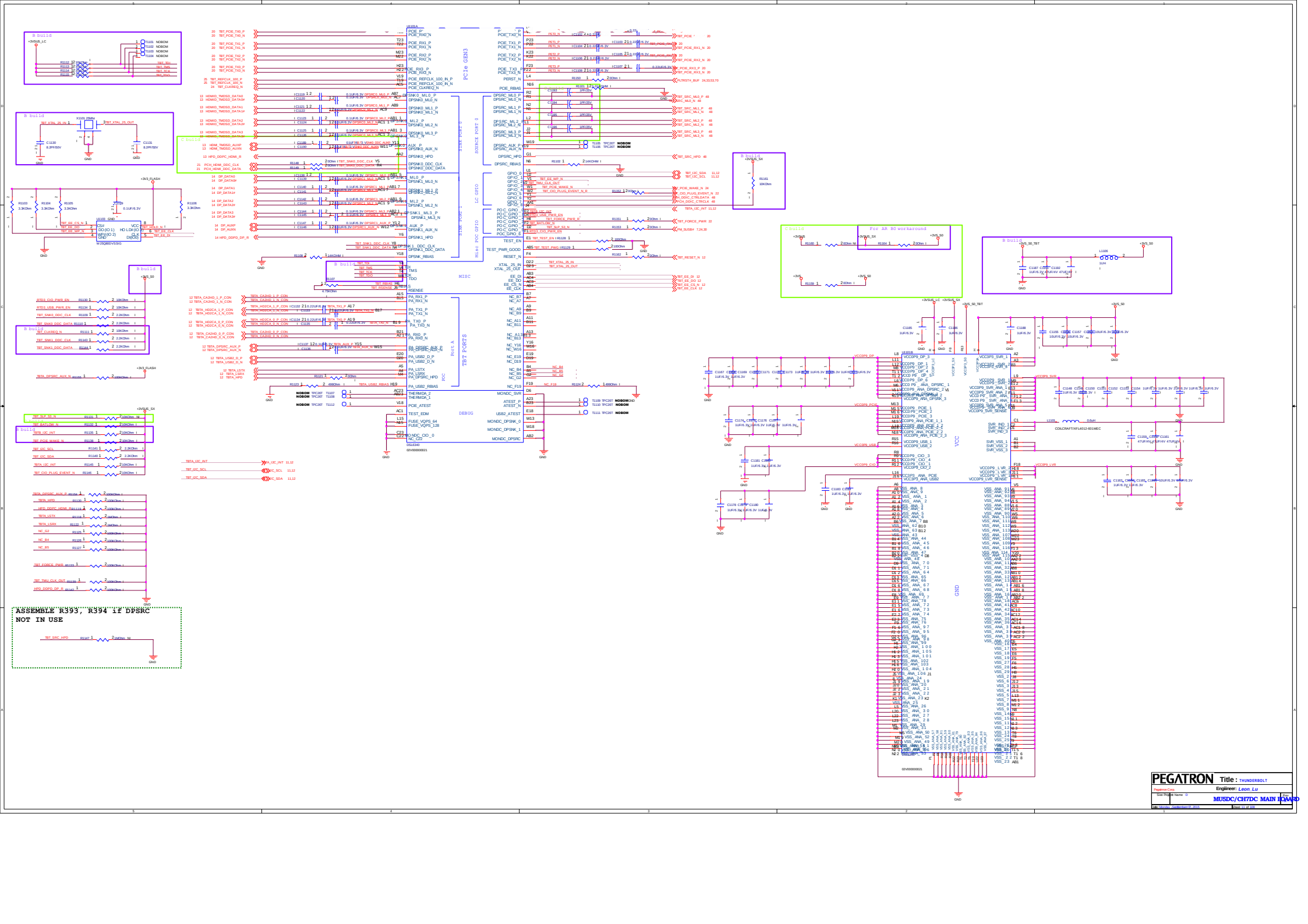
PEGATRON DT-MB RESTRICTED SECRET

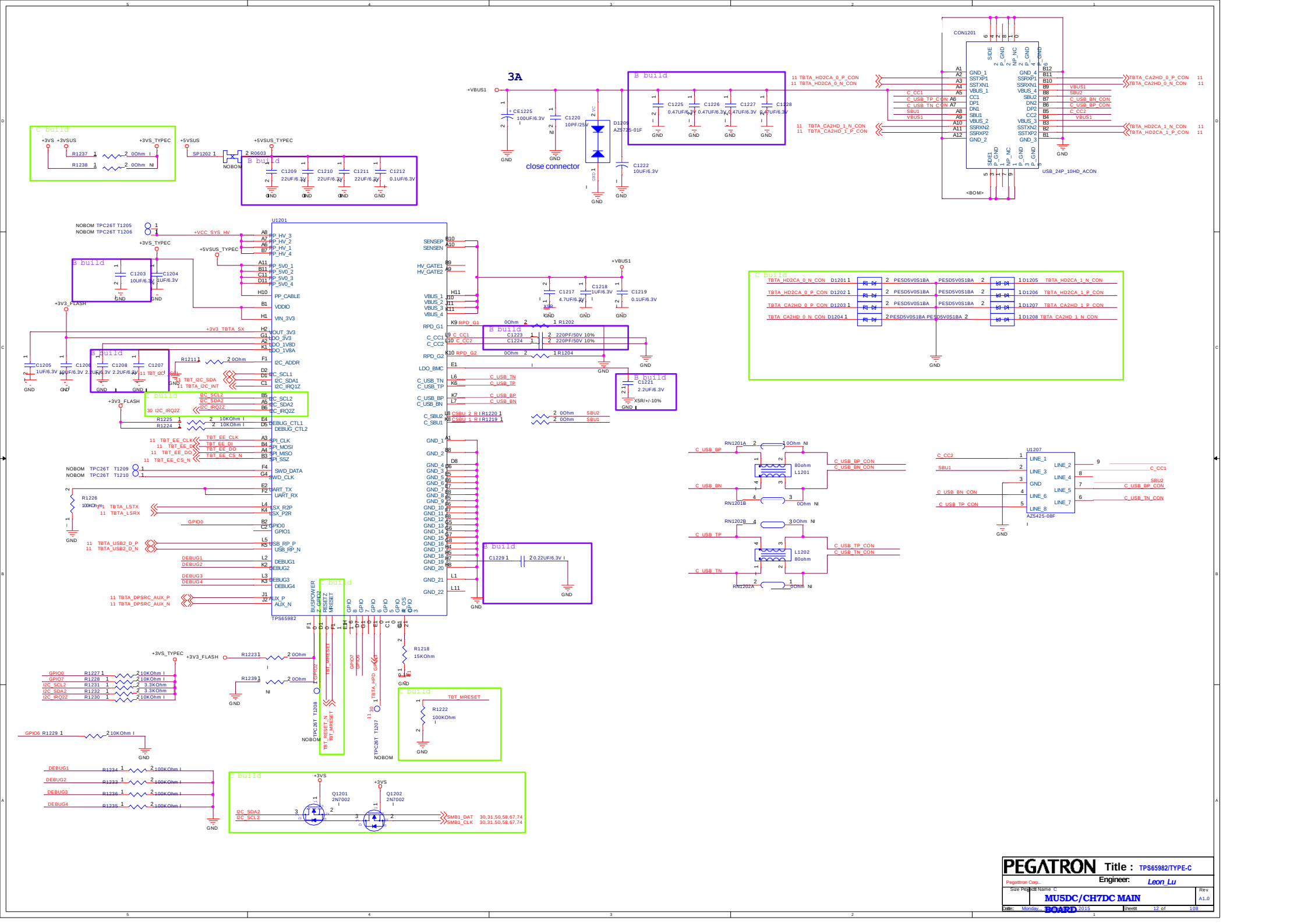
PEGATRON Title : CPU_POWER2

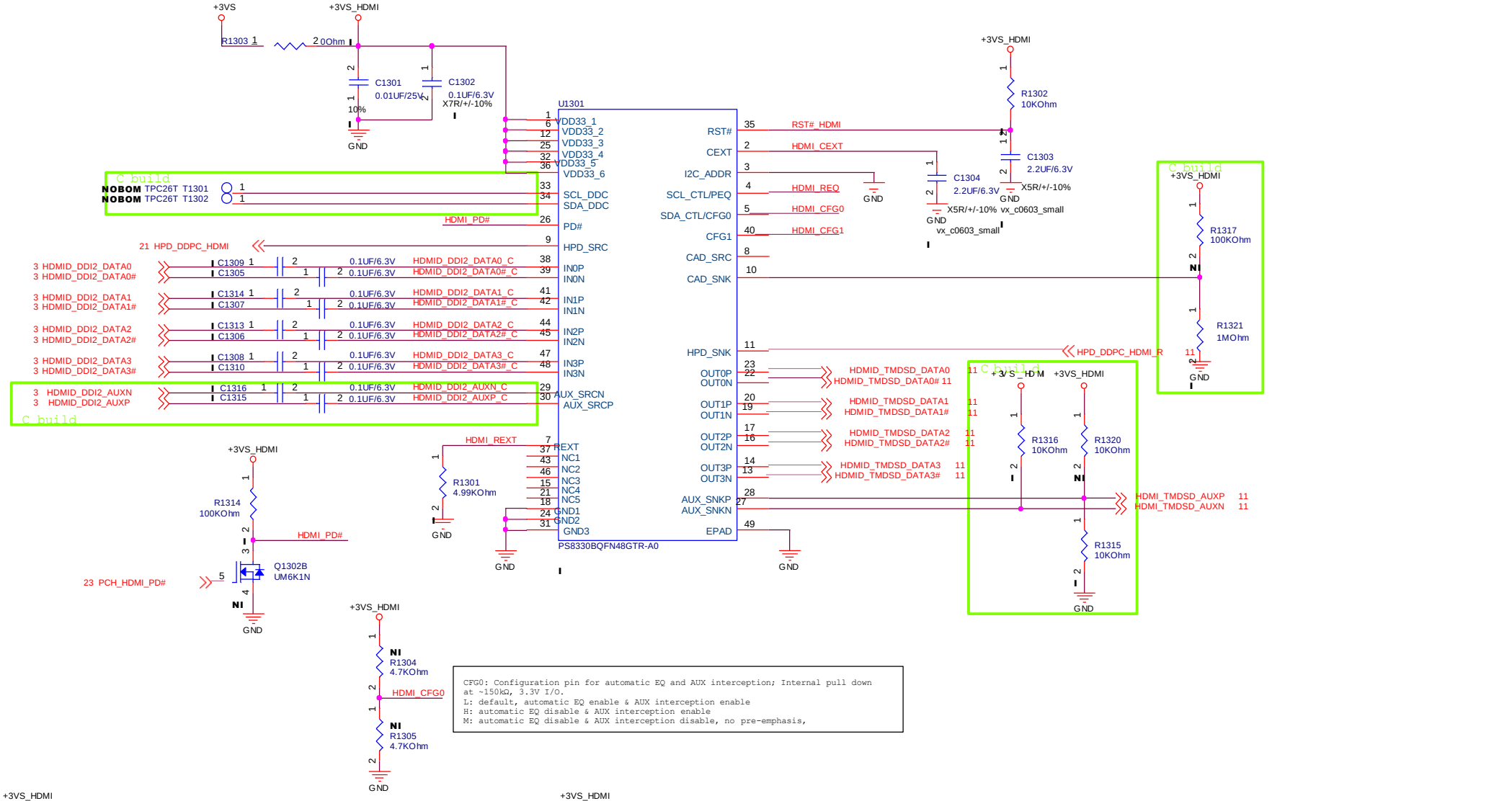
Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A3	MU5DC/CH7DC MAIN BOARD	A1.0

Date: Monday, September 21, 2015 Sheet 10 of 108


ASSEMBLY R393, R394 IF DPSRC NOT IN USE
PEGATRON
Title : THUNDERBOLT
Engineer: Leon_Lu
MUSDC/CH7DC MAIN BOARD


3A
close connector
CON1201
USB_24P_10HD_ACON
U1201
TPS65982
Title : TPS65982/TYPE-C
Engineer: Leon_Lu
MU5DC/CH7DC MAIN BOARD
Rev A1.0

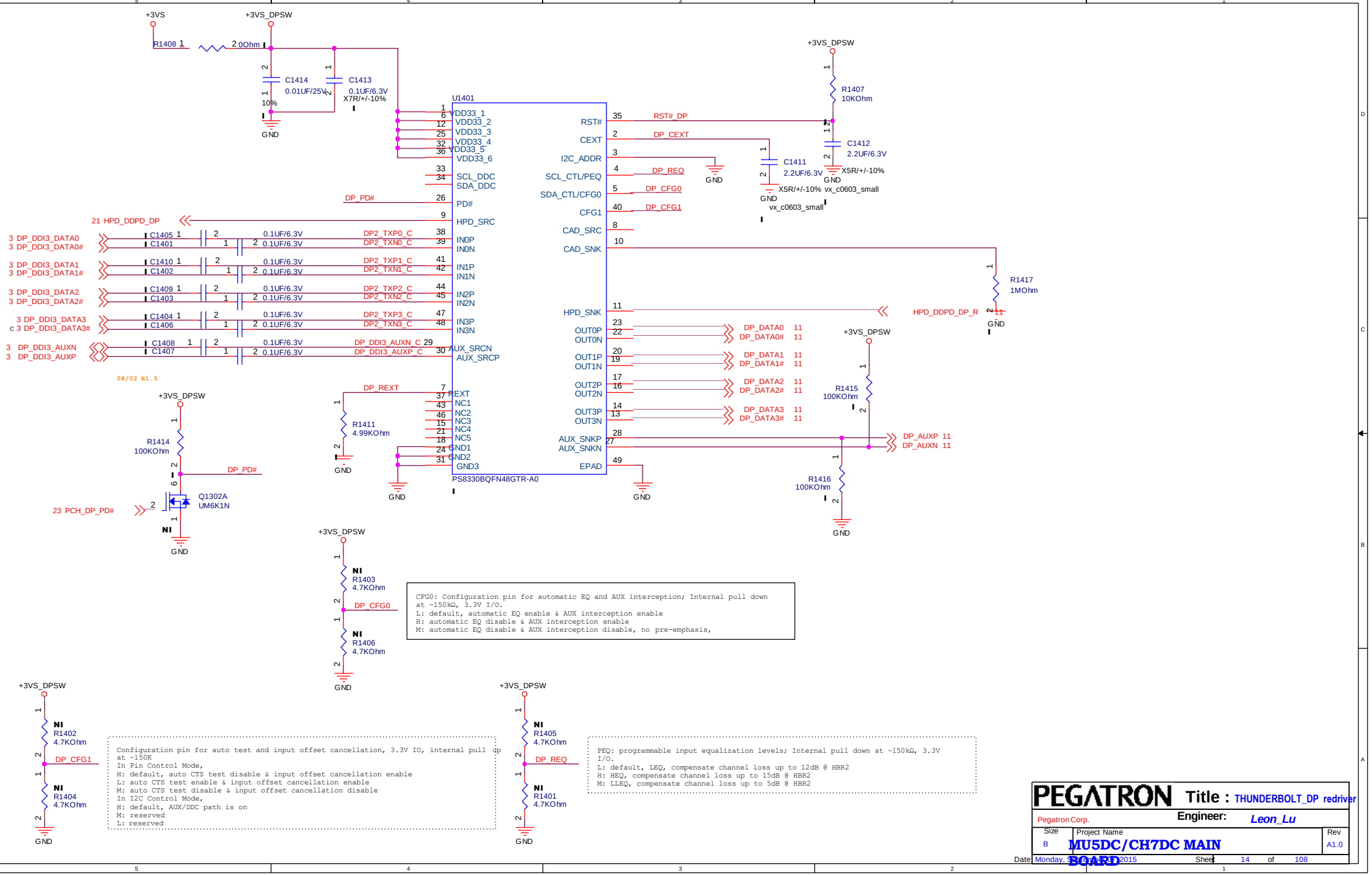


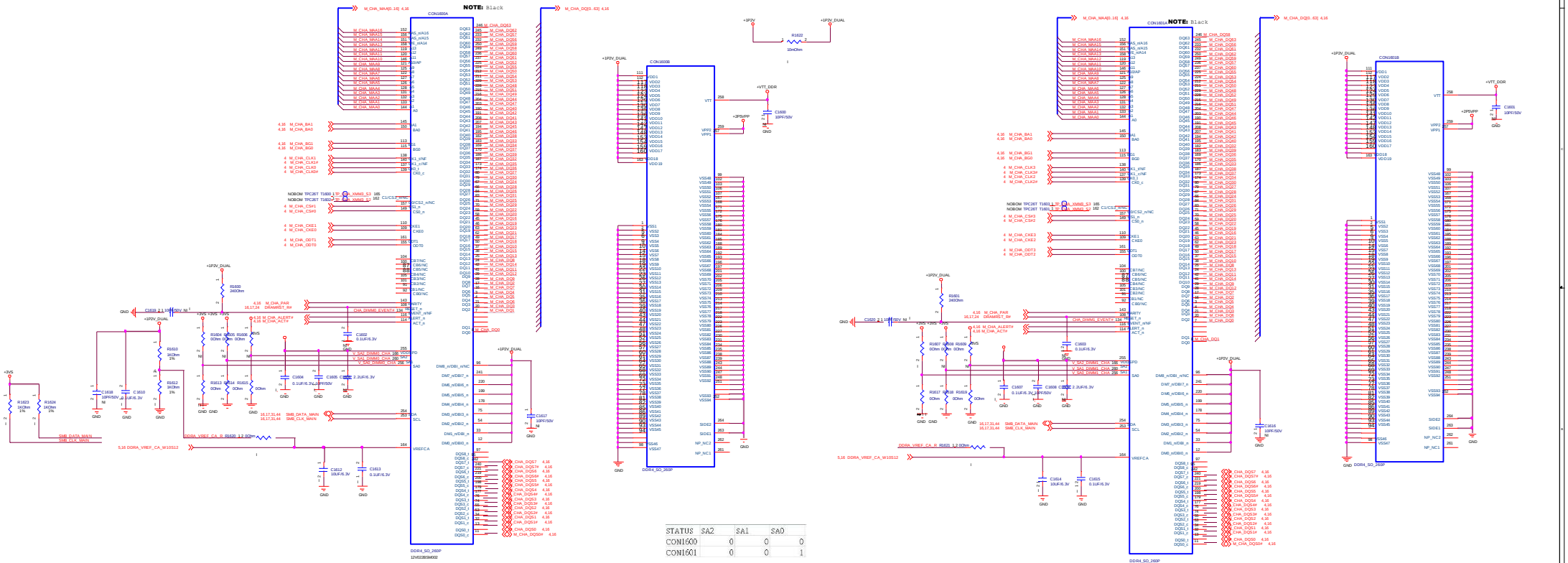
PEGATRON Title : THUNDERBOLT_HDMI redriver

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
B	MU5DC/CH7DC MAIN BOARD	A1.0

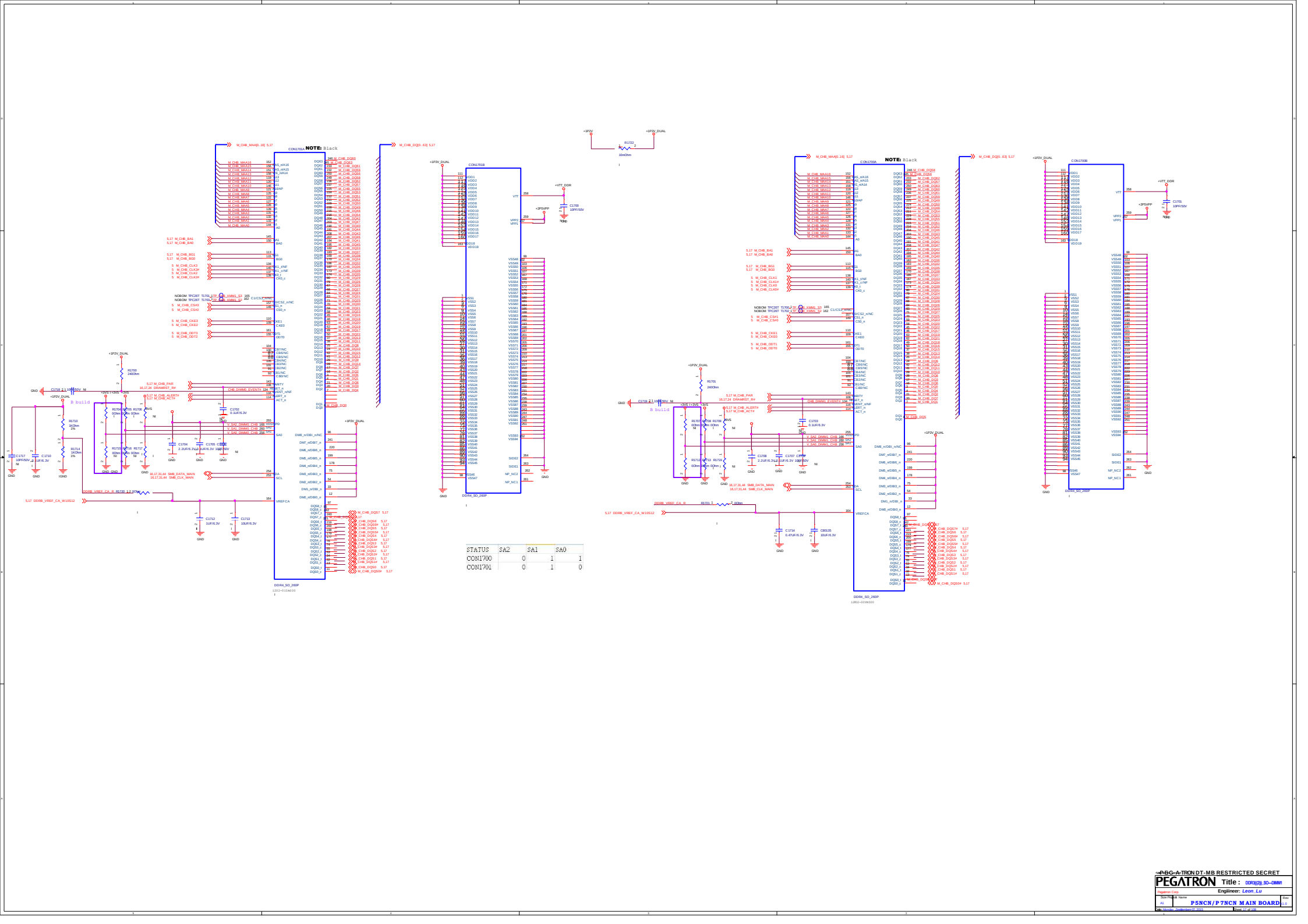
Date: Monday, [illegible] 2015 Sheet 13 of 108


+3VS
+3VS_DPSW
R1408 1
2 0Ohm
C1414
0.01UF/25V
10%
C1413
0.1UF/6.3V
X7R/+/-10%
GND
U1401
VDD33_1
VDD33_2
VDD33_3
VDD33_4
VDD33_5
VDD33_6
SCL_DDC
SDA_DDC
PD#
HPD_SRC
IN0P
IN0N
IN1P
IN1N
IN2P
IN2N
IN3P
IN3N
AUX_SRCN
AUX_SRCP
REXT
NC1
NC2
NC3
NC4
NC5
GND1
GND2
GND3
PS8330BQFN48GTR-A0
RST#
CEXT
I2C_ADDR
SCL_CTL/PEQ
SDA_CTL/CFG0
CFG1
CAD_SRC
CAD_SNK
HPD_SNK
OUT0P
OUT0N
OUT1P
OUT1N
OUT2P
OUT2N
OUT3P
OUT3N
AUX_SNKP
AUX_SNKN
EPAD
RST#_DP
DP_CEXT
DP_REQ
DP_CFG0
DP_CFG1
R1407
10KOhm
C1412
2.2UF/6.3V
X5R/+/-10%
C1411
2.2UF/6.3V
X5R/+/-10%
vx_c0603_small
R1417
1MOhm
HPD_DDPD_DP_R
DP_PD#
21 HPD_DDPD_DP
3 DP_DDI3_DATA0
3 DP_DDI3_DATA0#
3 DP_DDI3_DATA1
3 DP_DDI3_DATA1#
3 DP_DDI3_DATA2
3 DP_DDI3_DATA2#
3 DP_DDI3_DATA3
3 DP_DDI3_DATA3#
3 DP_DDI3_AUXN
3 DP_DDI3_AUXP
C1405
C1401
C1410
C1402
C1409
C1403
C1404
C1406
C1408
C1407
0.1UF/6.3V
DP2_TXP0_C
DP2_TXN0_C
DP2_TXP1_C
DP2_TXN1_C
DP2_TXP2_C
DP2_TXN2_C
DP2_TXP3_C
DP2_TXN3_C
DP_DDI3_AUXN_C
DP_DDI3_AUXP_C
DP_DATA0
DP_DATA0#
DP_DATA1
DP_DATA1#
DP_DATA2
DP_DATA2#
DP_DATA3
DP_DATA3#
DP_AUXP
DP_AUXN
R1415
100KOhm
R1416
100KOhm
R1411
4.99KOhm
R1414
100KOhm
Q1302A
UM6K1N
23 PCH_DP_PD#
NI
R1403
4.7KOhm
R1406
4.7KOhm
R1402
4.7KOhm
R1404
4.7KOhm
R1405
4.7KOhm
R1401
4.7KOhm
08/02 R1.5
CFG0: Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis,
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K
In Pin Control Mode,
H: default, auto CTS test disable & input offset cancellation enable
L: auto CTS test enable & input offset cancellation enable
M: auto CTS test disable & input offset cancellation disable
In I2C Control Mode,
H: default, AUX/DDC path is on
M: reserved
L: reserved
PEQ: programmable input equalization levels; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, LEQ, compensate channel loss up to 12dB @ HBR2
H: HEQ, compensate channel loss up to 15dB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2
PEGATRON
Title : THUNDERBOLT_DP redriver
Pegatron Corp.
Engineer: Leon_Lu
Size B
Project Name MU5DC/CH7DC MAIN BOARD
Rev A1.0
Date: Monday, September 21, 2015
Sheet 14 of 108



NOTE: Black

PEGATRON	Title : DDR3(1)_SO-DIMM0		
Pegatron Corp.	Engiineer: Leon_Lu		
Size	Project Name		Rev
A1	P5NCN/P7NCN MAIN BOARD		1.0
Date: Monday, September 09, 2013		Sheet 16 of 100	



PEGATRON Title : DDR3(2)_SO-DIMM

Engineer: Leon_Lu

Size: A1 | Project Name: P5NCN/P7NCN MAIN BOARD | Rev: 1.0

Date: Monday, September 05, 2016 | Sheet 17 of 58

NOTE:
PCH EDS 0.7

NOTE:
Lynx Point: USB2[0:13]
Sunrise Point PCH-H: USB2[1:14]

U2000A

DMI

6 DMI_TXP0 → N27 DMI_RXP0
6 DMI_TXN0 → L27 DMI_RXN0
6 DMI_RXP0 → B27 DMI_TXP0
6 DMI_RXN0 → C27 DMI_TXN0

6 DMI_TXP1 → G24 DMI_RXP1
6 DMI_TXN1 → E24 DMI_RXN1
6 DMI_RXP1 → A28 DMI_TXP1
6 DMI_RXN1 → B28 DMI_TXN1

6 DMI_TXP2 → E26 DMI_RXP2
6 DMI_TXN2 → G27 DMI_RXN2
6 DMI_RXP2 → C29 DMI_TXP2
6 DMI_RXN2 → B29 DMI_TXN2

6 DMI_TXP3 → K29 DMI_RXP3
6 DMI_TXN3 → L29 DMI_RXN3
6 DMI_RXP3 → A30 DMI_TXP3
6 DMI_RXN3 → B30 DMI_TXN3

USB2.0

USB2P_1	AG7 IPD 14~24KOHM	USBP1 52	OC0
USB2N_1	AF5 IPD 14~24KOHM	USBN1 52	
USB2P_2	AD7 IPD 14~24KOHM	USBP2 55	OC2
USB2N_2	AD5 IPD 14~24KOHM	USBN2 55	
USB2P_3	AG10 IPD 14~24KOHM	USBP3 67	OC1
USB2N_3	AG8 IPD 14~24KOHM	USBN3 67	
USB2P_4	AE2 IPD 14~24KOHM	USBP4 67	
USB2N_4	AE1 IPD 14~24KOHM	USBN4 67	
USB2P_5	AC3 IPD 14~24KOHM		
USB2N_5	AC2 IPD 14~24KOHM		
USB2P_6	AF3 IPD 14~24KOHM		
USB2N_6	AF2 IPD 14~24KOHM		
USB2P_7	AB2 IPD 14~24KOHM	USBP7 53	
USB2N_7	AB3 IPD 14~24KOHM	USBN7 53	
USB2P_8	AL7 IPD 14~24KOHM	USBP8 43	
USB2N_8	AL8 IPD 14~24KOHM	USBN8 43	
USB2P_9	AA2 IPD 14~24KOHM	USBP9 45	
USB2N_9	AA1 IPD 14~24KOHM	USBN9 45	
USB2P_10	AJ7 IPD 14~24KOHM	USBP10 67	
USB2N_10	AJ8 IPD 14~24KOHM	USBN10 67	
USB2P_11	W3 IPD 14~24KOHM		
USB2N_11	W2 IPD 14~24KOHM		
USB2P_12	AD2 IPD 14~24KOHM		
USB2N_12	AD3 IPD 14~24KOHM		
USB2P_13	V1 IPD 14~24KOHM		
USB2N_13	V2 IPD 14~24KOHM		
USB2P_14	AJ13 IPD 14~24KOHM		
USB2N_14	AJ11 IPD 14~24KOHM		

LEFT USB3.0
SMALL CARD USB3.0
M.2 BT
TOUCH
WEBCAM
CARD READER

PCIE/USB/ SATA

C build
3D CAMERA
43 USB3_TX_P5 → B16 PCIE1_TXP/USB3_7_TXP
43 USB3_TX_N5 → A16 PCIE1_TXN/USB3_7_TXN
43 USB3_RX_P5 → G15 PCIE1_RXP/USB3_7_RXP
43 USB3_RX_N5 → H15 PCIE1_RXN/USB3_7_RXN

C19 PCIE2_TXP/USB3_8_TXP
B19 PCIE2_TXN/USB3_8_TXN
G17 PCIE2_RXP/USB3_8_RXP
E17 PCIE2_RXN/USB3_8_RXN

M.2 WLAN
53 PCIE_TXP7_WLAN → C2020 1 — 2 0.1UF/6.3V → PCIE_TXP7_WLAN_C → C20 PCIE3_TXP/USB3_9_TXP
53 PCIE_TXN7_WLAN → C2021 1 — 2 0.1UF/6.3V → PCIE_TXN7_WLAN_C → B20 PCIE3_TXN/USB3_9_TXN
53 PCIE_RXP7_WLAN → K17 PCIE3_RXP/USB3_9_RXP
53 PCIE_RXN7_WLAN → L17 PCIE3_RXN/USB3_9_RXN

LAN RTL8111H
33 LAN_TXP → C2012 1 — 2 0.1UF/6.3V → PCIE_LAN_TXP → A21 PCIE4_TXP/USB3_10_TXP
33 LAN_TXN → C2013 1 — 2 0.1UF/6.3V → PCIE_LAN_TXN → B21 PCIE4_TXN/USB3_10_TXN
33 LAN_RXP → G19 PCIE4_RXP/USB3_10_RXP
33 LAN_RXN → E20 PCIE4_RXN/USB3_10_RXN

Thunderbolt
11 TBT_PCIE_TX0_P → C2000 1 — 2 0.1UF/6.3V → TBT_PCIE_TX0_P_C → C22 PCIE5_TXP
11 TBT_PCIE_TX0_N → C2001 1 — 2 0.1UF/6.3V → TBT_PCIE_TX0_N_C → D22 PCIE5_TXN
11 TBT_PCIE_RX0_P → L19 PCIE5_RXP
11 TBT_PCIE_RX0_N → K19 PCIE5_RXN

11 TBT_PCIE_TX1_P → C2015 1 — 2 0.1UF/6.3V → TBT_PCIE_TX1_P_C → A23 PCIE6_TXP
11 TBT_PCIE_TX1_N → C2014 1 — 2 0.1UF/6.3V → TBT_PCIE_TX1_N_C → B22 PCIE6_TXN
11 TBT_PCIE_RX1_P → E22 PCIE6_RXP
11 TBT_PCIE_RX1_N → G22 PCIE6_RXN

11 TBT_PCIE_TX2_P → C2017 1 — 2 0.1UF/6.3V → TBT_PCIE_TX2_P_C → B23 PCIE7_TXP
11 TBT_PCIE_TX2_N → C2016 1 — 2 0.1UF/6.3V → TBT_PCIE_TX2_N_C → C23 PCIE7_TXN
11 TBT_PCIE_RX2_P → K22 PCIE7_RXP
11 TBT_PCIE_RX2_N → L22 PCIE7_RXN

11 TBT_PCIE_TX3_P → C2019 1 — 2 0.1UF/6.3V → TBT_PCIE_TX3_P_C → B24 PCIE8_TXP
11 TBT_PCIE_TX3_N → C2018 1 — 2 0.1UF/6.3V → TBT_PCIE_TX3_N_C → C24 PCIE8_TXN
11 TBT_PCIE_RX3_P → L24 PCIE8_RXP
11 TBT_PCIE_RX3_N → K24 PCIE8_RXN

SATA Port1 (SSD)
51 PCIE_SATA_TXP0 → B31 PCIE9_TXP/SATA0A_TXP
51 PCIE_SATA_TXN0 → C31 PCIE9_TXN/SATA0A_TXN
51 PCIE_SATA_RXP0 → H31 PCIE9_RXP/SATA0A_RXP
51 PCIE_SATA_RXN0 → G31 PCIE9_RXN/SATA0A_RXN

SATA Port1 (SSD)
51 PCIE_SATA_TXP1 → B32 PCIE10_TXP/SATA1A_TXP
51 PCIE_SATA_TXN1 → C32 PCIE10_TXN/SATA1A_TXN
51 PCIE_SATA_RXP1 → E29 PCIE10_RXP/SATA1A_RXP
51 PCIE_SATA_RXN1 → G29 PCIE10_RXN/SATA1A_RXN

SATA Port1 (SSD)
51 PCIE_SATA_TXP2 → B33 PCIE11_TXP
51 PCIE_SATA_TXN2 → C33 PCIE11_TXN
51 PCIE_SATA_RXP2 → K31 PCIE11_RXP
51 PCIE_SATA_RXN2 → L31 PCIE11_RXN

SATA Port1 (SSD)
51 PCIE_SATA_TXP3 → A35 PCIE12_TXP
51 PCIE_SATA_TXN3 → B35 PCIE12_TXN
51 PCIE_SATA_RXP3 → H33 PCIE12_RXP
51 PCIE_SATA_RXN3 → G33 PCIE12_RXN

USB3.0

USB3_1_TXP	B11			
USB3_1_TXN	C11			
USB3_1_RXP	A7			
USB3_1_RXN	B7			
USB3_2_TXP/SSIC_1_TXP	A12 USB3_TX_P2_C	C2004 1	2 0.1UF/6.3V	USB3_TX_P2 55
USB3_2_TXN/SSIC_1_TXN	B12 USB3_TX_N2_C	C2005 1	2 0.1UF/6.3V	USB3_TX_N2 55
USB3_2_RXP/SSIC_1_RXP	B8			USB3_RX_P2 55
USB3_2_RXN/SSIC_1_RXN	C8			USB3_RX_N2 55
USB3_3_TXP/SSIC_2_TXP	D13 USB3_TX_P3_C	C2006 1	2 0.1UF/6.3V	USB3_TX_P3 67
USB3_3_TXN/SSIC_2_TXN	C13 USB3_TX_N3_C	C2007 1	2 0.1UF/6.3V	USB3_TX_N3 67
USB3_3_RXP/SSIC_2_RXP	A9			USB3_RX_P3 67
USB3_3_RXN/SSIC_2_RXN	B10			USB3_RX_N3 67
USB3_4_TXP	G13 USB3_TX_P4_C	C2009 1	2 0.1UF/6.3V	USB3_TX_P4 67
USB3_4_TXN	A14 USB3_TX_N4_C	C2011 1	2 0.1UF/6.3V	USB3_TX_N4 67
USB3_4_RXP	G11			USB3_RX_P4 67
USB3_4_RXN	E11			USB3_RX_N4 67
USB3_5_TXP	G14 USB3_TX_P1_C	C2002 1	2 0.1UF/6.3V	USB3_TX_P1 55
USB3_5_TXN	G14 USB3_TX_N1_C	C2003 1	2 0.1UF/6.3V	USB3_TX_N1 55
USB3_5_RXP	H13			USB3_RX_P1 55
USB3_5_RXN	G13			USB3_RX_N1 55
USB3_6_TXP	C15			USB3_TX_P6 67
USB3_6_TXN	B15			USB3_TX_N6 67
USB3_6_RXP	K13			USB3_RX_P6 67
USB3_6_RXN	K15			USB3_RX_N6 67

LEFT USB3.0 (SIDE)
USB3.0
C build
LEFT USB3.0 (SIDE)
USB3.0 CARD

USB2_ID AG2 — IWPU USB2_ID
USB2_VBUSSENSE AD10 — USB2_VBUSSENSE

R2000 1KOhm (1–2) GND
R2001 0Ohm (2–1) GND

SKYLAKE_PCH Rev 0.9

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH_DMI/PCIE
Pegatron Corp. Engineer: Leon_Lu
Size A3 | Project Name MU5DC/CH7DC MAIN BOARD | Rev A1.0
Date: Monday, Sep 15 | Sheet 20 of 108

NOTE:
Check PU/PD

NOTE:
CPU_GP can be used from external sensors for the thermal management.

NOTE:
Check real OC# application

NOTE:
NI SR39(POLYSWITCH)
I SR39(POWER SWITCH)

STATUS	CTL1	CTL2	CTL3	ILIM_SEL
S0(CDP)	1	1	1	1
S3(CDP)	1	1	1	1
S4(DCP)	0	0	1	0
S5(DCP)	0	0	1	0

NOTE:
GPP_F[11:10] for SWITCH#0 to select source from ISH or HOST

NOTE:

SATAXPCIE[0:7]	SATA/PCIE
SATAXPCIE0	SATA0A/PCIE9 SATA0B/PCIE13
SATAXPCIE1	SATA1A/PCIE10 SATA1B/PCIE14
SATAXPCIE2	SATA2/PCIE15
SATAXPCIE3	SATA3/PCIE16
SATAXPCIE4	SATA4/PCIE17
SATAXPCIE5	SATA5/PCIE18
SATAXPCIE6	SATA5/PCIE19
SATAXPCIE7	SATA7/PCIE20

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH_SATA/PCI/EI

PegatronCorp. Engineer: Leon_Lu

Size: A2 | Project Name: MU5DC/CH7DC MAIN | Rev: A1.0

Date: December 07, 2015 | Sheet 21 of 101

NOTE:
eSPI operates at 1.8V

NOTE:
Check SERIRQ & PIRQA volt level

NOTE:
Be carful on LPC/eSPI layout routing
eSPI clock/data mismatch < 500mil

NOTE:
Check GPP_A0 power well

NOTE:
ESPI_ALERT[0:1]# & ESPI_CS1# are Server Only
ESPI interface are Primary Well

NOTE:
Check PCA spec for specific implementation

NOTE:
CLKOUT_LPC[0:1] are 24MHz(TBD) with Rs=22ohm
ESPI_CLK is xxHz with Rs=15ohm

NOTE:
Check PCA spec SIO_SMI# to GPIO or SMI#?

NOTE:
TBD; Check ISH GPIO[0:7]
PU/PD and power rail

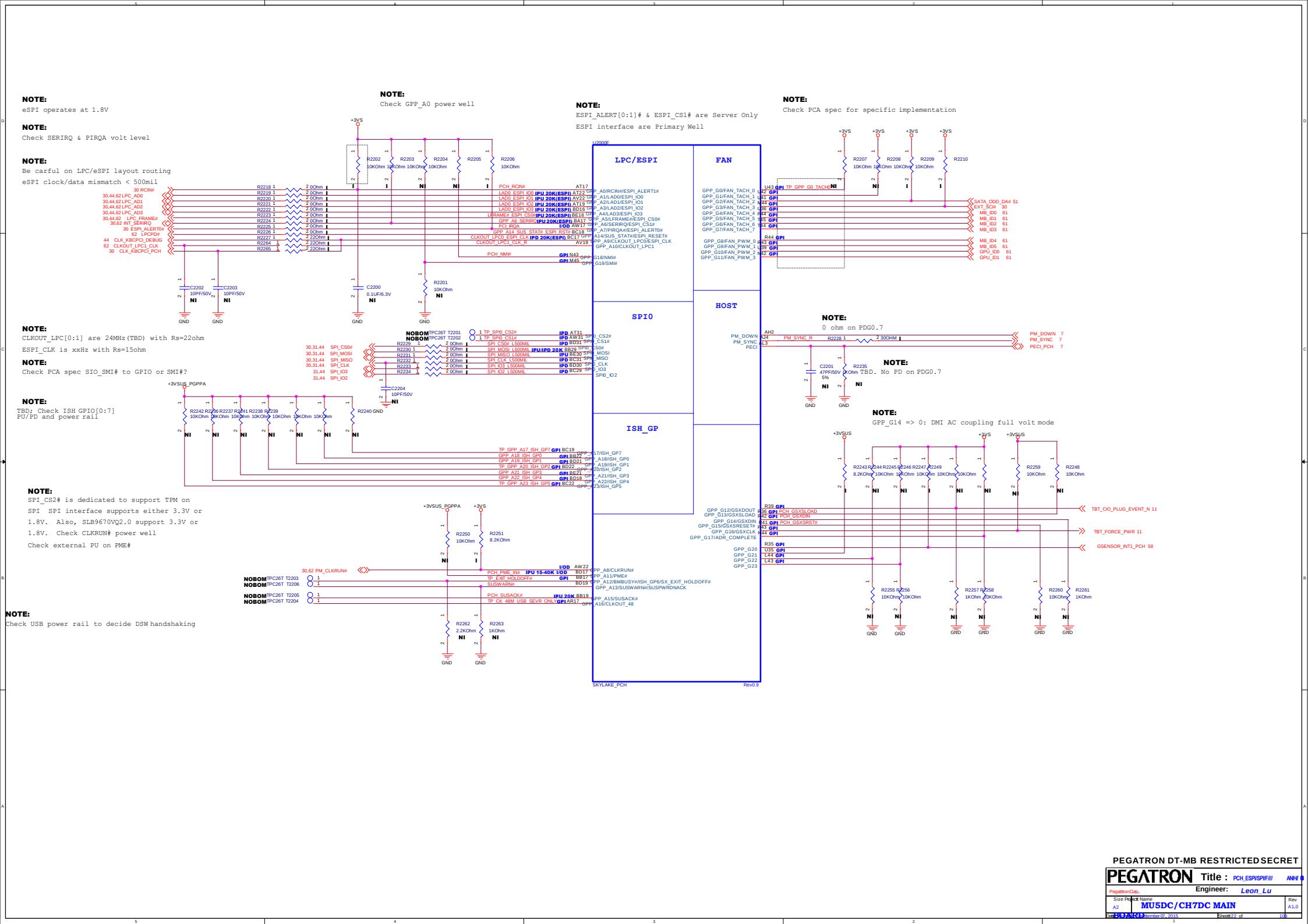
NOTE:
SPI_CS2# is dedicated to support TPM on
SPI SPI interface supports either 3.3V or
1.8V. Also, SLB9670VQ2.0 support 3.3V or
1.8V. Check CLKRUN# power well
Check external PU on PME#

NOTE:
Check USB power rail to decide DSW handshaking

NOTE:
0 ohm on PDG0.7

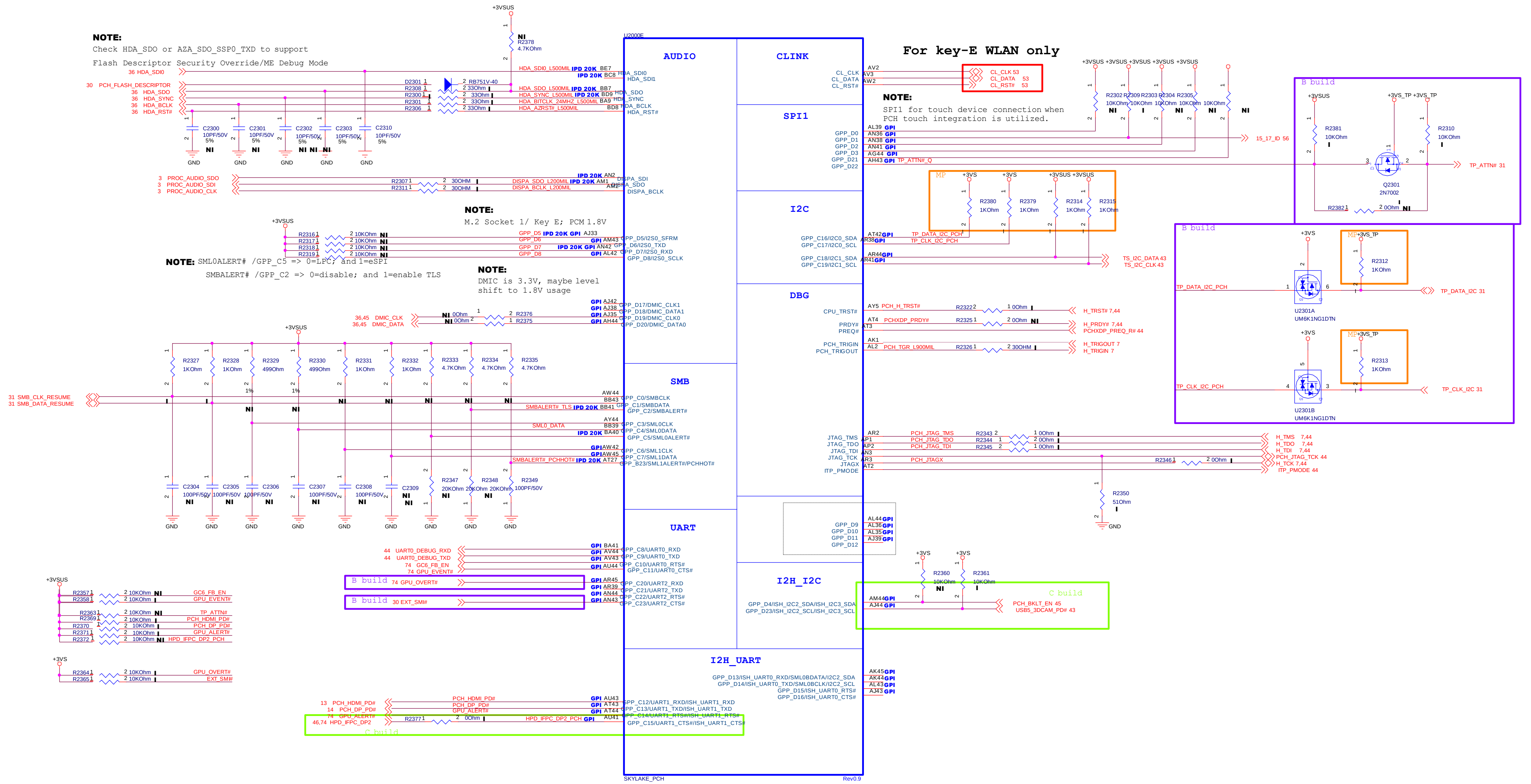
NOTE:
TBD. No PD on PDG0.7

NOTE:
GPP_G14 => 0: DMI AC coupling full volt mode



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH_ESPI/SPI/F/I/ ANH 0
PegatronCorp. Engineer: Leon_Lu
Size Project Name MU5DC/CH7DC MAIN Rev A1.0
Date: December 07, 2015 Sheet 22 of 108


NOTE:
Check HDA_SDO or AZA_SDO_SSP0_TXD to support
Flash Descriptor Security Override/ME Debug Mode
NOTE:
M.2 Socket 1/ Key E; PCM 1.8V
NOTE: SML0ALERT# /GPP_C5 => 0=LPC; and 1=eSPI
SMBALERT# /GPP_C2 => 0=disable; and 1=enable TLS
NOTE:
DMIC is 3.3V, maybe level
shift to 1.8V usage
For key-E WLAN only
NOTE:
SPI1 for touch device connection when
PCH touch integration is utilized.
U2000E
AUDIO
CLINK
SPI1
I2C
DBG
SMB
UART
I2H_I2C
I2H_UART
SKYLAKE_PCH
Rev0.9
B build
MP
C build

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON

Title : PCH_AUDIO/CLK/I2C/UART

Pegatron Corp.

Engineer: Leon_Lu

Size	Project Name	Rev
A2	MU5DC/CH7DC MAIN BOARD	A1.0

Date: September 07, 2015 Sheet 23 of 108

NOTE:
GPP_B22/GSPI1_MOSI
Offset 3410h:Bit 10
0: SPI
1: LPC

NOTE:
GSPI is not the same as SPI
It's used mainly for sensor

NOTE:
GSPI0_MOSI/GPP_B18
0 = Disable "No Reboot" mode.
1 = Enable "No Reboot" mode
(PCH will disable the TCO Timer system reboot feature).

NOTE:
HP PCA spec request probe points

NOTE:
1. DRAM_RESET# used on DDR3L, DDR4. Not applicable to LPDDR3
2. Check PCA spec if we need isolation CKT since DRAM_RESET# is changed from SHB processor to SKL PCH assertion 3.Also be careful while changing push-pull to OD
4. PU 475ohm on Zumba Beach CRB 0.5

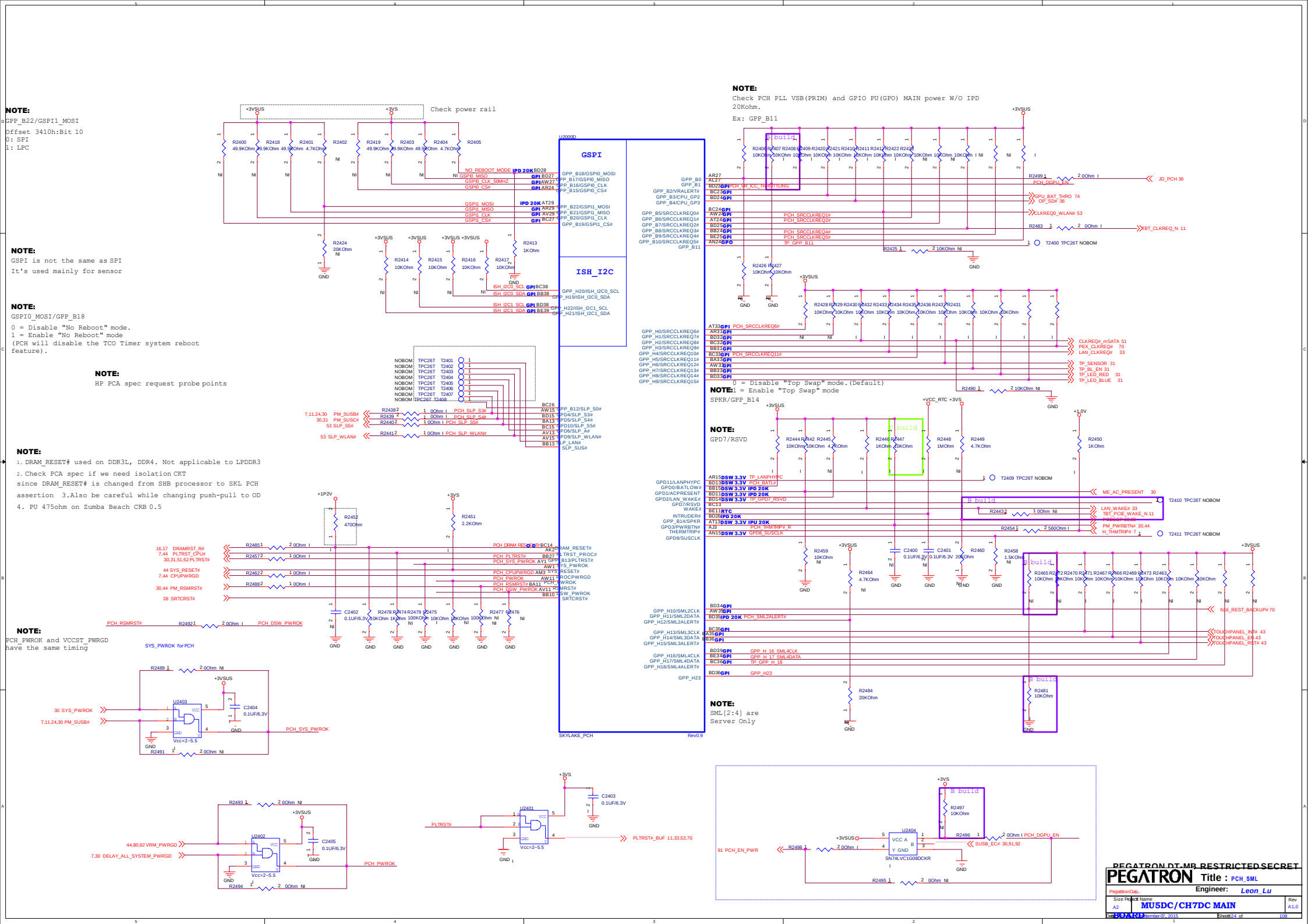
NOTE:
PCH_PWROK and VCCST_PWRGD have the same timing

NOTE:
Check PCH PLL VSB(PRIM) and GPIO PU(GPO) MAIN power W/O IPD 20Kohm.
Ex: GPP_B11

NOTE:
0 = Disable "Top Swap" mode.(Default)
1 = Enable "Top Swap" mode
SPKR/GPP_B14

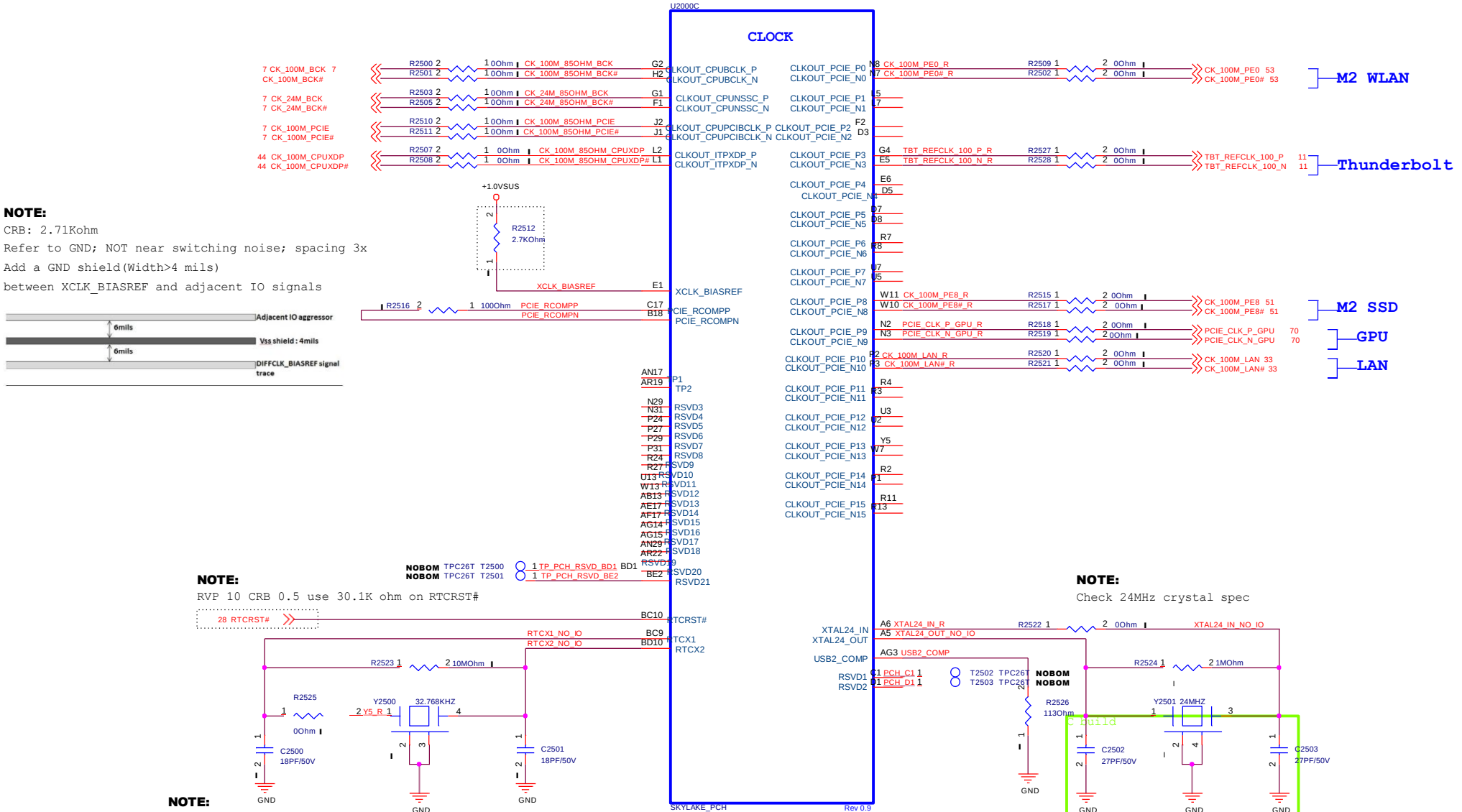
NOTE:
GPD7/RSVD

NOTE:
SML[2:4] are Server Only



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH_SML
PegatronCorp. Engineer: Leon_Lu
Size A2 | Project Name MU5DC/CH7DC MAIN | Rev A1.0
Date: Tuesday, September 07, 2015 | Sheet 24 of 108



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH_CLOCK

Pegatron Corp. Engineer: Leon_Lu

Size: A3 Project Name: MU5DC/CH7DC MAIN Rev: A1.0

Date: Monday, August 17, 2015 Sheet 25 of 108

BOARD

NOTE:
Add 2x 22uF(instead of 47uF) 0603 caps
on 3.3V/1.8V/1.0V plane at PCH
Check 22uF qty on power CKT

NOTE:
Check real C TO implementation to decide VccGPIO rail is 3.3V or 1.8V

U2000G

PRIMARY
CLOCK
MPHY
SPI
VCCGPIO
PRIMARY

+1.0VSUS
R2613 1 2 10mOhm +1V_PRIM_W12MIL
Icc(max):6.01A
C2600 22UF/6.3V
C2601 22UF/6.3V
GND
AL22 VCCPRIM_1p0_17
AJ20 AJ21 AJ23 AJ25 AC17 AD15 Y25 Y23 AA26 AA23 AA28 AC28 AE26 AE23 AC26 AC23
VCCPRIM_1p0_13 VCCPRIM_1p0_14 VCCPRIM_1p0_15 VCCPRIM_1p0_16 VCCPRIM_1p0_6 VCCPRIM_1p0_10 VCCPRIM_1p0_2 VCCPRIM_1p0_1 VCCPRIM_1p0_4 VCCPRIM_1p0_3 VCCPRIM_1p0_5 VCCPRIM_1p0_9 VCCPRIM_1p0_12 VCCPRIM_1p0_11 VCCPRIM_1p0_8 VCCPRIM_1p0_7

+3VSUS_PGPPA
B build
SP2601 1 2 R0603 NOBOM
+3VSUS
Icc(max):0.082A
BA31 VCCPGPPA
Icc(max):0.408A
BC42 VCCPGPPBCH1 BD40 VCCPGPPBCH2 AJ41 VCCPGPPEF1 AL41 VCCPGPPEF2 AD41 VCCPGPPG
R2615 1 2 0Ohm +3VSUS
B build
C2630 C2602 0.1UF/6.3V 0.1UF/6.3V
C2603 0.1UF/6.3V
C2604 0.1UF/6.3V
GND

NOTE:
Place 0.1uF near U3.BC42/ AJ41/ AD41 pins

NOTE:
Add 2x 22uF(instead of 47uF) 0603 caps
on 3.3V/1.8V/1.0V plane at PCH
Check 22uF qty on power CKT

+1.0VSUS
R2604 0Ohm
Icc(max):0.006A +V1P0A_VCCF24_W15MIL
C2605 22UF/6.3V
C2606 22UF/6.3V NI
C2607 1UF/6.3V
GND
K2 K3 VCCCLK5_1 VCCCLK5_2
+1.0VSUS
N17 R19 U20 V17 R17 VCCCLK1 VCCCLK3 VCCCLK4 VCCCLK2_2 VCCCLK2_1

NOTE:
Reserve 0 ohm/0603 for 2.2uH Series Inductor

Icc(max):0.232A

+3VSUS
R2603 0Ohm
Icc(max):0.078A
BC44 +VCCPGPPCD_W15MIL 2
VCCPGPPD3 BA45 VCCPGPPD1 BC45 VCCPGPPD4 BB45 VCCPGPPD2

NOTE:

GPIO Group	Power Pins	Voltage
Primary Well Group A(GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B(GPP_B) Primary Well Group C(GPP_C) Primary Well Group H(GPP_H)	VCCPGPPBCH	1.8V or 3.3V
Primary Well Group D(GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E(GPP_E) Primary Well Group F(GPP_F)	VCCPGPPEF	1.8V or 3.3V
Primary Well Group G(GPP_G)	VCCPGPPG	1.8V or 3.3V
Primary Well Group I(GPP_I)	VCCPRIM_3P3	3.3V
Deep Sleep Well Group(GPD)	VCCDSW_3P3	3.3V

B build
+3VSUS +3VA
VCCSPI1 BE41 VCCSPI3 BE43 VCCSPI2 BE42
Icc(max):0.029A
R2616 1 2 0Ohm
R2619 1 2 0Ohm NI

NOTE:
1.8VSPI(with Quad IO) is expensive than 3.3V part.

+1.0VSUS
Icc(max):0.08A
C2608 22UF/6.3V
C2609 1UF/6.3V
GND
U21 U23 U25 U26 V26 VCCMPHY_1p0_1 VCCMPHY_1p0_2 VCCMPHY_1p0_3 VCCMPHY_1p0_4 VCCMPHY_1p0_5

NOTE:
Place to U3.U21
PDG request 22uF 0805

+1.0VSUS
R2606 0Ohm
Icc(max):0.08A +V1P0A_VCCAMPHYPLL_W25MIL
C2613 22UF/6.3V
C2614 22UF/6.3V NI
C2615 1UF/6.3V
GND
A43 B43 C44 C45 VCCAMPHYPLL_1p0_1 VCCAMPHYPLL_1p0_2 VCCPCIE3PLL_1p0_1 VCCPCIE3PLL_1p0_2

NOTE:
Place to U3.A43

VCCPRIM_3p3_2 BD3 VCCPRIM_3p3_3 BE3 VCCPRIM_3p3_4 BE4 VCCPRIM_3p3_1 AN5
Icc(max):0.117A +VCCPFUSE_W20MIL R2605 2 1 0Ohm +3VSUS
C2610 0.1UF/6.3V
C2611 22UF/6.3V
C2612 22UF/6.3V
GND
VCCRTCPRIM_3p3 BA20
Icc(max):0.001A +3VSUS
C2616 0.1UF/6.3V NI
C2617 1UF/6.3V
GND

NOTE:
Place 0.1uF near U3.AN5

+1.0VSUS
R2607 0Ohm
Icc(max):0.045A +V1P0A_VCCAPLL_W15MIL
C2618 22UF/6.3V
C2619 22UF/6.3V NI
GND
Icc(max):0.03A
V2 AJ5 AL5 AN19 VCCAPLLEBB_1p0 VCCUSB2PLL_1p0_1 VCCUSB2PLL_1p0_2 VCCHDAPLL_1P0

VCCATS AD13
Icc(max):0.007A R2618 1 2 0Ohm +3VS
VCCDSW_3p3_2 W15 VCCDSW_3p3_1 BA24
Icc(max):0.195A R2617 1 2 0Ohm +3VSUS
C2621 1UF/6.3V
C2620 1UF/6.3V
GND

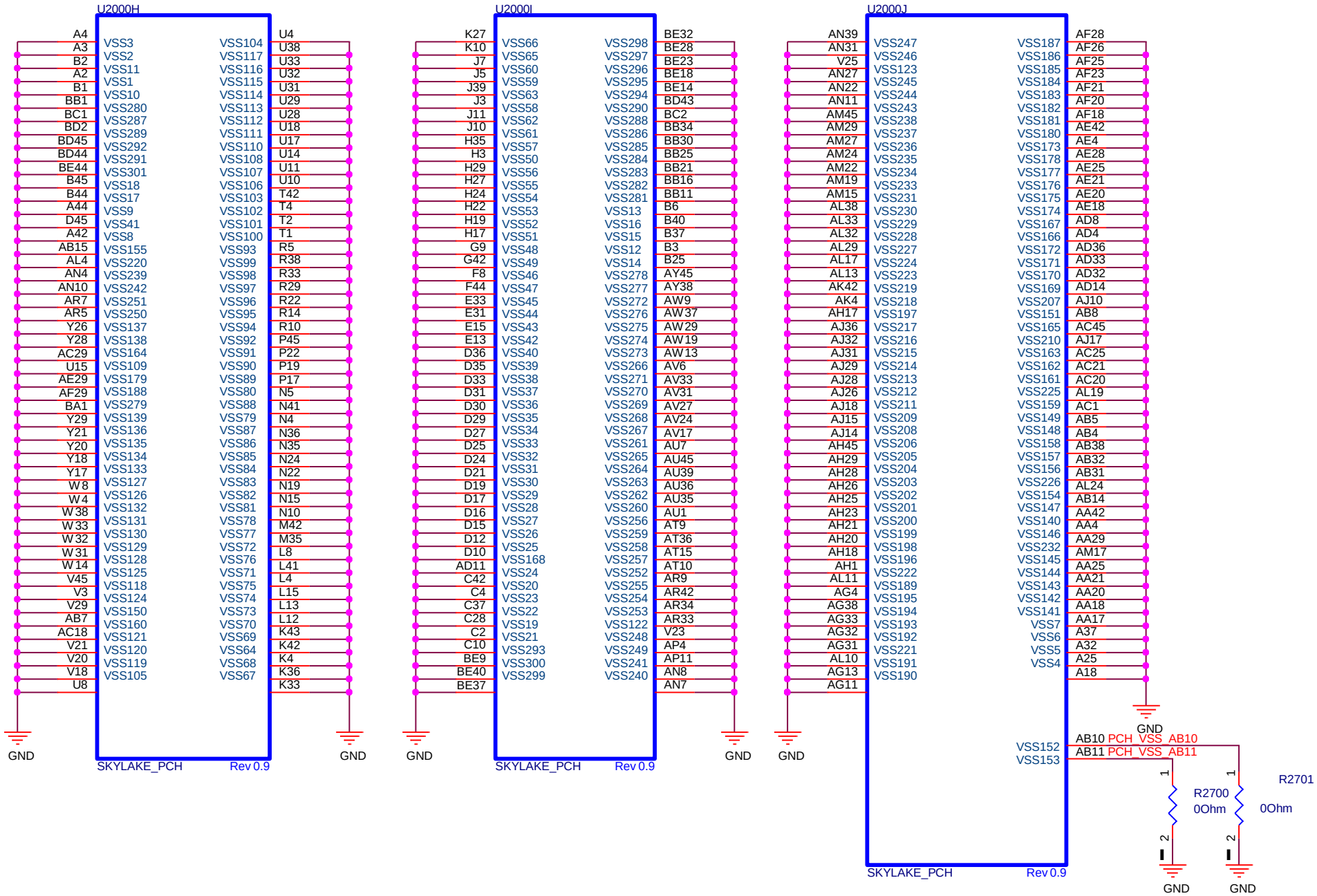
NOTE:
Place 1uF near U3.W15

+1V_DCPDSW BA29 VCCDSW_1p0
DCPRTC BA26 DCPRTC
C2622 1UF/6.3V
C2623 0.1UF/6.3V
GND

VCCHDA BA15
Icc(max):0.06A +DVDDIO_AUDIO_W10MIL R2608 2 1 0Ohm +3VSUS
VCCRTC BA22
Icc(max):0.001A +VCCRTC_W8MIL R2609 2 1 0Ohm +VCC_RTC
C2629 0.1UF/6.3V
C2624 0.1UF/6.3V NI
C2625 1UF/6.3V
GND

SKYLAKE_PCH
02V000000020
Rev 0.9

PEGATRON Title : PCH_VCC
Pegatron Corp. Engineer: Leon_Lu
Size A3 Project Name MU5DC/CH7DC MAIN Rev A1.0
Date: Monday, August 17, 2015 Sheet 26 of 108
BOARD



PEGATRON

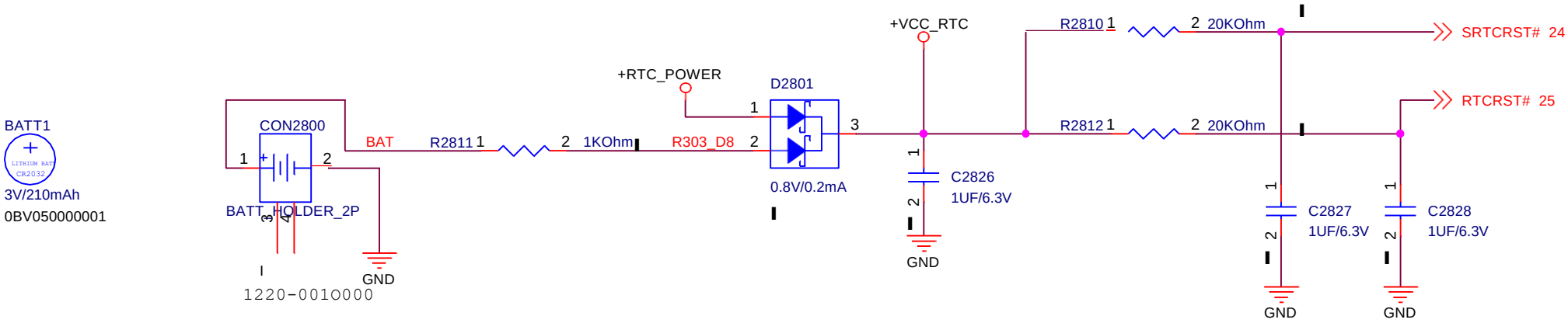
Title : PCH_VSS

Pegatron Corp. Engineer: Leon_Lu

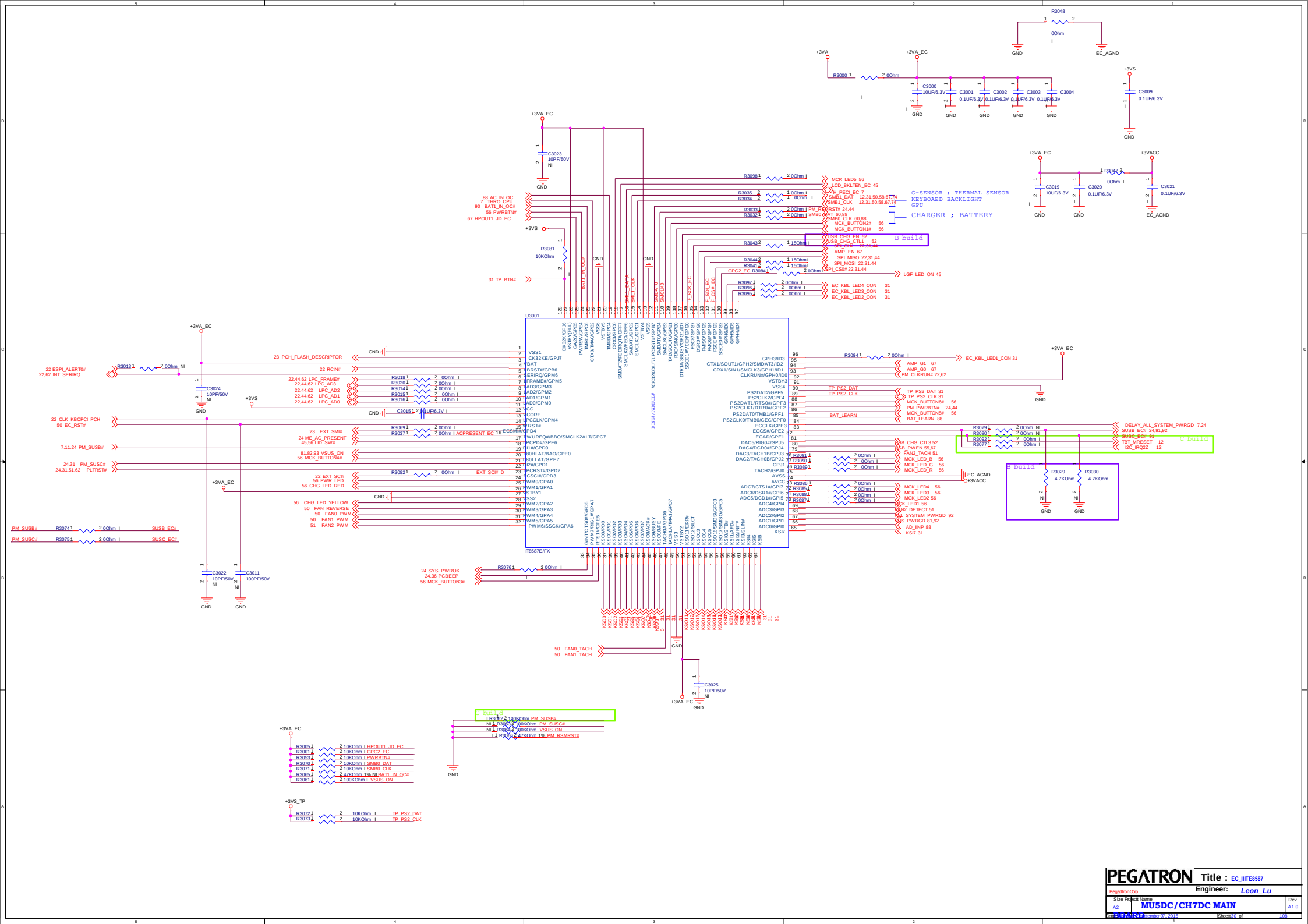
Size	Project Name	Rev
A4	P5NCN/CH7DC MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 27 of 108

RTC

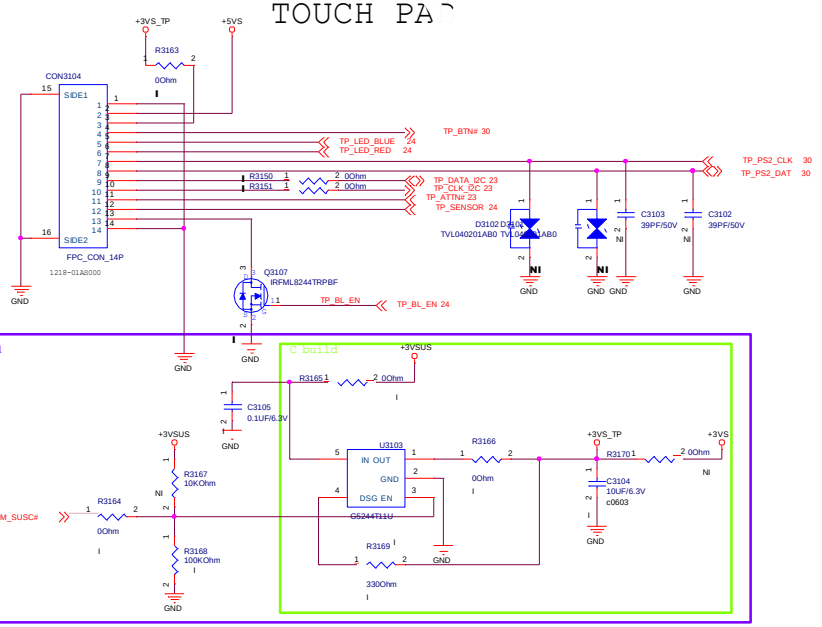


PEGATRON	Title : RTC	
Pegatron Corp.	Engineer: Leon_Lu	
Size: A	Project Name: MU5DC/CH7DC MAIN BOARD	Rev: A1.0
Date: Monday, September 07, 2015	Sheet 28 of 108	

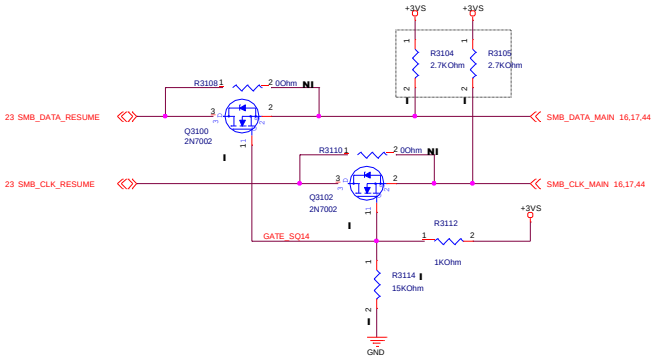

U3001
IT8587E/FX
G-SENSOR ; THERMAL SENSOR
KEYBOAED BACKLIGHT
GPU
CHARGER ; BATTERY
B build
C build
PEGATRON
Title : EC_IITE8587
Engineer: Leon_Lu
Project Name
MU5DC/CH7DC MAIN
Rev
A1.0
Sheet 30 of 101

TOUCH PA

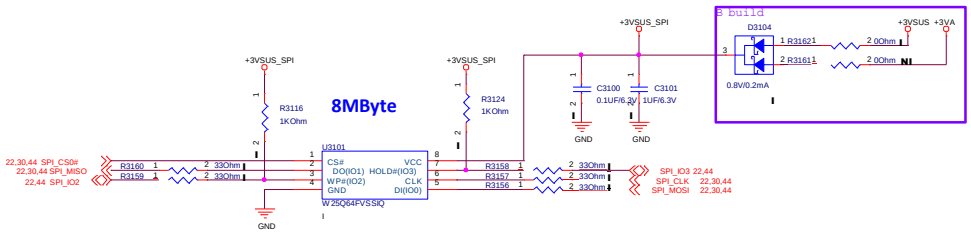
MB Connector side(14pin)	
1	GND
2	+5VS
3	+3VSUS
4	TP_BTN#
5	TP_LED_WITHE
6	TP_LED_RED
7	TP_PS2_CLK
8	TP_PS2_DAT
9	SMB_DATA_RESUME
10	SMB_CLK_RESUME
11	TP_ATTN#
12	TP_SENSOR
13	TP_BL_EN
14	GND



Avoid leakage in S5

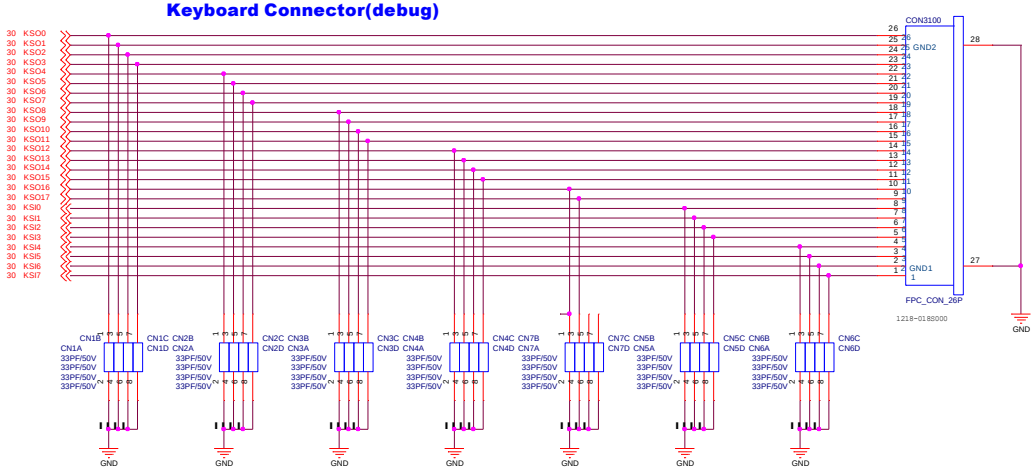


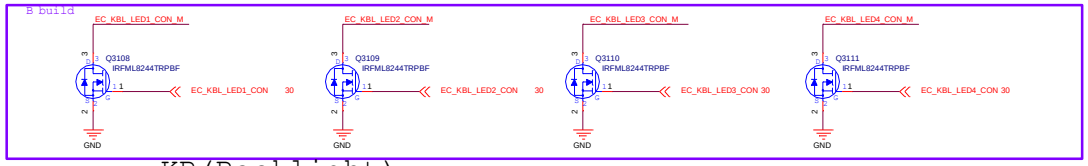
SPI ROM (Quad I/O Supported)



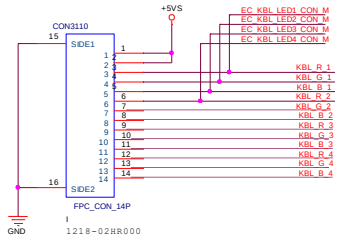
NOTE:
Making use of WP* and HOLD* for Quad I/O support

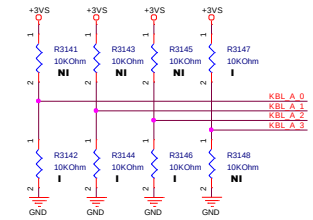
Keyboard Connector(debug)

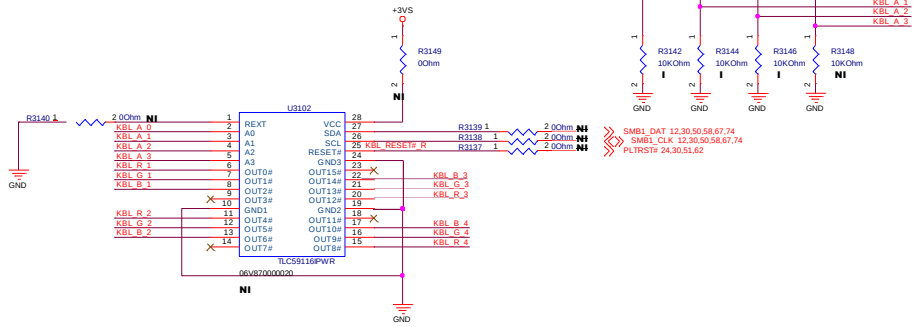




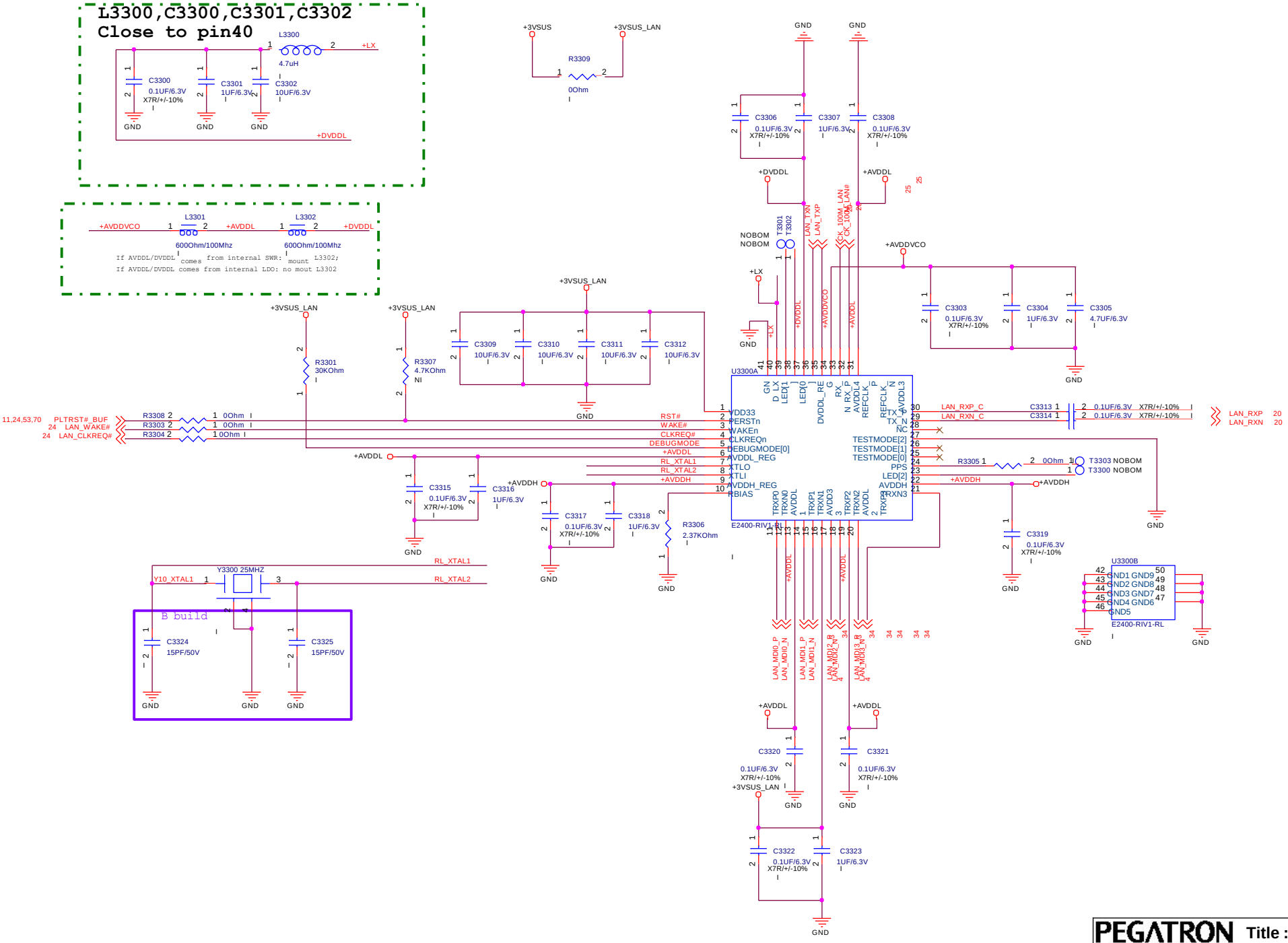
KB(Backlight)





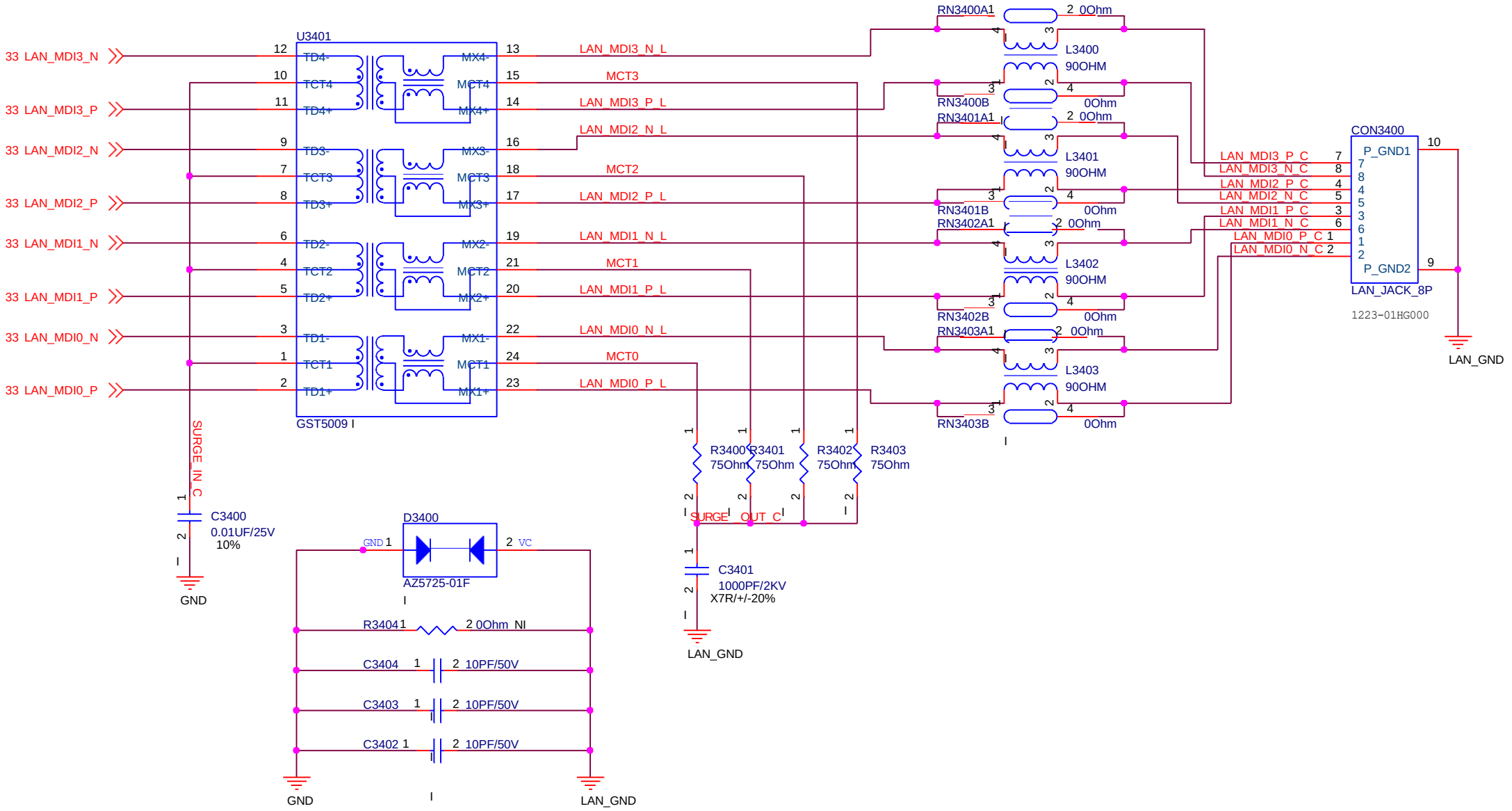


PEGATRON	Title : KB/TP//SPIII		
PegatronCorp.	Engineer: Leon_Lu		
Size A2	Project Name MU5DC/CH7DC MAIN		Rev A1.0
Date: BOARD	September 07, 2015	Sheet 31 of	108



PEGATRON	Title : LAN_E2400		
Pegatron Corp.	Engineer: Leon_Lu		
Size: A3	Project Name: MU5DC/CH7DC MAIN BOARD		Rev: A1.0
Date: Monday, September 07, 2015	Sheet 33 of 108		

SURGE

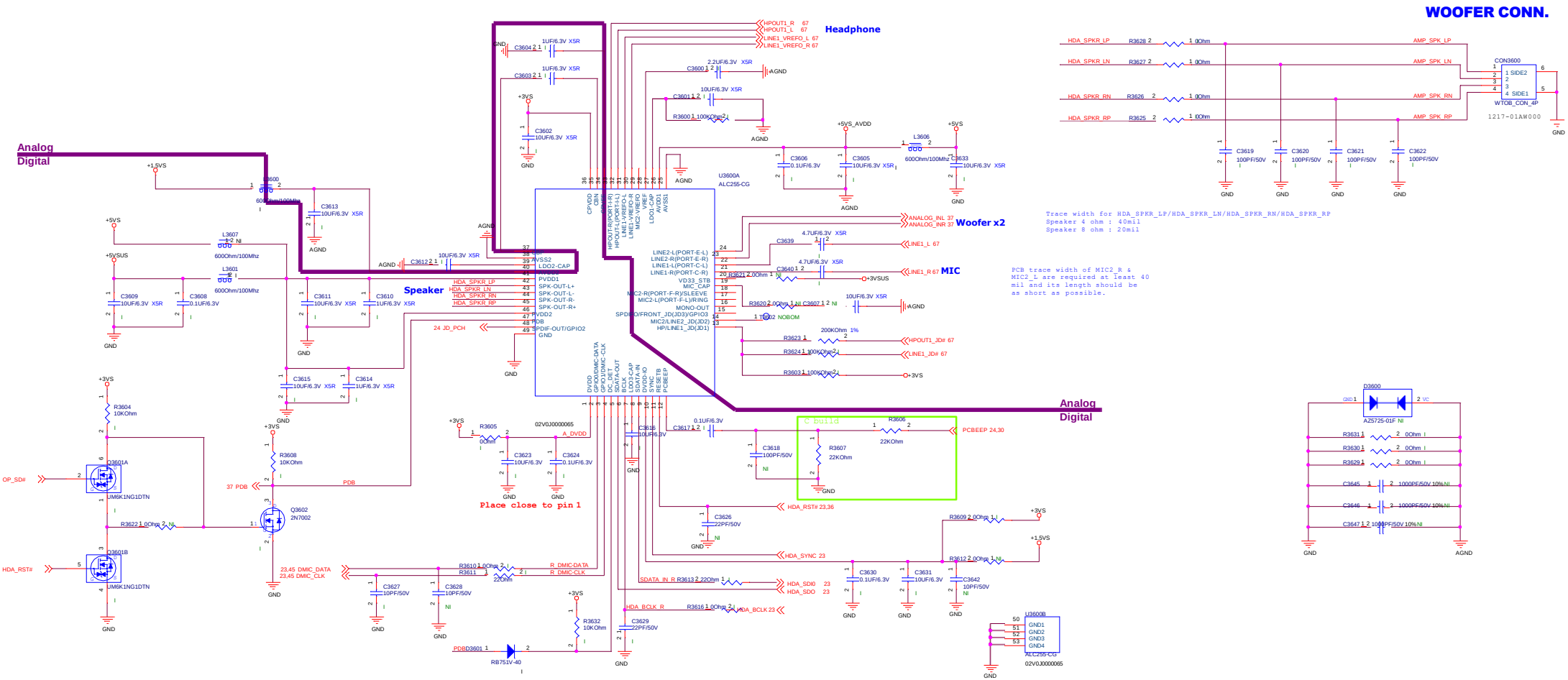


PEGATRON DT-MB RESTRICTED SECRET

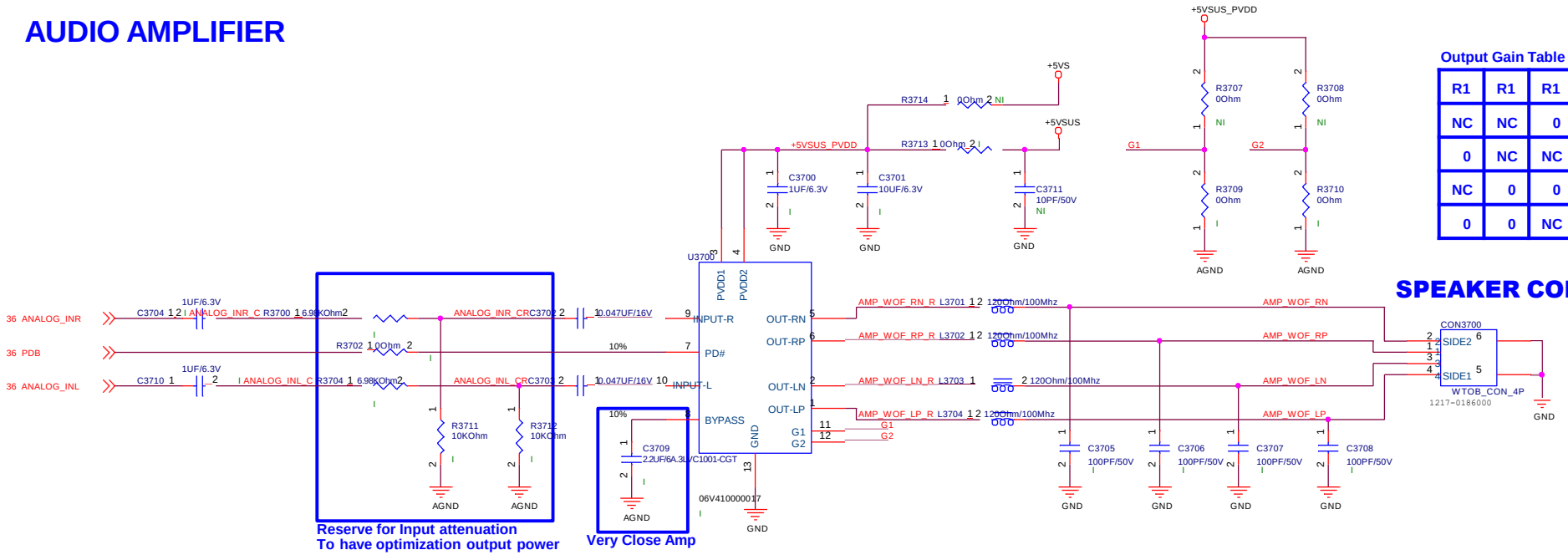
<Variant Name>

PEGATRON	Title : RJ45 CONN.	
Pegatron Corp.	Engineer: Leon_Lu	
Size: A4	Project Name: MU5DC/CH7DC MAIN BOARD	Rev: A1.0
Date: Monday, September 07, 2015	Sheet 34 of 108	

ALC255 CODEC



AUDIO AMPLIFIER



SPEAKER CONN.

Output Gain Table

R1	R1	R1	R1	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

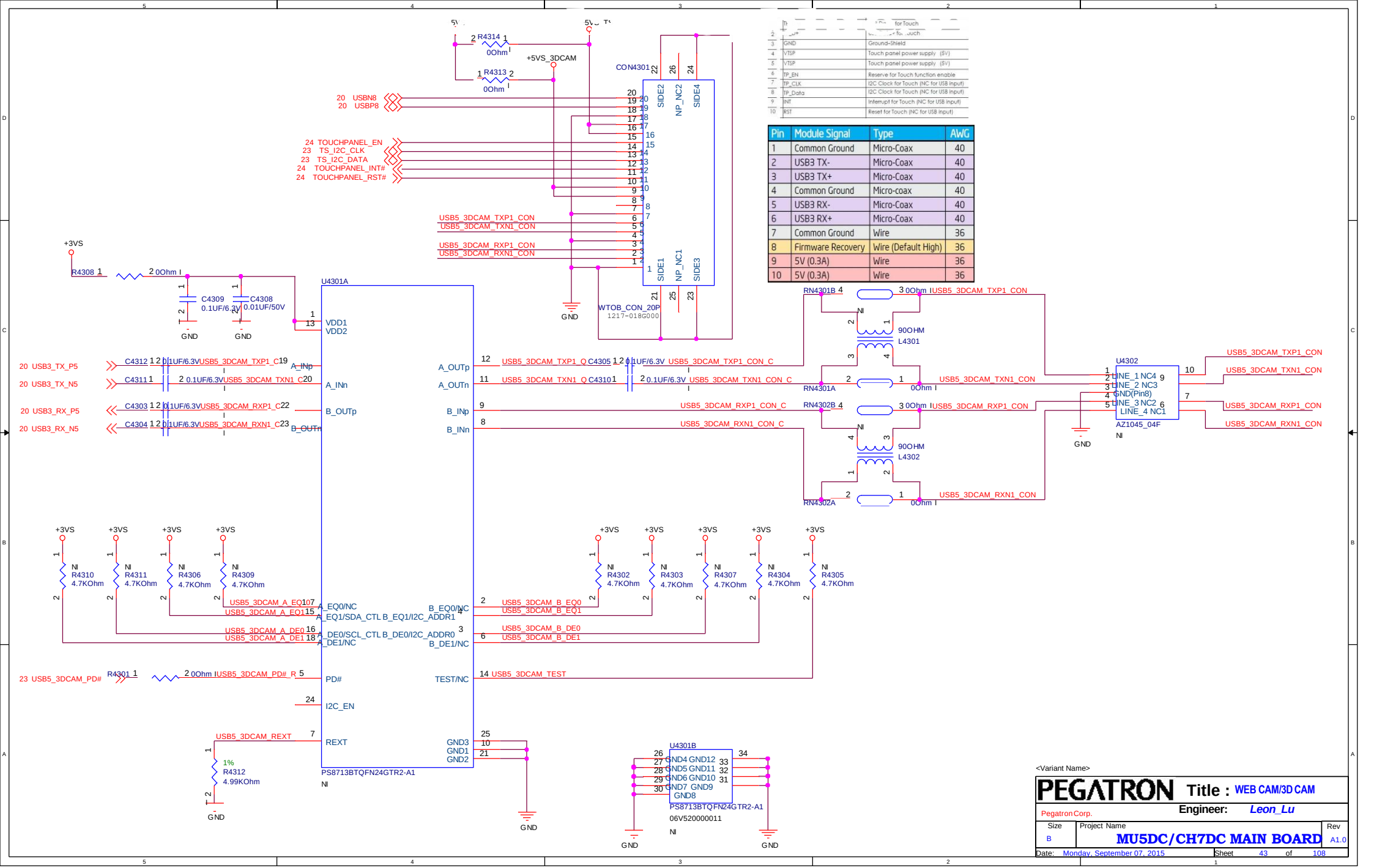
<Variiant Name>

PEGATRON Title : SPEAKER & SIDE MIC1

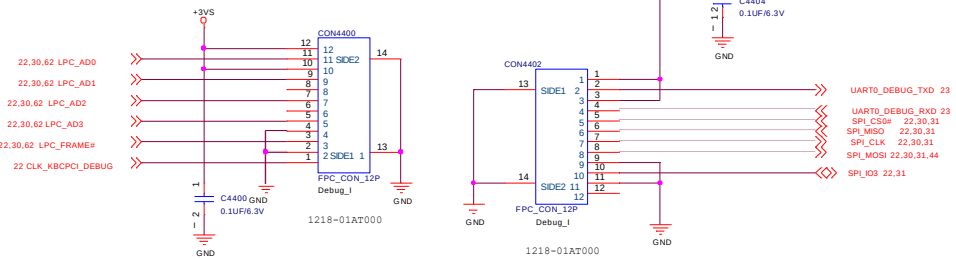
Pegatron Corp. Engineer: Leon_Lu

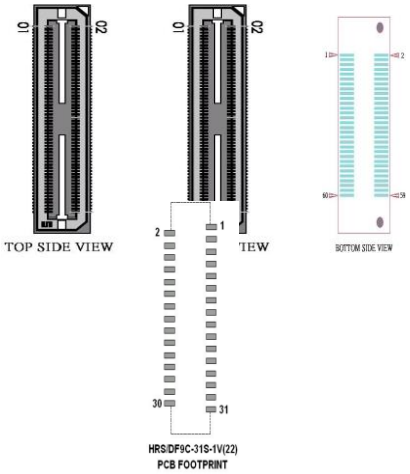
Size	Project Name	Rev
A3	MU5DC/CH7DC MAIN BOARD	A1.0

Date: Monday, Sep... 15 Sheet 37 of 108

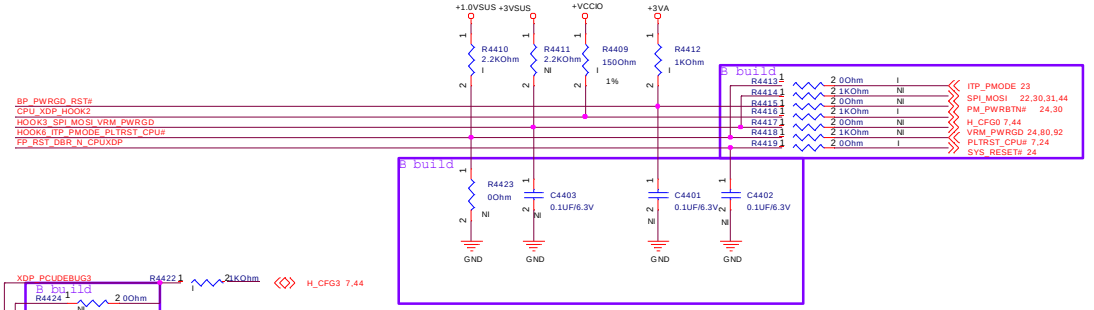

for Touch
GND Ground-Shield
VTSP Touch panel power supply (5V)
VTSP Touch panel power supply (5V)
TP_EN Reserve for Touch function enable
TP_CLK I2C Clock for Touch (NC for USB input)
TP_Data I2C Clock for Touch (NC for USB input)
INT Interrupt for Touch (NC for USB input)
RST Reset for Touch (NC for USB input)
Pin | Module Signal | Type | AWG
1 | Common Ground | Micro-Coax | 40
2 | USB3 TX- | Micro-Coax | 40
3 | USB3 TX+ | Micro-Coax | 40
4 | Common Ground | Micro-coax | 40
5 | USB3 RX- | Micro-Coax | 40
6 | USB3 RX+ | Micro-Coax | 40
7 | Common Ground | Wire | 36
8 | Firmware Recovery | Wire (Default High) | 36
9 | 5V (0.3A) | Wire | 36
10 | 5V (0.3A) | Wire | 36
CON4301
WTOB_CON_20P
1217-018G000
U4301A
PS8713BTQFN24GTR2-A1
U4301B
PS8713BTQFN24GTR2-A1
06V520000011
U4302
AZ1045_04F
RN4301A
RN4301B
RN4302A
RN4302B
L4301
L4302
<Variant Name>
PEGATRON
Title : WEB CAM/3D CAM
Pegatron Corp.
Engineer: Leon_Lu
Size B
Project Name MU5DC/CH7DC MAIN BOARD
Rev A1.0
Date: Monday, September 07, 2015
Sheet 43 of 108

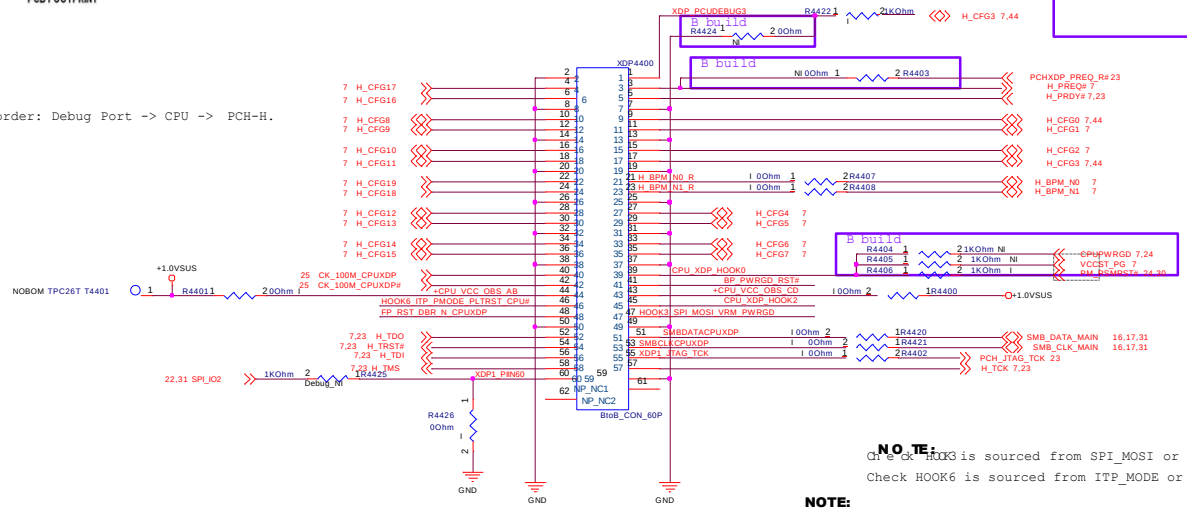
LPC DEBUG SMD





INTEL CPU XDP DEBUG PORT





NOTE: PREQ# and PRDY#
MUST be routed in this order: Debug Port -> CPU -> PCH-H.

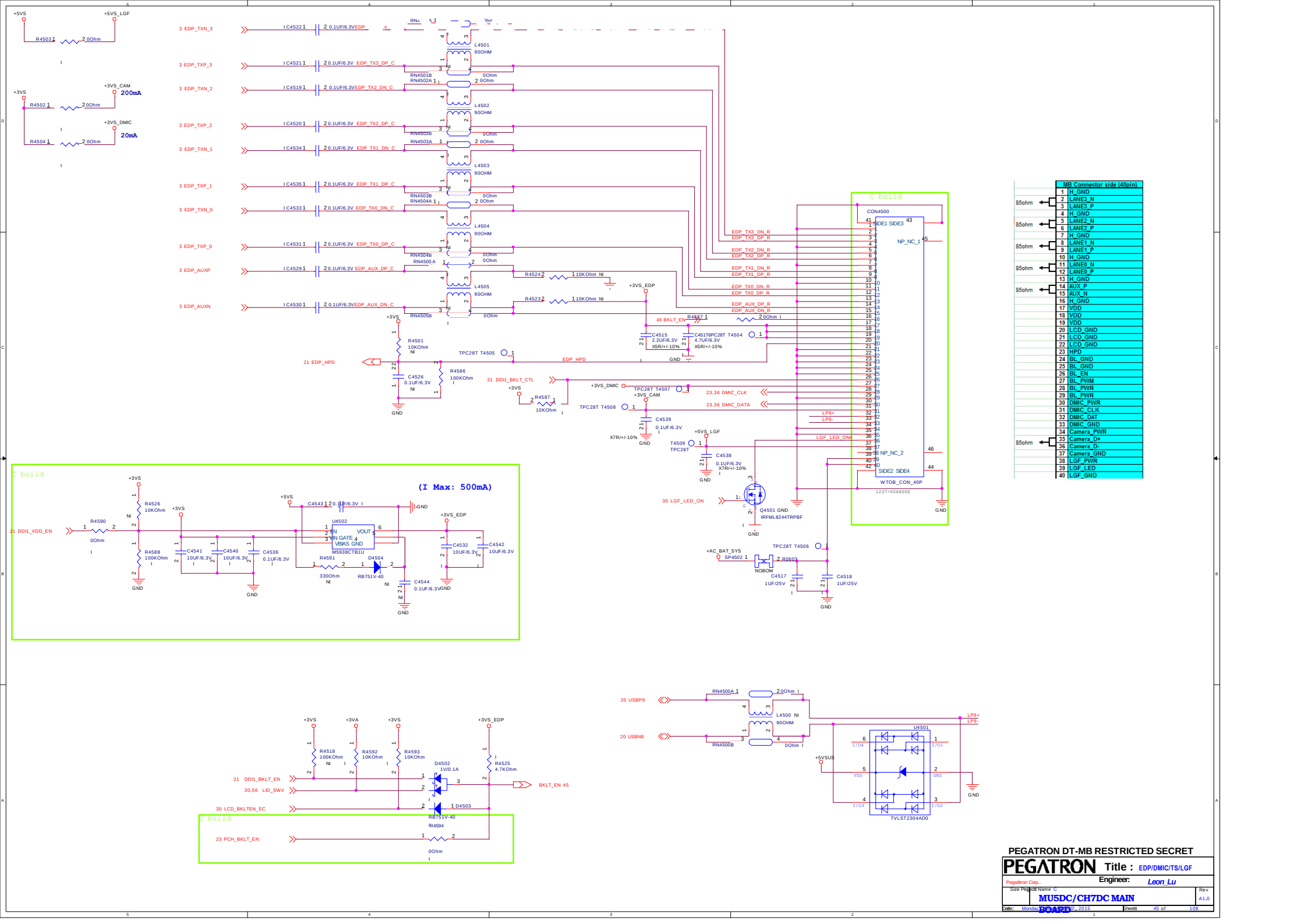
NOTE:
Check HOOK3 is sourced from SPI_MOSI or VRM_PWRGD?
Check HOOK6 is sourced from ITP_MODE or PLTRST_CPU#?

NOTE:
XDP_PRESENT#(PIN 60) to enable +1V_ST for Sx debug purpose

NOTE:
Place SPI_IO2 0 ohm near PCH

<Variant Name>

PEGATRON Title : DEBUG CON
Pegatron Corp. Engineer: Leon_Lu
Size: C | Project Name: MU5DC/CH7DC MAIN | Rev: A1.0
Date: Thursday, October 10, 2015 | Sheet: 44 of 108
BOARD



	1	H_GND
85ohm	2	LANE3_N
	3	LANE3_P
	4	H_GND
85ohm	5	LANE2_N
	6	LANE2_P
	7	H_GND
85ohm	8	LANE1_N
	9	LANE1_P
	10	H_GND
85ohm	11	LANE0_N
	12	LANE0_P
	13	H_GND
85ohm	14	AUX_P
	15	AUX_N
	16	H_GND
	17	VDD
	18	VDD
	19	VDD
	20	LCD_GND
	21	LCD_GND
	22	LCD_GND
	23	HPD
	24	BL_GND
	25	BL_GND
	26	BL_EN
	27	BL_PWM
	28	BL_PWR
	29	BL_PWR
	30	DMIC_PWR
	31	DMIC_CLK
	32	DMIC_DAT
	33	DMIC_GND
	34	Camera_PWR
85ohm	35	Camera_D+
	36	Camera_D-
	37	Camera_GND
	38	LGF_PWR
	39	LGF_LED
	40	LGF_GND

PEGATRON DT-MB RESTRICTED SECRET

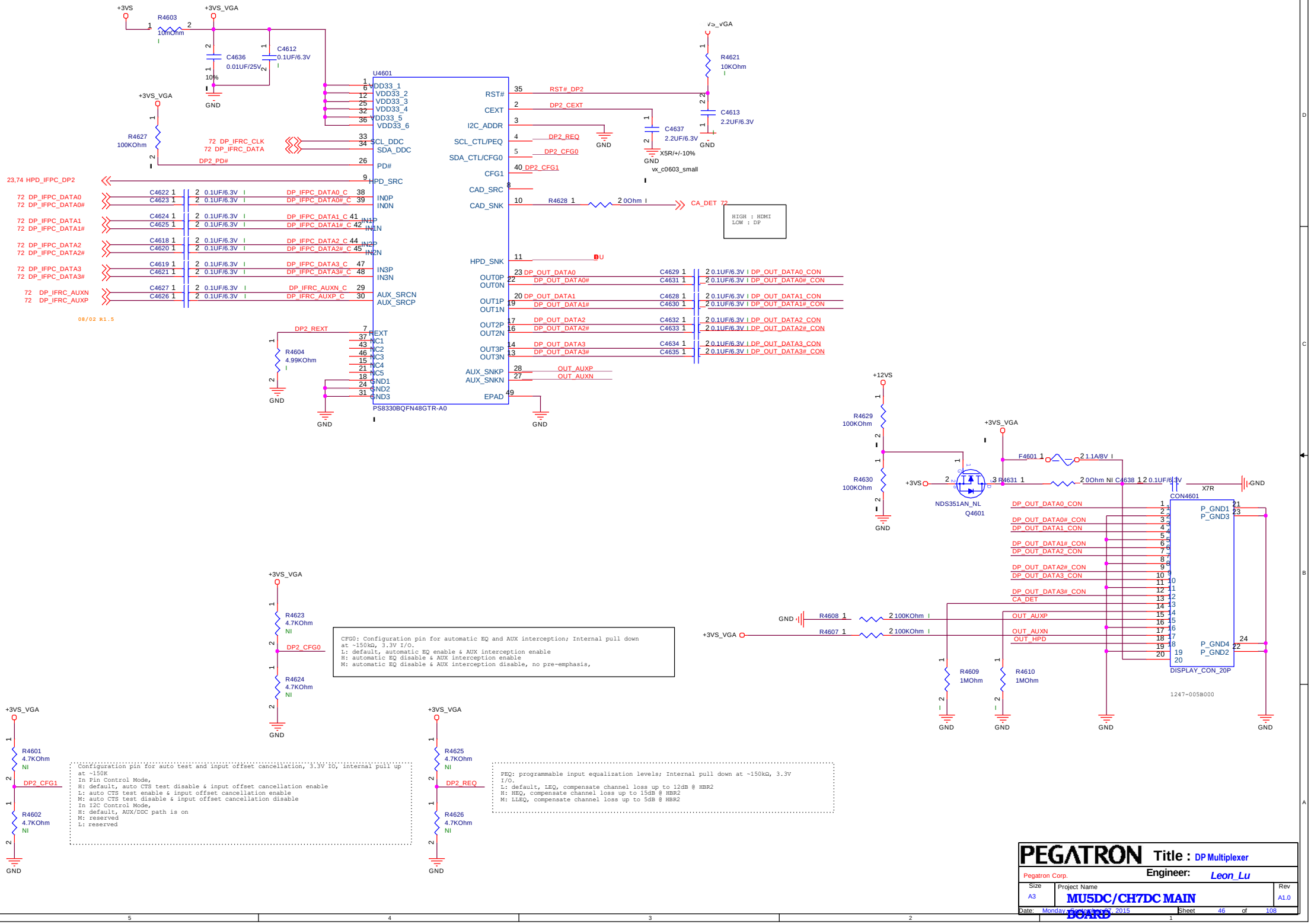
PEGATRON Title : EDP/DMIC/TS/LGF

Pegatitron Corp.. Engineer: Leon_Lu

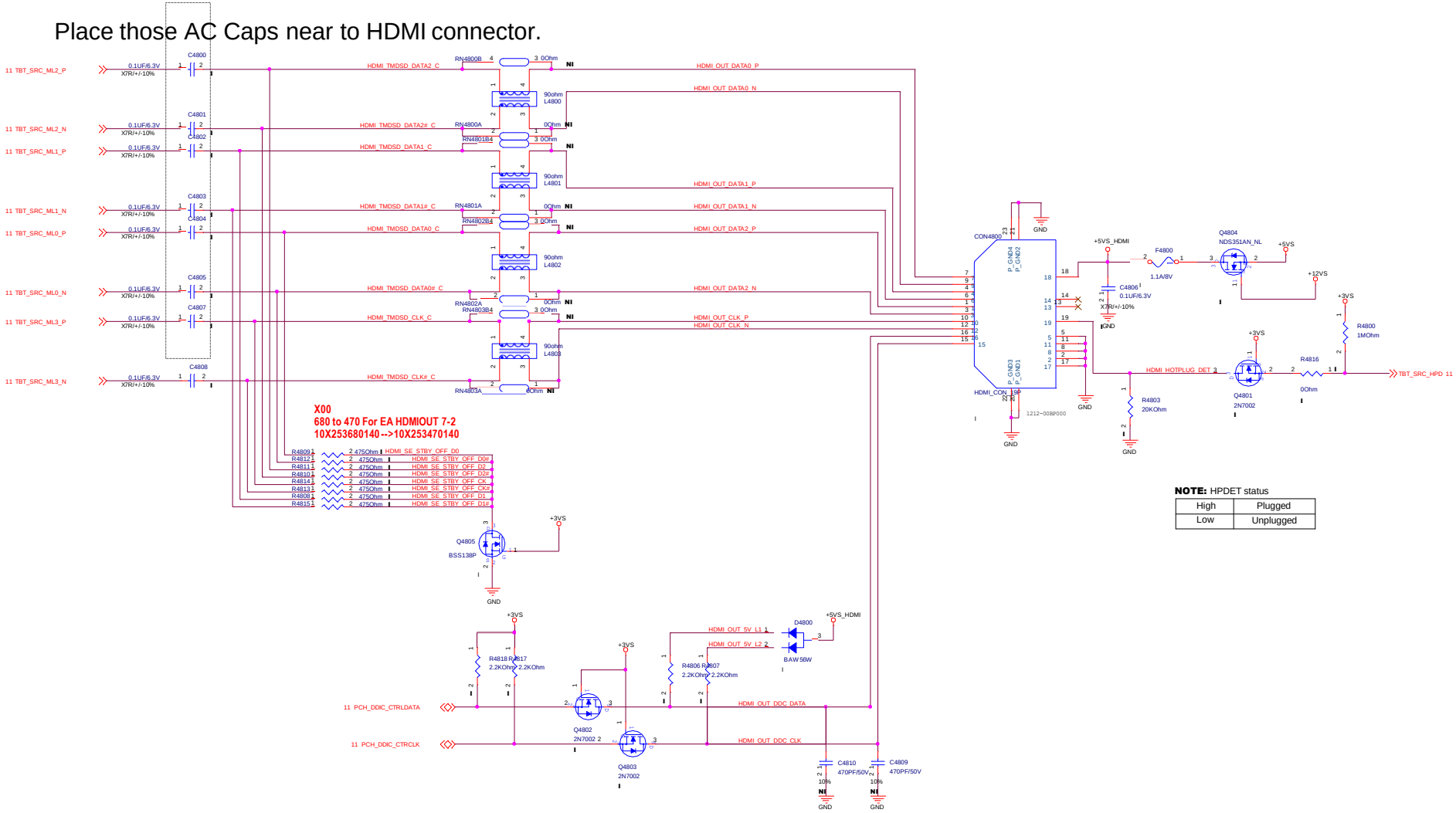
Size: Project Name: C MU5DC/CH7DC MAIN Rev: A1.0

Date: Monday, [illegible] 07, 2015 Sheet: 45 of 108

BOARD

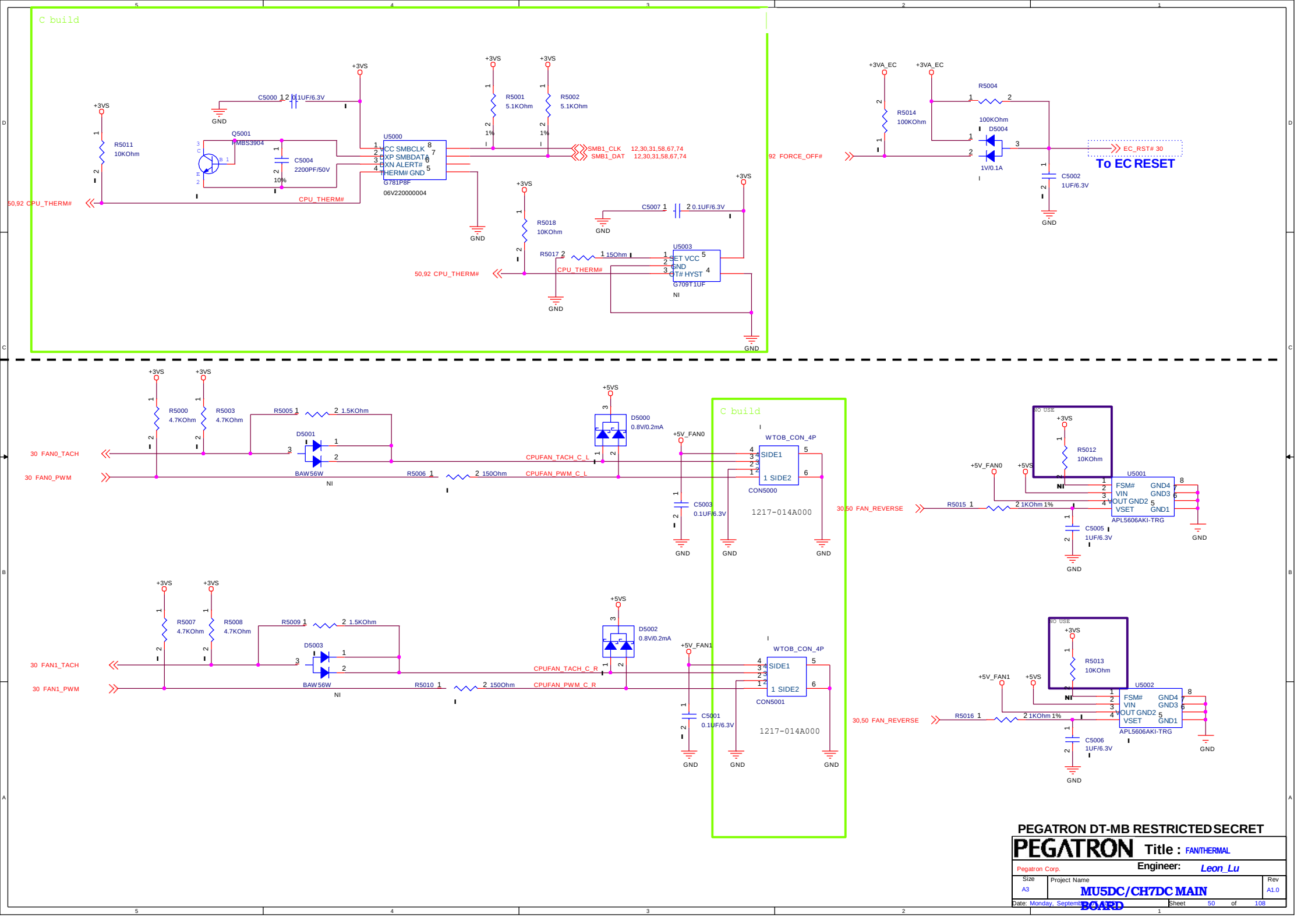

+3VS
+3VS_VGA
R4603
10mOhm
C4636
0.01UF/25V
10%
C4612
0.1UF/6.3V
GND
U4601
VDD33_1
VDD33_2
VDD33_3
VDD33_4
VDD33_5
VDD33_6
R4627
100KOhm
72 DP_IFRC_CLK
72 DP_IFRC_DATA
DP2_PD#
SCL_DDC
SDA_DDC
PD#
23,74 HPD_IFPC_DP2
HPD_SRC
72 DP_IFPC_DATA0
72 DP_IFPC_DATA0#
72 DP_IFPC_DATA1
72 DP_IFPC_DATA1#
72 DP_IFPC_DATA2
72 DP_IFPC_DATA2#
72 DP_IFPC_DATA3
72 DP_IFPC_DATA3#
72 DP_IFRC_AUXN
72 DP_IFRC_AUXP
IN0P
IN0N
IN1P
IN1N
IN2P
IN2N
IN3P
IN3N
AUX_SRCN
AUX_SRCP
08/02 R1.5
DP2_REXT
R4604
4.99KOhm
REXT
NC1
NC2
NC3
NC4
NC5
GND1
GND2
GND3
PS8330BQFN48GTR-A0
RST#
CEXT
I2C_ADDR
SCL_CTL/PEQ
SDA_CTL/CFG0
CFG1
CAD_SRC
CAD_SNK
HPD_SNK
OUT0P
OUT0N
OUT1P
OUT1N
OUT2P
OUT2N
OUT3P
OUT3N
AUX_SNKP
AUX_SNKN
EPAD
RST#_DP2
DP2_CEXT
DP2_REQ
DP2_CFG0
DP2_CFG1
R4628
0Ohm
CA_DET
HIGH : HDMI
LOW : DP
DP_OUT_DATA0
DP_OUT_DATA0#
DP_OUT_DATA1
DP_OUT_DATA1#
DP_OUT_DATA2
DP_OUT_DATA2#
DP_OUT_DATA3
DP_OUT_DATA3#
OUT_AUXP
OUT_AUXN
C4637
2.2UF/6.3V
X5R/+/-10%
vx_c0603_small
R4621
10KOhm
C4613
2.2UF/6.3V
+12VS
R4629
100KOhm
R4630
100KOhm
NDS351AN_NL
Q4601
F4601
1.1A/8V
R4631
0Ohm NI
C4638
0.1UF/6.3V
X7R
CON4601
DP_OUT_DATA0_CON
DP_OUT_DATA0#_CON
DP_OUT_DATA1_CON
DP_OUT_DATA1#_CON
DP_OUT_DATA2_CON
DP_OUT_DATA2#_CON
DP_OUT_DATA3_CON
DP_OUT_DATA3#_CON
CA_DET
OUT_AUXP
OUT_AUXN
OUT_HPD
P_GND1
P_GND3
P_GND4
P_GND2
DISPLAY_CON_20P
1247-005B000
R4608
100KOhm
R4607
100KOhm
R4609
1MOhm
R4610
1MOhm
R4623
4.7KOhm
NI
R4624
4.7KOhm
NI
CFG0: Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis,
R4601
4.7KOhm
NI
R4602
4.7KOhm
NI
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K
In Pin Control Mode,
H: default, auto CTS test disable & input offset cancellation enable
L: auto CTS test enable & input offset cancellation enable
M: auto CTS test disable & input offset cancellation disable
In I2C Control Mode,
H: default, AUX/DDC path is on
M: reserved
L: reserved
R4625
4.7KOhm
NI
R4626
4.7KOhm
NI
PEQ: programmable input equalization levels; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, LEQ, compensate channel loss up to 12dB @ HBR2
H: HEQ, compensate channel loss up to 15dB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2
PEGATRON
Title : DP Multiplexer
Pegatron Corp.
Engineer: Leon_Lu
Size A3
Project Name MU5DC/CH7DC MAIN
Rev A1.0
Date: Monday, September 07, 2015
Sheet 46 of 108
BOARD

Place those AC Caps near to HDMI connector.



NOTE: HPDET status

High	Plugged
Low	Unplugged



PEGATRON DT-MB RESTRICTED SECRET

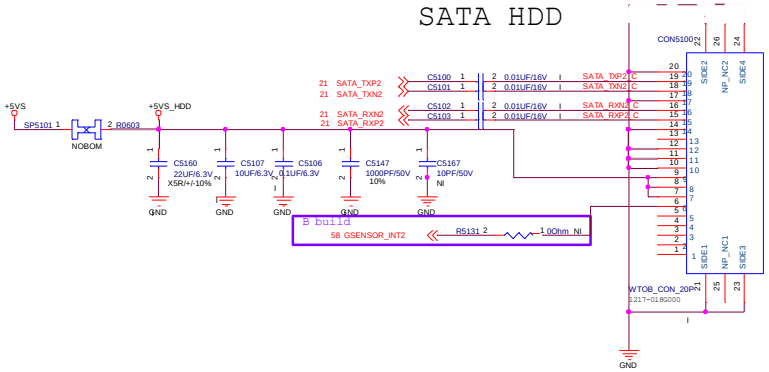
PEGATRON Title : FAN/THERMAL

Pegatron Corp. Engineer: Leon_Lu

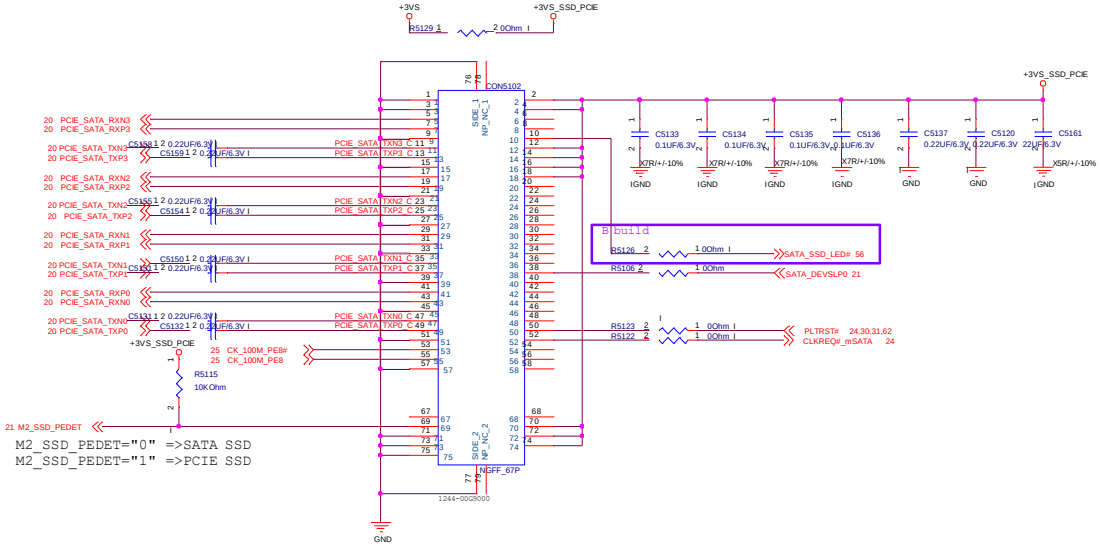
Size	Project Name	Rev
A3	MU5DC/CH7DC MAIN BOARD	A1.0

Date: Monday, September 09, 2013 Sheet 50 of 108

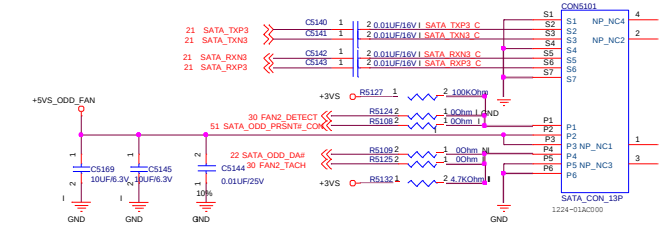
SATA HDD

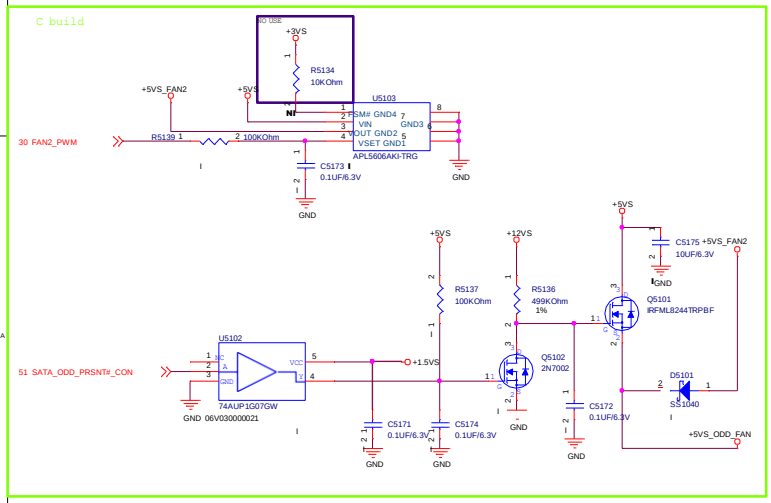


PCIE & SATA SSD

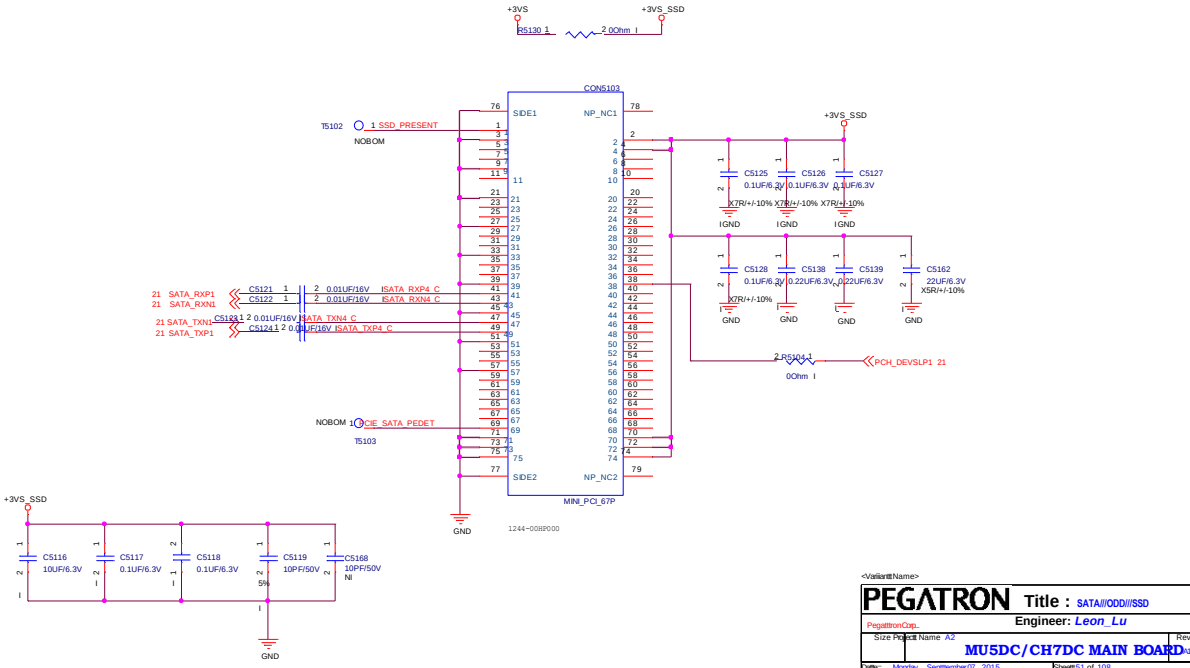


SATA ODD & 3'TH FAN





SATA SSD



STATUS#, FAULT#, ILIM_LO, ILIM_HI Voltage: -0.3 to 7v.
STATUS#, FAULT# Continuous output sink current:25mA.
ILIM_LO, ILIM_HI Continuous output source current: Internally limited.

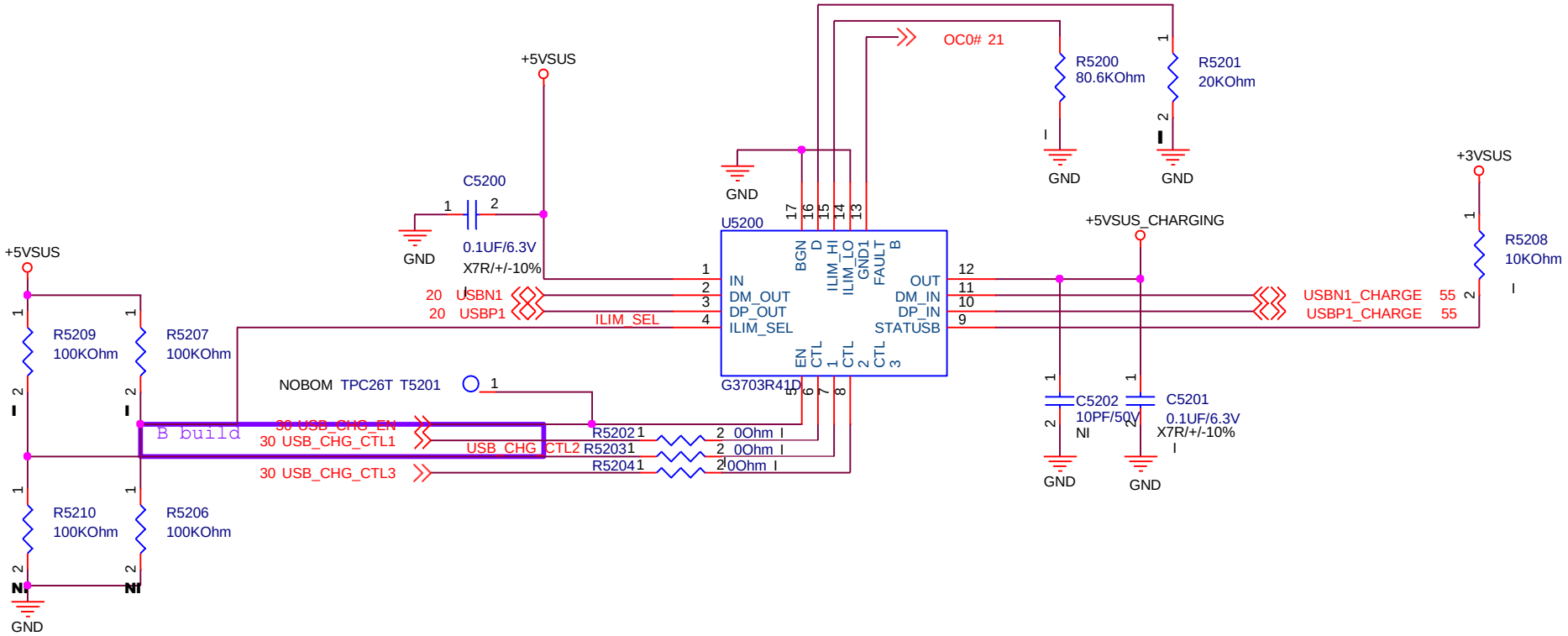


Table 2. Truth Table

CTL1	CTL2	CTL3	ILIM_ SEL	MODE	Current Limit Setting	Status Output	Notice
0	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	
0	1	1	0	DCP_Auto	ILIM_LO	OFF	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active

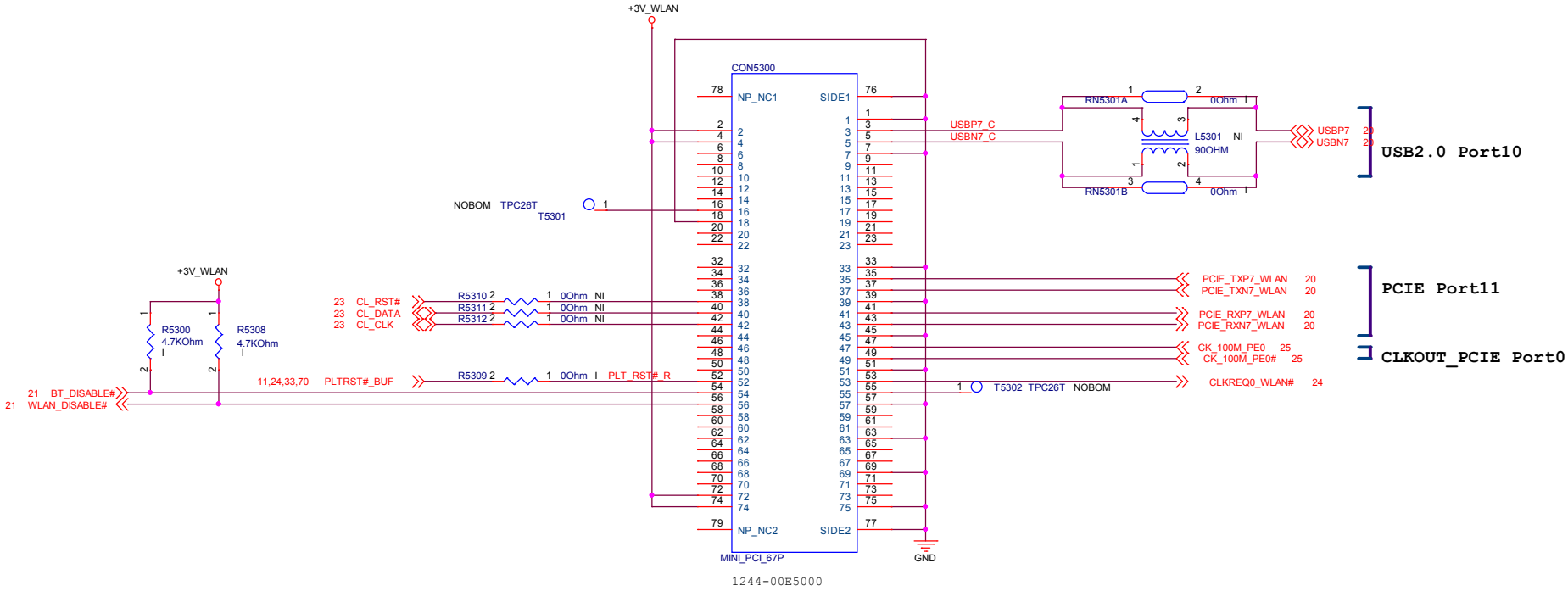
PEGATRON Title : USB CHARGE IC

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A4	MU5DC/CH7DC MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 52 of 108

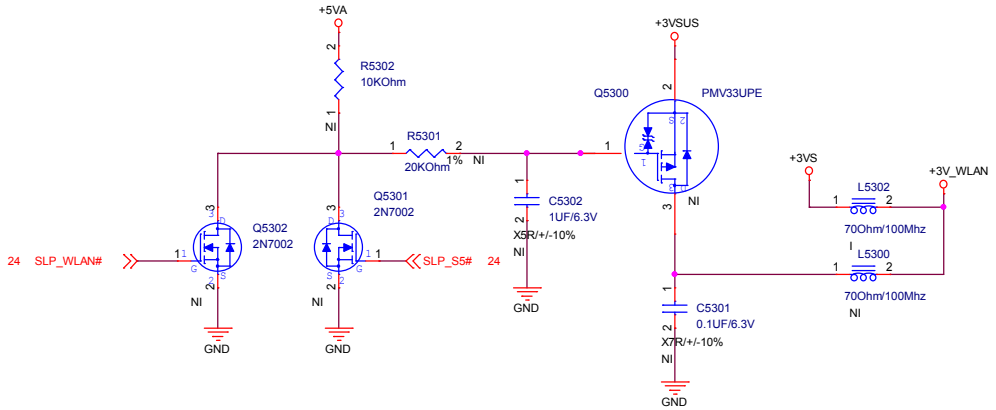
WLAN

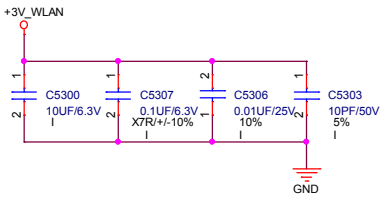


1244-00E5000

+3P3V_MINI1
Imax=2A /TDC=1.4A

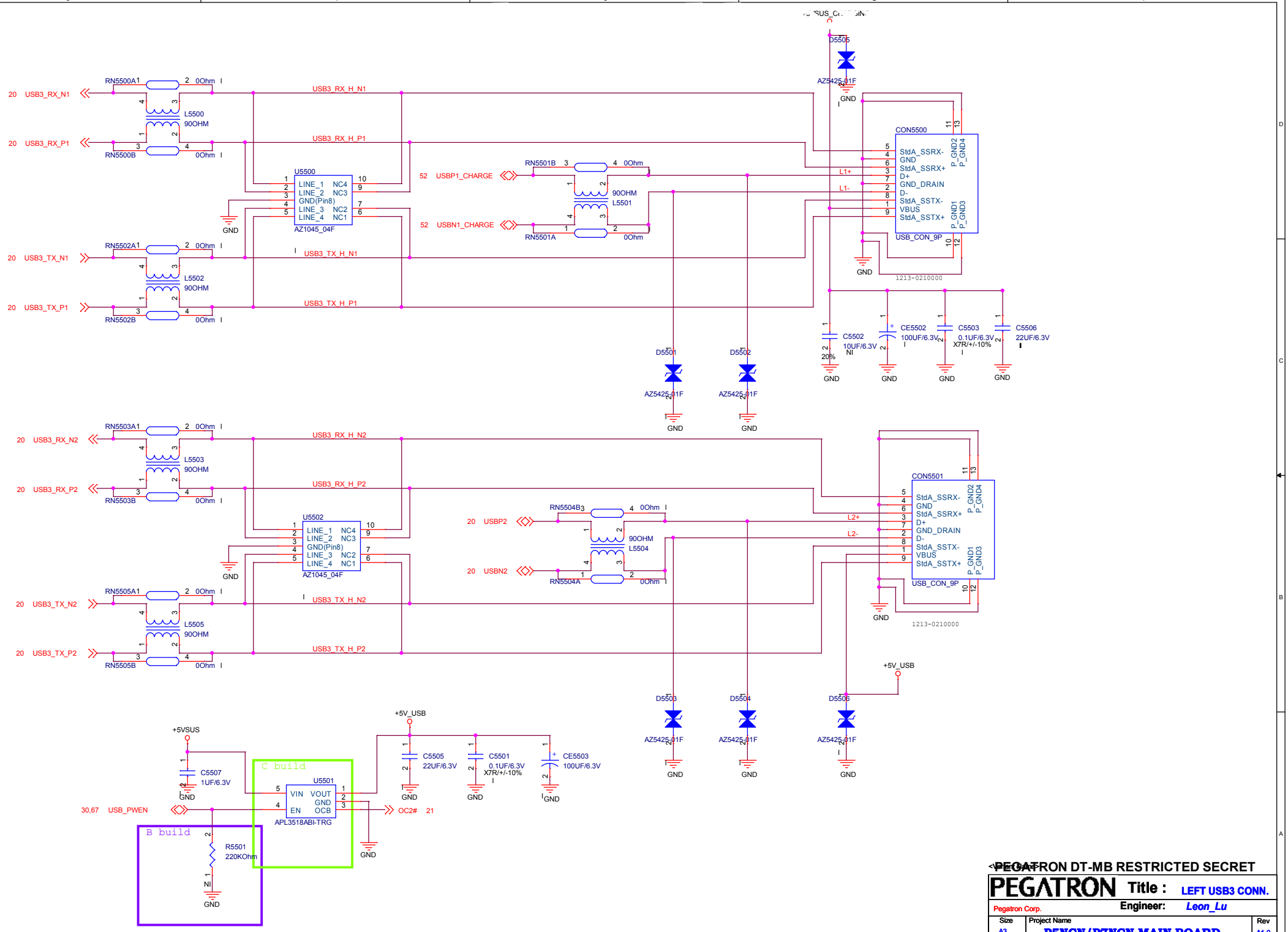
Vdroop: 1.4A*65mohm=91mV >3.3*0.95





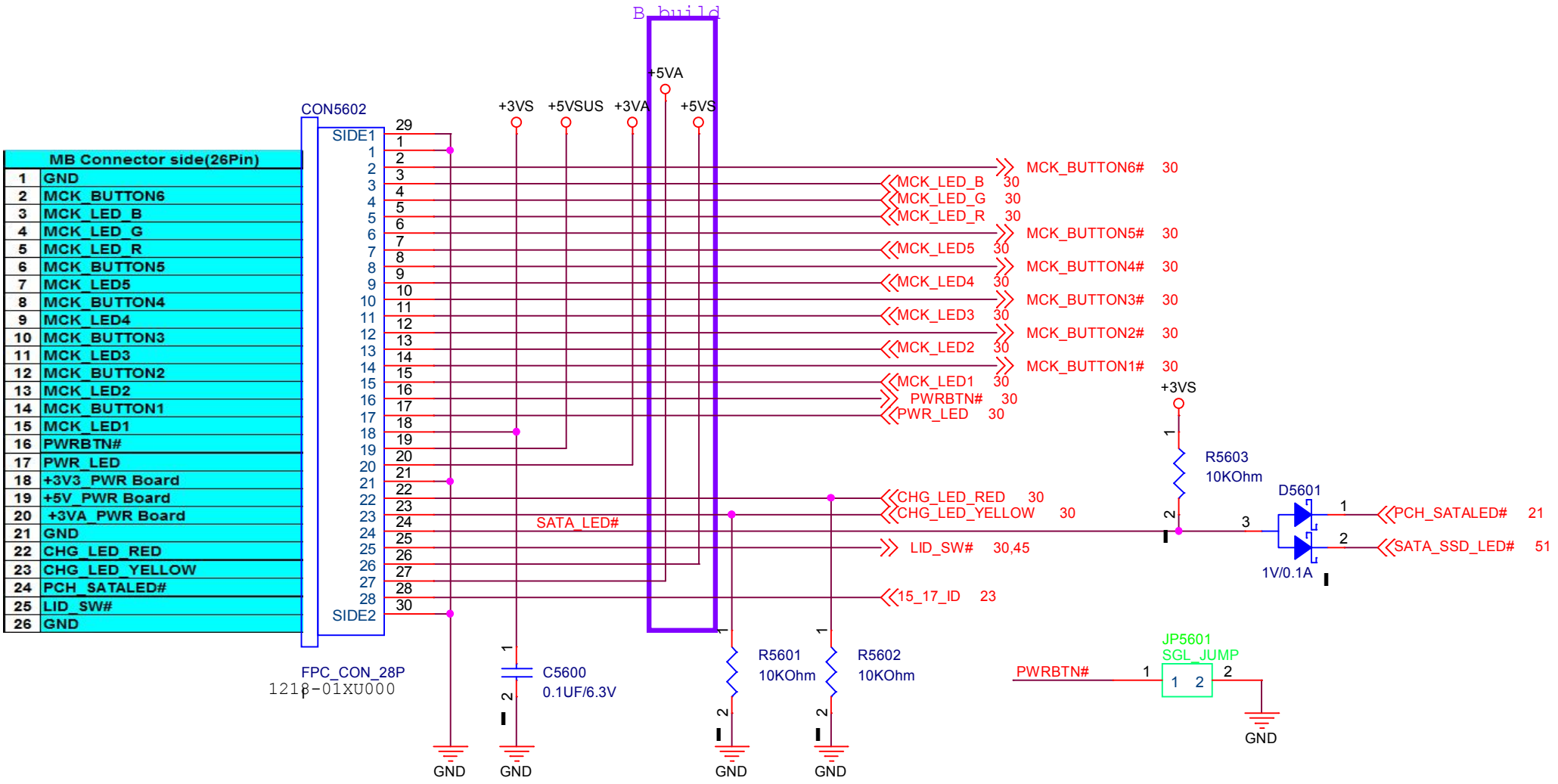
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : NGFF_WLAN	
Pegatron Corp.	Engineer: Leon_Lu	
Size: A3	Project Name: P5NCN/P7NCN MAIN BOARD	Rev: A1.0
Date: Monday, September 07, 2015	Sheet 53 of 108	



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title :	LEFT USB3 CONN.
Pegatron Corp.	Engineer:	Leon_Lu
Size: A3	Project Name: P5NCN/P7NCN MAIN BOARD	Rev: A1.0
Date: Monday, September 07, 2015	Sheet 55 of 108	



<Variant Name>

PEGATRON

Title : PWR BOARD CON

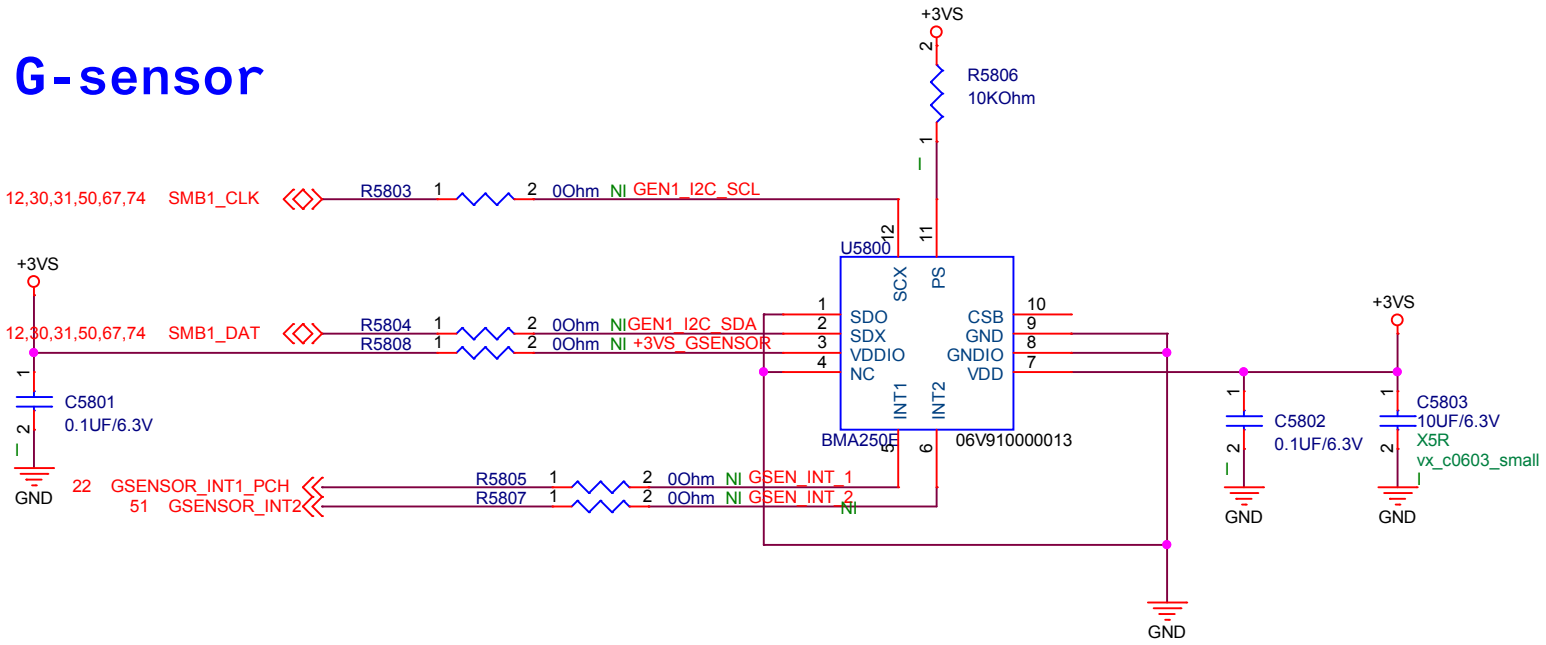
Pegatron Corp.

Engineer: Leon_Lu

Size	Project Name	Rev
A	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 56 of 108

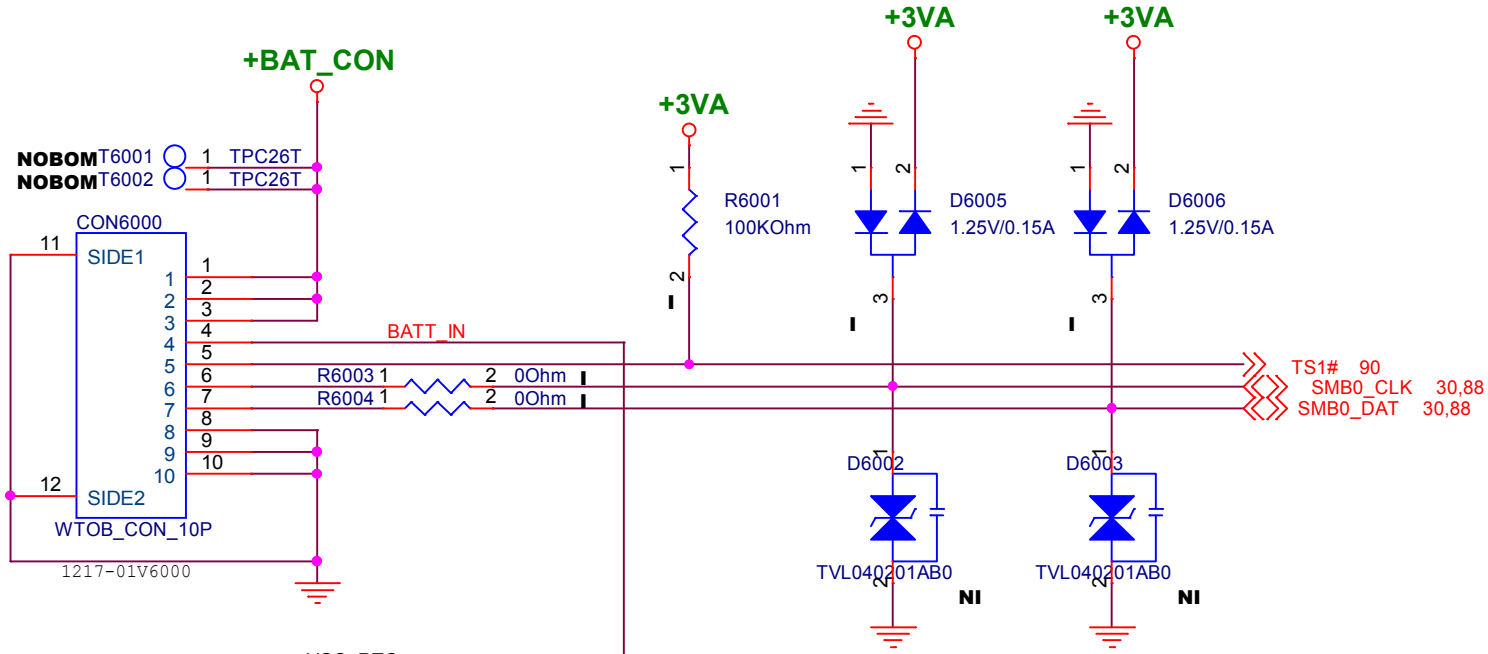
G-sensor

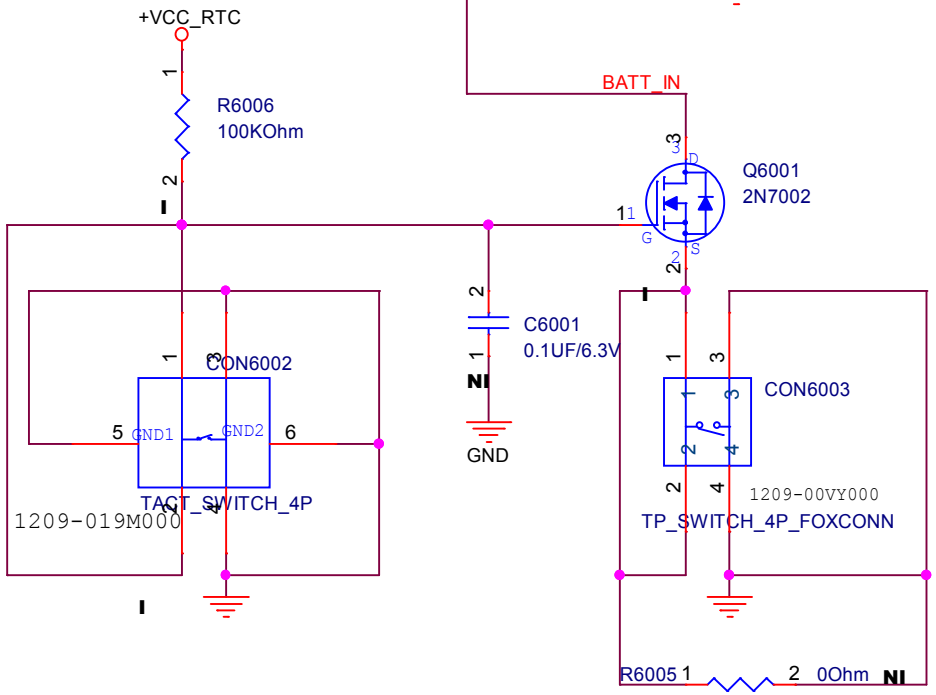


<Variant Name>

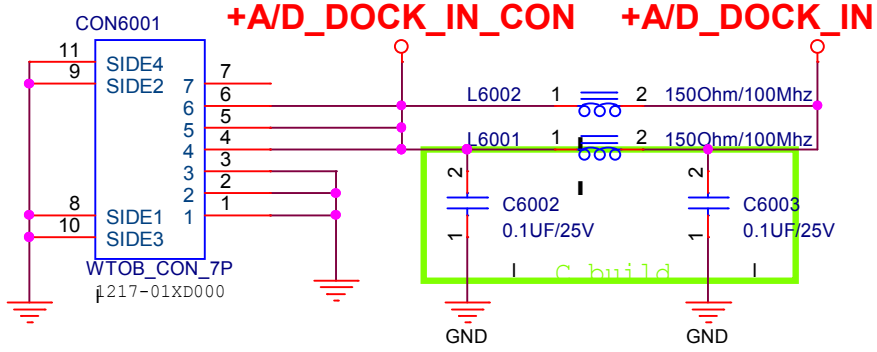
PEGATRON	Title : G-sensor	
Pegatron Corp.	Engineer: Leon_Lu	
Size: A4	Project Name: P5NCN/P7NCN MAIN BOARD	Rev: A1.0
Date: Monday, September 07, 2015	Sheet 58 of 108	

BATTERY CONNECTOR

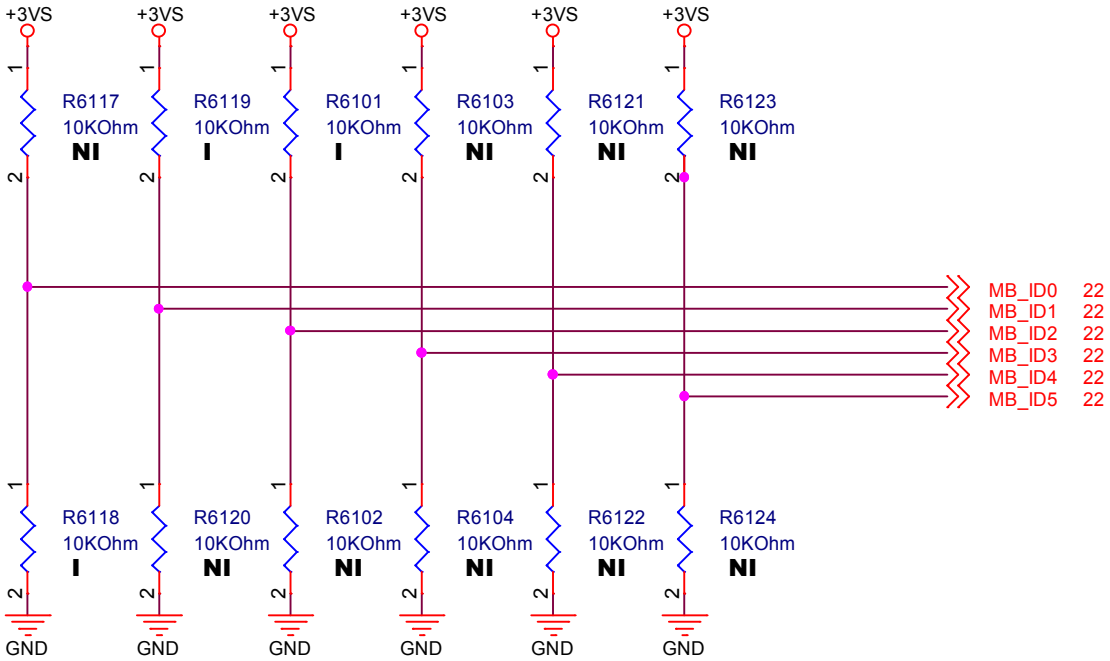


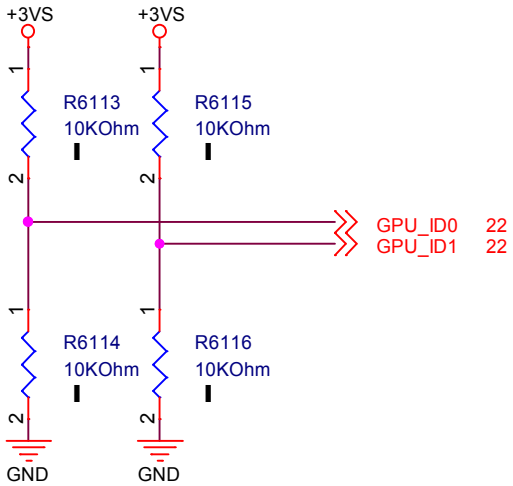


AC IN CONNECTOR



PEGATRON	Title :	BATT CON/AC IN
Pegatron Corp.	Engineer:	Leon_Lu
Size: A	Project Name: P5NCN/P7NCN MAIN BOARD	Rev: A1.0
Date: Monday, September 07, 2015	Sheet 60 of 108	





	ID2	ID1	ID0
1.0	0	0	0
1.1	0	0	1
1.2	0	0	1
1.3	0	1	0
1.4	0	1	1
1.5/1.6	1	0	0
1.5/1.6 C8	1	0	1
2	1	1	0

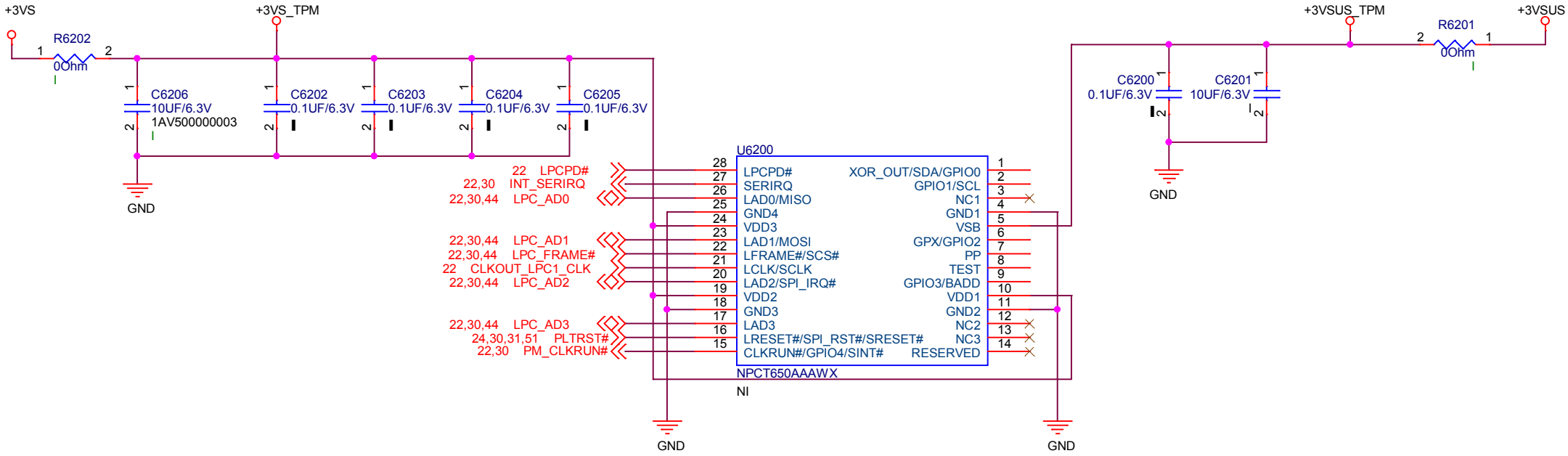
PEGATRON Title : BOARD ID

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 61 of 108

NPCT650



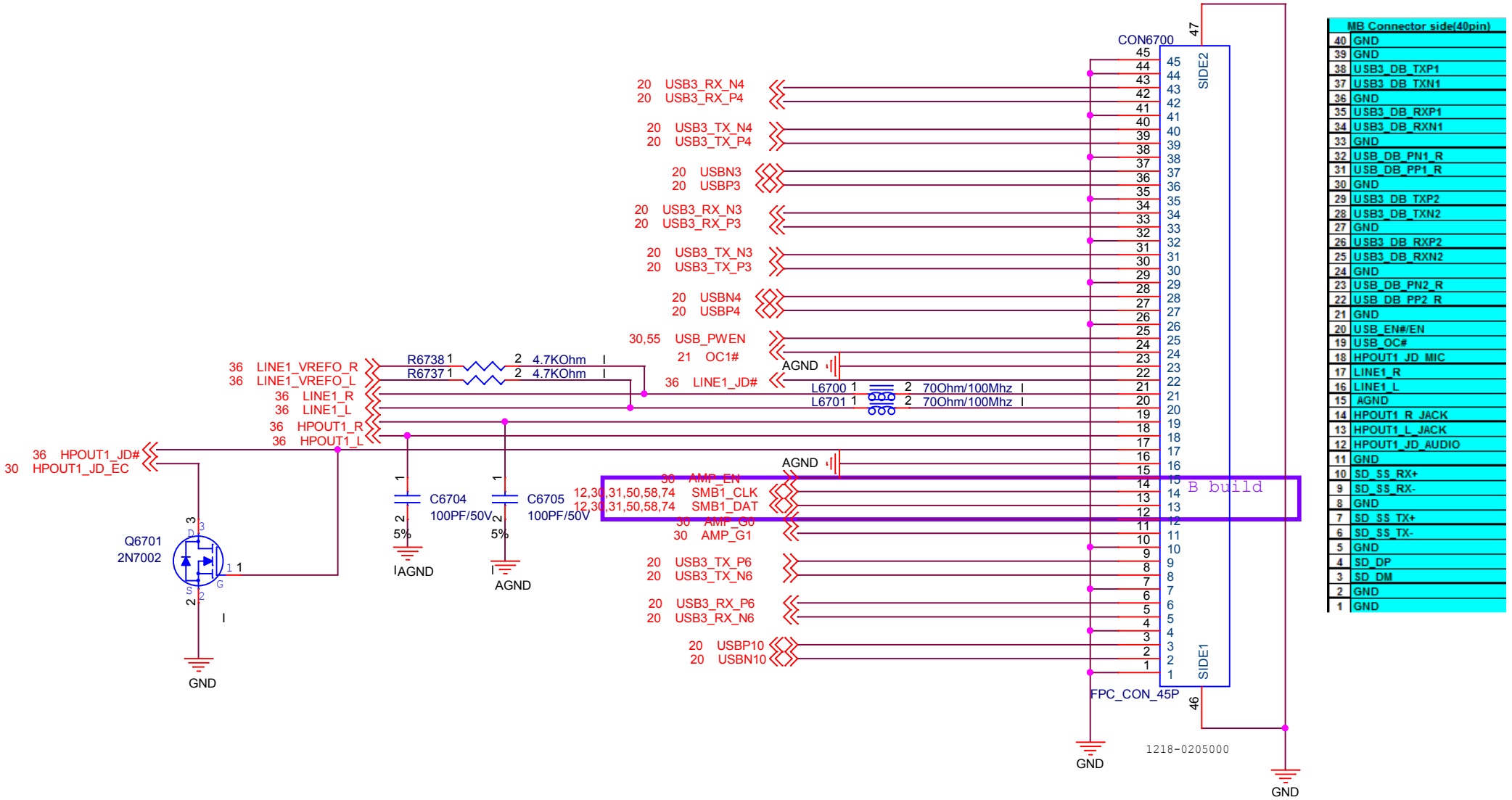
<Variant Name>

PEGATRON Title : TPM

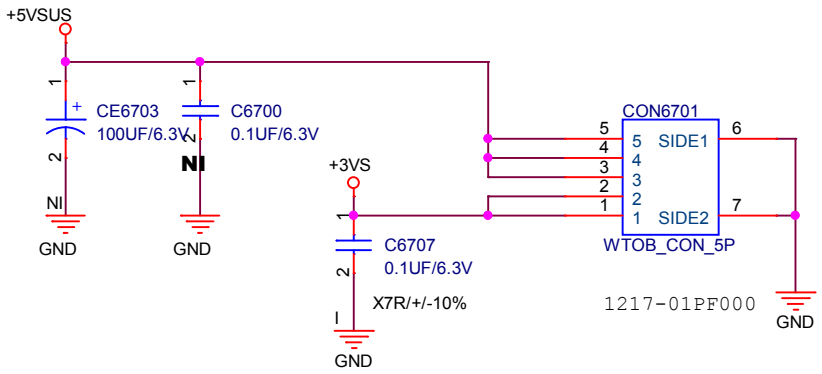
Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A4	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 62 of 108



MB Connector side(40pin)	
40	GND
39	GND
38	USB3_DB_TXP1
37	USB3_DB_TXN1
36	GND
35	USB3_DB_RXP1
34	USB3_DB_RXN1
33	GND
32	USB_DB_PN1_R
31	USB_DB_PP1_R
30	GND
29	USB3_DB_TXP2
28	USB3_DB_TXN2
27	GND
26	USB3_DB_RXP2
25	USB3_DB_RXN2
24	GND
23	USB_DB_PN2_R
22	USB_DB_PP2_R
21	GND
20	USB_EN#/EN
19	USB_OC#
18	HPOUT1_JD_MIC
17	LINE1_R
16	LINE1_L
15	AGND
14	HPOUT1_R_JACK
13	HPOUT1_L_JACK
12	HPOUT1_JD_AUDIO
11	GND
10	SD_SS_RX+
9	SD_SS_RX-
8	GND
7	SD_SS_TX+
6	SD_SS_TX-
5	GND
4	SD_DP
3	SD_DM
2	GND
1	GND



MB Connector side(5pin)	
1	+3VS_DB
2	+3VS_DB
3	+5V_POWER
4	+5V_POWER
5	+5V_POWER

PEGATRON DT-MB RESTRICTED SECRET

Variant Name:

PEGATRON Title : IO BOARD CON

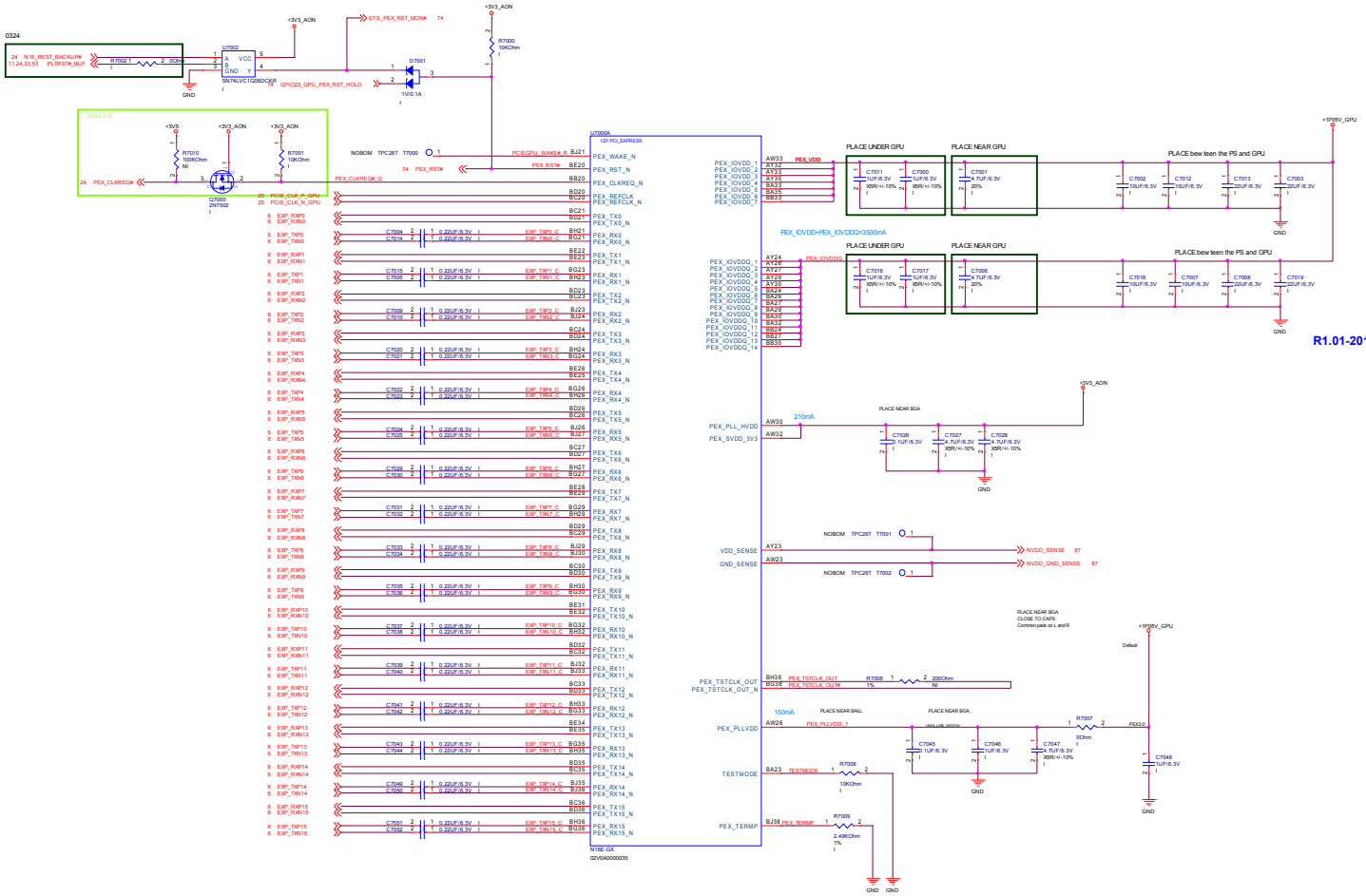
Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A4	P5NCN/P7NCN MAIN BOARD	A1.0

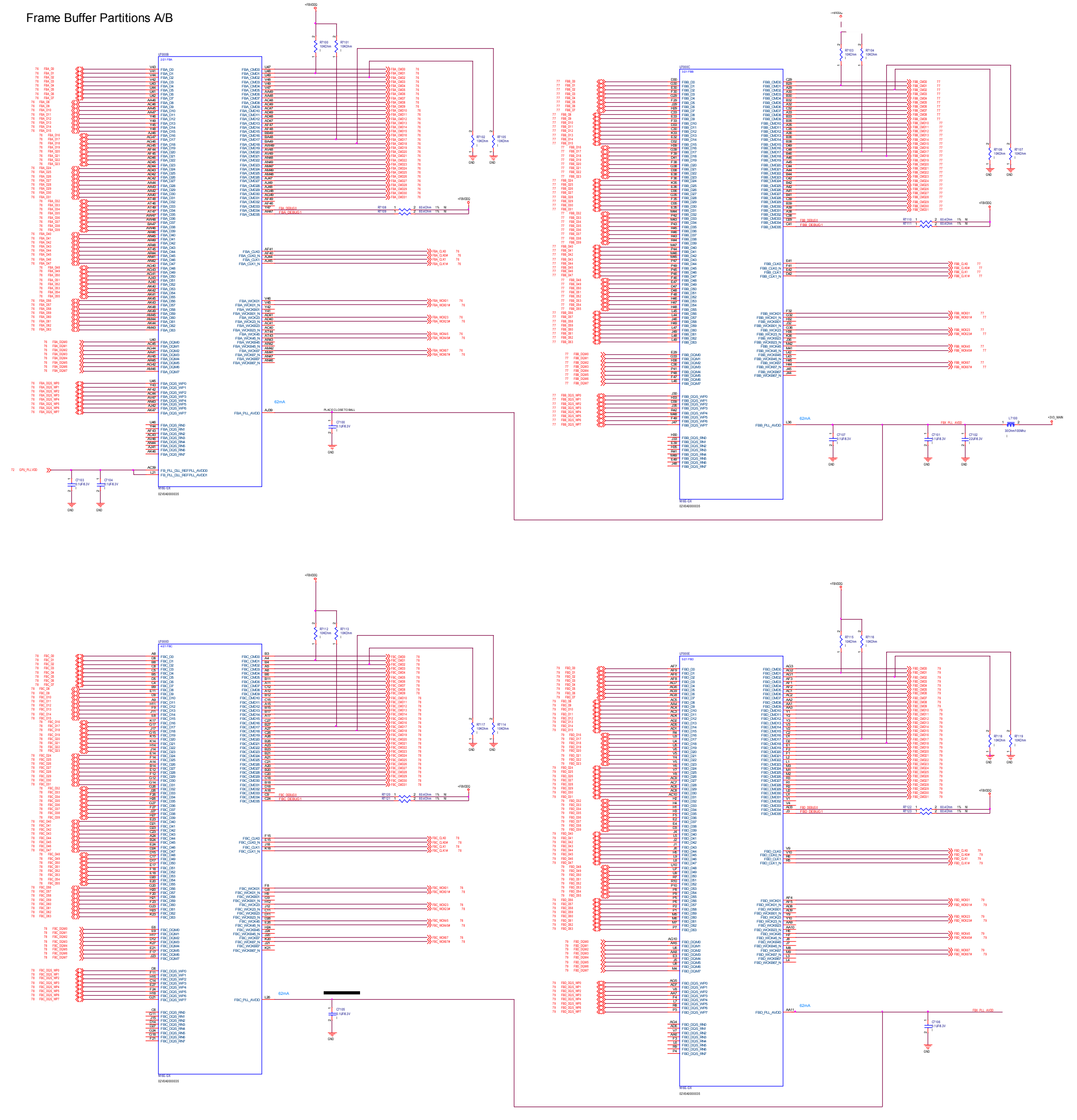
Date: Monday, September 07, 2015 Sheet 67 of 108

PCI-Express Gen2 x 8 Interface

R1.01-2012/09/26:add C9972 220pf "NI" for GPU "PCIE_RST#"
R1.01-2012/09/28: For GPU PCIE_WAKE#,Add NR132 0ohm for switch.



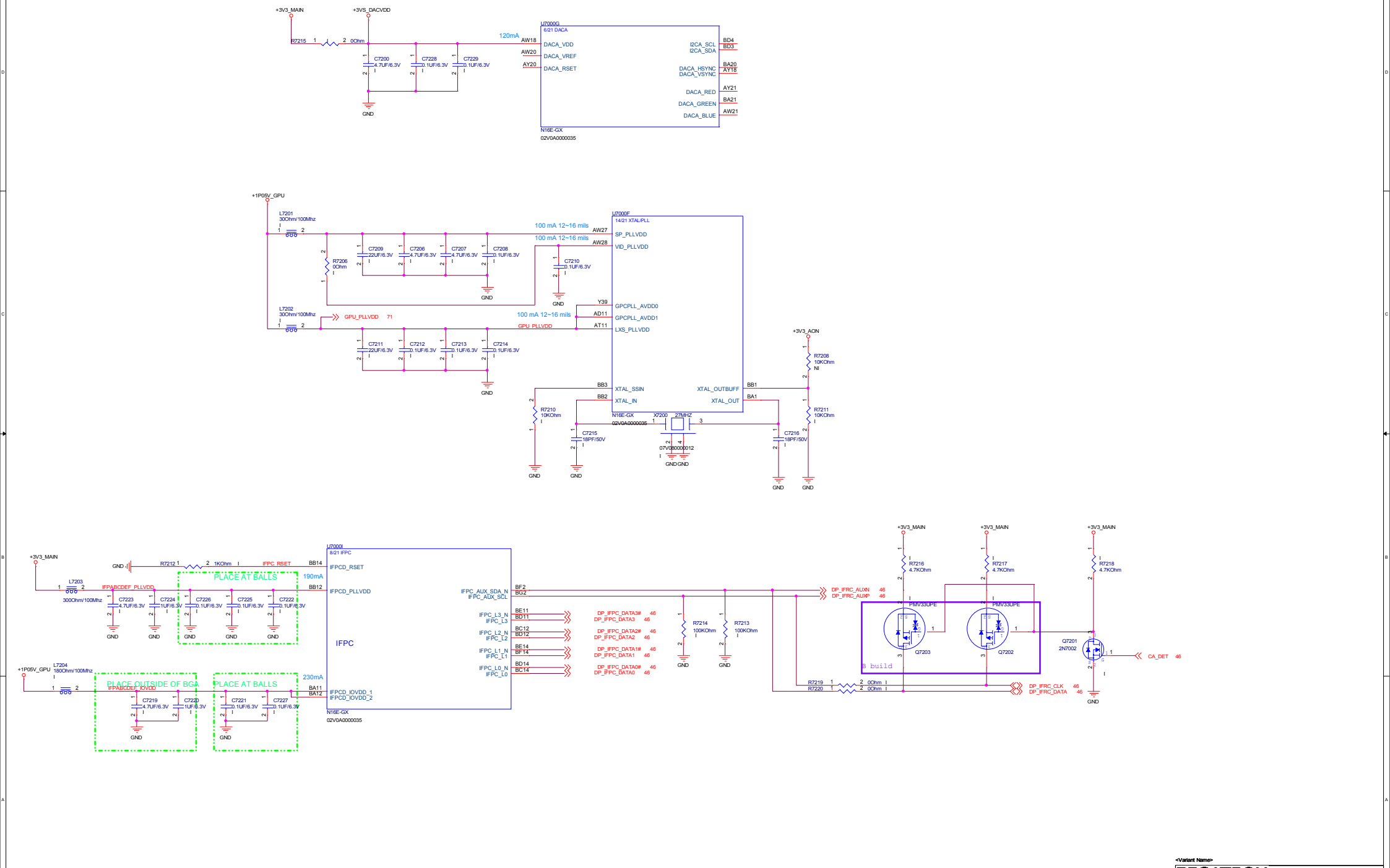
Frame Buffer Partitions A/B



<Variant Name>

PEGATRON	Title : NVDIA/BUFFERA/B		
Pegatron Corp.	Engineer: Aliens_Hsu		
Size: Custom	Project Name: P5NCN/P7NCN MAIN BOARD		Rev: A1.0
Date: Monday, September 07, 2015	Sheet 71 of 104		

Power/Decoupling: +NVVDD,3V3_NV,GRND,and [illegible]



<Variant Name>

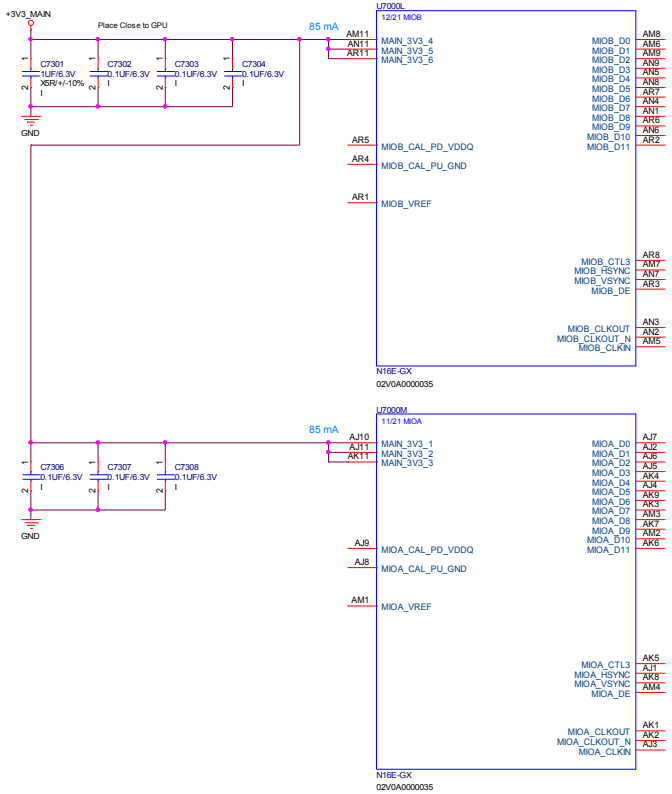
PEGATRON Title : NVDIA/DACA/XTAL

Pegatron Corp. Engineer: Aliens_Hsu

Size	Project Name	Rev
A2	P5NCN/P7NCN MAIN BOARD	A1.0

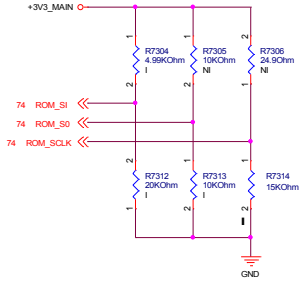
Date: Monday, September 07, 2015 Sheet 72 of 104

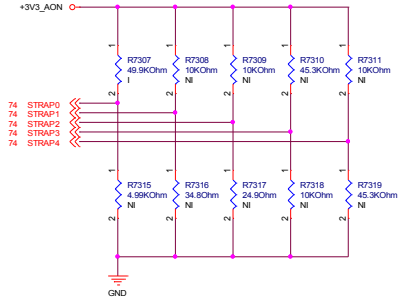
BIOS, External SS, and Miscellaneous Components



ROM_SI RAM CONFIG

```
Hynix(H5GC4H24AJR)  128Mx32  -> ram_cfg = 0x8      4.99K PU
Samsung 128Mx32 -> ram_cfg = 0x3                    20K PD
```





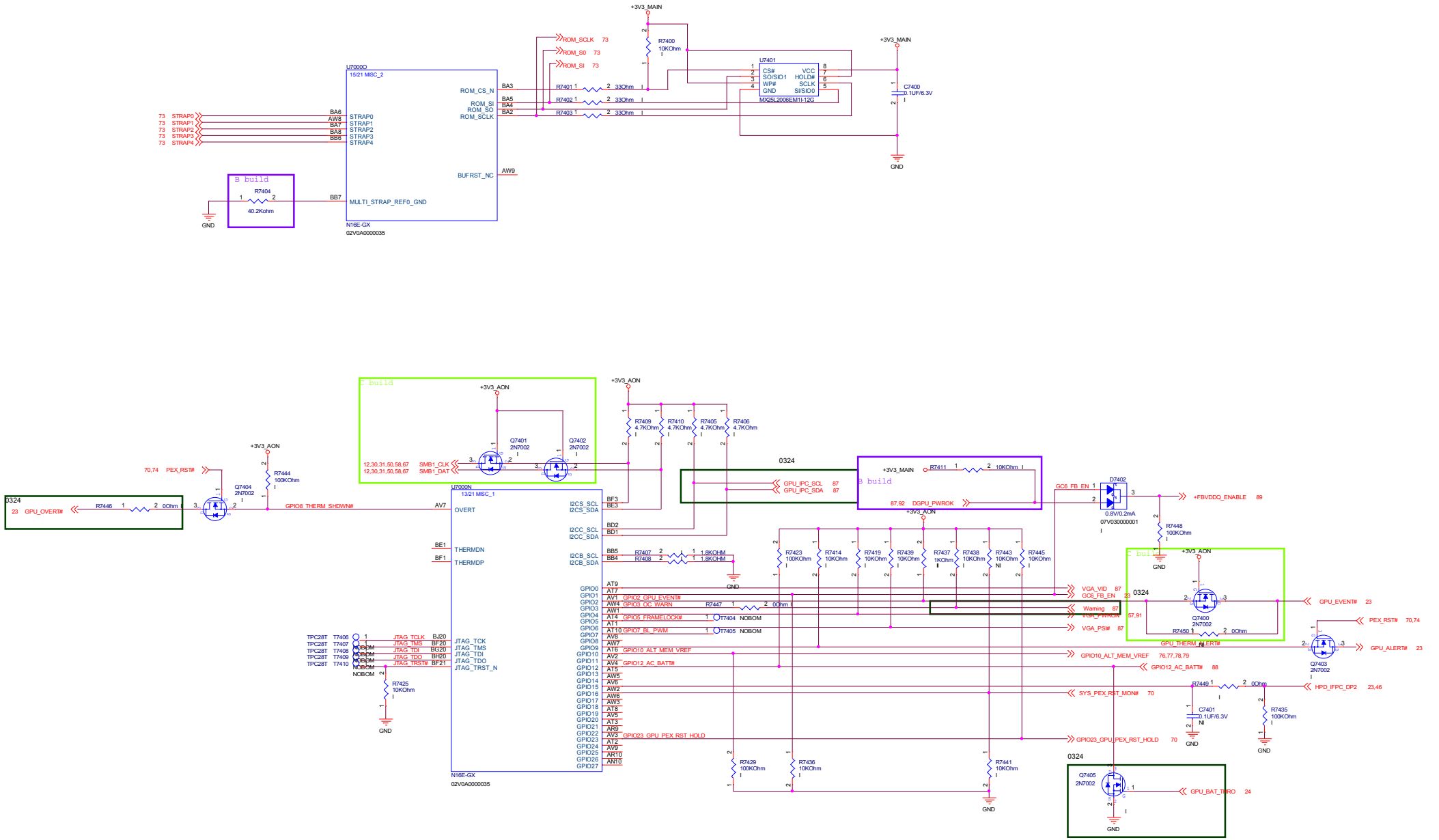
<Variant Name>

PEGATRON Title : NVDIA/Multi-use IO

Pegatron Corp. Engineer: Aliens_Hsu

Size	Project Name	Rev
A2	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 73 of 104



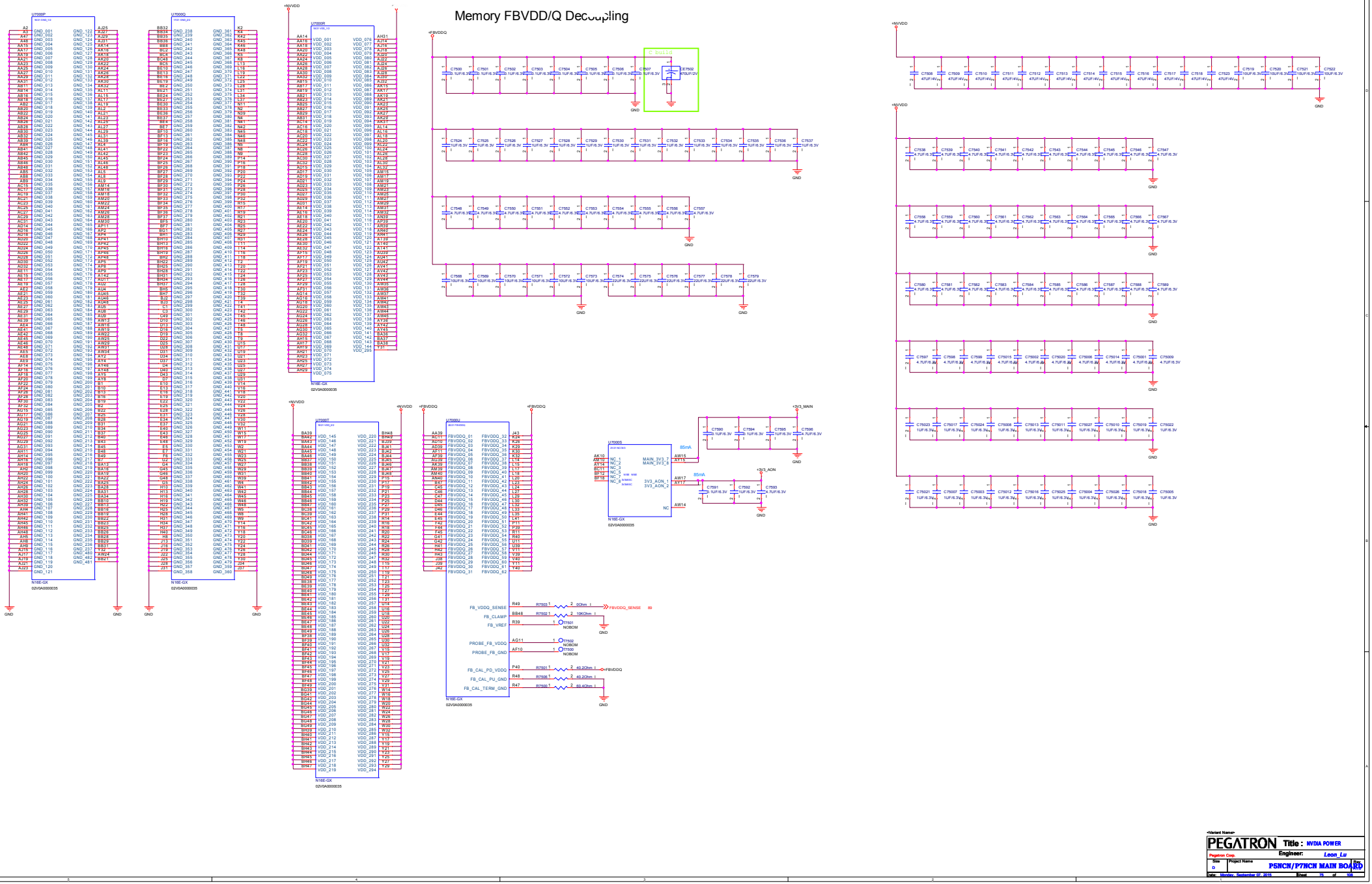
PEGATRON Title : NVDIA MISC/GPIO

Pegatron Corp. Engineer: Leon_Lu

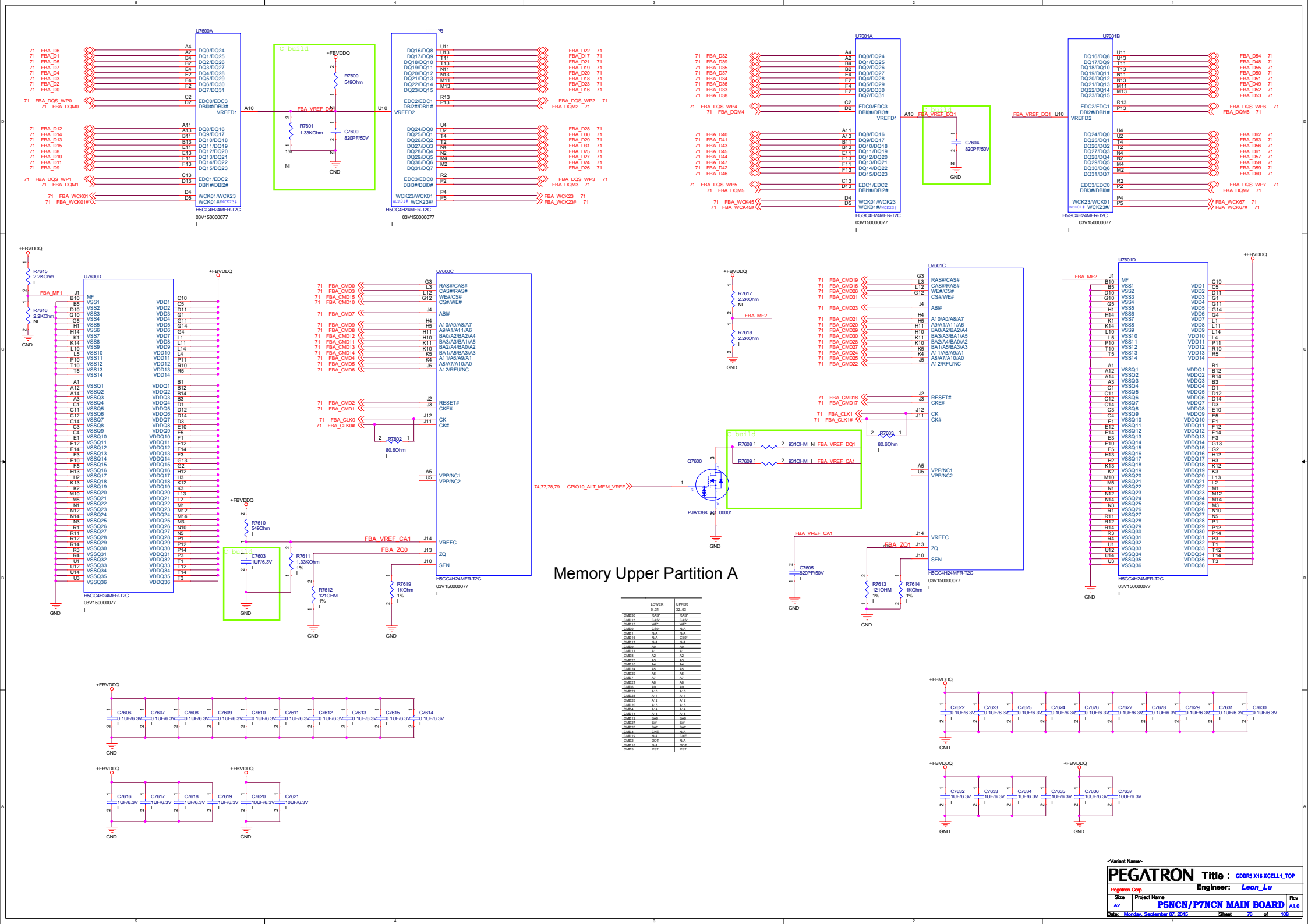
Size	Project Name	Rev
A2	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 74 of 108

Memory FBVDD/Q Decoupling



PEGATRON Title : NVDIA POWER
Pegatron Corp. Engineer: Leon_Lu
Size: D Project Name: P5NCN/P7NCN MAIN BOARD Rev:
Date: Monday, September 07, 2015 Sheet: 75 of: 108



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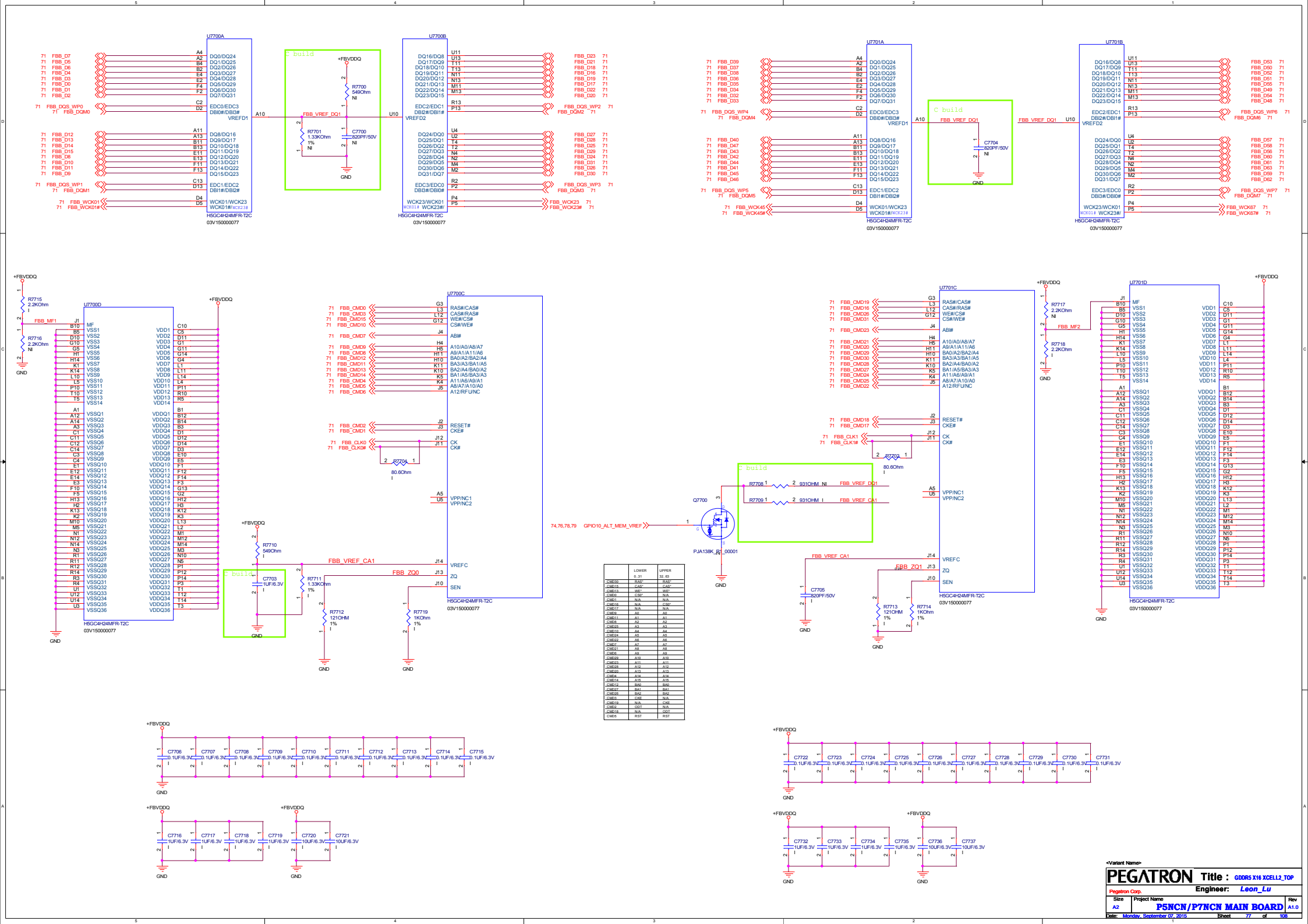
CMD30	RAS#	RAS#
CMD15	CAS#	CAS#
CMD13	WE#	WE#
CMD5	CS0#	N/A
CMD1	N/A	N/A
CMD16	N/A	CS0#
CMD17	N/A	N/A
CMD9	A0	A0
CMD11	A1	A1
CMD8	A2	A2
CMD28	A3	A3
CMD10	A4	A4
CMD24	A5	A5
CMD22	A6	A6
CMD7	A7	A7
CMD21	A8	A8
CMD6	A9	A9
CMD29	A10	A10
CMD23	A11	A11
CMD26	A12	A12
CMD20	A13	A13
CMD4	A14	A14
CMD14	A15	A15
CMD12	BA0	BA0
CMD27	BA1	BA1
CMD25	BA2	BA2
CMD3	CKE	CKE
CMD19	N/A	CKE
CMD2	ODT	N/A
CMD18	N/A	ODT
CMD5	RST	RST

<Variant Name>
PEGATRON Title : GDDR5 X16 XCELL1_TOP
Pegatron Corp. Engineer: Leon_Lu
Size A2 | Project Name P5NCN/P7NCN MAIN BOARD | Rev A1.0
Date: Monday, September 07, 2015 Sheet 78 of 108


U7700A
U7700B
U7701A
U7701B
U7700C
U7700D
U7701C
U7701D
H5GC4H24MFR-T2C
03V150000077
C build
+FBVDDQ
GND
R7700 549Ohm NI
R7701 1.33KOhm 1% NI
C7700 820PF/50V NI
FBB_VREF_DQ1
R7715 2.2KOhm I
R7716 2.2KOhm NI
FBB_MF1
R7717 2.2KOhm NI
R7718 2.2KOhm I
FBB_MF2
R7710 549Ohm I
R7711 1.33KOhm 1% I
R7712 121OHM 1%
R7719 1KOhm 1%
C7703 1UF/6.3V I
FBB_VREF_CA1
FBB_ZQ0
R7702 80.6Ohm I
R7703 80.6Ohm I
R7708 931OHM_NI
R7709 931OHM I
Q7700
PJA138K_R1_00001
74,76,78,79 GPIO10_ALT_MEM_VREF
C7704 820PF/50V NI
C7705 820PF/50V
FBB_ZQ1
R7713 121OHM 1%
R7714 1KOhm 1%
C7706 C7707 C7708 C7709 C7710 C7711 C7712 C7713 C7714 C7715 0.1UF/6.3V
C7716 C7717 C7718 C7719 1UF/6.3V
C7720 C7721 10UF/6.3V
C7722 C7723 C7724 C7725 C7726 C7727 C7728 C7729 C7730 C7731 0.1UF/6.3V
C7732 C7733 C7734 C7735 1UF/6.3V
C7736 C7737 10UF/6.3V
RAS#/CAS#
CAS#/RAS#
WE#/CS#
CS#/WE#
ABI#
RESET#
CKE#
CK
CK#
VPP/NC1
VPP/NC2
ZQ
SEN
VREFC
A10/A0/A8/A7
A9/A1/A11/A6
BA0/A2/BA2/A4
BA3/A3/BA1/A5
BA2/A4/BA0/A2
BA1/A5/BA3/A3
A11/A6/A9/A1
A8/A7/A10/A0
A12/RFU/NC
DQ0/DQ24
DQ1/DQ25
DQ2/DQ26
DQ3/DQ27
DQ4/DQ28
DQ5/DQ29
DQ6/DQ30
DQ7/DQ31
DQ8/DQ16
DQ9/DQ17
DQ10/DQ18
DQ11/DQ19
DQ12/DQ20
DQ13/DQ21
DQ14/DQ22
DQ15/DQ23
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DBI0#/DBI3#
EDC1/EDC2
DBI1#/DBI2#
EDC2/EDC1
DBI2#/DBI1#
EDC3/EDC0
DBI3#/DBI0#
WCK01/WCK23
WCK01#/WCK23#
WCK23/WCK01
WCK23#/WCK01#
VREFD1
VREFD2
MF
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VSS2
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VDDQ3
VDDQ4
VDDQ5
VDDQ6
VDDQ7
VDDQ8
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VDDQ14
VDDQ15
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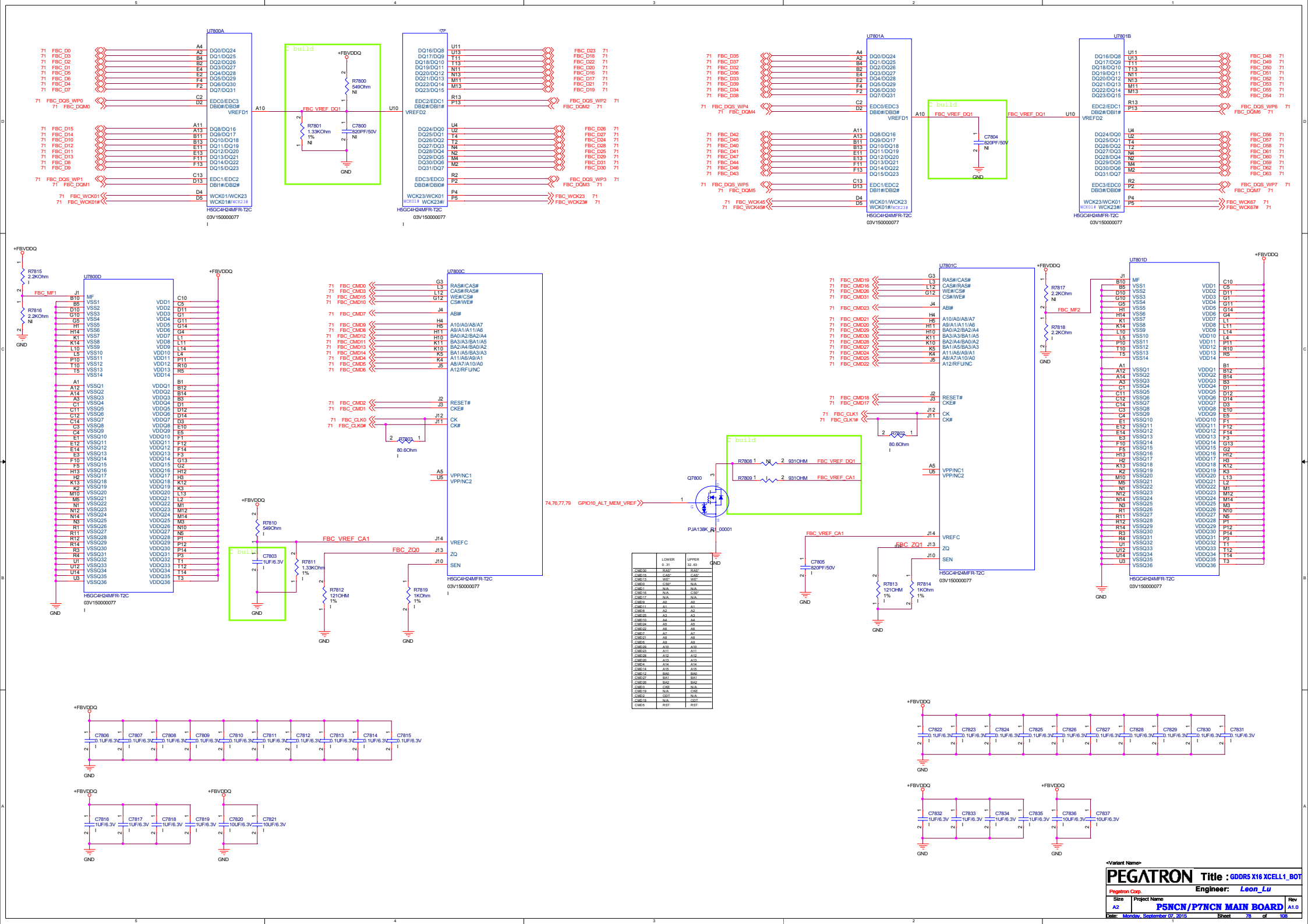
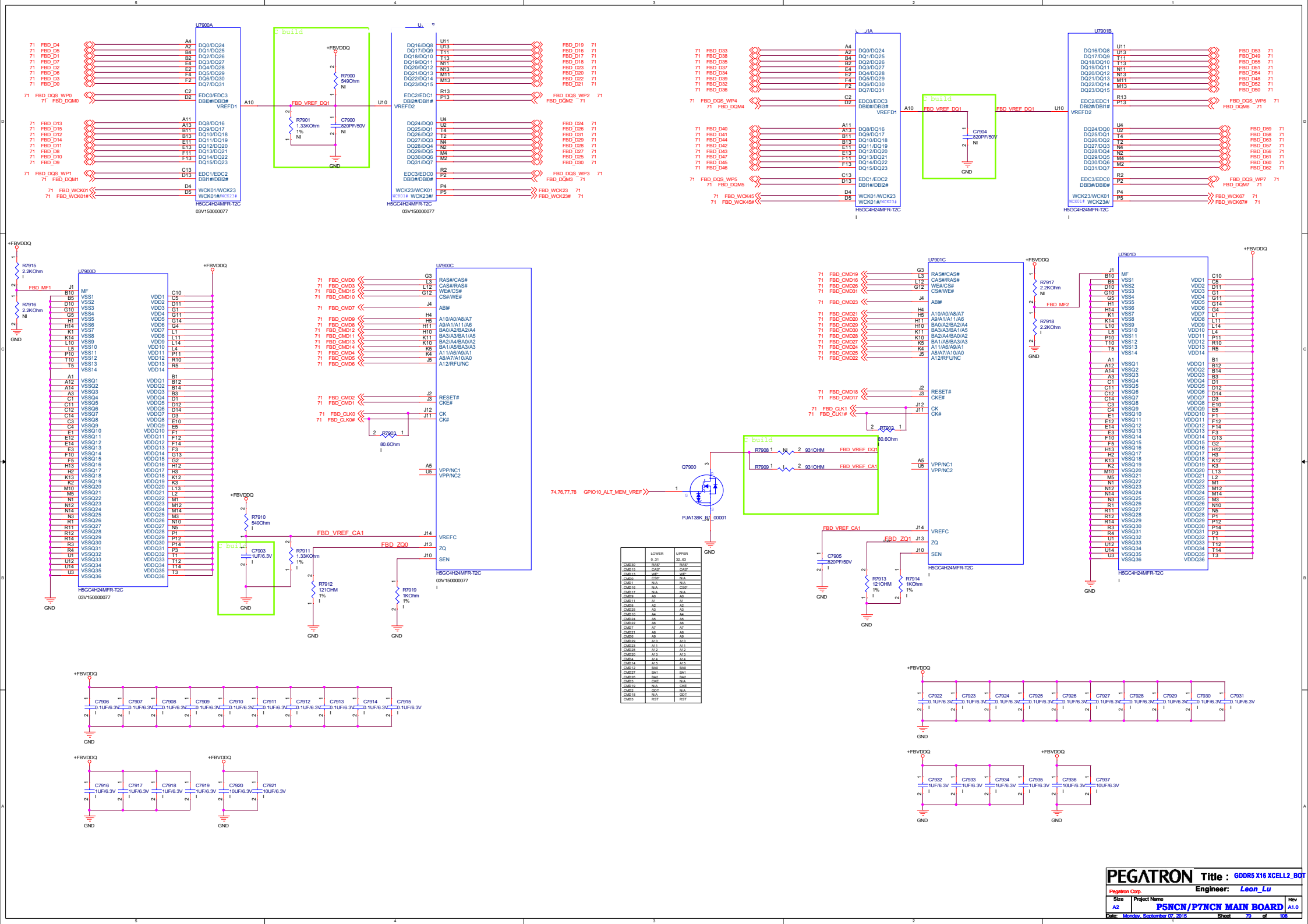
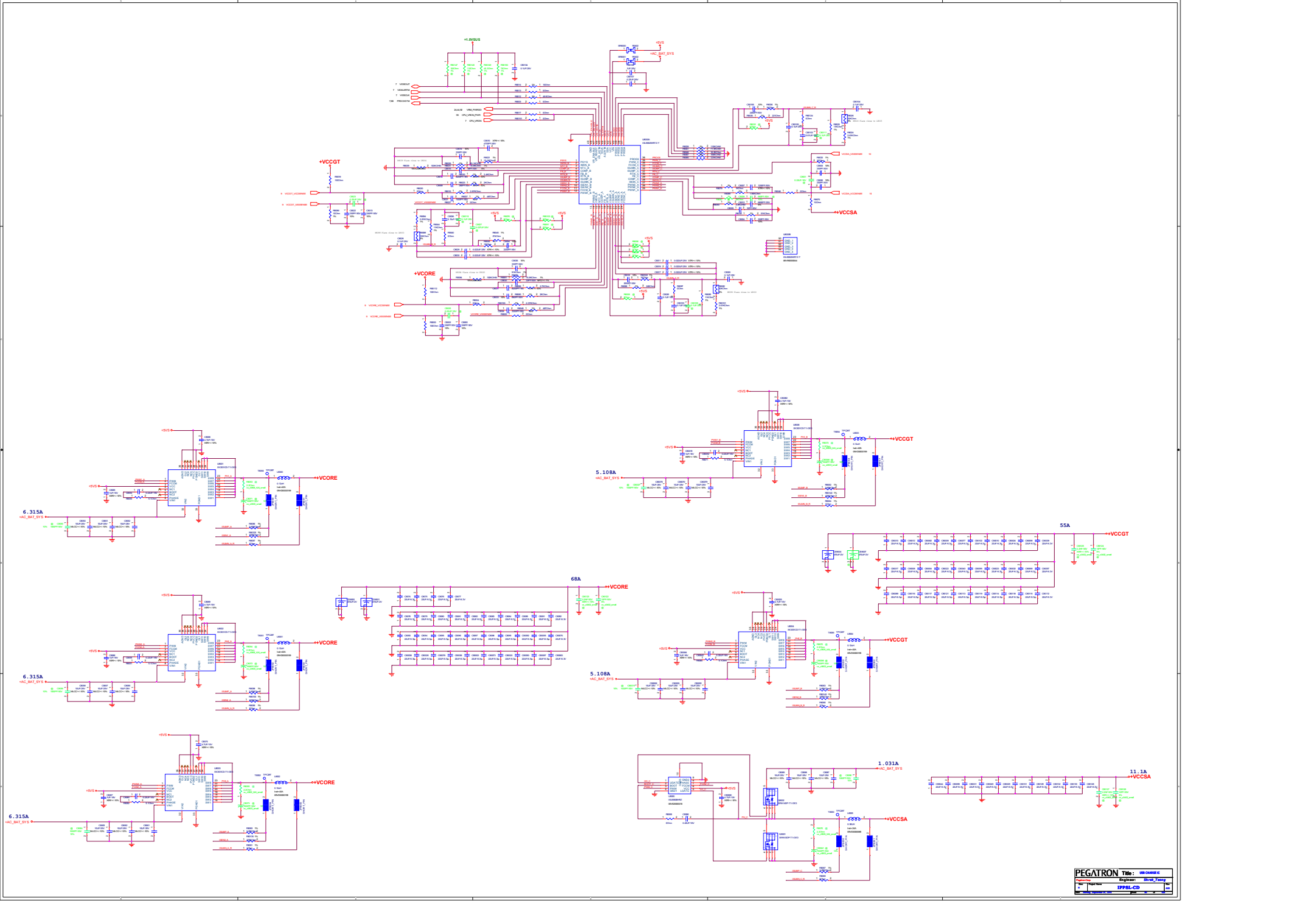
VDDQ31
VDDQ32
VDDQ33
VDDQ34
VDDQ35
VDDQ36
LOWER 5..31
UPPER 32..63
CMD20 RAS# RAS#
CMD19 CAS# CAS#
CMD13 WE# WE#
CMD0 CS0# N/A
CMD1 N/A N/A
CMD16 N/A CS0#
CMD17 N/A N/A
CMD9 A0 A0
CMD11 A1 A1
CMD8 A2 A2
CMD25 A3 A3
CMD10 A4 A4
CMD24 A5 A5
CMD22 A6 A6
CMD7 A7 A7
CMD21 A8 A8
CMD5 A9 A9
CMD29 A10 A10
CMD23 A11 A11
CMD28 A12 A12
CMD20 A13 A13
CMD4 A14 A14
CMD14 A15 A15
CMD12 BA0 BA0
CMD27 BA1 BA1
CMD26 BA2 BA2
CMD3 CKE N/A
CMD19 N/A CKE
CMD2 ODT N/A
CMD18 N/A ODT
CMD15 RST RST
Title : GDDR5 X16 XCELL2_TOP
Engineer: Leon_Lu
Pegatron Corp.
Size A2
Project Name P5NCN/P7NCN MAIN BOARD
Rev A1.0
Date: Monday, September 07, 2015
Sheet 77 of 108


U7800A
U7800B
U7801A
U7801B
U7800C
U7800D
U7801C
U7801D
H5GC4H24MFR-T2C
03V150000077
+FBVDDQ
GND
C build
R7800 549Ohm NI
R7801 1.33KOhm 1%
C7800 820PF/50V NI
R7804 820PF/50V NI
R7815 2.2KOhm
R7816 2.2KOhm NI
R7817 2.2KOhm NI
R7818 2.2KOhm
R7802 80.6Ohm
R7803 80.6Ohm
R7808 931OHM
R7809 931OHM
Q7800
PJA138K_R1_00001
R7810 549Ohm
C7803 1UF/6.3V
R7811 1.33KOhm 1%
R7812 121OHM 1%
R7819 1KOhm 1%
C7805 820PF/50V
R7813 121OHM 1%
R7814 1KOhm 1%
FBC_VREF_DQ1
FBC_VREF_CA1
FBC_ZQ0
FBC_ZQ1
FBC_MF1
FBC_MF2
GPIO10_ALT_MEM_VREF
C7806 C7807 C7808 C7809 C7810 C7811 C7812 C7813 C7814 C7815 0.1UF/6.3V
C7816 C7817 C7818 C7819 1UF/6.3V
C7820 C7821 10UF/6.3V
C7822 C7823 C7824 C7825 C7826 C7827 C7828 C7829 C7830 C7831 0.1UF/6.3V
C7832 C7833 C7834 C7835 1UF/6.3V
C7836 C7837 10UF/6.3V
<Variant Name>
PEGATRON
Title : GDDR5 X16 XCELL1_BOT
Pegatron Corp.
Engineer: Leon_Lu
Size A2
Project Name P5NCN/P7NCN MAIN BOARD
Rev A1.0
Date: Monday, September 07, 2015
Sheet 78 of 108

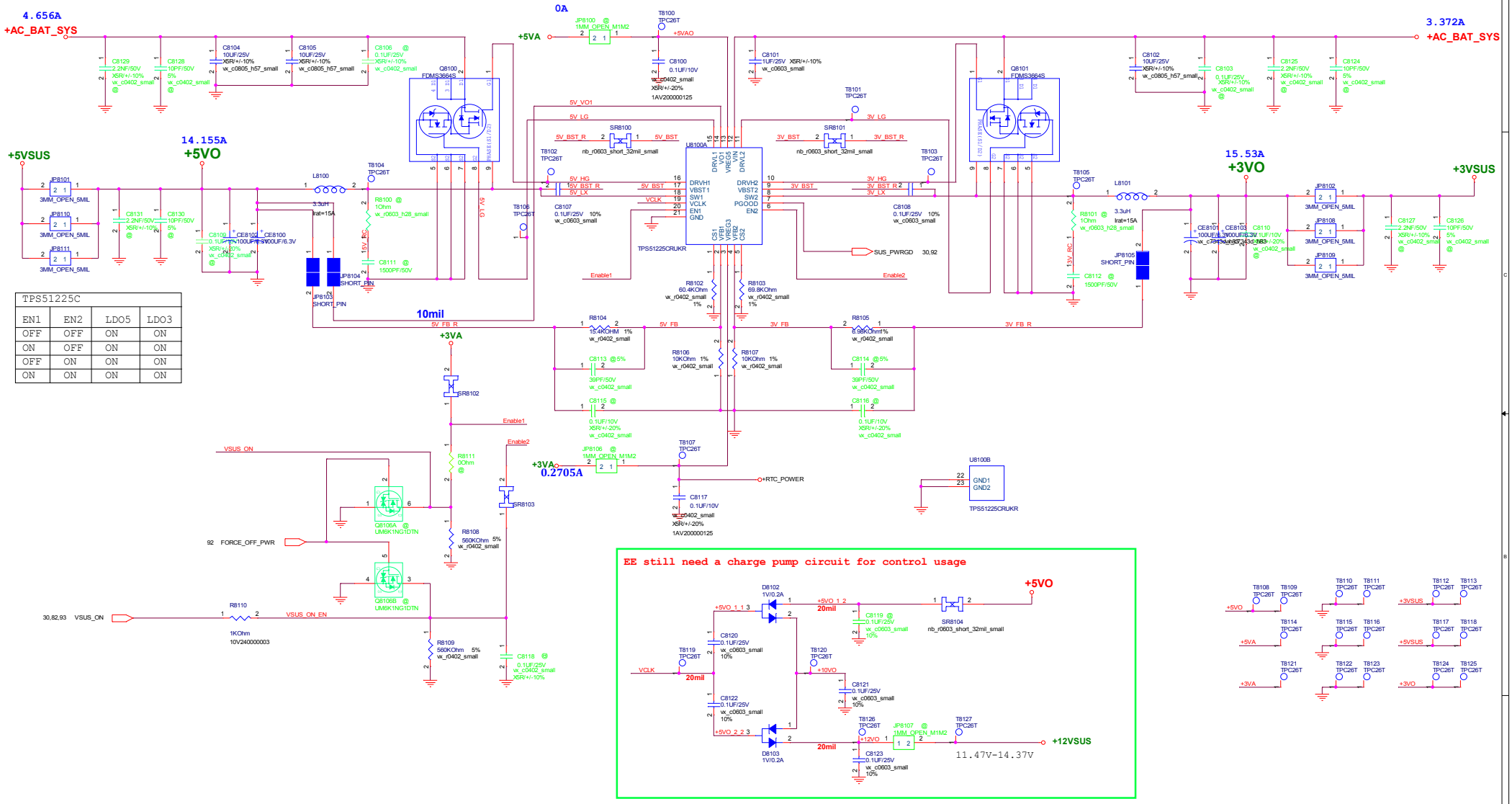


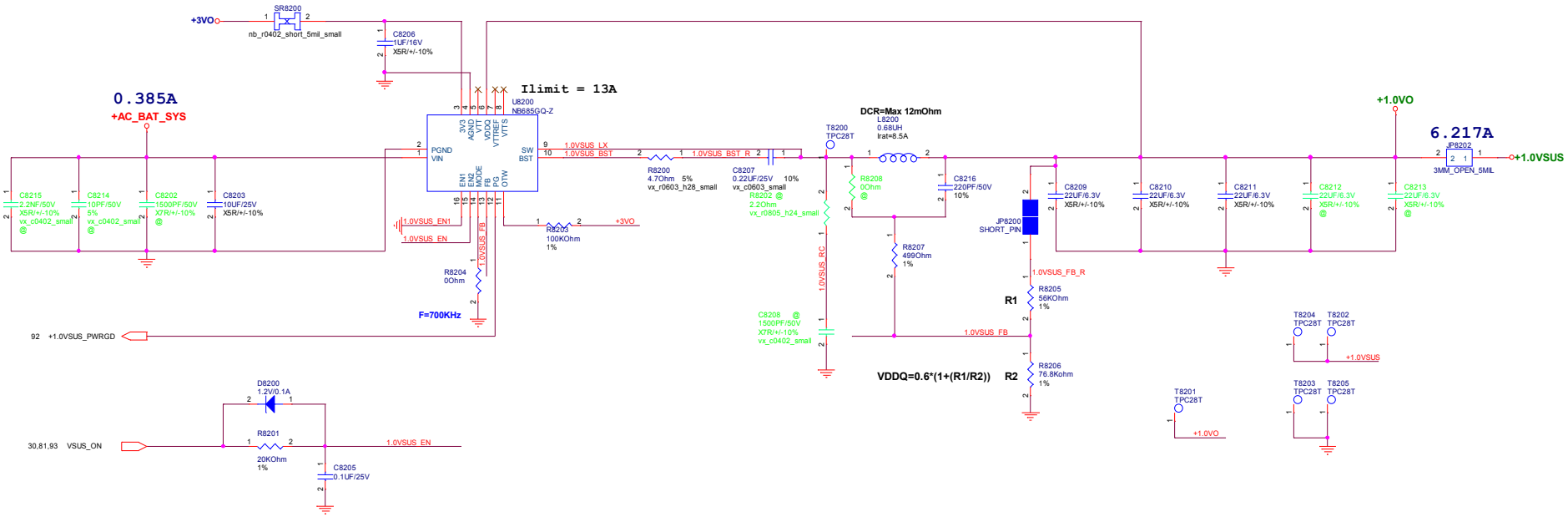
	LOWER 0..31	UPPER 32..63
CMD30	RAS#	RAS#
CMD15	CAS#	CAS#
CMD13	WE#	WE#
CMD29	CS0#	N/A
CMD1	N/A	N/A
CMD16	N/A	CS0#
CMD17	N/A	N/A
CMD9	A0	A0
CMD11	A1	A1
CMD8	A2	A2
CMD25	A3	A3
CMD10	A4	A4
CMD24	A5	A5
CMD22	A6	A6
CMD7	A7	A7
CMD21	A8	A8
CMD5	A9	A9
CMD20	A10	A10
CMD23	A11	A11
CMD28	A12	A12
CMD20	A13	A13
CMD4	A14	A14
CMD14	A15	A15
CMD12	BA0	BA0
CMD27	BA1	BA1
CMD26	BA2	BA2
CMD3	CKE	N/A
CMD19	N/A	CKE
CMD2	ODT	N/A
CMD18	N/A	ODT
CMD31	RST	RST

PEGATRON	Title :	GDDR5 X16 XCELL2_BOT
Pegatron Corp.	Engineer:	Leon_Lu
Size: A2	Project Name:	P5NCN/P7NCN MAIN BOARD
Rev: A1.0		
Date: Monday, September 07, 2015	Sheet:	79 of 108


+1.05VSUS
+VCCGT
+VCORE
+VCCSA
+5VS
+AC_BAT_SYS
6.315A
5.108A
68A
55A
1.031A
11.1A
PEGATRON
Title : USB CHARGE IC
Engineer: Brad_Tseng
IPP81_CD

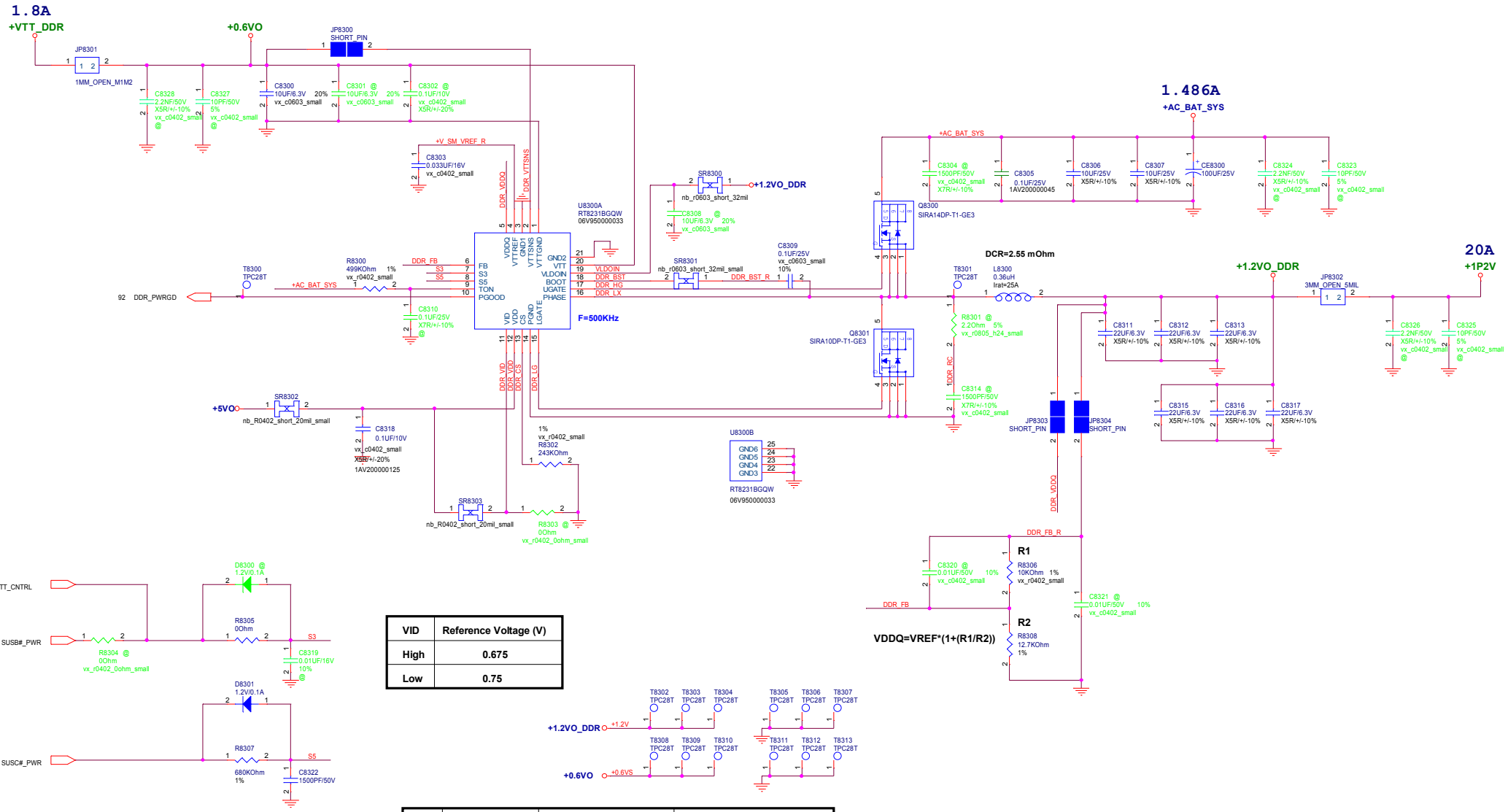
+5VO & +3VO POWER SUPPLY





PEGATRON	Title :	USB CHARGE IC	
Pegatron Corp.	Engineer:	Shrek_Tseng	
Size: Custom	Project Name: IPPSL-CD		Rev: A00
Date: Monday, September 07, 2015	Sheet 82 of 108		

DDR & VTT POWER SUPPLY



VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

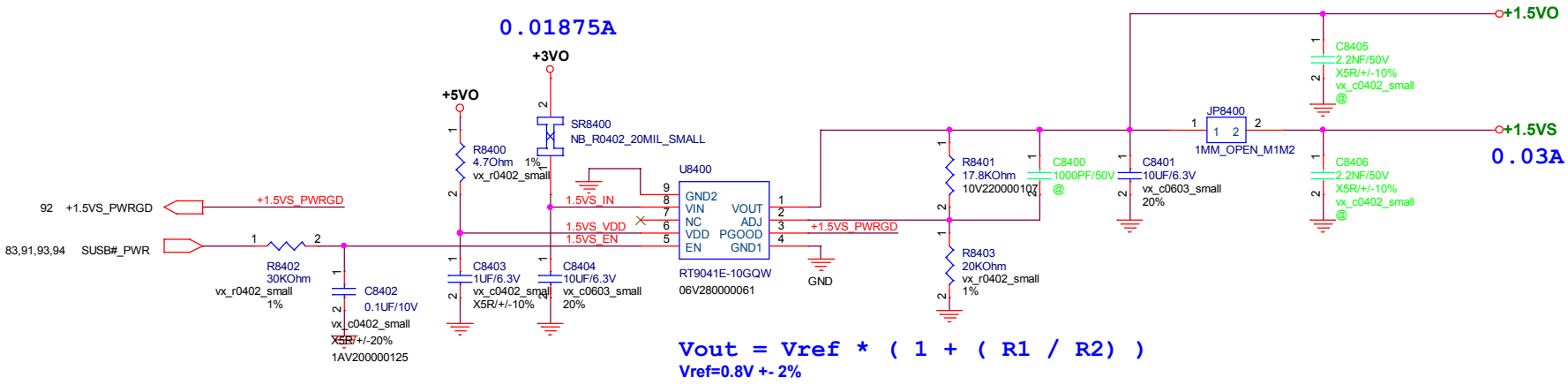
PEGATRON Title : USB CHARGE IC

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
Custom	IPPSL-CD	A00

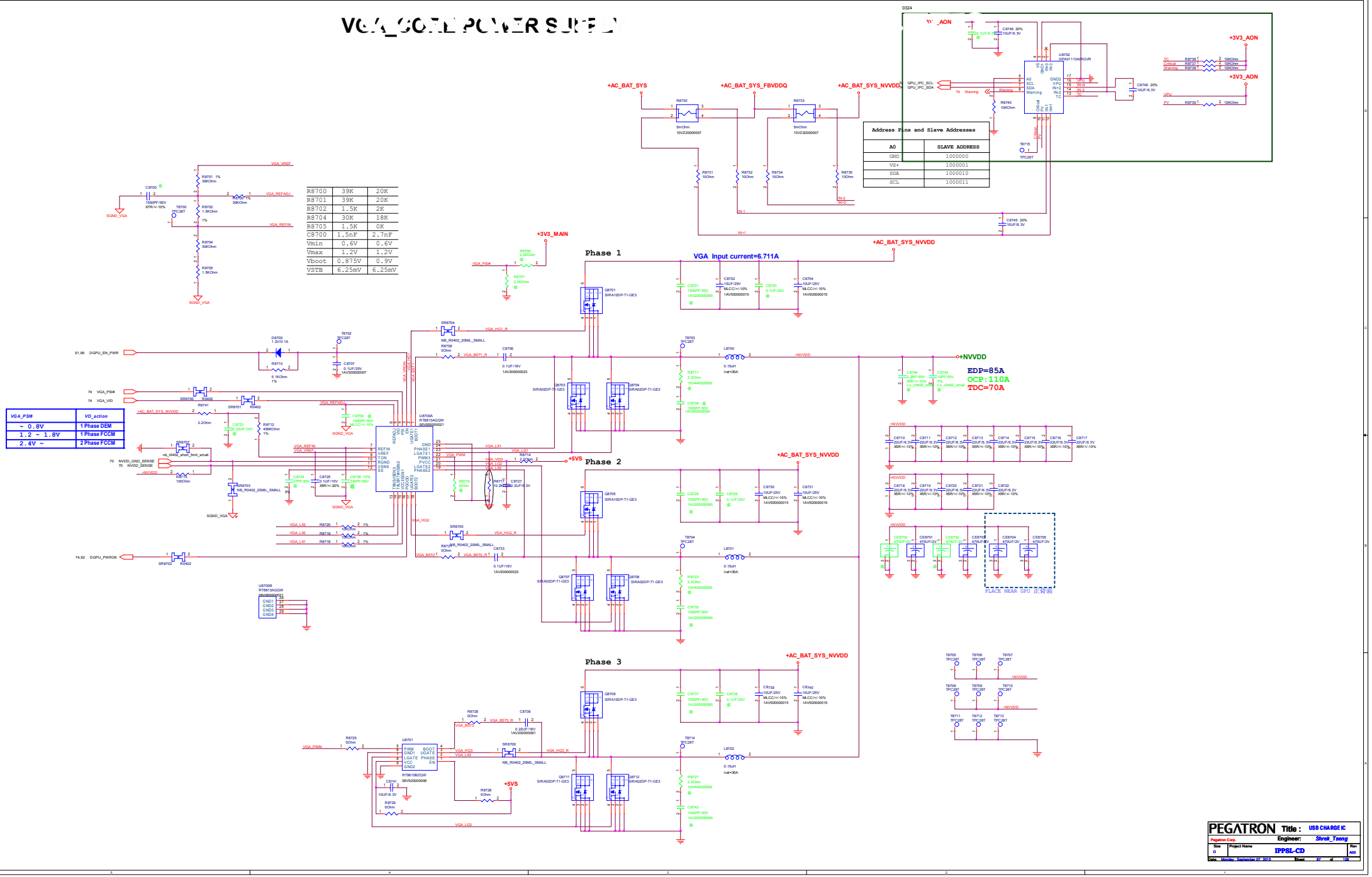
Date: Monday, September 07, 2015 Sheet 83 of 108

1.5V POWER SUPPLY



PEGATRON	Title : USB CHARGE IC		
Pegatron Corp.	Engineer: Shrek_Tseng		
Size: B	Project Name: IPPSL-CD		Rev: A00
Date: Monday, September 07, 2015	Sheet 84 of 108		

VGA_CORE POWER SUPPLY

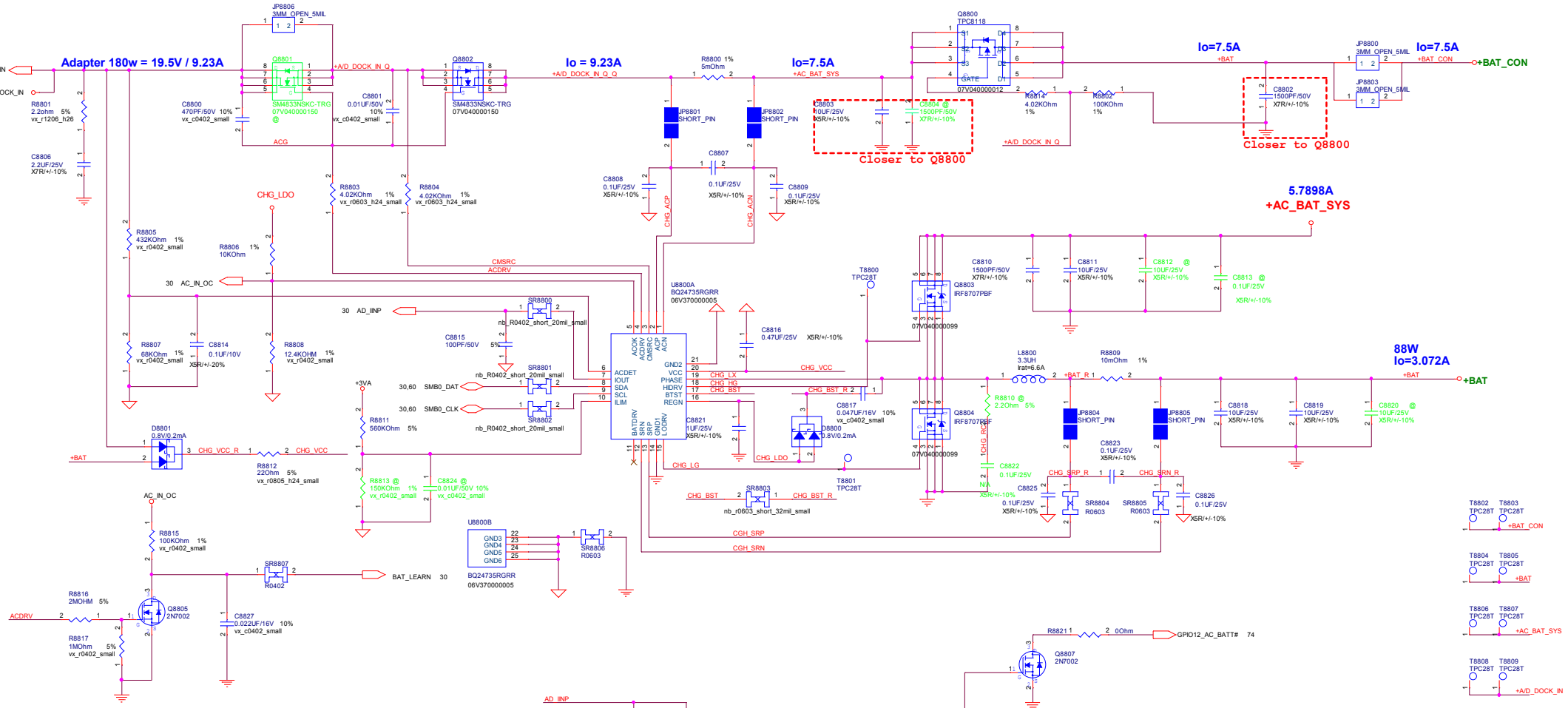


R8700	39K	20K
R8701	39K	20K
R8702	1.5K	2K
R8704	30K	18K
R8705	1.5K	0K
C8700	1.5nF	2.7nF
Vmin	0.6V	0.6V
Vmax	1.2V	1.2V
Vboot	0.875V	0.9V
VSTB	6.25mV	6.25mV

VGA_PSI#	VO_action
~ 0.8V	1 Phase DEM
1.2 ~ 1.8V	1 Phase FCCM
2.4V ~	2 Phase FCCM

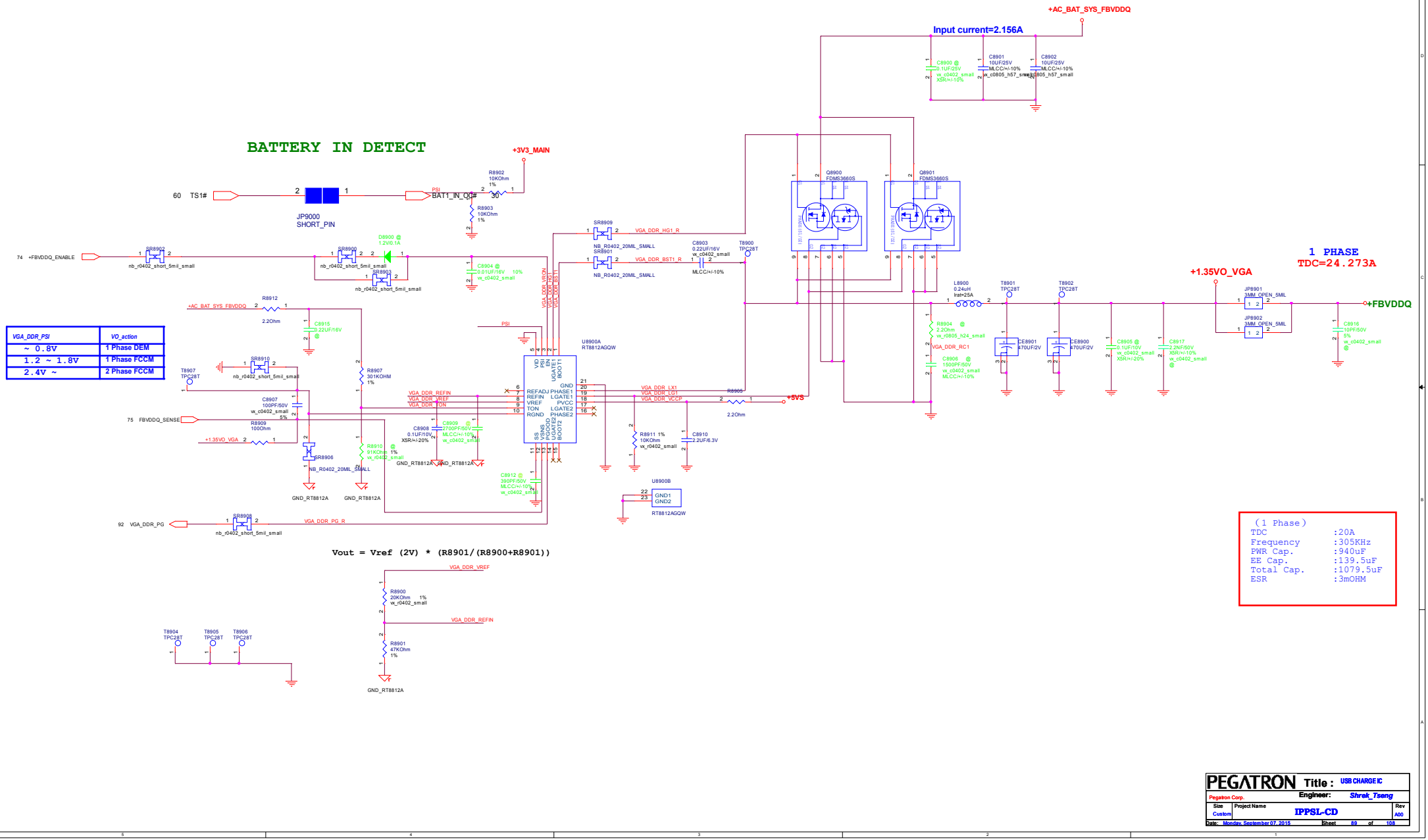
PEGATRON Title : USB CHARGE IC
Pegatron Corp. Engineer: Shrek_Tseng
Size D | Project Name IPPSL-CD | Rev A00
Date: Monday, September 07, 2015 Sheet 87 of 106

BATTERY CHARGER



Charger Vendor	TI
Charger P/N	BQ24735RGRR
Support Hybrid Boost?	YES
Adapter capacity	180W
Active/Release Point (Hybrid Boost)	Active - 163.7W Release - 142.3W
Enable condition Disable condition	RSOC>40% RSOC<30%

+FBVDDQ POWER SUPPLY



VGA_DDR_PSI	VO_action
~ 0.8V	1 Phase DEM
1.2 ~ 1.8V	1 Phase FCCM
2.4V ~	2 Phase FCCM

(1 Phase)

TDC	:20A
Frequency	:305KHz
PWR Cap.	:940uF
EE Cap.	:139.5uF
Total Cap.	:1079.5uF
ESR	:3mOHM

PEGATRON Title : USB CHARGE IC

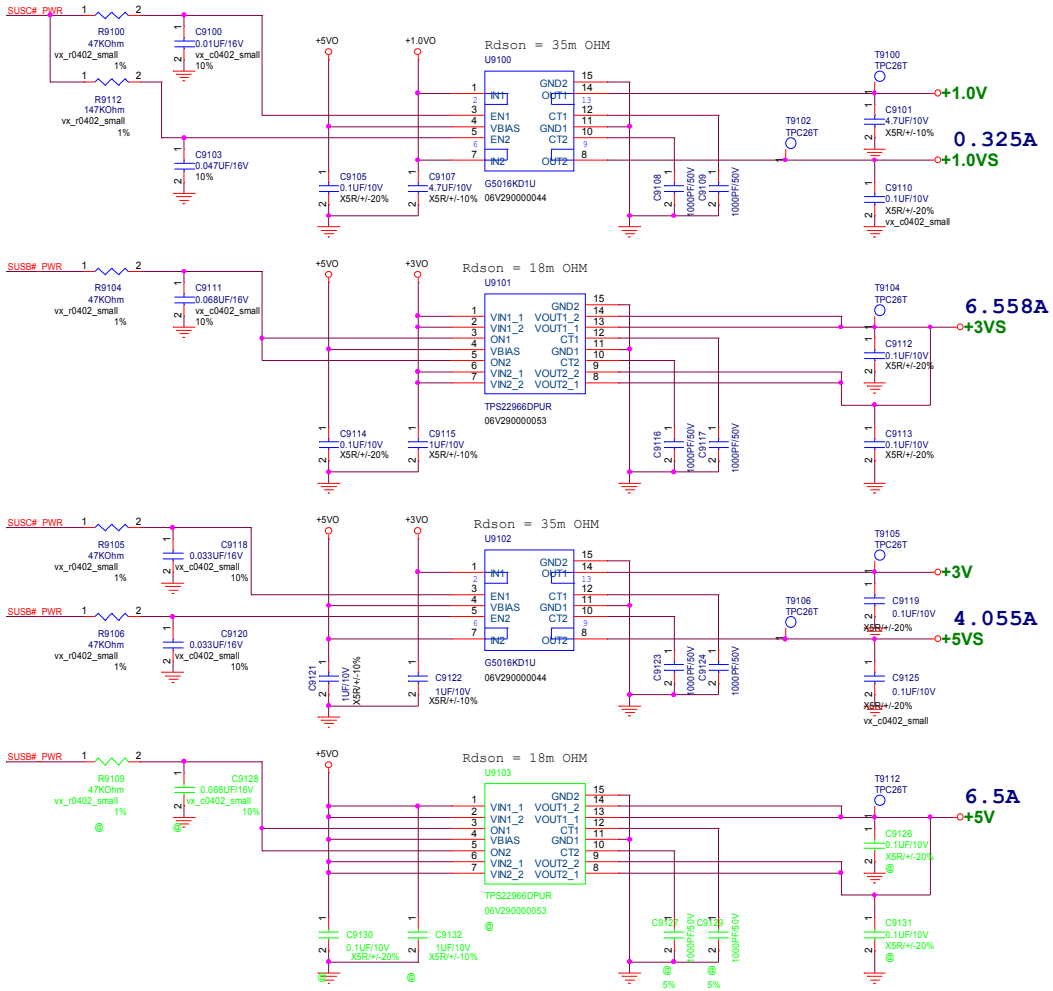
Pegatron Corp. Engineer: Shrek_Tseng

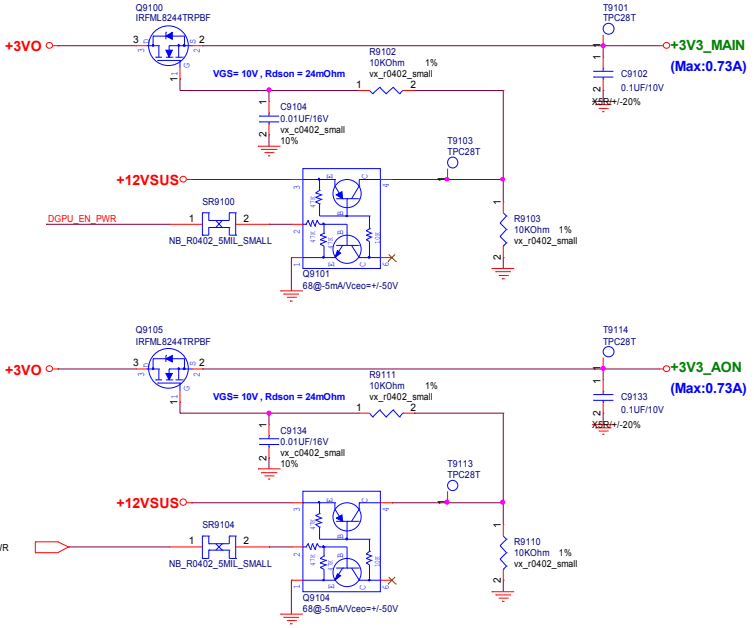
Size	Project Name	Rev
Custom	IPPSL-CD	A00

Date: Monday, September 07, 2015 Sheet 89 of 108

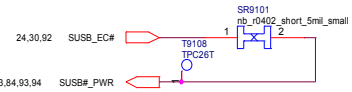
SUSB#_PWR POWER

SUSC#_PWR POWER

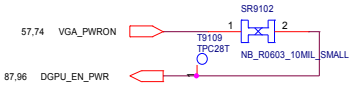




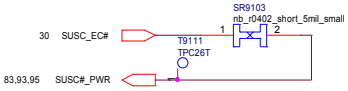
SUSB#_PWR POWER Control



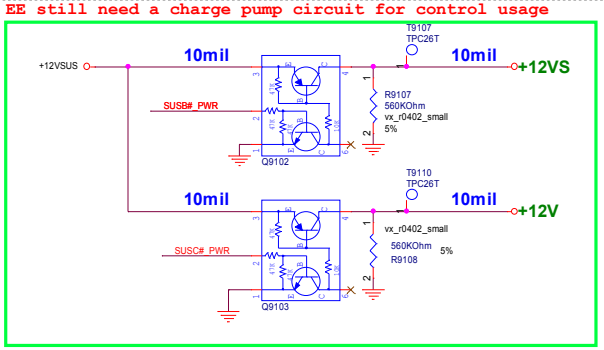
DSC_VGA_PWR POWER Control



SUSC#_PWR POWER Control



EE still need a charge pump circuit for control usage



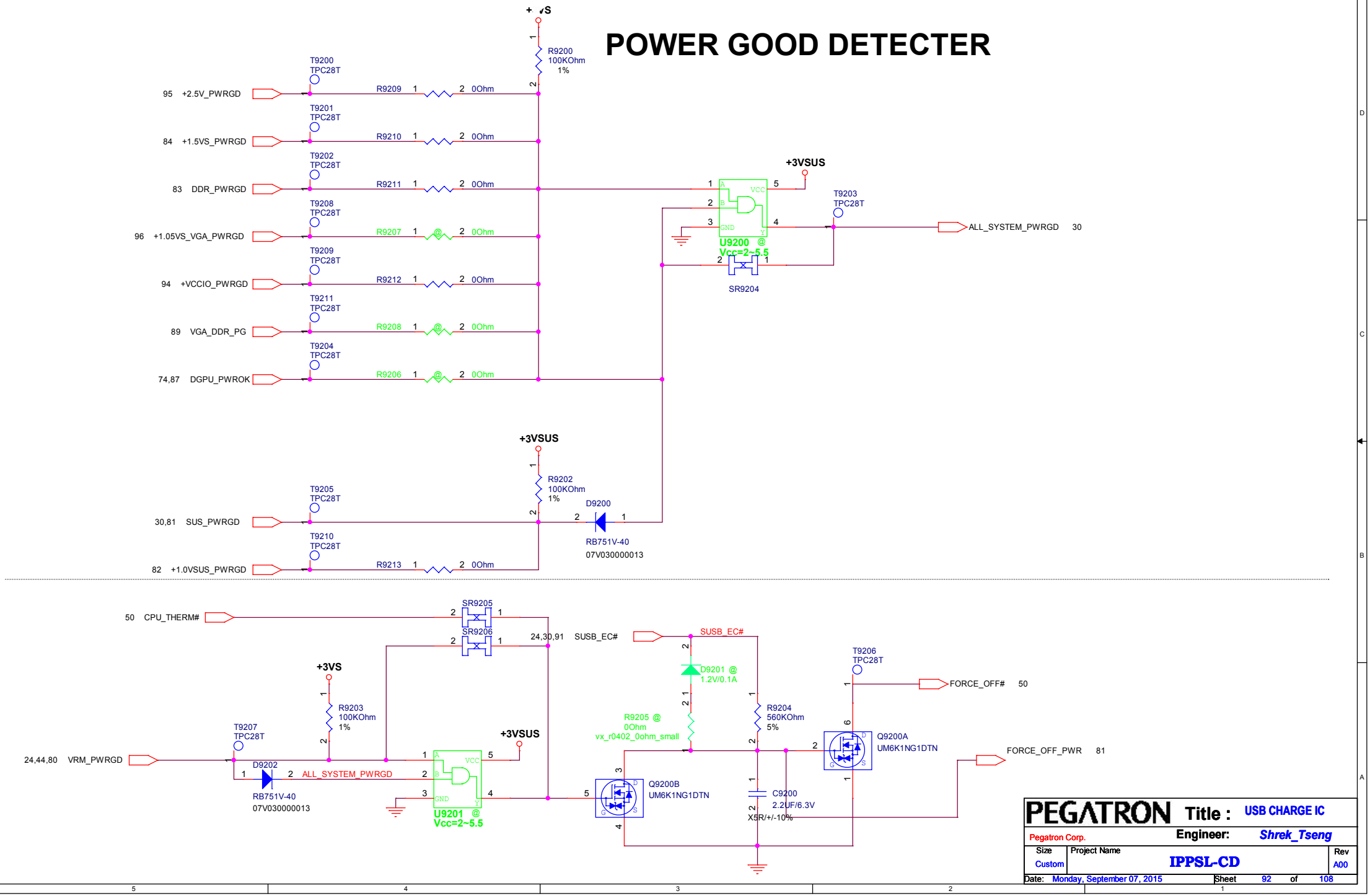
PEGATRON Title : USB CHARGE IC

Pegatron Corp. Engineer: Shrek_Tseng

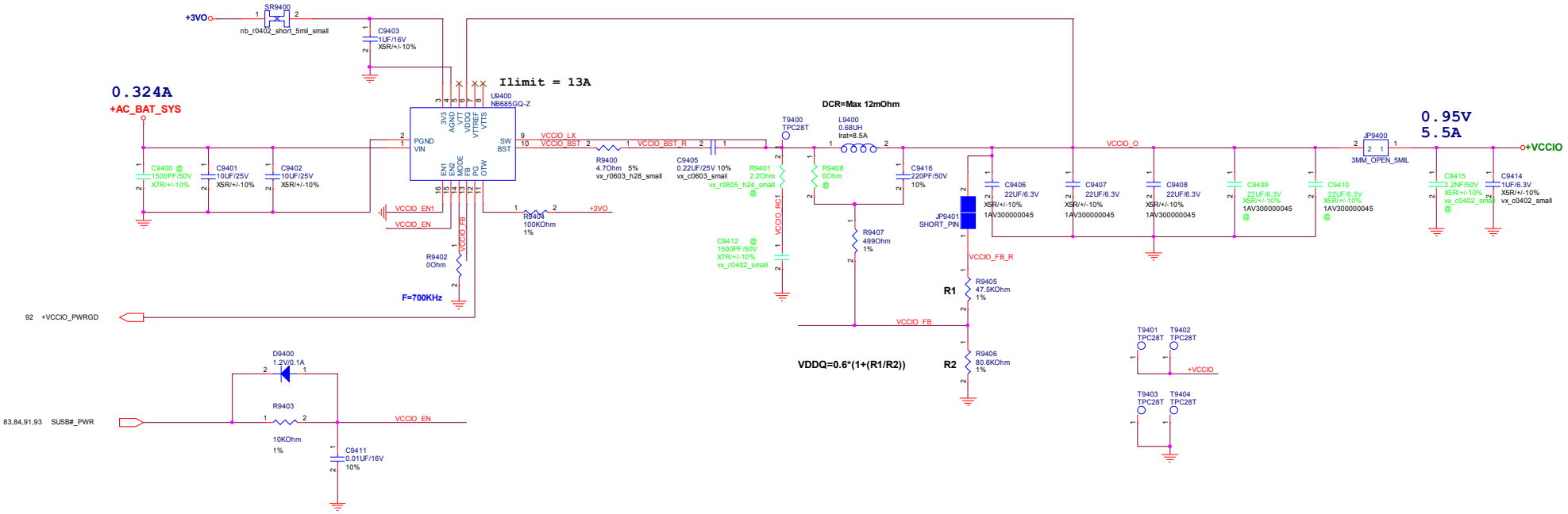
Size	Project Name	Rev
Custom	IPPSL-CD	A00

Date: Monday, September 07, 2015 Sheet 91 of 108

POWER GOOD DETECTER

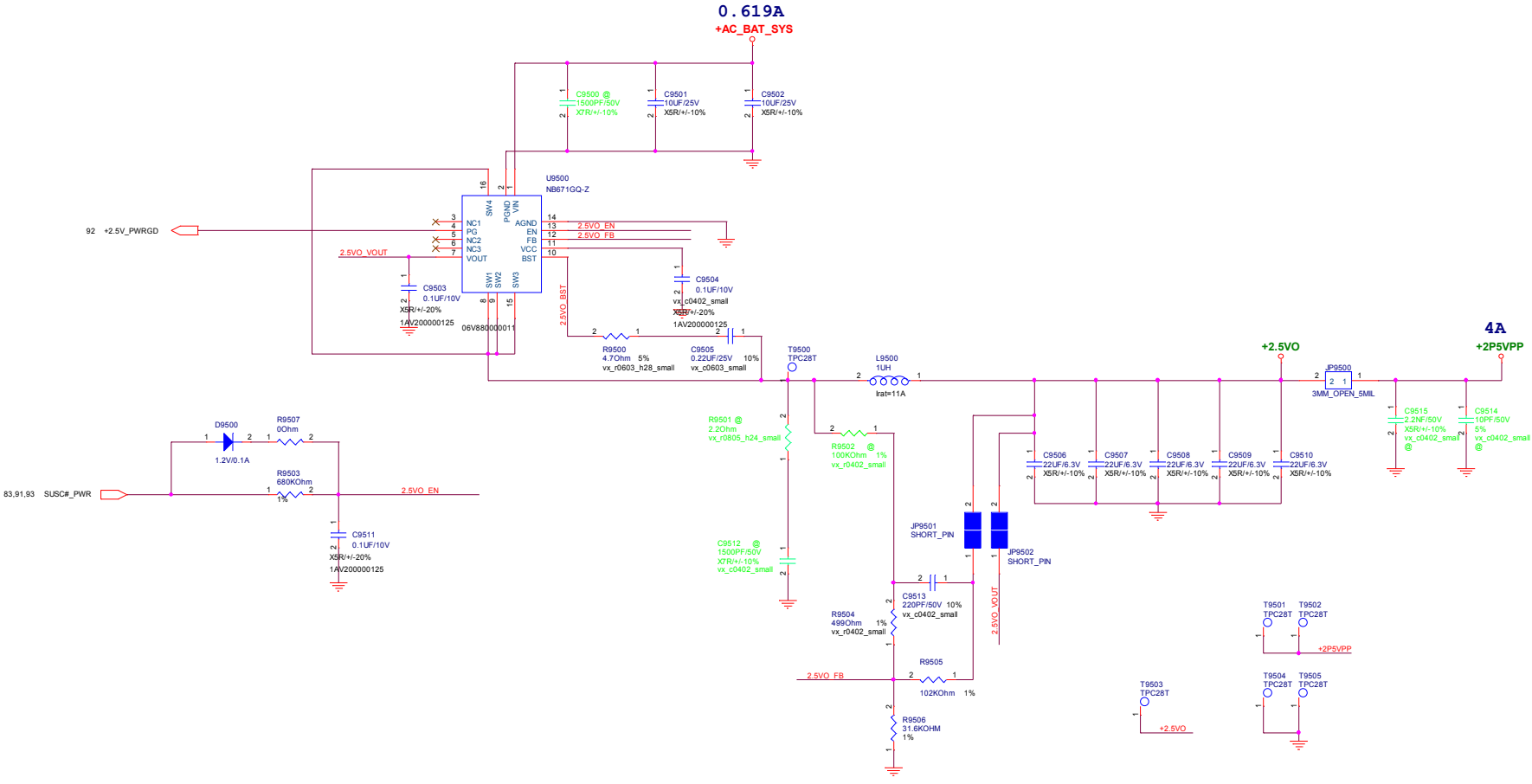


PEGATRON	Title :	USB CHARGE IC	
Pegatron Corp.	Engineer:	Shrek_Tseng	
Size: Custom	Project Name: IPPSL-CD		Rev: A00
Date: Monday, September 07, 2015	Sheet 92 of 108		



PEGATRON	Title :	USB CHARGE IC	
Pegatron Corp.	Engineer:	Shrek_Tseng	
Size: Custom	Project Name: IPPSL-CD		Rev: A00
Date: Monday, September 07, 2015	Sheet 94 of 108		

+2.5V POWER SUPPLY

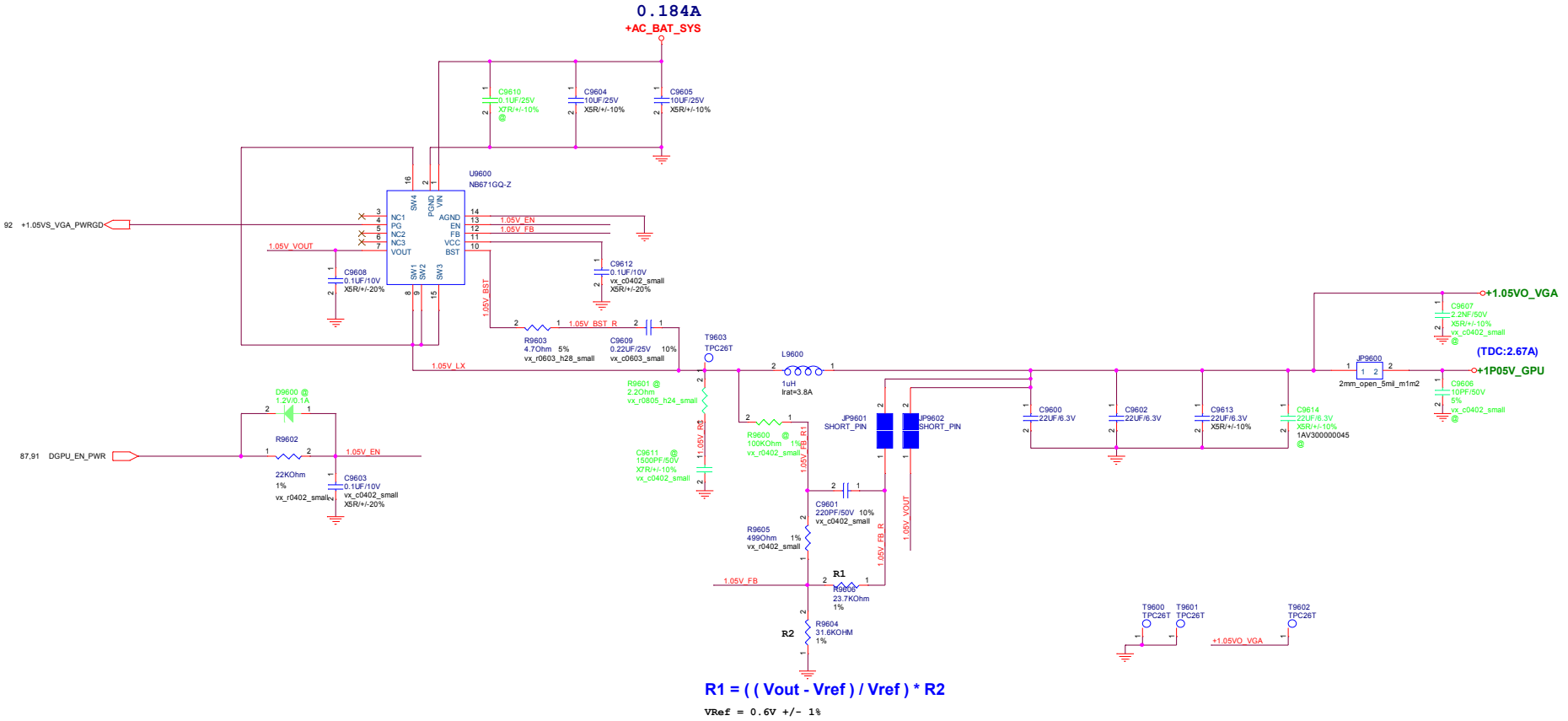


R1 = ((Vout - Vref) / Vref) * R2

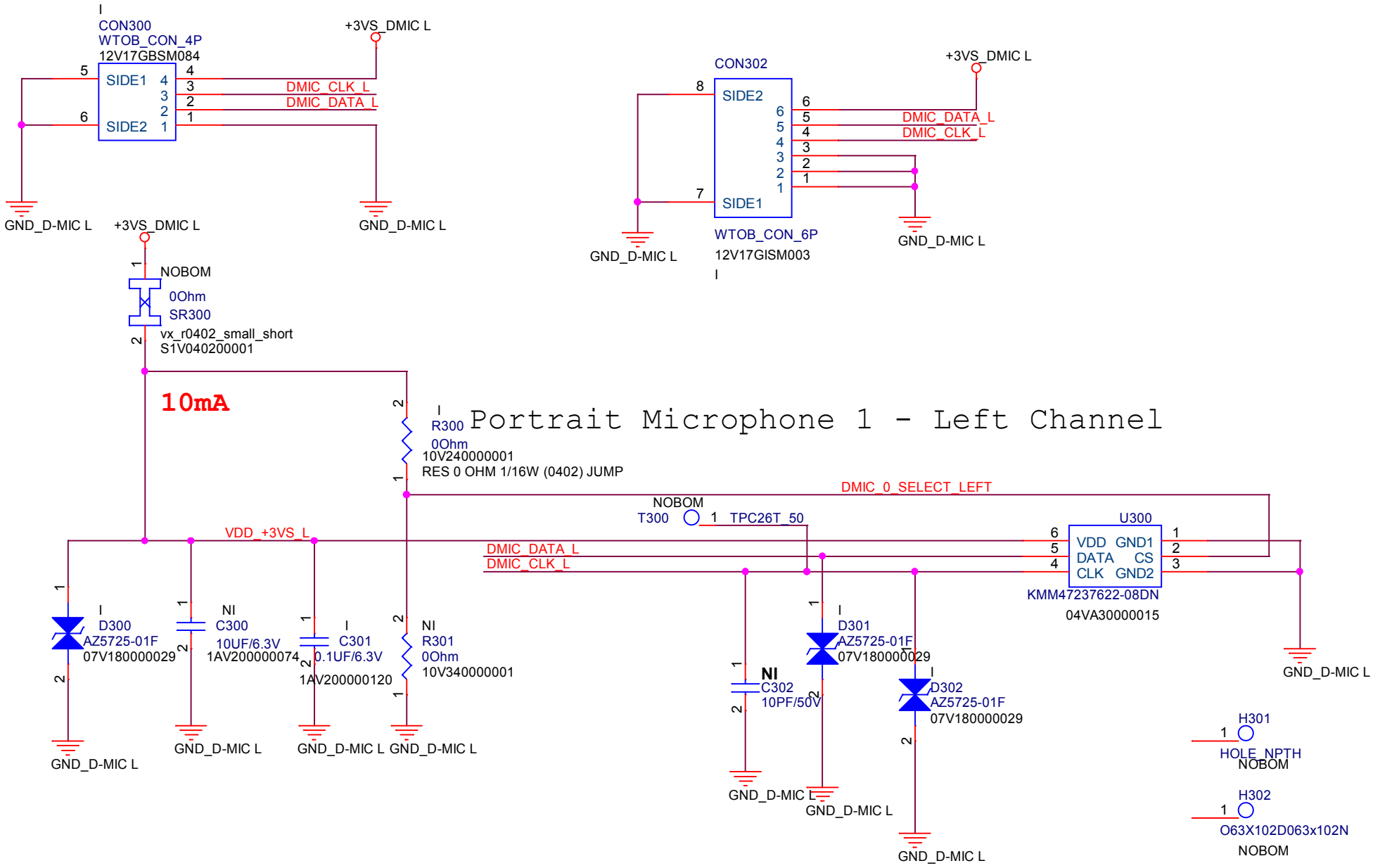
Vref = 0.6V +/- 1%

PEGATRON	Title :	USB CHARGE IC	
Pegatron Corp.	Engineer:	Shrek_Tseng	
Size: Custom	Project Name: IPPSL-CD		Rev: A00
Date: Monday, September 07, 2015	Sheet 95 of 108		

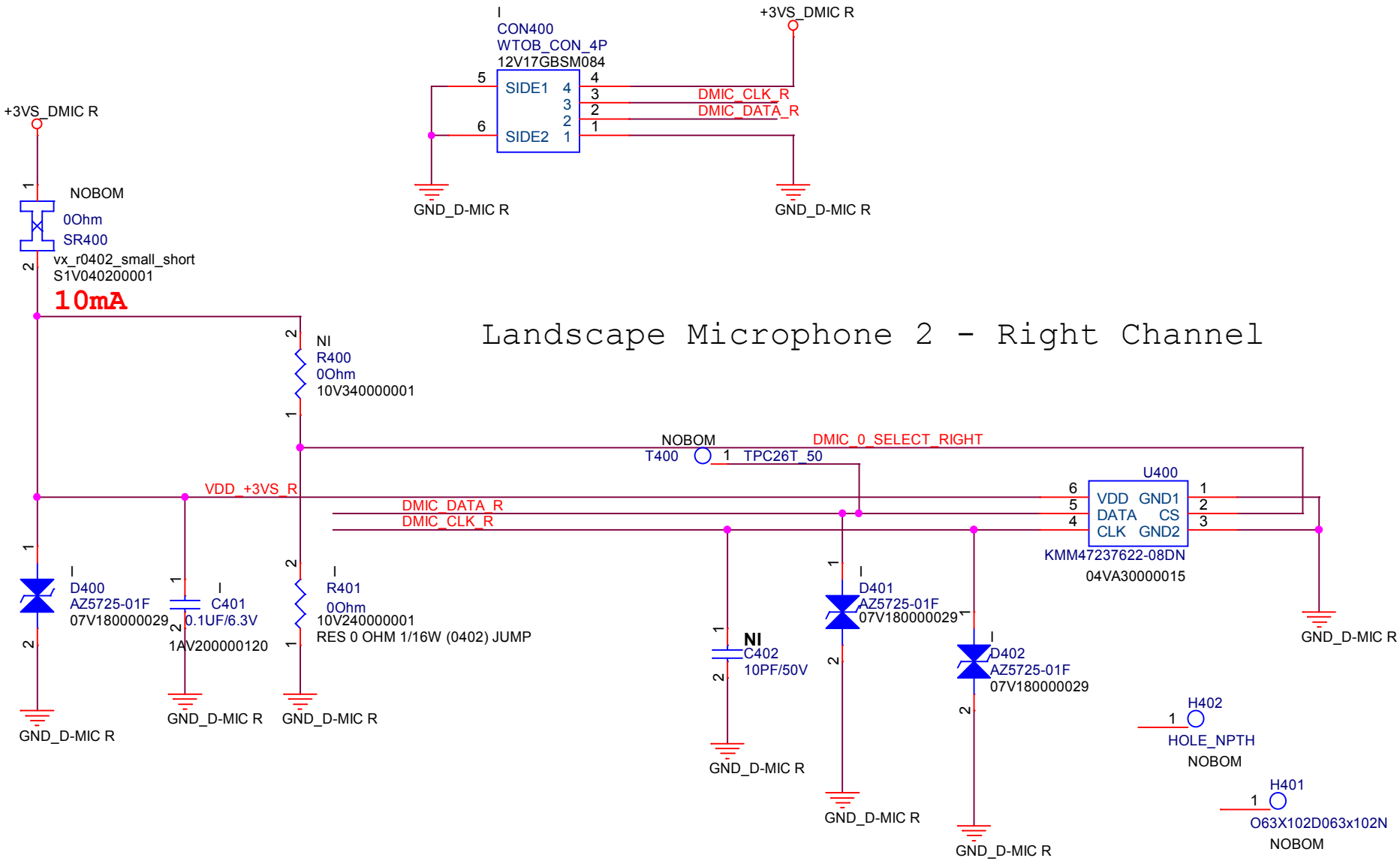
1.05VS_VGA POWER SUPPLY



PEGATRON	Title :	USB CHARGE IC	
Pegatron Corp.	Engineer:	Shrek_Tseng	
Size: Custom	Project Name: IPPSL-CD		Rev: A00
Date: Monday, September 07, 2015	Sheet 96 of 108		

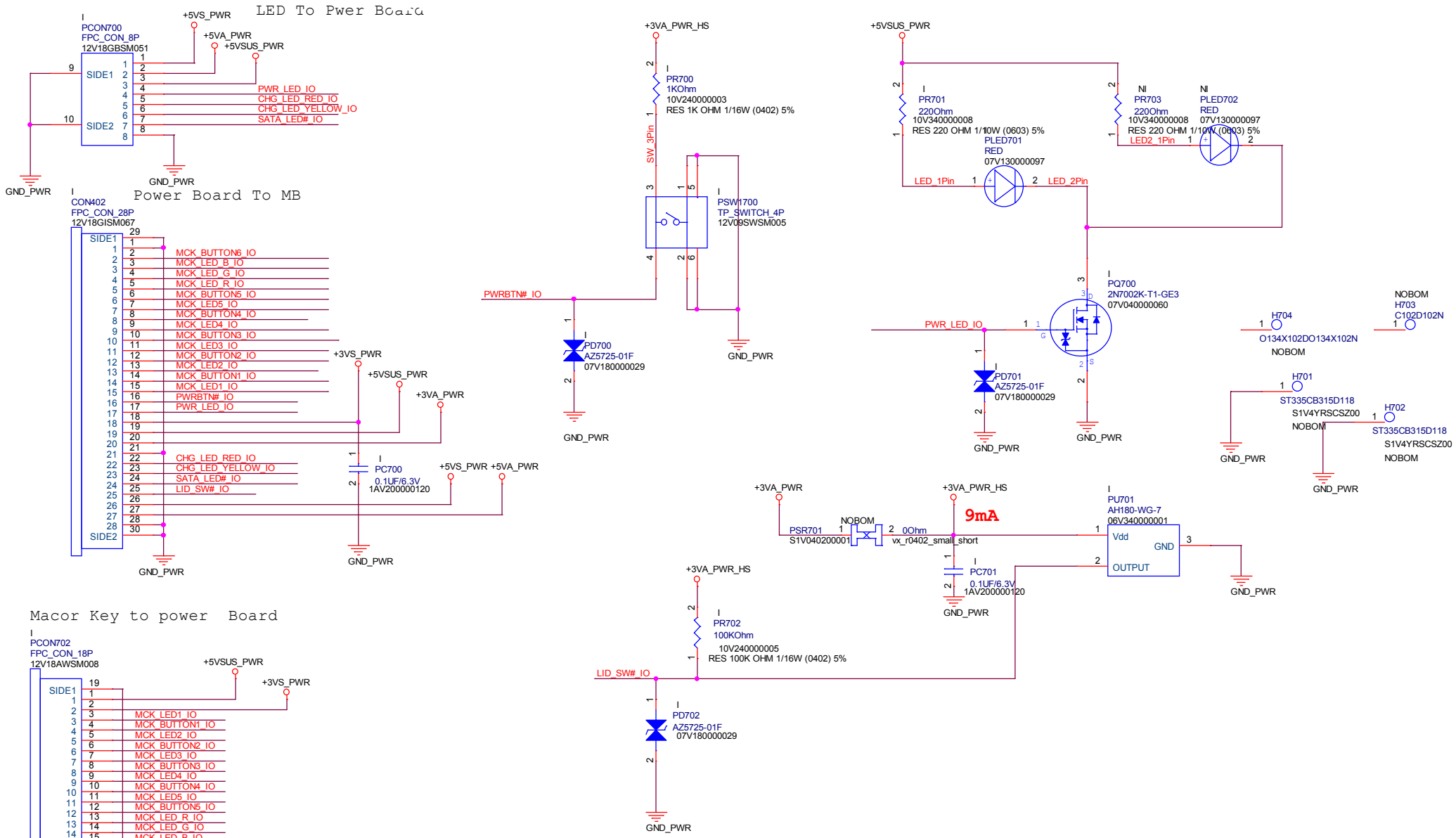

I
CON300
WTOB_CON_4P
12V17GBSM084
SIDE1
SIDE2
+3VS_DMIC L
DMIC_CLK_L
DMIC_DATA_L
GND_D-MIC L
CON302
WTOB_CON_6P
12V17GISM003
NOBOM
0Ohm
SR300
vx_r0402_small_short
S1V040200001
10mA
Portrait Microphone 1 - Left Channel
R300
0Ohm
10V240000001
RES 0 OHM 1/16W (0402) JUMP
DMIC_0_SELECT_LEFT
T300
TPC26T_50
VDD_+3VS_L
U300
VDD GND1
DATA CS
CLK GND2
KMM47237622-08DN
04VA30000015
D300
AZ5725-01F
07V180000029
C300
10UF/6.3V
1AV200000074
C301
0.1UF/6.3V
1AV200000120
R301
0Ohm
10V340000001
D301
D302
C302
10PF/50V
H301
HOLE_NPTH
H302
O63X102D063x102N
<Variant Name>
PEGATRON
Title : D-MIC L BOARD.
Pegatron Corp.
Engineer: Aliens_Hsu
Size A
Project Name IP5NCN/P7NCN DB
Rev A00
Date: Monday, September 07, 2015
Sheet 105 of 108

Landscape Microphone 2 - Right Channel



<Variant Name>

PEGATRON	Title : D-MIC R BOARD.	
Pegatron Corp.	Engineer: Aliens_Hsu	
Size: A	Project Name: IP5NCN/P7NCN DB	Rev: A00
Date: Monday, September 07, 2015	Sheet 106 of 108	



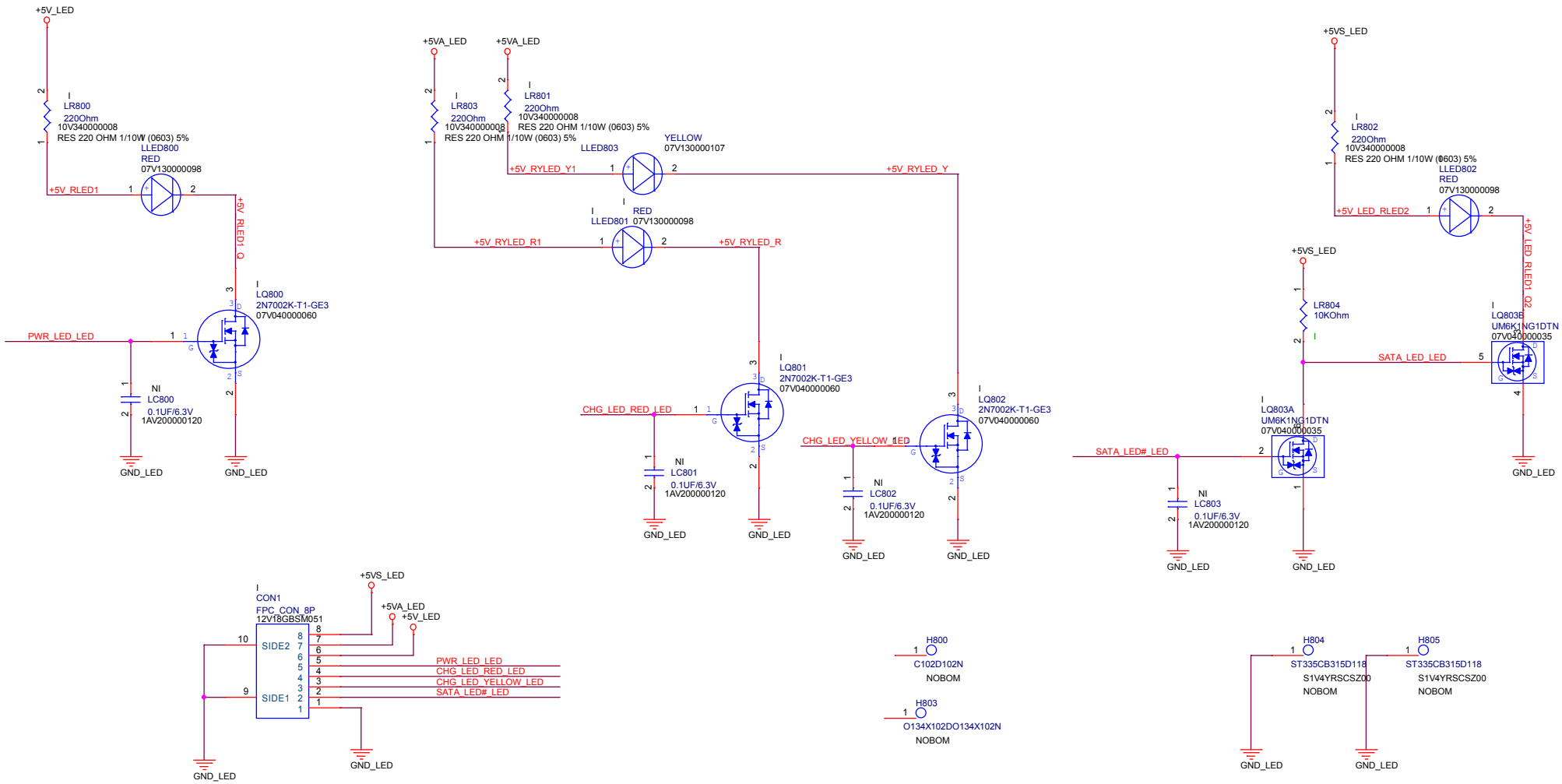
<Variant Name>

PEGATRON Title : POWER BOARD.

Pegatron Corp. Engineer: Aliens_Hsu

Size	Project Name	Rev
B	IP5NCN/P7NCN DB	A00

Date: Monday, September 07, 2015 Sheet 107 of 108



<Variant Name>

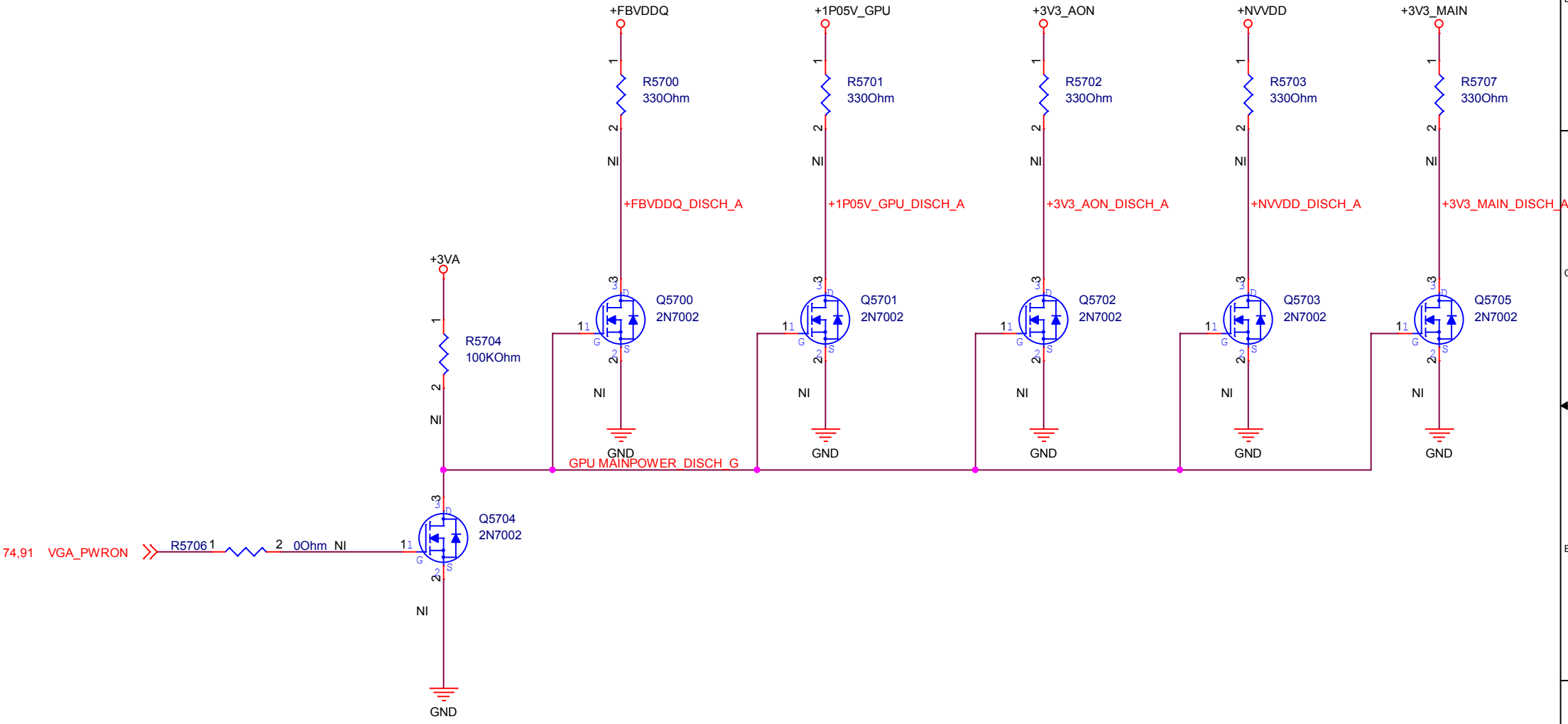
PEGATRON **Title :** LED BOARD.

Pegatron Corp. **Engineer:** *Aliens_Hsu*

Size	Project Name	Rev
A3	IP5NCN/P7NCN DB	A00

Date: Monday, September 07, 2015 Sheet 108 of 108

NV GPU POWER DISCHARGE



PEGATRON DT-MB RESTRICTED SECRET

<Variant Name>

PEGATRON	Title : GPU PWR discharge	
Pegatron Corp.	Engineer: Leon_Lu	
Size: A4	Project Name: P5NCN/P7NCN MAIN BOARD	Rev: A1.0
Date: Monday, September 07, 2015	Sheet 57 of 108	

H31
ST335CB315D118
S1V4YRSCSZ00
NOBOM
GND

H33
ST335CB315D118
S1V4YRSCSZ00
NOBOM
GND

H34
ST335CB315D118
S1V4YRSCSZ00
NOBOM
GND

H36
ST335CB315D118
S1V4YRSCSZ00
NOBOM
GND

H54
CT276B315D118
S1V2YHCCMZ00
NOBOM
GND

H53
CT276B315D118
S1V2YHCCMZ00
NOBOM
GND

H56
CT276B315D118
S1V2YHCCMZ00
NOBOM
GND

H11
RT419X335B335D118
GND

H21
RT335X350CBD118
GND

H32
RT335X315B315D118
GND

H35
RT335X315B315D118
GND

H51
CT276B315D118
S1V2YHCCMZ00
NOBOM
GND

H52
CT276B315D118
S1V2YHCCMZ00
NOBOM
GND

H55
CT276B315D118
S1V2YHCCMZ00
NOBOM
GND

CPU NUT

H61
CT256BD146

H64
CT256BD146

H66
CT256BD146

GND

GPU NUT

H60
CT256BD146

H63
CT256BD146

H65
CT256BD146

GND

U6901
SV-11A1M
GND

U6902
SV-11A1M
GND

H6901
O122X102DO122X102N
NOBOM

H6902
C102D102N
NOBOM

H6903
O122X102DO122X102N
NOBOM

PCH NUT

H68
CT256SB315D146
GND

H69
CT256BD146
GND

H62
CT256BD146
GND

<Variant Name>

~~PEGATRON PT MB RESTRICTED SECRET~~

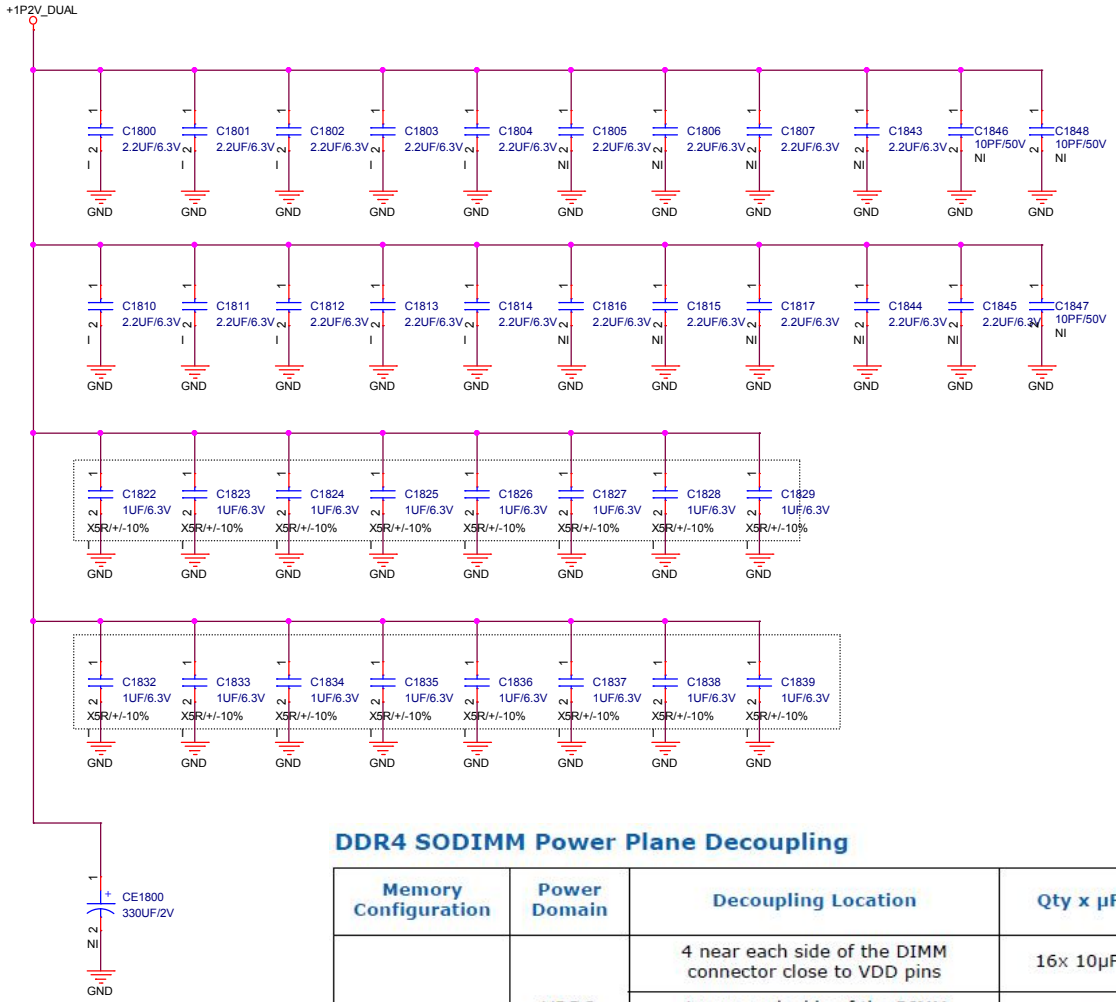
PEGATRON Title : Screw hole

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A4	P5NCN/P7NCN MAIN BOARD	A1.0

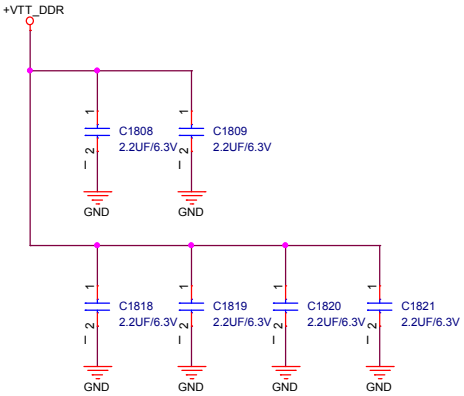
Date: Monday, September 07, 2015 Sheet 69 of 108

Need to check SODIMM DDR4 Termination Cap.



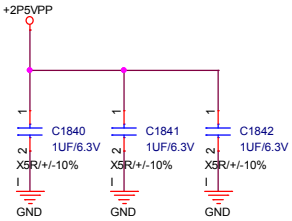
NOTE:
Place those cap close to CH A DIMM

NOTE:
Place those cap close to CH B DIMM



NOTE:
Place those cap close to CH A DIMM

NOTE:
Place those cap close to CH B DIMM



DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM **1DPC**	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Placeholder Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Place these caps on the VTT plane close to SODIMM	4x 1µF (0402)	
	VPP	DRAM Side	2x 10µF (0603)	
		DRAM Side	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	1x 0.1µF (0402)	
		Place close to DIMM	1x 22µF (0402)	

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DDR3 TERMINATION A&B

Pegatron Corp. Engineer: Leon_Lu

Size	Project Name	Rev
A3	P5NCN/P7NCN MAIN BOARD	A1.0

Date: Monday, September 07, 2015 Sheet 18 of 108

Intel Haswell CPU			
	I (max) (A)	TDC (A)	Wattage (W)
+VCORE	85	27	47
+1P35V_DUAL	4.2	2.94	5.67

Intel PCH - Lynx Point HM87			
	I (max) (A)	TDC (A)	Wattage (W)
+3P3V	0.202	0.141	0.67
+3P3VSB	0.293	0.205	0.97
+3VA	0.015	0.011	0.05
+1P5V	0.253	0.177	0.38
+1P05V_PCH	5.921	4.1447	6.22

AMD GPU - SUN-XT (64bit)			
	I (max) (A)	TDC (A)	Wattage (W)
+VDDC (1.125V)	37.5	25	49.19
+VDDCI (0.95V)	9	6	8.55
+3P3V_GPU	0.086	0.06	0.283
+1P8V_MDM	0.53	0.35	0.954
+1P35V_GPU	1.5	1	2.025
+0P95V_GPU	6.03	4.02	5.73

GDDR5 - 2GB			
	I (max) (A)	TDC (A)	Wattage (W)
+1P35V_GPU	5.43	3.8	7.33

SO - DIMM x 2 (DDR3L)			
	I (max) (A)	TDC (A)	Wattage (W)
+1P35V_DUAL	5.12	3.584	6.912
+VTT_DDR	1.43	1	0.97

Scalar - MSTAR TSUMU88BDC2-1			
	I (max) (A)	TDC (A)	Wattage (W)
+3P3V	0.5	0.35	1.65
+1P26V	0.5	0.35	0.6

LCM - Realtek RTL8151GD			
	I (max) (A)	TDC (A)	Wattage (W)
+3P3VSB	0.1	0.07	0.33

Audio - Realtek ALC3661-CG			
	I (max) (A)	TDC (A)	Wattage (W)
+3P3V	0.071	0.05	0.236
+5VSB	0.5	0.35	2.5

Audio AMP - TPA3110D2PWPR			
	I (max) (A)	TDC (A)	Wattage (W)
+19V	0.58	0.404	11.97

SIO - Fintek F71808AU			
	I (max) (A)	TDC (A)	Wattage (W)
+3P3V	0.011	0.008	0.38
+3P3VSB	0.0014	0.001	0.005
+5VA	0.0014	0.001	0.005

Card Reader - Realtek RTS5209-GR			
	I (max) (A)	TDC (A)	Wattage (W)
+3P3V	1.71	1.2	5.66

SATA 3.0 (1-Port for 2.5" HDD)			
	I (max) (A)	TDC (A)	Wattage (W)
+5V	1.57	1.1	7.86

mini_PCIE (Half card)			
	I (max) (A)	TDC (A)	Wattage (W)
+1P5V	0.5	0.375	0.5
+3P3VSB	2.75	1.1	9.075

mini_PCIE (Full card)			
	I (max) (A)	TDC (A)	Wattage (W)
+1P5V	0.5	0.375	0.5
+3P3VSB	2.75	1.1	9.075

USB3.0 (6-Ports)			
	I (max) (A)	TDC (A)	Wattage (W)
+5V_DUAL	5.4	3.78	27

Webcam			
	I (max) (A)	TDC (A)	Wattage (W)
+3P3V	0.323	0.226	1.065

Touch			
	I (max) (A)	TDC (A)	Wattage (W)
+5V_DUAL	1.57	1.1	7.86

HDMI			
	I (max) (A)	TDC (A)	Wattage (W)
+5V	0.055	0.039	0.275

FAN			
	I (max) (A)	TDC (A)	Wattage (W)
+5V	0.5	0.35	2.5

SPI			
	I (max) (A)	TDC (A)	Wattage (W)
+3P3V	0.03	0.03	0.099

PANEL			
	I (max) (A)	TDC (A)	Wattage (W)
+19V_BL	2.1	1.47	39.9
+5V_LCD	1.1	0.8	0.5

PEGATRON Title : POWER DISTRIBUTION

Pegatron Corp. Engineer: Stanley_Chang

Size: A3 Project Name: IMPLP-MS

Date: Monday, September 07, 2015 Sheet: 100

Schematics Change History

Version	Date	Description	Comments
1.00			