G3AE 15" N17E-G1 Max-Q INTEL CFL-H SYSTEM DIAGRAM

01

Charger
DDR4
CPU Core
+1.0V/+1.2VSUS
+3V/+5V S5
+VGACORE
FBVDDQ
1V8_MAIN/PEX_VDD

SODIMM1 Max. 8GB STD — DDR4 2400MHz — Channel A
SODIMM2 Max. 8GB RVS — DDR4 2400MHz — Channel B

INTEL
Coffee Lake - H6+2
Processor : Quad Core
Power : 45 (Watt)
Package : BGA1440
Size : 42 x 28 (mm)
Die Size : 13.6 x 9.1 (mm)

PEG X16 Lanes
15.6" R17M-P1-70, 40W TDP
15.6" R17P-G0/G1, 40W/50W TDP
15.6" N17E-G1, 60W TDP
17.3" N17P-G0/G1, 40W/50W TDP
17.3" N17E-G1/G2, 78W/115W TDP
17.3" R17M-E1-90, 85W TDP
R17M-P1-70, N17P-G0/G1 gDDR5 x4pcs , 3GHz
N17E-G1,gDDR5 x6pcs, 4GHz
R17M-E1-90, N17E-G2 gDDR5 x8pcs, 4GHz

eDP — G-sync FreeSync — LCD
eDP — Optimus MuxIss
DP — PS8409/PS8209 re-driver IC — HDMI2.0
DP — PI3DPX1203ZHEX re-driver IC — mini display port
DP — Optimus MuxIss

DMI

M.2 2280-S3 SSD — SATA 6GB/s (SATA0A) / PCIEx4 32GB/s (LANE9,10,11,12)
HDD — SATA 6GB/s (SATA1B)
ODD For 17.3" — SATA

INTEL PCH
CNL
Power : Watt
Package : FCBGA837
Size : 23 x 23 (mm)

G-sync FreeSync
PS8330BQFN48GTR-A0 re-driver IC — For N17E-G1/G2 abd R17M-E1-90
PCIE 4 Lanes (LANE1-4) — Thunderbolt Intel Alpine Ridge (SP) — USB type C PD CCG4 — PW SW TPS2592 — USB-C Conn

USB 3.0 — PORT1 / PORT2 / PORT3
USB 3.0 Port (MB)
PTN36242LBS re-driver
USB3/DP MUX — N17P-G0/G1 / R17M-P1-70
USB 3.0 Ports (DB)
USB 3.0 Ports (DB)
CAM
IR CAM
Charger TPS2546

USB 2.0 — PORT1 / PORT2 / PORT3 / PORT6 / PORT5

PCI-E x 1 Gen1 — PORT7
LANE5 — LAN RTL8118ASH-CG 10/100/1G — RJ45 Conn
LANE7 — Card Reader RTS5237S-GRT — SD Conn
LANE6 — WLAN BT COMBO M.2 2230/1630

SMBus
Touchpad
ROM — SPI
LPC — KBC ITE IT8987E/BX
LPC — TPM SLB9665TT2.0
G-Sensor HP2DC
Keyboard
K/B Backit
FAN

HDA — AUDIO CODEC ALC3258-CG
I2S — SPK AMP ALC1305H — SPK x2
DMIC
MIC Jack
HP AMP HPA0022642RTJR — HP Jack

STACKUP

TOP
GND
IN1
IN2
VCC
GND
IN3
*GND
IN4
IN5
GND
BOT

*For VRAM, Config IN6

Size	PCB	CPU	GPU	VRAM	Display	PCB Type	Thunderbolt	Display	Adapter
15"	PCB1	KBL-H 4+2 35W	R17M-P1-70, 24.5mmX24.5mm, 40W	4 PCS	FreeSync	Type3 / 10L	No	DGPU	150W
	PCB2	KBL-H 4+2 35W	N17P G0/G1,29mm*29mm40W/50W	4 PCS	Optimus	Type3 / 10L	No	IGPU	150W
	PCB3	KBL-H 4+2 35W	N17E G1,29mm*29mm , 60W	6/8 PCS	G-sync	Type3 / 12L	yes	DGPU	150W
17"	PCB4	KBL-H 4+2 35W	N17P G0/G1,29mm*29mm40W/50W	4 PCS	Optimus	Type3 / 10L	No	IGPU	150W (TBD)
	PCB5	KBL-H 4+2 35W	N17E G1/G2,29mm*29mm , 78W/115	6/8 PCS	G-sync	Type3 / 12L	yes	DGPU	230W
	PCB6	KBL-H 4+2 35W	R17M-E1-90 ,40W x 40W ,85W	8 PCS	FreeSync	Type3 / 12L	yes	DGPU	230W

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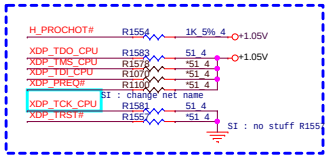
CFL-H Processor (CLK,MISC,JTAG)

02

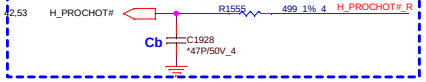
Processor pull-up (CPU)



PROCHOT# (50ohm)

Trace Length <11 inches

Cb need placment near VR



Layout Notes:

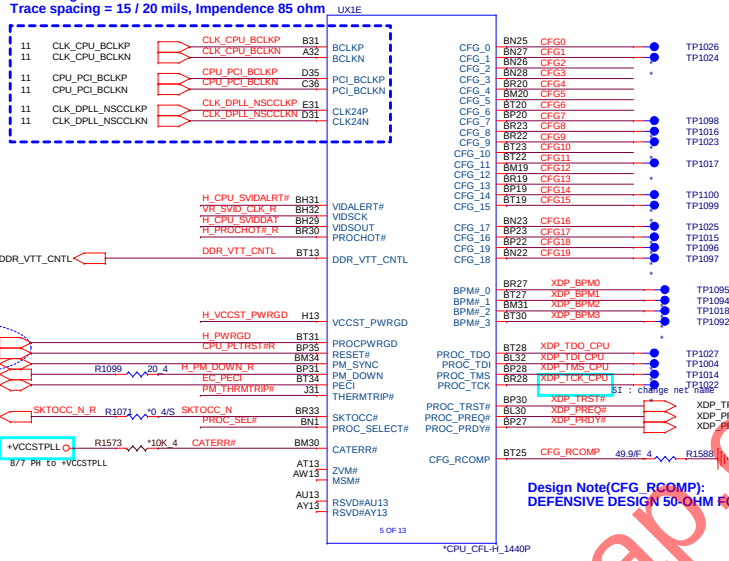
H_PWRGD (50ohm)
Trace Length: 1~11 inches

CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

PM_SYNC (50ohm)
Trace Length: 1~11.25 inches

Host CLK:

Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impendence 85 ohm



*CPU_CFL-H_1440P

Design Note(CFG_RCOMP):
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

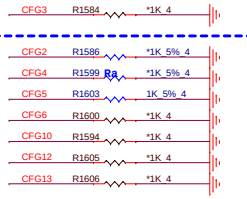
	CFG[4]	Ra
EDP Output from DGPU	Hi	Non Stuff
EDP Output from iGPU	Low	Stuff

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

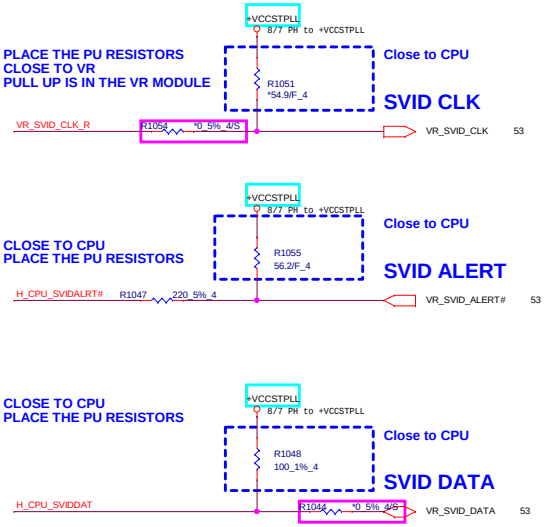
0 Enable; SET DFX ENABLED BIT IN DEBUG

1 , Disable;



CPU CORE SVID

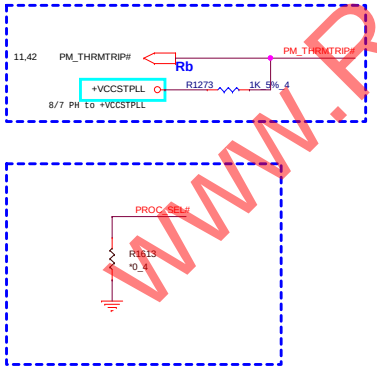
Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.



THERMTRIP# (50ohm)

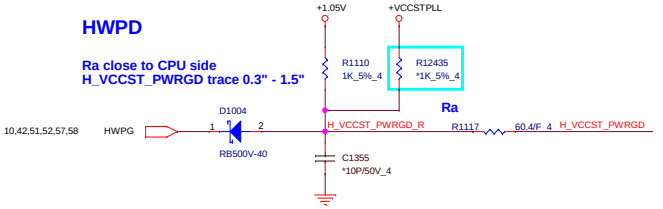
Trace Length: 1.1~12 inches

Rb need placment near PCH



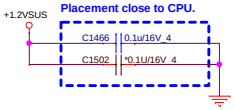
HWPD

Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



CPU VDDQ

Note: please keep plane is enough for VDDQ 2.8A



Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board.

CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a OXM board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asseted x0 = PEG wait for BIOS fro training	

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Custom	CFL 1/7 (JTAG/MISC)	1A
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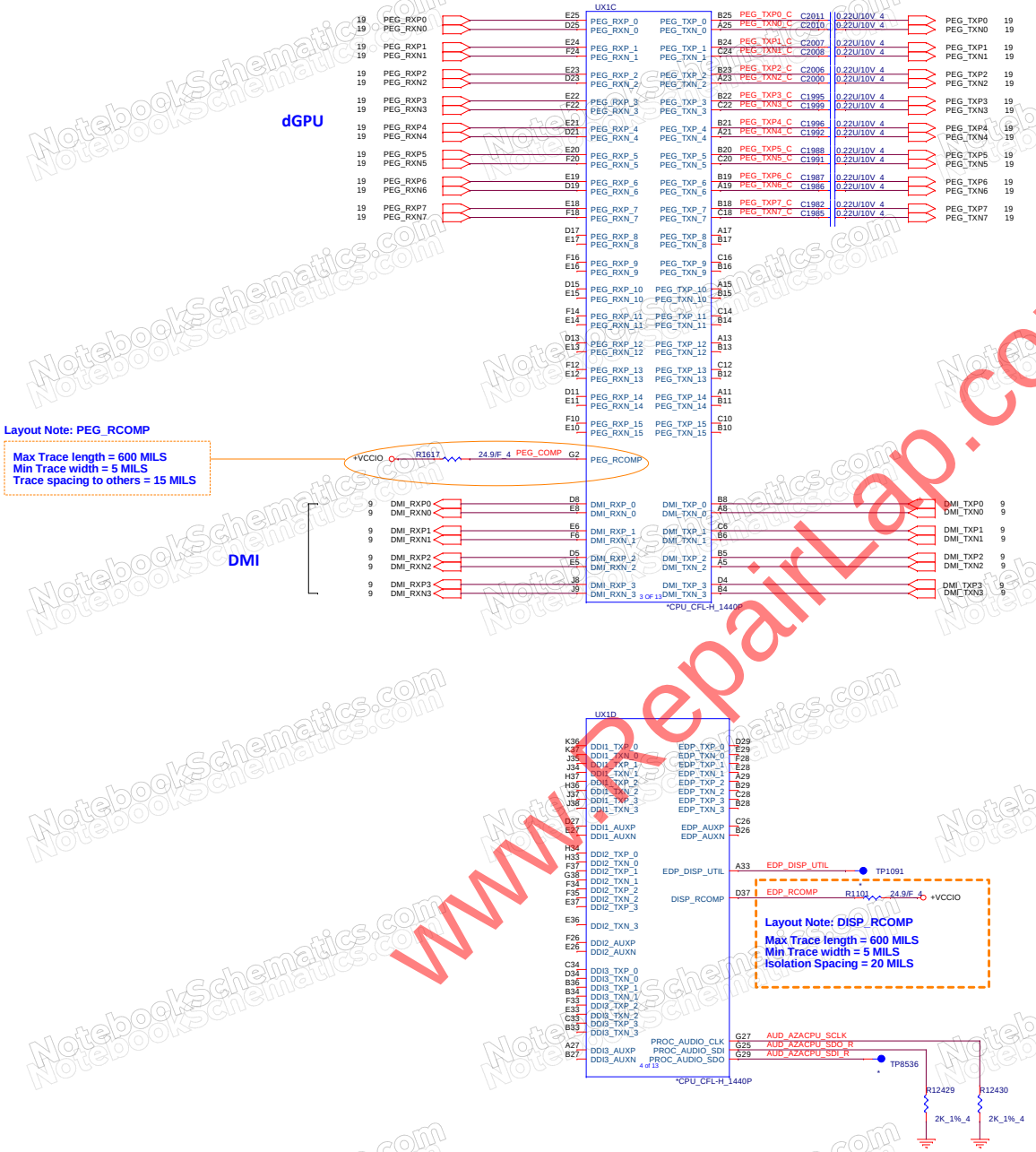
CFL-H Processor (DMI,PEG,FDI)

+1.2VSUS 2,6,10,17,18,52,58,61
+3VS5 10,12,14,29,30,33,34,35,37,42,43,44,45,46,51,52,53,56,57,58
+3V 9,10,11,12,13,14,16,17,18,21,22,28,29,30,31,34,36,37,38,39,40,41,42,46,53,55,56,61,62,63



NB5

PROJECT : G3AE
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Size	Document Number	Rev
Custom	CFL 2/7 (DMI/EDP/PEG)	1A

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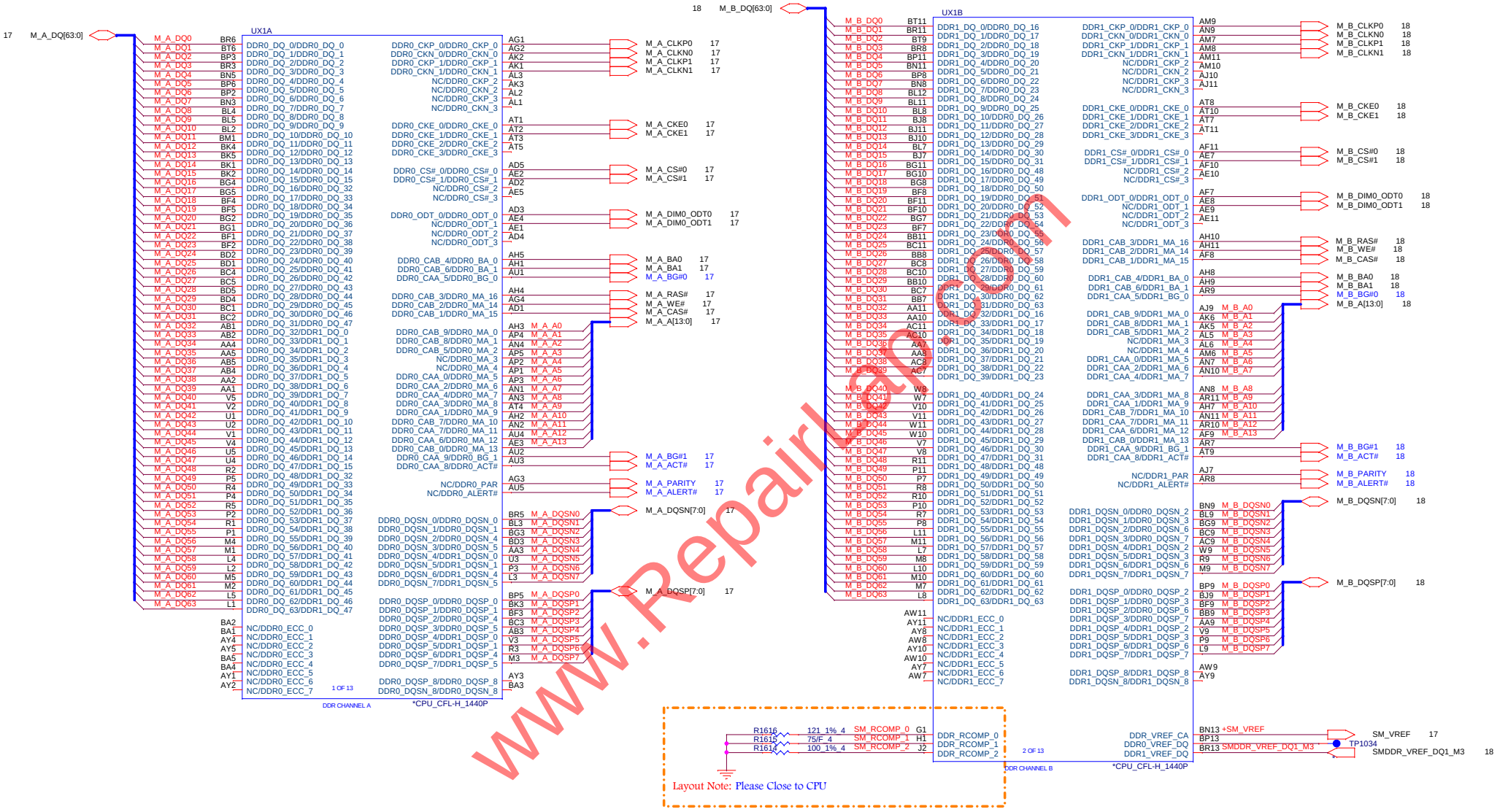
CFL-H Processor (DDR4)



NB5	PROJECT : G3AE Quanta Computer Inc.		
	Size: Custom	Document Number: CFL 3/7 (DDR4 I/F)	Rev: 1A
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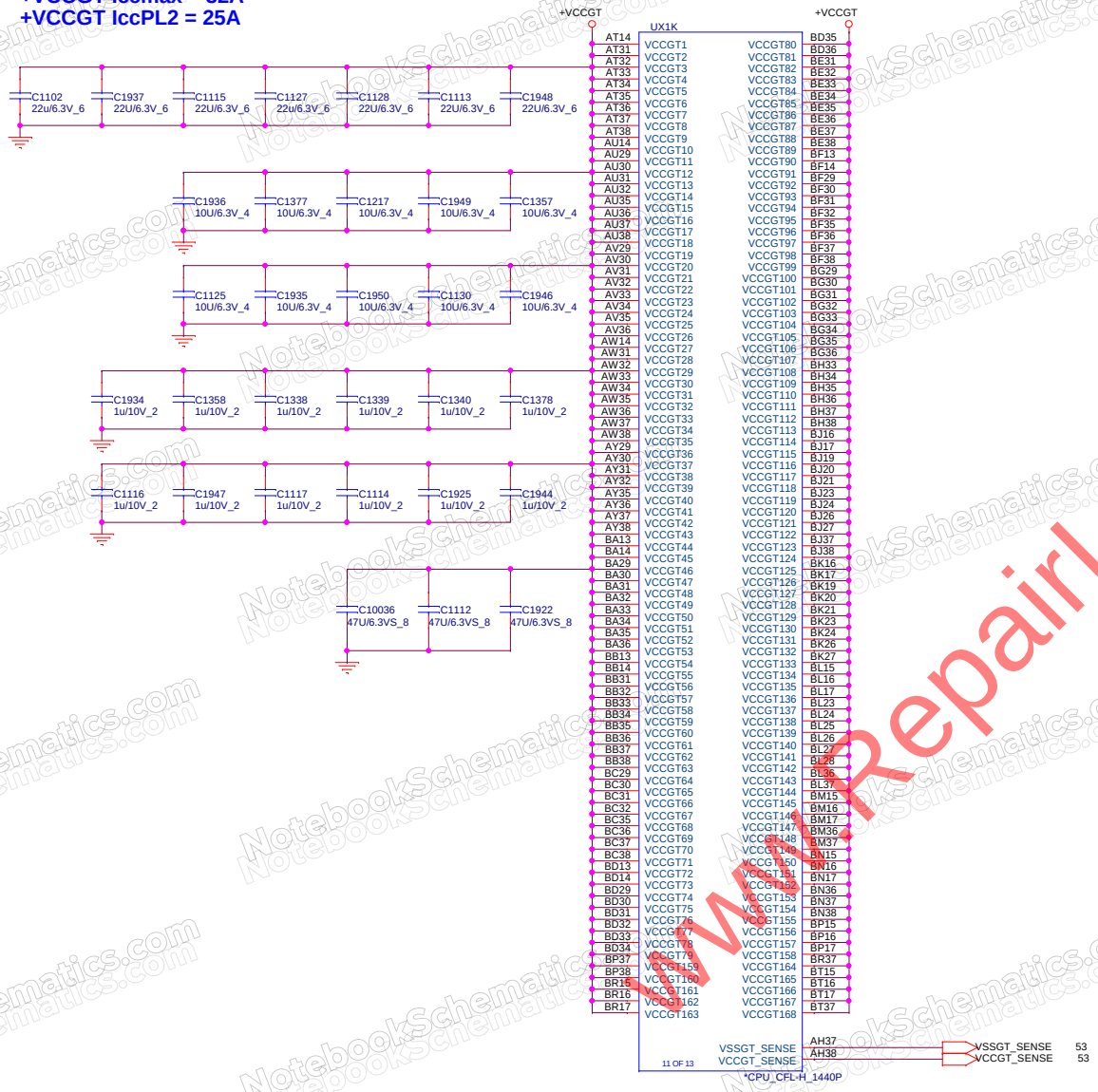
SKYLAKE Processor (POWER)

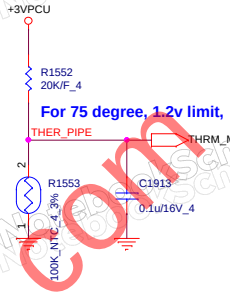
From CFL-H Power Map
+VCCGT Iccmax = 32A
+VCCGT IccPL2 = 25A



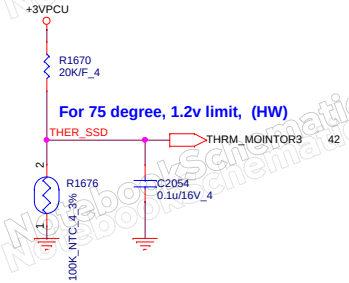
+VCCGT 53,55
+1.2VSUS 2,6,10,17,18,52,58,61

Thermal Protect

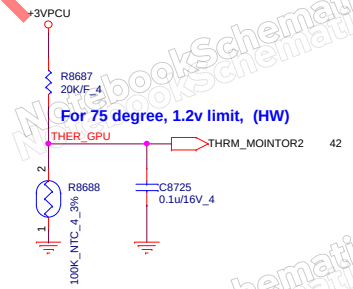
Under CPU pipe for travel bag test



For SSD



GPU VR area to monitor VR/VRAM temp.



NB5	PROJECT : G3AE Quanta Computer Inc.		
Size: Custom	Document Number: CFL 4/7 (POWER)		Rev: 1A
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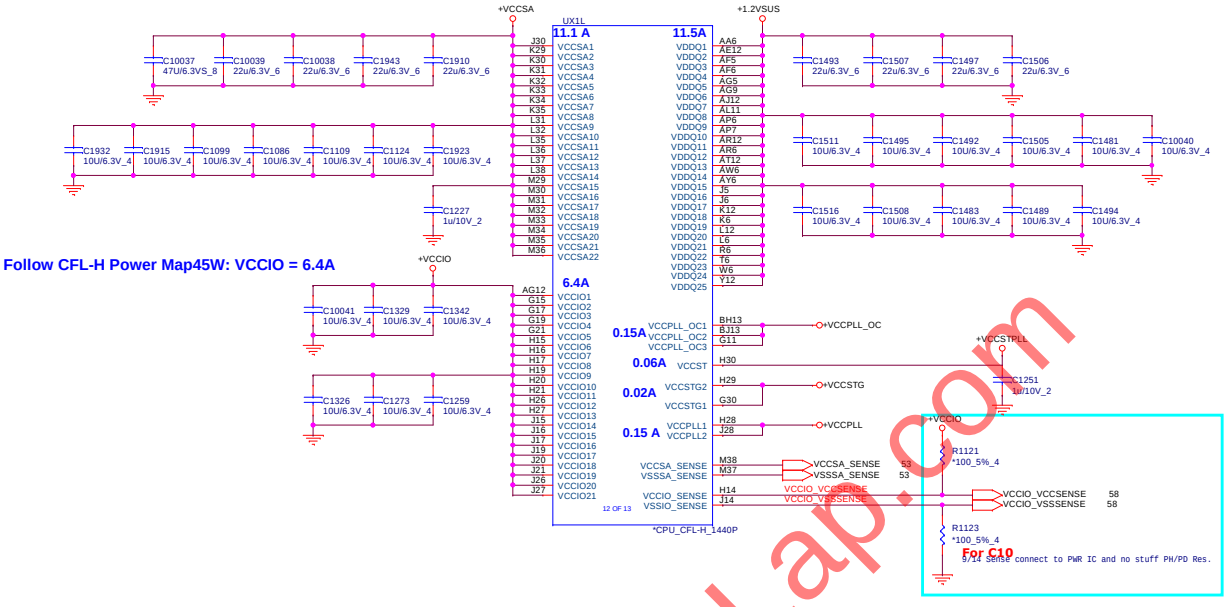
+VCCSA 53,55
+VCCIO 3,58
+1.2VSUS 2,10,17,18,52,58,61

Follow CFL-H Power Map 45W(GT2): VCCSA=11.1A

Follow CFL-H Power Map 45W: VDDQ=11.5A

Follow CFL-H Power Map45W: VCCIO = 6.4A



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Quanta Computer Inc.	
Size: Custom	Document Number: CFL 5/7 (POWER&GND)
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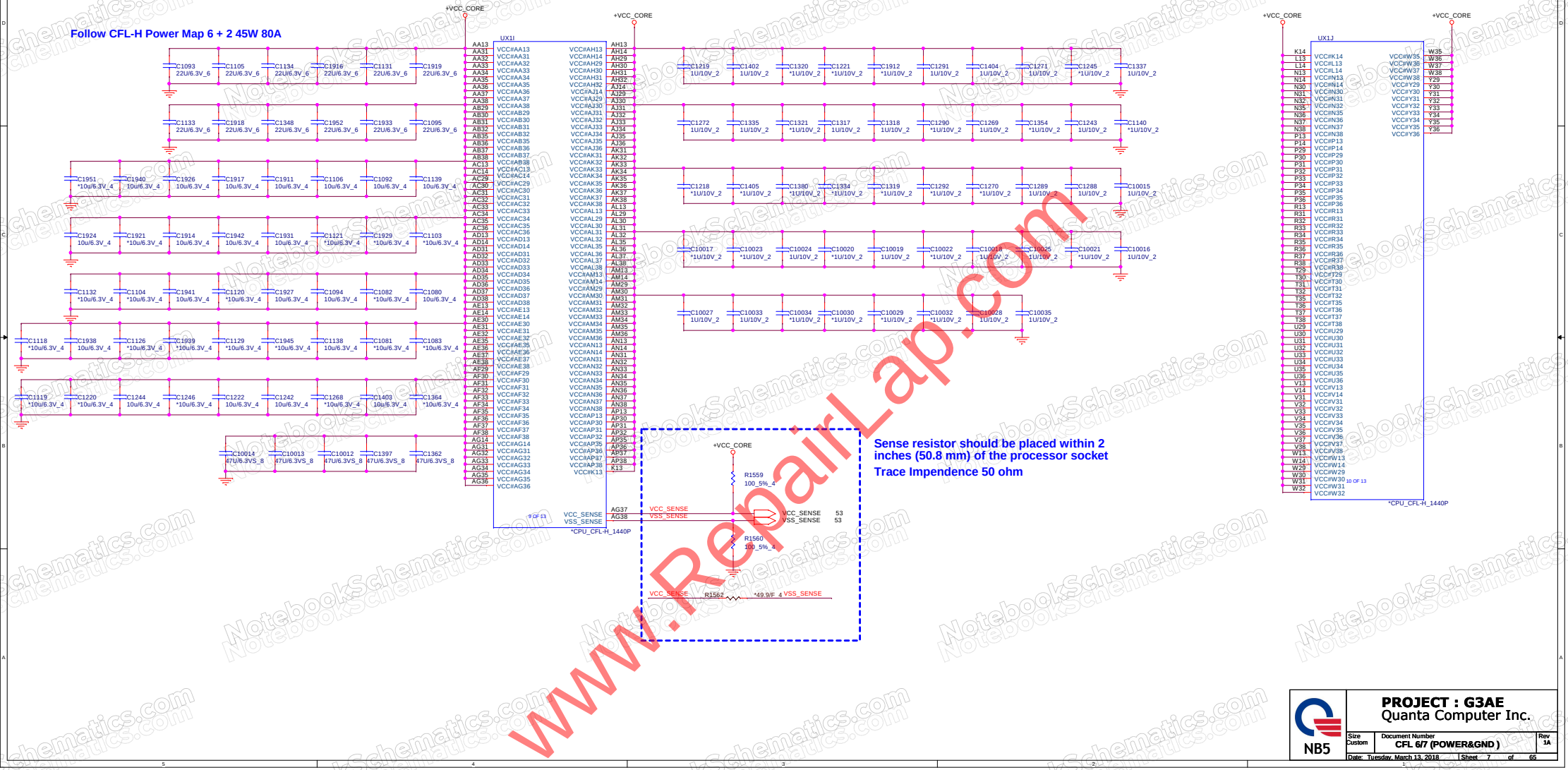
+VCC_CORE 53,54

Follow CFL-H Power Map 6 + 2 45W 80A



NB5	PROJECT : G3AE Quanta Computer Inc.	
Size: Custom	Document Number: CFL 6/7 (POWER&GND)	Rev: 1A
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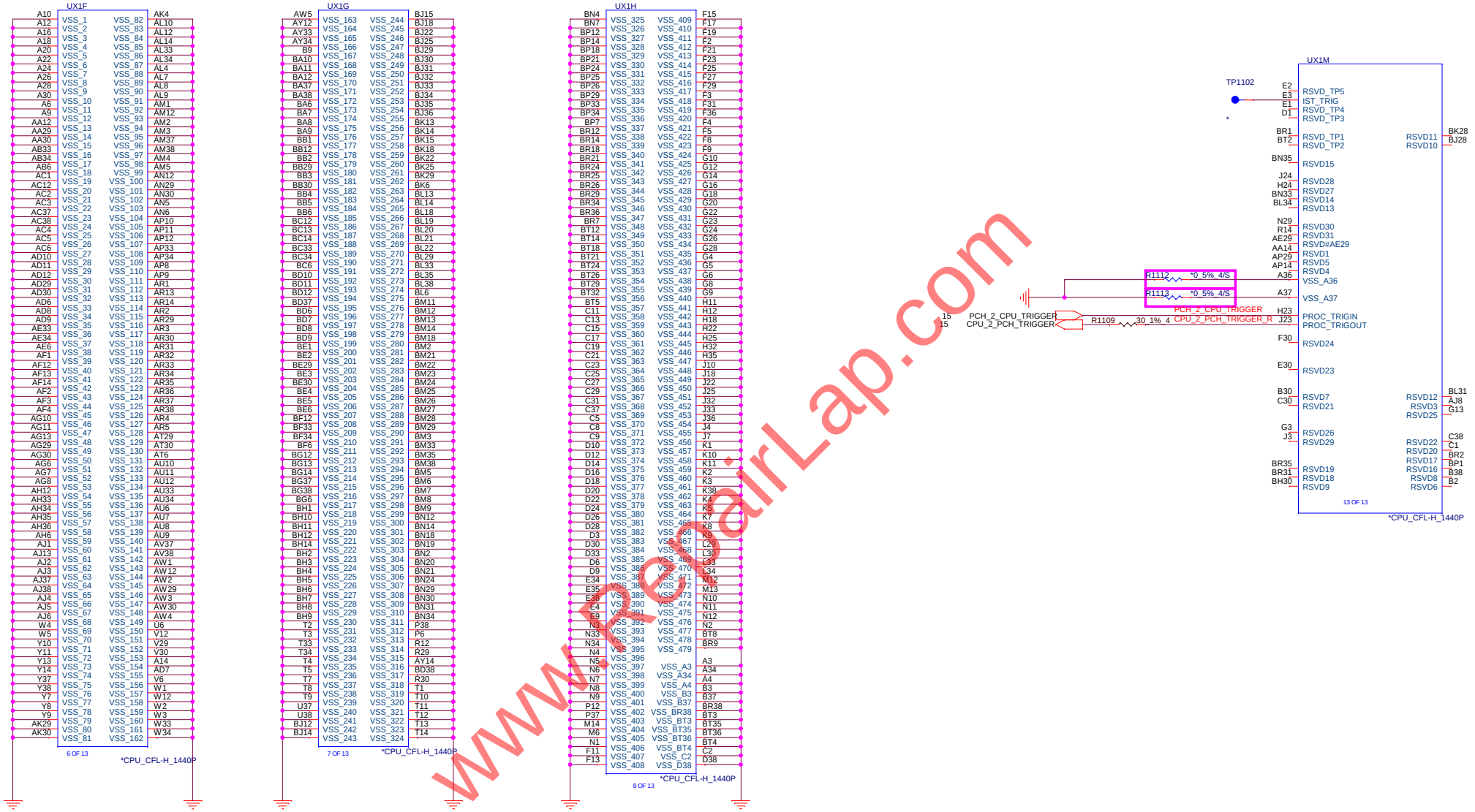

PROJECT : G3AE
Quanta Computer Inc.

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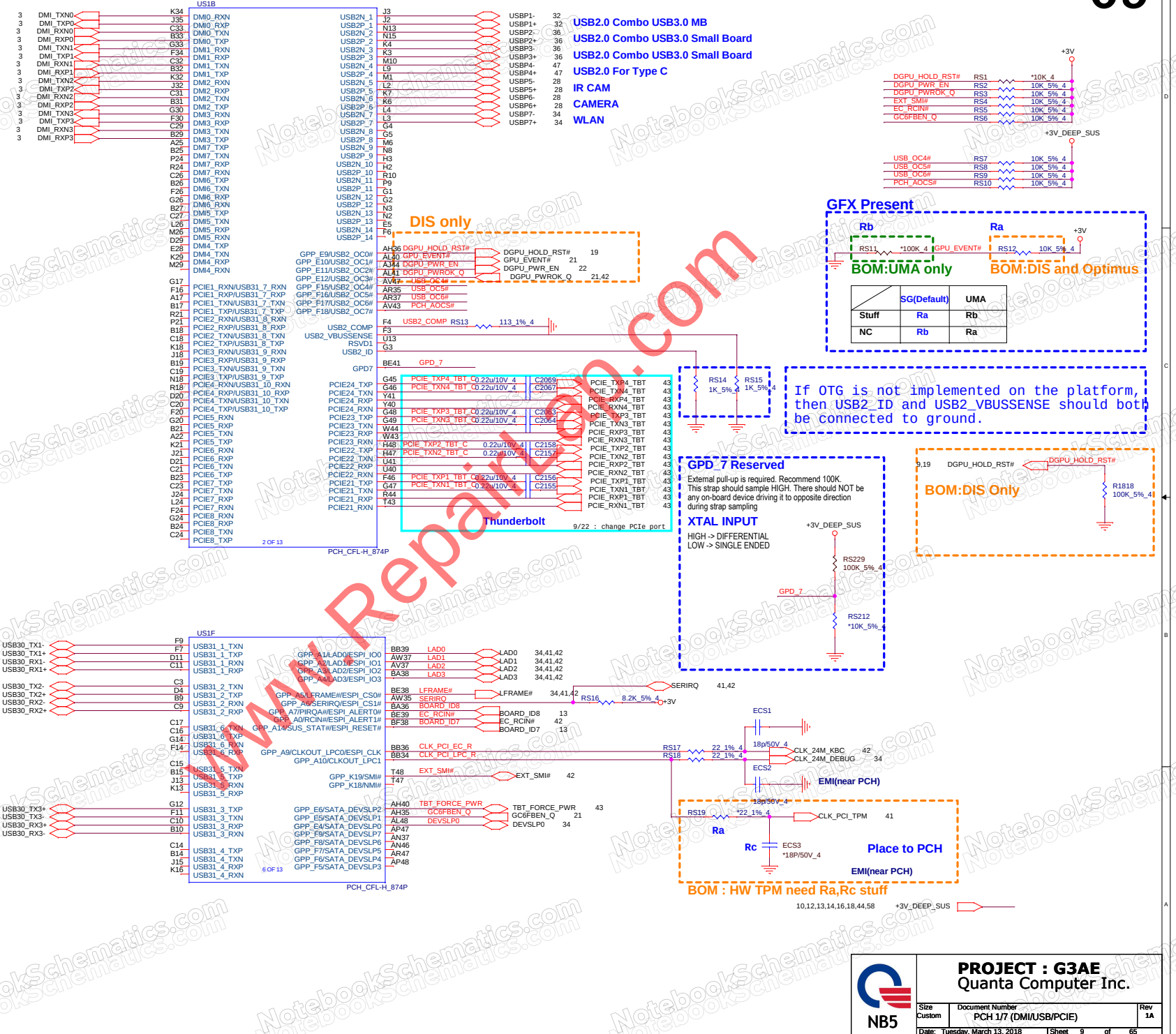
USB 2.0 PORT	
PORT1	USB2 MB
PORT2	USB2 DB-1
PORT3	USB2 DB-2
PORT4	USB2.0 For Type C
PORT5	IR CAM
PORT6	CAMERA
PORT7	WLAN
PORT8	NC
PORT9-14	NC

USB 3.0 PORT	
PORT1	USB3 MB
PORT2	USB3 DB-1
PORT3	USB3 DB-2
PORT4	USB Typec w/o TBT



NB5	PROJECT : G3AE Quanta Computer Inc.		
Size: Custom	Document Number: PCH 1/7 (DMI/USB/PCIE)		Rev: 1A
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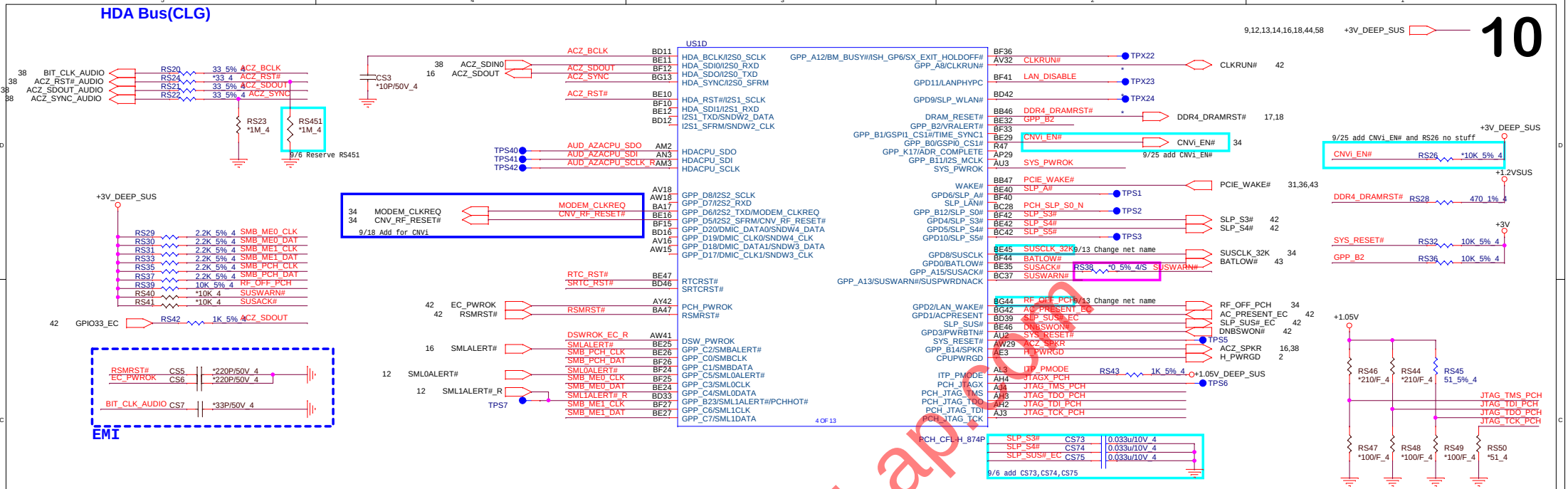
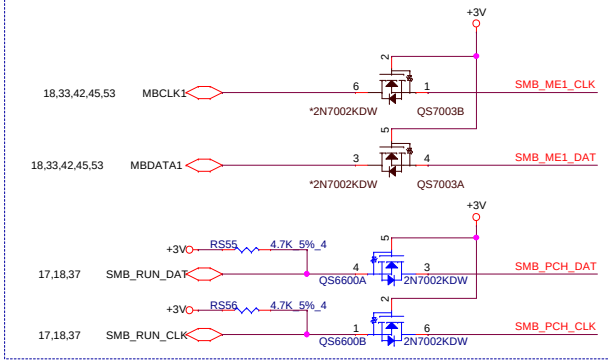
HDA Bus(CLG)



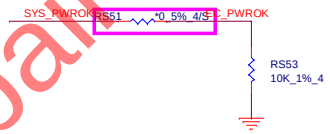
EMI

CPU heat pipe local thermal sensor
GPU thermal sensor
EC

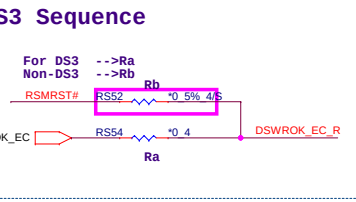


Touch Pad
XDP
DDR4

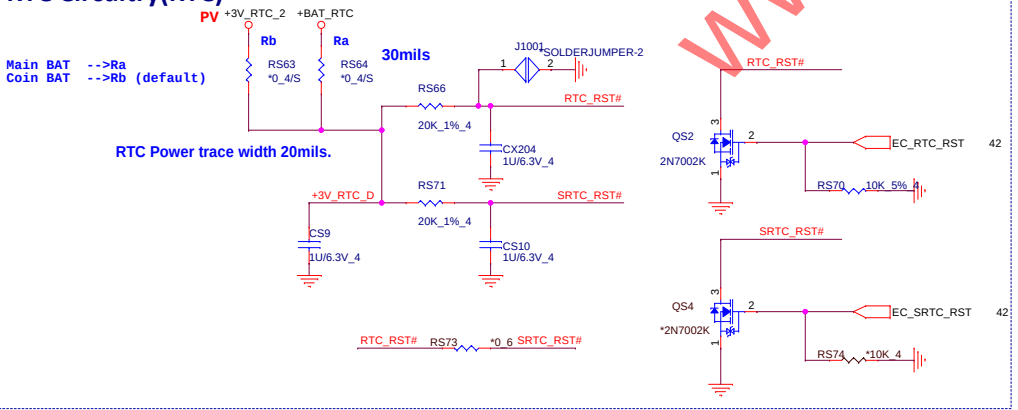
System PWR_OK(CLG)



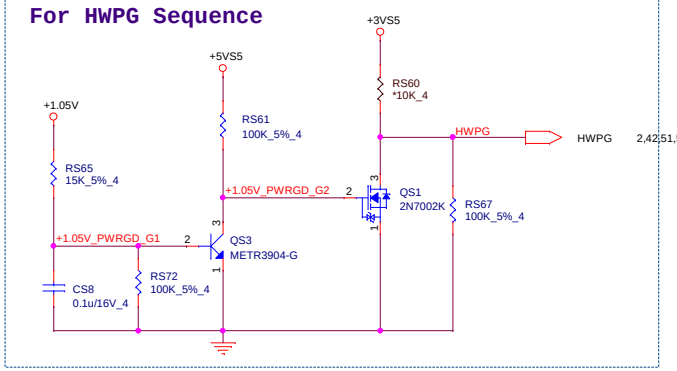
For DS3 Sequence

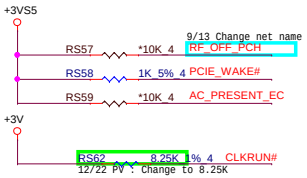


RTC Circuitry(RTC)

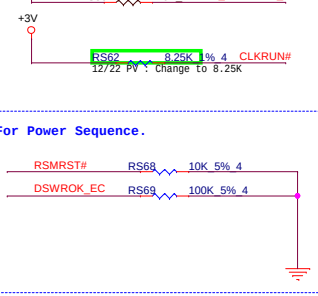


For HWPG Sequence

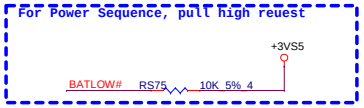




For Power Sequence.



For Power Sequence, pull high reuest



NB5	PROJECT : G3AE Quanta Computer Inc.	
Size: Custom	Document Number: PCH 2/7 (HDA/SMBUS)	Rev: 1A
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HSIO MUX PORT	
PCIE1-4	NC
PCIE5	Lan
PCIE6	Wlan
PCIE7	Cardreader
PCIE8	NC
PCIE9	SSD PCIE * 4
PCIE10	
PCIE11	
PCIE12	
PCIE13	NC
PCIE14	NC
PCIE15	HDD
PCIE16	ODD
PCIE17	NC
PCIE18-20	NC

SSD PCIE x4 LANE

SSD PCIE x4 (SATA0A) LANE

SSD PCIE x4 LANE

WLAN

CardReader

HDD1 (SATA2 6Gb/s)

LAN

9/22 : change PCIe port

9/5 update net name

GPIO35:
SSD SATA IF => High
SSD PCIE IF => Low

For SSD Det (SATA0A)

BOM:SSD only

Please follow Intel CFL-H DG 571391 to meet Layout Requirment "12.3.224 MHz Input Clock Routing Guidelines"

Crystal Components with Surrounding 10 mil Wide GND Shield Trace
Break Out:4-10 mil Wide GND Shield Trace

H_PECI (50ohm)
Trace Length: <0.5 iches
Ra,Ca need placement close to PCH.

RTC Clock 32.768KHz

RS197 RS198 for Debug used.
Please do not change to Short pad

SI : RS86 change to PD 60.4 ohm

BOM:DIS only

BOM:SSD only

Close to PCH

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Quanta Computer Inc.	
Size: Custom	Document Number: PCH 3/7 (SATA/LPC/CLK)
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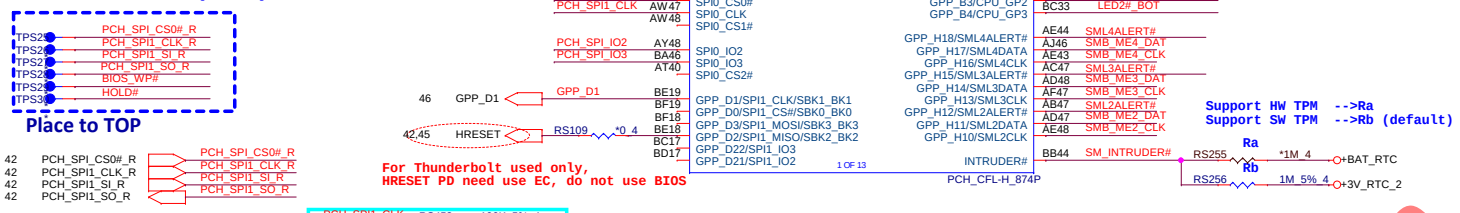
PCH SPI ROM(CLG)



8/22 Update ROM parts list

Vender	Size	P/N
MAX	16MB	AKE3DZN0Z03 (MX25L12873FM2I-10G)
Winbond	16MB	AKE3DF-KN01 (W25Q128JVSIQ)
GigaDevice	16MB	AKE3DZN0Q02 (GD25B127DSIGR)
Socket		DG003000011

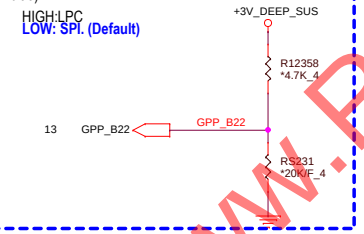
Pin Straps (Sheet 2 of 4)

Signal	Usage	When Sampled	Comment
GPP_B22 / GSPI1_MOSI	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6). Bit 6: 0 = SPI (Default), 1 = LPC. Notes: 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
GPP_C5 / SML0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = LPC is selected (for EC). (Default) 1 = eSPI is selected (for EC). Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. Warning: If this strap is configured to '0' (eSPI is disabled), the eSPI Flash Sharing Mode strap must be configured to '0' as well (SAFS is disabled)
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_H15 / SML3ALERT#	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_B23 / SML1ALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

BOOT SELECT STRAP

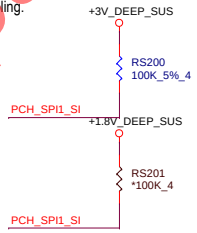
This Signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6).

HIGH:LPC
LOW: SPI. (Default)



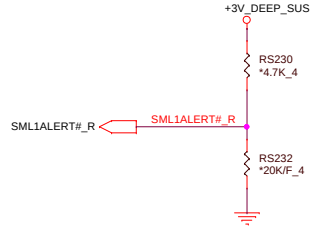
RESERVED

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



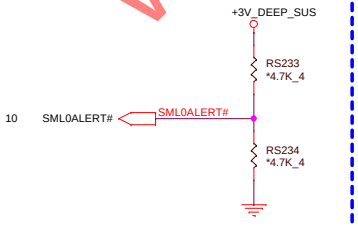
RESERVED

This signal has an internal pull-down.
0 = Disable IntelR DCI-OOB (Default)
1 = Enable IntelR DCI-OOB



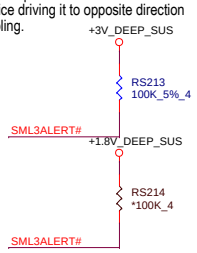
ESPI/LPC SELECT STRAP

HIGH:eSPI Is selected for EC.
LOW: LPC is selected for EC. (Default)



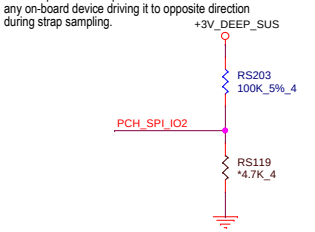
RESERVED

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



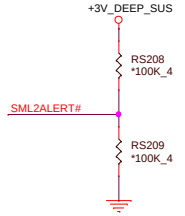
RESERVED

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



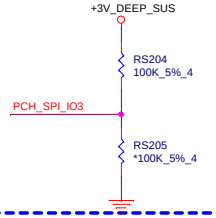
ESPI FLASH SHARING MODE

This signal has a weak internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.



RESERVED

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



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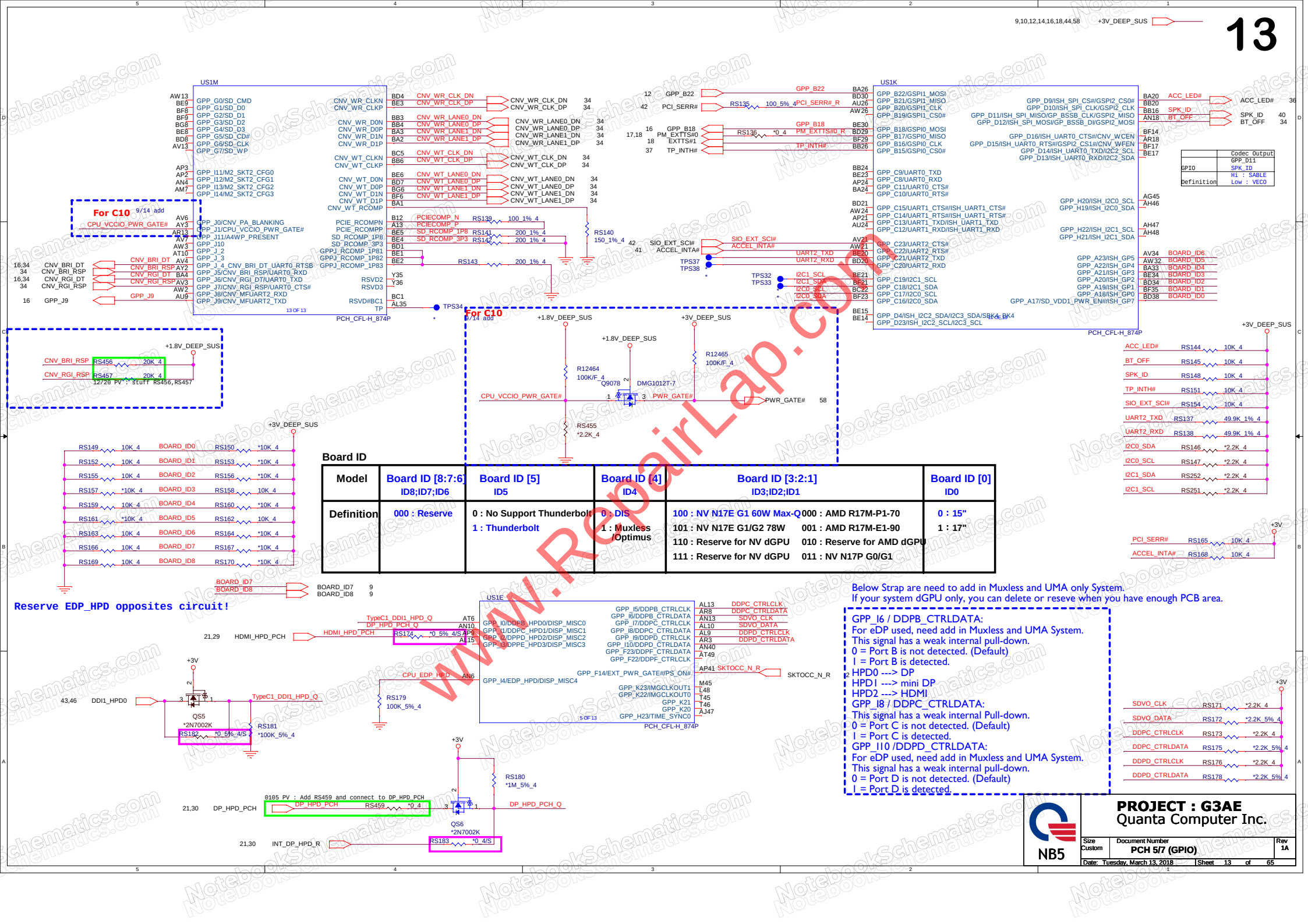

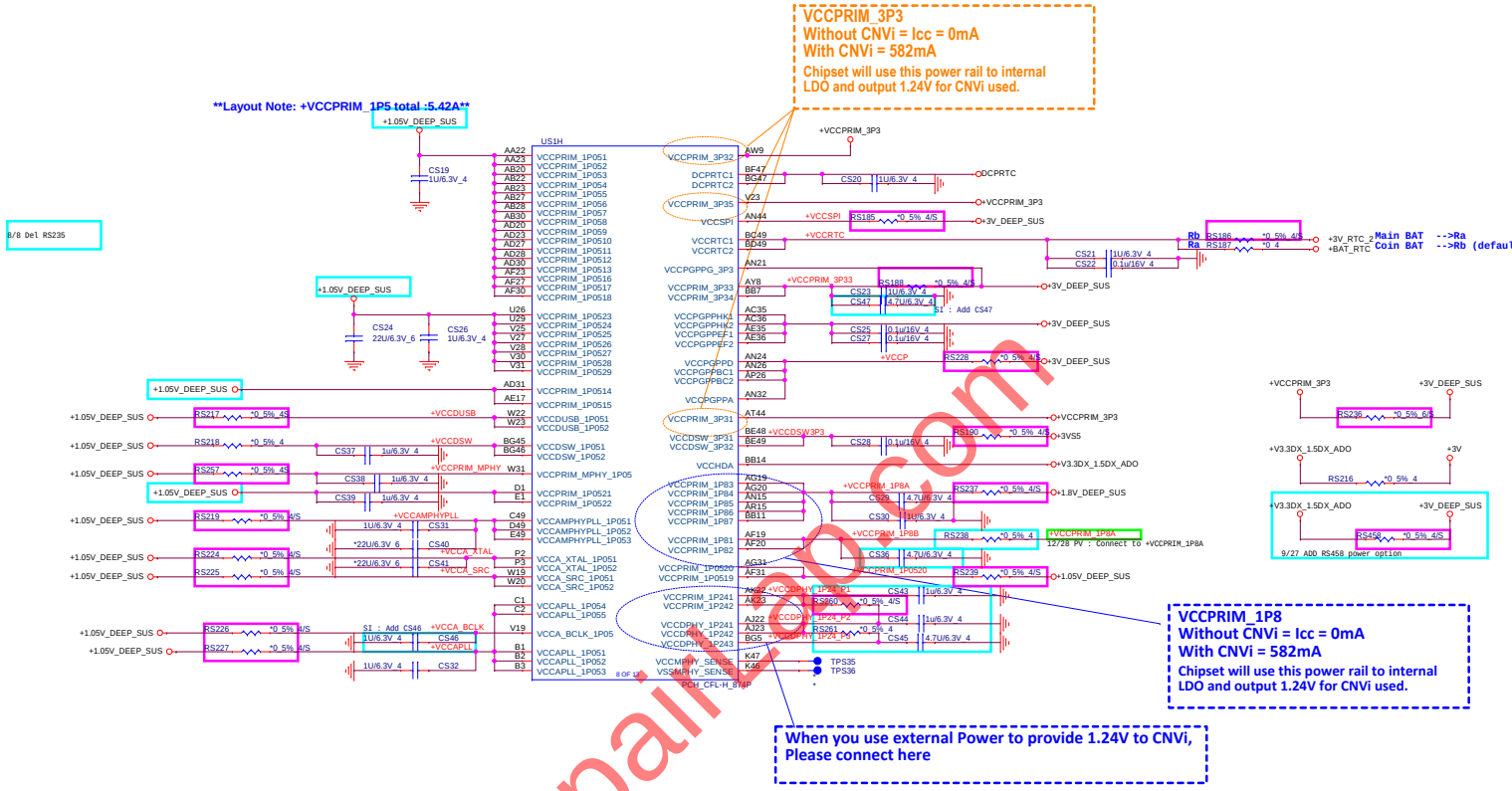

Please follow below table to check Layout

Table 10-4. PCH-H Estimated I_{cc}[3] with Integrated 1.8V VRM Mode OFF (H Mobile SKUs)

Voltage Rail	Voltage (V)	S0 Iccmax Current[2] (A)	Sx Icc Idle Current[4] (mA)	S0ix Icccmax Current (mA)	Deep Sx Icc Idle Current (mA)	G3 (µA)
VCCAPLL_1P05	1.05	0.034	0.2	0.801	0	0
VCCA_BCLK_1P05	1.05	0.007	0.1	0.087	0	0
VCCA_SRC_1P05	1.05	0.141	0.3	0.838	0	0
VCCA_XTAL_1P05	1.05	0.005	0.544	0.195	0	0
VCCAMPHYPLL_1P05	1.05	0.114	0.4	1.192	0	0
VCCPRIM_1P05	1.05	4.174 HSIO Lane Adder refer to Table 10-7 column HALO	40.344	0.477A	0	0
VCCPRIM_MPHY_1P05	1.05	0.088	0.2	1.22	0	0
VCCDSW_1P05	1.05	0.01	0.2	0.001	0.2	0
VCCDUSB_1P05	1.05	0.33	1.288	16.373	0	0
VCCHDA	3.3	0.007	0.1	4.908	0	0
VCCDSW_3P3	3.3	0.094	0.2	0.705	1.05	0
VCCPRIM_3P3	3.3	0.318	0.3	0.916	0	0
VCCPGPPA	3.3	0.085	0.1	0.103	0	0
VCCPGPPBC	3.3	0.286	0.2	0.232	0	0
VCCPGPPD	3.3	0.117	0.1	0.109	0	0
VCCPGPPEF	3.3	0.145	0.2	0.094	0	0
VCCPGPPG_3P3	3.3	0.121	0.1	0.072	0	0
VCCPGPPHK	3.3	0.219	0.2	0.138	0	0
VCCPRIM_1P8	1.8	0.152 CNVI Adder refer to Table 10-8, column HALO	6.607	9.411	0	0
VCCRTC[1]	3.0	0.31mA	0.299	0.075	0.316	6
VCCSPI	3.3	0.042	0.1	0.153	0	0

Notes:
1. The VCC rail ICC data is taken at 3.0V while the system is in a mechanical off (G3) state at room temperature.
2. Iccmax estimates assumes 110 °C.
3. The Iccmax value is a steady state current that can happen after respective power ok has asserted (or reset signal has de-asserted).
4. Sx Icc Idle assumes PCH is idle and ME is power gated.
5. Sx Icc at 3.3V level is assumed. Sx Icc data at the 1.8 V and/or 1.5V level not measured.

9,10,12,13,16,18,44,58 +3V_DEEP_SUS

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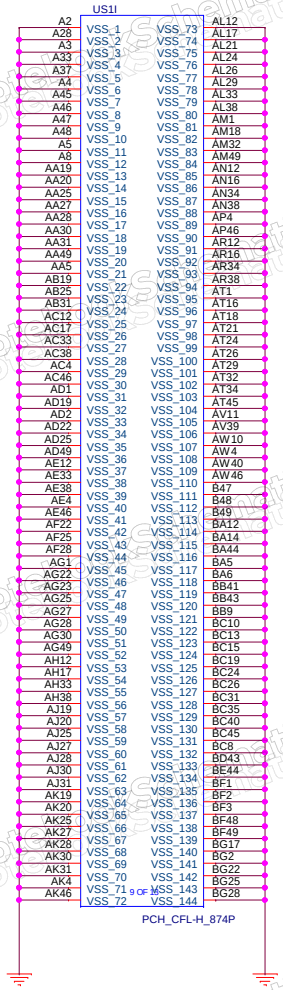

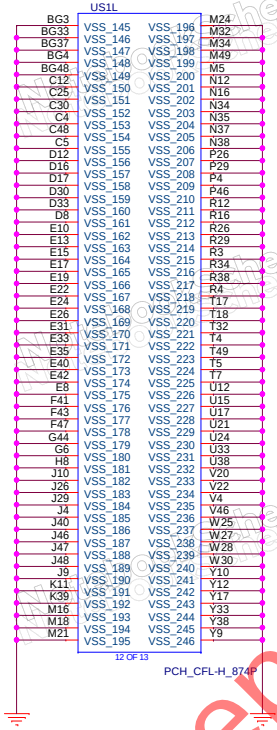

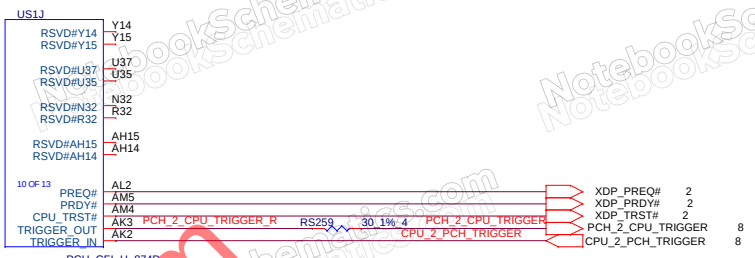

NB5

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Quanta Computer Inc.

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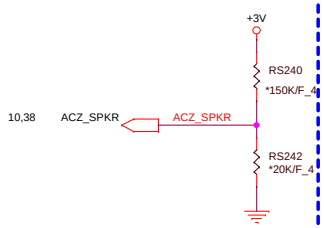
Pin Straps (Sheet 1 of 4)

Signal	Usage	When Sampled	Comment
GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap . ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_C2 / SMBALERT#	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

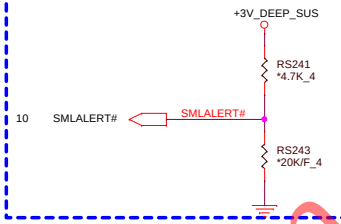
TOP SWAP OVERRIDE STRAP

The signal has a weak internal pull-down.
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode. This inverts an address



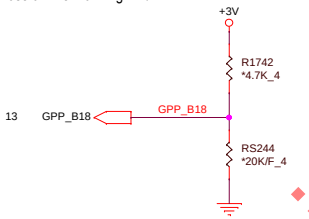
TLS CONFIDENTIALITY ENABLED

This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.

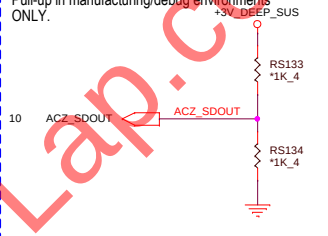


NO REBOOT IF SAMPLED HIGH

The signal has a weak internal pull-down.
0 = Disable "No Reboot" mode. (Default)
1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY.



Pin Straps (Sheet 3 of 4)

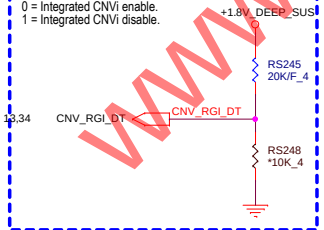
Signal	Usage	When Sampled	Comment
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H12 / SML2ALERT#	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC strap is configured to '0' (eSPI is disabled)**
GPP_I6 / DDPB_CTRLDATA	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_I8 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_I10 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_F23	Display Port F Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port F is not detected. (Default) 1 = Port F is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well. 3. This strap applies to platforms that support Display Port F only. Refer to the platform's processor documentation for info on Display Port F support.

Pin Straps (Sheet 4 of 4)

Signal	Usage	When Sampled	Comment
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
GPP_J9	1.8V VCCPSPI	Rising edge of RSMRST#	The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail ***Note:*** If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os
GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

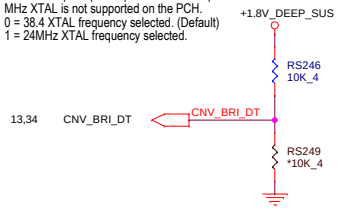
M.2 CNVi Mode Select

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.



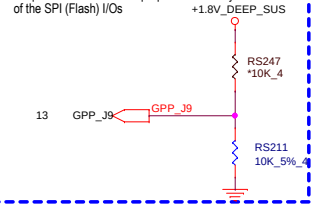
XTAL Frequency Select

This signal has a weak internal pull-down.
An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.
0 = 38.4 XTAL frequency selected. (Default)
1 = 24MHz XTAL frequency selected.



GPP_J9 1.8V VCCPSPI:

The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail
Note: If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os



NB5

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Quanta Computer Inc.

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	APS(NA)	1A
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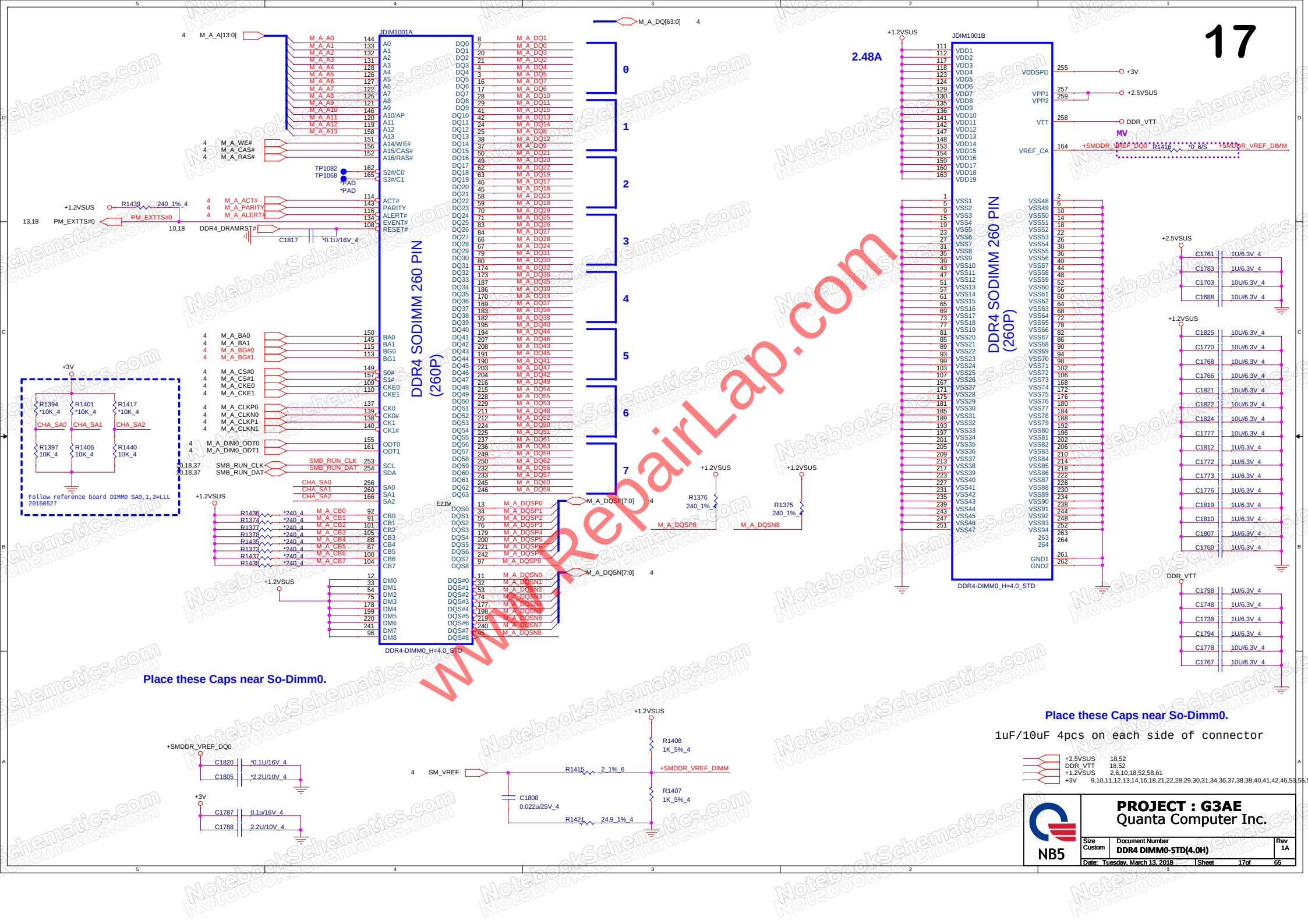

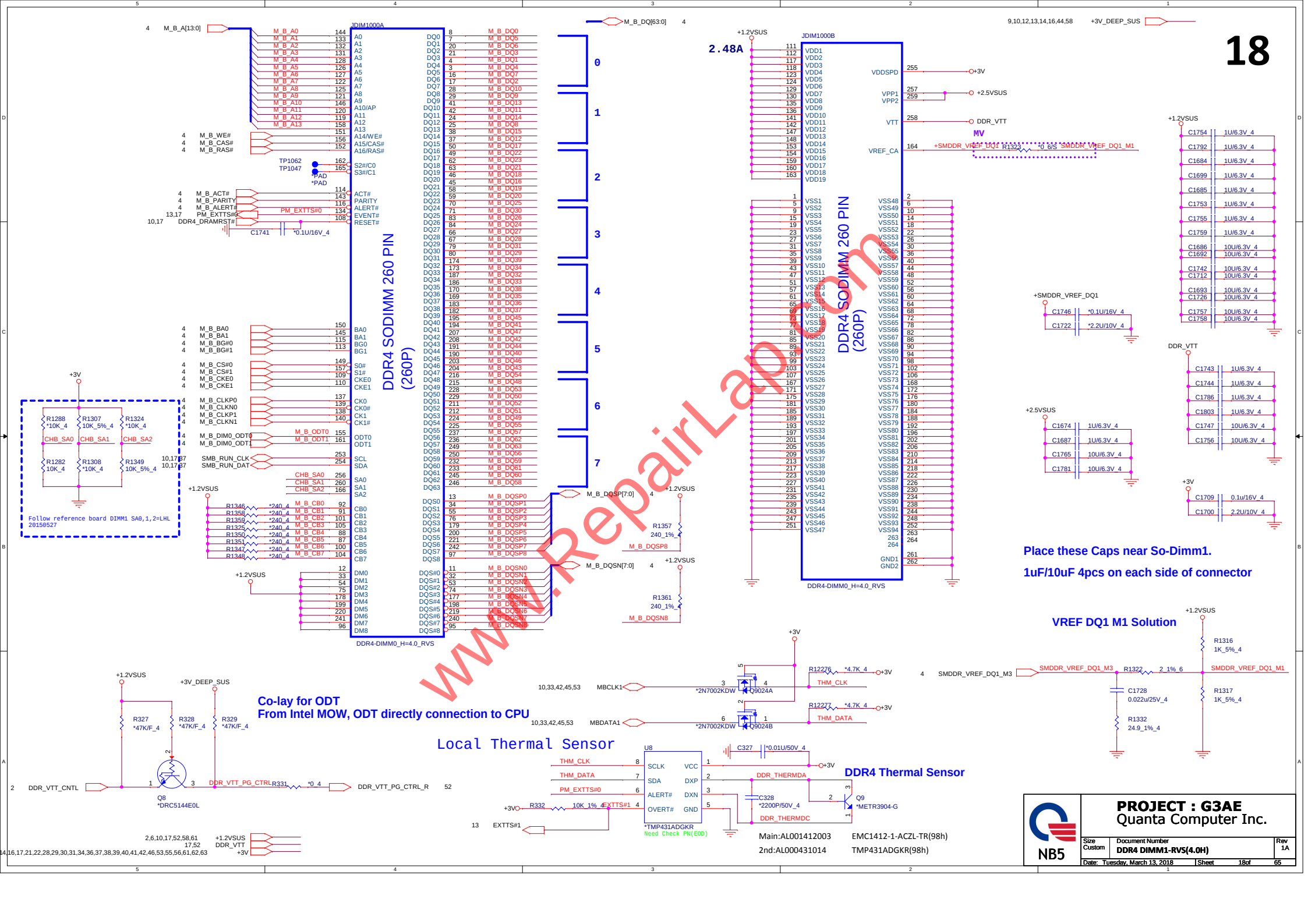

NB5	**PROJECT : G3AE** Quanta Computer Inc.
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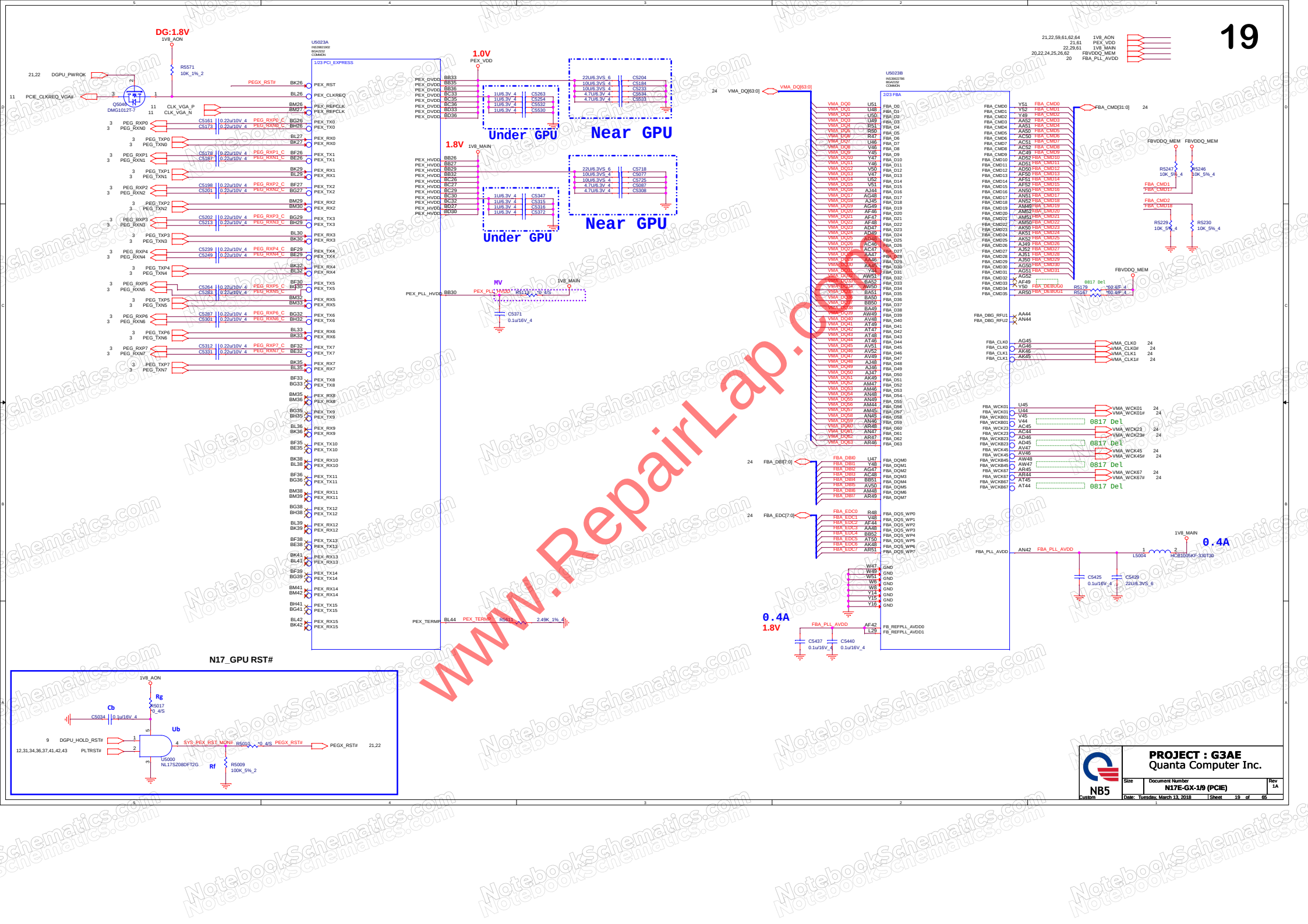
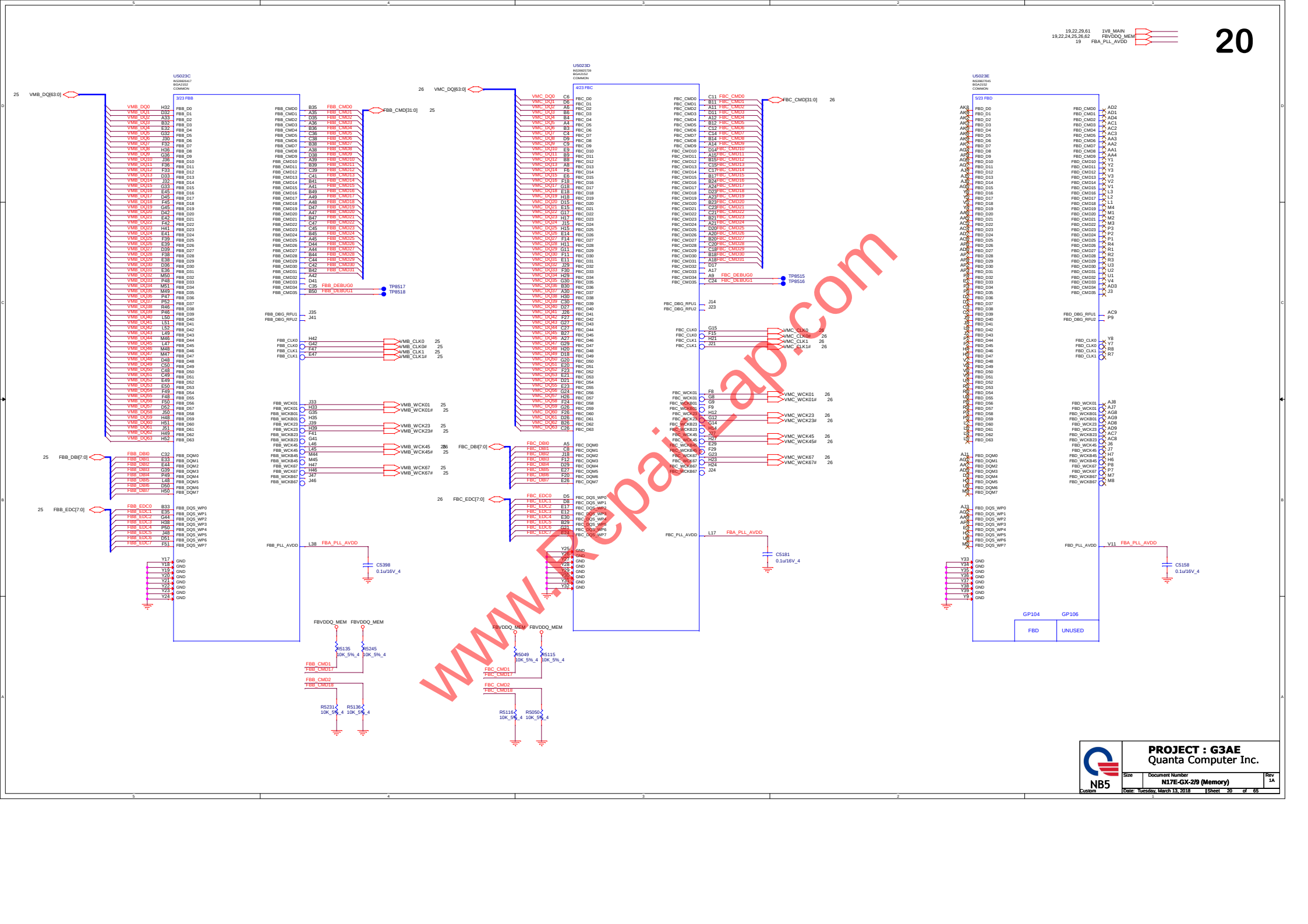
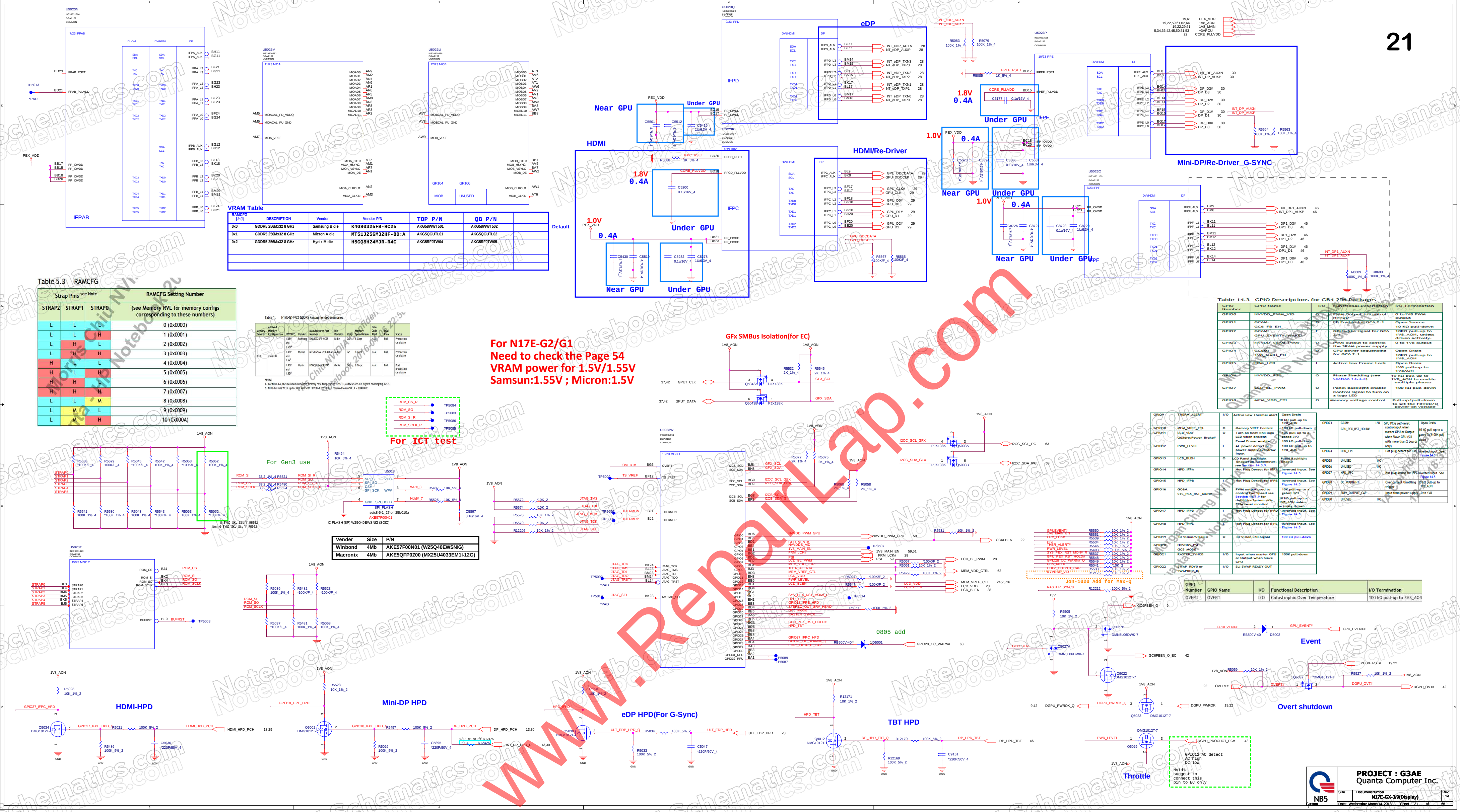






VRAM Table

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	QB P/N	
0x0	GDDR5 256Mx32 8 GHz	Samsung B die	K4G80325FB-HC25	AKG58WWT501	AKG58WWT502	
0x1	GDDR5 256Mx32 8 GHz	Micron A die	MT51J256M32HF-80:A	AKG5QGUTL01	AKG5QGUTL02	
0x2	GDDR5 256Mx32 8 GHz	Hynix M die	H5GQ8H24MJR-R4C	AKG5RF0TW04	AKG5RF0TW05	

Default

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)

Table 1. N17E-G1/-G2 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.55V[2]	Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.5V[2]	Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V[2]	Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	Full	Post production candidate

Notes:

1. For N17E-Gx, the maximum allowable memory case temperature is 95 °C, as these are our highest end flagship GPUs.
2. N17E-Gx runs WCLK up to 3000 MHz with FBVDD=1.35V. DVS is required to run WCLK > 3000 MHz.

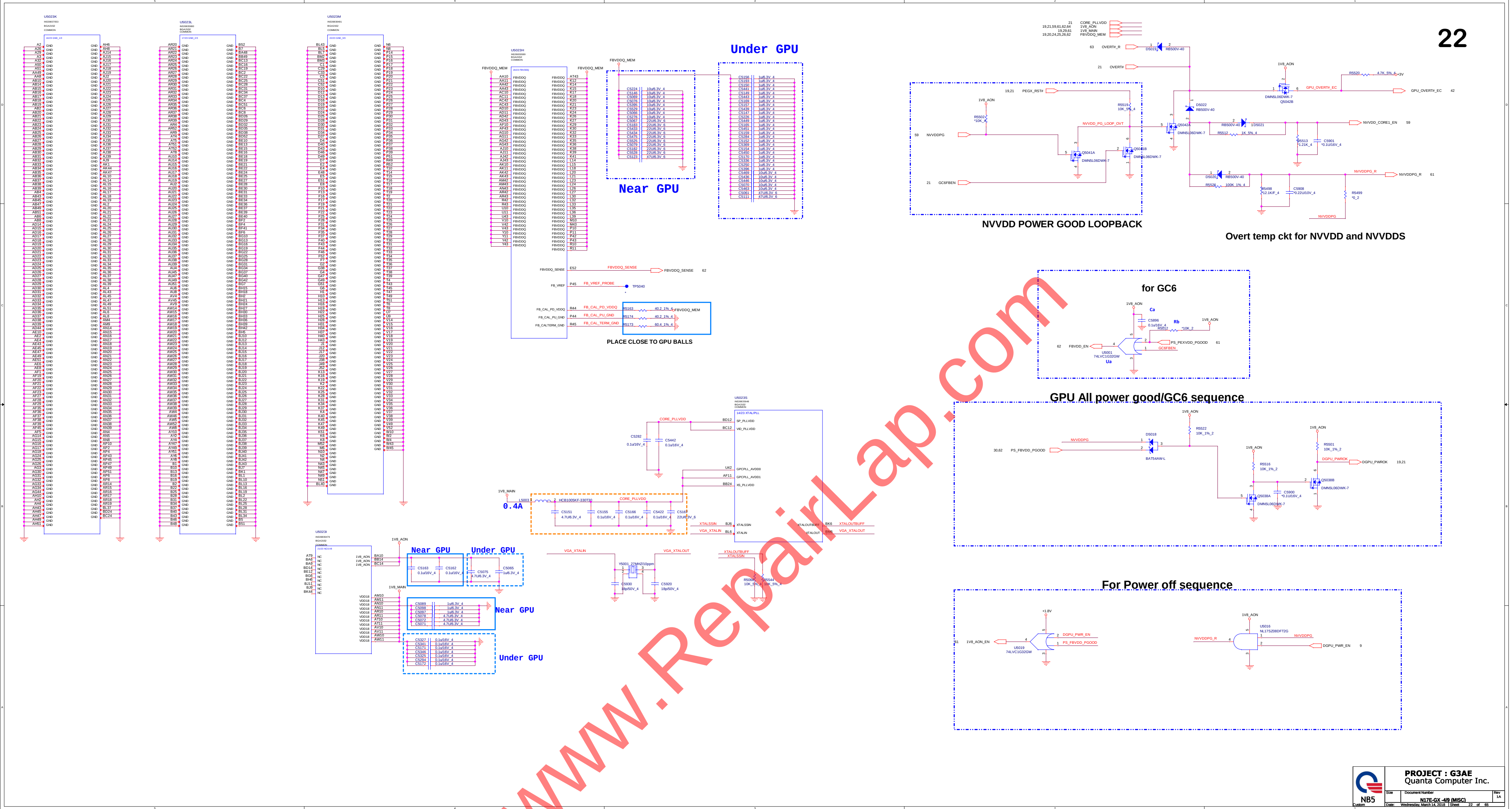
SPI Flash

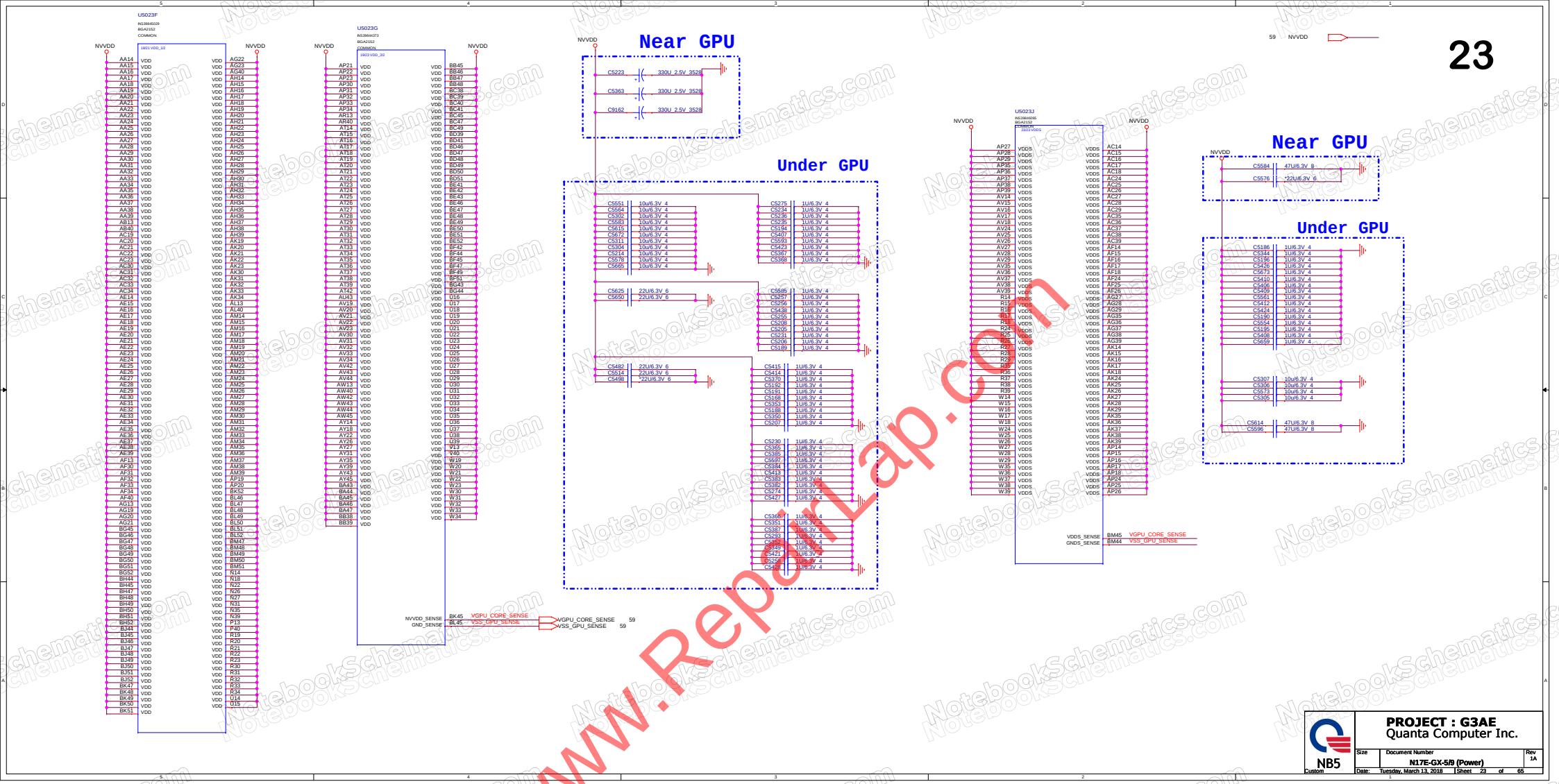
Vender	Size	P/N
Winbond	4Mb	AKE57F00N01 (W25Q40EWSNIG)
Macronix	4Mb	AKE5QFP0Z00 (MX25U4033EM1I-12G)

Table 14.3 GPIO Descriptions for GB4-256 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	0 to1V8 PWM output
GPIO1	GC6M: GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source 10 KΩ pull-down
GPIO2	GC6M: GPU_EVENT#/WAKE*	I	GPU wake signal for GC6 2.1	10KΩ pull-up to 1V8_AON, unless driven actively.
GPIO3	NVVDD_SRAM_PWM	O	PWM output to control the SRAM power supply	0 to 1V8 output
GPIO4	GC6M: 1V8_MAIN_EN	O	GPU power sequencing for GC6 2.1	Open Drain 10KΩ pull-up to 1V8_AON
GPIO5	FRM_LCK	I	Active low Frame Lock	Open Drain 1V8 pull-up to 1V8AON
GPIO6	NVVDD_PSI*	O	Phase Shedding (see Section 14.3.3)	10 kΩ pull-up to 1V8_AON to enable multiple phases
GPIO7	LCD_BL_PWM	O	Panel Backlight enable Control signal to turn on a logo LED	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LCD_VDD Quadro:Power_Brake#	O	Turn on heat sink logo LED when present Panel Power enable	10K pull-up to a gated 3V3 100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 kΩ pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	LCD Panel Backlight EnableFan Tachometer; see Section 14.3.9.	Panel Backlight Enable
GPIO14	HPD_IFPA	I	Hot Plug Detect for IFPA	Inverted input. See Figure 14.5
GPIO15	HPD_IFPB	I	Hot Plug Detect for IFPB	Inverted input. See Figure 14.5
GPIO16	GC6M: SYS_PEX_RST_MON#	O	PWM output used to control Fan Speed see Section 14.3.9 for definitionSystem side PCIe reset monitor	10K pull-up to a gated 3V3 10 kΩ pull-up to 1V8_AON unless actively driven
GPIO17	HPD_IFPD	I	Hot Plug Detect for IFPD	Inverted input. See Figure 14.5
GPIO18	HPD_IFPE	I	Hot Plug Detect for IFPE	Inverted input. See Figure 14.5
GPIO19	3D Vision/STEREO	O	3D Vision L/R Signal	100 kΩ pull-down
GPIO20	NVVDDS_PSI GC5_MODE			
GPIO21	RASTER_SYNC0	I/O	Input when master GPU or Output when Slave GPU	100K pull-down
GPIO22	SWAP_RDY0 or SWAPRDY_IN	I/O	SLI SWAP READY OUT	
GPIO23	GC6M: GPU_PEX_RST_HOLD#	I/O	GPU PCIe self-reset controlInput when master GPU or Output when Slave GPU (SLI with more than 2 boards only)	Open Drain 10 kΩ pull-up to a gated 3V3100K pull-down
GPIO24	HPD_IFPF	I	Hot plug detect for IFPF	Inverted input. See Figure 14.5
GPIO25	UNUSED	I/O		
GPIO26	UNUSED	I/O		
GPIO27	HPD_IFPC	I	Hot plug detect for IFPC	Inverted input. See Figure 14.5
GPIO28	OC_WARN/HT	I	Over current throttling trigger	10 kΩ pull-up to 1V8_AON
GPIO29	EDPc_OUTPUT_CAP	I	Input from power supply	0 to 1V8
GPIO30	UNUSED	I/O		

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AON





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CHANNEL A: 2G/4G GDDR5

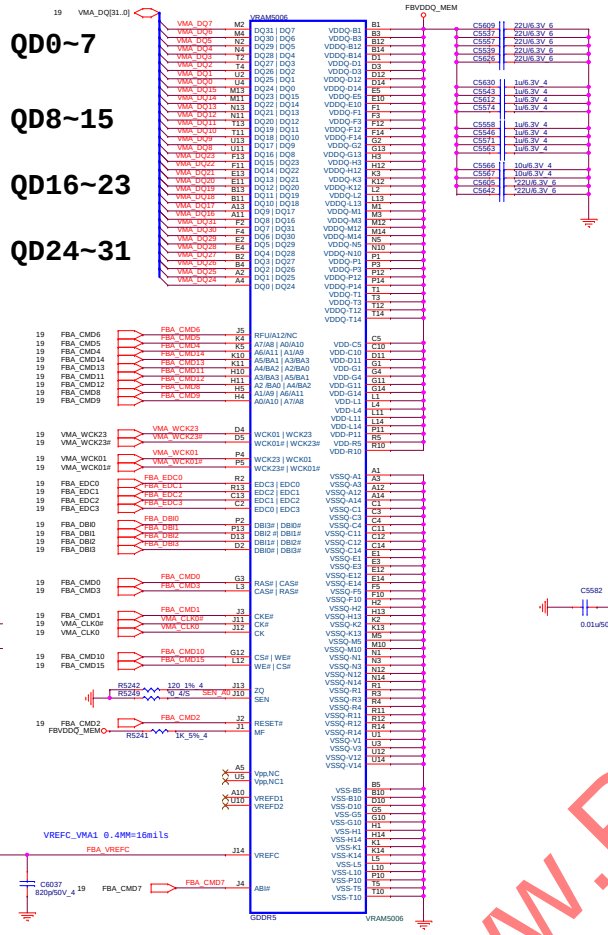
Channel 0
<0-31>
MF=1 mirrored

QD0~7

QD8~15

QD16~23

QD24~31



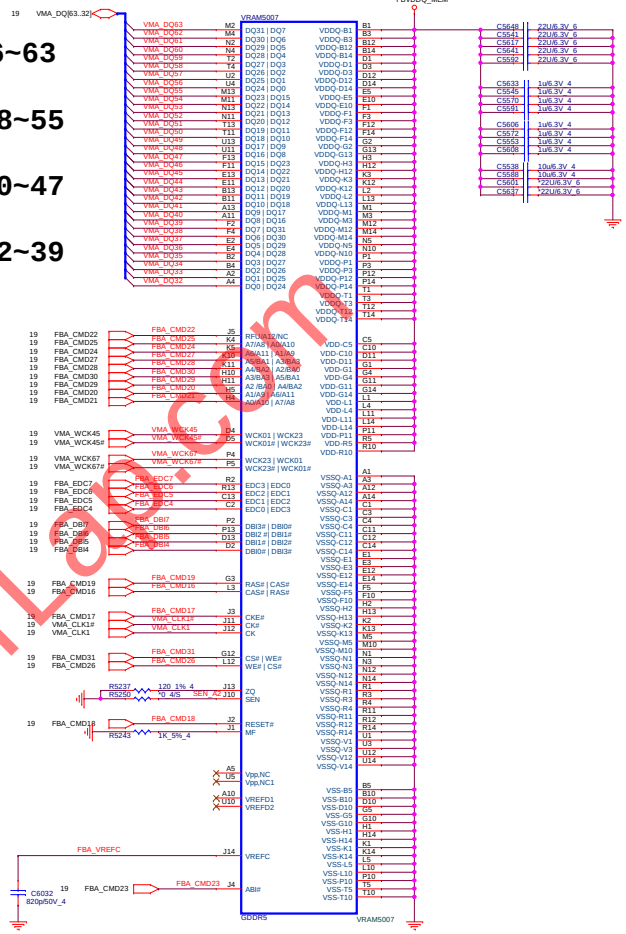
Channel 1
<32-63>
MF=0 Non-mirrored

QD56~63

QD48~55

QD40~47

QD32~39



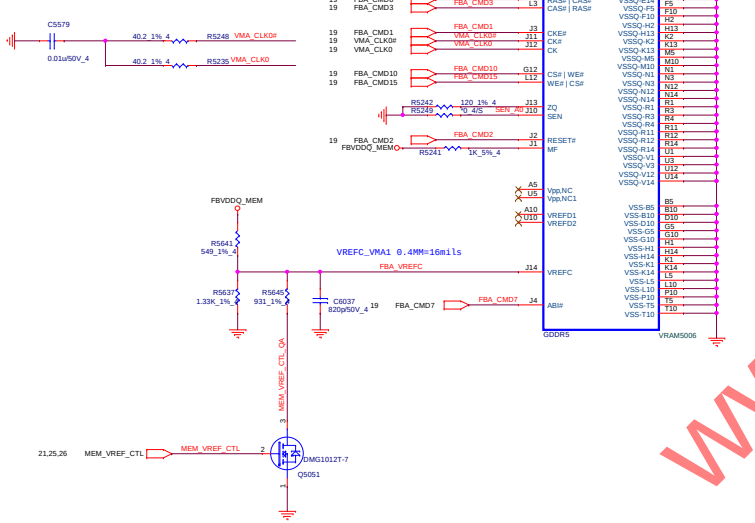


Table 7-5. GDDR5 Mode F Mapping

GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
CMD0	CAS*	CMD16	CAS*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RAS*	CMD19	RAS*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	ABI*	CMD23	ABI*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
GB3-256	Channel 0 & 1		
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG0[1]		
CMD35	DEBUG1[1]		

Notes:
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

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CHANNEL B: 2G/4G GDDR5

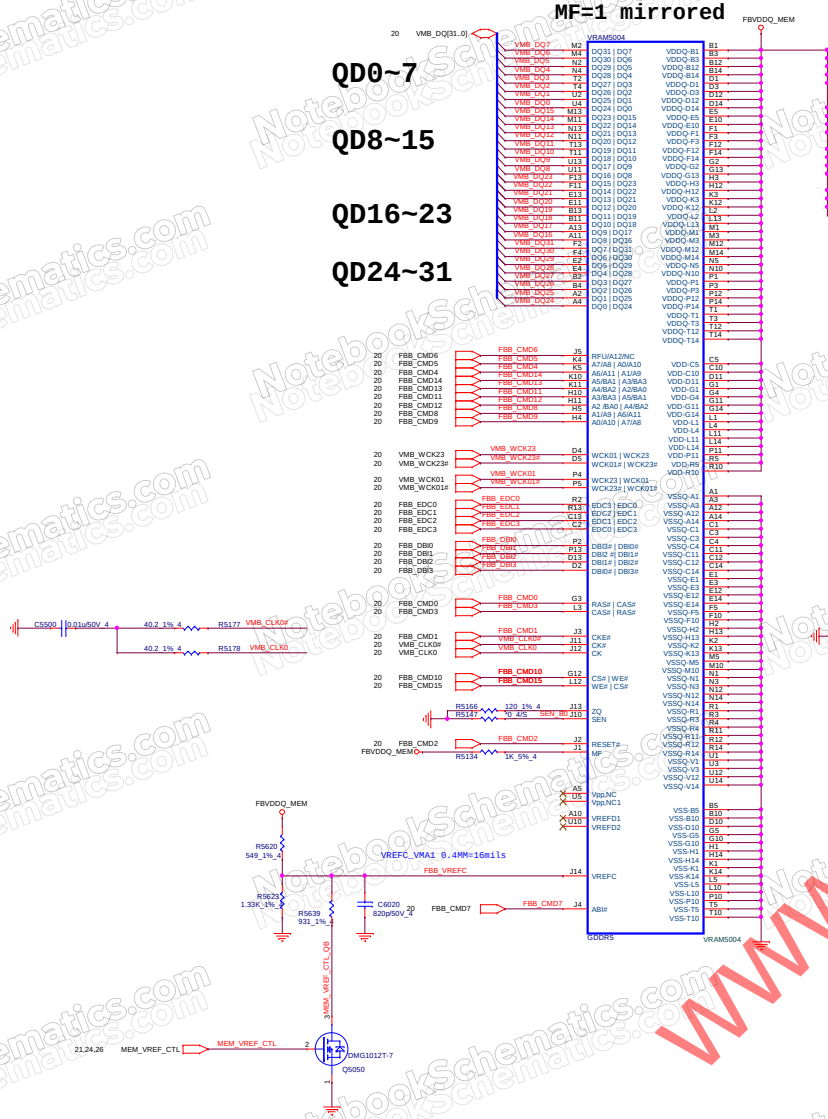
Channel 0 <0-31> MF=1 mirrored

QD0~7

QD8~15

QD16~23

QD24~31



Channel 1 <0-31> MF=0 Non-mirrored

QD56~63

QD48~55

QD40~47

QD32~39

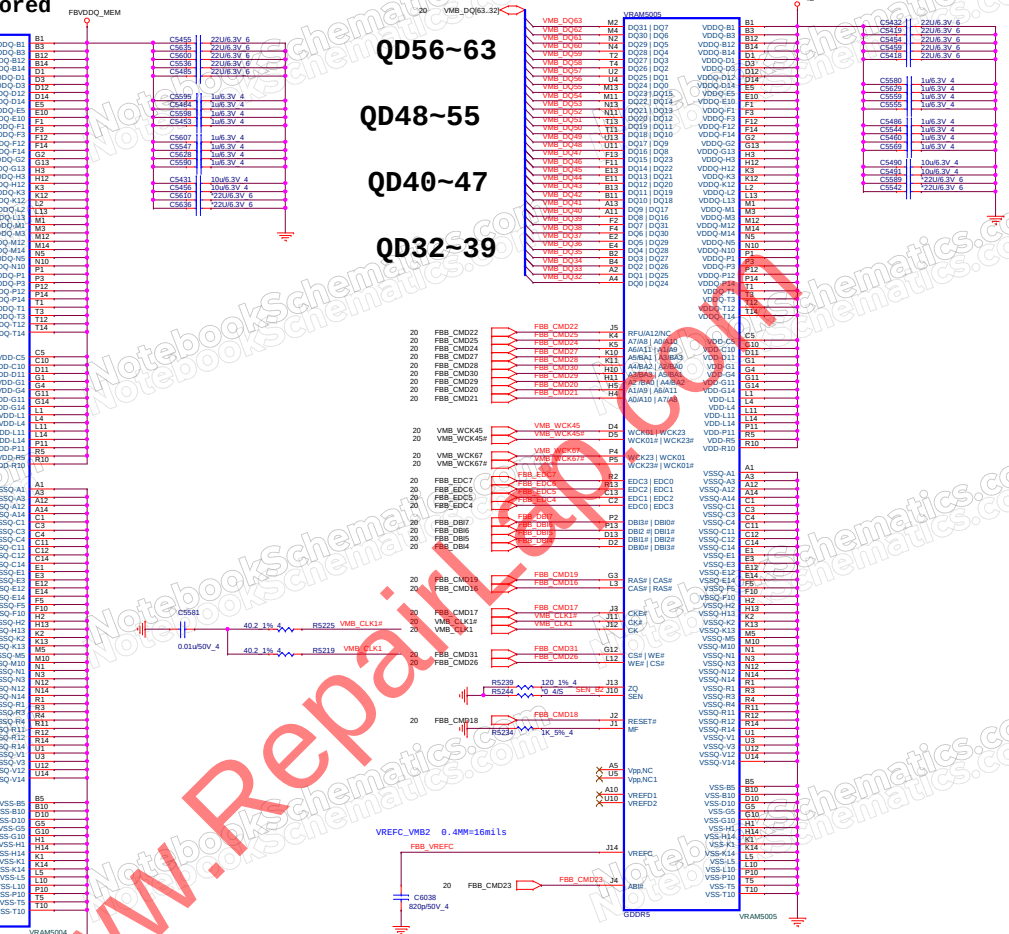


Table 7-5. GDDR5 Mode F Mapping

GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
CMD0	CAS*	CMD16	CAS*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RAS*	CMD19	RAS*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	ABI*	CMD23	ABI*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
GB3-256	Channel 0 B 1		
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG0[1]		
CMD35	DEBUG1[1]		

Notes:
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

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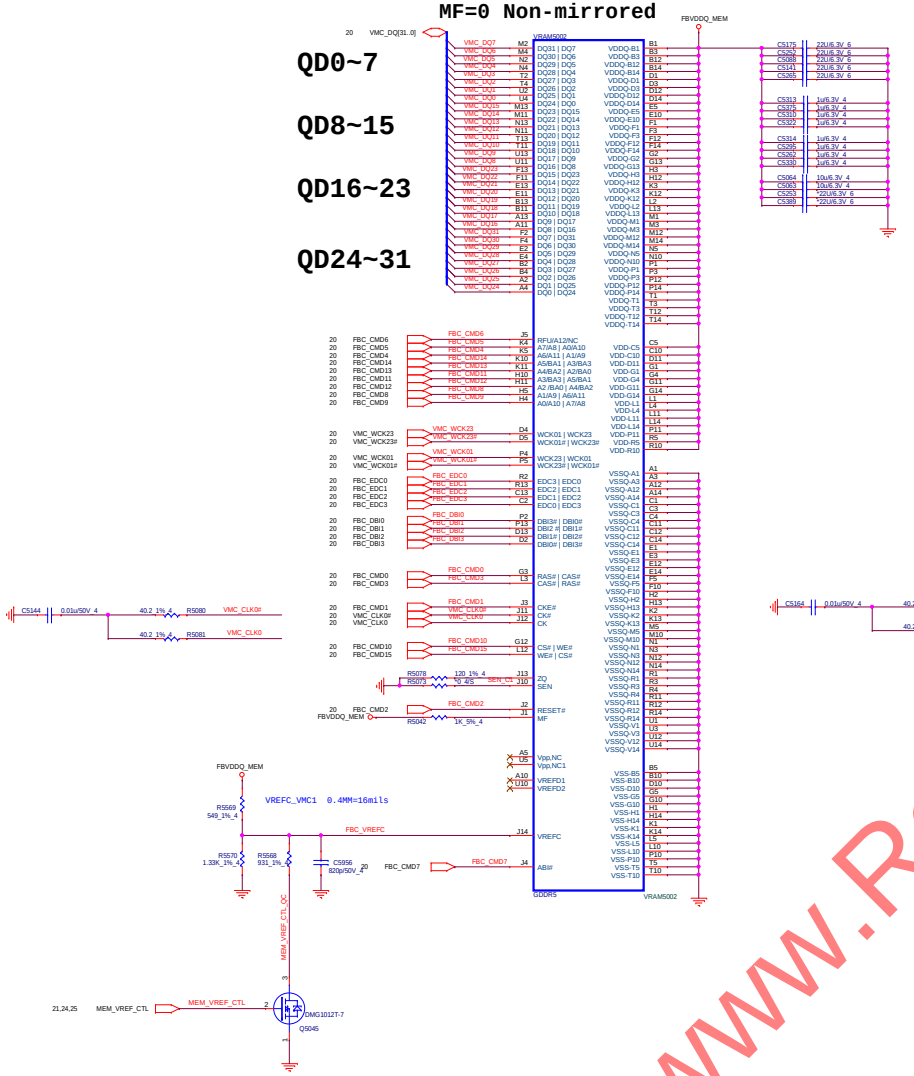
Channel 0
<0-31>
MF=0 Non-mirrored

QD0~7

QD8~15

QD16~23

QD24~31



Channel 1
<0-31>
MF=0 Non-mirrored

QD56~63

QD48~55

QD40~47

QD32~39

Table 7-5. GDDR5 Mode F Mapping

GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
CMD0	CAS*	CMD16	CAS*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RAS*	CMD19	RAS*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	ABI*	CMD23	ABI*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	C5*	CMD31	C5*
GB3-256	Channel 0 & 1		
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG0		
CMD35	DEBUG1		

Notes:
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

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Not Support for N17E-G1

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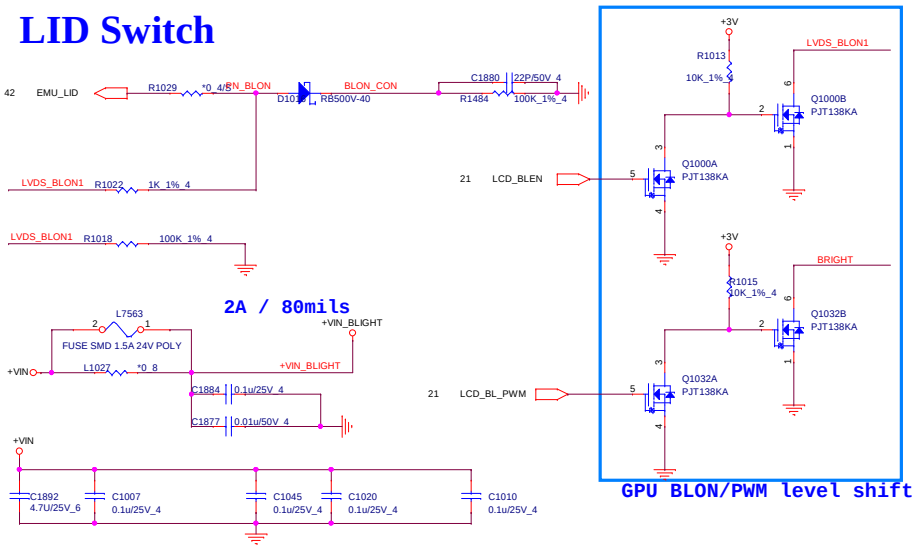
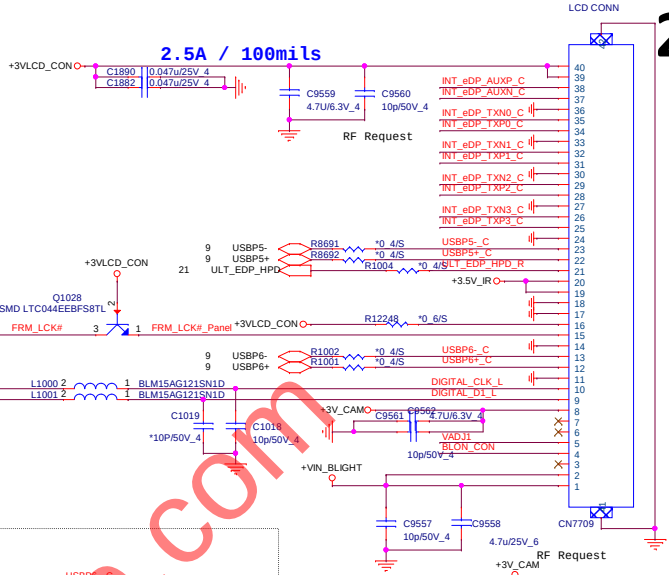
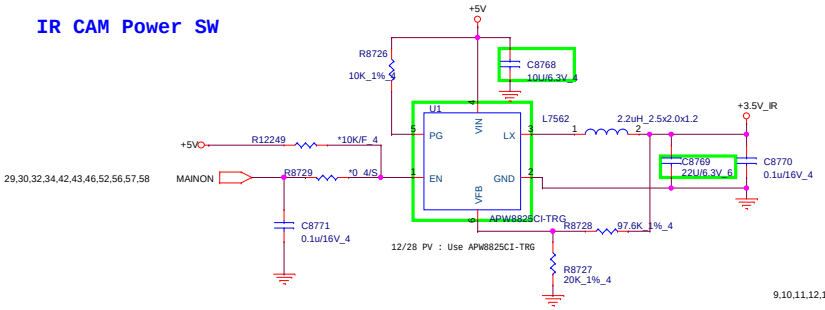
LID Switch

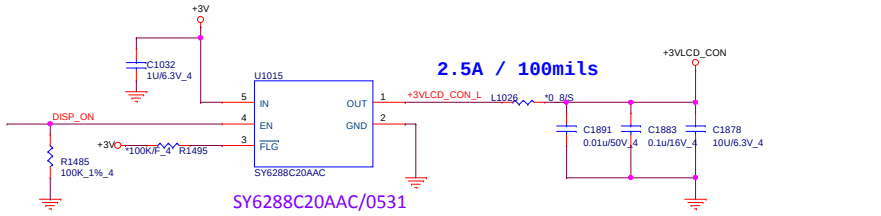


eDP Conn.



IR CAM Power SW





9,10,11,12,13,14,16,17,18,21,22,29,30,31,34,36,37,38,39,40,41,42,46,53,55,56,61,62,63 +3V
5,34,36,42,45,50,51,53 +3VPCU
29,30,33,35,37,38,39,54,56,59 +5V
35,37,40,50,51,52,53,54,55,57,58,59,62,64 +VIN

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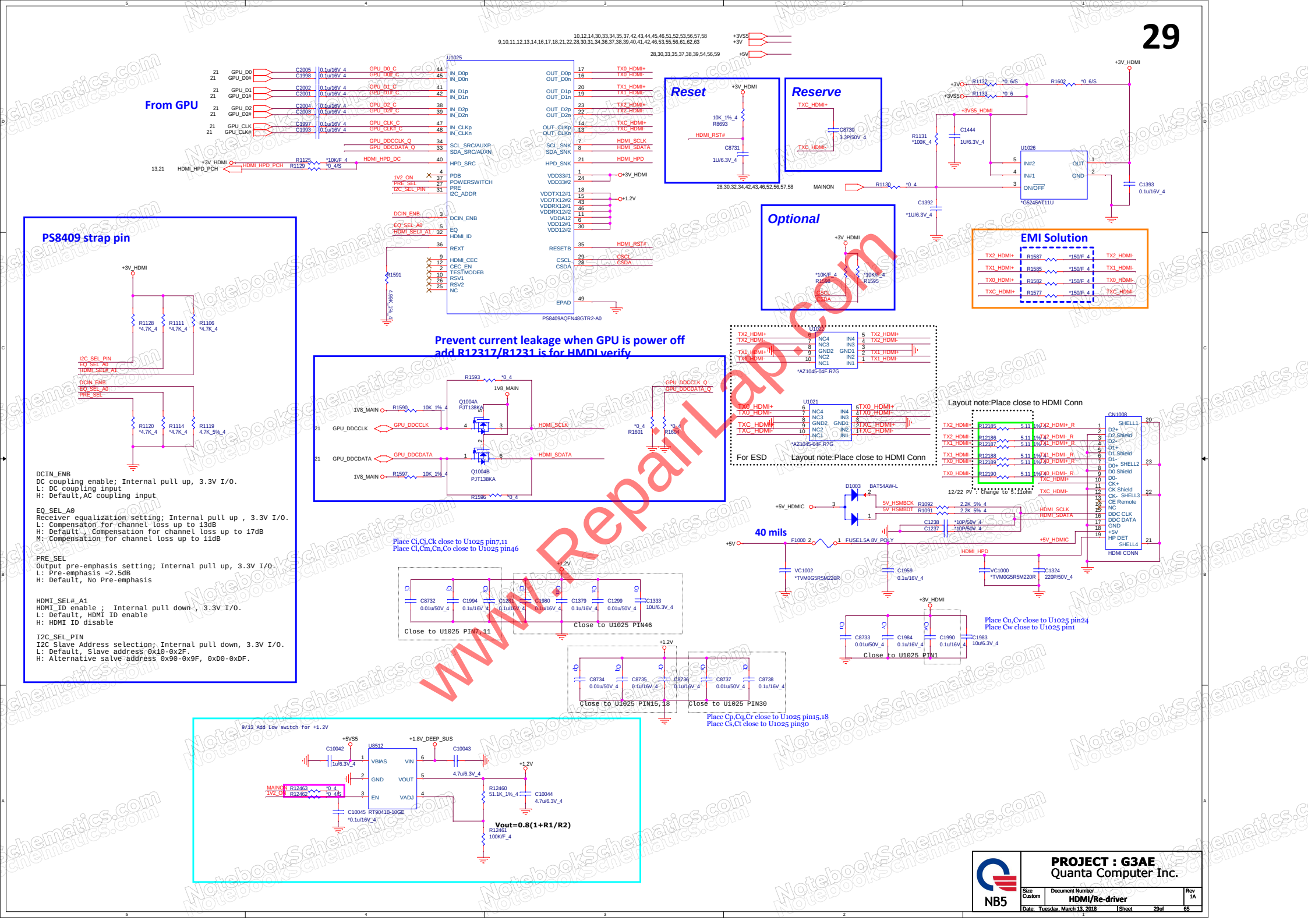
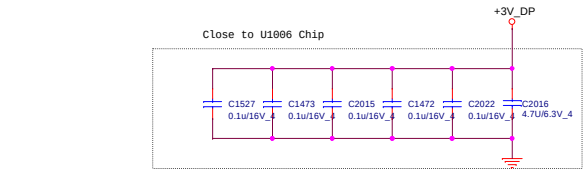
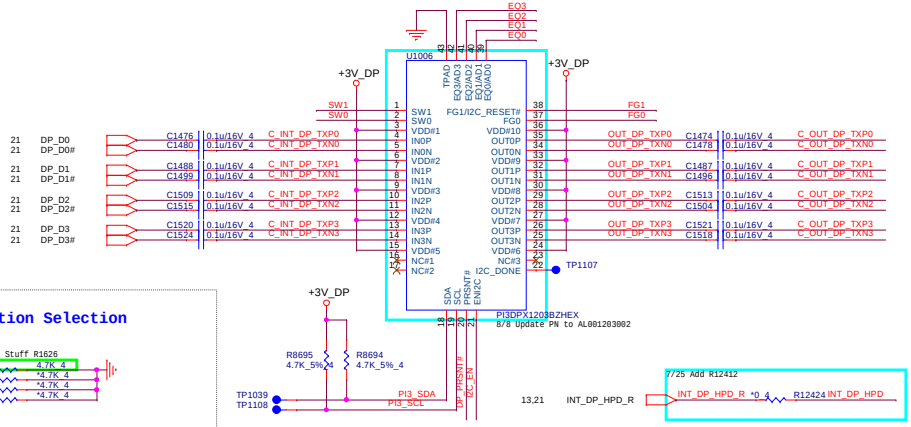
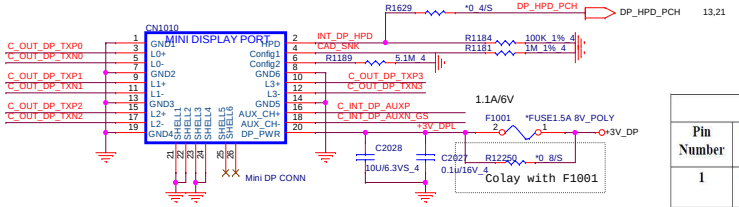


+5V 28,29,33,35,37,38,39,54,56,59
+3V 9,10,11,12,13,14,16,17,18,21,22,28,29,31,34,36,37,38,39,40,41,42,46,53,55,56,61,62,63

DisplayPort Source







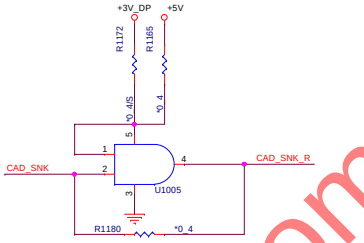
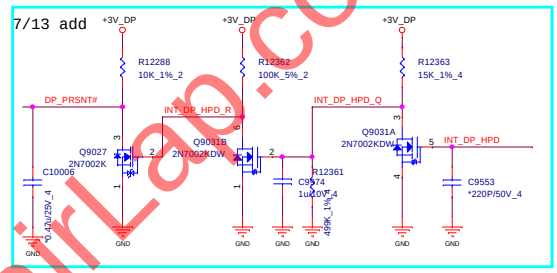


Table 2-1: Source-Side Mini DisplayPort Connector Pin Assignment

Top Row			Bottom Row		
Pin Number	Signal Type	Pin Name	Pin Number	Signal Type	Pin Name
1	GND	GND	2	In	Hot Plug Detect
3	Out	ML_Lane 0 (p)	4	CONFIG (see note 1)	CONFIG1
5	Out	ML_Lane 0 (n)	6	CONFIG (see note 1)	CONFIG2
7	GND	GND	8	GND	GND
9	Out	ML_Lane 1 (p)	10	Out	ML_Lane 3 (p)
11	Out	ML_Lane 1 (n)	12	Out	ML_Lane 3 (n)
13	GND	GND	14	GND	GND
15	Out	ML_Lane 2 (p)	16	I/O	AUX_CH (p)
17	Out	ML_Lane 2 (n)	18	I/O	AUX_CH (n)
19	GND	GND	20	PWR Out (see note 2)	DP_PWR

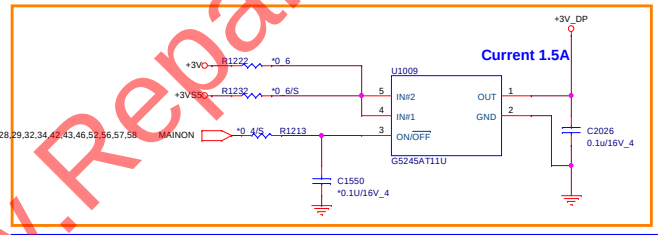


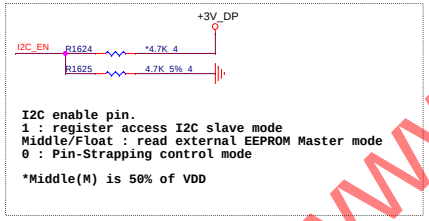
9/26 Del TVS

For ESD Layout note:Place close to mini display Conn

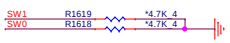
Input Equalization Selection for Main Link

EQ3	EQ2	EQ1	EQ0	8 Gbps Input EQ(dB)
0	0	0	0	3.3
0	0	0	1	3.8
0	0	1	0	4.3
0	0	1	1	4.8
0	1	0	0	5.4
0	1	0	1	5.8
0	1	1	0	6.3
0	1	1	1	6.8
1	0	0	0	7.2
1	0	0	1	7.7
1	0	1	0	8.1
1	0	1	1	8.5
1	1	0	0	8.9
1	1	0	1	9.2
1	1	1	0	9.6
1	1	1	1	9.9



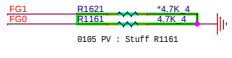


Output -1dB Compression Setting



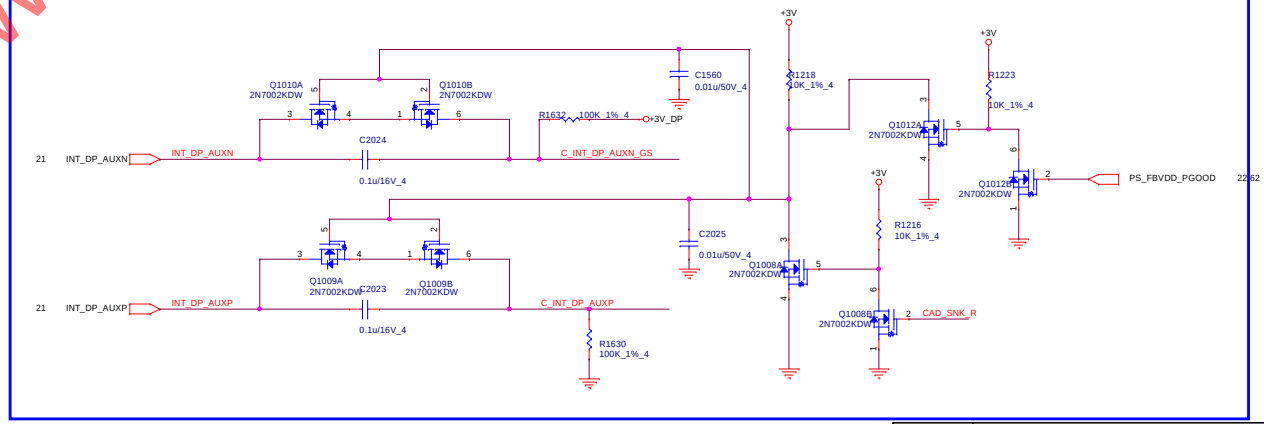
SW1	SW0	mVppd@8 Gbps
0	0	700
0	1	800
1	0	900
1	1	1000

Flat Gain Setting



FG1	FG0	Gain
0	0	-4 dB
0	1	-2 dB
1	0	+0 dB
1	1	+2 dB

support dual mode /0525



NB5

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9. Power Sequence

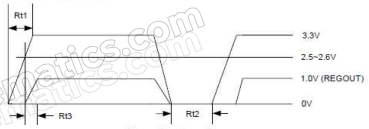


Figure 4. Power Sequence

Table 16. Power Sequence Parameter

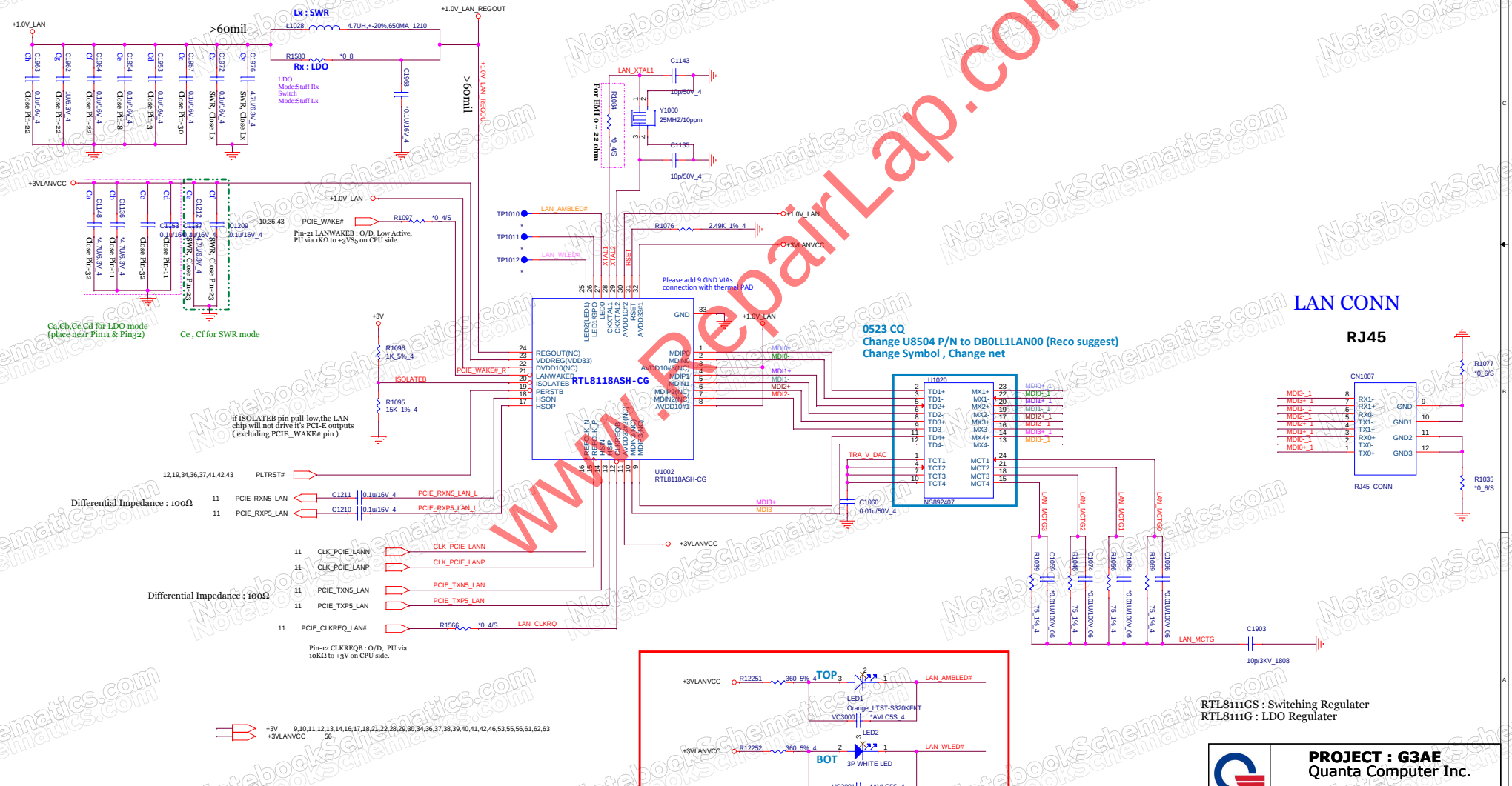
Symbol	Description	Min	Typical	Max	Units
Rt1	3.3V Rise Time	0.5	-	100	ms
Rt2	3.3V Off Time	50	-	-	ms
Rt3	1.0V (REGOUT) Settle Time	-	-	15	ms

Note: See the following section for power sequence requirements.

Place Cc,Ch,Ce,Cf close to each VDD10 pin-- 3,8,22,30
Place Cg & Cd close to each VDD10 pin22

Power trace Layout W > 60mil
Trace<30 mil
Width > 60 mil

RTL8111HS (SWR Mode) Pin-24 REGOUT : Switching Regulator 1.0V Output.
RTL8111H (LDO Mode) Pin-24 REGOUT : LDO Regulator 1.0V Output.



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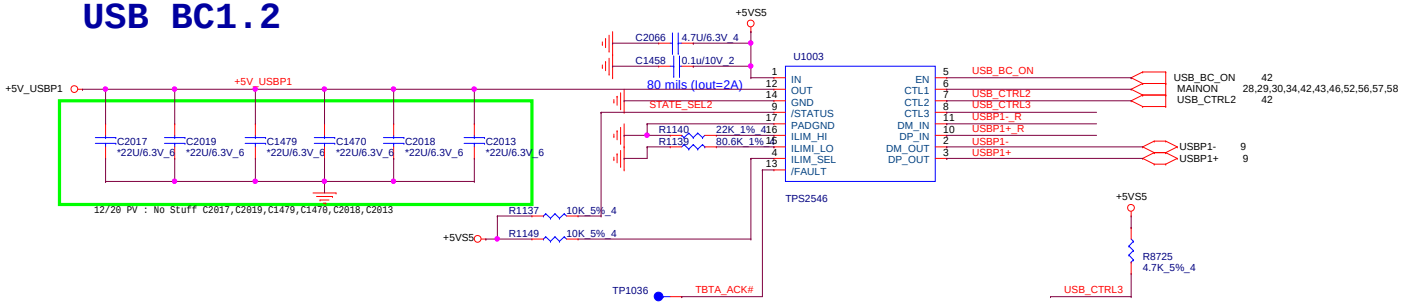
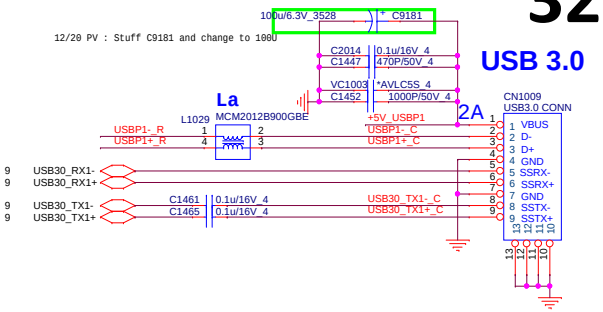
USB BC1.2



USB 2.0/3.0 Combo MB



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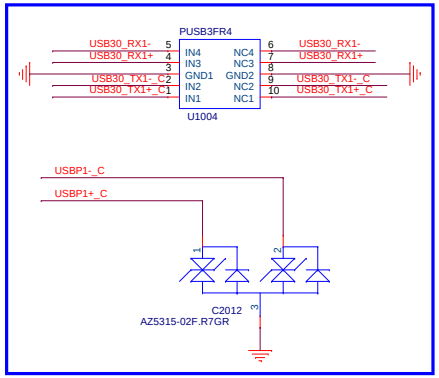
USB 3.0

USB3 Re-Driver (Only For 17")



TST : Low = Normal LFPS swing / Hight =Turn down LFPS swing

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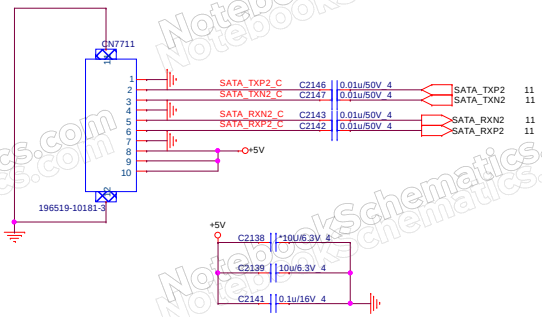
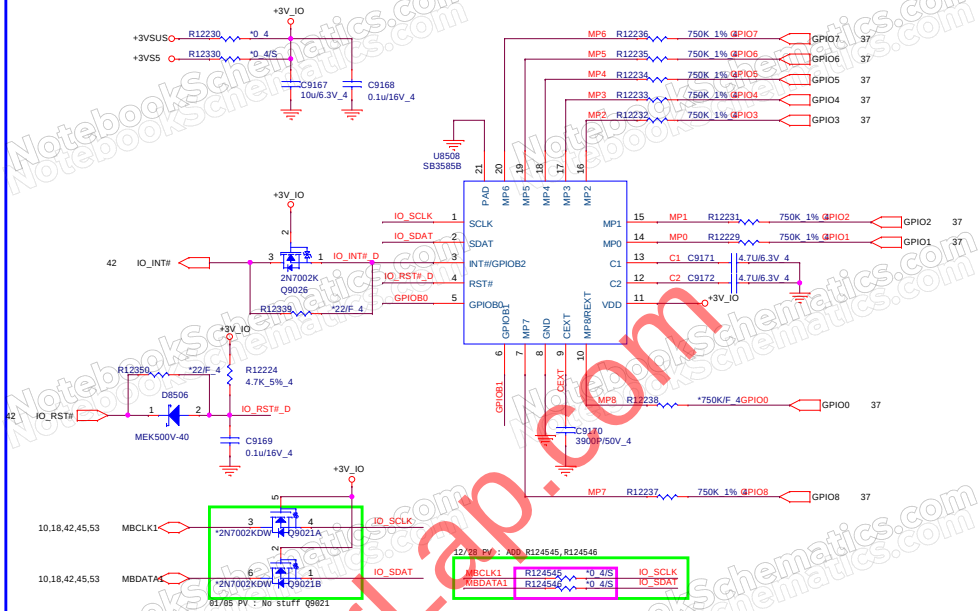
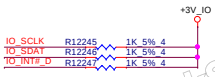
HDD

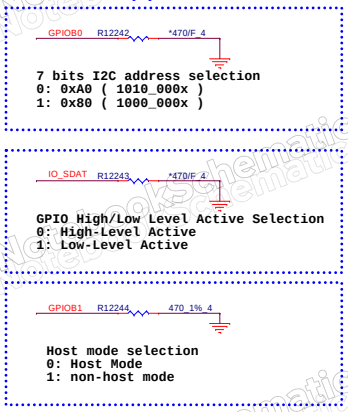


GPIO EXPENDER





Hardware strap pin



SATA ODD 17" ONLY

9,10,11,12,13,14,16,17,18,21,22,28,29,30,31,34,36,37,38,39,40,41,42,46,53,55,56,61,62,63 +3V
28,29,30,35,37,38,39,54,56,59 +5V

NB5	PROJECT : G3AE Quanta Computer Inc.	
Size: Custom	Document Number: HDD/ODD/GPIO EXPENDER	Rev: 1A
Date: Tuesday, March 13, 2018	Sheet 33 of 65	

SSD

CN1014
SSD CONN

3.2H

NGFF

1	CONFIG3/GND	3.3Vaux_1	2
3	GND1	3.3Vaux_2	4
5	PERN3	N/A_2	6
7	PERP3	N/A_3	8
9	GND2	DAS/DSS#(O)(OD)	10
11	PETN3	3.3Vaux_3	12
13	PETP3	3.3Vaux_4	14
15	GND3	3.3Vaux_5	16
17	PERN2	3.3Vaux_6	18
19	PERP2	N/A_4	20
21	CONFIG0/GND	N/A_5	22
23	PETN2	N/A_6	24
25	PETP2	N/A_7	26
27	GND4	N/A_8	28
29	PERN1	N/A_9	30
31	PERP1	N/A_10	32
33	GND5	N/A_11	34
35	PETN1	N/A_12	36
37	PETP1	DEVSLP	38
39	GND6	N/A_13	40
41	SATA RX+/PERN0	N/A_14	42
43	SATA RX-/PERP0	N/A_15	44
45	GND7	N/A_16	46
47	SATA TX-/PETN0	N/A_17	48
49	SATA TX+/PETP0	PERST#	50
51	GND8	CLKREQ#	52
53	REFCLKN	PEWAKE#/NC	54
55	REFCLKP	MFGDAT	56
57	GND9	MFGCLK	58
67	N/A_1	SUSCLK	68
69	PEDET(NC-PCIE/GND-SATA)		70
71	GND10	3.3Vaux_7	72
73	GND11	3.3Vaux_8	74
75	GND12	3.3Vaux_9	76 77 78 79

ngff-ypci0029-p002a-75p-km

+3V_SSD
RB500V-40 D8512
SATA_LED# 11,36
R1831 *0_8/S +3V
C2132 0.01u/50V_4 C2137 0.1u/16V_4 C2096 4.7U/6.3V_4
R1824 10K_5%_4 +3V
R1816 *0_4 DEVSLP0 9
R1805 *0_4/S R1798 *0_4/S PLTRST# 12,19,31,36,37,41,42,43
PCIE_CLKREQ_SSD# 11
*PAD TP1125
R1828 *0_8/S +3V
EC1054 470p/50V/X7R_4 EC1044 10U/6.3V_4 EC1045 10U/6.3V_4

PCIE_SATA_RXN9 11
PCIE_SATA_RXP9 11
R1801 *0_5%_4/S R1806 *0_5%_4/S
PCIE_SATA_RXN9_C PCIE_SATA_RXP9_C
C2116 0.22u/10V_4 C2110 0.22u/10V_4
PCIE_SATA_TXN9 PCIE_SATA_TXP9
PCIE_SATA_RXN10 PCIE_SATA_RXP10
C2128 0.22u/10V_4 C2125 0.22u/10V_4
PCIE_SATA_TXN10_C PCIE_SATA_TXP10_C
PCIE_SATA_RXN11 PCIE_SATA_RXP11
C2135 0.22u/10V_4 C2131 0.22u/10V_4
PCIE_SATA_TXN11_C PCIE_SATA_TXP11_C
PCIE_SATA_RXP12 PCIE_SATA_RXN12
C2140 0.22u/10V_4 C2136 0.22u/10V_4
PCIE_SATA_TXN12_C PCIE_SATA_TXP12_C
CLK_PCIE_SSDN CLK_PCIE_SSDP

R1769 100K_1%_4 PEDET
GPIO35 11 R1802 *0_4/S
Q1056 2N7002K
12/20 PV : reserve R124539
PULSAR_38P4M_REFCLK_R1 R124539 *10K_4
SUSCLK_32KHZ R12471 *100K/F_4
Near connector

Mini Card WLAN/BT(Option)

0925 for CNVi power control

+3VPCU R1188 10K_4
+3VPCU R124531 10K_4
R1187 200K_4
Q1007A 2N7002KDW
Q1007B 2N7002KDW
CNVI_EN# 10
R23026 75K_1%_4
MAINON 28,29,30,32,42,43,46,52,56,57,58
C1793 0.022U/25V_4

+3VS5 R12468 *0_8 R12286 *0_8
8/4 R12286 change FP
Q1018 PJA3415
24mil
+3V_AOCS
C2030 0.1U/16V_4
+3V_WLAN_P
+3V
C2072 0.1u/16V_4 C2071 0.01u/50V_4 C2066 10U/6.3V_4
C2029 10U/6.3V_4 C2031 0.1u/16V_4

For EMI Suggestion

CLK_24M_DEBUG EC1037 *33P/50V_4
R1715 *0_4
R1333 *0_4/S REQ_WLAN#
PCIE_CLKREQ_WLAN# 11

CN1012

6.4H

NGFF

1	GND_1	3.3Vaux_1	2
3	USB_D+	3.3Vaux_2	4
5	USB_D-	LED#1	6
7	GND_2	PCM_CLK	8
9	WR_D1N	PCM_SYNC	10
11	WR_D1P	PCM_IN	12
13	GND_14	PCM_OUT	14
15	WR_D0N	LED#2	16
17	WR_D0P	GND_11	18
19	GND_15	UART Wake	20
21	WR_CLKN	CNV_BRI_RSP	22
23	WR_CLKP		24
33	GND_3	CNV_RGI_DT	32
35	PETp0	CNV_RGI_RSP	34
37	PETn0	CNV_BRI_DT	36
39	GND_4	Clink RESET	38
41	PERp0	CLink DATA	40
43	PERn0	CLink CLK	42
45	GND_5	COEX3	44
47	REFCLKP0	COEX2	46
49	REFCLKN0	COEX1	48
51	GND_6	SUSCLK(32KHz)	50
53	CLKREQ0#	PERST0#	52
55	PEWake0#	W_DISABLE2#	54
57	GND_7	W_DISABLE1#	56
59	WT_D1N	NFC I2C SM DATA	58
61	WT_D1P	NFC I2C SM CLK	60
63	GND_8	ALERT#	62
65	WT_D0N	REFCLK0	64
67	WT_D0P	UIM_SWP/PERST1#	66
69	GND_9	UIM_POWER_SNK	68
71	WT_CLKN	UIM_POWER_SRC	70
73	WT_CLKP	3.3Vaux_3	72
75	GND_10	3.3Vaux_4	74
79 78 76 77		GND_12 GND_13	

WLAN_NGFF CONN (E-Key)

USBP7+ 9
USBP7- 9
CNV_WR_LANE1_DN 13
CNV_WR_LANE1_DP 13
CNV_WR_LANE0_DN 13
CNV_WR_LANE0_DP 13
CNV_WR_CLK_DN 13
CNV_WR_CLK_DP 13
SI : 0830 ADD

PCIE_TXP6_WLAN 11
PCIE_TXN6_WLAN 11
C2083 0.1u/16V_4 PCIE_TXP6_WLAN_C
C2080 0.1u/16V_4 PCIE_TXN6_WLAN_C
PCIE_RXP6_WLAN 11
PCIE_RXN6_WLAN 11
CLK_PCIE_WLANP 11
CLK_PCIE_WLANN 11
TP1058 *PAD
REQ_WLAN#
MINICAR_PME#
CNV_WT_LANE1_DN 13
CNV_WT_LANE1_DP 13
CNV_WT_LANE0_DN 13
CNV_WT_LANE0_DP 13
CNV_WT_CLK_DN 13
CNV_WT_CLK_DP 13

+3V_WLAN_P
WLAN_LED#
R1635 4.7K_5%_4 +3V_WLAN_P
R1640 *0_4/S
CNV_RF_RESET# L
SI : 9/20 SWAP net for pin10/14
MODEM_CLKREQ_L
CNV_BRI_RSP_L R12475 22/F_4 CNV_BRI_RSP 13
CNVi RBI_RSP, RGI_RSP 22 Ohm, to be placed close to the connector.
CNVi RBI_DT, RGI_DT 33 Ohm, to be placed close to the PCH.
CNV_RGI_DT_L R12476 33_4 CNV_RGI_DT 13,16
CNV_RGI_RSP_L R12477 22/F_4 CNV_RGI_RSP 13
CNV_BRI_DT_L R12478 33_4 CNV_BRI_DT 13,16
SI : ADD R12440 9/13 Change net name
SUSCLK_32KHZ R12440 *0_2 SUSCLK_32K SUSCLK_32K 10
PLTRST#
INT_BT_OFF#
INT_RF_OFF#
R1690 10K_5%_4
R1693 10K_5%_4 +3V_WLAN_P
LAD0 9,41,42
CLK_24M_DEBUG 9
LFRAME# 9,41,42
PULSAR_38P4M_REFCLK_R1 R12421 *0_2/S PULSAR_38P4M_REFCLK 11
LAD1 9,41,42
LAD2 9,41,42
LAD3 9,41,42
9/18 Del CNVi and nomal debug card option Res..

BT_OFF 13
Q1053A 2N7002KDW INT_BT_OFF#
RF_OFF_PCH 10
Q1053B 2N7002KDW INT_RF_OFF#

+1.8V_DEEP_SUS
12/20 PV : Level shift change to TTL type
U8513 NL17SZ08DFT2G
MODEM_CLKREQ_L 4
R124535 75K_1%_4 R124536 10K_4
MODEM_CLKREQ 10
U8514 NL17SZ08DFT2G
CNV_RF_RESET# L 4
R124537 75K_1%_4 R124538 10K_4
CNV_RF_RESET# 10

NB5

PROJECT : G3AE
Quanta Computer Inc.

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Custom	SSD/WLAN	1A

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12/27 PV : change to +5V

+5V

EC1009 1000P/50V_4

EC1063 1000P/50V_4

+3VS5

EC1038 1000P/50V_4

EC1053 1000P/50V_4

+VIN

EC1059 100p/50V_4

EC1060 100p/50V_4

EC1061 100p/50V_4

EC1033 2200P/50V_4

EC1035 2200P/50V_4

EC1000 1000P/50V_4

EC1062 1000P/50V_4

EC1056 1000P/50V_4

GPU BTK Hole

H18 *h-tc315bc181d142p2

H19 *h-tc315bc181d142p2

H21 *h-tc315bc181d142p2

H20 *h-tc315ic142bc181d142p2

CPU BTK Hole

H11 *h-tc315bc181d142p2

H12 *h-tc315bc181d142p2

H13 *H-TC315I181BC142D142P2

H14 *h-tc315bc181d142p2

SSD NUT

H17 H-TC157BC102D102P2

WLAN NUT

H4 H-TC177BC102D102P2

EMI PAD

FAN Hole

H1 *h-c315d150p2

H8 *h-w15-hne-2

H9 *h-w15-hne-1

H27 *SPAD-W15-HNE-1NP

ESD PAD

R12290 64.9K_1%_6

C9554 Clamp-Diode For ESD

H28 *spad-re276x98nmp

H29 *spad-re276x98nmp

H30 *spad-re276x98nmp

H31 *spad-re276x98nmp

MV

H32 *SPAD-RE393X137NMP

H2 *h-tc217bo118x98d118x98p2

H3 *H-C315i118D118P2

H5 *h-tc217bo118x98d118x98p2

H6 *H-C315D173X150P2

H7 *H-G3AB-1

H10 *H-C315i150D150P2

H15 *h-w15-hne-4

H16 *H-C315D173X150P2

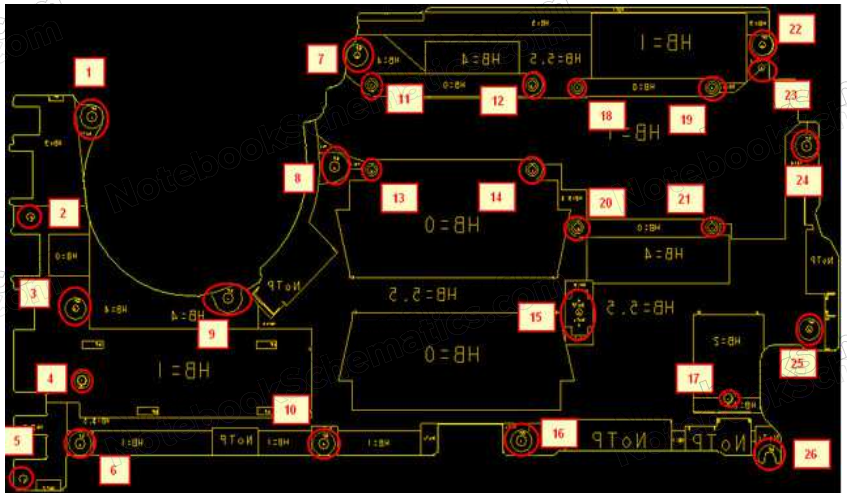
H22 *H-C276I118D118P2

H23 *H-TC315I98BC98D98P2

H24 *H-W15-HNE-3

H25 *H-T315B275D118P

H26 *h-w15-hne-5



NB5

PROJECT : G3AE
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RF Solution/HOLE	1A
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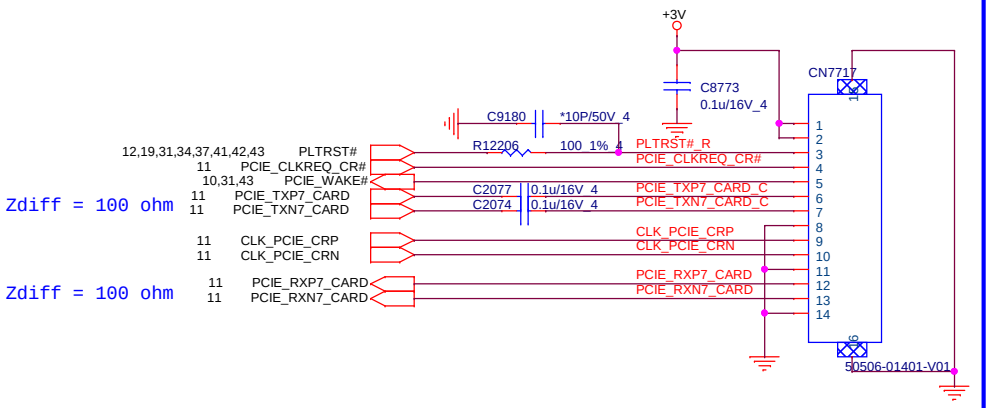
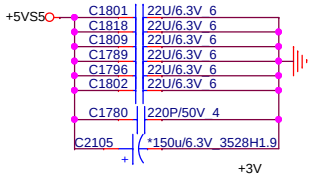
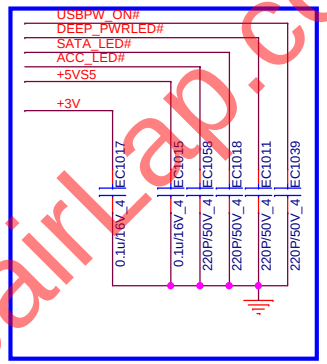
Daughter Board

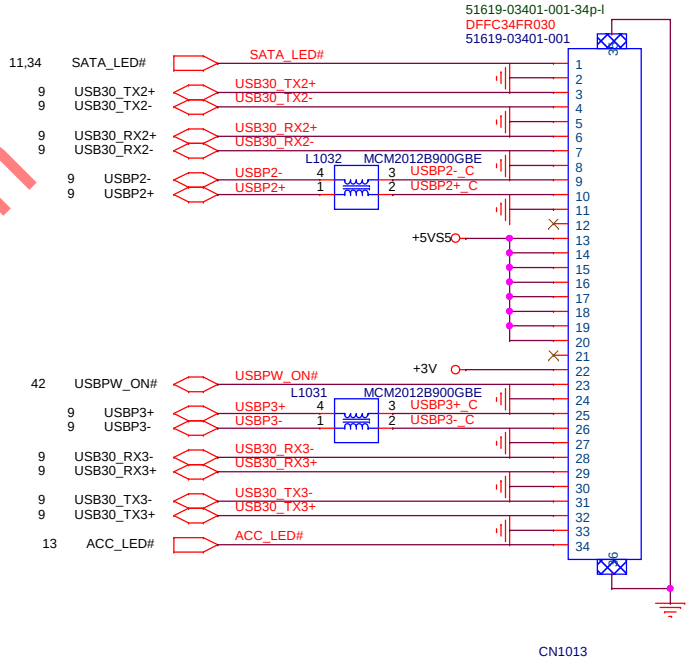
SD Card to Small Board



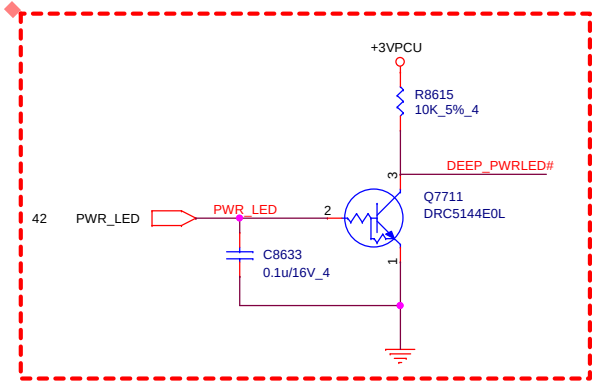


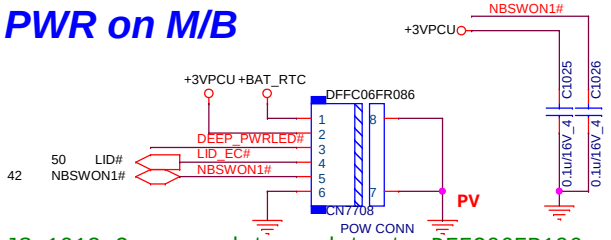
For EMI





PWR on M/B





JS-1012 Conn need to update to DFFC06FR196

B	NB5	PROJECT : G3AE Quanta Computer Inc.
Size	Document Number	Rev
	DB/PWRB/CARDB	1A
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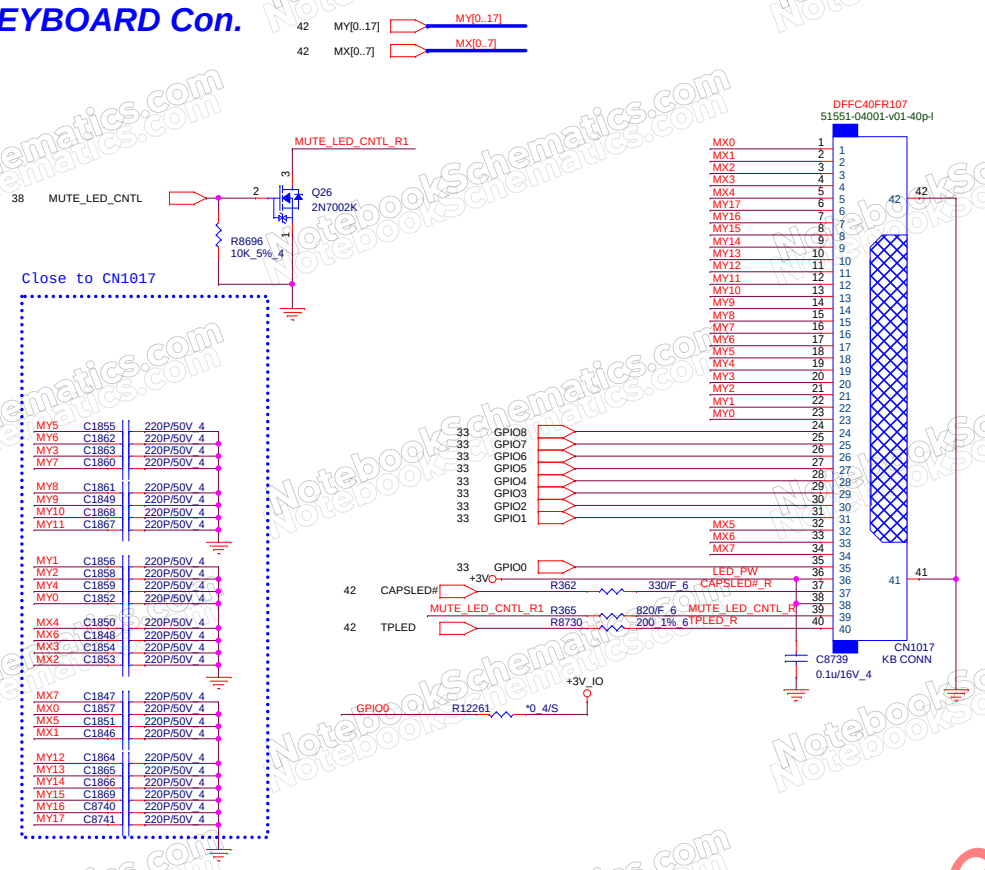
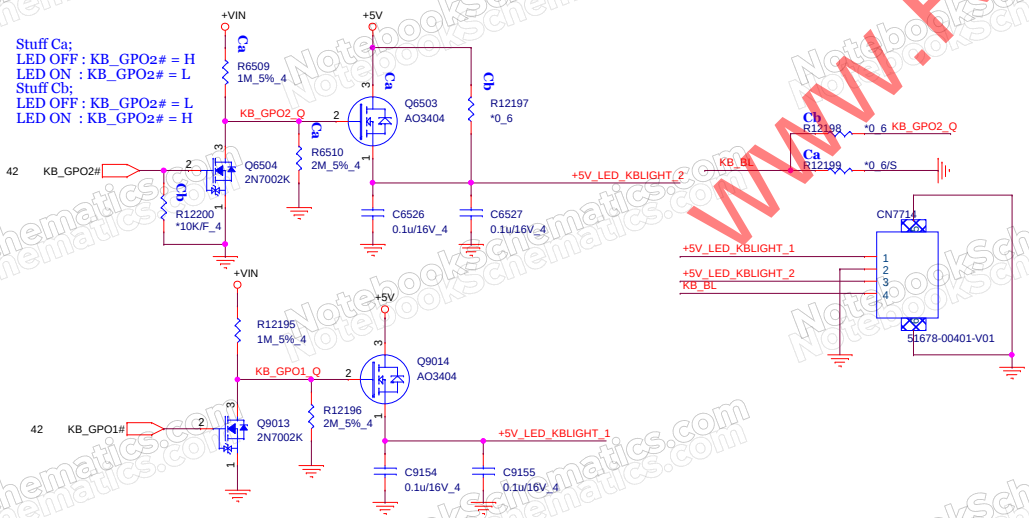
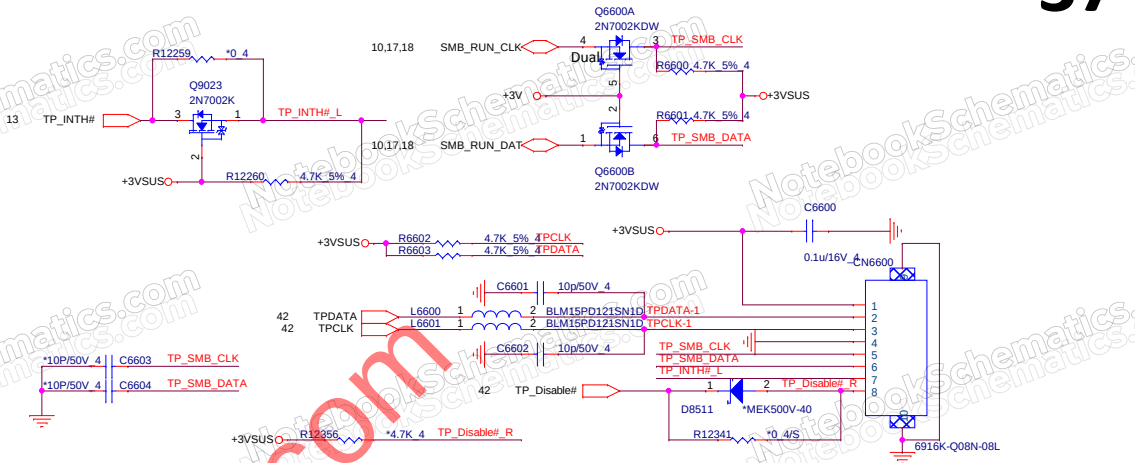
KEYBOARD Con.



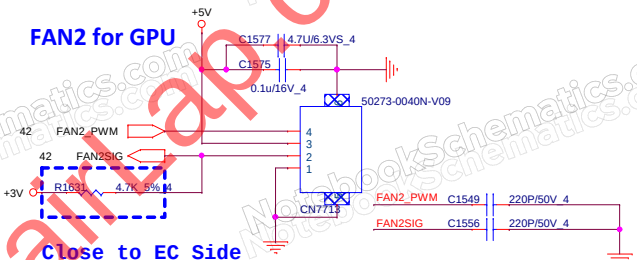
KEYBOARD BACKLIGHT Con.



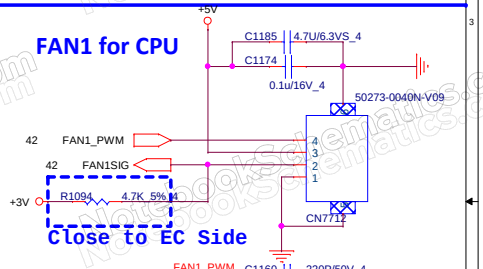
Touch Pad Connector AA type

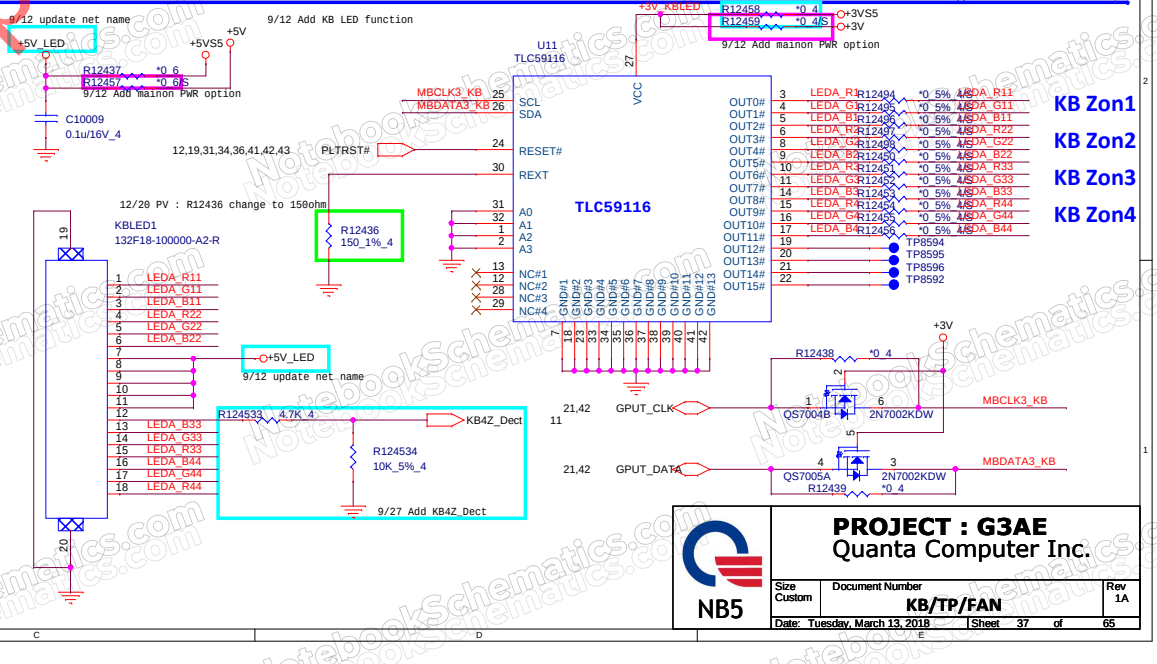


FAN2 for GPU



FAN1 for CPU





NB5	PROJECT : G3AE Quanta Computer Inc.		
Size: Custom	Document Number: KB/TP/FAN		Rev: 1A
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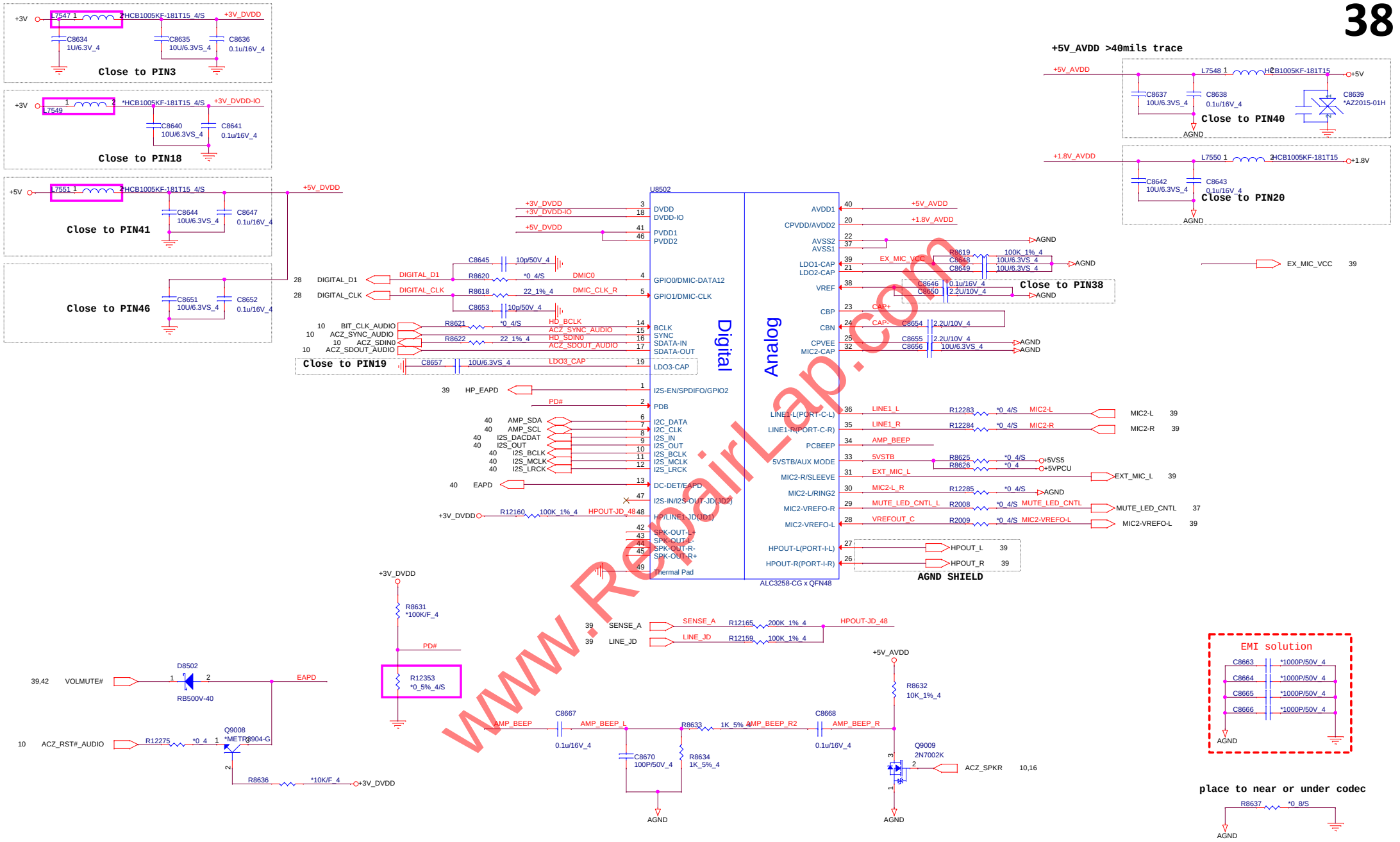
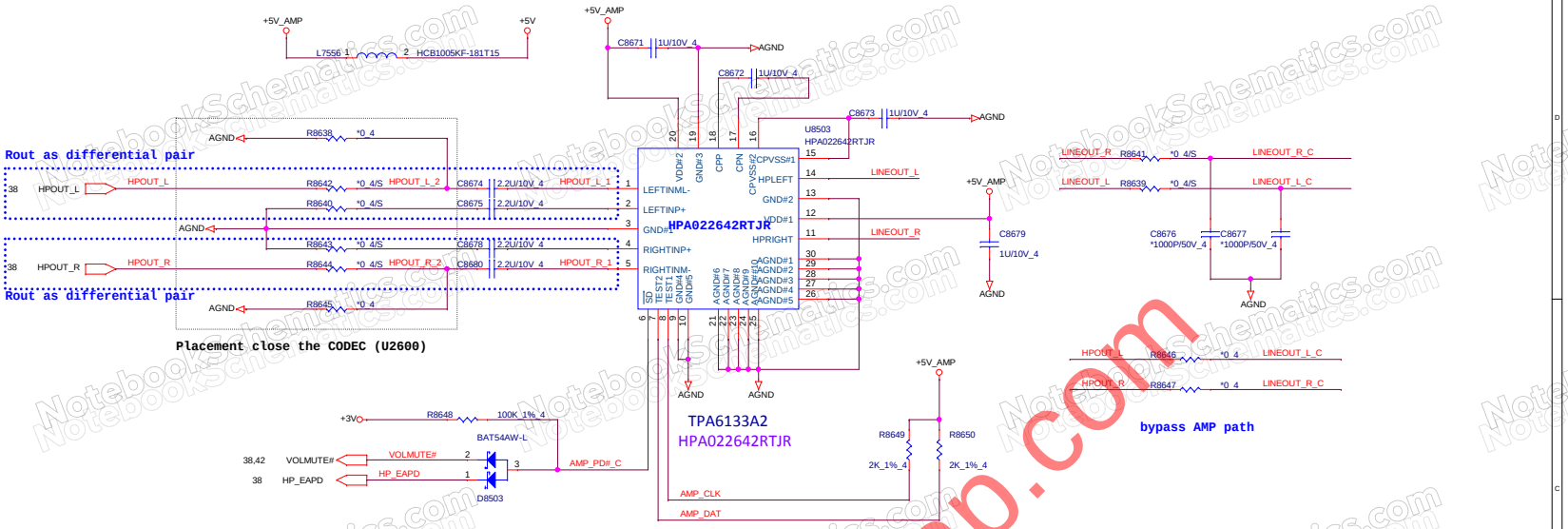
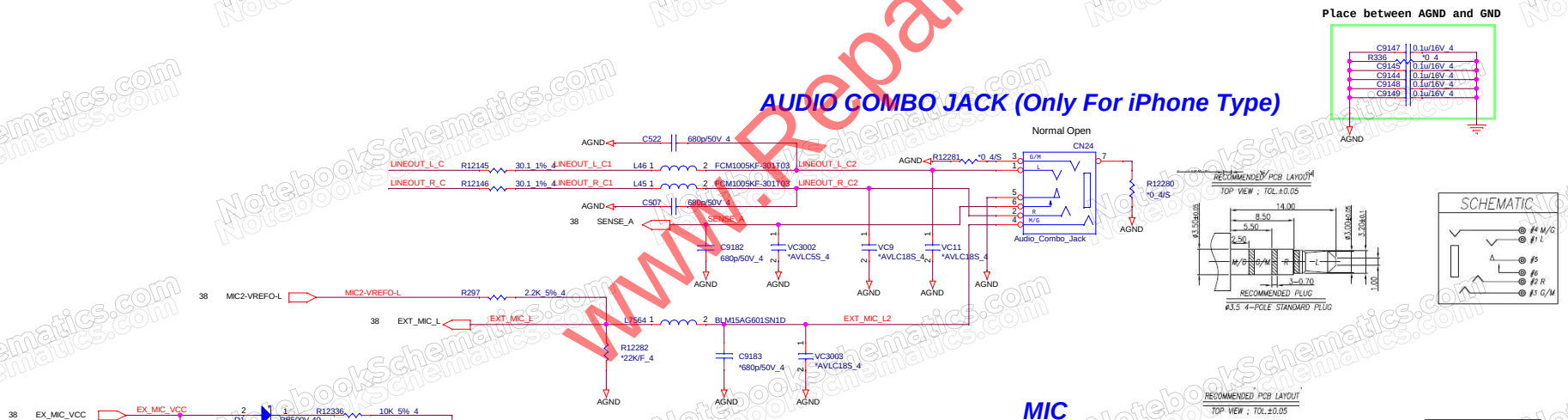


Head Phone out

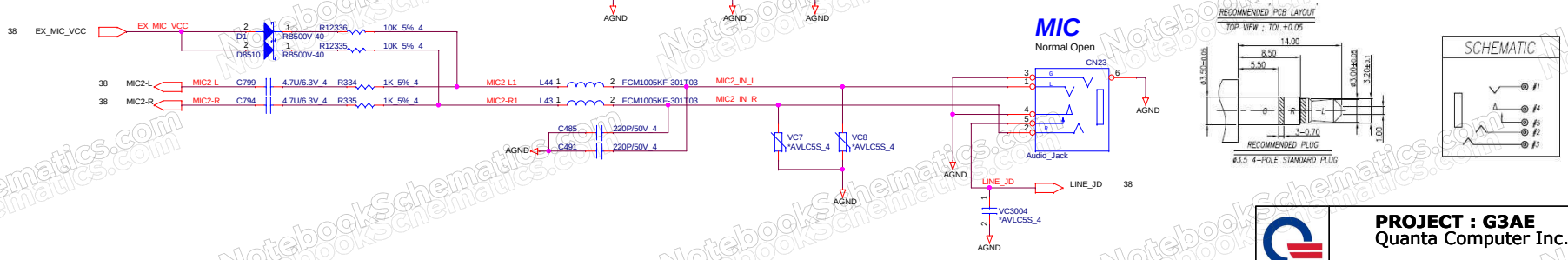


Combo Jack& Mic Jack

AUDIO COMBO JACK (Only For iPhone Type)



MIC



NB5	PROJECT : G3AE Quanta Computer Inc.	
Size: Custom	Document Number: HP AMP/Combo & MIC Jack	Rev: 1A
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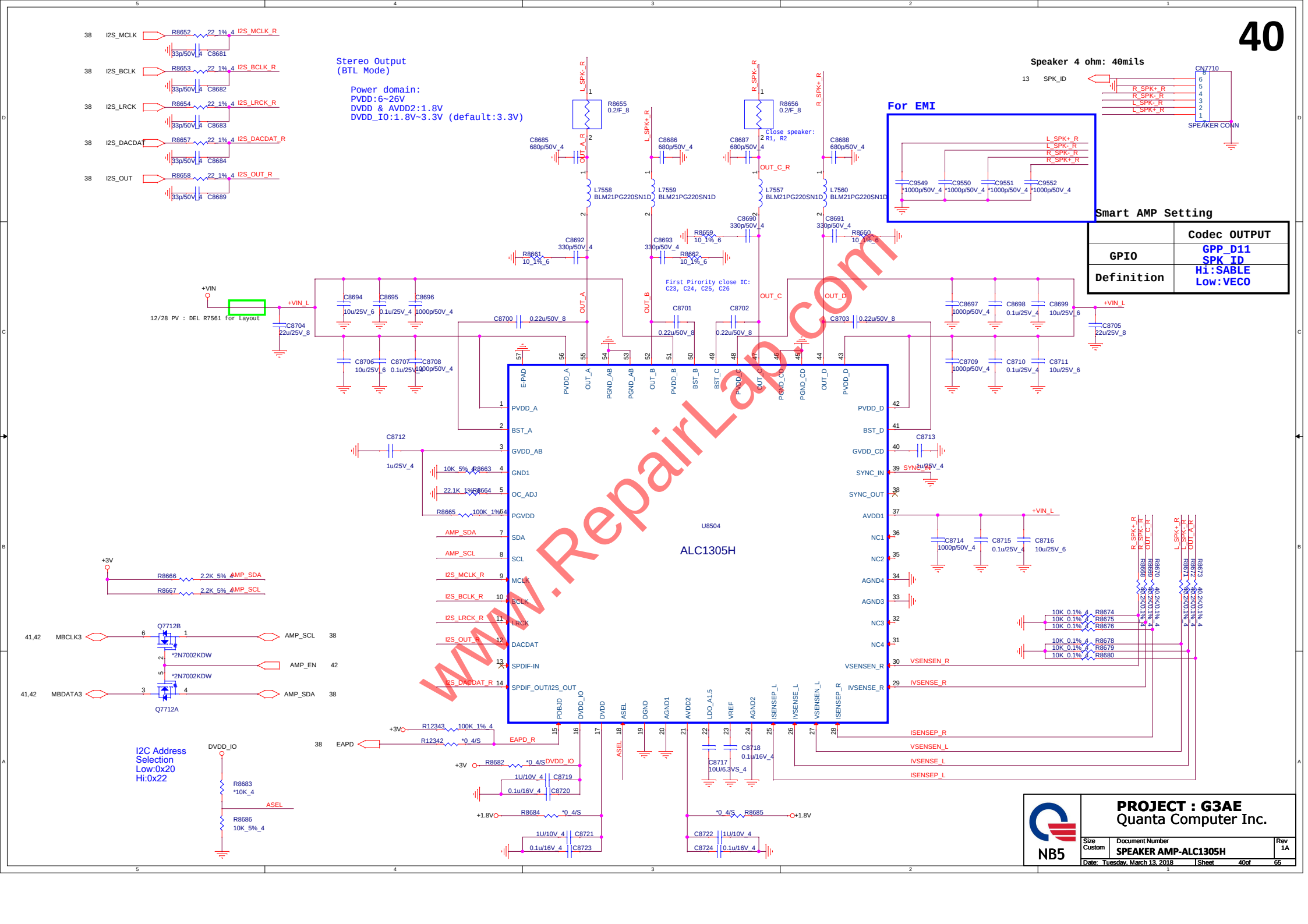
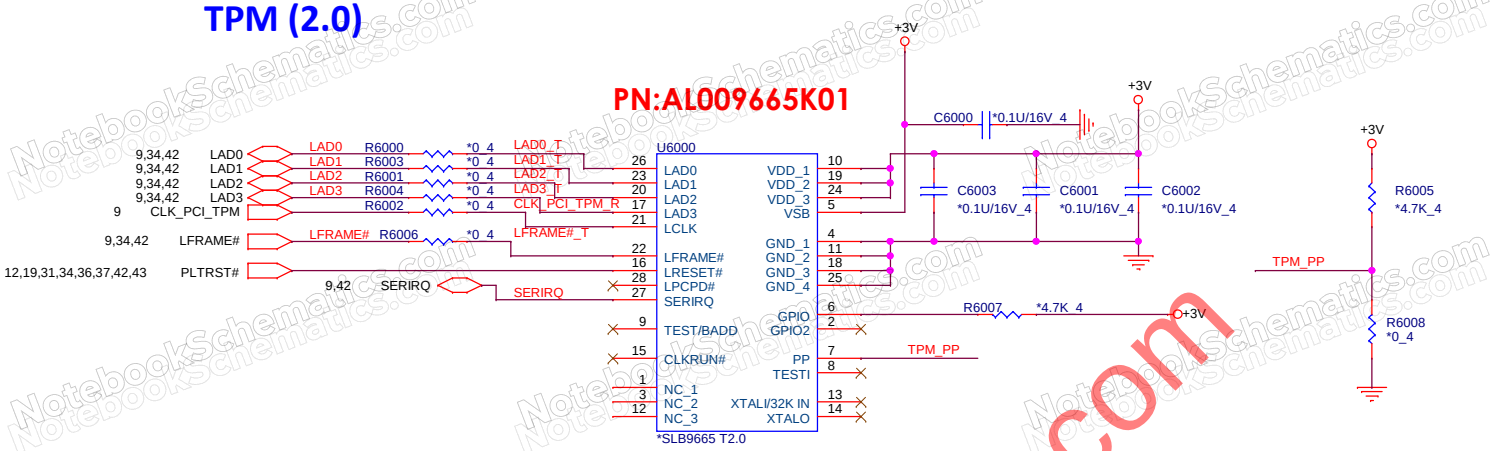
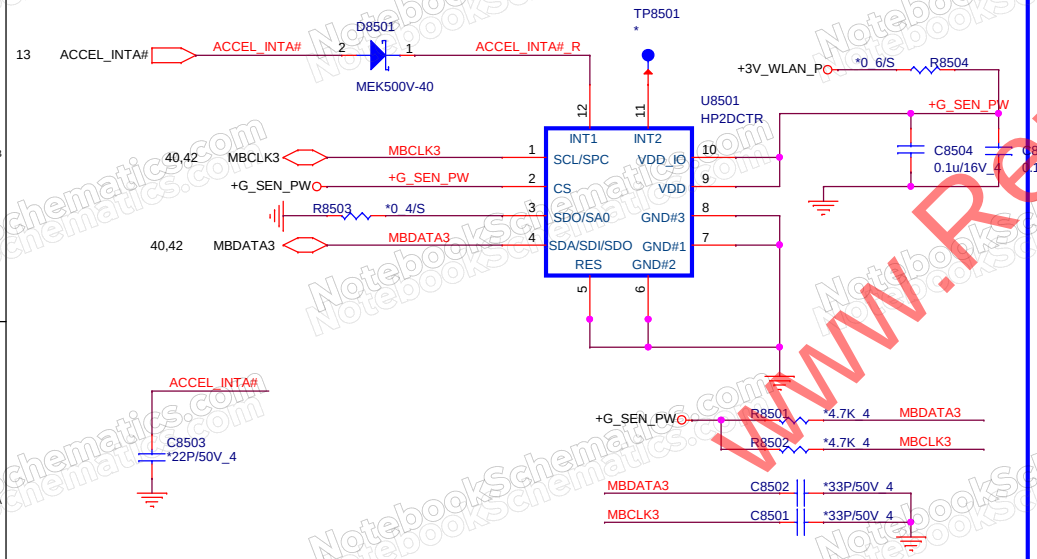


TPM (2.0)

PN:AL009665K01



Accelerometer Sensor



LED Bar

7/13 Remove LED Bar Schematic

Custom NB5	PROJECT : G3AE Quanta Computer Inc.	
	Size / Document Number: TPM/G-Sensor/LED Bar	Rev 1A
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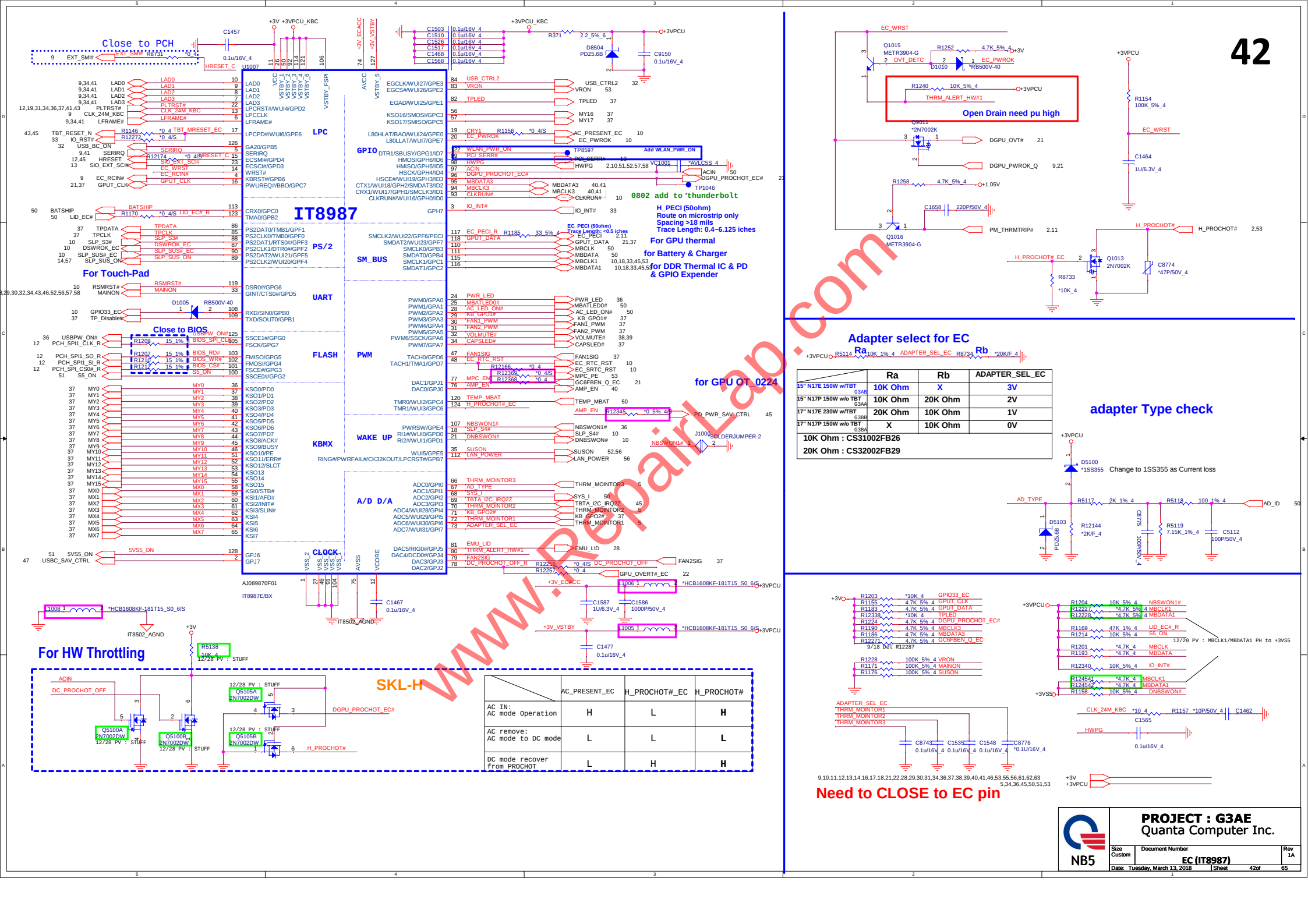


	Ra	Rb	ADAPTER_SEL_EC
15" N17E 150W w/TBT G3AB	10K Ohm	X	3V
15" N17P 150W w/o TBT G3AA	10K Ohm	20K Ohm	2V
17" N17E 230W w/TBT G3BB	20K Ohm	10K Ohm	1V
17" N17P 150W w/o TBT G3BA	X	10K Ohm	0V

10K Ohm : CS31002FB26
20K Ohm : CS32002FB29

	AC_PRESENT_EC	H_PROCHOT#_EC	H_PROCHOT#
AC IN: AC mode Operation	H	L	H
AC remove: AC mode to DC mode	L	L	L
DC mode recover from PROCHOT	L	H	H

25MHz, 30ppm, 20pF AR Crystal

C2041 6.8P/50V_4
Y1002 25MHZ/10ppm
TBT_XTAL_25_IN
TBT_XTAL_25_OUT
C2040 6.8P/50V_4

8Mbit Flash (Mutual for AR and ACE)

+VCC3P3_SX R1341 *0_4/S
R1336 3.32K_1% R1337 43.32K_1% R1338 43.32K_1%_4
C1727 0.1u/10V_2
R1340 3.32K_1%_4
U1011 W25Q80DVSSIG
TBT_EE_CS_N TBT_EE_DO TBT_EE_WP_N
TBT_HOLD_N TBT_EE_CLK TBT_EE_DI
AKE3GGN0N00
IC FLASH (8P)W25Q80DVSSIG (SOIC)
Silk: "NVM"

SPI/EE: AR to/from NVM & ACE

AR_DDC_CLK R1299 *2.2K_2
AR_DDC_DAT R1291 *2.2K_2
TBT_HDMI_DDC_DATA R1699 *2.2K_5%_2
TBT_HDMI_DDC_CLK R1703 *2.2K_5%_2
SI : No stuff R1699,R1703
TBT_FORCE_PWR R12449 10K_1%_2 SI : Add R12445,R12449 PD
TBTB_I2C_INT R12445 10K_1%_2
TBT_CIO_PLUG_EVENT R1318 10K_1%_2
TBT_I2C_SDA R1705 2.2K_5%_2
TBT_I2C_SCL R1704 2.2K_5%_2
TBTA_I2C_INT R1296 10K_1%_2
TBT_RESET_N R12273 10K/F_2
VCC3P3_S0
+VCC3P3_SX
SI : Add R12447 , R12448 100k PD
TBT_HDMI_DDC_DATA R12448 100K_1%_2
TBT_HDMI_DDC_CLK R12447 100K_1%_2
TBTA_ACE_GPIO0 R1284 100K_1%_2
AR_DDC_CLK R12333 100K_1%_2
AR_DDC_DAT R12334 100K_1%_2
TBT_SNK1_DDC_CLK R1276 100K_1%_2
AR_DDC_EN R1294 100K_1%_2
TBT_FORCE_PWR R1297 *10K_1%_2 SI : No stuff R1297
TBT_TMU_CLK_OUT R1700 100K_1%_2
DDI1_HPD0 R1302 100K_1%_2
TBTA_LSTX R1679 1M_1%_2
TBTA_HPD R1293 100K_1%_2
TBTA_LSRX R1680 1M_1%_2
TBTB_ACE_GPIO0 R12446 100K_1%_2 SI : Add R12446 PD

TBT_SRC_CFG1 = 0 , AUX CONNECTS TO AR
TBT_SRC_CFG1 = 1 , ddc CONNECTS TO AR

TBT_GPIO8 R1702 *10K/F_2 +3VS5
SI : net name update

NOTE:
ASSEMBLE R548, R549 if DPSRC
NOT IN USE

TBT_GPIO8 R1701 1M_1%_2
SI : net name update

0816 TypeC2_DDI2_HPD

IF SOME OF GPIOs ARE NOT IN USE FOLLOW TABLE BELOW:

GPIO	TERMINATION	Power Rail
GPIO_0	10K PU	VCC3V3_LC
GPIO_1	10K PU	VCC3V3_LC
GPIO_2	100K PD	
GPIO_3	100k PD	
GPIO_4	10K PU	VCC3V3_LC
GPIO_5	10K PU	VCC3V3_LC
GPIO_6	100K PD	
GPIO_7	100K PD	
GPIO_8	100K PD	
POC_GPIO_0	10K PU	VCC3V3_TBT_SX
POC_GPIO_1	10K PU	VCC3V3_TBT_SX
POC_GPIO_2	100K PD	
POC_GPIO_3	100K PD	
POC_GPIO_4	10K PU	VCC3V3_TBT_SX
POC_GPIO_5	10K PU	VCC3V3_TBT_SX
POC_GPIO_6	100K PD	

NOTE:
SNK0_DDC_data/clk ?connect to 2k PU only if SRC0 is connected and support HDMI (a.i HDMI or DP++ connector). Otherwise can be 100k PD.
SNK1_DDC_data ?connect to 100k PD. If SRC0 support HDMI, connect as SNK0_CFG1 to GPU and/or appropriate AUX/DDC demux control
SNK1_DDC_clk ?connect to 100k PD.

JS-1007 Change to 4 lan

CPU PCIE TX
PCIE_TXP1_TBT PCIE_TXN1_TBT
PCIE_TXP2_TBT PCIE_TXN2_TBT
PCIE_TXP3_TBT PCIE_TXN3_TBT
PCIE_TXP4_TBT PCIE_TXN4_TBT
CLK_PCIE_TBTP CLK_PCIE_TBTN PCIE_CLKREQ_TBT#
OUT_DP_TXP0_TBT OUT_DP_TXN0_TBT
OUT_DP_TXP1_TBT OUT_DP_TXN1_TBT
OUT_DP_TXP2_TBT OUT_DP_TXN2_TBT
OUT_DP_TXP3_TBT OUT_DP_TXN3_TBT
DP_AUXP_TBT DP_AUXN_TBT
C1664 0.1u/10V_2 C1676 0.1u/10V_2
DDI1_HPD0

PCIe GEN3
PCIE_RX0_P PCIE_RX0_N
PCIE_RX1_P PCIE_RX1_N
PCIE_RX2_P PCIE_RX2_N
PCIE_RX3_P PCIE_RX3_N
PCIE_REFCLK_100_IN_P PCIE_REFCLK_100_IN_N PCIE_CLKREQ_N
PERST_N
PCIE_RBIAS R1255 3.01K_1%_4

PCIE_TX0_P PCIE_TX0_N C2150 0.22u/6.3V_2 C2151 0.22u/6.3V_2
PCIE_TX1_P PCIE_TX1_N C2152 0.22u/6.3V_2 C2153 0.22u/6.3V_2
PCIE_TX2_P PCIE_TX2_N C2035 0.22u/6.3V_2 C2036 0.22u/6.3V_2
PCIE_TX3_P PCIE_TX3_N C2034 0.22u/6.3V_2 C2033 0.22u/6.3V_2
CPU PCIE RX
PLTRST# 12,19,31,34,36,37,41,42

SINK PORT 0
DPSNK0_ML0_P DPSNK0_ML0_N
DPSNK0_ML1_P DPSNK0_ML1_N
DPSNK0_ML2_P DPSNK0_ML2_N
DPSNK0_ML3_P DPSNK0_ML3_N
DPSNK0_AUX_P DPSNK0_AUX_N
DPSNK0_HPD
DPSNK0_DDC_CLK DPSNK0_DDC_DATA

SOURCE PORT 0
DPSRC_ML0_P DPSRC_ML0_N
DPSRC_ML1_P DPSRC_ML1_N
DPSRC_ML2_P DPSRC_ML2_N
DPSRC_ML3_P DPSRC_ML3_N
DPSRC_AUX_P DPSRC_AUX_N
DPSRC_HPD
DPSRC_RBIAS R1281 14K_1%_4
SI : R1312 change to 1M ohm R1312 1M_1%_2

SINK PORT 1
DPSNK1_ML0_P DPSNK1_ML0_N
DPSNK1_ML1_P DPSNK1_ML1_N
DPSNK1_ML2_P DPSNK1_ML2_N
DPSNK1_ML3_P DPSNK1_ML3_N
DPSNK1_AUX_P DPSNK1_AUX_N
DPSNK1_HPD
DPSNK1_DDC_CLK DPSNK1_DDC_DATA
DPSNK_RBIAS R1271 14K_1%_4

GPIO LC GPIO
GPIO_0 TBT_I2C_SDA
GPIO_1 TBT_I2C_SCL
GPIO_2 TBT_TMU_CLK_OUT
GPIO_3 PCIE_WAKE#
GPIO_4 TBT_CIO_PLUG_EVENT
GPIO_5 TBT_HDMI_DDC_DATA
GPIO_6 TBT_HDMI_DDC_CLK
GPIO_7 TBT_GPIO8
GPIO_8
TBT_I2C_SDA 45
TBT_I2C_SCL 45
PCIE_WAKE# 10,31,36
SI : net name update

POC GPIO
POC_GPIO_0 TBTB_I2C_INT
POC_GPIO_1 TBTA_ACE_GPIO0
POC_GPIO_2
POC_GPIO_3 TBT_FORCE_PWR
POC_GPIO_4 BATLOW#
POC_GPIO_5 MAINON
POC_GPIO_6
TBTB_I2C_INT 45
TP1059
TBT_FORCE_PWR 9
R1697 *0_2/S BATLOW# 10
R1711 *0_2/S MAINON 28,29,30,32,34,42,46,52,56,57,58
TP1053

Misc
TEST_EN R1698 100_1%_2
TEST_PWR_GOOD R1681 100_1%_2
RESET_N
TBT_TEST_EN
TBT_TEST_PWG
TBT_RESET_N 42,45

MISC
TDI TMS TCK TDO
RBIAS R1283 4.75K_0.5%_4 +/-0.5%
RSENSE
XTAL_25_IN TBT_XTAL_25_IN
XTAL_25_OUT TBT_XTAL_25_OUT
EE_DI TBT_EE_DI
EE_DO TBT_EE_DO
EE_CS_N TBT_EE_CS_N
EE_CLK TBT_EE_CLK

TBT PORT A
TBTA_CA2HD_1_P C10539 0.33u/6.3V_2 TBTA_RX1_P R12482 2.2_5%_2
TBTA_CA2HD_1_N C10540 0.33u/6.3V_2 TBTA_RX1_N R12483 2.2_5%_2
TBTA_HD2CA_1_P C2048 0.22U/6.3V_2 TBTA_TX1_P R12484 2.2_5%_2
TBTA_HD2CA_1_N C2047 0.22U/6.3V_2 TBTA_TX1_N R12485 2.2_5%_2
TBTA_HD2CA_0_P C2043 0.22U/6.3V_2 TBTA_TX0_P R12486 2.2_5%_2
TBTA_HD2CA_0_N C2042 0.22U/6.3V_2 TBTA_TX0_N R12487 2.2_5%_2
TBTA_CA2HD_0_P C10541 0.33u/6.3V_2 TBTA_RX0_P R12488 2.2_5%_2
TBTA_CA2HD_0_N C10542 0.33u/6.3V_2 TBTA_RX0_N R12489 2.2_5%_2
TBTA_DPSRC_AUX_P C1620 0.1u/10V_2
TBTA_DPSRC_AUX_N C1632 0.1u/10V_2
TBTA_LSTX
TBTA_LSRX
TBTA_HPD
R1254 499_1%_4 PA_USB2_RBIAS

Port A
PA_RX1_P PA_RX1_N
PA_TX1_P PA_TX1_N
PA_TX0_P PA_TX0_N
PA_RX0_P PA_RX0_N
PA_DPSRC_AUX_P PA_DPSRC_AUX_N
PA_USB2_D_P PA_USB2_D_N
PA_LSTX PA_LSRX PA_DPSRC_HPD
PA_USB2_RBIAS

TBT PORTS
POC

PORT B
PB_RX1_P PB_RX1_N
PB_TX1_P PB_TX1_N
PB_TX0_P PB_TX0_N
PB_RX0_P PB_RX0_N
PB_DPSRC_AUX_P PB_DPSRC_AUX_N
PB_USB2_D_P PB_USB2_D_N
PB_LSTX PB_LSRX PB_DPSRC_HPD
PB_USB2_RBIAS R1253 499_1%_4
SI : Add R12442,R12443,R12444
PB_LSTX R12444 1M_1%_2
PB_LSRX R12443 1M_1%_2
PB_DPSRC_HPD R12442 100K_1%_2

DEBUG
THERMDA
PCIE_ATEST
TEST_EDM
FUSE_VQPS_64 FUSE_VQPS_128
MONDC_CIO_0 MONDC_CIO_1
MONDC_SVR
ATEST_P ATEST_N
USB2_ATEST
MONDC_DPSNK_0 MONDC_DPSNK_1 MONDC_DPSRC
U1030A AR_4C

DEBUG PINs:

PIN	TERMINATION
MONDC_SVR	GND
MONDC_DPSNK_0	GND
MONDC_DPSNK_1	GND
MONDC_DPSRC	GND
MONDC_CIO_0	GND
MONDC_CIO_1	GND
TEST_EDM	GND
FUSE_VQPS_64	GND
FUSE_VQPS_128	GND
ATEST_P/N	FLOATING
USB2_ATEST	FLOATING
PCIE_ATEST	FLOATING

0805 Modify
0822 MOdify

For ICT test
TBT_EE_DI TP8532
TBT_EE_DO TP8533
TBT_EE_CS_N TP8531
TBT_EE_CLK TP8534
TBT_EE_WP_N TP8535

D1015 MEK500V-40 TBT_HTPLG 12

TBT_CIO_PLUG_EVENT_N:
Connect to PCH (Make sure PCH supports SCI)

TBT_EE_CLK
EC1046 *10P/50V_4

SI Add
BATLOW# R1710 *10K_1%_2 +VCC3P3_SX
8/7 no stuffR1710

D8514 D8516 D8518 D8517 D8520 D8519 D8513 D8515
ESD101-B1-02ELS
TBTA_RX1_P TBTA_RX1_N TBTA_TX1_P TBTA_TX1_N TBTA_TX0_P TBTA_TX0_N TBTA_RX0_P TBTA_RX0_N
TBTA_CA2HD_1_P R12490 220K_5%_2
TBTA_CA2HD_1_N R12491 220K_5%_2
TBTA_CA2HD_0_P R12492 220K_5%_2
TBTA_CA2HD_0_N R12493 220K_5%_2

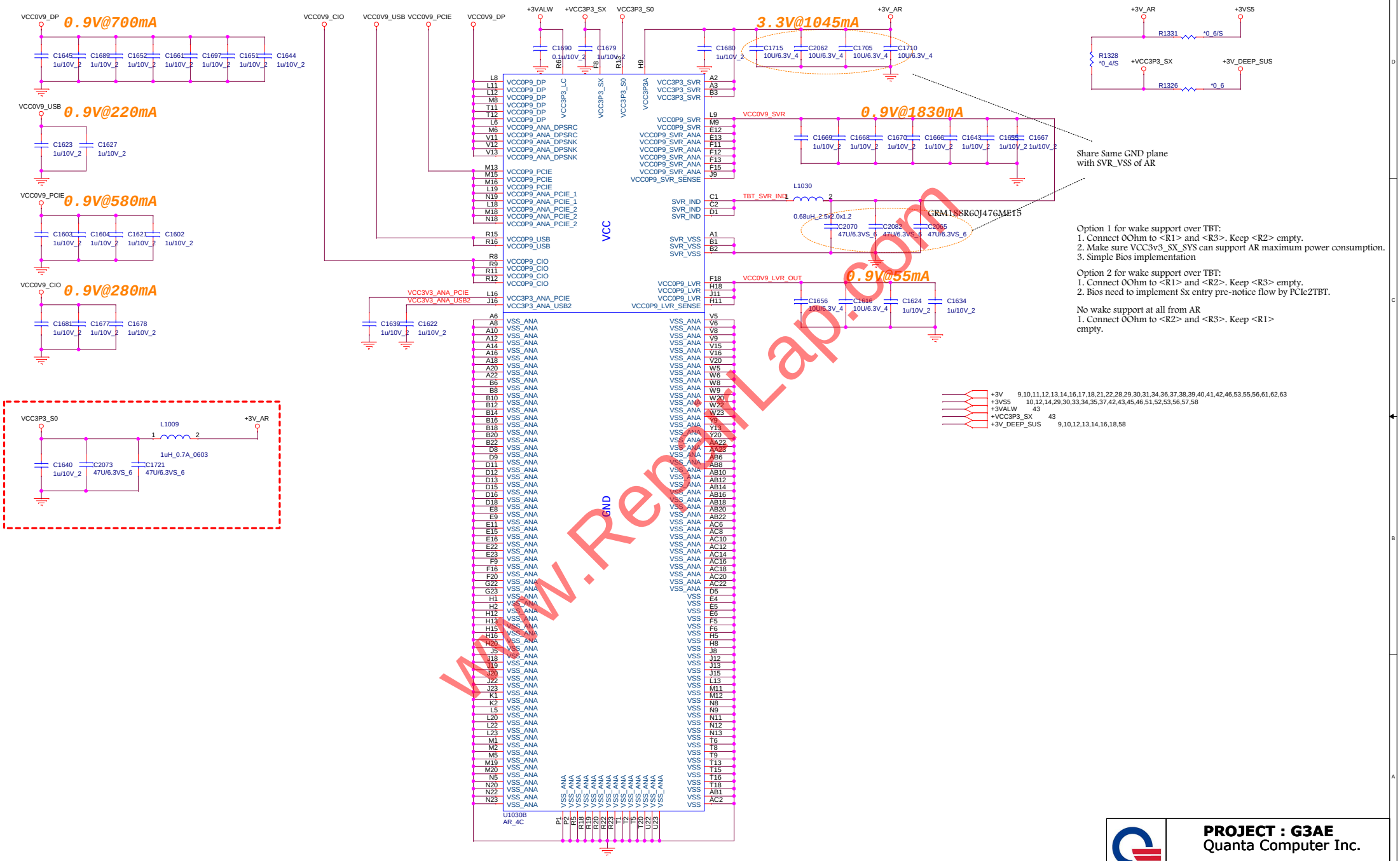
JTAG
+3VALW
TBT_TDI R1300 10K_1%_2
TBT_TMS R1298 10K_1%_2
TBT_TCK R1295 10K_1%_2
TBT_TDO R1301 10K_1%_2

+3V 9,10,11,12,13,14,16,17,18,21,22,28,29,30,31,34,36,37,38,39,40,41,42,46,53,55,56,61,62,63
+3VS5 10,12,14,29,30,33,34,35,37,42,44,45,46,51,52,53,56,57,58
+3VALW 44
+VCC3P3_SX 44

NB5

PROJECT : G3AE
Quanta Computer Inc.

Size	Document Number	Rev
	Alpine Ridge _TBT	1A
Date: Tuesday, March 13, 2018	Sheet 43 of 65	

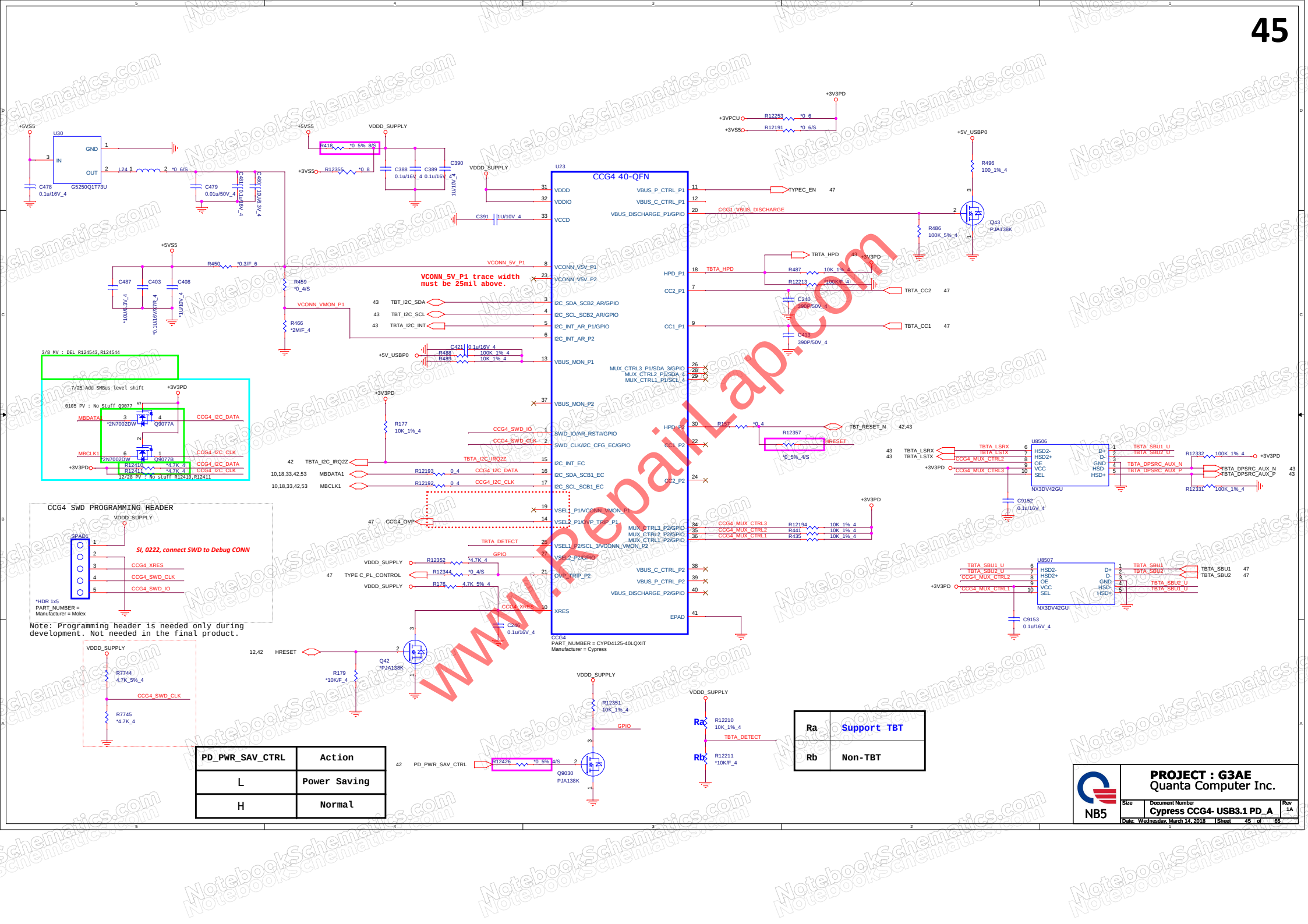


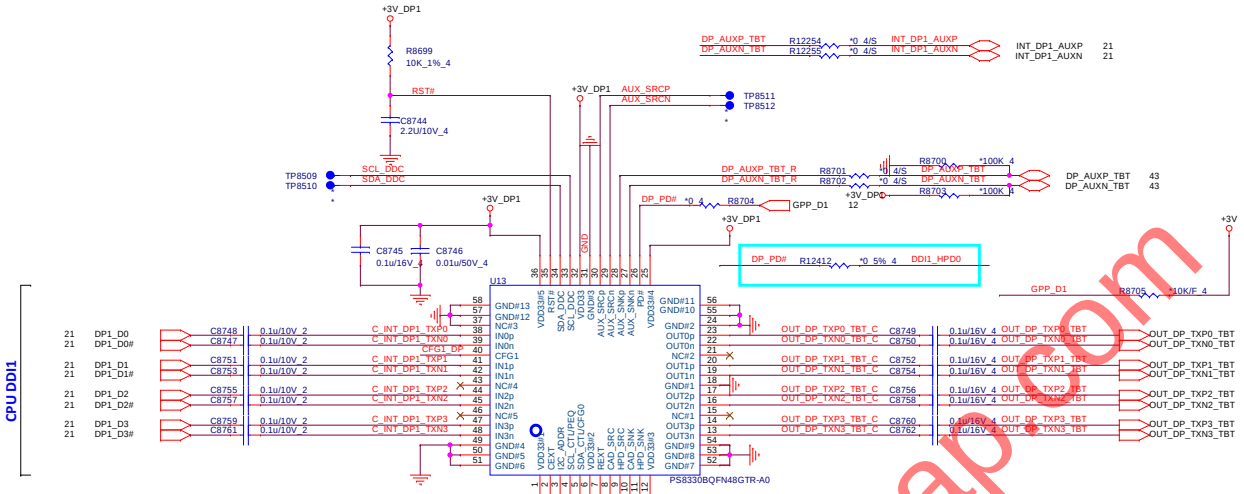
NB5

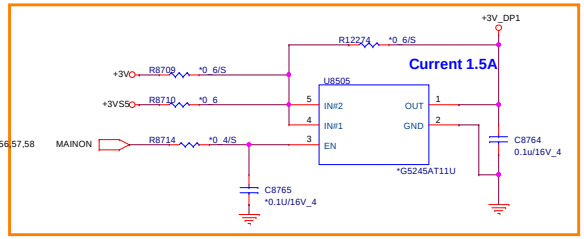
PROJECT : G3AE
Quanta Computer Inc.

Size	Document Number	Rev
	Alpine Rideg_Power	1A

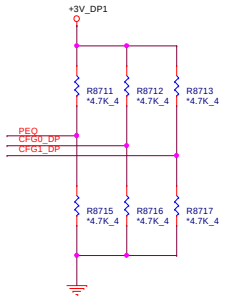
Date: Tuesday, March 13, 2018 Sheet 44 of 65







PS8330 strap pin



PEQ
Programmable input equalization levels; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, LEQ, compensate channel loss up to 12dB @ HBR2
H: HEQ, compensate channel loss up to 15dB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2

CFG0_DP
Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

CFG1_DP
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K
H: default, auto test disable & input offset cancellation enable
L: auto test enable & input offset cancellation enable
M: auto test disable & input offset cancellation disable

NB5	PROJECT : G3AE Quanta Computer Inc.	
Size: Custom	Document Number: DP Redriver for TBT	Rev: 1A
Date: Tuesday, March 13, 2018	Sheet 46 of 65	

+5VS5 10,29,32,36,37,38,45,51,52,56,57,58,59,61,62
+5V_USBP0 45

0604 update PN as BC0101B1Z01
0503 update FP as d-0_62x0_32-0_32h

Note : R12214/R12215/R12216/R12217 Close to CN7715

CN7715
UT11123-11501-7H

D1032 P4SMAJ20A

C1691 0.47u/25V_4
C1704 0.47u/25V_4
C1707 0.47u/25V_4
C1701 0.47u/25V_4

R12214 *0_5%_4/S
R12215 *0_5%_4/S

TBTA_HD2CA_0_P
TBTA_HD2CA_0_N
TBTA_CA2HD_0_P
TBTA_CA2HD_0_N
TBTA_HD2CA_1_N
TBTA_HD2CA_1_P
TBTA_CA2HD_1_N
TBTA_CA2HD_1_P
TBTA_USB2_D_P_R
TBTA_USB2_D_N_R
TBTA_SBU1
TBTA_SBU2
TBTA_CC1
TBTA_CC2
USBP4+
USBP4-

C10007 AZ5315-02F.R7G

TBTA_CC1 D1014 PESD5V0H1BSF
TBTA_CC2 D1029 PESD5V0H1BSF
TBTA_SBU1 D1027 PESD5V0H1BSF
TBTA_SBU2 D1028 PESD5V0H1BSF

9/27 DEL TVS

U28 TPS2592BADRCR

R555 *10K/F_4
R553 *0_4
R556 1M_1%_4
R552 *10K/F_4
R554 470K_5%_4
C450 *10U/6.3V_4
C451 1U/6.3V_4
C452 0.1u/16V_4
C453 0.022u/25V_4
R241 100K_1%_4

D22 RB500V-40
D7704 *RB500V-40
R7735 *10K/F_4

Q53 AON7400AL
R242 1M_1%_4
C284 0.01u/50V_4
Q52 BSS84
R7736 1K_1%_4
Q55 PMBT3906YS
R245 200K_1%_4
D7705 UDZ15B-7-F
R564 200K_1%_4
D24 PDZ5.1B
R563 47K_1%_4
R557 20K_1%_4
R561 4.99K_1%_4
Q20 2N7002K
C455 470P/50V_4
R558 1K_1%_4
R560 15K_1%_4

TYPE C_PL_CONTROL	ILIM
L	3.7A
H	1.75A

R12348 *36K/F_4
R12427 *0_5%_4
R12428 *0_5%_4
R12349 *100K/F_4
Q9029 *2N7002K
12/28 PV : NO STUFF

NB5

PROJECT : G3AE
Quanta Computer Inc.

Size	Document Number	Rev
	USB TYPE-C_Port A	1A

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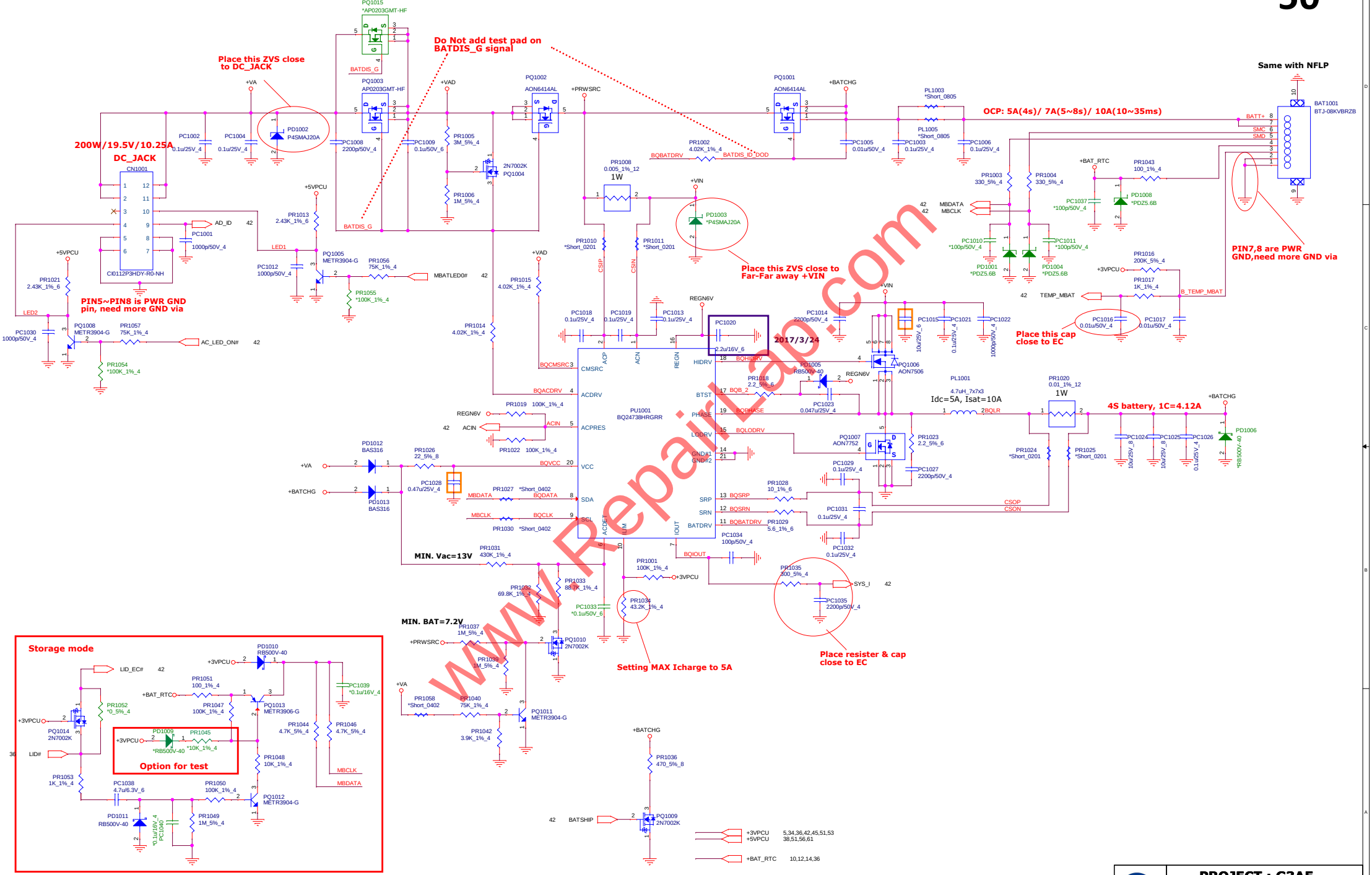
NB5

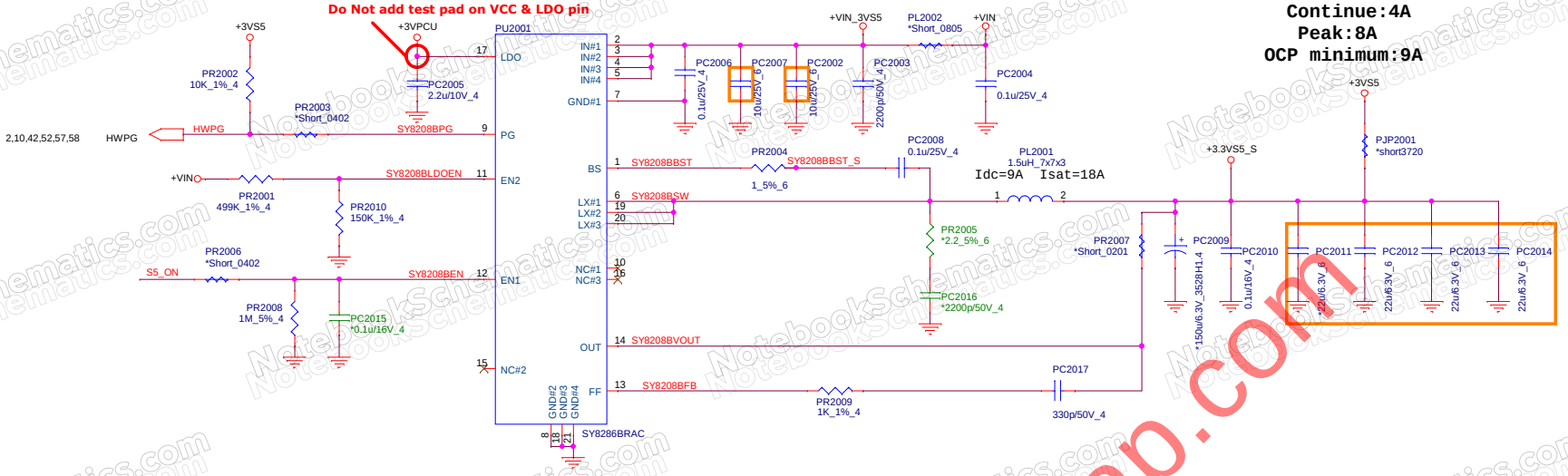
PROJECT : G3AE
Quanta Computer Inc.

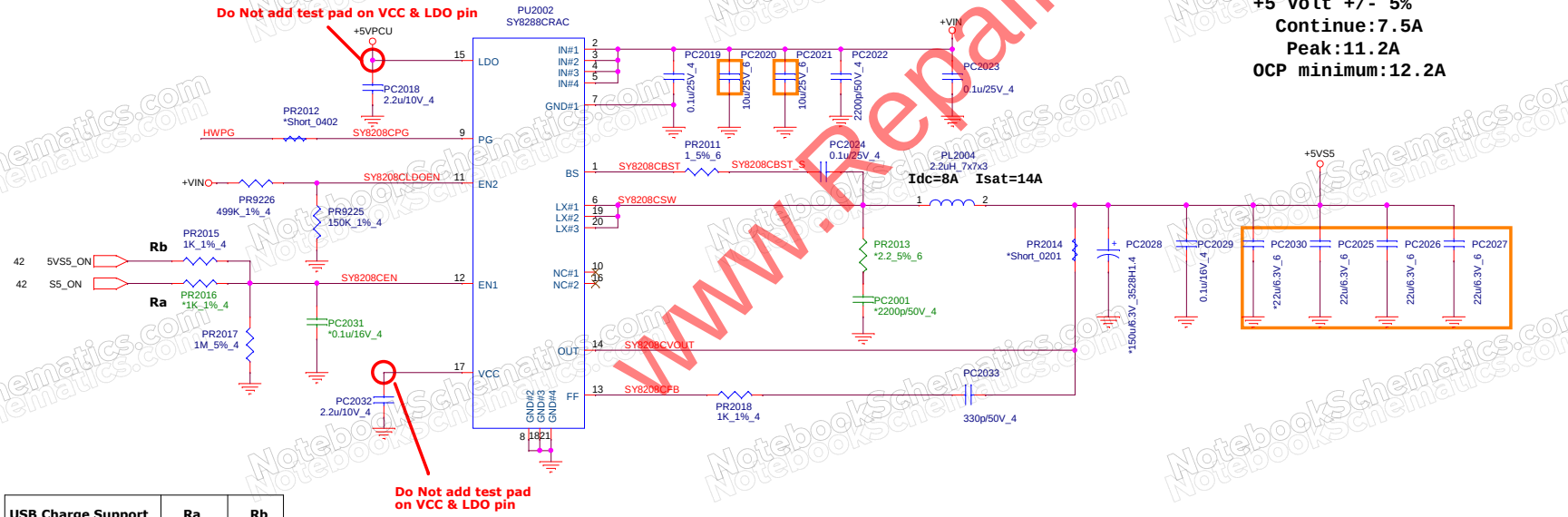
Size	Document Number	Rev
Custom	Thunderbolt & Type C2(NA)	

Date: Tuesday, March 13, 2018 Sheet 49 of 65



NB5	PROJECT : G3AE Quanta Computer Inc.	
Size: Custom	Document Number: Charger (BQ24738H)	Rev: 1A
Date: Tuesday, March 13, 2018	Sheet: 50 of 65	





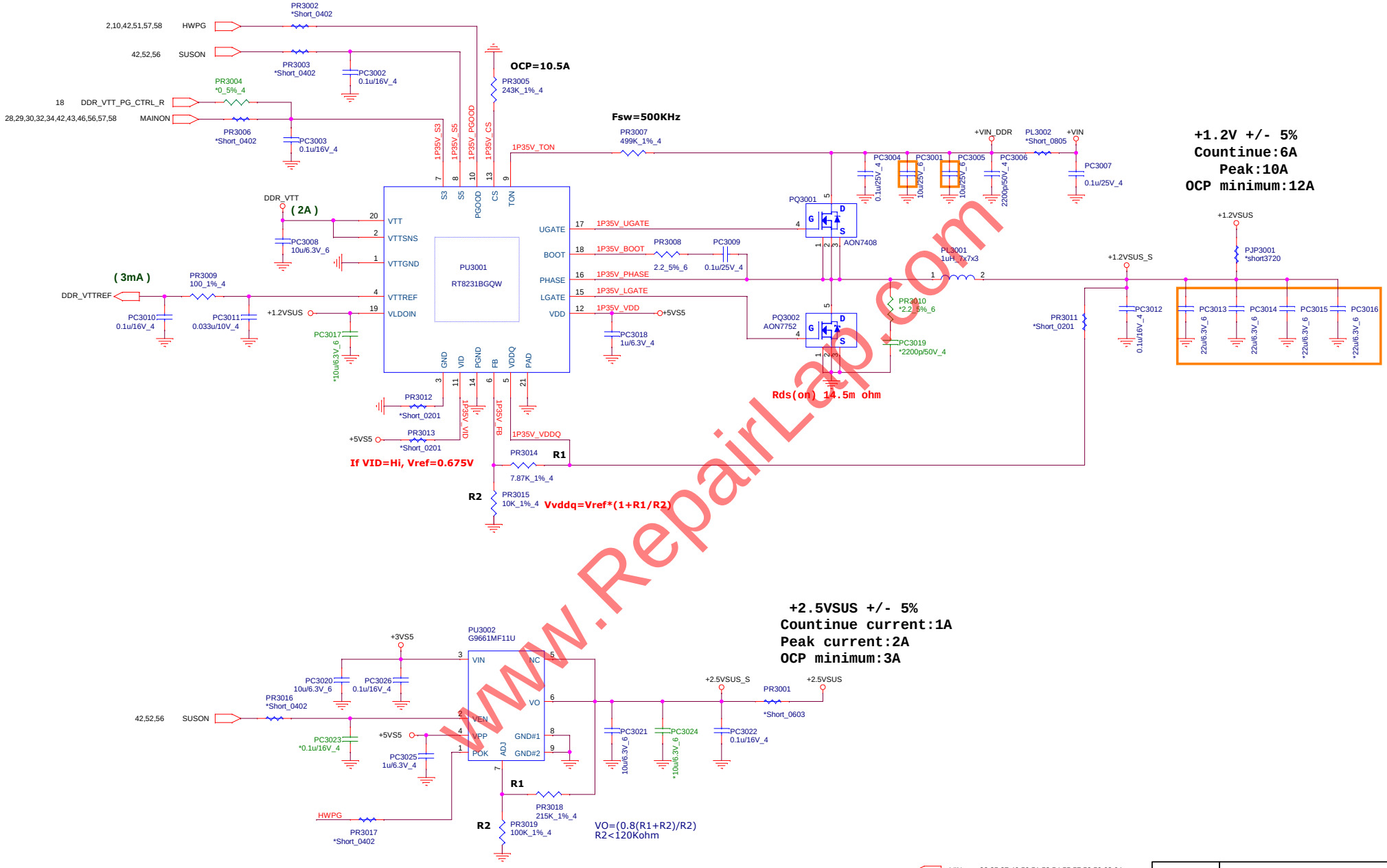
USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

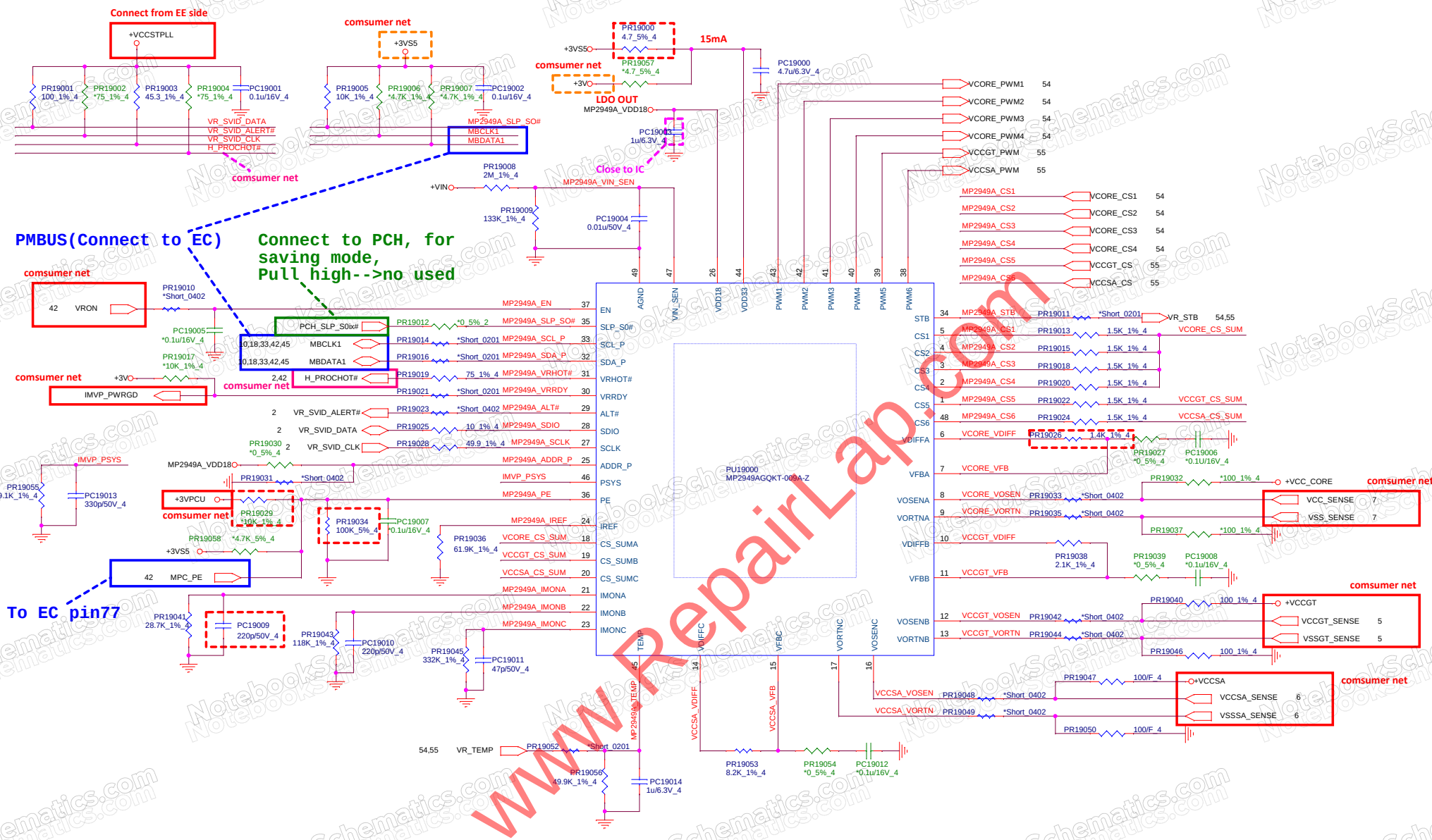
+VIN	28,35,37,40,50,52,53,54,55,57,58,59,62,64
+3VS5	10,12,14,29,30,33,34,35,37,42,43,44,45,46,52,53,55,56,57,58
+5VS5	10,29,32,35,36,37,38,45,47,52,54,56,57,58,59,61,62
+3VPCU	5,34,36,42,45,50,53
+5VPCU	38,50,56,61

NB5

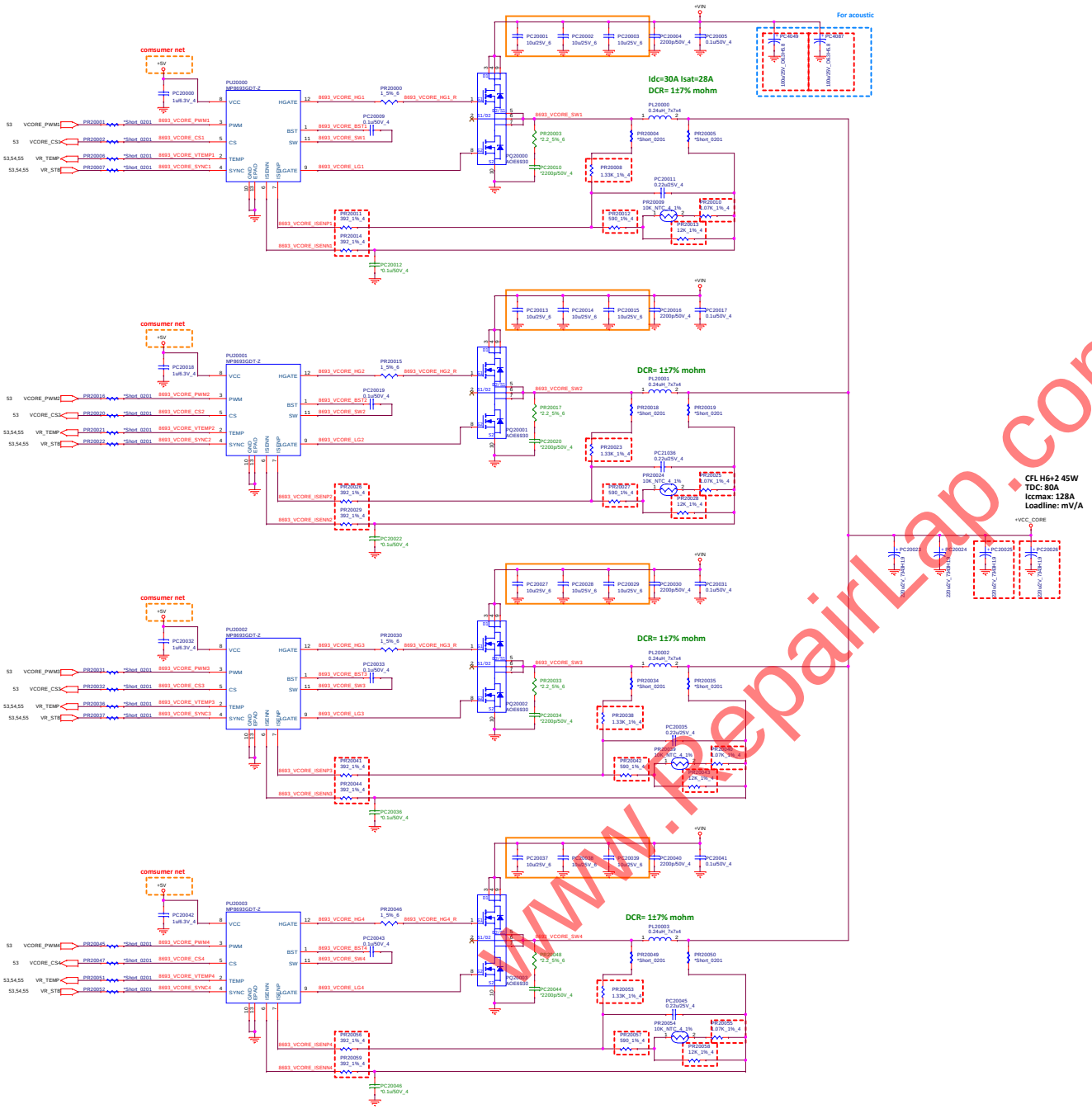
PROJECT : G3AE
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VS5 (SY8208B/SY8208C)	1A
Date: Tuesday, March 13, 2018	Sheet 51 of 65	

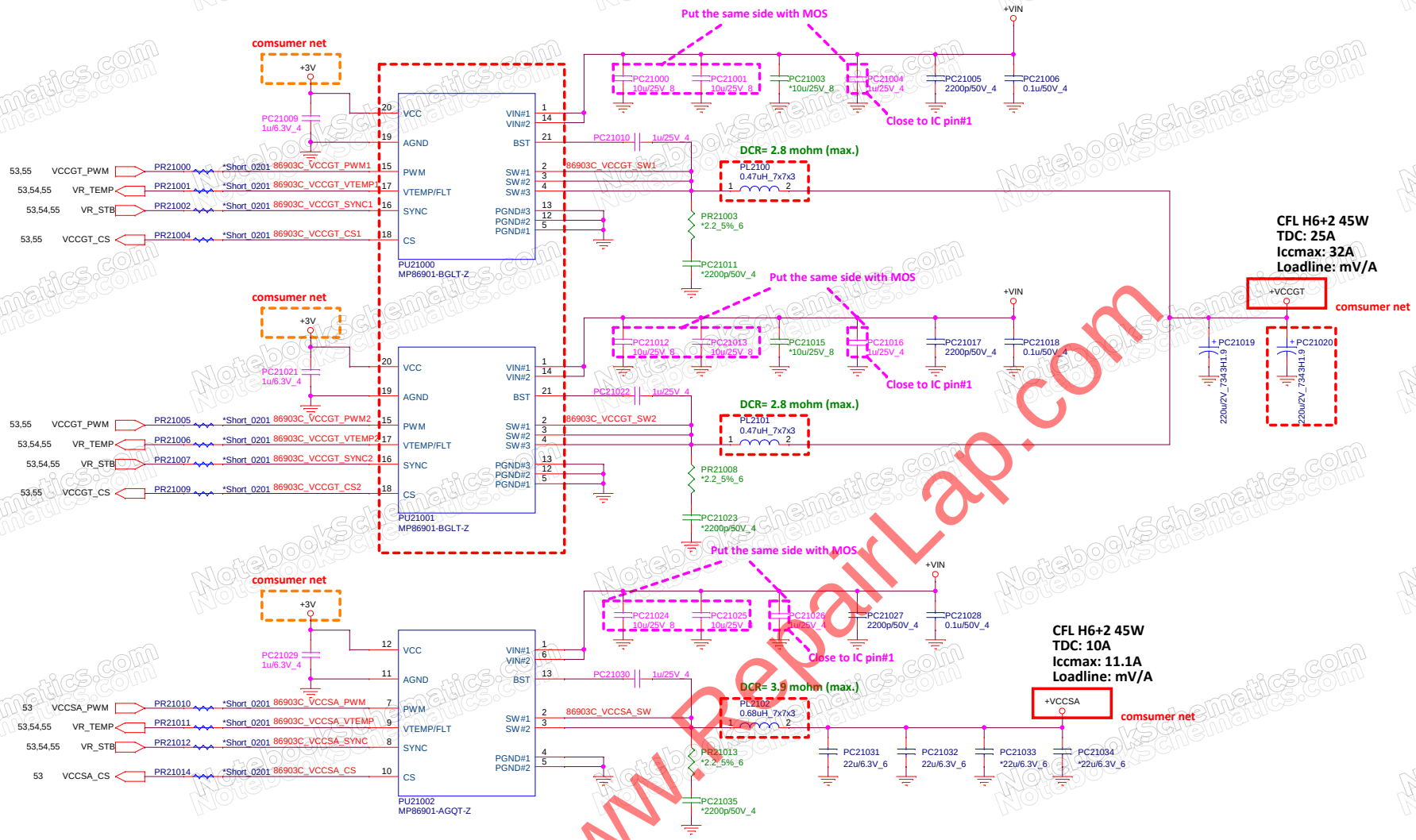




NB5	**PROJECT : G3AE** Quanta Computer Inc.	
Size: Custom	Document Number: **84 -- CPU CORE VR (MP2949A)**	Rev: 1A
Date: Tuesday, March 13, 2018	Sheet 53 of 65	



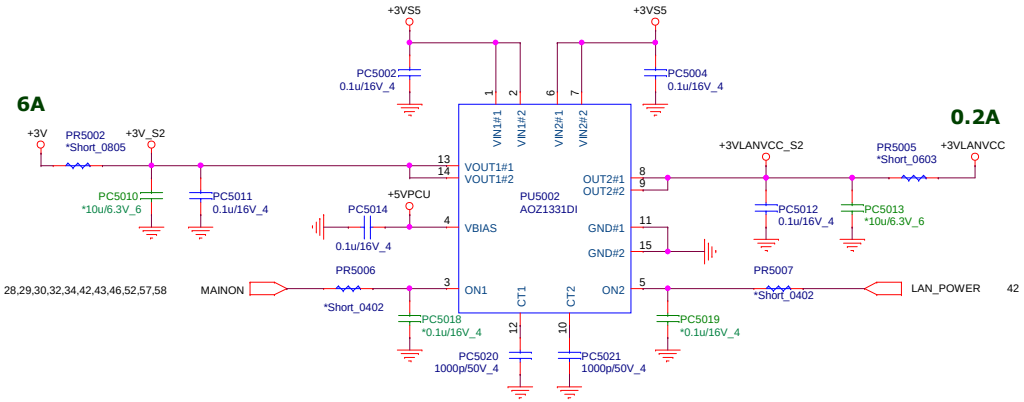
NB5	PROJECT : G3AE Quanta Computer Inc.	
Size: D	Document Number: 85 -- +VCC_CORE (MP86903-C)	Rev: 1A
Date: Tuesday, March 13, 2018	Sheet 54 of 85	

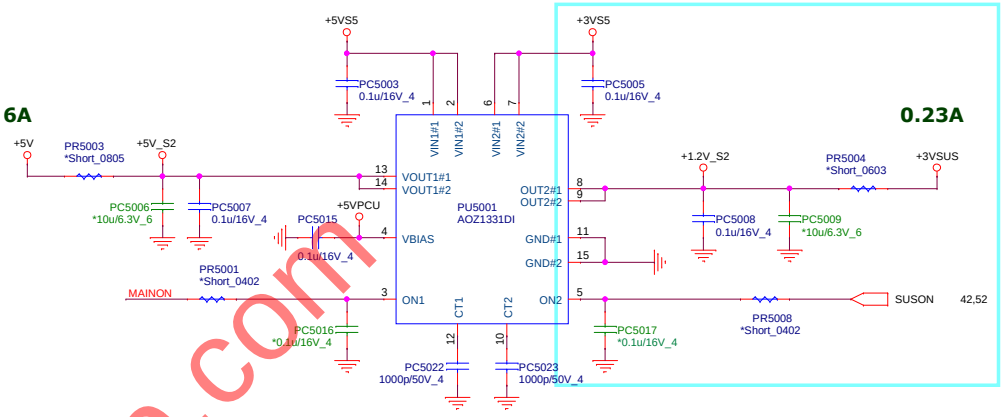


NB5

PROJECT : G3AE
Quanta Computer Inc.

Size	Document Number	Rev
Custom	86 -- +VCC_GT/+VCC_SA	1A
Date: Tuesday, March 13, 2018	Sheet 55 of 65	





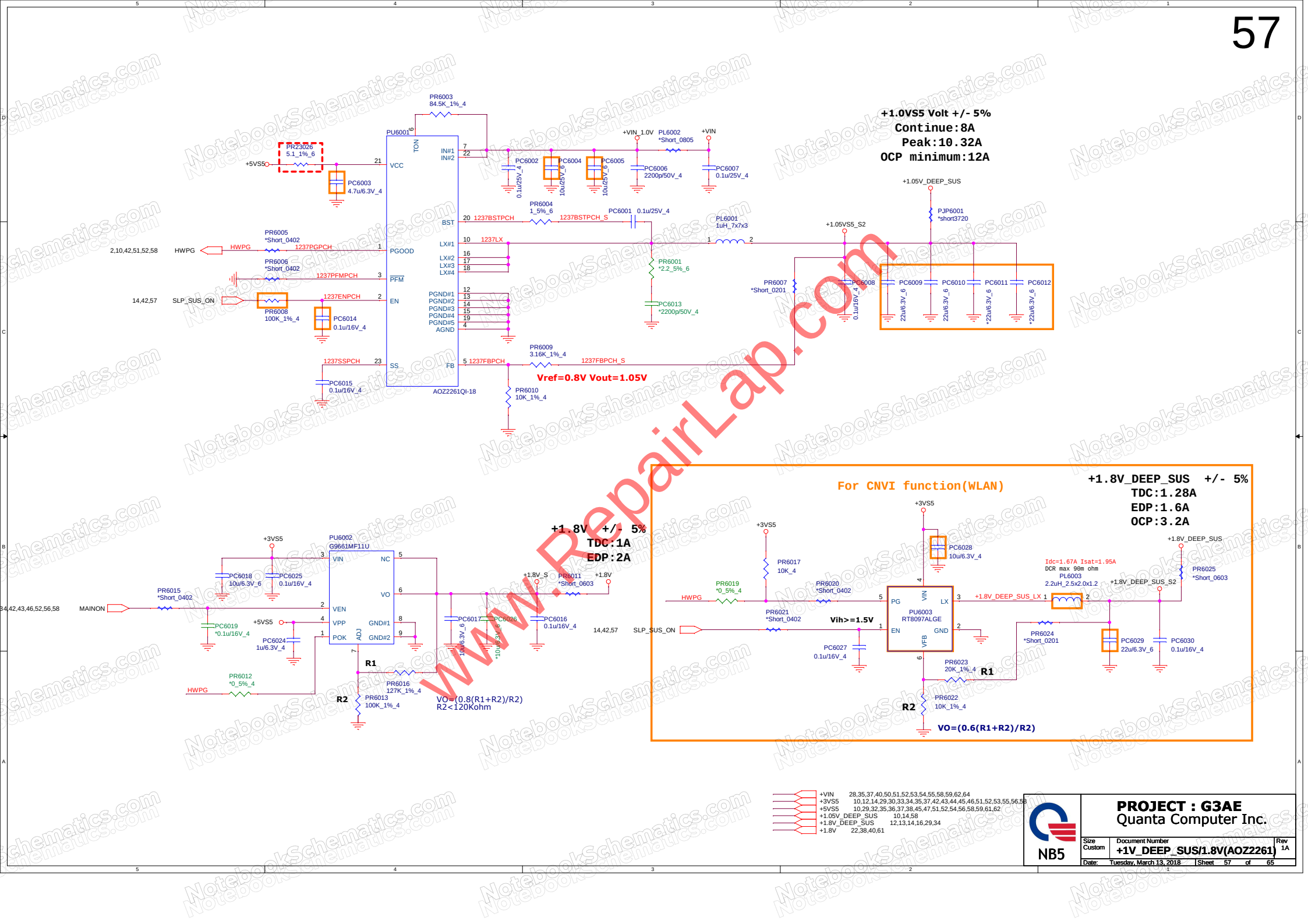
+3V 9,10,11,12,13,14,16,17,18,21,22,28,29,30,31,34,36,37,38,39,40,41,42,46,53,61,62,63
+5V 28,29,30,33,37,38,39,59
+3VS5 10,12,14,29,30,33,34,35,37,42,43,44,45,46,51,52,53,55,57,58
+5VS5 10,29,32,35,36,37,38,45,47,51,52,54,57,58,59,61,62
+3VSUS 33,37
+3VLANVCC 31

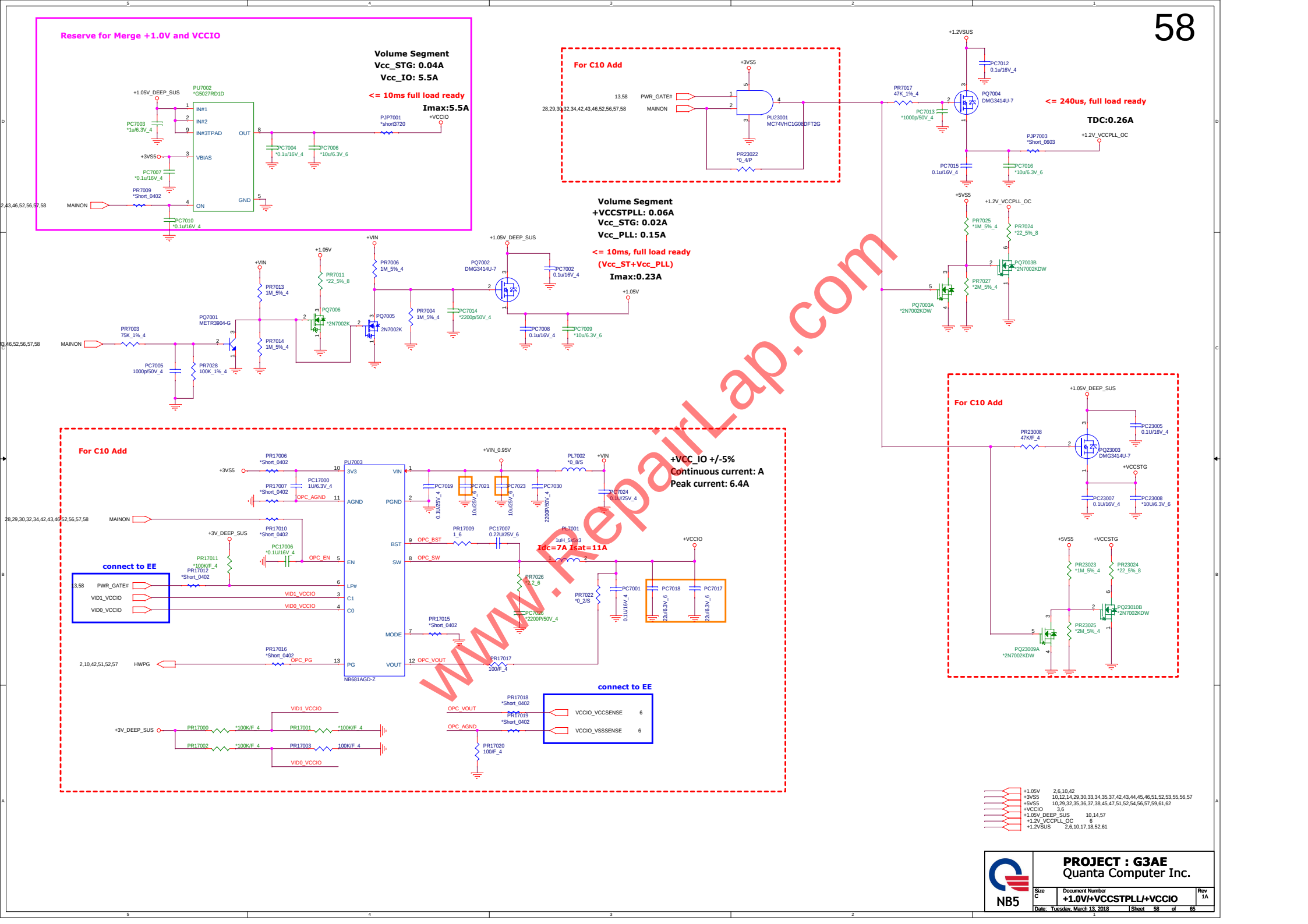
+3V_DEEP_SUS 9,10,12,13,14,16,18,34,44,58

NB5

PROJECT : G3AE
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**Load switch IC (AOZ1331D)**	1A
Date: Tuesday, March 13, 2018	Sheet 56 of 65	





+1.05V 2,6,10,42
+3VS5 10,12,14,29,30,33,34,35,37,42,43,44,45,46,51,52,53,55,56,57
+5VS5 10,29,32,35,36,37,38,45,47,51,52,54,56,57,59,61,62
+VCCIO 3,6
+1.05V_DEEP_SUS 10,14,57
+1.2V_VCCPLL_OC 6
+1.2VSUS 2,6,10,17,18,52,61

NB5	**PROJECT : G3AE** Quanta Computer Inc.
Size C	Document Number +1.0V/+VCCSTPLL/+VCCIO
Rev 1A	
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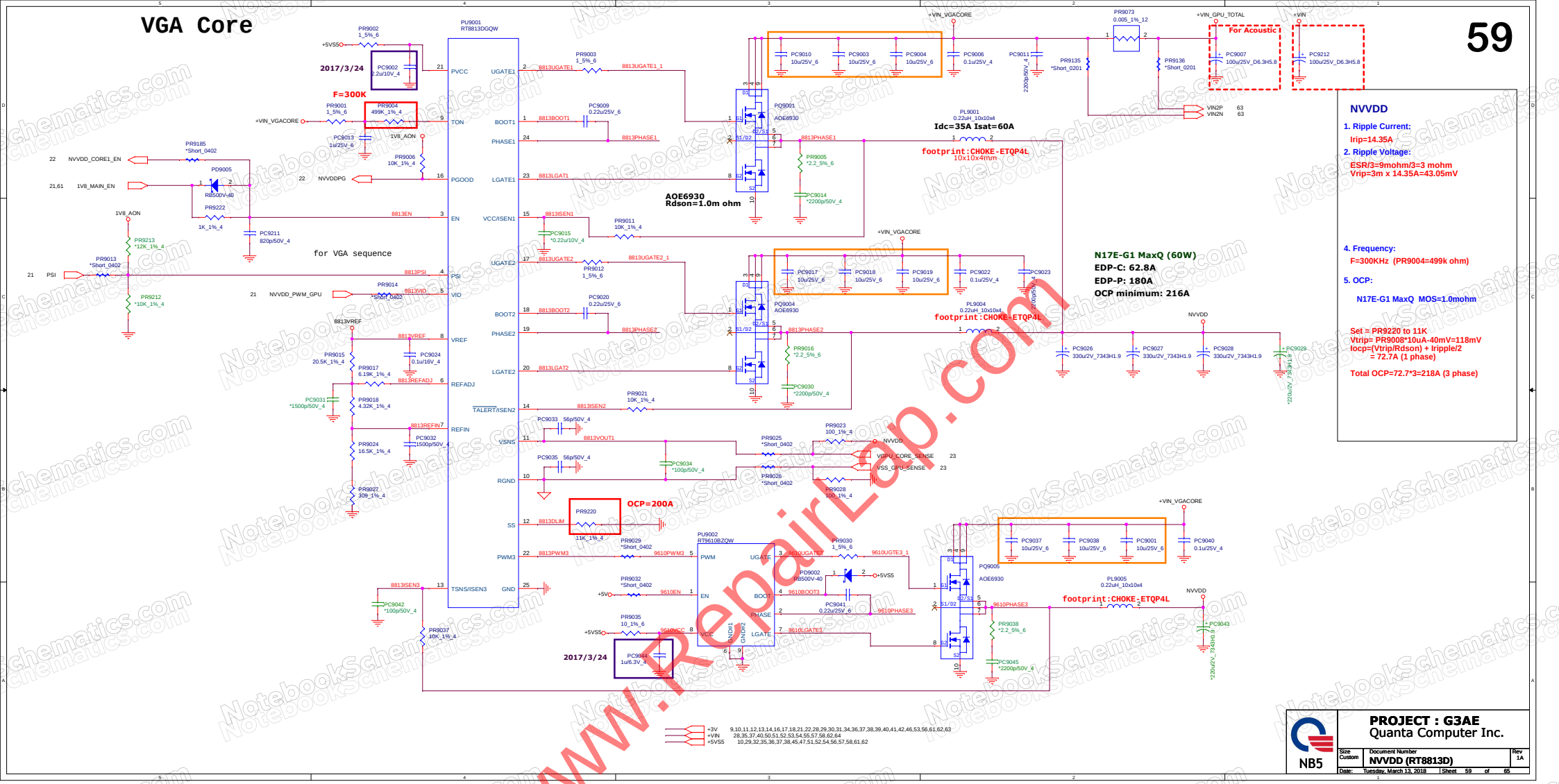

NB5

PROJECT : G3AE
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NVDDS(NA)	1A

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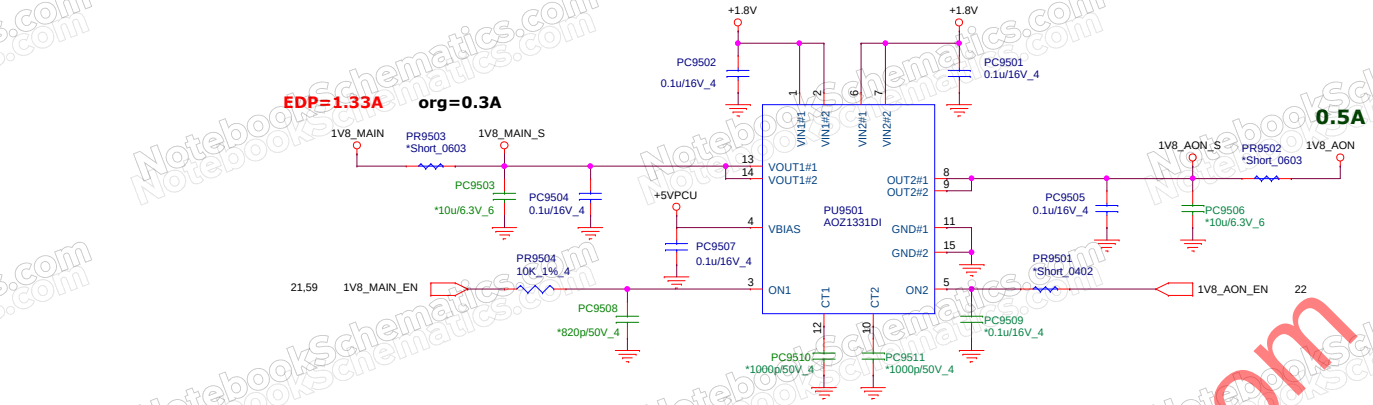
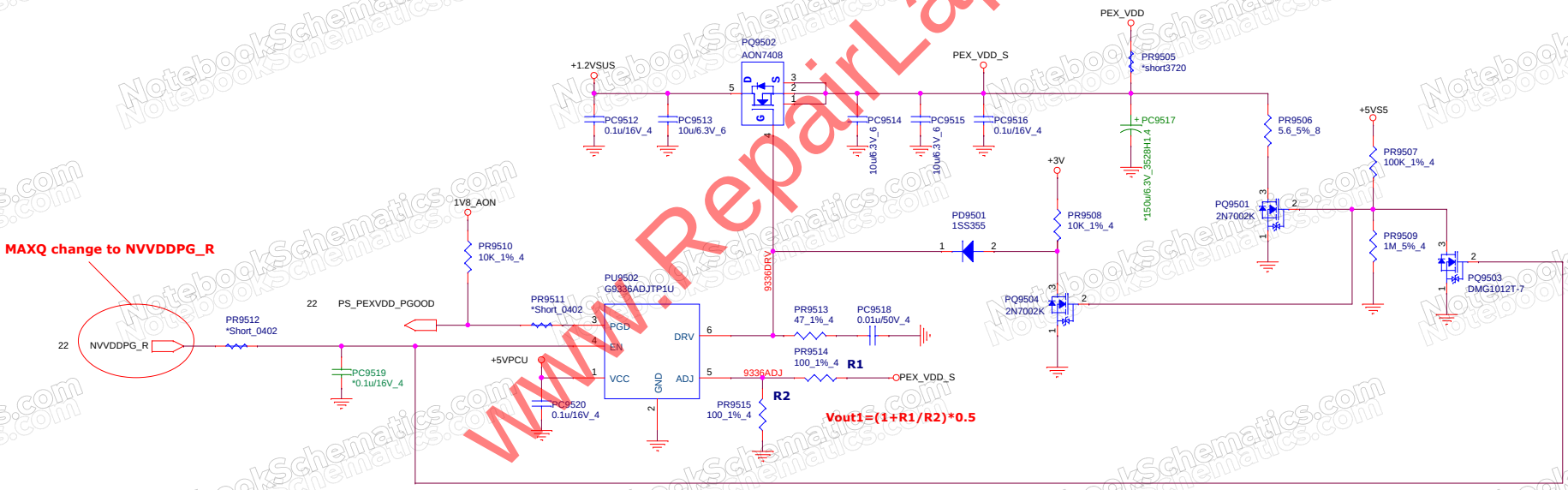


+1.0V_GFX Volt +/- 5%
EDP=3.31A
EDP_peak = TBD



+VIN	28,35,37,40,50,51,52,53,54,55,57,58,59,62,64
+3VS5	10,12,14,29,30,33,34,35,37,42,43,44,45,46,51,52,53,55,56,57,58
+5VS5	10,29,32,35,36,37,38,45,47,51,52,54,56,57,58,59,62
+1.2VSUS	2,6,10,17,18,52,58

PROJECT : G3AE
Quanta Computer Inc.

Size: Custom	Document Number: 1V8_MAIN_AON/PEX_VDD	Rev: 1A
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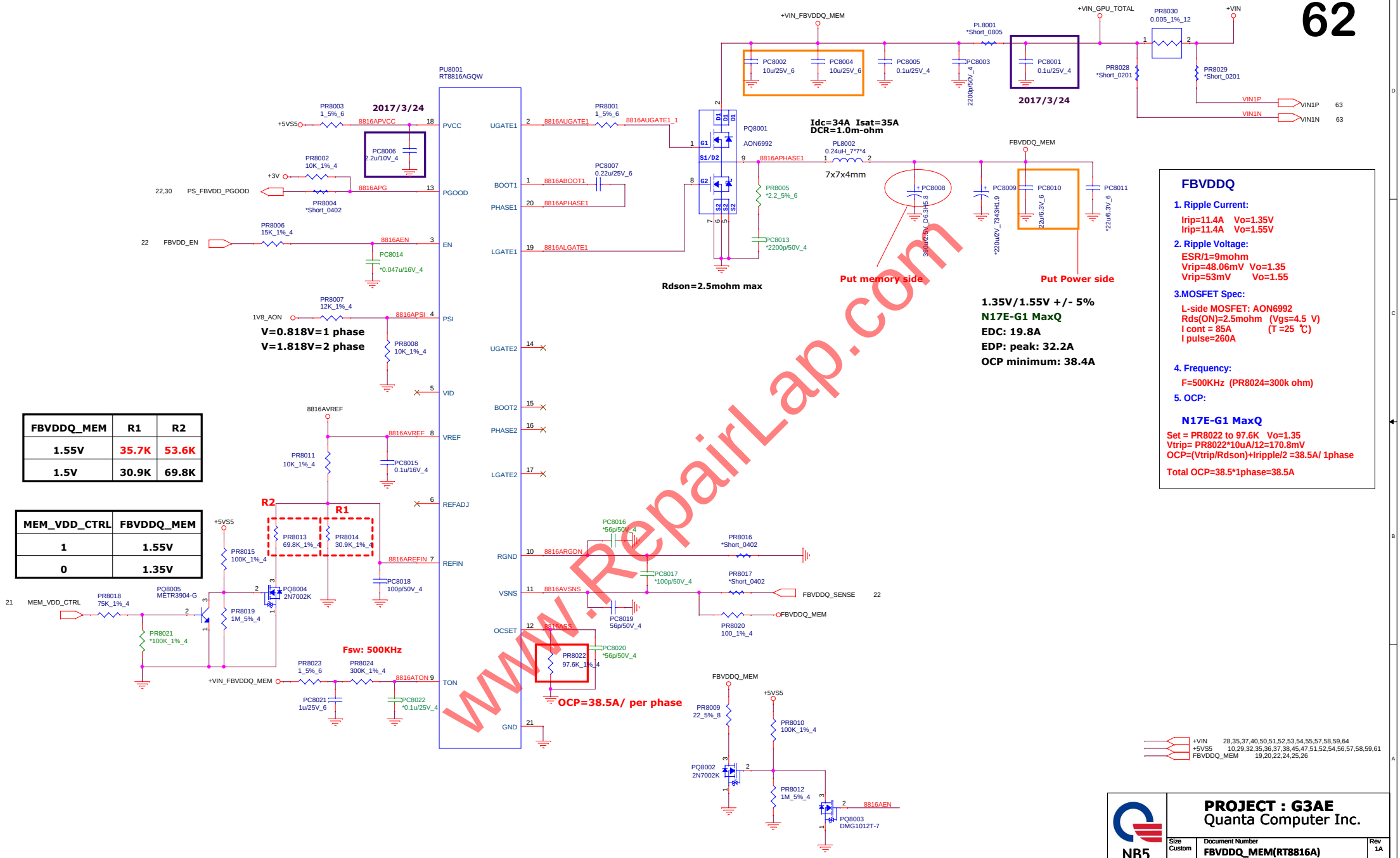
NB5



FBVDDQ_MEM	R1	R2
1.55V	35.7K	53.6K
1.5V	30.9K	69.8K

MEM_VDD_CTRL	FBVDDQ_MEM
1	1.55V
0	1.35V

FBVDDQ

1. Ripple Current:

Irip=11.4A Vo=1.35V
Irip=11.4A Vo=1.55V

2. Ripple Voltage:

ESR/1=9mohm
Vrip=48.06mV Vo=1.35
Vrip=53mV Vo=1.55

3.MOSFET Spec:

L-side MOSFET: AON6992
Rds(ON)=2.5mohm (Vgs=4.5 V)
I cont = 85A (T =25 ℃)
I pulse=260A

4. Frequency:

F=500KHz (PR8024=300k ohm)

5. OCP:

N17E-G1 MaxQ

Set = PR8022 to 97.6K Vo=1.35
Vtrip= PR8022*10uA/12=170.8mV
OCP=(Vtrip/Rdson)+Iripple/2 =38.5A/ 1phase

Total OCP=38.5*1phase=38.5A

+VIN 28,35,37,40,50,51,52,53,54,55,57,58,59,64
+5VS5 10,29,32,35,36,37,38,45,47,51,52,54,56,57,58,59,61
FBVDDQ_MEM 19,20,22,24,25,26

NB5

PROJECT : G3AE
Quanta Computer Inc.

Size	Document Number	Rev
Custom	FBVDDQ_MEM(RT8816A)	1A

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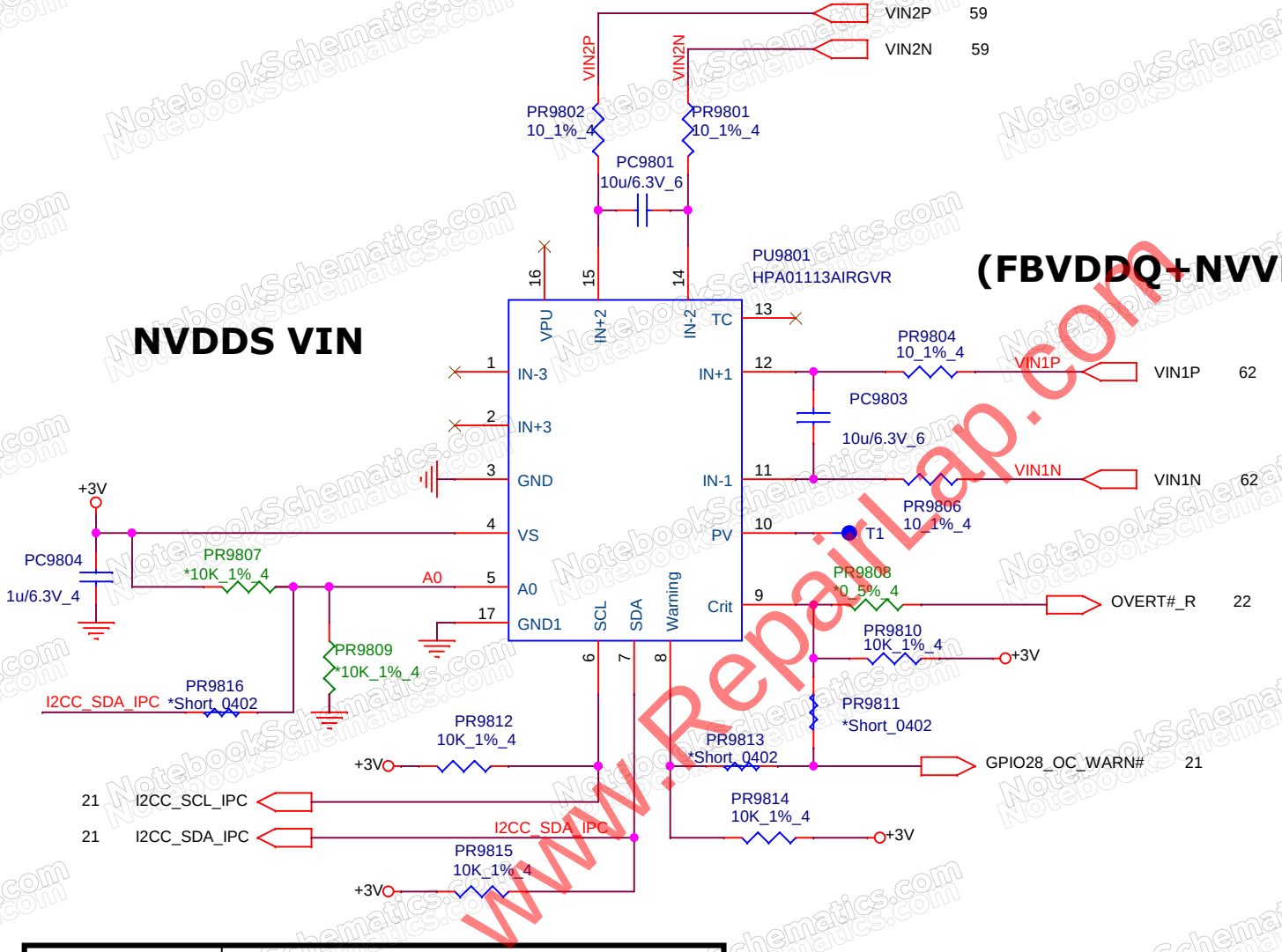
NVVDD VIN

(FBVDDQ+NVVDD+NVDDS) VIN

NVDDS VIN



Address	HPA01113AIRGVR Pin5
0X80	10K to GND
0X84	pin5 connect to pin7

NB5

PROJECT : G3AE
Quanta Computer Inc.

Size	Document Number	Rev
Custom	FBVDDQ_MEM(RT8816A)	1A

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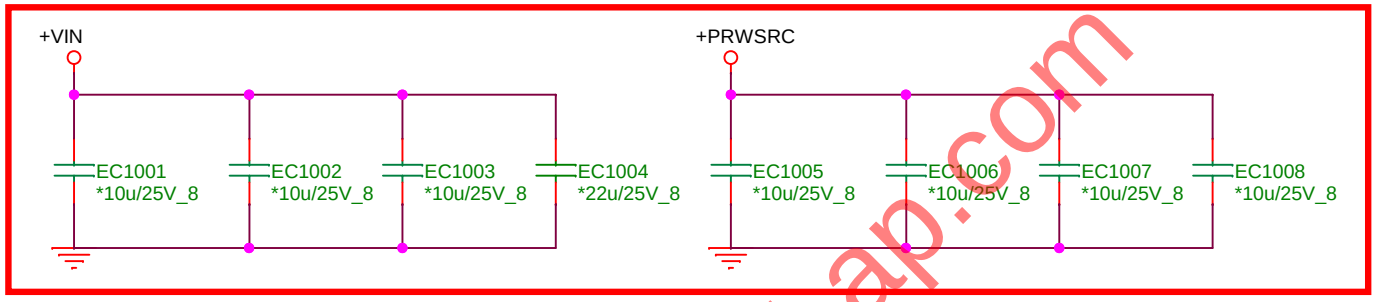
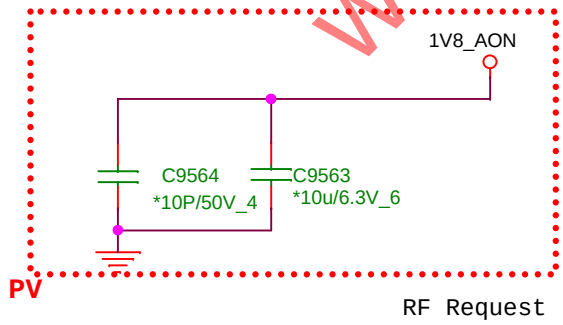
EMI RD decide location, DB stage all no stuff

64

EMI reserve for ISN(High Voltage/AC in ,DC in...)



EMI reserve for ISN(Low Voltage/3V, 5V or...)



NB5

PROJECT : G3AE
Quanta Computer Inc.

Size	Document Number	Rev
A	**EMI CAP**	1A

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Change history (DB to SI)

Change history (SI to PV)

NB5	PROJECT : G3AE Quanta Computer Inc.	
Size: Custom	Document Number: Change List	Rev: 1A
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