GK7CP6S/GK5CN6X

PAGE CONTENT

M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

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Title: INDEX

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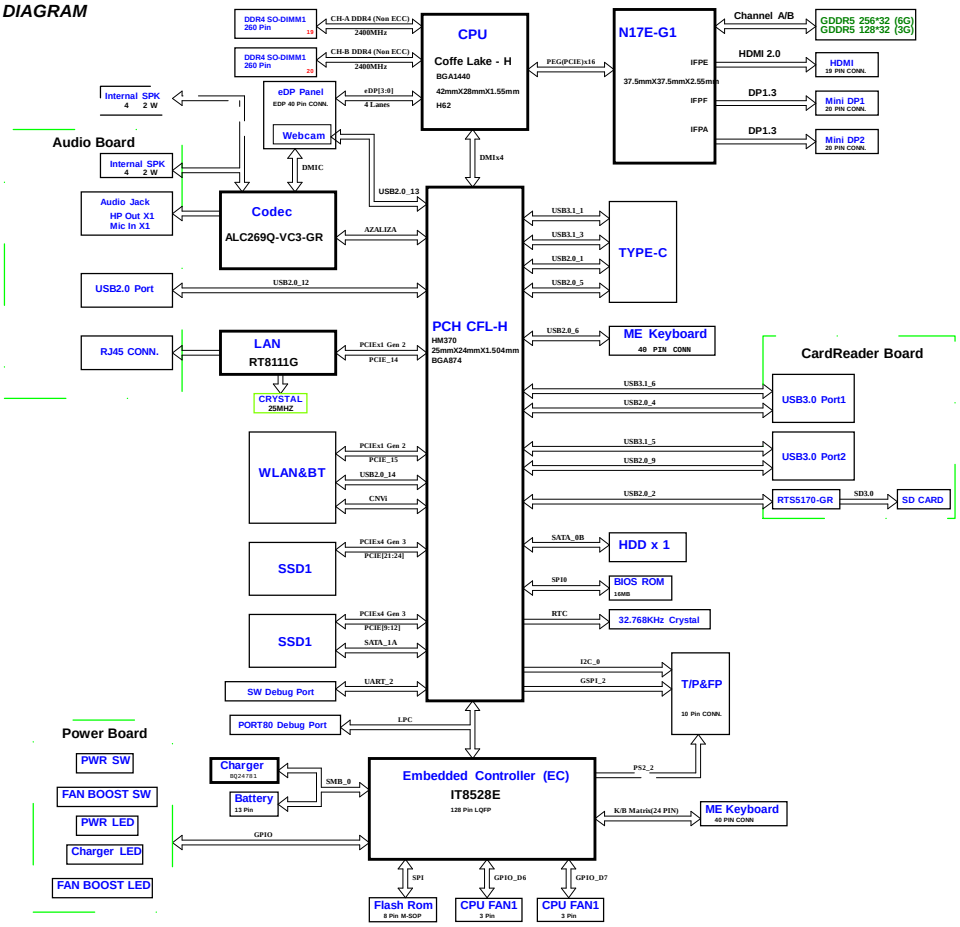
SYSTEM BLOCK DIAGRAM



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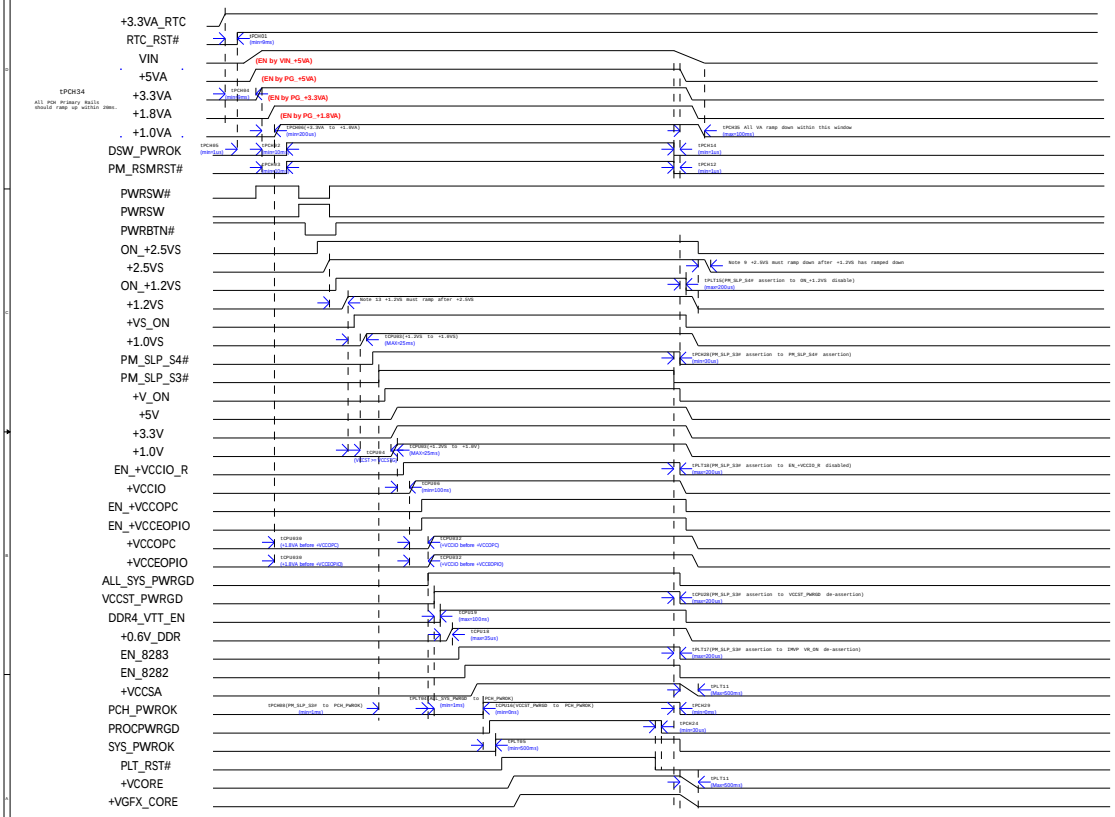
SYSTEM BLOCK

GKSCN0X

POWER ON SEQUENCE



Tong Fang(Suzhou)			
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Size: Custom	Document Number: GK5CN6X		Rev: V A
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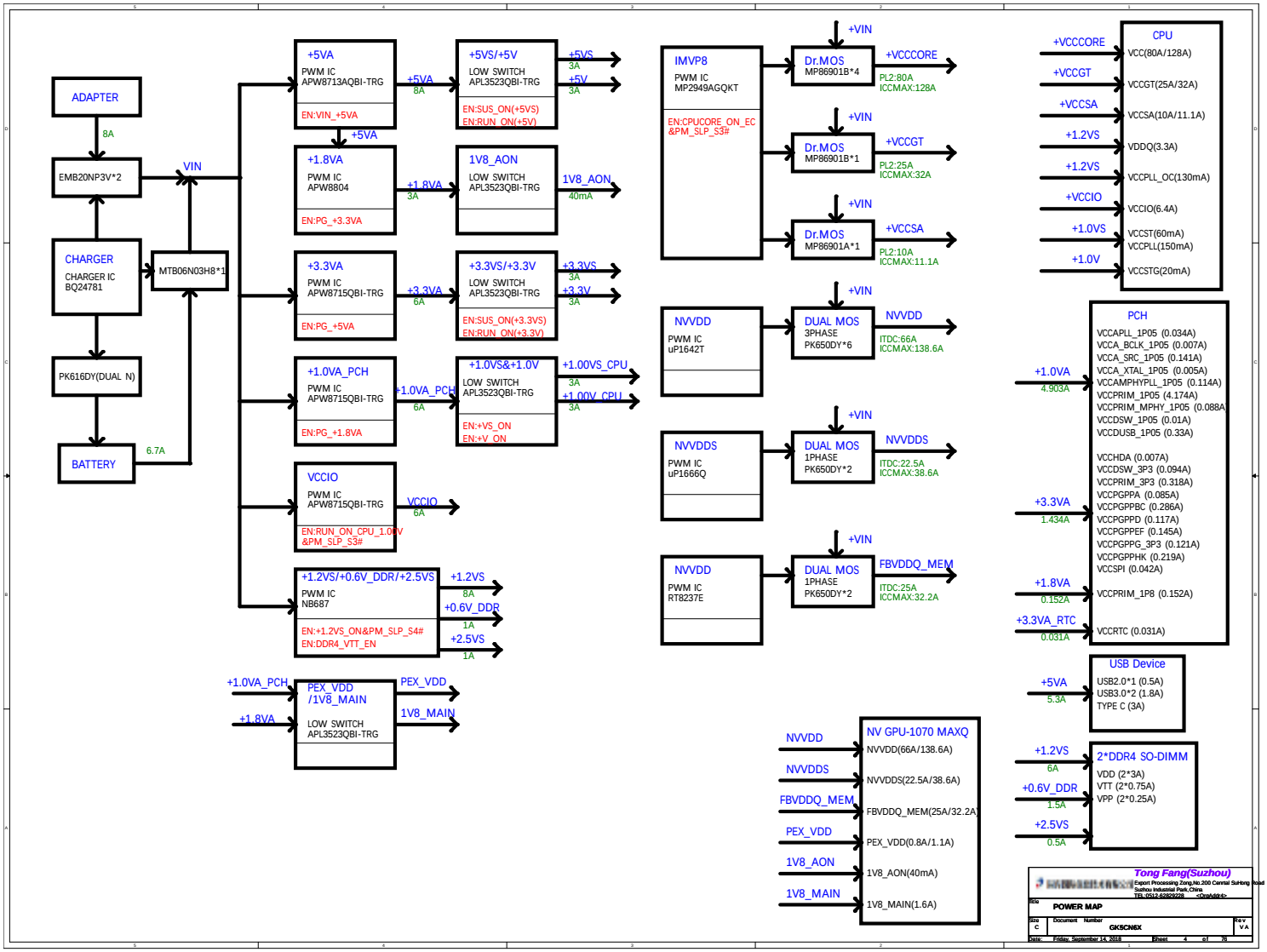
ADAPTER
8A
EMB20NP3V*2
VIN
CHARGER
CHARGER IC
BQ24781
MTB06N03H8*1
PK616DY(DUAL N)
BATTERY
6.7A
+5VA
PWM IC
APW8713AQBI-TRG
EN:VIN_+5VA
+5VA
8A
+5VS/+5V
LOW SWITCH
APL3523QBI-TRG
EN:SUS_ON(+5VS)
EN:RUN_ON(+5V)
+5VS
3A
+5V
3A
+1.8VA
PWM IC
APW8804
EN:PG_+3.3VA
+1.8VA
3A
1V8_AON
LOW SWITCH
APL3523QBI-TRG
1V8_AON
40mA
+3.3VA
PWM IC
APW8715QBI-TRG
EN:PG_+5VA
+3.3VA
6A
+3.3VS/+3.3V
LOW SWITCH
APL3523QBI-TRG
EN:SUS_ON(+3.3VS)
EN:RUN_ON(+3.3V)
+3.3VS
3A
+3.3V
3A
+1.0VA_PCH
PWM IC
APW8715QBI-TRG
EN:PG_+1.8VA
+1.0VA_PCH
6A
+1.0VS&+1.0V
LOW SWITCH
APL3523QBI-TRG
EN:+VS_ON
EN:+V_ON
+1.00VS_CPU
3A
+1.00V_CPU
3A
VCCIO
PWM IC
APW8715QBI-TRG
EN:RUN_ON_CPU_1.0V
&PM_SLP_S3#
VCCIO
6A
+1.2VS/+0.6V_DDR/+2.5VS
PWM IC
NB687
EN:+1.2VS_ON&PM_SLP_S4#
EN:DDR4_VTT_EN
+1.2VS
8A
+0.6V_DDR
1A
+2.5VS
1A
+1.0VA_PCH
+1.8VA
PEX_VDD
/1V8_MAIN
LOW SWITCH
APL3523QBI-TRG
PEX_VDD
1V8_MAIN
IMVP8
PWM IC
MP2949AGQKT
EN:CPUCORE_ON_EC
&PM_SLP_S3#
+VIN
Dr.MOS
MP86901B*4
+VCCCORE
PL2:80A
ICCMAX:128A
+VIN
Dr.MOS
MP86901B*1
+VCCGT
PL2:25A
ICCMAX:32A
+VIN
Dr.MOS
MP86901A*1
+VCCSA
PL2:10A
ICCMAX:11.1A
NVVDD
PWM IC
uP1642T
+VIN
DUAL MOS
3PHASE
PK650DY*6
NVVDD
ITDC:66A
ICCMAX:138.6A
NVVDDS
PWM IC
uP1666Q
+VIN
DUAL MOS
1PHASE
PK650DY*2
NVVDDS
ITDC:22.5A
ICCMAX:38.6A
NVVDD
PWM IC
RT8237E
+VIN
DUAL MOS
1PHASE
PK650DY*2
FBVDDQ_MEM
ITDC:25A
ICCMAX:32.2A
NV GPU-1070 MAXQ
NVVDD
NVVDD(66A/138.6A)
NVVDDS
NVVDDS(22.5A/38.6A)
FBVDDQ_MEM
FBVDDQ_MEM(25A/32.2A)
PEX_VDD
PEX_VDD(0.8A/1.1A)
1V8_AON
1V8_AON(40mA)
1V8_MAIN
1V8_MAIN(1.6A)
CPU
+VCCCORE
VCC(80A/128A)
+VCCGT
VCCGT(25A/32A)
+VCCSA
VCCSA(10A/11.1A)
+1.2VS
VDDQ(3.3A)
+1.2VS
VCCPLL_OC(130mA)
+VCCIO
VCCIO(6.4A)
+1.0VS
VCCST(60mA)
VCCPLL(150mA)
+1.0V
VCCSTG(20mA)
PCH
+1.0VA
4.903A
VCCAPLL_1P05 (0.034A)
VCCA_BCLK_1P05 (0.007A)
VCCA_SRC_1P05 (0.141A)
VCCA_XTAL_1P05 (0.005A)
VCCAMPHYPLL_1P05 (0.114A)
VCCPRIM_1P05 (4.174A)
VCCPRIM_MPHY_1P05 (0.088A)
VCCDSW_1P05 (0.01A)
VCCDUSB_1P05 (0.33A)
+3.3VA
1.434A
VCCHDA (0.007A)
VCCDSW_3P3 (0.094A)
VCCPRIM_3P3 (0.318A)
VCCPGPPA (0.085A)
VCCPGPPBC (0.286A)
VCCPGPPD (0.117A)
VCCPGPPEF (0.145A)
VCCPGPPG_3P3 (0.121A)
VCCPGPPHK (0.219A)
VCCSPI (0.042A)
+1.8VA
0.152A
VCCPRIM_1P8 (0.152A)
+3.3VA_RTC
0.031A
VCCRTC (0.031A)
USB Device
+5VA
5.3A
USB2.0*1 (0.5A)
USB3.0*2 (1.8A)
TYPE C (3A)
2*DDR4 SO-DIMM
+1.2VS
6A
VDD (2*3A)
+0.6V_DDR
1.5A
VTT (2*0.75A)
+2.5VS
0.5A
VPP (2*0.25A)
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POWER MAP
Size
C
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GPP_F21	PCH_BL_PWM	DEL
GPP_F20	T/P LED_PWM	
GPP_F19	PWM_KB BLUE	
GPA3	PWM_KB RED	
GPA4	PID_1_CHG_R_LED	
GPA5	PID_2_PWR_LED	
GPA6	ME_KB_LED	
GPA7	Board ID	

GH5KN

ITE8528 GPIO		Default Pull/Mode
GPA0	PWM_KB GREEN	UP / GPO
GPA1	T/P LED_PWM	UP / GPO
GPA2	PWM_KB BLUE	UP / GPO
GPA3	PWM_KB RED	UP / GPO
GPA4	PID_1_CHG_R_LED	UP / GPO
GPA5	PID_2_PWR_LED	UP / GPO
GPA6	ME_KB_LED	UP / GPO
GPA7	Board ID	UP / GPO
GPB0	PM_SLP_S4#	UP / GPI
GPB1	PM_SLP_S3#	UP / GPI
GPB2	GPU_Adaptor In	Dn / GPI
GPB3	BAT_SMBCLK	Z / GPI
GPB4	BAT_SMBDAT	Z / GPI
GPB5	H_A20GATE	Z / GPO
GPB6	H_RCIN#	UP / GPI
GPB7	SAFTY_PROTECT	Dn / GPI
GPC0	LAN_PWR	Dn / GPI
GPC1	SMBCLK_EC	Z / GPI
GPC2	SMBDAT_EC	Z / GPI
GPC3	SENBAT_V	Dn / GPO
GPC4	FAN_enable0	Dn / GPO
GPC5	SYS_PWROK	Dn / GPO
GPC6	Boost FAN_EN1	Dn / GPO
GPC7	+2.5VS_ON	UP / GPO
GPD0	ADAP_IN	UP / GPI
GPD1	PWRBTN#	UP / GPO
GPD2	PLT_RST#	UP / GPI
GPD3	HDMI_HPD	UP / GPI
GPD4	EC_EXTSMI#	UP / GPI
GPD5	ME_WE#	UP / GPO
GPD6	FAN0_detect	Dn / GPO
GPD7	FAN1_detect	Dn / GPO
GPE0	LID#	Dn / GPI
GPE1	EG_DA	
GPE2	EG_Cycle start	
GPE3	EG_CLK	
GPE4	PWRSW	UP / GPI
GPE5	LVDS_VIN	Dn / GPO
GPE6	WLAN_ON	Dn / GPO
GPE7	AMP_MUTE#	UP / GPO
GPF0	PANEL_VCC	UP / GPO
GPF1	PCH_PWROK	UP / GPI
GPF2	BT_ON	UP / GPO
GPF3	Q_key1	UP / GPI
GPF4	TP_CLK	UP / GPI
GPF5	TP_DATA	UP / GPI
GPF6	EC_PECI	UP / GPI
GPF7	RUN_ON	UP / GPI
GPG0	PANEL_3.3V_ON	Z/ GPO
GPG1	Reserved for AC remove	Dn/GPO/ID7
GPG2	CPUCORE_ON	Z/ GPO
GPG6	WEBCAM_ON	Z/ GPO
GPH0	PM_CLKRUN#	Dn/GPI/ID8
GPH1	PCH_BL_EN	Dn/GPO/ID1
GPH2	ID_DET	Dn/GPI/ID2
GPH3		Dn/GPI/ID3
GPH4		Dn/GPI/ID4
GPH5	HYB_ON#	Dn/GPI/ID5
GPH6		Dn/GPI/ID6
GPI0	Boost FAN_EN	/GPI/Z
GPI1	PANEL_DETECT	/GPI/Z
GPI2	PCIE_WAKE#	/GPI/Z
GPI3	FAN_enable1	/GPI/Z
GPI4	BAT_I	/GPI/Z
GPI5	BATT_TEMP	/GPI/Z
GPI6	Iadapter_I bat	/GPI/Z
GPI7	BAT_V	/GPI/Z
GPJ0	EC_BL_ON	/GPO/Z
GPJ1	EC_PROCHOT	/GPOI/Z
GPJ2	FAN_CTRL0	/GPO/Z
GPJ3	BATT_VA_OFF#	/GPO/Z
GPJ4	FAN_CTRL1	/GPO/Z
GPJ5	CHG_REF	/GPO/Z
GPM0	LPC_AD0	/GPI/Z
GPM1	LPC_AD1	/GPI/Z
GPM2	LPC_AD2	/GPI/Z
GPM3	LPC_AD3	/GPI/Z
GPM4	CLK_EC_LPC	/GPI/Z
GPM5	LPC_FRAME#	/GPI/Z
GPM6	INT_SERIRQ	/GPI/Z

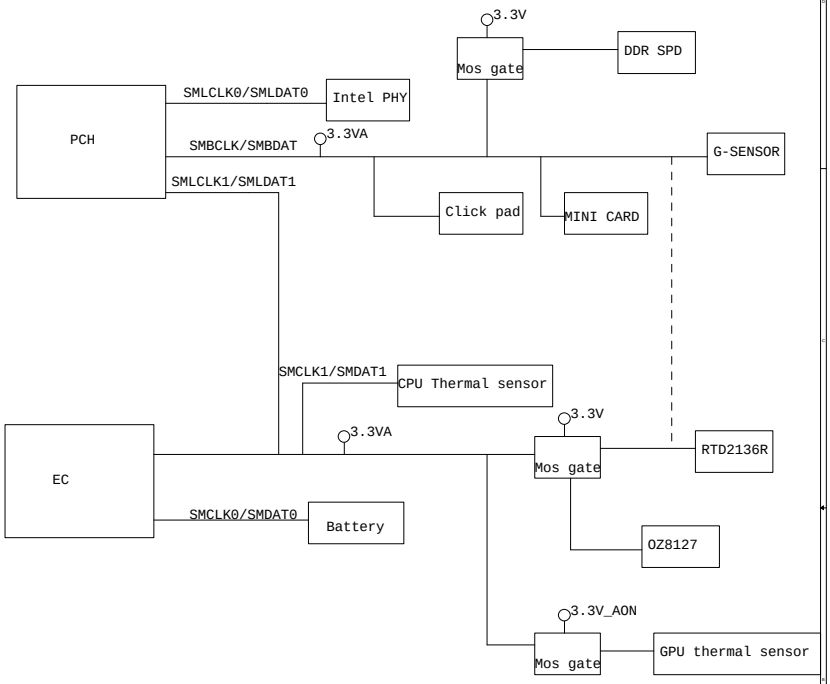
GI5KN

ITE8528 GPIO		Default Pull/Mode
GPA0	PWM_KB GREEN	UP / GPO
GPA1	T/P LED_PWM	UP / GPO
GPA2	PWM_KB BLUE	UP / GPO
GPA3	PWM_KB RED	UP / GPO
GPA4	PID_1_CHG_R_LED	UP / GPO
GPA5	PID_2_PWR_LED	UP / GPO
GPA6	PM_RSMRST#	UP / GPO
GPA7	Board ID	UP / GPO
GPB0	PM_SLP_S4#	UP / GPI
GPB1	PM_SLP_S3#	UP / GPI
GPB2	GPU_Adaptor In	Dn / GPI
GPB3	BAT_SMBCLK	Z / GPI
GPB4	BAT_SMBDAT	Z / GPI
GPB5	H_A20GATE	Z / GPO
GPB6	H_RCIN#	UP / GPI
GPB7	SAFTY_PROTECT	Dn / GPI
GPC0	LAN_PWR	Dn / GPI
GPC1	SMBCLK_EC	Z / GPI
GPC2	SMBDAT_EC	Z / GPI
GPC3	SENBAT_V	Dn / GPO
GPC4	FAN_enable0	Dn / GPO
GPC5	SYS_PWROK	Dn / GPO
GPC6	Boost FAN_EN1	Dn / GPO
GPC7	+2.5VS_ON	UP / GPO
GPD0	ADAP_IN	UP / GPI
GPD1	PWRBTN#	UP / GPO
GPD2	PLT_RST#	UP / GPI
GPD3	HDMI_HPD	UP / GPI
GPD4	EC_EXTSMI#	UP / GPI
GPD5	ME_WE#	UP / GPO
GPD6	FAN0_detect	Dn / GPO
GPD7	FAN1_detect	Dn / GPO
GPE0	LID#	Dn / GPI
GPE1	+1.2VS_ON	Dn / GPI
GPE2	PWR_USB#	Dn / GPO
GPE3	EXT_WIFI_ON	Dn / GPO
GPE4	PWRSW	UP / GPI
GPE5	LVDS_VIN	Dn / GPO
GPE6	WLAN_ON	Dn / GPO
GPE7	AMP_MUTE#	UP / GPO
GPF0	DGPU_EN_EC	UP / GPO
GPF1	PCH_PWROK	UP / GPI
GPF2	BT_ON	UP / GPO
GPF3	Q_key1	UP / GPI
GPF4	TP_CLK	UP / GPI
GPF5	TP_DATA	UP / GPI
GPF6	EC_PECI	UP / GPI
GPF7	RUN_ON	UP / GPI
GPG0	PANEL_3.3V_ON	Z/ GPO
GPG1	Reserved for AC remove	Dn/GPO/ID7
GPG2	CPUCORE_ON	Z/ GPO
GPG6	WEBCAM_ON/SUS_ON	Z/ GPO
GPH0	PM_CLKRUN#	Dn/GPI/ID8
GPH1	PCH_BL_EN	Dn/GPO/ID1
GPH2	ID_DET	Dn/GPI/ID2
GPH3	DGPU_EN_EC_Keep	Dn/GPI/ID3
GPH4	Dgpu_RST_EC#	Dn/GPI/ID4
GPH5	HYB_ON#	Dn/GPI/ID5
GPH6	Clear CMOS	Dn/GPI/ID6
GPI0	Boost FAN_EN	/GPI/Z
GPI1	EC_OVERT_NVVDD#	/GPI/Z
GPI2	PCIE_WAKE#/Dgpu_RST_EC#_keep	/GPI/Z
GPI3	FAN_enable1	/GPI/Z
GPI4	BAT_I	/GPI/Z
GPI5	BATT_TEMP	/GPI/Z
GPI6	Iadapter_I bat	/GPI/Z
GPI7	BAT_V	/GPI/Z
GPJ0	EC_BL_ON	/GPO/Z
GPJ1	EC_PROCHOT	/GPOI/Z
GPJ2	FAN_CTRL0	/GPO/Z
GPJ3	BATT_VA_OFF#	/GPO/Z
GPJ4	FAN_CTRL1	/GPO/Z
GPJ5	CHG_REF	/GPO/Z
GPM0	LPC_AD0	/GPI/Z
GPM1	LPC_AD1	/GPI/Z
GPM2	LPC_AD2	/GPI/Z
GPM3	LPC_AD3	/GPI/Z
GPM4	CLK_EC_LPC	/GPI/Z
GPM5	LPC_FRAME#	/GPI/Z
GPM6	INT_SERIRQ	/GPI/Z

EXT EC

ITE8302 GPIO		Default Pull/Mode
GPIO4	EXT_WIFI_ON	UP / GPO
GPIO5	EC_OVERT_NVVDD#	UP / GPO
GPIO7	Dgpu_RST_EC#_keep	UP / GPO
GPIO9	SUS_ON	UP / GPO
GPIO11	CTL3	UP / GPO
GPIO13	CTL2	UP / GPO
GPIO18	EXT_Q_key0	UP / GPO
GPIO20	EXT_Q_key1	UP / GPO
GPIO22	PWR_USB#	UP / GPI
GPIO24	+1.2VS_ON	UP / GPI
GPIO26	LID1#	Dn / GPI
GPIO27	Dgpu_RST_EC#	Z / GPI
GPIO29	PM_RSMRST#	Z / GPI
GPIO31	DGPU_EN_EC_Keep	Z / GPO
GPIO33	DGPU_EN_EC	UP / GPI
GPIO35	Clear CMOS	Dn / GPI

SMBUS BLOCK



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GPIO & SMBUS Block

GI5CNBX

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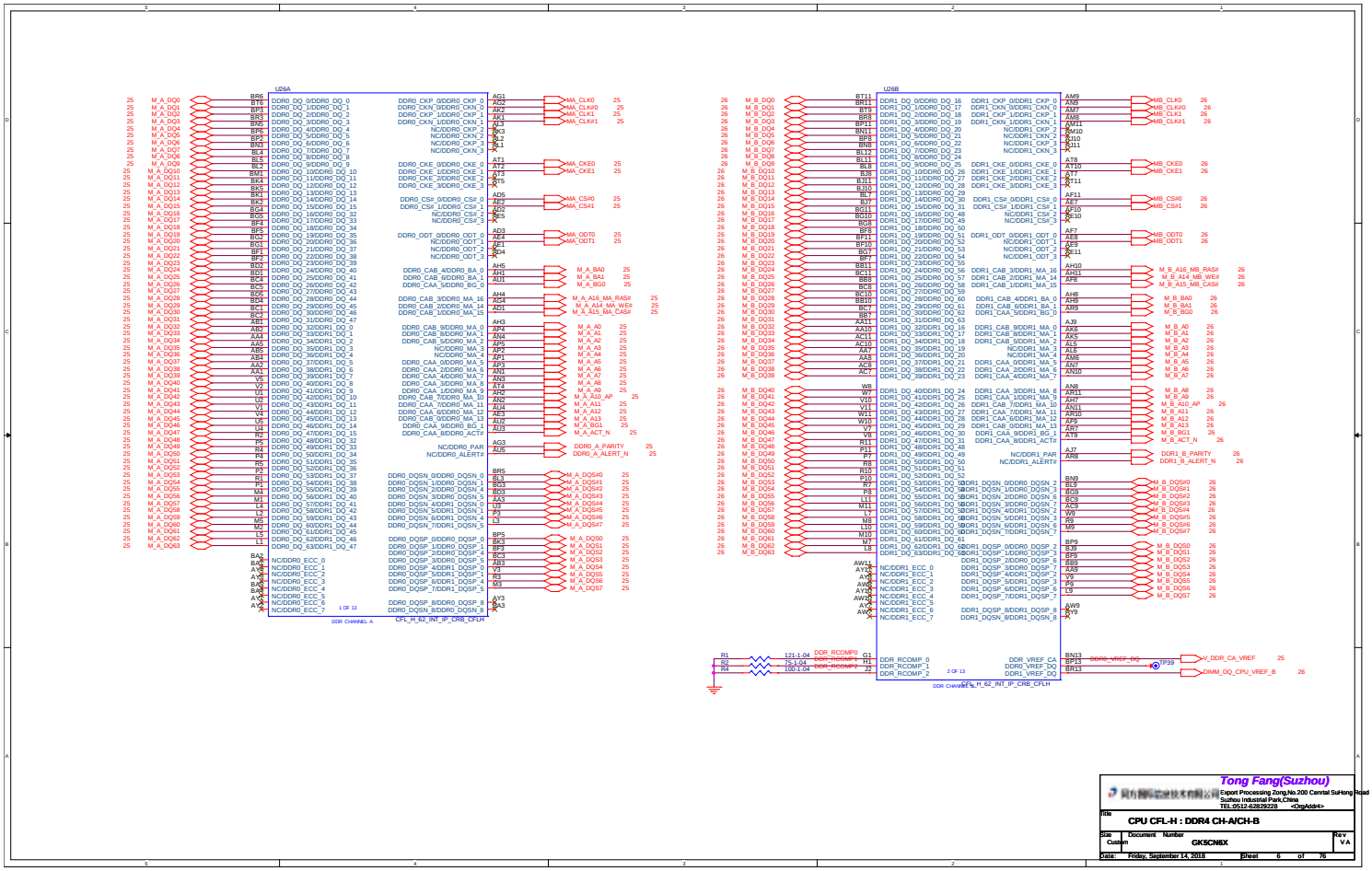

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Title: CPU CFL-H : DDR4 CH-A/CH-B

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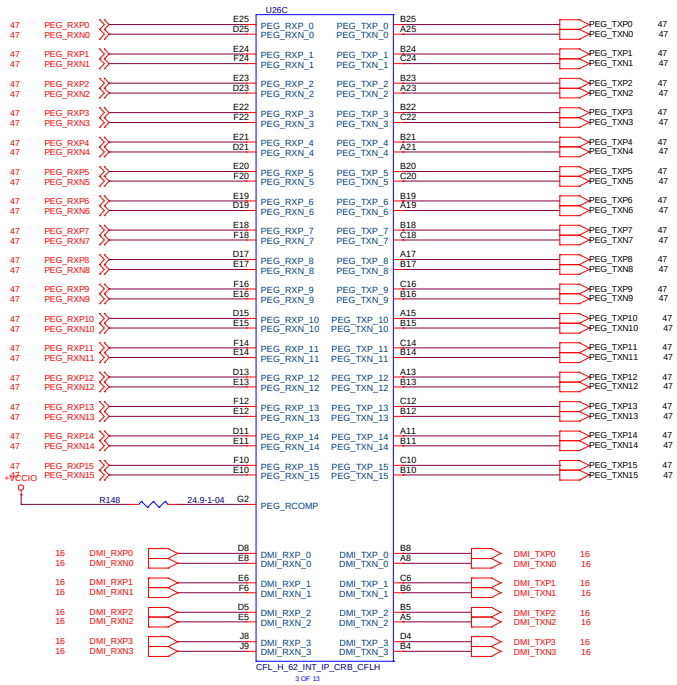
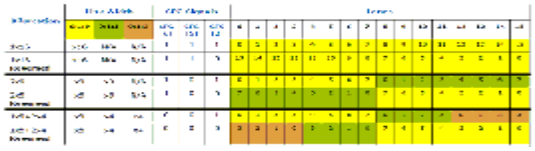


Table 1-12. PCI Express* Bifurcation and Lane Reversal Mapping



Company	Tong Fang(Suzhou)
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Title	CPU CFL-H : PEG/DMI
Size	B
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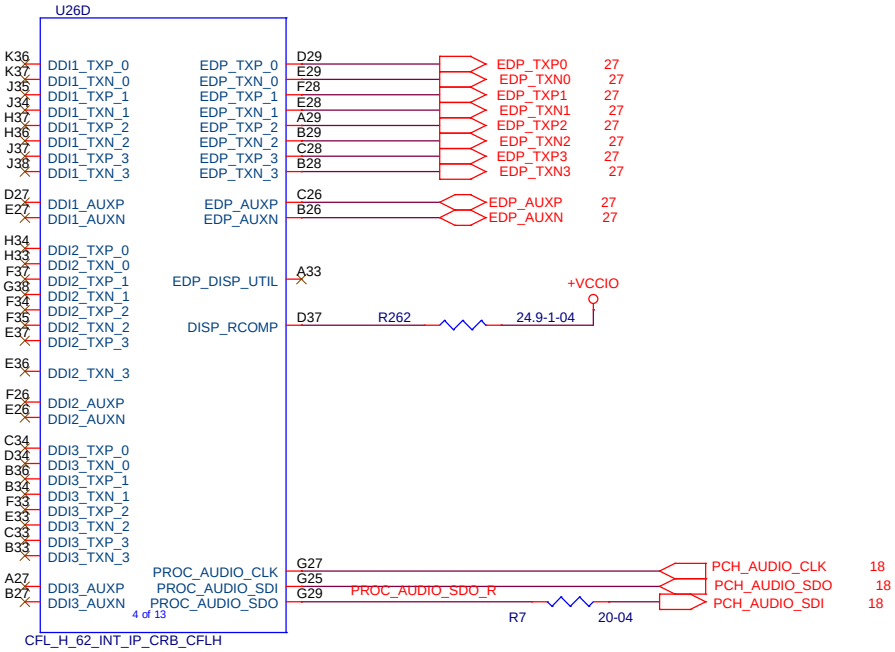

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Title
CPU CFL-H : DDI/EDP

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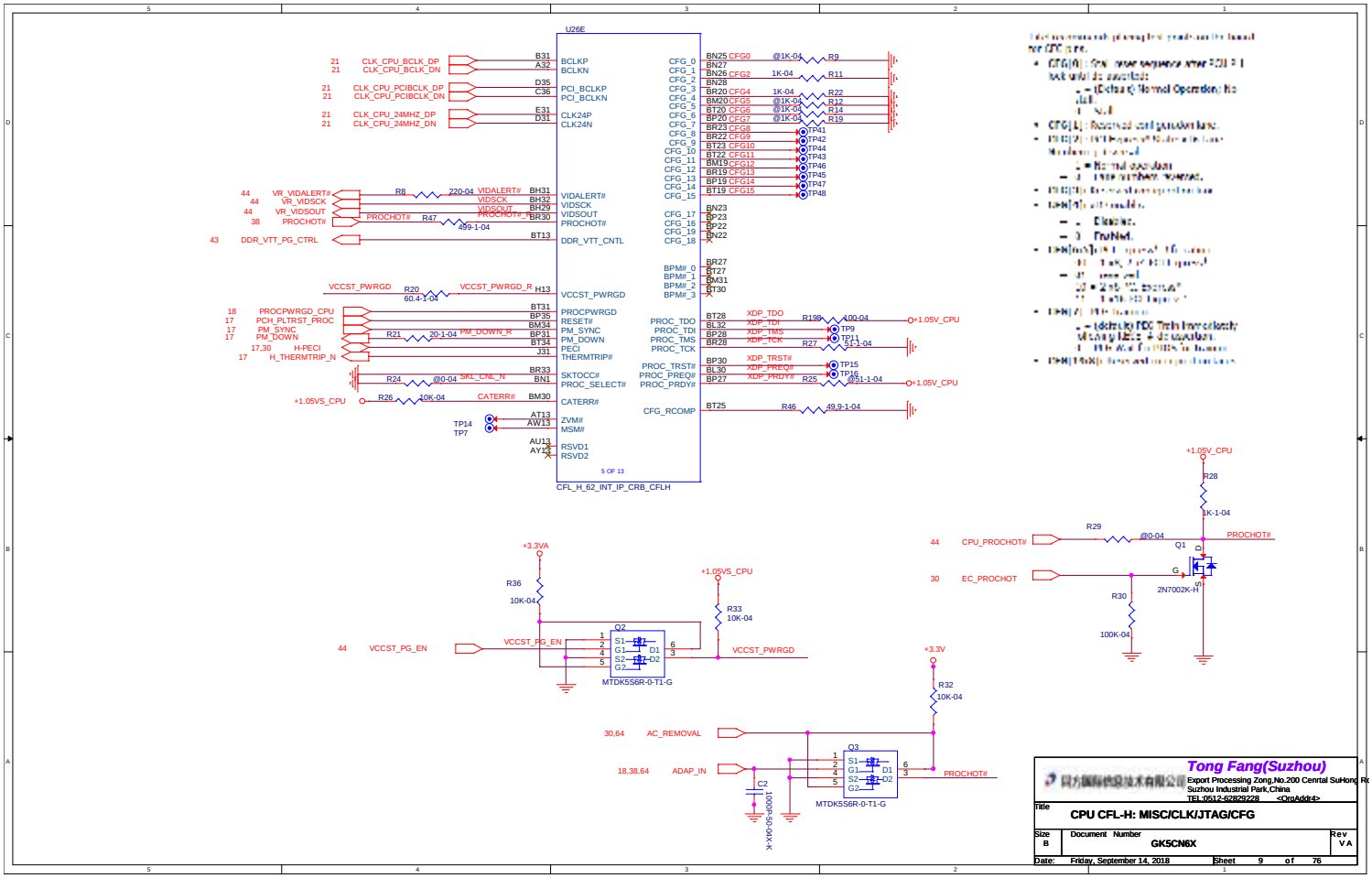
U26E
CFL_H_62_INT_IP_CRB_CFLH
5 OF 13
CLK_CPU_BCLK_DP
CLK_CPU_BCLK_DN
CLK_CPU_PCIBCLK_DP
CLK_CPU_PCIBCLK_DN
CLK_CPU_24MHZ_DP
CLK_CPU_24MHZ_DN
BCLKP
BCLKN
PCI_BCLKP
PCI_BCLKN
CLK24P
CLK24N
VR_VIDALERT#
VR_VIDSCK
VR_VIDSOUT
PROCHOT#
DDR_VTT_PG_CTRL
VIDALERT#
VIDSCK
VIDSOUT
PROCHOT#
DDR_VTT_CNTL
VCCST_PWRGD
VCCST_PWRGD_R
PROCPWRGD_CPU
PCH_PLTRST_PROC
PM_SYNC
PM_DOWN
H-PECI
H_THERMTRIP_N
PROCPWRGD
RESET#
PM_SYNC
PM_DOWN
PECI
THERMTRIP#
SKL_CNL_N
SKTOCC#
PROC_SELECT#
CATERR#
CATERR#
ZVM#
MSM#
RSVD1
RSVD2
CFG_RCOMP
PROC_TDO
PROC_TDI
PROC_TMS
PROC_TCK
PROC_TRST#
PROC_PREQ#
PROC_PRDY#
XDP_TDO
XDP_TDI
XDP_TMS
XDP_TCK
XDP_TRST#
XDP_PREQ#
XDP_PRDY#
+1.05V_CPU
+1.05VS_CPU
+3.3VA
+3.3V
CPU_PROCHOT#
EC_PROCHOT
VCCST_PG_EN
AC_REMOVAL
ADAP_IN
2N7002K-H
MTDK5S6R-0-T1-G
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CPU CFL-H: MISC/CLK/JTAG/CFG
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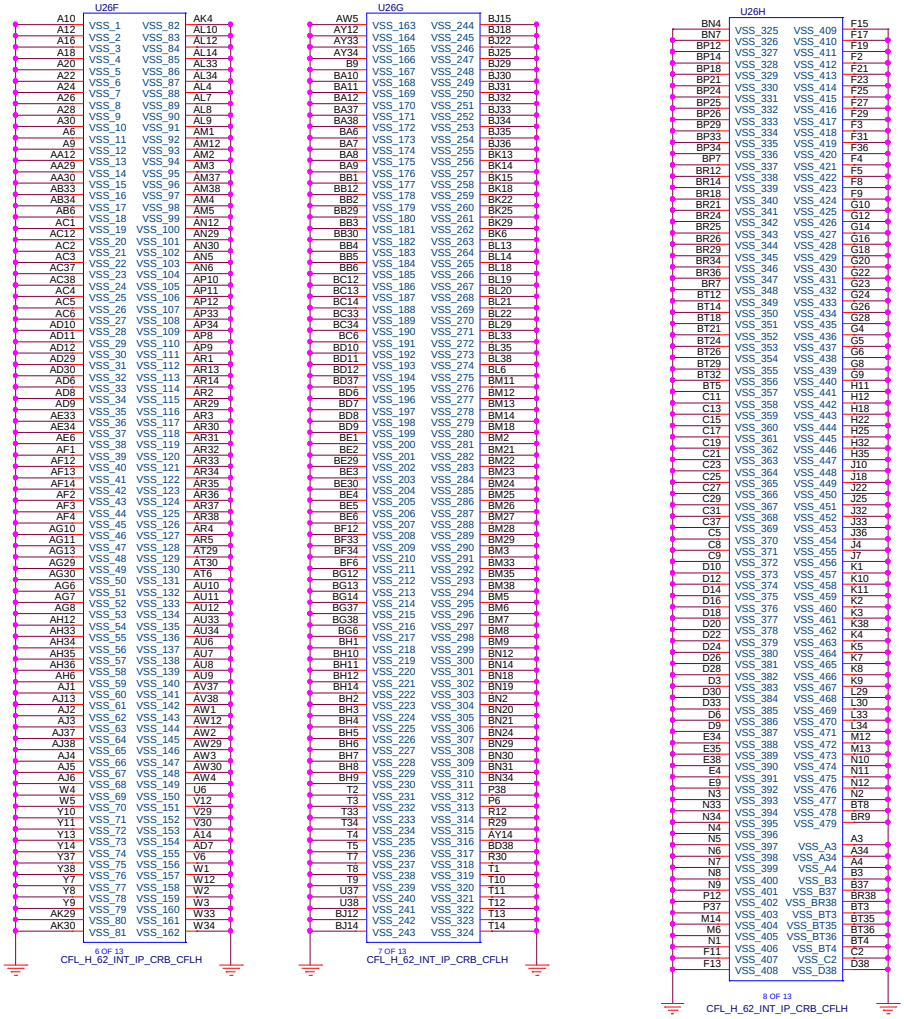

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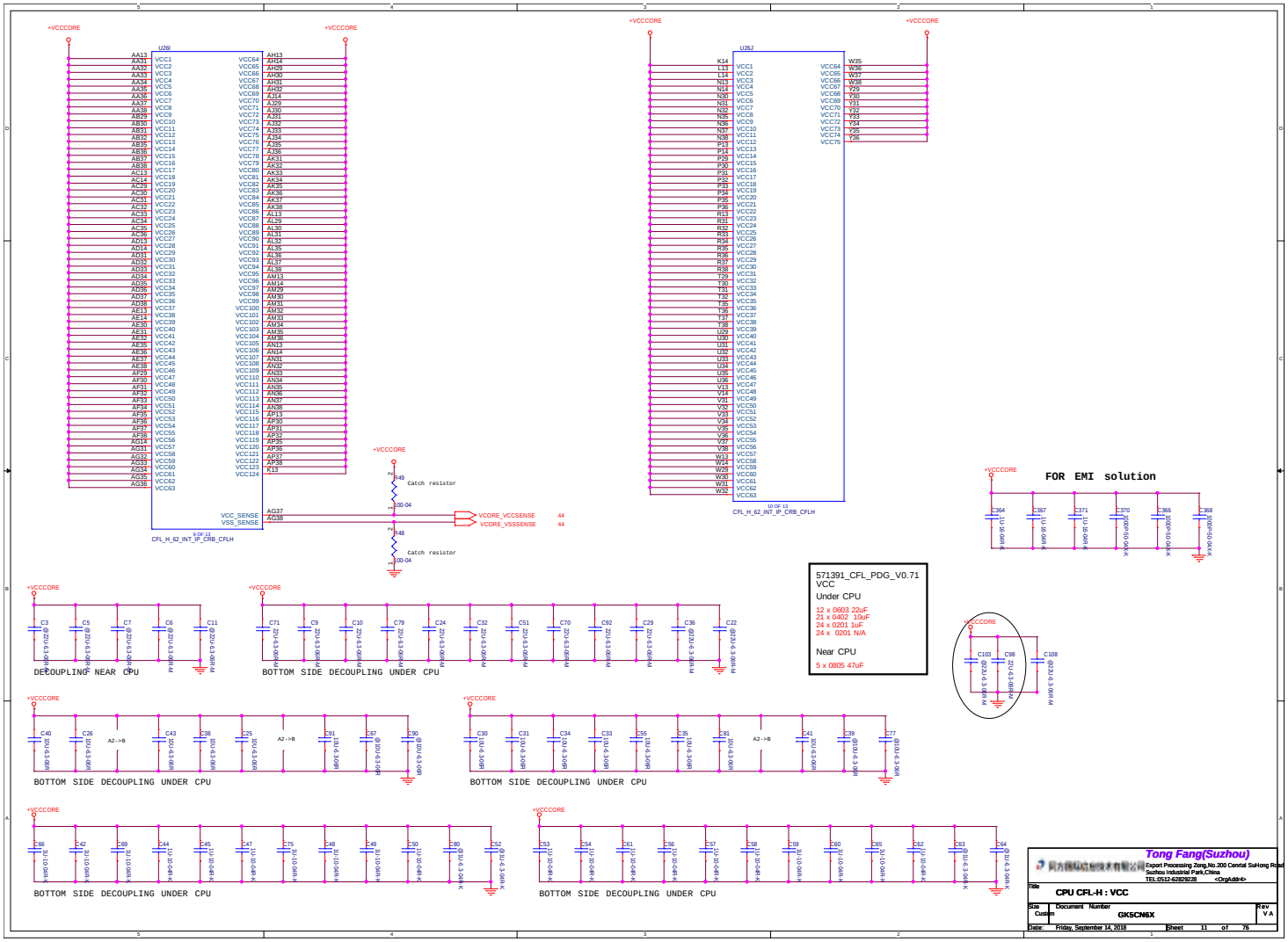
+VCCCORE
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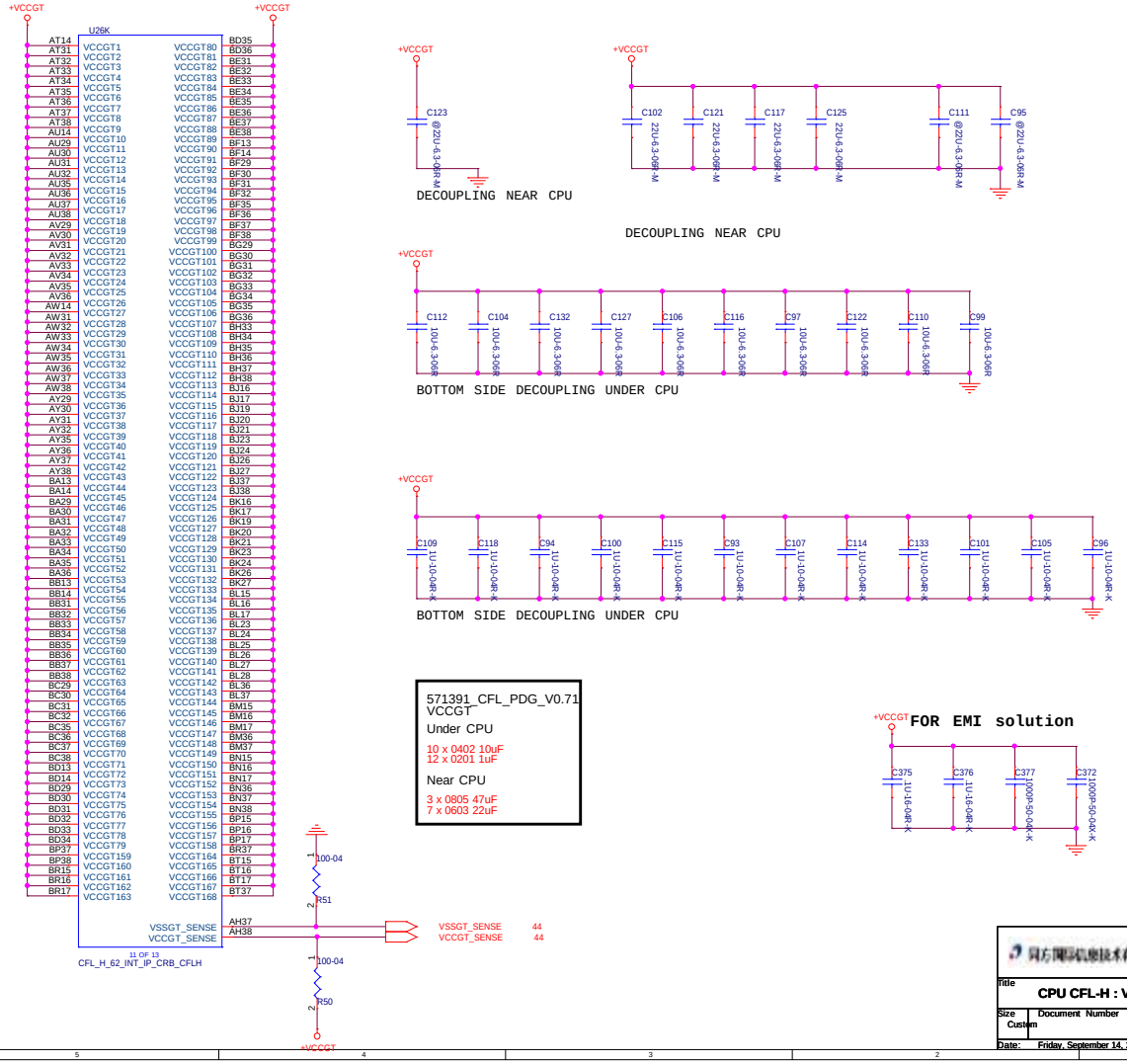
CFL_H_62_INT_IP_CRB_CFLH
U26J
CFL_H_62_INT_IP_CRB_CFLH
VCORE_VCCSENSE
VCORE_VSSSENSE
Catch resistor
FOR EMI solution
571391_CFL_PDG_V0.71
VCC
Under CPU
12 x 0603 22uF
21 x 0402 10uF
24 x 0201 1uF
24 x 0201 N/A
Near CPU
5 x 0805 47uF
DECOUPLING NEAR CPU
BOTTOM SIDE DECOUPLING UNDER CPU
BOTTOM SIDE DECOUPLING UNDER CPU
BOTTOM SIDE DECOUPLING UNDER CPU
BOTTOM SIDE DECOUPLING UNDER CPU
BOTTOM SIDE DECOUPLING UNDER CPU
Tong Fang(Suzhou)
CPU CFL-H : VCC
GK5CN6X
Friday, September 14, 2018



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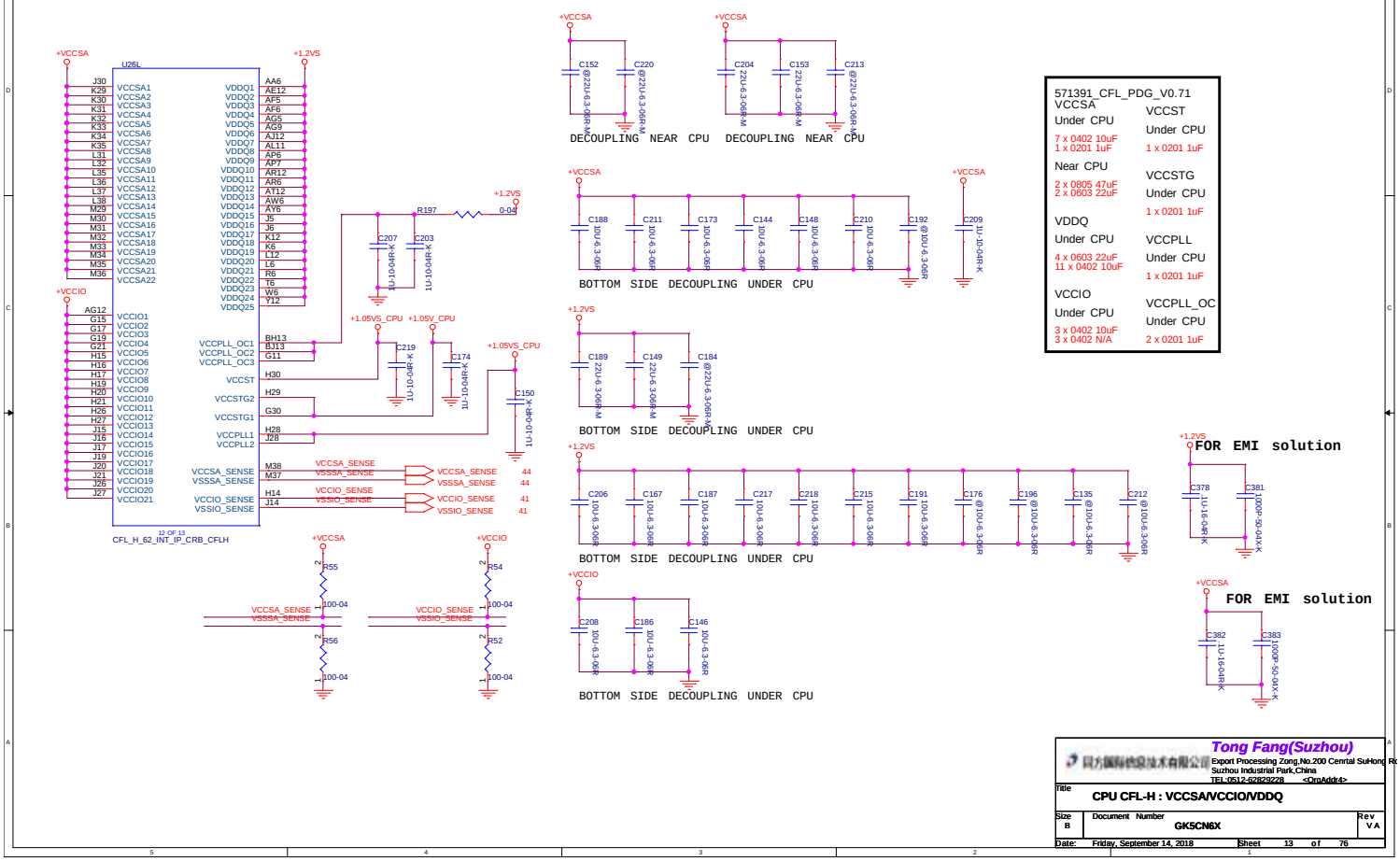
Title	CPU CFL-H : VCCGT	
Size: Custom	Document Number: GK5CN6X	Rev: V A
Date: Friday, September 14, 2018	Sheet 12 of 76	



571391_CFL_PDG_V0.71

VCCSA
Under CPU
7 x 0402 10uF
1 x 0201 1uF
Near CPU
2 x 0805 47uF
2 x 0603 22uF
VDDQ
Under CPU
4 x 0603 22uF
11 x 0402 10uF
VCCIO
Under CPU
3 x 0402 10uF
3 x 0402 N/A

VCCST
Under CPU
1 x 0201 1uF
VCCSTG
Under CPU
1 x 0201 1uF
VCCPLL
Under CPU
1 x 0201 1uF
VCCPLL_OC
Under CPU
2 x 0201 1uF

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Title: CPU CFL-H : VCCSA/VCCIO/VDDQ

Size	Document Number	Rev
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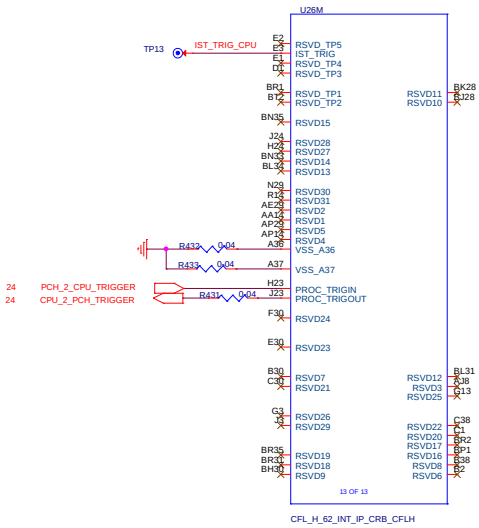
Date: Friday, September 14, 2018 Sheet 13 of 76



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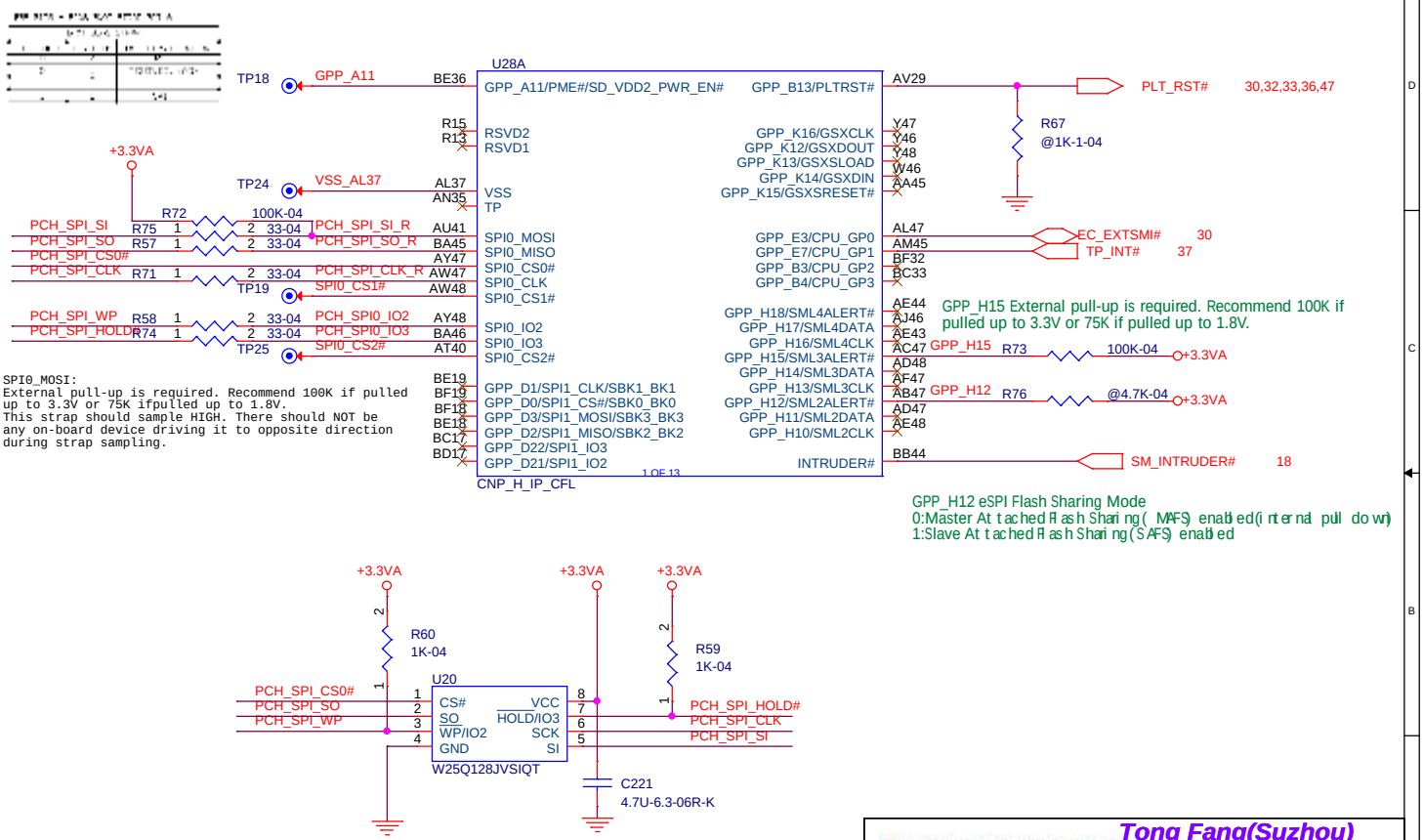
Title: CPU CFL-H : TRIG/RSVD

Size	Document Number	Rev
B	GK5CN6X	V A

Date: Friday, September 14, 2018 Sheet 14 of 76



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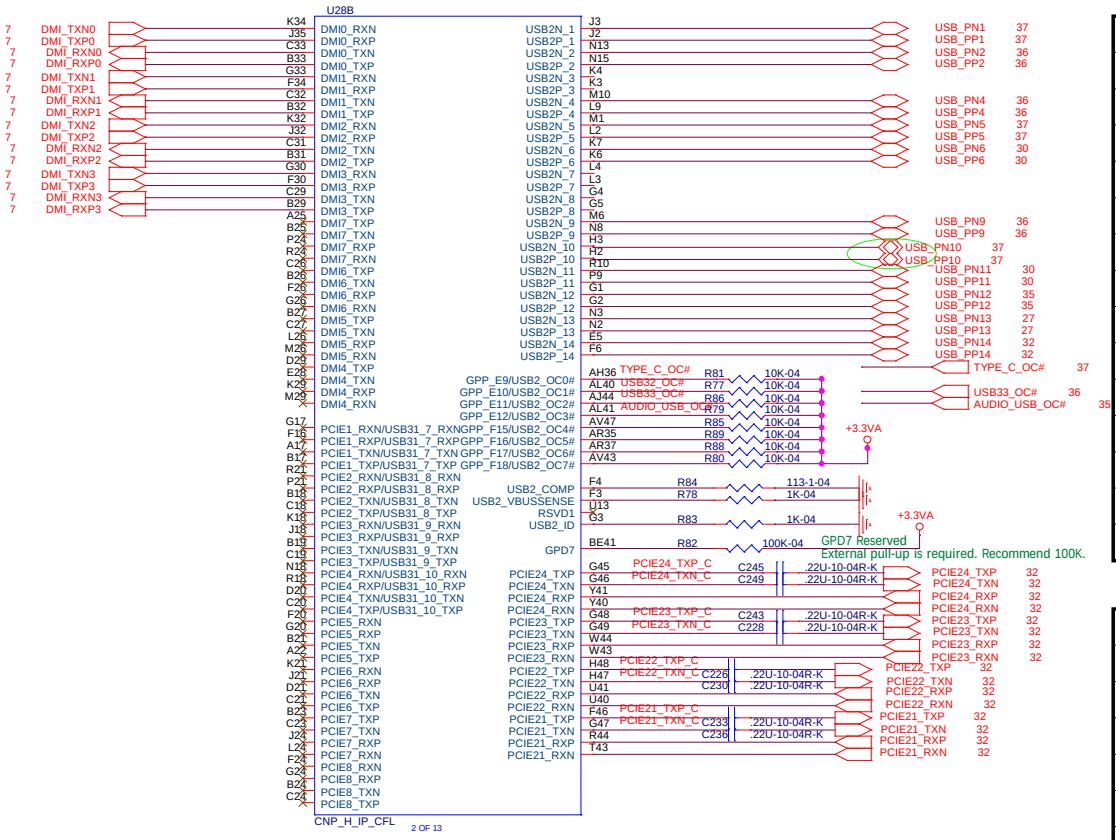
Title	PCH CFL-H : SPI	
Size A	Document Number GK5CN6X	Rev V A
Date: Friday, September 14, 2018	Sheet 15 of 76	



USB2.0 Configuration Table	
USB1	TYPE-C Port
USB2	CardReader on USB3.0 DB
USB3	N/A
USB4	USB3.0 Port1 on USB3.0 DB
USB5	TYPE-C Port
USB6	ME Keyboard CONN
USB7	N/A
USB8	N/A
USB9	USB3.0 Port2 on USB3.0 DB
USB10	N/A
USB11	USB3.0 Port1 on USB3.0 DB
USB12	USB2.0 PORT on Audio DB
USB13	Web Camera
USB14	Bluetooth

USB OC Configuration Table	
OC0	TYPE_C_OC#
OC1	N/A
OC2	USB3.0 DB
OC3	AUDIO_USB DB
OC4	N/A
OC5	N/A
OC6	N/A
OC7	N/A

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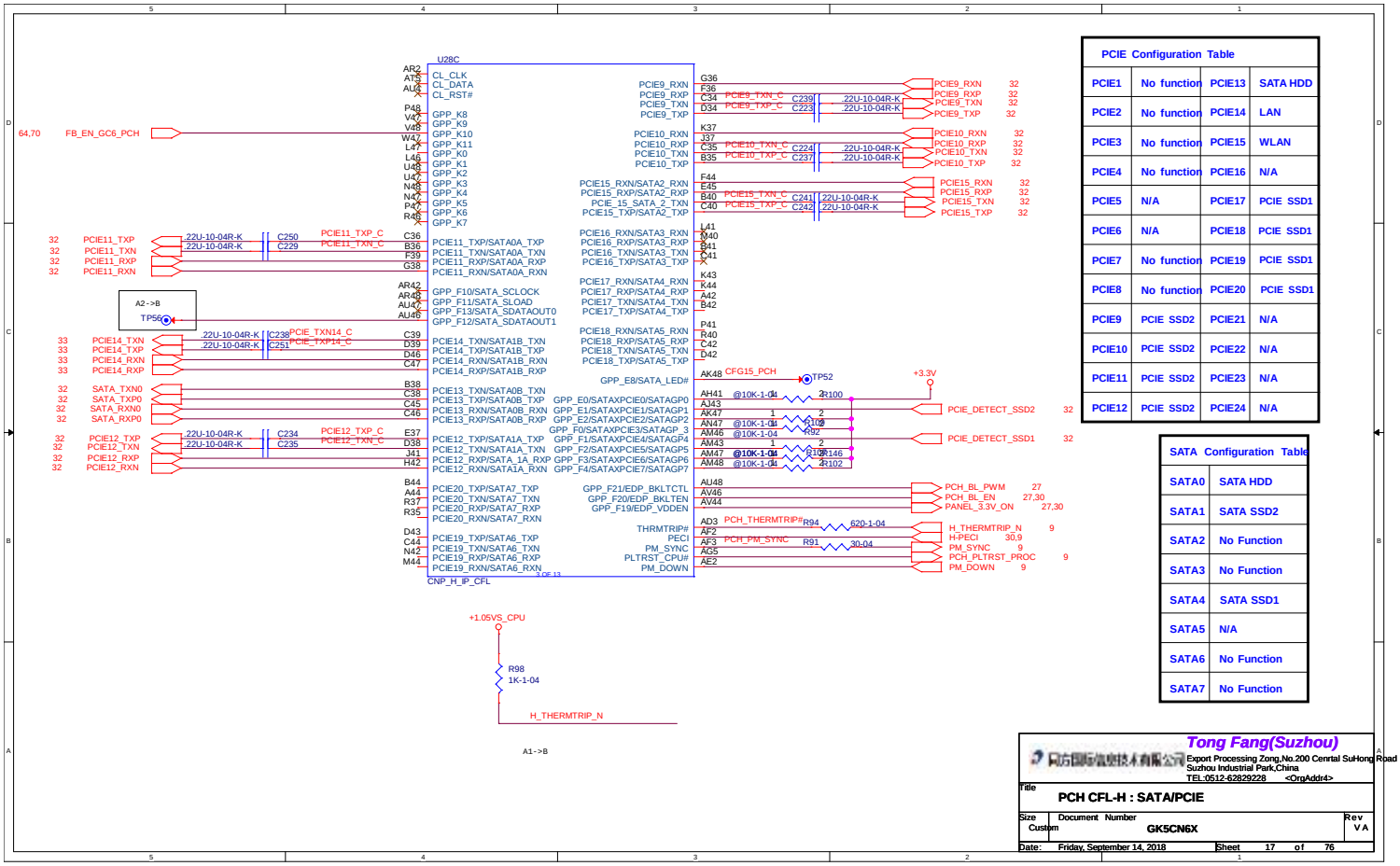
Title: PCH CFL-H : DMI/USB2.0

Size: Custom | Document Number: GK5CN6X | Rev: V A

Date: Friday, September 14, 2018 | Sheet 16 of 76



PCIE Configuration Table			
PCIE1	No function	PCIE13	SATA HDD
PCIE2	No function	PCIE14	LAN
PCIE3	No function	PCIE15	WLAN
PCIE4	No function	PCIE16	N/A
PCIE5	N/A	PCIE17	PCIE SSD1
PCIE6	N/A	PCIE18	PCIE SSD1
PCIE7	No function	PCIE19	PCIE SSD1
PCIE8	No function	PCIE20	PCIE SSD1
PCIE9	PCIE SSD2	PCIE21	N/A
PCIE10	PCIE SSD2	PCIE22	N/A
PCIE11	PCIE SSD2	PCIE23	N/A
PCIE12	PCIE SSD2	PCIE24	N/A

SATA Configuration Table	
SATA0	SATA HDD
SATA1	SATA SSD2
SATA2	No Function
SATA3	No Function
SATA4	SATA SSD1
SATA5	N/A
SATA6	No Function
SATA7	No Function

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Title: PCH CFL-H : SATA/PCIE

Size: Custom | Document Number: GK5CN6X | Rev: V A

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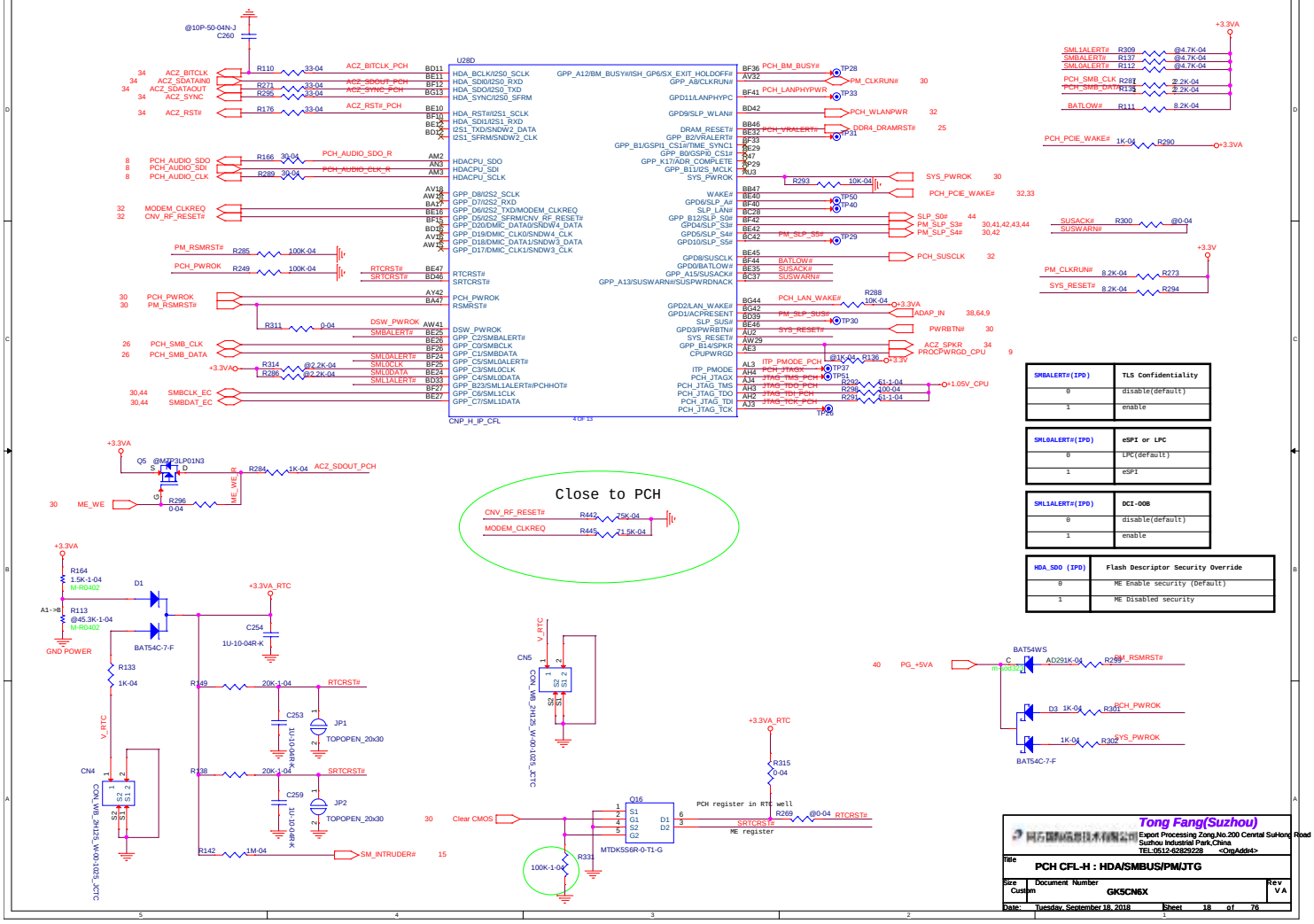
U28D
HDA_BCLK/I2S0_SCLK
HDA_SDO/I2S0_RXD
HDA_SDI/I2S0_TXD
HDA_SYNC/I2S0_SFRM
HDA_RST#/I2S1_SCLK
HDA_SDI1/I2S1_RXD
I2S1_TXD/SNDW2_DATA
I2S1_SFRM/SNDW2_CLK
HDACPU_SDO
HDACPU_SDI
HDACPU_SCLK
GPP_D8/I2S2_SCLK
GPP_D7/I2S2_RXD
GPP_D6/I2S2_TXD/MODEM_CLKREQ
GPP_D5/I2S2_SFRM/CNV_RF_RESET#
GPP_D20/DMIC_DATA0/SNDW4_DATA
GPP_D19/DMIC_CLK0/SNDW4_CLK
GPP_D18/DMIC_DATA1/SNDW3_DATA
GPP_D17/DMIC_CLK1/SNDW3_CLK
RTCRST#
SRTCRST#
PCH_PWROK
RSMRST#
DSW_PWROK
GPP_C2/SMBALERT#
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C5/SML0ALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_B23/SML1ALERT#/PCHHOT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
GPP_A12/BM_BUSY#/ISH_GP6/SX_EXIT_HOLDOFF#
GPP_A8/CLKRUN#
GPD11/LANPHYPC
GPD9/SLP_WLAN#
DRAM_RESET#
GPP_B2/VRALERT#
GPP_B1/GSPI1_CS1#/TIME_SYNC1
GPP_B0/GSPI0_CS1#
GPP_K17/ADR_COMPLETE
GPP_B11/I2S_MCLK
SYS_PWROK
WAKE#
GPD6/SLP_A#
SLP_LAN#
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
GPD8/SUSCLK
GPD0/BATLOW#
GPP_A15/SUSACK#
GPP_A13/SUSWARN#/SUSPWRDNACK
GPD2/LAN_WAKE#
GPD1/ACPRESENT
SLP_SUS#
GPD3/PWRBTN#
SYS_RESET#
GPP_B14/SPKR
CPUPWRGD
ITP_PMODE
PCH_JTAGX
PCH_JTAG_TMS
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TCK
CNP_H_IP_CFL
4 OF 13
Close to PCH
CNV_RF_RESET#
MODEM_CLKREQ
R442 75K-04
R445 71.5K-04
SMBALERT#(IPD)
TLS Confidentiality
0 disable(default)
1 enable
SML0ALERT#(IPD)
eSPI or LPC
0 LPC(default)
1 eSPI
SML1ALERT#(IPD)
DCI-OOB
0 disable(default)
1 enable
HDA_SDO (IPD)
Flash Descriptor Security Override
0 ME Enable security (Default)
1 ME Disabled security
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Title
PCH CFL-H : HDA/SMBUS/PM/JTG
Size Custom
Document Number GK5CN6X
Rev V A
Date: Tuesday, September 18, 2018
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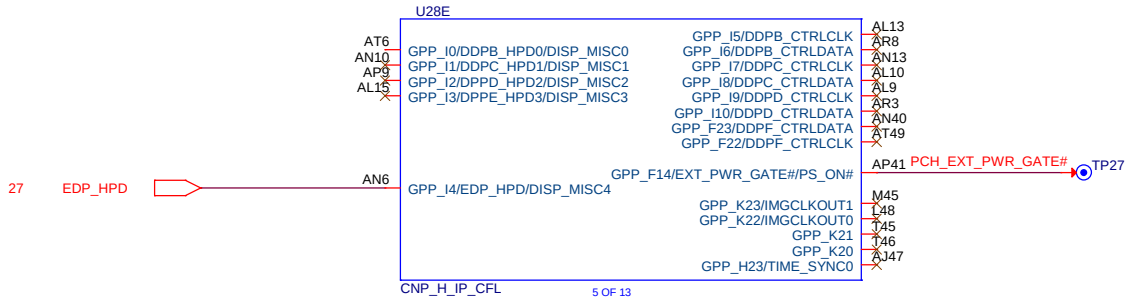

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Title	PCH CFL-H : DDI CONTROL	
Size A	Document Number GK5CN6X	Rev V A
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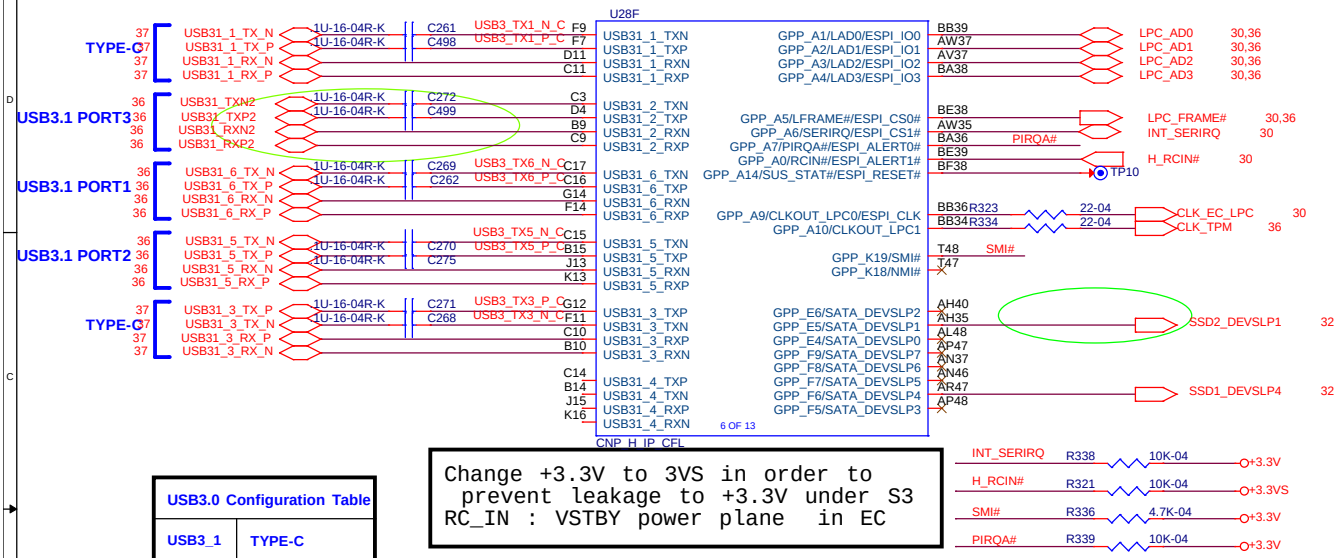

USB3.0 Configuration Table	
USB3_1	TYPE-C
USB3_2	N/A
USB3_3	TYPE-C
USB3_4	N/A
USB3_5	USB3.0 Port2
USB3_6	USB3.0 Port1
USB3_7	N/A
USB3_8	N/A
USB3_9	No Function
USB3_10	No Function

Change +3.3V to 3VS in order to prevent leakage to +3.3V under S3
RC_IN : VSTBY power plane in EC

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Title: PCH CFL-H : USB3.0/LPC

Size: Custom | Document Number: GK5CN6X | Rev: V A

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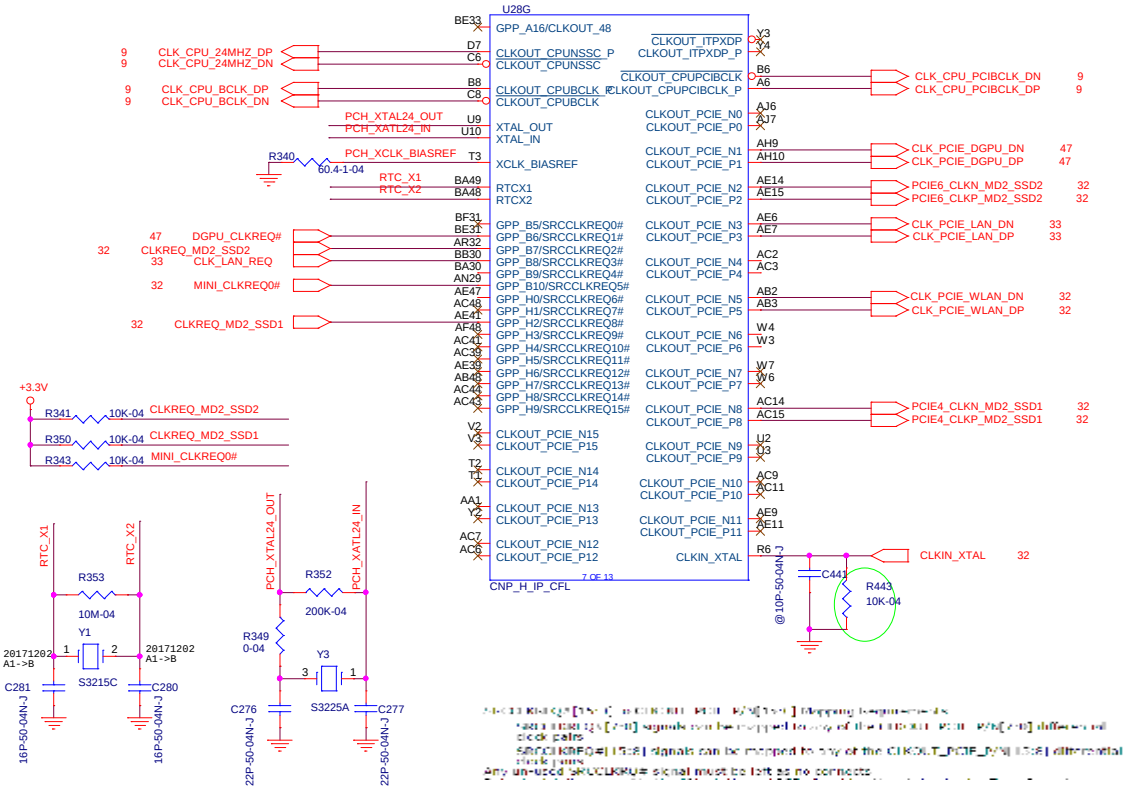

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Title	PCH CFL-H : CLK
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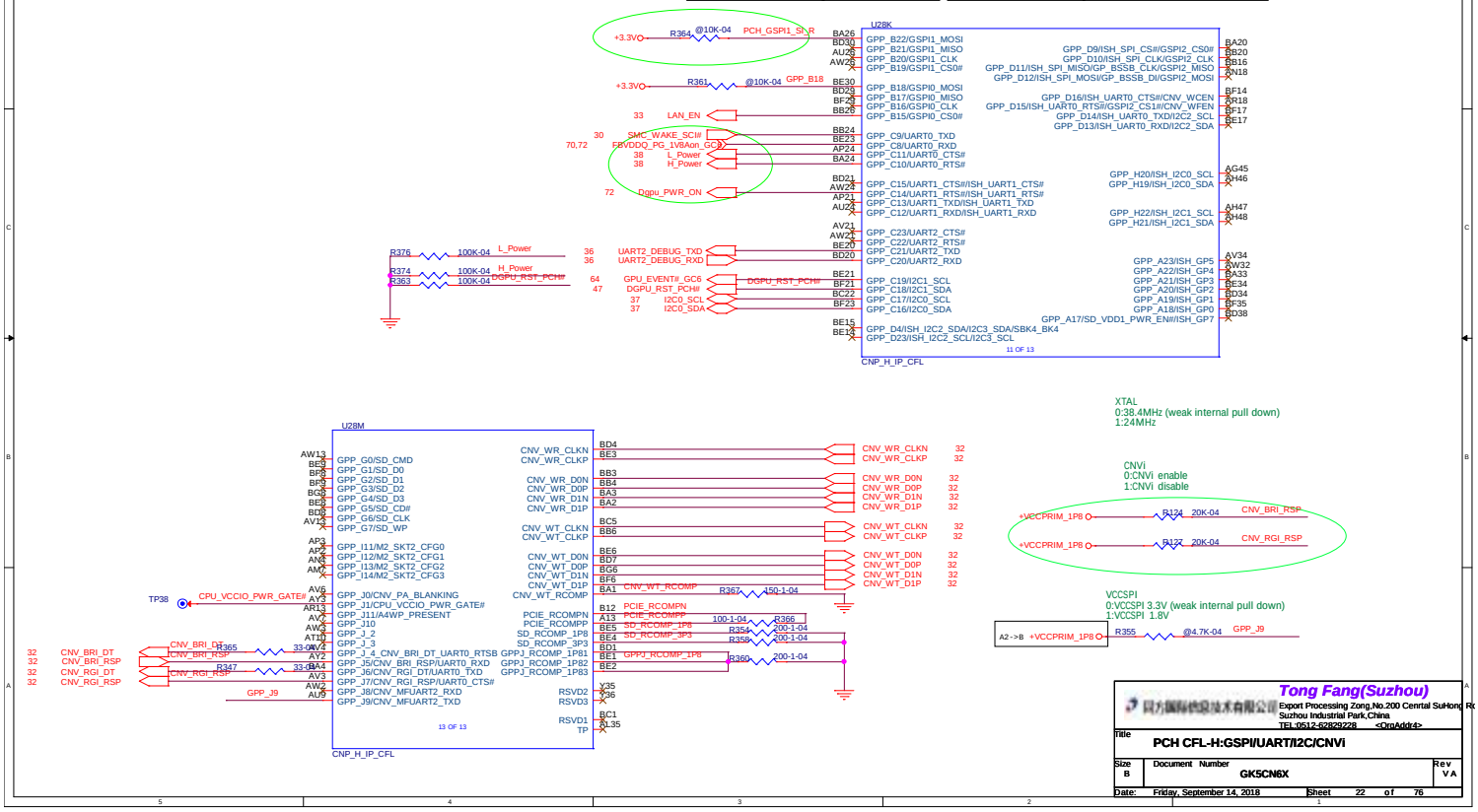
GPP_B22/GSPI1_MOSI(IPD)	Boot BIOS Strap Bit
0(weak internal pull down)	SPI
1	LPC

GPP_B18/GSPI0_MOSI(IPD)	No Reboot
0	Disable No Reboot mode (Default)
1	Enable No Reboot mode



XTAL
0:38.4MHz (weak internal pull down)
1:24MHz

CNVi
0:CNVi enable
1:CNVi disable

VCCSPI
0:VCCSPI 3.3V (weak internal pull down)
1:VCCSPI 1.8V

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Title: PCH CFL-H:GSPI/UART/I2C/CNVi

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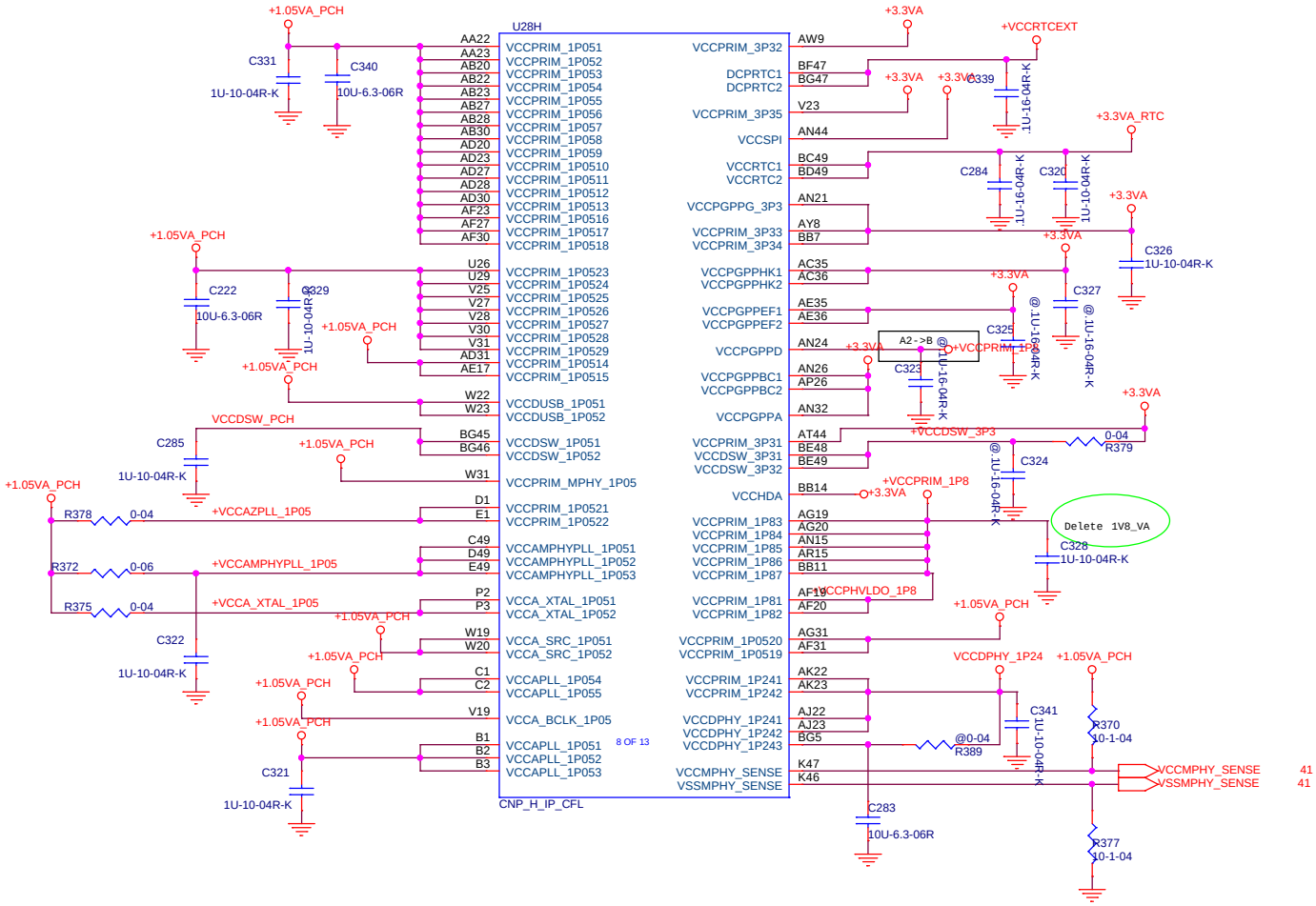
Date: Friday, September 14, 2018 Sheet 22 of 76



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Title	PCH CFL-H : POWER
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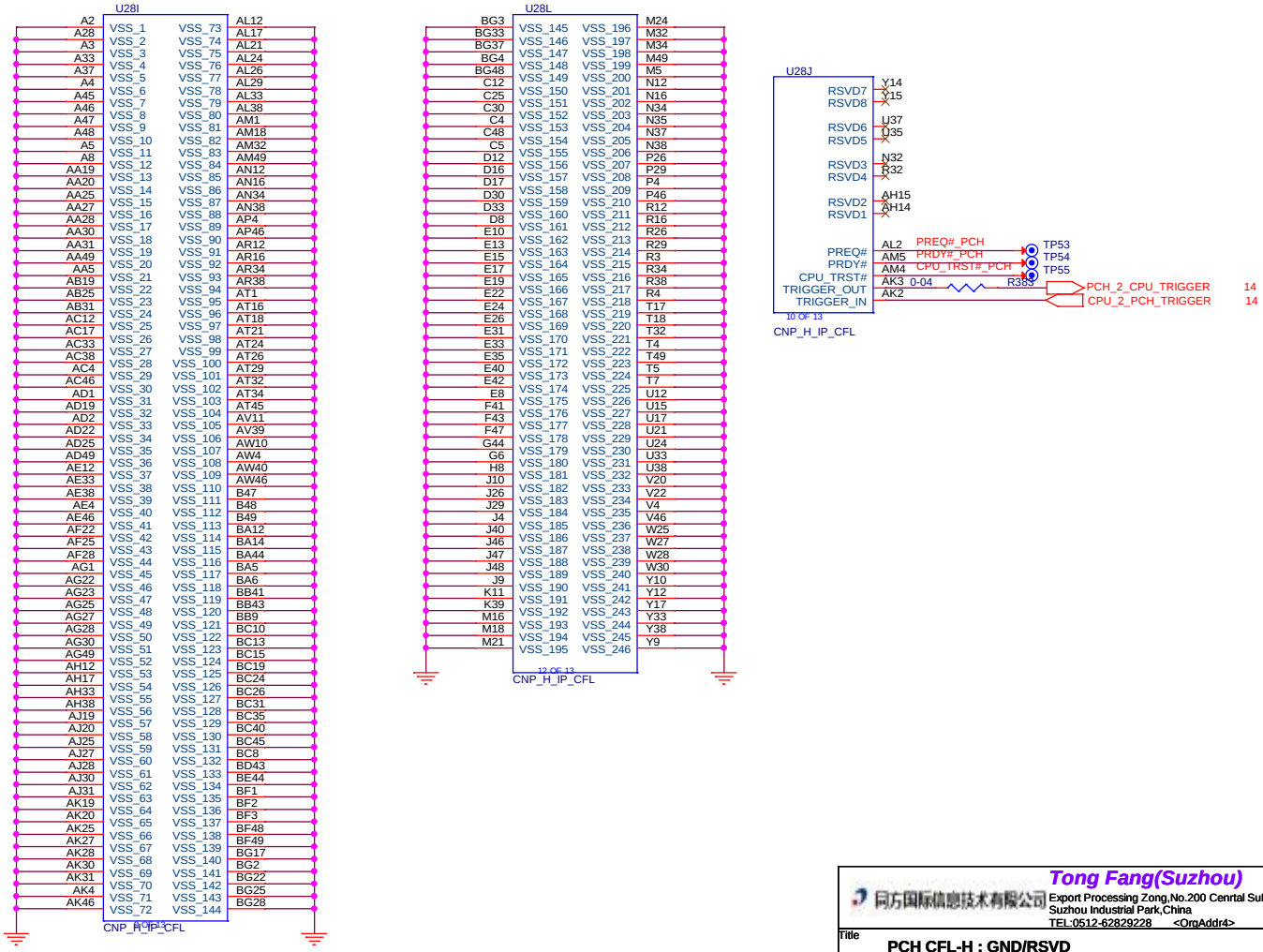

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Title: PCH CFL-H : GND/RSVD

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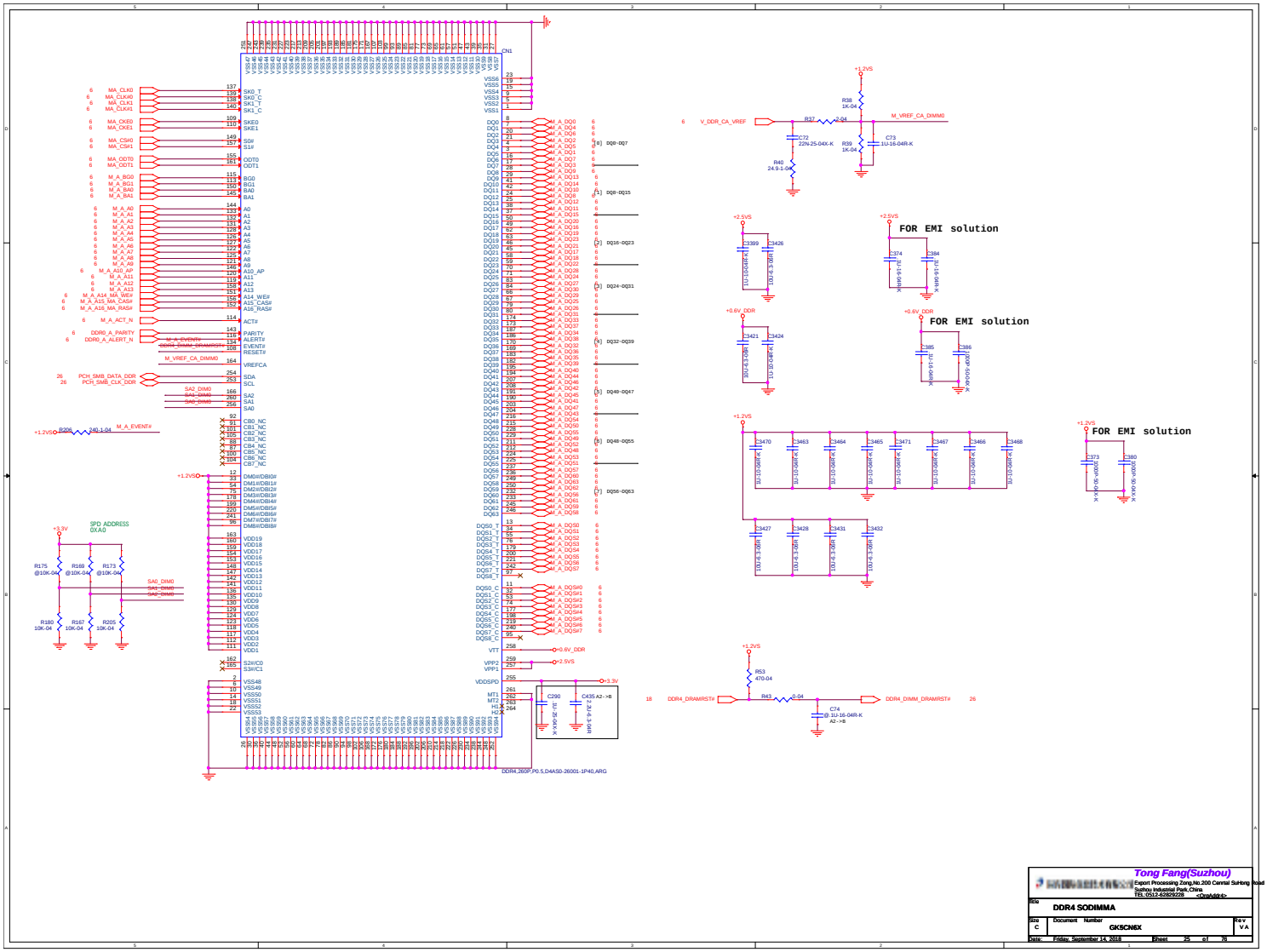

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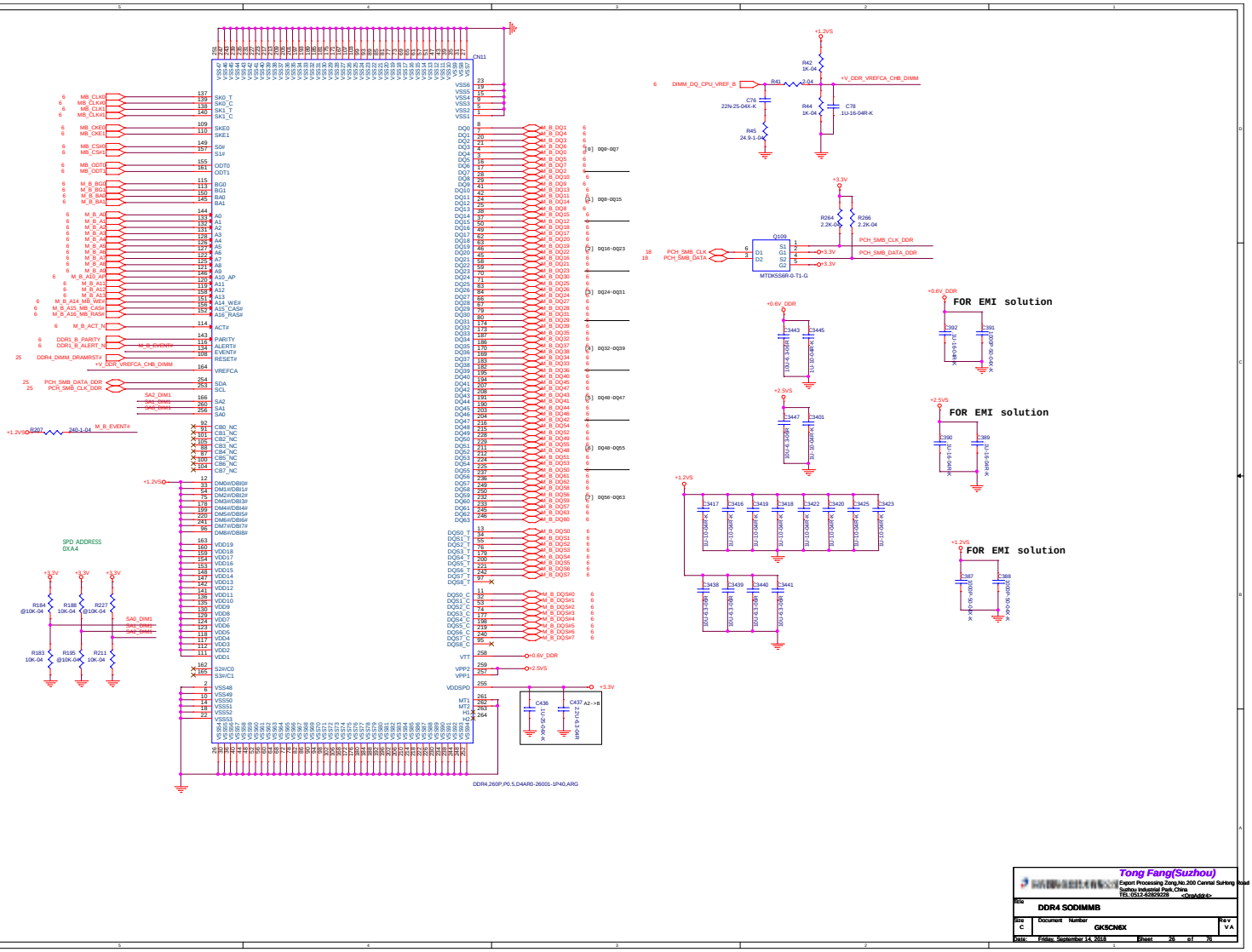
Title
DDR4 SODIMMA
Size C
Document Number GKSCN6X
Rev V.A
Date: Friday, September 14, 2018 Sheet 25 of 78



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Title	DDR4 SODIMMB		
Size: C	Document Number: GK5CN6X		Rev: V.A
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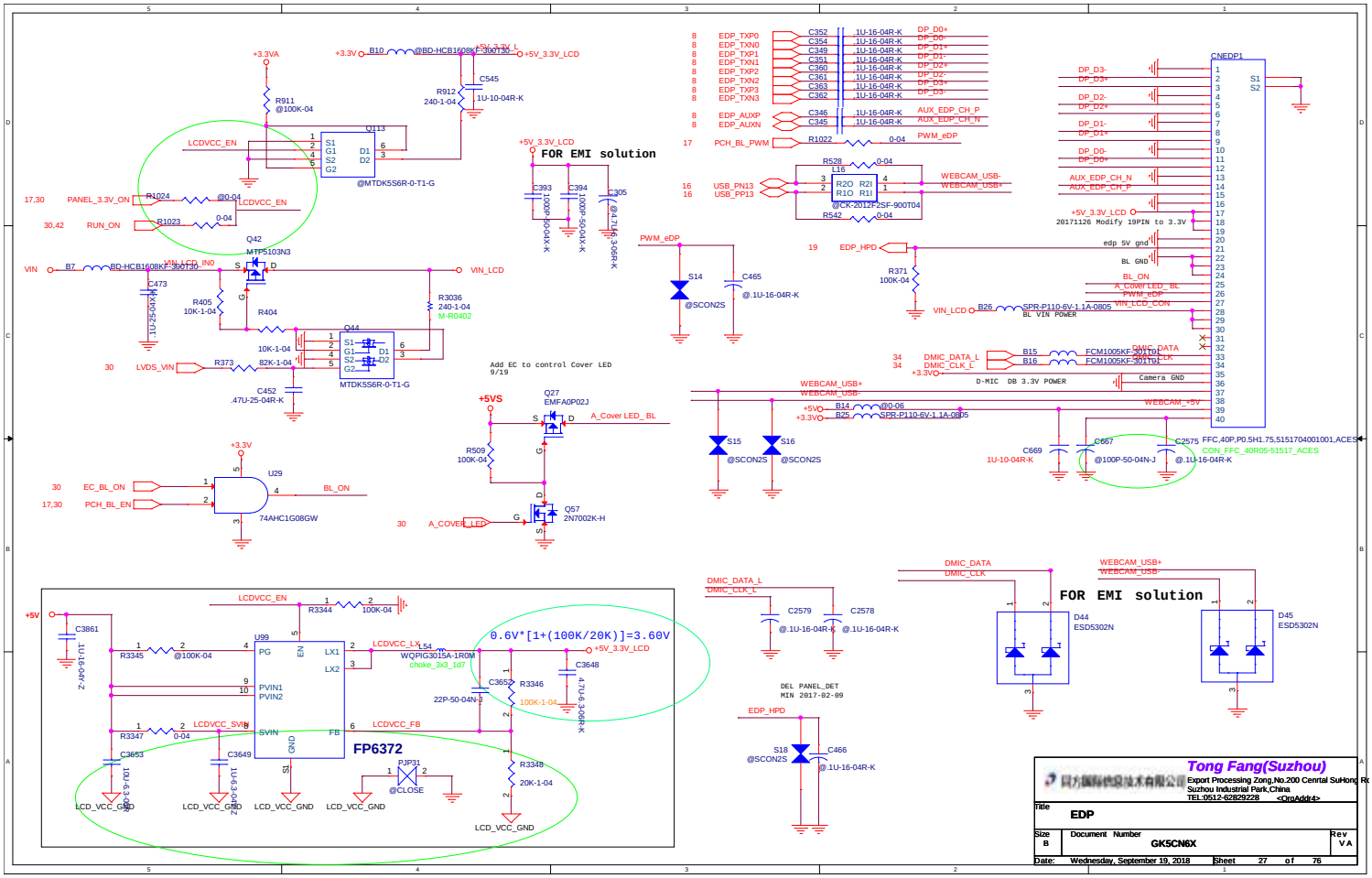
FOR EMI solution
Add EC to control Cover LED 9/19
FP6372
0.6V*[1+(100K/20K)]=3.60V
DEL PANEL_DET MIN 2017-02-09
FOR EMI solution
CNEDP1
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Title
EDP
Size B
Document Number GK5CN6X
Rev V.A
Date: Wednesday, September 19, 2018
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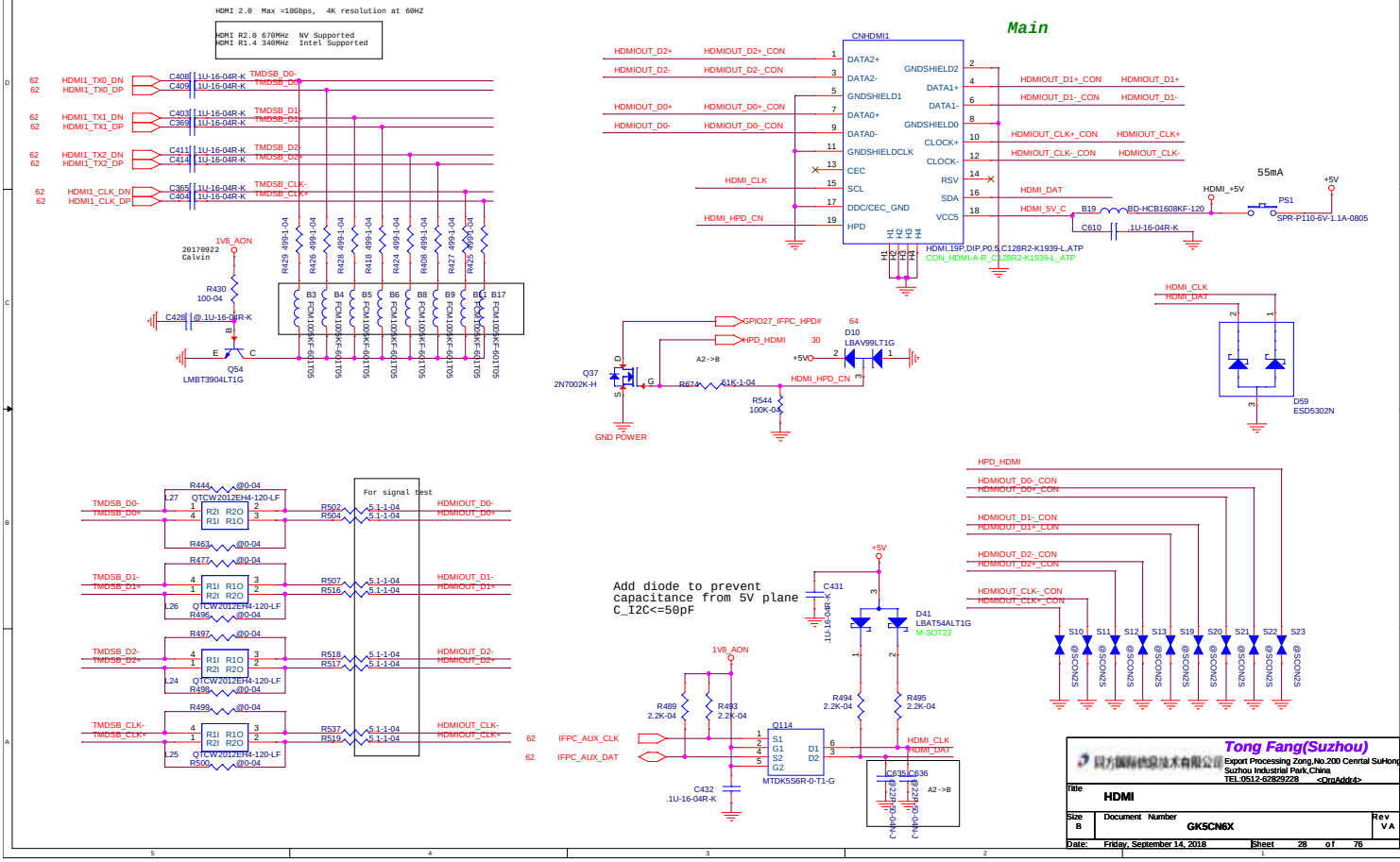
HDMI CONN

Main

HDMI 2.0 Max =18Gbps, 4K resolution at 60HZ

HDMI R2.0 670MHz NV Supported
HDMI R1.4 340MHz Intel Supported



Add diode to prevent capacitance from 5V plane
C_I2C<=50pF

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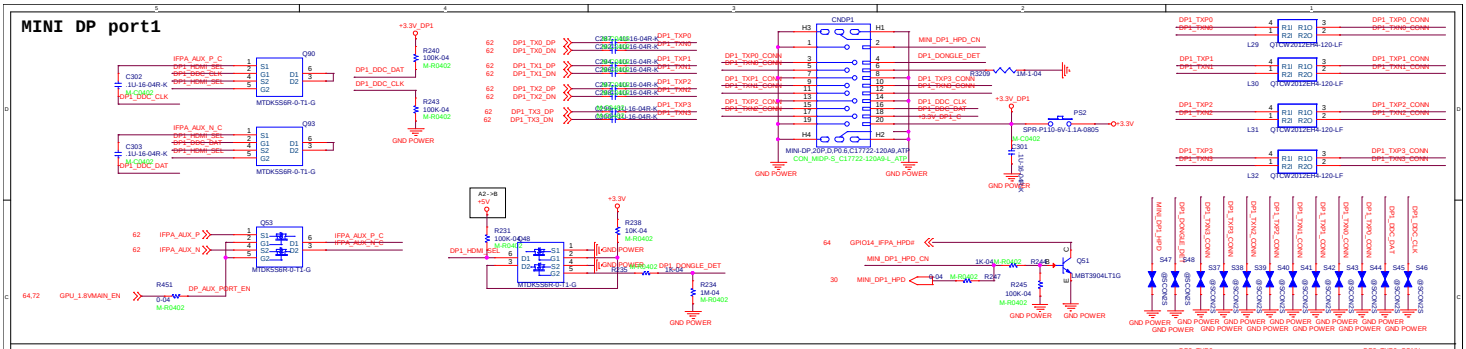
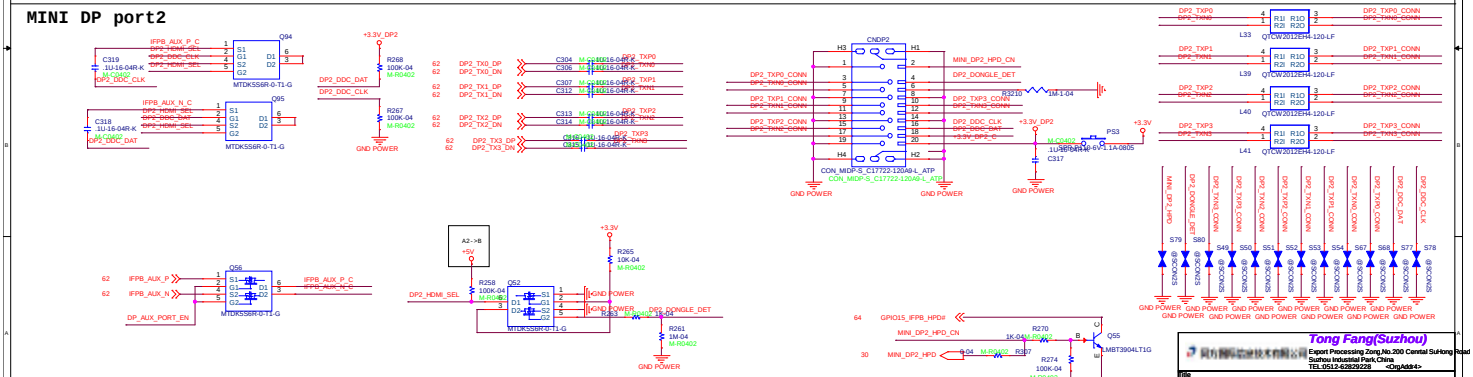
Title: HDMI			
Size: B	Document Number: GK5CN6X		Rev: V.A
Date: Friday, September 14, 2018	Sheet: 28 of 76		

MINI DP port1



MINI DP port2



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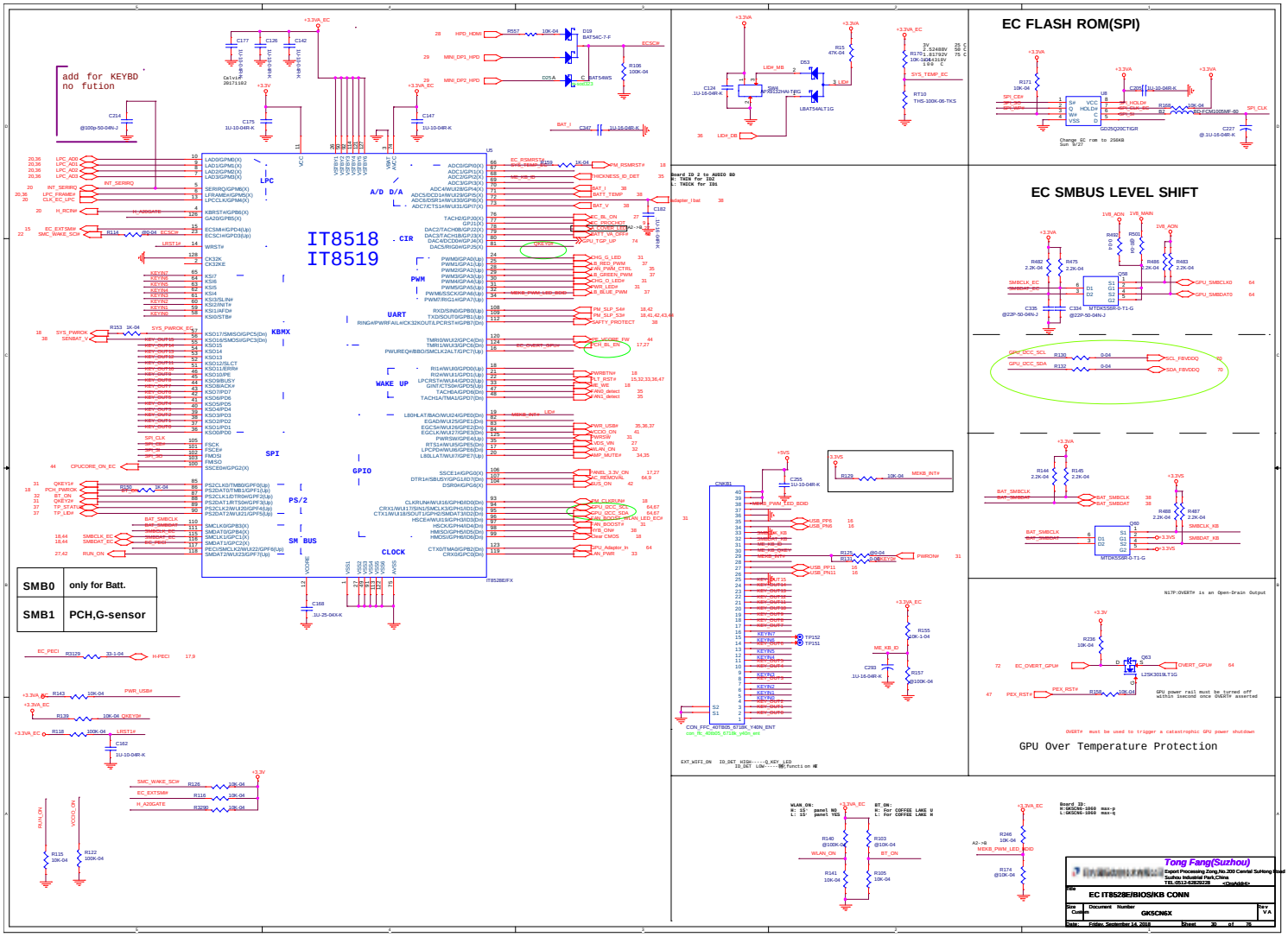
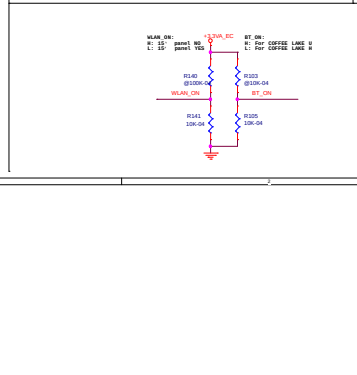
Title	Mini DP		
Size: Custom	Document Number: GK5CN6X		Rev: V.A
Date: Friday, September 14, 2018	Sheet 29 of 76		

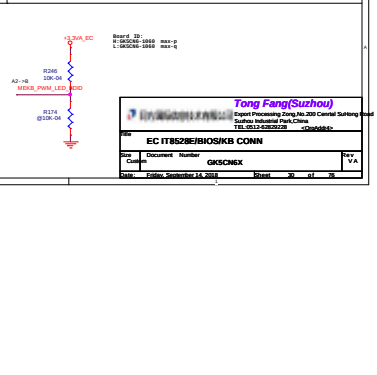

add for KEYBD
no futions
IT8518
IT8519
LPC
A/D D/A
CIR
PWM
UART
WAKE UP
GPIO
SPI
PS/2
SM BUS
CLOCK
KBMX
SMB0 only for Batt.
SMB1 PCH,G-sensor

EC FLASH ROM(SPI)

Board ID 2 to ADDIO 8D
H: THIN for IBZ
L: THICK for IDL

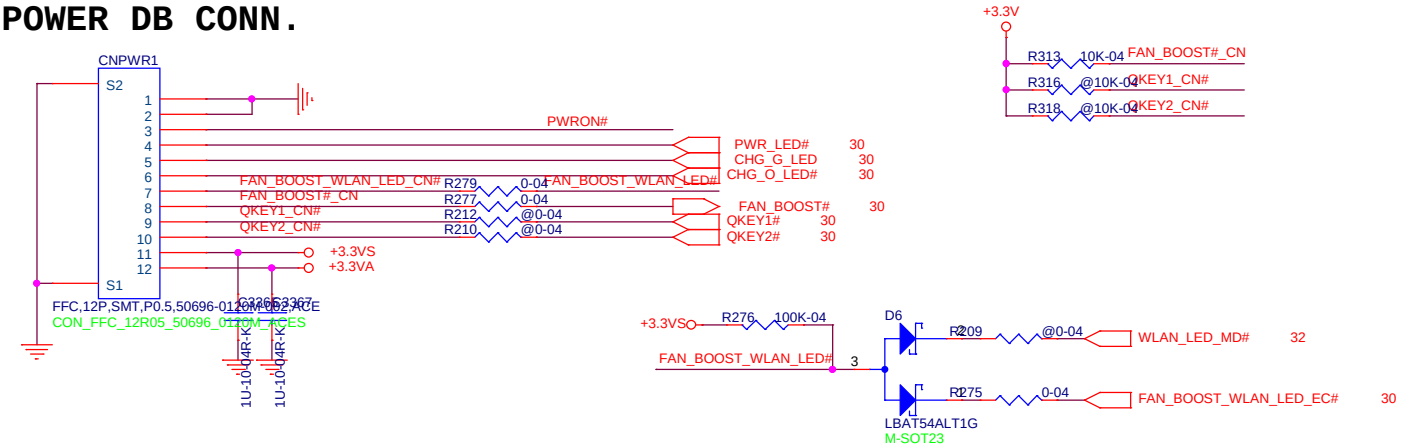
EC SMBUS LEVEL SHIFT



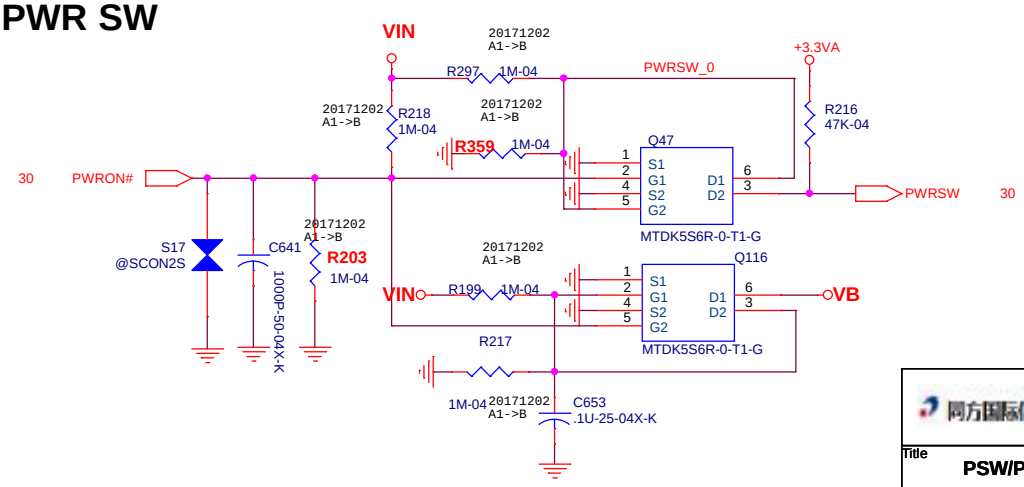


GPU Over Temperature Protection

POWER DB CONN.



PWR SW



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Title	PSW/PWR DB CON	
Size A	Document Number GK5CN6X	Rev V A
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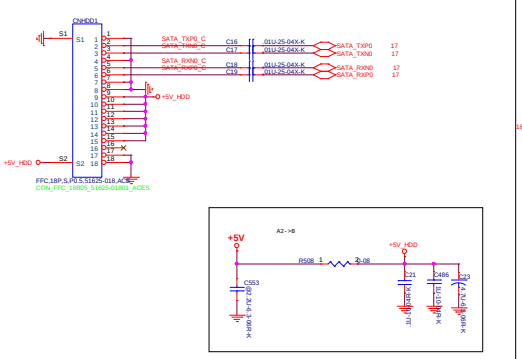
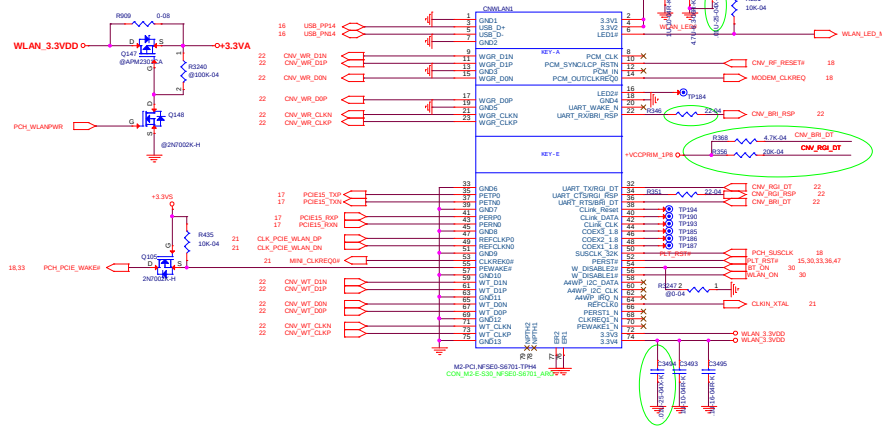
SATA-HDD

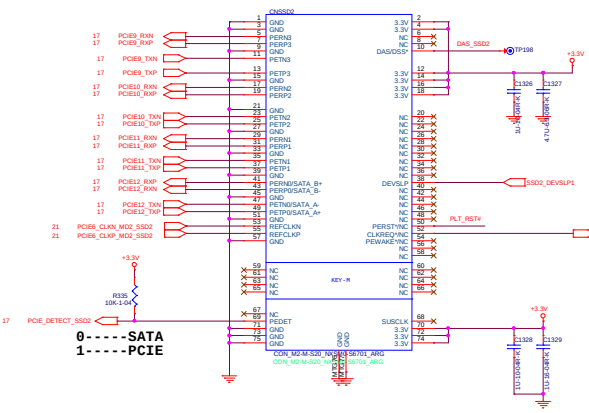


M.2 WIFI

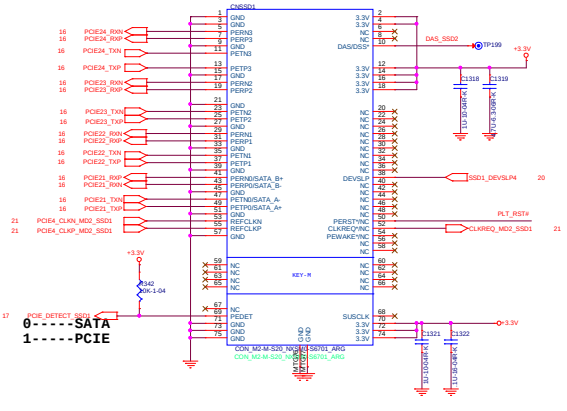


M.2 SSD

SSD2



SSD1



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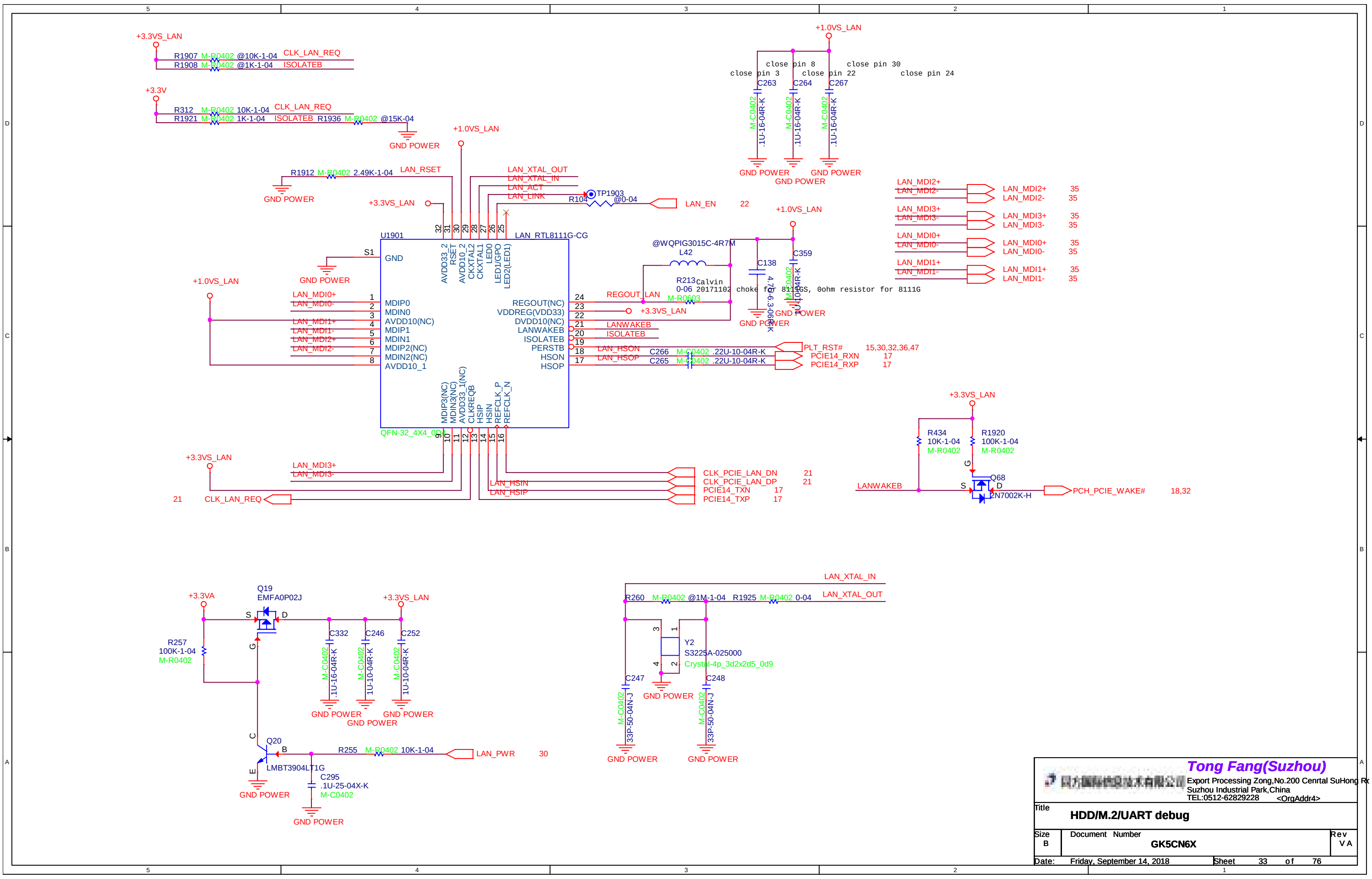
Title	LAN RTL8111		
Size: C	Document Number: GK5CN6X		Rev: V.A
Date: Tuesday, September 18, 2018	Sheet 32 of 78		


LAN_RTL8111G-CG
U1901
REGOUT_LAN
LAN_XTAL_OUT
LAN_XTAL_IN
LAN_EN
PLT_RST#
PCIE14_RXN
PCIE14_RXP
CLK_PCIE_LAN_DN
CLK_PCIE_LAN_DP
PCIE14_TXN
PCIE14_TXP
CLK_LAN_REQ
LANWAKEB
PCH_PCIE_WAKE#
LAN_PWR
GND POWER
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Title
HDD/M.2/UART debug
Size B
Document Number GK5CN6X
Rev VA
Date: Friday, September 14, 2018
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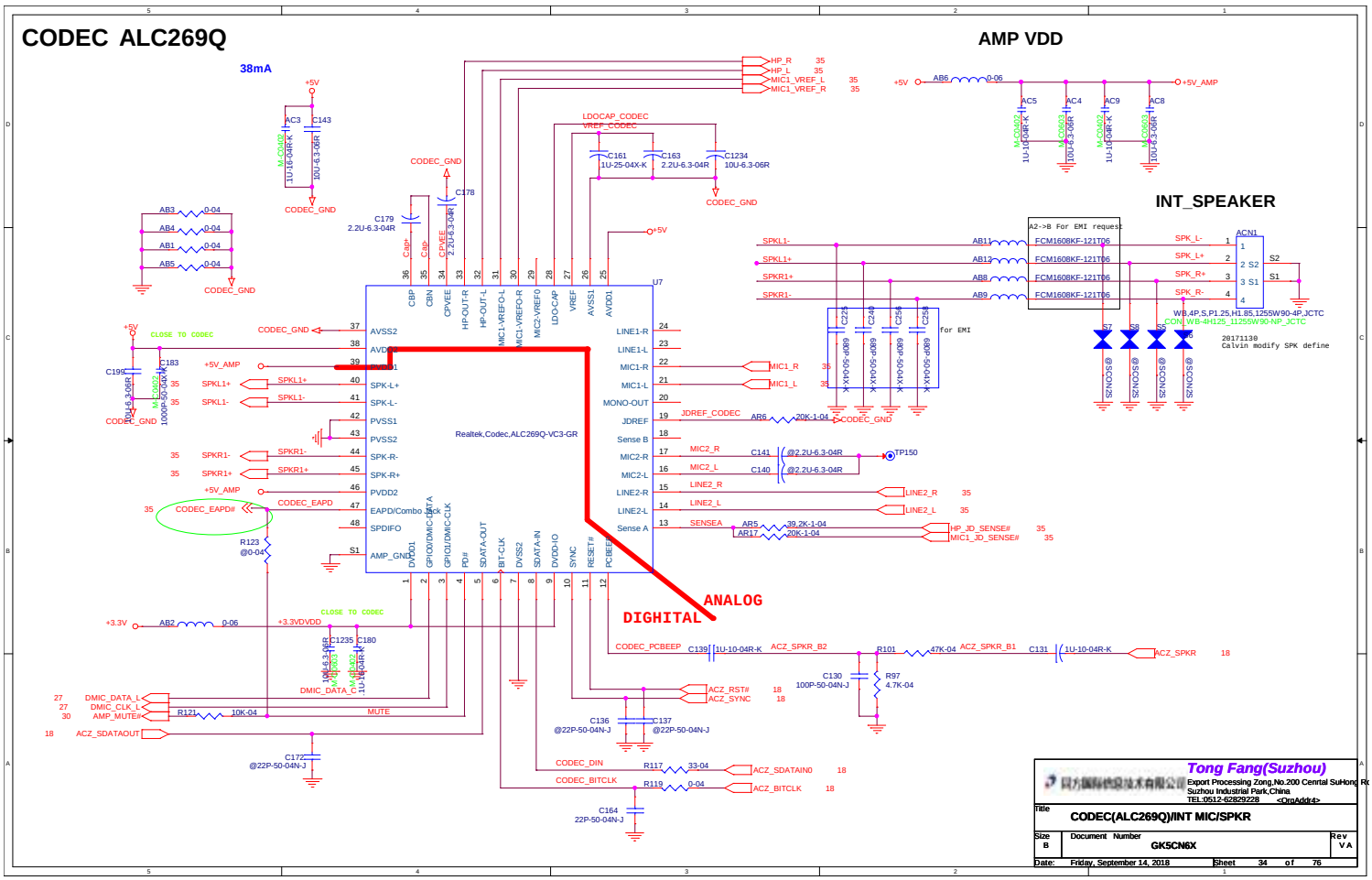
CODEC ALC269Q
38mA
AMP VDD
INT_SPEAKER
Realtek,Codec,ALC269Q-VC3-GR
U7
ANALOG
DIGHITAL
CLOSE TO CODEC
for EMI
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Title
CODEC(ALC269Q)/INT MIC/SPKR
Size B
Document Number
GK5CN6X
Rev V A
Date: Friday, September 14, 2018
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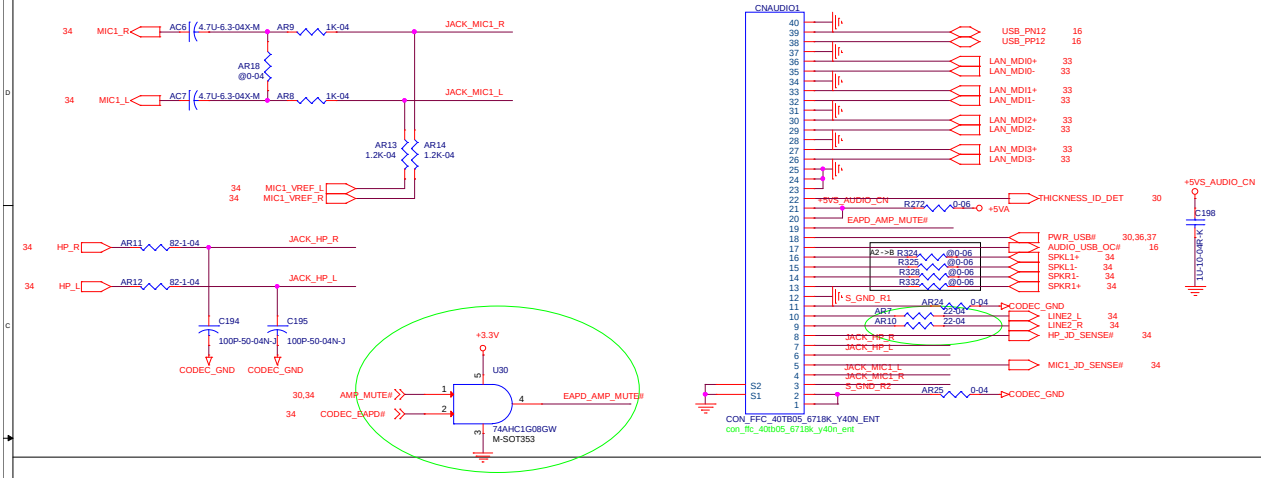
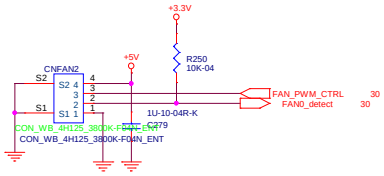
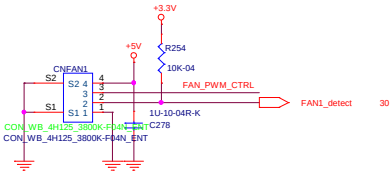
EXT MIC / EXT LINE IN / EXT USB JACK



FAN CONTROLLER 0



FAN CONTROLLER 1



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Title	EXT_AUDIO/EXT_USB/FAN	
Size B	Document Number GK5CN6X	Rev V.A
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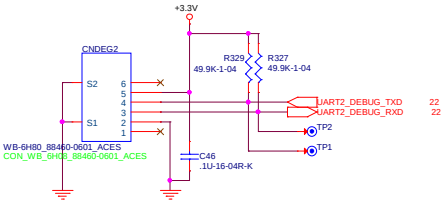
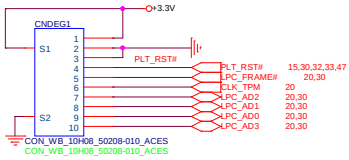
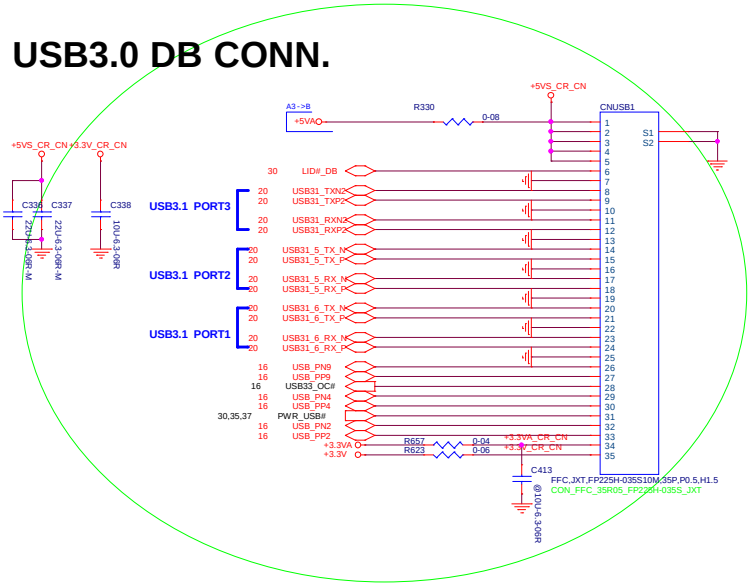
UART debug port



LPC debug port



USB3.0 DB CONN.



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Title: EXT USB3.0

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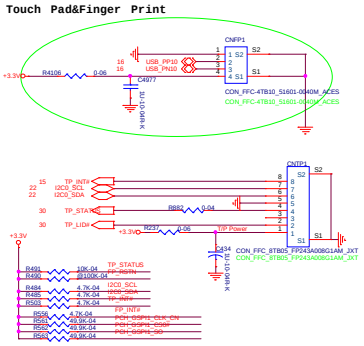
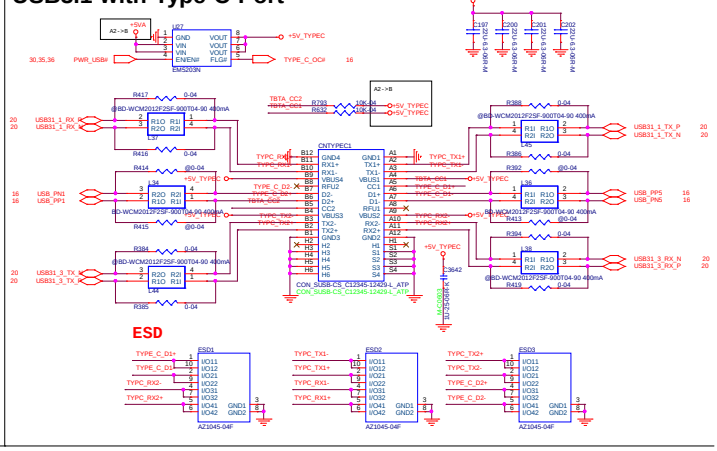
Touch Pad&Finger Print

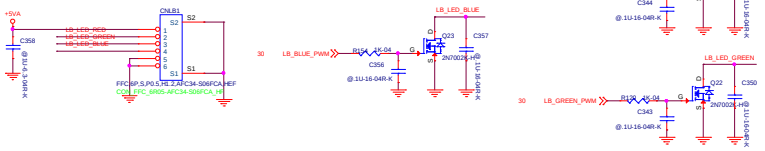


USB3.1 with Type-C Port



ESD

Light bar Control



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Title	TP/USB/TYPEC		
Size: C	Document Number: GK5CN6X		Rev: V.A
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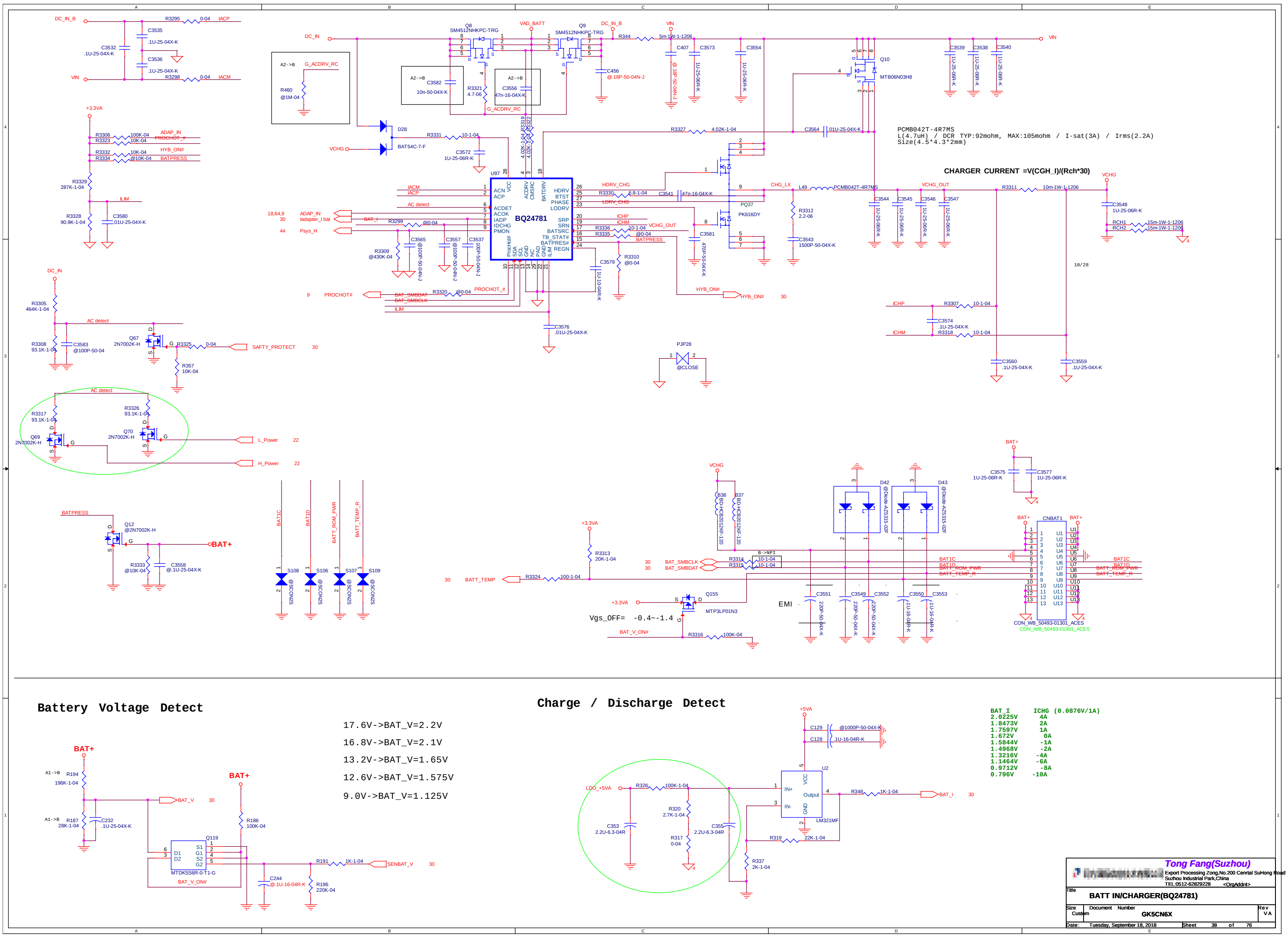
BQ24781
CHARGER CURRENT =V(CGH_I)/(Rch*30)
PCMB042T-4R7MS
L(4.7uH) / DCR TYP:92mohm, MAX:105mohm / I-sat(3A) / Irms(2.2A)
Size(4.5*4.3*2mm)
Vgs_OFF= -0.4~-1.4
EMI
Battery Voltage Detect
17.6V->BAT_V=2.2V
16.8V->BAT_V=2.1V
13.2V->BAT_V=1.65V
12.6V->BAT_V=1.575V
9.0V->BAT_V=1.125V
Charge / Discharge Detect
BAT_I ICHG (0.0876V/1A)
2.0225V 4A
1.8473V 2A
1.7597V 1A
1.672V 0A
1.5844V -1A
1.4968V -2A
1.3216V -4A
1.1464V -6A
0.9712V -8A
0.796V -10A
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BATT IN/CHARGER(BQ24781)
GK5CN6X
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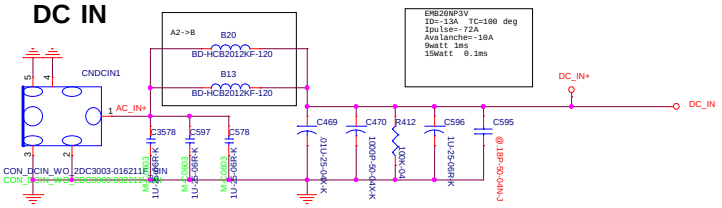
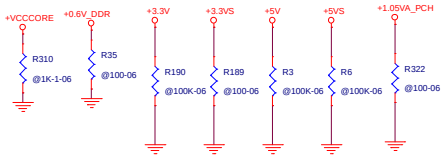
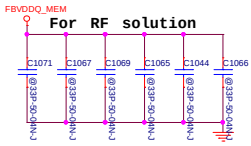
DC IN



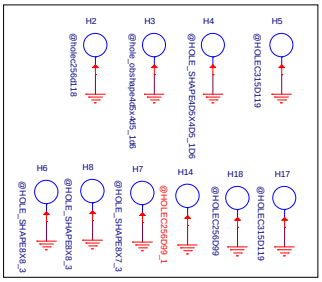
Discharge Resistor



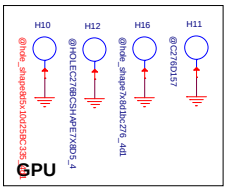
HIGH-SPEED CAP

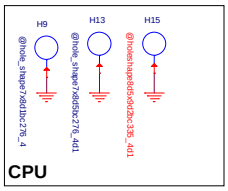


PCB HOLE



THERMAL HOLE





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Title	DC IN/TPM/D-Resis/HOLE	
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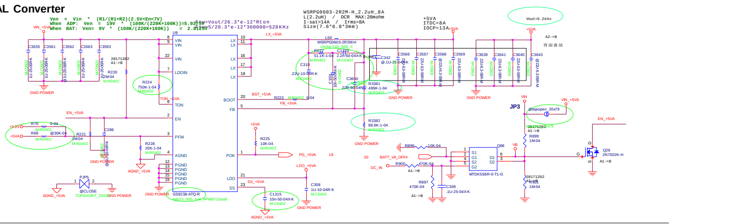
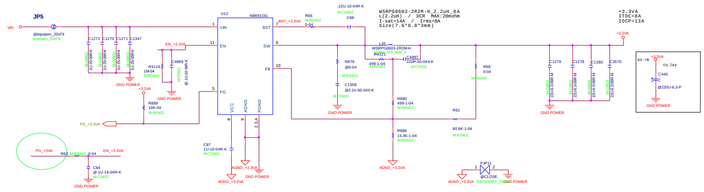
5VAL Converter



3VAL Converter



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Title: +5VA/+3.3VA		
Size: D	Document Number: GK5CN6X	Rev: VA
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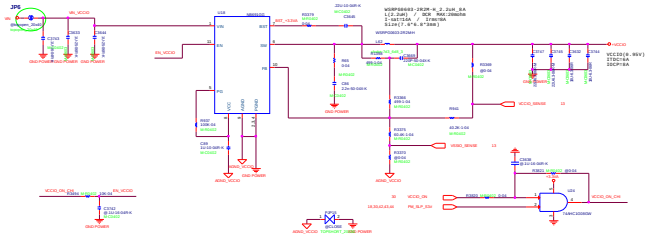
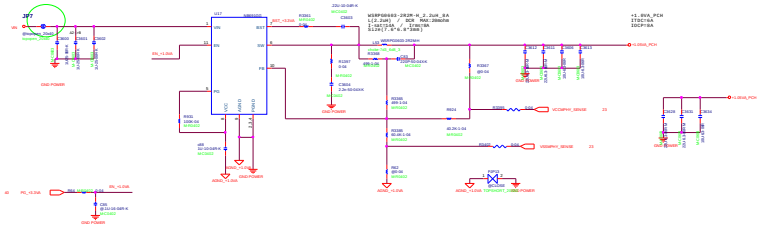
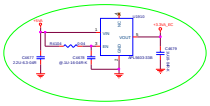
VCCIO Converter



1.05VA Converter



Delete 1V8_VA



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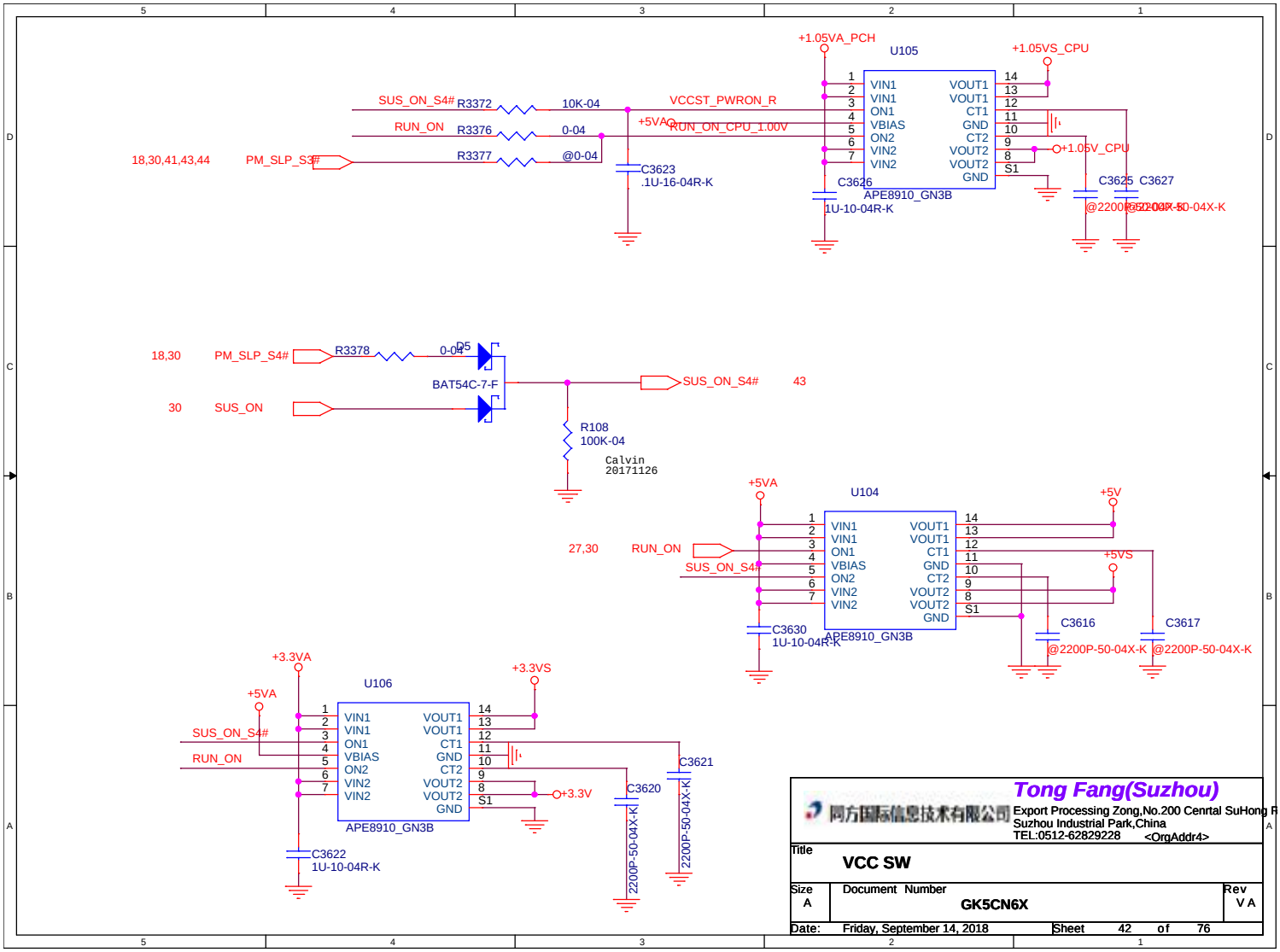
+1.05VA_PCH/VCCIO/+1.8VA

GIGCHIK



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Title	VCC SW	
Size A	Document Number GK5CN6X	Rev V A
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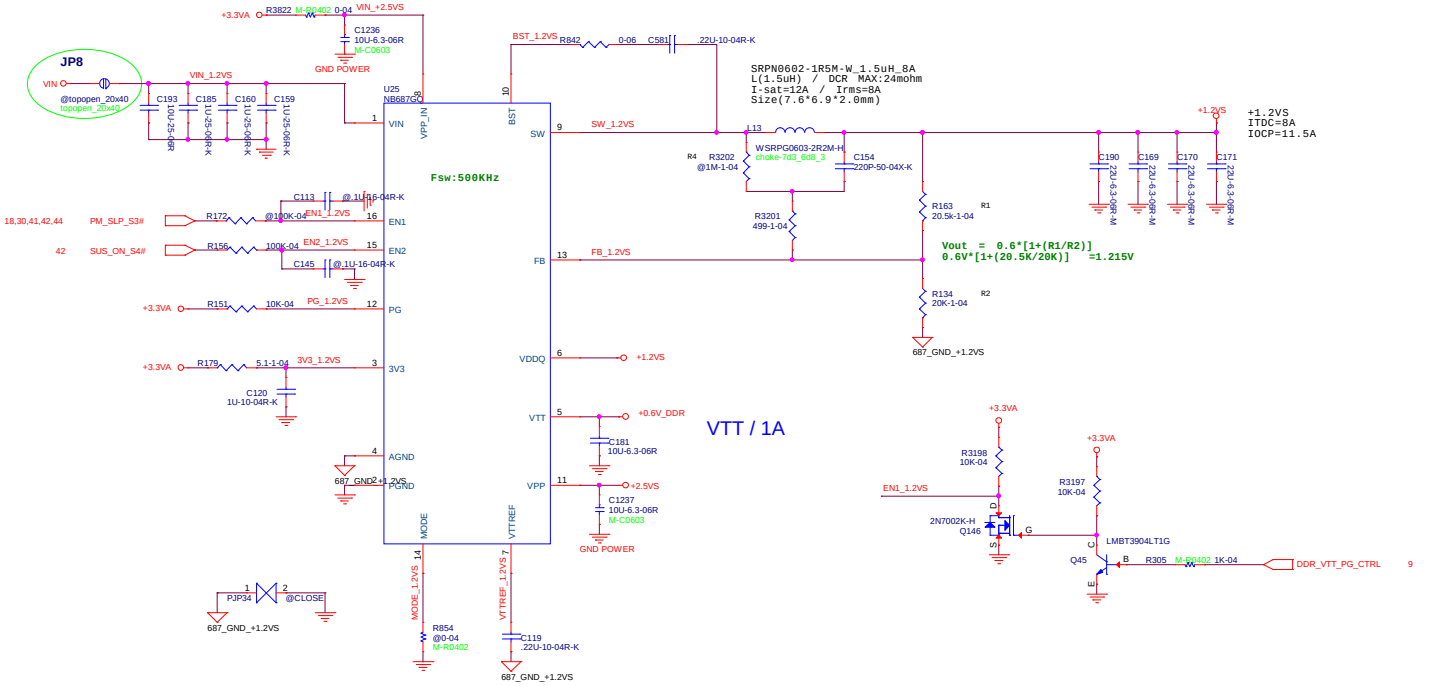
1.2VS/VTT/2.5VS



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Title: +1.2VS/+2.5VS

Size	Document Number	Rev
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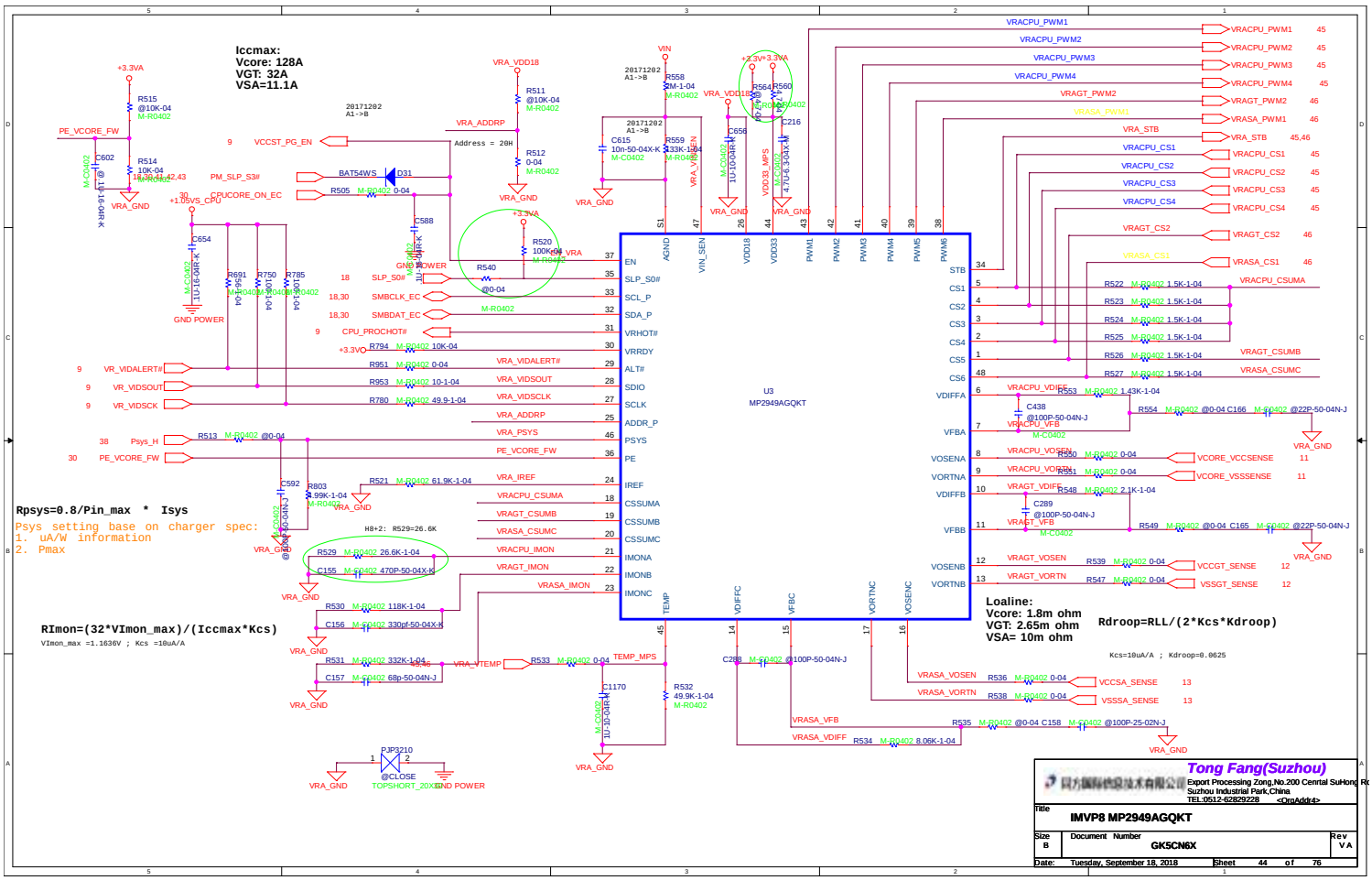
Iccmax:
Vcore: 128A
VGT: 32A
VSA=11.1A
U3
MP2949AGQKT
Rpsys=0.8/Pin_max * Isys
Psys setting base on charger spec:
1. uA/W information
2. Pmax
RImon=(32*VImon_max)/(Iccmax*Kcs)
VImon_max =1.1636V ; Kcs =10uA/A
Loaline:
Vcore: 1.8m ohm
VGT: 2.65m ohm
VSA= 10m ohm
Rdroop=RLL/(2*Kcs*Kdroop)
Kcs=10uA/A ; Kdroop=0.0625
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TEL:0512-62829228
Title
IMVP8 MP2949AGQKT
Size B
Document Number
GK5CN6X
Rev VA
Date: Tuesday, September 18, 2018
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VCCCORE

VCORE:0.55~1.52V Vboot:0V
Core: Iccmax=128A(H62)/140A(H82)
Core: (TDC)IPL2=60A(4+2)/80A(6+2)/86A(8+2)
FSW:600KHz
di(IccMax transient)/dt:91A@65ns for H62

Overshoot: 200mV@30ns
IMVP8 Domain Address HEX:00h
LL:1.8m ohm
Slew Rate=200mV/us & 90mV/us
PL2/PL4=90W/130W(H62)
PL2/PL4=107W/163W(H82)

High side
Rds(on) TYP:10.5mohm

Low side
Rds(on) TYP:3.7mohm

MP86910B
ITDC:20A
ICCMAX:35A

WSRPG0603A-R22M-AG
(L1*W2*H3mm)
Size(7.6*6.8*3mm)

FOR EMI solution

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Title: VCORE
Size: B
Document Number: GK5CN6X
Rev: V A
Date: Friday, September 14, 2018
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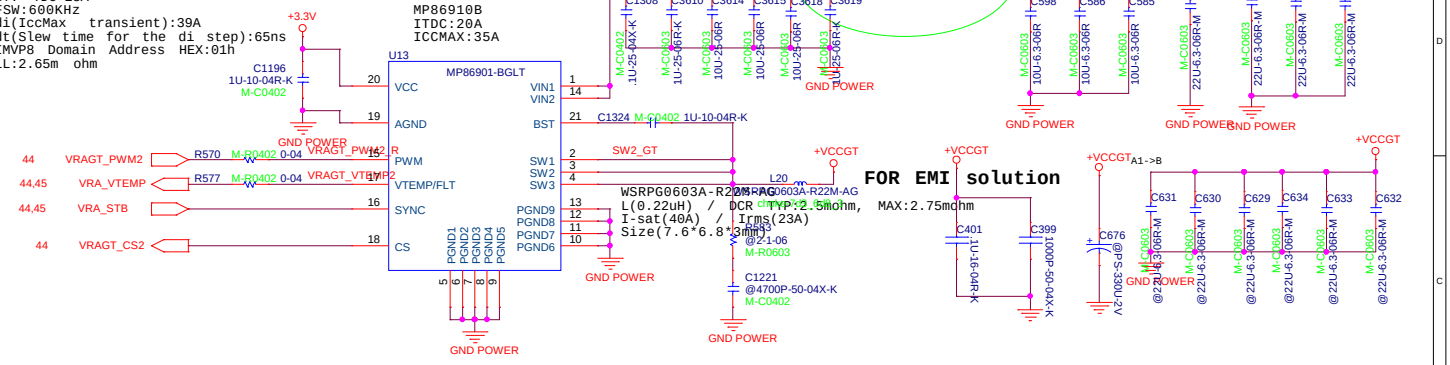
VCCGT

VGT:0.55V~1.52V Vboot:0V
GT: Iccmax=55A
GT: TDC=25A
FSW:600KHz
di(IccMax transient):39A
dt(Slew time for the di step):65ns
IMVP8 Domain Address HEX:01h
LL:2.65m ohm

High side
Rds(on) TYP:10.5mohm

Low side
Rds(on) TYP:3.7mohm

MP86910B
ITDC:20A
ICCMAX:35A



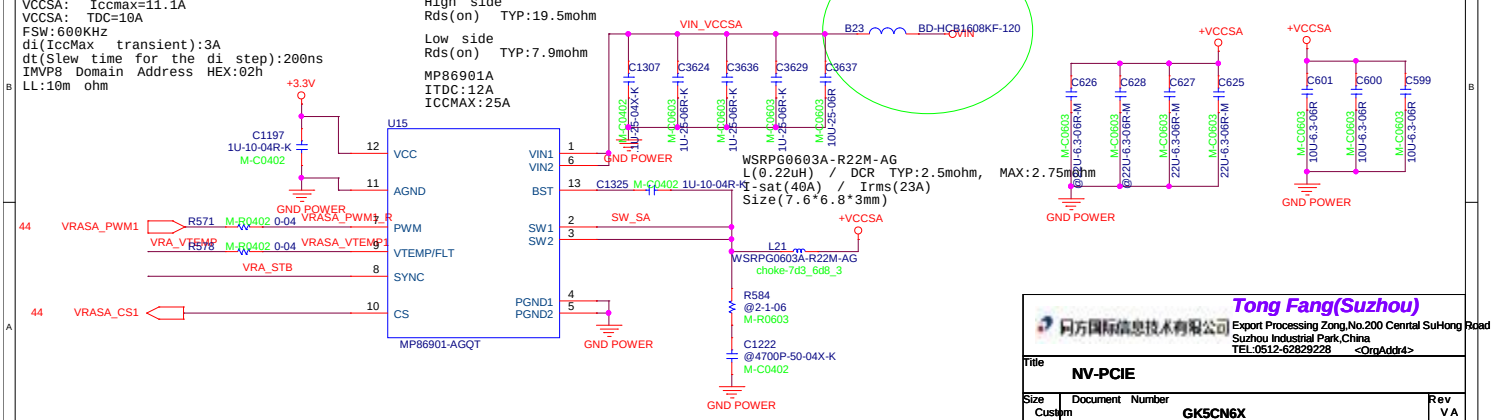
VCCSA

VCCSA:0.55~1.52V Vboot:1.05V
VCCSA: Iccmax=11.1A
VCCSA: TDC=10A
FSW:600KHz
di(IccMax transient):3A
dt(Slew time for the di step):200ns
IMVP8 Domain Address HEX:02h
LL:10m ohm

High side
Rds(on) TYP:19.5mohm

Low side
Rds(on) TYP:7.9mohm

MP86901A
ITDC:12A
ICCMAX:25A



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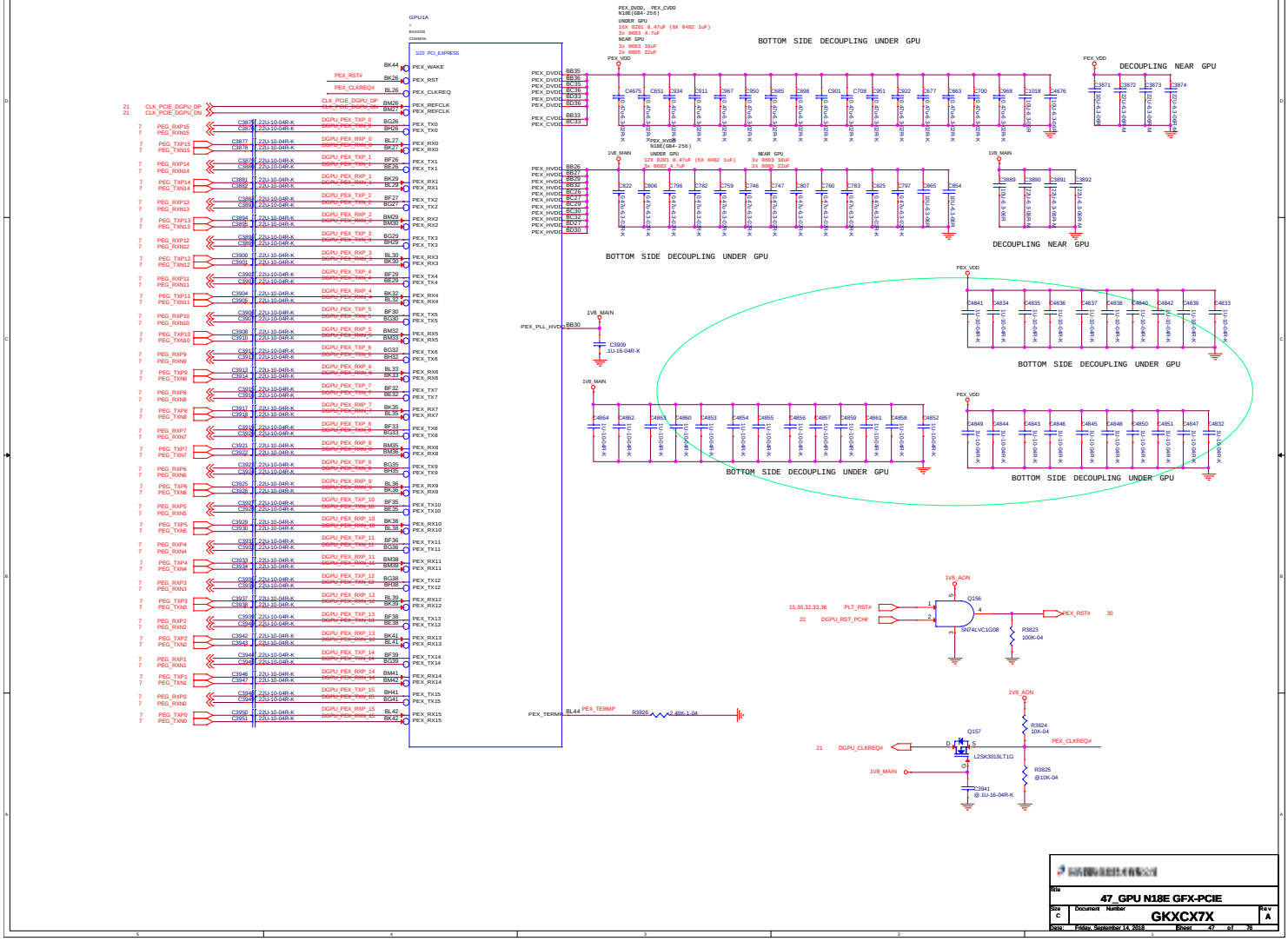
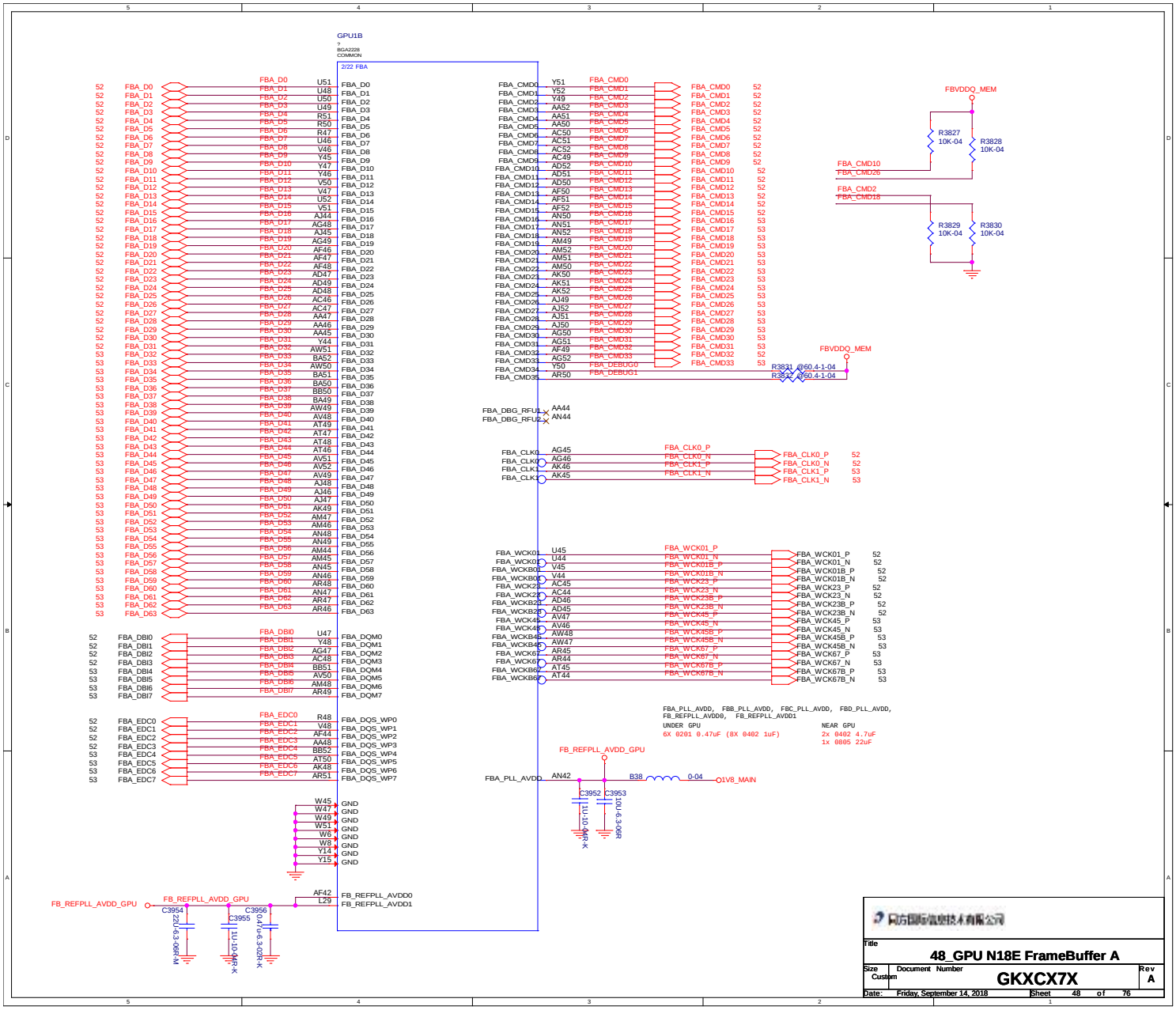
Title	NV-PCIE		
Size: Custom	Document Number: GK5CN6X		Rev: V A
Date: Friday, September 14, 2018	Sheet 46 of 76		



Title	47_GPU N18E GFX-PCIE		
Size C	Document Number GKXCX7X		Rev A
Date: Friday, September 14, 2018	Sheet 47 of 79		



Title	48_GPU N18E FrameBuffer A
Size / Document Number	Custom / GKXCX7X
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Date:	Friday, September 14, 2018
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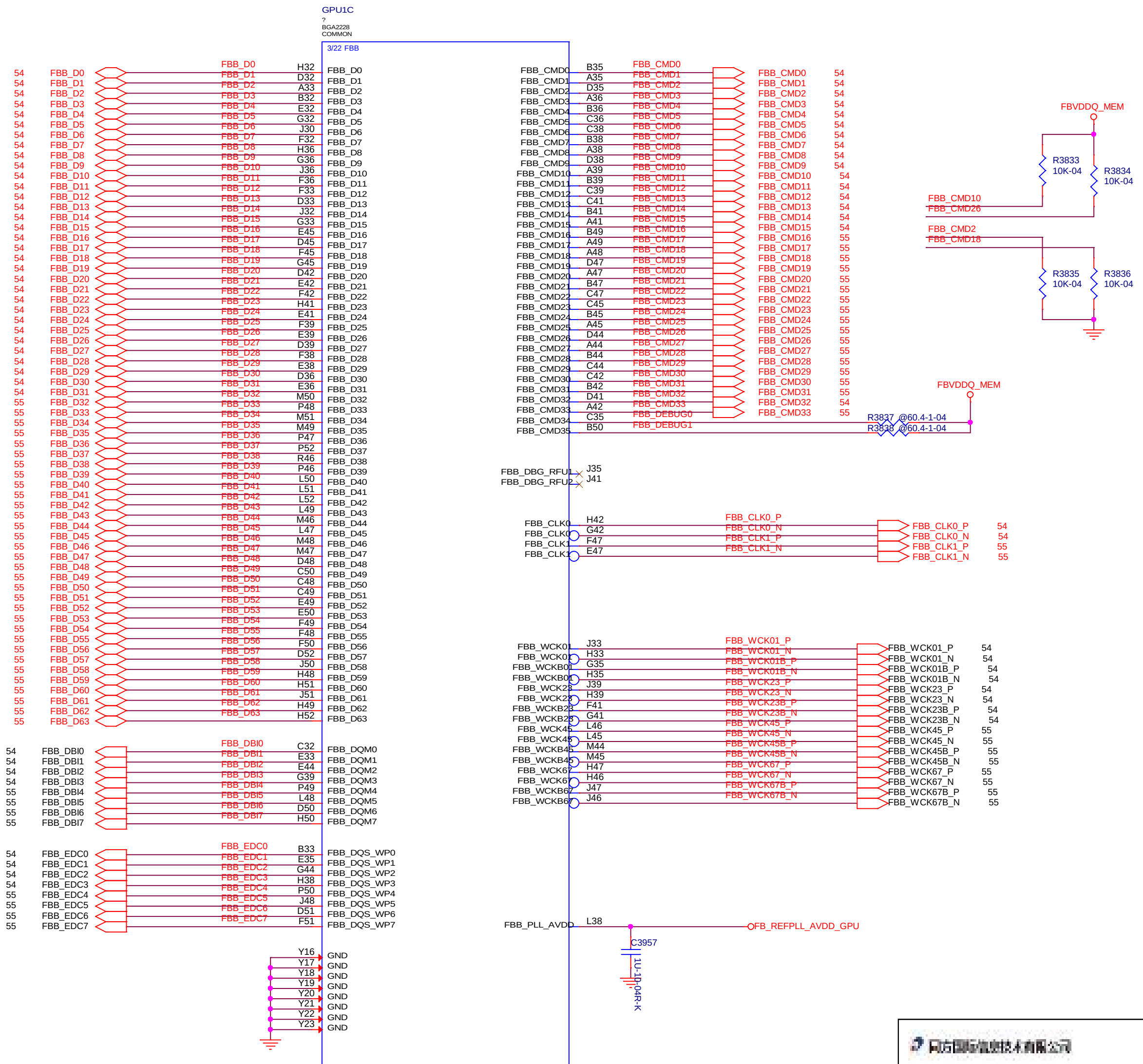

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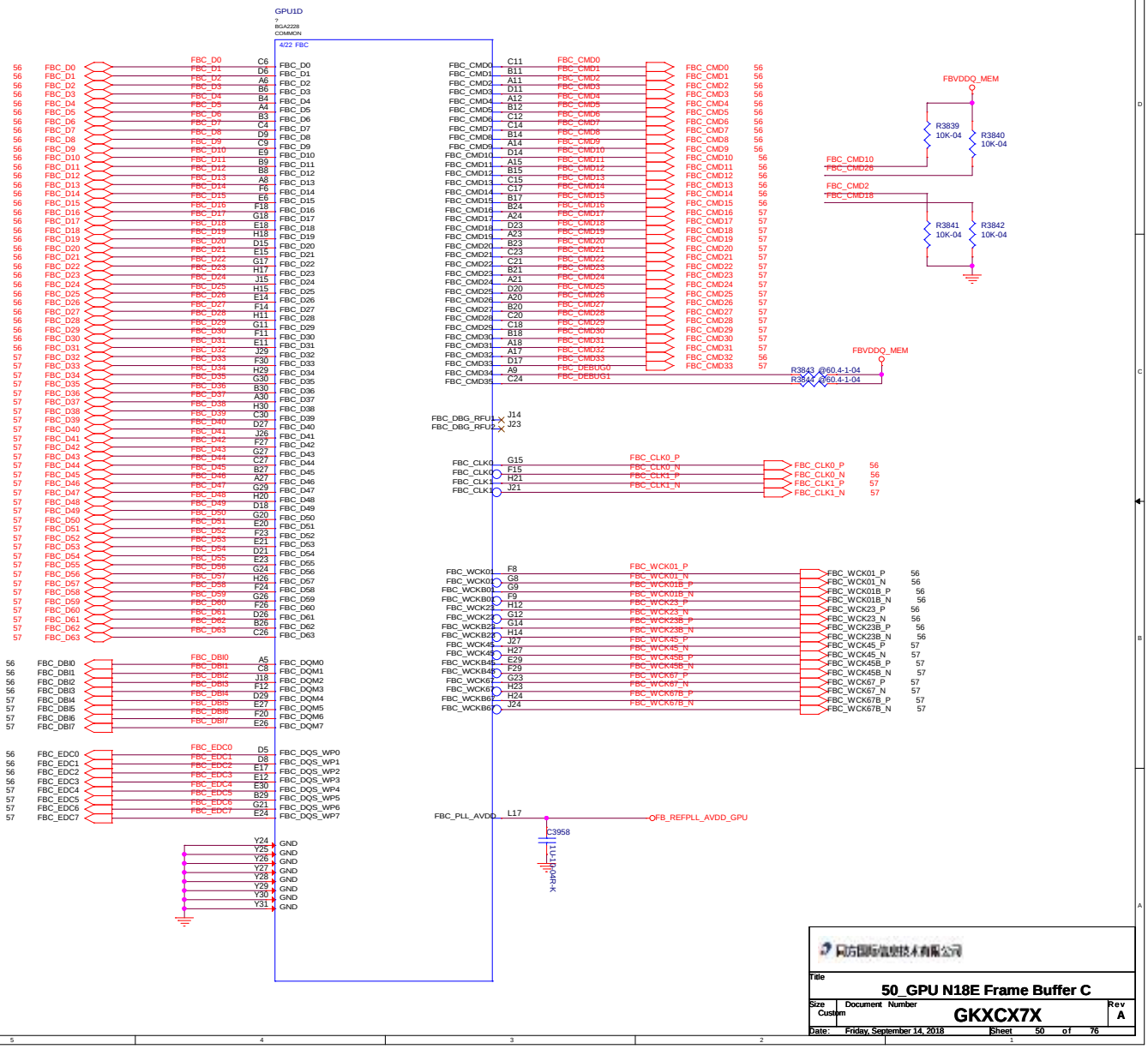
Title

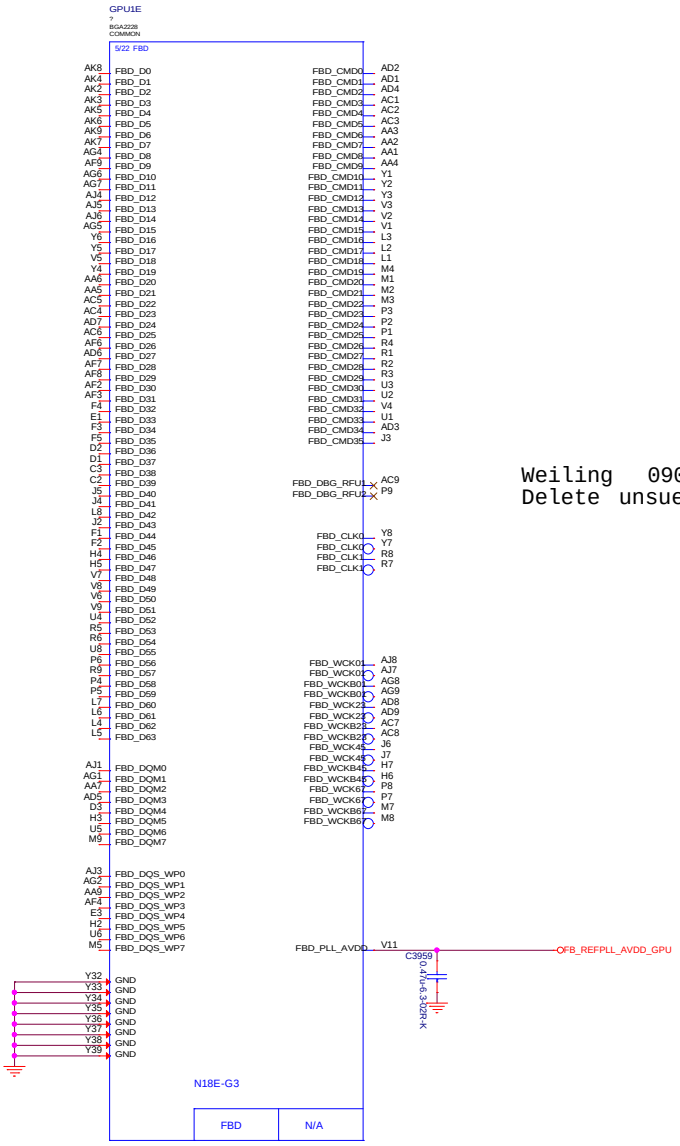
49_GPU N18E Frame Buffer B

Size	Document Number	Rev
Custom	GKXCX7X	A

Date: Friday, September 14, 2018 | Sheet 49 of 76



Title	50_GPU N18E Frame Buffer C
Size: Custom	Document Number: GKXCX7X
Rev	A
Date:	Friday, September 14, 2018
Sheet	50 of 76



Weiling 0904
Delete unsued FBD partition

Title	51_GPU N18E Frame Buffer D	
Size: Custom	Document Number: GKXCX7X	Rev: A
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MEM_FBA[31_0]

GDDR6: Maximum allowable case temp =95 degree

VRAM1A

VRAM1B

VRAM1C

VRAM1D

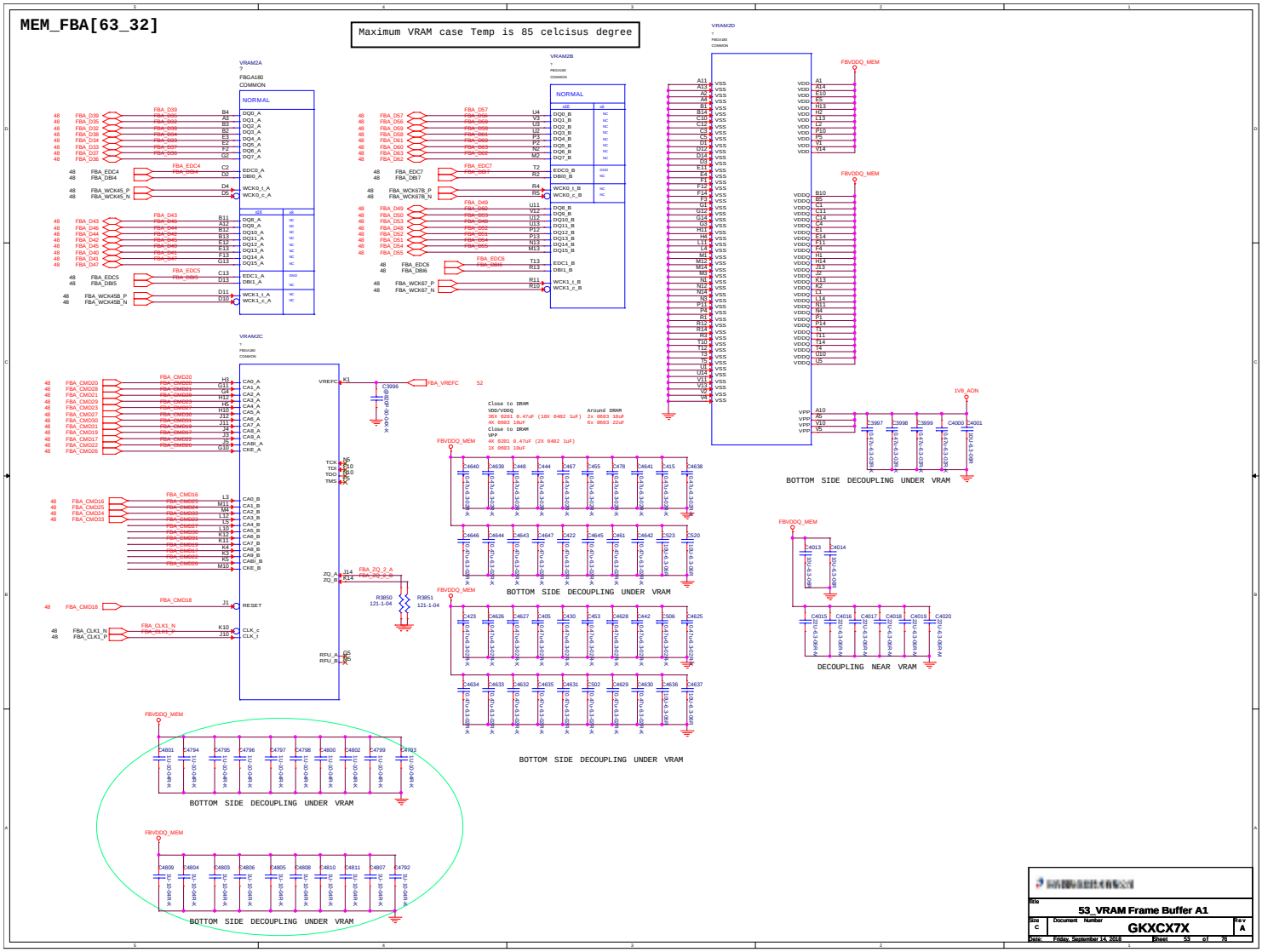
BOTTOM SIDE DECOUPLING UNDER VRAM

DECOUPLING NEAR VRAM

Title	52_VRAM Frame Buffer A0		
Size C	Document Number GKXCX7X		Rev A
Date: Friday, September 14, 2018	Sheet 52 of 79		

MEM_FBA[63_32]

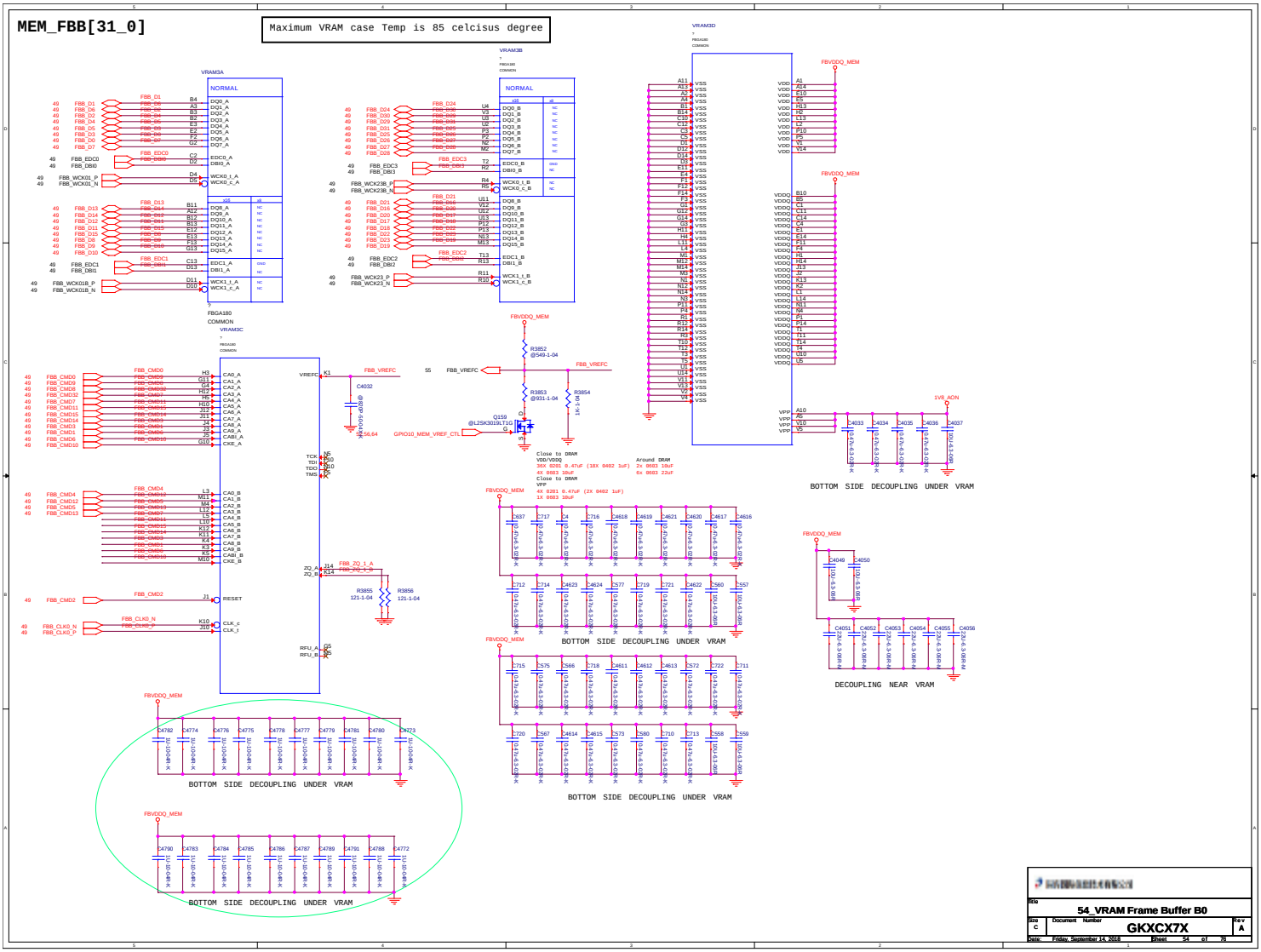
Maximum VRAM case Temp is 85 celcisus degree



Title	53_VRAM Frame Buffer A1		
Size C	Document Number GKXCX7X		Rev A
Date: Friday, September 14, 2018	Sheet 53 of 78		

MEM_FBB[31_0]

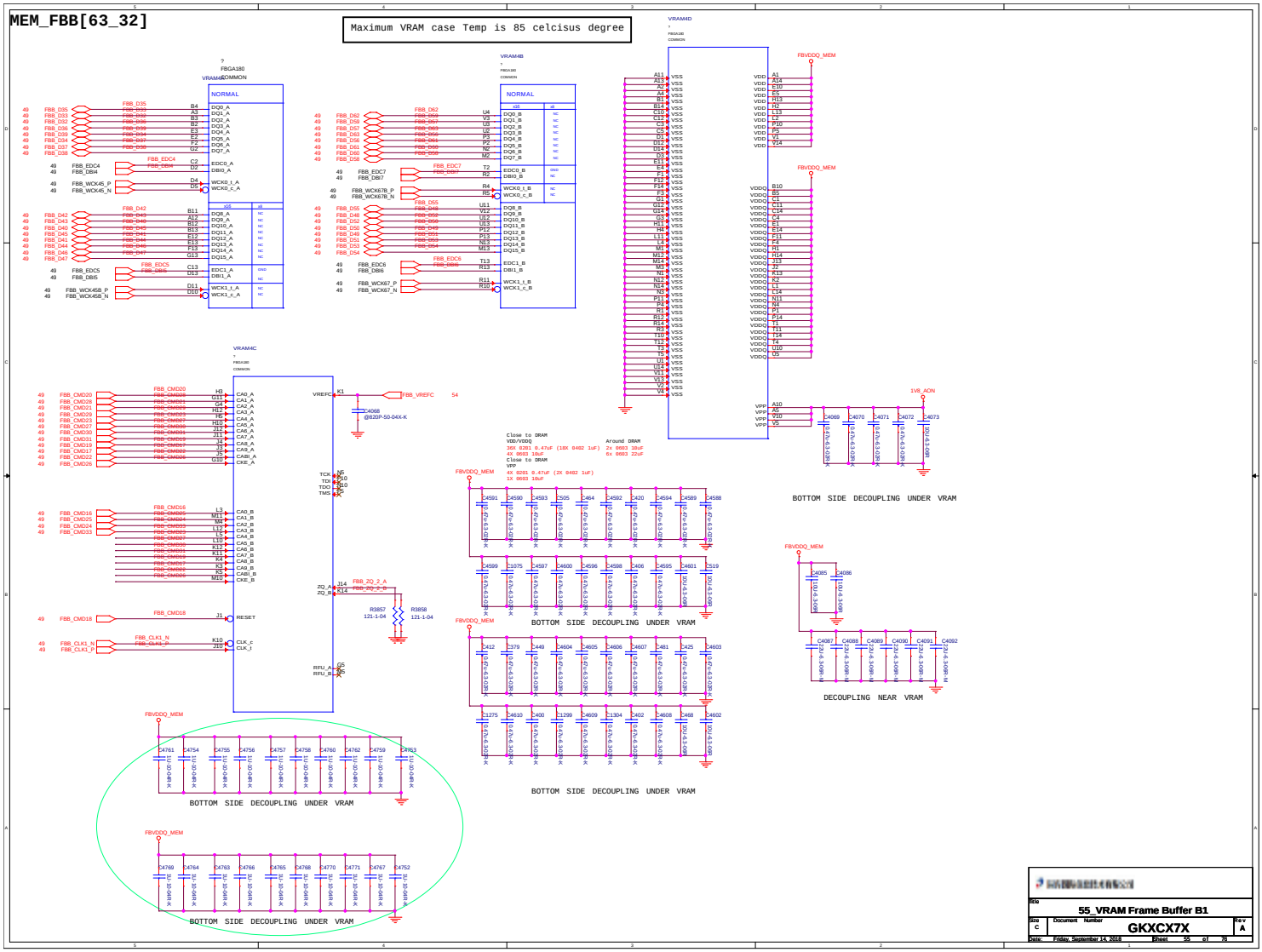
Maximum VRAM case Temp is 85 celcisus degree



Title	54_VRAM Frame Buffer B0		
Size C	Document Number GKXCX7X		Rev A
Date: Friday, September 14, 2018	Sheet 54 of 78		

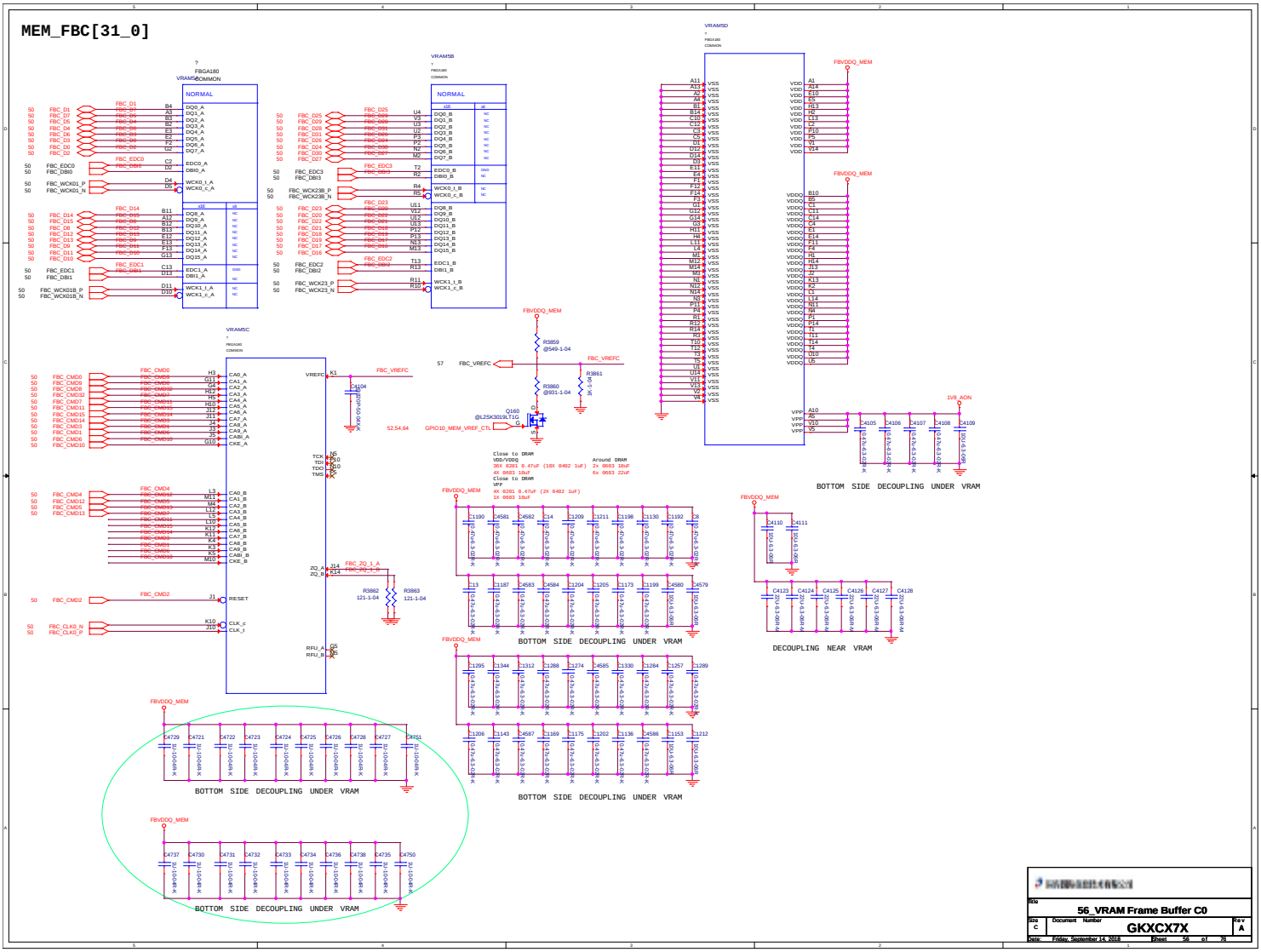
MEM_FBB[63_32]

Maximum VRAM case Temp is 85 celcisus degree



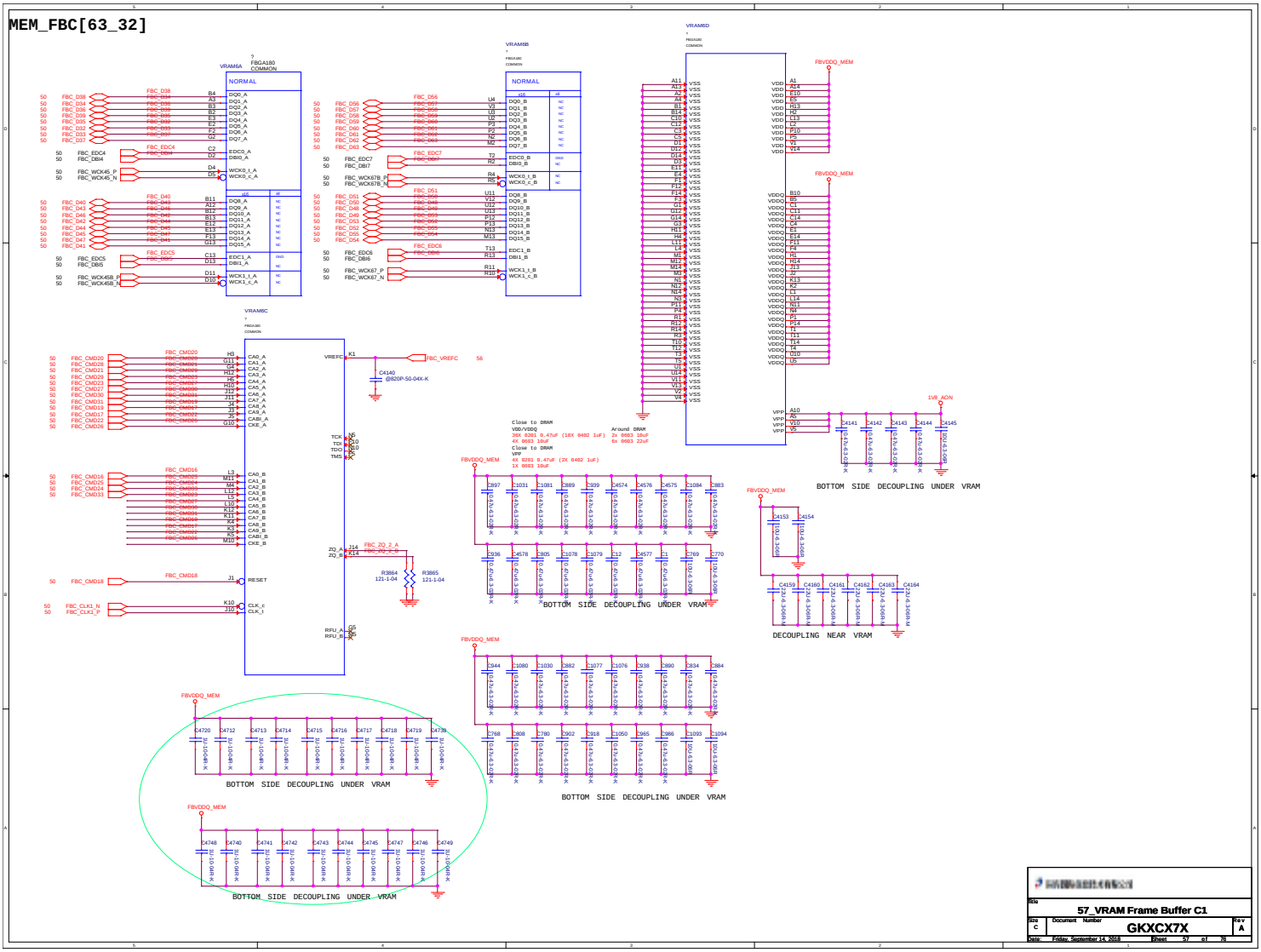
Title	55_VRAM Frame Buffer B1		
Size C	Document Number GKXCX7X		Rev A
Date: Friday, September 14, 2018	Sheet 55 of 78		

MEM_FBC[31_0]



Title	56_VRAM Frame Buffer C0		
Size	Document Number		Rev
C	GKXCX7X		A
Date:	Friday, September 14, 2018	Sheet	56 of 79

MEM_FBC[63_32]



Title	57_VRAM Frame Buffer C1		
Size C	Document Number GKXCX7X		Rev A
Date: Friday, September 14, 2018	Sheet 57 of 78		

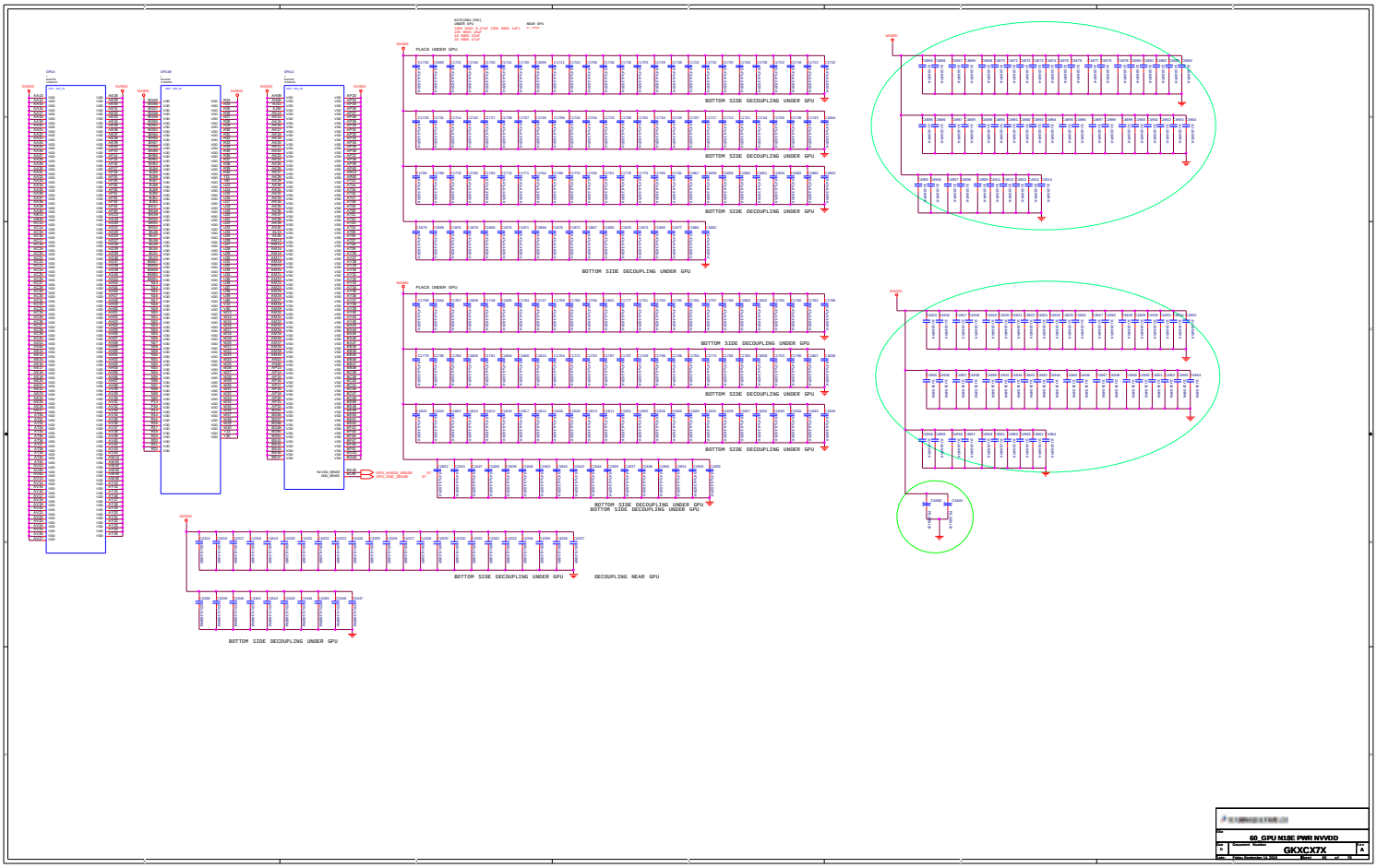
MEM_FBD[31_0]

Weiling 0904
Delete VRAM due to G1
 only supporting 192bits

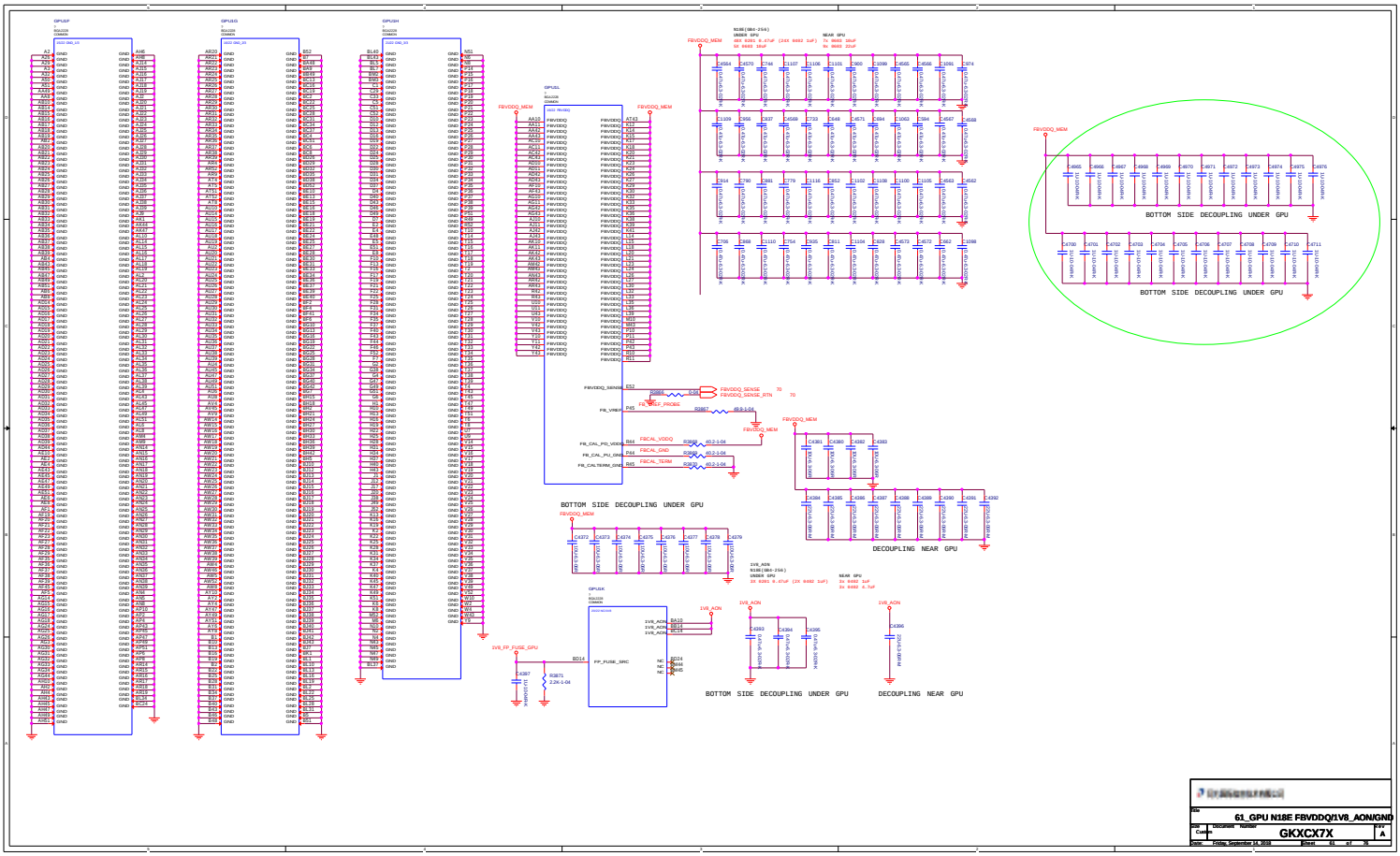
[redacted]			
Title	58_VRAM Frame Buffer D0		
Size: Custom	Document Number: GKXCX7X		Rev: A
Date: Friday, September 14, 2018	Sheet 58 of 76		

MEM_FBC[63_32]

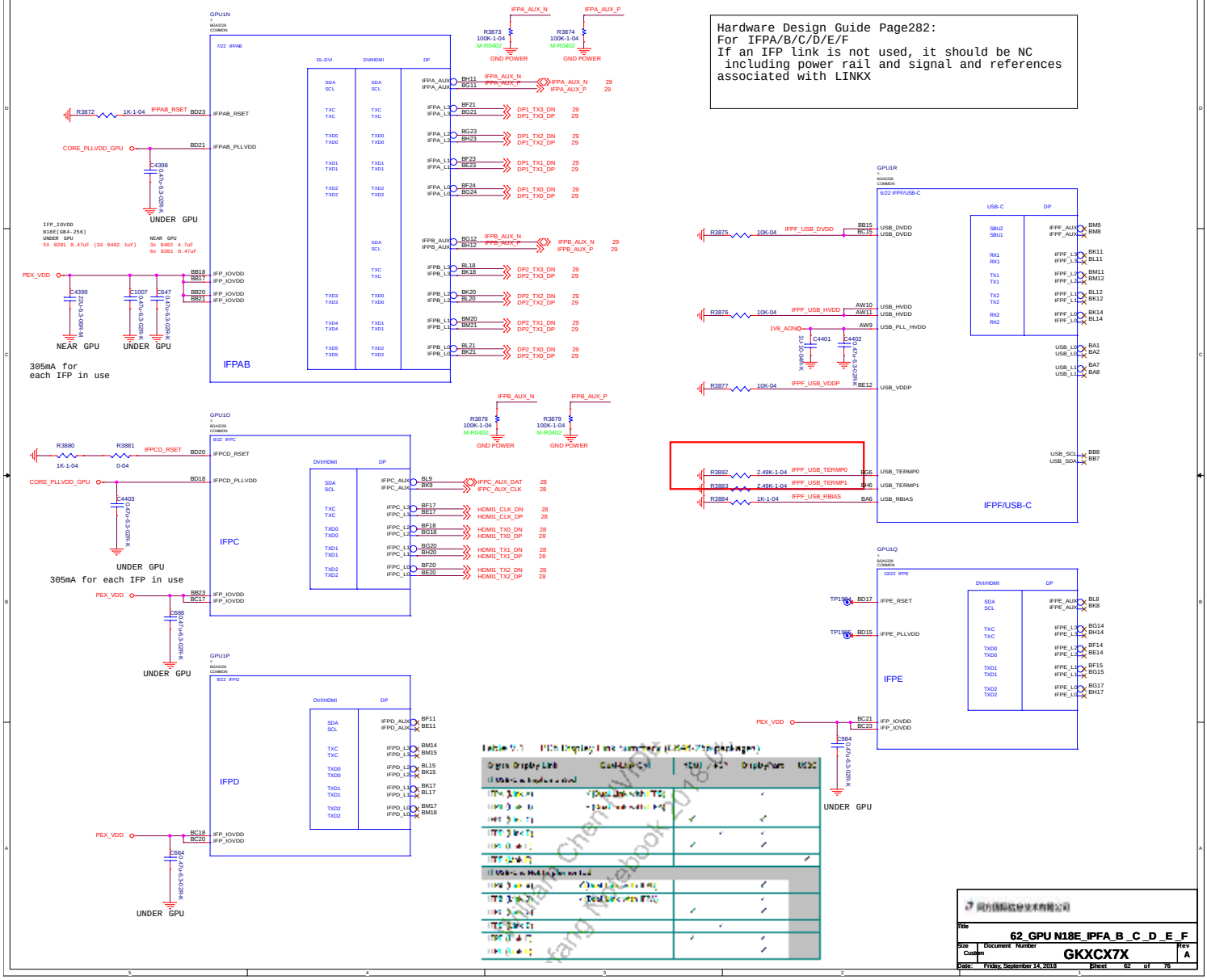
Weiling 0904
Delete VRAM due to G1
 only supporting 192bits

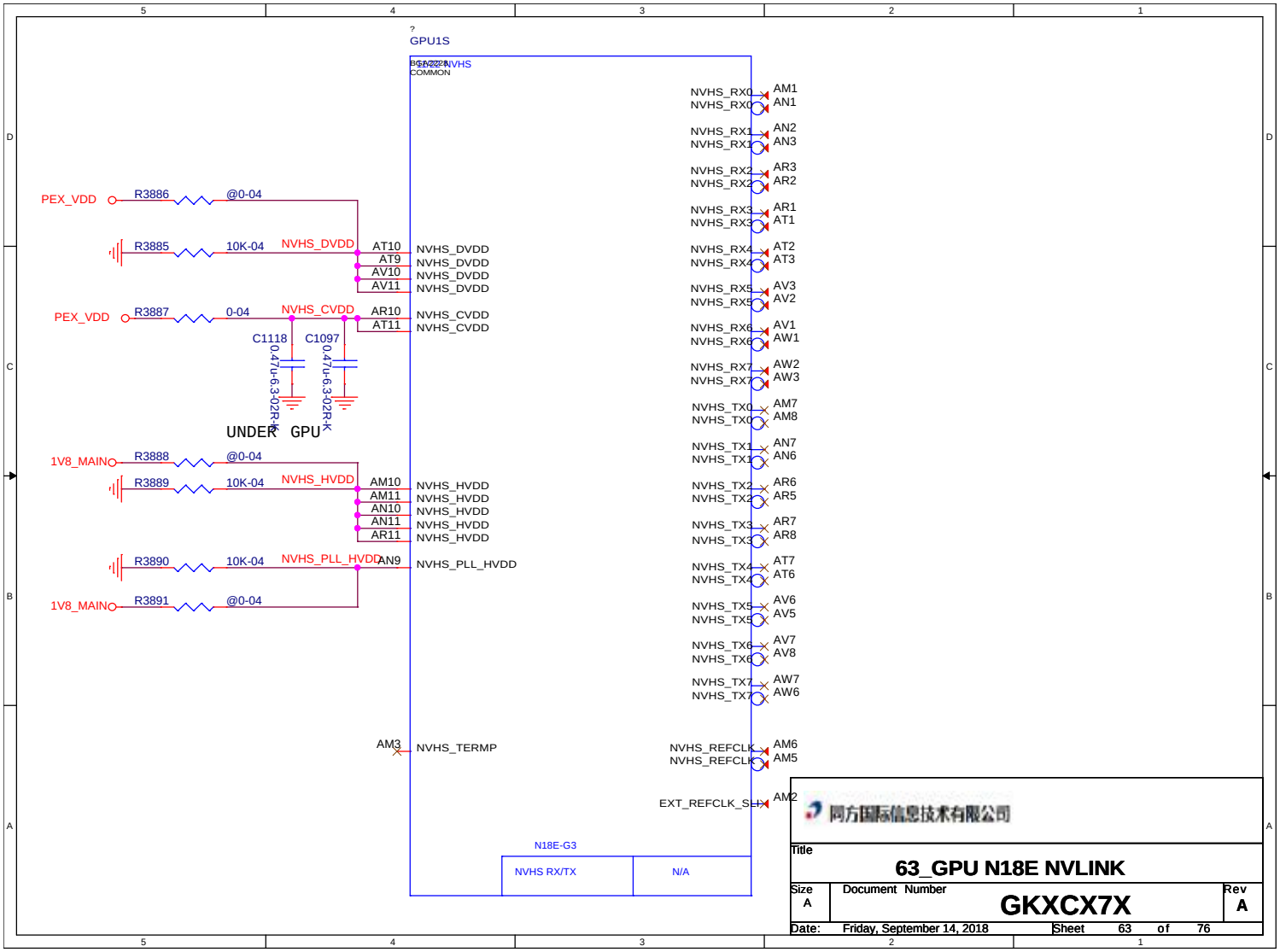


	60_GPU N18E PWR NVVDD		
Size: D	Document Number: GKXCX7X		Rev: A
Date: Friday, December 14, 2012	Sheet: 38 of 76		



Title	61_GPU N18E FBVDDQ/1V8_AON/GND		
Size	Document Number		Rev
C	GKXCX7X		A
Date: Friday, September 14, 2018	Sheet 63 of 76		


Hardware Design Guide Page282:
For IFPA/B/C/D/E/F
If an IFP link is not used, it should be NC
including power rail and signal and references
associated with LINKX
IFPAB
IFPC
IFPD
IFPE
IFPF/USB-C
305mA for
each IFP in use
305mA for each IFP in use
UNDER GPU
NEAR GPU
GND POWER
62_GPU N18E_IFPA_B_C_D_E_F
GKXCX7X
Date: Friday, September 14, 2018
Sheet 62 of 76


GPU1S
NVHS
COMMON
PEX_VDD
R3886
@0-04
R3885
10K-04
NVHS_DVDD
AT10
AT9
AV10
AV11
NVHS_DVDD
PEX_VDD
R3887
0-04
NVHS_CVDD
AR10
AT11
NVHS_CVDD
C1118
C1097
0.47u-6.3-02R-K
UNDER GPU
1V8_MAIN
R3888
@0-04
R3889
10K-04
NVHS_HVDD
AM10
AM11
AN10
AN11
AR11
NVHS_HVDD
R3890
10K-04
NVHS_PLL_HVDD
AN9
NVHS_PLL_HVDD
1V8_MAIN
R3891
@0-04
AM3
NVHS_TERMP
NVHS_RX0
NVHS_RX0
AM1
AN1
NVHS_RX1
NVHS_RX1
AN2
AN3
NVHS_RX2
NVHS_RX2
AR3
AR2
NVHS_RX3
NVHS_RX3
AR1
AT1
NVHS_RX4
NVHS_RX4
AT2
AT3
NVHS_RX5
NVHS_RX5
AV3
AV2
NVHS_RX6
NVHS_RX6
AV1
AW1
NVHS_RX7
NVHS_RX7
AW2
AW3
NVHS_TX0
NVHS_TX0
AM7
AM8
NVHS_TX1
NVHS_TX1
AN7
AN6
NVHS_TX2
NVHS_TX2
AR6
AR5
NVHS_TX3
NVHS_TX3
AR7
AR8
NVHS_TX4
NVHS_TX4
AT7
AT6
NVHS_TX5
NVHS_TX5
AV6
AV5
NVHS_TX6
NVHS_TX6
AV7
AV8
NVHS_TX7
NVHS_TX7
AW7
AW6
NVHS_REFCLK
NVHS_REFCLK
AM6
AM5
EXT_REFCLK_SLI
AM2
N18E-G3
NVHS RX/TX
N/A
同方国际信息技术有限公司
Title
63_GPU N18E NVLINK
Size
A
Document Number
GKXCX7X
Rev
A
Date:
Friday, September 14, 2018
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63
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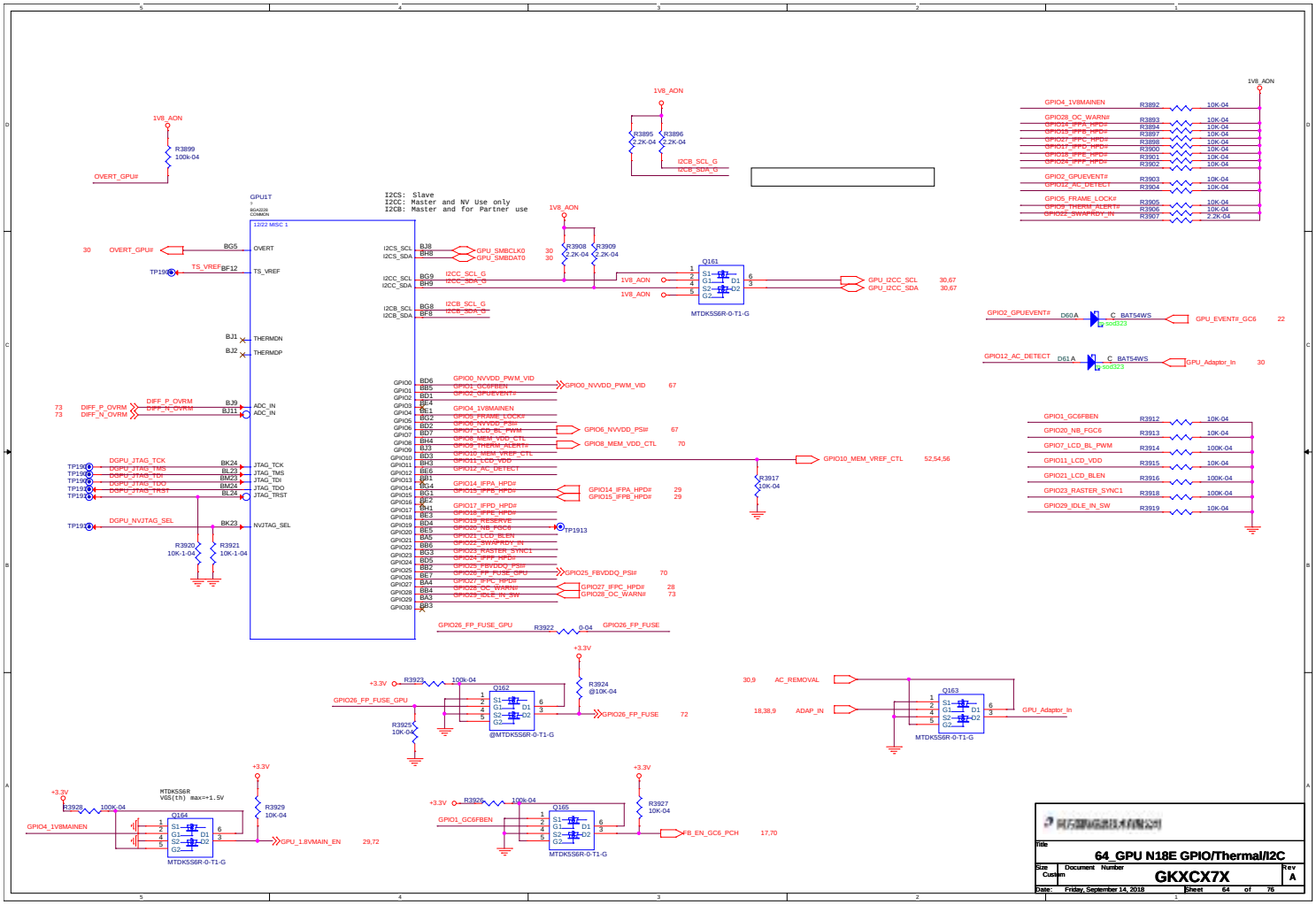
76


1V8_AON
R3899 100k-04
OVERT_GPU#
GPU1T
I2C5: Slave
I2CC: Master and NV Use only
I2CB: Master and for Partner use
OVERT_GPU#
TS_VREF
THERMDN
THERMDP
DIFF_P_OVRM
DIFF_N_OVRM
ADC_IN
DGPU_JTAG_TCK
DGPU_JTAG_TMS
DGPU_JTAG_TDI
DGPU_JTAG_TDO
DGPU_JTAG_TRST
DGPU_NVJTAG_SEL
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST
NVJTAG_SEL
R3920 10K-1-04
R3921 10K-1-04
I2C5_SCL
I2C5_SDA
I2CC_SCL
I2CC_SDA
I2CB_SCL
I2CB_SDA
GPU_SMBCLK0
GPU_SMBDAT0
I2CC_SCL_G
I2CC_SDA_G
I2CB_SCL_G
I2CB_SDA_G
R3908 2.2K-04
R3909 2.2K-04
Q161
MTDK5S6R-0-T1-G
GPU_I2CC_SCL
GPU_I2CC_SDA
R3895 2.2K-04
R3896 2.2K-04
I2CB_SCL_G
I2CB_SDA_G
GPIO0_NVVDD_PWM_VID
GPIO1_GC6FBEN
GPIO2_GPUEVENT#
GPIO4_1V8MAINEN
GPIO5_FRAME_LOCK#
GPIO6_NVVDD_PSI#
GPIO7_LCD_BL_PWM
GPIO8_MEM_VDD_CTL
GPIO9_THERM_ALERT#
GPIO10_MEM_VREF_CTL
GPIO11_LCD_VDD
GPIO12_AC_DETECT
GPIO14_IFPA_HPD#
GPIO15_IFPB_HPD#
GPIO17_IFPD_HPD#
GPIO18_IFPE_HPD#
GPIO19_RESERVE
GPIO20_NB_FGC6
GPIO21_LCD_BLEN
GPIO22_SWAPRDY_IN
GPIO23_RASTER_SYNC1
GPIO24_IFPF_HPD#
GPIO25_FBVDDQ_PSI#
GPIO26_FP_FUSE_GPU
GPIO27_IFPC_HPD#
GPIO28_OC_WARN#
GPIO29_IDLE_IN_SW
R3917 10K-04
TP1913
R3922 0-04
GPIO26_FP_FUSE
R3923 100k-04
R3924 @10K-04
R3925 10K-04
Q162
@MTDK5S6R-0-T1-G
GPIO26_FP_FUSE
AC_REMOVAL
ADAP_IN
Q163
MTDK5S6R-0-T1-G
GPU_Adaptor_In
R3928 100K-04
R3929 10K-04
Q164
MTDK5S6R-0-T1-G
GPU_1.8VMAIN_EN
R3926 100k-04
R3927 10K-04
Q165
MTDK5S6R-0-T1-G
FB_EN_GC6_PCH
GPIO4_1V8MAINEN R3892 10K-04
GPIO28_OC_WARN# R3893 10K-04
GPIO14_IFPA_HPD# R3894 10K-04
GPIO15_IFPB_HPD# R3897 10K-04
GPIO27_IFPC_HPD# R3898 10K-04
GPIO17_IFPD_HPD# R3900 10K-04
GPIO18_IFPE_HPD# R3901 10K-04
GPIO24_IFPF_HPD# R3902 10K-04
GPIO2_GPUEVENT# R3903 10K-04
GPIO12_AC_DETECT R3904 10K-04
GPIO5_FRAME_LOCK# R3905 10K-04
GPIO9_THERM_ALERT# R3906 10K-04
GPIO22_SWAPRDY_IN R3907 2.2K-04
GPIO2_GPUEVENT# D60A C_BAT54WS GPU_EVENT#_GC6
GPIO12_AC_DETECT D61A C_BAT54WS GPU_Adaptor_In
GPIO1_GC6FBEN R3912 10K-04
GPIO20_NB_FGC6 R3913 10K-04
GPIO7_LCD_BL_PWM R3914 100K-04
GPIO11_LCD_VDD R3915 10K-04
GPIO21_LCD_BLEN R3916 100K-04
GPIO23_RASTER_SYNC1 R3918 100K-04
GPIO29_IDLE_IN_SW R3919 10K-04
Title
64_GPU N18E GPIO/Thermal/I2C
Size Custom
Document Number
GKXCX7X
Rev A
Date: Friday, September 14, 2018
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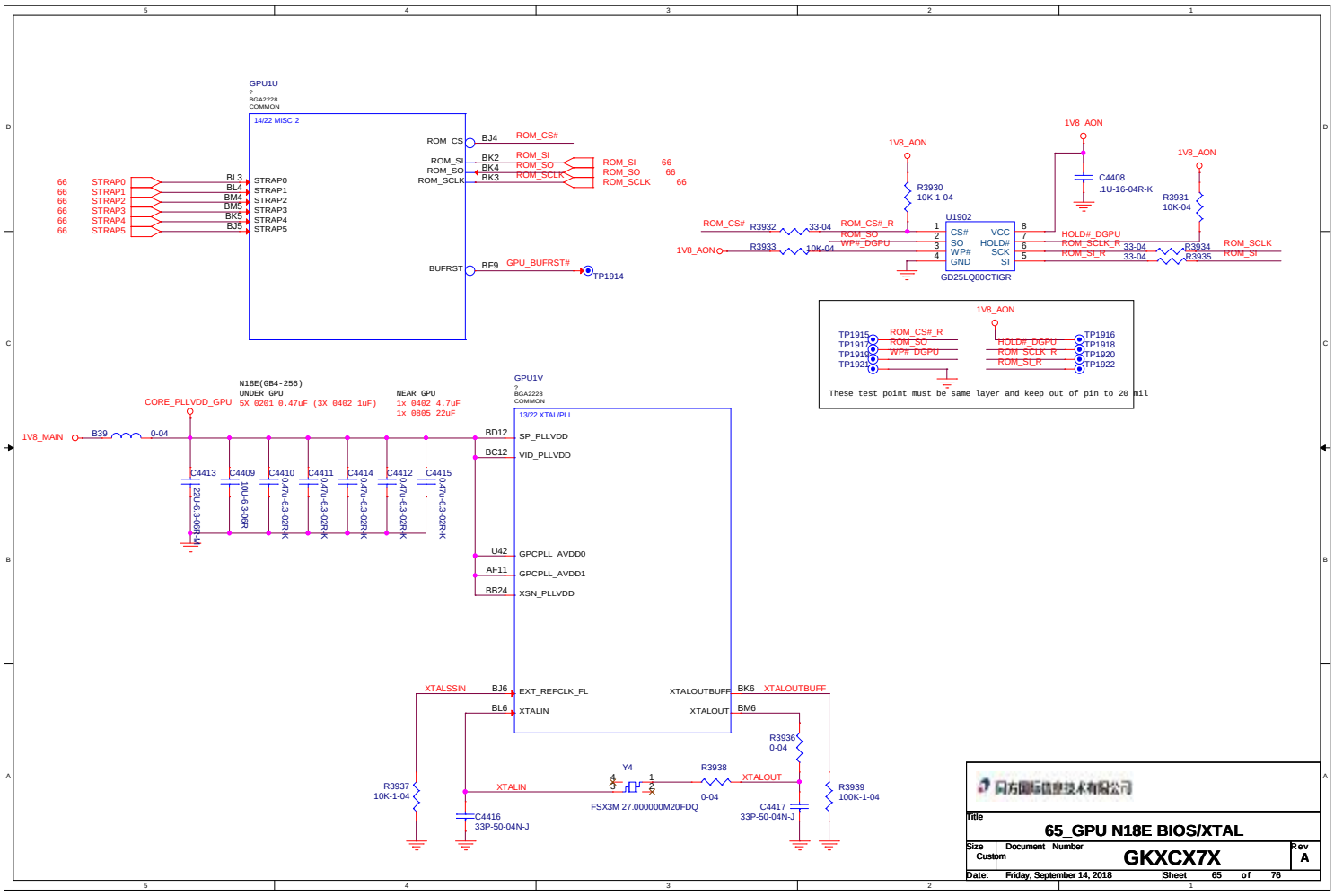

Title	65_GPU N18E BIOS/XTAL		
Size: Custom	Document Number: GKXCX7X		Rev: A
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	Voltage(V)		
LEVEL	Min	Normal	Max
H	1.5	1.8	1.854
M	0.5	0.9	1.3
L	0	0	0.3
Invalid	1.3V<pin voltage<1.5V		
	0.3V<pin voltage<0.5V		

Table 11-4 FS_OVERT Strap Enablement

Strap Pins Settings			FS_OVERT Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT Function ENABLED
L	L	H	FS_OVERT Function DISABLED (Reserved; do not configure)
all other configurations			Invalid; do not configure

Note that configurations other than those listed in Table 11-4 must be avoided as otherwise damage to strap inputs may result.

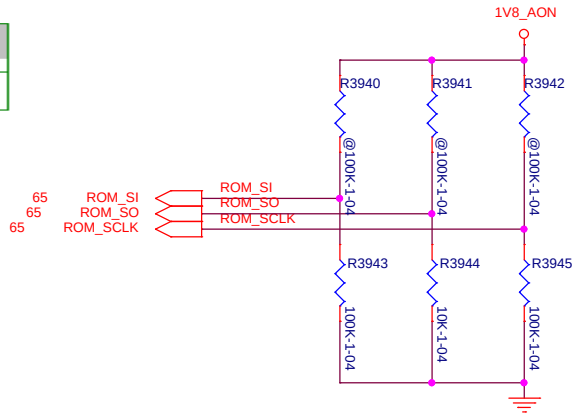
For N18x GPUs, the hardware-default FS_OVERT[1:0] strap is selected by ROM_SO, ROM_SI and ROM_SCLK straps. It no longer provided. The register-based method for configuring this value (to disable FS_OVERT) is the only method provided. This method is implemented in VBIOS settings.

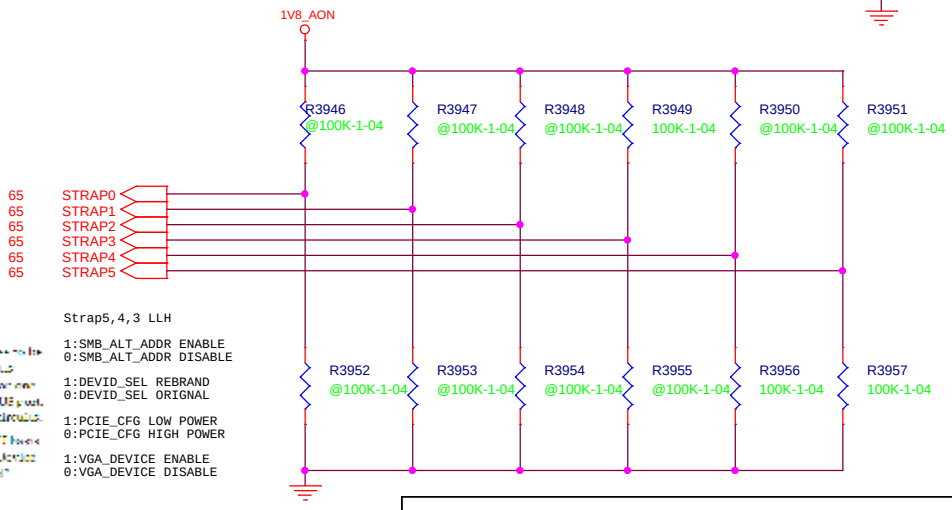
Based on RVL_07916_001_V10 JUNE 2017

GDDR5						
Density	Vendor	Part Number	Strap	Strap 2	Strap 1	Strap 0
8Gb	Samsung	K4Z80325BC-HC14 C-die	0X0	L	L	L
8Gb	Micron	MT61K256M32JE-14:A A-die	0X1	L	L	H
8Gb	Hynix	H56C8H24MJR-S4C M-die	0X2	L	H	L
4Gb	Samsung		0X7	H	H	H
4Gb	Hynix		0X6	H	H	L
4Gb	Micron					

POWER

1.25V/1.35V
1.25V/1.35V
1.25V/1.35V N18E-G2 only





Strap5,4,3 LLH

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

- SMB_ALT_ADDR Enable: The strap function allows an alternate SMBus address to be configured, so that graphics circuits with multiple GPUs can have separate SMBus connections for each GPU. In dual GPU configurations, use a "fixed" alternate address on one GPU (by setting this strap to "1") to avoid conflicts between the two GPUs on the SMBUS port. The "SMB_ALT_ADDR disabled" setting ("0") is correct for single GPU graphics circuits.
- DEVID_SEL: NVIDIA defines an original and a rebrand Device ID on a per-GPU basis. This device ID select strap function allows selection between the original PCIe Device ID (decimal for the GPU (see a function setting of "0"), and the alternate "rebranded" Device ID defined for the GPU (see a function setting of "1").
- PCIE_CFG: This function sets selected characteristics of PCIe buses, in particular signal amplitude (see §). A setting of "0" selects normal (full) signal swing. Mobile graphics circuits should use this setting (a setting of "1" uses reduced signal amplitude, available if special concerns require. Consult NVIDIA for guidance.)
- VGA_DEVICE: This strap function is used to report the graphics circuit (device) as a 3D device (class code 302, designated by a setting of "0" for this strap) or as a VGA device (class code 300, designated by a setting of "1" for this strap) to the host system. The 3D Device (class code 302, strap="0") setting is correct for most N8x-based notebook GeForce graphics circuits (consult NVIDIA for details on proper BIOS setting for MSHybrid solutions).

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Title	66_GPU N18E STRAP	
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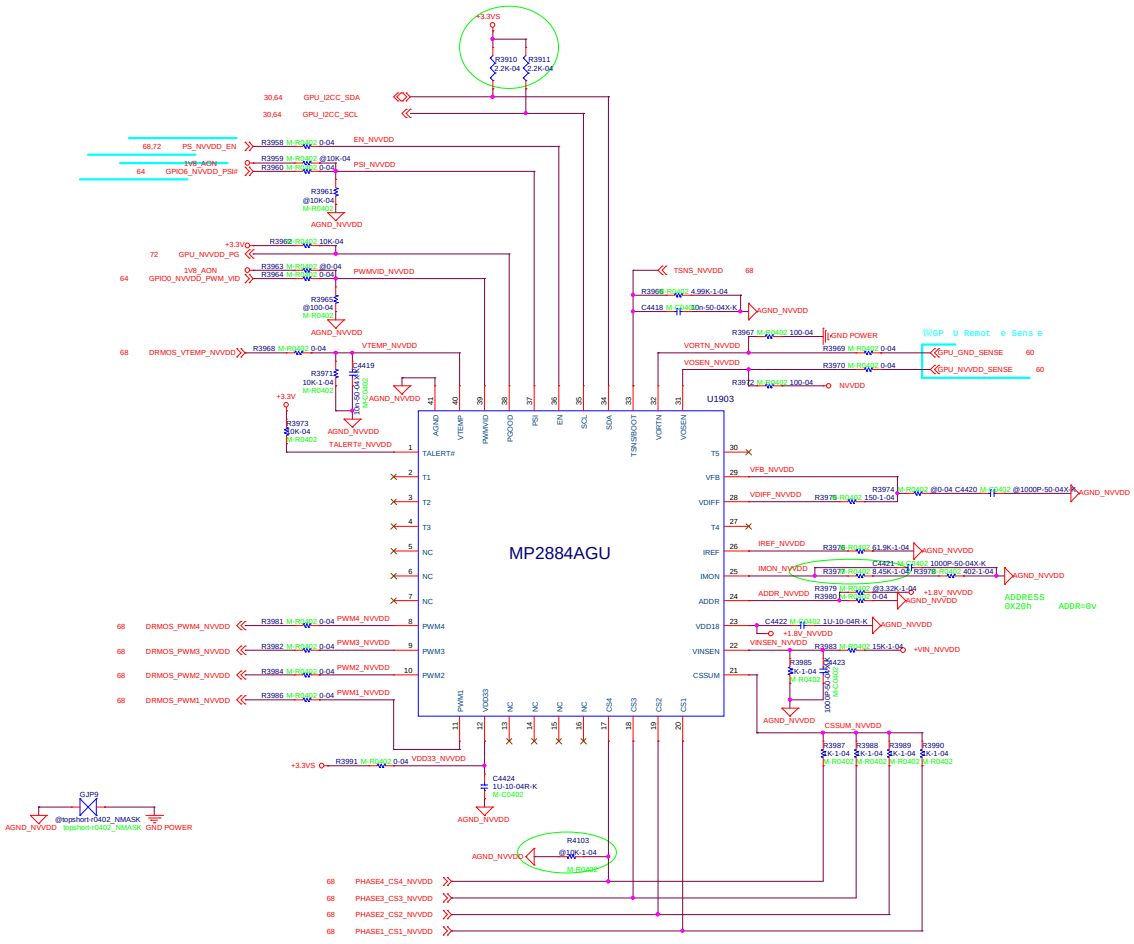

Title: 67_POWER N18E NVVDD CONTROLLER

Size: Custom | Document Number: GKXCX7X | Rev: A

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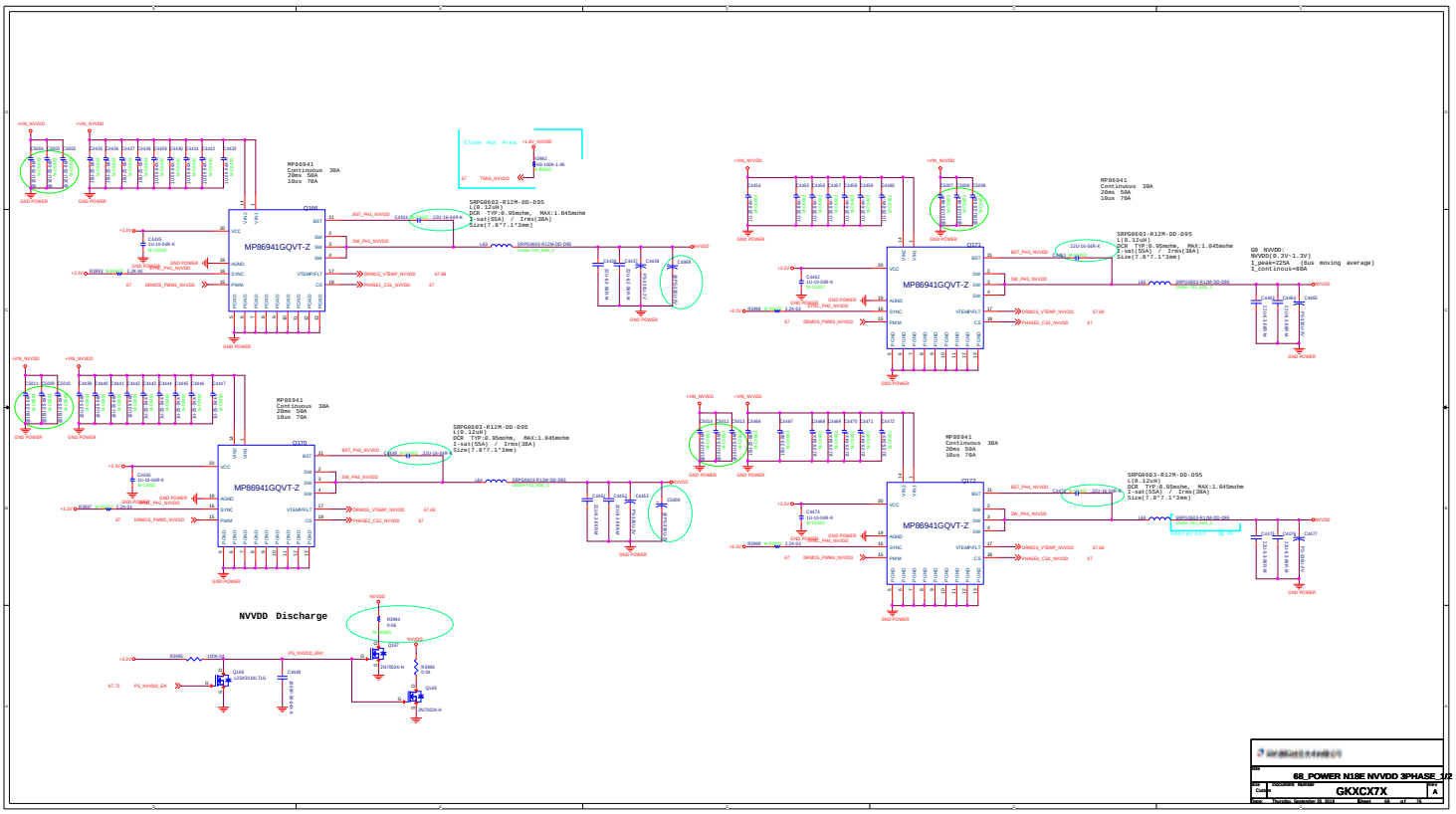
MP86941GQVT-Z
MP86941
Continuous 30A
20ms 50A
10us 70A
SRPG0603-R12M-DD-D9S
L(0.12uH)
DCR TYP:0.95mohm, MAX:1.045mohm
I-sat(55A) / Irms(38A)
Size(7.8*7.1*3mm)
NVVDD Discharge
GB_NVVDD:
NVVDD(0.3V~1.3V)
I_peak=225A (@us moving average)
I_continous=80A
68_POWER N18E NVVDD 3PHASE_1/2
GKXCX7X
Thursday, December 20, 2018

Del Q16, Q21

[redacted]			
Title	69_POWER N18E NVVDD 3PHASE_2/2		
Size: C	Document Number: GKXCX7X		Rev: A
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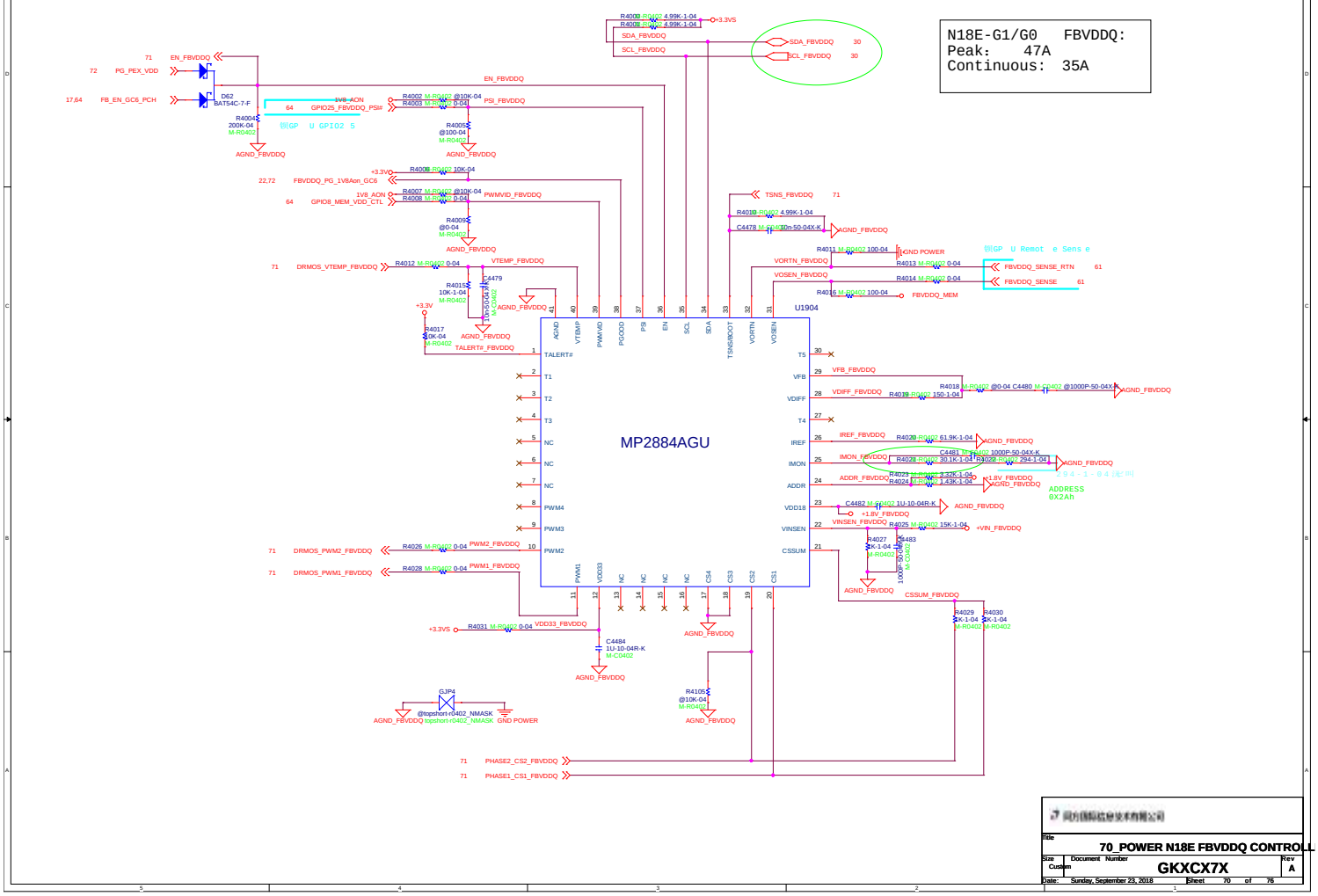
N18E-G1/G0 FBVDDQ:
Peak: 47A
Continuous: 35A
MP2884AGU
U1904
SDA_FBVDDQ
SCL_FBVDDQ
EN_FBVDDQ
PSI_FBVDDQ
PWMVID_FBVDDQ
VTEMP_FBVDDQ
TALERT#_FBVDDQ
PWM2_FBVDDQ
PWM1_FBVDDQ
VDD33_FBVDDQ
CSSUM_FBVDDQ
VFB_FBVDDQ
VDIFF_FBVDDQ
IREF_FBVDDQ
IMON_FBVDDQ
ADDR_FBVDDQ
VINSEN_FBVDDQ
PHASE2_CS2_FBVDDQ
PHASE1_CS1_FBVDDQ
AGND_FBVDDQ
+3.3VS
+1.8V_FBVDDQ
+VIN_FBVDDQ
TSNS_FBVDDQ
VORTN_FBVDDQ
VOSEN_FBVDDQ
FBVDDQ_SENSE_RTN
FBVDDQ_SENSE
FBVDDQ_MEM
ADDRESS 0X2Ah
70_POWER N18E FBVDDQ CONTROLL
GKXCX7X
Sunday, September 23, 2018
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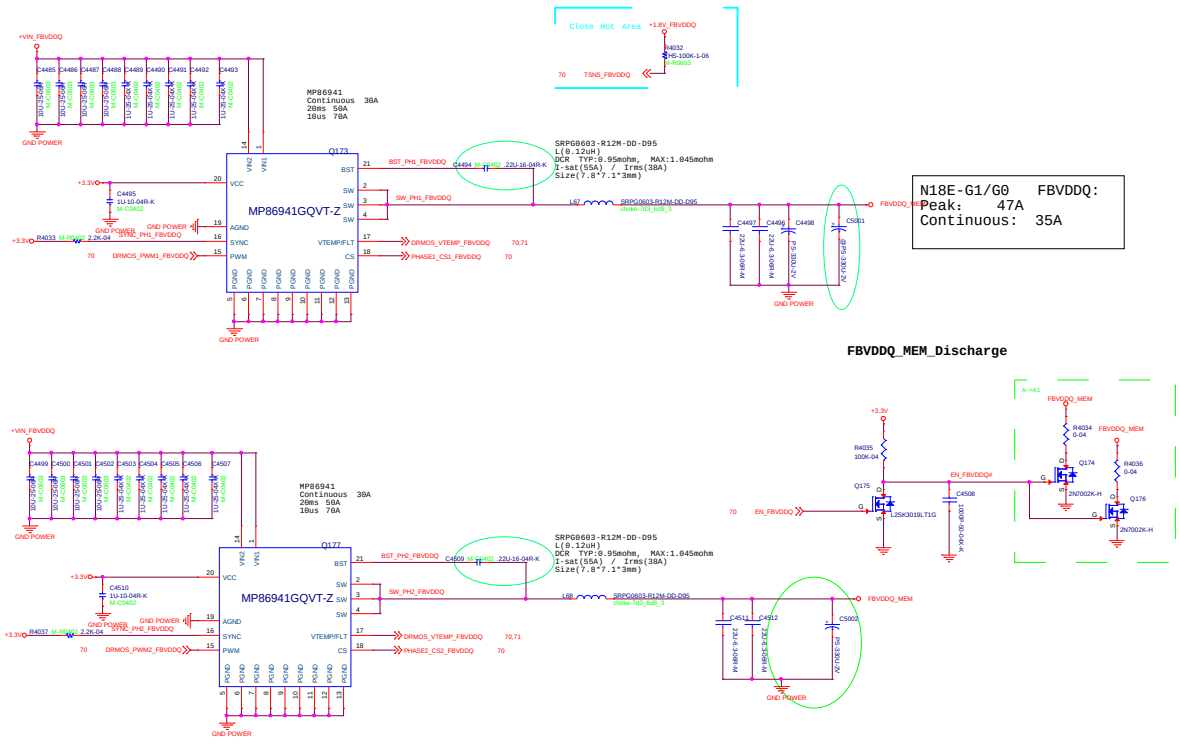

Title	71_POWER N18E FBVDDQ 2PHASE		
Size C	Document Number GKXCX7X		Rev A
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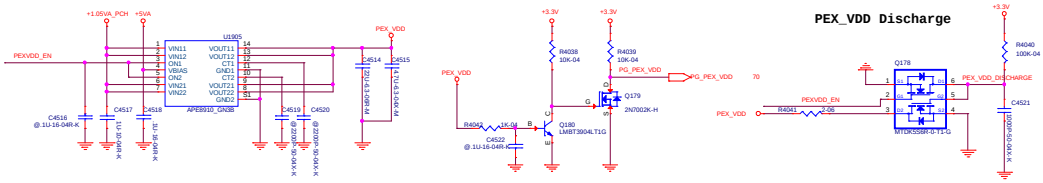
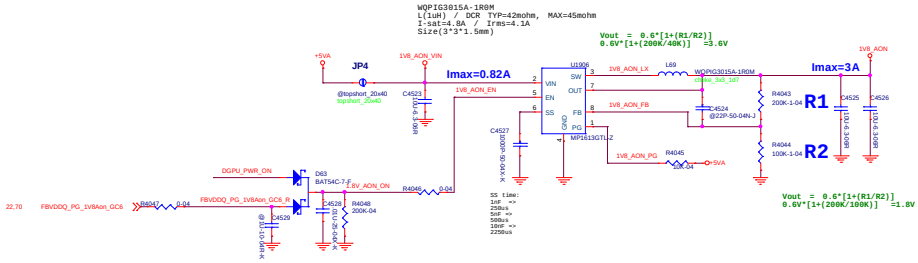
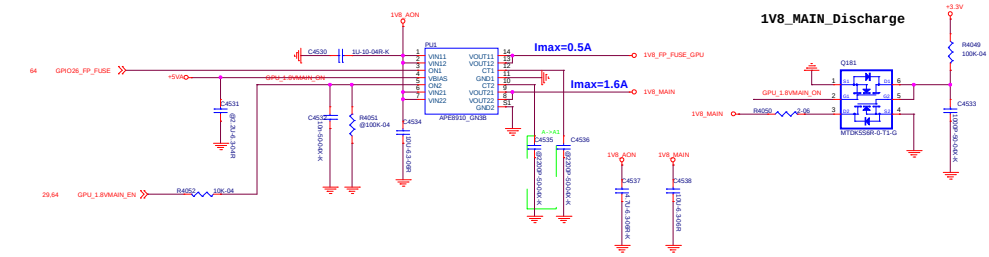
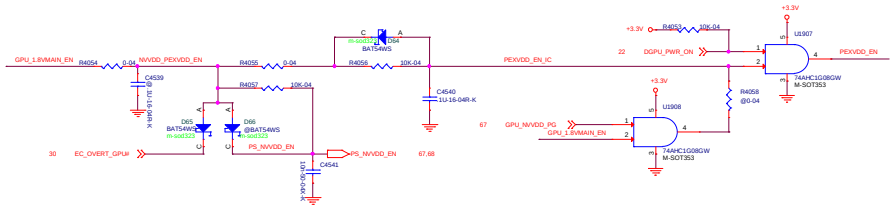
PEX_VDD SW



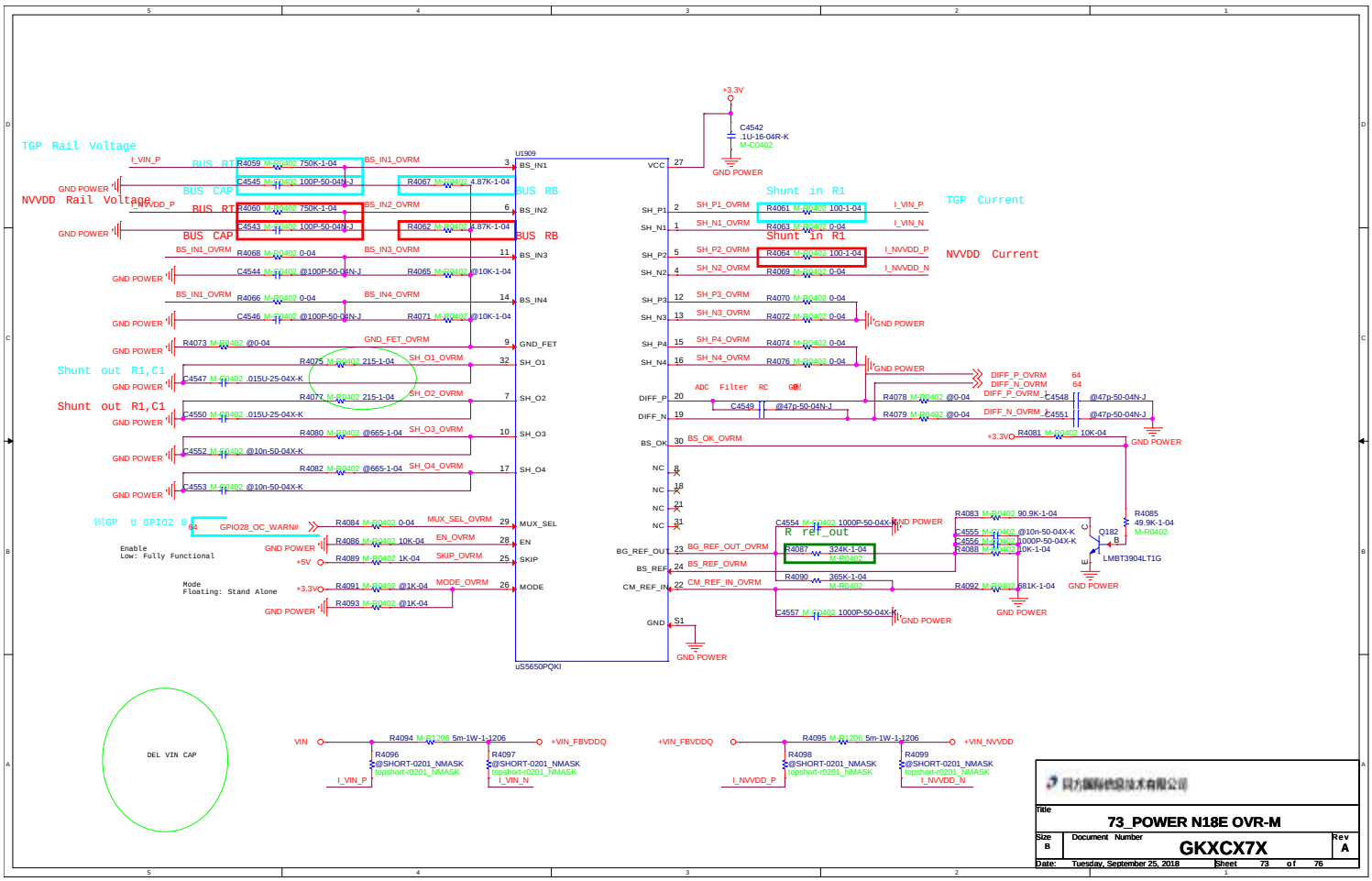
1V8_AON/1V8_MAIN

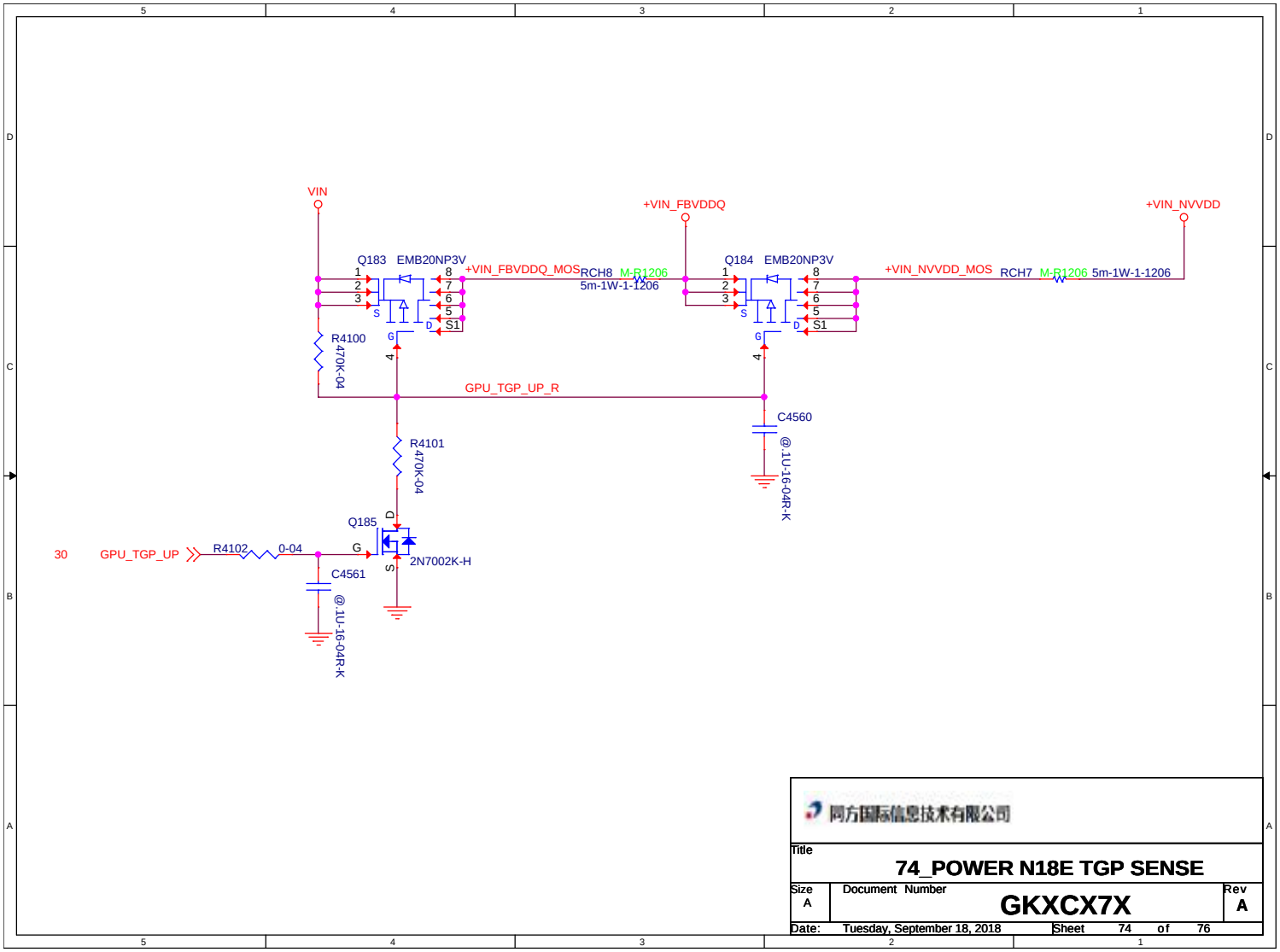






Title	72_POWER N18E PEX_VDD/1V8_AON			
Size C	Document Number GKXCX7X			Rev A
Date: Friday, September 14, 2018	Sheet 72 of 78			


TGP Rail Voltage
NVVDD Rail Voltage
BUS RT
BUS CAP
BUS RB
Shunt out R1,C1
Shunt in R1
TGP Current
NVVDD Current
U1909
uS5650PQKI
+3.3V
GND POWER
DEL VIN CAP
Title
73_POWER N18E OVR-M
Size B
Document Number
GKXCX7X
Rev A
Date: Tuesday, September 25, 2018
Sheet 73 of 76



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Title: 74_POWER N18E TGP SENSE

Size	Document Number	Rev
A	GKXCX7X	A

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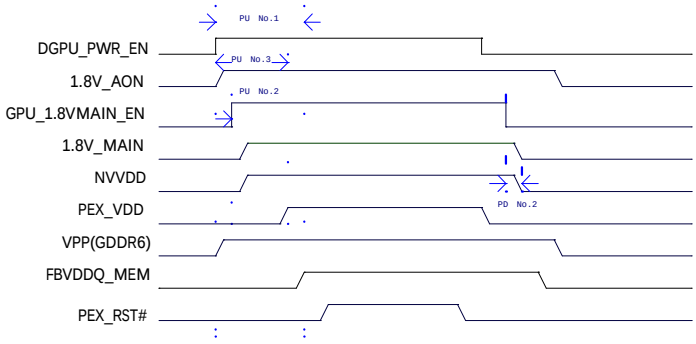
Not Used

DGPU POWER SEQUENCE



POWER UP sequence is required:1.8V_AON->1.8V_MAIN->NVVDD->/PEX_DVDD->FBVDDQ_MEM
1.The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.
2.Delay From GPU_1.8VMAIN_EN to PEX_DVDD/PG_PEX_VDD) must NOT exceed 4ms.
3.Delay From 1.8V_AON to PEX_DVDD/PG_PEX_VDD) must NOT exceed 20ms.
4.The ramp-up overshoot should not exceed the silicon reliability limit voltage
5.Power up NVVDD must be 90% before PEX_DVDD and NVVDDS can start ramp up.
6.Power up 1.8V_AON must be 90% before NV 3.3V ramp up.
7.All 3.3V devices that connect to the GPU must be powered after 1.8V_AON ; GPU can't have any 3.3V leakage path before 1.8V_AON present.
8.FBVDDQ.USB_VPP and 1.8_AON don't need power cycle for GC6

POWER DOWN sequence is required
1.PEX_DVDD must ramp down before NVVDD.
2.The propagation delay between GPU_1.8VMAIN_EN and the NVVDD_EN pin needs to be less than 1ms during both power down.
3.For GDDR6,VPP must be equal to or higher than FBVDDQ at all time ; use gate logic and discharge circuit as needed.
4.All 3.3V devices that connect to the GPU must be ramp down before +1.8V_AON; GPU can't have any 3.3V leakage path after +1.8V_AON and +1.8V_MAIN power down.
5.Power down PEX_DVDD must be less than 10% before NVVDD can start ramp down.
6.Power down NV 3.3V must be less than 10% before +1.8V_AON can start ramp down.

[redacted]

Title	75_GPU POWER SEQUENCE	
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1. Unmount R176,R177 ,R188 for GDDR6 strap pin

2. Modify VALUE for Q5,Q7,Q9,Q10,Q11,Q12,Q16,Q21,U3,U1

3. Unmount CAP 10U 6.3V 0603
C1140,C1125,C1069,C1145,C1134,C600,C1119,C1113,C601,
C976,C1043,C591,C975,C983,C1044,C1083,C1159,C1042,C1114,
C1112,C734,C1001,C1150,C997,C998,C999,C1148,C1154,C1139,
C1147,C1149,C605,C607,C625,C628,C606,C626,C885,C943,C1228,
C1223,C1185,C1232,C1225,C1191,C1184,C1226,C1229,C1234,C1227,
C1021,C1095,C226,C243,C233,C224,C235,C255,C210,C1021,C1095

4. Mount 22U 6.3V 0603 CAP
C983,C1119,C1145,C1044,C1140,C1112,C1042,C976,C975,C600,
C1150,C1148,C1139,C998,C1001,C885,C943,C1191,C1184,C1185,
C1226,C1228,C1223,C1021,C243,C224,C235,C255,C211,C205,C1021

5. Unmount CAP 1U 10V 0402
C1178,C1111,C1047,C1019,C933,C809,C1155,C1167,C1164,C931,C1073,
C932,C867,C866,C930,C910,C1165,C1170,C1156,C1177,C1176,C849,
C1162,C1182,C899,C1049,C929,C1180,C1006,C821,C937,C848,C1172,C1117,C863,C877

6. Mount 4.7U 6.3V 0402 CAP
C1155,C1178,C1111,C933,C867,C849,C1172,C877,C848

7. R465 40K 0402 change to 40.2K 0402

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Title: 76_History		
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