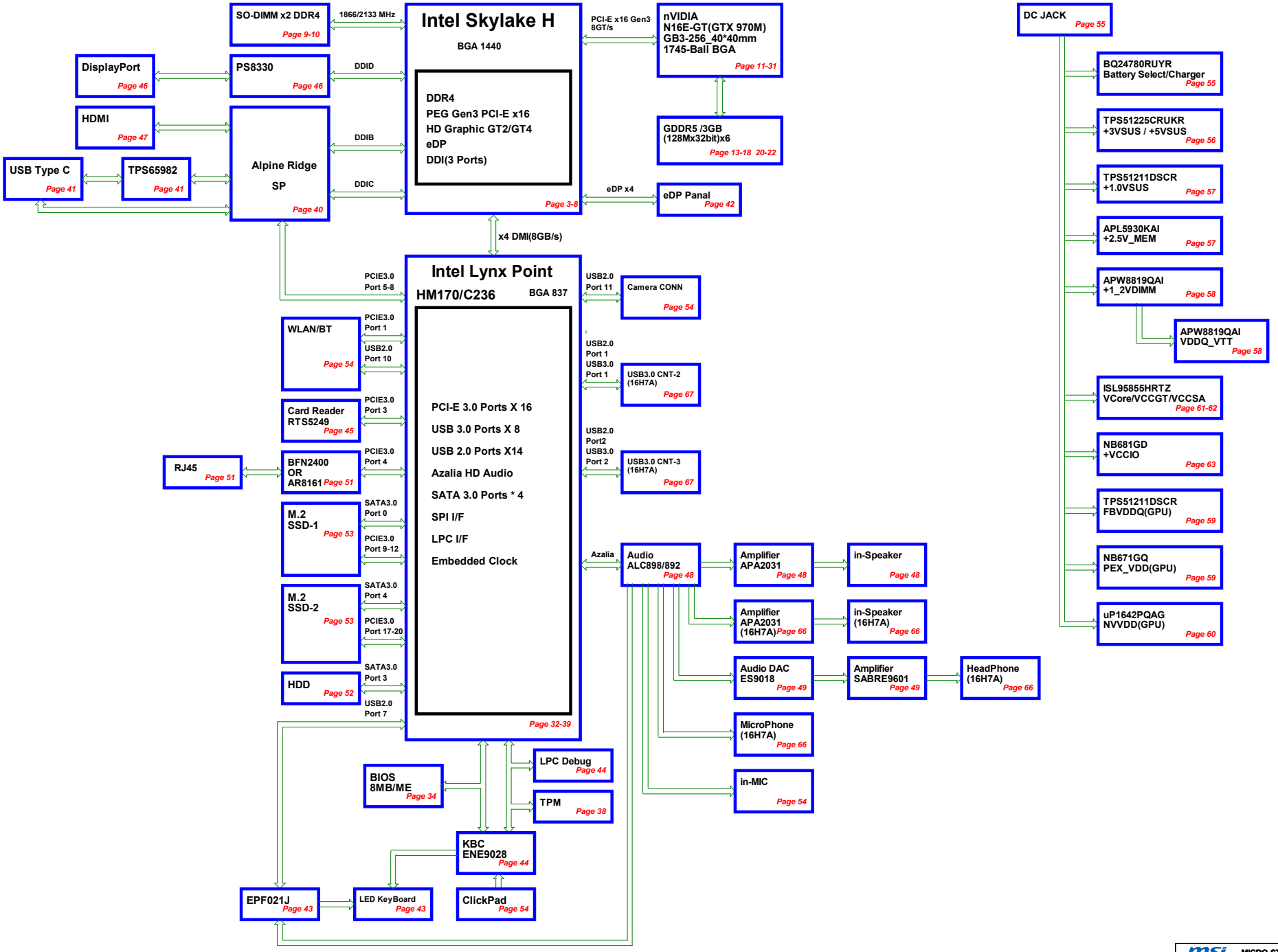
MS-16H7 Ver:1.1 Intel Skylake Platform



msi MICRO-STAR INT'L CO.,LTD.

Title: Block Diagram

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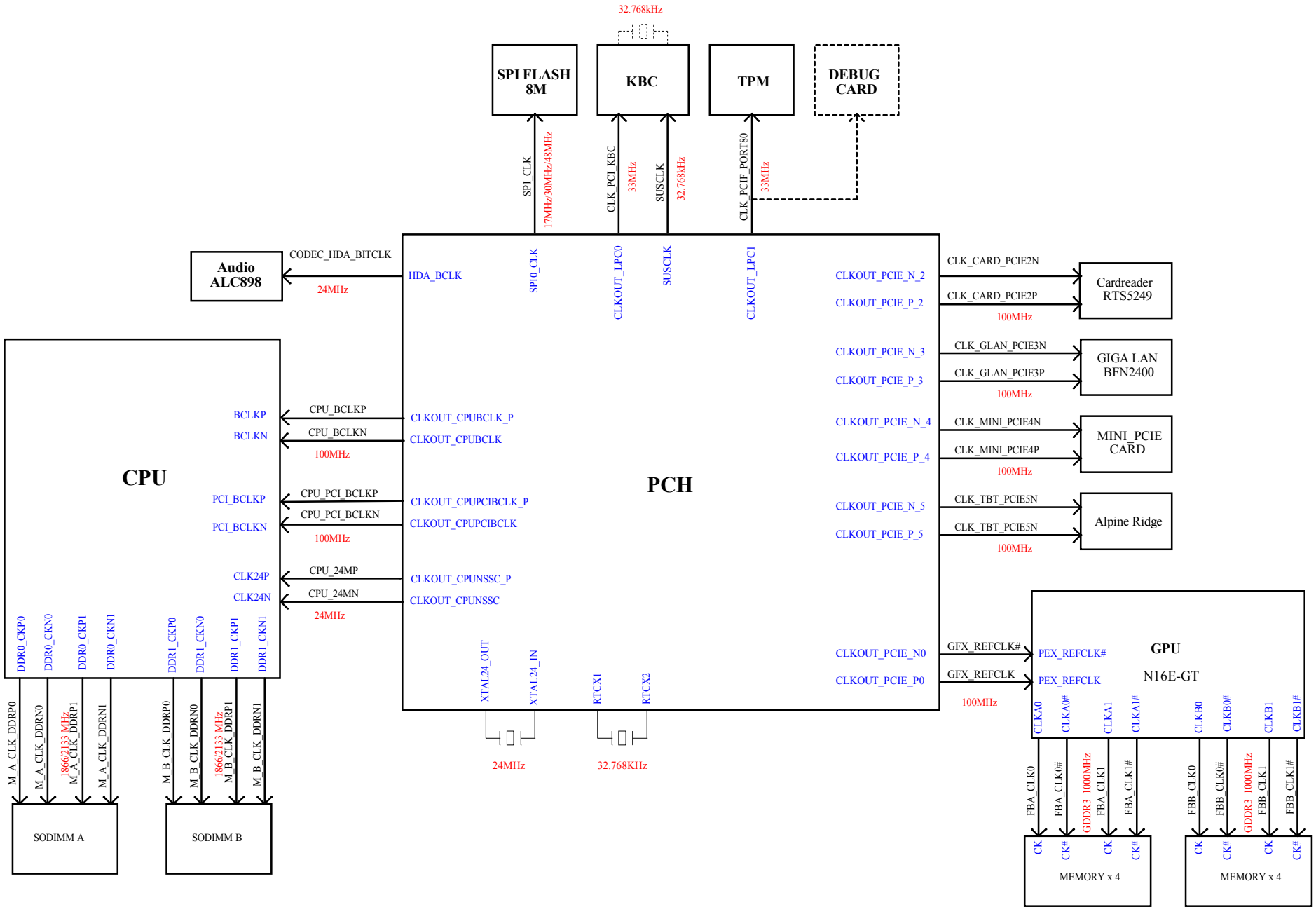
Date: | Sheet 1 of 74



MICRO-STAR INT'L CO.,LTD.

Title: CLock Delivery chart

Size | Document Number: MS-16H7 | Rev: 1.1

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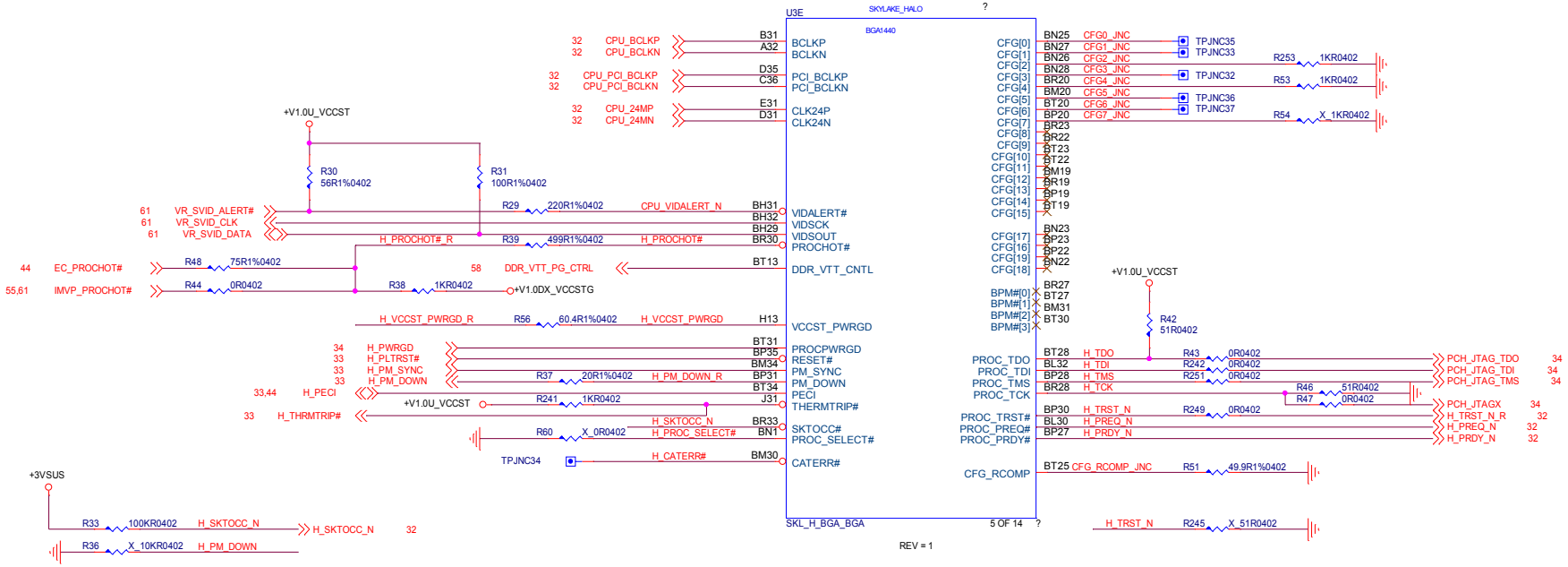

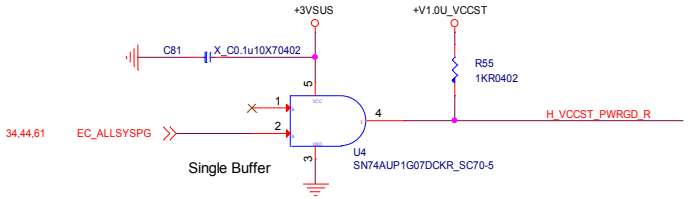

PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reserved

Display Port Presence strap	
CFG4	1:Disabled - No Physical Display Port attached to Embedded DisplayPort*. No connect for disable. 0:Enabled - A Display Port device is connected to the Embedded Display Port. Pull-down to GND through a 1 KΩ ±5% resistor to enable port

PCI Express* Bifurcation	
CFG[6:5]	00 = 1x8, 2x4 PCI Express* 01 = reserved 10 = 2x8 PCI Express* 11 = 1x16 PCI Express* Recommend 1K Ω ±5% pull-down resistor to GND.

PEG Training	
CFG7	1 = (default) PEG train immediately following RESET# de assertion. 0 = PEG wait BIOS for training.

I7-6700HQ

I7_6700

A0D-6700H15-I06

I7-6700HQ

MICRO-STAR INT'L CO.,LTD.

Title: Skylake(HOST)

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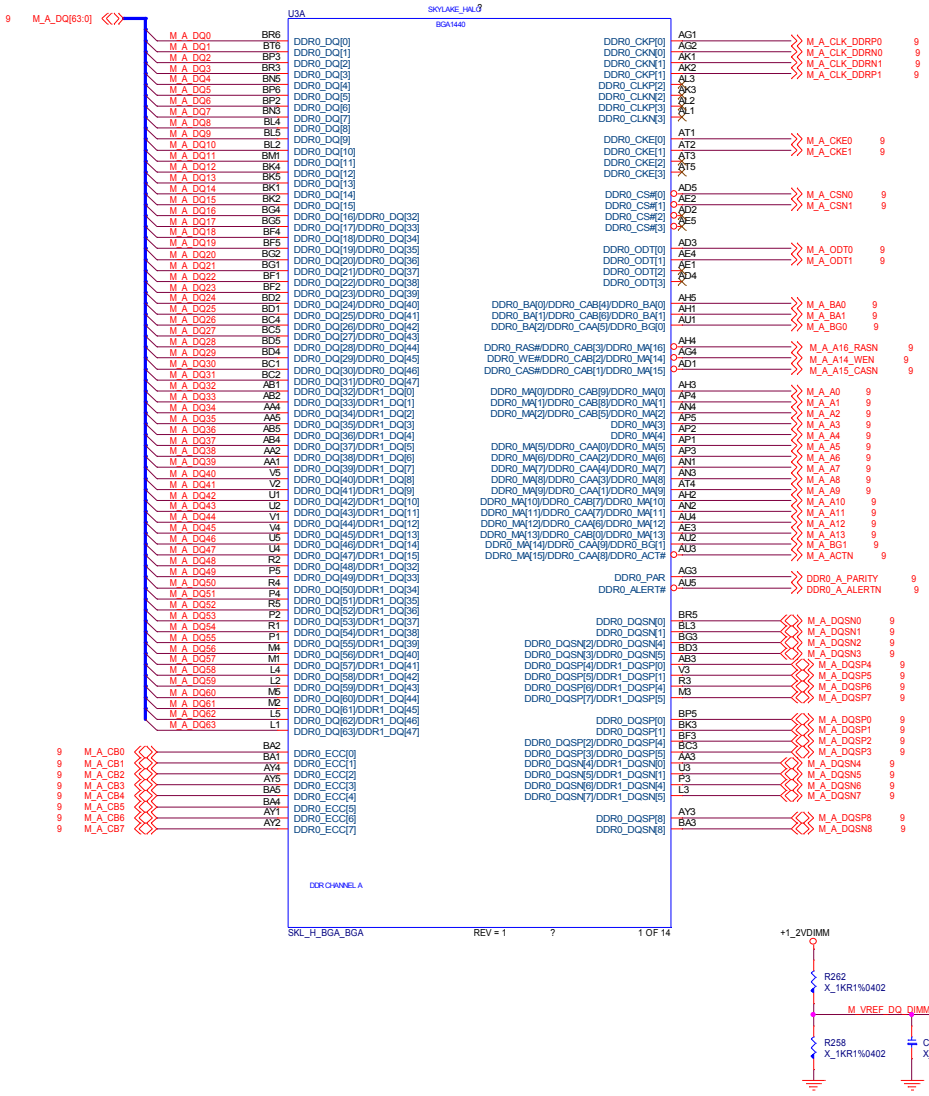
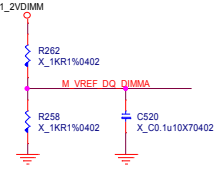
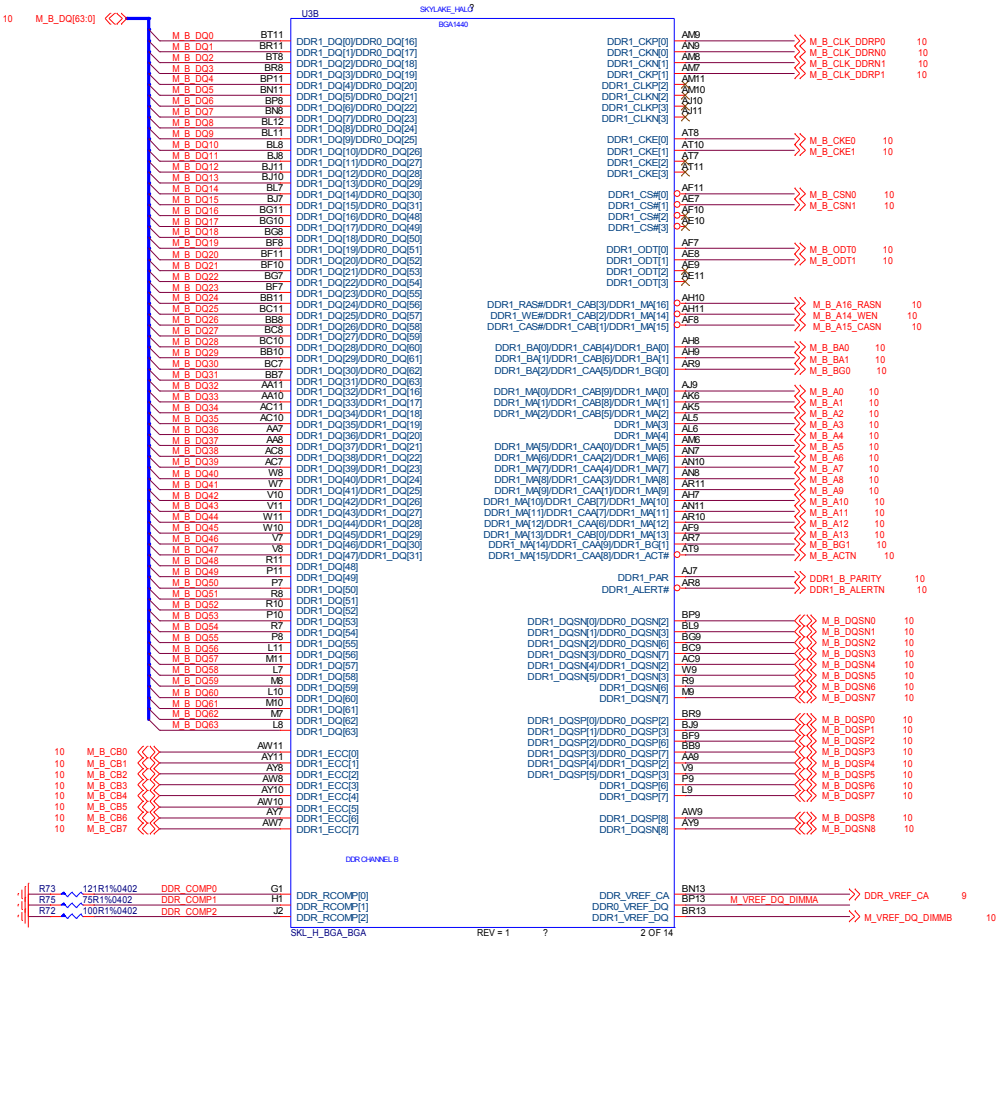
DDR Channel A





DDR Channel B



msi	MICRO-STAR INT'L CO.,LTD.	
Title	Skylake(DDR4)	
Size	Document Number MS-16H7	Rev 1.1
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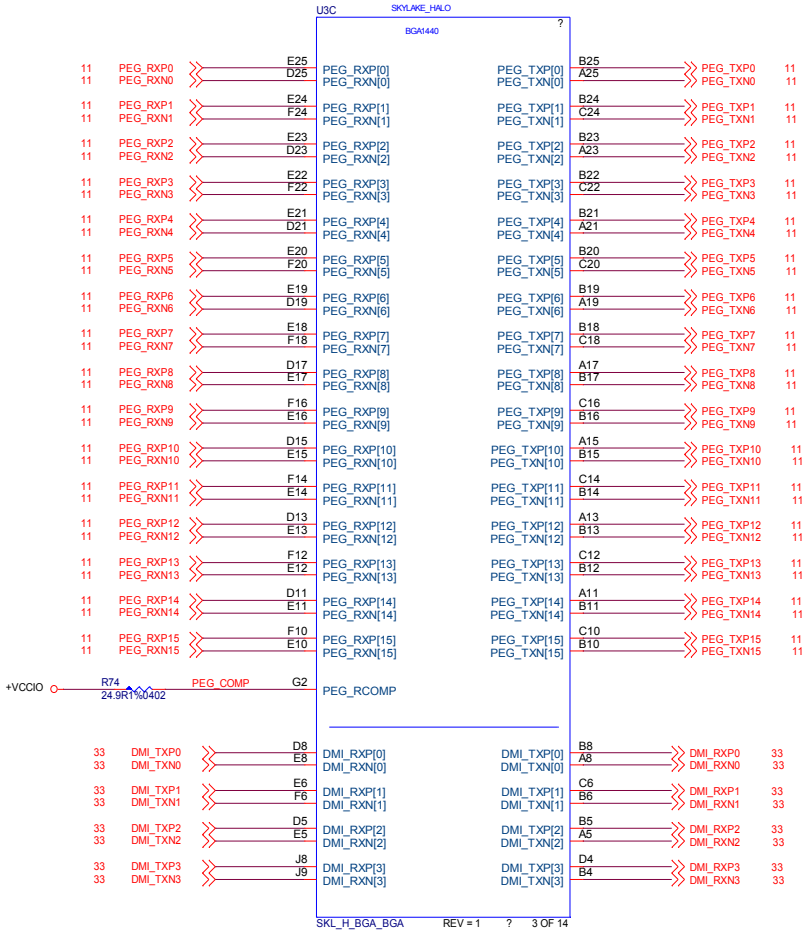

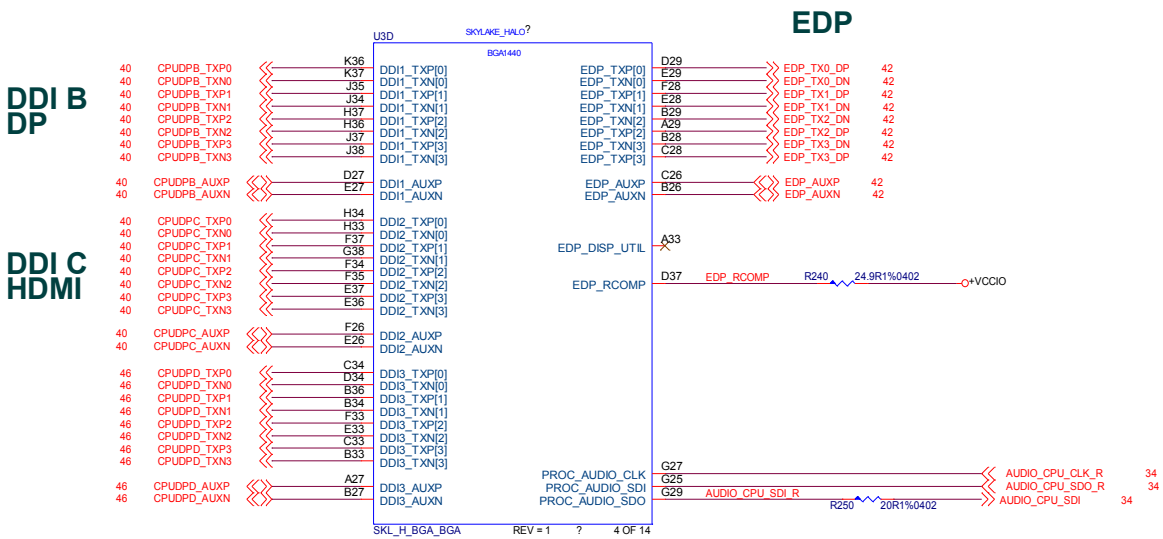

MICRO-STAR INT'L CO.,LTD.

Title	Skylake(DMI/Display)	
Size	Document Number: MS-16H7	Rev: 1.1
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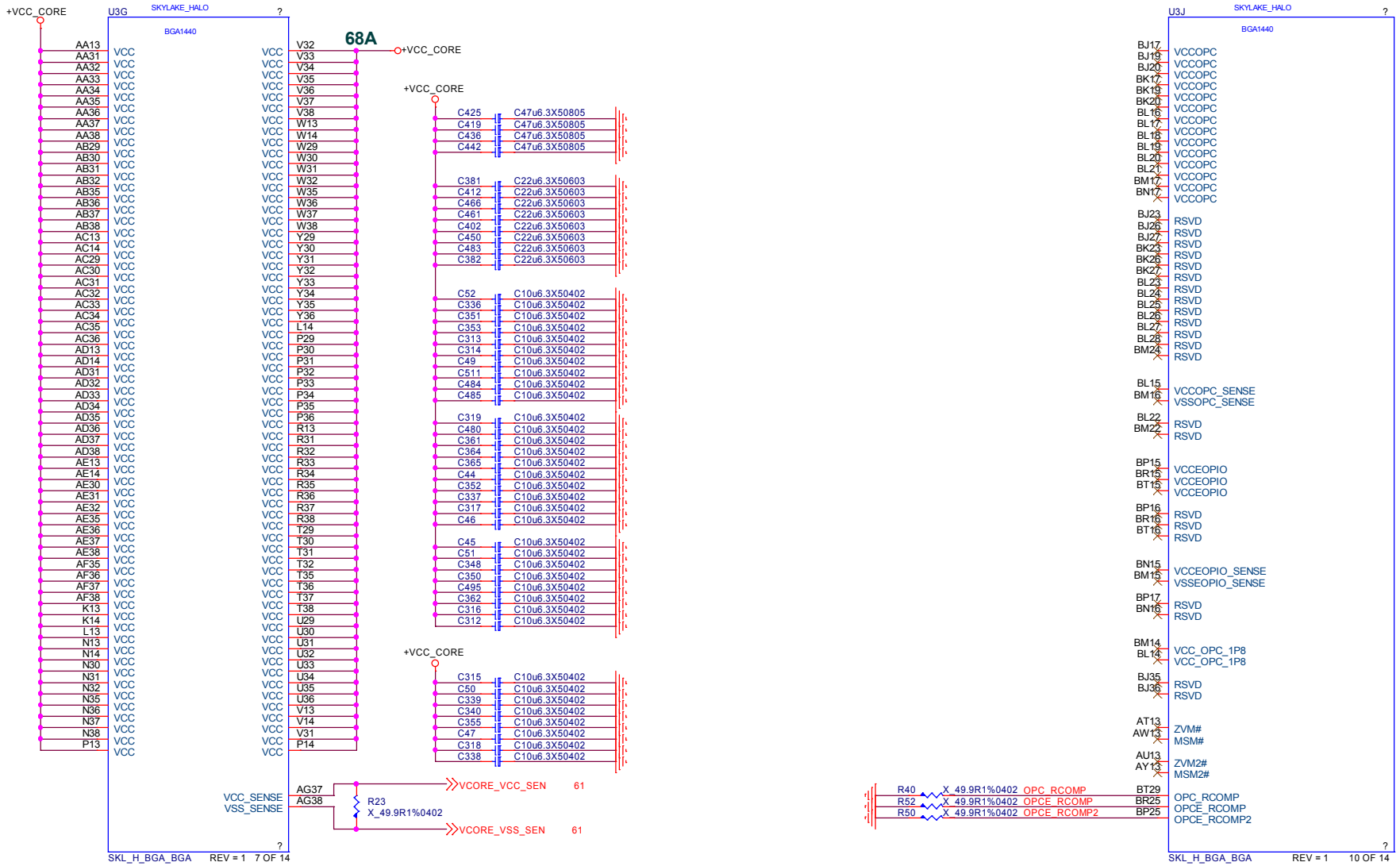
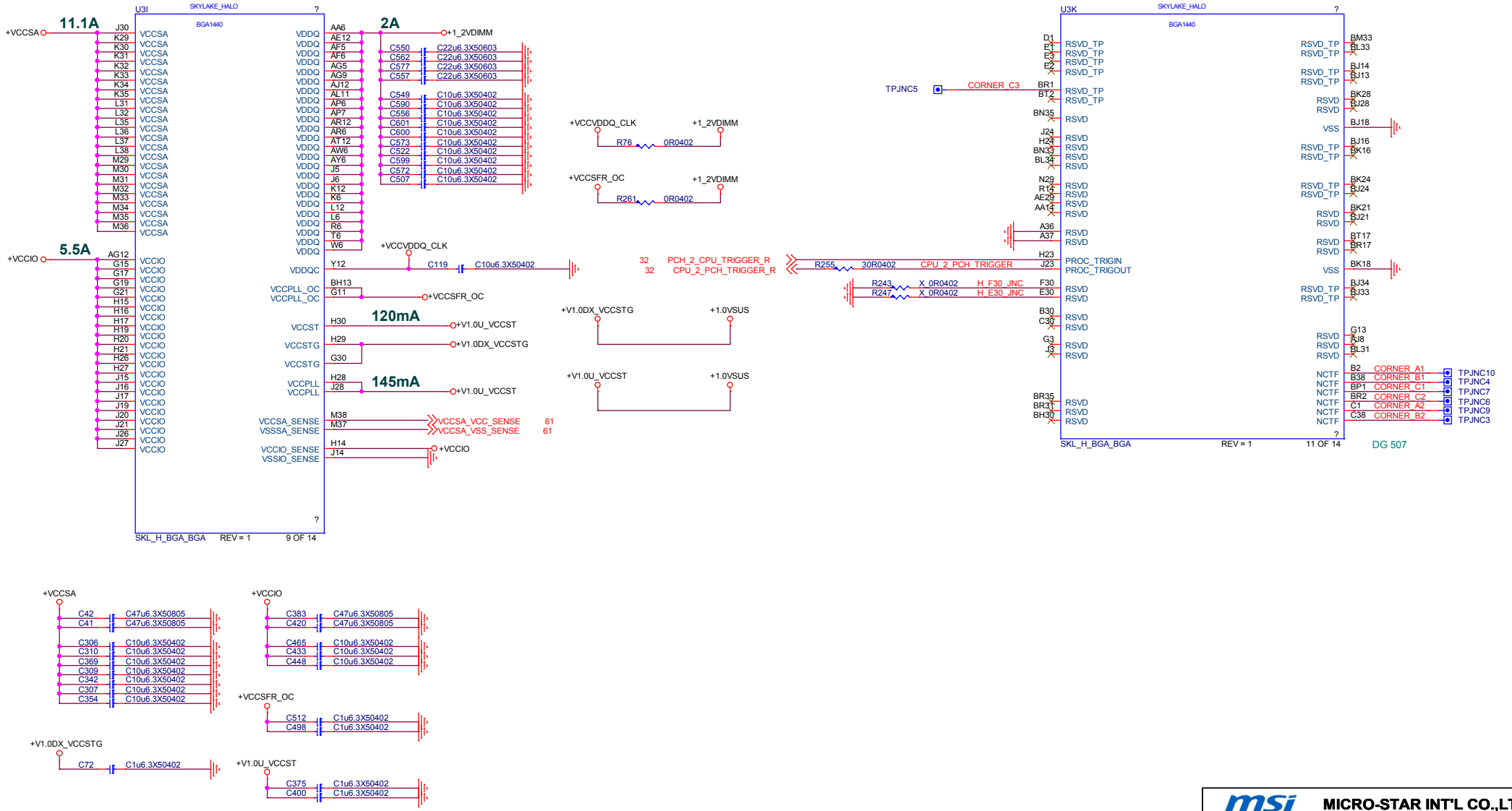


MICRO-STAR INT'L CO.,LTD.

Title: Skylake(Power1)

Size | Document Number: MS-16H7 | Rev: 1.1

Date: Wednesday, July 08, 2015 | Sheet 6 of 74

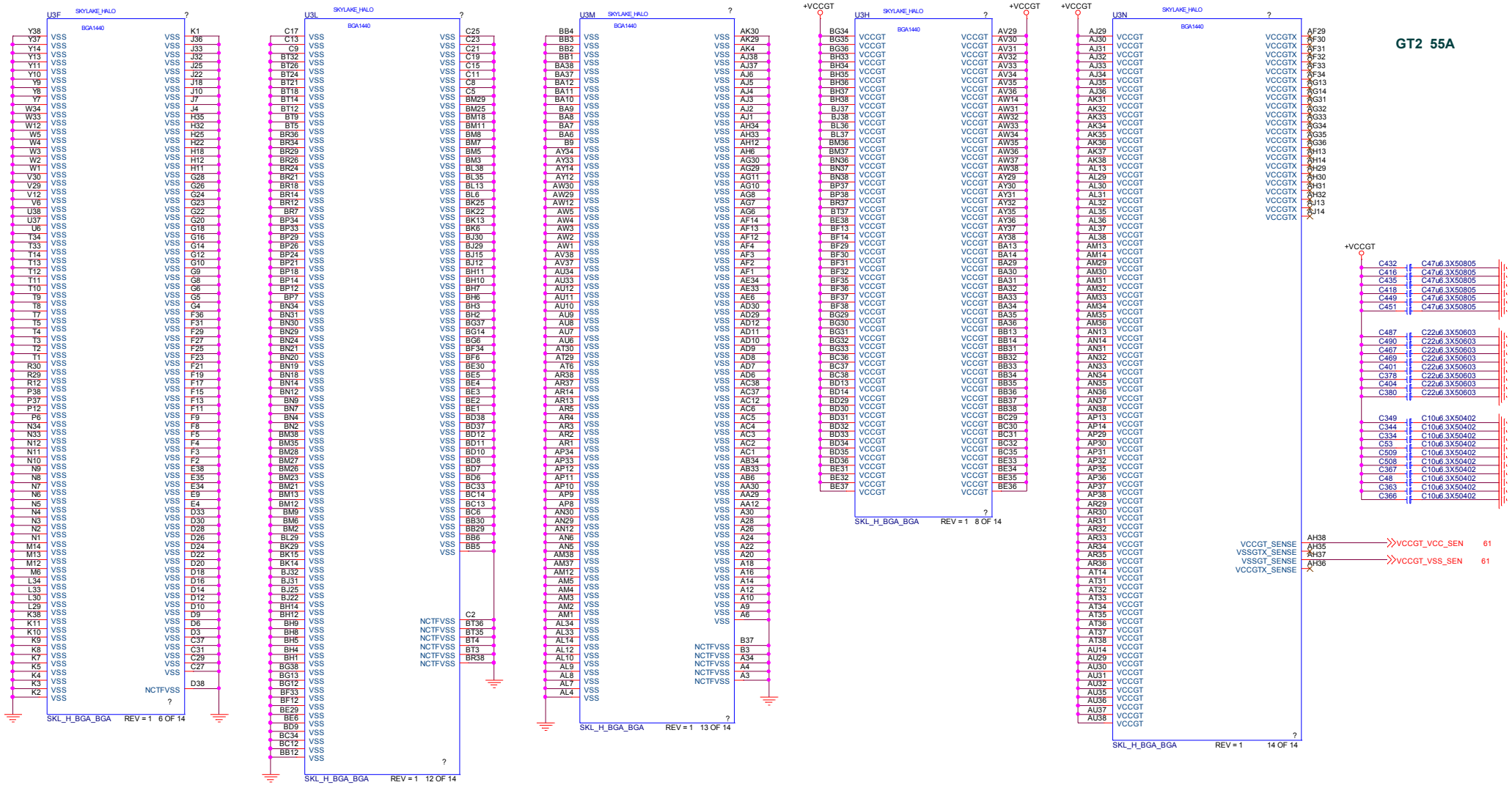


MICRO-STAR INT'L CO.,LTD.

Title: Skylake(Power2)

Size | Document Number: MS-16H7 | Rev: 1.1

Date: Wednesday, July 08, 2015 | Sheet 7 of 74



MICRO-STAR INT'L CO.,LTD.

Title: Skylake(Power3)

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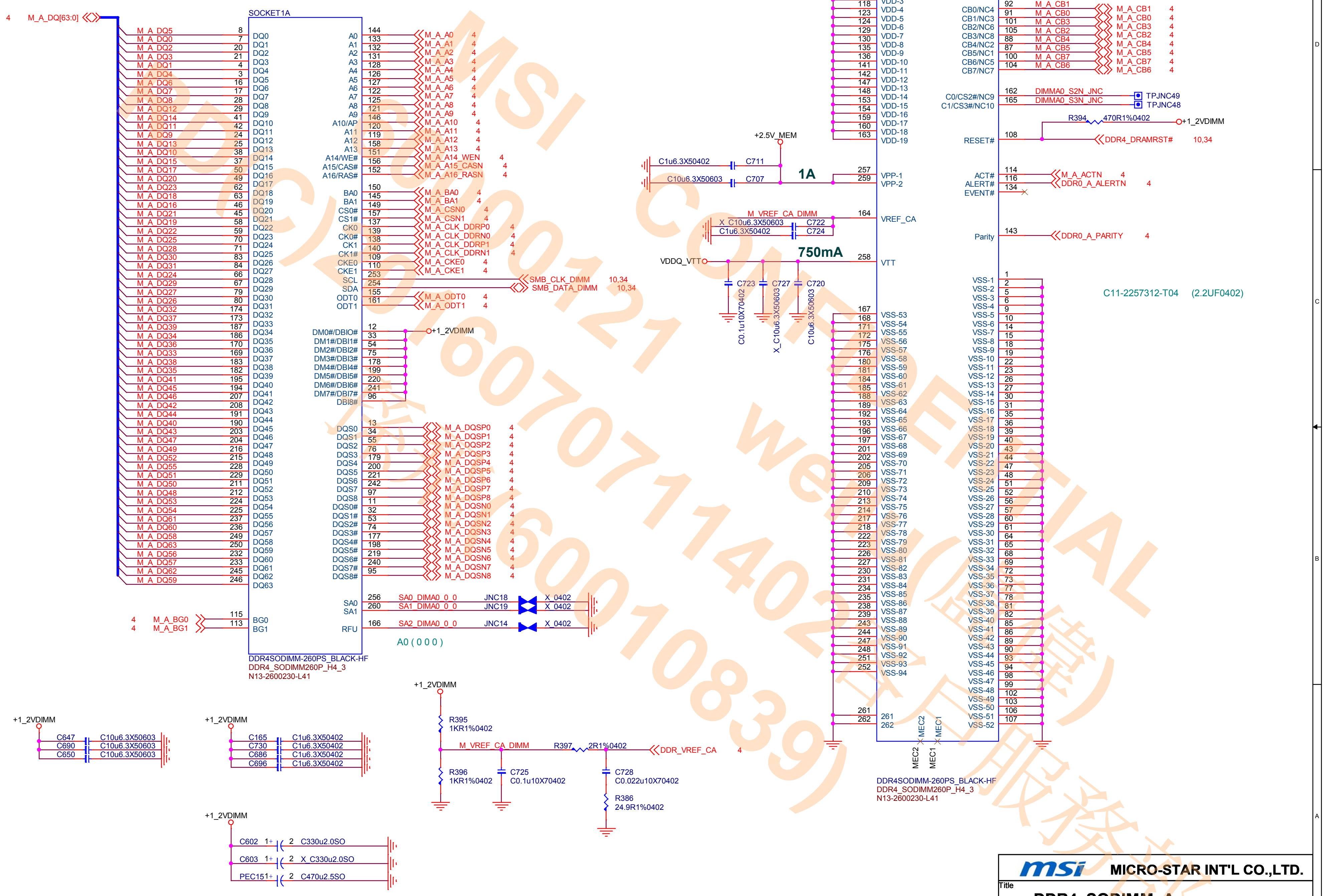
SODIMM_A0 (TOP-Standard)



msi MICRO-STAR INT'L CO.,LTD.

Title: DDR4_SODIMM_A

Size | Document Number: MS-16H7 | Rev 1.1

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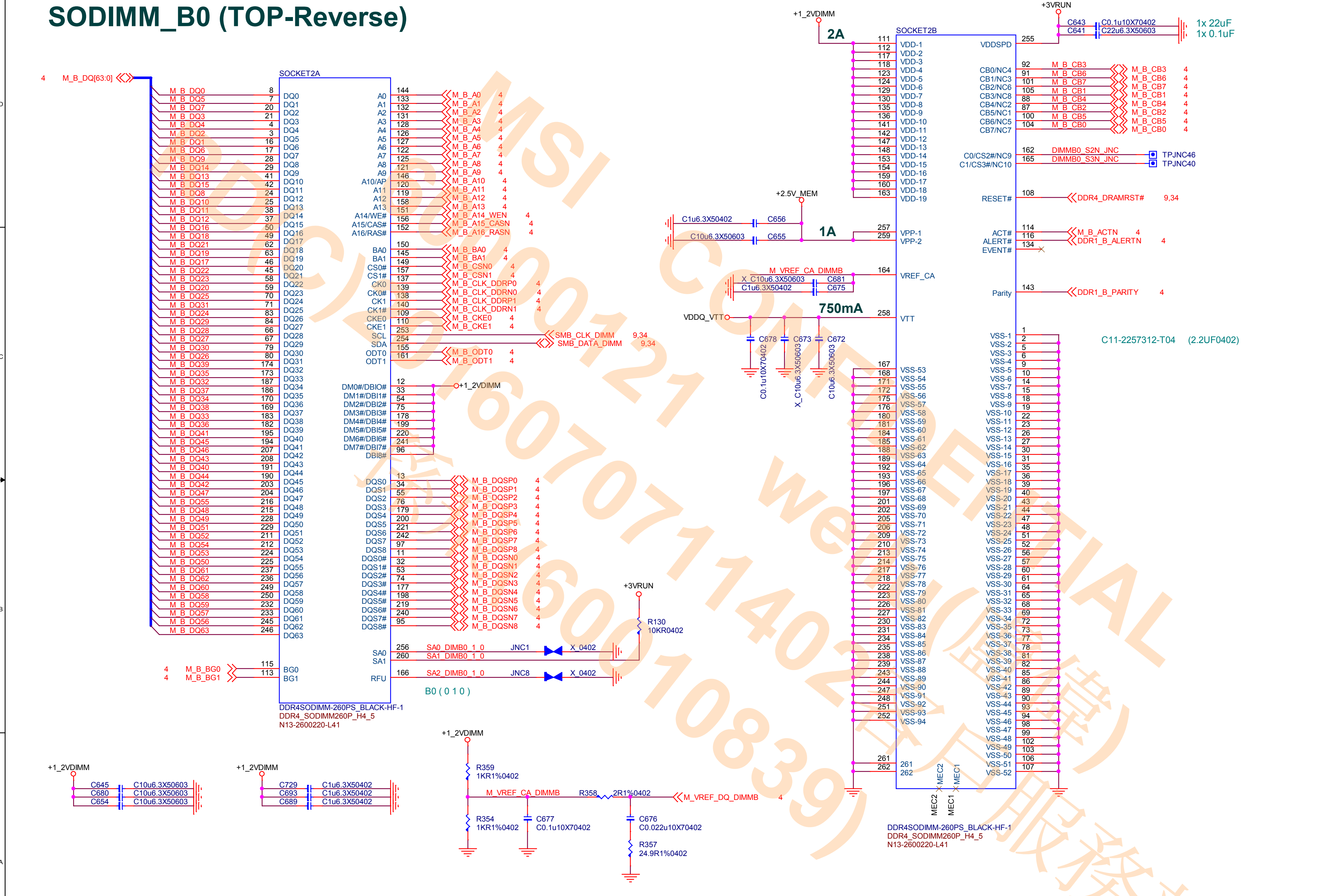
SODIMM_B0 (TOP-Reverse)



MICRO-STAR INT'L CO.,LTD.

Title: **DDR4_SODIMM_B**

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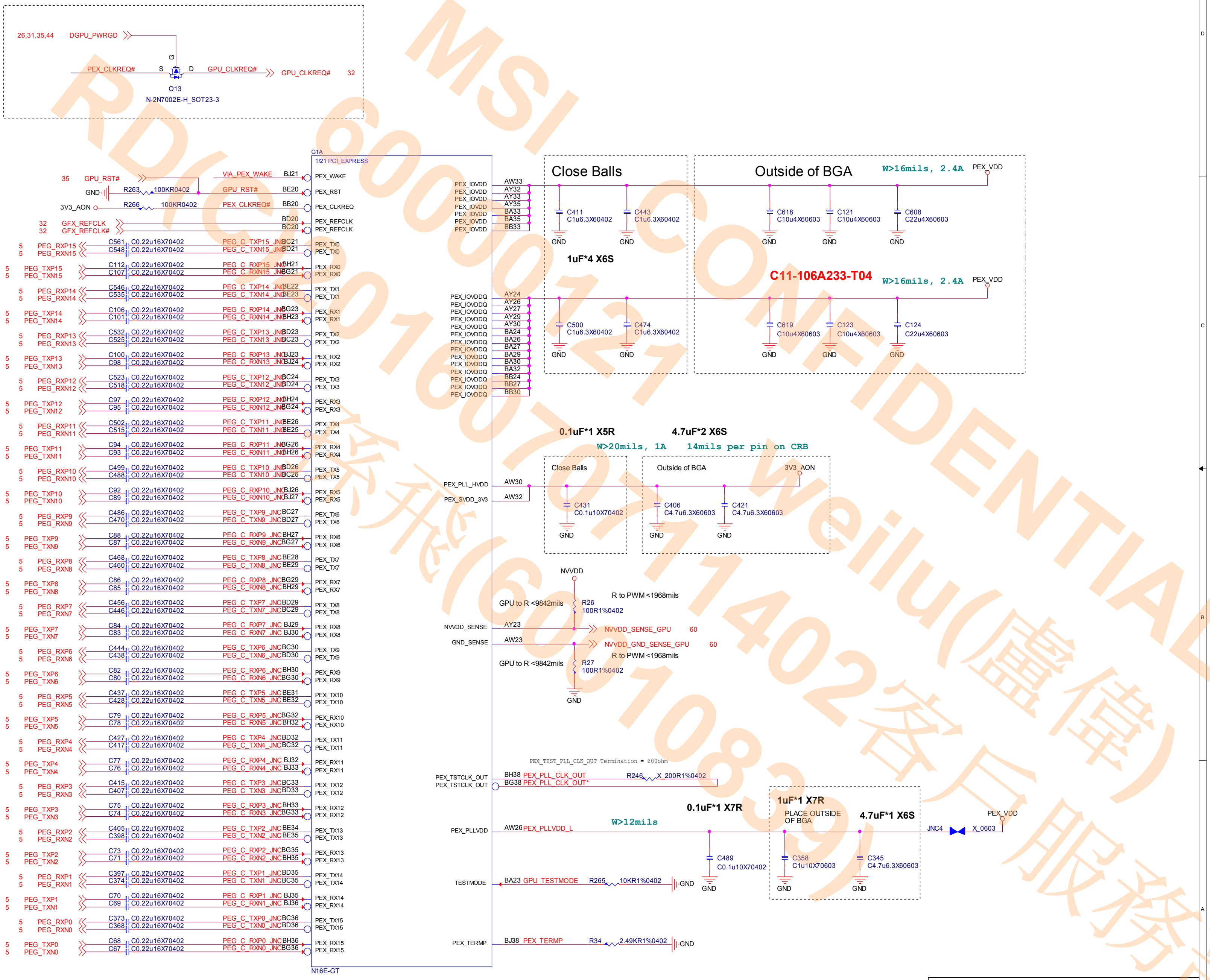
GPU PCI EXPRESS



msi MICRO-STAR INT'L CO.,LTD.

Title	DGPU_PCI-E Host
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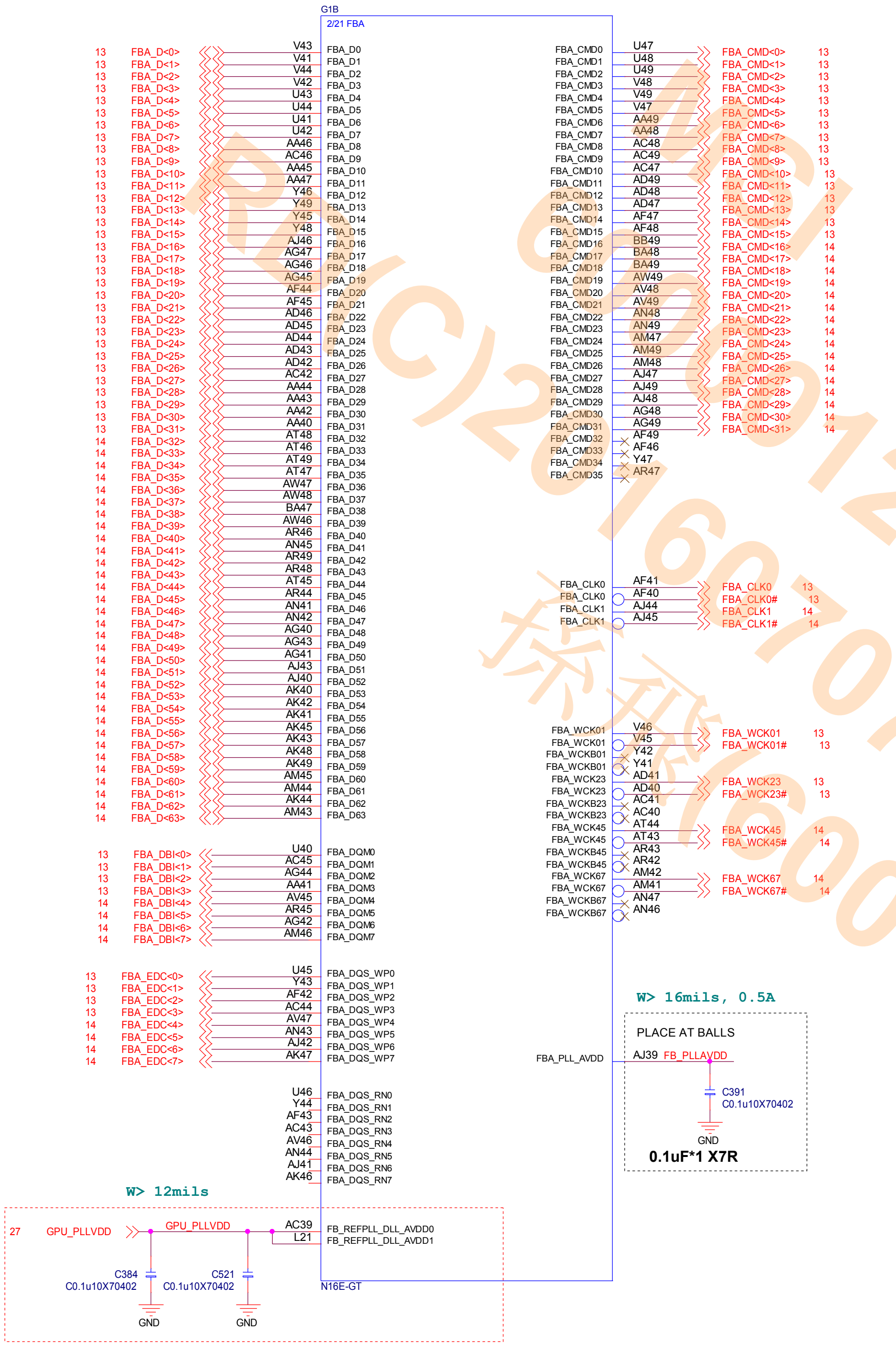
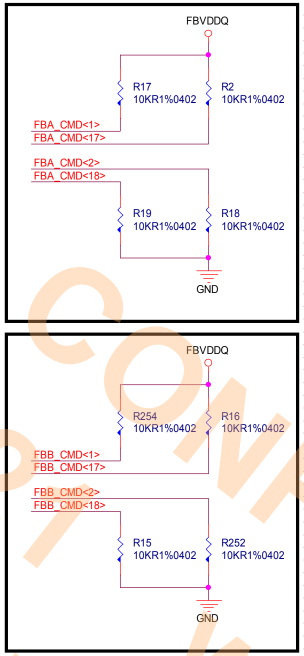
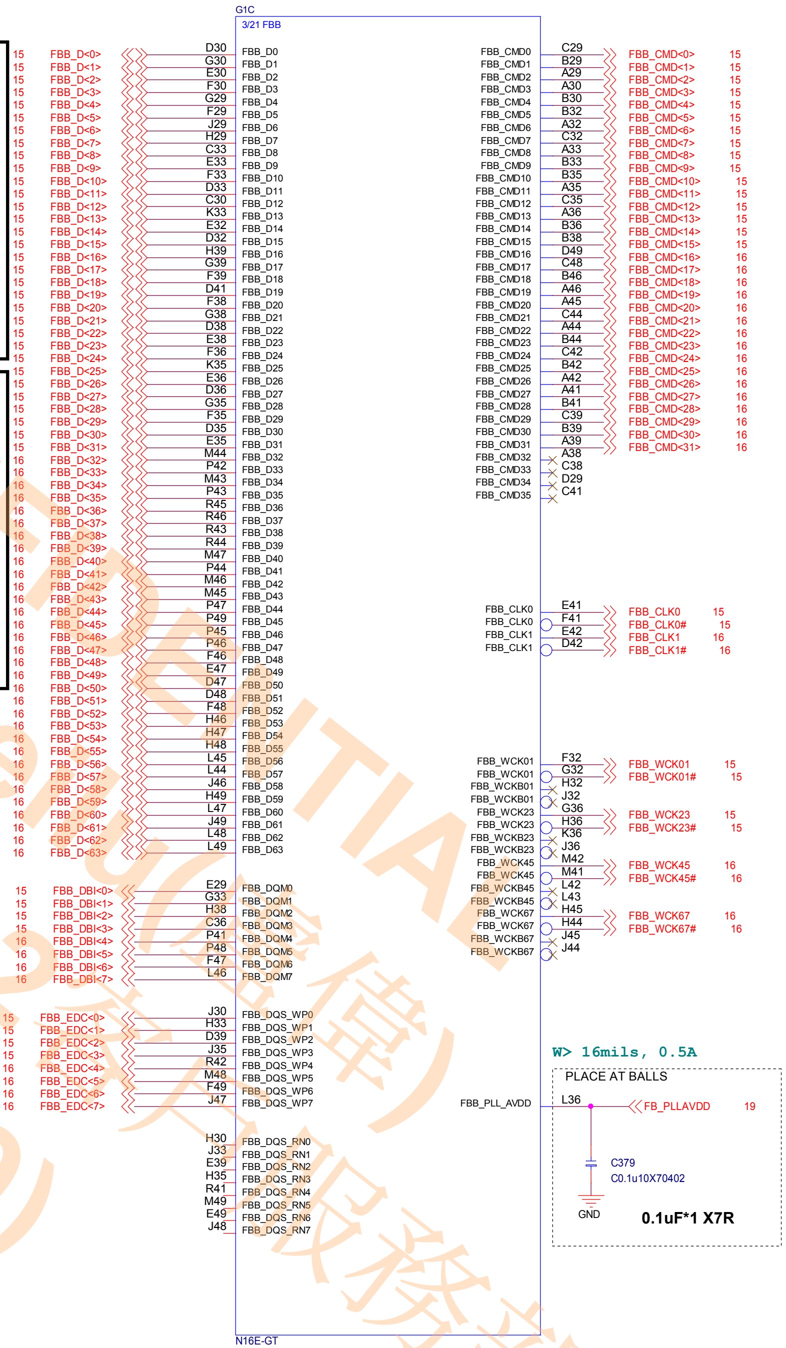
GPU Frame Buffer Partition A/B





GDDR5 Mode F Mapping By GB3-256

	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*



MICRO-STAR INT'L CO.,LTD.

Title: DGPU_MEM IF A/B

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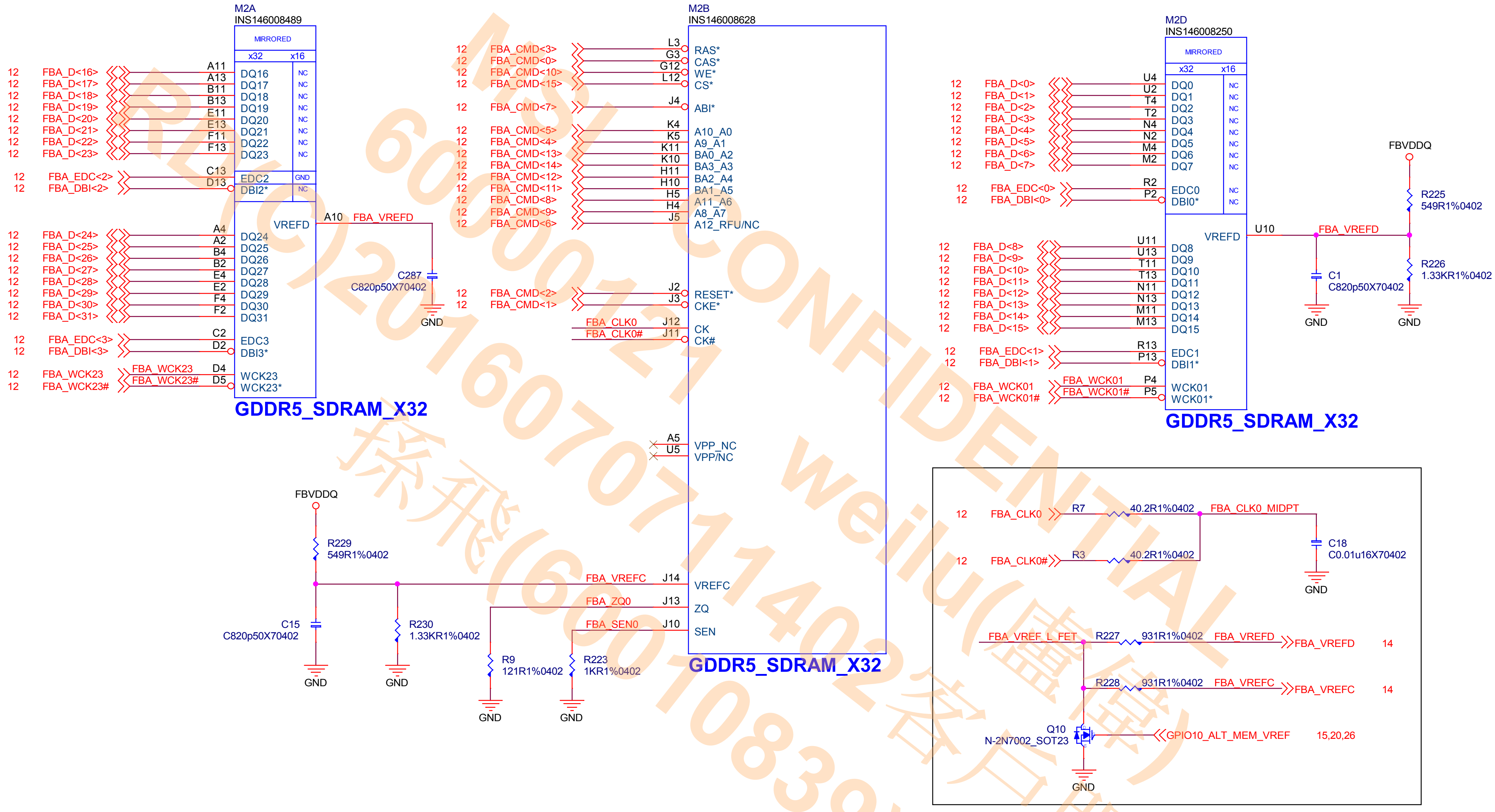
DGPU_GDDR5 FrameBuffer A0

M3 5010



MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GDDR5 FrameBuffer A0

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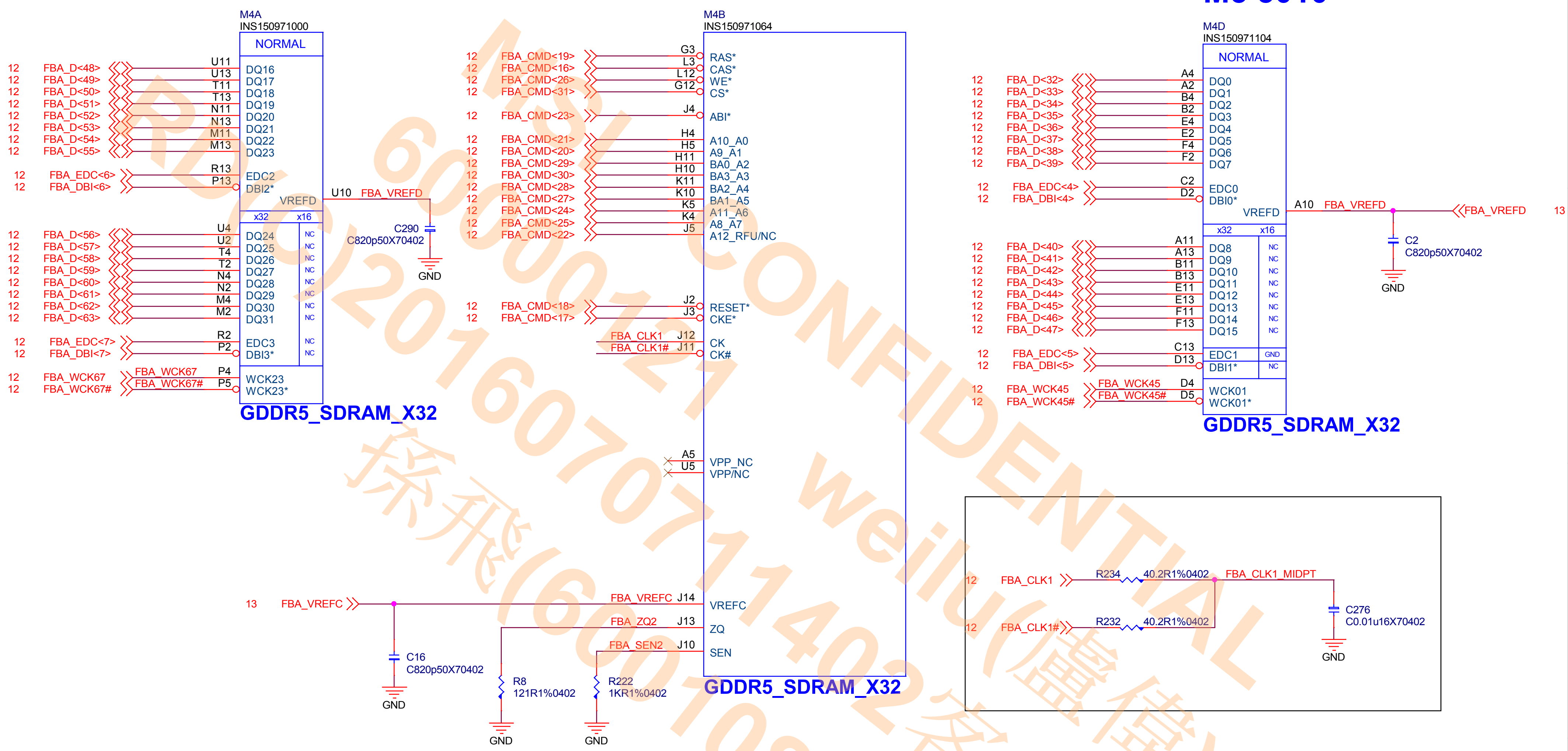
DGPU_GDDR5 FrameBuffer A1

M5 5010



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FrameBuffer A1
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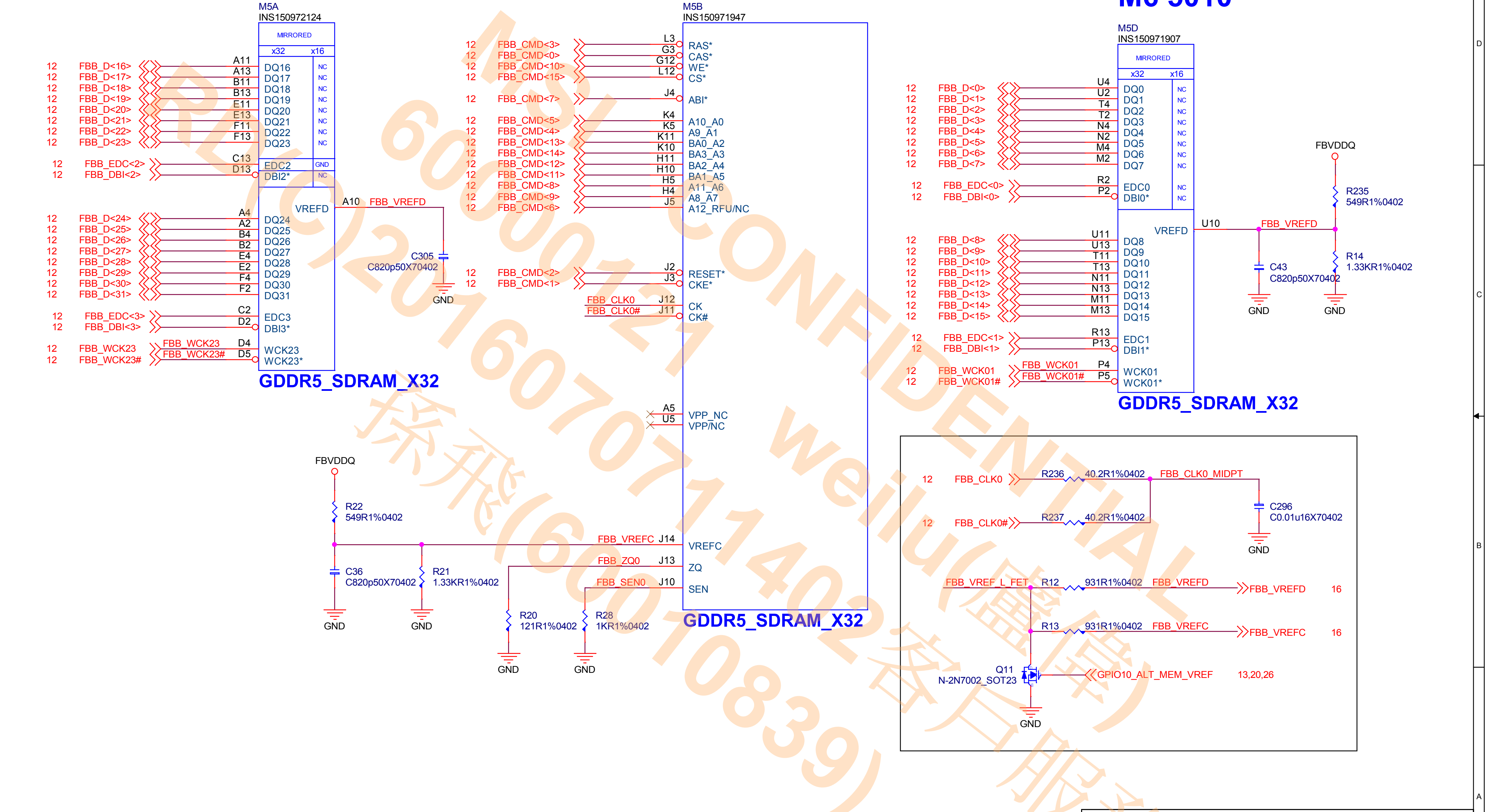
DGPU_GDDR5 FrameBuffer B0

M6 5010



msi MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FrameBuffer B0	
Size	Document Number: MS-16H7	Rev: 1.1
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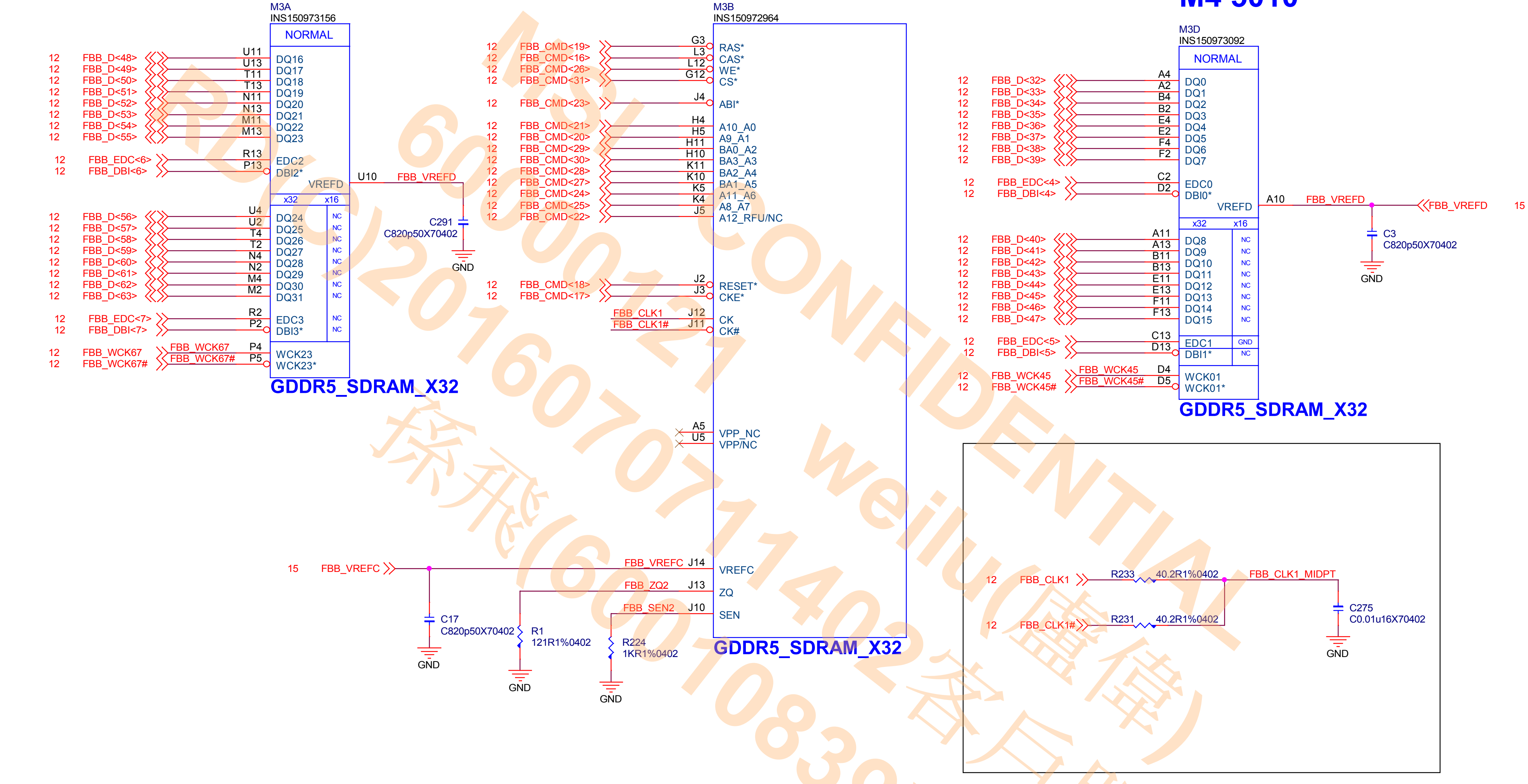
DGPU_GDDR5 FrameBuffer B1

M4 5010



msi	MICRO-STAR INT'L CO.,LTD.	
Title	DGPU_GDDR5 FrameBuffer B1	
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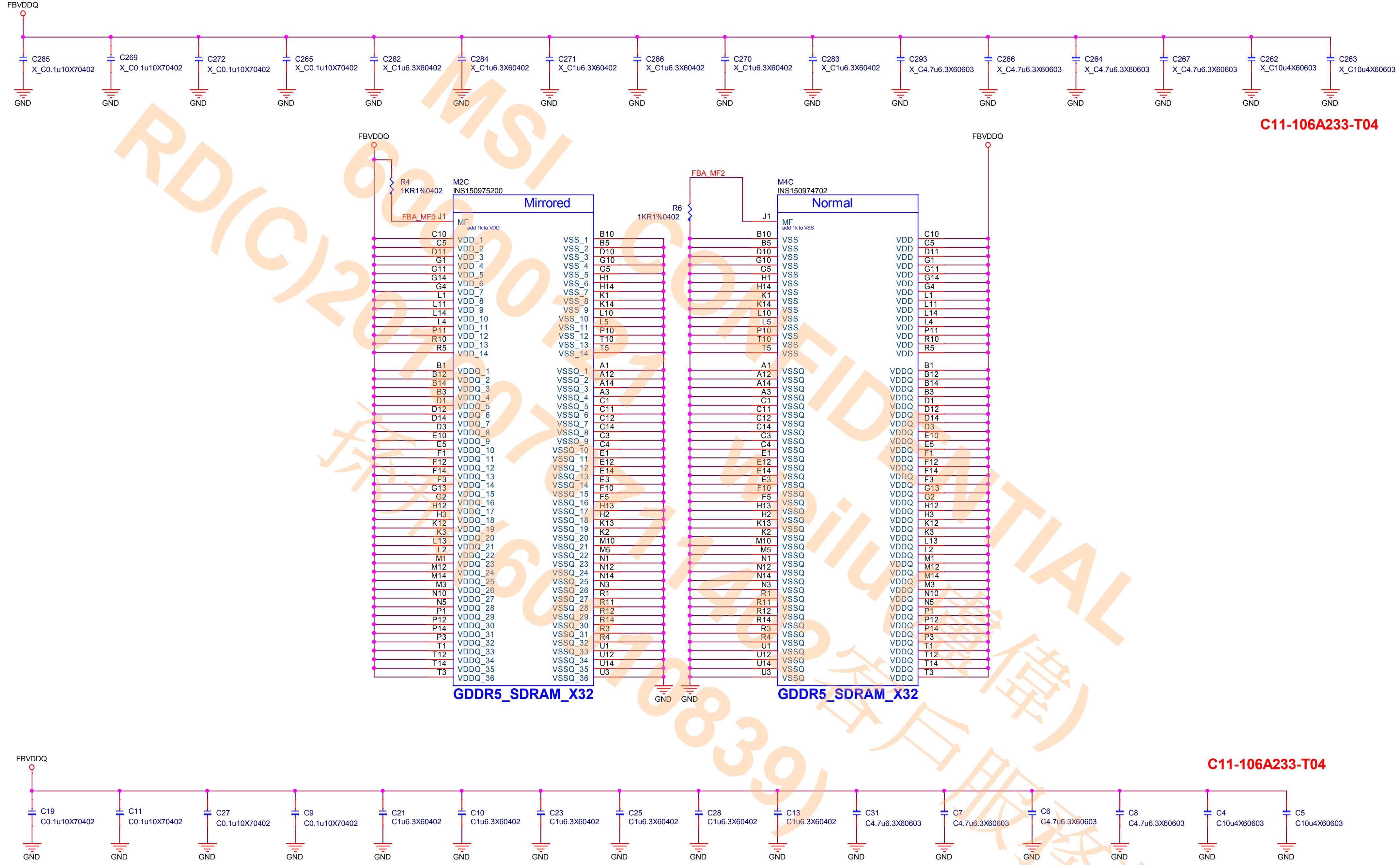
Frame Buffer Partition A Decoupling



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FB-A_DECOUPLING	
Size	Document Number: MS-16H7	Rev 1.1
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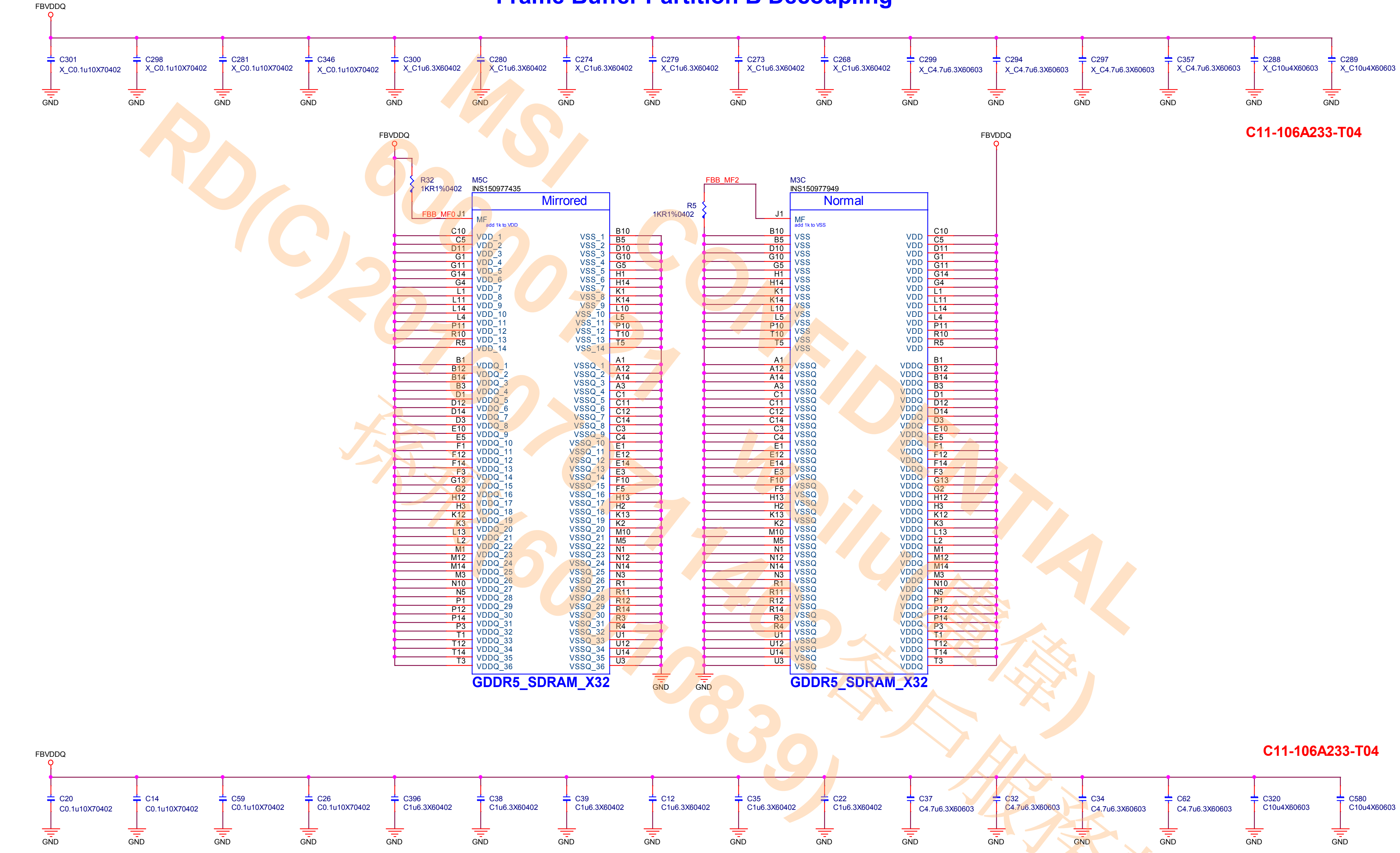
Frame Buffer Partition B Decoupling



MICRO-STAR INT'L CO.,LTD.	
Title	DGPU_GDDR5 FB-B_DECOUPLING
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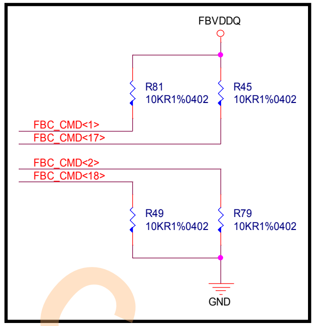
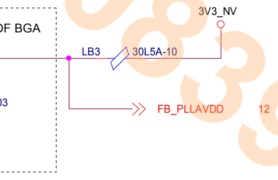
GPU Frame Buffer Partition C/D



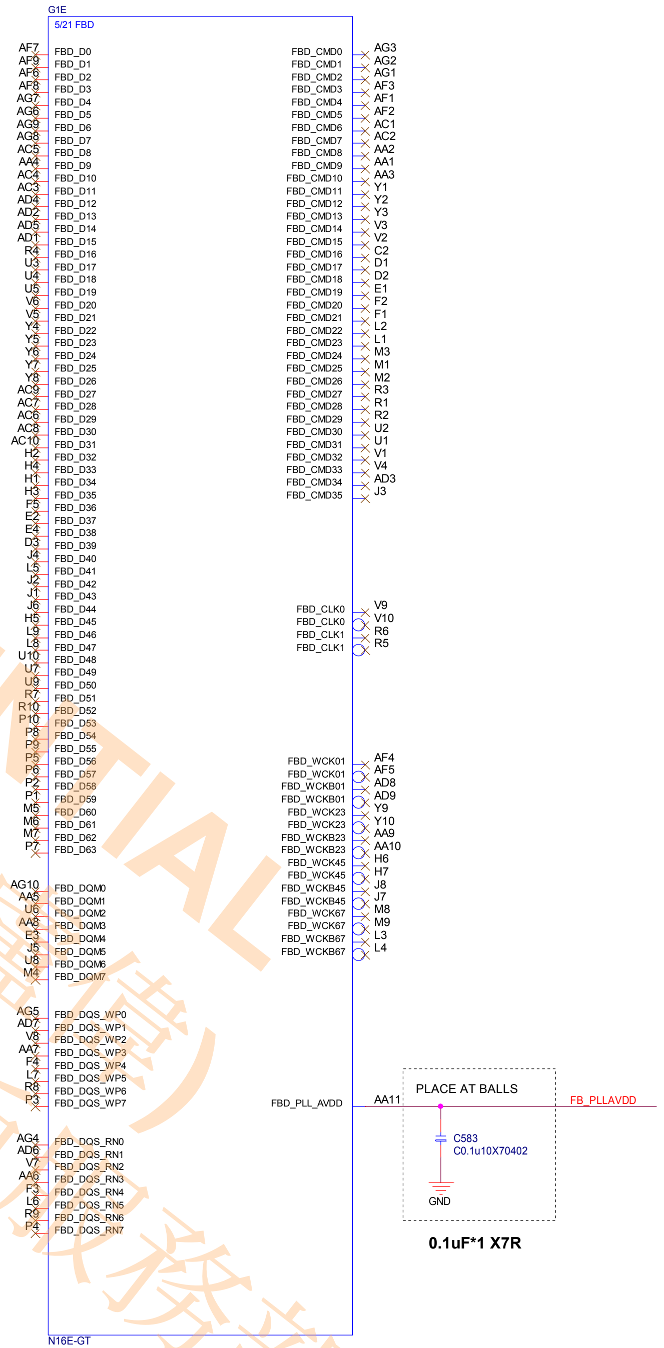
GDDR5 Mode F Mapping By GB3-256

	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*



0.1uF*1 X7R

22uF*1 X5R



0.1uF*1 X7R

MICRO-STAR INT'L CO.,LTD.

Title	DGPU_MEM IF C/D	
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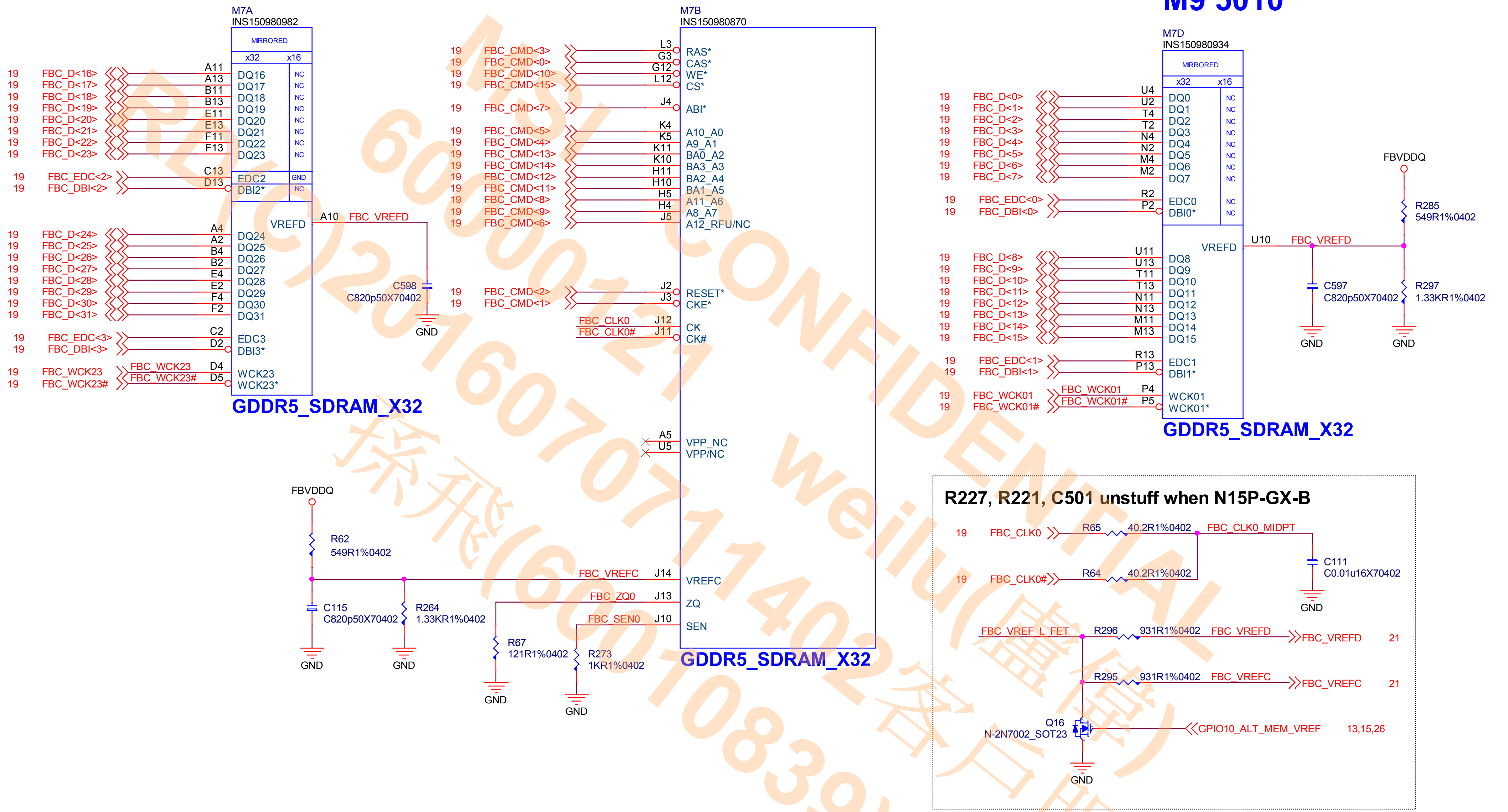
DGPU_GDDR5 FrameBuffer C0

M9 5010



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FrameBuffer C
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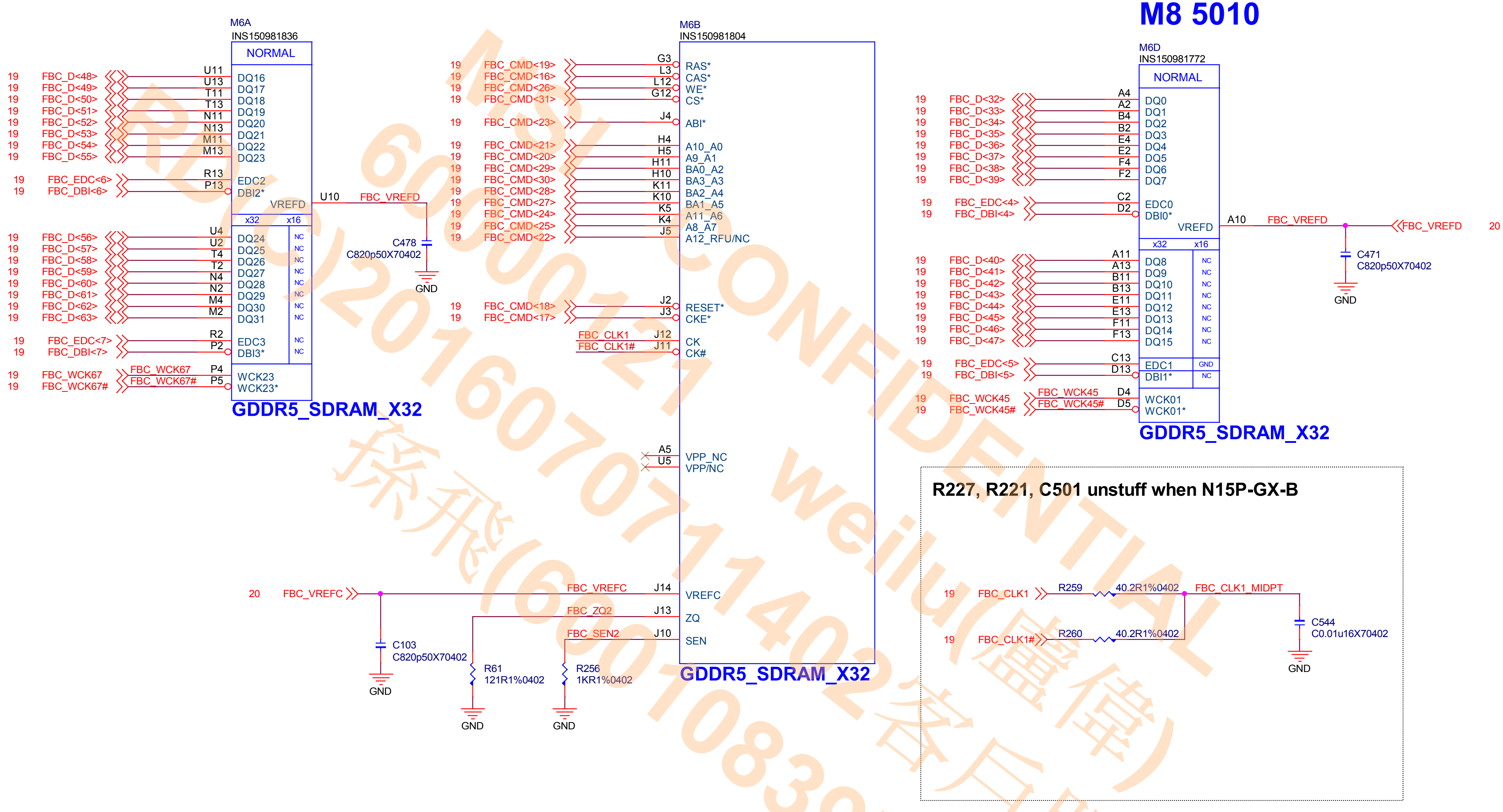
DGPU_GDDR5 FrameBuffer C1

M8 5010



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FrameBuffer C	
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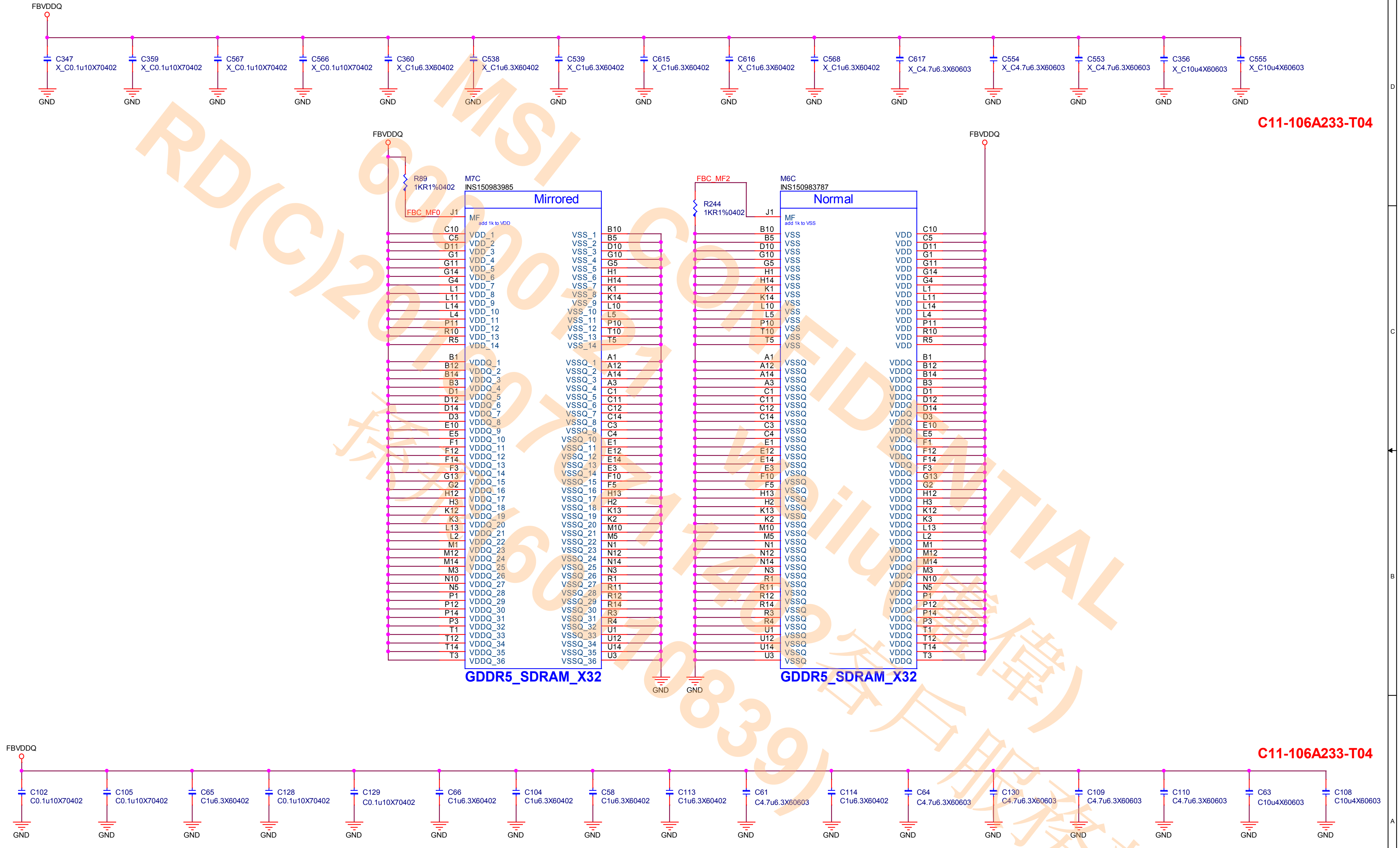
Frame Buffer Partition C Decoupling



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FB-C_DECOUPLING
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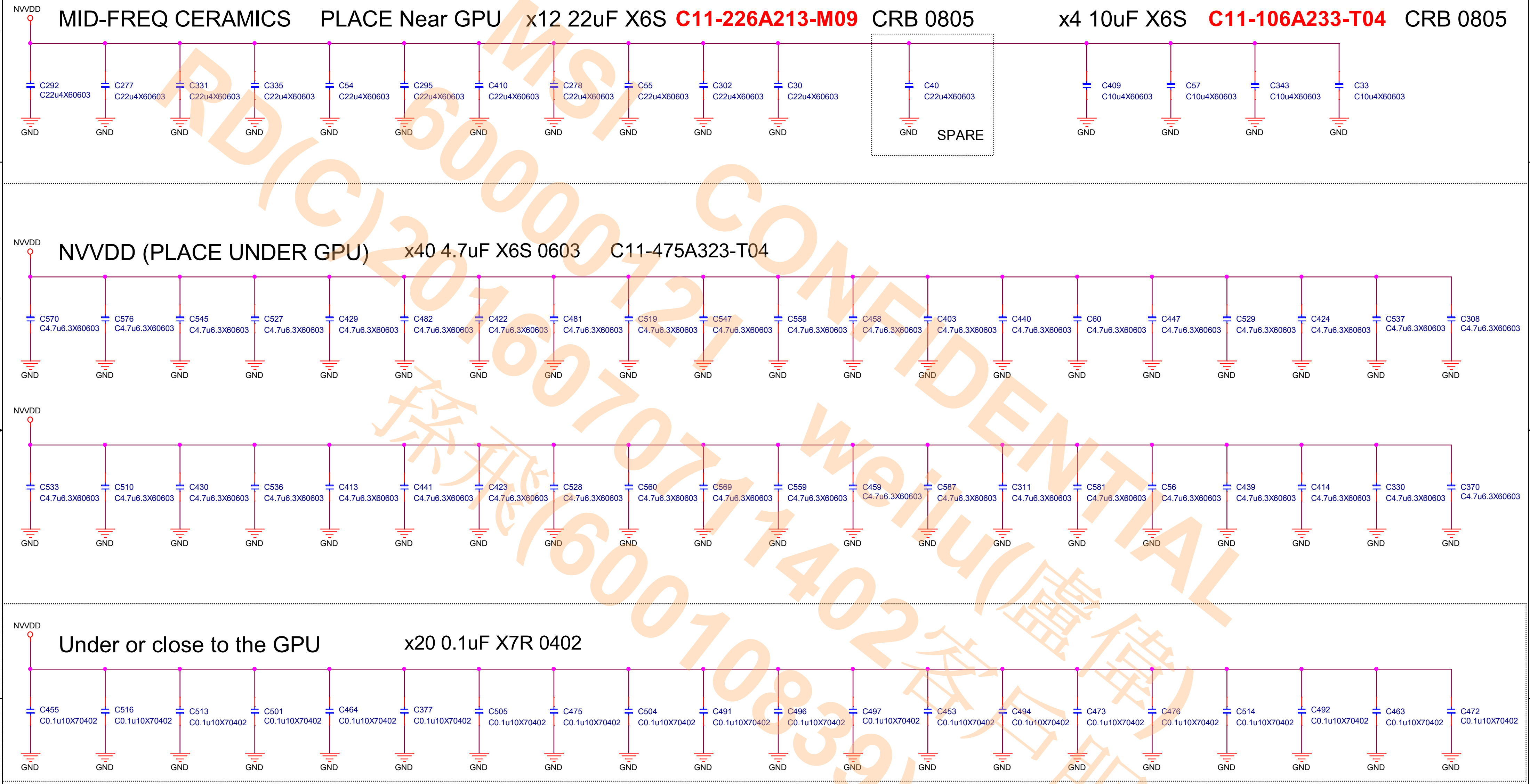
GPU DECOUPLING A



MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GPU DECOUPLING A

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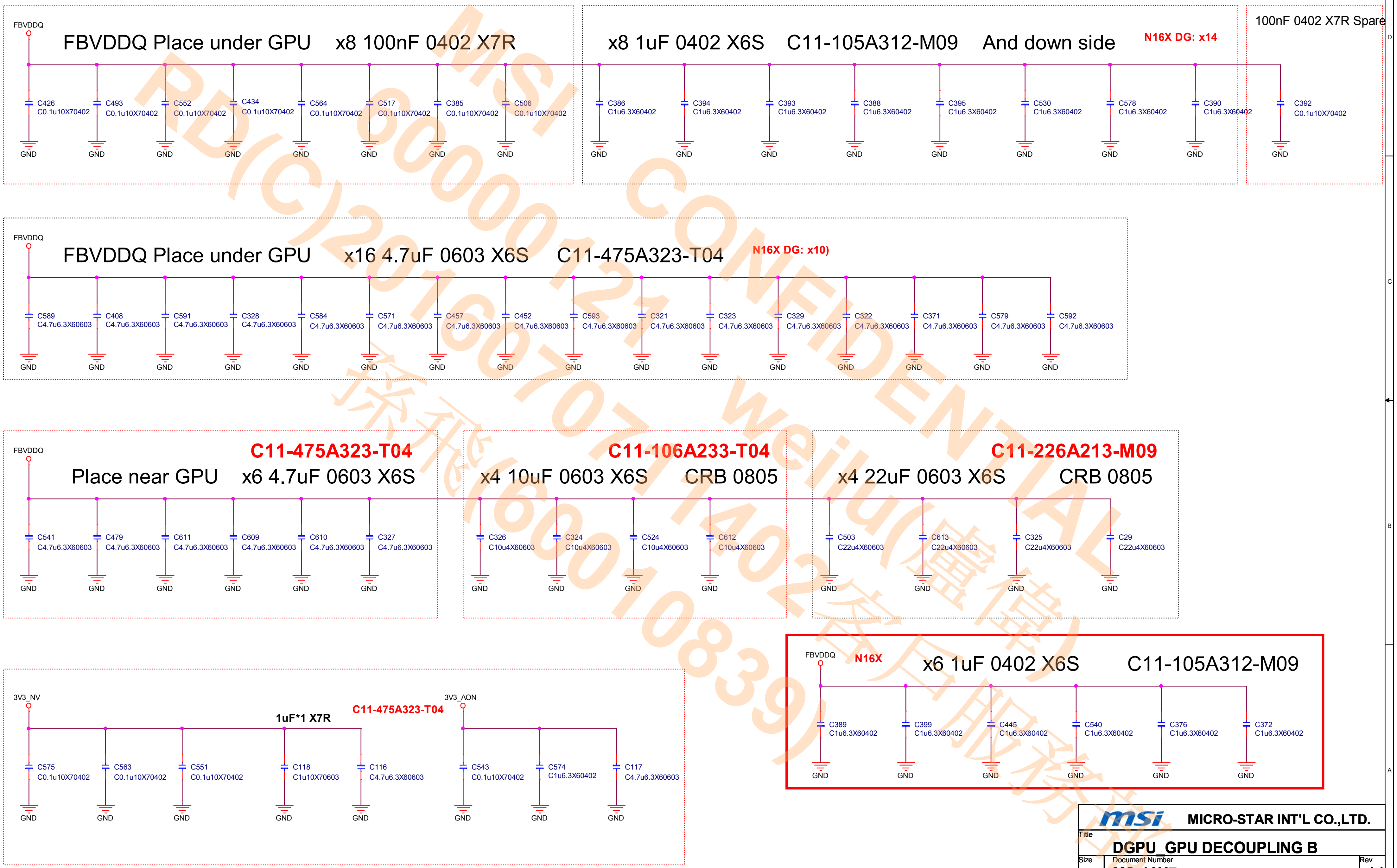
GPU DECOUPLING B



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GPU DECOUPLING B
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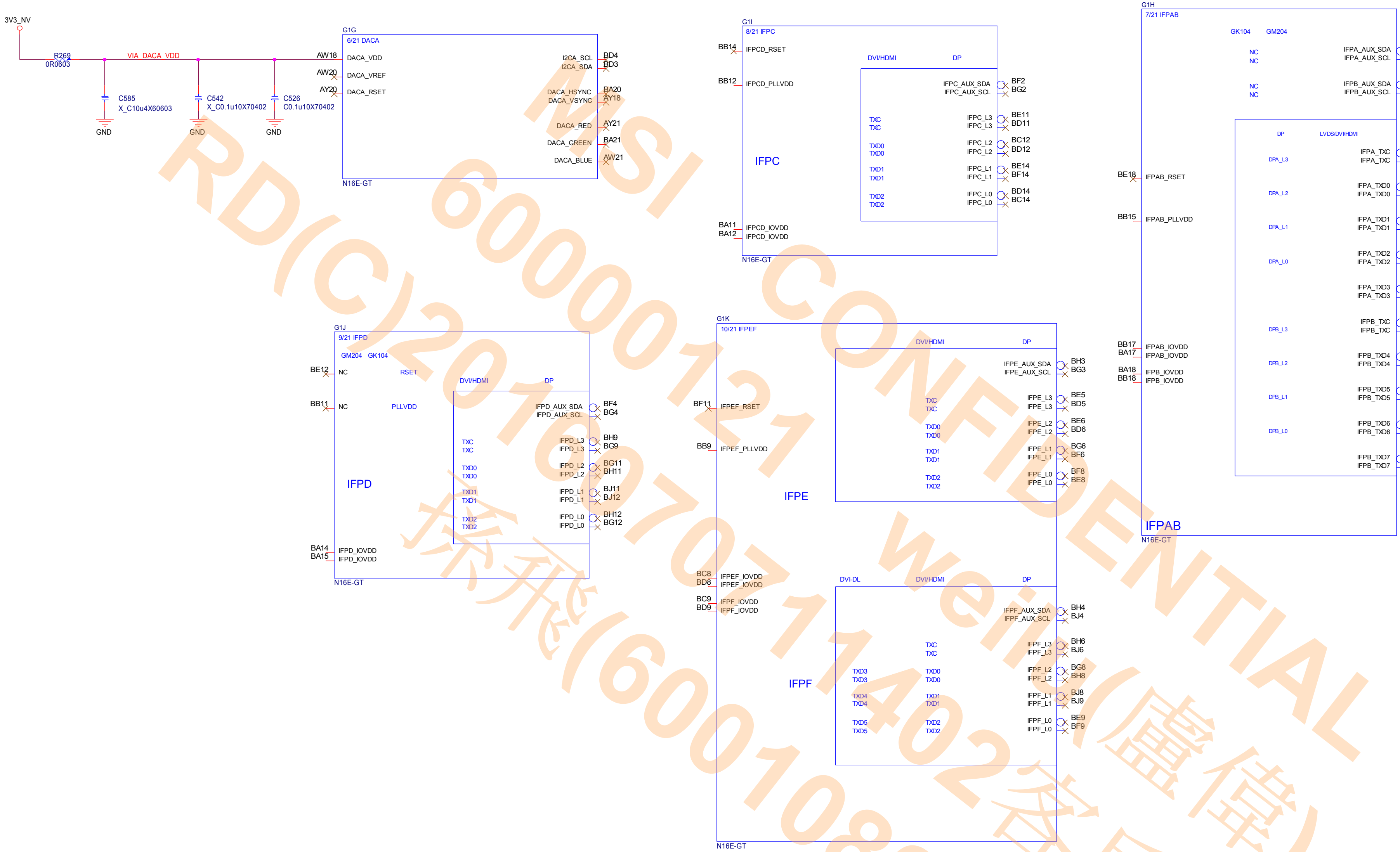
DACA,Display IF



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_DACA,Display IF	
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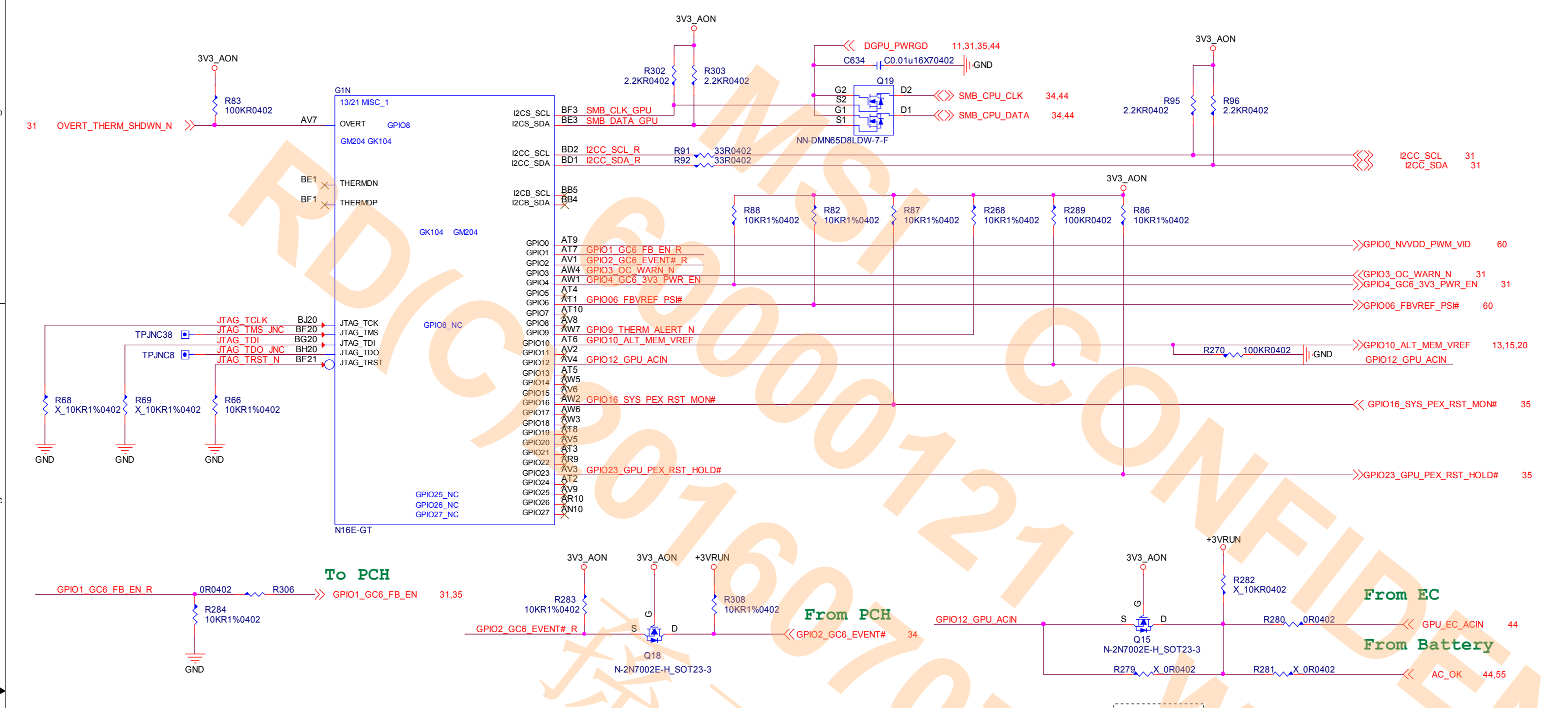
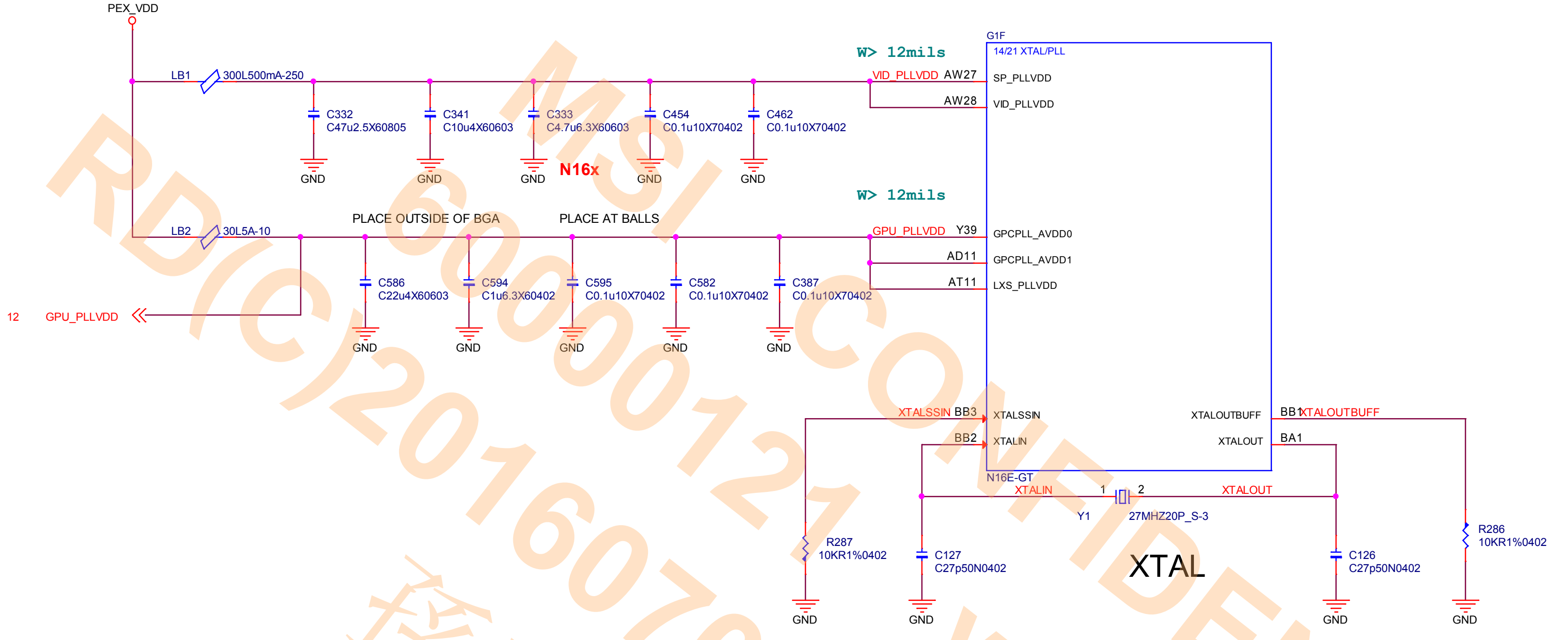
DGPU GPIO, I2C

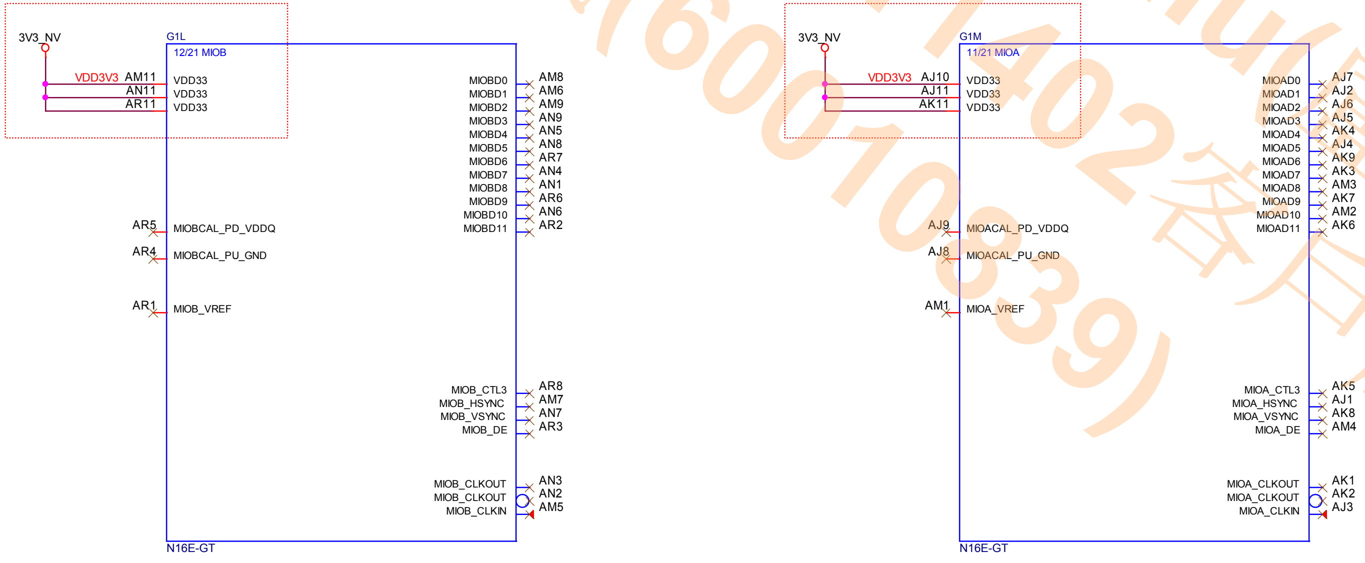


Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	PWR_VID	O	GPU Core VDD PWM control signal	
GPIO1	GC6_FB_EN	O	FB Enable for GC6 2.0	10K pull-down
GPIO2	GPU_EVENT#	I	GPU wake signal for GC6 2.0	10K pull-up to 3V3 _AON
GPIO3	OC_WARN	I	Over current throttling	10K pull-up to 3V3 _AON
GPIO4	3V3_MAIN_EN	O	GPU POWER Sequencing for GC6 2.0	10K pull-up to 3V3 _AON
GPIO5	RESERVED			
GPIO6	PSI	O	Phase shedding	
GPIO7	LCD_BL_PWM	O	Panel Backlight PWM Brighteness Control	100K pull-down
GPIO8	HPD_F	I	Hot Plug Detect for IFPDF	
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	10K pull-up to 3V3 _AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 3V3 _AON
GPIO13	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO14	HPD_A	I	Hot Plug Detect for IFPAB	
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	
GPIO16	SYS_PEX_RST_MON#	I	System side PCI reset Monitor	10K pull-up to 3V3 _AON
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	
GPIO19	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO20	RESERVED			
GPIO21	SLI_RASTER_SYNC	I	SLI Raster Sync	100K pull-down
GPIO22	SLI_SWAP_DRY	I	SLI Swap Ready	1K pull-up to 3V3 _AON
GPIO23	GPU_PEX_RST_HOLD	O	GPU PCIE self-reset control	10K pull-up to 3V3 _AON
GPIO24	MEM_VDD_CTL	O	Memory VDD VID	
GPIO25	RESERVED			
GPIO26	RESERVED			
GPIO27	HPD_B	I	Hot Plug Detect for IFPB	
OVERT	OVERT(OVERT#)	I/O	Catastrophic Over Temperature	100K pull-up to 3V3 _AON

DGPU MIO & XTAL



Multi-use IO(MIO) Interface



MICRO-STAR INT'L CO.,LTD.		
Title: DGPU MIO & XTAL		
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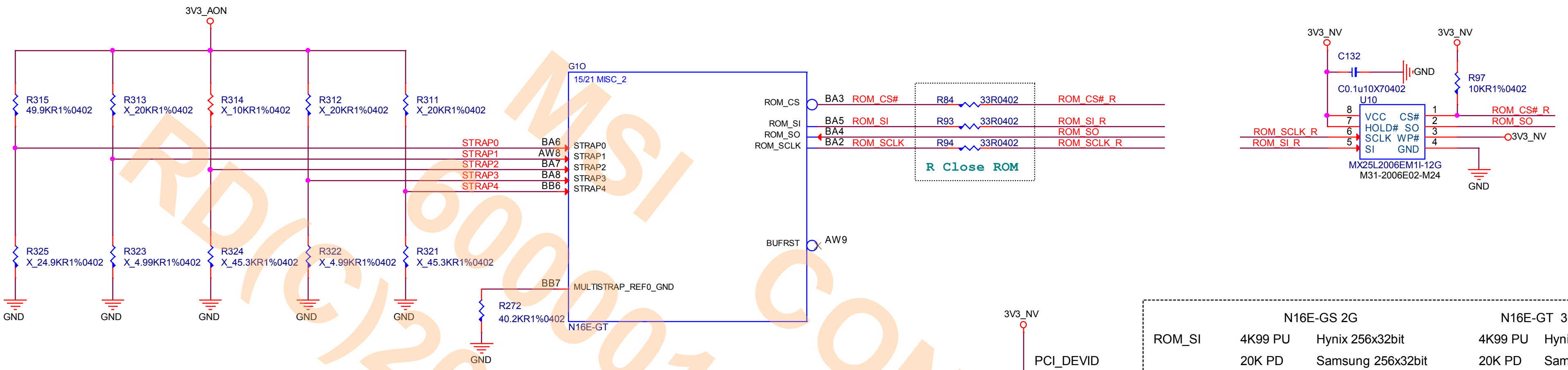
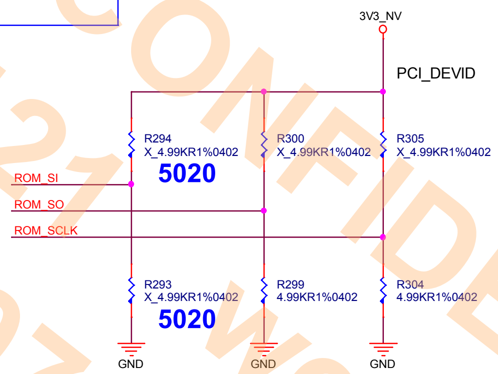
ROM, MULTI-LEVEL STRAPS





	N16E-GS 2G		N16E-GT 3G	
ROM_SI	4K99 PU	Hynix 256x32bit	4K99 PU	Hynix 256x32bit
	20K PD	Samsung 256x32bit	20K PD	Samsung 256x32bit
	24R9 PD	Micron 256x32bit	24R9 PD	Micron 256x32bit
ROM_SO	5K PD		5K PD	
ROM_SCLK	5K PD		5K PD	
STRAP0	50K PU 3V3_AON		50K PU 3V3_AON	
STRAP1	Reserved		Reserved	
STRAP2	Reserved		Reserved	
STRAP3	Reserved		Reserved	
STRAP4	Reserved		Reserved	

3G/2G

PU4K99 **Hynix** **256Mx32bit**	V_TOP1 **5010**
R11-4991T12-W08	M12-5GC4H65-H23
X_4.99KR1%0402	X_H5GC4H24AJR-T2C
PD20K **Samsung** **256Mx32bit**	V_TOP2 **5010**
R11-0203T12-W08	M12-4132525-S02
X_20KR1%0402	X_K4G41325FC-HC03
PD24R9 **Micron** **256Mx32bit**	V_TOP3 **5010**
R11-249AT12-W08	M12-4032B05-E59
X_24.9R1%0402	X_EDW4032BABG-60-F

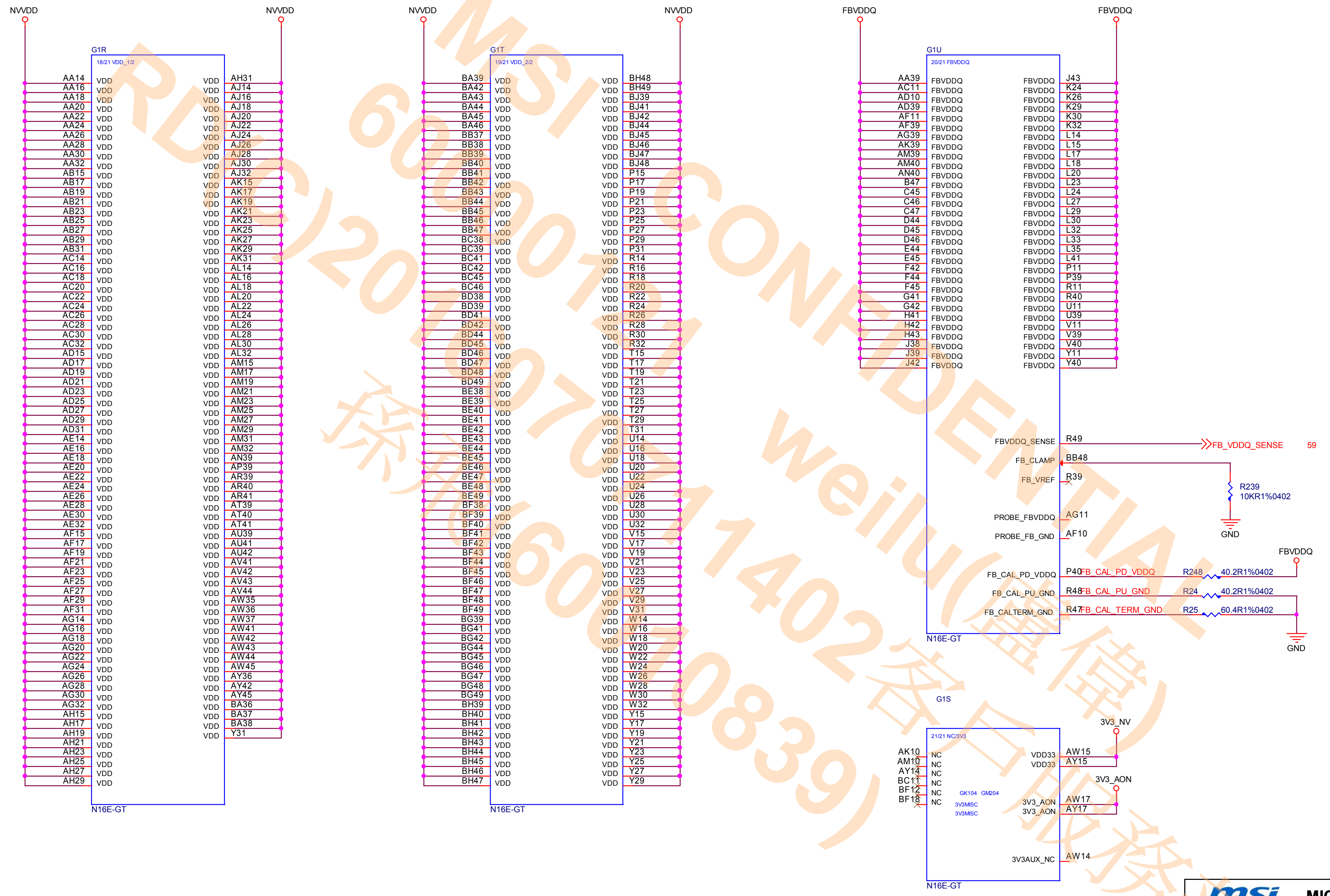
GDDR5 Parts
5010 : M2 , M3 , M4 , M5 , M6 , M7

N16E_GS N16E_GS **B03-N16EG05-N08** N16E-GS-KCD-A1

N16E_GT N16E_GT **B03-0N16E25-N08** N16E-GT-A1

MICRO-STAR INT'L CO.,LTD.
Title: DGPU_ROM,HW Straps
Size | Document Number: MS-16H7 | Rev 1.1
Date: Wednesday, July 08, 2015 | Sheet 28 of 74

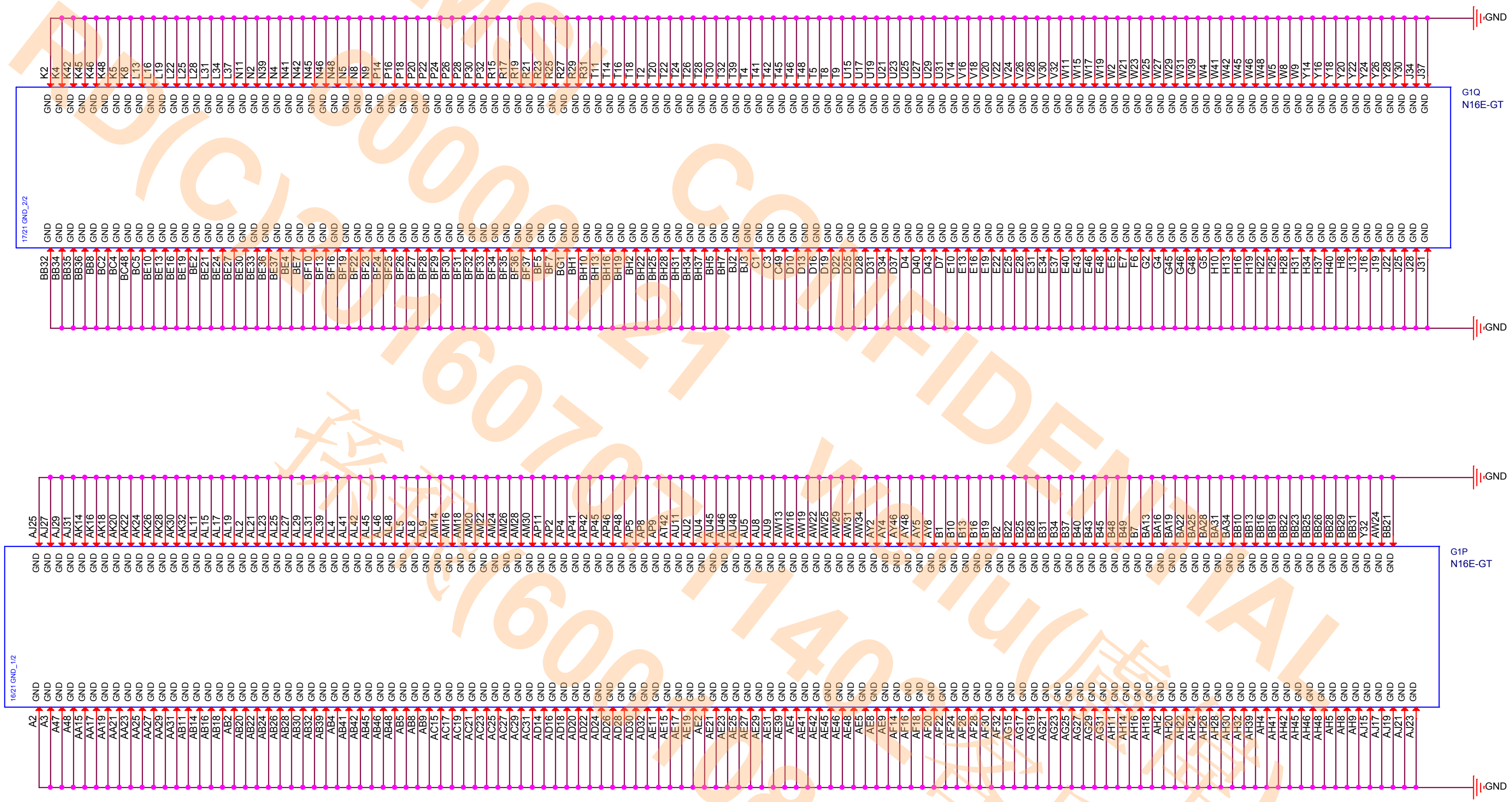
GPU NVVDD, FBVDDQ



MSI MICRO-STAR INT'L CO.,LTD.

Title	DGPU NVVDD, FBVDDQ	
Size	Document Number: MS-16H7	Rev 1.1
Date: Wednesday, July 08, 2015	Sheet 29 of 74	

DGPU GND



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Title	DGPU GND
Size	
Document Number	MS-16H7
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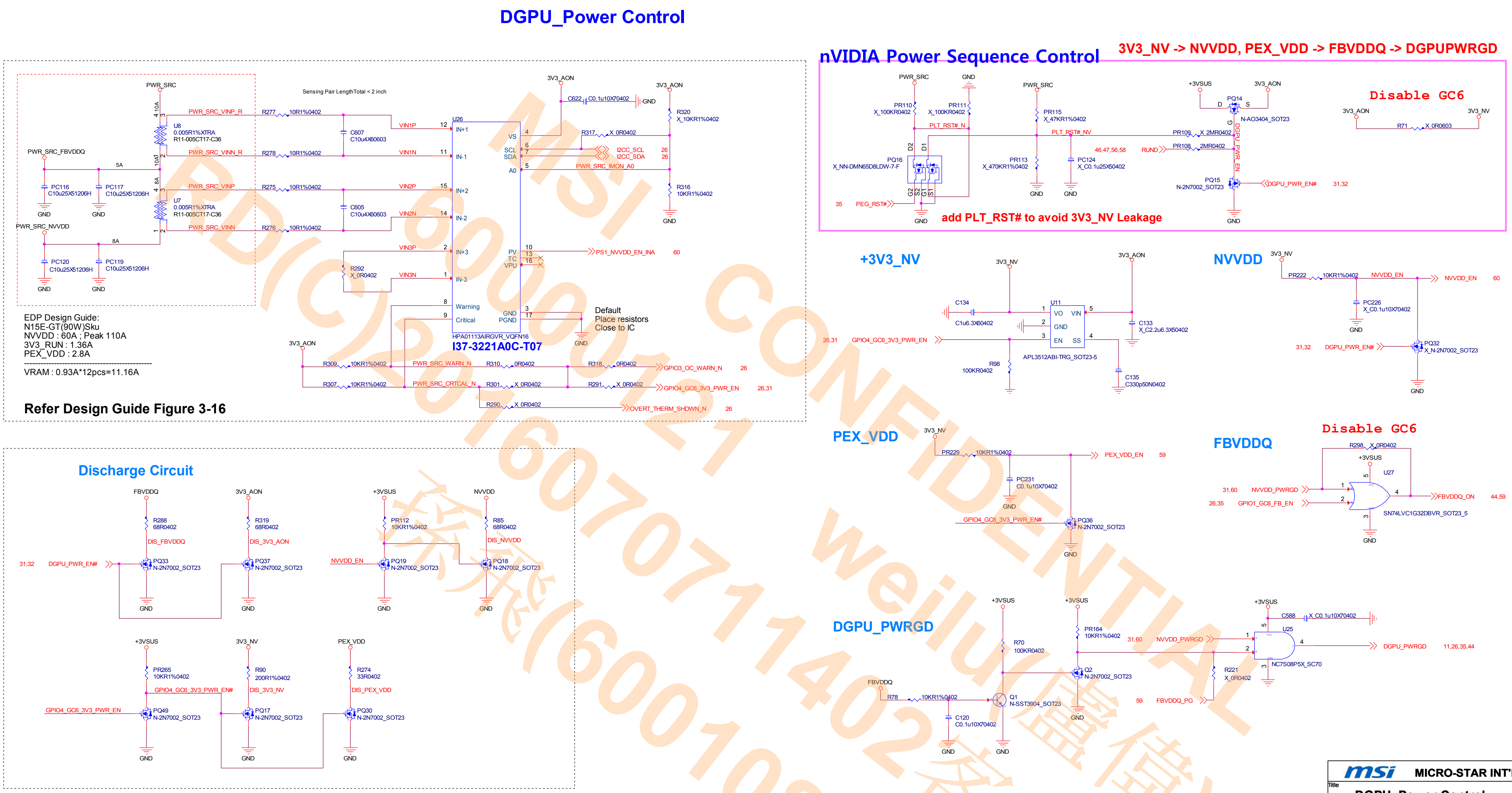
Date:	Wednesday, July 08, 2015
Sheet	30 of 74


DGPU_Power Control
nVIDIA Power Sequence Control
3V3_NV -> NVVDD, PEX_VDD -> FBVDDQ -> DGPUPWRGD
Disable GC6
add PLT_RST# to avoid 3V3_NV Leakage
EDP Design Guide:
N15E-GT(90W)Sku
NVVDD : 60A ; Peak 110A
3V3_RUN : 1.36A
PEX_VDD : 2.8A
VRAM : 0.93A*12pcs=11.16A
Refer Design Guide Figure 3-16
Sensing Pair LengthTotal < 2 inch
Default
Place resistors
Close to IC
I37-3221A0C-T07
HPA01113AIRGVR_VQFN16
+3V3_NV
NVVDD
PEX_VDD
FBVDDQ
Disable GC6
DGPU_PWRGD
Discharge Circuit
APL3512ABI-TRG_SOT23-5
SN74LVC1G32DBVR_SOT23_5
NC7SO8P5X_SC70

MICRO-STAR INT'L CO.,LTD.

Title: DGPU_Power Control

Size | Document Number: MS-16H7 | Rev: 1.1

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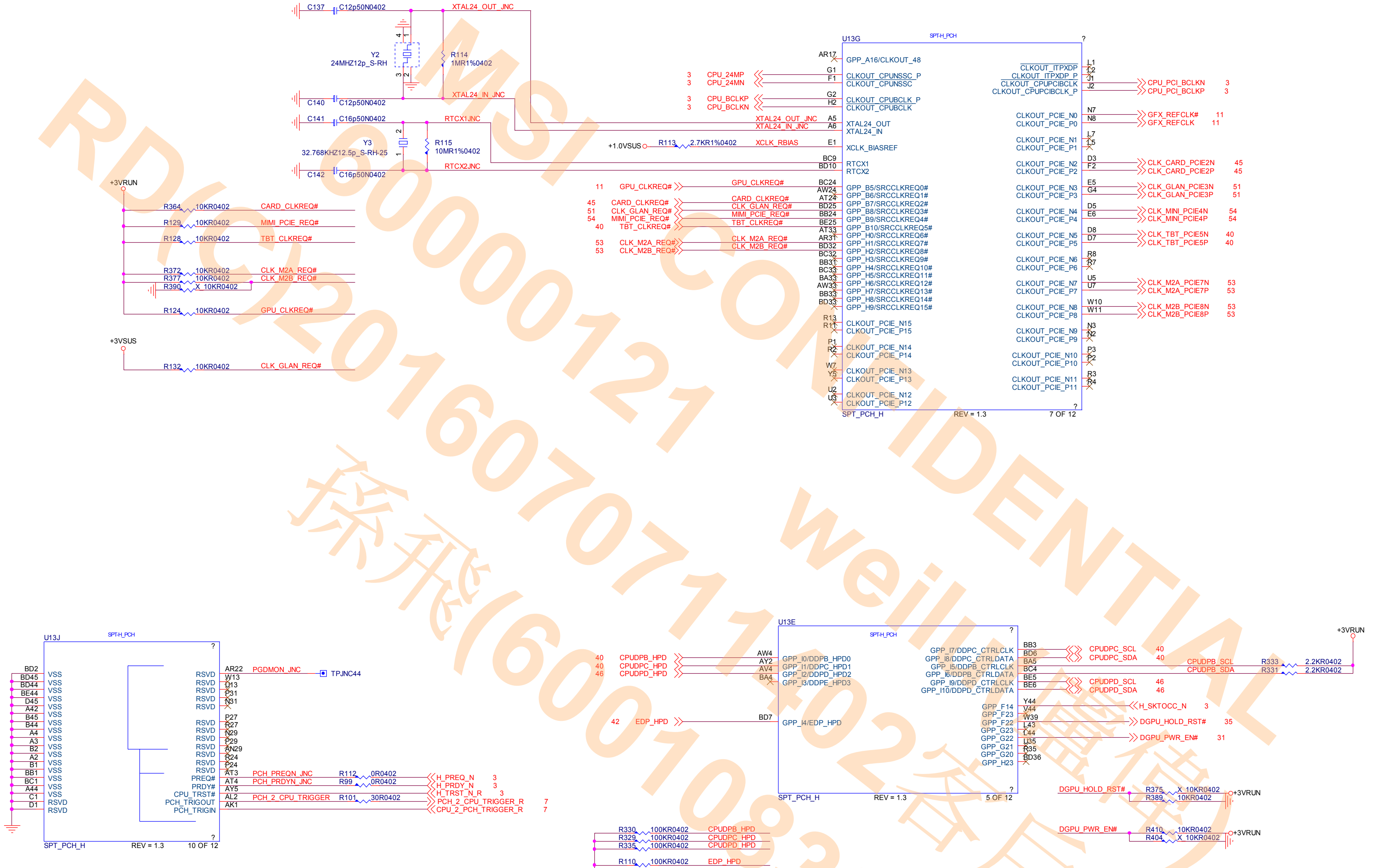


Signal	GPIO Assignment
DGPU_PWR_EN#	GPP_G22
DGPU_PWROK	NA
DGPU_HOLD_RST#	GPP_F22

HM170 HM170 B01-HM17005-I06 HM170

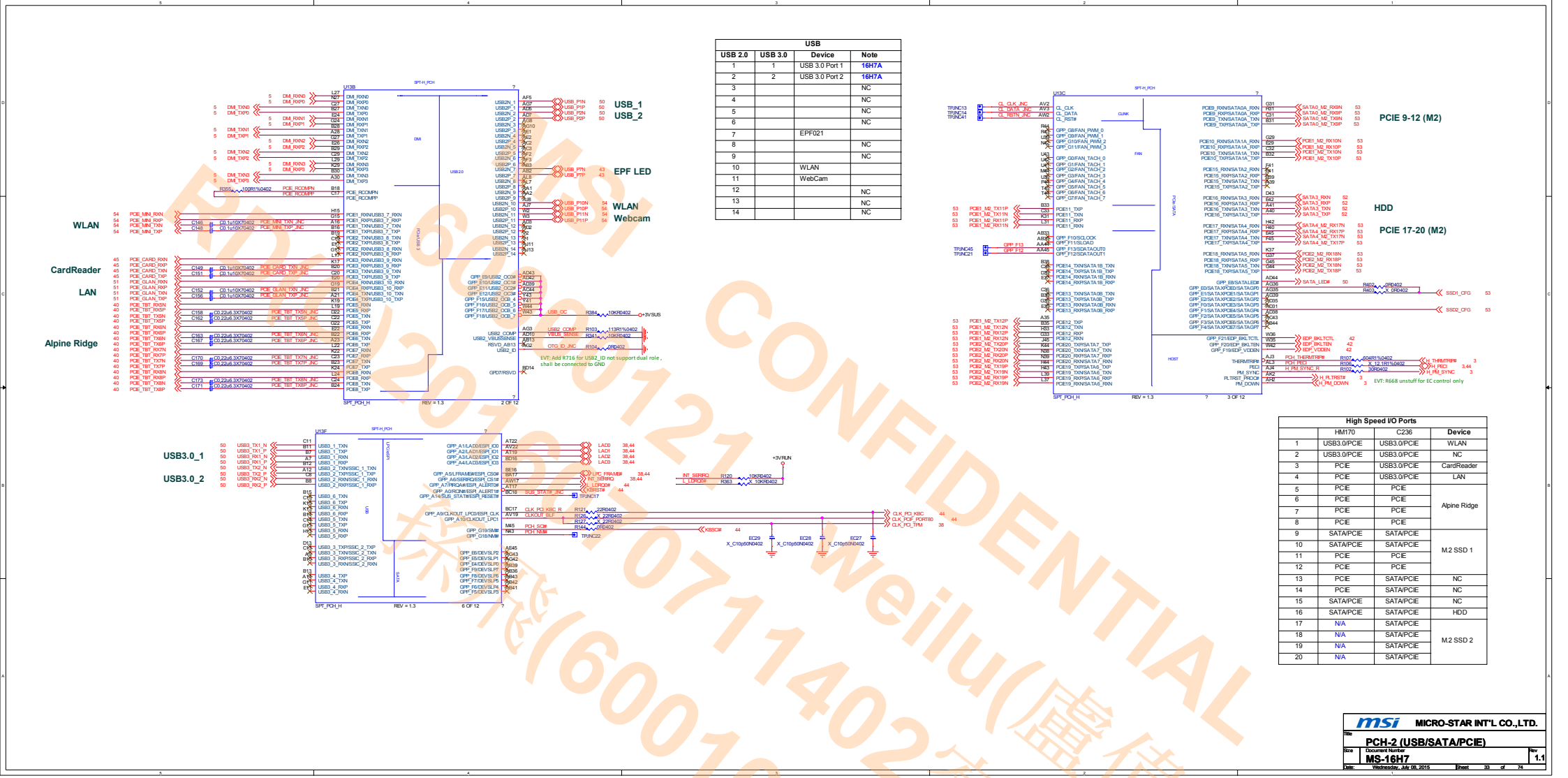
CM236 CM236 B01-CM23605-I06 CM236

MICRO-STAR INT'L CO.,LTD.

Title: PCH-1 (CLK/DDI)

Size | Document Number: MS-16H7 | Rev: 1.1

Date: Thursday, July 09, 2015 | Sheet 32 of 74


USB
USB 2.0 | USB 3.0 | Device | Note
1 | 1 | USB 3.0 Port 1 | 16H7A
2 | 2 | USB 3.0 Port 2 | 16H7A
3 | | | NC
4 | | | NC
5 | | | NC
6 | | | NC
7 | | EPF021 |
8 | | | NC
9 | | | NC
10 | | WLAN |
11 | | WebCam |
12 | | | NC
13 | | | NC
14 | | | NC
USB_1
USB_2
EPF LED
WLAN
Webcam
PCIE 9-12 (M2)
HDD
PCIE 17-20 (M2)
WLAN
CardReader
LAN
Alpine Ridge
USB3.0_1
USB3.0_2
High Speed I/O Ports
HM170 | C236 | Device
1 | USB3.0/PCIE | USB3.0/PCIE | WLAN
2 | USB3.0/PCIE | USB3.0/PCIE | NC
3 | PCIE | USB3.0/PCIE | CardReader
4 | PCIE | USB3.0/PCIE | LAN
5 | PCIE | PCIE | Alpine Ridge
6 | PCIE | PCIE |
7 | PCIE | PCIE |
8 | PCIE | PCIE |
9 | SATA/PCIE | SATA/PCIE | M.2 SSD 1
10 | SATA/PCIE | SATA/PCIE |
11 | PCIE | PCIE |
12 | PCIE | PCIE |
13 | PCIE | SATA/PCIE | NC
14 | PCIE | SATA/PCIE | NC
15 | SATA/PCIE | SATA/PCIE | NC
16 | SATA/PCIE | SATA/PCIE | HDD
17 | N/A | SATA/PCIE | M.2 SSD 2
18 | N/A | SATA/PCIE |
19 | N/A | SATA/PCIE |
20 | N/A | SATA/PCIE |
MICRO-STAR INT'L CO.,LTD.
PCH-2 (USB/SATA/PCIE)
MS-16H7
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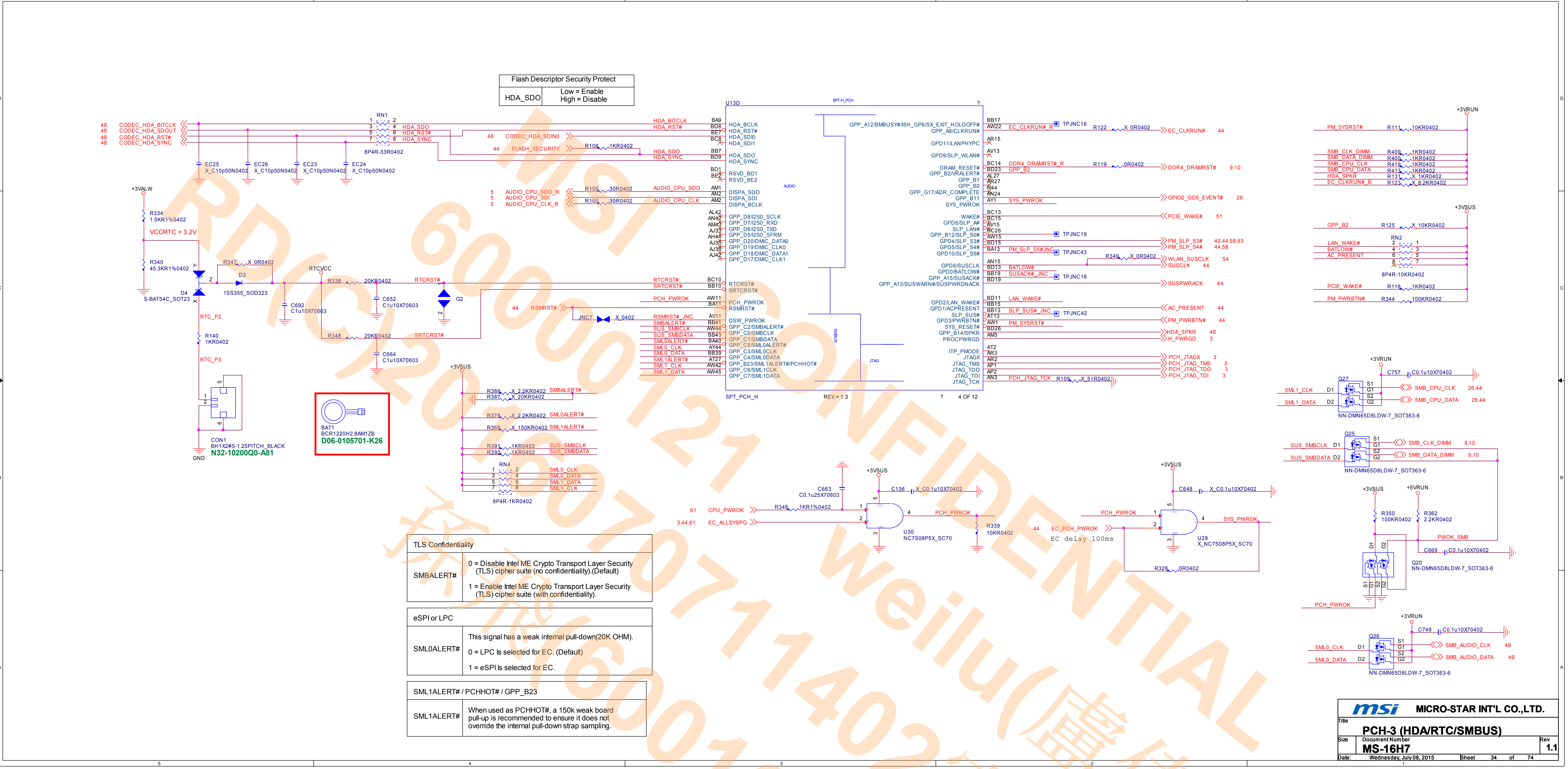

TLS Confidentiality

SMBALERT#	0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).(Default) 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).

eSPI or LPC

SML0ALERT#	This signal has a weak internal pull-down(20K OHM). 0 = LPC is selected for EC. (Default) 1 = eSPI is selected for EC.

SML1ALERT# / PCHHOT# / GPP_B23

SML1ALERT#	When used as PCHHOT#, a 150k weak board pull-up is recommended to ensure it does not override the internal pull-down strap sampling.

msi MICRO-STAR INT'L CO.,LTD.

Title	PCH-3 (HDA/RTC/SMBUS)
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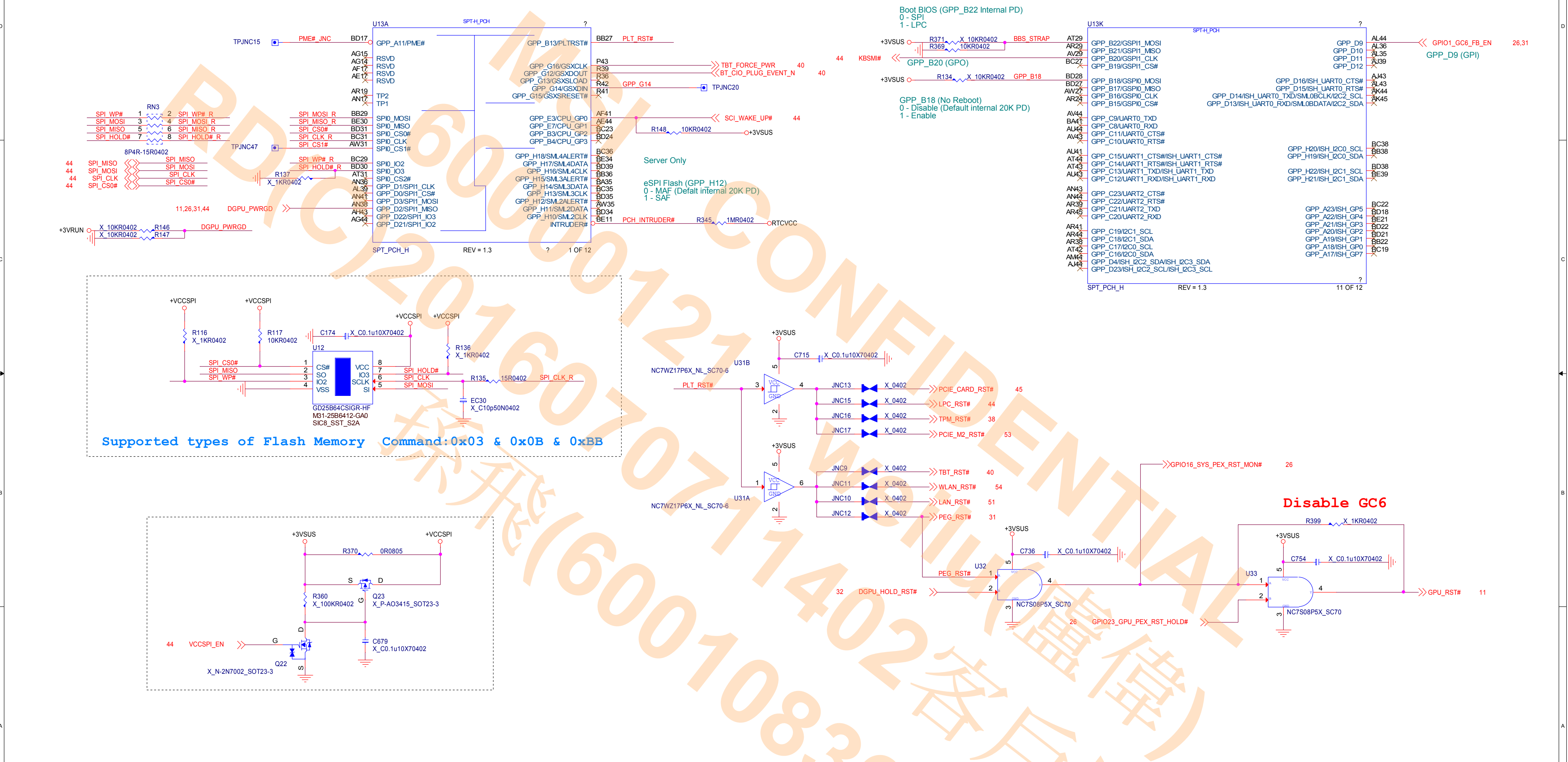
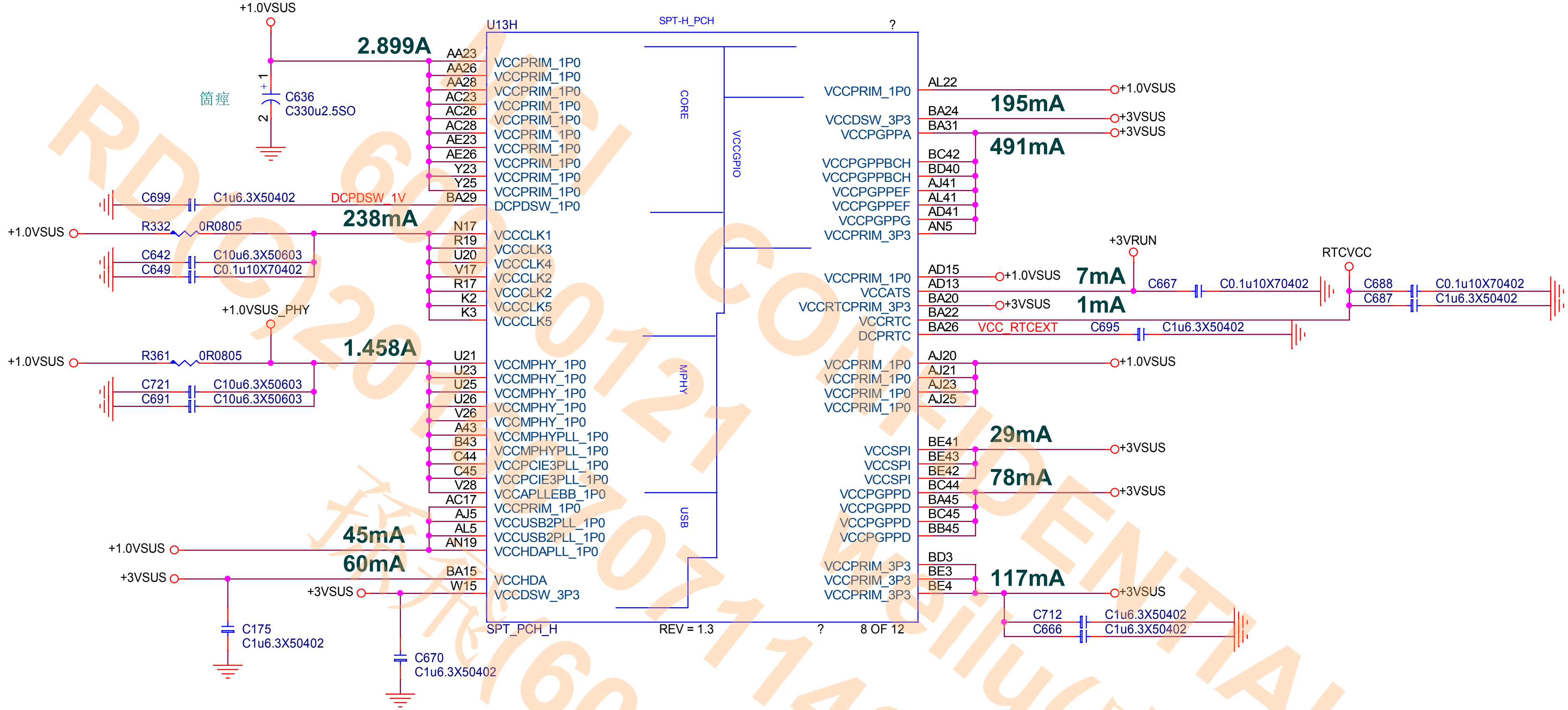


MICRO-STAR INT'L CO.,LTD.

Title: PCH-4 (SPI/GPIO)

Size | Document Number: MS-16H7 | Rev 1.1

Date: Wednesday, July 08, 2015 | Sheet 35 of 74



MICRO-STAR INT'L CO.,LTD.

Title

PCH-5 (Power)

Size | Document Number | Rev

MS-16H7 — 1.1

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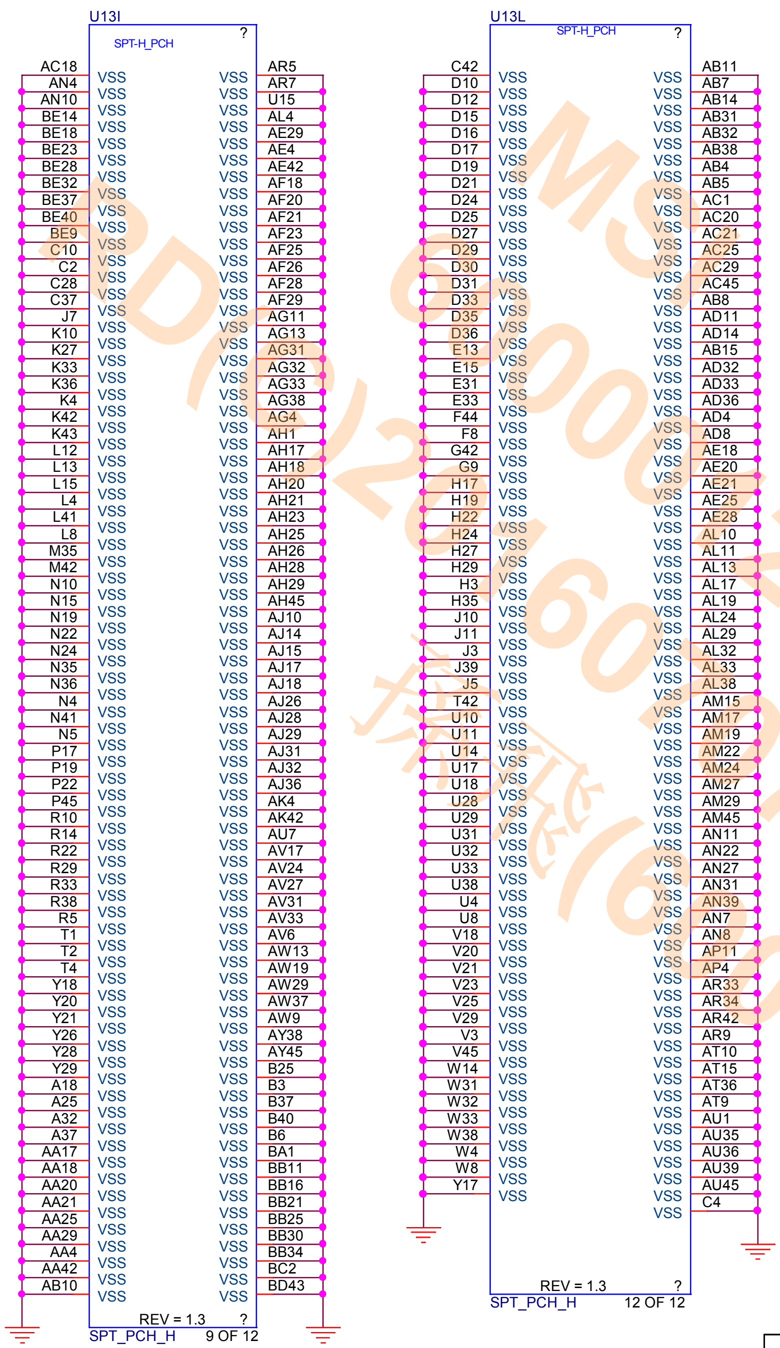

MICRO-STAR INT'L CO.,LTD.

Title: **PCH-06 (GND)**

Size	Document Number	Rev
	MS-16H7	1.1

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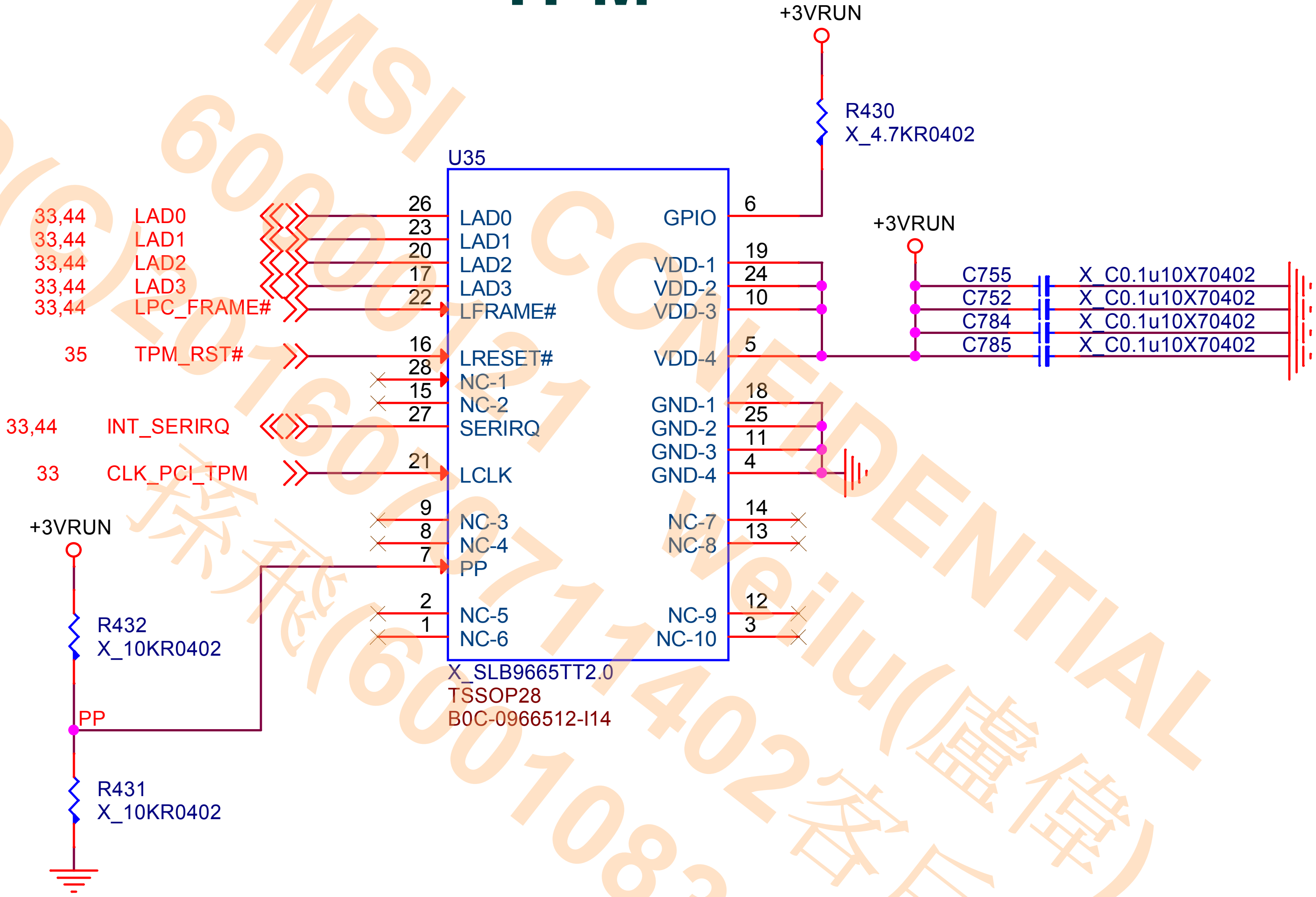
TPM



MICRO-STAR INT'L CO.,LTD.

Title: TPM		
Size	Document Number: MS-16H7	Rev: 1.1
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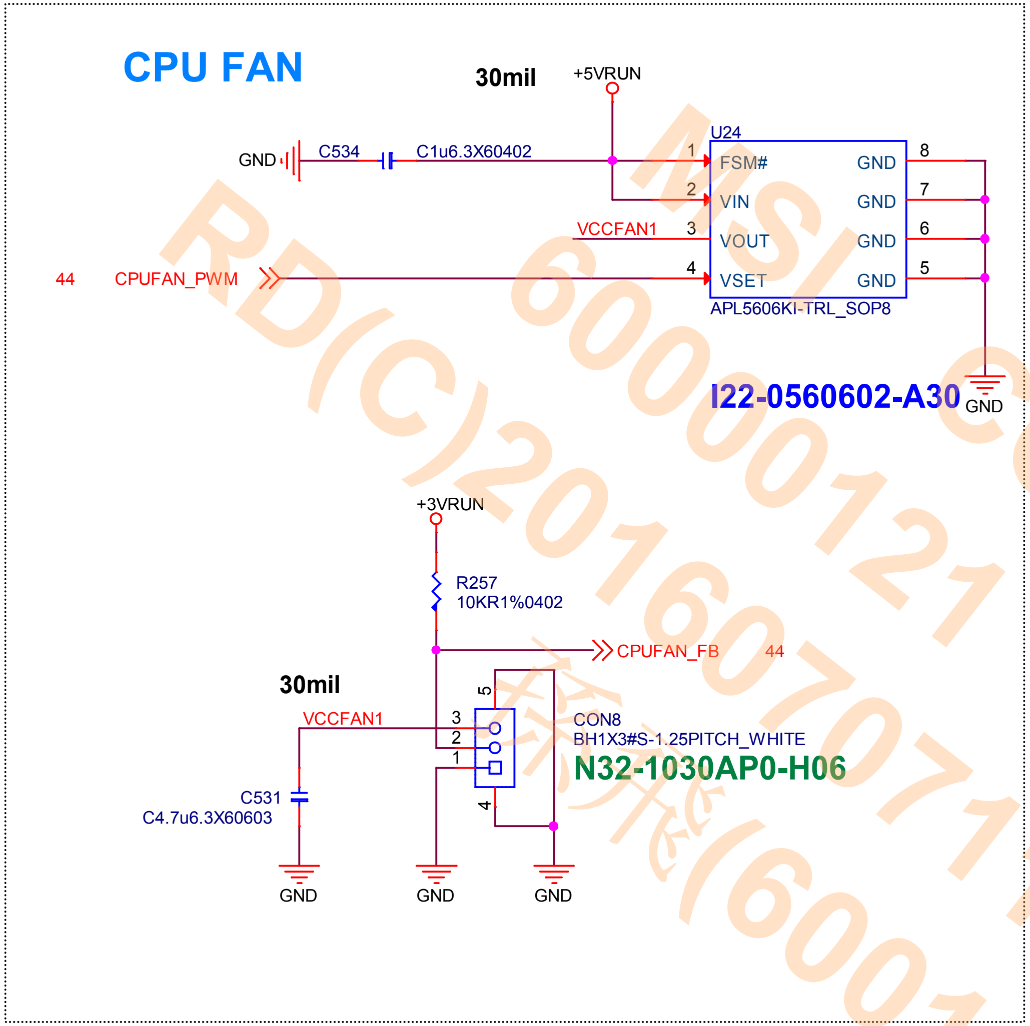

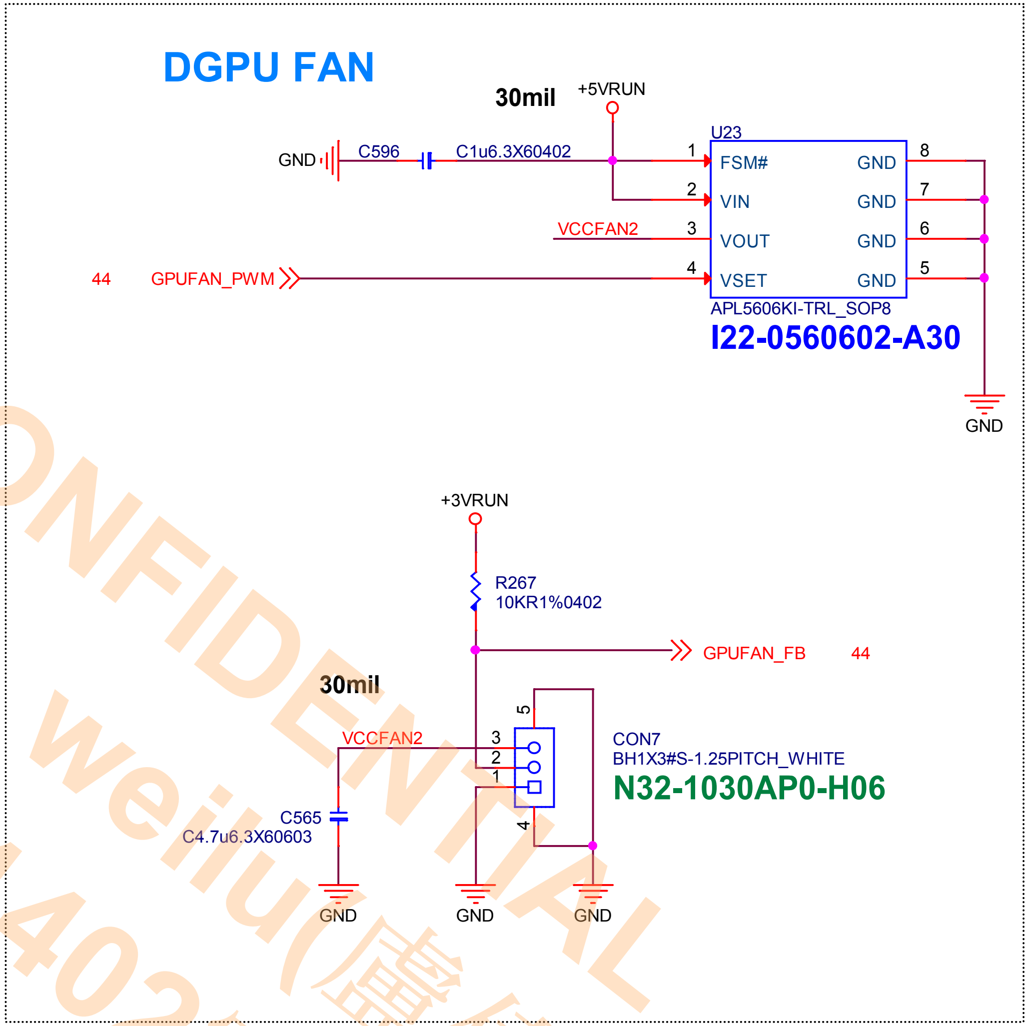

MICRO-STAR INT'L CO.,LTD.

Title: CPU FAN/DGPU FAN

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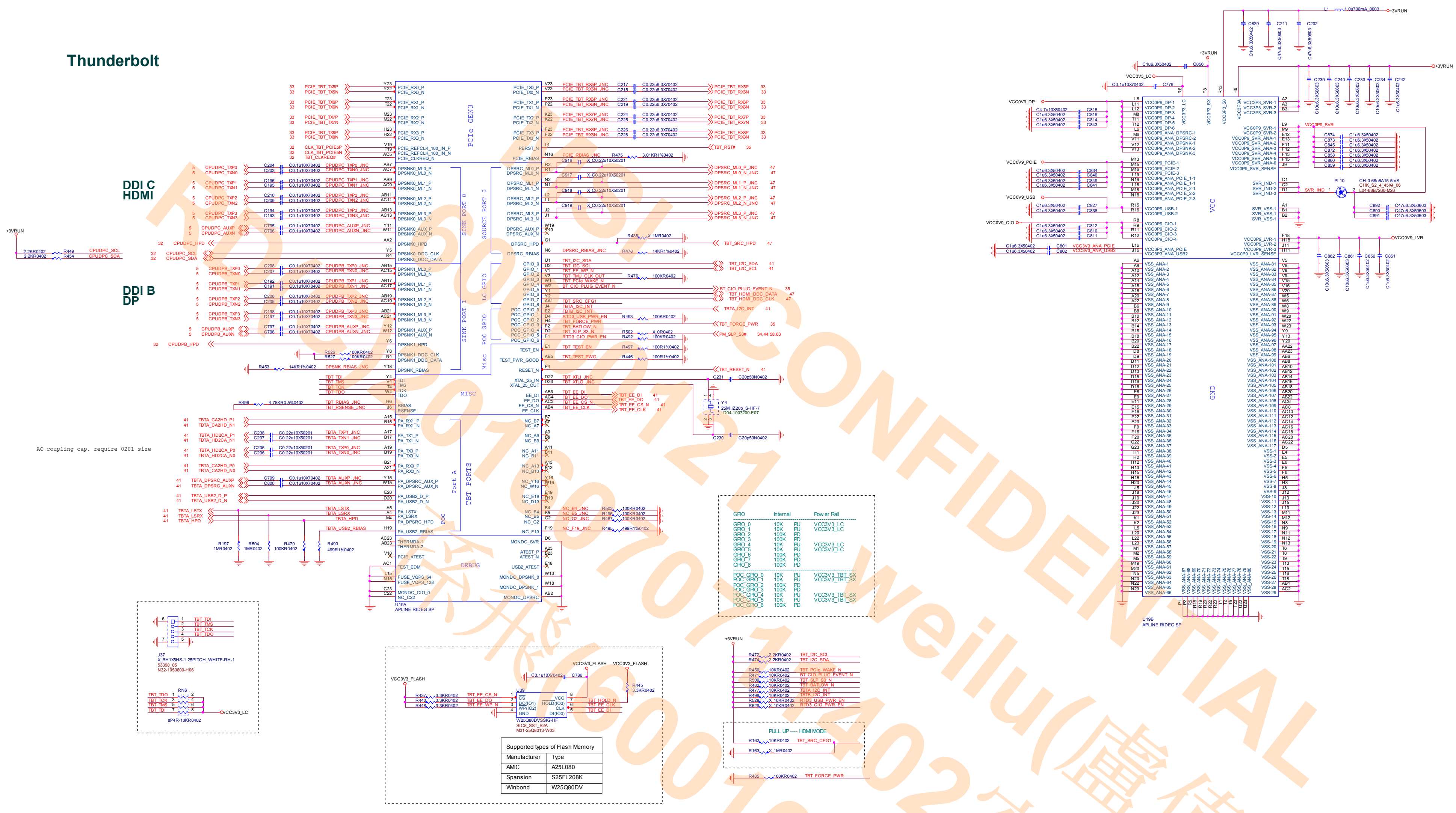
Thunderbolt



GPIO	Internal		Power Rail
GPIO_0	10K	PU	VCC3V3_LC
GPIO_1	10K	PU	VCC3V3_LC
GPIO_2	100K	PD	
GPIO_3	100K	PD	
GPIO_4	10K	PU	VCC3V3_LC
GPIO_5	10K	PU	VCC3V3_LC
GPIO_6	100K	PD	
GPIO_7	100K	PD	
GPIO_8	100K	PD	
POC_GPIO_0	10K	PU	VCC3V3_TBT_SX
POC_GPIO_1	10K	PU	VCC3V3_TBT_SX
POC_GPIO_2	100K	PD	
POC_GPIO_3	100K	PD	
POC_GPIO_4	10K	PU	VCC3V3_TBT_SX
POC_GPIO_5	10K	PU	VCC3V3_TBT_SX
POC_GPIO_6	100K	PD	

Supported types of Flash Memory

Manufacturer	Type
AMIC	A25L080
Spansion	S25FL208K
Winbond	W25Q80DV

MICRO-STAR INT'L CO.,LTD.

Title	Alpine Ridge (1)	
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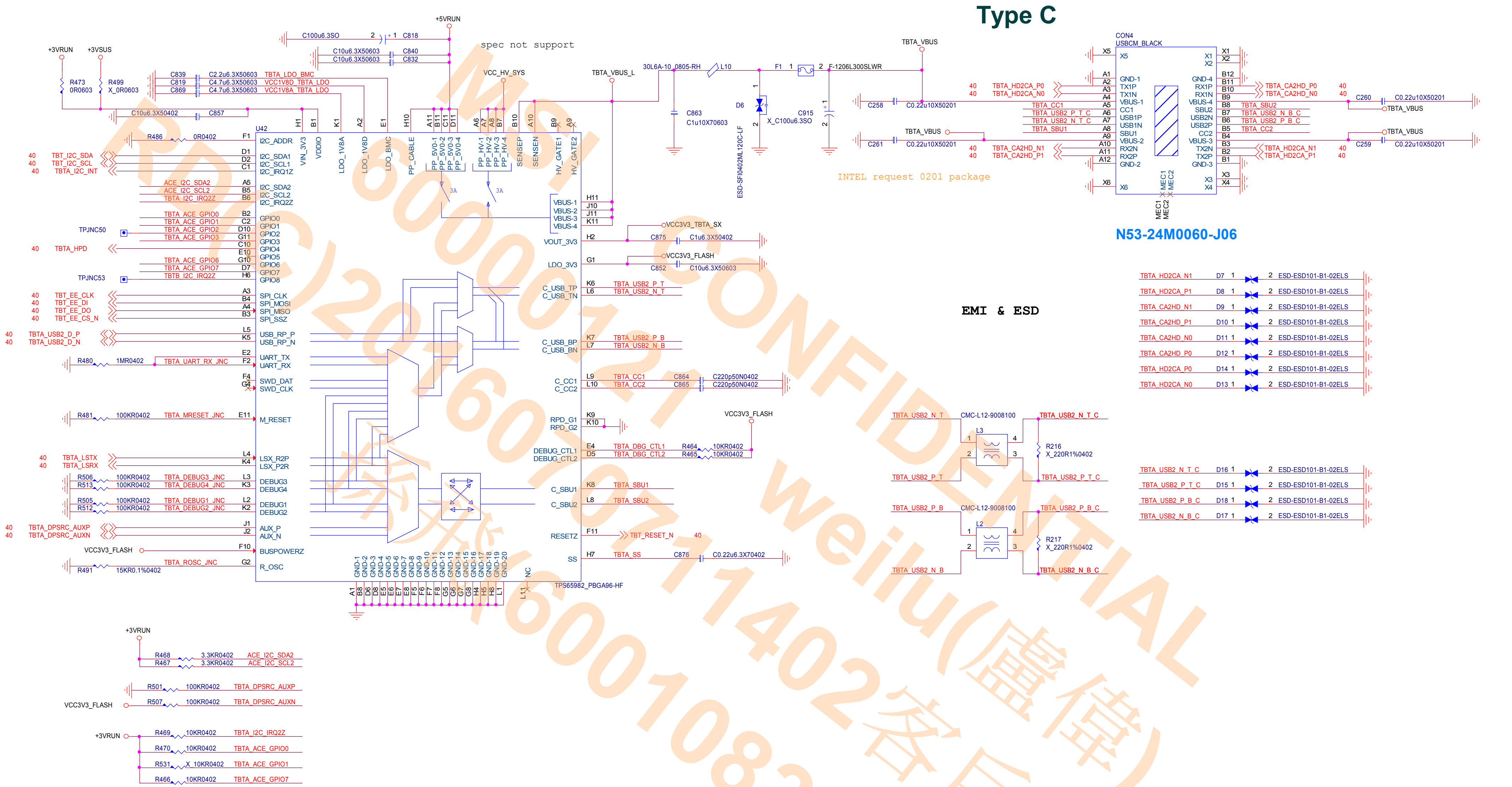
Type C



msi	MICRO-STAR INT'L CO.,LTD.	
Title	Apline Ridge (2)	
Size	Document Number: MS-16H7	Rev 1.1
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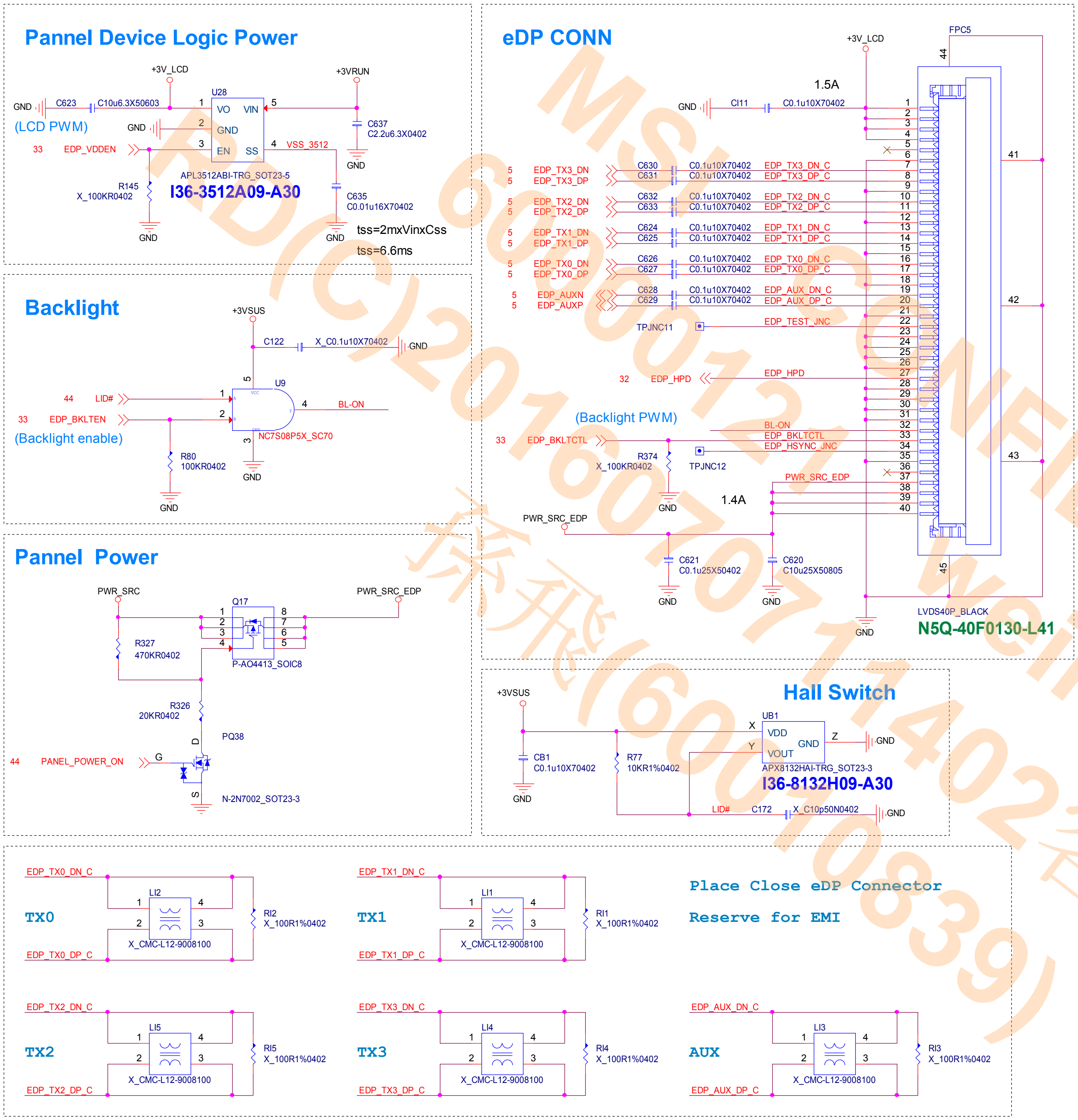
eDP Connector



LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPD	HPD signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

MICRO-STAR INT'L CO.,LTD.

Title: eDP Connector

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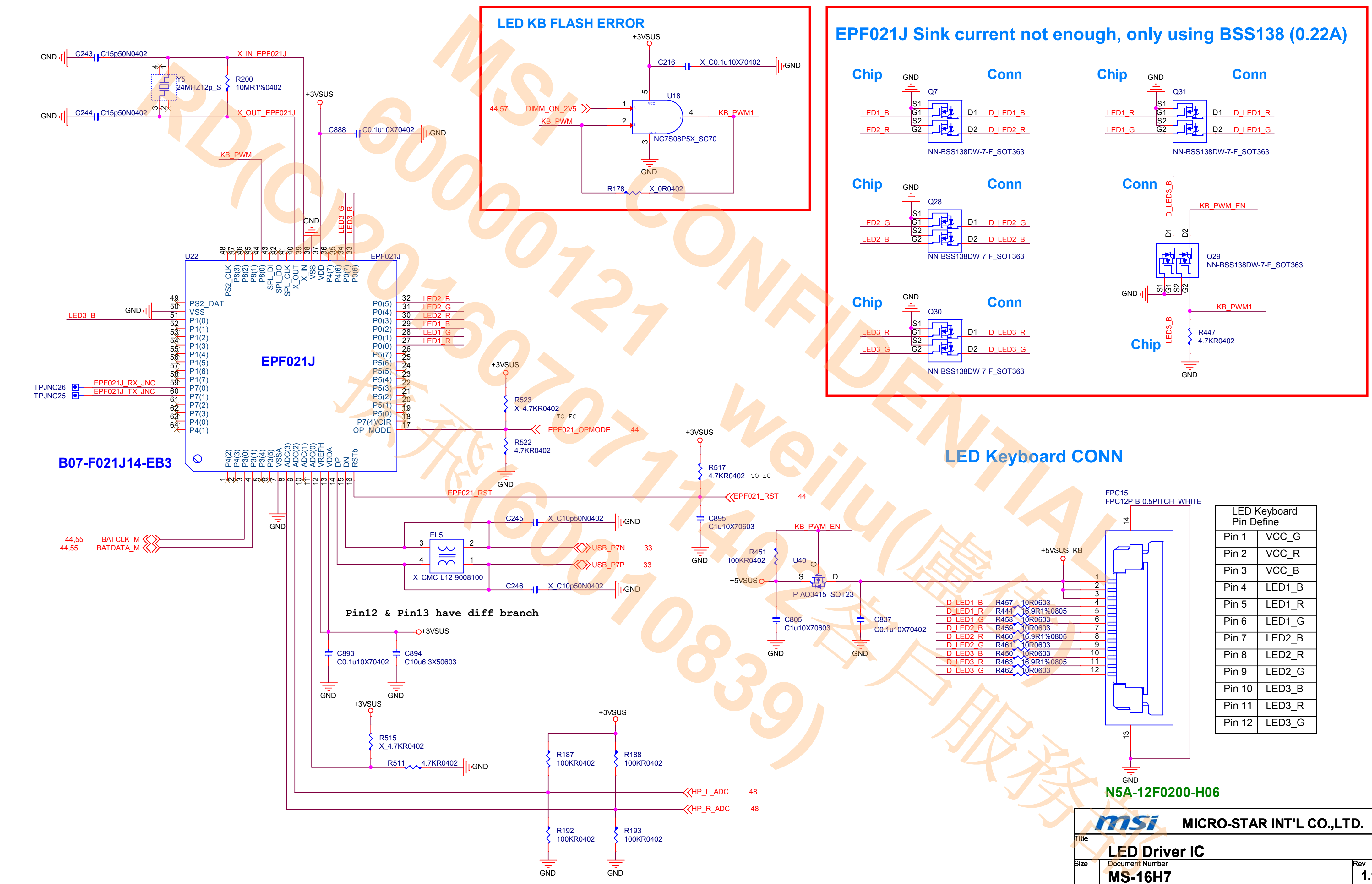
LED Driver IC(EPF021J)



LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

MICRO-STAR INT'L CO.,LTD.

Title: LED Driver IC

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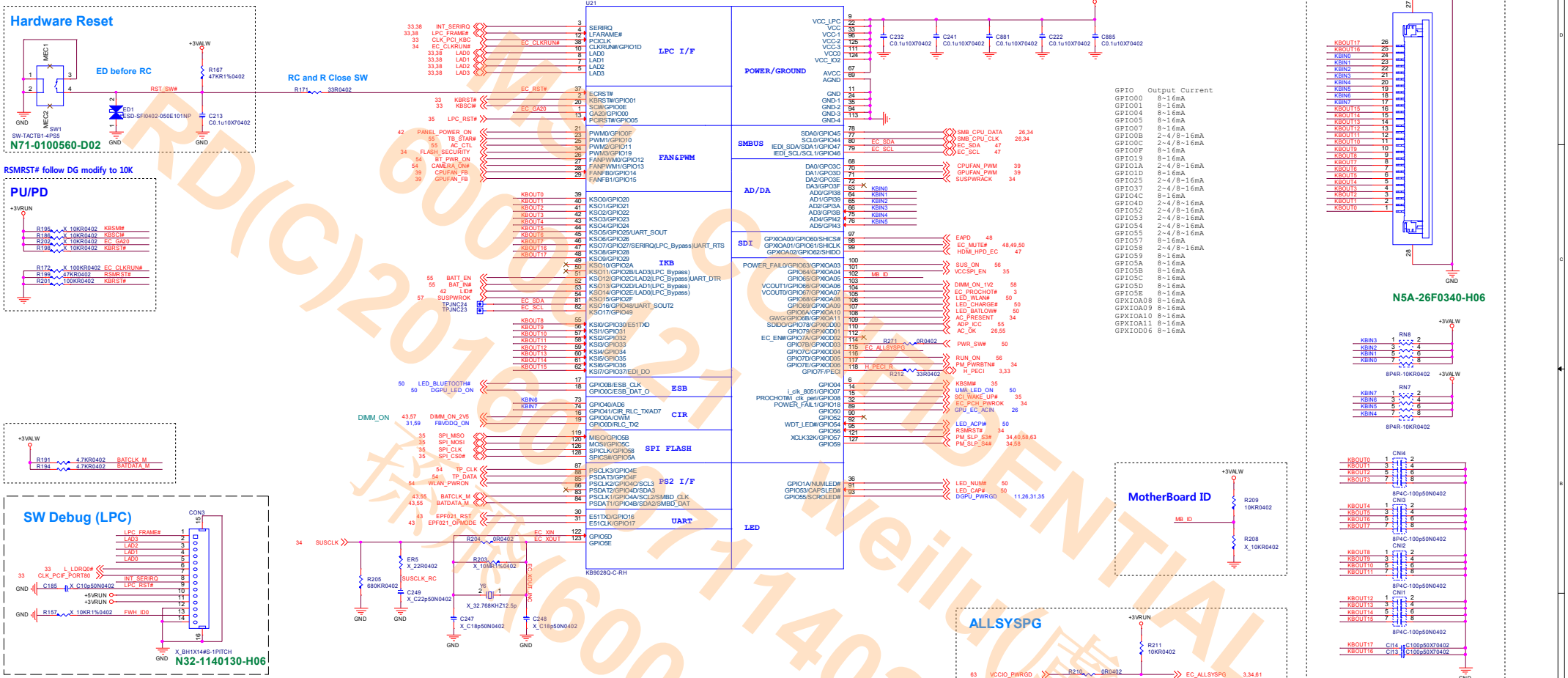
KBC/EC/uP (ENE9028)



GPIO	Output Current
GPIO00	8~16mA
GPIO01	8~16mA
GPIO04	8~16mA
GPIO05	8~16mA
GPIO07	8~16mA
GPIO0B	2~4/8~16mA
GPIO0C	2~4/8~16mA
GPIO0F	8~16mA
GPIO19	8~16mA
GPIO1A	2~4/8~16mA
GPIO1D	8~16mA
GPIO25	2~4/8~16mA
GPIO37	2~4/8~16mA
GPIO4C	8~16mA
GPIO4D	2~4/8~16mA
GPIO52	2~4/8~16mA
GPIO53	2~4/8~16mA
GPIO54	2~4/8~16mA
GPIO55	2~4/8~16mA
GPIO57	8~16mA
GPIO58	2~4/8~16mA
GPIO59	8~16mA
GPIO5A	8~16mA
GPIO5B	8~16mA
GPIO5C	8~16mA
GPIO5D	8~16mA
GPIO5E	8~16mA
GPXIOA08	8~16mA
GPXIOA09	8~16mA
GPXIOA10	8~16mA
GPXIOA11	8~16mA
GPXIOD06	8~16mA

Title	KBC (ENE9028)
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MICRO-STAR INT'L CO.,LTD.

CardReader (RTS5249)

RTS5249 Colay RTS5227

Pin 13/15/16/22/23/24/25/26 definition are different from RTS5227

Power Trace

Pin11(3V3_IN) / Pin 12(CARD_3V3)trace fixed width is 40 mils (minimum)

Pin27(3V3aux) / Pin 13(SD_VDD2)trace fixed width is 30 mils (minimum)

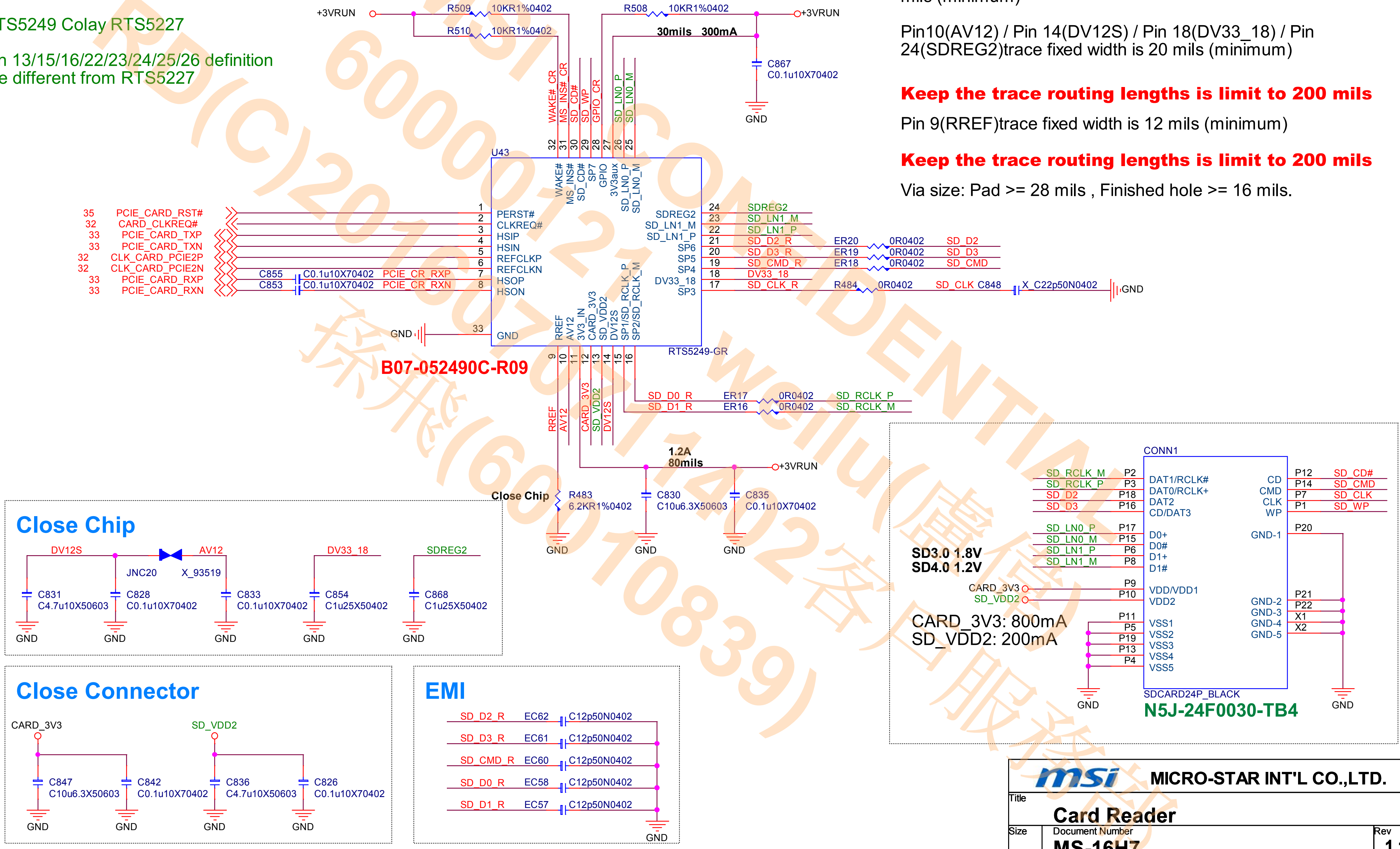
Pin10(AV12) / Pin 14(DV12S) / Pin 18(DV33_18) / Pin 24(SDREG2)trace fixed width is 20 mils (minimum)

Keep the trace routing lengths is limit to 200 mils

Pin 9(RREF)trace fixed width is 12 mils (minimum)

Keep the trace routing lengths is limit to 200 mils

Via size: Pad >= 28 mils , Finished hole >= 16 mils.



msi	MICRO-STAR INT'L CO.,LTD.
Title	Card Reader
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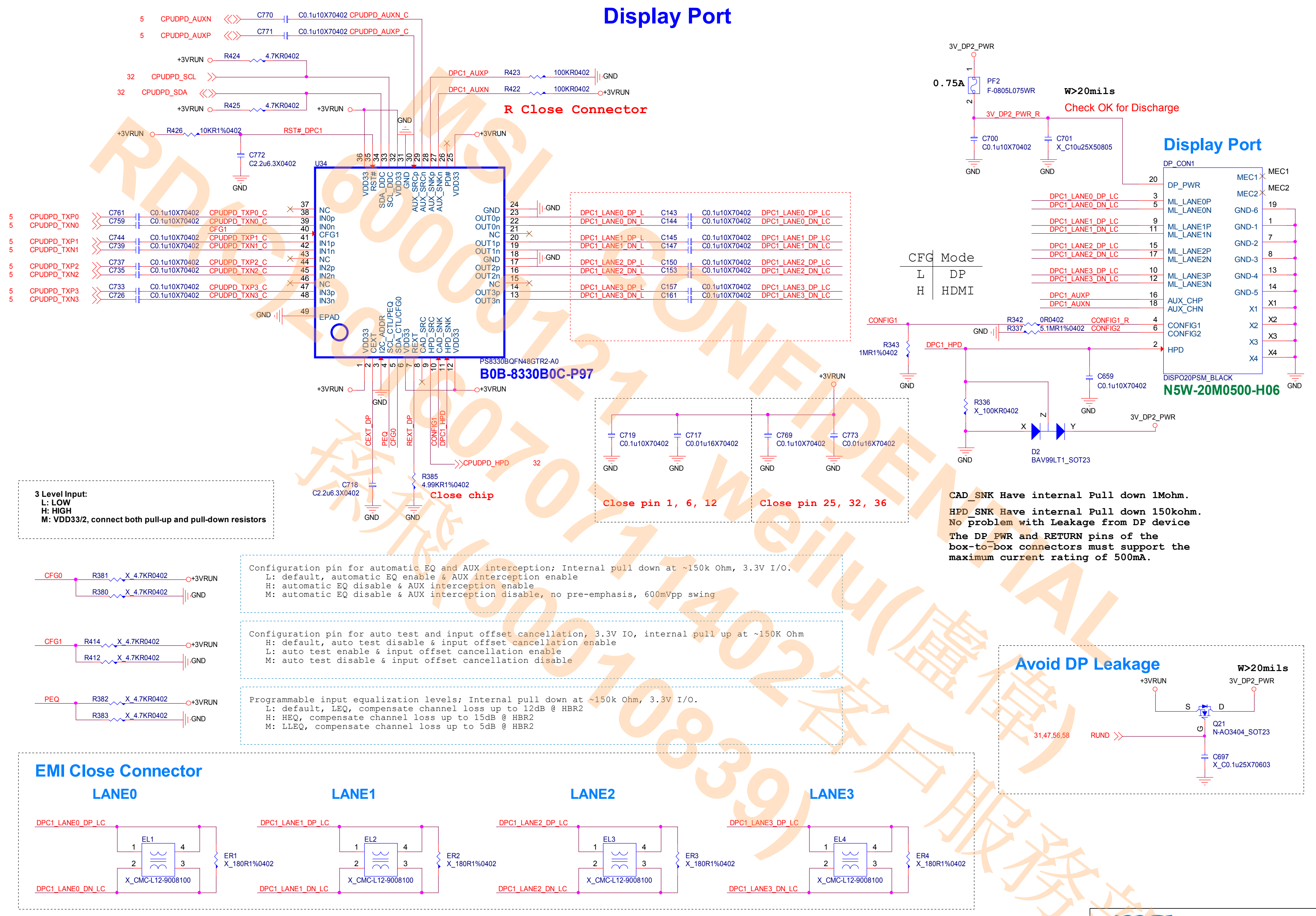
Display Port



CAD_SNK Have internal Pull down 1Mohm.

HPD_SNK Have internal Pull down 150kohm.
No problem with Leakage from DP device

The DP_PWR and RETURN pins of the box-to-box connectors must support the maximum current rating of 500mA.

3 Level Input:
L: LOW
H: HIGH
M: VDD33/2, connect both pull-up and pull-down resistors

CFG0: R381 X_4.7KR0402 +3VRUN; R380 X_4.7KR0402 GND

Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k Ohm, 3.3V I/O.
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

CFG1: R414 X_4.7KR0402 +3VRUN; R412 X_4.7KR0402 GND

Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K Ohm
H: default, auto test disable & input offset cancellation enable
L: auto test enable & input offset cancellation enable
M: auto test disable & input offset cancellation disable

PEQ: R382 X_4.7KR0402 +3VRUN; R383 X_4.7KR0402 GND

Programmable input equalization levels; Internal pull down at ~150k Ohm, 3.3V I/O.
L: default, LEQ, compensate channel loss up to 12dB @ HBR2
H: HEQ, compensate channel loss up to 15dB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2

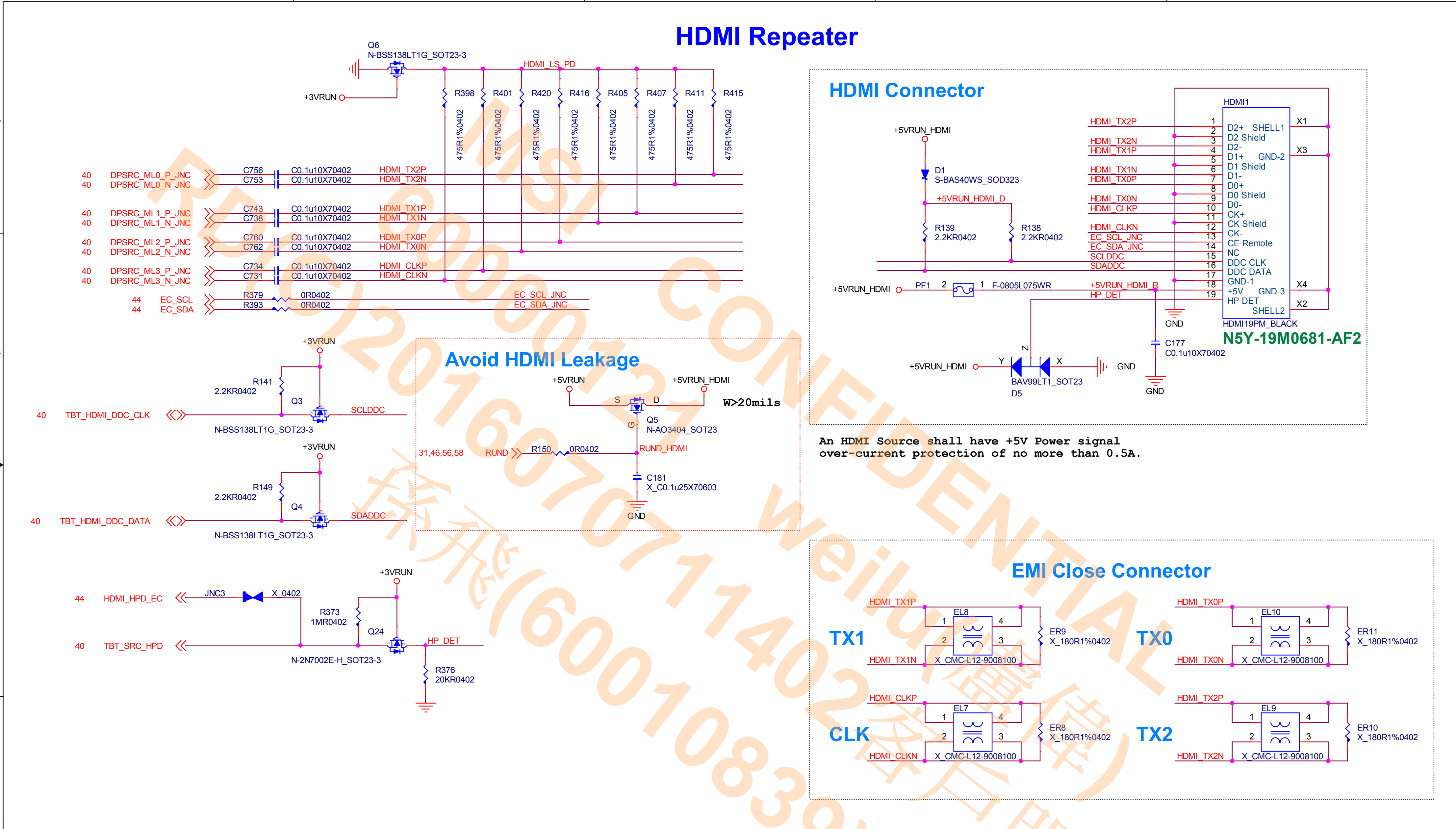
EMI Close Connector

LANE0 — EL1 X_CMC-L12-9008100, ER1 X_180R1%0402
LANE1 — EL2 X_CMC-L12-9008100, ER2 X_180R1%0402
LANE2 — EL3 X_CMC-L12-9008100, ER3 X_180R1%0402
LANE3 — EL4 X_CMC-L12-9008100, ER4 X_180R1%0402

Avoid DP Leakage

W>20mils
+3VRUN, 3V_DP2_PWR, Q21 N-AO3404_SOT23, RUND (31,47,56,58), C697 X_C0.1u25X70603

HDMI Repeater



msi	**MICRO-STAR INT'L CO.,LTD.**
Title	**HDMI Repeater**
Size / Document Number	**MS-16H7**
Rev	**1.1**
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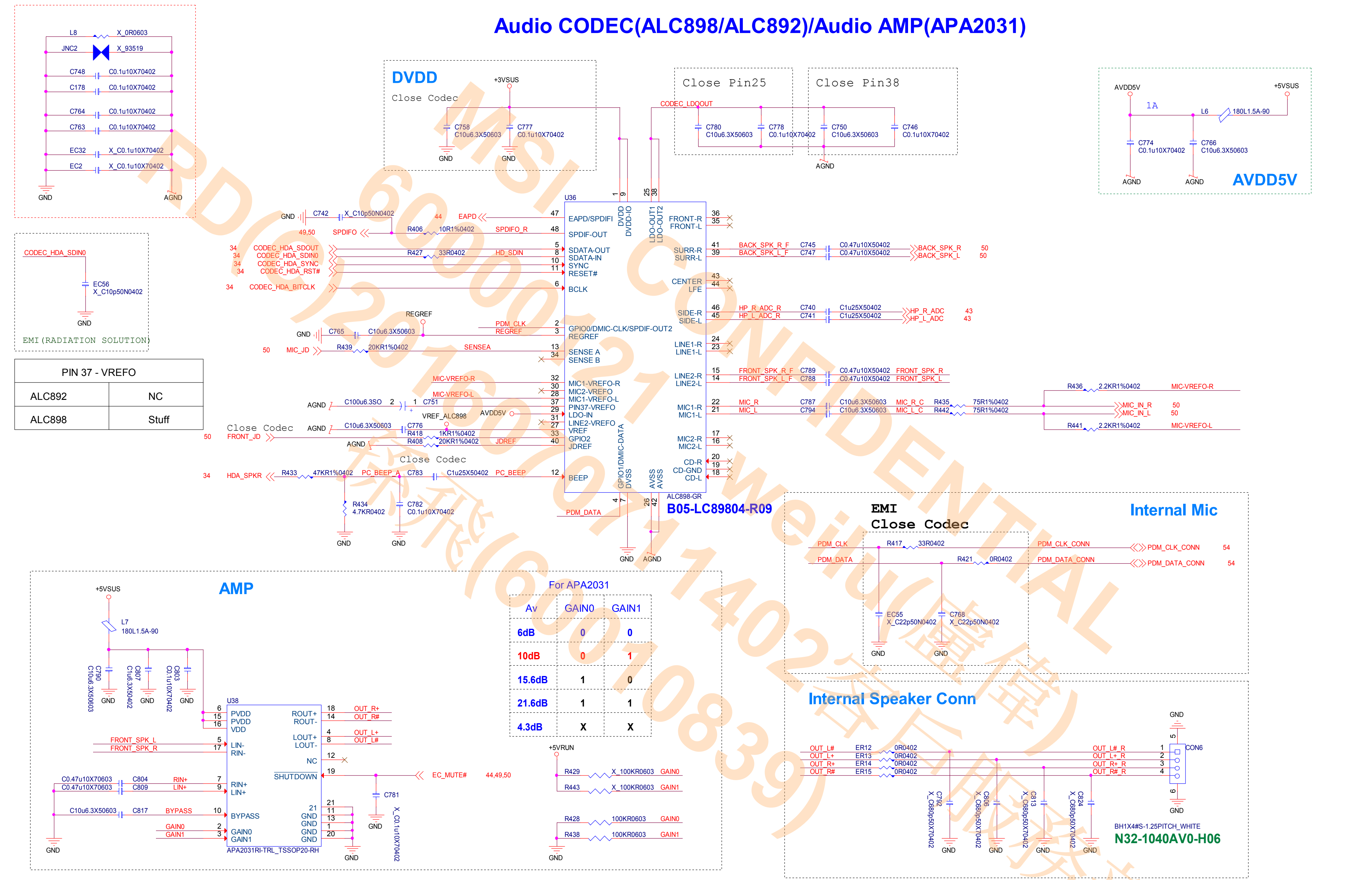
Audio CODEC(ALC898/ALC892)/Audio AMP(APA2031)



PIN 37 - VREFO	
ALC892	NC
ALC898	Stuff

For APA2031

Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

MICRO-STAR INT'L CO.,LTD.

Title: Audio CODEC/Audio AMP

Document Number: MS-16H7

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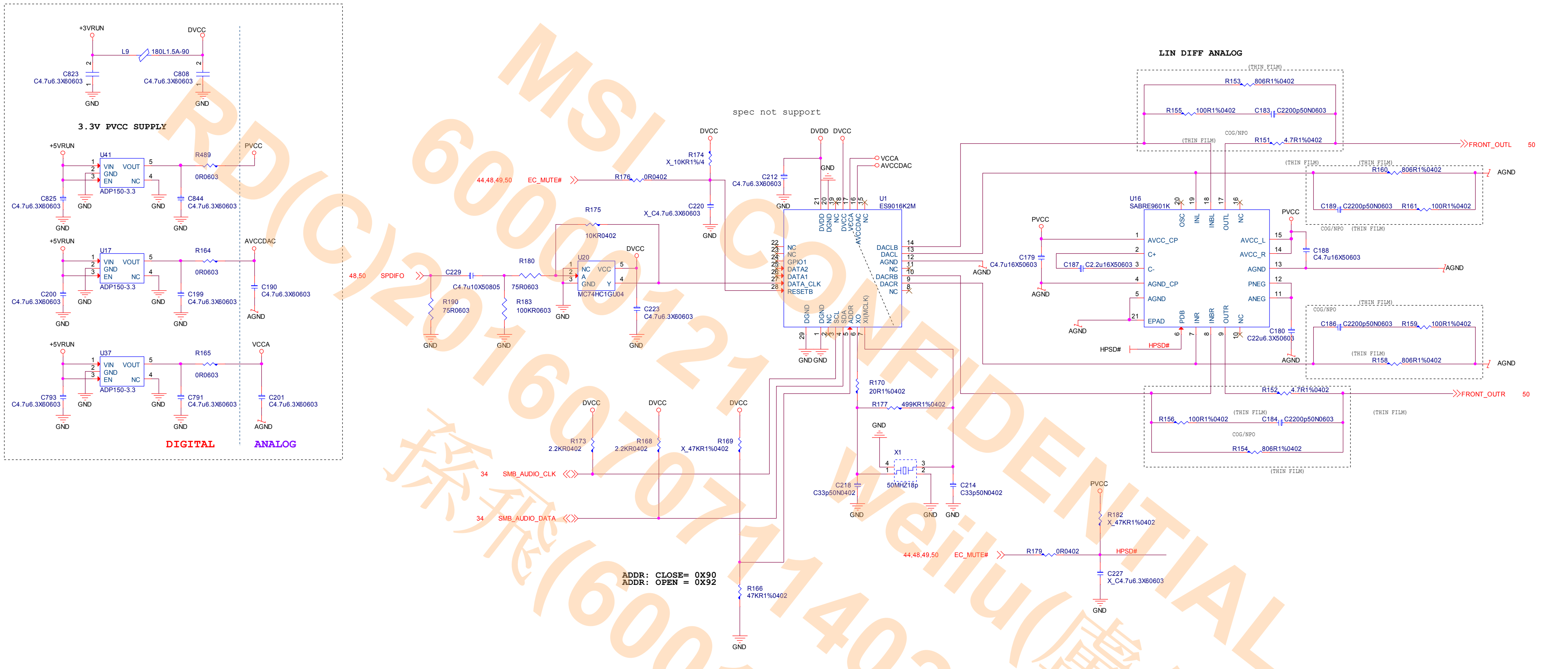
Audio DAC(ES9018)/Headphone Driver(SABRE9601)



msi	MICRO-STAR INT'L CO.,LTD.		
Title	Audio DAC/Headphone Driver		
Size	Document Number: MS-16H7		Rev 1.1
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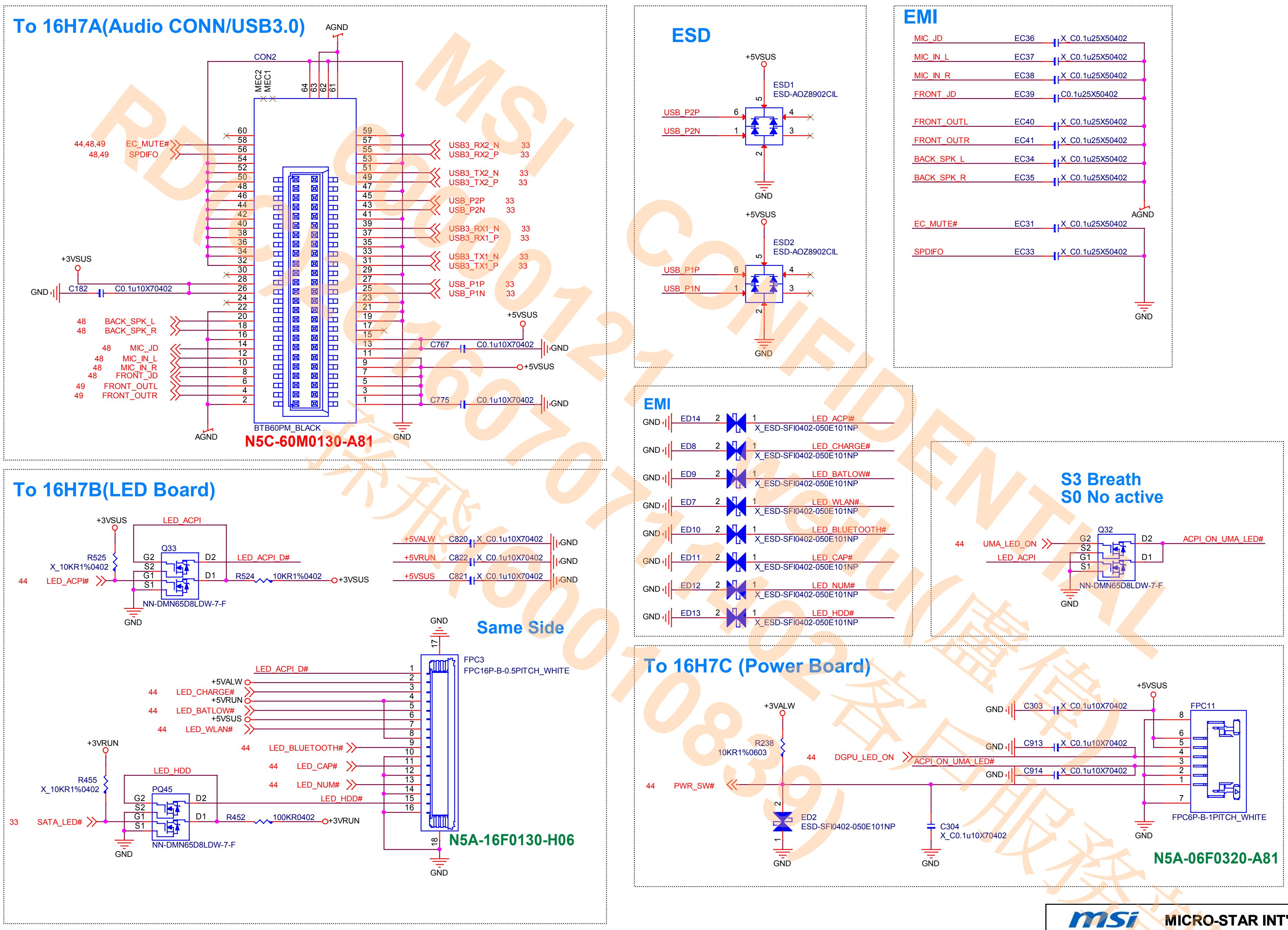
BTB CONN



MICRO-STAR INT'L CO.,LTD.

Title	BTB CONN	
Size	Document Number: MS-16H7	Rev 1.1
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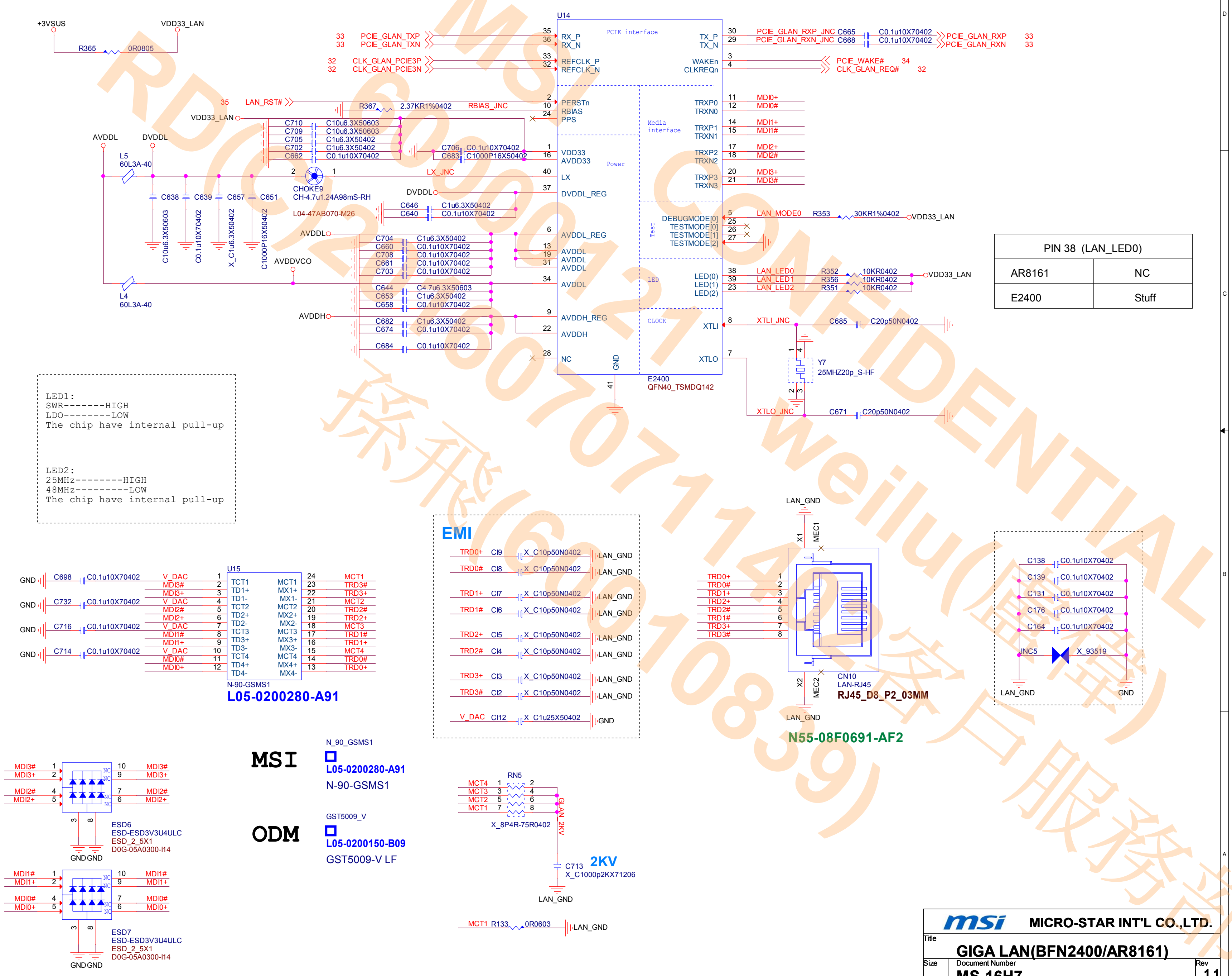
GIGA LAN(BFN2400/AR8161)



LED1:
SWR--------HIGH
LDO---------LOW
The chip have internal pull-up

LED2:
25MHz---------HIGH
48MHz---------LOW
The chip have internal pull-up

PIN 38 (LAN_LED0)	
AR8161	NC
E2400	Stuff

MSI
N_90_GSMS1
L05-0200280-A91
N-90-GSMS1

ODM
GST5009_V
L05-0200150-B09
GST5009-V LF

MICRO-STAR INT'L CO.,LTD.

Title	GIGA LAN(BFN2400/AR8161)	
Size	Document Number: MS-16H7	Rev 1.1
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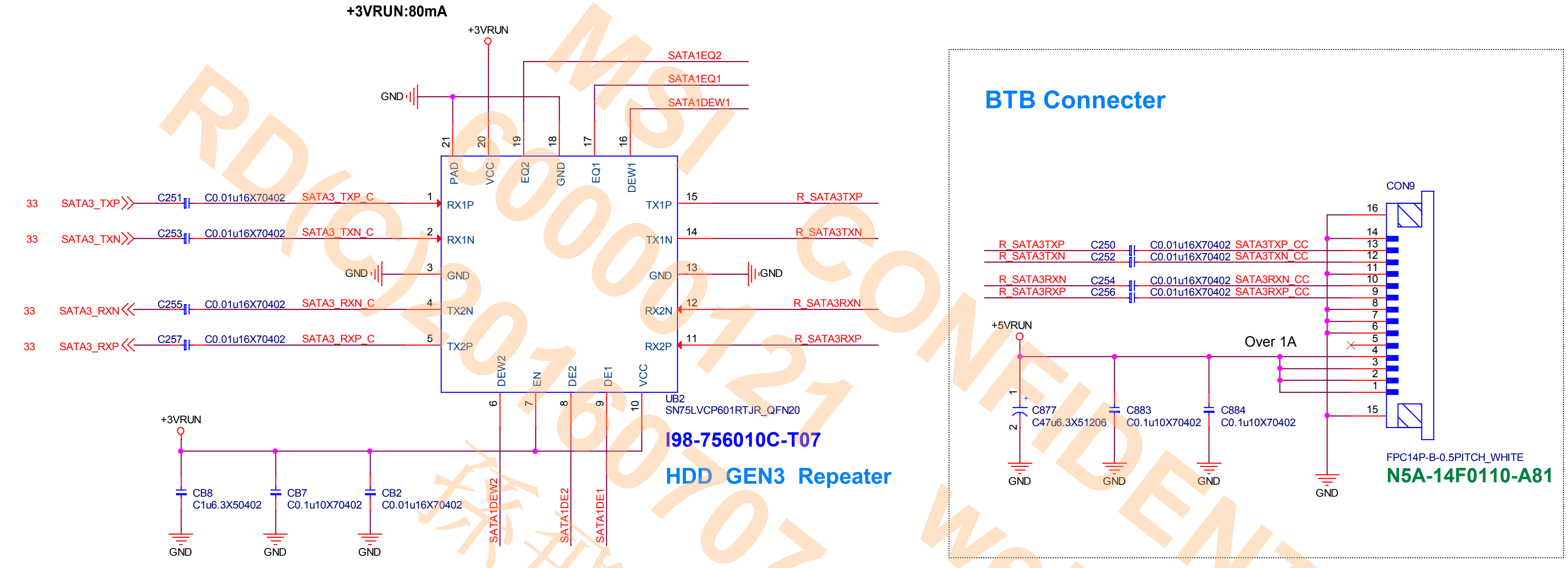
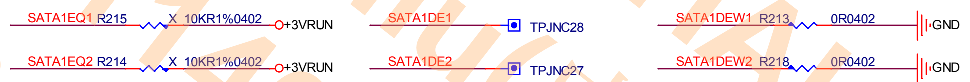
HDD (With Repeater)





TI SN75LVCP601RTJR HW Setting

DE1/DE2	CH1/CH2De-Emphasis dB(at 6Gbps)	DQ1/DQ2	CH1/CH2De-Emphasis dB(at 6Gbps)
NC(default)	-4	NC(default)	0
0	0	0	7
1	-2	1	14

DEW1/DEW2	Device Function --> De Width for CH1/CH2
0	De-emphasis Pulse duration, short(recommended setting when linkoperates at SATA 1.5/3/6 Gbps)
1(default)	De-emphasis Pulse duration, long(recommended setting when linkoperates at SATA 1.5/3/6 Gbps)

MICRO-STAR INT'L CO.,LTD.

Title: HDD With Repeater

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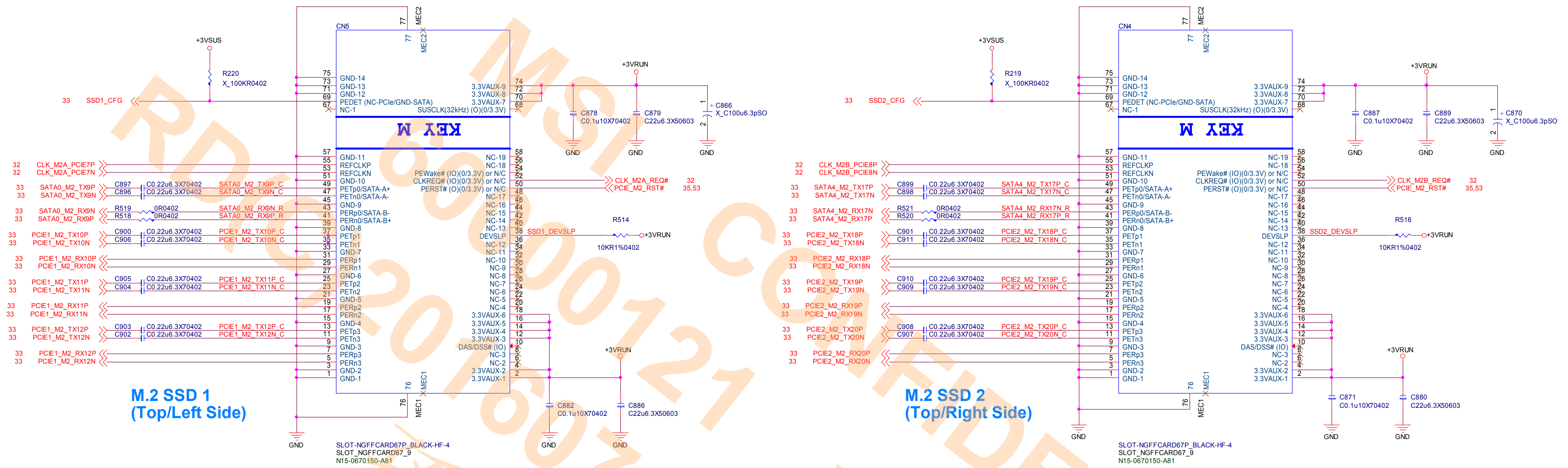
SSD



MICRO-STAR INT'L CO.,LTD.			
Title	SSD		
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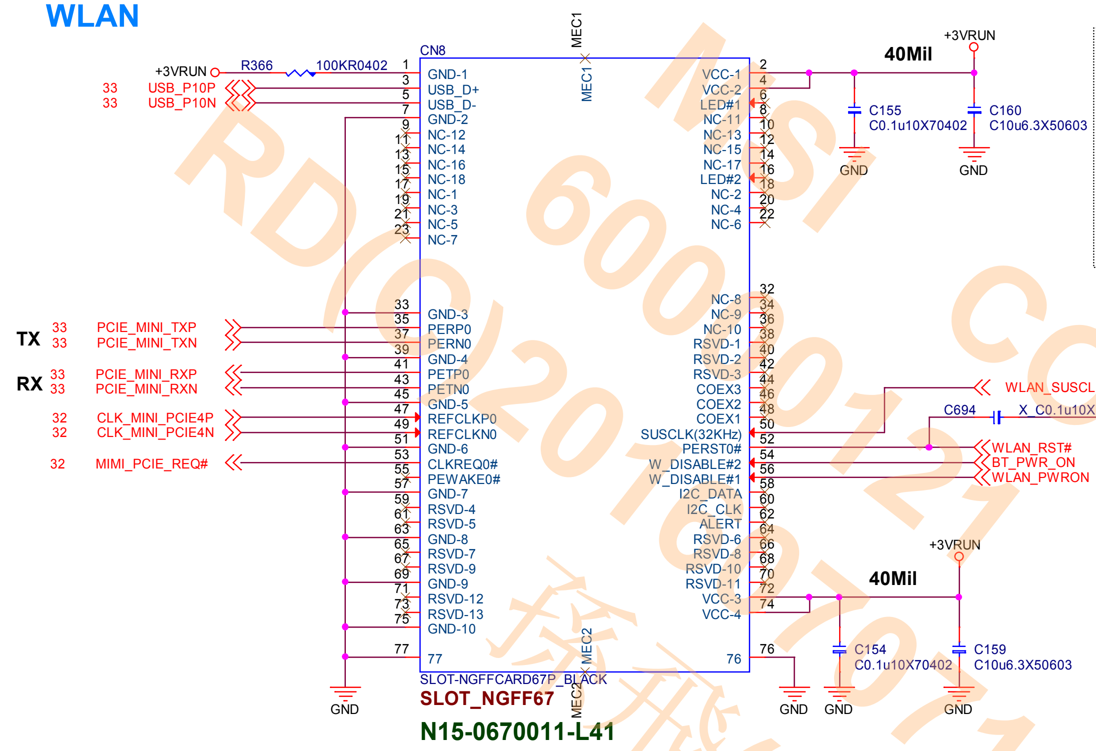
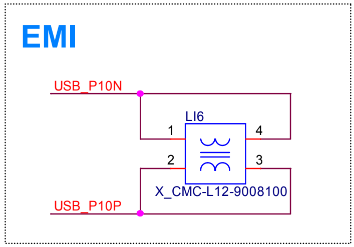
WLAN /Camera/ClickPad/FP

WLAN

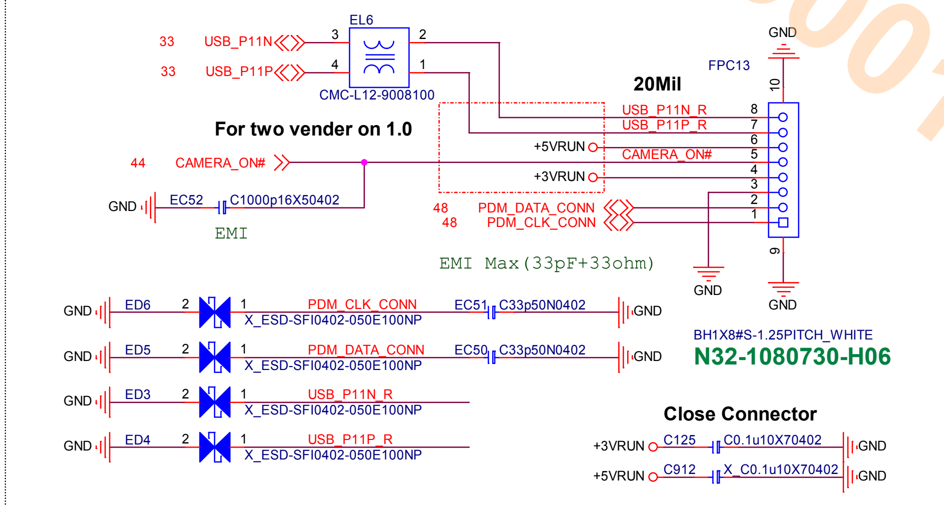


EMI



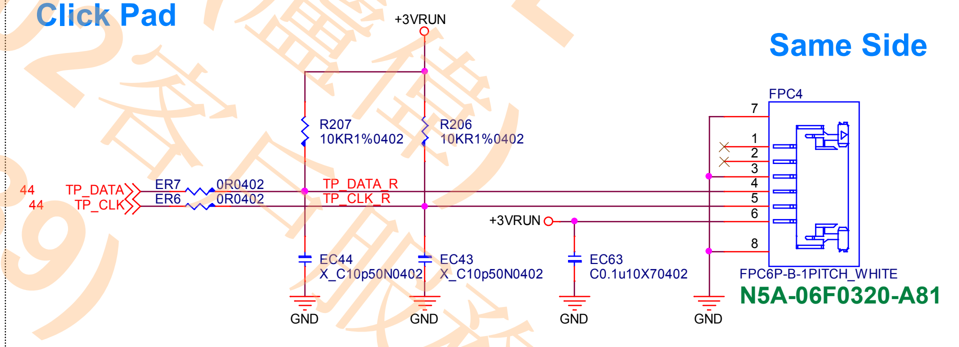
Pin 1	GND		
Pin 3	USB_D+	Pin 2	3.3V
Pin 5	USB_D-	Pin 4	3.3V
Pin 7	GND	Pin 6	LED1#
Pin 9	Module Key	Pin 8	Module Key
Pin 11	Module Key	Pin 10	Module Key
Pin 13	Module Key	Pin 12	Module Key
Pin 15	Module Key	Pin 14	Module Key
Pin 17	N/C	Pin 16	LED2#
Pin 19	N/C	Pin 18	GND
Pin 21	N/C	Pin 20	N/C
Pin 23	N/C	Pin 22	N/C
Pin 25	Module Key	Pin 24	Module Key
Pin 27	Module Key	Pin 26	Module Key
Pin 29	Module Key	Pin 28	Module Key
Pin 31	Module Key	Pin 30	Module Key
Pin 33	GND	Pin 32	N/C
Pin 35	PERP0	Pin 34	N/C
Pin 37	PERN0	Pin 36	N/C
Pin 39	GND	Pin 38	Clink Reset (I 3.3V)
Pin 41	PETP0	Pin 40	N/C
Pin 43	PETN0	Pin 42	N/C
Pin 45	GND	Pin 44	N/C
Pin 47	REFCLKP0	Pin 46	N/C
Pin 49	REFCLKN0	Pin 48	N/C
Pin 51	GND	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 53	CLKREQ0#	Pin 52	PERST0#
Pin 55	PEWAKE0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 57	GND	Pin 56	WLAN_EN(W_DISABLE2#)
Pin 59	N/C	Pin 58	N/C
Pin 61	N/C	Pin 60	N/C
Pin 63	GND	Pin 62	N/C
Pin 65	N/C	Pin 64	Resever
Pin 67	N/C	Pin 66	N/C
Pin 69	GND	Pin 68	N/C
Pin 71	N/C	Pin 70	N/C
Pin 73	N/C	Pin 72	3.3V
Pin 75	GND	Pin 74	3.3V

CAMERA



Click Pad

Same Side



MICRO-STAR INT'L CO.,LTD.

Title: WLAN /Camera/ClickPad/FP

Size | Document Number: MS-16H7 | Rev 1.1

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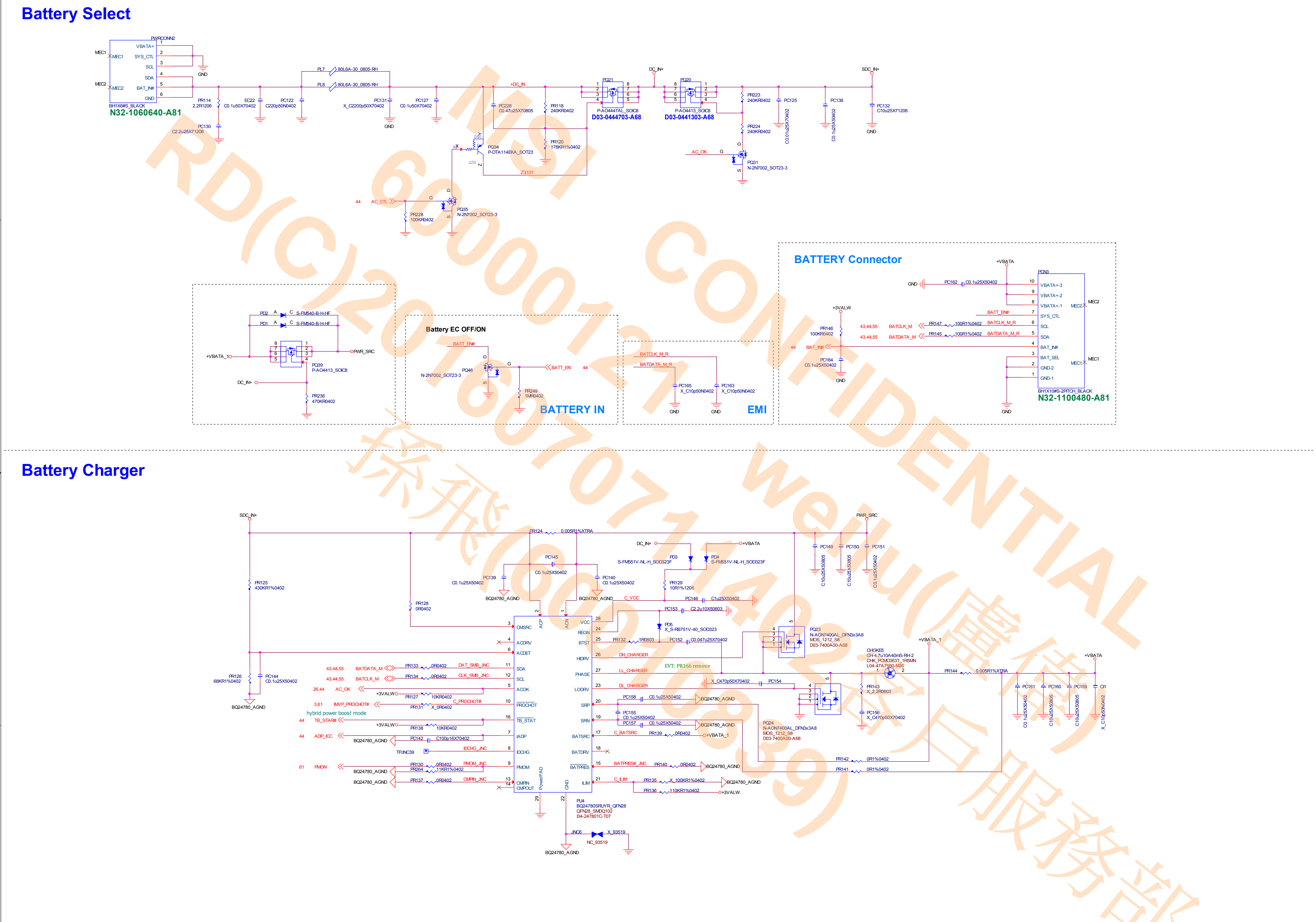
Battery Select/Charger



MICRO-STAR INT'L CO.,LTD.

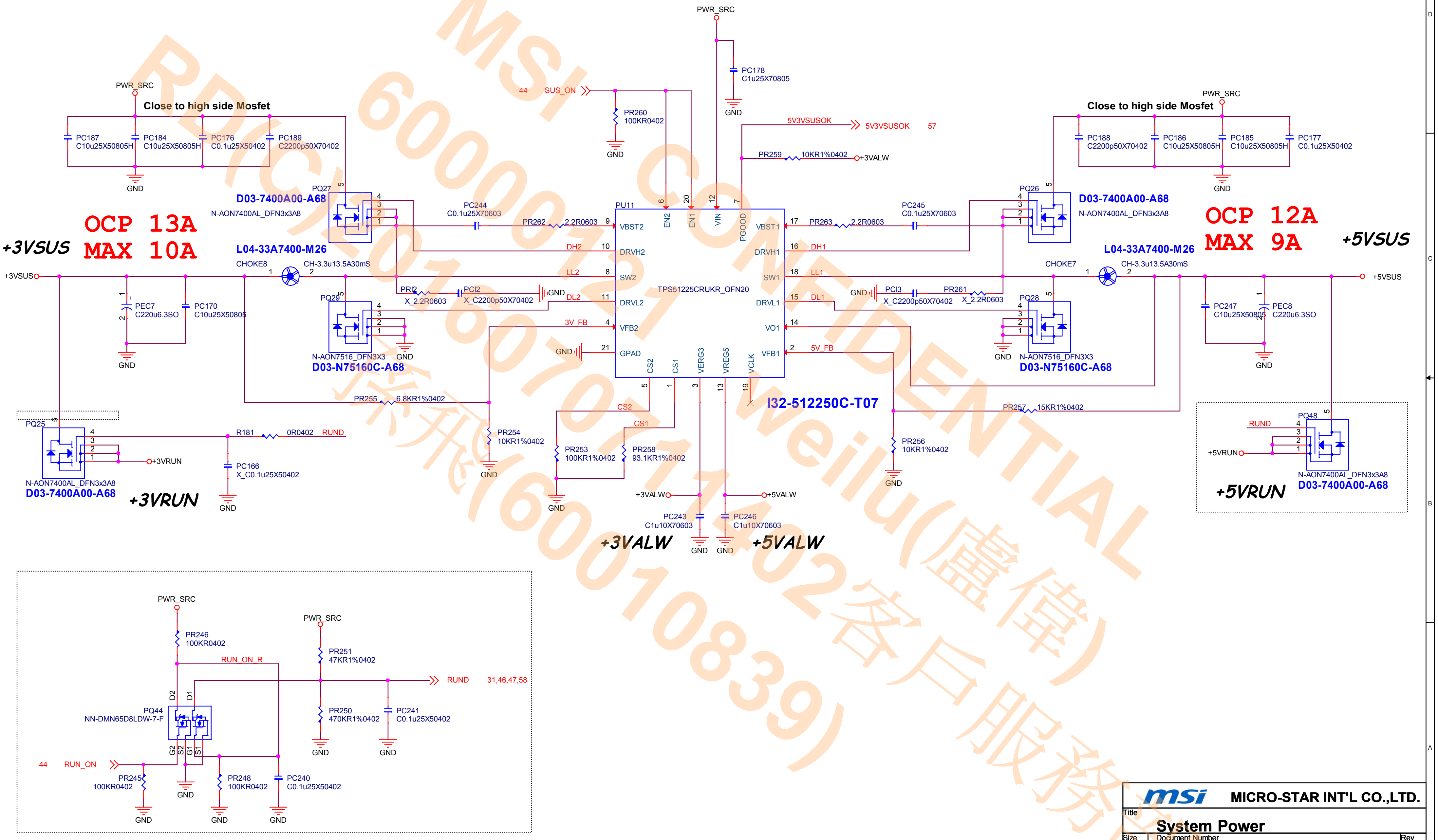
Title: Battery Select/Charger

Document Number: MS-16H7

Rev: 1.1

Date: Wednesday, July 08, 2015 Sheet 55 of 74

System Power

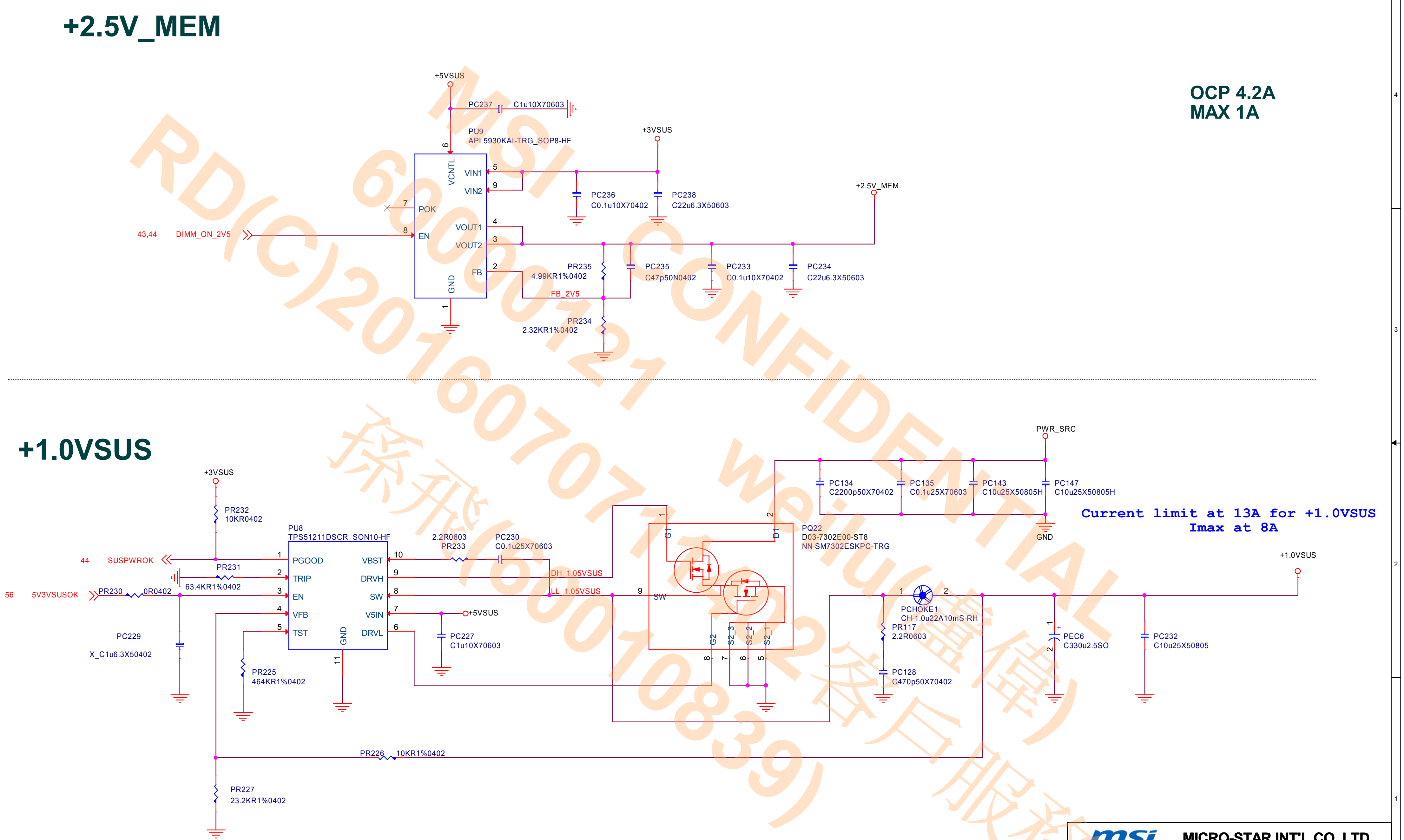


MICRO-STAR INT'L CO.,LTD.

Title: System Power

Size | Document Number: MS-16H7 | Rev: 1.1

Date: Wednesday, July 08, 2015 | Sheet 56 of 74



msi MICRO-STAR INT'L CO.,LTD.

Title: 2.5VMEM/1.0VSUS

Size | Document Number: MS-16H7 | Rev: 1.1

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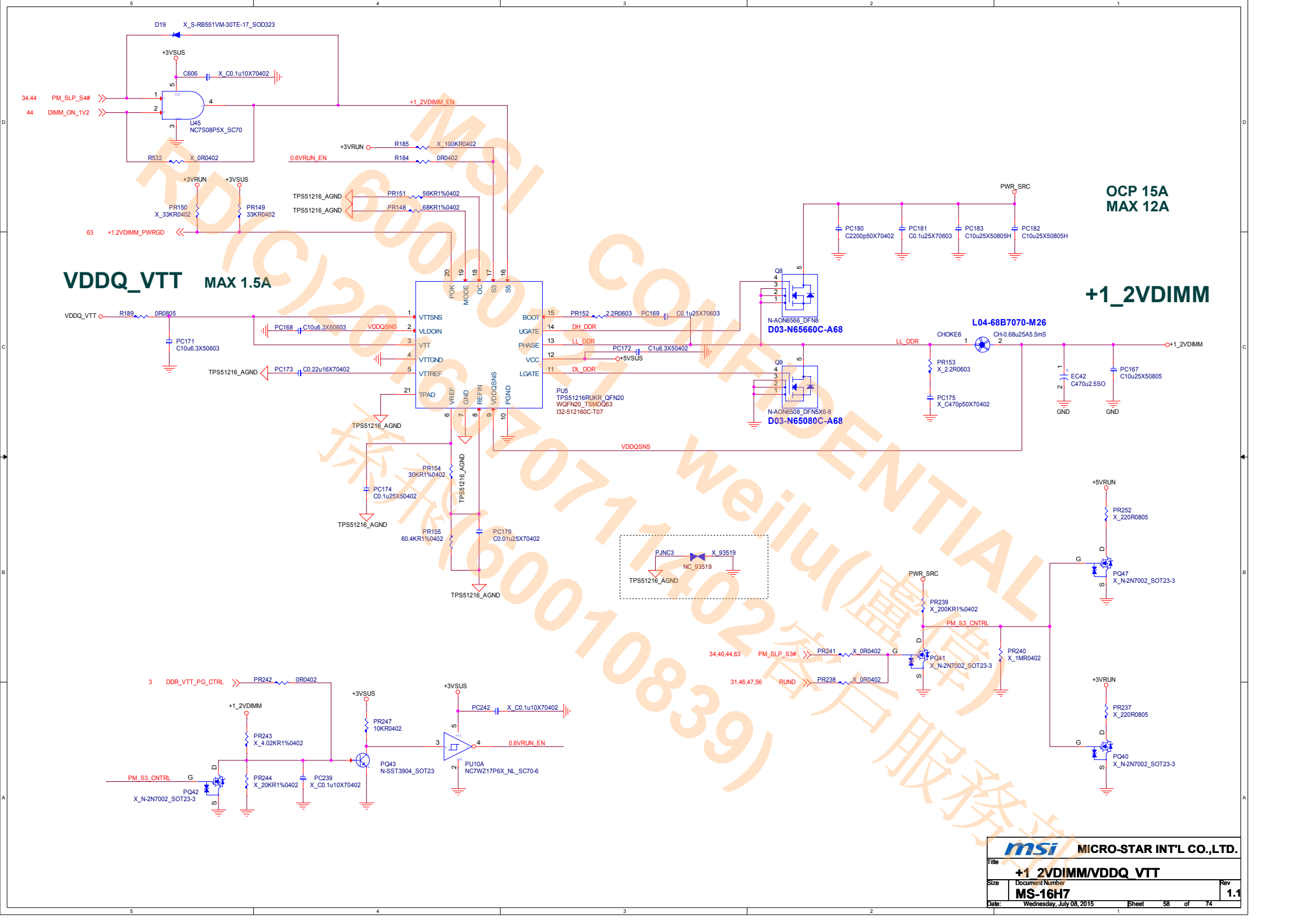
VDDQ_VTT
MAX 1.5A
+1_2VDIMM
OCP 15A
MAX 12A
D03-N65660C-A68
D03-N65080C-A68
L04-68B7070-M26
TPS51216RUKR_QFN20
WQFN20_TSMD63
I32-512160C-T07
MICRO-STAR INT'L CO.,LTD.
+1_2VDIMM/VDDQ_VTT
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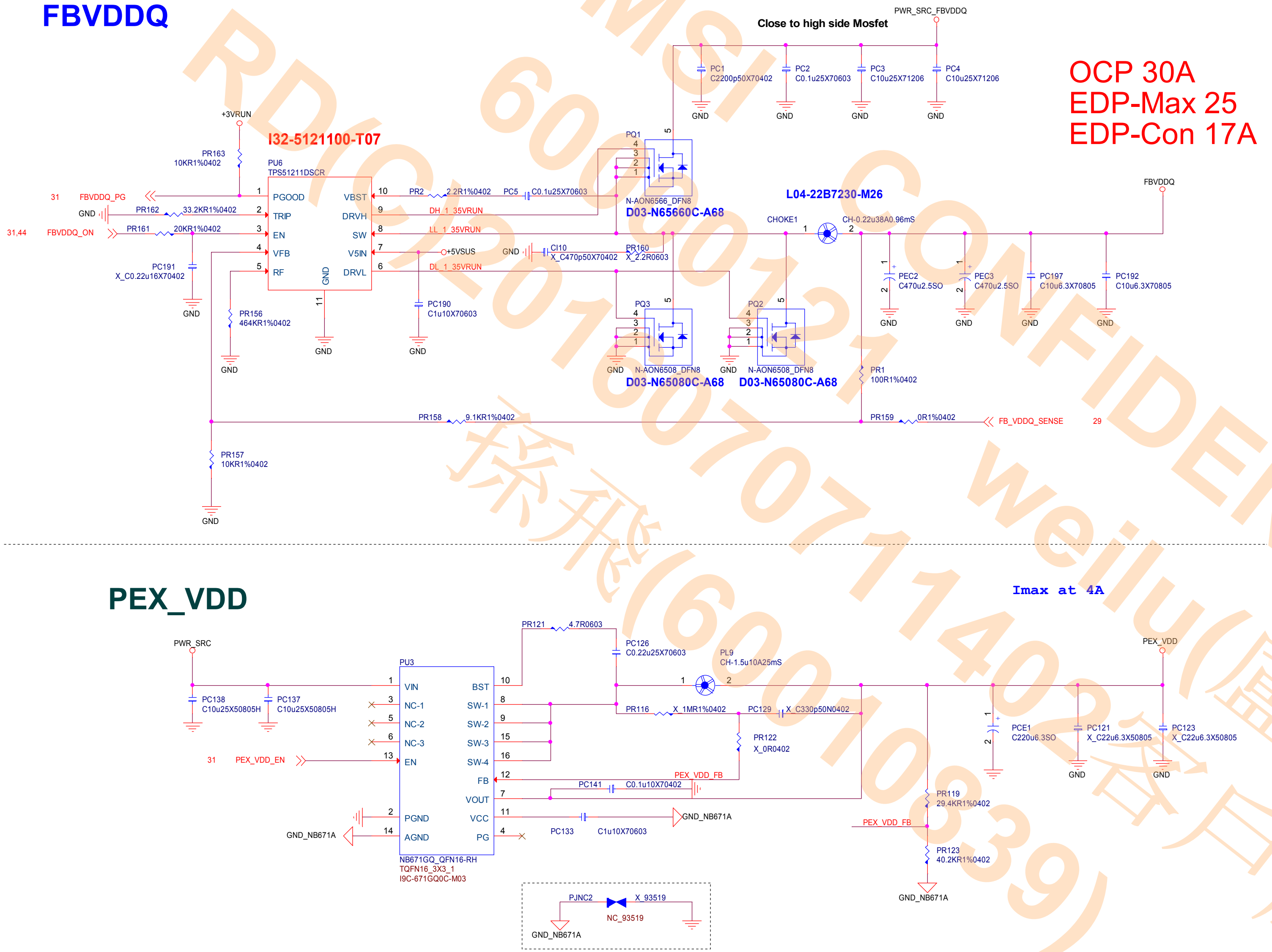
DGPU POWER FBVDDQ



FBVDDQ

PEX_VDD

MICRO-STAR INT'L CO.,LTD.

Title: DGPU POWER FBVDDQ / PEX_VDD

Size	Document Number	Rev
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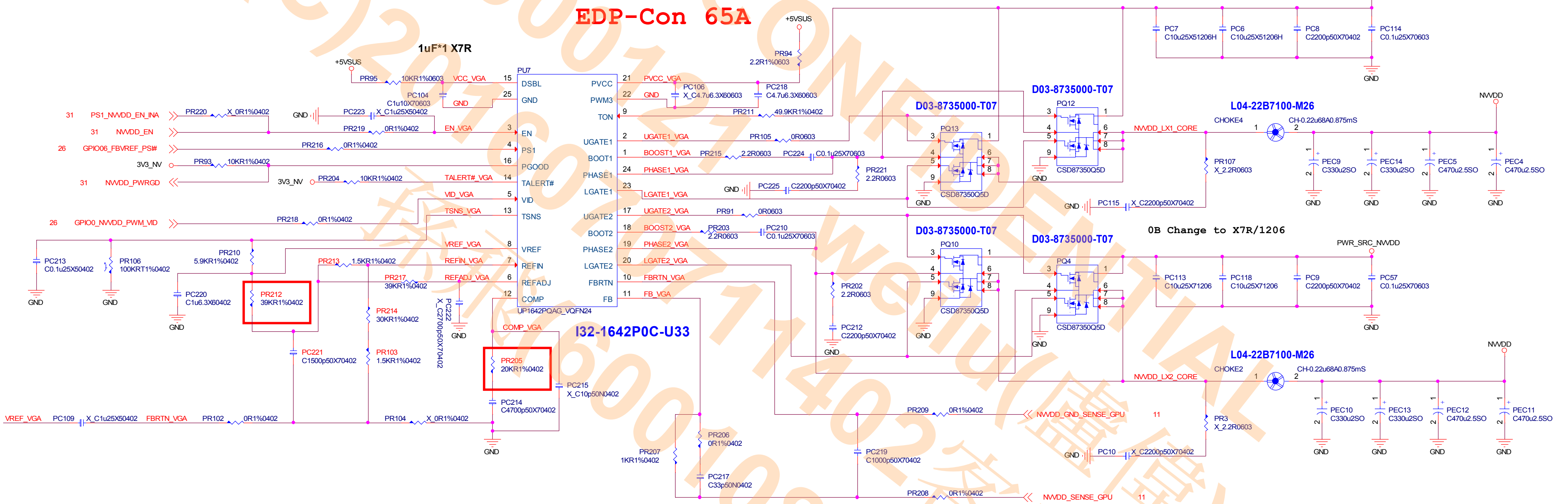
DGPU POWER NVVDD

DGPU POWER / UP1642PQAG

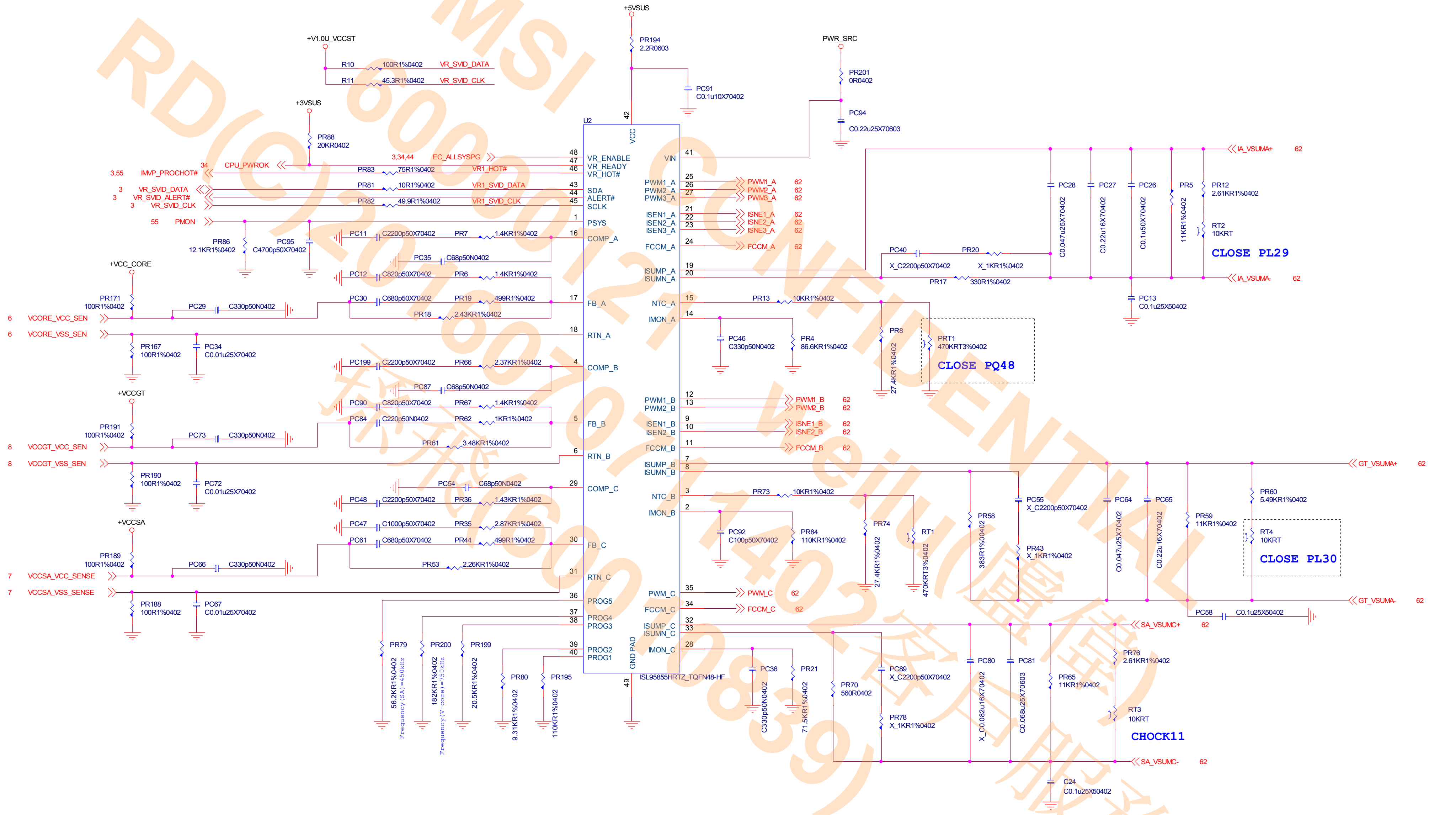
CONFIG B
VBoot:0.9V
Vmin:0.6V / Vmax:1.2V

EDP-Peak 130A
EDP-MAX 69A
EDP-Con 65A



1uF*1 X7R
+5VSUS
PU7
UP1642PQAG_VQFN24
I32-1642P0C-U33
DSBL
GND
EN
PS1
PGOOD
TALERT#
VID
TSNS
VREF
REFIN
REFADJ
COMP
PVCC
PWM3
TON
UGATE1
BOOT1
PHASE1
LGATE1
UGATE2
BOOT2
PHASE2
LGATE2
FBRTN
FB
PS1_NVDD_EN_INA
NVDD_EN
GPIO06_FBVREF_PSI#
3V3_NV
NVDD_PWRGD
GPIO0_NVDD_PWM_VID
VREF_VGA
FBRTN_VGA
VCC_VGA
PVCC_VGA
EN_VGA
TALERT#_VGA
VID_VGA
TSNS_VGA
REFIN_VGA
REFADJ_VGA
COMP_VGA
UGATE1_VGA
BOOT1_VGA
PHASE1_VGA
LGATE1_VGA
UGATE2_VGA
BOOST2_VGA
PHASE2_VGA
LGATE2_VGA
FBRTN_VGA
FB_VGA
PR212
39KR1%0402
PR205
20KR1%0402
D03-8735000-T07
CSD87350Q5D
PQ13
PQ12
PQ10
PQ4
L04-22B7100-M26
CHOKE4
CHOKE2
CH-0.22u68A0.875mS
NVDD_LX1_CORE
NVDD_LX2_CORE
NVDD
PWR_SRC_NVDD
0B Change to X7R/1206
1.0 Change to X5R/1206 high
0B Change to X7R/1206
NVDD_GND_SENSE_GPU
NVDD_SENSE_GPU
GND

CPU Power IC (ISL95855)

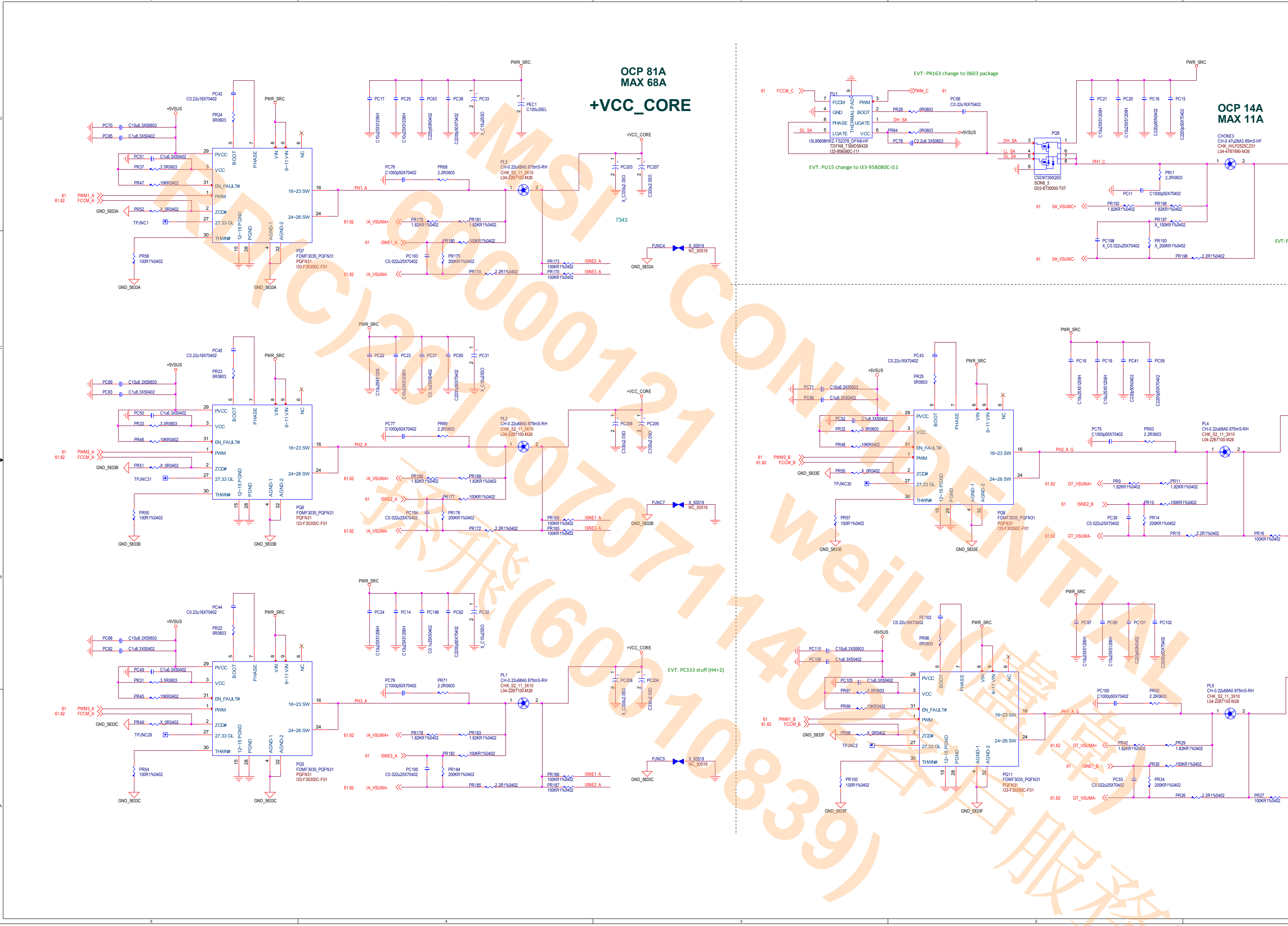


MICRO-STAR INT'L CO.,LTD.

Title: CPU Power IC (ISL95855)

Size	Document Number	Rev
	MS-16H7	1.1

Date: Wednesday, July 08, 2015 Sheet 61 of 74



MICRO-STAR INT'L CO.,LTD.

Title: CPU Power(VCore/VCCGT/VCCSA)

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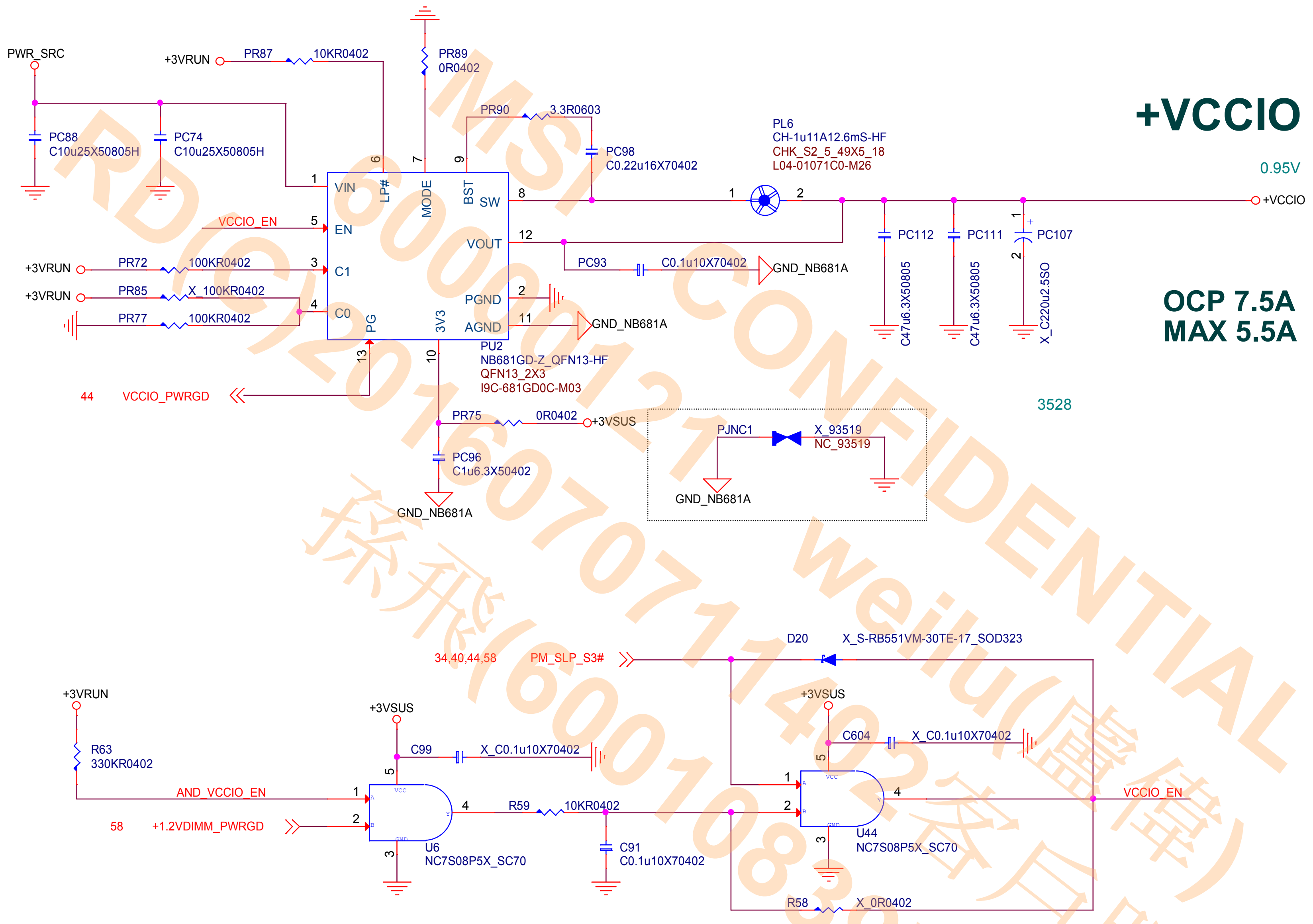
+VCCIO



msi	MICRO-STAR INT'L CO.,LTD.	
Title	CPU Power(VCCIO)	
Size	Document Number: MS-16H7	Rev 1.1
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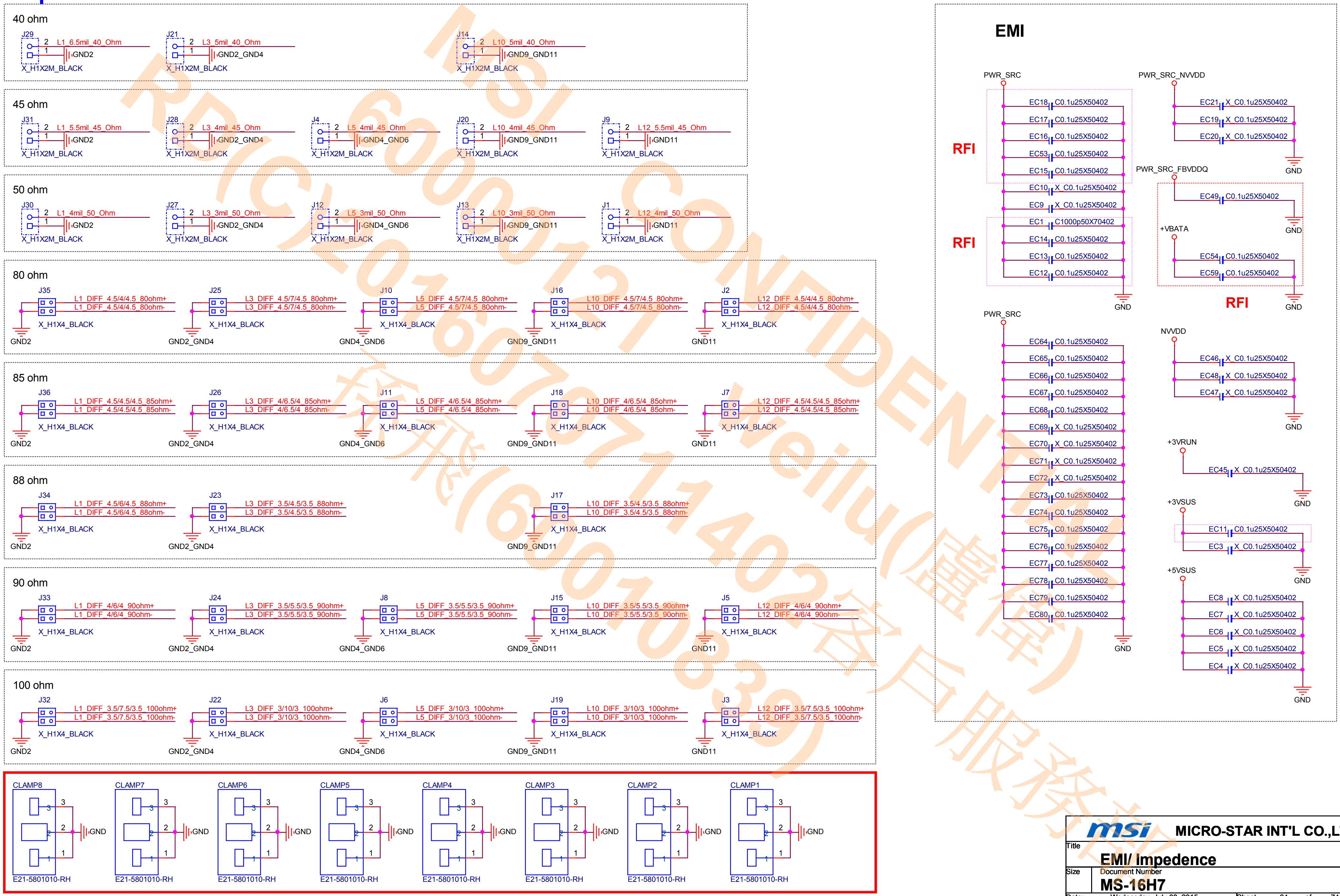
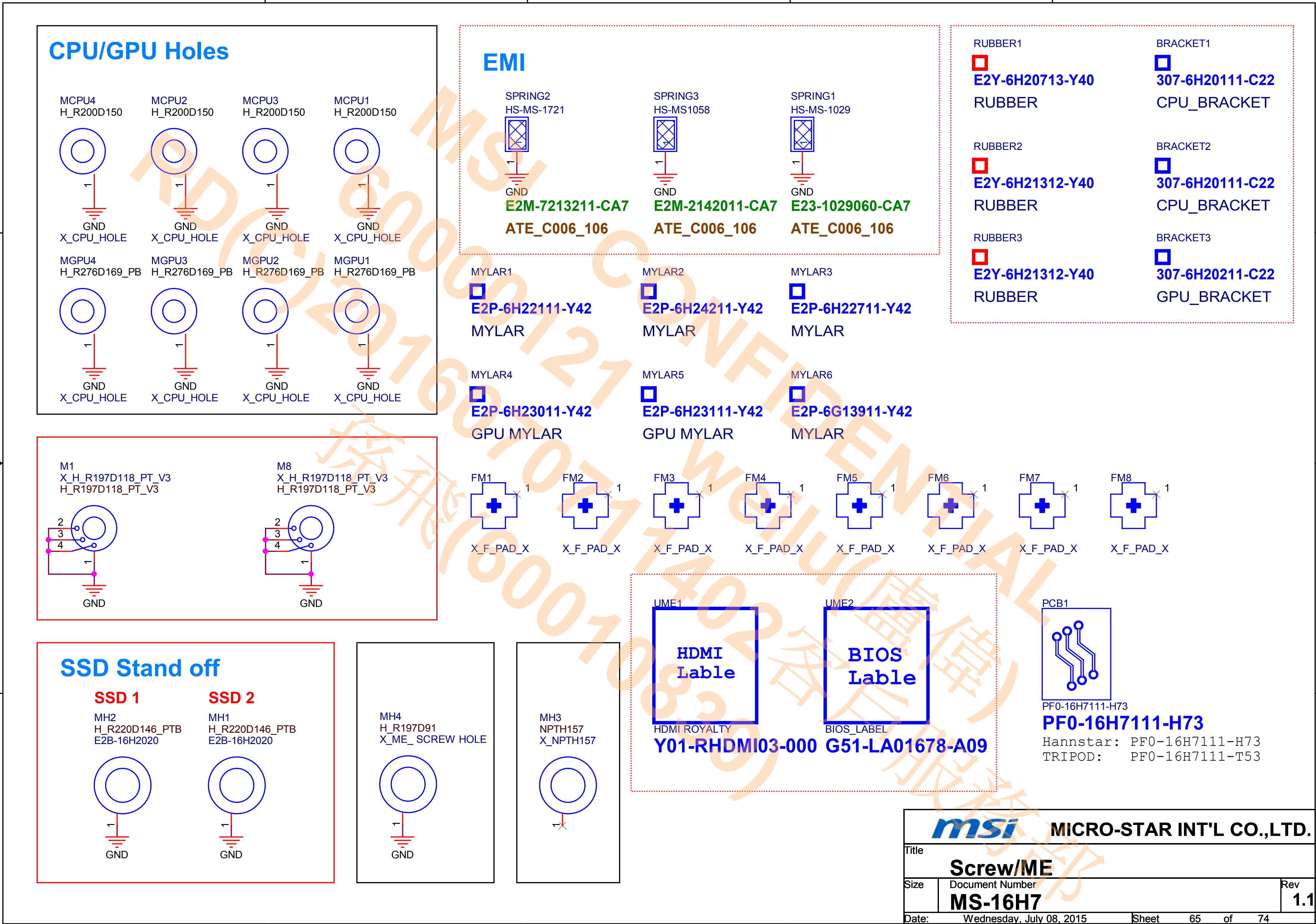
EMI/ Impedence

Impedence Connector No PN



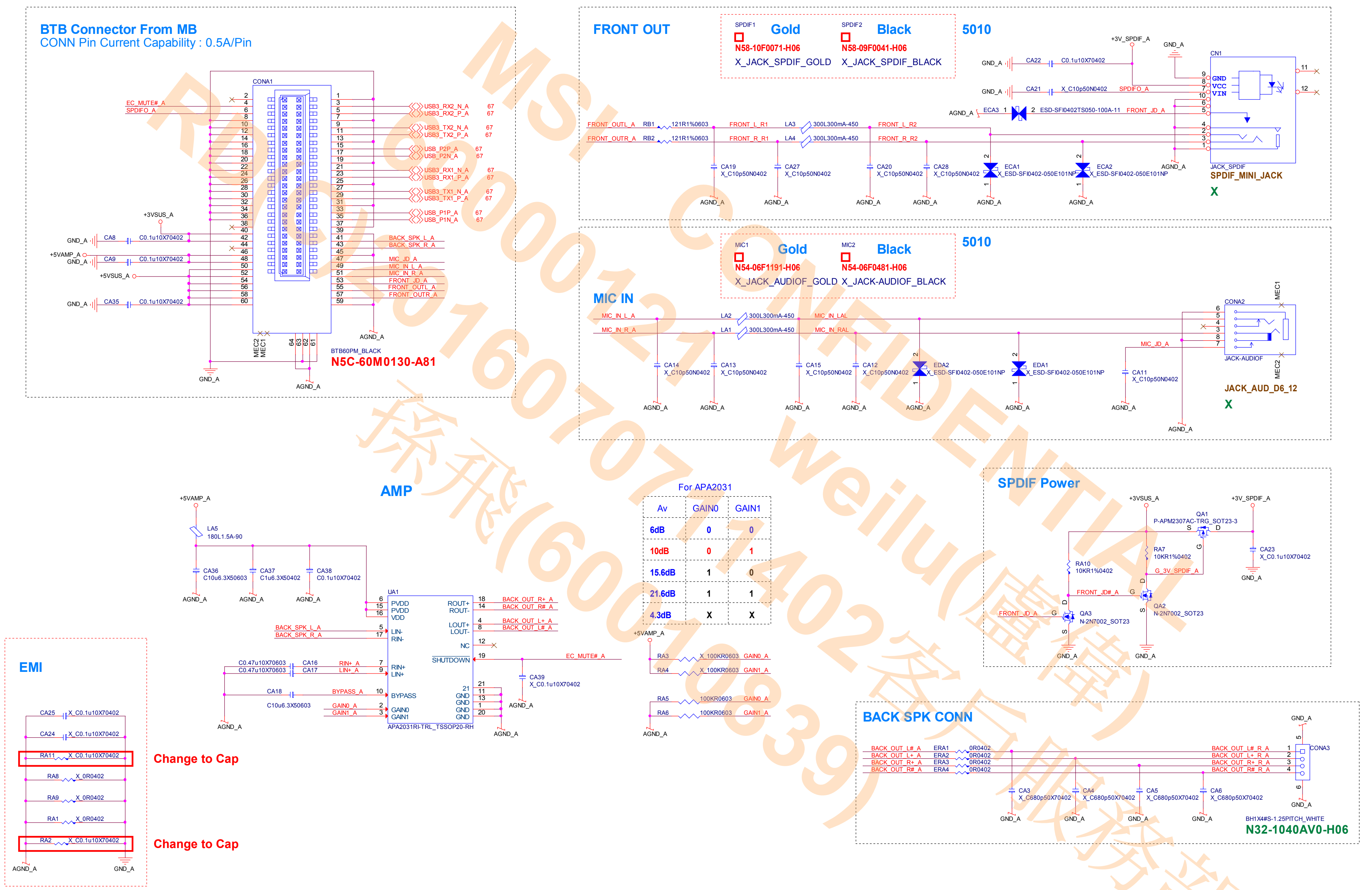
MICRO-STAR INT'L CO.,LTD.

Title	EMI/ Impedence		
Size	Document Number: MS-16H7		Rev 1.1
Date:	Wednesday, July 08, 2015	Sheet 64 of 74	



CPU/GPU Holes
MCPU4 H_R200D150 GND X_CPU_HOLE
MCPU2 H_R200D150 GND X_CPU_HOLE
MCPU3 H_R200D150 GND X_CPU_HOLE
MCPU1 H_R200D150 GND X_CPU_HOLE
MGPU4 H_R276D169_PB GND X_CPU_HOLE
MGPU3 H_R276D169_PB GND X_CPU_HOLE
MGPU2 H_R276D169_PB GND X_CPU_HOLE
MGPU1 H_R276D169_PB GND X_CPU_HOLE
EMI
SPRING2 HS-MS-1721 GND E2M-7213211-CA7 ATE_C006_106
SPRING3 HS-MS1058 GND E2M-2142011-CA7 ATE_C006_106
SPRING1 HS-MS-1029 GND E23-1029060-CA7 ATE_C006_106
RUBBER1 E2Y-6H20713-Y40 RUBBER
BRACKET1 307-6H20111-C22 CPU_BRACKET
RUBBER2 E2Y-6H21312-Y40 RUBBER
BRACKET2 307-6H20111-C22 CPU_BRACKET
RUBBER3 E2Y-6H21312-Y40 RUBBER
BRACKET3 307-6H20211-C22 GPU_BRACKET
MYLAR1 E2P-6H22111-Y42 MYLAR
MYLAR2 E2P-6H24211-Y42 MYLAR
MYLAR3 E2P-6H22711-Y42 MYLAR
MYLAR4 E2P-6H23011-Y42 GPU MYLAR
MYLAR5 E2P-6H23111-Y42 GPU MYLAR
MYLAR6 E2P-6G13911-Y42 MYLAR
M1 X_H_R197D118_PT_V3 H_R197D118_PT_V3 GND
M8 X_H_R197D118_PT_V3 H_R197D118_PT_V3 GND
FM1 X_F_PAD_X
FM2 X_F_PAD_X
FM3 X_F_PAD_X
FM4 X_F_PAD_X
FM5 X_F_PAD_X
FM6 X_F_PAD_X
FM7 X_F_PAD_X
FM8 X_F_PAD_X
SSD Stand off
SSD 1
MH2 H_R220D146_PTB E2B-16H2020 GND
SSD 2
MH1 H_R220D146_PTB E2B-16H2020 GND
MH4 H_R197D91 X_ME_ SCREW HOLE GND
MH3 NPTH157 X_NPTH157
UME1 HDMI Lable HDMI ROYALTY Y01-RHDMI03-000
UME2 BIOS Lable BIOS_LABEL G51-LA01678-A09
PCB1 PF0-16H7111-H73
PF0-16H7111-H73
Hannstar: PF0-16H7111-H73
TRIPOD: PF0-16H7111-T53
MICRO-STAR INT'L CO.,LTD.
Title Screw/ME
Size Document Number MS-16H7 Rev 1.1
Date: Wednesday, July 08, 2015 Sheet 65 of 74

16H7-A Board (Audio CONN)



BTB Connector From MB
CONN Pin Current Capability : 0.5A/Pin
CONA1
BTB60PM_BLACK
N5C-60M0130-A81
FRONT OUT
SPDIF1 Gold N58-10F0071-H06 X_JACK_SPDIF_GOLD
SPDIF2 Black N58-09F0041-H06 X_JACK_SPDIF_BLACK
5010
CN1
JACK_SPDIF
SPDIF_MINI_JACK
MIC IN
MIC1 Gold N54-06F1191-H06 X_JACK_AUDIOF_GOLD
MIC2 Black N54-06F0481-H06 X_JACK-AUDIOF_BLACK
5010
CONA2
JACK-AUDIOF
JACK_AUD_D6_12
AMP
UA1
APA2031RI-TRL_TSSOP20-RH
SPDIF Power
QA1 P-APM2307AC-TRG_SOT23-3
QA2 N-2N7002_SOT23
QA3 N-2N7002_SOT23
EMI
Change to Cap
Change to Cap
BACK SPK CONN
CONA3
BH1X4#S-1.25PITCH_WHITE
N32-1040AV0-H06

For APA2031

Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

MICRO-STAR INT'L CO.,LTD.

Title: [A] Audio

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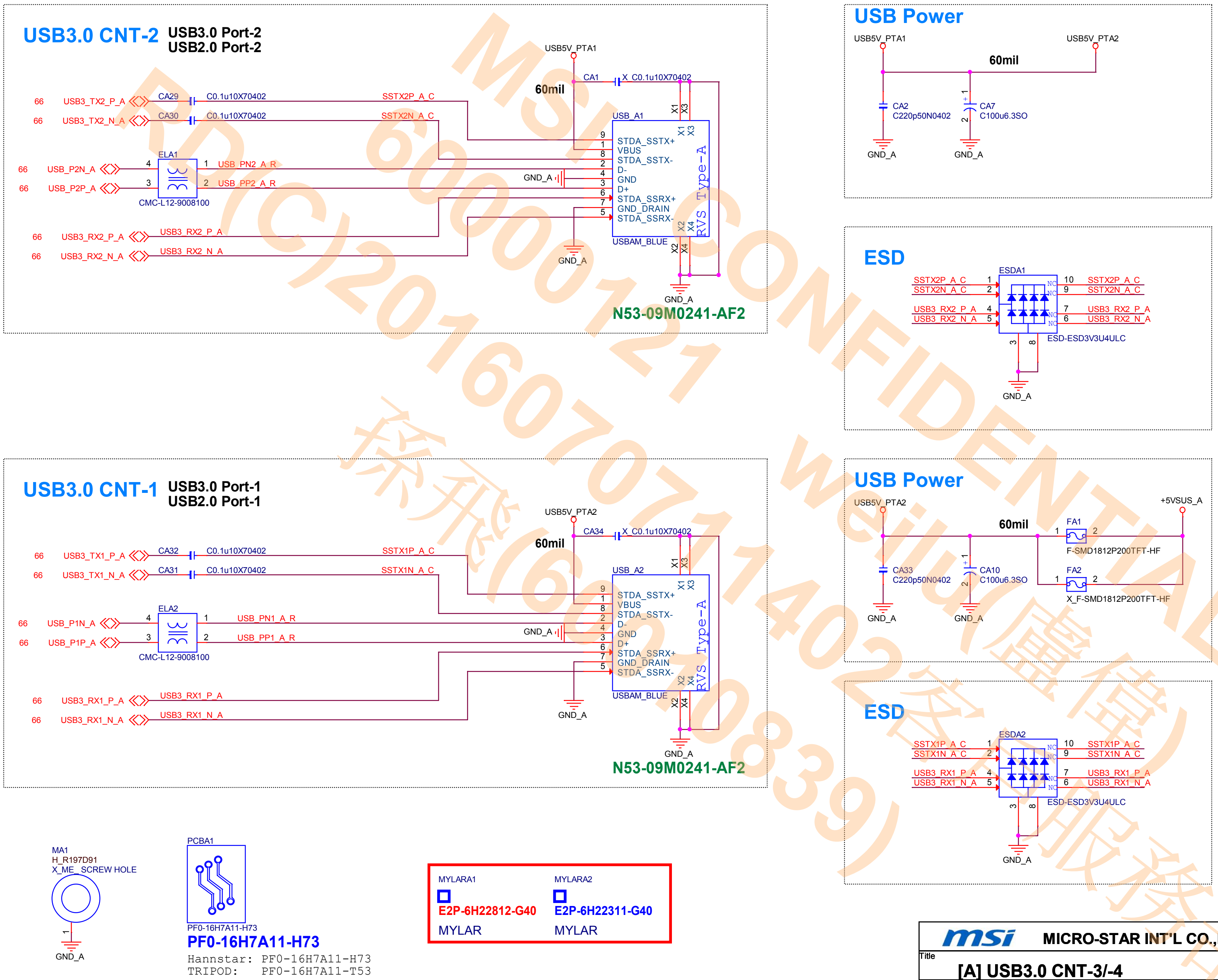
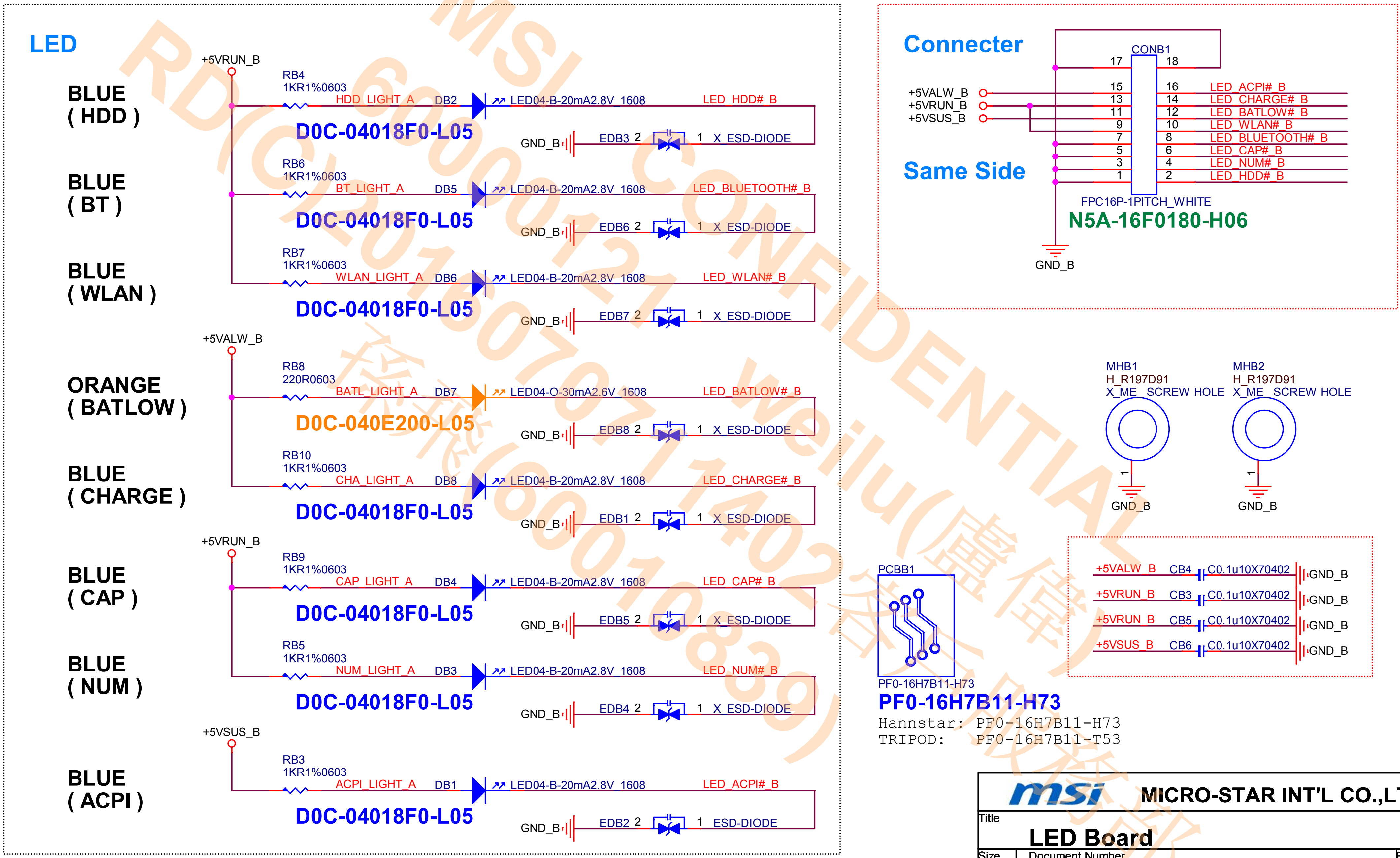
[A] USB3.0 CNT-2/-3



MICRO-STAR INT'L CO.,LTD.

Title	[A] USB3.0 CNT-3/-4	
Size	Document Number: MS-16H7	Rev 1.1
Date: Wednesday, July 08, 2015	Sheet 67 of 74	

16H7-B Board (LED Board)



MICRO-STAR INT'L CO.,LTD.

Title	LED Board	
Size	Document Number: MS-16H7	Rev 1.1
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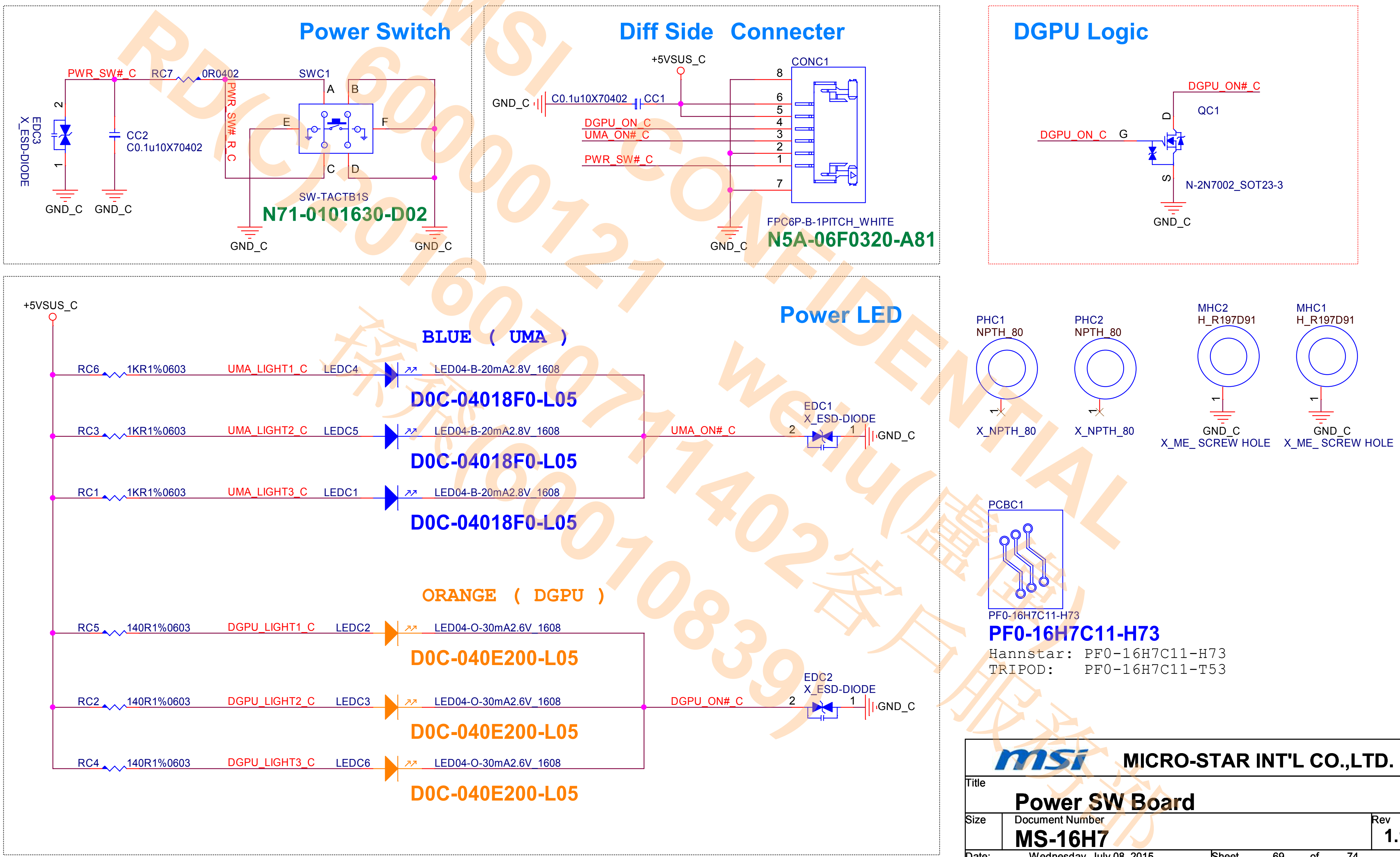
16H7-C Board (Power SW Board)



MICRO-STAR INT'L CO.,LTD.

Title: Power SW Board

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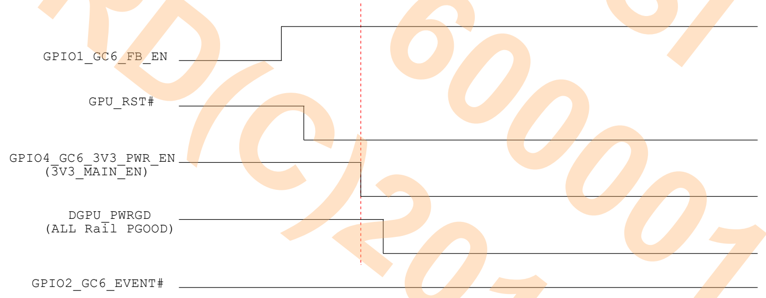
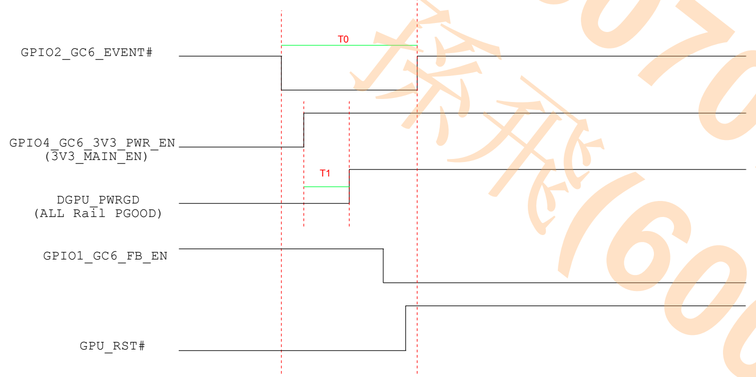
MS-16H7 DGPU POWER SEQUENCE

GC6 2.0 ENTRY SEQUENCE



GC6 2.0 EXIT SEQUENCE



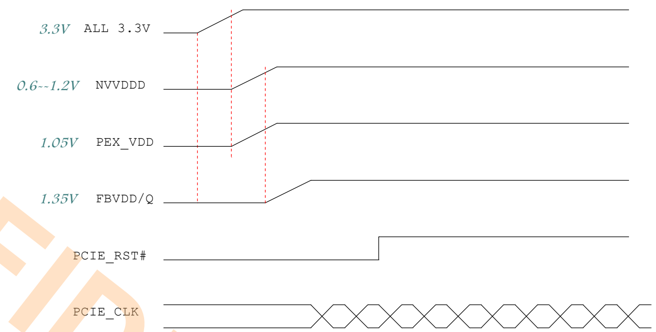
GC6 2.0 TIMING

	Min	Max	Unit	Description
T0	0.001	N/A	mS	GPU_EVENT# assertion
T1	0.04	4	mS	3V3_MAIN_EN assertion to all power rails up and stable

NOTES:

1. ALL RailPGOOD=1 represents all GPU power rails are ramped up and in regulation.
   If any GPU power rail cannot ge guaranteed in regulation this state should equal to 0.
2. During GC6 exit, the order of power rail ramp-up must follow the Power up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
3. All delays should be minimized to increase time spent in GC6 for maximum power saving.
4. The entire entry and exit sequence must complete within 200 ms.

GPU POWER ON SEQUENCE



NOTES:

1. The ramp time for any rail must be more than 40 us and is recommended to be less than 2ms.
2. The ramp up overshoot should not exceed the silicon reliability limit voltagr.
3. A VDD33 must ramp up to 90% before NVVDD and PEX_VDD in sequence can ramping up.
   NVVDD must ramp up to 90% before FBVDD/Q in sequence can ramping up.
3. No signal should be applied to the GPU before the power rails are fully ramped.
4. Refer to JEDEC Memory Specification for memory related power sequencing.

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Title: DGPU POWER SEQUENCE

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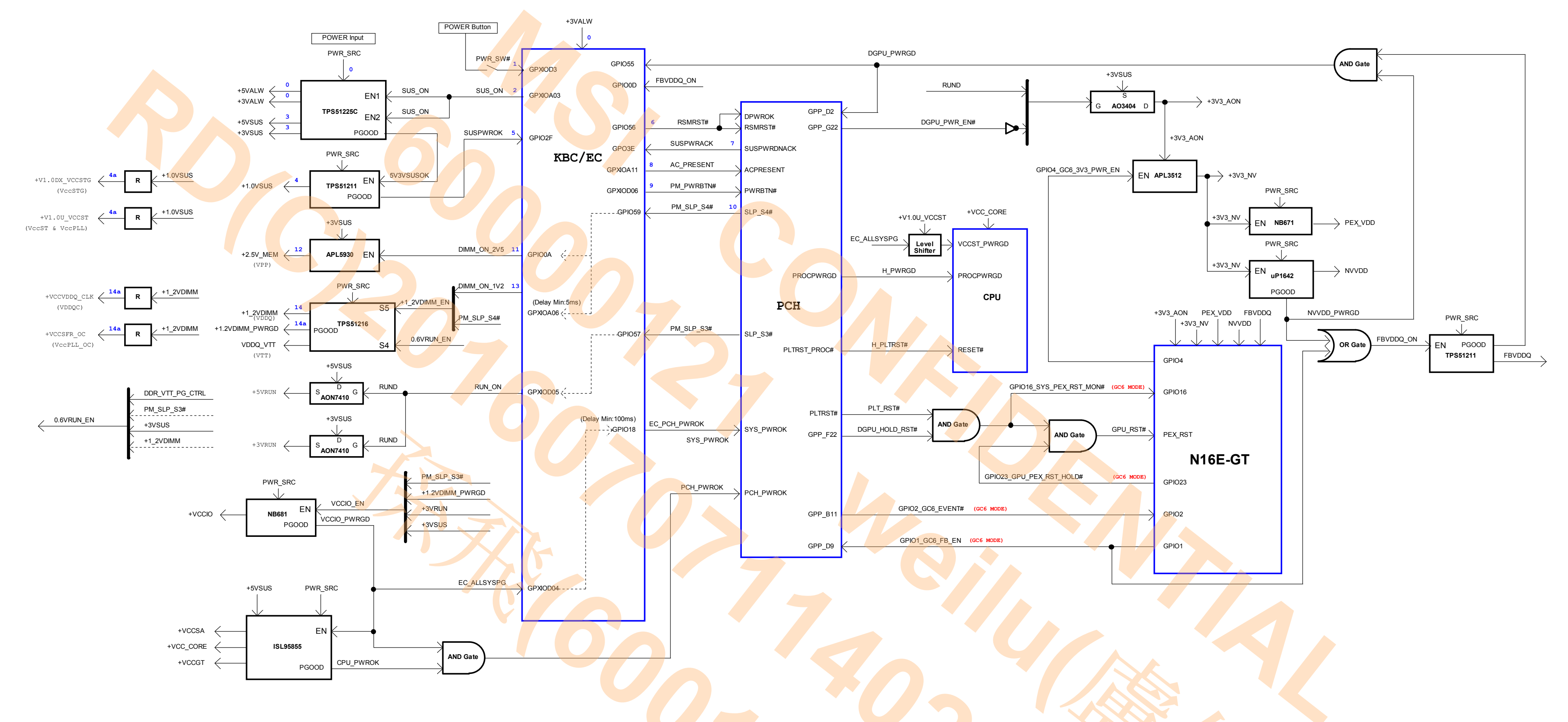
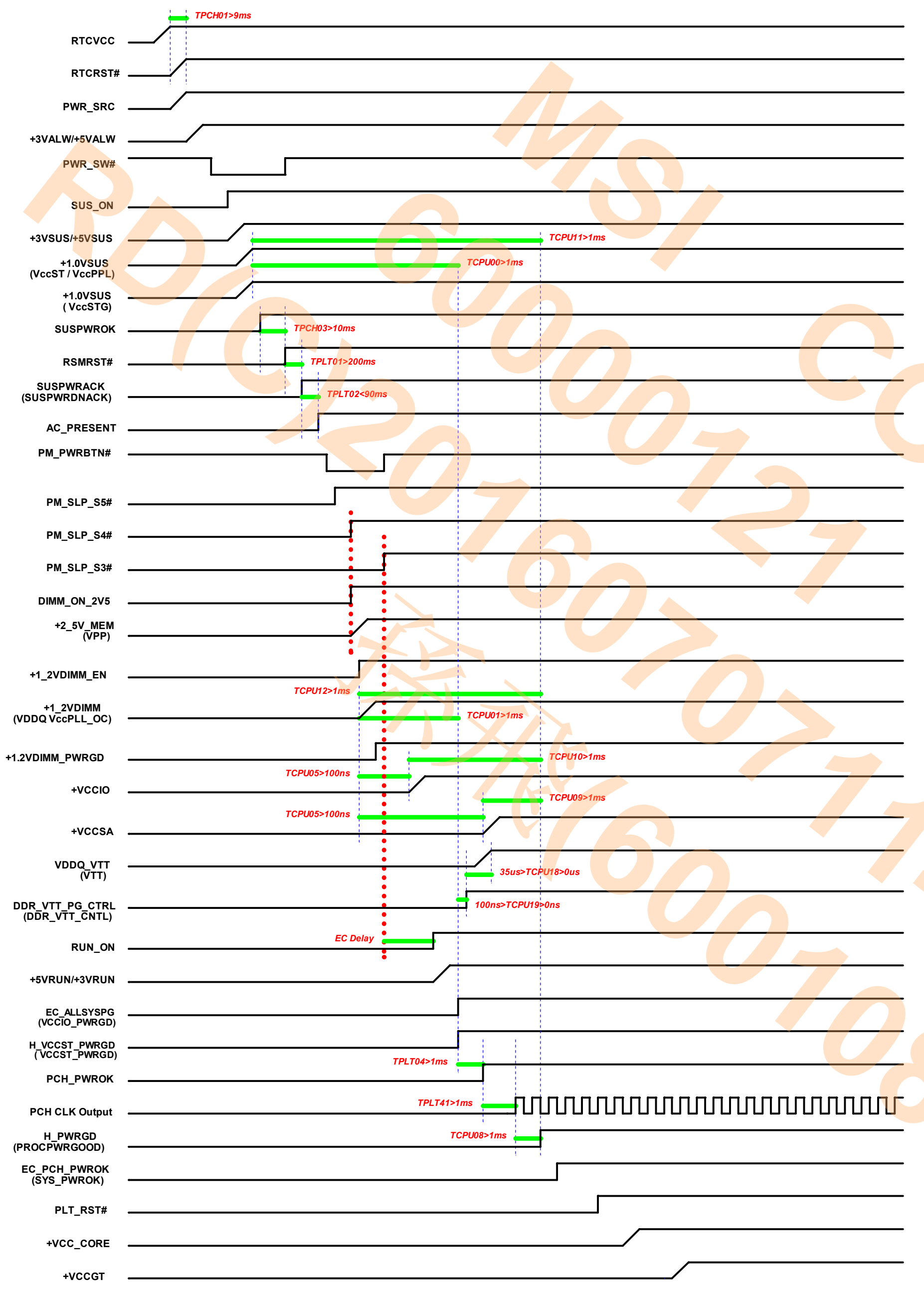
MS-16H7 Power On Block Diagram



MSI MICRO-STAR INT'L CO.,LTD.
Title: Power On Block Diagram
Document Number: MS-16H7
Rev 1.1
Date: Wednesday, July 06, 2016 Sheet 71 of 74

Power On Sequence

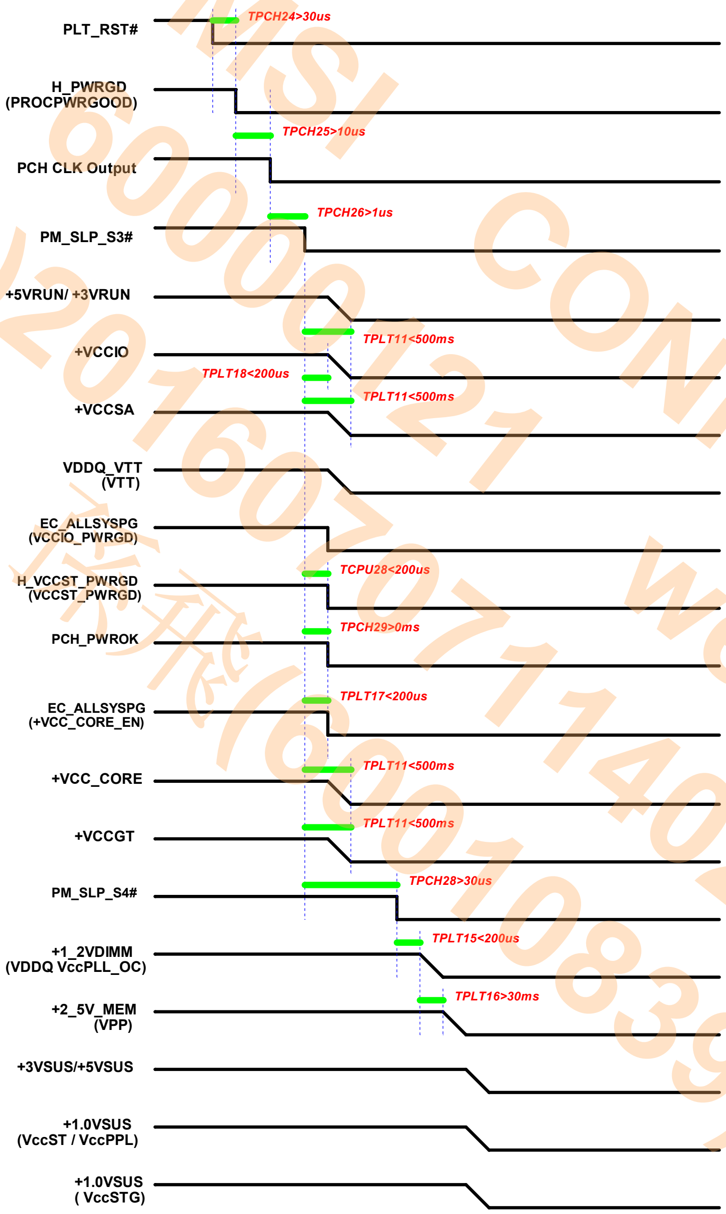
G3 -> S0



RTCVCC
RTCRST#
PWR_SRC
+3VALW/+5VALW
PWR_SW#
SUS_ON
+3VSUS/+5VSUS
+1.0VSUS
(VccST / VccPPL)
+1.0VSUS
(VccSTG)
SUSPWROK
RSMRST#
SUSPWRACK
(SUSPWRDNACK)
AC_PRESENT
PM_PWRBTN#
PM_SLP_S5#
PM_SLP_S4#
PM_SLP_S3#
DIMM_ON_2V5
+2_5V_MEM
(VPP)
+1_2VDIMM_EN
+1_2VDIMM
(VDDQ VccPLL_OC)
+1.2VDIMM_PWRGD
+VCCIO
+VCCSA
VDDQ_VTT
(VTT)
DDR_VTT_PG_CTRL
(DDR_VTT_CNTL)
RUN_ON
+5VRUN/+3VRUN
EC_ALLSYSPG
(VCCIO_PWRGD)
H_VCCST_PWRGD
(VCCST_PWRGD)
PCH_PWROK
PCH CLK Output
H_PWRGD
(PROCPWRGOOD)
EC_PCH_PWROK
(SYS_PWROK)
PLT_RST#
+VCC_CORE
+VCCGT
TPCH01>9ms
TCPU11>1ms
TCPU00>1ms
TPCH03>10ms
TPLT01>200ms
TPLT02<90ms
TCPU12>1ms
TCPU01>1ms
TCPU10>1ms
TCPU05>100ns
TCPU09>1ms
TCPU05>100ns
35us>TCPU18>0us
100ns>TCPU19>0ns
EC Delay
TPLT04>1ms
TPLT41>1ms
TCPU08>1ms

Power Down Sequence

S0 -> G3


PLT_RST#
TPCH24>30us
H_PWRGD
(PROCPWRGOOD)
TPCH25>10us
PCH CLK Output
TPCH26>1us
PM_SLP_S3#
+5VRUN/ +3VRUN
TPLT11<500ms
+VCCIO
TPLT18<200us
TPLT11<500ms
+VCCSA
VDDQ_VTT
(VTT)
EC_ALLSYSPG
(VCCIO_PWRGD)
TCPU28<200us
H_VCCST_PWRGD
(VCCST_PWRGD)
TPCH29>0ms
PCH_PWROK
TPLT17<200us
EC_ALLSYSPG
(+VCC_CORE_EN)
TPLT11<500ms
+VCC_CORE
TPLT11<500ms
+VCCGT
TPCH28>30us
PM_SLP_S4#
TPLT15<200us
+1_2VDIMM
(VDDQ VccPLL_OC)
TPLT16>30ms
+2_5V_MEM
(VPP)
+3VSUS/+5VSUS
+1.0VSUS
(VccST / VccPPL)
+1.0VSUS
(VccSTG)

History

1.0: 2015/5/18

01. P55 DEL PC148
    ADD PR264

02 P40 ADD R526
    ADD R527
    ADD R528
    ADD R529

03 P41 DEL ESD3
    DEL ESD4
    DEL ESD5
    ADD D4~D18

2015/5/22

01. P56 R220 to +3VSUS
    R219 to +3VSUS

2015/5/25

01. P58 ADD U45
    ADD R532
    ADD C606

02. P63 ADD U44
    ADD C604

03. P49 U1 PIN29 to GND

04. P58 ADD D19

05. P63 ADD D20

2015/5/25

01. P64 ADD EC64~EC68
    ADD EC69~EC72

1.1: 2015/6/26

01. P31 ADD PR265
    ADD PQ49

02 P40 ADD C916
    ADD C917
    ADD C918
    ADD C919

03 P49 C183 0402---->0603
    C184 0402---->0603
    C186 0402---->0603
    C189 0402---->0603

04 P55 PC132 0805----->1206

05 P64 ADD EC73~EC80

2015/7/2

01. P10 SOCKET2
    DDR4_SODIMM260P_H4_2---->DDR4_SODIMM260P_H4_5

02 P44 ADD R271

2015/7/3

01. P41 ADD R530
    ADD R531
    ADD R533
    DEL TPJNC50