Compal Confidential

ADL-P MB Schematic Document

LA-L651P

Rev: 1.0

2021.11.10

@ : Un-pop Component
@EMI@/@ESD@/@RF@ : EMI, ESD, RF Un-POP Component
EMI@/ESD@/RF@ : EMI, ESD, RF Component
JUMP@/JP@/PJP@ : JUMP
5VFAN@/12VFAN@ : JUMP for FAN power
XDP@ : XDP Component
CONN@ : Connector Component
SW@ : Debug PWR Button
CNV@/@CNV@ : CNVi Support
G3@ : EC G3 Flash Sharing
N18P@/GN20P@ : GPU Support
GN20P0@/GN20P1@ : P0 or P1 SKU
VS8GR3@/VM8GR3@/VH8GR1@ : VRAM SKU
VS@/VM@/VH@ : VRAM Support
BBY@ : BBY Support

ZZZ

PCB 3LP LA-L651P REV0 M/B S
DAB0009U000
AXIOM_PCB@

ZZZ

PCB 3LP LA-L659P REV0 M/B S
DAB000A8000
SIFMLK_PCB@

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Compal Electronics, Inc.			
Title: Cover Sheet			
Size: Custom	Document Number: LA-L651P		Rev: 0.2
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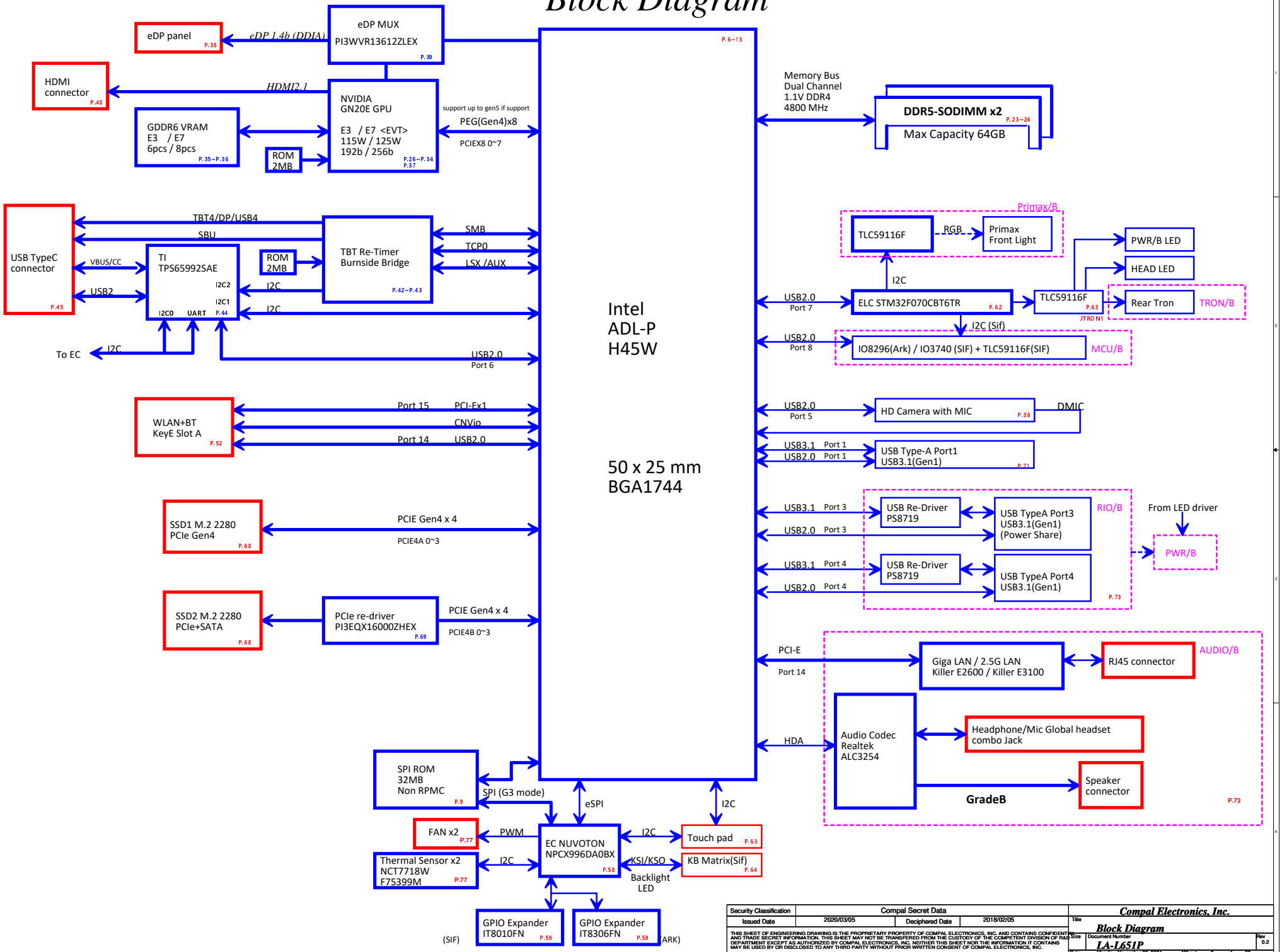
Block Diagram



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title: Block Diagram			
Size	Document Number: LA-L651P		Rev: 0.2
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Board ID table

Item	Pull-down	Pull-up	Voltage	Board ID/Model ID
1	100	10K	3.000	Pre-EVT
2	100	17.8K	2.801	EVT
3	100	27K	2.598	
4	100	37.4K	2.402	DVT1
5	100	49.9K	2.201	DVT2
6	100	64.9K	2.001	
7	100	82.5K	1.808	Pilot
8	100	107K	1.594	
9	100	154K	1.299	
10	100	200K	1.1	

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

PCH SMBUS Address Table

PCH_SMBUS Port	Power Rail	Device	Address
PCH_SMBCLK PCH_SMBDATA	+3VALW_PCH	JDIMM1	
		JDIMM2	

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address
GPU_THM_SMBCLK GPU_THM_SMBDAT	+3VS		
		Thermal 1	0x98h
		Thermal 2	0x9Ah
		GPU (GN20E)	0x9E
PBAT_CHG_SMBCLK PBAT_CHG_SMBDAT	+3VALW_EC	BAT	0x16
		CHGR	0x12
DAT_TP_SIO_I2C_CLK CLK_TP_SIO_I2C_DAT	+TP_VDD	Touch Pad	0x2C
UPD1_SMBCLK UPD1_SMBDAT	+3V_VSYS	CCG6SF	0x08

TGL-H-PCH H510

HSIO	USB3.2	PCIe	SATA3	Function
0	1			JUSB1
1	2			
2	3			JUSB (DB)
3	4			JUSB (DB)
4	5			
5	6			
6	7			
7	8			
8				
9				
10				
11				
12		7		
13				
14		9		JSSD2 , 2280 SATA x2 / PCIe x4
15		10		
16		11	0A	
17		12	1A	
18		13	0B	
19		14	1B	LAN
20		15		WLAN
21		16		
22		17		
23		18		
24		19		
25		20		
26		21		
27		22		
28		23		
29		24		

USB2	Function
1	JUSB1
2	
3	JUSB (DB)
4	JUSB (DB)
5	HD CAM
6	Type C
7	ELC MCU
8	4Zone MCU
9	
10	
11	
12	
13	
14	Bluetooth

TGL-H-CPU

PCIE4	Function
0	JSSD1 , 2280 PCIe x4 (GEN4)
1	
2	
3	

TCP0	Function
0	CPU side Type C
1	

Symbol Note :

Digital Ground

Analog Ground

60 mils/1A = 1/3 oz
40 mils/1A = 0.5 oz
20 mils/1A = 1 oz
10 mils/1A = 2 oz

Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5	DS3
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A	N/A
+12.6V_BATT+	Battery power supply	N/A	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A	N/A
+VCCIN	CPU FIVR input power supply	ON	OFF	OFF	OFF	OFF
+VCCIN_AUX	PCH FIVR input power supply	ON	OFF	OFF	OFF	OFF
+VCCIN_AUX_PCH	PCH power supply	ON	OFF	OFF	OFF	OFF
+3.3V_BAT_LDO	RTC power	ON	ON	ON	ON	ON
+RTC_CELL	+3.3V_BAT_LDO/+3VLP for suspend power	ON	ON	ON	ON	ON
+5VALW	System +5VALW power rail	ON	ON	ON	ON*	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+3VALW_PCH	+3VALW Primary Power Well for PCH	ON	ON	ON	ON*	OFF
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*	ON
+1.8V_PRIM	System +1.8V power rail	ON	ON	ON	ON*	OFF
+1.05VO_OUT_FET	System +1.05V power rail	ON	ON	ON	ON*	OFF
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	ON	OFF	ON
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+2.5V_MEM	DDR4 +2.5Vpp power rail	ON	ON	ON	OFF	ON
+1.05V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF	OFF
+1.05V_VCCSTG	Gated version of VCCST	ON	OFF	OFF	OFF	OFF
+5VS	System +5VS power rail	ON	ON	OFF	OFF	OFF
+3VS	System +3VS power rail	ON	ON	OFF	OFF	OFF
+1.8V_RUN	System +1.8VS power rail	ON	ON	OFF	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

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Title: Notes List

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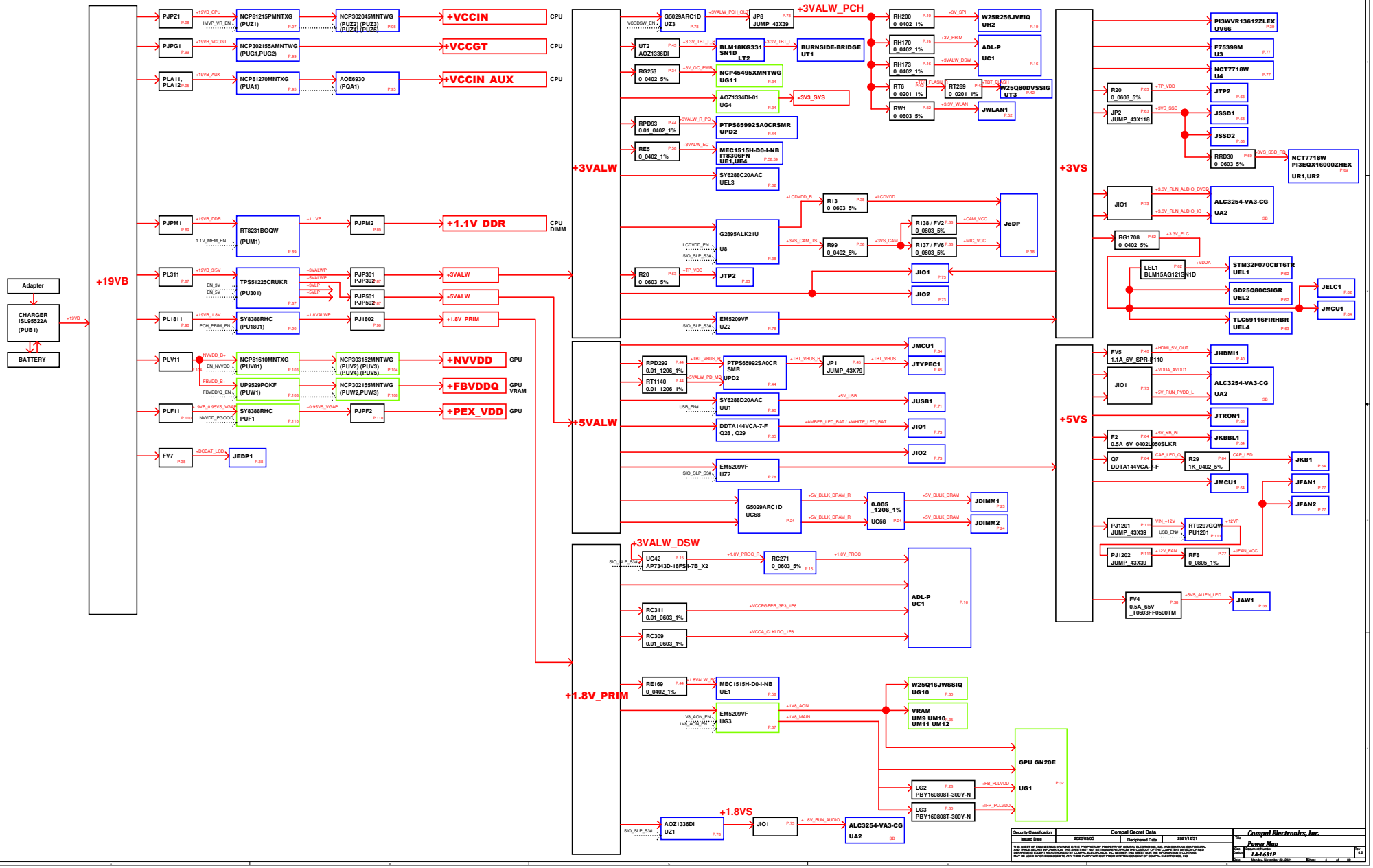
Adapter
CHARGER ISL95522A (PUB1)
BATTERY
+19VB
+19VB
+3VALW
+5VALW
+1.8V_PRIM
+3VALW_PCH
+3VALW_DSW
+1.8VS
+3VS
+5VS
+VCCIN
+VCCGT
+VCCIN_AUX
+1.1V_DDR
+NVVDD
+FBVDDQ
+PEX_VDD
NCP81215PMNTXG (PUZ1)
NCP302045MNTWG (PUZ2) (PUZ3) (PUZ4) (PUZ5)
NCP302155AMNTWG (PUG1,PUG2)
NCP81270MNTXG (PUA1)
AOE6930 (PQA1)
RT8231BGQW (PUM1)
TPS51225CRUKR (PU301)
SY8388RHC (PU1801)
NCP81610MNTXG (PUV01)
NCP303152MNTWG (PUV2) (PUV3) (PUV4) (PUV5)
UP5529PQKF (PUW1)
NCP302155MNTWG (PUW2,PUW3)
SY8388RHC PUF1
JEDP1
G5029ARC1D UZ3
BLM18KG331 SN1D LT2
BURNSIDE-BRIDGE UT1
NCP45495XMNTWG UG11
AOZ1334DI-01 UG4
PTPS65992SA0CRSMR UPD2
MEC1515H-D0-I-NB IT8306FN UE1,UE4
SY6288C20AAC UEL3
G2895ALK21U U8
JTP2
EM5209VF UZ2
PTPS65992SA0CR SMR UPD2
SY6288D20AAC UU1
DDTA144VCA-7-F Q28 , Q29
G5029ARC1D UC68
AP7343D-18FS4-7B_X2
ADL-P UC1
MEC1515H-D0-I-NB UE1
EM5209VF UG3
AOZ1336DI UZ1
ALC3254-VA3-CG UA2
GPU GN20E UG1
W25Q16JWSSIQ UG10
VRAM UM9 UM10 UM11 UM12
W25R256JVEIQ UH2
ADL-P UC1
W25Q80DVSSIG UT3
JWLAN1
PI3WVR13612ZLEX UV66
F75399M U3
NCT7718W U4
NCT7718W PI3EQX16000ZHEX UR1,UR2
ALC3254-VA3-CG UA2
STM32F070CBT6TR UEL1
GD25Q80CSIGR UEL2
TLC59116FIRHBR UEL4
JeDP
JHDMI1
JTRON1
JKBBL1
JKB1
JFAN1
JFAN2
JAW1
JMCU1
JUSB1
JTYPEC1
JDIMM1
JDIMM2
RT9297GQW PU1201
RF8 0_0805_1%
FV4 0.5A_65V_T0603FF0500TM
Compal Secret Data
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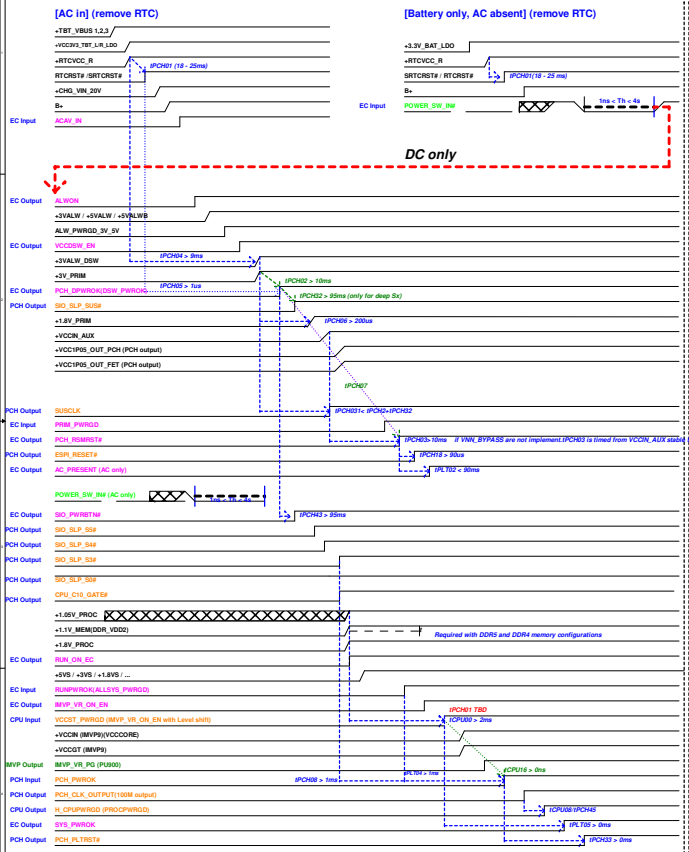
Power Map
LA-L451P

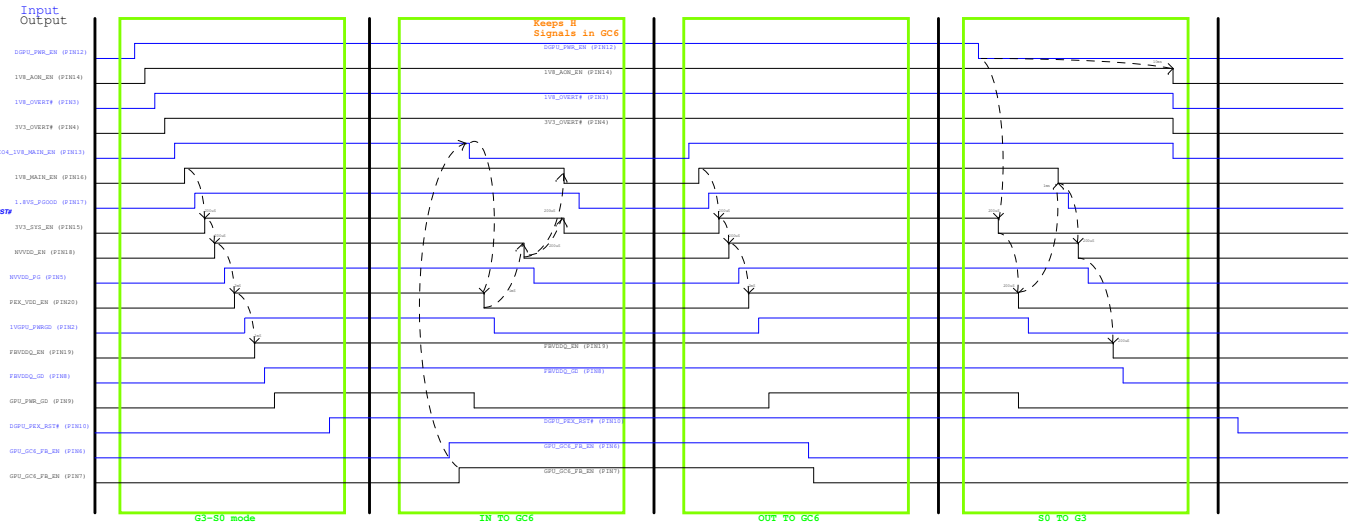
Power Sequence
G3 -> S0



Original power seuence is copied from Tributo ADLP

Modification
1. CPU_C10_GATE goes high earlier than VCCSTG(Need to check Modenat TGL power sequence report)
2. Add VCC1P8A signal
3. Net name need to aligened with Fiorano TGL-H

GPU squence



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Title	Power Sequence		
Size	Document Number		Rev
	LA-J451P		0.3
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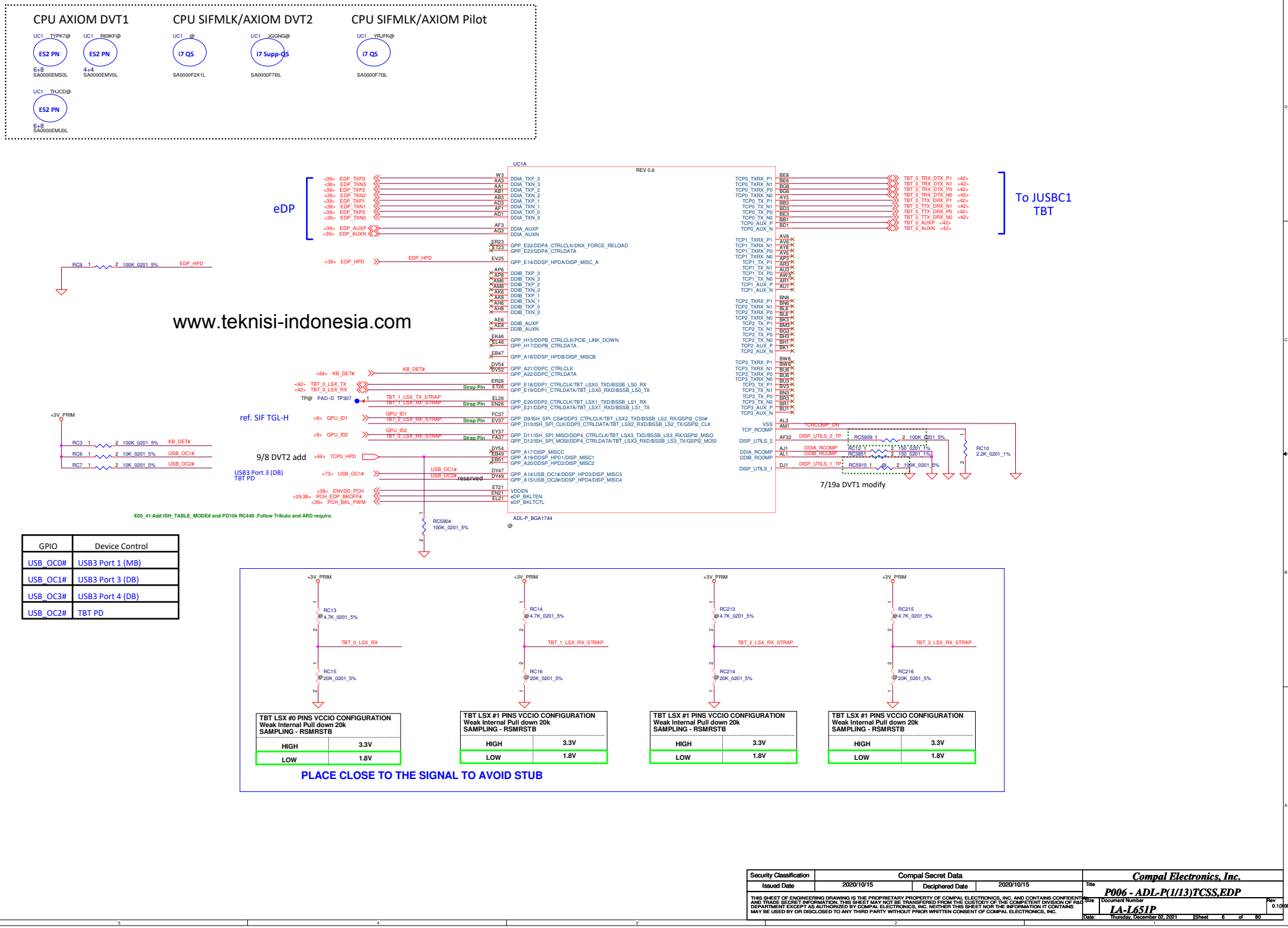

GPIO	Device Control
USB_OC0#	USB3 Port 1 (MB)
USB_OC1#	USB3 Port 3 (DB)
USB_OC3#	USB3 Port 4 (DB)
USB_OC2#	TBT PD

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	LA-L651P		0.1(00
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TOP SWAP OVERRIDE

GPP_B14 / SPKR (Internal 20 K Pull Down)

0 = Disable "Top Swap" mode. (Default)

1 = Enable "Top Swap" mode.

NO REBOOT

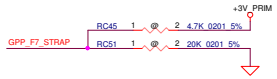
GPP_B18/GSPI0_MOS (Internal 20 K Pull Down)

0 = Disable "No Reboot" mode

1 = Enable "No Reboot" mode (This function is useful when running ITP/XDP).

Reserved

GPP_F7 (Weak internal PD 20K)



Reserved

GPP_F10 (Weak internal PD 20K)

BOOT STRAP 1

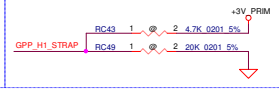
GPP_H0 (Weak internal PD 20K)

This bit 1 of a total of 4-bit encoded pin straps for boot configuration.

BOOT STRAP 2

GPP_H1 (Weak internal PD 20K)

This bit 2 of a total of 4-bit encoded pin straps for boot configuration.



BOOT STRAP 3

GPP_H2 (Weak internal PD 20K)

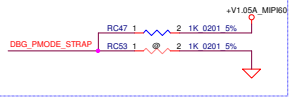
This is bit 3 of a total of 4-bit encoded pin straps for boot configuration.

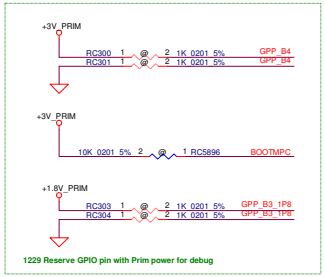
DFXTESTMODE(ITP_PMODE)

DBG_PMODE (Internal 20 K Pull UP)

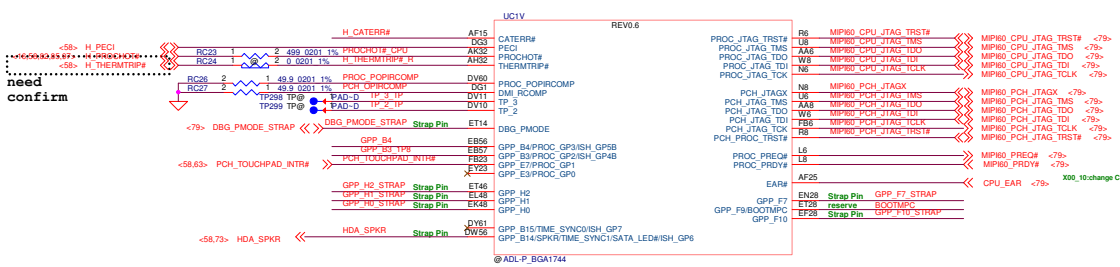
0 = DFXTESTMODE ENABLED

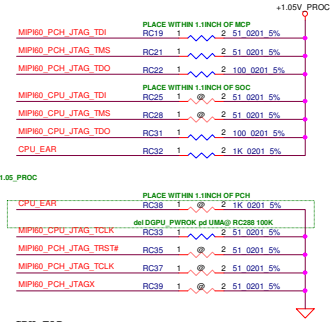
1 = DFXTESTMODE DISABLED(DEFAULT)





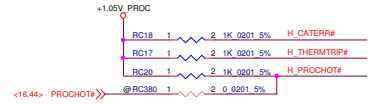
need confirm

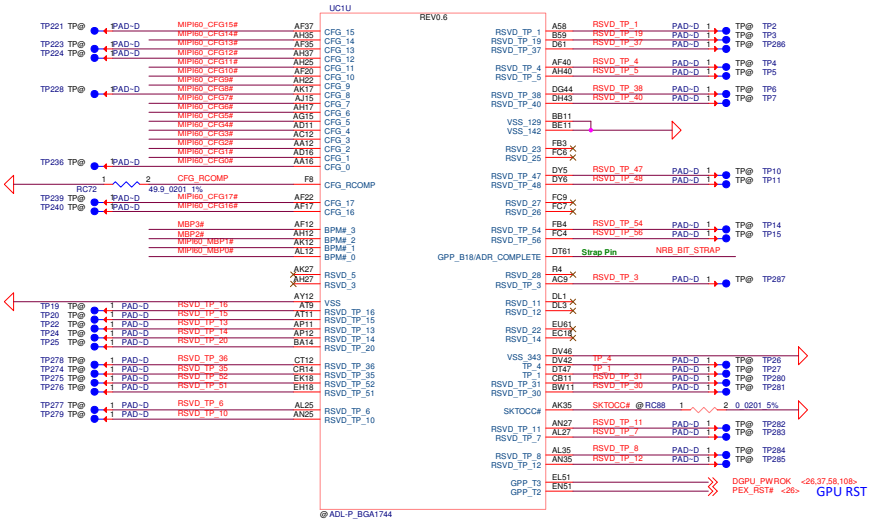




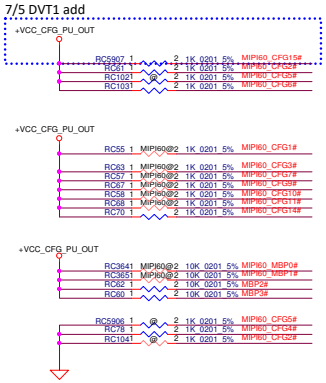
CPU_EAR

```
Stall CPU reset sequence until de-asserted
- 1 = (Default) Normal Operation; No stall
- 0 = Stall
```

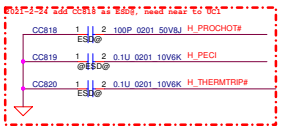




7/5 DVT1 add



ref. HORIZON



The ADL-P processor supports the configurations shown in the following tables:

Table 54. PCI Express* 8 - Lane Reversal Mapping

Bifurcation	Link Width		CFG Signals			Lanes							
	0:1:0	0:1:1	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7
PCIe controller						PCIe 010							
1x8	x8	N/A	1		1	0	1	2	3	4	5	6	7
1x8 **Reversed**	x8	N/A	1		0	7	6	5	4	3	2	1	0

Notes: 1. For CFG bus details, refer to Reset and Miscellaneous Signals on page 144.
2. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
3. For reversal lanes, for example: When using 1x4, the 4 lane device should use lanes 4:7, so lane 7 will be connected to lane 0 of the Device.

Table 56. ADL P PCI Express* 4 - Lane Reversal Mapping

Bifurcation	Link Width	CFG Signals	Lanes			
	0:6:0	CFG [14]	0	1	2	3
PCIe controller			PCIe 060			
1x4	x4	1	0	1	2	3
1x4 **Reversed**	x4	0	3	2	1	0
PCIe controller						PCIe 062
1x4	x4	1	0	1	2	3
1x4 **Reversed**	x4	0	3	2	1	0

11.4 Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[17:0]	Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • CFG[3:0]: Reserved configuration lanes. • CFG[4]: eDP enable: — 1 = Disabled. — 0 = Enabled. • CFG[6:5]: Reserved configuration lanes. • CFG[7]: PEG Training: — 1 = (default) PEG Train immediately following RESET# de-assertion. — 0 = PEG Wait for BIOS for training. • CFG[13:8]: Reserved configuration lanes. • CFG[14]: PEG60 Lane Reversal — 1 - (Default) Normal — 0 - Reversed • CFG[17:15]: Reserved configuration lanes.	I	GTL	SE	S-Processor Line P-Processor Line

Compal Electronics, Inc.
Title: P007 - ADL-P(2/13)MISC,MIPI60
Size: Document Number: LA-L651P Rev: 0.1(X00)
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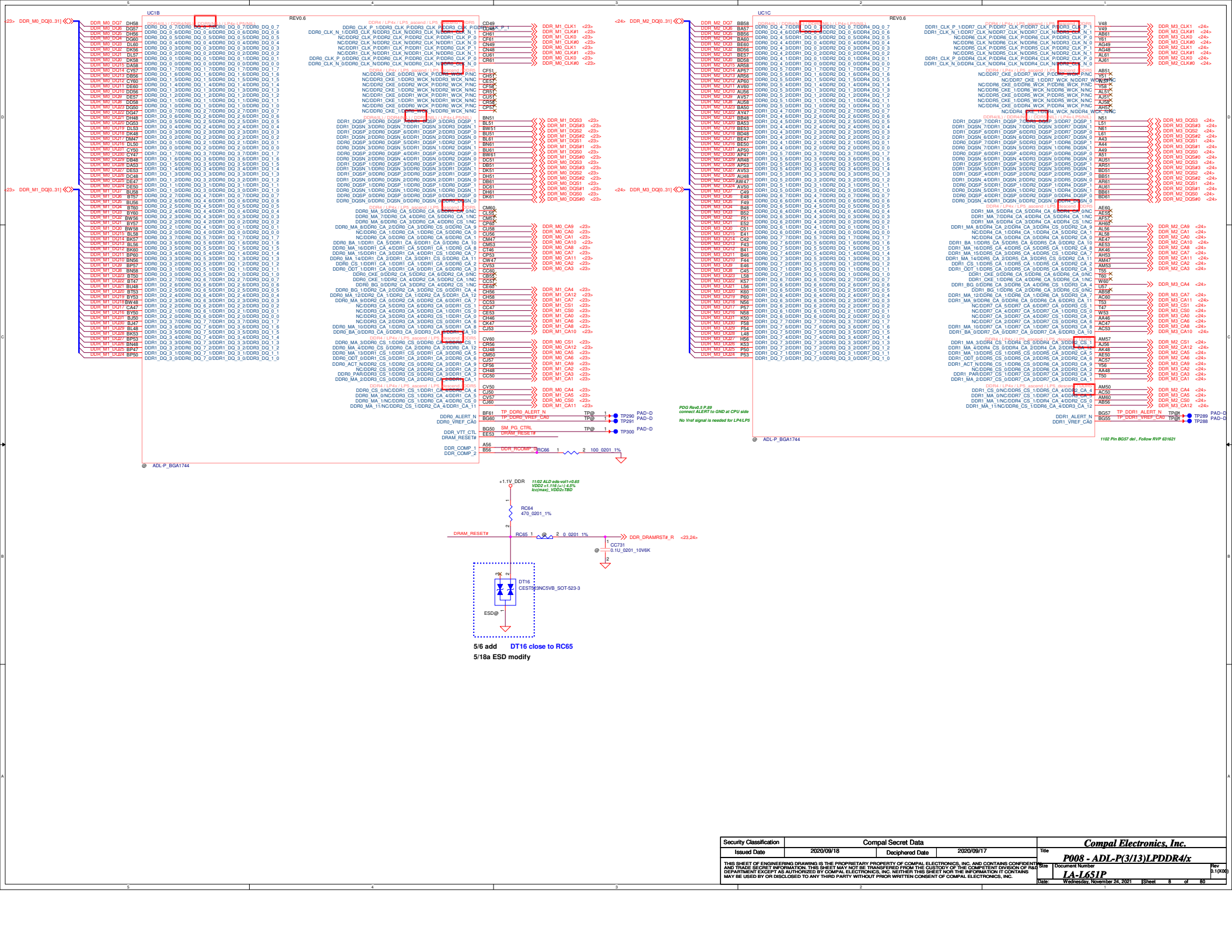

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/09/18	Deciphered Date 2020/09/17	Title P008 - ADL-P(3/13)LPDDR4/x
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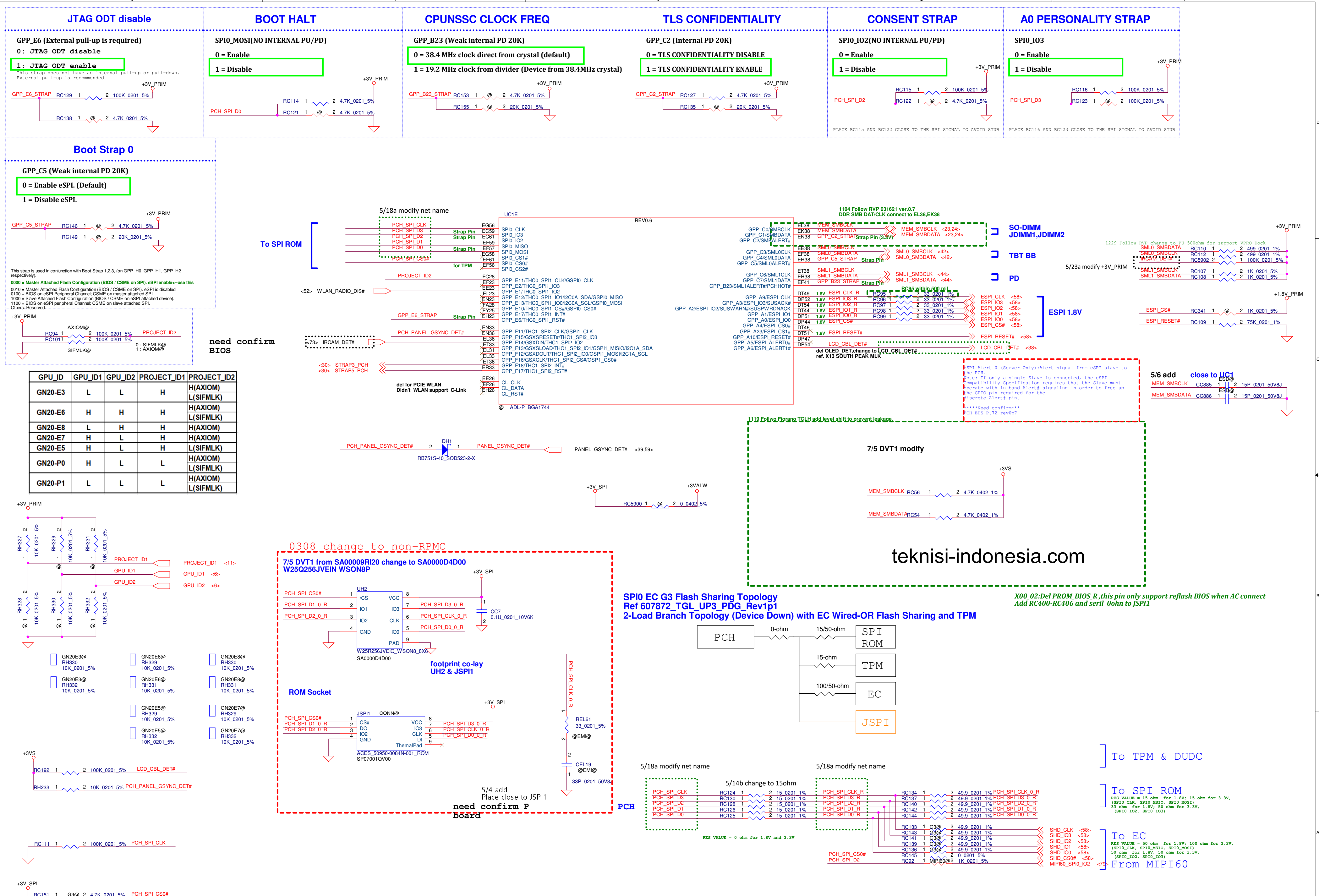


JTAG ODT disable
GPP_E6 (External pull-up is required)
0: JTAG ODT disable
1: JTAG ODT enable
This strap does not have an internal pull-up or pull-down. External pull-up is recommended
BOOT HALT
SPI0_MOSI(NO INTERNAL PU/PD)
0 = Enable
1 = Disable
CPUNSSC CLOCK FREQ
GPP_B23 (Weak internal PD 20K)
0 = 38.4 MHz clock direct from crystal (default)
1 = 19.2 MHz clock from divider (Device from 38.4MHz crystal)
TLS CONFIDENTIALITY
GPP_C2 (Internal PD 20K)
0 = TLS CONFIDENTIALITY DISABLE
1 = TLS CONFIDENTIALITY ENABLE
CONSENT STRAP
SPI0_IO2(NO INTERNAL PU/PD)
0 = Enable
1 = Disable
PLACE RC115 AND RC122 CLOSE TO THE SPI SIGNAL TO AVOID STUB
A0 PERSONALITY STRAP
SPI0_IO3
0 = Enable
1 = Disable
PLACE RC116 AND RC123 CLOSE TO THE SPI SIGNAL TO AVOID STUB
Boot Strap 0
GPP_C5 (Weak internal PD 20K)
0 = Enable eSPI. (Default)
1 = Disable eSPI.
This strap is used in conjunction with Boot Strap 1,2,3, (on GPP_H0, GPP_H1, GPP_H2 respectively).
0000 = Master Attached Flash Configuration (BIOS / CSME on SPI). eSPI enable<--use this
0010 = Master Attached Flash Configuration (BIOS / CSME on SPI). eSPI is disabled
0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI.
1000 = Slave Attached Flash Configuration (BIOS / CSME on eSPI attached device).
1100 = BIOS on eSPI peripheral Channel; CSME on slave attached SPI.
Others: Reserved.
need confirm BIOS
5/18a modify net name
To SPI ROM
UC1E
ADL-P_BGA1744
1104 Follow RVP 631621 ver.0.7
DDR SMB DAT/CLK connect to EL38,EK38
SO-DIMM
JDIMM1,JDIMM2
TBT BB
PD
ESPI 1.8V
5/23a modify +3V_PRIM
1229 Follow RVP change to PU 500ohm for support VPRO Dock
del for PCIE WLAN
Didn't WLAN support C-Link
del OLED_DET,change to LCD_CBL_DET#
ref. X13 SOUTH PEAK MLK
eSPI Alert 0 (Server Only):Alert signal from eSPI slave to the PCH.
Note: If only a single Slave is connected, the eSPI Compatibility Specification requires that the Slave must operate with in-band Alert# signaling in order to free up the GPIO pin required for the discrete Alert# pin.
****Need confirm***
PCH EDS P.72 rev0p7
5/6 add close to UC1
1119 Follow Florano TGLH add level shift to prevent leakage
7/5 DVT1 modify
teknisi-indonesia.com
0308 change to non-RPMC
7/5 DVT1 from SA00009RI20 change to SA0000D4D00
W25Q256JVEIN WSON8P
footprint co-lay
UH2 & JSPI1
ROM Socket
5/4 add
Place close to JSPI1
need confirm P board
SPI0 EC G3 Flash Sharing Topology
Ref 607872_TGL_UP3_PDG_Rev1p1
2-Load Branch Topology (Device Down) with EC Wired-OR Flash Sharing and TPM
X00_02:Del PROM_BIOS_R ,this pin only support reflash BIOS when AC connect
Add RC400-RC406 and seril 0ohn to JSPI1
PCH
SPI ROM
TPM
EC
JSPI
0-ohm
15/50-ohm
15-ohm
100/50-ohm
5/18a modify net name
5/14b change to 15ohm
RES VALUE = 0 ohm for 1.8V and 3.3V
To TPM & DUDC
To SPI ROM
RES VALUE = 15 ohm for 1.8V; 15 ohm for 3.3V, (SPI0_CLK, SPI0_MSIO, SPI0_MOSI)
33 ohm for 1.8V; 50 ohm for 3.3V, (SPI0_IO2, SPI0_IO3)
To EC
RES VALUE = 50 ohm for 1.8V; 100 ohm for 3.3V, (SPI0_CLK, SPI0_MSIO, SPI0_MOSI)
50 ohm for 1.8V; 50 ohm for 3.3V, (SPI0_IO2, SPI0_IO3)
From MIPI60

GPU_ID	GPU_ID1	GPU_ID2	PROJECT_ID1	PROJECT_ID2
GN20-E3	L	L	H	H(AXIOM) L(SIFMLK)
GN20-E6	H	H	H	H(AXIOM) L(SIFMLK)
GN20-E8	L	H	H	H(AXIOM)
GN20-E7	H	L	H	H(AXIOM)
GN20-E5	H	L	H	L(SIFMLK)
GN20-P0	H	L	L	H(AXIOM) L(SIFMLK)
GN20-P1	L	L	L	H(AXIOM) L(SIFMLK)

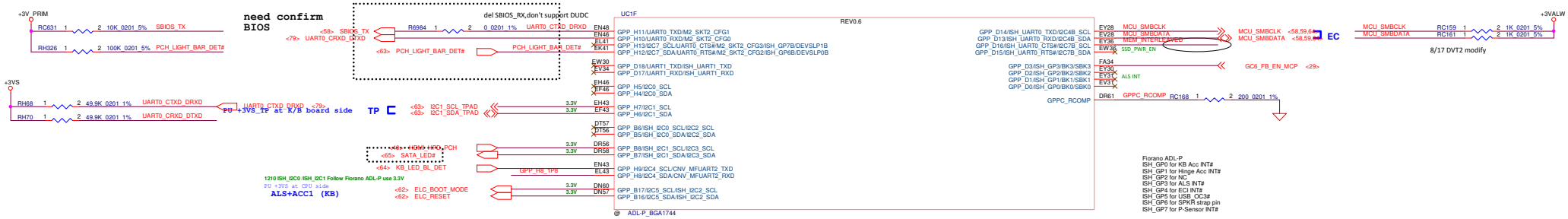
Security Classification	Compal Secret Data		
Issued Date	2020/10/15	Deciphered Date	2020/10/15

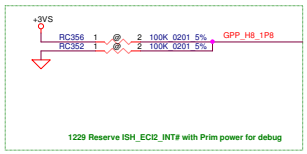
Compal Electronics, Inc.

Title: P009 - ADL-P(4/13)SPI,SMB,ESPI

Document Number: LA-L651P — Rev 0.1(X00)

Date: Monday, February 21, 2022 — Sheet 9 of 80



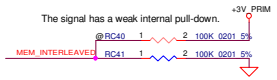


DIMM TYPE

1 : Interleave

0 : Non-Interleave

The signal has a weak internal pull-down.

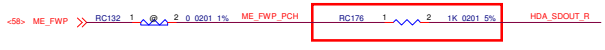


FLASH DESCRIPTOR SECURITY OVERRIDE

GPP_R2/HDA_SDO (Internal 20 K Pull Down)

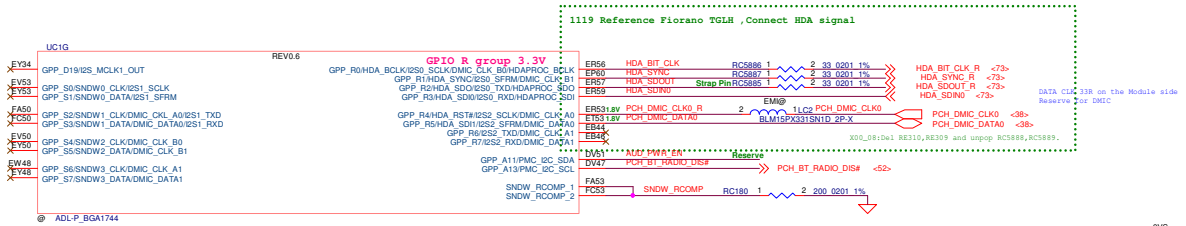
0 = ENABLE (DEFAULT)

1 = DISABLE (ME can update)

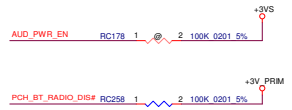


1228 need check follow Fiorano TGLH or CSLP

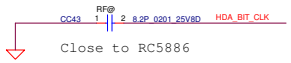
1119 Reference Fiorano TGLH ,Connect HDA signal



S Group 1.8V only



5/5b add



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/10/15	Deciphered Date 2020/10/15	Title: P010 - ADL-P(5/13)HDA,I2C,ISH

Size	Document Number	Rev
	LA-L651P	0.1(X00)
Date: Wednesday, November 24, 2021	Sheet 10 of 80	

STRAP FOR SPI 1.8V/3.3V SEL

SPIVCCIOSEL

0 = SPI voltage is 3.3V (4.7 k pull-down to GND)

1 = SPI voltage is 1.8V (4.7K pull-up to DSW_PWROK)

Reserved

Weak Internal PD 20k.
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

X00_43:Customer request Reference CSLP
PCIE:CR 7->4
PCIE:WLAN 8->12
PCIE CLK:WLAN 2->1
PCIE CLK:CR 1->2
PCIE CLK:SSD 3->0
PCIE CLK:GPU 0->3

Gen4 SSD2
Gen4 PEG
LAN
WLAN
Gen4 SSD1

need confirm BIOS

8/17 DVT2 modify

PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification
compliant differential output clocks to PCIe* devices

and Gen3 support

support

5/18 add

5/4a add

CPU Type	Config		SYSTEM_ID1	SYSTEMID_2	SYSTEM_ID3
			BID_DIS	XPS or Precision (BID_BC)	P1 or P3 (BID_GPU)
IGFX	XPS	UMA	H	L	L
	Precision	UMA	H	H	L
DGPU	XPS	GN20-P1			
		N20Z-QS1-A1(DVT1)	L	L	L
		QN20-P1	L	H	H
	Precision	QN20-P3			
		N20Z-QS1-A1(DVT1)	L	H	L

PDG_An RC delay circuit with a time delay in the range of 18 - 25 ms should be provided. The circuit should be connected to VCCRTC.

PLACE RC245 and RC248 CLOSE TO MCP - WITHIN 100mils

5/5b add close to UC1

ESD Request:place near CPU side

PCH GLITCH ISSUE MITIGATION(PDG p.112)

PLTRST#

5/22 modify

X00_28:Follow CSLP and RVP7.2.

ref. SIF TGL

X01_04:Follow 631621_ADL_P_DDR5_SODIMM_1DPC_T3_RVP_SCH_REV1P1 pull down 100k

7/19a add

need confirm

1119 Dell request Del SYS_RESET# UC29 AND Gate,follow tributo remove it.

5/11 follow intel pull up 1M

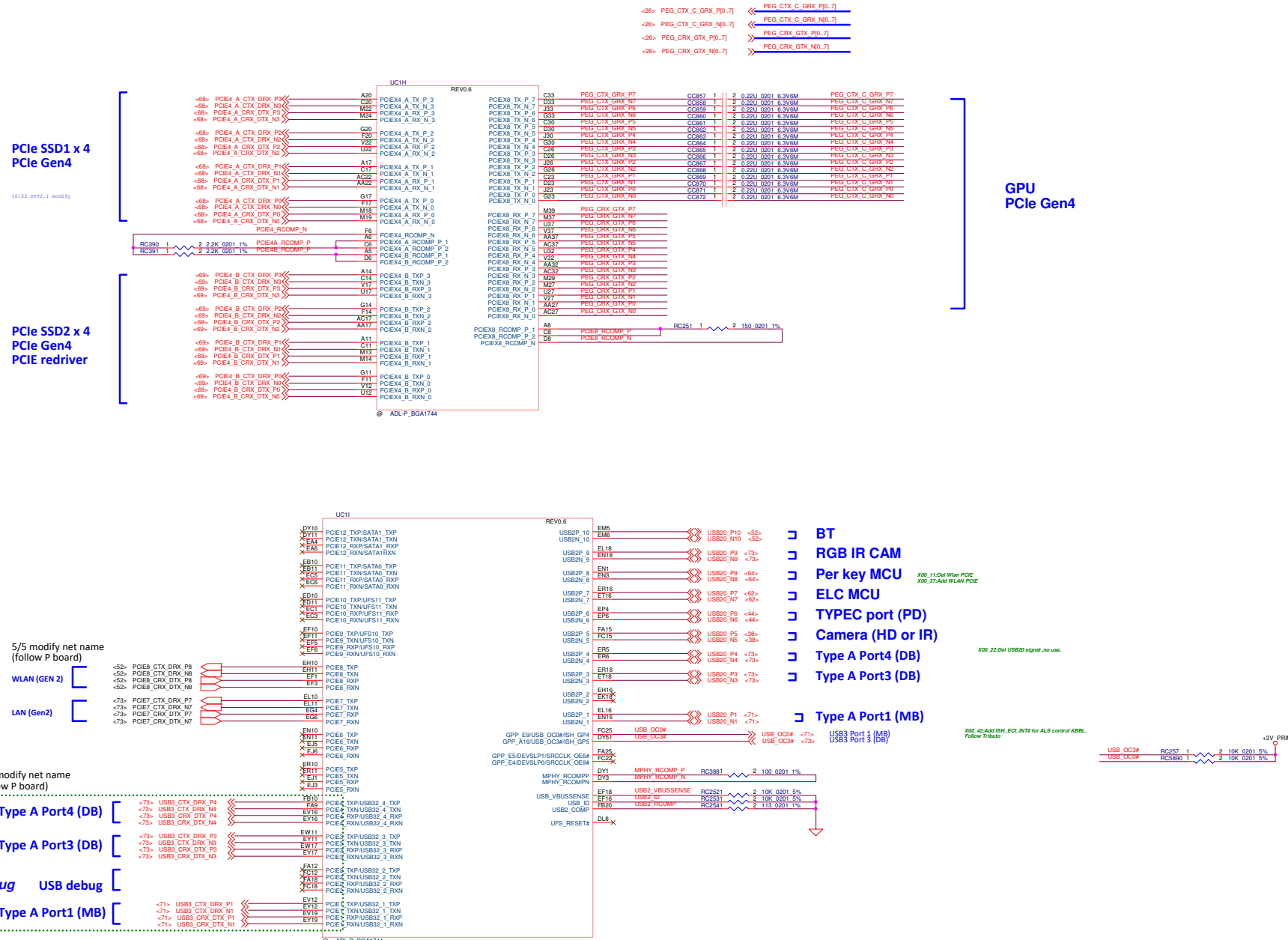
Security Classification	Compal Secret Data		
Issued Date	2020/10/15	Deciphered Date	2020/10/15

Compal Electronics, Inc.

Title: P011 - ADL-P(6/13)CLK,GPIO

Size: | Document Number: LA-L651P | Rev: 0.1(X00)

Date: Wednesday, November 24, 2021 | Sheet 11 of 80



Security Classification	Compal Secret Data		
Issued Date	2020/10/15	Deciphered Date	2020/10/15

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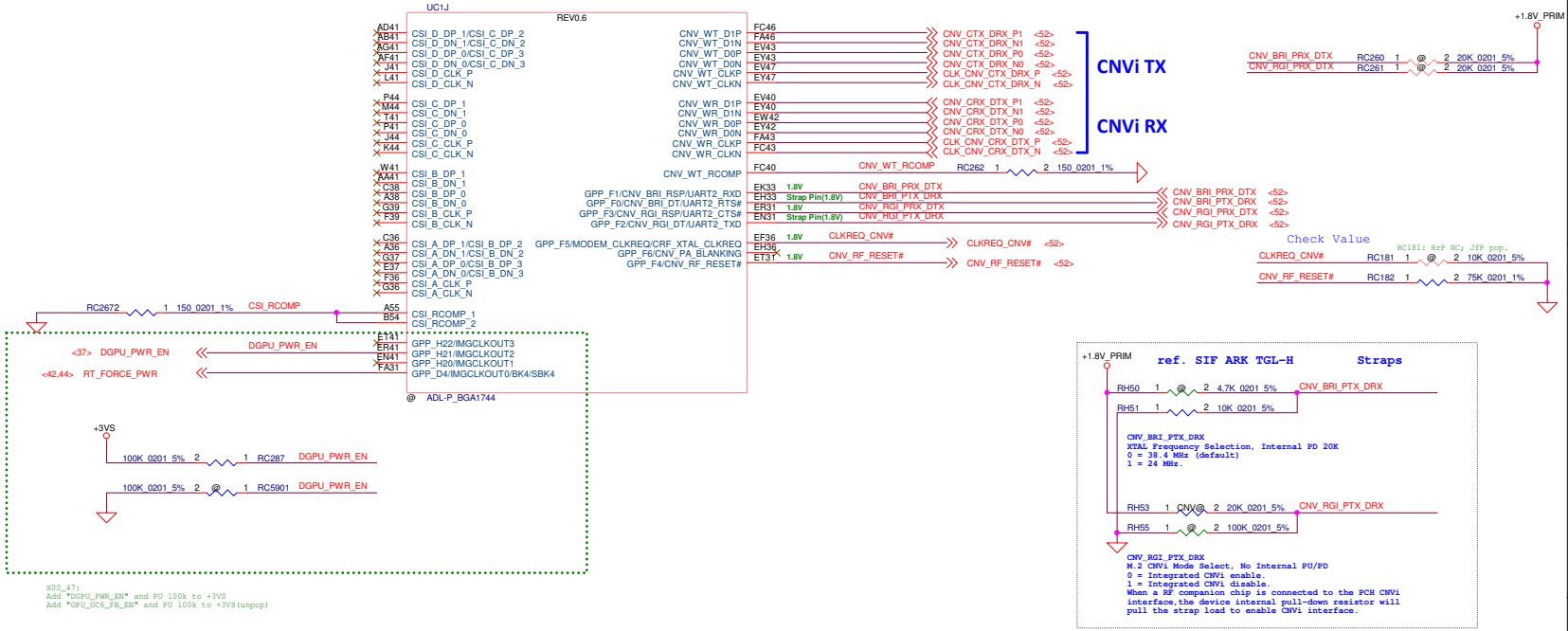
Compal Electronics, Inc.

Title: P012 - ADL-P(7/13)PCIE,USB

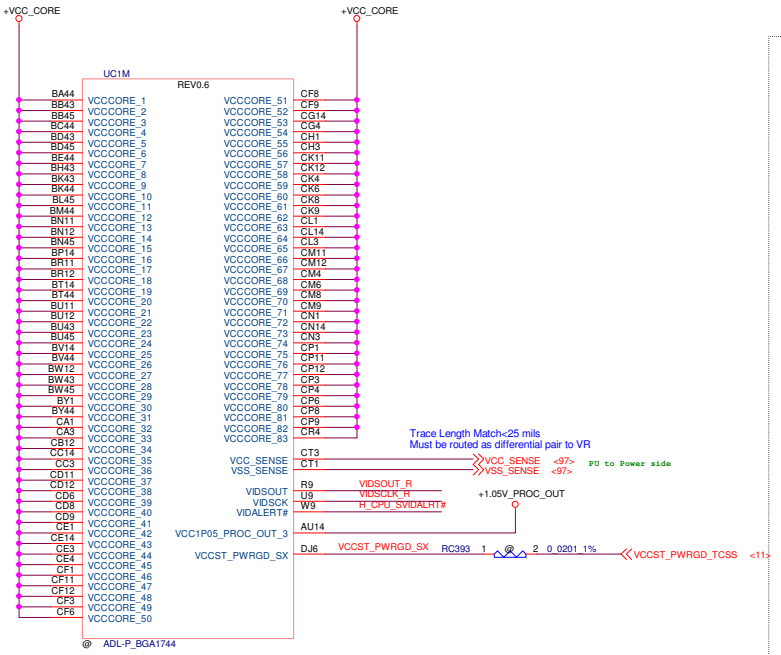
Size: | Document Number: LA-L651P | Rev: 0.1(X00)

Date: Thursday, February 10, 2022 | Sheet 12 of 80



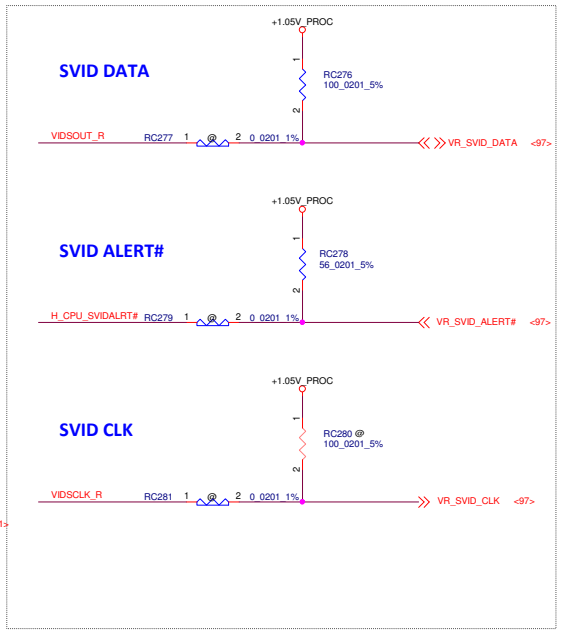
Security Classification	Compal Secret Data		
Issued Date	2020/10/15	Deciphered Date	2020/10/15

Compal Electronics, Inc.	
Title	P013 - ADL-P(8/13)CSI,CNVi
Size	Document Number: LA-L651P
Rev	0.1(X00)
Date: Monday, November 22, 2021	Sheet 13 of 80



1.Route the Alert signal between the Clock and the Data signals.

CAD Note:
1.Place the PUresistors close to CPU. And breakout as 2 traces.
2.Place the PU resistors close to CPU



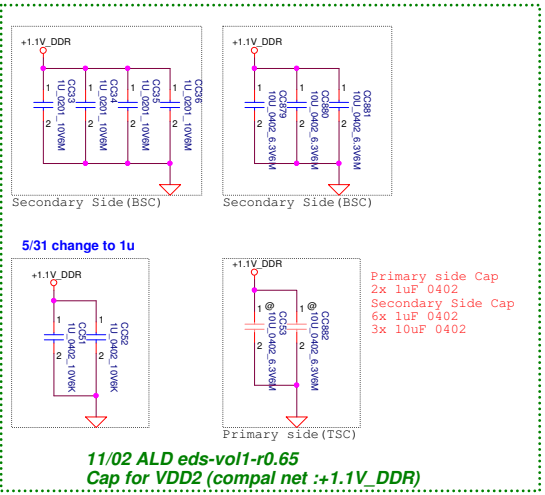
Security Classification	Compal Secret Data		
Issued Date	2020/10/15	Deciphered Date	2020/10/15

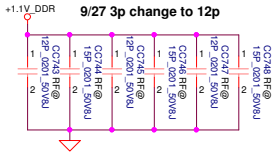
Compal Electronics, Inc.

Title: P014 - ADL-P(9/13)CPU PWR,SVID

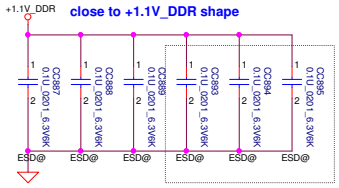
Size: LA-L651P | Document Number | Rev: 0.1(X00)

Date: Wednesday, November 24, 2021 | Sheet 14 of 80

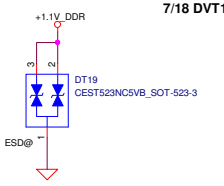




5/6 add



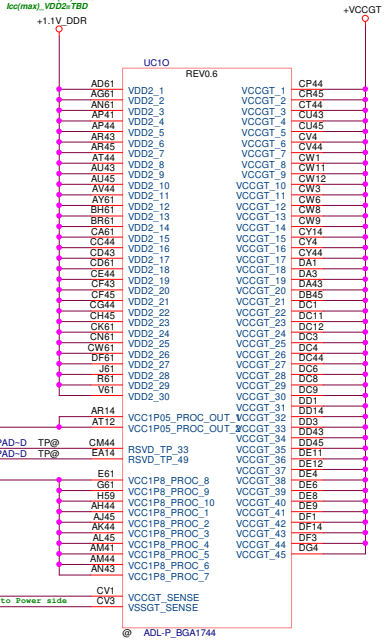
7/18 DVT1 add



5/6 add DT19 close to CC33

12/13 DVT2 modify
ESD request

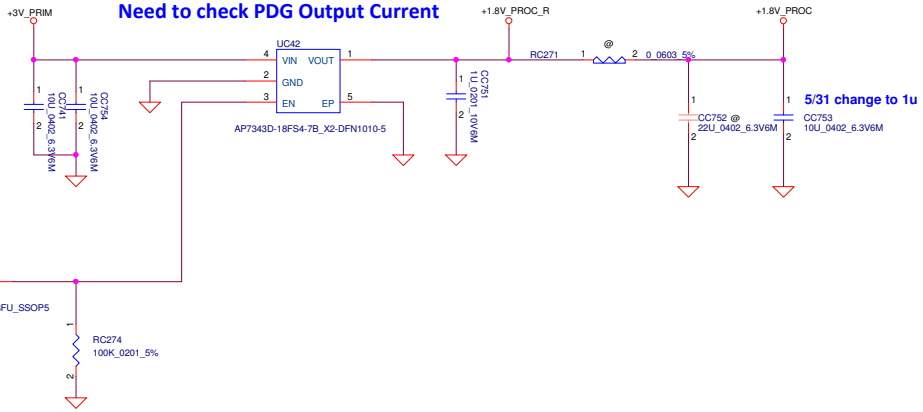
11/02 ALD eds-vol1-r0.65
VDD2 =1.116 (+/-) 4.5%
Icc(max), VDD2=TBD

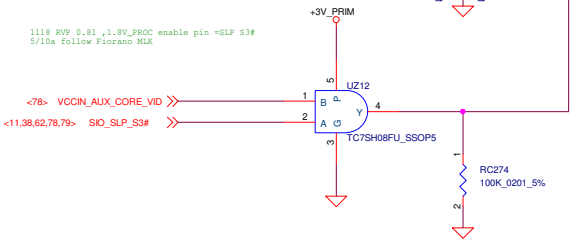


1105 Ref PDG627205
Layout notice:
VCC1p8_PROC LDO output to inner BGA pins near AM41 not exceed

VCC1P8_PROC

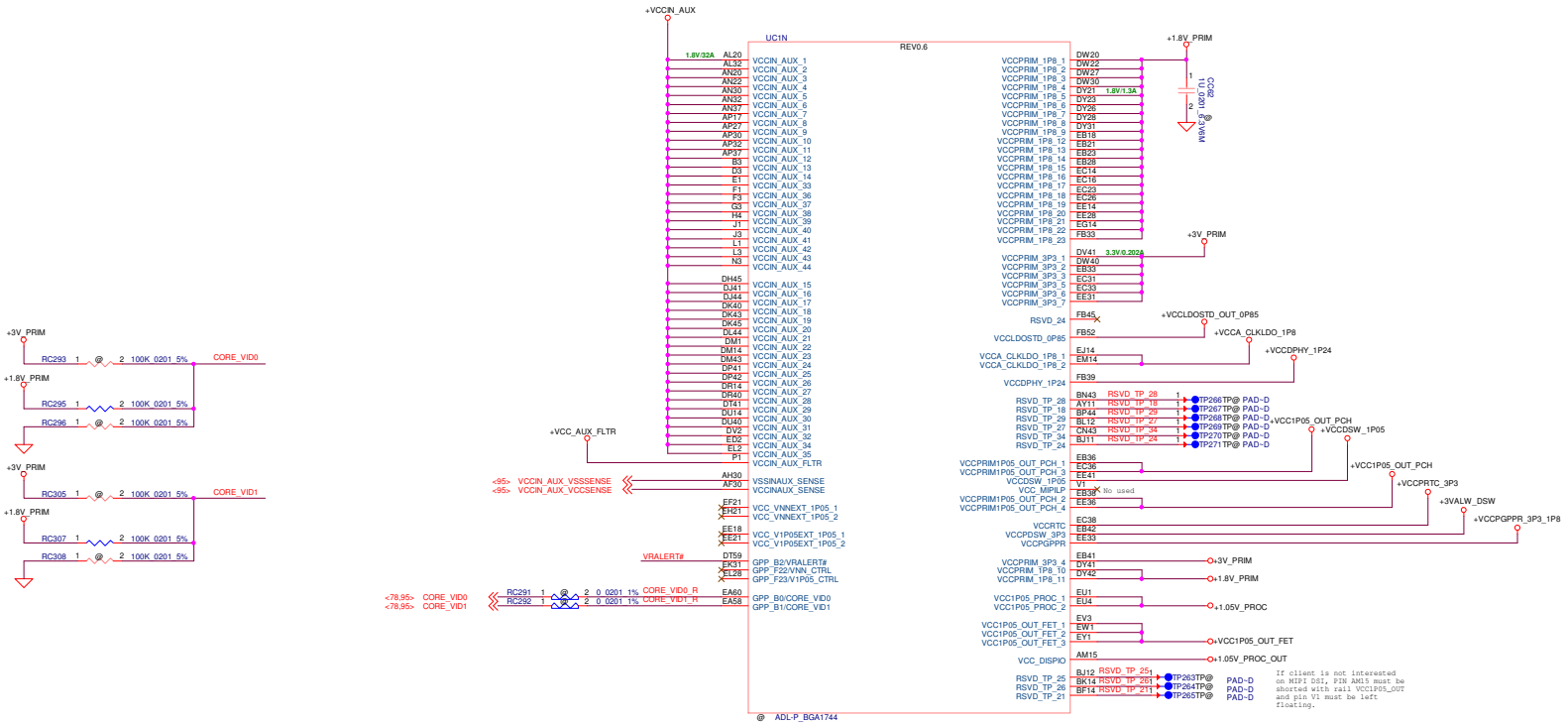
Need to check PDG Output Current

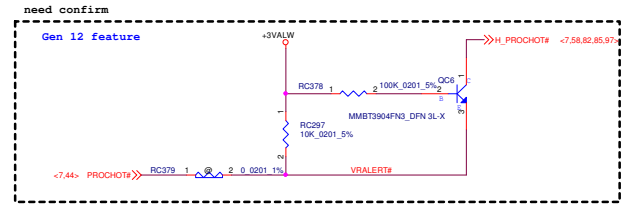


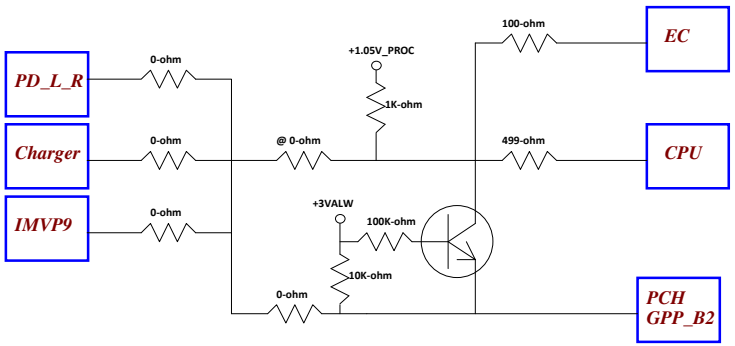


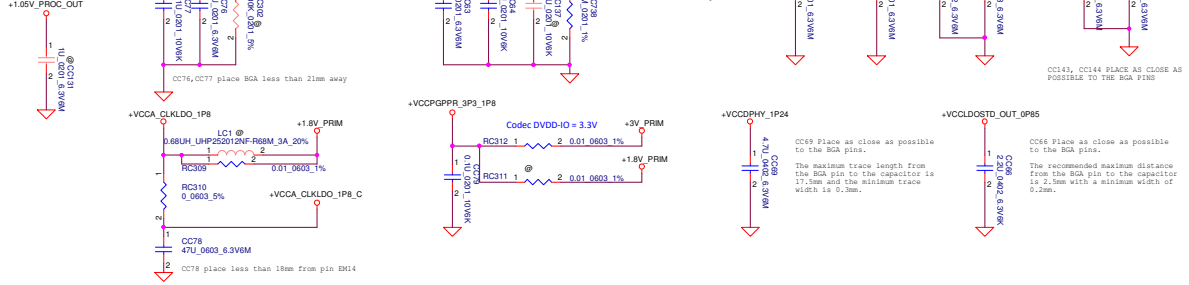
Security Classification	Compal Secret Data		
Issued Date	2020/10/15	Deciphered Date	2020/10/15

Compal Electronics, Inc.	
Title	P015 - ADL-P(10/13)CPU PWR
Size	Document Number: LA-L651P
Rev	0.1(X00)
Date: Tuesday, November 23, 2021	Sheet 15 of 80



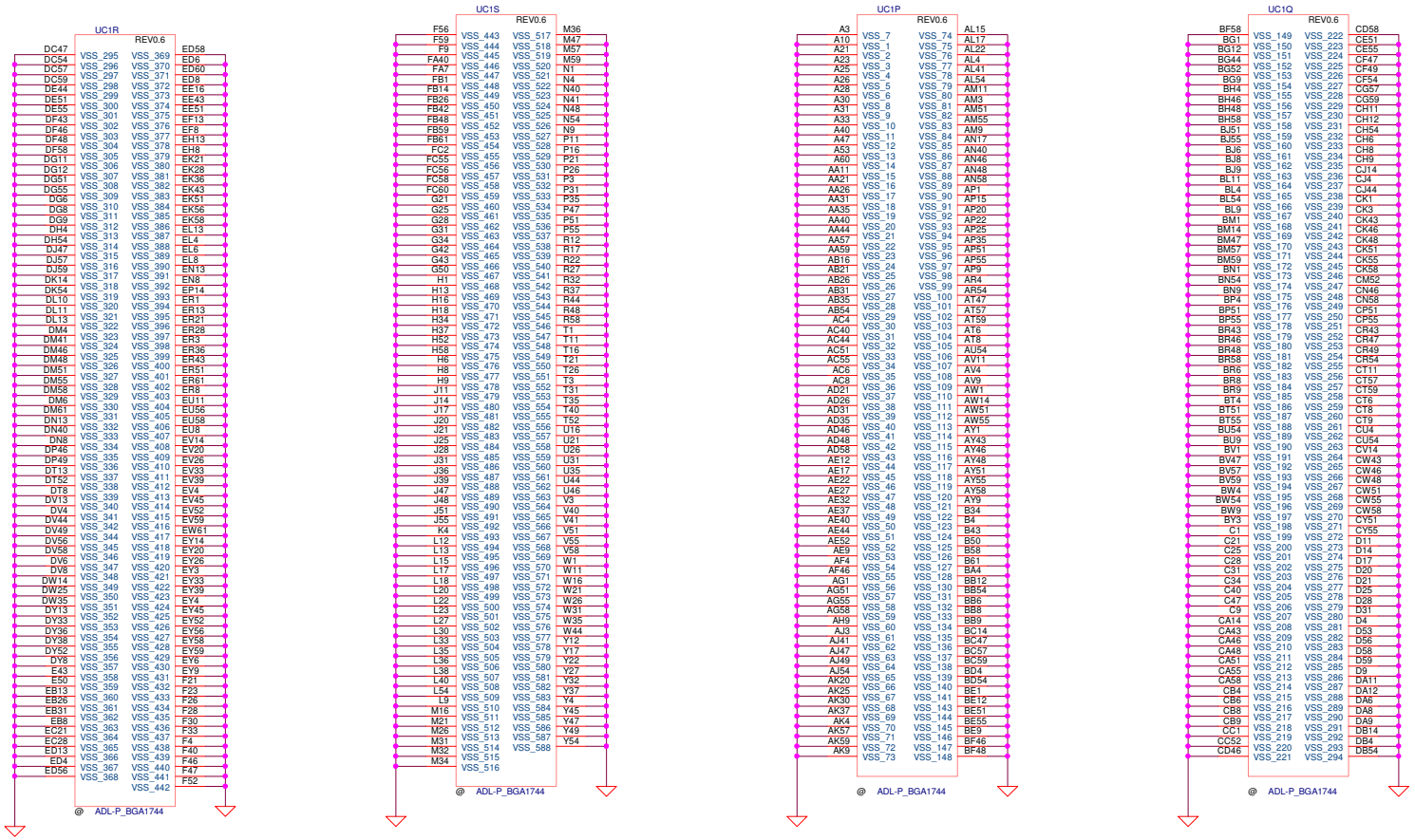




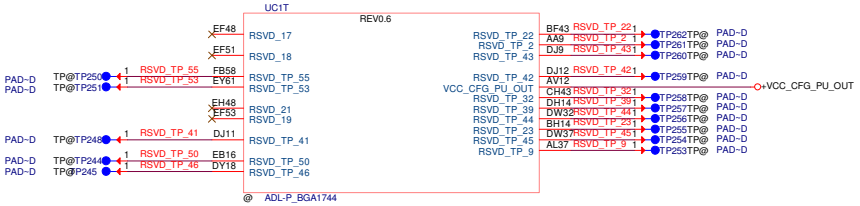


Security Classification	Compal Secret Data		
Issued Date	2020/10/15	Deciphered Date	2020/10/15

Compal Electronics, Inc.			
Title: P016 - ADL-P(11/13)PCH Power			
Size	Document Number: LA-L651P		Rev: 0.1(X00)
Date: Wednesday, November 24, 2021	Sheet 16 of 80		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/10/15	Deciphered Date 2020/10/15	Title: P017 - ADL-P(12/13)GND
			Size: Document Number: LA-L651P Rev: 0.1(X00)
			Date: Monday, November 22, 2021 Sheet 17 of 80



Security Classification	Compal Secret Data		
Issued Date	2020/10/15	Deciphered Date	2020/10/15

Compal Electronics, Inc.

Title: **P018 - ADL-P(13/13)RSVD**

Size: Document Number: **LA-L651P** Rev: 0.1(X00)

Date: Monday, November 22, 2021 Sheet 18 of 80

Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.

Title: ***P019 - Reserve***

Size | Document Number: ***LA-L651P*** | Rev: 0.1 (X00)

Date: Monday, November 22, 2021 | Sheet 19 of 80

Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.

Title: **P020 - Reserve**

Size | Document Number: **LA-L651P** | Rev: 0.1 (X00)

Date: Monday, November 22, 2021 | Sheet 20 of 80

Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.

Title: **P021 - Reserve**

Size | Document Number: **LA-L651P** | Rev: 0.1 (X00)

Date: Monday, November 22, 2021 | Sheet 21 of 80

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2019/04/01

Compal Electronics, Inc.		
Title: RSV		
Size: B	Document Number: LA-L651P	Rev: 0.2
Date: Monday, November 22, 2021	Sheet 22 of 80	

Main Func = DDR

RVS type connector

Layout Note:
Place near JDIMM2.257,259

+5V_BULK_DRAM

1104 DDR5 SODIMM request ,+5V_BULK_DRAM cap.

DT20
CEST523NC5VB_SOT-523-3

1026 Modify DDR foorprint and Data/CLK pin define

close to +5V_BULK_DRAM shape

5/6 add DT20 close to CD3362

9/27 3p change to 12p

5/6 add

11/02 ALD RVP document 631621
HID address for 1st DIMM is 000 and resistor value is 23.2K

7/5 DVT1 modify

Fiorano MLK use TP

JDIMM1

M1

M0

X00_01:Add TP49-TP60 follow RVP

PLACE THE CAP WITHIN 200 MILS FROM THE SOCKET

S type change to normal

LOTES_ADR50012-P003A

CONN@

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: DDR4 DIMMA_RVS

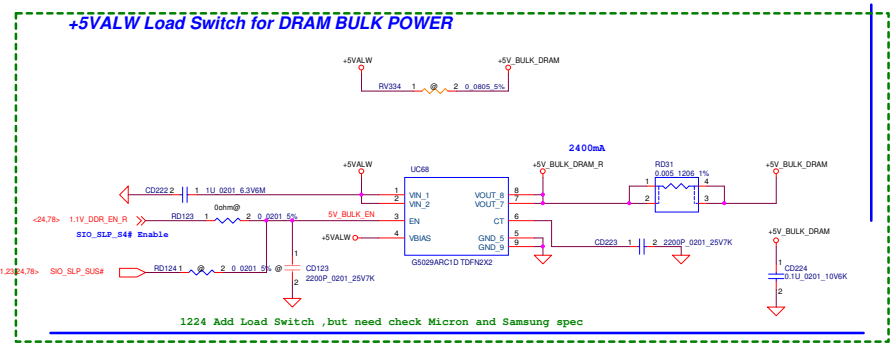
Size: | Document Number: LA-L651P | Rev: 0.1

Date: Monday, November 22, 2021 | Sheet 23 of 80

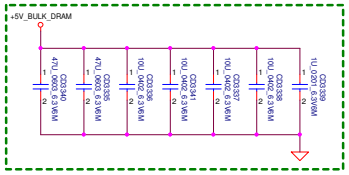
Main Func = DDR

STD type connector

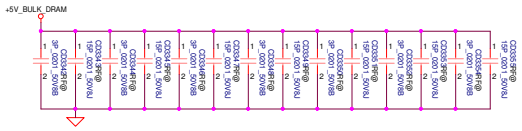
+5VALW Load Switch for DRAM BULK POWER



1224 Add Load Switch ,but need check Micron and Samsung spec

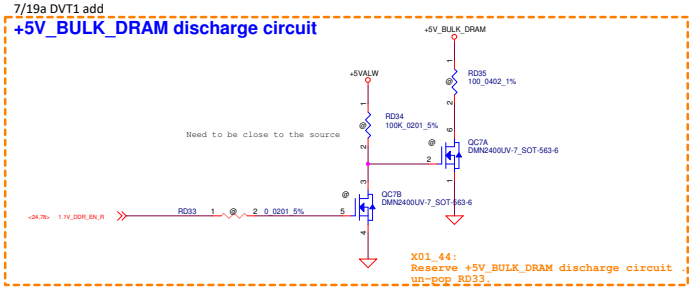


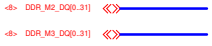
1104 DDR5 SODIMM request ,+5V_BULK_DRAM cap.



7/19a DVT1 add

+5V_BULK_DRAM discharge circuit

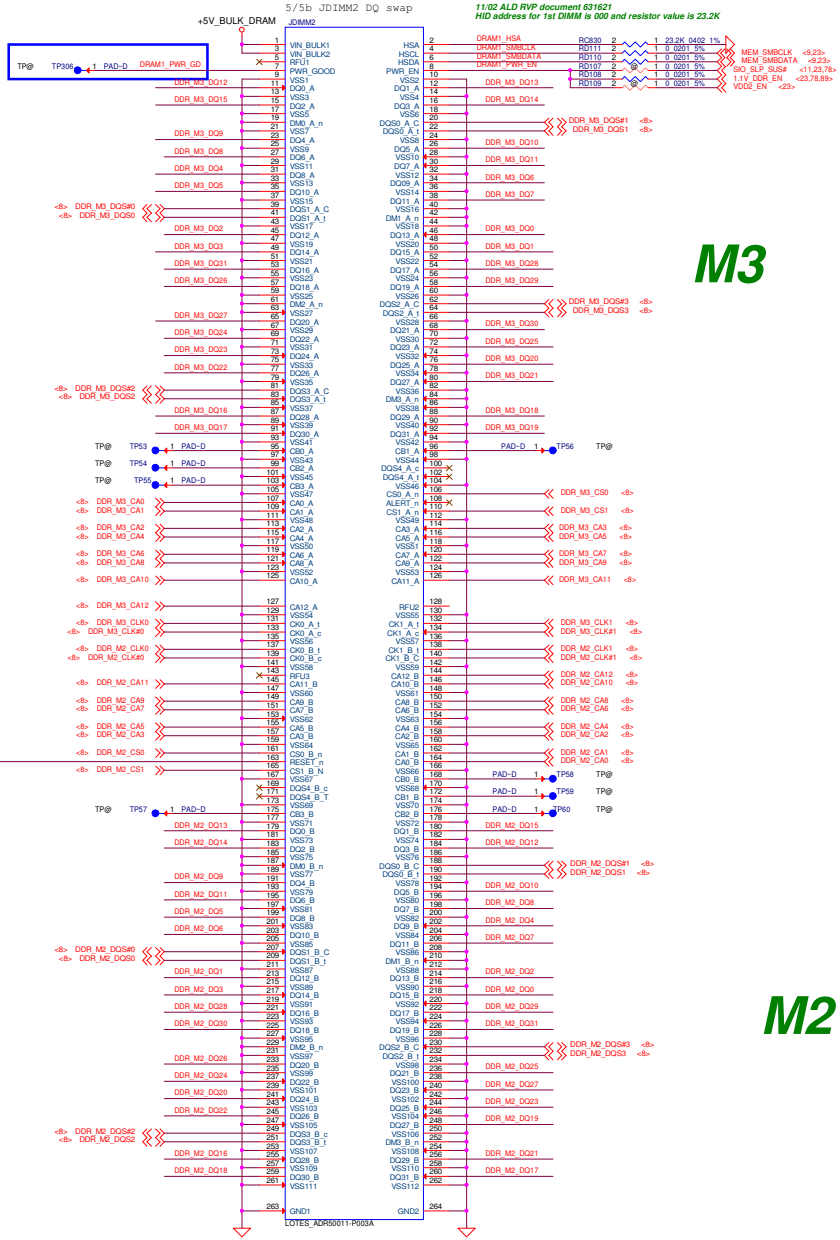




5/5b JDIMM2 DQ swap

11/02 ALD RVP document 631621
HID address for 1st DIMM is 000 and resistor value is 23.2K

Fiorano MLK rvs to EC



M3

M2

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: DDR4 DIMMB_STD

Size: Document Number: LA-L651P Rev: 0.1

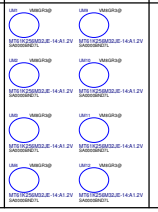
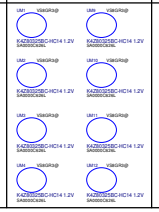
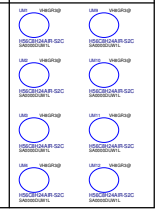
Date: Wednesday, December 01, 2021 Sheet 24 of 80

VRAM X76:

7/25 DVT1 modify
follow DVT1 proto plan

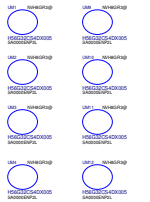
7/25 DVT1 modify
follow DVT1 proto plan

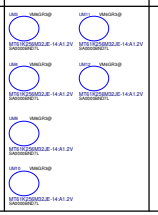
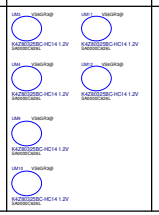
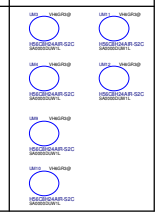
7/25 DVT1 modify
follow DVT1 proto plan

8G bit GDDR6					
Micron 8GB SKU		Samsung 8GB SKU		Hynix 8GB SKU	
R1	R3	R1	R3	R1	R3
					

R3

New Hynix (C-die)



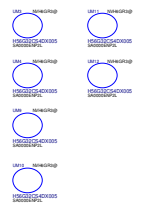
8G bit GDDR6					
Micron 6GB SKU		Samsung 6GB SKU		Hynix 6GB SKU	
R1	R3	R1	R3	R1	R3
					

R1

New Hynix (C-die)

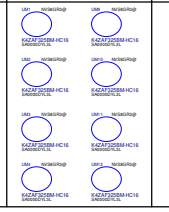
R3

New Hynix (C-die)



GN20E6/E8 DVT1.1

16G bit GDDR6					
		Samsung 6GB SKU		Hynix 6GB SKU	
R1	R3	R1	R3	R1	R3

16G bit GDDR6					
		Samsung 8GB SKU		Hynix 8GB SKU	
R1	R3	R1	R3	R1	R3
					

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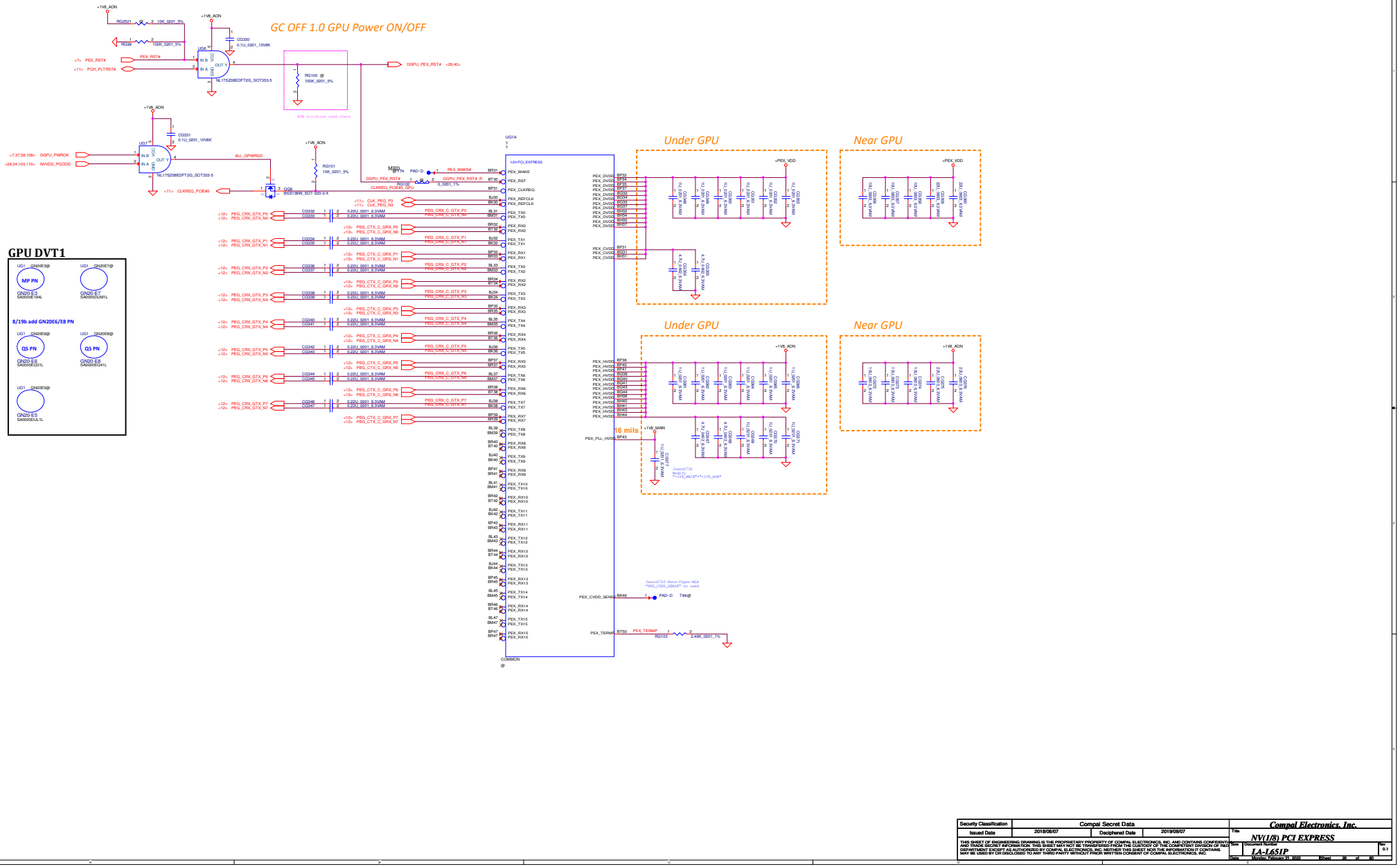
			Size: LA-L651P
			Date: Thursday, December 30, 2021
			Sheet: 36 of 69



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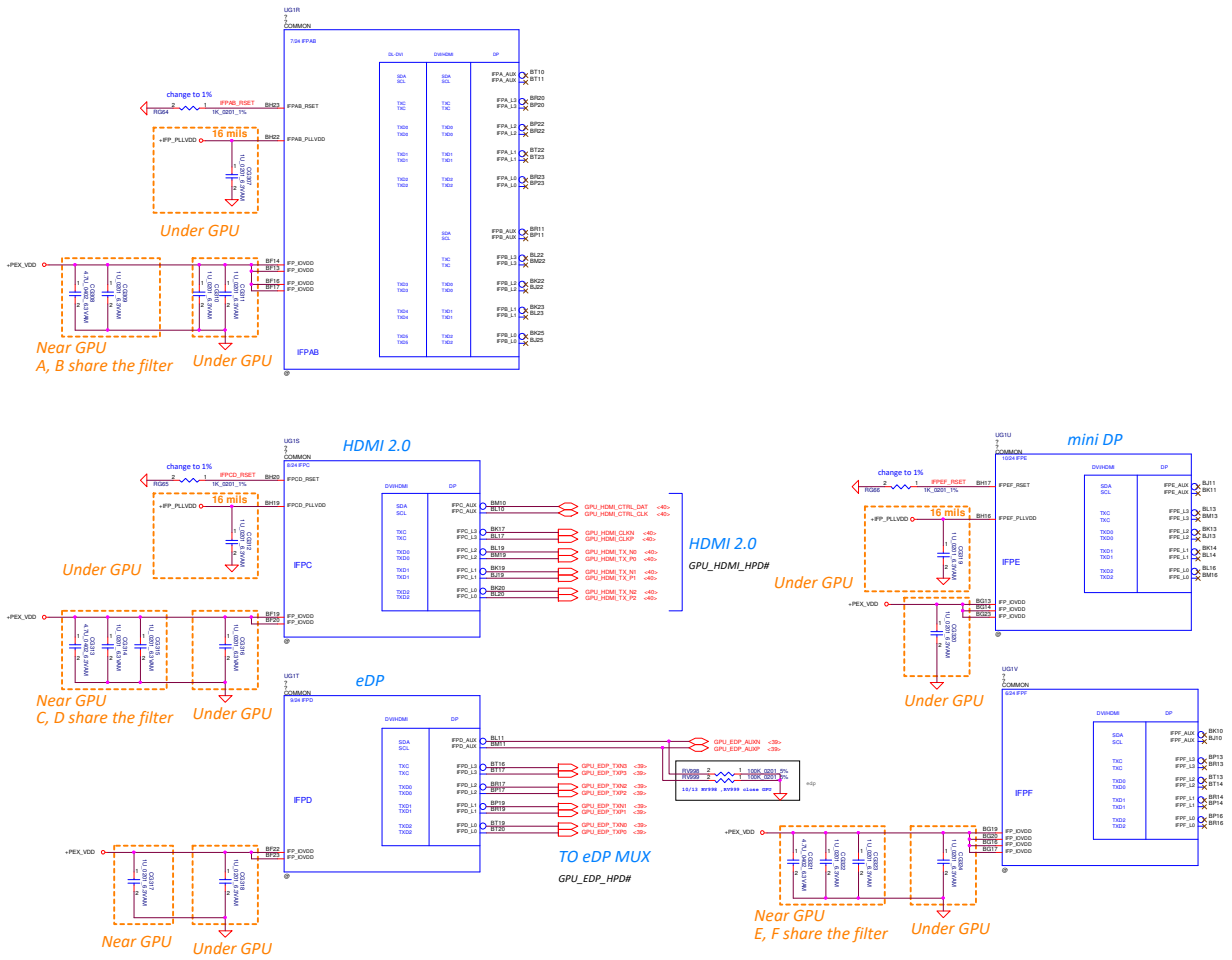
			Size: Document Number: LA-J651P Rev: 0.1
			Date: Monday, February 21, 2022 Sheet 26 of 80



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Issued Date	2018/08/07	Deciphered Date 2019/08/07	Title NV(2/8) IFP_ABCDEF
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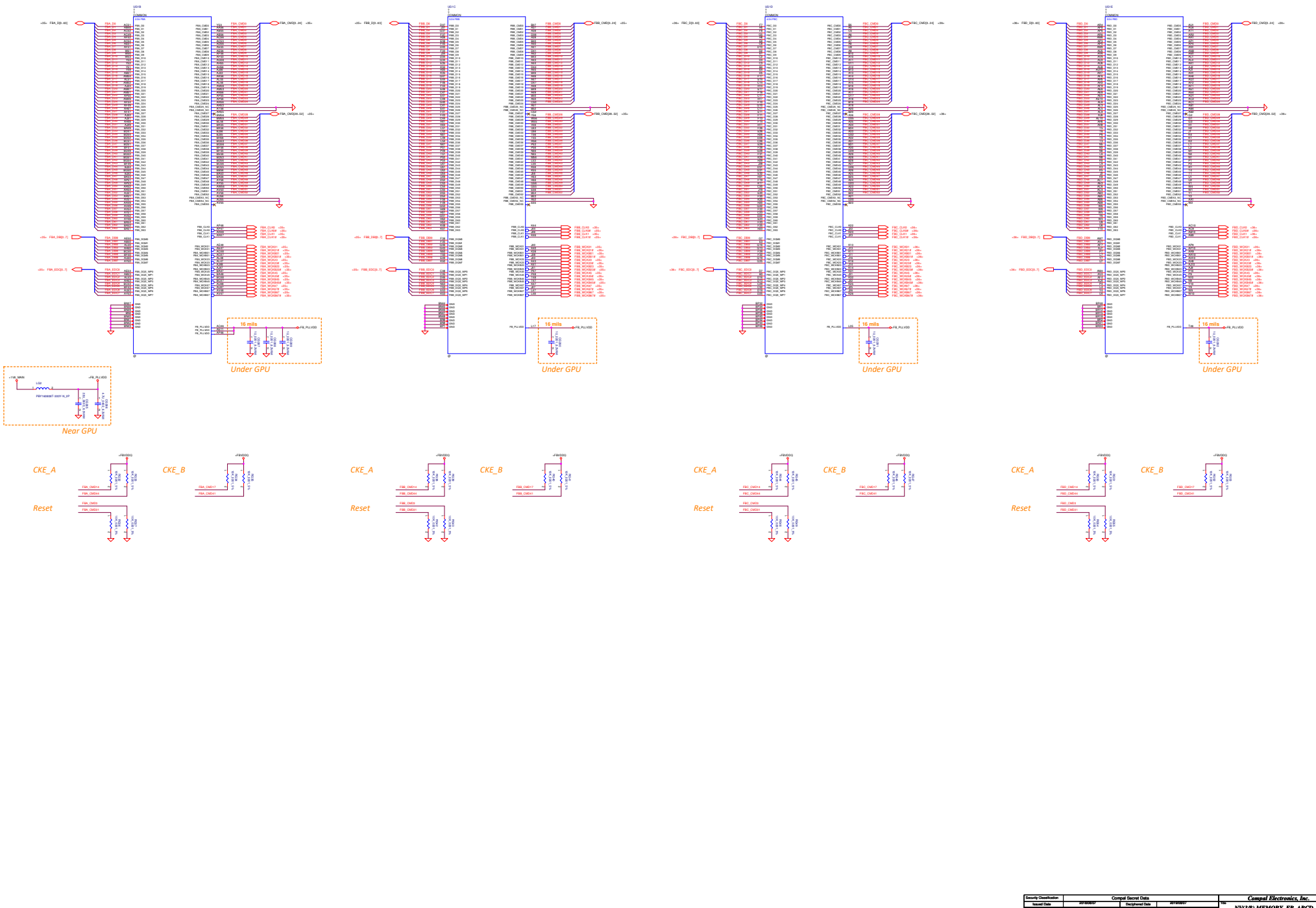
			Date Monday, November 29, 2021 Sheet 27 of 80



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/07	Deciphered Date	2016/09/07	Title: NV(3/8) MEMORY_FB_ABCD
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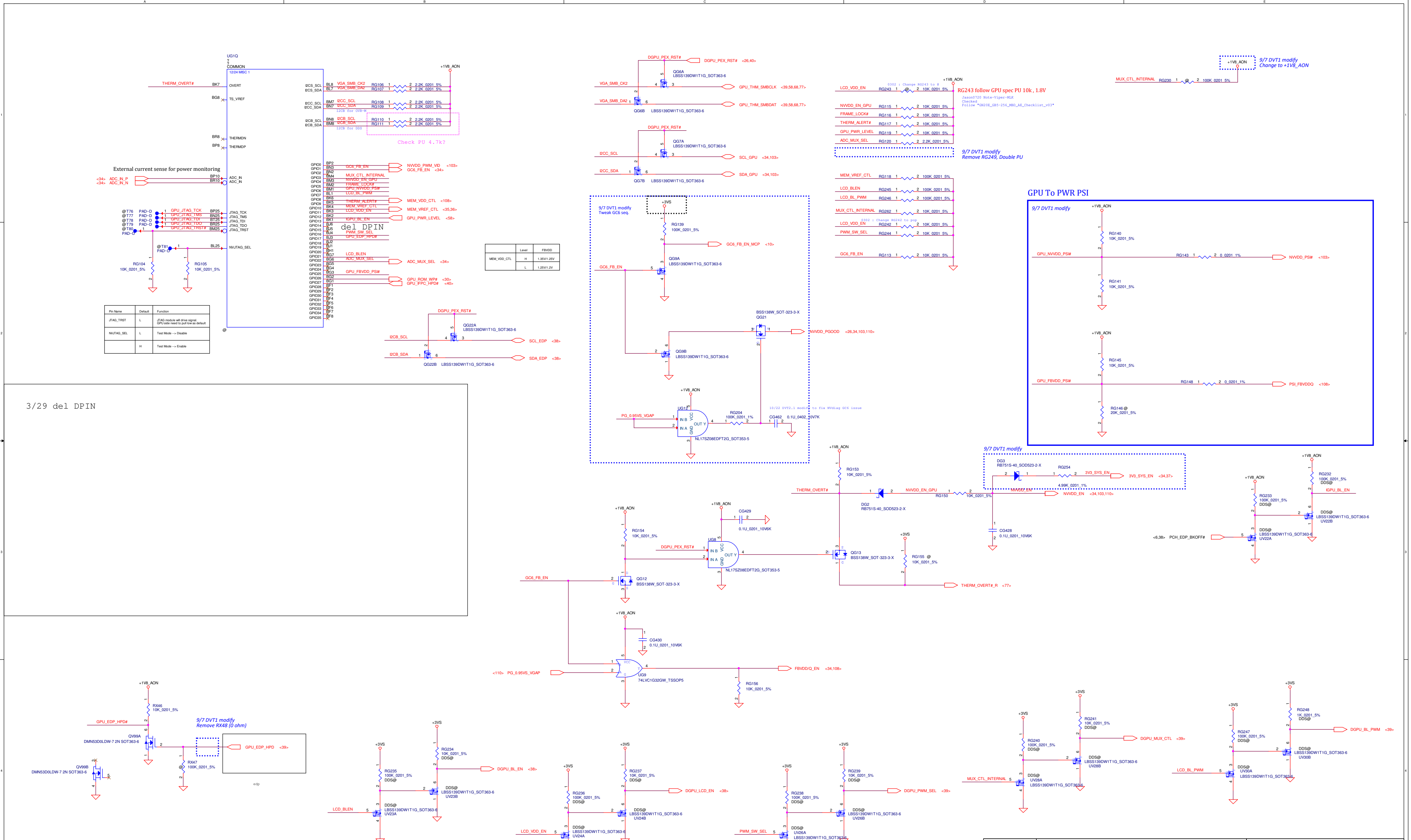
			Date: Monday, November 23, 2020	Sheet 39 of 49



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2018/08/07	Deciphered Date	2019/08/07	Title: NV(4/8) GPIO
				Size / Document Number: LA-L651P / Rev 0.1
				Date: Thursday, December 02, 2021 / Sheet 29 of 80

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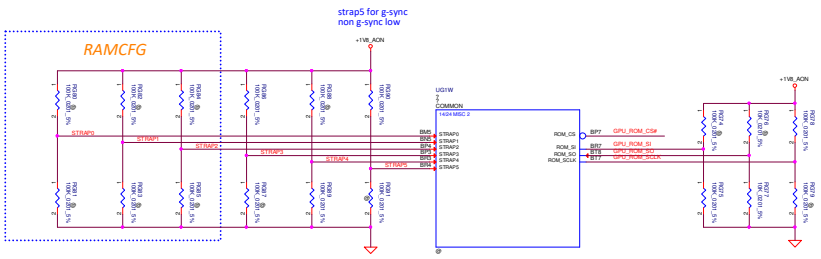

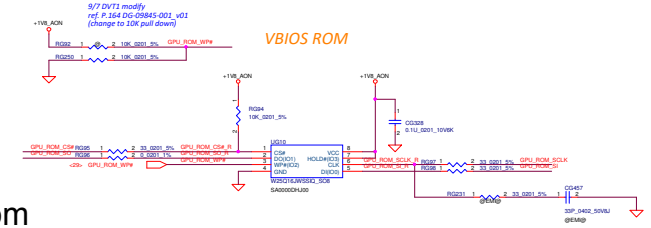

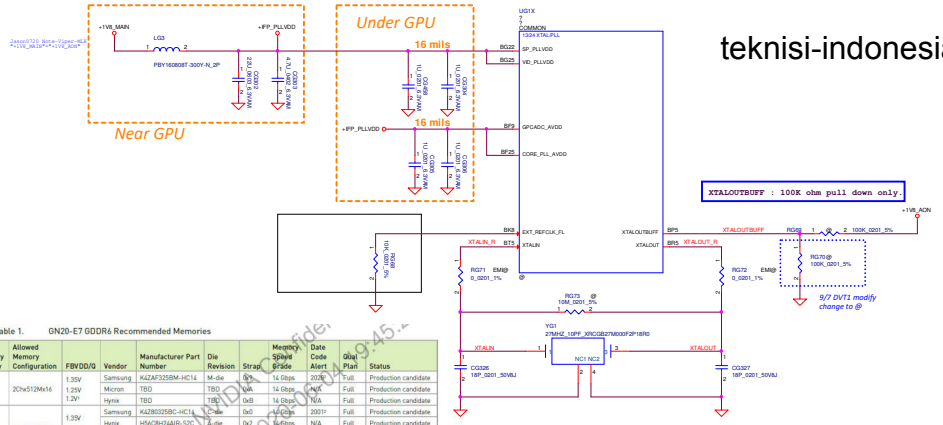

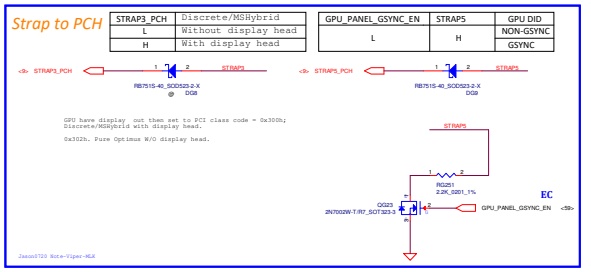

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Table 1. GN20-E7 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
16 Gb	2Chx512Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4ZAF325BM-HC14	M-die	0x6	14 Gbps	2030[2]	Full	Production candidate
			Micron	TBD	N/A		14 Gbps	N/A	Full	Production candidate
			Hynix	TBD	TBD	0x8	14 Gbps	N/A	Full	Production candidate
8 Gb	2Chx256Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001[2]	Full	Production candidate
			Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate
			Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940[2]	Full	Production candidate

Notes:
[1] Refer to GN20-E GeForce Product Spec for memory voltages and clocks.
[2] Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Samsung memory is identified by "SPL" letters inserted before the seven digits in its lot ID.
[3] Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Micron memory will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
For GN20-E7, the maximum allowable memory case temperature is 95 °C.

Table 3. GN20-E3 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001[2]	Full	Production candidate
			Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate
			Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940[2]	Full	Production candidate

Notes:
[1] Refer to GN20-E GeForce Product Spec for memory voltages and clocks.
[2] Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Samsung memory is identified by "SPL" letters inserted before the seven digits in its lot ID.
[3] Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Micron memory will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
For GN20-E3, the maximum allowable memory case temperature is 95 °C.

Table 3. GN20-E6 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status	Supported GPU Milestone
16 Gb	2Chx512Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4ZAF325BM-HC14	M-die	0x6	16 Gbps	2137[2]	Full	Production candidate	QS or later
				K4ZAF325BC-SC16	C-die	0xA	16 Gbps	N/A	Full	Post-production candidate	TBD
			Hynix	H56G42AS4DX014	A-die	0x8	16 Gbps	N/A	Full	Production candidate	QS or later
8 Gb	2Chx256Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001	Full	Production candidate	QS or later
			Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate	QS or later
				H56G32CS4DX005	C-die	0x5	16 Gbps	N/A	Full	Post-production candidate	TBD
			Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940	Full	Production candidate	QS or later

Table 9.3 RAMCFG

Strap Pins (see Note)			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)

Table 9.3 RAMCFG

Strap Pins (see Note)			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	For DDS unify VBIOS used
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	Default
L	L	H	0	0	0	1	
L	L	L	0	0	0	0	

GDDR6 Memory RVL

NVIDIA recommends the following GDDR6 memories for use in conjunction with notebook designs using GN20 GPUs.

Table 1. GN20-E8 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status	Supported GPU Milestone
16 Gb	2Chx512Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4ZAF325BM-HC14	M-die	0x6	16 Gbps	2137[2]	Full	Production candidate	QS or later
				K4ZAF325BC-SC16	C-die	0xA	16 Gbps	N/A	Full	Post-production candidate	TBD

Notes:
[1] Refer to the *GN20-E8/E4 Refresh GeForce Product Specification* for memory voltages and clocks.
[2] Before the date code is available, the Samsung memory is screened for 12 Gbps @ 1.2V support. The Samsung memory is identified by the letters "SPL", which are inserted before the seven digits in its lot ID.
- GN20-E8 will be single sourced for the foreseeable future until further notice from NVIDIA.
- For GN20-E8, the maximum allowable memory case temperature is 95 °C.

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2021/12/31

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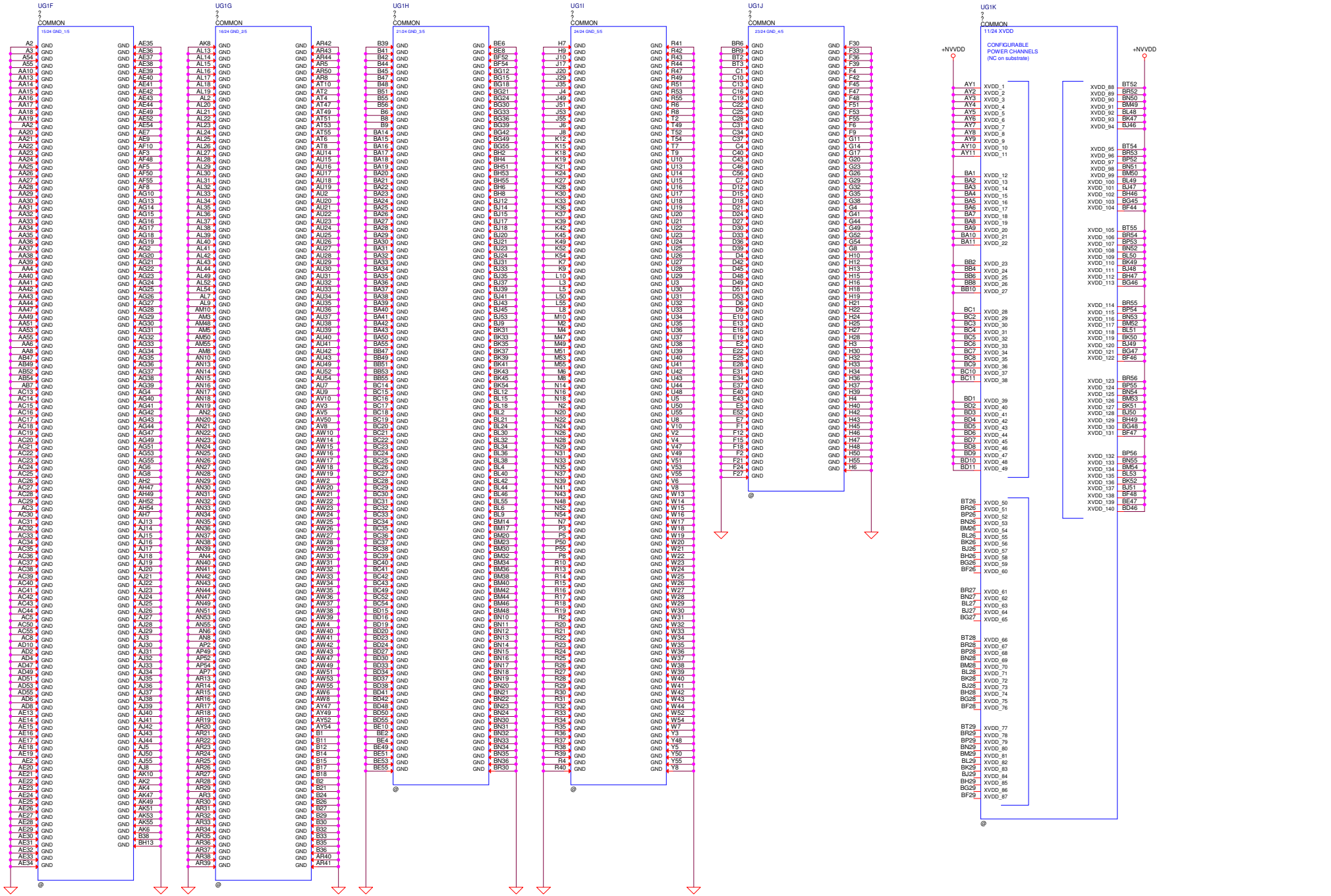
Title: NV(4/8) STRAP, ROM, XTAL

Size: D | Document Number: LA-L651P | Rev: 0.1

Date: Monday, November 29, 2021 | Sheet 30 of 80



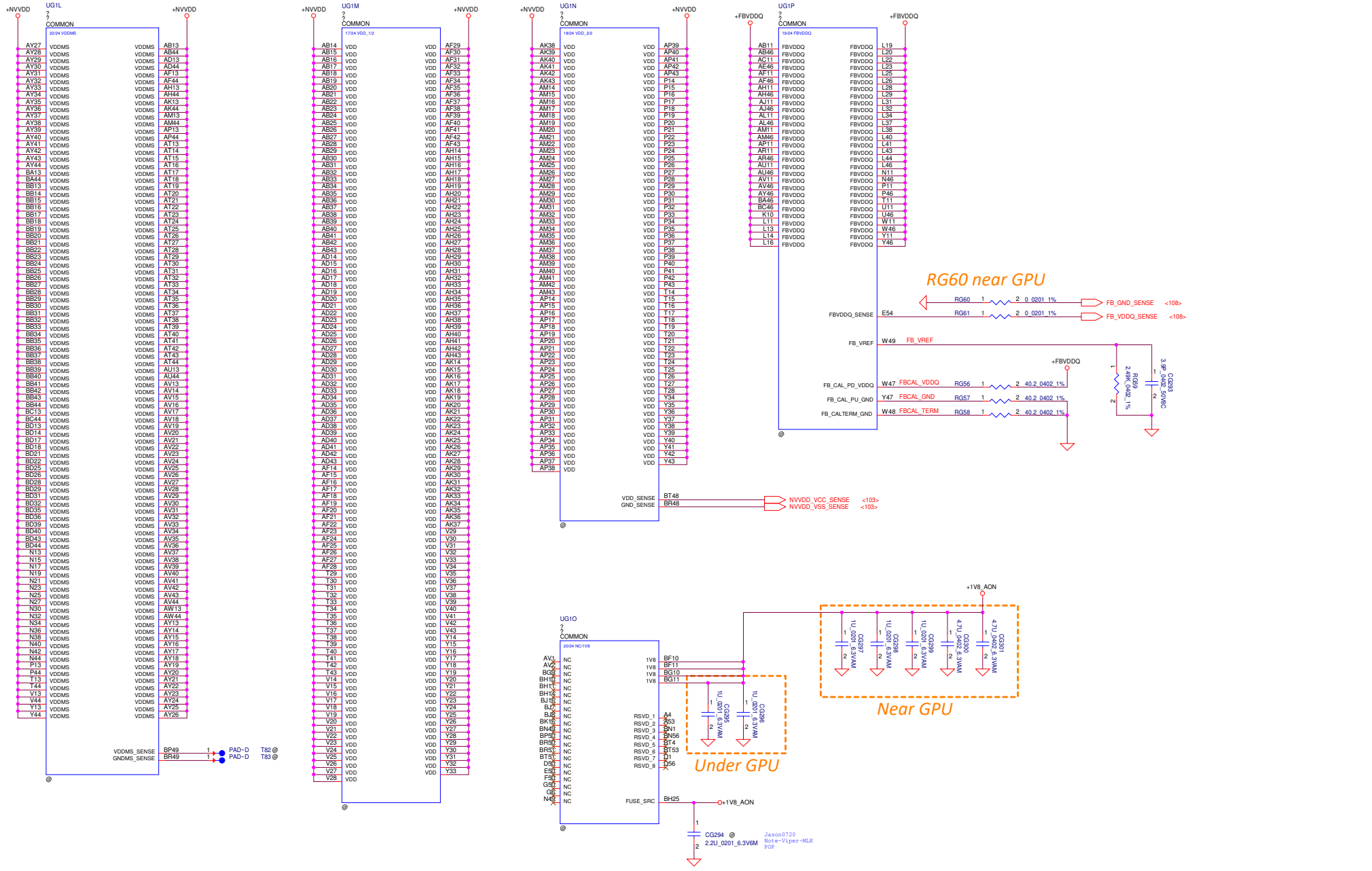
Security Classification	Compal Secret Data		
Issued Date	2018/08/07	Deciphered Date	2019/08/07

Compal Electronics, Inc.

Title: **NV(6/8) GND, RFUs**

Size	Document Number	Rev
	LA-L651P	0.1

Date: Monday, November 22, 2021 | Sheet 31 of 80



Security Classification	Compal Secret Data		
Issued Date	2018/08/07	Deciphered Date	2019/08/07

Compal Electronics, Inc.

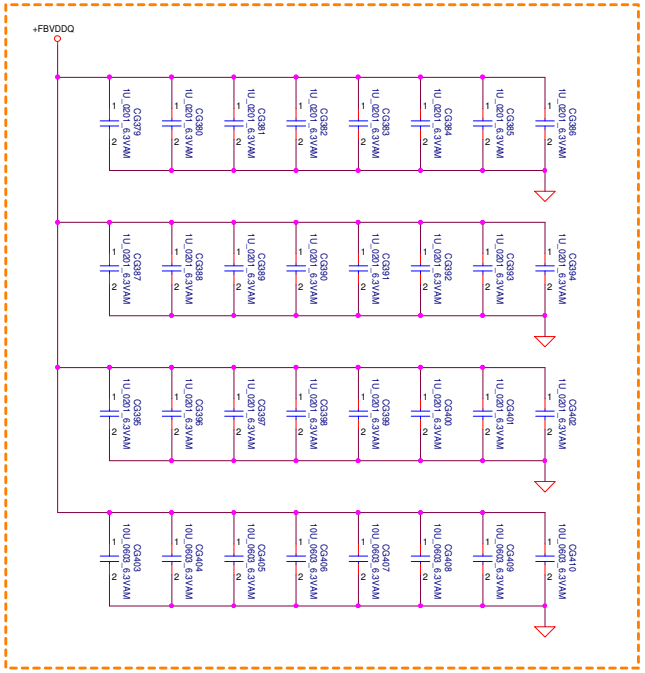
Title: **NV(7/8) POWERS**

Size	Document Number	Rev
	LA-L651P	0.1

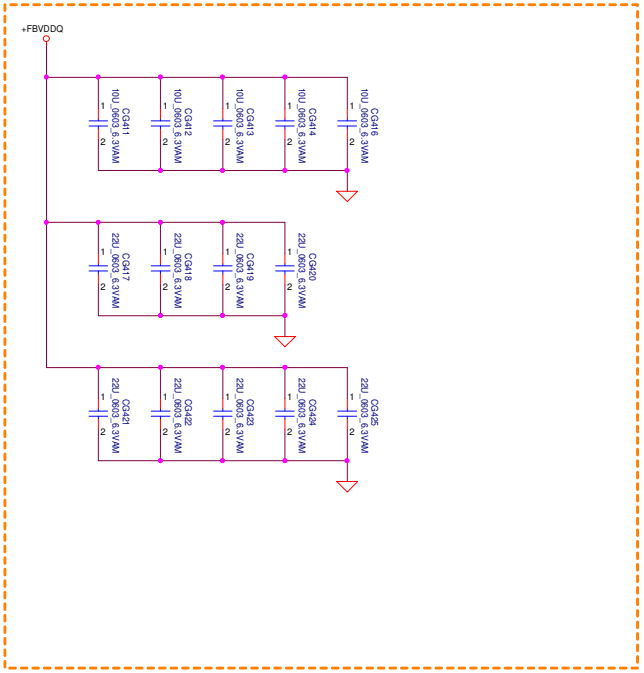
Date: Monday, November 22, 2021 Sheet 32 of 80

FBVDDQ_GPU

Under GPU



Near GPU

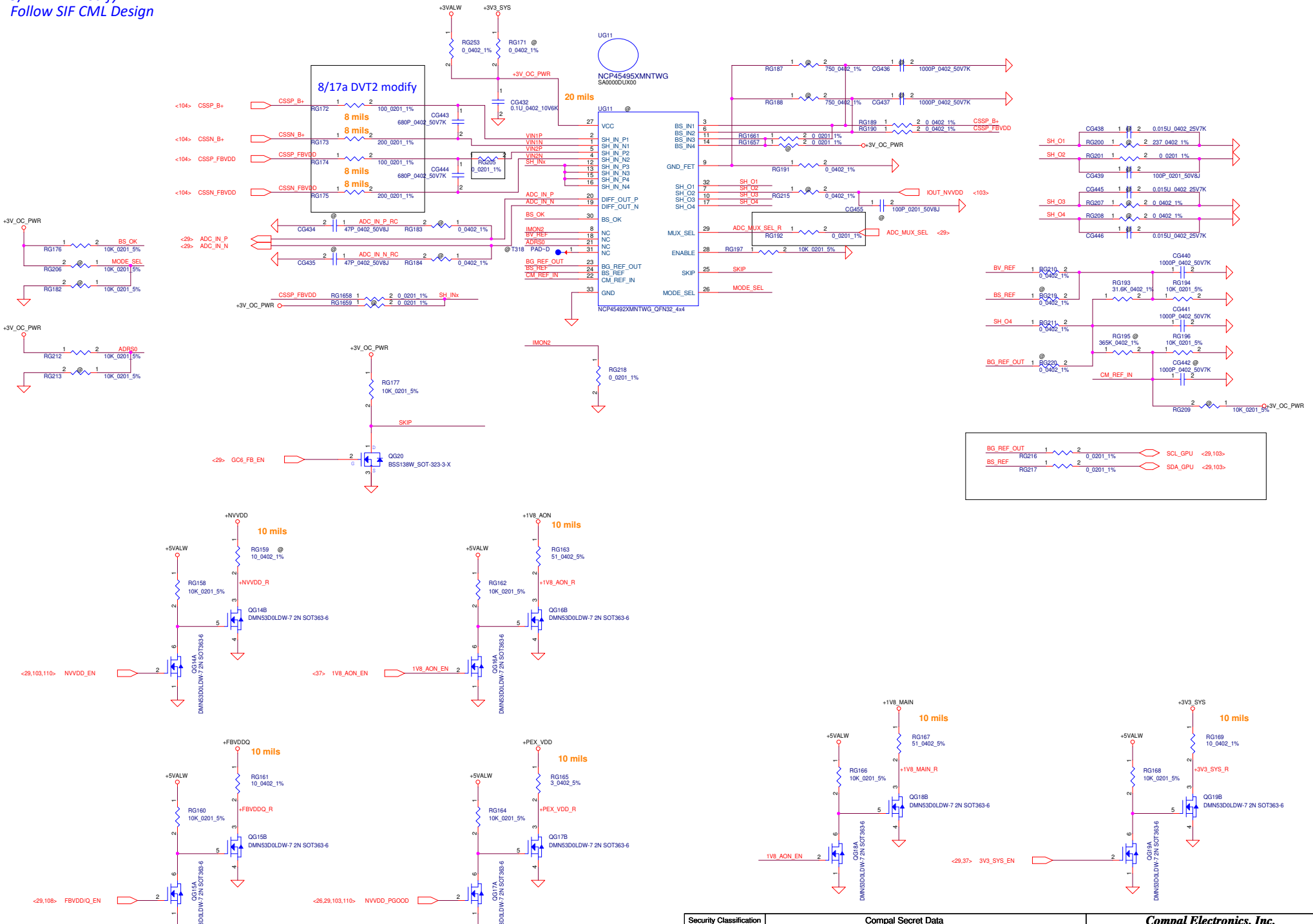


Security Classification	Compal Secret Data		
Issued Date	2018/08/07	Deciphered Date	2019/08/07

Compal Electronics, Inc.		
Title: NV(8/8) GPU DECOUPLING		
Size	Document Number: LA-L651P	Rev: 0.1
Date: Monday, November 22, 2021	Sheet 33 of 80	

9/7 DVT1 modify
Follow SIF CML Design

8/17a DVT2 modify



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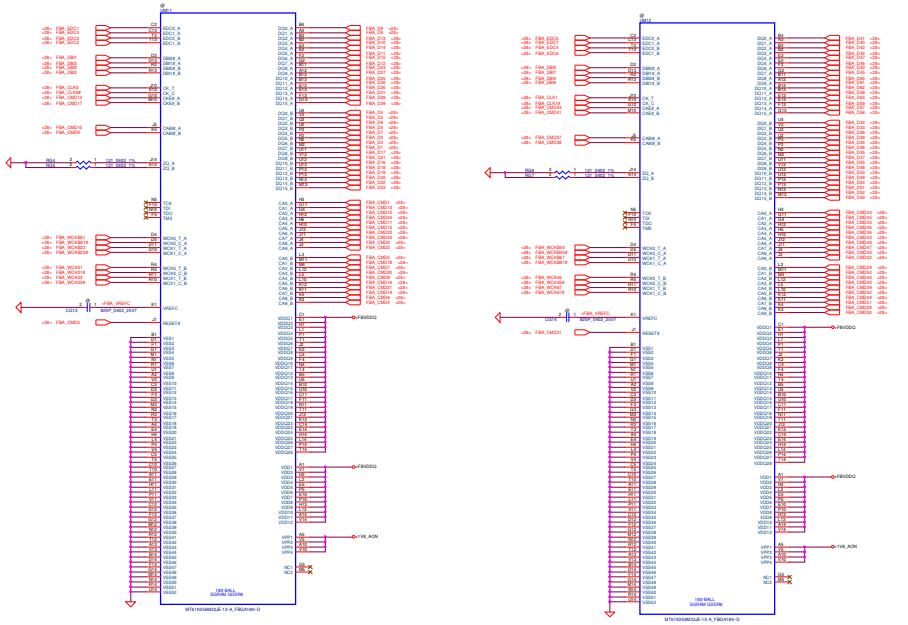
Issued Date	2018/08/07	Deciphered Date	2019/08/07

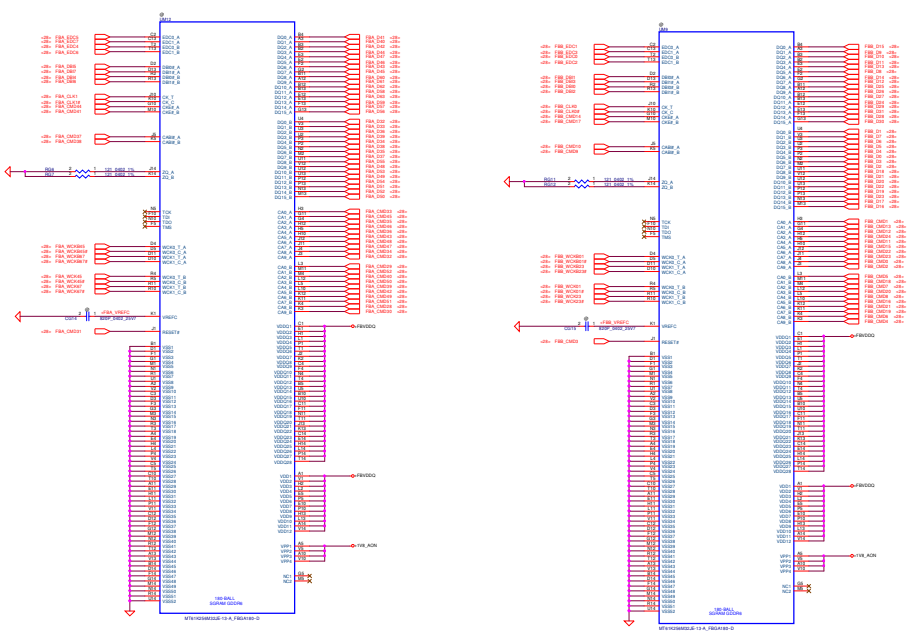
Compal Electronics, Inc.

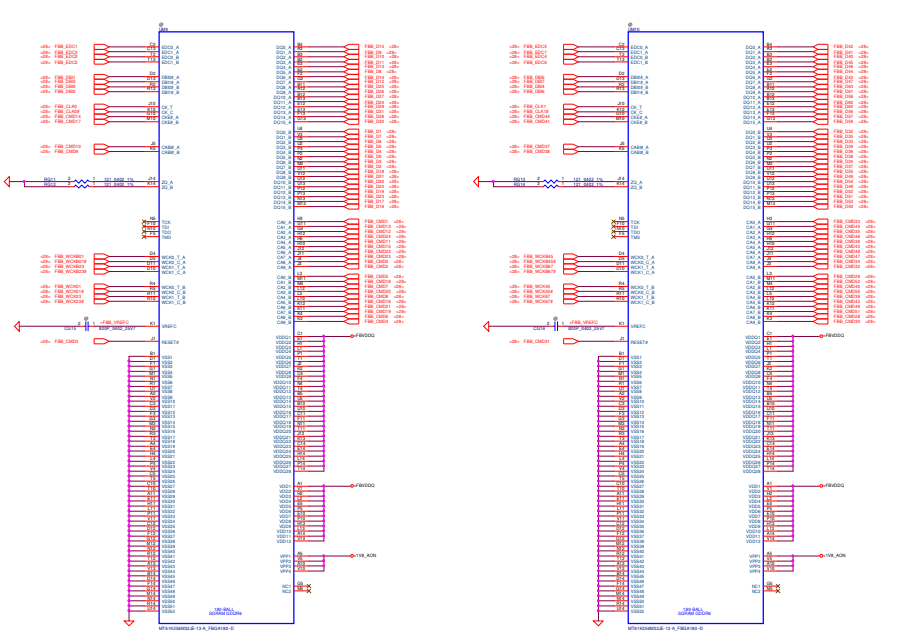
Title: **OC, Discharging**

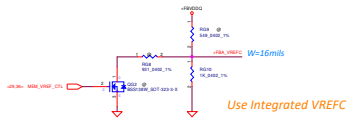
Size	Document Number	Rev
	LA-L651P	0.1

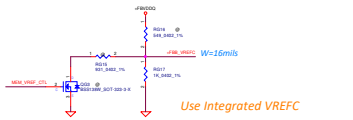
Date: Thursday, December 02, 2021 Sheet 34 of 80



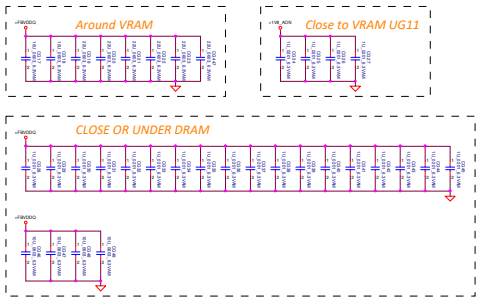




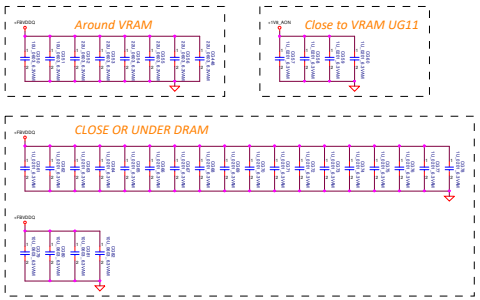




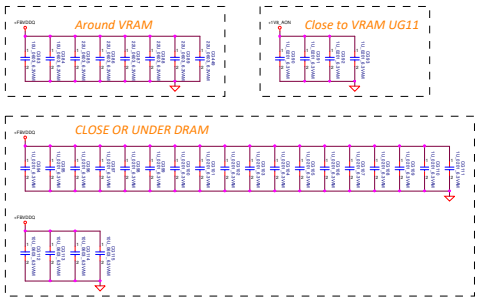
UM11



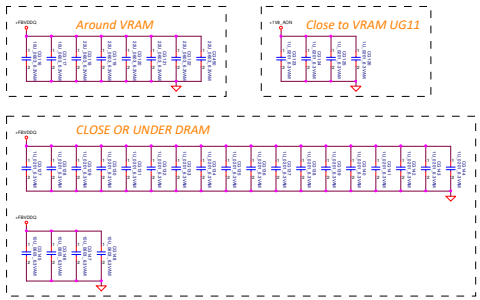
UM12



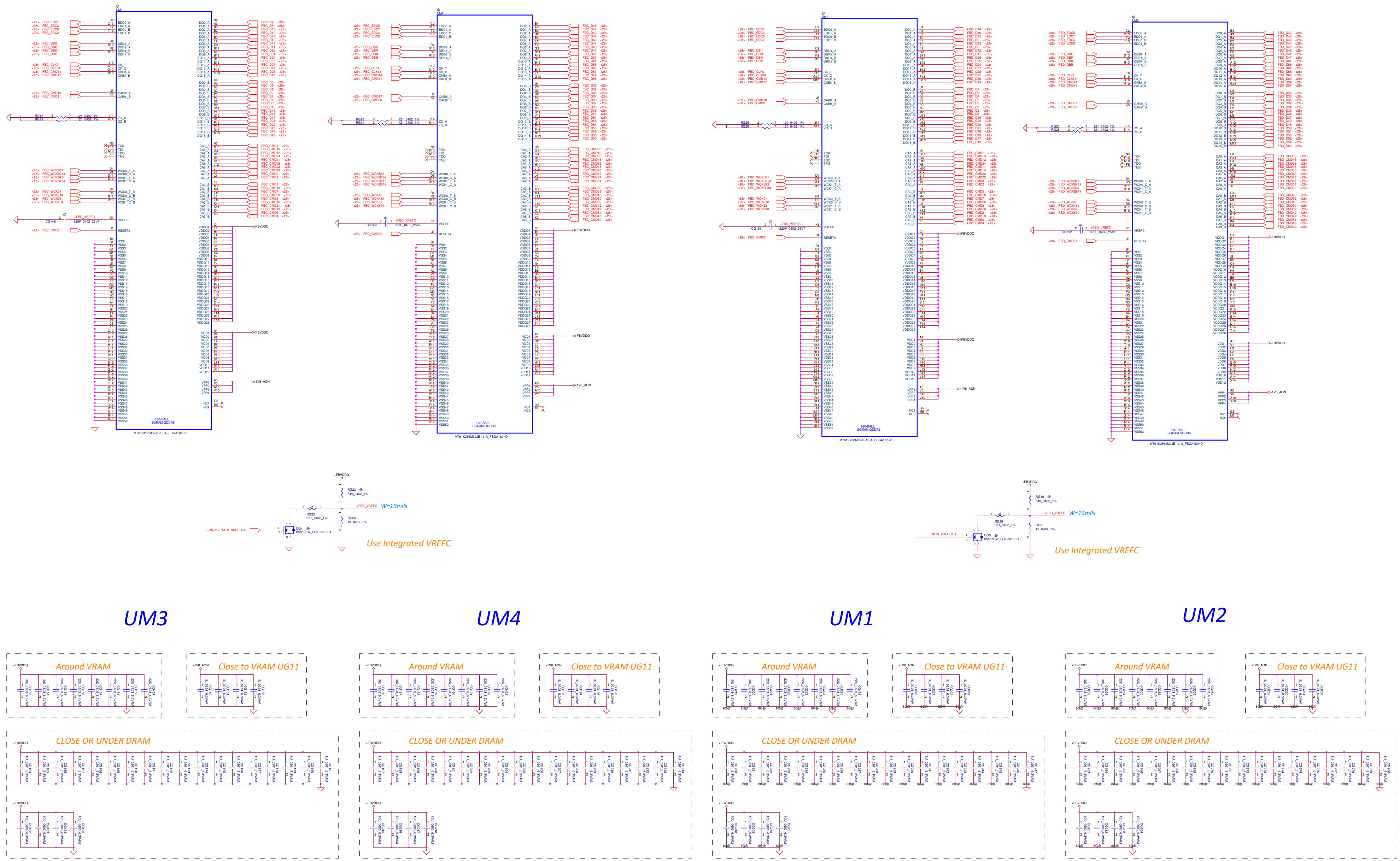
UM9



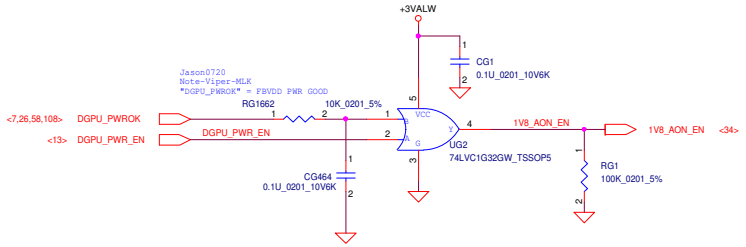
UM10



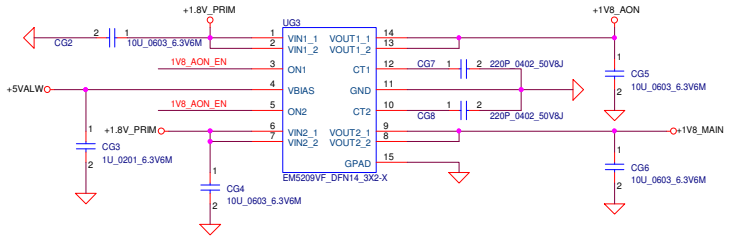
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/07	Deciphered Date	2016/09/07
			Title: VRAM_GDDR6_AB
			Size: LA-L451P
			Rev: 0.4
			Date: Monday, November 23, 2020
			Sheet: 36 of 49

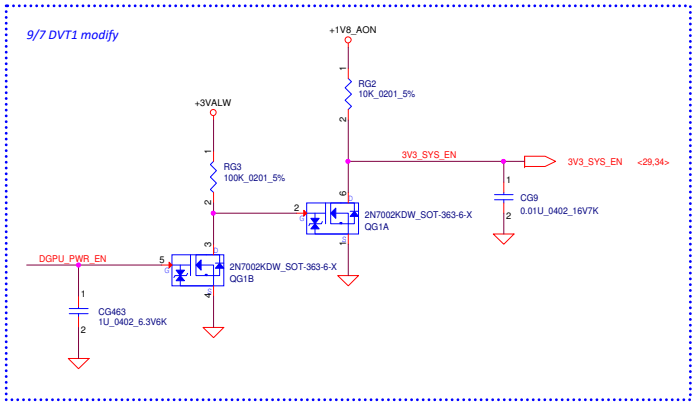


Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2018/08/07	Deciphered Date	2019/08/07	Title: VRAM_GDDR6_CD
				Size / Document Number: LA-L651P / Rev 0.1
				Date: Monday, November 22, 2021 / Sheet 36 of 80

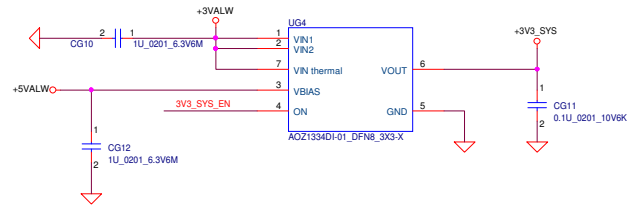


+1V8_AON / +1V8_MAIN(PLL)

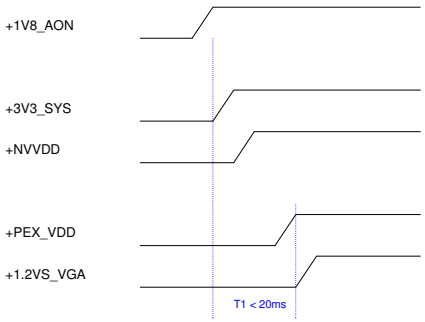




NV_3V3(For Sequence)

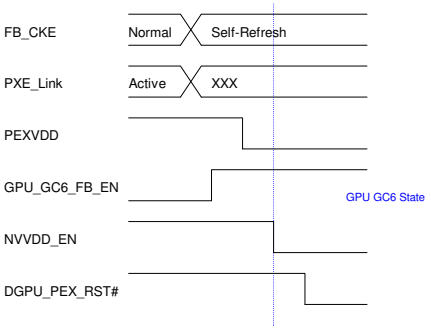


GPU Power Up Sequence



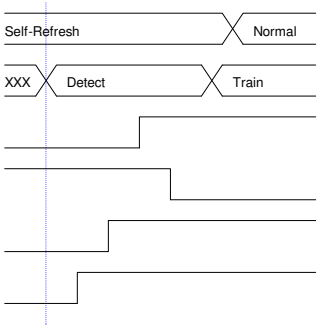
The ramp time for any rail must be more than 40us and less than 2ms.

GPU GC6 Entry Sequence

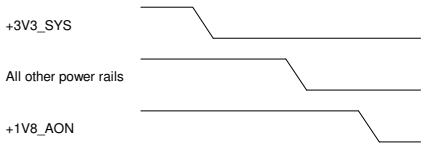


The entire entry/exit sequence must complete within 200 ms.

GPU GC6 Exit Sequence



GPU Power Down Sequence



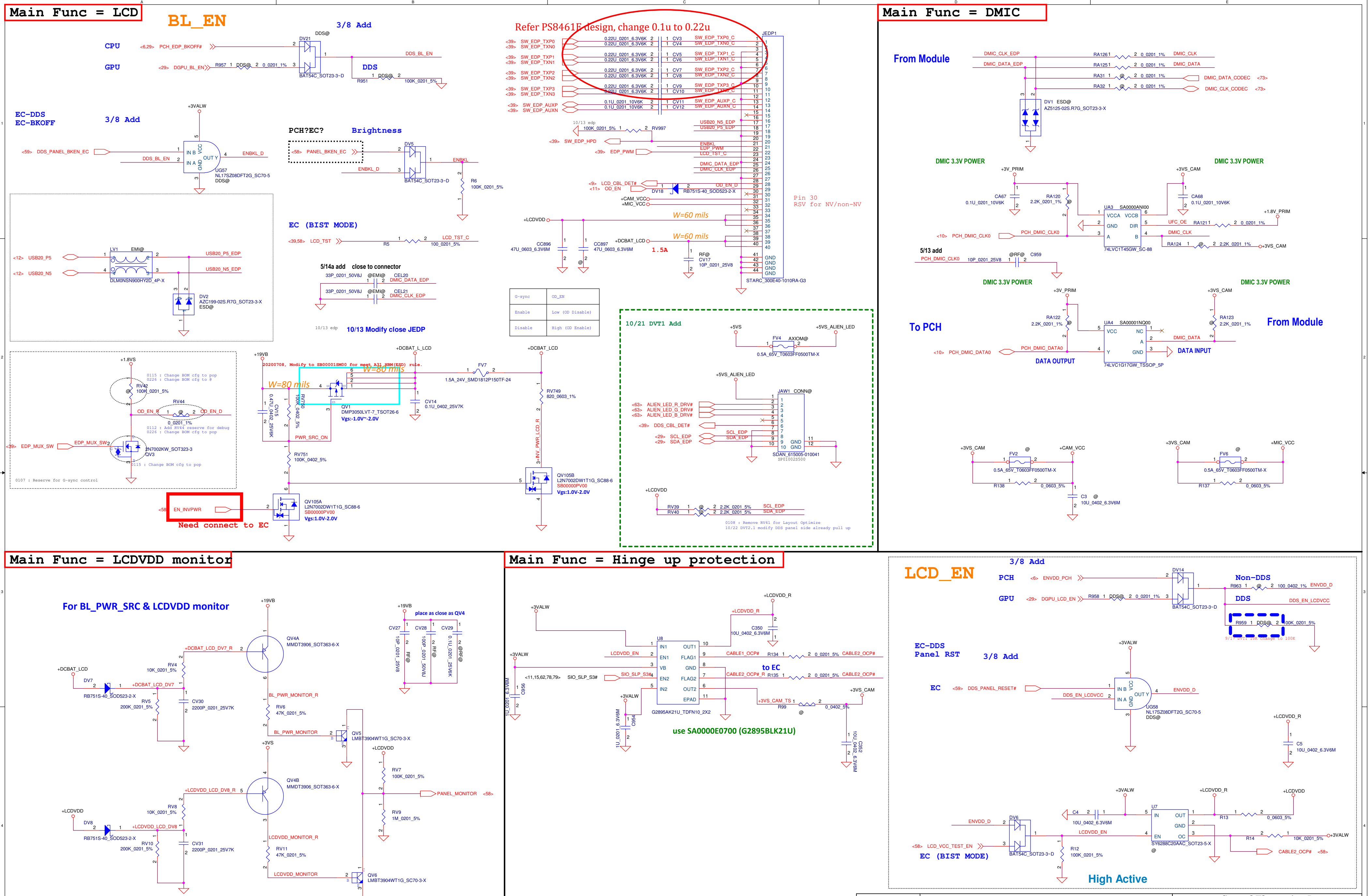
Security Classification	Compal Secret Data		
Issued Date	2018/08/07	Deciphered Date	2019/08/07

Compal Electronics, Inc.

Title: DGPU_DC/DC Interface

Size	Document Number	Rev
	LA-L651P	0.1

Date: Monday, November 22, 2021 Sheet 37 of 80



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/02/05

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Compal Electronics, Inc.

Title: eDP/Camera

Document Number: LA-L651P — Rev 0.2

Date: Wednesday, November 24, 2021 — Sheet 38 of 80

Main Func = eDP DDS PWM

9/12 DVT1 modify
Change DDS detect logic to "Low" (EC)

PU on EC side

To PWM Switch

To MUX Switch

BL_PWM

9/12 DVT1 modify

PU on EC side

EN#	IN	NC to COM COM to NC	NO to COM COM to NO	Function
L	L	ON	OFF	IGPU
L	H	OFF	ON	DGPU
H	X	OFF	OFF	X

9/16 DVT1 modify
For 360Hz Panel support (Min PWM level 3.0)

Main Func = eDP DDS MUX

PS8461=3.3V , 210 mA

9/12 DVT2 modify

FROM CPU

FROM GPU

Refer PS8461E design

UV66 need modify symbol

Refer PS8461E reference design 9/2

pull down at GPU side

need pull down at GPU side???

TO JEDP1

9/3b A3 rev ,RV1000 & RV1001 un pop

9/3a vendor request

9/3b A3 rev ,R7000 pop

MUX Switch	EDP_SW
0 (Default)	IGPU
1	DGPU

EQ Value

need the bom suggestions from vendor

Refer PS8461E design

+1.2V_RUN power ripple need <30mV

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2019/04/01

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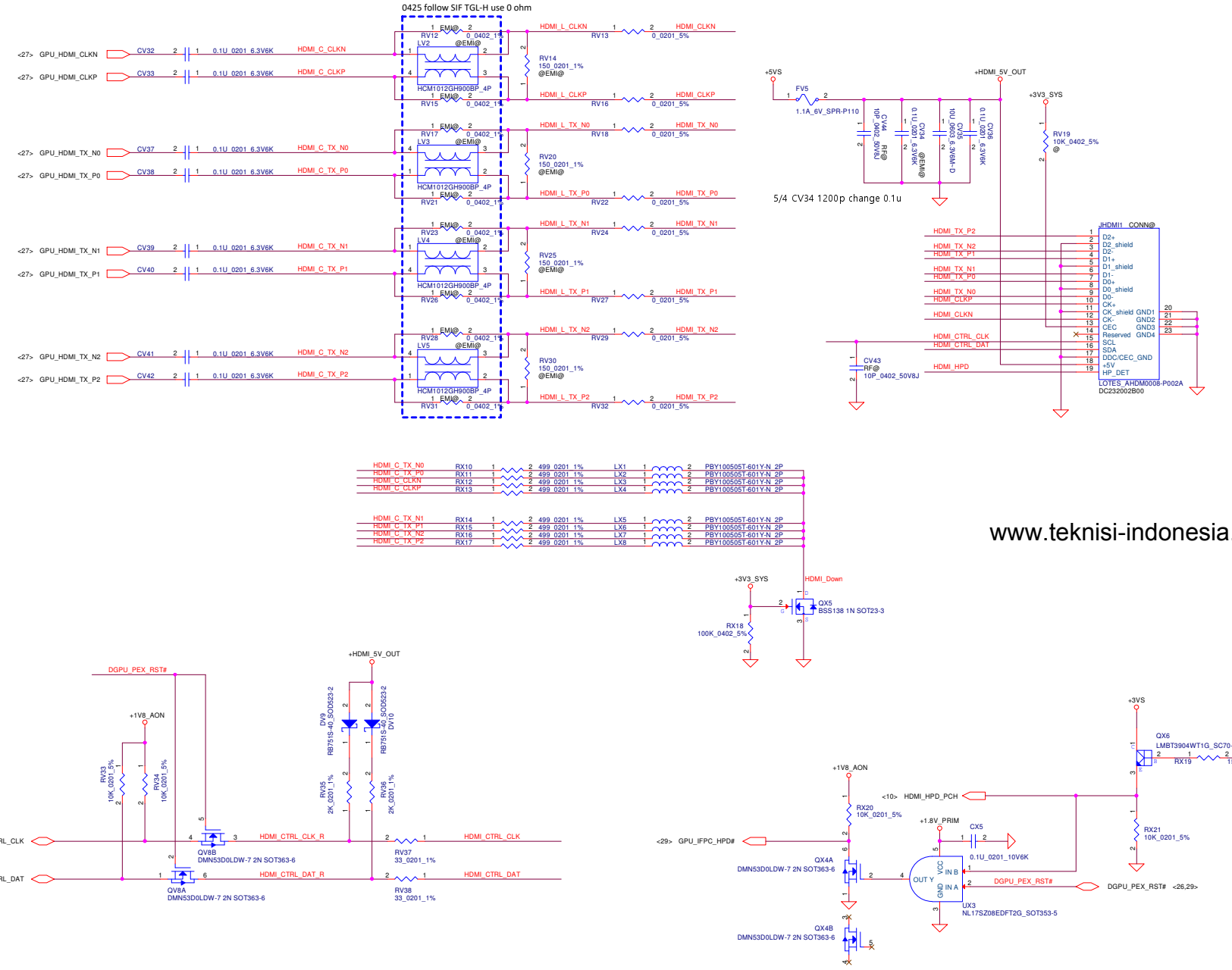
Compal Electronics, Inc.

Title: eDP MUX/DDS

Size: Document Number: LA-L651P Rev: 0.1

Date: Wednesday, November 24, 2021 Sheet 39 of 80



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **HDMI**

Size | Document Number: **LA-L651P** | Rev: 0.2

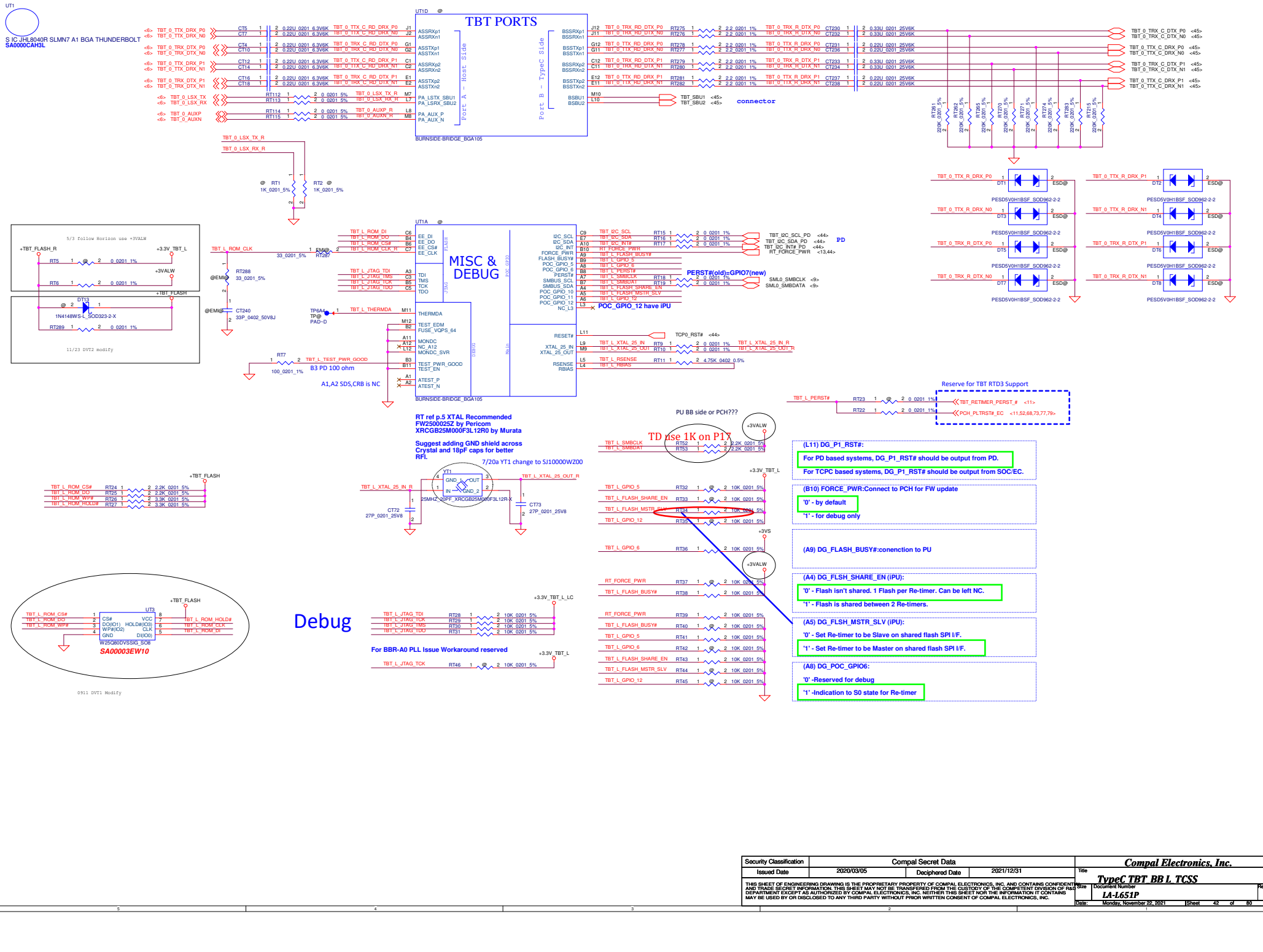
Date: Tuesday, November 23, 2021 | Sheet 40 of 80

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2019/04/01

Compal Electronics, Inc.		
Title: RSV		
Size: B	Document Number: LA-L651P	Rev: 0.2
Date: Monday, November 22, 2021	Sheet 41 of 80	



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2021/12/31	Title: TypeC TBT BB L TCSS
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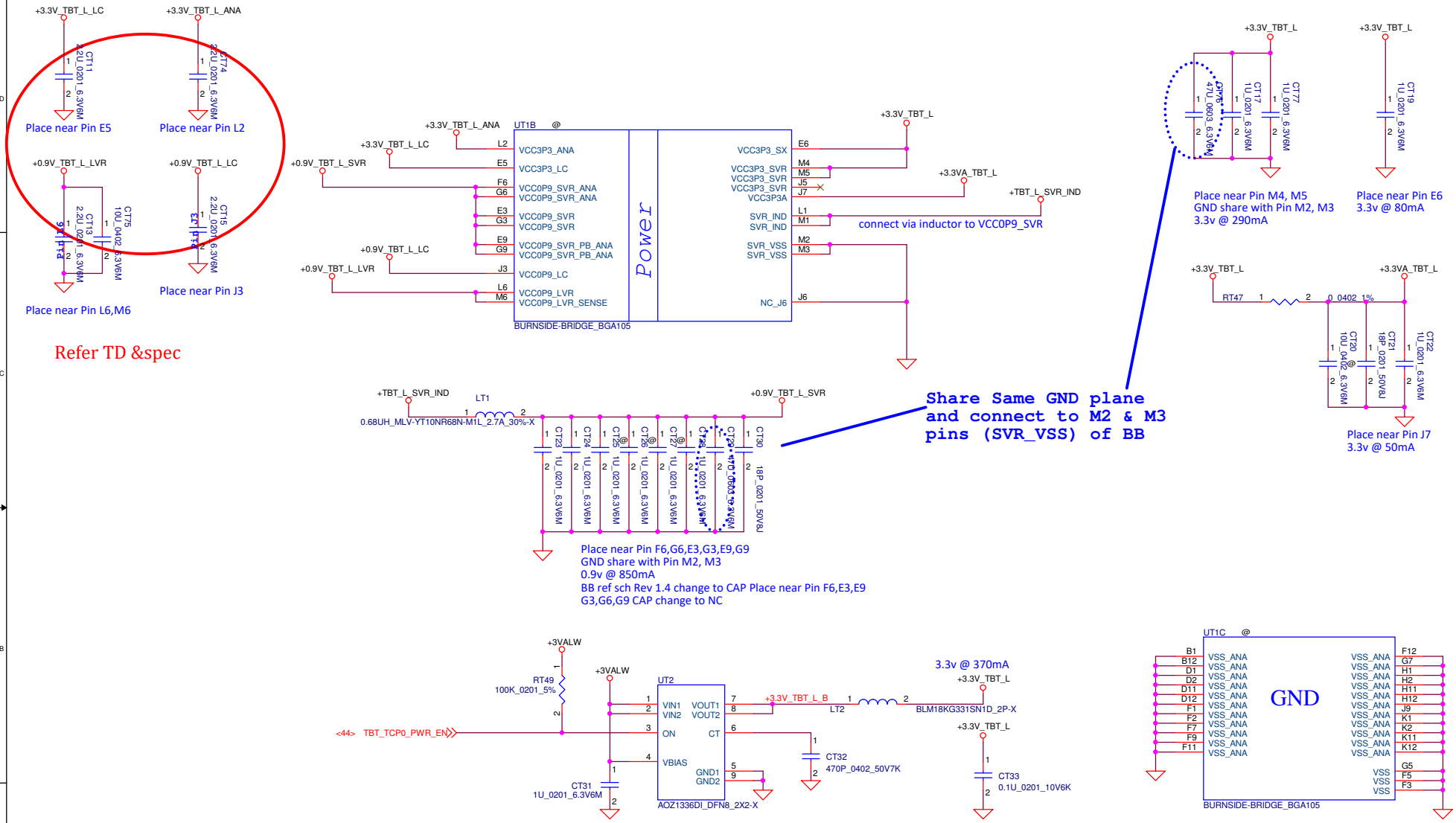
			Date: Monday, November 22, 2021 Sheet 42 of 80



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2021/12/31

Compal Electronics, Inc.

Title: **TypeC TBT_BB L_PWR,GND**

Size | Document Number: **LA-L651P** | Rev: 0.1

Date: Monday, November 22, 2021 | Sheet 43 of 80

Main Function:

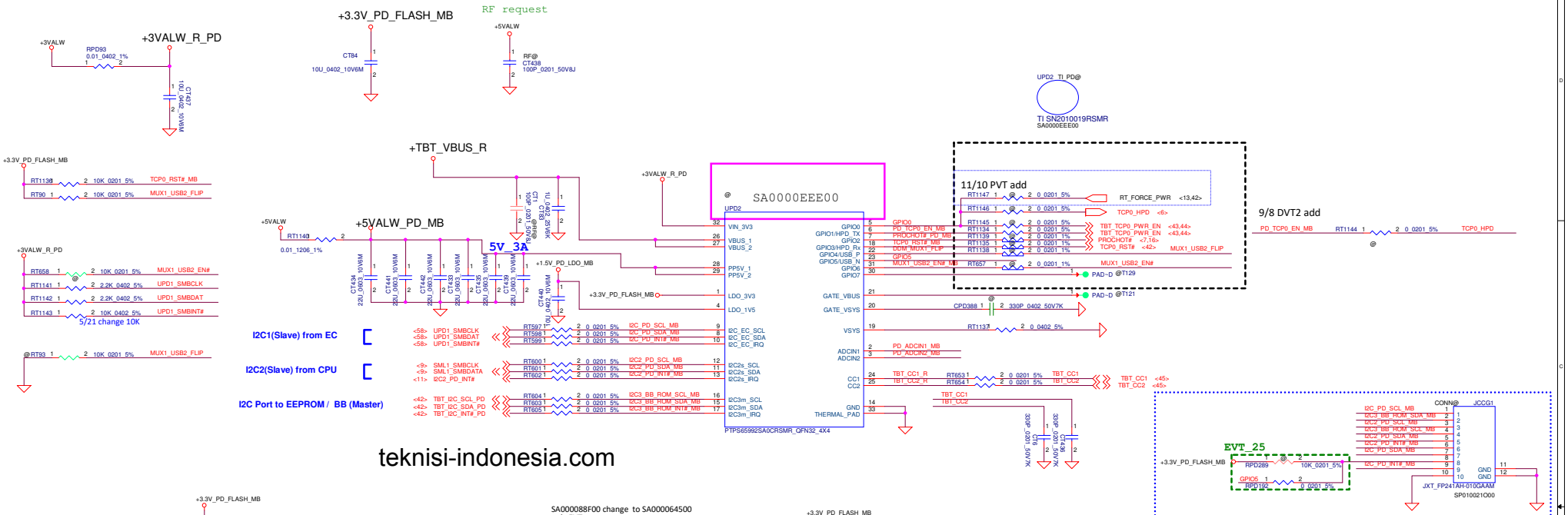


Table 2. Decoding of ADCIN1 and ADCIN2 Pins

DIV = R_{DOWN} / (R_{UP} + R_{DOWN})[1]		Without using R_{UP} or R_{DOWN}	ADCINx decoded value
MIN	MAX		
0	0.0228	tie to GND	0
0.0229	0.0722	N/A	1
0.0723	0.1425	N/A	2
0.1426	0.2372	N/A	3
0.2373	0.3671	N/A	4
0.3672	0.7064	tie to LDO_1V5	5
0.7065	0.8950	N/A	6
0.8951	1.0	tie to LDO_3V3	7

(1) External resistor tolerance of 1% is recommended. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

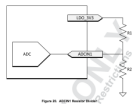


Table 5. I²C Default Slave Address for I2C_EC_SCL/SDA.

I²C address index (decoded from ADCIN1 and ADCIN2)[1]	Port	Slave Address								Available During BOOT
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
#1	A	0	1	0	0	0	0	0	R/W	Yes
#2	A	0	1	0	0	0	0	1	R/W	Yes
#3	A	0	1	0	0	0	1	0	R/W	Yes
#4	A	0	1	0	0	0	1	1	R/W	Yes

ADCIN1_PD:100K/10K = 0.09

ADCIN2_PD:NC/100K = 0

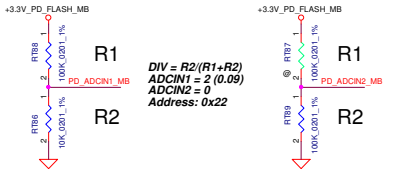


Table 6. Device Configuration using ADCIN1 and ADCIN2

ADCIN1 decoded value [1]	ADCIN2 decoded value [1]	I²C address index [2]	Dead Battery Configuration
7	5	#1	AlwaysEnableSink: The device always enables the sink path regardless of the amount of current the attached source is offering. USB PD is disabled until configuration is loaded.
5	5	#2	
2	2	#3	
1	7	#4	
7	4	#1	SinkRequires_3.0A: The device only enables the sink path if the attached source is offering at least 3.0A. USB PD is disabled until configuration is loaded.
4	4	#2	
3	0	#3	
2	7	#4	
7	6	#1	SinkRequires_1.5A: The device only enables the sink path if the attached source is offering at least 1.5A. USB PD is disabled until configuration is loaded.
6	6	#2	
6	5	#3	
6	7	#4	
7	3	#1	NegotiateHighVoltage: The device always enables the sink path during the initial implicit contract regardless of the amount of current the attached source is offering. The PD controller will enter the 'APP ' mode, enable USB PD PHY and negotiate a contract for the highest power contract that is offered up to 20 V.
3	3	#2	
4	0	#3	
3	7	#4	
7	0	#1	SafeMode: The device does not enable he sink path. USB PD is disabled until configuration is loaded. Note that the configuration could put the device into a source-only mode.
0	0	#2	
6	0	#3	
5	7	#4	

Table 4. Function table[1]

Input		Channel
S	OE	
L	L	D+ = 1D+, D– = 1D–
H	L	D+ = 2D+, D– = 2D–
X	H	switches off

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

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Issued Date	2020/03/05	Deciphered Date 2017/01/06	Title: TypeC PD TI
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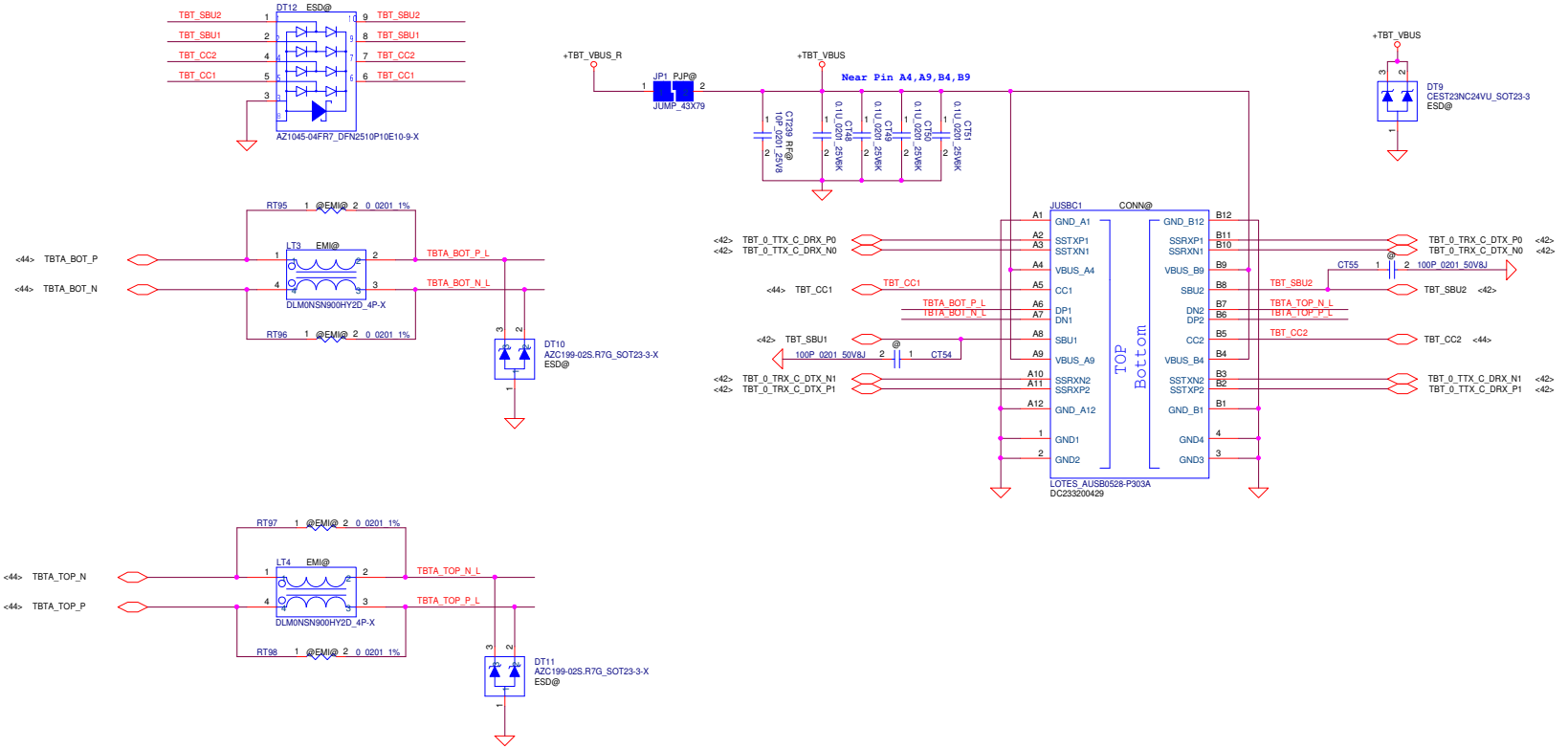
			Date: Wednesday, December 01, 2021; Sheet 44 of 80

Main Function:



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **TypeC CONN**

Size	Document Number	Rev
	LA-L651P	0.1

Date: Tuesday, November 23, 2021 Sheet 45 of 80

Reserve

Reserve

MOD_ID Settings			
Voltage Levels	MOD_ID1	MOD_ID2	Description
L0 = 0V	L0	NA	TBT Config1 (with BB Retimer)
L1 = VDDD/8	L1	NA	TBT Config2 (with BB Retimer)
L2 = 2*VDDD/8	L2	NA	non-TBT Config1 (with BB Retimer)
L3 = 3*VDDD/8	L3	NA	non-TBT Config2 (with BB Retimer)
L4 = 4*VDDD/8	L4	Reserved	Reserved
L5 = 5*VDDD/8	L5	Reserved	Reserved
L6 = 6*VDDD/8	L6	Mux1: L0 - L3 Mux2: L4 - L7	non-TBT Mux1 & Mux2 Configs
L7 = 7*VDDD/8	L7	Mux3: L0 - L3 Mux4: L4 - L7	non-TBT Mux3 & Mux4 Configs

Dell TGL Platform MOD_ID Options			
MUX	MOD_ID1	MOD_ID2	Description
BB8040R	L0	N/A	TBT Configuration w/BB Retimer
BB8010R	L2	N/A	non-TBT Configuration w/BB Retimer
TUSB546/1046	L6	L0	TUSB546 Equalizer config #1
TUSB546/1046	L6	L1 - L3	Reserved for TUSB546 Equalizer config #2,3,4 reserved

Compal Electronics, Inc.			
Title	TypeC PD_CCG6SF		
Size	Document Number		Rev
	LA-L651P		0.1
Date:	Monday, November 22, 2021	Sheet 46 of 80	

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: *RSV*

Size: B | Document Number: *LA-L651P* | Rev: 0.2

Date: Monday, November 22, 2021 | Sheet 47 of 80

Main Function:

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Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.		
Title: RSV		
Size: B	Document Number: LA-L651P	Rev: 0.2
Date: Monday, November 22, 2021	Sheet 48 of 80	

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: *RSV*

Size: Document Number: *LA-L651P* Rev: 0.2

Date: Monday, November 22, 2021 Sheet 49 of 80

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: *RSV*

Size: B29 | Document Number: *LA-L651P* | Rev: 0.2

Date: Monday, November 22, 2021 | Sheet 50 of 80

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

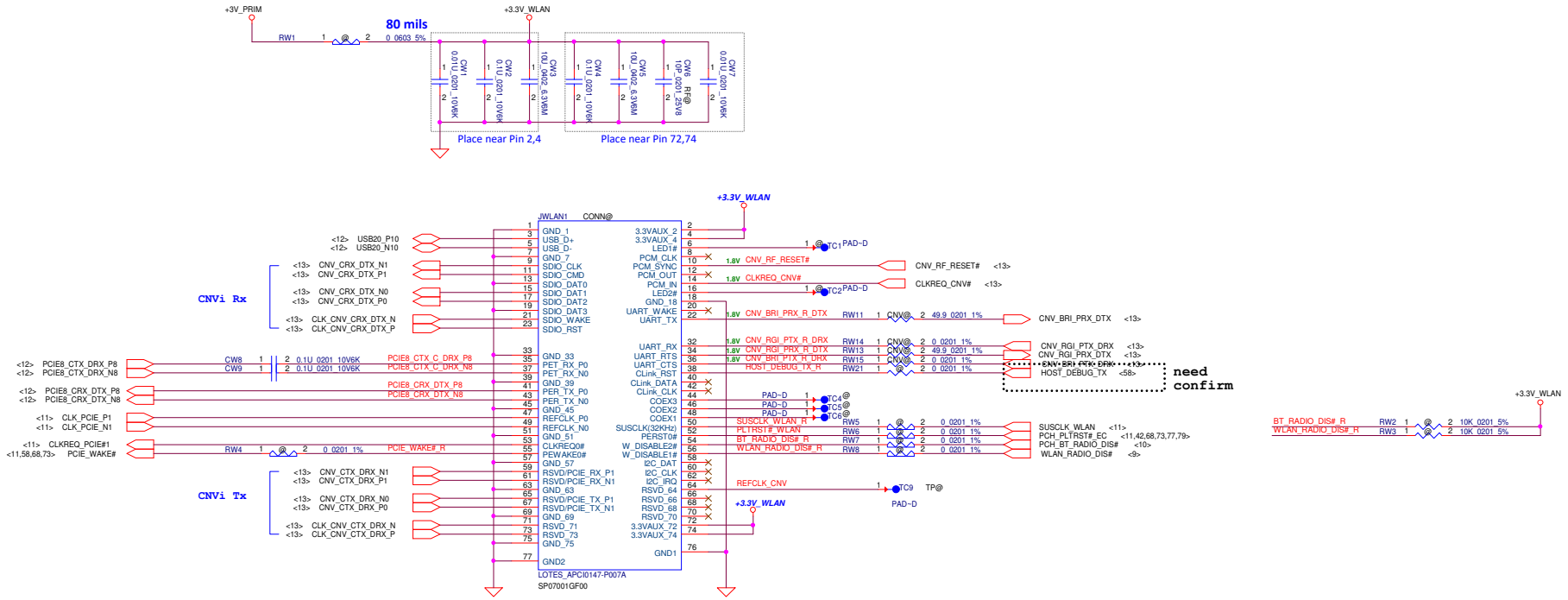
Compal Electronics, Inc.

Title: *RSV*

Size: B | Document Number: *LA-L651P* | Rev: 0.2

Date: Monday, November 22, 2021 | Sheet 51 of 80

Main Func = WLAN M.2



E Key CONN

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/10/01

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Compal Electronics, Inc.

Title: WLAN/BT (w/ CNVi) M.2

Size | Document Number: LA-L651P | Rev: 0.2

Date: Wednesday, November 24, 2021 | Sheet 52 of 80

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.		
Title: RSV		
Size: B2B	Document Number: LA-L651P	Rev: 0.2
Date: Monday, November 22, 2021	Sheet 53 of 80	

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.		
Title: RSV		
Size: B	Document Number: LA-L651P	Rev: 0.2
Date: Monday, November 22, 2021	Sheet 54 of 80	

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: *RSV*

Size: Document Number: *LA-L651P* Rev: 0.2

Date: Monday, November 22, 2021 Sheet 55 of 80

Title	<Title>
Size A	Document Number LA-L651P
Rev	<RevCo
Date:	Monday, November 22, 2021
Sheet	56 of 80

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: *RSV*

Size: Document Number: *LA-L651P* Rev: 0.2

Date: Monday, November 22, 2021 Sheet 57 of 80

Main Func = EC

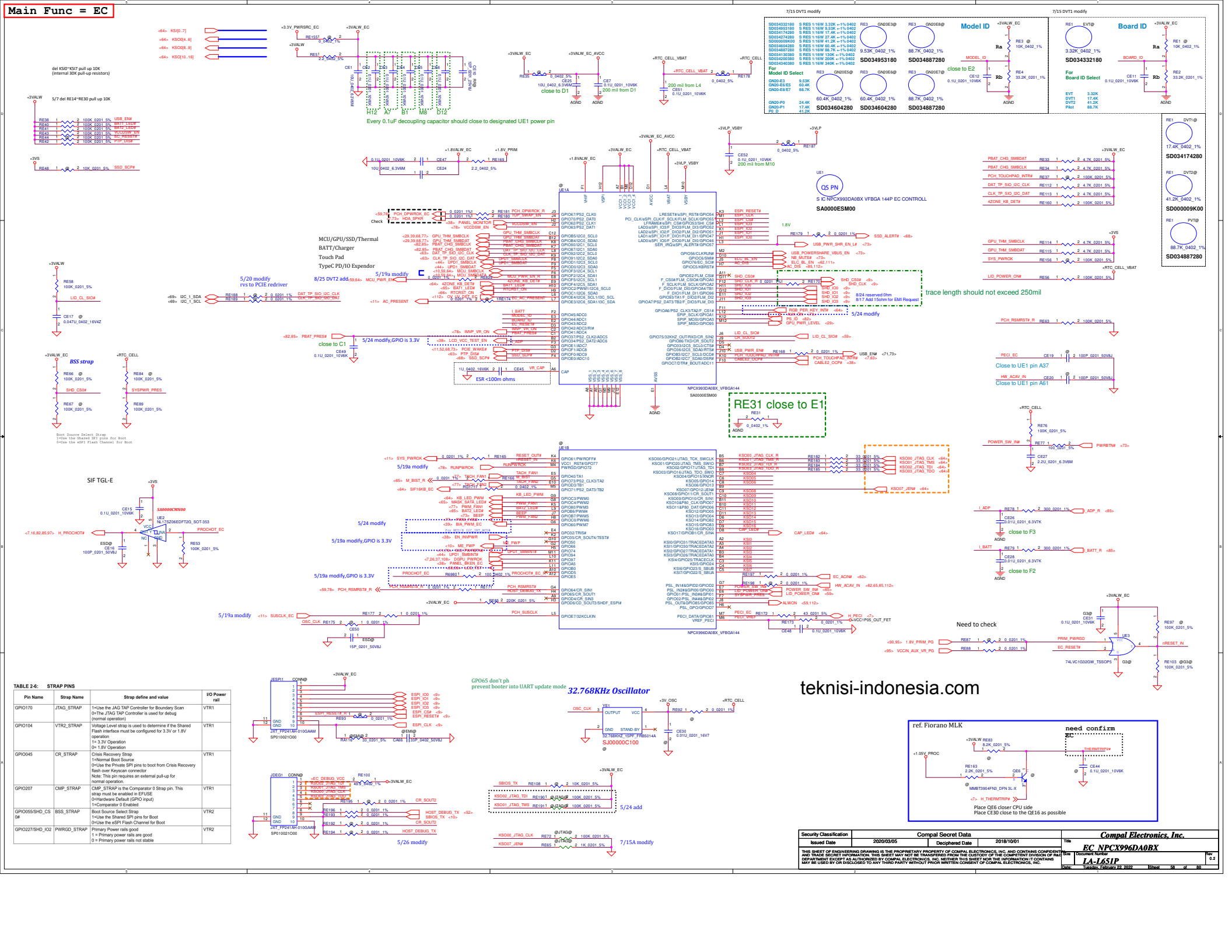


TABLE 2-6: STRAP PINS

Pin Name	Strap Name	Strap define and value	I/O Power rail
GPIO170	JTAG_STRAP	1=Use the JAG TAP Controller for Boundary Scan 0=The JTAG TAP Controller is used for debug (normal operation)	VTR1
GPIO104	VTR2_STRAP	Voltage Level strap is used to determine if the Shared Flash interface must be configured for 3.3V or 1.8V operation 1= 3.3V Operation 0= 1.8V Operation	VTR1
GPIO045	CR_STRAP	Crisis Recovery Strap 1=Normal Boot Source 0=Use the Private SPI pins to boot from Crisis Recovery flash over Keyscan connector Note: This pin requires an external pull-up for normal operation.	VTR1
GPIO207	CMP_STRAP	CMP_STRAP is the Comparator 0 Strap pin. This strap must be enabled in EFUSE 0=Hardwares Default (GPIO input) 1=Comparator 0 Enabled	VTR1
GPIO055/SHD_CS 0#	BSS_STRAP	Boot Source Select Strap 1=Use the Shared SPI pins for Boot 0=Use the eSPI Flash Channel for Boot	VTR2
GPIO227/SHD_IO2	PWRGD_STRAP	Primary Power rails good 1 = Primary power rails are good 0 = Primary power rails not stable	VTR2

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/10/01

Compal Electronics, Inc.			
Title	EC_NPCX996DA0BX		
Size	Document Number		Rev
	LA-L651P		0.2
Date:	Tuesday, February 22, 2022	Sheet	58 of 80

Main Func = GPIO Expander

Control Byte

0	1	0	0	A2	A1	A0	R/W

R/W = 0 = Write
R/W = 1 = Read
SMbus address 0x40

10/21 DVT1 modify from TP I2C to PD I2C

5/14 modify pin define

7/5 DVT1 modify

5/23 add

10/21 DVT1 Add

place close to UE4.14

8/25 DVT2 add

Add By 7/5 For IT8306 colay

8/25 DVT2 modify to MCU_PWR_EN_8306

FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{CLR}$	$\overline{A}$	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	↑	⎍
H	↓	H	⎍
↑	L	H	⎍

WDT

S5 LID CLOSE

11/4 DVT1 modify for material preparation
SC100000S00 change to SCS00006300

8/18 DVT2 modify to pop

7/20a DVT1 add for EC LID issue

5/14 vendor suggest PU or PD
8/25 Update for SIF 16

11/4 DVT1 modify for material preparation
SC100000S00 change to SCS00006300

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/10/01

Compal Electronics, Inc.

Title: GPIO Expander/WDT/S5 LID

Size | Document Number: LA-L651P | Rev: 0.2

Date: Wednesday, November 24, 2021 | Sheet 59 of 80

Main Function:

Reserve

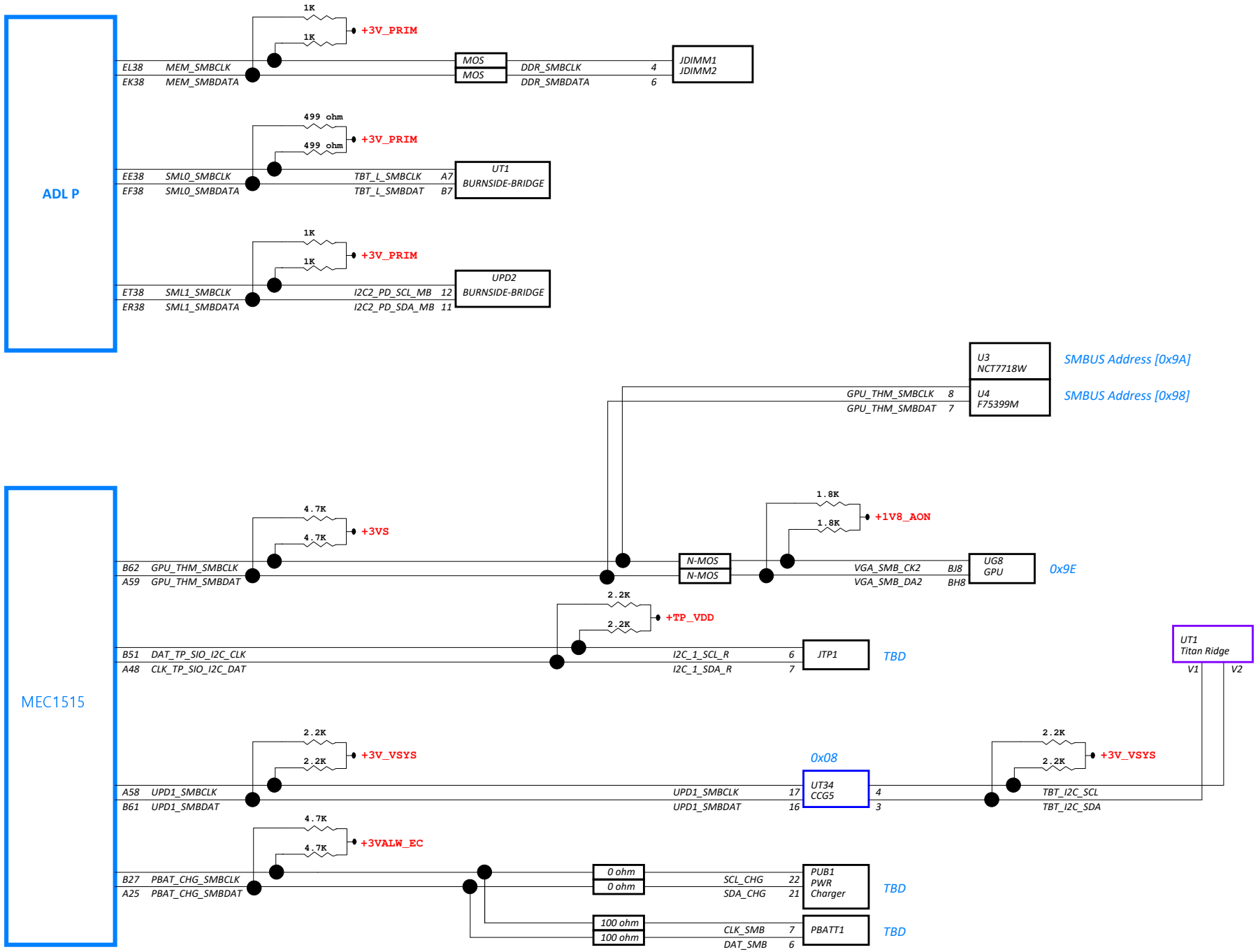
Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: *RSV*

Size: Document Number: *LA-L651P* Rev: 0.2

Date: Monday, November 22, 2021 Sheet 60 of 80



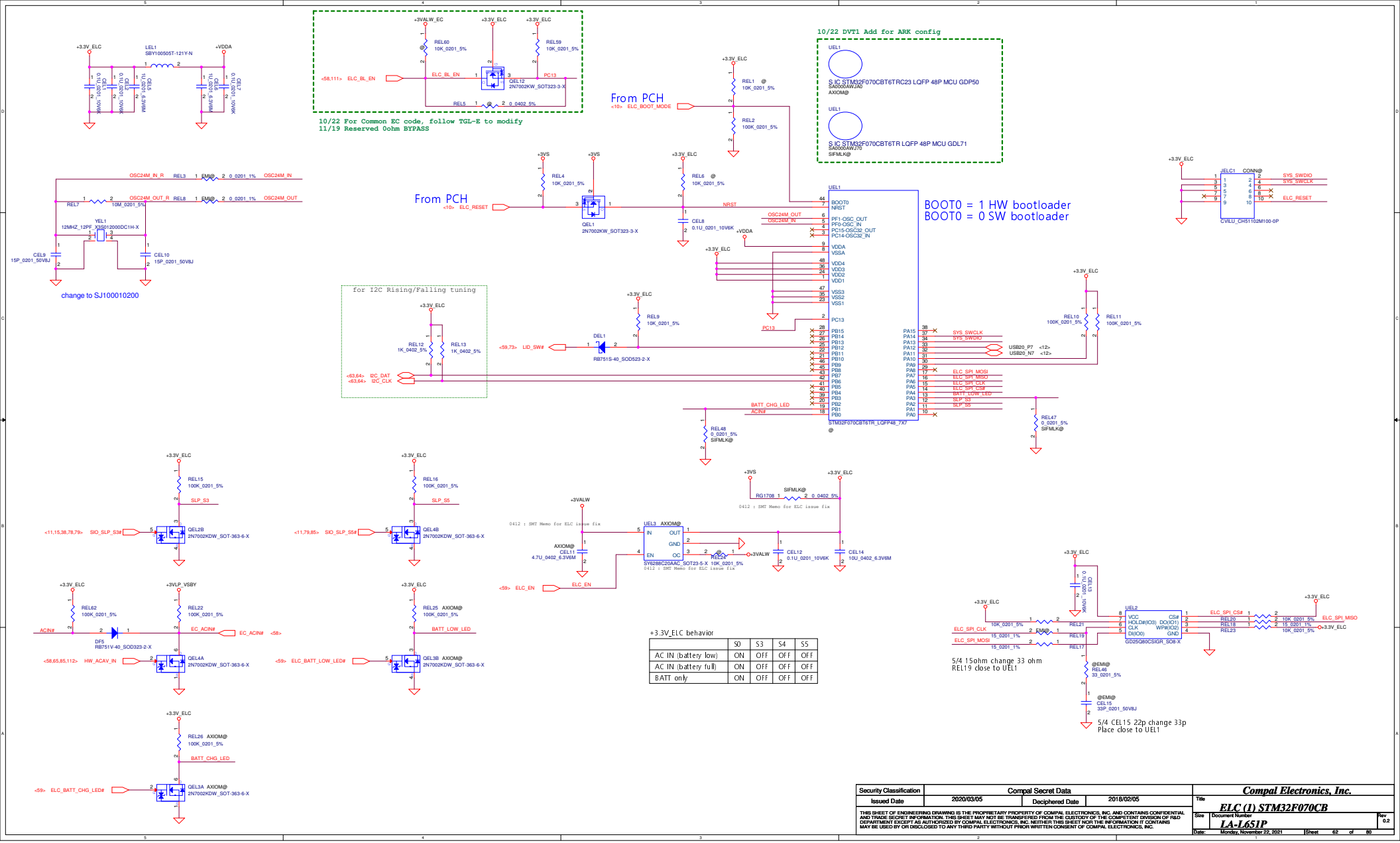
Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: SMBus Block Diagram

Size	Document Number	Rev
	LA-L651P	0.2

Date: Monday, November 22, 2021 Sheet 61 of 80


10/22 For Common EC code, follow TGL-E to modify
11/19 Reserved 0ohm BYPASS
10/22 DVT1 Add for ARK config
S IC STM32F070CBT6TRC23 LQFP 48P MCU GDP50
S IC STM32F070CBT6TR LQFP 48P MCU GDL71
From PCH
BOOT0 = 1 HW bootloader
BOOT0 = 0 SW bootloader
change to SJ100010200
for I2C Rising/Falling tuning
5/4 15ohm change 33 ohm
REL19 close to UEL1
5/4 CEL15 22p change 33p
Place close to UEL1
+3.3V_ELC behavior
S0 S3 S4 S5
AC IN (battery low) ON OFF OFF OFF
AC IN (battery full) ON OFF OFF OFF
BATT only ON OFF OFF OFF
Compal Secret Data
2020/03/05
2018/02/05
Compal Electronics, Inc.
ELC (1) STM32F070CB
LA-L651P
0.2
Monday, November 22, 2021
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Main Func = ELC

10/21 DVT1 Add

AXIOM

AD0 0
AD1 1
AD2 0
AD3 0

Vendor suggestion

06/09 Co-lay NXP ELC

7/5 DVT1 add

AD0 0
AD1 0
AD2 1
AD3 0

7/5 DVT1 modify

Main Func = Power LED

10/21 DVT1 Add

BAT1_LED#

BAT2_LED#

QEL8
SB00000R10 change to SB00001SN00
2nd SB00001WN00
need change footprint

Main Func = ON/OFF TRON

10/21 DVT1 Add

ISPD SP01001UP00 and SP010020U00 are substitute

Main Func = Touch pad

PCH/I2C

EC/I2C

Co-lay EC to PAD I2C/PS2

it's used for TP I2C (EC will do PS2 virturlization)
as control it in eFSA mode or BIOS menu

EC/PS2

Main Func = Primax Front Lighting

need to change to SP01002T200

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/02/05

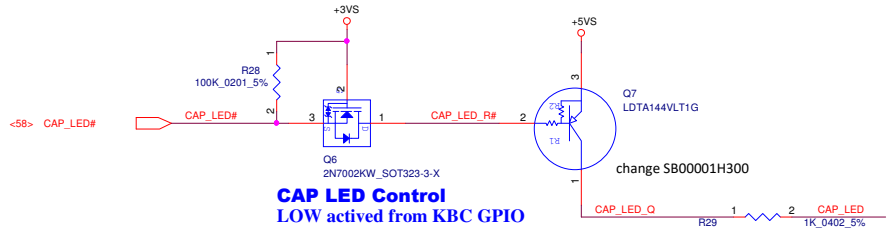
Compal Electronics, Inc.

Title: ELC (2) TP/PWR/TRON

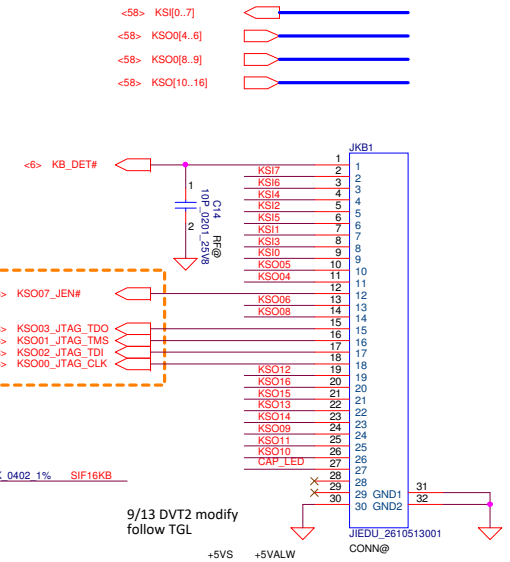
Size: LA-L651P | Document Number | Rev: 0.2

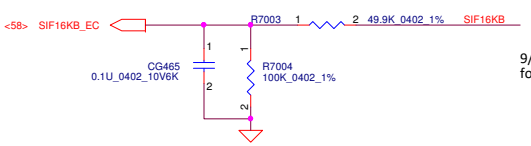
Date: Monday, November 22, 2021 | Sheet 83 of 90

Main Func = KB/KBBL

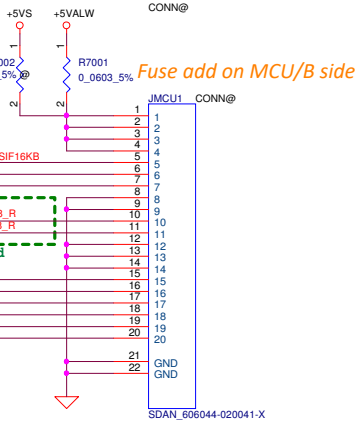


CAP LED Control
LOW actived from KBC GPIO





9/13 DVT2 modify
follow TGL

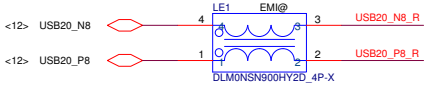


Fuse add on MCU/B side

+3VS Change to +3VALW for Modern Stanby
follow SIF MLK AMD

PD on MCU/B side

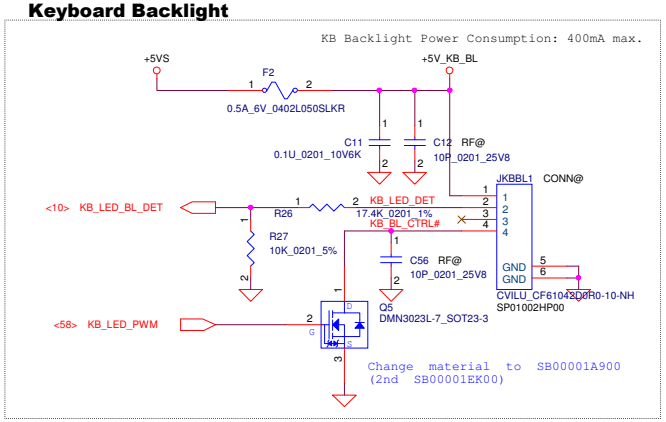
10/21 DVT1 Add



10/21 DVT1 Add

SIF only

Keyboard Backlight



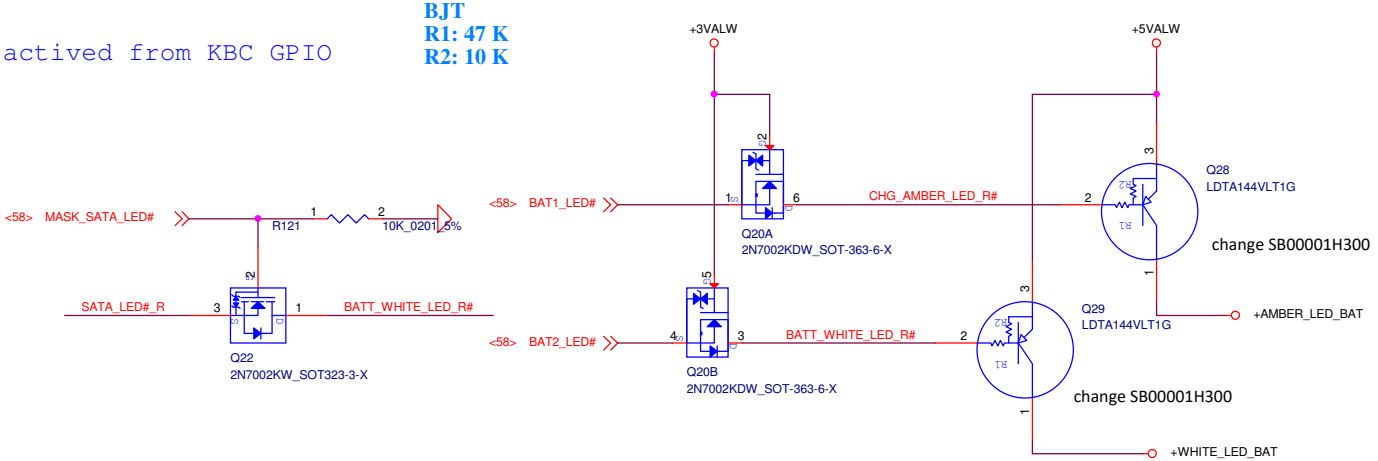
Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/02/05

Compal Electronics, Inc.			
Title: MCU Per Key/4 Zone KB			
Size	Document Number: LA-L651P		Rev: 0.2
Date: Monday, November 22, 2021		Sheet 64 of 80	

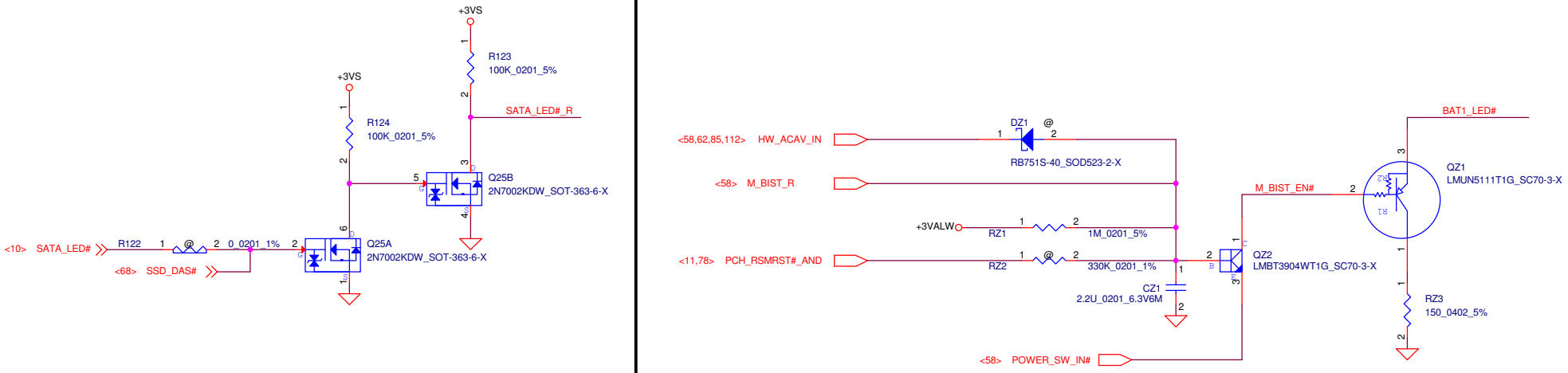
Main Func = Battery LED

Low actived from KBC GPIO

BJT
R1: 47 K
R2: 10 K



Main Func = M_BIST



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2019/04/01

Compal Electronics, Inc.

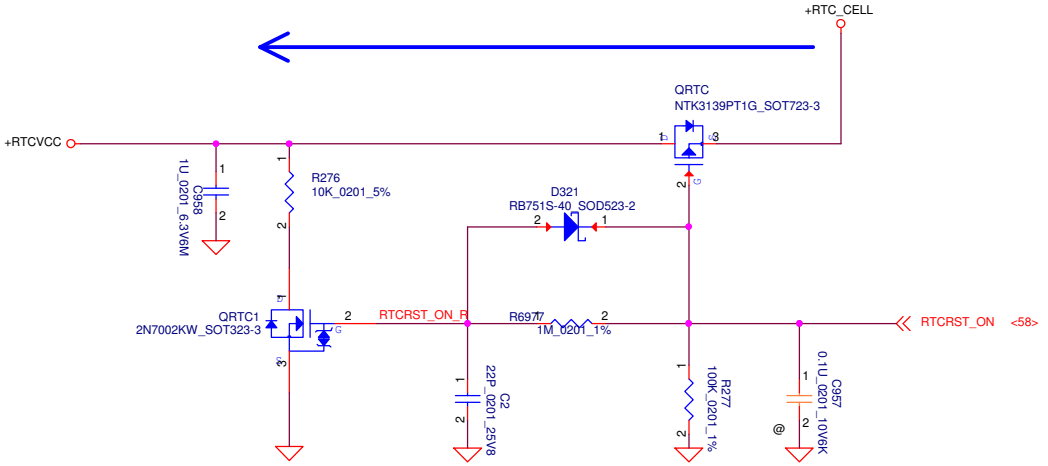
Title: **LED (SIF)**

Size: B | Document Number: **LA-L651P** | Rev: 0.2

Date: Wednesday, November 24, 2021 | Sheet 65 of 80

Main Func = RTC Gen9

Default: OD EC drives GPIOs to LOW to turn ON power to VCCRTC.



follow Intel Keep old RTC
X9&X8 RTC discharge schematic

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: RTC Gen9

Size: B | Document Number: LA-L651P | Rev: 0.2

Date: Monday, November 22, 2021 | Sheet 66 of 80

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.

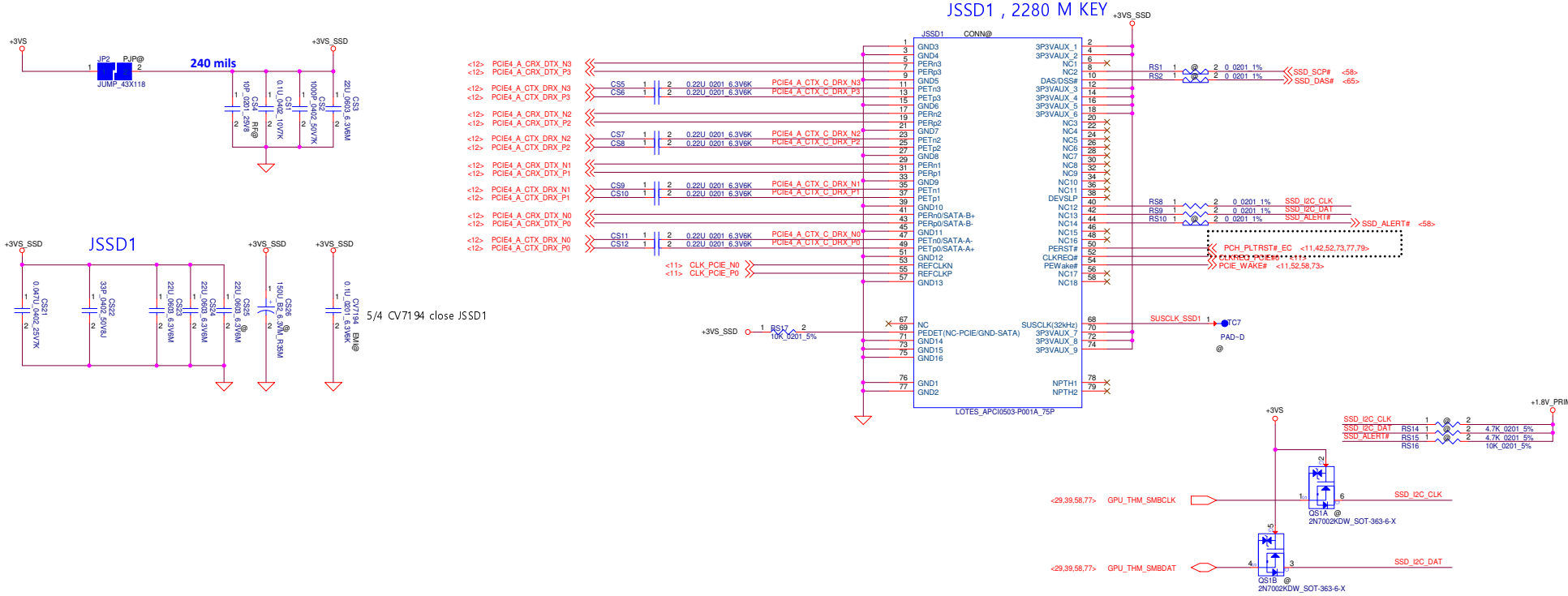
Title: *RSV*

Size | Document Number: *LA-L651P* | Rev: 0.2

Date: Monday, November 22, 2021 | Sheet 67 of 80

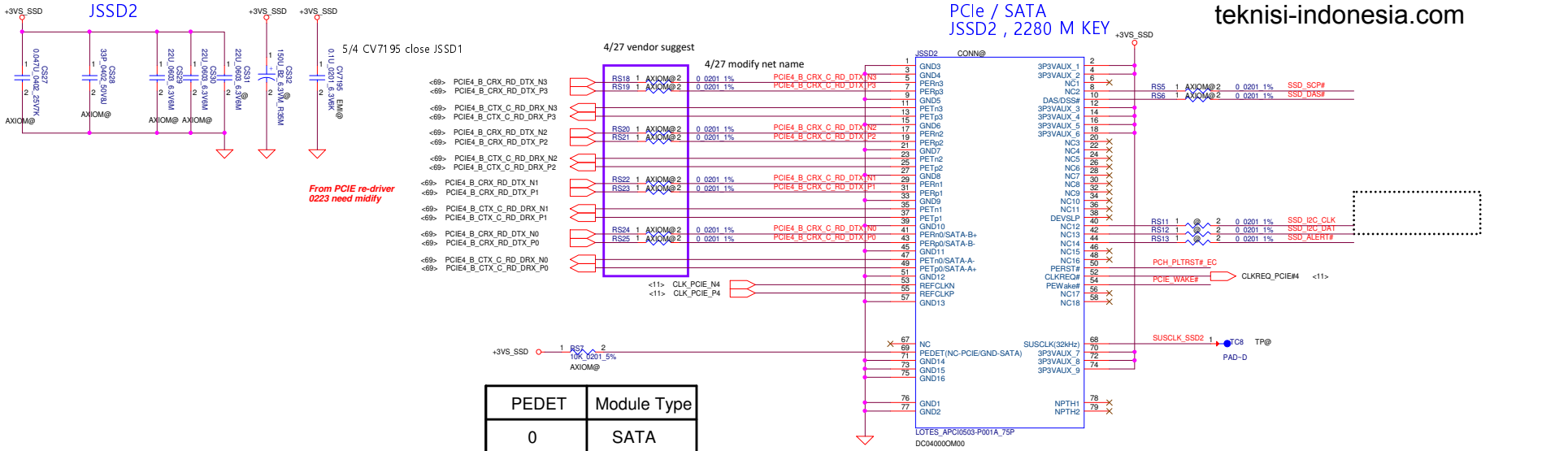
7/7 modify footprint

PCIe GEN4
JSSD1 , 2280 M KEY



7/7 modify footprint

PCIe / SATA
JSSD2 , 2280 M KEY



teknisi-indonesia.com

PEDET	Module Type
0	SATA
1	PCIe

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/02/05

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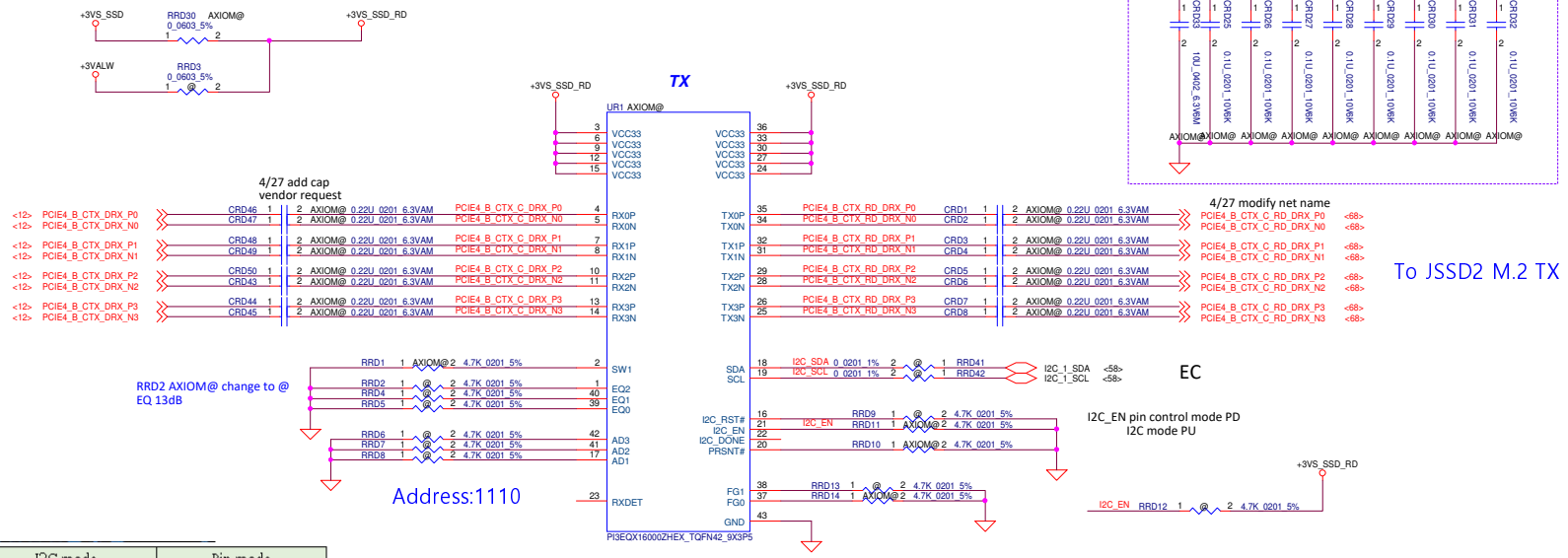
Compal Electronics, Inc.

Title: **NGFF SSD x2**

Size: | Document Number: **LA-L651P** | Rev: 0.2

Date: Wednesday, November 24, 2021 | Sheet 68 of 80

Main Function:



	I2C mode	Pin mode
RRD12/RRD23	擇一上件即可	都不上件
RRD41/RRD43	擇一上件即可	都不上件
RRD42/RRD44	擇一上件即可	都不上件
RRD11	不上件	上件
RRD24	不上件	上件

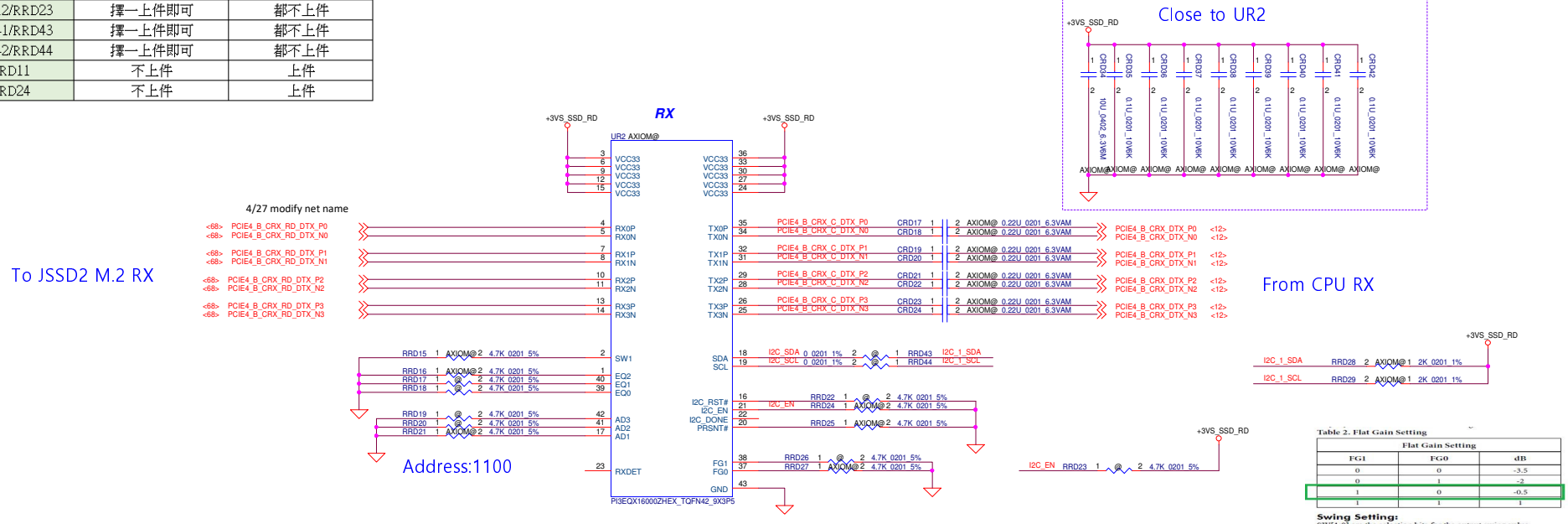


Table 1. Equalization Setting

Equalizer Setting (dB)						
EQ2	EQ1	EQ0	@1.25GHz	@2.5GHz	@4GHz	@8GHz
0	0	0	0.2	1.0	2.3	5.6
0	0	1	0.2	1.1	2.6	6.2
0	1	0	1.8	2.7	3.9	7.0
0	1	1	2.1	3.3	4.8	8.5
1	0	0	3.0	4.2	5.8	9.4
1	0	1	3.2	4.6	6.5	10.4
1	1	0	4.3	5.8	7.8	11.7
1	1	1	4.5	6.5	8.8	13.0

Table 2. Flat Gain Setting

Flat Gain Setting		
FG1	FG0	dB
0	0	-3.5
0	1	-2
1	0	-0.5
1	1	1

Swing Setting:
SW[1:0] are the selection bits for the output swing value.

Table 3. Swing Setting

Output Swing Setting		
SW1	SW0	mVp-p
0	0	800
0	1	1000
1	0	1100
1	1	1200

Note: SW0 is from I2C, SW1 is from pin or I2C.

Compal Electronics, Inc.

Title: RSV

Size: | Document Number: LA-L651P | Rev: 0.1

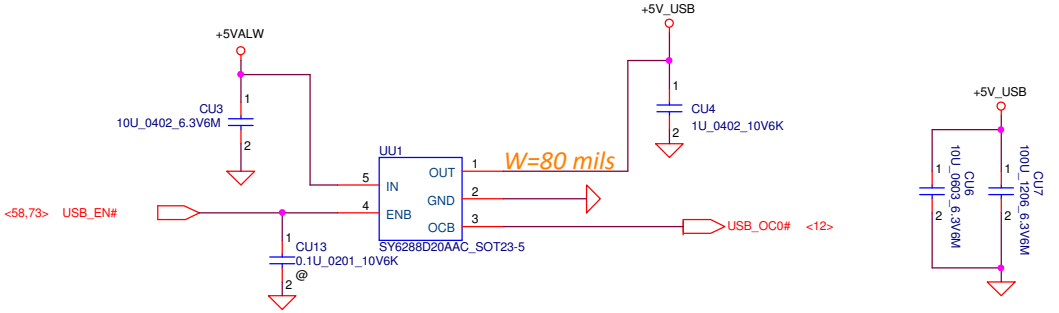
Date: Monday, November 22, 2021 | Sheet 69 of 80

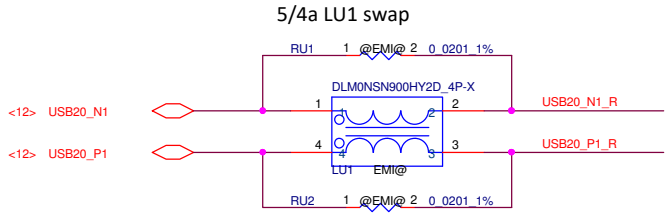
Main Function:

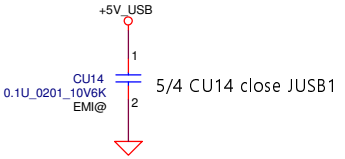
Reserve

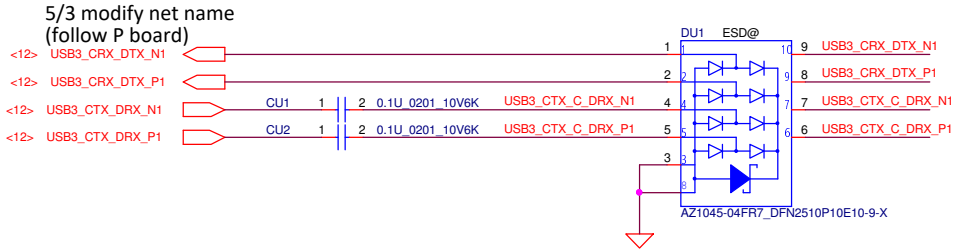
Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

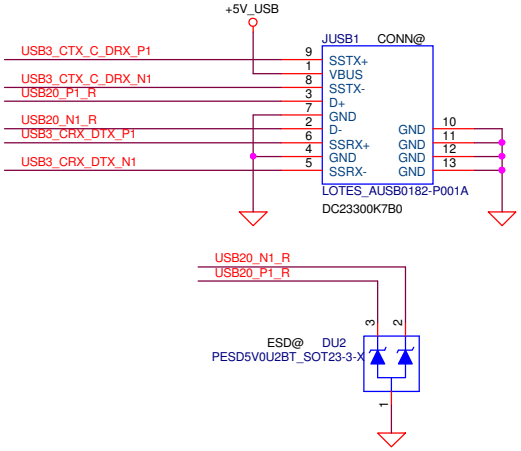
Compal Electronics, Inc.		
Title: RSV		
Size: B	Document Number: LA-L651P	Rev: 0.2
Date: Monday, November 22, 2021	Sheet 70 of 80	











Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **USB3.1 TypeA Gen1**

Size | Document Number: **LA-L651P** | Rev: 0.2

Date: Tuesday, November 23, 2021 | Sheet 71 of 80

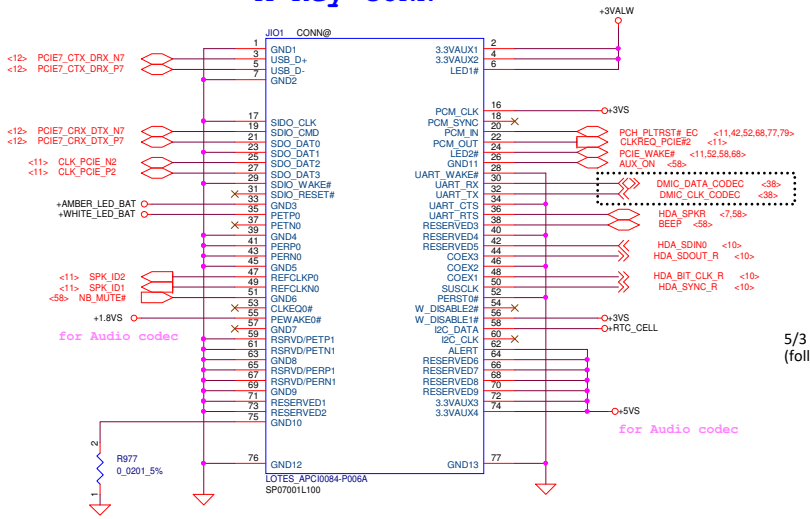
Main Function:

Reserve

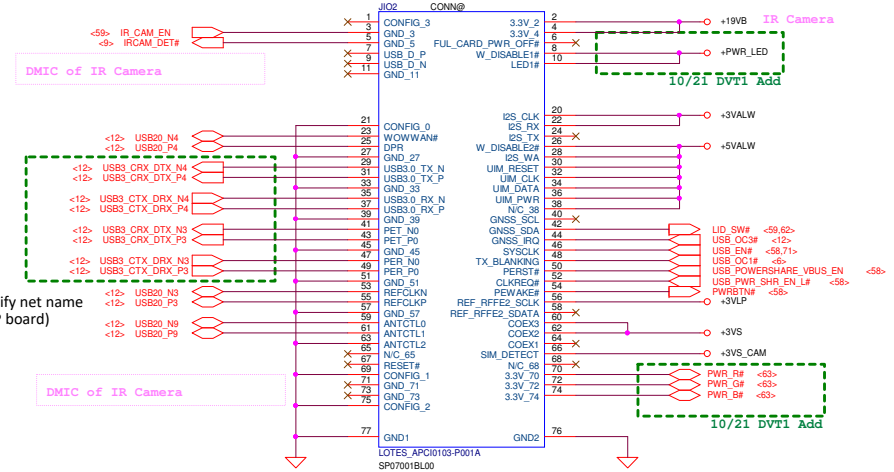
Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.		
Title: RSV		
Size: B	Document Number: LA-L651P	Rev: 0.2
Date: Monday, November 22, 2021	Sheet 72 of 80	

A Key CONN



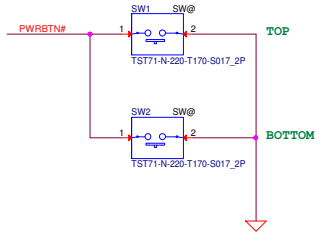
B Key CONN



5/3 modify net name
(follow P board)

For LAN DB CONN (LEFT)

For USB DB CONN (RIGHT)



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/02/05

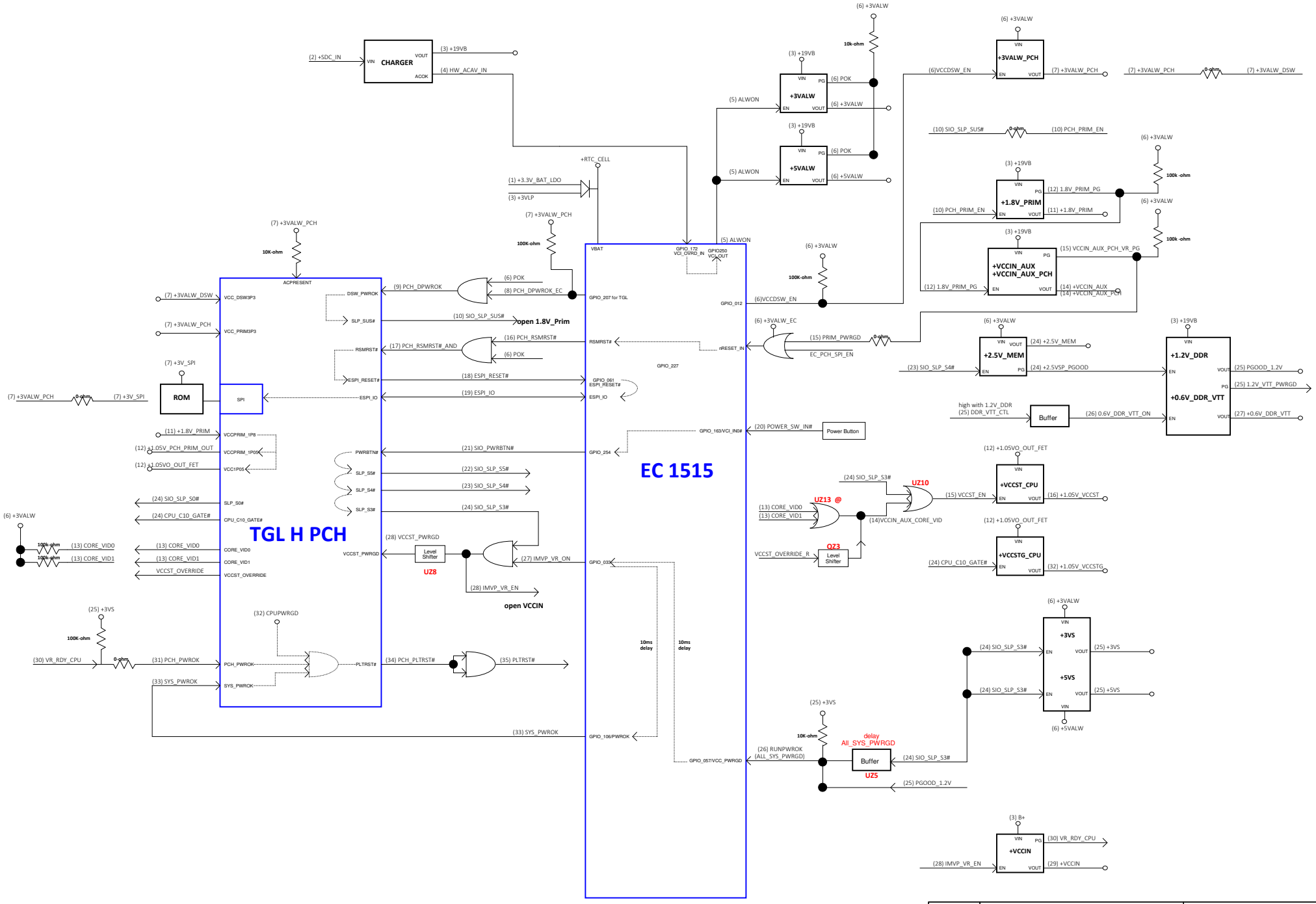
Compal Electronics, Inc.			
Title: IO Board CONN			
Size	Document Number: LA-L651P		Rev: 0.2
Date: Monday, November 22, 2021		Sheet 73 of 80	

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2019/04/01

Compal Electronics, Inc.		
Title: DOCK(RSVD)		
Size: B2B	Document Number: LA-L651P	Rev: 0.2
Date: Monday, November 22, 2021	Sheet 74 of 80	

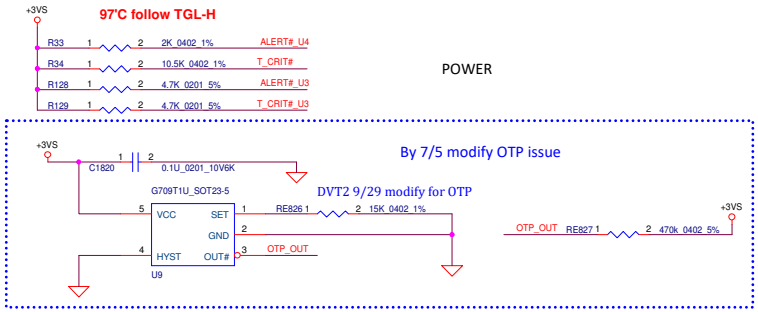

CHARGER
+3VALW
+5VALW
+3VALW_PCH
+1.8V_PRIM
+VCCIN_AUX
+VCCIN_AUX_PCH
+2.5V_MEM
+1.2V_DDR
+0.6V_DDR_VTT
+VCCST_CPU
+VCCSTG_CPU
+3VS
+5VS
+VCCIN
ROM
SPI
TGL H PCH
EC 1515
Power Button
Buffer
Level Shifter
UZ8
UZ10
UZ13 @
QZ3
UZ5
open 1.8V_Prim
open VCCIN
delay All_SYS_PWRGD
Compal Secret Data
Compal Electronics, Inc.
Power Sequence Diagram
LA-L651P

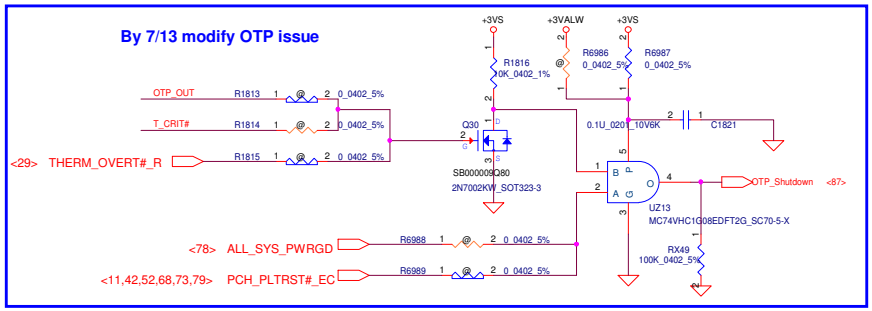
Main Function:

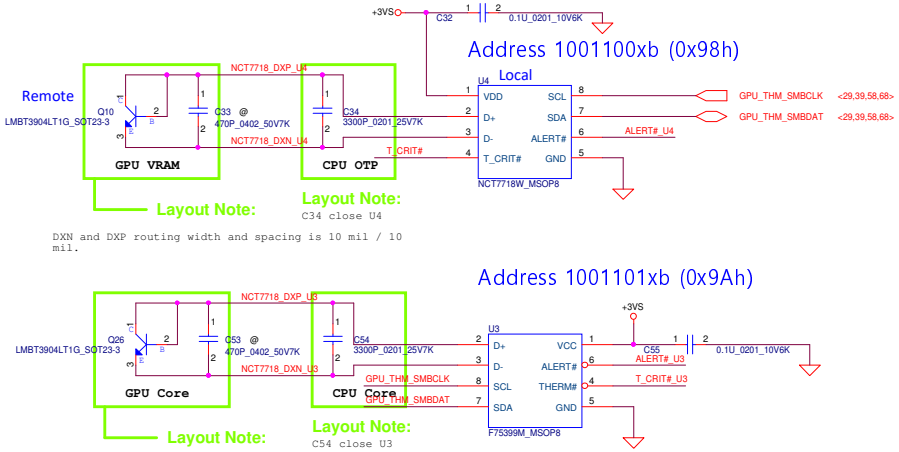
Reserve

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

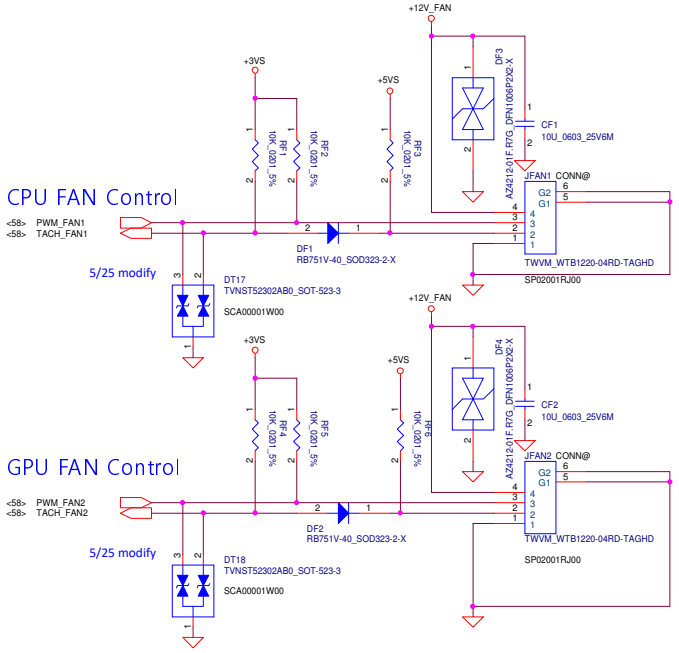
Compal Electronics, Inc.		
Title: RSV		
Size: B	Document Number: LA-L651P	Rev: 0.2
Date: Monday, November 22, 2021	Sheet 76 of 80	







TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

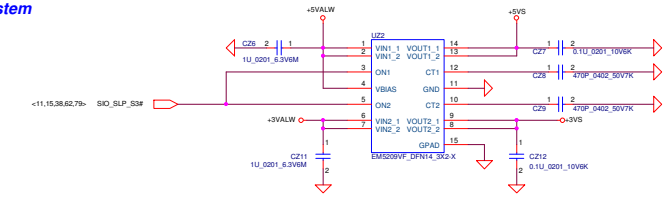


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date	2018/02/05

Title	FAN/Thermal		
Size	Document Number		Rev
	LA-L651P		0.2
Date:	Tuesday, November 23, 2021	Sheet	77 of 80

Main Func = DC/DC

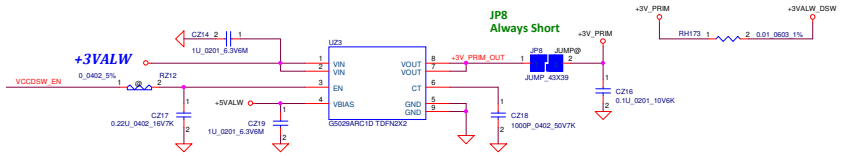
+5VALW to +5VS for System
+3VALW to +3VS for System



+3VALW TO +3VALW_PCH

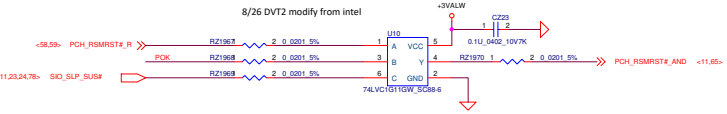
+3VALW_DSW Source

JP8 Always Short



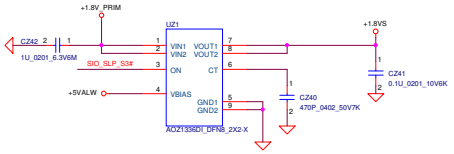
RSMRST circuit

8/26 DVT2 modify from intel



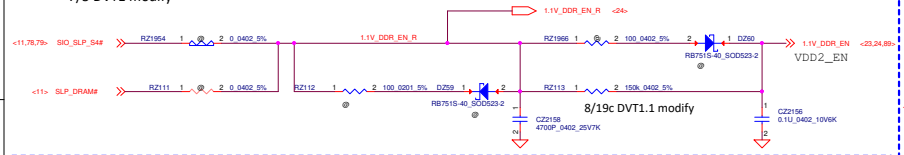
11/18 Pilot reserve for U10 shortage

+1.8VS for System,Audio



VDD2 ENABLE SIGNAL GENERATION (Follow Intel 631621 RVP rev1p0)

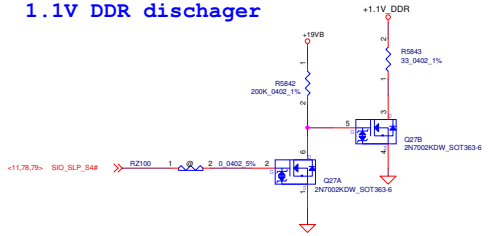
7/5 DVT1 modify



8/19c DVT1.1 modify

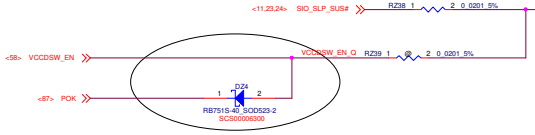
+1.1V

1.1V DDR dischager



Sequence Logic

Enable +1.2V_DDR

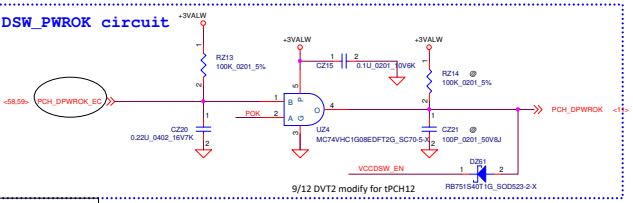


POWER

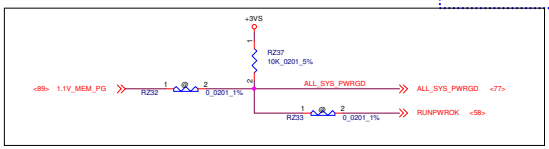
Enable +1.8V_PRIM

IMVP_VR_ON&VCCST_PWRGD

DSW_PWROK circuit

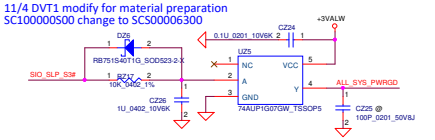


9/12 DVT2 modify for tPCH12

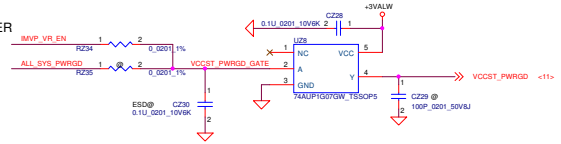


Buffer with Open Drain Output For ALL_SYS_PWRGD

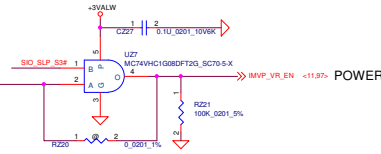
11/4 DVT1 modify for material preparation
SC100000500 change to SCS00006300



Buffer with Open Drain Output For H_VCCST_PWRGD



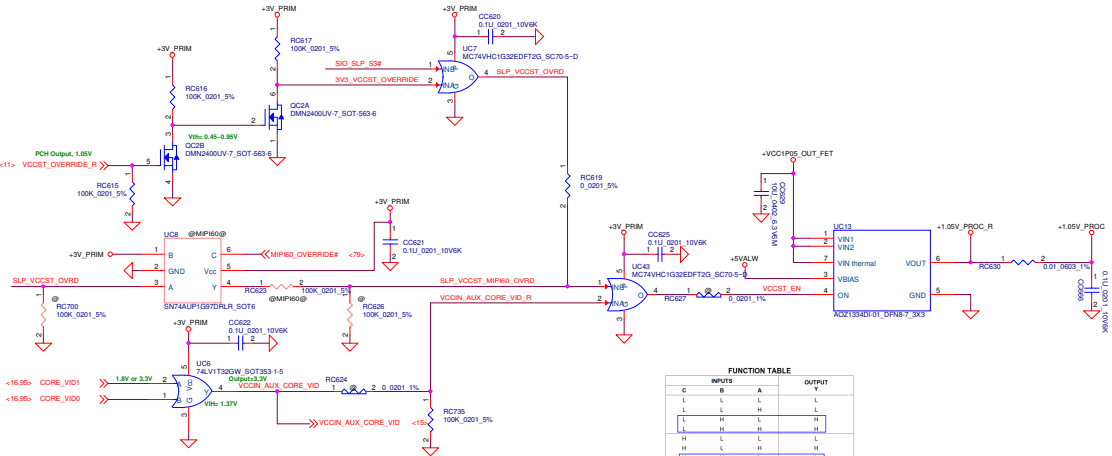
EC



POWER

11/4 DVT1 modify for material preparation
SA00000OH00 change to SA0000BIP00

+1.05V_PROC



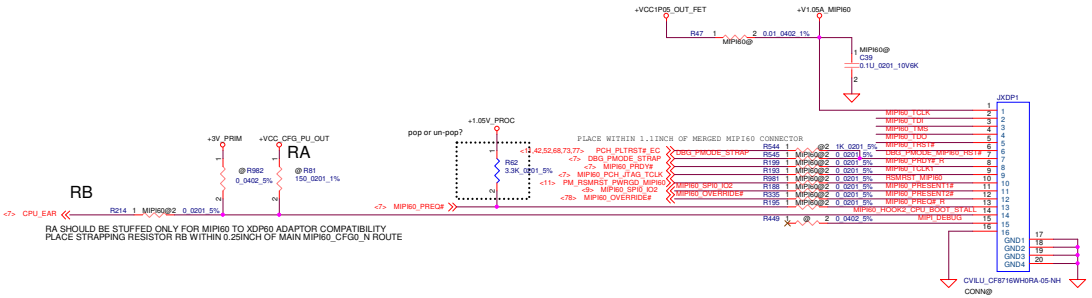
FUNCTION TABLE

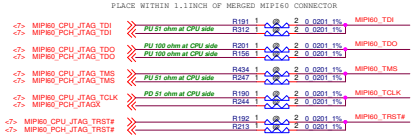
INPUTS C	INPUTS B	INPUTS A	OUTPUT Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title: DC/DC Interface			
Size:	Document Number: LA-L651P		Rev: 0.2
Date: Thursday, February 10, 2022	Sheet 78 of 80		

MIPI 60





CFG Config

11/25 DVT1 modify to pull high

PEG x16 Lane reversal

0: Reversal

1: Non-Reversal

eDP enable strap

0 : enable

1 : disable

PCIE16 Port Bifurcation - CGF[6:5]

11 : x16 (Default)
10 : x8, x8
01 : Reserved
00 : x8,x4,x4

PCIE4 Lane Reversal

0 : Reseved

1 : Normal (default)

E3
Power Monitor

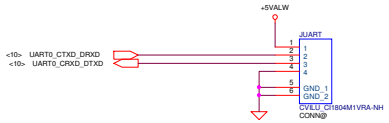
RB14 Close to F1
RB1 Close to F1
RB2 Close to R8
RB3 Close to R8
RB4 Close to PCZ34
RB15 Close to PCZ34
RB5 Close to PRB01
RB6 Close to PRB01

RB13 Close to RW1
RB7 Close to RW1
RB8 Close to RS32
RB9 Close to RS32
RB10 Close to PJPM01
RB16 Close to PJPM01
RB11 Close to PJG2
RB12 Close to PJG2

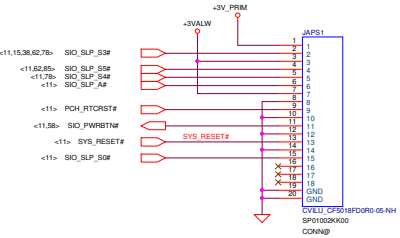
2	4	6	8	10	12	14	16	18	20
P1+	P1-	P2+	P2-	CLK	GND	P7-	P7+	P8-	P8+

P4+	P4-	P3+	P3-	DATA	3.3V	P6-	P6+	P5-	P5+
1	3	5	7	9	11	13	15	17	19

BIOS UART Debug



APS



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/10/01

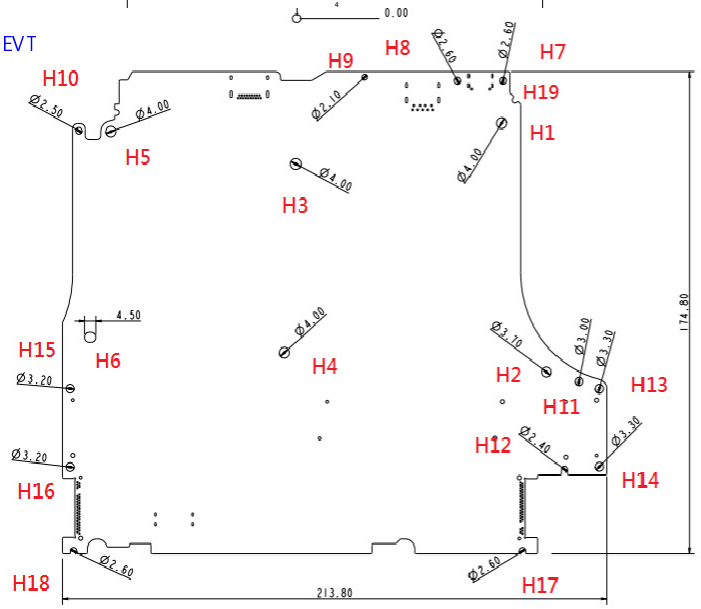
Compal Electronics, Inc.

Title: Debug APS,DEG

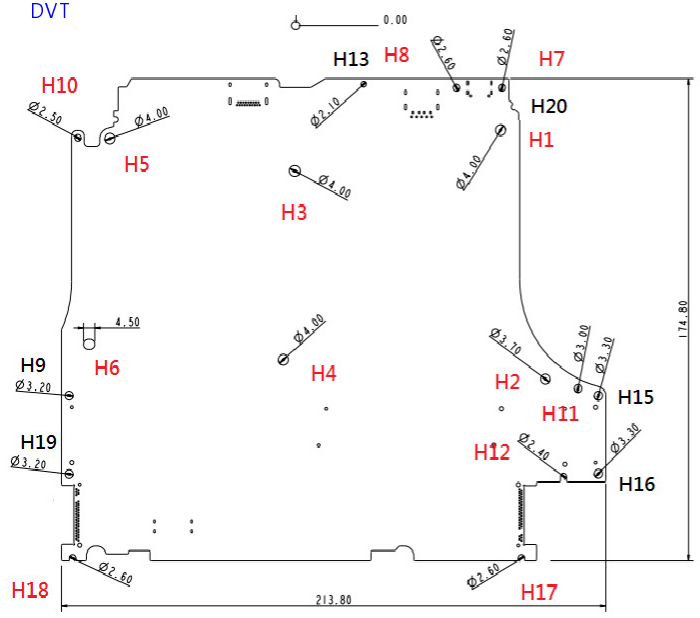
Size: Document Number: LA-L651P Rev: 0.2

Date: Wednesday, November 24, 2021 Sheet 79 of 80

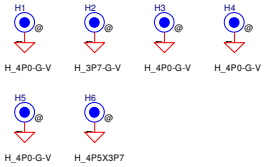
EVT



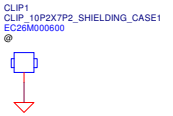
DVT



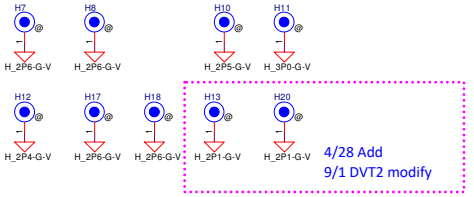
CPU & GPU



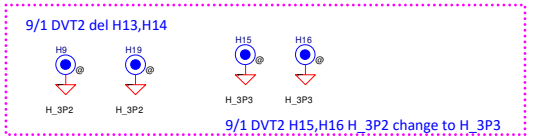
SHIELDING CASE



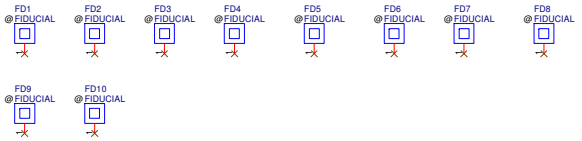
PTH



Stand-off



Fiducial Mark



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/02/05

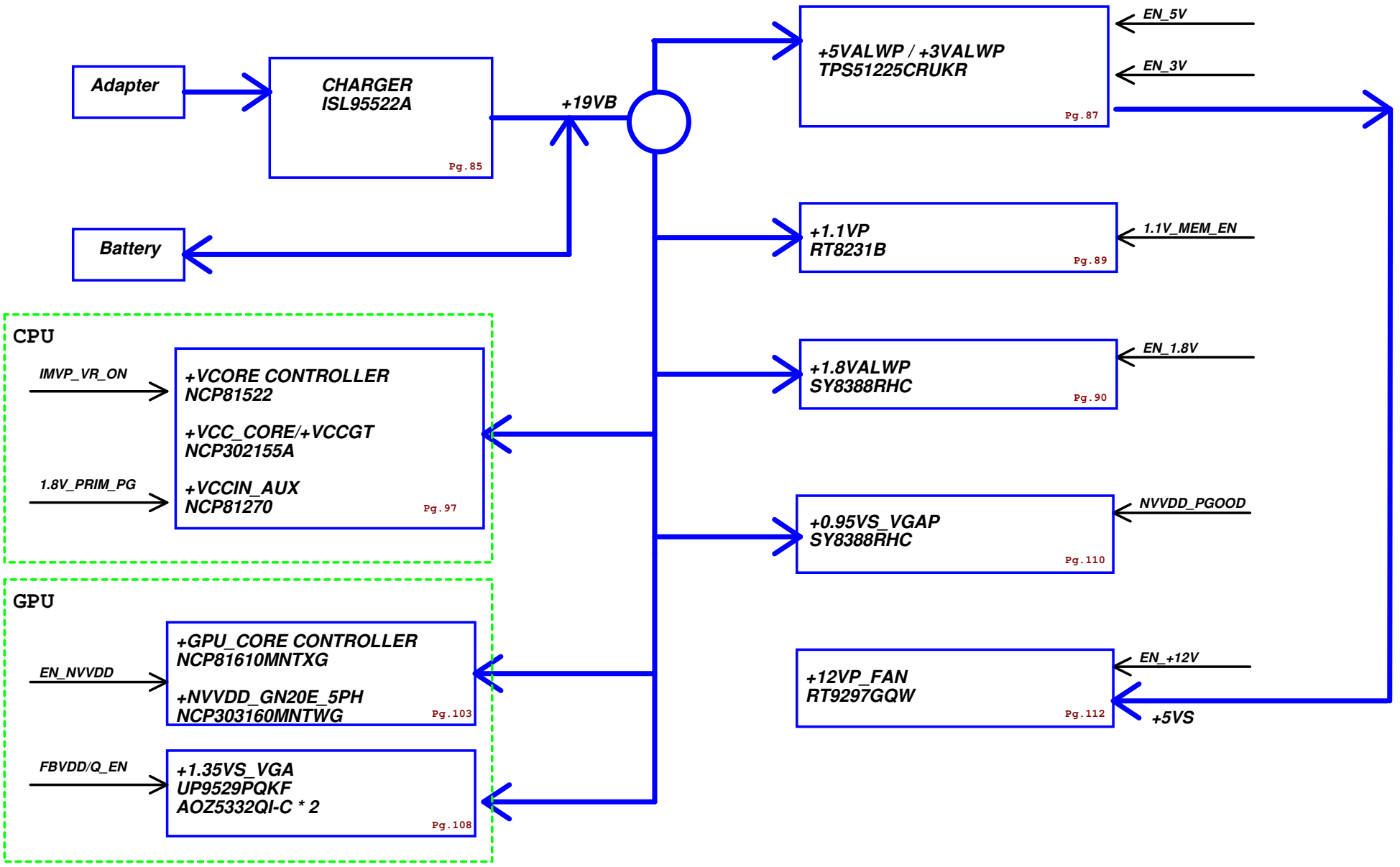
Compal Electronics, Inc.

Title: **Screw Hole**

Size | Document Number: **LA-L651P** | Rev: 0.2

Date: Monday, November 22, 2021 | Sheet 80 of 80

Power block



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2021/08/01

Compal Electronics, Inc.			
Title	PWR_POWER BLOCK DIAGRAM		
Size	Document Number		Rev
	LA-L651P		0.1
Date:	Monday, November 22, 2021	Sheet	81 of 120

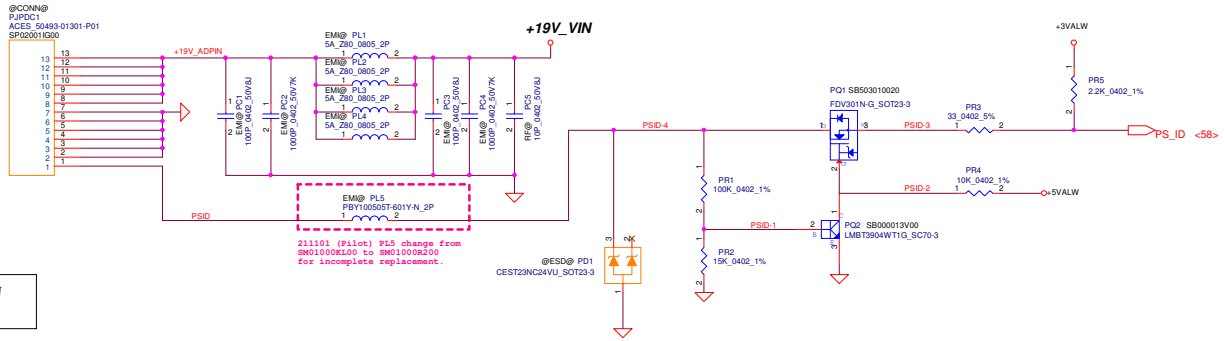
Main Func = DCIN CONN

Adapter Connector

Adapter Bot Side

PIN1 PSID
PIN2 GND
PIN3 GND
PIN4 GND
PIN5 GND
PIN6 GND
PIN7 GND
PIN8 ADPIN
PIN9 ADPIN
PIN10 ADPIN
PIN11 ADPIN
PIN12 ADPIN
PIN13 ADPIN
ACES_50493-01301-P01

Adapter 180W / 240W
240W/19V=12.63A



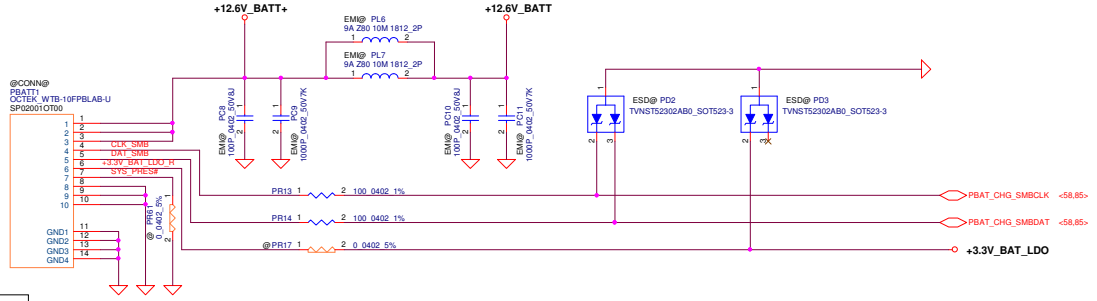
Main Func = BATT CONN

Battery Connector

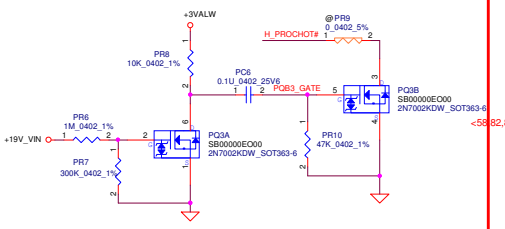
Battery Bot Side

PIN10 GND
PIN09 GND
PIN08 GND
PIN07 SYS_PRES#
PIN06 BATT_PRS#
PIN05 DAT_SMB
PIN04 CLK_SMB
PIN03 BATT+
PIN02 BATT+
PIN01 BATT+
SP07001R500

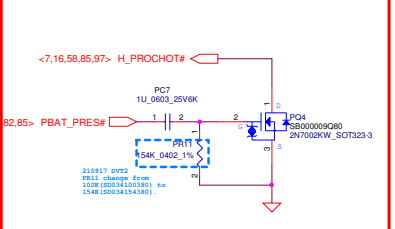
Battery 56W
56W/11.4V=4.91A
Battery 86W
86W/11.4V=7.54A

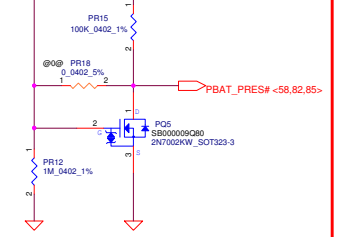


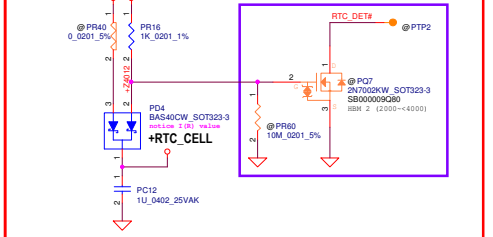
Adapter protection:



Battery protection:







Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.			
Title	PWR_DCIN / OTP / BATT CONN / RTC		
Size	Document Number		Rev
	LA-L651P		0.1
Date: Monday, November 22, 2021	Sheet 82 of 120		

Reserve

Reserve

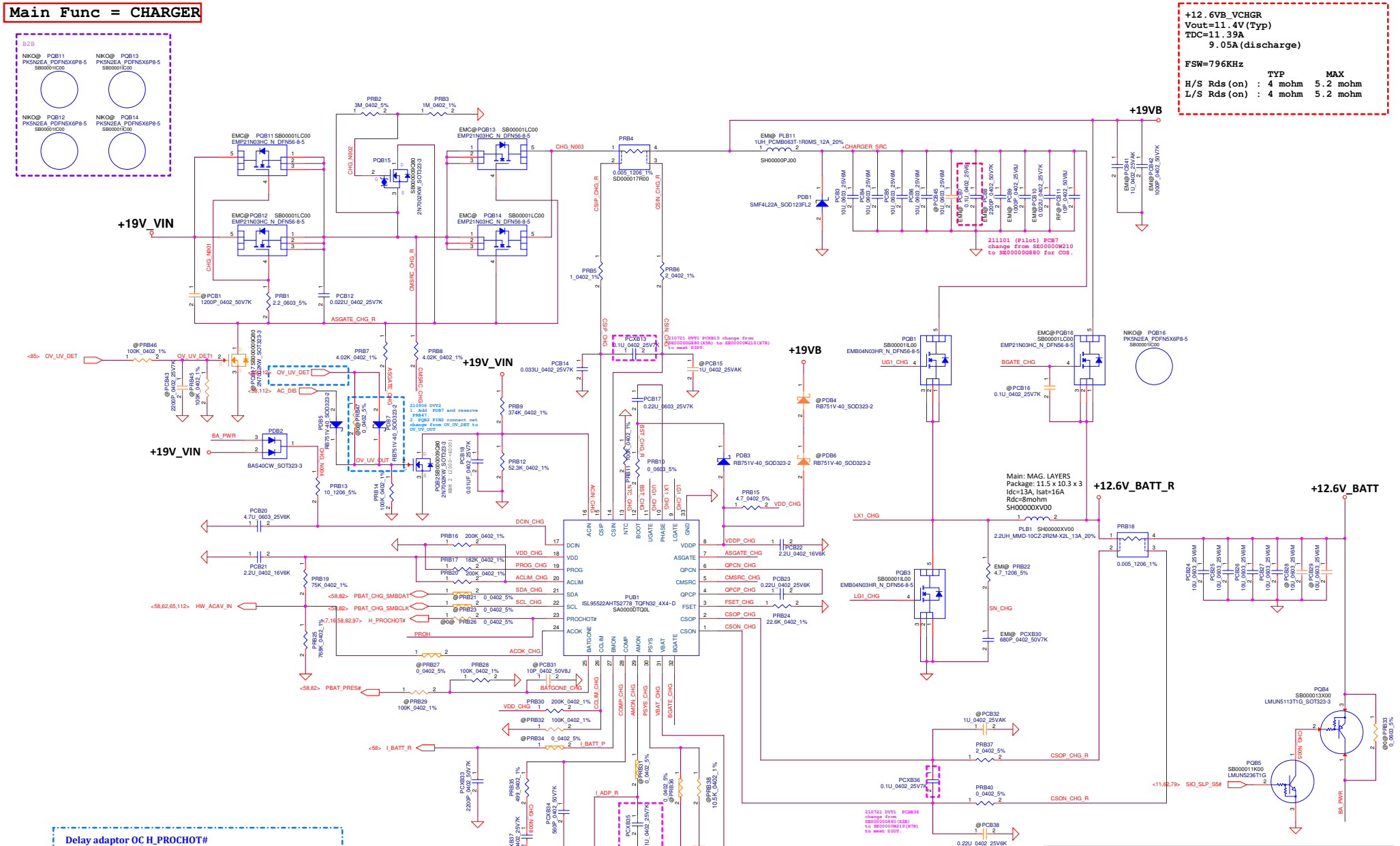
Compal Electronics, Inc.		
Title		
Size	Document Number: LA-L651P	Rev: 0.1
Date: Monday, November 22, 2021	Sheet 84 of 120	

Main Func = CHARGER

+12.6VB_VCHGR
Vout=11.4V(Typ)
TDC=11.39A
9.05A(discharge)

FSW=796KHz

	TYP	MAX
H/S Rds(on)	4 mohm	5.2 mohm
L/S Rds(on)	4 mohm	5.2 mohm



	CPN	Value	Effective capacitance	Renesas recommend
DCIN	SE000013880	4.7uF_0603_25V	0.4uF	0.4uF
VDD	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
VDDP	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
CBOOT	SE000005Z80	0.22U_0603_25V7K	0.15uF	0.15uF

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: PWR_CHARGER

Size | Document Number: LA-L651P | Rev: 0.1

Date: Monday, November 22, 2021 | Sheet 85 of 120

Reserve

Main Func = 3.3VALWP / 5VALWP

3.3VALWP
Vout=3.4V
TDC 8.05A
Peak Current 11.5A
OCP current 14.95A
OVP=3.824V~3.994V(112.5%~117.5%)
UVP=1.869V~2.209V(55%~65%)
FSW=355kHz

MOS (VGS = 4.5V)

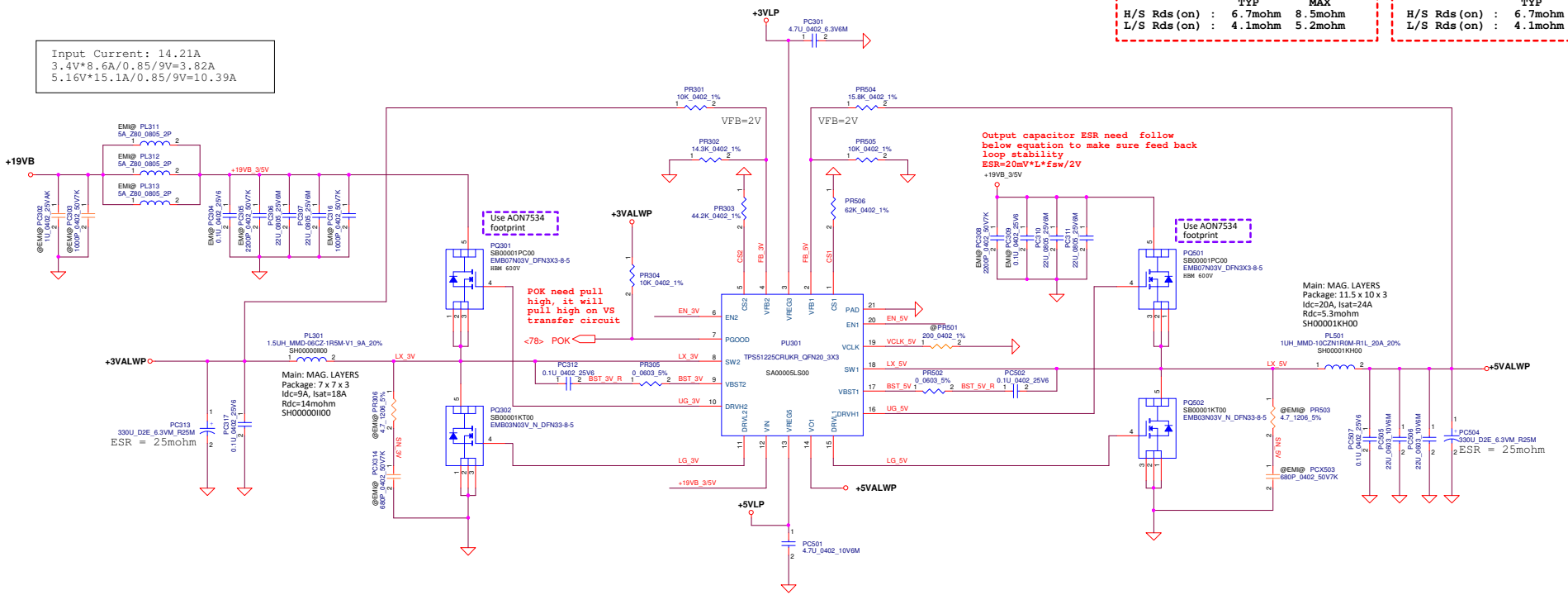
	TYP	MAX
H/S Rds(on) :	6.7mohm	8.5mohm
L/S Rds(on) :	4.1mohm	5.2mohm

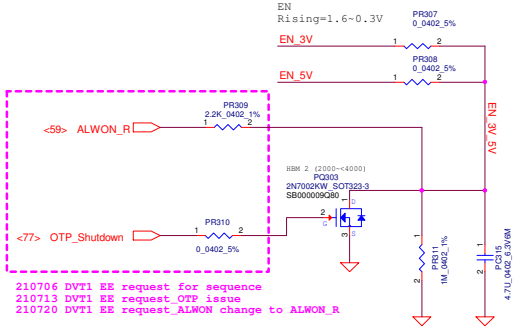
5VALWP
Vout= 5.16V
TDC =13.61A
Peak Current 17A
OCP current 22.1A
OVP=5.805V~6.063V(112.5%~117.5%)
UVP=2.838V~3.354V(55%~65%)
FSW=300kHz

MOS (VGS = 4.5V)

	TYP	MAX
H/S Rds(on) :	6.7mohm	8.5mohm
L/S Rds(on) :	4.1mohm	5.2mohm

Input Current: 14.21A
3.4V*8.6A/0.85/9V=3.82A
5.16V*15.1A/0.85/9V=10.39A





	ALWON	+5VALWP	+3VALWP
S5	H	on	on
S3	H	on	on
S0	H	on	on

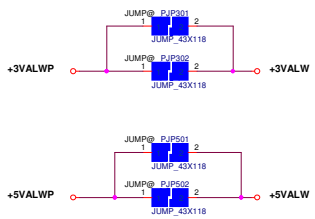
Note: S3 - sleep ; S5 - power off

T_CRIT#	+5VALWP	+3VALWP
L	off	off

Note: T_CRIT# for thermal protection

THERM_OVERT#_R	+5VALWP	+3VALWP
L	off	off

Note: THERM_OVERT#_R for thermal protection



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/12/31

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Compal Electronics, Inc.

Title: PWR +3.3VALWP/+5VALWP

Size | Document Number | Rev 0.1

LA-K453P

Date: Monday, November 22, 2021 | Sheet 87 of 120

Reserve

Main Func = +1.1VP

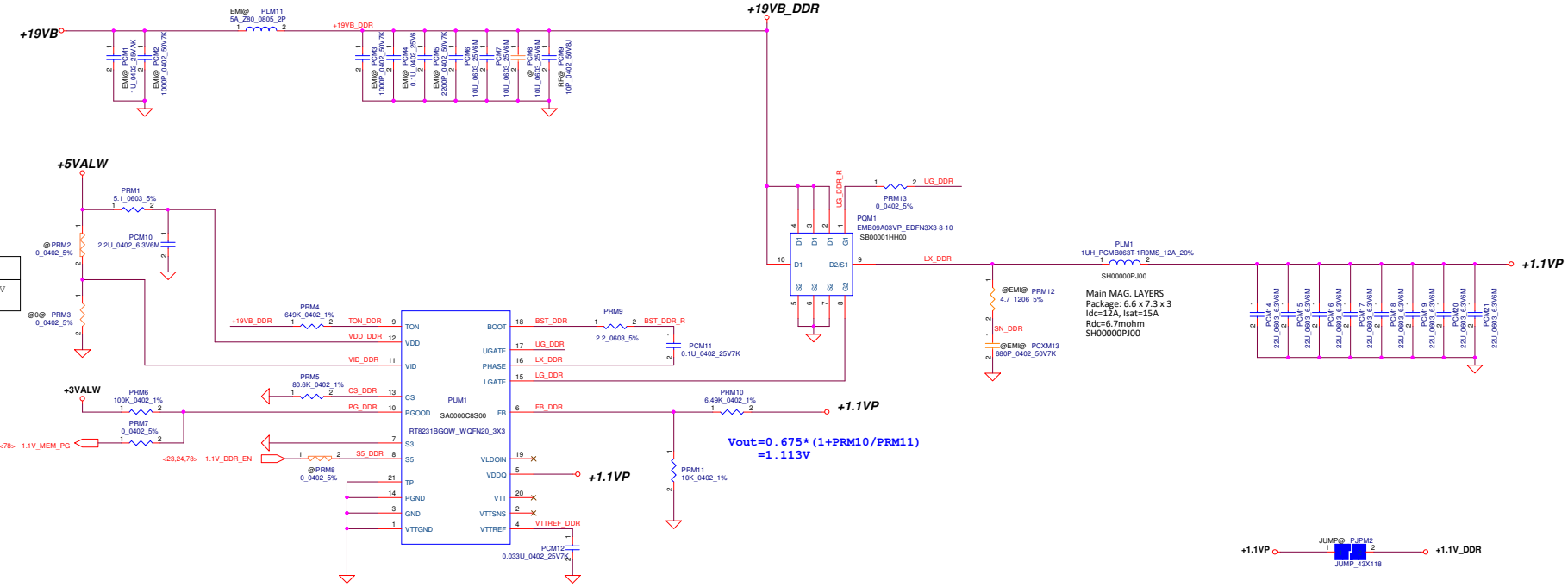
Input Current: 0.265

1.113V*1.82A/0.85/9V=0.265A

```
+1.1VP
Vout= 1.113V
TDC 1.82A
Peak Current 2.6A
OCP current 3.12A
OVP=1.22V~1.34V(110%~120%)
UVP=0.4V~0.5V
FSW= 400K Hz

MOS (VGS = 4.5V )
                    TYP       MAX
H/S Rds(on) :   11 mohm   13 mohm
L/S Rds(on) :   11 mohm   13 mohm
```

VID	Vref
High	0.675V
Low	0.75V



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: PWR +1.1VP DDR

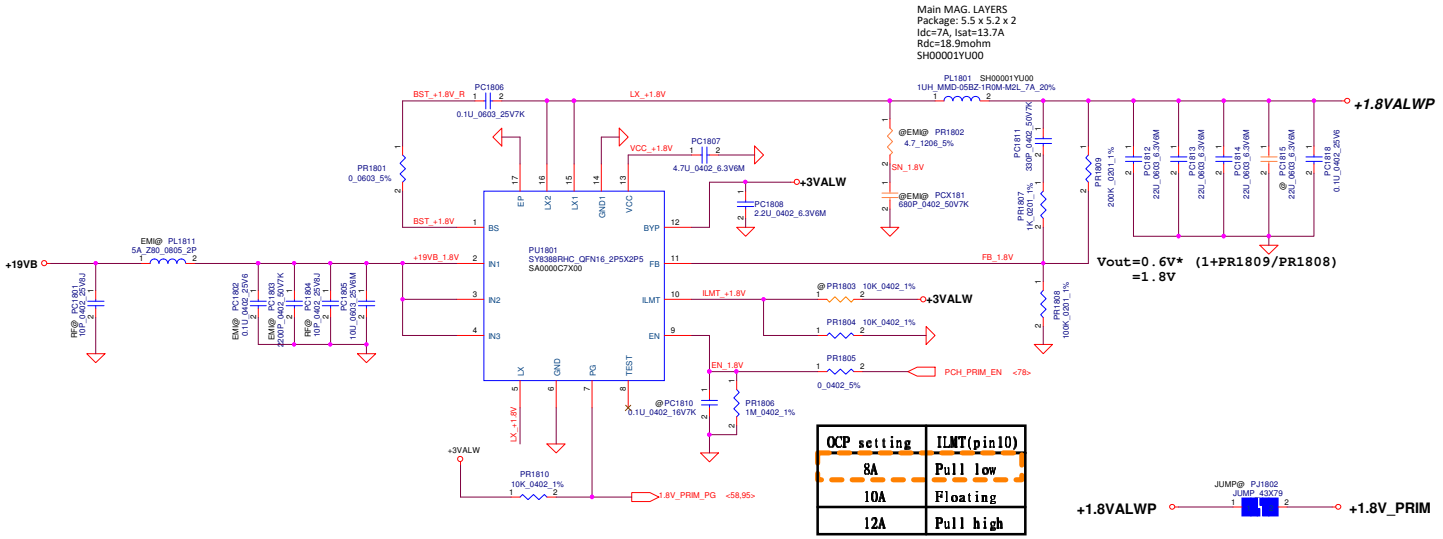
Size | Document Number: LA-L651P | Rev: 0.1

Date: Monday, November 22, 2021 | Sheet 89 of 120

Main Func = 1.8VALWP

Input Current: 0.73A
1.8V*3.1A/0.85/9V=0.73A

+1.8VALWP
Vout = 1.8V
TDC = 3.1A
Peak Current = 4.45 A
OVP=2.106V~2.214V(117%~123%)
Current limit = 8A
UVP=0.99V~1.17V(55%~65%)
FSW= 500K Hz



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2021/08/01

Compal Electronics, Inc.

Title: PWR +1.8VALWP

Size | Document Number: LA-L651P | Rev: 0.1

Date: Monday, November 22, 2021 | Sheet 90 of 120

Reserve

Reserve

Reserve

Reserve

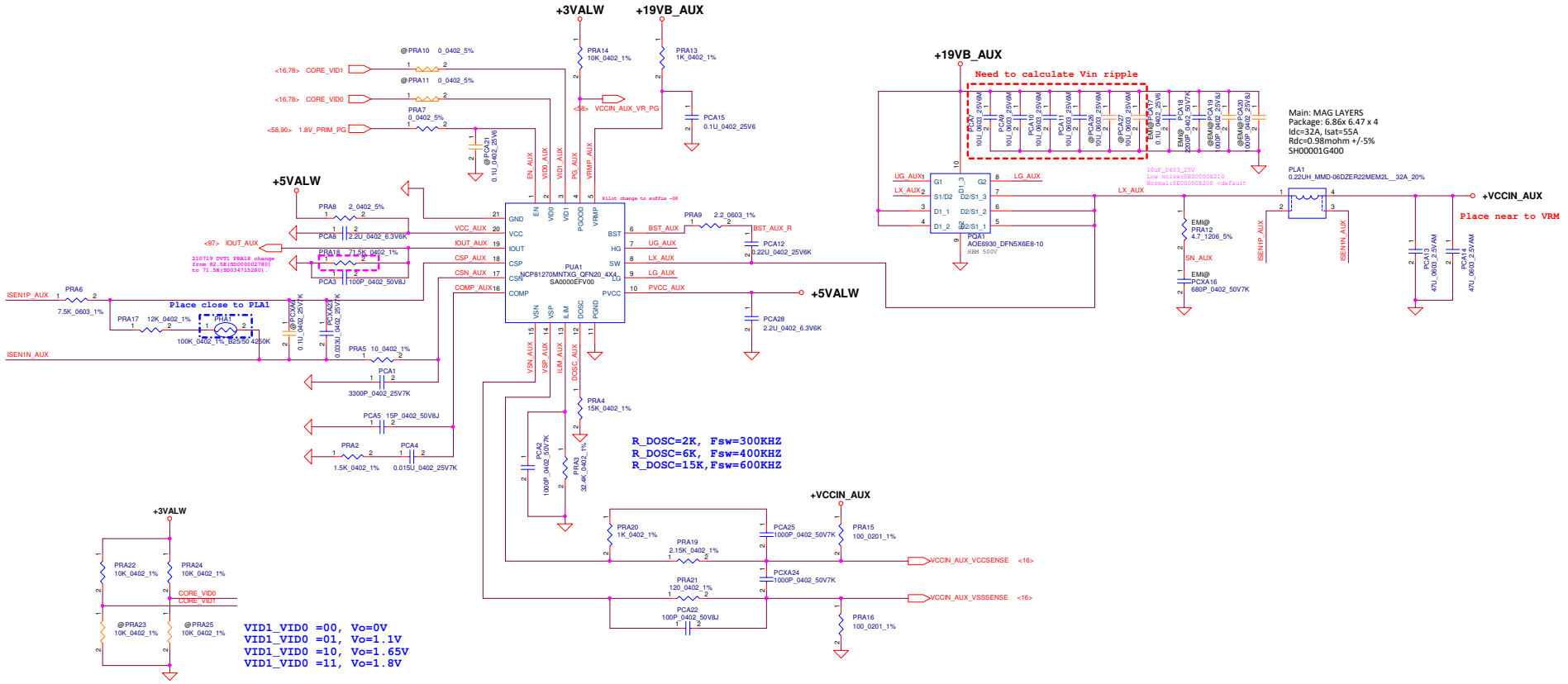
Compal Electronics, Inc.		
Title		
Size	Document Number: LA-L651P	Rev: 0.1
Date: Monday, November 22, 2021	Sheet 94 of 120	

Main Func = +VCCIN_AUX

+VCCIN_AUX
Vout 1.8V
IPL2(TDC) = 18A
Peak Current = 33A(ICCmax)
OCP 42.9 A
FSW= 600KHz

MOS (VGS = 4.5V)

	TYP	MAX
Rds(on) :	5.2 mohm	7 mohm



Security Classification	Compal Secret Data		
Issued Date	2021/01/07	Deciphered Date	2021/01/07

Compal Electronics, Inc.

Title

Size | Document Number | Rev
LA-L651P | 0.1

Date: Monday, November 22, 2021 | Sheet 95 of 120

Main Func = +VCCIN_AUX DECOUPLING

Follow Intel ADL-P PDG Rev1.0
+VCCIN_AUX Output CAP :

CPU Primary Side:
330uF *1pcs
47uF_0603 *4 pcs

CPU Secondary side:
10uF_0402 *10pcs
47uF_0603 *4pcs

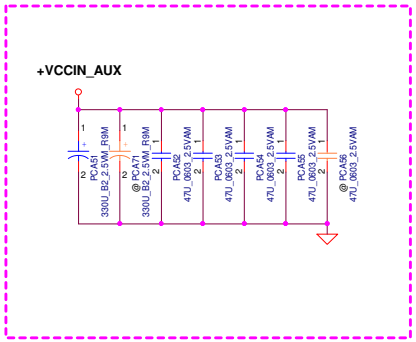
Compal
+VCCIN_AUX Output CAP :

CPU Primary Side:
330uF_B2_2.5V_R9M *1pcs
47uF_0603_2.5V_X6S *5 pcs(1pcs reserved)

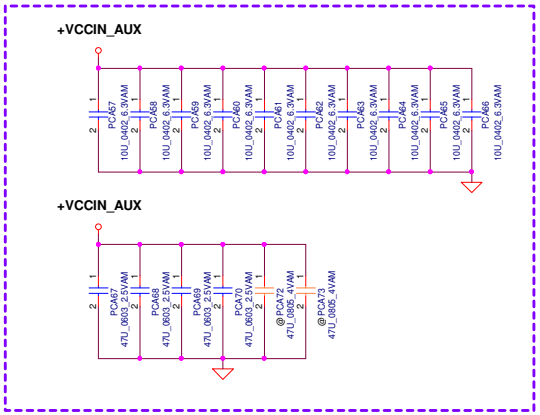
CPU Secondary side:
10uF_0402_6.3V_X6S *10pcs
47uF_0603_2.5V_X6S *4pcs

For FIVR solution
CPU Primary Side:
47uF_0603 *1
Placeholder 0402 *1
on EE side

CPU Primary Side



CPU Secondary side



Compal Electronics, Inc.			
Title			
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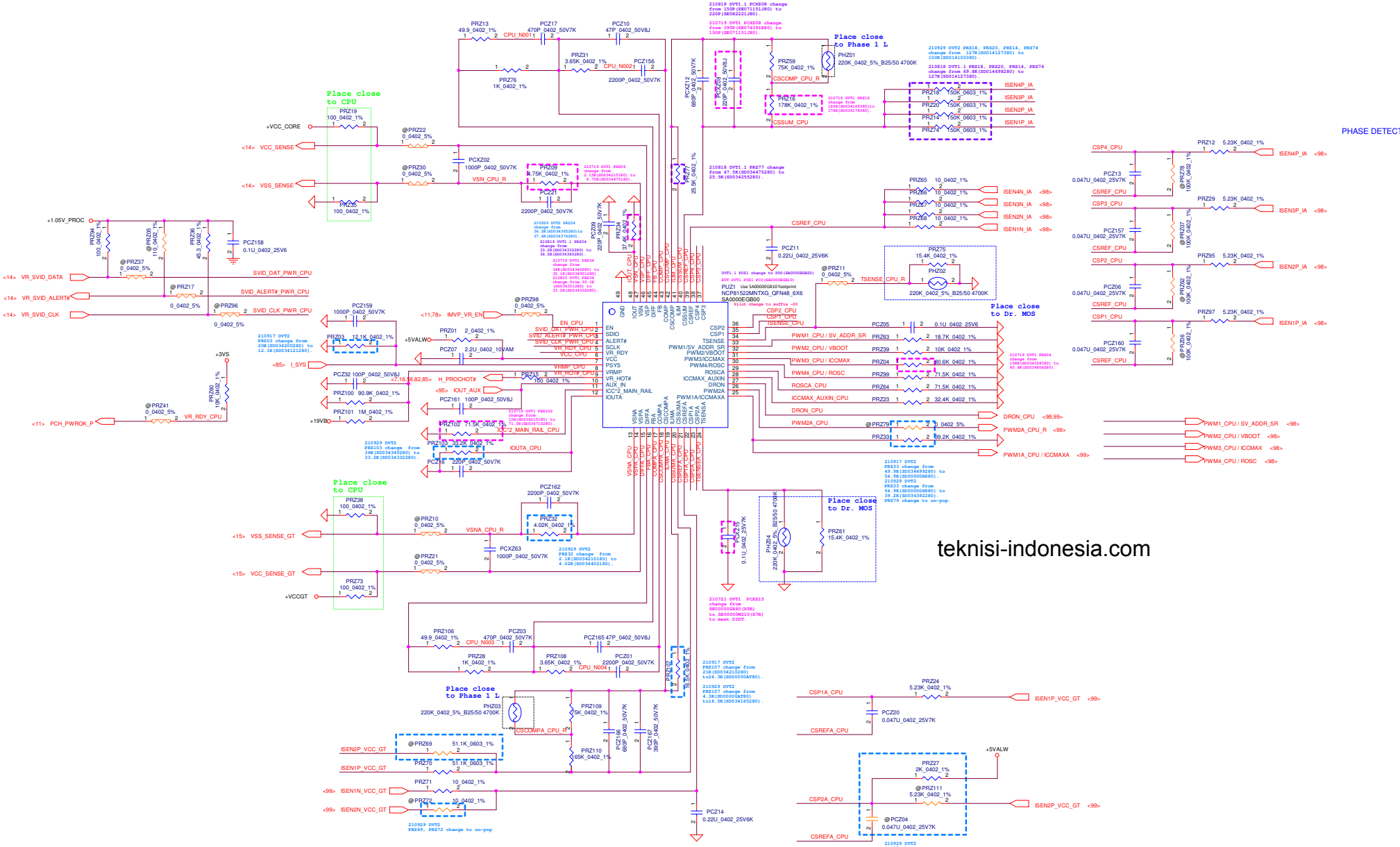
Main Func = CPU (IA/GT)



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Issued Date	2020/03/05	Deciphered Date	2017/01/06
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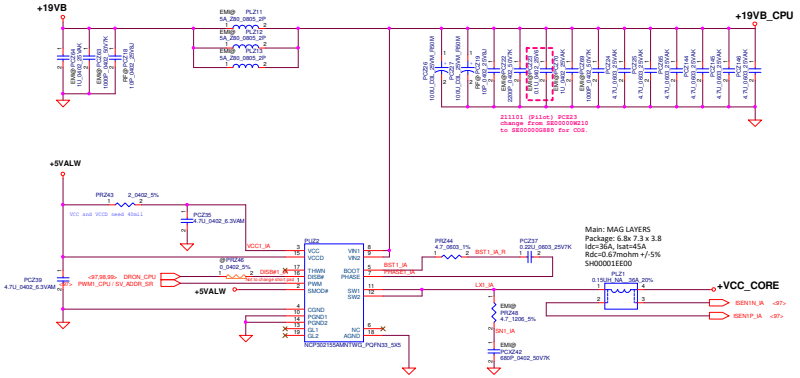
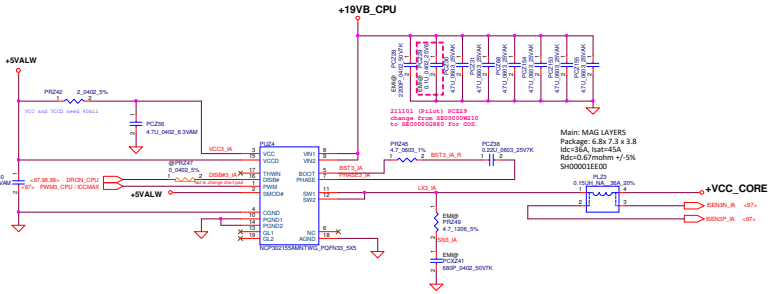
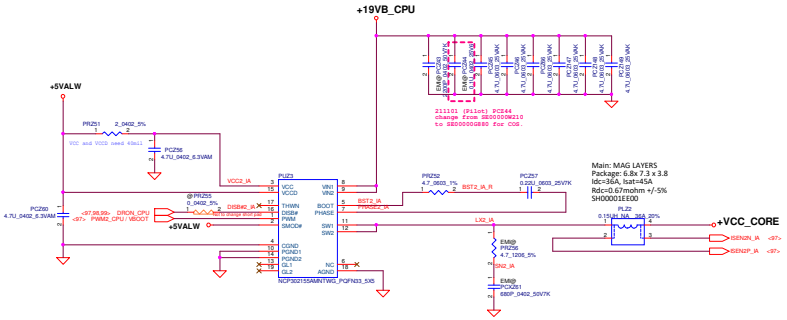
			Size: Document Number: LA-L651P Rev: 1
			Date: Monday, November 22, 2021 Sheet 97 of 120

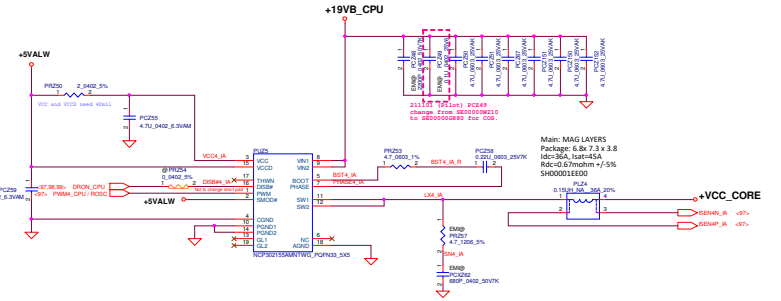
Main Func = +VCCCORE

+VCCCORE
IPL2 = 93A
Peak Current = 160A(ICCmax)
DC Load line: 2.3mohm
AC Load line: 2.3mohm
OCP = 208A
FSW= 540K Hz









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Issued Date	2020/03/05	Deciphered Date 2021/01/06	Title PWR +VCCCORE SW

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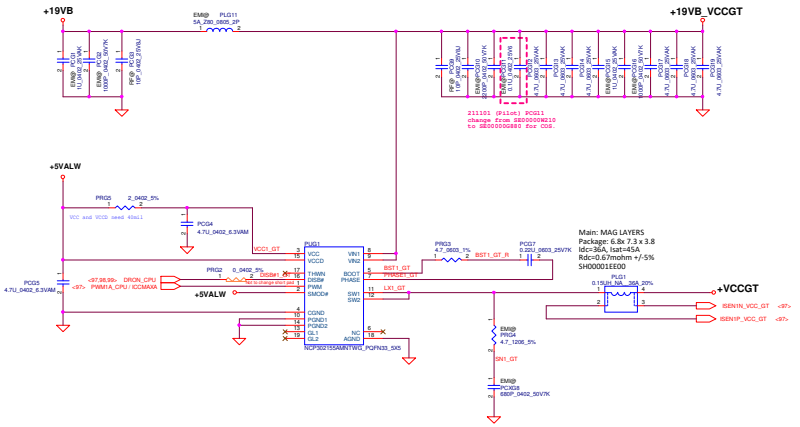
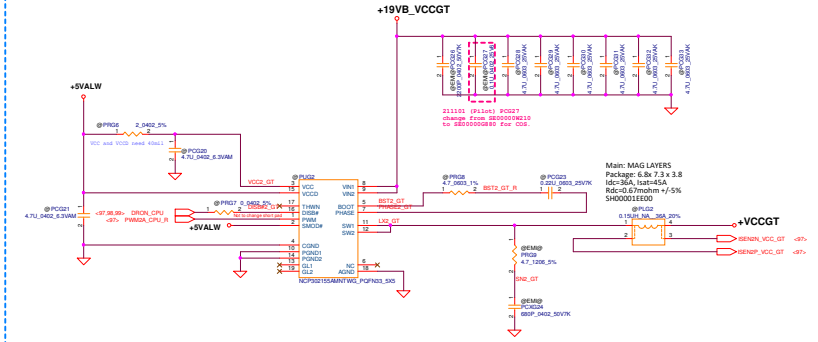
Main Func = +VCCGT

+VCCGT
IPL2 = 30A
Peak Current = 50A(ICCmax)
DC Load line: 3.2mohm
AC Load line: 3.2mohm
OCP = 65A
FSW= 540K Hz



210928 DVT2
GT DTC to 1PH



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Issued Date	2020/03/05	Deciphered Date 2017/01/06	Title PWR +VCCGT
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Reserve

Main Func = +VCCIN DECOUPLING

Intel ADL-P PDG Rev1.0
+VCC_CORE Output CAP :

CPU Primary Side:
330uF_D2 *3pcs
47uF_0603 *8 pcs

CPU Secondary side:
2.2uF_0402 *8pcs

Compal
+VCC_CORE Output CAP :

CPU Primary Side:
330uF_D2_2.5VM_R6M *1pcs
220uF_D7_2.5V_R6M *3pcs
47uF_0603_2.5V_X6S *10pcs
(2pcs reserved)
47U_0805_4V_X6S *6pcs
(6pcs reserved)

CPU Secondary side:
2.2uF_0402_6.3V_X6S *8pcs

Intel ADL-P PDG Rev1.0
+VCC_GT Output CAP :

CPU Primary Side:
330uF_D2 *2pcs
47uF_0603 *8 pcs
(1pcs reserved)
22uF_0402 *2 pcs

CPU Secondary side:
22uF_0402 *6pcs
10uF_0402 *4pcs
(2pcs reserved)

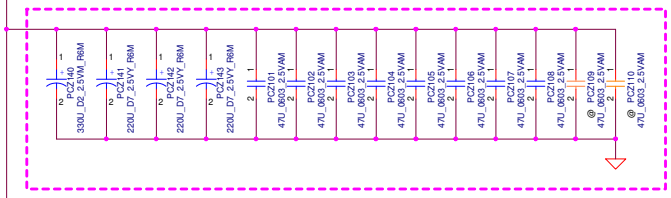
Compal
+VCCGT Output CAP :

CPU primary side:
220uF_D7_2.5V_R6M *3pcs
47uF_0603_2.5V_X6S *8pcs
(1pcs reserved)
22uF_0603_6.3V_X6S *2pcs
47U_0805_4V_X6S *2pcs
(2pcs reserved)

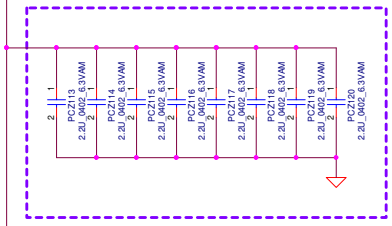
CPU Secondary side:
22uF_0603_6.3V_X6S *6pcs
10uF_0402_6.3V_X6S *4pcs
(2pcs reserved)

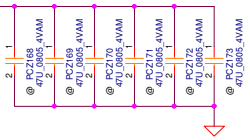
+VCC_CORE

CPU Primary Side



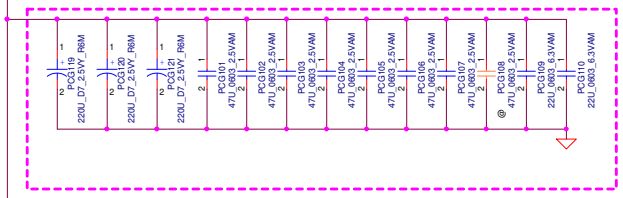
CPU Secondary side



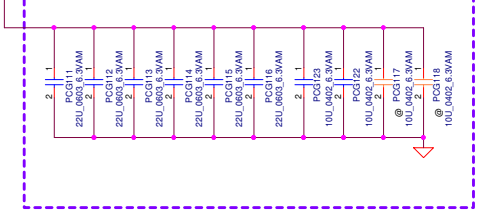


+VCCGT

CPU Primary Side



CPU Secondary side



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: PWR_+VCORE DECOUPLING

Size: | Document Number: LA-K452P | Rev: 0.1

Date: Monday, November 23, 2020 | Sheet 101 of 120

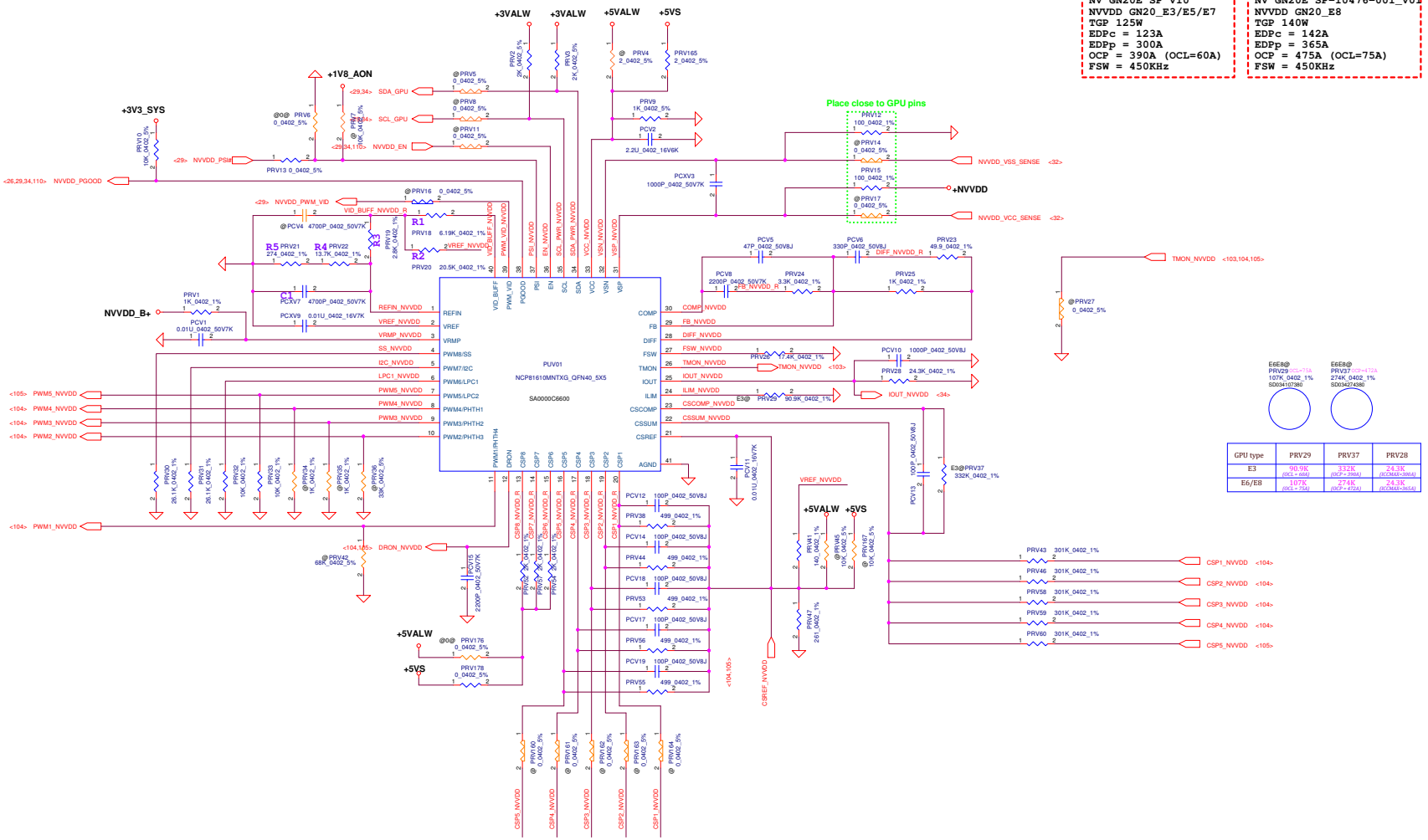
Reserve

Main Func = VGA CORE

Config	
Vmin	0.3
Vmax	1.3
Vboot	0.75
R1	6.19K
R2	20.5K
R3	2.8K
R4	13.7K
R5	0.274K
C	4.7n

NV GN20E SP V10
NVVDD GN20_E3/E5/E7
TGP 125W
EDPc = 123A
EDPp = 300A
OCP = 390A (OCL=60A)
FSW = 450KHz

NV GN20E SP-10476-001_V01
NVVDD GN20_E8
TGP 140W
EDPc = 142A
EDPp = 365A
OCP = 475A (OCL=75A)
FSW = 450KHz



GPU type	PRV29	PRV37	PRV28
E3	90.9K (OCL = 60A)	332K (OCP = 390A)	24.3K (ICCMAX=300A)
E6/E8	107K (OCL = 75A)	274K (OCP = 472A)	24.3K (ICCMAX=365A)

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2020/04/19

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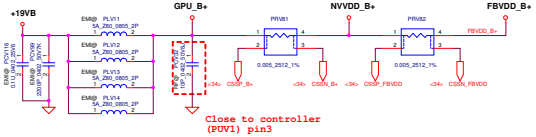
Compal Electronics, Inc.

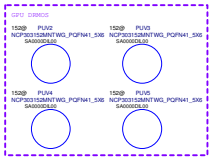
Title: PWR_GPU_CORE(NCP81610)

Size: | Document Number: LA-L651P | Rev: 0.1

Date: Monday, November 22, 2021 | Sheet 103 of 120

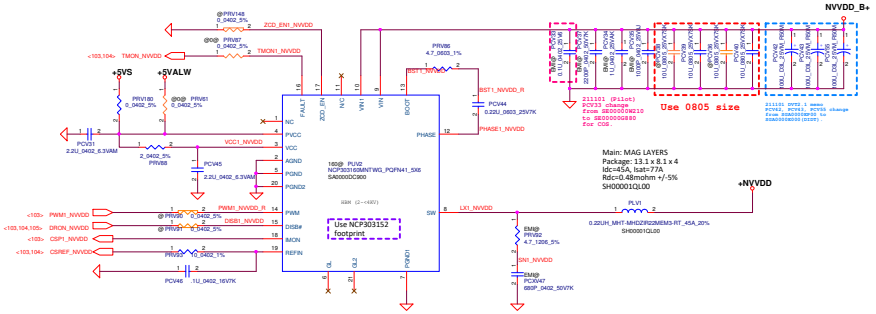
Main Func = GPU_CORE SW(1-4PH)

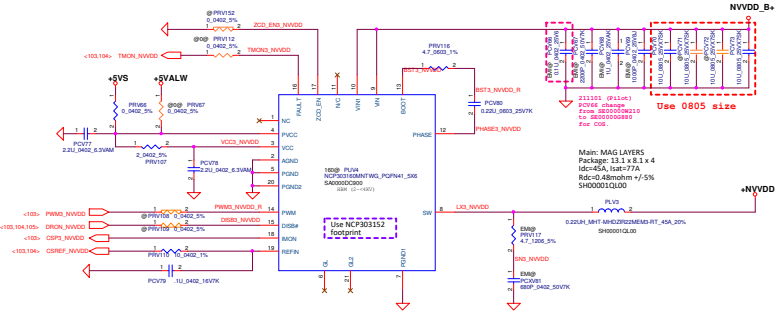


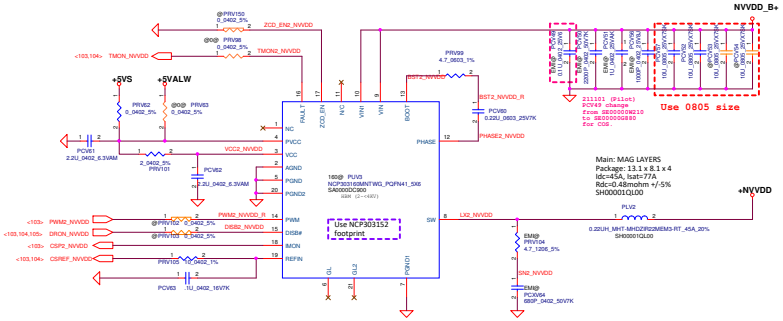


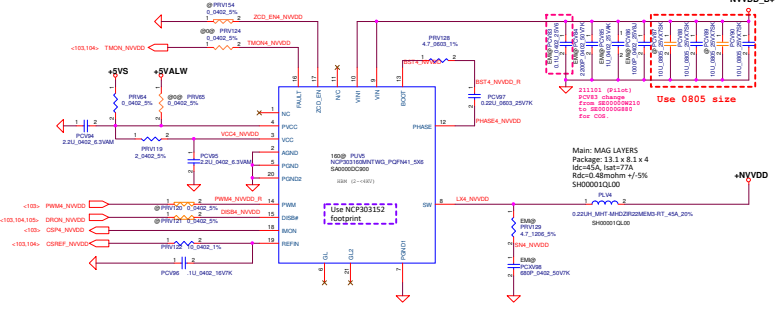
NV GN20E SP V10
NVVDD GN20_E3/E5/E7
TGP 125W
EDPc = 123A
EDPp = 300A
OCP = 390A (OCL=60A)
FSW = 450KHz

NV GN20E SP-10476-001_V01
NVVDD GN20_E8
TGP 140W
EDPc = 142A
EDPp = 365A
OCP = 475A (OCL=75A)
FSW = 450KHz









Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2020/04/19	Title: PWR_GPU_CORE SW(NCP303152)
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			Date: Monday, November 29, 2021; Sheet 104 of 120

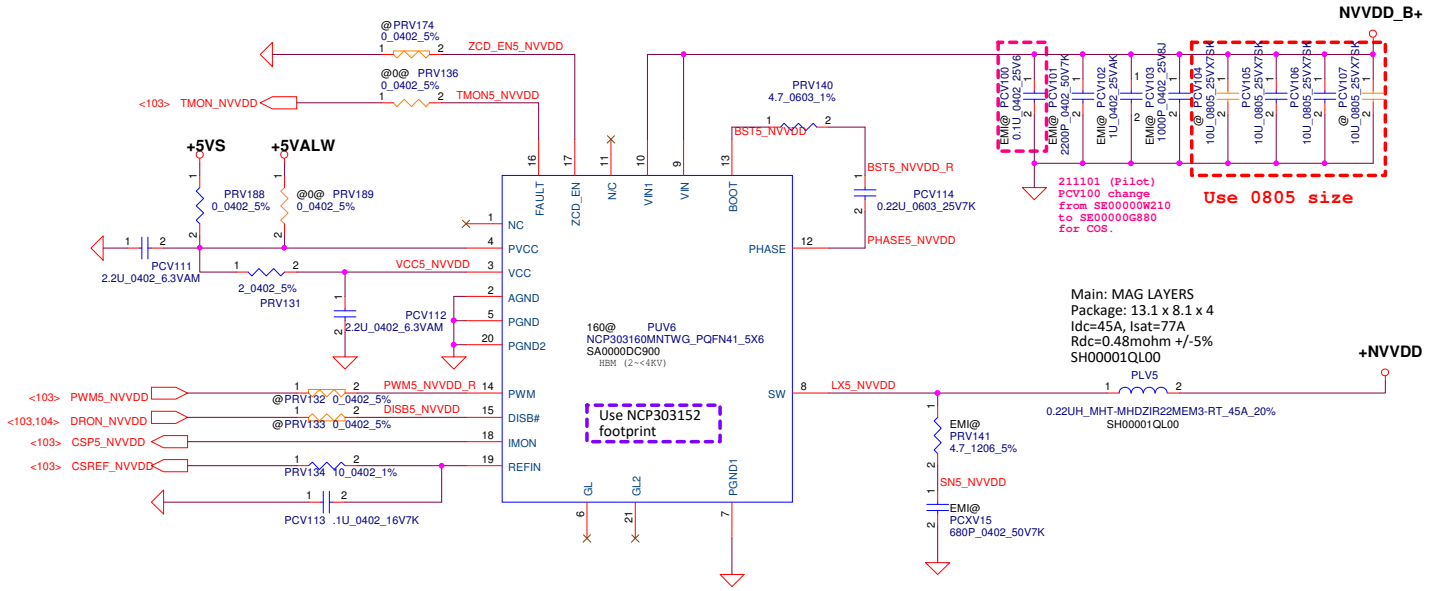
Main Func = GPU_CORE SW(5PH)

GPU DRMOS

152@ PUV6
NCP303152MNTWG_PQFN41_5X6
SA0000DIL00

NV GN20E SP V10
NVVDD GN20_E3/E5/E7
TGP 125W
EDPc = 123A
EDPp = 300A
OCP = 390A (OCL=60A)
FSW = 450KHz

NV GN20E SP-10476-001_V01
NVVDD GN20_E8
TGP 140W
EDPc = 142A
EDPp = 365A
OCP = 475A (OCL=75A)
FSW = 450KHz



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: PWR_GPU_CORE SW(5PH)

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Reserve

Main Func = VGA CORE DECOUPLING

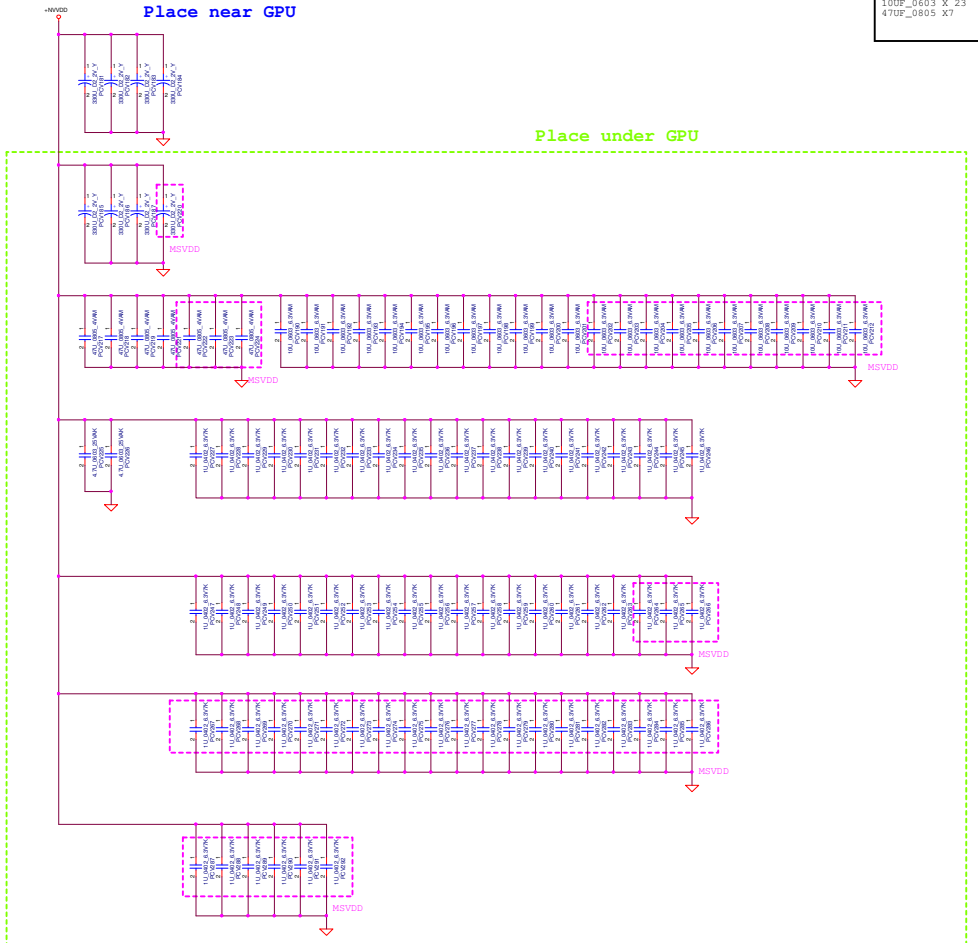
```
+NVVDD / +MSVDD
330UF X 8
1UF_0402 X 66
4.7UF_0603 X 2
10UF_D603 X 23
47UF_0805 X7
```

```
DG-09845-001_v07
+NVVDD
330UF X 3
1UF_0402 X 37
4.7UF_0603 X 2
10UF_0603 X 12
47UF_0805 X 4

+MSVDD
330UF X 1
1UF_0402 X 29
10UF_0603 X 11
47UF_0805 X 3
```

Place near GPU

Place under GPU



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Issued Date	2020/03/05	Deciphered Date 2020/04/19	Title PWR_GPU_CORE DECOUPLING
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			Date Monday, November 29, 2021 Sheet 107 of 120

Main Func =+FBVDDQ

Vout = 1.25V ~ 1.35V
EDPc 47 A
Peak Current 61 A
OCP=90.74A
OVP 2.09 V (155%)
FSW=300KHz

GPU type	FBVDD VOUT	PRW26	PRW27
E3/E6/E8	1.35V-1.25V	21K	82.5K

Vout=2*[(PRW26//PRW27)/[PRW19+(PRW26//PRW27)]

P0:high P8:low

Main: MAG LAYERS
Package: 6.95 x 6.6 x 3
Idc=30A, Isat=40A
Rdc=1.17mohm +/-5%
SH000025000

Main: MAG LAYERS
Package: 6.95 x 6.6 x 3
Idc=30A, Isat=40A
Rdc=1.17mohm +/-5%
SH000025000

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2020/04/19

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Compal Electronics, Inc.

Title: PWR_GPU_VRAM

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Date: Monday, November 22, 2021 | Sheet 108 of 120

Reserve

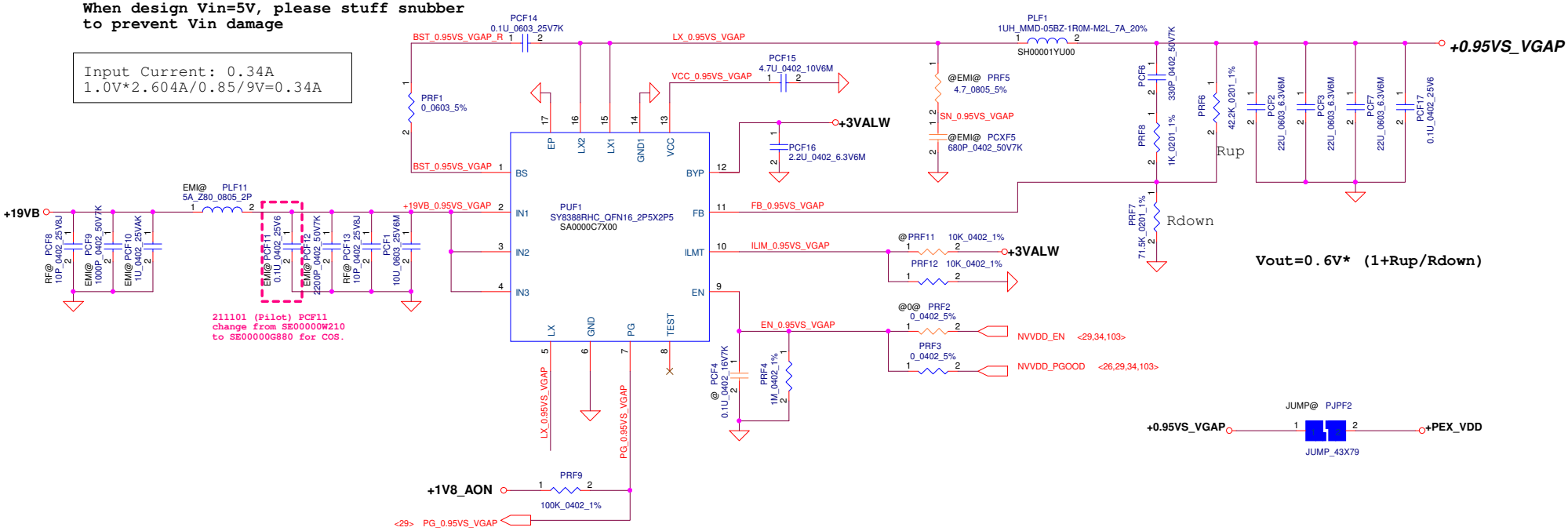
Main Func =+0.95VS_VGAP

+0.95VS_VGAP
Vout = 0.954V
TDC = 2.7A
Peak Current = 4.8A
Current limit = 8A
FSW= 500K Hz

M1_CYNTEC_PCMB053T-1R0MS
M3_MAG LAYERS_MMD-05CZ-1R0M-M7L
M4_CHILISIN_MHCI05030C-1R0M-R8
Package: 5.49 x 5.18 x 2
Idc=7A, Isat=13.7A
Rdc=18.9mohm +/-5%
SH00001YU00

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Input Current: 0.34A
1.0V*2.604A/0.85/9V=0.34A



Vout=0.6V* (1+Rup/Rdown)

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2021/08/01

Compal Electronics, Inc.

Title: **PWR +0.95VS_VGAP**

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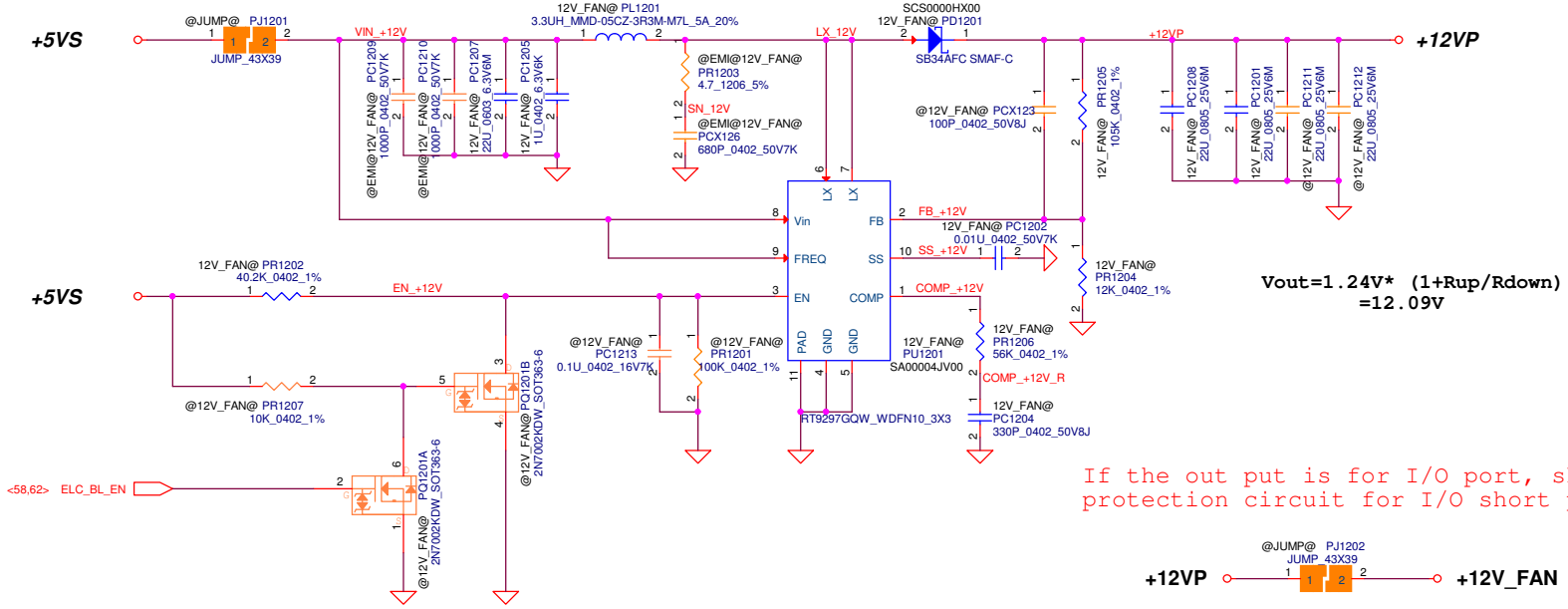
Main Func =+12VP_FAN

Add a switch circuit to turn off the +12V_VIN if need.

Input Current: 1.792A
12.09V*0.63A/0.85/5V=1.792A

+12VP
Vout = 12.09 V
TDC 0.63A
Peak Current 0.9A
Current limit 3A
FSW=1.24MHz

Main: MAG LAYERS
Package: 5.2*4.9*3
Idc=5A, Isat=7A
Rdc=32mohm +/-5%
SH00000R200



Vout=1.24V* (1+Rup/Rdown)
=12.09V

If the out put is for I/O port, should be add protection circuit for I/O short protection.

EN high: > VIN pin* 0.7
EN Low: < VIN pin* 0.3

FREQ high : Frequency = 1.2MHz
FREQ low : Frequency = 640KHz

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date	2018/12/31
Title	PWR_+12VP_FAN		
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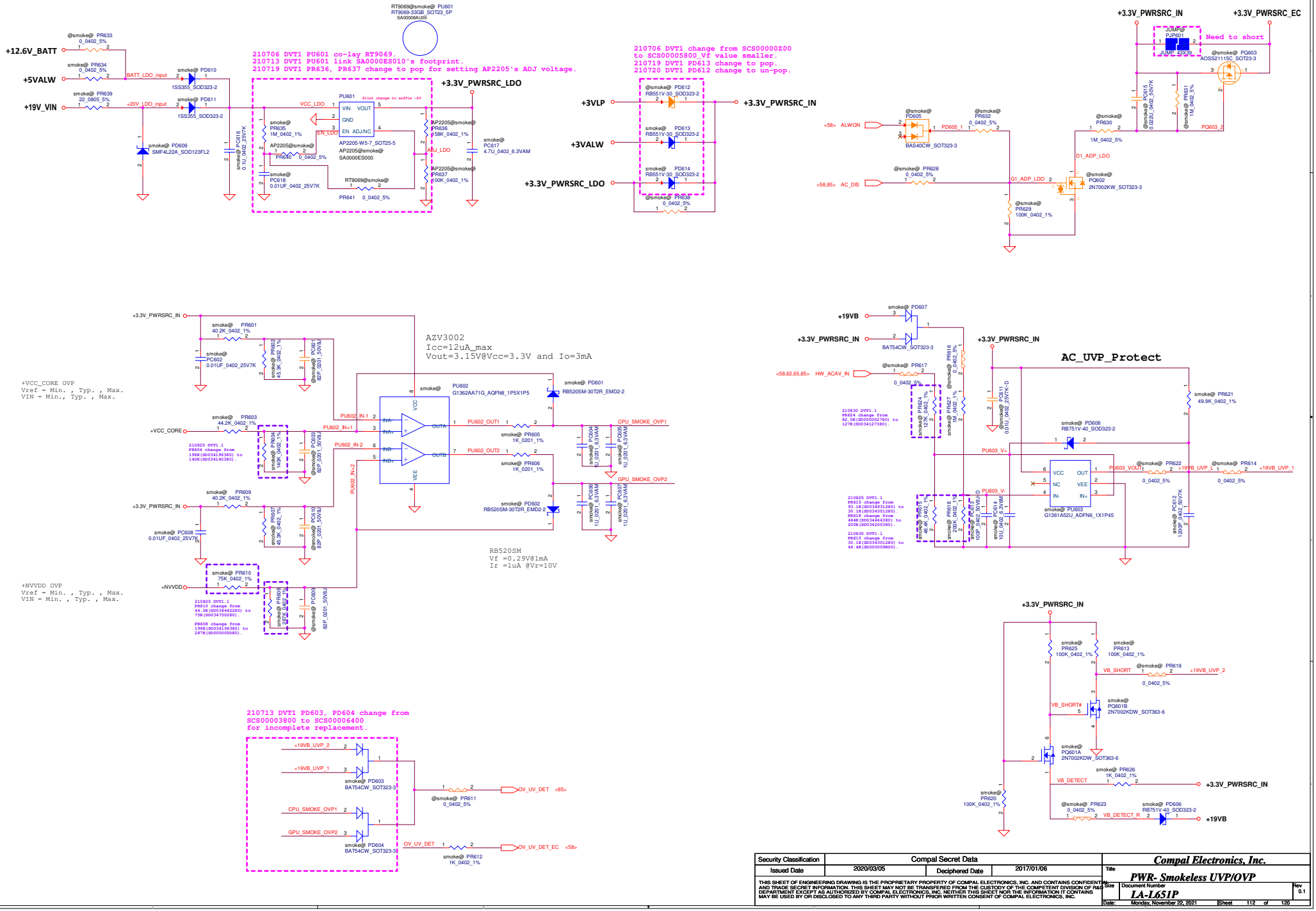
Main Func = Smokeless UVP



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.			
Title	PWR- Smokeless UVP/OVP		
Size	Document Number		Rev
	LA-L651P		0.1
Date: Monday, November 22, 2021	Sheet 112 of 120		

Reserve

Reserve

Reserve

Reserve

Reserve

Reserve

Compal Electronics, Inc.		
Title		
Size	Document Number: LA-L651P	Rev: 0.1
Date: Monday, November 22, 2021	Sheet 118 of 120	

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Compal Electronics, Inc.

Title: PWR_PIR

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Date: Monday, November 22, 2021 | Sheet 119 of 120

Version Change List (P. I. R. List)

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10							

Compal Electronics, Inc.

Title: PWR_PIR

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