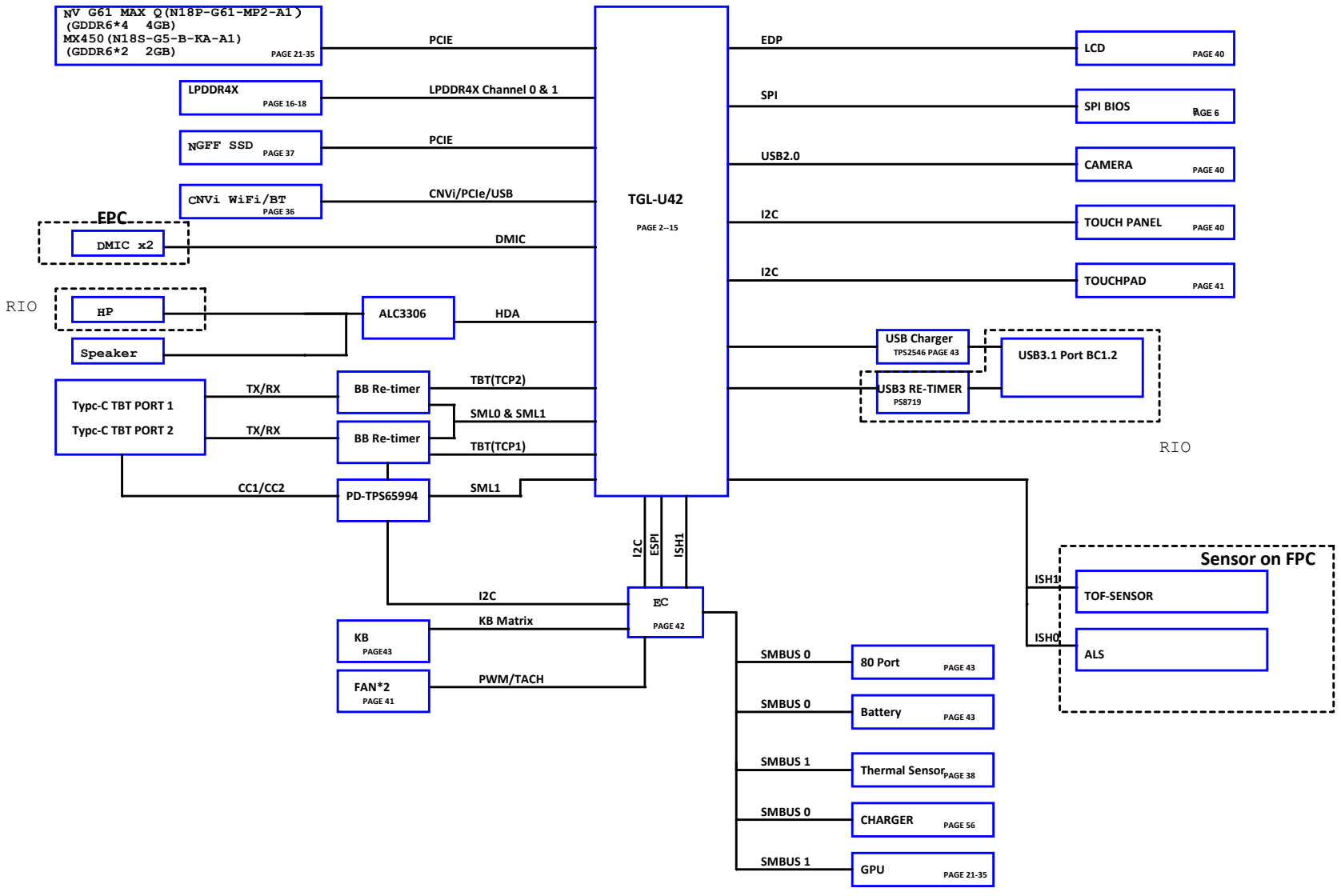
S750 TGL-U42 Schematic Block Diagram



SMBus ADDRESS:
EC_SMB1: 0x9A, 0x98 THERMAL SENSOR
I2C ADDRESS:
ISH-I2C0: 0x88 ALS
ISH I2C1: 0X52 TOF

lenovo 联想 LENOVO.CRDN

Title: T GL-U Block Diagram

Size	Document Number	Rev
C	S 750	0.5

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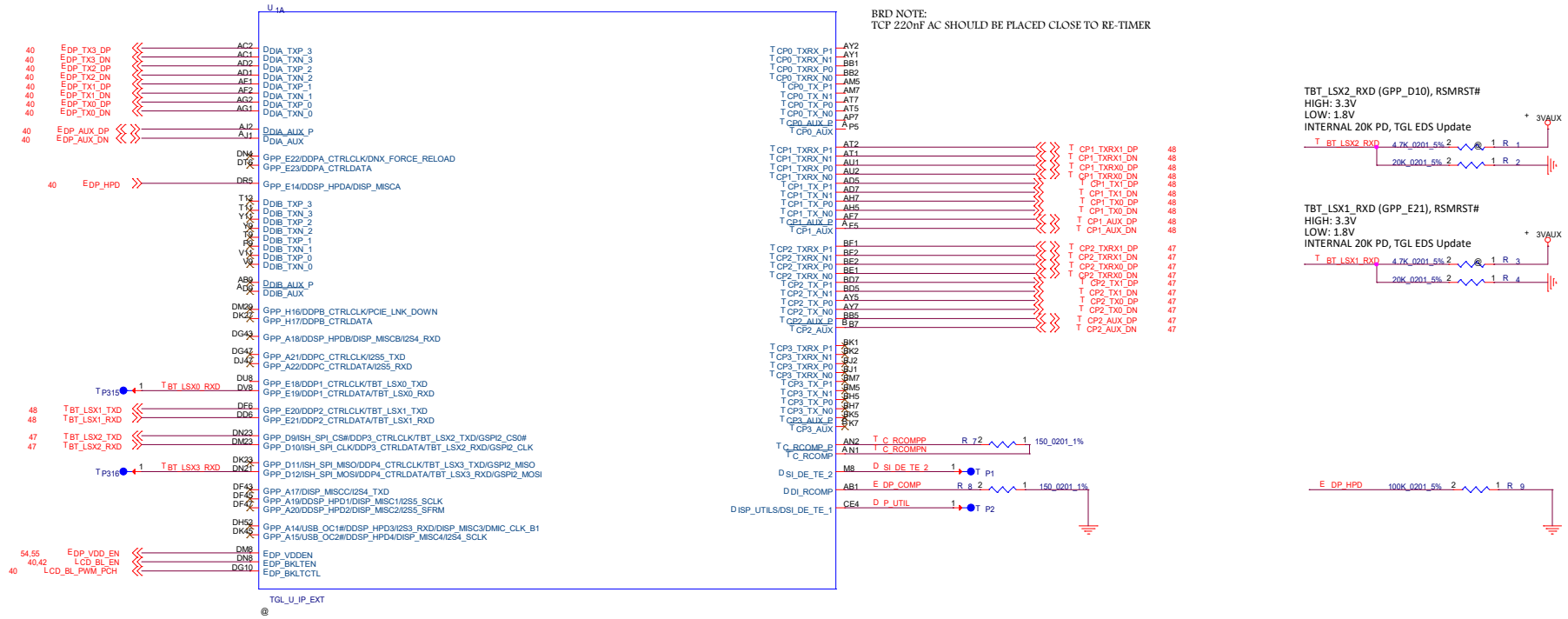

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Title	T iger Lake MCP (TBT,EDP)
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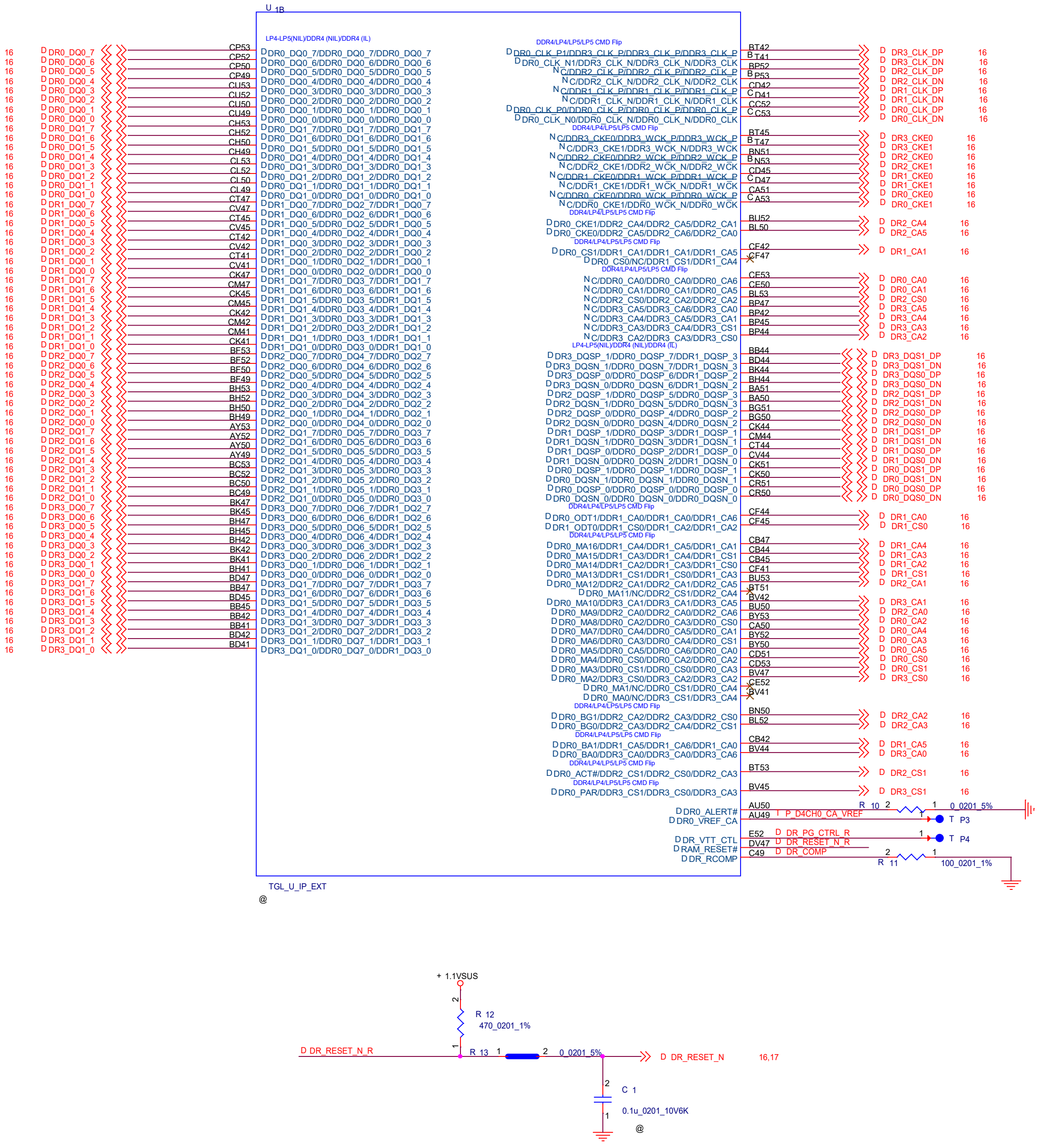
CPU LPDDR4X CHANNEL 0



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Title: Tiger Lake MCP (PROCESSOR LP4X)

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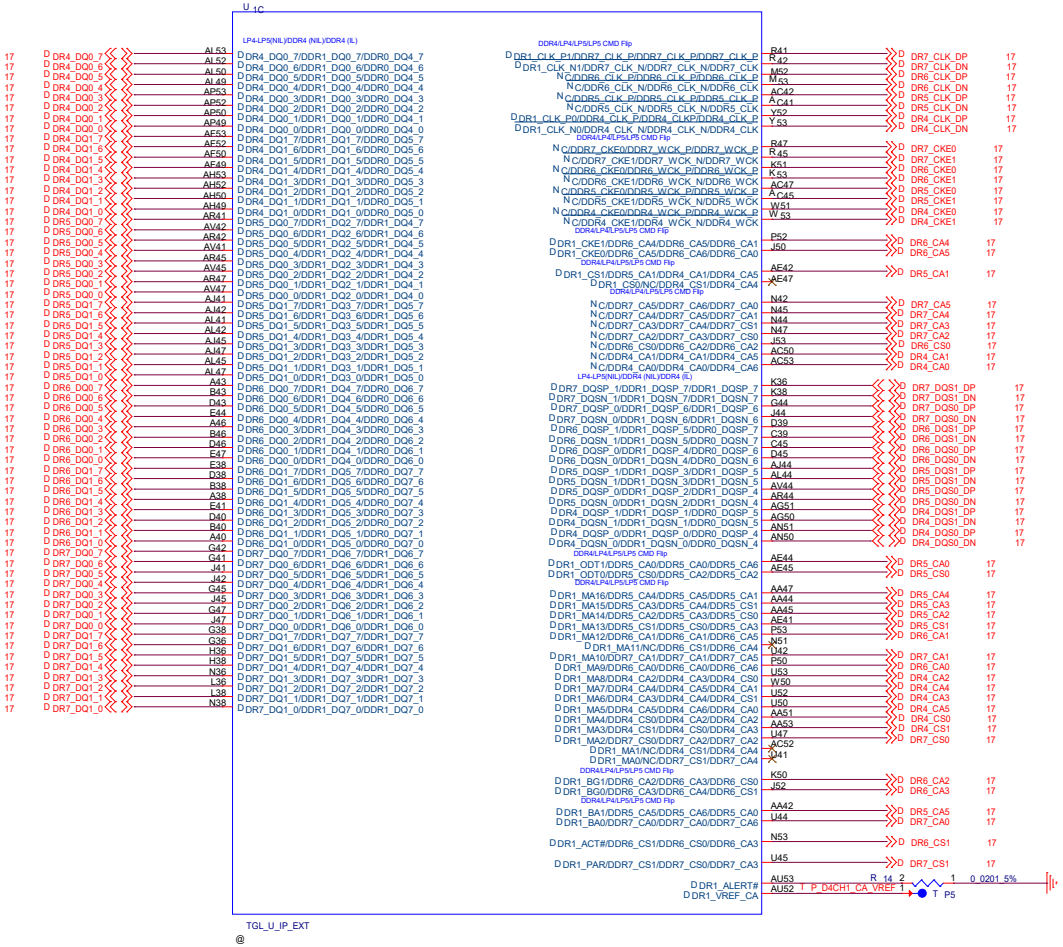
CPU LPDDR4X CHANNEL 1



lenovo联想	LENOVO.CRDN
Title	T iger Lake MCP (PROCESSOR LP4X)
Size C	Document Number S 750
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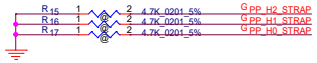
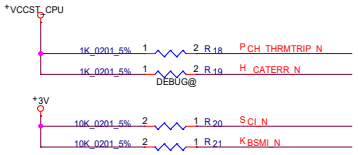
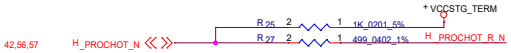
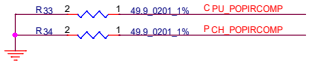
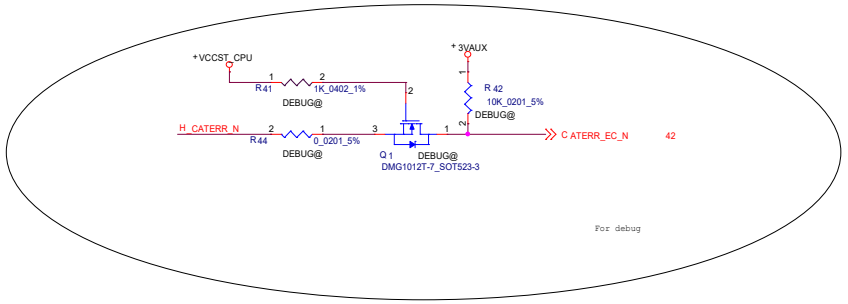


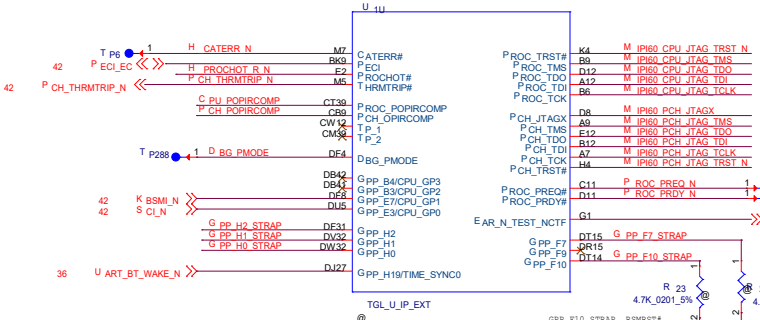
GPP_H0, GPP_H1, GPP_H2 (RSMRST#)
These signals have 20 K+- 30% internal pull-down.
0 = Master Attached Flash Sharing (MAFS) is enabled. (Default)
1 = Slave Attached Flash Sharing (SAFS) is enabled.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.





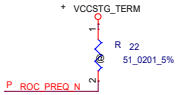


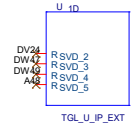




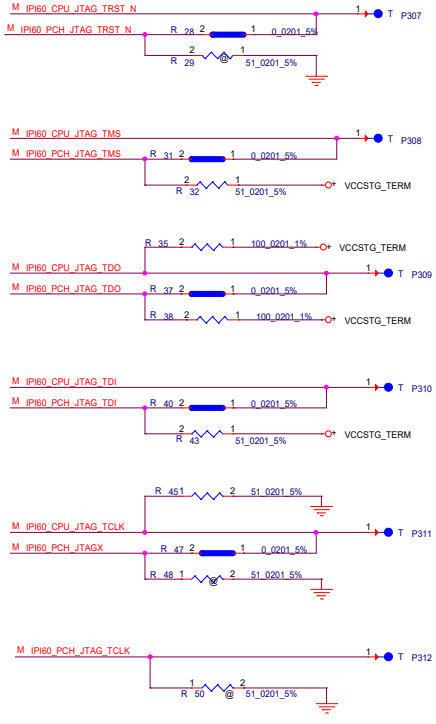
GPP_F10 STRAP, RSMRST#
This strap should sample LOW
This strap has a 20 kohm ± 30% internal pull-down.

G PP_F7 STRAP, RSMRST#
This strap should sample LOW
This strap has a 20 kohm ± 30% internal pull-down.





Place these 51ohm and 100ohm resistors close to PCH/CPU



lenovo联想	LENOVO.CRDN	
Title: T iger Lake MCP (MISC THERM CPU JTAG)		
Size: C	Document Number: S 750	Rev: 0.5
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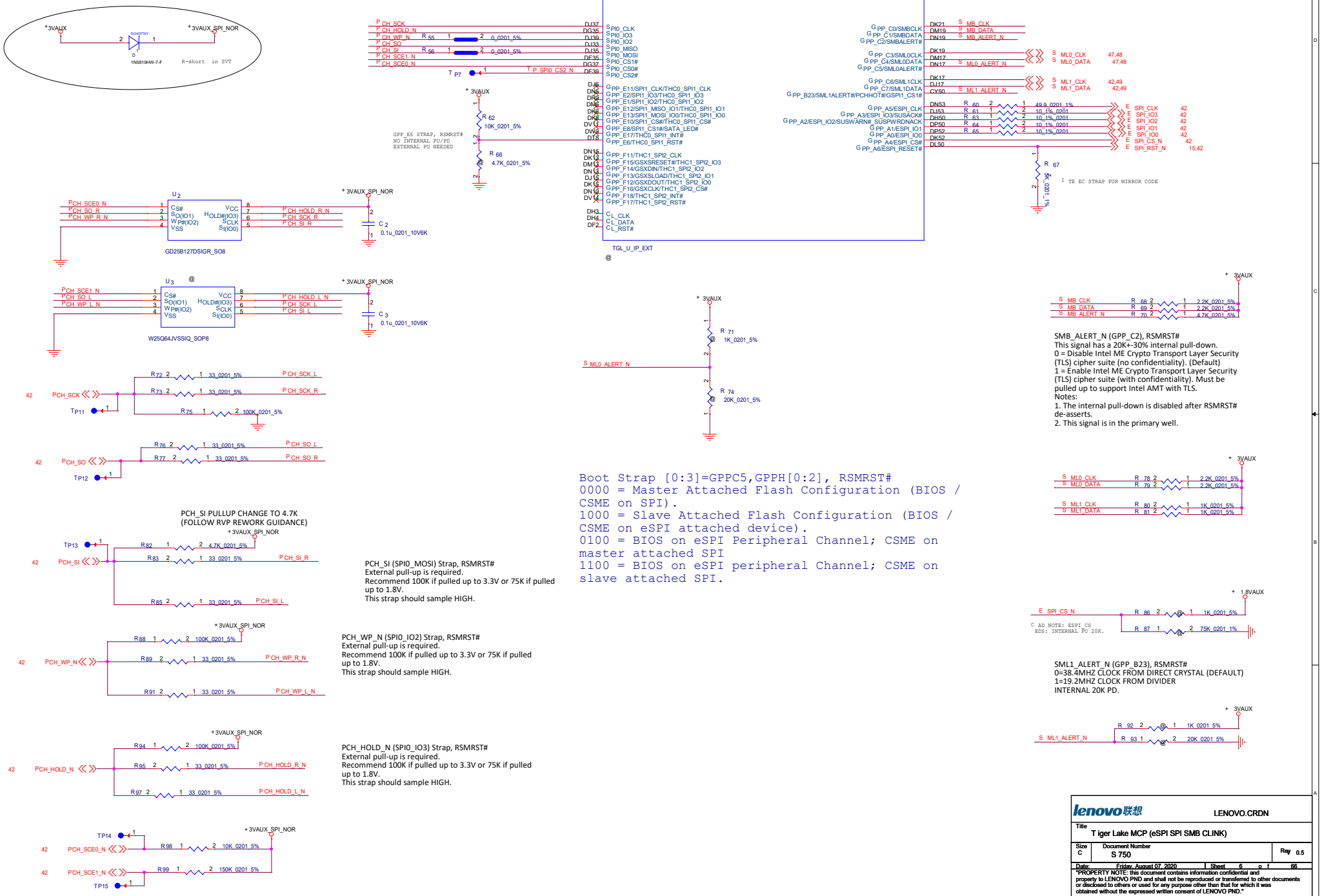
+3VAUX
+3VAUX_SPI_NOR
1N5819HW-7-F
R-short in SVT
U_1E
TGL_U_IP_EXT
GPP_E6 STRAP, RSMRST# NO INTERNAL PU/PD EXTERNAL PU NEEDED
I TE EC STRAP FOR MIRROR CODE
U2
GD25B127DSIGR_SO8
U3
W25Q64JVSSIQ_SOP8
PCH_SI PULLUP CHANGE TO 4.7K
(FOLLOW RVP REWORK GUIDANCE)
PCH_SI (SPI0_MOSI) Strap, RSMRST#
External pull-up is required.
Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH.
PCH_WP_N (SPI0_IO2) Strap, RSMRST#
External pull-up is required.
Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH.
PCH_HOLD_N (SPI0_IO3) Strap, RSMRST#
External pull-up is required.
Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH.
Boot Strap [0:3]=GPPC5,GPPH[0:2], RSMRST#
0000 = Master Attached Flash Configuration (BIOS / CSME on SPI).
1000 = Slave Attached Flash Configuration (BIOS / CSME on eSPI attached device).
0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI
1100 = BIOS on eSPI peripheral Channel; CSME on slave attached SPI.
SMB_ALERT_N (GPP_C2), RSMRST#
This signal has a 20K+-30% internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.
SML1_ALERT_N (GPP_B23), RSMRST#
0=38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)
1=19.2MHZ CLOCK FROM DIVIDER
INTERNAL 20K PD.
LENOVO.CRDN
Title
T iger Lake MCP (eSPI SPI SMB CLINK)
Size C
Document Number S 750
Rev 0.5
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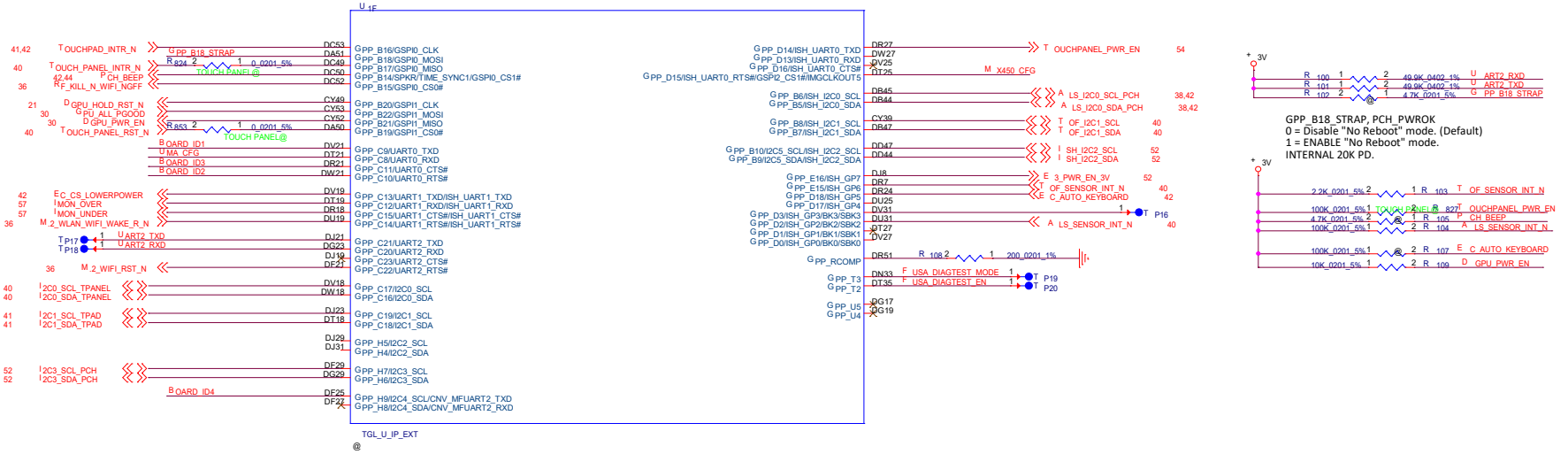
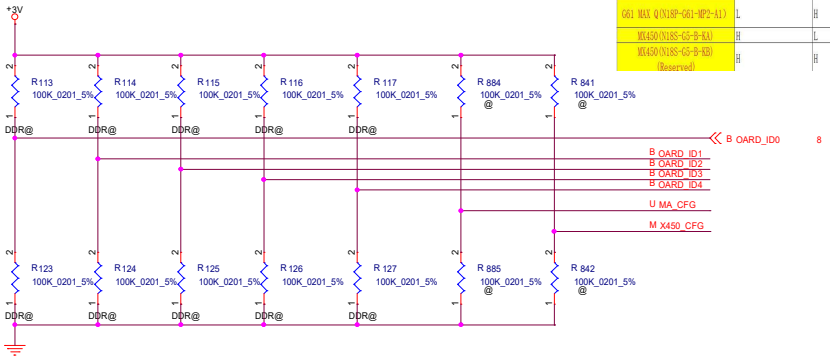
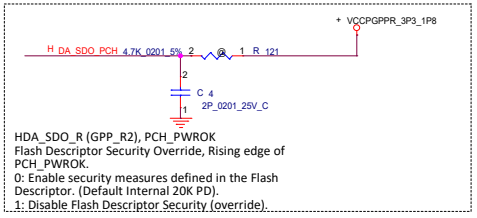
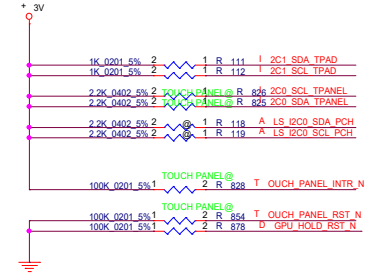


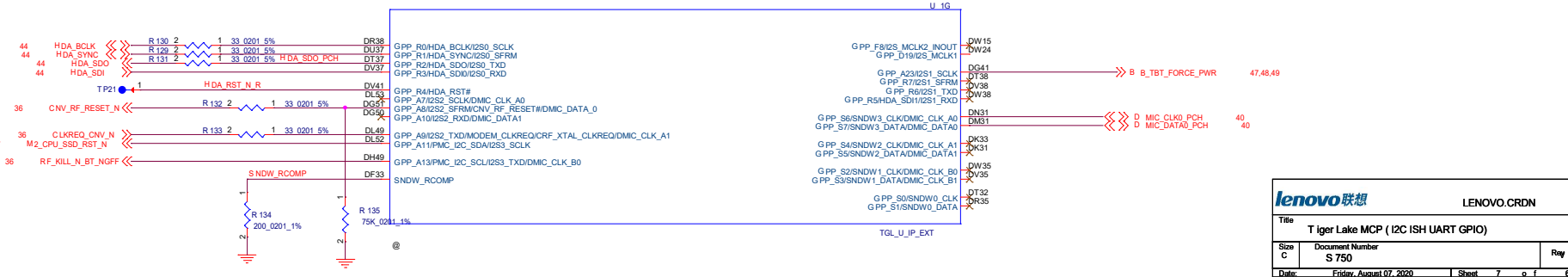
BOARD ID

	UMA_CFG R884=1/R885=0	MX450_CFG R841=1/R842=0
UMA	L	L
G61 MAX Q(N18P-G61-MP2-A1)	L	H
MX450(N18S-G5-B-KA)	H	L
MX450(N18S-G5-B-KB) (Reserved)	H	H









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Title: T iger Lake MCP (I2C ISH UART GPIO)			
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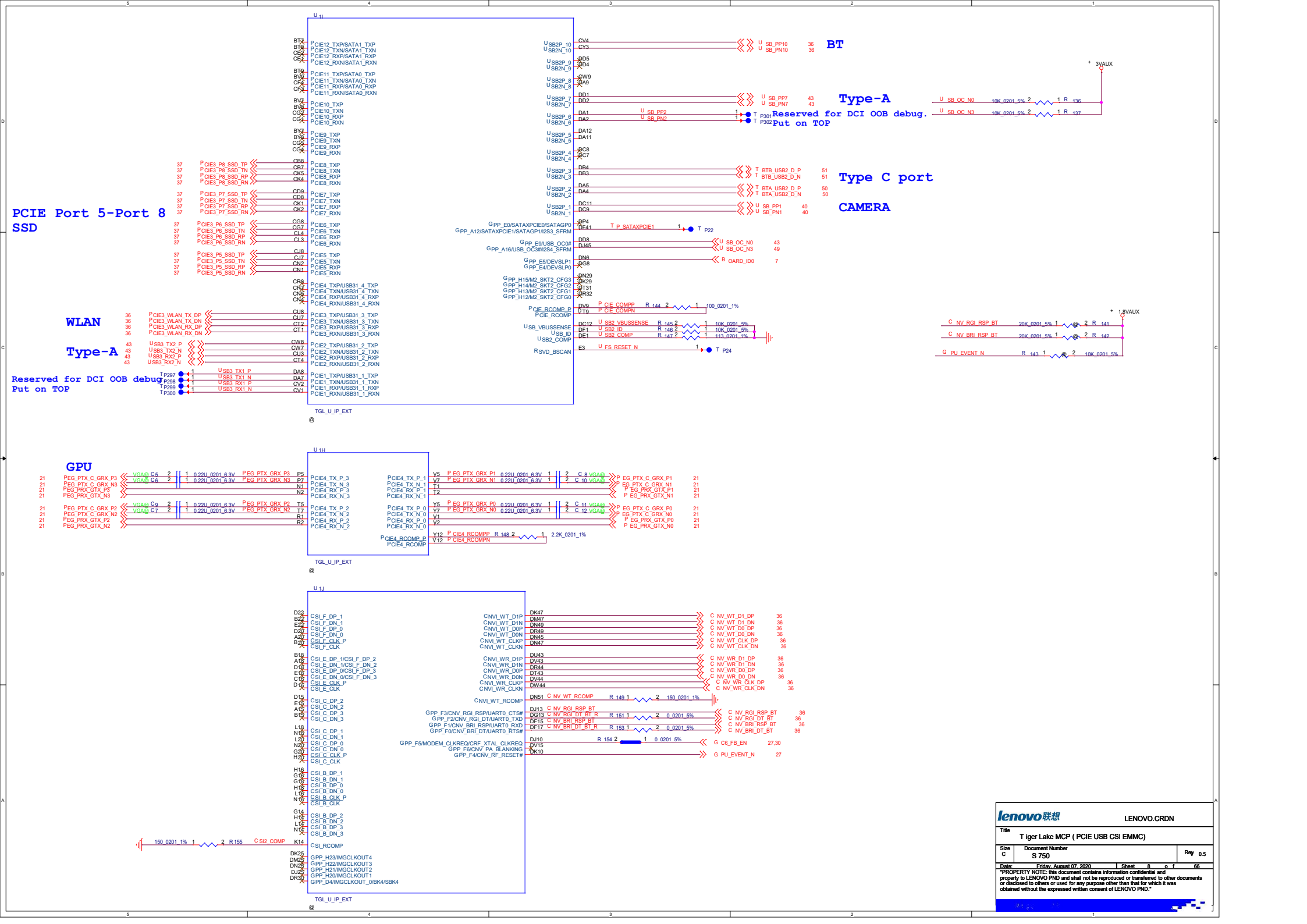
PCIE Port 5-Port 8
SSD
WLAN
Type-A
Reserved for DCI OOB debug
Put on TOP
BT
Type-A
Reserved for DCI OOB debug.
Put on TOP
Type C port
CAMERA
GPU
TGL_U_IP_EXT
LENOVO.CRDN
T iger Lake MCP (PCIE USB CSI EMMC)
S 750
Friday, August 07, 2020
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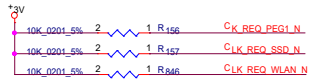
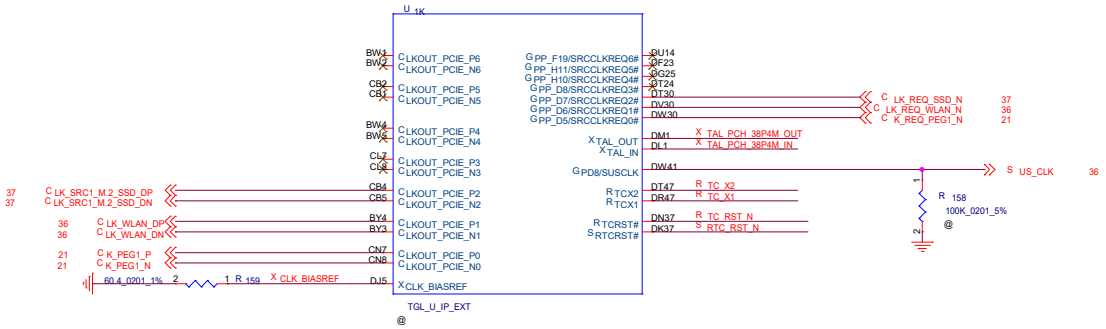
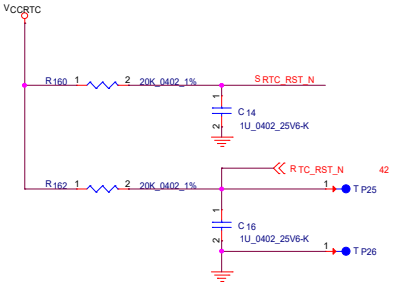


CAD NOTE:
Any un-used SRCCLKRQ# signal must be left as no connects

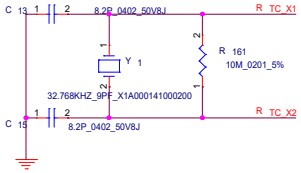


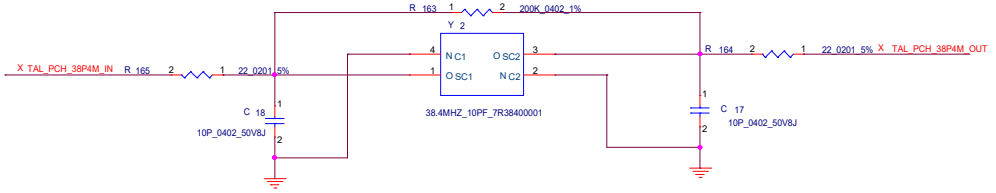


ME RESET
SAVE ME = PU (Default)
CLEAR ME = PD

CMOS RESET
SAVE CMOS = PU (Default)
CLEAR CMOS = PD

TP8 TP9 Need to put on the TOP





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Title	T iger Lake MCP (CLK)		
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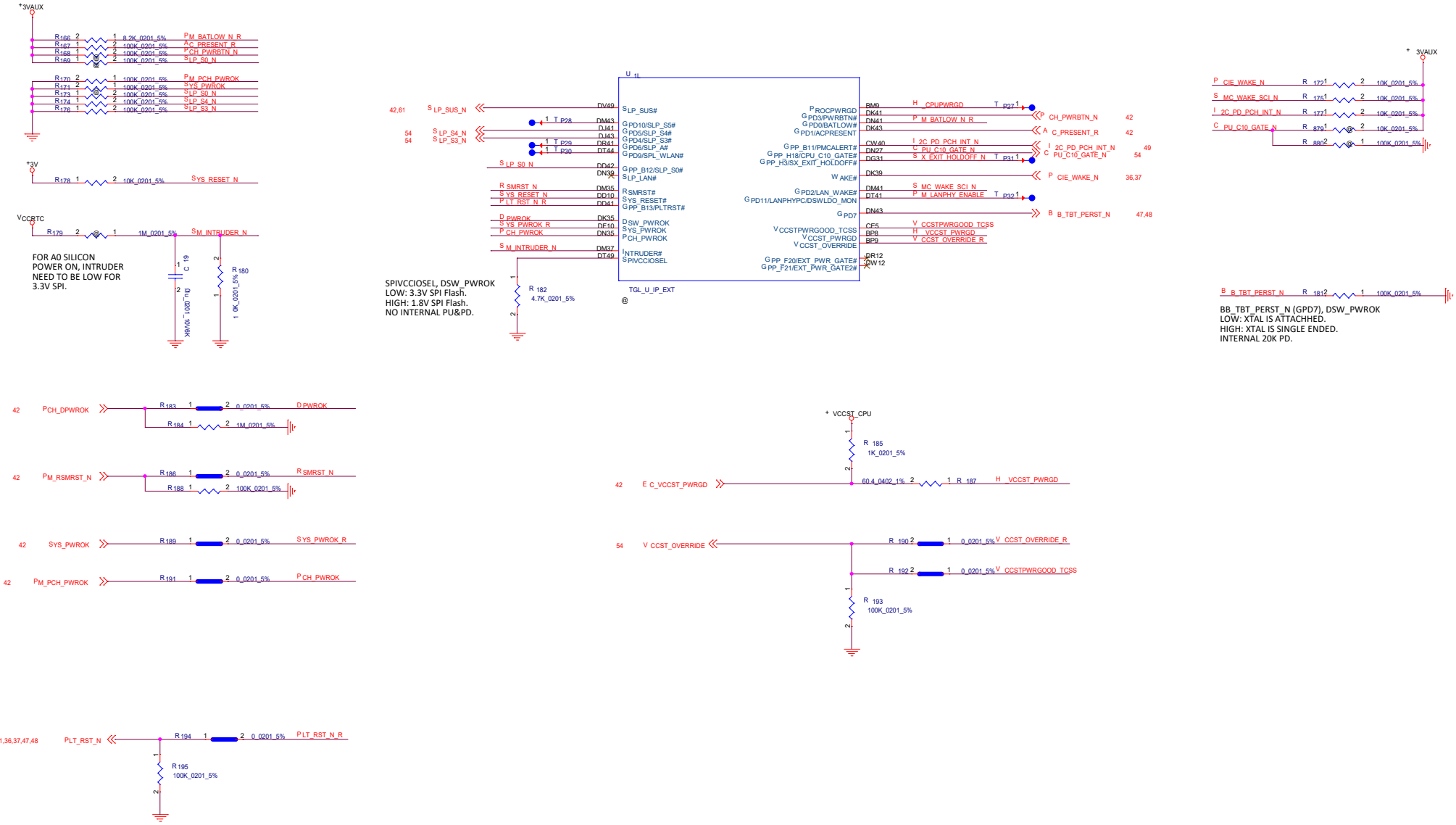

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Title: T iger Lake MCP (PM)

Size: C | Document Number: S 750 | Rev: 0.5

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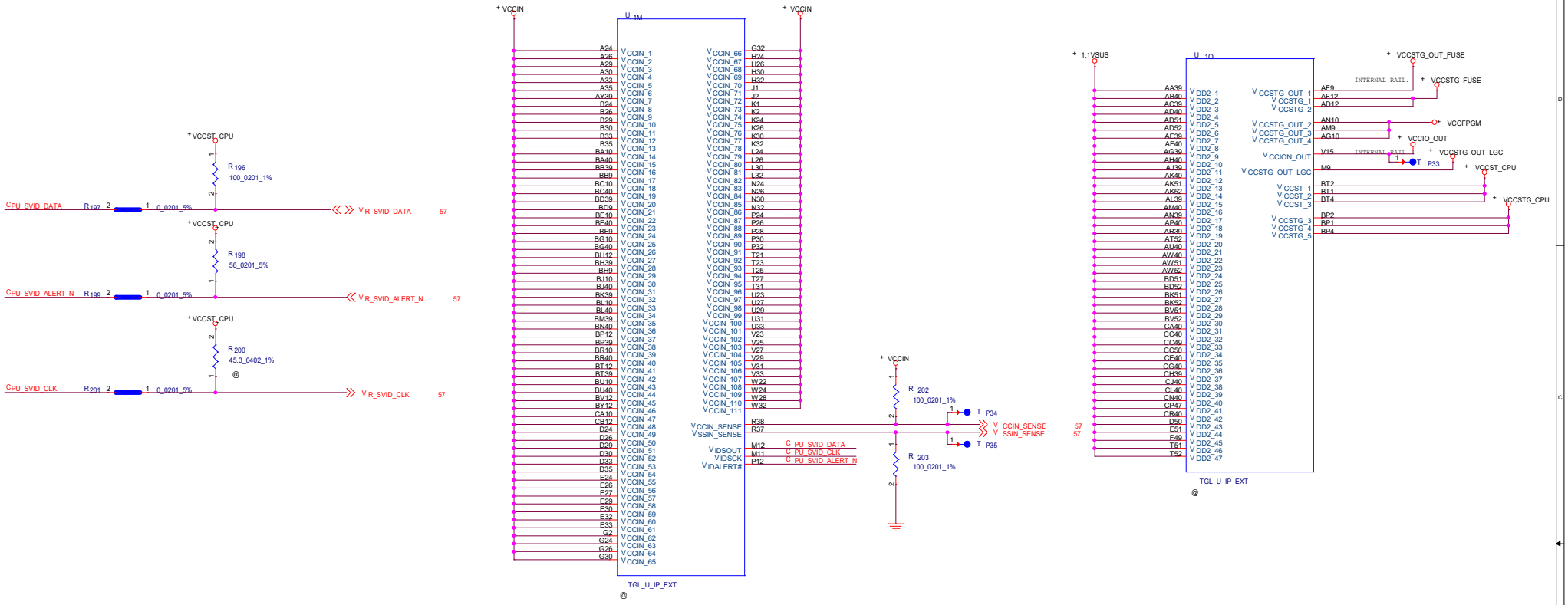
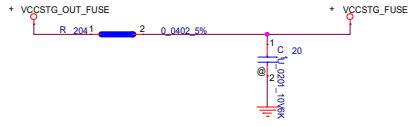
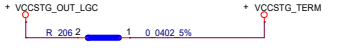
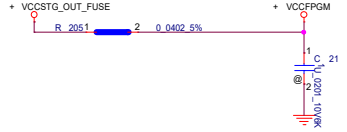


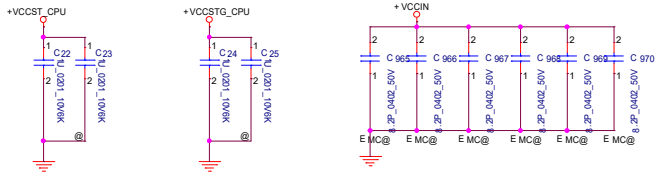


C AD NOTE:
FOR SIDEBAND TERMINATION.

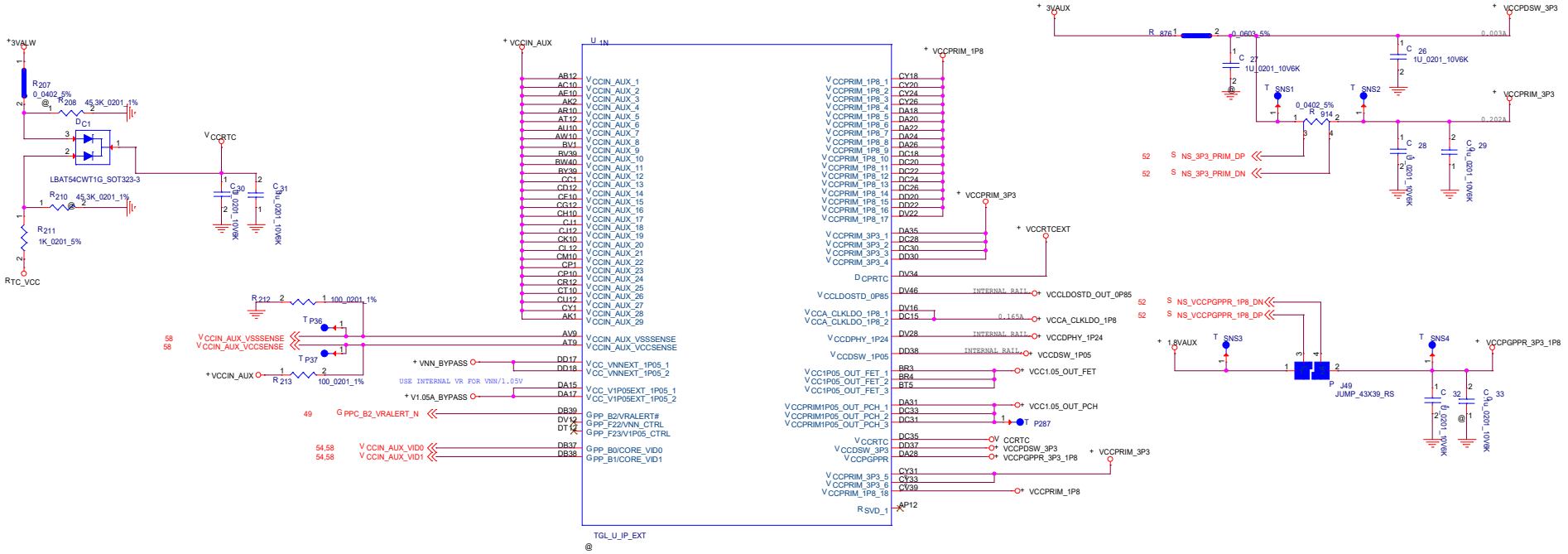


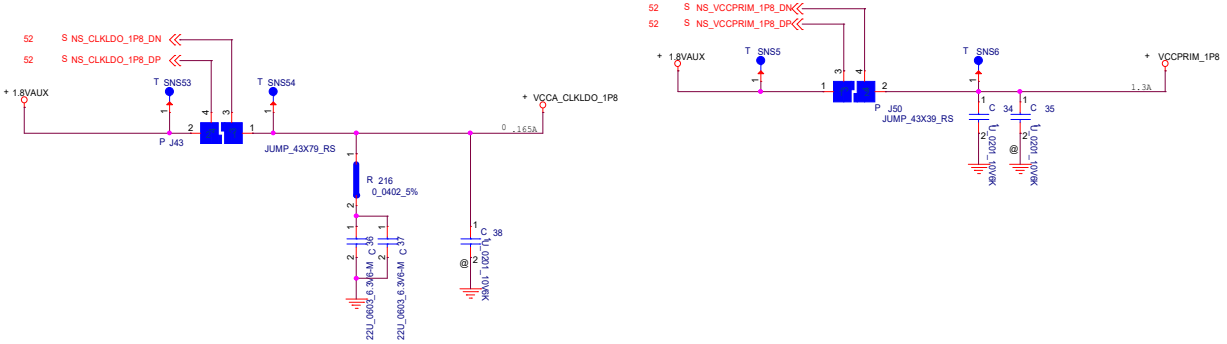


VCCST, VCCSTG DE-COUPLING

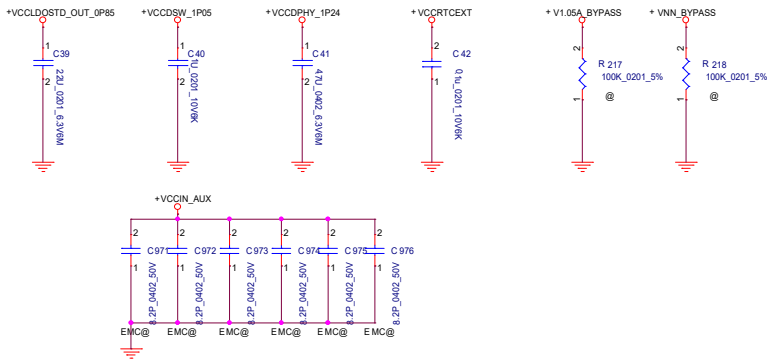


lenovo联想	LENOVO.CRDN	
Title: T iger Lake MCP (PROCESSOR POWER)		
Size: C	Document Number: S 750	Rev: 0.5
Date: Friday, August 07, 2020	Sheet 1 1 of 66	





PCH POWER RAIL DE-COUPLING



lenovo联想	LENOVO.CRDN		
Title	T iger Lake MCP (PCH POWER)		
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Required: 4X220uF, 29x10uF, 10X22uF, 12X1uF
Designed: 1X330uF, 23x10uF, 13X22uF, 12X1uF

+VCCIN

For EE noise debug MLCC

PLACE COLSED TO HEAT SINK.

Place CPU back side

Required: 2X47uF, 10X1uF, 16X10uF
Designed: VR 4X22uF, 2X22uF,12X1uF, 19X10uF

+ 1.1VSUS

EMC

EMC CAPS -PLACEMENT: < 5MM FROM SOC'S VCCIN

+ VCCIN

C 126 0.1u_0201_10V6K
C 127 120P_0201_50V
C 128 15P_0201_50V
C 129 3P_0201_25V_C

Required: 2X220uF, 6X47uF, 12X22uF, 17X10uF
Designed: 1X330uF, 20X22uF, 19X10uF, 4X1uF

+VCCIN_AUX

1pcs 3T 22uF instead of 1pcs 2T 22uF 4pcs 1uF

Place CPU back side

EMC

EMC CAPS -PLACEMENT: < 5MM FROM SOC'S VCCIN_AUX

+ VCCIN_AUX

C 149 0.1u_0201_10V6K
C 150 120P_0201_50V
C 151 15P_0201_50V
C 152 3P_0201_25V_C

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LENOVO.CRDN

Title: T iger Lake MCP (Power CAP)

Size: C | Document Number: S 750 | Rev: 0.5

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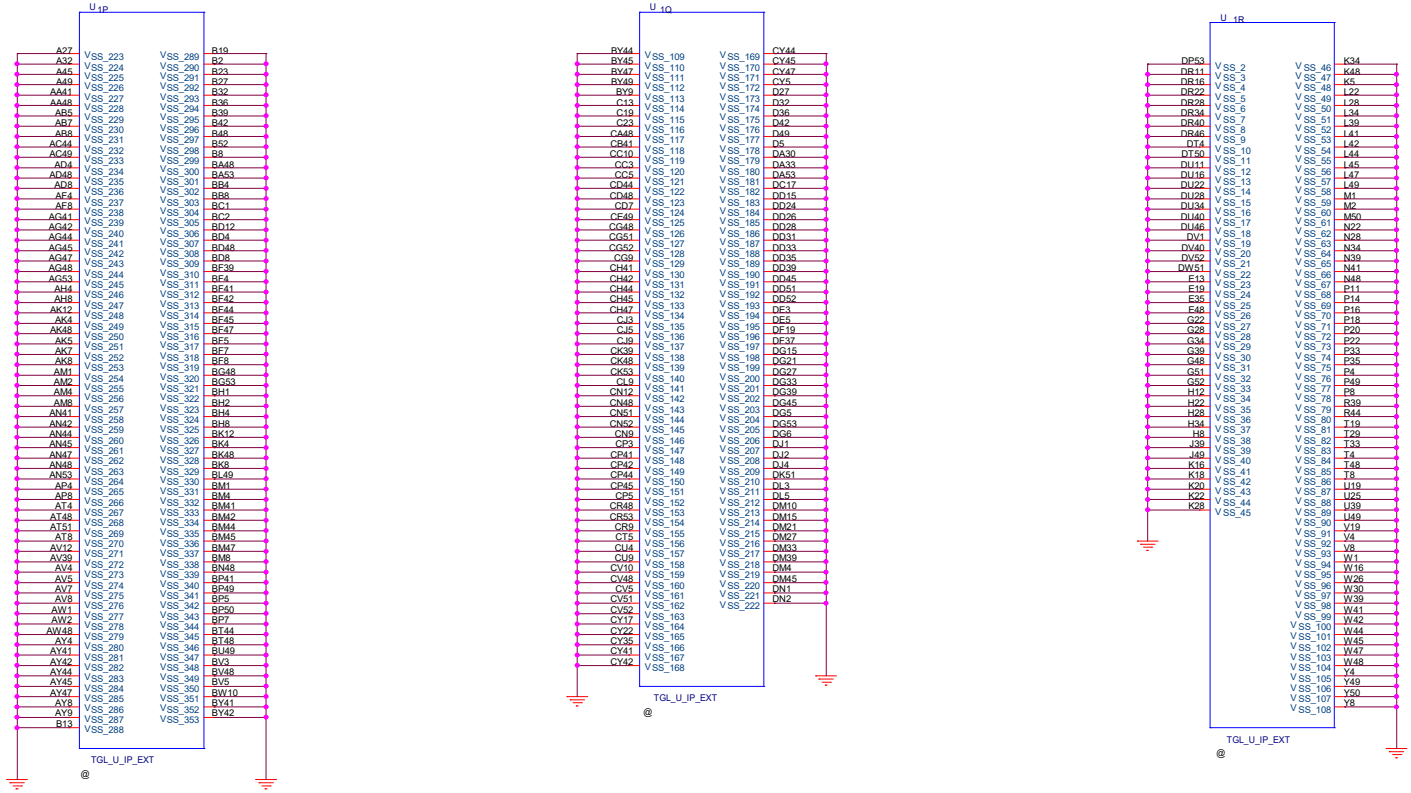

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Title: T iger Lake MCP (GND)		
Size: C	Document Number: S 750	Rev: 0.5
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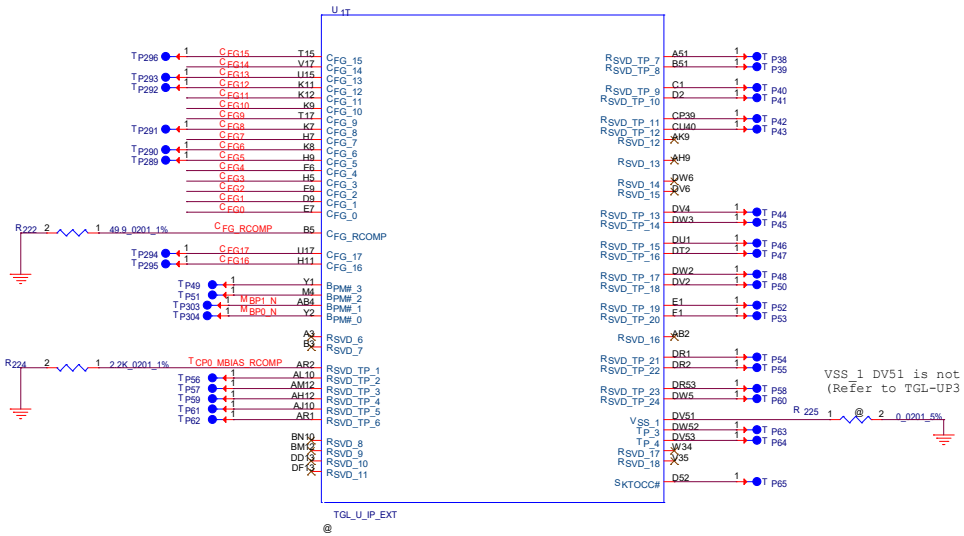
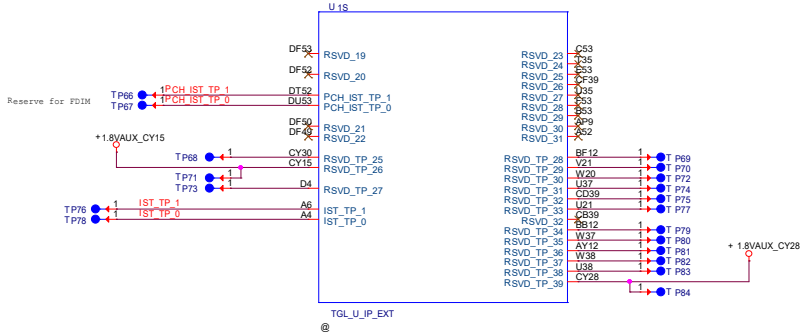
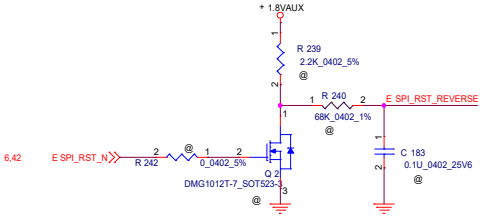
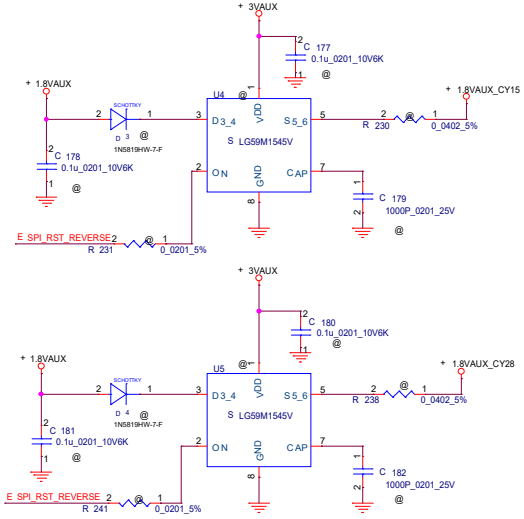


VSS_1 DV51 is not connected to GND
(Refer to TGL-UP3 RVP/AEP design)

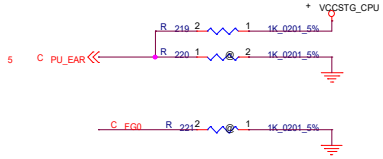






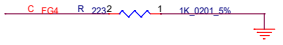
ES1 Workaround Circuit (DOC# 614056)

PROCESSOR CFG STRAPS

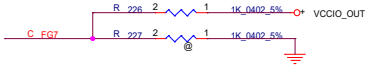


Stall reset sequence after PCU PLL lock until de-asserted	
EAR	1:Normal(Default) *
	0:Stall

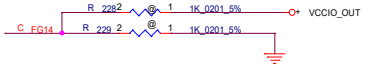
Changed From CFG0 to EAR (Refer to WW32 MOW)



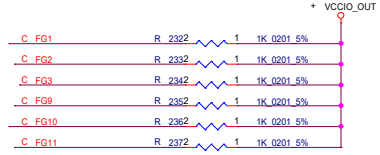
Embedded Display Port Presence Strap	
CFG4	1:Disable
	0:Enable(Default) *



PEG deferred link training	
CFG7	1:TBD(Default) *
	0:TBD



PEG60 Lane Reversal	
CFG14	1:Normal
	0:Reversed(Default) *



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Title: T iger Lake MCP (RSVD)

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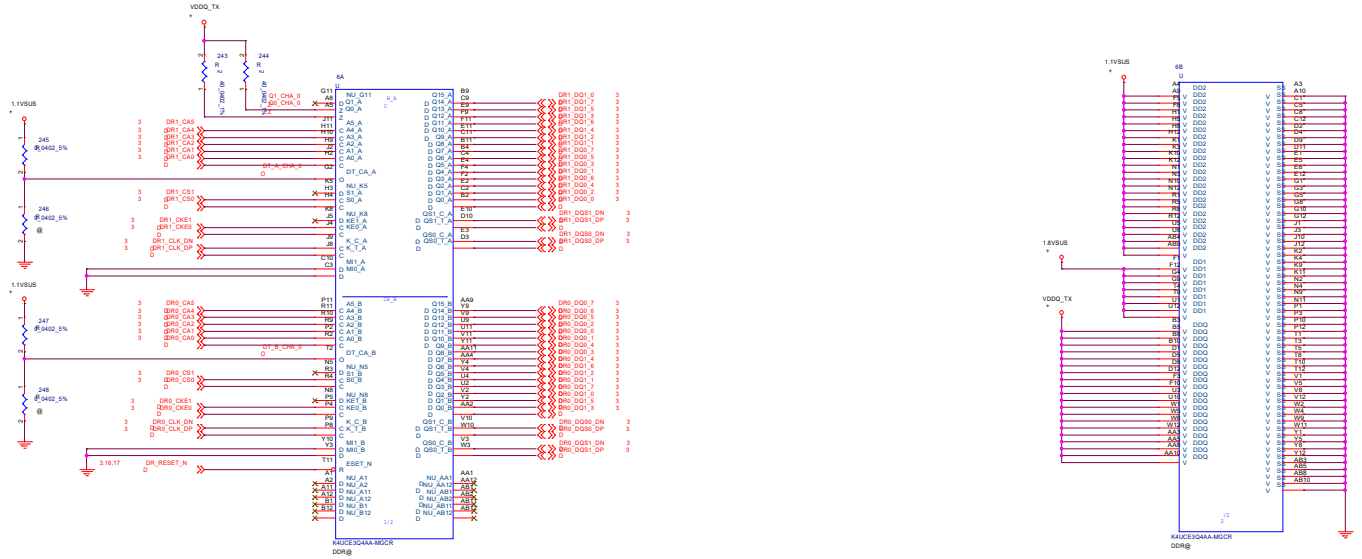

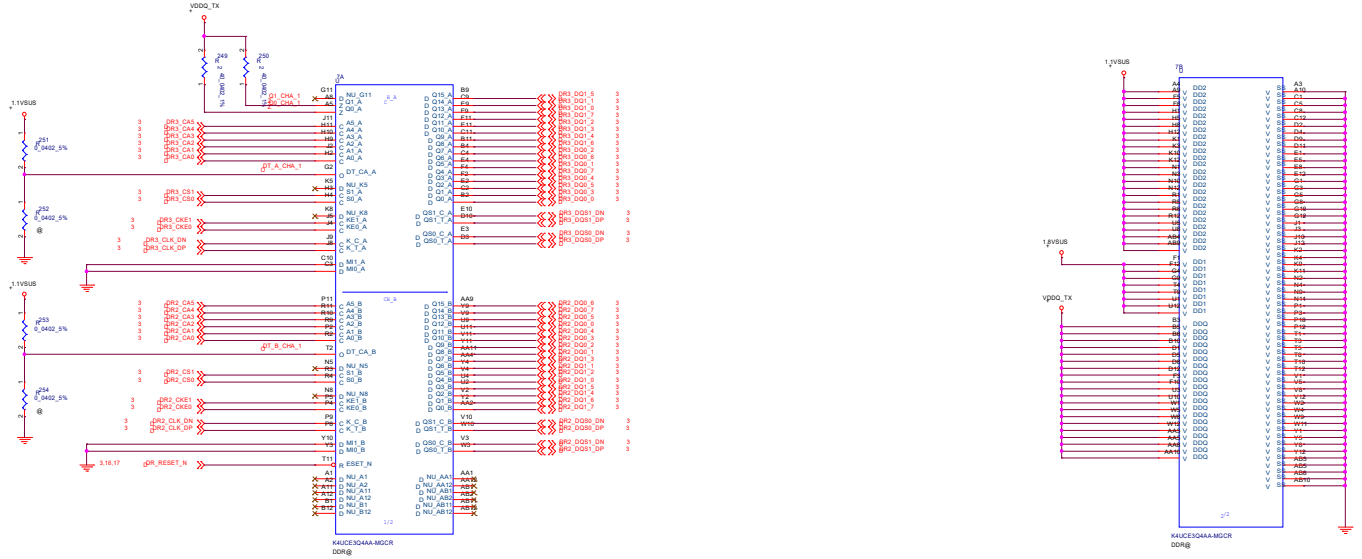

Title	LP4X-CHA ONBD
Size	D
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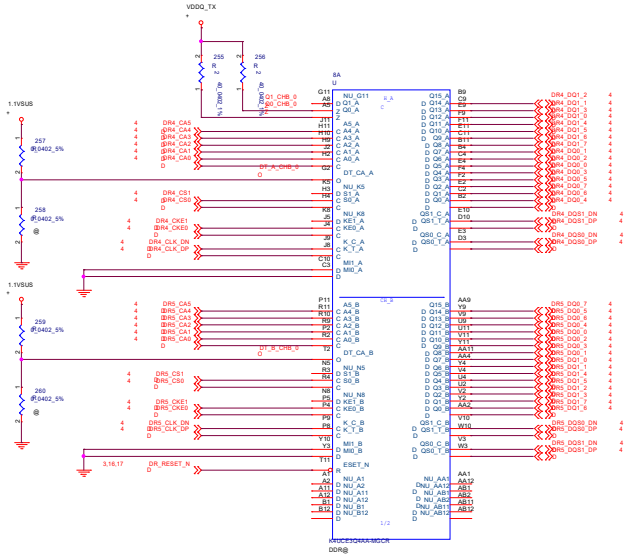

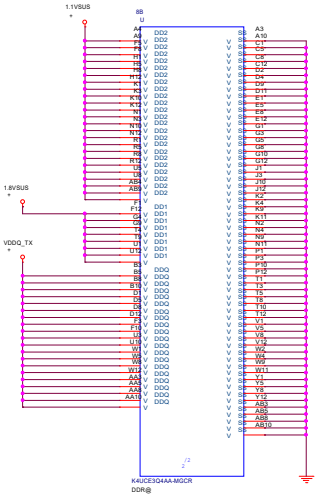

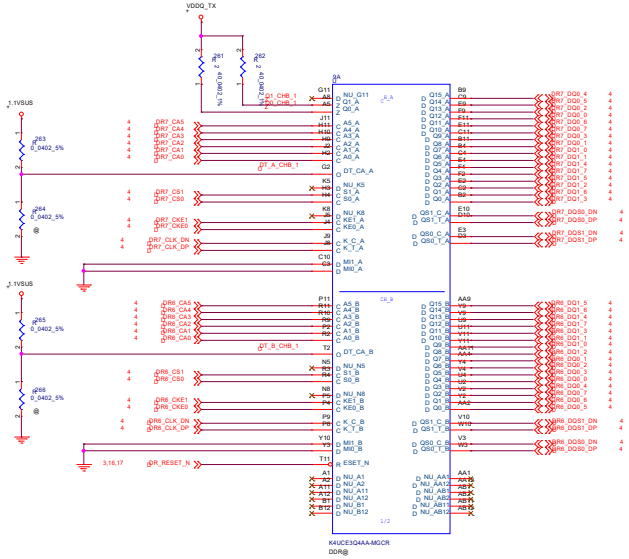

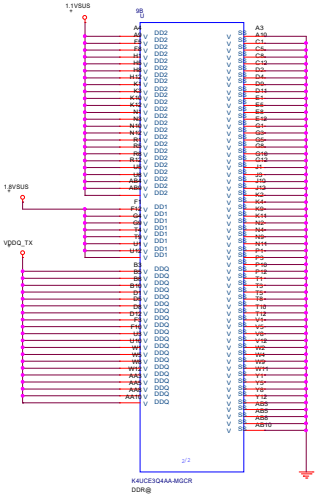

lenovo 联想	LENOVO.CRDN		
Title:	LP4X-CHB ONBD		
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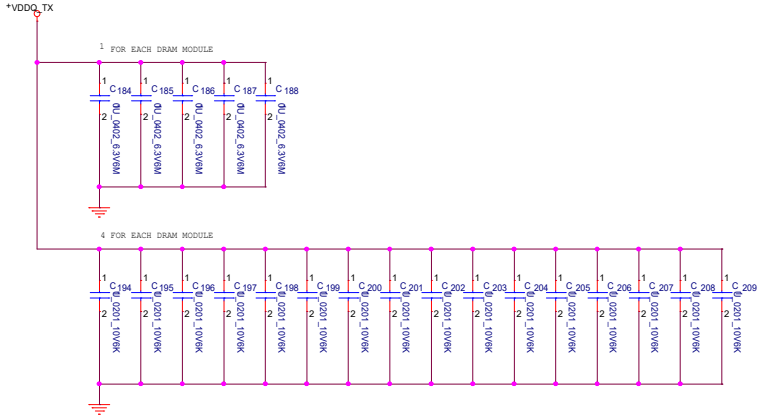
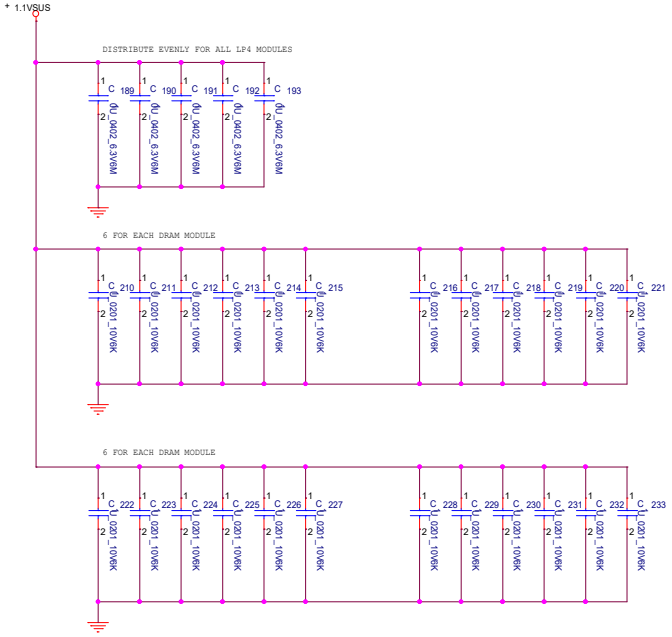
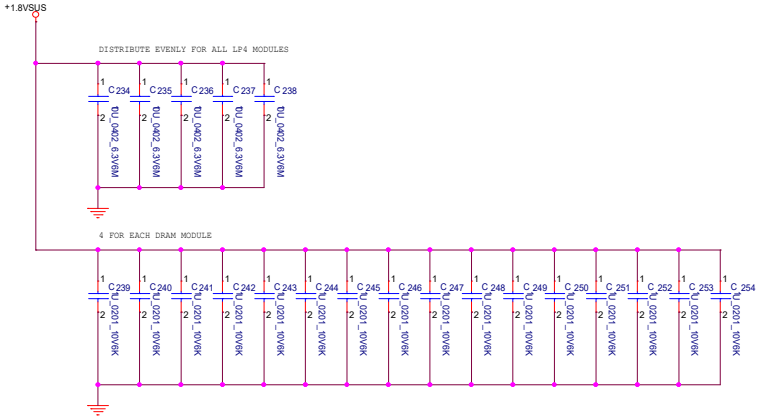
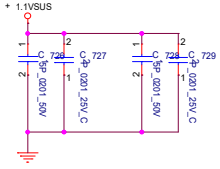






EMC CAP CHANNEL 0 AND 1



EMC CAP:
1. PLACE 4MM FROM DRAM
2. PLACE EACH SET WITHIN 12MM

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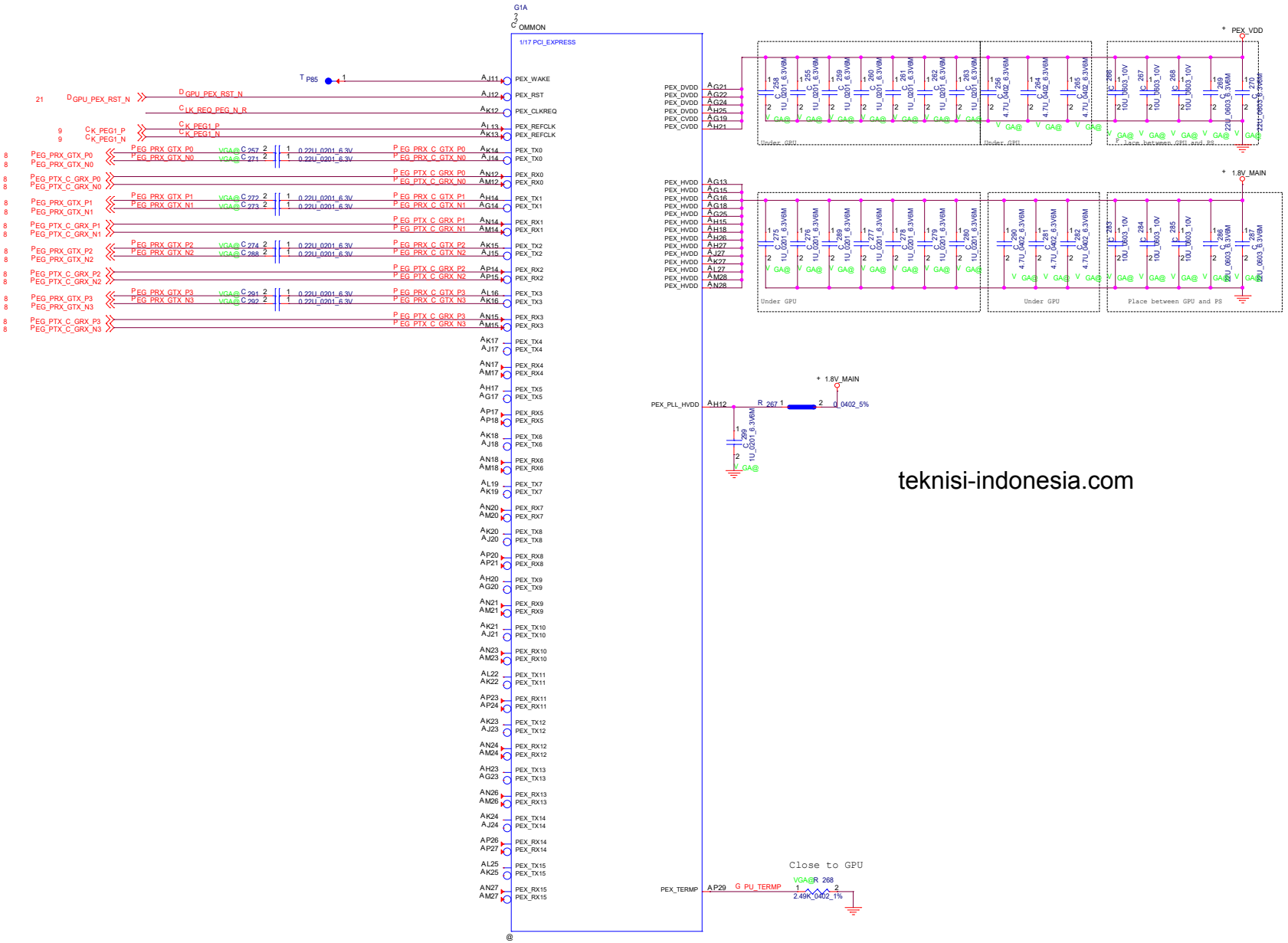
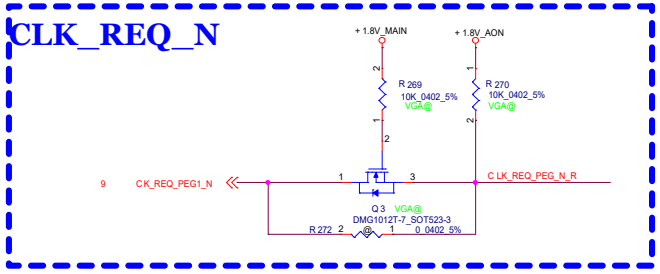
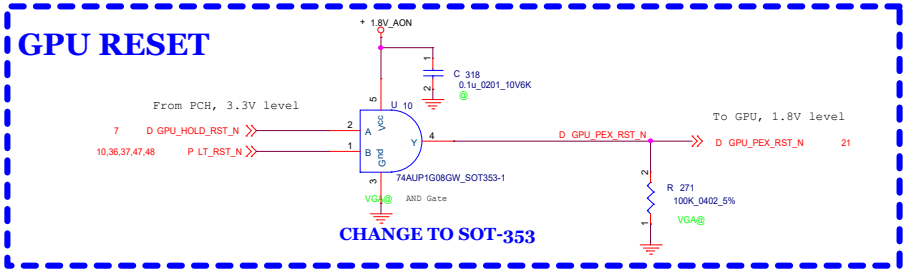


CLK_REQ_N



GPU RESET



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Title: G PU PCIE		
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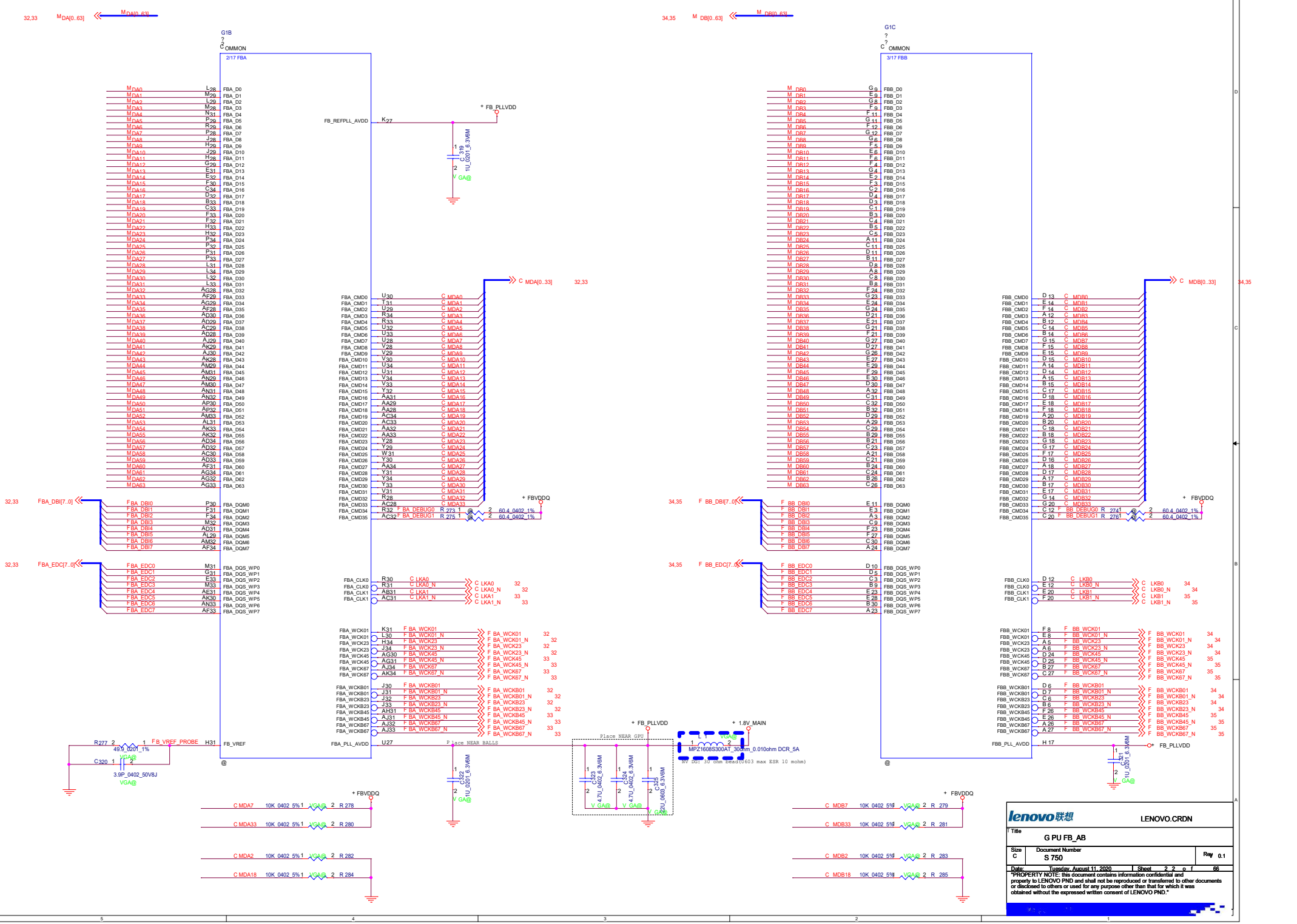
G1B
COMMON
2/17 FBA
G1C
COMMON
3/17 FBB
FB_REFPLL_AVDD
FB_PLLVDD
FBA_PLL_AVDD
FBB_PLL_AVDD
FB_VREF
FB_VREF_PROBE
FBVDDQ
1.8V_MAIN
MPZ1608S300AT_300ohm_0.010ohm DCR_5A
Place NEAR GPU
Place NEAR BALLS
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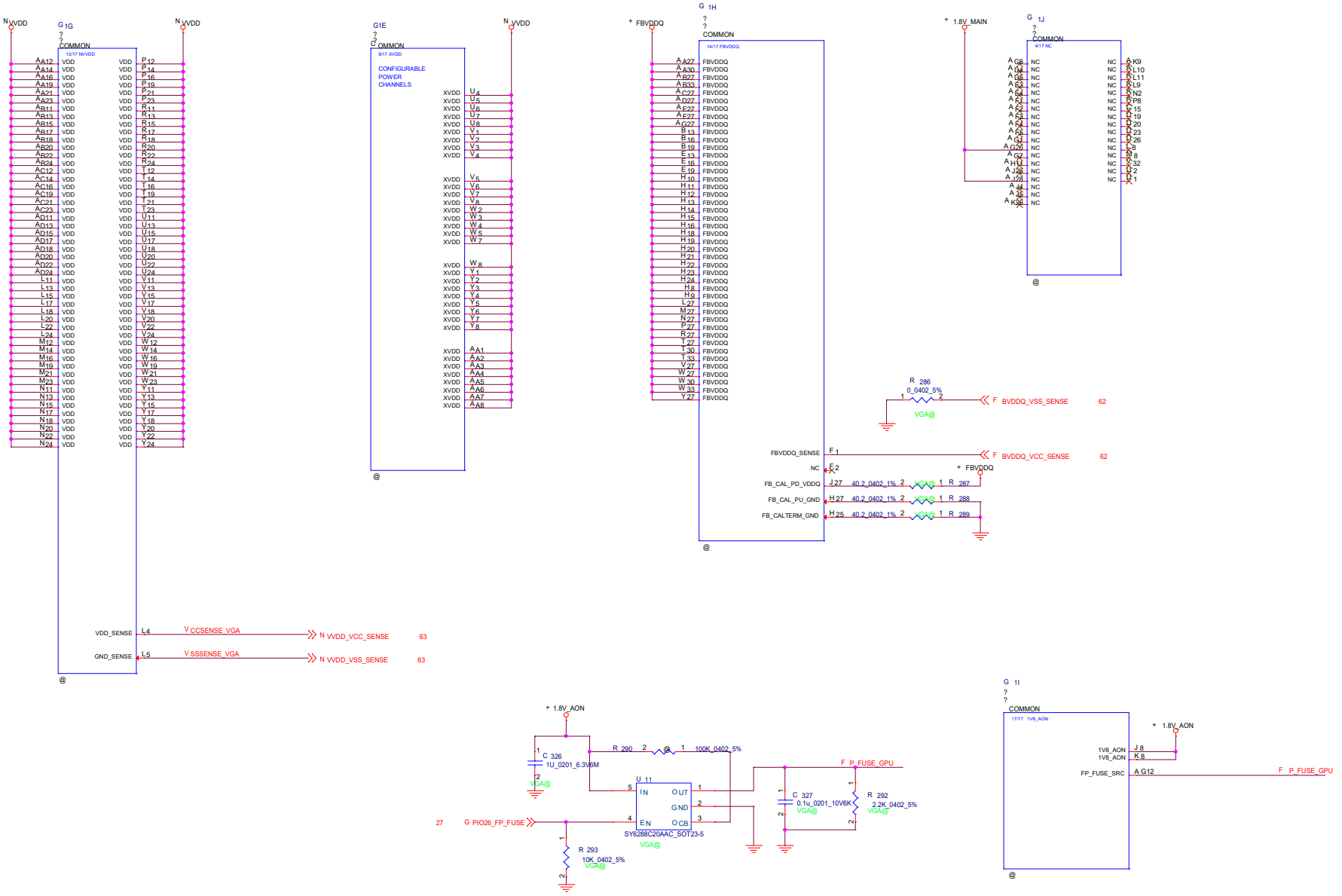

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Title: G PU PWR			
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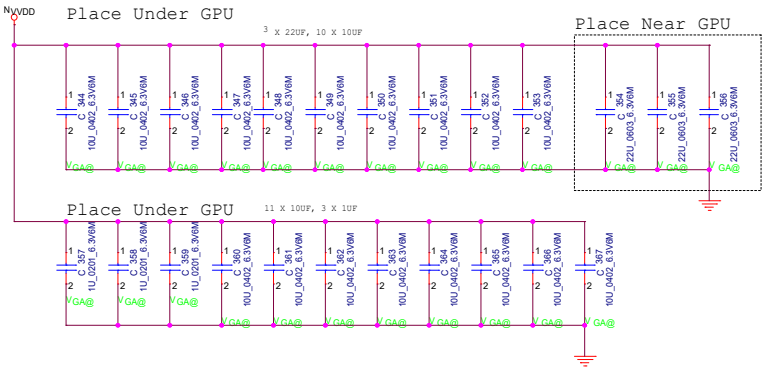
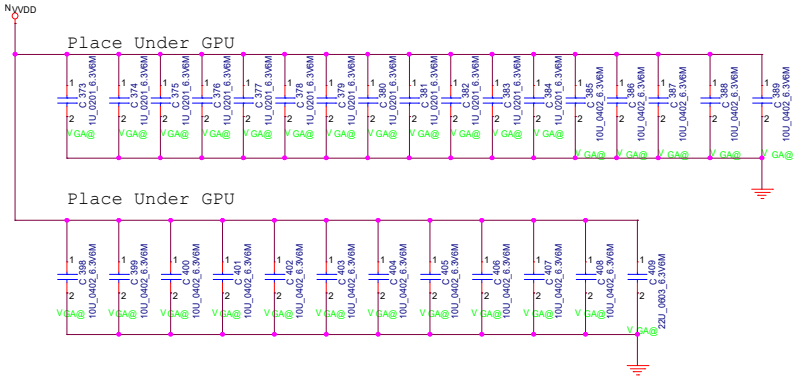
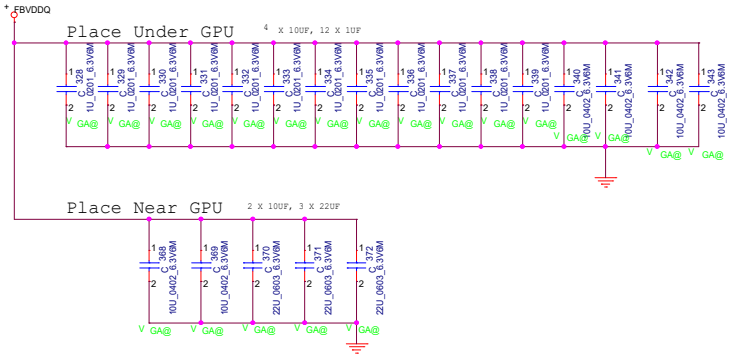
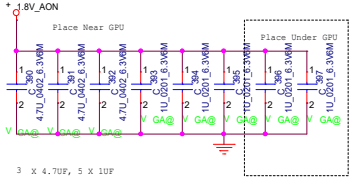
Follow NV ref-design



1 x 22uF
16x 10uF
12x 1uF







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Title: G PU Decoupling

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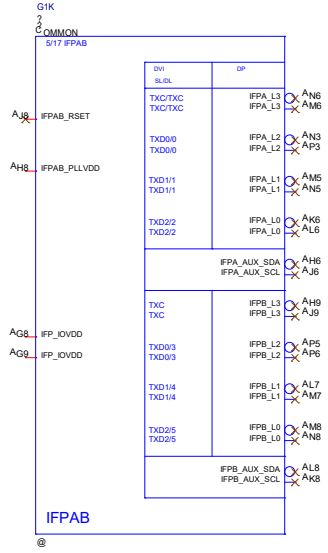

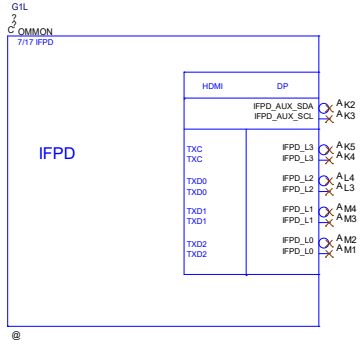

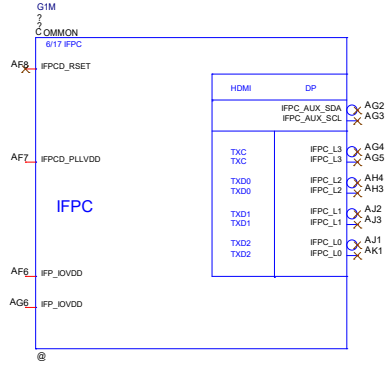

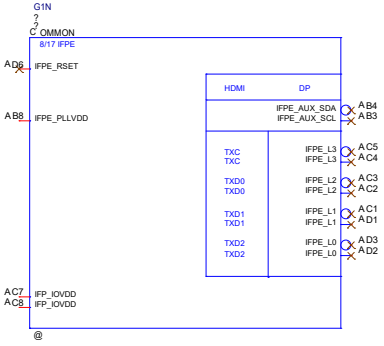

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Title
G PU IFP ABCDE

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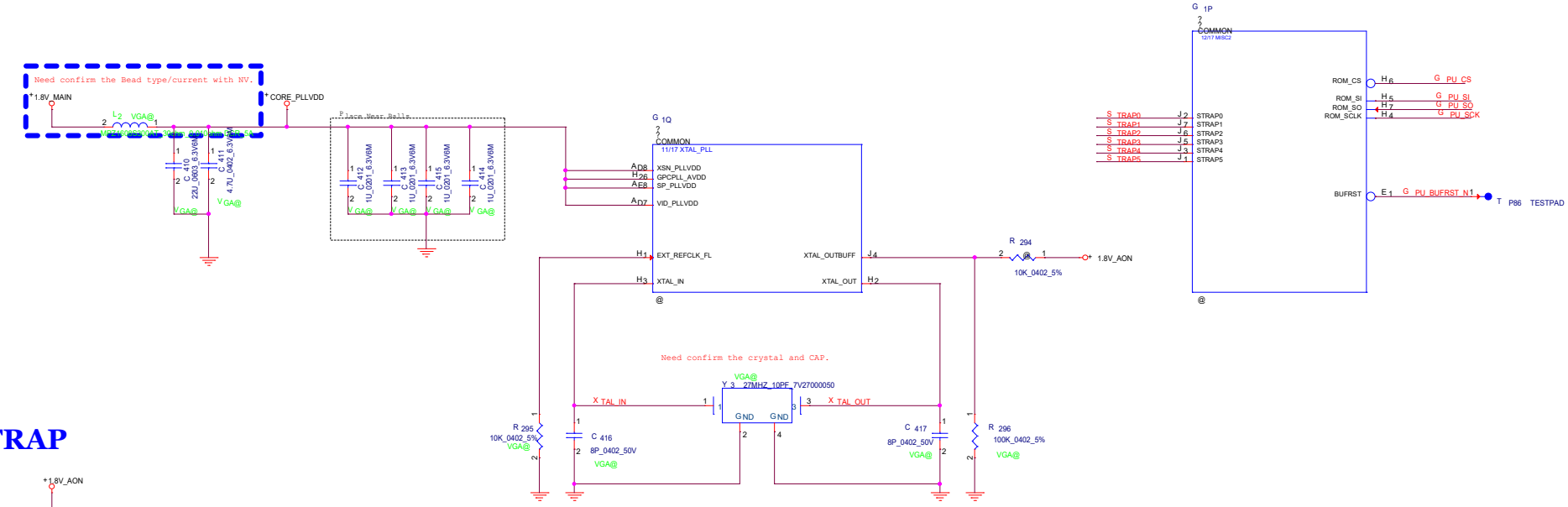
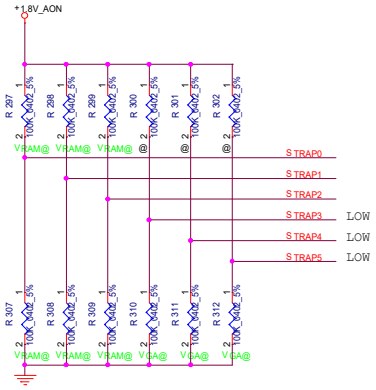
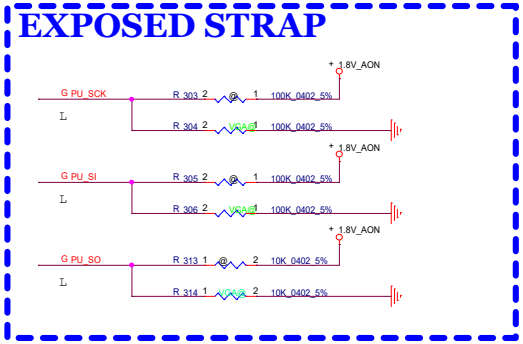


STRAP

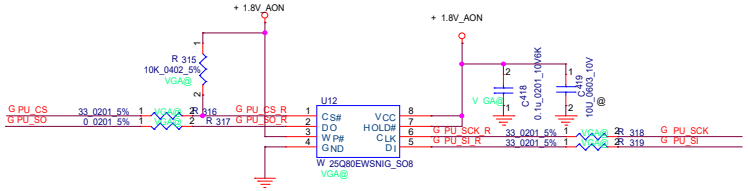


EXPOSED STRAP



STRAP2-0 , Please ref RVL for BOM stuffing
Samsung: L L L
Micron: L L H

GPU_SCK(LSB)/GPU_SI/GPU_SO(MSB) : L L L



GDDR6 RAM_CFG													
GPU	Memory Type	FBVDD/ FBVDDQ	Memory Density	Memroy configuration	Vendor	Manufacturer Part Number	Die Revision	Memory Speed CK Grade	Memory D/C Minimum	Strap	Strap2	Strap1	Strap0	Status
N18P-G62/G61	GDDR6	1.20V and 1.25V	8Gb	2chx256Mx16	Micron	MT61K256M32JE-14:A	A-die	14 Gbps	N/A	0x1	L	L	H	Prodution Candidate
					Samsung	K4Z80325BC-HC14	C-die	14 Gbps	N/A	0x0	L	L	L	Prodution Candidate

GDDR6 RAM_CFG													
GPU	Memory Type	FBVDD/ FBVDDQ	Memory Density	Memroy configuration	Vendor	Manufacturer Part Number	Die Revision	Memory Speed CK Grade	Memory D/C Minimum	Strap	Strap2	Strap1	Strap0	Status
N18S-G5	GDDR6	1.20V	8Gb	2chx256Mx16	Micron	MT61K256M32JE-14:A	A-die	14 Gbps	1940	0x1	L	L	H	Prodution Candidate
					Samsung	K4Z80325BC-HC14	C-die	14 Gbps	2001	0x0	L	L	L	Prodution Candidate

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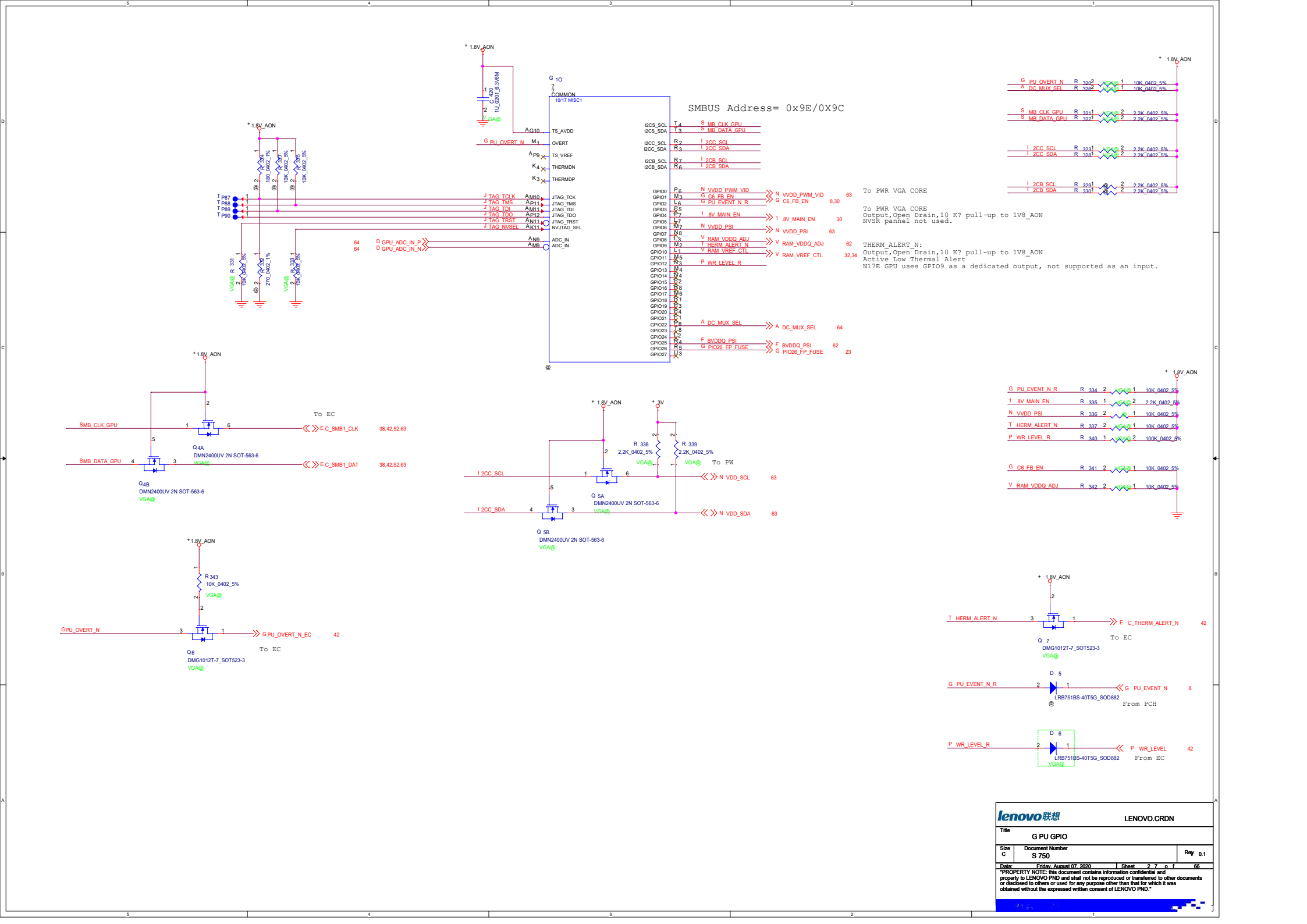
SMBUS Address= 0x9E/0X9C
To PWR VGA CORE
To PWR VGA CORE
Output,Open Drain,10 K? pull-up to 1V8_AON
NVSR pannel not used.
THERM_ALERT_N:
Output,Open Drain,10 K? pull-up to 1V8_AON
Active Low Thermal Alert
N17E GPU uses GPIO9 as a dedicated output, not supported as an input.
To EC
To EC
To PW
From PCH
From EC
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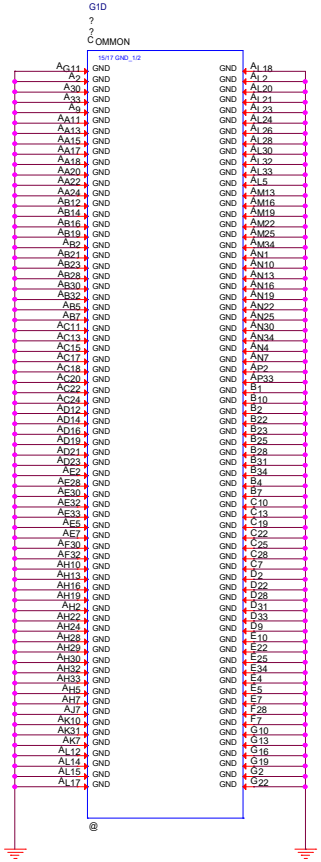

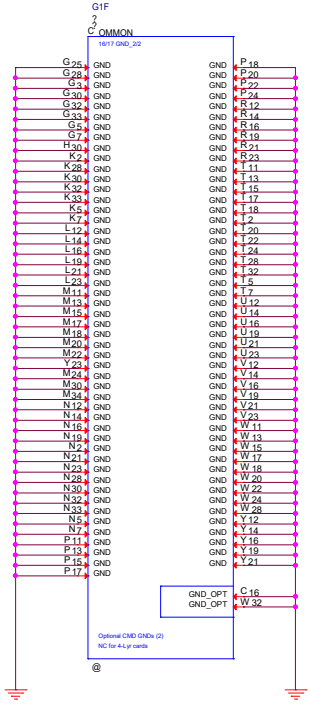

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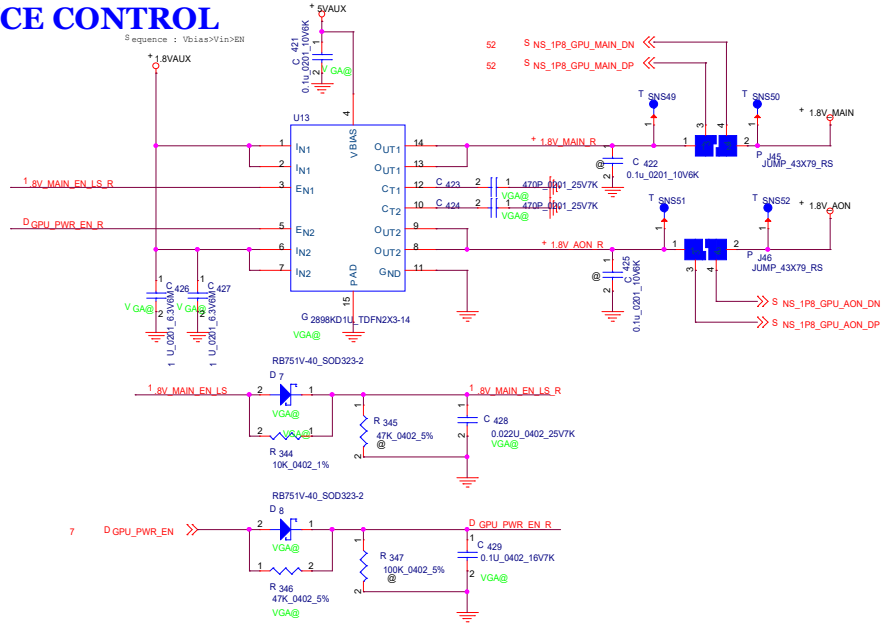
POWER SEQUENCE CONTROL



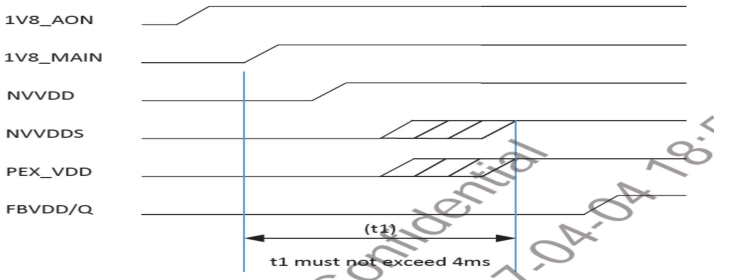


Figure 7.5 Example of Power-Up Sequencing Order

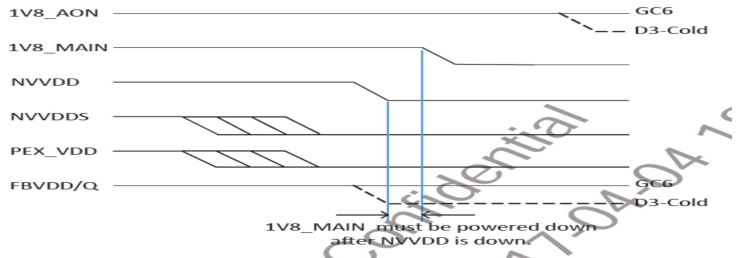
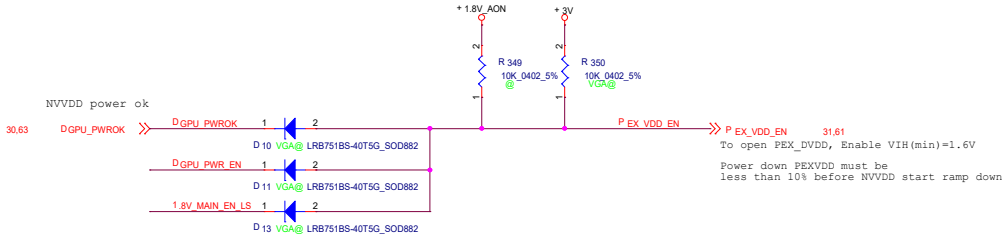
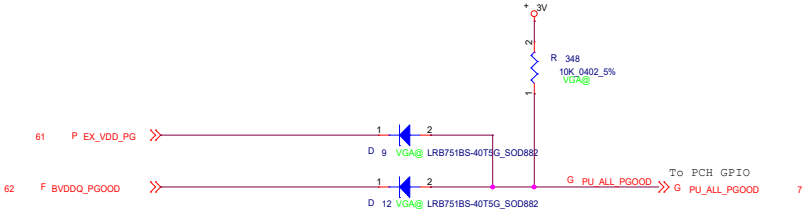
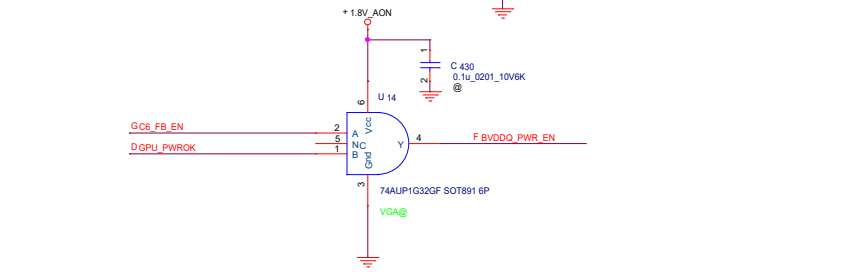
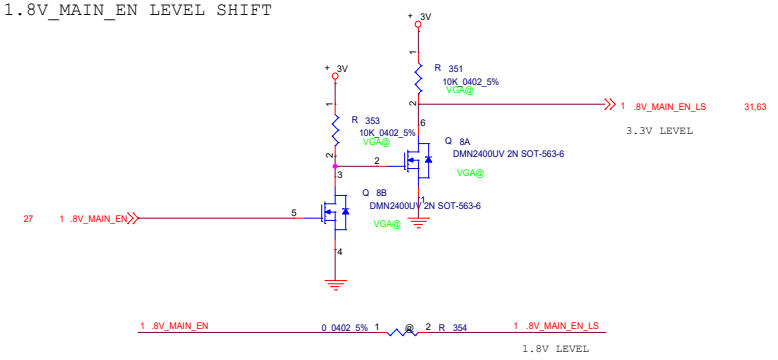


Figure 7.6 Example of Power-Down Sequencing Order









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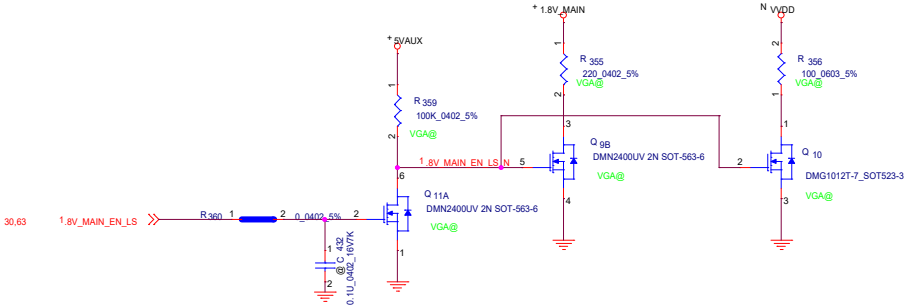

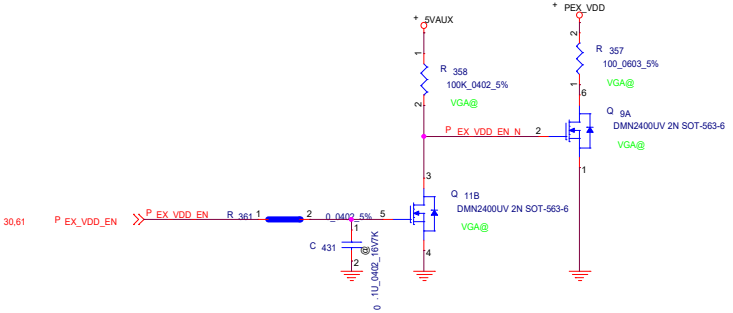

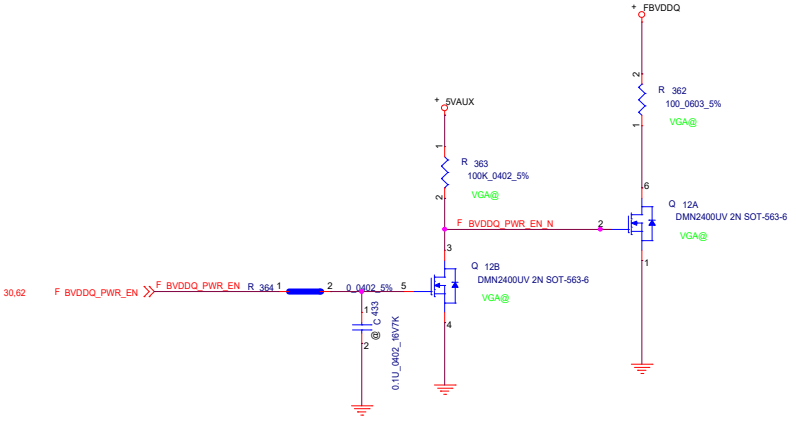

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Title: G PU POWER DISCHARGE

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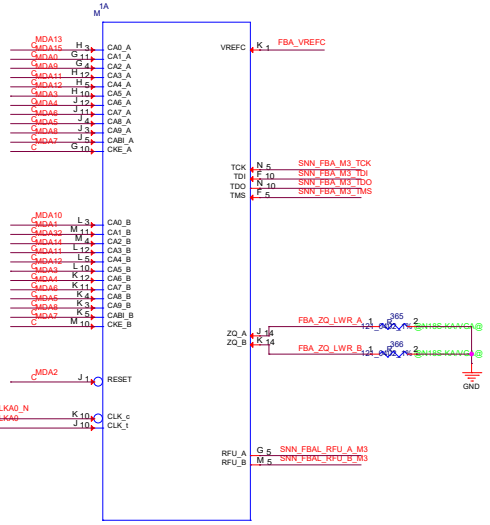
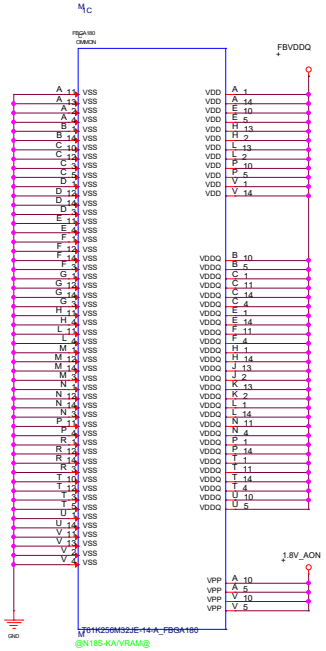
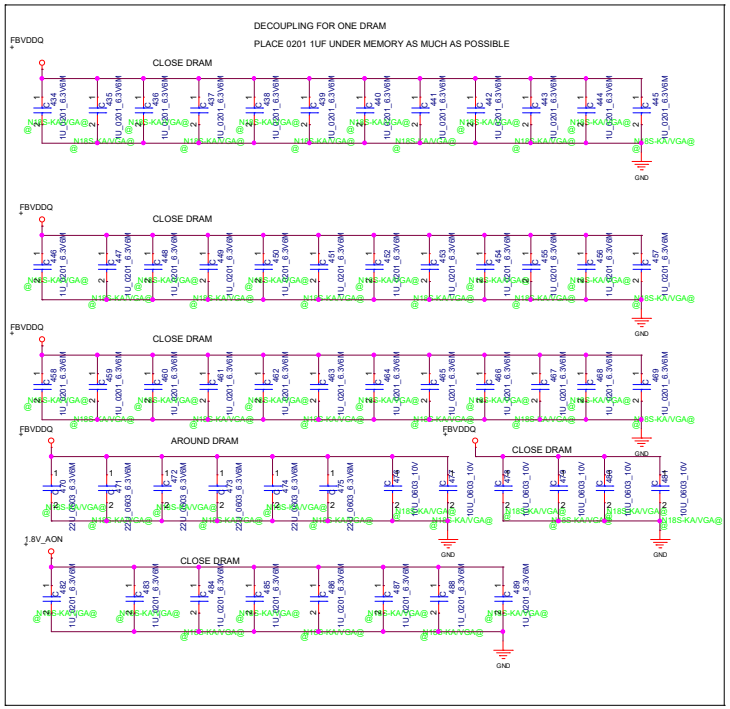
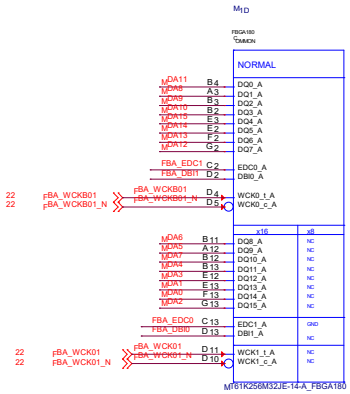
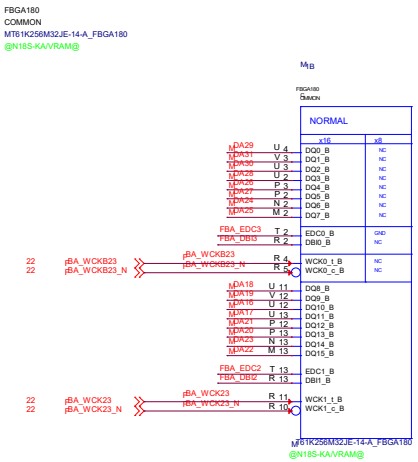
MEMORY: FBA Partition 31..0

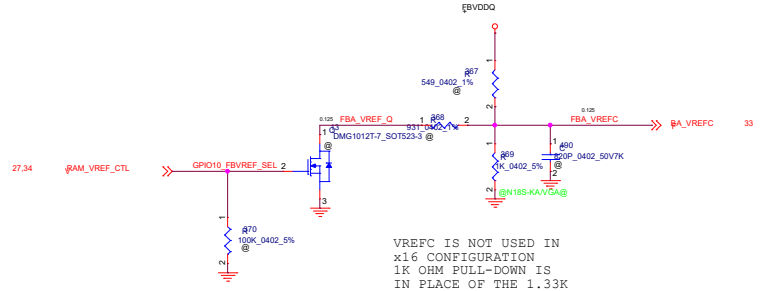












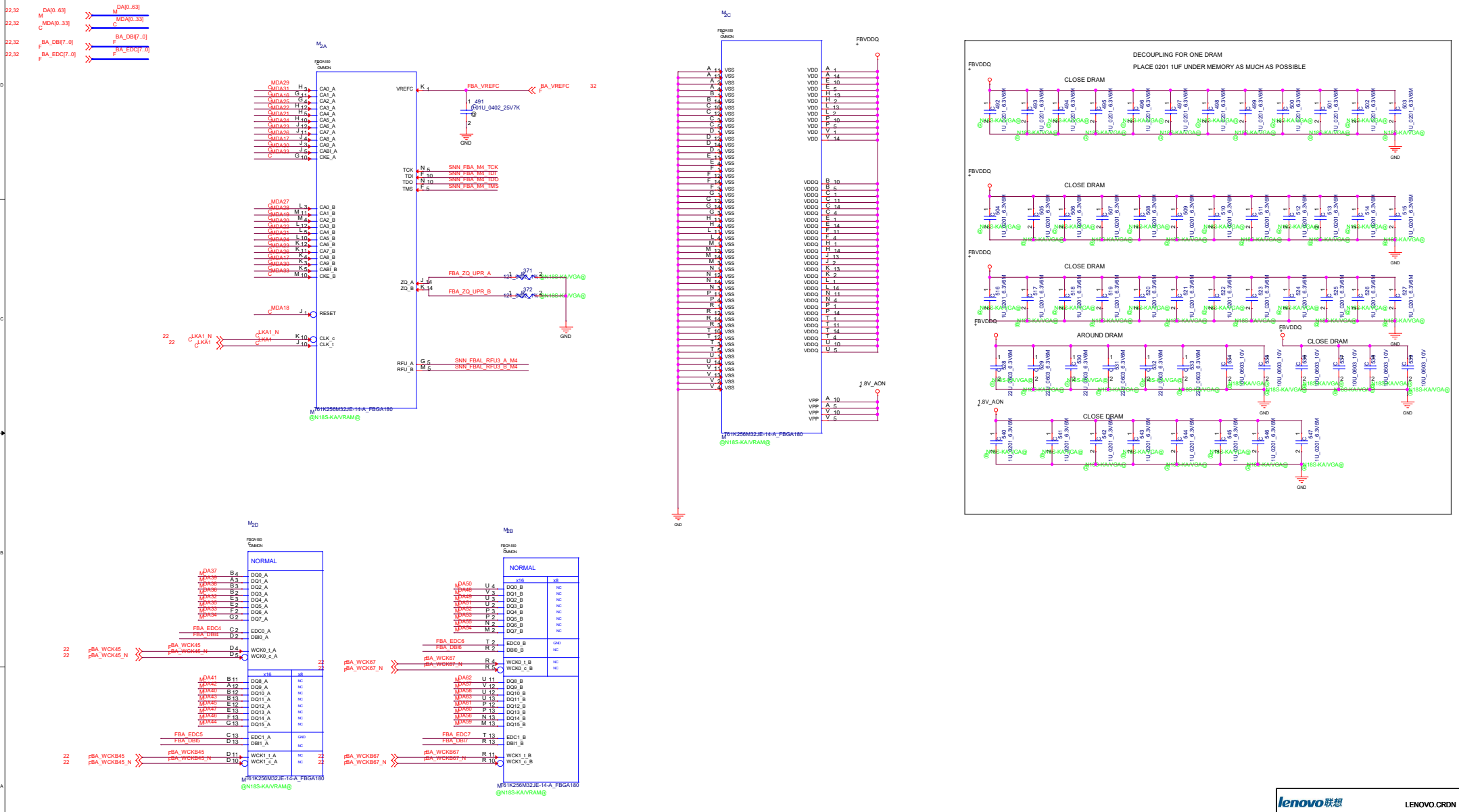
lenovo联想 LENOVO.CRDN

Title: GPU VRAM B

Size: custom | Document Number: S/50 | Rev: 0.1

Date: Friday, August 07, 2020 | Sheet: 32 of 66

MEMORY: FBA Partition 63..32



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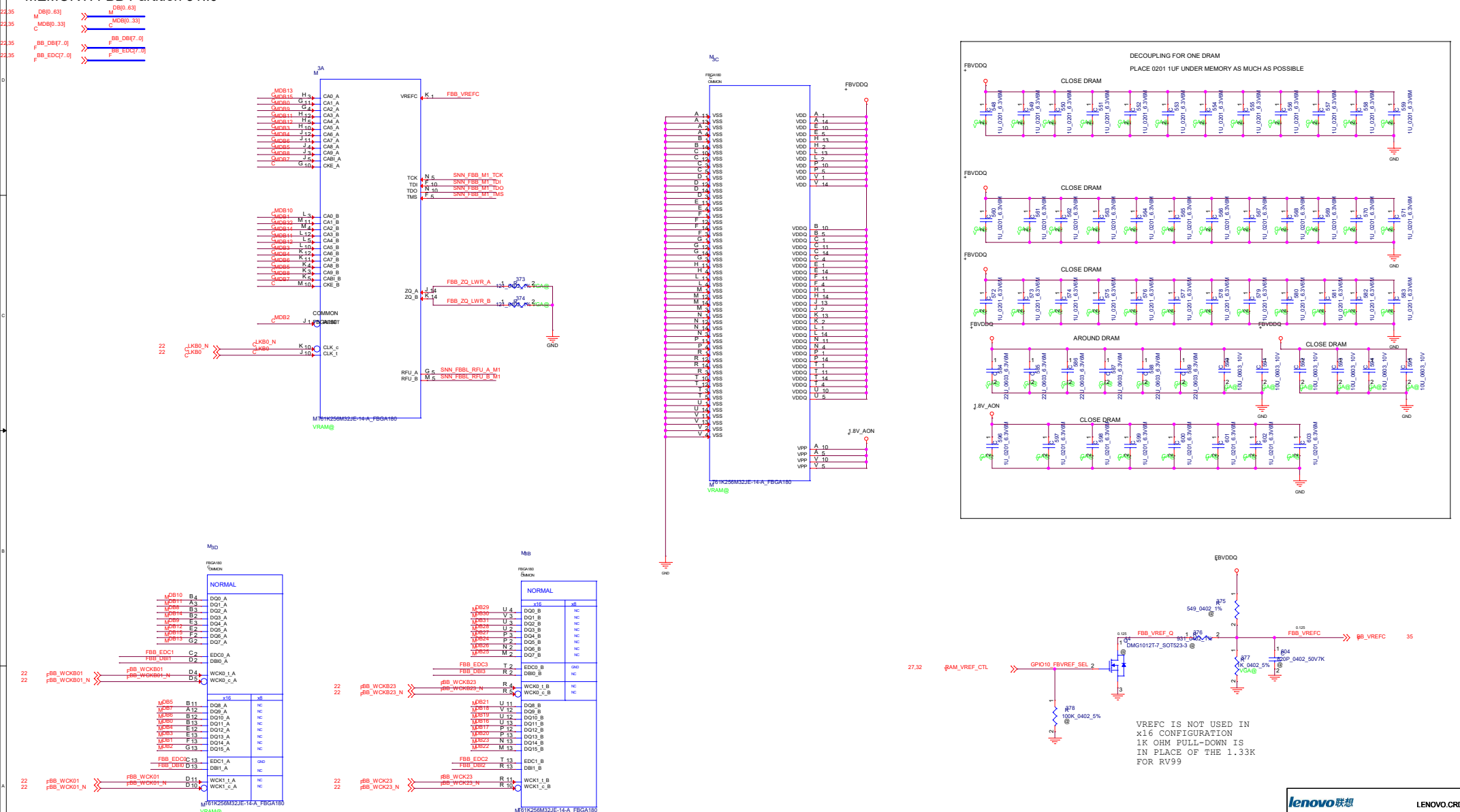
Title: GPU VRAM A

Size: custom | Document Number: S/50 | Rev: 0.1

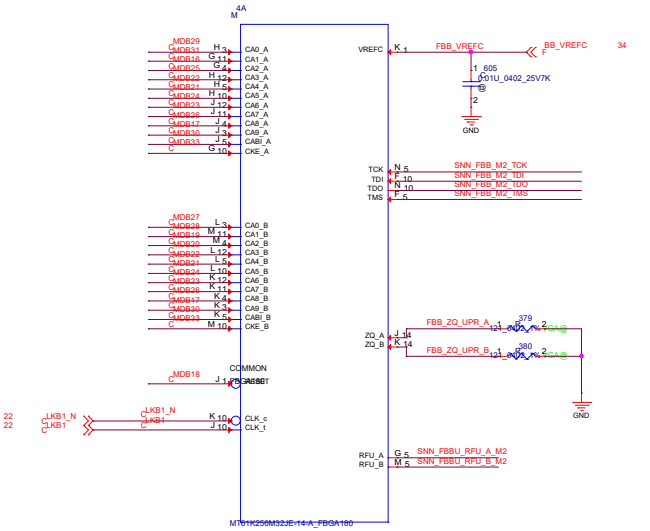
Date: Friday, August 07, 2020 | Sheet 33 of 66

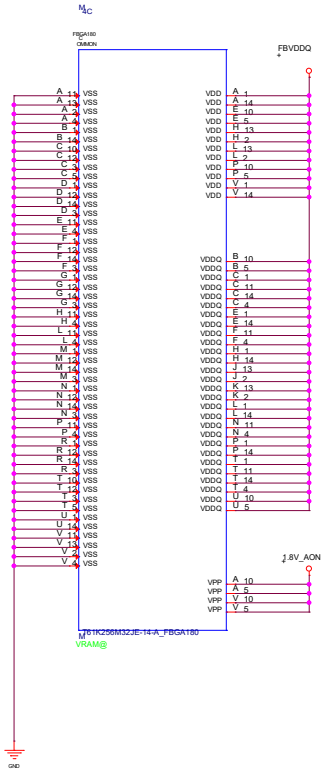
MEMORY: FBB Partition 31..0

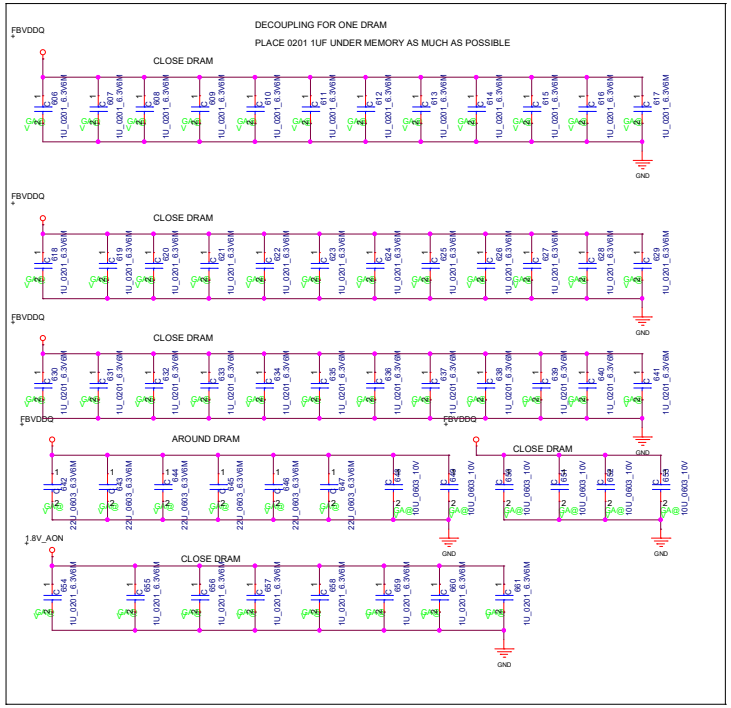


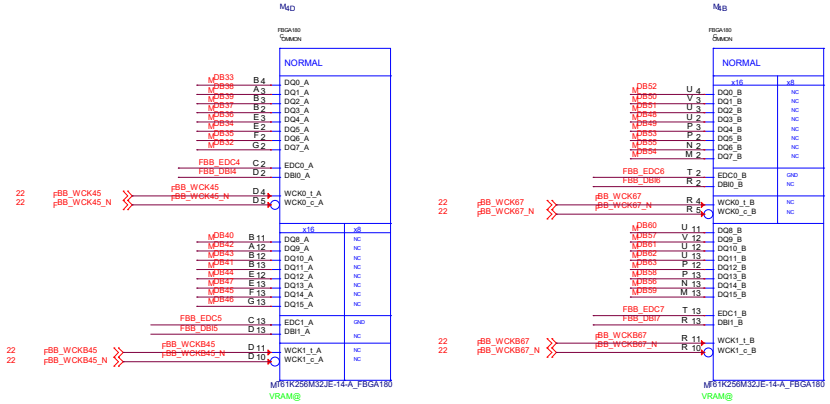
Title	GPU VRAM B
Size	Document Number: 5750
Rev	0.1
Date:	Friday, August 07, 2020
Sheet	34 of 66

MEMORY: FBB Partition 63..32









Place DRAM on TOP with PIN A1 Toward GPU

lenovo联想	LENOVO.CRDN
Title	GPU VRAM A
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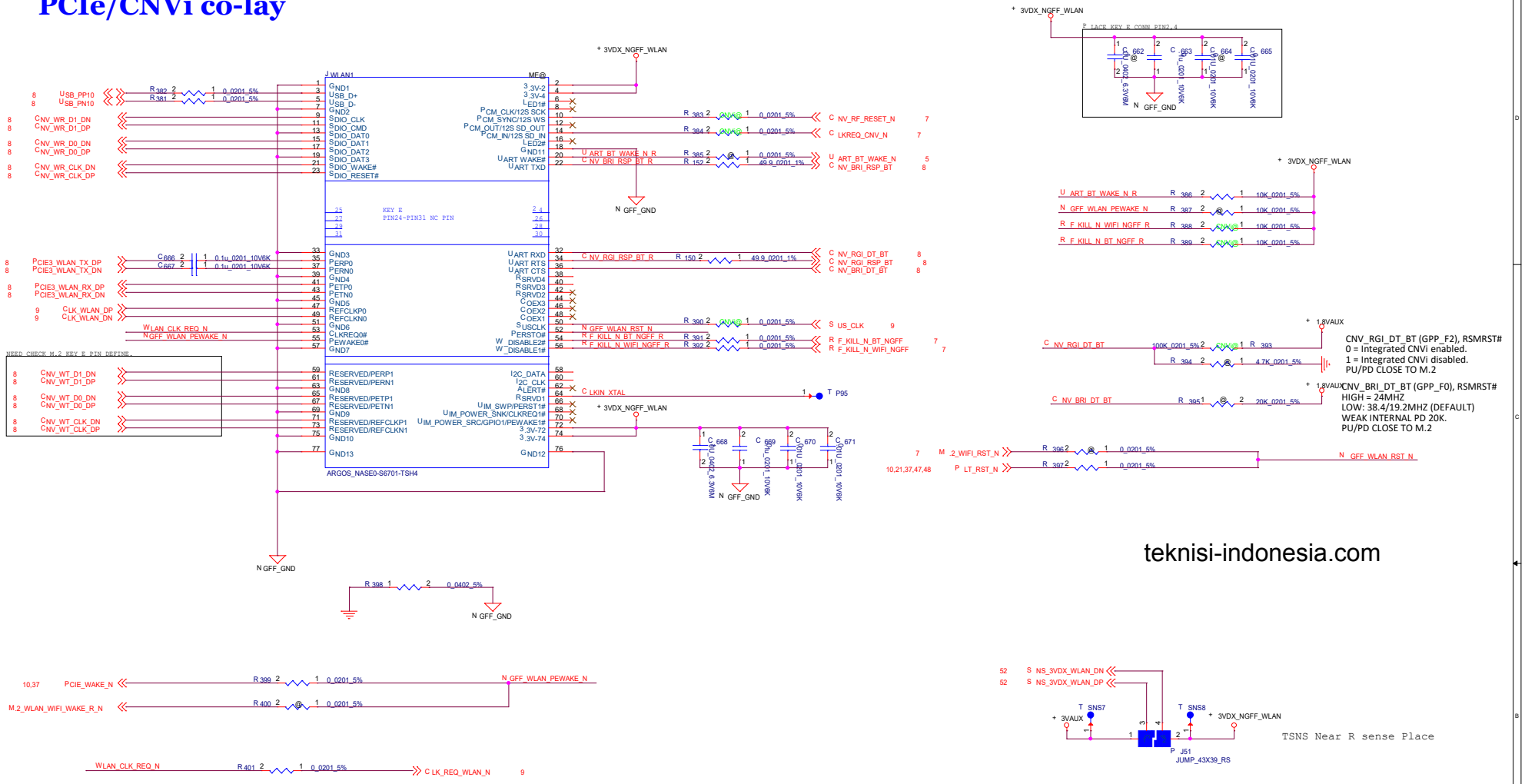
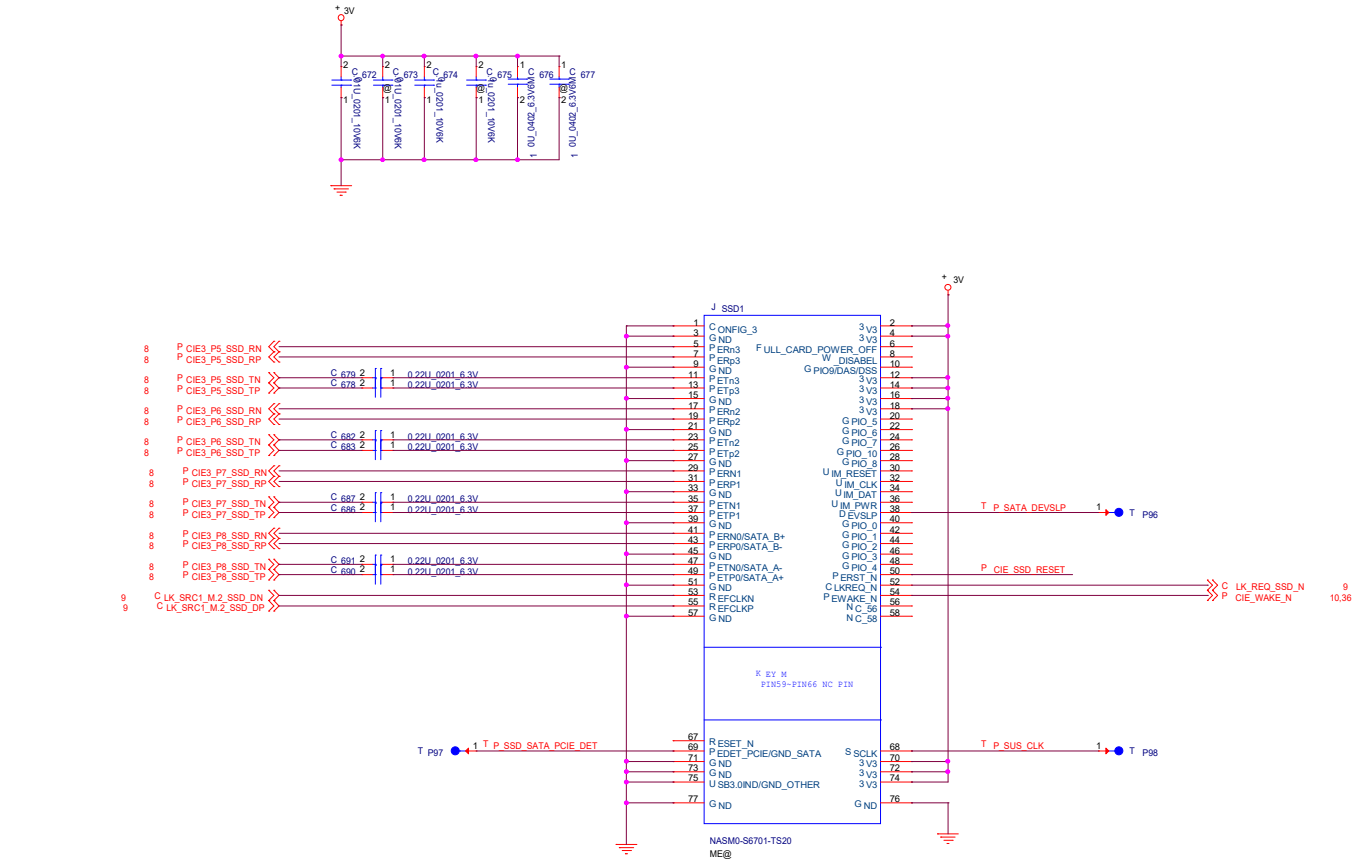
PCIe/CNVi co-lay



lenovo联想	LENOVO.CRDN
Title	N GFF WLAN
Size: C	Document Number: S 750
Rev: 0.5	
Date: Friday, August 07, 2020	Sheet 3 6 of 66



lenovo联想	LENOVO.CRDN
Title	N GFF SSD
Size C	Document Number S 750
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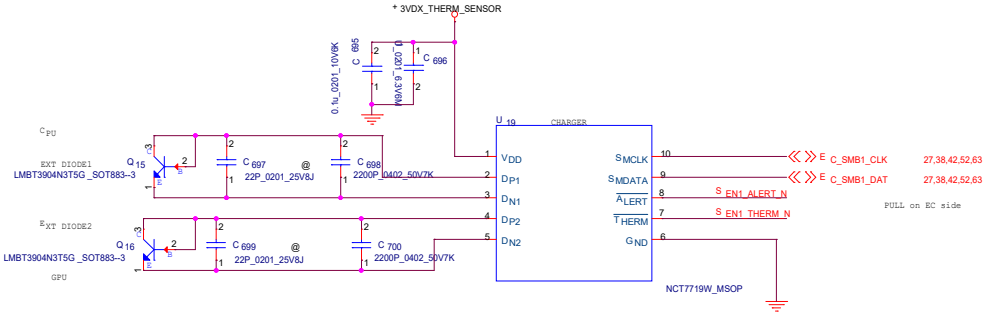
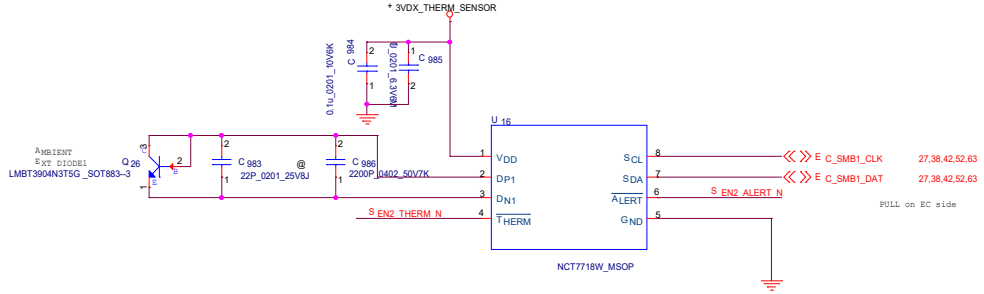
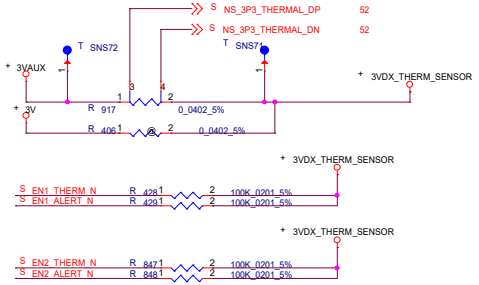
Date:	Friday, August 07, 2020
Sheet	37 of 66

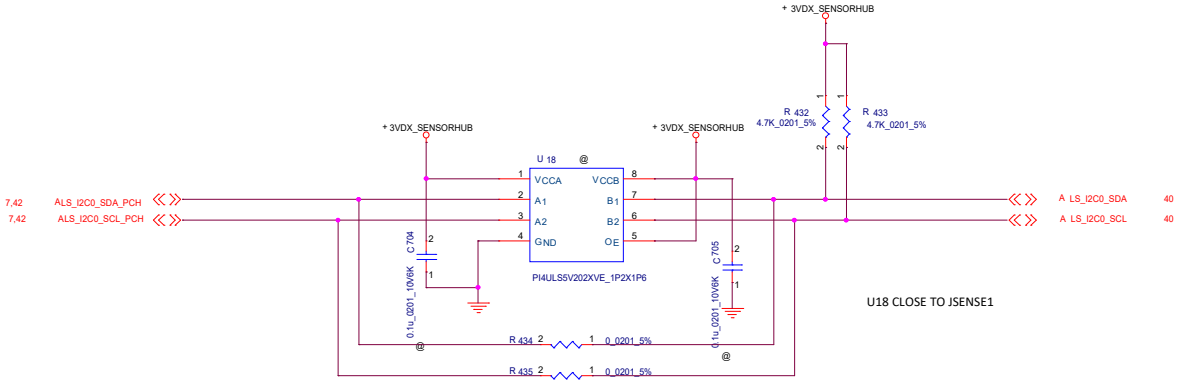


SMBus ADDRESS:0x9A



SMBus ADDRESS:0x98





lenovo联想	LENOVO.CRDN
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Size C	Document Number S 750
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Date:	Friday, August 07, 2020
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lenovo联想

LENOVO.CRDN

Title

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Size	Document Number	Rev
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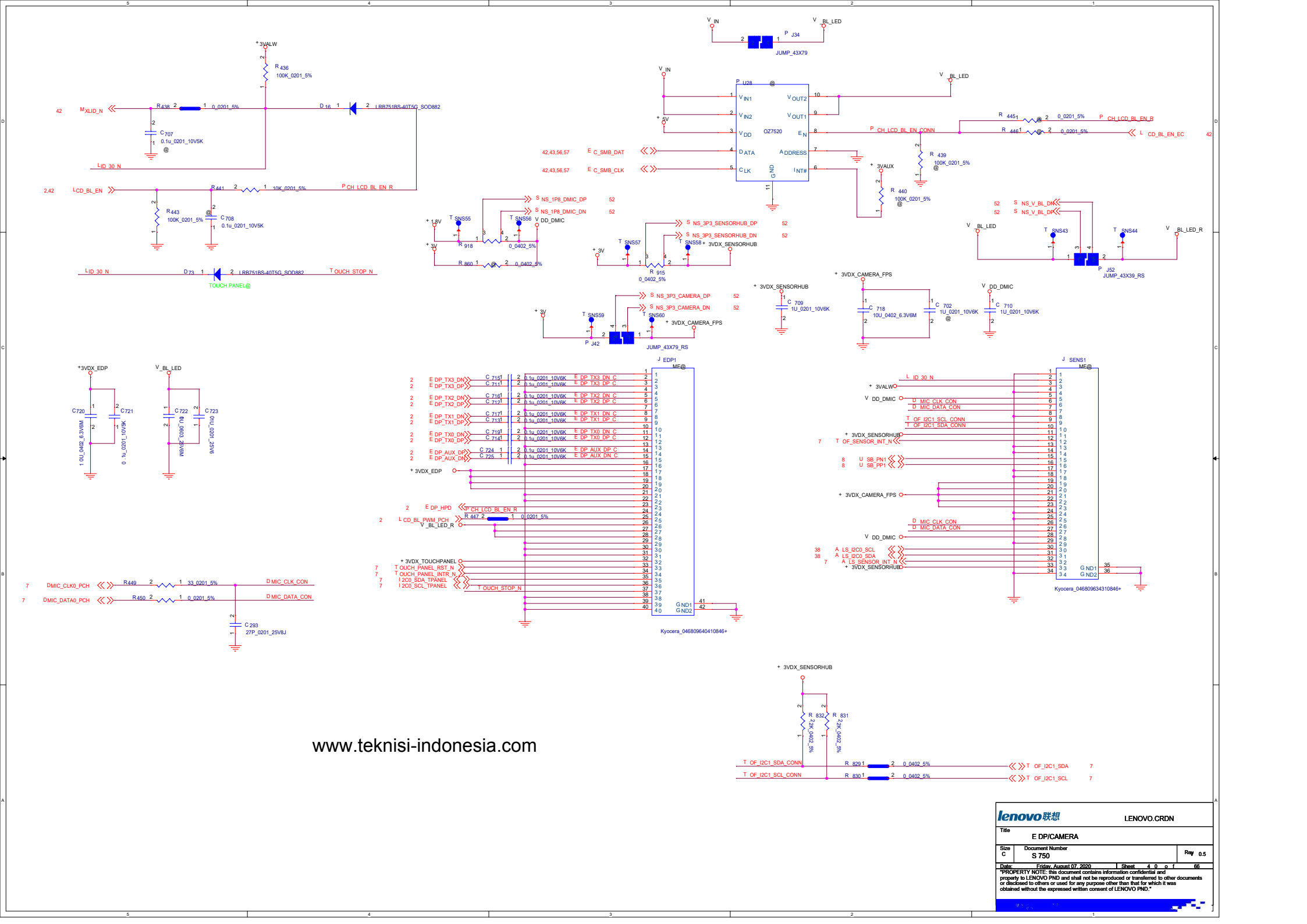

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Title: E DP/CAMERA

Size	Document Number	Rev
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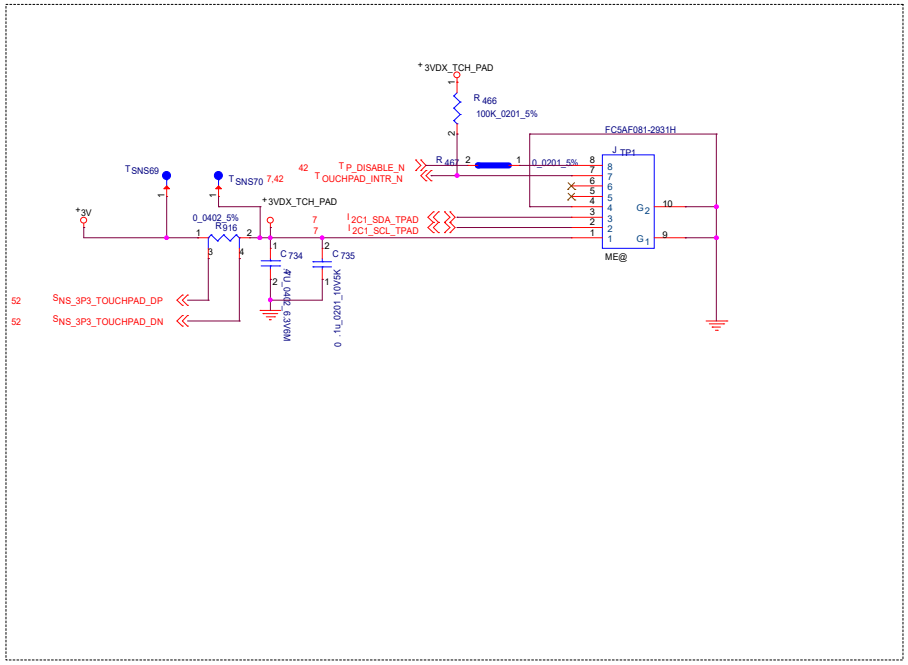
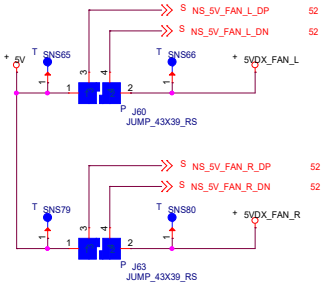
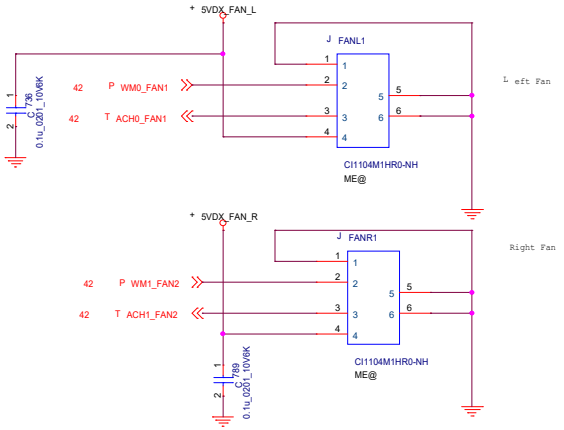
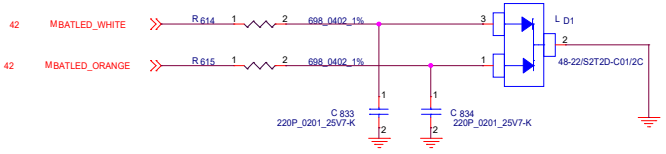
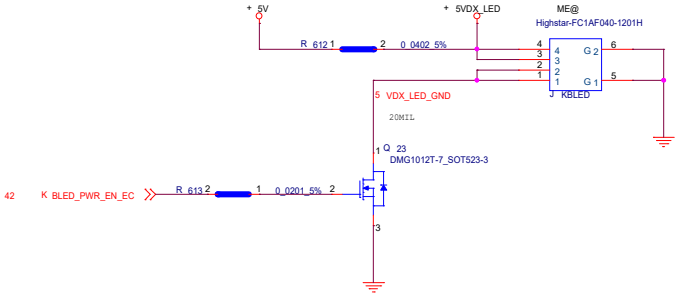
Date: Friday, August 07, 2020 Sheet 40 of 66











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Title: T P/FAN/KB LED

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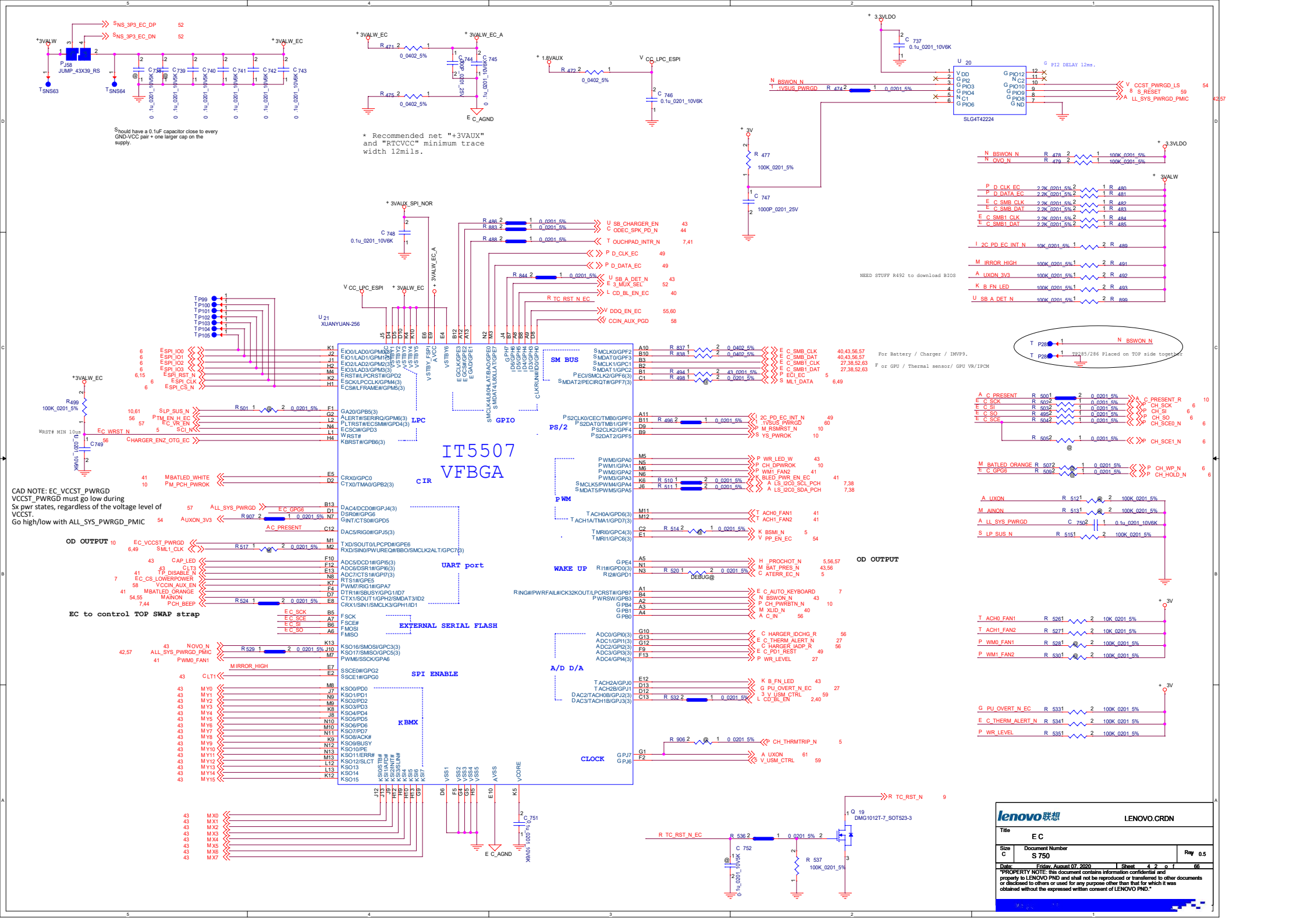
IT5507
VFBGA
LPC
GPIO
SM BUS
PS/2
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
OD OUTPUT
EC to control TOP SWAP strap
CAD NOTE: EC_VCCST_PWRGD
VCCST_PWRGD must go low during
Sx pwr states, regardless of the voltage level of
VCCST.
Go high/low with ALL_SYS_PWRGD_PMIC
* Recommended net "+3VAUX" and "RTCVCC" minimum trace width 12mils.
Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.
NEED STUFF R492 to download BIOS
For Battery / Charger / IMVP9.
For GPU / Thermal sensor/ GPU VR/IPCM
TP285/286 Placed on TOP side together
DEBUG@
SLG4T42224
XUANYUAN-256
LENOVO.CRDN
Title
EC
Size C
Document Number S 750
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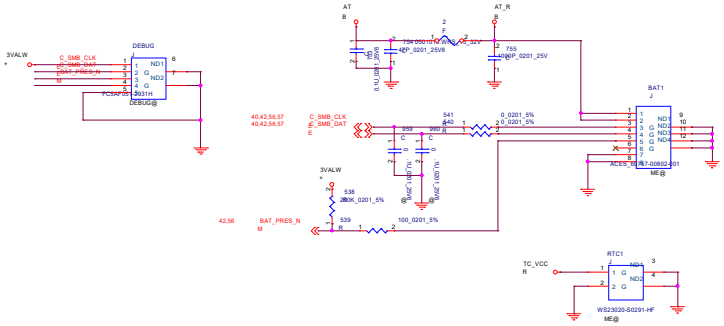
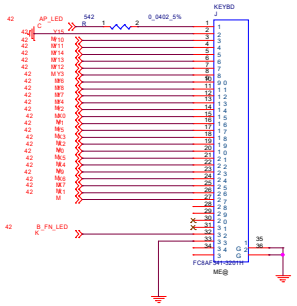
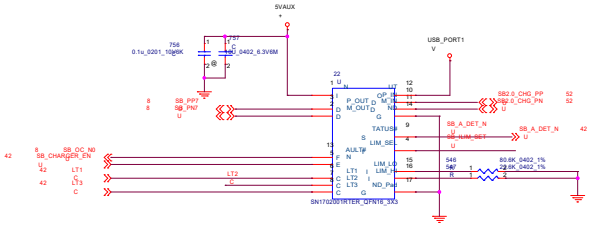
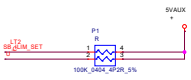




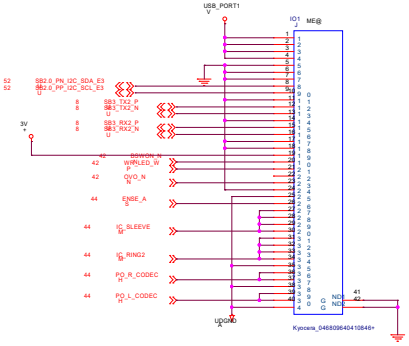
KB PIN DEFINE TBD





Install ILIM_SEL shunt for ILIM = ILIM_LO = 0.63A
Remove ILIM_SEL shunt for ILIM =ILIM_HI = 2.3A
Support Mouse/Keyboard wake up.
Support Power Wake

CLT1	CLT3	
1	0	-- SDP
0	1	-- DCP/Auto
1	1	-- CDP



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Title:	CONNECTOR	
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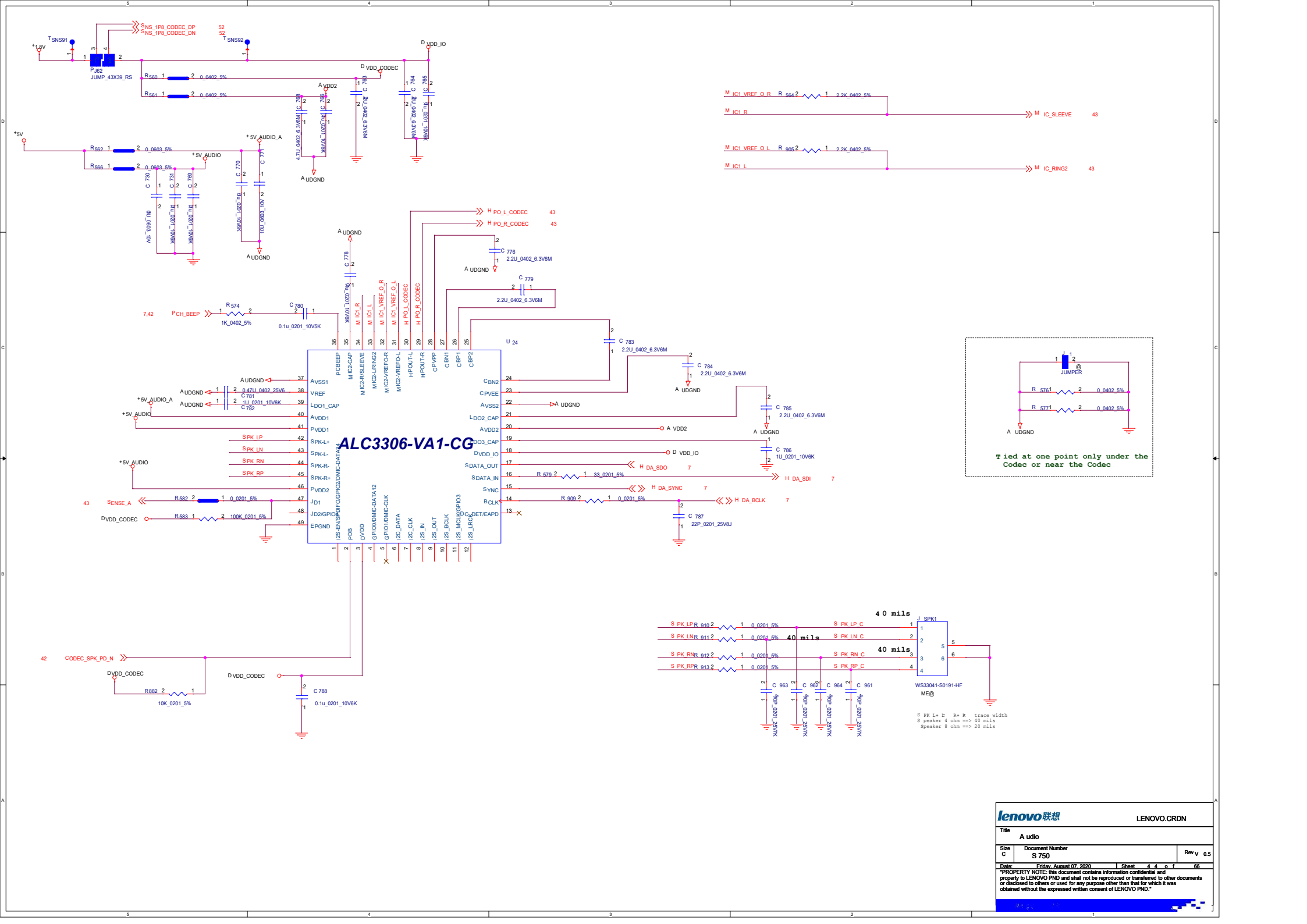
Date: Friday, August 07, 2020	Sheet 3 4 1 o	BS


ALC3306-VA1-CG
Tied at one point only under the Codec or near the Codec
40 mils
40 mils
40 mils
LENOVO.CRDN
Title
A udio
Size C
Document Number S 750
Rev V 0.5
Date: Friday, August 07, 2020
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Title

B LANK

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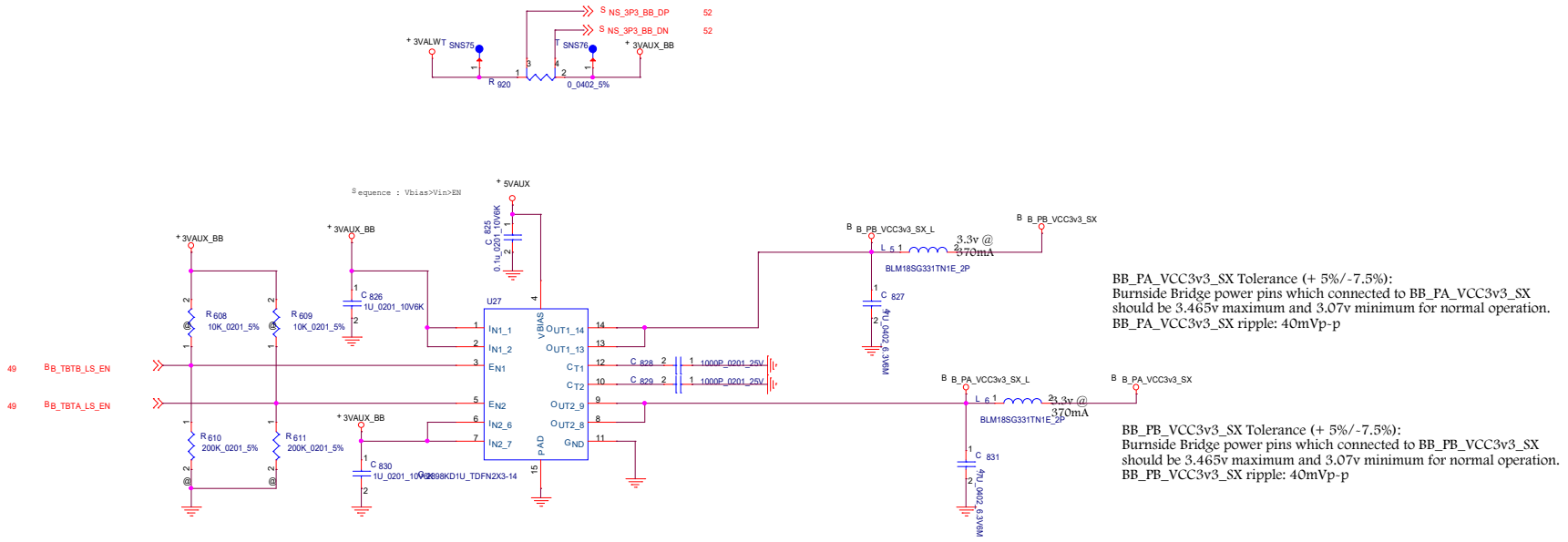

BB_PA_VCC3v3_SX Tolerance (+ 5%/-7.5%):
Burnside Bridge power pins which connected to BB_PA_VCC3v3_SX should be 3.465v maximum and 3.07v minimum for normal operation.
BB_PA_VCC3v3_SX ripple: 40mVp-p

BB_PB_VCC3v3_SX Tolerance (+ 5%/-7.5%):
Burnside Bridge power pins which connected to BB_PB_VCC3v3_SX should be 3.465v maximum and 3.07v minimum for normal operation.
BB_PB_VCC3v3_SX ripple: 40mVp-p

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Title: B BPOWSWITCH

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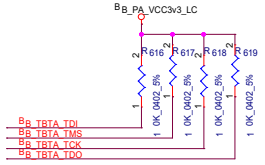
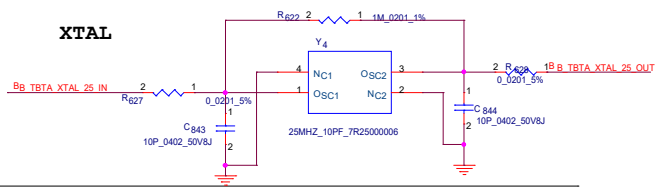
Burnside Bridge for TBT Port A

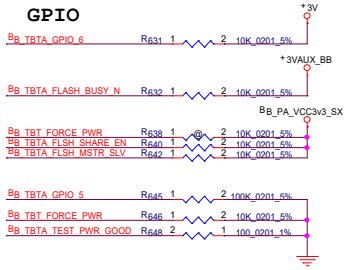
JTAG



XTAL



GPIO



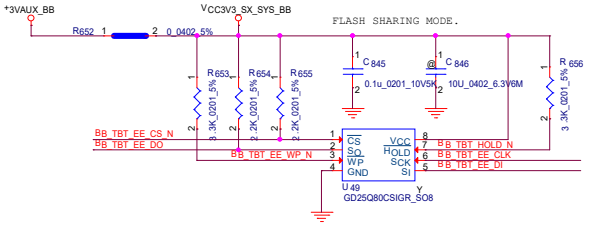
BB_FORCE_PWR:
Connect to EC/PCH for FW update
'0' - by default
'1' - for debug only

FLASH_BUSY#:
If Flash sharing is being used, PU should be used.
If Flash sharing isn't being used, PD should be used.

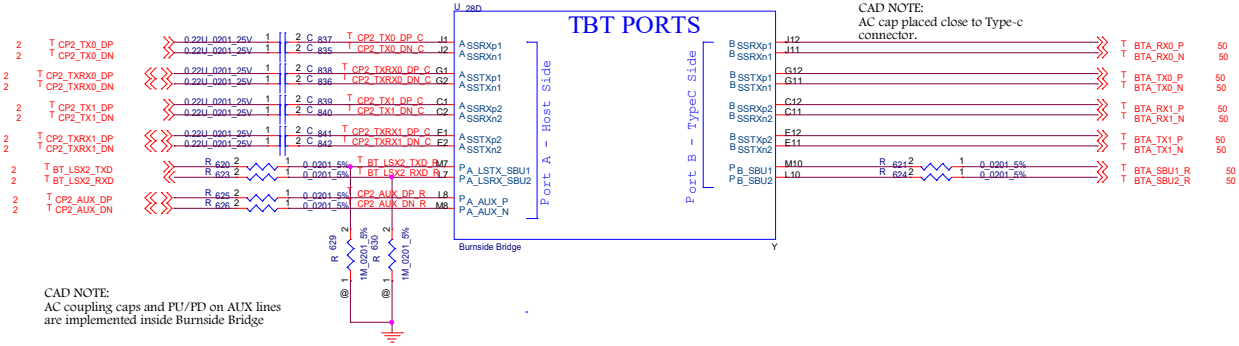
FLSH_SHARE_EN:
'0' - Flash isn't shared. 1 Flash per Re-timer
'1' - Flash is shared between 2 Re-timers

FLSH_MSTR_SLV:
'0' - Set Re-timer to be Slave on shared flash SPI I/F.
'1' - Set Re-timer to be Master on shared flash SPI I/F
If shared, BB1 PU as master, BB2 PD as slave.

ROM

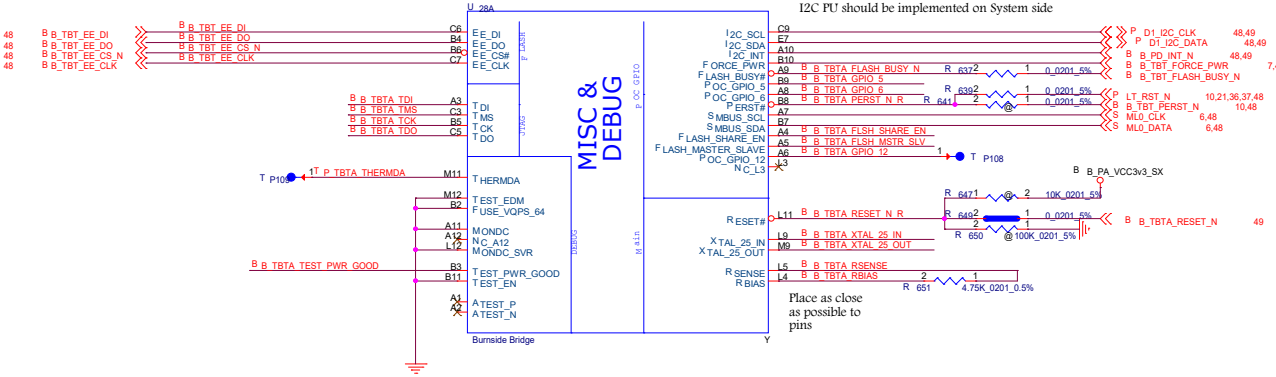


TBT PORTS



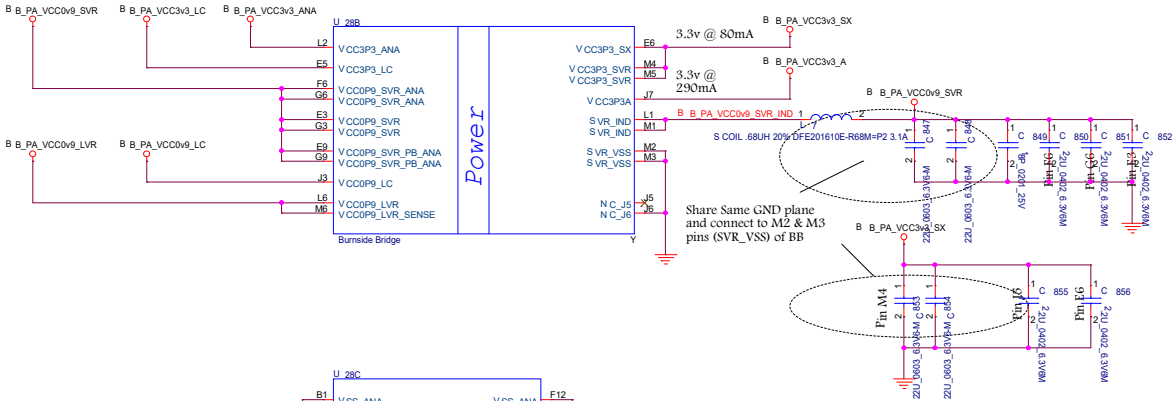
CAD NOTE:
AC cap placed close to Type-c connector.

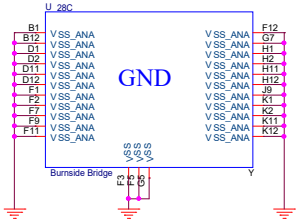
CAD NOTE:
AC coupling caps and PU/PD on AUX lines are implemented inside Burnside Bridge

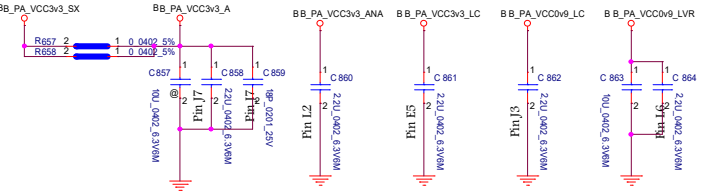


I2C PU should be implemented on System side

Place as close as possible to pins







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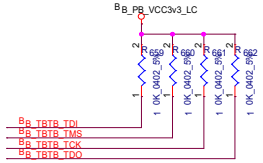
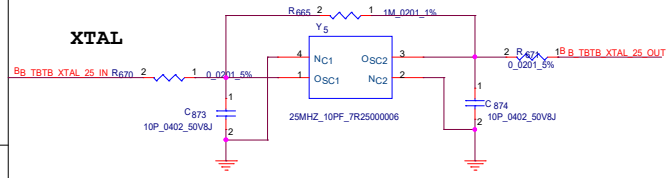
Burnside Bridge for TBT Port B

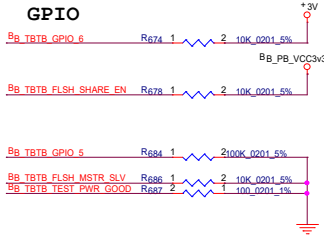
JTAG



XTAL



GPIO



BB_FORCE_PWR:
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'0' - by default
'1' - for debug only

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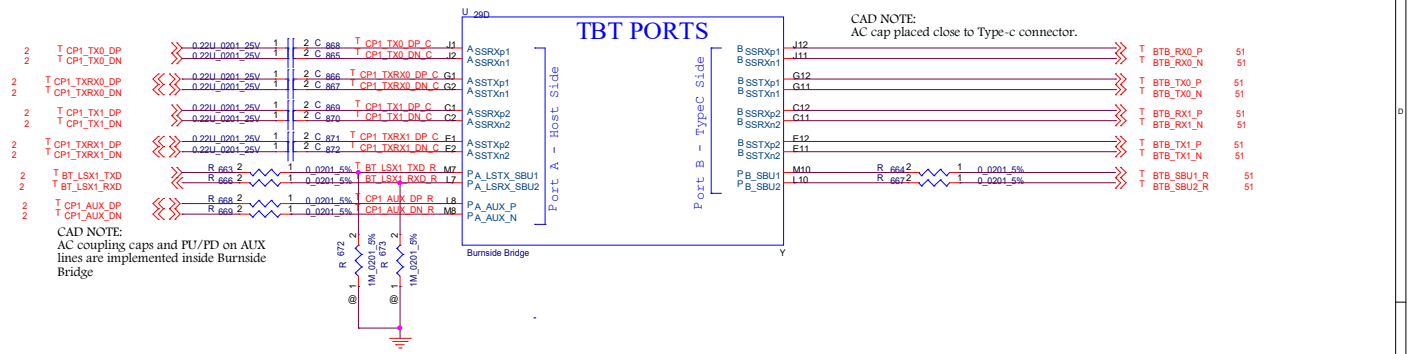
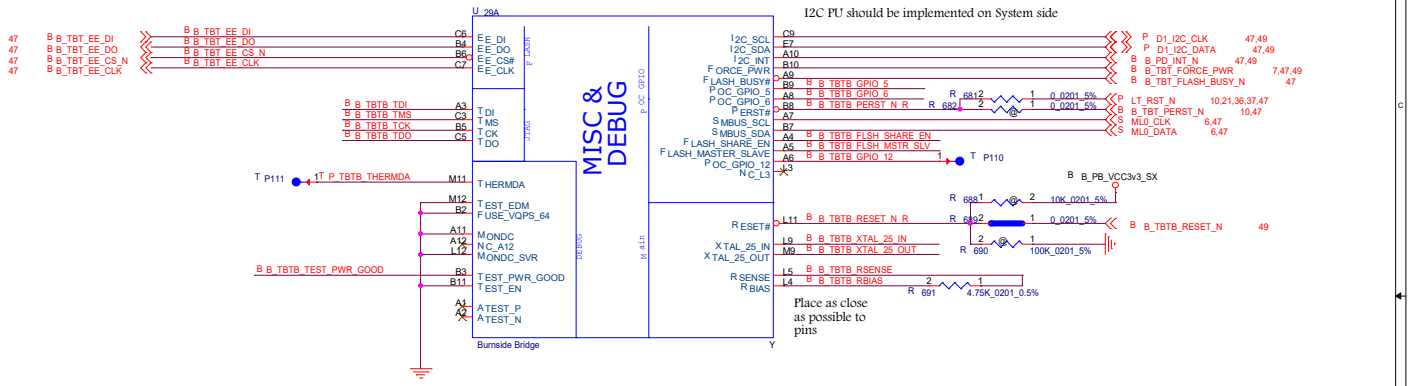
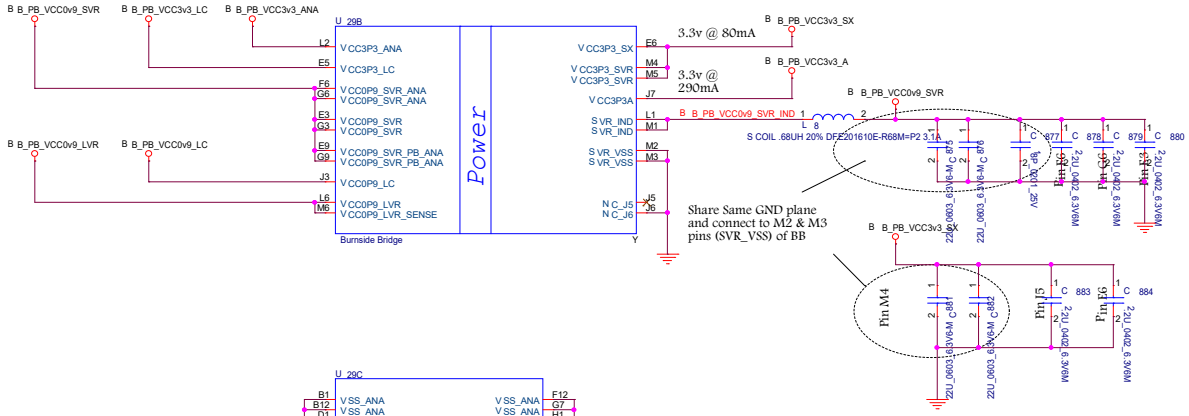
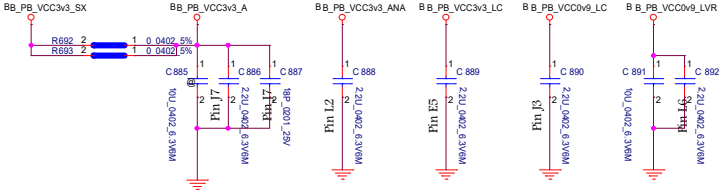
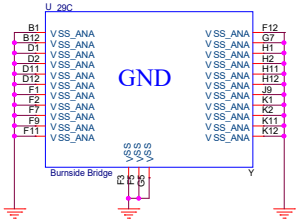
FLSH_MSTR_SLV:
'0' - Set Re-timer to be Slave on shared flash SPI I/F.
'1' - Set Re-timer to be Master on shared flash SPI I/F
If shared, BB1 PU as master, BB2 PD as slave.











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Title: T BT_BB_PORT B

Size: C | Document Number: S 750 | Rev: 0.5

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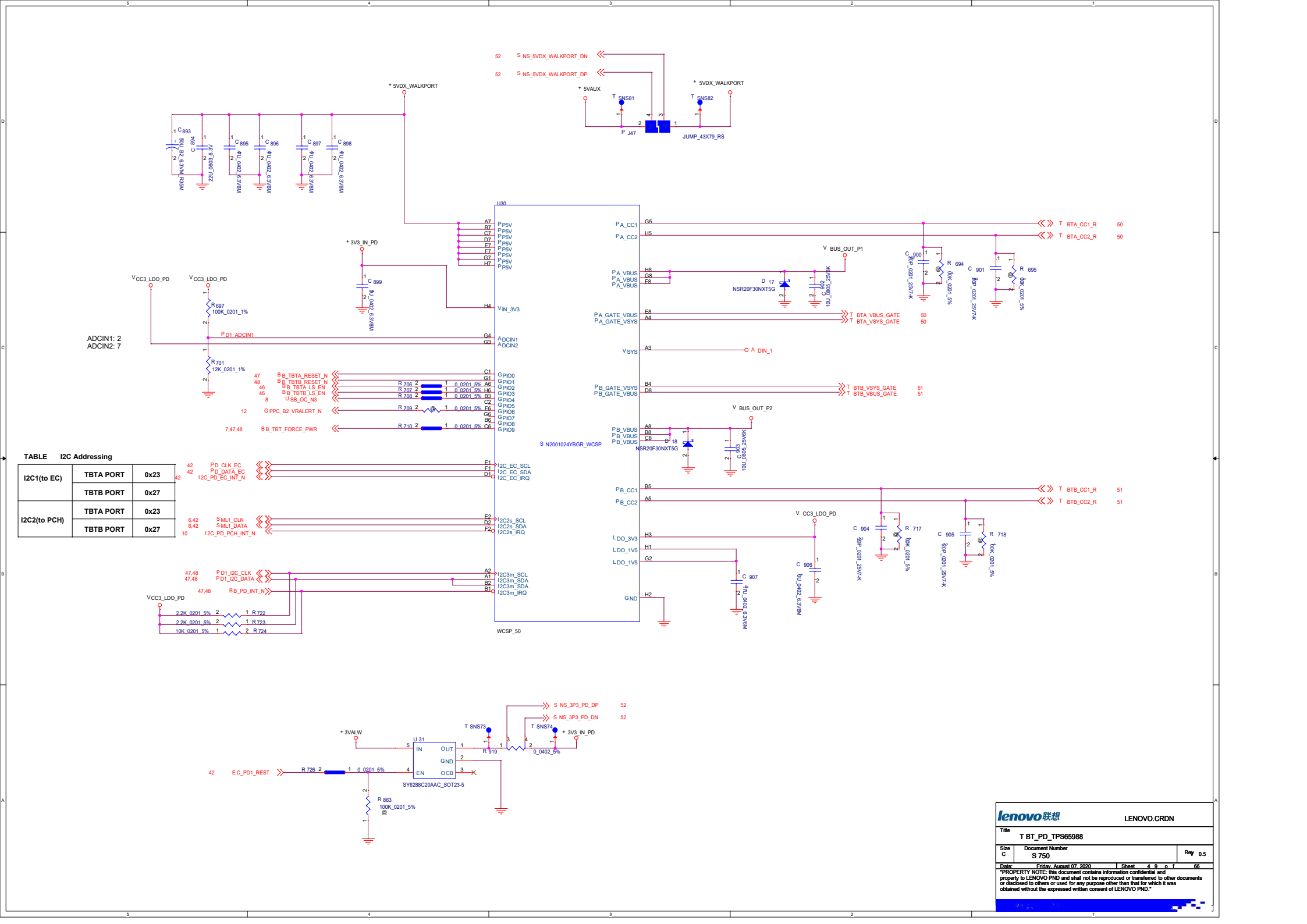

TABLE I2C Addressing

I2C1(to EC)	TBTA PORT	0x23
	TBTB PORT	0x27
I2C2(to PCH)	TBTA PORT	0x23
	TBTB PORT	0x27

Title	T BT_PD_TPS65988
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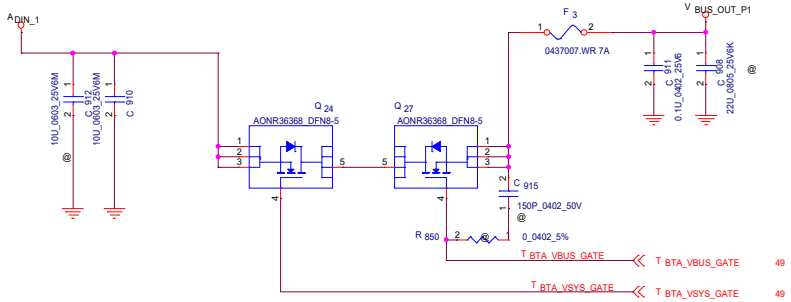
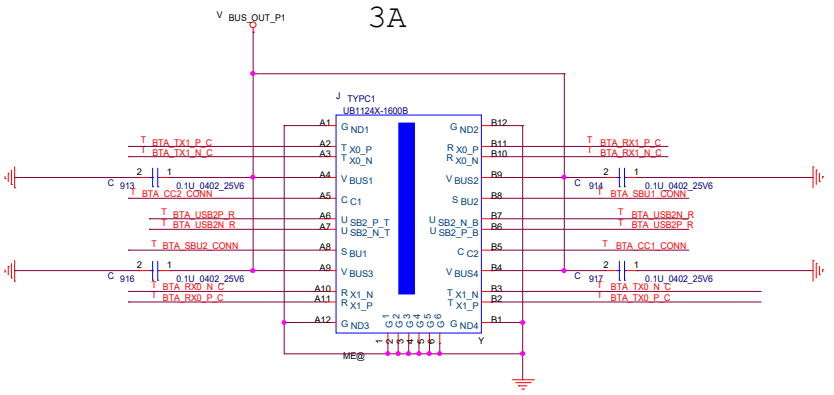
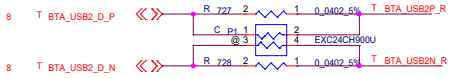
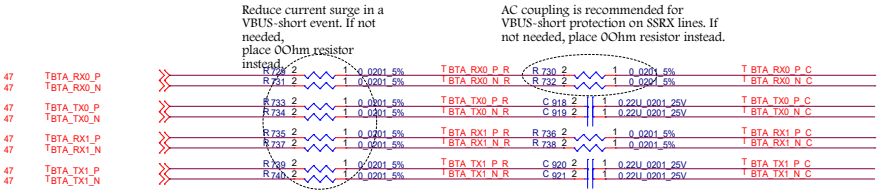
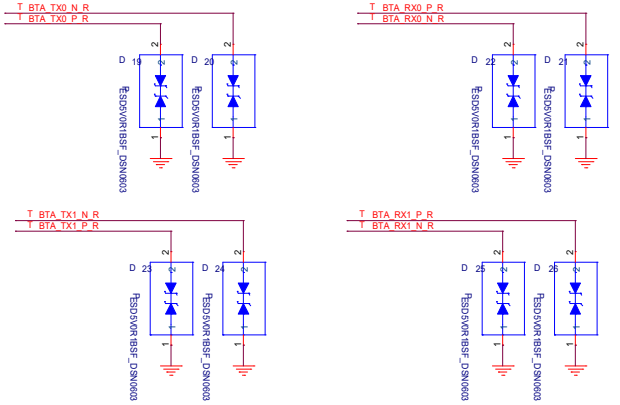
TBT A PORT VBUS SWITCH

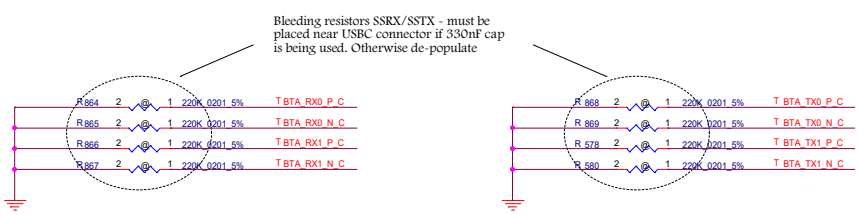


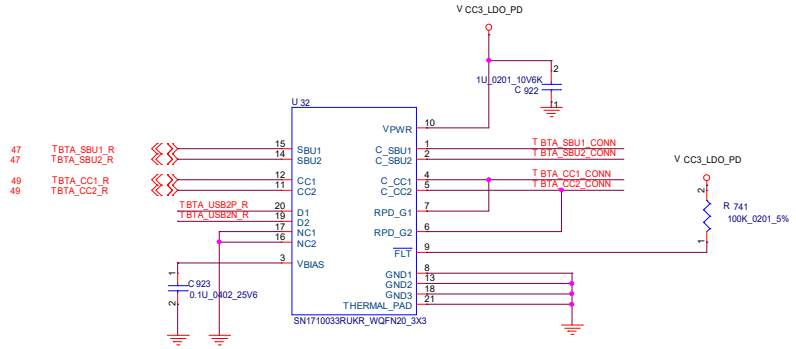












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Title	TYPEC_PORTA		
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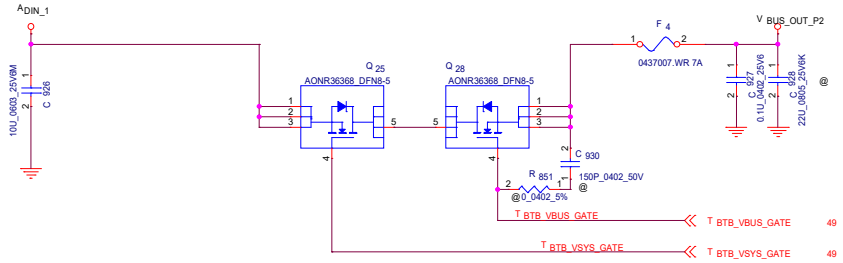
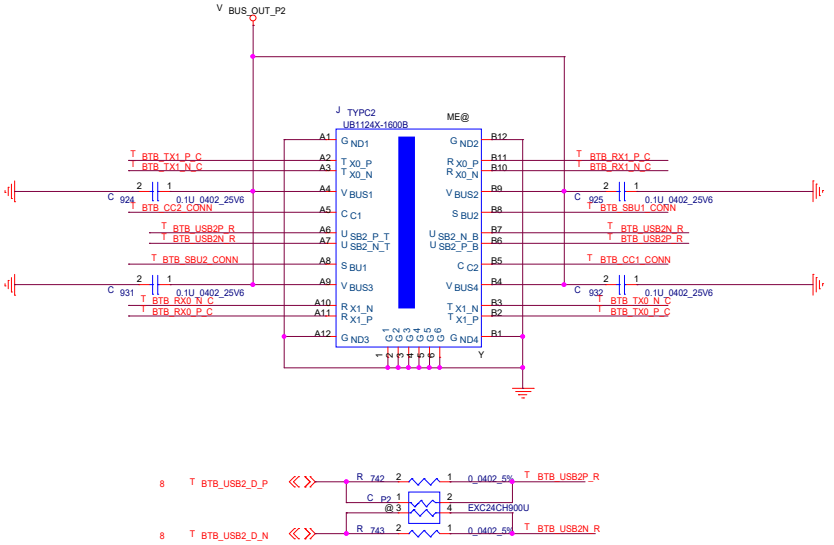
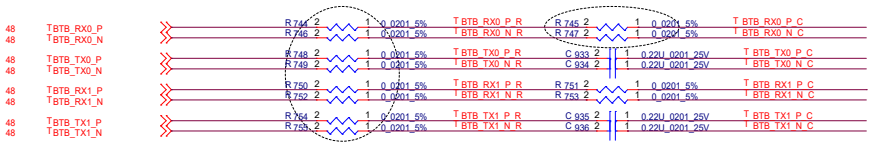
TBT B PORT VBUS SWITCH



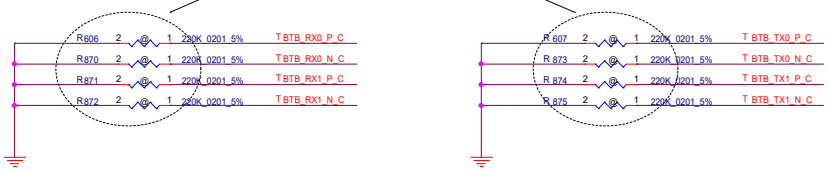


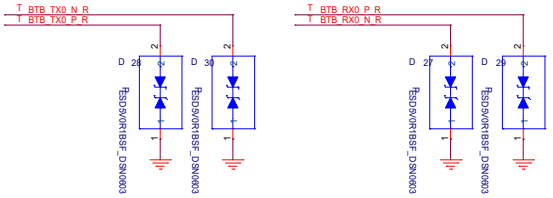
Reduce current surge in a VBUS-short event. If not needed, place 0Ohm resistor instead.

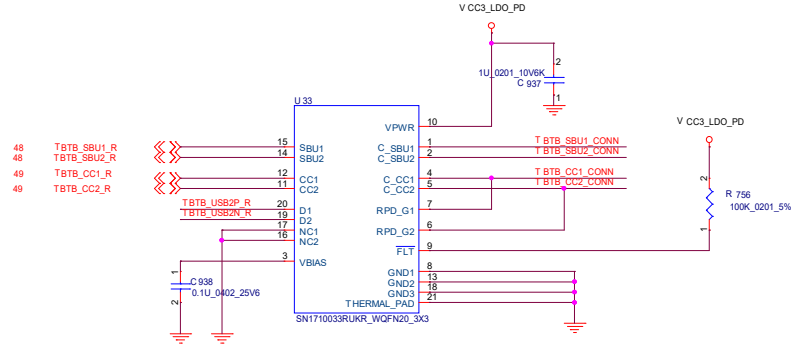
AC coupling is recommended for VBUS-short protection on SSRX lines. If not needed, place 0Ohm resistor instead.



Bleeding resistors SSRX/SSTX - must be placed near USBC connector if 330nF cap is being used. Otherwise de-populate







lenovo联想	LENOVO.CRDN	
Title: T YPEC_PORTB		
Size: C	Document Number: S 750	Rev: 0.5
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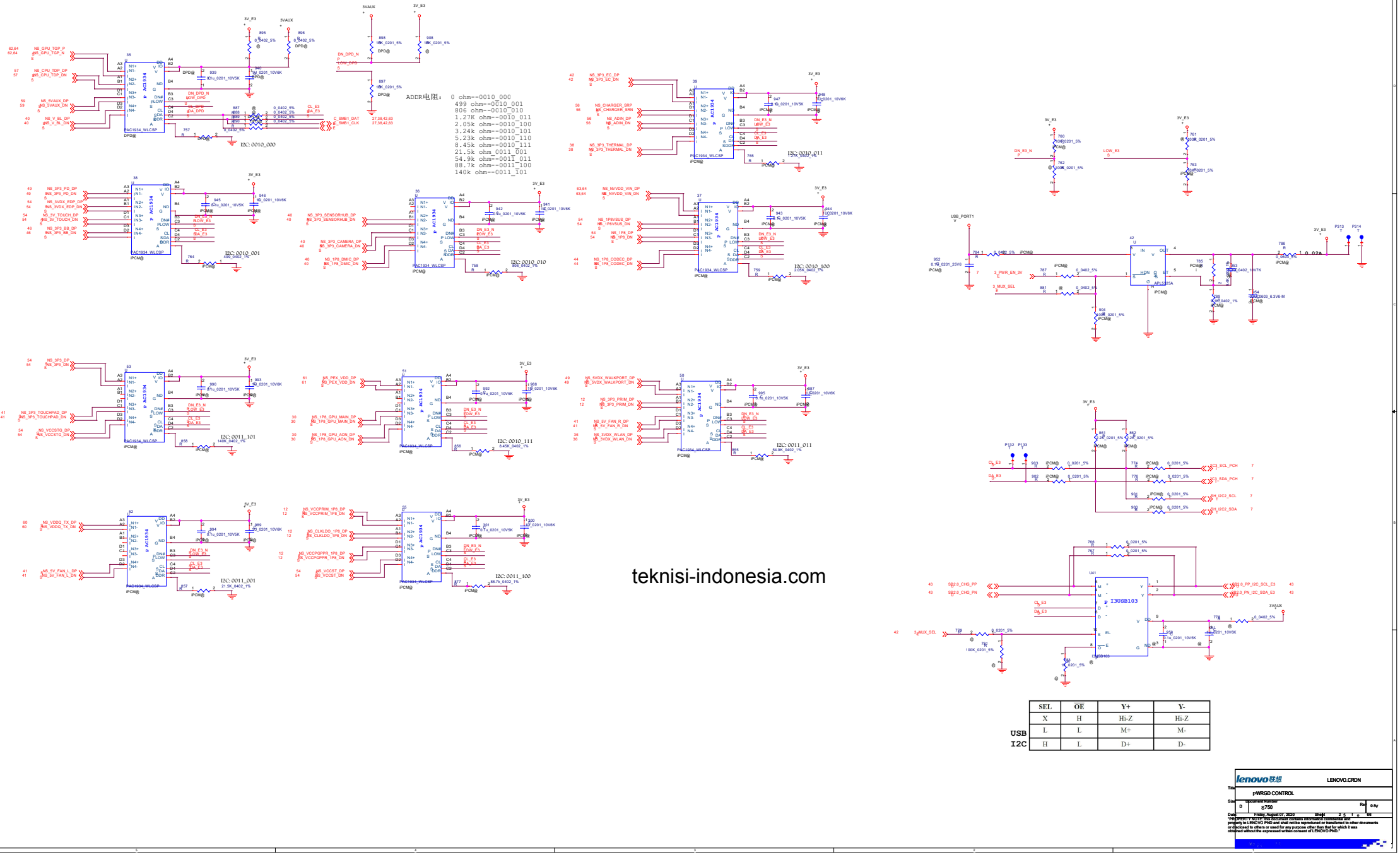

	SEL	$\overline{OE}$	Y+	Y-
USB	X	H	Hi-Z	Hi-Z
I2C	L	L	M+	M-
	H	L	D+	D-

Title	PWRGD CONTROL
Size	D
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Title

B LANK

Size	Document Number	Rev
C	S 750	1.0

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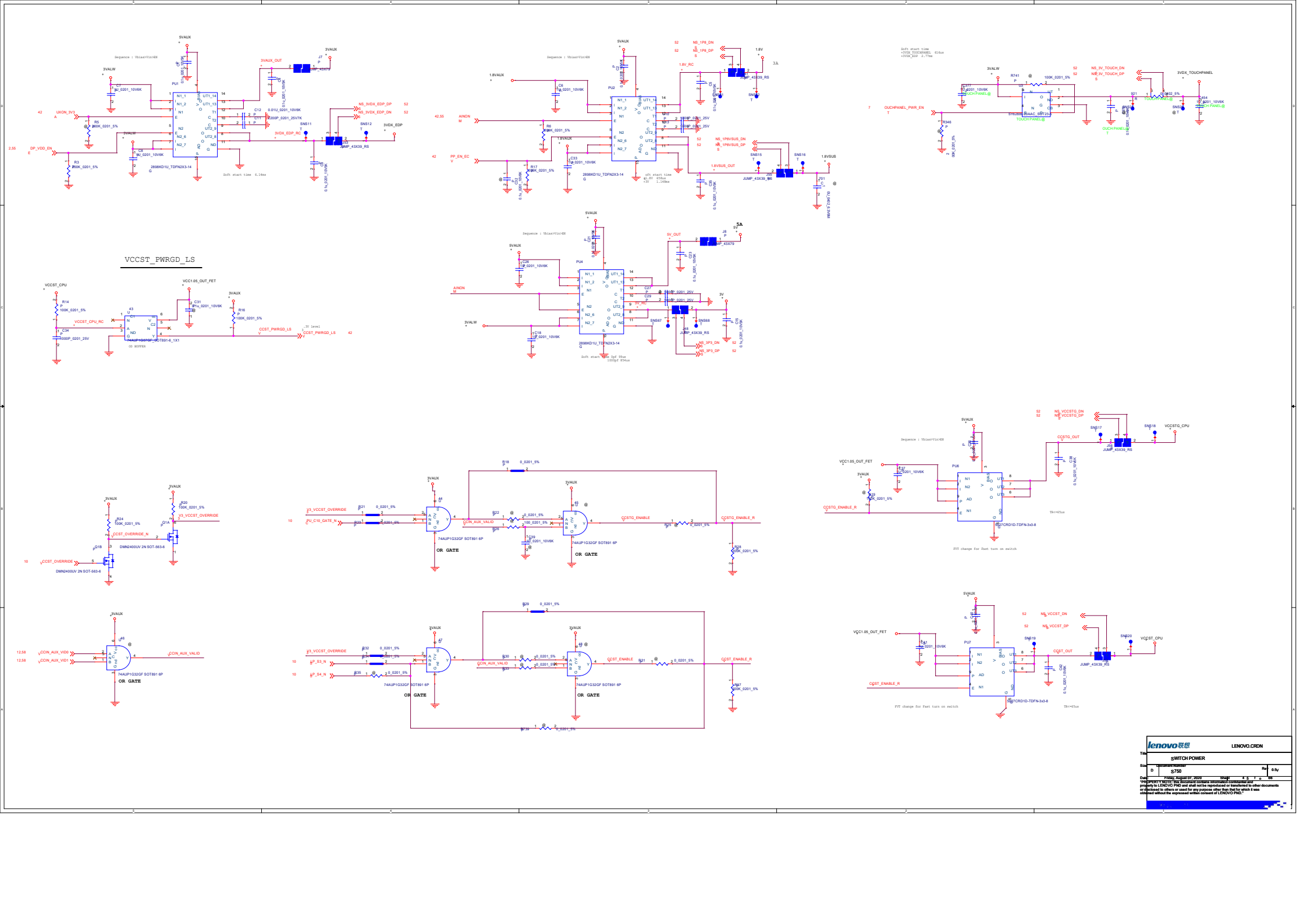
VCCST_PWRGD_LS
OR GATE
OR GATE
OR GATE
OR GATE
OR GATE
OR GATE
lenovo
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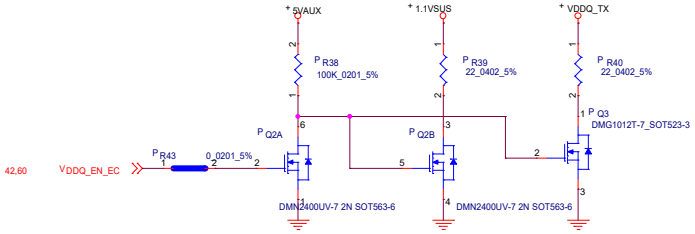
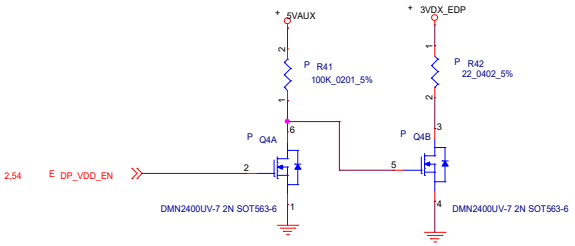
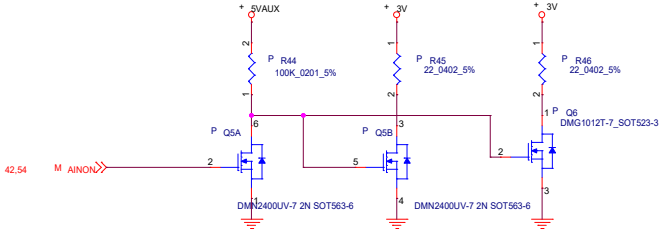
SWITCH POWER
S750
Friday, August 07, 2020
0.5y







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Title: D ISCHARGE

Size	Document Number	Rev
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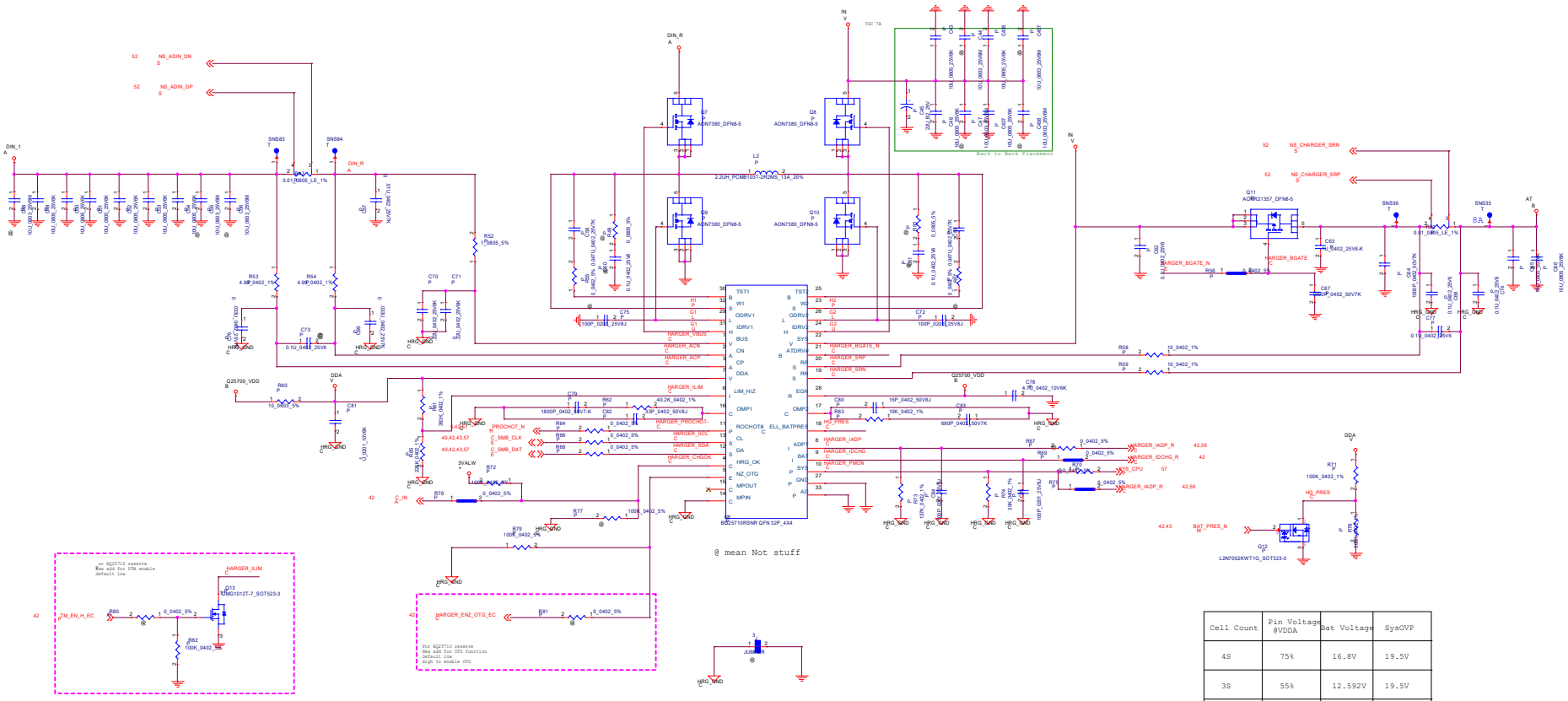

Cell Count	Pin Voltage @VDDA	Bat Voltage	SysOVP
4S	75%	16.8V	19.5V
3S	55%	12.592V	19.5V
2S	40%	8.4V	12V
1S	25%	4.192V	5V

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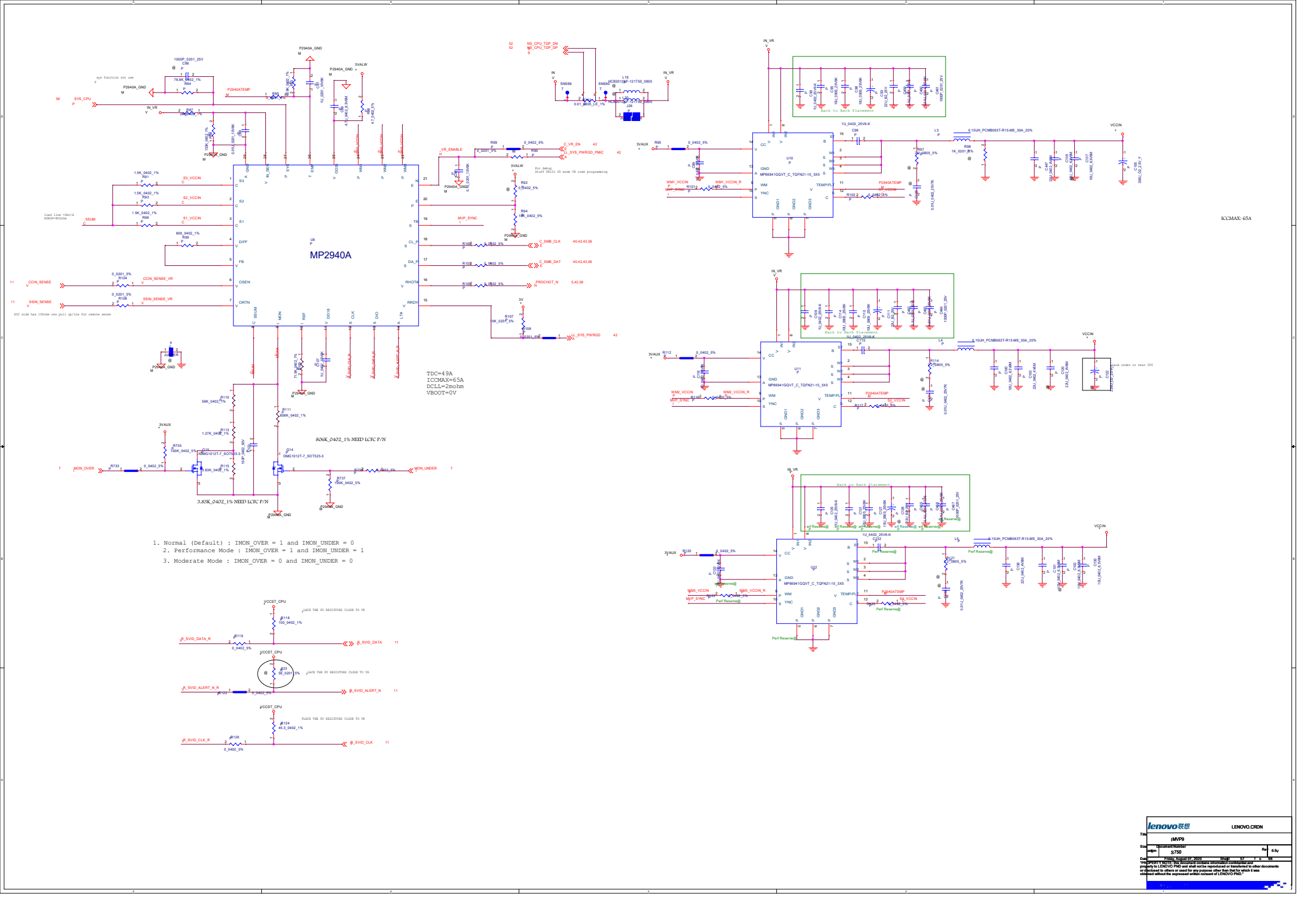
Title: NVDC CHARGER

Size: D | Document Number: S750 | Rev: 1.0

Date: Tuesday, August 11, 2020 | Sheet: 6 of 6


MP2940A
TDC=49A
ICCMAX=65A
DCLL=2mohm
VBOOT=0V
806K_0402_1% NEED LCFC P/N
3.83K_0402_1% NEED LCFC P/N
1. Normal (Default) : IMON_OVER = 1 and IMON_UNDER = 0
2. Performance Mode : IMON_OVER = 1 and IMON_UNDER = 0
3. Moderate Mode : IMON_OVER = 0 and IMON_UNDER = 0
ICCMAX: 65A
MP86941GQVT_C_TQFN21-15_5X5
MP86941GQVT_C_TQFN21-15_3X5
Back to Back Placement
Perf Reserve@
PLACE THE PU RESISTORS CLOSE TO VR
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iMVP9
S750
Friday, August 07, 2020
0.5y
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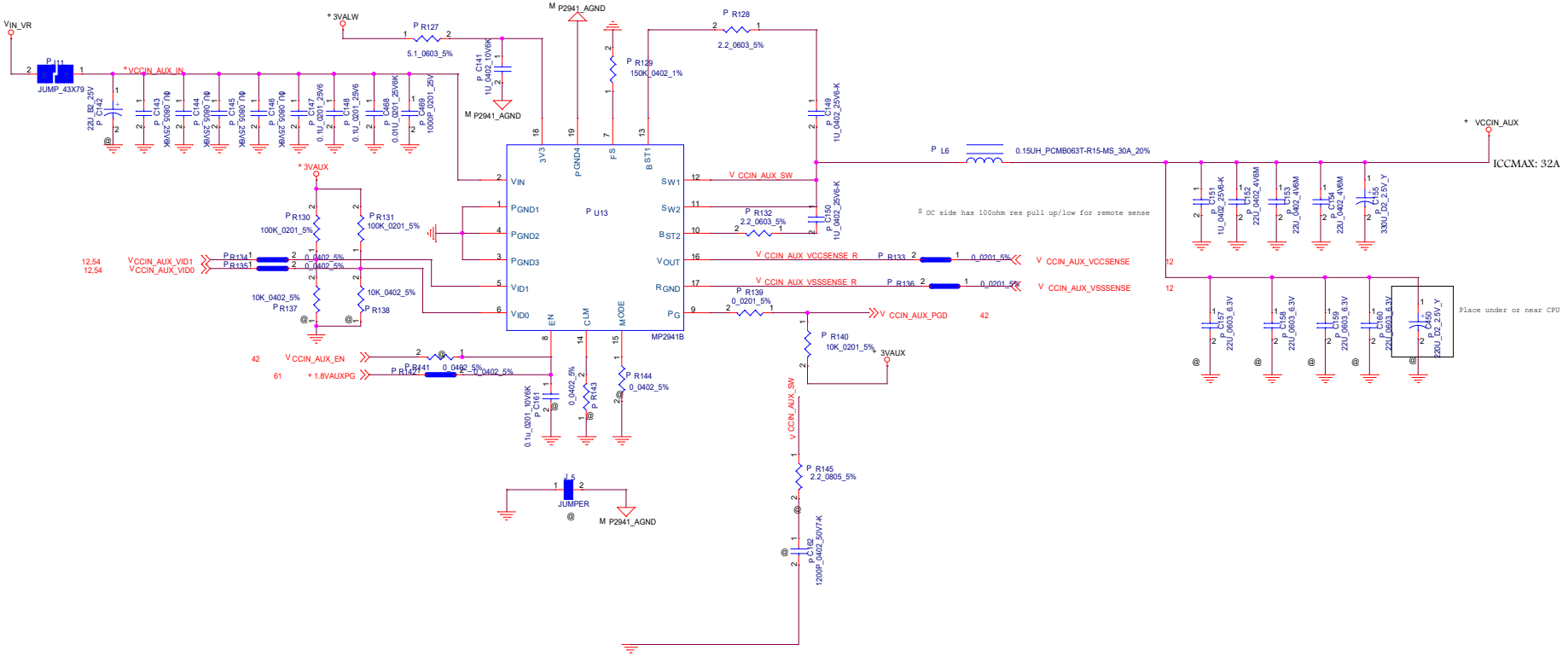

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Title: V CCINAUX

Size	Document Number	Rev
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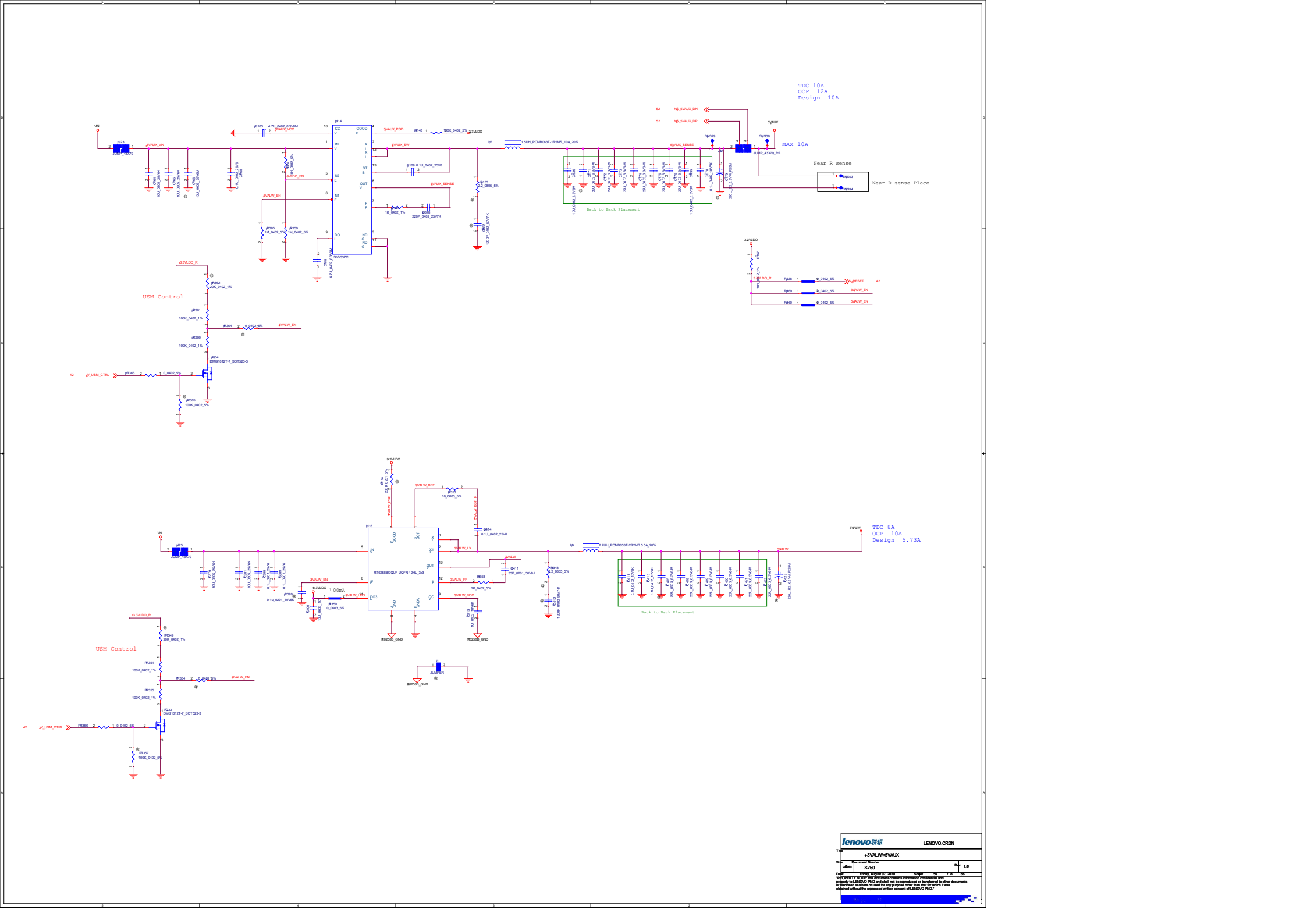
TDC 10A
OCP 12A
Design 10A
MAX 10A
Near R sense
Near R sense Place
Back to Back Placement
USM Control
TDC 8A
OCP 10A
Design 5.73A
Back to Back Placement
USM Control
LENOVO.CRDN
+3VALW/+5VAUX
S750
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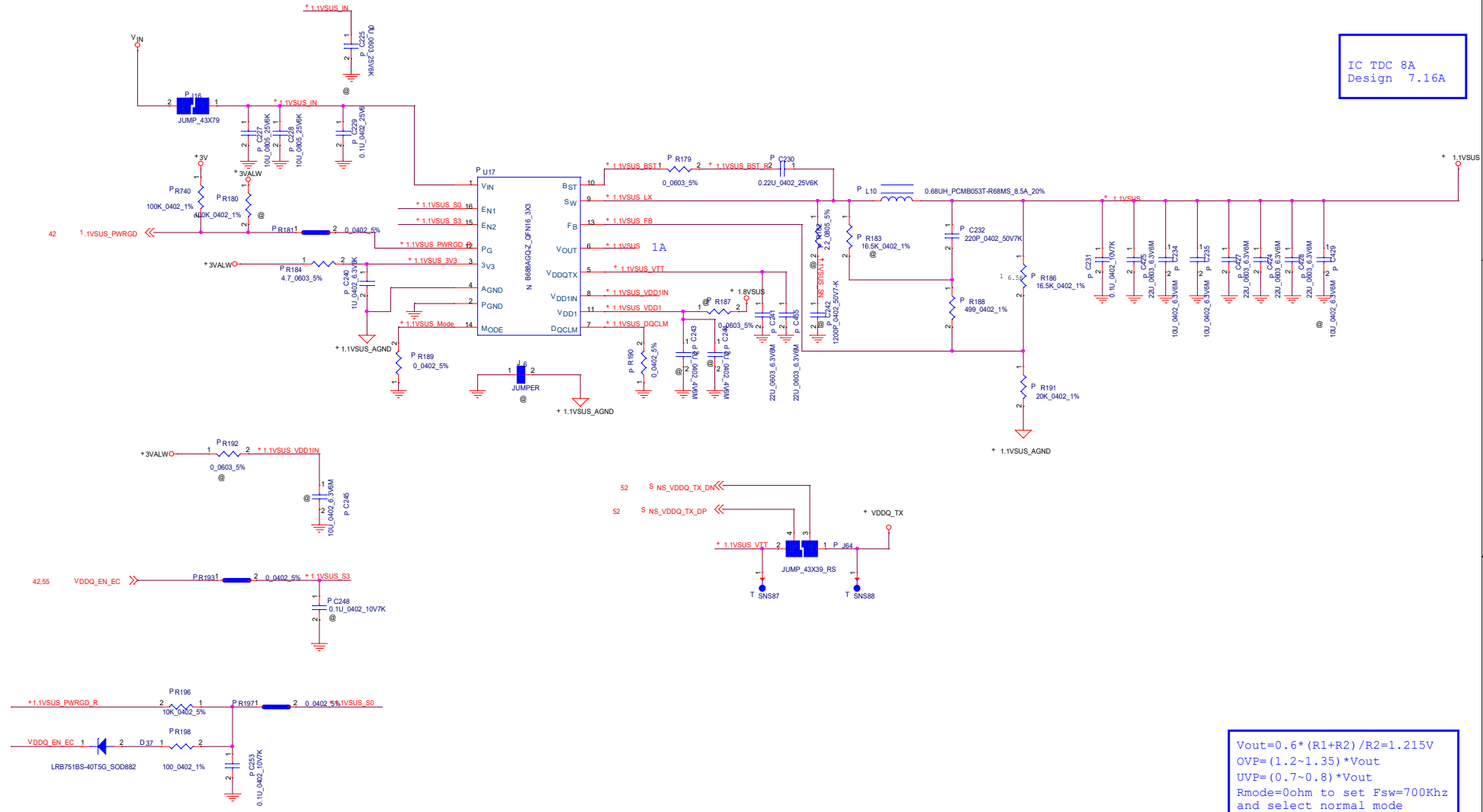
1.0



confirm with EE 0.6V enable

STATE	EN1	EN2	+1.1VSUS	+1.8VSUS	+0.6V
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off

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Title: + 1.1VSUS/+1.8VSUS

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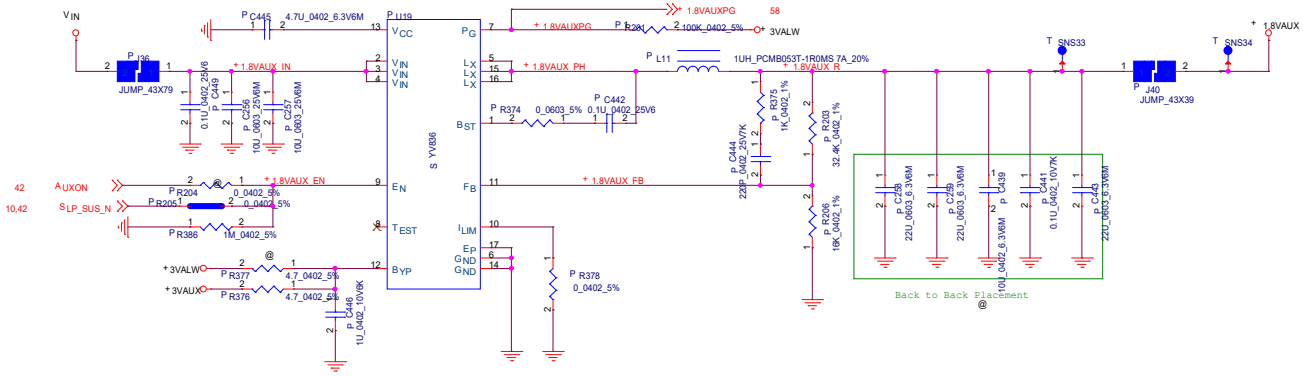
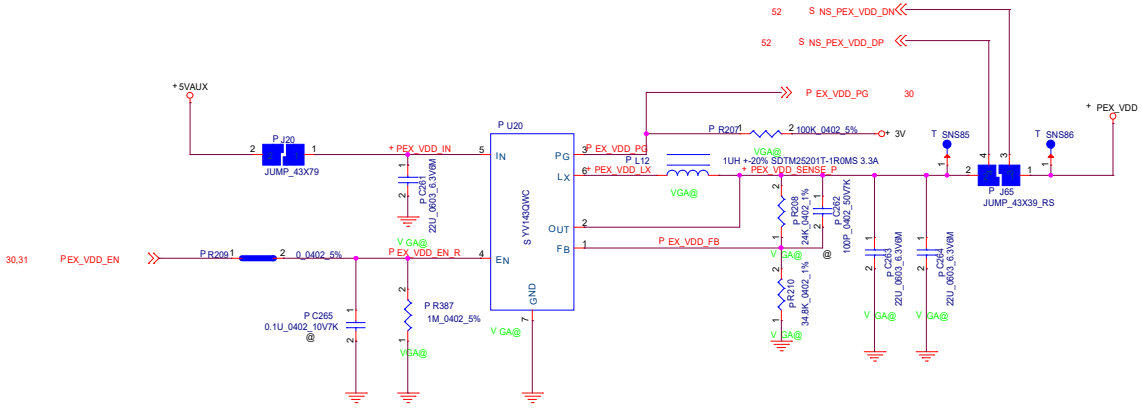


IC TDC 6A

Design 5.2A

Vout=0.6*(R1+R2)/R2=1.815V
OVP=1.2*Vout
Fsw=1Mhz



IC TDC 3A
Design 2A

Vout=0.6*(R1+R2)/R2=1.014V
OVP=1.2*Vout
UVP=0.4*Vout
Fsw=1.5Mhz

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Title: + 1.8VAUX

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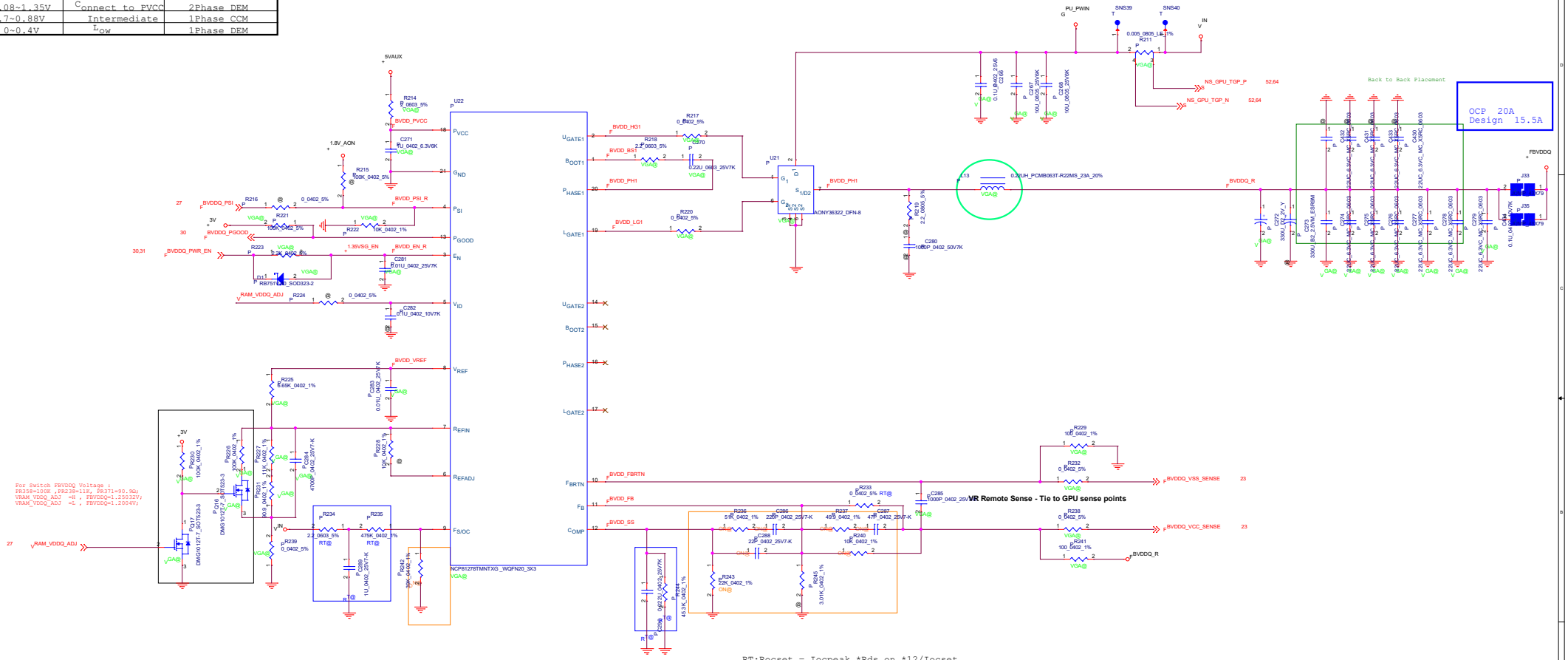
RT8816 PSI	$N_{CP81278PSI}$	Phase Configuration
1.6V~5.5V	High	2Phase CCM
1.08~1.35V	Connect to PVCC	2Phase DEM
0.7~0.88V	Intermediate	1Phase CCM
0~0.4V	Low	1Phase DEM



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Title: + FBVDDQ

Size: C (Custom) | Document Number: S 750 | Rev: V1.0

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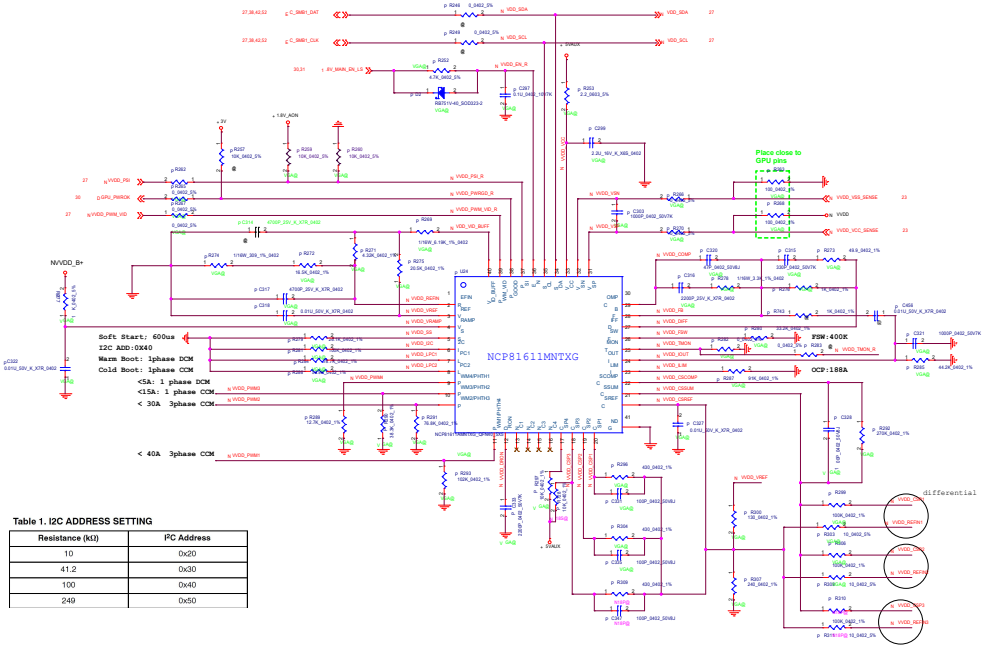
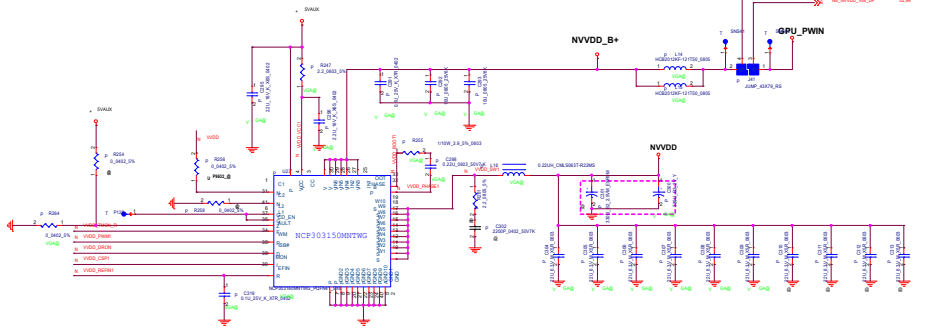
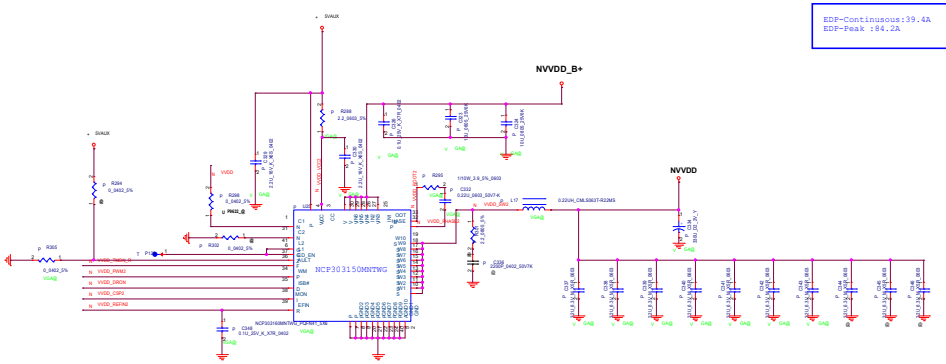




EDP-Continuous:39.4A
EDP-Peak :84.2A



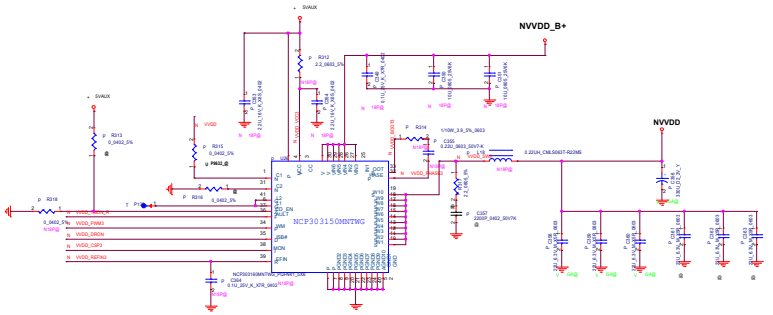


Table 1. I2C ADDRESS SETTING

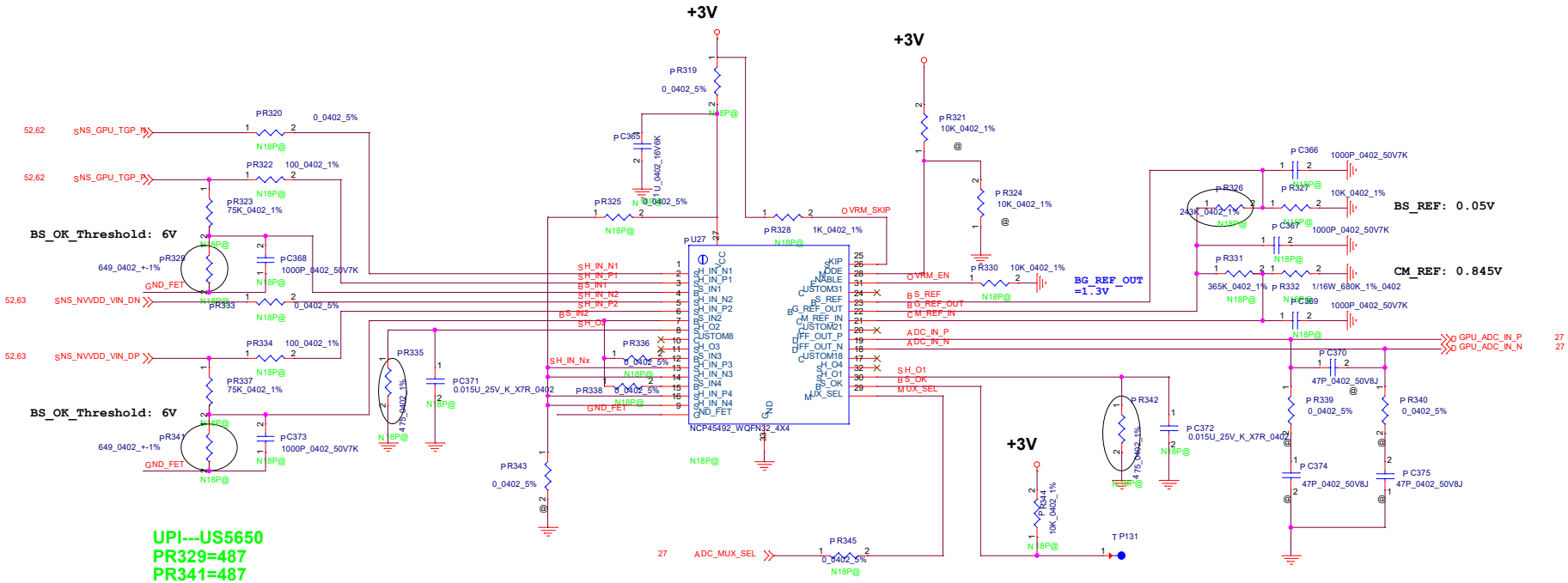
Resistance (kΩ)	I²C Address
10	0x20
41.2	0x30
100	0x40
249	0x50

When Stuff N18P GPU ,Pls Stuff N18P@ and Unstuff N18S@
When stuff N18S GPU ,Pls Stuff N18S@ and Unstuff N18P@

Bom Change (Default N18S)

For N18P GPU
PR285 : SDD3440228J,S RES 1/16W 40.2K +-1% 0402,
PR292 : SDD0001640D,S RES 1/16W 274K +-1% 0402,
PR280 : SDD3420282J,S RES 1/16W 200 +-1% 0402,
PR289 : SDD3412202J,S RES 1/16W 12K +-1% 0402
PR290 : SDD0001709D,S RES 1/16W 35.7K +-1% 0402
PR291 : SDD3495328J,S RES 1/16W 95.3K +-1% 0402
PR293 : SDD3495328J,S RES 1/16W 95.3K +-1% 0402

For N18S GPU
PR285 : SDD3440228J, S RES 1/16W 44.2K+-1%0402,
PR292 : SDD0001890D, S RES 1/16W 270K +-1% 0402,
PR280 : SDD3432282J, S RES 1/16W 33.2K +-1% 0402,
PR289 : SDD3412728J, S RES 1/16W 12.7K +-1% 0402,
PR290 : SDD3438382J, S RES 1/16W 38.3K +-1% 0402,
PR291 : SDD3476826J, S RES 1/16W 76.8K +-1% 0402,
PR293 : SDD0001840J, S RES 1/16W 102K +-1% 0402,



UPI---US5650
PR329=487
PR341=487
PR335=357ohm for Lower 70W 215 for 75W to 90W 165 for 100W to 110W
PR342=357ohm for Lower 70W 215 for 75W to 90W 165 for 100W to 110W
PR326=324K
PR323=75K
PR337=75K
PC368=1nF
PC373=1nF

ON---NCP45491
PR329=649
PR341=649
PR335=475ohm for lower 70W 287 for 75W to 90W 221 for 100W to 110W
PR342=475ohm for lower 70W 287 for 75W to 90W 221 for 100W to 110W
PR326=243K
PR323=75K
PR337=75K
PC368=1nF
PC373=1nF
Stuff PR325

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Title: Power Monitor

Size: C ustom | Document Number: S750 | Rev: V 1.0

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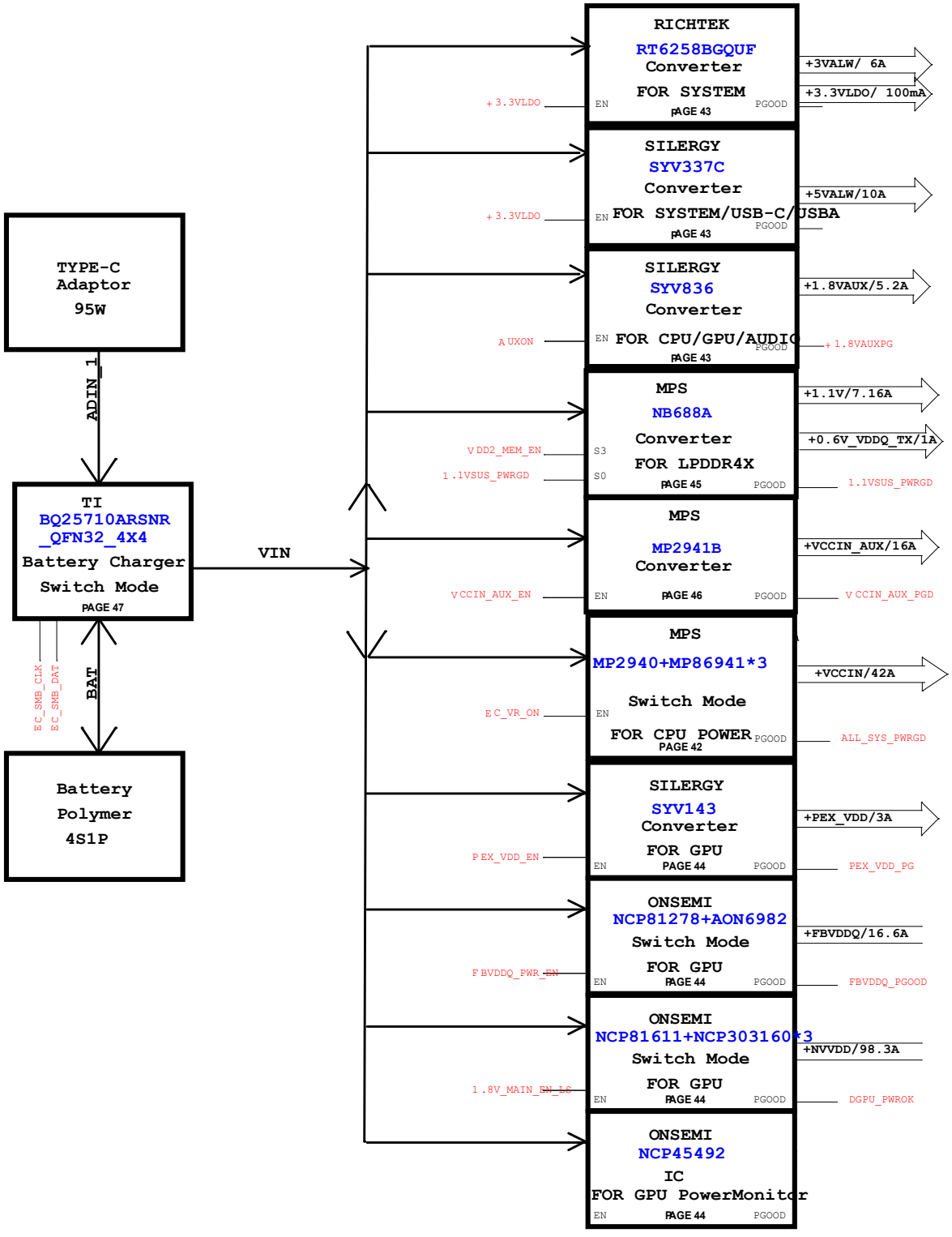

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Title: P WR-Power Diagram

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H1
HOLEA
h-c232d130

H2
HOLEA
hole236_102

H3
HOLEA
hole236_102

H4
HOLEA
h-c232d130

FD1
CF

FD2
CF

FD3
CF

FD4
CF

FD5
CF

FD6
CF

H7
HOLEA
hole236_102

H9
HOLEA
hole236_102

H10
HOLEA
hole236_102

H12
HOLEA
hole236_102

H11
HOLEA
hole236_102

N15
NUT-WLAN
NUT-D3_4-7x5_2x2_1mm
ME@

H13
HOLEA
hole236_90

H14
HOLEA
hole236_90

H15
HOLEA
hole236_90

N16
NUT-THM
NUT-D3_3-5_9x5_9x1mm
ME@

N17
NUT-THM
NUT-D3_3-5_9x5_9x1mm
ME@

N19
NUT-THM
NUT-D3_3-5_9x5_9x1mm
ME@

N18
NUT-THM
NUT-D3_3-5_9x5_9x1mm
ME@

N21
NUT-THM
NUT-D3_3-5_9x5_9x1mm
ME@

N20
NUT-THM
NUT-D3_3-5_9x5_9x1mm
ME@

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Title
M OUNTING HOLE/EMI

Size
B

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