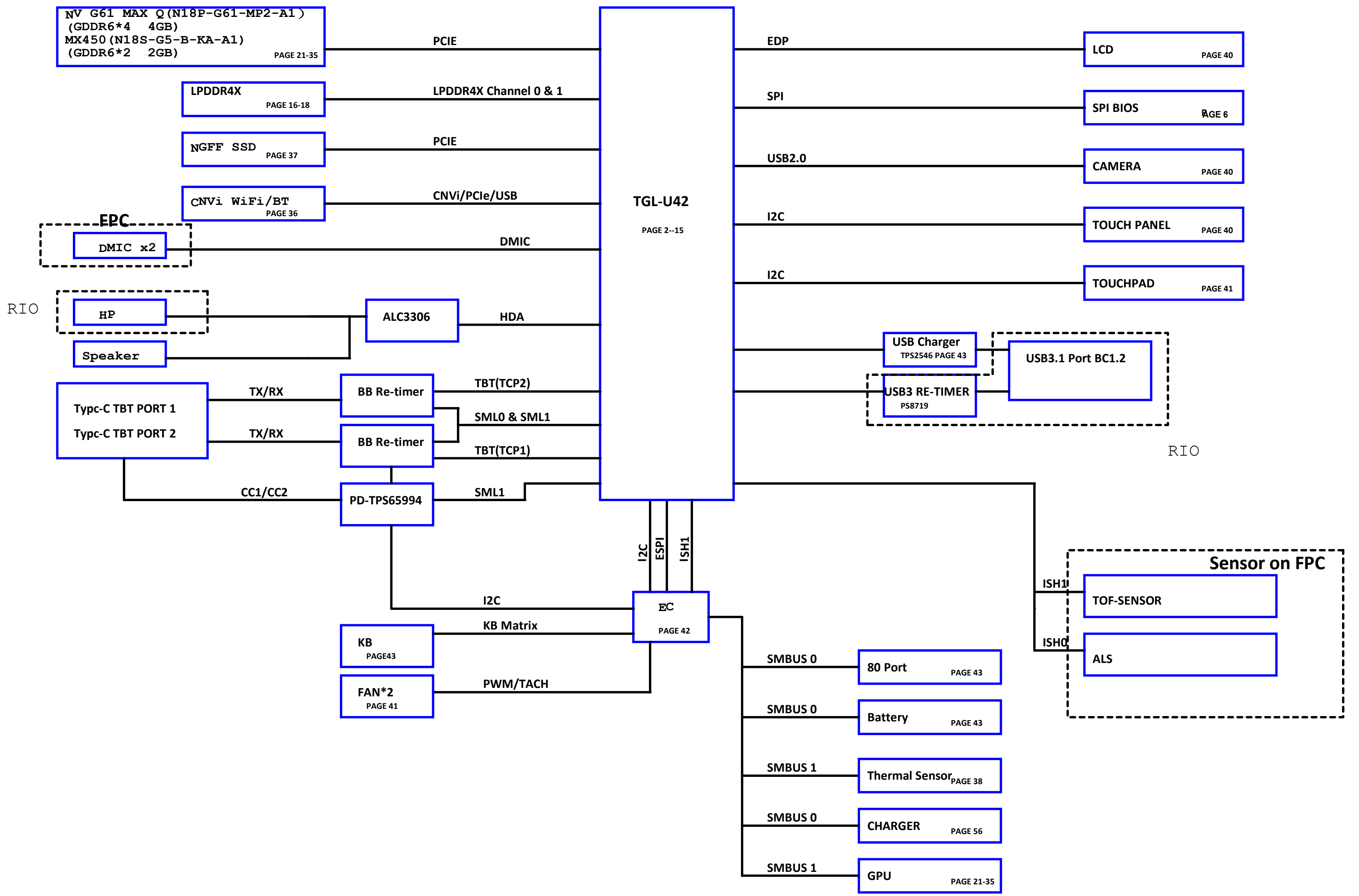
S750 TGL-U42 Schematic Block Diagram



SMBus ADDRESS:
EC_SMB1: 0x9A, 0x98 THERMAL SENSOR
I2C ADDRESS:
ISH-I2C0: 0x88 ALS
ISH I2C1: 0X52 TOF

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Title: T GL-U Block Diagram		
Size: C	Document Number: S 750	Rev: 0.5
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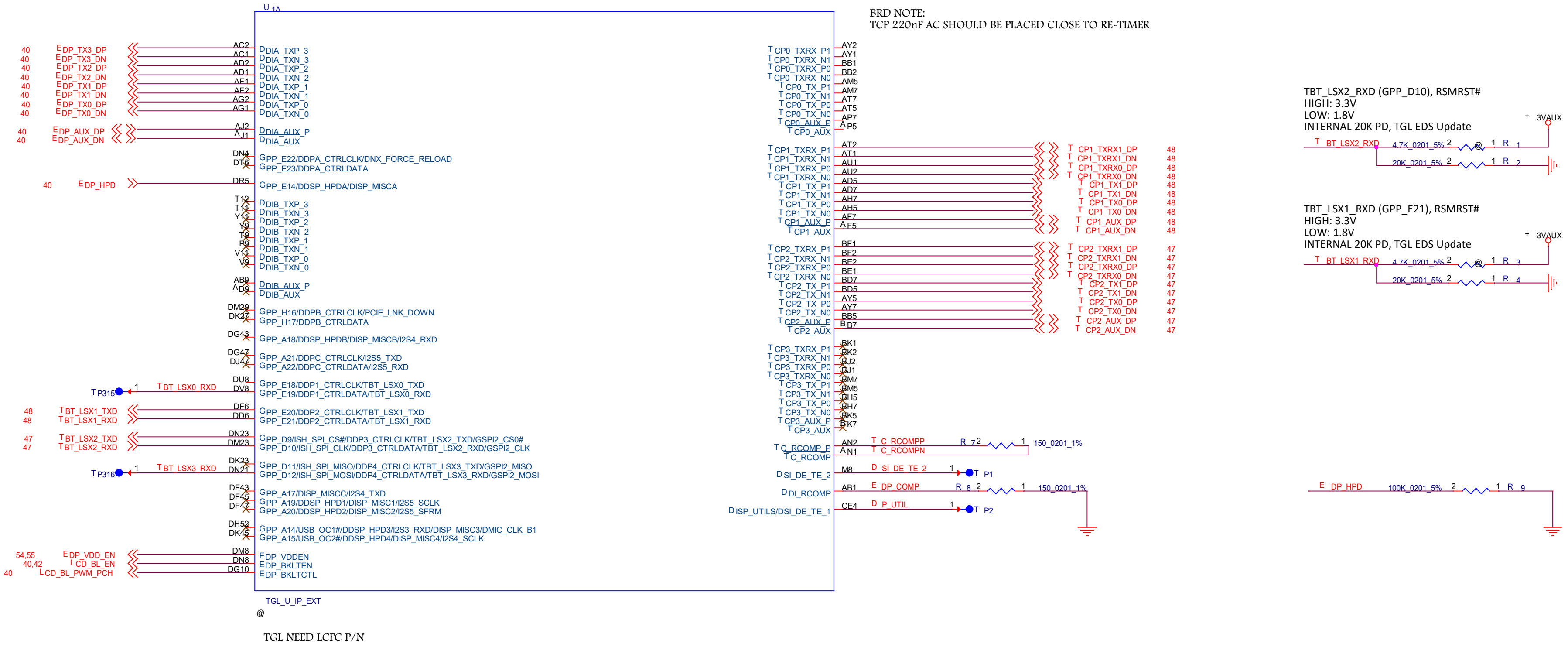

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Title: Tiger Lake MCP (TBT,EDP)

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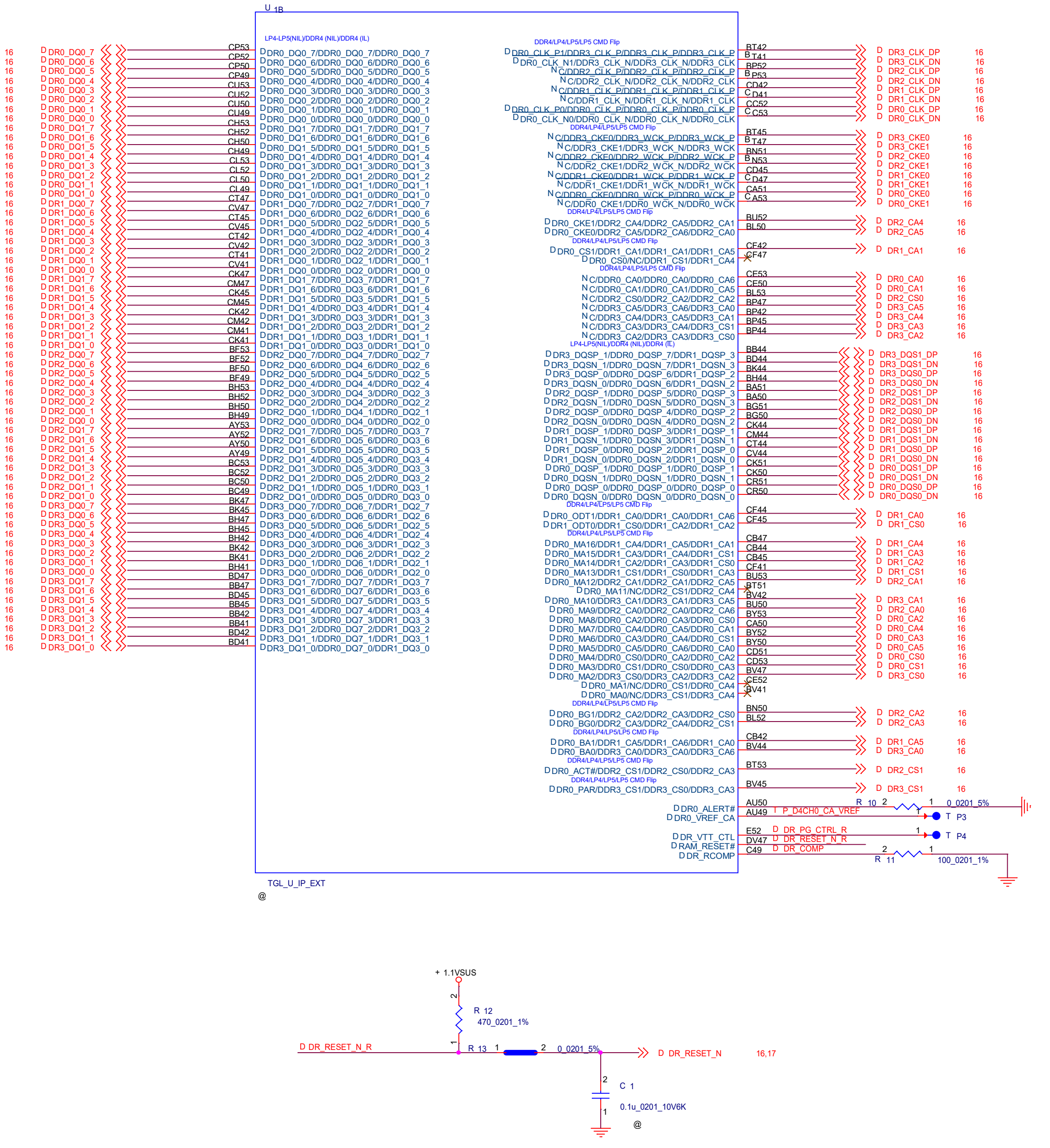
CPU LPDDR4X CHANNEL 0



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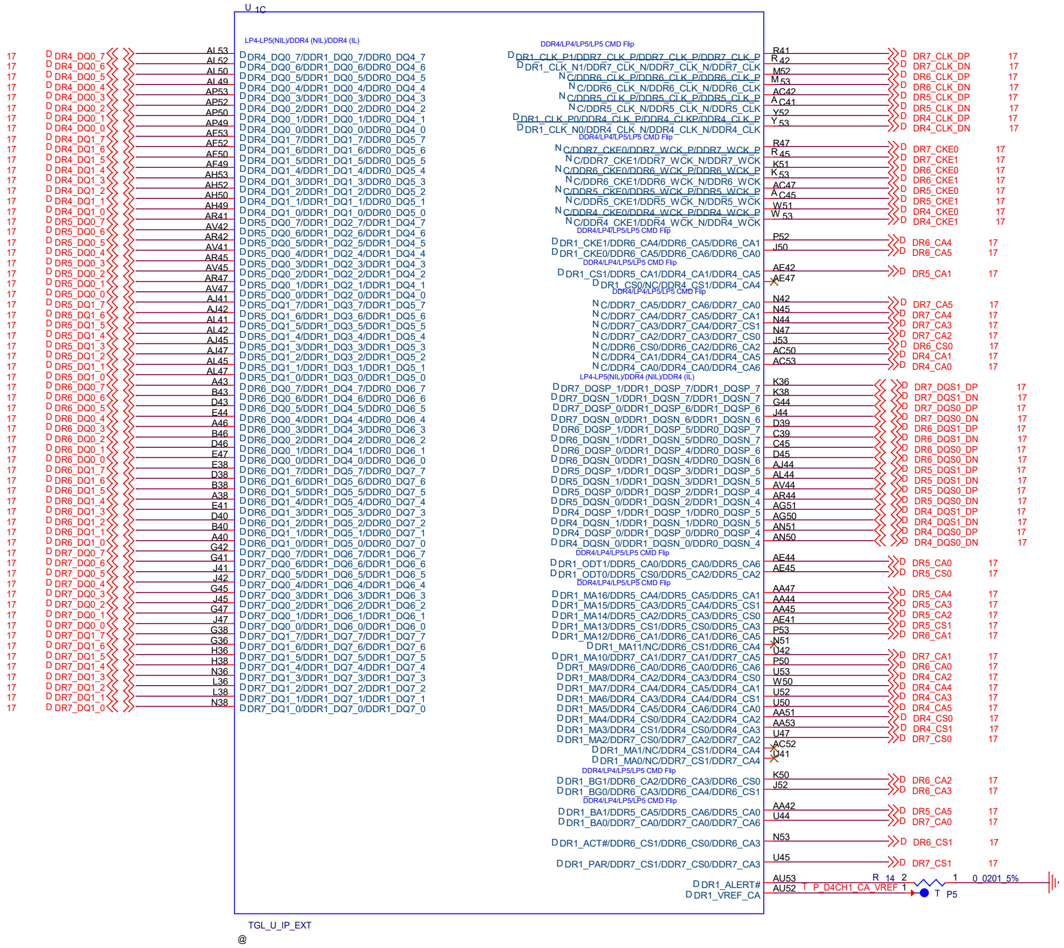
Title: Tiger Lake MCP (PROCESSOR LP4X)

Size	Document Number	Rev
C	S 750	0.5

Date: Friday, August 07, 2020 Sheet 3 of 66

CPU LPDDR4X CHANNEL 1



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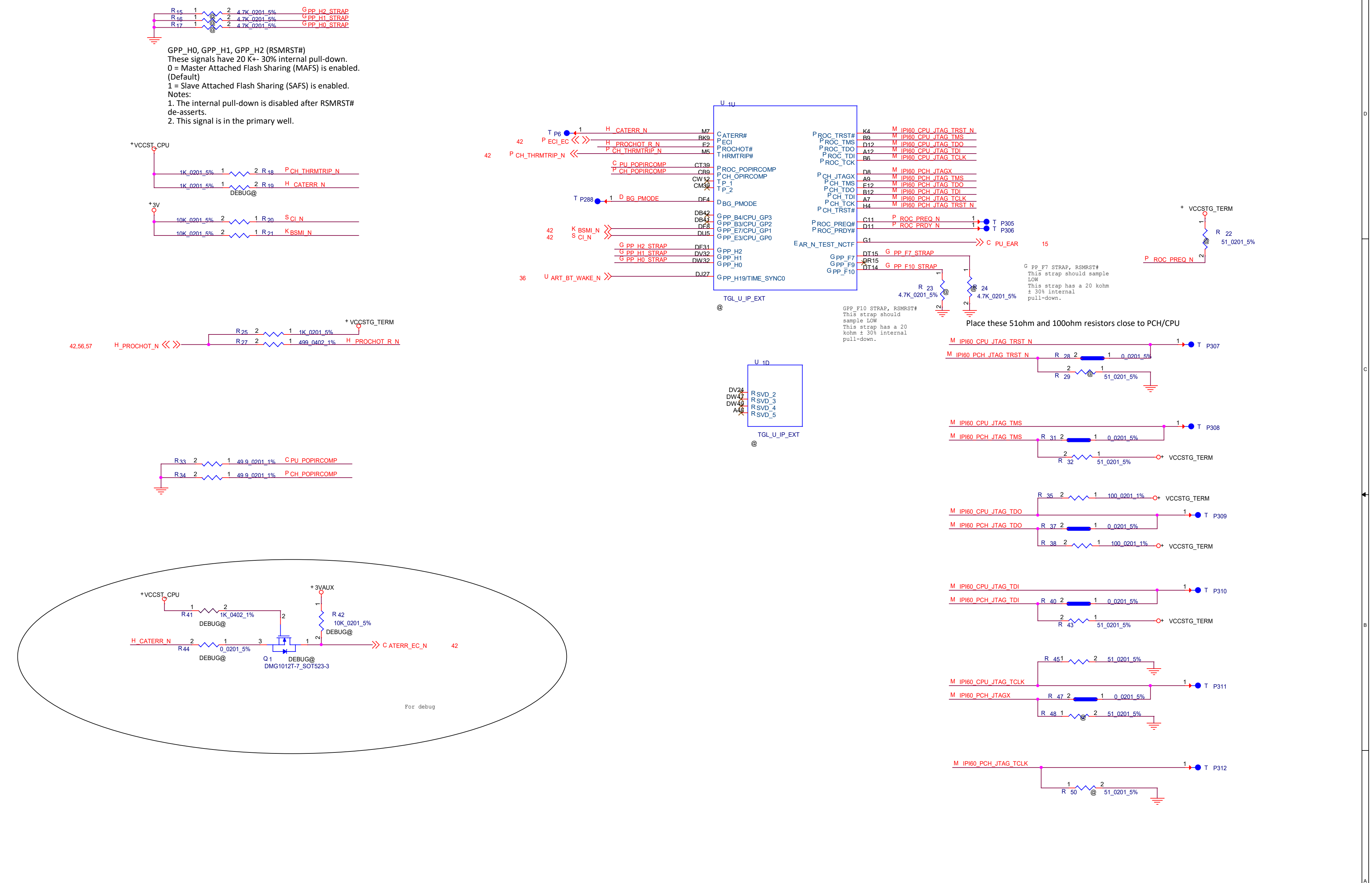
Title: Tiger Lake MCP (PROCESSOR LP4X)

Size: C | Document Number: S 750 | Rev: 0.5

Date: Friday, August 07, 2020 | Sheet 4 of 66



GPP_H0, GPP_H1, GPP_H2 (RSMRST#)
These signals have 20 K+- 30% internal pull-down.
0 = Master Attached Flash Sharing (MAFS) is enabled.
(Default)
1 = Slave Attached Flash Sharing (SAFS) is enabled.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

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Title: Tiger Lake MCP (MISC THERM CPU JTAG)

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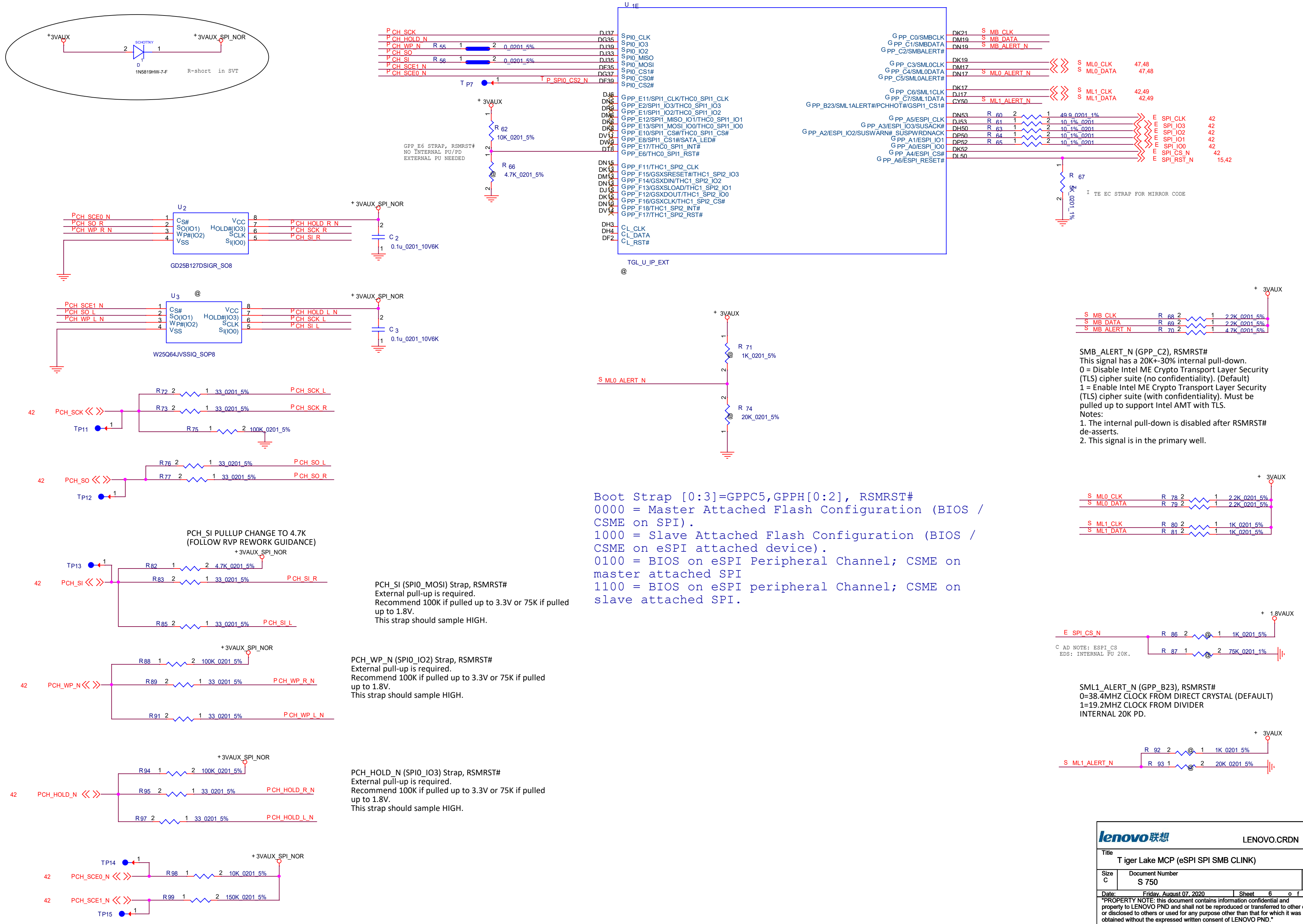
Date: Friday, August 07, 2020 | Sheet 5 of 66



PCH_SI PULLUP CHANGE TO 4.7K
(FOLLOW RVP REWORK GUIDANCE)

PCH_SI (SPI0_MOSI) Strap, RSMRST#
External pull-up is required.
Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH.

PCH_WP_N (SPI0_IO2) Strap, RSMRST#
External pull-up is required.
Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH.

PCH_HOLD_N (SPI0_IO3) Strap, RSMRST#
External pull-up is required.
Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH.

Boot Strap [0:3]=GPPC5,GPPH[0:2], RSMRST#
0000 = Master Attached Flash Configuration (BIOS / CSME on SPI).
1000 = Slave Attached Flash Configuration (BIOS / CSME on eSPI attached device).
0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI
1100 = BIOS on eSPI peripheral Channel; CSME on slave attached SPI.

SMB_ALERT_N (GPP_C2), RSMRST#
This signal has a 20K+-30% internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

SML1_ALERT_N (GPP_B23), RSMRST#
0=38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)
1=19.2MHZ CLOCK FROM DIVIDER
INTERNAL 20K PD.

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Title: Tiger Lake MCP (eSPI SPI SMB CLINK)

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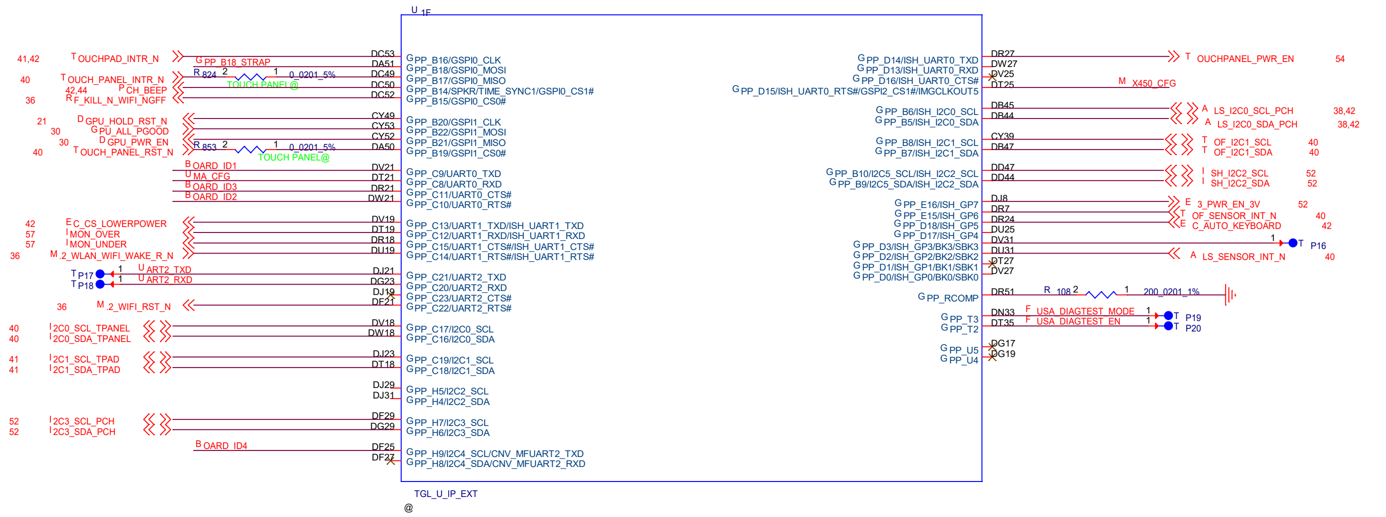
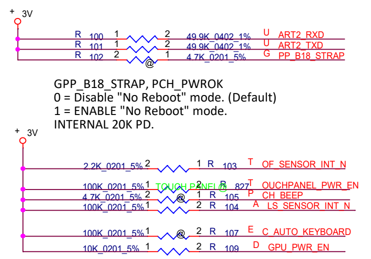
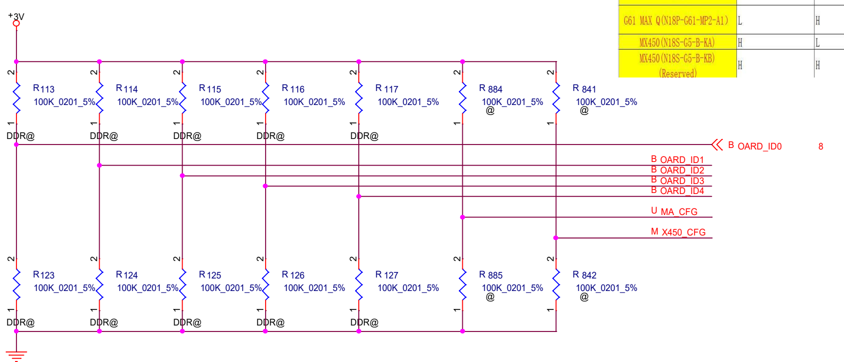


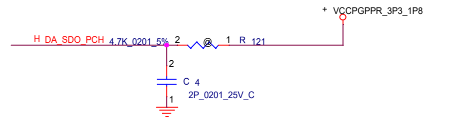
GPP_B18_STRAP, PCH_PWROK
0 = Disable "No Reboot" mode. (Default)
1 = ENABLE "No Reboot" mode.
INTERNAL 20K PD.



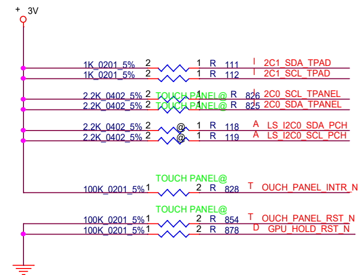
BOARD ID

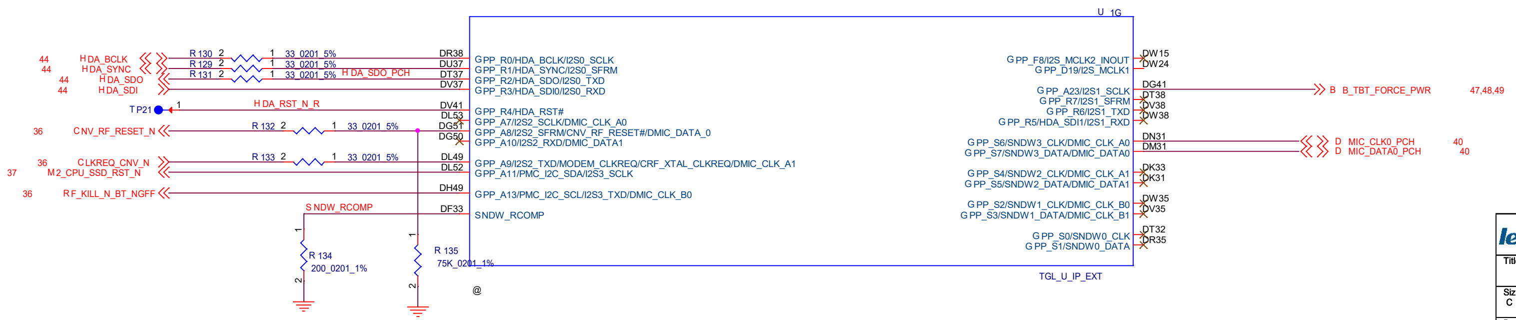


	UMA_CFG R884=1/R885=0	MX450_CFG R841=1/R842=0
UMA	L	L
G61 MAX Q(N18P-G61-MP2-A1)	L	H
MX450(N18S-G5-B-KA)	H	L
MX450(N18S-G5-B-KB) (Reserved)	H	H



HDA_SDO_R (GPP_R2), PCH_PWROK
Flash Descriptor Security Override, Rising edge of PCH_PWROK.
0: Enable security measures defined in the Flash Descriptor. (Default Internal 20K PD)
1: Disable Flash Descriptor Security (override).





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Title: Tiger Lake MCP (I2C ISH UART GPIO)

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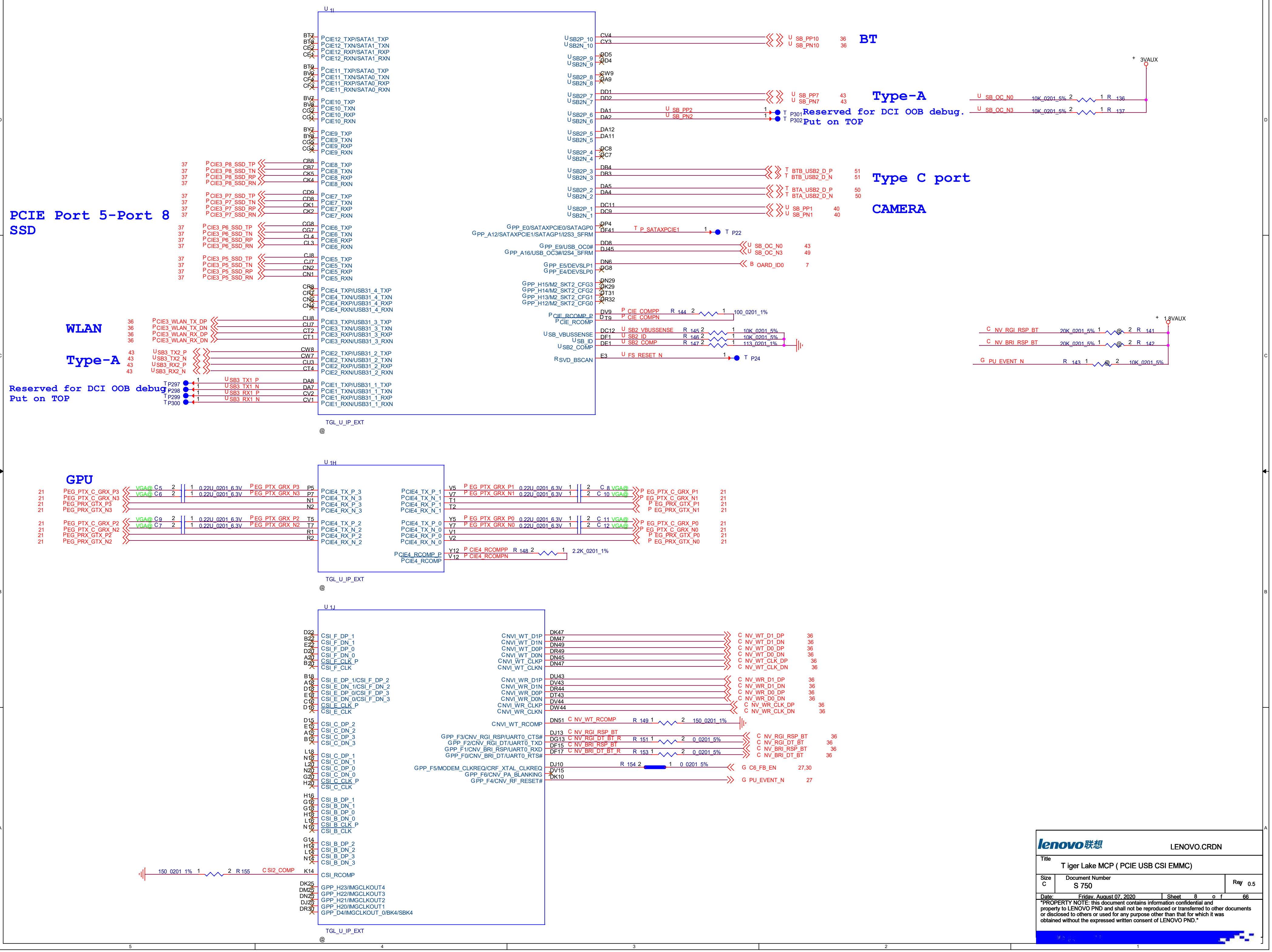

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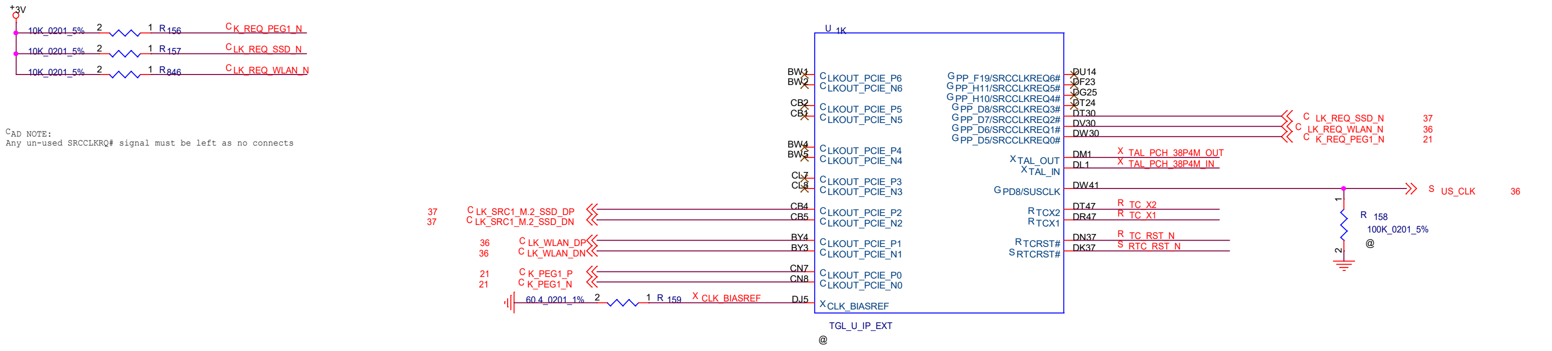
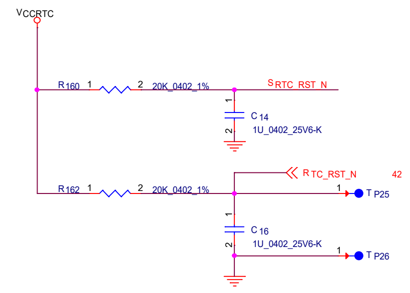
Title: Tiger Lake MCP (PCIE USB CSI EMMC)

Size: C | Document Number: S 750 | Rev: 0.5

Date: Friday, August 07, 2020 | Sheet 8 of 66

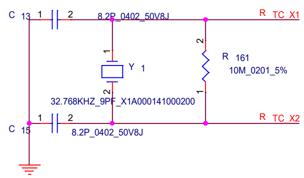


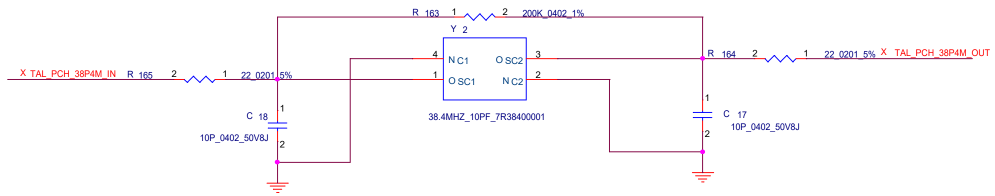


ME RESET
SAVE ME = PU (Default)
CLEAR ME = PD

CMOS RESET
SAVE CMOS = PU (Default)
CLEAR CMOS = PD

TP8 TP9 Need to put on the TOP





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Title: Tiger Lake MCP (CLK)

Size	Document Number	Rev
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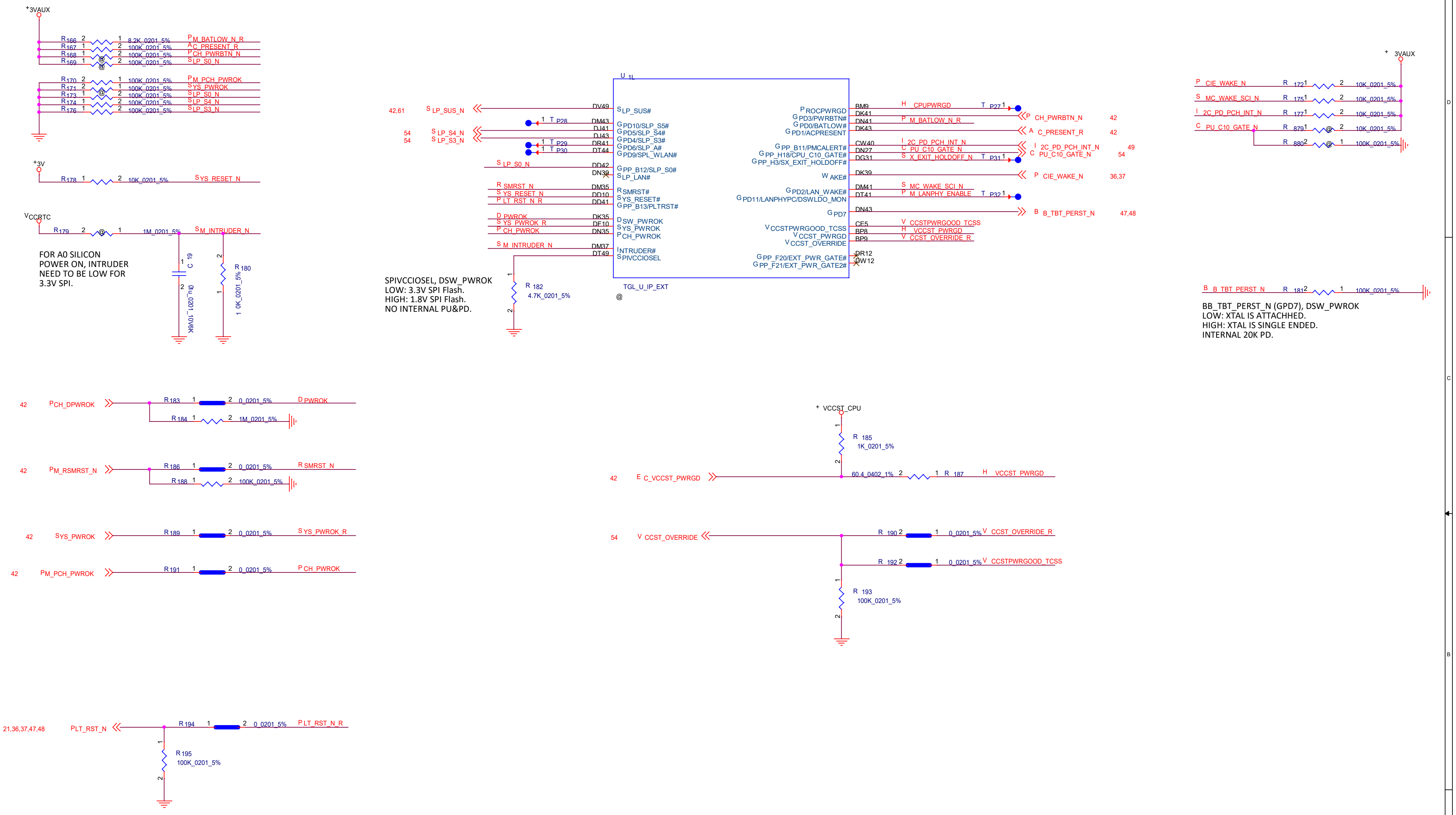
Date: Friday, August 07, 2020 Sheet 9 of 66



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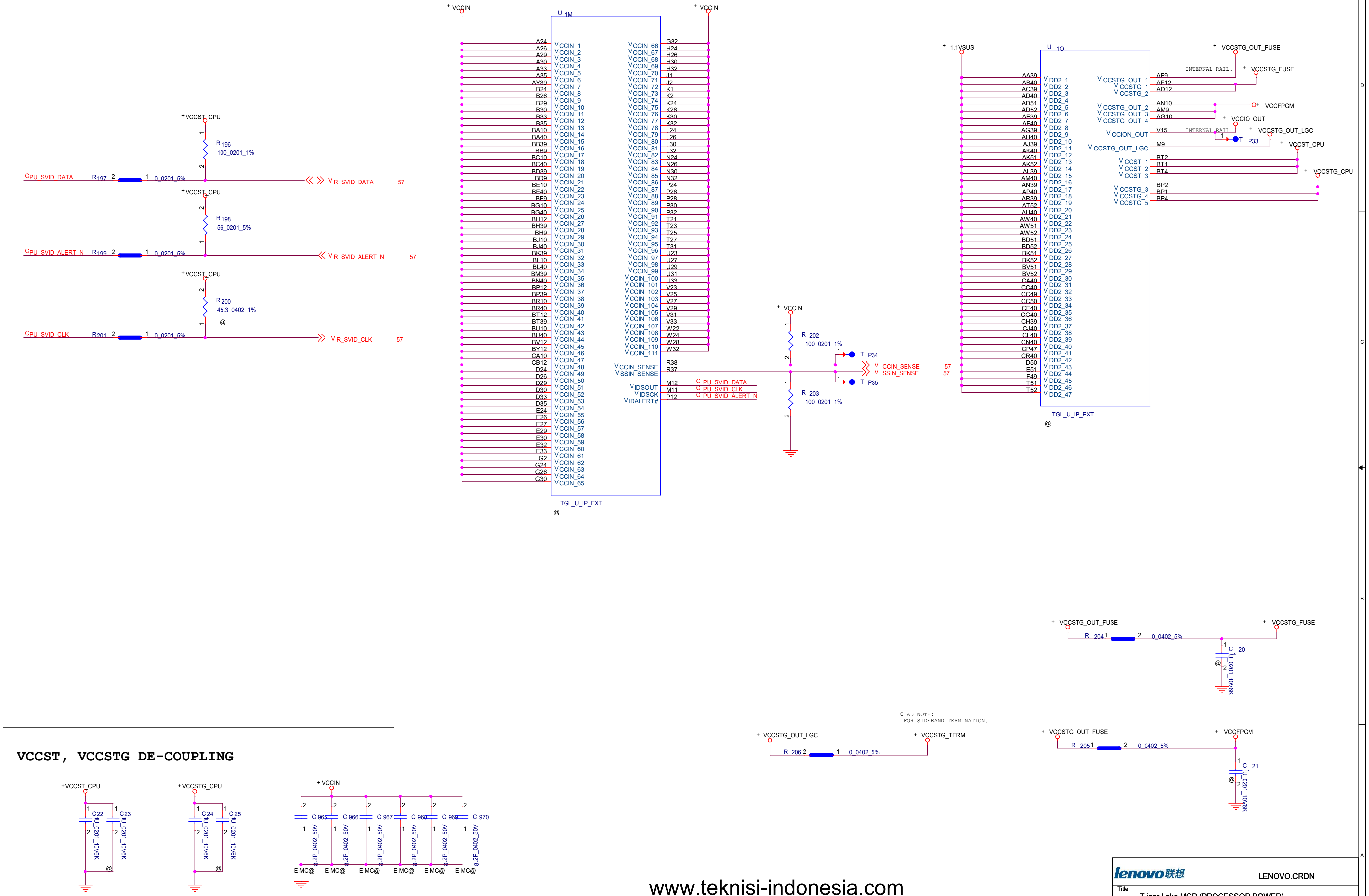
Title: Tiger Lake MCP (PM)

Size: C | Document Number: S750 | Rev: 0.5

Date: Friday, August 07, 2020 | Sheet 10 of 66



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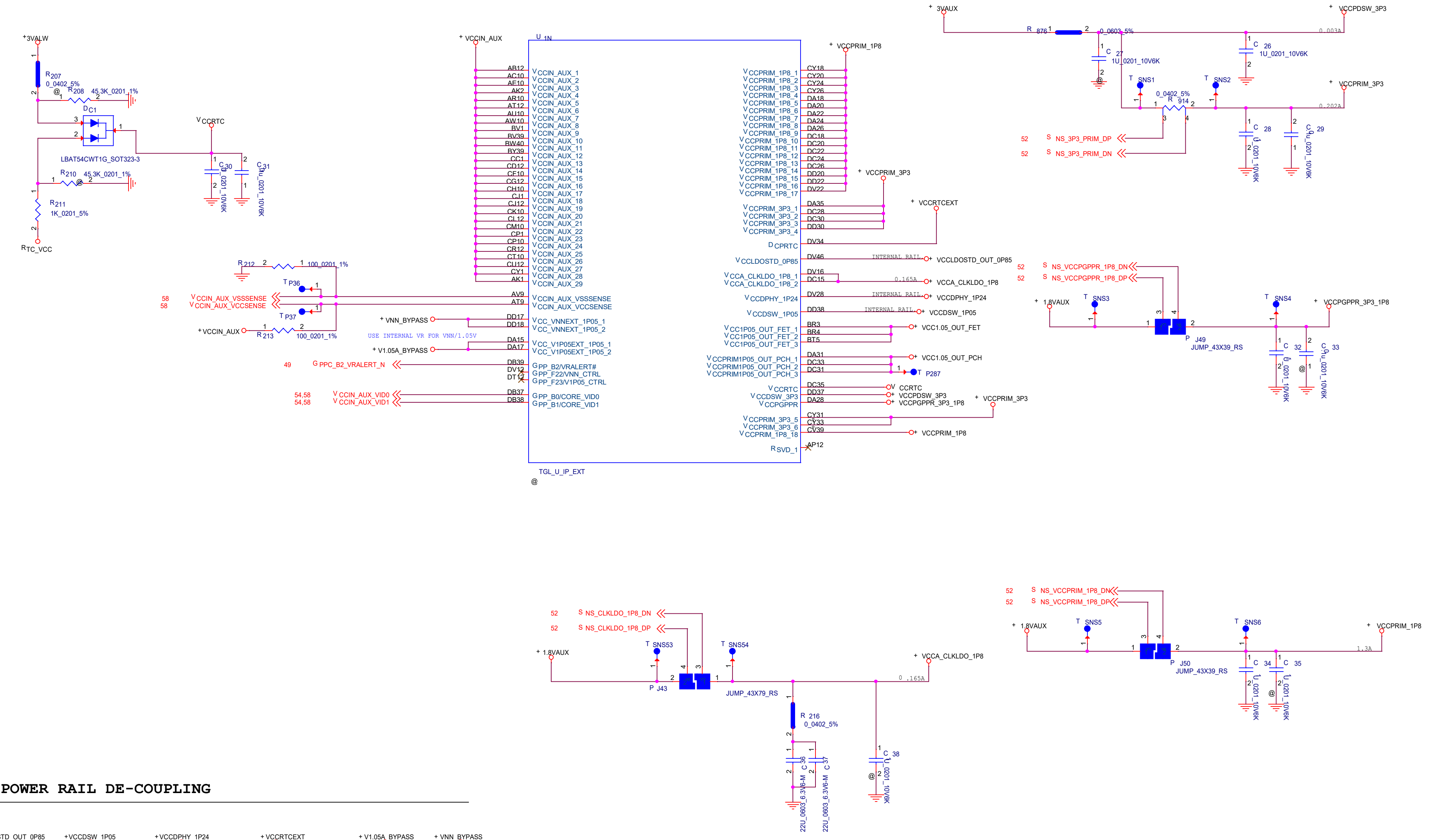
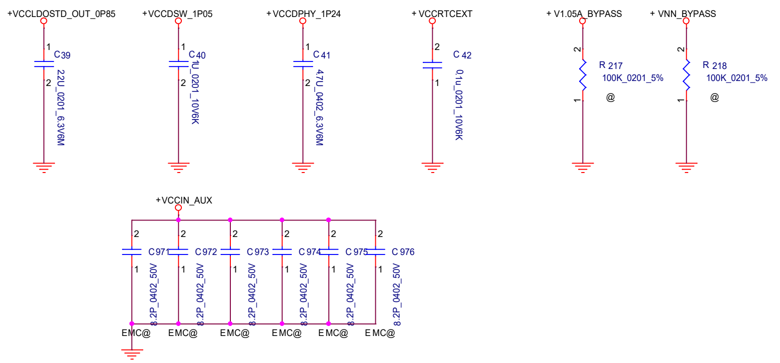
Title: Tiger Lake MCP (PROCESSOR POWER)

Size: C | Document Number: S 750 | Rev: 0.5

Date: Friday, August 07, 2020 | Sheet 11 of 66



PCH POWER RAIL DE-COUPLING



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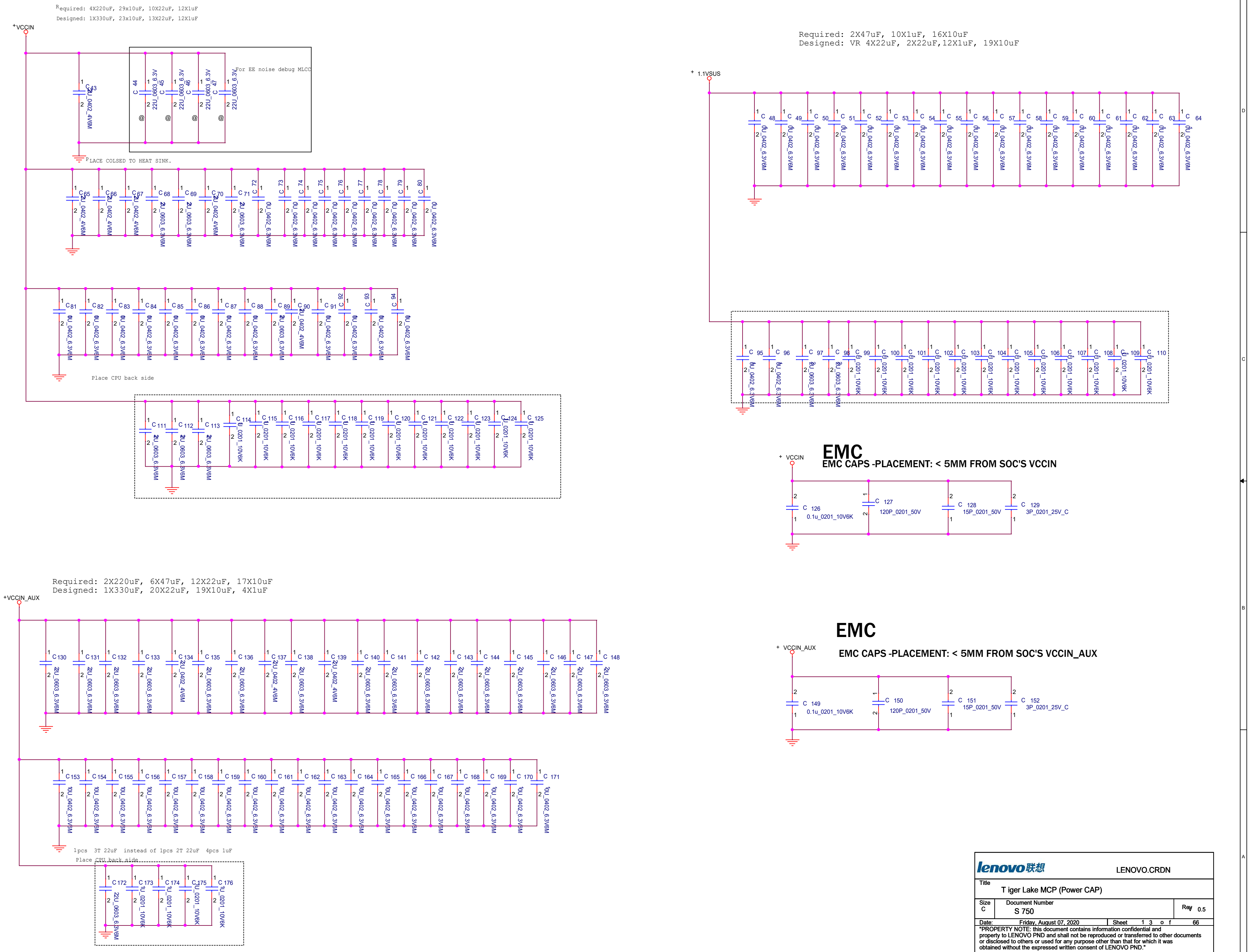
Title: Tiger Lake MCP (PCH POWER)

Size: C | Document Number: S 750 | Rev: 0.5

Date: Friday, August 07, 2020 | Sheet 12 of 66



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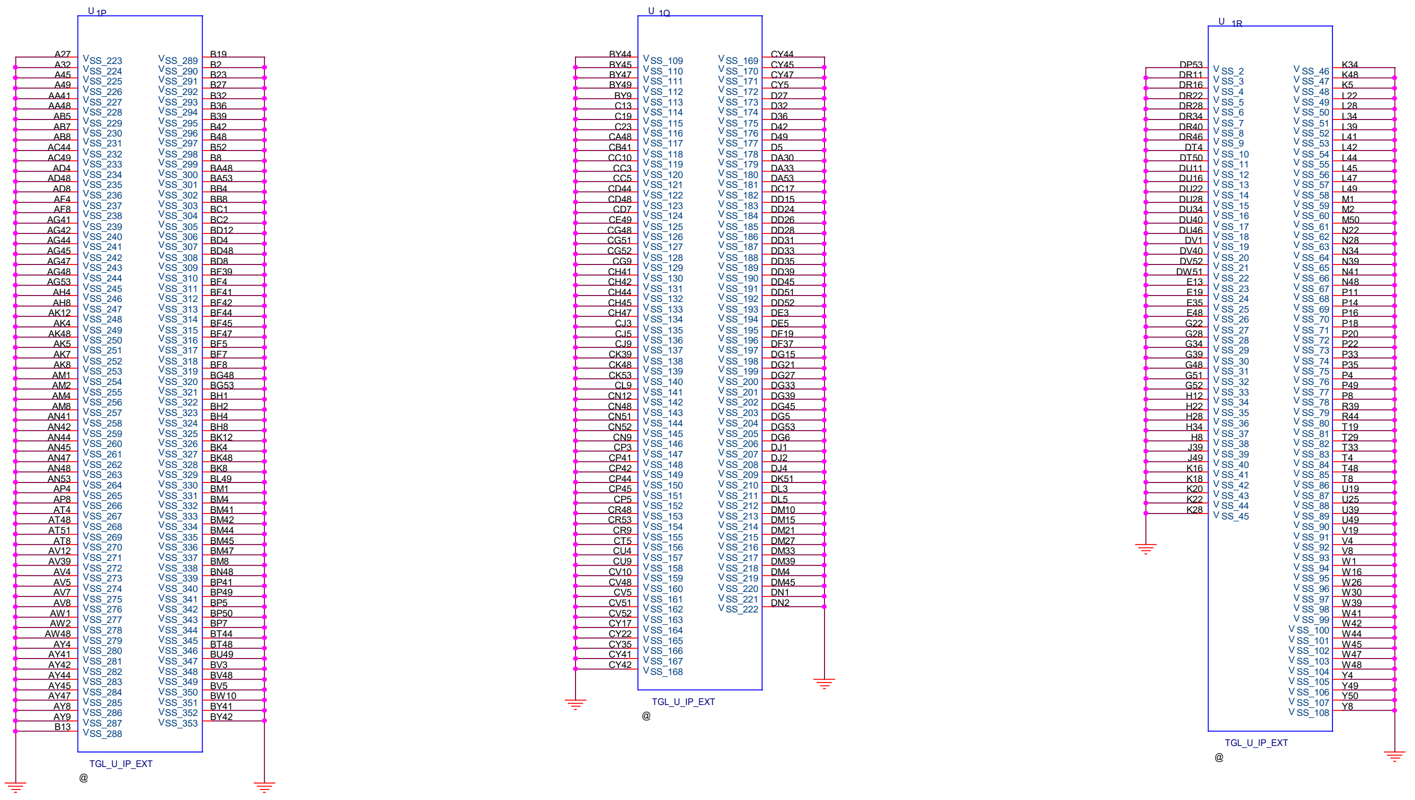
Title: Tiger Lake MCP (Power CAP)

Size: C | Document Number: S 750 | Rev: 0.5

Date: Friday, August 07, 2020 | Sheet 13 of 66



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Title: Tiger Lake MCP (GND)

Size: C

Document Number: S 750

Rev: 0.5

Date: Friday, August 07, 2020

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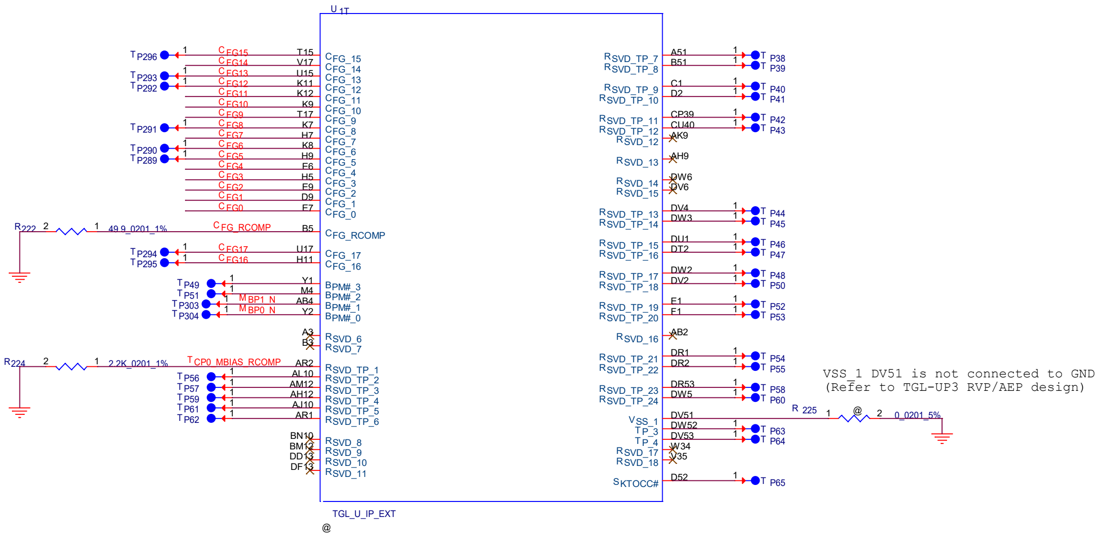
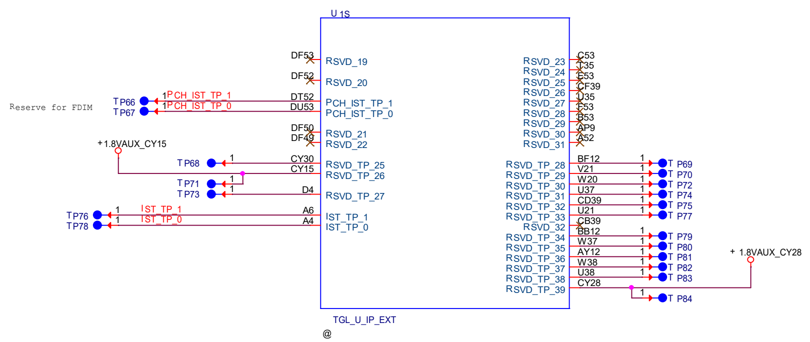
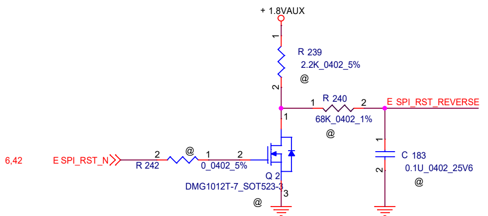
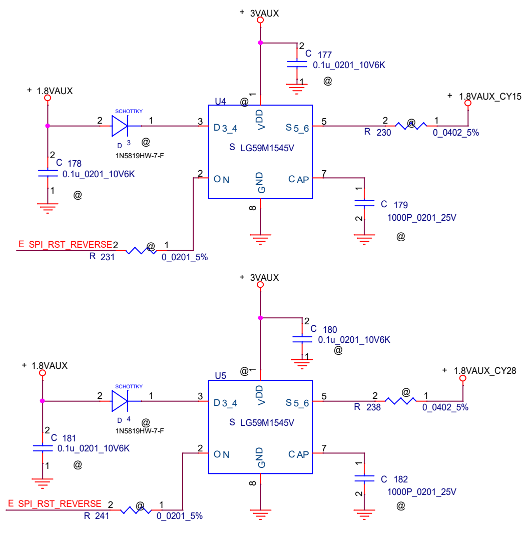


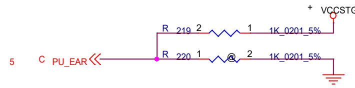


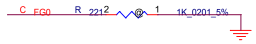




ES1 Workaround Circuit (DOC# 614056)

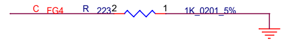
PROCESSOR CFG STRAPS



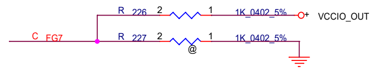


Stall reset sequence after PCU PLL lock until de-asserted	
EAR	1:Normal(Default) *
	0:Stall

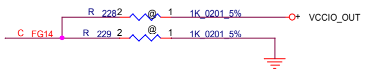
Changed From CFG0 to EAR (Refer to WW32 MOW)



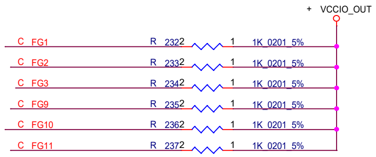
Embedded Display Port Presence Strap	
CFG4	1:Disable
	0:Enable(Default) *



PEG deferred link training	
CFG7	1:TBD(Default) *
	0:TBD



PEG60 Lane Reversal	
CFG14	1:Normal
	0:Reversed(Default) *



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Title: Tiger Lake MCP (RSVD)

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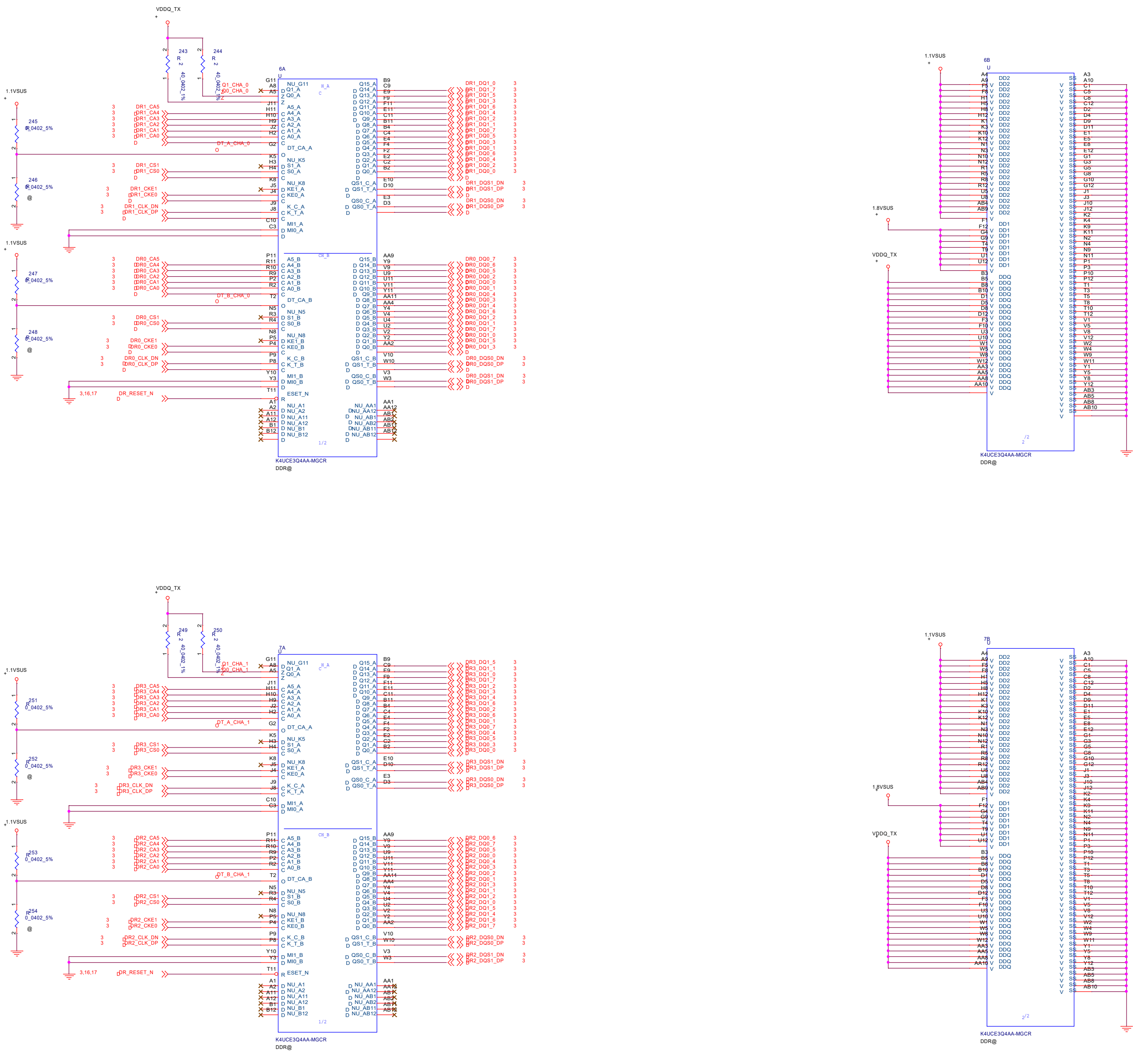

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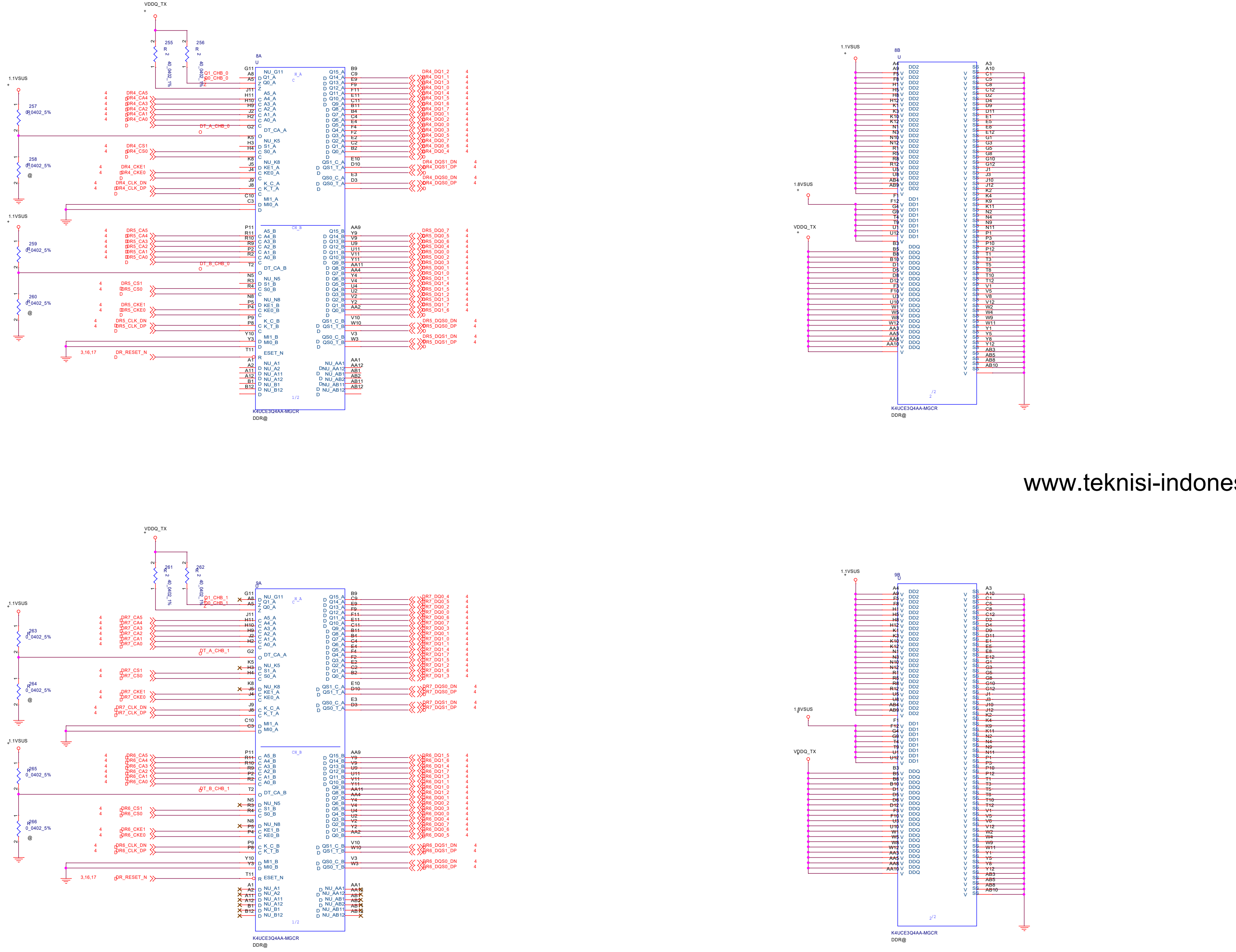
Title: LP4X-CHA ONBD

Size: D | Document Number: S750 | Rev: 0.5y

Date: Friday, August 07, 2020 | Sheet 16 of 66



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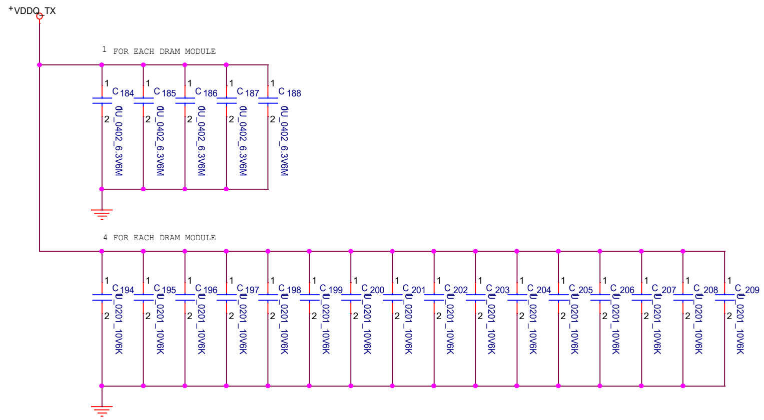
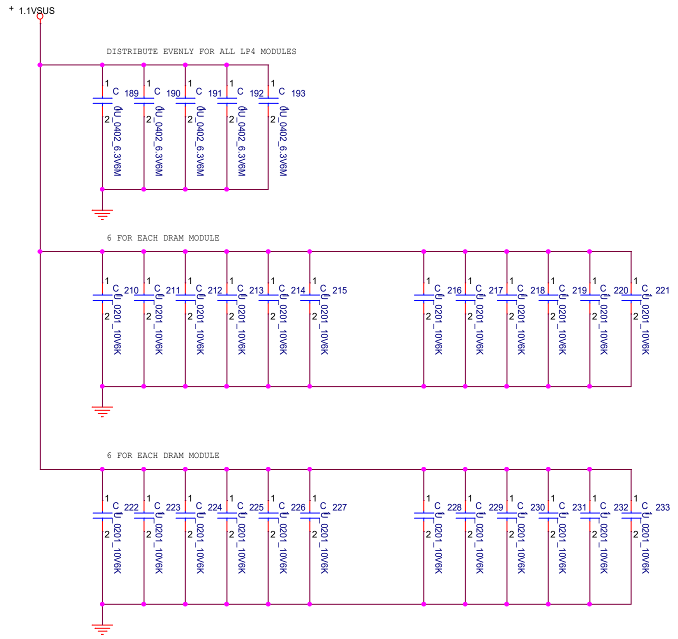
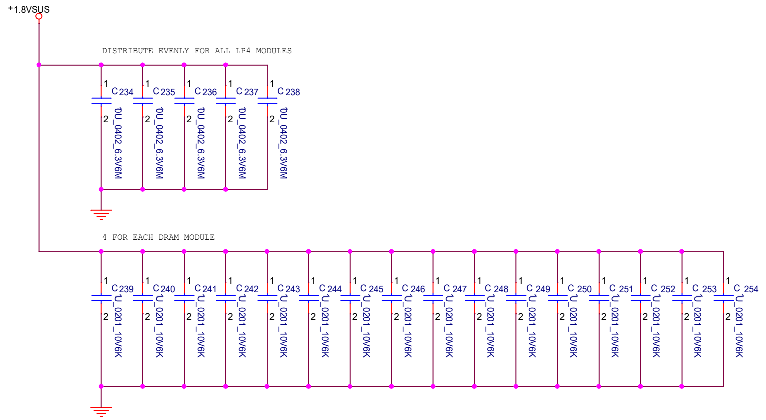
Title: LP4X-CHB ONBD

Size: D Document Number: S750 Rev: 0.5y

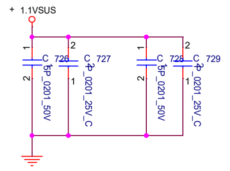
Date: Friday, August 07, 2020 Sheet 17 of 66







EMC CAP CHANNEL 0 AND 1



EMC CAP:
1. PLACE 4MM FROM DRAM
2. PLACE EACH SET WITHIN 12MM

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Title: L P4X-DECOUPLING

Size: C | Document Number: S 750 | Rev: 0.5

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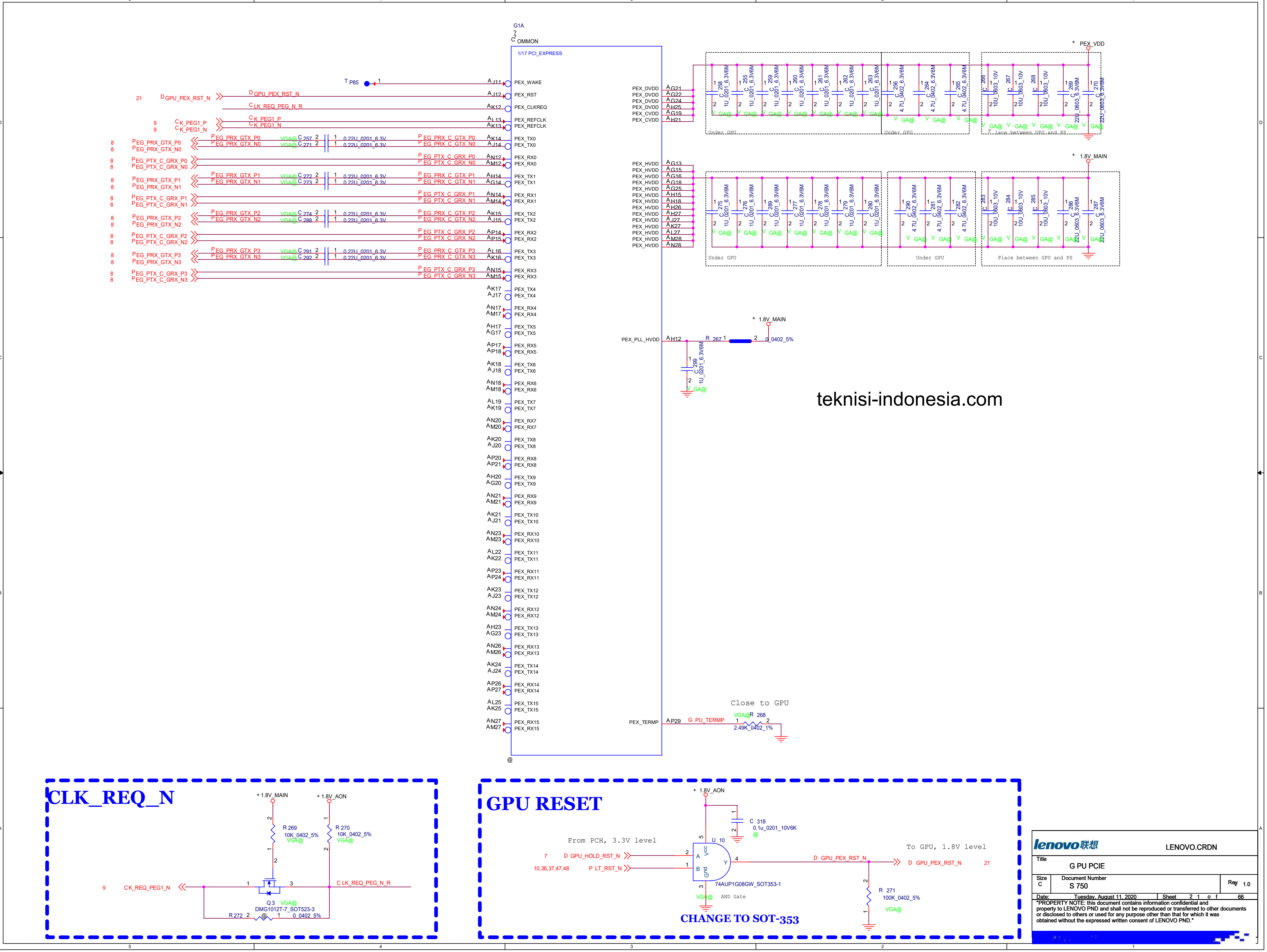

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Title: GPU PCIE

Size	Document Number	Rev
C	S750	1.0

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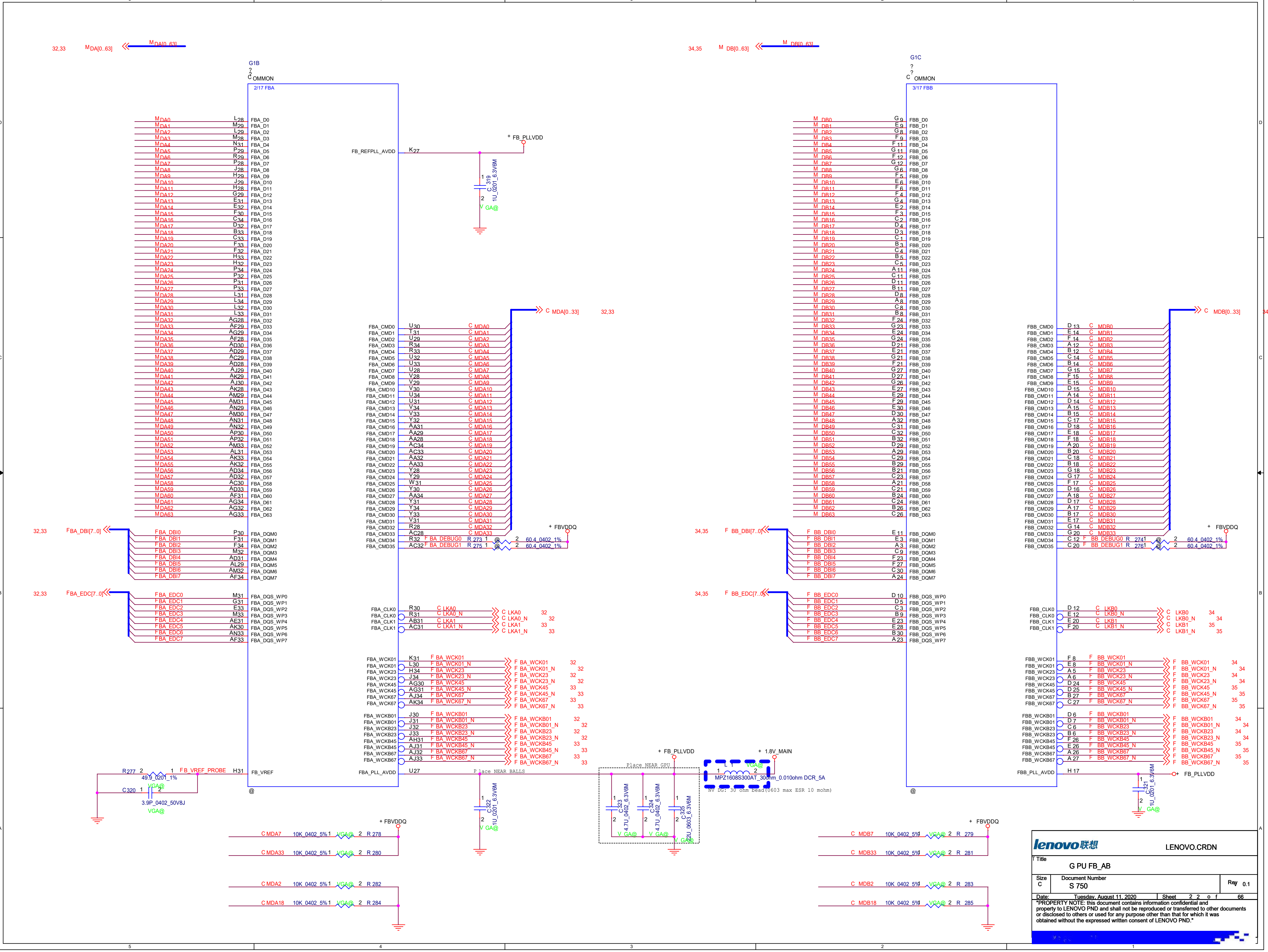

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Title: GPU FB_AB

Size: C

Document Number: S750

Rev: 0.1

Date: Tuesday, August 11, 2020

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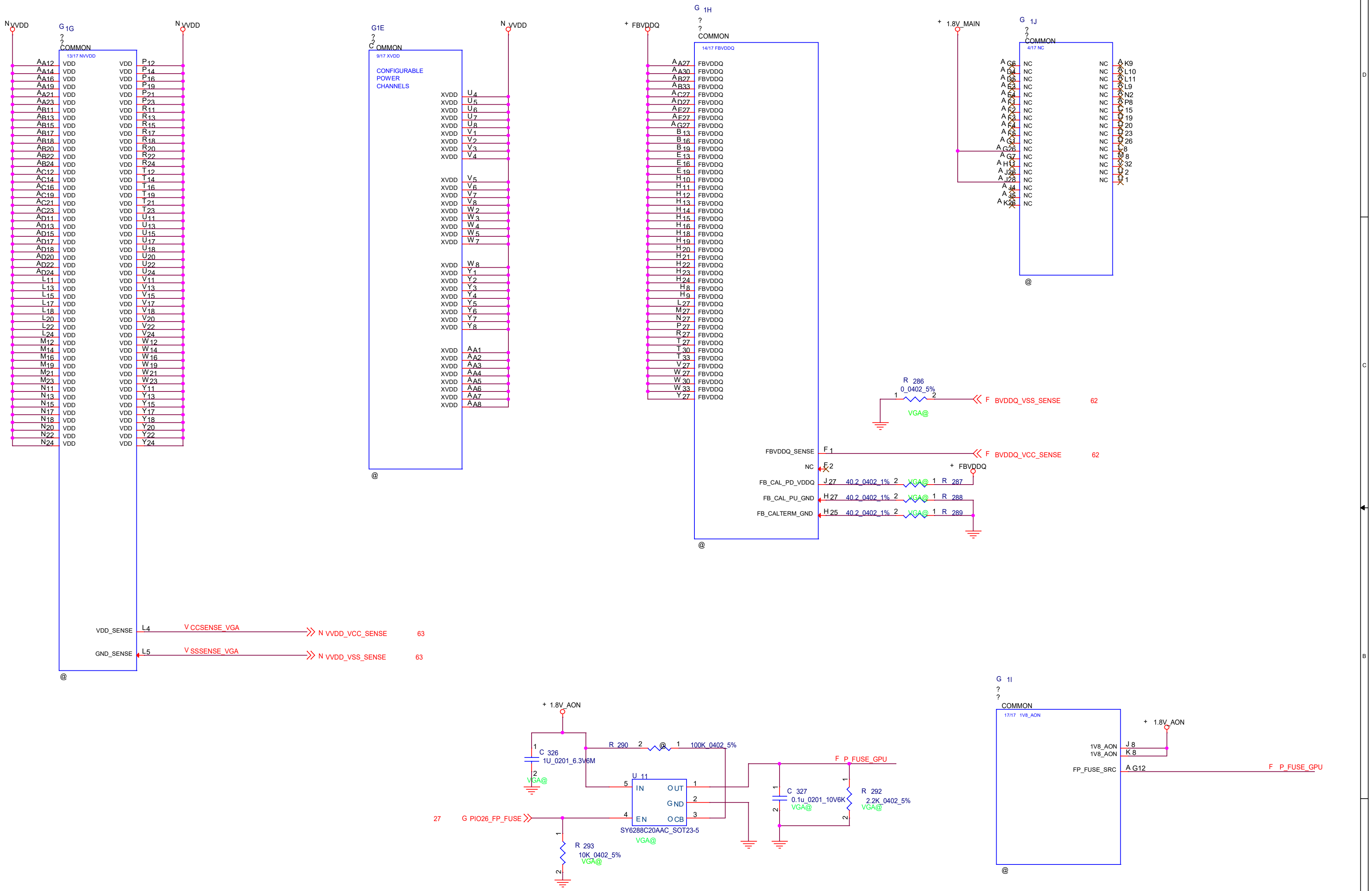

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Title: GPU PWR

Size: C
Document Number: S750
Rev: 0.1

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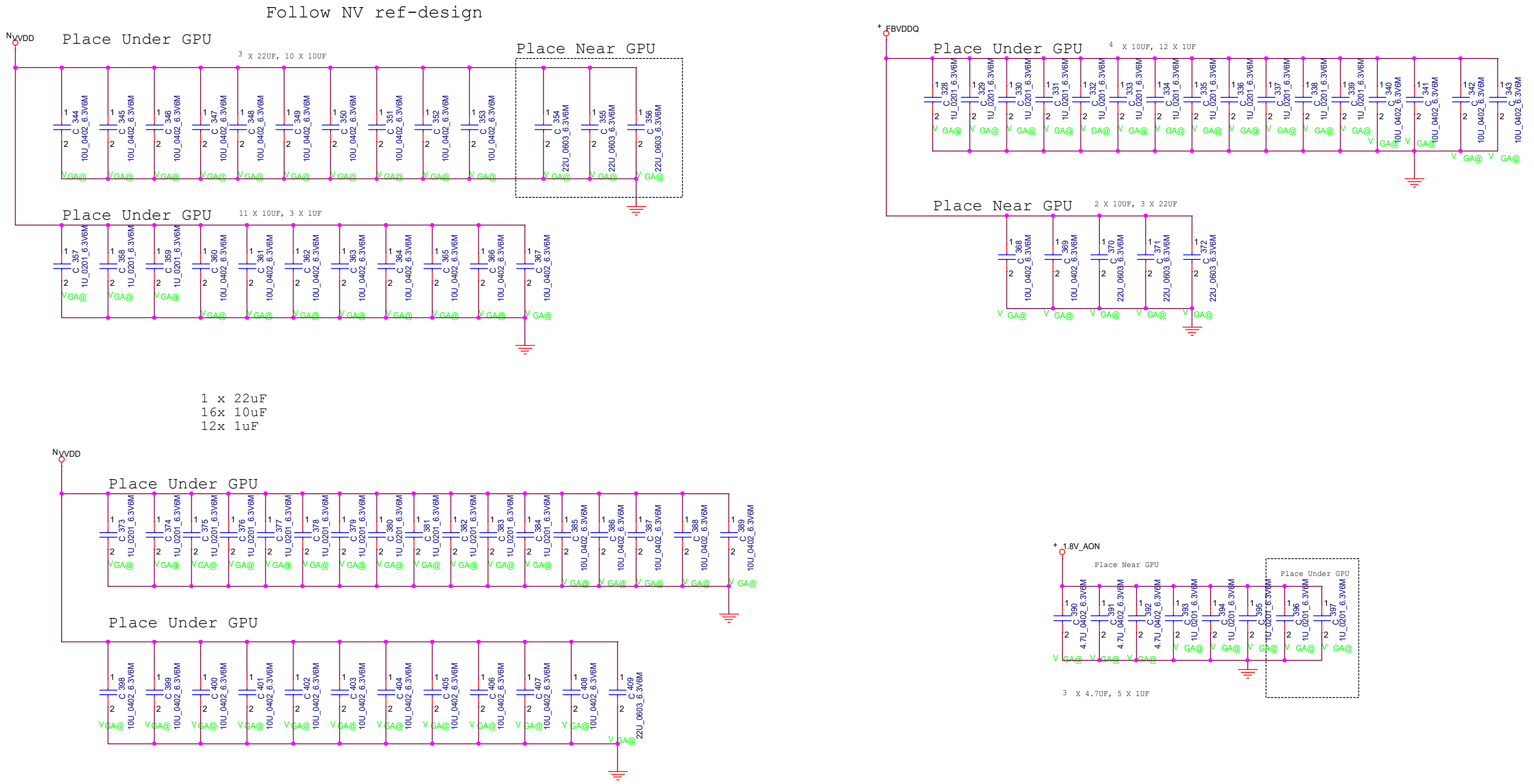

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Title: G PU Decoupling

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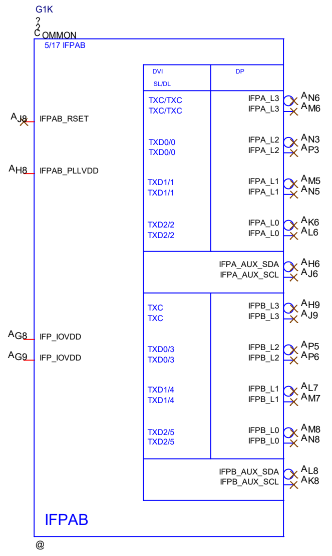

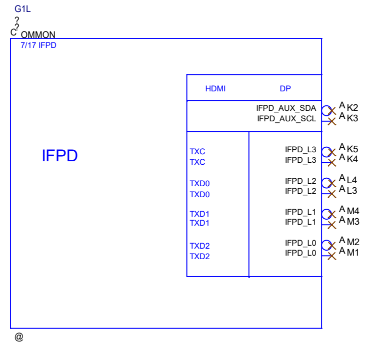

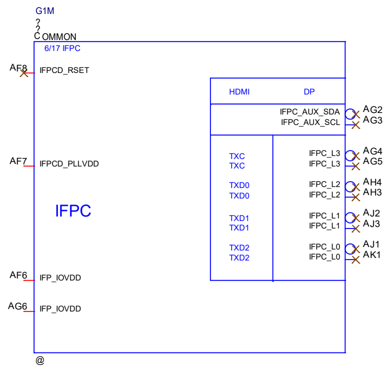

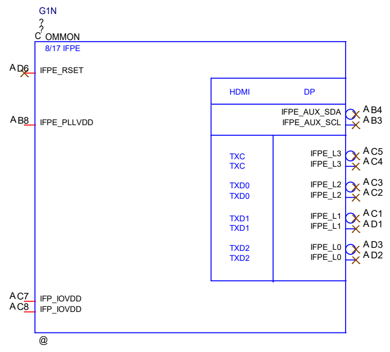

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Title: G PU IFP ABCDE

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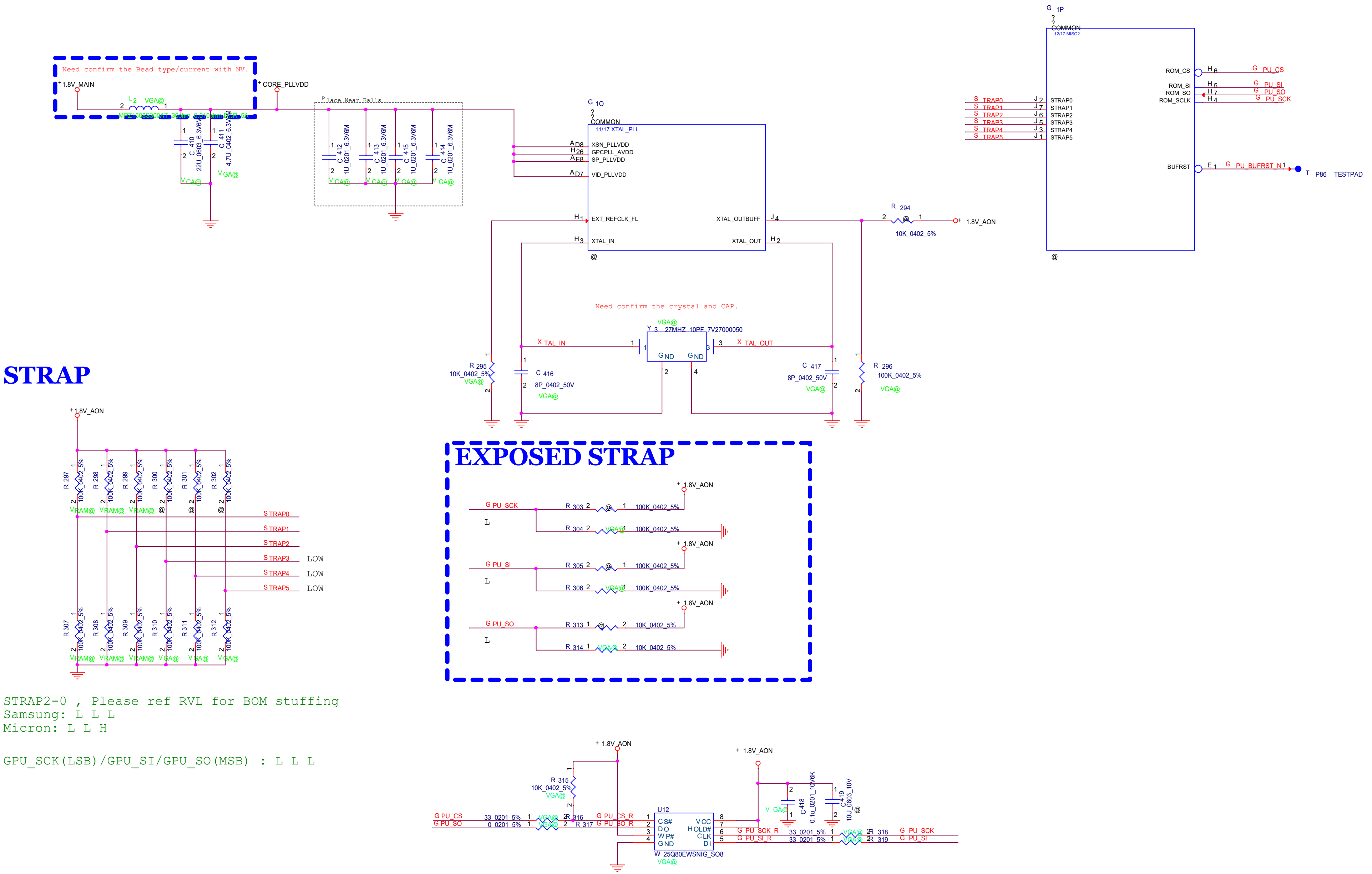

STRAP2-0 , Please ref RVL for BOM stuffing
Samsung: L L L
Micron: L L H

GPU_SCK(LSB)/GPU_SI/GPU_SO(MSB) : L L L

GDDR6 RAM_CFG

GPU	Memory Type	FBVDD/ FBVDDQ	Memory Density	Memroy configuration	Vendor	Manufacturer Part Number	Die Revision	Memory Speed CK Grade	Memory D/C Minimum	Strap	Strap2	Strap1	Strap0	Status
N18P-G62/G61	GDDR6	1.20V and 1.25V	8Gb	2chx256Mx16	Micron	MT61K256M32JE-14:A	A-die	14 Gbps	N/A	0x1	L	L	H	Prodution Candidate
					Samsung	K4Z80325BC-HC14	C-die	14 Gbps	N/A	0x0	L	L	L	Prodution Candidate

GDDR6 RAM_CFG

GPU	Memory Type	FBVDD/ FBVDDQ	Memory Density	Memroy configuration	Vendor	Manufacturer Part Number	Die Revision	Memory Speed CK Grade	Memory D/C Minimum	Strap	Strap2	Strap1	Strap0	Status
N18S-G5	GDDR6	1.20V	8Gb	2chx256Mx16	Micron	MT61K256M32JE-14:A	A-die	14 Gbps	1940	0x1	L	L	H	Prodution Candidate
					Samsung	K4Z80325BC-HC14	C-die	14 Gbps	2001	0x0	L	L	L	Prodution Candidate

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Title: G PU PLL/XTAL

Size: C | Document Number: S 750 | Rev: 0.1

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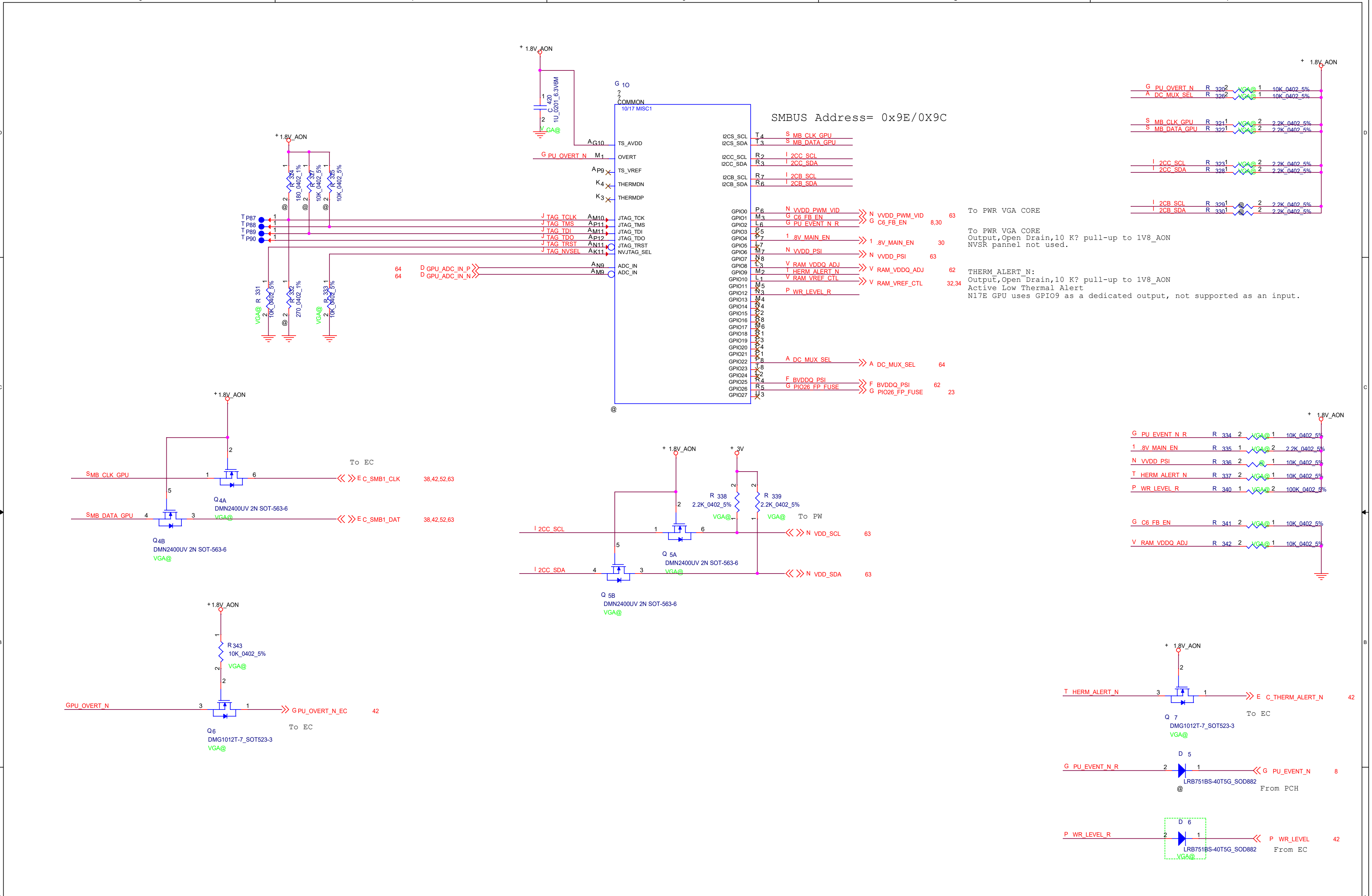
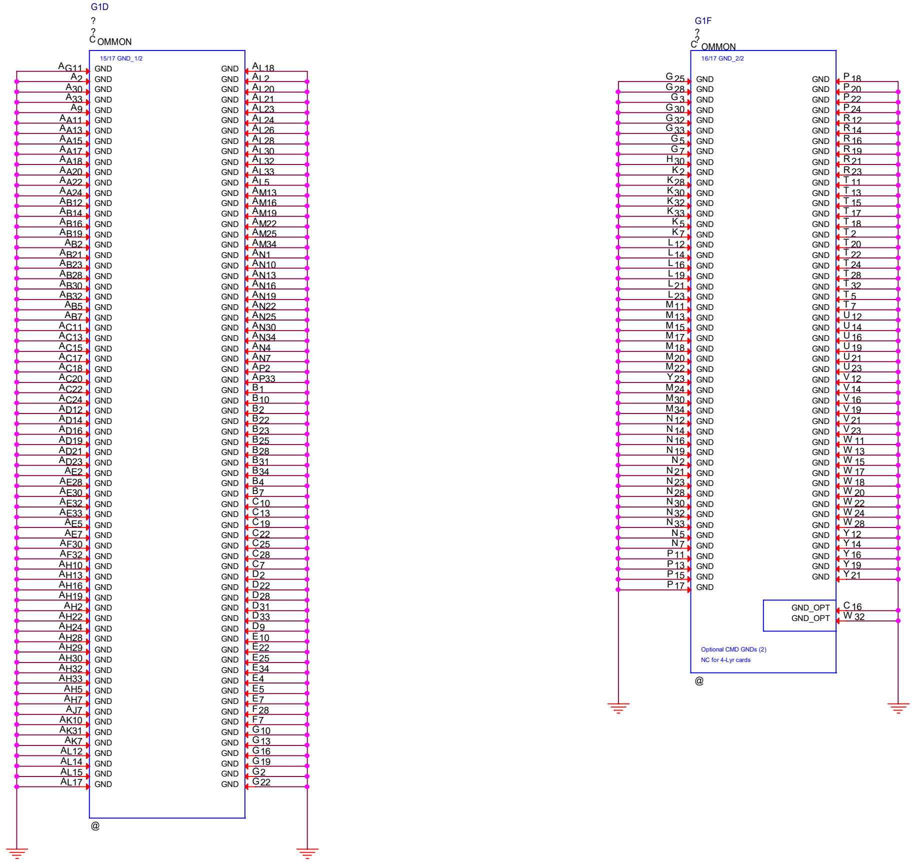


lenovo联想	LENOVO.CRDN	
Title	GPU GPIO	
Size C	Document Number S750	Rev 0.1
Date: Friday, August 07, 2020	Sheet 27 of 66	



lenovo联想

LENOVO.CRDN

Title: GPU GND

Size: C

Document Number: S750

Rev: 0.1

Date: Friday, August 07, 2020

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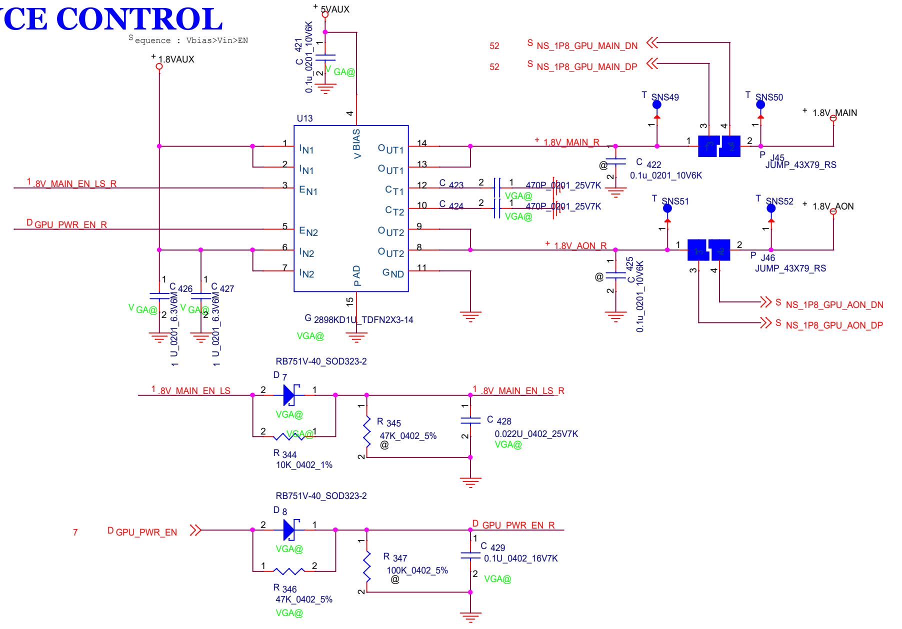
POWER SEQUENCE CONTROL



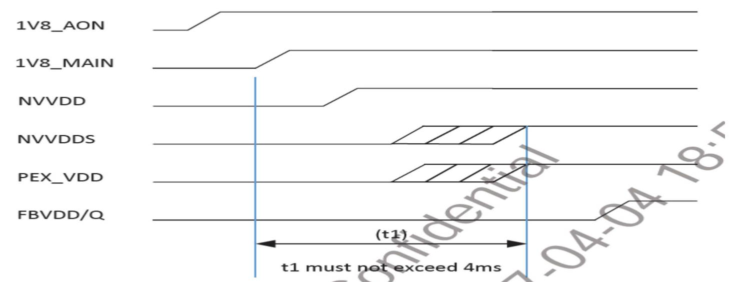


Figure 7.5 Example of Power-Up Sequencing Order

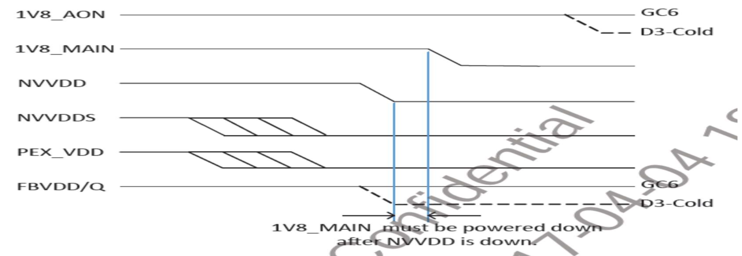
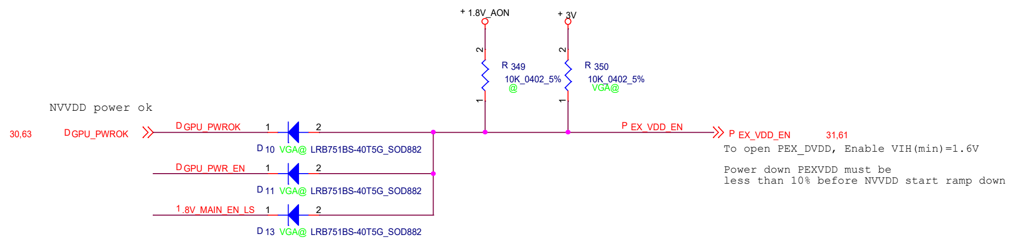
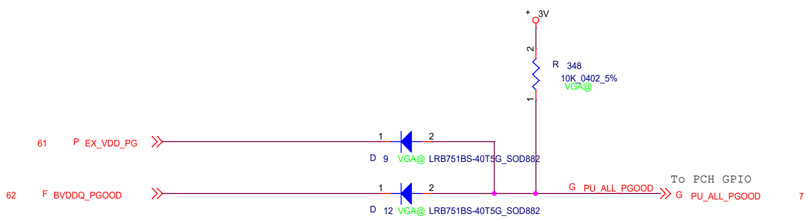
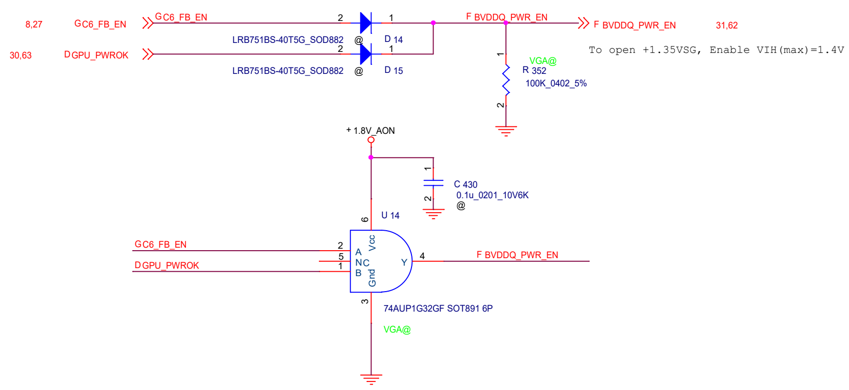


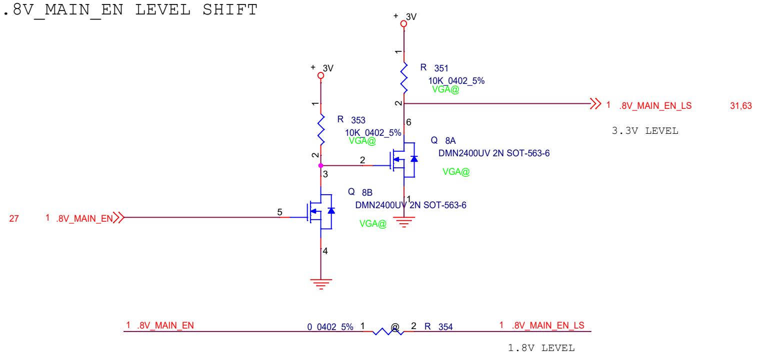
Figure 7.6 Example of Power-Down Sequencing Order







1.8V_MAIN_EN LEVEL SHIFT



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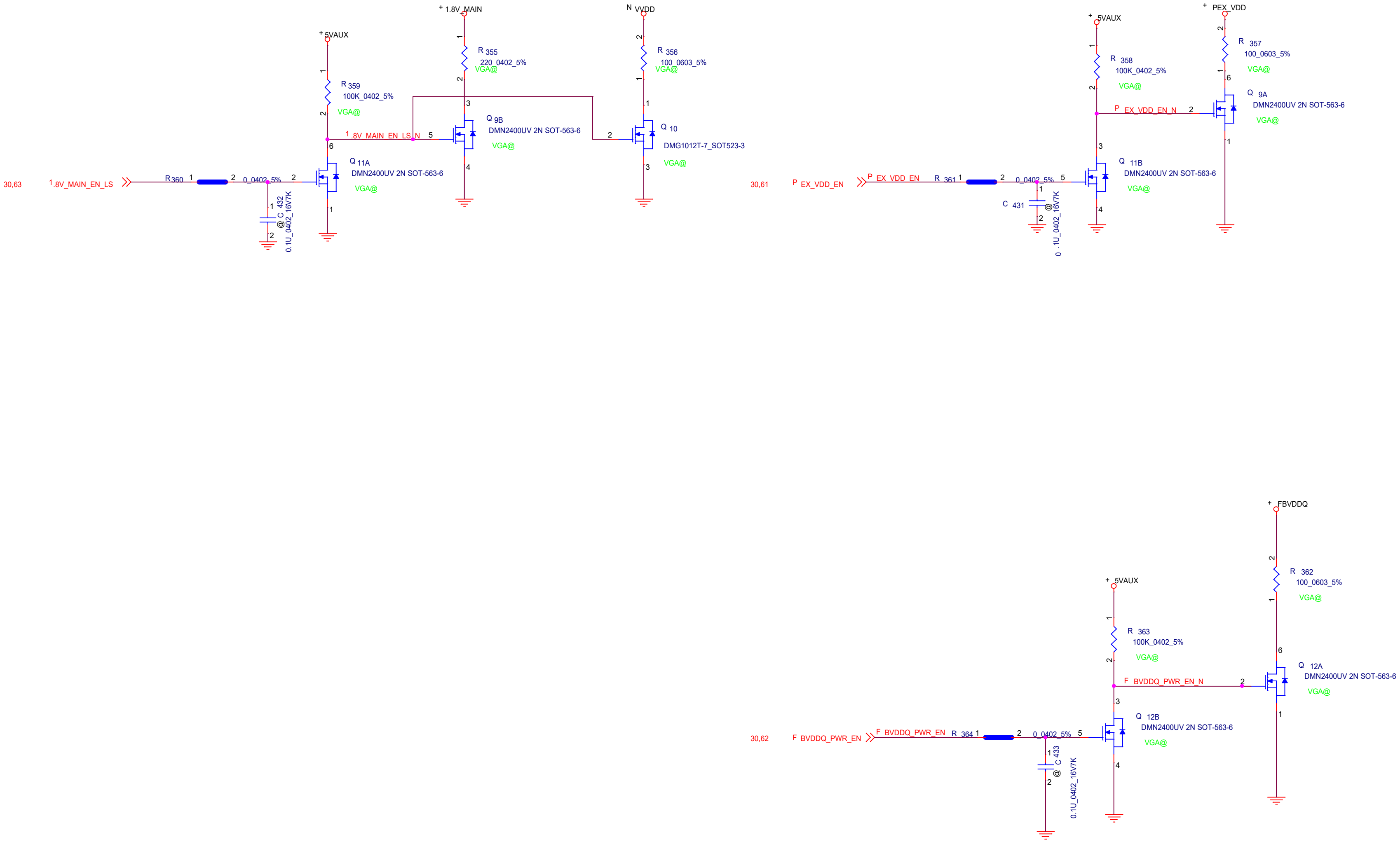
Title: GPU Switch/Thermal

Size	Document Number	Rev
C	S 750	0.1

Date: Friday, August 07, 2020 Sheet 30 of 66



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Title: G PU POWER DISCHARGE

Size	Document Number	Rev
C	S 750	0.1

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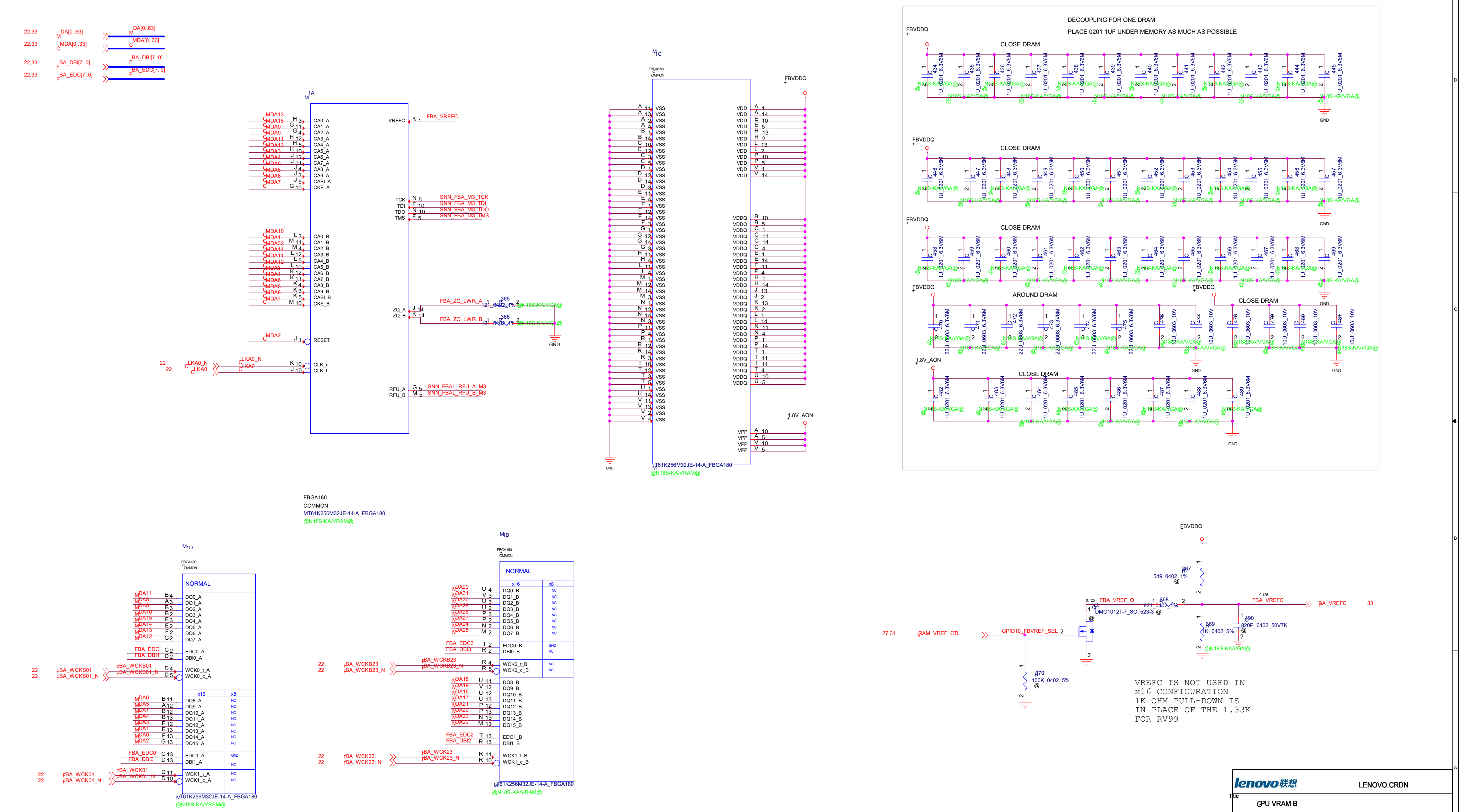
MEMORY: FBA Partition 31..0



VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR RV99

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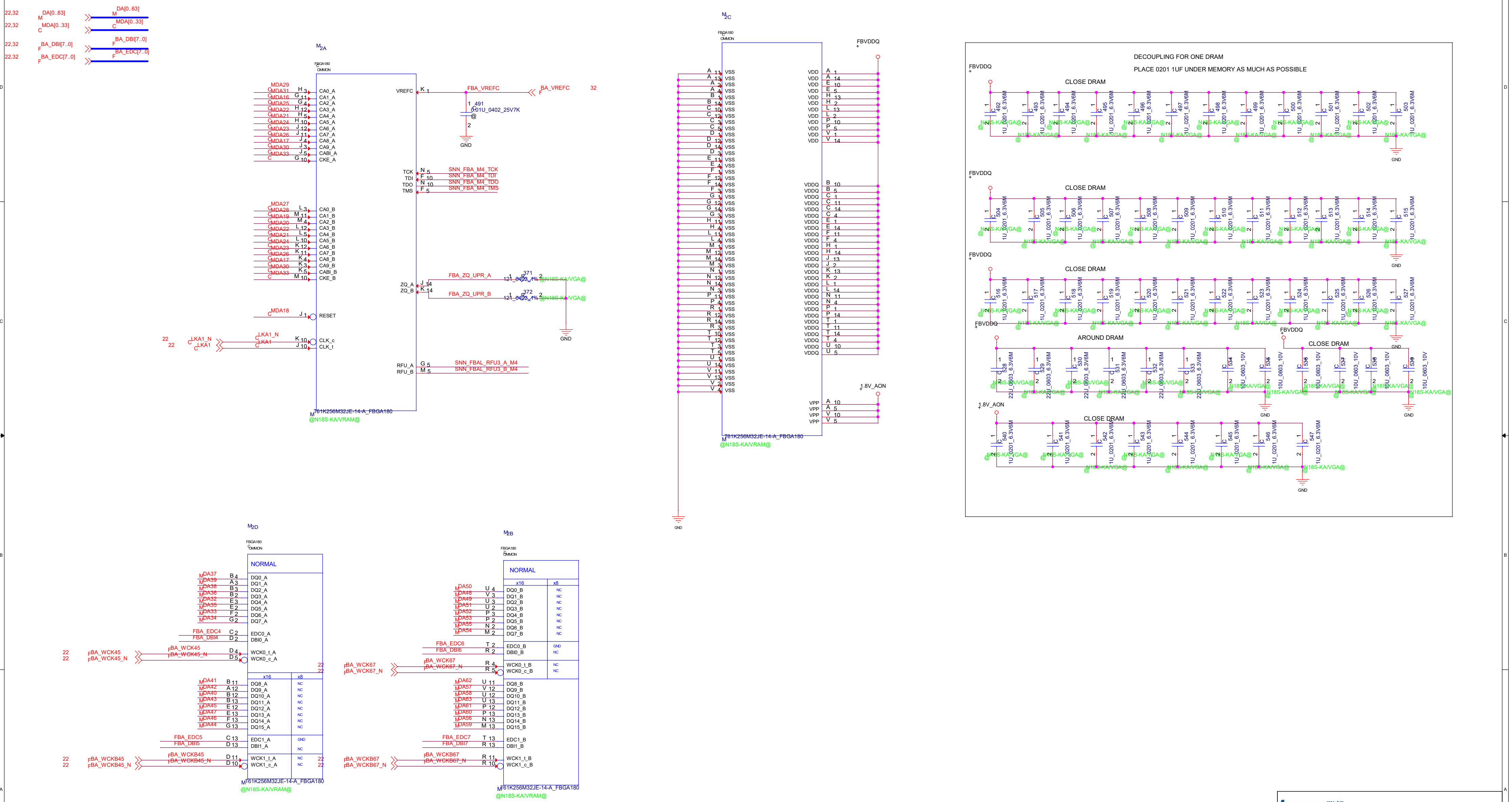
Title: GPU VRAM B

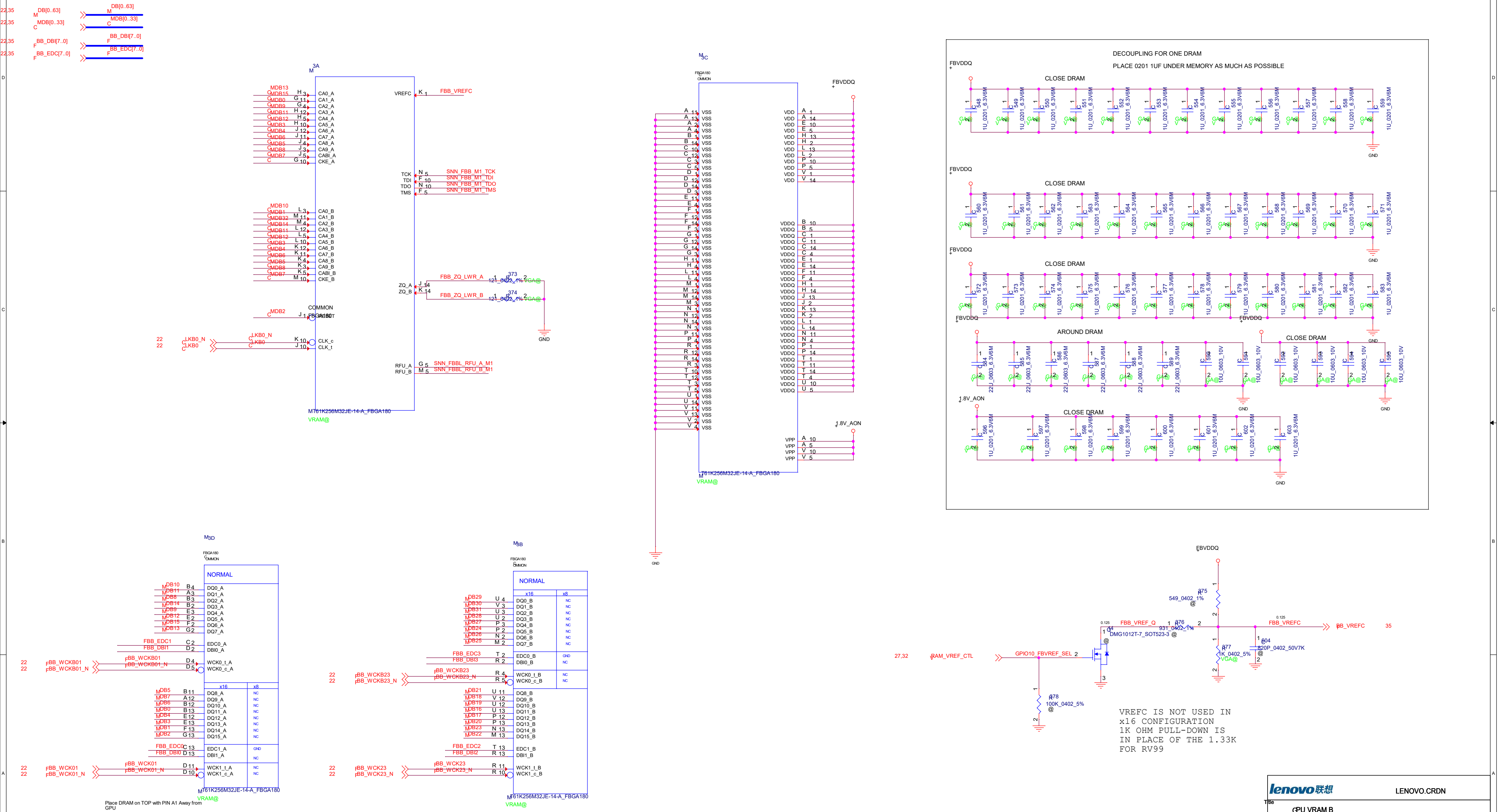
Size: Custom | Document Number: S750 | Rev: 0.1

Date: Friday, August 07, 2020 | Sheet 32 of 66

MEMORY: FBA Partition 63..32



MEMORY: FBB Partition 31..0



VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR RV99

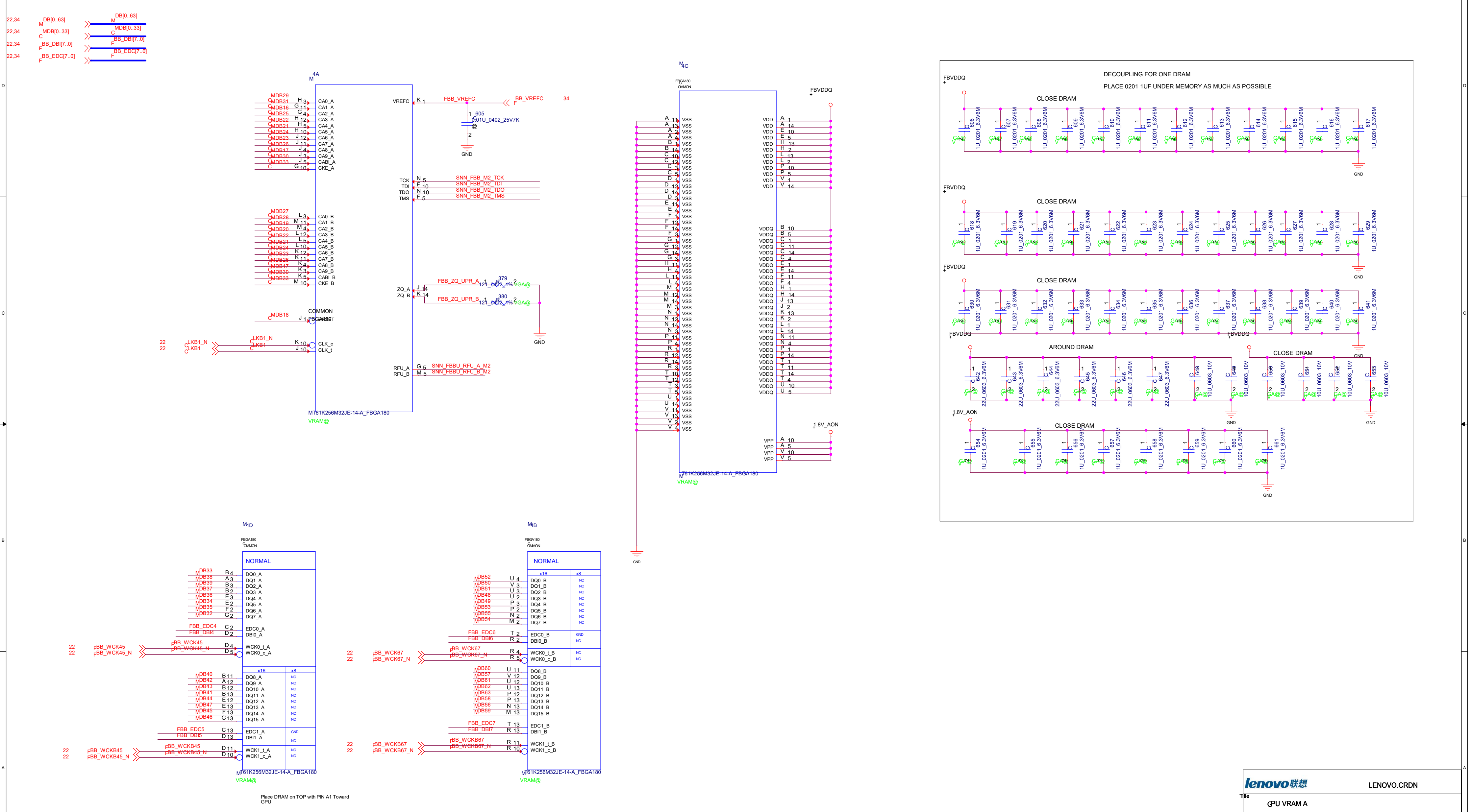
lenovo联想 LENOVO.CRDN

Title: GPU VRAM B

Size: Custom | Document Number: S750 | Rev: 0.1

Date: Friday, August 07, 2020 | Sheet 34 of 66

MEMORY: FBB Partition 63..32



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Title: GPU VRAM A

Size: Custom | Document Number: S750 | Rev: 0.1

Date: Friday, August 07, 2020 | Sheet 35 of 66

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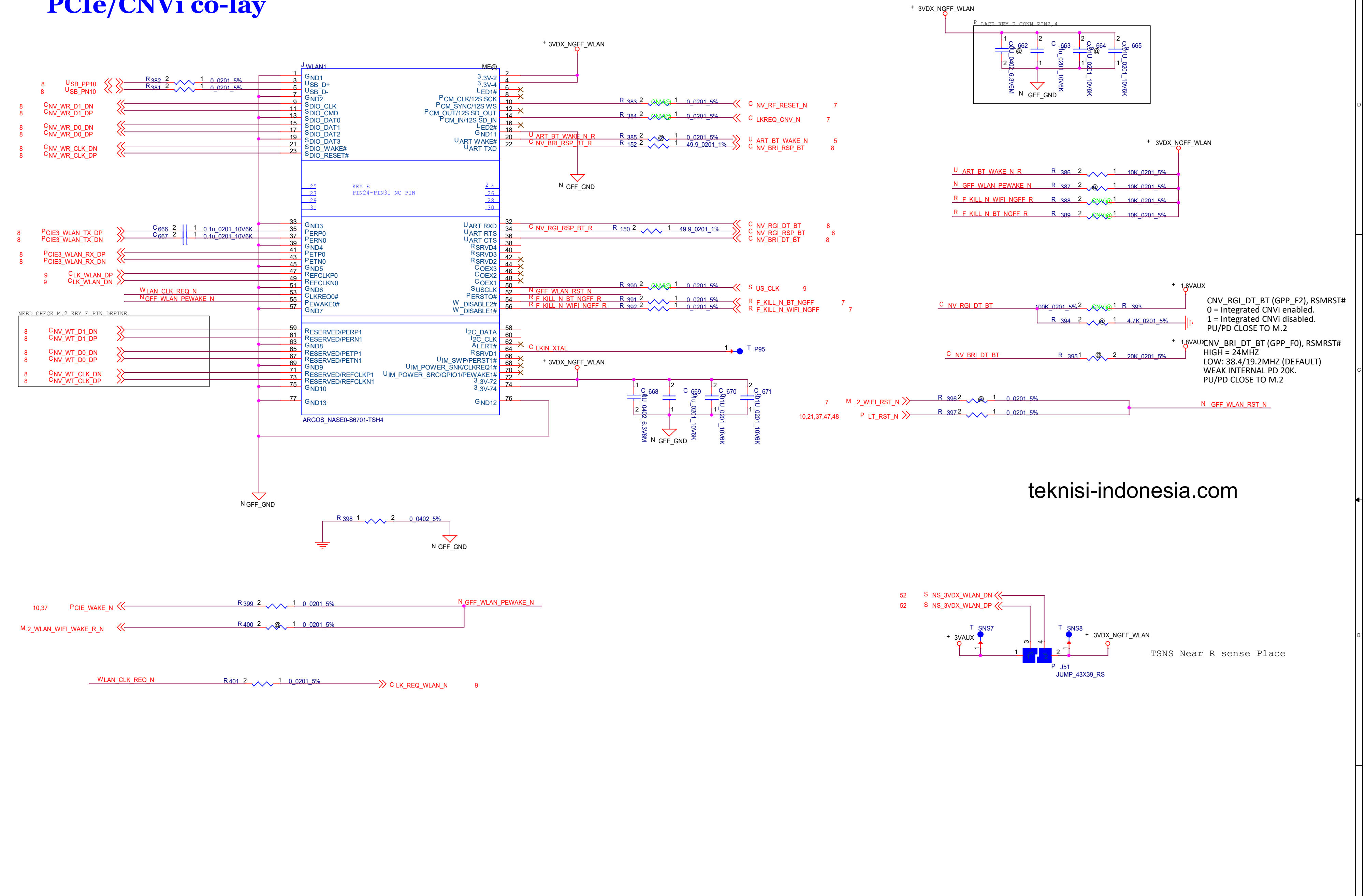
PCIe/CNVi co-lay

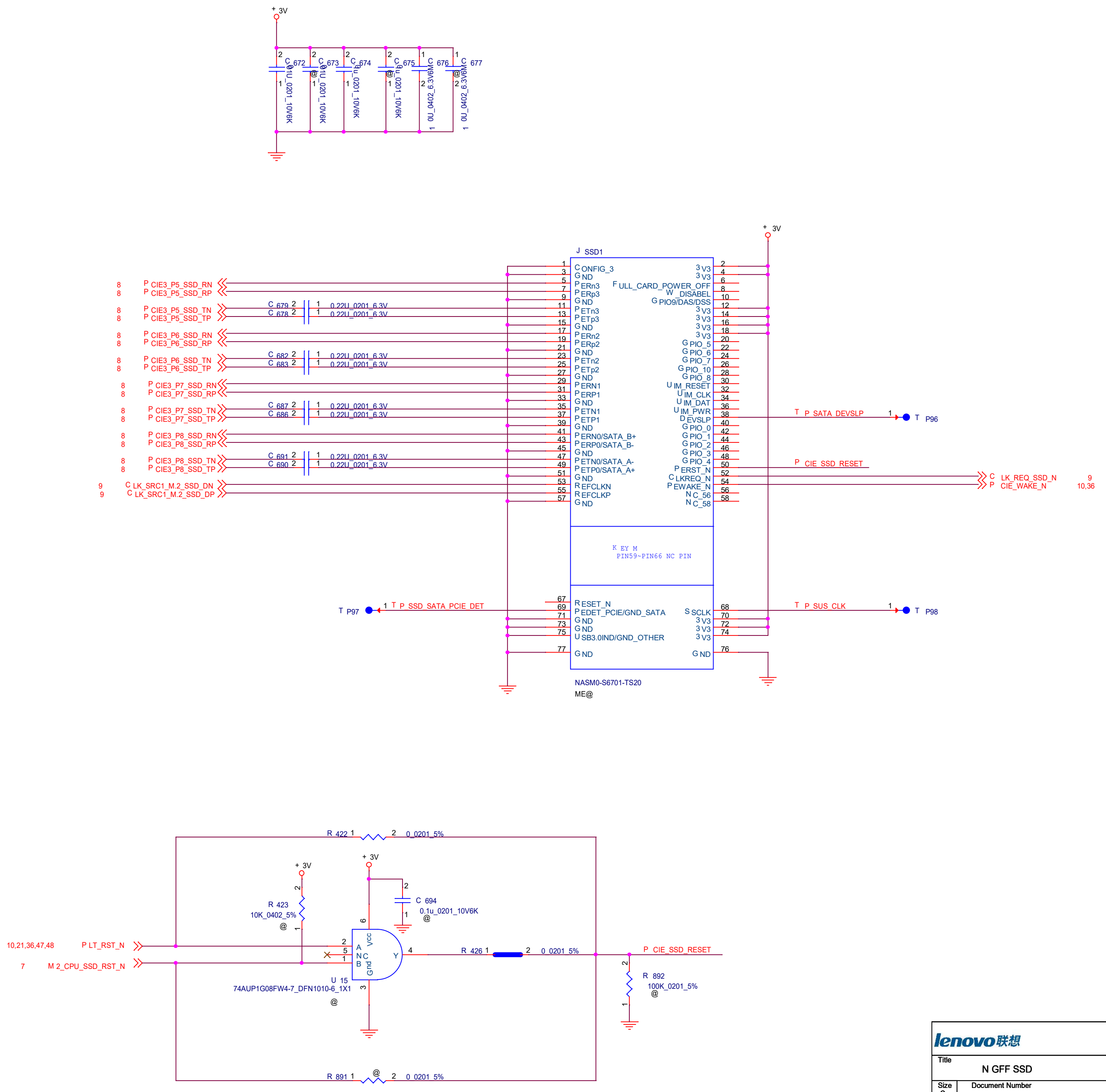


lenovo联想 LENOVO.CRDN

Title: NGFF WLAN

Size: C | Document Number: S 750 | Rev: 0.5

Date: Friday, August 07, 2020 | Sheet 36 of 66

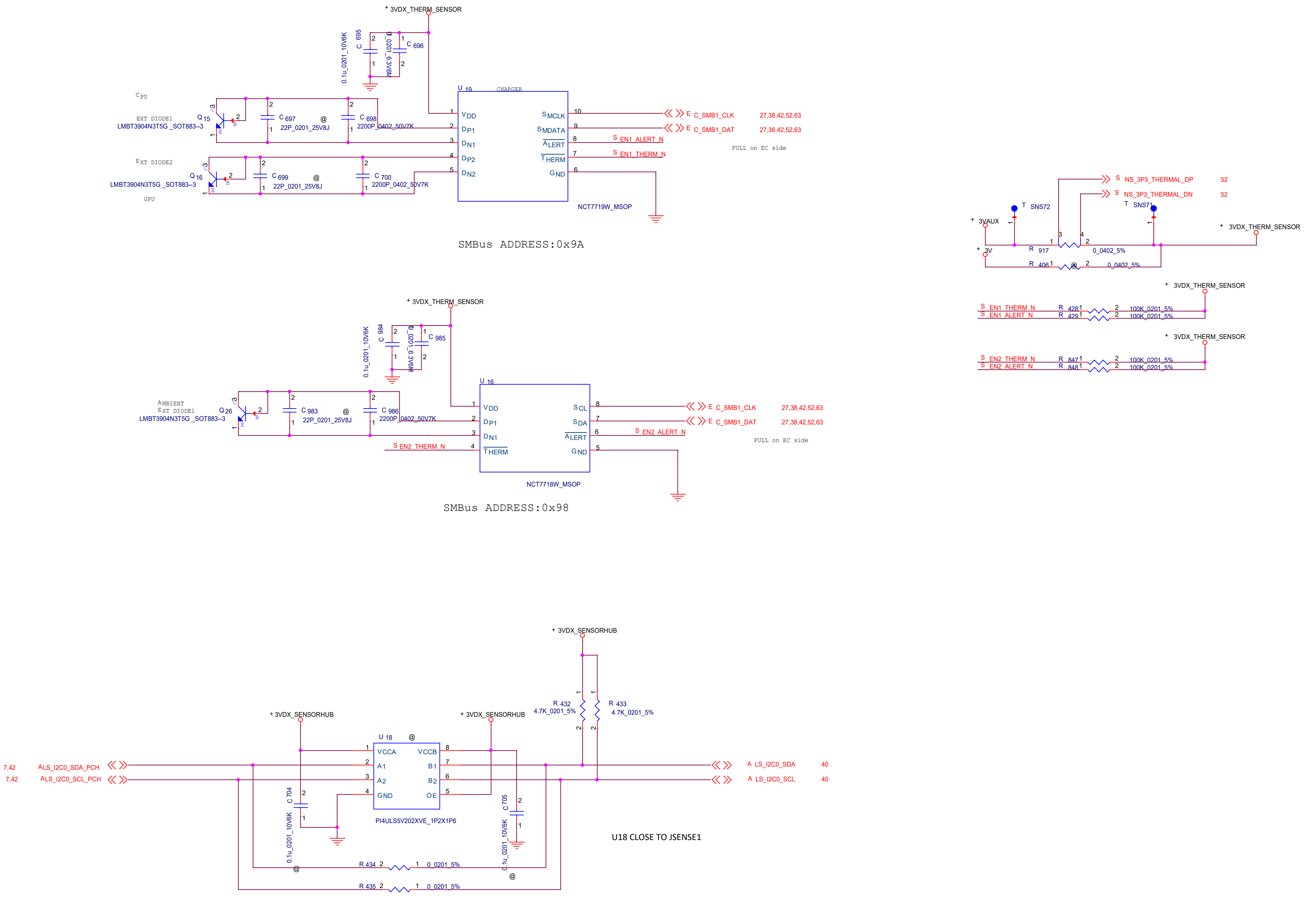


LENOVO.CRDN

Title: NGFF SSD

Size	Document Number	Rev
C	S750	0.5

Date: Friday, August 07, 2020 Sheet 37 of 66



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Title: Sensor

Size: C | Document Number: S750 | Rev: 0.5

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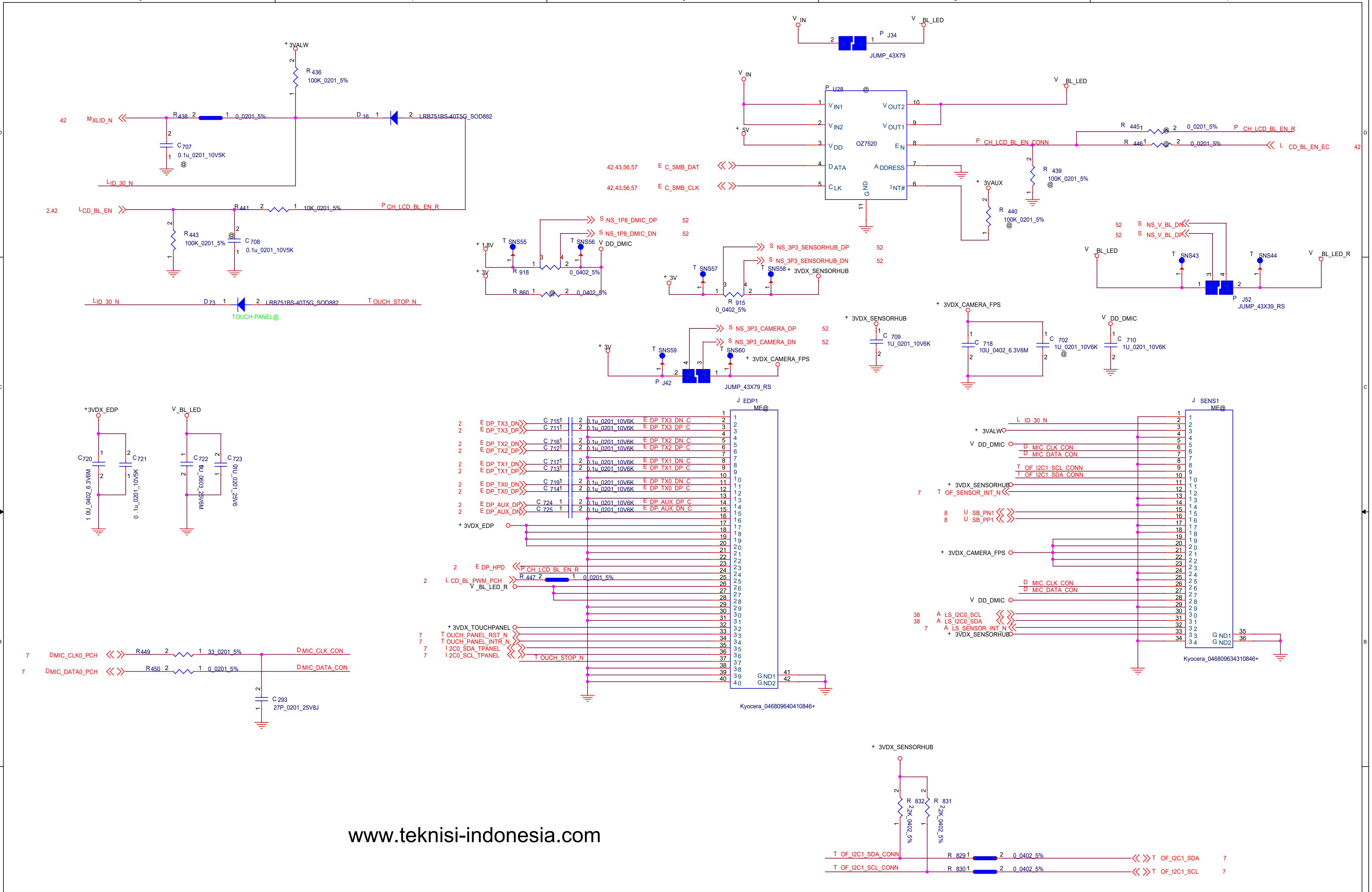
LENOVO.CRDN

Title

R ESERVED

Size	Document Number	Rev
C	S 750	1.0

Date: Friday, August 07, 2020 Sheet 39 of 66

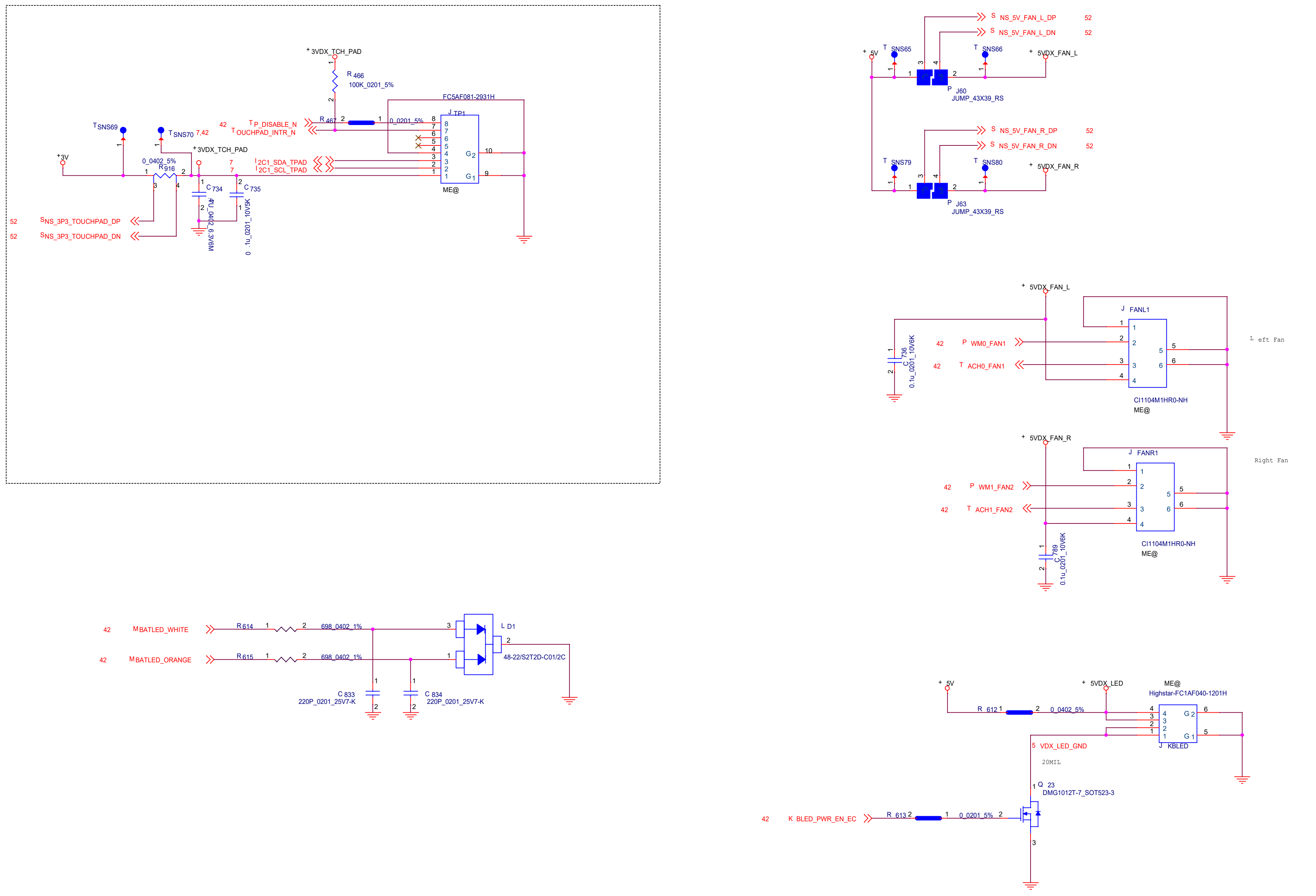


LENOVO.CRDN

Title: EDP/CAMERA

Size: C | Document Number: S 750 | Rev: 0.5

Date: Friday, August 07, 2020 | Sheet 40 of 66

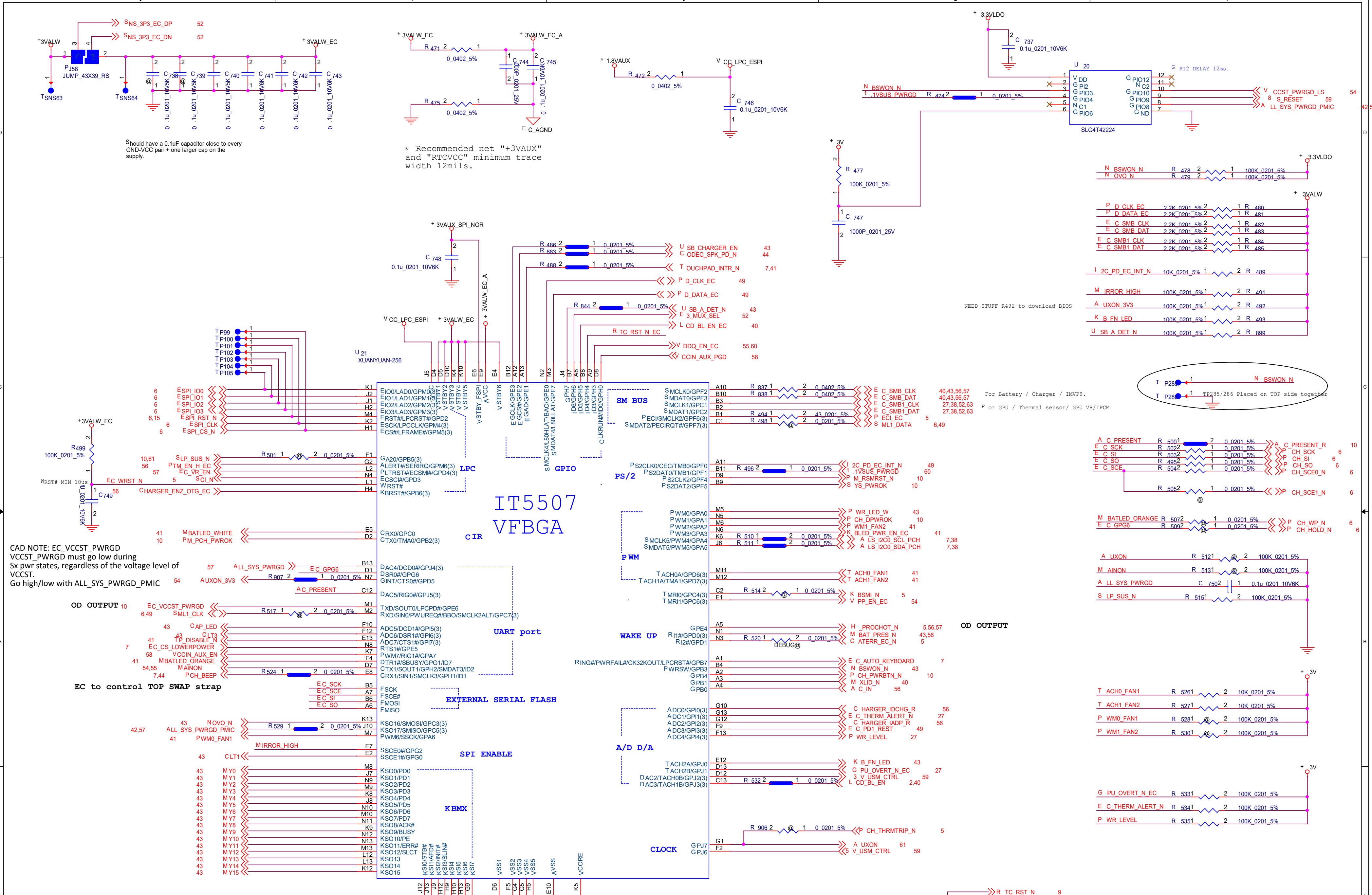


lenovo联想 LENOVO.CRDN

Title: TP/FAN/KB LED

Size: C | Document Number: S750 | Rev: 0.5

Date: Friday, August 07, 2020 | Sheet 41 of 66



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Title	EC	
Size C	Document Number S 750	Rev 0.5
Date: Friday, August 07, 2020	Sheet 42 of 66	

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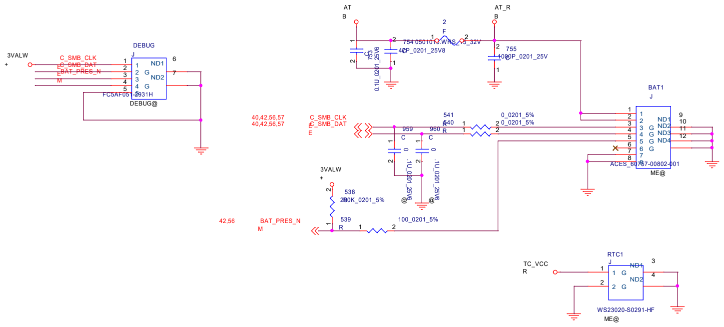
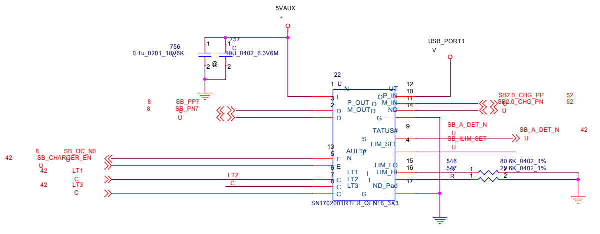
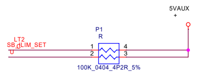
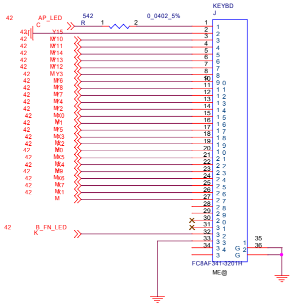




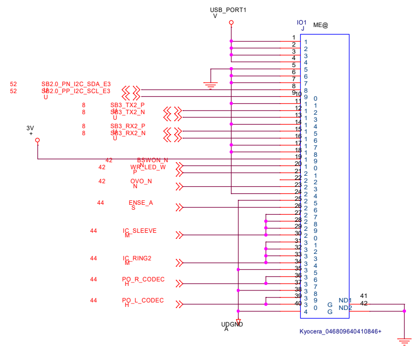


Install ILIM_SEL shunt for ILIM = ILIM_LO = 0.63A
Remove ILIM_SEL shunt for ILIM =ILIM_HI = 2.3A
Support Mouse/Keyboard wake up.
Support Power Wake

CLT1	CLT3		
1	0	--	SDP
0	1	--	DCP/Auto
1	1	--	CDP



KB PIN DEFINE TBD



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Title: CONNECTOR

Size: D Document Number: S750 Rev: 0.5y

Date: Friday, August 07, 2020 Sheet 43 of 66

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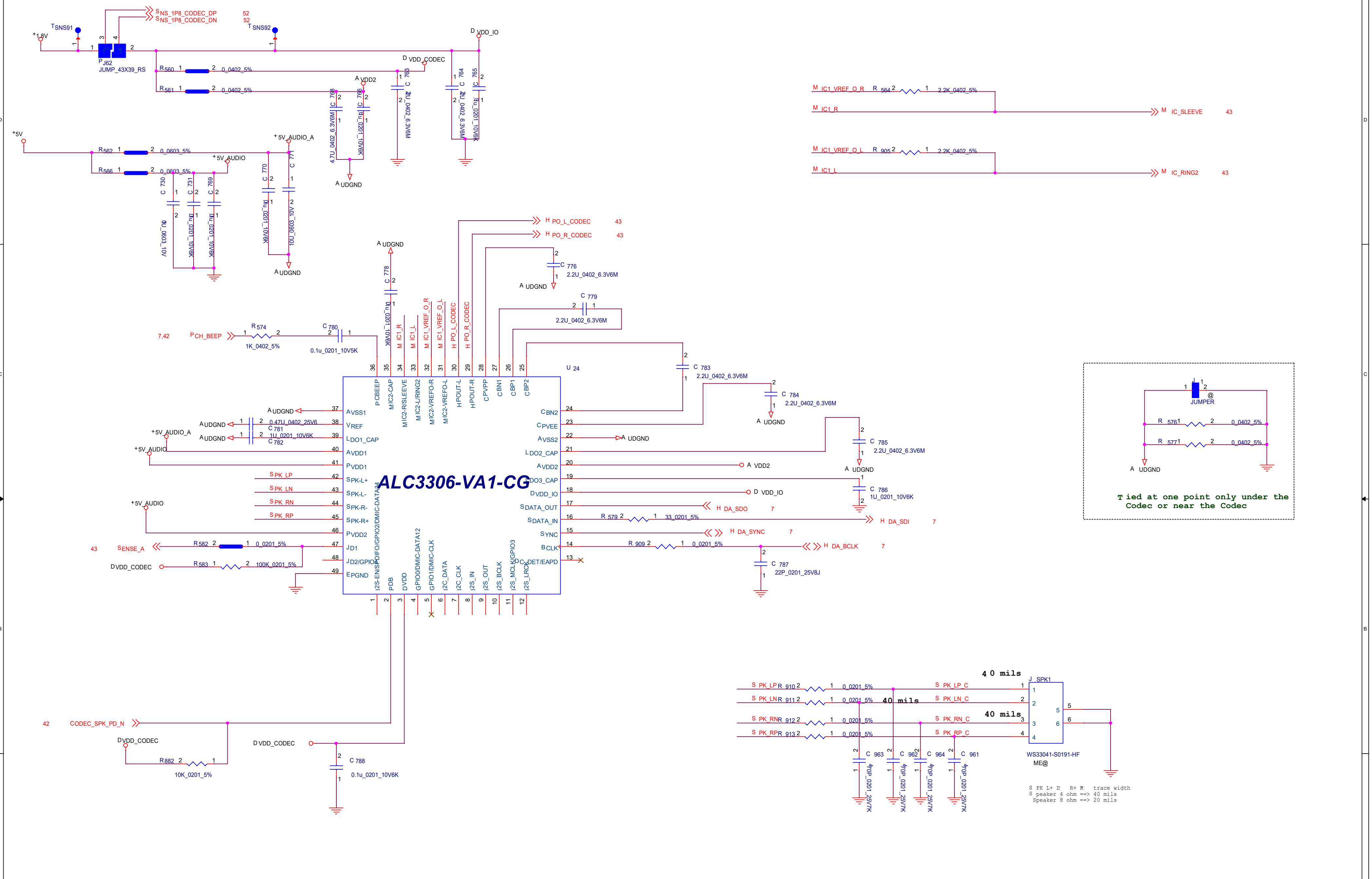

lenovo联想 LENOVO.CRDN

Title: Audio

Size: C | Document Number: S750 | Rev: V0.5

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5 4 3 2 1

D C B A

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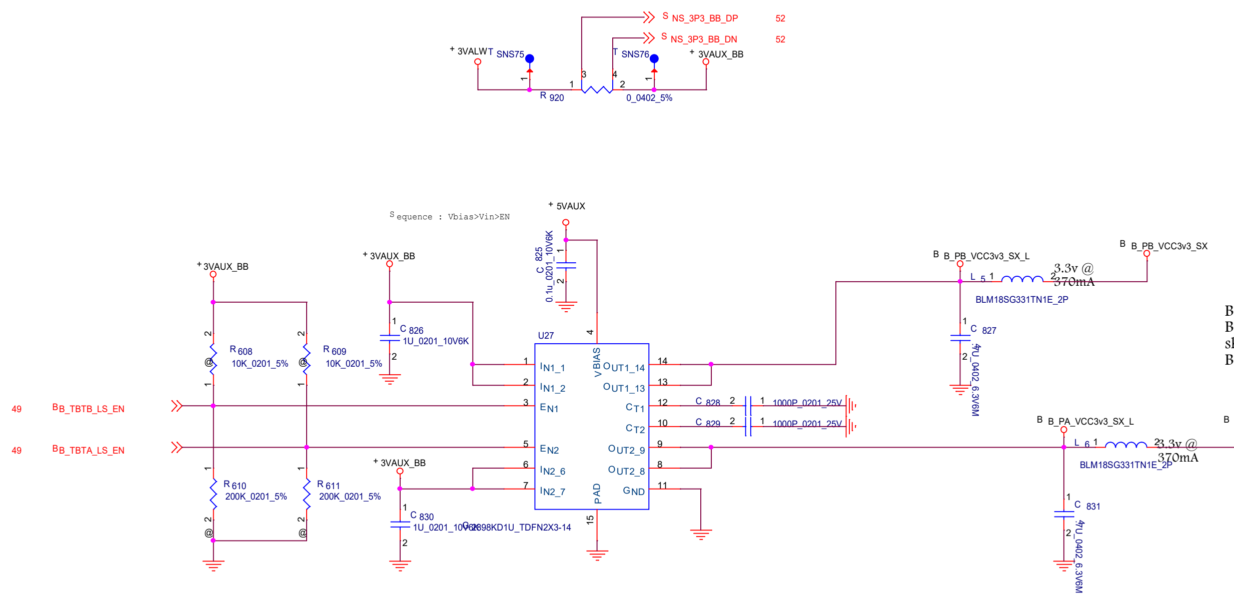
Title
B LANK

Size	Document Number	Rev
C	S 750	V 0.5

Date: Friday, August 07, 2020 Sheet 4 5 o f 66



BB_PA_VCC3v3_SX Tolerance (+ 5%/-7.5%):
Burnside Bridge power pins which connected to BB_PA_VCC3v3_SX should be 3.465v maximum and 3.07v minimum for normal operation.
BB_PA_VCC3v3_SX ripple: 40mVp-p

BB_PB_VCC3v3_SX Tolerance (+ 5%/-7.5%):
Burnside Bridge power pins which connected to BB_PB_VCC3v3_SX should be 3.465v maximum and 3.07v minimum for normal operation.
BB_PB_VCC3v3_SX ripple: 40mVp-p

lenovo联想	LENOVO.CRDN	
Title	BBPOWSWITCH	
Size C	Document Number S750	Rev 0.5
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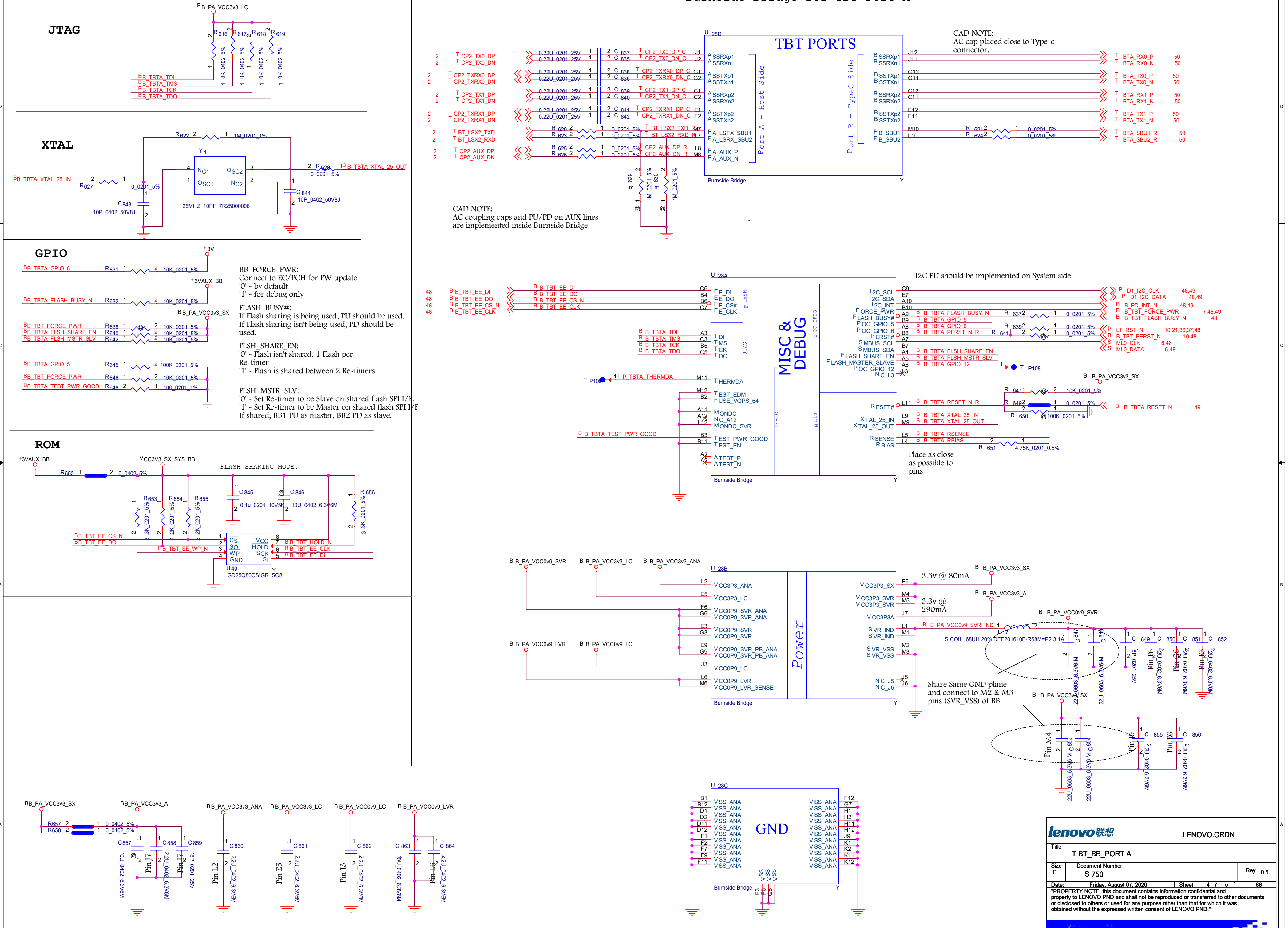
Burnside Bridge for TBT Port A



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Title	T BT_BB_PORT A	
Size C	Document Number S 750	Rev 0.5
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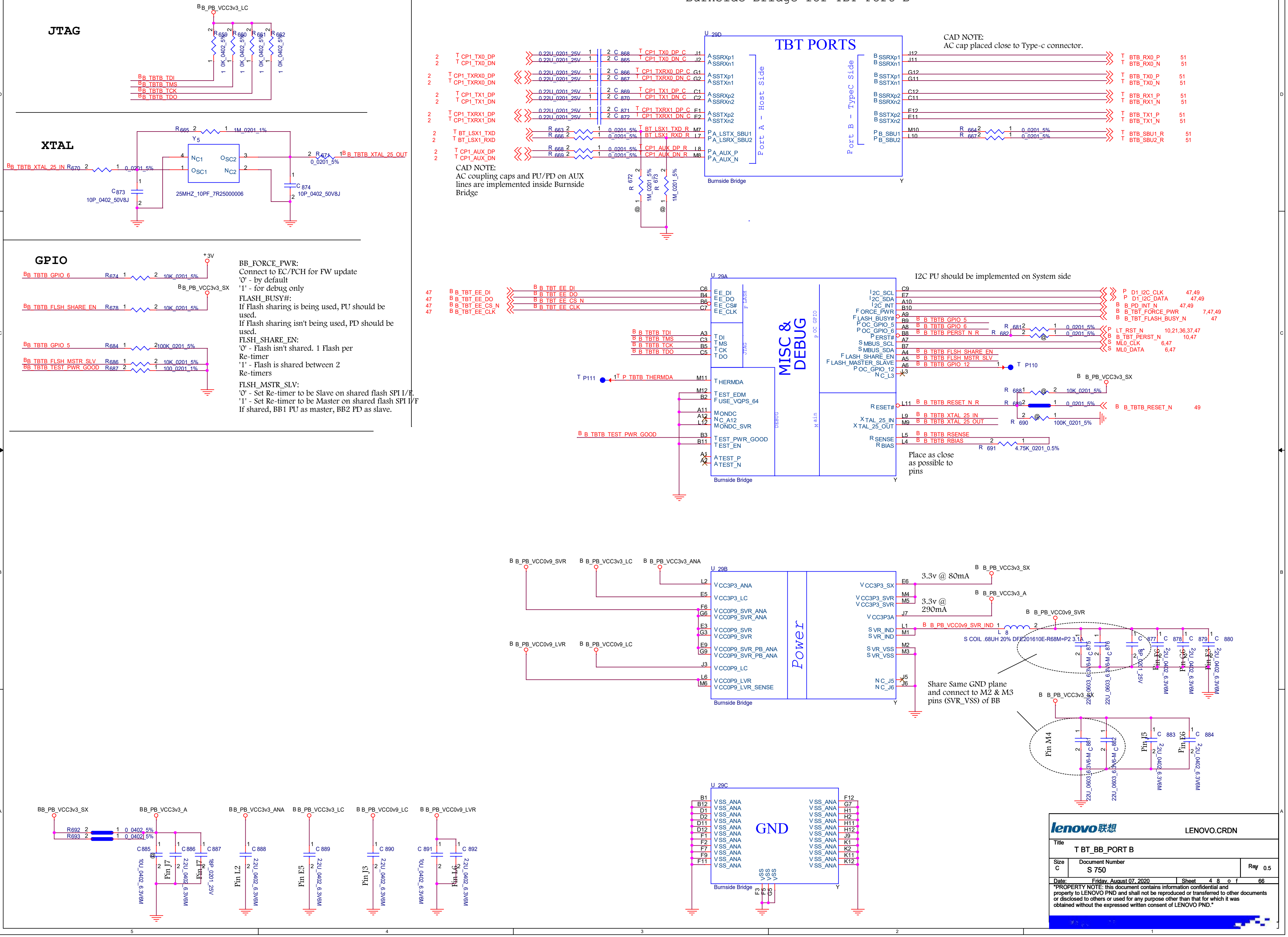
Burnside Bridge for TBT Port B



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Title: TBT_BB_PORT B

Size: C Document Number: S 750 Rev: 0.5

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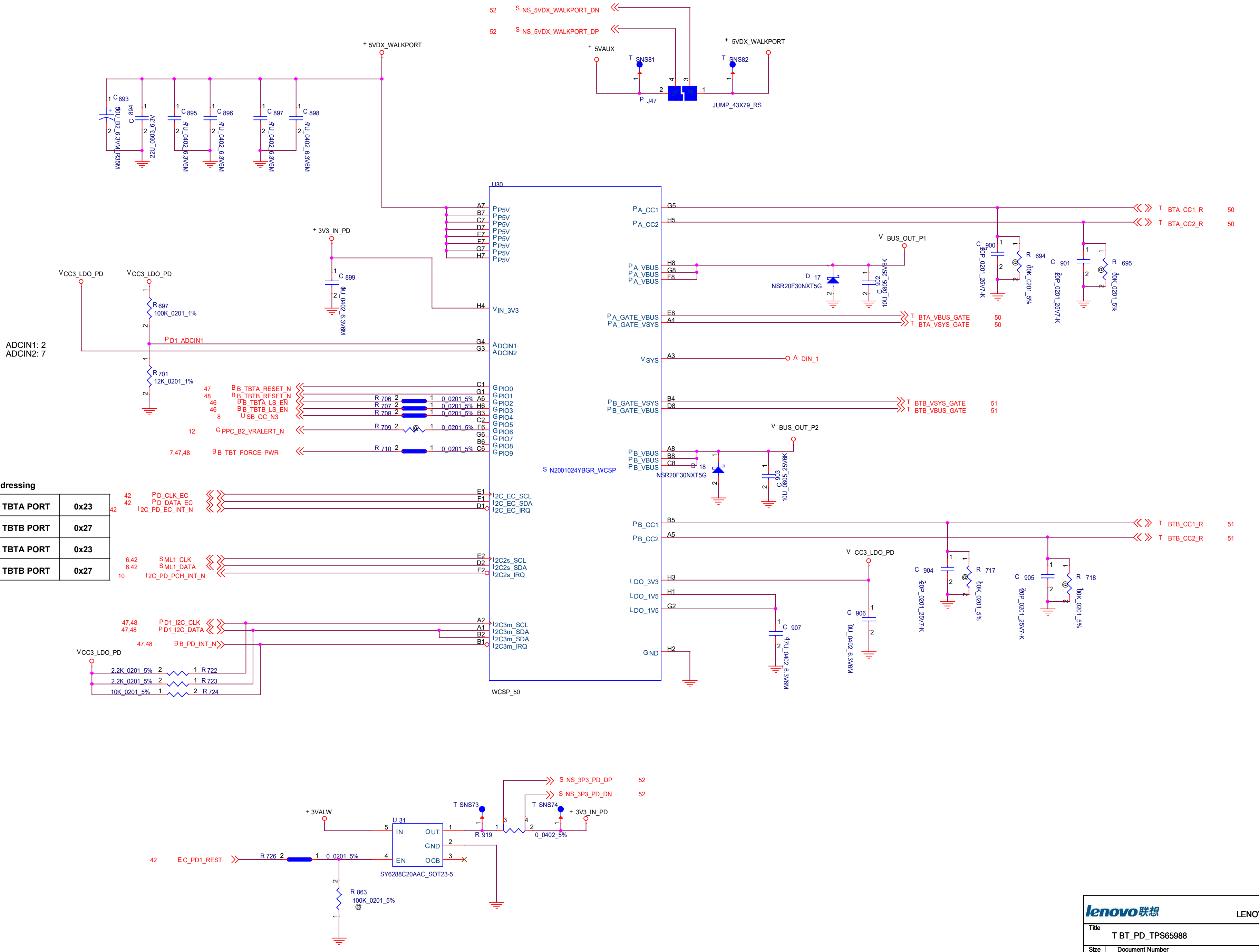

TABLE I2C Addressing

I2C1(to EC)	TBTA PORT	0x23
	TBTB PORT	0x27
I2C2(to PCH)	TBTA PORT	0x23
	TBTB PORT	0x27

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Title: TBT_PD_TPS65988

Size: C | Document Number: S750 | Rev: 0.5

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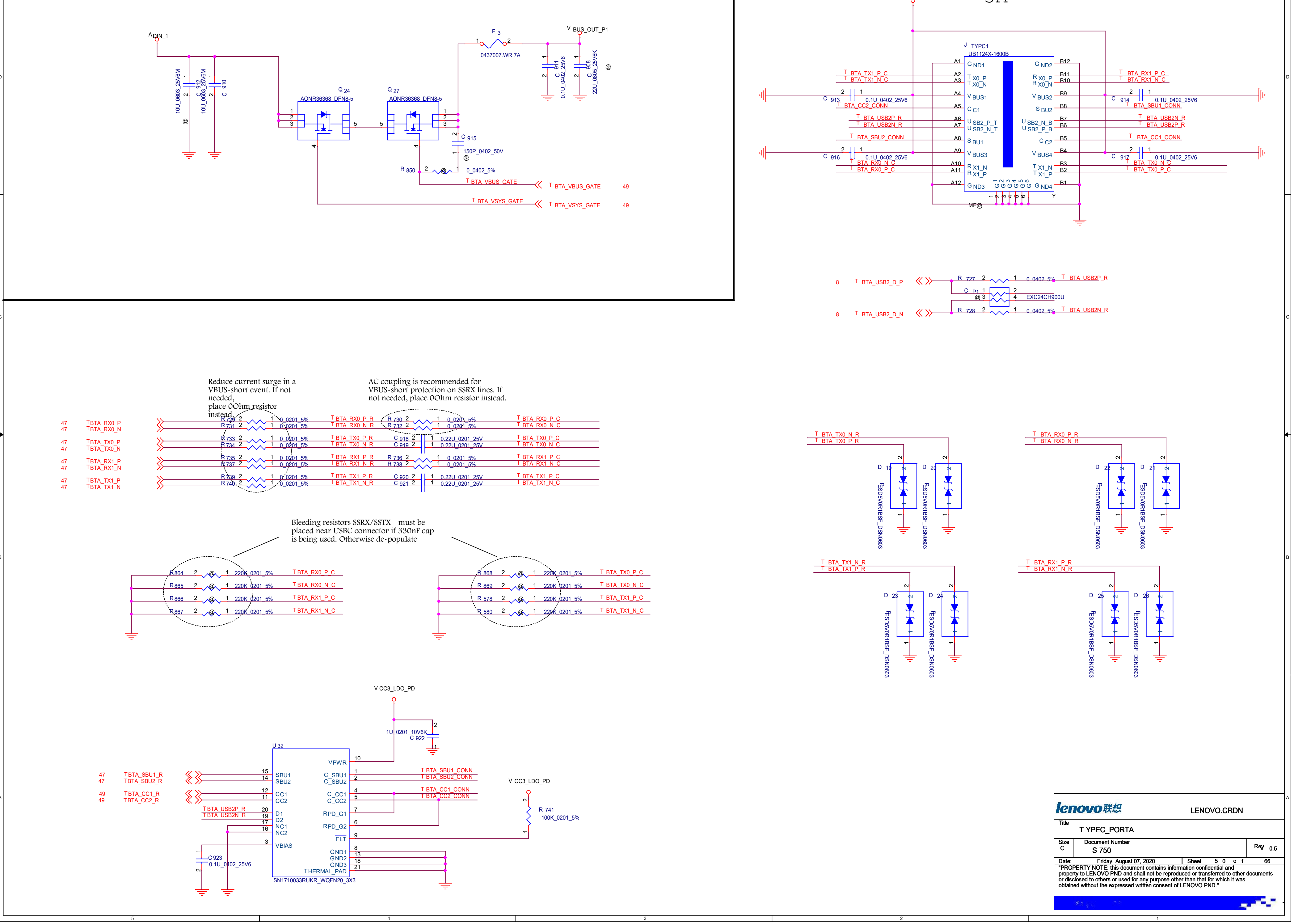
TBT A PORT VBUS SWITCH



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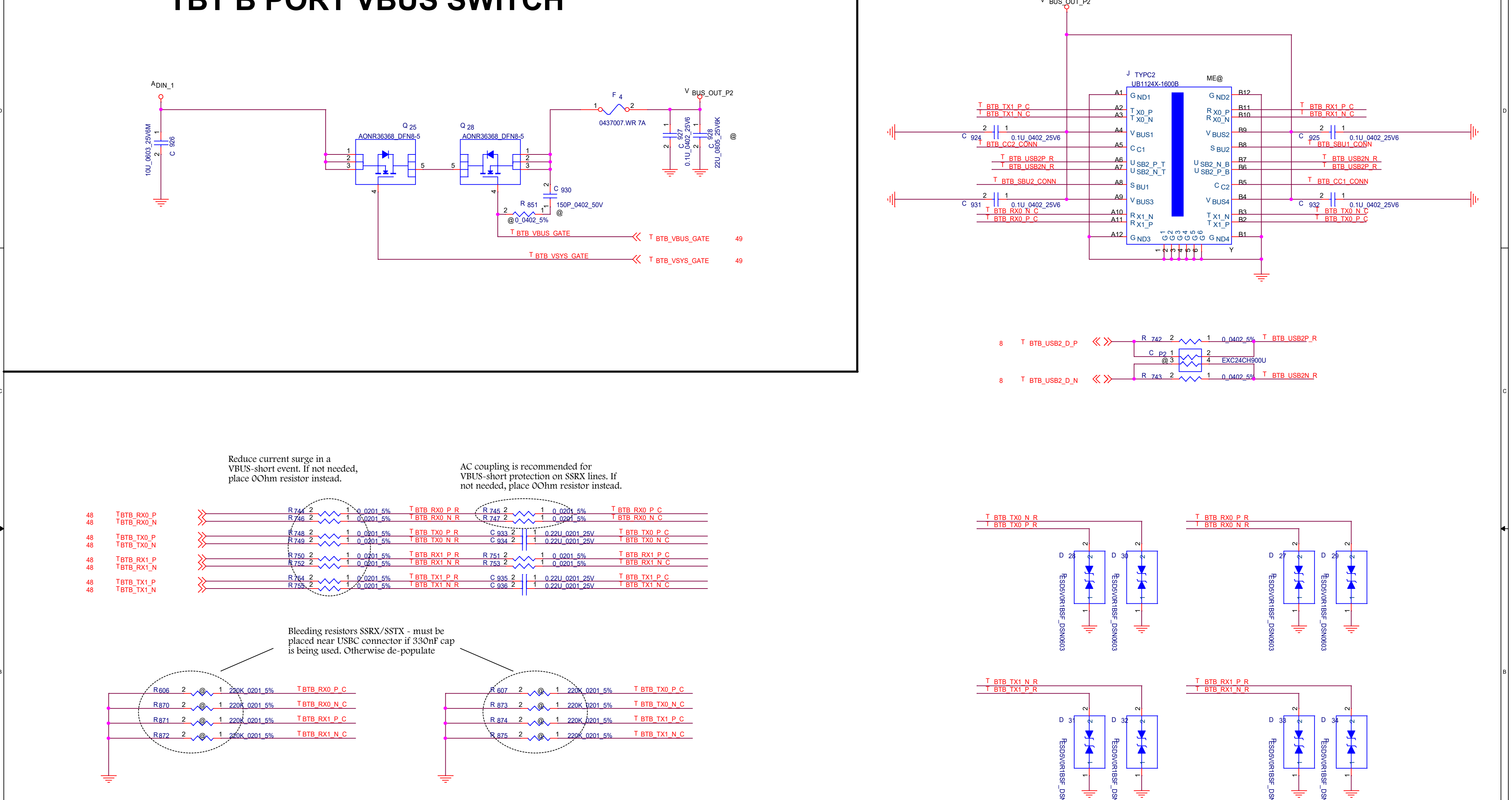
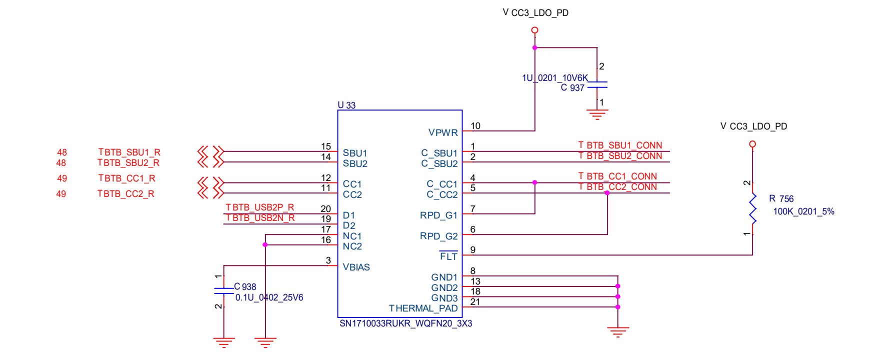
Title: TYPEC_PORTA

Size: C | Document Number: S 750 | Rev: 0.5

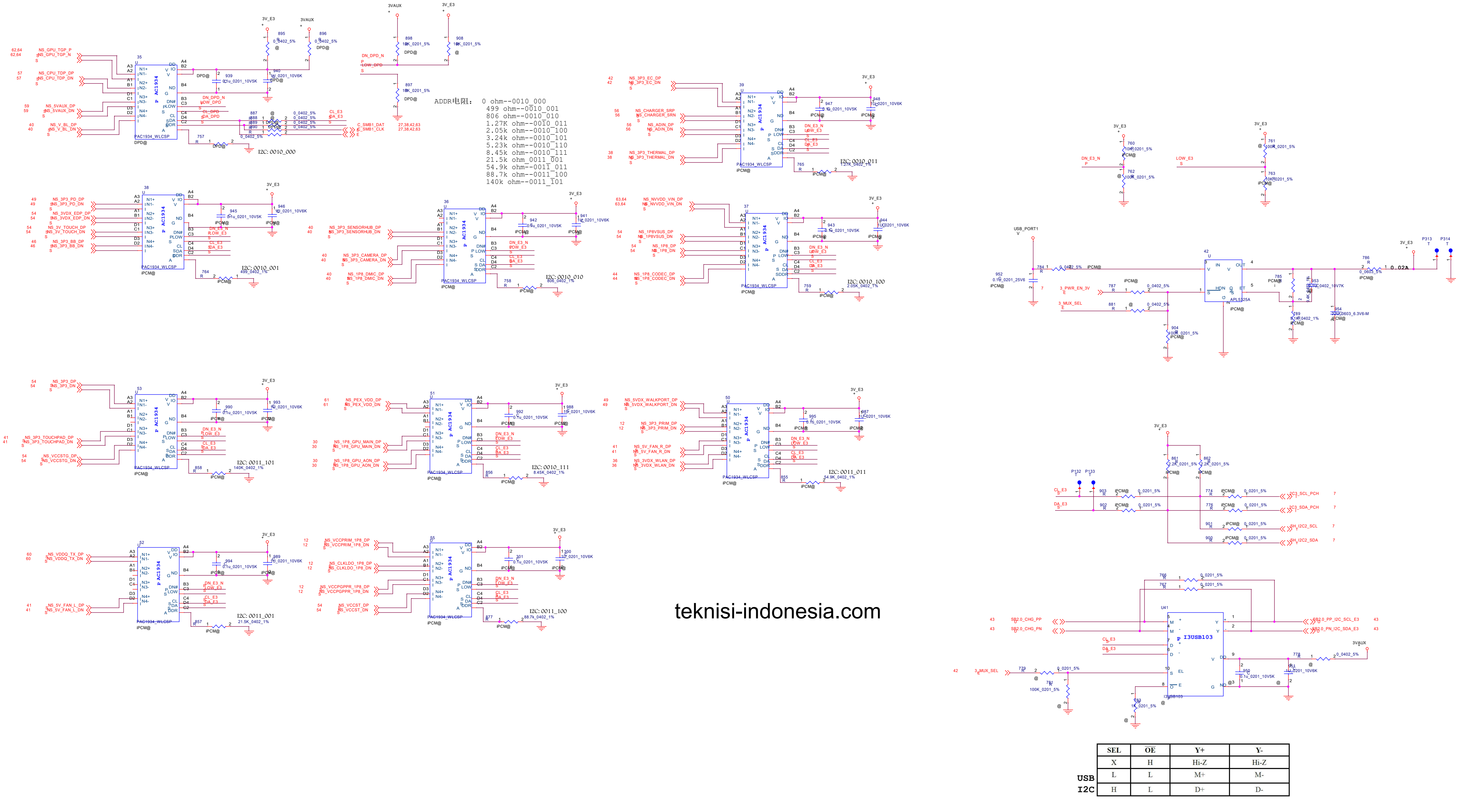
Date: Friday, August 07, 2020 | Sheet 50 of 66

TBT B PORT VBUS SWITCH





lenovo联想	LENOVO.CRDN		
Title	TYPEC_PORTB		
Size C	Document Number S750		Rev 0.5
Date: Friday, August 07, 2020	Sheet 51 of 66		



ADDR电阻： 0 ohm--0010_000
499 ohm--0010_001
806 ohm--0010_010
1.27K ohm--0010_011
2.05k ohm--0010_100
3.24k ohm--0010_101
5.23k ohm--0010_110
8.45k ohm--0010_111
21.5k ohm_0011_001
54.9k ohm--0011_011
88.7k ohm--0011_100
140k ohm--0011_101

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	SEL	OE	Y+	Y-
	X	H	Hi-Z	Hi-Z
USB	L	L	M+	M-
I2C	H	L	D+	D-

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Title: pWRGD CONTROL

Size: D | Document Number: S750 | Rev: 0.5v

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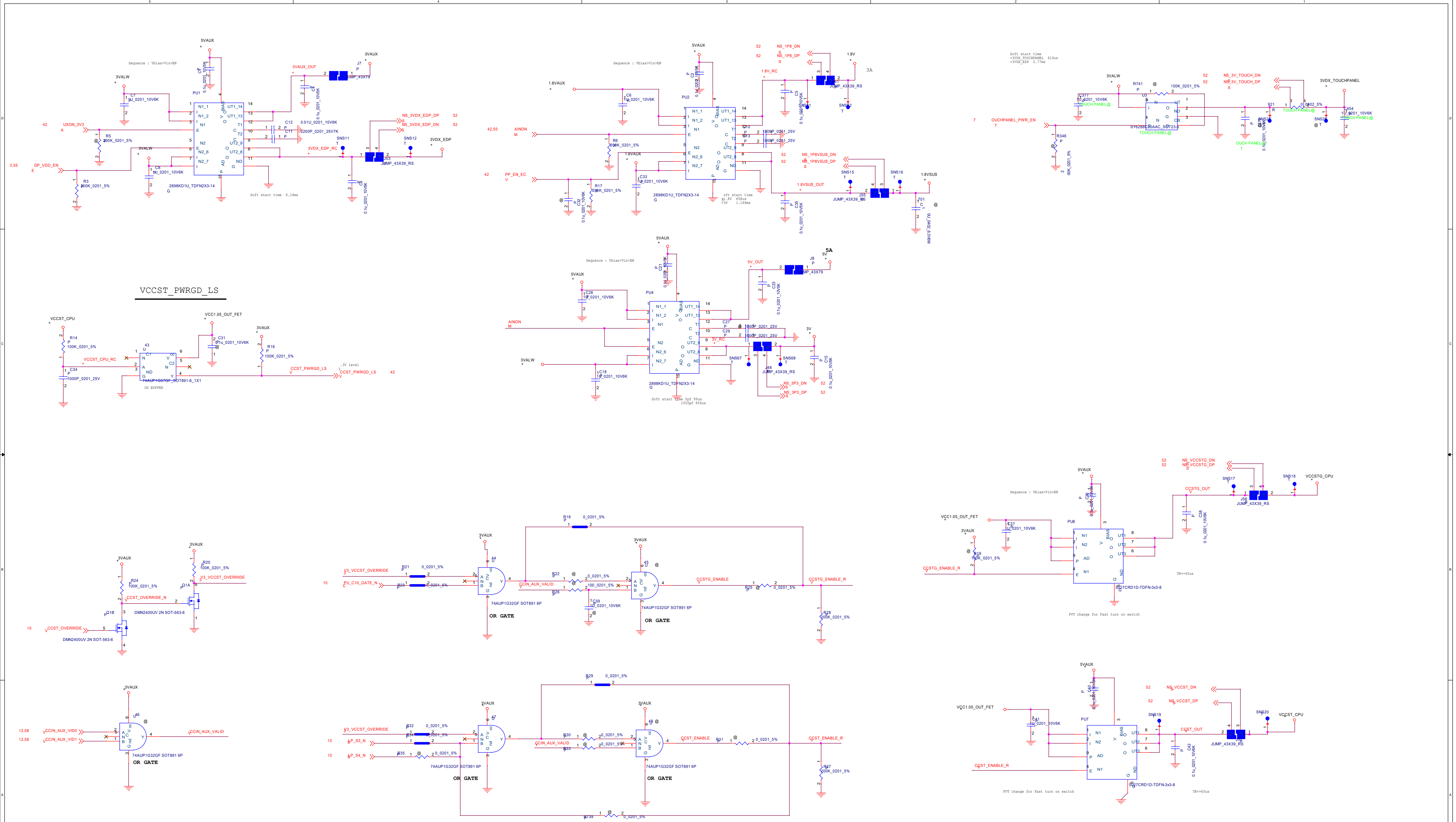
lenovo联想	LENOVO.CRDN
Title	B LANK
Size C	Document Number S 750 — Rev 1.0
Date: Friday, August 07, 2020	Sheet 5 3 o f 66

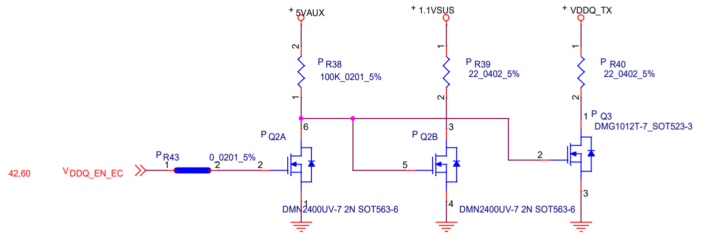


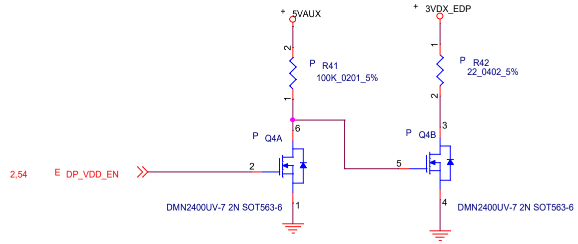
LENOVO.CRDN

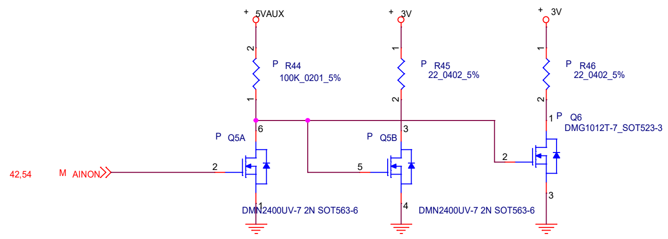
Title: SWITCH POWER

Size: D | Document Number: S750 | Rev: 0.5V

Date: Friday, August 07, 2020 | Sheet 54 of 66







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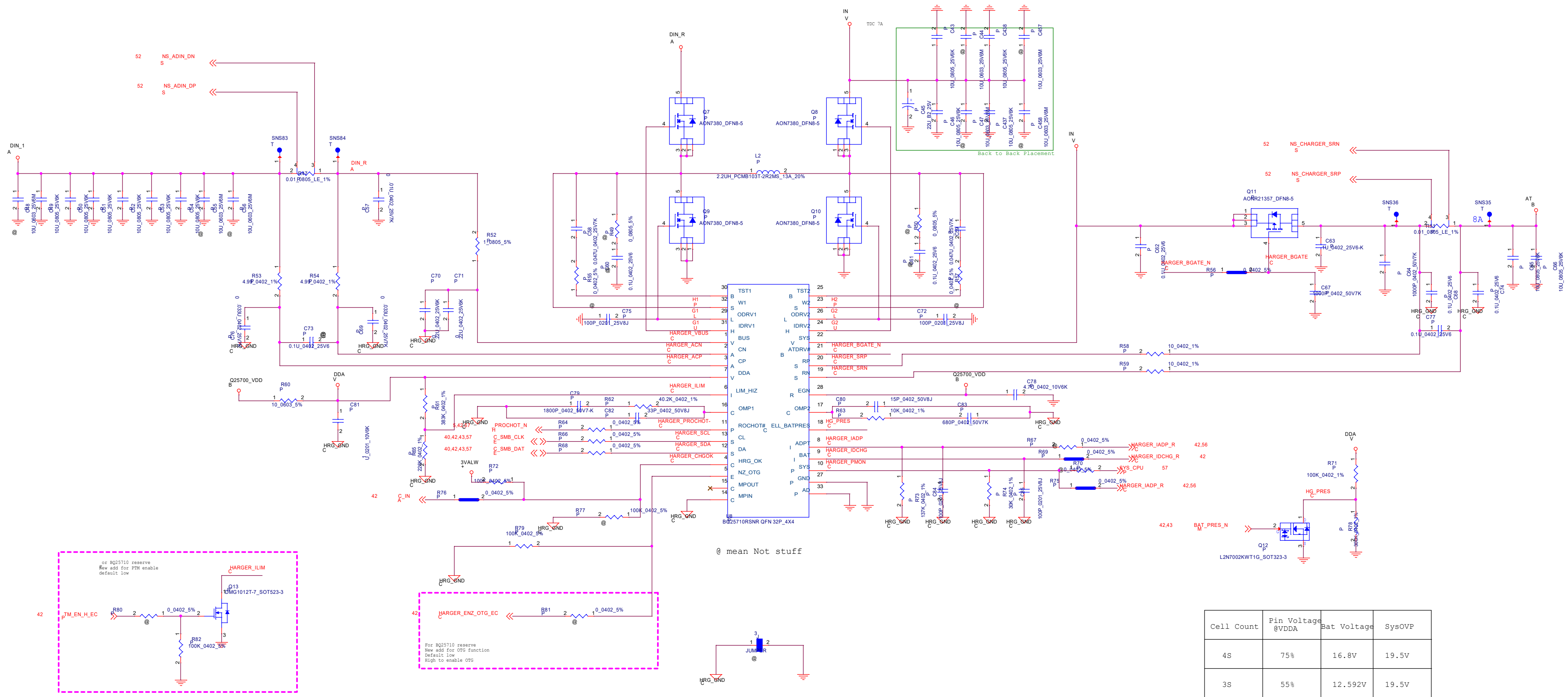
Title: DISCHARGE

Size: C
Document Number: S 750
Rev: 0.5

Date: Friday, August 07, 2020 Sheet 55 of 66



Cell Count	Pin Voltage @VDDA	Bat Voltage	SysOVP
4S	75%	16.8V	19.5V
3S	55%	12.592V	19.5V
2S	40%	8.4V	12V
1S	25%	4.192V	5V

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Title: NVDC CHARGER

Size: D | Document Number: S750 | Rev: 1.0V

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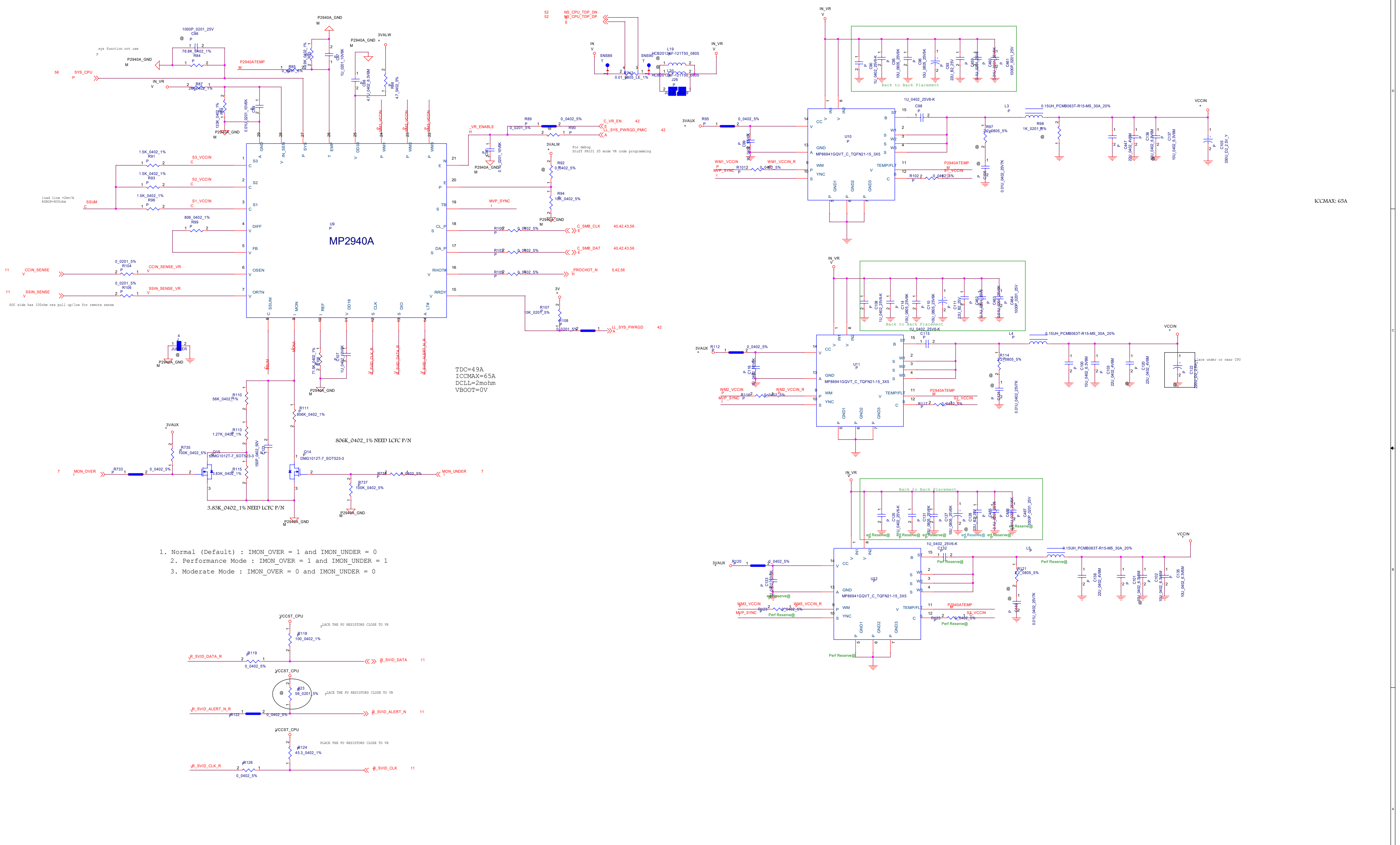

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Title: IMVP9

Document Number: S750 Rev 0.9v

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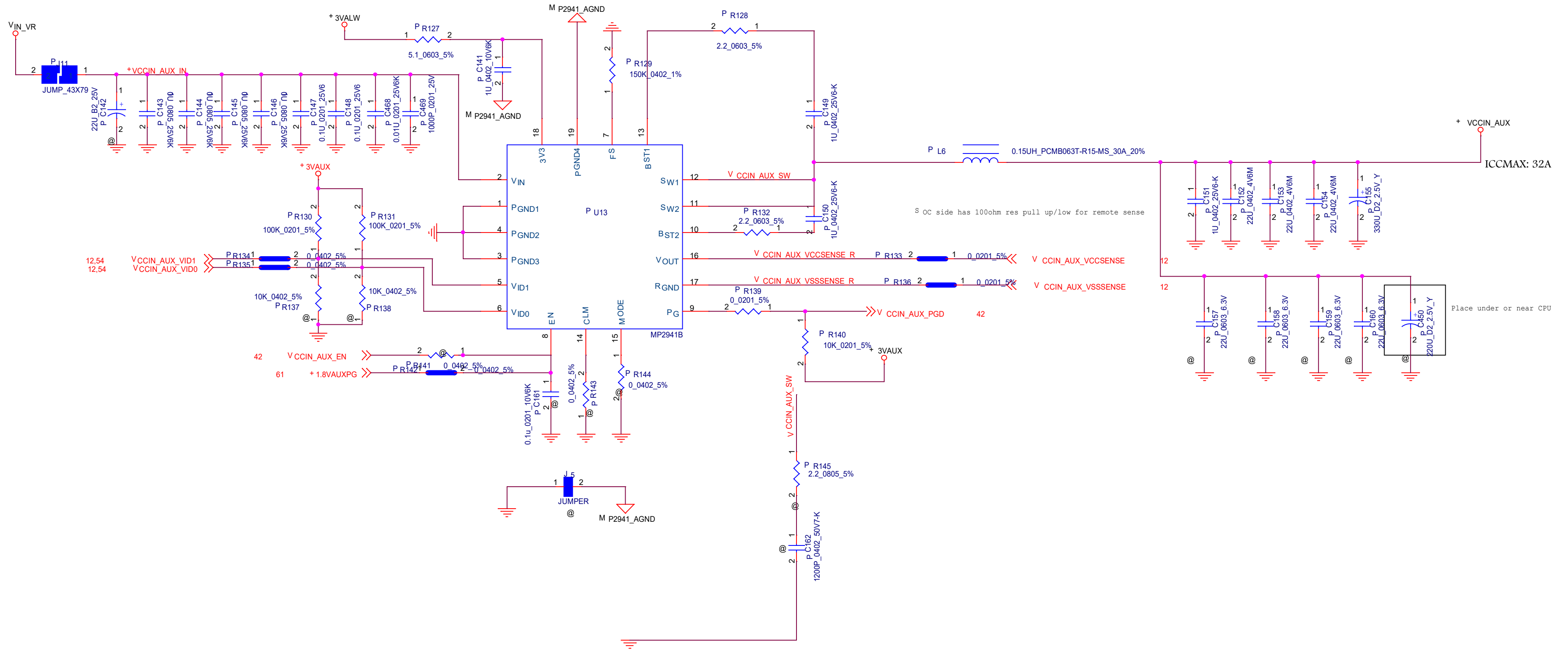


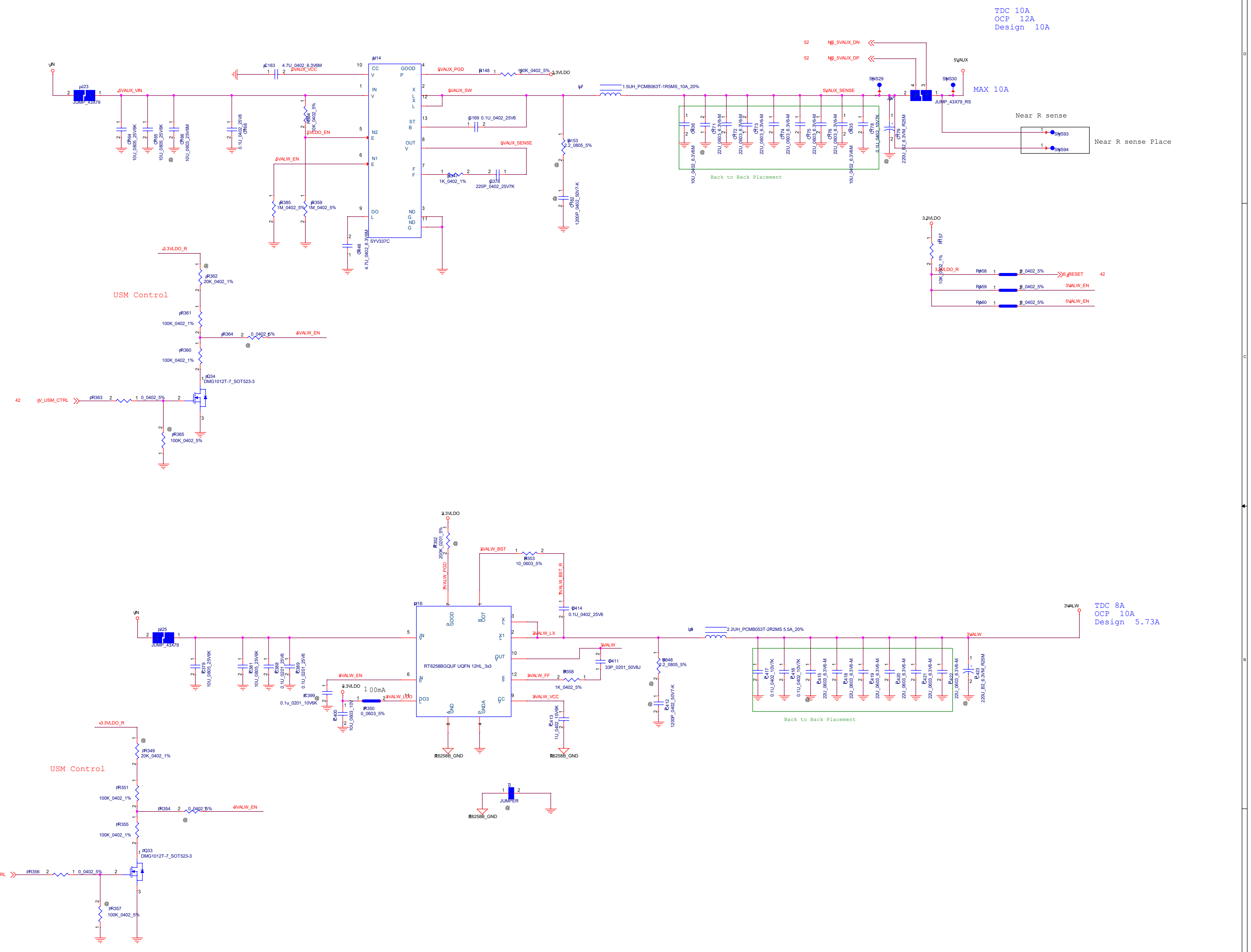
lenovo联想

LENOVO.CRDN

Title
V CCINAUX

Size	Document Number	Rev
C	S 750	0.5

Date: Friday, August 07, 2020 Sheet 58 of 66

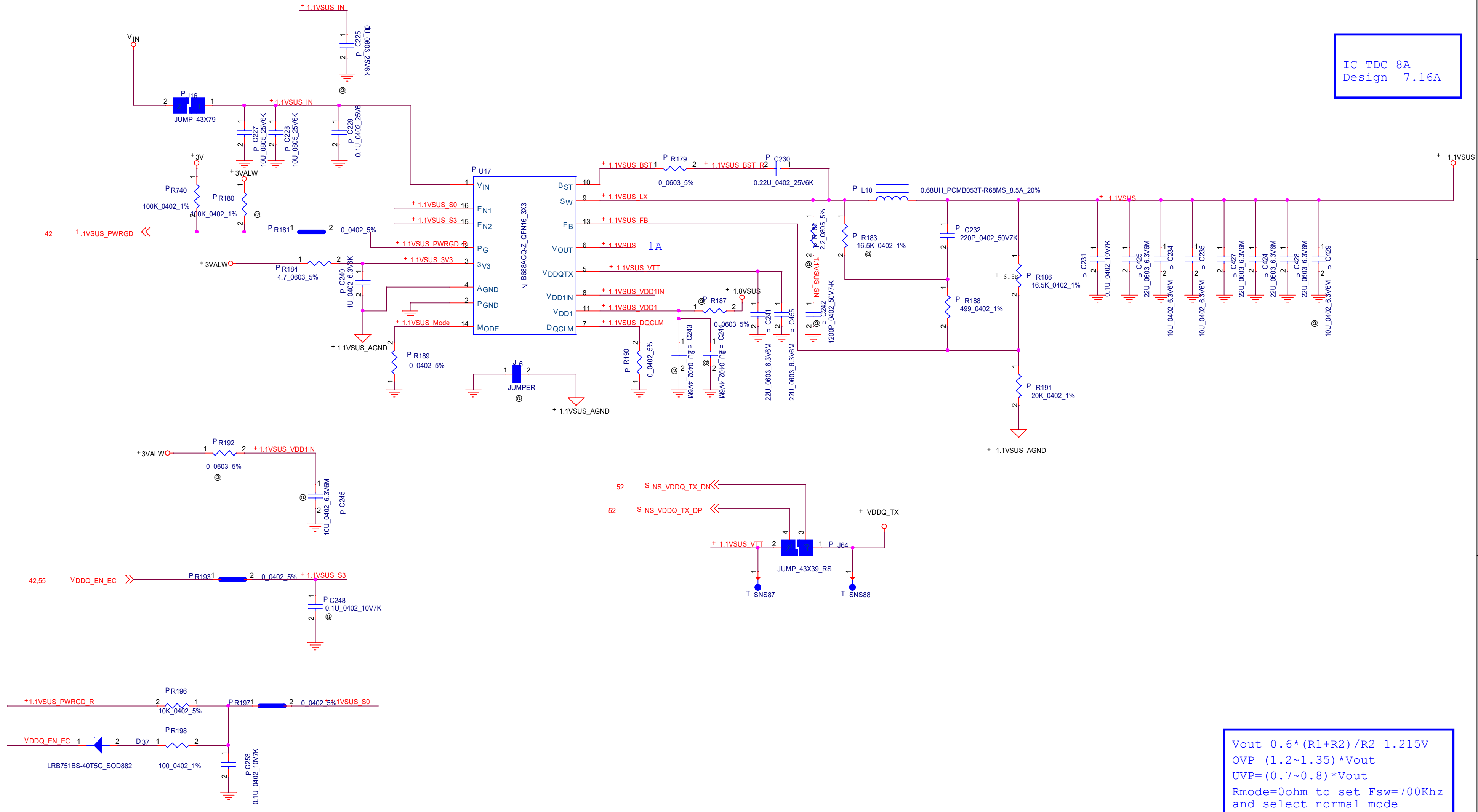


LENOVO.CRDN

Title: +3VALW/+5VAUX

Size: Custom | Document Number: S750 | Rev: 1.0

Date: Friday, August 07, 2020 | Sheet 59 of 66



IC TDC 8A
Design 7.16A

Vout=0.6*(R1+R2)/R2=1.215V
OVP=(1.2~1.35)*Vout
UVP=(0.7~0.8)*Vout
Rmode=0ohm to set Fsw=700Khz
and select normal mode

confirm with EE 0.6V enable

STATE	EN1	EN2	+1.1VSUS	+1.8VSUS	+0.6V
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off

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Title: +1.1VSUS/+1.8VSUS

Size: C | Document Number: S 750 | Rev: 1.0

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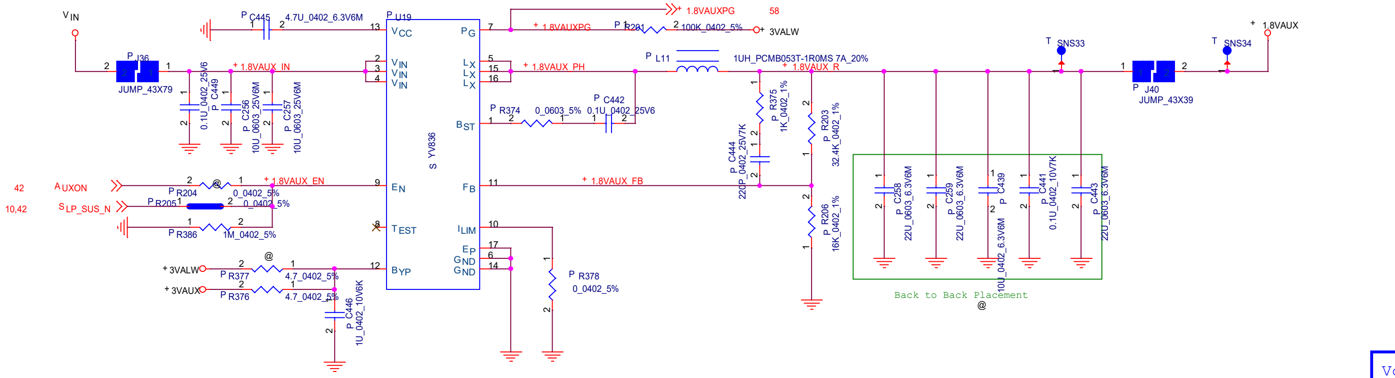
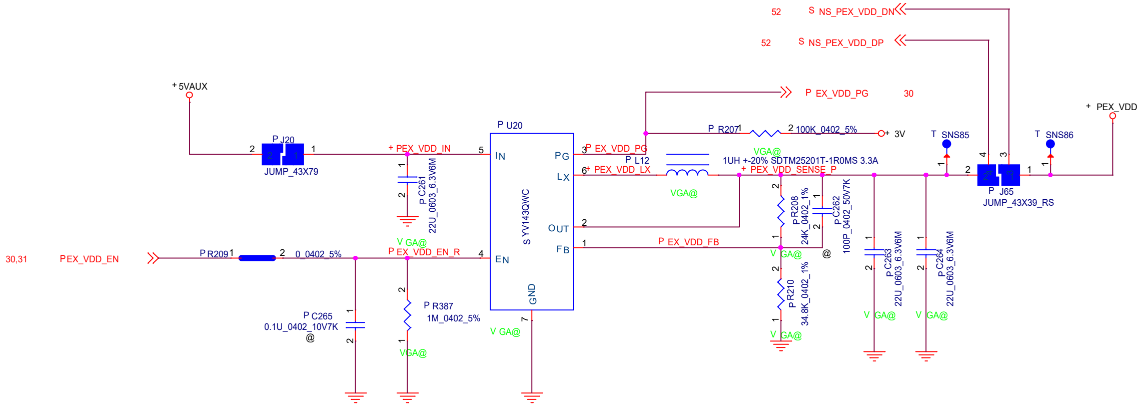


IC TDC 6A

Design 5.2A

Vout=0.6*(R1+R2)/R2=1.815V
OVP=1.2*Vout
Fsw=1Mhz



IC TDC 3A
Design 2A

Vout=0.6*(R1+R2)/R2=1.014V
OVP=1.2*Vout
UVP=0.4*Vout
Fsw=1.5Mhz

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Title	+1.8VAUX
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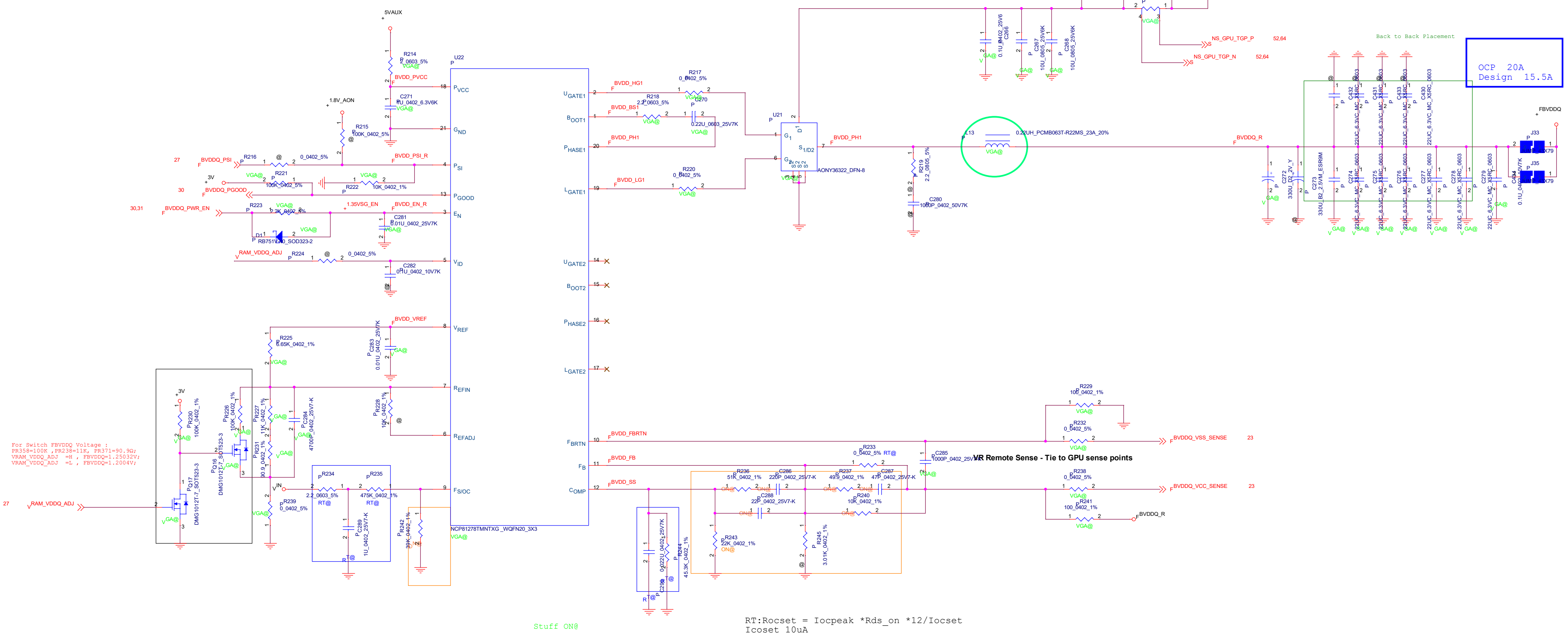
RT8816 PSI	NCP81278PSI	Phase Configuration
1.6V~5.5V	High	2Phase CCM
1.08~1.35V	Connect to PVCC	2Phase DEM
0.7~0.88V	Intermediate	1Phase CCM
0~0.4V	Low	1Phase DEM



RT:Rocset = Iocpeak *Rds_on *12/Iocset
Icoset 10uA
ON: Rocset=10^6*Iocpeak*Rds_on/2
AONE6982 Q2 Vgs=4.5V Rds_ON= (2-2.45) mohm

:Place For NCP81278 :PR242,PR236,PR243,PR237,PR240,PC286,PC288,PC287

: Place For RT8816:PR234,PR235,PR244,PR233,PC289,PC290

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Title: FBVDDQ

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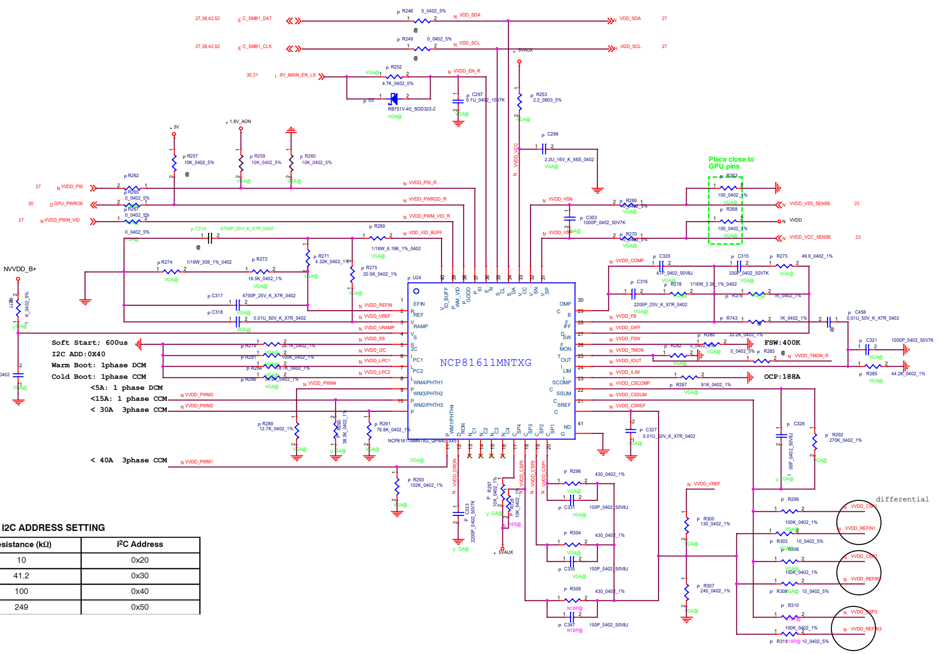
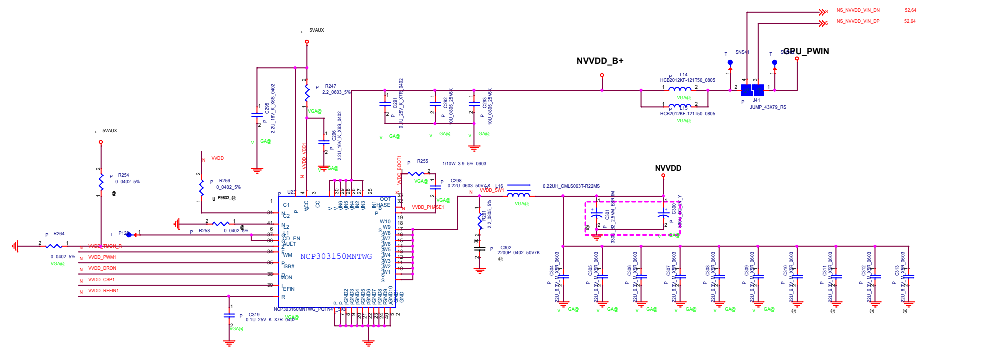
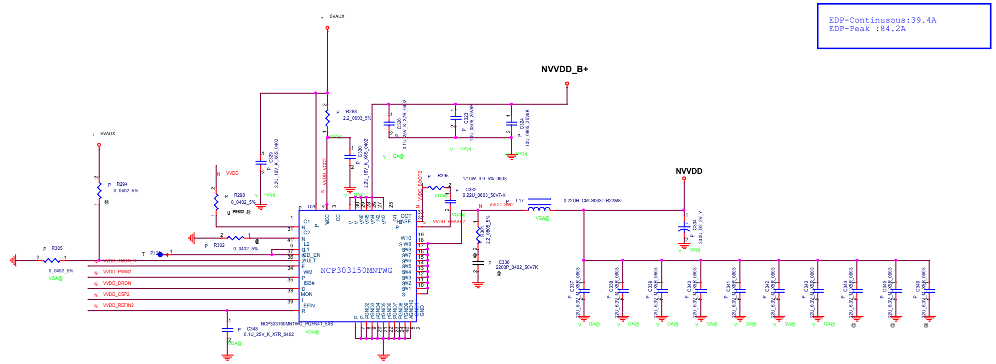


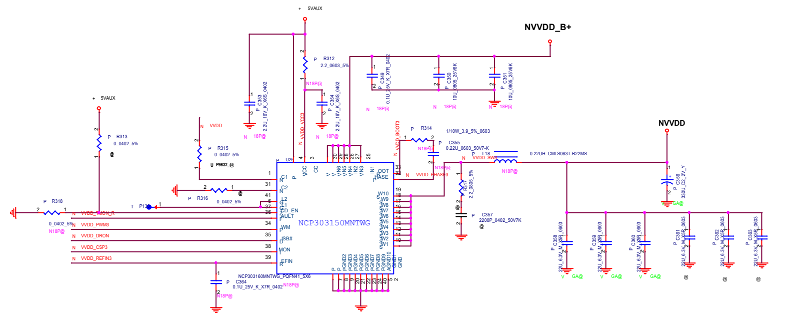
Table 1. I2C ADDRESS SETTING

Resistance (kΩ)	I²C Address
10	0x20
41.2	0x30
100	0x40
249	0x50



EDP-Continuous:39.4A
EDP-Peak :84.2A





When Stuff N18P GPU ,Pls Stuff N18P@ and Unstuff N18S@
When stuff N18S GPU ,Pls Stuff N18S@ and Unstuff N18P@

Bom Change（Default N18S）

For N18P GPU
PR285 : SD03440228J,S RES 1/16W 40.2K +-1% 0402,
PR292 : SD000016400,S RES 1/16W 274K +-1% 0402,
PR280 : SD03420028J,S RES 1/16W 20K +-1% 0402,
PR289 : SD03412020J,S RES 1/16W 12K +-1% 0402
PR290 : SD000017Q00,S RES 1/16W 35.7K +-1% 0402
PR291 : SD03495328J,S RES 1/16W 95.3K +-1% 0402
PR293 : SD03495328J,S RES 1/16W 95.3K +-1% 0402

For N18S GPU
PR285 : SD03444228J, S RES 1/16W 44.2K+-1%0402,
PR292 : SD000018P00, S RES 1/16W 270K +-1% 0402,
PR280 : SD03433228J, S RES 1/16W 33.2K +-1% 0402,
PR289 : SD03412728J, S RES 1/16W 12.7K +-1% 0402,
PR290 : SD03438328J, S RES 1/16W 38.3K +-1% 0402,
PR291 : SD03476828J, S RES 1/16W 76.8K +-1% 0402,
PR293 : SD000018400, S RES 1/16W 102K +-1% 0402,

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Title: NVVDD

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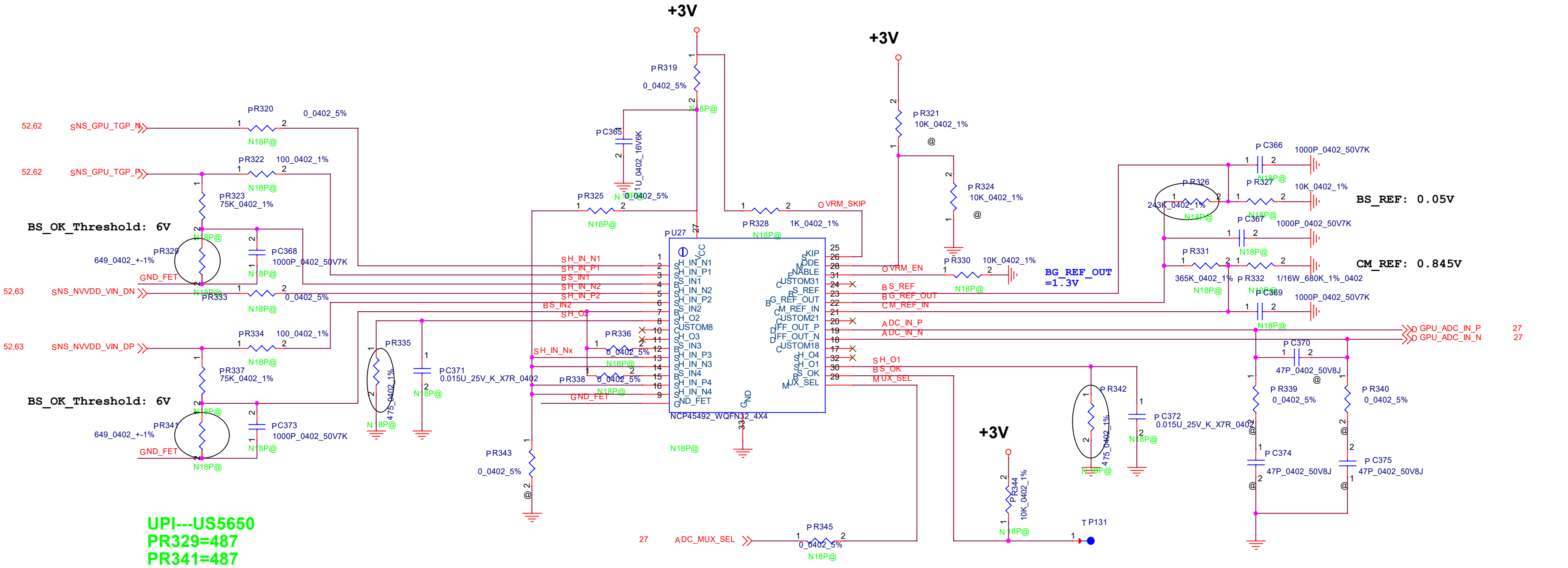

UPI---US5650
PR329=487
PR341=487
PR335=357ohm for Lower 70W 215 for 75W to 90W 165 for 100W to 110W
PR342=357ohm for Lower 70W 215 for 75W to 90W 165 for 100W to 110W
PR326=324K
PR323=75K
PR337=75K
PC368=1nF
PC373=1nF

When Stuff N18P GPU ,Stuff N18P@

ON---NCP45491
PR329=649
PR341=649
PR335=475ohm for lower 70W 287 for 75W to 90W 221 for 100W to 110W
PR342=475ohm for lower 70W 287 for 75W to 90W 221 for 100W to 110W
PR326=243K
PR323=75K
PR337=75K
PC368=1nF
PC373=1nF
Stuff PR325

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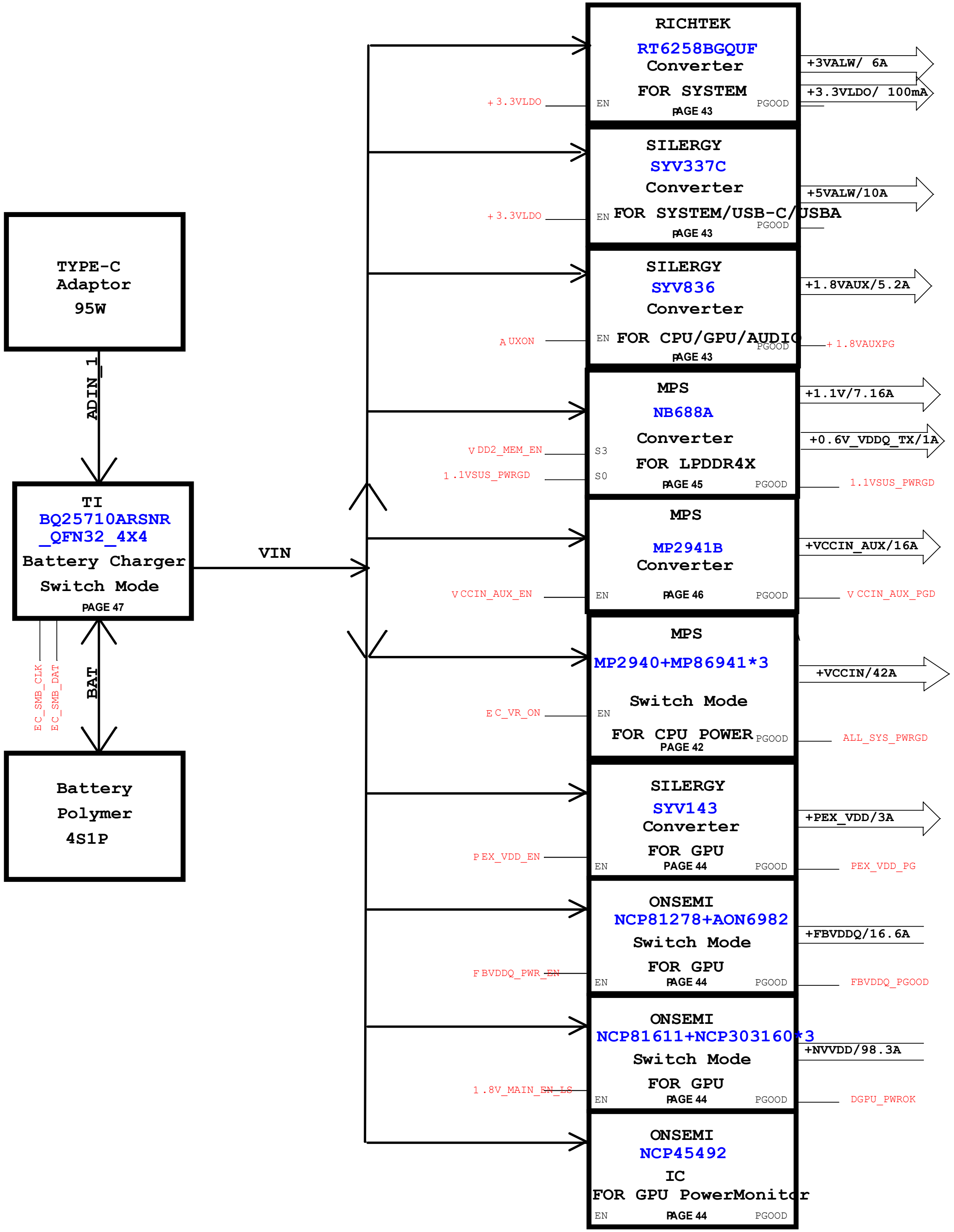

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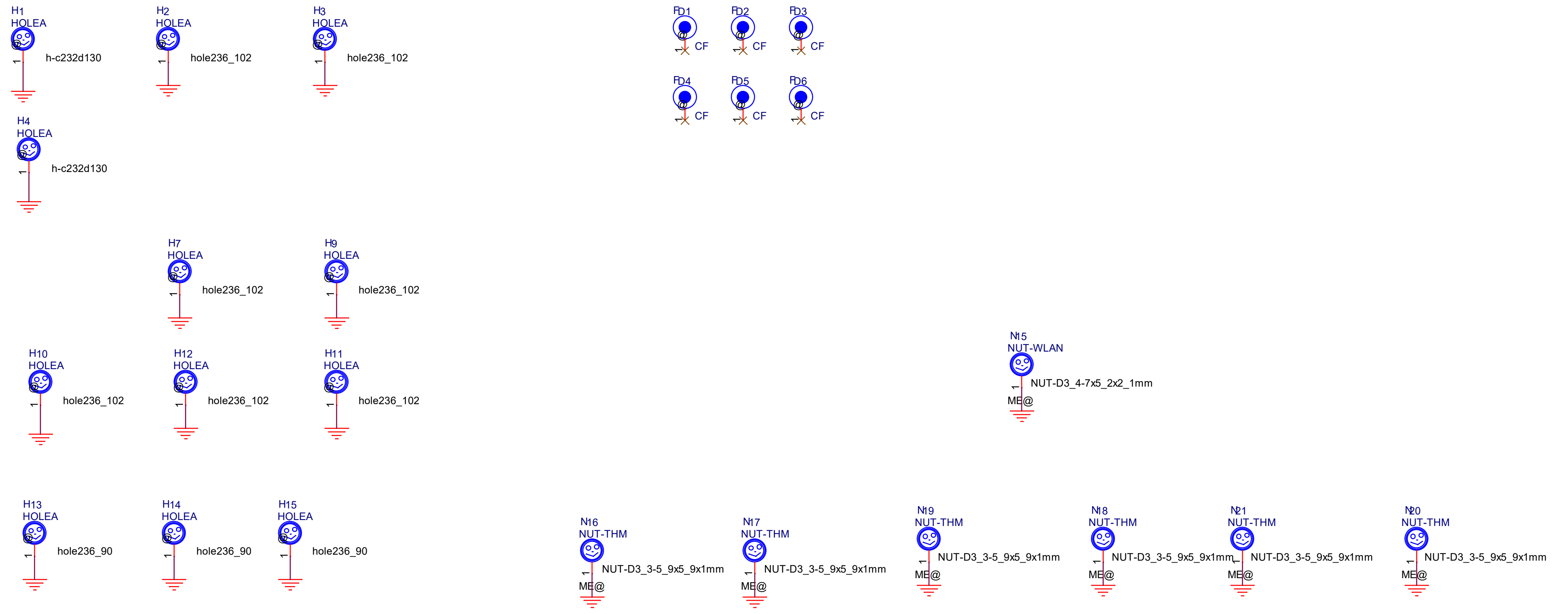
Title	PWR-Power Diagram
Size: C	Document Number: S 950 — Rev 0.5
Date: Friday, August 07, 2020	Sheet 65 of 66



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Title: M OUNTING HOLE/EMI

Size	Document Number	Rev
B	S 750	0.5

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