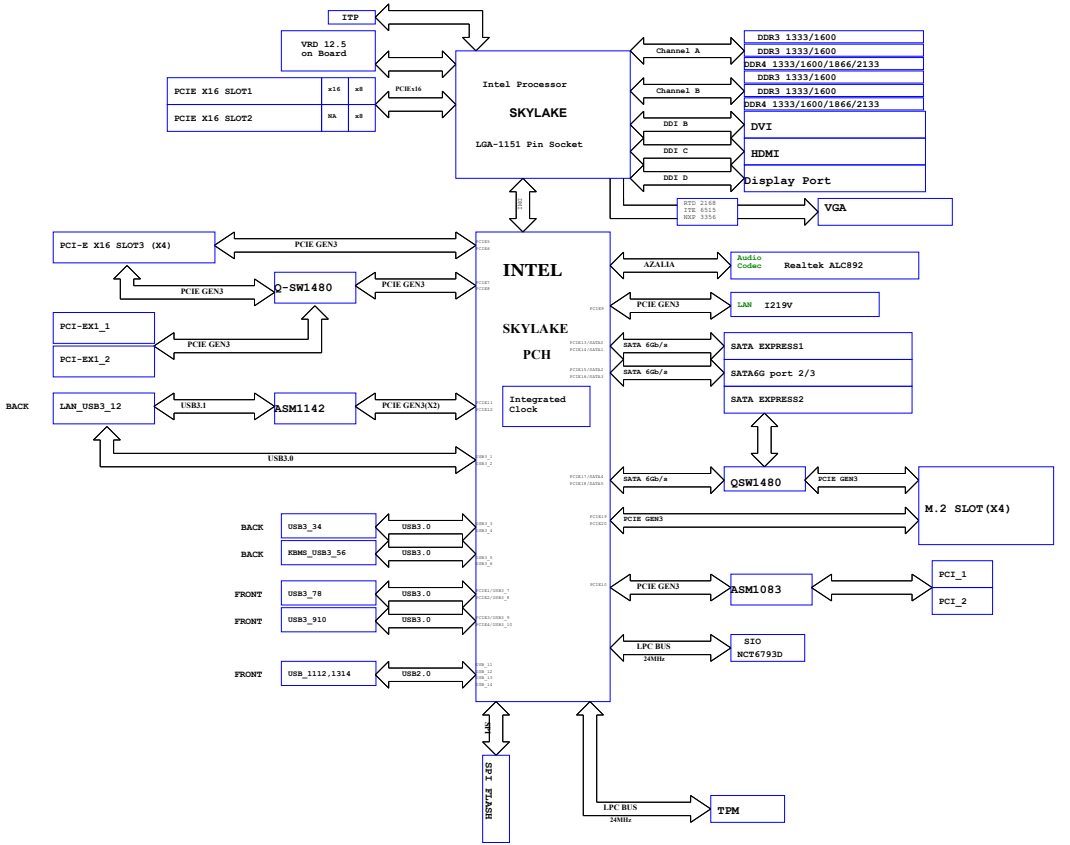
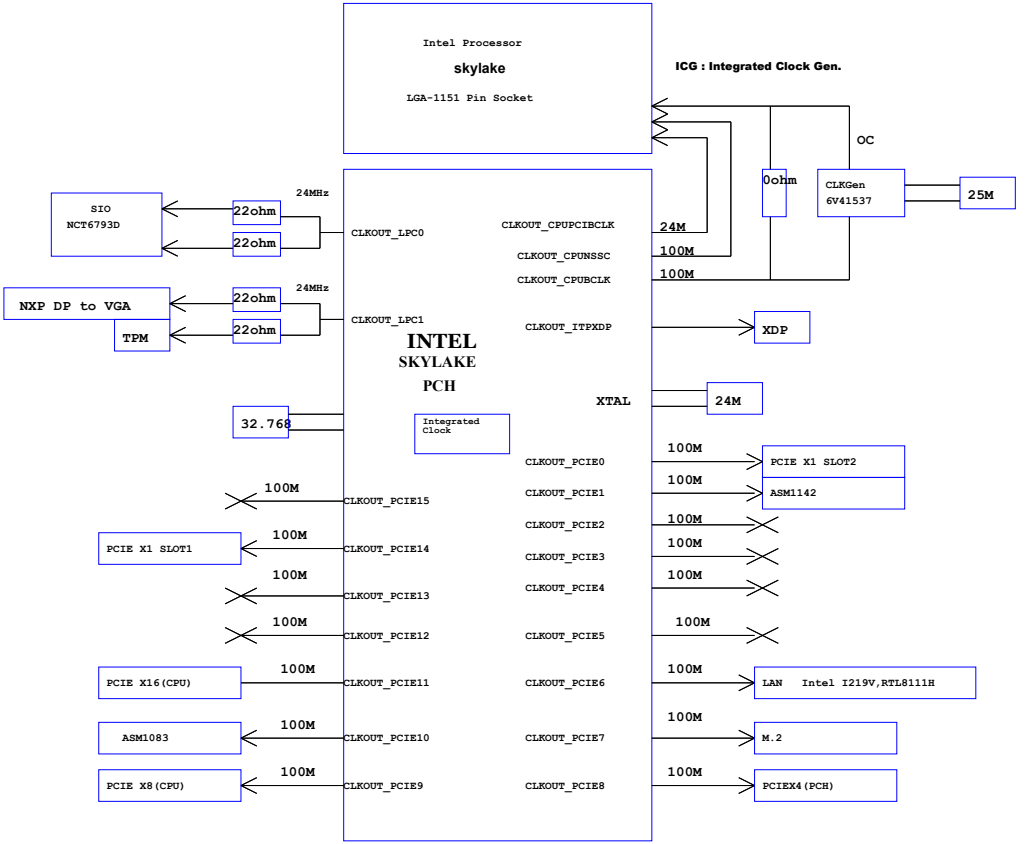
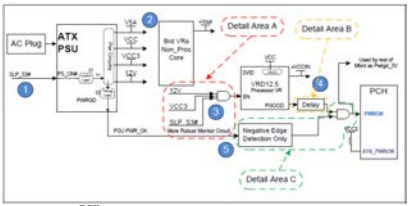
H110I-PLUS

Rev 1.01




Intel Processor
skylake
LGA-1151 Pin Socket
ICG : Integrated Clock Gen.
OC
0ohm
CLKGen
6V41537
25M
SIO
NCT6793D
24MHz
22ohm
22ohm
CLKOUT_LPC0
NXP DP to VGA
TPM
24MHz
22ohm
22ohm
CLKOUT_LPC1
INTEL
SKYLAKE
PCH
Integrated
Clock
32.768
CLKOUT_CPUPCIBCLK
CLKOUT_CPUNSSC
CLKOUT_CPUBCLK
24M
100M
100M
CLKOUT_ITPXDP
XDP
XTAL
24M
CLKOUT_PCIE0
CLKOUT_PCIE1
CLKOUT_PCIE2
CLKOUT_PCIE3
CLKOUT_PCIE4
CLKOUT_PCIE5
CLKOUT_PCIE6
CLKOUT_PCIE7
CLKOUT_PCIE8
100M
100M
100M
100M
100M
100M
100M
100M
PCIE X1 SLOT2
ASM1142
CLKOUT_PCIE15
CLKOUT_PCIE14
CLKOUT_PCIE13
CLKOUT_PCIE12
CLKOUT_PCIE11
CLKOUT_PCIE10
CLKOUT_PCIE9
100M
100M
100M
100M
100M
100M
100M
PCIE X1 SLOT1
PCIE X16(CPU)
ASM1083
PCIE X8(CPU)
LAN Intel I219V,RTL8111H
M.2
PCIEX4(PCH)



PCI_Express x 16_1 — PWRGD — <19>O_X16_RST#

PCI_Express x 16_2 — PWRGD — <19>O_X16_RST#

PCI_Express x 1_1,2 & x16_3 — PWRGD — <19>O_X1_RST#

RESET_SWITCH

XDP — DBR# — RESET# — OBSDATA

SYS_RESET# — H_CPURST#

SIO NCT6793D

POWER_SWITCH — PWRBTN — <5>PWRBTN#

PS_IN# — PCIRST1# — PCIRST2# — PCIRST3# — LRESET# — KBRST# — RSMRST# — PS_OUT# — SUSC# — SUSB# — PSON# *1 — ATXPGD *2 — PWROK

PCH skylake

HDA_RST# — AZ_RST# — RESET# — AUDIO ALC898

PLTRST# — PLTRST_PROC# — RCIN# — RSMRST# — PWRBTN# — SLP_S5# — SLP_S4# *4 — SLP_S3# *5 — PROCPUPWRGD — SLP_A# *3 — SLP_LAN# — SYS_PWROK — PCH_PWROK — RTCRST# — SRTCRST# — DPWROK

<17>S_PLTRST# *8 — O_KB_RST# — <4>O_RSMRST# — <6>O_IOPWRBTN# — <4.1> / <8>S_SLP_S4# — <4.2> / <7>S_SLP_S3# — <7>S_SLP_A# — <7.1>S_SLP_LAN#

<1>S_RTCRST# — <1>S_SRTCRST# — BATTERY

<3.1>S_DPWROK(if NO DSW, S_DPWROK=S_RSMRST#)

PROCESSOR skylake — DBR# — RESET# — CFG — PWRGOOD — SVID — VCORE

SYS_RESET# *9 — <18>H_CPURST# *5 — <13>H_CPUPWRGD *7 — <14>VRM_SVID — <15>VCORE

POWER SUPPLY — Main PWR — VSB — PSON# — PWROK

<10>12V,5V,3V — <3>+5VSB, +3VSB — <9>ATX_PSON#_R — <11>P_PWROK_PS

<2>AC_Power Switch On

11.Some SIO don't use, use +3V

<12>O_PWROK

SPI Power (AMT) intel LAN

Vcore Controller — SVID — VCORE — VR_ON — PGOOD — ASP1400(ASP1401)

<16>P_VR_READY_10 — *6 S_SLP_S3# — +12V — +3V

*1 PSON# is inverted by SLP_S3#, but gated and delayed by PWRBTN#

*2 PWROK will assert when +3V arrives at +2.1V then delay 300ms~500ms and gated by ATXPGD

*3 If support AMT, SLP_A# could already be high before sequence begins. If not support AMT, SLP_A# will come with SLP_S3

*4 SLP_S4# controls +1.5VDual and +VTTDDR

*5 Come with 1.5VDUAL

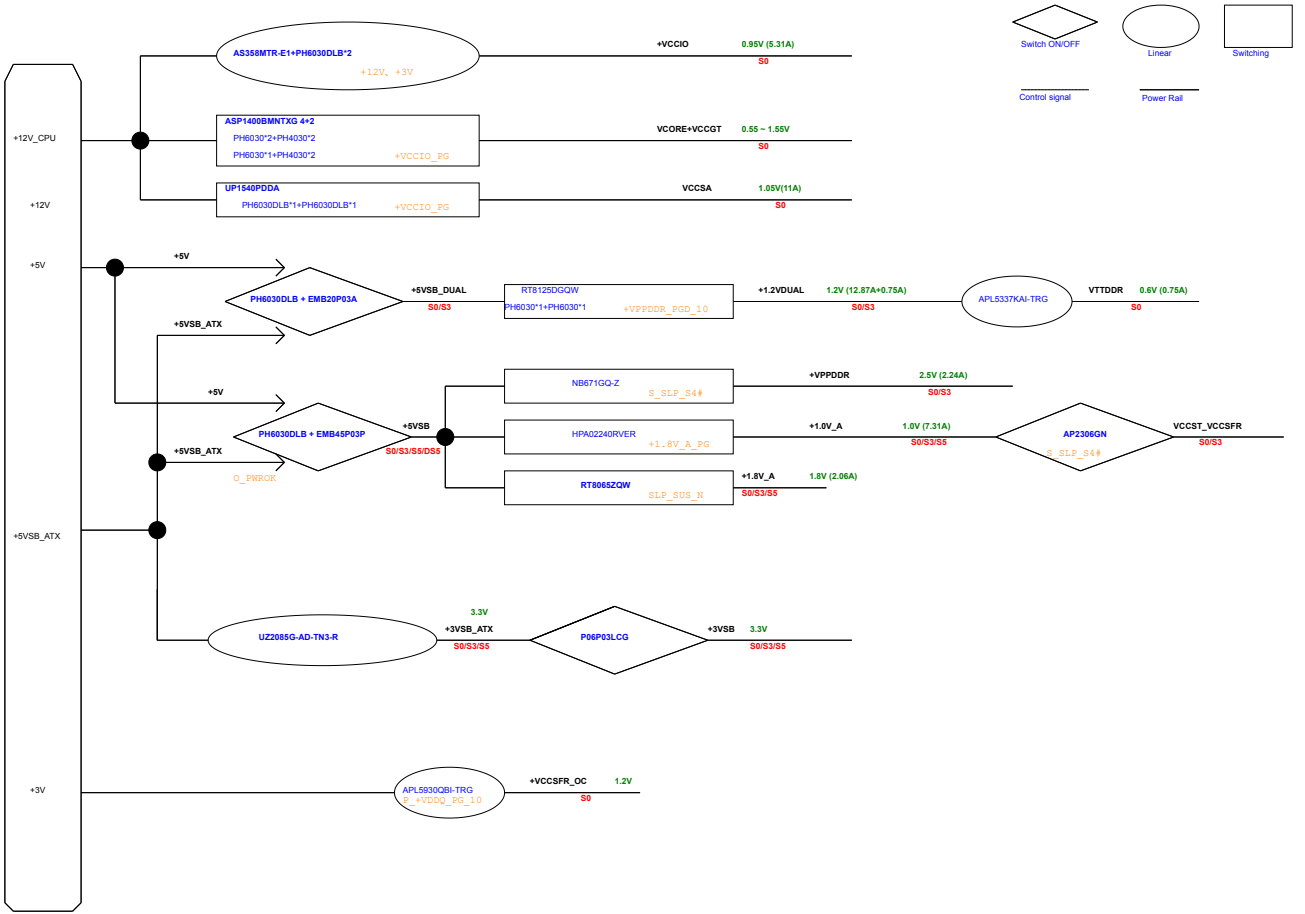
*6 Come with +3V,+12V and gated by SLP_S3#

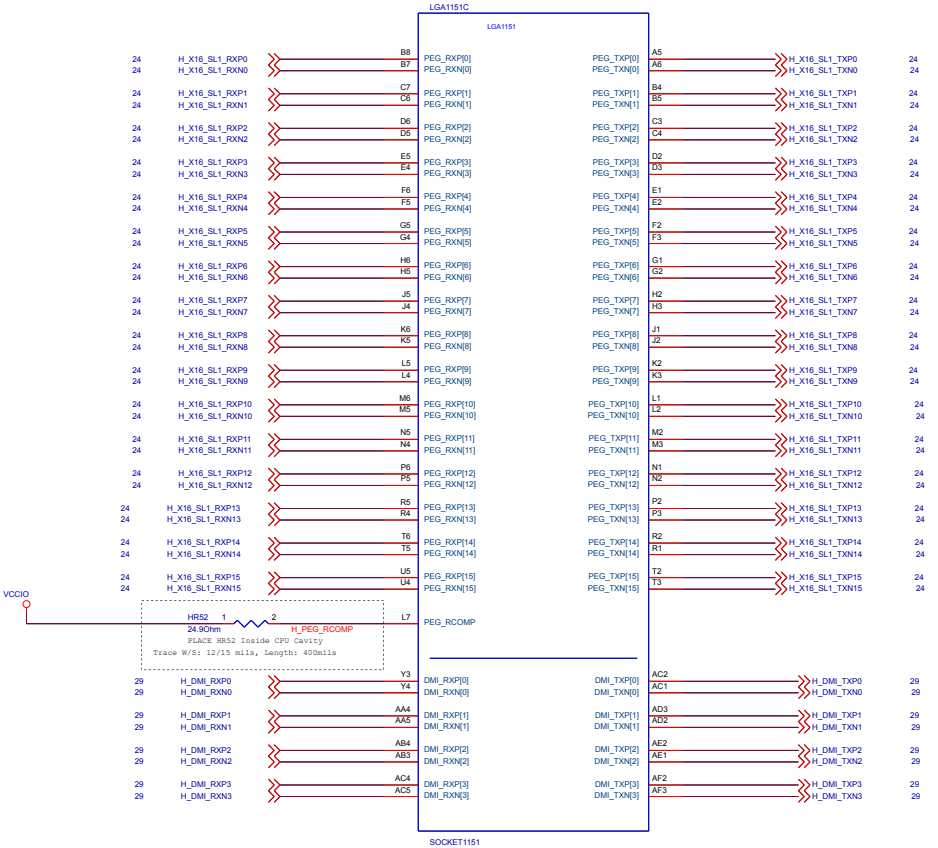
*7 CPUPWRGD= After PWROK

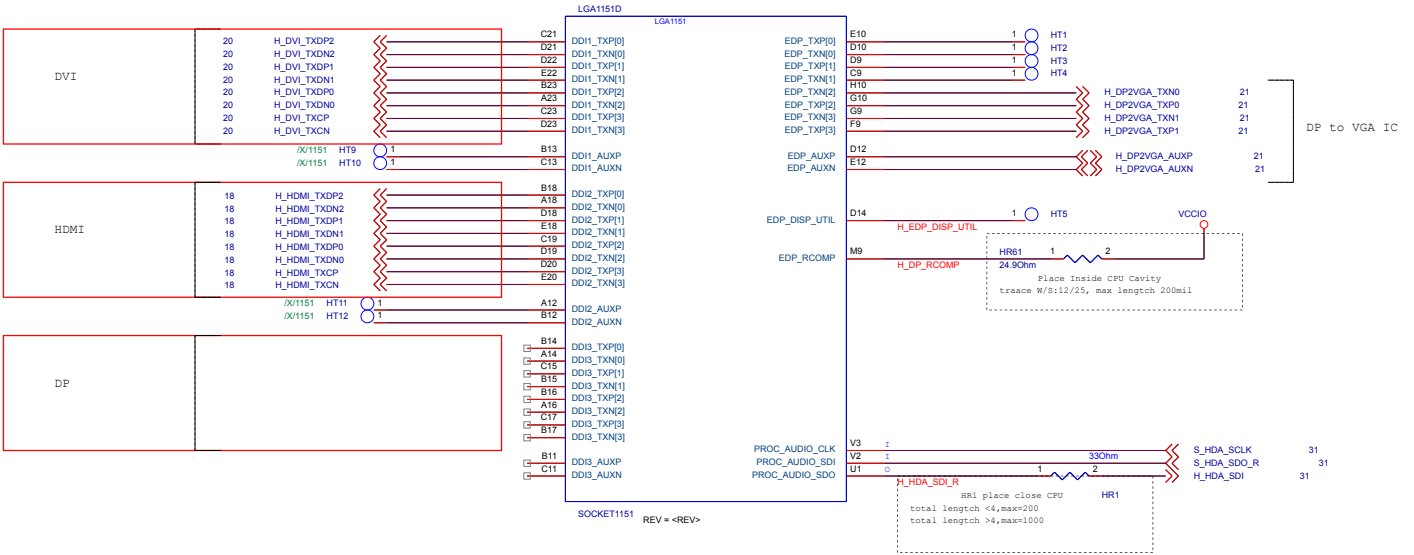
*8 PLTRST# = PCH PWROK AND PCH SYS_PWROK

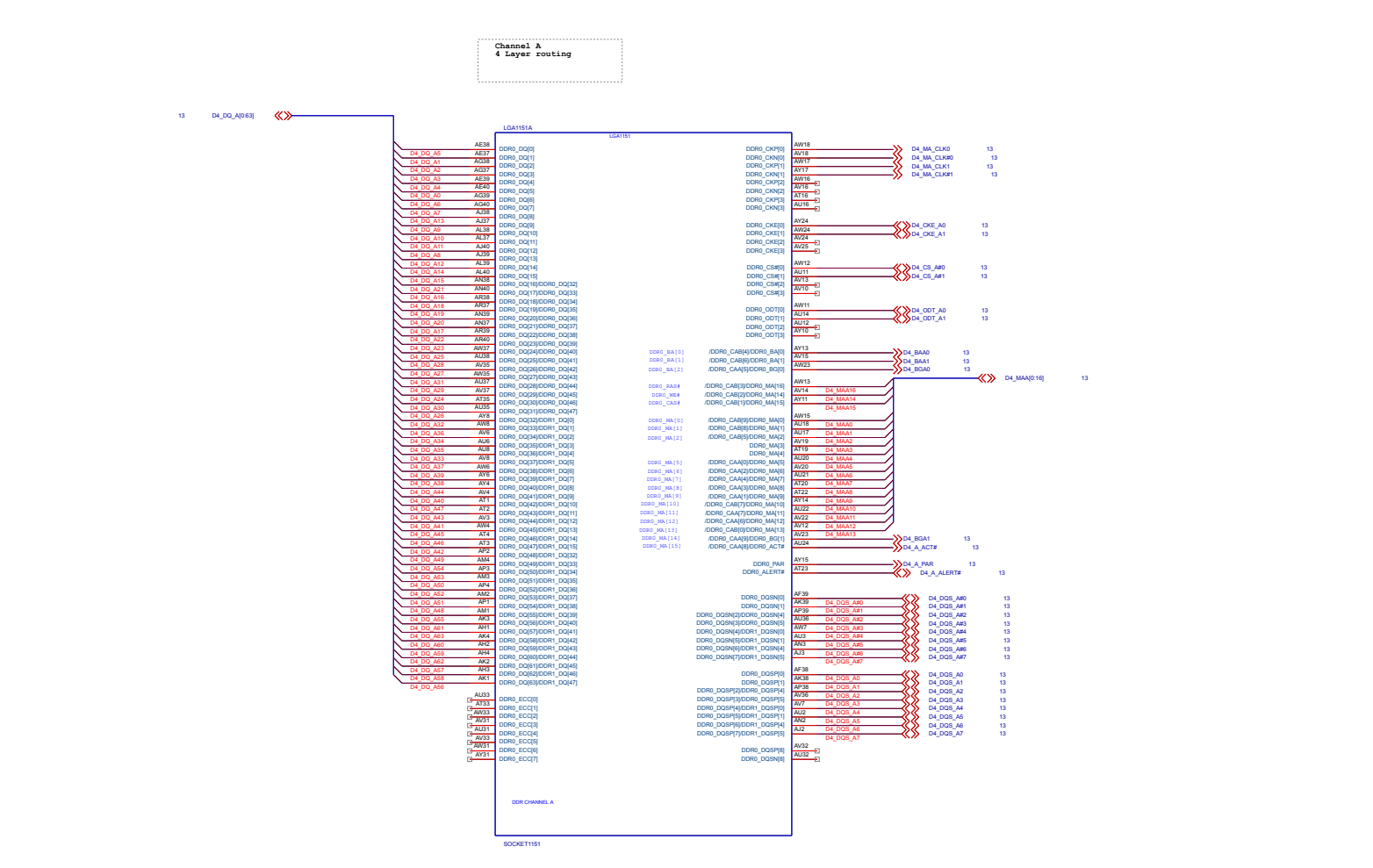
*9 PLTRST_PROC#=PLTRST#, voltage=1V, directly connect to CPU

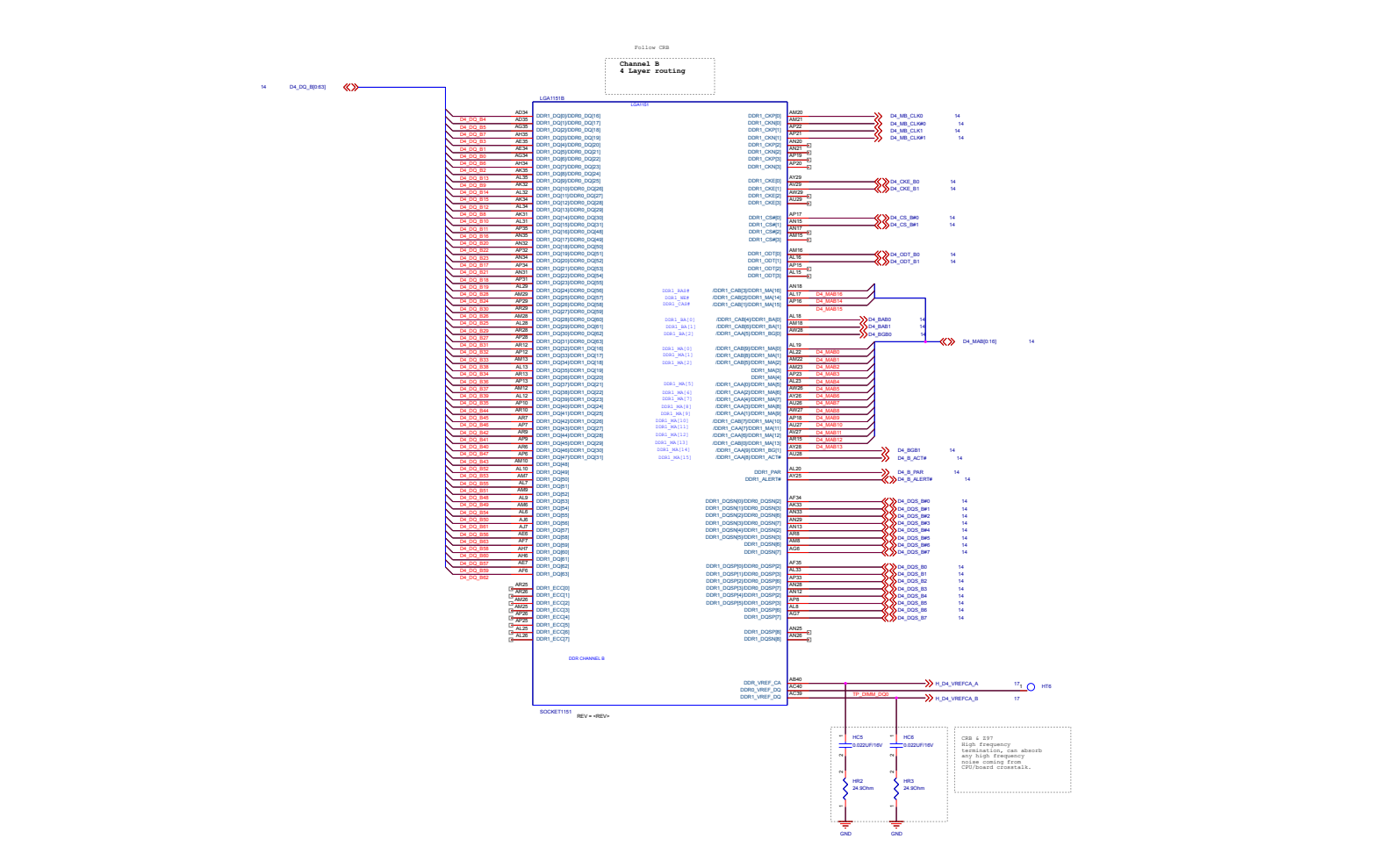
CHIP — SOCKET or SLOT

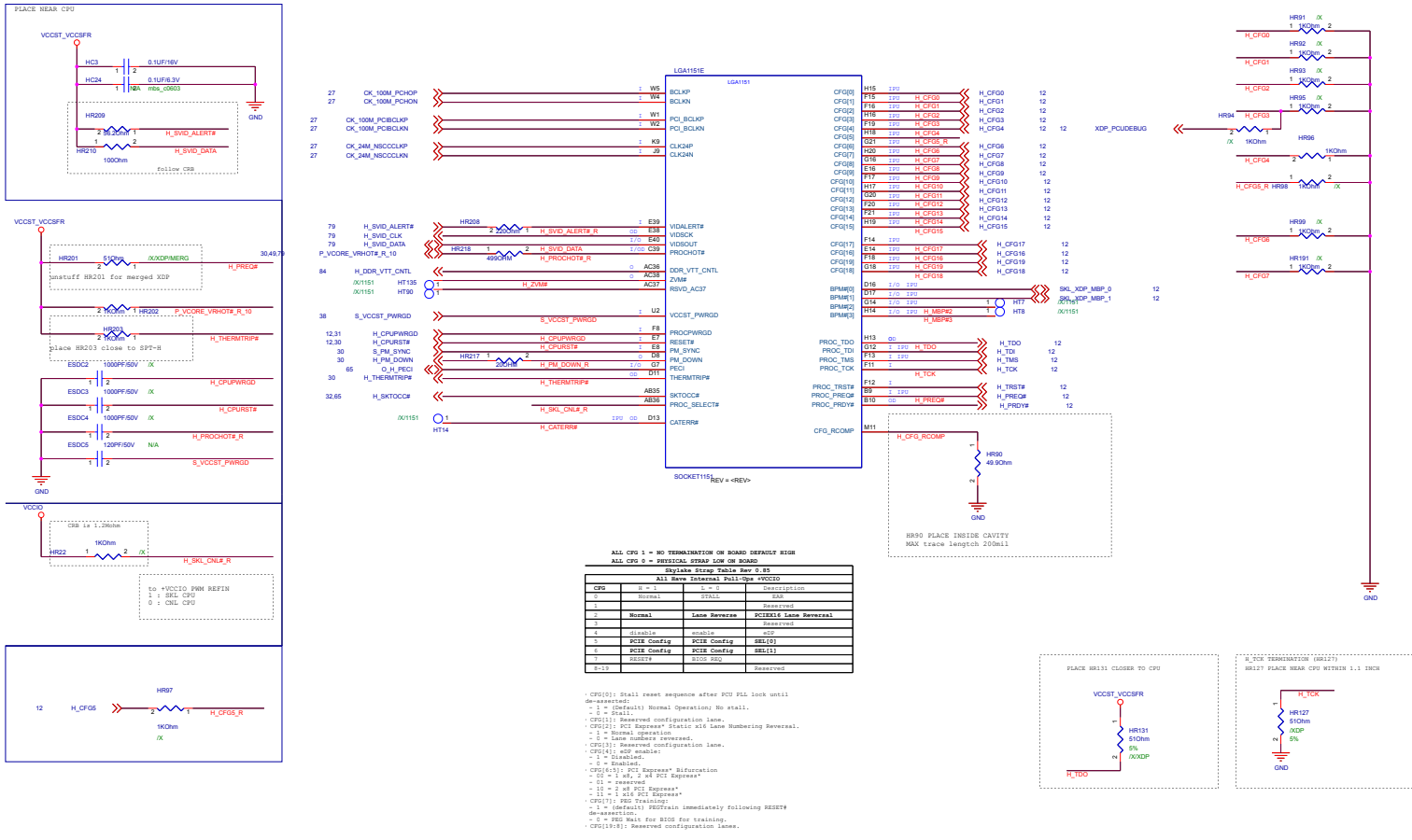

Switch ON/OFF
Linear
Switching
Control signal
Power Rail
+12V_CPU
+12V
+5V
+5VSB_ATX
+3V
AS358MTR-E1+PH6030DLB*2
+12V、+3V
+VCCIO
0.95V (5.31A)
S0
ASP1400BMNTXG 4+2
PH6030*2+PH4030*2
PH6030*1+PH4030*2
+VCCIO_PG
VCORE+VCCGT
0.55 ~ 1.55V
S0
UP1540PDDA
PH6030DLB*1+PH6030DLB*1
+VCCIO_PG
VCCSA
1.05V(11A)
S0
+5V
PH6030DLB + EMB20P03A
+5VSB_DUAL
S0/S3
RT8125DGQW
PH6030*1+PH6030*1
+VPPDDR_PGD_10
+1.2VDUAL
1.2V (12.87A+0.75A)
S0/S3
APL5337KAI-TRG
VTTDDR
0.6V (0.75A)
S0
+5VSB_ATX
+5V
PH6030DLB + EMB45P03P
+5VSB
S0/S3/S5/DS5
+5VSB_ATX
O_PWROK
NB671GQ-Z
S_SLP_S4#
+VPPDDR
2.5V (2.24A)
S0/S3
HPA02240RVER
+1.8V_A_PG
+1.0V_A
1.0V (7.31A)
S0/S3/S5
AP2306GN
S_SLP_S4#
VCCST_VCCSFR
S0/S3
RT8065ZQW
SLP_SUS_N
+1.8V_A
1.8V (2.06A)
S0/S3/S5
UZ2085G-AD-TN3-R
3.3V
+3VSB_ATX
S0/S3/S5
P06P03LCG
+3VSB
3.3V
S0/S3/S5
APL5930QBI-TRG
P_+VDDQ_PG_10
+VCCSFR_OC
1.2V
S0


LGA1151C
LGA1151
PEG_RXP[0]
PEG_RXN[0]
PEG_TXP[0]
PEG_TXN[0]
H_X16_SL1_RXP0
H_X16_SL1_RXN0
H_X16_SL1_TXP0
H_X16_SL1_TXN0
PEG_RXP[1]
PEG_RXN[1]
PEG_TXP[1]
PEG_TXN[1]
H_X16_SL1_RXP1
H_X16_SL1_RXN1
H_X16_SL1_TXP1
H_X16_SL1_TXN1
PEG_RXP[2]
PEG_RXN[2]
PEG_TXP[2]
PEG_TXN[2]
H_X16_SL1_RXP2
H_X16_SL1_RXN2
H_X16_SL1_TXP2
H_X16_SL1_TXN2
PEG_RXP[3]
PEG_RXN[3]
PEG_TXP[3]
PEG_TXN[3]
H_X16_SL1_RXP3
H_X16_SL1_RXN3
H_X16_SL1_TXP3
H_X16_SL1_TXN3
PEG_RXP[4]
PEG_RXN[4]
PEG_TXP[4]
PEG_TXN[4]
H_X16_SL1_RXP4
H_X16_SL1_RXN4
H_X16_SL1_TXP4
H_X16_SL1_TXN4
PEG_RXP[5]
PEG_RXN[5]
PEG_TXP[5]
PEG_TXN[5]
H_X16_SL1_RXP5
H_X16_SL1_RXN5
H_X16_SL1_TXP5
H_X16_SL1_TXN5
PEG_RXP[6]
PEG_RXN[6]
PEG_TXP[6]
PEG_TXN[6]
H_X16_SL1_RXP6
H_X16_SL1_RXN6
H_X16_SL1_TXP6
H_X16_SL1_TXN6
PEG_RXP[7]
PEG_RXN[7]
PEG_TXP[7]
PEG_TXN[7]
H_X16_SL1_RXP7
H_X16_SL1_RXN7
H_X16_SL1_TXP7
H_X16_SL1_TXN7
PEG_RXP[8]
PEG_RXN[8]
PEG_TXP[8]
PEG_TXN[8]
H_X16_SL1_RXP8
H_X16_SL1_RXN8
H_X16_SL1_TXP8
H_X16_SL1_TXN8
PEG_RXP[9]
PEG_RXN[9]
PEG_TXP[9]
PEG_TXN[9]
H_X16_SL1_RXP9
H_X16_SL1_RXN9
H_X16_SL1_TXP9
H_X16_SL1_TXN9
PEG_RXP[10]
PEG_RXN[10]
PEG_TXP[10]
PEG_TXN[10]
H_X16_SL1_RXP10
H_X16_SL1_RXN10
H_X16_SL1_TXP10
H_X16_SL1_TXN10
PEG_RXP[11]
PEG_RXN[11]
PEG_TXP[11]
PEG_TXN[11]
H_X16_SL1_RXP11
H_X16_SL1_RXN11
H_X16_SL1_TXP11
H_X16_SL1_TXN11
PEG_RXP[12]
PEG_RXN[12]
PEG_TXP[12]
PEG_TXN[12]
H_X16_SL1_RXP12
H_X16_SL1_RXN12
H_X16_SL1_TXP12
H_X16_SL1_TXN12
PEG_RXP[13]
PEG_RXN[13]
PEG_TXP[13]
PEG_TXN[13]
H_X16_SL1_RXP13
H_X16_SL1_RXN13
H_X16_SL1_TXP13
H_X16_SL1_TXN13
PEG_RXP[14]
PEG_RXN[14]
PEG_TXP[14]
PEG_TXN[14]
H_X16_SL1_RXP14
H_X16_SL1_RXN14
H_X16_SL1_TXP14
H_X16_SL1_TXN14
PEG_RXP[15]
PEG_RXN[15]
PEG_TXP[15]
PEG_TXN[15]
H_X16_SL1_RXP15
H_X16_SL1_RXN15
H_X16_SL1_TXP15
H_X16_SL1_TXN15
VCCIO
HR52
24.9Ohm
H_PEG_RCOMP
PLACE HR52 Inside CPU Cavity
Trace W/S: 12/15 mils, Length: 400mils
PEG_RCOMP
DMI_RXP[0]
DMI_RXN[0]
DMI_TXP[0]
DMI_TXN[0]
H_DMI_RXP0
H_DMI_RXN0
H_DMI_TXP0
H_DMI_TXN0
DMI_RXP[1]
DMI_RXN[1]
DMI_TXP[1]
DMI_TXN[1]
H_DMI_RXP1
H_DMI_RXN1
H_DMI_TXP1
H_DMI_TXN1
DMI_RXP[2]
DMI_RXN[2]
DMI_TXP[2]
DMI_TXN[2]
H_DMI_RXP2
H_DMI_RXN2
H_DMI_TXP2
H_DMI_TXN2
DMI_RXP[3]
DMI_RXN[3]
DMI_TXP[3]
DMI_TXN[3]
H_DMI_RXP3
H_DMI_RXN3
H_DMI_TXP3
H_DMI_TXN3
SOCKET1151
REV = <REV>


LGA1151D
LGA1151
DVI
20 H_DVI_TXDP2
20 H_DVI_TXDN2
20 H_DVI_TXDP1
20 H_DVI_TXDN1
20 H_DVI_TXDP0
20 H_DVI_TXDN0
20 H_DVI_TXCP
20 H_DVI_TXCN
C21 DDI1_TXP[0]
D21 DDI1_TXN[0]
D22 DDI1_TXP[1]
E22 DDI1_TXN[1]
B23 DDI1_TXP[2]
A23 DDI1_TXN[2]
C23 DDI1_TXP[3]
D23 DDI1_TXN[3]
/X/1151 HT9
/X/1151 HT10
B13 DDI1_AUXP
C13 DDI1_AUXN
HDMI
18 H_HDMI_TXDP2
18 H_HDMI_TXDN2
18 H_HDMI_TXDP1
18 H_HDMI_TXDN1
18 H_HDMI_TXDP0
18 H_HDMI_TXDN0
18 H_HDMI_TXCP
18 H_HDMI_TXCN
B18 DDI2_TXP[0]
A18 DDI2_TXN[0]
D18 DDI2_TXP[1]
E18 DDI2_TXN[1]
C19 DDI2_TXP[2]
D19 DDI2_TXN[2]
D20 DDI2_TXP[3]
E20 DDI2_TXN[3]
/X/1151 HT11
/X/1151 HT12
A12 DDI2_AUXP
B12 DDI2_AUXN
DP
B14 DDI3_TXP[0]
A14 DDI3_TXN[0]
C15 DDI3_TXP[1]
B15 DDI3_TXN[1]
B16 DDI3_TXP[2]
A16 DDI3_TXN[2]
C17 DDI3_TXP[3]
B17 DDI3_TXN[3]
B11 DDI3_AUXP
C11 DDI3_AUXN
SOCKET1151
REV = <REV>
EDP_TXP[0]
EDP_TXN[0]
EDP_TXP[1]
EDP_TXN[1]
EDP_TXN[2]
EDP_TXP[2]
EDP_TXN[3]
EDP_TXP[3]
EDP_AUXP
EDP_AUXN
EDP_DISP_UTIL
EDP_RCOMP
PROC_AUDIO_CLK
PROC_AUDIO_SDI
PROC_AUDIO_SDO
E10 HT1
D10 HT2
D9 HT3
C9 HT4
H10
G10 H_DP2VGA_TXN0 21
G9 H_DP2VGA_TXP0 21
F9 H_DP2VGA_TXN1 21
H_DP2VGA_TXP1 21
D12 H_DP2VGA_AUXP 21
E12 H_DP2VGA_AUXN 21
DP to VGA IC
D14 HT5
H_EDP_DISP_UTIL
VCCIO
M9
H_DP_RCOMP
HR61
24.9Ohm
Place Inside CPU Cavity
traace W/S:12/25, max lengtch 200mil
V3
V2
U1
33Ohm
S_HDA_SCLK 31
S_HDA_SDO_R 31
H_HDA_SDI 31
H_HDA_SDI_R
HR1 place close CPU
HR1
total lengtch <4,max=200
total lengtch >4,max=1000


Channel A
4 Layer routing
13
D4_DQ_A[0:63]
LGA1151A
LGA1151
DDR0_DQ[0]
DDR0_DQ[1]
DDR0_DQ[2]
DDR0_DQ[3]
DDR0_DQ[4]
DDR0_DQ[5]
DDR0_DQ[6]
DDR0_DQ[7]
DDR0_DQ[8]
DDR0_DQ[9]
DDR0_DQ[10]
DDR0_DQ[11]
DDR0_DQ[12]
DDR0_DQ[13]
DDR0_DQ[14]
DDR0_DQ[15]
DDR0_DQ[16]/DDR0_DQ[32]
DDR0_DQ[17]/DDR0_DQ[33]
DDR0_DQ[18]/DDR0_DQ[34]
DDR0_DQ[19]/DDR0_DQ[35]
DDR0_DQ[20]/DDR0_DQ[36]
DDR0_DQ[21]/DDR0_DQ[37]
DDR0_DQ[22]/DDR0_DQ[38]
DDR0_DQ[23]/DDR0_DQ[39]
DDR0_DQ[24]/DDR0_DQ[40]
DDR0_DQ[25]/DDR0_DQ[41]
DDR0_DQ[26]/DDR0_DQ[42]
DDR0_DQ[27]/DDR0_DQ[43]
DDR0_DQ[28]/DDR0_DQ[44]
DDR0_DQ[29]/DDR0_DQ[45]
DDR0_DQ[30]/DDR0_DQ[46]
DDR0_DQ[31]/DDR0_DQ[47]
DDR0_DQ[32]/DDR1_DQ[0]
DDR0_DQ[33]/DDR1_DQ[1]
DDR0_DQ[34]/DDR1_DQ[2]
DDR0_DQ[35]/DDR1_DQ[3]
DDR0_DQ[36]/DDR1_DQ[4]
DDR0_DQ[37]/DDR1_DQ[5]
DDR0_DQ[38]/DDR1_DQ[6]
DDR0_DQ[39]/DDR1_DQ[7]
DDR0_DQ[40]/DDR1_DQ[8]
DDR0_DQ[41]/DDR1_DQ[9]
DDR0_DQ[42]/DDR1_DQ[10]
DDR0_DQ[43]/DDR1_DQ[11]
DDR0_DQ[44]/DDR1_DQ[12]
DDR0_DQ[45]/DDR1_DQ[13]
DDR0_DQ[46]/DDR1_DQ[14]
DDR0_DQ[47]/DDR1_DQ[15]
DDR0_DQ[48]/DDR1_DQ[32]
DDR0_DQ[49]/DDR1_DQ[33]
DDR0_DQ[50]/DDR1_DQ[34]
DDR0_DQ[51]/DDR1_DQ[35]
DDR0_DQ[52]/DDR1_DQ[36]
DDR0_DQ[53]/DDR1_DQ[37]
DDR0_DQ[54]/DDR1_DQ[38]
DDR0_DQ[55]/DDR1_DQ[39]
DDR0_DQ[56]/DDR1_DQ[40]
DDR0_DQ[57]/DDR1_DQ[41]
DDR0_DQ[58]/DDR1_DQ[42]
DDR0_DQ[59]/DDR1_DQ[43]
DDR0_DQ[60]/DDR1_DQ[44]
DDR0_DQ[61]/DDR1_DQ[45]
DDR0_DQ[62]/DDR1_DQ[46]
DDR0_DQ[63]/DDR1_DQ[47]
DDR0_ECC[0]
DDR0_ECC[1]
DDR0_ECC[2]
DDR0_ECC[3]
DDR0_ECC[4]
DDR0_ECC[5]
DDR0_ECC[6]
DDR0_ECC[7]
DDR CHANNEL A
SOCKET1151
DDR0_CKP[0]
DDR0_CKN[0]
DDR0_CKP[1]
DDR0_CKN[1]
DDR0_CKP[2]
DDR0_CKN[2]
DDR0_CKP[3]
DDR0_CKN[3]
D4_MA_CLK0
D4_MA_CLK#0
D4_MA_CLK1
D4_MA_CLK#1
DDR0_CKE[0]
DDR0_CKE[1]
DDR0_CKE[2]
DDR0_CKE[3]
D4_CKE_A0
D4_CKE_A1
DDR0_CS#[0]
DDR0_CS#[1]
DDR0_CS#[2]
DDR0_CS#[3]
D4_CS_A#0
D4_CS_A#1
DDR0_ODT[0]
DDR0_ODT[1]
DDR0_ODT[2]
DDR0_ODT[3]
D4_ODT_A0
D4_ODT_A1
DDR0_BA[0]
DDR0_BA[1]
DDR0_BA[2]
/DDR0_CAB4)/DDR0_BA[0]
/DDR0_CAB5)/DDR0_BA[1]
/DDR0_CAA(5)/DDR0_BG[0]
D4_BAA0
D4_BAA1
D4_BGA0
D4_MAA[0:16]
DDR0_RAS#
DDR0_WE#
DDR0_CAS#
/DDR0_CAB(3)/DDR0_MA[16]
/DDR0_CAB(2)/DDR0_MA[14]
/DDR0_CAB(1)/DDR0_MA[15]
D4_MAA16
D4_MAA14
D4_MAA15
DDR0_MA[0]
DDR0_MA[1]
DDR0_MA[2]
/DDR0_CAB(9)/DDR0_MA[0]
/DDR0_CAB(8)/DDR0_MA[1]
/DDR0_CAB(5)/DDR0_MA[2]
DDR0_MA[3]
DDR0_MA[4]
D4_MAA0
D4_MAA1
D4_MAA2
D4_MAA3
D4_MAA4
D4_MAA5
D4_MAA6
D4_MAA7
D4_MAA8
D4_MAA9
D4_MAA10
D4_MAA11
D4_MAA12
D4_MAA13
DDR0_MA[5]
DDR0_MA[6]
DDR0_MA[7]
DDR0_MA[8]
DDR0_MA[9]
DDR0_MA[10]
DDR0_MA[11]
DDR0_MA[12]
DDR0_MA[13]
DDR0_MA[14]
DDR0_MA[15]
/DDR0_CAA(0)/DDR0_MA[5]
/DDR0_CAA(2)/DDR0_MA[6]
/DDR0_CAA(4)/DDR0_MA[7]
/DDR0_CAA(3)/DDR0_MA[8]
/DDR0_CAA(1)/DDR0_MA[9]
/DDR0_CAB(7)/DDR0_MA[10]
/DDR0_CAA(7)/DDR0_MA[11]
/DDR0_CAA(6)/DDR0_MA[12]
/DDR0_CAB(0)/DDR0_MA[13]
/DDR0_CAA(8)/DDR0_BG[1]
/DDR0_CAA(8)/DDR0_ACT#
D4_BGA1
D4_A_ACT#
DDR0_PAR
DDR0_ALERT#
D4_A_PAR
D4_A_ALERT#
DDR0_DQSN[0]
DDR0_DQSN[1]
DDR0_DQSN[2]/DDR0_DQSN[4]
DDR0_DQSN[3]/DDR0_DQSN[5]
DDR0_DQSN[4]/DDR1_DQSN[0]
DDR0_DQSN[5]/DDR1_DQSN[1]
DDR0_DQSN[6]/DDR1_DQSN[4]
DDR0_DQSN[7]/DDR1_DQSN[5]
D4_DQS_A#0
D4_DQS_A#1
D4_DQS_A#2
D4_DQS_A#3
D4_DQS_A#4
D4_DQS_A#5
D4_DQS_A#6
D4_DQS_A#7
DDR0_DQSP[0]
DDR0_DQSP[1]
DDR0_DQSP[2]/DDR0_DQSP[4]
DDR0_DQSP[3]/DDR0_DQSP[5]
DDR0_DQSP[4]/DDR1_DQSP[0]
DDR0_DQSP[5]/DDR1_DQSP[1]
DDR0_DQSP[6]/DDR1_DQSP[4]
DDR0_DQSP[7]/DDR1_DQSP[5]
D4_DQS_A0
D4_DQS_A1
D4_DQS_A2
D4_DQS_A3
D4_DQS_A4
D4_DQS_A5
D4_DQS_A6
D4_DQS_A7
DDR0_DQSP[8]
DDR0_DQSN[8]


Follow CRB
Channel B
4 Layer routing
14
D4_DQ_B[0:63]
LGA1151B
LGA1151
D4_DQ_B4
D4_DQ_B5
D4_DQ_B7
D4_DQ_B3
D4_DQ_B1
D4_DQ_B0
D4_DQ_B6
D4_DQ_B2
D4_DQ_B13
D4_DQ_B9
D4_DQ_B14
D4_DQ_B15
D4_DQ_B12
D4_DQ_B8
D4_DQ_B10
D4_DQ_B11
D4_DQ_B16
D4_DQ_B20
D4_DQ_B22
D4_DQ_B23
D4_DQ_B17
D4_DQ_B21
D4_DQ_B18
D4_DQ_B19
D4_DQ_B25
D4_DQ_B24
D4_DQ_B30
D4_DQ_B26
D4_DQ_B29
D4_DQ_B27
D4_DQ_B31
D4_DQ_B32
D4_DQ_B33
D4_DQ_B35
D4_DQ_B34
D4_DQ_B36
D4_DQ_B37
D4_DQ_B39
D4_DQ_B38
D4_DQ_B44
D4_DQ_B45
D4_DQ_B46
D4_DQ_B42
D4_DQ_B41
D4_DQ_B40
D4_DQ_B47
D4_DQ_B43
D4_DQ_B52
D4_DQ_B53
D4_DQ_B55
D4_DQ_B51
D4_DQ_B48
D4_DQ_B49
D4_DQ_B54
D4_DQ_B50
D4_DQ_B61
D4_DQ_B56
D4_DQ_B63
D4_DQ_B58
D4_DQ_B60
D4_DQ_B57
D4_DQ_B59
D4_DQ_B62
DDR1_DQ[0]/DDR0_DQ[16]
DDR1_DQ[1]/DDR0_DQ[17]
DDR1_DQ[2]/DDR0_DQ[18]
DDR1_DQ[3]/DDR0_DQ[19]
DDR1_DQ[4]/DDR0_DQ[20]
DDR1_DQ[5]/DDR0_DQ[21]
DDR1_DQ[6]/DDR0_DQ[22]
DDR1_DQ[7]/DDR0_DQ[23]
DDR1_DQ[8]/DDR0_DQ[24]
DDR1_DQ[9]/DDR0_DQ[25]
DDR1_DQ[10]/DDR0_DQ[26]
DDR1_DQ[11]/DDR0_DQ[27]
DDR1_DQ[12]/DDR0_DQ[28]
DDR1_DQ[13]/DDR0_DQ[29]
DDR1_DQ[14]/DDR0_DQ[30]
DDR1_DQ[15]/DDR0_DQ[31]
DDR1_DQ[16]
DDR1_DQ[17]
DDR1_DQ[18]
DDR1_DQ[19]
DDR1_DQ[20]
DDR1_DQ[21]
DDR1_DQ[22]
DDR1_DQ[23]
DDR1_DQ[24]
DDR1_DQ[25]
DDR1_DQ[26]
DDR1_DQ[27]
DDR1_DQ[28]
DDR1_DQ[29]
DDR1_DQ[30]
DDR1_DQ[31]
DDR1_ECC[0]
DDR1_ECC[1]
DDR1_ECC[2]
DDR1_ECC[3]
DDR1_ECC[4]
DDR1_ECC[5]
DDR1_ECC[6]
DDR1_ECC[7]
DDR CHANNEL B
DDR1_CKP[5]
DDR1_CKN[5]
DDR1_CKP[0]
DDR1_CKN[0]
DDR1_CKP[2]
DDR1_CKN[2]
DDR1_CKP[3]
DDR1_CKN[3]
DDR1_CKE[5]
DDR1_CKE[1]
DDR1_CKE[2]
DDR1_CKE[3]
DDR1_CS#[5]
DDR1_CS#[1]
DDR1_CS#[2]
DDR1_CS#[3]
DDR1_ODT[5]
DDR1_ODT[1]
DDR1_ODT[2]
DDR1_ODT[3]
DDR3_RAS#
DDR3_WE#
DDR3_CAS#
DDR3_BA[0]
DDR3_BA[1]
DDR3_BA[2]
DDR3_MA[0]
DDR3_MA[1]
DDR3_MA[2]
DDR3_MA[5]
DDR3_MA[6]
DDR3_MA[7]
DDR3_MA[8]
DDR3_MA[9]
DDR3_MA[10]
DDR3_MA[11]
DDR3_MA[12]
DDR3_MA[13]
DDR3_MA[14]
DDR3_MA[15]
/DDR1_CAB[5]/DDR1_MA[16]
/DDR1_CAB[2]/DDR1_MA[14]
/DDR1_CAB[1]/DDR1_MA[15]
/DDR1_CAA[5]/DDR1_BA[0]
/DDR1_CAB[4]/DDR1_BA[1]
/DDR1_CAA[3]/DDR1_BG[0]
/DDR1_CAB[3]/DDR1_MA[0]
/DDR1_CAB[0]/DDR1_MA[1]
/DDR1_CAB[5]/DDR1_MA[2]
DDR1_MA[5]
DDR1_MA[4]
/DDR1_CAA[3]/DDR1_MA[5]
/DDR1_CAA[2]/DDR1_MA[6]
/DDR1_CAA[4]/DDR1_MA[7]
/DDR1_CAA[3]/DDR1_MA[8]
/DDR1_CAA[1]/DDR1_MA[9]
/DDR1_CAB[7]/DDR1_MA[10]
/DDR1_CAA[7]/DDR1_MA[11]
/DDR1_CAB[5]/DDR1_MA[12]
/DDR1_CAB[0]/DDR1_MA[13]
/DDR1_CAA[6]/DDR1_BG[1]
/DDR1_CAA[5]/DDR1_ACT#
DDR1_PAR
DDR1_ALERT#
DDR1_DQSN[0]/DDR0_DQSN[2]
DDR1_DQSN[1]/DDR0_DQSN[3]
DDR1_DQSN[2]/DDR0_DQSN[8]
DDR1_DQSN[3]/DDR0_DQSN[7]
DDR1_DQSN[4]/DDR1_DQSN[2]
DDR1_DQSN[5]/DDR1_DQSN[3]
DDR1_DQSN[6]
DDR1_DQSN[7]
DDR1_DQSP[0]/DDR0_DQSP[2]
DDR1_DQSP[1]/DDR0_DQSP[3]
DDR1_DQSP[2]/DDR0_DQSP[8]
DDR1_DQSP[3]/DDR0_DQSP[7]
DDR1_DQSP[4]/DDR1_DQSP[2]
DDR1_DQSP[5]/DDR1_DQSP[3]
DDR1_DQSP[6]
DDR1_DQSP[7]
DDR1_DQSP[8]
DDR1_DQSN[8]
DDR_VREF_CA
DDR0_VREF_DQ
DDR1_VREF_DQ
SOCKET1151
REV = <REV>
D4_MB_CLK0
D4_MB_CLK0#
D4_MB_CLK1
D4_MB_CLK1#
D4_CKE_B0
D4_CKE_B1
D4_CS_B#0
D4_CS_B#1
D4_ODT_B0
D4_ODT_B1
D4_MA[0:16]
D4_MA#16
D4_MA#14
D4_MA#15
D4_BA#0
D4_BA#1
D4_BG#0
D4_MA0
D4_MA1
D4_MA2
D4_MA3
D4_MA4
D4_MA5
D4_MA6
D4_MA7
D4_MA8
D4_MA9
D4_MA#10
D4_MA11
D4_MA#12
D4_MA#13
D4_BG#1
D4_B_ACT#
D4_B_PAR
D4_B_ALERT#
D4_DQS_B#0
D4_DQS_B#1
D4_DQS_B#2
D4_DQS_B#3
D4_DQS_B#4
D4_DQS_B#5
D4_DQS_B#6
D4_DQS_B#7
D4_DQS_B0
D4_DQS_B1
D4_DQS_B2
D4_DQS_B3
D4_DQS_B4
D4_DQS_B5
D4_DQS_B6
D4_DQS_B7
H_D4_VREFCA_A
H_D4_VREFCA_B
TP_DIMM_DQ0
HT6
HC3
0.022UF/16V
HC6
0.022UF/16V
HR2
24.9Ohm
HR3
24.9Ohm
GND
GND
CRB & Z97
High frequency
termination, can absorb
any high frequency
noise coming from
CPU/board crosstalk.

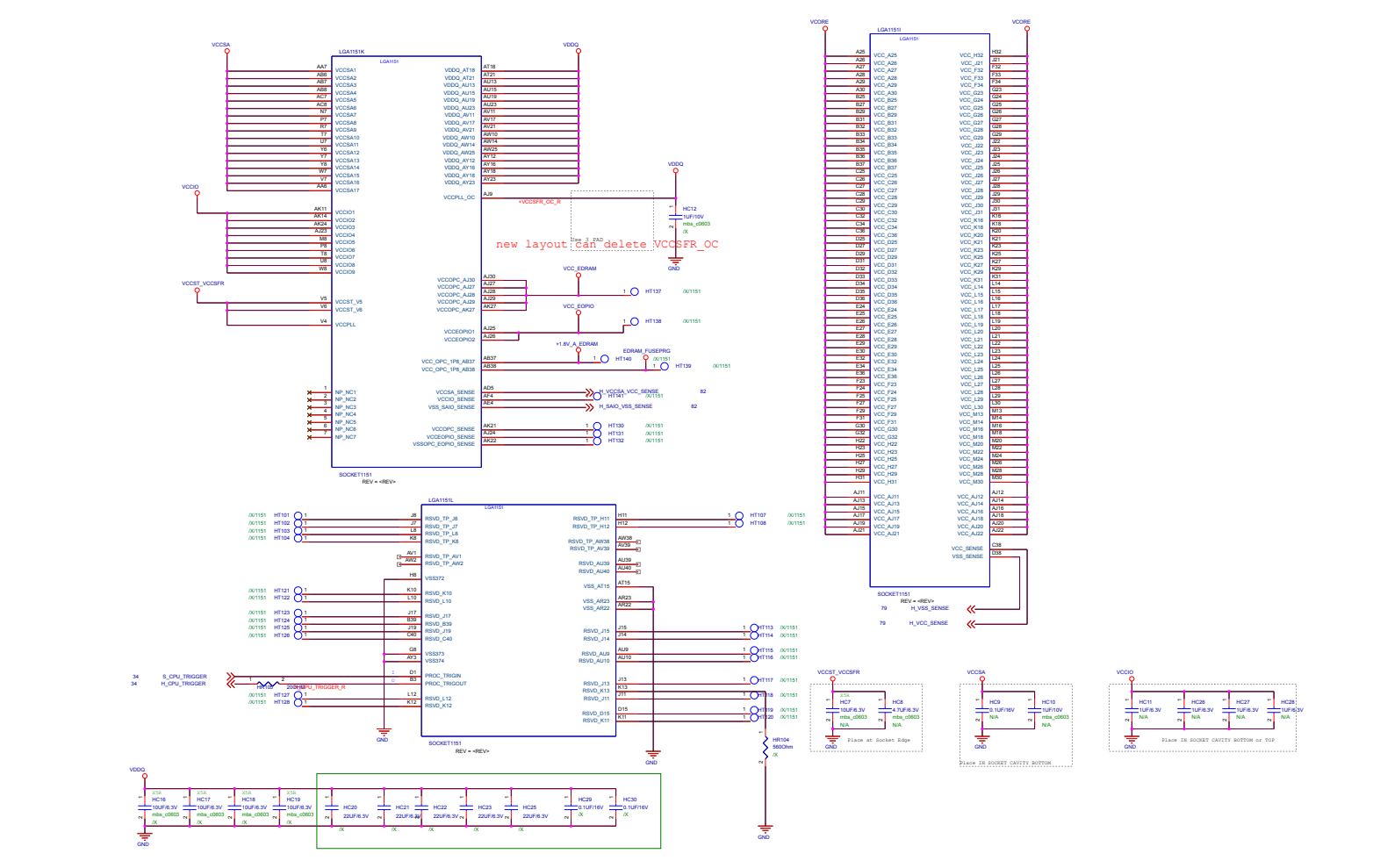


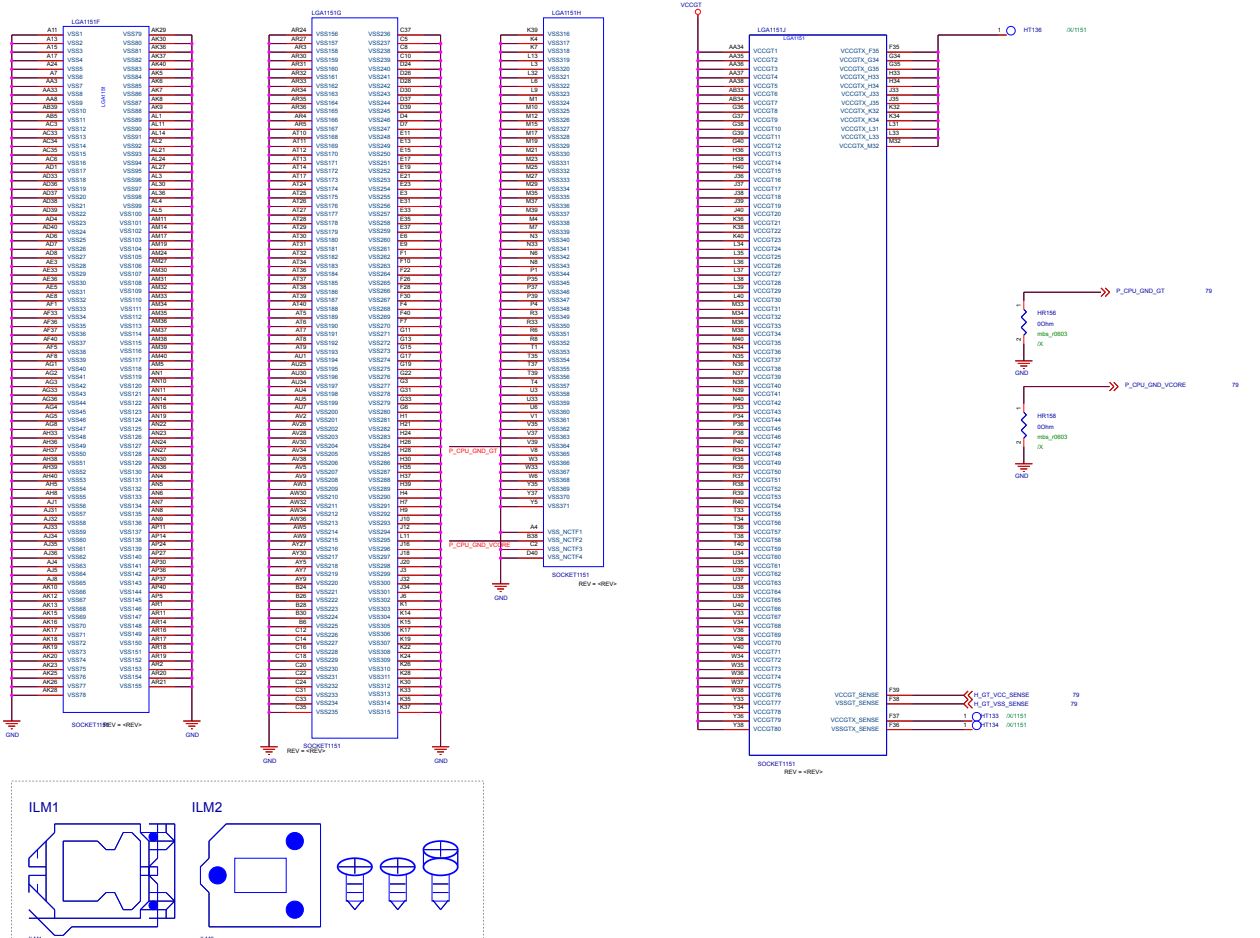
ALL CFG 1 = NO TERMINATION ON BOARD DEFAULT HIGH
ALL CFG 0 = PHYSICAL STRAP LOW OR BOARD

Skylake Strap Table Rev 0.85

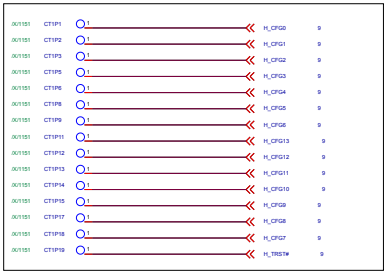
	All Have Internal Pull-Ups +VCCIO		
CFG	X = 1	X = 0	Description
0	Normal	STALL	EAR
1			Reserved
2	**Normal**	**Lane Reverse**	**PCIEX16 Lane Reversal**
3			Reserved
4	disable	enable	eDP
5	**PCIE Config**	**PCIE Config**	**SEL[0]**
6	**PCIE Config**	**PCIE Config**	**SEL[1]**
7	RESET#	BIOS REQ	
8-19			Reserved

- CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted:
  - 1 = (Default) Normal Operation; No stall.
  - 0 = Stall.
- CFG[1]: Reserved configuration lane.
- CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation.
  - 0 = Lanes numbered reversed.
- CFG[3]: Reserved configuration lane.
- CFG[4]: eDP enable:
  - 1 = Disabled.
  - 0 = Enabled.
- CFG[6:5]: PCI Express* Bifurcation
  - 00 = 1 x8, 2 x4 PCI Express*
  - 01 = reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x16 PCI Express*
- CFG[7]: PEG Training:
  - 1 = (default) PEGTrain immediately following RESET# de-assertion.
  - 0 = PEG Wait for BIOS for training.
- CFG[19:8]: Reserved configuration lanes.

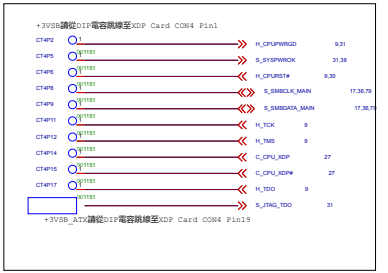

VCCSA
VDDQ
VCCIO
VCCST_VCCSFR
VCCPLL
LGA1151K
LGA1151
SOCKET1151
REV = <REV>
VCCSA_SENSE
VCCIO_SENSE
VSS_SAIO_SENSE
VCCOPC_SENSE
VCCEOPIO_SENSE
VSSOPC_EOPIO_SENSE
VCCPLL_OC
+VCCSFR_OC_R
1mm 3 PAD
new layout can delete VCCSFR_OC
HC12
1UF/10V
mba_c0603
VCC_EDRAM
VCC_EOPIO
+1.8V_A_EDRAM
EDRAM_FUSEPRG
H_VCCSA VCC_SENSE
H_SAIO_VSS_SENSE
LGA1151L
RSVD_TP_AV1
RSVD_TP_AV2
VSS372
RSVD_K10
RSVD_L10
RSVD_J17
RSVD_B39
RSVD_J19
RSVD_C40
VSS373
VSS374
PROC_TRIGIN
PROC_TRIGOUT
RSVD_L12
RSVD_K12
RSVD_TP_HH1
RSVD_TP_HH2
RSVD_TP_AW38
RSVD_TP_AV39
RSVD_AU39
RSVD_AU40
VSS_AT15
VSS_AR23
VSS_AR22
RSVD_J15
RSVD_J14
RSVD_AU9
RSVD_AU10
RSVD_J13
RSVD_K13
RSVD_J11
RSVD_D15
RSVD_K11
S_CPU_TRIGGER
H_CPU_TRIGGER
200HB
H_CPU_TRIGGER_R
HR104
360Ohm
LGA1151I
VCC_SENSE
VSS_SENSE
H_VSS_SENSE
H_VCC_SENSE
VCCST_VCCSFR
VCCSA
VCCIO
Place at Socket Edge
Place IN SOCKET CAVITY BOTTOM
Place IN SOCKET CAVITY BOTTOM or TOP
VDDQ
GND


LGA1151F
LGA1151G
LGA1151H
LGA1151J
SOCKET1151
REV = <REV>
GND
VCCGT
P_CPU_GND_GT
P_CPU_GND_VCORE
HT136
HT133
HT134
HR156
HR158
0Ohm
mba_r0603
ILM1
ILM2

XDP Card USB3 CON1



XDP Card USB3 CON4



Naming Rule:

CTxPy==>請跳線到XDP Card CONx connector的Piny

Placement Rule:

此頁面測點全部放置背面靠近輸出端,

Layout會協助把Reference文字面開出,

若有需求初期PCB版本可洗背面文字,

但低階機種PVT PCB版本請記得通知板廠不洗背面文字

Power Rework:

+1.0V_A請從DIP電容跳線至XDP Card CON2 Pin19

+3VSB請從DIP電容跳線至XDP Card CON4 Pin1

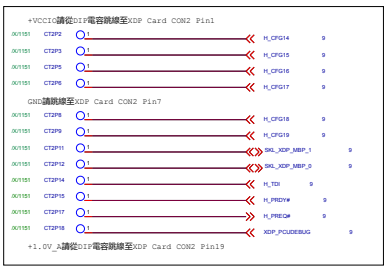
+VCCST請從DIP電容跳線至XDP Card CON3 Pin19

+VCCIC請從DIP電容跳線至XDP Card CON2 Pin1

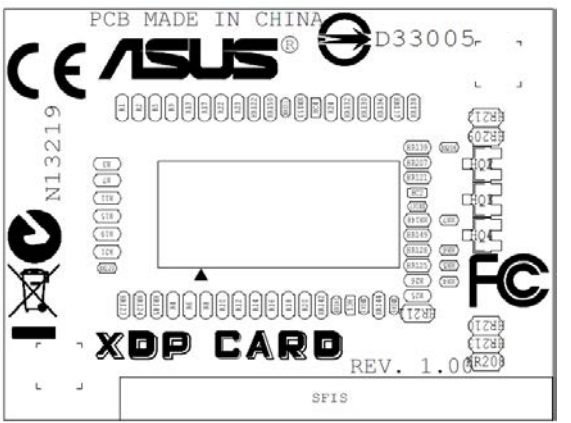
+3VSB_ATX請從DIP電容跳線至XDP Card CON4 Pin19

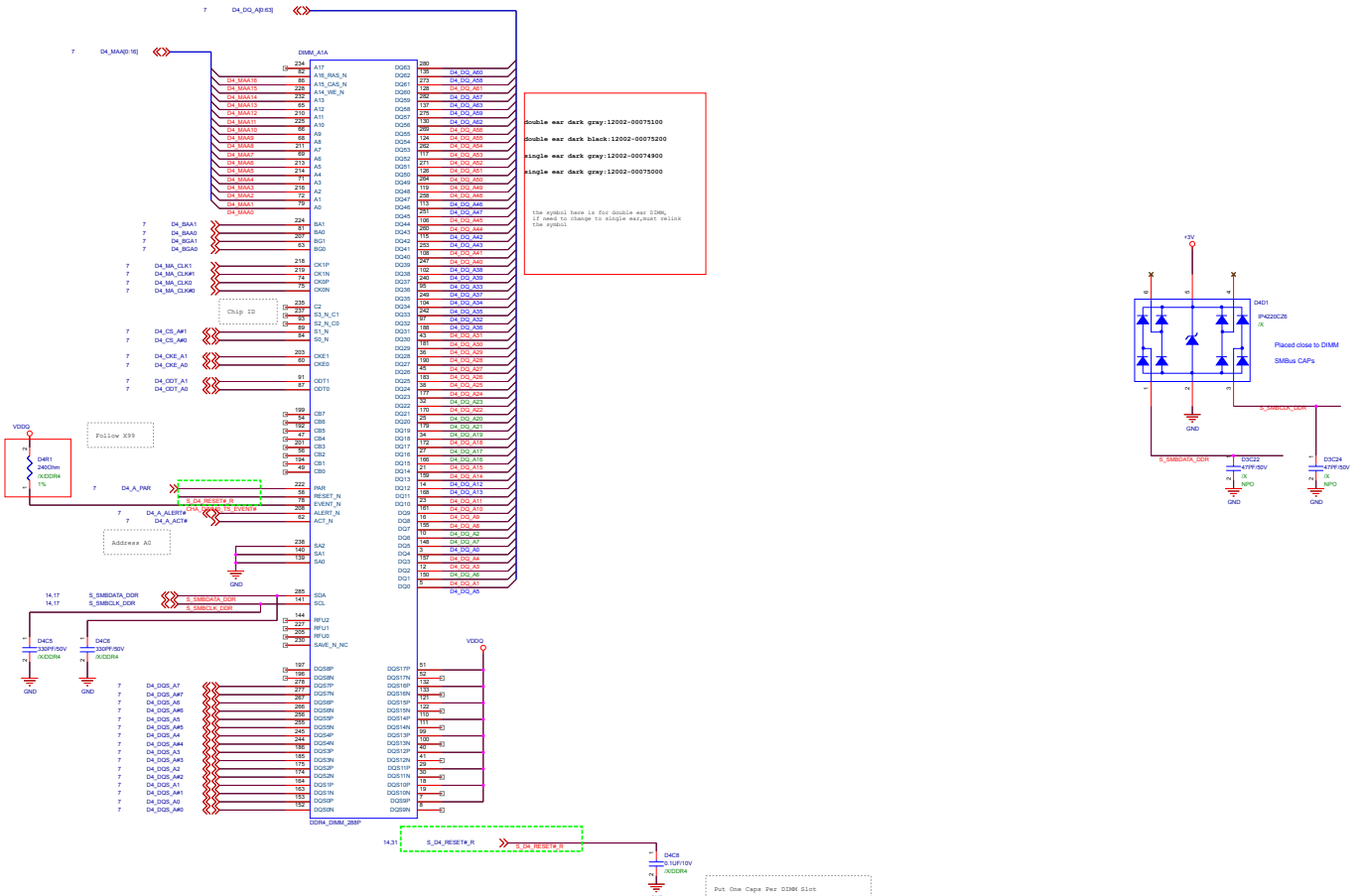
GND請跳線至XDP Card CON2 Pin7

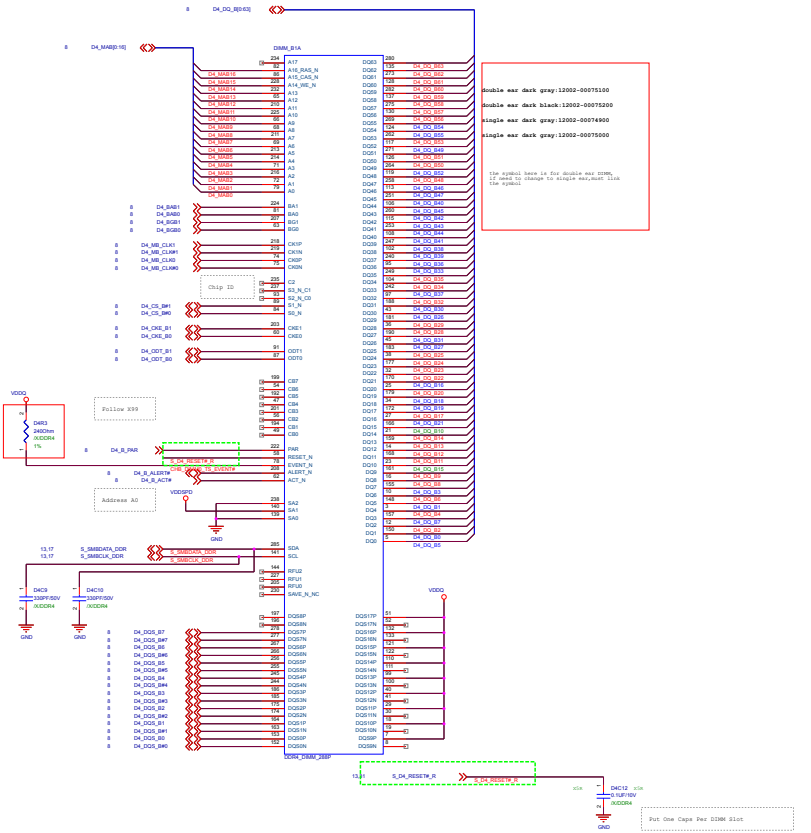
XDP Card USB3 CON2



XDP Card USB3 CON3




DIMM_A1A
DDR4_DIMM_288P
D4_DQ_A[0:63]
D4_MAA[0:16]
double ear dark gray:12002-00075100
double ear dark black:12002-00075200
single ear dark gray:12002-00074900
single ear dark gray:12002-00075000
the symbol here is for double ear DIMM, if need to change to single ear,must relink the symbol
Chip ID
Follow X99
Address A0
D4R1 240Ohm /X/DDR4 1%
D4C5 330PF/50V /X/DDR4
D4C6 330PF/50V /X/DDR4
D4C8 0.1UF/10V /X/DDR4
Put One Caps Per DIMM Slot
S_D4_RESET#_R
S_SMBDATA_DDR
S_SMBCLK_DDR
D4_A_ALERT#
D4_A_ACT#
D4_A_PAR
VDDQ
GND
+3V
D4D1 IP4220CZ6 /X
Placed close to DIMM SMBus CAPs
D3C22 .47PF/50V /X NPO
D3C24 .47PF/50V /X NPO


DIMM_B1A
D4_DQ_B[0:63]
D4_MAB[0:16]
D4_MAB16
D4_MAB15
D4_MAB14
D4_MAB13
D4_MAB12
D4_MAB11
D4_MAB10
D4_MAB9
D4_MAB8
D4_MAB7
D4_MAB6
D4_MAB5
D4_MAB4
D4_MAB3
D4_MAB2
D4_MAB1
D4_MAB0
A17
A16_RAS_N
A15_CAS_N
A14_WE_N
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
D4_BAB1
D4_BAB0
D4_BGB1
D4_BGB0
BA1
BA0
BG1
BG0
D4_MB_CLK1
D4_MB_CLK#1
D4_MB_CLK0
D4_MB_CLK#0
CK1P
CK1N
CK0P
CK0N
Chip ID
C2
S3_N_C1
S2_N_C0
D4_CS_B#1
D4_CS_B#0
S1_N
S0_N
D4_CKE_B1
D4_CKE_B0
CKE1
CKE0
D4_ODT_B1
D4_ODT_B0
ODT1
ODT0
CB7
CB6
CB5
CB4
CB3
CB2
CB1
CB0
D4_B_PAR
PAR
D4_B_RESET#_R
S_D4_RESET#_R
RESET_N
D4_B_ALERT#
CHG_TO_EVENT#
EVENT_N
D4_B_ACT#
ALERT_N
ACT_N
Follow X99
Address A0
VDDIO
D4R3
240Ohm
1%
0402
VDDSPD
SA2
SA1
SA0
GND
13,17
S_SMBDATA_DDR
S_SMBCLK_DDR
S_SMBDATA_DDR
S_SMBCLK_DDR
SDA
SCL
RFU2
RFU1
RFU0
SAVE_N_NC
D4C9
330PF/50V
0402/X5R
D4C10
330PF/50V
0402/X5R
D4_DQS_B7
D4_DQS_B#7
D4_DQS_B6
D4_DQS_B#6
D4_DQS_B5
D4_DQS_B#5
D4_DQS_B4
D4_DQS_B#4
D4_DQS_B3
D4_DQS_B#3
D4_DQS_B2
D4_DQS_B#2
D4_DQS_B1
D4_DQS_B#1
D4_DQS_B0
D4_DQS_B#0
DQS8P
DQS8N
DQS7P
DQS7N
DQS6P
DQS6N
DQS5P
DQS5N
DQS4P
DQS4N
DQS3P
DQS3N
DQS2P
DQS2N
DQS1P
DQS1N
DQS0P
DQS0N
DDR4_VTAO_288P
DQS17P
DQS17N
DQS16P
DQS16N
DQS15P
DQS15N
DQS14P
DQS14N
DQS13P
DQS13N
DQS12P
DQS12N
DQS11P
DQS11N
DQS10P
DQS10N
DQS9P
DQS9N
D4_DQ_B63
D4_DQ_B62
D4_DQ_B61
D4_DQ_B60
D4_DQ_B59
D4_DQ_B58
D4_DQ_B57
D4_DQ_B56
D4_DQ_B55
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D4_DQ_B52
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D4_DQ_B49
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D4_DQ_B47
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D4_DQ_B45
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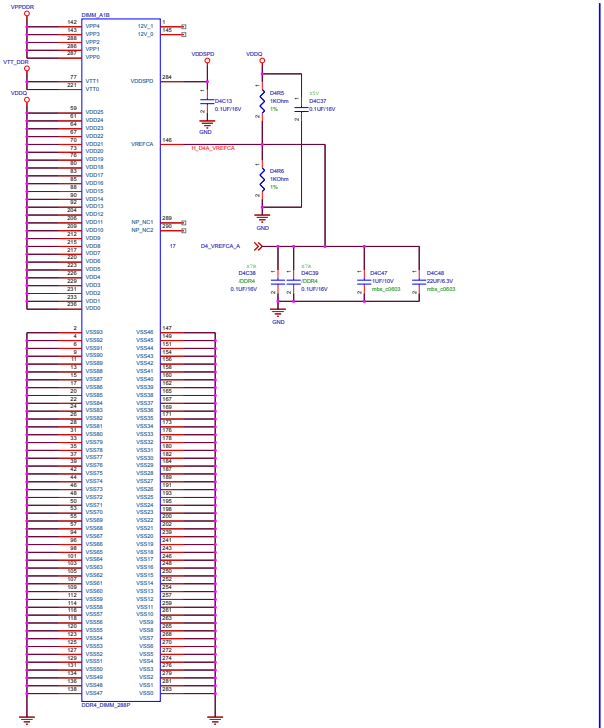
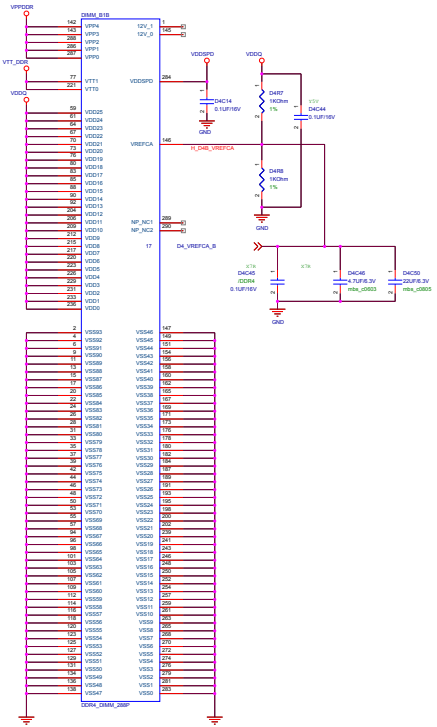
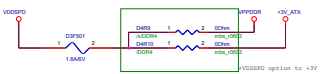
D4_DQ_B42
D4_DQ_B41
D4_DQ_B40
D4_DQ_B39
D4_DQ_B38
D4_DQ_B37
D4_DQ_B36
D4_DQ_B35
D4_DQ_B34
D4_DQ_B33
D4_DQ_B32
D4_DQ_B31
D4_DQ_B30
D4_DQ_B29
D4_DQ_B28
D4_DQ_B27
D4_DQ_B26
D4_DQ_B25
D4_DQ_B24
D4_DQ_B23
D4_DQ_B22
D4_DQ_B21
D4_DQ_B20
D4_DQ_B19
D4_DQ_B18
D4_DQ_B17
D4_DQ_B16
D4_DQ_B15
D4_DQ_B14
D4_DQ_B13
D4_DQ_B12
D4_DQ_B11
D4_DQ_B10
D4_DQ_B9
D4_DQ_B8
D4_DQ_B7
D4_DQ_B6
D4_DQ_B5
D4_DQ_B4
D4_DQ_B3
D4_DQ_B2
D4_DQ_B1
D4_DQ_B0
VDDIO
D4C12
0.1UF/10V
0402/X5R
GND
xlw
Put One Caps Per DIMM Slot
double ear dark gray:12002-00075100
double ear dark black:12002-00075200
single ear dark gray:12002-00074900
single ear dark gray:12002-00075000
the symbol here is for double ear DIMM, if need to change to single ear,must link the symbol

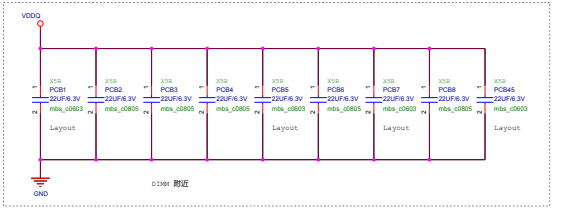

DIMM_A1B
DDR4_DIMM_288P
VPPDDR
VTT_DDR
VDDQ
VDDSPD
VREFCA
GND
D4_VREFCA_A
H_DHA_VREFCA
D4R5
1KOhm
1%
D4R6
1KOhm
1%
D4C13
0.1UF/16V
D4C37
0.1UF/16V
D4C38
/DDR4
0.1UF/16V
D4C39
/DDR4
0.1UF/16V
D4C47
1UF/10V
mba_c0003
D4C48
22UF/6.3V
mba_c0003
X7R
X5V

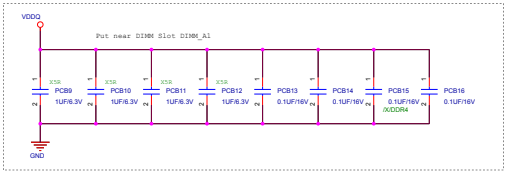

DIMM_B1B
DDR4_DIMM_288P
VPPDDR
VTT_DDR
VDDQ
VDDSPD
VREFCA
GND
D4_VREFCA_B
H_D4B_VREFCA
D4R7
1KOhm
1%
D4R8
1KOhm
1%
D4C14
0.1UF/16V
D4C44
0.1UF/16V
D4C45
/DDR4
0.1UF/16V
D4C46
4.7UF/6.3V
mba_c0003
D4C50
22UF/6.3V
mba_c0003
X7R
X5V

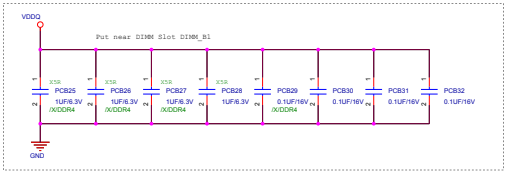

VDDSPD
D3FS01
1.6A/6V
D4R9
/DDR4
D4R10
/DDR4
0Ohm
mba_r0603
0Ohm
mba_r0603
VPPDDR
+3V_ATX
+VDDSPD option to +3V

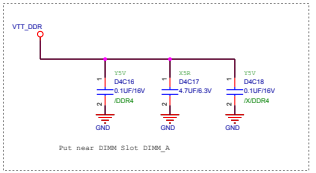
Rev 1.0 to +3V

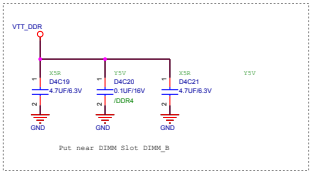

Layout to 0603

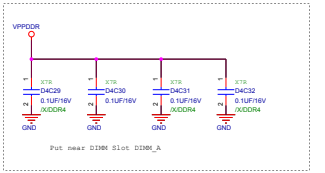

VDDQ
X5R
PCB1
22UF/6.3V
mbs_c0603
Layout
X5R
PCB2
22UF/6.3V
mbs_c0805
X5R
PCB3
22UF/6.3V
mbs_c0805
X5R
PCB4
22UF/6.3V
mbs_c0805
X5R
PCB5
22UF/6.3V
mbs_c0603
Layout
X5R
PCB6
22UF/6.3V
mbs_c0805
X5R
PCB7
22UF/6.3V
mbs_c0603
Layout
X5R
PCB8
22UF/6.3V
mbs_c0805
X5R
PCB45
22UF/6.3V
mbs_c0603
Layout
GND
DIMM 附近

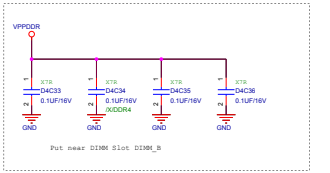

VDDQ
Put near DIMM Slot DIMM_A1
X5R
PCB9
1UF/6.3V
X5R
PCB10
1UF/6.3V
X5R
PCB11
1UF/6.3V
X5R
PCB12
1UF/6.3V
PCB13
0.1UF/16V
PCB14
0.1UF/16V
PCB15
0.1UF/16V
/XDDR4
PCB16
0.1UF/16V
GND


VDDQ
Put near DIMM Slot DIMM_B1
X5R
PCB25
1UF/6.3V
/XDDR4
X5R
PCB26
1UF/6.3V
/XDDR4
X5R
PCB27
1UF/6.3V
/XDDR4
X5R
PCB28
1UF/6.3V
PCB29
0.1UF/16V
/XDDR4
PCB30
0.1UF/16V
PCB31
0.1UF/16V
PCB32
0.1UF/16V
GND

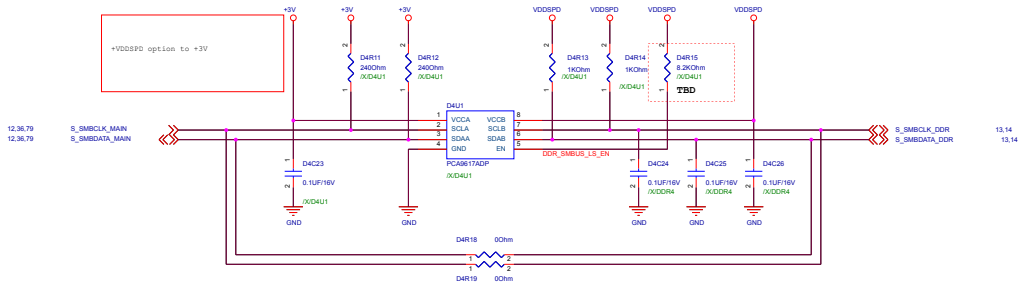

VTT_DDR
Y5V
D4C16
0.1UF/16V
/DDR4
X5R
D4C17
4.7UF/6.3V
Y5V
D4C18
0.1UF/16V
/XDDR4
GND
Put near DIMM Slot DIMM_A


VTT_DDR
X5R
D4C19
4.7UF/6.3V
Y5V
D4C20
0.1UF/16V
/DDR4
X5R
D4C21
4.7UF/6.3V
Y5V
GND
Put near DIMM Slot DIMM_B


VPPDDR
X7R
D4C29
0.1UF/16V
/XDDR4
X7R
D4C30
0.1UF/16V
X7R
D4C31
0.1UF/16V
/XDDR4
X7R
D4C32
0.1UF/16V
/XDDR4
GND
Put near DIMM Slot DIMM_A

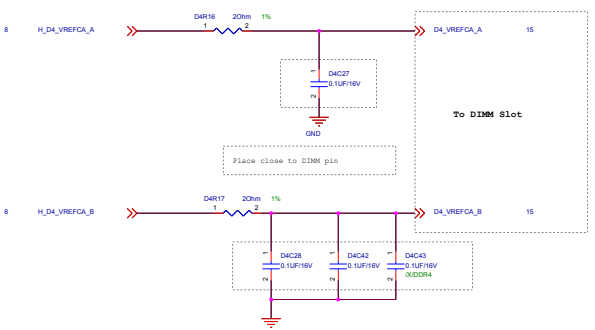

VPPDDR
X7R
D4C33
0.1UF/16V
X7R
D4C34
0.1UF/16V
/XDDR4
X7R
D4C35
0.1UF/16V
X7R
D4C36
0.1UF/16V
GND
Put near DIMM Slot DIMM_B

DRAM SMBUS From PCH (Thru Level Shift)



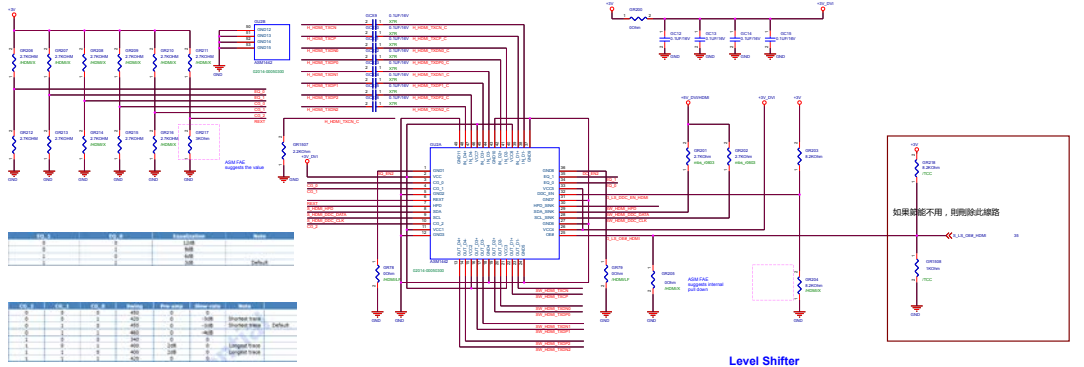
CPU DDR Vref

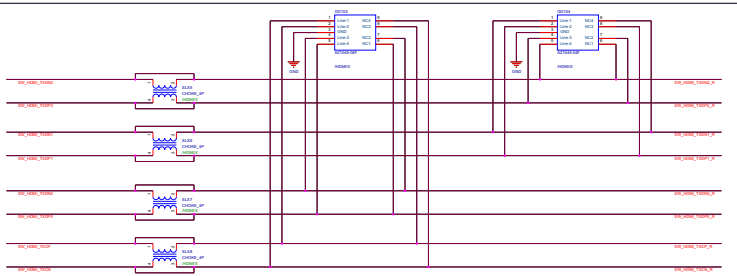
For CPU DDR Vref

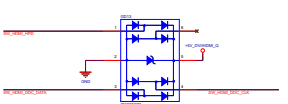


delete it
delete

delete this page for HDMI/DVI colay





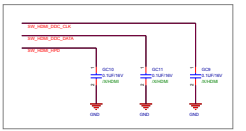


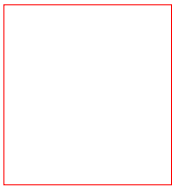
delete it
for DP

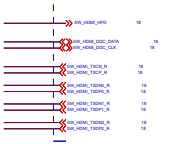
HDMI+SPDIF in one part,P/N:

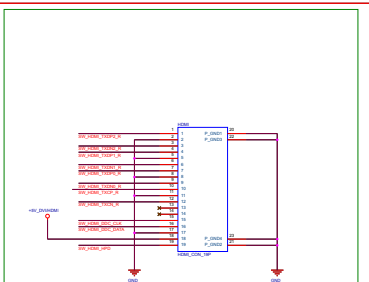
HDMI+SPDIF: 12G2404002201

if use two part,delete this block









delete it
for DP

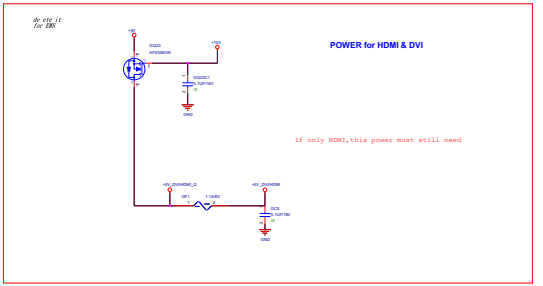
HDMI+SPDIF in two part,P/N:

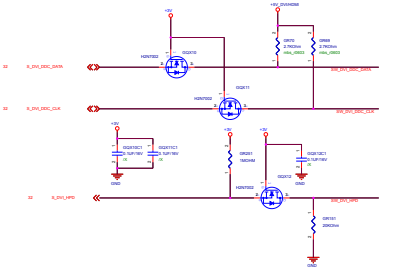
SPDIF: 12G2404003301

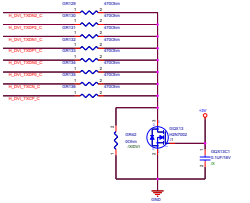
HDMI: 12022-00046900

if use one part,delete this block

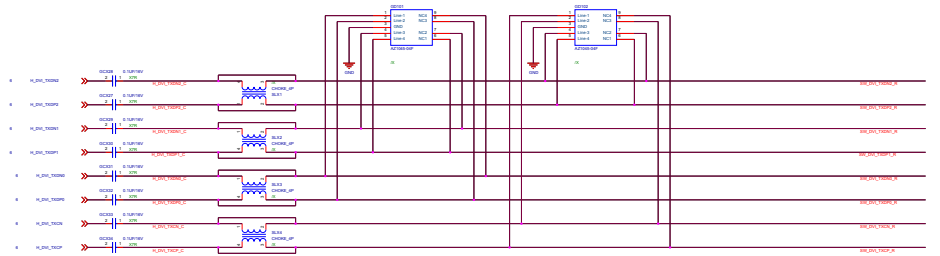
if use DP&HDMI port,remain this part

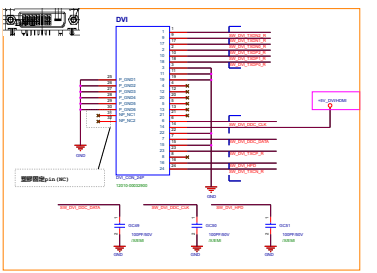


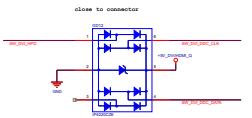


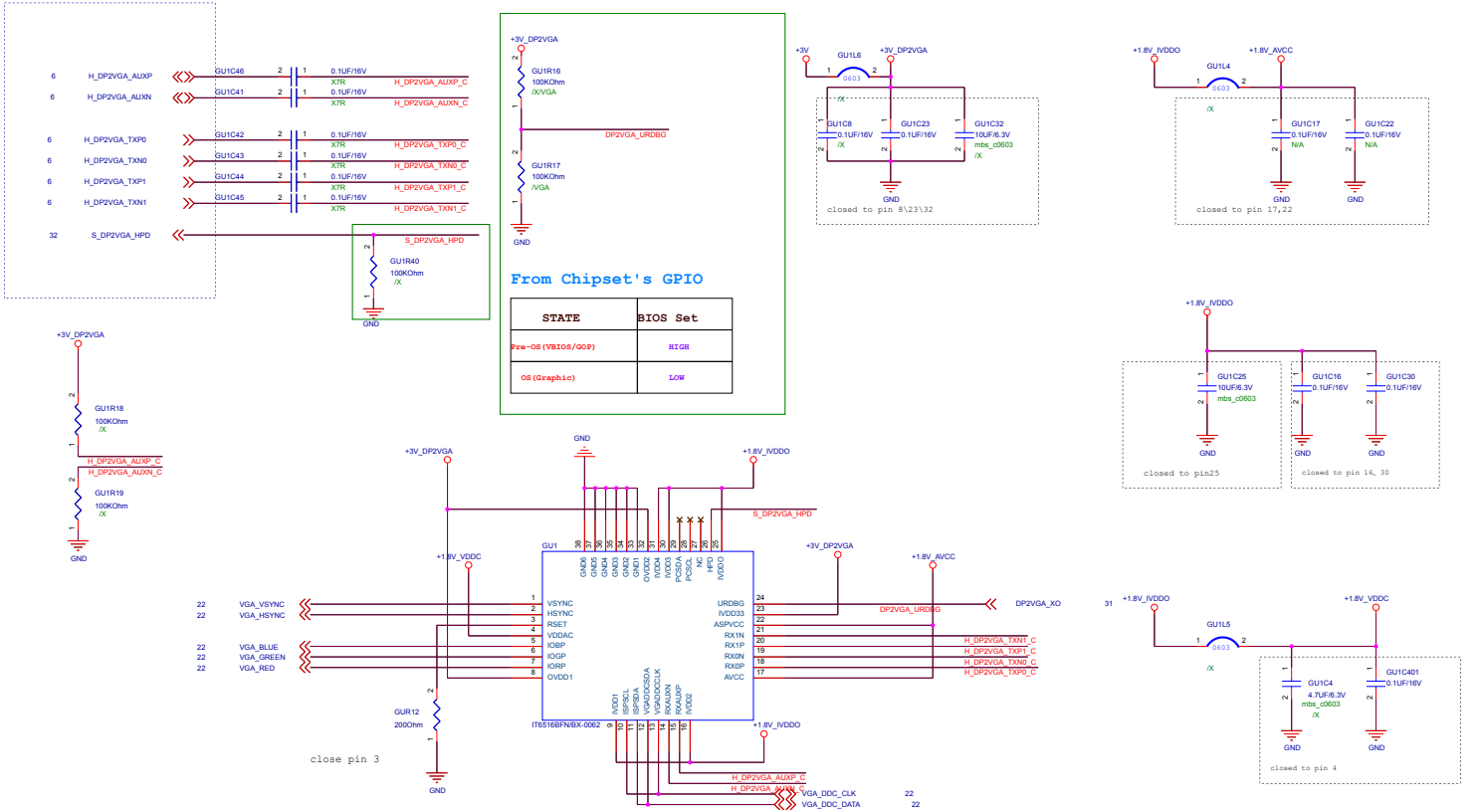


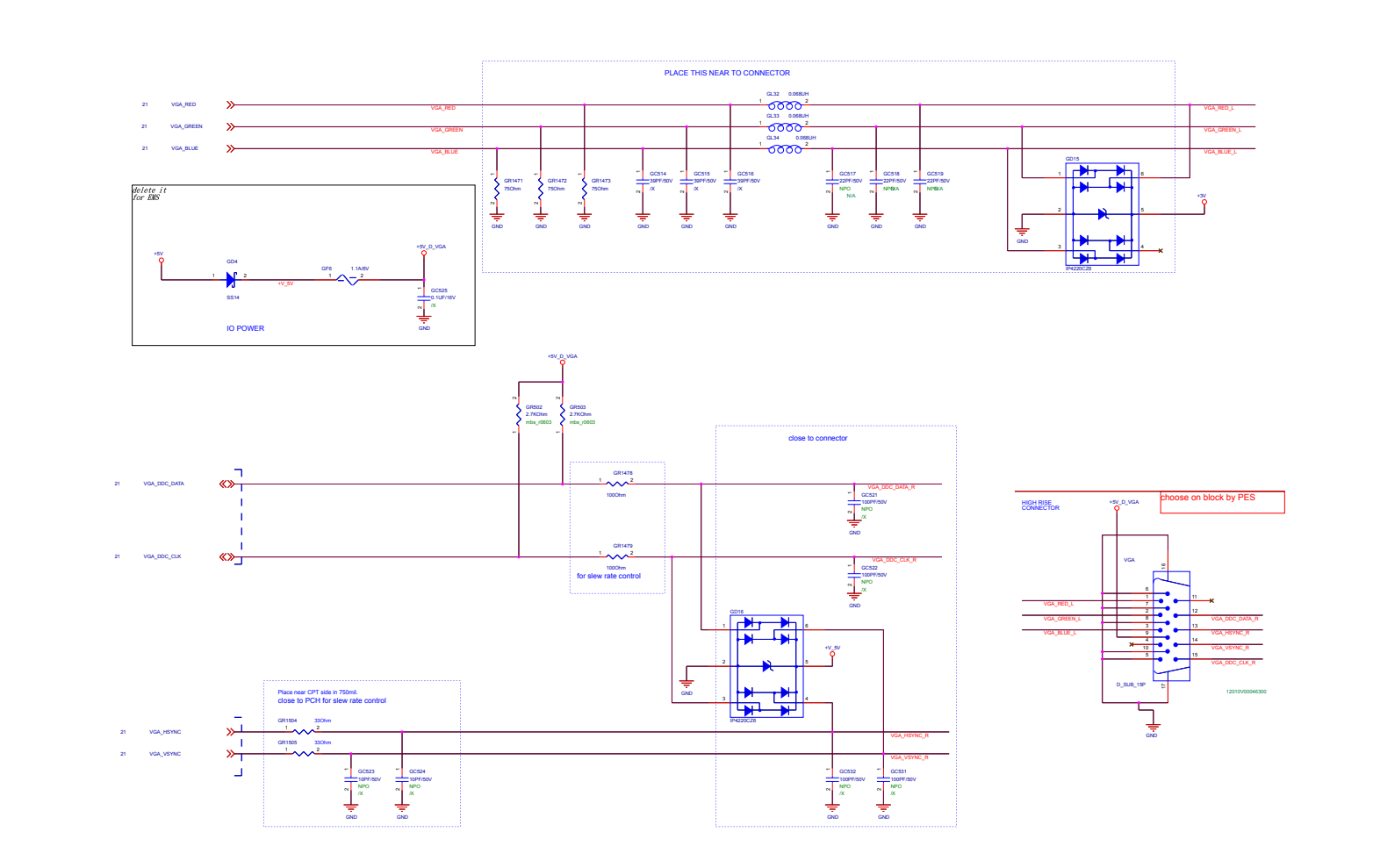
Passive/Active Devices				
Max Capacitance (Backdrive | Protection)	Schottky Diode	NA	pF	10	10
Resistor Value (+/- 5%)	R=0Ω	NA	Ω	0Ω	NA
ESD Protection	ESD	NA	NA	Optional	Optional
Max nFET Ron/Coss	NA	NA	10nF	3ohm/10pF	NA

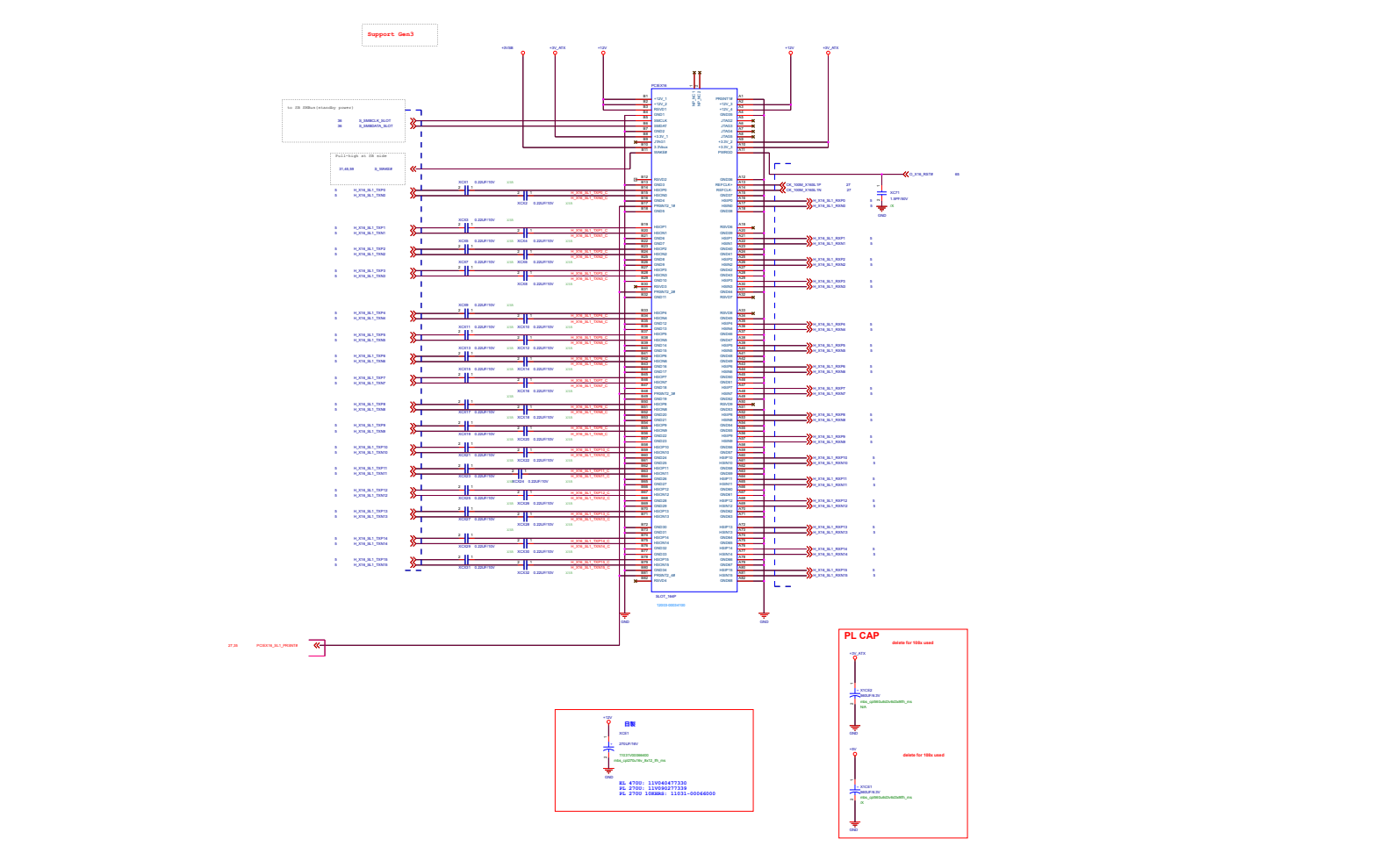


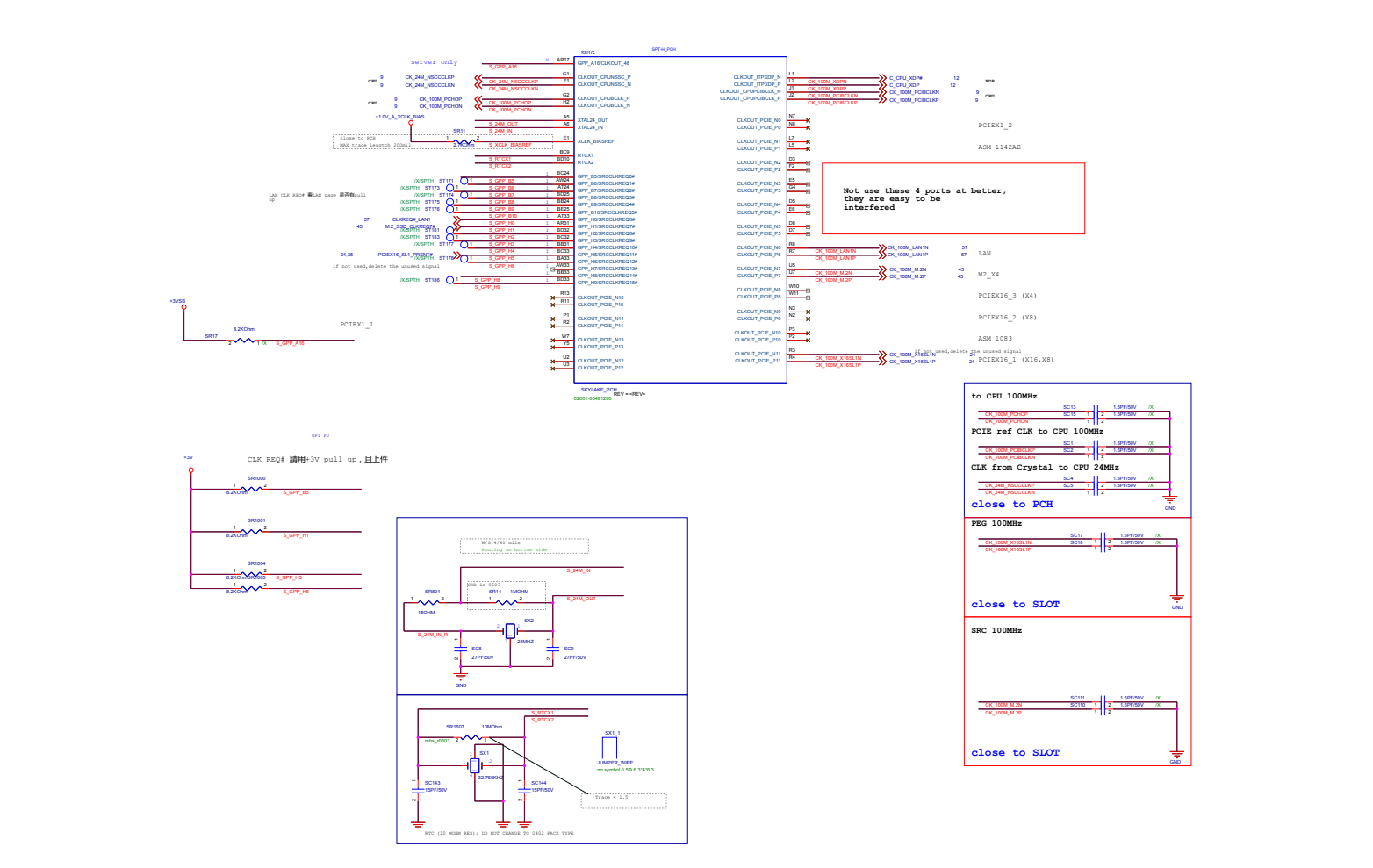


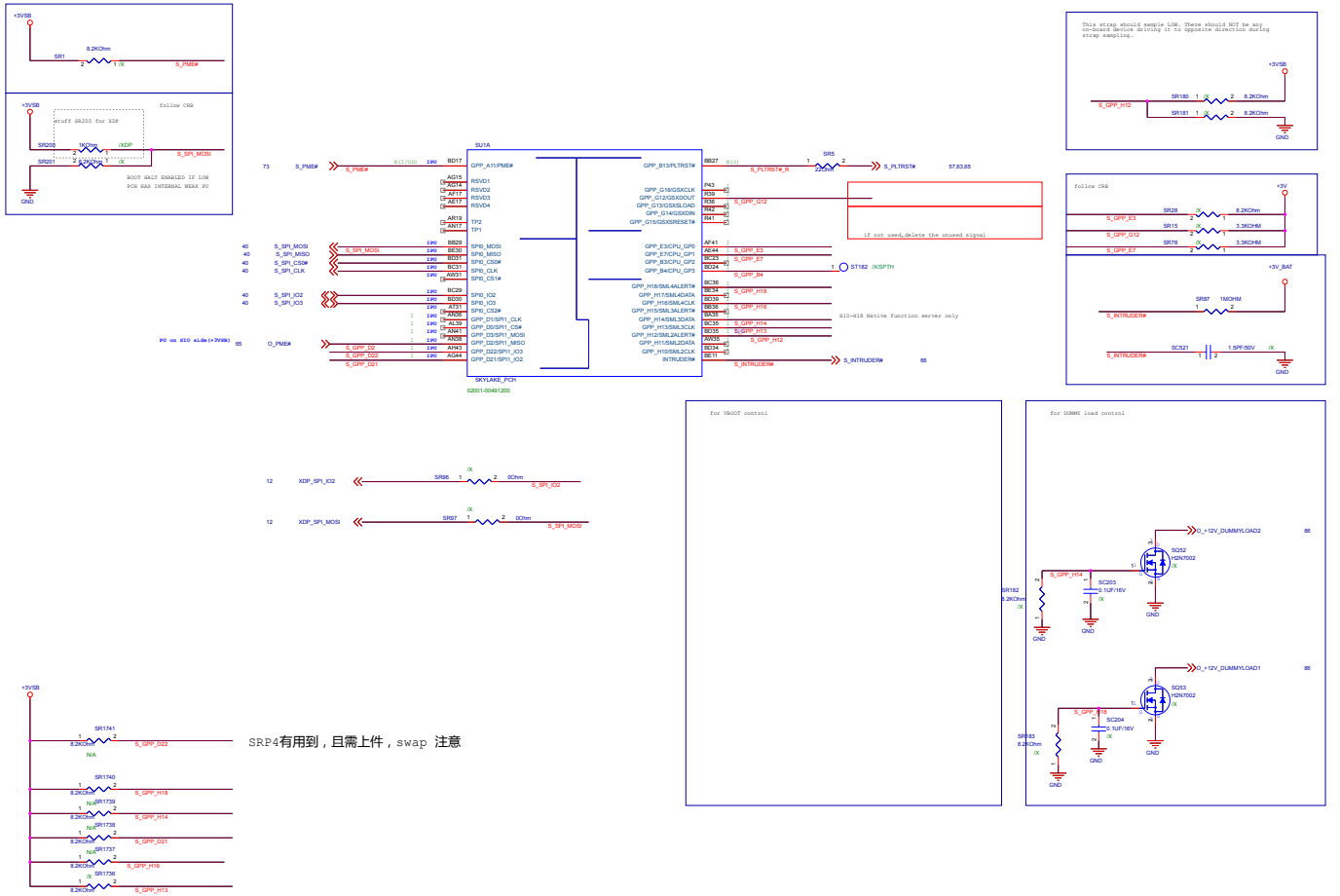



6 H_DP2VGA_AUXP
6 H_DP2VGA_AUXN
GU1C46 2 1 0.1UF/16V X7R H_DP2VGA_AUXP_C
GU1C41 2 1 0.1UF/16V X7R H_DP2VGA_AUXN_C
6 H_DP2VGA_TXP0
6 H_DP2VGA_TXN0
6 H_DP2VGA_TXP1
6 H_DP2VGA_TXN1
GU1C42 2 1 0.1UF/16V X7R H_DP2VGA_TXP0_C
GU1C43 2 1 0.1UF/16V X7R H_DP2VGA_TXN0_C
GU1C44 2 1 0.1UF/16V X7R H_DP2VGA_TXP1_C
GU1C45 2 1 0.1UF/16V X7R H_DP2VGA_TXN1_C
32 S_DP2VGA_HPD
S_DP2VGA_HPD
GU1R40 100KOhm /X
GND
+3V_DP2VGA
GU1R16 100KOhm /X/VGA
DP2VGA_URDBG
GU1R17 100KOhm /VGA
GND
From Chipset's GPIO
STATE | BIOS Set
Pre-OS(VBIOS/GOP) | HIGH
OS(Graphic) | LOW
+3V
GU1L6 0603 /X
+3V_DP2VGA
GU1C18 0.1UF/16V /X
GU1C23 0.1UF/16V
GU1C32 10UF/6.3V mbs_c0603 /X
GND
closed to pin 8\23\32
+1.8V_IVDDO
GU1L4 0603 /X
+1.8V_AVCC
GU1C17 0.1UF/16V N/A
GU1C22 0.1UF/16V N/A
GND
closed to pin 17,22
+3V_DP2VGA
GU1R18 100KOhm /X
H_DP2VGA_AUXP_C
H_DP2VGA_AUXN_C
GU1R19 100KOhm /X
GND
+1.8V_IVDDO
GU1C25 10UF/6.3V mbs_c0603
GU1C16 0.1UF/16V
GU1C30 0.1UF/16V
GND
closed to pin25
closed to pin 16, 30
GND
+3V_DP2VGA
+1.8V_IVDDO
S_DP2VGA_HPD
+1.8V_VDDC
GU1
GND5 GND6 GND4 GND3 GND2 GND1 OVDD2 IVDD4 IVDD3 PCSDA PCSCL NC HPD IVDD0
+3V_DP2VGA
+1.8V_AVCC
22 VGA_VSYNC
22 VGA_HSYNC
22 VGA_BLUE
22 VGA_GREEN
22 VGA_RED
VSYNC HSYNC RSET VDDAC IOBP IOGP IORP OVDD1
URDBG IVDD33 ASPVCC RX1N RX1P RX0N RX0P AVCC
DP2VGA_URDBG
DP2VGA_XO
H_DP2VGA_TXN1_C
H_DP2VGA_TXP1_C
H_DP2VGA_TXN0_C
H_DP2VGA_TXP0_C
GUR12 200Ohm
close pin 3
GND
IVDD1 ISPSCL ISPSDA VGADDCSDA VGADDCCLK RXAUXN RXAUXP IVDD2
IT6516BFN/BX-0062
+1.8V_IVDDO
H_DP2VGA_AUXP_C
H_DP2VGA_AUXN_C
VGA_DDC_CLK 22
VGA_DDC_DATA 22
31 +1.8V_IVDDO
GU1L5 0603 /X
+1.8V_VDDC
GU1C4 4.7UF/6.3V mbs_c0603 /X
GU1C401 0.1UF/16V
GND
closed to pin 4

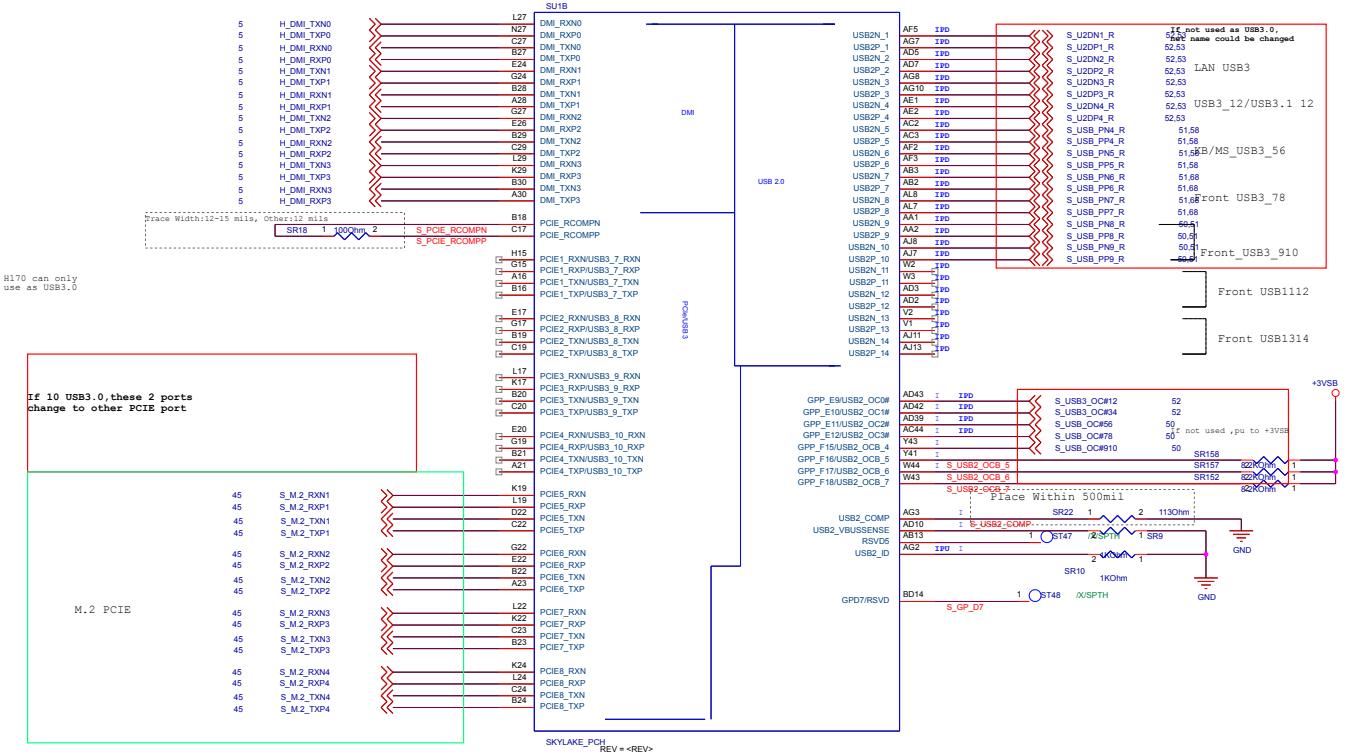

PLACE THIS NEAR TO CONNECTOR
21 VGA_RED
21 VGA_GREEN
21 VGA_BLUE
VGA_RED
VGA_GREEN
VGA_BLUE
GL32 0.068UH
GL33 0.068UH
GL34 0.068UH
VGA_RED_L
VGA_GREEN_L
VGA_BLUE_L
GR1471 75Ohm
GR1472 75Ohm
GR1473 75Ohm
GC514 39PF/50V /X
GC515 39PF/50V /X
GC516 39PF/50V /X
GC517 22PF/50V NPO N/A
GC518 22PF/50V NPO/A
GC519 22PF/50V NPO/A
GD15
IP4220CZ6
+3V
GND
delete it for EMS
+5V
GD4
SS14
+V_5V
GF6 1.1A/6V
+5V_D_VGA
GC525 0.1UF/16V /X
IO POWER
+5V_D_VGA
GR502 2.7KOhm mbs_r0603
GR503 2.7KOhm mbs_r0603
close to connector
21 VGA_DDC_DATA
21 VGA_DDC_CLK
GR1478 100Ohm
GR1479 100Ohm
for slew rate control
VGA_DDC_DATA_R
VGA_DDC_CLK_R
GC521 100PF/50V NPO /X
GC522 100PF/50V NPO /X
GD16
IP4220CZ6
+V_5V
Place near CPT side in 750mil.
close to PCH for slew rate control
21 VGA_HSYNC
21 VGA_VSYNC
GR1504 33Ohm
GR1505 33Ohm
GC523 10PF/50V NPO /X
GC524 10PF/50V NPO /X
VGA_HSYNC_R
VGA_VSYNC_R
GC532 100PF/50V NPO /X
GC531 100PF/50V NPO /X
HIGH RISE CONNECTOR
+5V_D_VGA
choose on block by PES
VGA
D_SUB_15P
VGA_RED_L
VGA_GREEN_L
VGA_BLUE_L
VGA_DDC_DATA_R
VGA_HSYNC_R
VGA_VSYNC_R
VGA_DDC_CLK_R
12010V00046309

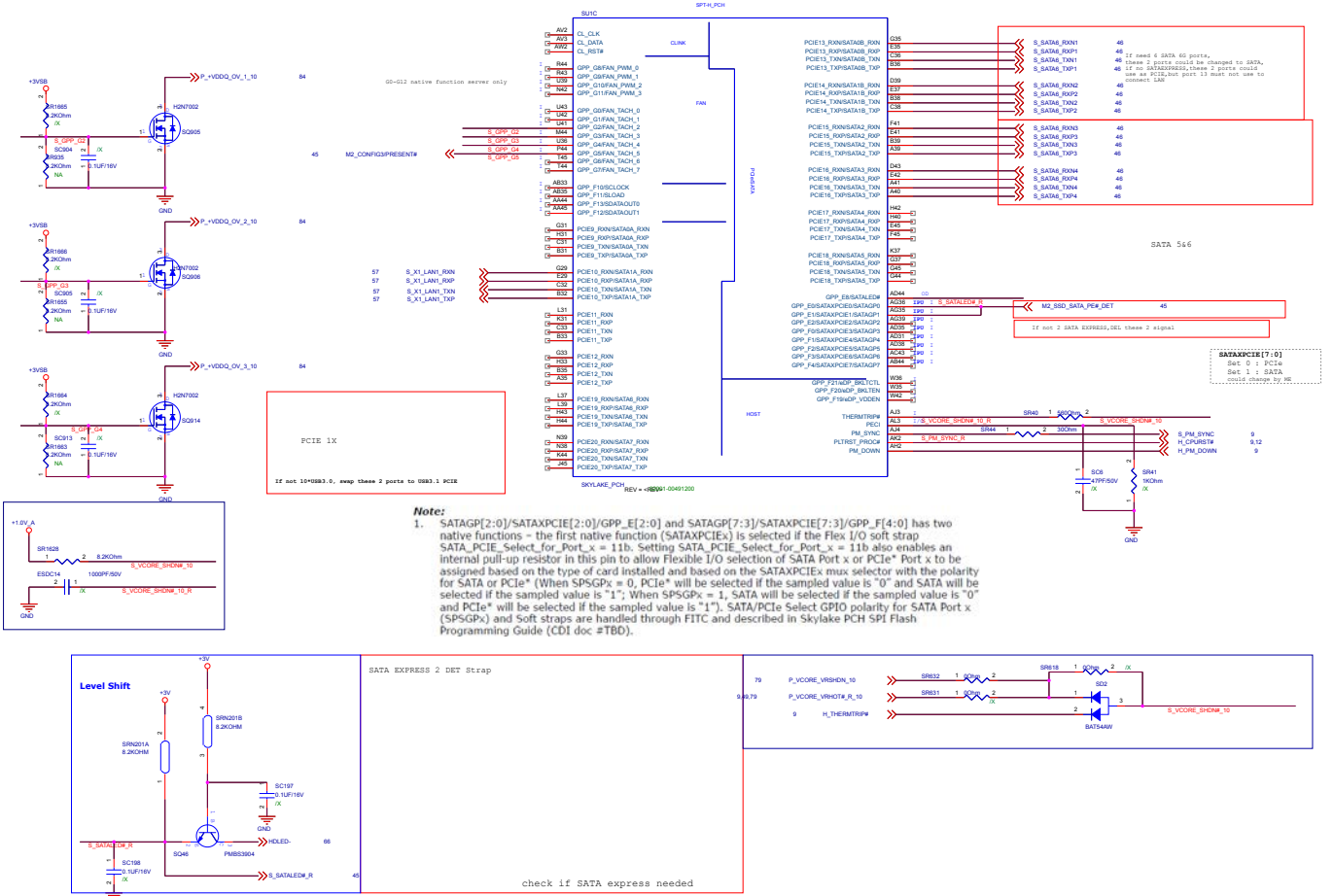

Support Gen3
PCIE3C16
SLOT_164P
PL CAP
delete for 100x used
delete for 100x used
EL 4700: 11V040477330
PL 2700: 11V090277330
PL 2700 100X&U: 11031-00060000


server only
SPT-H_PCH
SU1G
GPP_A16/CLKOUT_48
CK_24M_NSCCLKP
CK_24M_NSCCLKN
CK_100M_PCHOP
CK_100M_PCHON
+1.0V_A_XCLK_BIAS
SR11
close to PCH
max trace length 200mil
S_XCLK_BIASREF
RTCX1
RTCX2
LAN CLK REQ# 看LAN page 是否有pull up
CLKREQ#_LAN1
M.2_SSD_CLKREQ#
PCIEX16_SL1_PRSNT#
if not used,delete the unused signal
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKOUT_CPUPCIBCLK_N
CLKOUT_CPUPCIBCLK_P
C_CPU_XDP#
C_CPU_XDP
CK_100M_XDP#
CK_100M_XDP
CK_100M_PCIBCLKN
CK_100M_PCIBCLKP
PCIEX1_2
ASM 1142AE
Not use these 4 ports at better, they are easy to be interfered
CK_100M_LAN1N
CK_100M_LAN1P
LAN
CK_100M_M.2N
CK_100M_M.2P
M2_X4
PCIEX16_3 (X4)
PCIEX16_2 (X8)
ASM 1083
CK_100M_X16SL1N
CK_100M_X16SL1P
PCIEX16_1 (X16,X8)
+3VSB
8.2KOhm
SR17
PCIEX1_1
GPI PU
CLK REQ# 請用+3V pull up，且上件
SR1000
SR1001
SR1004
S_GPP_B5
S_GPP_H1
S_GPP_H5
S_GPP_H6
to CPU 100MHz
PCIE ref CLK to CPU 100MHz
CLK from Crystal to CPU 24MHz
close to PCH
PEG 100MHz
close to SLOT
SRC 100MHz
close to SLOT
SR8001
SR14
SX2
24MHZ
SC8
SC9
27PF/50V
S_24M_IN
S_24M_OUT
SR1607
10MOhm
SX1
32.768KHZ
SC143
SC144
15PF/50V
SX1_1
JUMPER_WIRE
RTC (10 MOHM RES): DO NOT CHANGE TO 0402 PACK_TYPE



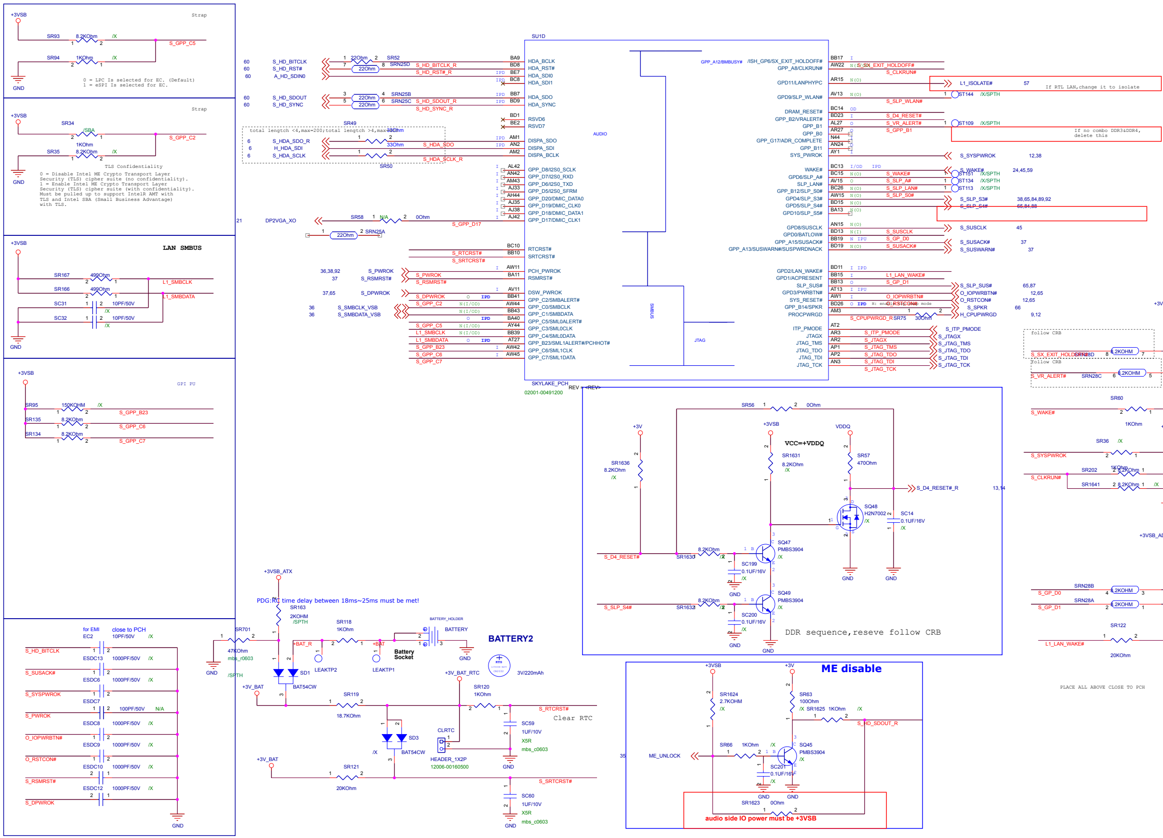
SRP4有用到，且需上件，swap 注意


SU1B
DMI_RXN0
DMI_RXP0
DMI_TXN0
DMI_TXP0
DMI_RXN1
DMI_RXP1
DMI_TXN1
DMI_TXP1
DMI_RXN2
DMI_RXP2
DMI_TXN2
DMI_TXP2
DMI_RXN3
DMI_RXP3
DMI_TXN3
DMI_TXP3
DMI
PCIe/USB3
USB 2.0
H_DMI_TXN0
H_DMI_TXP0
H_DMI_RXN0
H_DMI_RXP0
H_DMI_TXN1
H_DMI_TXP1
H_DMI_RXN1
H_DMI_RXP1
H_DMI_TXN2
H_DMI_TXP2
H_DMI_RXN2
H_DMI_RXP2
H_DMI_TXN3
H_DMI_RXP3
Trace Width:12-15 mils, Other:12 mils
SR18
1000hm
S_PCIE_RCOMPN
S_PCIE_RCOMPP
PCIE_RCOMPN
PCIE_RCOMPP
PCIE1_RXN/USB3_7_RXN
PCIE1_RXP/USB3_7_RXP
PCIE1_TXN/USB3_7_TXN
PCIE1_TXP/USB3_7_TXP
PCIE2_RXN/USB3_8_RXN
PCIE2_RXP/USB3_8_RXP
PCIE2_TXN/USB3_8_TXN
PCIE2_TXP/USB3_8_TXP
PCIE3_RXN/USB3_9_RXN
PCIE3_RXP/USB3_9_RXP
PCIE3_TXN/USB3_9_TXN
PCIE3_TXP/USB3_9_TXP
PCIE4_RXN/USB3_10_RXN
PCIE4_RXP/USB3_10_RXP
PCIE4_TXN/USB3_10_TXN
PCIE4_TXP/USB3_10_TXP
PCIE5_RXN
PCIE5_RXP
PCIE5_TXN
PCIE5_TXP
PCIE6_RXN
PCIE6_RXP
PCIE6_TXN
PCIE6_TXP
PCIE7_RXN
PCIE7_RXP
PCIE7_TXN
PCIE7_TXP
PCIE8_RXN
PCIE8_RXP
PCIE8_TXN
PCIE8_TXP
USB2N_1
USB2P_1
USB2N_2
USB2P_2
USB2N_3
USB2P_3
USB2N_4
USB2P_4
USB2N_5
USB2P_5
USB2N_6
USB2P_6
USB2N_7
USB2P_7
USB2N_8
USB2P_8
USB2N_9
USB2P_9
USB2N_10
USB2P_10
USB2N_11
USB2P_11
USB2N_12
USB2P_12
USB2N_13
USB2P_13
USB2N_14
USB2P_14
S_U2DN1_R
S_U2DP1_R
S_U2DN2_R
S_U2DP2_R
S_U2DN3_R
S_U2DP3_R
S_U2DN4_R
S_U2DP4_R
S_USB_PN4_R
S_USB_PP4_R
S_USB_PN5_R
S_USB_PP5_R
S_USB_PN6_R
S_USB_PP6_R
S_USB_PN7_R
S_USB_PP7_R
S_USB_PN8_R
S_USB_PP8_R
S_USB_PN9_R
S_USB_PP9_R
If not used as USB3.0, port name could be changed
LAN USB3
USB3_12/USB3.1 12
USB/MS_USB3_56
Front USB3_78
Front_USB3_910
Front USB1112
Front USB1314
H170 can only use as USB3.0
If 10 USB3.0,these 2 ports change to other PCIE port
M.2 PCIE
S_M.2_RXN1
S_M.2_RXP1
S_M.2_TXN1
S_M.2_TXP1
S_M.2_RXN2
S_M.2_RXP2
S_M.2_TXN2
S_M.2_TXP2
S_M.2_RXN3
S_M.2_RXP3
S_M.2_TXN3
S_M.2_TXP3
S_M.2_RXN4
S_M.2_RXP4
S_M.2_TXN4
S_M.2_TXP4
GPP_E9/USB2_OC0#
GPP_E10/USB2_OC1#
GPP_E11/USB2_OC2#
GPP_E12/USB2_OC3#
GPP_F15/USB2_OCB_4
GPP_F16/USB2_OCB_5
GPP_F17/USB2_OCB_6
GPP_F18/USB2_OCB_7
S_USB3_OC#12
S_USB3_OC#34
S_USB_OC#56
S_USB_OC#78
S_USB_OC#910
If not used ,pu to +3VSB
SR158
SR157
SR152
82KOhm
+3VSB
S_USB2_OCB_5
S_USB2_OCB_6
S_USB2_OCB_7
Place Within 500mil
USB2_COMP
USB2_VBUSSENSE
RSVD5
USB2_ID
S_USB2_COMP
SR22
113Ohm
ST47
/X/SPTH
SR9
GND
SR10
1KOhm
GPD7/RSVD
ST48
S_GP_D7
SKYLAKE_PCH
REV = <REV>
02001-00491200

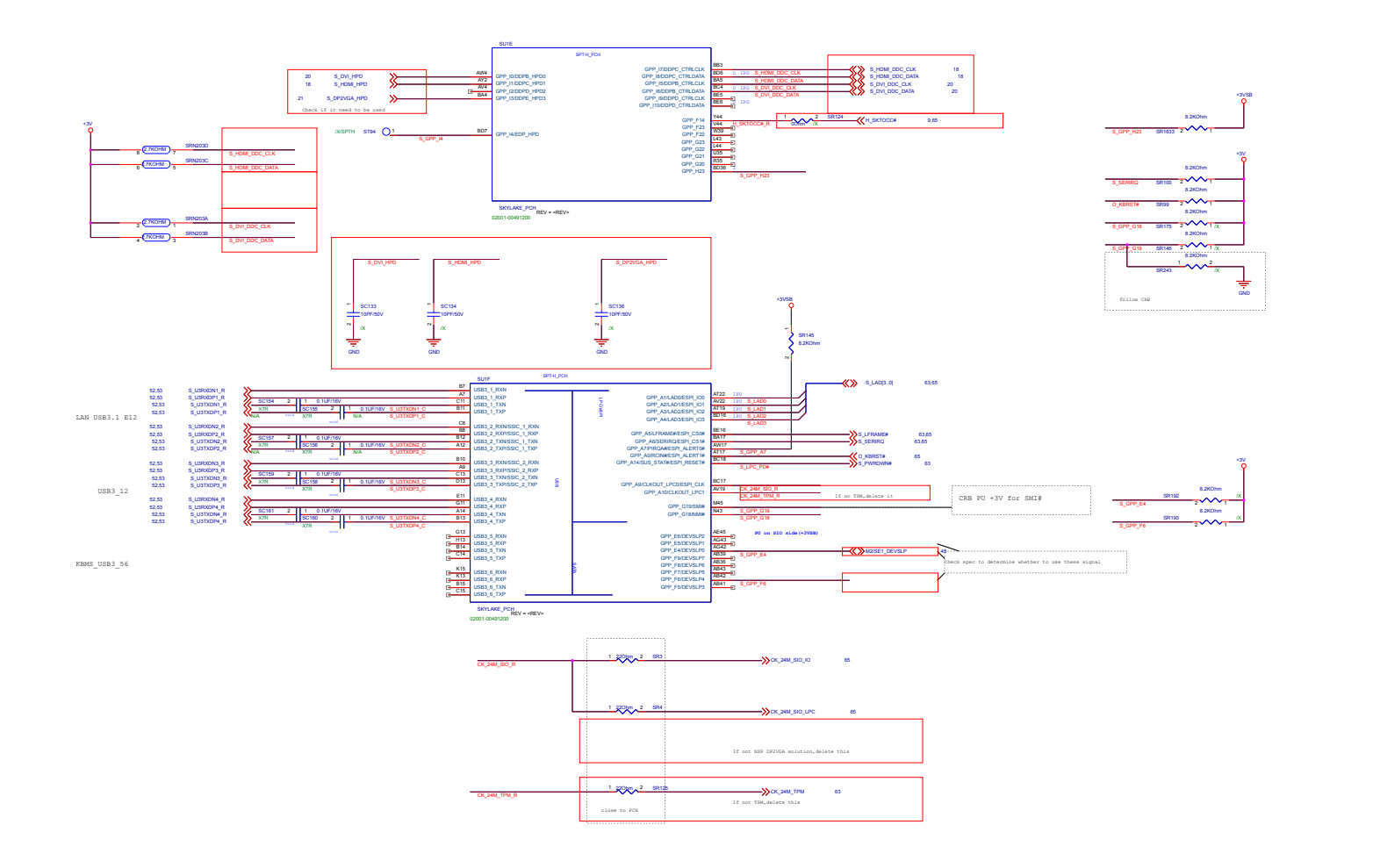


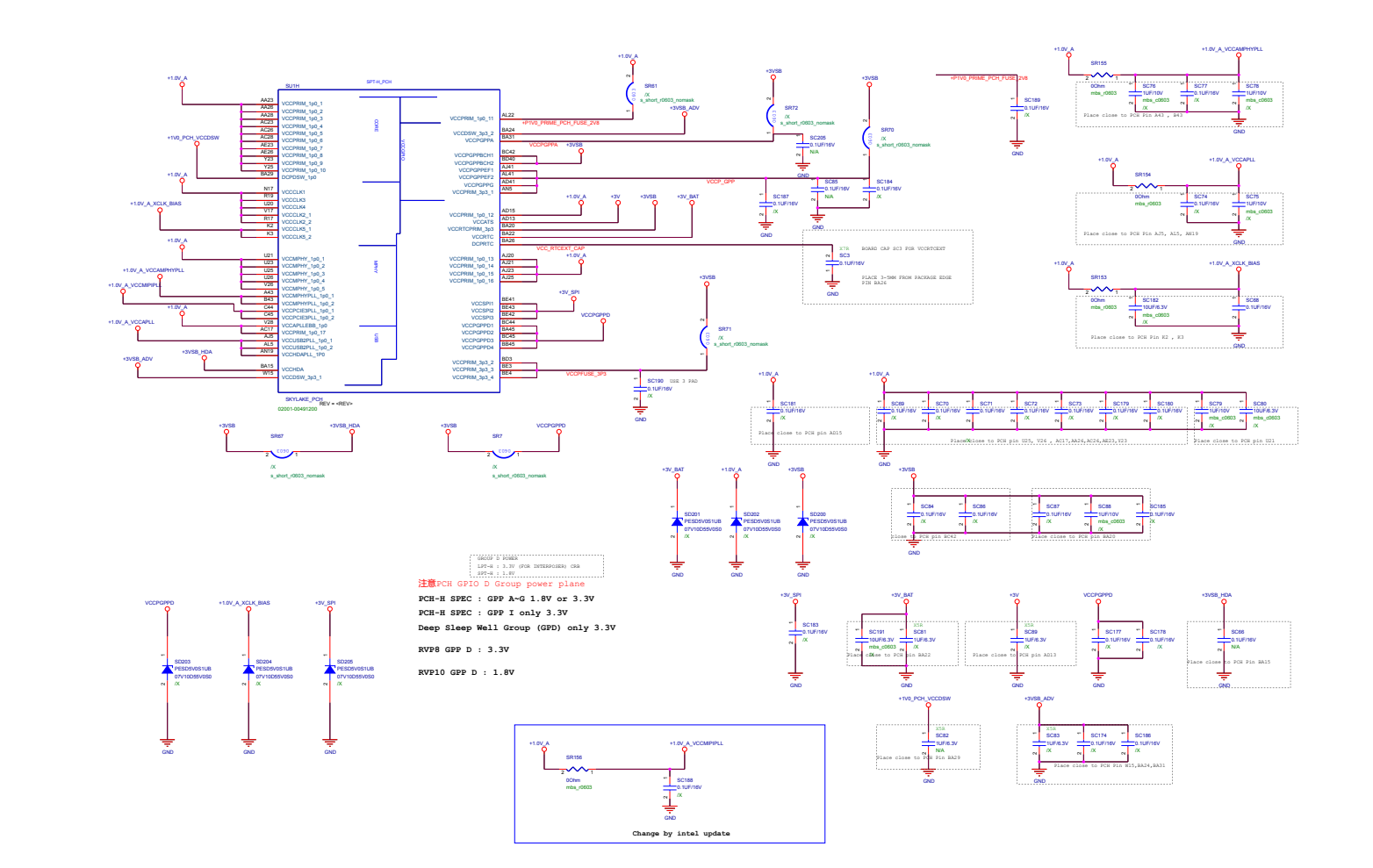
Note:

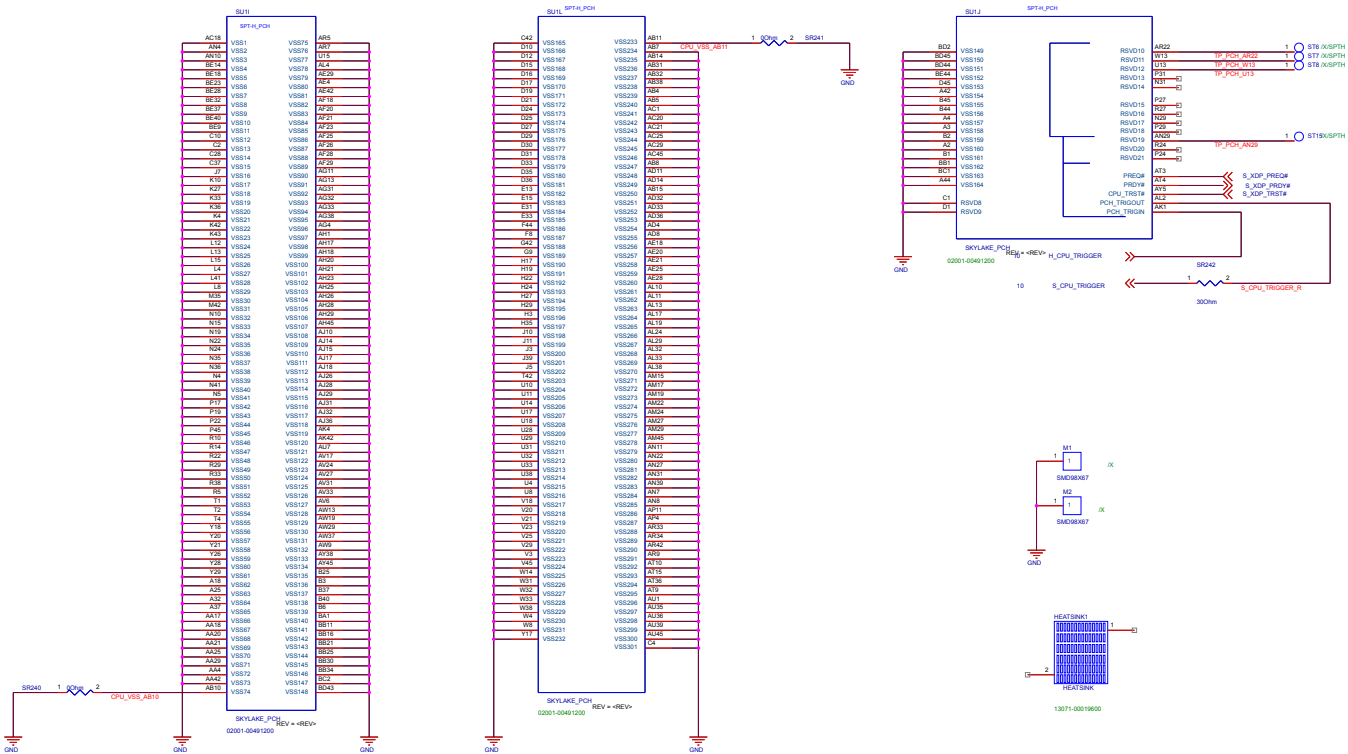
1. SATAGP[2:0]/SATAXPCIE[2:0]/GPP_E[2:0] and SATAGP[7:3]/SATAXPCIE[7:3]/GPP_F[4:0] has two native functions - the first native function (SATAXPCIEx) is selected if the Flex I/O soft strap SATA_PCIE_Select_for_Port_x = 11b. Setting SATA_PCIE_Select_for_Port_x = 11b also enables an internal pull-up resistor in this pin to allow Flexible I/O selection of SATA Port x or PCIe* Port x to be assigned based on the type of card installed and based on the SATAXPCIEx mux selector with the polarity for SATA or PCIe* (When SPSGPx = 0, PCIe* will be selected if the sampled value is "0" and SATA will be selected if the sampled value is "1"; When SPSGPx = 1, SATA will be selected if the sampled value is "0" and PCIe* will be selected if the sampled value is "1"). SATA/PCIe Select GPIO polarity for SATA Port x (SPSGPx) and Soft straps are handled through FITC and described in Skylake PCH SPI Flash Programming Guide (CDI doc #TBD).

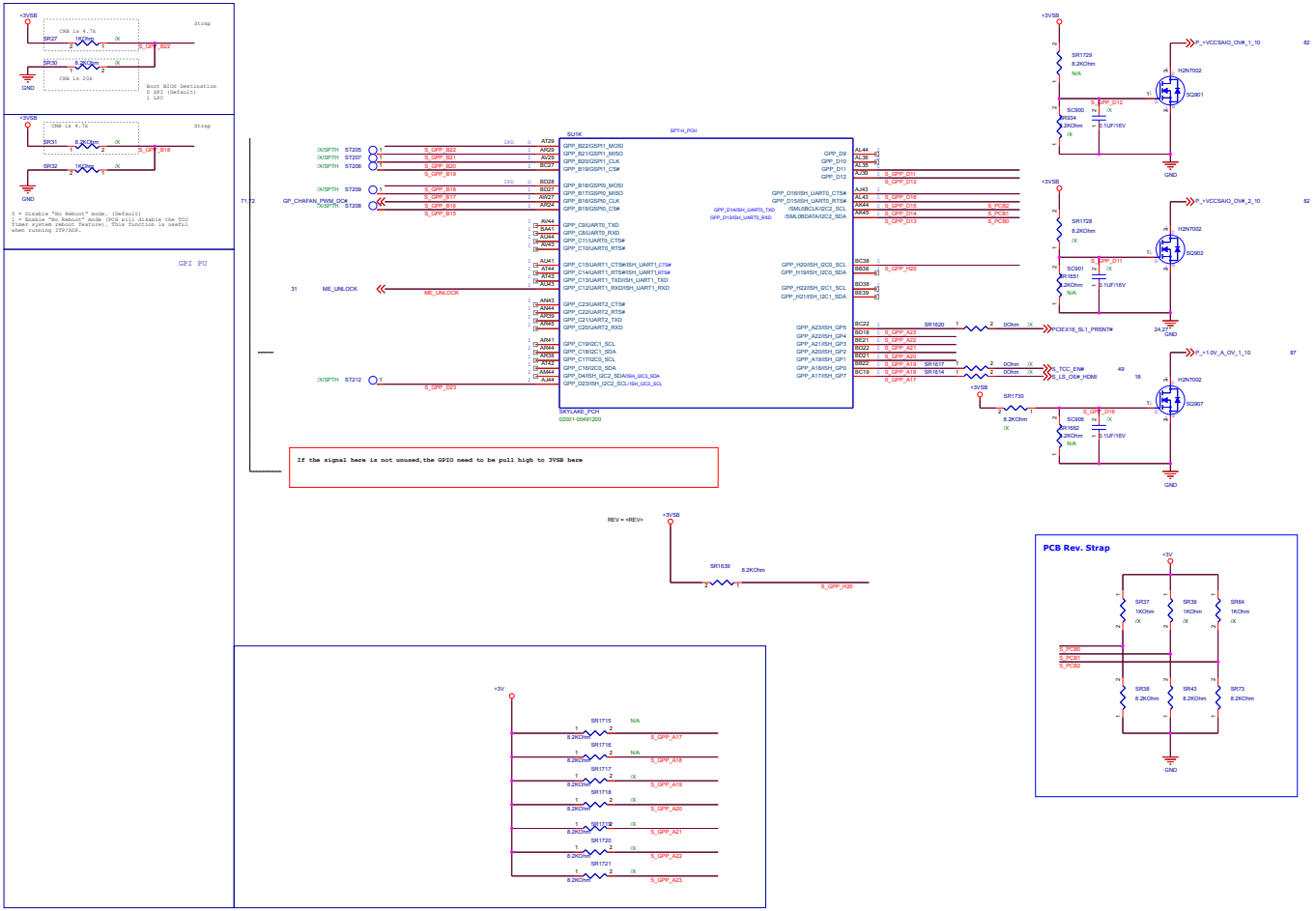


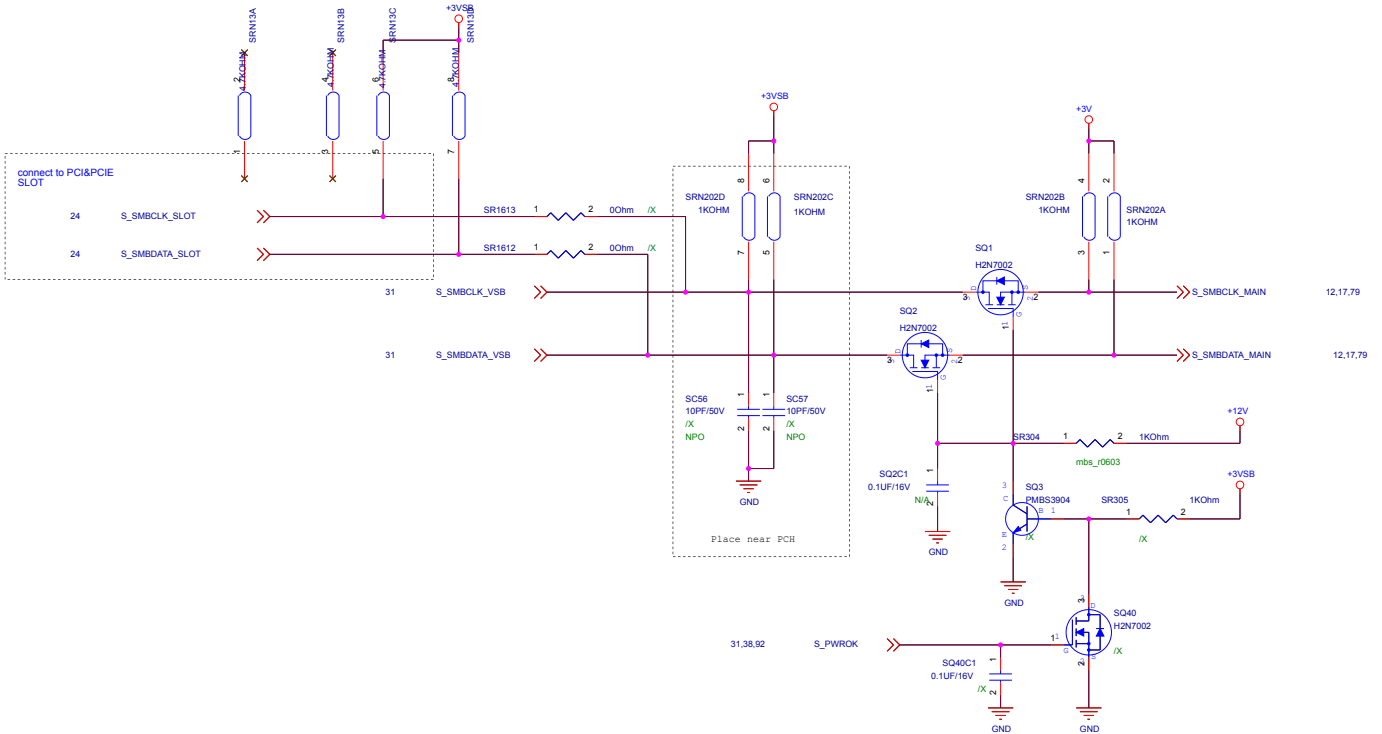
Strap
+3VSB
SR93 8.2KOhm /X
SR94 1KOhm /X
S_GPP_C5
GND
0 = LPC Is selected for EC. (Default)
1 = eSPI Is selected for EC.
SR34 /SBA
SR35 8.2KOhm /X
S_GPP_C2
TLS Confidentiality
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).
Must be pulled up to support IntelR AMT with TLS and Intel SBA (Small Business Advantage) with TLS.
LAN SMBUS
SR167 499Ohm
SR166 499Ohm
SC31 10PF/50V /X
SC32 10PF/50V /X
L1_SMBCLK
L1_SMBDATA
GPI PU
SR95 150KOHM /X
SR135 8.2KOhm
SR134 8.2KOhm
S_GPP_B23
S_GPP_C6
S_GPP_C7
for EMI
close to PCH
EC2 10PF/50V /X
S_HD_BITCLK
ESDC13 1000PF/50V /X
S_SUSACK#
ESDC6 1000PF/50V /X
S_SYSPWROK
ESDC7 100PF/50V N/A
S_PWROK
ESDC8 1000PF/50V /X
O_IOPWRBTN#
ESDC9 1000PF/50V /X
O_RSTCON#
ESDC10 1000PF/50V /X
S_RSMRST#
ESDC12 1000PF/50V /X
S_DPWROK
SU1D
S_HD_BITCLK
S_HD_RST#
A_HD_SDIN0
S_HD_SDOUT
S_HD_SYNC
SR52 22Ohm
SRN25D 22Ohm
SRN25B 22Ohm
SRN25C 22Ohm
S_HD_BITCLK_R
S_HD_RST#_R
S_HD_SDOUT_R
S_HD_SYNC_R
total length <4,max=200;total length >4,max=33Ohm
SR49 33Ohm
SR50
S_HDA_SDO_R
H_HDA_SDI
S_HDA_SCLK
S_HDA_SDO
S_HDA_SCLK_R
HDA_BCLK
HDA_RST#
HDA_SDI0
HDA_SDI1
HDA_SDO
HDA_SYNC
RSVD6
RSVD7
DISPA_SDO
DISPA_SDI
DISPA_BCLK
AUDIO
GPP_D8/I2S0_SCLK
GPP_D7/I2S0_RXD
GPP_D6/I2S0_TXD
GPP_D5/I2S0_SFRM
GPP_D20/DMIC_DATA0
GPP_D19/DMIC_CLK0
GPP_D18/DMIC_DATA1
GPP_D17/DMIC_CLK1
DP2VGA_XO
SR58 N/A 0Ohm
S_GPP_D17
SRN25A 22Ohm
RTCRST#
SRTCRST#
S_RTCRST#
S_SRTCRST#
PCH_PWROK
RSMRST#
DSW_PWROK
S_PWROK
S_RSMRST#
S_DPWROK
S_SMBCLK_VSB
S_SMBDATA_VSB
GPP_C2/SMBALERT#
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C5/SML0ALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_B23/SML1ALERT#/PCHHOT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
SMBUS
JTAG
SKYLAKE_PCH
02001-00491200
REV = <REV>
GPP_A12/BMBUSY#
ISH_GP6/SX_EXIT_HOLDOFF#
GPP_A8/CLKRUN#
GPD11/LANPHYPC
GPD9/SLP_WLAN#
DRAM_RESET#
GPP_B2/VRALERT#
GPP_B1
GPP_B0
GPP_G17/ADR_COMPLETE
GPP_B11
SYS_PWROK
WAKE#
GPD6/SLP_A#
SLP_LAN#
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
GPD8/SUSCLK
GPD0/BATLOW#
GPP_A15/SUSACK#
GPP_A13/SUSWARN#/SUSPWRDNACK
GPD2/LAN_WAKE#
GPD1/ACPRESENT
SLP_SUS#
GPD3/PWRBTN#
SYS_RESET#
GPP_B14/SPKR
PROCPWRGD
ITP_PMODE
JTAGX
JTAG_TMS
JTAG_TDO
JTAG_TDI
JTAG_TCK
S_SX_EXIT_HOLDOFF#
S_CLKRUN#
L1_ISOLATE#
If RTL LAN,change it to isolate
S_SLP_WLAN#
S_D4_RESET#
S_VR_ALERT#
S_GPP_B1
If no combo DDR3&DDR4, delete this
S_SYSPWROK
S_WAKE#
S_SLP_A#
S_SLP_LAN#
S_SLP_S0#
S_SLP_S3#
S_SLP_S4#
S_SUSCLK
S_GP_D0
S_SUSACK#
S_SUSWARN#
L1_LAN_WAKE#
S_GP_D1
S_SLP_SUS#
O_IOPWRBTN#
O_RSTCON#
S_SPKR
H_CPUPWRGD
S_CPUPWRGD_R
SR75 30Ohm
S_ITP_PMODE
S_JTAGX
S_JTAG_TMS
S_JTAG_TDO
S_JTAG_TDI
S_JTAG_TCK
follow CRB
SRN28D 2KOHM
SRN28C 2KOHM
SR60 1KOhm
SR36 /X
SR202 1KOhm
SR1641 8.2KOhm /X
S_SYSPWROK
S_CLKRUN#
+3VSB_ADV
SRN28B 2KOHM
SRN28A 2KOHM
S_GP_D0
S_GP_D1
SR122 20KOhm
L1_LAN_WAKE#
PLACE ALL ABOVE CLOSE TO PCH
SR56 0Ohm
VCC=+VDDQ
VDDQ
SR1636 8.2KOhm /X
SR1631 8.2KOhm /X
SR57 470Ohm
S_D4_RESET#_R
SQ48 H2N7002 /X
SC14 0.1UF/16V /X
SR1630 8.2KOhm
SQ47 PMBS3904 /X
SC199 0.1UF/16V /X
SR1632 8.2KOhm
SQ49 PMBS3904 /X
SC200 0.1UF/16V /X
S_SLP_S4#
DDR sequence,reseve follow CRB
+3VSB_ATX
PDG:RC time delay between 18ms~25ms must be met!
SR163 2KOHM /SPTH
SR701 47KOhm mbs_r0603 /SPTH
SD1 BAT54CW
SR118 1KOhm
+BAT_R
+BAT
LEAKTP2
LEAKTP1
Battery Socket
BATTERY_HOLDER
BATTERY
BATTERY2
3V/220mAh
+3V_BAT
+3V_BAT_RTC
SR119 18.7KOhm
SR120 1KOhm
SD3 BAT54CW
CLRTC
HEADER_1X2P
12006-00160500
SC59 1UF/10V X5R mbs_c0603
Clear RTC
SR121 20KOhm
SC60 1UF/10V X5R mbs_c0603
ME disable
SR1624 2.7KOHM /X
SR63 100Ohm
SR1625 1KOhm /X
S_HD_SDOUT_R
SR66 1KOhm /X
SQ45 PMBS3904 /X
SC201 0.1UF/16V /X
ME_UNLOCK
SR1623 0Ohm
audio side IO power must be +3VSB


SU1E
SPT-H_PCH
S_DVI_HPD
S_HDMI_HPD
S_DP2VGA_HPD
Check if it need to be used
GPP_I0/DDPB_HPD0
GPP_I1/DDPC_HPD1
GPP_I2/DDPD_HPD2
GPP_I3/DDPE_HPD3
GPP_I7/DDPC_CTRLCLK
GPP_I6/DDPC_CTRLDATA
GPP_I5/DDPB_CTRLCLK
GPP_I8/DDPB_CTRLDATA
GPP_I9/DDPD_CTRLCLK
GPP_I10/DDPD_CTRLDATA
S_HDMI_DDC_CLK
S_HDMI_DDC_DATA
S_DVI_DDC_CLK
S_DVI_DDC_DATA
H_SKTOCC#
SR124
9.65
+3V
2.7KOHM
SRN203D
SRN203C
SRN203A
SRN203B
S_HDMI_DDC_CLK
S_HDMI_DDC_DATA
S_DVI_DDC_CLK
S_DVI_DDC_DATA
/XSPTH
ST94
S_GPP_I4
GPP_I4/EDP_HPD
SKYLAKE_PCH
REV = <REV>
02001-00491200
GPP_F14
GPP_F23
GPP_F22
GPP_G23
GPP_G22
GPP_G21
GPP_G20
GPP_H23
S_GPP_H23
+3VSB
8.2KOhm
SR1633
S_SERIRQ
SR100
O_KBRST#
SR99
S_GPP_G18
SR175
S_GPP_G19
SR146
SR243
follow CRB
GND
S_DVI_HPD
S_HDMI_HPD
S_DP2VGA_HPD
SC133
SC134
SC136
10PF/50V
LAN USB3.1 E12
USB3_12
KBMS_USB3_56
SU1F
USB3_1_RXN
USB3_1_RXP
USB3_1_TXN
USB3_1_TXP
USB3_2_RXN/SSIC_1_RXN
USB3_2_RXP/SSIC_1_RXP
USB3_2_TXN/SSIC_1_TXN
USB3_2_TXP/SSIC_1_TXP
USB3_3_RXN/SSIC_2_RXN
USB3_3_RXP/SSIC_2_RXP
USB3_3_TXN/SSIC_2_TXN
USB3_3_TXP/SSIC_2_TXP
USB3_4_RXN
USB3_4_RXP
USB3_4_TXN
USB3_4_TXP
USB3_5_RXN
USB3_5_RXP
USB3_5_TXN
USB3_5_TXP
USB3_6_RXN
USB3_6_RXP
USB3_6_TXN
USB3_6_TXP
USB_SPT_1
USB_SPT_2
S_U2RXDN1_R
S_U2RXDP1_R
S_U3TXDN1_R
S_U3TXDP1_R
S_U2RXDN2_R
S_U2RXDP2_R
S_U3TXDN2_R
S_U3TXDP2_R
S_U2RXDN3_R
S_U2RXDP3_R
S_U3TXDN3_R
S_U3TXDP3_R
S_U2RXDN4_R
S_U2RXDP4_R
S_U3TXDN4_R
S_U3TXDP4_R
SC154
SC155
SC157
SC156
SC159
SC158
SC161
SC160
0.1UF/16V
X7R
N/A
S_U3TXDN1_C
S_U3TXDP1_C
S_U3TXDN2_C
S_U3TXDP2_C
S_U3TXDN3_C
S_U3TXDP3_C
S_U3TXDN4_C
S_U3TXDP4_C
GPP_A1/LAD1/ESPI_IO0
GPP_A2/LAD2/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS0#
GPP_A6/SERIRQ/ESPI_CS1#
GPP_A7/PIRQA#/ESPI_ALERT0#
GPP_A8/RCIN#/ESPI_ALERT1#
GPP_A14/SUS_STAT#/ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_G19/SM#
GPP_G18/NM#
GPP_E6/DEVSLP2
GPP_E5/DEVSLP1
GPP_E4/DEVSLP0
GPP_F9/DEVSLP7
GPP_F8/DEVSLP6
GPP_F7/DEVSLP5
GPP_F6/DEVSLP4
GPP_F5/DEVSLP3
S_LAD[3..0]
S_LAD0
S_LAD1
S_LAD2
S_LAD3
S_LFRAME#
S_SERIRQ
S_GPP_A7
O_KBRST#
S_PWRDWN#
S_LPC_PD#
CK_24M_SIO_R
If no TPM,delete it
CRB PU +3V for SMI#
S_GPP_G19
S_GPP_G18
S_GPP_E4
S_GPP_F6
M2/SE1_DEVSLP
Check spec to determine whether to use these signal
PD on SIO side(+3VSB)
SR145
8.2KOhm
SR192
SR193
CK_24M_SIO_R
SR3
SR4
CK_24M_SIO_IO
CK_24M_SIO_LPC
If not NXP DP2VGA solution,delete this
CK_24M_TPM_R
SR128
CK_24M_TPM
If not TPM,delete this
close to PCH

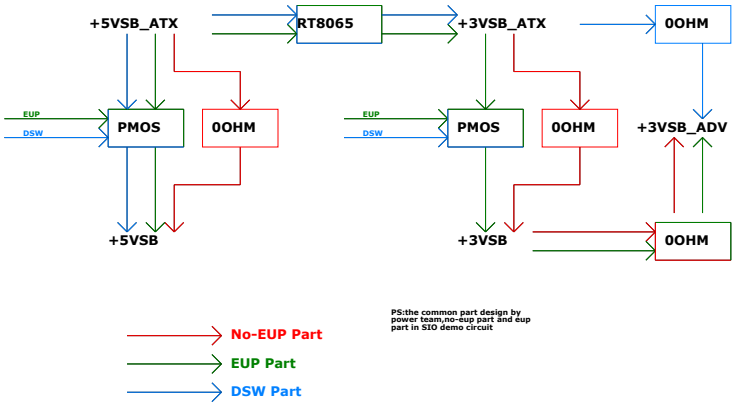

SU1H
SPT-H_PCH
SKYLAKE_PCH
REV = <REV>
02001-00491200
CORE
VCCPGPPD
MISC
USB
SR61
SR72
SR70
SR71
SR7
SR87
SR155
SR154
SR153
SR156
SC181
SC189
SC187
SC185
SC183
SC188
SC186
SC184
SC85
SC3
SC160
SC191
SC81
SC89
SC177
SC178
SC82
SC83
SC174
SC84
SC86
SC87
SC88
SC179
SC180
SC79
SC80
SC192
SC188
SD201
SD202
SD200
SD203
SD204
SD205
PESD5V0S1UB
07V10D55V0S0
+1.0V_A
+1.0V_A_VCCAMPHYPLL
+1.0V_A_VCCAPLL
+1.0V_A_XCLK_BIAS
+3V_SPI
+3V_BAT
+3V
+3VSB
+3VSB_ADV
+3VSB_HDA
+1V0_PCH_VCCDSW
+P1V0_PRIME_PCH_FUSE_2V8
VCCPGPPD
VCC_RTCEXT_CAP
VCCPFUSE_3P3
VCCPRIM_1p0_11
VCCPRIM_1p0_12
VCCPRIM_1p0_13
VCCPRIM_1p0_14
VCCPRIM_1p0_15
VCCPRIM_1p0_16
VCCPGPPA
VCCPGPPB
VCCPGPPC
VCCPGPPD
VCCPGPPE
VCCPGPPF
VCCPGPPG
VCCPGPPH
VCCPGPPBCH1
VCCPGPPBCH2
VCCPGPPEF1
VCCPGPPEF2
VCCPGPPG
VCCPRIM_3p3_1
VCCDSW_3p3_2
VCCSPI
VCCSPI2
VCCSPI3
VCCRTCPRIM_3p3
VCCRTC
DCPRTC
VCCPRIM_3p3_2
VCCPRIM_3p3_3
VCCPRIM_3p3_4
VCCPRIM_1p0_1
VCCPRIM_1p0_2
VCCPRIM_1p0_3
VCCPRIM_1p0_4
VCCPRIM_1p0_5
VCCPRIM_1p0_6
VCCPRIM_1p0_7
VCCPRIM_1p0_8
VCCPRIM_1p0_9
VCCPRIM_1p0_10
DCPDSW_1p0
VCCCLK1
VCCCLK3
VCCCLK4
VCCCLK2_1
VCCCLK2_2
VCCCLK5_1
VCCCLK5_2
VCCMPHY_1p0_1
VCCMPHY_1p0_2
VCCMPHY_1p0_3
VCCMPHY_1p0_4
VCCMPHY_1p0_5
VCCMPHYPLL_1p0_1
VCCMPHYPLL_1p0_2
VCCPCIE3PLL_1p0_1
VCCPCIE3PLL_1p0_2
VCCAPLLEBB_1p0
VCCPRIM_1p0_17
VCCUSB2PLL_1p0_1
VCCUSB2PLL_1p0_2
VCCHDAPLL_1P0
VCCHDA
VCCDSW_3p3_1
VCCSTG
VCCIO
VCCSPI
VCCRTCEXT
VCCDSW_3P3
VCCPRIM_1P0
VCCPRIM_3P3
VCCMPHYPLL
VCCPCIE3PLL
VCCAPLLEBB
VCCUSB2PLL
VCCHDAPLL
VCCHDA
VCCDSW_3P3
Place close to PCH Pin AJ43 , AH43
Place close to PCH Pin AJ5, AL5, AR19
Place close to PCH Pin K2 , R3
Place close to PCH pin AD15
Place close to PCH pin U25, V26 , AC17,AA26,AC26,AE23,Y23
Place close to PCH pin U21
Place close to PCH pin BC42
Place close to PCH pin AA23
Place close to PCH pin AA22
Place close to PCH pin AD13
Place close to PCH pin BA29
Place close to PCH Pin W15,BA24,BA31
Place close to PCH Pin BA15
BOARD CAP SC3 FOR VCCRTCEXT
PLACE 3-5MM FROM PACKAGE EDGE PIN BA26
GROUP D POWER
LPT-H : 3.3V (FOR INTERPOSER) CRB
SPT-H : 1.8V
注意PCH GPIO D Group power plane
PCH-H SPEC : GPP A~G 1.8V or 3.3V
PCH-H SPEC : GPP I only 3.3V
Deep Sleep Well Group (GPD) only 3.3V
RVP8 GPP D : 3.3V
RVP10 GPP D : 1.8V
Change by intel update


SU1I
SPT-H_PCH
SKYLAKE_PCH
REV = <REV>
02001-00491200
SU1L
SPT-H_PCH
SKYLAKE_PCH
REV = <REV>
02001-00491200
CPU_VSS_AB11
SR241
SU1J
SPT-H_PCH
SKYLAKE_PCH
REV = <REV>
02001-00491200
TP_PCH_AR22
TP_PCH_W13
TP_PCH_U13
TP_PCH_AN29
PREQ#
PRDY#
CPU_TRST#
PCH_TRIGOUT
PCH_TRIGIN
H_CPU_TRIGGER
S_CPU_TRIGGER
SR242
300hm
S_CPU_TRIGGER_R
S_XDP_PREQ#
S_XDP_PRDY#
S_XDP_TRST#
M1
M2
SMD98X87
HEATSINK1
HEATSINK
13071-00019600
SR240
CPU_VSS_AB10
GND


+3VSB
Strap
CMB is 4.7k
SR27
10K/5%
/X
S_GPP_B22
SR30
2.2K/5%
CMB is 20k
GND
Boot BIOS Destination
0 SPI (Default)
1 LPC
+3VSB
Strap
CMB is 4.7k
SR31
10K/5%
/X
S_GPP_B18
SR32
10K/5%
/X
GND
0 = Disable "No Reboot" mode. (Default)
1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.
GPI PU
SU1K
SPT-H_PCH
/X/SPTH ST205
/X/SPTH ST207
/X/SPTH ST206
/X/SPTH ST209
/X/SPTH ST208
/X/SPTH ST212
S_GPP_B22
S_GPP_B21
S_GPP_B20
S_GPP_B19
S_GPP_B18
S_GPP_B17
S_GPP_B16
S_GPP_B15
S_GPP_D23
GP_CHAFAN_PWM_DCR
71,72
31
ME_UNLOCK
GPP_B22/GSPI1_MOSI
GPP_B21/GSPI1_MISO
GPP_B20/GSPI1_CLK
GPP_B19/GSPI1_CS#
GPP_B18/GSPI0_MOSI
GPP_B17/GSPI0_MISO
GPP_B16/GSPI0_CLK
GPP_B15/GSPI0_CS#
GPP_C9/UART0_TXD
GPP_C8/UART0_RXD
GPP_C11/UART0_CTS#
GPP_C10/UART0_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD
GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA
GPP_D4/ISH_I2C2_SDA/ISH_I2C3_SDA
GPP_D23/ISH_I2C2_SCL/ISH_I2C3_SCL
GPP_D9
GPP_D10
GPP_D11
GPP_D12
GPP_D15/ISH_UART0_CTS#
GPP_D15/ISH_UART0_RTS#
GPP_D14/ISH_UART0_TXD
GPP_D13/ISH_UART0_RXD
/SML0CLK/I2C2_SCL
/SML0DATA/I2C2_SDA
GPP_H20/ISH_I2C0_SCL
GPP_H19/ISH_I2C0_SDA
GPP_H22/ISH_I2C1_SCL
GPP_H21/ISH_I2C1_SDA
GPP_A23/ISH_GP5
GPP_A22/ISH_GP4
GPP_A21/ISH_GP3
GPP_A20/ISH_GP2
GPP_A19/ISH_GP1
GPP_A18/ISH_GP0
GPP_A17/ISH_GP7
S_GPP_D11
S_GPP_D12
S_GPP_D16
S_GPP_D15
S_PCB2
S_PCB1
S_GPP_D14
S_PCB0
S_GPP_D13
S_GPP_H20
S_GPP_H19
S_GPP_A23
S_GPP_A22
S_GPP_A21
S_GPP_A20
S_GPP_A19
SR1617
S_GPP_A18
SR1614
S_GPP_A17
SR1620
PCIEX16_SL1_PRSNT#
PS_TCC_EN#
PS_LS_OE#_HDMI
49
18
SKYLAKE_PCH
620501-004912G0
If the signal here is not unused,the GPIO need to be pull high to 3VSB here
REV = <REV>
+3VSB
SR1639
8.2KOhm
S_GPP_H20
+3V
SR1715
SR1716
SR1717
SR1718
SR1719
SR1720
SR1721
8.2KOhm
N/A
/X
S_GPP_A17
S_GPP_A18
S_GPP_A19
S_GPP_A20
S_GPP_A21
S_GPP_A22
S_GPP_A23
+3VSB
SR1729
8.2KOhm
N/A
SC900
SR934
2.2KOhm
/X
0.1UF/16V
S_GPP_D12
H2N7002
SQ901
P_+VCCSAIO_OVI_1_10
82
GND
+3VSB
SR1728
8.2KOhm
/X
SC901
SR1651
2.2KOhm
N/A
0.1UF/16V
S_GPP_D11
H2N7002
SQ902
P_+VCCSAIO_OVI_2_10
82
GND
+3VSB
SR1730
8.2KOhm
/X
SC905
SR1662
2.2KOhm
N/A
0.1UF/16V
S_GPP_D16
H2N7002
SQ907
P_+1.0V_A_OV_1_10
87
GND
PCB Rev. Strap
+3V
SR37
SR39
SR64
SR38
SR43
SR73
1KOhm
8.2KOhm
/X
S_PCB0
S_PCB1
S_PCB2
GND


connect to PCI&PCIE SLOT
24 S_SMBCLK_SLOT
24 S_SMBDATA_SLOT
SR1613 0Ohm /X
SR1612 0Ohm /X
31 S_SMBCLK_VSB
31 S_SMBDATA_VSB
SRN13A 2.2KOHM
SRN13B 4.7KOHM
SRN13C 4.7KOHM
SRN13D 4.7KOHM
+3VSB
SRN202D 1KOHM
SRN202C 1KOHM
SRN202B 1KOHM
SRN202A 1KOHM
+3V
SQ1 H2N7002
SQ2 H2N7002
S_SMBCLK_MAIN 12,17,79
S_SMBDATA_MAIN 12,17,79
SC56 10PF/50V /X NPO
SC57 10PF/50V /X NPO
GND
Place near PCH
SR304 1KOhm mbs_r0603
+12V
SQ2C1 0.1UF/16V N/A
SQ3 PMBS3904 /X
SR305 1KOhm /X
+3VSB
SQ40 H2N7002 /X
31,38,92 S_PWROK
SQ40C1 0.1UF/16V /X

POWER FLOW

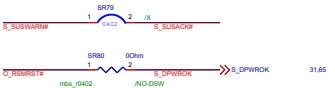


PS:the common part design by power team,no-eup part and eup part in SIO demo circuit

NOT SUPPORT DSW

Power plane

Control link

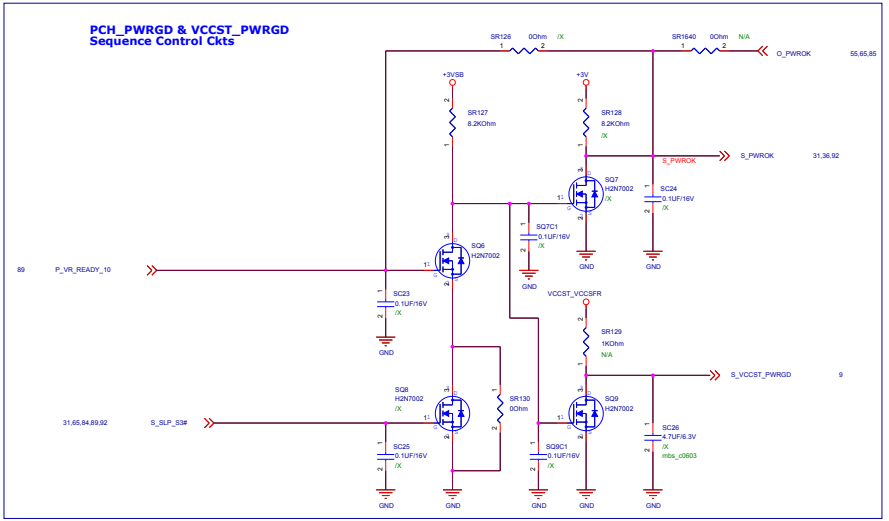


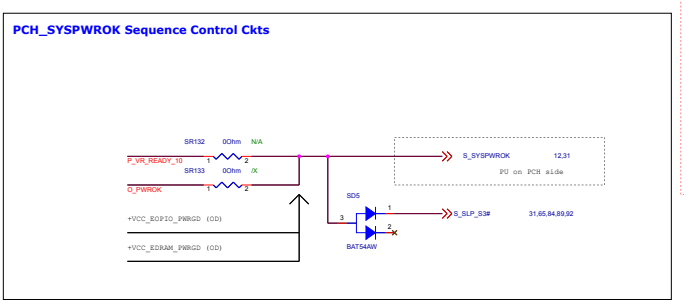
SUPPORT DSW

Power plane

Control link

S_DPOWER Sequence





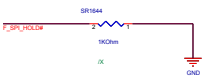
1. PCH will have a minimum of a 1ms delay from PCH_PWROK to assertion of PROCPWRGD.
2. PLTRST# = AND (PCH_PWROK, SYS_PWROK, PROCPWRGD) Refer to PDG Figure 4S-1 SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation
3. It is recommended that SYS_PWROK be asserted after both PWROK assertion and processor PCH does not monitor
4. PCH_PWROK and SYS_PWROK both needs to be high to exit reset, but either signal can come up first. SYS_PWROK be asserted after both PWROK assertion and processor core VR PWRGD assertion.

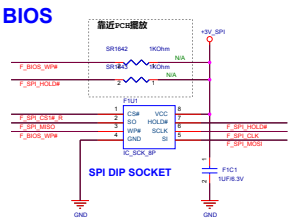
0.3G Beta

Standard Circuit	
BIOS	SPI
REV.	P1_0.3G_Beta

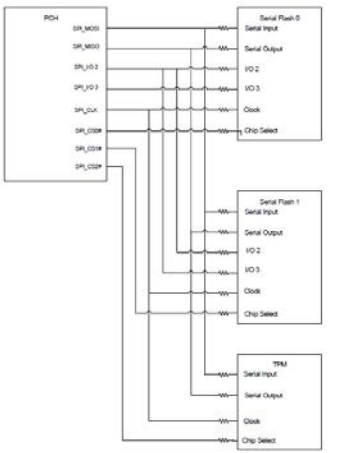
SPI /XSPI

BIOS





Reserved for support SBA/AMT



SPI DIP 64M Flash P/N:

05006-00010600

SPI DIP 128M Flash P/N:

05006-00090700

F1U2

SPI ROM
DIP 64M

05006-00090700

PCB

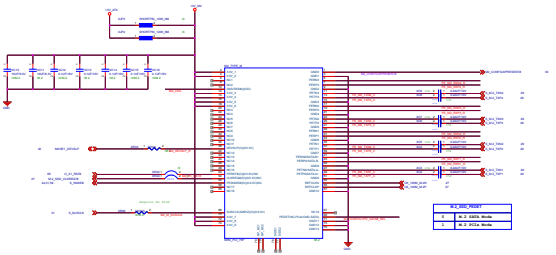
SPI ROM
DIP 64M

08001-07050200

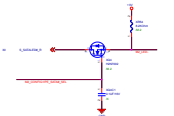
MB_LABEL

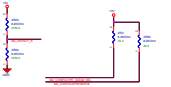
SPI ROM
DIP 64M

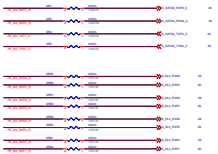
15100-13200000

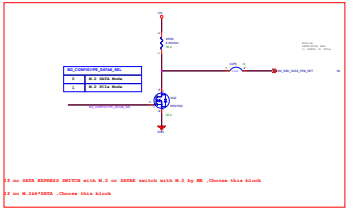


M2_SATA_FRONT	
0	M.2 SATA Mode
1	M.2 PCIe Mode

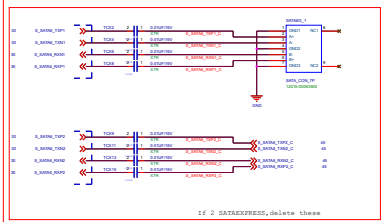


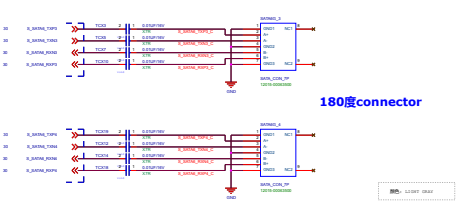




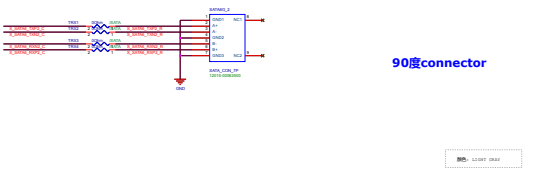


M2_CONFIG(PE_SATA#_SEL	GATA#1_GPIO37	M2_CONFIG1(PERST0#)	Result
0	0	0	M.2 change to SATA mode,PCIe #1 change to SATA,PCIe #11 change to DISB
0	0	1	M.2 change to SATA mode,PCIe #1 hold change to SATA mode
0	1	0	M.2 change to SATA mode,PCIe #1 hold change to DISB mode
0	1	1	M.2 keep to SATA mode,PCIe #1 hold change to DISB mode
1	0	0	M.2 change to DISB mode,PCIe #1 hold change to SATA mode
1	0	1	M.2 keep to DISB mode,PCIe #1 hold change to SATA mode
1	1	0	M.2 change to DISB mode,PCIe #1 hold change to DISB mode
1	1	1	M.2 keep to DISB mode,PCIe #1 hold change to DISB mode

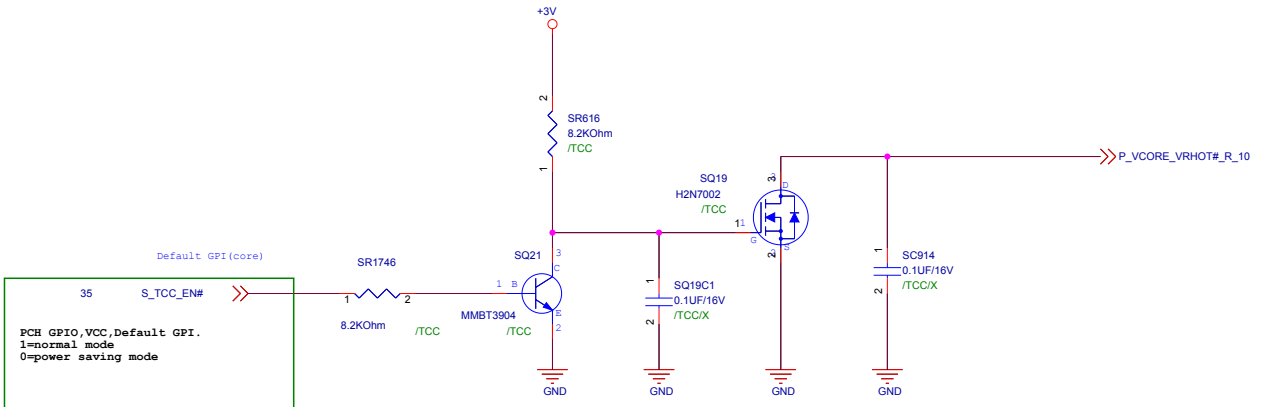

If 2 SATAEXPRESS,delete these


180度connector

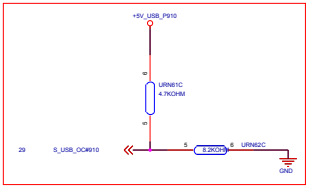

If 2 SATAEXPRESS,delete these

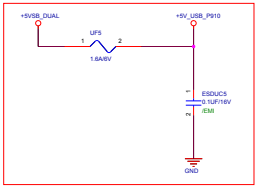

90度connector

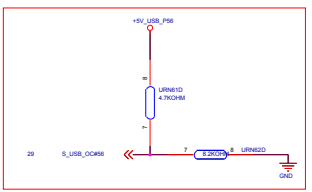
TCC control

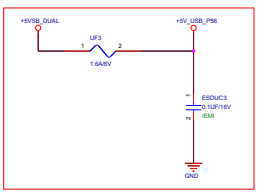

+3V
SR616
8.2KOhm
/TCC
SQ19
H2N7002
/TCC
P_VCORE_VRHOT#_R_10
Default GPI(core)
35
S_TCC_EN#
PCH GPIO,VCC,Default GPI.
1=normal mode
0=power saving mode
SR1746
8.2KOhm
/TCC
SQ21
MMBT3904
/TCC
SQ19C1
0.1UF/16V
/TCC/X
SC914
0.1UF/16V
/TCC/X
GND
GND
GND
GND

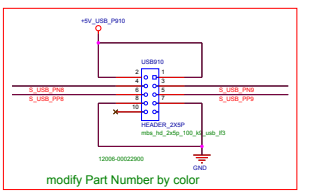
OC# circuit for Intel



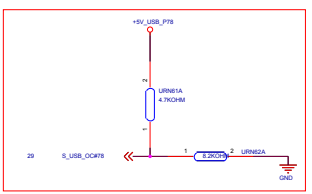


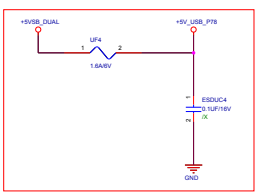






29,51 S_USB_PN8
29,51 S_USB_PP8
29,51 S_USB_PN9
29,51 S_USB_PP9

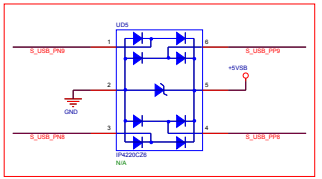




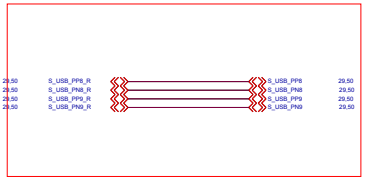
29,51,68 S_USB_PN6
29,51,68 S_USB_PP6
29,51,68 S_USB_PN7
29,51,68 S_USB_PP7

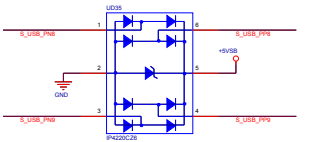
Delete it for EMS

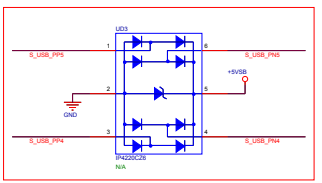
ESD Diode

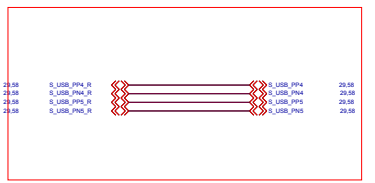


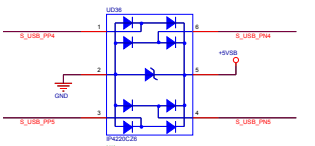
Reserve Location (RES A)

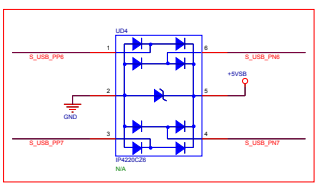


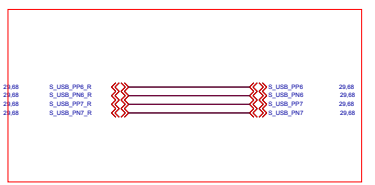


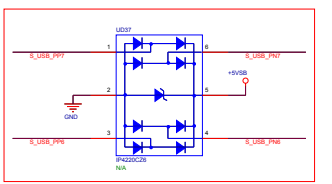




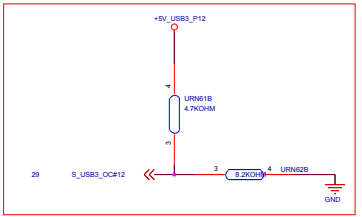


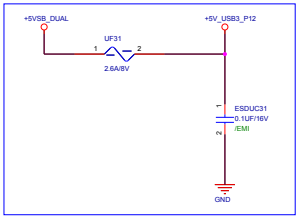


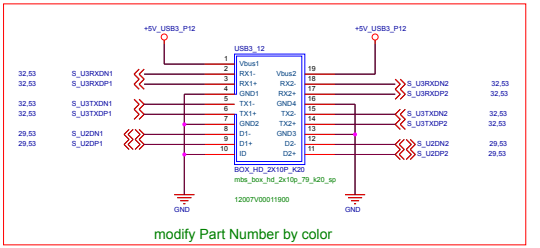


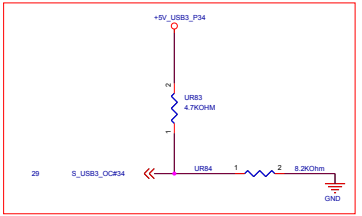


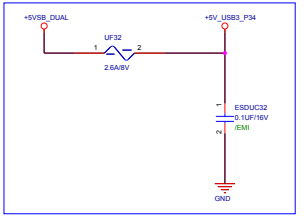
OC# circuit for Intel





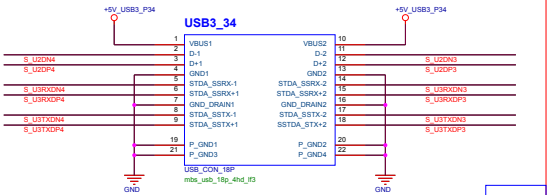






OP3 - Connector

Ext USB3 Connector 1&2

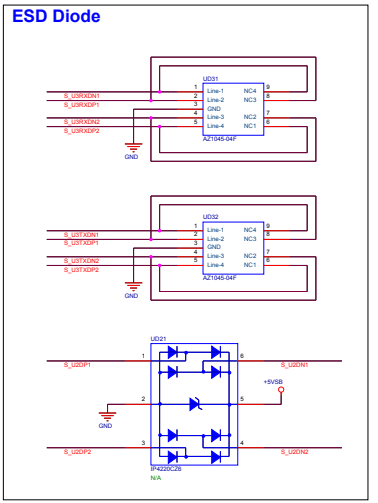


OP3

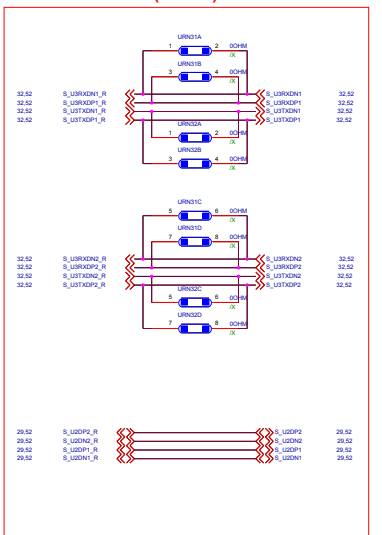
Port 12

Delete it for EMS

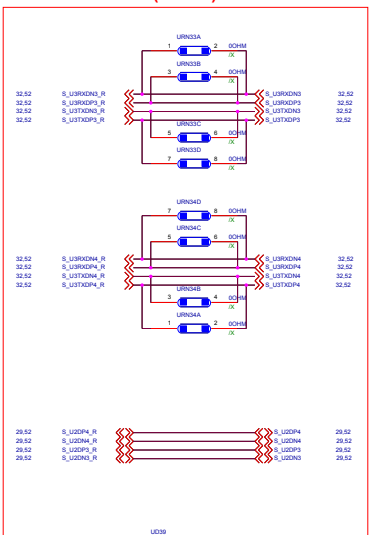
ESD Diode



Reserve Location (RES A)

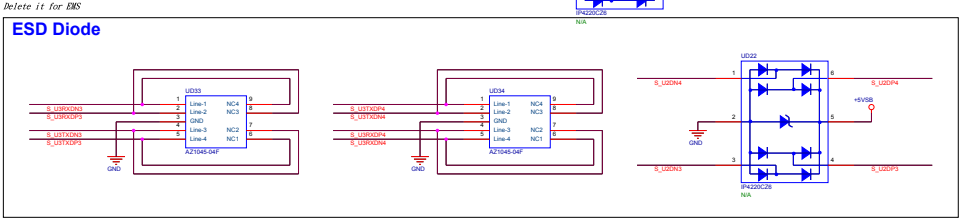


Reserve Location (RES A)



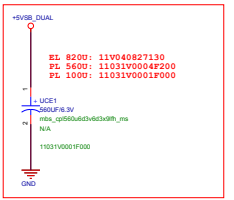
Delete it for EMS

ESD Diode

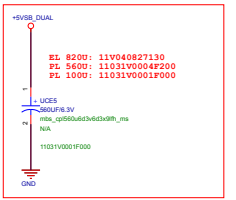


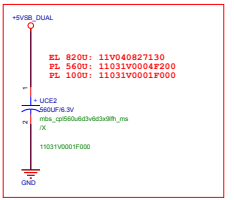
Port 34

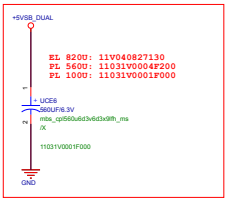
PL CAP & EL CAP co-lay



PL CAP & EL CAP co-lay



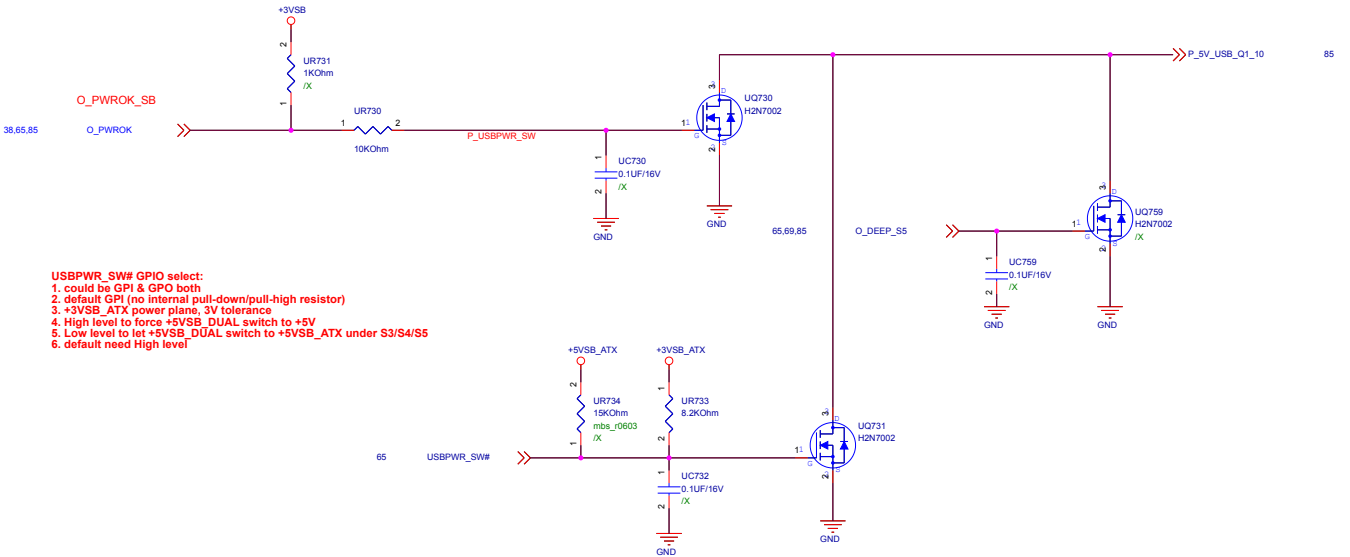


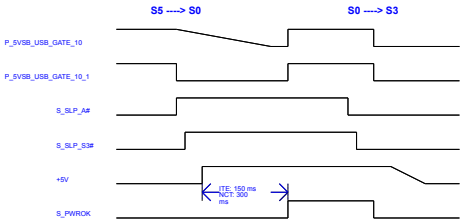


BOM	
N/A	mount
/X	unmount

STANDARD CIRCUIT	
XDMS	USB
CS_USB_0.2B	

HD_DEMO_USB
/X

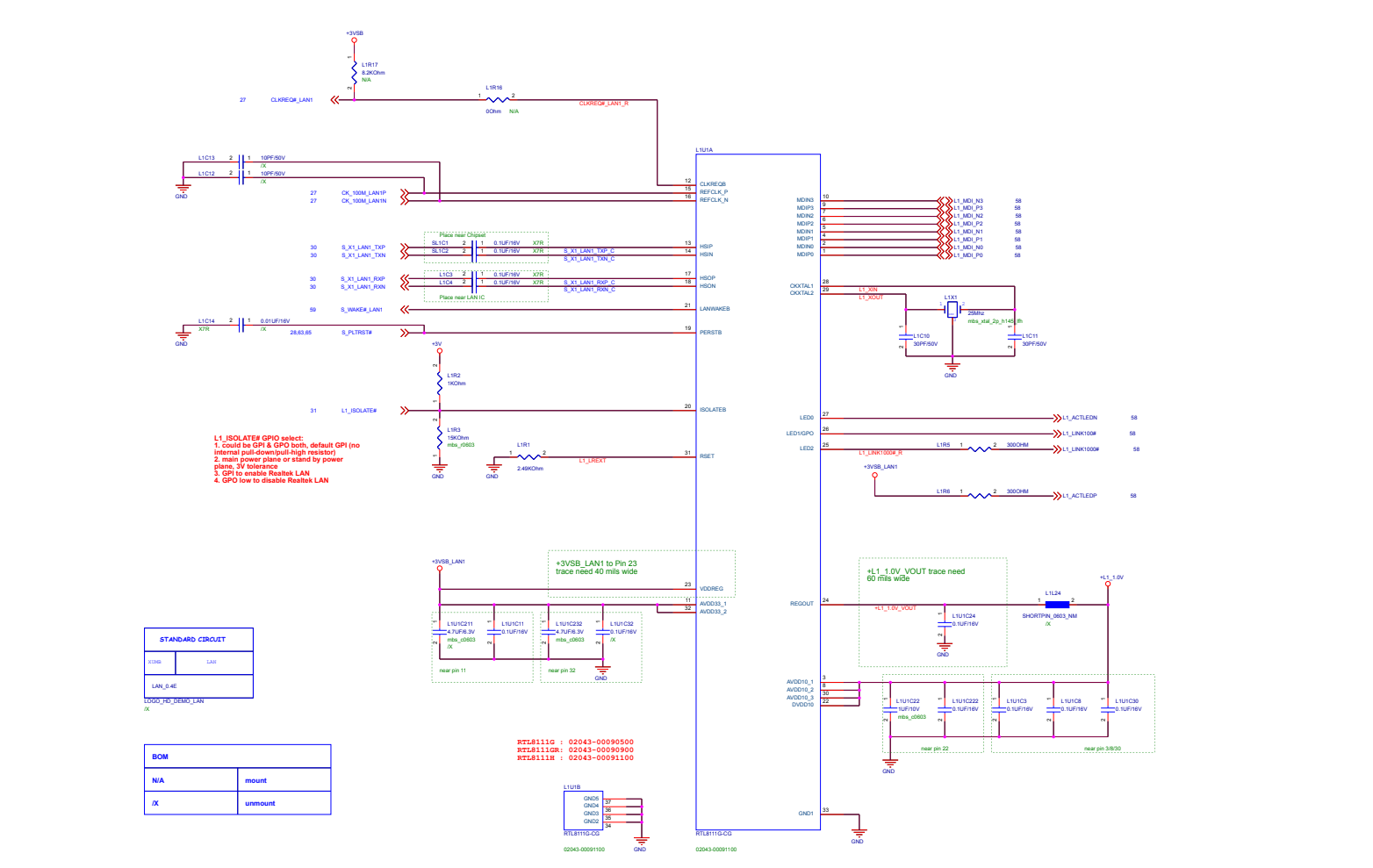

+3VSB
UR731
1KOhm
/X
O_PWROK_SB
38,65,85
O_PWROK
UR730
10KOhm
P_USBPWR_SW
UC730
0.1UF/16V
/X
GND
UQ730
H2N7002
P_5V_USB_Q1_10
85
65,69,85
O_DEEP_S5
UQ759
H2N7002
/X
UC759
0.1UF/16V
/X
USBPWR_SW# GPIO select:
1. could be GPI & GPO both
2. default GPI (no internal pull-down/pull-high resistor)
3. +3VSB_ATX power plane, 3V tolerance
4. High level to force +5VSB_DUAL switch to +5V
5. Low level to let +5VSB_DUAL switch to +5VSB_ATX under S3/S4/S5
6. default need High level
+5VSB_ATX
+3VSB_ATX
UR734
15KOhm
mbs_r0603
/X
UR733
8.2KOhm
65
USBPWR_SW#
UC732
0.1UF/16V
/X
UQ731
H2N7002



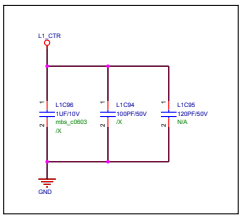
don't need for Flash Back

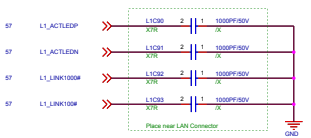
for USB Port default have Power

Inrush Circuit for USB Port default have Power or Flash Back Function

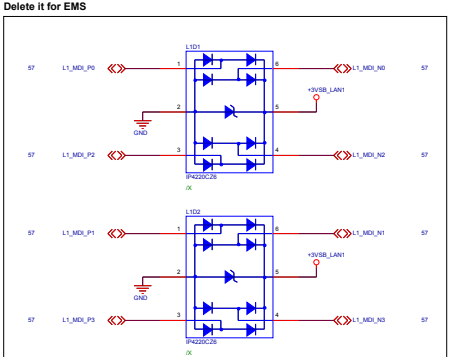

+3VSB
L1R17
8.2KOhm
N/A
27
CLKREQ#_LAN1
L1R16
0Ohm
N/A
CLKREQ#_LAN1_R
L1U1A
L1C13
10PF/50V
/X
L1C12
10PF/50V
/X
GND
27
CK_100M_LAN1P
27
CK_100M_LAN1N
12
CLKREQB
15
REFCLK_P
16
REFCLK_N
Place near Chipset
SL1C1
SL1C2
0.1UF/16V
X7R
30
S_X1_LAN1_TXP
30
S_X1_LAN1_TXN
13
HSIP
14
HSIN
S_X1_LAN1_TXP_C
S_X1_LAN1_TXN_C
L1C3
L1C4
0.1UF/16V
X7R
30
S_X1_LAN1_RXP
30
S_X1_LAN1_RXN
17
HSOP
18
HSON
S_X1_LAN1_RXP_C
S_X1_LAN1_RXN_C
Place near LAN IC
59
S_WAKE#_LAN1
21
LANWAKEB
L1C14
0.01UF/16V
X7R
/X
28,63,65
S_PLTRST#
19
PERSTB
+3V
L1R2
1KOhm
31
L1_ISOLATE#
20
ISOLATEB
L1R3
15KOhm
mbs_r0603
L1R1
2.49KOhm
L1_1REXT
31
RSET
GND
L1 ISOLATE# GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-down/pull-high resistor)
2. main power plane or stand by power plane, 3V tolerance
3. GPI to enable Realtek LAN
4. GPO low to disable Realtek LAN
+3VSB_LAN1
+3VSB_LAN1 to Pin 23
trace need 40 mils wide
23
VDDREG
11
AVDD33_1
32
AVDD33_2
L1U1C211
4.7UF/6.3V
mbs_c0603
/X
L1U1C11
0.1UF/16V
near pin 11
L1U1C232
4.7UF/6.3V
mbs_c0603
L1U1C32
0.1UF/16V
/X
near pin 32
GND
MDIN3
MDIP3
MDIN2
MDIP2
MDIN1
MDIP1
MDIN0
MDIP0
L1_MDI_N3
L1_MDI_P3
L1_MDI_N2
L1_MDI_P2
L1_MDI_N1
L1_MDI_P1
L1_MDI_N0
L1_MDI_P0
58
OKXTAL1
OKXTAL2
L1_XIN
L1_XOUT
L1X1
25Mhz
mbs_xtal_2p_h145dth
L1C10
30PF/50V
L1C11
30PF/50V
LED0
LED1/GPO
LED2
L1_ACTLEDN
L1_LINK100#
L1_LINK1000#
L1_ACTLEDP
L1_LINK1000#_R
L1R5
L1R6
300OHM
+3VSB_LAN1
REGOUT
+L1_1.0V_VOUT trace need
60 mils wide
+L1_1.0V
L1L24
SHORTPIN_0603_NM
/X
+L1_1.0V_VOUT
L1U1C24
0.1UF/16V
AVDD10_1
AVDD10_2
AVDD10_3
DVDD10
L1U1C22
1UF/10V
mbs_c0603
L1U1C222
0.1UF/16V
near pin 22
L1U1C3
0.1UF/16V
L1U1C8
0.1UF/16V
L1U1C30
0.1UF/16V
near pin 3/8/30
GND1
L1U1B
GND5
GND4
GND3
GND2
RTL8111G-CG
02043-00091100
RTL8111G : 02043-00090500
RTL8111GR: 02043-00090900
RTL8111H : 02043-00091100
STANDARD CIRCUIT
XTBB
LAN
LAN_0.4E
LOGO_HD_DEMO_LAN
/X
BOM
N/A
mount
/X
unmount

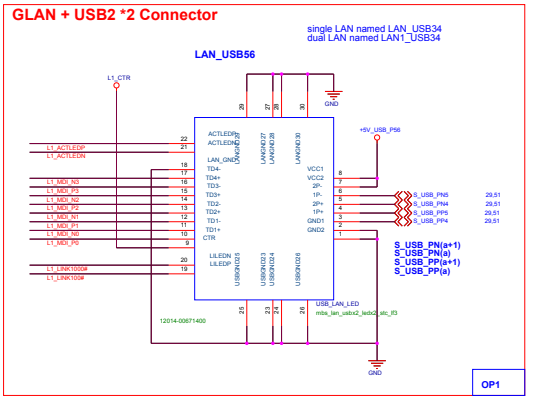
for Intel LAN





Delete it for EMS





Intel LAN I217 should use old LAN Surge Connector
U2+LAN Connector: 12014-00061500
U3+LAN Connector: 12014-00061400

LAN1 POWER

1. LAN IC power change to +3VSB_ATX (remove short-pin L1R88, add resistor L1R88 & L1R89)

---

for Intel PHY

2. for Intel PHY LAN, L1_LAN_DISABLE# renamed L1_LAN_DISABLE#_R in LAN IC Page

3. for Intel PHY LAN, L1_LAN_DISABLE# pull high resistor L1R7 Optional change to /LAN1_ERP_WAKE

4. for Intel PHY LAN, L1_LAN_WAKE# renamed L1_LAN_WAKE#_R in LAN IC Page

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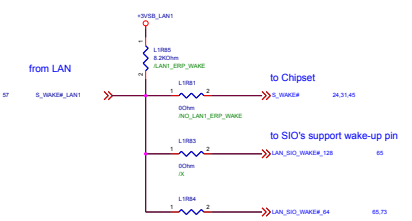
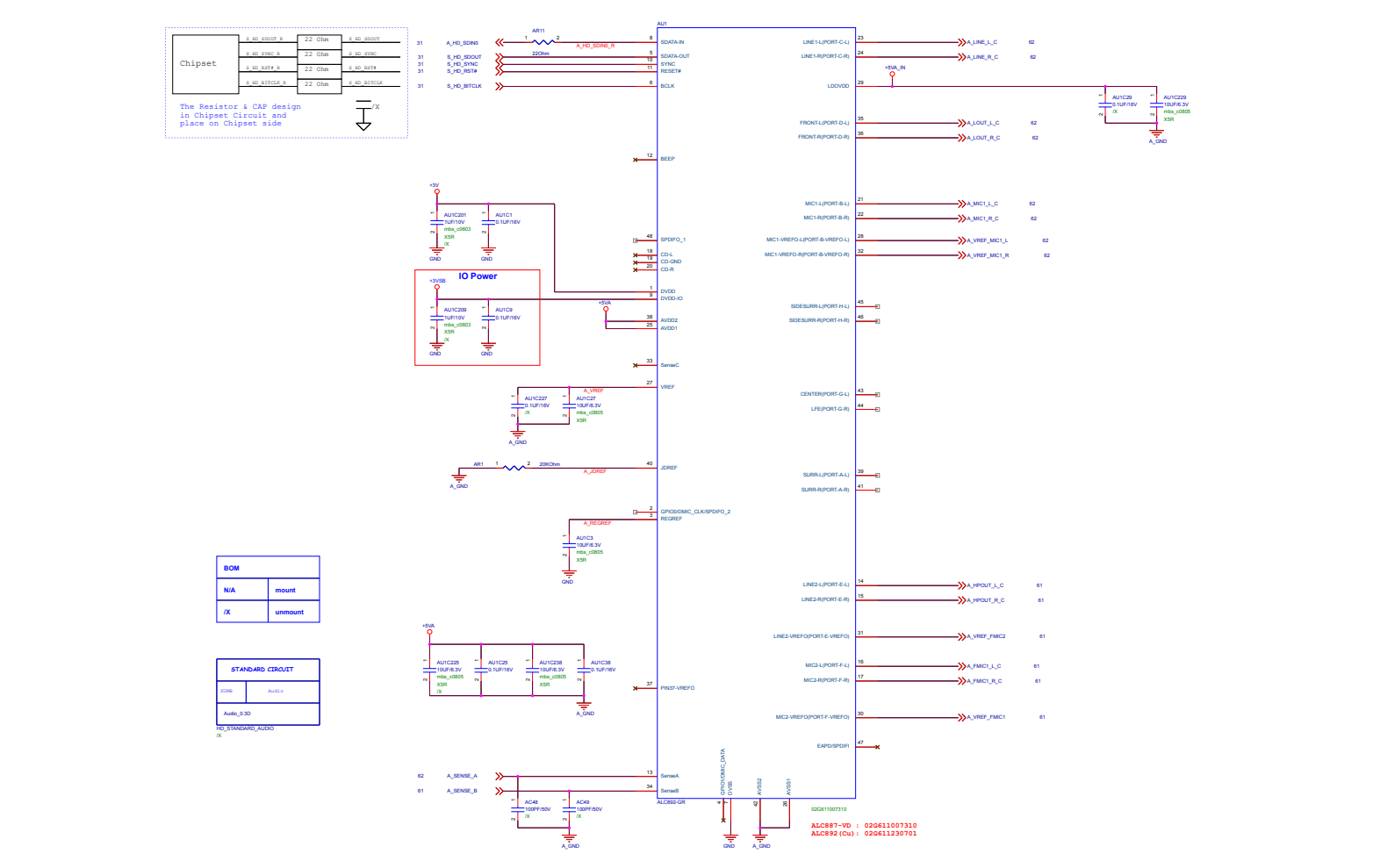
for PCIE LAN1

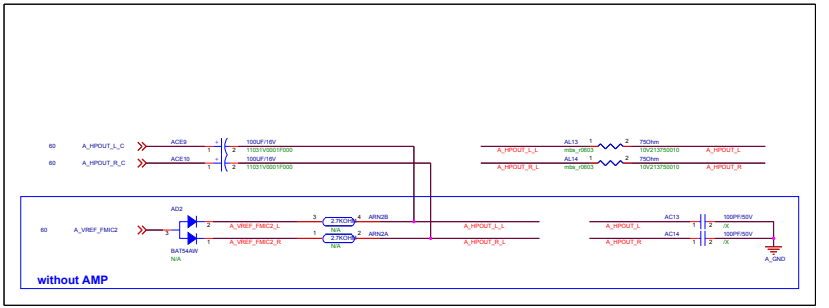
5. for Intel PCIE LAN, L1_DEV_OFF# choose +3VSB_ATX power plane GPIO

6. for PCIE LAN, S_WAKE# renamed S_WAKE#_LAN1 in LAN IC Page



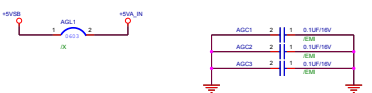

Chipset
S_HD_SDOUT_R
S_HD_SYNC_R
S_HD_RST#_R
S_HD_BITCLK_R
22 Ohn
S_HD_SDOUT
S_HD_SYNC
S_HD_RST#
S_HD_BITCLK
The Resistor & CAP design in Chipset Circuit and place on Chipset side
/X
A_HD_SDIN0
S_HD_SDOUT
S_HD_SYNC
S_HD_RST#
S_HD_BITCLK
AR11
22Ohm
A_HD_SDIN0_R
AU1
SDATA-IN
SDATA-OUT
SYNC
RESET#
BCLK
BEEP
SPDIFO_1
CD-L
CD-GND
CD-R
DVDD
DVDD-IO
AVDD2
AVDD1
SenseC
VREF
JDREF
GPIO0/DMIC_CLK/SPDIFO_2
REGREF
PIN37-VREFO
SenseA
SenseB
ALC892-GR
GPIO1/DMIC_DATA
DVSS
AVSS2
AVSS1
LINE1-L(PORT-C-L)
LINE1-R(PORT-C-R)
LDOVDD
FRONT-L(PORT-D-L)
FRONT-R(PORT-D-R)
MIC1-L(PORT-B-L)
MIC1-R(PORT-B-R)
MIC1-VREFO-L(PORT-B-VREFO-L)
MIC1-VREFO-R(PORT-B-VREFO-R)
SIDESURR-L(PORT-H-L)
SIDESURR-R(PORT-H-R)
CENTER(PORT-G-L)
LFE(PORT-G-R)
SURR-L(PORT-A-L)
SURR-R(PORT-A-R)
LINE2-L(PORT-E-L)
LINE2-R(PORT-E-R)
LINE2-VREFO(PORT-E-VREFO)
MIC2-L(PORT-F-L)
MIC2-R(PORT-F-R)
MIC2-VREFO(PORT-F-VREFO)
EAPD/SPDIF1
+5VA_IN
A_LINE_L_C
A_LINE_R_C
A_LOUT_L_C
A_LOUT_R_C
A_MIC1_L_C
A_MIC1_R_C
A_VREF_MIC1_L
A_VREF_MIC1_R
A_HPOUT_L_C
A_HPOUT_R_C
A_VREF_FMIC2
A_FMIC1_L_C
A_FMIC1_R_C
A_VREF_FMIC1
02G611007310
ALC887-VD : 02G611007310
ALC892(Cu) : 02G611230701
+3V
+3VSB
+5VA
IO Power
AU1C201
AU1C1
AU1C209
AU1C9
AU1C227
AU1C27
AU1C3
AU1C225
AU1C25
AU1C238
AU1C38
AR1
20KOhm
A_JDREF
A_REGREF
A_VREF
AC48
AC49
A_SENSE_A
A_SENSE_B
A_GND
GND
BOM
N/A
mount
/X
unmount
STANDARD CIRCUIT
KEMO
Audio
Audio_0.3D
HD_STANDARD_AUDIO
/X

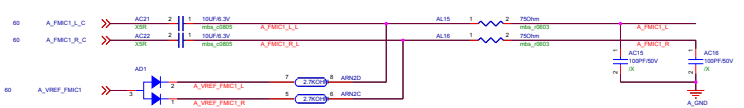
for ALC887-VD2/ALC892/ALC1150



DIP CAP
EL 100U : 11G040810743
PL 100U : 11031V00019000
Audio 100U: 11011-00026000
Gamer 100U: 11011-00028000

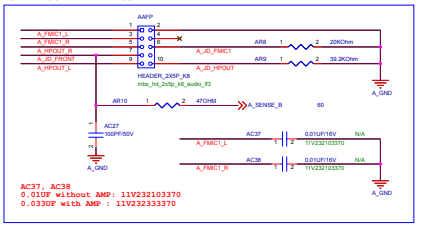
AL13, AL14
75 Ohm: 10V213750010
47 Ohm: 10V213470010





AAFP

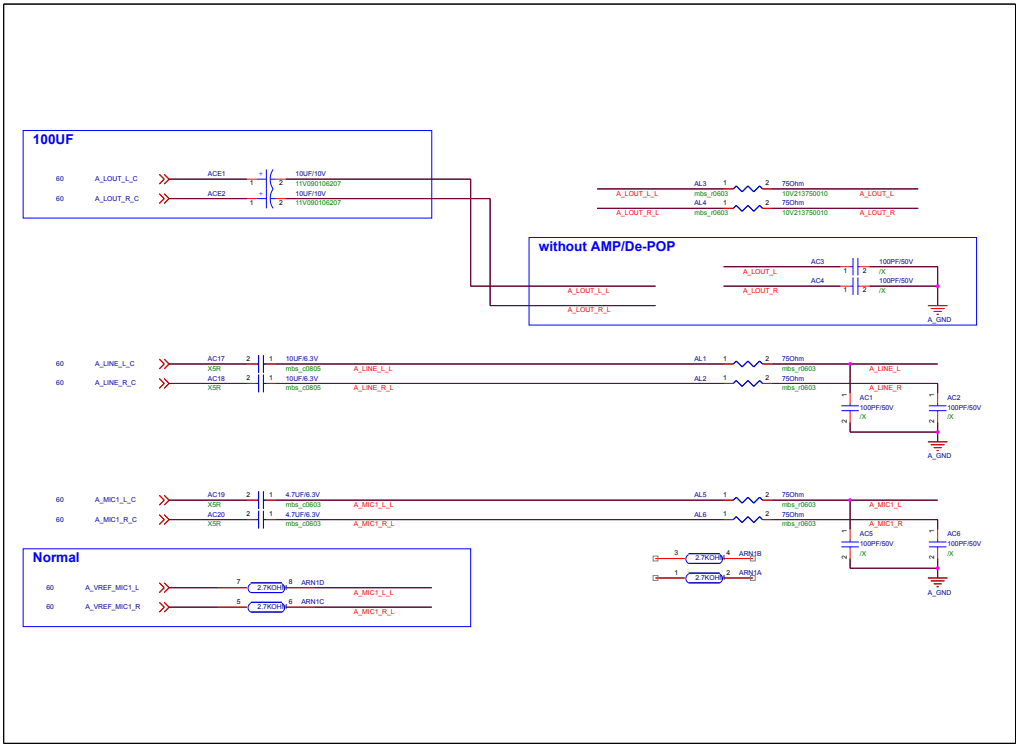
for ALC887-VD2/ALC892



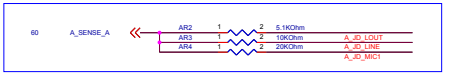
SPDIF Header

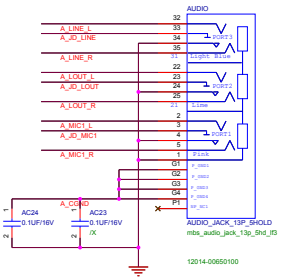
Delete it for EMS

Delete it for EMS



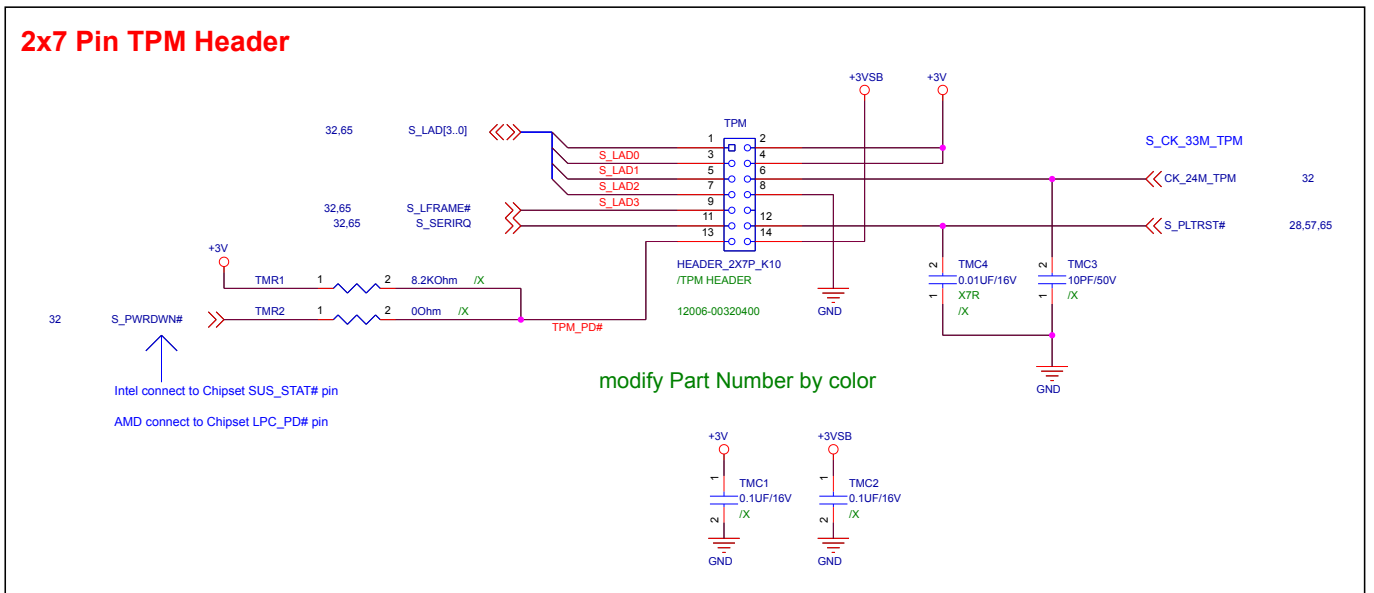
for ALC887-VD2/ALC892





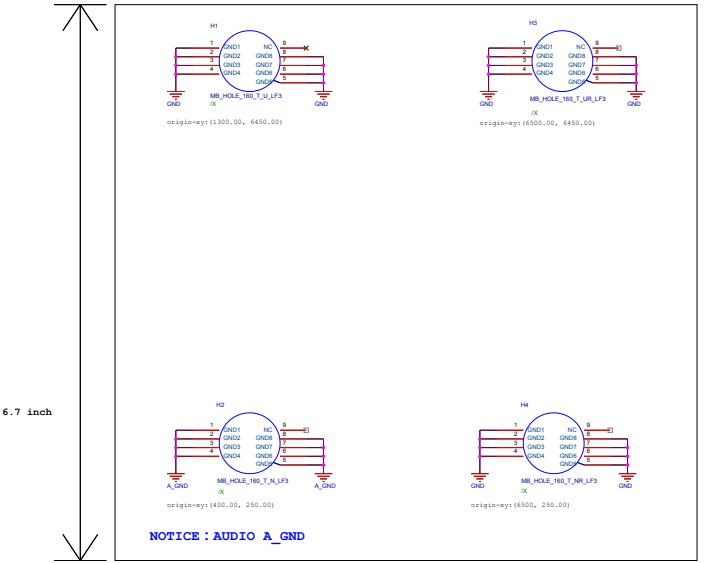
DIP CAP
EL 10U : 11G040822620
PL 10U : 11V090106207
Audio 10U: 11011-00066000
Gamer 10U: 11011-00062000
EL 100U : 11G040810743
PL 100U : 11031V0001P000
Audio 100U: 11011-00026000
Gamer 100U: 11011-00022000

Delete it for EMS

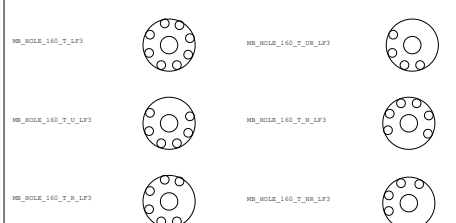


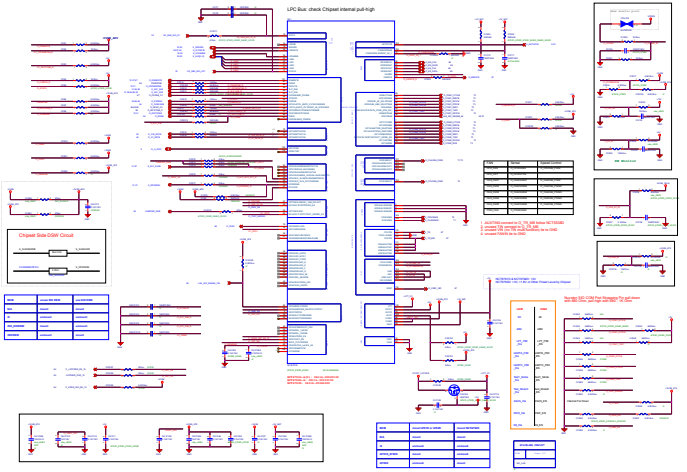
Mini-ITX Screw Hole

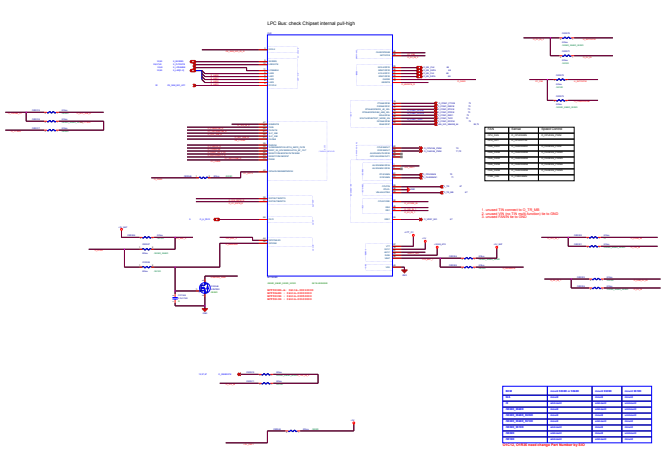
Delete it for EMS



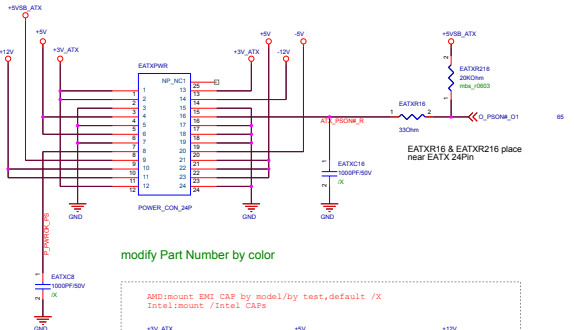
MB SCREW FOOTPRINT



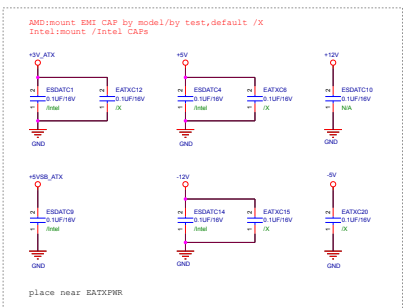

LPC Bus: check Chipset internal pull-high
Chipset Side-SWM Circuit
1. 2nd BIOS connect to G_TP_SPI follow HCT3100D
2. unmount TS5 connect to G_TP_SPI
3. unmount R56 (pin 79) must functionality be to GND
4. unmount R5429 not to GND
Must be EMC CTM Part Depending On Layout
Must Near CPU, with High-speed SIGNAL Trace


LPC Bus: check Chipset internal pull-high
1. unmount TS5 connect to G_TP_SPI
2. unmount R56 (pin 79) must functionality be to GND
3. unmount R5429 not to GND

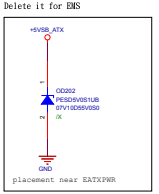
EATX POWER



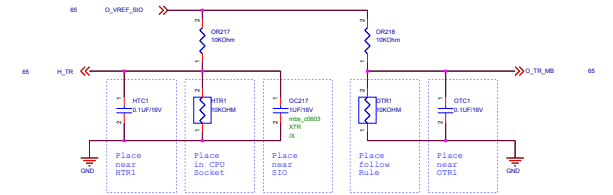
modify Part Number by color



Delete it for EMS



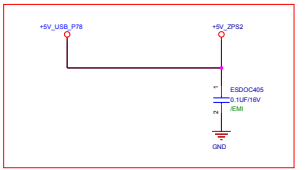
HW Monitor



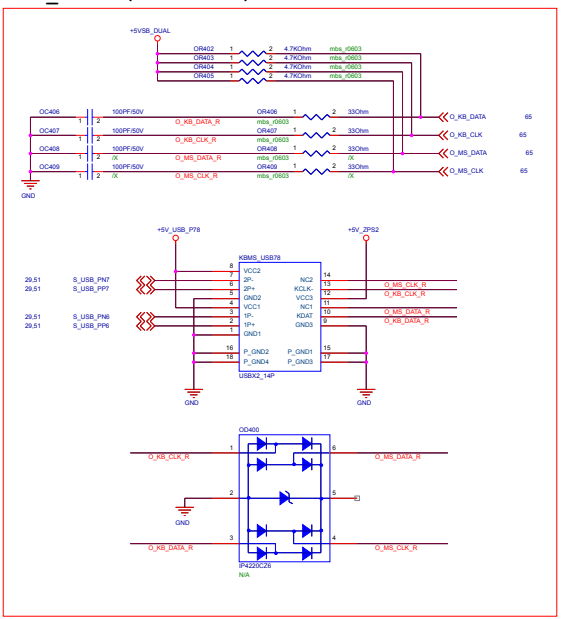
If no CPU thermistor, unmount components HTR1, OC430, OR431

If no MB thermistor, unmount components OTR1, OC432, OR433

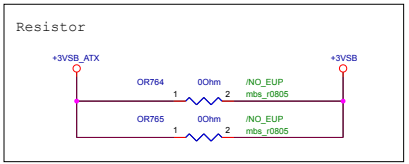
share USB Port Power

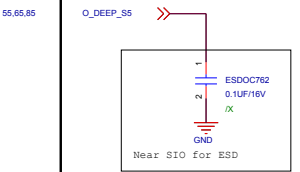


KBMS_USB56 (reserve MS)

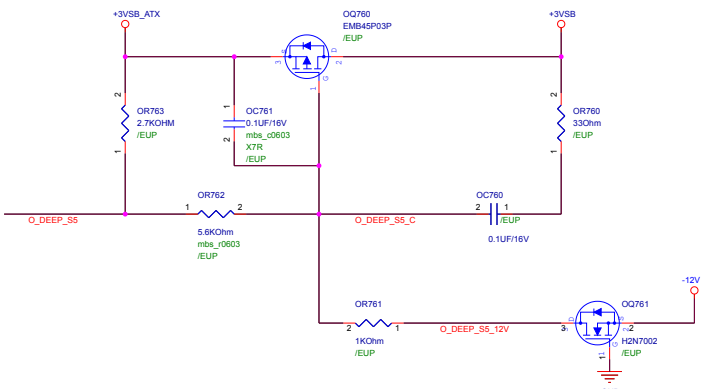


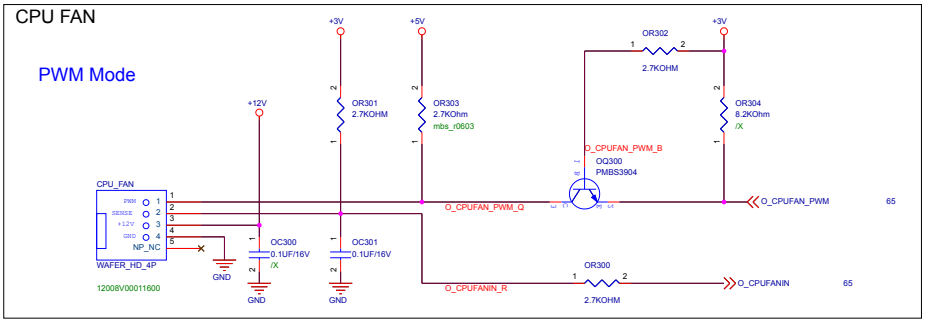
ERP Circuit

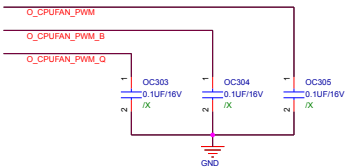




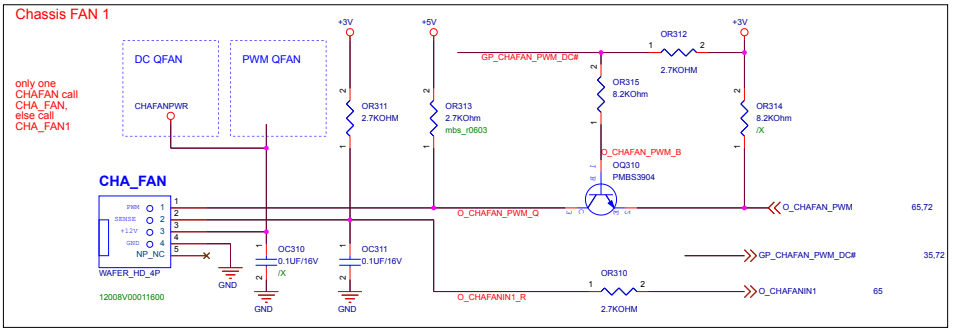
No ERP Circuit

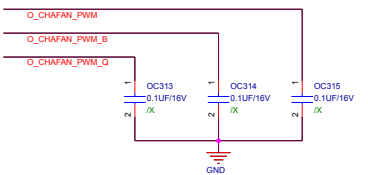



CPU FAN
PWM Mode
+3V
+5V
+12V
+3V
OR302
2.7KOHM
OR301
2.7KOHM
OR303
2.7KOhm
mbs_r0603
OR304
8.2KOhm
/X
O_CPUFAN_PWM_B
OQ300
PMBS3904
CPU_FAN
PWM
SENSE
+12V
GND
NP_NC
WAFER_HD_4P
12008V00011600
O_CPUFAN_PWM_Q
O_CPUFAN_PWM
65
OC300
0.1UF/16V
/X
OC301
0.1UF/16V
/X
GND
GND
GND
OR300
2.7KOHM
O_CPUFANIN_R
O_CPUFANIN
65

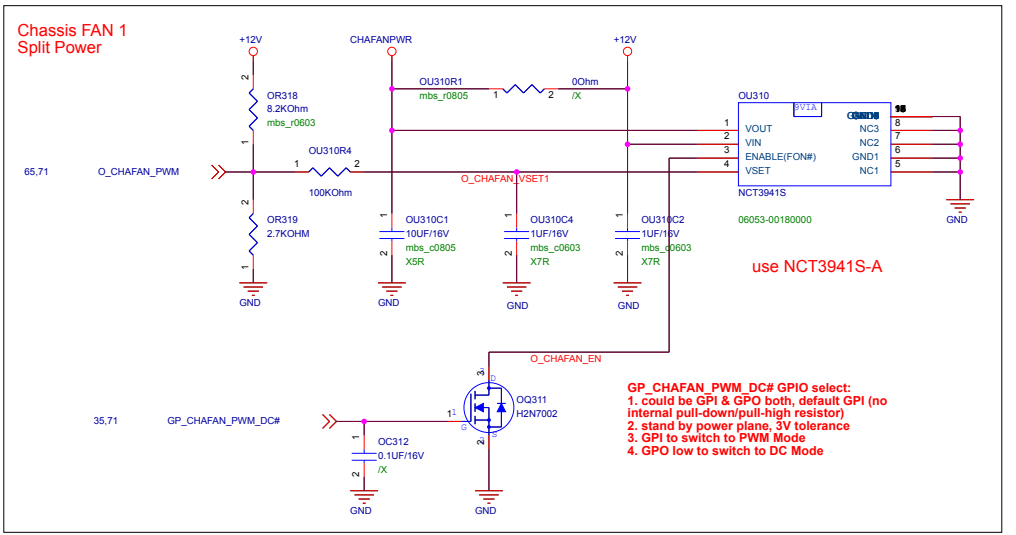

O_CPUFAN_PWM
O_CPUFAN_PWM_B
O_CPUFAN_PWM_Q
OC303
0.1UF/16V
/X
OC304
0.1UF/16V
/X
OC305
0.1UF/16V
/X
GND

4 Pin PWM Mode & DC Mode

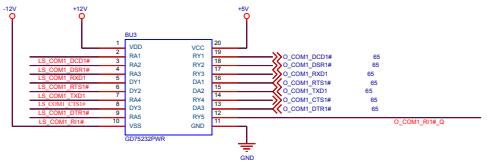


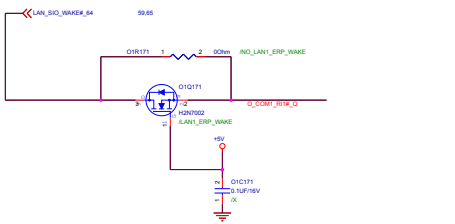


PWM Mode & DC Mode Power Solution

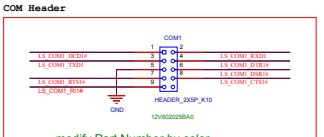


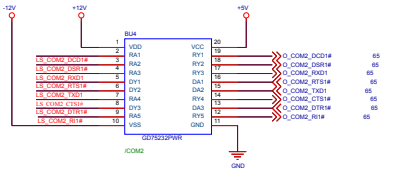
COM 1



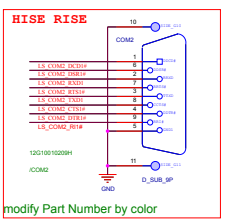


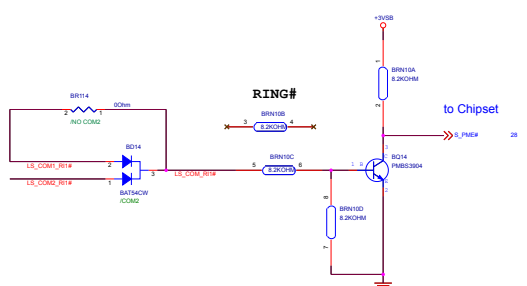
COM Header

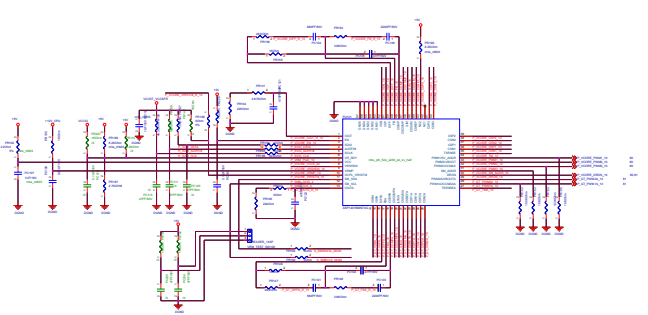


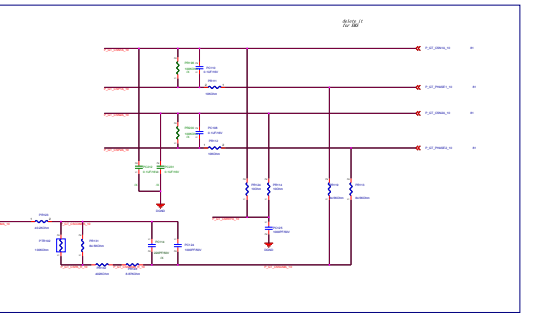


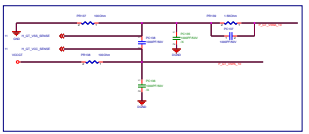
COM 2

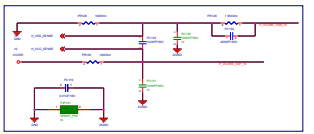


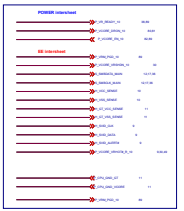


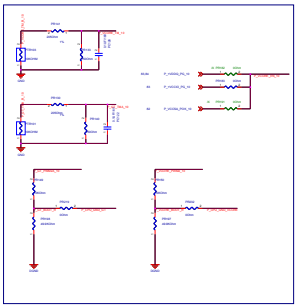


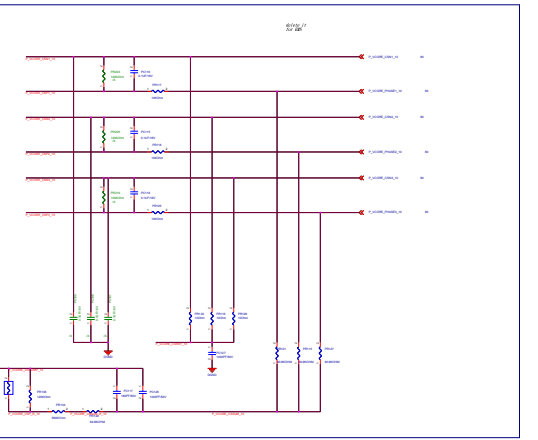


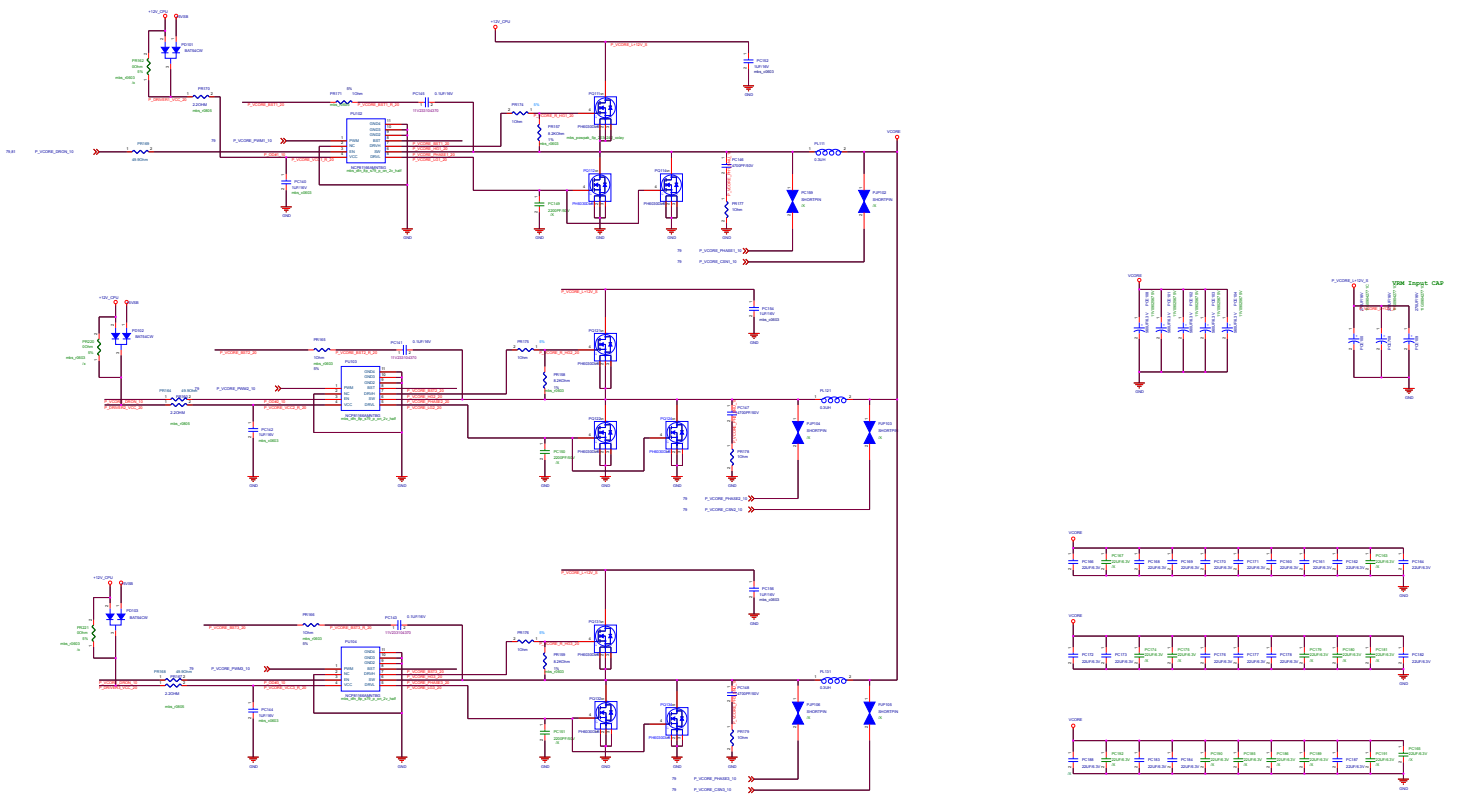


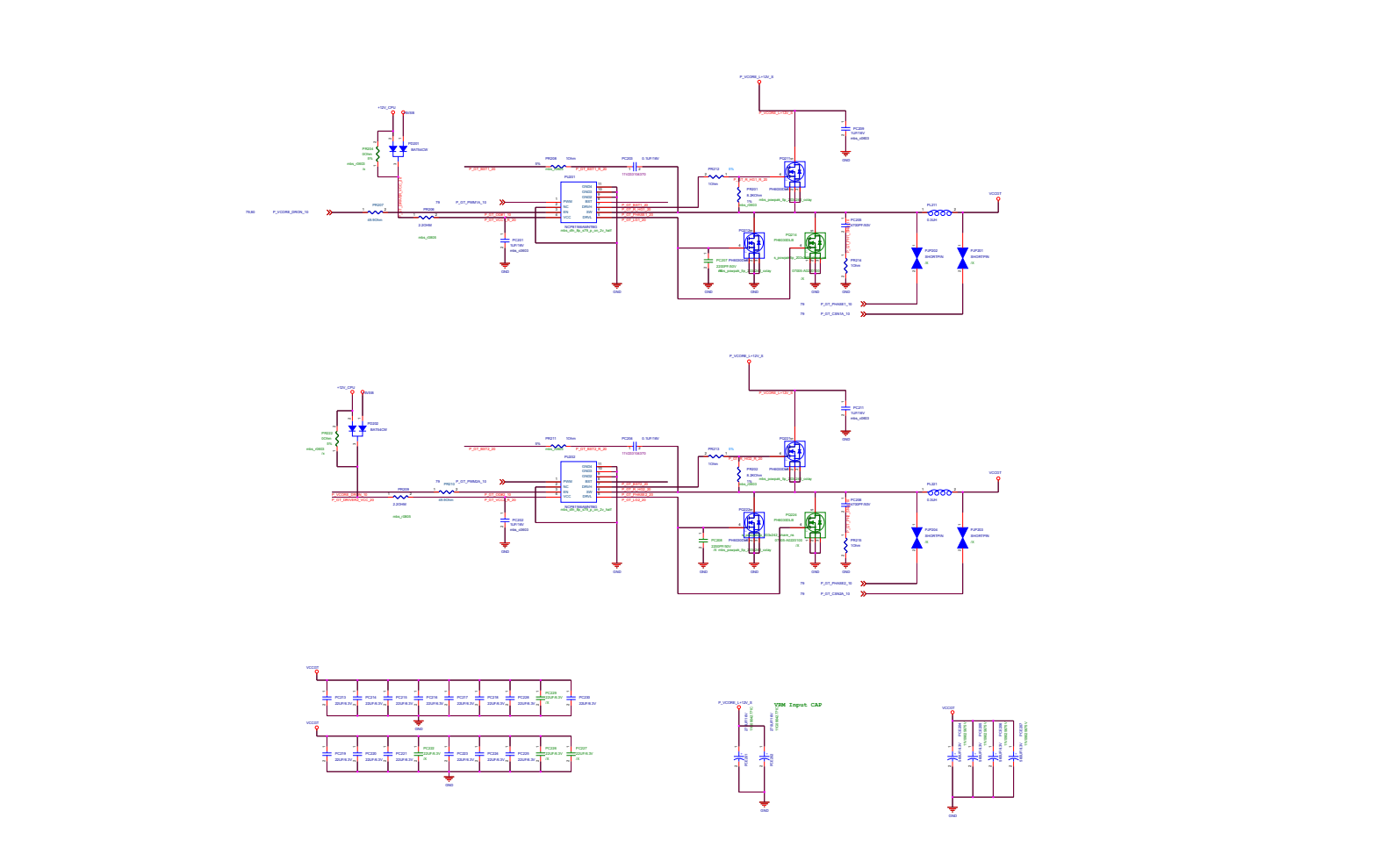


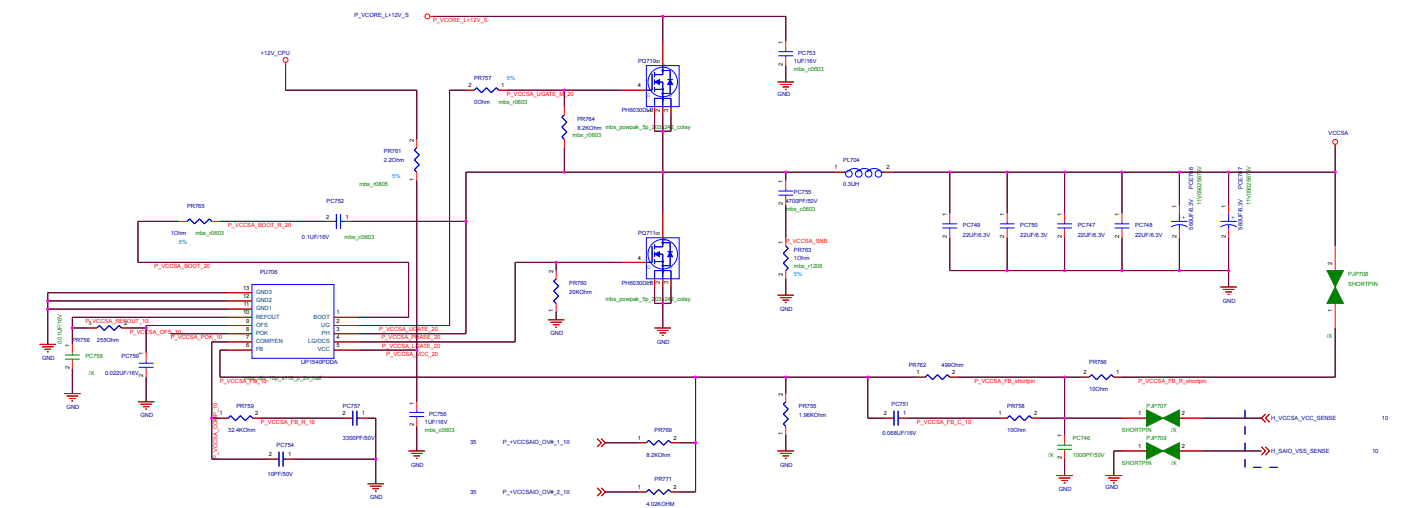

PCIE8X8 interchanel
EE interchanel





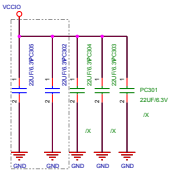

VRM Input CAP

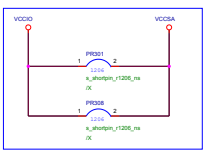

VRM Input CAP



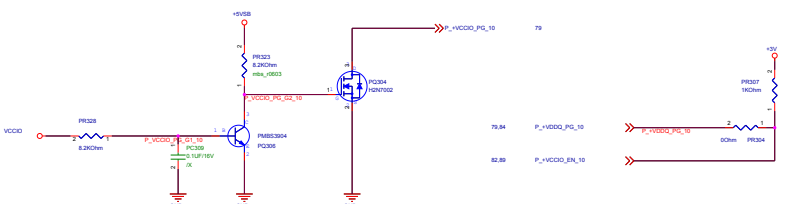
P_+VCCSAIO_OV#_1_10	P_+VCCSAIO_OV#_2_10	VCCSA
X	X	1.0V
0	X	1.05V(default)
X	0	1.1V
0	0	1.15V

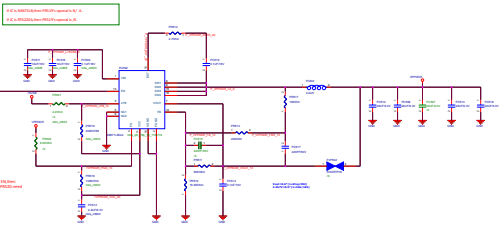
Put PC302 and PC305 MLCC inside the socket.

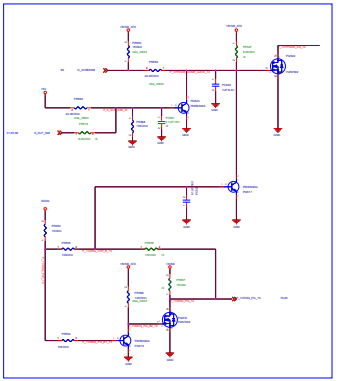


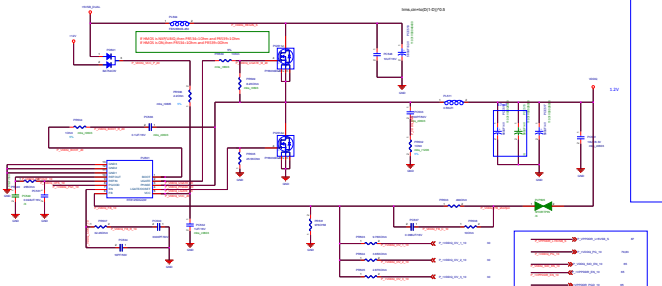


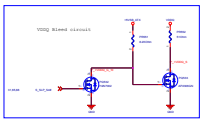
P_+VCCSAIO_OV#_1_10	P_+VCCSAIO_OV#_2_10	VCCIO
X	X	0.95V
0	1	1.0V
0	0	1.05V



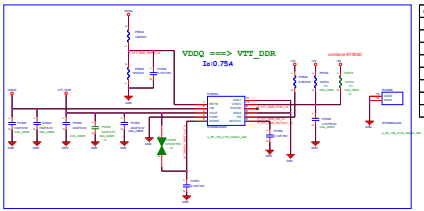


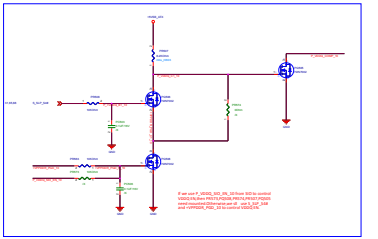


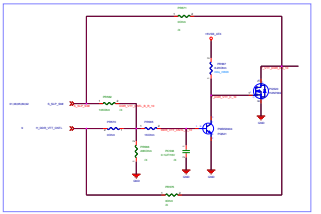


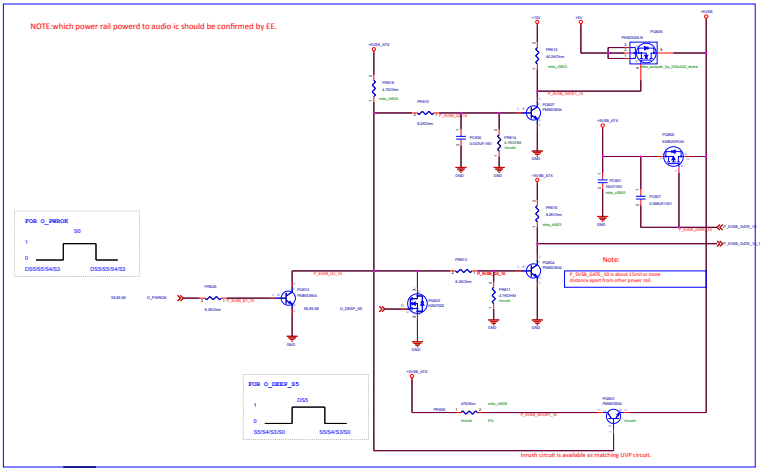


P_+VDDQ_OV_1_10	P_+VDDQ_OV_2_10	P_+VDDQ_OV_3_10	VDDQ
X	X	X	1.2V
0	X	X	1.35V
X	0	X	1.32V
X	X	0	1.28V
0	0	X	1.32V
0	X	0	1.28V
X	0	0	1.40V
0	0	0	1.0V

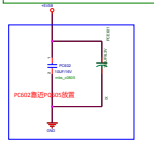


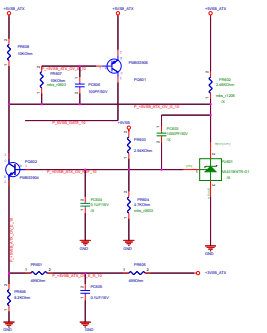


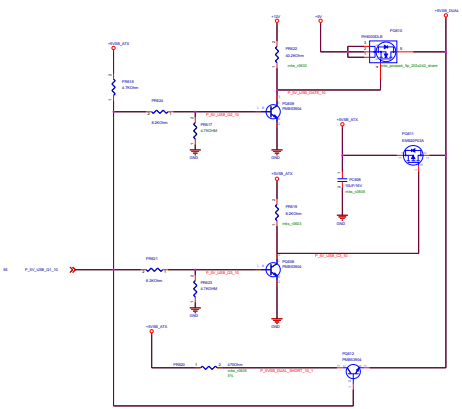


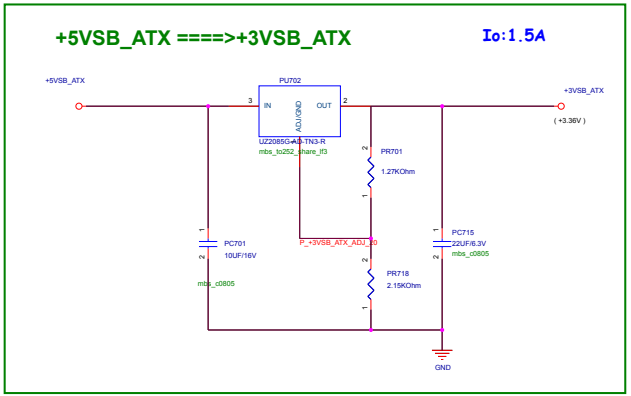

NOTE:which power rail powerd to audio ic should be confirmed by EE.
FOR O_PWROK
S0
DS5/S5/S4/S3
FOR O_DEEP_S5
DS5
S5/S4/S3/S0
Note:
P_SVSB_GATE_S0 is about 15mil or more distance apart from other power rail.
Intrush circuit is available as matching UVP circuit.

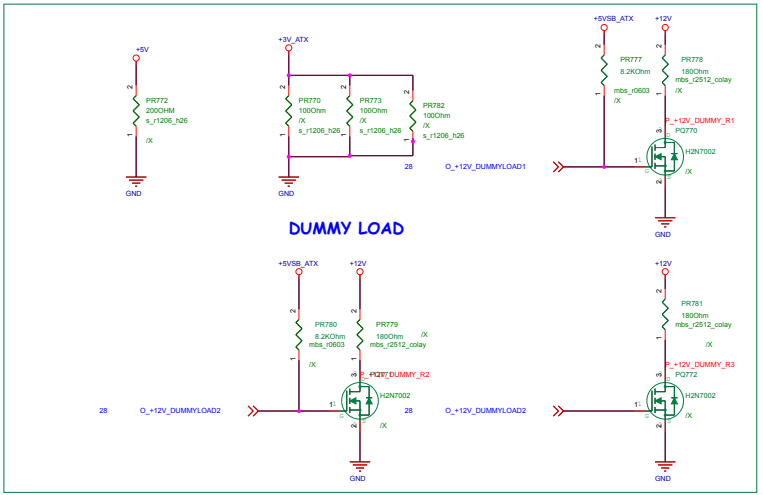

1.Vin and Vout keep more than 30mils away.
2.Input cap and Output cap can't use same GND.
3.P_SVSB_GATE_S0 is away from Vin more than 15mils ,from Vout more than 30mils.

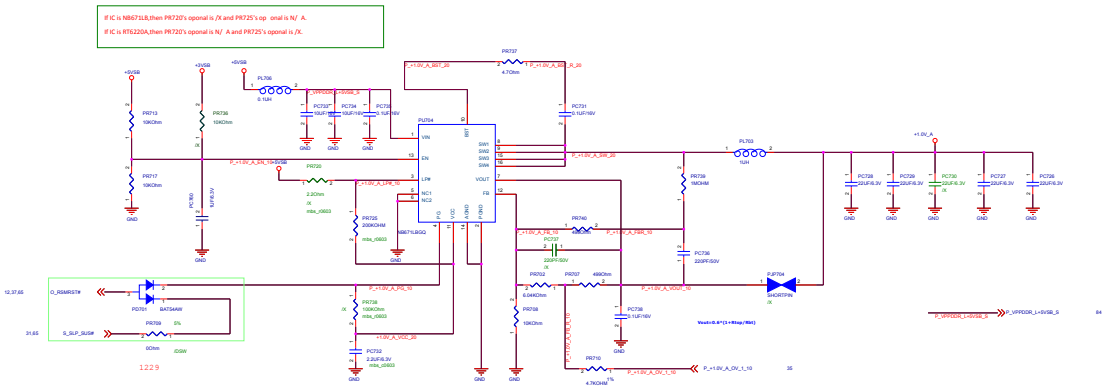

Note:
PC502靠近VIN放置



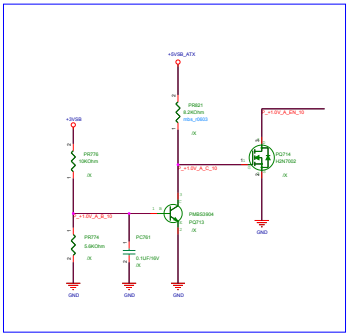


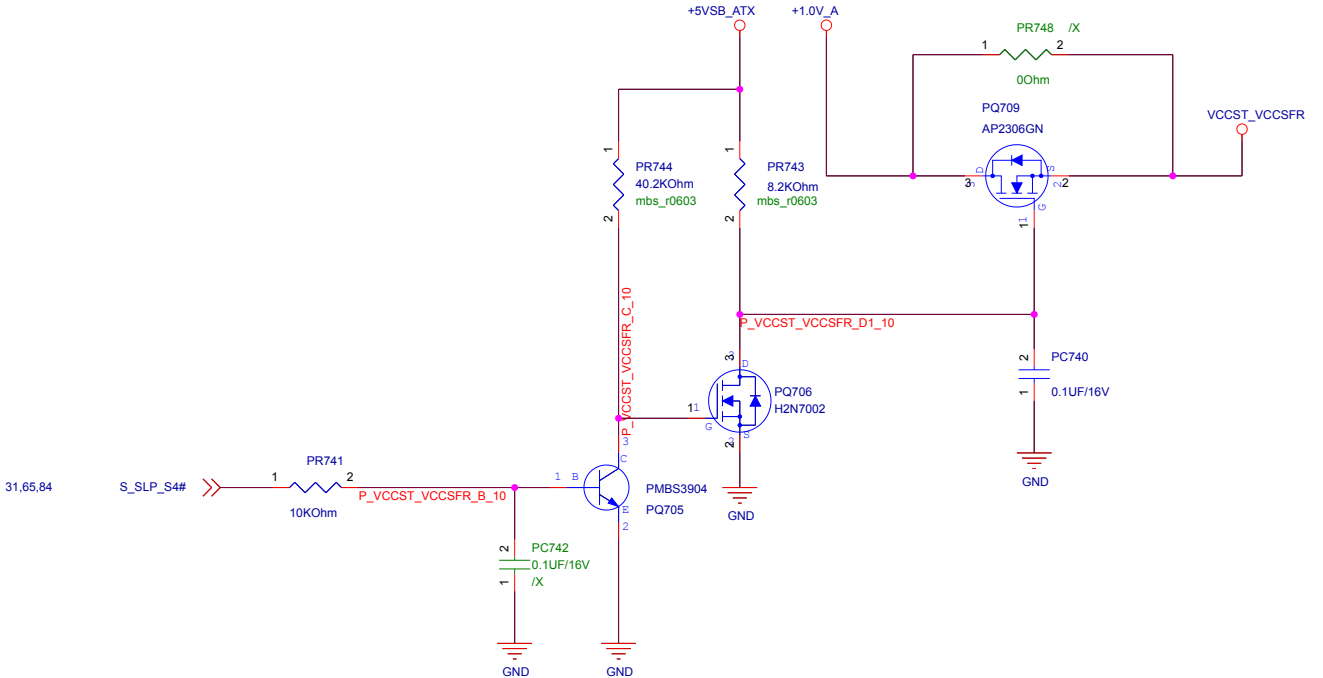

+5VSB_ATX ====>+3VSB_ATX
Io:1.5A
+5VSB_ATX
PU702
IN
OUT
ADJ/GND
3
2
UZ2085G-AB-TN3-R
mbs_to252_share_lf3
+3VSB_ATX
(+3.36V)
PR701
1.27KOhm
PC701
10UF/16V
mbs_c0805
P_+3VSB_ATX_ADJ_R0
PR718
2.15KOhm
PC715
22UF/6.3V
mbs_c0805
GND

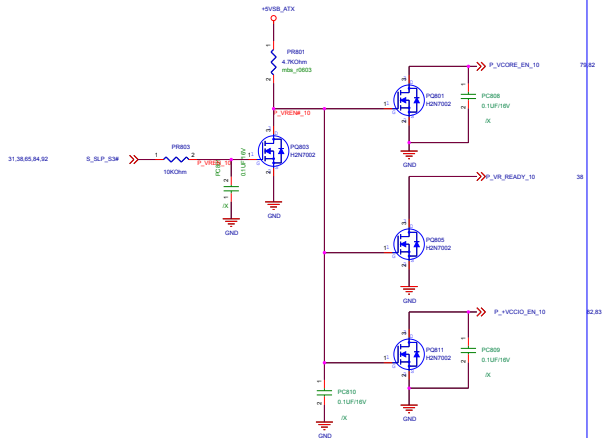

+5V
PR772
200OHM
s_r1206_h26
/X
GND
+3V_ATX
PR770
100Ohm
/X
s_r1206_h26
PR773
100Ohm
/X
s_r1206_h26
PR782
100Ohm
/X
s_r1206_h26
28
O_+12V_DUMMYLOAD1
+5VSB_ATX
+12V
PR777
8.2KOhm
mbs_r0603
/X
PR778
180Ohm
mbs_r2512_colay
/X
P_+12V_DUMMY_R1
PQ770
H2N7002
/X
GND
DUMMY LOAD
+5VSB_ATX
+12V
PR780
8.2KOhm
mbs_r0603
/X
PR779
180Ohm
mbs_r2512_colay
/X
P_+12V_DUMMY_R2
PQ771
H2N7002
/X
28
O_+12V_DUMMYLOAD2
28
O_+12V_DUMMYLOAD2
GND
+12V
PR781
180Ohm
mbs_r2512_colay
/X
P_+12V_DUMMY_R3
PQ772
H2N7002
/X
GND

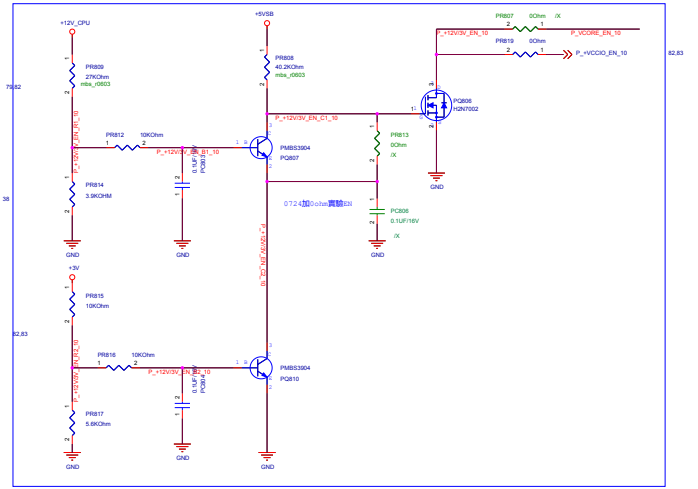


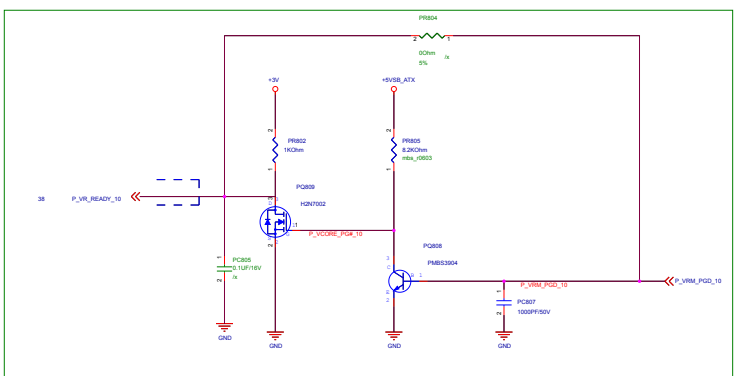
P_+1.0V_A_OV_1_10	+1.0V_A
X	1.0V
0	1.1V

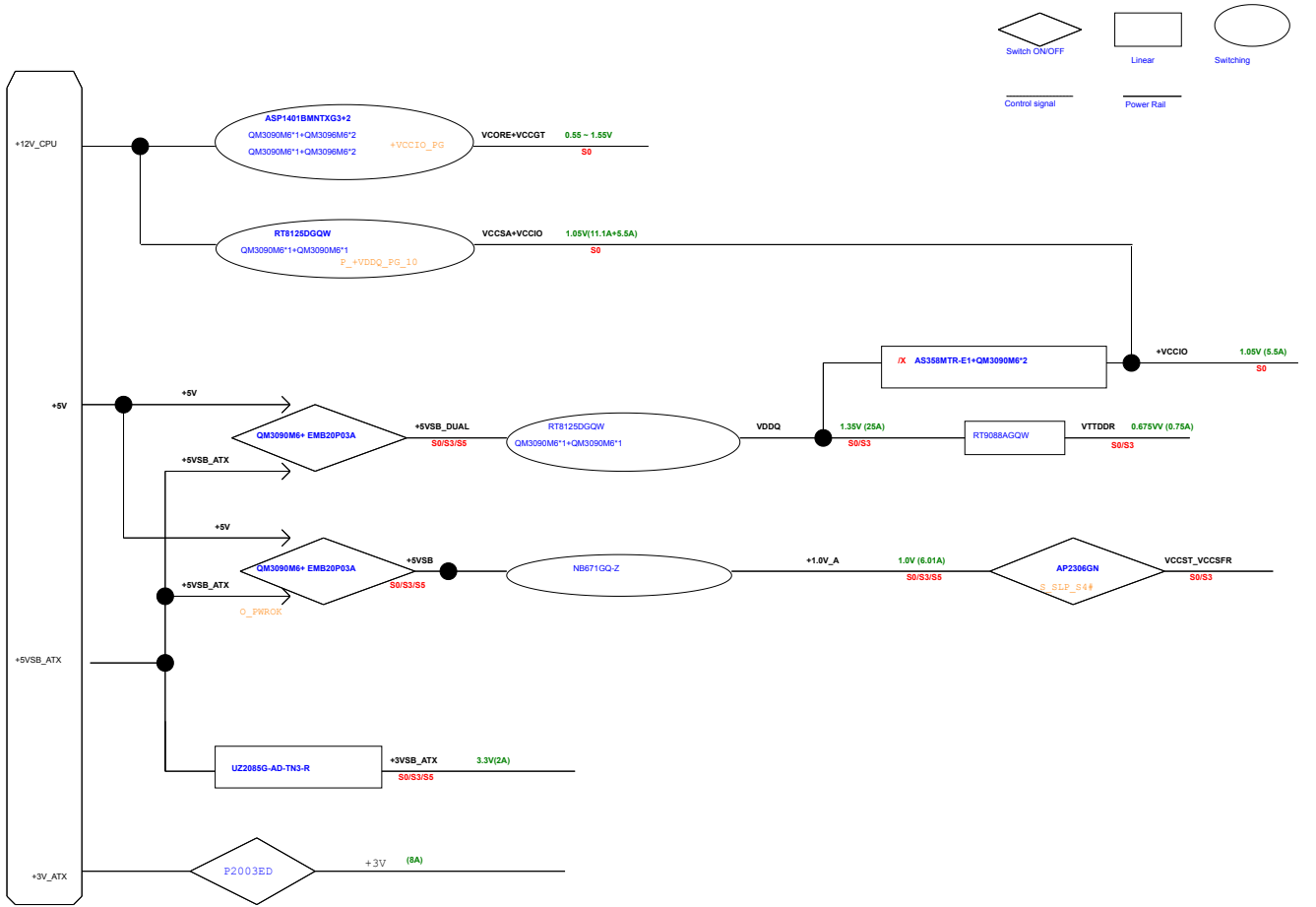


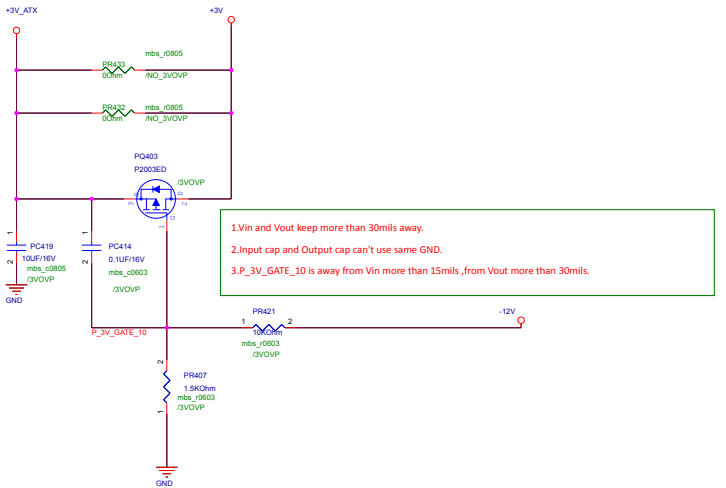

+5VSB_ATX
+1.0V_A
PR748 /X
0Ohm
PQ709
AP2306GN
VCCST_VCCSFR
PR744
40.2KOhm
mbs_r0603
PR743
8.2KOhm
mbs_r0603
P_VCCST_VCCSFR_C_10
P_VCCST_VCCSFR_D1_10
PQ706
H2N7002
PC740
0.1UF/16V
GND
31,65,84
S_SLP_S4#
PR741
10KOhm
P_VCCST_VCCSFR_B_10
PMBS3904
PQ705
PC742
0.1UF/16V
/X
GND
GND


+5VSB_ATX
PR801
4.7KOhm
mba_r0603
P_VCORE_EN_10
PQ801
H2N7002
PC808
0.1UF/16V
/X
P_VR_READY_10
PQ805
H2N7002
P_+VCCIO_EN_10
PQ811
H2N7002
PC809
0.1UF/16V
/X
PC810
0.1UF/16V
/X
GND
P_VREN#_10
PQ803
H2N7002
PR803
10KOhm
S_SLP_S3#
31,38,65,84,92
P_VREN_10
PC804
0.1UF/16V
/X
79,82
38
82,83


+12V_CPU
+5VSB
PR809
27KOhm
mba_r0603
PR808
40.2KOhm
mba_r0603
PR807
0Ohm
/X
P_+12V3V_EN_10
P_VCORE_EN_10
PR819
0Ohm
P_+VCCIO_EN_10
82,83
P_+12V3V_EN_R1_10
PR812
10KOhm
P_+12V3V_EN_B1_10
PQ807
PMBS3904
P_+12V3V_EN_C1_10
PQ806
H2N7002
PR813
0Ohm
/X
PR814
3.9KOHM
PC807
0.1UF/16V
PC805
0.1UF/16V
/X
GND
+3V
PR815
10KOhm
P_+3V_EN_R2_10
PR816
10KOhm
P_+12V3V_EN_B2_10
PQ810
PMBS3904
PR817
5.6KOhm
PC806
0.1UF/16V
/X


PR804
0Ohm
5%
/X
+3V
+5VSB_ATX
PR802
1KOhm
PR805
8.2KOhm
mba_r0603
38
P_VR_READY_10
PC809
H2N7002
P_VCORE_PG#_10
PC805
0.1UF/16V
/X
PC808
PMBS3904
P_VRM_PGD_10
PC807
1000PF/50V
79
GND


Switch ON/OFF
Linear
Switching
Control signal
Power Rail
+12V_CPU
ASP1401BMNTXG3+2
QM3090M6*1+QM3096M6*2
QM3090M6*1+QM3096M6*2
+VCCIO_PG
VCORE+VCCGT
0.55 ~ 1.55V
S0
RT8125DGQW
QM3090M6*1+QM3090M6*1
P_+VDDQ_PG_10
VCCSA+VCCIO
1.05V(11.1A+5.5A)
S0
+5V
+5V
QM3090M6+ EMB20P03A
+5VSB_DUAL
S0/S3/S5
RT8125DGQW
QM3090M6*1+QM3090M6*1
VDDQ
1.35V (25A)
S0/S3
RT9088AGQW
VTTDDR
0.675VV (0.75A)
S0/S3
/X AS358MTR-E1+QM3090M6*2
+VCCIO
1.05V (5.5A)
S0
+5VSB_ATX
+5V
QM3090M6+ EMB20P03A
+5VSB
S0/S3/S5
+5VSB_ATX
O_PWROK
NB671GQ-Z
+1.0V_A
1.0V (6.01A)
S0/S3/S5
AP2306GN
S_SLP_S4#
VCCST_VCCSFR
S0/S3
+5VSB_ATX
UZ2085G-AD-TN3-R
+3VSB_ATX
3.3V(2A)
S0/S3/S5
+3V_ATX
P2003ED
+3V
(8A)

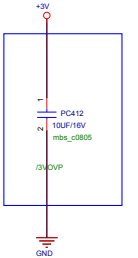


1.Vin and Vout keep more than 30mils away.

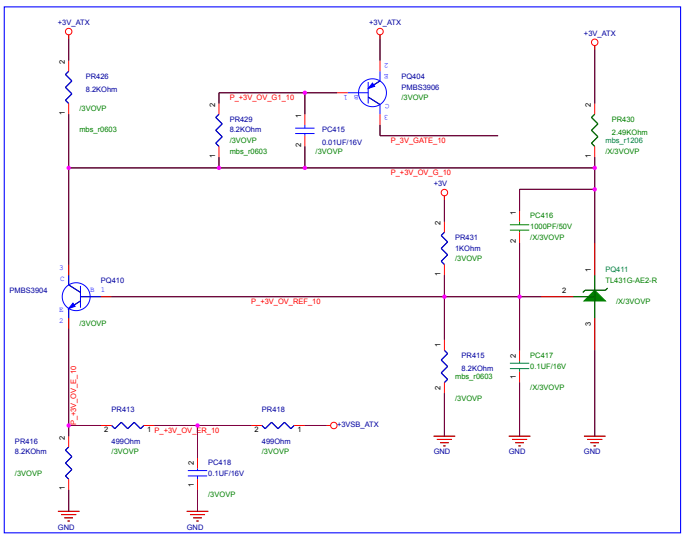
2.Input cap and Output cap can't use same GND.

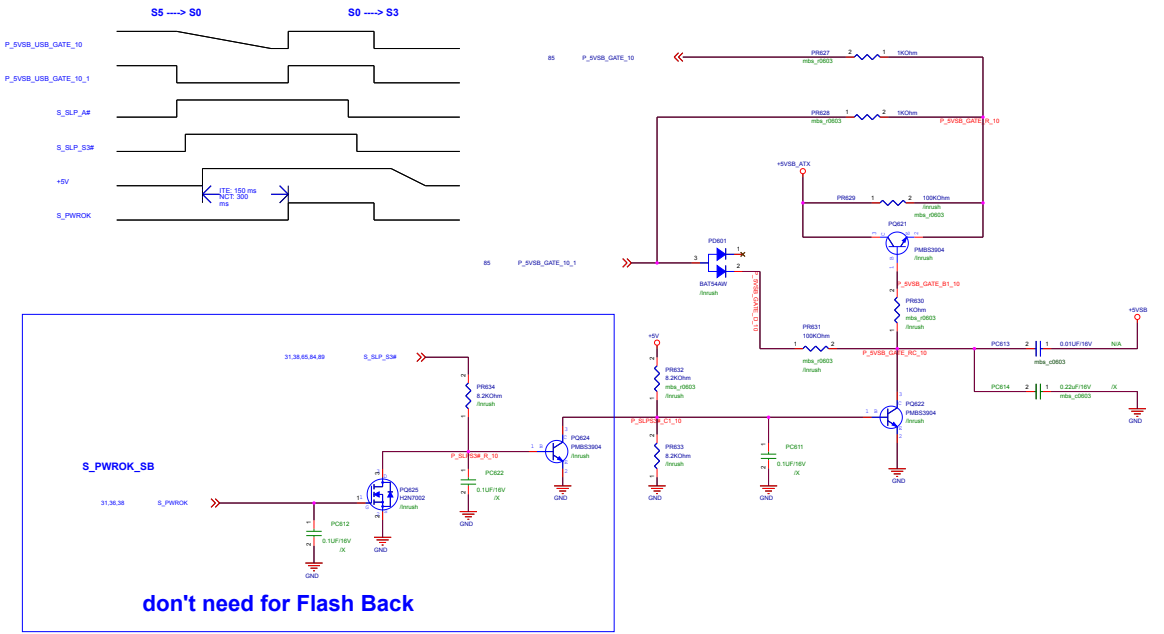
3.P_3V_GATE_10 is away from Vin more than 15mils ,from Vout more than 30mils.

PC412靠近PQ403放置



PQ404,PQ410 and other components are be er to place close to PQ403.



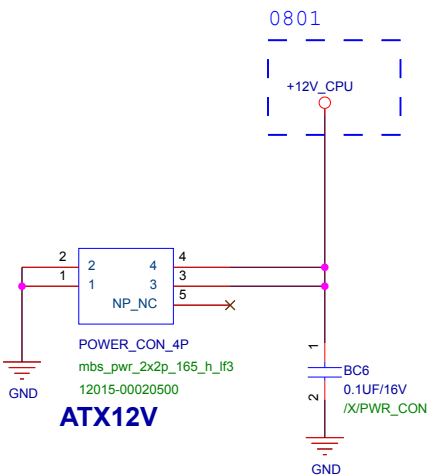


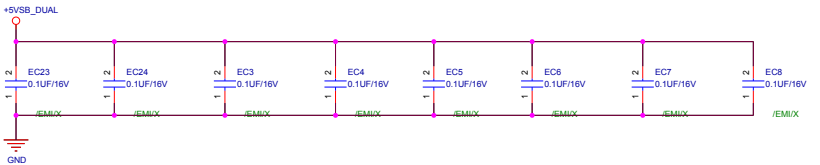
Inrush Circuit for USB Port default have Power or Flash Back Function

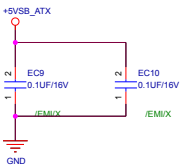
4 Pin +12V Connector

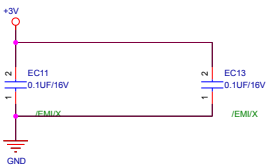
顏色: CHL

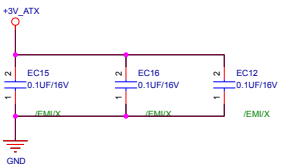
Z97 : 12015-00053200

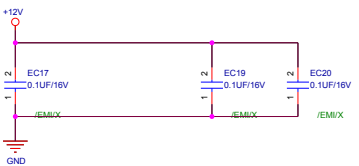


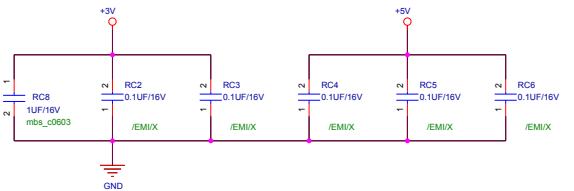

+5VSB_DUAL
EC23
0.1UF/16V
EC24
0.1UF/16V
EC3
0.1UF/16V
EC4
0.1UF/16V
EC5
0.1UF/16V
EC6
0.1UF/16V
EC7
0.1UF/16V
EC8
0.1UF/16V
/EMI/X
GND


+5VSB_ATX
EC9
0.1UF/16V
EC10
0.1UF/16V
/EMI/X
GND


+3V
EC11
0.1UF/16V
EC13
0.1UF/16V
/EMI/X
GND


+3V_ATX
EC15
0.1UF/16V
EC16
0.1UF/16V
EC12
0.1UF/16V
/EMI/X
GND


+12V
EC17
0.1UF/16V
EC19
0.1UF/16V
EC20
0.1UF/16V
/EMI/X
GND


+3V
RC8
1UF/16V
mbs_c0603
RC2
0.1UF/16V
RC3
0.1UF/16V
+5V
RC4
0.1UF/16V
RC5
0.1UF/16V
RC6
0.1UF/16V
/EMI/X
GND