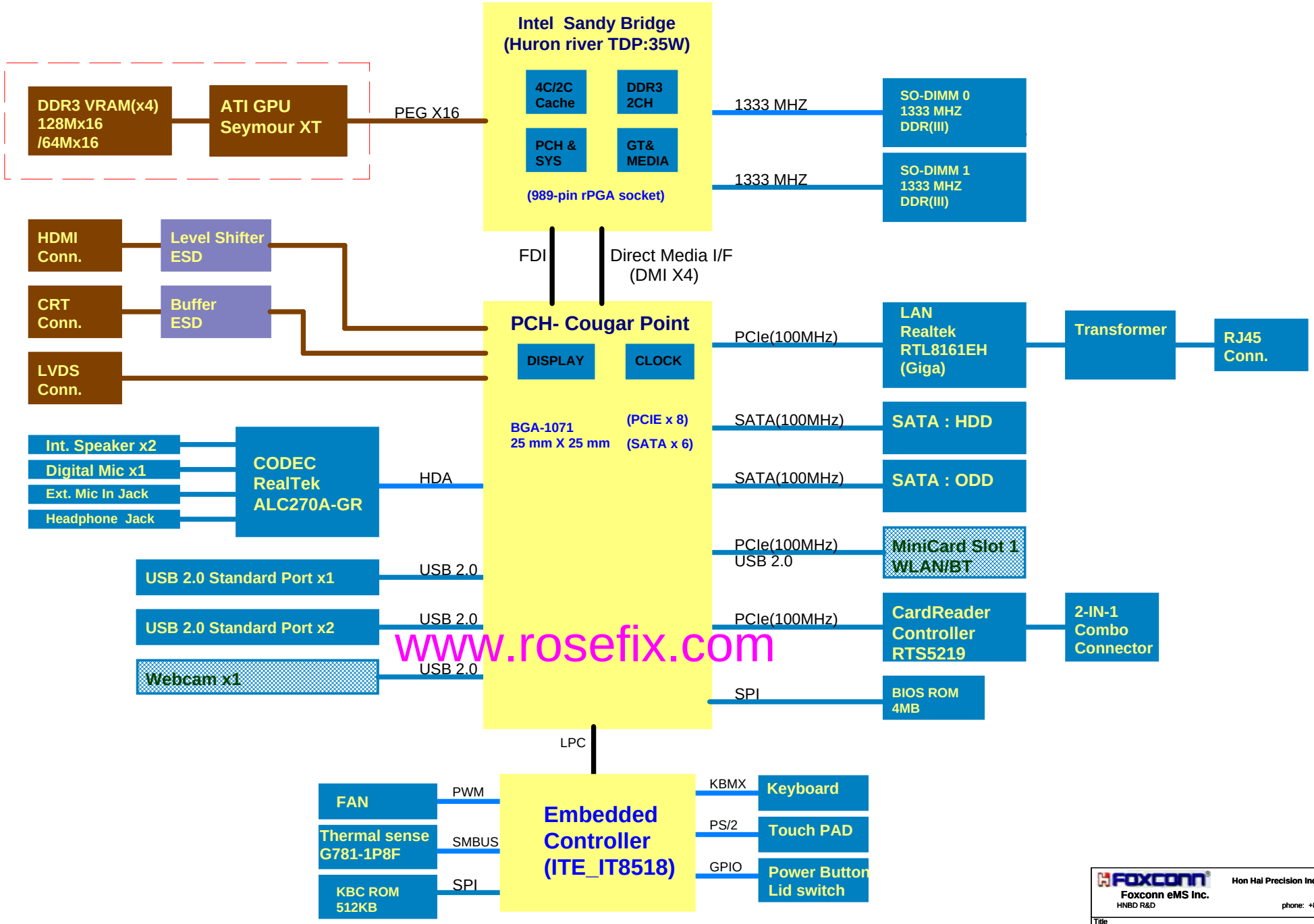

www.rosefix.com

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Title: SYSTEM BLOCK DIAGRAM

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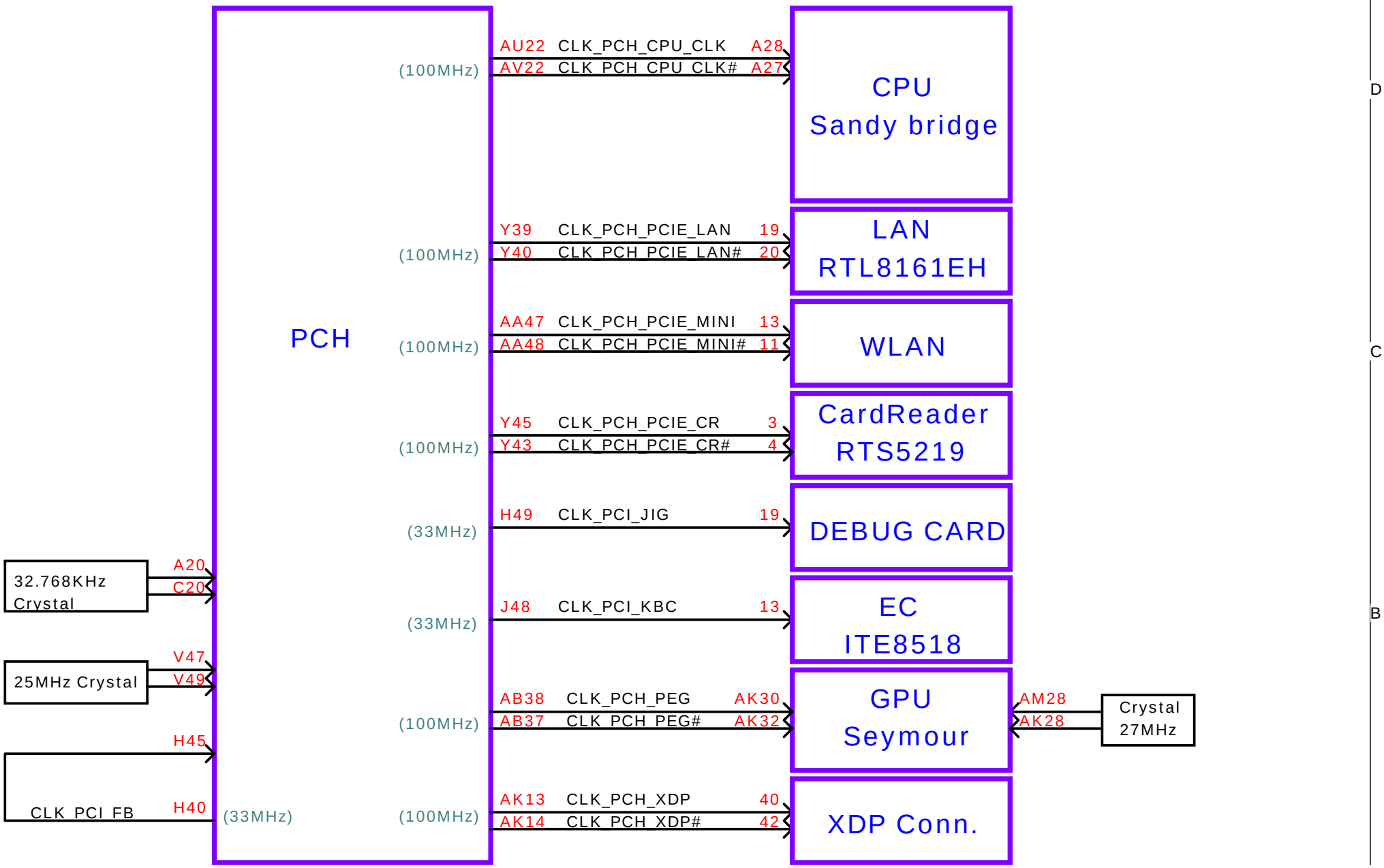
Page Modified: Tuesday, March 08, 2011 08:29:00 (UTC/GMT) | Sheet 2 of 43



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Title: CLOCK MAP

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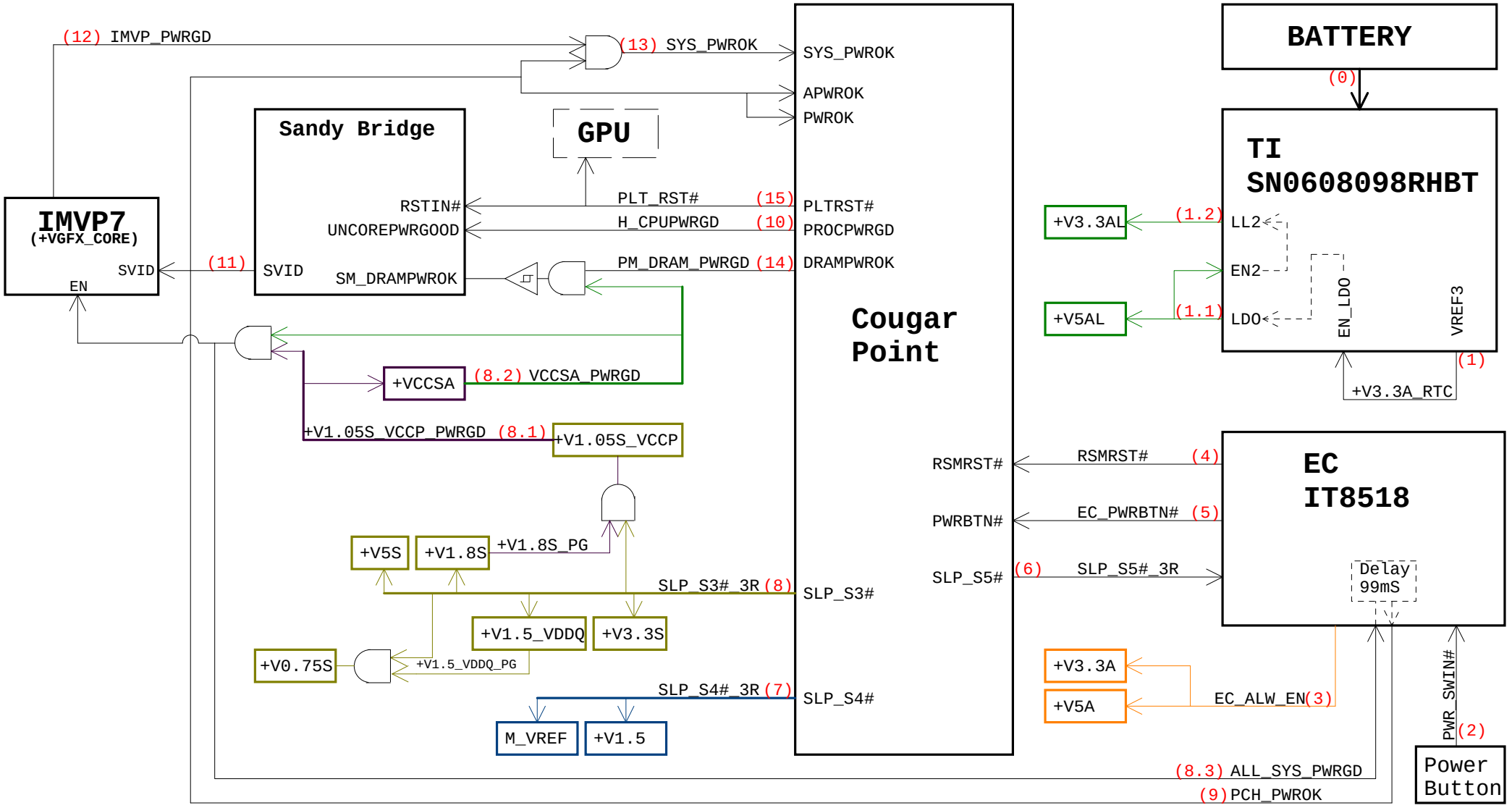

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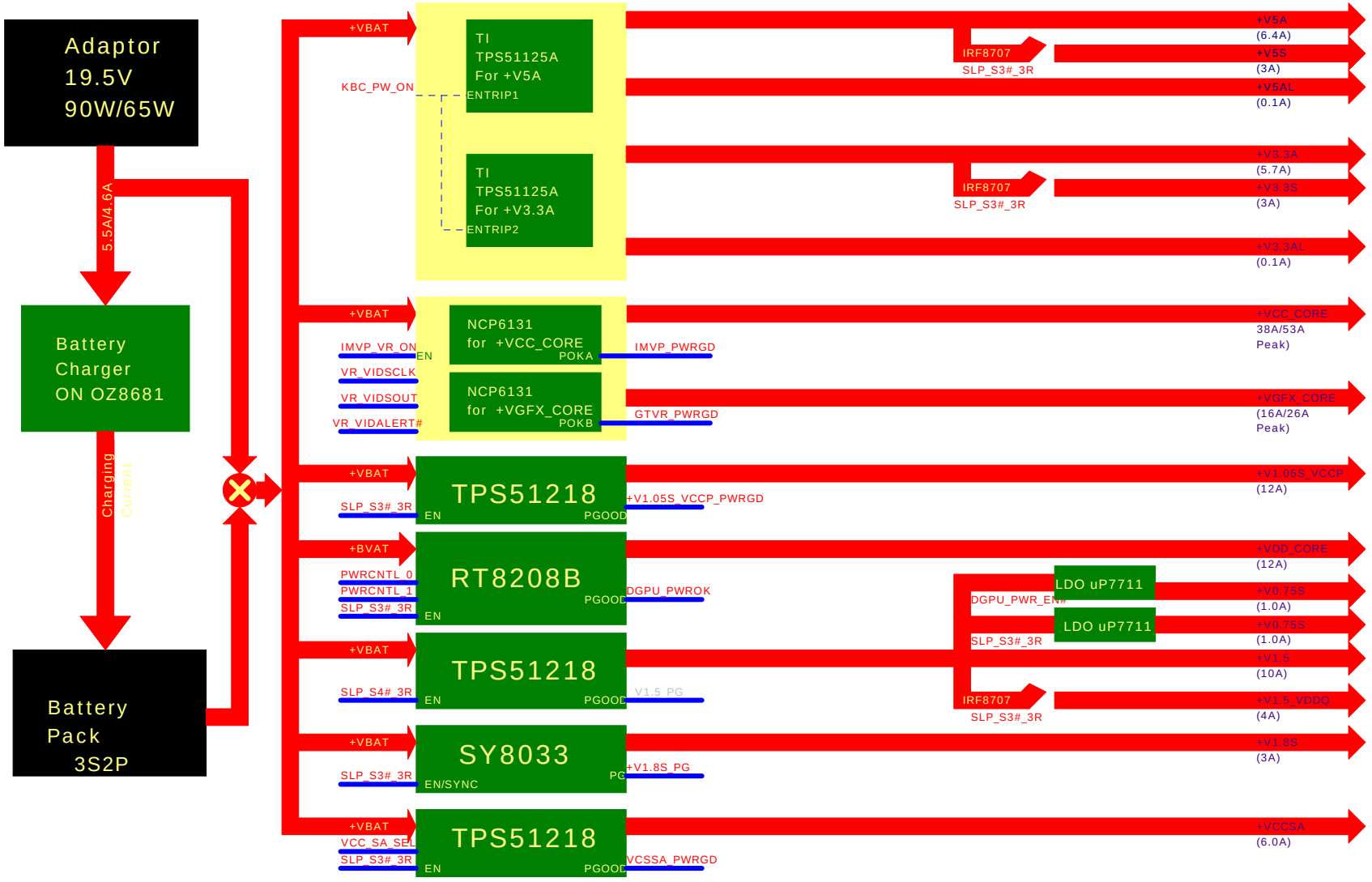
Title	POWER SEQUENCY DIAGRAM
Size / Document Number	Custom / CHICAGO
Rev	MV
Page Modified: Tuesday, March 08, 2011 08:28:00 (UTC/GMT)	Sheet 4 of 43

POWER MAP



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Title		
POWER MAP		
Size: C	Document Number: CHICAGO	Rev: MV
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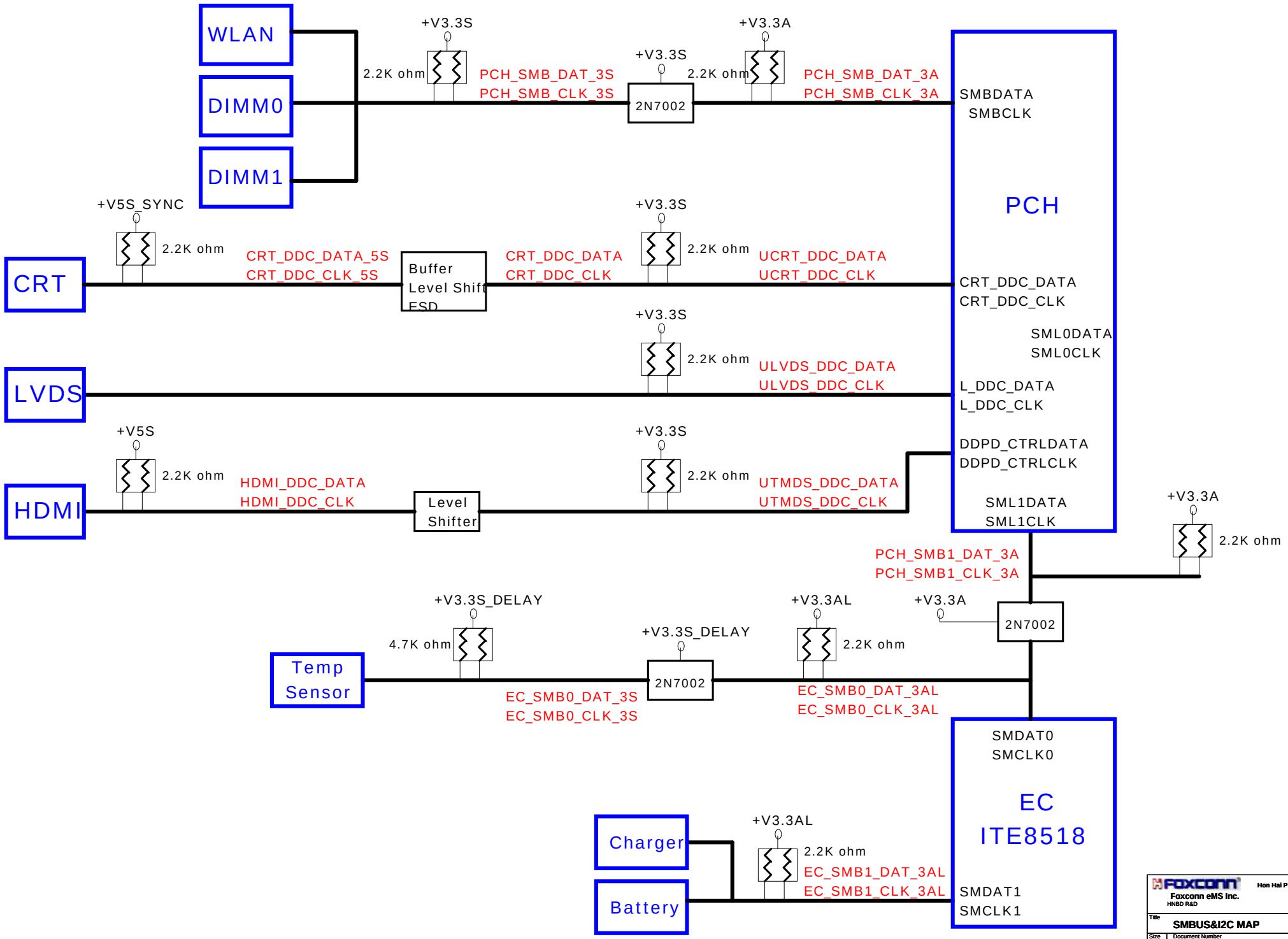

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Title: SMBUS&I2C MAP

Size: Custom | Document Number: CHICAGO | Rev: MV

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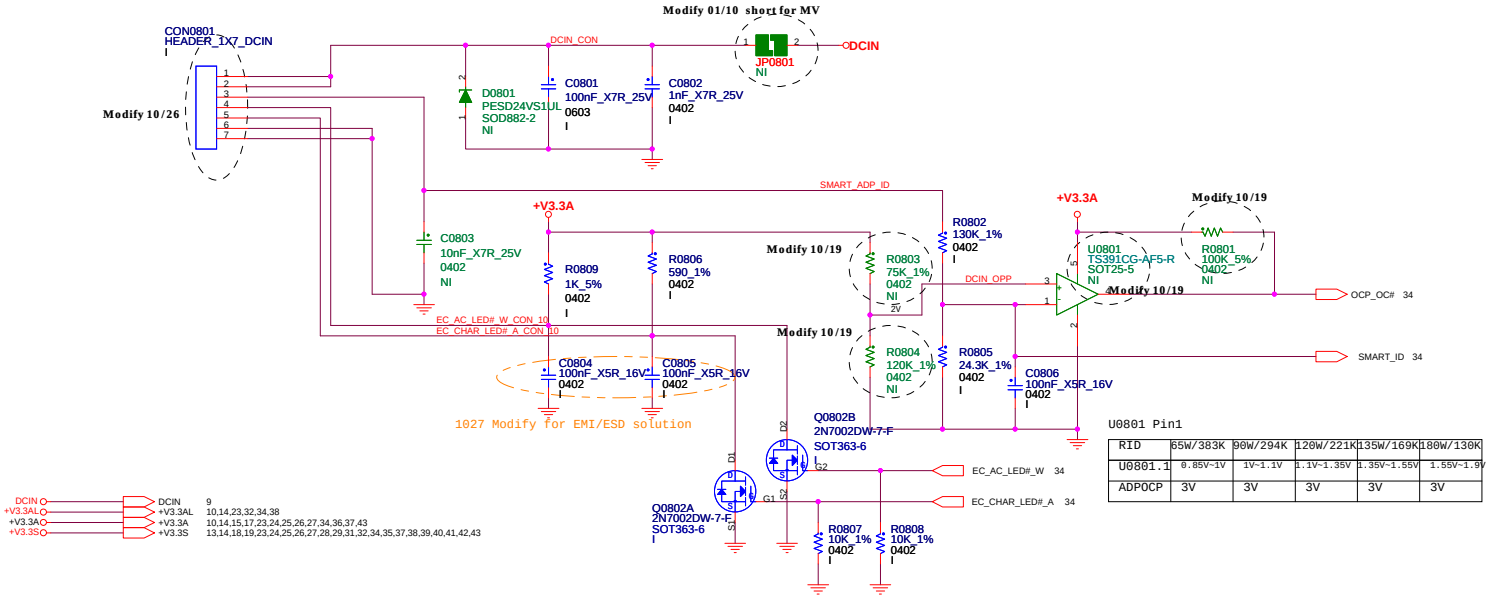
Size: A	Document Number: CHICAGO — Rev: MV
Page Modified: Tuesday, March 08, 2011 08:28:58 (UTC/GMT)	Sheet 7 of 43

DC_JACK WIRE to BOARD CONNECTOR

2010.1203.0

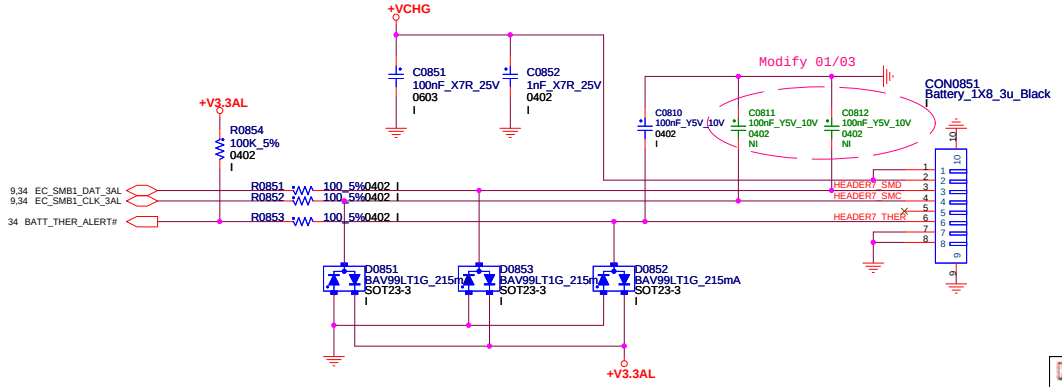


U0801 Pin1

RID	65W/383K	90W/294K	120W/221K	135W/169K	180W/130K
U0801.1	0.85V~1V	1V~1.1V	1.1V~1.35V	1.35V~1.55V	1.55V~1.9V
ADPOCP	3V	3V	3V	3V	3V

BATTERY CONNECTOR

2010.0914.0



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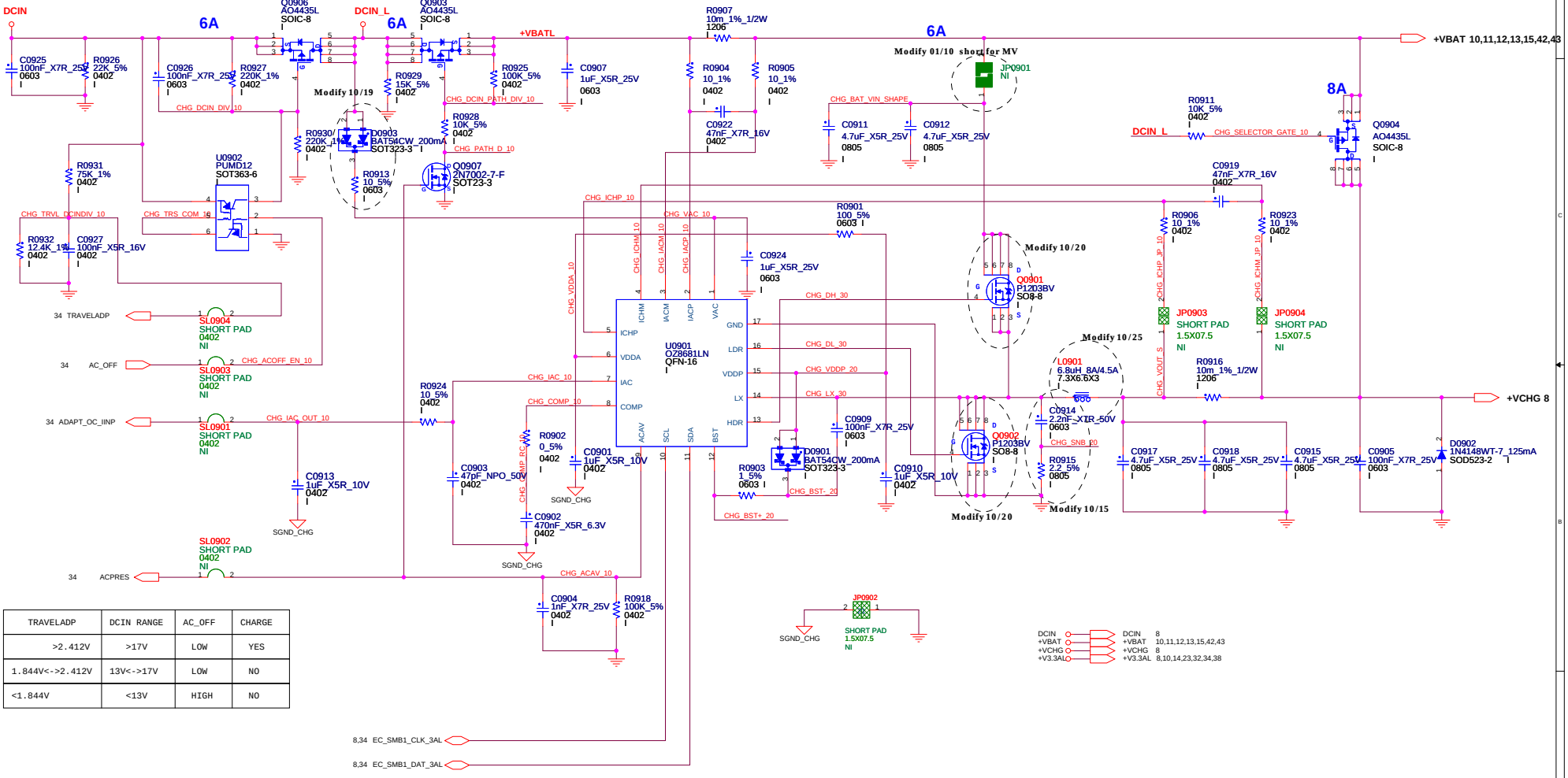
Title: DCIN/BATTERY			
Size	Document Number: CHICAGO		Rev: MV
Page Modified: Tuesday, March 08, 2011 08:29:09 (UTC/GMT)		Sheet 8	of 43

BATTERY CHARGER



TRAVELADP	DCIN RANGE	AC_OFF	CHARGE
>2.412V	>17V	LOW	YES
1.844V<->2.412V	13V<->17V	LOW	NO
<1.844V	<13V	HIGH	NO

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Page Modified: Tuesday, March 08, 2011 08:28:58 (UTC/GMT) | Sheet 9 of 43

+V5A / +V3.3A POWER SUPPLY

2010.1103.0

+V5A:	+V3.3A:
1. I/P Current:	1.I/P Current:
Iin=Vo*Io/(0.75*Vin)=3.7A	Iin=Vo*Io/(0.75*Vin)=2.2A
2. Ripple Current:	2.Ripple Current:
Irip=3.72A	Irip=2.21A
3. Ripple Voltage:	3.Ripple Voltage:
ESR/1=15mohm Vrip=55.8mV	ESR/1=15mohm Vrip=33.15mV
4. Inductor Spec:	4.Inductor Spec:
Isat=13.5A Idc=6A DCR=30mohm	Isat=13.5A Idc=6A DCR=30mohm
5.MOSFET Spec:	
H-side MOSFET: IRF8707PBF Rds(ON)=17.5mohm (Vgs=4.5 V) I cont = 11A (T =25 ℃) I peak = 88A (Pause =10 us)	L-side MOSFET: IRF8707PBF Rds(ON)=17.5mohm (Vgs=4.5 V) I cont = 11A (T =25 ℃) I peak = 88A (Pause =10 us)
6. Frequency:	6. Frequency:
F=300KHz	F=375KHz
7. OCP:	7. OCP:
Set = R1002 to 100K Vtrip= (R1002*10uA/9)-24mV=0.0655V Iocp=Vtrip/Rdson + Iripple/2 = 6.4A	Set = R1003 to 100K Vtrip= (R1003*10uA/9)-24mV=0.0655V Iocp=Vtrip/Rdson + Iripple/2 = 5.7A

Imax=4.5A
OCP=5.7A

Imax=5A
OCP=6.4A

U1001 TPS51123RGER QFN-24

1027 Modify for EMI/ESD solution
Size change from 0402 to 0603

DCIN	DCIN	8,9
+V12A	+V12A	14
+VBAT	+VBAT	9,11,12,13,15,42,43
+V3.3AL	+V3.3AL	8,14,23,32,34,38
+V5AL	+V5AL	14,32
+V3.3S	+V3.3S	13,14,18,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V5S	+V5S	12,14,23,27,32,35,36,38,39,41,42,43

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Title: 5V/3.3V	
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Rev: MV	
Page Modified: Tuesday, March 08, 2011 08:28:59 (UTC/GMT)	Sheet 10 of 43

+VTT POWER SUPPLY

2010.1103.0

+V1.05S_VCCP:

1. I/P Current:

Iin=Vo*Io/(0.75*Vin)=1.24A

2. Ripple Current:

Irip=3.42A

3. Ripple Voltage:

ESR/1=9mohm
Vrip=30.78mV

4. Inductor Spec:

Isat=36A
Idc=18A
DCR=3.3mohm

5.MOSFET Spec:

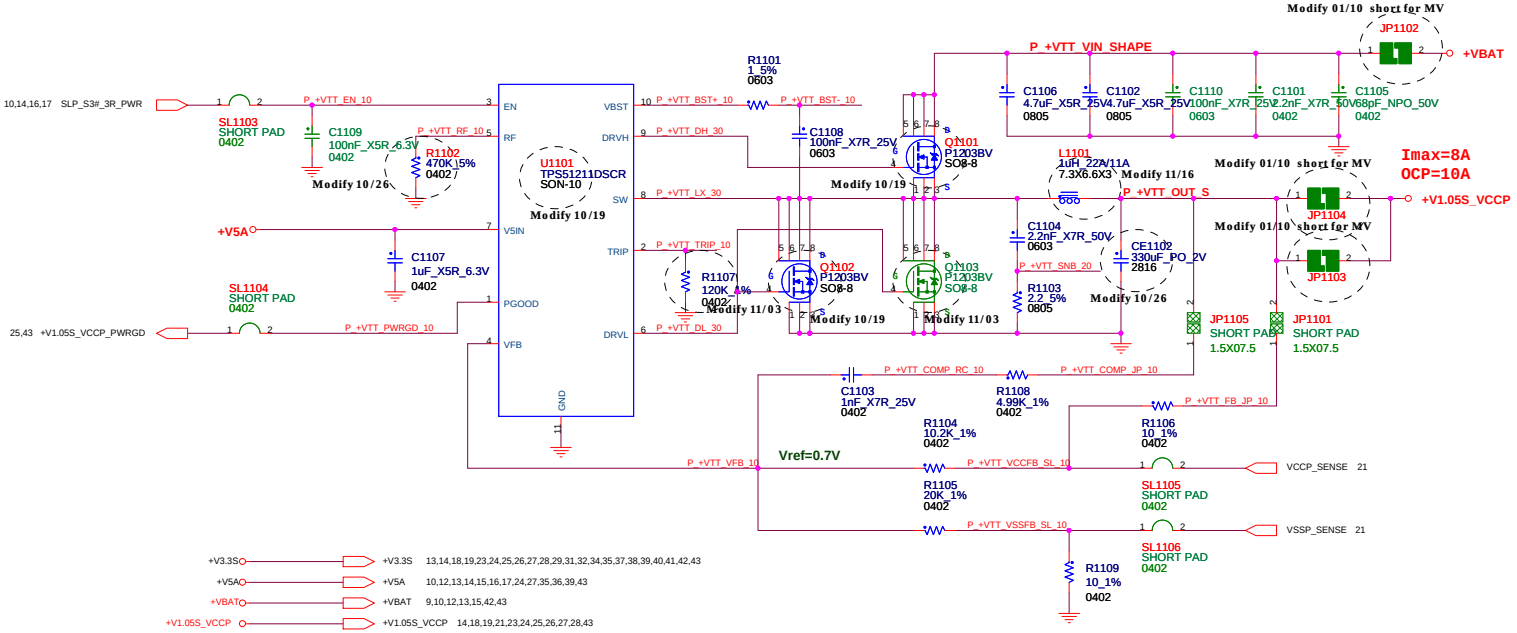
H-side MOSFET: IRF8707PBF	L-side MOSFET: IRF8707PBF
Rds(ON)=17.5mohm (Vgs=4.5 V)	Rds(ON)=17.5mohm (Vgs=4.5 V)
I cont = 11A (T =25 ℃)	I cont = 11A (T =25 ℃)
I peak = 88A (Pause =10 us)	I peak = 88A (Pause =10 us)

6. Frequency:

F=290KHz (R1102=0ohm)

7. OCP:

Set = R1107 to 120K
Vtrip= R1107*10uA=1.2V
Iocp=(Vtrip/8*Rdson) + Iripple/2 = 10A



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Rev: MV	
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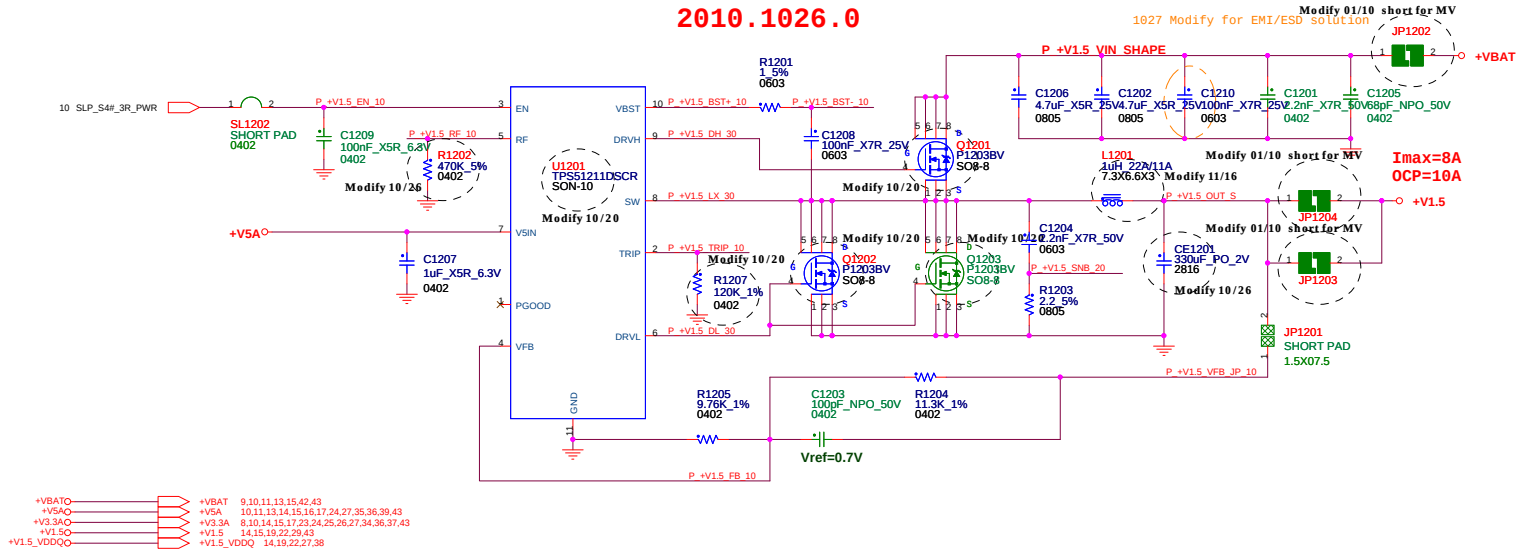
+V1.5 POWER SUPPLY

2010.1026.0



+V1.5:

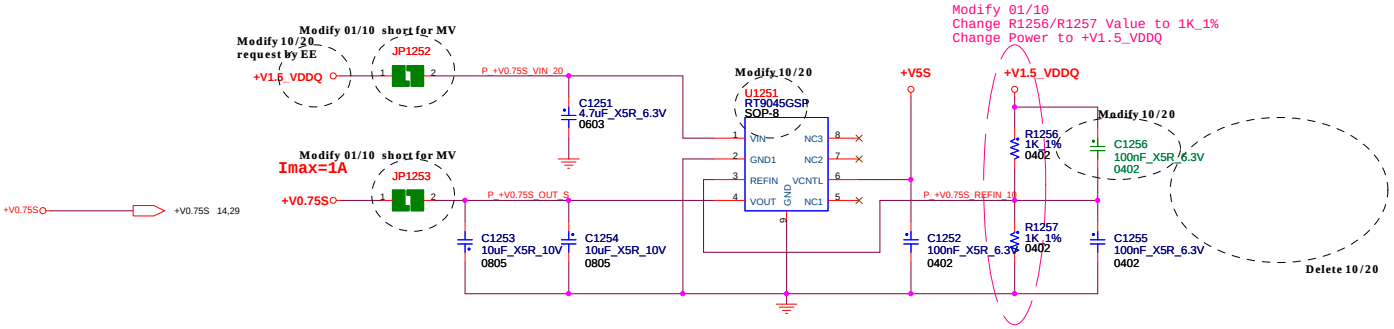
1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=1.78A
2. Ripple Current:
   Irip=3.34A
3. Ripple Voltage:
   ESR/1=9mohm
   Vrip=30.6mV
4. Inductor Spec:
   Isat=36A
   Idc=18A
   DCR=3.3mohm
5. MOSFET Spec:

H-side MOSFET: IRF8707PBF	L-side MOSFET: IRF8707PBF
Rds(ON)=17.5mohm (Vgs=4.5 V)	Rds(ON)=17.5mohm (Vgs=4.5 V)
I cont = 11A (T =25 ℃)	I cont = 11A (T =25 ℃)
I peak = 88A (Pause =10 us)	I peak = 88A (Pause =10 us)

6. Frequency:
   F=290KHz (R0902=0ohm)
7. OCP:
   Set = R1207 to 120K
   Vtrip= R1207*10uA=1.2V
   Iocp=(Vtrip/8*Rdson) + Iripple/2 = 10A

+V0.75S POWER SUPPLY

2010.1026.0



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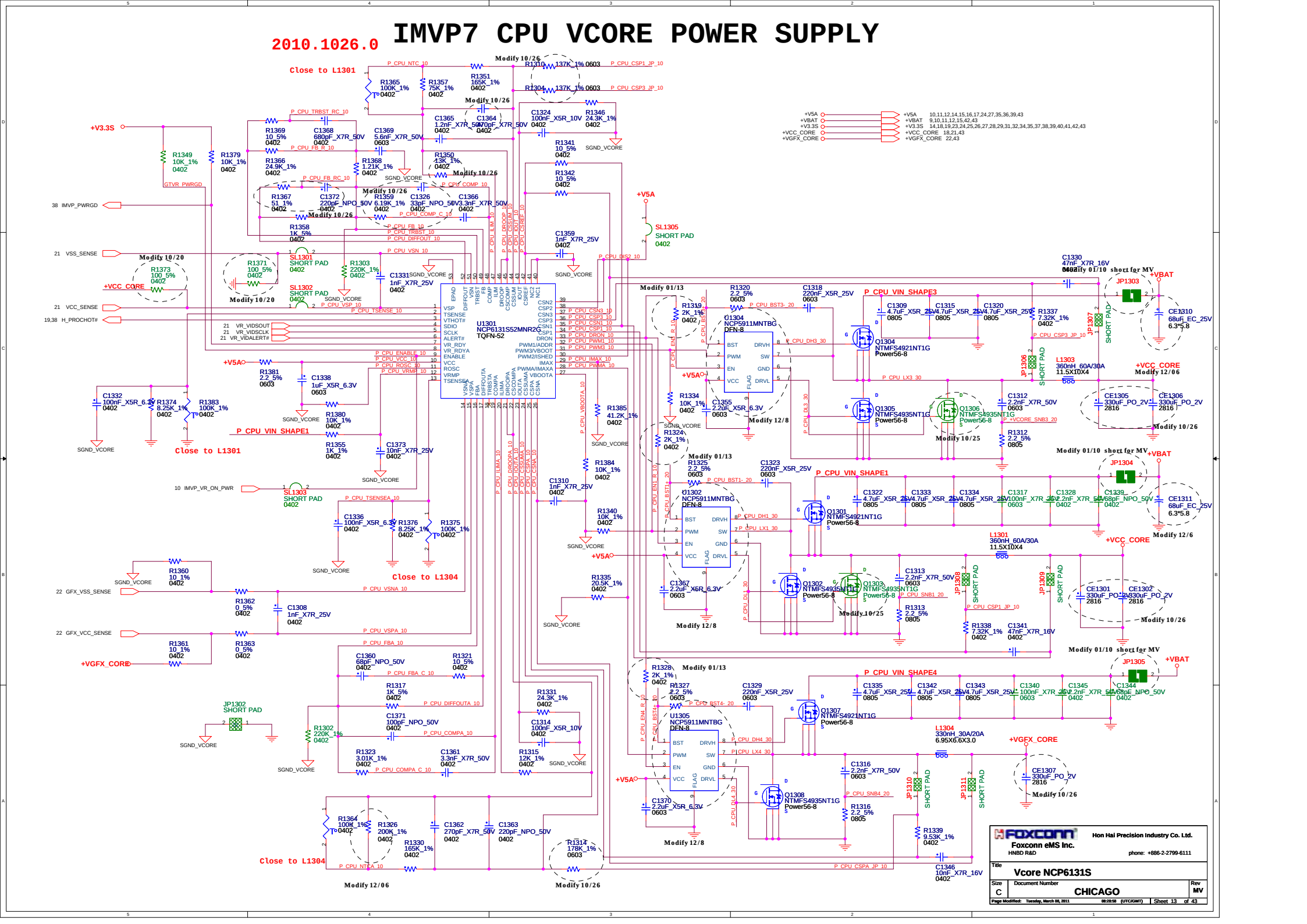
Page Modified: Tuesday, March 08, 2011	08:28:59 (UTC/GMT)	Sheet 12 of 43	

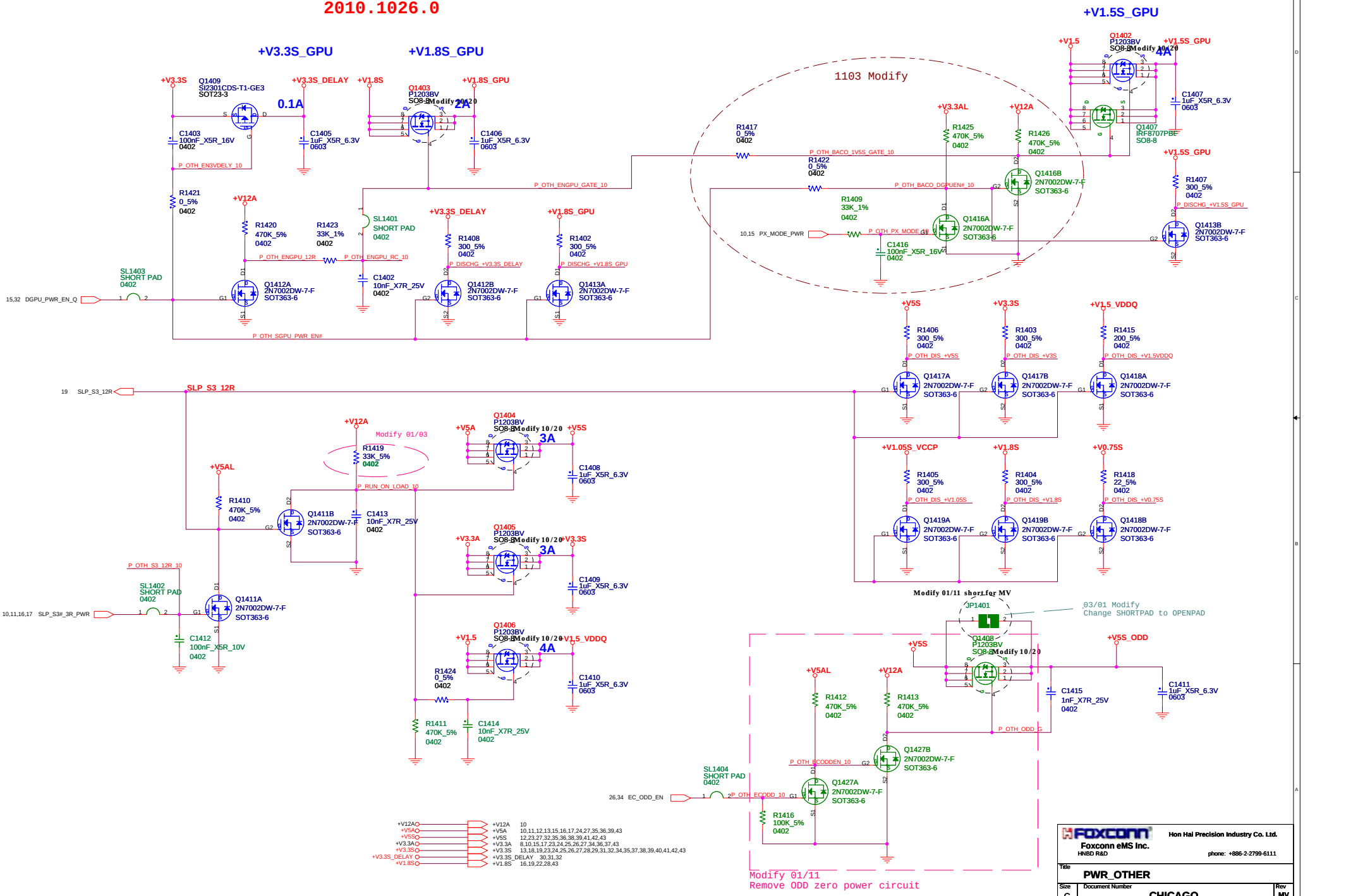
IMVP7 CPU VCORE POWER SUPPLY

2010.1026.0



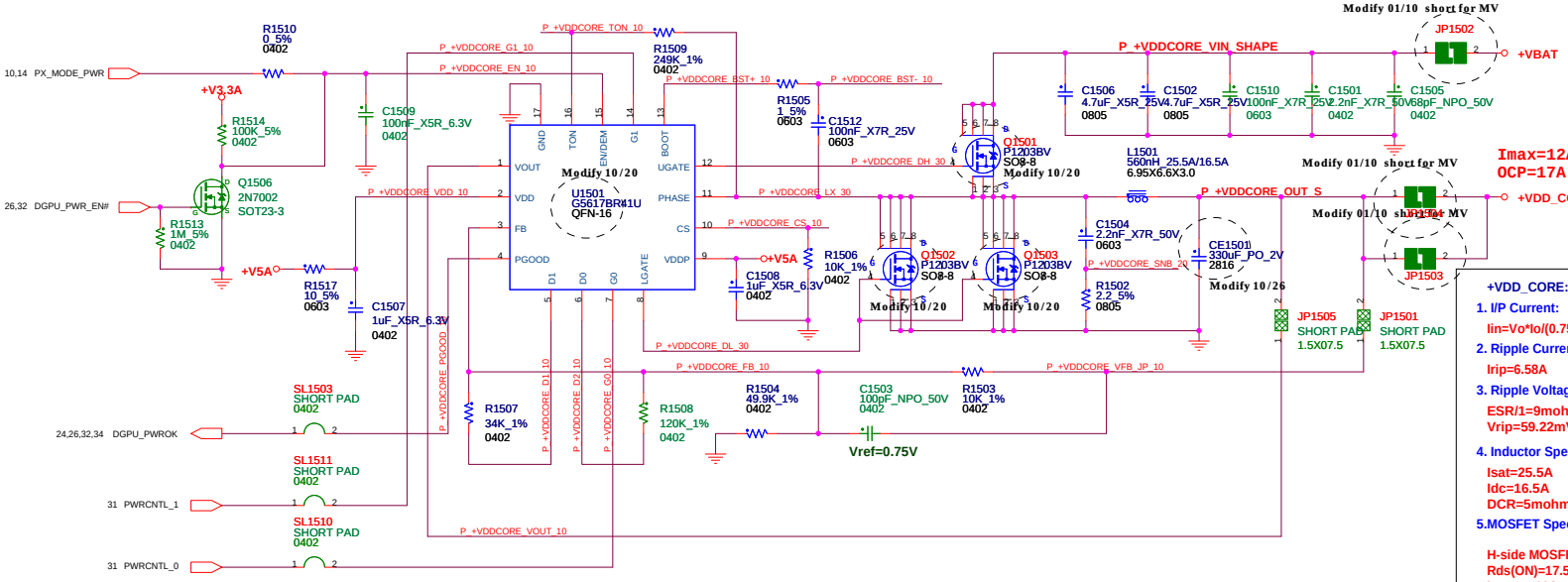
OTHER POWER / DISCHARGE CIRCUITS

2010.1026.0



+VDD_CORE POWER SUPPLY

2010.1026.0



PWRCNTL_1	PWRCNTL_0	VDD_CORE
0	---	1.121V
---	---	---
1	---	0.9V
---	---	---

+VDD_CORE:

1. I/P Current:

Iin=Vo*Io/(0.75*Vin)=1.48A

2. Ripple Current:

Irip=6.58A

3. Ripple Voltage:

ESR/1=9mohm
Vrip=59.22mV

4. Inductor Spec:

Isat=25.5A
Idc=16.5A
DCR=5mohm

5.MOSFET Spec:

H-side MOSFET: IRF8707PBF	L-side MOSFET: IRF8707PBF
Rds(ON)=17.5mohm (Vgs=4.5 V)	Rds(ON)=17.5mohm (Vgs=4.5 V)
I cont = 11A (T =25 ℃)	I cont = 11A (T =25 ℃)
I peak = 88A (Pause =10 us)	I peak = 88A (Pause =10 us)

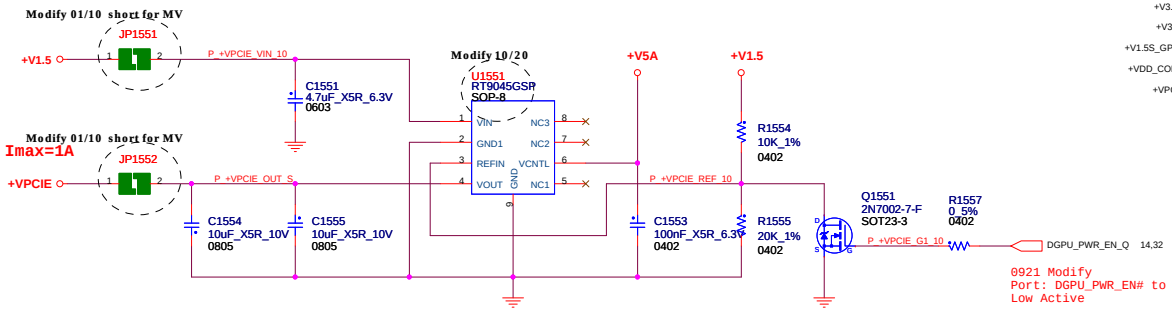
6. Frequency:

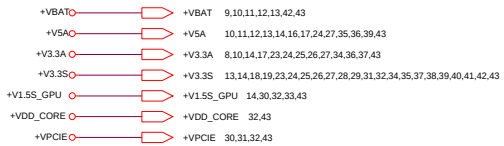
TON=9.6P*R1509*(VOUT+0.1) / (VIN-0.3)+50ns=206ns
F=VOUT/(VIN*TON)=286KHz

7. OCP:

Set = R1506 to 10K
Vtrip= R1206*10uA=0.1V
Iocp=(Vtrip/Rdson) + Iripple/2 = 17A

2010.1020.0 +VPCIE POWER SUPPLY





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Page Modified: Tuesday, March 08, 2011 08:28:58 (UTC/GMT) | Sheet 15 of 43

+V1.8S POWER SUPPLY

2010.1025.0

+V1.8S:

1. I/P Current:

Iin=Vo*Io/(0.75*Vin)=1.44A

2. Ripple Current:

Irip=0.53A

3. Ripple Voltage:

ESR/3=3.3mohm
Vrip=1.75mV

4. Inductor Spec:

Isat=14A
Idc=8A
DCR=20mohm

5.MOSFET Spec:

H-side P-MOSFET: Rds(ON)=110mohm (Vgs=4.5 V)

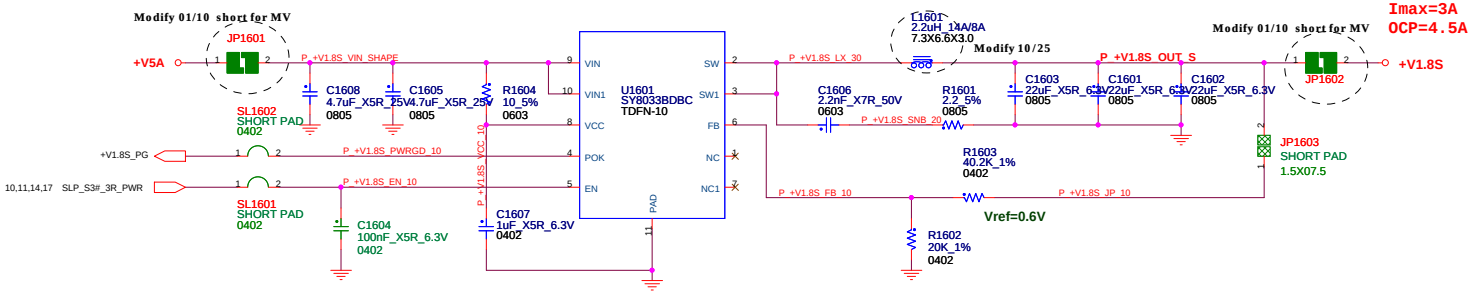
L-side N-MOSFET: Rds(ON)=75mohm (Vgs=4.5 V)

6. Frequency:

F=1MHz (min=800KHz, max=1.2MHz)

7. OCP:

Iocp=4A(min)/4.5A(typ)/5A(max)



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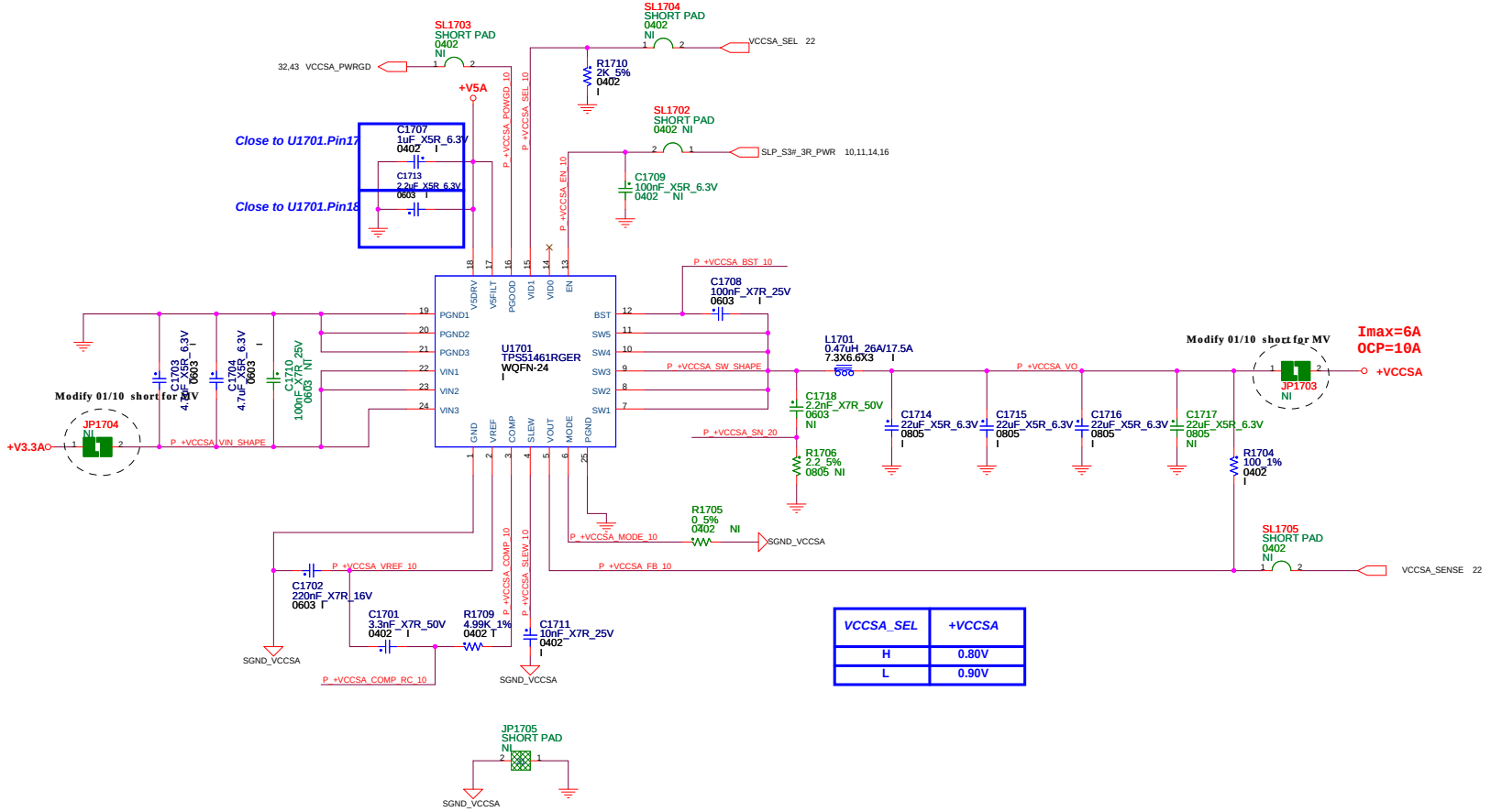
Page Modified: Tuesday, March 08, 2011 08:29:09 (UTC/GMT)		Sheet 16 of 43

+VCCSA POWER SUPPLY

2010.1026.0

+VCCSA:
1. I/P Current:
Iin=Vo*Io/(0.75*Vin)=2.18A
2. Ripple Current:
Irip=1.39A
3. Ripple Voltage:
ESR/4=1mohm
Vrip=1.39mV
4. Inductor Spec:
Isat=26A
Idc=17.5A
DCR=4.2mohm
5.MOSFET Spec:
6. Frequency:
F=1MHz (R1705=Open)
7. OCP:
Min : 6A / Typ : 7.5A



VCCSA_SEL	+VCCSA
H	0.80V
L	0.90V

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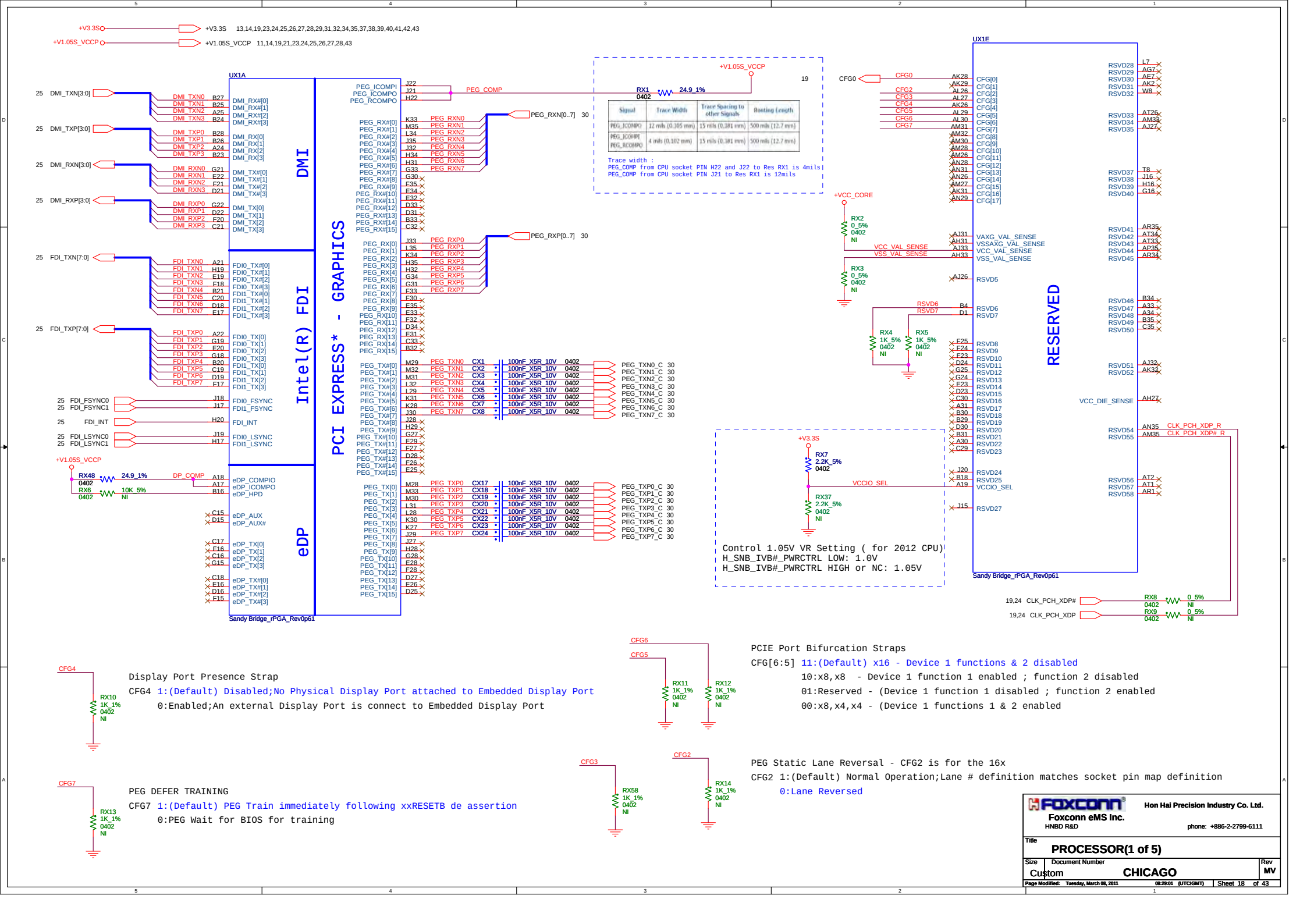
Page Modified: Tuesday, March 08, 2011 08:28:59 (UTC/GMT)
Sheet 17 of 43


+V3.3S +V3.3S 13,14,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V1.05S_VCCP +V1.05S_VCCP 11,14,19,21,23,24,25,26,27,28,43
UX1A
DMI
Intel(R) FDI
PCI EXPRESS* - GRAPHICS
eDP
Sandy Bridge_rPGA_Rev0p61
Trace width :
PEG_COMP from CPU socket PIN H22 and J22 to Res RX1 is 4mils
PEG_COMP from CPU socket PIN J21 to Res RX1 is 12mils
UX1E
RESERVED
Sandy Bridge_rPGA_Rev0p61
Control 1.05V VR Setting (for 2012 CPU)
H_SNB_IVB#_PWRCTRL LOW: 1.0V
H_SNB_IVB#_PWRCTRL HIGH or NC: 1.05V
Display Port Presence Strap
CFG4 1:(Default) Disabled;No Physical Display Port attached to Embedded Display Port
0:Enabled;An external Display Port is connect to Embedded Display Port
PEG DEFER TRAINING
CFG7 1:(Default) PEG Train immediately following xxRESETB de assertion
0:PEG Wait for BIOS for training
PCIE Port Bifurcation Straps
CFG[6:5] 11:(Default) x16 - Device 1 functions & 2 disabled
10:x8,x8 - Device 1 function 1 enabled ; function 2 disabled
01:Reserved - (Device 1 function 1 disabled ; function 2 enabled
00:x8,x4,x4 - (Device 1 functions 1 & 2 enabled
PEG Static Lane Reversal - CFG2 is for the 16x
CFG2 1:(Default) Normal Operation;Lane # definition matches socket pin map definition
0:Lane Reversed
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PROCESSOR(1 of 5)
Size Custom
Document Number CHICAGO
Rev MV
Page Modified: Tuesday, March 08, 2011 08:29:01 (UTC/GMT)
Sheet 18 of 43

+V3.3S +V3.3S 13,14,18,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V1.05S_VCCP +V1.05S_VCCP 11,14,18,21,23,24,25,26,27,28,43
+V1.5_VDDQ +V1.5_VDDQ 12,14,22,27,38
+V1.8S +V1.8S 14,16,22,28,43
+V1.5 +V1.5 12,14,15,22,29,43

UX1B

MISC
26 H_SNB_IVB# — C26 PROC_SELECT# (RX15 2.2K_5% 0402 to +V1.8S)
AN34 SKTOCC#

CLOCKS
BCLK A28 / BCLK# A27 — CLK_PCH_CPU_CLK 24 / CLK_PCH_CPU_CLK# 24 (100MHz)
DPLL_REF_CLK A16 / DPLL_REF_CLK# A15 — 0402 RX71 1K_5% / 0402 RX72 1K_5% to +V1.05S_VCCP

THERMAL
+V1.05S_VCCP
TP_P30 TP1 — 1 H_CATERR# — AL33 CATERR#
26,34 H_PECI — AN33 PECI
13,38 H_PROCHOT# — H_PROCHOT# — RX20 0402 56_5% — H_PROCHOT# R — AL32 PROCHOT#
RX18 62_5% 0402 (+V1.05S_VCCP)
CX33 43pF_X7R_50V 0402 (Close to VR)
26 H_THRMTRIP# — AN32 THERMTRIP#

DDR3 MISC
SM_DRAMRST# R8 — SM_DRAMRST#
SM_RCOMP[0] AK1 — SM_RCOMP0 RX22 140_1% 0402
SM_RCOMP[1] A5 — SM_RCOMP1 RX23 25.5_1% 0402
SM_RCOMP[2] A4 — SM_RCOMP2 RX24 200_1% 0402

RX16 0402 0_5% NI
+V1.5
RX17 1K_5% 0402
RX21 4.99K_1% 0402
QX1 2N7002-7-F SOT23-3 (SM_DRAMRST# Q)
RX19 0402 1K_5% — DDR3_DRAMRST# 29
RX25 0402 0_5% — DRAMRST_CNTRL 22,24
CX34 47nF_X7R_16V 0402

PWR MANAGEMENT
25 H_PM_SYNC — AM34 PM_SYNC
26 H_CPUPWRGD — H_CPUPWRGD — AP33 UNCOREPWRGOOD
CX125 100nF_X5R_10V 0402
RX27 10K_5% 0402 (SM_DRAMPWROK)
V8 SM_DRAMPWROK
BUF_PLT_RST# R — AR33 RESET#

JTAG & BPM
PRDY# AP29 — XDP_PRDY#
PREQ# AP27 — XDP_PREQ#
TCK AR26 — XDP_TCK
TMS AR27 — XDP_TMS
TRST# AP30 — XDP_TRST#
TDI AR28 — XDP_TDI
TDO AP26 — XDP_TDO
DBR# AL35 — XDP_DBR# — RX26 0402 1K_5% NI (+V3.3S) / RX69 0402 0_5% NI — SB_RST# 25
BPM#[0] AT28 XDP_OBS0
BPM#[1] AR29 XDP_OBS1
BPM#[2] AR30 XDP_OBS2
BPM#[3] AT30 XDP_OBS3
BPM#[4] AP32 XDP_OBS4
BPM#[5] AR31 XDP_OBS5
BPM#[6] AT31 XDP_OBS6
BPM#[7] AR32 XDP_OBS7

Sandy Bridge_rPGA_Rev0p61

PU/PD for JTAG signals
+V1.05S_VCCP
XDP_TDO RX28 0402 51_5%
XDP_TMS RX29 0402 51_5%
XDP_TDI RX30 0402 51_5%
XDP_PREQ# RX32 0402 51_5% NI
XDP_TCK RX33 0402 51_5%
XDP_TRST# RX35 0402 51_5%

RX31 0402 0_5% NI (SM_DRAMPWROK_R)
+V3.3S
RX36 200_1% 0402
CX126 100nF_Y5V_10V 0402
CX129 1uF_Y5V_6.3V 0402
+V1.5_VDDQ
RX34 200_1% 0402
25 PM_DRAM_PWRGD
34,43 ALL_SYS_PWRGD
UX4 74LVC2G07GW.125 (1A 1Y 6 / GND 3 / VCC 5 / 2A 2Y 4)
RX38 0402 130_1% — SM_DRAMPWROK
RX75 39_5% 0603 NI
QX4 2N7002-7-F SOT23-3 NI — SLP_S3_12R 14

HEADER1
XDP_PREQ# XDP_PRDY# XDP_OBS0 XDP_OBS1 XDP_OBS2 XDP_OBS3 XDP_OBS4 XDP_OBS5 XDP_OBS6 XDP_OBS7
GND0 OBSFN_A0 OBSFN_A1 GND2 OBSDATA_A0 OBSDATA_A1 GND4 OBSDATA_A2 OBSDATA_A3 GND6 OBSFN_B0 OBSFN_B1 GND8 OBSDATA_B0 OBSDATA_B1 GND10 OBSDATA_B2 OBSDATA_B3 GND12 PWRGOOD_HOOK0 HOOK1 VCC_OBS_AB HOOK2 HOOK3 GND14 SDA SCL TCK1 TCK0 GND16
GND1 OBSFN_C0 OBSFN_C1 GND3 OBSDATA_C0 OBSDATA_C1 GND5 OBSDATA_C2 OBSDATA_C3 GND7 OBSFN_D0 OBSFN_D1 GND9 OBSDATA_D0 OBSDATA_D1 GND11 OBSDATA_D2 OBSDATA_D3 GND13 ITPCLK_HOOK4 ITPCLK#_HOOK5 VCC_OBS_CD RESET#_HOOK6 DBR#_HOOK7 GND15 TDO TRSTn TDI TMS GND17
Hole2 62 Hole1 61
BSH-030-01-L-D-A-TR NI

H_CPUPWRGD — RX39 0402 1K_5% NI — XDP_H_CPUPWRGD
25,34 EC_PWRBTN#
+V1.05S_VCCP — RX40 0402 1K_5% NI — XDP_HOOK2
18 CFG0
25,43 SYS_PWROK
CX37 100nF_X5R_6.3V 0402 NI
XDP_TCK
CLK_PCH_XDP 18,24
CLK_PCH_XDP# 18,24
XDP_RST# — RX41 0402 1K_5% NI (+V1.05S_VCCP) — BUF_PLT_RST# 26,34,37,38,40
XDP_DBR#
XDP_TDO
XDP_TRST#
XDP_TDI
XDP_TMS

RX70 0402 1.5K_1%
+V3.3S
CX36 0402 100nF_Y5V_10V NI
+V1.05S_VCCP
RX42 0402 75_1% NI
26,34,37,38,40 BUF_PLT_RST#
UX3 74LVC1G07GW.125 SOT353-5 NI
BUFO_CPU_RST# — RX43 0402 43_1% NI — BUF_PLT_RST# R
RX44 0402 750_1%

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Title: PROCESSOR(2 of 5)
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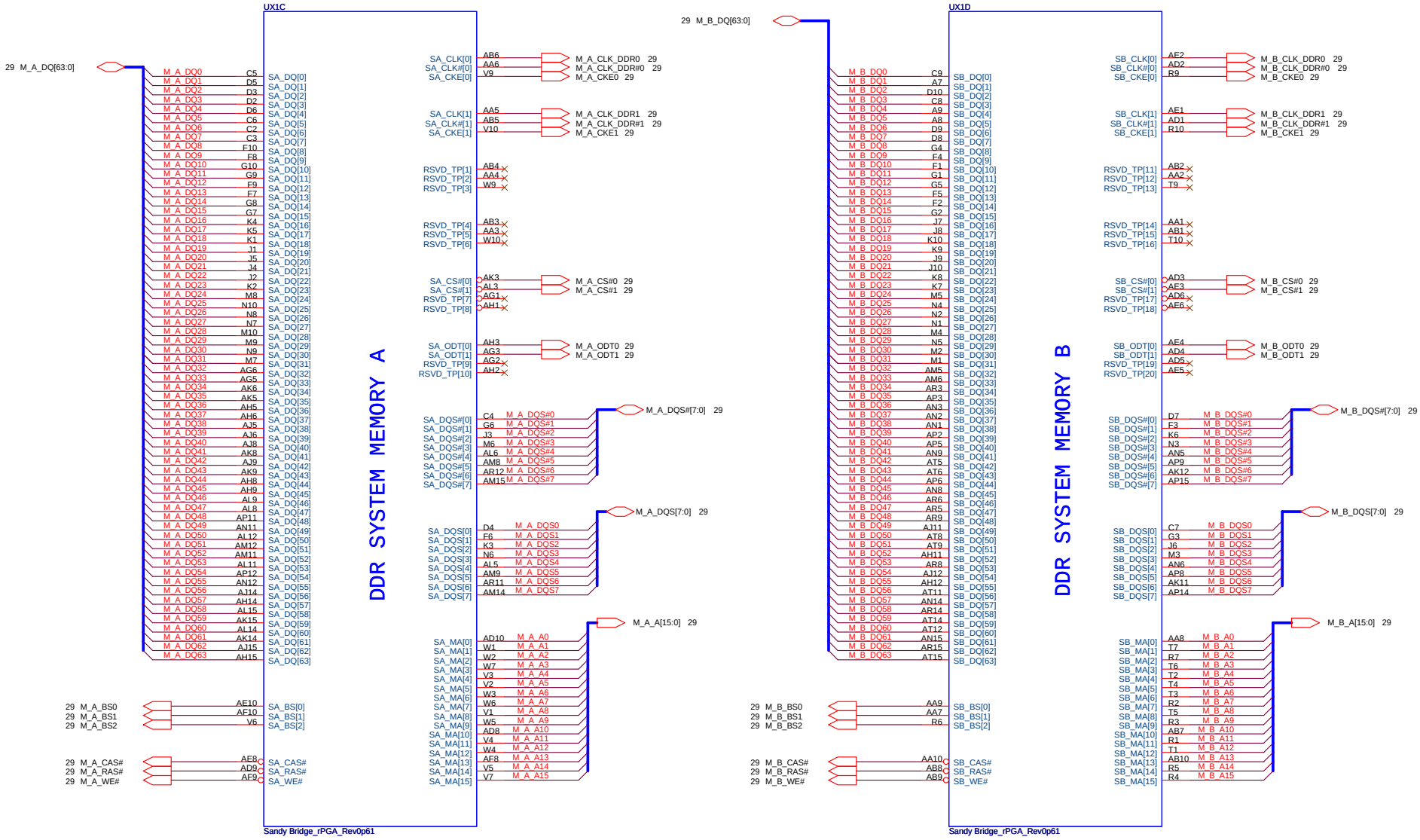
Page Modified: Tuesday, March 08, 2011 08:28:56 (UTC/GMT) | Sheet 19 of 43



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Title: PROCESSOR(3 of 5)

Size: Custom | Document Number: CHICAGO | Rev: MV

Page Modified: Tuesday, March 08, 2011 08:29:00 (UTC/GMT) | Sheet 20 of 43

+V1.05S_VCCP +V1.05S_VCCP 11,14,18,19,23,24,25,26,27,28,43

+VCC_CORE +VCC_CORE 13,18,43

POWER

FOR VCC:
4x 330 µF Bottom Edge,
10x 0603 10 µF Bottom Cavity,
8x 0805 22 µF Top Cavity,
8x 0805 22 µF Top Edge,

53A />2120mils

+VCC_CORE
CX41 22uF_X5R_6.3V 0805
CX42 22uF_X5R_6.3V 0805
CX43 22uF_X5R_6.3V 0805
CX44 22uF_X5R_6.3V 0805
CX50 22uF_X5R_6.3V 0805
CX59 22uF_X5R_6.3V 0805
CX60 22uF_X5R_6.3V 0805
CX61 22uF_X5R_6.3V 0805
CX62 22uF_X5R_6.3V 0805
CX63 22uF_X5R_6.3V 0805
RX45 22uF_X5R_6.3V 0805
CX72 22uF_X5R_6.3V 0805
RX46 22uF_X5R_6.3V 0805
CX73 22uF_X5R_6.3V 0805
CX74 22uF_X5R_6.3V 0805
CX75 22uF_X5R_6.3V 0805
CX79 10uF_X5R_6.3V 0603
CX80 10uF_X5R_6.3V 0603
CX81 10uF_X5R_6.3V 0603
RX51 10uF_X5R_6.3V 0603
CX82 10uF_X5R_6.3V 0603
RX54 10uF_X5R_6.3V 0603
CX83 10uF_X5R_6.3V 0603
RX55 10uF_X5R_6.3V 0603
CX84 10uF_X5R_6.3V 0603
CX85 10uF_X5R_6.3V 0603
RX59 33pF_NPO_50V 0402
CX87 33pF_NPO_50V 0402

UX1F

PEG AND DDR

+VCC_CORE
AG35 VCC1 … AG34 VCC2 … AG33 VCC3 … AG32 VCC4 … AG31 VCC5 … AG30 VCC6 … AG29 VCC7 … AG28 VCC8 … AG27 VCC9 … AG26 VCC10 … AF35 VCC11 … AF34 VCC12 … AF33 VCC13 … AF32 VCC14 … AF31 VCC15 … AF30 VCC16 … AF29 VCC17 … AF28 VCC18 … AF27 VCC19 … AF26 VCC20 … AD35 VCC21 … AD34 VCC22 … AD33 VCC23 … AD32 VCC24 … AD31 VCC25 … AD30 VCC26 … AD29 VCC27 … AD28 VCC28 … AD27 VCC29 … AD26 VCC30 … AC35 VCC31 … AC34 VCC32 … AC33 VCC33 … AC32 VCC34 … AC31 VCC35 … AC30 VCC36 … AC29 VCC37 … AC28 VCC38 … AC27 VCC39 … AC26 VCC40 … AA35 VCC41 … AA34 VCC42 … AA33 VCC43 … AA32 VCC44 … AA31 VCC45 … AA30 VCC46 … AA29 VCC47 … AA28 VCC48 … AA27 VCC49 … AA26 VCC50 … Y35 VCC51 … Y34 VCC52 … Y33 VCC53 … Y32 VCC54 … Y31 VCC55 … Y30 VCC56 … Y29 VCC57 … Y28 VCC58 … Y27 VCC59 … Y26 VCC60 … V35 VCC61 … V34 VCC62 … V33 VCC63 … V32 VCC64 … V31 VCC65 … V30 VCC66 … V29 VCC67 … V28 VCC68 … V27 VCC69 … V26 VCC70 … U35 VCC71 … U34 VCC72 … U33 VCC73 … U32 VCC74 … U31 VCC75 … U30 VCC76 … U29 VCC77 … U28 VCC78 … U27 VCC79 … U26 VCC80 … R35 VCC81 … R34 VCC82 … R33 VCC83 … R32 VCC84 … R31 VCC85 … R30 VCC86 … R29 VCC87 … R28 VCC88 … R27 VCC89 … R26 VCC90 … P35 VCC91 … P34 VCC92 … P33 VCC93 … P32 VCC94 … P31 VCC95 … P30 VCC96 … P29 VCC97 … P28 VCC98 … P27 VCC99 … P26 VCC100

CORE SUPPLY

FOR VCCIO:
2x 330 µF,
5x 0805 22 µF Bottom Cavity,
7x 0805 22 µF Top Cavity,

RF solution
0402 68pF_NPO_50V CX113 NI
0402 1nF_X7R_16V CX112 NI

8.5A />340mils

+V1.05S_VCCP
VCCIO1 AH13 … VCCIO2 AH10 … VCCIO3 AG10 … VCCIO4 AC10 … VCCIO5 Y10 … VCCIO6 U10 … VCCIO7 P10 … VCCIO8 L10 … VCCIO9 J14 … VCCIO10 J13 … VCCIO11 J12 … VCCIO12 J11 … VCCIO13 H14 … VCCIO14 H12 … VCCIO15 H11 … VCCIO16 G14 … VCCIO17 G13 … VCCIO18 G12 … VCCIO19 F14 … VCCIO20 F13 … VCCIO21 F12 … VCCIO22 F11 … VCCIO23 E14 … VCCIO24 E12 … VCCIO25 E11 … VCCIO26 D14 … VCCIO27 D13 … VCCIO28 D12 … VCCIO29 D11 … VCCIO30 C14 … VCCIO31 C13 … VCCIO32 C12 … VCCIO33 C11 … VCCIO34 B14 … VCCIO35 B12 … VCCIO36 A14 … VCCIO37 A13 … VCCIO38 A12 … VCCIO39 A11 … VCCIO40 J23

CX65 0805 22uF_X5R_6.3V
CX66 0805 22uF_X5R_6.3V
CX47 0805 22uF_X5R_6.3V
CX38 0805 22uF_X5R_6.3V
CX48 0805 22uF_X5R_6.3V
CX39 0805 22uF_X5R_6.3V
CX40 0805 22uF_X5R_6.3V
CX70 330uF_PO_2V 2816
CX54 0805 22uF_X5R_6.3V
CX55 0805 22uF_X5R_6.3V
CX56 0805 22uF_X5R_6.3V
CX57 0805 22uF_X5R_6.3V
CX58 0805 22uF_X5R_6.3V

SVID

VIDALERT# AJ29 VR_SVID_ALERT#_R
VIDSCLK AJ30 VR_SVID_CLK_R
VIDSOUT AJ28 VR_SVID_DATA_R

Close to VR
+V1.05S_VCCP
RX47 75_5% 0402
CX123 0402 NI 100nF_X5R_10V
Close to CPU
RX49 0402 43_5%
VR_VIDALERT# 13

Close to VR
+V1.05S_VCCP
RX50 54.9_1% 0402
Close to CPU
RX52 0402 0_5%
VR_VIDSCLK 13

Close to CPU
+V1.05S_VCCP
CX124 0402 NI 100nF_X5R_10V
RX53 130_5% 0402
Close to VR
+V1.05S_VCCP
RX56 130_5% 0402
RX57 0402 0_5%
VR_VIDSOUT 13

SENSE LINES

+VCC_CORE
RX76 100_5% 0402
RX77 100_5% 0402

VCC_SENSE AJ35
VSS_SENSE AJ34
VCC_SENSE 13
VSS_SENSE 13

VCCIO_SENSE B10
VSSIO_SENSE A10
VCCP_SENSE 11
VSSP_SENSE 11

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UX1H

VSS

AT35 VSS1 … AT32 VSS2 … AT29 VSS3 … AT27 VSS4 … AT25 VSS5 … AT22 VSS6 … AT19 VSS7 … AT16 VSS8 … AT13 VSS9 … AT10 VSS10 … AT7 VSS11 … AT4 VSS12 … AT3 VSS13 … AR25 VSS14 … AR22 VSS15 … AR19 VSS16 … AR16 VSS17 … AR13 VSS18 … AR10 VSS19 … AR7 VSS20 … AR4 VSS21 … AR2 VSS22 … AP34 VSS23 … AP31 VSS24 … AP28 VSS25 … AP25 VSS26 … AP22 VSS27 … AP19 VSS28 … AP16 VSS29 … AP13 VSS30 … AP10 VSS31 … AP7 VSS32 … AP4 VSS33 … AP1 VSS34 … AN30 VSS35 … AN27 VSS36 … AN25 VSS37 … AN22 VSS38 … AN19 VSS39 … AN16 VSS40 … AN13 VSS41 … AN10 VSS42 … AN7 VSS43 … AN4 VSS44 … AM29 VSS45 … AM25 VSS46 … AM22 VSS47 … AM19 VSS48 … AM16 VSS49 … AM13 VSS50 … AM10 VSS51 … AM7 VSS52 … AM4 VSS53 … AM3 VSS54 … AM2 VSS55 … AM1 VSS56 … AL34 VSS57 … AL31 VSS58 … AL28 VSS59 … AL25 VSS60 … AL22 VSS61 … AL19 VSS62 … AL16 VSS63 … AL13 VSS64 … AL10 VSS65 … AL7 VSS66 … AL4 VSS67 … AL2 VSS68 … AK33 VSS69 … AK30 VSS70 … AK27 VSS71 … AK25 VSS72 … AK22 VSS73 … AK19 VSS74 … AK16 VSS75 … AK13 VSS76 … AK10 VSS77 … AK7 VSS78 … AK4 VSS79 … AJ25 VSS80

VSS81 AJ22 … VSS82 AJ19 … VSS83 AJ16 … VSS84 AJ13 … VSS85 AJ10 … VSS86 AJ7 … VSS87 AJ4 … VSS88 AJ3 … VSS89 AJ2 … VSS90 AJ1 … VSS91 AH35 … VSS92 AH34 … VSS93 AH32 … VSS94 AH30 … VSS95 AH29 … VSS96 AH28 … VSS97 AH26 … VSS98 AH25 … VSS99 AH22 … VSS100 AH19 … VSS101 AH16 … VSS102 AH7 … VSS103 AH4 … VSS104 AG9 … VSS105 AG8 … VSS106 AG4 … VSS107 AF6 … VSS108 AF5 … VSS109 AF3 … VSS110 AF2 … VSS111 AE35 … VSS112 AE34 … VSS113 AE33 … VSS114 AE32 … VSS115 AE31 … VSS116 AE30 … VSS117 AE29 … VSS118 AE28 … VSS119 AE27 … VSS120 AE26 … VSS121 AE9 … VSS122 AD7 … VSS123 AC9 … VSS124 AC8 … VSS125 AC6 … VSS126 AC5 … VSS127 AC3 … VSS128 AC2 … VSS129 AB35 … VSS130 AB34 … VSS131 AB33 … VSS132 AB32 … VSS133 AB31 … VSS134 AB30 … VSS135 AB29 … VSS136 AB28 … VSS137 AB27 … VSS138 AB26 … VSS139 Y9 … VSS140 Y8 … VSS141 Y6 … VSS142 Y5 … VSS143 Y3 … VSS144 Y2 … VSS145 W35 … VSS146 W34 … VSS147 W33 … VSS148 W32 … VSS149 W31 … VSS150 W30 … VSS151 W29 … VSS152 W28 … VSS153 W27 … VSS154 W26 … VSS155 U9 … VSS156 U8 … VSS157 U6 … VSS158 U5 … VSS159 U3 … VSS160 U2

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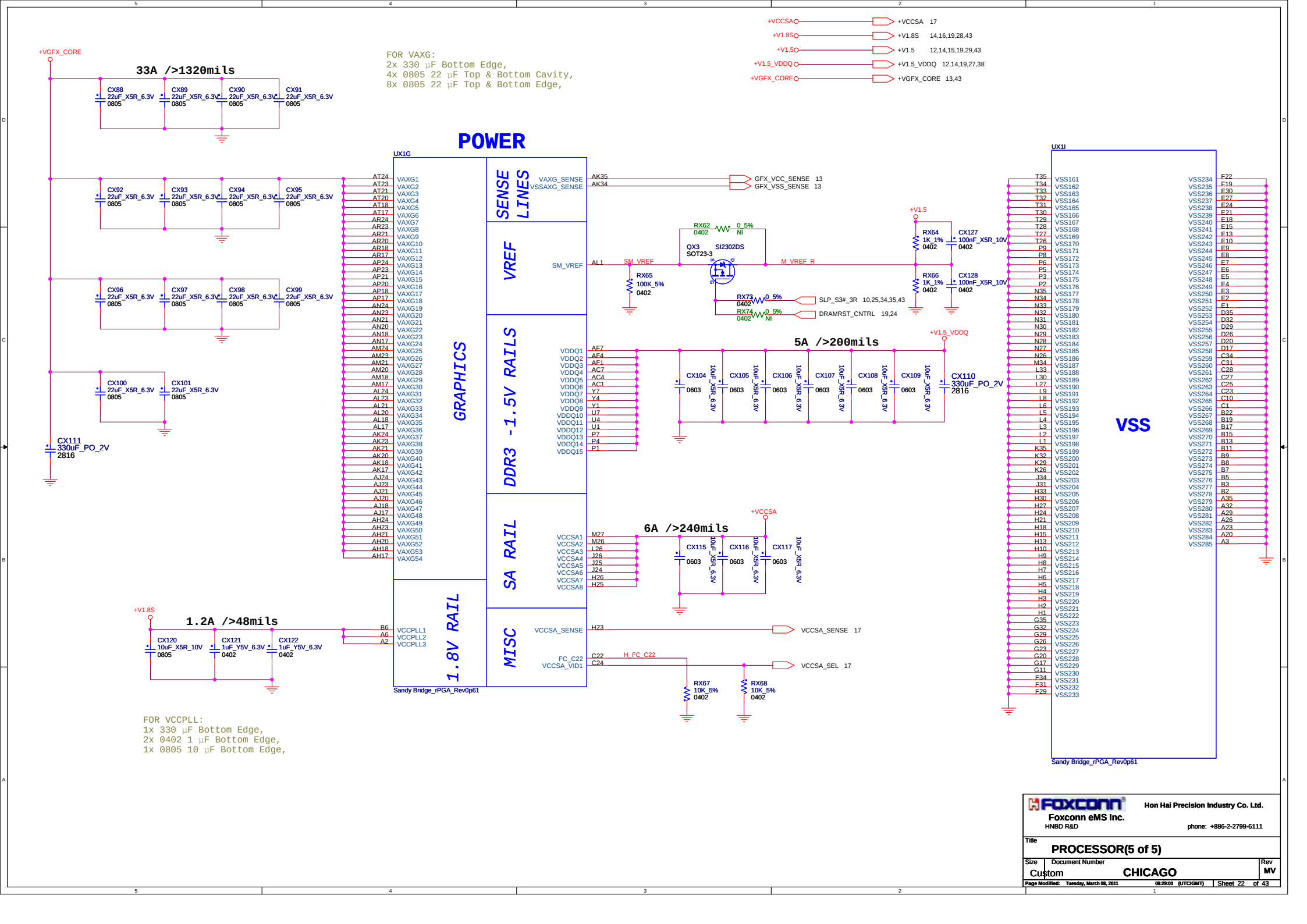
Size: Custom | Document Number: CHICAGO | Rev: MV
Page Modified: Tuesday, March 08, 2011 08:29:00 (UTC/GMT) | Sheet 21 of 43


+VCCSA +VCCSA 17
+V1.8S +V1.8S 14,16,19,28,43
+V1.5 +V1.5 12,14,15,19,29,43
+V1.5_VDDQ +V1.5_VDDQ 12,14,19,27,38
+VGFX_CORE +VGFX_CORE 13,43
FOR VAXG:
2x 330 µF Bottom Edge,
4x 0805 22 µF Top & Bottom Cavity,
8x 0805 22 µF Top & Bottom Edge,
+VGFX_CORE
33A />1320mils
CX88 22uF_X5R_6.3V 0805
CX89 22uF_X5R_6.3V 0805
CX90 22uF_X5R_6.3V 0805
CX91 22uF_X5R_6.3V 0805
CX92 22uF_X5R_6.3V 0805
CX93 22uF_X5R_6.3V 0805
CX94 22uF_X5R_6.3V 0805
CX95 22uF_X5R_6.3V 0805
CX96 22uF_X5R_6.3V 0805
CX97 22uF_X5R_6.3V 0805
CX98 22uF_X5R_6.3V 0805
CX99 22uF_X5R_6.3V 0805
CX100 22uF_X5R_6.3V 0805
CX101 22uF_X5R_6.3V 0805
CX111 330uF_PO_2V 2816
POWER
UX1G
SENSE LINES
VAXG_SENSE
VSSAXG_SENSE
AK35
AK34
GFX_VCC_SENSE 13
GFX_VSS_SENSE 13
VREF
SM_VREF
AL1
RX62 0402 0_5% NI
QX3 SI2302DS SOT23-3
RX65 100K_5% 0402
RX73 0402 0_5%
RX74 0402 0_5% NI
SLP_S3#_3R 10,25,34,35,43
DRAMRST_CNTRL 19,24
+V1.5
RX64 1K_1% 0402
RX66 1K_1% 0402
CX127 100nF_X5R_10V 0402
CX128 100nF_X5R_10V 0402
DDR3 -1.5V RAILS
5A />200mils
+V1.5_VDDQ
VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15
AF7 AF4 AF1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1
CX104 CX105 CX106 CX107 CX108 CX109 0603 10uF_X5R_6.3V
CX110 330uF_PO_2V 2816
SA RAIL
6A />240mils
+VCCSA
VCCSA1 VCCSA2 VCCSA3 VCCSA4 VCCSA5 VCCSA6 VCCSA7 VCCSA8
M27 M26 L26 J26 J25 J24 H26 H25
CX115 CX116 CX117 0603 10uF_X5R_6.3V
MISC
VCCSA_SENSE
H23
VCCSA_SENSE 17
FC_C22
VCCSA_VID1
C22 C24
H_FC_C22
VCCSA_SEL 17
RX67 10K_5% 0402
RX68 10K_5% 0402
GRAPHICS
AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17
VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54
1.8V RAIL
+V1.8S
1.2A />48mils
CX120 10uF_X5R_10V 0805
CX121 1uF_Y5V_6.3V 0402
CX122 1uF_Y5V_6.3V 0402
B6 A6 A2
VCCPLL1 VCCPLL2 VCCPLL3
Sandy Bridge_rPGA_Rev0p61
FOR VCCPLL:
1x 330 µF Bottom Edge,
2x 0402 1 µF Bottom Edge,
1x 0805 10 µF Bottom Edge,
UX1I
VSS
T35 T34 T33 T32 T31 T30 T29 T28 T27 T26 P9 P8 P6 P5 P3 P2 N35 N34 N33 N32 N31 N30 N29 N28 N27 N26 M34 L33 L30 L27 L9 L8 L6 L5 L4 L3 L2 L1 K35 K32 K29 K26 J34 J31 H33 H30 H27 H24 H21 H18 H15 H13 H10 H9 H8 H7 H6 H5 H4 H3 H2 H1 G35 G32 G29 G26 G23 G20 G17 G11 F34 F31 F29
VSS161 VSS162 VSS163 VSS164 VSS165 VSS166 VSS167 VSS168 VSS169 VSS170 VSS171 VSS172 VSS173 VSS174 VSS175 VSS176 VSS177 VSS178 VSS179 VSS180 VSS181 VSS182 VSS183 VSS184 VSS185 VSS186 VSS187 VSS188 VSS189 VSS190 VSS191 VSS192 VSS193 VSS194 VSS195 VSS196 VSS197 VSS198 VSS199 VSS200 VSS201 VSS202 VSS203 VSS204 VSS205 VSS206 VSS207 VSS208 VSS209 VSS210 VSS211 VSS212 VSS213 VSS214 VSS215 VSS216 VSS217 VSS218 VSS219 VSS220 VSS221 VSS222 VSS223 VSS224 VSS225 VSS226 VSS227 VSS228 VSS229 VSS230 VSS231 VSS232 VSS233
VSS234 VSS235 VSS236 VSS237 VSS238 VSS239 VSS240 VSS241 VSS242 VSS243 VSS244 VSS245 VSS246 VSS247 VSS248 VSS249 VSS250 VSS251 VSS252 VSS253 VSS254 VSS255 VSS256 VSS257 VSS258 VSS259 VSS260 VSS261 VSS262 VSS263 VSS264 VSS265 VSS266 VSS267 VSS268 VSS269 VSS270 VSS271 VSS272 VSS273 VSS274 VSS275 VSS276 VSS277 VSS278 VSS279 VSS280 VSS281 VSS282 VSS283 VSS284 VSS285
F22 F19 E30 E27 E24 E21 E18 E15 E13 E10 E9 E8 E7 E6 E5 E4 E3 E2 E1 D35 D32 D29 D26 D20 D17 C34 C31 C28 C27 C25 C23 C10 C1 B22 B19 B17 B15 B13 B11 B9 B8 B7 B5 B3 B2 A35 A32 A29 A26 A23 A20 A3
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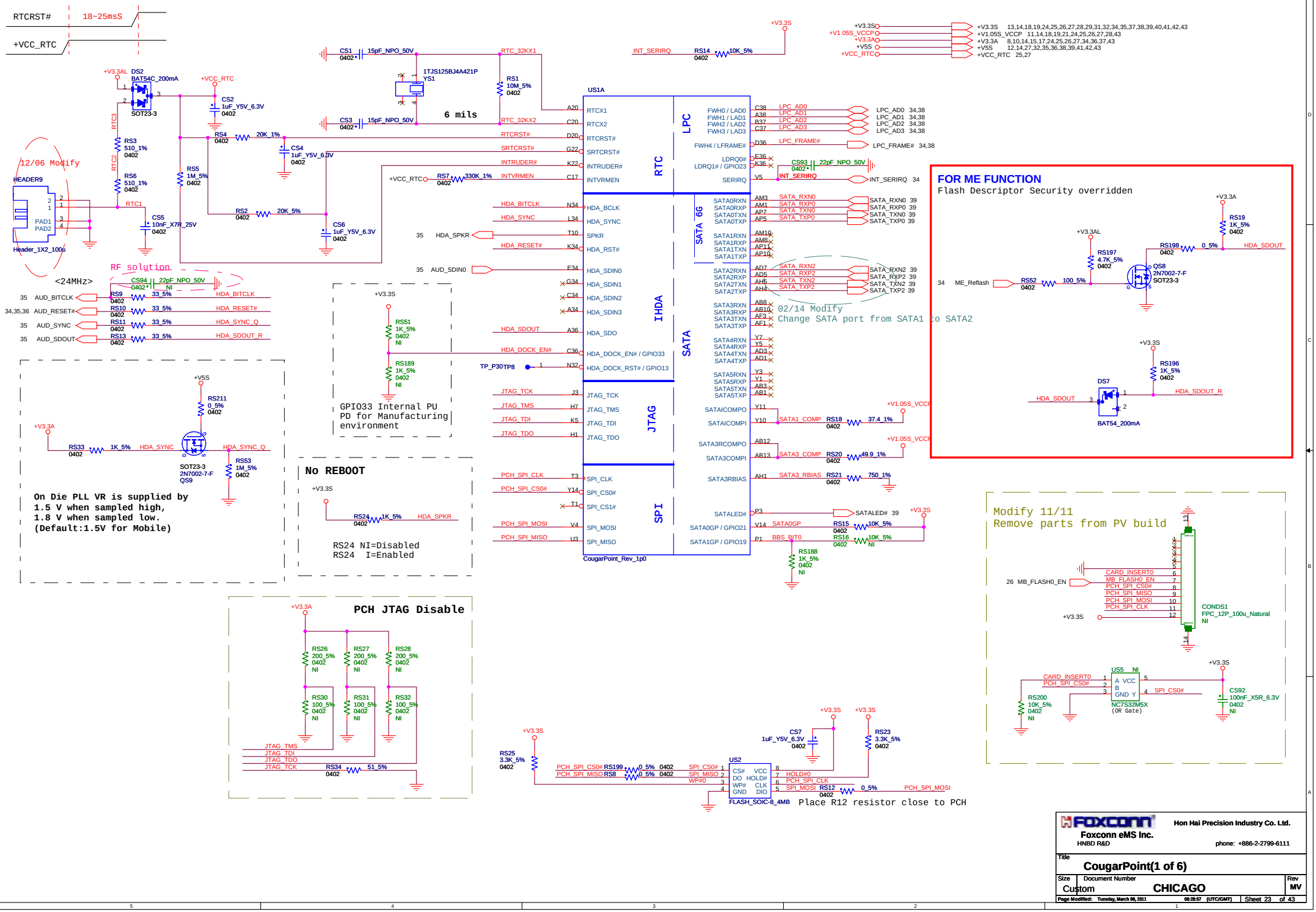
Document Number CHICAGO
Rev MV
Page Modified: Tuesday, March 08, 2011 08:29:00 (UTC/GMT)
Sheet 22 of 43



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Size: Custom	Document Number: CHICAGO
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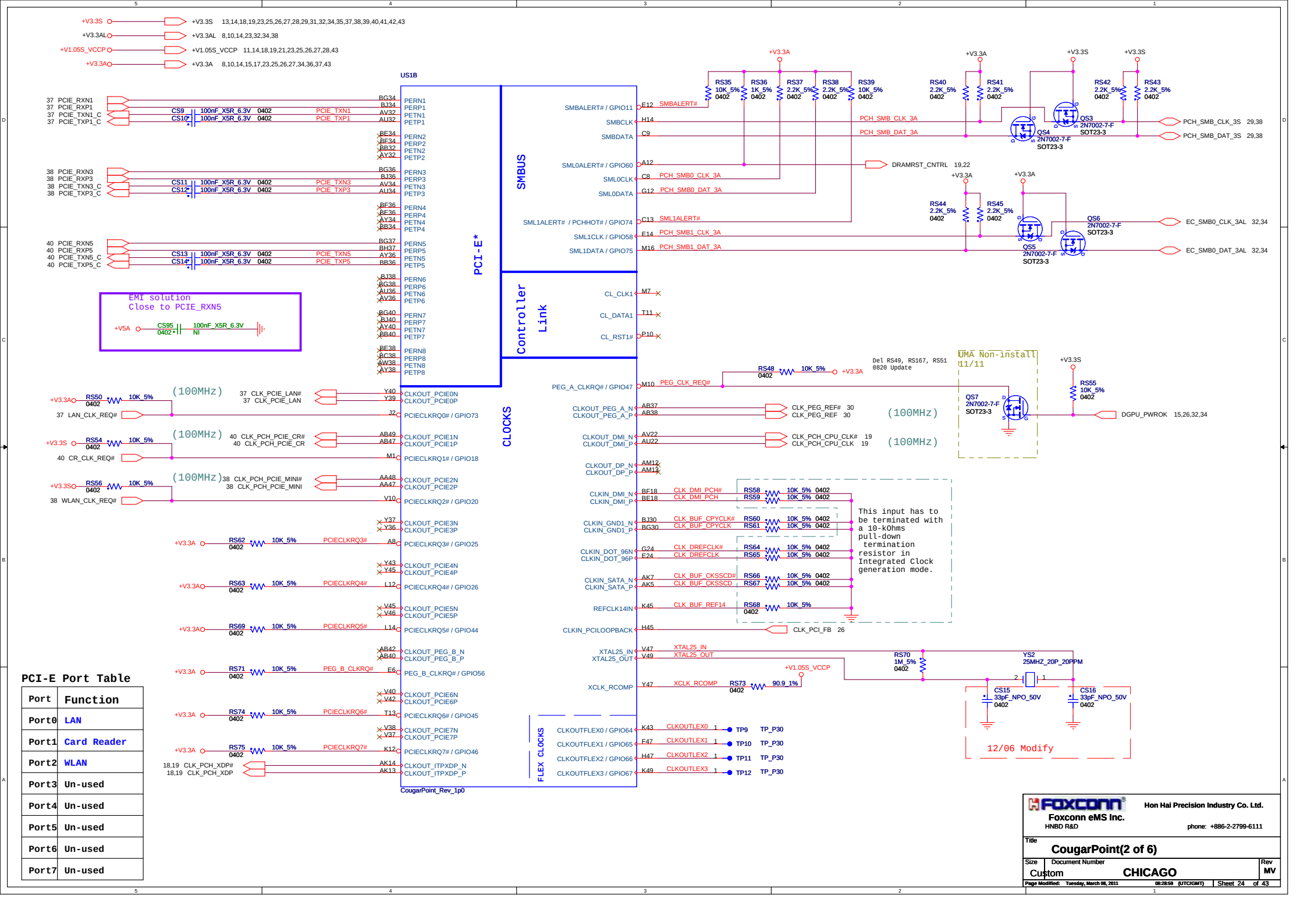
Page Modified: Tuesday, March 08, 2011 08:28:57 (UTC/GMT)	Sheet 23 of 43



PCI-E Port Table

Port	Function
Port0	LAN
Port1	Card Reader
Port2	WLAN
Port3	Un-used
Port4	Un-used
Port5	Un-used
Port6	Un-used
Port7	Un-used

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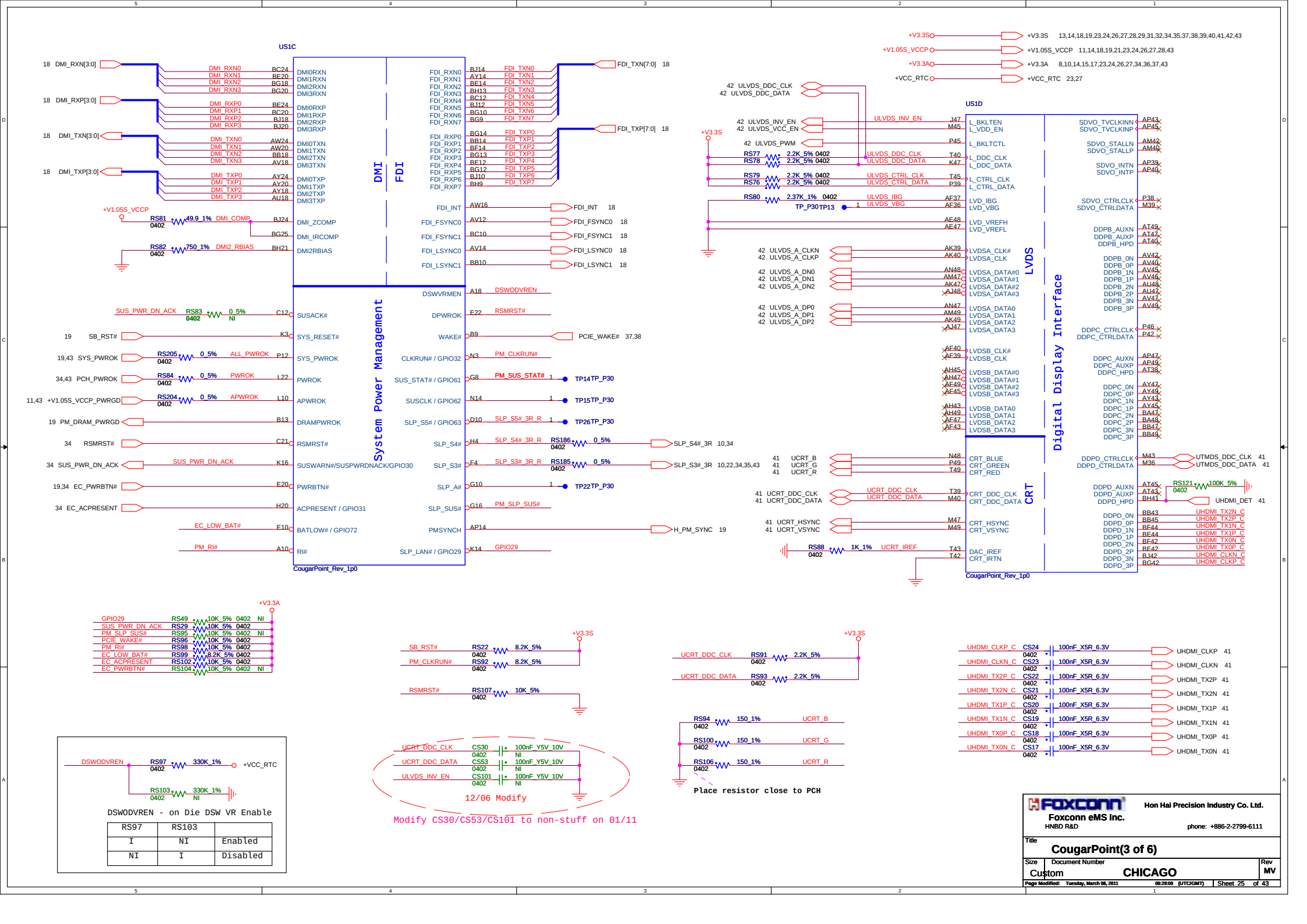
Size: Custom | Document Number: CHICAGO | Rev: MV

Page Modified: Tuesday, March 08, 2011 08:28:59 (UTC/GMT) | Sheet 24 of 43


US1C
DMI
FDI
System Power Management
CougarPoint_Rev_1p0
US1D
LVDS
Digital Display Interface
CRT
CougarPoint_Rev_1p0
DSWODVREN - on Die DSW VR Enable
RS97 | RS103 | Enabled
I | NI | Enabled
NI | I | Disabled
12/06 Modify
Modify CS30/CS53/CS101 to non-stuff on 01/11
Place resistor close to PCH
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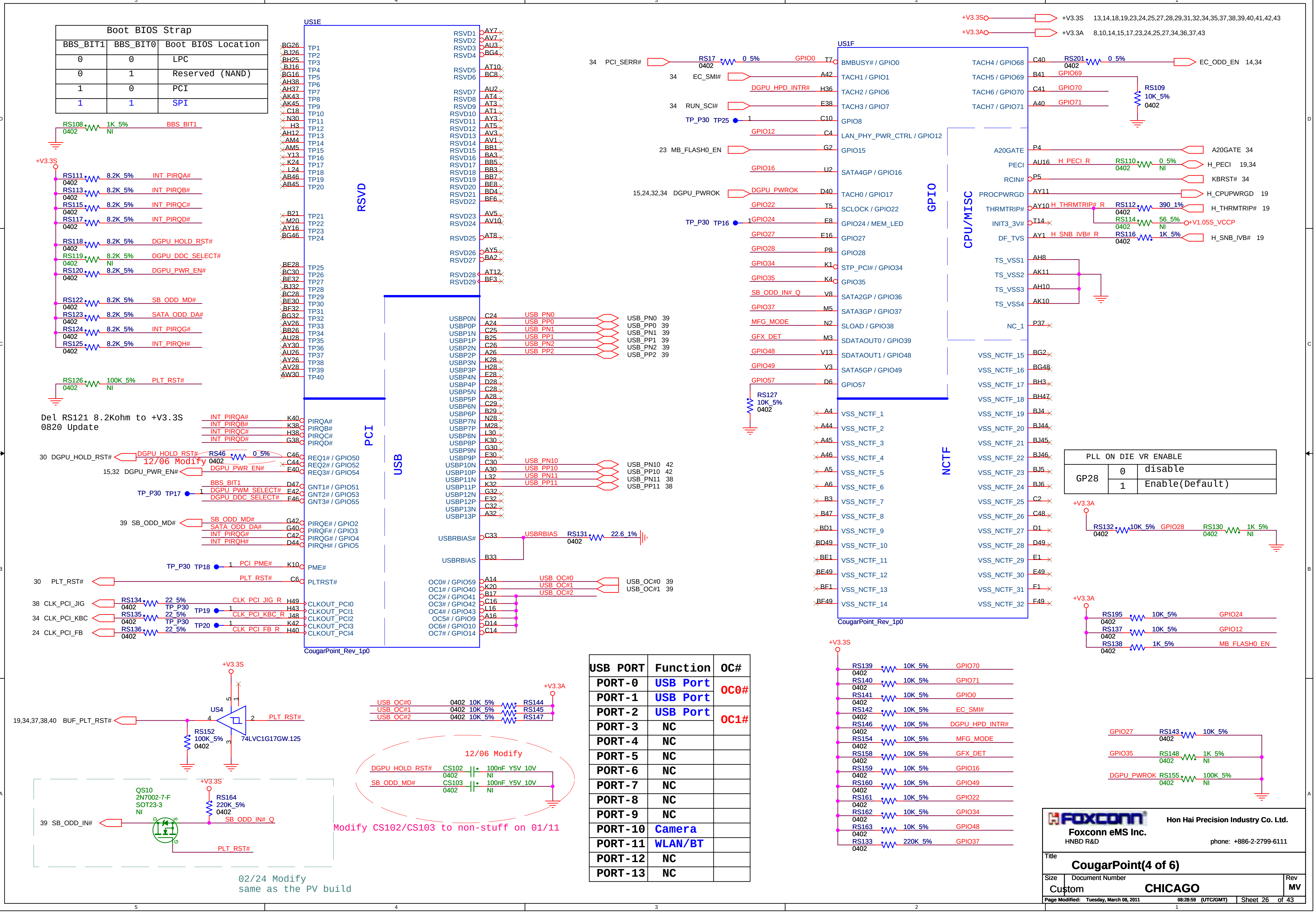
CougarPoint(3 of 6)
Custom
CHICAGO
MV
Sheet 25 of 43

Boot BIOS Strap

BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



USB PORT	Function	OC#
PORT-0	USB Port	OC0#
PORT-1	USB Port	
PORT-2	USB Port	OC1#
PORT-3	NC	
PORT-4	NC	
PORT-5	NC	
PORT-6	NC	
PORT-7	NC	
PORT-8	NC	
PORT-9	NC	
PORT-10	Camera	
PORT-11	WLAN/BT	
PORT-12	NC	
PORT-13	NC	

PLL ON DIE VR ENABLE

GP28	0	disable
	1	Enable(Default)

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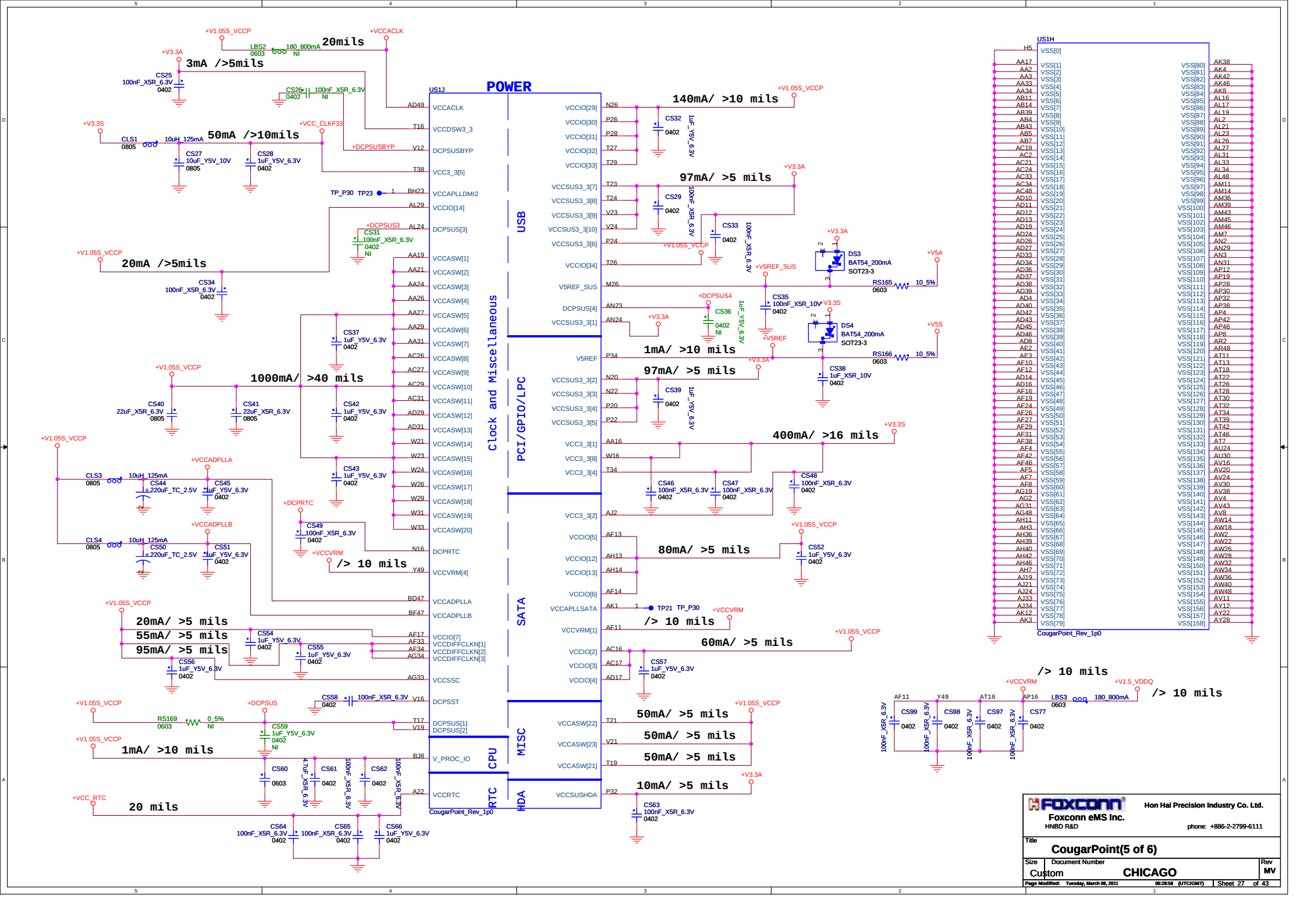
POWER
US1J
CougarPoint_Rev_1p0
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
20mils
3mA />5mils
50mA />10mils
20mA />5mils
1000mA/ >40 mils
1mA/ >10 mils
20mA/ >5 mils
55mA/ >5 mils
95mA/ >5 mils
20 mils
140mA/ >10 mils
97mA/ >5 mils
1mA/ >10 mils
97mA/ >5 mils
400mA/ >16 mils
80mA/ >5 mils
/> 10 mils
60mA/ >5 mils
50mA/ >5 mils
50mA/ >5 mils
50mA/ >5 mils
10mA/ >5 mils
/> 10 mils
/> 10 mils
US1H
CougarPoint_Rev_1p0
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CougarPoint(5 of 6)
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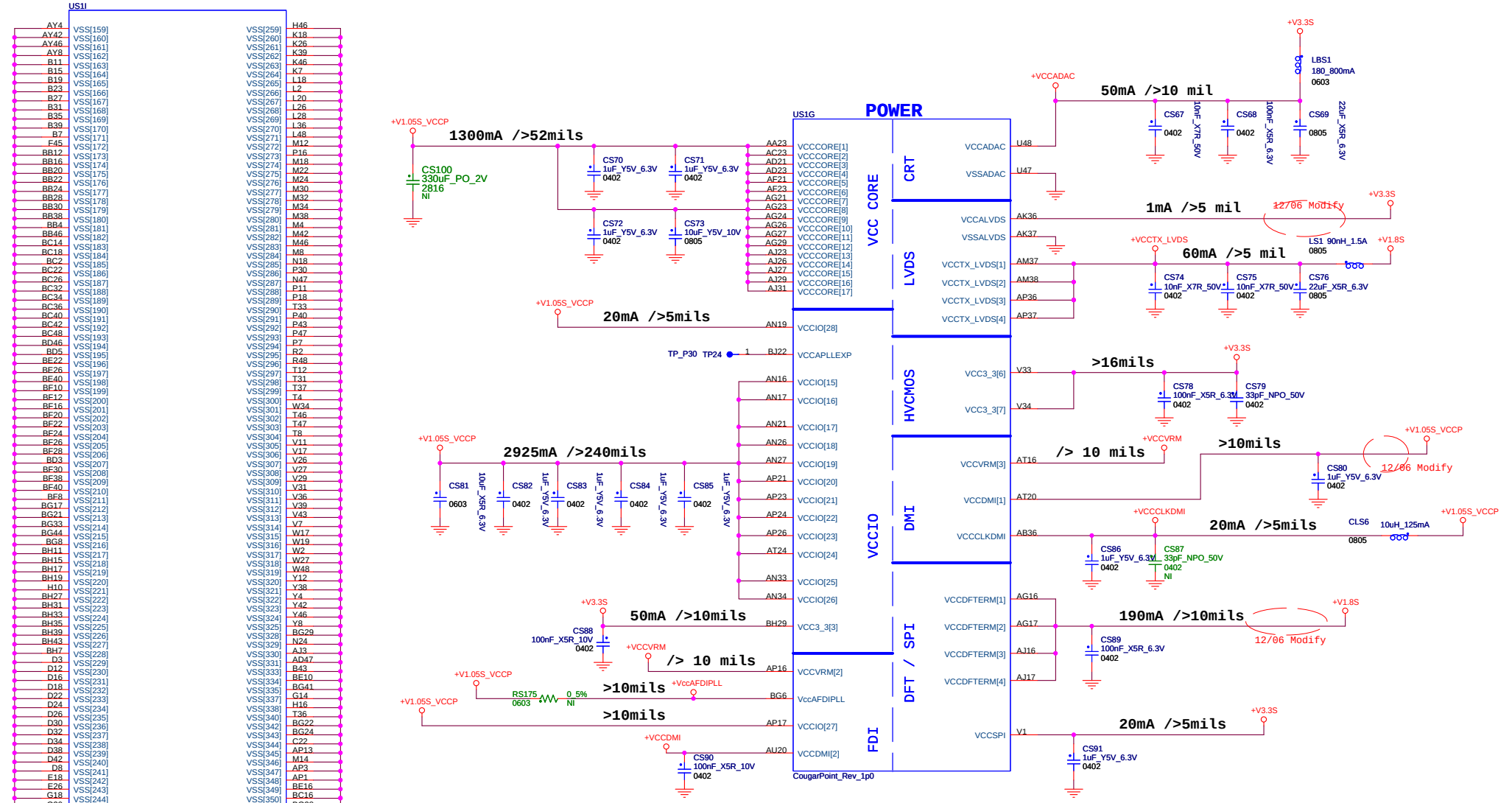
Sheet 27 of 43



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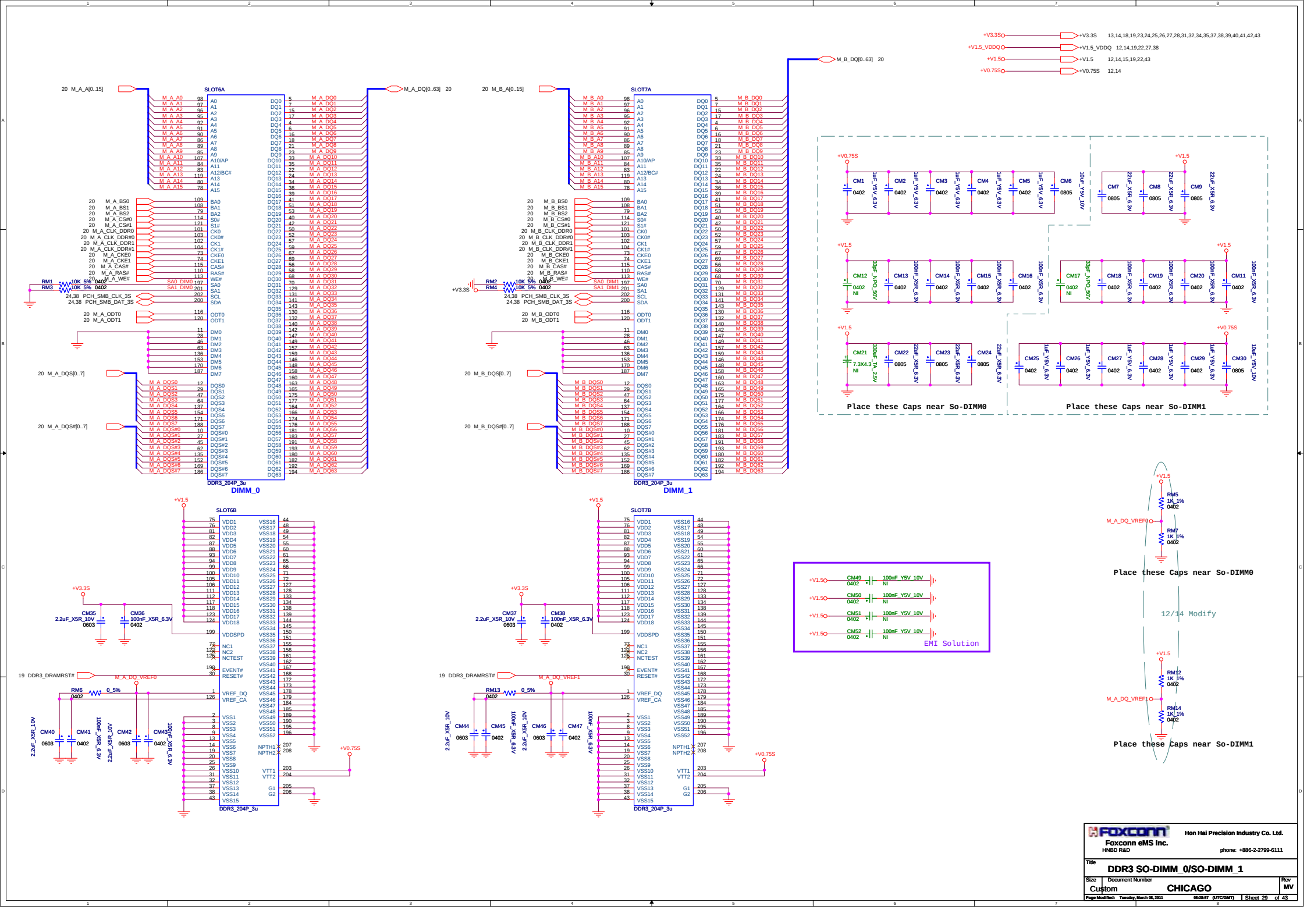
Title: CougarPoint(6 of 6)		
Size: Custom	Document Number: CHICAGO	Rev: MV
Page Modified: Tuesday, March 08, 2011 08:28:59 (UTC/GMT)		Sheet 28 of 43


+V3.3S +V3.3S 13,14,18,19,23,24,25,26,27,28,31,32,34,35,37,38,39,40,41,42,43
+V1.5_VDDQ +V1.5_VDDQ 12,14,19,22,27,38
+V1.5 +V1.5 12,14,15,19,22,43
+V0.75S +V0.75S 12,14
M_B_DQ[0..63] 20
SLOT6A
SLOT7A
M_A_A[0..15]
M_B_A[0..15]
M_A_DQ[0..63] 20
M_A_DQS[0..7]
M_A_DQS#[0..7]
M_B_DQS[0..7]
M_B_DQS#[0..7]
DDR3_204P_3u
DIMM_0
DIMM_1
Place these Caps near So-DIMM0
Place these Caps near So-DIMM1
EMI Solution
12/14 Modify
SLOT6B
SLOT7B
M_A_DQ_VREF0
M_A_DQ_VREF1
DDR3_DRAMRST#
+V3.3S
+V0.75S
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DDR3 SO-DIMM_0/SO-DIMM_1
Size
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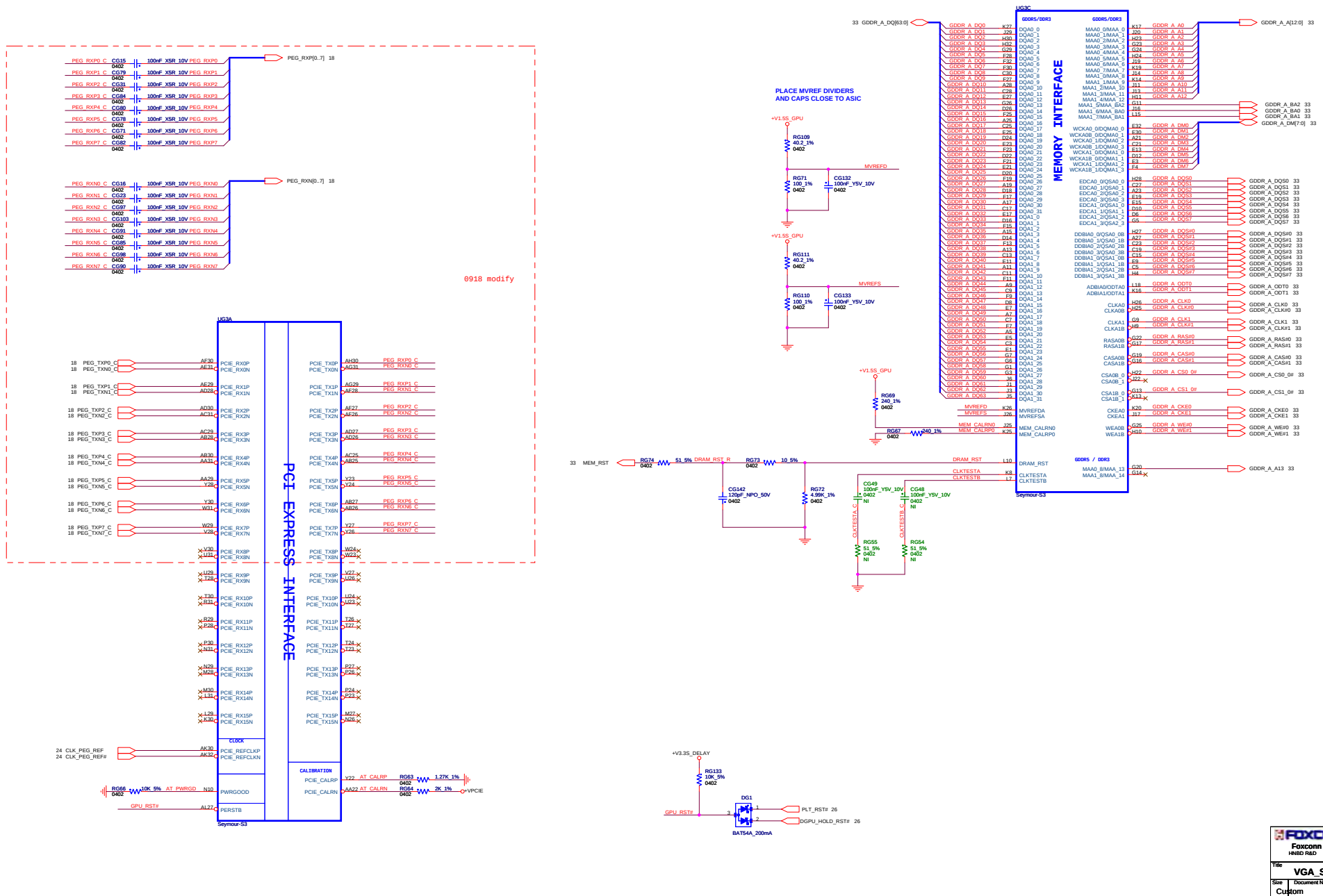
Document Number
CHICAGO
Rev
MV
Sheet 29 of 43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PEG_RXP1_C CG79 0402 100nF_X5R_10V PEG_RXP1
PEG_RXP2_C CG31 0402 100nF_X5R_10V PEG_RXP2
PEG_RXP3_C CG84 0402 100nF_X5R_10V PEG_RXP3
PEG_RXP4_C CG80 0402 100nF_X5R_10V PEG_RXP4
PEG_RXP5_C CG78 0402 100nF_X5R_10V PEG_RXP5
PEG_RXP6_C CG71 0402 100nF_X5R_10V PEG_RXP6
PEG_RXP7_C CG82 0402 100nF_X5R_10V PEG_RXP7
PEG_RXP[0..7] 18
PEG_RXN0_C CG16 0402 100nF_X5R_10V PEG_RXN0
PEG_RXN1_C CG23 0402 100nF_X5R_10V PEG_RXN1
PEG_RXN2_C CG97 0402 100nF_X5R_10V PEG_RXN2
PEG_RXN3_C CG103 0402 100nF_X5R_10V PEG_RXN3
PEG_RXN4_C CG91 0402 100nF_X5R_10V PEG_RXN4
PEG_RXN5_C CG85 0402 100nF_X5R_10V PEG_RXN5
PEG_RXN6_C CG98 0402 100nF_X5R_10V PEG_RXN6
PEG_RXN7_C CG90 0402 100nF_X5R_10V PEG_RXN7
PEG_RXN[0..7] 18
0918 modify
UG3A
PCI EXPRESS INTERFACE
18 PEG_TXP0_C
18 PEG_TXN0_C
AE30 PCIE_RX0P
AE31 PCIE_RX0N
PCIE_TX0P AH30 PEG_RXP0_C
PCIE_TX0N AG31 PEG_RXN0_C
18 PEG_TXP1_C
18 PEG_TXN1_C
AE29 PCIE_RX1P
AD28 PCIE_RX1N
PCIE_TX1P AG29 PEG_RXP1_C
PCIE_TX1N AF28 PEG_RXN1_C
18 PEG_TXP2_C
18 PEG_TXN2_C
AD30 PCIE_RX2P
AC31 PCIE_RX2N
PCIE_TX2P AF27 PEG_RXP2_C
PCIE_TX2N AF26 PEG_RXN2_C
18 PEG_TXP3_C
18 PEG_TXN3_C
AC29 PCIE_RX3P
AB28 PCIE_RX3N
PCIE_TX3P AD27 PEG_RXP3_C
PCIE_TX3N AD26 PEG_RXN3_C
18 PEG_TXP4_C
18 PEG_TXN4_C
AB30 PCIE_RX4P
AA31 PCIE_RX4N
PCIE_TX4P AC25 PEG_RXP4_C
PCIE_TX4N AB25 PEG_RXN4_C
18 PEG_TXP5_C
18 PEG_TXN5_C
AA29 PCIE_RX5P
Y28 PCIE_RX5N
PCIE_TX5P Y23 PEG_RXP5_C
PCIE_TX5N Y24 PEG_RXN5_C
18 PEG_TXP6_C
18 PEG_TXN6_C
Y30 PCIE_RX6P
W31 PCIE_RX6N
PCIE_TX6P AB27 PEG_RXP6_C
PCIE_TX6N AB26 PEG_RXN6_C
18 PEG_TXP7_C
18 PEG_TXN7_C
W29 PCIE_RX7P
V28 PCIE_RX7N
PCIE_TX7P Y27 PEG_RXP7_C
PCIE_TX7N Y26 PEG_RXN7_C
V30 PCIE_RX8P
U31 PCIE_RX8N
PCIE_TX8P W24
PCIE_TX8N W23
U29 PCIE_RX9P
T28 PCIE_RX9N
PCIE_TX9P V27
PCIE_TX9N V26
T30 PCIE_RX10P
R31 PCIE_RX10N
PCIE_TX10P U24
PCIE_TX10N U23
R29 PCIE_RX11P
P28 PCIE_RX11N
PCIE_TX11P T26
PCIE_TX11N T27
P30 PCIE_RX12P
N31 PCIE_RX12N
PCIE_TX12P T24
PCIE_TX12N T23
N29 PCIE_RX13P
M28 PCIE_RX13N
PCIE_TX13P P27
PCIE_TX13N P26
M30 PCIE_RX14P
L31 PCIE_RX14N
PCIE_TX14P P24
PCIE_TX14N P23
L29 PCIE_RX15P
K30 PCIE_RX15N
PCIE_TX15P M27
PCIE_TX15N N26
CLOCK
24 CLK_PEG_REF
24 CLK_PEG_REF#
AK30 PCIE_REFCLKP
AK32 PCIE_REFCLKN
RG66 0402 10K_5% AT_PWRGD
N10 PWRGOOD
GPU_RST#
A127 PERSTB
CALIBRATION
PCIE_CALRP Y22 AT_CALRP
PCIE_CALRN AA22 AT_CALRN
RG63 0402 1.27K_1%
RG64 0402 2K_1%
+VPCIE
Seymour-S3
PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC
+V1.5S_GPU
RG109 40.2_1% 0402
MVREFD
RG71 100_1% 0402
CG132 100nF_Y5V_10V 0402
+V1.5S_GPU
RG111 40.2_1% 0402
MVREFS
RG110 100_1% 0402
CG133 100nF_Y5V_10V 0402
+V1.5S_GPU
RG69 240_1% 0402
RG67 0402 240_1%
33 MEM_RST
RG74 0402 51_5% DRAM_RST_R
RG73 0402 10_5%
DRAM_RST
CG142 120pF_NPO_50V 0402
RG72 4.99K_1% 0402
CG49 100nF_Y5V_10V 0402 NI
CG48 100nF_Y5V_10V 0402 NI
CLKTEST_A_C
CLKTEST_B_C
RG55 51_5% 0402 NI
RG54 51_5% 0402 NI
+V3.3S_DELAY
RG133 10K_5% 0402
GPU_RST#
DG1
BAT54A_200mA
PLT_RST# 26
DGPU_HOLD_RST# 26
UG3C
MEMORY INTERFACE
GDDR5/DDR3
33 GDDR_A_DQ[63:0]
GDDR_A_DQ0 K27
GDDR_A_DQ1 J29
GDDR_A_DQ2 H30
GDDR_A_DQ3 H32
GDDR_A_DQ4 G29
GDDR_A_DQ5 F29
GDDR_A_DQ6 F32
GDDR_A_DQ7 F30
GDDR_A_DQ8 C30
GDDR_A_DQ9 F27
GDDR_A_DQ10 A29
GDDR_A_DQ11 C28
GDDR_A_DQ12 E27
GDDR_A_DQ13 G26
GDDR_A_DQ14 D26
GDDR_A_DQ15 F25
GDDR_A_DQ16 A25
GDDR_A_DQ17 C25
GDDR_A_DQ18 E25
GDDR_A_DQ19 D24
GDDR_A_DQ20 E23
GDDR_A_DQ21 F23
GDDR_A_DQ22 D22
GDDR_A_DQ23 F21
GDDR_A_DQ24 E21
GDDR_A_DQ25 D20
GDDR_A_DQ26 F19
GDDR_A_DQ27 A19
GDDR_A_DQ28 D18
GDDR_A_DQ29 F17
GDDR_A_DQ30 A17
GDDR_A_DQ31 C17
GDDR_A_DQ32 E17
GDDR_A_DQ33 D16
GDDR_A_DQ34 F15
GDDR_A_DQ35 A15
GDDR_A_DQ36 D14
GDDR_A_DQ37 F13
GDDR_A_DQ38 A13
GDDR_A_DQ39 C13
GDDR_A_DQ40 E11
GDDR_A_DQ41 A11
GDDR_A_DQ42 C11
GDDR_A_DQ43 F11
GDDR_A_DQ44 A9
GDDR_A_DQ45 C9
GDDR_A_DQ46 F9
GDDR_A_DQ47 D8
GDDR_A_DQ48 E7
GDDR_A_DQ49 A7
GDDR_A_DQ50 C7
GDDR_A_DQ51 F7
GDDR_A_DQ52 A5
GDDR_A_DQ53 E5
GDDR_A_DQ54 C3
GDDR_A_DQ55 E1
GDDR_A_DQ56 G7
GDDR_A_DQ57 G6
GDDR_A_DQ58 G1
GDDR_A_DQ59 G3
GDDR_A_DQ60 J6
GDDR_A_DQ61 J1
GDDR_A_DQ62 J3
GDDR_A_DQ63 J5
MVREFD K26
MVREFS J26
MEM_CALRN0 J25
MEM_CALRP0 K25
DQA0_0 DQA0_1 DQA0_2 DQA0_3 DQA0_4 DQA0_5 DQA0_6 DQA0_7 DQA0_8 DQA0_9 DQA0_10 DQA0_11 DQA0_12 DQA0_13 DQA0_14 DQA0_15 DQA0_16 DQA0_17 DQA0_18 DQA0_19 DQA0_20 DQA0_21 DQA0_22 DQA0_23 DQA0_24 DQA0_25 DQA0_26 DQA0_27 DQA0_28 DQA0_29 DQA0_30 DQA0_31
DQA1_0 DQA1_1 DQA1_2 DQA1_3 DQA1_4 DQA1_5 DQA1_6 DQA1_7 DQA1_8 DQA1_9 DQA1_10 DQA1_11 DQA1_12 DQA1_13 DQA1_14 DQA1_15 DQA1_16 DQA1_17 DQA1_18 DQA1_19 DQA1_20 DQA1_21 DQA1_22 DQA1_23 DQA1_24 DQA1_25 DQA1_26 DQA1_27 DQA1_28 DQA1_29 DQA1_30 DQA1_31
MVREFDA
MVREFSA
MEM_CALRN0
MEM_CALRP0
DRAM_RST L10
CLKTESTA K8
CLKTESTB L7
MAA0_0/MAA_0 K17
MAA0_1/MAA_1 J20
MAA0_2/MAA_2 H23
MAA0_3/MAA_3 G23
MAA0_4/MAA_4 G24
MAA0_5/MAA_5 H24
MAA0_6/MAA_6 J19
MAA0_7/MAA_7 K19
MAA1_0/MAA_8 J14
MAA1_1/MAA_9 K14
MAA1_2/MAA_10 J11
MAA1_3/MAA_11 J13
MAA1_4/MAA_12 H11
MAA1_5/MAA_BA2 G11
MAA1_6/MAA_BA0 J16
MAA1_7/MAA_BA1 L15
WCKA0_0/DQMA0_0 E32
WCKA0B_0/DQMA0_1 E30
WCKA0_1/DQMA0_2 A21
WCKA0B_1/DQMA0_3 C21
WCKA1_0/DQMA1_0 E13
WCKA1B_0/DQMA1_1 D12
WCKA1_1/DQMA1_2 E3
WCKA1B_1/DQMA1_3 F4
EDCA0_0/QSA0_0 H28
EDCA0_1/QSA0_1 C27
EDCA0_2/QSA0_2 A23
EDCA0_3/QSA0_3 E19
EDCA1_0/QSA1_0 E15
EDCA1_1/QSA1_1 D10
EDCA1_2/QSA1_2 D6
EDCA1_3/QSA2_3 G5
DDBIA0_0/QSA0_0B H27
DDBIA0_1/QSA0_1B A27
DDBIA0_2/QSA0_2B C23
DDBIA0_3/QSA0_3B C19
DDBIA1_0/QSA1_0B C15
DDBIA1_1/QSA1_1B E9
DDBIA1_2/QSA1_2B C5
DDBIA1_3/QSA1_3B H4
ADBIA0/ODTA0 L18
ADBIA1/ODTA1 K16
CLKA0 H26
CLKA0B H25
CLKA1 G9
CLKA1B H9
RASA0B G22
RASA1B G17
CASA0B G19
CASA1B G16
CSA0B_0 H22
CSA0B_1 J22
CSA1B_0 G13
CSA1B_1 K13
CKEA0 K20
CKEA1 J17
WEA0B G25
WEA1B H10
GDDR5 / DDR3
MAA0_8/MAA_13 G20
MAA1_8/MAA_14 G14
GDDR_A_A[12:0] 33
GDDR_A_BA2 33
GDDR_A_BA0 33
GDDR_A_BA1 33
GDDR_A_DM[7:0] 33
GDDR_A_DQS0 33
GDDR_A_DQS1 33
GDDR_A_DQS2 33
GDDR_A_DQS3 33
GDDR_A_DQS4 33
GDDR_A_DQS5 33
GDDR_A_DQS6 33
GDDR_A_DQS7 33
GDDR_A_DQS#0 33
GDDR_A_DQS#1 33
GDDR_A_DQS#2 33
GDDR_A_DQS#3 33
GDDR_A_DQS#4 33
GDDR_A_DQS#5 33
GDDR_A_DQS#6 33
GDDR_A_DQS#7 33
GDDR_A_ODT0 33
GDDR_A_ODT1 33
GDDR_A_CLK0 33
GDDR_A_CLK0# 33
GDDR_A_CLK1 33
GDDR_A_CLK1# 33
GDDR_A_RAS#0 33
GDDR_A_RAS#1 33
GDDR_A_CAS#0 33
GDDR_A_CAS#1 33
GDDR_A_CS0_0# 33
GDDR_A_CS1_0# 33
GDDR_A_CKE0 33
GDDR_A_CKE1 33
GDDR_A_WE#0 33
GDDR_A_WE#1 33
GDDR_A_A13 33
Seymour-S3
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Title
VGA_S3 (PCI-E) 1/3
Size Custom
Document Number CHICAGO
Rev MV
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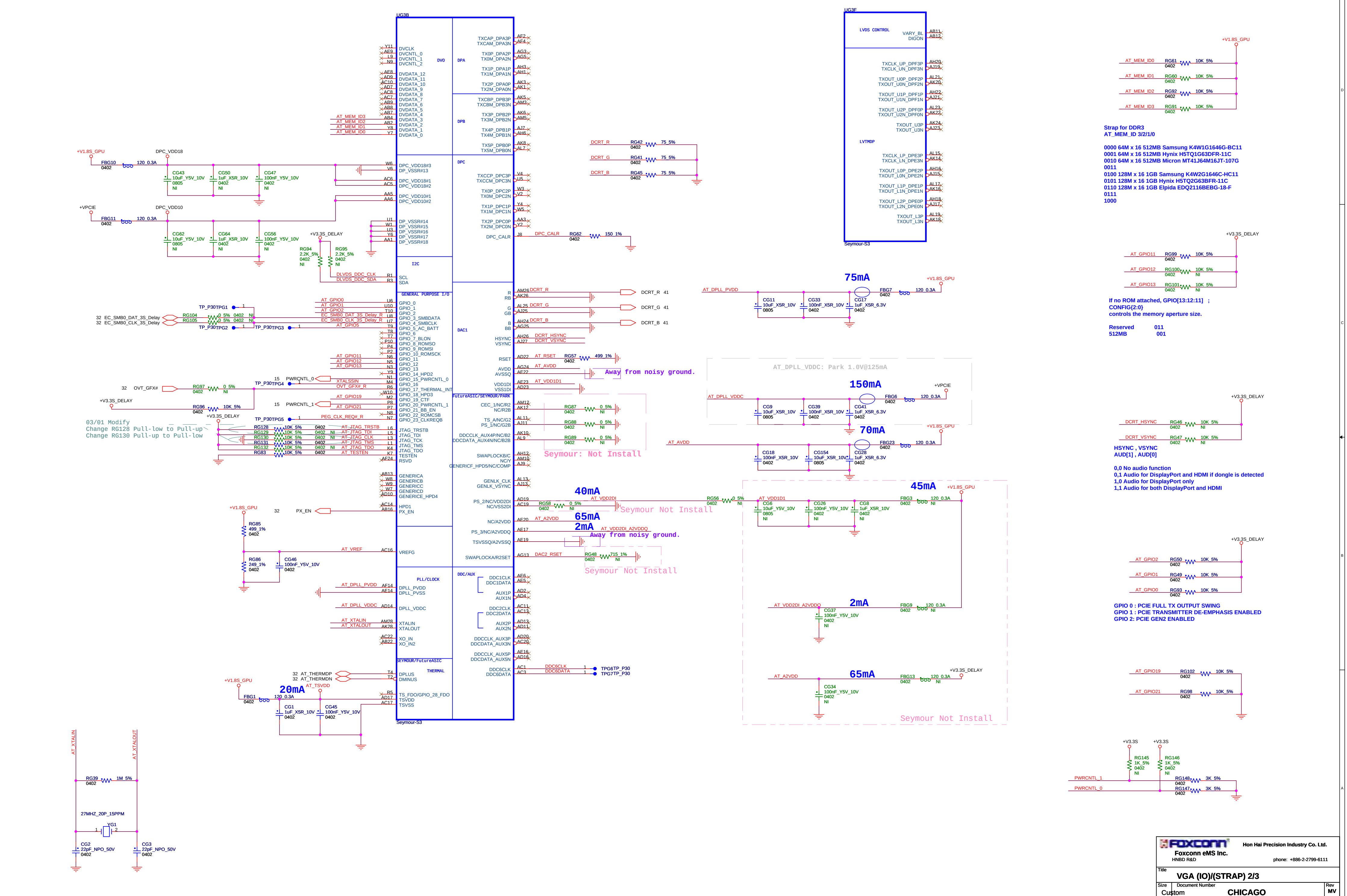
Sheet 30 of 43



UG3B
Seymour-S3
UG3F
LVDS CONTROL
LVTMDP
DVO
DPA
DPB
DPC
I2C
GENERAL PURPOSE I/O
DAC1
FutureASIC/SEYMOUR/PARK
PLL/CLOCK
DDC/AUX
SEYMOUR/FutureASIC
THERMAL
Strap for DDR3
AT_MEM_ID 3/2/1/0
0000 64M x 16 512MB Samsung K4W1G1646G-BC11
0001 64M x 16 512MB Hynix H5TQ1G63DFR-11C
0010 64M x 16 512MB Micron MT41J64M16JT-107G
0011
0100 128M x 16 1GB Samsung K4W2G1646C-HC11
0101 128M x 16 1GB Hynix H5TQ2G63BFR-11C
0110 128M x 16 1GB Elpida EDQ2116BEBG-18-F
0111
1000
If no ROM attached, GPIO[13:12:11] ;
CONFIG[2:0}
controls the memory aperture size.
Reserved 011
512MB 001
AT_DPLL_VDDC: Park 1.0V@125mA
75mA
150mA
70mA
45mA
40mA
65mA
2mA
20mA
Away from noisy ground.
Seymour: Not Install
Seymour Not Install
HSYNC , VSYNC
AUD[1] , AUD[0]
0,0 No audio function
0,1 Audio for DisplayPort and HDMI if dongle is detected
1,0 Audio for DisplayPort only
1,1 Audio for both DisplayPort and HDMI
GPIO 0 : PCIE FULL TX OUTPUT SWING
GPIO 1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED
GPIO 2: PCIE GEN2 ENABLED
03/01 Modify
Change RG128 Pull-low to Pull-up
Change RG130 Pull-up to Pull-low
27MHZ_20P_15PPM

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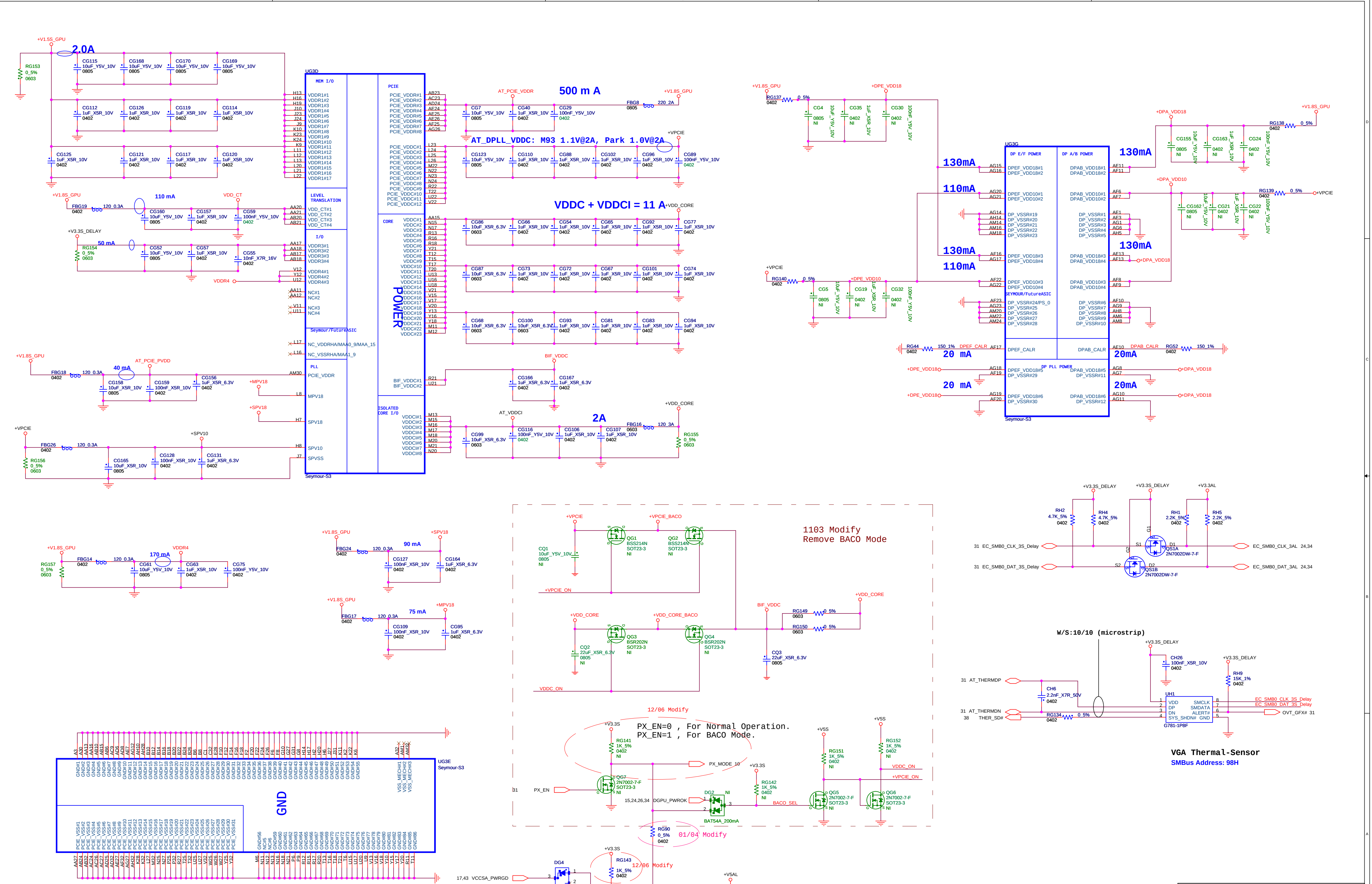
Page Modified: Tuesday, March 08, 2011 | Sheet 31 of 43


2.0A
500 m A
AT_DPLL_VDDC: M93 1.1V@2A, Park 1.0V@2A
VDDC + VDDCI = 11 A
110 mA
50 mA
40 mA
2A
90 mA
75 mA
170 mA
130mA
110mA
20 mA
20mA
UG3D
MEM I/O
PCIE
LEVEL TRANSLATION
I/O
CORE
POWER
PLL
ISOLATED CORE I/O
Seymour-S3
UG3G
DP E/F POWER
DP A/B POWER
DP PLL POWER
UG3E
GND
1103 Modify
Remove BACO Mode
12/06 Modify
PX_EN=0 , For Normal Operation.
PX_EN=1 , For BACO Mode.
01/04 Modify
W/S:10/10 (microstrip)
VGA Thermal-Sensor
SMBus Address: 98H
G781-1P8F
EC_SMB0_CLK_3S_Delay
EC_SMB0_DAT_3S_Delay
EC_SMB0_CLK_3AL
EC_SMB0_DAT_3AL
OVT_GFX#
DGPU_PWR_EN#
DGPU_PWR_EN_Q
VCCSA_PWRGD
PX_MODE
PX_EN
DGPU_PWROK
BACO_SEL

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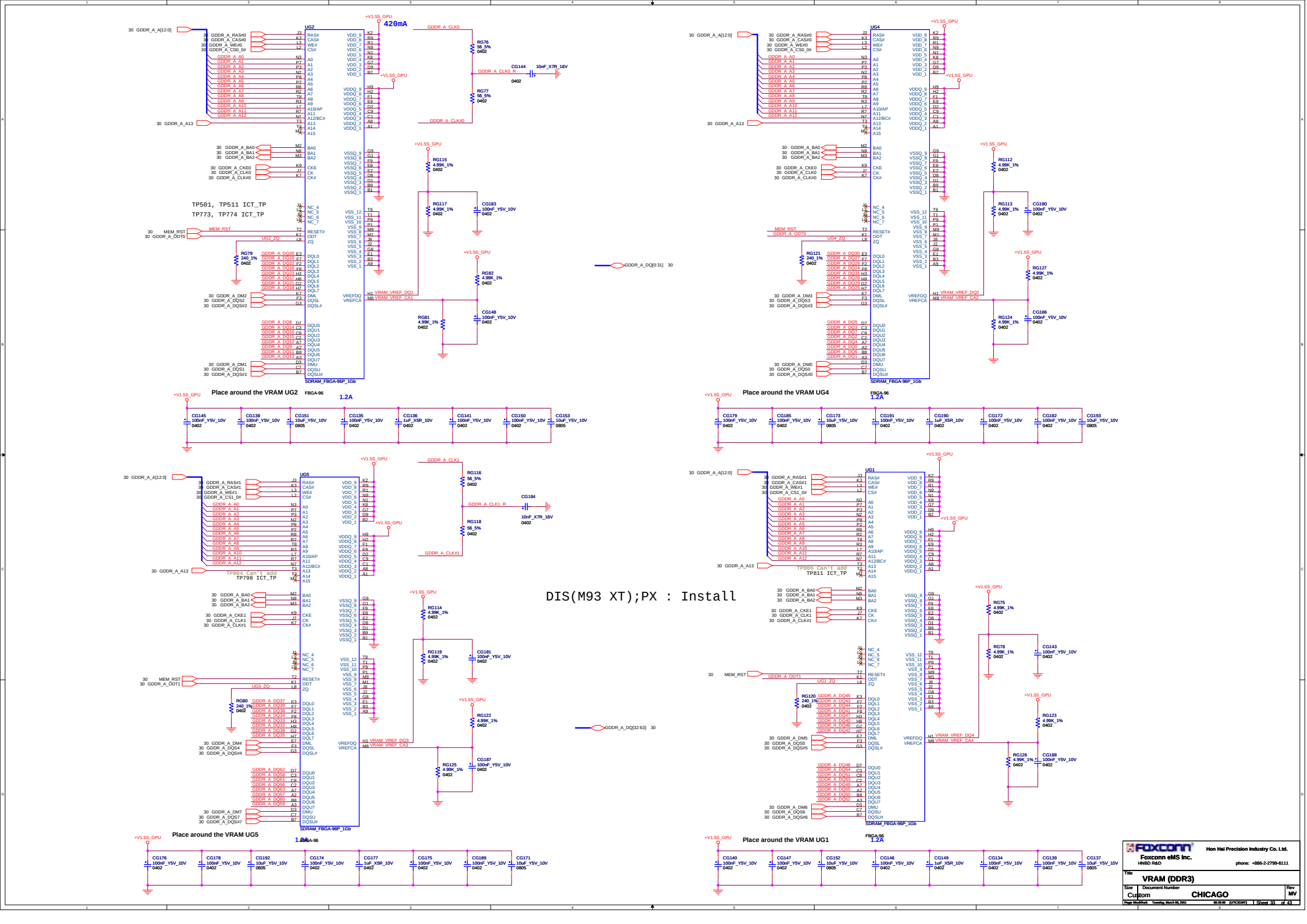
Size: Custom | Document Number: CHICAGO | Rev: MV

Page Modified: Tuesday, March 08, 2011 | Sheet 32 of 43


UG2
420mA
+V1.5S_GPU
GDDR_A_CLK0
GDDR_A_CLK0_R
GDDR_A_CLK#0
RG76 56_5% 0402
RG77 56_5% 0402
CG144 10nF_X7R_16V 0402
RG115 4.99K_1% 0402
RG117 4.99K_1% 0402
CG183 100nF_Y5V_10V 0402
RG82 4.99K_1% 0402
RG81 4.99K_1% 0402
CG148 100nF_Y5V_10V 0402
RG79 240_1% 0402
TP501, TP511 ICT_TP
TP773, TP774 ICT_TP
MEM_RST
UG2_ZQ
GDDR_A_DQ[0:31]
GDDR_A_DM2
GDDR_A_DQS2
GDDR_A_DQS#2
GDDR_A_DM1
GDDR_A_DQS1
GDDR_A_DQS#1
VRAM_VREF_DQ1
VRAM_VREF_CA1
SDRAM_FBGA-96P_1Gb
Place around the VRAM UG2
FBGA-96
1.2A
UG4
RG112 4.99K_1% 0402
RG113 4.99K_1% 0402
CG180 100nF_Y5V_10V 0402
RG127 4.99K_1% 0402
RG124 4.99K_1% 0402
CG186 100nF_Y5V_10V 0402
RG121 240_1% 0402
UG4_ZQ
GDDR_A_DM3
GDDR_A_DQS3
GDDR_A_DQS#3
GDDR_A_DM0
GDDR_A_DQS0
GDDR_A_DQS#0
VRAM_VREF_DQ2
VRAM_VREF_CA2
Place around the VRAM UG4
CG145 100nF_Y5V_10V 0402
CG138 100nF_Y5V_10V 0402
CG151 10uF_Y5V_10V 0805
CG135 100nF_Y5V_10V 0402
CG136 1uF_X5R_10V 0402
CG141 100nF_Y5V_10V 0402
CG150 100nF_Y5V_10V 0402
CG153 10uF_Y5V_10V 0805
CG179 100nF_Y5V_10V 0402
CG185 100nF_Y5V_10V 0402
CG173 10uF_Y5V_10V 0805
CG191 100nF_Y5V_10V 0402
CG190 1uF_X5R_10V 0402
CG172 100nF_Y5V_10V 0402
CG182 100nF_Y5V_10V 0402
CG192 10uF_Y5V_10V 0805
UG5
GDDR_A_CLK1
GDDR_A_CLK1_R
GDDR_A_CLK#1
RG116 56_5% 0402
RG118 56_5% 0402
CG184 10nF_X7R_16V 0402
RG114 4.99K_1% 0402
RG119 4.99K_1% 0402
CG181 100nF_Y5V_10V 0402
RG122 4.99K_1% 0402
RG125 4.99K_1% 0402
CG187 100nF_Y5V_10V 0402
RG80 240_1% 0402
UG5_ZQ
GDDR_A_DM4
GDDR_A_DQS4
GDDR_A_DQS#4
GDDR_A_DM7
GDDR_A_DQS7
GDDR_A_DQS#7
VRAM_VREF_DQ3
VRAM_VREF_CA3
SDRAM_FBGA-96P_1Gb
Place around the VRAM UG5
FBGA-96
1.2A
UG1
RG75 4.99K_1% 0402
RG78 4.99K_1% 0402
CG143 100nF_Y5V_10V 0402
RG123 4.99K_1% 0402
RG126 4.99K_1% 0402
CG188 100nF_Y5V_10V 0402
RG120 240_1% 0402
UG1_ZQ
GDDR_A_DM5
GDDR_A_DQS5
GDDR_A_DQS#5
GDDR_A_DM6
GDDR_A_DQS6
GDDR_A_DQS#6
VRAM_VREF_DQ4
VRAM_VREF_CA4
Place around the VRAM UG1
CG176 100nF_Y5V_10V 0402
CG178 100nF_Y5V_10V 0402
CG192 10uF_Y5V_10V 0805
CG174 100nF_Y5V_10V 0402
CG177 1uF_X5R_10V 0402
CG175 100nF_Y5V_10V 0402
CG189 100nF_Y5V_10V 0402
CG171 10uF_Y5V_10V 0805
CG140 100nF_Y5V_10V 0402
CG147 100nF_Y5V_10V 0402
CG152 10uF_Y5V_10V 0805
CG146 100nF_Y5V_10V 0402
CG149 1uF_X5R_10V 0402
CG134 100nF_Y5V_10V 0402
CG139 100nF_Y5V_10V 0402
CG137 10uF_Y5V_10V 0805
DIS(M93 XT);PX : Install
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HNBD R&D
Hon Hai Precision Industry Co. Ltd.
phone: +886-2-2799-6111
Title
VRAM (DDR3)
Size
Custom
Document Number
CHICAGO
Rev
MV
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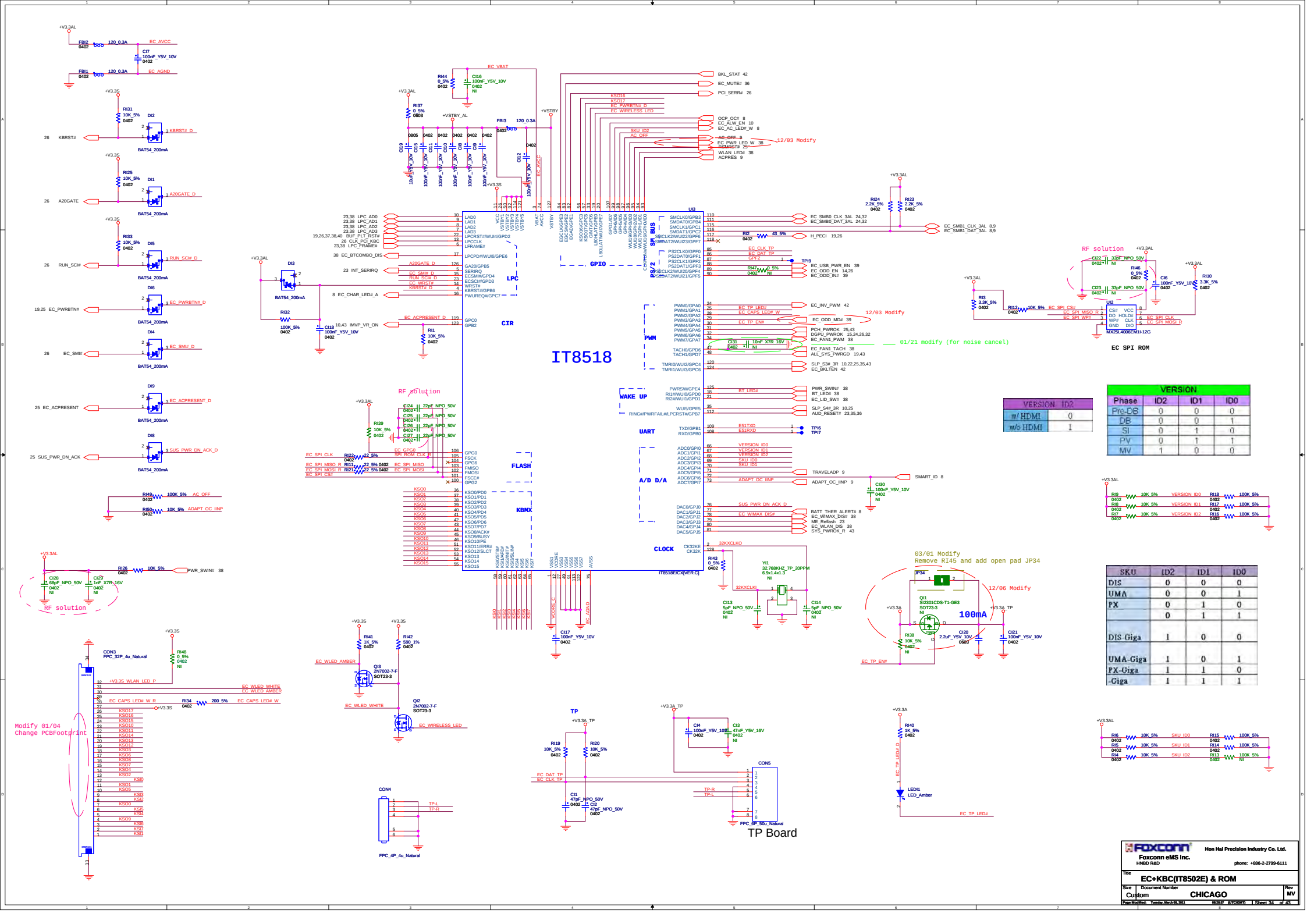
Sheet 33 of 43


IT8518
IT8518E/CX[VER.C]
LPC
CIR
FLASH
KBMX
GPIO
SMB
PWM
WAKE UP
UART
A/D D/A
CLOCK
RF solution
01/21 modify (for noise cancel)
12/03 Modify
03/01 Modify
Remove RI45 and add open pad JP34
12/06 Modify
100mA
Modify 01/04
Change PCBFootprint
TP Board
EC SPI ROM
MX25L4006EM1I-12G
VERSION
Phase ID2 ID1 ID0
Pre-DB 0 0 0
DB 0 0 1
SI 0 1 0
PV 0 1 1
MV 1 0 0
VERSION_ID2
w/ HDMI 0
w/o HDMI 1
SKU ID2 ID1 ID0
DIS 0 0 0
UMA 0 0 1
PX 0 1 0
0 1 1
DIS-Giga 1 0 0
UMA-Giga 1 0 1
PX-Giga 1 1 0
-Giga 1 1 1
CON3
FPC_32P_4u_Natural
CON4
FPC_4P_4u_Natural
CON5
FPC_6P_50u_Natural
Foxconn
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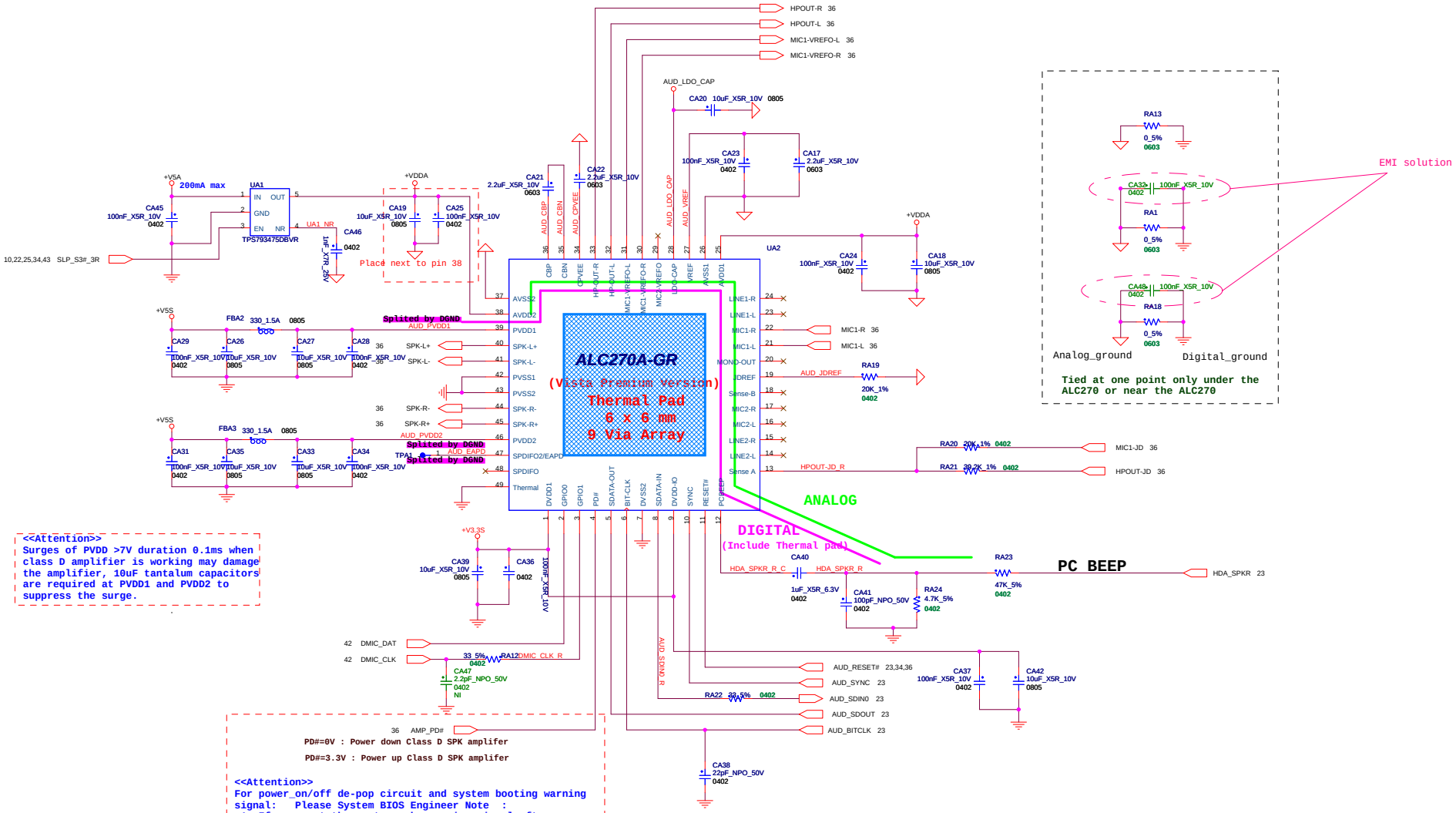
EC+KBC(IT8502E) & ROM
Size
Custom
Document Number
CHICAGO
Rev
MV
Sheet 34 of 43



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Size: Custom	Document Number:
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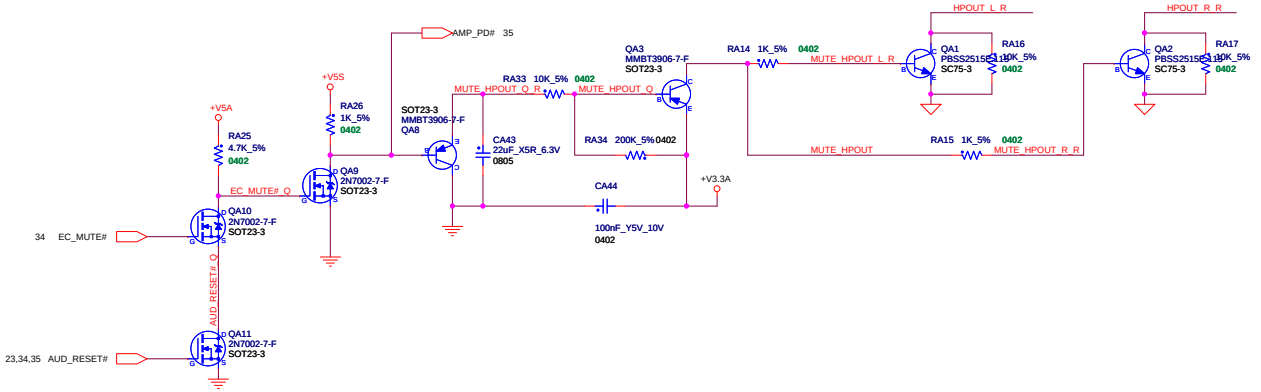
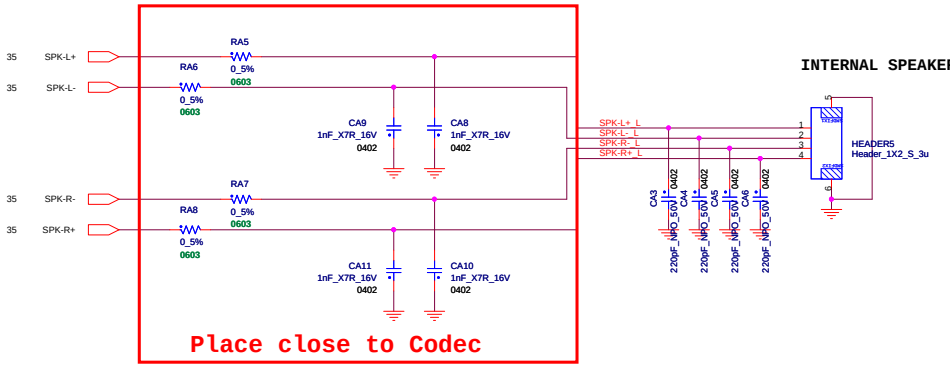
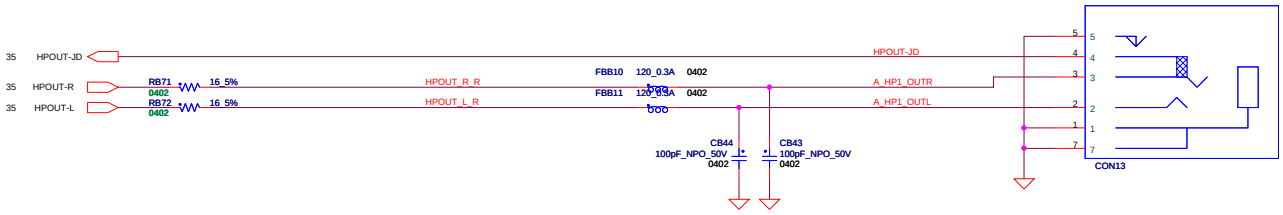
Mute



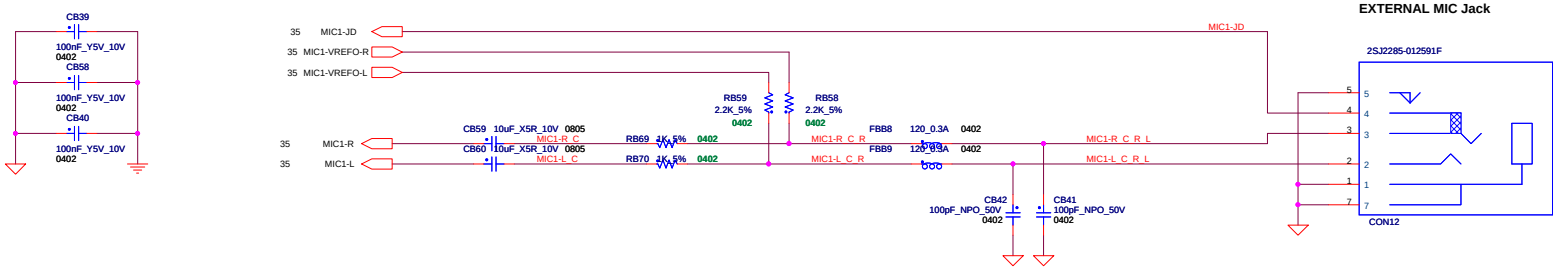
INTERNAL SPEAKER



HEADPHONE Jack



EXTERNAL MIC Jack



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Title: Audio (JACK+AMP+SPK+Mute)

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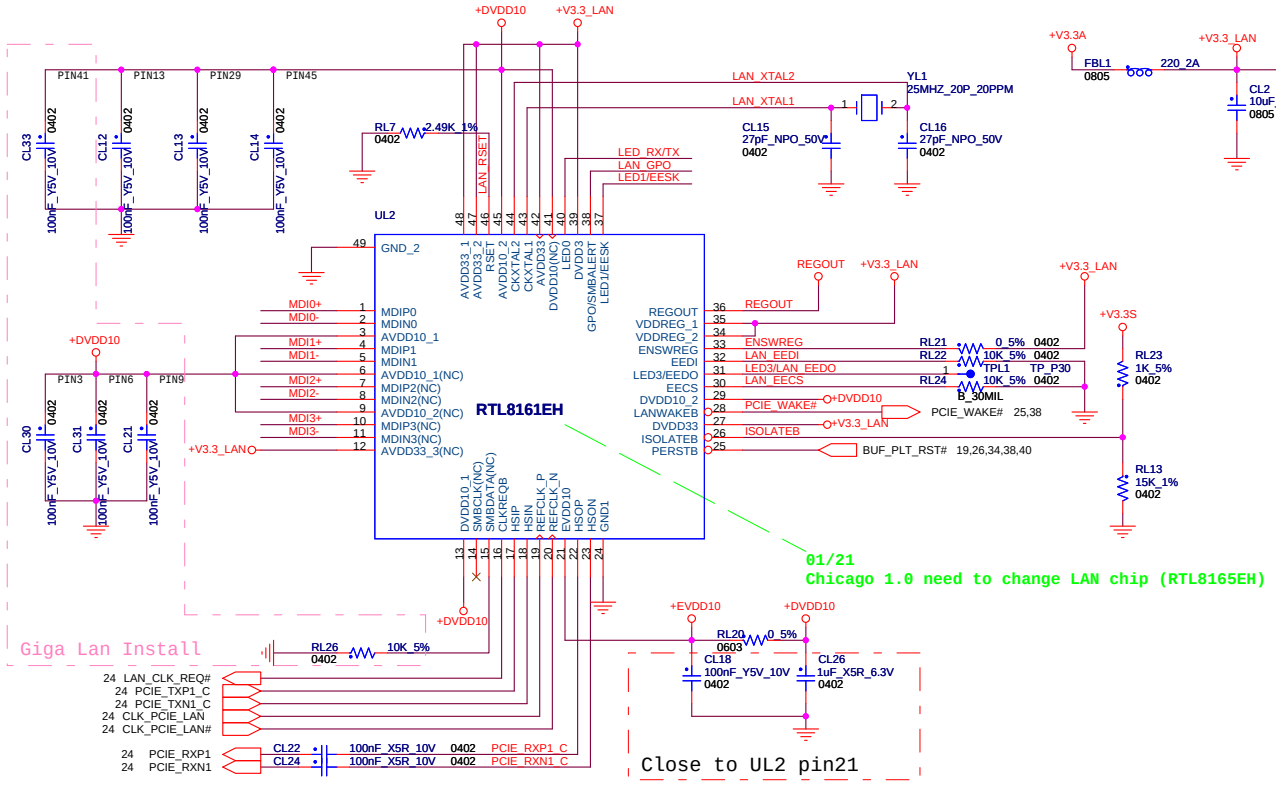
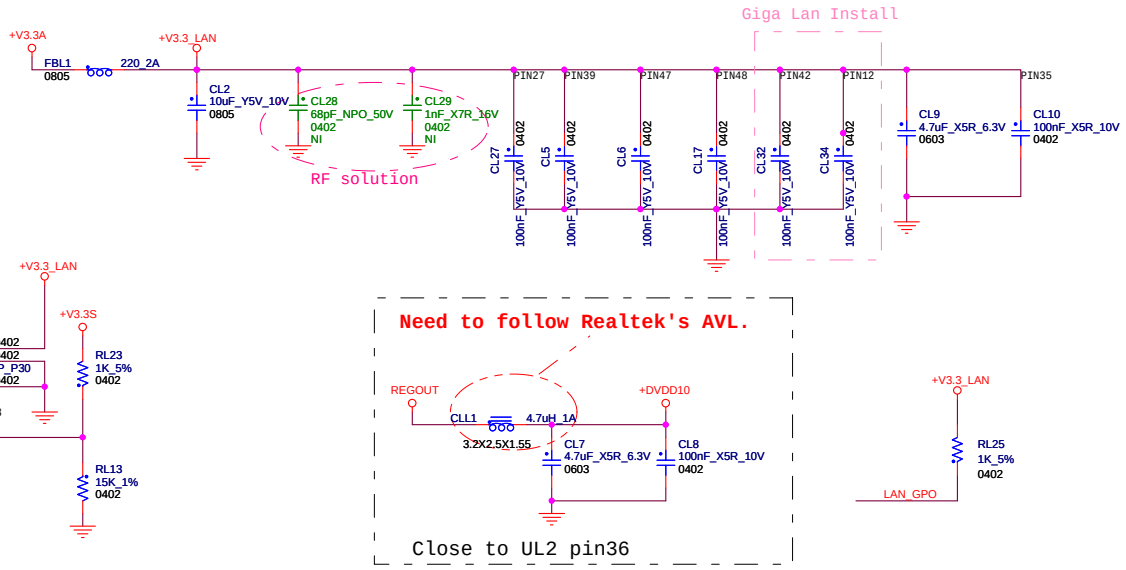
Page Modified: Tuesday, March 08, 2011 08:29:09 (UTC/GMT) | Sheet 36 of 43

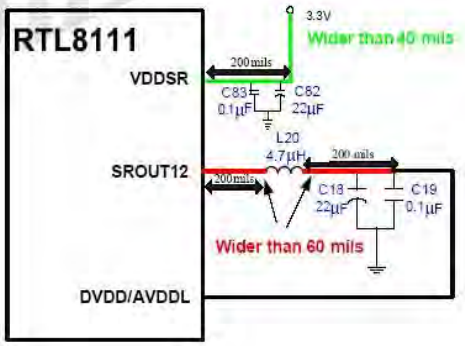


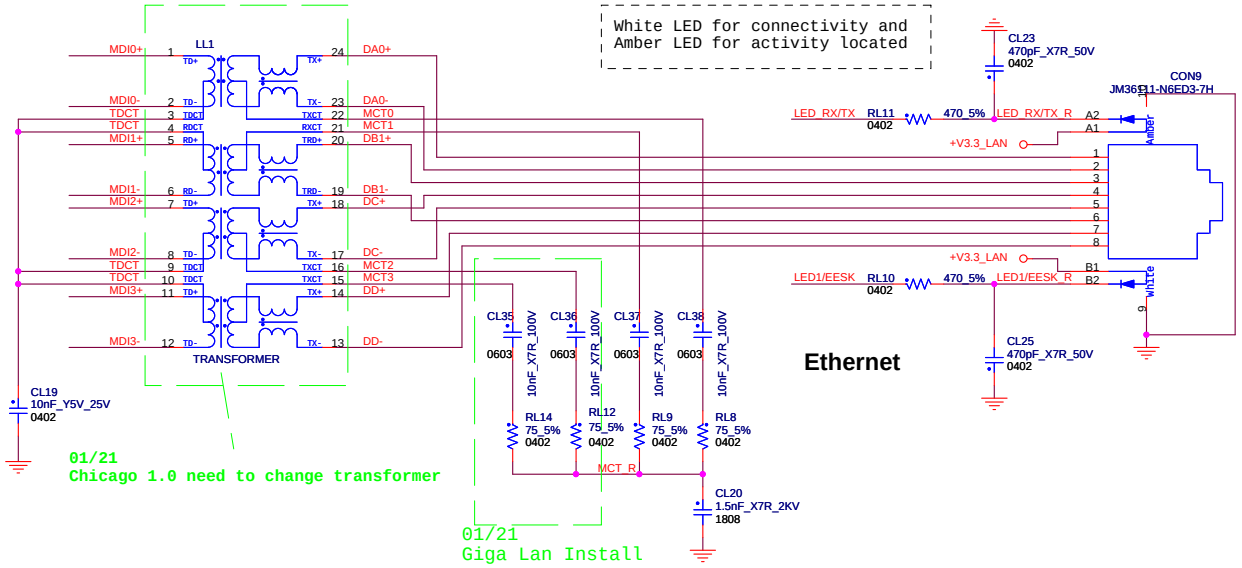


7.1. PCB Layout

- The input 3.3V power trace connected to the VDDSR pin should be wider than 40mils.
- The bulk de-coupling capacitors (C82 and C83) should be placed within 200mils (0.5cm) of the VDDSR pin to prevent input voltage overshoot.
- The output power trace out of the SROUT12 pin should be wider than 60mils.
- Keep L20 within 200mils (0.5cm) of the SROUT12 pin.
- Keep C18 and C19 within 200mils (0.5cm) of L20 to ensure stable output power and better power efficiency.
- Both C18 and C82 are strongly recommended to be ceramic capacitors.

Note: Violation of the above rules will damage the IC.





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Title	LAN (RTL8165EH)
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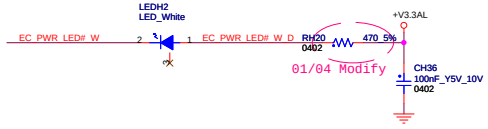
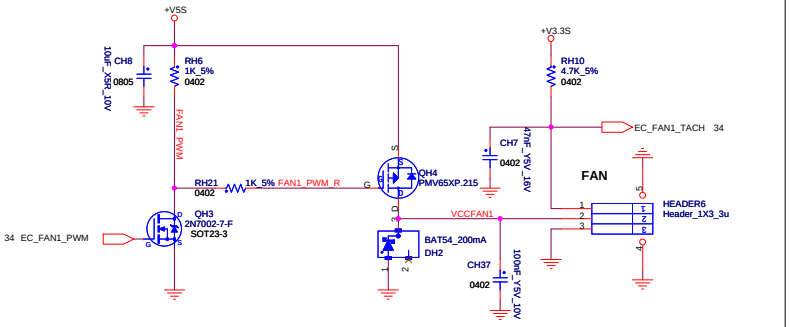
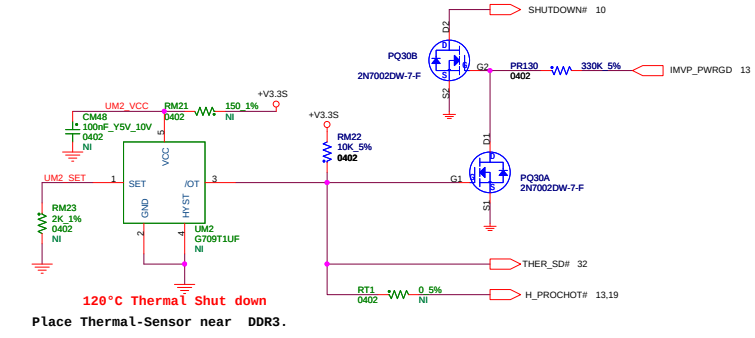
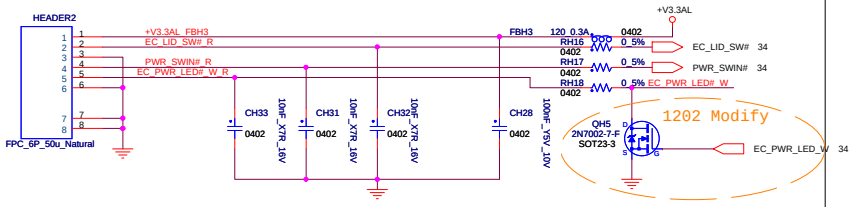
Page Modified: Tuesday, March 08, 2011 08:28:59 (UTC/GMT)	Sheet 37 of 43

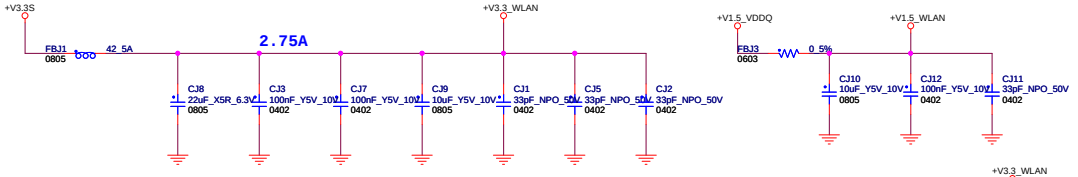


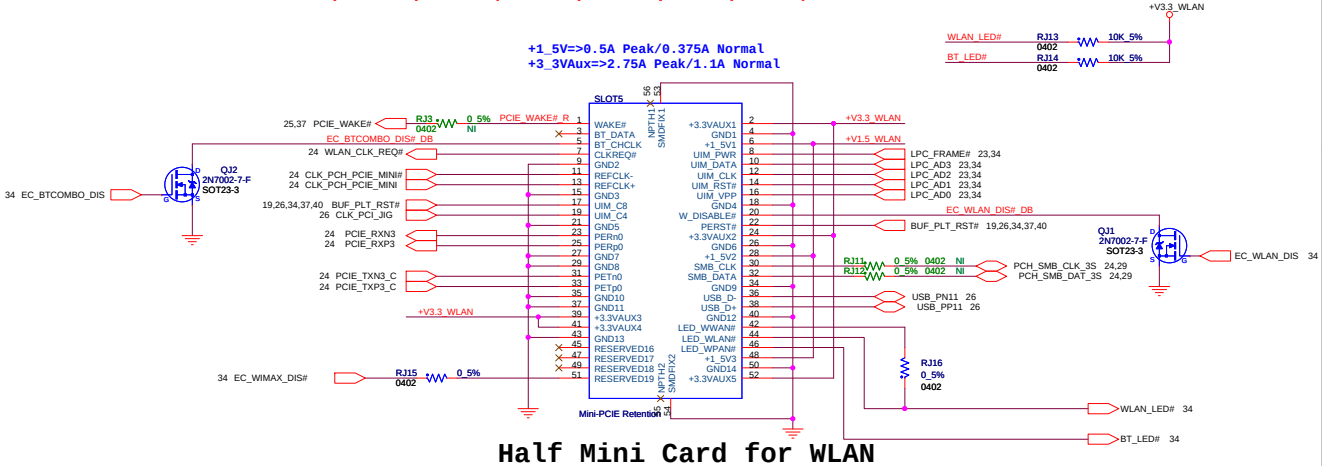




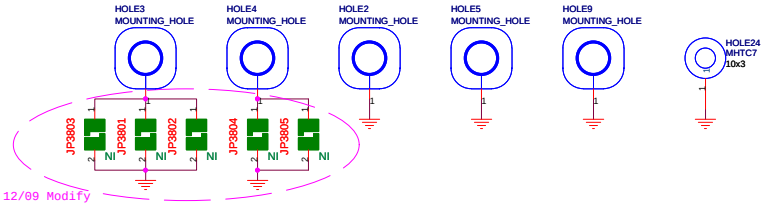
PWR Board CONN.

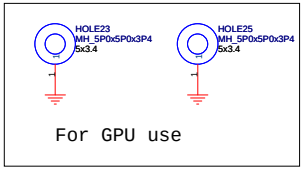


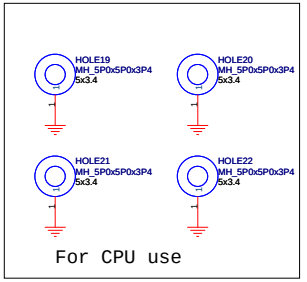




Half Mini Card for WLAN

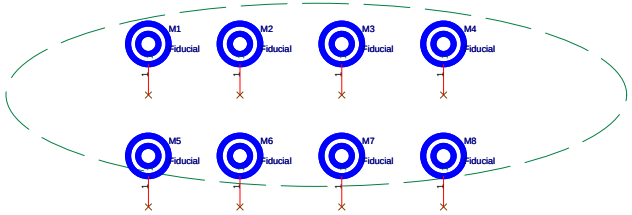






Mounting HOLE

02/09 Modify
Change PCBfootprint from FIDUCIAL_1P_3P_B to FIDUCIAL_MARK



Fiducial Mark

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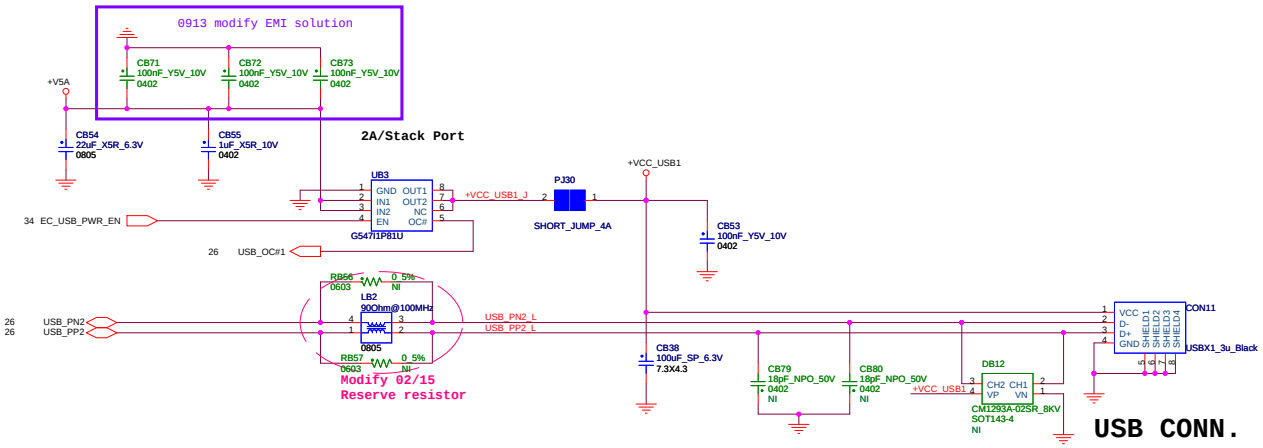
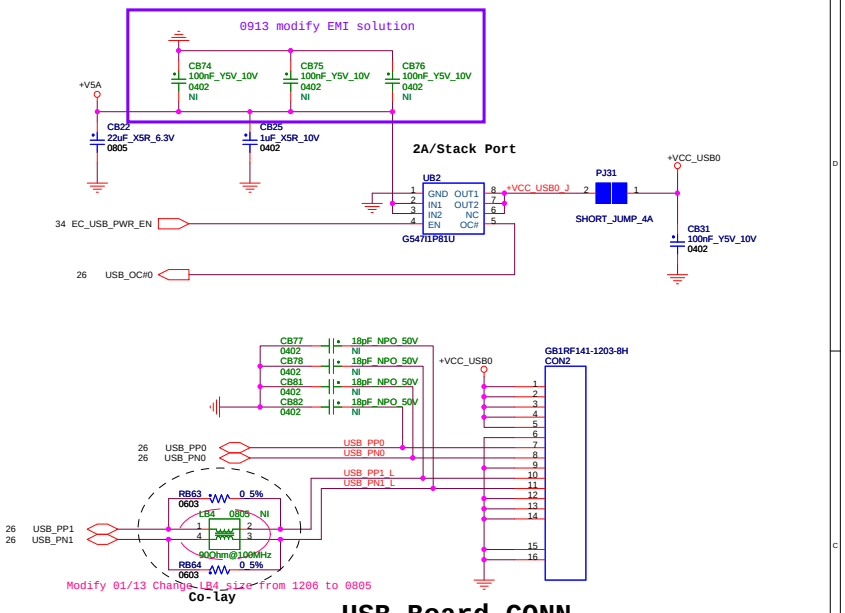
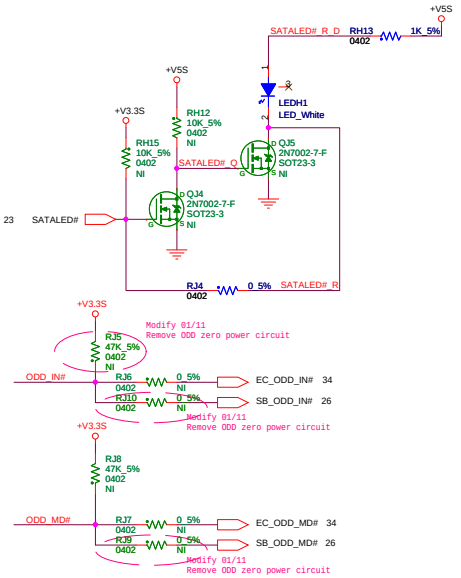
Page Modified: Tuesday, March 08, 2011 08:29:09 (UTC/GMT) | Sheet 38 of 43

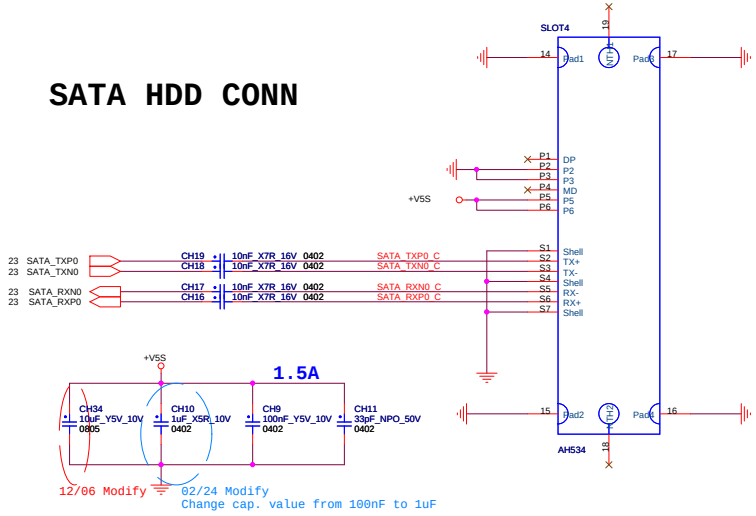




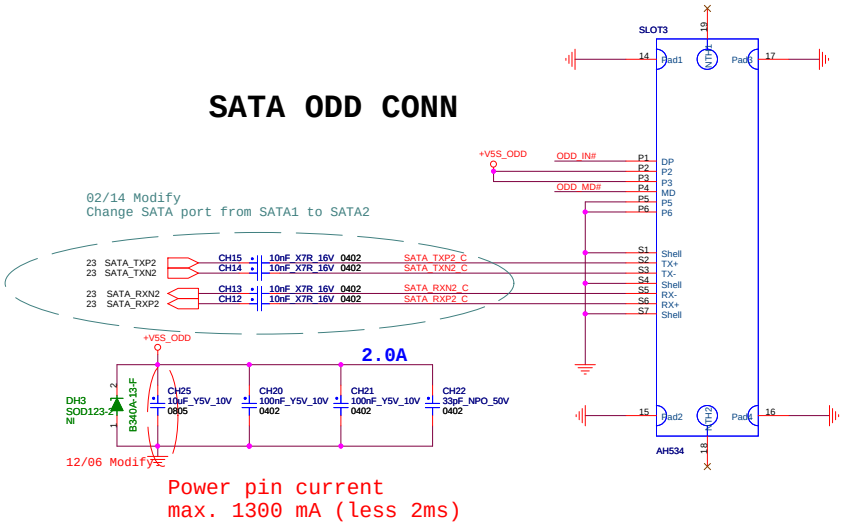
HDD/ODD Status LED



SATA HDD CONN



SATA ODD CONN



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Title	USBX2/USB DB CONN./SATA CONN.
Size: Custom	Document Number: CHICAGO
Rev	MV
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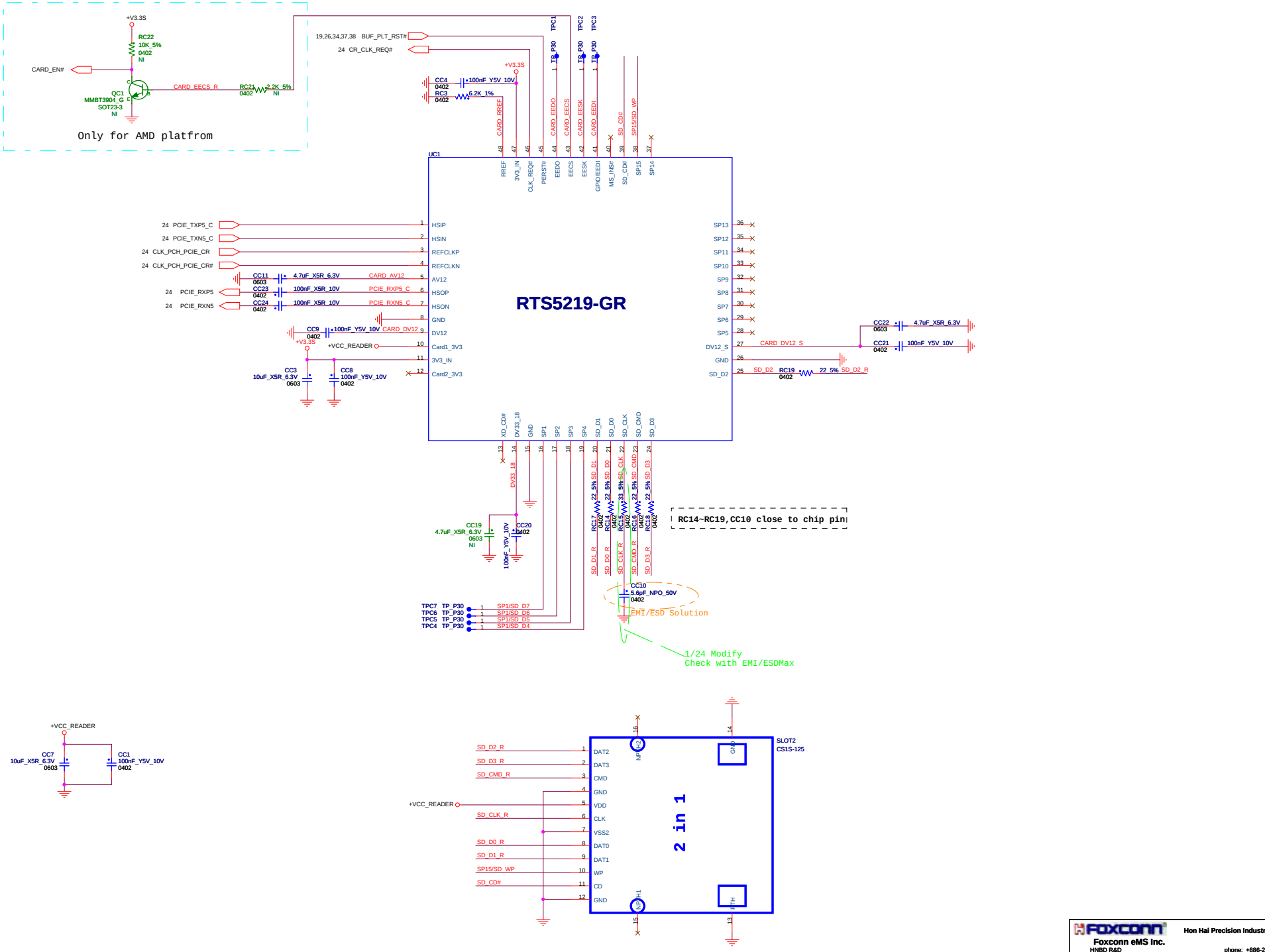

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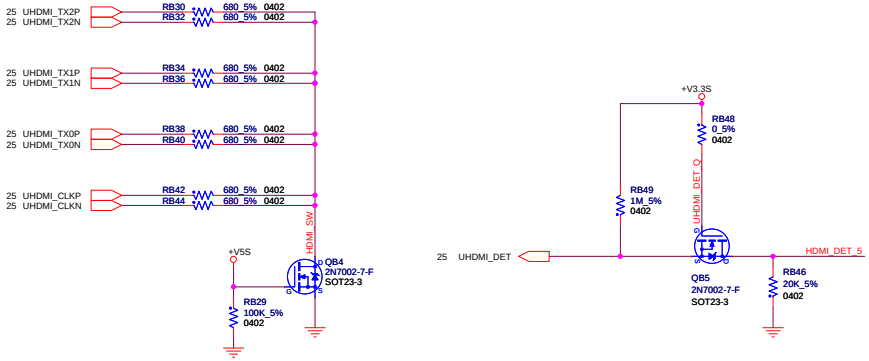
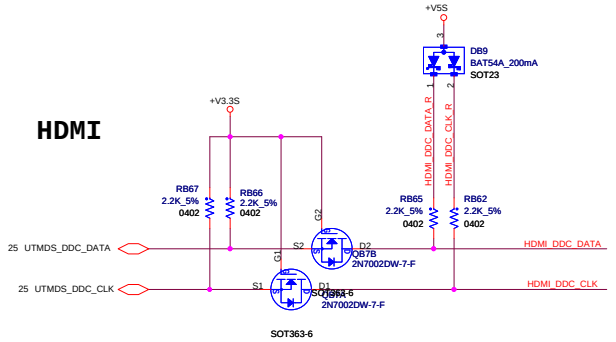
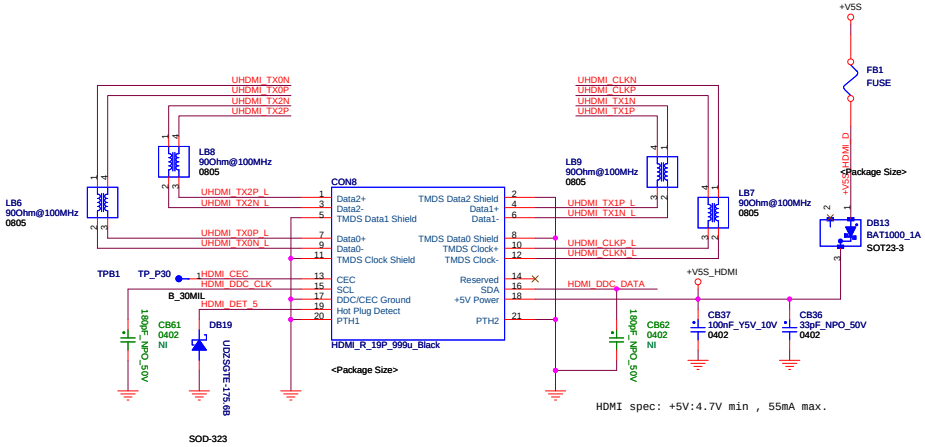
Title	Card Reader
Size: Custom	Document Number	Rev: MV
Page Modified: Tuesday, March 08, 2011 08:29:09 (UTC/GMT)	Sheet 40 of 43



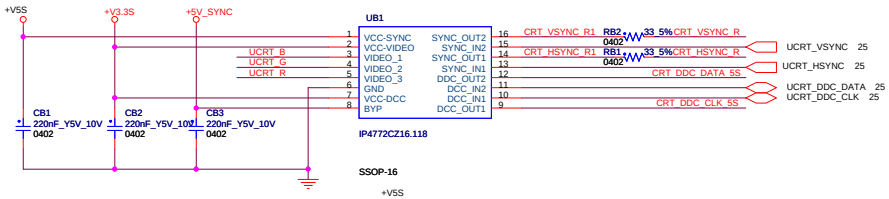
HDMI

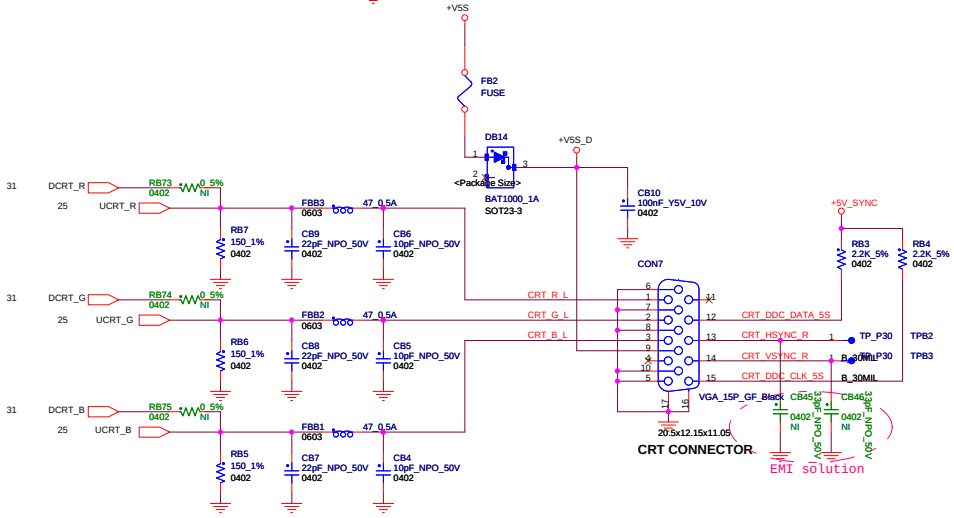




HDMI spec: +5V:4.7V min , 55mA max.

CRT





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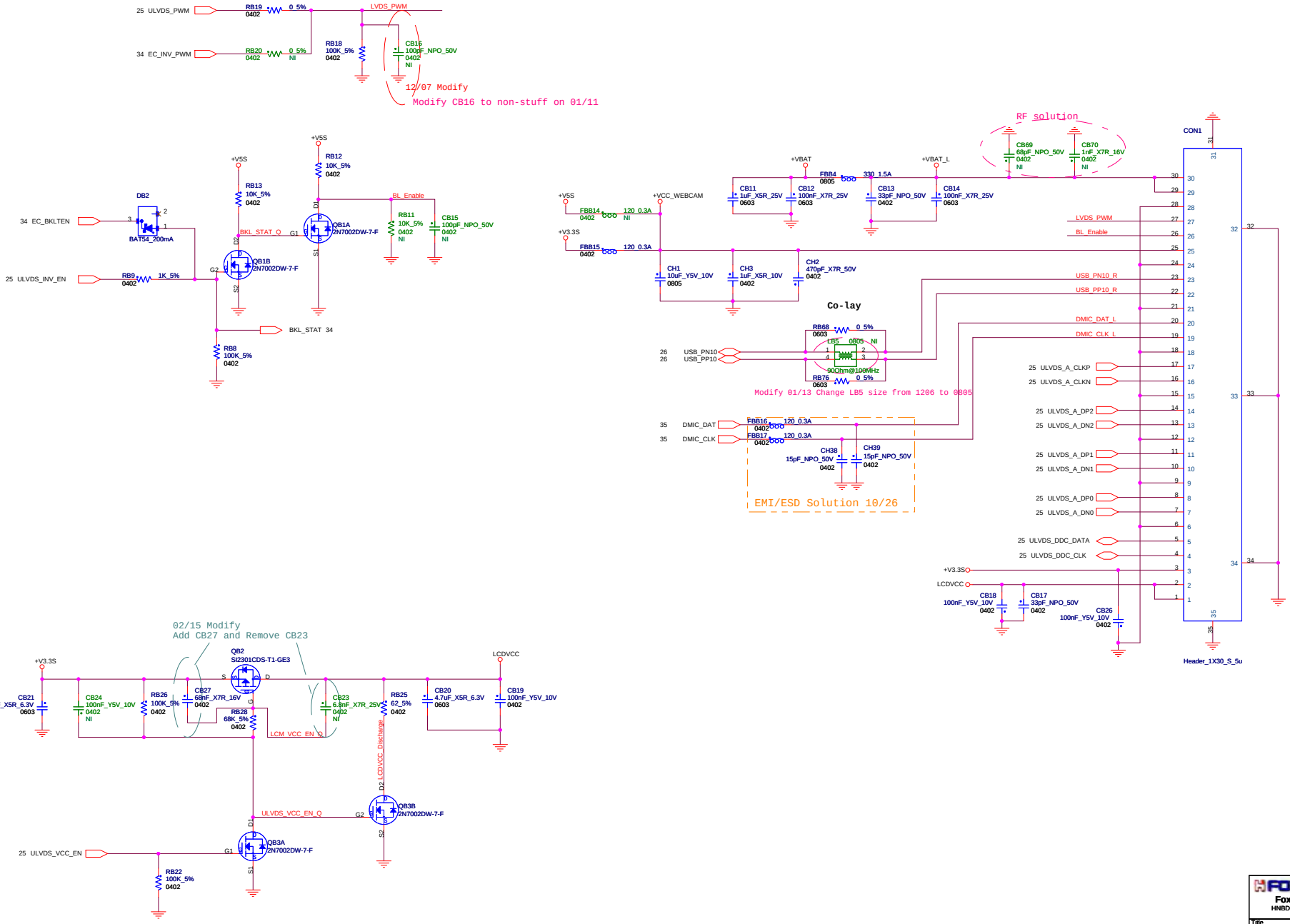

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Title: LVDS&Webcam

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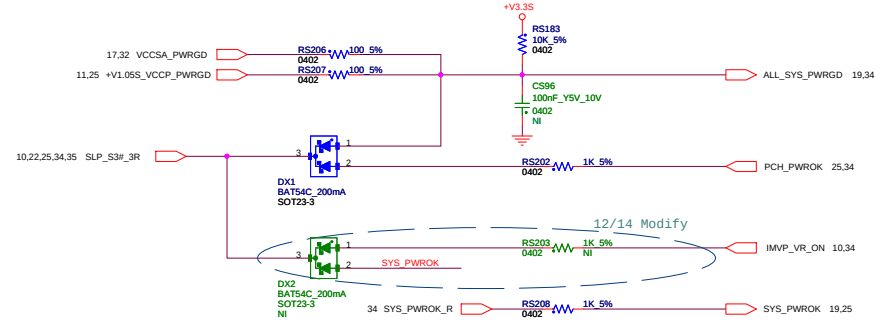

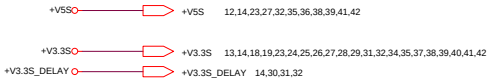

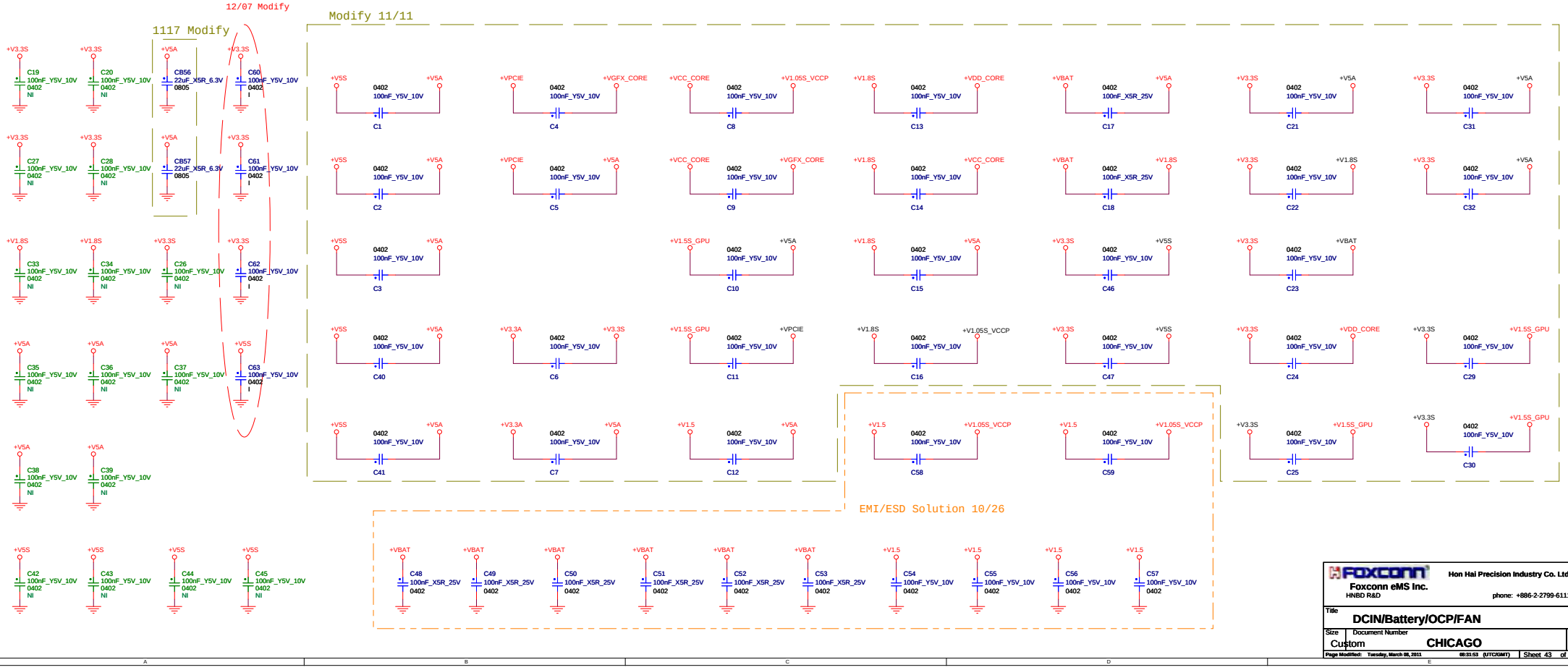

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HNBD R&D	phone: +886-2-2799-6111	
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