

GA102 DT SKU P-BOARD

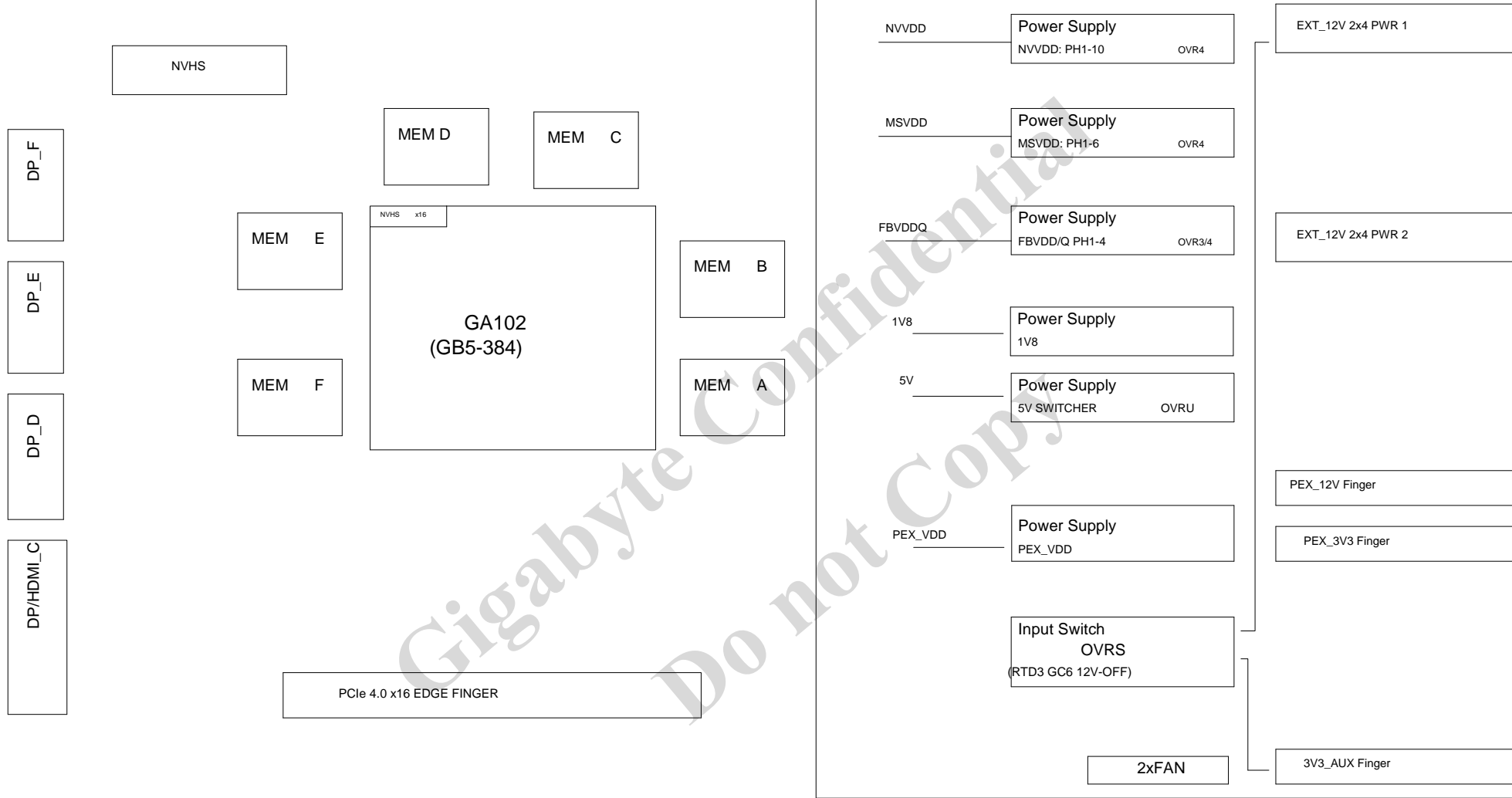
350W , FH Std PCB, 384b, GDDR6X x8
DP + DP + DP + HDMI/DP

TABLE OF CONTENTS

Page	Description	Page	Description	Page	Description
1	Table of Contents	26	MISC: THERMAL, JTAG, GPIO	51	PS: NVVDD Controller_OVR8
2	BLOCK DIAGRAM	27	IFPA UNUSED, IFPB UNUSED	52	PS: NVVDD PH1 (PWM1)
3	PCI EXPRESS	28	IFPE DP	53	PS: NVVDD PH2 (PWM6)
4	MEMORY: GPU PARTITION A/B	29	IFPD DP	54	PS: NVVDD PH3 (PWM3) and PH4 (PWM3)
5	MEMORY: FBA PARTITION[31:0]	30	IFPC HDMI/DP	55	PS: NVVDD PH5 (PWM7) and PH7 (PWM8)
6	MEMORY: FBA PARTITION[63:32]	31	IFPF DP	56	PS: NVVDD PH6 (PWM7)
7	MEMORY: FBB PARTITION[31:0]	32	MISC. ROM, STRAPS	57	PS: NVVDD PH8(PWM5) and PH9(PWM2)
8	MEMORY: FBB PARTITION[63:31]	33	MISC. XTAL, PLL	58	PS: NVVDD PH10 (PWM4)
9	MEMORY: GPU PARTITION C/D	34	PS: 5V	59	Colayout Notes
10	MEMORY: FBC PARTITION[31:0]	35	PS: PEX_DVDD and 1V8	60	BLANK
11	MEMORY: FBC PARTITION[63:32]	36	BLANK	61	PS: NVVDD OUTPUT CAP(TOP)
12	MEMORY: FBD PARTITION[31:0]	37	PS: FBVDD Controller OVR3	62	BLANK
13	MEMORY: FBD PARTITION[63:32]	38	PS: FBVDDQ OVR4	63	PS: INPUT SWITCH RTD3
14	MEMORY: GPU PARTITION E/F	39	PS: FBVDD PH1	64	BLANK
15	MEMORY: FBE PARTITION[31:0]	40	PS: FBVDD PH3	65	PS: INPUTS, FILTERING, and, MONITORING
16	MEMORY: FBE PARTITION[63:32]	41	PS: FBVDD PH2	66	PS: HOT UNPLUG
17	MEMORY: FBF PARTITION[31:0]	42	PS: FBVDD PH4	67	PS: Discrete Power Steering
18	MEMORY: FBF PARTITION[63:32]	43	PS: FBVDD OUTPUT CAP	68	PS: PREFILTER
19	GPU GND, RFUs & RSVD	44	PS: MSVDD CONTROLLER	69	PS: PREFILTER B
20	GPU POWERS	45	PS: MSVDD PH1	70	Sequence: 5V, 1V8, 3V3_SEQ
21	GPU: NVVDD DECOUPLING	46	PS: MSVDD PH2	71	Sequence: NV, PEX, FB EN
22	GPU: FBVDD DECOUPLING	47	PS: MSVDD PH3 and PH5	72	Sequence: 3V3 MONITOR
23	GPU: MSVDD DECOUPLING	48	PS: MSVDD PH4 and PH6	73	Sequence: MISC
24	BLANK	49	PS: MSVDD OUTPUT CAP(TOP)	74	MISC: LED & FAN
25	NVHS x16	50	BLANK	75	RGBW LED REF

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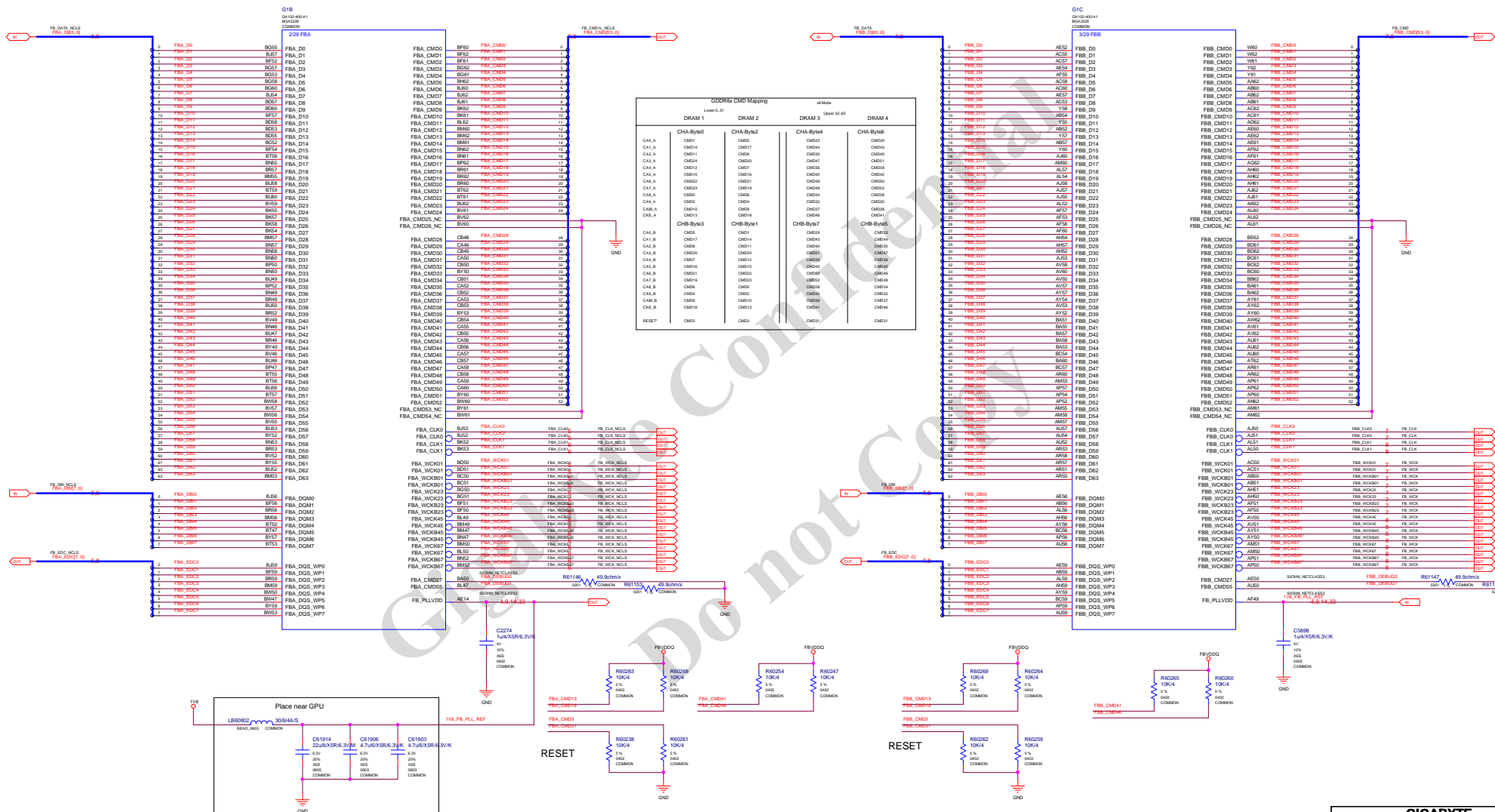
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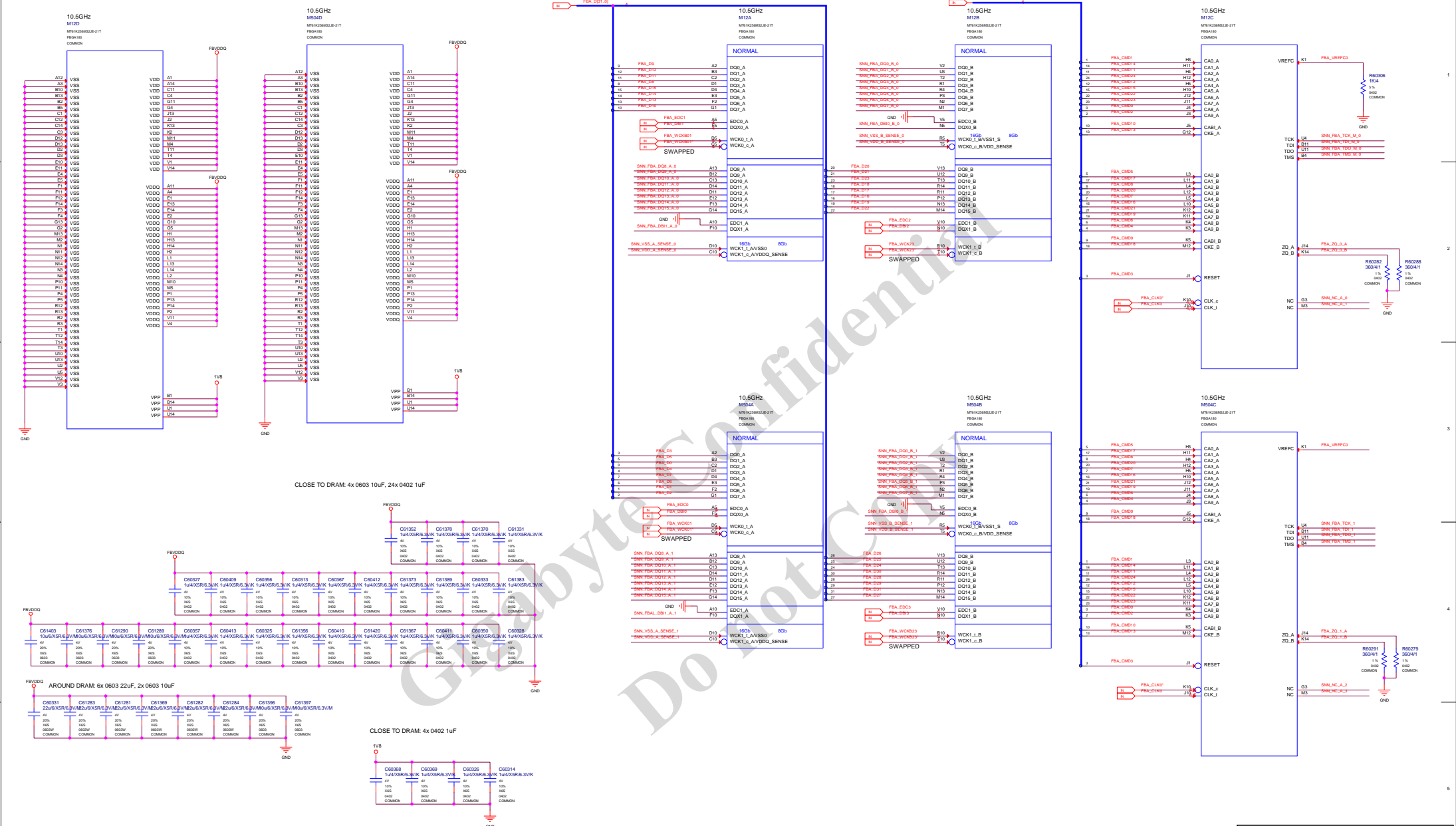
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ASSEMBLY PAGE DETAIL
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File	PCIE			
Size	Custom	Document Number	GV-N3090AORUS M-24GD	
Date	Tuesday, August 25, 2020	Sheet	2	of 82



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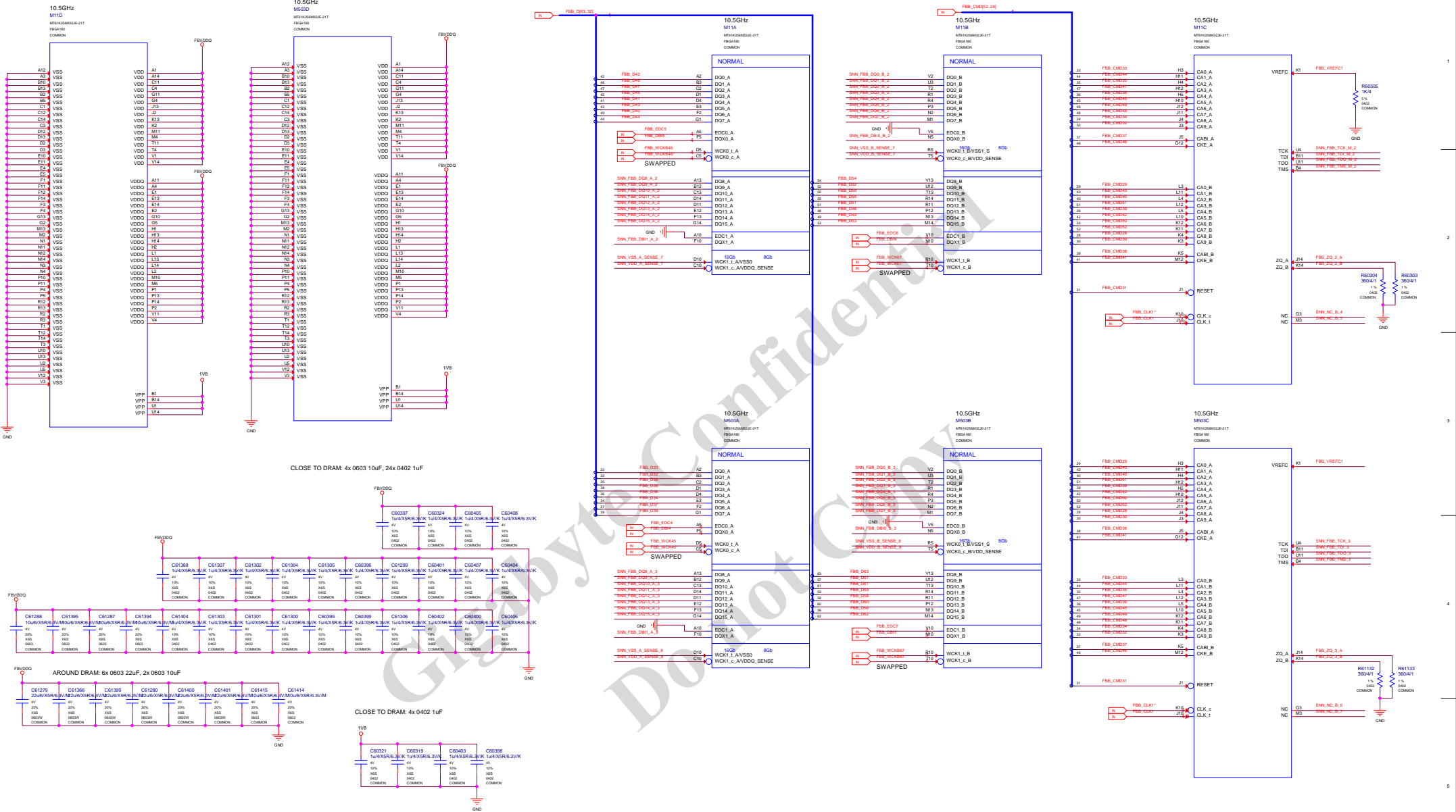
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MEMORY: FBA PARTITION 31..0

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File	PCIE	Rev	1.01
Size	Document Number	GV-N3090AORUS M-24GD	
Date	Tuesday, August 25, 2020	Sheet	5 of 82



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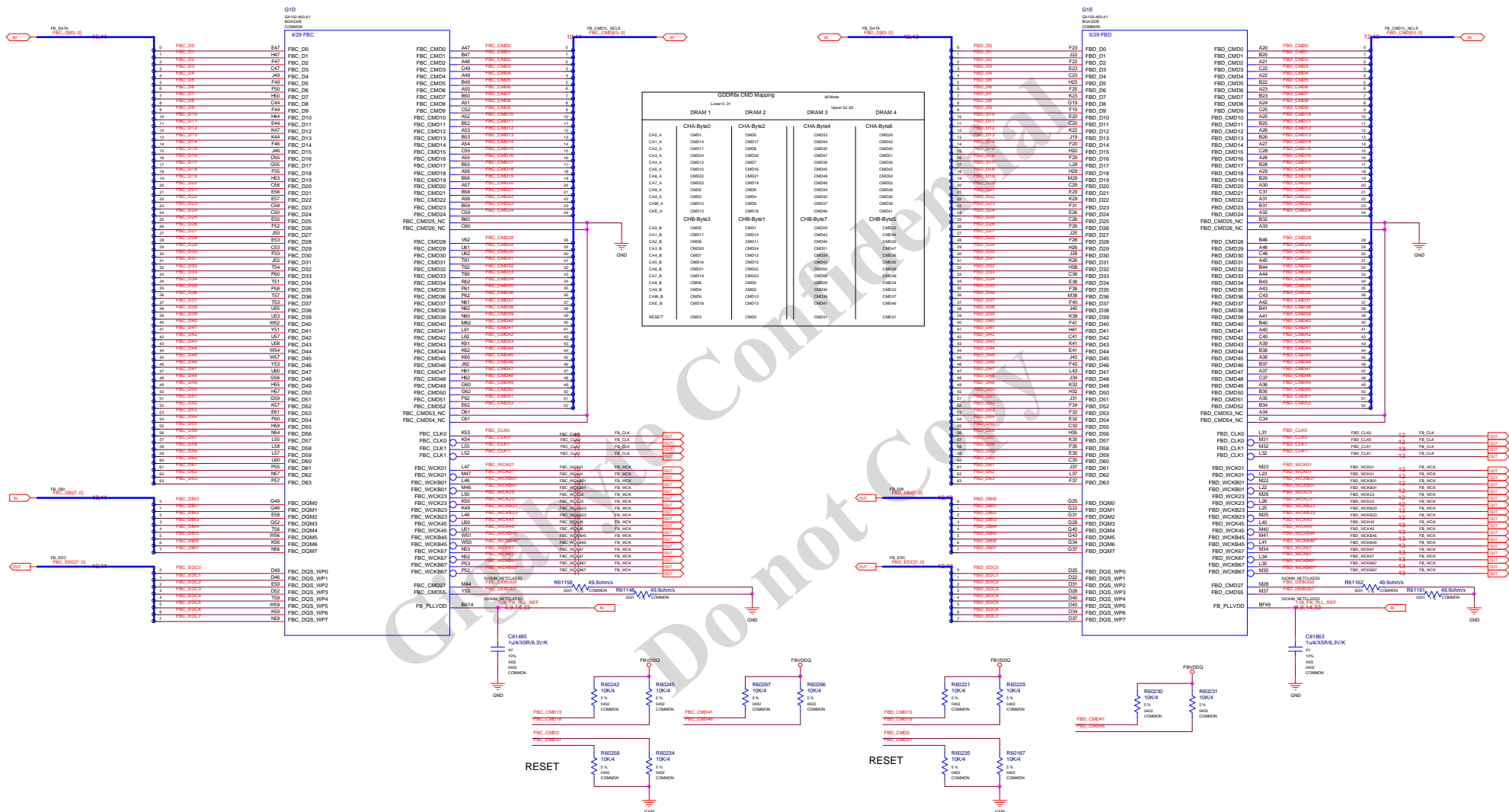
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ASSEMBLY
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 MEMORY FBB PARTITION 63..32

GIGABYTE				
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Size	Document Number	Rev		1.01
Cust	GV-N3090AORUS M-24GD			
Date:	Tuesday, August 28, 2020	Sheet	8	of 82

MEMORY: GPU Partition C/D



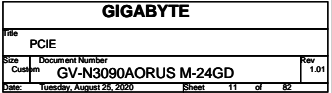
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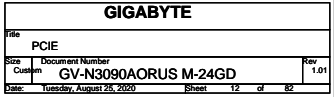
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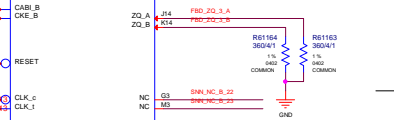
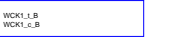
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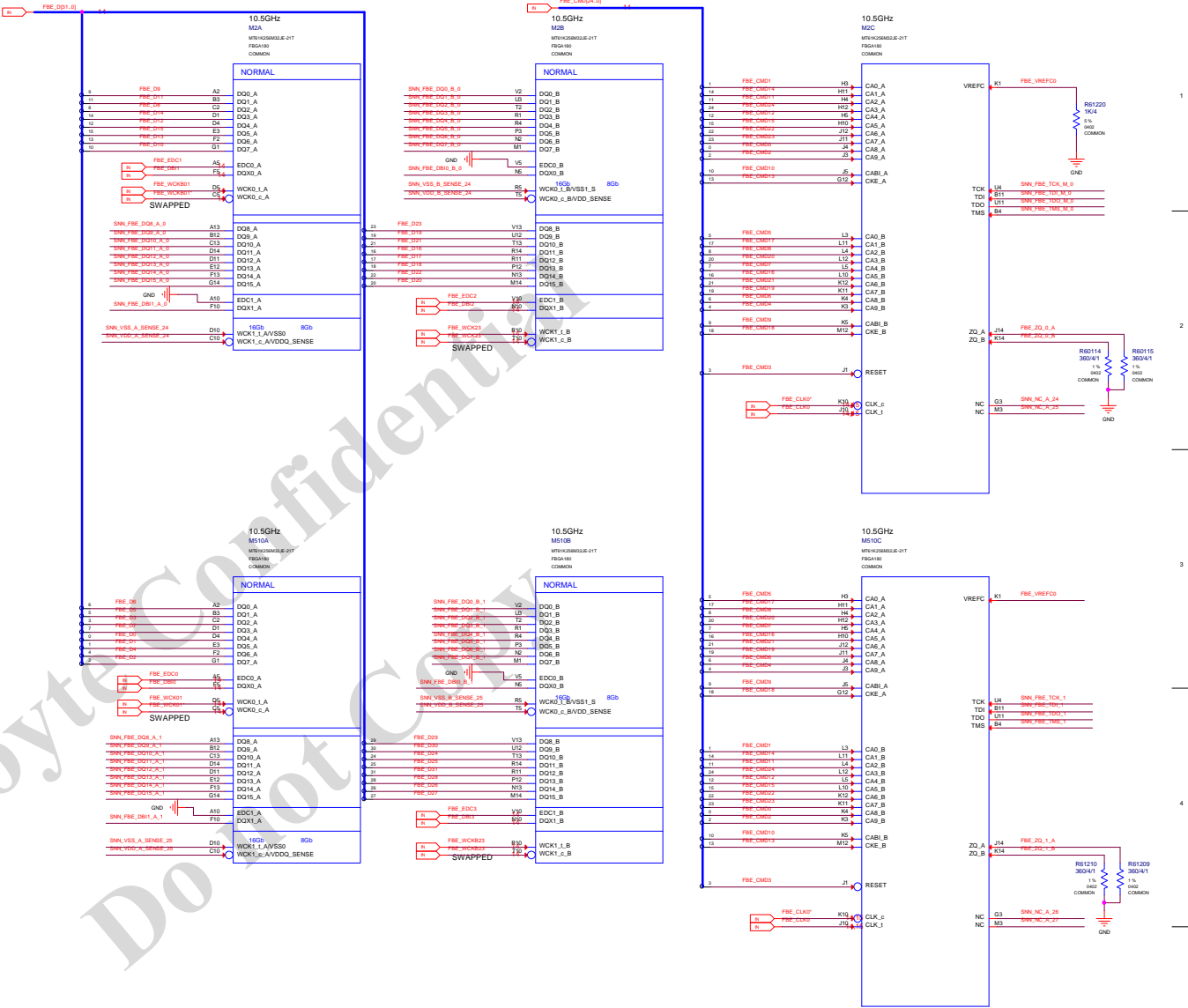
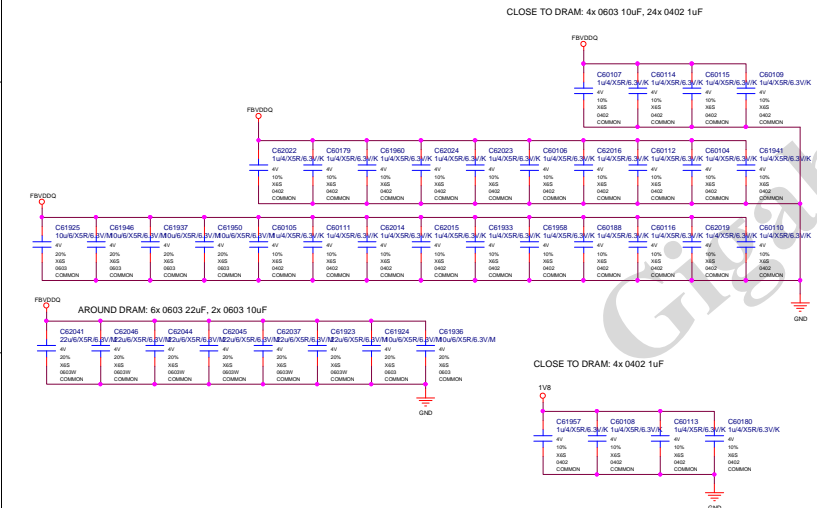
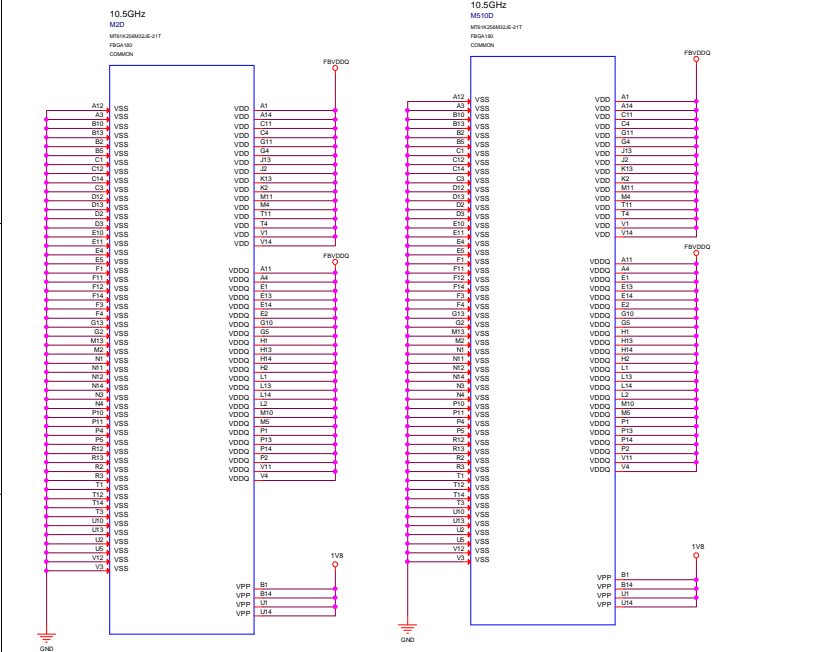
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Size	Customer	Document Number	Rev
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Date:	Tuesday, August 25, 2020		Sheet 9 of 82







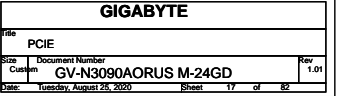


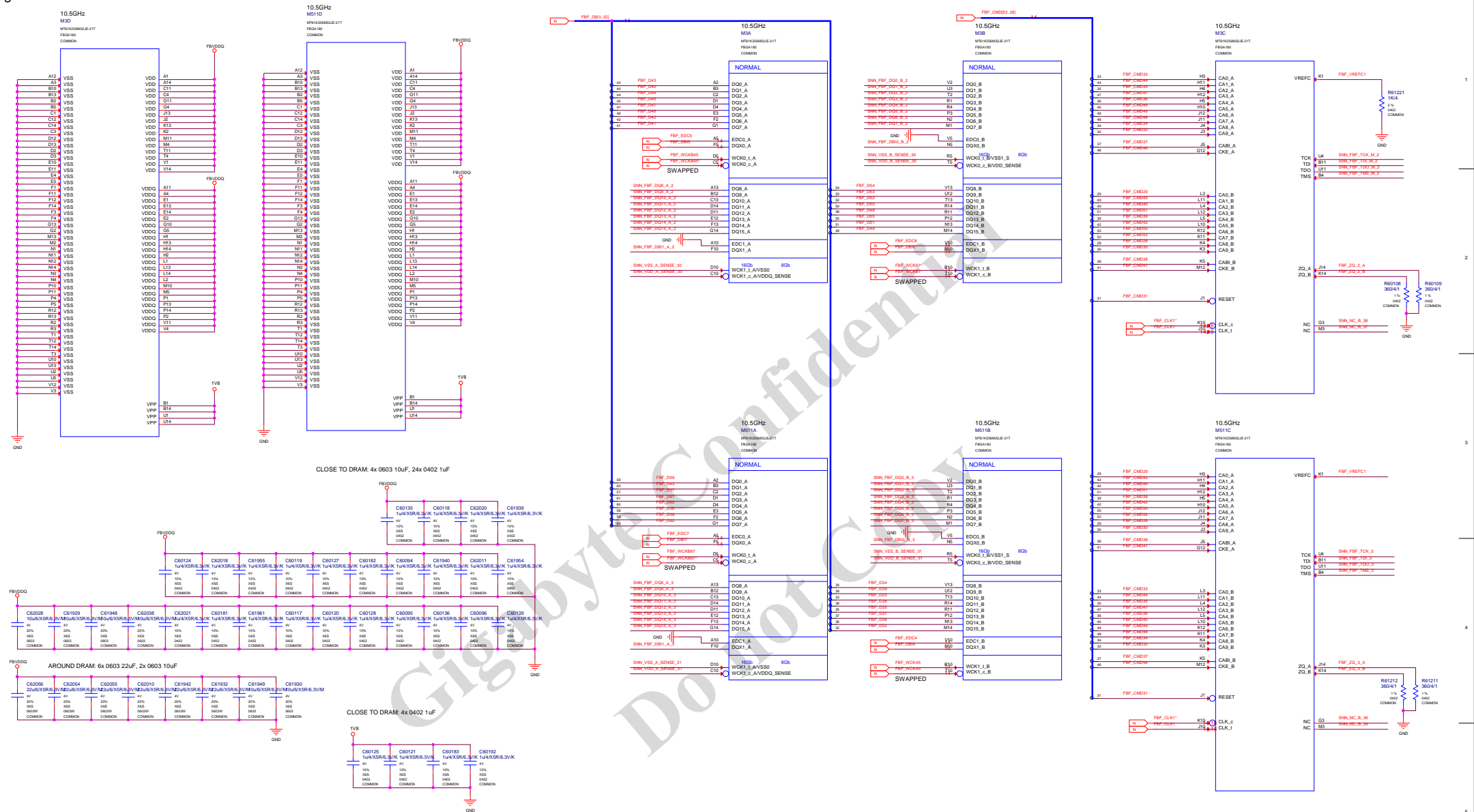


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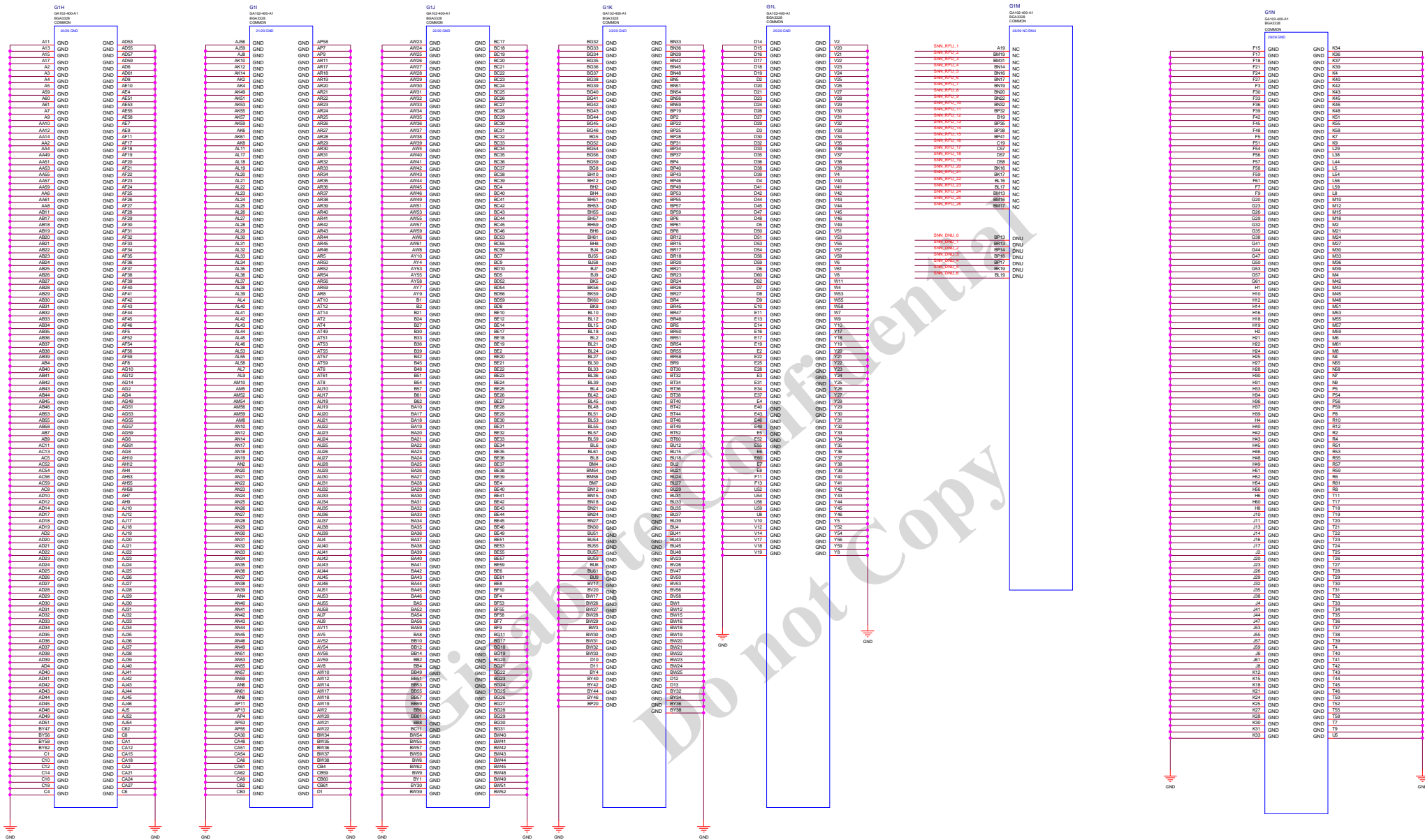
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MEMORY: FBE PARTITION31..0

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Size	Document Number	Rev	
Custom	GV-N3090AORUS M-24GD	1.01	
Date:	Tuesday, August 25, 2020	Sheet	15 of 22

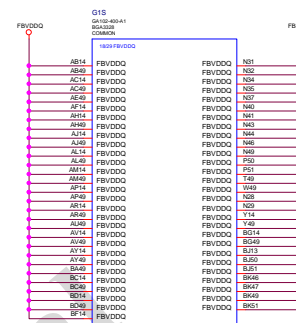
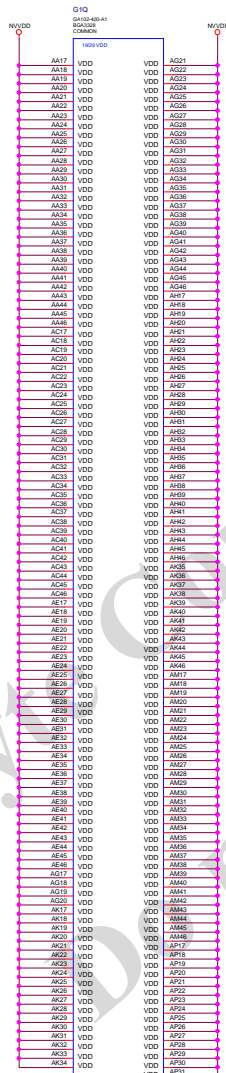
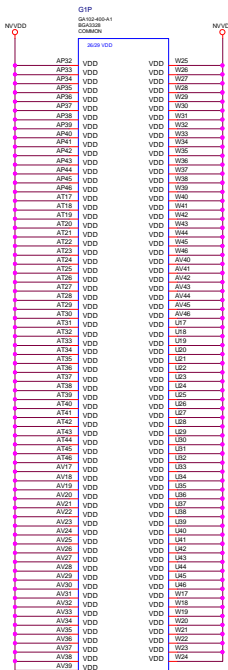
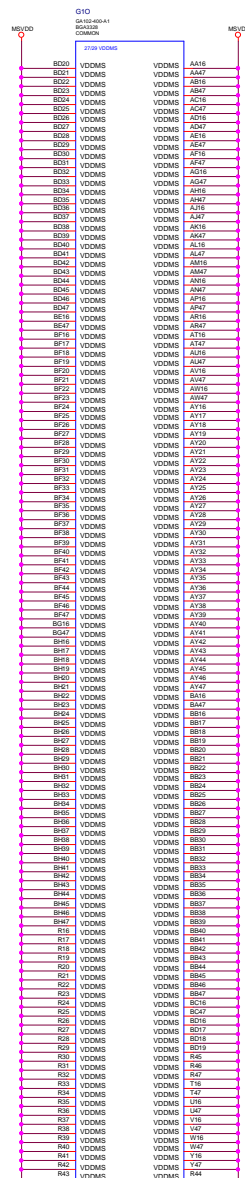




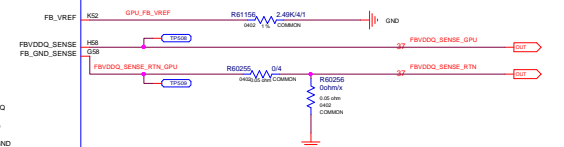
GPU GND, RFUs & RSVD



GPU PWR and GND



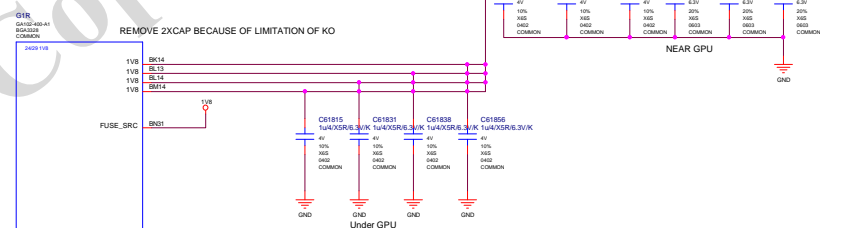
FB_VREF CAP IS REMOVED. NO NEED OF AMPERE



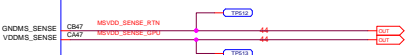
NEAR GPU/ REMOVE GND OPTION

uP9529P has 1GHz glitch on its GND remote sense (Bug 200449976)

TO LE:TPs close to GPU for qualification purpose



Under GPU



ASSEMBLY
PAGE DETAIL

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GPU POWERS

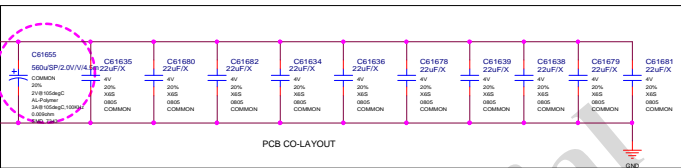
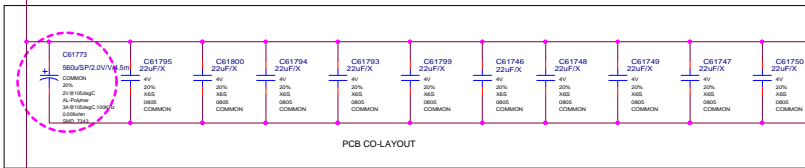
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Title			
PCIE			
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Custom	GV-N3090AORUS M-24GD		1.01
Date:	Tuesday, August 25, 2020	Sheet	20 of 82

NVVDD UNDER GPU

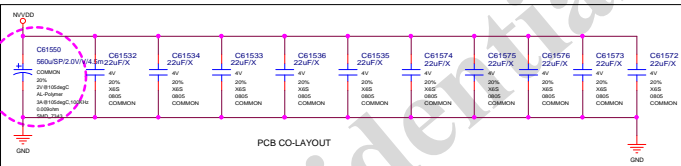
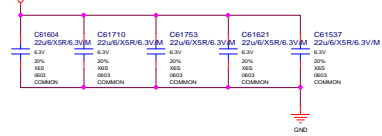
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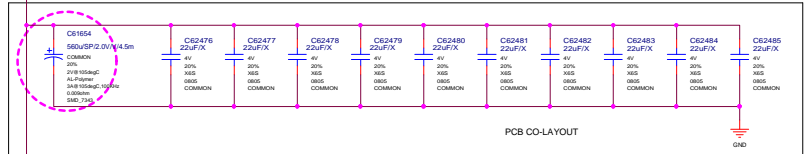
1x 0805 22uF



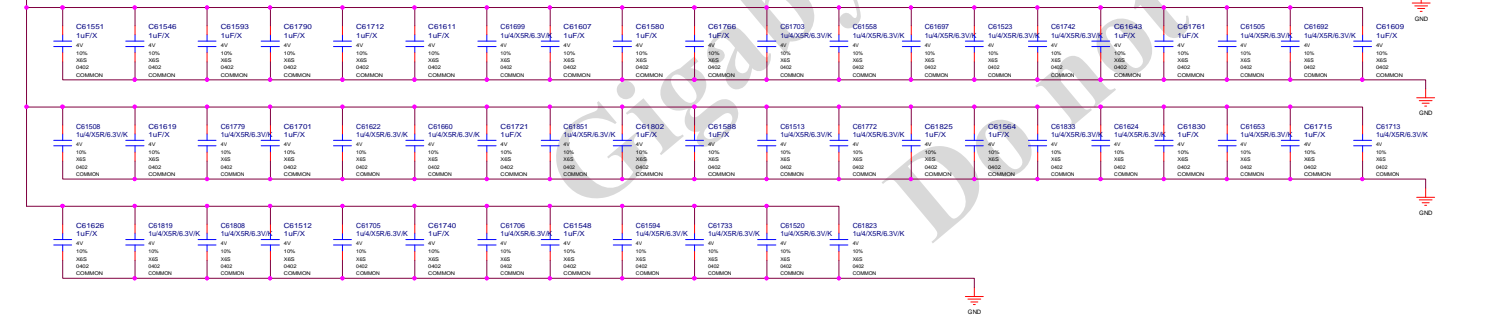
5x 0603 4.7uF



14x 0603 10uF



52 x 0402 1uF

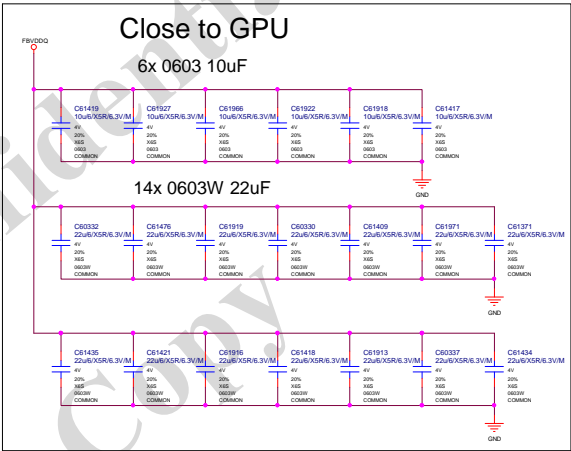


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ASSEMBLY
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-ASSEMBLY DESCRIPTION-
GPU NVVDD DECOUPLING

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File	PCIE			
Size	Customer	Document Number	Rev	
		GV-N3090AORUS M-24GD	1.01	
Date:	Tuesday, August 26, 2020	Sheet	21	of 82

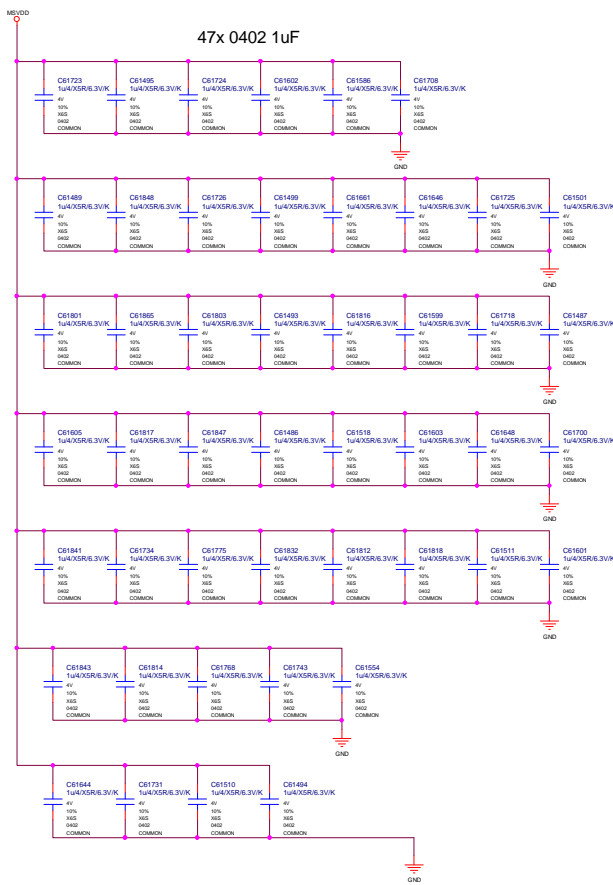
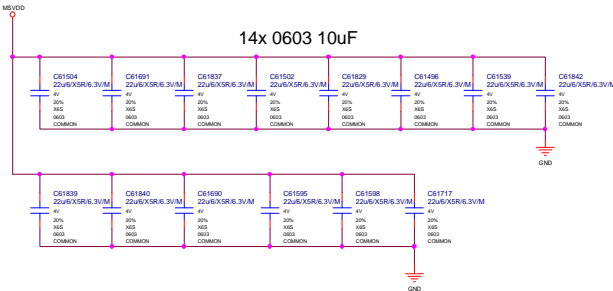
FBVDDQ



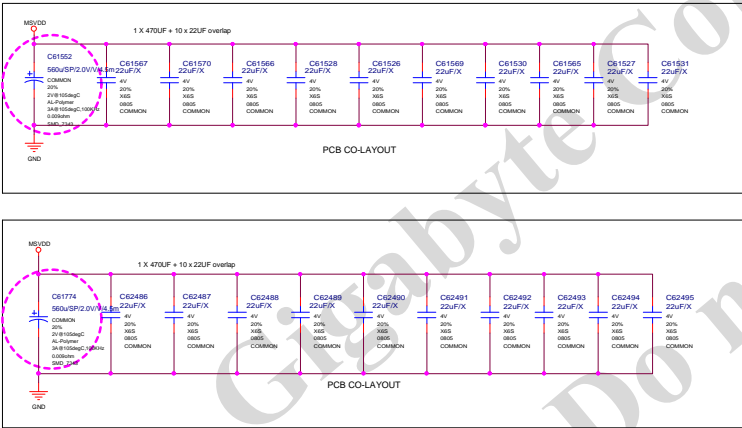
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UNDER GPU

MSVDD



2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION

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Date:	Tuesday, August 26, 2020	Sheet	23	of 82

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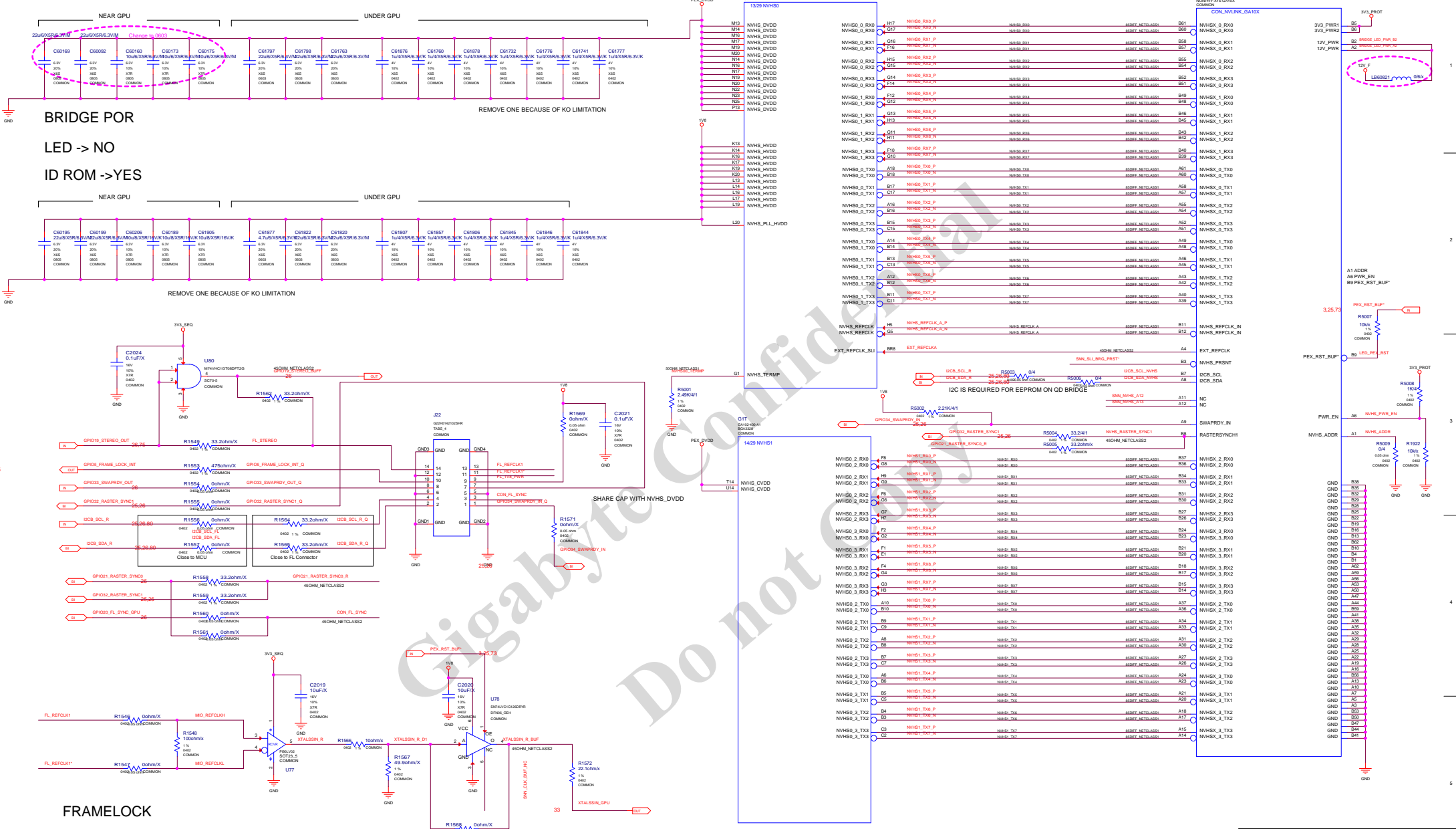
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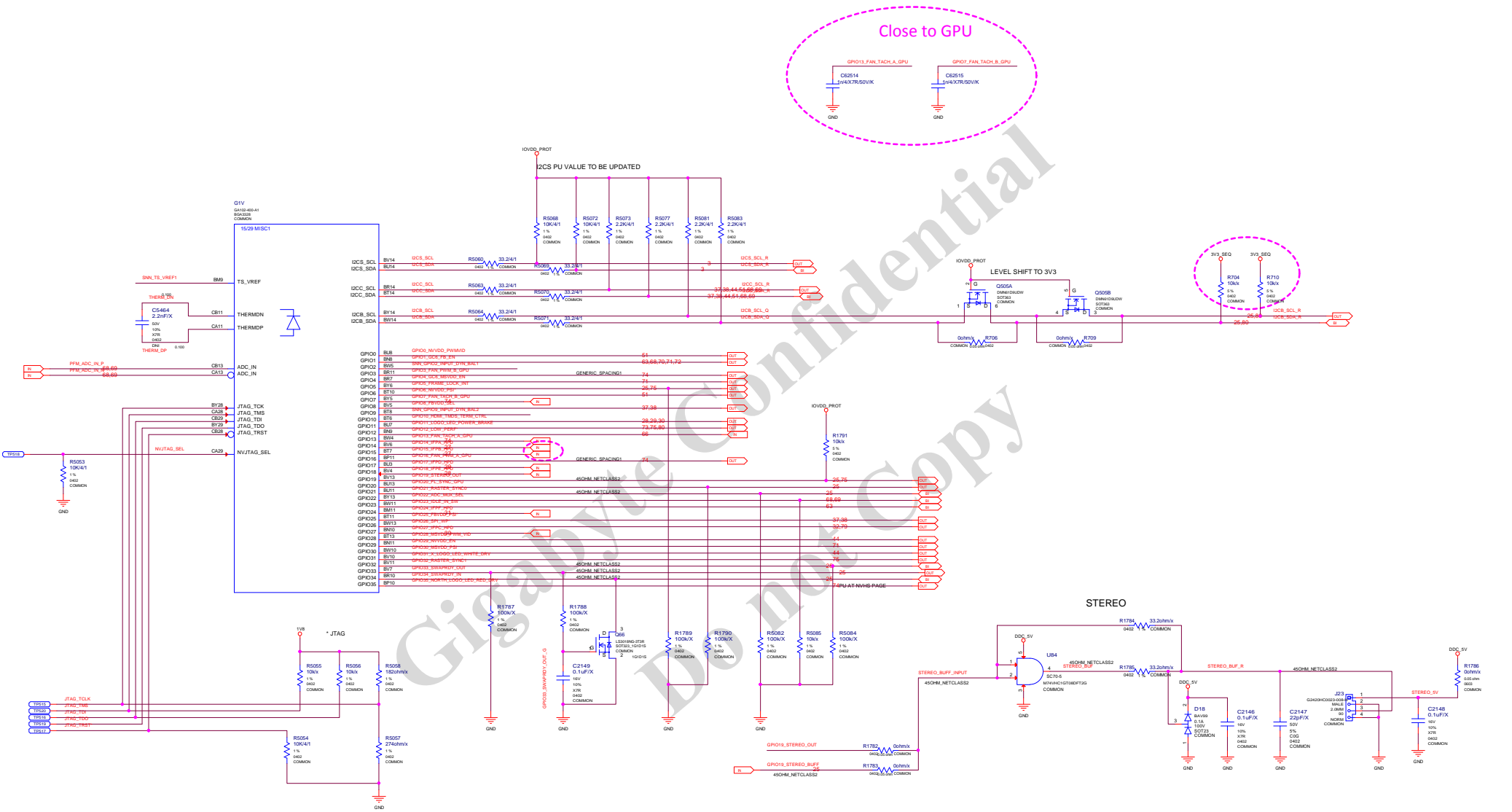
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Title		PCIE	
Size	Document Number	Rev	
Custom	GV-N3090AORUS M-24GD	1.01	
Date:	Tuesday, August 25, 2020	Sheet	24 of 82

NVHS Interface and FRAME LOCK



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MISC1: Fan, Thermal, JTAG, GPIO, STEREO

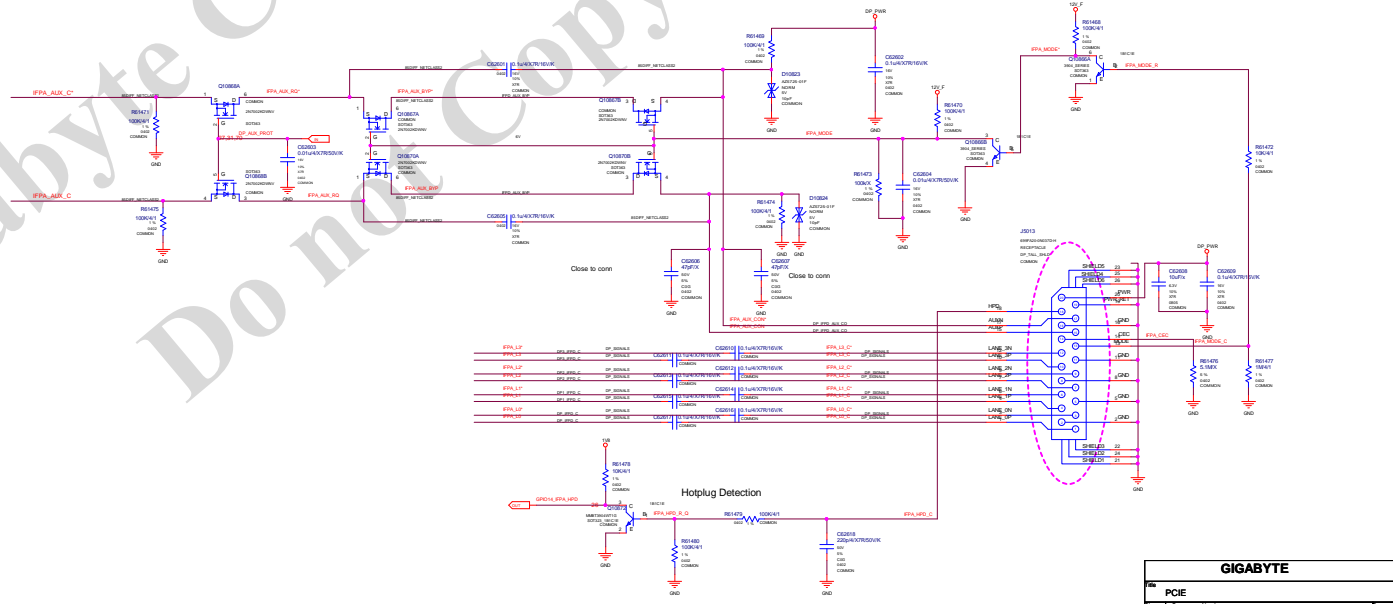
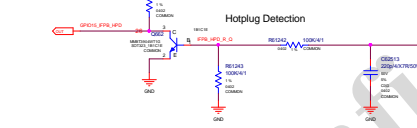
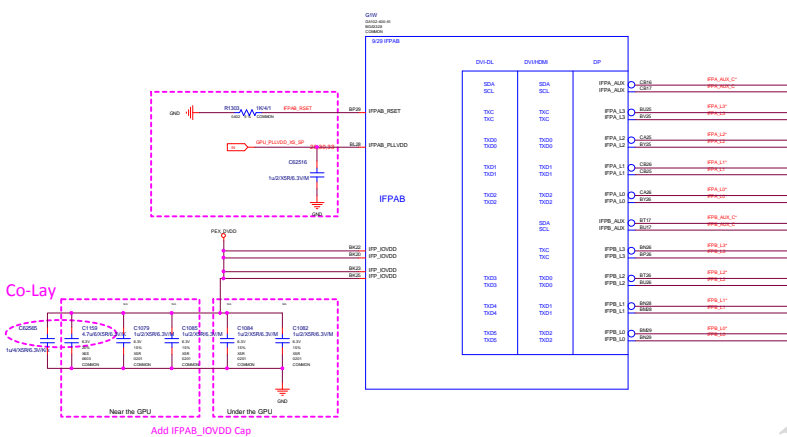
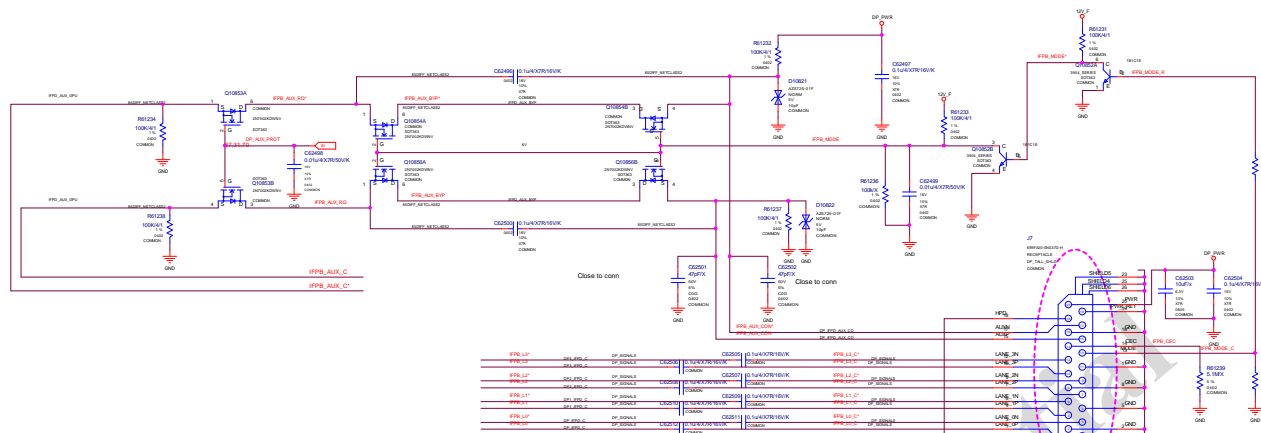


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MISC THERMAL, JTAG, GPIO

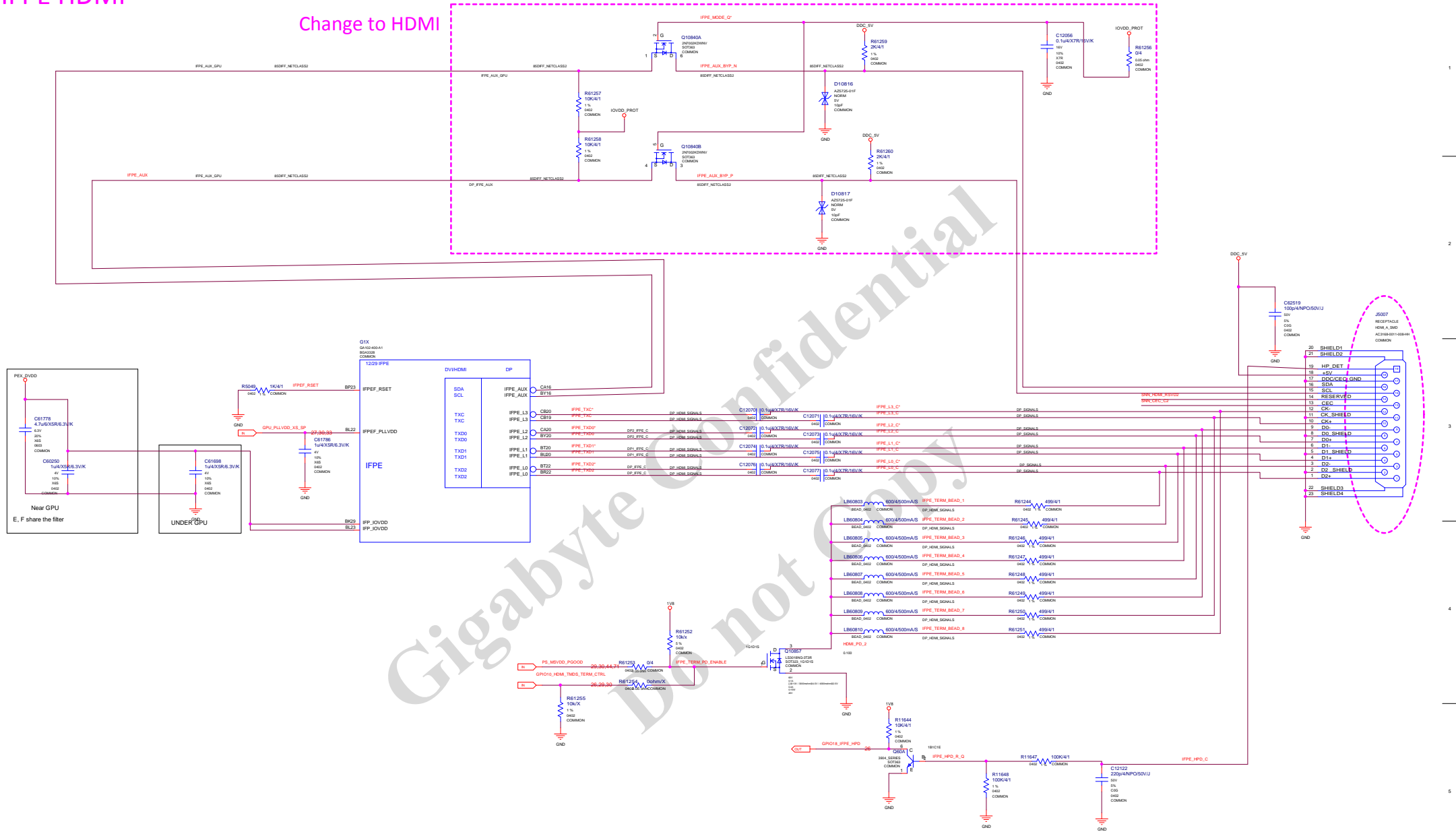
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File	PCIE		
Doc Number	GV-N3090AORUS M-24GD		
Rev	1.01		
Date	Tuesday, August 28, 2023		
Sheet	26	of 92	

IFPA, IFPB For DP x2



IFPE HDMI

Change to HDMI

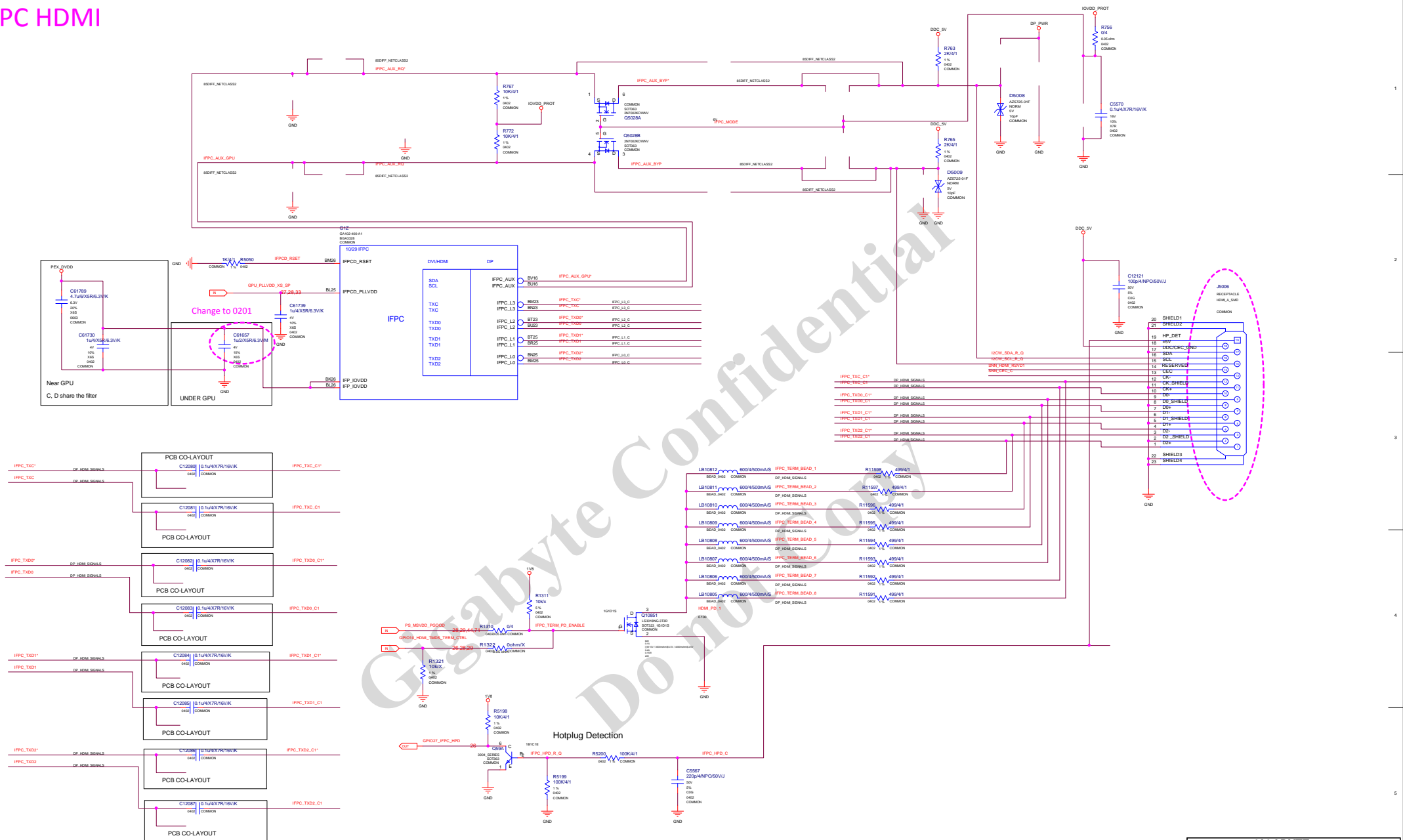


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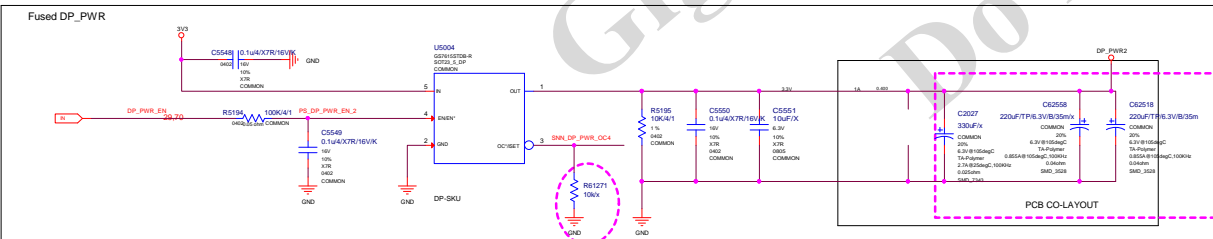
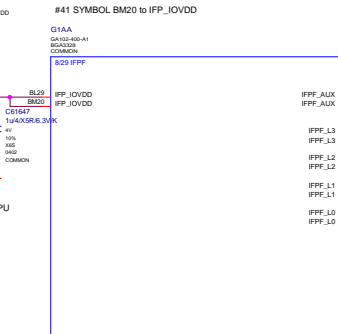
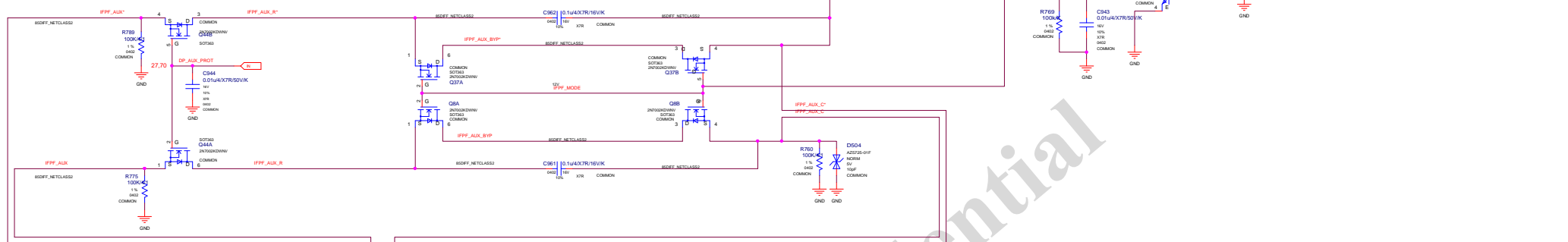
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Doc Number	GV-N3090AORUS M-24GD		
Rev	1.01		
Date	Tuesday, August 28, 2023		
Sheet	28	of 82	

IFPC HDMI



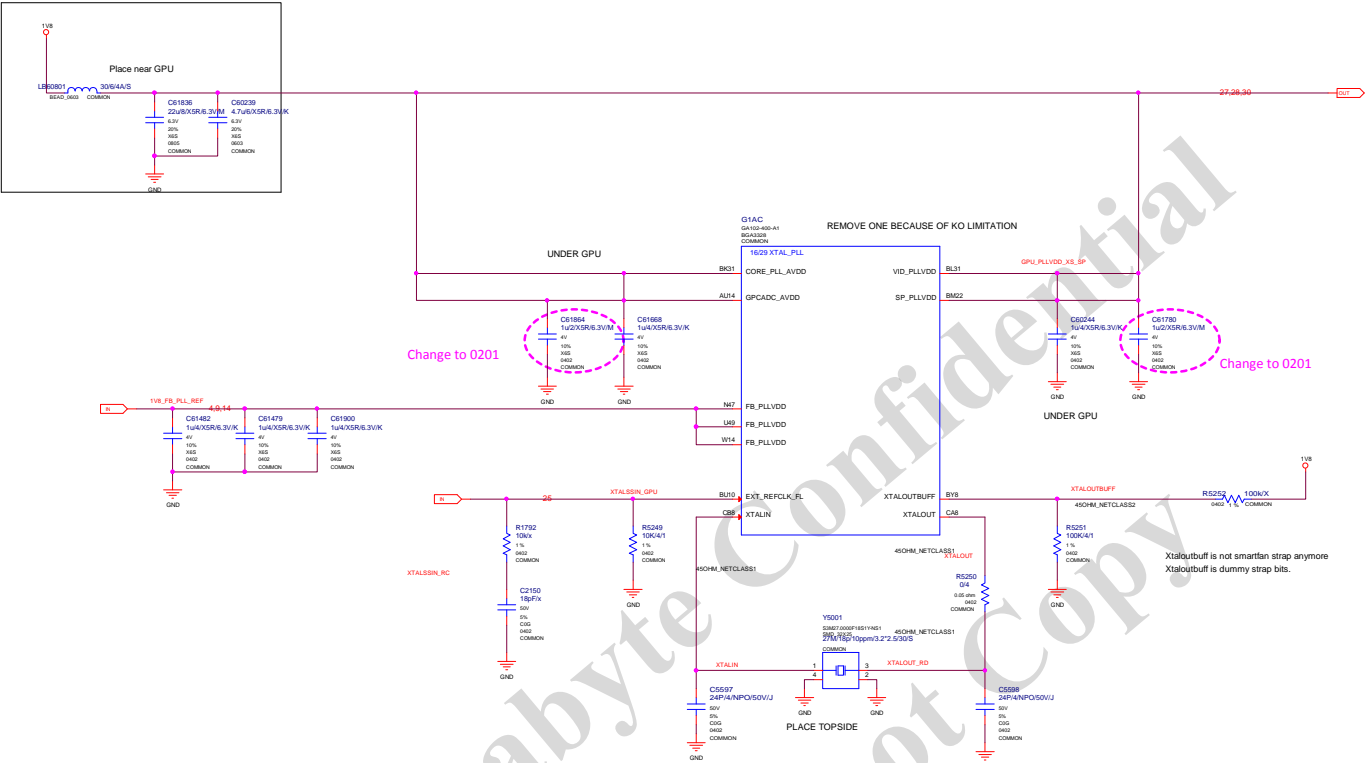
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IFPF DP



ASSEMBLY		ASSEMBLY DESCRIPTION	
PAGE DETAIL		IFPF DP	
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A	B	C	D
E	F	G	H

GIGABYTE			
Part	PCIE		
Doc Number	GV-N3090AORUS M-24GD		
Date	1/10/2024	Rev	1.01
Page	31	of	82



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PAGE DETAIL

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MISC: XTAL. PLL

GIGABYTE			
File	PCIE		
Size	Document Number	Rev	
Comen	GV-N3090AORUS M-24GD	1.01	
Date	Tuesday, August 26, 2025	Sheet	33 of 82

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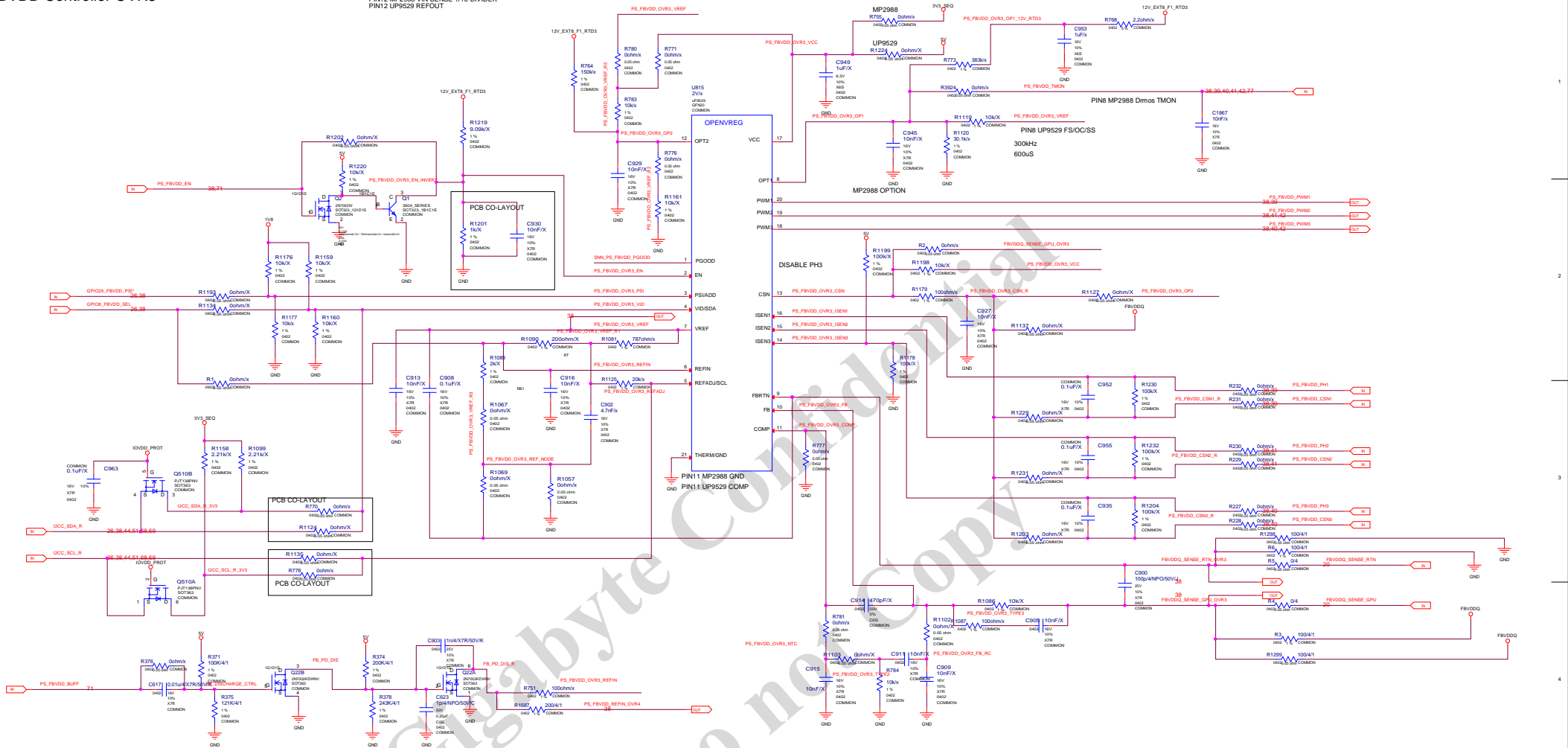
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Title		PCIE	
Size	Document Number	Rev	
Custom	GV-N3090AORUS M-24GD	1.01	
Date:	Tuesday, August 26, 2025	Sheet	36 of 82

PS: FBVDD Controller OVR3

PIN12 MP2988 VIN SENSE 1/16 DIVIDER
PIN12 UP9529 REFOUT



FOR DT SKU

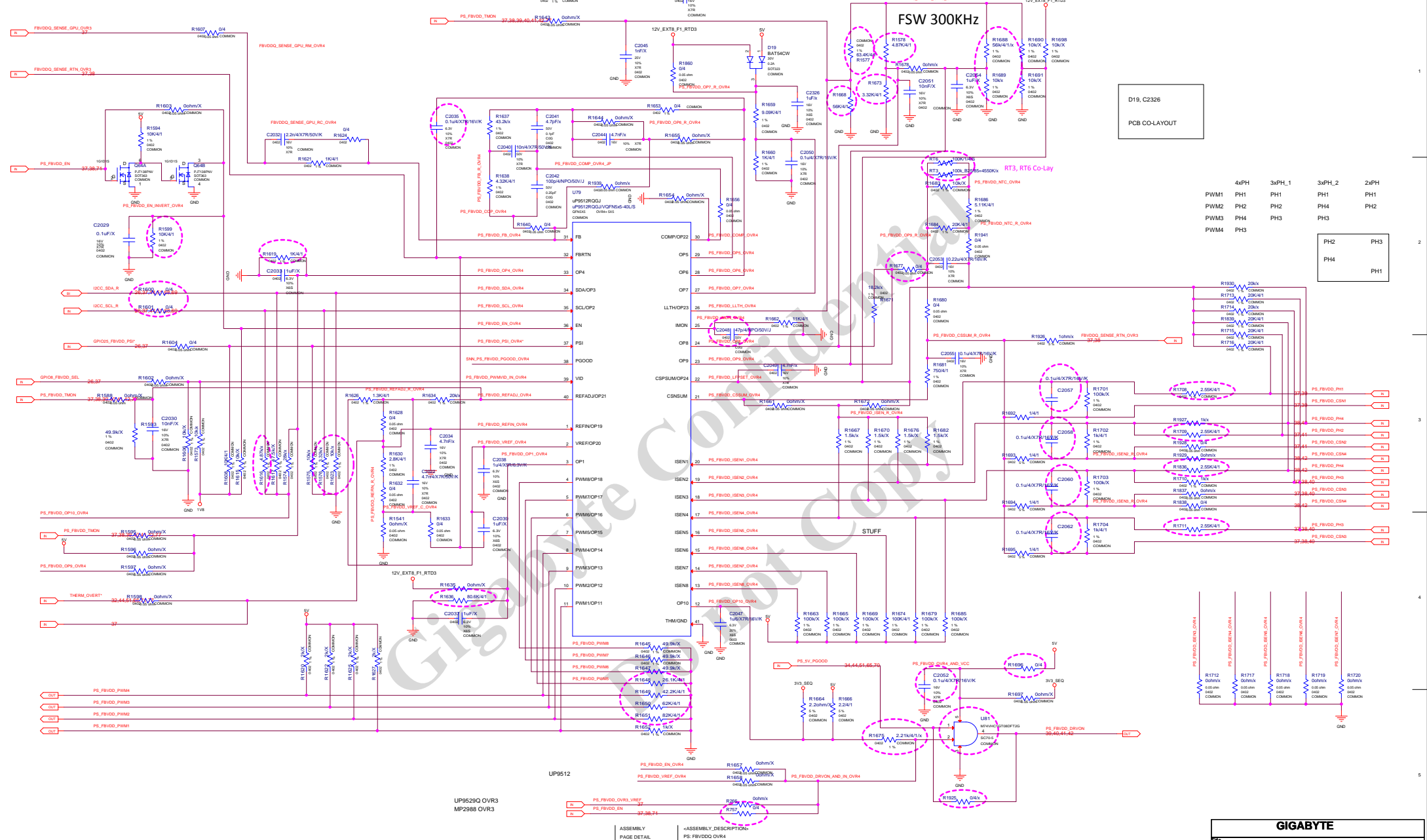
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GIGABYTE			
PCIE			
Size	Document Number	Rev	
Custn	GV-N3090AORUS M-24GD	1.01	
Date:	Tuesday, August 25, 2020	Sheet	37 of 82

PS:FBVDDQ OVR4



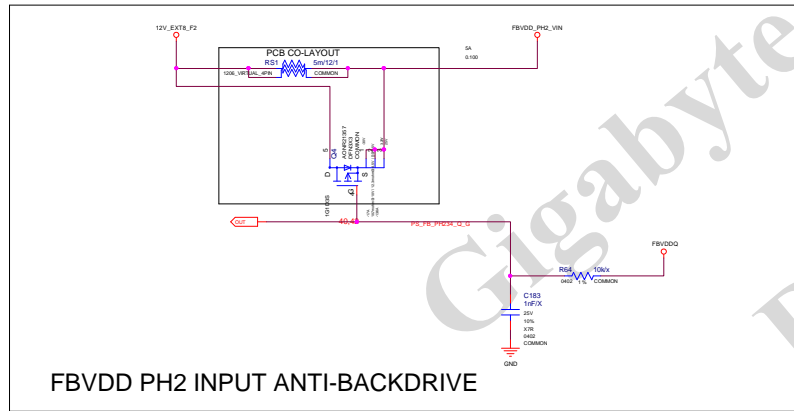
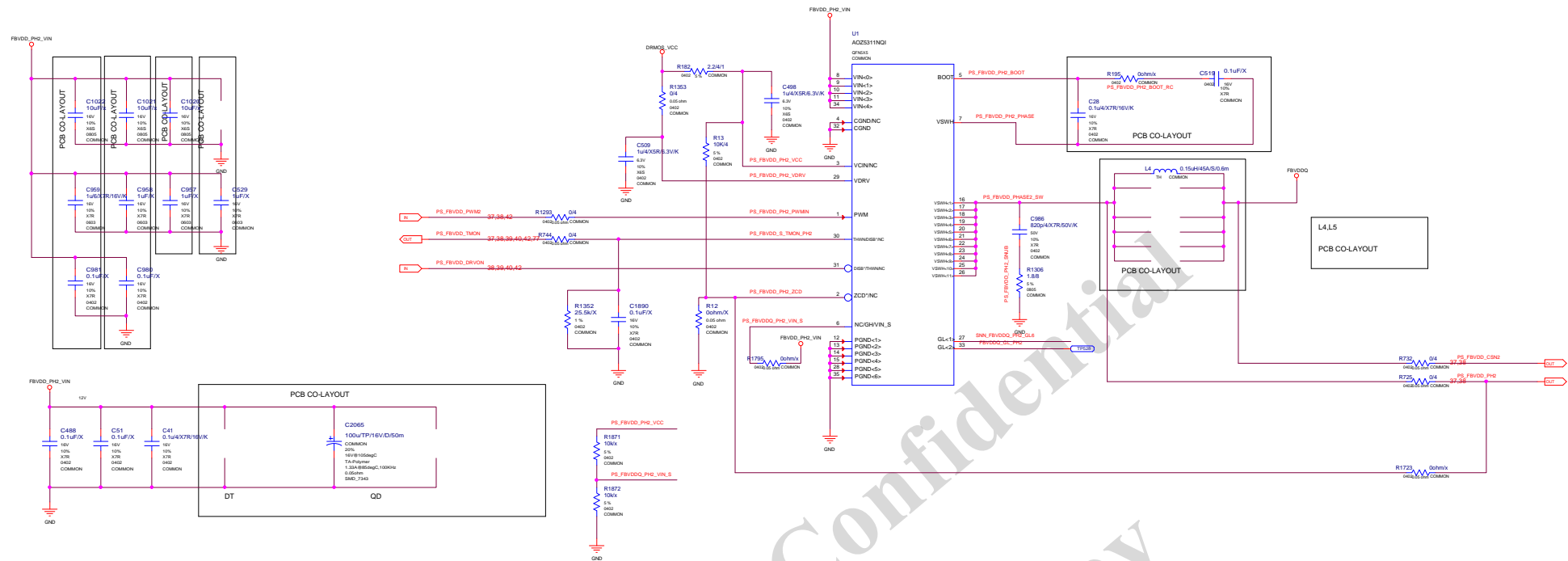
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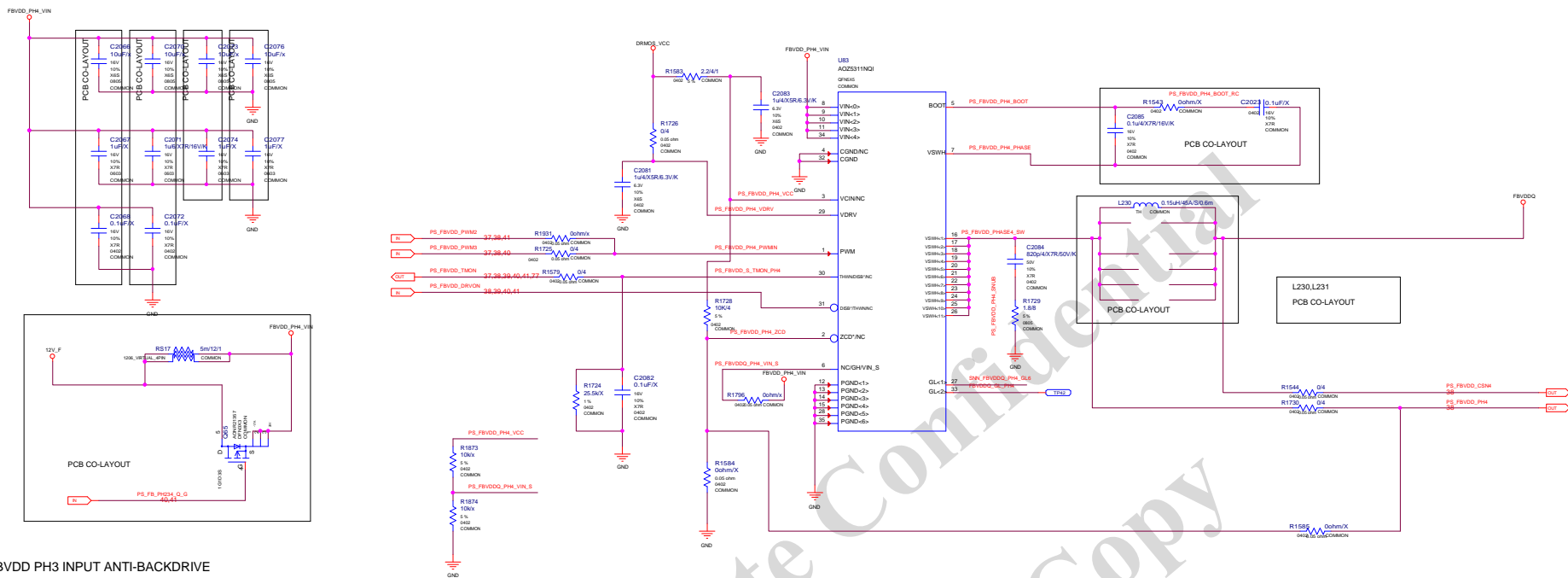
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Size	Custom	Document Number	Rev
		GV-N3090AORUS M-24GD	1.01
Date:	Tuesday, August 25, 2020		Sheet 38 of 82

PS: FBVDD PH2

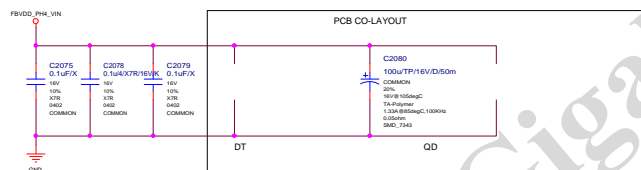


FBVDD PH2 INPUT ANTI-BACKDRIVE

PS: FBVDD PH4



FBVDD PH3 INPUT ANTI-BACKDRIVE



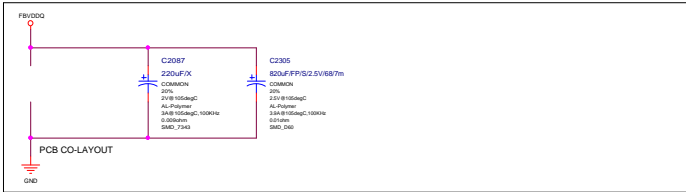
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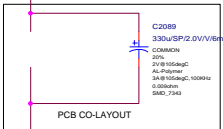
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Title PCIE			
Size	Document Number	Rev 1.	
Custom	GV-N3090AORUS M-24GD		
Date:	Tuesday, August 25, 2020	Sheet	42 of 82

REFER TO PCB FOR BOM STUFFING

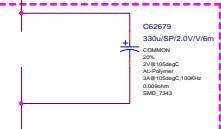
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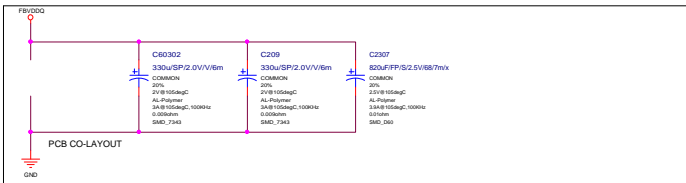
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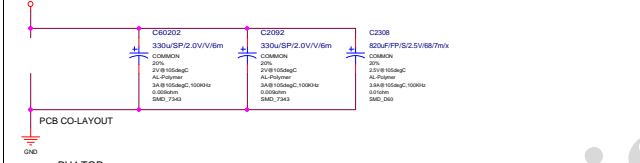
PH3 Bottom



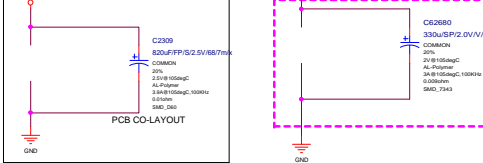
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PH4 TOP



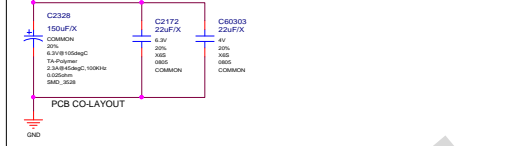
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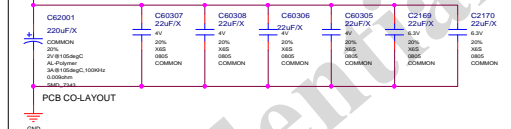
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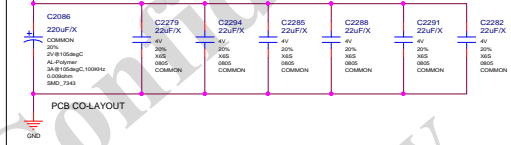
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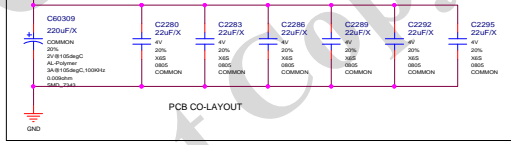
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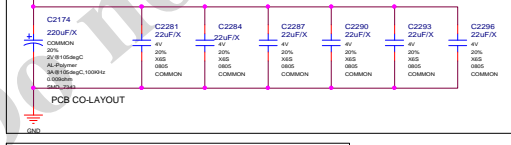
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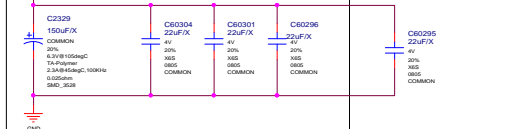
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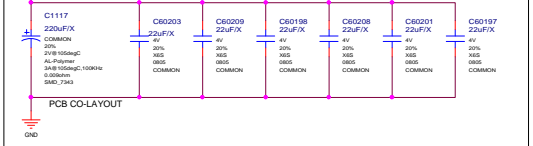
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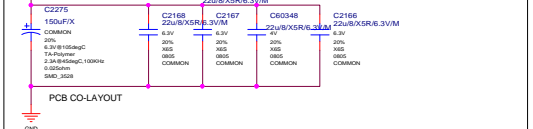
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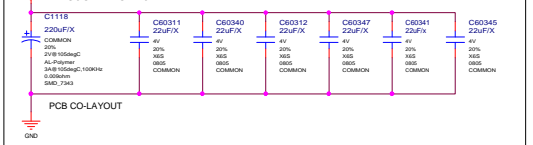
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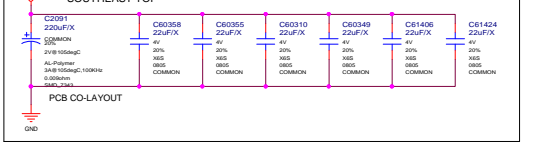
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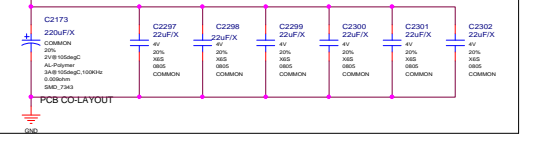
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SOUTHEAST TOP



NORTHEAST TOP



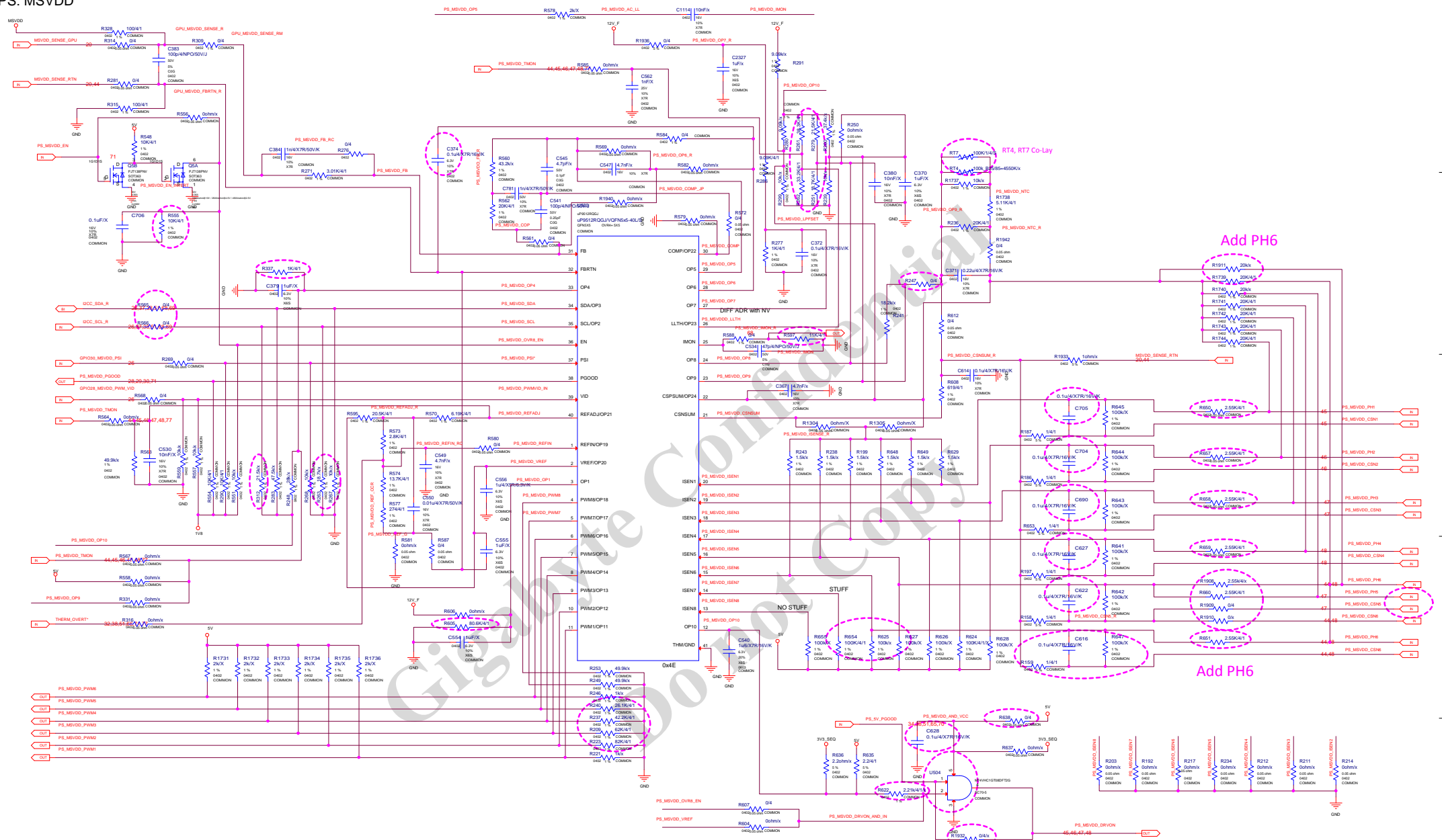
PCB CO-LAYOUT



GIGABYTE

File	PCIE	Rev	1.01
Doc	Document Number		
Rev	GV-N3090AORUS M-24GD		
Doc	Issued, August 28, 2023	Sheet	43 of 82

PS: MSVDD



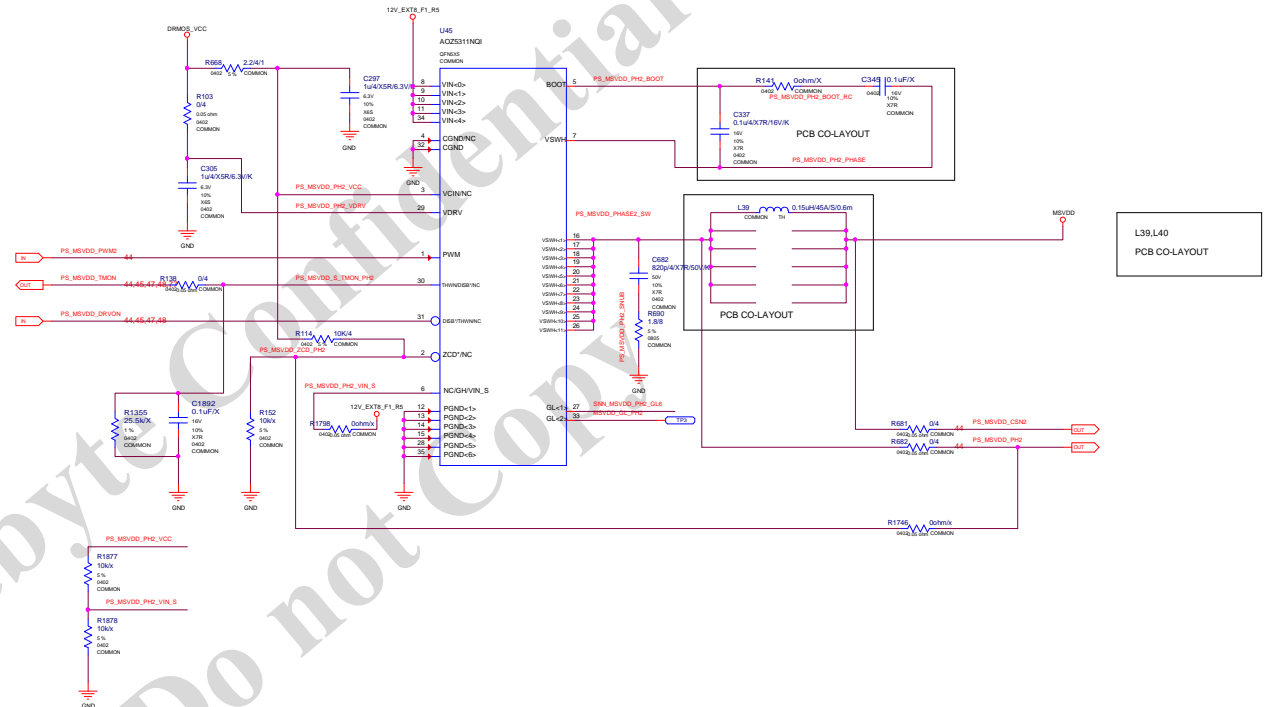
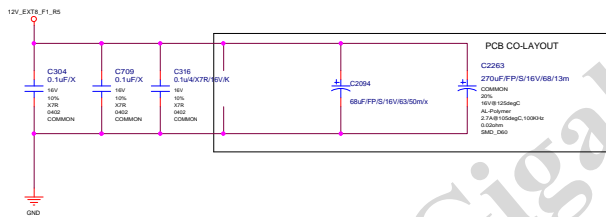
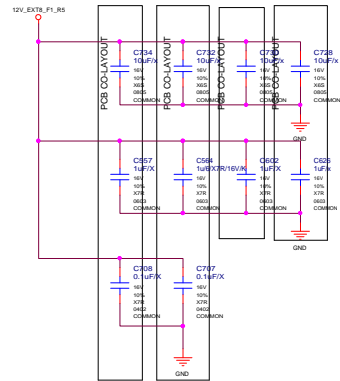
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PS: MSVDD CONTROLLER

GIGABYTE

Title			
PCIE			
Size	Document Number	Rev	
Custom	GV-N3090AORUS M-24GD	1.01	
Date:	Tuesday, August 26, 2020	Sheet	44 of 82

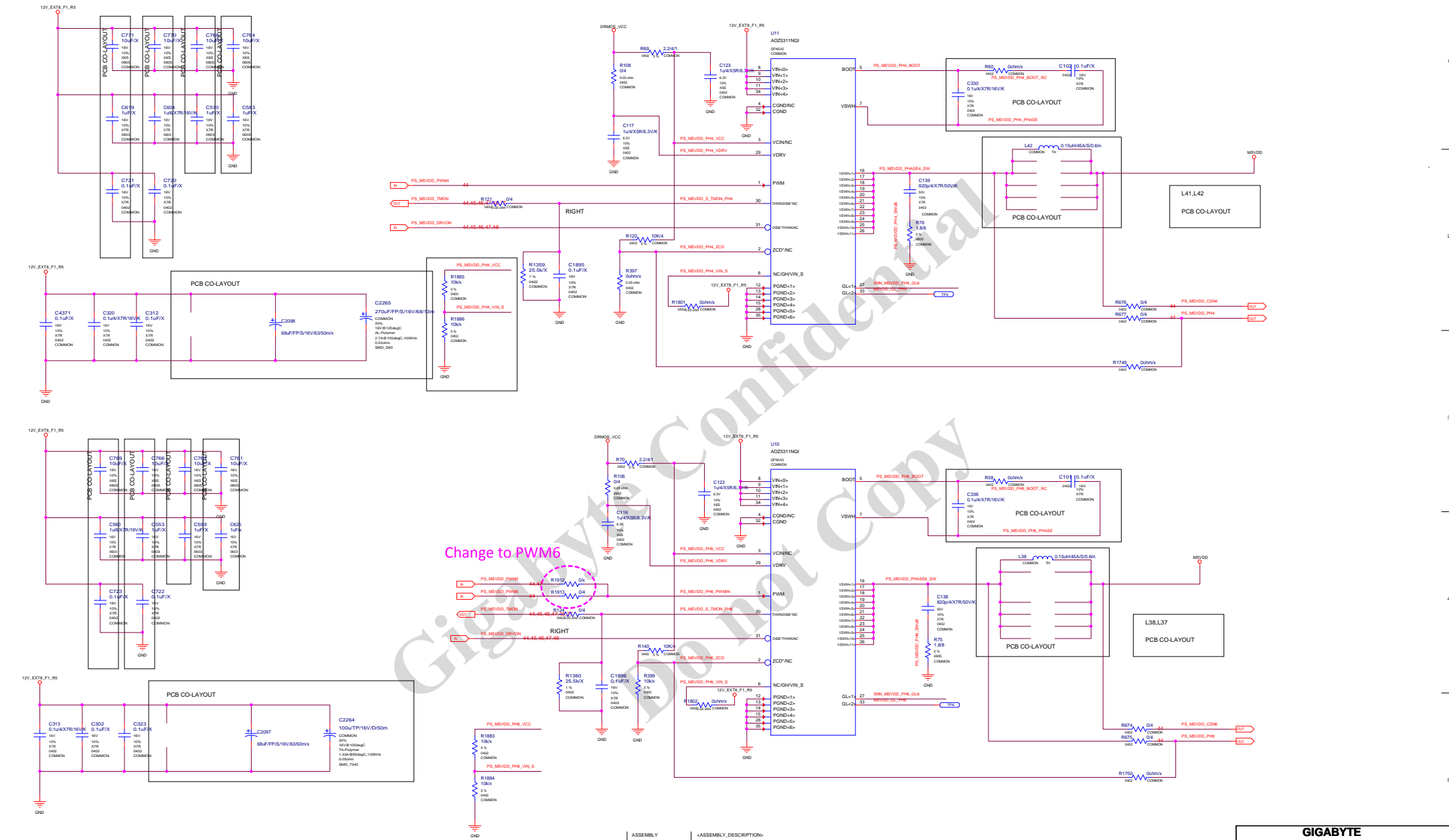


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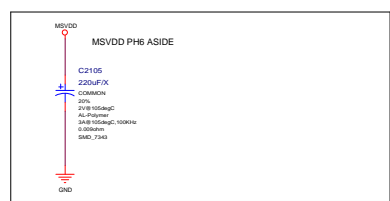
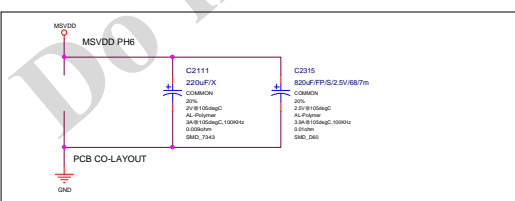
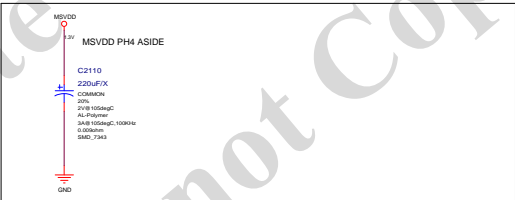
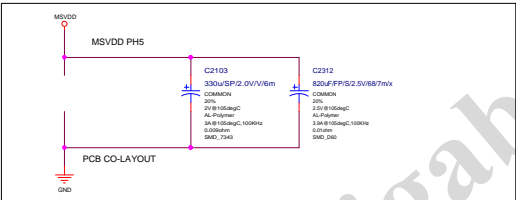
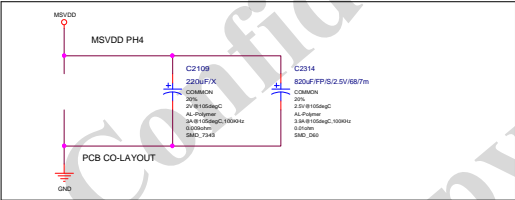
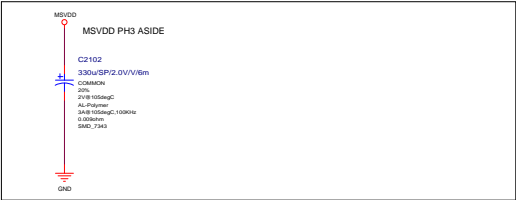
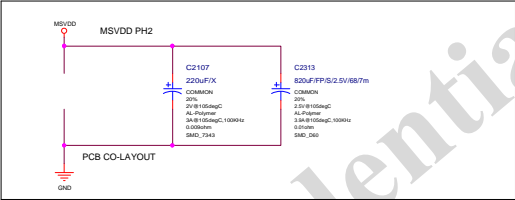
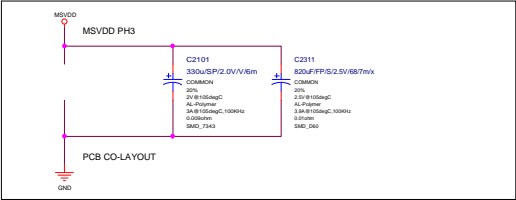
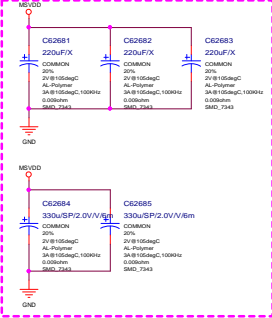
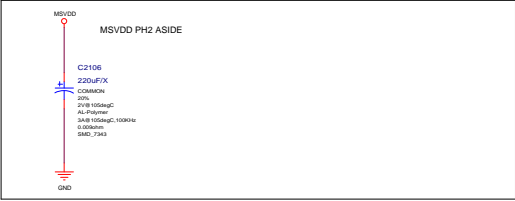
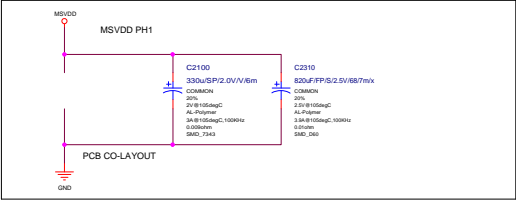
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PS: MSVDD PH 4,6



PS:MSVDD OUTPUT CAP (TOP)

REFER TO PCB FOR BOM STUFFING



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ASSEMBLY
PAGE DETAIL

ASSEMBLY DESCRIPTION
PS: MSVDD OUTPUT CAP(TOP)

GIGABYTE			
File	PCIE		
Doc Number	GV-N3090AORUS M-24GD		
Date	Thursday, August 26, 2020	Sheet	49 of 92

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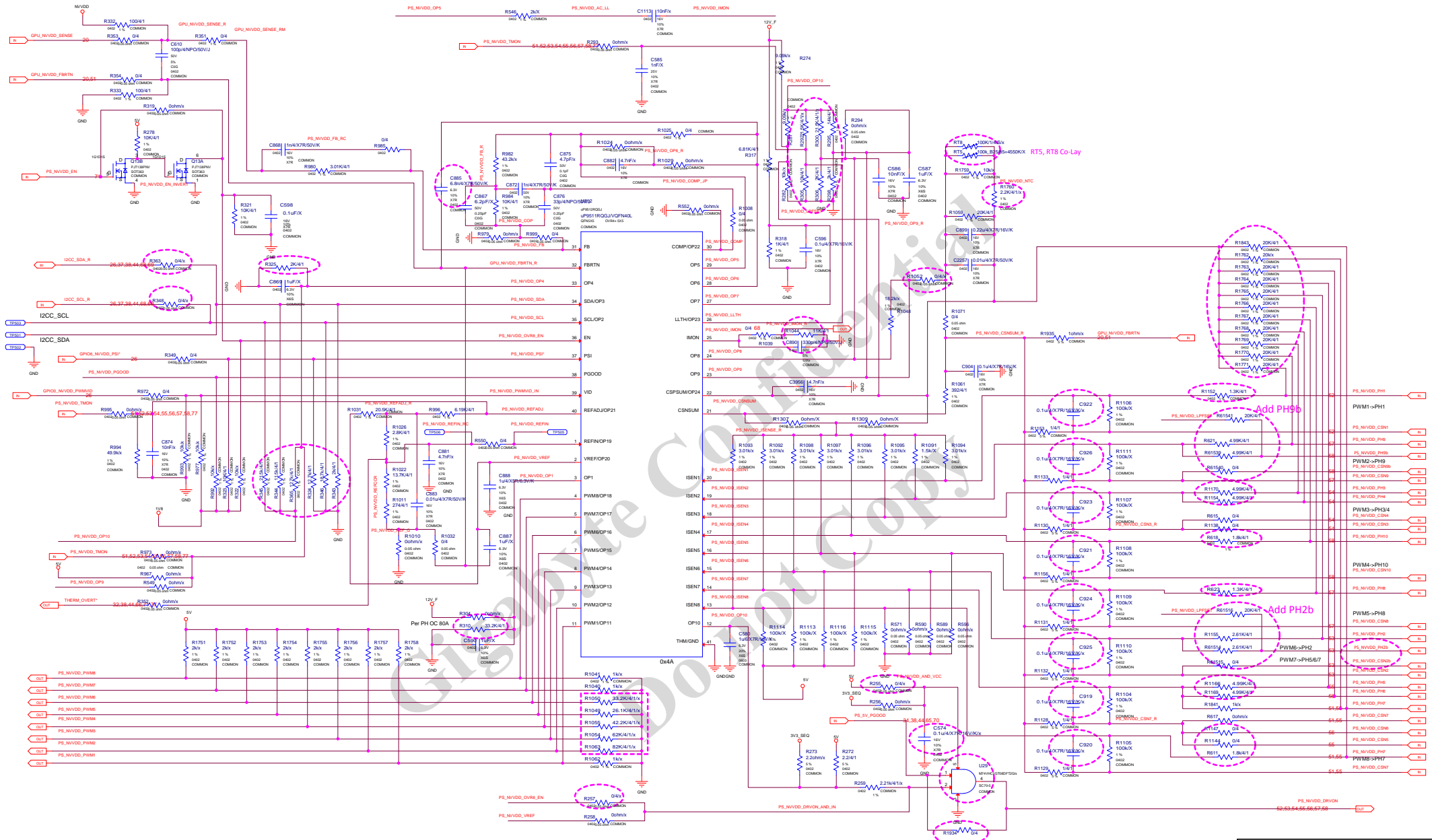
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Title		PCIE	
Size	Document Number	Rev	
Custom	GV-N3090AORUS M-24GD	1.01	
Date: Tuesday, August 26, 2025		Sheet	50 of 82

PS: NVVDD Controller_OVR8



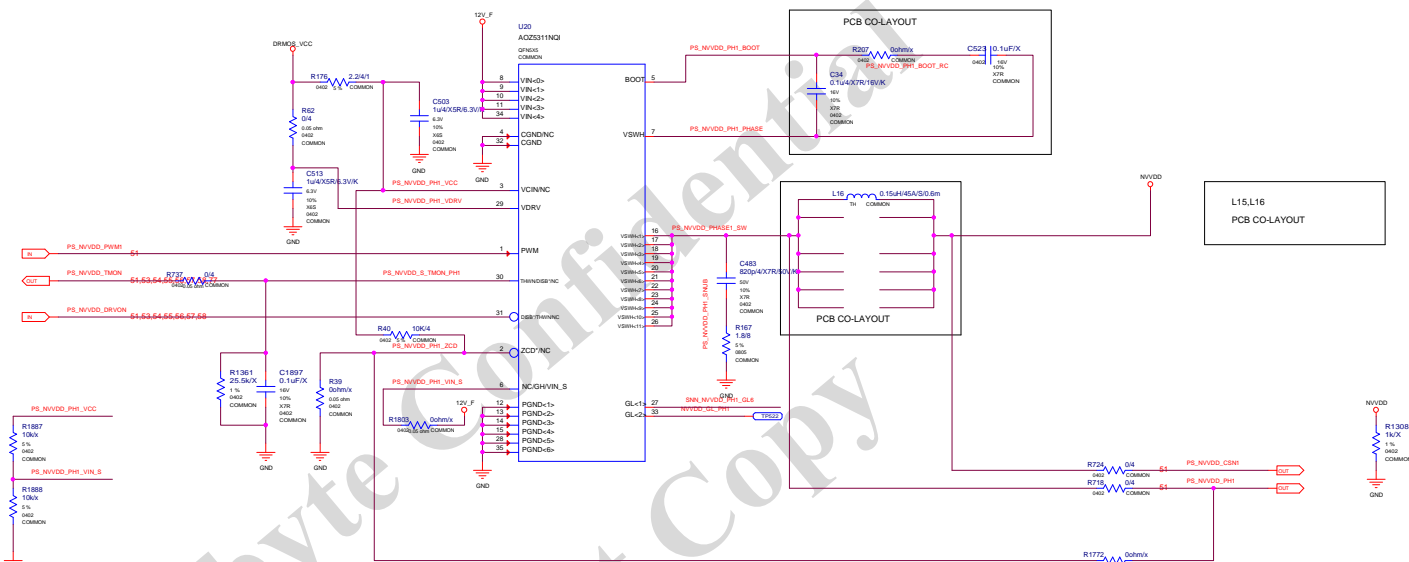
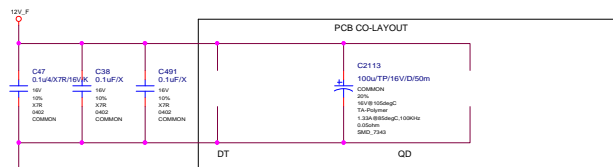
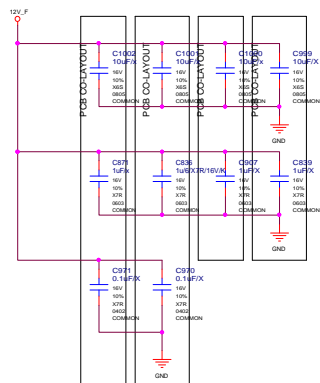
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PS: NVVDD Controller_OVR8
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Title			
PCIE			
Size	Document Number	Rev	
Custm	GV-N3090AORUS M-24GD	1.01	
Date:	Tuesday, August 25, 2020	Sheet	51 of 82

PS: NVVDD Phase 1



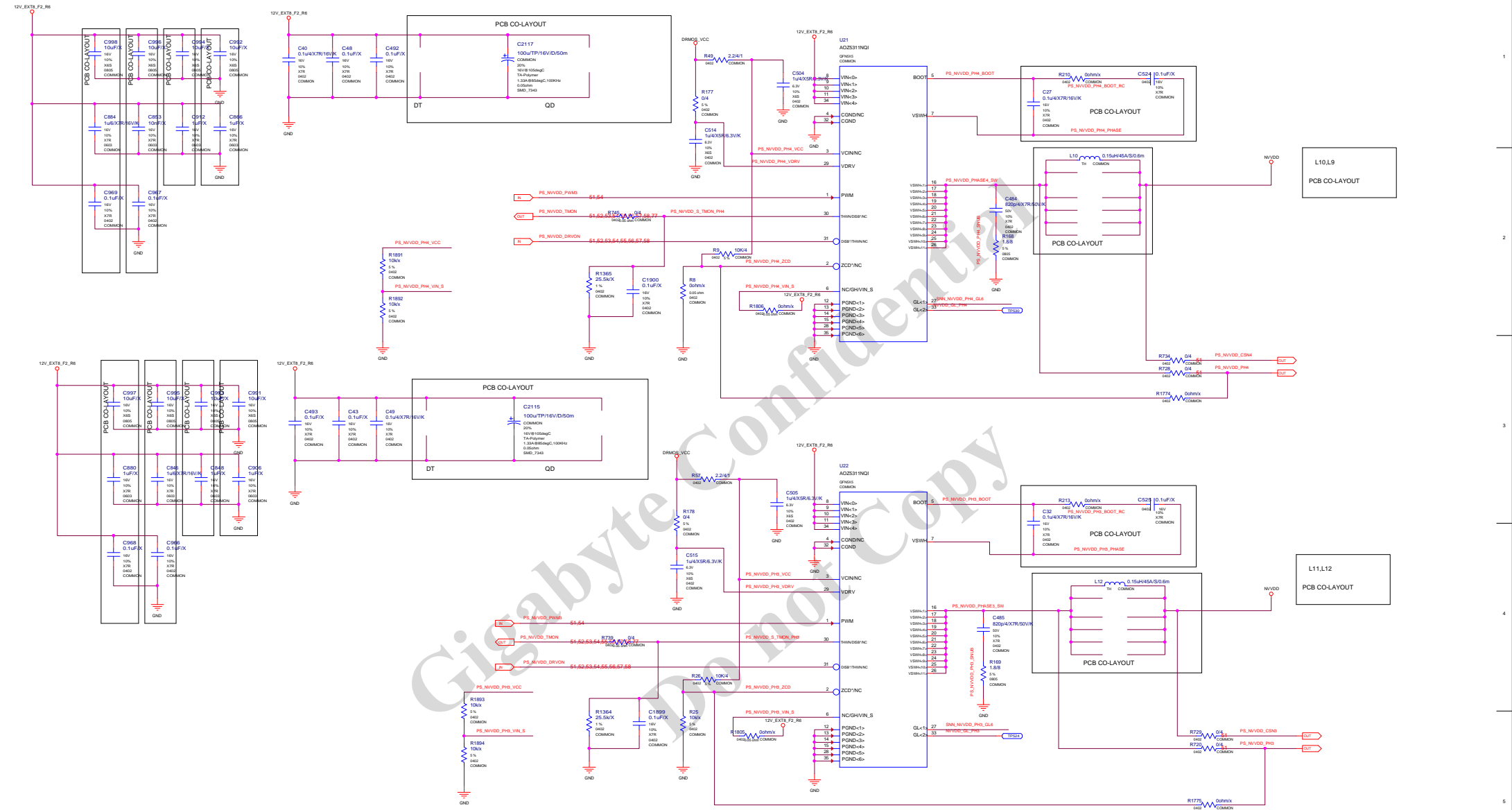
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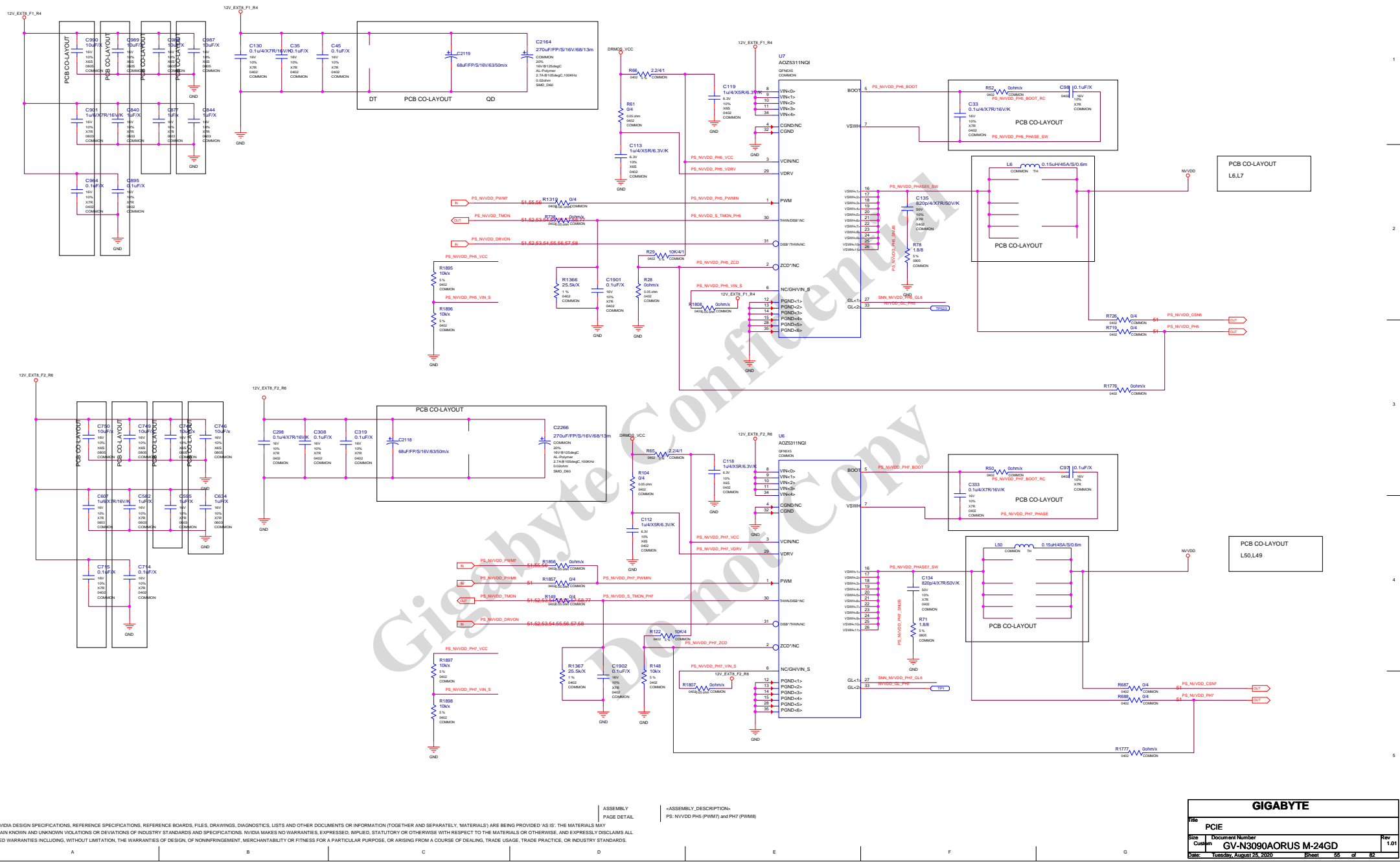
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Size	Document Number		Rev
Custom	GV-N3090AORUS M-24GD		1.01
Date:	Tuesday, August 25, 2020	Sheet	52 of 82

PS: NVVDD Phase 3 (PWM3), PHASE4 (PWM3)



PS: NVVDD PH 5(PWM4), PH7(PWM8/4)

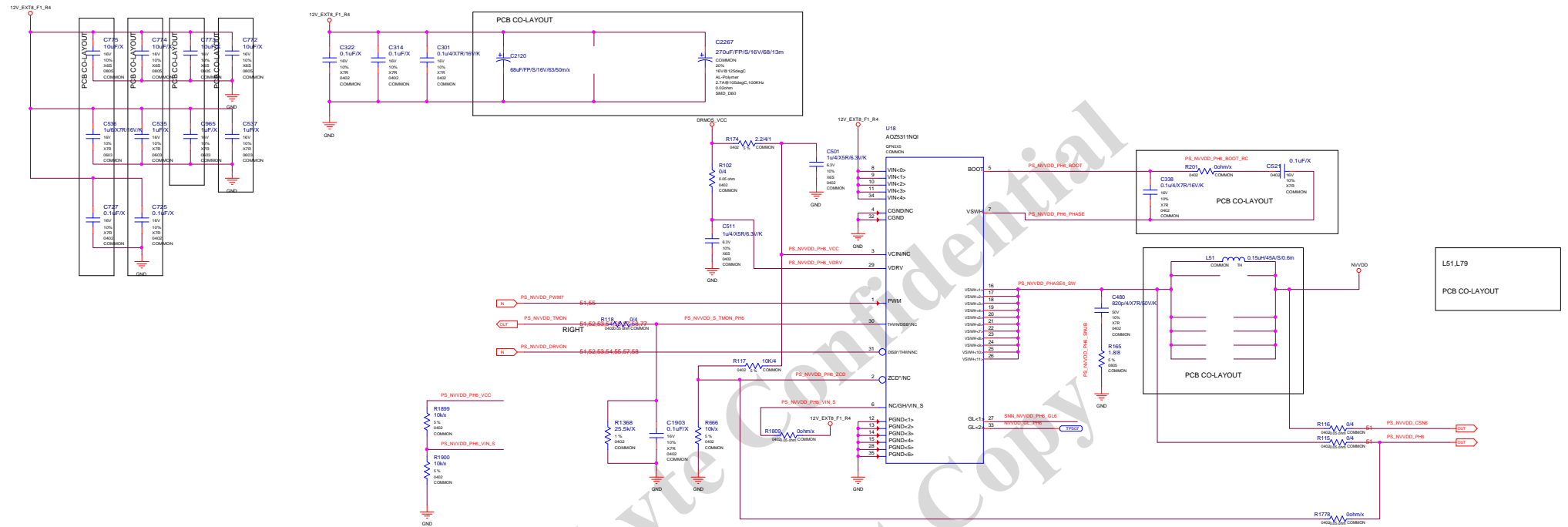


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ASSEMBLY
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PS: NVVDD PH 5(PWM4) AND PH7 (PWM8)

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Doc	Document Number	Rev	
Com	GV-N3090AORUS M-24GD	1.01	
Date	Tuesday, August 28, 2024	Sheet	55 of 82

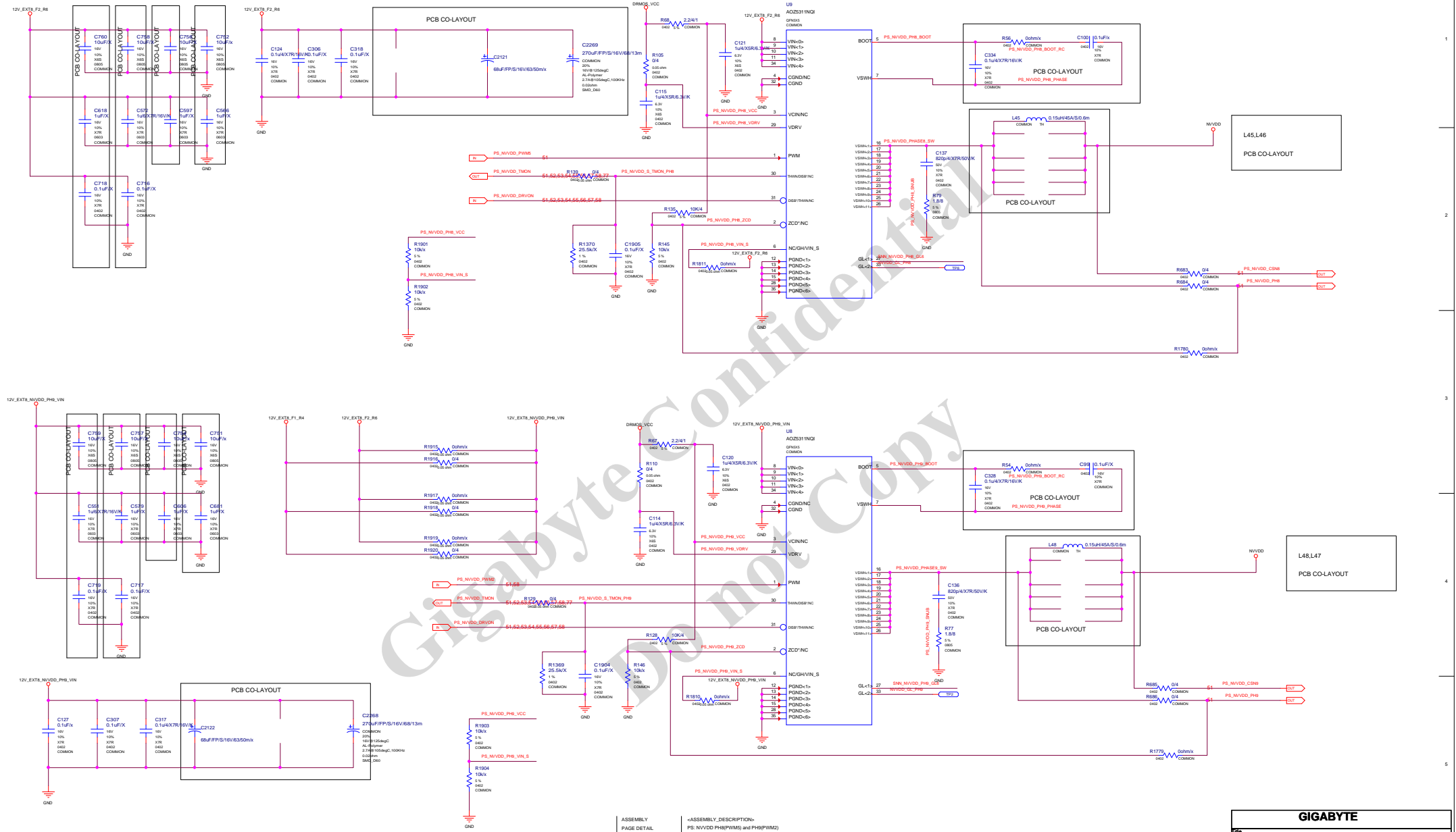
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PS: NVVDD PH 8 (PWM5), PH 9(PWM2)



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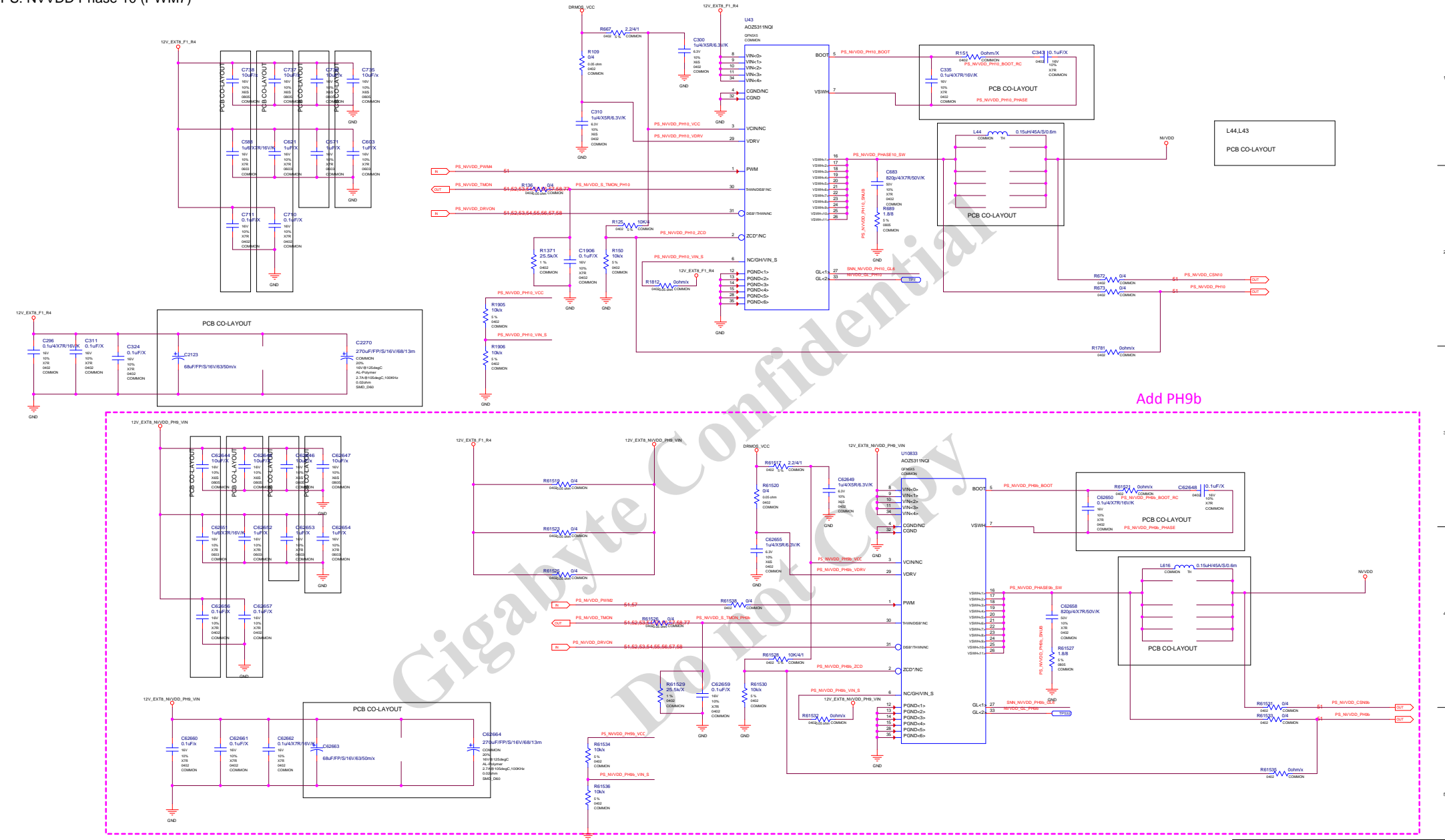
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Size	Document Number		Rev
Custom	GV-N3090AORUS M-24GD		1.01
Date:	Tuesday, August 25, 2020	Sheet	57 of 82

PS: NVVDD Phase 10 (PWM7)



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Title			
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Size	Document Number	Rev	
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Date:	Tuesday, August 25, 2020	Sheet	59 of 82

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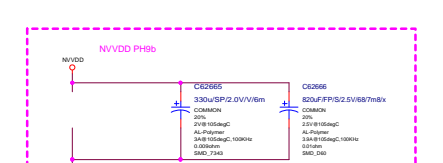
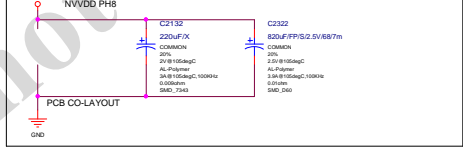
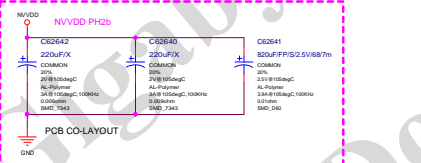
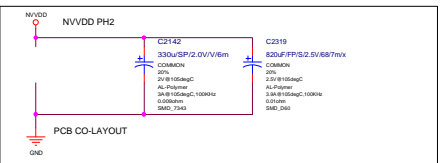
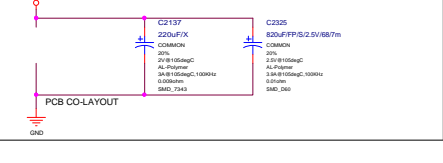
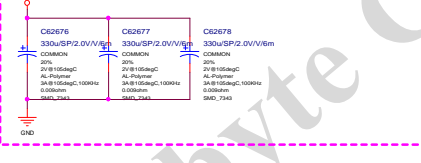
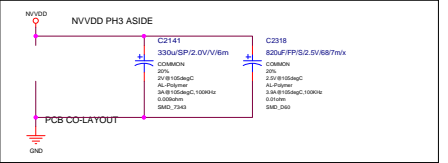
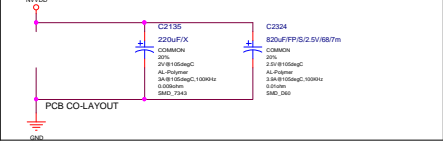
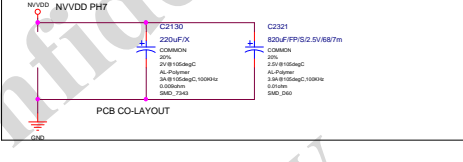
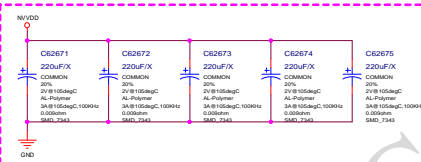
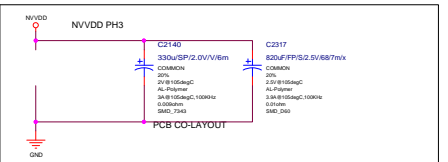
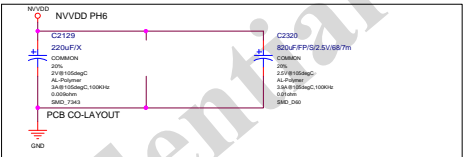
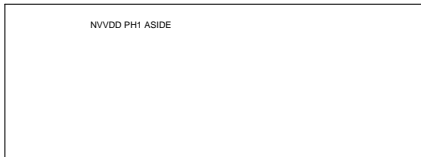
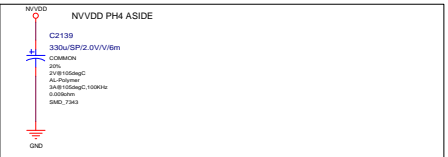
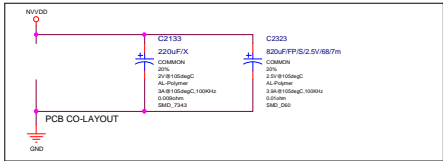
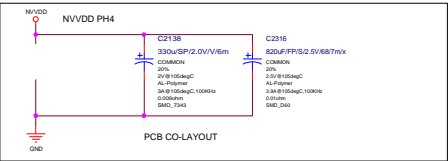
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Title		PCIE	
Size	Custom	Document Number	Rev
		GV-N3090AORUS M-24GD	1.01
Date		Tuesday, August 26, 2026	Sheet 60 of 82

REFER TO PCB FOR BOM STUFFING



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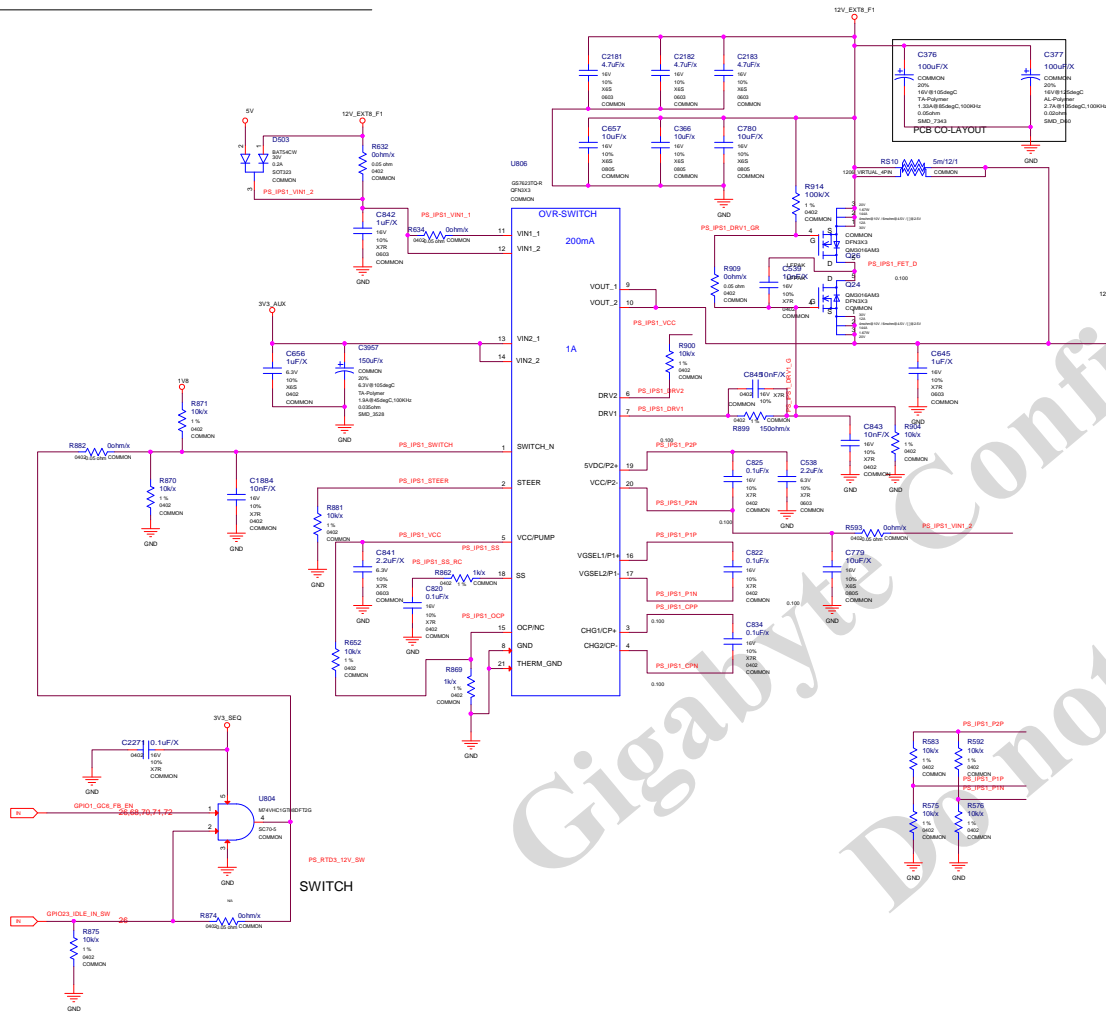
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Size	Document Number	Rev	
Custom	GV-N3090AORUS M-24GD	1.01	
Date: Tuesday, August 26, 2025		Sheet	82 of 82

PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPI01	GPI023	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: INPUT SWITCH RTD3

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PCIE			
Size	Custom	Document Number	Rev
		GV-N3090AORUS M-24GD	1.01
Date:	Tuesday, August 25, 2020		Sheet 63 of 82

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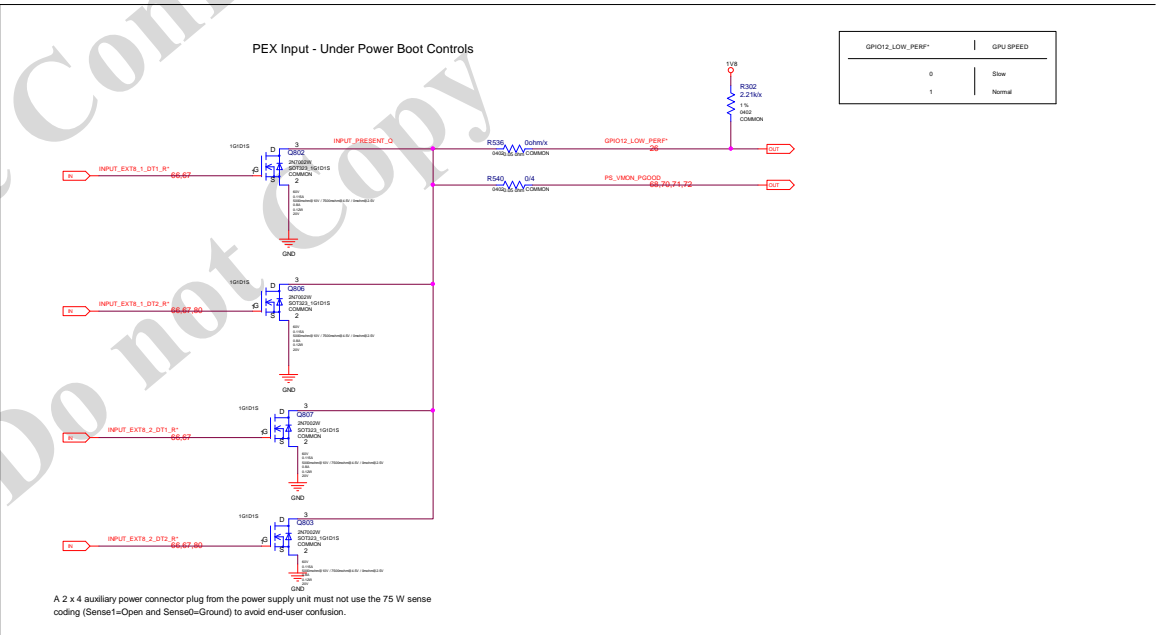
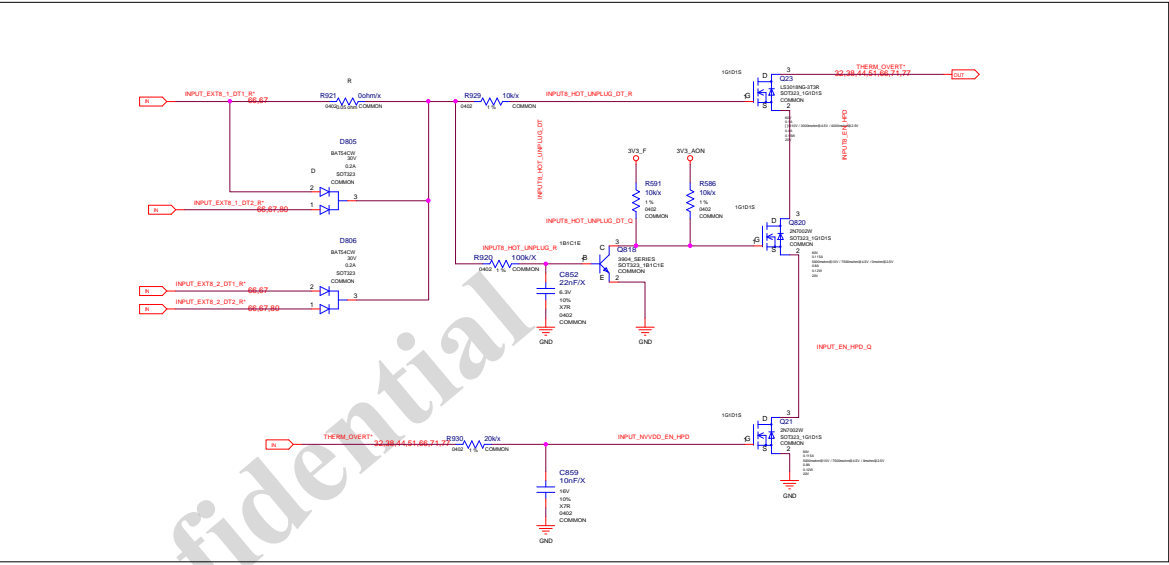
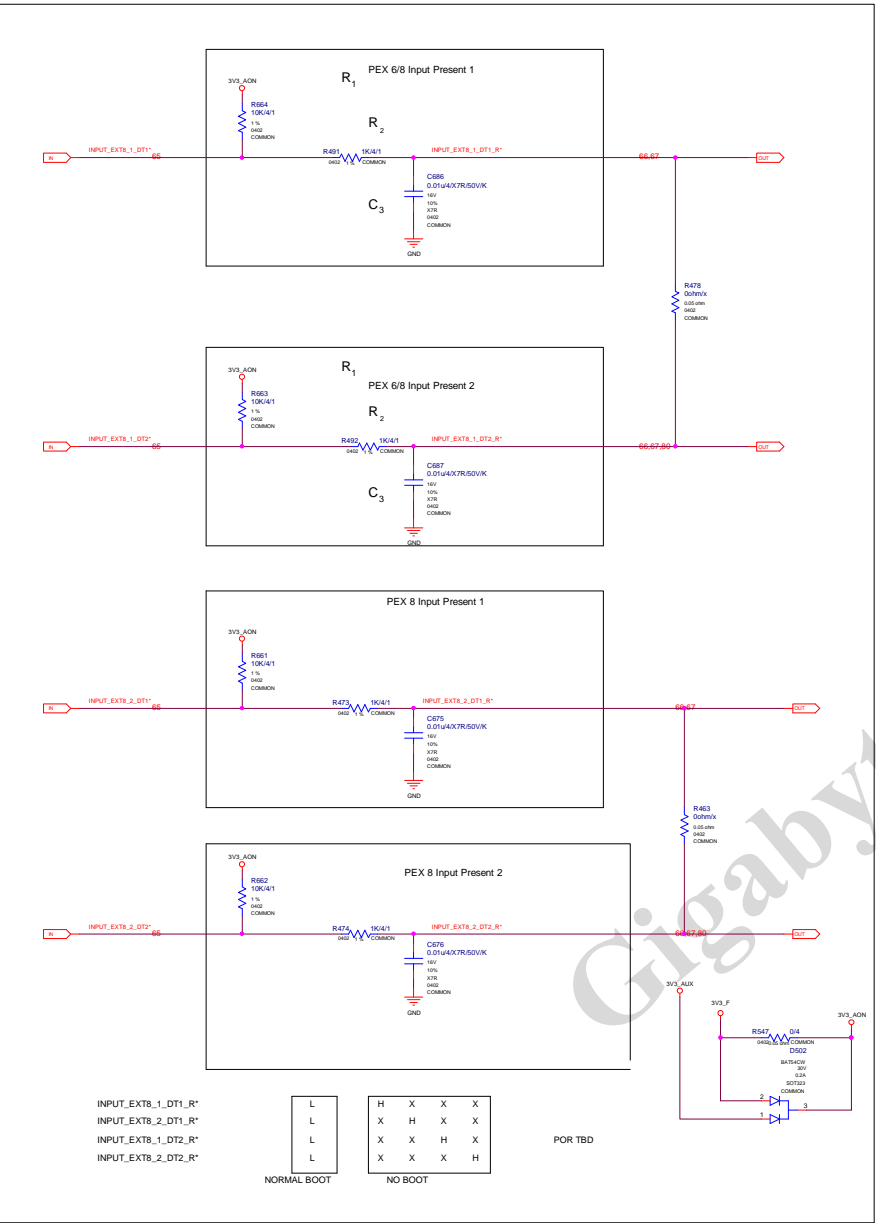
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Title		PCIE	
Size	Document Number	Rev	
Custom	GV-N3090AORUS M-24GD	1.01	
Date: Tuesday, August 26, 2025		Sheet	64 of 82

PS: 12V Current Steering & Hot Unplug Detect



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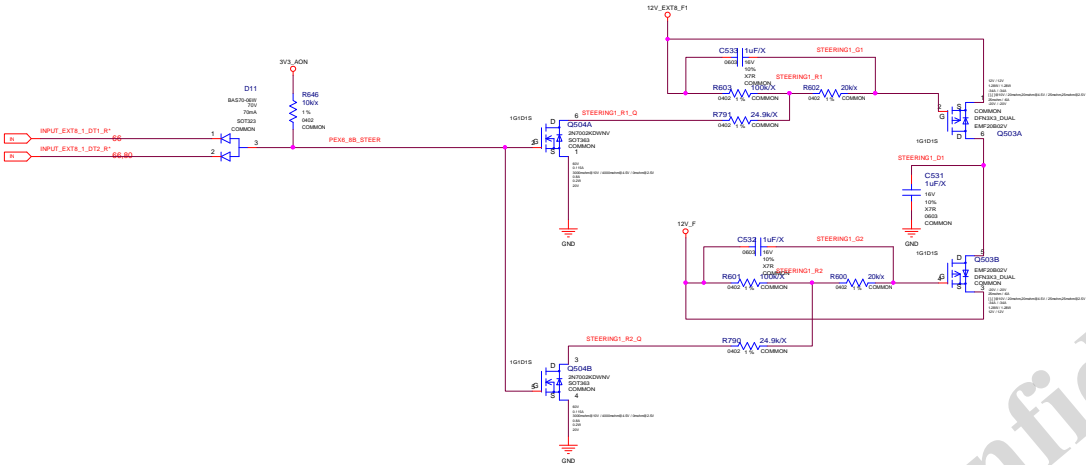
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Doc Number	GV-N3090AORUS M-24GD		
Rev	1.01		
Date	Tuesday, August 26, 2025		
Sheet	66	of 82	

PS: Discrete Steering

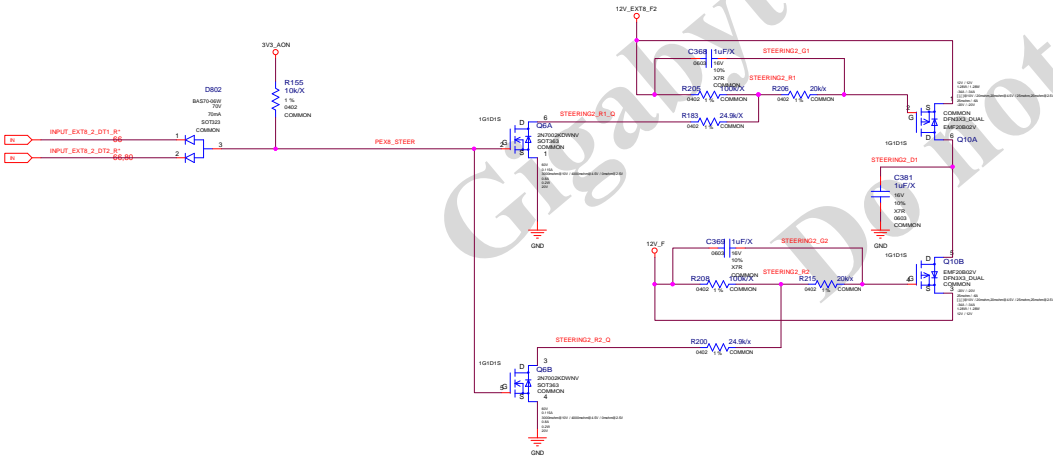
12V CURRENT STEERING (UNDER POWER BOOT):

PEX12V AND 12V_EXT8_F1



NO STUFF BY DEFAULT REF ONLY

PEX12V AND 12V_EXT8_F2



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ASSEMBLY PAGE DETAIL
PS: Discrete Power Steering

GIGABYTE			
File	PCIE		
Size	Document Number	Rev	
Custom	GV-N3090AORUS M-24GD	1.01	
Date:	Tuesday, August 25, 2020	Sheet	87 of 82

PS: Pre-Filter

Route the trace to PEX Golden Finger

STUFF IF USING 2XMUX

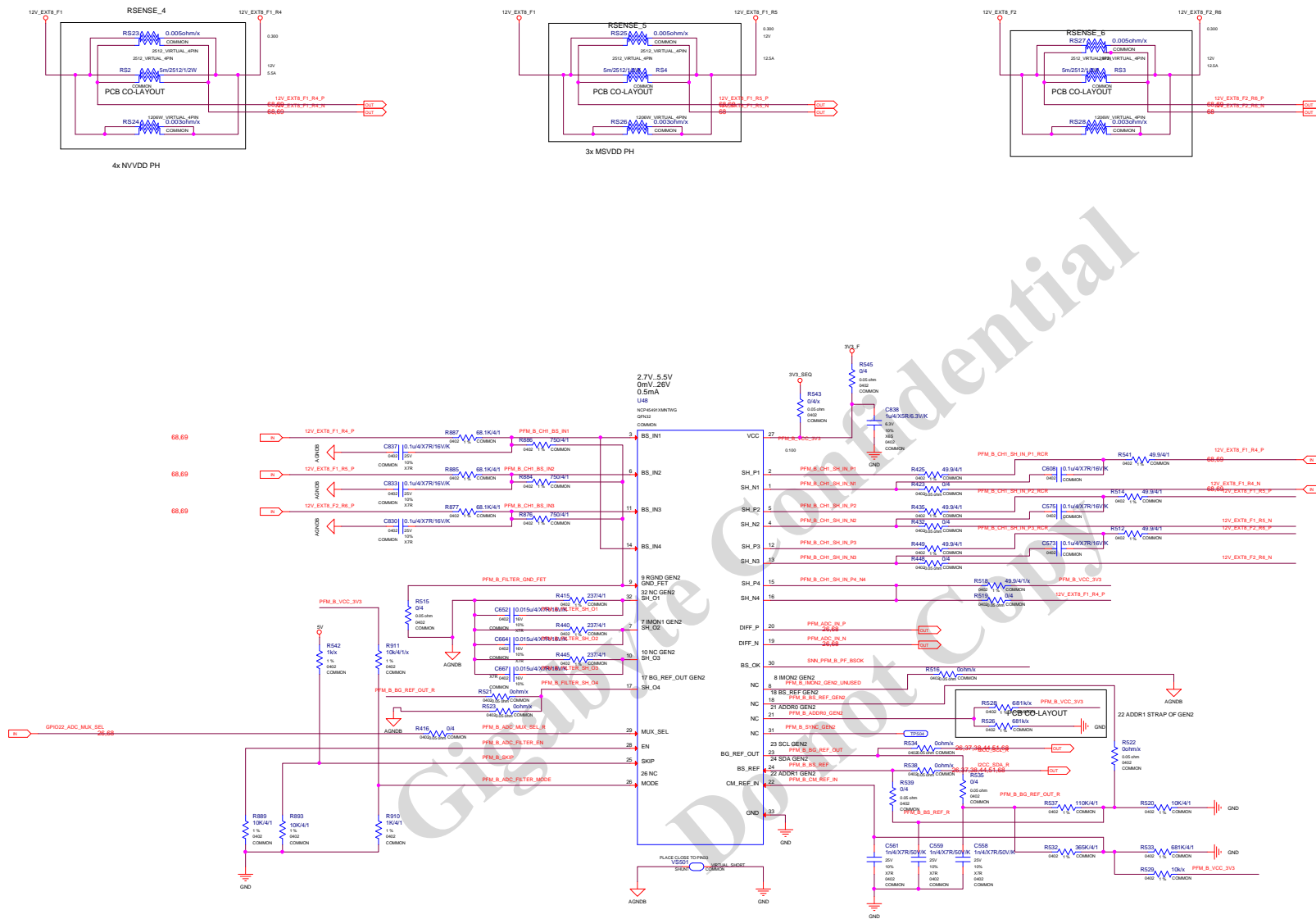
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0mV..26V
0.5mA
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VDD
COMMONASSEMBLY
PAGE DETAILASSEMBLY DESCRIPTION
PS: PRE-FILTER

GIGABYTE

File	PCIE	Rev	1.01
Doc	Document Number		
Part	GV-N3090AORUS M-24GD		
Date	Tuesday, August 28, 2023	Sheet	68 of 82

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PS: Pre-Filter B



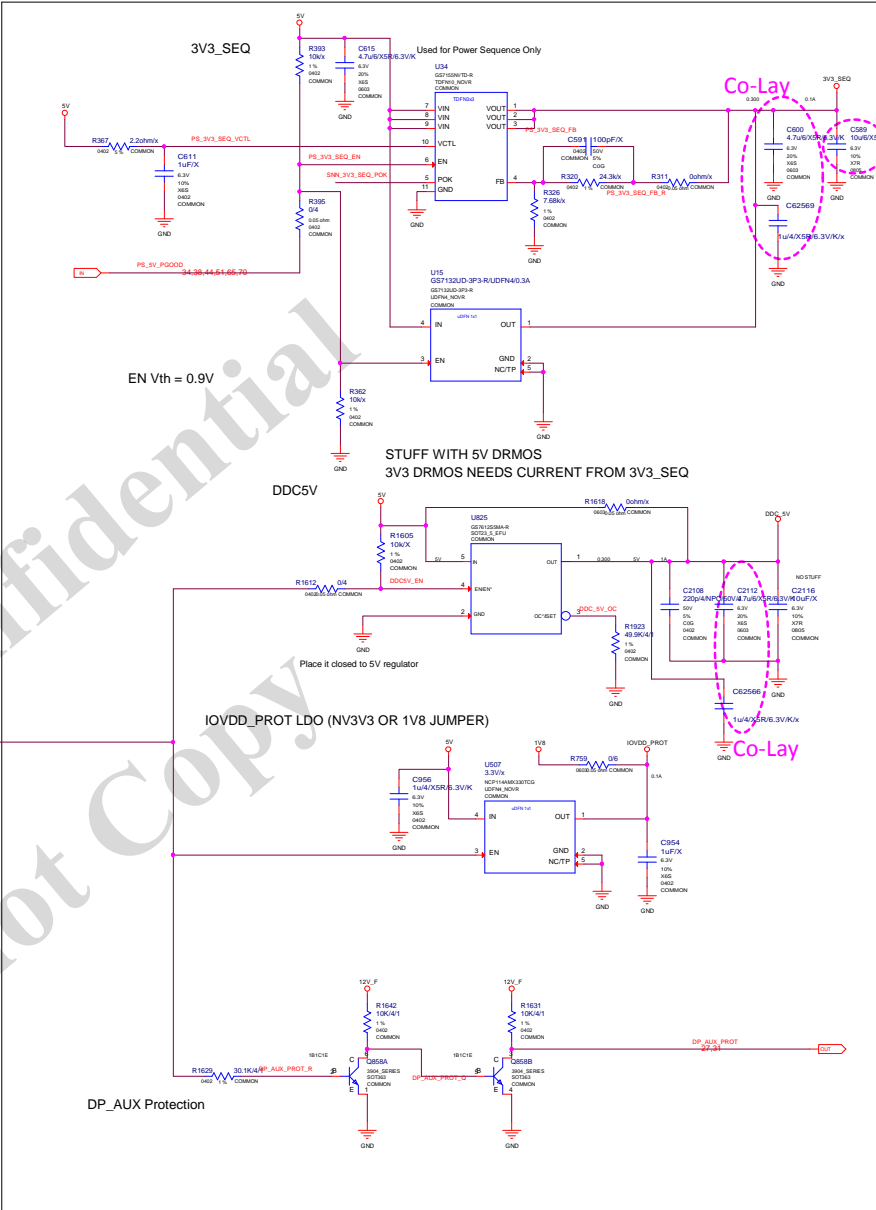
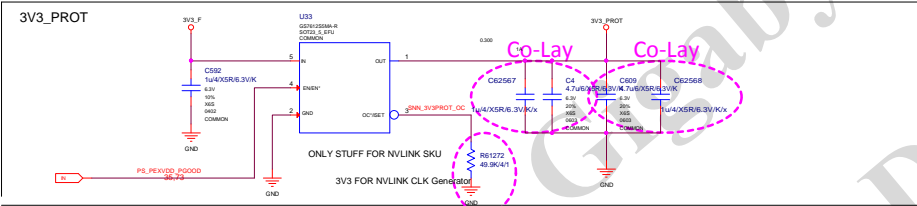
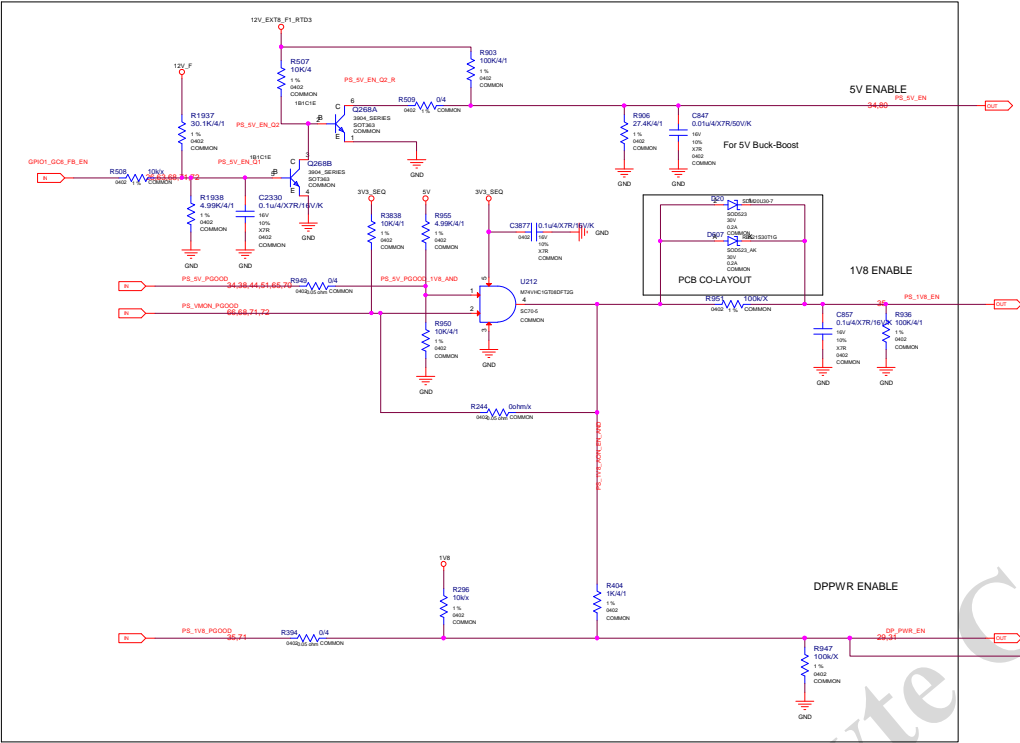
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Custom	GV-N3090AORUS M-24GD	1.01	
Date:	Tuesday, August 25, 2020	Sheet	69 of 82

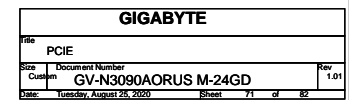
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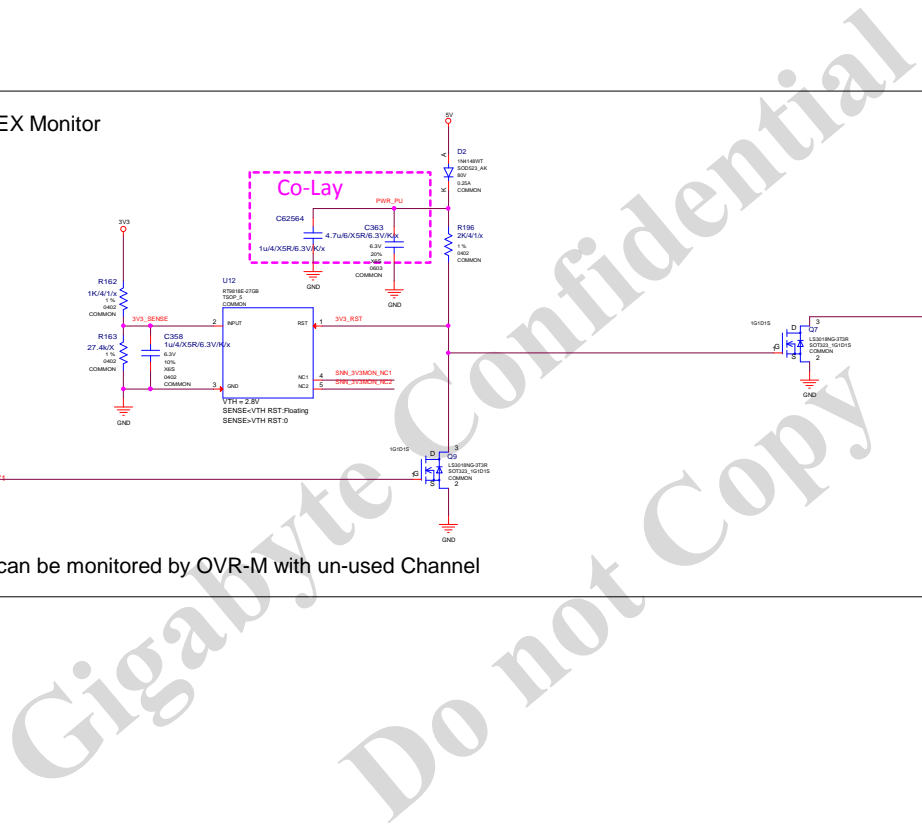


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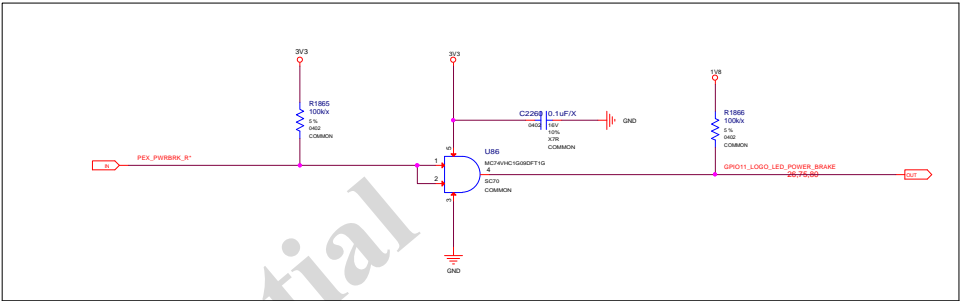
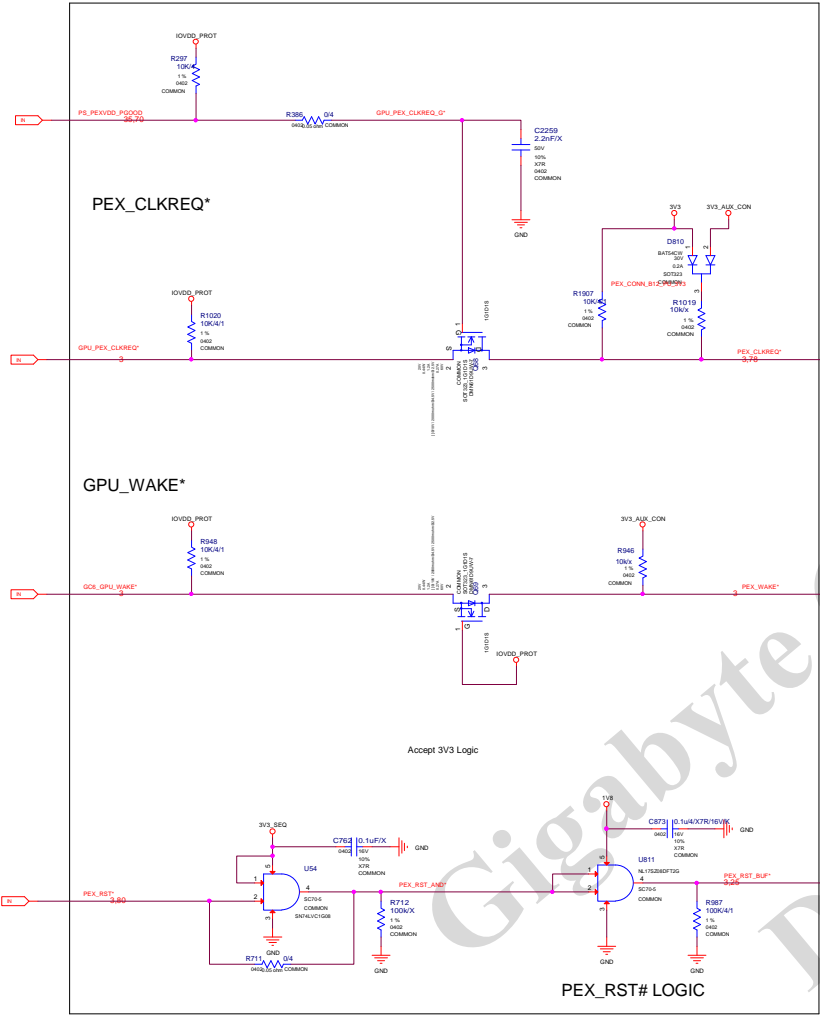
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File	PCI-E		
Doc Number	GV-N3090AORUS M-24GD		
Rev	1.01		
Date	Tuesday, August 28, 2023		
Sheet	70	of 82	





3V3 can be monitored by OVR-M with un-used Channel



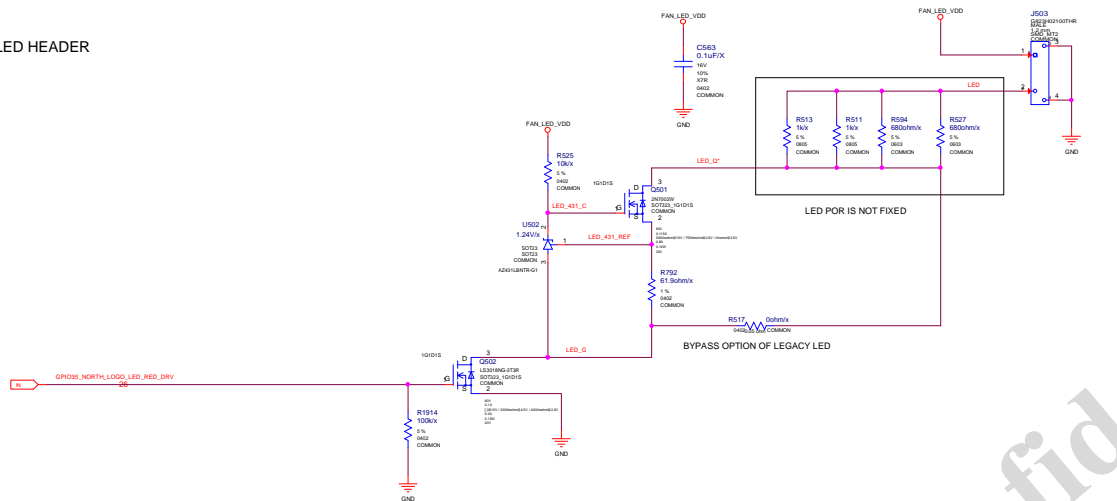
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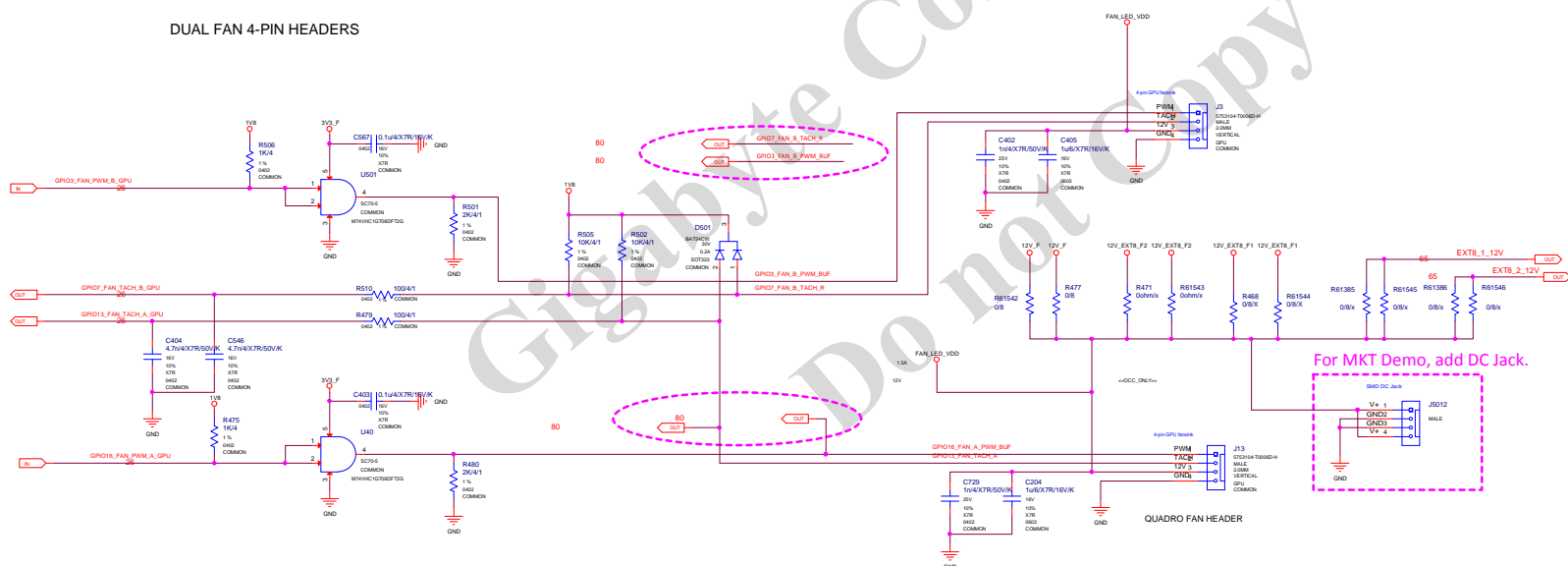
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		GV-N3090AORUS M-24GD	1.01
Date:	Tuesday, August 25, 2020	Sheet	73 of 82

2-PIN LED HEADER



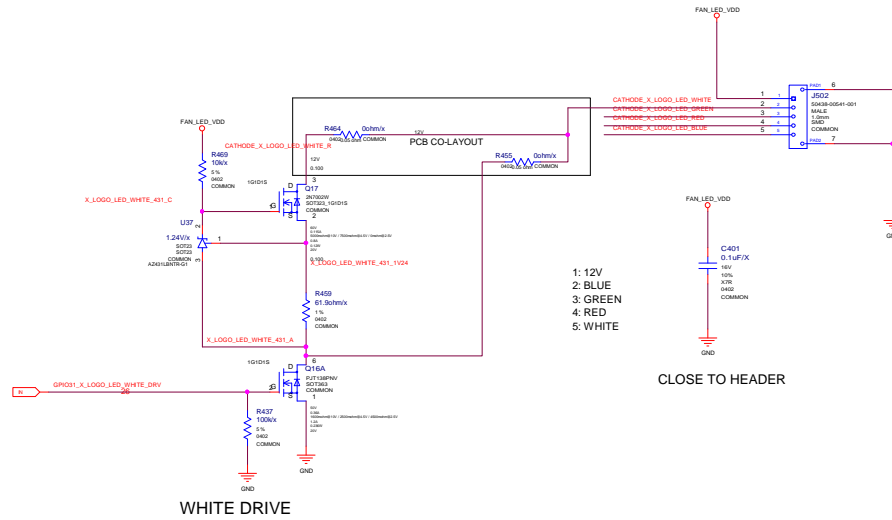
DUAL FAN 4-PIN HEADERS



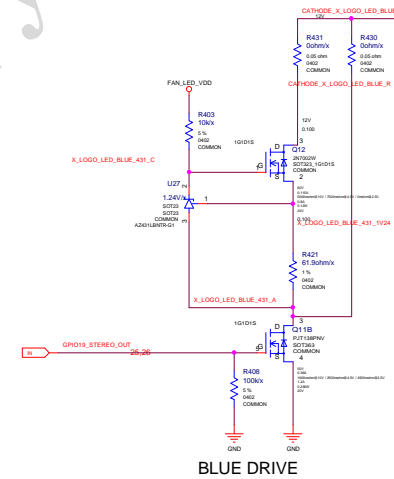
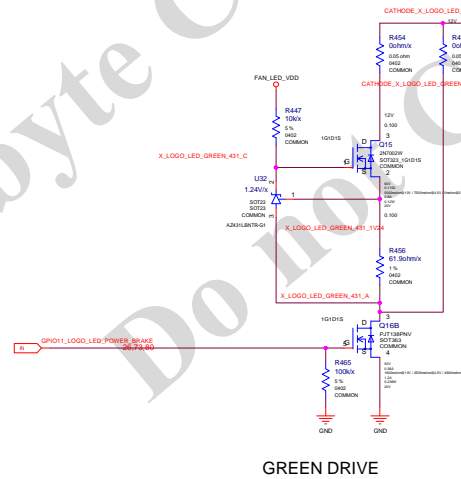
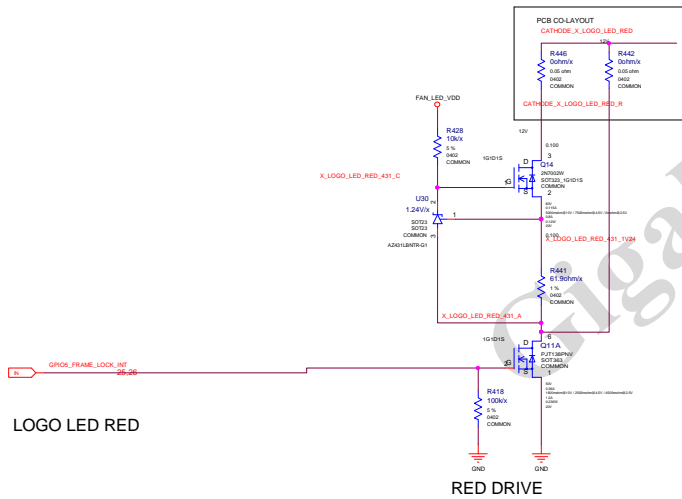
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ASSEMBLY
PAGE DETAIL

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<ASSEMBLY_DESCRIPTION>
MISC: LED & FAN
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CONNECTOR SIZE TO FIT LAYOUT
ALL CIRCUIT NO STUFF BY DEFAULT
ALINGN WITH PASH
IF ADDTIONAL POWER CONSUPTION R
NEEDED, IT SHOULD BE ON LED MOD.

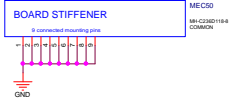


Mechanical: Mounting holes

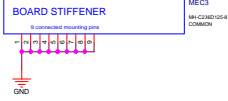
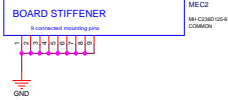
BK up



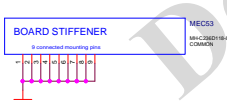
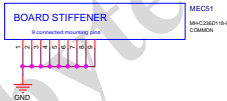
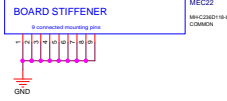
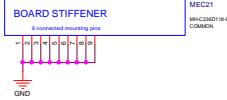
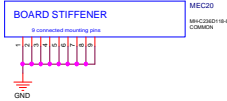
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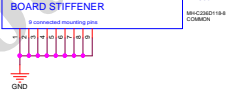
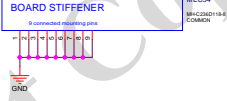
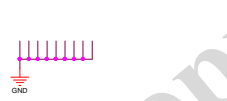
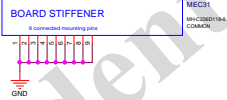
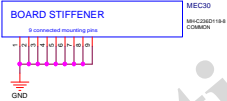
GPU



MOS



Backplane

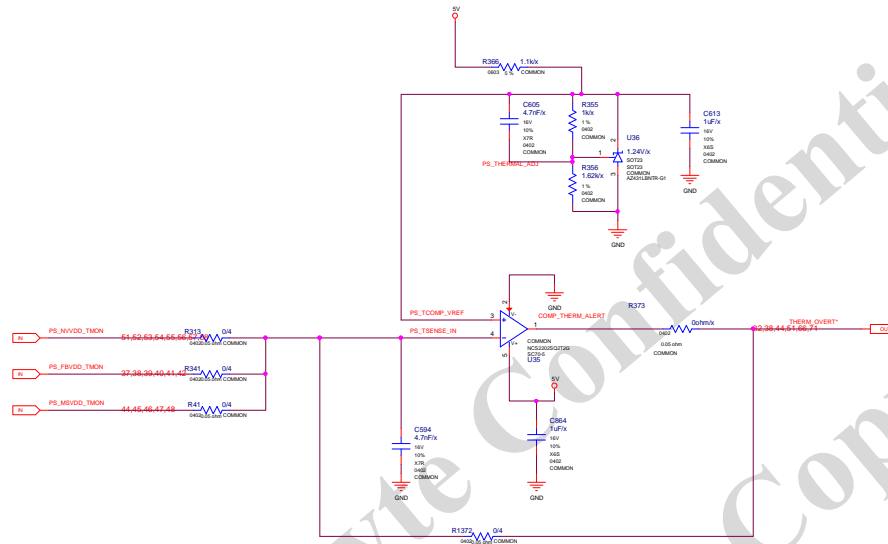


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ASSEMBLY
PAGE DETAIL
MECH

GIGABYTE			
File	PCIE		
Size	Document Number	Rev	
Common	GV-N3090AORUS M-24GD	1.01	
Date	Tuesday, August 26, 2025	Sheet	76 of 82

VR THERMAL PROTECTION



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ASSEMBLY
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VR Thermal Protection

PCI TERM

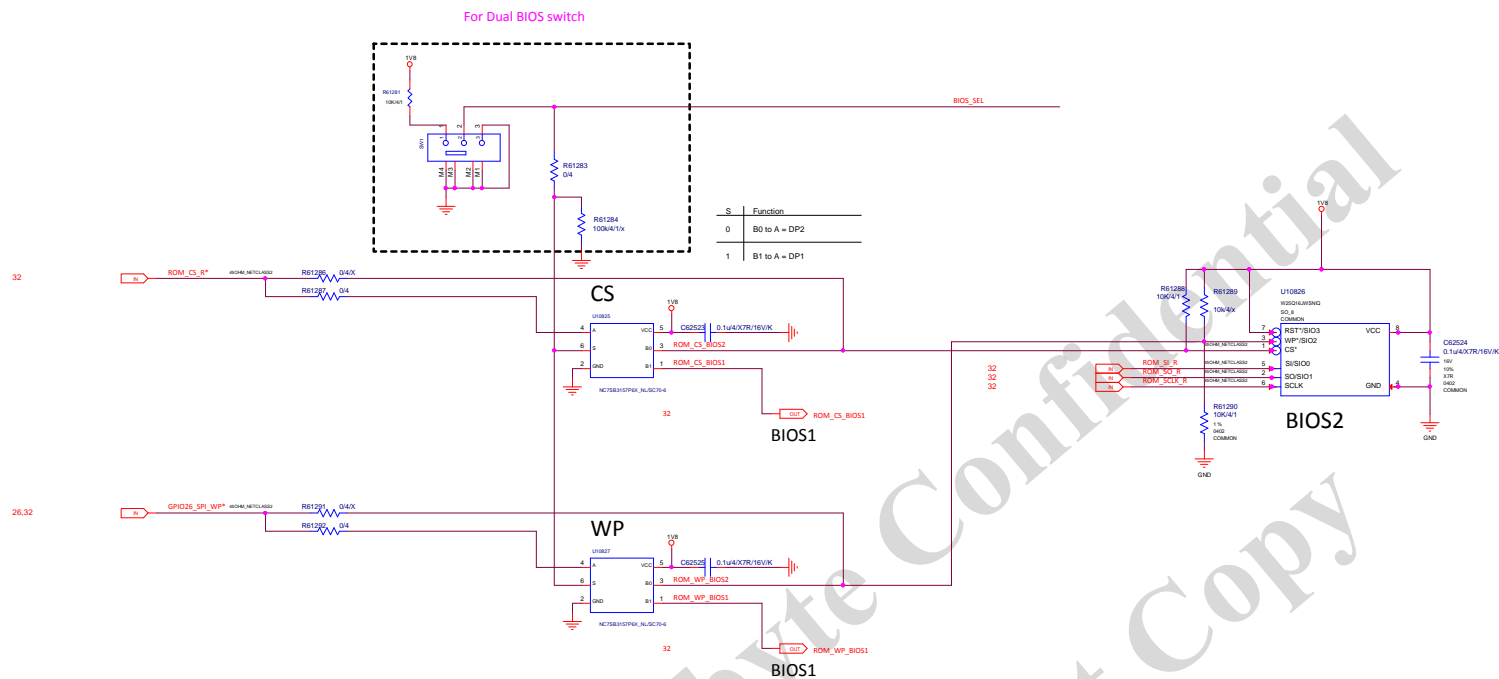


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ASSEMBLY
PAGE DETAIL
PCIE TERM

GIGABYTE			
PCIE			
Doc	Document Number	Rev	1.01
GV-N3090AORUS M-24GD			
Date	Thursday, August 26, 2020	Sheet	78 of 82

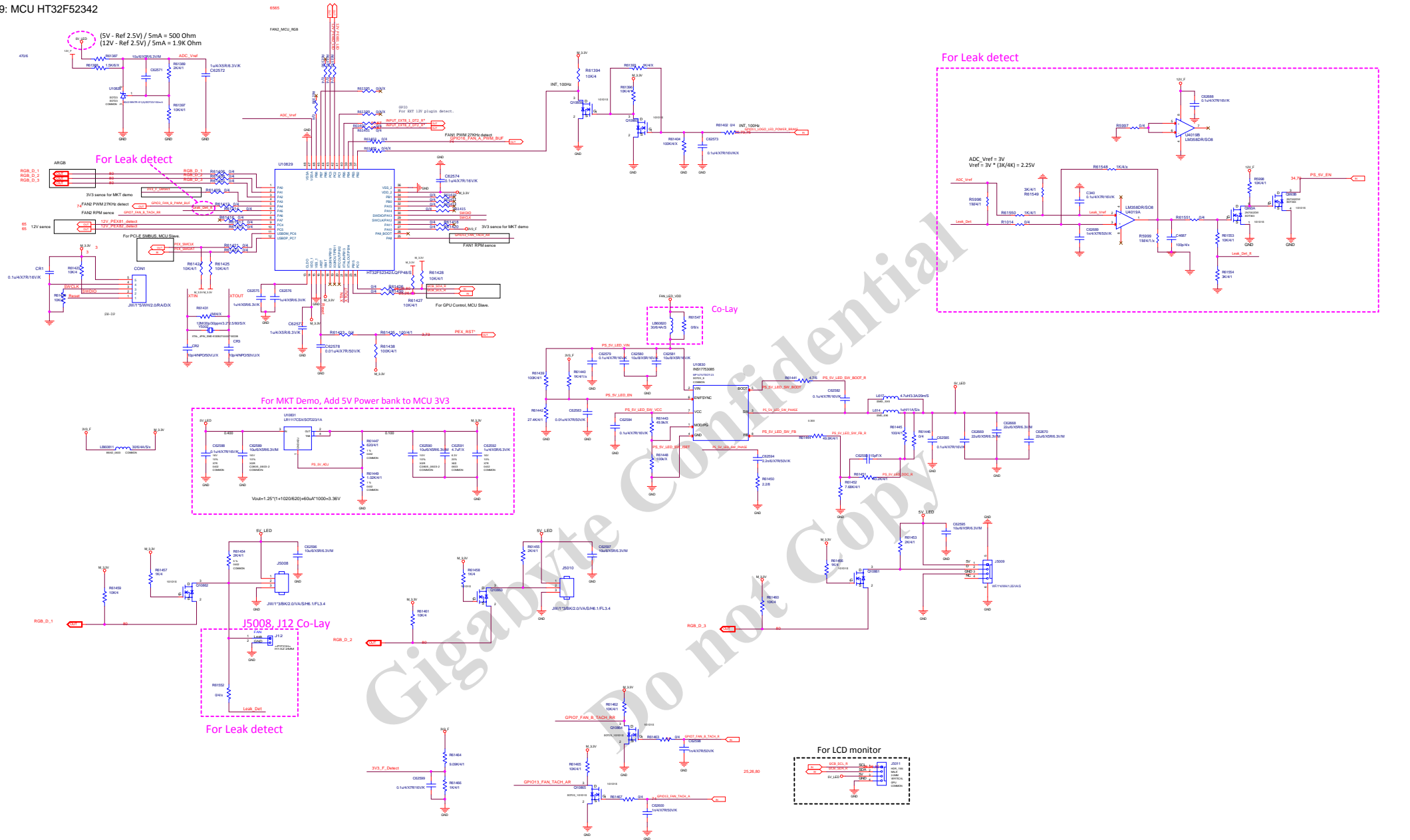
BIOS Switch



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MCU ZERO POWER IDLE



Del RGB LED

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MECH

GIGABYTE			
File PCIE			
Size	Document Number		Rev
Content	GV-N3090AORUS M-24GD		1.01
Date	Tuesday, August 26, 2025	Sheet	81 of 82

History

Date	Modify
2018.07.21	First version

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GIGABYTE			
Title PCIE			
Size	Document Number		Rev
Custom	GV-N3090AORUS M-24GD		1.01
Date	Tuesday, August 25, 2020	Sheet 12	of 12