1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

J16 MLB

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
13	0002231663	ENGINEERING RELEASED	2013-08-10

LAST_MODIFIED=Sat Aug 10 21:13:36 2013

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4	Holes/PD parts	J16_DG 04/21/2013
5	CPU DMI/PEG/FDI/RSVD	J17 04/21/2013
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11	PCH RTC/HDA/JTAG/SATA/CLK	J17 04/21/2013
12	PCH DMI/FDI/PM/GFX/PCI	J17 04/21/2013
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14	PCH GPIO/MISC/NCTF	J17 04/21/2013
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18	CPU & PCH XDP	MASTER 04/21/2013
19	Chipset Support	J17 04/21/2013
20	Project Chipset Support	MASTER 04/21/2013
21	CPU Memory S3 Support	J17 04/21/2013
22	DDR3 VREF MARGINING	J17 04/21/2013
23	DDR3 SO-DIMM Connector A	J16_MLB_IG 05/01/2013
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25	DDR3 ALIASES AND BITSWAPS	J16_MLB_IG 05/01/2013
26	Thunderbolt Host (1 of 2)	J16_MLB_IG 05/01/2013
27	Thunderbolt Host (2 of 2)	J16_MLB_IG 05/01/2013
28	Thunderbolt Power Support	J16_MLB_IG 05/01/2013
29	Thunderbolt Connector A	J16_MLB_IG 05/01/2013
30	Thunderbolt Connector B	J16_MLB_IG 04/21/2013
31	TBT DDC Crossbar	J16_DG 05/01/2013
32	AIRPORT/BT	J16_MLB_IG 05/01/2013
33	SATA/SSD Connectors	MASTER 05/01/2013
34	HDD Connector	J16_MLB_IG 05/01/2013
35	ETHERNET PHY (CAESAR IV)	J16_MLB_IG 05/01/2013
36	Ethernet Support & Connector	J16_MLB_IG 05/01/2013
37	SD READER CONNECTOR	J16_MLB_IG 05/01/2013
38	Camera Controller	J16_MLB_IG 05/01/2013
39	Camera Controller Support	J16_MLB_IG 05/01/2013
40	Internal DP Support	J16_MLB_IG 04/21/2013
41	Internal DP MUXing	J16_DG 05/01/2013
42	EXTERNAL USB PORTS A & B	J16_MLB_IG 05/01/2013
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44	SMC	J16_MLB_IG 06/11/2013
45	SMC Support	J16_TONY 06/17/2013
46	SPI and Debug Connector	J16_TONY 04/21/2013
47	SMBus Connections	J16_DG 06/11/2013
48	I and V Sense	J16_TONY
49	I and V Sense(Continued)	J16_TONY 06/03/2013
50	Temperature Sensors	J16_FIYIN 06/11/2013
51	System Fan	J16_MLB_IG 05/01/2013
52	AUDIO: CODEC/REGULATORS	J16_MLB_IG 05/01/2013
53	AUDIO: HEADPHONE AMP	J16_MLB_IG 05/01/2013
54	AUDIO: LEFT SPKR AMP	J16_MLB_IG 05/01/2013
55	AUDIO: RIGHT SPKR AMP	J16_MLB_IG 05/01/2013
56	AUDIO: Jack, Mikey, CHS Switch	J16_MLB_IG 05/01/2013
57	Audio: Spkr/Mic Conn.	J16_MLB_IG 05/01/2013
58	AUDIO: Detects/Grounding	J16_MLB_IG 05/01/2013
59	AUDIO: Speaker ID	J16_MLB_IG 05/01/2013
60	Power Connectors / VReg G3Hot	J16_MLB_IG 05/01/2013
61	VReg CPU VCC Cntl	J16_MLB_IG 04/21/2013
62	VReg CPU VCC Phases	J16_DG 06/17/2013
63	VReg VDDQ S3	J16_ROSSANA 04/21/2013
64	VReg PCH/GPU/TBT 1V05 S0	J16_DG 05/01/2013
65	VReg 3.3V S5/5V S4	J16_MLB_IG 04/21/2013
66	VReg GPU VDDQ	J16_DG 06/17/2013
67	VReg GPU Core	J16_ROSSANA 05/01/2013
68	LCD Backlight Driver (LP8561)	J16_MLB_IG 05/01/2013
69	FET-Controlled S0 and S4	MASTER 05/01/2013
70	PM Regulator Enables	MASTER 05/01/2013
71	PM Power Good	J16_MLB_IG 04/21/2013
72	KEPLER PCI-E	J16_DG 04/21/2013
73	KEPLER CORE/FB POWER	J16_DG 04/21/2013
74	KEPLER FRAME BUFFER I/F	J16_DG 04/21/2013
75	GDDR5 Frame Buffer A	J16_DG 04/21/2013
76	GDDR5 Frame Buffer B	J16_DG 04/21/2013
77	KEPLER EDP/DP/GPIO	J16_DG 04/21/2013
78	KEPLER GPIOS,CLK & STRAPS	J16_DG 04/21/2013
79	KEPLER PEX PWR/GNDS	J16_DG 04/21/2013
80	Power Connectors/Aliases	MASTER 04/21/2013
81	Signal Aliases	MASTER 04/21/2013
82	Unused Signal Aliases	MASTER 04/21/2013
83	Functional / ICT Test	J16_DG 04/21/2013
84	J16 RULE DEFINITIONS	J16_DG 06/03/2013
85	DDR3 Constraints	J16_NICK 06/03/2013
86	CPU PCIe Constraints	J16_NICK 04/21/2013
87	PCH PCIe/DMI Constaints	J16_DG 05/30/2013
88	SATA/FDI/XDP Constraints	J16_NICK 05/30/2013
89	PCH and BR Constraints	J16_NICK 05/30/2013
90	USB/Ethernet/SD Constraints	J16_NICK 06/03/2013
91	SMBus/Sensor Constraints	J16_TONY 04/21/2013
92	VReg Constraints	J16_DG 04/21/2013
93	CPU VReg Constraints	J16_DG 04/21/2013
94	Platform VReg Constraints	MASTER 04/21/2013
95	TBT/DP Constraints	MASTER 05/30/2013
96	GDDR5/GPU Constraints	J16_NICK 04/21/2013
97	BLC Constraints	J16_DG

DRAWING
TITLE=J16
ABBREV=DRAWING
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DRAWING TITLE: SCHEM,MLB,J16

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DRAWING NUMBER: 051-9889 SIZE: D
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Main BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
985-0035	PCBA,MLB,DEV,J16	DEVELOPMENT,J16_DEVEL
639-4281	PCBA,MLB,107GX,VRAM_HYNIX,BETTER,J16	J16,J16_COMMON,CPU:BETTER,GPU:107GX,FBA,FBB,FB:BOTH_HYNIX,SSD:Y,EEEE:F9RR
639-4286	PCBA,MLB,107GX,VRAM_ELPIDA,BETTER,J16	J16,J16_COMMON,CPU:BETTER,GPU:107GX,FBA,FBB,FB:BOTH_ELPIDA,SSD:Y,EEEE:F9T5
639-4282	PCBA,MLB,107GX,VRAM_HYNIX,CTO,J16	J16,J16_COMMON,CPU:CTO,GPU:107GX,FBA,FBB,FB:BOTH_HYNIX,SSD:Y,EEEE:F9T3
639-4287	PCBA,MLB,107GX,VRAM_ELPIDA,CTO,J16	J16,J16_COMMON,CPU:CTO,GPU:107GX,FBA,FBB,FB:BOTH_ELPIDA,SSD:Y,EEEE:F9RW

BOM Groups

BOM GROUP	BOM OPTIONS
J16_COMMON	COMMON,ALTERNATE,J16_COMMON1,J16_COMMON2,J16_PROGPARTS,J16_PRODUCTION
J16_COMMON1	XDP,SPEAKERID,TBTHV:P12V,CPUVCC:3PHASE,EXT_GPU:YES,VDDQ:P1V5
J16_PROGPARTS	SMC:PROG,BOOTROM:PROG,T29ROM:PROG,CIVROM:PROG,CAMROM:PROG
J16_DEVEL	XDP_CONN,LPCPLUS,DDRVREF_DAC,DEVEL_SENSORS,DEVEL_AUDIO
DEVEL_SENSORS	AP_ISNS:Y,HDD_IVSNS:Y,TEMPSNSDEV
J16_PRODUCTION	AP_ISNS:N,HDD_IVSNS:N

ADD 'J16_PRODUCTION' AT REVA RELEASE

CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4610	1	HSW,SR14J,PRQ,C0,2.9G,65W,4+2,1.15,6M,LGA	CPU	CRITICAL	CPU:BETTER
337S4608	1	HSW,SR14H,PRQ,C0,3.1G,65W,4+2,1.2,8M,LGA	CPU	CRITICAL	CPU:CTO

CPU Socket

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0080	1	SOCKET,MOLEX,LGA1150,CPU-LF	U0500	CRITICAL	

ASIC Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4541	1	IC,LFT-D,SR19S87,C2,PBQFCBGA708,23X22MM	U1100	CRITICAL	
338S1113	1	IC,TBT,CR-4C,B1,PBQ,C1O,288 12X12 FC-CSP	U2800	CRITICAL	
343S0616	1	IC,BCM57766A,CIV+,A0,8X8	U3900	CRITICAL	
353S3908	1	IC,LP8561,LED BLKT CTLR,LLP24,80-F	U8100	CRITICAL	

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S3928	1	IC,EFI,V0112,J16G	U5210	CRITICAL	BOOTROM:PROG
335S0807	1	IC,64 MBIT SPI SERIAL FLASH	U5210	CRITICAL	BOOTROM:BLANK
341S3903	1	IC,SMC-A3,V2.16A4,PROTO0,J16G	U5000	CRITICAL	SMC:PROG
338S1159	1	IC,SMC12-A3,40MHZ/50MIPS,SCPL FW,157BGA	U5000	CRITICAL	SMC:BLANK
341S3859	1	IC,TBT,EEPROM,CR,V23.10,J16	U2890	CRITICAL	T29ROM:PROG
335S0865	1	IC,EEPROM,SERIAL,256KB,MLP8	U2890	CRITICAL	T29ROM:BLANK
341S3912	1	IC,ENET SPI ROM,NUMONYX,V1.15,J16/J17	U3990	CRITICAL	CIVROM:PROG
335S0862	1	IC,SERIAL FLASH,2MBIT,2.7V,REV F	U3990	CRITICAL	CIVROM:BLANK
341S3778	1	IC,CAMERA,FLASH,V7230,J16/J17	U4202	CRITICAL	CAMROM:PROG
335S0852	1	IC,FLASH,SPI,1MBIT,3V3	U4202	CRITICAL	CAMROM:BLANK

NEED NEW EFI,SMC PROG PARTS

Bar Code Labels / EEEE #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7896	1	MLB LABEL,2D	EEEE_F9RR	CRITICAL	EEEE:F9RR
825-7896	1	MLB LABEL,2D	EEEE_F9T5	CRITICAL	EEEE:F9T5
825-7896	1	MLB LABEL,2D	EEEE_F9T3	CRITICAL	EEEE:F9T3
825-7896	1	MLB LABEL,2D	EEEE_F9RW	CRITICAL	EEEE:F9RW

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-9889	1	SCH,MLB,J16	SCH	CRITICAL	J16
820-3482	1	PCBF,MLB,J16	PCB	CRITICAL	J16

GPU & VRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4427	1	IC,GPU,NV,GK107-GX,PS,926MHZ,2.5GHZ	U8700	CRITICAL	GPU:107GX
333S0630	4	IC,GDDR5,2GBIT,64MX32,5GBPS,GEMMA-DIE	U9200,U9250,U9300,U9350	CRITICAL	FB:BOTH_HYNIX
333S0695	4	IC,GDDR5,2GBIT,64MX32,5GBPS,B-DIE	U9200,U9250,U9300,U9350	CRITICAL	FB:BOTH_ELPIDA

Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0147	377S0126		ALL	USB Diode Array
377S0124	377S0057		ALL	TVS
376S0975	376S1081		ALL	P/NCh dual FET
155S0578	155S0367		ALL	120OHM EMI BEAD
128S0368	128S0365		ALL	150UF AL POLY
128S0298	128S0293		ALL	330 UF AL POLY
138S0681	138S0638		ALL	Taiyo 10uf 805 alt
197S0481	197S0480		Y1905	25MHz PCH Xtal
197S0464	197S0477		Y9700	27 MHz GPU Xtal
197S0466	197S0477		Y9700	27 MHz GPU Xtal
197S0479	197S0478		Y4200	12 MHz Cam. Xtal
341S3913	341S3912		U3990	Enet ROM,ATMEL,V1.15
377S0155	377S0104		ALL	USB Diode
138S0860	138S0775		ALL	Single-source 1uF 402
138S0859	138S0788		ALL	Single-source 10uF
107S0251	107S0249		ALL	Sense resistor
138S0648	138S0652		ALL	4.7uF GFX decoupling
138S0746	138S0705		ALL	10uF alt;Audio
138S0715	138S0740		ALL	4.7uF GFX decoupling
107S0254	107S0241		ALL	5mOhm Sense Resistor
107S0250	107S0248		ALL	3mOhm Sense Resistor

R5400,R5520,R5530

SYNC MASTER=MASTER SYNC DATE=04/21/2013

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BOM Configuration

Apple Inc.

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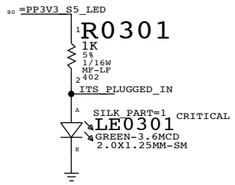
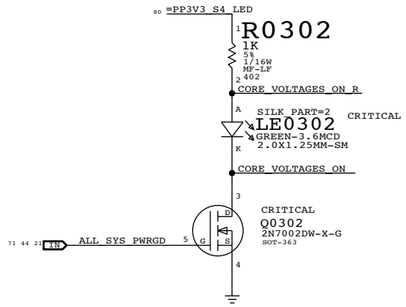
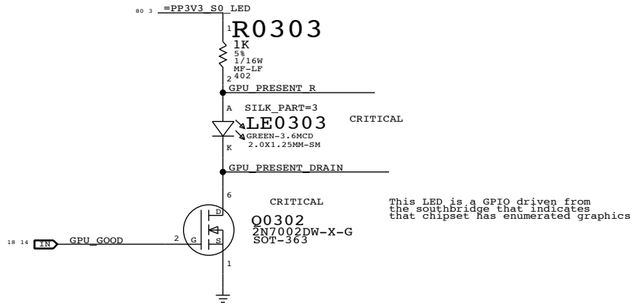
S5 Led



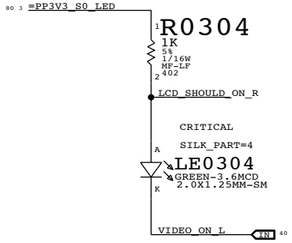
ALL_SYS_PWRGD Led



GPU GOOD Led



VIDEO ON Led



SYNC MASTER=J16 MLB IG SYNC DATE=05/01/2013

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DEBUG LEDS

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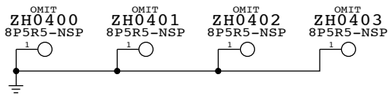
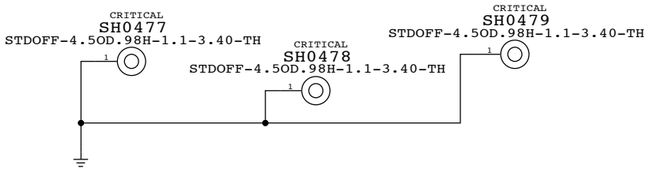
CPU Heatsink

4mm Plated Holes (998-0850)



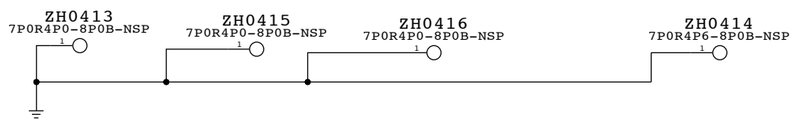
GPU HEATSINK MOUNTING FEATURES

(860-1532)



Rear Cover

998-4559 (Plated holes, 4mm inner diameter, 8mm pad)
998-5089 (ZH0414) near BLC has slightly larger hole to allow for grommet

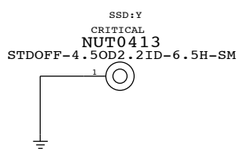


WIRELESS CARD MTG HOLES

998-4560 (Plated holes, 2.3mm inner diameter, 4.3mm pad)

SSD STANDOFF

APN: 860-1624



SYNC MASTER=J16 DG SYNC DATE=04/21/2013

PAGE TITLE: Holes/PD parts

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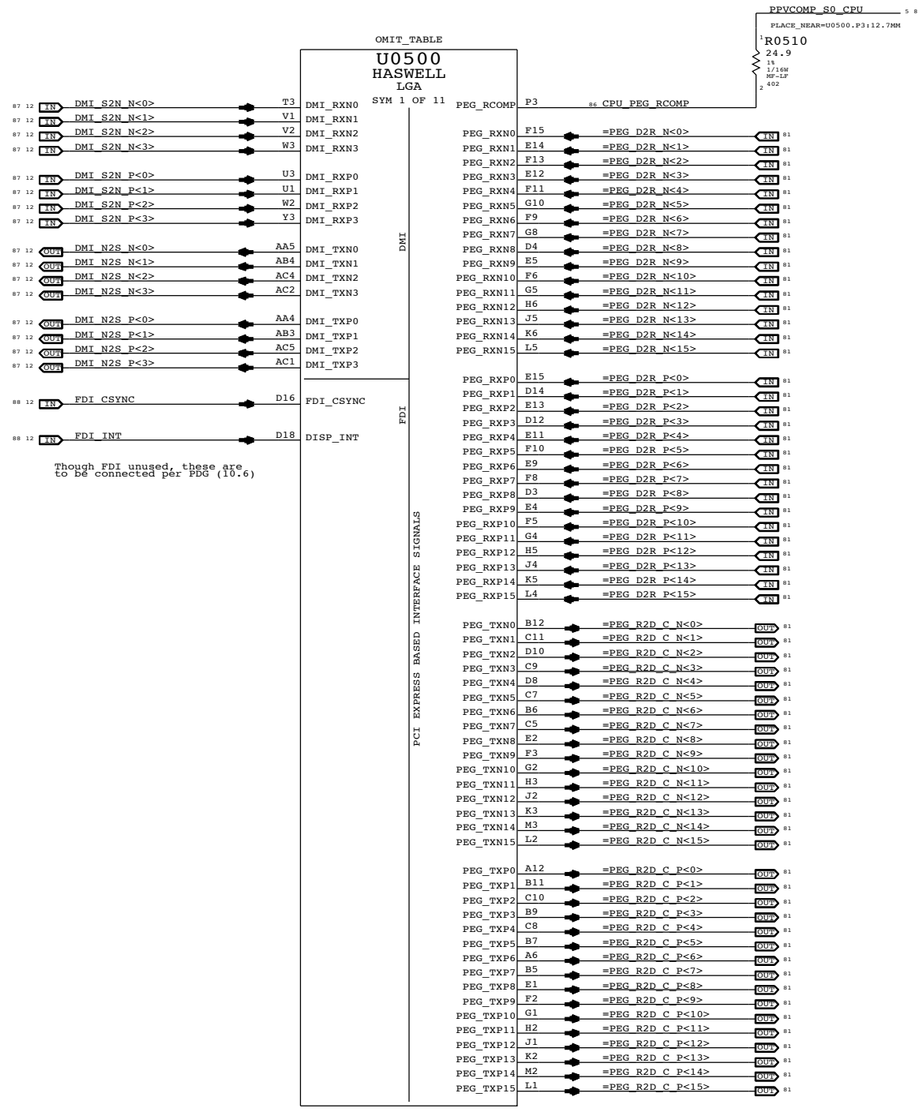

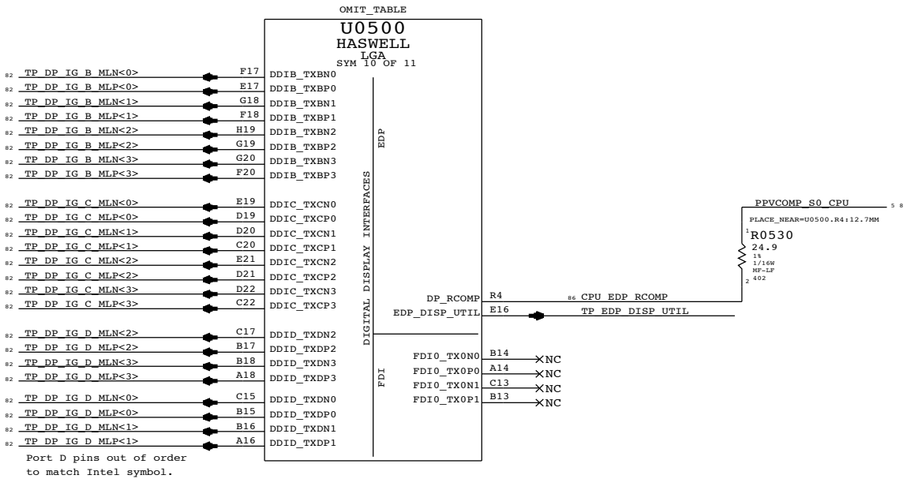

SYNC MASTER=J17 SYNC DATE=04/21/2013

PAGE TITLE

CPU DMI/PEG/FDI/RSVD

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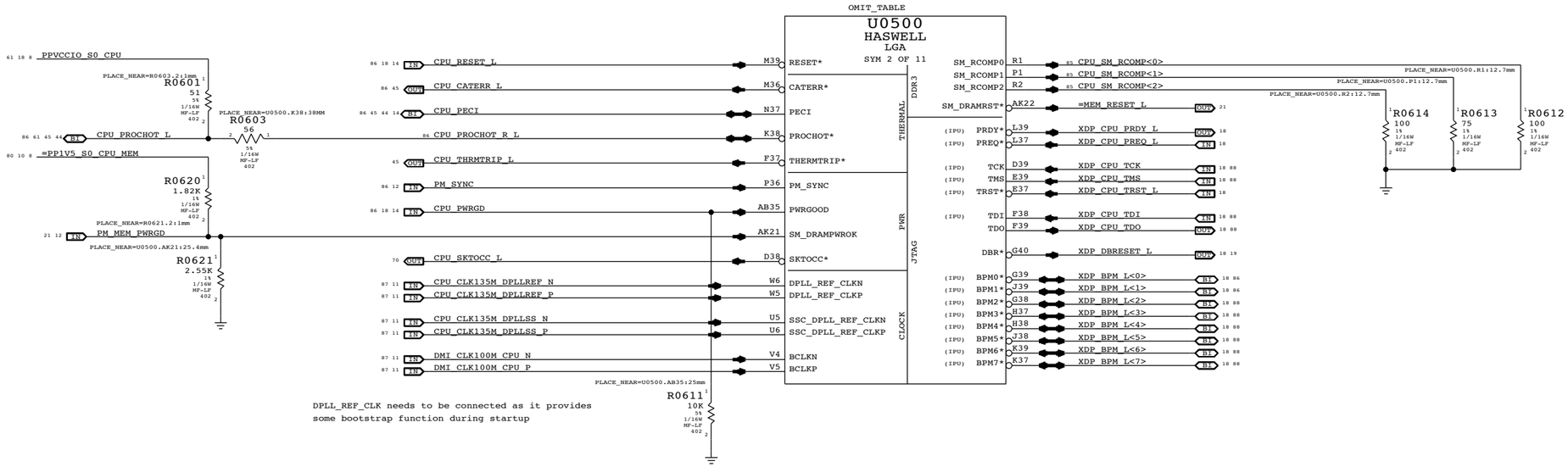

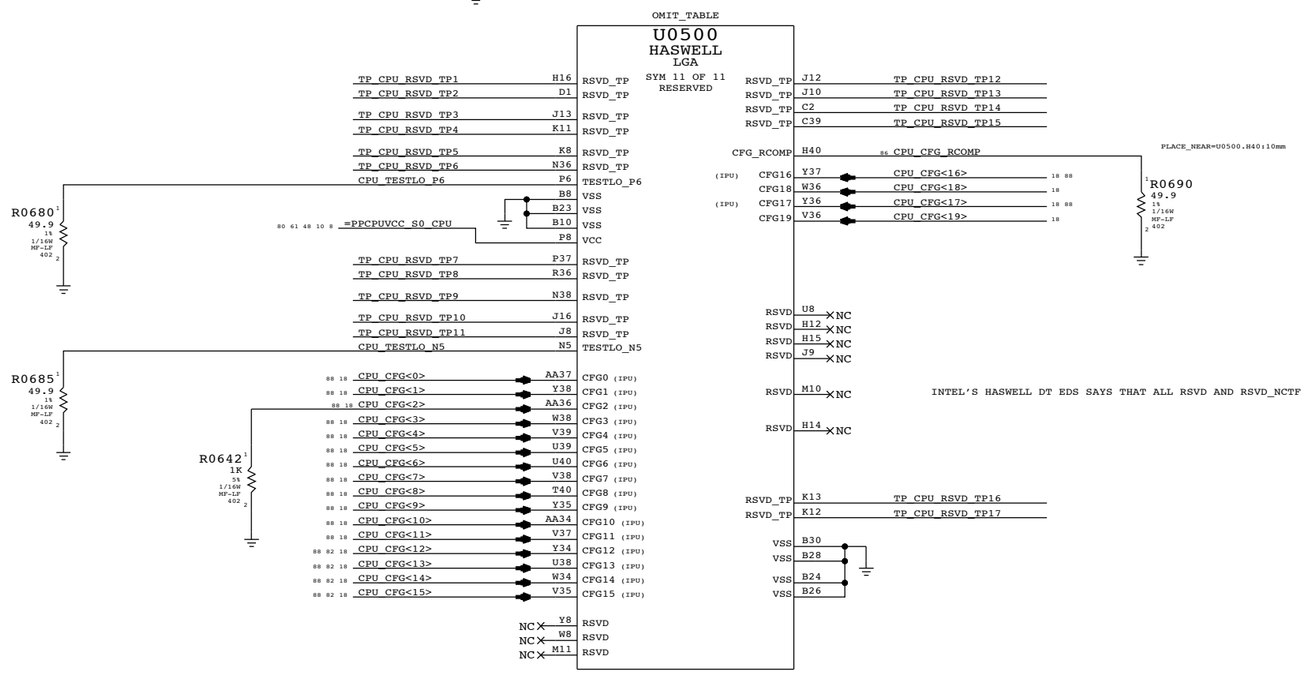


```
CFG [7] :PEG DEFER TRAINING              1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB   0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION              11 = 1 X16 (default)   10 = 2 X8    01 = RSVD    00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE              1 = DISABLED(default)   0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL           1 = NORMAL OPERATION(default)   0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL          1 = NORMAL OPERATION(default)   0 = LANES REVERSED
```

SYNC MASTER=J17 SYNC DATE=04/21/2013

PAGE TITLE

CPU Clock/Misc/JTAG/CFG

Apple Inc.

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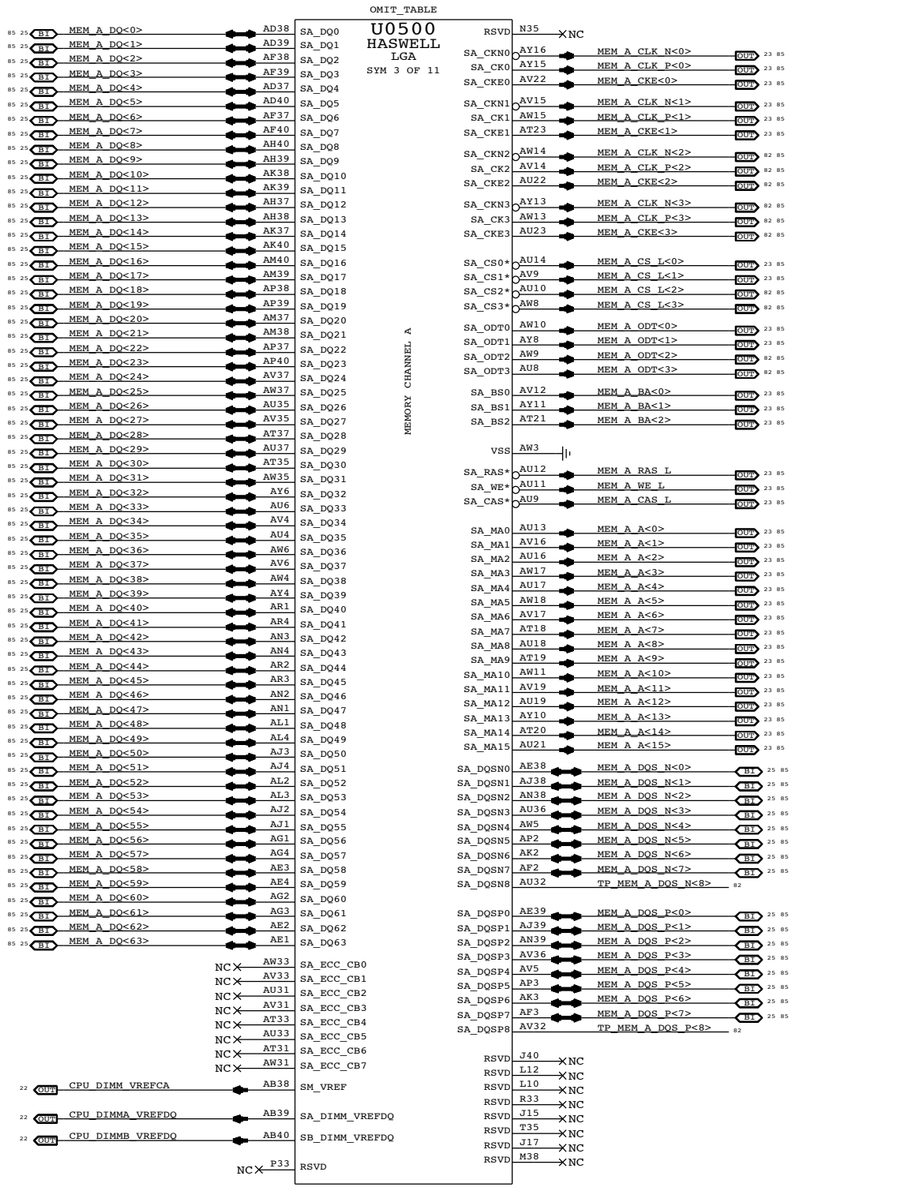

INTEL'S HASWELL DT EDS SAYS THAT ALL RSVD AND RSVD_NCTF SHOULD BE NC'D

SYNC_MASTER=J17 SYNC_DATE=04/21/2013

PAGE TITLE

CPU DDR3 Interfaces

Apple Inc.

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NOTE: Aliases not used on CPU supply outputs
to avoid any extraneous connections.

61 18 6 PPVCCIO_S0_CPU
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
Max load: 300mA

R0801 75 1% 1/16W MF-LF 402
R0802 43 5% 1/16W MF-LF 402
R0803 0 5% 1/16W MF-LF 402
R0804 110 1% 1/16W MF-LF 402
R0805 0 5% 1/16W MF-LF 402
Max load: 300mA

93 61 IN CPU_VIDALERT_L
93 61 OUT CPU_VIDSCLK
93 61 IN CPU_VIDSOUT

R0804.2: PLACE_NEAR=U0500.C37:12.7mm
R0802.2: PLACE_NEAR=U0500.B37:12.7mm
R0801.2: PLACE_NEAR=R0802.1:25.4mm

80 10 6 =PP1V5_S0_CPU_MEM

80 61 48 10 8 6 =PPCPUVCC_S0_CPU

R0800 100 5% 1/16W MF-LF 402
PLACE_NEAR=U0500.E40:50.8mm
PLACE_SIDE=BOTTOM

93 61 OUT CPU_VCCSENSE_P

5 PPVCOMP_S0_CPU
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V

93 CPU_VIDALERT_R_L
93 CPU_VIDSCLK_R
93 CPU_VIDSOUT_R

18 IN CPU_PWR_DEBUG

OMIT_TABLE

U0500
HASWELL
LGA
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NC	AW12	RSVD
NC	AW23	RSVD
NC	AW24	RSVD
NC	AW27	RSVD
	AJ12	VDDQ
	AJ13	
	AJ15	
	AJ17	
	AJ20	
	AJ21	
	AJ24	
	AJ25	
	AJ28	
	AJ29	
	AJ9	
	AT17	
	AT22	
	AU15	
	AU20	
	AU24	
	AV10	
	AV11	
	AV13	
	AV18	
	AV23	
	AV8	
	AW16	
	AY12	
	AY14	
	AY9	
NC	AU39	RSVD
	L22	VCC
	L23	VCC
NC	AU27	RSVD
NC	AU1	RSVD
	E40	VCC_SENSE
NC	AK20	RSVD
	L40	VCCIO_OUT
NC	AV24	RSVD
	P4	VCOMP_OUT
NC	AV2	RSVD
NC	AY18	RSVD
NC	AV29	RSVD
NC	AV20	RSVD
	B37	VIDALERT*
	C38	VIDSCLK
	C37	VIDSOUT
	AY5	VSS
	N40	PWR_DEBUG
	AY7	VSS
NC	AW2	RSVD
NC	AV1	RSVD
NC	A4	RSVD
NC	B3	RSVD
	B4	VSS
	AY26	VSS
	AW34	VSS
	AW32	VSS
	AY17	VSS
	AW36	VSS
	AY27	VSS
	AW26	VSS
	AY30	VSS
	AW30	VSS
	AY23	VSS
	A29	VCC
	A30	
	B25	
	B27	
	B29	
	B31	
	B33	
	B35	
	C26	
	C27	
	C24	
	C25	

=PPCPUVCC_S0_CPU 6 8 10 48 61 80

	C28	VCC
	C29	
	C30	
	C31	
	C32	
	C33	
	C34	
	C35	
	D25	
	D27	
	D29	
	D31	
	D33	
	D35	
	E24	
	E25	
	E26	
	E27	
	E28	
	E29	
	E30	
	E31	
	E32	
	E33	
	E34	
	E35	
	F23	
	F25	
	F27	
	F29	
	F31	
	F33	
	F35	
	G22	
	G23	
	G24	
	G25	
	G26	
	G27	
	G28	
	G29	
	G30	
	G31	
	G32	
	G33	
	G34	
	G35	
	H23	
	H25	
	H27	
	H29	
	H31	
	H33	
	H35	
	J21	
	J22	
	J23	
	J24	
	J25	
	J26	
	J27	
	J28	
	J29	
	J30	
	J31	
	J32	
	J33	
	J34	
	J35	
	K19	
	K21	
	K23	
	K25	
	K27	
	K29	
	K31	
	K33	
	K35	
	L15	
	L16	
	L17	
	L18	
	L19	
	L20	
	L21	
FC_Y7	Y7	TP_CPU_VCCST_PWRGD
FC_K9	K9	TP_CPU_VCCST

Y7,K9 FOR FUTURE CPU COMPATIBILITY
NC FOR NOW BUT NEEDED FOR 2014 CPUS

80 61 48 10 8 6 =PPCPUVCC_S0_CPU

OMIT_TABLE

U0500
HASWELL
LGA
SYM 6 OF 11
POWER

	M33	VCC
	M29	
	M27	
	M25	
	M23	
	M21	
	M19	
	M17	
	M15	
	M13	
	M8	
	L34	
	L33	
	L32	
	L31	
	L30	
	L29	
	L28	
	L27	
	L26	
	L25	
	L24	
	A28	
	A27	
	A26	
	A25	
	A24	

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PAGE TITLE
CPU Power

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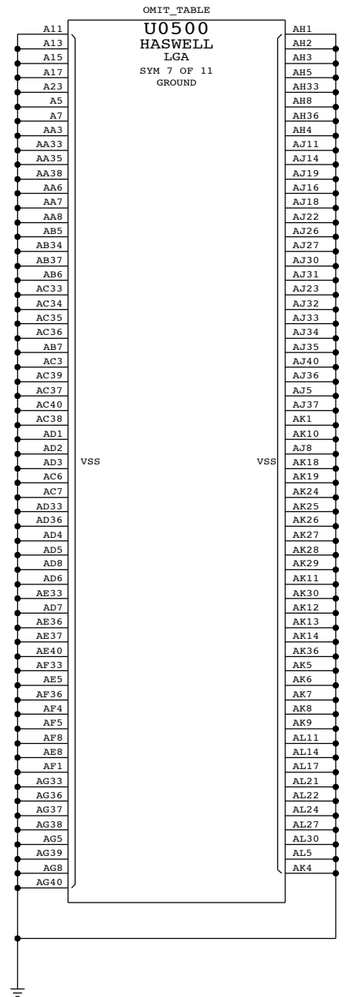

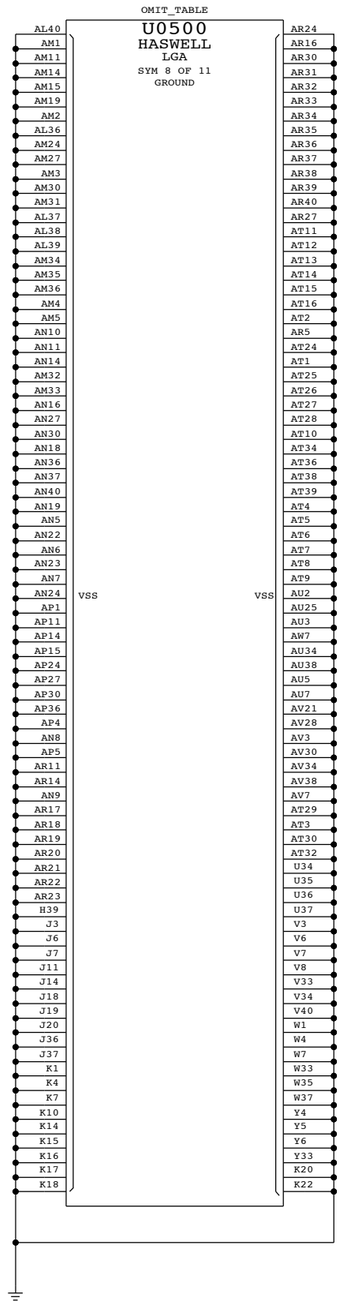

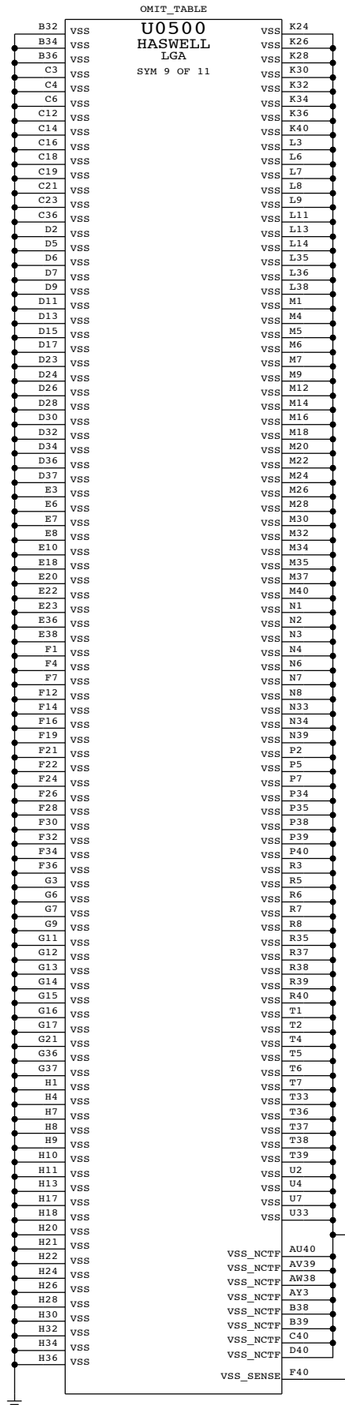

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CPU Ground

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CPU VCORE DECOUPLING

Intel Recommendation:22x 22UF 0805,topside (18 inside cavity, 4 north of processor),8x 470uF bulk caps(5 stuffed,3 no-stuffed)
Apple Implementation:28x 22UF 0603 per Harold
18x 10UF 0603 placed inside socket cavity

Layout Note: These caps should be placed symmetrically on Top and Bottom sides.
BULK CAPS ON CPU VREG PAGE 71

80 61 48 8 6 =PPCPUVCC_S0_CPU

CRITICAL C1000 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1001 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1002 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1003 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1004 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1005 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1006 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1007 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1008 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1009 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1010 22UF 20% 6.3V X5R-CERM2 0603

CRITICAL C1011 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1012 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1013 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1014 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1015 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1016 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1017 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1018 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1019 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1020 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1021 22UF 20% 6.3V X5R-CERM2 0603

CRITICAL C1022 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1023 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1024 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1025 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1026 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1027 22UF 20% 6.3V X5R-CERM2 0603

ADDED CRITICAL PROPERTY TO CPU CORE DECOUPLING
DUE TO ACOUSTICS CONCERNS

CRITICAL C1030 10UF 20% 6.3V X5R 603
CRITICAL C1031 10UF 20% 6.3V X5R 603
CRITICAL C1032 10UF 20% 6.3V X5R 603
CRITICAL C1033 10UF 20% 6.3V X5R 603
CRITICAL C1034 10UF 20% 6.3V X5R 603
CRITICAL C1035 10UF 20% 6.3V X5R 603
CRITICAL C1036 10UF 20% 6.3V X5R 603
CRITICAL C1037 10UF 20% 6.3V X5R 603
CRITICAL C1038 10UF 20% 6.3V X5R 603

CRITICAL C1039 10UF 20% 6.3V X5R 603
CRITICAL C1040 10UF 20% 6.3V X5R 603
CRITICAL C1041 10UF 20% 6.3V X5R 603
CRITICAL C1042 10UF 20% 6.3V X5R 603
CRITICAL C1043 10UF 20% 6.3V X5R 603
CRITICAL C1044 10UF 20% 6.3V X5R 603
CRITICAL C1045 10UF 20% 6.3V X5R 603
CRITICAL C1046 10UF 20% 6.3V X5R 603
CRITICAL C1047 10UF 20% 6.3V X5R 603

Memory (CPU VCCDDR) DECOUPLING

Intel Recommendation:9x 22UF 0805 near CPU power pins
Apple Implementation:9x 22UF 0603 per Harold

Layout Note: These caps should be placed symmetrically on Top and Bottom sides.

80 8 6 =PP1V5_S0_CPU_MEM

C1050 22UF 20% 6.3V X5R-CERM2 0603
C1051 22UF 20% 6.3V X5R-CERM2 0603
C1052 22UF 20% 6.3V X5R-CERM2 0603
C1053 22UF 20% 6.3V X5R-CERM2 0603
C1054 22UF 20% 6.3V X5R-CERM2 0603
C1055 22UF 20% 6.3V X5R-CERM2 0603
C1056 22UF 20% 6.3V X5R-CERM2 0603
C1057 22UF 20% 6.3V X5R-CERM2 0603
C1058 22UF 20% 6.3V X5R-CERM2 0603

NOSTUFF C1060 22UF 20% 6.3V X5R-CERM2 0603
NOSTUFF C1061 22UF 20% 6.3V X5R-CERM2 0603
NOSTUFF C1062 22UF 20% 6.3V X5R-CERM2 0603

NOSTUFF CRITICAL C1059 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

SYNC MASTER=J17 SYNC DATE=04/21/2013

PAGE TITLE: CPU DECOUPLING

Apple Inc.

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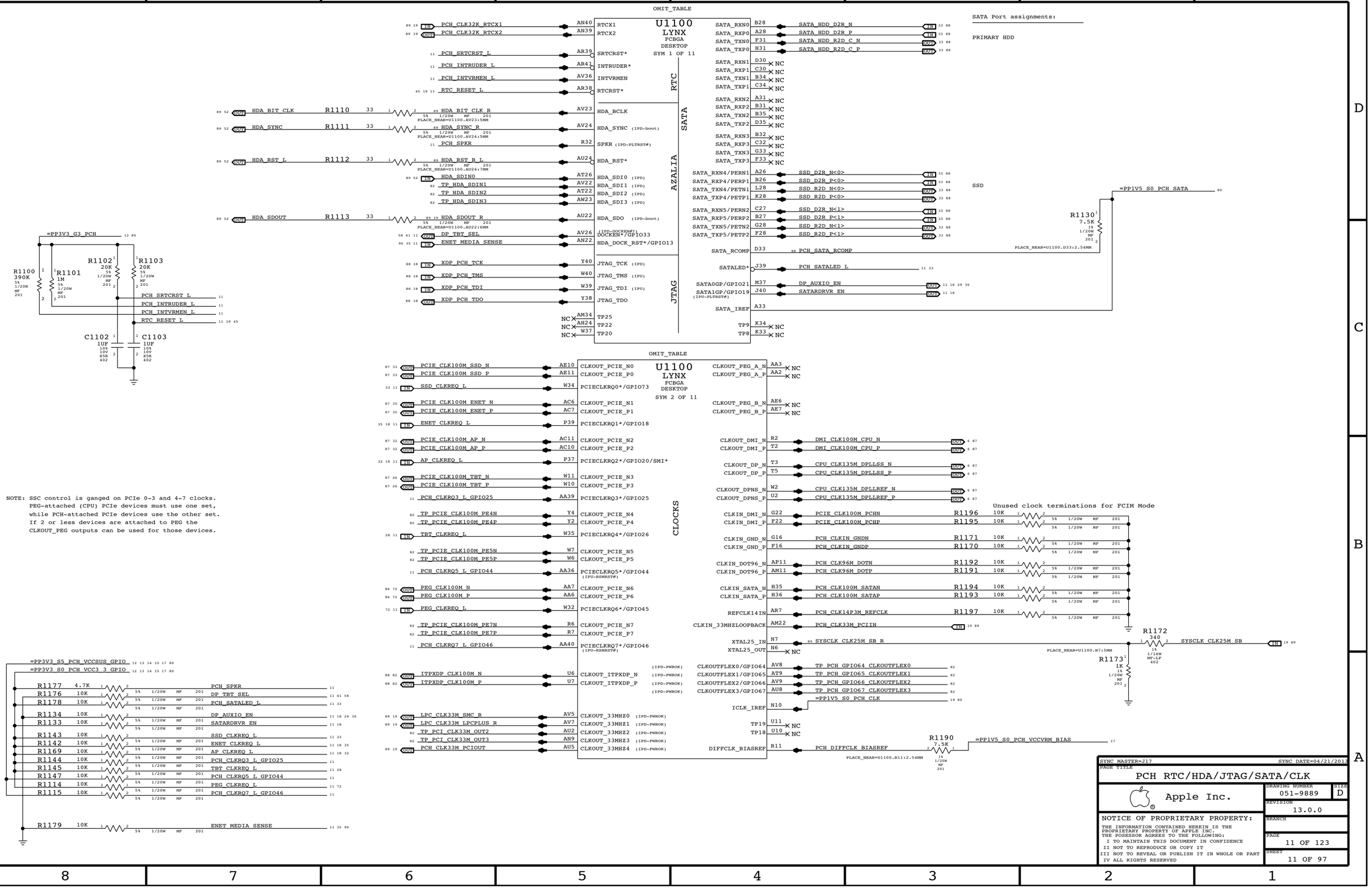
OMIT_TABLE
U1100
LYNX
FCBGA
DESKTOP
SYM 1 OF 11
RTC
SATA
AZALIA
JTAG
PCH_CLK32K_RTCX1
PCH_CLK32K_RTCX2
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
RTC_RESET_L
HDA_BIT_CLK
HDA_SYNC
PCH_SPKR
HDA_RST_L
HDA_SDIN0
TP_HDA_SDIN1
TP_HDA_SDIN2
TP_HDA_SDIN3
HDA_SDOUT
DP_TBT_SEL
ENET_MEDIA_SENSE
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
SATA_RXN1
SATA_RXP1
SATA_TXN1
SATA_TXP1
SATA_RXN2
SATA_RXP2
SATA_TXN2
SATA_TXP2
SATA_RXN3
SATA_RXP3
SATA_TXN3
SATA_TXP3
SATA_RXN4/PERN1
SATA_RXP4/PERP1
SATA_TXN4/PETN1
SATA_TXP4/PETP1
SATA_RXN5/PERN2
SATA_RXP5/PERP2
SATA_TXN5/PETN2
SATA_TXP5/PETP2
SATA_RCOMP
SATALED*
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA_IREF
TP9
TP8
SATA Port assignments:
PRIMARY HDD
SSD
=PP1V5_S0_PCH_SATA
R1130 7.5K
PLACE_NEAR=U1100.D33:2.54MM
=PP3V3_G3_PCH
R1100 390K
R1101 1M
R1102 20K
R1103 20K
C1102 1UF
C1103 1UF
OMIT_TABLE
U1100
LYNX
FCBGA
DESKTOP
SYM 2 OF 11
CLOCKS
PCIE_CLK100M_SSD_N
PCIE_CLK100M_SSD_P
SSD_CLKREQ_L
PCIE_CLK100M_ENET_N
PCIE_CLK100M_ENET_P
ENET_CLKREQ_L
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
AP_CLKREQ_L
PCIE_CLK100M_TBT_N
PCIE_CLK100M_TBT_P
PCH_CLKRQ3_L_GPIO25
TP_PCIE_CLK100M_PE4N
TP_PCIE_CLK100M_PE4P
TBT_CLKREQ_L
TP_PCIE_CLK100M_PE5N
TP_PCIE_CLK100M_PE5P
PCH_CLKRQ5_L_GPIO44
PEG_CLK100M_N
PEG_CLK100M_P
PEG_CLKREQ_L
TP_PCIE_CLK100M_PE7N
TP_PCIE_CLK100M_PE7P
PCH_CLKRQ7_L_GPIO46
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
LPC_CLK33M_SMC_R
LPC_CLK33M_LPCPLUS_R
TP_PCI_CLK33M_OUT2
TP_PCI_CLK33M_OUT3
PCH_CLK33M_PCIOUT
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
CLKOUT_PCIE_N6
CLKOUT_PCIE_P6
CLKOUT_PCIE_N7
CLKOUT_PCIE_P7
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKOUT_33MHZ0
CLKOUT_33MHZ1
CLKOUT_33MHZ2
CLKOUT_33MHZ3
CLKOUT_33MHZ4
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKOUT_DPNS_N
CLKOUT_DPNS_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_GND_N
CLKIN_GND_P
CLKIN_DOT96_N
CLKIN_DOT96_P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_33MHZLOOPBACK
XTAL25_IN
XTAL25_OUT
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
ICLK_IREF
TP19
TP18
DIFFCLK_BIASREF
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
CPU_CLK135M_DPLLSS_N
CPU_CLK135M_DPLLSS_P
CPU_CLK135M_DPLLREF_N
CPU_CLK135M_DPLLREF_P
PCIE_CLK100M_PCHN
PCIE_CLK100M_PCHP
PCH_CLKIN_GNDN
PCH_CLKIN_GNDP
PCH_CLK96M_DOTN
PCH_CLK96M_DOTP
PCH_CLK100M_SATAN
PCH_CLK100M_SATAP
PCH_CLK14P3M_REFCLK
PCH_CLK33M_PCIIN
SYSCLK_CLK25M_SB_R
TP_PCH_GPIO64_CLKOUTFLEX0
TP_PCH_GPIO65_CLKOUTFLEX1
TP_PCH_GPIO66_CLKOUTFLEX2
TP_PCH_GPIO67_CLKOUTFLEX3
=PP1V5_S0_PCH_CLK
PCH_DIFFCLK_BIASREF
R1190 7.5K
PLACE_NEAR=U1100.R11:2.54MM
=PP1V5_S0_PCH_VCCVRM_BIAS
Unused clock terminations for FCIM Mode
R1196 10K
R1195 10K
R1171 10K
R1170 10K
R1192 10K
R1191 10K
R1194 10K
R1193 10K
R1197 10K
R1172 340
R1173 1K
SYSCLK_CLK25M_SB
PLACE_NEAR=U1100.N7:5MM
NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks.
PEG-attached (CPU) PCIe devices must use one set,
while PCH-attached PCIe devices use the other set.
If 2 or less devices are attached to PEG the
CLKOUT_PEG outputs can be used for those devices.
=PP3V3_S5_PCH_VCCSUS_GPIO
=PP3V3_S0_PCH_VCC3_3_GPIO
R1177 4.7K
R1176 10K
R1178 10K
R1134 10K
R1133 10K
R1143 10K
R1142 10K
R1169 10K
R1144 10K
R1145 10K
R1147 10K
R1114 10K
R1115 10K
R1179 10K
PCH_SPKR
DP_TBT_SEL
PCH_SATALED_L
DP_AUXIO_EN
SATARDRVR_EN
SSD_CLKREQ_L
ENET_CLKREQ_L
AP_CLKREQ_L
PCH_CLKRQ3_L_GPIO25
TBT_CLKREQ_L
PCH_CLKRQ5_L_GPIO44
PEG_CLKREQ_L
PCH_CLKRQ7_L_GPIO46
ENET_MEDIA_SENSE
SYNC MASTER=J17
SYNC DATE=04/21/2013
PAGE TITLE
PCH RTC/HDA/JTAG/SATA/CLK
Apple Inc.
DRAWING NUMBER
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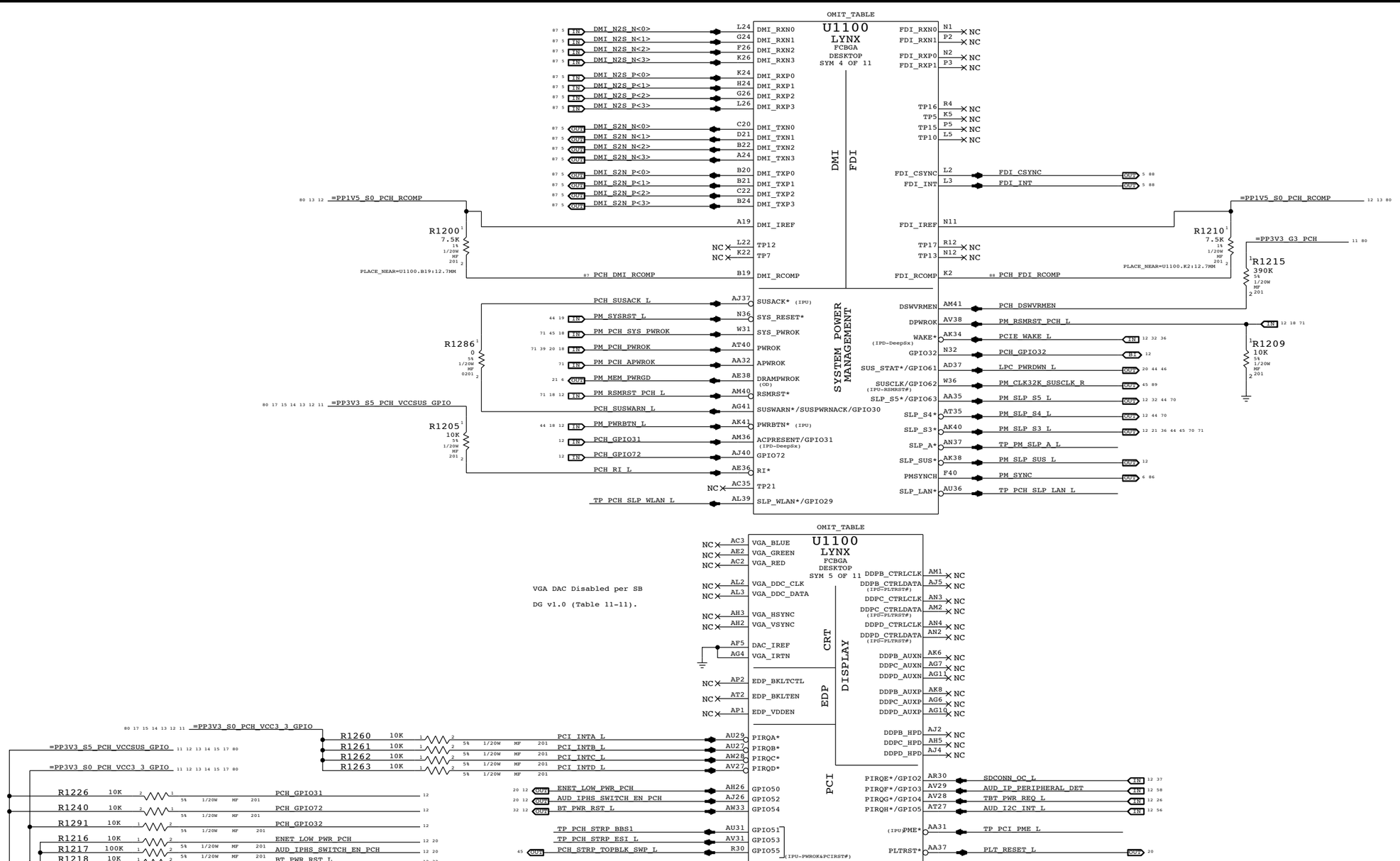

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PCH DMI/FDI/PM/GFX/PCI

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U1100
LYNX
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DESKTOP
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PCI-E

NC	L14	PERN1_USB3RN3
NC	K14	PERP1_USB3RP3
NC	B12	PETN1_USB3TN3
NC	B11	PETP1_USB3TP3
NC	F14	PERN2_USB3RN4
NC	G14	PERP2_USB3RP4
NC	D11	PETN2_USB3TN4
NC	C11	PETP2_USB3TP4

AirPort

87 32 IN	PCIE_AP_D2R_N	F11	PERN3
87 32 IN	PCIE_AP_D2R_P	H11	PERP3
87 32 OUT	PCIE_AP_R2D_C_N	B9	PETN3
87 32 OUT	PCIE_AP_R2D_C_P	A9	PETP3

ENET

87 35 IN	PCIE_ENET_D2R_N	J11	PERN4
87 35 IN	PCIE_ENET_D2R_P	L11	PERP4
87 35 OUT	PCIE_ENET_R2D_C_N	B8	PETN4
87 35 OUT	PCIE_ENET_R2D_C_P	C8	PETP4

TBT

87 26 IN	PCIE_TBT_D2R_N<0>	G9	PERN5
87 26 IN	PCIE_TBT_D2R_P<0>	F9	PERP5
87 26 OUT	PCIE_TBT_R2D_C_N<0>	B7	PETN5
87 26 OUT	PCIE_TBT_R2D_C_P<0>	A7	PETP5
87 26 IN	PCIE_TBT_D2R_N<1>	F7	PERN6
87 26 IN	PCIE_TBT_D2R_P<1>	H7	PERP6
87 26 OUT	PCIE_TBT_R2D_C_N<1>	E1	PETN6
87 26 OUT	PCIE_TBT_R2D_C_P<1>	D2	PETP6
87 26 IN	PCIE_TBT_D2R_N<2>	K6	PERN7
87 26 IN	PCIE_TBT_D2R_P<2>	K8	PERP7
87 26 OUT	PCIE_TBT_R2D_C_N<2>	G3	PETN7
87 26 OUT	PCIE_TBT_R2D_C_P<2>	G5	PETP7
87 26 IN	PCIE_TBT_D2R_N<3>	J2	PERN8
87 26 IN	PCIE_TBT_D2R_P<3>	J3	PERP8
87 26 OUT	PCIE_TBT_R2D_C_N<3>	H2	PETN8
87 26 OUT	PCIE_TBT_R2D_C_P<3>	H1	PETP8

80 12 =PP1V5_S0_PCH_RCOMP

R1300 7.5K 1% 1/20W MF 201 — PLACE_NEAR=U1100.C13:12.7MM

	B13	PCIE_IREF
NC	L16	TP11
NC	K16	TP6
87 PCH_PCIE_RCOMP	C13	PCIE_RCOMP

USB

USB2N0	AV10	USB_EXTA_0_N	42 90 BI
USB2P0	AU10	USB_EXTA_0_P	42 90 BI
USB2N1	AV11	USB_EXTC_1_N	43 90 BI
USB2P1	AW11	USB_EXTC_1_P	43 90 BI
USB2N2	AN14	NC	
USB2P2	AP14	NC	
USB2N3	AJ16	NC	
USB2P3	AK16	NC	
USB2N4	AU15	NC	
USB2P4	AV15	NC	
USB2N5	AU12	NC	
USB2P5	AT12	NC	
USB2N6	AV14	NC	
USB2P6	AW14	NC	
USB2N7	AU17	NC	
USB2P7	AT17	NC	
USB2N8	AW16	USB_EXTB_8_N	42 90 BI
USB2P8	AV16	USB_EXTB_8_P	42 90 BI
USB2N9	AN16	USB_EXTD_9_N	43 90 BI
USB2P9	AP16	USB_EXTD_9_P	43 90 BI
USB2N10	AJ18	USB_CAMERA_N	38 90 BI
USB2P10	AK18	USB_CAMERA_P	38 90 BI
USB2N11	AP18	USB_BT_N	32 90 BI
USB2P11	AN18	USB_BT_P	32 90 BI
USB2N12	AW18	NC	
USB2P12	AV18	NC	
USB2N13	AP20	NC	
USB2P13 (IPD)	AN20	NC	

USB Port Assignments:

Ext A (LS/FS/HS)

Ext C (LS/FS/HS)

Ext B (LS/FS/HS)

Ext D (LS/FS/HS)

CAMERA

BT

USB3RN1	F20	USB3_EXTA_RX_F_N	42 90 IN
USB3RP1	G20	USB3_EXTA_RX_F_P	42 90 IN
USB3TN1	B18	USB3_EXTA_TX_N	42 90 OUT
USB3TP1	C18	USB3_EXTA_TX_P	42 90 OUT
USB3RN2	G18	USB3_EXTB_RX_F_N	42 90 IN
USB3RP2	H18	USB3_EXTB_RX_F_P	42 90 IN
USB3TN2	B15	USB3_EXTB_TX_N	42 90 OUT
USB3TP2	B16	USB3_EXTB_TX_P	42 90 OUT
USB3RN5	K20	USB3_EXTC_RX_F_N	43 90 IN
USB3RP5	L20	USB3_EXTC_RX_F_P	43 90 IN
USB3TN5	D15	USB3_EXTC_TX_N	43 90 OUT
USB3TP5	C15	USB3_EXTC_TX_P	43 90 OUT
USB3RN6	L18	USB3_EXTD_RX_F_N	43 90 IN
USB3RP6	K18	USB3_EXTD_RX_F_P	43 90 IN
USB3TN6	B14	USB3_EXTD_TX_N	43 90 OUT
USB3TP6	A14	USB3_EXTD_TX_P	43 90 OUT

USB3 Port Assignments:

Ext A (SS)

Ext B (SS)

Ext C (SS)

Ext D (SS)

90 PCH_USB_RBIAS

R1370 22.6 1% 1/20W MF 201 — PLACE_NEAR=U1100.AV20:11.4MM

USBRBIAS*	AV20	
USBRBIAS	AU20	
TP24	AK14	NC
TP23	AJ14	NC

OC0*/GPIO59	AE40	USB_EXTA_OC_L	13 18 42 IN
OC1*/GPIO40	AF37	USB_EXTC_OC_L	13 18 43 IN
OC2*/GPIO41	AD39	PCH_GPIO41	13 18 OUT
OC3*/GPIO42	AD40	PCH_GPIO42	13 18 OUT
OC4*/GPIO43	AF39	USB_EXTB_OC_L	13 18 42 IN
OC5*/GPIO9	AC41	USB_EXTD_OC_L	13 18 43 IN
OC6*/GPIO10	AF40	PCH_GPIO10	13 18 OUT
OC7*/GPIO14	AG40	SDCONN_STATE_CHANGE	13 18 37 IN

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LPC

89 46 44 BI	LPC_AD<0>	R1340 33 1% 1/20W MF 201	89 LPC_AD_R<0>
89 46 44 BI	LPC_AD<1>	R1341 33 1% 1/20W MF 201	89 LPC_AD_R<1>
89 46 44 BI	LPC_AD<2>	R1342 33 1% 1/20W MF 201	89 LPC_AD_R<2>
89 46 44 BI	LPC_AD<3>	R1343 33 1% 1/20W MF 201	89 LPC_AD_R<3>
89 46 44 OUT	LPC_FRAME_L	R1344 33 1% 1/20W MF 201	89 LPC_FRAME_R_L

	AN24	LAD0 (IPU)	
	AP26	LAD1 (IPU)	
	AJ24	LAD2 (IPU)	
	AN26	LAD3 (IPU)	
	AP24	LFRAME*	
82 TP_LPC_DREQ0_L	AK22	LDRQ0* (IPU)	
20 13 OUT TBT_PWR_EN_PCH	AK26	LDRQ1*/GPIO23 (IPU-LDRQ1#7)	
46 44 13 BI LPC_SERIRQ	G39	SERIRQ	

SMBUS

AG31	SMBALERT*/GPIO11	PCH_SMBALERT_L 13
AG36	SMBCLK	SMBUS_PCH_CLK OUT 47 91
AG32	SMBDATA	SMBUS_PCH_DATA BI 47 91
AG35	SML0ALERT*/GPIO60	PCH_SML0ALERT_L 13
AE32	SML0CLK	SML_PCH_0_CLK OUT 47 91
AE35	SML0DATA	SML_PCH_0_DATA BI 47 91
AJ39	SML1ALERT*/PCHHOT*/GPIO74	PCH_SML1ALERT_L 13
AK36	SML1CLK/GPIO58	SML_PCH_1_CLK IN 47 91
AK33	SML1DATA/GPIO75	SML_PCH_1_DATA BI 47 91

SPI

89 46 OUT SPI_CLK_R	U39	SPI_CLK
89 46 OUT SPI_CS0_R_L	R38	SPI_CS0* (IPU)
NC	R35	SPI_CS1* (IPU)
NC	R40	SPI_CS2* (IPU)
89 46 BI SPI_MOSI_R	P40	SPI_MOSI (IPD)
89 46 BI SPI_MISO	R36	SPI_MISO (IPU)
NC	U40	SPI_IO2 (IPU)
NC	U37	SPI_IO3 (IPU)

C-LINK

(IPU/IPD) CL_CLK	U36	TP_CLINK_CLK
(IPU/IPD) CL_DATA	U35	TP_CLINK_DATA
CL_RST*	U34	TP_CLINK_RESET_L

TP1	A2	NC
TP2	A3	NC
TP4	B2	NC
TP3	B1	NC
TD_IREF	C3	PCH_TD_IREF

PLACE_NEAR=U1100.C3:11.4MM

R1380 8.2K 1% 1/20W MF 201

=PP3V3_S5_PCH_VCCSUS_GPIO 11 12 14 15 17 80

=PP3V3_S4_PCH 80

=PP3V3_S0_PCH_VCC3_3_GPIO 11 12 14 15 17 80

R1350	10K 5% 1/20W MF 201	LPC_SERIRQ	13 44 46
R1351	10K 5% 1/20W MF 201	TBT_PWR_EN_PCH	13 20
R1360	10K 5% 1/20W MF 201	USB_EXTA_OC_L	13 18 42
R1361	10K 5% 1/20W MF 201	USB_EXTC_OC_L	13 18 43
R1362	10K 5% 1/20W MF 201	PCH_GPIO41	13 18
R1368	10K 5% 1/20W MF 201	PCH_GPIO42	13 18
R1320	10K 5% 1/20W MF 201	USB_EXTB_OC_L	13 18 42
R1321	10K 5% 1/20W MF 201	USB_EXTD_OC_L	13 18 43
R1367	10K 5% 1/20W MF 201	PCH_GPIO10	13 18
R1369	10K 5% 1/20W MF 201	SDCONN_STATE_CHANGE	13 18 37
R1353	10K 5% 1/20W MF 201	PCH_SMBALERT_L	13
R1354	10K 5% 1/20W MF 201	PCH_SML0ALERT_L	13
R1355	10K 5% 1/20W MF 201	PCH_SML1ALERT_L	13

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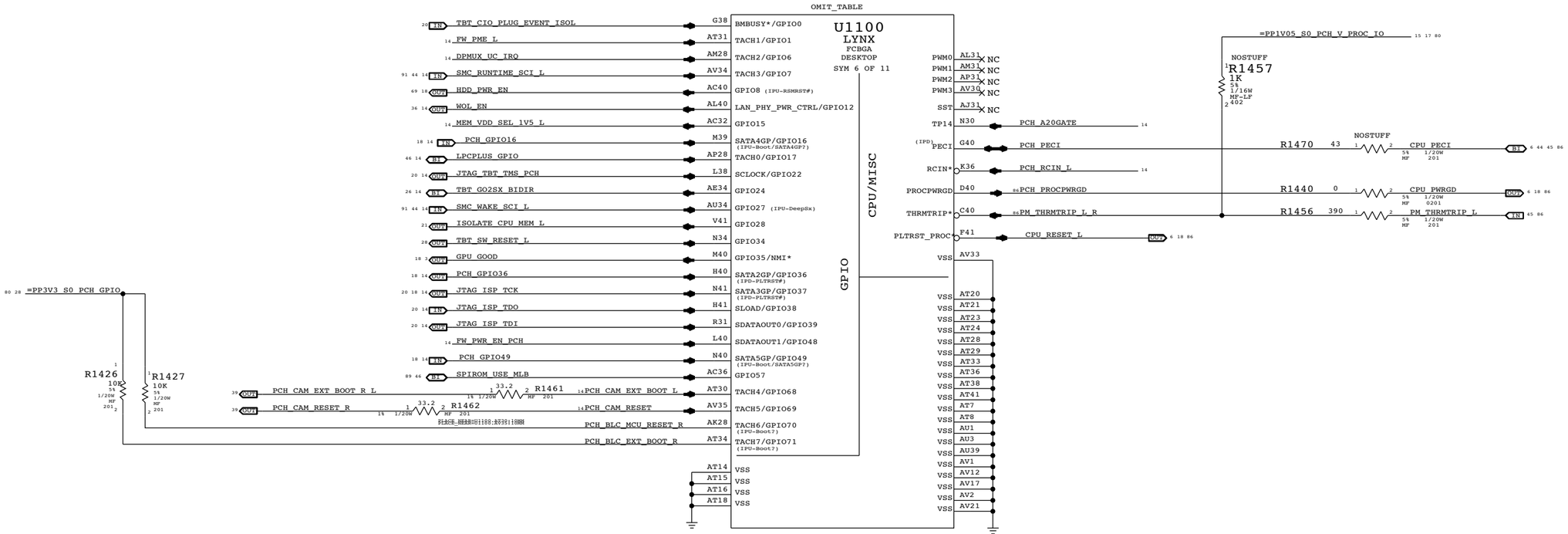

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80 17 =PP1V05_S0_PCH_VCC
VCC: 1312mA Max, 130mA Idle

V20 VCC
V22 VCC
V23 VCC
V25 VCC
W17 VCC
W19 VCC
W23 VCC
W25 VCC
AA19 VCC
AA20 VCC
17 =PP1V05_S0_PCH_VCC_CLK_F AB1 VCC
AB16 VCC
AB17 VCC
AB19 VCC
AB20 VCC
AD16 VCC

PLACE_NEAR=R1550.1:2.54mm
PPVOUT_S5_PCH_DCPSUSBYP
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V

C1550
1UF
10%
6.3V
CERM
402

R1550
5.11
1%
1/20W
MF-LF
201

PLACE_NEAR=U1100.AU40:2.54MM
PPVOUT_S5_PCH_DCPSUSBYP_R
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V

Powered in DeepSx

AU40 DCPSUSBYP
AU41 DCPSUSBYP
C1 VCCVRM
C2 VCCVRM
K1 VCCVRM
17 15 =PP1V5_S0_PCH_VCCVRM_CLK T14 VCCVRM
VCCVRM: 158mA Max, 43mA Idle

80 17 15 =PP1V05_S0_PCH_VCCASW AF25 VCCASW
VCCASW: 670mA Max, 34mA Idle
AA25 VCCASW
AA26 VCCASW
AB22 VCCASW
AB23 VCCASW
AB25 VCCASW
AB26 VCCASW
AD17 VCCASW
AD19 VCCASW
AD20 VCCASW
AD22 VCCASW
AD23 VCCASW
AD25 VCCASW

CORE
CRT
FDI
HVCMOS
USB3
PCIE/DMI
SATA
VCCMPHY

VCCADAC1_5 AF2 CKPLUS_WAIVE=PWRTERM2GND
VSS AV40 VGA DAC Disabled per LPT DG v1.0 (Table 12-18).
VCCADACBG3_3 AE1 CKPLUS_WAIVE=PWRTERM2GND

VCCVRM B39 =PP1V5_S0_PCH_VCCVRM_FDI 17
VCCVRM: 158mA Max, 43mA Idle
VCCIO AC12 =PP1V05_S0_PCH_VCCIO 15 17 80
VCCIO: 3491mA Max, 199mA Idle
VCCIO AF19 =PP1V05_S0_PCH_VCCIO_USB2 15 17 80

VCC3_3 AG1 =PP3V3_S0_PCH_VCC3_3_HVCMOS 17 80
VCC3_3: 133mA Max, 3mA Idle

DCPSUS1 AE30 NC
VCCSUS3_3 AN33 =PP3V3_S5_PCH_VCCSUS_GPIO 11 12 13 14 15 17 80
VCCSUS3_3: 261mA Max, 6mA Idle
VCCSUS3_3 P20 =PP3V3_S5_PCH_VCCSUS_USB3 80
DCPSUS3 P19 NC

VCCIO P25 =PP1V05_S0_PCH_VCCIO 15 17 80
VCCIO: 3491mA Max, 199mA Idle
VCCVRM A39 =PP1V5_S0_PCH_VCCVRM_USB3 17
VCCVRM: 158mA Max, 43mA Idle
VCCVRM A4

VCCVRM B4 =PP1V5_S0_PCH_VCCVRM_PCIE 17
VCCVRM: 158mA Max, 43mA Idle
VCCIO P23

VCCVRM A40 =PP1V5_S0_PCH_VCCVRM_SATA 17
VCCVRM: 158mA Max, 43mA Idle
VCCIO P26

VCCIO P28
VCCIO T19
VCCIO T20
VCCIO AF20 =PP1V05_S0_PCH_VCCIO_USB2 15 17 80
VCCIO AF22
VCCIO AF23

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80 17 15 =PP3V3_S5_PCH_VCCSUS_USB AH22 VCCSUS3_3
VCCSUS3_3: 261mA Max, 6mA Idle
AJ20 VCCSUS3_3
AK20 VCCSUS3_3
80 17 15 14 13 12 11 =PP3V3_S5_PCH_VCCSUS_GPIO AM33 VCCSUS3_3

AV41 VSS

80 17 =PP1V05_S0_PCH_VCCUSBPLL AP22 VCCUSBPLL

80 17 =PP1V05_S0_PCH_VCCIO_FDI M14 VCCIO
80 17 15 =PP1V05_S0_PCH_VCCIO P16 VCCIO
VCCIO: 3491mA Max, 199mA Idle
P17 VCCIO
P22 VCCIO

NC AJ22 DCPSUS2

17 16 =PP1V5_S0_PCH_VCCVRM_CLK A38 VCCVRM
VCCVRM: 158mA Max, 43mA Idle

80 17 =PP1V05_S0_PCH_VCCCLK_SSC T16 VCCCLK
VCCCLK: 306mA Max, 89mA Idle
80 17 =PP3V3_S0_PCH_VCCCLK3_3 AM9 VCCCLK3_3
VCCCLK3_3: 55mA Max, 11mA Idle
AK11 VCCCLK3_3
AG12 VCCCLK3_3
AM7 VCCCLK3_3
AP5 VCCCLK3_3
AP7 VCCCLK3_3
AW3 VCCCLK3_3
AW4 VCCCLK3_3
AW9 VCCCLK3_3
AR4 VCCCLK3_3
AT5 VCCCLK3_3
AV3 VCCCLK3_3
AV4 VCCCLK3_3

V16 VCCCLK
80 17 =PP1V05_S0_PCH_VCCCLK_CLK100 U12 VCCCLK
VCCCLK: 306mA Max, 89mA Idle
V14 VCCCLK
80 17 =PP1V05_S0_PCH_VCCCLK_CLK135 W14 VCCCLK
VCCCLK: 306mA Max, 89mA Idle
W16 VCCCLK
80 17 =PP1V05_S0_PCH_VCCCLK_SSC100 AA16 VCCCLK
VCCCLK: 306mA Max, 89mA Idle
AB2 VCCCLK

CLK/MISC
USB
GPIO/LPC
HDA
RTC
CPU
SPI
THERMAL

VCCSUS3_3 AH18 =PP3V3_S5_PCH_VCCSUS_USB 15 17 80
VCCSUS3_3: 261mA Max, 6mA Idle
VCCSUS3_3 AH20
VCCDSW3_3 AV39 =PP3V3_S5_PCH_VCCDSW 17 80
VCCDSW3_3: 15mA Max, 1mA Idle
VCCDSW3_3 AW38
VCCDSW3_3 AW39

DCPSST AH28 PPVOUT_S0_PCH_DCPSST BYPASS=U1100.AH28:6.35MM
MIN_LINE_WIDTH=0.2 mm VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 mm
C1580 0.1UF 20% 10V CERM 402

VCC3_3 AF26 =PP3V3_S0_PCH_VCC_FUSE 17 80
VCC3_3 U30 =PP3V3_S0_PCH_VCC3_3_GPIO 11 12 13 14 15 17 80
VCC3_3 AW21 =PP3V3_S0_PCH_VCC3_3_USB 17 80
VCC3_3 W30 =PP3V3_S0_PCH_VCC3_3_GPIO 11 12 13 14 15 17 80
VCCIO P14 =PP1V05_S0_PCH_VCCIO 15 17 80
VCCIO: 3491mA Max, 199mA Idle

VCCSUSHDA AW26 =PP3V3_S5_PCH_VCCSUS_HDA 17 80
VCCSUSHDA: 10mA Max, 1mA Idle

VCCSUS3_3 AP35 =PP3V3_S5_PCH_VCCSUS_RTC 17 80
VCCRTC AP33 =PP3V3_G3_PCH_RTC 80
6uA Max (3.0V, room temperature)
DCPRTC AW35 PPVOUT_S0_PCH_DCPRTC BYPASS=U1100.AW35:6.35MM
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
C1590 0.1UF 20% 10V CERM 402

C1533 0.1UF 20% 10V CERM 402
C1532 0.1UF 20% 10V CERM 402
C1531 1UF 10% 6.3V CERM 402
BYPASS=U1100.AP33:6.35MM
BYPASS=U1100.AP33:6.35MM
BYPASS=U1100.AP33:6.35MM

V_PROC_IO C39 =PP1V05_S0_PCH_V_PROC_IO 14 17 80
V_PROC_IO: 4mA Max, 2mA Idle

VCCSPI R41 =PP3V3_S5_PCH_VCC_SPI 17 80
VCCSPI: 22mA Max, 1mA Idle

VCC V17 =PP1V05_S0_PCH_VCCIO 15 17 80
VCC V19
VCCASW W26 =PP1V05_S0_PCH_VCCASW 15 17 80
VCCASW: 670mA Max, 34mA Idle
VCCASW AA23 =PP1V05_S0_PCH_VCCASW 15 17 80
VCCASW: 670mA Max, 34mA Idle

VCCVRM B37 =PP1V5_S0_PCH_VCCVRM_THRM 17
VCCVRM: 158mA Max, 43mA Idle
VCC3_3 B6 =PP3V3_S0_PCH_VCC3_3_THRM 17 80
VCC3_3: 133mA Max, 3mA Idle

Current data from LPT EDS (doc #486708, Rev 1.0).

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A12	VSS	VSS	F18
A16	VSS	VSS	F24
A21	VSS	VSS	F35
A35	VSS	VSS	F37
B25	VSS	VSS	F38
B3	VSS	VSS	G2
B30	VSS	VSS	H14
B33	VSS	VSS	H16
B38	VSS	VSS	H20
B40	VSS	VSS	H22
B41	VSS	VSS	H26
C25	VSS	VSS	H28
C37	VSS	VSS	H33
C41	VSS	VSS	H34
C6	VSS	VSS	H38
D1	VSS	VSS	H4
D12	VSS	VSS	H6
D13	VSS	VSS	H8
D14	VSS	VSS	H9
D16	VSS	VSS	J31
D18	VSS	VSS	J37
D19	VSS	VSS	J5
D20	VSS	VSS	K31
D22	VSS	VSS	K4
D24	VSS	VSS	K9
D25	VSS	VSS	L37
D26	VSS	VSS	L41
D27	VSS	VSS	M16
D28	VSS	VSS	M18
D31	VSS	VSS	M20
D32	VSS	VSS	M22
D34	VSS	VSS	M24
D37	VSS	VSS	M26
D4	VSS	VSS	M28
D41	VSS	VSS	N31
D6	VSS	VSS	N35
D7	VSS	VSS	N38
D8	VSS	VSS	N4
D9	VSS	VSS	N8
E12	VSS	VSS	R1
E3	VSS	VSS	R10
E31	VSS	VSS	R34
E35	VSS	VSS	R8
E38	VSS	VSS	T17
E4	VSS	VSS	T22
E5	VSS	VSS	AW2
E7	VSS	VSS	AW30
		VSS	AW40
		VSS	AW7

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T23	VSS	VSS	AE12
T25	VSS	VSS	AE31
T26	VSS	VSS	AE4
T28	VSS	VSS	AE41
U1	VSS	VSS	AE8
U31	VSS	VSS	AF14
U32	VSS	VSS	AF16
U4	VSS	VSS	AF17
U8	VSS	VSS	AF28
V26	VSS	VSS	AF3
V28	VSS	VSS	AG2
V38	VSS	VSS	AG30
V40	VSS	VSS	AG34
W12	VSS	VSS	AG38
W20	VSS	VSS	AG8
W22	VSS	VSS	AH14
W28	VSS	VSS	AH16
W3	VSS	VSS	AJ1
W5	VSS	VSS	AJ28
W8	VSS	VSS	AK24
Y1	VSS	VSS	AK37
Y41	VSS	VSS	AK9
AA10	VSS	VSS	AL11
AA11	VSS	VSS	AL37
AA12	VSS	VSS	AL5
AA14	VSS	VSS	AM14
AA17	VSS	VSS	AM16
AA22	VSS	VSS	AM18
AA28	VSS	VSS	AM20
AA30	VSS	VSS	AM24
AA34	VSS	VSS	AM26
AA5	VSS	VSS	AM35
AA8	VSS	VSS	AM38
AB14	VSS	VSS	AM4
AB28	VSS	VSS	AM6
AB4	VSS	VSS	AM8
AC30	VSS	VSS	AN28
AC31	VSS	VSS	AP4
AC34	VSS	VSS	AP9
AC38	VSS	VSS	AR11
AC5	VSS	VSS	AR35
AC8	VSS	VSS	AR37
AD14	VSS	VSS	AT1
AD26	VSS	VSS	AT10
AD28	VSS	VSS	AT11

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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR) INTEL:1X 0.1UF(402)
80 15 =PP3V3_S5_PCH_VCCDSW
15mA Max, 1mA Idle
C1700 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.AW39:6.35MM

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR) INTEL:1X 1UF(402)
80 15 =PP3V3_S5_PCH_VCC_SPI
22mA Max, 1mA Idle
C1702 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.R41:6.35MM

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR) INTEL:1X 0.1UF(402)
80 15 14 13 12 11 =PP3V3_S5_PCH_VCCSUS_GPIO
261mA Max, 6mA Idle
C1704 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.AN33:6.35MM

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND USB PWR) INTEL:1X 0.1UF(402)
80 15 =PP3V3_S5_PCH_VCCSUS_USB
261mA Max, 6mA Idle
C1706 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.AK20:6.35MM

PCH VCCSUS3_3 BYPASS
(PCH 3.3V DSW RTC PWR) INTEL:1X 1UF(402)
80 15 =PP3V3_S5_PCH_VCCSUS_RTC
C1708 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.AP35:6.35MM

PCH VCCCLK3_3 BYPASS 55mA Max, 11mA Idle
(PCH 3.3V CLK PWR) INTEL:4X 1UF(402)
80 15 =PP3V3_S0_PCH_VCCCLK3_3
C1720 1 1UF 10% 6.3V CERM 402 2
C1721 1 1UF 10% 6.3V CERM 402 2
C1722 1 1UF 10% 6.3V CERM 402 2
C1723 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.AP5:6.35MM
BYPASS=U1100.AV4:6.35MM
BYPASS=U1100.AR4:6.35MM
BYPASS=U1100.AT5:6.35MM

PCH VCC3_3 BYPASS
(PCH 3.3V HVCMOS PWR) INTEL:1X 0.1UF(402)
80 15 =PP3V3_S0_PCH_VCC3_3_HVCMOS
133mA Max, 3mA Idle
C1726 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.AG1:6.35MM

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR) INTEL:1X 0.1UF(402)
80 15 14 13 12 11 =PP3V3_S0_PCH_VCC3_3_GPIO
133mA Max, 3mA Idle
C1728 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.W30:6.35MM

PCH VCC3_3 BYPASS
(PCH 3.3V USB2 PWR) INTEL:1X 1UF(402)
80 15 =PP3V3_S0_PCH_VCC3_3_USB
133mA Max, 3mA Idle
C1730 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.AW21:6.35MM

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR) INTEL:1X 0.1UF(402)
80 15 =PP3V3_S0_PCH_VCC3_3_THRM
133mA Max, 3mA Idle
C1732 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.B6:6.35MM

PCH VCC BYPASS
(PCH 3.3V FUSE PWR) INTEL:1X 1UF(402)
80 15 =PP3V3_S0_PCH_VCC_FUSE
133mA Max, 3mA Idle
C1734 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.AP26:6.35MM

PCH VCCSUSHDA BYPASS
(PCH 3.3V HDA PWR) INTEL:1X 0.1UF(402)
80 15 =PP3V3_S5_PCH_VCCSUS_HDA
10mA Max, 1mA Idle
C1710 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.AW26:6.35MM

PCH VCCVRM BYPASS
(PCH 1.5V VCCVRM PWR) INTEL:1X 0.1UF(402)
80 =PP1V5_S0_PCH_VCCVRM
158mA Max, 43mA Idle
11 =PP1V5_S0_PCH_VCCVRM_BIAS
15 =PP1V5_S0_PCH_VCCVRM_FDI
15 =PP1V5_S0_PCH_VCCVRM_USB3
15 =PP1V5_S0_PCH_VCCVRM_PCIE
15 =PP1V5_S0_PCH_VCCVRM_SATA
15 =PP1V5_S0_PCH_VCCVRM_CLK
15 =PP1V5_S0_PCH_VCCVRM_THRM
C1740 1 0.1UF 20% 16V CERM 603 2
BYPASS=U1100.T14:12.7MM

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR) INTEL:1X10UF(805), 1X1UF(402)
80 15 =PP1V05_S0_PCH_VCCASW
670mA Max, 34mA Idle
C1750 1 10UF 20% 6.3V X5R 603 2
C1751 1 1UF 10% 6.3V CERM 402 2
C1752 1 1UF 10% 6.3V CERM 402 2
place_near=U1100.AD17:2.54MM
place_near=U1100.AD17:2.54MM
place_near=U1100.AD19:2.54MM

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
80 15 =PP1V05_S0_PCH_VCC
1312mA Max, 130mA Idle
THESE 4X1UF ARE EXTRA BYPASS
C1761 1 1UF 10% 6.3V CERM 402 2
C1756 1 1UF 10% 6.3V CERM 402 2
C1757 1 1UF 10% 6.3V CERM 402 2
C1758 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.P14:6.35MM
BYPASS=U1100.V22:6.35MM
BYPASS=U1100.V25:6.35MM
BYPASS=U1100.AA19:6.35MM

PCH VCCIO BYPASS
(PCH 1.05V PCIe/DMI/SATA/USB3 PWR) INTEL:2X10UF(805), 3X1UF(402)
80 15 =PP1V05_S0_PCH_VCCIO
3491mA Max, 114mA Idle
C1760 1 10UF 20% 6.3V X5R 603 2
C1755 1 10UF 20% 6.3V X5R 603 2
C1762 1 1UF 10% 6.3V CERM 402 2
C1763 1 1UF 10% 6.3V CERM 402 2
C1764 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.P14:12.7MM
BYPASS=U1100.P28:12.7MM
BYPASS=U1100.P16:6.35MM
BYPASS=U1100.P17:6.35MM
BYPASS=U1100.P26:6.35MM

PCH VCCUSBPLL BYPASS
(PCH 1.05V USB2 PLL PWR) INTEL:1X 1UF(402)
80 15 =PP1V05_S0_PCH_VCCUSBPLL
C1770 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.AP22:6.35MM

PCH VCCIO BYPASS
(PCH 1.05V FDI PWR) INTEL:1X 1UF(402)
80 15 =PP1V05_S0_PCH_VCCIO_FDI
3491mA Max, 114mA Idle
C1772 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.M14:6.35MM

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR) INTEL:1X 1UF(402)
80 15 =PP1V05_S0_PCH_VCCIO_USB2
3491mA Max, 114mA Idle
C1774 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.AF19:6.35MM

PCH V_PROC_IO BYPASS
(PCH 1.05V CPU I/F PWR) INTEL:1X1UF(603), 2X0.1UF(402)
80 15 14 =PP1V05_S0_PCH_V_PROC_IO
4mA Max, 2mA Idle
C1785 1 1UF 10% 6.3V CERM 402 2
C1786 1 0.1UF 20% 10V CERM 402 2
C1787 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.C39:12.7MM
BYPASS=U1100.C39:6.35MM
BYPASS=U1100.C39:6.35MM

PCH VCCCLK BYPASS
(PCH 1.05V SSC100 PWR) INTEL:2X 1UF(402)
80 15 =PP1V05_S0_PCH_VCCCLK_SSC100
306mA Max, 89mA Idle
C1776 1 1UF 10% 6.3V CERM 402 2
C1777 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.AA16:6.35MM
BYPASS=U1100.W16:6.35MM

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK PWR) INTEL:2X 1UF(402)
80 15 =PP1V05_S0_PCH_VCCCLK_CLK100
306mA Max, 89mA Idle
C1778 1 1UF 10% 6.3V CERM 402 2
C1783 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.U12:6.35MM
BYPASS=U1100.AB2:6.35MM

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK135 PWR) INTEL:1X 1UF(402)
80 15 =PP1V05_S0_PCH_VCCCLK_CLK135
306mA Max, 89mA Idle
C1780 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.W14:6.35MM

PCH VCCCLK BYPASS
(PCH 1.05V SSC PWR) INTEL:1X 1UF(402)
80 15 =PP1V05_S0_PCH_VCCCLK_SSC
306mA Max, 89mA Idle
C1782 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.V16:6.35MM

PCH_CLK_VCC BYPASS INTEL:1X10UF(603), 1X1UF(402)
(PCH 1.05V CLK PLL PWR. NOSTUFF 10UF IF IDG NO USED)
80 =PP1V05_S0_PCH_VCC_CLK
306mA Max, 89mA Idle
L1790 0 5% 1/10W MF-LF 603 1 2
15 PP1V05_S0_PCH_VCC_CLK_F
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
C1790 1 NOSTUFF 10UF 20% 6.3V X5R 603 2
C1791 1 1UF 10% 10V X5R 402 2
BYPASS=U1100.AB1:12.7MM
BYPASS=U1100.AB1:6.35MM

Current data from LPT EDS (doc #486708, Rev 1.0).

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Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807

(TP-P6)

CPU Micro2-XDP

PPVCCIO_S0_CPU

=PP1V05_S0_XDP → R1830 150 5% 1/16W MF-LF 402

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1
998-2516

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

XDP_CPU_PREQ_L	OBSFN_A0	OBSFN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSFN_A1	OBSFN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSFN_B0	OBSFN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSFN_B1	OBSFN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
CPU_PWR_DEBUG	VCC_OBS_AB	VCC_OBS_CD	
XDP_VR_READY	HOOK2	RESET#/HOOK6	XDP_CPURST_L
=SMBUS_XDP_SDA	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SCL	SDA	TDO	XDP_CPU_TDO
XDP_CPU_TCK	SCL	TRSTn	XDP_CPU_TRST_L
	TCK1	TDI	XDP_CPU_TDI
	TCK0	TMS	XDP_CPU_TMS
		XDP_PRESENT#	

NC per Intel DPDG.

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP_CPU_PRESENT_L

XDP C1804 0.1UF 20% 10V CERM 402
XDP C1800 0.1UF 20% 10V CERM 402
XDP C1801 0.1UF 20% 10V CERM 402
XDP C1806 0.1UF 20% 10V CERM 402

XDP R1831 1K 5% 1/16W MF-LF 402

=PP1V05_S0_XDP

XDP_CPU_TDO → R1820 51 5% 1/20W MF 201
XDP_CPU_TCK → R1823 51 5% 1/20W MF 201
XDP_CPU_TRST_L → R1824 51 5% 1/20W MF 201

TDI and TMS are terminated in CPU.

CPU_PWRGD → R1800 1K 5% 1/20W MF 201 (PLACE_NEAR=U0500.AB35:16.5mm)

PM_PWRBTN_L → R1802 0 5% 1/20W MF 0201

WF: SB DPDG says HOOK1 is BP_PWRGD_RST#

PM_PCH_SYS_PWROK → R1804 220 5% 1/20W MF 201

XDP_CPU_PRESET_L → R1805 1K 5% 1/20W MF 201 → CPU_RESET_L

CPU-PCH JTAG Chain Support

To link CPU and PCH JTAG pull ICT_JTAG_EN to 5V (must be in S0)

TP1845 (TP-P6) — ICT_JTAG_EN

Q1840 DMN5L06VK-7 SOT-563 — XDP_CPU_TMS (PLACE_NEAR=J1800.57:5.08mm) — XDP_CPU_PCH_TMS — Q1846 DMN5L06VK-7 SOT-563 — XDP_PCH_TMS (PLACE_NEAR=J1850.57:6mm)

TP1840 (TP-P6)

Q1840 DMN5L06VK-7 SOT-563 — XDP_CPU_TCK (PLACE_NEAR=J1800.58:5.08mm) — XDP_CPU_PCH_TCK — Q1846 DMN5L06VK-7 SOT-563 — XDP_PCH_TCK (PLACE_NEAR=J1850.58:5.08mm)

TP1841 (TP-P6)

Q1842 DMN32D2LFB4 DFN1006B4-3 SYM_VER_3 — XDP_CPU_TDO (PLACE_NEAR=J1800.51:5.08mm) — XDP_CPU_TDO_PCH_TDI — Q1848 DMN32D2LFB4 DFN1006B4-3 SYM_VER_3 — XDP_PCH_TDI (PLACE_NEAR=J1850.55:5.08mm)

R1842 1M 5% 1/20W MF 201
R1841 1M 5% 1/20W MF 201
R1840 1M 5% 1/20W MF 201
R1845 1K 5% 1/20W MF 201

R1892 0 5% 1/16W MF-LF 402 NOSTUFF
=PP3V3_S5_XDP → PP3V3_S5_XDP_R
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
MAX_NECK_LENGTH=3MM

XDP_PCH_TDO (J1850.51:2.54mm)
XDP_PCH_TDI (U1100.W39:21mm)
XDP_PCH_TMS (U1100.W40:21mm)
XDP_PCH_TCK

R1860 210 1% 1/20W MF 201
R1861 210 1% 1/20W MF 201
R1862 210 1% 1/20W MF 201

R1867 100 5% 1/20W MF 201 (J1850.51:5mm)
R1868 100 5% 1/20W MF 201 (U1100.W39:21MM)
R1869 100 5% 1/20W MF 201 (U1100.W40:20MM)
R1866 51 5% 1/20W MF 201

XDP SIGNALS

USB_EXTA_OC_L	R1890	SHORT	XDP_DA0_USB_EXTA_OC_L	18
USB_EXTC_OC_L	R1893	SHORT	XDP_DA1_USB_EXTC_OC_L	18
PCH_GPIO41	R1894	SHORT	XDP_DA2_PCH_GPIO41	18
PCH_GPIO42	R1895	SHORT	XDP_DA3_PCH_GPIO42	18
USB_EXTB_OC_L	R1880	SHORT	XDP_DB0_USB_EXTB_OC_L	18
USB_EXTD_OC_L	R1881	SHORT	XDP_DB1_USB_EXTD_OC_L	18
PCH_GPIO10	R1896	SHORT	XDP_DB2_PCH_GPIO10	18
SDCONN_STATE_CHANGE	R1897	SHORT	XDP_DB3_SDCONN_STATE_CHANGE_L	18
DP_AUXIO_EN	R1872	SHORT	XDP_DC0_DP_AUXCH_ISOL_L	18
SATARDRVR_EN	R1873	SHORT	XDP_DC1_SATARDRVR_EN	18
PCH_GPIO36	R1874	SHORT	XDP_DC2_PCH_GPIO36	18
JTAG_ISP_TCK	R1875	SHORT	XDP_DC3_JTAG_ISP_TCK	18
PCH_GPIO16	R1878	SHORT	XDP_DD0_PCH_GPIO16	18
PCH_GPIO49	R1879	SHORT	XDP_DD1_PCH_GPIO49	18
ENET_CLKREQ_L	R1882	SHORT	XDP_DD2_ENET_CLKREQ_L	18
AP_CLKREQ_L	R1883	SHORT	XDP_DD3_AP_CLKREQ_L	18
HDD_PWR_EN	R1886	SHORT	XDP_FC0_HDD_PWR_EN	18
GPU_GOOD	R1887	SHORT	XDP_FC1_GPU_GOOD	18

(All 18 R's) OMIT — NONE NONE NONE 402

PCH SIGNALS

PM_RSMRST_PCH_L → R1884 1K 5% 1/20W MF 201 (PLACE_NEAR=J1850.40:2.54mm)

PM_PWRBTN_L → R1885 0 5% 1/20W MF 0201 (PLACE_NEAR=U5000.J3:2.54mm)

PCH Micro2-XDP

=PP3V3_S5_XDP

CRITICAL
XDP_CONN
J1850
DF40RC-60DP-0.4V
M-ST-SM1
998-2516

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

XDP_DA0_USB_EXTA_OC_L	OBSFN_A0	OBSFN_C0	XDP_FC0_HDD_PWR_EN
XDP_DA1_USB_EXTC_OC_L	OBSFN_A1	OBSFN_C1	XDP_FC1_GPU_GOOD
	OBSDATA_A0	OBSDATA_C0	XDP_DC0_DP_AUXCH_ISOL_L
	OBSDATA_A1	OBSDATA_C1	XDP_DC1_SATARDRVR_EN
XDP_DA2_PCH_GPIO41	OBSDATA_A2	OBSDATA_C2	XDP_DC2_PCH_GPIO36
XDP_DA3_PCH_GPIO42	OBSDATA_A3	OBSDATA_C3	XDP_DC3_JTAG_ISP_TCK
	OBSFN_B0	OBSFN_D0	
	OBSFN_B1	OBSFN_D1	
XDP_DB0_USB_EXTB_OC_L	OBSDATA_B0	OBSDATA_D0	XDP_DD0_PCH_GPIO16
XDP_DB1_USB_EXTD_OC_L	OBSDATA_B1	OBSDATA_D1	XDP_DD1_PCH_GPIO49
XDP_DB2_PCH_GPIO10	OBSDATA_B2	OBSDATA_D2	XDP_DD2_ENET_CLKREQ_L
XDP_DB3_SDCONN_STATE_CHANGE_L	OBSDATA_B3	OBSDATA_D3	XDP_DD3_AP_CLKREQ_L
XDP_PCH_S5_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	
XDP_PCH_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	
	VCC_OBS_AB	VCC_OBS_CD	
	HOOK2	RESET#/HOOK6	XDP_PM_PCH_PWROK
	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_PCH_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	TP_XDP_PCH_TRST_L
	TCK1	TDI	XDP_PCH_TDI
XDP_PCH_TCK	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	

R1870 1K 5% 1/20W MF 201 → PM_PCH_PWROK

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP C1880 0.1UF 20% 10V CERM 402
XDP C1881 0.1UF 20% 10V CERM 402

PCH/XDP Signal Isolation Notes:

'Output' non-XDP signals require pulls.
'Output' PCH/XDP signals require pulls.

R187x and R189x should be placed where signal path needs to split between route from PCH to J1850 and path to non-XDP signal destination (to minimize stub).

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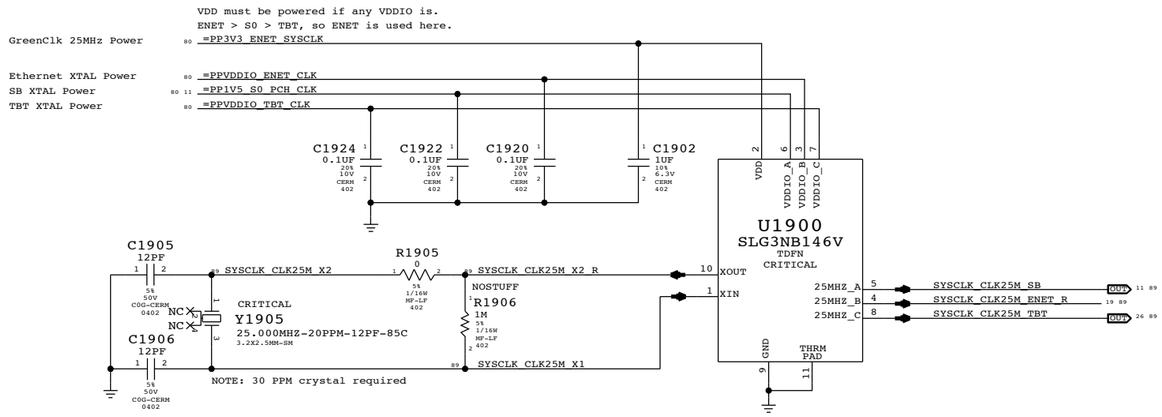
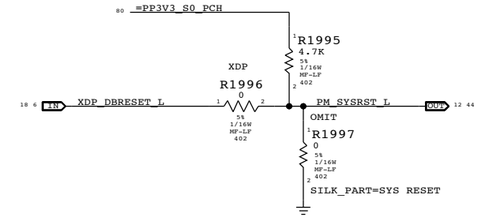
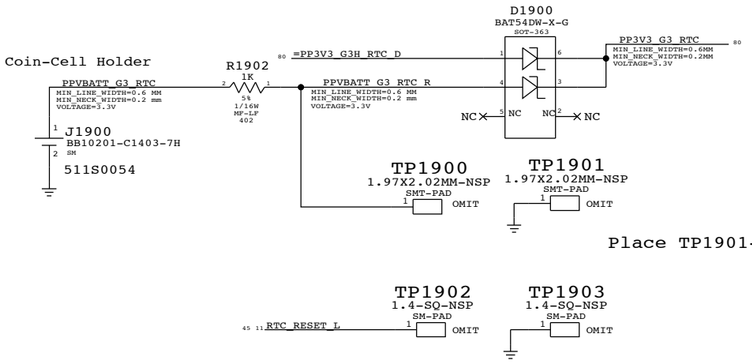
System 25MHz Clock Generator



PCH Reset Button

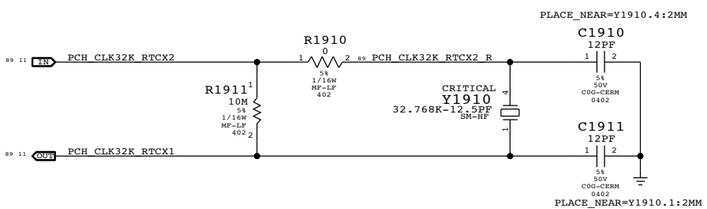


RTC Power Sources

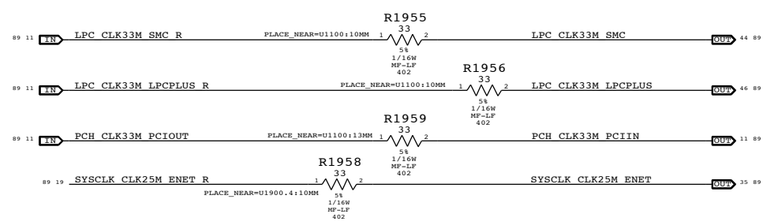


Place TP1901-TP1903 on bottom side

PCH RTC Crystal

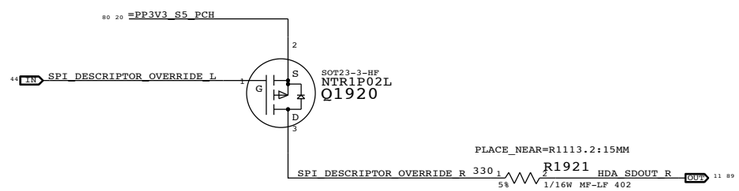


Clock series termination



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.



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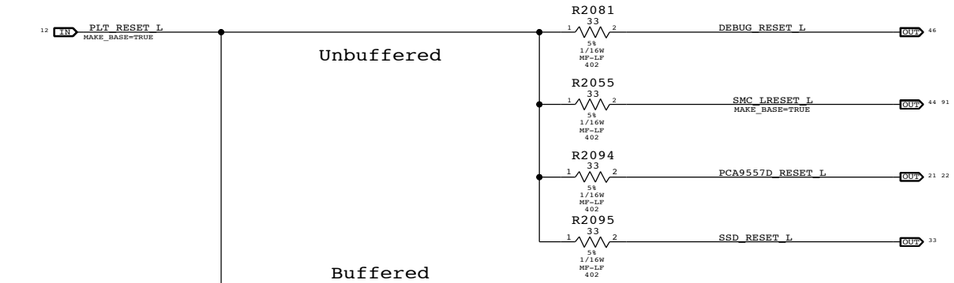
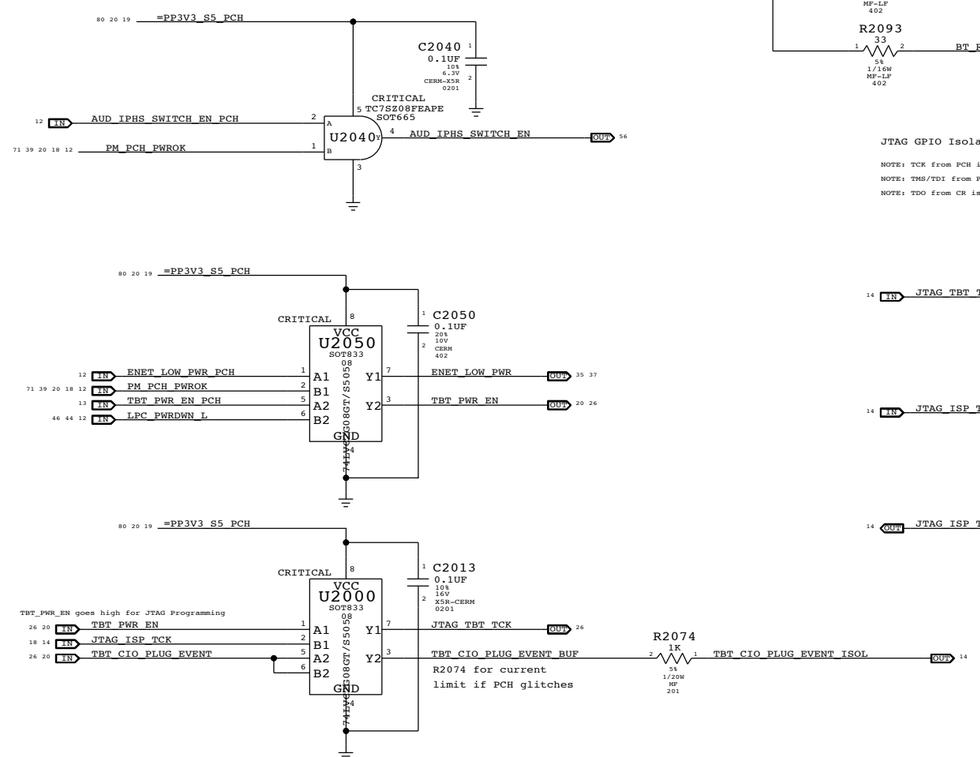
Platform Reset Connections

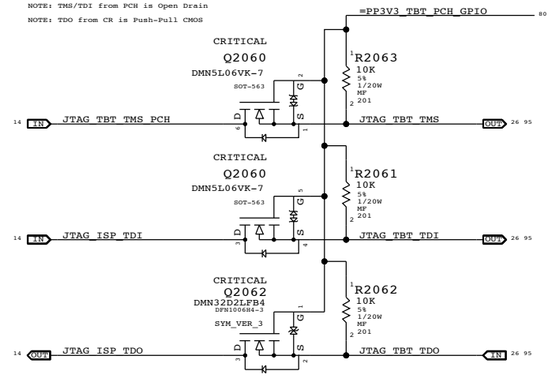


GPIO Glitch Prevention



JTAG GPIO Isolation due to glitch in and out of sleep

NOTE: TCK from PCH is Push-Pull CMOS
NOTE: TMS/TDI from PCH is Open Drain
NOTE: TDO from CR is Push-Pull CMOS



R2060 10K 5% 1/20W MF 201 — TBT_CIO_PLUG_EVENT 20 26

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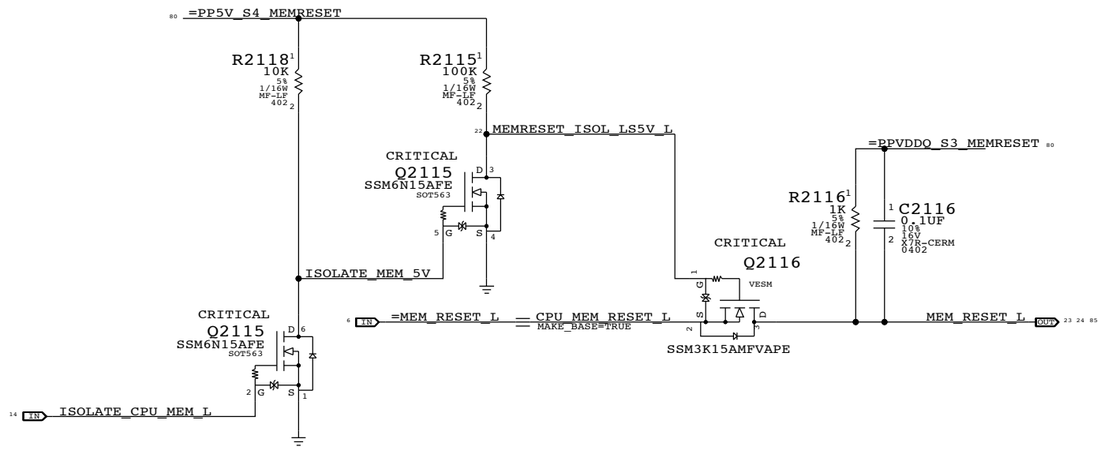
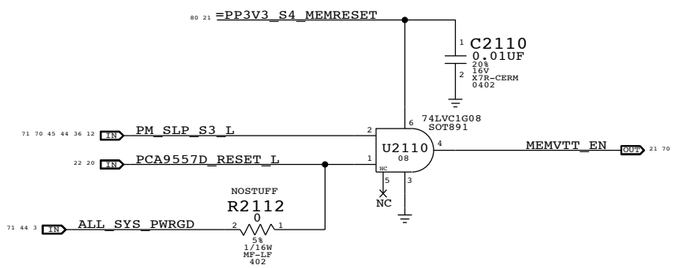
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

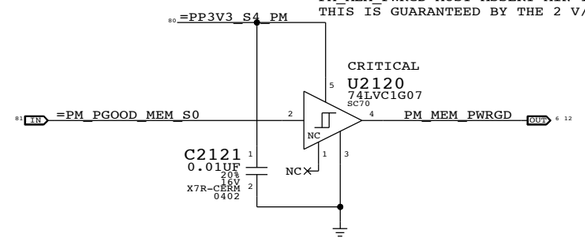
MEMVTT_EN = PLT_RESET_L * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L





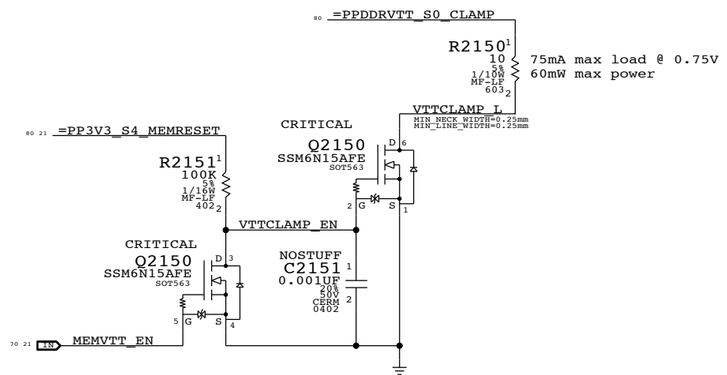
MEM S0 "PGOOD" FOR CPU

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page
PM_MEM_PWRGD MUST ASSERT MIN 100 NS AFTER MEM_VDDQ RAMPS 80%
THIS IS GUARANTEED BY THE 2 V/MS RAMP RATE OF THE FET



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1
to	1	0	1	1	1	1	1
S3	2	0	0	1	1	1	0
	3	0	0	0	X	1	0
S3	4	0	0	1	X	1	0
to	5	0	1	1	0 (*)	1	1
S0	6	0	1	1	1	1	1
	7	1	1	1	1	CPU_MEM_RESET_L	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must de-assert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=J17 SYNC_DATE=04/21/2013
PAGE TITLE
CPU Memory S3 Support

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Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during S3

21 MEMRESET_ISOL_LS5V_L
7 CPU_DIMMA_VREFDQ
7 CPU_DIMMB_VREFDQ
7 CPU_DIMM_VREFCA

CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563
CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure ISOLATE_CPU_MEM_L is low to remove short due to CPU.

CPU_MEM_VREFDQ_A_ISOL
CPU_MEM_VREFDQ_B_ISOL
CPU_MEM_VREFCA_A_ISOL
CPU_MEM_VREFCA_B_ISOL

EN RC's to avoid drain glitches

DDRVREF_DAC R2225 100K 5% 1/16W MF-LF 402 — VREFMRGN_DQ_A_EN_RC
DDRVREF_DAC R2201 100K 5% 1/20W MF 201
DDRVREF_DAC C2225 0.1UF 20% 10V CERM 402
CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563
Q2225 pin 6: PLACE_NEAR=Q2220.6:5mm

DDRVREF_DAC R2245 100K 5% 1/16W MF-LF 402 — VREFMRGN_DQ_B_EN_RC
DDRVREF_DAC R2202 100K 5% 1/20W MF 201
DDRVREF_DAC C2245 0.1UF 20% 10V CERM 402
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563
Q2265 pin 6: PLACE_NEAR=Q2260.6:5mm

DDRVREF_DAC R2265 100K 5% 1/16W MF-LF 402 — VREFMRGN_CA_A_EN_RC
DDRVREF_DAC R2207 100K 5% 1/20W MF 201
DDRVREF_DAC C2265 0.1UF 20% 10V CERM 402
CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563

DDRVREF_DAC R2285 100K 5% 1/16W MF-LF 402 — VREFMRGN_CA_B_EN_RC
DDRVREF_DAC R2208 100K 5% 1/20W MF 201
DDRVREF_DAC C2285 0.1UF 20% 10V CERM 402
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563

(All 4 R's) DDRVREF_DAC
R2226 332 1% 1/16W MF-LF 402 — VREFMRGN_DQ_A_RDIV
R2246 332 1% 1/16W MF-LF 402 — VREFMRGN_DQ_B_RDIV
R2266 332 1% 1/16W MF-LF 402 — VREFMRGN_CA_A_RDIV
R2286 332 1% 1/16W MF-LF 402 — VREFMRGN_CA_B_RDIV

R22x6 pin 2:
PLACE_NEAR=Q2225.1:5.5mm
PLACE_NEAR=Q2265.4:5.5mm
PLACE_NEAR=Q2225.1:5.5mm
PLACE_NEAR=Q2265.4:5.5mm

VRef Dividers

Always used, regardless of margining option.

=PPDDR_S3_MEMVREF 80

PLACE_NEAR=C2220.1:2mm
R2223 2 5% 1/20W MF 201
C2220 0.022UF 10% 6.3V X5R-CERM 0201
MEM_VREFDQ_A_RC
PLACE_NEAR=C2220.6:2mm
PLACE_NEAR=C2221.2:1mm
R2221 1K 1% 1/16W MF-LF 402 — PLACE_NEAR=R2223.2:1.5MM
R2222 1K 1% 1/16W MF-LF 402
R2220 24.9 1% 1/20W MF 201
PPVPREF_S3_MEM_VREFDQ_A 23
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm

PLACE_NEAR=C2240.1:2mm
R2243 2 5% 1/20W MF 201
C2240 0.022UF 10% 6.3V X5R-CERM 0201
MEM_VREFDQ_B_RC
PLACE_NEAR=C2260.6:4MM
PLACE_NEAR=C2241.2:1mm
R2241 1K 1% 1/16W MF-LF 402 — PLACE_NEAR=R2243.2:1mm
R2242 1K 1% 1/16W MF-LF 402
R2240 24.9 1% 1/20W MF 201
PPVPREF_S3_MEM_VREFDQ_B 24
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm

PLACE_NEAR=C2260.1:2mm
R2263 2 5% 1/20W MF 201
C2260 0.022UF 10% 6.3V X5R-CERM 0201
MEM_VREFCA_A_RC
PLACE_NEAR=C2220.3:2mm
PLACE_NEAR=C2261.2:1mm
R2261 1K 1% 1/16W MF-LF 402 — PLACE_NEAR=R2263.2:1mm
R2262 1K 1% 1/16W MF-LF 402
R2260 24.9 1% 1/20W MF 201
PPVPREF_S3_MEM_VREFCA_A 23
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm

PLACE_NEAR=C2280.1:2mm
R2283 2 5% 1/20W MF 201
C2280 0.022UF 10% 6.3V X5R-CERM 0201
MEM_VREFCA_B_RC
PLACE_NEAR=C2260.3:2mm
PLACE_NEAR=C2281.2:1mm
R2281 1K 1% 1/16W MF-LF 402 — PLACE_NEAR=R2283.2:1.5MM
R2282 1K 1% 1/16W MF-LF 402
R2280 24.9 1% 1/20W MF 201
PPVPREF_S3_MEM_VREFCA_B 24
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

80 22 =PP3V3_S3_VREFMRGN
OMIT R2218 SHORT NONE NONE 402
PP3V3_S3_VREFMRGN
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

DDRVREF_DAC C2200 2.2UF 20% 6.3V CERM 402-LF
DDRVREF_DAC C2201 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL DDRVREF_DAC U2200 MSOP DAC55574
VDD
47 =I2C_VREFDACS_SCL — SCL
47 =I2C_VREFDACS_SDA — SDA
A0
A1
GND
VOUTA VREFMRGN_DQ_A
VOUTB VREFMRGN_DQ_B
VOUTC VREFMRGN_CA_AB
VOUTD VREFMRGN_MEMVREG_FBVREF
Addr=0x98(WR)/0x99(RD)

NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

DDRVREF_DAC C2202 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL DDRVREF_DAC U2201 PCA9557 QFN
VCC
(OD) P0 NC
P1 VREFMRGN_DQ_A_EN
P2 VREFMRGN_DQ_B_EN
P3 VREFMRGN_CA_A_EN
P4 VREFMRGN_CA_B_EN
P5 VREFMRGN_MEMVREG_EN
P6 VREFMRGN_FRAMEBUF_EN
P7 NC
A0
A1
A2
47 =I2C_PCA9557D_SCL — SCL
47 =I2C_PCA9557D_SDA — SDA
RESET*
THRM PAD
GND
Addr=0x30(WR)/0x31(RD)

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

21 20 PCA9557D_RESET_L

=PP3V3_S3_VREFMRGN 22 80
DDRVREF_DAC C2205 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL DDRVREF_DAC U2204 MAX4253 UCSP
VREFMRGN_MEMVREG_BUF
DDRVREF_DAC R2214 33.2K 1% 1/16W MF-LF 402
DDREG_FB OUT 63

DDRVREF_DAC R2213 100K 5% 1/20W MF 201
CRITICAL DDRVREF_DAC U2204 MAX4253 UCSP
VREFMRGN_FRAMEBUF_BUF
DDRVREF_DAC R2217 1M 5% 1/16W MF-LF 402
Pins B1 & B4:
CKPLUS_WAIVE=unconnected_pins

DDRVREF_DAC R2215 100K 5% 1/20W MF 201

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	
DAC Channel:	A	B	C	C	D	
PCA9557D Pin:	1	2	3	4	5	
	DDR3 (1.5V)		DDR3L (1.35V)		DDR3 (1.5V)	DDR3L (1.35V)
Nominal value	0.750V (DAC: 0x3A = 0.747mV)		0.675V (DAC: 0x34 = 0.670mV)		1.500V (DAC: 0x74 = 1.495V)	1.343V (DAC: 0x68 = 1.341V)
Margined target:	0.300V - 1.200V (+/- 450mV)		0.275V - 1.075V (+/- 400mV)		1.200V - 1.800V (+/- 300mV)	0.950V - 1.750V (+/- 400mV)
DAC range:	0.000V - 1.508V (0x00 - 0x75)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 3.004V (0x00 - 0xE9)	0.000V - 2.707V (0x00 - 0xD2)
Margined range:	0.299V - 1.206V (+/- 453mV)		0.269V - 1.083V (+/- 406mV)		1.199V - 1.801V (+/- 301mV)	0.932V - 1.760V (+/- 414mV)
VRef current:	+901uA - -911uA (- = sourced)		+811uA - -816uA (- = sourced)		+36uA - -36uA (- = sourced)	+28uA - -29uA (- = sourced)
DAC step size:	7.68mV / step @ output		7.67mV / step @ output		2.575mV / step @ output	3.923mV / step @ output

NOTE: DDR3 assumes TPS51916 supply with 10.0k/49.9k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

SYNC MASTER=J17 SYNC DATE=04/21/2013
PAGE TITLE: DDR3 VREF MARGINING

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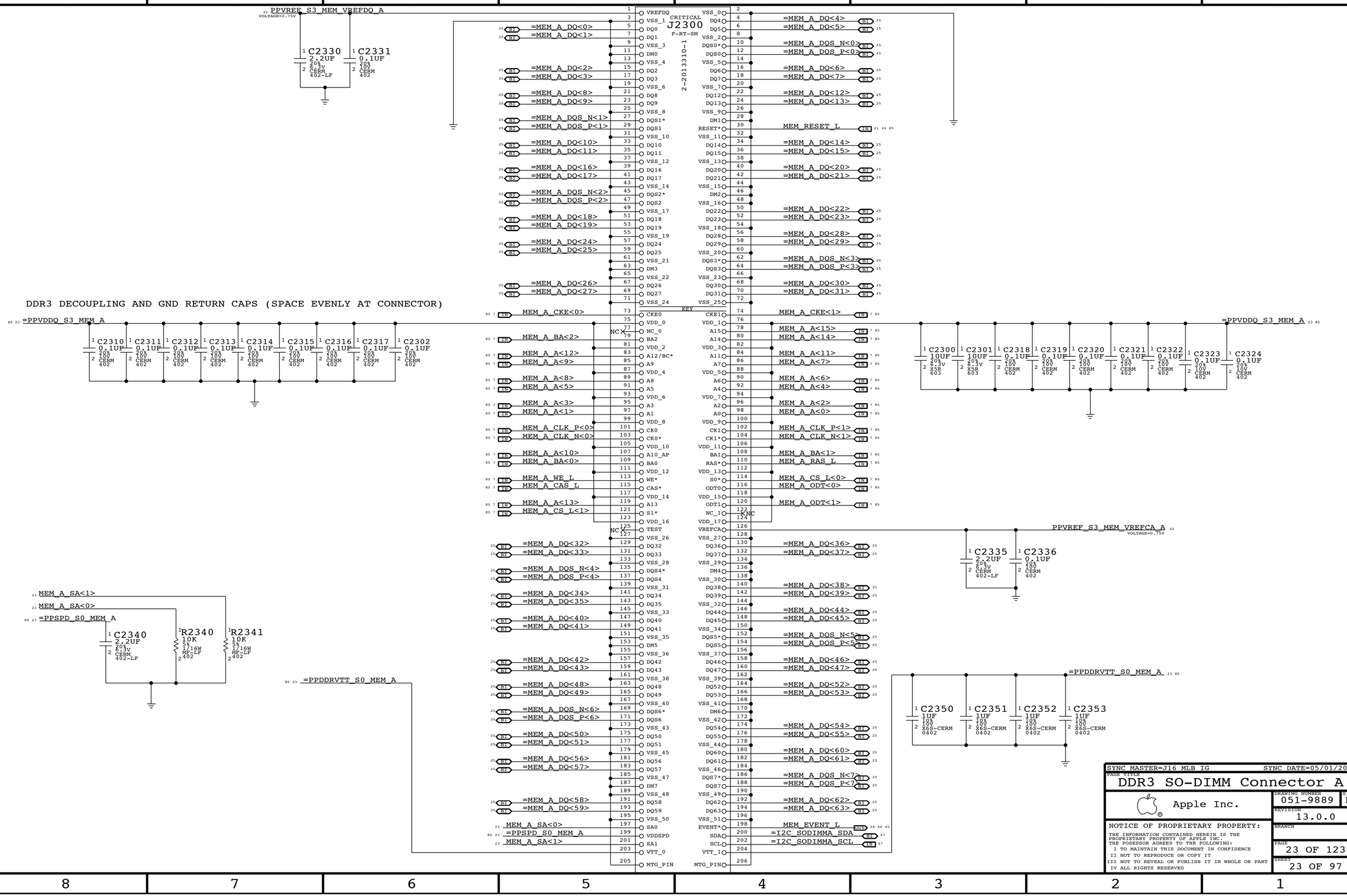
PPVREF_S3_MEM_VREFDQ_A
VOLTAGE=0.75V
C2330 2.2UF 20% 6.3V CERM 402-LF
C2331 0.1UF 20% 10V CERM 402
J2300
CRITICAL
F-RT-SM
2-2013310-1
DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)
=PPVDDQ_S3_MEM_A
C2310 0.1UF 20% 10V CERM 402
C2311 0.1UF 20% 10V CERM 402
C2312 0.1UF 20% 10V CERM 402
C2313 0.1UF 20% 10V CERM 402
C2314 0.1UF 20% 10V CERM 402
C2315 0.1UF 20% 10V CERM 402
C2316 0.1UF 20% 10V CERM 402
C2317 0.1UF 20% 10V CERM 402
C2302 0.1UF 20% 10V CERM 402
C2300 10UF 20% 6.3V X5R 603
C2301 10UF 20% 6.3V X5R 603
C2318 0.1UF 20% 10V CERM 402
C2319 0.1UF 20% 10V CERM 402
C2320 0.1UF 20% 10V CERM 402
C2321 0.1UF 20% 10V CERM 402
C2322 0.1UF 20% 10V CERM 402
C2323 0.1UF 20% 10V CERM 402
C2324 0.1UF 20% 10V CERM 402
MEM_A_SA<1>
MEM_A_SA<0>
=PPSPD_S0_MEM_A
C2340 2.2UF 20% 6.3V CERM 402-LF
R2340 10K 5% 1/16W ME-LF 402
R2341 10K 5% 1/16W ME-LF 402
=PPDDRVTT_S0_MEM_A
C2335 2.2UF 20% 6.3V CERM 402-LF
C2336 0.1UF 20% 10V CERM 402
C2350 1UF 10% 10V X6S-CERM 0402
C2351 1UF 10% 10V X6S-CERM 0402
C2352 1UF 10% 10V X6S-CERM 0402
C2353 1UF 10% 10V X6S-CERM 0402
SYNC_MASTER=J16_MLB_IG
SYNC_DATE=05/01/2013
PAGE TITLE
DDR3 SO-DIMM Connector A
Apple Inc.
DRAWING NUMBER 051-9889
SIZE D
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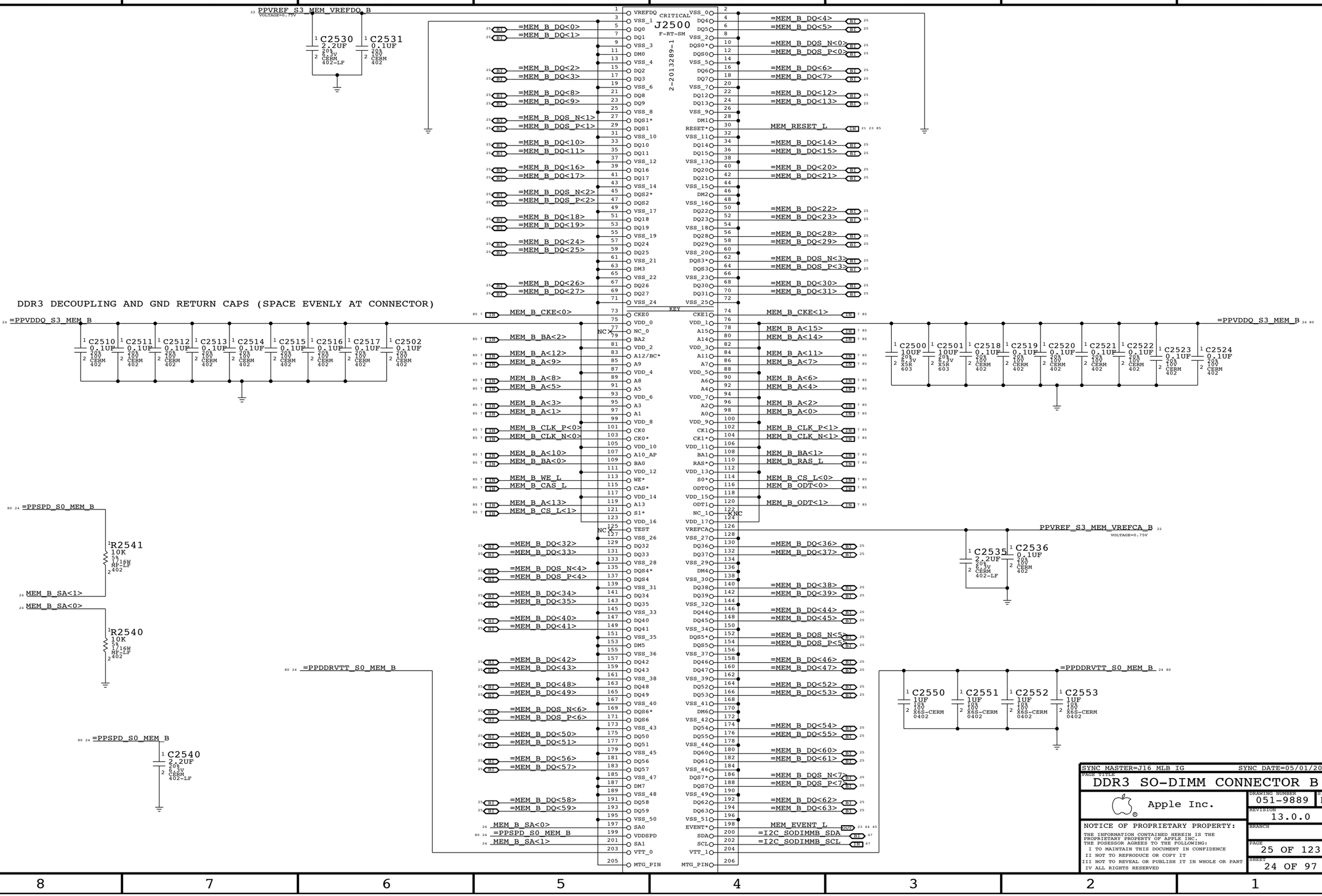

SYNC_MASTER=J16_MLB_IG SYNC_DATE=05/01/2013

PAGE TITLE
DDR3 SO-DIMM CONNECTOR B

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THERE ARE NO PIN SWAPS

MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<0>
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<0>
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MEM_A_DQ<3>	MAKE_BASE=TRUE	=	=MEM_A_DQ<3>
MEM_A_DQ<2>	MAKE_BASE=TRUE	=	=MEM_A_DQ<2>
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MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<1>
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MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<3>
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<3>
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MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<4>
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MEM_A_DQ<44>	MAKE_BASE=TRUE	=	=MEM_A_DQ<44>
MEM_A_DQ<43>	MAKE_BASE=TRUE	=	=MEM_A_DQ<43>
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MEM_A_DQ<41>	MAKE_BASE=TRUE	=	=MEM_A_DQ<41>
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MEM_A_DQ<52>	MAKE_BASE=TRUE	=	=MEM_A_DQ<52>
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MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<0>
MEM_B_DQ<7>	MAKE_BASE=TRUE	=	=MEM_B_DQ<7>
MEM_B_DQ<6>	MAKE_BASE=TRUE	=	=MEM_B_DQ<6>
MEM_B_DQ<5>	MAKE_BASE=TRUE	=	=MEM_B_DQ<5>
MEM_B_DQ<4>	MAKE_BASE=TRUE	=	=MEM_B_DQ<4>
MEM_B_DQ<3>	MAKE_BASE=TRUE	=	=MEM_B_DQ<3>
MEM_B_DQ<2>	MAKE_BASE=TRUE	=	=MEM_B_DQ<2>
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MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<1>
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MEM_B_DQ<19>	MAKE_BASE=TRUE	=	=MEM_B_DQ<19>
MEM_B_DQ<18>	MAKE_BASE=TRUE	=	=MEM_B_DQ<18>
MEM_B_DQ<17>	MAKE_BASE=TRUE	=	=MEM_B_DQ<17>
MEM_B_DQ<16>	MAKE_BASE=TRUE	=	=MEM_B_DQ<16>
MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<3>
MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<3>
MEM_B_DQ<31>	MAKE_BASE=TRUE	=	=MEM_B_DQ<31>
MEM_B_DQ<30>	MAKE_BASE=TRUE	=	=MEM_B_DQ<30>
MEM_B_DQ<29>	MAKE_BASE=TRUE	=	=MEM_B_DQ<29>
MEM_B_DQ<28>	MAKE_BASE=TRUE	=	=MEM_B_DQ<28>
MEM_B_DQ<27>	MAKE_BASE=TRUE	=	=MEM_B_DQ<27>
MEM_B_DQ<26>	MAKE_BASE=TRUE	=	=MEM_B_DQ<26>
MEM_B_DQ<25>	MAKE_BASE=TRUE	=	=MEM_B_DQ<25>
MEM_B_DQ<24>	MAKE_BASE=TRUE	=	=MEM_B_DQ<24>
MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<4>
MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<4>
MEM_B_DQ<39>	MAKE_BASE=TRUE	=	=MEM_B_DQ<39>
MEM_B_DQ<38>	MAKE_BASE=TRUE	=	=MEM_B_DQ<38>
MEM_B_DQ<37>	MAKE_BASE=TRUE	=	=MEM_B_DQ<37>
MEM_B_DQ<36>	MAKE_BASE=TRUE	=	=MEM_B_DQ<36>
MEM_B_DQ<35>	MAKE_BASE=TRUE	=	=MEM_B_DQ<35>
MEM_B_DQ<34>	MAKE_BASE=TRUE	=	=MEM_B_DQ<34>
MEM_B_DQ<33>	MAKE_BASE=TRUE	=	=MEM_B_DQ<33>
MEM_B_DQ<32>	MAKE_BASE=TRUE	=	=MEM_B_DQ<32>
MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<5>
MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<5>
MEM_B_DQ<47>	MAKE_BASE=TRUE	=	=MEM_B_DQ<47>
MEM_B_DQ<46>	MAKE_BASE=TRUE	=	=MEM_B_DQ<46>
MEM_B_DQ<45>	MAKE_BASE=TRUE	=	=MEM_B_DQ<45>
MEM_B_DQ<44>	MAKE_BASE=TRUE	=	=MEM_B_DQ<44>
MEM_B_DQ<43>	MAKE_BASE=TRUE	=	=MEM_B_DQ<43>
MEM_B_DQ<42>	MAKE_BASE=TRUE	=	=MEM_B_DQ<42>
MEM_B_DQ<41>	MAKE_BASE=TRUE	=	=MEM_B_DQ<41>
MEM_B_DQ<40>	MAKE_BASE=TRUE	=	=MEM_B_DQ<40>
MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<6>
MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<6>
MEM_B_DQ<55>	MAKE_BASE=TRUE	=	=MEM_B_DQ<55>
MEM_B_DQ<54>	MAKE_BASE=TRUE	=	=MEM_B_DQ<54>
MEM_B_DQ<53>	MAKE_BASE=TRUE	=	=MEM_B_DQ<53>
MEM_B_DQ<52>	MAKE_BASE=TRUE	=	=MEM_B_DQ<52>
MEM_B_DQ<51>	MAKE_BASE=TRUE	=	=MEM_B_DQ<51>
MEM_B_DQ<50>	MAKE_BASE=TRUE	=	=MEM_B_DQ<50>
MEM_B_DQ<49>	MAKE_BASE=TRUE	=	=MEM_B_DQ<49>
MEM_B_DQ<48>	MAKE_BASE=TRUE	=	=MEM_B_DQ<48>
MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<7>
MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<7>
MEM_B_DQ<63>	MAKE_BASE=TRUE	=	=MEM_B_DQ<63>
MEM_B_DQ<62>	MAKE_BASE=TRUE	=	=MEM_B_DQ<62>
MEM_B_DQ<61>	MAKE_BASE=TRUE	=	=MEM_B_DQ<61>
MEM_B_DQ<60>	MAKE_BASE=TRUE	=	=MEM_B_DQ<60>
MEM_B_DQ<59>	MAKE_BASE=TRUE	=	=MEM_B_DQ<59>
MEM_B_DQ<58>	MAKE_BASE=TRUE	=	=MEM_B_DQ<58>
MEM_B_DQ<57>	MAKE_BASE=TRUE	=	=MEM_B_DQ<57>
MEM_B_DQ<56>	MAKE_BASE=TRUE	=	=MEM_B_DQ<56>

SYNC MASTER=J16_MLB_IG SYNC DATE=05/01/2013

PAGE TITLE
DDR3 ALIASES AND BITSWAPS

Apple Inc.

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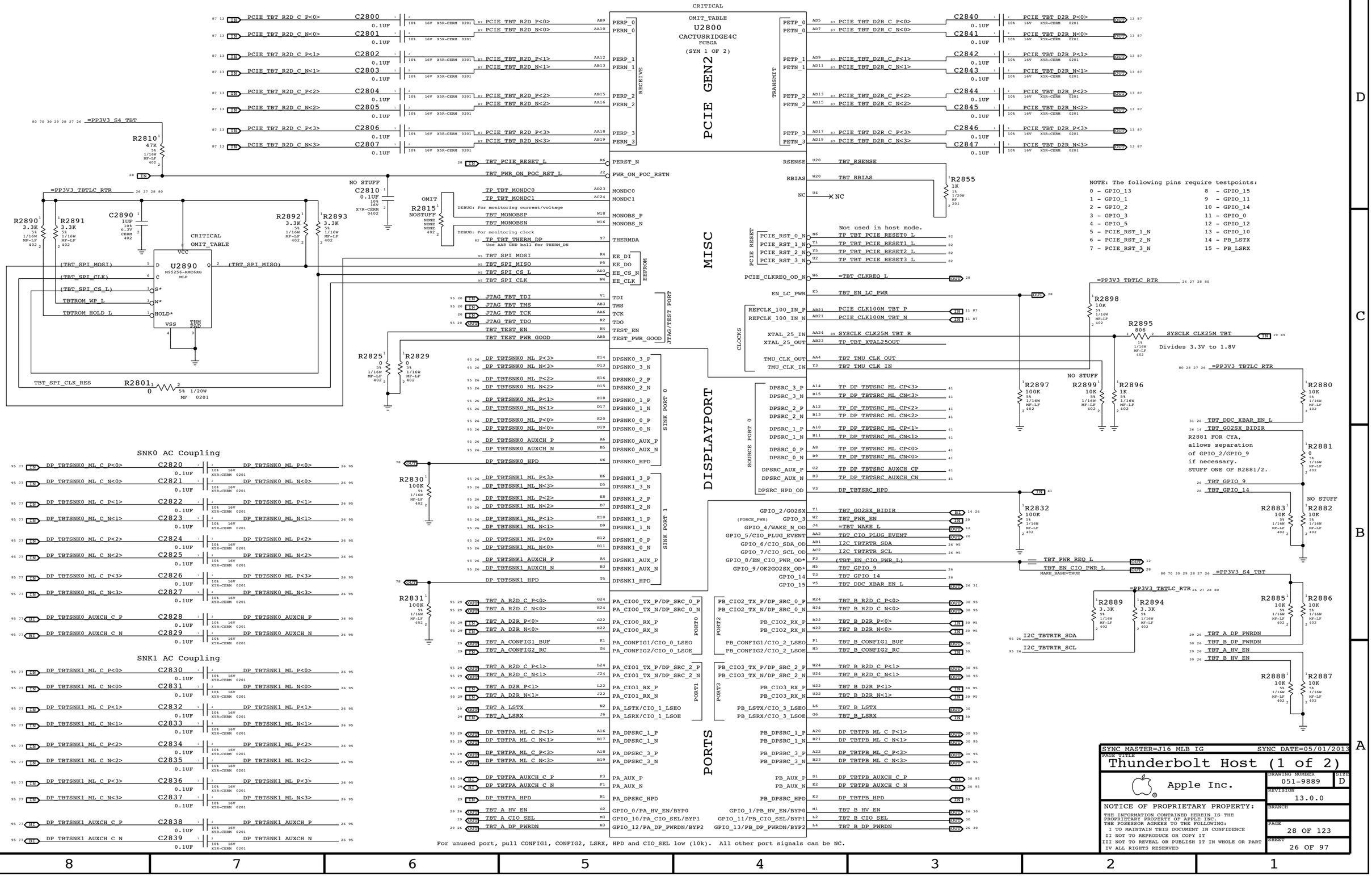
PCIE GEN2
MISC
DISPLAYPORTS
U2800
CACTUSRIDGE4C
FCBGA
(SYM 1 OF 2)
CRITICAL
OMIT_TABLE
RECEIVE
TRANSMIT
U2890
M95256-RMC6XG
MLP
EEPROM
JTAG/TEST PORT
SINK PORT 0
SINK PORT 1
SOURCE PORT 0
PORT0
PORT1
PORT2
PORT3
CLOCKS
PCIE RESET
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
SNK0 AC Coupling
SNK1 AC Coupling
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
SYNC MASTER=J16 MLB IG
SYNC DATE=05/01/2013
PAGE TITLE
Thunderbolt Host (1 of 2)
Apple Inc.
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SIZE D
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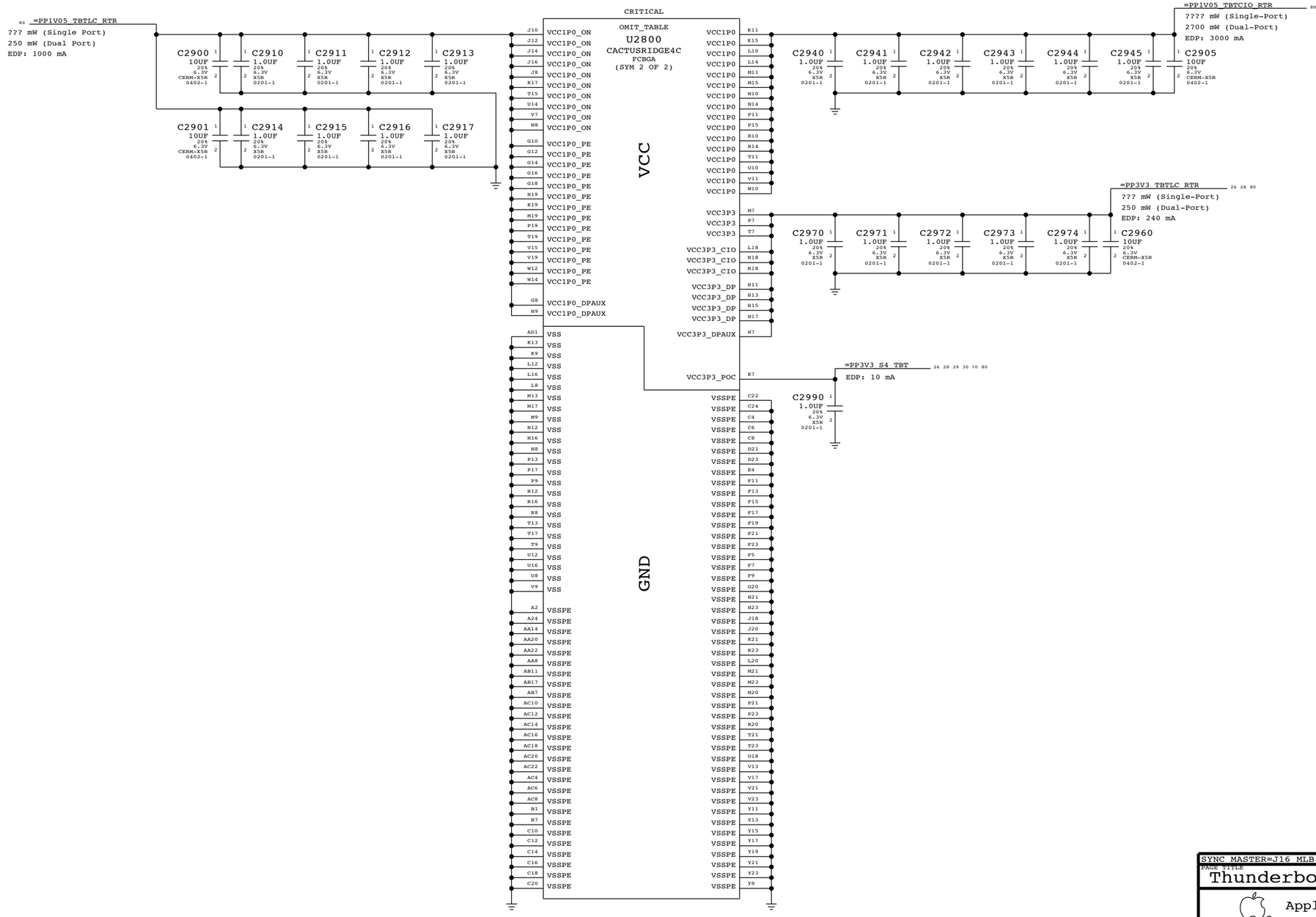

EDP current / power consumption figures from CR DG v0.57, IBL doc #472455.

SYNC MASTER=J16 MLB IG SYNC DATE=05/01/2013

PAGE TITLE
Thunderbolt Host (2 of 2)

Apple Inc.

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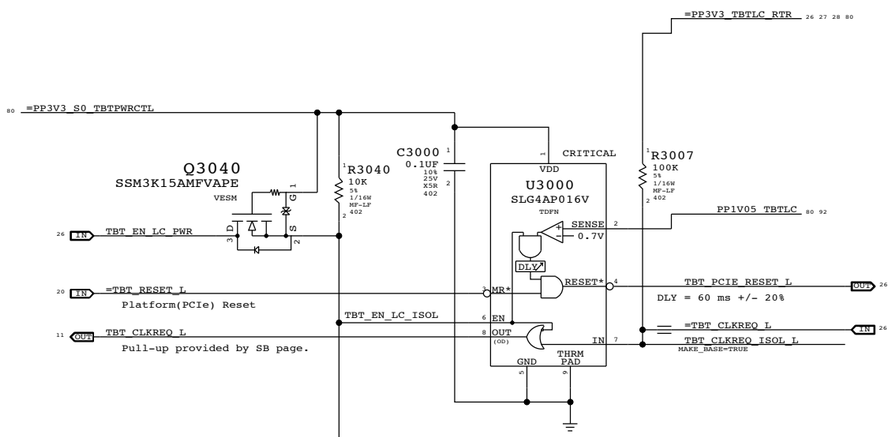
Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

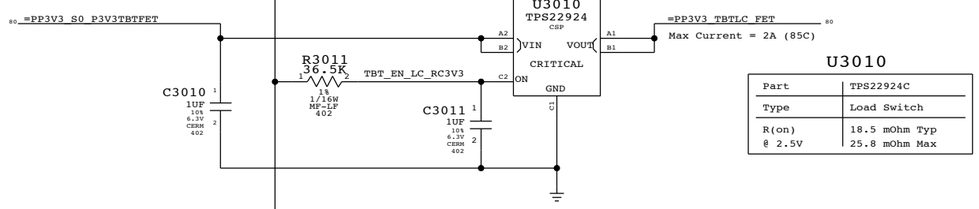
Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

Supervisor & CLKREQ# Isolation

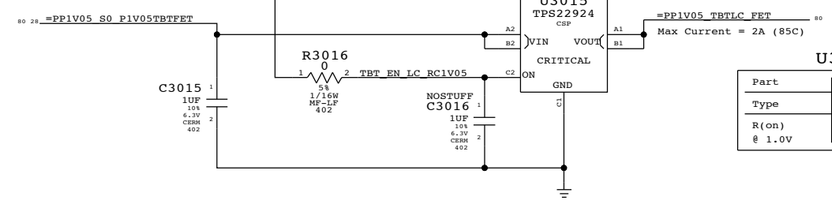


3.3V TBT "LC" Switch



U3010	
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

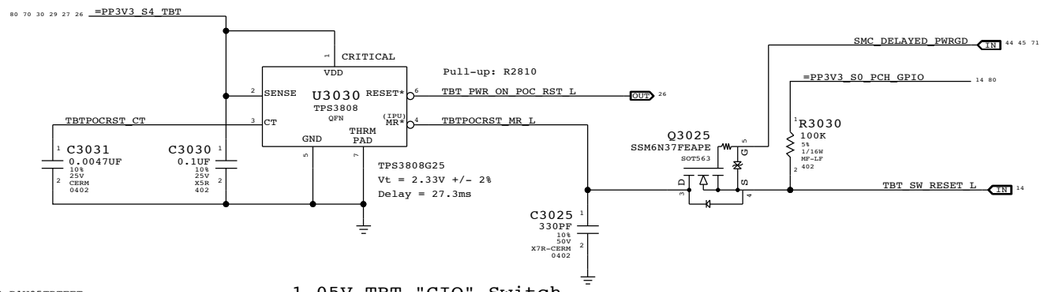
1.05V TBT "LC" Switch



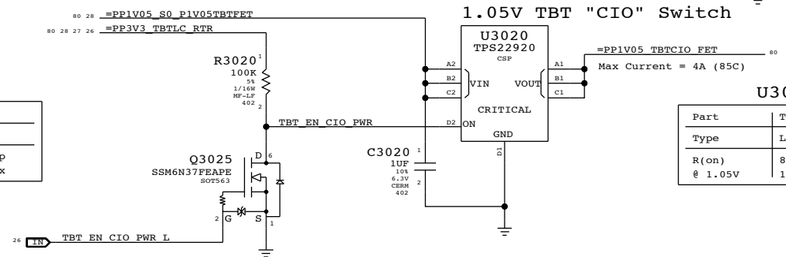
U3015	
Part	TPS22924C
Type	Load Switch
R(on) @ 1.0V	20.3 mOhm Typ 28.6 mOhm Max

TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.



1.05V TBT "CIO" Switch



U3020	
Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

SYNC MASTER=J16_MLB_IG SYNC DATE=05/01/2013

PAGE TITLE
Thunderbolt Power Support

Apple Inc.

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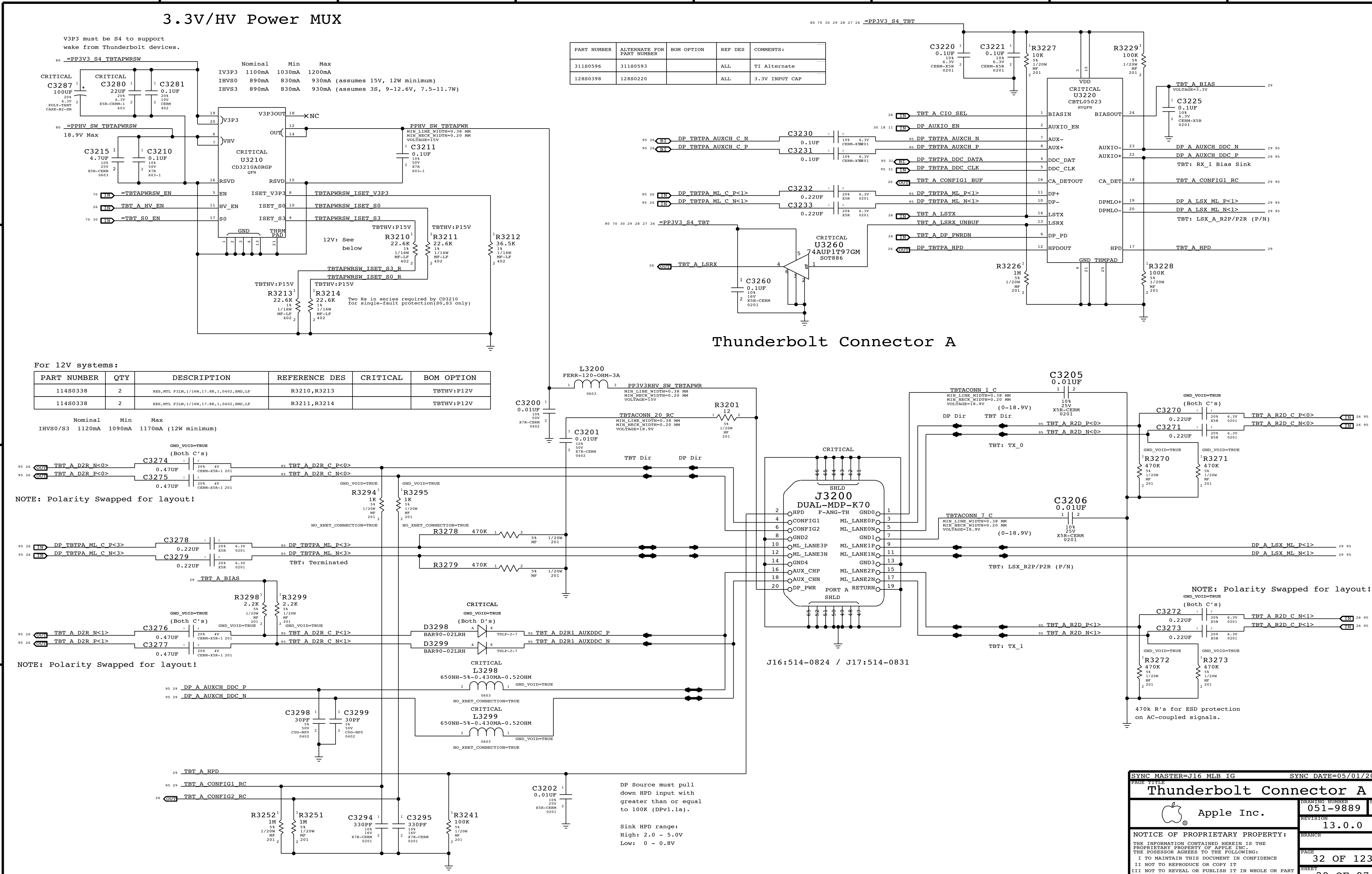
3.3V/HV Power MUX


V3P3 must be S4 to support
wake from Thunderbolt devices.
Nominal Min Max
IV3P3 1100mA 1030mA 1200mA
IHVS0 890mA 830mA 930mA (assumes 15V, 12W minimum)
IHVS3 890mA 830mA 930mA (assumes 3S, 9-12.6V, 7.5-11.7W)
=PP3V3_S4_TBTAPWRSW
=PPHV_SW_TBTAPWRSW
18.9V Max
CRITICAL
C3287
100UF
C3280
22UF
C3281
0.1UF
C3215
4.7UF
C3210
0.1UF
CRITICAL
U3210
CD3210A0RGP
QFN
V3P3OUT
NC
PPHV_SW_TBTAPWR
C3211
0.1UF
=TBTAPWRSW_EN
TBT_A_HV_EN
=TBT_S0_EN
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
12V: See below
TBTHV:P15V
R3210
22.6K
R3211
22.6K
R3212
36.5K
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
R3213
22.6K
R3214
22.6K
Two Rs in series required by CD3210 for single-fault protection(S0,S3 only)
Thunderbolt Connector A
=PP3V3_S4_TBT
C3220
0.1UF
C3221
0.1UF
R3227
10K
R3229
100K
CRITICAL
U3220
CBTL05023
HVQFN
TBT_A_BIAS
VOLTAGE=3.3V
C3225
0.1UF
TBT_A_CIO_SEL
DP_AUXIO_EN
DP_TBTPA_AUXCH_C_N
DP_TBTPA_AUXCH_C_P
C3230
0.1UF
C3231
0.1UF
DP_TBTPA_AUXCH_N
DP_TBTPA_AUXCH_P
DP_TBTPA_DDC_DATA
DP_TBTPA_DDC_CLK
TBT_A_CONFIG1_BUF
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
C3232
0.22UF
C3233
0.22UF
DP_TBTPA_ML_P<1>
DP_TBTPA_ML_N<1>
TBT_A_LSTX
TBT_A_LSRX_UNBUF
TBT_A_DP_PWRDN
DP_TBTPA_HPD
DP_A_AUXCH_DDC_N
DP_A_AUXCH_DDC_P
TBT: RX_1 Bias Sink
TBT_A_CONFIG1_RC
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_A_HPD
CRITICAL
U3260
74AUP1T97GM
SOT886
TBT_A_LSRX
C3260
0.1UF
R3226
1M
R3228
100K
L3200
FERR-120-OHM-3A
PP3V3RHV_SW_TBTAPWR
C3200
0.01UF
C3201
0.01UF
TBTACONN_20_RC
R3201
12
C3205
0.01UF
TBTACONN_1_C
(0-18.9V)
DP Dir
TBT Dir
TBT_A_R2D_P<0>
TBT_A_R2D_N<0>
TBT: TX_0
C3270
0.22UF
C3271
0.22UF
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
R3270
470K
R3271
470K
CRITICAL
J3200
DUAL-MDP-K70
F-ANG-TH
PORT A
HPD
CONFIG1
CONFIG2
GND2
ML_LANE3P
ML_LANE3N
GND4
AUX_CHP
AUX_CHN
DP_PWR
GND0
ML_LANE0P
ML_LANE0N
GND1
ML_LANE1P
ML_LANE1N
GND3
ML_LANE2P
ML_LANE2N
RETURN
C3206
0.01UF
TBTACONN_7_C
TBT: LSX_R2P/P2R (P/N)
NOTE: Polarity Swapped for layout!
C3272
0.22UF
C3273
0.22UF
TBT_A_R2D_C_N<1>
TBT_A_R2D_C_P<1>
TBT_A_R2D_P<1>
TBT_A_R2D_N<1>
TBT: TX_1
R3272
470K
R3273
470K
470k R's for ESD protection on AC-coupled signals.
J16:514-0824 / J17:514-0831
TBT_A_D2R_N<0>
TBT_A_D2R_P<0>
C3274
0.47UF
C3275
0.47UF
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
NOTE: Polarity Swapped for layout!
R3294
1K
R3295
1K
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
C3278
0.22UF
C3279
0.22UF
DP_TBTPA_ML_P<3>
DP_TBTPA_ML_N<3>
TBT: Terminated
R3278
470K
R3279
470K
TBT_A_BIAS
R3298
2.2K
R3299
2.2K
TBT_A_D2R_N<1>
TBT_A_D2R_P<1>
C3276
0.47UF
C3277
0.47UF
TBT_A_D2R_C_P<1>
TBT_A_D2R_C_N<1>
D3298
BAR90-02LRH
D3299
BAR90-02LRH
TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N
NOTE: Polarity Swapped for layout!
CRITICAL
L3298
650NH-5%-0.430MA-0.52OHM
DP_A_AUXCH_DDC_P
DP_A_AUXCH_DDC_N
C3298
30PF
C3299
30PF
CRITICAL
L3299
650NH-5%-0.430MA-0.52OHM
TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
R3252
1M
R3251
1M
C3294
330PF
C3295
330PF
R3241
100K
C3202
0.01UF
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0596	311S0593		ALL	TI Alternate
128S0398	128S0220		ALL	3.3V INPUT CAP

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R3210,R3213		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R3211,R3214		TBTHV:P12V

Nominal Min Max
IHVS0/S3 1120mA 1090mA 1170mA (12W minimum)

SYNC_MASTER=J16_MLB_IG SYNC_DATE=05/01/2013

PAGE TITLE
Thunderbolt Connector A

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DRAWING NUMBER 051-9889 SIZE D

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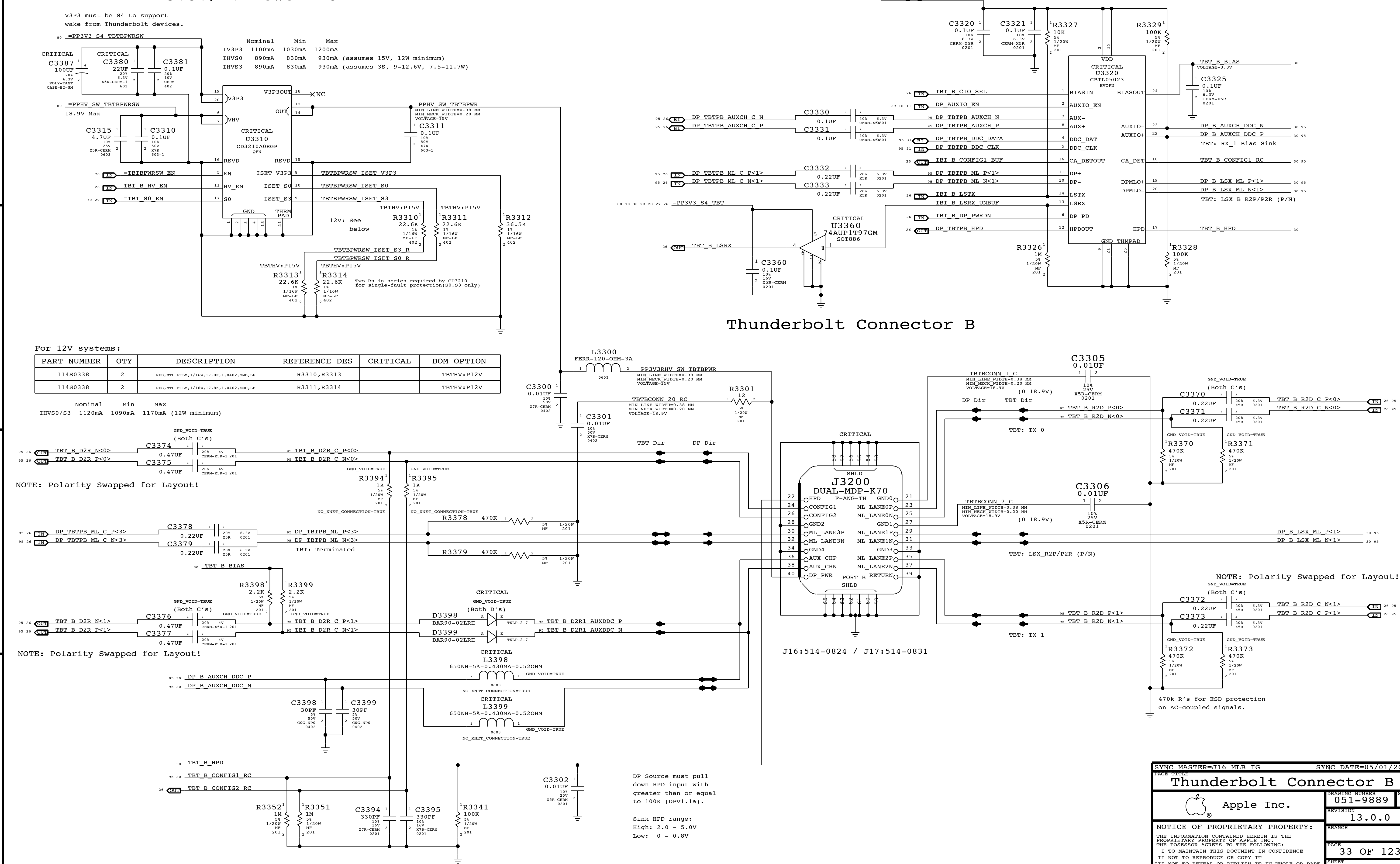
3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)



For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R3310,R3313		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R3311,R3314		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector B

SYNC_MASTER=J16_MLB_IG SYNC_DATE=05/01/2013

PAGE TITLE: Thunderbolt Connector B

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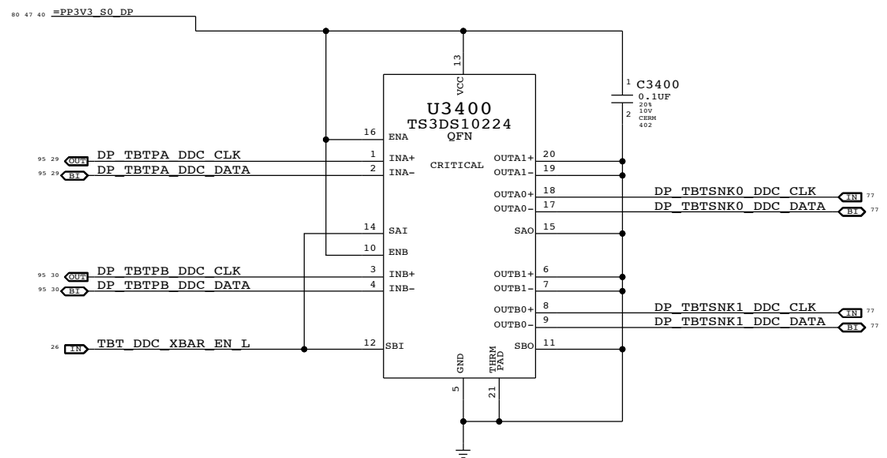
Dual-Port Host DDC Crossbar



SYNC MASTER=J16_DG SYNC DATE=04/21/2013

PAGE TITLE

TBT DDC Crossbar

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AIRPORT BLUETOOTH

AP & BT Load Switch

SWITCH	TPS22924B
CHANNEL	N-TYPE
RDS(ON)	18.4 MOHM @3.3V
LOADING	2 A (EDP)

=PP3V3_S4_AP → U3510 TPS22924 CSP (A2/B2 VIN, A1/B1 VOUT, C2 ON, GND, C1) CRITICAL
AP_PWR_EN → ON
PP3V3_S4_AP_FET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
CRITICAL L3502 FERR-220-OHM-2.5A 0603
PP3V3_S4_AP_FLT
C3502 0.1UF 10% 16V X7R-CERM 0402
C3503 0.1UF 10% 16V X7R-CERM 0402
C3504 10UF 20% 6.3V X5R 603
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

514S0335 CRITICAL
J3500 SSD-K99 F-RT-SM1

PCIE_AP_R2D_C_N → C3505 0.1UF 0201 10V X5R-CERM
PCIE_AP_R2D_C_P → C3506 0.1UF 0201 10V X5R-CERM
PLACE_NEAR=J3500.4:7mm
PLACE_NEAR=J3500.5:7mm

AP_EVENT_L
PCIE_AP_R2D_N
PCIE_AP_R2D_P
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
PCIE_AP_D2R_P
PCIE_AP_D2R_N
AP_WAKE_L
AP_RESET_CONN_L
AP_CLKREQ_Q_L
USB_BT_MUX_N
USB_BT_MUX_P

=PP3V3_G3H_BT → CRITICAL U3540 TPS22924B CSP (A2/B2 VIN, A1/B1 VOUT, C2 ON, GND, C1)
PP3V3_G3H_BT_FET
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
CRITICAL L3501 FERR-220-OHM-2.5A 0603
PP3V3_G3H_BT_FLT
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

C3507 0.1UF 10% 16V X7R-CERM 0402
C3508 10UF 20% 6.3V X5R 603

BT_RESET_MASK_L
BT_RESET_MASK_L GATES BT_PWR_RST_L
until after S0 GPIO is guranteed stable

CRITICAL Q3540 DMC2400UV SOT563 P-CHN (D, S, G)
BT_PWR_RST_L
BT_PWR_RST
R3543 10K 5% 1/16W MF-LF 402
C3541 0.01UF 20% 16V CERM 402

SMC_G3_WAKESRC_EN
R3542 10K 5% 1/16W MF-LF 402
BT_PWR_EN
Q3540 DMC2400UV SOT563 N-CHN (D, S, G)

Supervisor & CLKREQ# Isolation
Delay = 130 ms +/- 20%

PP3V3_S4_AP_FLT
=PP3V3_S4_AP
R3530 100K 1% 1/16W MF-LF 402
R3531 232K 1% 1/16W MF-LF 402
CRITICAL U3530 SLG4AP041V TDFN (VDD, SENSE, VREF, DLY, RESET*, MR*, EN, IN, OUT (OD), THRM PAD, GND)
P3V3AP_VMON
C3530 0.1uF 10% 10V CERM 402
R3532 100K 1% 1/16W MF-LF 402
AP_RESET_CONN_L → AP_RESET_L
AP_CLKREQ_Q_L → AP_CLKREQ_L
AP_PWR_EN

Wake from BT in G3H circuit

SMC_PME_S4_WAKE_L
CRITICAL Q3501 SSM3K15AMFVAPE VESM
=PP3V3_G3H_BT
C3500 0.1UF 10% 10V X5R-CERM 0201
U3501 USB3740 DFN (VDD, DP_2, DM_2, DP_1, DM_1, OE*, S, GND) CRITICAL
USB_BT_N → DP_2
USB_BT_P → DM_2
USB_BT_WAKEN → DP_1
NC → DM_1
PM_SLP_S5_L → OE*
DP → USB_BT_MUX_N
DM → USB_BT_MUX_P
R3501 15K 5% 1/20W MF 201
SIGNAL_MODEL=SWI_USB3740_DFN_USB3740_MOJO

Q3570 SSM3K15AMFVAPE VESM CRITICAL
PP3V3_S4_AP_FLT
R3570 10K 5% 1/16W MF-LF 402
PCIE_WAKE_L → AP_WAKE_L

SYNC MASTER=J16_MLB_IG	SYNC DATE=05/01/2013
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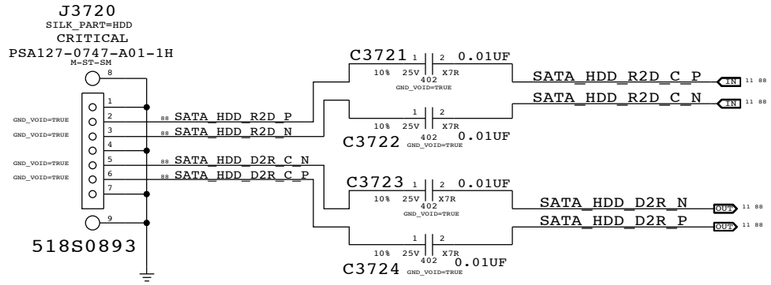
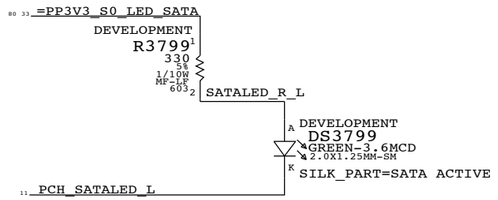
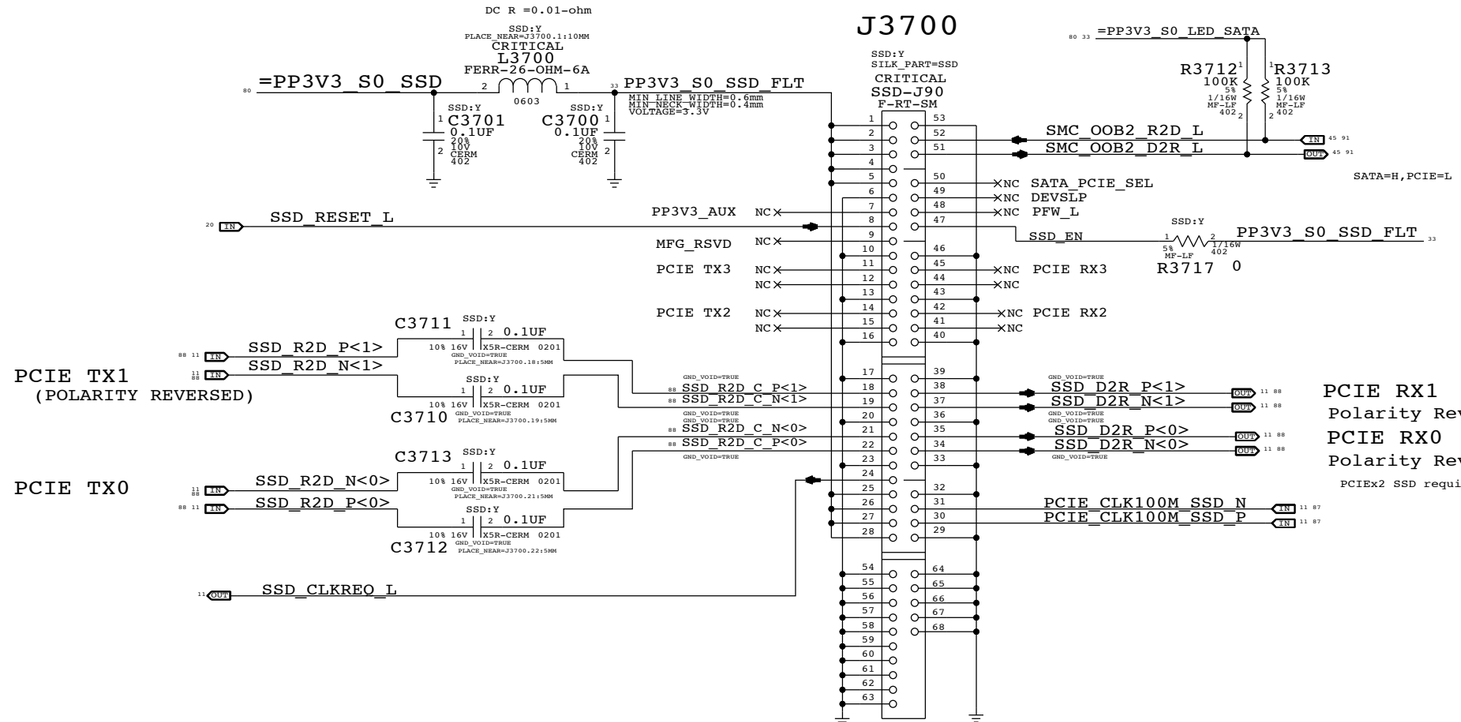
HDD SIGNAL CONNECTOR



SATA Activity LED



GS3 SSD



SYNC_MASTER=MASTER SYNC_DATE=05/01/2013

PAGE TITLE

SATA/SSD Connectors

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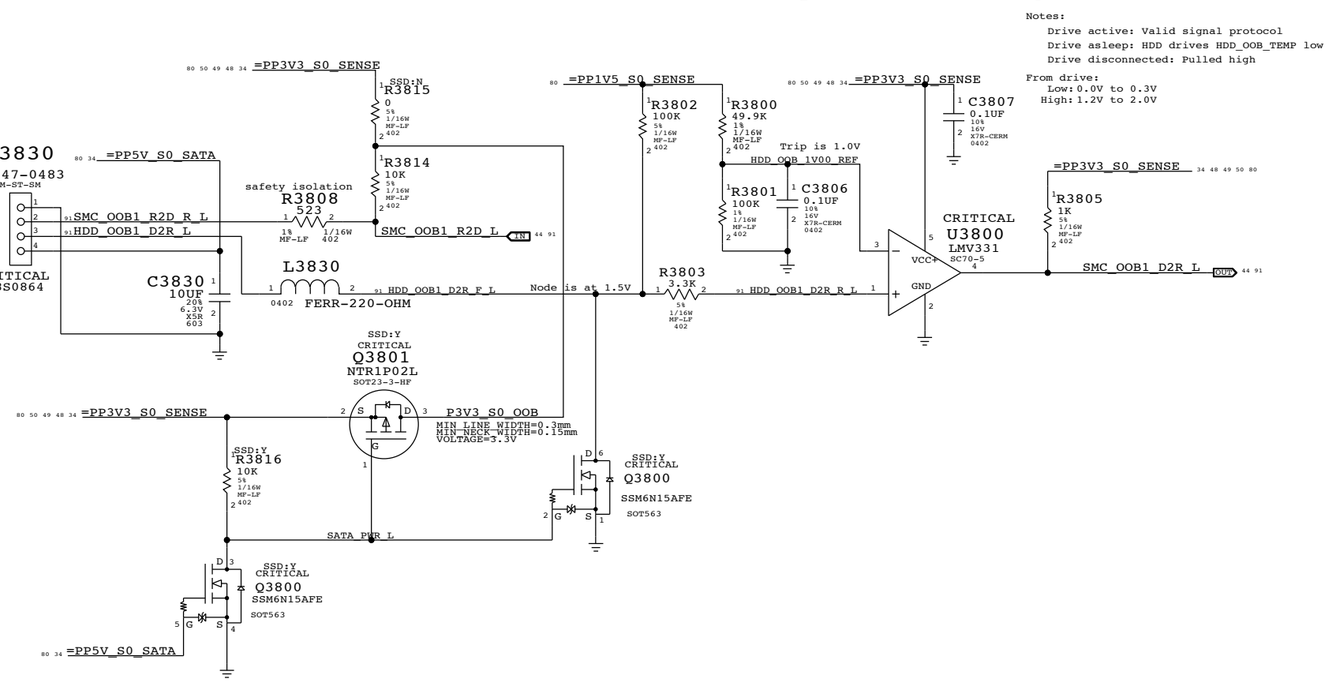
HDD POWER/OOB CONNECTOR

HDD Out-of-Band Temperature Sensing



SYNC MASTER=J16 MLB IG	SYNC DATE=05/01/2013
PAGE TITLE: HDD Connector	
Apple Inc.	DRAWING NUMBER: 051-9889 SIZE: D
	REVISION: 13.0.0
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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

80 36 35 =PP3V3_ENET_PHY

281mA (1000base-T max power, Caesar IV)

CRITICAL L3900 FERR-600-OHM-300MA-0.85OHM 0402 — MIN LINE WIDTH=0.4 mm, MIN NECK WIDTH=0.2 mm, VOLTAGE=3.3V

C3900 0.1UF 10% 16V X5R-CERM 0201

ENET_XTALVDDH — MIN LINE WIDTH=0.4 mm, MIN NECK WIDTH=0.2 mm, VOLTAGE=3.3V

CRITICAL L3905 FERR-600-OHM-300MA-0.85OHM 0402

PP3V3_ENET_PHY_BIASVDDH — MIN LINE WIDTH=0.4 mm, MIN NECK WIDTH=0.2 mm, VOLTAGE=3.3V

C3905 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L3910 FERR-600-OHM-300MA-0.85OHM 0402

PP3V3_ENET_PHY_AVDDH — MIN LINE WIDTH=0.4 mm, MIN NECK WIDTH=0.2 mm, VOLTAGE=3.3V

R3910 4.7K 5% 1/16W MF-LF 402

C3910 0.1UF 10% 16V X5R-CERM 0201

C3911 0.1UF 10% 16V X5R-CERM 0201

VDD for Card Reader I/O

36 =PP3V3R1V8_CR_VDDIO

ENET_SR_LX 36

Internal 1.2V Switching Regulator pins.

=ENET_SR_VFB 36

=PP1V2_ENET_PHY 36

396mA (1000base-T, Caesar II)

CRITICAL L3920 FERR-600-OHM-300MA-0.85OHM 0402

PP1V2_ENET_PHY_AVDDL — MIN LINE WIDTH=0.4 mm, MIN NECK WIDTH=0.2 mm, VOLTAGE=1.2V

C3921 0.1UF 10% 16V X5R-CERM 0201

C3920 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3925 FERR-600-OHM-0.5A SM

PP1V2_ENET_PHY_PCIEPLL — MIN LINE WIDTH=0.4 mm, MIN NECK WIDTH=0.2 mm, VOLTAGE=1.2V

C3926 0.1UF 10% 16V X5R-CERM 0201

C3925 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3930 FERR-600-OHM-300MA-0.85OHM 0402

PP1V2_ENET_PHY_GPHYPLL — MIN LINE WIDTH=0.4 mm, MIN NECK WIDTH=0.15 mm, VOLTAGE=1.2V

C3931 0.1UF 10% 16V X5R-CERM 0201

C3930 4.7UF 20% 6.3V X5R-CERM1 402

C3936 0.1UF 10% 16V X5R-CERM 0201

C3935 10UF 20% 6.3V X5R 603

R3940 4.7K 5% 1/16W MF-LF 402

R3941 4.7K 5% 1/16W MF-LF 402

C3915 4.7UF 20% 6.3V X5R-CERM1 402

C3916 0.1UF 10% 16V X5R-CERM 0201

AVDDH, BIASVDDH, XTALVDDH, VDDO, SR_VDD, SR_VDDP, SR_LX, SR_VFB, AVDDL, PCIE_PLLVDDL, GPHY_PLLVDDL, VDDC

80 =PP3V3_S0_ENET

R3942 1K 5% 1/16W MF-LF 402 Current Limiting Resistor

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

OMIT_TABLE

U3900 BCM57766C0KMLG QFN-8X8

C3950 0.1UF 10% 16V X5R-CERM 0201 — 87 13 OUT PCIE_ENET_D2R_N

C3951 0.1UF 10% 16V X5R-CERM 0201 — 87 13 OUT PCIE_ENET_D2R_P

C3955 0.1UF 10% 16V X5R-CERM 0201 — 87 13 IN PCIE_ENET_R2D_C_P

C3956 0.1UF 10% 16V X5R-CERM 0201 — 87 13 IN PCIE_ENET_R2D_C_N

ENET_VMAIN_PRSNT — 58 VMAIN_PRSNT (IPD-ENET)

87 PCIE_ENET_D2R_C_N — 27 PCIE_TXD_N

87 PCIE_ENET_D2R_C_P — 28 PCIE_TXD_P

87 PCIE_ENET_R2D_P — 33 PCIE_RXD_P

87 PCIE_ENET_R2D_N — 34 PCIE_RXD_N

87 11 IN PCIE_CLK100M_ENET_P — 31 PCIE_REFCLK_P

87 11 IN PCIE_CLK100M_ENET_N — 30 PCIE_REFCLK_N

37 IN ENET_RESET_L — 11 PERST* (IPD)

18 11 OUT ENET_CLKREQ_L — 12 CLKREQ* (OD)

36 OUT =ENET_WAKE_L (See note) — 3 WAKE* (OD)

37 20 IN ENET_LOW_PWR — 4 LOW_PWR (IPD)

SMB_ENET_SCL — 6 SMB_CLK

SMB_ENET_SDA — 10 SMB_DATA (IPD-ENETM)

90 35 B/I ENET_SCLK — 66 SCLK_SPD1000LED*

90 35 IN ENET_MISO — 64 SI/EEDATA

90 35 B/I ENET_MOSI — 65 SO_LINKLED*

90 35 B/I ENET_CS_L — 63 CS*/EECLK

(IPD)

NC — 2 SPD100LED*/SERIAL_DO (OD)

36 OUT ENET_TRAFFICLED_L — 67 TRAFFICLED*/SERIAL_DI (OD)

89 19 IN SYSCLK_CLK25M_ENET — 18 XTALI

NC — 19 XTALO

90 ENET_RDAC — 38 RDAC

R3965 1.24K 1% 1/16W MF-LF 402

(NO IPU OR IPD-ENET) THRM_PAD 69

NOTE: "IPx" == Programmable pull-up/down

SD_DETECT can only be used active low due to errata.

(IPD) GPIO_0/CR_ACT_LED* 5 — NC

GPIO_1/LR_OUT 8

GPIO_2/MEDIA_SENSE 9 — ENET_MEDIA_SENSE — OUT 11 90

(IPx-ENET) SD_DETECT 1 — ENET_SD_DETECT_L — IN 37 90

(IPU-ENET) CR_CMD 26 — 90 ENET_SD_CMD — R3961 33 — SDCONN_CMD — IN 37 90

CR_CLK 21 — 90 ENET_SD_CLK — R3979 33 — SDCONN_CLK — OUT 37 90

(IPU-ENET) CR_DATA0 25 — 90 ENET_CR_DATA<0> — R3971 33 — SDCONN_DATA<0> — B/I 37 90

CR_DATA1 24 — 90 ENET_CR_DATA<1> — R3972 33 — SDCONN_DATA<1> — B/I 37 90

CR_DATA2 23 — 90 ENET_CR_DATA<2> — R3973 33 — SDCONN_DATA<2> — B/I 37 90

CR_DATA3 22 — 90 ENET_CR_DATA<3> — R3974 33 — SDCONN_DATA<3> — B/I 37 90

CR_DATA4 52 — 90 ENET_CR_DATA<4> — R3975 33 — SDCONN_DATA<4> — B/I 37 90

CR_DATA5 53 — 90 ENET_CR_DATA<5> — R3976 33 — SDCONN_DATA<5> — B/I 37 90

CR_DATA6 54 — 90 ENET_CR_DATA<6> — R3977 33 — SDCONN_DATA<6> — B/I 37 90

CR_DATA7 55 — 90 ENET_CR_DATA<7> — R3978 33 — SDCONN_DATA<7> — B/I 37 90

All 33 ohm resistors: 5% 1/20W MF 201

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

(IPU-ENET) MS_INS* 59 — NC

(IPU-ENET) CR_LED*/CR_BUS_PWR 60 — ENET_CR_PWREN — OUT 37

(IPU-ENET) CR_WP* 57 — SDCONN_WP — IN 37

(NO IPU OR IPD-ENET) SR_DISABLE 68 — ENET_SR_DISABLE — R3981 1K 5% 1/16W MF-LF 402 (See note)

ENET 1.2V SR IS ENABLED IF FLOATING.

ENET supports both active-levels for WP.

PP3V3R1V8_ENET_LR_OUT 36 — MIN LINE WIDTH=0.4 mm, MIN NECK WIDTH=0.15 mm, VOLTAGE=3.3V

ENETCONN_MDI_P<0> — TRD0_P 40 — B/I 36 90

ENETCONN_MDI_N<0> — TRD0_N 41 — B/I 36 90

ENETCONN_MDI_P<1> — TRD1_P 44 — B/I 36 90

ENETCONN_MDI_N<1> — TRD1_N 43 — B/I 36 90

ENETCONN_MDI_P<2> — TRD2_P 46 — B/I 36 90

ENETCONN_MDI_N<2> — TRD2_N 47 — B/I 36 90

ENETCONN_MDI_P<3> — TRD3_P 50 — B/I 36 90

ENETCONN_MDI_N<3> — TRD3_N 49 — B/I 36 90

ENET_CR Signals

BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE

If ENET switching regulator is used, this pin should have a 1K pull-down to GND

PLACEMENT_NOTE=PLACE R3961 NEAR U3900
PLACEMENT_NOTE=PLACE R3979 NEAR U3900
PLACEMENT_NOTE=PLACE R3971 NEAR U3900
PLACEMENT_NOTE=PLACE R3972 NEAR U3900
PLACEMENT_NOTE=PLACE R3973 NEAR U3900
PLACEMENT_NOTE=PLACE R3974 NEAR U3900
PLACEMENT_NOTE=PLACE R3975 NEAR U3900
PLACEMENT_NOTE=PLACE R3976 NEAR U3900
PLACEMENT_NOTE=PLACE R3977 NEAR U3900
PLACEMENT_NOTE=PLACE R3978 NEAR U3900

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EFI to program at startup. (Required ROM size 1 Mbit)

80 36 35 =PP3V3_ENET_PHY

C3990 0.1UF 10% 16V X5R-CERM 0201

U3990 AT45DB011D SOIC-8S1 OMIT_TABLE

VCC 5, SCK 2, CS* 4, WP* 5, RESET* 3, GND 7, SI 1, SO 8

90 35 IN ENET_SCLK

90 35 IN ENET_CS_L

ENET_MOSI — IN 35 90

ENET_MISO — OUT 35 90

NOSTUFF R3990 4.7K 5% 1/16W MF-LF 402

R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=J16_MLB_IG SYNC_DATE=05/01/2013

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CAESAR IV 1.2V INT.VR CMPTS

80 36 35 =PP3V3_ENET_PHY

Power decoupling

C4010 4.7UF 20% 6.3V X5R-CERM1 402

C4011 0.1UF 10% 16V X7R-CERM 0402

35 ENET_SR_LX

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.2V
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL
L4010 4.7UH-0.8A
PCAA031B-SM

C4012 10UF 20% 6.3V X5R 603

C4013 0.1UF 10% 16V X7R-CERM 0402

PP1V2_ENET_INTREG 16

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.2V

Feedback loop

36 PP1V2_ENET_INTREG

MAKE_BASE=TRUE

=PP1V2_ENET_PHY 35

=ENET_SR_VFB 35

ENET Enable Generation

"ENET" = "S0" || ("S4" && "WOL_EN")

3.3V ENET FET

80 =PP3V3_S4_FET_ENET

CRITICAL
Q4020
NTR4101P
SOT-23-HF

PP3V3_ENET_FET 80

R4020 10K 5% 1/16W MF-LF 402

C4020 0.033UF 10% 16V X5R 402

R4021 100K 5% 1/16W MF-LF 402

C4021 0.01UF 10% 50V X7R-CERM 0402

PM_EN_ENET_L

P3V3ENET_SS

CRITICAL
Q4021
2N7002DW-X-G
SOT-363

14 IN WOL_EN

CRITICAL
Q4021
2N7002DW-X-G
SOT-363

71 70 45 44 21 12 IN PM_SLP_S3_L

CAESAR IV ACTIVITY LED

80 36 35 =PP3V3_ENET_PHY

DEVELOPMENT
R4050 330 5% 1/16W MF-LF 402

ENET_ACT

DEVELOPMENT
LED4050
GREEN-3.6MCD 2.0X1.25MM-SM
SILKSCREEN:ENET ACT

35 ENET_TRAFFICLED_L

CAESAR IV WAKE# ISOLATION

=PP3V3_ENET_PHY 35 36 80

Q4070
SSM3K15AMFVAPE
VESM

R4070 10K 5% 1/16W MF-LF 402

32 12 PCIE_WAKE_L

ENET_WAKE_L
MAKE_BASE=TRUE

=ENET_WAKE_L 35

PP3V3R1V8_ENET_LR_OUT 35

MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.15 mm

=PP3V3R1V8_CR_VDDIO 35

C4030 4.7UF 20% 6.3V X5R-CERM 402

C4031 0.1UF 10% 16V X5R-CERM 0201

C4032 0.1UF 10% 16V X5R-CERM 0201

157S0058
CRITICAL
T4000
SM

90 35 ENETCONN_MDI_P<1> — 1 — 12 — ENETCONN_MDI_T_P<1> 36 90

90 35 ENETCONN_MDI_N<1> — 2 — 11 — ENETCONN_MDI_T_N<1> 36 90

3 — 10 ENETCONN_MCT1

TX →

LFE8904CF

4 — 9 ENETCONN_MCT3

90 35 ENETCONN_MDI_P<3> — 5 — 8 — ENETCONN_MDI_T_P<3> 36 90

90 35 ENETCONN_MDI_N<3> — 6 — 7 — ENETCONN_MDI_T_N<3> 36 90

← RX

CRITICAL
T4010
SM

90 35 ENETCONN_MDI_N<2> — 1 — 12 — ENETCONN_MDI_T_N<2> 36 90

90 35 ENETCONN_MDI_P<2> — 2 — 11 — ENETCONN_MDI_T_P<2> 36 90

3 — 10 ENETCONN_MCT2

TX →

LFE8904CF

4 — 9 ENETCONN_MCT0

90 35 ENETCONN_MDI_N<0> — 5 — 8 — ENETCONN_MDI_T_N<0> 36 90

90 35 ENETCONN_MDI_P<0> — 6 — 7 — ENETCONN_MDI_T_P<0> 36 90

← RX

ENETCONN_TCT

C4001 0.1UF 20% 10V CERM 402

C4002 0.1UF 20% 10V CERM 402

C4003 0.1UF 20% 10V CERM 402

C4004 0.1UF 20% 10V CERM 402

R4000 75 5% 1/16W MF-LF 402

R4001 75 5% 1/16W MF-LF 402

R4002 75 5% 1/16W MF-LF 402

R4003 75 5% 1/16W MF-LF 402

90 ENETCONN_MCT_BS

MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm

NOSTUFF
C4000 1000PF 10% 2KV CERM 1206

514-0822
CRITICAL
J4000
K70-K72
F-ANG-TH

ENET_MDI

90 36 ENETCONN_MDI_T_N<3> — 8 — ENET_MDI_TRAN3-

90 36 ENETCONN_MDI_T_P<3> — 7 — ENET_MDI_TRAN3+

90 36 ENETCONN_MDI_T_N<1> — 6 — ENET_MDI_TRAN1-

90 36 ENETCONN_MDI_T_N<2> — 5 — ENET_MDI_TRAN2-

90 36 ENETCONN_MDI_T_P<2> — 4 — ENET_MDI_TRAN2+

90 36 ENETCONN_MDI_T_P<1> — 3 — ENET_MDI_TRAN1+

90 36 ENETCONN_MDI_T_N<0> — 2 — ENET_MDI_TRAN0-

90 36 ENETCONN_MDI_T_P<0> — 1 — ENET_MDI_TRAN0+

9 10 11 12 13 14 — SHIELD PINS

SYNC MASTER=J16_MLB_IG SYNC DATE=05/01/2013

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Ethernet Support & Connector

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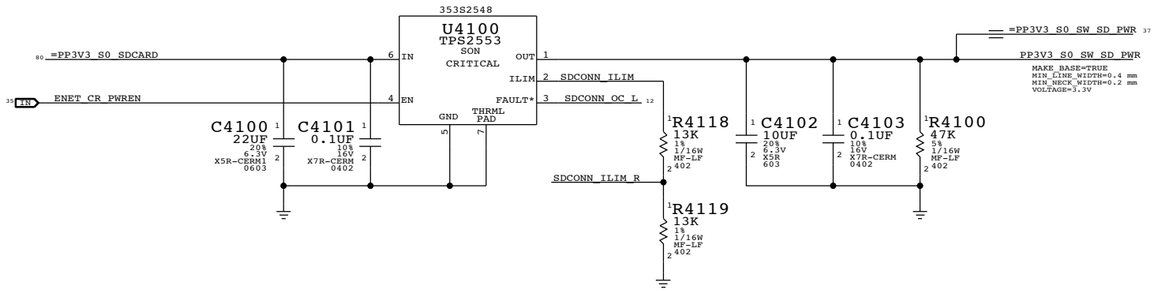
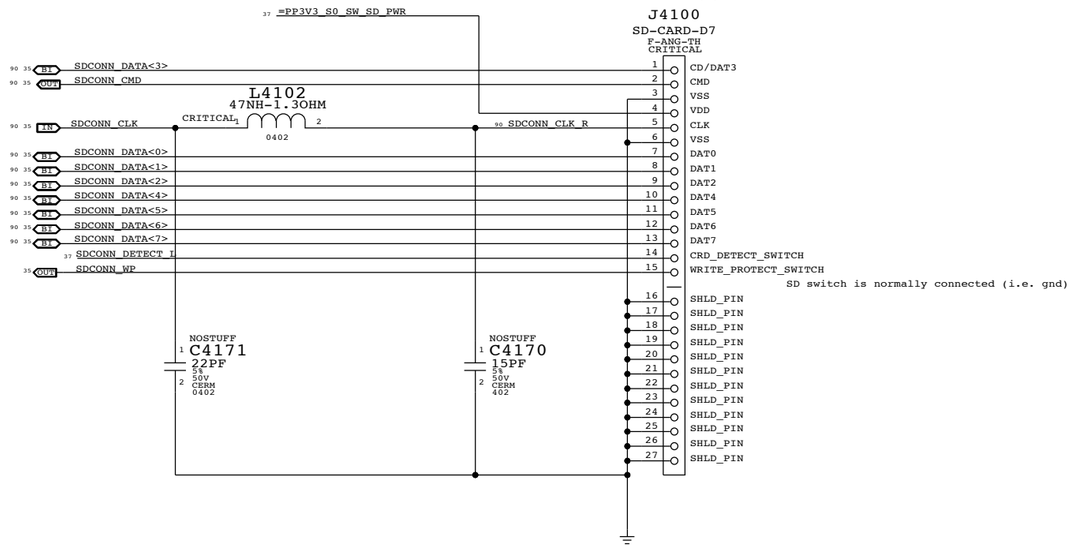
SD CARD 3.3V OVERCURRENT PROTECTION CHIP

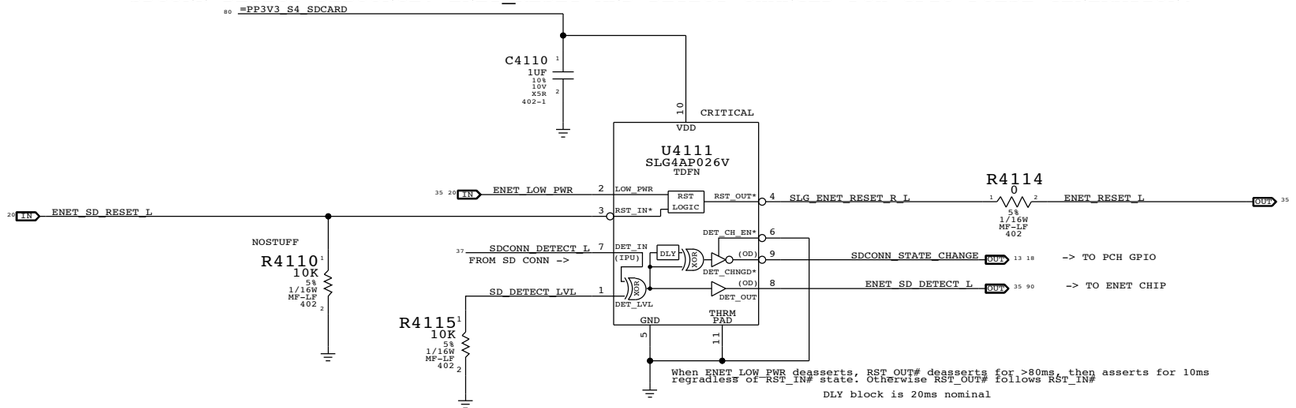


J16:516-0249 / J17:512-0038

SD CARD CONNECTOR



SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



SYNC MASTER=J16 MLB IG SYNC DATE=05/01/2013

PAGE TITLE

SD READER CONNECTOR

Apple Inc.

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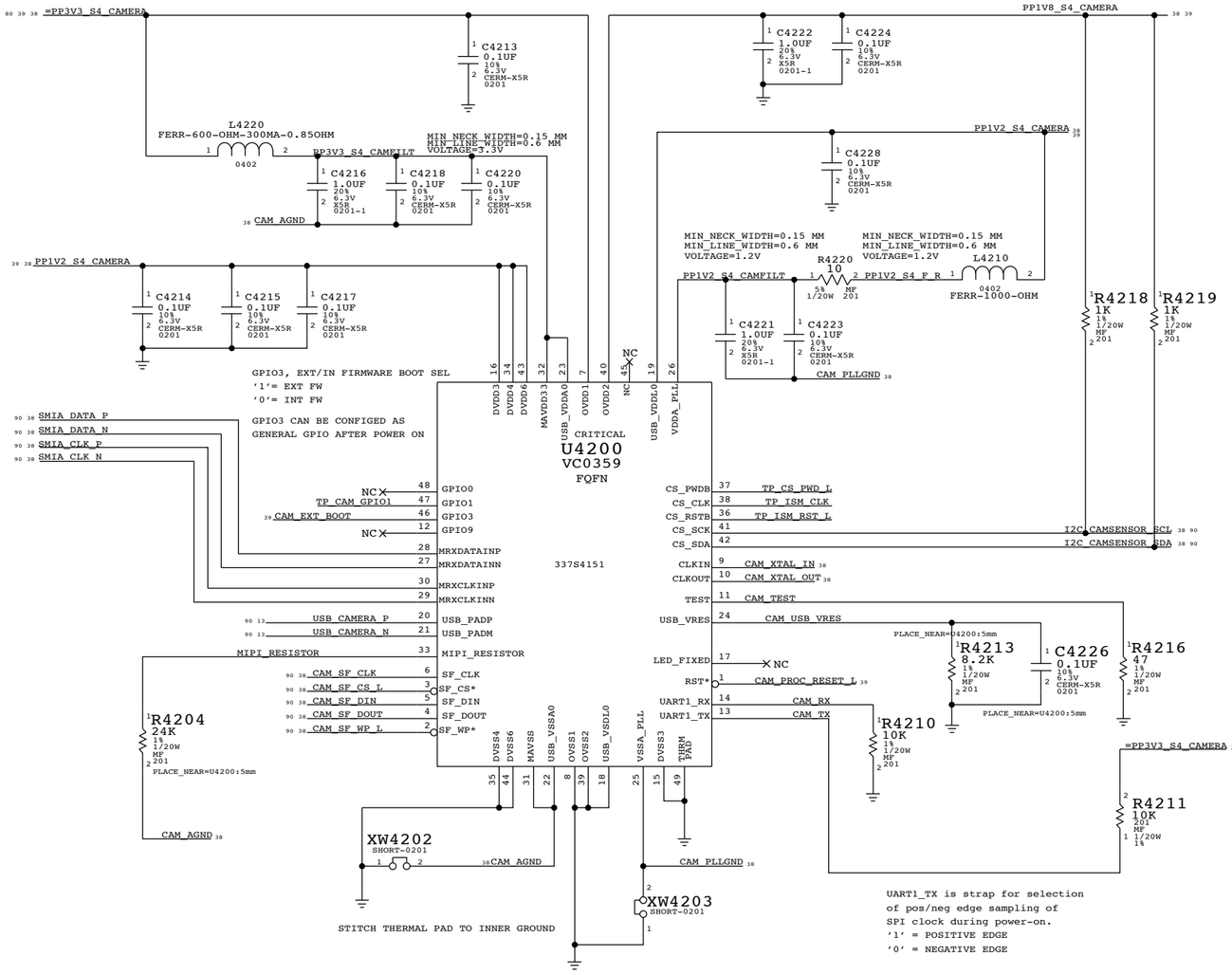
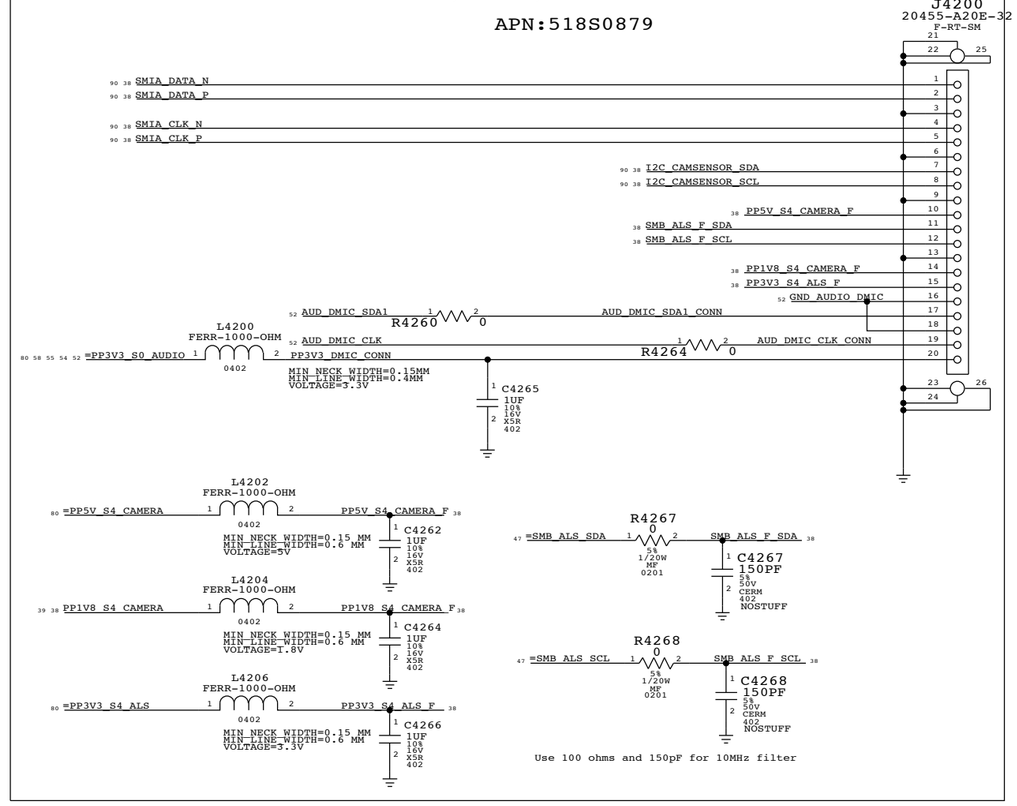
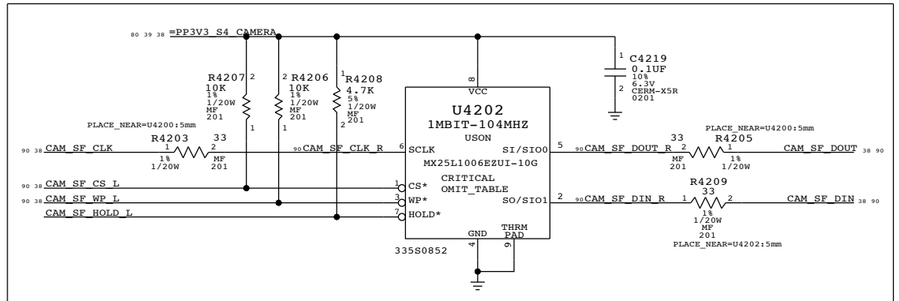
USB CAMERA CONTROLLER



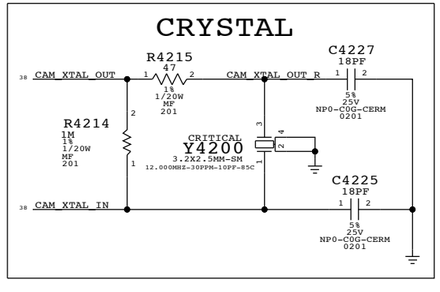
Camera/ALS/DMIC connector

APN:518S0879





SERIAL FLASH



SYNC_MASTER=J16_MLB_IG SYNC_DATE=05/01/2013

PAGE TITLE: Camera Controller

Apple Inc.

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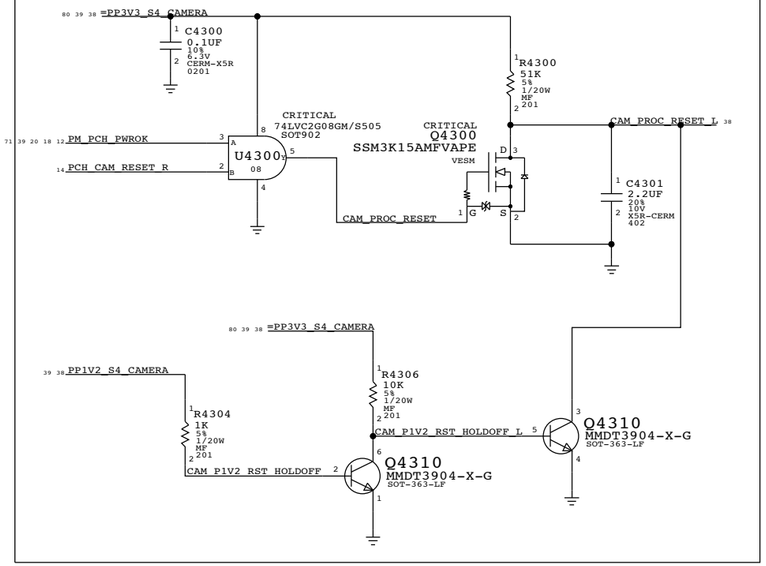
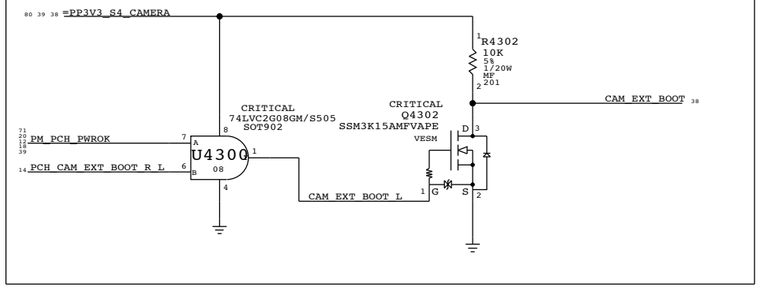
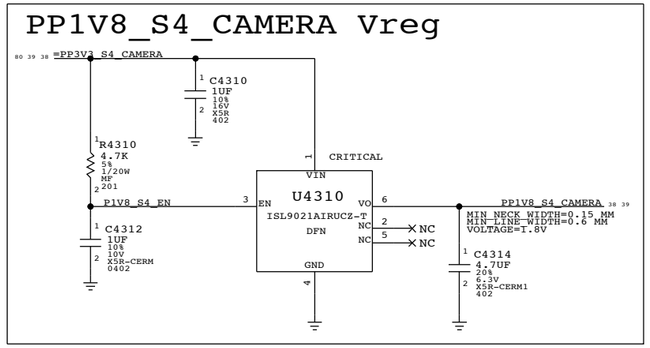
Camera Processor Reset



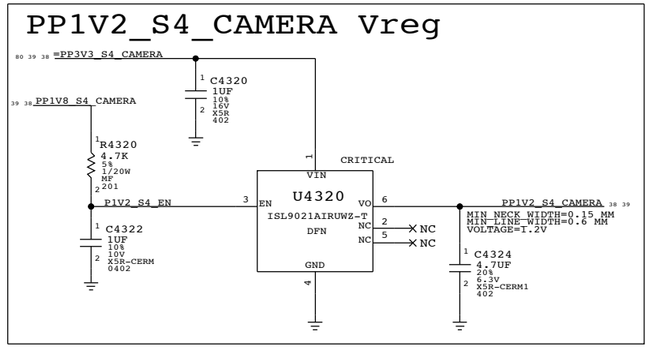
Camera Processor ExtBoot Cntl



PP1V8_S4_CAMERA Vreg



PP1V2_S4_CAMERA Vreg



SYNC_MASTER=J16_MLB_IG SYNC_DATE=05/01/2013

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Internal DP Connector

518S0829

CRITICAL

J4400
20525-130E-01
F-RT-SM

80 =PP12V_S0_LCD — F4400 3AMP-32V-467 (603-HF) — PP12V_LCD_F — L4400 FERR-220-OHM (0805) — PP12V_LCD
VOLTAGE=12V, MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.1 mm

C4420 10UF 10% 16V X5R-CERM 0805

C4401 0.001UF 20% 50V CERM 0402

Display TCon Master	91 47	BI	SMB_DP_TCON_SDA
	91 47	OUT	SMB_DP_TCON_SCL
Display TCon Slave	47	BI	SMB_DP_TCON_SLA_SDA
	47	IN	SMB_DP_TCON_SLA_SCL
	95 52	OUT	DP_INT_SPDIF_AUDIO
	43	OUT	DP_INTPNL_HPD
	95 41	BI	DP_INTPNL_AUX_N
	95 41	BI	DP_INTPNL_AUX_P
	95 41	IN	DP_INTPNL_ML_P<0>
	95 41	IN	DP_INTPNL_ML_N<0>
	95 41	IN	DP_INTPNL_ML_P<1>
	95 41	IN	DP_INTPNL_ML_N<1>
	40		VIDEO_ON
	68	OUT	BKLT_VSYNC

Backlight Control

Delay applies only on a L->H transition on VIDEO_ON. This guarantees video is valid before the backlight is enabled.
On a H->L transition, output follows with standard logic propagation delay. This ensures the backlight is off immediately after loss of video

80 47 31 =PP3V3_S0_DP

C4450 0.1UF 10% 6.3V CERM-X5R 0201

U4450 74AUP2G14GM SOT886

40 VIDEO_ON

R4451 100K 5% 1/20W MF 201

D4450 SOD-523 BAT54XV2T1

R4450 30.1K 1% 1/20W MF 201

VIDEO_ON_L_DLY

C4451 10UF 20% 6.3V CERM-X5R 0402-1

U4450 74AUP2G14GM SOT886

BKLT_EN OUT 68
TO BLC

VIDEO_ON_L OUT 3
To Diag LED

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TP to DP aliases

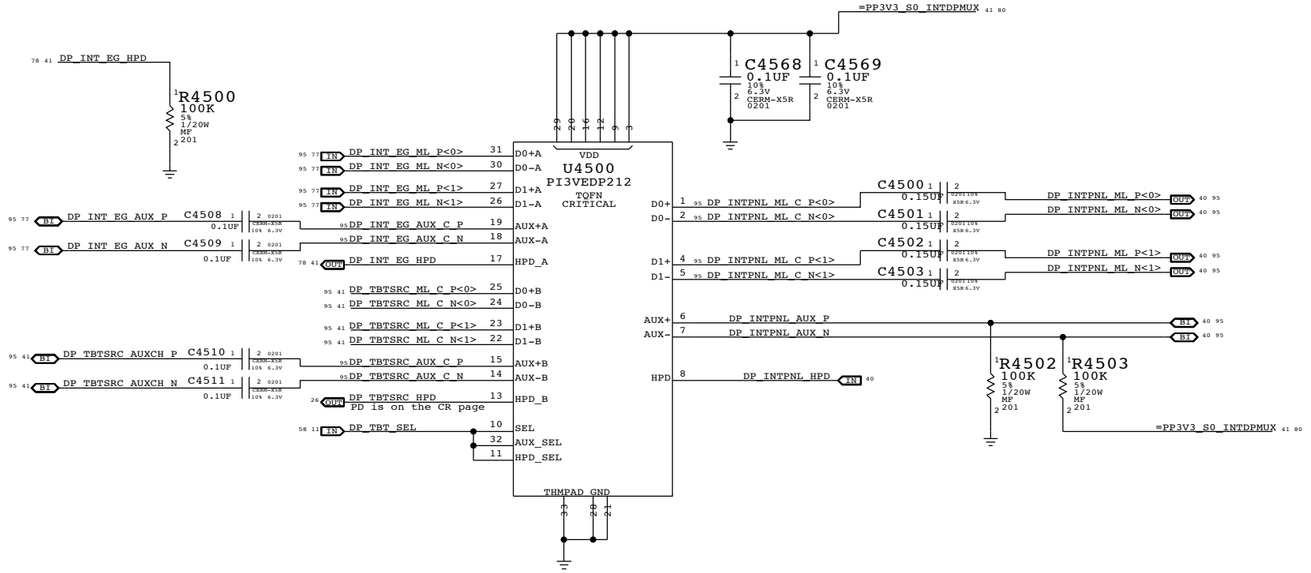
26 IN	TP_DP_TBTSRC_ML_CP<0>	DP_TBTSRC_ML_P<0>	41 95
26 IN	TP_DP_TBTSRC_ML_CN<0>	DP_TBTSRC_ML_N<0>	41 95
26 IN	TP_DP_TBTSRC_ML_CP<1>	DP_TBTSRC_ML_P<1>	41 95
26 IN	TP_DP_TBTSRC_ML_CN<1>	DP_TBTSRC_ML_N<1>	41 95
26 BI	TP_DP_TBTSRC_AUXCH_CP	DP_TBTSRC_AUXCH_P	41 95
26 BI	TP_DP_TBTSRC_AUXCH_CN	DP_TBTSRC_AUXCH_N	41 95

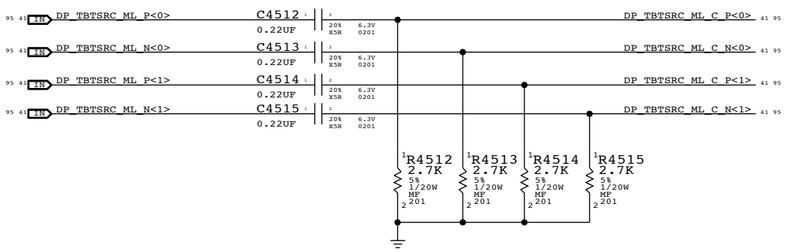
MAKE_BASE=TRUE

NC aliases

26 IN	TP_DP_TBTSRC_ML_CP<2>	NC_DP_TBTSRC_ML_P<2>
26 IN	TP_DP_TBTSRC_ML_CN<2>	NC_DP_TBTSRC_ML_N<2>
26 IN	TP_DP_TBTSRC_ML_CP<3>	NC_DP_TBTSRC_ML_P<3>
26 IN	TP_DP_TBTSRC_ML_CN<3>	NC_DP_TBTSRC_ML_N<3>
77 IN	DP_INT_EG_ML_P<2>	NC_DP_INT_EG_ML_P<2>
77 IN	DP_INT_EG_ML_N<2>	NC_DP_INT_EG_ML_N<2>
77 IN	DP_INT_EG_ML_P<3>	NC_DP_INT_EG_ML_P<3>
77 IN	DP_INT_EG_ML_N<3>	NC_DP_INT_EG_ML_N<3>

NO_TEST=TRUE MAKE_BASE=TRUE





SYNC_MASTER=J16_DG SYNC_DATE=04/21/2013

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Internal DP MUXing

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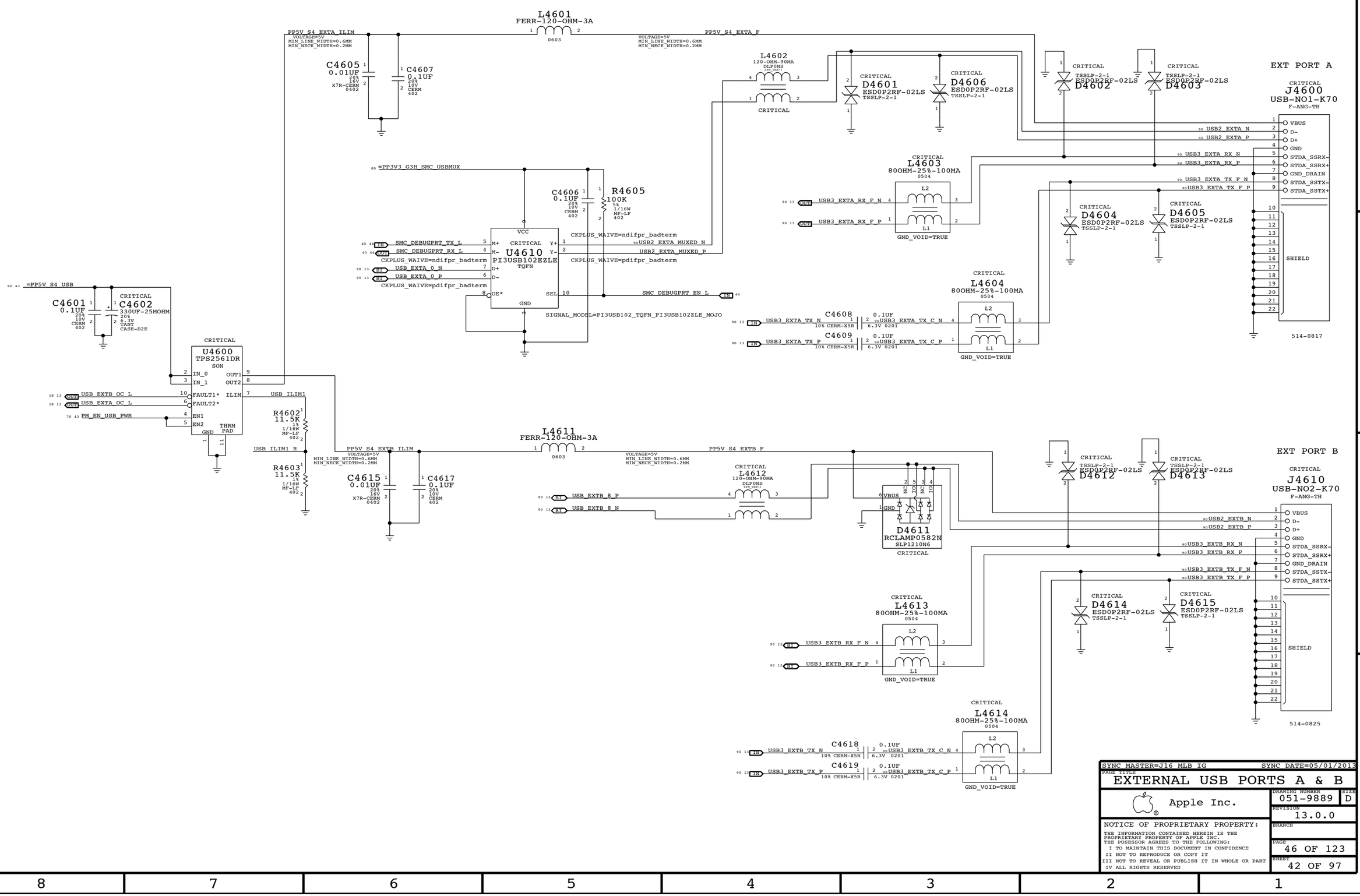
L4601
FERR-120-OHM-3A
0603
PP5V_S4_EXTA_ILIM
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
PP5V_S4_EXTA_F
C4605
0.01UF
20%
16V
X7R-CERM
0402
C4607
0.1UF
20%
10V
CERM
402
L4602
120-OHM-90MA
DLP0NS
CRITICAL
D4601
ESD0P2RF-02LS
TSSLP-2-1
D4606
ESD0P2RF-02LS
TSSLP-2-1
D4602
ESD0P2RF-02LS
TSSLP-2-1
D4603
ESD0P2RF-02LS
TSSLP-2-1
EXT PORT A
J4600
USB-NO1-K70
F-ANG-TH
VBUS
D-
D+
GND
STDA_SSRX-
STDA_SSRX+
GND_DRAIN
STDA_SSTX-
STDA_SSTX+
SHIELD
514-0817
=PP3V3_G3H_SMC_USBMUX
C4606
0.1UF
R4605
100K
5%
1/16W
MF-LF
U4610
PI3USB102EZLE
TQFN
SMC_DEBUGPRT_TX_L
SMC_DEBUGPRT_RX_L
USB_EXTA_O_N
USB_EXTA_O_P
CKPLUS_WAIVE=ndifpr_badterm
CKPLUS_WAIVE=pdifpr_badterm
USB2_EXTA_MUXED_N
USB2_EXTA_MUXED_P
SMC_DEBUGPRT_EN_L
SIGNAL_MODEL=PI3USB102_TQFN_PI3USB102ZLE_MOJO
L4603
80OHM-25%-100MA
0504
L4604
80OHM-25%-100MA
0504
D4604
ESD0P2RF-02LS
TSSLP-2-1
D4605
ESD0P2RF-02LS
TSSLP-2-1
USB3_EXTA_RX_F_N
USB3_EXTA_RX_F_P
GND_VOID=TRUE
C4608
0.1UF
10% CERM-X5R
6.3V 0201
C4609
0.1UF
10% CERM-X5R
6.3V 0201
USB3_EXTA_TX_N
USB3_EXTA_TX_P
USB3_EXTA_TX_C_N
USB3_EXTA_TX_C_P
=PP5V_S4_USB
C4601
0.1UF
C4602
330UF-25MOHM
6.3V
TANT
CASE-D2E
U4600
TPS2561DR
SON
IN_0
IN_1
OUT1
OUT2
FAULT1*
FAULT2*
ILIM
EN1
EN2
GND
THRM PAD
USB_EXTB_OC_L
USB_EXTA_OC_L
PM_EN_USB_PWR
USB_ILIM1
R4602
11.5K
1%
1/16W
MF-LF
402
R4603
11.5K
USB_ILIM1_R
L4611
FERR-120-OHM-3A
0603
PP5V_S4_EXTB_ILIM
PP5V_S4_EXTB_F
C4615
0.01UF
C4617
0.1UF
L4612
120-OHM-90MA
D4611
RCLAMP0582N
SLP1210N6
D4612
ESD0P2RF-02LS
TSSLP-2-1
D4613
ESD0P2RF-02LS
TSSLP-2-1
EXT PORT B
J4610
USB-NO2-K70
F-ANG-TH
SHIELD
514-0825
USB_EXTB_8_P
USB_EXTB_8_N
L4613
80OHM-25%-100MA
0504
L4614
80OHM-25%-100MA
0504
D4614
ESD0P2RF-02LS
TSSLP-2-1
D4615
ESD0P2RF-02LS
TSSLP-2-1
USB3_EXTB_RX_F_N
USB3_EXTB_RX_F_P
GND_VOID=TRUE
C4618
0.1UF
10% CERM-X5R
6.3V 0201
C4619
0.1UF
10% CERM-X5R
6.3V 0201
USB3_EXTB_TX_N
USB3_EXTB_TX_P
USB3_EXTB_TX_C_N
USB3_EXTB_TX_C_P
SYNC_MASTER=J16_MLB_IG
SYNC_DATE=05/01/2013
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EXTERNAL USB PORTS A & B
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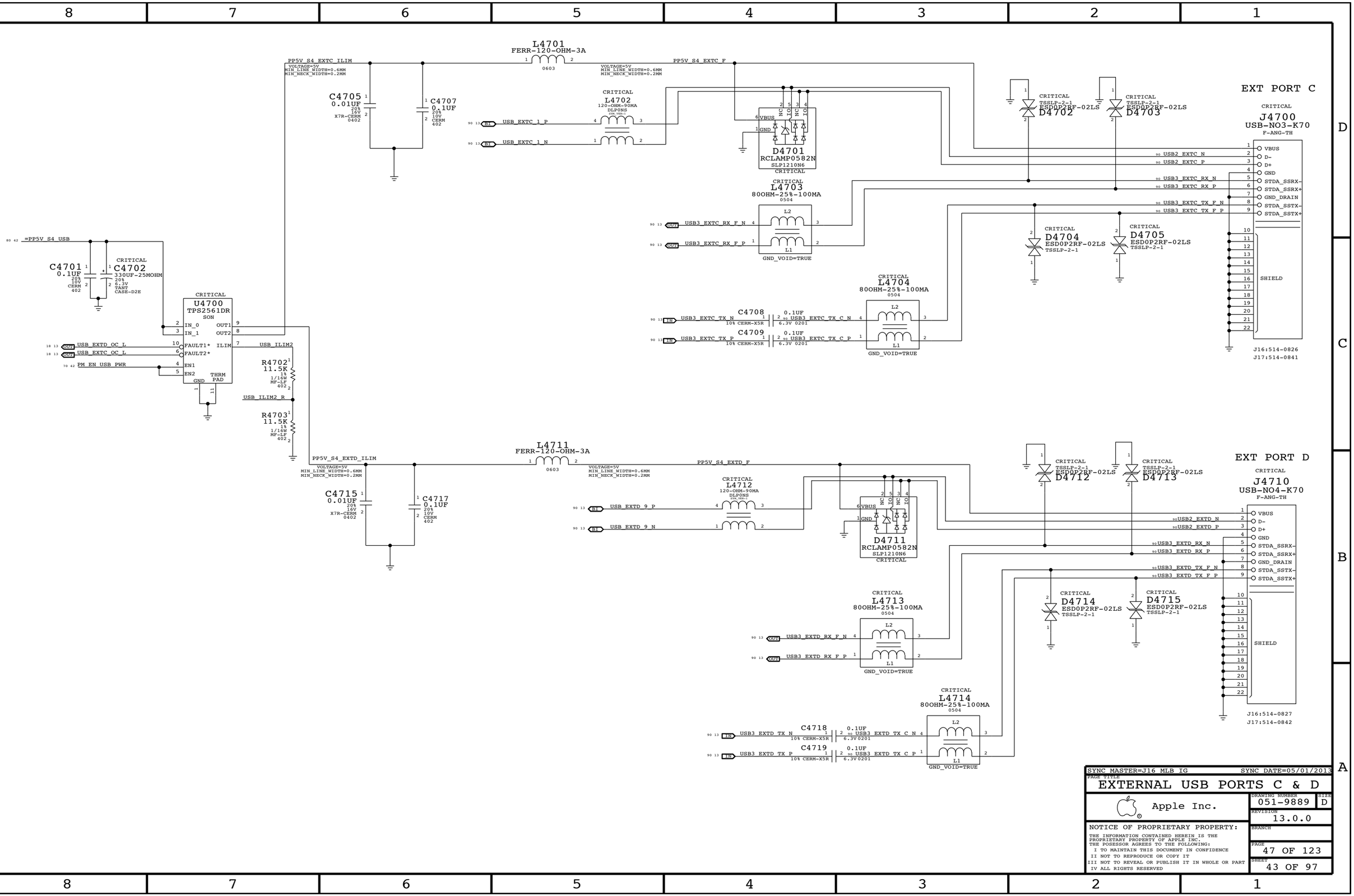

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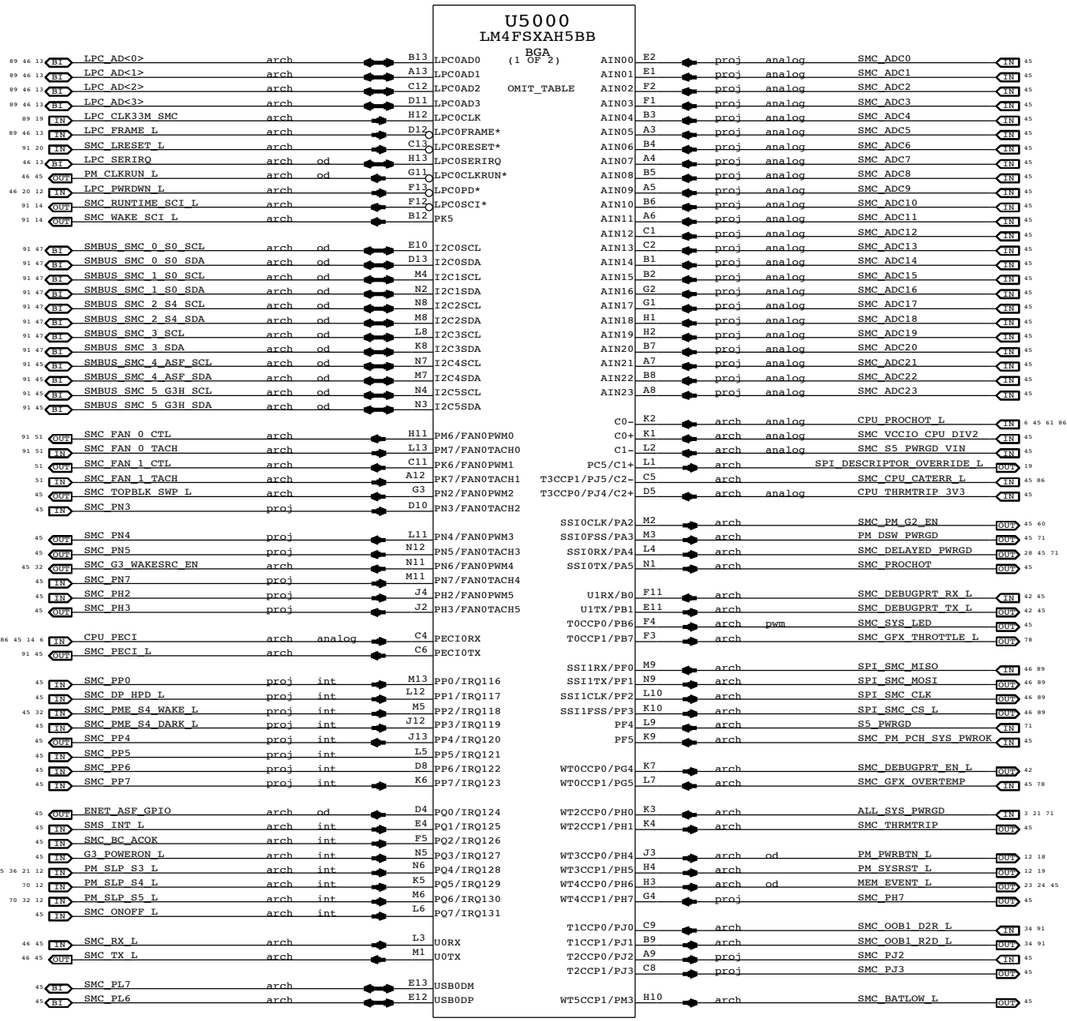
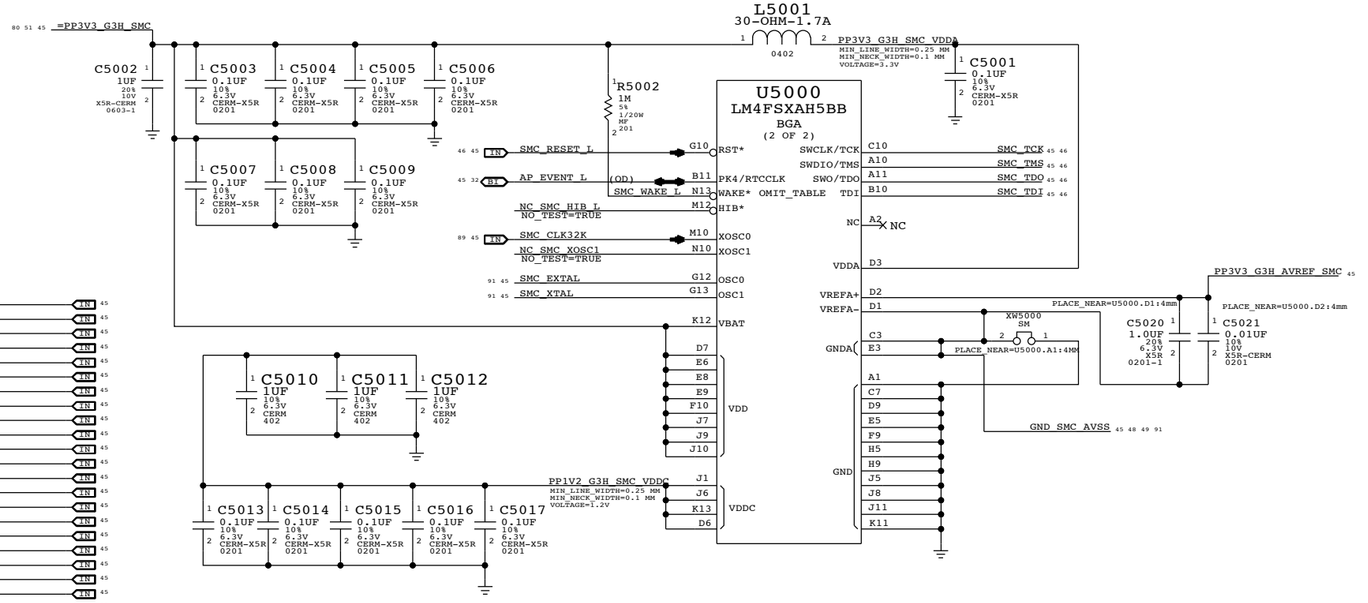
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





SYNC_MASTER=J16_MLB_IG	SYNC_DATE=05/01/2013
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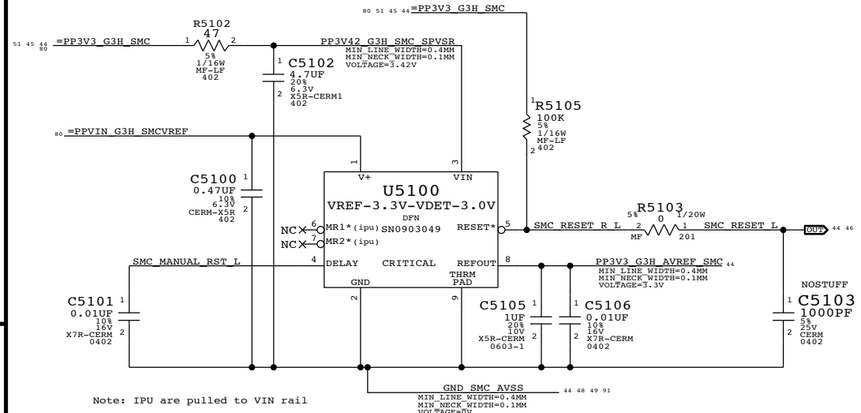
SMC Supervisor and AVREF Supply



Note: IPU are pulled to VIN rail

ADC Channel Aliases

SMC_ADC0	VSNS_P12VG3H	MAKE_BASE=TRUE
SMC_ADC1	ISNS_P12VG3H	MAKE_BASE=TRUE
SMC_ADC2	VSNS_P12VS0_GPUCORE	MAKE_BASE=TRUE
SMC_ADC3	ISNS_P12VS0_GPUCORE	MAKE_BASE=TRUE
SMC_ADC4	VSNS_P1V5S0	MAKE_BASE=TRUE
SMC_ADC5	ISNS_P1V5S0	MAKE_BASE=TRUE
SMC_ADC6	VSNS_VDDQS3_DDR	MAKE_BASE=TRUE
SMC_ADC7	ISNS_VDDQS3_DDR	MAKE_BASE=TRUE
SMC_ADC8	VSNS_P12VS0_FBVDDQ	MAKE_BASE=TRUE
SMC_ADC9	ISNS_P12VS0_FBVDDQ	MAKE_BASE=TRUE
SMC_ADC10	VSNS_CPUVCC	MAKE_BASE=TRUE
SMC_ADC11	ISNS_CPUVCC	MAKE_BASE=TRUE
SMC_ADC12	VSNS_GPUCORE_ALT	MAKE_BASE=TRUE
SMC_ADC13	ISNS_GPUCORE_ALT	MAKE_BASE=TRUE
SMC_ADC14	VSNS_HDDS0	MAKE_BASE=TRUE
SMC_ADC15	ISNS_HDDS0	MAKE_BASE=TRUE
SMC_ADC17	VSNS_P1V05S0_PCH	MAKE_BASE=TRUE
SMC_ADC20	ISNS_SSDS0	MAKE_BASE=TRUE
SMC_ADC21	VSNS_P3V3S5	MAKE_BASE=TRUE

Unused ADC Channels

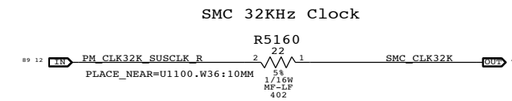
SMC_PH3	NC_SMC_PH3	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC16	NC_SMC_ADC16	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC18	NC_SMC_ADC18	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC19	NC_SMC_ADC19	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC22	NC_SMC_ADC22	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC23	NC_SMC_ADC23	MAKE_BASE=TRUE NO_TEST=TRUE

Unused Project-specific

SMC_S5_PWRGD_VIN	NC_SMC_S5_PWRGD_VIN	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PL7	NC_SMC_PL7	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PN3	NC_SMC_PN3	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PN4	NC_SMC_PN4	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PP4	NC_SMC_S4_WAKESRC_EN	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PN7	NC_SMC_PN7	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PP5	NC_SMC_PP5	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PP6	NC_SMC_PP6	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PP7	NC_SMC_PP7	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_DP_HPD_L	NC_SMC_DP_HPD_L	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PME_S4_DARK_L	NC_SMC_PME_S4_DARK_L	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PH7	TP_SMC_PH7	MAKE_BASE=TRUE NO_TEST=TRUE
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	MAKE_BASE=TRUE NO_TEST=TRUE
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	MAKE_BASE=TRUE NO_TEST=TRUE
SMBUS_SMC_5_G3H_SCL	NC_SMBUS_SMC_5_G3H_SCL	MAKE_BASE=TRUE NO_TEST=TRUE
SMBUS_SMC_5_G3H_SDA	NC_SMBUS_SMC_5_G3H_SDA	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_BATLOW_L	NC_SMC_BATLOW_L	MAKE_BASE=TRUE NO_TEST=TRUE

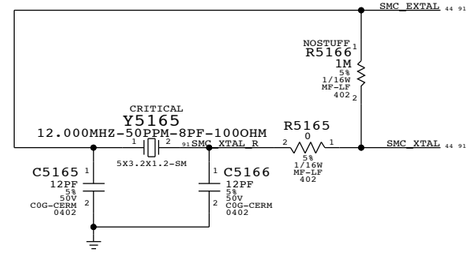
TP for access if ZPB re-intstated

SMC 32KHz Clock

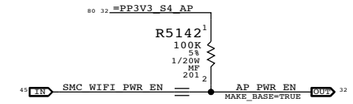


SMC Crystal

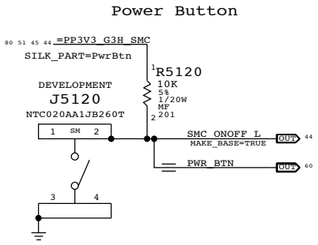
NOTE: SMC team wants 12MHz for this Xtal



SMC control for AirPort power

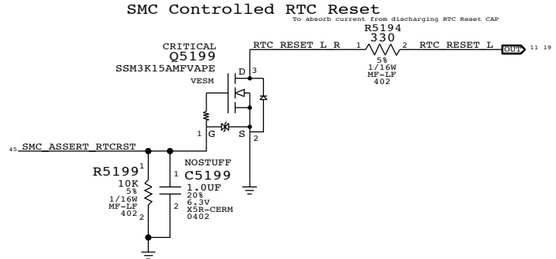


Power Button



SMC Controlled RTC Reset

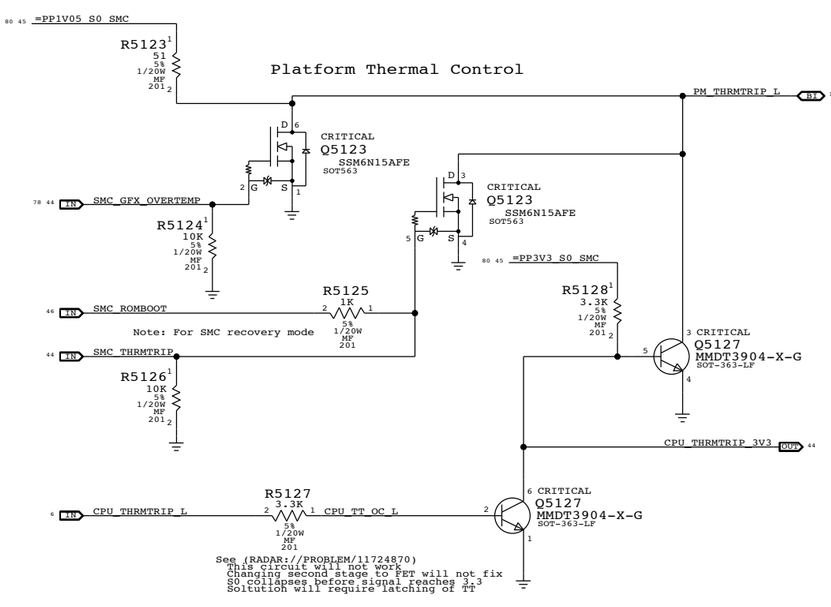
To absorb current from discharging RTC Reset CAP



Project-specific Aliases

SMC_PN5	ACDC_BURST_EN_L	MAKE_BASE=TRUE
SMC_PJ3	SMC_OOB2_R2D_L	MAKE_BASE=TRUE
SMC_PJ2	SMC_OOB2_D2R_L	MAKE_BASE=TRUE
SMC_PP0	SMC_ACDC_ID	MAKE_BASE=TRUE
SMC_PH2	SMC_ASSERT_RTCRST	MAKE_BASE=TRUE
SMC_PL6	SMC_WIFI_PWR_EN	MAKE_BASE=TRUE

Platform Thermal Control



See (RADAR://PROBLEM/11724870)
This circuit will not work
Changing second stage to FET will not fix
S0 collapses before signal reaches 3.3
Soltution will require latching of TT

Arch Pull Up/Down

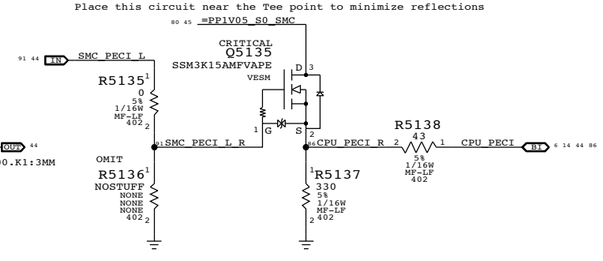
MEM_EVENT_L	R5170	10K	=PP3V3_S0_SMC	1/20W MF 201
PM_CLKRUN_L	R5171	10K	=PP3V3_S0_SMC	1/20W MF 201
ENET_ASF_GPIO	R5175	10K	=PP3V3_G3H_SMC	1/20W MF 201
G3_POWERON_L	R5176	10K	=PP3V3_G3H_SMC	1/20W MF 201
SMC_BC_ACOK	R5178	100K	=PP3V3_G3H_SMC	1/20W MF 201
SMC_SYS_LED NOSTUFF	R5179	100K	=PP3V3_G3H_SMC	1/20W MF 201
SMS_INT_L	R5180	10K	=PP3V3_G3H_SMC	1/20W MF 201
SMC_PME_S4_WAKE_L	R5181	10K	=PP3V3_G3H_SMC	1/20W MF 201
AP_EVENT_L	R5185	10K	PP3V3_S4_AP_FET	1/20W MF 201
SMC_G3_WAKESRC_EN	R5118	100K	PP3V3_S4_AP_FET	1/20W MF 201
SMC_DELAYED_PWRGD	R5186	100K	=PP3V3_G3H_SMC	1/16W MF-LF 402
PM_DSW_PWRGD	R5184	100K	=PP3V3_G3H_SMC	1/16W MF-LF 402
SMC_PM_G2_EN	R5187	100K	=PP3V3_G3H_SMC	1/20W MF 201

Serial/JTAG Interface Pull-ups

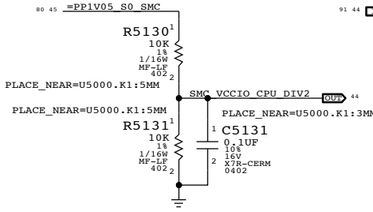
SMC_TX_L	R5190	10K	=PP3V3_G3H_SMC	1/20W MF 201
SMC_RX_L	R5191	100K	=PP3V3_G3H_SMC	1/20W MF 201
SMC_TCK	R5195	10K	=PP3V3_G3H_SMC	1/20W MF 201
SMC_TDI	R5196	10K	=PP3V3_G3H_SMC	1/20W MF 201
SMC_TDO	R5197	10K	=PP3V3_G3H_SMC	1/20W MF 201
SMC_TMS	R5198	10K	=PP3V3_G3H_SMC	1/20W MF 201
SMC_DEBUGPRT_TX_L	R5192	20K	=PP3V3_G3H_SMC	1/20W MF 201
SMC_DEBUGPRT_RX_L	R5193	20K	=PP3V3_G3H_SMC	1/20W MF 201

PECI Support

Level-shifter that allows SMC to drive PECI
Place this circuit near the Tee point to minimize reflections

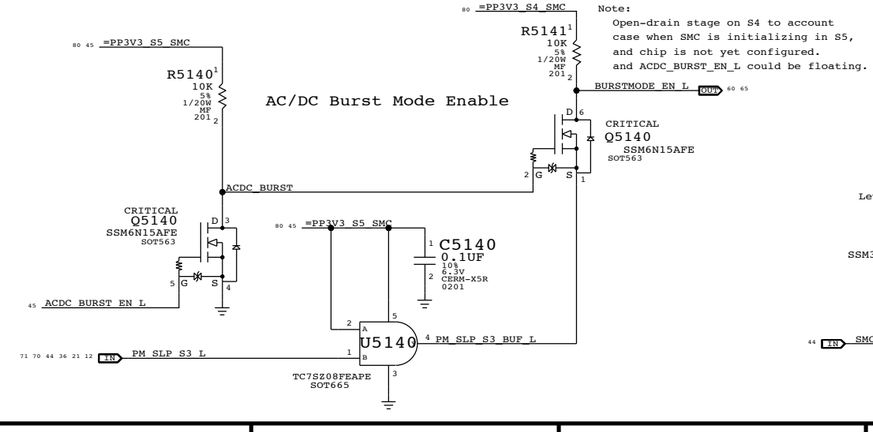


Comparator Reference



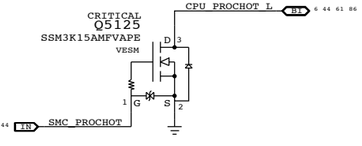
AC/DC Burst Mode Enable

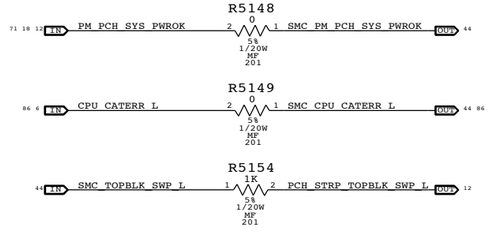
Note:
Open-drain stage on S4 to account
case when SMC is initializing in S5,
and chip is not yet configured.
and ACDC_BURST_EN_L could be floating.



PROCHOT Support

Level-shifter that allows SMC to drive PROCHOT





SYNC_MASTER=J16_TONY	SYNC_DATE=06/11/2013
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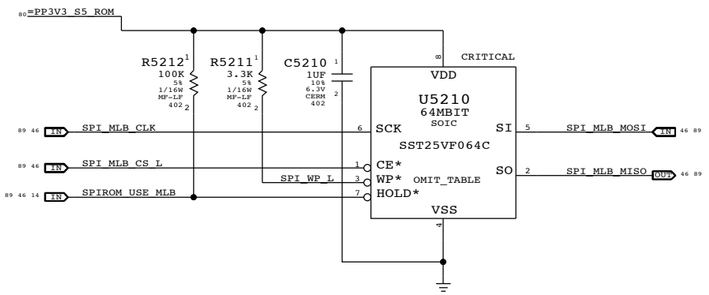
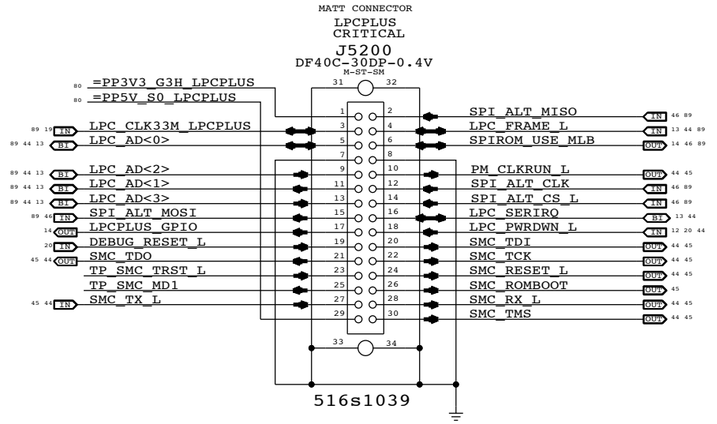
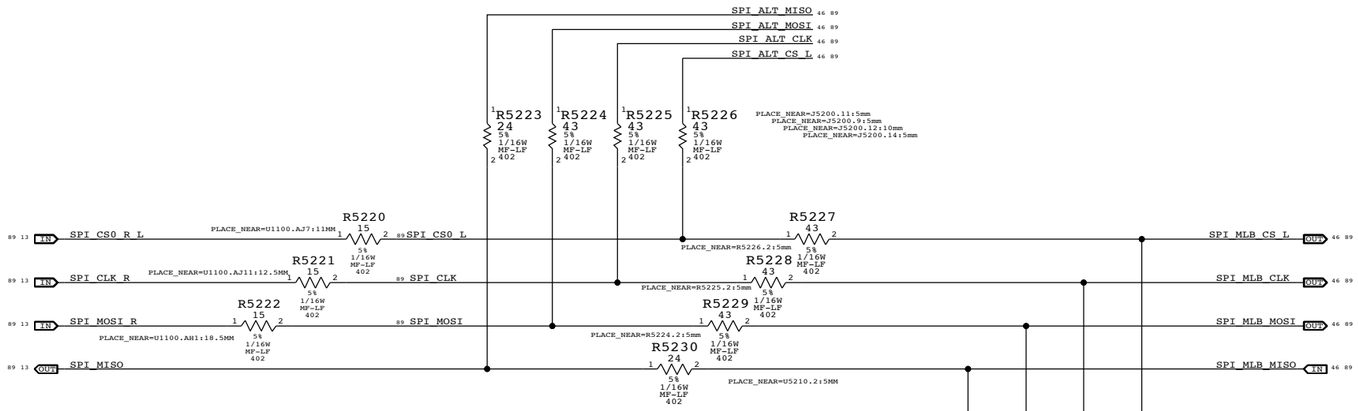
SPI BootROM



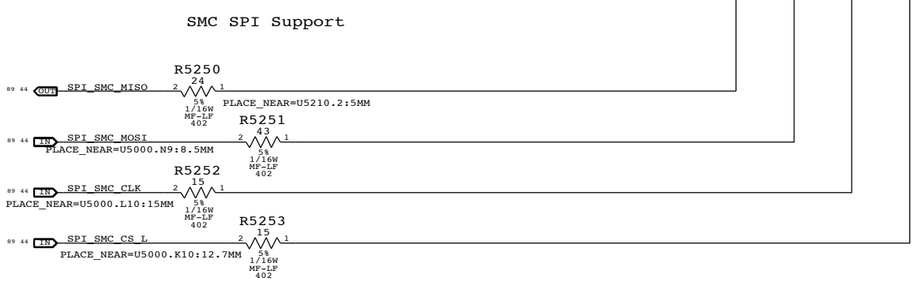
LPC+SPI Connector



SPI Series Termination



SMC SPI Support



SYNC MASTER=J16 TONY SYNC DATE=06/17/2013

PAGE TITLE
SPI and Debug Connector

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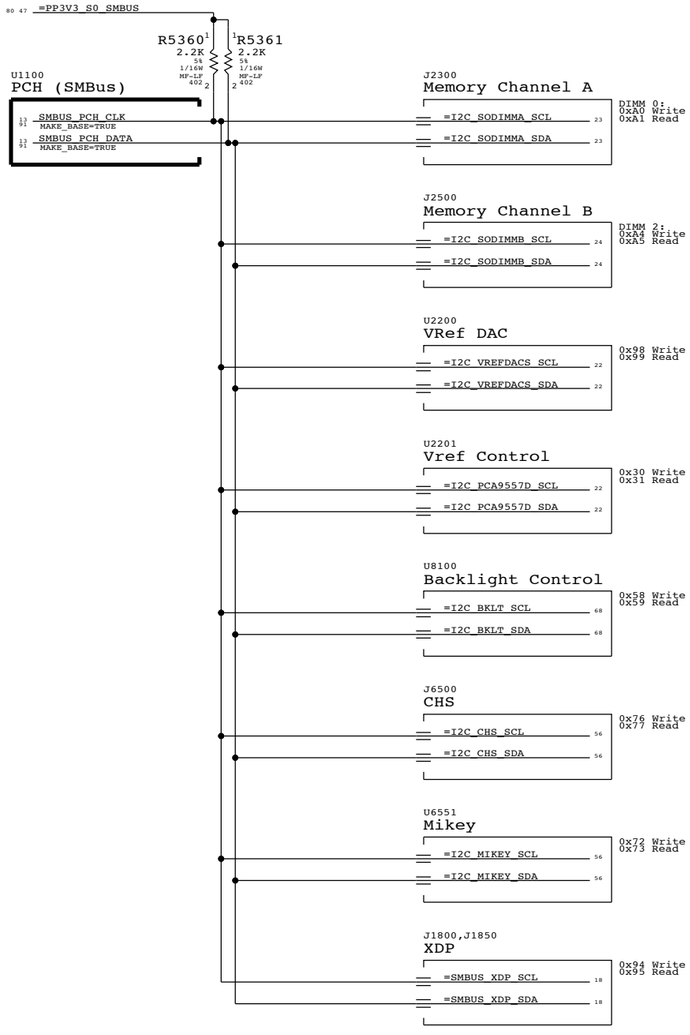
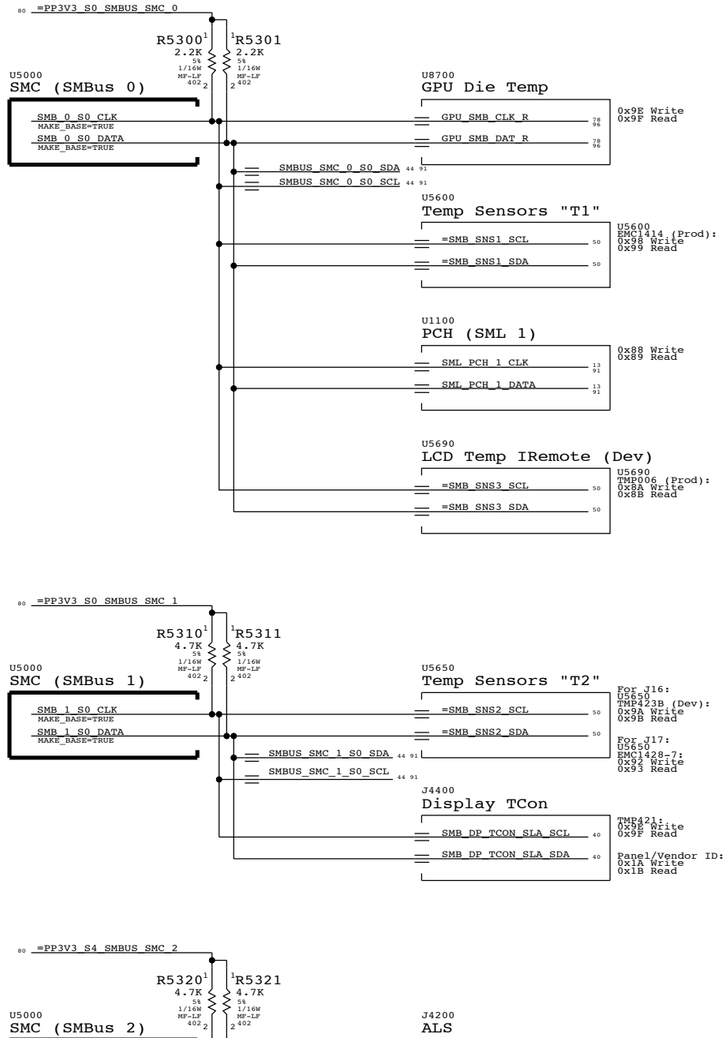
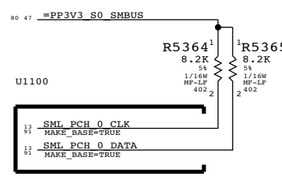
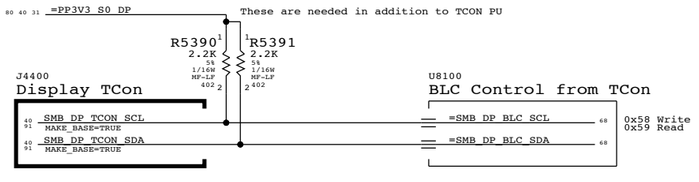




SMC multi-master experiment



Unused PCH SM Link



Line Legend
- Master
- Slave
- Mux

SYNC_MASTER=J16_DG SYNC_DATE=04/21/2013

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SMBus Connections

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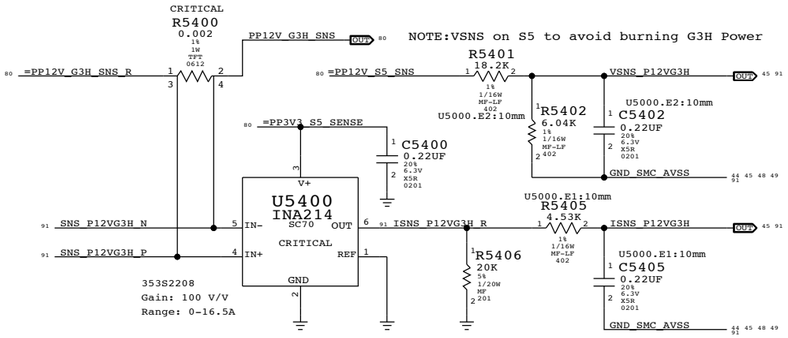
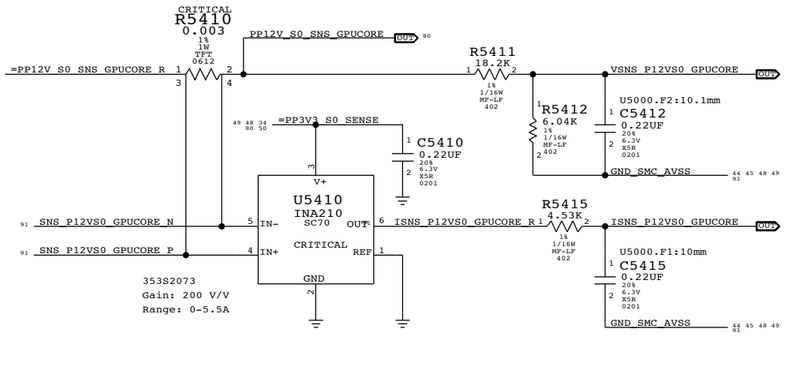
12V G3H (VD2R:ADC0/ID2R:ADC1) AC/DC lowside sense (System total)

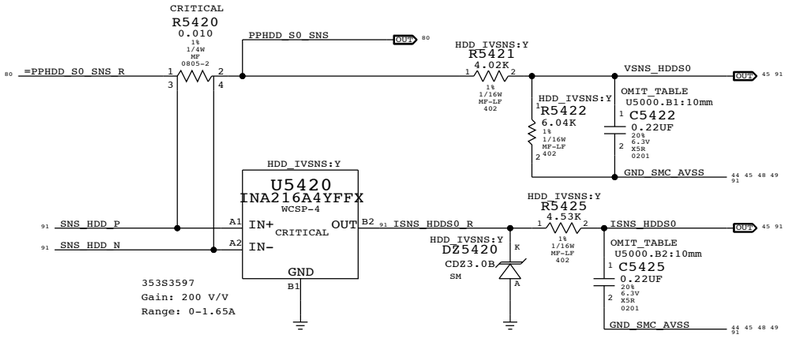


GPU Core (VG1C:ADC2/IG1C:ADC3) GPU highside sense for GPU Core Regulator



HDD S0 (VH05:ADC14/IH05:ADC15)

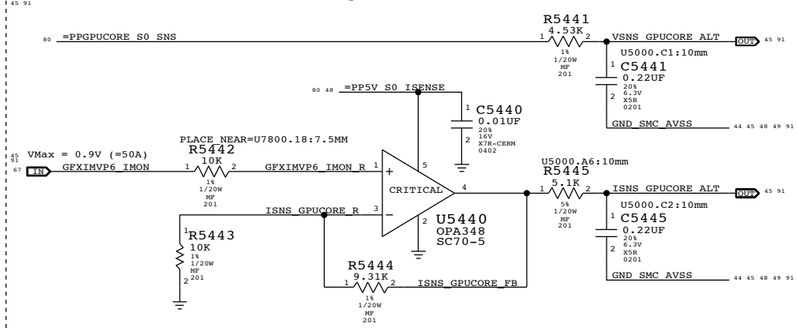
I/V-sense for HDD (Development, but need R5420)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
1328O304	2	CAP,0.22UF,201	C5422,C5425	HDD_IVSNS:Y
1178O002	2	RES,0 OHM,201	C5422,C5425	HDD_IVSNS:N

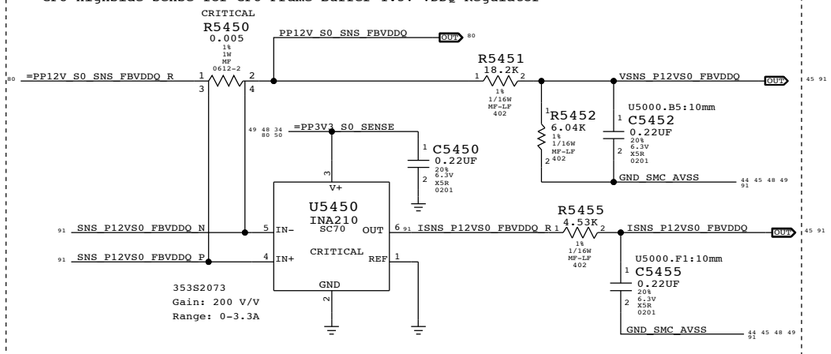
GPU Core - Alt (VG0C:ADC12/IG0C:ADC13)

Alternate low side V-sense and IMON amp



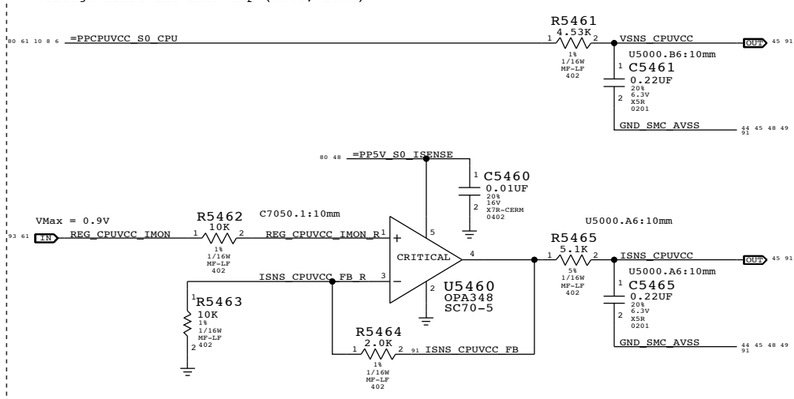
GPU FB (VG0F:ADC8/IG0F:ADC9)

GPU highside sense for GPU Frame Buffer 1.5V VDDQ Regulator



CPU Core (VC0C:ADC10/IC0C:ADC11)

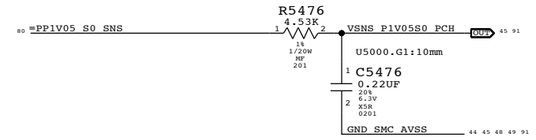
Voltage sense and IMON amp (VC0C, IC0C)



PP1V05_S0_PCH (VN1R:ADC17)

I/V-sense for PP1V05_S0_PCH

Since PP1V05 Vreg feedback is coming
from near GPU, place this sensor near PCH.



SYNC_MASTER=J16 TONY	SYNC_DATE=06/11/2013
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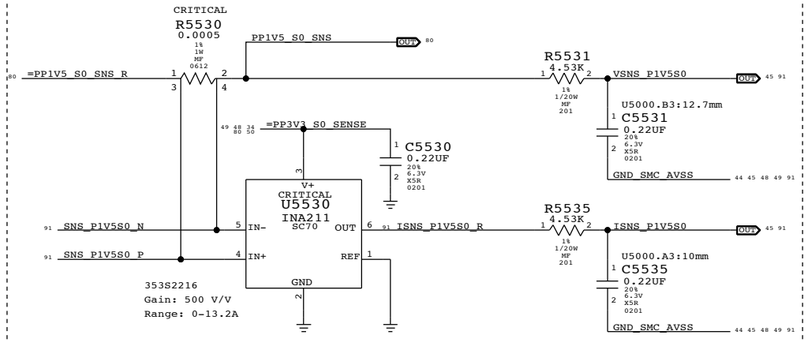
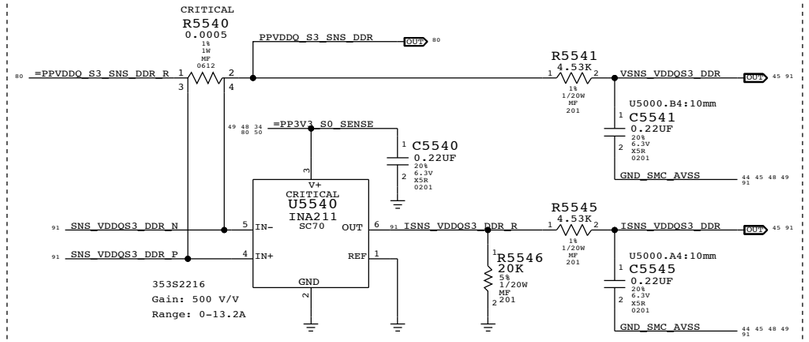
PP1V5_S0 (VC0M:ADC4/IC0M:ADC5)

lowside sense for VCCVRM,PCH,CPU mem, audio

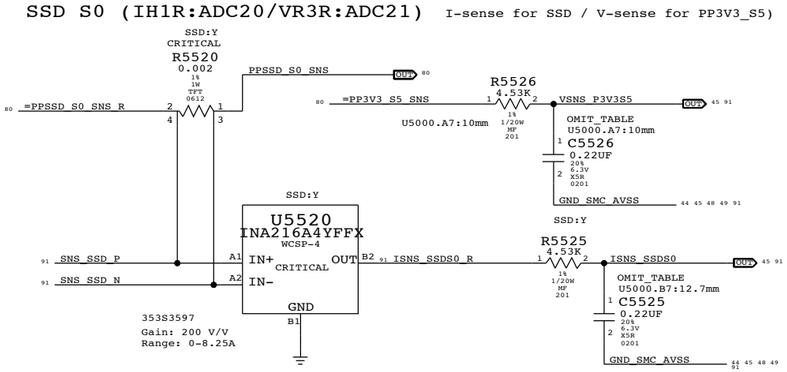


VDDQ S3 (VM0R:ADC6/IM0R:ADC7)

VDDQ lowside sense for SO-DIMM modules



SSD S0 (IH1R:ADC20/VR3R:ADC21) I-sense for SSD / V-sense for PP3V3_S5)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0304	2	CAP,0.22UF,201	C5525,C5526	SSD:Y
117S0002	2	RES,0 OHM,201	C5525,C5526	SSD:N

SYNC_MASTER=J16 TONY SYNC_DATE=06/03/2013

PAGE TITLE: I and V Sense(Continued)

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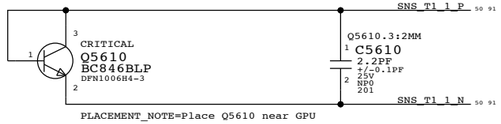
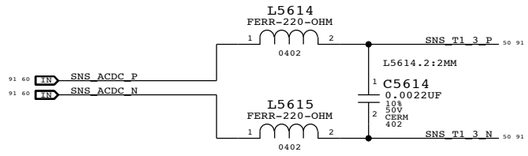
Temperature Sensor T1

GPU Proximity

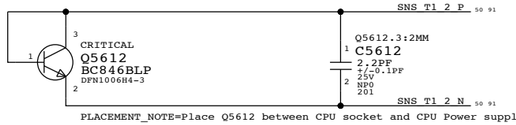


PLACEMENT_NOTE=Place Q5610 near GPU

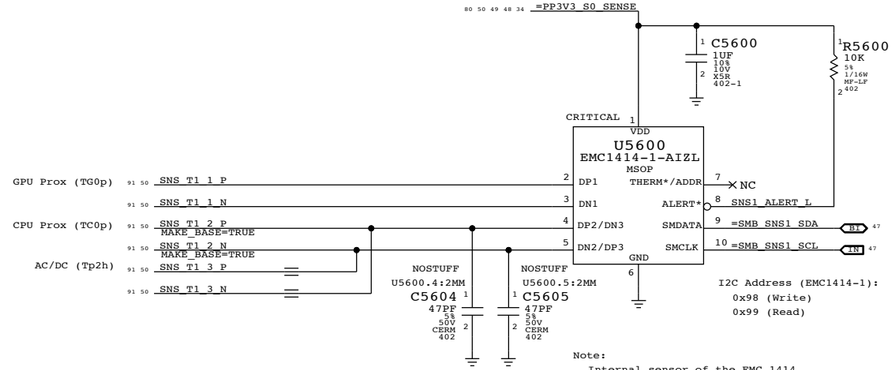
AC/DC Diode on supply



CPU Proximity



PLACEMENT_NOTE=Place Q5612 between CPU socket and CPU Power supply components



I2C Address (EMC1414-1):
0x98 (Write)
0x99 (Read)

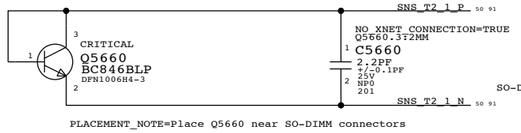
Note:
Internal sensor of the EMC 1414 will be used as the ambient sensor. Place U5600 at the coolest location on the MLB.

Filter Caps: Stuff if needed for PSU sensor SI

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode

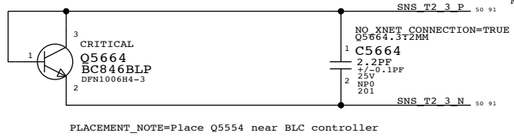
Temperature Sensor T2

SO-DIMM Proximity



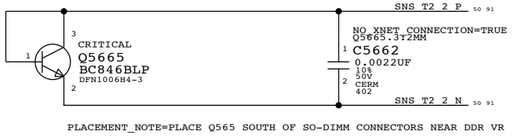
PLACEMENT_NOTE=Place Q5660 near SO-DIMM connectors

BLC Proximity

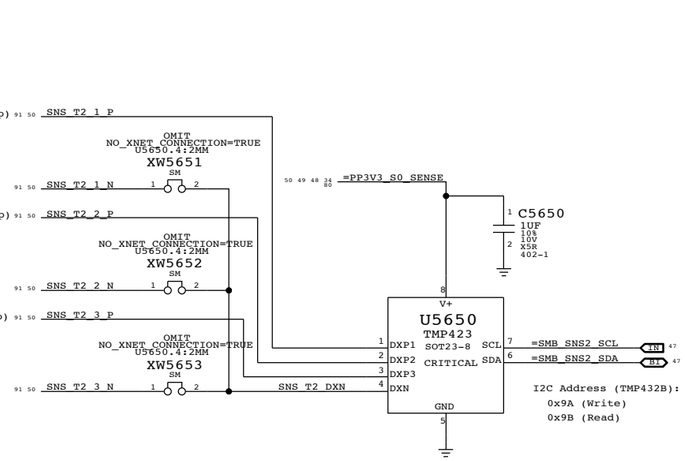


PLACEMENT_NOTE=Place Q5554 near BLC controller

MLB Proximity

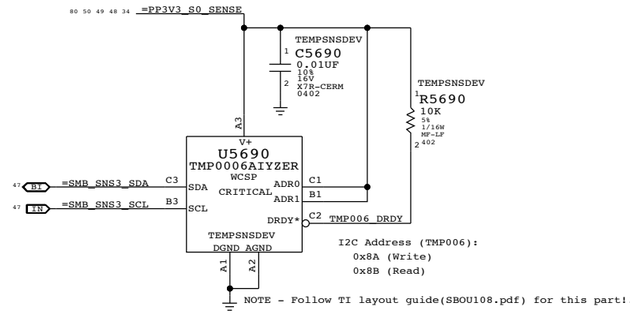


PLACEMENT_NOTE=PLACE Q565 SOUTH OF SO-DIMM CONNECTORS NEAR DDR VR



I2C Address (TMP432B):
0x9A (Write)
0x9B (Read)

Temperature Sensor T3: LCD Remote Sensor(Dev Only)



I2C Address (TMP006):
0x8A (Write)
0x8B (Read)

NOTE - Follow TI layout guide(SBOU108.pdf) for this part!!!

This PD part is a rubber bumper to protect TMP006
Added to board BOM (DEV only) to clean up PD BOM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
875-6433	1	BUMPER,U5690,D7	BUMPER_U5690	TEMPSNSDEV

SYNC_MASTER=J16_FIYIN SYNC_DATE=06/11/2013

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Temperature Sensors

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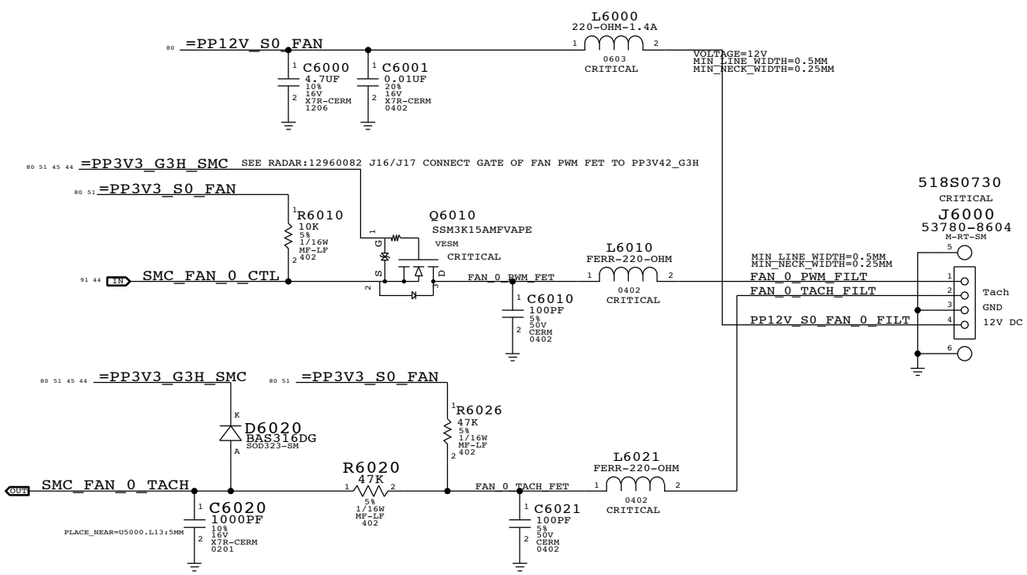
SMC Fan 0 (System)

Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q6010 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q6010 is at common and the SMC sinks current when Q6010 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).



Add C6020 1000pF Cap, Change R6020 to 47K -- Radar 11661918 D8 Proto1 Fan Tach instability.

SMC Fan 1 (Unused)

44 IN SMC_FAN_1_CTL — NC_SMC_FAN_1_CTL
MAKE_BASE=TRUE NO_TEST=TRUE

44 OUT SMC_FAN_1_TACH — NC_SMC_FAN_1_TACH
MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=J16_MLB_IG SYNC_DATE=05/01/2013

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System Fan

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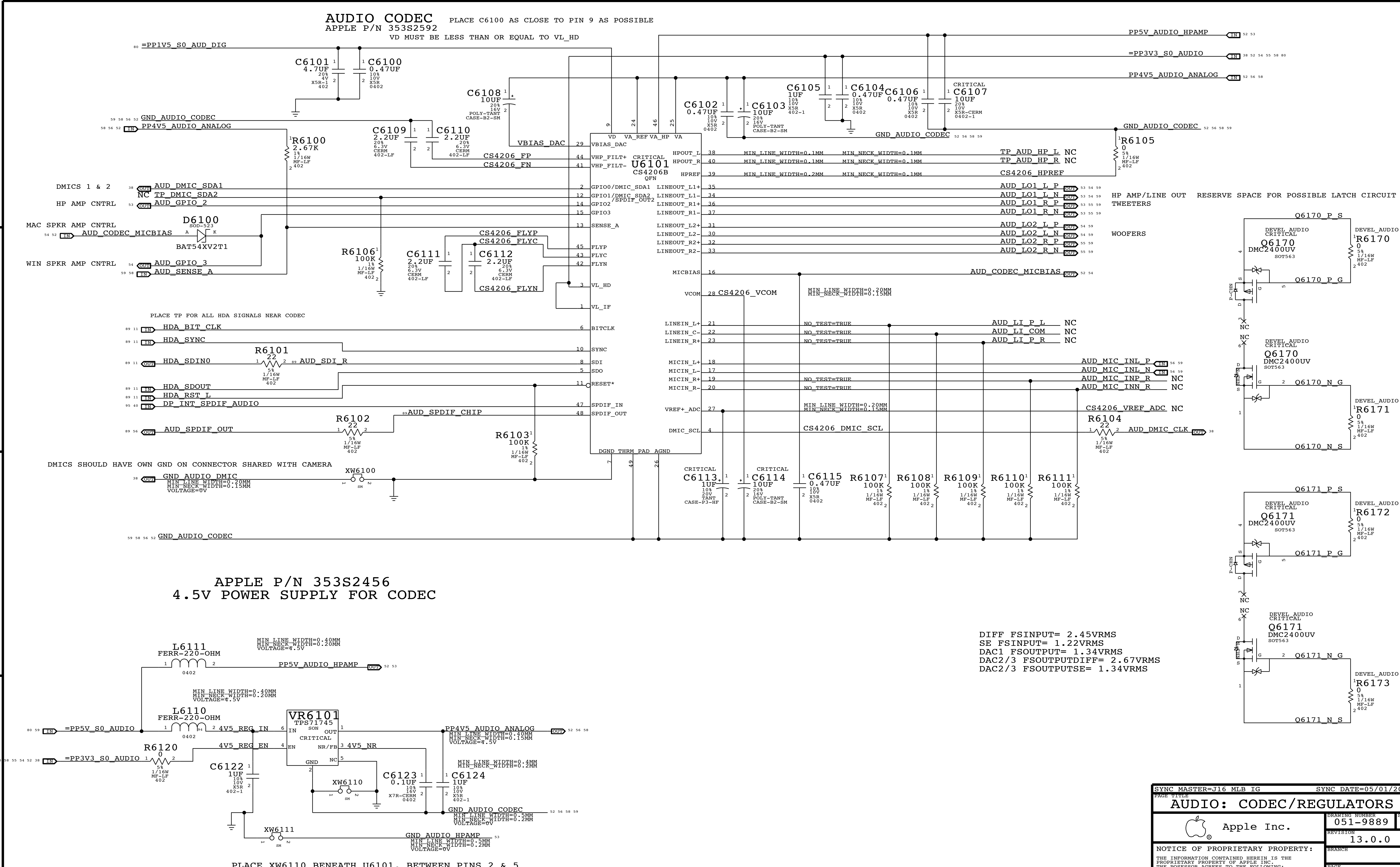

SYNC_MASTER=J16_MLB_IG SYNC_DATE=05/01/2013

PAGE TITLE: AUDIO: CODEC/REGULATORS

Apple Inc.

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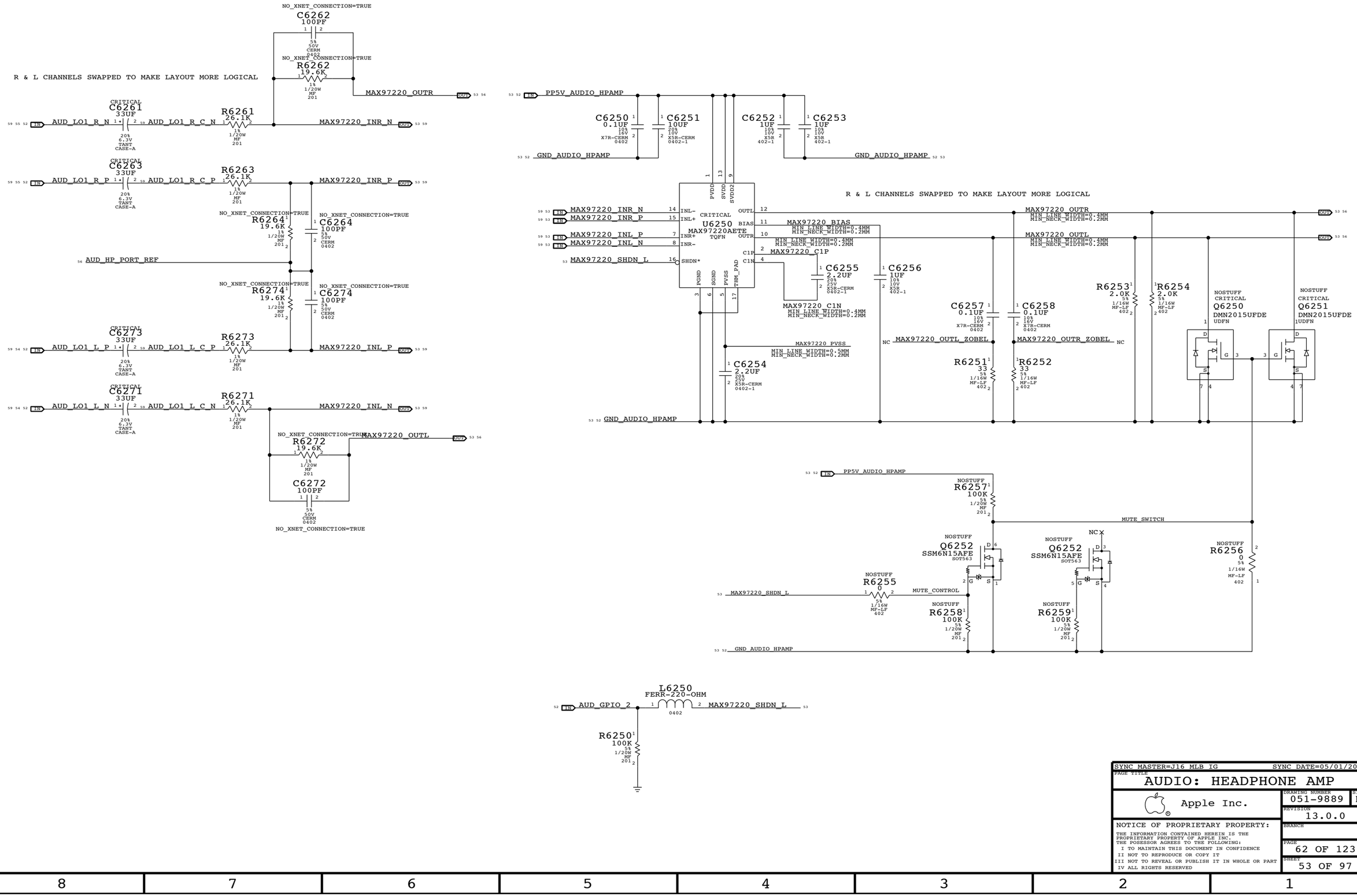

SYNC MASTER=J16_MLB_IG SYNC DATE=05/01/2013

PAGE TITLE

AUDIO: HEADPHONE AMP

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LEFT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)

80 55 IN =PP12V_S0_AUDIO_SPKRAMP

C6300 10UF 10% 25V X5R 805
C6301 10UF 10% 25V X5R 805
C6302 0.1UF 10% 25V X5R 402
C6303 1UF 20% 25V X5R 603-1
C6304 0.1UF 10% 25V X5R 402
C6305 1UF 10% 25V X5R 603-1
CRITICAL C6306 470UF 20% 16V POLY SM

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

59 53 52 IN AUD_LO1_L_N — L6303 FERR-1000-OHM 0402 — C6308 4700PF 5% 50V NPO-C0G-CERM 0805 — AUD_LAMP_RINC_P — AUD_LAMP_RIN_P
59 53 52 IN AUD_LO1_L_P — L6302 FERR-1000-OHM 0402 — C6309 4700PF 5% 50V NPO-C0G-CERM 0805 — AUD_LAMP_RINC_N — AUD_LAMP_RIN_N
59 52 IN AUD_LO2_L_N — L6300 FERR-1000-OHM 0402 — C6310 1UF 10% 25V X5R 0402 — AUD_LAMP_LINC_P — AUD_LAMP_LIN_P
59 52 IN AUD_LO2_L_P — L6301 FERR-1000-OHM 0402 — C6311 1UF 10% 25V X5R 0402 — AUD_LAMP_LINC_N — AUD_LAMP_LIN_N

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

80 58 55 52 38 =PP3V3_S0_AUDIO

CRITICAL U6300 SSM3302 LFCSP

20	INR+	
19	INR-	
22	SDNR*	WOOFERS & TWEETERS ON UNDER MAC OS — 55 54 IN AUD_SPKRAMP_MAC_SHDN_L
16	MONO	54 AUD_LAMP_MONO
9	SDNL*	ONLY WOOFERS ON UNDER WINDOWS — 55 54 IN AUD_SPKRAMP_WIN_SHDN_L
11	INL+	
12	INL-	
21	GAIN	54 AUD_LAMP_GAIN
8	VREG/AVDD	54 AUD_LAMP_AVDD (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM, VOLTAGE=5V)
23	REGEN	
17	THERM	TP_AUD_LAMP_THERM NC
30	BOOTR+	AUD_LAMP_BOOTRP (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM) — C6313 0.22UF 20% 25V X5R 603
28	OUTR+	
29		
26	OUTR-	
27		
25	BOOTR-	AUD_LAMP_BOOTRN (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM) — C6314 0.22UF 20% 25V X5R 603
10	EDGE	54 AUD_LAMP_EDGE
1	BOOTL+	AUD_LAMP_BOOTLP (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM) — C6315 0.22UF 20% 25V X5R 603
2	OUTL+	
3		
4	OUTL-	
5		
6	BOOTL-	AUD_LAMP_BOOTLN (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM) — C6316 0.22UF 20% 25V X5R 603
18	NC	NC
13	NC	NC
14		
15	TEST	
34 35 36 37	PVDD	
7 24 41	AGND	
31 32 33 38 39 40	PGND	
	THRM_PAD	

C6317 2.2UF 20% 10V X5R-CERM 402

PINS 14 & 15 ARE TEST PINS AND SHOULD BE TIED TO GND

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

AUD_LAMP_OUTPR (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM) — AUD_LAMP_OUTNR
NO_XNET_CONNECTION=TRUE CRITICAL L6305 110-OHM-3A DLY5ATN1111SQ2 (SM_VSS-1)
AUD_SPKR_LTWT_OUT_P — NO_XNET_CONNECTION=TRUE CRITICAL C6323 1000PF 5% 25V CERM 0402 — AUD_SPKR_LTWT_OUT_N
AUD_LAMP_OUTPL (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM) — AUD_LAMP_OUTNL
NO_XNET_CONNECTION=TRUE CRITICAL L6307 110-OHM-3A DLY5ATN1111SQ2 (SM_VSS-1)
AUD_SPKR_LWFR_OUT_N — NO_XNET_CONNECTION=TRUE CRITICAL C6324 1000PF 5% 25V CERM 0402 — AUD_SPKR_LWFR_OUT_P

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

NO_XNET_CONNECTION=TRUE — CRITICAL C6320 1000PF 5% 25V CERM 0402
CRITICAL C6322 1000PF 5% 25V CERM 0402 — NO_XNET_CONNECTION=TRUE
NO_XNET_CONNECTION=TRUE — CRITICAL C6319 1000PF 5% 25V CERM 0402
CRITICAL C6321 1000PF 5% 25V CERM 0402 — NO_XNET_CONNECTION=TRUE

L6308 FERR-1000-OHM 0402
52 IN AUD_CODEC_MICBIAS — AUD_SPKRAMP_MAC_SHDN_L OUT 54 55
R6301 100K 5% 1/16W MF-LF 402
NOSTUFF C6312 100PF 5% 50V CERM 0402

R6308 0 5% 1/16W MF-LF 402
52 IN AUD_GPIO_3 — AUD_SPKRAMP_WIN_SHDN_L OUT 54 55
R6309 100K 5% 1/16W MF-LF 402
NOSTUFF C6318 100PF 5% 50V CERM 0402

EDGE RATE CONTROL

	R6304	R6305
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6306	R6307
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF

54 AUD_LAMP_AVDD
R6304 0 5% 1/16W MF-LF 402 — AUD_LAMP_EDGE 54
NOSTUFF R6305 0 5% 1/16W MF-LF 402
R6303 0 5% 1/16W MF-LF 402 — AUD_LAMP_MONO 54
NOSTUFF R6306 0 5% 1/16W MF-LF 402 — AUD_LAMP_GAIN 54
R6307 47K 5% 1/16W MF-LF 402

SYNC MASTER=J16_MLB_IG SYNC DATE=05/01/2013
PAGE TITLE: AUDIO: LEFT SPKR AMP

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RIGHT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)

=PP12V_S0_AUDIO_SPKRAMP

C6400 10UF 10% 25V X5R 805
C6401 10UF 10% 25V X5R 805
C6402 0.1UF 10% 25V X5R 402
C6403 1UF 10% 25V X5R 603-1
C6404 0.1UF 10% 25V X5R 402
C6405 1UF 10% 25V X5R 603-1
CRITICAL C6406 470UF 20% 16V POLY SM

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

L6400 FERR-1000-OHM 0402 — AUD_LO2_R_N — AUD_RAMP_RINC_P — C6408 1UF 10% 25V X5R 0402 — AUD_RAMP_RIN_P
L6401 FERR-1000-OHM 0402 — AUD_LO2_R_P — AUD_RAMP_RINC_N — C6409 1UF 10% 25V X5R 0402 — AUD_RAMP_RIN_N
L6402 FERR-1000-OHM 0402 — AUD_LO1_R_P — AUD_RAMP_LINC_P — C6410 4700PF 5% 50V NPO-C0G-CERM 0805 — AUD_RAMP_LIN_P
L6403 FERR-1000-OHM 0402 — AUD_LO1_R_N — AUD_RAMP_LINC_N — C6411 4700PF 5% 50V NPO-C0G-CERM 0805 — AUD_RAMP_LIN_N

CRITICAL
U6400
SSM3302
LFCSP

PVDD (34, 35, 36, 37)

INR+ (20)
INR- (19)
SDNR* (22) ← AUD_SPKRAMP_WIN_SHDN_L — ONLY WOOFERS ON UNDER WINDOWS
MONO (16) ← AUD_RAMP_MONO
SDNL* (9) ← AUD_SPKRAMP_MAC_SHDN_L — WOOFERS & TWEETERS ON UNDER MAC OS
INL+ (11)
INL- (12)
GAIN (21) ← AUD_RAMP_GAIN
VREG/AVDD (8) ← AUD_RAMP_AVDD (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM, VOLTAGE=5V)
REGEN (23) ← =PP3V3_S0_AUDIO

THERM (17) — TP_AUD_RAMP_THERM — NC
BOOTR+ (30) — C6413 0.22UF 20% 25V X5R 603 — AUD_RAMP_BOOTRP (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)
OUTR+ (28, 29) — AUD_RAMP_OUTPR (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
OUTR- (26, 27) — AUD_RAMP_OUTNR (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
BOOTR- (25) — C6414 0.22UF 20% 25V X5R 603 — AUD_RAMP_BOOTRN (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)
EDGE (10) ← AUD_RAMP_EDGE
BOOTL+ (1) — C6415 0.22UF 20% 25V X5R 603 — AUD_RAMP_BOOTLP (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)
OUTL+ (2, 3) — AUD_RAMP_OUTPL (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
OUTL- (4, 5) — AUD_RAMP_OUTNL (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
BOOTL- (6) — C6416 0.22UF 20% 25V X5R 603 — AUD_RAMP_BOOTLN (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)
NC (18) — NC
NC (13) — NC
TEST (14, 15)

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

NO_XNET_CONNECTION=TRUE
CRITICAL
L6405 110-OHM-3A DLY5ATN111SQ2 (SM_VSS-1)
AUD_SPKR_RWFR_OUT_P — NO_XNET_CONNECTION=TRUE CRITICAL C6423 1000PF 5% 25V CERM 0402 — AUD_SPKR_RWFR_OUT_N

NO_XNET_CONNECTION=TRUE
CRITICAL
L6407 110-OHM-3A DLY5ATN111SQ2 (SM_VSS-1)
AUD_SPKR_RTWT_OUT_P — NO_XNET_CONNECTION=TRUE CRITICAL C6424 1000PF 5% 25V CERM 0402 — AUD_SPKR_RTWT_OUT_N

CRITICAL C6420 1000PF 5% 25V CERM 0402 — NO_XNET_CONNECTION=TRUE
CRITICAL C6422 1000PF 5% 25V CERM 0402 — NO_XNET_CONNECTION=TRUE
CRITICAL C6419 1000PF 5% 25V CERM 0402 — NO_XNET_CONNECTION=TRUE
CRITICAL C6421 1000PF 5% 25V CERM 0402 — NO_XNET_CONNECTION=TRUE

AGND (7, 24) — THRM_PAD (41) — PGND (31, 32, 33, 38, 39, 40)

PINS 14 & 15 ARE TEST PINS AND SHOULD BE TIED TO GND

EDGE RATE CONTROL

	R6404	R6405
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6406	R6407
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF

AUD_RAMP_AVDD — R6404 0 5% 1/16W MF-LF 402 — AUD_RAMP_EDGE
NOSTUFF R6405 0 5% 1/16W MF-LF 402
AUD_RAMP_MONO — R6403 0 5% 1/16W MF-LF 402
NOSTUFF R6406 0 5% 1/16W MF-LF 402 — AUD_RAMP_GAIN
R6407 47K 5% 1/16W MF-LF 402

SYNC MASTER=J16 MLB IG — SYNC DATE=05/01/2013

PAGE TITLE
AUDIO: RIGHT SPKR AMP

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MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2640

PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=10.63KHZ

MIKEY 1A
APN:353S2640
MIKEY ADDRESS: WRITE=72H, READ=73H

I2C ADDRESSES

MIKEY	READ	0111 0011	0X73
MIKEY	WRITE	0111 0010	0X72
CHS	READ	0111 0111	0X77
CHS	WRITE	0111 0110	0X76

AUDIO JACK: HP CONNECTOR WITH MIKEY
PLACE XWS 6500 & 6501 AT J6500 PINS

I2C PULLUPS ON SOUTHBRIDGE PAGE

PP4V5_AUDIO_ANALOG
=PP3V3_S0_AUDIO_DIG
R6562 10K 5% 1/20W MF 201
CRITICAL C6555 4.7UF 20% 10V X5R-CERM 0402
C6560 0.1UF 10% 16V X7R-CERM 0402
CRITICAL U6551 CD3285A0 MQFN-RSV
AVDD
=I2C_MIKEY_SCL
=I2C_MIKEY_SDA
AUD_I2C_INT_L
AUD_IPHS_SWITCH_EN
SCL
SDA
INT*
ENABLE
HDET
CS
DGND AGND
MICBIAS
DETECT
BYPASS
HS_MIC_BIAS
HS_SW_DET
HS_RX_BP
MIN_LINE_WIDTH=0.25MM MIN_NECK_WIDTH=0.20MM
NO_XNET_CONNECTION=TRUE
R6554 1K 5% 1/16W MF-LF 402
C6556 0.01UF 10% 25V X7R 402
NOSTUFF R6561 47K 5% 1/16W MF-LF 402
HS_HDET
AUD_PORTD_DET_L
R6555 100K 5% 1/20W MF 201
GND_AUDIO_CODEC

C6552 0.1UF 10% 16V X7R-CERM 0402
AUD_MIC_INL_P
R6550 2.2K 5% 1/16W MF-LF 402
AUD_HS_MIC_RC_P
AUD_HS_MIC_P
R6556 100K 5% 1/20W MF 201
CRITICAL C6550 0.0082UF 10% 25V X7R-CERM 0402
CRITICAL C6558 27PF 5% 50V CERM 0402-1
C6553 0.1UF 10% 16V X7R-CERM 0402
AUD_MIC_INL_N
R6551 0 5% 1/16W MF-LF 402
AUD_HS_MIC_RC_N
AUD_HS_MIC_N
R/C6750 FILTER TO ADDRESS OUT-OF-BAND NOISE ISSUE SEEN ON EARLY HEADSETS (SEE RADAR # 6210118)
NOSTUFF NO_XNET_CONNECTION=TRUE R6553 1K 5% 1/16W MF-LF 402

L6500 FERR-1000-OHM 0402 AUD_TYPEDET_R
L6501 FERR-1000-OHM 0402 AUD_HS_MIC_N
L6502 FERR-1000-OHM 0402 AUD_HS_MIC_P
CRITICAL L6503 FERR-120-OHM-2.0A 0402 HS_MIC_BIAS MIN_LINE_WIDTH=0.25MM MIN_NECK_WIDTH=0.20MM
CRITICAL L6511 FERR-120-OHM-2.0A 0402 =PP3V3_S4_AUDIO_DIG MIN_LINE_WIDTH=0.25MM MIN_NECK_WIDTH=0.20MM
L6505 FERR-1000-OHM 0402 AUD_TIPDET2_R
R6506 0 5% 1/16W MF-LF 402 GND_AUDIO_CODEC MIN_LINE_WIDTH=0.50MM MIN_NECK_WIDTH=0.20MM VOLTAGE=0V

APN 516S0687

CRITICAL NO_XNET_CONNECTION=TRUE J6500 54722-0224 F-ST-SM

AUD_J1_TYPEDET_R	1	2	AUD_J1_HP_OUTL
AUD_J1_MIC_N	3	4	AUD_J1_HP_PORT_REF
AUD_J1_MIC_P	5	6	AUD_J1_HP_OUTR
	7	8	
	9	10	
AUD_J1_MIC_BIAS	11	12	
	13	14	
AUD_J1_PP3V3_S0	15	16	
=I2C_CHS_SCL	17	18	
=I2C_CHS_SDA	19	20	AUD_SPDIF_OUT
AUD_J1_TIPDET2_R	21	22	AUD_J1_TIPDET1_R

CRITICAL L6507 FERR-120-OHM-2.0A 0402 MAX97220_OUTL MIN_LINE_WIDTH=0.25MM MIN_NECK_WIDTH=0.20MM
CRITICAL L6508 FERR-120-OHM-2.0A 0402 AUD_HP_PORT_REF
CRITICAL L6509 FERR-120-OHM-2.0A 0402 MAX97220_OUTR MIN_LINE_WIDTH=0.25MM MIN_NECK_WIDTH=0.20MM
L6510 FERR-1000-OHM 0402 AUD_TIPDET1_R

NOSTUFF DZ6500 ESDALC5-1BM2 SOD882 POLARITY INTENTIONALLY OPPOSITE
NOSTUFF DZ6501 ESDALC5-1BM2 SOD882
NOSTUFF DZ6502 ESDALC5-1BM2 SOD882
NOSTUFF DZ6503 ESDALC5-1BM2 SOD882
NOSTUFF DZ6504 ESDALC5-1BM2 SOD882
NOSTUFF DZ6505 ESDALC5-1BM2 SOD882

SYNC_MASTER=J16 MLB_TG SYNC_DATE=05/01/2013
PAGE TITLE
AUDIO: Jack, Mikey, CHS Switch

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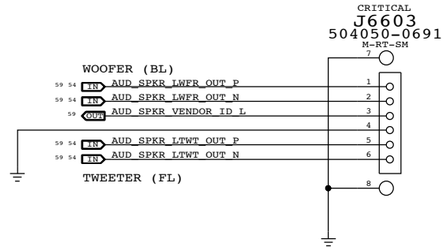
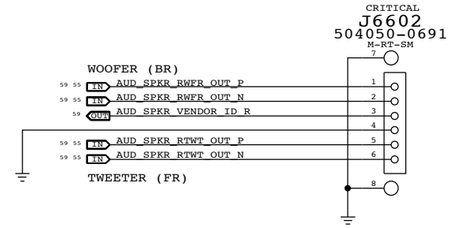
SPEAKER CABLE CONNECTORS

APPLE P/N 518S0862





SYNC MASTER=J16 MLB IG SYNC DATE=05/01/2013

PAGE TITLE

Audio: Spkr/Mic Conn.

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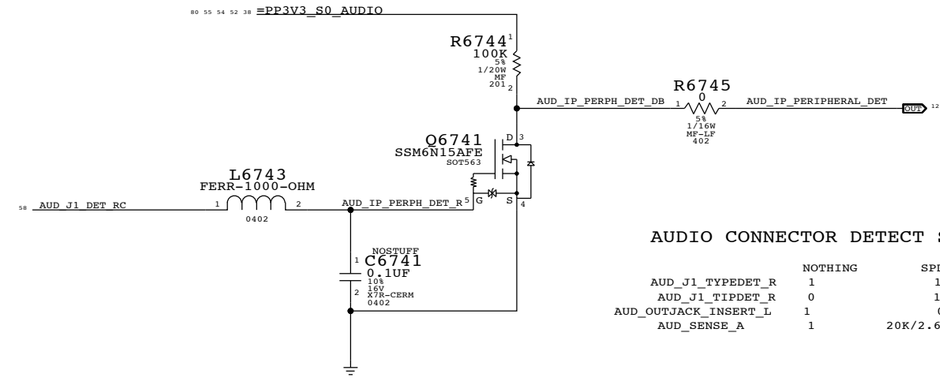
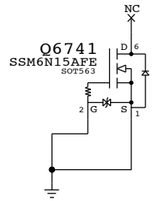
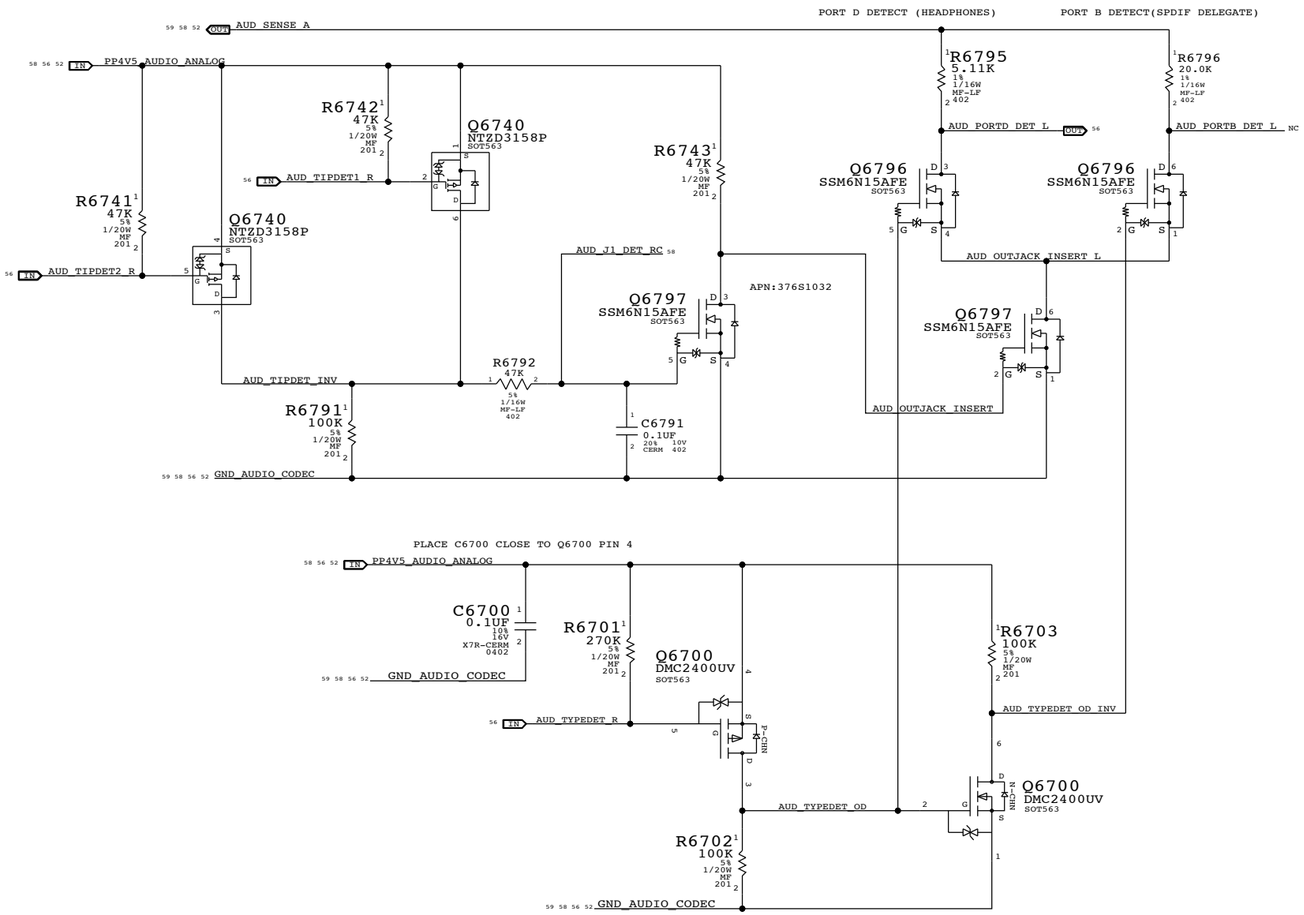
IPHS HS Detect Debounce CKT



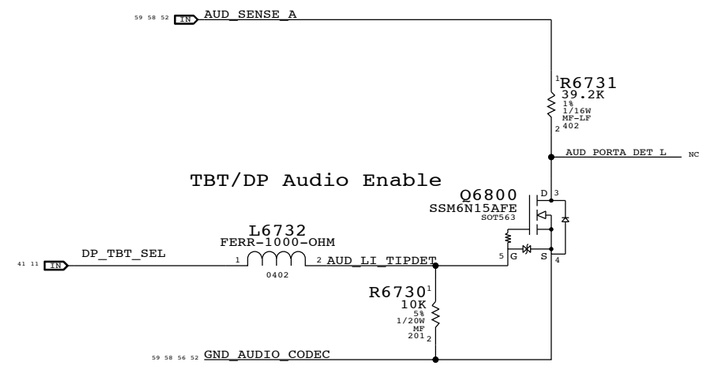
AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_J1_TYPEDET_R	1	1	0
AUD_J1_TIPDET_R	0	1	1
AUD_OUTJACK_INSERT_L	1	0	0
AUD_SENSE_A	1	20K/2.67K RDIV	39.2K/2.67K RDIV





Target Display Mode Detect



TBT/DP Audio Enable

SYNC MASTER=J16 MLB IG SYNC DATE=05/01/2013

PAGE TITLE
AUDIO: Detects/Grounding

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_2	0X0A (DET D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	MICBIAS	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X03 (3)	0X03 (3)	0X0A (10,V24)	MICBIAS	N/A	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (DET B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
SPDIF IN	0X07 (7)	0x0F (15)	N/A	0X09 (DET A)
INTERNAL MIC ARRAY	0X06 (6) 0X05 (5)	0X0E (14,LEFT & RIGHT) 0X12 (18,LEFT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	Lynx POINT GPIO 16	Lynx POINT GPIO 5 (RCVR INT) Lynx POINT GPIO 3 (PERIPH DET)

OTHER DETECT

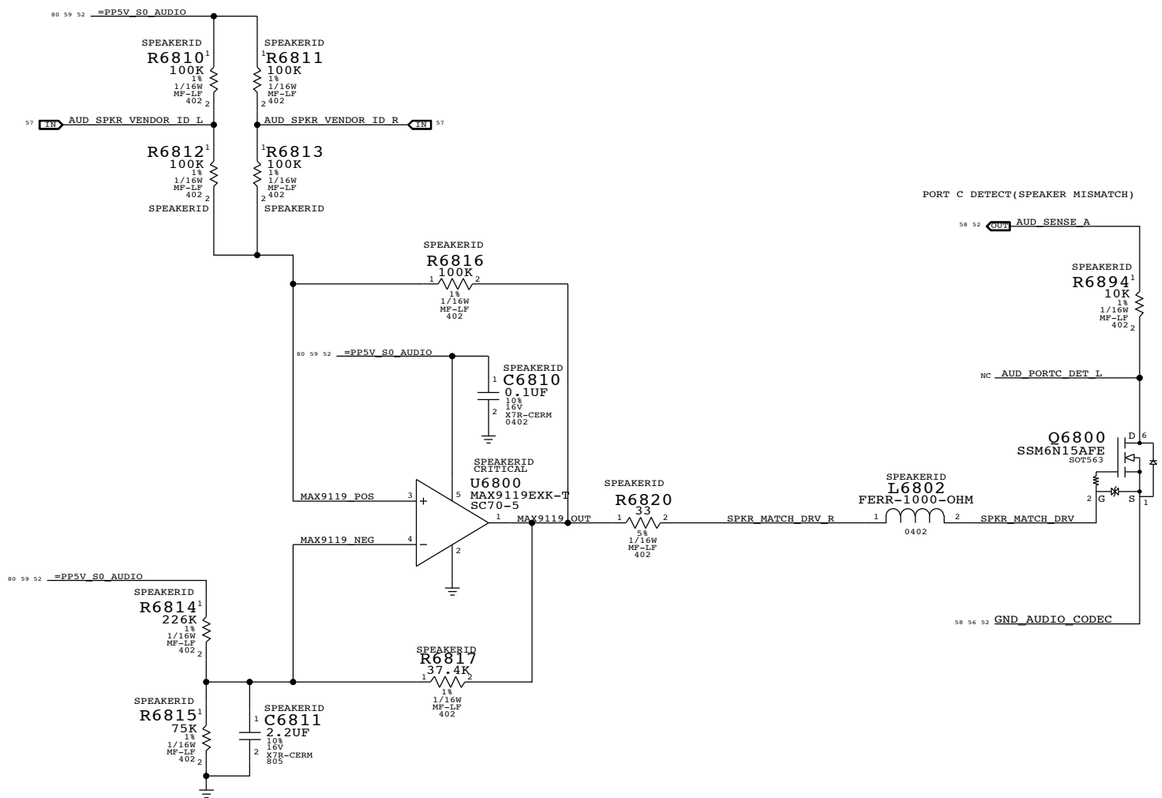
FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
MULTIPLE SPKR VENDORS	N/A	N/A	N/A	0X0C (DET C)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.1 MM	?
SPKROUT	*	0.2 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	52 53 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	52 53 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	52 53 55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	52 53 55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	52 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	52 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	52 55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	52 55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_P	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_N	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_P	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_N	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_P	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_N	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_P	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_N	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_P	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_N	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_P	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_N	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_P	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_N	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_P	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_N	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_N	53
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	55 57
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_N	55 57
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	55 57
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_N	55 57
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	54 57
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_N	54 57
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	54 57
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_N	54 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	52 56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N	52 56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_P	56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_N	56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_P	56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_N	56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_P	56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_N	56



SYNC MASTER=J16 MLB IG	SYNC DATE=05/01/2013
PAGE TITLE: AUDIO: Speaker ID	
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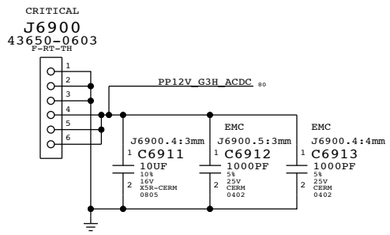
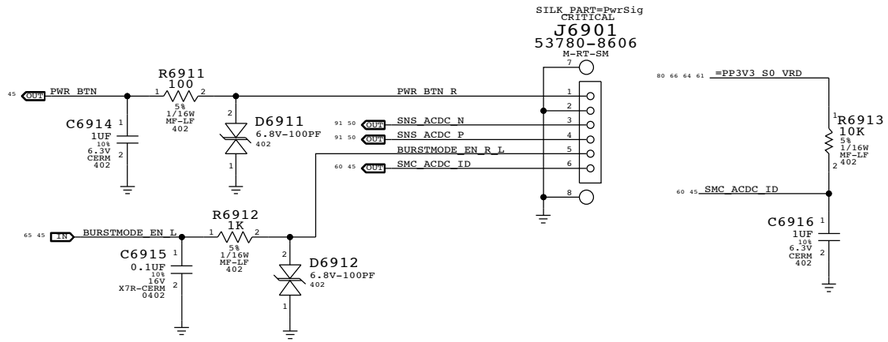
MLB to AC-DC Connector



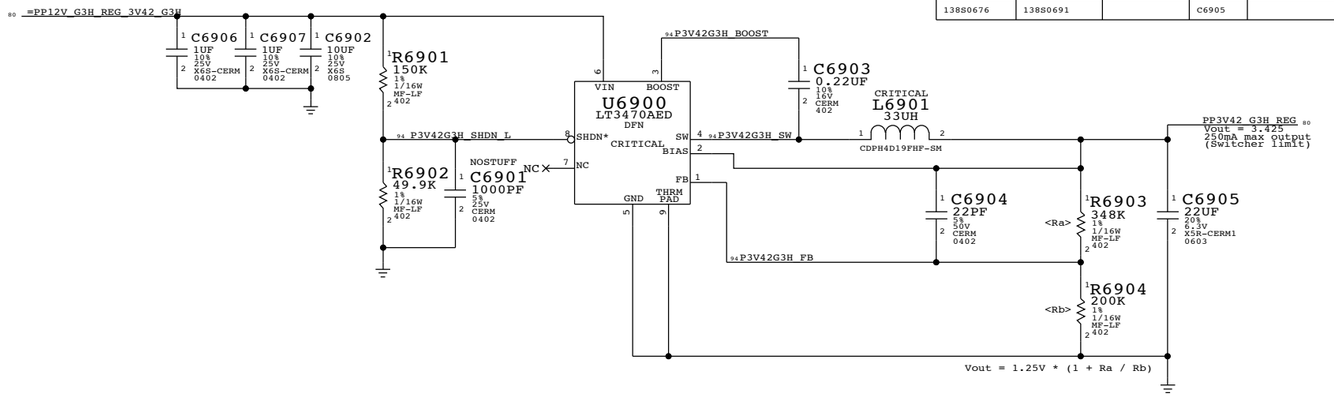
MLB to AC-DC Supplemental Signal Connector



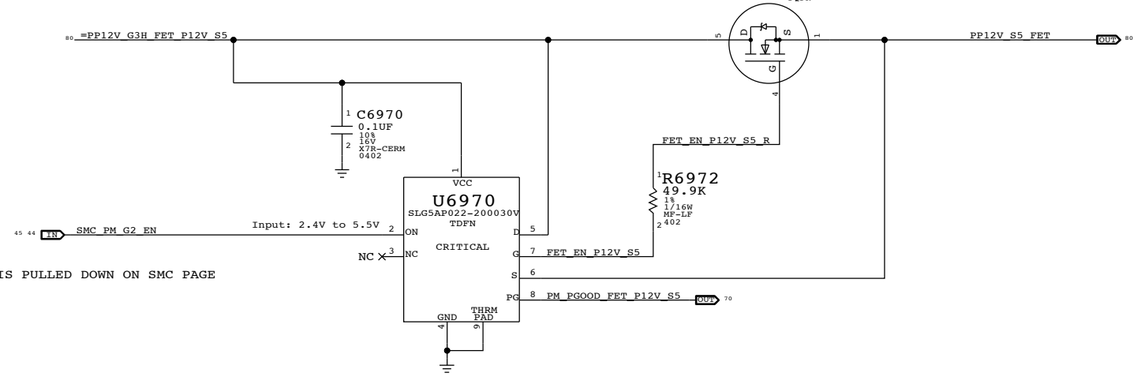
3.425V "G3Hot" Regulator

Switching freq: 409 kHz = $\frac{13.5}{L6901}$

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0676	138S0691		C6905	



12V S5 FET



SMC_PM_G2_EN IS PULLED DOWN ON SMC PAGE

SYNC_MASTER=J16_MLB_IG SYNC_DATE=05/01/2013

PAGE TITLE

Power Connectors / VReg G3Hot

Apple Inc.

DRAWING NUMBER 051-9889 SIZE D

REVISION 13.0.0

BRANCH

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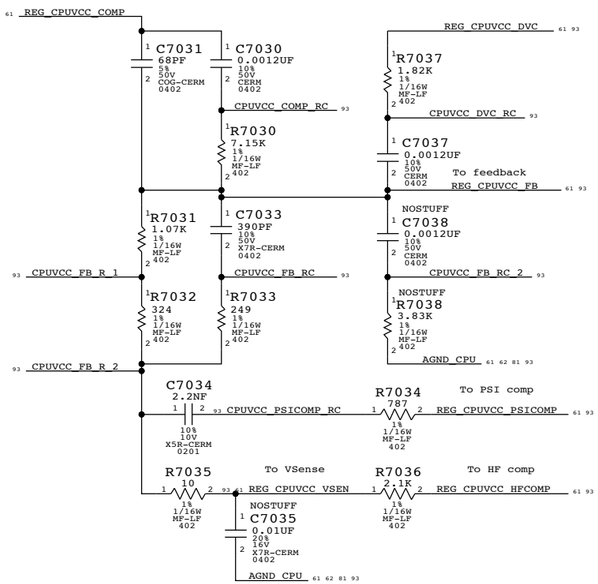
CPU VCC S0 Regulator

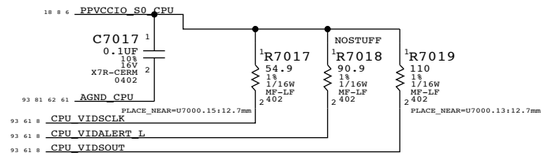
OC trip point: 114 A

Switching freq: 403 kHz = 5 E10 / R7003

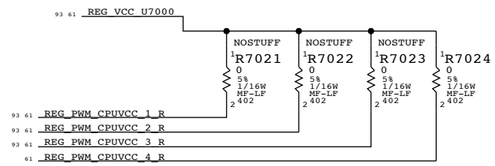
Compensation and feedback

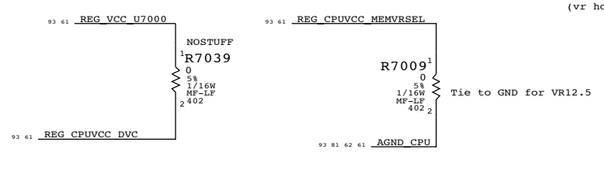


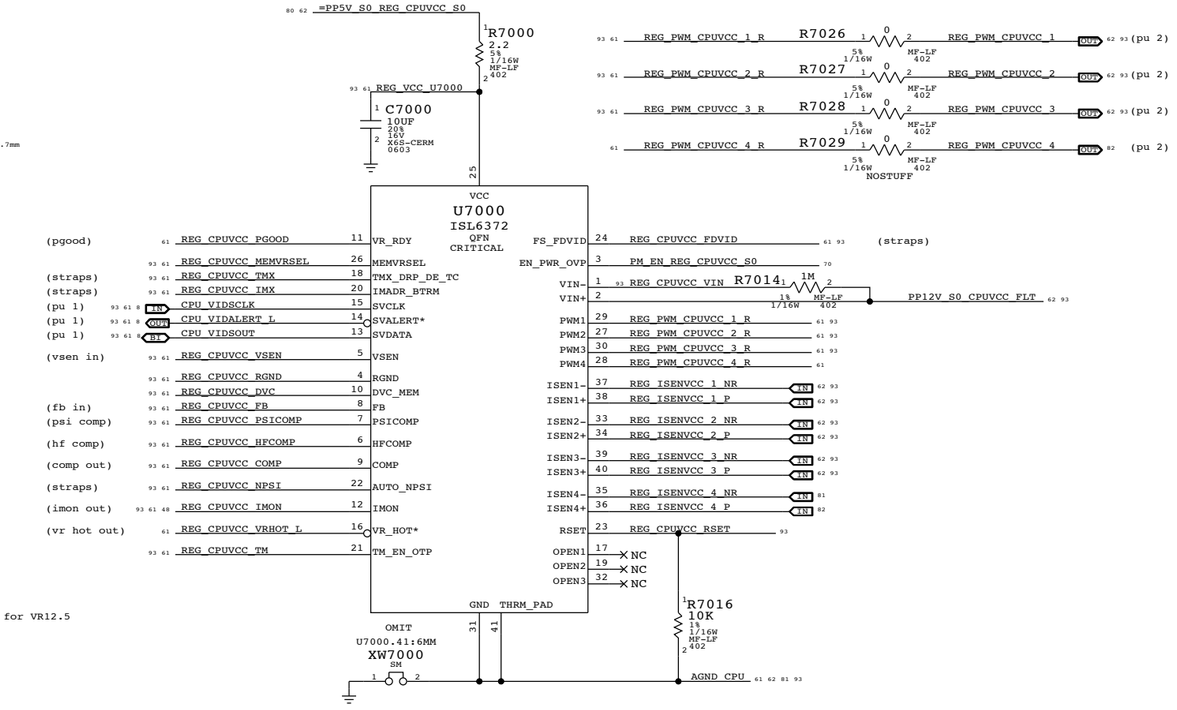
Pull-ups 1



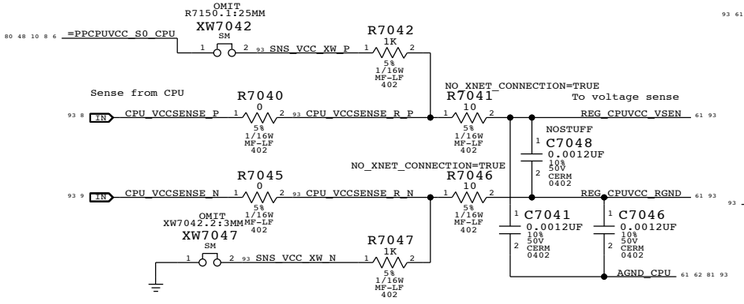
Pull-ups 2



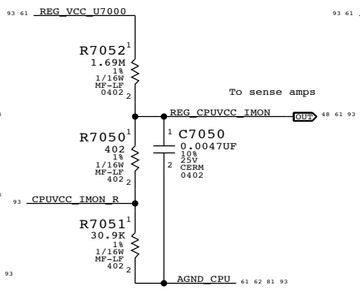




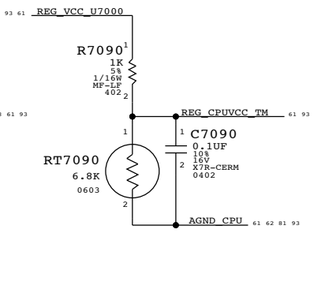
Voltage sense input



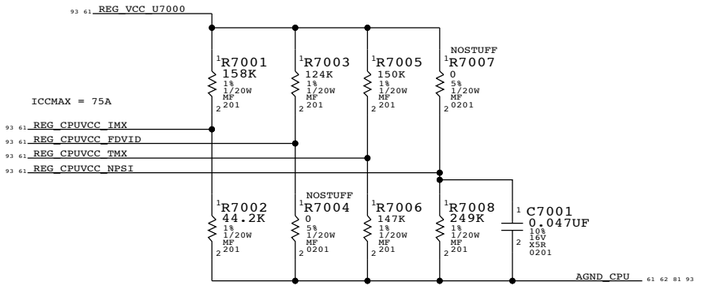
IMON output



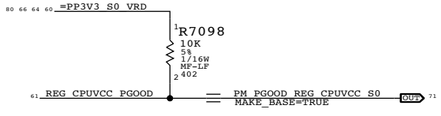
Temp measurement



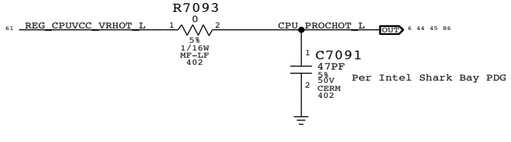
Straps



Power good



VRHot to ProcHot



SYNC_MASTER=J16_ROSSANA SYNC_DATE=07/29/2013

PAGE TITLE: VReg CPU VCC Cntl

Apple Inc.

DRAWING NUMBER: 051-9889 SIZE: D

REVISION: 13.0.0

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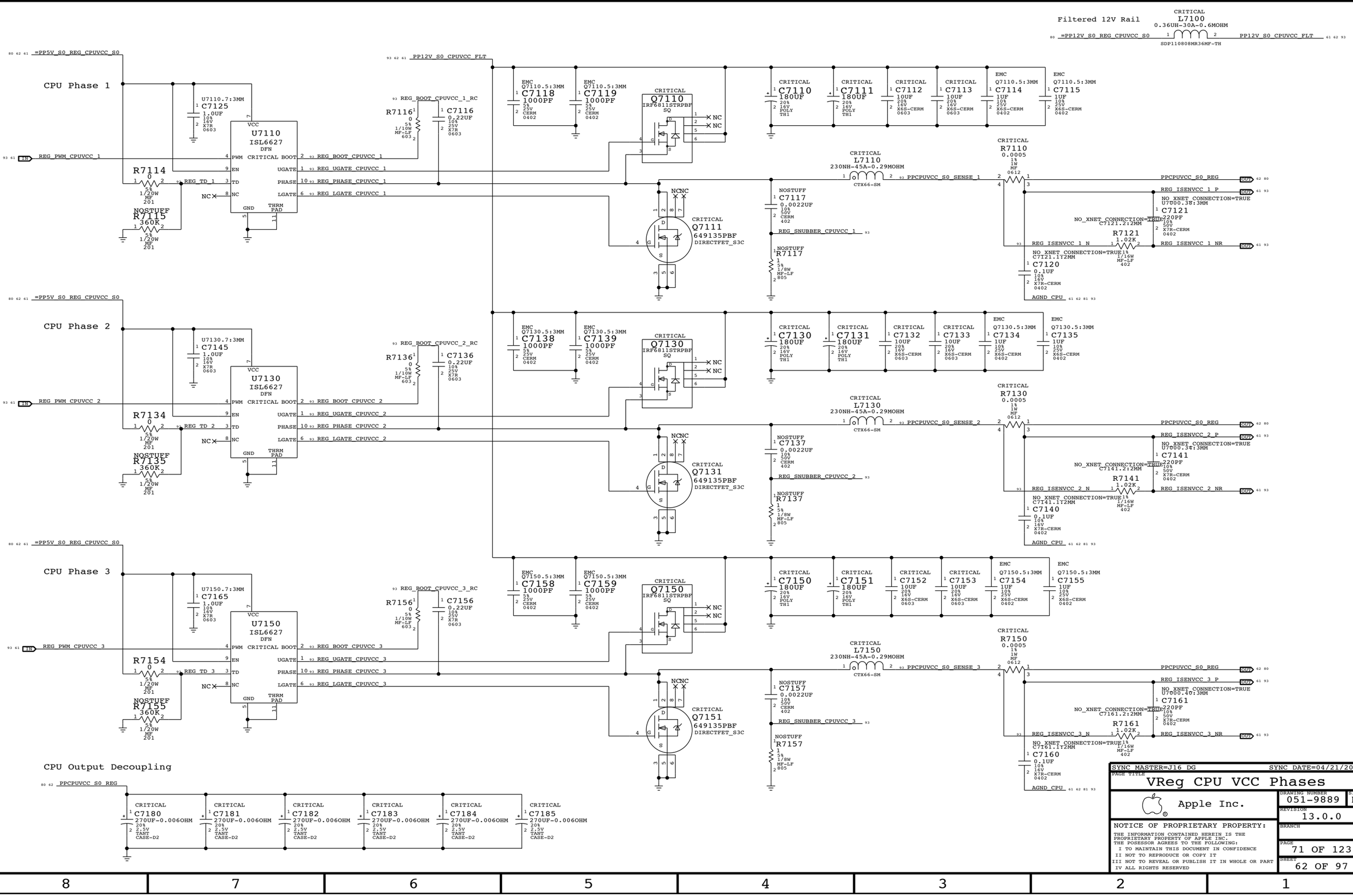

SYNC_MASTER=J16_DG SYNC_DATE=04/21/2013

PAGE TITLE

VReg CPU VCC Phases

Apple Inc.

DRAWING NUMBER 051-9889 SIZE D

REVISION 13.0.0

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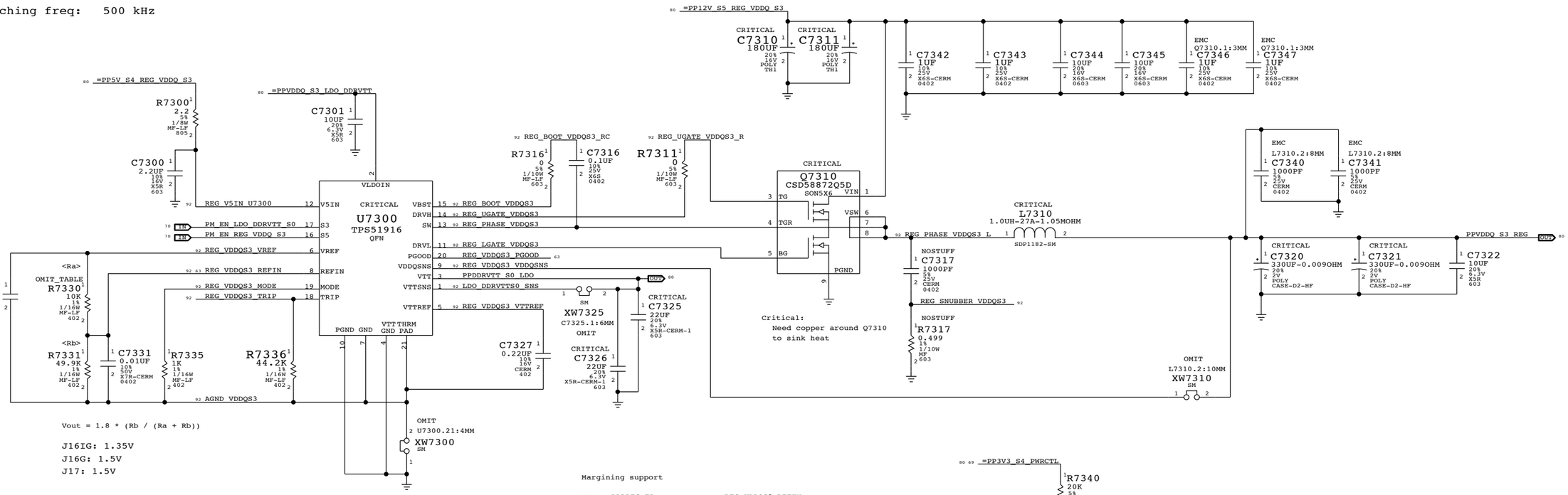
VDDQ (1.5V / 1.35V) S3 Regulator

OC trip point: 30.4 A VDDQ = $\frac{R7336}{8\ E5\ *\ Rds(Q7310)} + \frac{0.65625}{L7310\ *\ f(switch)}$

3 A VTT (FIXED)
10 mA VTTREF (FIXED)

Switching freq: 500 kHz



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0335	1	RES,16.5K,402	R7330	VDDQ:P1V35
114S0315	1	RES,10K,402	R7330	VDDQ:P1V5

SYNC MASTER=J16 ROSSANA SYNC DATE=06/17/2013

PAGE TITLE: VReg VDDQ S3

Apple Inc.

DRAWING NUMBER: 051-9889 SIZE: D

REVISION: 13.0.0

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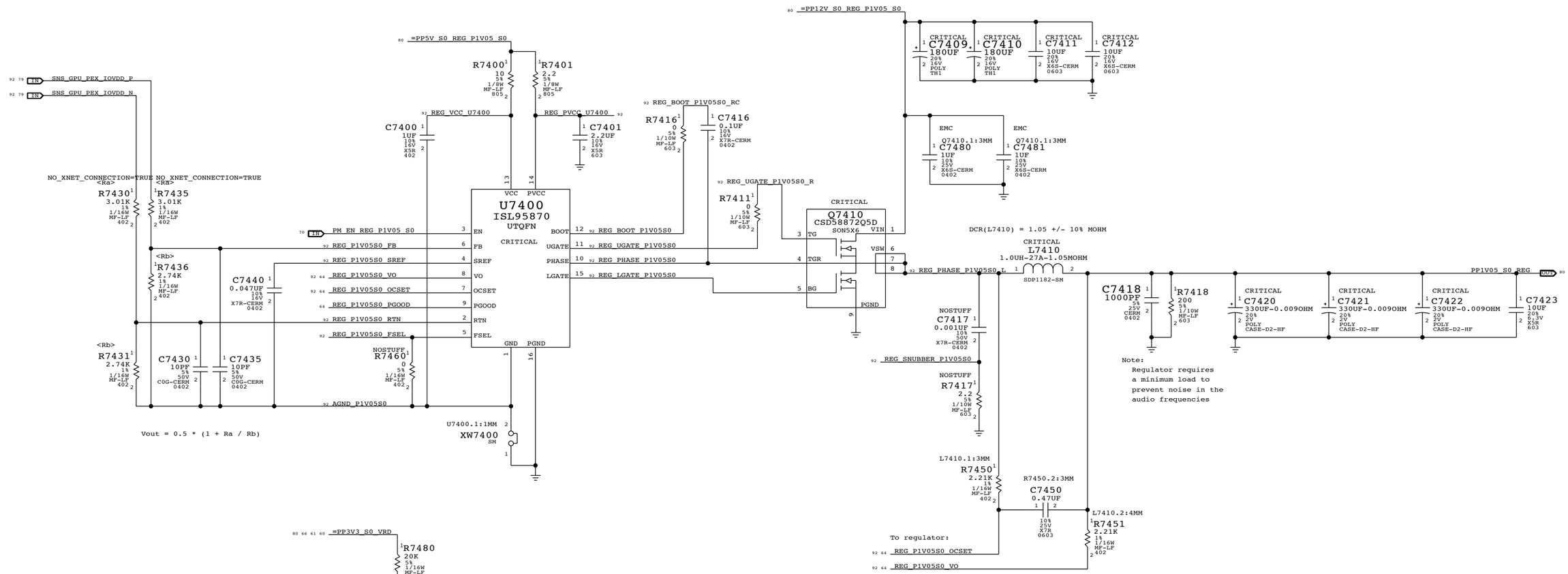
PCH/GPU/TBT (1.05V) S0 Regulator

Switching freq: 500 kHz OC trip point: 16.3 A = $\frac{R7450 * 8.5\ E\text{-}6}{DCR(L7410)}$

FSEL STRAP	SW FREQ
GND	300 kHz
VCC	1 MHz
100k to GND	600 kHz
FLOAT	500 kHz



SYNC MASTER=J16 ROSSANA SYNC DATE=07/29/2013

PAGE TITLE
VReg PCH/GPU/TBT 1V05 S0

Apple Inc.

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3.3V S5 Regulator

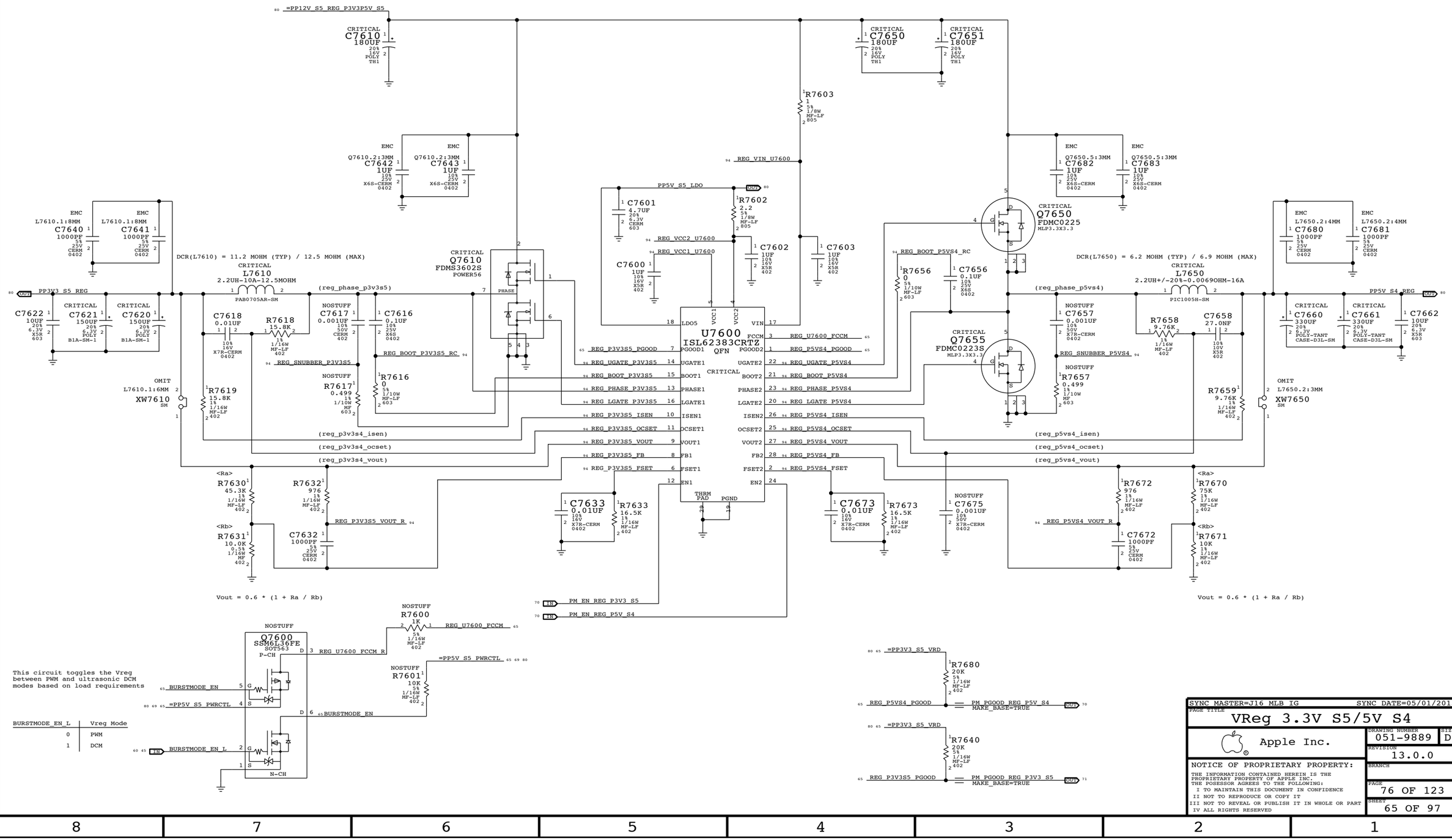
OC trip point: 12.5 A = $\frac{\text{R7618 * 10 E-6}}{\text{DCR(L7610)}}$

Switching freq: 356 kHz = $\frac{1}{\text{170 E-12 * R7633}}$

5V S4 Regulator

OC trip point: 14.1 A = $\frac{\text{R7658 * 10 E-6}}{\text{DCR(L7650)}}$

Switching freq: 356 kHz = $\frac{1}{\text{170 E-12 * R7673}}$



SYNC MASTER=J16 MLB IG SYNC DATE=05/01/2013

PAGE TITLE: VReg 3.3V S5/5V S4

Apple Inc.

DRAWING NUMBER: 051-9889 SIZE: D

REVISION: 13.0.0

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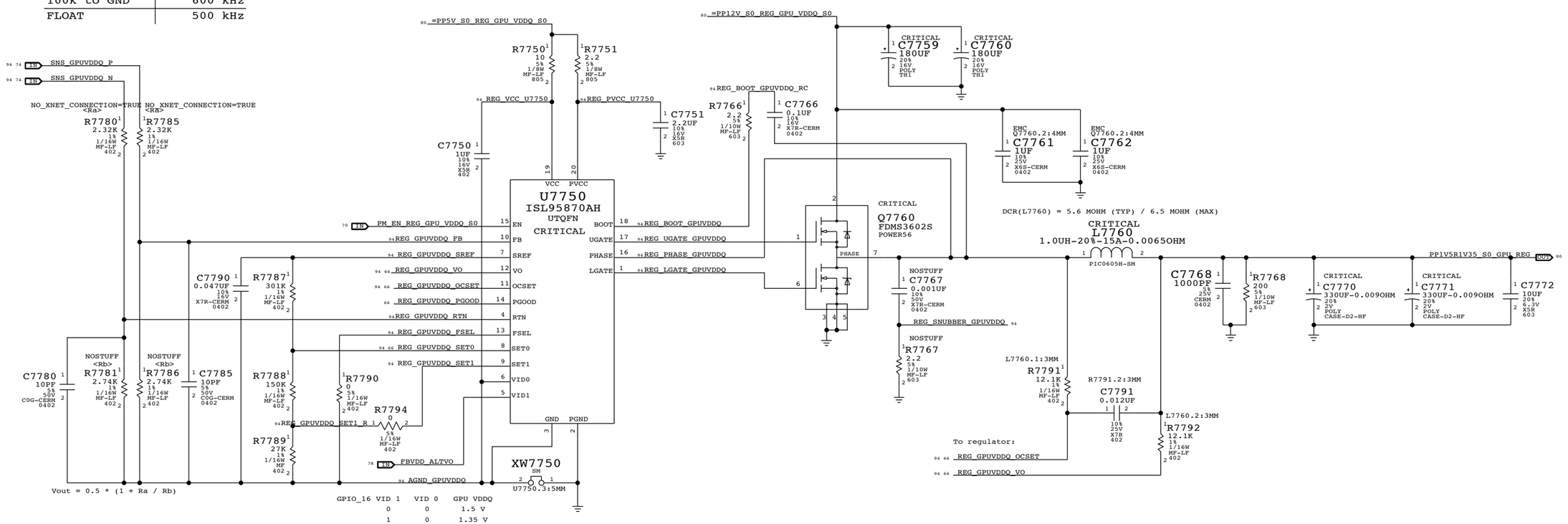
GPU VDDQ S0 REGULATOR

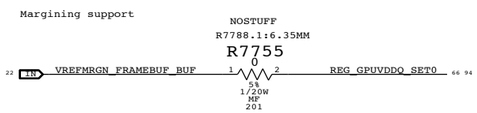
OC trip point: 15.8 A = $\frac{\text{R7791} * 8.5\ \text{E-6}}{\text{DCR(L7760)}}$

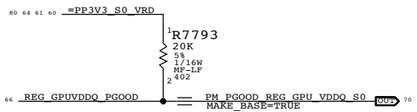
Switching freq: 300 kHz

FSEL STRAP	SW FREQ
GND	300 kHz
VCC	1 MHz
100k to GND	600 kHz
FLOAT	500 kHz



Margining support





SYNC MASTER=J16_DG SYNC DATE=04/21/2013

PAGE TITLE: VReg GPU VDDQ

Apple Inc.

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REVISION: 13.0.0

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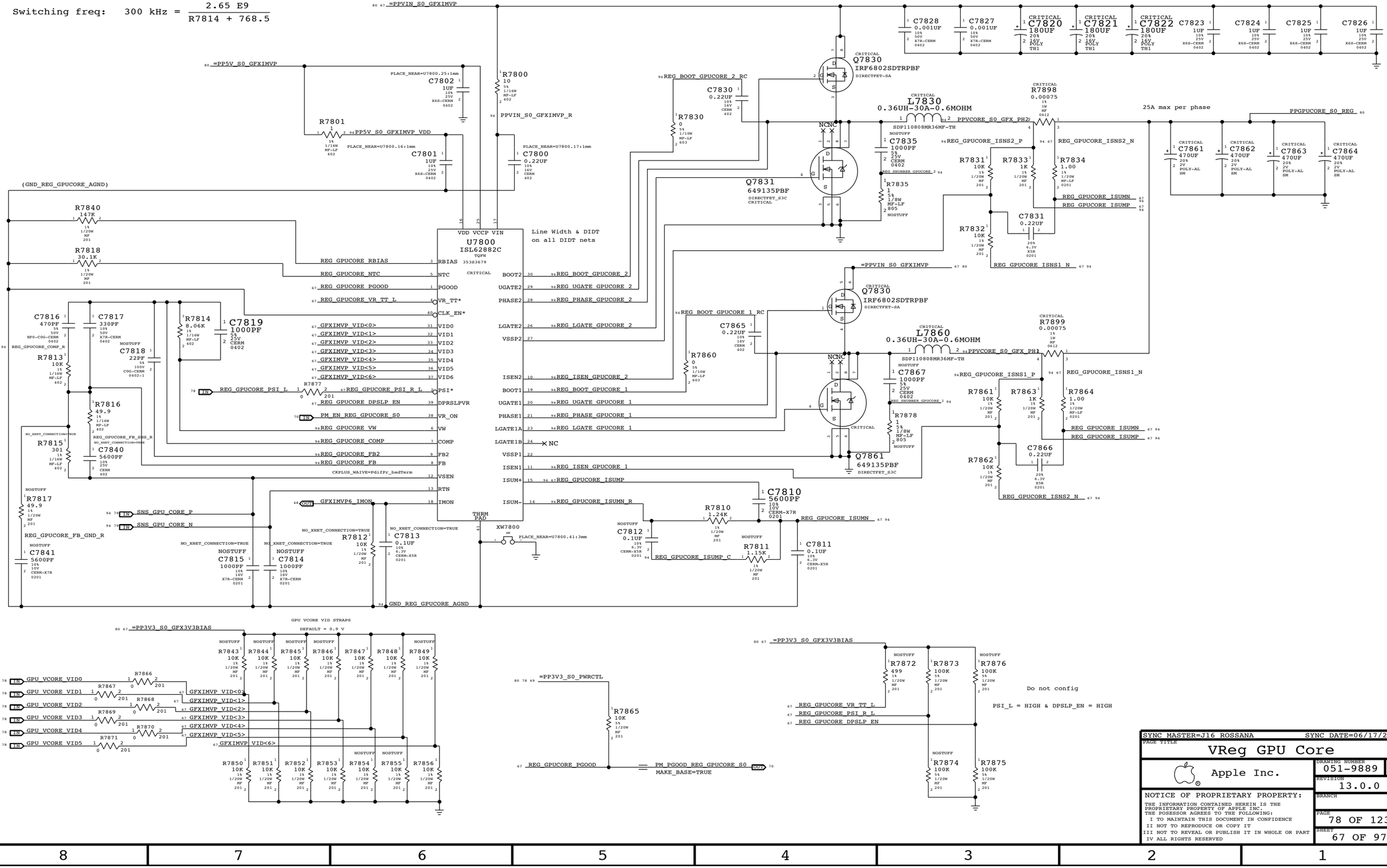
GPU Core S0 Regulator

OC trip point: 66.79 A

Switching freq: 300 kHz = $\frac{2.65\ E9}{R7814 + 768.5}$



SYNC MASTER=J16 ROSSANA	SYNC DATE=06/17/2013
PAGE TITLE	VReg GPU Core
Apple Inc.	DRAWING NUMBER 051-9889 SIZE D
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1668	1	IND,PWR,33UH,20%,10A,35MOHM	L8100	CRITICAL	

OMIT/table L8100 due to late sourcing change, did not want footprint change
Add 152s1668 (Cyntec) directly for next program

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
371S0648	371S0694		D8100	BLC Switch Diode

ACOUSTICS E-NOISE COMPONENTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0810	138S0839		2.2UF_CAP	BLC OUTPUT CAPS

371S0748	371S0731		D8101	INPUT DIODE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1071	376S1073		ALL	Short Protection FET
155S0831	155S0797		ALL	FB8100 to FB8107

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1121	376S1116		Q8102	BLC Inrush FET
740S0145	740S0146		F8100	BLC Fuse

SYNC_MASTER=J16_MLB_IG SYNC_DATE=05/01/2013

PAGE TITLE
LCD Backlight Driver (LP8561)

Apple Inc.

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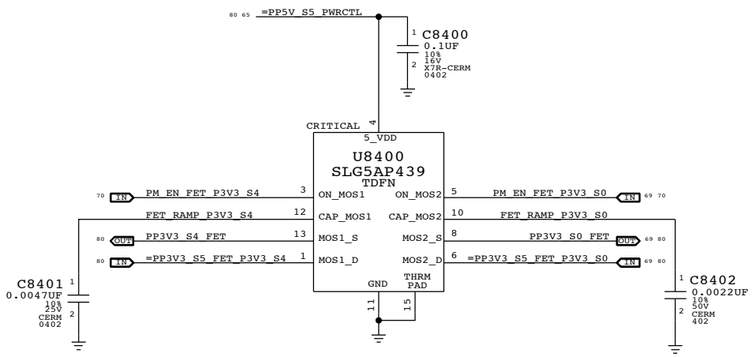
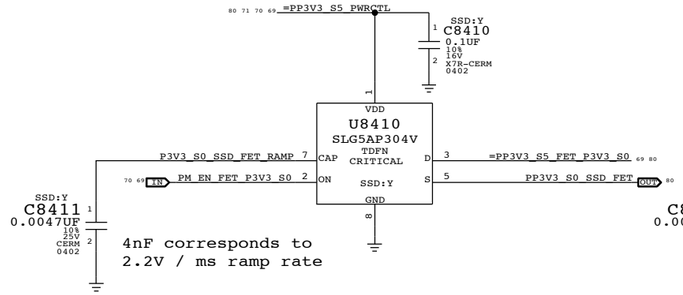
3.3V S4 FET

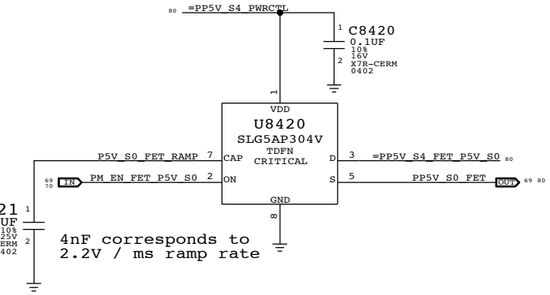


3.3V S0 FET

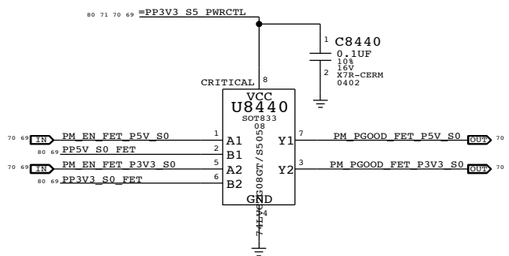
3V3 S0 SSD



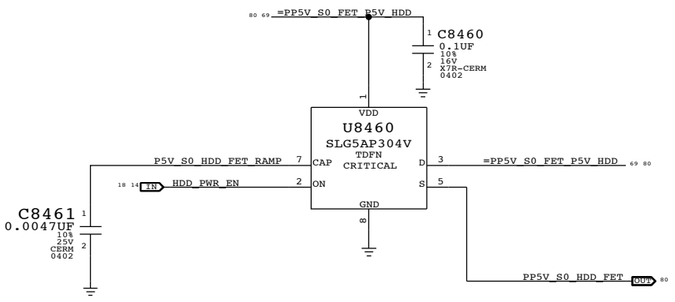
5V S0 FET



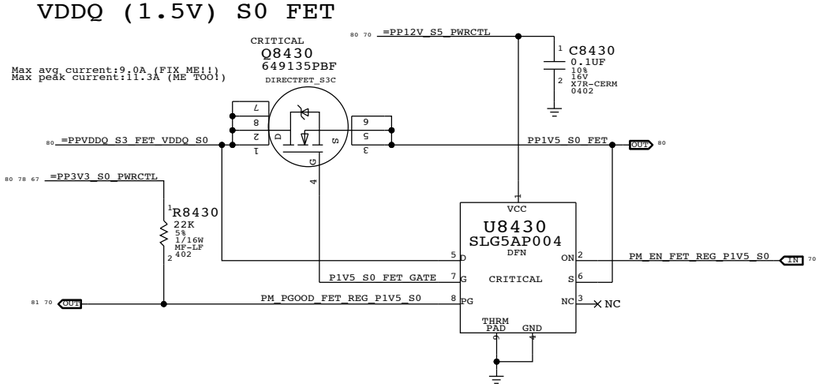
5V / 3V3 S0 PGOODs



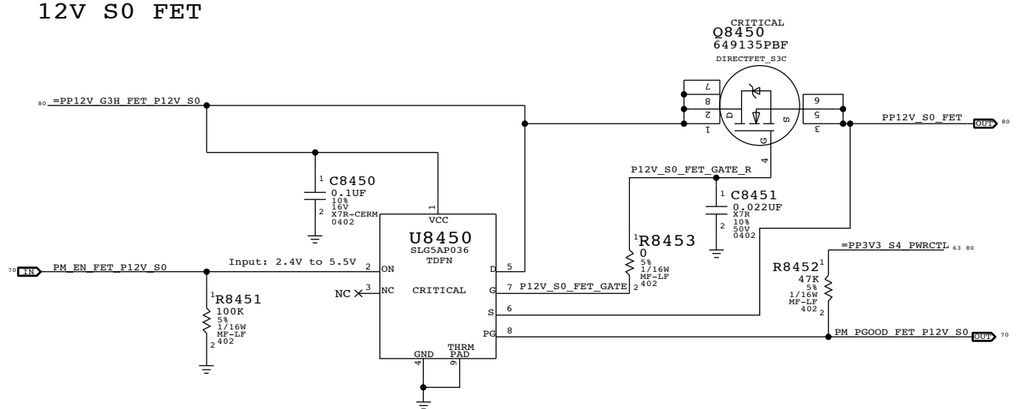
5V HDD FET



VDDQ (1.5V) S0 FET



12V S0 FET



SYNC_MASTER=MASTER	SYNC_DATE=05/01/2013
PAGE TITLE	FET-Controlled S0 and S4
Apple Inc.	DRAWING NUMBER 051-9889 · SIZE D
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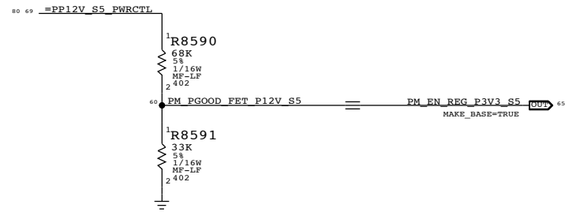
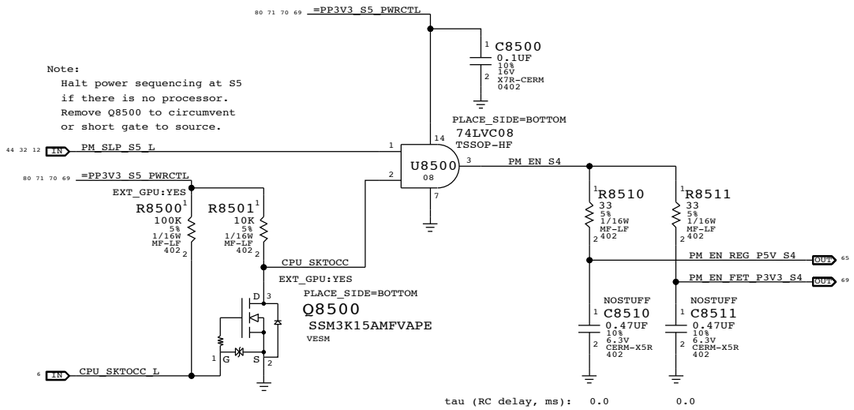
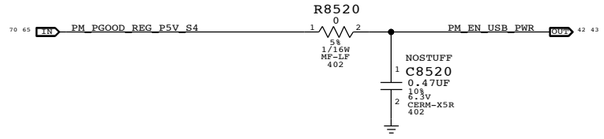
S5 Enable



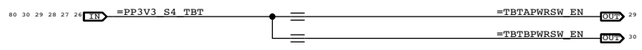
S4 Enables



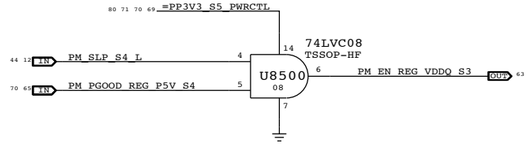
S4 USB Enable



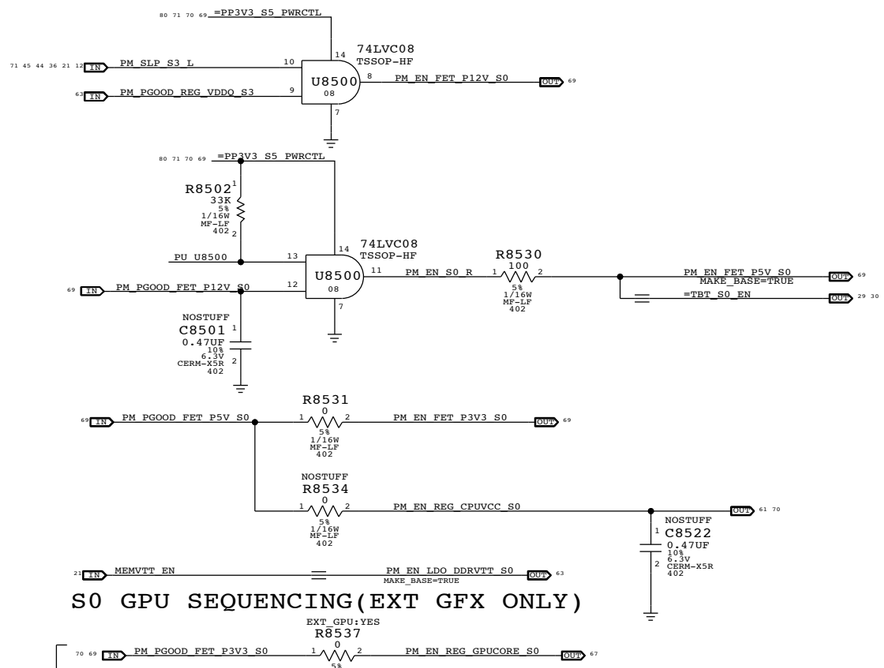
S4 TBT S4 Port Enable



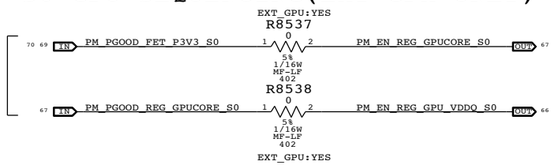
S3 VDDQ Enable



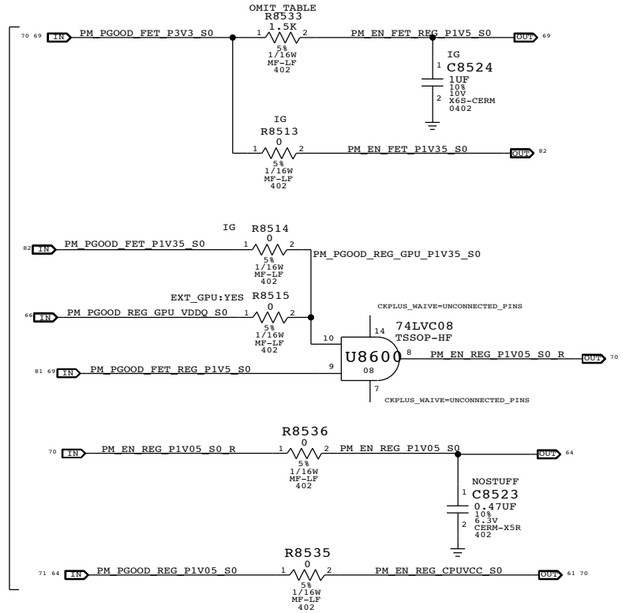
S0 Enables



S0 GPU SEQUENCING(EXT GFX ONLY)



S0 PCH Sequencing



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0070	1	RES,1.5K,0402,5%	R8533	IG
116S0004	1	RES,0OHM,0402,5%	R8533	EXT_GPU:YES

Rail definitions

Platform: All processor non-Core and non-Graphics (5 V, 3.3 V, 1.5 V, 1.05V for PCH/TBT/GPU)
Uncore: VDDQ

Notes on sequencing requirements

Intel:
1. No hard specification on platform rails
2. SMC guarantees timing on PCH DPWROK and PWROK
3. VCC3_3 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC3V3 ramping to 2.6V
4. VCC1_5 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC1V5 ramping to 1.35V
5. VCC may power down before VCC3_3, VCC3_3 must ramp down to 2.6V within 35ms
6. VCC may power down before VCC1_5, VCC1_5 must ramp down to 1.35V within 35ms

NVIDIA:
1. 3V3_S0 must ramp first
4. VDDQ MUST RAMP AFTER GPU_CORE
5. PEX_VDD with IFPC/D/E/F_IOVDD (1.05V) must ramp after VDDQ
6. All rails must reach their target voltages in more than 40 uS

SYNC_MASTER=MASTER SYNC_DATE=05/01/2013

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PM Regulator Enables

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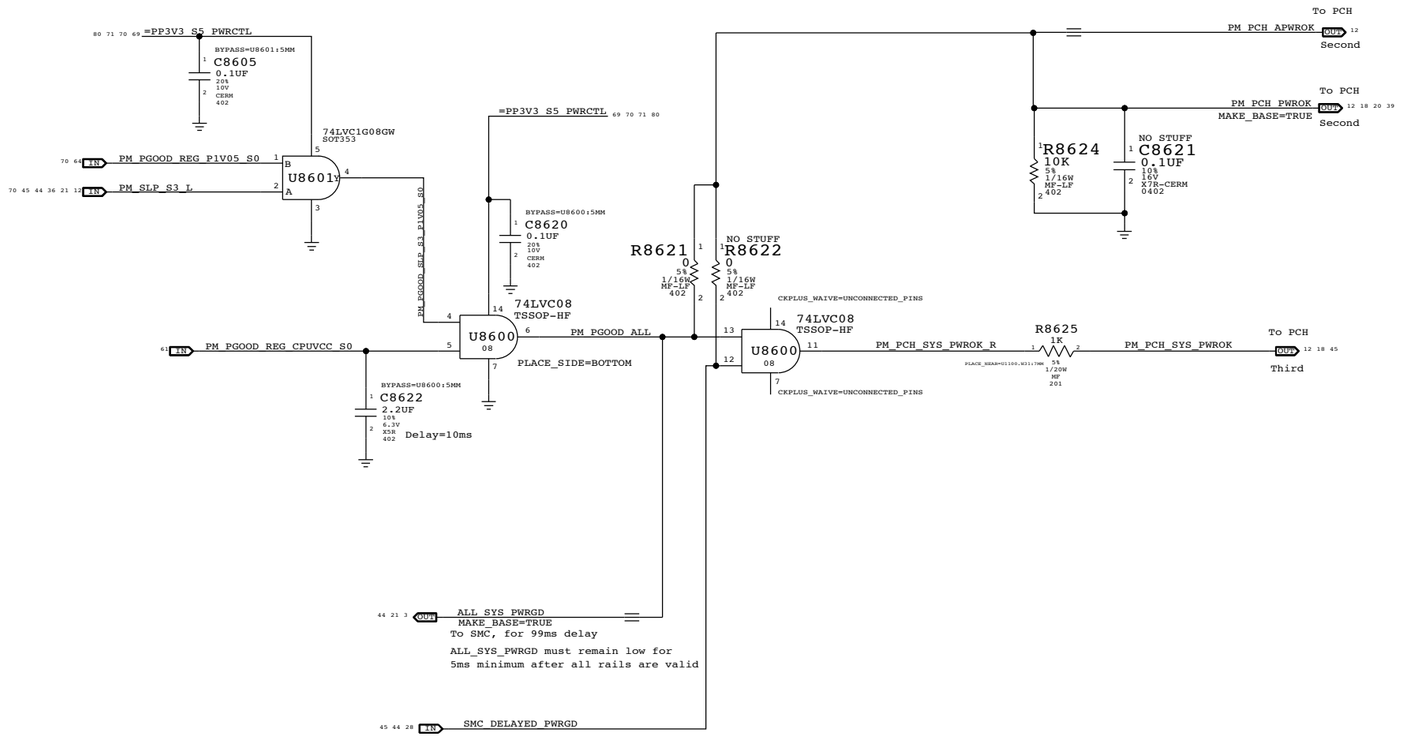
ALL_SYS_PWRGD,PCH_PWROK & SYS_PWROK Generation

PCH Power Goods



Resume Reset

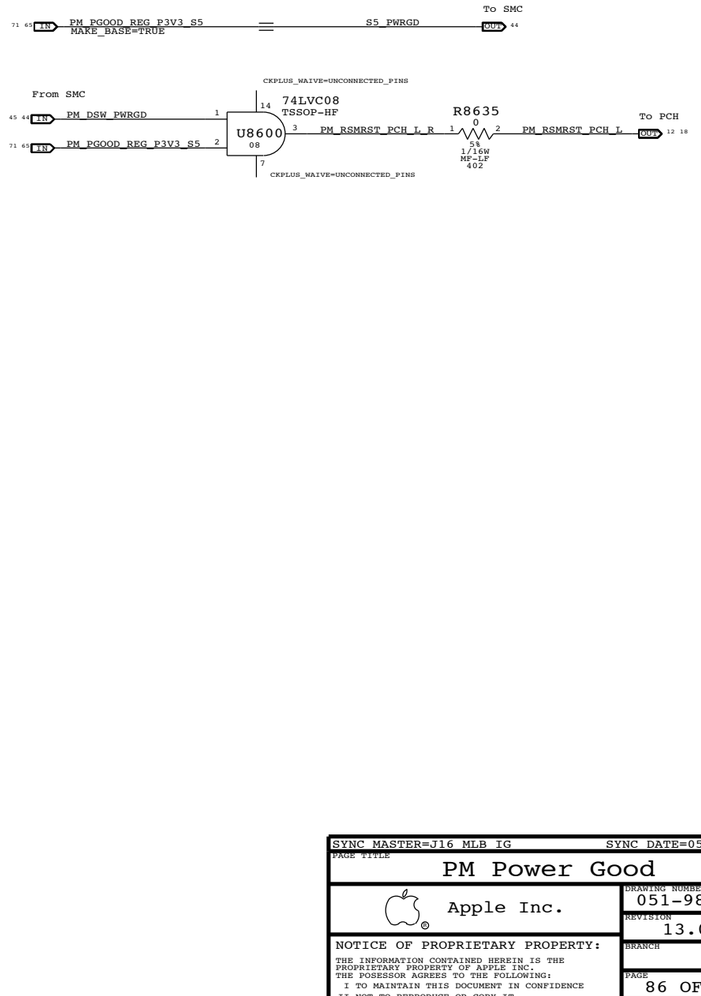
Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

Note:
The iMac J16/J17 designs does not support Deep Sx modes so both DPWROK and RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V to allow PCH to switch suspend well to battery without excessive loading

Method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.



SYNC MASTER=J16 MLB IG SYNC DATE=05/01/2013

PAGE TITLE
PM Power Good

Apple Inc.

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Page Notes

power aliases required by this page:

- +PP3V3_GPU_VDD33

signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

POLARITY SWAPS INTENDED ON LANES,SEE NOTES AT DIFF PAIRS.
ALL LANES ARE ALSO REVERSED, SEE ALIASES ON CSA 102

86 81	PEG_R2D_C_P<0>	C8720	0.22UF	PEG_R2D_N<0>	72 86		
86 81	PEG_R2D_C_N<0>	C8721	0.22UF	PEG_R2D_P<0>	72 86		
86 81	PEG_R2D_C_P<1>	C8722	0.22UF	PEG_R2D_P<1>	72 86		
86 81	PEG_R2D_C_N<1>	C8723	0.22UF	PEG_R2D_N<1>	72 86		
86 81	PEG_R2D_C_P<2>	C8724	0.22UF	PEG_R2D_P<2>	72 86		
86 81	PEG_R2D_C_N<2>	C8725	0.22UF	PEG_R2D_N<2>	72 86		
86 81	PEG_R2D_C_P<3>	C8726	0.22UF	PEG_R2D_P<3>	72 86		
86 81	PEG_R2D_C_N<3>	C8727	0.22UF	PEG_R2D_N<3>	72 86		
86 81	PEG_R2D_C_P<4>	C8728	0.22UF	PEG_R2D_P<4>	72 86		
86 81	PEG_R2D_C_N<4>	C8729	0.22UF	PEG_R2D_N<4>	72 86		
86 81	PEG_R2D_C_P<5>	C8730	0.22UF	PEG_R2D_N<5>	72 86		
86 81	PEG_R2D_C_N<5>	C8731	0.22UF	PEG_R2D_P<5>	72 86	Polarity swapped!!	
86 81	PEG_R2D_C_P<6>	C8732	0.22UF	PEG_R2D_P<6>	72 86		
86 81	PEG_R2D_C_N<6>	C8733	0.22UF	PEG_R2D_N<6>	72 86		
86 81	PEG_R2D_C_P<7>	C8734	0.22UF	PEG_R2D_P<7>	72 86		
86 81	PEG_R2D_C_N<7>	C8735	0.22UF	PEG_R2D_N<7>	72 86		

86 81	PEG_R2D_C_P<8>	C8736	0.22UF	PEG_R2D_N<8>	72 86		
86 81	PEG_R2D_C_N<8>	C8737	0.22UF	PEG_R2D_P<8>	72 86		
86 81	PEG_R2D_C_P<9>	C8738	0.22UF	PEG_R2D_N<9>	72 86		
86 81	PEG_R2D_C_N<9>	C8739	0.22UF	PEG_R2D_P<9>	72 86	Polarity swapped!!	
86 81	PEG_R2D_C_P<10>	C8740	0.22UF	PEG_R2D_P<10>	72 86		
86 81	PEG_R2D_C_N<10>	C8741	0.22UF	PEG_R2D_N<10>	72 86		
86 81	PEG_R2D_C_P<11>	C8742	0.22UF	PEG_R2D_P<11>	72 86		
86 81	PEG_R2D_C_N<11>	C8743	0.22UF	PEG_R2D_N<11>	72 86		
86 81	PEG_R2D_C_P<12>	C8744	0.22UF	PEG_R2D_P<12>	72 86		
86 81	PEG_R2D_C_N<12>	C8745	0.22UF	PEG_R2D_N<12>	72 86		
86 81	PEG_R2D_C_P<13>	C8746	0.22UF	PEG_R2D_N<13>	72 86		
86 81	PEG_R2D_C_N<13>	C8747	0.22UF	PEG_R2D_P<13>	72 86	Polarity swapped!!	
86 81	PEG_R2D_C_P<14>	C8748	0.22UF	PEG_R2D_P<14>	72 86		
86 81	PEG_R2D_C_N<14>	C8749	0.22UF	PEG_R2D_N<14>	72 86		
86 81	PEG_R2D_C_P<15>	C8750	0.22UF	PEG_R2D_P<15>	72 86		
86 81	PEG_R2D_C_N<15>	C8751	0.22UF	PEG_R2D_N<15>	72 86		

86 72	PEG_R2D_C_N<0>	C8755	0.22UF	PEG_D2R_P<0>	81 86		
86 72	PEG_R2D_C_P<0>	C8756	0.22UF	PEG_D2R_N<0>	81 86	Polarity swapped!!	
86 72	PEG_R2D_C_P<1>	C8757	0.22UF	PEG_D2R_P<1>	81 86		
86 72	PEG_R2D_C_N<1>	C8758	0.22UF	PEG_D2R_N<1>	81 86		
86 72	PEG_R2D_C_P<2>	C8759	0.22UF	PEG_D2R_P<2>	81 86		
86 72	PEG_R2D_C_N<2>	C8760	0.22UF	PEG_D2R_N<2>	81 86		
86 72	PEG_R2D_C_P<3>	C8761	0.22UF	PEG_D2R_P<3>	81 86		
86 72	PEG_R2D_C_N<3>	C8762	0.22UF	PEG_D2R_N<3>	81 86		
86 72	PEG_R2D_C_P<4>	C8763	0.22UF	PEG_D2R_P<4>	81 86		
86 72	PEG_R2D_C_N<4>	C8764	0.22UF	PEG_D2R_N<4>	81 86		
86 72	PEG_R2D_C_P<5>	C8765	0.22UF	PEG_D2R_P<5>	81 86		
86 72	PEG_R2D_C_N<5>	C8766	0.22UF	PEG_D2R_N<5>	81 86	Polarity swapped!!	
86 72	PEG_R2D_C_P<6>	C8767	0.22UF	PEG_D2R_P<6>	81 86		
86 72	PEG_R2D_C_N<6>	C8768	0.22UF	PEG_D2R_N<6>	81 86		
86 72	PEG_R2D_C_N<7>	C8769	0.22UF	PEG_D2R_N<7>	81 86		
86 72	PEG_R2D_C_P<7>	C8770	0.22UF	PEG_D2R_P<7>	81 86		

86 72	PEG_R2D_C_N<8>	C8771	0.22UF	PEG_D2R_P<8>	81 86		
86 72	PEG_R2D_C_P<8>	C8772	0.22UF	PEG_D2R_N<8>	81 86	Polarity swapped!!	
86 72	PEG_R2D_C_P<9>	C8773	0.22UF	PEG_D2R_P<9>	81 86		
86 72	PEG_R2D_C_N<9>	C8774	0.22UF	PEG_D2R_N<9>	81 86	Polarity swapped!!	
86 72	PEG_R2D_C_P<10>	C8775	0.22UF	PEG_D2R_P<10>	81 86		
86 72	PEG_R2D_C_N<10>	C8776	0.22UF	PEG_D2R_N<10>	81 86		
86 72	PEG_R2D_C_P<11>	C8777	0.22UF	PEG_D2R_N<11>	81 86		
86 72	PEG_R2D_C_N<11>	C8778	0.22UF	PEG_D2R_P<11>	81 86	Polarity swapped!!	
86 72	PEG_R2D_C_P<12>	C8779	0.22UF	PEG_D2R_P<12>	81 86		
86 72	PEG_R2D_C_N<12>	C8780	0.22UF	PEG_D2R_N<12>	81 86		
86 72	PEG_R2D_C_P<13>	C8781	0.22UF	PEG_D2R_P<13>	81 86		
86 72	PEG_R2D_C_N<13>	C8782	0.22UF	PEG_D2R_N<13>	81 86		
86 72	PEG_R2D_C_P<14>	C8783	0.22UF	PEG_D2R_P<14>	81 86		
86 72	PEG_R2D_C_N<14>	C8784	0.22UF	PEG_D2R_N<14>	81 86		
86 72	PEG_R2D_C_P<15>	C8785	0.22UF	PEG_D2R_P<15>	81 86		
86 72	PEG_R2D_C_N<15>	C8786	0.22UF	PEG_D2R_N<15>	81 86		

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86 72	PEG_R2D_P<0>	AN12	PEX_RX0	PEX_TX0	AK14	PEG_D2R_C_P<0> 72 86
86 72	PEG_R2D_N<0>	AM12	PEX_RX0*	PEX_TX0*	AJ14	PEG_D2R_C_N<0> 72 86
86 72	PEG_R2D_P<1>	AN14	PEX_RX1	PEX_TX1	AH14	PEG_D2R_C_P<1> 72 86
86 72	PEG_R2D_N<1>	AM14	PEX_RX1*	PEX_TX1*	AG14	PEG_D2R_C_N<1> 72 86
86 72	PEG_R2D_P<2>	AP14	PEX_RX2	PEX_TX2	AK15	PEG_D2R_C_P<2> 72 86
86 72	PEG_R2D_N<2>	AP15	PEX_RX2*	PEX_TX2*	AJ15	PEG_D2R_C_N<2> 72 86
86 72	PEG_R2D_P<3>	AN15	PEX_RX3	PEX_TX3	AL16	PEG_D2R_C_P<3> 72 86
86 72	PEG_R2D_N<3>	AM15	PEX_RX3*	PEX_TX3*	AK16	PEG_D2R_C_N<3> 72 86
86 72	PEG_R2D_P<4>	AN17	PEX_RX4	PEX_TX4	AK17	PEG_D2R_C_P<4> 72 86
86 72	PEG_R2D_N<4>	AM17	PEX_RX4*	PEX_TX4*	AJ17	PEG_D2R_C_N<4> 72 86
86 72	PEG_R2D_P<5>	AP17	PEX_RX5	PEX_TX5	AH17	PEG_D2R_C_P<5> 72 86
86 72	PEG_R2D_N<5>	AP18	PEX_RX5*	PEX_TX5*	AG17	PEG_D2R_C_N<5> 72 86
86 72	PEG_R2D_P<6>	AN18	PEX_RX6	PEX_TX6	AK18	PEG_D2R_C_P<6> 72 86
86 72	PEG_R2D_N<6>	AM18	PEX_RX6*	PEX_TX6*	AJ18	PEG_D2R_C_N<6> 72 86
86 72	PEG_R2D_P<7>	AN20	PEX_RX7	PEX_TX7	AL19	PEG_D2R_C_P<7> 72 86
86 72	PEG_R2D_N<7>	AM20	PEX_RX7*	PEX_TX7*	AK19	PEG_D2R_C_N<7> 72 86
86 72	PEG_R2D_P<8>	AP20	PEX_RX8	PEX_TX8	AK20	PEG_D2R_C_P<8> 72 86
86 72	PEG_R2D_N<8>	AP21	PEX_RX8*	PEX_TX8*	AJ20	PEG_D2R_C_N<8> 72 86
86 72	PEG_R2D_P<9>	AN21	PEX_RX9	PEX_TX9	AH20	PEG_D2R_C_P<9> 72 86
86 72	PEG_R2D_N<9>	AM21	PEX_RX9*	PEX_TX9*	AG20	PEG_D2R_C_N<9> 72 86
86 72	PEG_R2D_P<10>	AN23	PEX_RX10	PEX_TX10	AK21	PEG_D2R_C_P<10> 72 86
86 72	PEG_R2D_N<10>	AM23	PEX_RX10*	PEX_TX10*	AJ21	PEG_D2R_C_N<10> 72 86
86 72	PEG_R2D_P<11>	AP23	PEX_RX11	PEX_TX11	AL22	PEG_D2R_C_P<11> 72 86
86 72	PEG_R2D_N<11>	AP24	PEX_RX11*	PEX_TX11*	AK22	PEG_D2R_C_N<11> 72 86
86 72	PEG_R2D_P<12>	AN24	PEX_RX12	PEX_TX12	AK23	PEG_D2R_C_P<12> 72 86
86 72	PEG_R2D_N<12>	AM24	PEX_RX12*	PEX_TX12*	AJ23	PEG_D2R_C_N<12> 72 86
86 72	PEG_R2D_P<13>	AN26	PEX_RX13	PEX_TX13	AH23	PEG_D2R_C_P<13> 72 86
86 72	PEG_R2D_N<13>	AM26	PEX_RX13*	PEX_TX13*	AG23	PEG_D2R_C_N<13> 72 86
86 72	PEG_R2D_P<14>	AP26	PEX_RX14	PEX_TX14	AK24	PEG_D2R_C_P<14> 72 86
86 72	PEG_R2D_N<14>	AP27	PEX_RX14*	PEX_TX14*	AJ24	PEG_D2R_C_N<14> 72 86
86 72	PEG_R2D_P<15>	AN27	PEX_RX15	PEX_TX15	AL25	PEG_D2R_C_P<15> 72 86
86 72	PEG_R2D_N<15>	AM27	PEX_RX15*	PEX_TX15*	AK25	PEG_D2R_C_N<15> 72 86
86 11	PEG_CLK100M_P	AL13	PEX_REFCLK	PEX_TSTCLK_OUT	AJ26	96 PEX_TSTCLK_O_PL
86 11	PEG_CLK100M_N	AK13	PEX_REFCLK*	PEX_TSTCLK_OUT*	AK26	96 PEX_TSTCLK_O_NG
78 20	GPU_RESET_L	AJ12	PEX_RST*	PEX_TERMP	AP29	96 GPU_PEX_TERMP
11	PEG_CLKREQ_L	AK12	PEX_CLKREQ*			
NC		AJ11	PEX_WAKE*	PEX_SVDD_3V3	AG12	+PP3V3_GPU_VDD33 77 78 79 80

R8702 200 1% 1/10W MF 201 — NOSTUFF — PLACE_NEAR=U8700.AJ26:8MM

R8700 0 GPU_RESET_R_L 1% MF 1/20W 201

R8705 2.49K 1% 1/20W MF 201 — PLACE_NEAR=U8700.AP29:8MM

SYNC_MASTER=J16_DG	SYNC_DATE=04/21/2013
PAGE TITLE	KEPLER PCI-E
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	REVISION 13.0.0
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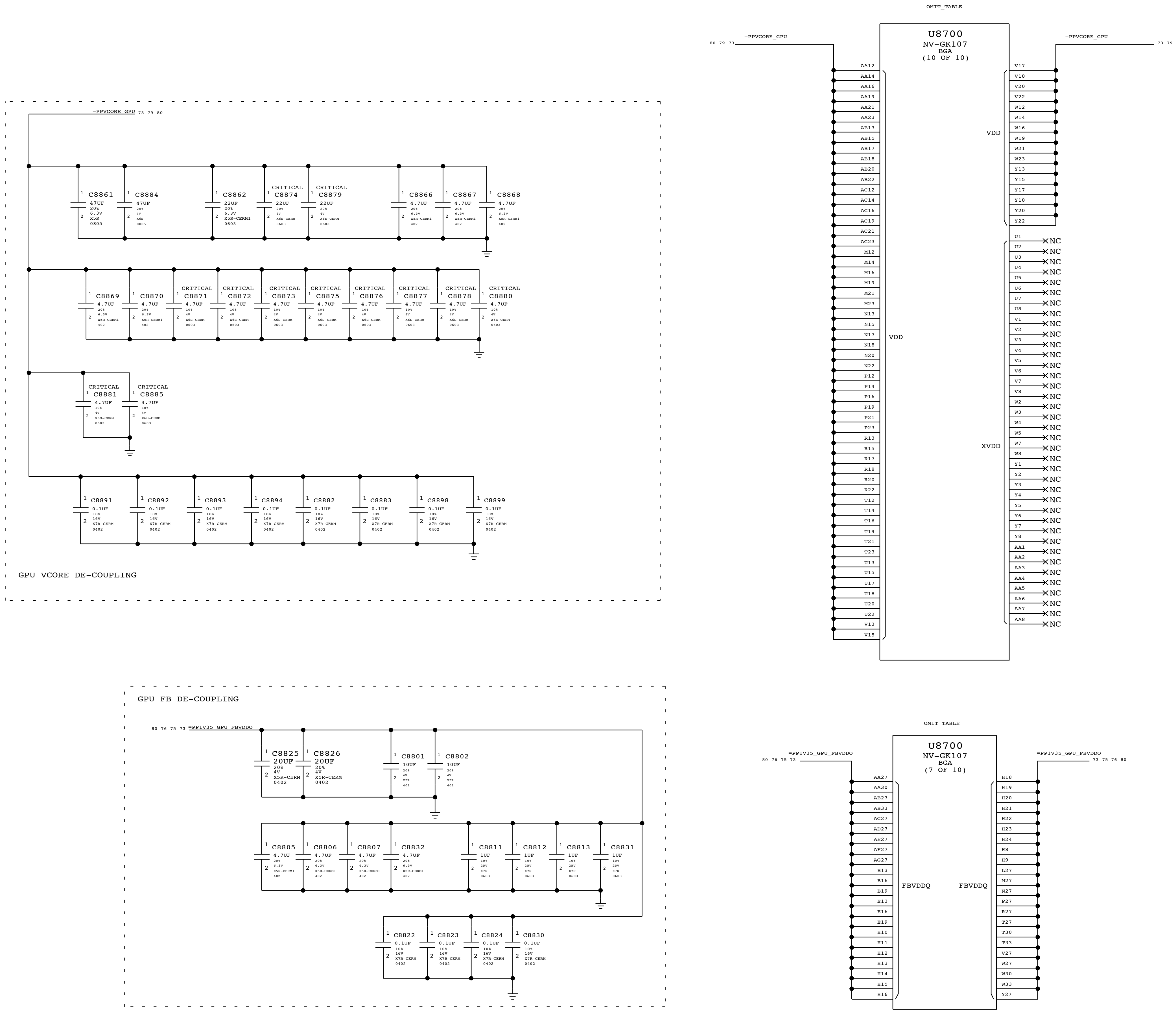

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NOTE:GDDR5 MODE N MAPPING

OMIT_TABLE

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MEM INTERFACE A

FBA_D0 FBA_D1 FBA_D2 FBA_D3 FBA_D4 FBA_D5 FBA_D6 FBA_D7 FBA_D8 FBA_D9 FBA_D10 FBA_D11 FBA_D12 FBA_D13 FBA_D14 FBA_D15 FBA_D16 FBA_D17 FBA_D18 FBA_D19 FBA_D20 FBA_D21 FBA_D22 FBA_D23 FBA_D24 FBA_D25 FBA_D26 FBA_D27 FBA_D28 FBA_D29 FBA_D30 FBA_D31 FBA_D32 FBA_D33 FBA_D34 FBA_D35 FBA_D36 FBA_D37 FBA_D38 FBA_D39 FBA_D40 FBA_D41 FBA_D42 FBA_D43 FBA_D44 FBA_D45 FBA_D46 FBA_D47 FBA_D48 FBA_D49 FBA_D50 FBA_D51 FBA_D52 FBA_D53 FBA_D54 FBA_D55 FBA_D56 FBA_D57 FBA_D58 FBA_D59 FBA_D60 FBA_D61 FBA_D62 FBA_D63

FBA_WCK01 FBA_WCK01* FBA_WCK23 FBA_WCK23* FBA_WCK45 FBA_WCK45* FBA_WCK67 FBA_WCK67*

FBA_WCKB01 FBA_WCKB01* FBA_WCKB23 FBA_WCKB23* FBA_WCKB45 FBA_WCKB45* FBA_WCKB67 FBA_WCKB67*

FBA_CMD0 FBA_CMD1 FBA_CMD2 FBA_CMD3 FBA_CMD4 FBA_CMD5 FBA_CMD6 FBA_CMD7 FBA_CMD8 FBA_CMD9 FBA_CMD10 FBA_CMD11 FBA_CMD12 FBA_CMD13 FBA_CMD14 FBA_CMD15 FBA_CMD16 FBA_CMD17 FBA_CMD18 FBA_CMD19 FBA_CMD20 FBA_CMD21 FBA_CMD22 FBA_CMD23 FBA_CMD24 FBA_CMD25 FBA_CMD26 FBA_CMD27 FBA_CMD28 FBA_CMD29 FBA_CMD30 FBA_CMD31

FBA_CLK0 FBA_CLK0* FBA_CLK1 FBA_CLK1*

FBA_DQM0 FBA_DQM1 FBA_DQM2 FBA_DQM3 FBA_DQM4 FBA_DQM5 FBA_DQM6 FBA_DQM7

FBA_DQS_RN0 FBA_DQS_RN1 FBA_DQS_RN2 FBA_DQS_RN3 FBA_DQS_RN4 FBA_DQS_RN5 FBA_DQS_RN6 FBA_DQS_RN7 (NC)

FBA_DQS_WP0 FBA_DQS_WP1 FBA_DQS_WP2 FBA_DQS_WP3 FBA_DQS_WP4 FBA_DQS_WP5 FBA_DQS_WP6 FBA_DQS_WP7

FBA_DLL_AVDD (PP1V05_GPU_FB_DLL_AVDD) FBA_PLL_AVDD (PP1V05_GPU_FB_PLL_AVDD)

FBA_DEBUG (GPU_FBA_DEBUG0) FBA_DEBUG (GPU_FBA_DEBUG1)

FB_CAL_PD_VDDQ (FB_CAL_PD_VDDQ) FB_CAL_PU_GND (FB_CAL_PU_GND) FB_CAL_TERM_GND (FB_CAL_TERM_GND) FB_CLAMP (FB_CLAMP) FBA_CMD_RFU FBA_CMD_RFU

FB_VDDQ_SENSE → SNS_GPUVDDQ_P

FB_GND_SENSE → SNS_GPUVDDQ_N

R9050 10K 1% 1/20W MF 201 — FB_A0_RESET_L
R9051 10K 1% 1/20W MF 201 — FB_A1_RESET_L
R9052 10K 1% 1/20W MF 201 — FB_A0_CKE_L
R9053 10K 1% 1/20W MF 201 — FB_A1_CKE_L

FB VREF GEN (TEST ONLY)
=PP1V35_GPU_S0_FB
R9058 1.33K 1% 1/20W MF 201 (NOSTUFF)
FB_VREF
R9059 1.33K 1% 1/20W MF 201 (NOSTUFF)
C9060 0.1UF 10% 6.3V CERM-X5R 0201 (NOSTUFF)

R9003 60.4 1% 1/20W MF 201 (NOSTUFF)
R9002 60.4 1% 1/20W MF 201 (NOSTUFF)
R9070 100 5% 1/20W MF 201 (NOSTUFF)
R9071 100 5% 1/20W MF 201 (NOSTUFF)
R9001 60.4 1% 1/20W MF 201
R9061 10K 1% 1/20W MF 201
R9004 40.2 1% 1/20W MF 201
R9005 40.2 1% 1/20W MF 201

PLACE CLOSE TO BGA

OMIT_TABLE

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MEM INTRERFACE B

FBB_D0 FBB_D1 FBB_D2 FBB_D3 FBB_D4 FBB_D5 FBB_D6 FBB_D7 FBB_D8 FBB_D9 FBB_D10 FBB_D11 FBB_D12 FBB_D13 FBB_D14 FBB_D15 FBB_D16 FBB_D17 FBB_D18 FBB_D19 FBB_D20 FBB_D21 FBB_D22 FBB_D23 FBB_D24 FBB_D25 FBB_D26 FBB_D27 FBB_D28 FBB_D29 FBB_D30 FBB_D31 FBB_D32 FBB_D33 FBB_D34 FBB_D35 FBB_D36 FBB_D37 FBB_D38 FBB_D39 FBB_D40 FBB_D41 FBB_D42 FBB_D43 FBB_D44 FBB_D45 FBB_D46 FBB_D47 FBB_D48 FBB_D49 FBB_D50 FBB_D51 FBB_D52 FBB_D53 FBB_D54 FBB_D55 FBB_D56 FBB_D57 FBB_D58 FBB_D59 FBB_D60 FBB_D61 FBB_D62 FBB_D63

FBB_WCK01 FBB_WCK01* FBB_WCK23 FBB_WCK23* FBB_WCK45 FBB_WCK45* FBB_WCK67 FBB_WCK67*

FBB_WCKB01 FBB_WCKB01* FBB_WCKB23 FBB_WCKB23* FBB_WCKB45 FBB_WCKB45* FBB_WCKB67 FBB_WCKB67*

FBB_CMD0 FBB_CMD1 FBB_CMD2 FBB_CMD3 FBB_CMD4 FBB_CMD5 FBB_CMD6 FBB_CMD7 FBB_CMD8 FBB_CMD9 FBB_CMD10 FBB_CMD11 FBB_CMD12 FBB_CMD13 FBB_CMD14 FBB_CMD15 FBB_CMD16 FBB_CMD17 FBB_CMD18 FBB_CMD19 FBB_CMD20 FBB_CMD21 FBB_CMD22 FBB_CMD23 FBB_CMD24 FBB_CMD25 FBB_CMD26 FBB_CMD27 FBB_CMD28 FBB_CMD29 FBB_CMD30 FBB_CMD31

FBB_CLK0 FBB_CLK0* FBB_CLK1 FBB_CLK1*

FBB_DQM0 FBB_DQM1 FBB_DQM2 FBB_DQM3 FBB_DQM4 FBB_DQM5 FBB_DQM6 FBB_DQM7

FBB_DQS_RN0 FBB_DQS_RN1 FBB_DQS_RN2 FBB_DQS_RN3 FBB_DQS_RN4 FBB_DQS_RN5 FBB_DQS_RN6 FBB_DQS_RN7 (NC)

FBB_DQS_WP0 FBB_DQS_WP1 FBB_DQS_WP2 FBB_DQS_WP3 FBB_DQS_WP4 FBB_DQS_WP5 FBB_DQS_WP6 FBB_DQS_WP7

FBB_PLL_AVDD (PP1V05_GPU_FB_PLL_AVDD) FBB_DEBUG0 (GPU_FBB_DEBUG0) FBB_DEBUG1 (GPU_FBB_DEBUG1) FB_VREF (FB_VREF) FBB_CMD_RFU0 (NC) FBB_CMD_RFU1 (NC)

C9006 1.0UF 20% 6.3V X5R 0201-1
C9007 0.1UF 10% 16V X7R-CERM 0201

=PP1V35_GPU_S0_FB
R9006 60.4 1% 1/20W MF 201 (NOSTUFF)
R9007 60.4 1% 1/20W MF 201 (NOSTUFF)

Page Notes

Power aliases required by this page:
- =PP1V35_GPU_S0_FB
- =PP1V05_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

L9001 30-OHM-25%-5A-0.01-OHM 0603 CRITICAL ESR = 0.050HM
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V
=PP1V05_GPU_PEX_IOVDD → PP1V05_GPU_FB_PLL_AVDD
C9001 200UF 20% 4V X5R-CERM 0402
C9002 1.0UF 20% 6.3V X5R 0201-1
C9003 0.1UF 10% 16V X7R-CERM 0402
C9004 0.1UF 10% 16V X7R-CERM 0402

L9002 30-OHM-25%-5A-0.01-OHM 0603 CRITICAL ESR = 0.050HM
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V
=PP1V05_GPU_PEX_IOVDD → PP1V05_GPU_FB_DLL_AVDD
C9008 200UF 20% 4V X5R-CERM 0402
C9009 1.0UF 20% 6.3V X5R 0201-1
C9005 0.1UF 10% 16V X7R-CERM 0402

FB PLL & DLL VDD

R9054 10K 1% 1/20W MF 201 — FB_B0_RESET_L
R9055 10K 1% 1/20W MF 201 — FB_B1_RESET_L
R9056 10K 1% 1/20W MF 201 — FB_B0_CKE_L
R9057 10K 1% 1/20W MF 201 — FB_B1_CKE_L

MEM VREFC & VREFD SWITCH

FB_SW_LEG → Q9065 SSM3K15AMFVAPE VESM (CRITICAL) → GPU_ALT_VREF
R9060 10K 5% 1/20W MF 201

SYNC_MASTER=J16_DG SYNC_DATE=04/21/2013

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Page Notes

Power aliases required by this page:

- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

This memory device is in Mirrored Mode.

CK TERMINATION - A0
NO_XNET_CONNECTION=TRUE
PLACE_NEAR=U9200.J11:8MM
R9201 40.2 1% 1/20W MF 201 FBA
R9202 40.2 1% 1/20W MF 201 FBA
C9290 0.01UF 10% 10V X5R-CERM 0201 FBA
PLACE_NEAR=U9200.J12:8MM

CK TERMINATION - A1
NO_XNET_CONNECTION=TRUE
PLACE_NEAR=U9250.J11:8MM
R9251 40.2 1% 1/20W MF 201 FBA
R9252 40.2 1% 1/20W MF 201 FBA
C9291 0.01UF 10% 10V X5R-CERM 0201 FBA
PLACE_NEAR=U9250.J12:8MM

R9200 120 1% 1/20W MF 201 FBA
R9204 120 1% 1/20W MF 201 FBA
R9203 120 1% 1/20W MF 201 FBA

U9200
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)

FB_A0_A<2>	H11	BA0/A2	
FB_A0_A<5>	K10	BA1/A5	
FB_A0_A<4>	K11	BA2/A4	
FB_A0_A<3>	H10	BA3/A3	
FB_A0_A<7>	K4	A8/A7	
FB_A0_A<1>	H5	A9/A1	
FB_A0_A<0>	H4	A10/A0	
FB_A0_A<6>	K5	A11/A6	
FB_A0_CKE_L	J3	CKE*	
FB_A0_CLK_P	J12	CK	
FB_A0_CLK_N	J11	CK*	
FB_A0_CS_L	G12	CS*	
FB_A0_WE_L	L12	WE*	
FB_A0_CAS_L	L3	CAS*	
FB_A0_RAS_L	G3	RAS*	
FB_A0_ZQ	J13	ZQ	
FB_A0_MF	J1	MF (MF=0)	
FB_A0_SEN	J10	SEN	
FB_A0_RESET_L	J2	RESET*	
FB_A0_ABI_L	J4	ABI*	
FB_A0_EDC<0>	C2	EDC0	
FB_A0_EDC<1>	C13	EDC1	
FB_A0_EDC<2>	R13	EDC2	
FB_A0_EDC<3>	R2	EDC3	
FB_A0_WCLK_P<0>	D4	WCK01	
FB_A0_WCLK_N<0>	D5	WCK01*	
FB_A0_WCLK_P<1>	P4	WCK23	
FB_A0_WCLK_N<1>	P5	WCK23*	

DBI0*	D2	FB_A0_DBI_L<0>	
DBI1*	D13	FB_A0_DBI_L<1>	
DBI2*	P13	FB_A0_DBI_L<2>	
DBI3*	P2	FB_A0_DBI_L<3>	
DQ0	A4	FB_A0_DQ<0>	
DQ1	A2	FB_A0_DQ<1>	
DQ2	B4	FB_A0_DQ<2>	
DQ3	B2	FB_A0_DQ<3>	
DQ4	E4	FB_A0_DQ<4>	
DQ5	E2	FB_A0_DQ<5>	
DQ6	F4	FB_A0_DQ<6>	
DQ7	F2	FB_A0_DQ<7>	
DQ8	A11	FB_A0_DQ<8>	
DQ9	A13	FB_A0_DQ<9>	
DQ10	B11	FB_A0_DQ<10>	
DQ11	B13	FB_A0_DQ<11>	
DQ12	E11	FB_A0_DQ<12>	
DQ13	E13	FB_A0_DQ<13>	
DQ14	F11	FB_A0_DQ<14>	
DQ15	F13	FB_A0_DQ<15>	
DQ16	U11	FB_A0_DQ<16>	
DQ17	U13	FB_A0_DQ<17>	
DQ18	T11	FB_A0_DQ<18>	
DQ19	T13	FB_A0_DQ<19>	
DQ20	N11	FB_A0_DQ<20>	
DQ21	N13	FB_A0_DQ<21>	
DQ22	M11	FB_A0_DQ<22>	
DQ23	M13	FB_A0_DQ<23>	
DQ24	U4	FB_A0_DQ<24>	
DQ25	U2	FB_A0_DQ<25>	
DQ26	T4	FB_A0_DQ<26>	
DQ27	T2	FB_A0_DQ<27>	
DQ28	N4	FB_A0_DQ<28>	
DQ29	N2	FB_A0_DQ<29>	
DQ30	M4	FB_A0_DQ<30>	
DQ31	M2	FB_A0_DQ<31>	
NC	A5	NC	
A12/RFU/NC	J5	FB_A0_A<8>	
NC	U5	NC	

OMIT_TABLE

U9200
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(2 OF 2)

=PP1V35_GPU_FBVDDQ	C5	VDD	
	C10		
	D11		
	G1		
	G4		
	G11		
	G14		
	L1		
	L4		
	L11		
	L14		
	P11		
	R5		
	R10		
	B1	VDDQ	
	B3		
	B12		
	B14		
	D1		
	D3		
	D12		
	D14		
	E5		
	E10		
	F1		
	F3		
	F12		
	F14		
	G2		
	G13		
	H3		
	H12		
	K3		
	K12		
	L2		
	L13		
	M1		
	M3		
	M12		
	M14		
	N5		
	N10		
	P1		
	P3		
	P12		
	P14		
	T1		
	T3		
	T12		
	T14		
FB_A0_VREFC	J14	VREFC	
FB_A0_VREFD	A10	VREFD	
	U10		

	B5	
	B10	
	D10	
	G5	
	G10	
	H1	
	H14	
	K1	
	K14	
	L5	
	L10	
	P10	
	T5	
	T10	
VSS	A1	
	A3	
	A12	
	A14	
	C1	
	C3	
	C4	
	C11	
	C12	
	C14	
	E1	
	E3	
	E12	
	E14	
	F5	
	F10	
VSSQ	H2	
	H13	
	K2	
	K13	
	M5	
	M10	
	N1	
	N3	
	N12	
	N14	
	R1	
	R3	
	R4	
	R11	
	R12	
	R14	
	U1	
	U3	
	U12	
	U14	

OMIT_TABLE

PLACE CLOSE TO U9200

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 mm

FB_A0_VREFC
R9230 549 1% 1/20W MF 201 FBA
C9231 820PF 10% 50V CERM 0402 FBA
R9231 1.33K 1% 1/20W MF 201 FBA
R9234 931 1% 1/20W MF 201 FBA
FB_SW_LEG

FB_A0_VREFD
R9232 549 1% 1/20W MF 201 FBA
C9232 820PF 10% 25V X7R-CERM 0201 FBA
C9233 820PF 10% 25V X7R-CERM 0201 FBA
R9233 1.33K 1% 1/20W MF 201 FBA
R9235 931 1% 1/20W MF 201 FBA
FB_SW_LEG

U9250
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(1 OF 2)

FB_A1_A<2>	K11	BA0/A2	
FB_A1_A<5>	H10	BA1/A5	
FB_A1_A<4>	H11	BA2/A4	
FB_A1_A<3>	K10	BA3/A3	
FB_A1_A<7>	H4	A8/A7	
FB_A1_A<1>	K5	A9/A1	
FB_A1_A<0>	K4	A10/A0	
FB_A1_A<6>	H5	A11/A6	
FB_A1_CKE_L	J3	CKE*	
FB_A1_CLK_P	J12	CK	
FB_A1_CLK_N	J11	CK*	
FB_A1_CS_L	L12	CS*	
FB_A1_WE_L	G12	WE*	
FB_A1_CAS_L	G3	CAS*	
FB_A1_RAS_L	L3	RAS*	
FB_A1_ZQ	J13	ZQ	
FB_A1_MF	J1	MF (MF=1)	
FB_A1_SEN	J10	SEN	
FB_A1_RESET_L	J2	RESET*	
FB_A1_ABI_L	J4	ABI*	
FB_A1_EDC<0>	R2	EDC0	
FB_A1_EDC<1>	R13	EDC1	
FB_A1_EDC<2>	C13	EDC2	
FB_A1_EDC<3>	C2	EDC3	
FB_A1_WCLK_P<0>	P4	WCK01	
FB_A1_WCLK_N<0>	P5	WCK01*	
FB_A1_WCLK_P<1>	D4	WCK23	
FB_A1_WCLK_N<1>	D5	WCK23*	

DBI1*	P13	FB_A1_DBI_L<1>	
DBI2*	D13	FB_A1_DBI_L<2>	
DBI0*	P2	FB_A1_DBI_L<0>	
DBI3*	D2	FB_A1_DBI_L<3>	
DQ0	U4	FB_A1_DQ<0>	
DQ1	U2	FB_A1_DQ<1>	
DQ2	T4	FB_A1_DQ<2>	
DQ3	T2	FB_A1_DQ<3>	
DQ4	N4	FB_A1_DQ<4>	
DQ5	N2	FB_A1_DQ<5>	
DQ6	M4	FB_A1_DQ<6>	
DQ7	M2	FB_A1_DQ<7>	
DQ8	U11	FB_A1_DQ<8>	
DQ9	U13	FB_A1_DQ<9>	
DQ10	T11	FB_A1_DQ<10>	
DQ11	T13	FB_A1_DQ<11>	
DQ12	N11	FB_A1_DQ<12>	
DQ13	N13	FB_A1_DQ<13>	
DQ14	M11	FB_A1_DQ<14>	
DQ15	M13	FB_A1_DQ<15>	
DQ16	A11	FB_A1_DQ<16>	
DQ17	A13	FB_A1_DQ<17>	
DQ18	B11	FB_A1_DQ<18>	
DQ19	B13	FB_A1_DQ<19>	
DQ20	E11	FB_A1_DQ<20>	
DQ21	E13	FB_A1_DQ<21>	
DQ22	F11	FB_A1_DQ<22>	
DQ23	F13	FB_A1_DQ<23>	
DQ24	A4	FB_A1_DQ<24>	
DQ25	A2	FB_A1_DQ<25>	
DQ26	B4	FB_A1_DQ<26>	
DQ27	B2	FB_A1_DQ<27>	
DQ28	E4	FB_A1_DQ<28>	
DQ29	E2	FB_A1_DQ<29>	
DQ30	F4	FB_A1_DQ<30>	
DQ31	F2	FB_A1_DQ<31>	
NC	A5	NC	
A12/RFU/NC	J5	FB_A1_A<8>	
NC	U5	NC	

OMIT_TABLE

R9254 1K 5% 1/20W MF 201 FBA
R9250 120 1% 1/20W MF 201 FBA
R9253 120 1% 1/20W MF 201 FBA

U9250
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)

=PP1V35_GPU_FBVDDQ	C5	VDD	
	L11		
	L14		
	P11		
	R5		
	R10		
	C10		
	D11		
	G1		
	G4		
	G11		
	G14		
	L1		
	L4		
	B1	VDDQ	
	E10		
	F1		
	F3		
	F12		
	F14		
	G2		
	G13		
	H3		
	H12		
	K3		
	B3		
	K12		
	L2		
	L13		
	M1		
	M3		
	M12		
	M14		
	N5		
	N10		
	P1		
	B12		
	P3		
	P12		
	P14		
	T1		
	T3		
	T12		
	T14		
	B14		
	D1		
	D3		
	D12		
	D14		
	E5		
FB_A1_VREFC	J14	VREFC	
FB_A1_VREFD	A10	VREFD	
	U10		

	B5	
	L5	
	L10	
	P10	
	T5	
	T10	
VSS	B10	
	D10	
	G5	
	G10	
	H1	
	H14	
	K1	
	K14	
	A1	
	C14	
	E1	
	E3	
	E12	
	E14	
	F5	
	F10	
VSSQ	H2	
	H13	
	K2	
	A3	
	K13	
	M5	
	M10	
	N1	
	N3	
	N12	
	N14	
	R1	
	R3	
	R4	
	A12	
	R11	
	R12	
	R14	
	U1	
	U3	
	U12	
	U14	
	A14	
	C1	
	C3	
	C4	
	C11	
	C12	

OMIT_TABLE

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 mm

FB_A1_VREFC
R9280 549 1% 1/20W MF 201 FBA
C9281 820PF 10% 50V CERM 0402 FBA
R9281 1.33K 1% 1/20W MF 201 FBA
R9284 931 1% 1/20W MF 201 FBA
FB_SW_LEG

PLACE CLOSE TO U9250

FB_A1_VREFD
R9282 549 1% 1/20W MF 201 FBA
C9282 820PF 10% 25V X7R-CERM 0201 FBA
C9283 820PF 10% 25V X7R-CERM 0201 FBA
R9283 1.33K 1% 1/20W MF 201 FBA
R9285 931 1% 1/20W MF 201 FBA
FB_SW_LEG

C9200 4.7UF 20% 6.3V X5R-CERM1 402 FBA
C9201 4.7UF 20% 6.3V X5R-CERM1 402 FBA
C9202 4.7UF 20% 6.3V X5R-CERM1 402 FBA
C9203 4.7UF 20% 6.3V X5R-CERM1 402 FBA
C9204 4.7UF 20% 6.3V X5R-CERM1 402 FBA
C9205 4.7UF 20% 6.3V X5R-CERM1 402 FBA
C9206 1.0UF 20% 6.3V X5R 0201-1 FBA
C9207 1.0UF 20% 6.3V X5R 0201-1 FBA
C9208 1.0UF 20% 6.3V X5R 0201-1 FBA
C9209 1.0UF 20% 6.3V X5R 0201-1 FBA
C9210 1.0UF 20% 6.3V X5R 0201-1 FBA
C9211 1.0UF 20% 6.3V X5R 0201-1 FBA
C9212 1.0UF 20% 6.3V X5R 0201-1 FBA
C9213 1.0UF 20% 6.3V X5R 0201-1 FBA
C9214 1.0UF 20% 6.3V X5R 0201-1 FBA
C9215 1.0UF 20% 6.3V X5R 0201-1 FBA
C9216 0.1UF 10% 6.3V CERM-X5R 0201 FBA
C9217 0.1UF 10% 6.3V CERM-X5R 0201 FBA
C9218 0.1UF 10% 6.3V CERM-X5R 0201 FBA
C9219 0.1UF 10% 6.3V CERM-X5R 0201 FBA
C9220 0.1UF 10% 6.3V CERM-X5R 0201 FBA
C9221 0.1UF 10% 6.3V CERM-X5R 0201 FBA
C9222 0.1UF 10% 6.3V CERM-X5R 0201 FBA
C9223 0.1UF 10% 6.3V CERM-X5R 0201 FBA
C9224 0.1UF 10% 6.3V CERM-X5R 0201 FBA
C9225 0.1UF 10% 6.3V CERM-X5R 0201 FBA

C9250 4.7UF 20% 6.3V X5R-CERM1 402 FBA
C9251 4.7UF 20% 6.3V X5R-CERM1 402 FBA
C9252 4.7UF 20% 6.3V X5R-CERM1 402 FBA
C9253 4.7UF 20% 6.3V X5R-CERM1 402 FBA
C9254 4.7UF 20% 6.3V X5R-CERM1 402 FBA
C9255 4.7UF 20% 6.3V X5R-CERM1 402 FBA
C9256 1.0UF 20% 6.3V X5R 0201-1 FBA
C9257 1.0UF 20% 6.3V X5R 0201-1 FBA
C9258 1.0UF 20% 6.3V X5R 0201-1 FBA
C9259 1.0UF 20% 6.3V X5R 0201-1 FBA
C9260 1.0UF 20% 6.3V X5R 0201-1 FBA
C9261 1.0UF 20% 6.3V X5R 0201-1 FBA
C9262 1.0UF 20% 6.3V X5R 0201-1 FBA
C9263 1.0UF 20% 6.3V X5R 0201-1 FBA
C9264 1.0UF 20% 6.3V X5R 0201-1 FBA
C9265 1.0UF 20% 6.3V X5R 0201-1 FBA
C9266 0.1UF 10% 6.3V CERM-X5R 0201 FBA
C9267 0.1UF 10% 6.3V CERM-X5R 0201 FBA
C9268 0.1UF 10% 6.3V CERM-X5R 0201 FBA
C9269 0.1UF 10% 6.3V CERM-X5R 0201 FBA
C9270 0.1UF 10% 6.3V CERM-X5R 0201 FBA
C9271 0.1UF 10% 6.3V CERM-X5R 0201 FBA
C9272 0.1UF 10% 6.3V CERM-X5R 0201 FBA
C9273 0.1UF 10% 6.3V CERM-X5R 0201 FBA
C9274 0.1UF 10% 6.3V CERM-X5R 0201 FBA
C9275 0.1UF 10% 6.3V CERM-X5R 0201 FBA

SYNC_MASTER=J16_DG SYNC_DATE=04/21/2013

PAGE TITLE
GDDR5 Frame Buffer A

Apple Inc.

DRAWING NUMBER	051-9889
SIZE	D
REVISION	13.0.0
BRANCH	
PAGE	92 OF 123
SHEET	75 OF 97

Page Notes

Power aliases required by this page:

- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

This memory device is in Mirrored Mode.

CK TERMINATION - B0
NO_XNET_CONNECTION=TRUE
NO_XNET_CONNECTION=TRUE
FB_B0_CLK_P
FB_B0_CLK_N
FB0_CK_MID
R9301 40.2 1% 1/20W MF 201
R9302 40.2 1% 1/20W MF 201
C9390 0.01UF 10% 10V X5R-CERM 0201
PLACE_NEAR=U9300.J11:8MM
PLACE_NEAR=U9300.J12:8MM

CK TERMINATION - B1
NO_XNET_CONNECTION=TRUE
NO_XNET_CONNECTION=TRUE
FB_B1_CLK_P
FB_B1_CLK_N
FBB1_CK_MID
R9351 40.2 1% 1/20W MF 201
R9352 40.2 1% 1/20W MF 201
C9391 0.01UF 10% 10V X5R-CERM 0201
PLACE_NEAR=U9350.J11:8MM
PLACE_NEAR=U9350.J12:8MM

U9300
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)
OMIT_TABLE

U9300
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(2 OF 2)
OMIT_TABLE

U9350
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(1 OF 2)
OMIT_TABLE

U9350
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)
OMIT_TABLE

PLACE CLOSE TO U9300

PLACE CLOSE TO U9350

SYNC_MASTER=J16_DG	SYNC_DATE=04/21/2013
PAGE TITLE	GDDR5 Frame Buffer B
Apple Inc.	DRAWING NUMBER 051-9889 SIZE D
	REVISION 13.0.0
	BRANCH
	PAGE 93 OF 123
	SHEET 76 OF 97

PD FOR AUX CHANNELS (FOR NVIDIA)

DP_INT_EG_AUX_P
DP_INT_EG_AUX_N
DP_TBTSNK0_EG_AUXCH_P
DP_TBTSNK0_EG_AUXCH_N
DP_TBTSNK1_EG_AUXCH_P
DP_TBTSNK1_EG_AUXCH_N

R9614 100K 1% 1/20W MF 201
R9613 100K 1% 1/20W MF 201
R9615 100K 1% 1/20W MF 201
R9616 100K 1% 1/20W MF 201
R9617 100K 1% 1/20W MF 201
R9618 100K 1% 1/20W MF 201

=PP3V3_GPU_VDD33

R9625 100K 1% 1/20W MF 201 NOSTUFF
R9626 100K 1% 1/20W MF 201 NOSTUFF
R9624 4.7K 1% 1/20W MF 201
R9623 4.7K 1% 1/20W MF 201
R9629 100K 5% 1/20W MF 201
R9630 100K 5% 1/20W MF 201

DP_TBTSNK0_DDC_CLK
DP_TBTSNK0_DDC_DATA
I2CA_SCL
I2CA_SDA

GPU_SSC_SMB_CLK
GPU_SSC_SMB_DAT
I2CC_SCL
I2CC_SDA

DDC MAPPING
I2CA -> IFPE DDC
I2CB -> IFPF DDC
I2CC -> Not used (was ext SSC cntl)

GPU_SMB_CLK
GPU_SMB_DAT
I2CS_SCL
I2CS_SDA

=PP3V3_GPU_VDD33

R9627 100K 5% 1/20W MF 201 NOSTUFF
R9628 100K 5% 1/20W MF 201 NOSTUFF

DP_TBTSNK1_DDC_CLK
DP_TBTSNK1_DDC_DATA
I2CB_SCL
I2CB_SDA

R9631 100K 1% 1/20W MF 201
R9632 100K 1% 1/20W MF 201

CRITICAL
L9604 330-OHM-1.2A 0603
=PP3V3_GPU_IFPX_PLLVDD
PP3V3_GPU_IFPX_PLLVDD
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

IFPX PLLVDD
C9619 4.7UF 20% 6.3V X5R-CERM 603
C9615 1UF 10% 6.3V X7R 0402
C9617 0.1UF 10% 16V X7R-CERM 0402
C9618 0.1UF 10% 16V X7R-CERM 0402
C9612 0.1UF 10% 16V X7R-CERM 0402

L9605 FERR-220-OHM-2A 0603
=PP1V05_GPU_IFPCD_IOVDD
PP1V05_GPU_IFPD_IOVDD
MIN_LINE_WIDTH=0.508MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V
CRITICAL
ESR = 0.050OHM

IFP CD IOVDD
C9625 4.7UF 20% 6.3V X5R-CERM1 402
C9656 1.0UF 20% 6.3V X5R 0201-1
C9657 0.1UF 10% 16V X7R-CERM 0402
C9658 0.1UF 10% 16V X7R-CERM 0402

L9606 FERR-220-OHM-2A 0603
=PP1V05_GPU_IFPEF_IOVDD
PP1V05_GPU_IFPEF_IOVDD
MIN_LINE_WIDTH=0.508MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V
CRITICAL
ESR = 0.050OHM

IFP EF IOVDD
C9633 4.7UF 20% 6.3V X5R-CERM1 402
C9634 4.7UF 20% 6.3V X5R-CERM1 402
C9635 1.0UF 20% 6.3V X5R 0201-1
C9636 1.0UF 20% 6.3V X5R 0201-1
C9637 0.1UF 10% 16V X7R-CERM 0402
C9638 0.1UF 10% 16V X7R-CERM 0402
C9631 0.1UF 10% 16V X7R-CERM 0402
C9632 0.1UF 10% 16V X7R-CERM 0402

DISABLE PHYs A, B & C FOR K70

OMIT_TABLE
CRITICAL
U8700
NV-GK107
BGA
(5 OF 10)

GPU_IFPA_IOVDD
GPU_IFPB_IOVDD
GPU_IFPC_IOVDD
PP1V05_GPU_IFPD_IOVDD
PP1V05_GPU_IFPEF_IOVDD
PP1V05_GPU_IFPEF_IOVDD

IFPA_IOVDD AG8
IFPB_IOVDD AG9
IFPC_IOVDD AF6
IFPD_IOVDD AG6
IFPE_IOVDD AC7
IFPF_IOVDD AC8

GPU_IFPAB_PLLVDD
IFPAB_PLLVDD AH8
IFPAB_RSET AJ8
NC

GPU_IFPX_PLLVDD
IFPC_PLLVDD AF7
IFPC_RSET AF8
NC

PP3V3_GPU_IFPX_PLLVDD
IFPD_RSET
PP3V3_GPU_IFPX_PLLVDD
IFPEF_RSET

IFPD_PLLVDD AG7
IFPD_RSET AN2
IFPEF_PLLVDD AH8
IFPEF_RSET AD6

IFPA_TXC AM6 NC
IFPA_TXC* AM6 NC
IFPA_TXD0 AP3 NC
IFPA_TXD0* AN3 NC
IFPA_TXD1 AN5 NC
IFPA_TXD1* AM5 NC
IFPA_TXD2 AL6 NC
IFPA_TXD2* AK6 NC
IFPA_TXD3 AJ6 NC
IFPA_TXD3* AH6 NC
IFPB_TXC AJ9 NC
IFPB_TXC* AH9 NC
IFPB_TXD4 AF6 NC
IFPB_TXD4* AF5 NC
IFPB_TXD5 AM7 NC
IFPB_TXD5* AL7 NC
IFPB_TXD6 AN8 NC
IFPB_TXD6* AM8 NC
IFPB_TXD7 AK8 NC
IFPB_TXD7* AL8 NC
IFPC_AUX_I2CW_SCL AG3 NC
IFPC_AUX_I2CW_SDA* AG2 NC
IFPC_L0 AK1 NC
IFPC_L0* AJ1 NC
IFPC_L1 AJ3 NC
IFPC_L1* AJ2 NC
IFPC_L2 AH3 NC
IFPC_L2* AH4 NC
IFPC_L3 AG5 NC
IFPC_L3* AG4 NC

IFPD_AUX_I2CX_SCL AK3 DP_INT_EG_AUX_P BI 41 77 95
IFPD_AUX_I2CX_SDA* AK2 DP_INT_EG_AUX_N BI 41 77 95
IFPD_L0 AM1 DP_INT_EG_ML_P<0> OUPD 41 95
IFPD_L0* AM2 DP_INT_EG_ML_N<0> OUPD 41 95
IFPD_L1 AM3 DP_INT_EG_ML_P<1> OUPD 41 95
IFPD_L1* AM4 DP_INT_EG_ML_N<1> OUPD 41 95
IFPD_L2 AL3 DP_INT_EG_ML_P<2> OUPD 41
IFPD_L2* AL4 DP_INT_EG_ML_N<2> OUPD 41
IFPD_L3 AK4 DP_INT_EG_ML_P<3> OUPD 41
IFPD_L3* AK5 DP_INT_EG_ML_N<3> OUPD 41

IFPE_AUX_I2CY_SCL AB3 DP_TBTSNK0_EG_AUXCH_P BI 77
IFPE_AUX_I2CY_SDA* AB4 DP_TBTSNK0_EG_AUXCH_N BI 77
IFPE_L0 AD2 DP_TBTSNK0_ML_C_P<0> OUPD 26 95
IFPE_L0* AD3 DP_TBTSNK0_ML_C_N<0> OUPD 26 95
IFPE_L1 AD1 DP_TBTSNK0_ML_C_P<1> OUPD 26 95
IFPE_L1* AC1 DP_TBTSNK0_ML_C_N<1> OUPD 26 95
IFPE_L2 AC2 DP_TBTSNK0_ML_C_P<2> OUPD 26 95
IFPE_L2* AC3 DP_TBTSNK0_ML_C_N<2> OUPD 26 95
IFPE_L3 AC4 DP_TBTSNK0_ML_C_P<3> OUPD 26 95
IFPE_L3* AC5 DP_TBTSNK0_ML_C_N<3> OUPD 26 95

IFPF_AUX_I2CZ_SCL AF3 DP_TBTSNK1_EG_AUXCH_P BI 77
IFPF_AUX_I2CZ_SDA* AF2 DP_TBTSNK1_EG_AUXCH_N BI 77
IFPF_L0 AE3 DP_TBTSNK1_ML_C_P<0> OUPD 26 95
IFPF_L0* AE4 DP_TBTSNK1_ML_C_N<0> OUPD 26 95
IFPF_L1 AF4 DP_TBTSNK1_ML_C_P<1> OUPD 26 95
IFPF_L1* AF5 DP_TBTSNK1_ML_C_N<1> OUPD 26 95
IFPF_L2 AD4 DP_TBTSNK1_ML_C_P<2> OUPD 26 95
IFPF_L2* AD5 DP_TBTSNK1_ML_C_N<2> OUPD 26 95
IFPF_L3 AG1 DP_TBTSNK1_ML_C_P<3> OUPD 26 95
IFPF_L3* AF1 DP_TBTSNK1_ML_C_N<3> OUPD 26 95

DAC_AVDD
DACA_VDD AG10
DACA_RED AK9 NC
DACA_GREEN AL10 NC
DACA_BLUE AL9 NC
DACA_VREF AP9 NC
DACA_RSET AP8 NC
DACA_HSYNC AM9 NC
DACA_VSYNC AN9 NC

R9600 10K 1% 1/20W MF 201

CEC L3 NC

GPU_IFPA_IOVDD
R9601 10K 1% 1/20W MF 201
GPU_IFPB_IOVDD
R9602 10K 1% 1/20W MF 201
GPU_IFPC_IOVDD
R9603 10K 1% 1/20W MF 201
GPU_TESTMODE
R9608 10K 1% 1/20W MF 201

GPU_IFPAB_PLLVDD
R9604 10K 1% 1/20W MF 201
GPU_IFPX_PLLVDD
R9619 10K 1% 1/20W MF 201

PD FOR RSET
PP3V3_GPU_VDD33
R9606 1K 1% 1/20W MF 201
PP3V3_GPU_VDD33
R9607 1K 1% 1/20W MF 201

Page Notes

Power aliases required by this page:
- +PP3V3_GPU_IFPA_IOVDD
- +PP1V05_GPU_IFPCD_IOVDD
- +PP1V8_GPU_IFPA_IOVDD
- +PP1V05_GPU_IFPEF_IOVDD
- +PP1V8_GPU_SMPLL
- +PP3V3_GPU_VDD33
- +PP1V05_GPU_SMPLL
- +PP3V3_GPU_IFPA_PLLVDD

Signal aliases required by this page:
(NONE)

ROM options provided by this page:
- J31:VBB
- J5:VBB

PP1V05_GPU_SP_PLLVDD
PP1V05_GPU_VID_PLLVDD
MAKE_BASE=TRUE
DP_TBTSNK0_EG_AUXCH_P
DP_TBTSNK0_AUXCH_C_P
DP_TBTSNK0_EG_AUXCH_N
DP_TBTSNK0_AUXCH_C_N
DP_TBTSNK1_EG_AUXCH_P
DP_TBTSNK1_AUXCH_C_P
DP_TBTSNK1_EG_AUXCH_N
DP_TBTSNK1_AUXCH_C_N

OMIT_TABLE
U8700
NV-GK107
BGA
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=PP3V3_GPU_MISC
=PP3V3_GPU_VDD33
VDD33 J8 K8 L8 M8

ROM_CS* H6 NC
ROM_SCLK H4 GPU_ROM_SCLK OUT
ROM_SI H5 GPU_ROM_SI IN
ROM_SO H7 GPU_ROM_SO OUT

R9609 40.2K 0.1% 1/20W MF 0201
MULTI_STRAP_REF J1 MULTI_STRAP_REF0_GND

GPU_TESTMODE
TESTMODE AK11
SP_PLLVDD AE8 PP1V05_GPU_SP_PLLVDD
PLLVDD AD8 PP1V05_GPU_PLLVDD
VID_PLLVDD AD7 PP1V05_GPU_VID_PLLVDD

GPU_OSC_27M_XTALIN
XTAL_IN H3
GPU_OSC_27M_XTALOUT
XTAL_OUT H2

GPU_XTAL_OUTBUFF
XTAL_OUTBUFF J4
GPU_XTAL_SSIN
XTAL_SSIN H1

R9620 10K 5% 1/20W MF 201
R9622 10K 5% 1/20W MF 201

GPU_MLS_STRAP0
STRAP0 J2
GPU_MLS_STRAP1
STRAP1 J7
GPU_MLS_STRAP2
STRAP2 J6
GPU_MLS_STRAP3
STRAP3 J5
GPU_MLS_STRAP4
STRAP4 J3

GPIO0 P6 GPU_GPIO_0 BI
GPIO1 M3 GPU_GPIO_1 BI
GPIO2 L6 GPU_GPIO_2 BI
GPIO3 P5 GPU_GPIO_3 BI
GPIO4 P7 GPU_GPIO_4 BI
GPIO5 L7 GPU_GPIO_5 BI
GPIO6 M7 GPU_GPIO_6 BI
GPIO7 N8 GPU_GPIO_7 BI
GPIO8 M1 GPU_GPIO_8 BI
GPIO9 M2 GPU_GPIO_9 BI
GPIO10 L1 GPU_GPIO_10 BI
GPIO11 M5 GPU_GPIO_11 BI
GPIO12 N3 GPU_GPIO_12 BI
GPIO13 M4 GPU_GPIO_13 BI
GPIO14 N4 GPU_GPIO_14 BI
GPIO15 P2 GPU_GPIO_15 BI
GPIO16 R8 GPU_GPIO_16 BI
GPIO17 M6 GPU_GPIO_17 BI
GPIO18 R1 GPU_GPIO_18 BI
GPIO19 P3 GPU_GPIO_19 BI
GPIO20 P4 GPU_GPIO_20 BI
GPIO21 P1 GPU_GPIO_21 BI

JTAG_TCK AM10 GPU_JTAG_TCK IN
JTAG_TDI AM11 GPU_JTAG_TDI IN
JTAG_TDO AP12 GPU_JTAG_TDO OUPD
JTAG_TMS AP11 GPU_JTAG_TMS IN
JTAG_TRST* AN11 GPU_JTAG_TRST_L IN

THERMDP K3 GPU_TDIODE_P IN
THERMDN K4 GPU_TDIODE_N OUPD

GPU PLL VDD
L9607 FERR-220-OHM-2A 0603
=PP1V05_GPU_PEX_PLLVDD
PP1V05_GPU_PLLVDD
MIN_LINE_WIDTH=0.41MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V
CRITICAL
ESR = 0.050OHM
C9651 20UF 20% 4V X5R-CERM 0402
C9654 0.1UF 10% 16V X7R-CERM 0402

GPU 3V3 VDD
=PP3V3_GPU_VDD33
C9642 1UF 10% 6.3V X7R 0402
C9643 0.1UF 10% 16V X7R-CERM 0402
C9644 0.1UF 10% 16V X7R-CERM 0402
=PP3V3_GPU_MISC
C9646 4.7UF 20% 6.3V X5R-CERM1 402
C9649 0.1UF 10% 16V X7R-CERM 0402
C9650 0.1UF 10% 16V X7R-CERM 0402

SYNC_MASTER=J16_DG
SYNC_DATE=04/21/2013
PAGE TITLE
KEPLER EDP/DP/GPIO
Apple Inc.
DRAWING NUMBER 051-9889
SIZE D
REVISION 13.0.0
BRANCH
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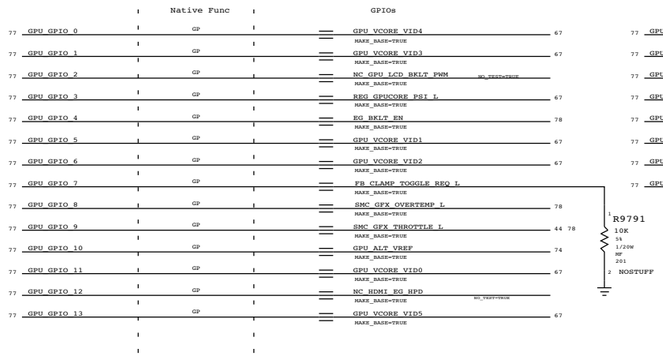
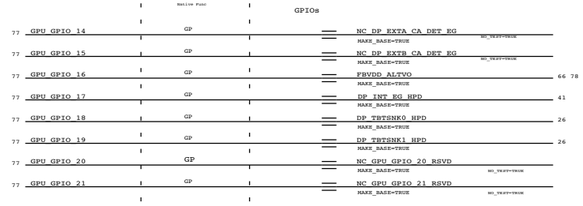
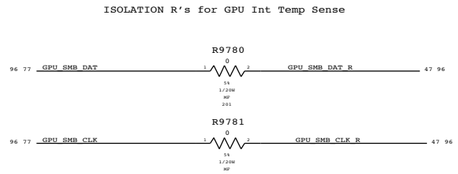
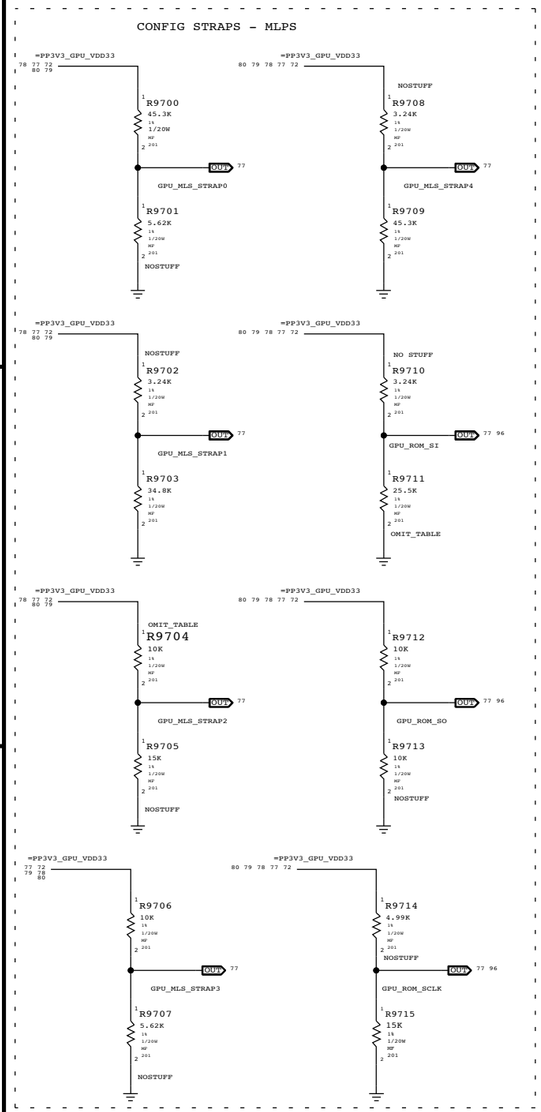
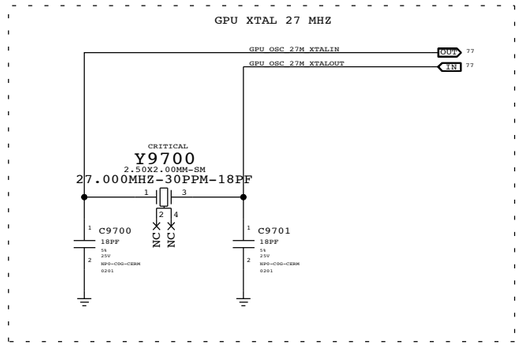
SHEET 77 OF 97

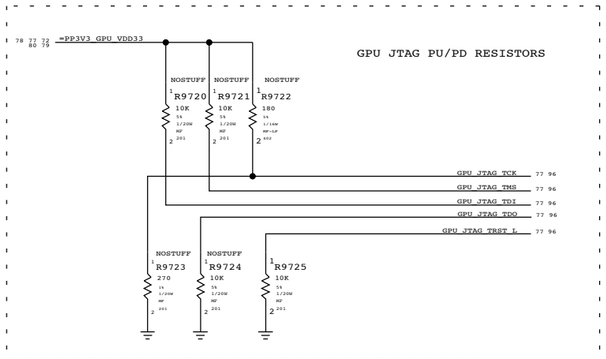


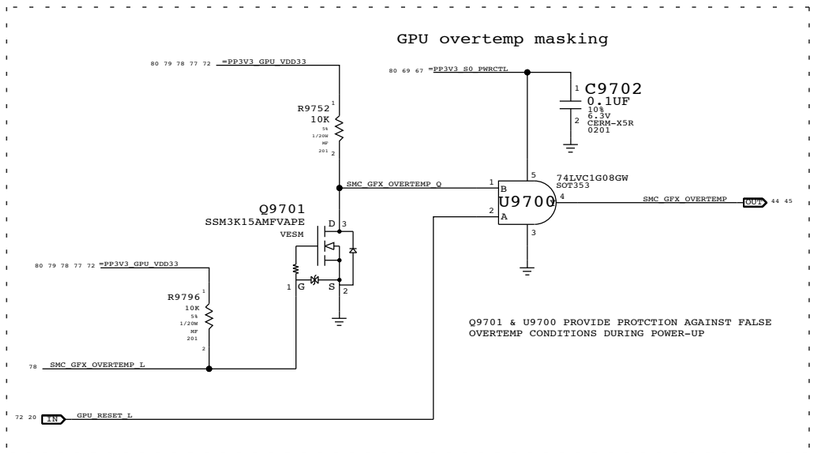


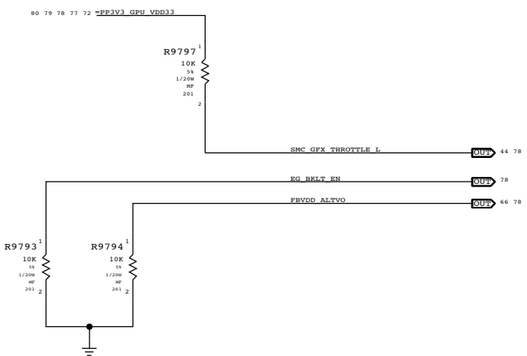












PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0409	1	RES,MF,4.99k ,1,1/20W,0201	R9704		GPU:107GSXA
118S0409	1	RES,MF,4.99k ,1,1/20W,0201	R9704		GPU:107GSXB
118S0013	1	RES,MF,10.0K ,1,1/20W,0201	R9704		GPU:107GX
118S0230	1	RES,MF,24.9k ,1,1/20W,0201	R9711		FB:CH1_HYNIX
118S0230	1	RES,MF,24.9k ,1,1/20W,0201	R9711		FB:CH2_HYNIX
118S0230	1	RES,MF,24.9K ,1,1/20W,0201	R9711		FB:BOTH_HYNIX
118S0280	1	RES,MF,30.1k ,1,1/20W,0201	R9711		FB:CH1_ELPIDA
118S0280	1	RES,MF,30.1k ,1,1/20W,0201	R9711		FB:CH2_ELPIDA
118S0280	1	RES,MF,30.1k ,1,1/20W,0201	R9711		FB:BOTH_ELPIDA

SYNC_MASTER=J16_DG SYNC_DATE=04/21/2013

PAGE TITLE
KEPLER GPIOS,CLK & STRAPS

Apple Inc.

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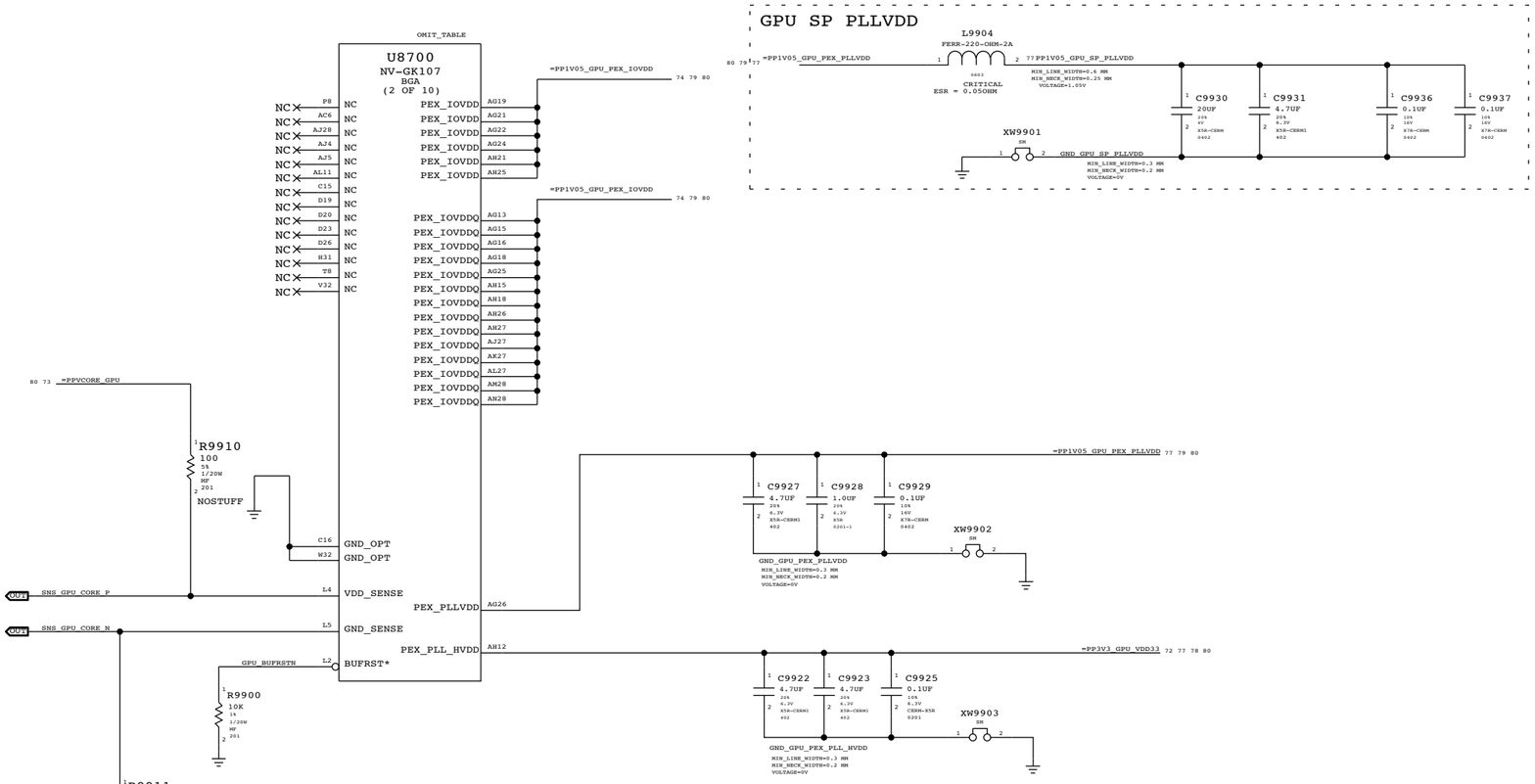

SYNC MASTER=J16 DG SYNC DATE=04/21/2013

PAGE TITLE: KEPLER PEX PWR/GNDS

Apple Inc.

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G3 Rails

Always on: Keeps the PCH RTC alive

94 PP3V3_G3 (MAKE_BASE=TRUE)
- PP3V3_G3_RTC — 19
- =PP3V3_G3_PCH_RTC — 15
- =PP3V3_G3_PCH — 11 12

G3H Rails

94 PP12V_ACDC (MAKE_BASE=TRUE)
- PP12V_G3H_ACDC — 60
- =PP12V_G3H_SNS_R — 48

94 PP12V_G3H (MAKE_BASE=TRUE)
- PP12V_G3H_SNS — 48
- =PP12V_G3H_REG_3V42_G3H — 60
- =PP12V_G3H_FET_P12V_S5 — 60
- =PP12V_G3H_FET_P12V_S0 — 69

94 PP3V42_G3H (MAKE_BASE=TRUE)
- PP3V42_G3H_REG — 60
- =PP3V3_G3H_BT — 32
- =PP3V3_G3H_SMC — 44 45 51
- =PP3V3_G3H_RTC_D — 19
- =PPVIN_G3H_SMCVREF — 45
- =PP3V3_G3H_SMC_USBMUX — 42
- =PP3V3_G3H_LPCPLUS — 46

Ground/Common

GND (MAKE_BASE=TRUE)

S5 Rails

Enabled when system has AC and is in S5

94 PP12V_S5 (MAKE_BASE=TRUE)
- PP12V_S5_FET — 60
- =PP12V_S5_REG_P3V3P5V_S5 — 65
- =PP12V_S5_REG_VDDQ_S3 — 63
- =PP12V_S5_PWRCTL — 69 70
- =PPHV_SW_TBTAPWRSW — 29
- =PPHV_SW_TBTBPWRSW — 30
- =PP12V_S5_SNS — 48

94 PP5V_S5 (MAKE_BASE=TRUE)
- PP5V_S5_LDO — 65
- =PP5V_S5_PWRCTL — 65 69

94 PP3V3_S5 (MAKE_BASE=TRUE)
- PP3V3_S5_REG — 65
- =PP3V3_S5_FET_P3V3_S4 — 69
- =PP3V3_S5_FET_P3V3_S0 — 69
- =PP3V3_S5_PWRCTL — 69 70 71
- =PP3V3_S5_VRD — 65
- =PP3V3_S5_LED — 3
- =PP3V3_S5_PCH_VCCSUS_GPIO — 11 12 13 14 15 17
- =PP3V3_S5_PCH_VCCDSW — 15 17
- =PP3V3_S5_PCH_VCC_SPI — 15 17
- =PP3V3_S5_PCH_VCCSUS_HDA — 15 17
- =PP3V3_S5_PCH_VCCSUS_USB — 15 17
- =PP3V3_S5_PCH_VCCSUS_RTC — 15 17
- =PP3V3_S5_PCH_VCCSUS_USB3 — 15
- =PP3V3_S5_PCH — 19 20
- =PP3V3_S5_ROM — 46
- =PP3V3_S5_SENSE — 48
- =PP3V3_S5_SMC — 45
- =PP3V3_S5_XDP — 18
- =PP3V3_S4_TBTAPWRSW — 29
- =PP3V3_S4_TBTBPWRSW — 30
- =PP3V3_S5_SNS — 49

S4 Rails

Enabled when system has AC and is in run or sleep

94 PP5V_S4 (MAKE_BASE=TRUE)
- PP5V_S4_REG — 65
- =PP5V_S4_REG_VDDQ_S3 — 63
- =PP5V_S4_FET_P5V_S0 — 69
- =PP5V_S4_MEMRESET — 21
- =PP5V_S4_PWRCTL — 69
- =PP5V_S4_USB — 42 43
- =PP5V_S4_CAMERA — 38

94 PP3V3_S4 (MAKE_BASE=TRUE)
- PP3V3_S4_FET — 69
- =PP3V3_S4_FET_ENET — 36
- =PP3V3_S4_PWRCTL — 63 69
- =PP3V3_S4_ALS — 38
- =PP3V3_S4_LED — 3
- =PP3V3_S4_MEMRESET — 21
- =PP3V3_S4_PCH — 13
- =PP3V3_S4_PM — 21
- =PP3V3_S4_SDCARD — 37
- =PP3V3_S4_SMC — 45
- =PP3V3_S4_SMBUS_SMC_2 — 47
- =PP3V3_S4_TBT — 26 27 28 29 30 70
- =PP3V3_S4_CAMERA — 38 39
- =PP3V3_S4_AUDIO_DIG — 56
- =PP3V3_S4_AP — 32 45
- =PP3V3_S3_VREFMRGN — 22

S3 Rails

Enabled when system is in run or sleep

94 PP3V3_ENET (MAKE_BASE=TRUE)
- PP3V3_ENET_FET — 36
- =PP3V3_ENET_PHY — 35 36
- =PP3V3_ENET_SYSCLK — 19
- =PPVDDIO_ENET_CLK — 19

92 PPVDDQ_S3 (MAKE_BASE=TRUE)
- PPVDDQ_S3_REG — 63
- =PPVDDQ_S3_FET_VDDQ_S0 — 69
- =PPVDDQ_S3_SNS_DDR_R — 49

92 PPVDDQ_S3_DDR (MAKE_BASE=TRUE)
- PPVDDQ_S3_SNS_DDR — 49
- =PPVDDQ_S3_LDO_DDRVTT — 63
- =PPDDR_S3_MEMVREF — 22
- =PPVDDQ_S3_MEM_A — 23
- =PPVDDQ_S3_MEM_B — 24
- =PPVDDQ_S3_MEMRESET — 21

S0 Rails

Enabled when system is in run

94 PP12V_S0 (MAKE_BASE=TRUE)
- PP12V_S0_FET — 69
- =PP12V_S0_REG_CPUVCC_S0 — 62
- =PP12V_S0_REG_P1V05_S0 — 64
- =PP12V_S0_SNS_GPUCORE_R — 48
- =PP12V_S0_SNS_FBVDDQ_R — 48
- =PP12V_S0_AUDIO_SPKRAMP — 54 55
- =PP12V_S0_BKLT — 68
- =PP12V_S0_FAN — 51
- =PP12V_S0_LCD — 40

94 PP12V_S0_GPUCORE (MAKE_BASE=TRUE)
- PP12V_S0_SNS_GPUCORE — 48
- =PPVIN_S0_GFXIMVP — 67

94 PP12V_S0_FBVDDQ (MAKE_BASE=TRUE)
- PP12V_S0_SNS_FBVDDQ — 48
- =PP12V_S0_REG_GPU_VDDQ_S0 — 66

94 PP5V_S0_HDD (MAKE_BASE=TRUE)
- PPHDD_S0_SNS — 48
- =PP5V_S0_SATA — 34

94 PPHDD_S0 (MAKE_BASE=TRUE)
- PP5V_S0_HDD_FET — 69
- =PPHDD_S0_SNS_R — 48

94 PP5V_S0 (MAKE_BASE=TRUE)
- PP5V_S0_FET — 69
- =PP5V_S0_REG_CPUVCC_S0 — 61 62
- =PP5V_S0_REG_P1V05_S0 — 64
- =PP5V_S0_REG_GPU_VDDQ_S0 — 66
- =PP5V_S0_AUDIO — 52 59
- =PP5V_S0_ISENSE — 48
- =PP5V_S0_LPCPLUS — 46
- =PP5V_S0_BKLT — 68
- =PP5V_S0_GFXIMVP — 67
- =PP5V_S0_FET_P5V_HDD — 69

94 PP3V3_S0 (MAKE_BASE=TRUE)
- PP3V3_S0_FET — 69
- =PP3V3_S0_P3V3TBTFET — 28
- =PP3V3_S0_PWRCTL — 67 69 78 80
- =PP3V3_S0_VRD — 60 61 64 66
- =PP3V3_S0_AUDIO — 38 52 54 55 58
- =PP3V3_S0_AUDIO_DIG — 56
- =PP3V3_S0_DP — 31 40 47
- =PP3V3_S0_FAN — 51
- =PP3V3_S0_INTDPMUX — 41
- =PP3V3_S0_LED — 3
- =PP3V3_S0_LED_SATA — 33
- =PP3V3_S0_PCH — 19
- =PP3V3_S0_ENET — 35
- =PP3V3_S0_PCH_VCC3_3_GPIO — 11 12 13 14 15 17
- =PP3V3_S0_PCH_VCC3_3_THRM — 15 17
- =PP3V3_S0_PCH_VCCCLK3_3 — 15 17
- =PP3V3_S0_PCH_VCC3_3_HVCMOS — 15 17
- =PP3V3_S0_PCH_VCC_FUSE — 15 17
- =PP3V3_S0_PCH_VCC3_3_USB — 15 17
- =PP3V3_S0_RSTBUF — 20
- =PP3V3_S0_SDCARD — 37
- =PP3V3_S0_SENSE — 34 48 49 50
- =PP3V3_S0_SMBUS — 47
- =PP3V3_S0_SMBUS_SMC_0 — 47
- =PP3V3_S0_SMBUS_SMC_1 — 47
- =PP3V3_S0_SMBUS_SMC_3 — 47
- =PP3V3_S0_SMC — 45
- =PP3V3_S0_TBTPWRCTL — 28
- =PP3V3_S0_BKLT_VDDIO — 68
- =PP3V3_S0_GPU_IFPX_PLLVDD — 77
- =PP3V3_S0_GPU_MISC — 77
- =PP3V3_S0_GPU_VDD33 — 72 77 78 79
- =PPSPD_S0_MEM_A — 23
- =PPSPD_S0_MEM_B — 24
- =PP3V3_S0_GFX3V3BIAS — 67
- =PP3V3_S0_PWRCTL — 67 69 78 80
- =PP3V3_S0_PCH_GPIO — 14 28

94 PP3V3_S0_SSD (MAKE_BASE=TRUE)
- PP3V3_S0_SSD_FET — 69
- =PPSSD_S0_SNS_R — 49

94 PPSSD_S0 (MAKE_BASE=TRUE)
- PPSSD_S0_SNS — 49
- =PP3V3_S0_SSD — 33

92 PP1V5_S0 (MAKE_BASE=TRUE)
- PP1V5_S0_FET — 69
- =PP1V5_S0_SNS_R — 49

92 PP1V5_S0_PCH (MAKE_BASE=TRUE)
- PP1V5_S0_SNS — 49
- =PP1V5_S0_CPU_MEM — 6 8 10
- =PP1V5_S0_AUD_DIG — 52
- =PP1V5_S0_SENSE — 34
- =PP1V5_S0_PCH_VCCVRM — 17
- =PP1V5_S0_PCH_RCOMP — 12 13
- =PP1V5_S0_PCH_SATA — 11
- =PP1V5_S0_PCH_CLK — 11 19

92 PPDDRVTT_S0 (MAKE_BASE=TRUE)
- PPDDRVTT_S0_LDO — 63
- =PPDDRVTT_S0_CLAMP — 21
- =PPDDRVTT_S0_MEM_A — 23
- =PPDDRVTT_S0_MEM_B — 24

92 PP1V05_S0 (MAKE_BASE=TRUE)
- PP1V05_S0_REG — 64
- =PP1V05_S0_P1V05TBTFET — 28
- =PP1V05_S0_PCH_VCC — 15 17
- =PP1V05_S0_PCH_VCCCLK_CLK100 — 15 17
- =PP1V05_S0_PCH_VCCASW — 15 17
- =PP1V05_S0_PCH_VCC_CLK — 17
- =PP1V05_S0_PCH_VCCIO_FDI — 15 17
- =PP1V05_S0_PCH_VCCCLK_SSC — 15 17
- =PP1V05_S0_PCH_VCCUSBPLL — 15 17
- =PP1V05_S0_PCH_VCCIO — 15 17
- =PP1V05_S0_PCH_VCCCLK_SSC100 — 15 17
- =PP1V05_S0_PCH_VCCCLK_CLK135 — 15 17
- =PP1V05_S0_PCH_VCCIO_USB2 — 15 17
- =PP1V05_S0_PCH_V_PROC_IO — 14 15 17
- =PP1V05_S0_SNS — 48
- =PP1V05_S0_SMC — 45
- =PP1V05_S0_XDP — 18
- =PP1V05_GPU_IFPCD_IOVDD — 77
- =PP1V05_GPU_IFPEF_IOVDD — 77
- =PP1V05_GPU_PEX_IOVDD — 74 79
- =PP1V05_GPU_PEX_PLLVDD — 77 79

93 PPCPUVCC_S0_CPU (MAKE_BASE=TRUE)
- PPCPUVCC_S0_REG — 62
- =PPCPUVCC_S0_CPU — 6 8 10 48 61

Thunderbolt Rails (S0)

Enabled when Thunderbolt cable is plugged in

94 PP3V3_TBTLC (MAKE_BASE=TRUE)
- =PP3V3_TBTLC_FET — 28
- =PP3V3_TBT_PCH_GPIO — 20
- =PP3V3_TBTLC_RTR — 26 27 28
- =PPVDDIO_TBT_CLK — 19

92 28 PP1V05_TBTLC (MAKE_BASE=TRUE)
- =PP1V05_TBTLC_FET — 28
- =PP1V05_TBTLC_RTR — 27

92 PP1V05_TBTCIO (MAKE_BASE=TRUE)
- =PP1V05_TBTCIO_FET — 28
- =PP1V05_TBTCIO_RTR — 27

GPU Rails (S0)

Enabled when system is in run

94 PPVCORE_S0_GPU (MAKE_BASE=TRUE)
- PPGPUCORE_S0_REG — 67
- =PPVCORE_GPU — 73 79
- =PPGPUCORE_S0_SNS — 48

94 PPVDDQ_S0_GPU (MAKE_BASE=TRUE)
- PP1V5R1V35_S0_GPU_REG — 66
- =PP1V35_GPU_FBVDDQ — 73 75 76
- =PP1V35_GPU_S0_FB — 74

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PEG aliases

86 72 PEG_D2R_N<0..15> ⟷ =PEG_D2R_N<15..0> 5
MAKE_BASE=TRUE

86 72 PEG_D2R_P<0..15> ⟷ =PEG_D2R_P<15..0> 5
MAKE_BASE=TRUE

86 72 PEG_R2D_C_N<0..15> ⟷ =PEG_R2D_C_N<15..0> 5
MAKE_BASE=TRUE

86 72 PEG_R2D_C_P<0..15> ⟷ =PEG_R2D_C_P<15..0> 5
MAKE_BASE=TRUE

61 REG_ISENVCC_4_NR ⟷ AGND_CPU 61 62 93
MAKE_BASE=TRUE

Memory PGOOD

21 =PM_PGOOD_MEM_S0 ⟷ PM_PGOOD_FET_REG_P1V5_S0 69 70
MAKE_BASE=TRUE

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Signal Aliases

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CPU Reserved

88 18 6	CPU_CFG<15..12>	TP_CPU_CFG<15..12>	MAKE_BASE=TRUE

CPU Memory

7	TP_MEM_A_DQS_N<8>	NC_MEM_A_DQSN<8>	MAKE_BASE=TRUE NO_TEST=TRUE
7	TP_MEM_A_DQS_P<8>	NC_MEM_A_DQSP<8>	MAKE_BASE=TRUE NO_TEST=TRUE
7	TP_MEM_B_DQS_N<8>	NC_MEM_B_DQSN<8>	MAKE_BASE=TRUE NO_TEST=TRUE
7	TP_MEM_B_DQS_P<8>	NC_MEM_B_DQSP<8>	MAKE_BASE=TRUE NO_TEST=TRUE
85 7	MEM_A_CLK_N<2..3>	NC_MEM_A_CLKN<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
85 7	MEM_A_CLK_P<2..3>	NC_MEM_A_CLKP<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
85 7	MEM_A_CS_L<2..3>	NC_MEM_A_CS_L<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
85 7	MEM_A_CKE<2..3>	NC_MEM_A_CKE<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
85 7	MEM_B_CLK_N<2..3>	NC_MEM_B_CLKN<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
85 7	MEM_B_CLK_P<2..3>	NC_MEM_B_CLKP<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
85 7	MEM_B_CS_L<2..3>	NC_MEM_B_CS_L<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
85 7	MEM_B_CKE<2..3>	NC_MEM_B_CKE<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
85 7	MEM_A_ODT<2..3>	NC_MEM_A_ODT<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
85 7	MEM_B_ODT<2..3>	NC_MEM_B_ODT<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Clocks

	TP_ITPXDP_CLK100MP	ITPXDP_CLK100M_P 11 88	MAKE_BASE=TRUE NO_TEST=TRUE
	TP_ITPXDP_CLK100MN	ITPXDP_CLK100M_N 11 88	MAKE_BASE=TRUE NO_TEST=TRUE
11	TP_PCIE_CLK100M_PE4N	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE NO_TEST=TRUE
11	TP_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE NO_TEST=TRUE
11	TP_PCIE_CLK100M_PE5N	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE NO_TEST=TRUE
11	TP_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE NO_TEST=TRUE
11	TP_PCIE_CLK100M_PE7N	NC_PCIE_CLK100M_PE7N	MAKE_BASE=TRUE NO_TEST=TRUE
11	TP_PCIE_CLK100M_PE7P	NC_PCIE_CLK100M_PE7P	MAKE_BASE=TRUE NO_TEST=TRUE

PCH GPIO

11	TP_PCH_GPIO64_CLKOUTFLEX0	NC_PCH_GPIO64_CLKOUTFLEX0	MAKE_BASE=TRUE NO_TEST=TRUE
11	TP_PCH_GPIO65_CLKOUTFLEX1	NC_PCH_GPIO65_CLKOUTFLEX1	MAKE_BASE=TRUE NO_TEST=TRUE
11	TP_PCH_GPIO66_CLKOUTFLEX2	NC_PCH_GPIO66_CLKOUTFLEX2	MAKE_BASE=TRUE NO_TEST=TRUE
11	TP_PCH_GPIO67_CLKOUTFLEX3	NC_PCH_GPIO67_CLKOUTFLEX3	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Unused Display

5	TP_DP_IG_B_MLN<3..0>	NC_DP_IG_B_MLN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
5	TP_DP_IG_B_MLP<3..0>	NC_DP_IG_B_MLP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
5	TP_DP_IG_C_MLN<3..0>	NC_DP_IG_C_MLN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
5	TP_DP_IG_C_MLP<3..0>	NC_DP_IG_C_MLP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
5	TP_DP_IG_D_MLN<3..0>	NC_DP_IG_D_MLN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
5	TP_DP_IG_D_MLP<3..0>	NC_DP_IG_D_MLP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE

PCH PCI

13	TP_LPC_DREQ0_L	NC_LPC_DREQ0_L	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Miscellaneous

11	TP_HDA_SDIN1	NC_HDA_SDIN1	MAKE_BASE=TRUE NO_TEST=TRUE
11	TP_HDA_SDIN2	NC_HDA_SDIN2	MAKE_BASE=TRUE NO_TEST=TRUE
11	TP_HDA_SDIN3	NC_HDA_SDIN3	MAKE_BASE=TRUE NO_TEST=TRUE
11	TP_PCI_CLK33M_OUT2	NC_PCI_CLK33M_OUT2	MAKE_BASE=TRUE NO_TEST=TRUE
11	TP_PCI_CLK33M_OUT3	NC_PCI_CLK33M_OUT3	MAKE_BASE=TRUE NO_TEST=TRUE

UNUSED GRAPHICS ALIASES

77	GPU_TDIODE_P	NC_GPU_TDIODE_P	MAKE_BASE=TRUE NO_TEST=TRUE
77	GPU_TDIODE_N	NC_GPU_TDIODE_N	MAKE_BASE=TRUE NO_TEST=TRUE

UNUSED THUNDERBOLT ALIASES

26	TP_TBT_PCIE_RESET0_L	NC_TBT_PCIE_RESET0_L	MAKE_BASE=TRUE NO_TEST=TRUE
26	TP_TBT_PCIE_RESET1_L	NC_TBT_PCIE_RESET1_L	MAKE_BASE=TRUE NO_TEST=TRUE
26	TP_TBT_PCIE_RESET2_L	NC_TBT_PCIE_RESET2_L	MAKE_BASE=TRUE NO_TEST=TRUE
26	TP_TBT_PCIE_RESET3_L	NC_TBT_PCIE_RESET3_L	MAKE_BASE=TRUE NO_TEST=TRUE
26	TP_TBT_THERM_DP	NC_TBT_THERM_DP	MAKE_BASE=TRUE NO_TEST=TRUE

UNUSED VREG ALIASES

61	REG_PWM_CPUVCC_4	NC_REG_PWM_CPUVCC_4	MAKE_BASE=TRUE NO_TEST=TRUE
61	REG_ISENVCC_4_P	NC_REG_ISENVCC_4P	MAKE_BASE=TRUE NO_TEST=TRUE

POWER SEQUENCING

70	PM_EN_FET_P1V35_S0	NC_PM_EN_FET_P1V35_S0	MAKE_BASE=TRUE NO_TEST=TRUE
70	PM_PGOOD_FET_P1V35_S0	NC_PM_PGOOD_FET_P1V35_S0	MAKE_BASE=TRUE NO_TEST=TRUE

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Unused Signal Aliases

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Functional / ICT Test

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J16 BOARD SPECIFIC PHYSICAL AND SPACING CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA	MM	16.2

General Physical Rule Definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.1 MM	=50_OHM_SE	12.7 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	*	Y	0.215 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	TOP,BOTTOM	Y	0.215 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	*	Y	0.170 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	*	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	0.138 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.138 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.110 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	Y	0.180 MM	0.085 MM	=STANDARD	0.140 MM	0.1 MM
68_OHM_DIFF	TOP,BOTTOM	Y	0.180 MM	0.085 MM	=STANDARD	0.140 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.135 MM	0.085 MM	=STANDARD	0.160 MM	0.1 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD	0.160 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.089 MM	0.085 MM	=STANDARD	0.220 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.085 MM	=STANDARD	0.220 MM	0.1 MM

General Spacing Definitions

Default

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

Fixed and Dielectric

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1X_DIELECTRIC	*	0.076 MM	?
1X_DIELECTRIC	TOP,BOTTOM	0.071 MM	?

BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=STANDARD	?

Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND_P2MM	*	=2:1_SPACING	1000
PWR_P2MM	*	=2:1_SPACING	1100

BGA Area Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM

Board Stack-up

Finished board thickness: 1.58 mm

Top	Signal	0.5 oz (Cu plated)	
	Prepreg	0.071 mm	
2	Plane	1 oz	
	Prepreg	0.076 mm	
3	Signal	0.5 oz	
	Prepreg	0.435 mm	
4	Plane	1 oz	
	Core	0.127 mm	
5	Plane	1 oz	
	Prepreg	0.435 mm	
6	Signal	0.5 oz	
	Prepreg	0.076 mm	
2	Plane	1 oz	
	Prepreg	0.071 mm	
Btm	Signal	0.5 oz (Cu plated)	

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J16 RULE DEFINITIONS

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DDR3

DDR3-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_34S	*	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=STANDARD	=STANDARD
DDR_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
DDR_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
DDR_42S_D	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	0.1016 MM	0.1016 MM
DDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
DDR_68D	*	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF
DDR_COMP	*	Y	0.305 MM	0.25 MM	=STANDARD	=STANDARD	=STANDARD

Minimum diff spacing is 4 mil
Table 4-5, Intel Doc# 486712

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
POWER_DDR_P4MM	*	Y	0.400 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_DDR	*	POWER_DDR_P4MM
DDR_CLK_PHY	*	DDR_68D
DDR_CTRL_PHY	*	DDR_39S
DDR_CMD_PHY	*	DDR_34S
DDR_DQ_PHY	*	DDR_42S
DDR_DQS_PHY	*	DDR_42S_D
DDR_COMP_PHY	*	DDR_COMP

DDR3 Power-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_DDR	*	=2:1_SPACING	?

DDR3-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DDR_CLK_ISO	*	=5:1_SPACING	?
DDR_CTRL_ISO	*	=3.5:1_SPACING	?
DDR_CTRL2CTRL	*	=2.5:1_SPACING	?
DDR_CMD_ISO	*	=3.5:1_SPACING	?
DDR_CMD2CMD	*	=2:1_SPACING	?
DDR_DATA_ISO	*	=3:1_SPACING	?
DDR_DQ2DQ	*	=2:1_SPACING	900
DDR_DQ2DQS	*	=3:1_SPACING	?
DDR_BL2BL	*	=3:1_SPACING	?
DDR_CH2CH	*	=6.5:1_SPACING	?
DDR_COMP_ISO	*	0.2 MM	?

Main Segment Min Spacing Rules (mils) (Shark Bay PDG, Intel Doc# 486712)

Table	Trace	Design	Iso	Design	Comments
4-2	4	(diff)	15	19.69	CLK trace spacing controlled by =68_OHM_DIFF
4-3	8	9.84	12	13.78	
4-4	6	7.87	12	13.78	
4-5	8.5	7.87	12	11.81	DQ or DQS to other signals not in the same bytelane (but not ch)
					DQ to DQ in the same bytelane of the same channel
			10	11.81	DQ to DQS in the same bytelane of the same channel
			12	11.81	DQ or DQS in different bytelanes of the same channel
			25	25.59	DQ or DQS in different channels
			-	25.59	DDR3 to any other signal not DDR3

Constraints

Clocks: CK[3:0], CK#[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CLK	*	*	DDR_CLK_ISO

Control: CS#[3:0], CKE[3:0], ODT[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CTRL	*	*	DDR_CTRL_ISO
DDR_CTRL	DDR_CTRL	*	DDR_CTRL2CTRL

Command: MA[15:0], RAS#, CAS#, WE# BS[2:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CMD	*	*	DDR_CMD_ISO
DDR_CMD	DDR_CMD	*	DDR_CMD2CMD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_COMP	*	*	DDR_COMP_ISO

Data: DQS[7:0], DQS#[7:0], DQ[63:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
DDR_A_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_A_DQS*	*	*	DDR_DATA_ISO	
DDR_B_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_B_DQS*	*	*	DDR_DATA_ISO	
DDR_*_DQ_BYTE*	=SAME	*	DDR_DQ2DQ	See Note (3)
DDR_A_DQ_BYTE*	DDR_A_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_A_DQ_BYTE*	DDR_A_DQ_BYTE*	*	DDR_BL2BL	See Note (3)
DDR_B_DQ_BYTE*	DDR_B_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_B_DQ_BYTE*	DDR_B_DQ_BYTE*	*	DDR_BL2BL	
DDR_A_*	DDR_B_*	*	DDR_CH2CH	See Note (2)

Note (1):
Deliberately set DQ to DQS spacing to 3:1 to avoid adding complexity to contraints, even though it can be less. Only one rule per channel is needed by trading off a little space.

Note (2):
Intel suggests 25 mil (0.65 mm) spacing for via to channel, and via to pad to two different channels. DDR3 draws about 20 mA per trace with edge rates in the 100s of ps. The main coupling mechanism is capacitive. A 0.65 mm spacing is used for power nets, which draw far more current (inductive coupling however). These rules are far too conservative. To meet these rules, the spacing must be applied to the net.

Note (3):
In order for the constraints DDR_*_DQ_BYTE* to =SAME to win out over DDR_{A,B}_DQ_BYTE* to DDR_{A,B}_DQ_BYTE* so that the small intra-bytelane spacing is used, the spacing rule DDR_DQ2DQ must have a weight greater than DDR_BL2BL.

DDR3

Electrical Contraint Set	Physical	Spacing		
Channel A				
T17 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<1..0>	? 23
T17 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<1..0>	? 23
T25 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<3..2>	? 82
T25 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<3..2>	? 82
T18 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<1..0>	? 23
T18 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<1..0>	? 23
T18 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<1..0>	? 23
T24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<3..2>	? 82
T24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<3..2>	? 82
T24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<3..2>	? 82
T18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_A<15..0>	? 23
T18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_BA<2..0>	? 23
T18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_RAS_L	? 23
T18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_CAS_L	? 23
T18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_WE_L	? 23
T19 DDR_A_DQ_BYTE0	DDR_DQ_PHY	DDR_A_DQ_BYTE0	MEM_A_DQ<7..0>	? 25
T19 DDR_A_DQ_BYTE1	DDR_DQ_PHY	DDR_A_DQ_BYTE1	MEM_A_DQ<15..8>	? 25
T19 DDR_A_DQ_BYTE2	DDR_DQ_PHY	DDR_A_DQ_BYTE2	MEM_A_DQ<23..16>	? 25
T19 DDR_A_DQ_BYTE3	DDR_DQ_PHY	DDR_A_DQ_BYTE3	MEM_A_DQ<31..24>	? 25
T19 DDR_A_DQ_BYTE4	DDR_DQ_PHY	DDR_A_DQ_BYTE4	MEM_A_DQ<39..32>	? 25
T19 DDR_A_DQ_BYTE5	DDR_DQ_PHY	DDR_A_DQ_BYTE5	MEM_A_DQ<47..40>	? 25
T19 DDR_A_DQ_BYTE6	DDR_DQ_PHY	DDR_A_DQ_BYTE6	MEM_A_DQ<55..48>	? 25
T19 DDR_A_DQ_BYTE7	DDR_DQ_PHY	DDR_A_DQ_BYTE7	MEM_A_DQ<63..56>	? 25
T19 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_P<0>	? 25
T19 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_N<0>	? 25
T19 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_P<1>	? 25
T19 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_N<1>	? 25
T20 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_P<2>	? 25
T20 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_N<2>	? 25
T20 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_P<3>	? 25
T20 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_N<3>	? 25
T20 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_P<4>	? 25
T20 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_N<4>	? 25
T20 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_P<5>	? 25
T20 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_N<5>	? 25
T20 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_P<6>	? 25
T20 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_N<6>	? 25
T21 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_P<7>	? 25
T21 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_N<7>	? 25
Channel B				
T21 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<1..0>	? 24
T21 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<1..0>	? 24
T25 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<3..2>	? 82
T25 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<3..2>	? 82
T21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<1..0>	? 24
T21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<1..0>	? 24
T21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<1..0>	? 24
T25 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<3..2>	? 82
T25 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<3..2>	? 82
T25 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<3..2>	? 82
T21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_A<15..0>	? 24
T21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_BA<2..0>	? 24
T21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_RAS_L	? 24
T22 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_CAS_L	? 24
T22 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_WE_L	? 24
T22 DDR_B_DQ_BYTE0	DDR_DQ_PHY	DDR_B_DQ_BYTE0	MEM_B_DQ<7..0>	? 25
T22 DDR_B_DQ_BYTE1	DDR_DQ_PHY	DDR_B_DQ_BYTE1	MEM_B_DQ<15..8>	? 25
T22 DDR_B_DQ_BYTE2	DDR_DQ_PHY	DDR_B_DQ_BYTE2	MEM_B_DQ<23..16>	? 25
T22 DDR_B_DQ_BYTE3	DDR_DQ_PHY	DDR_B_DQ_BYTE3	MEM_B_DQ<31..24>	? 25
T22 DDR_B_DQ_BYTE4	DDR_DQ_PHY	DDR_B_DQ_BYTE4	MEM_B_DQ<39..32>	? 25
T22 DDR_B_DQ_BYTE5	DDR_DQ_PHY	DDR_B_DQ_BYTE5	MEM_B_DQ<47..40>	? 25
T22 DDR_B_DQ_BYTE6	DDR_DQ_PHY	DDR_B_DQ_BYTE6	MEM_B_DQ<55..48>	? 25
T22 DDR_B_DQ_BYTE7	DDR_DQ_PHY	DDR_B_DQ_BYTE7	MEM_B_DQ<63..56>	? 25
T23 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_P<0>	? 25
T23 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_N<0>	? 25
T23 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_P<1>	? 25
T23 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_N<1>	? 25
T23 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_P<2>	? 25
T23 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_N<2>	? 25
T23 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_P<3>	? 25
T23 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_N<3>	? 25
T23 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_P<4>	? 25
T23 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_N<4>	? 25
T24 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_P<5>	? 25
T24 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_N<5>	? 25
T24 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_P<6>	? 25
T24 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_N<6>	? 25
T24 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_P<7>	? 25
T24 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_N<7>	? 25
Reset				
T24	DDR_50S		MEM_RESET_L	21 23 24
SM COMP				
T25	DDR_COMP_PHY	DDR_COMP	CPU_SM_RCOMP<0..2>	6

SYNC_MASTER=J16_NICK SYNC_DATE=06/03/2013

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Apple Inc.

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PCI Express/DMI

PCIe-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
PCIE_COMP	*	Y	0.305 MM	0.25 MM	=STANDARD	=STANDARD	=STANDARD
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE3_PHY	*	PCIE_80D
CLK_PCIE_PHY	*	PCIE_90D
COMP_PCIE_PHY	*	PCIE_COMP
CPU_ASYNC_PHY	*	CPU_50S

PCIe and DMI Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
4-5	50	50	15	15.75	PCIe. Impedance inferred from Table 4-7.
4-7	50	50	8	15.75	DMI. Numbers based on Intel stack-up.

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_ISO	*	=5:1_SPACING	?
COMP_PCIE_ISO	*	=2:1_SPACING	?
CPU_ASYNC_ISO	*	=2.5:1_SPACING	?
CPU_MS_ISO	TOP,BOTTOM	=4.5:1_SPACING	?
CPU_MS_ISO	*	=3:1_SPACING	?

Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	*	*	CLK_PCIE_ISO
COMP_PCIE	*	*	COMP_PCIE_ISO
PEG_R2D	PEG_R2D	*	PEG_SAME_DIR
PEG_D2R	PEG_D2R	*	PEG_SAME_DIR
PEG_D2R	PEG_R2D	*	PEG_ALT_DIR
PEG_D2R	*	*	PEG_ISO
PEG_R2D	*	*	PEG_ISO
CPU_ASYNC	*	*	CPU_ASYNC_ISO
CPU_ASYNC_MS	*	*	CPU_MS_ISO

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
PEG_SAME_DIR	*	=3.5X_DIELECTRIC	?
PEG_ALT_DIR	*	=7X_DIELECTRIC	?
PEG_ISO	*	=4:1_SPACING	?

PEG Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
4.2.1	80	80	16	15.75	PCIe Gen3. Allow looser spacing for same direction on stripline per Anil

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing		
x16 Graphics				
1440 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<15>	72
1441 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<15>	72
1442	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<15>	72 81
1443	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<15>	72 81
1444 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<15>	72 81
1445 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<15>	72 81
1446	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<15>	72
1447	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<15>	72
1448 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<14>	72
1449 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<14>	72
1450	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<14>	72 81
1451	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<14>	72 81
1452 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<14>	72 81
1453 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<14>	72 81
1454	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<14>	72
1455	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<14>	72
1456 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<13>	72
1457 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<13>	72
1458	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<13>	72 81
1459	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<13>	72 81
1460 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<13>	72 81
1461 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<13>	72 81
1462	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<13>	72
1463	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<13>	72
1464 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<12>	72
1465 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<12>	72
1466	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<12>	72 81
1467	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<12>	72 81
1468 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<12>	72 81
1469 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<12>	72 81
1470	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<12>	72
1471	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<12>	72
1472 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<11>	72
1473 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<11>	72
1474	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<11>	72 81
1475	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<11>	72 81
1476 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<11>	72 81
1477 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<11>	72 81
1478	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<11>	72
1479	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<11>	72
1480 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<10>	72
1481 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<10>	72
1482	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<10>	72 81
1483	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<10>	72 81
1484 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<10>	72 81
1485 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<10>	72 81
1486	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<10>	72
1487	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<10>	72
1488 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<9>	72
1489 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<9>	72
1490	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<9>	72 81
1491	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<9>	72 81
1492 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<9>	72 81
1493 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<9>	72 81
1494	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<9>	72
1495	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<9>	72
1496 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<8>	72
1497 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<8>	72
1498	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<8>	72 81
1499	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<8>	72 81
1500 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<8>	72 81
1501 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<8>	72 81
1502	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<8>	72
1503	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<8>	72

CPU ASYNCHRONOUS

Electrical Contraint Set	Physical	Spacing		
1572	CPU_ASYNC_PHY	CPU_ASYNC	CPU_PROCHOT_L	6 44 45 61
1574	CPU_ASYNC_PHY	CPU_ASYNC	CPU_PROCHOT_R_L	6
1575 PECI	SMC_3xCTRL	SMC_GEN	CPU_PECI	6 14 44 45
1588 PECI	CPU_ASYNC_PHY	CPU_ASYNC_MS	CPU_PECI_R	45
1577	CPU_ASYNC_PHY	CPU_ASYNC	CPU_CATERR_L	6 45
1584	CPU_ASYNC_PHY	CPU_ASYNC	SMC_CPU_CATERR_L	44 45
1579	CPU_ASYNC_PHY	CPU_ASYNC	CPU_PWRGD	6 14 18
1585	CPU_ASYNC_PHY	CPU_ASYNC	XDP_CPU_PWRGD	18
1586	CPU_ASYNC_PHY	CPU_ASYNC	PCH_PROCPWRGD	14
1576	CPU_ASYNC_PHY	CPU_ASYNC	PM_SYNC	6 12
1580	CPU_ASYNC_PHY	CPU_ASYNC	PM_THRMTRIP_L	14 45
1581	CPU_ASYNC_PHY	CPU_ASYNC	PM_THRMTRIP_L_R	14
1583	CPU_ASYNC_PHY	CPU_ASYNC	CPU_RESET_L	6 14 18
1582	CPU_ASYNC_PHY	CPU_ASYNC	XDP_CPURST_L	18
1582 XDP_BPM_L	CPU_ASYNC_PHY	CPU_ASYNC	XDP_BPM_L<1..0>	6 18

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing		
x16 Graphics				
1505 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<7>	72
1506 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<7>	72
1507	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<7>	72 81
1508	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<7>	72 81
1509 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<7>	72 81
1510 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<7>	72 81
1511	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<7>	72
1512	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<7>	72
1513 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<6>	72
1514 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<6>	72
1515	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<6>	72 81
1516	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<6>	72 81
1517 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<6>	72 81
1518 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<6>	72 81
1519	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<6>	72
1520	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<6>	72
1521 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<5>	72
1522 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<5>	72
1523	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<5>	72 81
1524	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<5>	72 81
1525 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<5>	72 81
1526 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<5>	72 81
1527	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<5>	72
1528	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<5>	72
1529 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<4>	72
1530 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<4>	72
1531	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<4>	72 81
1532	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<4>	72 81
1533 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<4>	72 81
1534 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<4>	72 81
1535	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<4>	72
1536	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<4>	72
1537 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<3>	72
1538 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<3>	72
1539	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<3>	72 81
1540	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<3>	72 81
1541 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<3>	72 81
1542 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<3>	72 81
1543	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<3>	72
1544	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<3>	72
1545 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<2>	72
1546 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<2>	72
1547	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<2>	72 81
1548	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<2>	72 81
1549 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<2>	72 81
1550 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<2>	72 81
1551	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<2>	72
1552	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<2>	72
1553 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<1>	72
1554 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<1>	72
1555	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<1>	72 81
1556	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<1>	72 81
1557 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<1>	72 81
1558 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<1>	72 81
1559	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<1>	72
1560	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<1>	72
1561 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<0>	72
1562 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<0>	72
1563	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<0>	72 81
1564	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<0>	72 81
1565 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<0>	72 81
1566 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<0>	72 81
1567	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<0>	72
1568	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<0>	72
CPU PCIe Clocks				
1569 PEG_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_P	11 72
1570 PEG_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_N	11 72
CPU PCIe Compensation				
1571	COMP_PCIE_PHY	COMP_PCIE	CPU_PEG_RCOMP	5
CPU eDP Compensation				
1573	COMP_PCIE_PHY	COMP_PCIE	CPU_EDP_RCOMP	5
1572	COMP_PCIE_PHY	COMP_PCIE	CPU_CFG_RCOMP	6

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Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_PHY	*	PCIE_85D
COMP_DMI_PHY	*	DMI_COMP

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
PCIE_SAME_DIR	*	=3.5X_DIELECTRIC	?
PCIE_ALT_DIR	*	=7X_DIELECTRIC	?
PCIE_ISO	*	=4:1_SPACING	?

TBT x4 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_TBT_R2D	PCIE_TBT_R2D	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_D2R	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_R2D	*	PCIE_ALT_DIR
PCIE_TBT_D2R	*	*	PCIE_ISO
PCIE_TBT_R2D	*	*	PCIE_ISO

PCH x1 PCIE Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE	*	*	PCIE_ISO

DMI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
DMI_SAME_DIR	*	=4X_DIELECTRIC	?
DMI_ALT_DIR	*	=5X_DIELECTRIC	?
DMI_ISO	*	=4X_DIELECTRIC	?

DMI x4 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_N2S	DMI_N2S	*	DMI_SAME_DIR
DMI_S2N	DMI_S2N	*	DMI_SAME_DIR
DMI_N2S	DMI_S2N	*	DMI_ALT_DIR
DMI_N2S	*	*	DMI_ISO
DMI_S2N	*	*	DMI_ISO

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DMI_COMP	*	Y	0.2032 MM	0.2032 MM	3 MM	=STANDARD	=STANDARD

PCIe (PCH)

Electrical Contraint Set	Physical	Spacing		
x4 Thunderbolt				
H132 PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_P<3..0>	26
H133 PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_N<3..0>	26
H134	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_P<3..0>	13 26
H135	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_N<3..0>	13 26
H136 PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_P<3..0>	13 26
H137 PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_N<3..0>	13 26
H138	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_P<3..0>	26
H139	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_N<3..0>	26
H140 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_P	11 26
H141 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_N	11 26
x1 AirPort				
H142 PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_P	32
H143 PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_N	32
H144	PCIE_PHY	PCIE	PCIE_AP_R2D_C_P	13 32
H145	PCIE_PHY	PCIE	PCIE_AP_R2D_C_N	13 32
H146 PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_P	13 32
H147 PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_N	13 32
H148 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_P	11 32
H149 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_N	11 32
x1 Caesar IV				
H150 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_P	35
H151 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_N	35
H152	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_P	13 35
H153	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_N	13 35
H154 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_P	13 35
H155 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_N	13 35
H156	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_P	35
H157	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_N	35
H158 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_P	11 35
H159 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_N	11 35
x2 SSD				
H172 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_SSD_P	11 33
H173 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_SSD_N	11 33
PCH PCIE Compensation				
H174	COMP_DMI_PHY	COMP_PCIE	PCH_PCIE_RCOMP	13

DMI

Electrical Contraint Set	Physical	Spacing		
DMI				
H160 DMI_N2S	PCIE_PHY	DMI_N2S	DMI_N2S_P<3..0>	5 12
H161 DMI_N2S	PCIE_PHY	DMI_N2S	DMI_N2S_N<3..0>	5 12
H162 DMI_S2N	PCIE_PHY	DMI_S2N	DMI_S2N_P<3..0>	5 12
H163 DMI_S2N	PCIE_PHY	DMI_S2N	DMI_S2N_N<3..0>	5 12
H164 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_P	6 11
H165 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_N	6 11
DMI Compensation				
H171	COMP_DMI_PHY	COMP_PCIE	PCH_DMI_RCOMP	12

CPU DP REF CLK

Electrical Contraint Set	Physical	Spacing		
CPU DP REF CLK				
H175 CPU_CLK135_PLL	PCIE_PHY	CLK_PCIE	CPU_CLK135M_DPLLREF_N	6 11
H176 CPU_CLK135_PLL	PCIE_PHY	CLK_PCIE	CPU_CLK135M_DPLLREF_P	6 11
H177 CPU_CLK135_PLL	PCIE_PHY	CLK_PCIE	CPU_CLK135M_DPLLSS_N	6 11
H178 CPU_CLK135_PLL	PCIE_PHY	CLK_PCIE	CPU_CLK135M_DPLLSS_P	6 11

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SATA

SATA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SATA_PHY	*	SATA_85D
COMP_SATA_PHY	*	PCIE_COMP
SATA_PHY_90	*	SATA_90D

SATA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ISO	*	=6:1_SPACING	?
COMP_SATA_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA	*	*	SATA_ISO
COMP_SATA	*	*	COMP_SATA_ISO

SATA Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
15.2.1	90	95	20	23.62	SATA Gen2, SATA Gen3

SATA Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
15-3	50	50	15	15.75	SATA Gen2, SATA Gen3

FDI

FDI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FDI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
COMP_FDI	*	Y	0.25 MM	0.25 MM	3 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
FDI_SE_PHY	*	FDI_50S
COMP_FDI_PHY	*	COMP_FDI

FDI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FDI_ISO	*	=3:1_SPACING	?
COMP_FDI_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FDI	*	*	FDI_ISO
COMP_FDI	*	*	COMP_FDI_ISO

FDI Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Table	Imp	Design	Iso	Design	Comments
6-1/6-2	85	85	12	11.81	FDI main length

FDI Compensation Rules (mils)

Table	Trace	Design	Iso	Design	Comments
6-4	10	11.81	-	15.75	Using PCIe guidelines

XDP

XDP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
XDP_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
XDP_PHY	*	XDP_55S

XDP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XDP_ISO	*	=2:1_SPACING	?
CLK_JTAG_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XDP	*	*	XDP_ISO
CLK_JTAG	*	*	CLK_JTAG_ISO

Desktop Debug Design Guide (Intel Doc# 430883)

Section	Imp	Design	Iso	Design	Comments
1.5	45-65	55	-	15.75	Isolation is for JTAG clocks. All signals default are 50 Ohm SE.

SATA

Electrical Contraint Set	Physical	Spacing		
PCH SATA Port 0 (HDD)				
SATA_R2D	SATA_PHY_90	SATA	SATA_HDD_R2D_P	33
SATA_R2D	SATA_PHY_90	SATA	SATA_HDD_R2D_N	33
	SATA_PHY_90	SATA	SATA_HDD_R2D_C_P	11 33
	SATA_PHY_90	SATA	SATA_HDD_R2D_C_N	11 33
SATA_D2R	SATA_PHY_90	SATA	SATA_HDD_D2R_P	11 33
SATA_D2R	SATA_PHY_90	SATA	SATA_HDD_D2R_N	11 33
	SATA_PHY_90	SATA	SATA_HDD_D2R_C_P	33
	SATA_PHY_90	SATA	SATA_HDD_D2R_C_N	33
PCH SATA Port 1 (SSD)				
SATA_SSD_R2D	SATA_PHY	SATA	SSD_R2D_P<0..1>	11 33
SATA_SSD_R2D	SATA_PHY	SATA	SSD_R2D_N<0..1>	11 33
SATA_SSD_R2D	SATA_PHY	SATA	SSD_R2D_C_P<0..1>	33
SATA_SSD_R2D	SATA_PHY	SATA	SSD_R2D_C_N<0..1>	33
SATA_SSD_D2R	SATA_PHY	SATA	SSD_D2R_P<0..1>	11 33
SATA_SSD_D2R	SATA_PHY	SATA	SSD_D2R_N<0..1>	11 33
PCH SATA Compensation				
	COMP_SATA_PHY	COMP_SATA	PCH_SATA_RCOMP	11

FDI

Electrical Contraint Set	Physical	Spacing		
FDI				
	FDI_SE_PHY	FDI	FDI_CSYNC	5 12
	FDI_SE_PHY	FDI	FDI_INT	5 12
FDI Compensation				
	COMP_FDI_PHY	COMP_FDI	PCH_FDI_RCOMP	12

XDP

Electrical Contraint Set	Physical	Spacing		
CPU XDP				
	XDP_PHY	XDP	XDP_BPM_L<7..2>	6 18
CPU_CFG	XDP_PHY	XDP	CPU_CFG<17..4>	6 18 82
CPU_CFG_3	XDP_PHY	XDP	CPU_CFG<3>	6 18
CPU_CFG	XDP_PHY	XDP	CPU_CFG<2..0>	6 18
ITP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_P	
ITP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_N	
	CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_P	11 82
	CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_N	11 82
	CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_P	
	CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_N	
	XDP_PHY	CLK_JTAG	XDP_CPU_TCK	6 18
	XDP_PHY	XDP	XDP_CPU_TMS	6 18
	XDP_PHY	XDP	XDP_CPU_TDI	6 18
	XDP_PHY	XDP	XDP_CPU_TDO	6 18
PCH XDP				
	XDP_PHY	CLK_JTAG	XDP_PCH_TCK	11 18
	XDP_PHY	XDP	XDP_PCH_TMS	11 18
	XDP_PHY	XDP	XDP_PCH_TDI	11 18
	XDP_PHY	XDP	XDP_PCH_TDO	11 18

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PCH

PCH-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

PCH-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	=4:1_SPACING	?
COMP_PCH	*	=2:1_SPACING	?

PCI

PCI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

PCI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCI	*	=2:1_SPACING	?

LPC

LPC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

LPC-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5:1_SPACING	?
CLK_LPC	*	=2:1_SPACING	?

HDA

HDA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

HDA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

Crystal

Crystal-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

Crystal-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

SPI

SPI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=2:1_SPACING	?

PCI

Electrical Contraint Set	Physical	Spacing		
PCI Clock				
E33	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIIN	11 19
E32	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIOUT	11 19

LPC

Electrical Contraint Set	Physical	Spacing		
LPC				
E32	LPC_55S	LPC	LPC_AD<3..0>	13 44 46
E33	LPC_55S	LPC	LPC_AD_R<3..0>	13
E33	LPC_55S	LPC	LPC_FRAME_L	13 44 46
E37	LPC_55S	LPC	LPC_FRAME_R_L	13
LPC Clocks				
E33	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	19 46
E34	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	11 19
E43	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	19 44
E42	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	11 19

PCH Clocks

Electrical Contraint Set	Physical	Spacing		
PCH Reference Clock				
E18	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_SB	11 19
E40	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_SB_R	11
PCH RTC 32K				
E44	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	11 19
E45	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	11 19
E52	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2_R	19
SMC 32K				
E24	CLK_PCH_55S	CLK_PCH	PM_CLK32K_SUSCLK_R	12 45
F50	CLK_PCH_55S	CLK_PCH	SMC_CLK32K	44 45

25 MHz Reference Clocks

Electrical Contraint Set	Physical	Spacing		
25M Reference Crystal				
E52	CLK_XTAL	XTAL	SYSCLK_CLK25M_X1	19
E46	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2	19
E47	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2_R	19
25M Reference Clocks				
E16	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_ENET	19 35
E16	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_ENET_R	19
E48	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_TBT	19 26
E48	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_TBT_R	26

HDA

Electrical Contraint Set	Physical	Spacing		
HDA				
E33	HDA_55S	HDA	HDA_BIT_CLK	11 52
E34	HDA_55S	HDA	HDA_BIT_CLK_R	11
E36	HDA_55S	HDA	HDA_RST_L	11 52
E40	HDA_55S	HDA	HDA_RST_R_L	11
E46	HDA_55S	HDA	HDA_SDOUT	11 52
E36	HDA_55S	HDA	HDA_SDOUT_R	11 19
E36	HDA_55S	HDA	HDA_SYNC	11 52
E36	HDA_55S	HDA	HDA_SYNC_R	11
E36	HDA_55S	HDA	HDA_SDIN0	11 52
E36	HDA_55S	HDA	AUD_SDI_R	52
SPDIF				
E37		HDA	AUD_SPDIF_CHIP	52
E37		HDA	AUD_SPDIF_OUT	52 56

SPI Bootrom

Electrical Contraint Set	Physical	Spacing		
SPI ROM				
E31	SPI_50S	SPI	SPI_CLK_R	13 46
E42	SPI_50S	SPI	SPI_CLK	46
E39	SPI_50S	SPI	SPI_ALT_CLK	46
E40	SPI_50S	SPI	SPI_SMC_CLK	44 46
E40	SPI_50S	SPI	SPI_MLB_CLK	46
E34	SPI_50S	SPI	SPI_CS0_R_L	13 46
E33	SPI_50S	SPI	SPI_CS0_L	46
E38	SPI_50S	SPI	SPI_ALT_CS_L	46
E40	SPI_50S	SPI	SPI_SMC_CS_L	44 46
E37	SPI_50S	SPI	SPI_MLB_CS_L	46
E39	SPI_50S	SPI	SPI_MOSI_R	13 46
E40	SPI_50S	SPI	SPI_MOSI	46
E40	SPI_50S	SPI	SPI_ALT_MOSI	46
E41	SPI_50S	SPI	SPI_SMC_MOSI	44 46
E41	SPI_50S	SPI	SPI_MLB_MOSI	46
E40	SPI_50S	SPI	SPI_MISO	13 46
E40	SPI_50S	SPI	SPI_ALT_MISO	46
E41	SPI_50S	SPI	SPI_SMC_MISO	44 46
E41	SPI_50S	SPI	SPI_MLB_MISO	46
E40	SPI_50S	SPI	SPIROM_USE_MLB	14 46

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USB

USB-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB2_PHY	*	USB_90D
USB3_PHY	*	USB_85D

USB-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2_ISO	*	=3:1_SPACING	?
USB2_ISO	TOP,BOTTOM	=3:1_SPACING	?
USB3_ISO	*	=5.5:1_SPACING	?
USB3_ISO	TOP,BOTTOM	=5.5:1_SPACING	?

USB Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
12.2.1	90	90	12	11.81	USB 2.0
13.3.1	85	85	20	21.65	USB 3.0

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB2	*	*	USB2_ISO
USB3	*	*	USB3_ISO

Caesar IV (Ethernet/SD)

CIV-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
ENET_COMP_PHY	*	ENET_50S
ENET_DIFF_PHY	*	ENET_100D
SD_PHY	*	SD_50S
CIV_SPI	*	SPI_55S

CIV-specific Spacing Definitions

Ethernet

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF_ISO	*	=6:1_SPACING	?
ENET_DIFF2DIFF	*	=3:1_SPACING	?
ENET_TRANS_ISO	*	1.27 MM	?
COMP_ENET_ISO	*	=4:1_SPACING	?

SD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_ISO	*	=3:1_SPACING	?

Constraints

Ethernet

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	*	*	ENET_DIFF_ISO
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_TRANS	*	*	ENET_TRANS_ISO
COMP_ENET	*	*	COMP_ENET_ISO
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF

2 kV isolation

SD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SD	*	*	SD_ISO

Camera Processor-to-Camera Sensor I/F (SMIA/MIPI)

Camera Processor's SMIA Interface Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMIA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMIA_DIFF_PHY	*	SMIA_100D

Camera Processor's SMIA Interface Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMIA_DIFF_ISO	*	=6:1_SPACING	?
SMIA_DIFF2DIFF	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMIA_DIFF	*	*	SMIA_DIFF_ISO
SMIA_DIFF	SMIA_DIFF	*	SMIA_DIFF2DIFF

USB 3.0 and USB 2.0 Trixies Muxing

Electrical Contraint Set	Physical	Spacing		
External Port A (J4600)				
142 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_P	42
142 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_N	42
143	USB3_PHY	USB3	USB3_EXTA_RX_F_P	13 42
143	USB3_PHY	USB3	USB3_EXTA_RX_F_N	13 42
141 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_P	13 42
141 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_N	13 42
141	USB3_PHY	USB3	USB3_EXTA_TX_F_P	42
141	USB3_PHY	USB3	USB3_EXTA_TX_F_N	42
140	USB3_PHY	USB3	USB3_EXTA_TX_C_P	42
140	USB3_PHY	USB3	USB3_EXTA_TX_C_N	42
141 USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_EXTA_0_P	13 42
141 USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_EXTA_0_N	13 42
141	USB2_PHY	USB2	USB2_EXTA_MUXED_P	42
142	USB2_PHY	USB2	USB2_EXTA_MUXED_N	42
139	USB2_PHY	USB2	USB2_EXTA_P	42
139	USB2_PHY	USB2	USB2_EXTA_N	42
External Port B (J4610)				
142 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_P	42
142 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_N	42
142	USB3_PHY	USB3	USB3_EXTB_RX_F_P	13 42
142	USB3_PHY	USB3	USB3_EXTB_RX_F_N	13 42
142 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_P	13 42
142 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_N	13 42
142	USB3_PHY	USB3	USB3_EXTB_TX_F_P	42
142	USB3_PHY	USB3	USB3_EXTB_TX_F_N	42
149	USB3_PHY	USB3	USB3_EXTB_TX_C_P	42
149	USB3_PHY	USB3	USB3_EXTB_TX_C_N	42
142 USB2_CONN	USB2_PHY	USB2	USB_EXTB_8_P	13 42
143 USB2_CONN	USB2_PHY	USB2	USB_EXTB_8_N	13 42
143	USB2_PHY	USB2	USB2_EXTB_P	42
143	USB2_PHY	USB2	USB2_EXTB_N	42
External Port C (J4700)				
143 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_P	43
143 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_N	43
143	USB3_PHY	USB3	USB3_EXTC_RX_F_P	13 43
144	USB3_PHY	USB3	USB3_EXTC_RX_F_N	13 43
144 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_P	13 43
144 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_N	13 43
144	USB3_PHY	USB3	USB3_EXTC_TX_F_P	43
144	USB3_PHY	USB3	USB3_EXTC_TX_F_N	43
140	USB3_PHY	USB3	USB3_EXTC_TX_C_P	43
140	USB3_PHY	USB3	USB3_EXTC_TX_C_N	43
144 USB2_CONN	USB2_PHY	USB2	USB_EXTC_1_P	13 43
144 USB2_CONN	USB2_PHY	USB2	USB_EXTC_1_N	13 43
145	USB2_PHY	USB2	USB2_EXTC_P	43
145	USB2_PHY	USB2	USB2_EXTC_N	43
External Port D (J4710)				
145 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_P	43
145 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_N	43
145	USB3_PHY	USB3	USB3_EXTD_RX_F_P	13 43
145	USB3_PHY	USB3	USB3_EXTD_RX_F_N	13 43
145 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_P	13 43
145 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_N	13 43
146	USB3_PHY	USB3	USB3_EXTD_TX_F_P	43
145	USB3_PHY	USB3	USB3_EXTD_TX_F_N	43
149	USB3_PHY	USB3	USB3_EXTD_TX_C_P	43
150	USB3_PHY	USB3	USB3_EXTD_TX_C_N	43
146 USB2_CONN	USB2_PHY	USB2	USB_EXTD_9_P	13 43
146 USB2_CONN	USB2_PHY	USB2	USB_EXTD_9_N	13 43
146	USB2_PHY	USB2	USB2_EXTD_P	43
146	USB2_PHY	USB2	USB2_EXTD_N	43
Camera (J3510)				
152 USB2_CONN_INT	USB2_PHY	USB2	USB_CAMERA_P	13 38
152 USB2_CONN_INT	USB2_PHY	USB2	USB_CAMERA_N	13 38
PCH USB Compensation				
118	PCH_55S	COMP_PCH	PCH_USB_RBIAS	13

RMH Love

Electrical Contraint Set	Physical	Spacing		
140 USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_P	13 32
141 USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_N	13 32
150 USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_MUX_P	32
150 USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_MUX_N	32

Et tu Brute?

Electrical Contraint Set	Physical	Spacing		
Ethernet				
147 ENET_MDI	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_P<3..0>	35 36
147 ENET_MDI	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_N<3..0>	35 36
147	ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_P<3..0>	36
147	ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_N<3..0>	36
151		ENET_TRANS	ENETCONN_MCT0	36
152		ENET_TRANS	ENETCONN_MCT1	36
152		ENET_TRANS	ENETCONN_MCT2	36
152		ENET_TRANS	ENETCONN_MCT3	36
152		ENET_TRANS	ENETCONN_MCT_BS	36
147	ENET_COMP_PHY	COMP_ENET	ENET_RDAC	35
SD				
147 SD_DATA	SD_PHY	SD	ENET_CR_DATA<7..0>	35
148	SD_PHY	SD	SDCONN_DATA<7..0>	35 37
151	SD_PHY	SD	SDCONN_DATA_R_<7..0>	
148 SD_CMD	SD_PHY	SD	ENET_SD_CMD	35
148	SD_PHY	SD	SDCONN_CMD	35 37
151	SD_PHY	SD	SDCONN_CMD_R	
148 SD_CLK	SD_PHY	SD	ENET_SD_CLK	35
148	SD_PHY	SD	SDCONN_CLK	35 37
148	SD_PHY	SD	SDCONN_CLK_R	37
148	SD_PHY	SD	ENET_MEDIA_SENSE	11 35
148	SD_PHY	SD	ENET_SD_DETECT_L	35 37
CIV SPI				
152	CIV_SPI	SPI	ENET_SCLK	35
148	CIV_SPI	SPI	ENET_MISO	35
152	CIV_SPI	SPI	ENET_MOSI	35
152	CIV_SPI	SPI	ENET_CS_L	35

Camera Processor-Camera Sensor I/F

Electrical Contraint Set	Physical	Spacing		
159 SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_P	38
159 SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_N	38
159 SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_P	38
159 SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_N	38
159	SPI_50S	SPI	CAM_SF_CLK	38
160	SPI_50S	SPI	CAM_SF_CLK_R	38
160	SPI_50S	SPI	CAM_SF_DIN	38
161	SPI_50S	SPI	CAM_SF_DIN_R	38
161	SPI_50S	SPI	CAM_SF_CS_L	38
161	SPI_50S	SPI	CAM_SF_WP_L	38
161	SPI_50S	SPI	CAM_SF_DOUT	38
161	SPI_50S	SPI	CAM_SF_DOUT_R	38
161	SMB_PHY	SMB	I2C_CAMSENSOR_SDA	38
161	SMB_PHY	SMB	I2C_CAMSENSOR_SCL	38

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SMBus

SMBus-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMB_PHY	*	SMB_55S

SMBus-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB_ISO	*	=2x_DIELECTRIC	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMB	*	*	SMB_ISO

Sensor

Sensor-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_DIFF_PHY	*	1:1_DIFFPAIR

Sensor-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE_ISO	*	=1.5:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SENSE	*	*	SENSE_ISO
SENSE	POWER	*	PWR_P2MM
SENSE	GND	*	GND_P2MM

SMC Generic Control Line Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMC_ISO	*	=1:1_SPACING	?
SMC_3xISO	*	=3:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMC_CTRL	*	*	SMC_ISO
SMC_3XCTRL	*	*	SMC_3xISO

SMC Generic Control Line Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MINIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMC_GEN	*	SMC_50S

Current/Voltage Sense

Electrical Contraint Set	Physical	Spacing		
Common				
I3		SENSE	GND_SMC_AVSS	44 45 48 49
12V S5 (System Total)				
I4	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VG3H_P 48
I5	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VG3H_N 48
I6			SENSE	ISNS_P12VG3H_R 48
I7			SENSE	ISNS_P12VG3H 45 48
I8			SENSE	VSNS_P12VG3H 45 48
12V S0 (GPU Core)				
I22	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUCORE_P 48
I23	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUCORE_N 48
I24			SENSE	ISNS_P12VS0_GPUCORE_R 48
I25			SENSE	ISNS_P12VS0_GPUCORE 45 48
I26			SENSE	VSNS_P12VS0_GPUCORE 45 48
HDD				
I80	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_HDD_P 48
I82	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_HDD_N 48
I81			SENSE	ISNS_HDDS0_R 48
I83			SENSE	ISNS_HDDS0 45 48
I84			SENSE	VSNS_HDDS0 45 48
GPU Core (alternate low side sense)				
I119	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_GPUCORE_P
I120	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_GPUCORE_N
I118			SENSE	ISNS_GPUCORE_ALT 45 48
I122			SENSE	VSNS_GPUCORE_ALT 45 48
SSD				
I85	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_SSD_P 49
I87	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_SSD_N 49
I86			SENSE	ISNS_SSDS0_R 49
I88			SENSE	ISNS_SSDS0 45 49
I89			SENSE	VSNS_P3V3S5 45 49
VDDQ S3 (DDR)				
I33	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_VDDQS3_DDR_P 49
I32	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_VDDQS3_DDR_N 49
I35			SENSE	ISNS_VDDQS3_DDR_R 49
I34			SENSE	ISNS_VDDQS3_DDR 45 49
I36			SENSE	VSNS_VDDQS3_DDR 45 49
VDDQ S0 (GPU FBVDDQ)				
I37	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_FBVDDQ_P 48
I38	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_FBVDDQ_N 48
I39			SENSE	ISNS_P12VS0_FBVDDQ_R 48
I40			SENSE	ISNS_P12VS0_FBVDDQ 45 48
I138			SENSE	VSNS_P12VS0_FBVDDQ 45 48
CPU Core				
I44			SENSE	ISNS_CPUVCC_FB 48
I45			SENSE	ISNS_CPUVCC 45 48
I46			SENSE	VSNS_CPUVCC 45 48
PP1V05_S0_PCH				
I110			SENSE	VSNS_P1V05S0_PCH 45 48
PP1V5_S0				
I113	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P1V5S0_P 49
I115	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P1V5S0_N 49
I112			SENSE	ISNS_P1V5S0_R 49
I114			SENSE	ISNS_P1V5S0 45 49
I116			SENSE	VSNS_P1V5S0 45 49
Airport				
I107	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P3V3S4_AP_P
I105	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P3V3S4_AP_N
I104			SENSE	ISNS_P3V3S4_AP_R
I106			SENSE	ISNS_P3V3S4_AP

SMC

Electrical Contraint Set	Physical	Spacing		
SMC				
H125	CLK_XTAL	XTAL	SMC_XTAL_R	45
H1	CLK_XTAL	XTAL	SMC_XTAL	44 45
H2	CLK_XTAL	XTAL	SMC_EXTAL	44 45
H91	SMC_GEN	SMC_CTRL	SMC_LRESET_L	20 44
H90	SMC_GEN	SMC_CTRL	SMC_RUNTIME_SCI_L	14 44
H92	SMC_GEN	SMC_CTRL	SMC_WAKE_SCI_L	14 44
H93	SMC_GEN	SMC_CTRL	SMC_FAN_0_CTL	44 51
H94	SMC_GEN	SMC_CTRL	SMC_FAN_0_TACH	44 51
H95	SMC_GEN	SMC_3XCTRL	SMC_PECI_L	44 45
H96	SMC_GEN	SMC_3XCTRL	SMC_PECI_L_R	45

SMBus

Electrical Contraint Set	Physical	Spacing		
SMC				
H10	SMB_PHY	SMB	SMBUS_SMC_0_S0_SCL	44 47
H9	SMB_PHY	SMB	SMBUS_SMC_0_S0_SDA	44 47
H11	SMB_PHY	SMB	SMBUS_SMC_1_S0_SCL	44 47
H12	SMB_PHY	SMB	SMBUS_SMC_1_S0_SDA	44 47
H13	SMB_PHY	SMB	SMBUS_SMC_2_S4_SCL	44 47
H14	SMB_PHY	SMB	SMBUS_SMC_2_S4_SDA	44 47
H15	SMB_PHY	SMB	SMBUS_SMC_3_SCL	44 47
H16	SMB_PHY	SMB	SMBUS_SMC_3_SDA	44 47
H19	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SCL	44 45
H20	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SDA	44 45
H126	SMB_PHY	SMB	SMBUS_SMC_4_ASF_SCL	44 45
H127	SMB_PHY	SMB	SMBUS_SMC_4_ASF_SDA	44 45
PCH				
H51	TBT_I2C_5SS	TBT_I2C	SMBUS_PCH_CLK	13 47
H52	TBT_I2C_5SS	TBT_I2C	SMBUS_PCH_DATA	13 47
H53	SMB_PHY	SMB	SML_PCH_0_CLK	13 47
H54	SMB_PHY	SMB	SML_PCH_0_DATA	13 47
H124	SMB_PHY	SMB	SML_PCH_1_CLK	13 47
H125	SMB_PHY	SMB	SML_PCH_1_DATA	13 47
Display TCon				
H55	SMB_PHY	SMB	SMB_DP_TCON_SCL	40 47
H56	SMB_PHY	SMB	SMB_DP_TCON_SDA	40 47

Temperature Sense

Electrical Contraint Set	Physical	Spacing		
EMC1414-1 (Production)				
H57	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_1_P 50
H58	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_1_N 50
H59	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_3_P 50
H60	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_3_N 50
H65	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_ACDC_P 50 60
H66	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_ACDC_N 50 60
H123		SNS_DIFF_PHY	SENSE	SNS_T1_2_P 50
H120		SNS_DIFF_PHY	SENSE	SNS_T1_2_N 50
TMP423 (Development)				
H67	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_1_P 50
H68	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_1_N 50
H69	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_2_P 50
H70	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_2_N 50
H71	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_3_P 50
H72	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_3_N 50
HDD Out-of-Band				
H73			SENSE	HDD_OOB1_D2R_L 34
H74			SENSE	HDD_OOB1_D2R_F_L 34
H75			SENSE	HDD_OOB1_D2R_R_L 34
H117			SENSE	SMC_OOB1_D2R_L 34 44
H76			SENSE	SMC_OOB1_R2D_L 34 44
H118			SENSE	SMC_OOB1_R2D_R_L 34
SSD Out-of-Band				
H77			SENSE	SMC_OOB2_R2D_L 33 45
H78			SENSE	SMC_OOB2_D2R_L 33 45

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DC-DC

Power-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GND_P3MM	*	Y	0.300 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
GND_P5MM	*	Y	0.500 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
POWER_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
POWER_P3MM	*	Y	0.300 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
POWER_P6MM	*	Y	0.600 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND	*	GND_P5MM
GND	BGA	GND_P3MM
POWER	*	POWER_P6MM
POWER	BGA	POWER_P3MM
VR_CTL_PHY	*	POWER_P3MM
VR_CTL_PHY	BGA	STANDARD
VR_VID_PHY	*	POWER_50S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VR_DIDT_PHY	*	POWER_P6MM
VR_DIDT_PHY	BGA	STANDARD

Power-specific Spacing Definitions
Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_ISO	*	=STANDARD	?
GND_ISO	*	=STANDARD	?

Constraints
Power and Common

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	POWER_ISO
GND	*	*	GND_ISO

DC-DC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SWNODE_ISO	*	=8:1_SPACING	1000
SWNODE_SW2SW	*	=1:1_SPACING	?
SWNODE_SW2PWR	*	=2:1_SPACING	?
SWNODE_SW2GND	*	=2:1_SPACING	?

DC-DC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_SWITCH	*	*	SWNODE_ISO
VR_SWITCH	*	BGA	BGA_P1MM
VR_SWITCH	VR_SWITCH	*	SWNODE_SW2SW
VR_SWITCH	POWER	*	SWNODE_SW2PWR
VR_SWITCH	GND	*	SWNODE_SW2GND

DC-DC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_ISO	*	=3:1_SPACING	?
VR_VID_ISO	*	=4X_DIELECTRIC	?

DC-DC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_CTL	*	*	VR_CTL_ISO
VR_VID	*	*	VR_VID_ISO

PCH/GPU/TBT 1.05V S0

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
I1	POWER	POWER	5V			REG_VCC_U7400	64
I2	POWER	POWER	5V			REG_PVCC_U7400	64
Local Ground							
I3	GND	GND	0V			AGND_P1V05S0	64
1.05V S0							
I5	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0	64
I4	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0_L	64
I7	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P1V05S0	64
I6	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P1V05S0_RC	64
I8	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0	64
I9	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0_R	64
I10	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P1V05S0	64
I12	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P1V05S0	64
I11	VR_CTL_PHY	VR_CTL				REG_P1V05S0_OCSET	64
I14	VR_CTL_PHY	VR_CTL				REG_P1V05S0_VO	64
I16	VSNS_GPU_P1V05	SNS_DIFF_PHY	SENSE			SNS_GPU_PEX_IOVDD_P	64 79
I17	VSNS_GPU_P1V05	SNS_DIFF_PHY	SENSE			SNS_GPU_PEX_IOVDD_N	64 79
I19			SENSE			REG_P1V05S0_FB	64
I18			SENSE			REG_P1V05S0_RTN	64
I21	VR_CTL_PHY	VR_CTL				REG_P1V05S0_SREF	64
I20	VR_CTL_PHY	VR_CTL				REG_P1V05S0_FSEL	64
Output Bus							
I22	POWER	POWER	1.05V			PP1V05_S0	80
FET Switched							
I23	POWER	POWER	1.05V			PP1V05_TBTLC	28 80
I66	POWER	POWER	1.05V			PP1V05_TBTCIO	80

VDDQ S3 (1.5V)/VTT S0

Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus						
I43 POWER	POWER	5V			REG_V5IN_U7300	63
Local Ground						
I44 GND	GND	0V			AGND_VDDQS3	63
VDDQ S3						
I45 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3	63
I47 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3_L	63
I46 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_VDDQS3	63
I48 VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_VDDQS3_RC	63
I49 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQS3	63
I50 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQS3_R	63
I52 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_VDDQS3	63
I51 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_VDDQS3	63
I53 VR_CTL_PHY	VR_CTL				REG_VDDQS3_VDDQSNS	63
I55 VR_CTL_PHY	VR_CTL				REG_VDDQS3_VREF	63
I56 VR_CTL_PHY	VR_CTL				REG_VDDQS3_REFIN	63
I57 VR_CTL_PHY	VR_CTL				REG_VDDQS3_MODE	63
I58 VR_CTL_PHY	VR_CTL				REG_VDDQS3_TRIP	63
I59 VR_CTL_PHY	VR_CTL				LDO_DDRVTTS0_SNS	63
I61 VR_CTL_PHY	VR_CTL				REG_VDDQS3_VTTREF	63
Output Bus						
I60 POWER	POWER	1.5V			PPVDDQ_S3	80
I62 POWER_DDR	POWER_DDR	0.75V			PPDDRVTT_S0	80
FET Switched						
I63 POWER	POWER	1.5V			PP1V5_S0	80
Sensed						
I65 POWER	POWER	1.5V			PPVDDQ_S3_DDR	80
I67 POWER	POWER	1.5V			PP1V5_S0_PCH	80

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CPU VCC Phases

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
H12	POWER	POWER	12V			PP12V_S0_CPUVCC_FLT 61 62
H13	POWER	POWER	5V			REG_VCC_U7000 61
Local Ground						
H17	GND	GND	0V			AGND_CPU 61 62 81
Phase 1						
H18	VR_CTL_PHY	VR_CTL				REG_TD_1 62
H19	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_1 61 62
H20	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_1_R 61
H21	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUVCC_1 62
H22	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_1 62
H23	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUVCC_1_RC 62
H24	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUVCC_1 62
H25	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUVCC_1 62
H26	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUVCC_1 62
H27	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_1 62
H28 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_1_P 61 62
H29 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_1_N 62
H30		SENSE				REG_ISENVCC_1_NR 61 62
Phase 2						
H31	VR_CTL_PHY	VR_CTL				REG_TD_2 62
H32	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_2 61 62
H33	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_2_R 61
H34	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUVCC_2 62
H35	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_2 62
H36	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUVCC_2_RC 62
H37	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUVCC_2 62
H38	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUVCC_2 62
H39	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUVCC_2 62
H40	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_2 62
H41 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_2_P 61 62
H42 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_2_N 62
H43		SENSE				REG_ISENVCC_2_NR 61 62
Phase 3						
H44	VR_CTL_PHY	VR_CTL				REG_TD_3 62
H45	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_3 61 62
H46	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_3_R 61
H47	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUVCC_3 62
H48	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_3 62
H49	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUVCC_3_RC 62
H50	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUVCC_3 62
H51	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUVCC_3 62
H52	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUVCC_3 62
H53	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_3 62
H54 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_3_P 61 62
H55 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_3_N 62
H56		SENSE				REG_ISENVCC_3_NR 61 62

CPU VCC Controller

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
ISL6372						
H62	VR_CTL_PHY	VR_CTL				REG_CPUVCC_DVC 61
H63	VR_CTL_PHY	VR_CTL				CPUVCC_DVC_RC 61
H64	VR_CTL_PHY	VR_CTL				CPUVCC_FB_RC_2 61
H65	VR_CTL_PHY	VR_CTL				REG_CPUVCC_COMP 61
H66	VR_CTL_PHY	VR_CTL				CPUVCC_COMP_RC 61
H67	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FB 61
H68	VR_CTL_PHY	VR_CTL				CPUVCC_FB_RC 61
H69	VR_CTL_PHY	VR_CTL				CPUVCC_FB_R_1 61
H70	VR_CTL_PHY	VR_CTL				CPUVCC_FB_R_2 61
H71	VR_CTL_PHY	VR_CTL				CPUVCC_PSICOMP_RC 61
H72	VR_CTL_PHY	VR_CTL				REG_CPUVCC_PSICOMP 61
H73	VR_CTL_PHY	VR_CTL				REG_CPUVCC_HFCOMP 61
H74 VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				CPU_VCCSENSE_P 8 61
H75 VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				CPU_VCCSENSE_N 9 61
H76	SNS_DIFF_PHY	SENSE				CPU_VCCSENSE_R_P 61
H77	SNS_DIFF_PHY	SENSE				CPU_VCCSENSE_R_N 61
H78	SNS_DIFF_PHY	SENSE	1.8V			SNS_VCC_XW_P 61
H79	SNS_DIFF_PHY	SENSE	0V			SNS_VCC_XW_N 61
H80		SENSE				REG_CPUVCC_VSEN 61
H81		SENSE				REG_CPUVCC_RGND 61
H82		SENSE				REG_CPUVCC_VIN 61
H83	VR_CTL_PHY	VR_CTL				REG_CPUVCC_IMON 48 61
H84	VR_CTL_PHY	VR_CTL				CPUVCC_IMON_R 61
H85	VR_CTL_PHY	VR_CTL				REG_CPUVCC_TM 61
H86	VR_CTL_PHY	VR_CTL				REG_CPUVCC_IMX 61
H87	VR_CTL_PHY	VR_CTL				REG_CPUVCC_NPSI 61
H88	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FDVID 61
H89	VR_CTL_PHY	VR_CTL				REG_CPUVCC_TMX 61
H90	VR_CTL_PHY	VR_CTL				REG_CPUVCC_MEMVRSEL 61
H91	VR_CTL_PHY	VR_CTL				REG_CPUVCC_RSET 61
H92 CPU_VIDSCLK	VR_VID_PHY	VR_VID				CPU_VIDSCLK 8 61
H93	VR_VID_PHY	VR_VID				CPU_VIDSCLK_R 8
H94 CPU_VIDALERT_L	VR_VID_PHY	VR_VID				CPU_VIDALERT_L 8 61
H95	VR_VID_PHY	VR_VID				CPU_VIDALERT_R_L 8
H96 CPU_VIDSOUT	VR_VID_PHY	VR_VID				CPU_VIDSOUT 8 61
H97	VR_VID_PHY	VR_VID				CPU_VIDSOUT_R 8
Output Bus						
H98	POWER	POWER	1.8V			PPCPUVCC_S0_CPU 80

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GPU Core Phases and Controller

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
J12	POWER	POWER	12V			PPVIN_S0_GFXIMVP_R 67
J12	POWER	POWER	5V			PP5V_S0_GFXIMVP_VDD 67
Phase 1						
J12	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_1 67
J12	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_1 67
J12	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_1_RC 67
J12	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_1 67
J12	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_1 67
J12	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_ISEN_GPUCORE_1 67
J12	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_GPUCORE_1 67
Phase 2						
J13	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_2 67
J13	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_2 67
J13	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_2_RC 67
J13	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_2 67
J13	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_2 67
J13	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_ISEN_GPUCORE_2 67
J13	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_GPUCORE_2 67
ISL62882C						
J14	VR_CTL_PHY	VR_CTL				REG_GPUCORE_ISUMN 67
J12	VR_CTL_PHY	VR_CTL				REG_GPUCORE_ISUMN_R 67
J14	VR_CTL_PHY	VR_CTL				REG_GPUCORE_ISUMP 67
J14	VR_CTL_PHY	VR_CTL				REG_GPUCORE_ISUMP_C 67
J12	VR_CTL_PHY	VR_CTL				REG_GPUCORE_COMP 67
J12	VR_CTL_PHY	VR_CTL				REG_GPUCORE_COMP_R 67
J14	VR_CTL_PHY	VR_CTL				REG_GPUCORE_VW 67
J13	VR_CTL_PHY	VR_CTL				REG_GPUCORE_FB 67
J14	VR_CTL_PHY	VR_CTL				REG_GPUCORE_FB2 67
J13	VSNS_GPU_CORE	SNS_DIFF_PHY	SENSE			SNS_GPU_CORE_P 67 79
J13	VSNS_GPU_CORE	SNS_DIFF_PHY	SENSE			SNS_GPU_CORE_N 67 79
J14	ISNS_GPU_CORE_PH1	SNS_DIFF_PHY	SENSE			REG_GPUCORE_ISNS1_P 67
J14	ISNS_GPU_CORE_PH1	SNS_DIFF_PHY	SENSE			REG_GPUCORE_ISNS1_N 67
J14	ISNS_GPU_CORE_PH2	SNS_DIFF_PHY	SENSE			REG_GPUCORE_ISNS2_P 67
J14	ISNS_GPU_CORE_PH2	SNS_DIFF_PHY	SENSE			REG_GPUCORE_ISNS2_N 67
J14	GND	GND	0V			GND_REG_GPUCORE_AGND 67
Output Bus						
J12	POWER	POWER	1.0V			PPVCORE_S0_GPU 80
J14	POWER	POWER	1.0V			PPVCORE_S0_GFX_PH2 67
J14	POWER	POWER	1.0V			PPVCORE_S0_GFX_PH1 67

GPU VDDQ

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
J43	POWER	POWER	5V			REG_VCC_U7750 66
J43	POWER	POWER	5V			REG_PVCC_U7750 66
Local Ground						
J43	GND	GND	0V			AGND_GPUVDDQ 66
GPU VDDQ						
J43	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUVDDQ 66
J43	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUVDDQ 66
J43	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUVDDQ_RC 66
J43	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUVDDQ 66
J43	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUVDDQ 66
J43	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_GPUVDDQ 66
J43	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_OCSET 66
J43	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_VO 66
J43	VSNS_GPU_VDDQ	SNS_DIFF_PHY	SENSE			SNS_GPUVDDQ_P 66 74
J43	VSNS_GPU_VDDQ	SNS_DIFF_PHY	SENSE			SNS_GPUVDDQ_N 66 74
J43			SENSE			REG_GPUVDDQ_FB 66
J43			SENSE			REG_GPUVDDQ_RTN 66
J43	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_SREF 66
J43	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_FSEL 66
J43	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_SET0 66
J43	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_SET1 66
J43	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_SET1_R 66
Output Bus						
J43	POWER	POWER	1.5V			PPVDDQ_S0_GPU 80

3.3V S5/5V S4

Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus					
J44 POWER	POWER	12V			REG_VIN_U7600 65
J42 POWER	POWER	5V			REG_VCC1_U7600 65
J42 POWER	POWER	5V			REG_VCC2_U7600 65
3.3V S5					
J44 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P3V3S5 65
J44 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P3V3S5 65
J45 VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P3V3S5_RC 65
J44 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P3V3S5 65
J44 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P3V3S5 65
J52 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P3V3S5 65
J40 VR_CTL_PHY	VR_CTL				REG_P3V3S5_ISEN 65
J40 VR_CTL_PHY	VR_CTL				REG_P3V3S5_OCSET 65
J38 VR_CTL_PHY	VR_CTL				REG_P3V3S5_FSET 65
J40 VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT 65
J40 VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT_R 65
J40 VR_CTL_PHY	VR_CTL				REG_P3V3S5_FB 65
5V S3					
J43 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P5VS4 65
J43 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P5VS4 65
J43 VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P5VS4_RC 65
J44 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P5VS4 65
J44 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P5VS4 65
J44 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P5VS4 65
J43 VR_CTL_PHY	VR_CTL				REG_P5VS4_ISEN 65
J43 VR_CTL_PHY	VR_CTL				REG_P5VS4_OCSET 65
J43 VR_CTL_PHY	VR_CTL				REG_P5VS4_FSET 65
J43 VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT 65
J43 VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT_R 65
J43 VR_CTL_PHY	VR_CTL				REG_P5VS4_FB 65
Output Bus					
J43 POWER	POWER	5V			PP5V_S5 80
J43 POWER	POWER	5V			PP5V_S4 80
J43 POWER	POWER	3.3V			PP3V3_S5 80
FET Switched					
J42 POWER	POWER	5V			PP5V_S0 80
J42 POWER	POWER	3.3V			PP3V3_S4 80
J42 POWER	POWER	3.3V			PP3V3_S0 80
J43 POWER	POWER	3.3V			PP3V3_S0_SSD 80
J42 POWER	POWER	3.3V			PP3V3_ENET 80
J43 POWER	POWER	3.3V			PP3V3_TBTLC 80
Sensed					
J43 POWER	POWER	3.3V			PPSSD_S0 80
J43 POWER	POWER	3.3V			PP3V3_S4_AP

3.42V G3H

Physical	Spacing	Voltage	DIDT	NO_TEST	
3.42V G3H					
J44 POWER	VR_SWITCH	12V			P3V42G3H_BOOST 60
J44 POWER	VR_SWITCH	12V			P3V42G3H_SW 60
J44 VR_CTL_PHY	VR_CTL				P3V42G3H_FB 60
J44 VR_CTL_PHY	VR_CTL				P3V42G3H_SHDN_L 60
Output Bus					
J44 POWER	POWER	3.425V			PP3V42_G3H 80

3.3V G3

Physical	Spacing	Voltage	DIDT	NO_TEST	
J44 POWER	POWER	3.3V			PP3V3_G3 80

HDD S0

Physical	Spacing	Voltage	DIDT	NO_TEST	
FET Switched					
J39 POWER	POWER	5V			PPHDD_S0 80
Sensed					
J44 POWER	POWER	5V			PP5V_S0_HDD 80

12V

Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus					
J44 POWER	POWER	12V			PP12V_ACDC 80
FET Switched					
J44 POWER	POWER	12V			PP12V_S5 80
J42 POWER	POWER	12V			PP12V_S0 80
Sensed					
J45 POWER	POWER	12V			PP12V_G3H 80
J43 POWER	POWER	12V			PP12V_S0_GPUCORE 80
J43 POWER	POWER	12V			PP12V_S0_FBVDDQ 80

4V5_*

Physical	Spacing	Netname	
J14 POWER	POWER	4V5_REG_IN	52

Ground/Common

Physical	Spacing	Voltage	DIDT	NO_TEST	
Common					
J39 GND	GND	0V			GND

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Thunderbolt

Thunderbolt-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBTDP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Thunderbolt-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_I2C	*	=2x_DIELECTRIC	?
TBT_SPI	*	=2x_DIELECTRIC	?
TBTDP	*	=5x_DIELECTRIC	?
TBTDP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

DisplayPort

DP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

DP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3:1_SPACING	?

Pairs should be within 100 mils of clock length.
Max length of DisplayPort traces: 12 inches

DisplayPort intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DisplayPort AUX channel intra-pair matching should be 5 ps. No relationship to other signals.

TBT IC Net Properties

Electrical Contraint Set		Physical	Spacing		
		DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	26 77
		DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	26 77
	DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	26
	DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	26
		DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	26 77
		DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	26 77
	DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	26
	DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	26
		DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	26 77
		DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	26 77
	DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	26
	DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	26
		DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	26 77
		DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	26 77
	DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	26
	DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	26
	DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_P<3..0>	41
	DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_N<3..0>	41
	DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	41
	DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	41
	DP_INTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_P	41
	DP_INTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_N	41
		DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_P	41
		DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_N	41
		TBT_I2C_55S	TBT_I2C	I2C_TBTRTR_SCL	26
		TBT_I2C_55S	TBT_I2C	I2C_TBTRTR_SDA	26
	TBT_SPI_CLK	TBT_SPI_55S	TBT_SPI	TBT_SPI_CLK	26
	TBT_SPI_MOSI	TBT_SPI_55S	TBT_SPI	TBT_SPI_MOSI	26
	TBT_SPI_MISO	TBT_SPI_55S	TBT_SPI	TBT_SPI_MISO	26
	TBT_SPI_CS_L	TBT_SPI_55S	TBT_SPI	TBT_SPI_CS_L	26

*: Only used on hosts supporting T29 video-in

DisplayPort

Electrical Contraint Set		Physical	Spacing		
Graphics Source					
	DP_INTPNL_EG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_ML_P<1..0>	41 77
	DP_INTPNL_EG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_ML_N<1..0>	41 77
	DP_INTPNL_EG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_P	41 77
	DP_INTPNL_EG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_N	41 77
		DP_85D	DISPLAYPORT	DP_INT_EG_AUX_C_P	41
		DP_85D	DISPLAYPORT	DP_INT_EG_AUX_C_N	41
Internal Panel					
		DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_P<3..0>	41
		DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_N<3..0>	41
	DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_P<3..0>	40 41
	DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_N<3..0>	40 41
	DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_P	40 41
	DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_N	40 41
Internal DP SPDIF					
			HDA	DP_INT_SPDIF_AUDIO	40 52

TBT/DP Net Properties

Electrical Contraint Set		Physical	Spacing		
Port A					
	TBT_A_R2D1	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<1>	26 29
	TBT_A_R2D1	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<1>	26 29
	TBT_A_R2D0	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<0>	26 29
	TBT_A_R2D0	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<0>	26 29
		TBTDP_90D	TBTDP	TBT_A_R2D_P<1..0>	29
		TBTDP_90D	TBTDP	TBT_A_R2D_N<1..0>	29
	DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>	26 29
	DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>	26 29
	DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>	26 29
	DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>	26 29
		DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>	29
		DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>	29
		DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>	29
		DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>	29
	DP_A_LSX	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	29
	DP_A_LSX	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	29
		TBTDP_90D	TBTDP	TBT_A_D2R_C_P<1..0>	29
		TBTDP_90D	TBTDP	TBT_A_D2R_C_N<1..0>	29
	TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_P<1>	26 29
	TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_N<1>	26 29
	TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_P<0>	26 29
	TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_N<0>	26 29
	TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P	26 29
	TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N	26 29
		DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P	29
		DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N	29
	DP_A_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_P	29
	DP_A_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_N	29
		TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_P	29
		TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_N	29
Port B					
	TBT_B_R2D1	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<1>	26 30
	TBT_B_R2D1	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<1>	26 30
	TBT_B_R2D0	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<0>	26 30
	TBT_B_R2D0	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<0>	26 30
		TBTDP_90D	TBTDP	TBT_B_R2D_P<1..0>	30
		TBTDP_90D	TBTDP	TBT_B_R2D_N<1..0>	30
	DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	26 30
	DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	26 30
	DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	26 30
	DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	26 30
		DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>	30
		DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	30
		DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	30
		DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	30
	DP_B_LSX	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	30
	DP_B_LSX	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	30
		TBTDP_90D	TBTDP	TBT_B_D2R_C_P<1..0>	30
		TBTDP_90D	TBTDP	TBT_B_D2R_C_N<1..0>	30
	TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_P<1>	26 30
	TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_N<1>	26 30
	TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_P<0>	26 30
	TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_N<0>	26 30
	TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P	26 30
	TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N	26 30
		DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P	30
		DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N	30
	DP_B_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_P	30
	DP_B_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_N	30
		TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_P	30
		TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_N	30

JTAG_*

Physical	Spacing	Netname	
XDP_PHY	XDP	JTAG_TBT_TDI	20 26
XDP_PHY	XDP	JTAG_TBT_TDO	20 26
XDP_PHY	XDP	JTAG_TBT_TMS	20 26

DP_*

Physical	Spacing	Netname	
TBT_I2C_55S	TBT_I2C	DP_TBTPA_DDC_CLK	29 31
TBT_I2C_55S	TBT_I2C	DP_TBTPA_DDC_DATA	29 31
TBT_I2C_55S	TBT_I2C	DP_TBTPB_DDC_CLK	30 31
TBT_I2C_55S	TBT_I2C	DP_TBTPB_DDC_DATA	30 31

TBT_*

Physical	Spacing	Voltage	Netname	
TBT_I2C_55S	TBT_I2C		TBT_A_CONFIG1_RC	29
TBT_I2C_55S	TBT_I2C		TBT_B_CONFIG1_RC	30

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GDDR5

GDDR5-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12 MM	=STANDARD	=STANDARD
GDDR_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GDDR_MA_PHY	*	GDDR_45S
GDDR_ADBI_PHY	*	GDDR_45S
GDDR_CTRL_PHY	*	GDDR_45S
GDDR_CLK_PHY	*	GDDR_80D
GDDR_DQ_PHY	*	GDDR_45S
GDDR_EDC_PHY	*	GDDR_45S
GDDR_DBI_PHY	*	GDDR_45S
GDDR_WCK_PHY	*	GDDR_80D

Main Segment Min Spacing Rules for 4.5 Gbps or Less (AMD Doc# 49919)

	Trace-to-Trace				Isolation				
Table	Micro	Design	Strip	Design	Micro	Design	Strip	Design	Comments
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Memory address (MA). Implented 4.5 Gbps or less rules for K70.
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Address dynamic bus inversion (ADBI)
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Control (CTRL)
5-6/5-7	5:1	5:1	5:1	5:1	5:1	5:1	5:1	5:1	Clock (CLK)
5-6/5-7	3:1	3:1	3:1	3:1	5:1	5:1	5:1	5:1	Data (DQ)
5-6/5-7	7:1	7:1	7:1	7:1	7:1	7:1	7:1	7:1	Error detection pins (EDC). Using larger isolation rules,
5-6/5-7	3:1	3:1	3:1	3:1	5:1	5:1	5:1	5:1	Data dynamic bus inversion (DBI)
5-6/5-7	5:1	5:1	5:1	5:1	5:1	5:1	5:1	5:1	Forwarded clock (WCK)

GDDR5-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR_ISO	*	=5x_DIELECTRIC	?
GDDR_ISO	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR_MA2MA	*	=2x_DIELECTRIC	?
GDDR_MA2MA	TOP,BOTTOM	=2x_DIELECTRIC	?
GDDR_ADBI2ADBI	*	=2x_DIELECTRIC	?
GDDR_ADBI2ADBI	TOP,BOTTOM	=2x_DIELECTRIC	?
GDDR_CTRL2CTRL	*	=2x_DIELECTRIC	?
GDDR_CTRL2CTRL	TOP,BOTTOM	=2x_DIELECTRIC	?
GDDR_CLK2CLK	*	=5x_DIELECTRIC	?
GDDR_CLK2CLK	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR_DQ2DQ	*	=3x_DIELECTRIC	?
GDDR_DQ2DQ	TOP,BOTTOM	=3x_DIELECTRIC	?
GDDR_EDC_ISO	*	=7x_DIELECTRIC	?
GDDR_EDC_ISO	TOP,BOTTOM	=7x_DIELECTRIC	?
GDDR_EDC2EDC	*	=7x_DIELECTRIC	?
GDDR_EDC2EDC	TOP,BOTTOM	=7x_DIELECTRIC	?
GDDR_DBI2DBI	*	=3x_DIELECTRIC	?
GDDR_DBI2DBI	TOP,BOTTOM	=3x_DIELECTRIC	?
GDDR_WCK2WCK	*	=5x_DIELECTRIC	?
GDDR_WCK2WCK	TOP,BOTTOM	=5x_DIELECTRIC	?

Constraints (x in {A, B}, y in {0, 1})

Memory Address: MAxy[8:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_MA	*	*	GDDR_ISO
GDDR_*_*_MA	=SAME	*	GDDR_MA2MA

Data: DQxy[31:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_DQ	*	*	GDDR_ISO
GDDR_*_*_DQ	=SAME	*	GDDR_DQ2DQ

Address Dynamic Bus Inversion: ADBIxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_ADBI	*	*	GDDR_ISO
GDDR_*_*_ADBI	=SAME	*	GDDR_ADBI2ADBI

Error Detection: EDCxy[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_EDC	*	*	GDDR_EDC_ISO
GDDR_*_*_EDC	=SAME	*	GDDR_EDC2EDC

Control: Reset, CKExy, CSxy, WExy, RASxy, CASxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_CTRL	*	*	GDDR_ISO
GDDR_*_*_CTRL	*	*	GDDR_ISO
GDDR_*_*_CTRL	=SAME	*	GDDR_CTRL2CTRL

Data Dynamic Bus Inversion: DDBIxy[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_DBI	*	*	GDDR_ISO
GDDR_*_*_DBI	=SAME	*	GDDR_DBI2DBI

Clock: CKxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_CLK	*	*	GDDR_ISO
GDDR_*_*_CLK	=SAME	*	GDDR_CLK2CLK

Forwarded Clock: WCKxy[1:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_WCK	*	*	GDDR_ISO
GDDR_*_*_WCK	=SAME	*	GDDR_WCK2WCK

GPU

GPU-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_GPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

GPU-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_GPU_ISO	*	=4:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_GPU	*	*	CLK_GPU_ISO

GDDR5 Frame Buffer A

Electrical Contraint Set	Physical	Spacing		
Memory Address				
J64 GDDR_A0_MA	GDDR_MA_PHY	GDDR_A_0_MA	FB_A0_A<8..0>	74 75
J64 GDDR_A1_MA	GDDR_MA_PHY	GDDR_A_1_MA	FB_A1_A<8..0>	74 75
Address Dynamic Bus Inv				
J64 GDDR_A0_ADBI	GDDR_ADBI_PHY	GDDR_A_0_ADBI	FB_A0_ABI_L	74 75
J63 GDDR_A1_ADBI	GDDR_ADBI_PHY	GDDR_A_1_ADBI	FB_A1_ABI_L	74 75
Control				
J63 GDDR_A0_CKE	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CKE_L	74 75
J63 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CS_L	74 75
J64 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_WE_L	74 75
J65 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CAS_L	74 75
J65 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_RAS_L	74 75
J65 GDDR_A1_CKE	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CKE_L	74 75
J65 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CS_L	74 75
J65 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_WE_L	74 75
J65 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CAS_L	74 75
J65 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_RAS_L	74 75
Clock				
J65 GDDR_A0_CLK	GDDR_CLK_PHY	GDDR_A_0_CLK	FB_A0_CLK_P	74 75
J65 GDDR_A0_CLK	GDDR_CLK_PHY	GDDR_A_0_CLK	FB_A0_CLK_N	74 75
J66 GDDR_A1_CLK	GDDR_CLK_PHY	GDDR_A_1_CLK	FB_A1_CLK_P	74 75
J65 GDDR_A1_CLK	GDDR_CLK_PHY	GDDR_A_1_CLK	FB_A1_CLK_N	74 75
Data				
J66 GDDR_A0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<7..0>	74 75
J66 GDDR_A0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<15..8>	74 75
J66 GDDR_A0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<23..16>	74 75
J66 GDDR_A0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<31..24>	74 75
J66 GDDR_A1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<7..0>	74 75
J66 GDDR_A1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<15..8>	74 75
J66 GDDR_A1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<23..16>	74 75
J66 GDDR_A1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<31..24>	74 75
Error Detection				
J67 GDDR_A0_EDC0	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<0>	74 75
J66 GDDR_A0_EDC1	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<1>	74 75
J67 GDDR_A0_EDC2	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<2>	74 75
J67 GDDR_A0_EDC3	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<3>	74 75
J67 GDDR_A1_EDC0	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<0>	74 75
J67 GDDR_A1_EDC1	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<1>	74 75
J67 GDDR_A1_EDC2	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<2>	74 75
J67 GDDR_A1_EDC3	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<3>	74 75
Data Dynamic Bus Inv				
J67 GDDR_A0_DBI0	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<0>	74 75
J67 GDDR_A0_DBI1	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<1>	74 75
J68 GDDR_A0_DBI2	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<2>	74 75
J67 GDDR_A0_DBI3	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<3>	74 75
J68 GDDR_A1_DBI0	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<0>	74 75
J68 GDDR_A1_DBI1	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<1>	74 75
J68 GDDR_A1_DBI2	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<2>	74 75
J68 GDDR_A1_DBI3	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<3>	74 75
Forwarded Clock				
J68 GDDR_A0_WCK0	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_P<0>	74 75
J68 GDDR_A0_WCK0	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_N<0>	74 75
J68 GDDR_A0_WCK1	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_P<1>	74 75
J68 GDDR_A0_WCK1	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_N<1>	74 75
J69 GDDR_A1_WCK0	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_P<0>	74 75
J69 GDDR_A1_WCK0	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_N<0>	74 75
J69 GDDR_A1_WCK1	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_P<1>	74 75
J69 GDDR_A1_WCK1	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_N<1>	74 75

GDDR5 Frame Buffer B

Electrical Contraint Set	Physical	Spacing		
Memory Address				
J69 GDDR_B0_MA	GDDR_MA_PHY	GDDR_B_0_MA	FB_B0_A<8..0>	74 76
J69 GDDR_B1_MA	GDDR_MA_PHY	GDDR_B_1_MA	FB_B1_A<8..0>	74 76
Address Dynamic Bus Inv				
J69 GDDR_B0_ADBI	GDDR_ADBI_PHY	GDDR_B_0_ADBI	FB_B0_ABI_L	74 76
J69 GDDR_B1_ADBI	GDDR_ADBI_PHY	GDDR_B_1_ADBI	FB_B1_ABI_L	74 76
Control				
J69 GDDR_B0_CKE	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CKE_L	74 76
J70 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CS_L	74 76
J70 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_WE_L	74 76
J70 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CAS_L	74 76
J70 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_RAS_L	74 76
J70 GDDR_B1_CKE	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CKE_L	74 76
J70 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CS_L	74 76
J70 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_WE_L	74 76
J70 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CAS_L	74 76
J70 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_RAS_L	74 76
Clock				
J69 GDDR_B0_CLK	GDDR_CLK_PHY	GDDR_B_0_CLK	FB_B0_CLK_P	74 76
J71 GDDR_B0_CLK	GDDR_CLK_PHY	GDDR_B_0_CLK	FB_B0_CLK_N	74 76
J70 GDDR_B1_CLK	GDDR_CLK_PHY	GDDR_B_1_CLK	FB_B1_CLK_P	74 76
J71 GDDR_B1_CLK	GDDR_CLK_PHY	GDDR_B_1_CLK	FB_B1_CLK_N	74 76
Data				
J71 GDDR_B0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<7..0>	74 76
J72 GDDR_B0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<15..8>	74 76
J72 GDDR_B0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<23..16>	74 76
J73 GDDR_B0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<31..24>	74 76
J71 GDDR_B1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<7..0>	74 76
J71 GDDR_B1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<15..8>	74 76
J71 GDDR_B1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<23..16>	74 76
J71 GDDR_B1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<31..24>	74 76
Error Detection				
J72 GDDR_B0_EDC0	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<0>	74 76
J72 GDDR_B0_EDC1	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<1>	74 76
J72 GDDR_B0_EDC2	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<2>	74 76
J72 GDDR_B0_EDC3	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<3>	74 76
J72 GDDR_B1_EDC0	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<0>	74 76
J72 GDDR_B1_EDC1	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<1>	74 76
J72 GDDR_B1_EDC2	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<2>	74 76
J72 GDDR_B1_EDC3	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<3>	74 76
Data Dynamic Bus Inv				
J72 GDDR_B0_DBI0	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<0>	74 76
J73 GDDR_B0_DBI1	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<1>	74 76
J73 GDDR_B0_DBI2	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<2>	74 76
J73 GDDR_B0_DBI3	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<3>	74 76
J73 GDDR_B1_DBI0	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<0>	74 76
J73 GDDR_B1_DBI1	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<1>	74 76
J73 GDDR_B1_DBI2	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<2>	74 76
J73 GDDR_B1_DBI3	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<3>	74 76
Forwarded Clock				
J73 GDDR_B0_WCK0	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_P<0>	74 76
J73 GDDR_B0_WCK0	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_N<0>	74 76
J73 GDDR_B0_WCK1	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_P<1>	74 76
J73 GDDR_B0_WCK1	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_N<1>	74 76
J74 GDDR_B1_WCK0	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_P<0>	74 76
J74 GDDR_B1_WCK0	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_N<0>	74 76
J74 GDDR_B1_WCK1	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_P<1>	74 76
J74 GDDR_B1_WCK1	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_N<1>	74 76

GPU

Electrical Contraint Set	Physical	Spacing		
Clocks				
J75	CLK_GPU_55S	CLK_GPU	PEX_TSTCLK_O_PL	72
J75	CLK_GPU_55S	CLK_GPU	PEX_TSTCLK_O_NG	72
J75	CLK_PCIE_PHY	CLK_PCIE	GPU_PEX_TERMP	72
J76	CLK_GPU_55S	CLK_GPU	GPU_JTAG_TCK	77 78
J76	CLK_GPU_55S	CLK_GPU	GPU_ROM_SCLK	77 78
J76 SPI_50S	SPI		GPU_ROM_SI	77 78
J76 SPI_50S	SPI		GPU_ROM_SO	77 78
J77	CLK_GPU_55S	CLK_GPU	GPU_OSC_27M_XTAL_IN	
J77	CLK_GPU_55S	CLK_GPU	GPU_OSC_27M_XTAL_OUT	
J78 XDP_PHY	XDP		GPU_JTAG_TDI	77 78
J78 XDP_PHY	XDP		GPU_JTAG_TDO	77 78
J78 XDP_PHY	XDP		GPU_JTAG_TMS	77 78
J78 XDP_PHY	XDP		GPU_JTAG_TRST_L	77 78
SMB				
J77	SMB_PHY	SMB	GPU_SMB_CLK	77 78
J77	SMB_PHY	SMB	GPU_SMB_DAT	77 78
J77	SMB_PHY	SMB	GPU_SMB_CLK_R	47 78
J77	SMB_PHY	SMB	GPU_SMB_DAT_R	47 78
PCIe Compensation				
J79	PCIE_50S	COMP_PCIE	FB_CAL_PD_VDDQ	74
J79	PCIE_50S	COMP_PCIE	FB_CAL_PU_GND	74
J79	PCIE_50S	COMP_PCIE	FB_CAL_TERM_GND	74

Frame Buffer Reset

Electrical Contraint Set	Physical	Spacing		
Reset				
J74 GDDR_A0_RESET	GDDR_50S	GDDR_CTRL	FB_A0_RESET_L	74 75
J74 GDDR_A1_RESET	GDDR_50S	GDDR_CTRL	FB_A1_RESET_L	74 75
J74 GDDR_B0_RESET	GDDR_50S	GDDR_CTRL	FB_B0_RESET_L	74 76
J74 GDDR_B1_RESET	GDDR_50S	GDDR_CTRL	FB_B1_RESET_L	74 76

SYNC_MASTER=J16_NICK SYNC_DATE=05/30/2013

PAGE TITLE: GDDR5/GPU Constraints

Apple Inc.

DRAWING NUMBER: 051-9889 SIZE: D

REVISION: 13.0.0

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Backlight Controller

BLC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BLC_P6MM	*	Y	0.600 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD
BLC_P3MM	*	Y	0.300 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_BLC	*	BLC_P6MM
POWER_BLC_RET	*	BLC_P3MM
BLC_CTL_PHY	*	BLC_P3MM

BLC-specific Spacing Definitions
BLC High Voltage Output

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_HV_ISO	*	0.45mm	1000

Constraints
BLC High Voltage Output

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_HV	BLC_CTL	*	BLC_CTL_ISO
BLC_HV	BLC_HV	*	BLC_CTL_ISO
BLC_HV	*	*	BLC_HV_ISO

BLC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PHASE_ISO	*	=8:1_SPACING	2000
PHASE_SW2SW	*	=1:1_SPACING	?
PHASE_SW2PWR	*	=2:1_SPACING	?
PHASE_SW2GND	*	=2:1_SPACING	?

BLC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_PHASE	*	*	PHASE_ISO
BLC_PHASE	BLC_PHASE	*	PHASE_SW2SW
BLC_PHASE	POWER	*	PHASE_SW2PWR
BLC_PHASE	GND	*	PHASE_SW2GND

BLC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_CTL_ISO	*	=3:1_SPACING	?

BLC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_CTL	*	*	BLC_CTL_ISO

Is it chel'oh or sel'oh?

	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
J30	POWER	POWER	12V			PP12V_BKLT_SNS 48
J24	POWER	POWER	12V			PP12V_BKLT_FUSED 48
J25	POWER	POWER	12V			PP12V_S0_BKLT_FILT 48
J22	POWER	POWER	12V			PP12V_S0_BKLT_PWR 48
J24	POWER	POWER	12V			PP12V_S0_BKLT_PWR_R 48
J25	POWER	POWER	5V			PP5V_S0_BKLT_R 48
J27	POWER	POWER	3.3V			PP3V3_S0_BKLT_VDDIO_R 48
Local Ground						
J23	BLC_CTL_PHY	BLC_PHASE	0V			PGND_BKLT 48
J27	BLC_CTL_PHY	BLC_PHASE	0V			DGND_BKLT 48
J30	BLC_CTL_PHY	BLC_PHASE	0V			LGND_BKLT 48
Backlight						
J52	POWER_BLC	BLC_PHASE	80V	TRUE		BKLT_PHASE 48
J55	BLC_CTL_PHY	BLC_PHASE	80V	TRUE		BKLT_GATE 48
J54	BLC_CTL_PHY	BLC_PHASE	80V	TRUE		BKLT_GATE_R 48
J35	BLC_CTL_PHY	BLC_PHASE	80V	TRUE		BKLT_SNUBBER 48
J35	BLC_CTL_PHY	BLC_PHASE	12V	TRUE		BKLT_SW_R 48
J35	BLC_CTL_PHY	BLC_CTL				BKLT_ISET 48
J26	BLC_CTL_PHY	BLC_CTL				BKLT_PLT 48
J26	BLC_CTL_PHY	BLC_CTL				BKLT_PLT_RC 48
J29	SNS_DIFF_PHY	SENSE				BKLT_SW_P 48
J28	SNS_DIFF_PHY	SENSE				BKLT_SW_N 48
J62		SENSE				BKLT_FB 48
J30		BLC_HV	67V			BKLT_FB_XW 48
J26		BLC_HV	67V			BKLT_FB_R 48
J27	POWER_BLC_RET	BLC_CTL				BKLT_ISEN1 48
J27	POWER_BLC_RET	BLC_CTL				BKLT_ISEN2 48
J27	POWER_BLC_RET	BLC_CTL				BKLT_ISEN3 48
J27	POWER_BLC_RET	BLC_CTL				BKLT_ISEN4 48
J28	POWER_BLC_RET	BLC_CTL				BKLT_ISEN5 48
J27	POWER_BLC_RET	BLC_CTL				BKLT_ISEN6 48
J28	POWER_BLC_RET	BLC_HV				BKLT_ISEN1_R 48
J28	POWER_BLC_RET	BLC_HV				BKLT_ISEN2_R 48
J27	POWER_BLC_RET	BLC_HV				BKLT_ISEN3_R 48
J29	POWER_BLC_RET	BLC_HV				BKLT_ISEN4_R 48
J27	POWER_BLC_RET	BLC_HV				BKLT_ISEN5_R 48
J27	POWER_BLC_RET	BLC_HV				BKLT_ISEN6_R 48
J28	POWER_BLC_RET	BLC_HV				LED_RETURN_1 48
J28	POWER_BLC_RET	BLC_HV				LED_RETURN_2 48
J28	POWER_BLC_RET	BLC_HV				LED_RETURN_3 48
J28	POWER_BLC_RET	BLC_HV				LED_RETURN_4 48
J28	POWER_BLC_RET	BLC_HV				LED_RETURN_5 48
J28	POWER_BLC_RET	BLC_HV				LED_RETURN_6 48
Output Bus						
J29	POWER_BLC	BLC_HV	67V			BKLT_BOOST 48
J23	POWER_BLC	BLC_HV	67V			BKLT_BOOST_1 48
J24	POWER_BLC	BLC_HV	67V			BKLT_BOOST_2 48

Cello Miscellaneous

Electrical Contraint Set	Physical	Spacing	
SPI			
J54	SMB_PHY	SMB	BKLT_SCL 48
J56	SMB_PHY	SMB	BKLT_SDA 48

SYNC_MASTER=J16_DG SYNC_DATE=04/21/2013

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