AMD AM4

MICRO-STAR INT'L CO.,LTD		
MS-7C92		
Size: Custom	Document Description: Cover Sheet	Rev: 12
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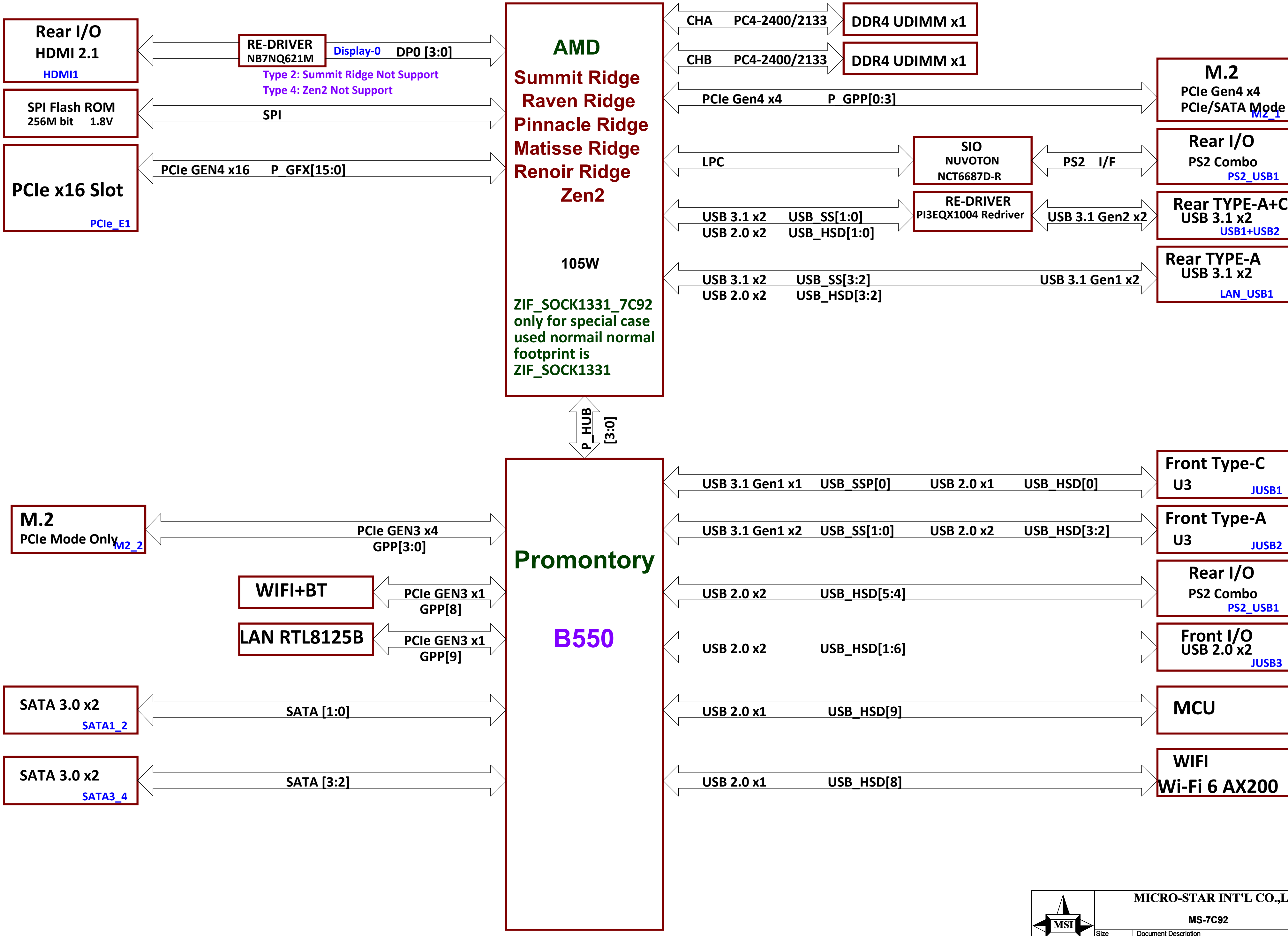

MICRO-STAR INT'L CO.,LTD			
MS-7C92			
Size: Custom	Document Description: Block Diagram		Rev: 12
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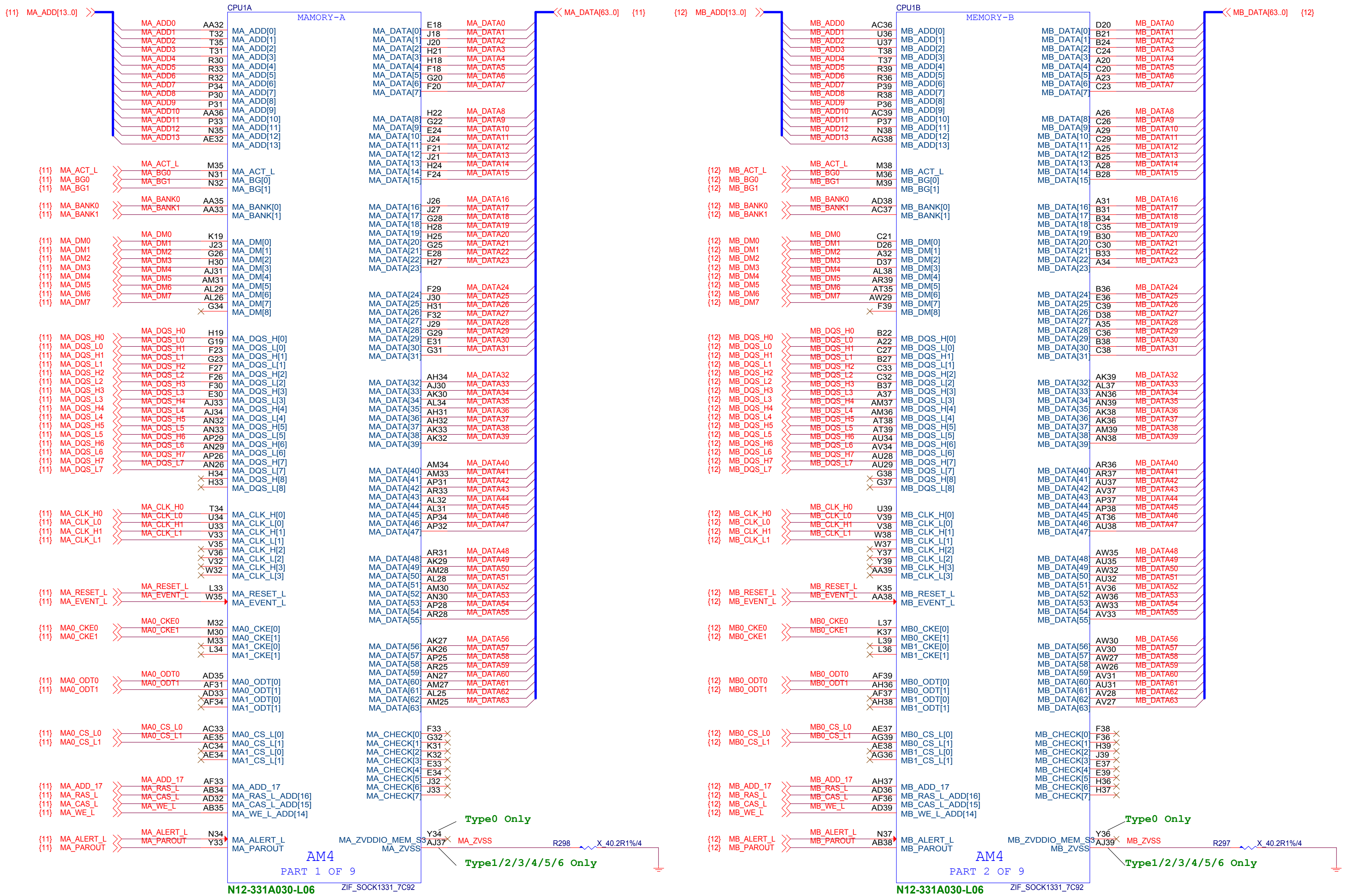

ZIF_SOCK1331_7C92 only for special case used
normal footprint is ZIF_SOCK1331

ZIF_SOCK1331_7C92 only for special case used
normal footprint is ZIF_SOCK1331

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C92	
Size: Custom	Document Description: AM4 DDR4 I/F	Rev: 12
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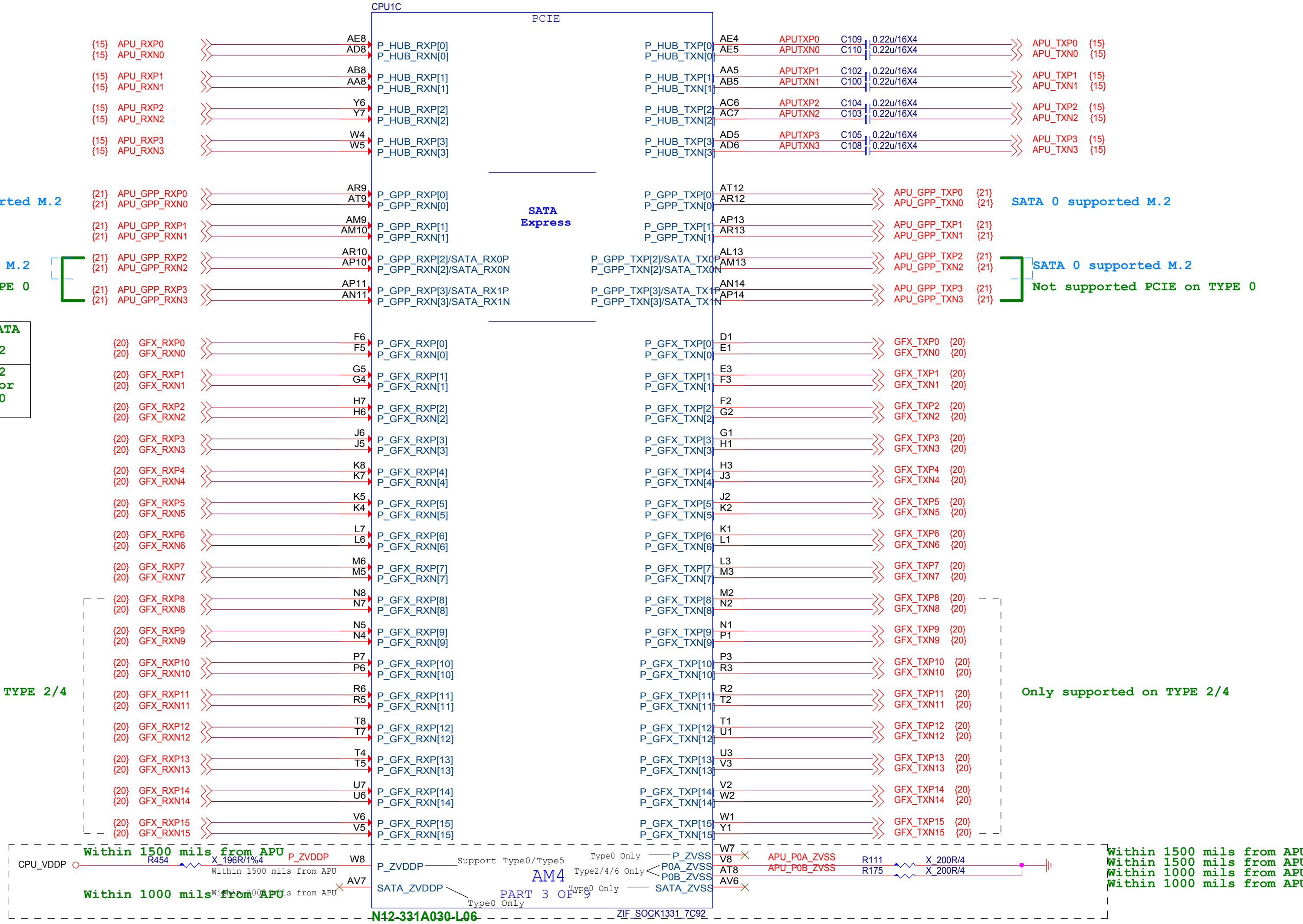

	PCIE	SATA
TYPE 0/1	2	2
TYPE 2/3/4	2 or 4	2 or 0

ZIF_SOCK1331_7C92 only for special case used
normal footprint is ZIF_SOCK1331

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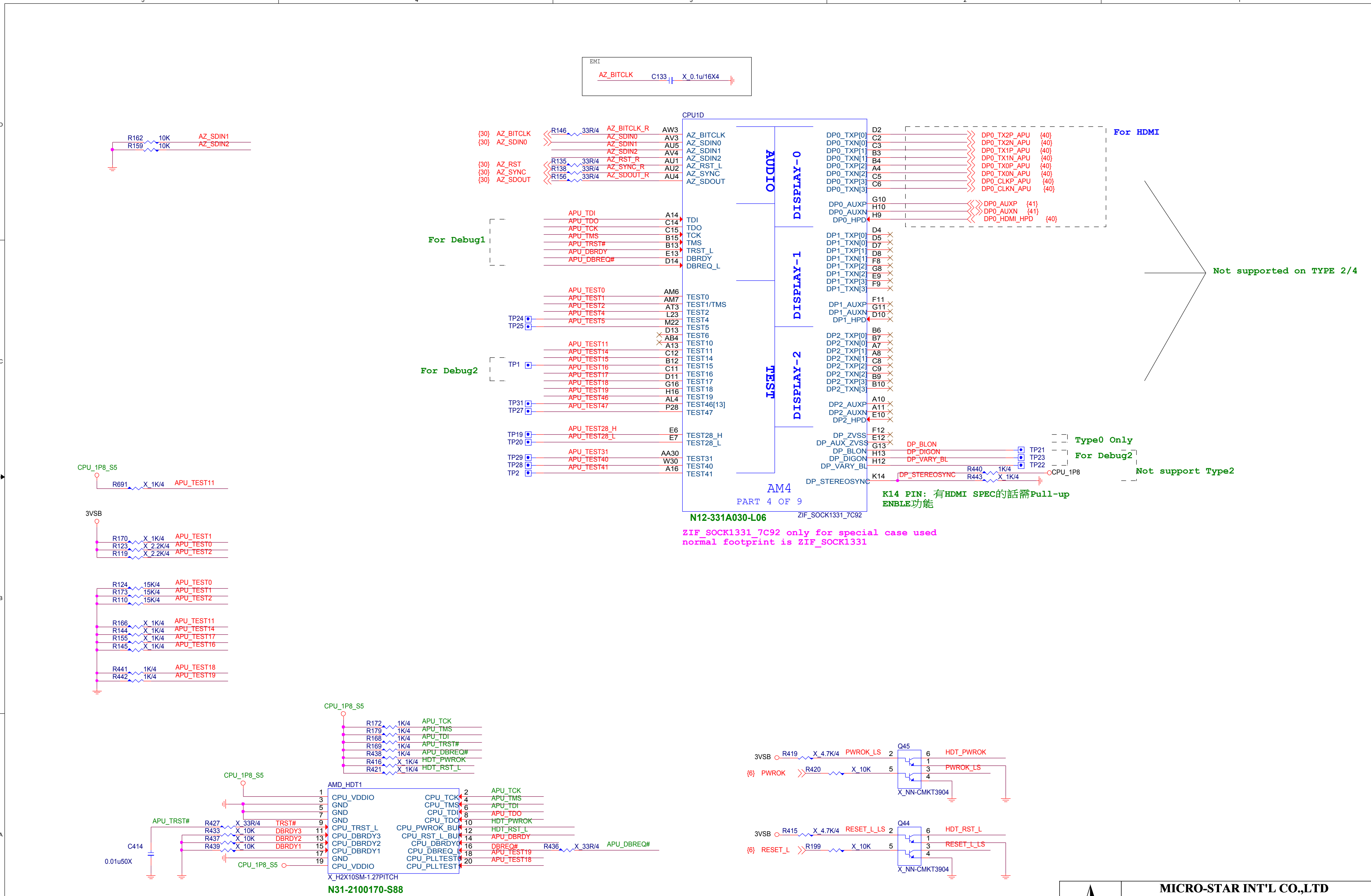

MICRO-STAR INT'L CO.,LTD

MS-7C92

Size	Document Description	Rev
Custom	AM4 Display / Audio	12

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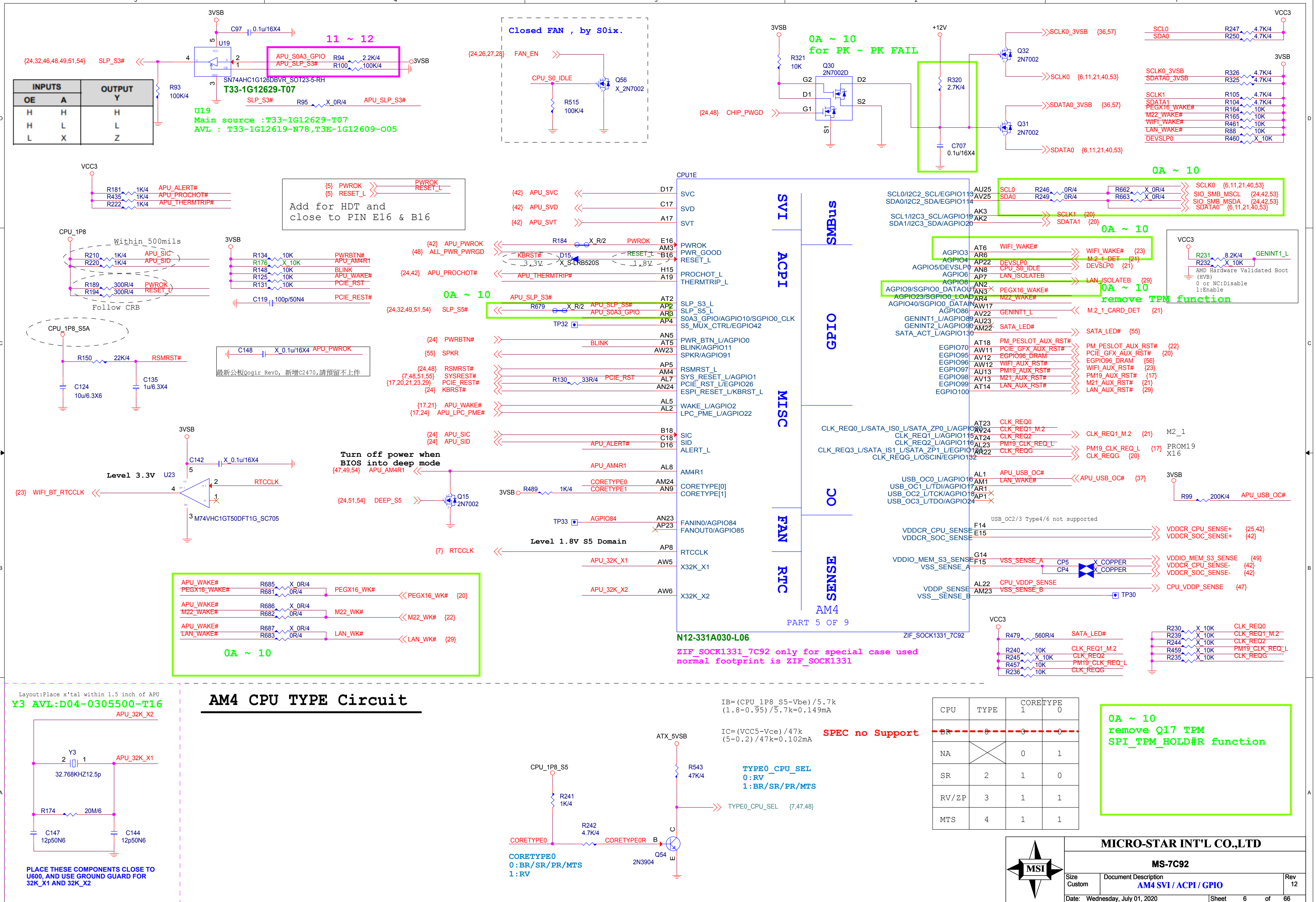

AM4 CPU TYPE Circuit

INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

CPU	TYPE	CORETYPE 1	CORETYPE 0
~~BR~~	~~0~~	~~0~~	~~0~~
NA		0	1
SR	2	1	0
RV/ZP	3	1	1
MTS	4	1	1

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Size: Custom | Document Description: AM4 SVI / ACPI / GPIO | Rev: 12

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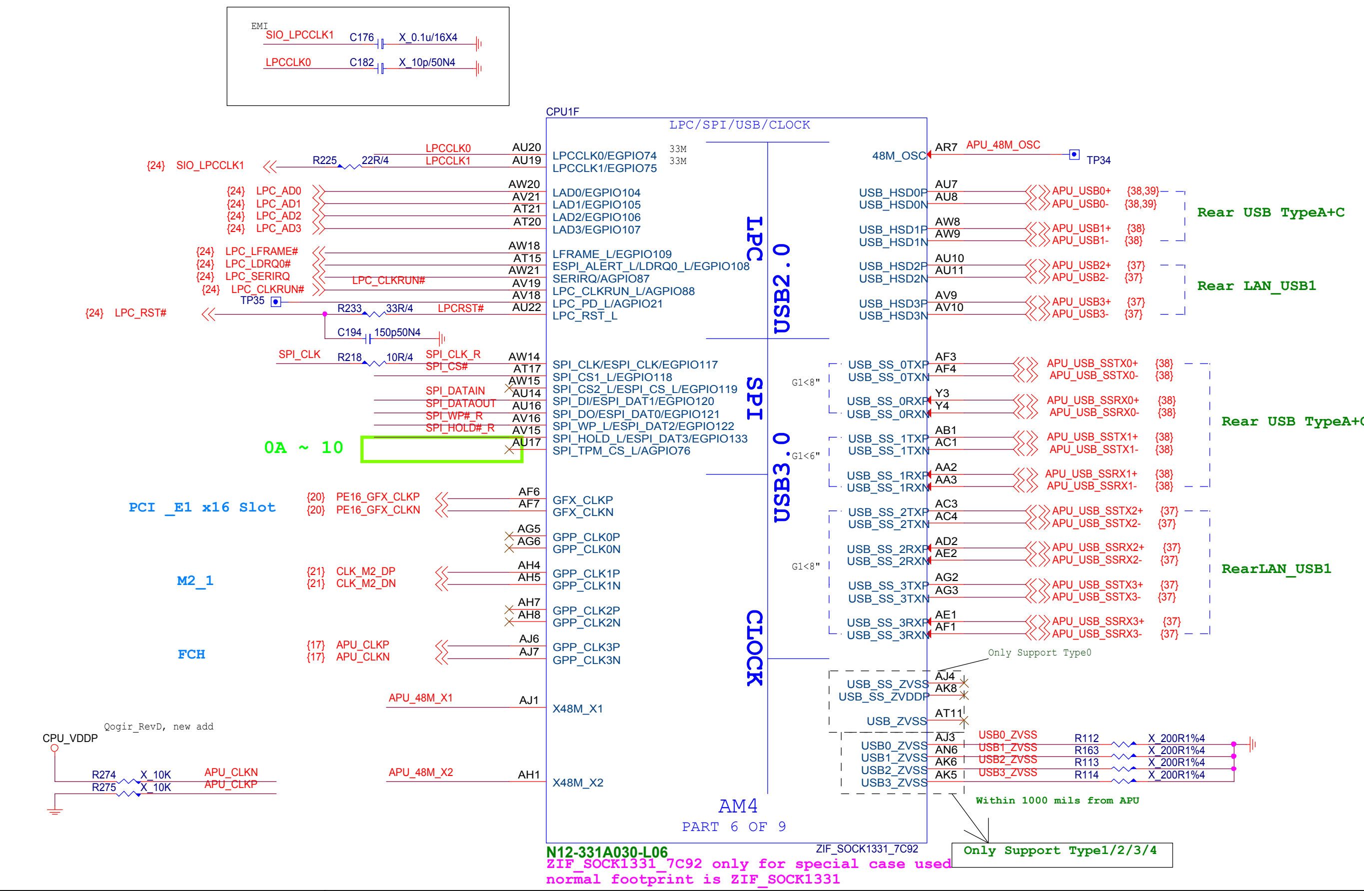
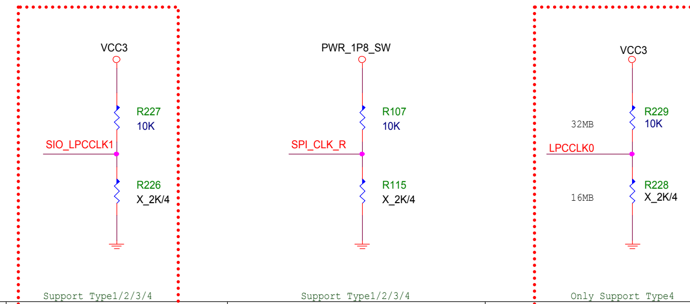
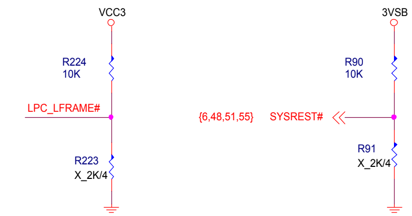


Strapping Options

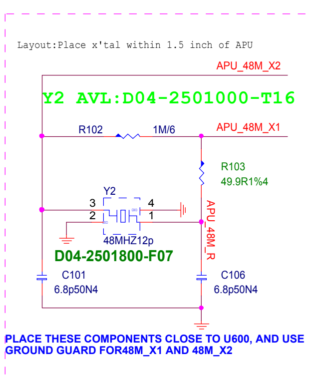


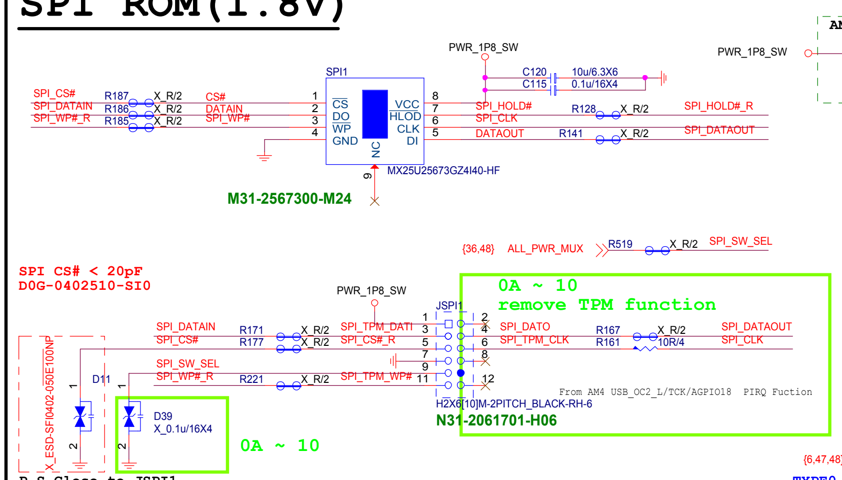
	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator **(Default)**	Use 48Mhz crystal clock and generate both internal and external clocks **(Default)**	PSP should modify SPI page register bits [25:24] to remap physical ROM to upper image **(Default)**
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	PSP should not modify SPI page register bits [25:24]

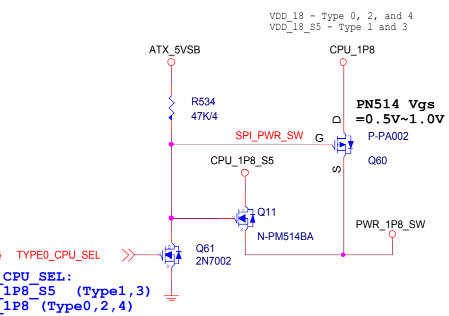


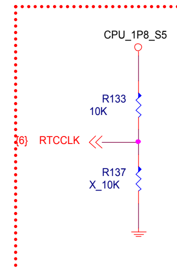
	AGPIO3	LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic **(Default)**	SPI ROM **(Default)**	Normal reset mode **(Default)**
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode

SPI ROM(1.8V)

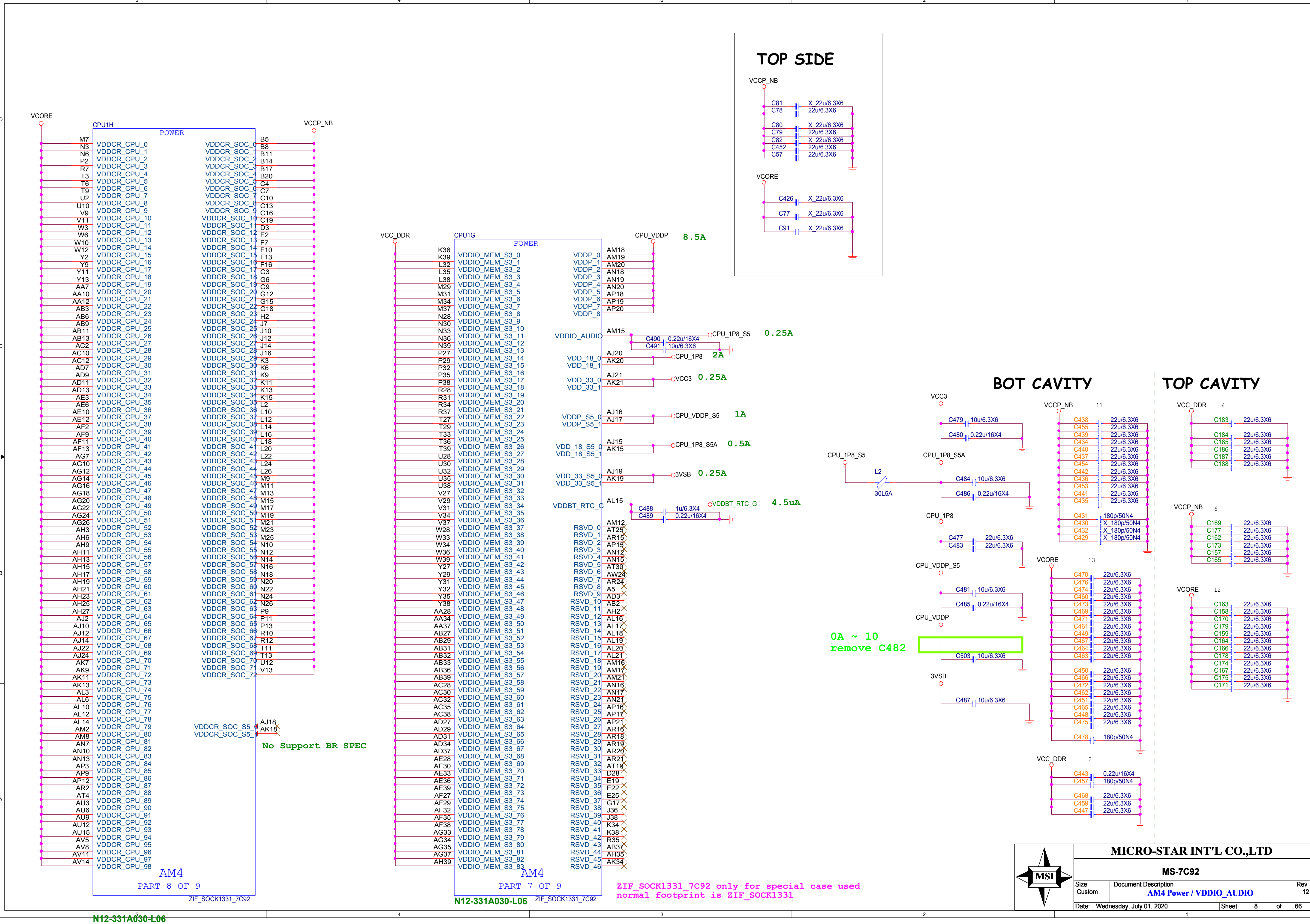








	RTCCLK
PULL HIGH	RTCCLK is input and is used as the bypass clock **(Default)**
PULL LOW	Normal Mode: Use 32Khz xtal as the source of RTC clock



MICRO-STAR INT'L CO.,LTD

MS-7C92

Size	Document Description	Rev
Custom	AM4 Power / VDDIO_AUDIO	12

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ZIF_SOCK1331_7C92 only for special case used
normal footprint is ZIF_SOCK1331

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	AM4 GND	12

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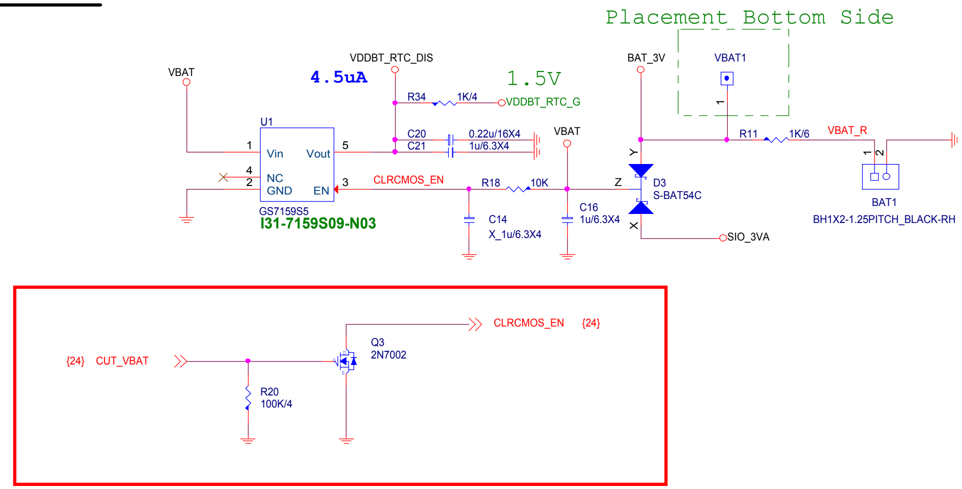
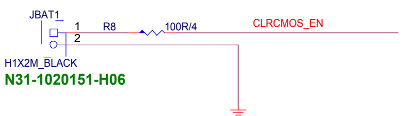
RTC & Clear CMOS Circuit



Clear CMOS button



MICRO-STAR INT'L CO.,LTD		
MS-7C92		
Size: Custom	Document Description: RTC / CMOS	Rev: 12
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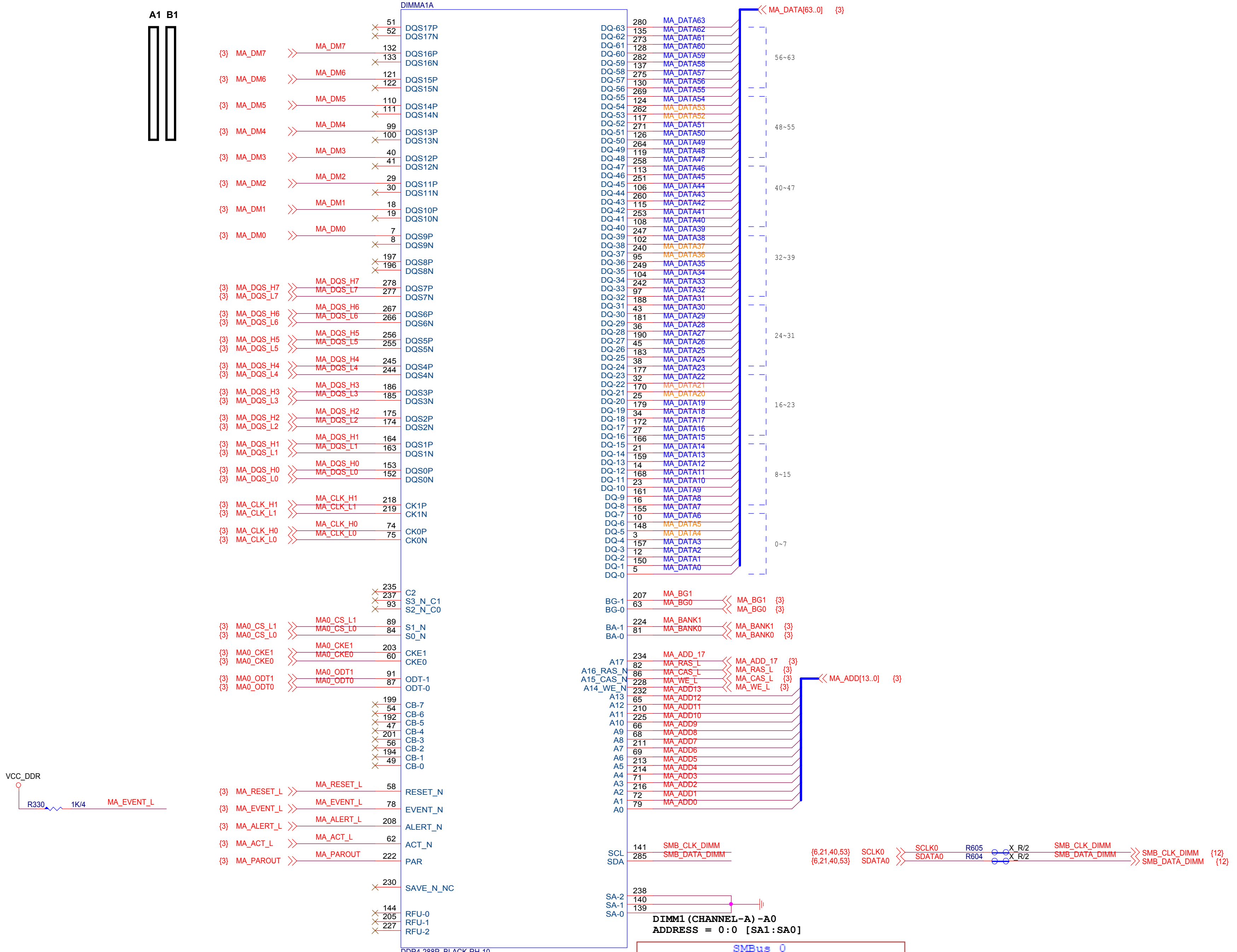

AVL: N13-2880441-F02

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
[redacted]	
DIMMB0	A2
[redacted]	

MSI	MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: DDR4 - DIMM CH-A	Rev: 12
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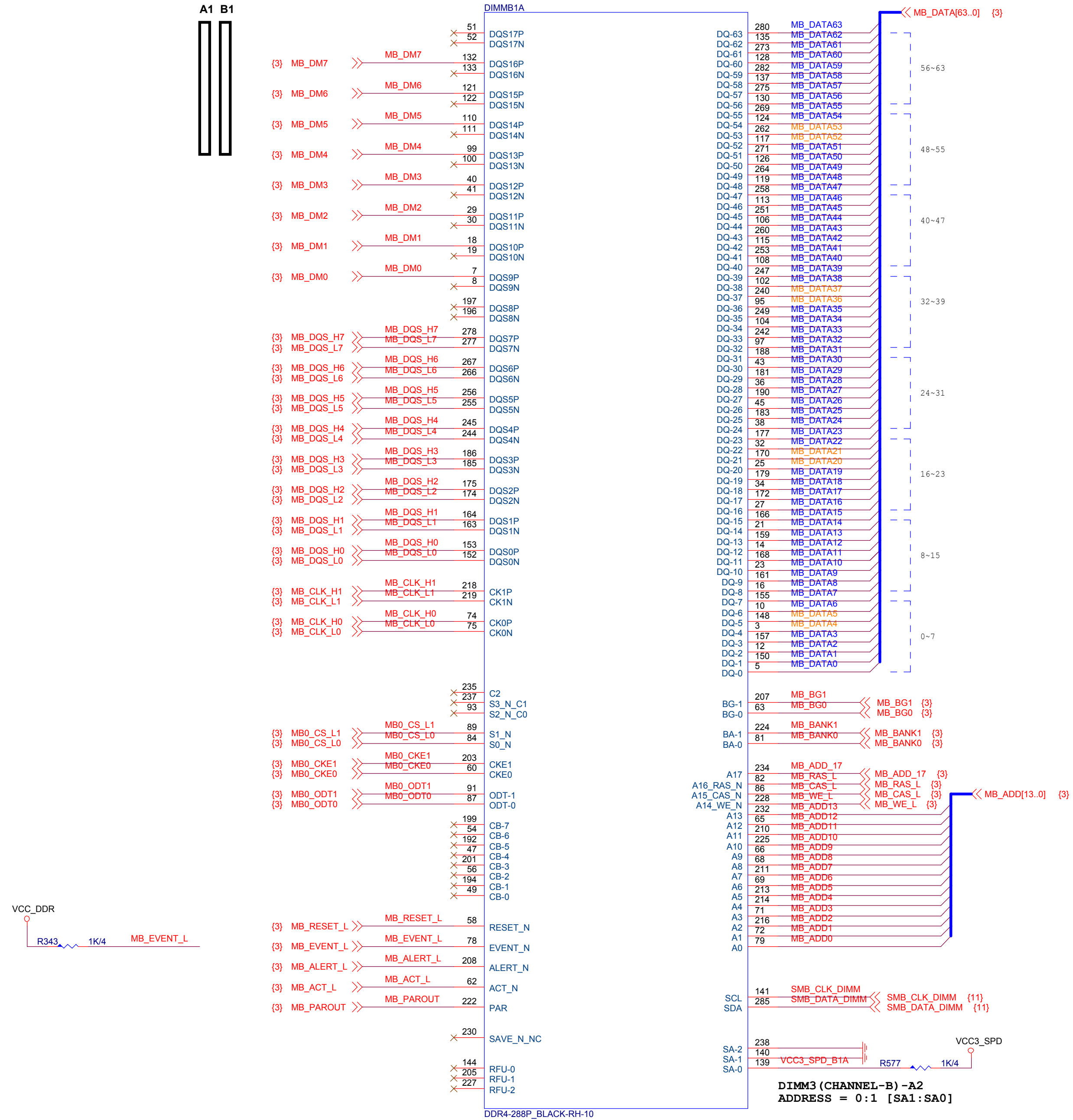

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MS-7C92

Size	Document Description	Rev
Custom	DDR4 - DIMM CH-B	12

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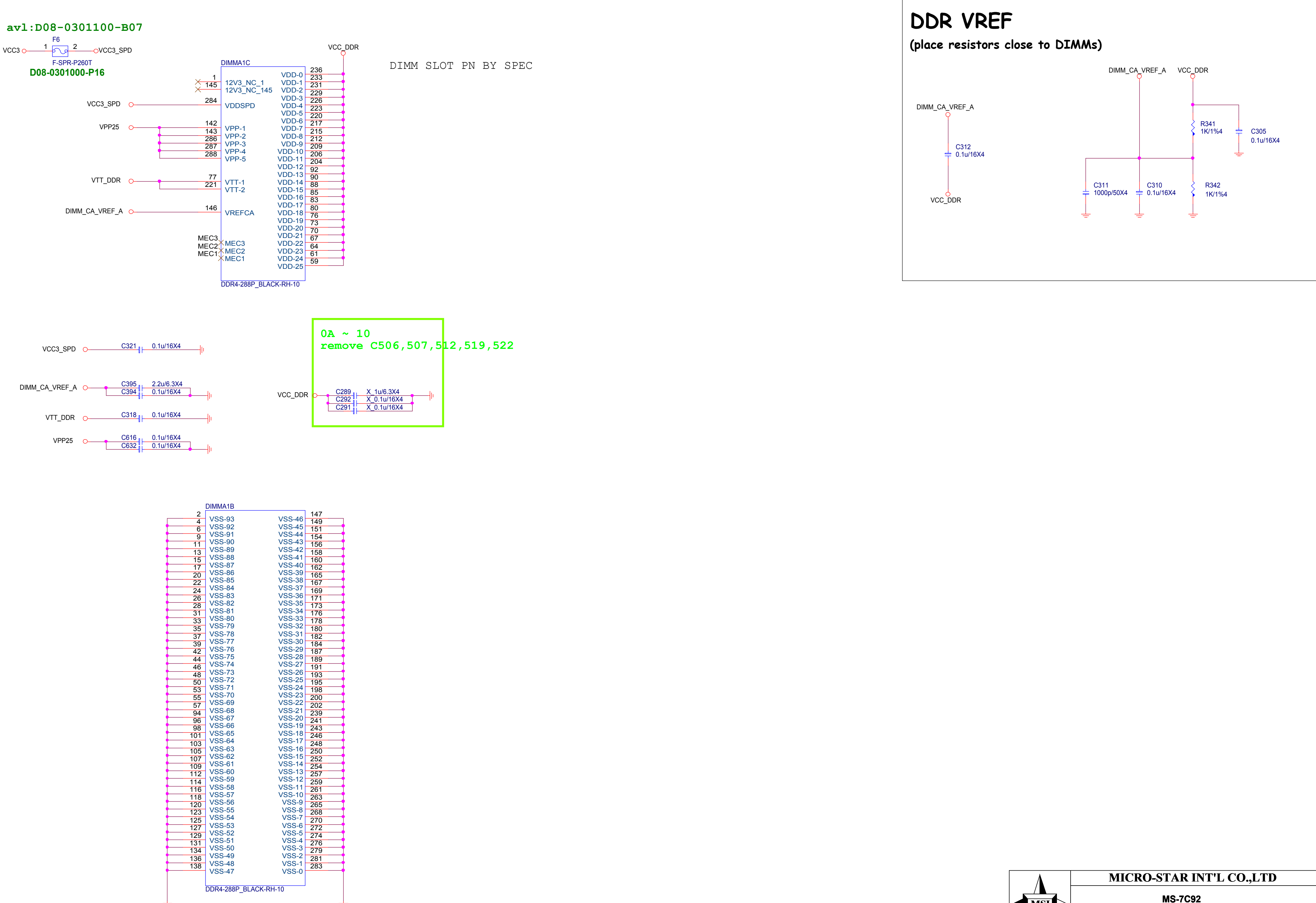

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Size	Document Description	Rev
Custom	DDR4 - POWER/GND-1	12

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DDR VREF

(place resistors close to DIMMs)

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MS-7C92	
Size: Custom	Document Description: DDR4 - POWER/GND-2	Rev: 12
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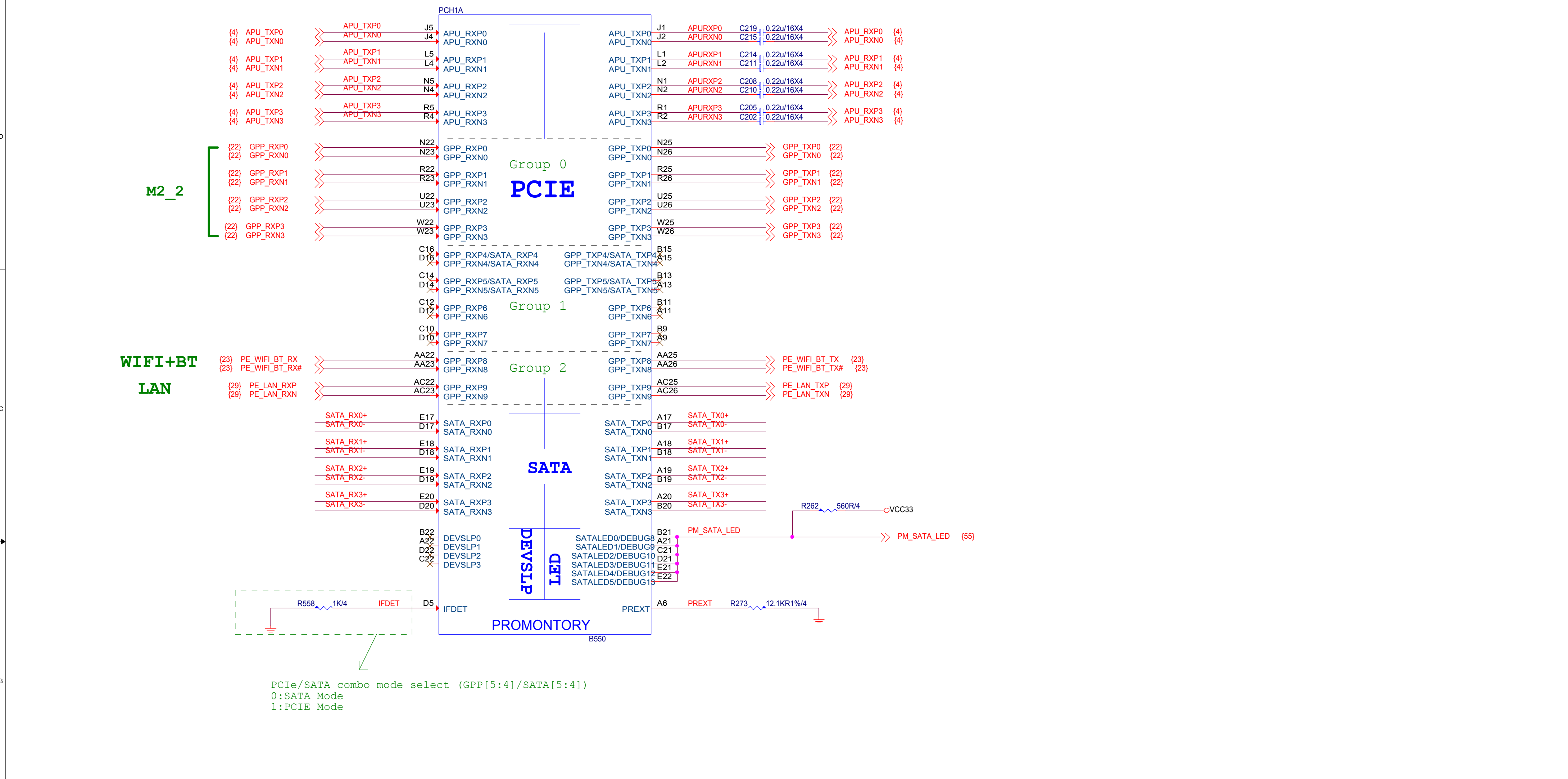
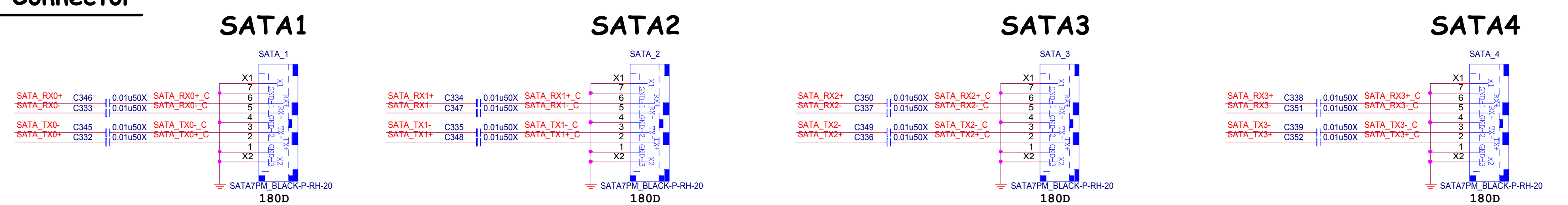


SATA Connector



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	Premium - PCIE/SATA	12

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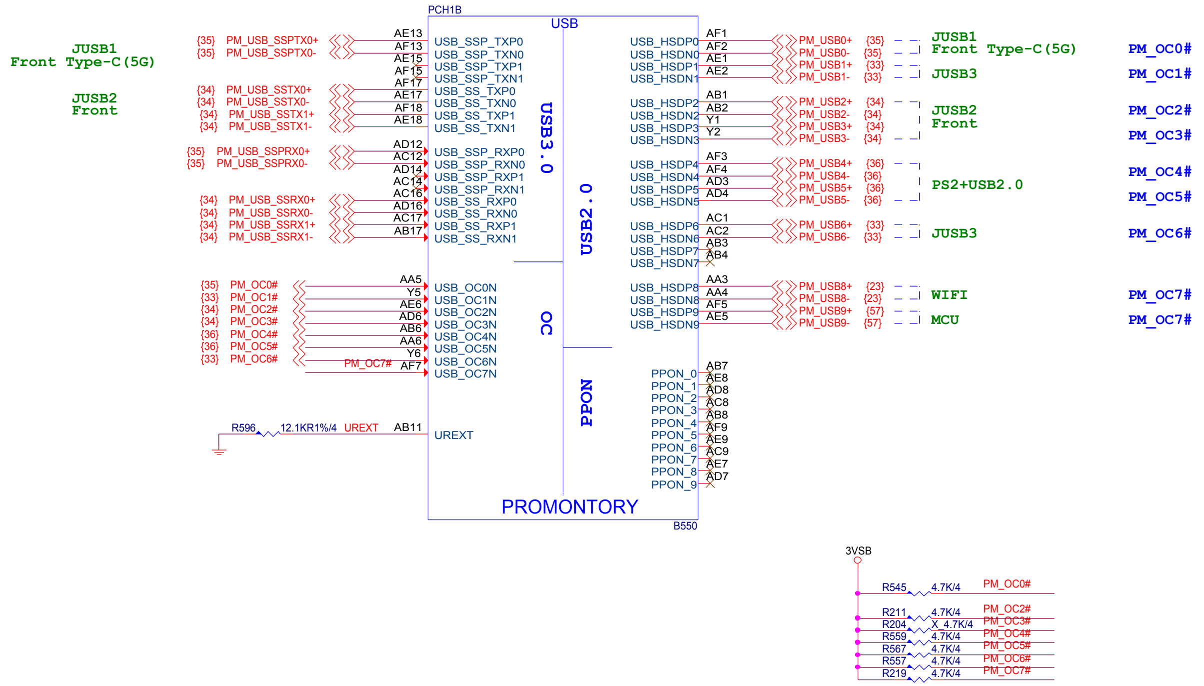

USB mapping

USB_SSP_TX/RX[0] + USB_HSDP/N[0] + USB_OC0N

USB_SSP_TX/RX[1] + USB_HSDP/N[1] + USB_OC1N

USB_SS_TX/RX[0] + USB_HSDP/N[2] + USB_OC2N

USB_SS_TX/RX[1] + USB_HSDP/N[3] + USB_OC3N

USB_HSDP/N[4] + USB_OC4N

USB_HSDP/N[5] + USB_OC5N

USB_HSDP/N[6] + USB_OC6N

USB_HSDP/N[7] + USB_OC7N

USB_HSDP/N[8] + USB_OC7N

USB_HSDP/N[9] + USB_OC7N

MICRO-STAR INT'L CO.,LTD

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Custom	Premium - USB/OC	12

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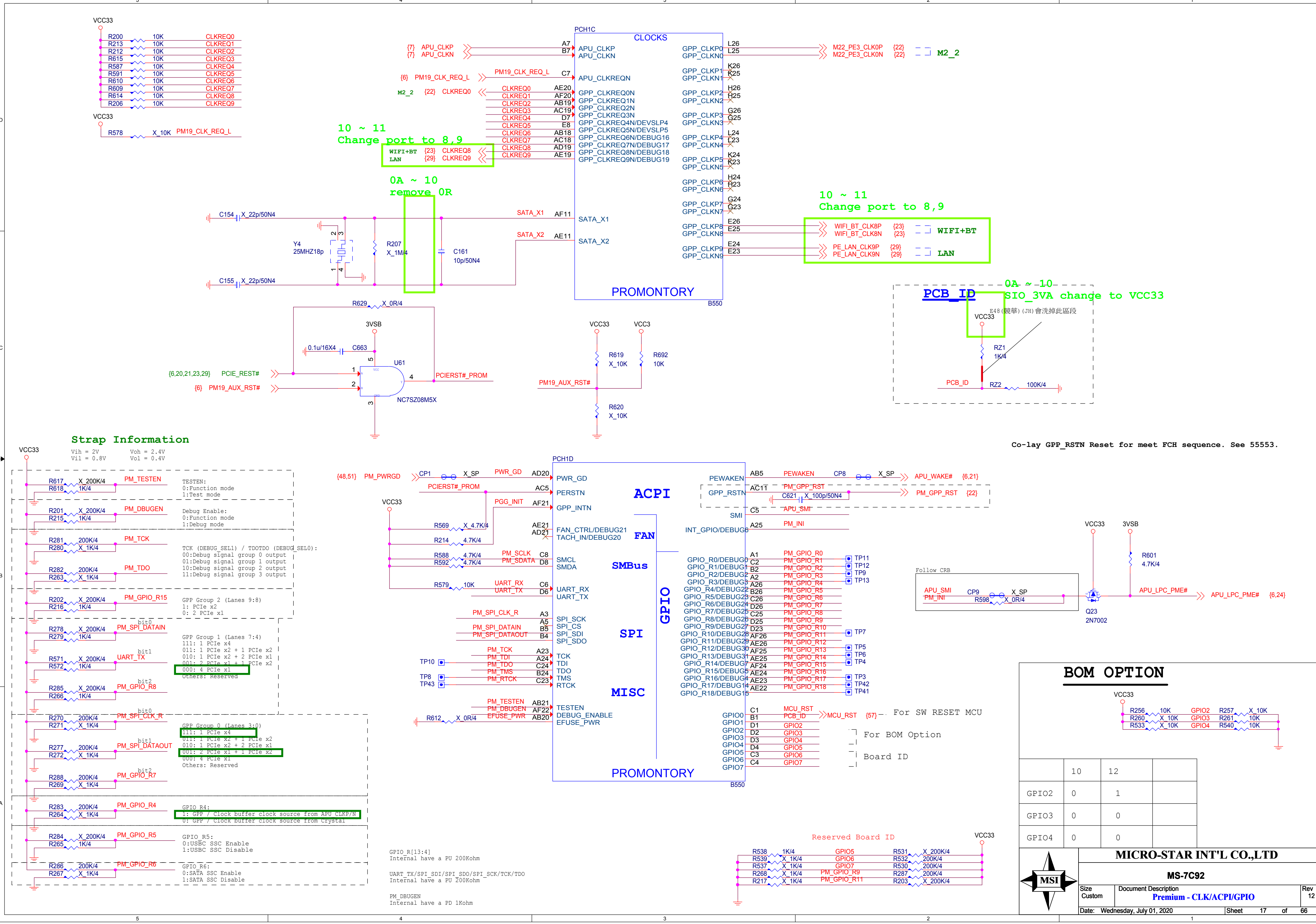

BOM OPTION

	10	12
GPIO2	0	1
GPIO3	0	0
GPIO4	0	0

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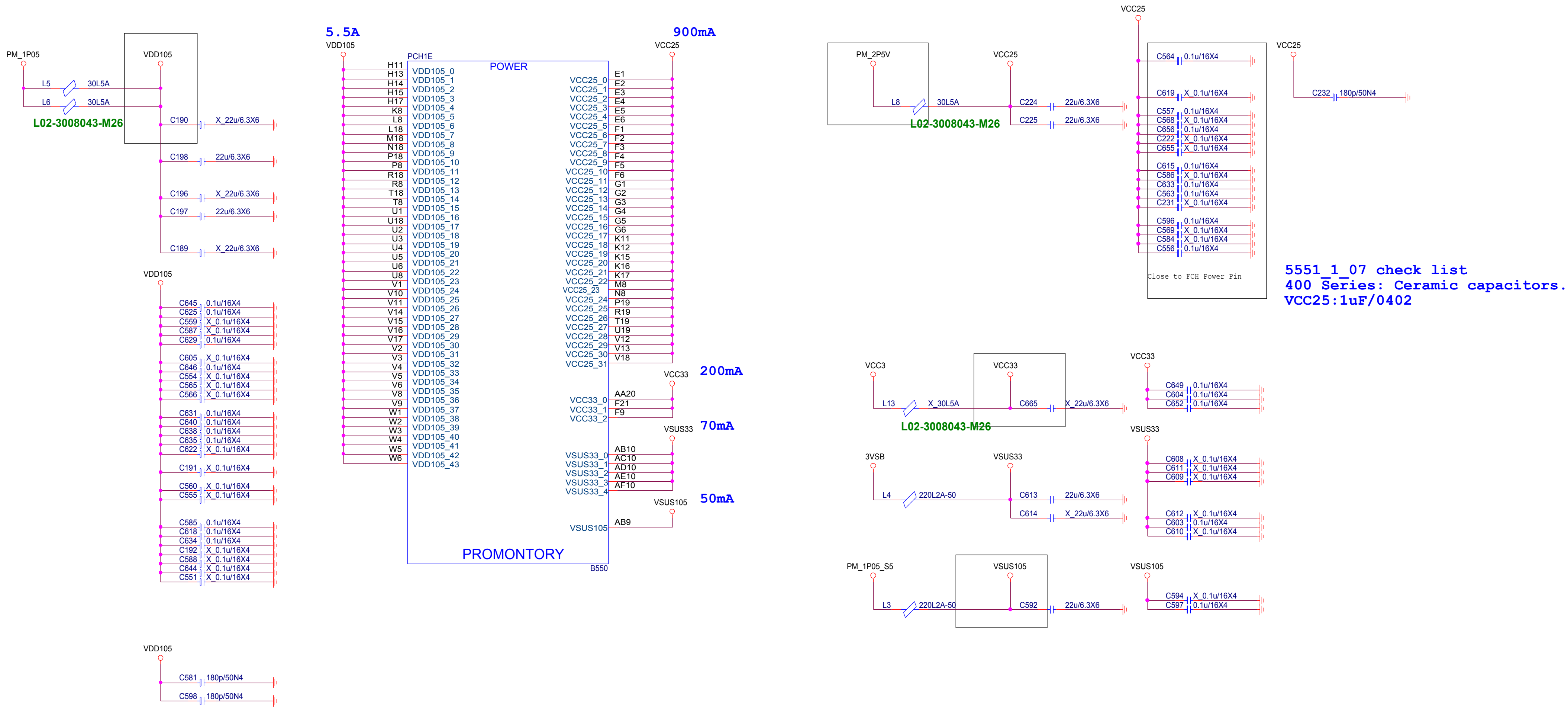

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Size: Custom	Document Description: Premium - Power	Rev: 12
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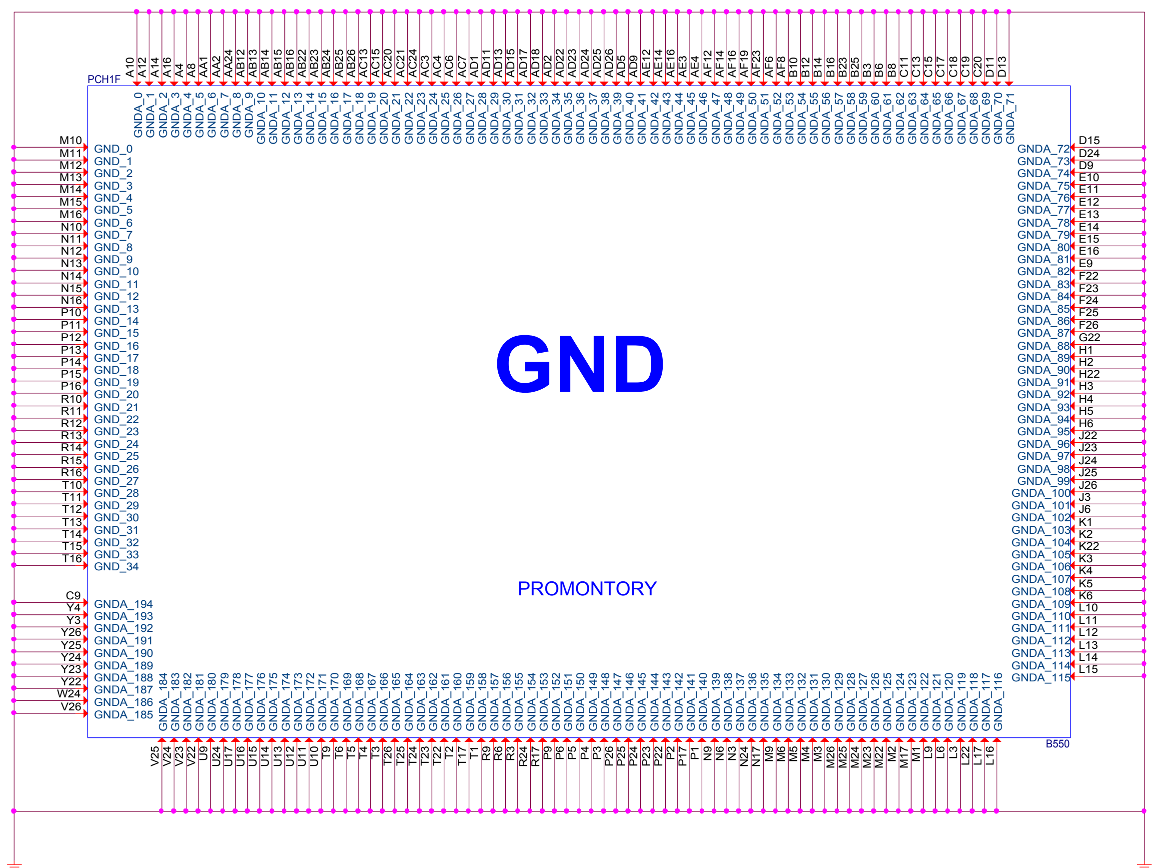

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MS-7C92			
Size Custom	Document Description **Premium - GND**		Rev 12
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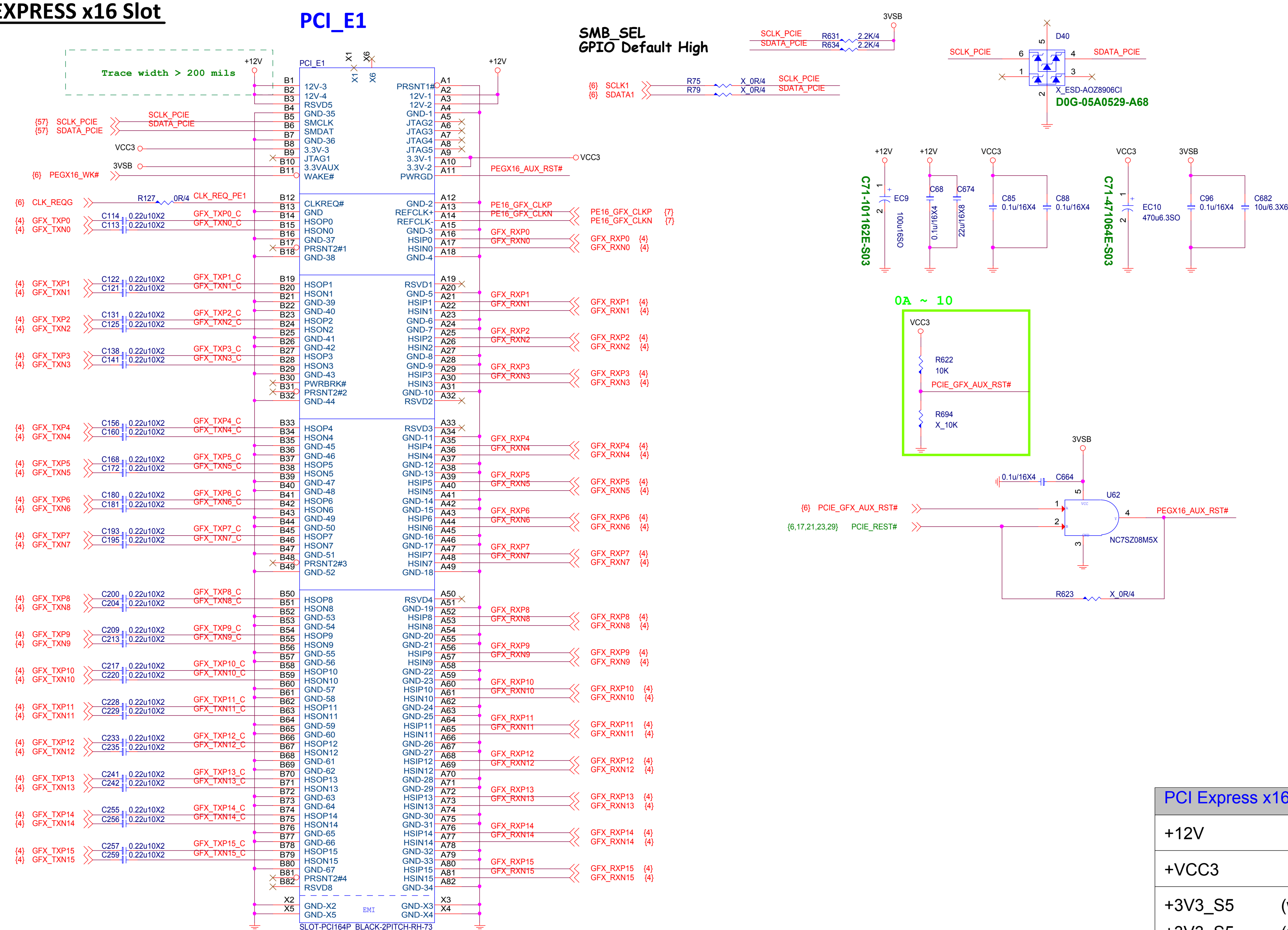
PCI EXPRESS x16 Slot



PCI Express x16 Slot		
+12V		- 5.5 A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

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Custom	PCI_E1 (X16)	12

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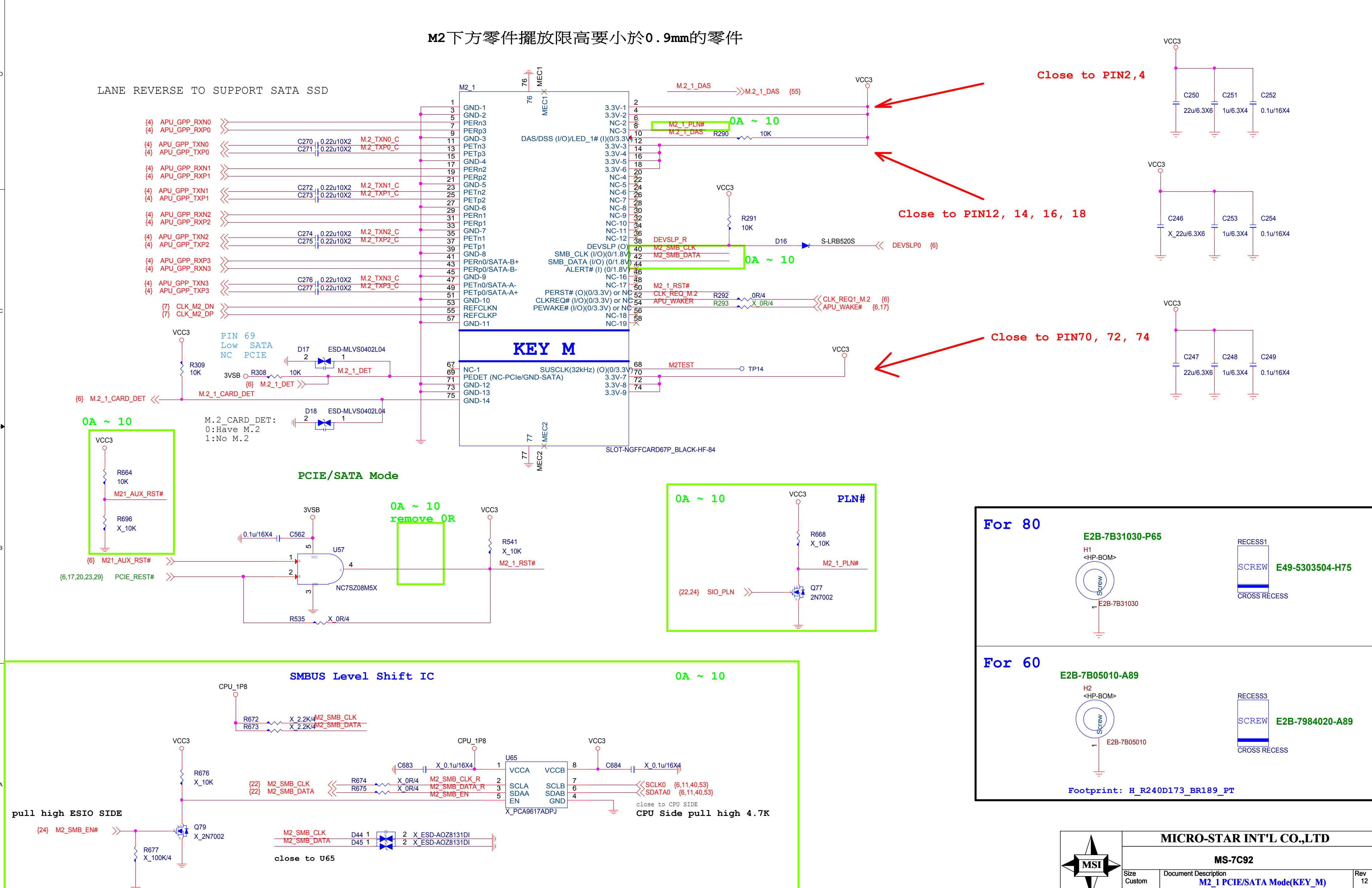
M.2_1 Connector



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Size	Document Description	Rev
Custom	M2_1 PCIE/SATA Mode(KEY_M)	12

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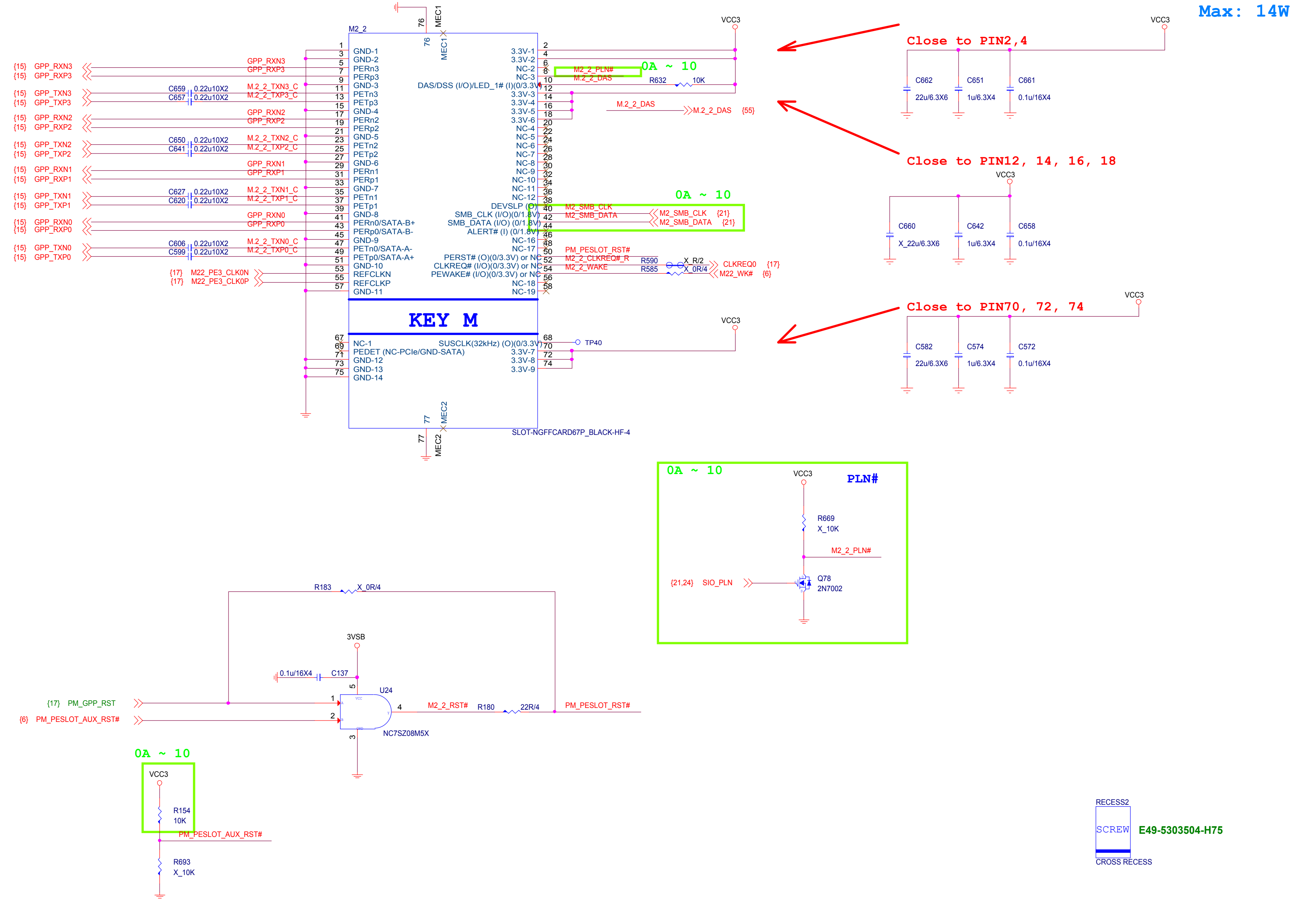
M.2_2 Connector

M2下方零件擺放限高要小於0.9mm的零件



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Size	Document Description	Rev
Custom	M2_2 PCIE Mode(KEY_M)	12

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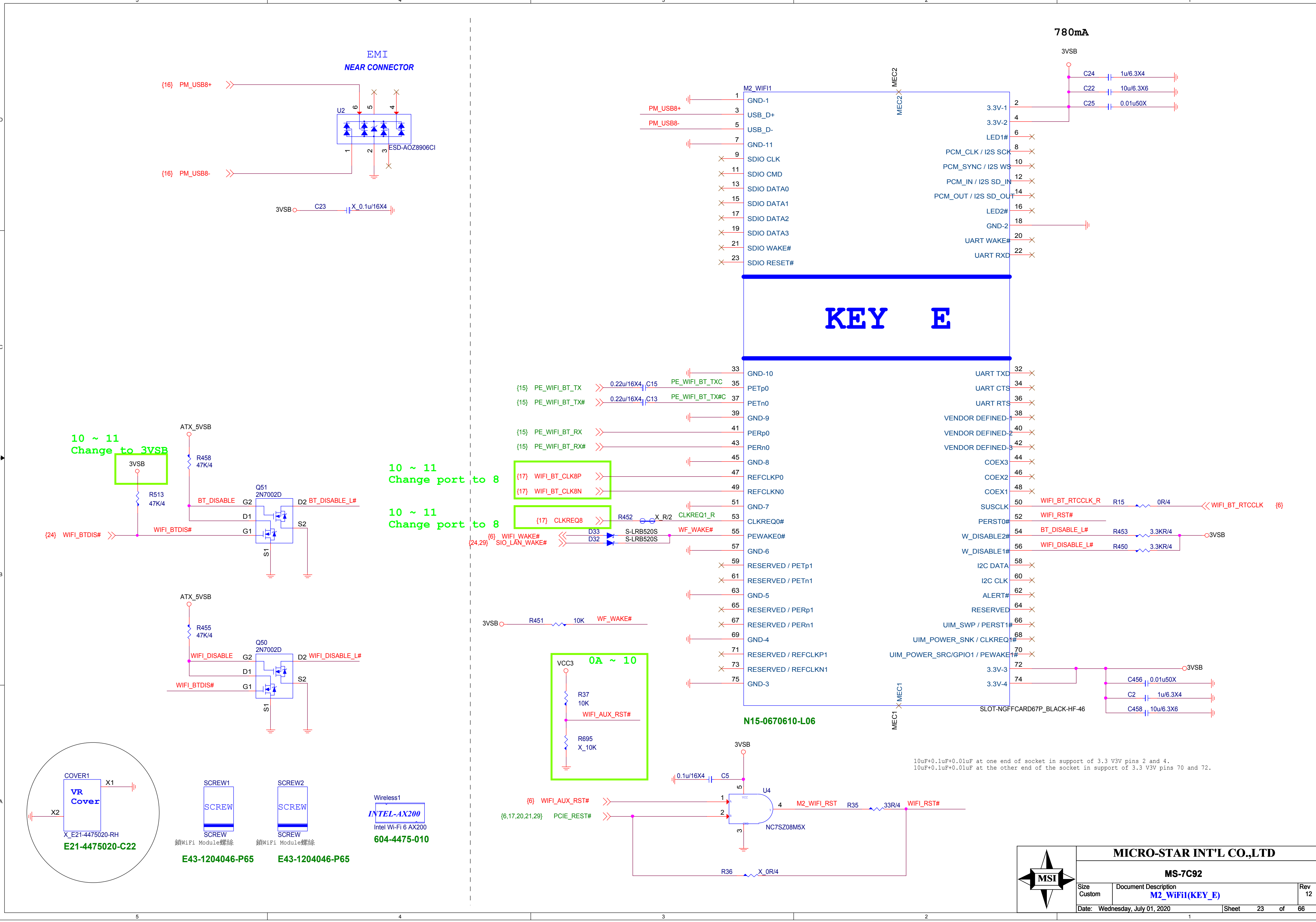
780mA
EMI
NEAR CONNECTOR
{16} PM_USB8+
{16} PM_USB8-
U2
ESD-AOZ8906CI
3VSB
C23
X_0.1u/16X4
M2_WIFI1
MEC2
1 GND-1
3 USB_D+
5 USB_D-
7 GND-11
9 SDIO CLK
11 SDIO CMD
13 SDIO DATA0
15 SDIO DATA1
17 SDIO DATA2
19 SDIO DATA3
21 SDIO WAKE#
23 SDIO RESET#
2 3.3V-1
4 3.3V-2
6 LED1#
8 PCM_CLK / I2S SCK
10 PCM_SYNC / I2S WS
12 PCM_IN / I2S SD_IN
14 PCM_OUT / I2S SD_OUT
16 LED2#
18 GND-2
20 UART WAKE#
22 UART RXD
C24 1u/6.3X4
C22 10u/6.3X6
C25 0.01u50X
KEY E
33 GND-10
35 PETp0
37 PETn0
39 GND-9
41 PERp0
43 PERn0
45 GND-8
47 REFCLKP0
49 REFCLKN0
51 GND-7
53 CLKREQ0#
55 PEWAKE0#
57 GND-6
59 RESERVED / PETp1
61 RESERVED / PETn1
63 GND-5
65 RESERVED / PERp1
67 RESERVED / PERn1
69 GND-4
71 RESERVED / REFCLKP1
73 RESERVED / REFCLKN1
75 GND-3
32 UART TXD
34 UART CTS
36 UART RTS
38 VENDOR DEFINED-1
40 VENDOR DEFINED-2
42 VENDOR DEFINED-3
44 COEX3
46 COEX2
48 COEX1
50 SUSCLK
52 PERST0#
54 W_DISABLE2#
56 W_DISABLE1#
58 I2C DATA
60 I2C CLK
62 ALERT#
64 RESERVED
66 UIM_SWP / PERST1#
68 UIM_POWER_SNK / CLKREQ1#
70 UIM_POWER_SRC/GPIO1 / PEWAKE1#
72 3.3V-3
74 3.3V-4
MEC1
SLOT-NGFFCARD67P_BLACK-HF-46
N15-0670610-L06
{15} PE_WIFI_BT_TX
{15} PE_WIFI_BT_TX#
0.22u/16X4 C15
0.22u/16X4 C13
PE_WIFI_BT_TXC
PE_WIFI_BT_TX#C
{15} PE_WIFI_BT_RX
{15} PE_WIFI_BT_RX#
10 ~ 11
Change port to 8
{17} WIFI_BT_CLK8P
{17} WIFI_BT_CLK8N
10 ~ 11
Change port to 8
{17} CLKREQ8
R452 X_R/2
CLKREQ1_R
D33 S-LRB520S
D32 S-LRB520S
WF_WAKE#
{6} WIFI_WAKE#
{24,29} SIO_LAN_WAKE#
WIFI_BT_RTCCLK_R R15 0R/4 WIFI_BT_RTCCLK {6}
WIFI_RST#
BT_DISABLE_L# R453 3.3KR/4
WIFI_DISABLE_L# R450 3.3KR/4
3VSB
C456 0.01u50X
C2 1u/6.3X4
C458 10u/6.3X6
10 ~ 11
Change to 3VSB
ATX_5VSB
R458 47K/4
R513 47K/4
Q51 2N7002D
BT_DISABLE
G2 D2 BT_DISABLE_L#
D1 S2 G1 S1
{24} WIFI_BTDIS#
WIFI_BTDIS#
ATX_5VSB
R455 47K/4
Q50 2N7002D
WIFI_DISABLE
D2 WIFI_DISABLE_L#
3VSB R451 10K WF_WAKE#
VCC3
0A ~ 10
R37 10K
WIFI_AUX_RST#
R695 X_10K
3VSB
0.1u/16X4 C5
U4
NC7SZ08M5X
{6} WIFI_AUX_RST#
{6,17,20,21,29} PCIE_REST#
M2_WIFI_RST R35 33R/4 WIFI_RST#
R36 X_0R/4
10uF+0.1uF+0.01uF at one end of socket in support of 3.3 V3V pins 2 and 4.
10uF+0.1uF+0.01uF at the other end of the socket in support of 3.3 V3V pins 70 and 72.
COVER1
VR Cover
X1
X2
X_E21-4475020-RH
E21-4475020-C22
SCREW1
SCREW
鎖WiFi Module螺絲
E43-1204046-P65
SCREW2
SCREW
鎖WiFi Module螺絲
E43-1204046-P65
Wireless1
INTEL-AX200
Intel Wi-Fi 6 AX200
604-4475-010
MICRO-STAR INT'L CO.,LTD
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Size Custom
Document Description
M2_WiFi1(KEY_E)
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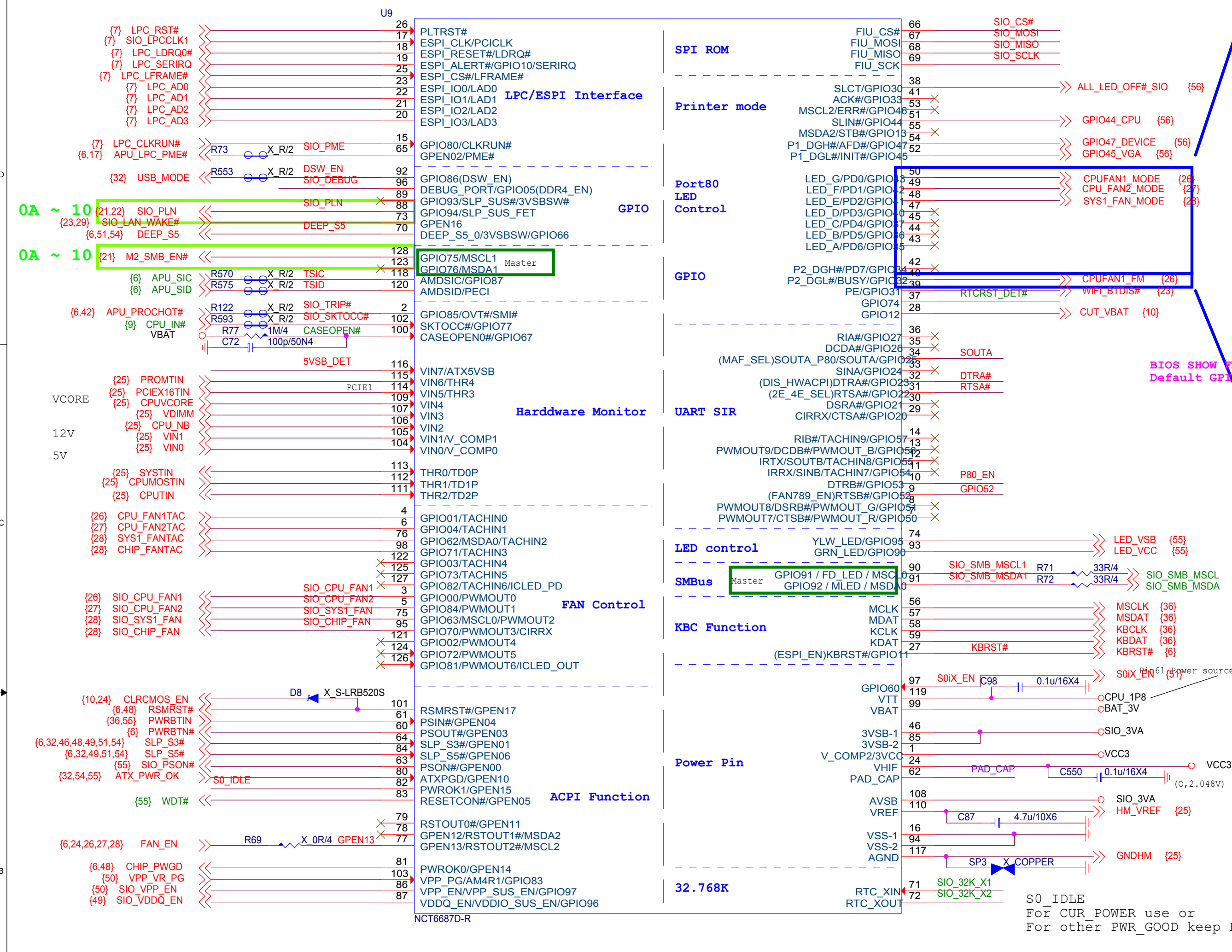


By PM Define FAN name

FAN MODE USE	FAN
GP43	CPUFAN1
GP42	CPUFAN2 PUMPFAN
GP41	SYSFAN1
GP40	SYSFAN2
GP37	SYSFAN3
GP36	SYSFAN4
GP35	SYSFAN5
GP34	SYSFAN6

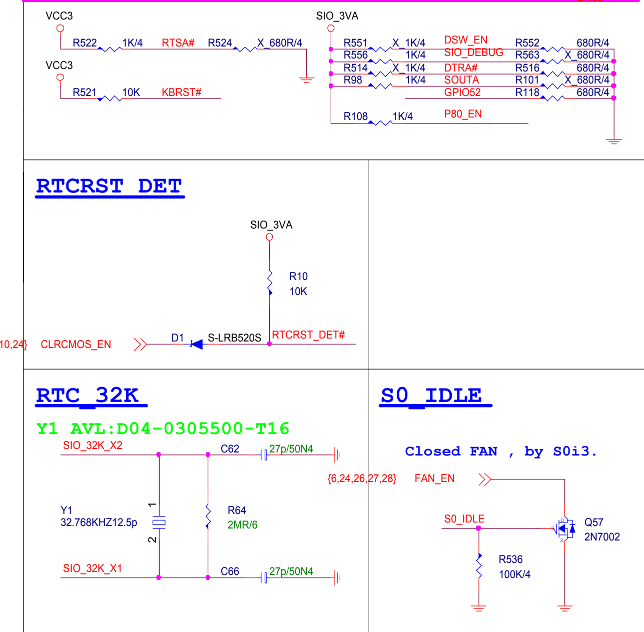
By PM Define FAN name

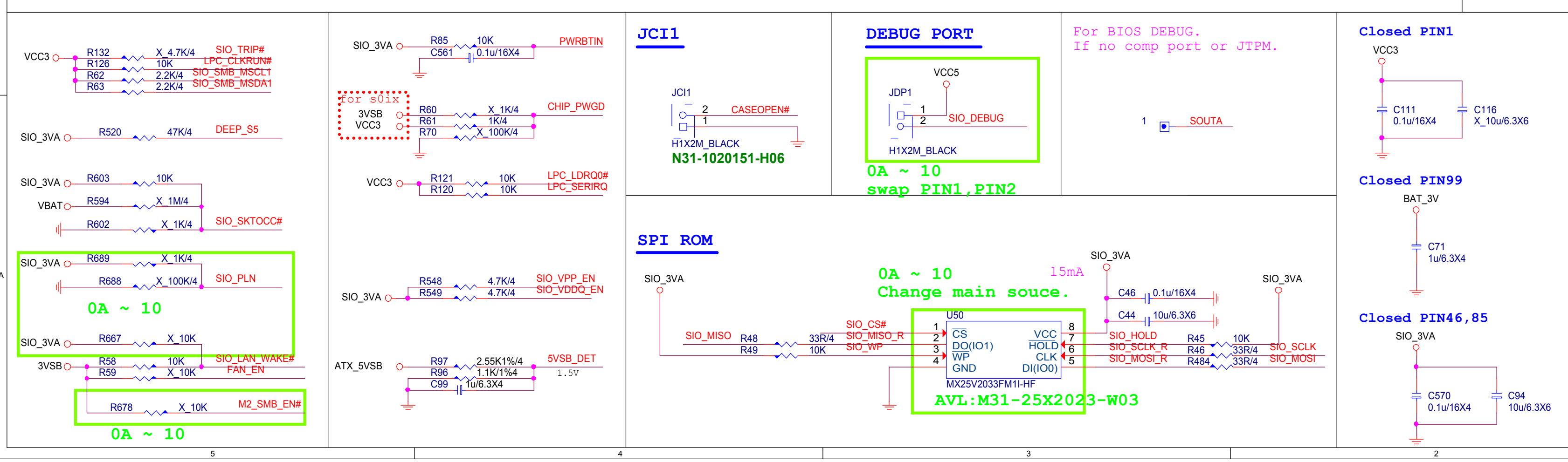
SHOW FAN MODE USE	FAN
GP32	CPUFAN1

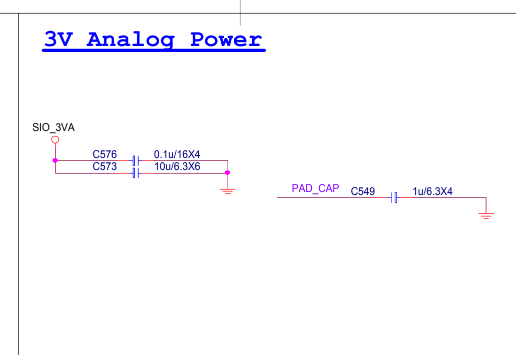
POWER ON STRAPPING PIN FOR NCT6687D-R

PIN	NAME	Circuit NAME	0	1	Strap Point
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	3VCC
32	DIS_HWACPI	DTRA#	HW ACPI enable	HW ACPI disable	3VA
34	MAF_SEL	SOUTA	MAF enable	MAF disable	3VA
92	DSW_EN	DSW_EN	DSW disable	DSW enable	3VA
96	DDR4_EN	SIO_DEBUG	DDR4 control disable	DDR4 control enable	3VA
9	FAN789_EN (FW setting)	GPIO52	FAN789 disable	FAN789 enable	3VA
10	P80_EN	GPIO53	Port80 LED	GPIO	3VA

PIN	NAME	Circuit NAME	VCC3	3VA	Strap Point
27	ESPI_EN	KBRST#	LPC	ESPI	VCC3 or 3VA







MICRO-STAR INT'L CO.,LTD

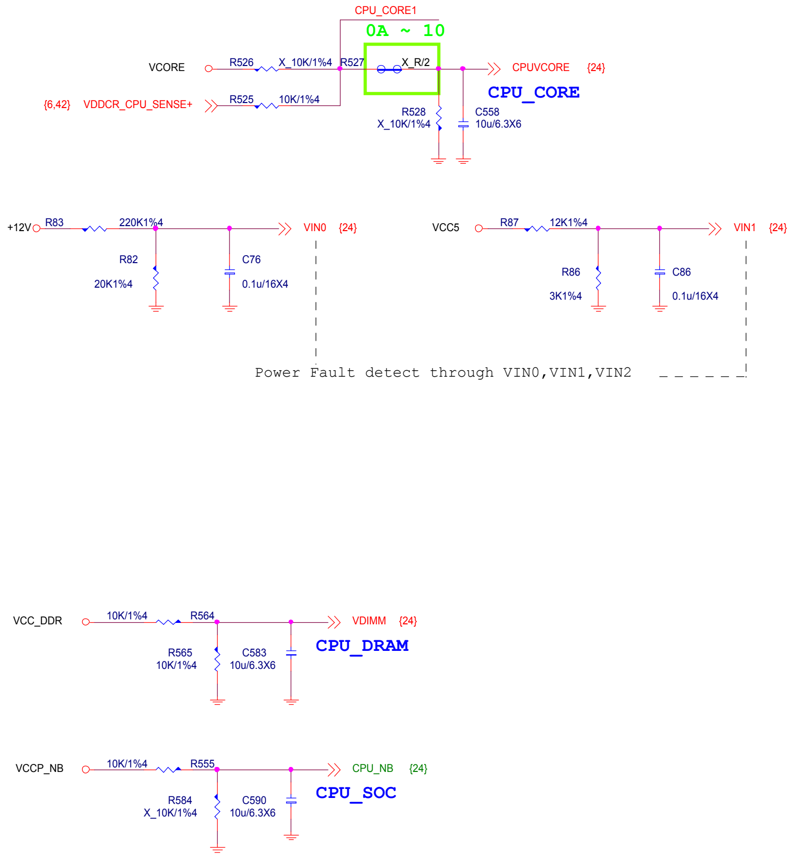
MS-7C92

Size	Document Description	Rev
Custom	SIO - NCT6687D-R(For AMD)	12

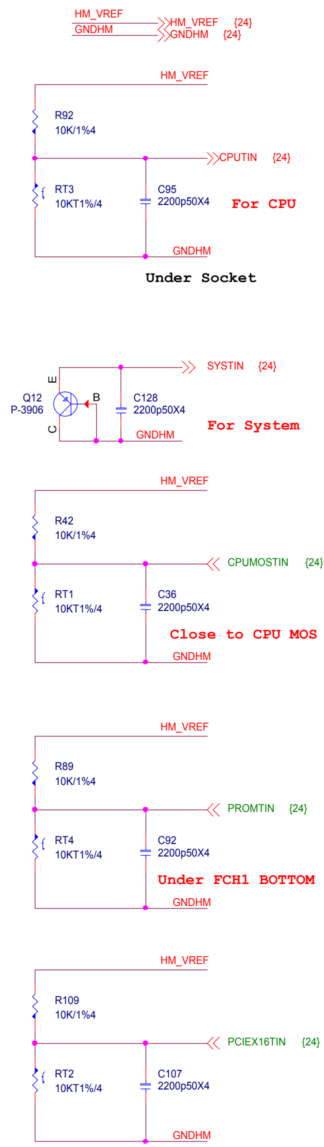
Date: Wednesday, July 01, 2020 — Sheet 24 of 66

HW Monitor - Voltage

SIO HM Voltage over 2.048V will not detect



TEMP SENSOR

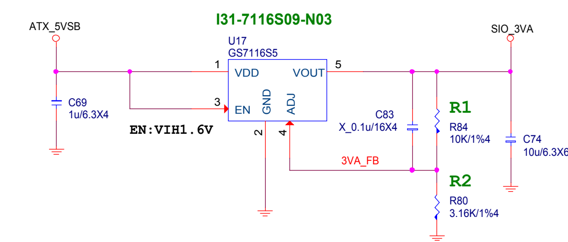


Close to "PCI_E1.X4" PIN

PM RESET

CPU RESET

SIO_3VA



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.16K))
= 3.33V

MICRO-STAR INT'L CO.,LTD

MS-7C92

Size: Custom | Document Description: SIO - HW Monitor | Rev: 12

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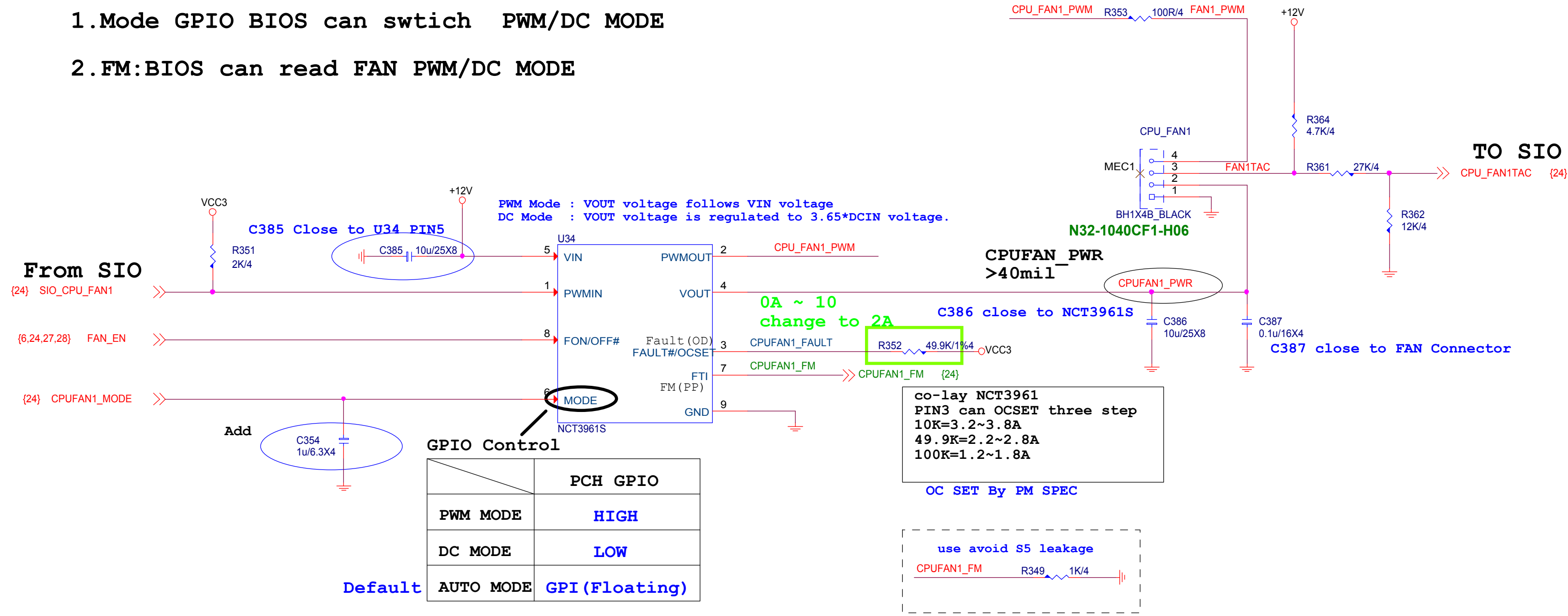
CPUFAN1

TYPE N : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

2.FM:BIOS can read FAN PWM/DC MODE



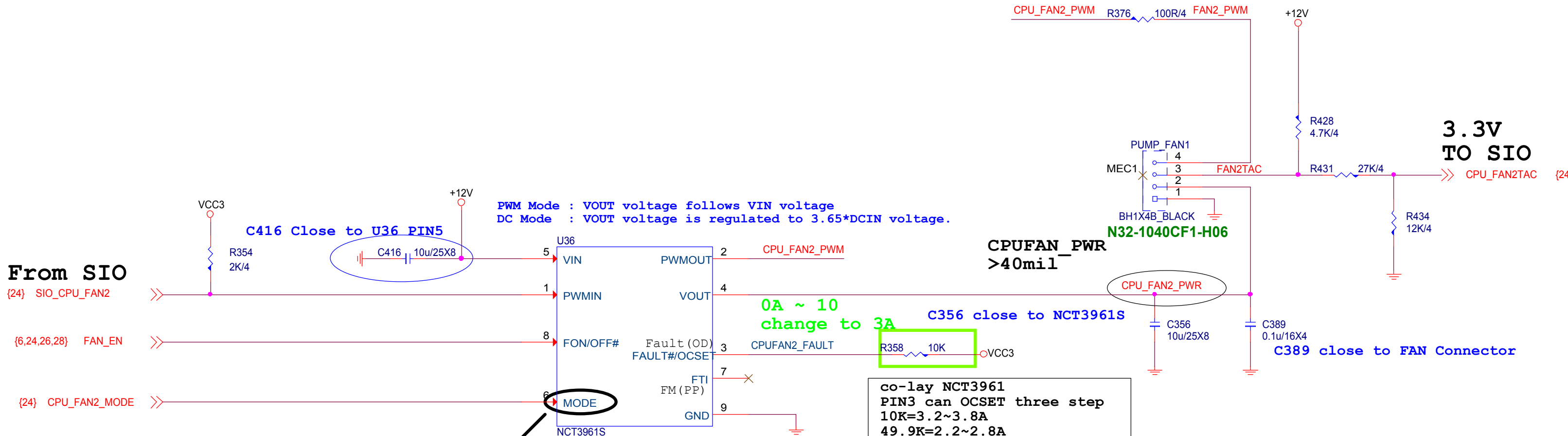
	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default

PUMPFAN1

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



co-lay NCT3961
PIN3 can OCSET three step
10K=3.2~3.8A
49.9K=2.2~2.8A
100K=1.2~1.8A

OC SET By PM SPEC

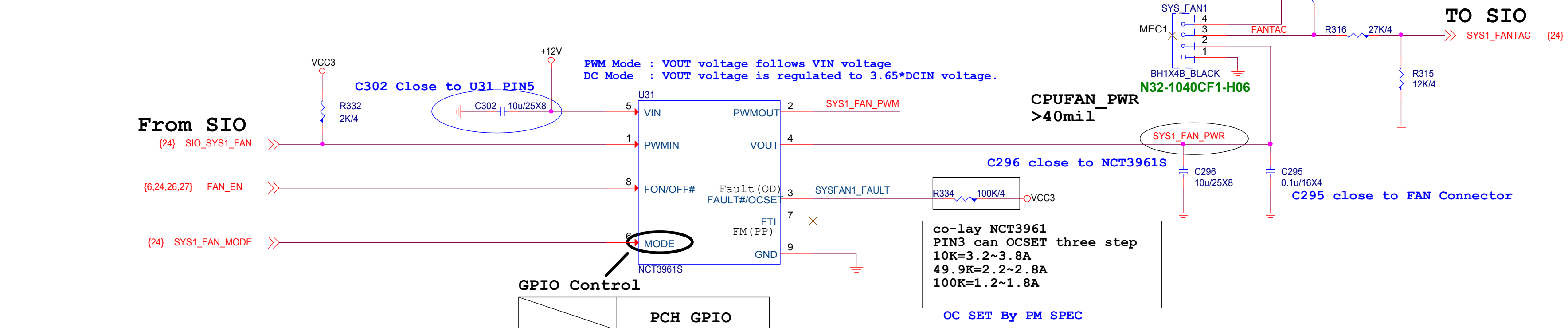
GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

SYSFAN1

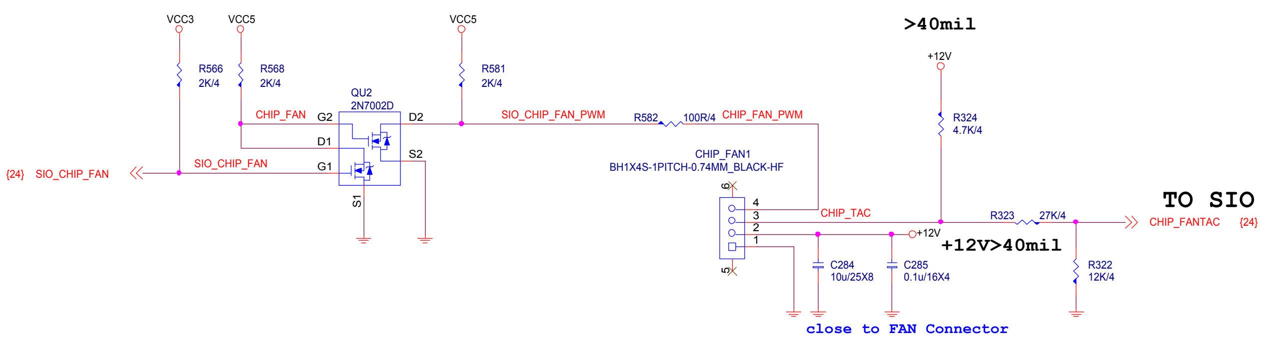
TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

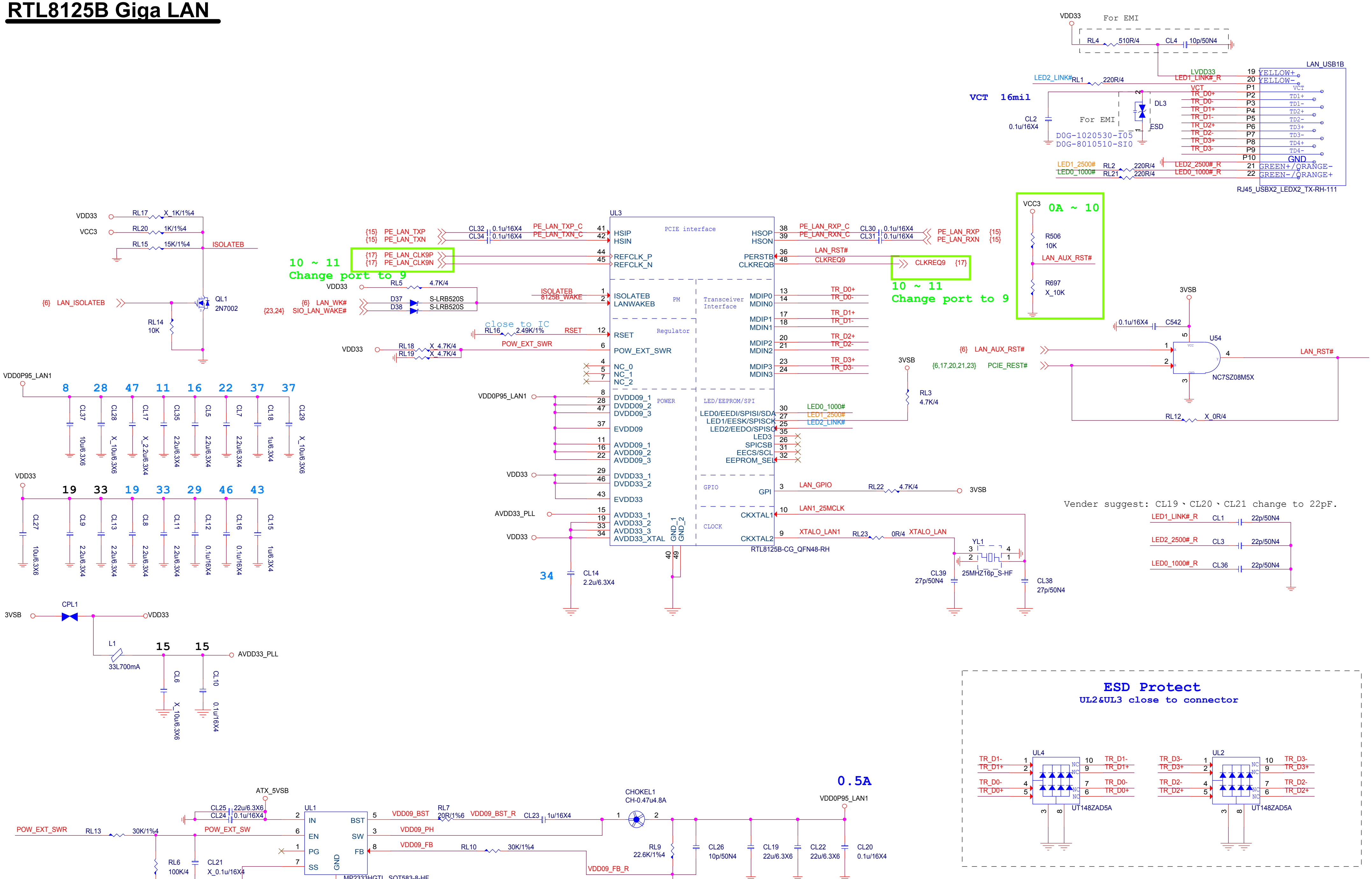


GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)



RTL8125B Giga LAN



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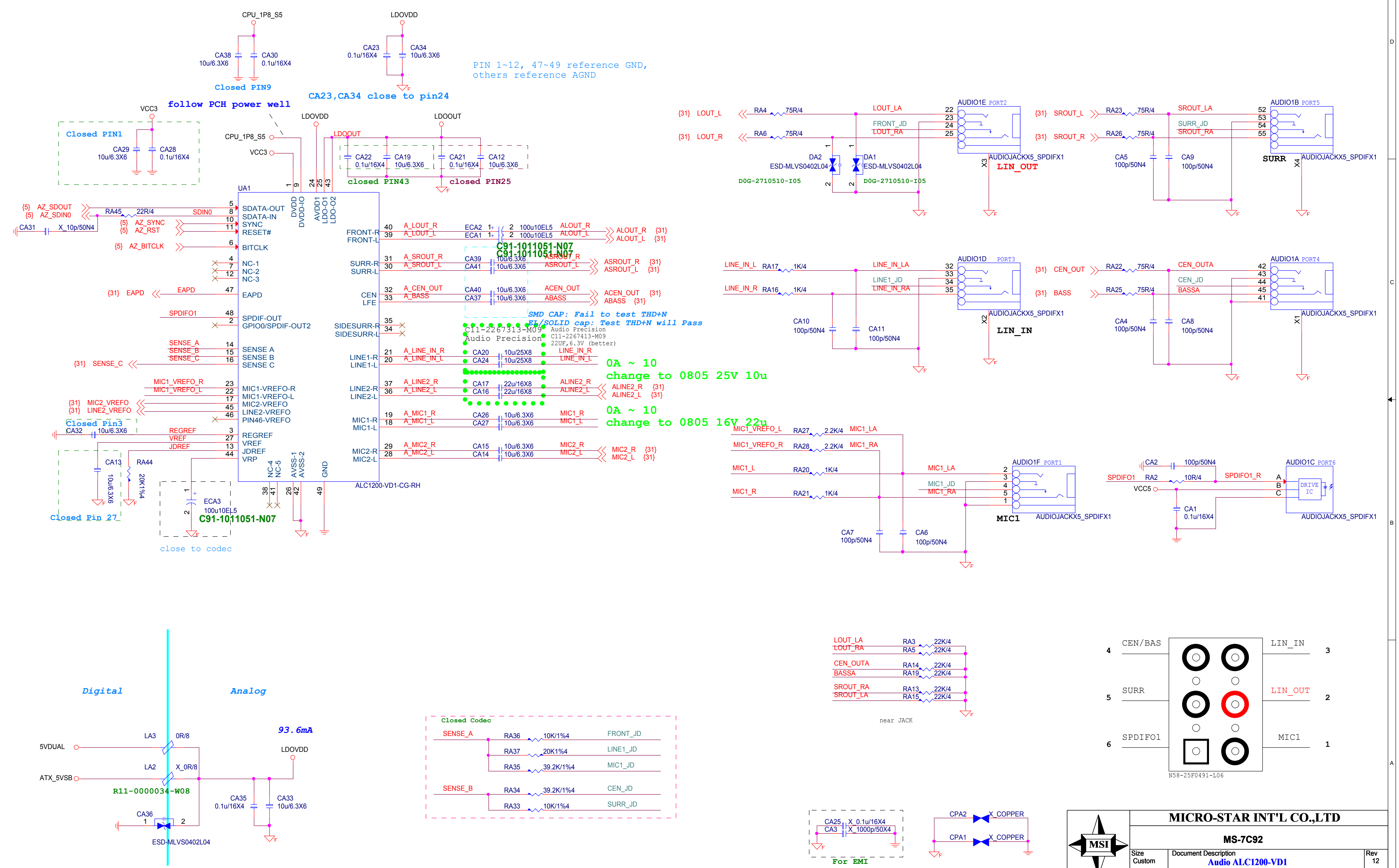
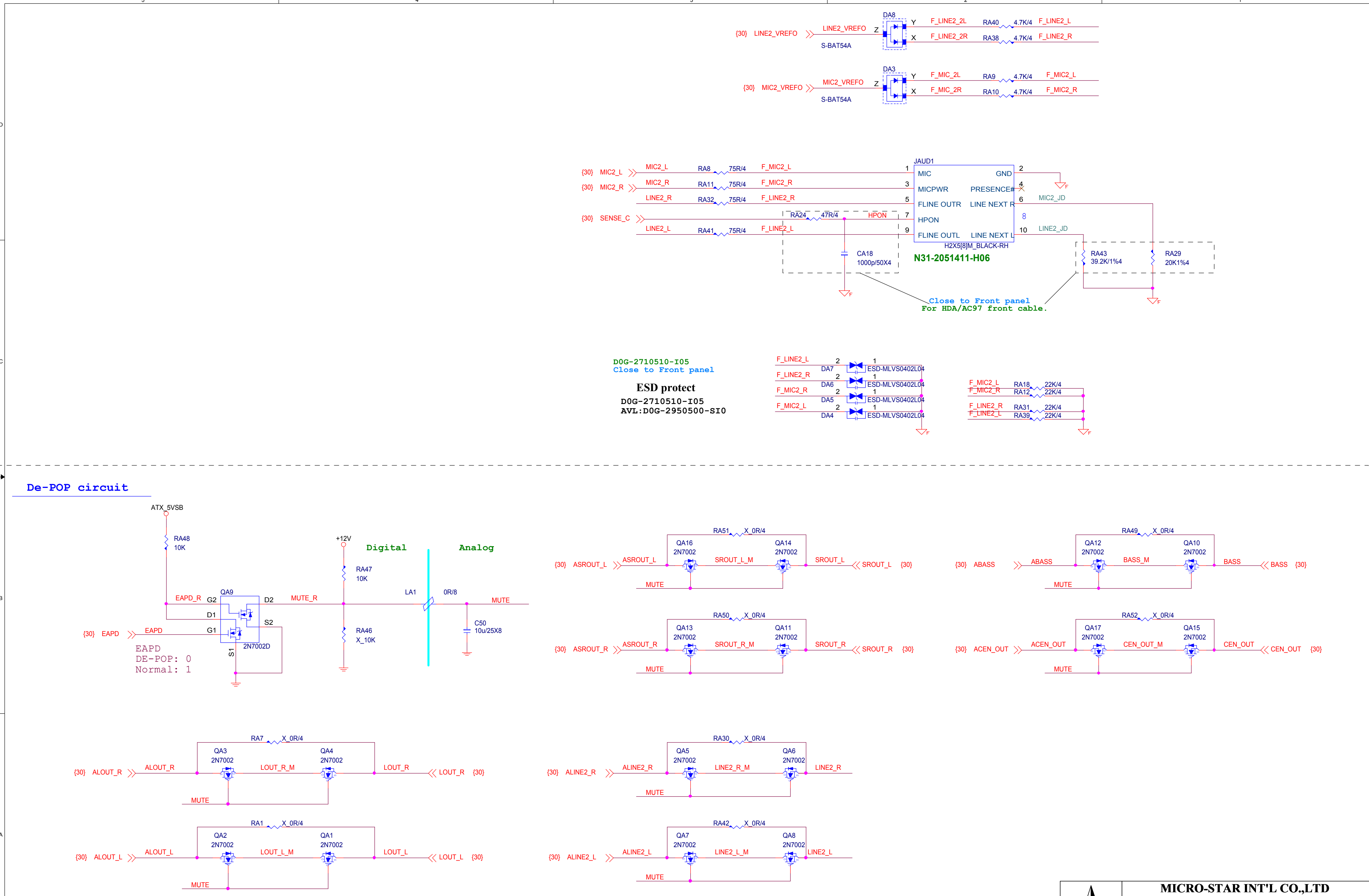
ALC1200-VD1_48PIN



MICRO-STAR INT'L CO.,LTD	
MS-7C92	
Size: Custom	Document Description: Audio ALC1200-VD1	Rev: 12
Date: Wednesday, July 01, 2020	Sheet 30 of 66



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MS-7C92

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Custom	Audio DePoP	12

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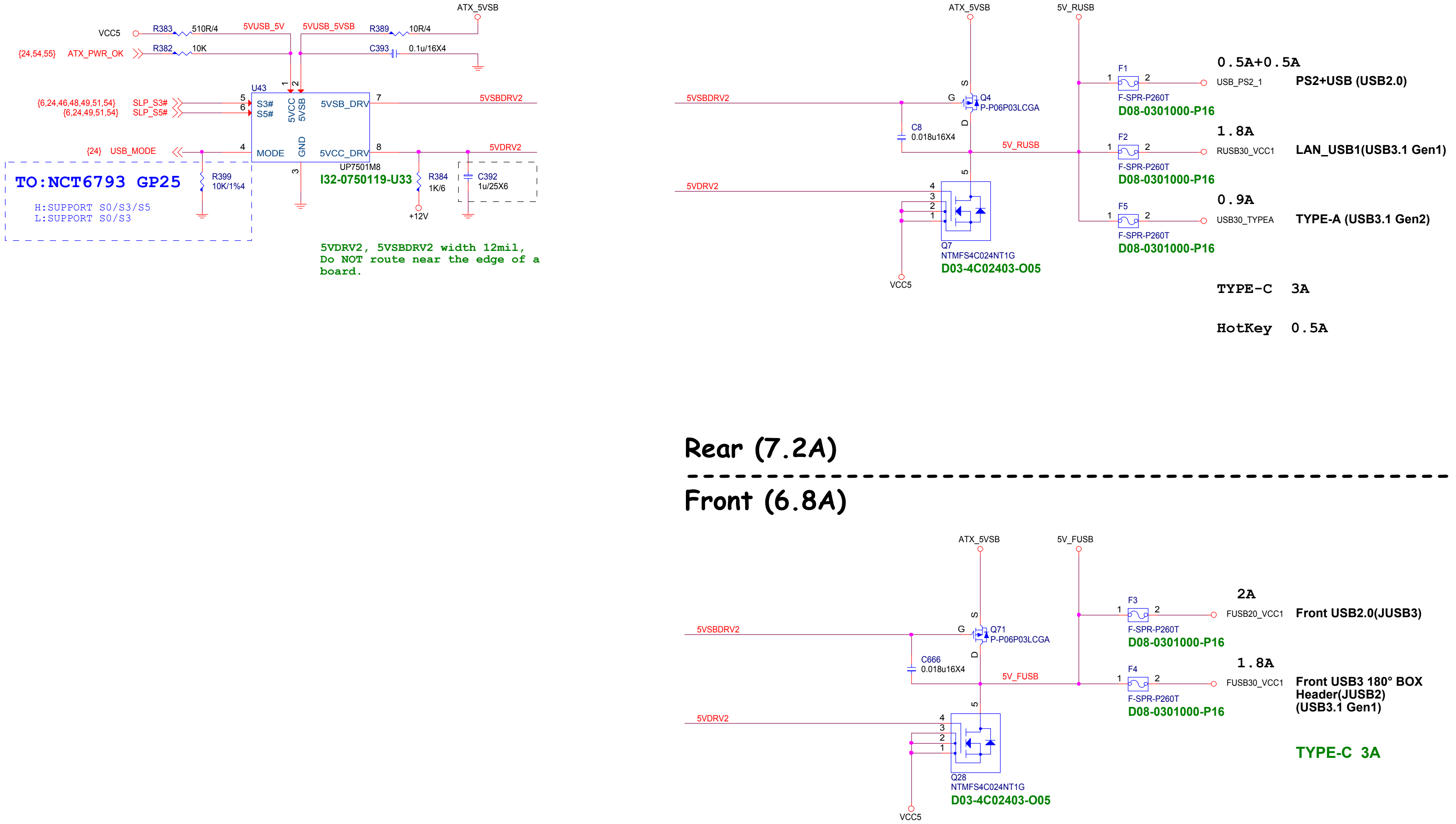
USB Power



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MS-7C92

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Custom	USB Power - UP7501	12

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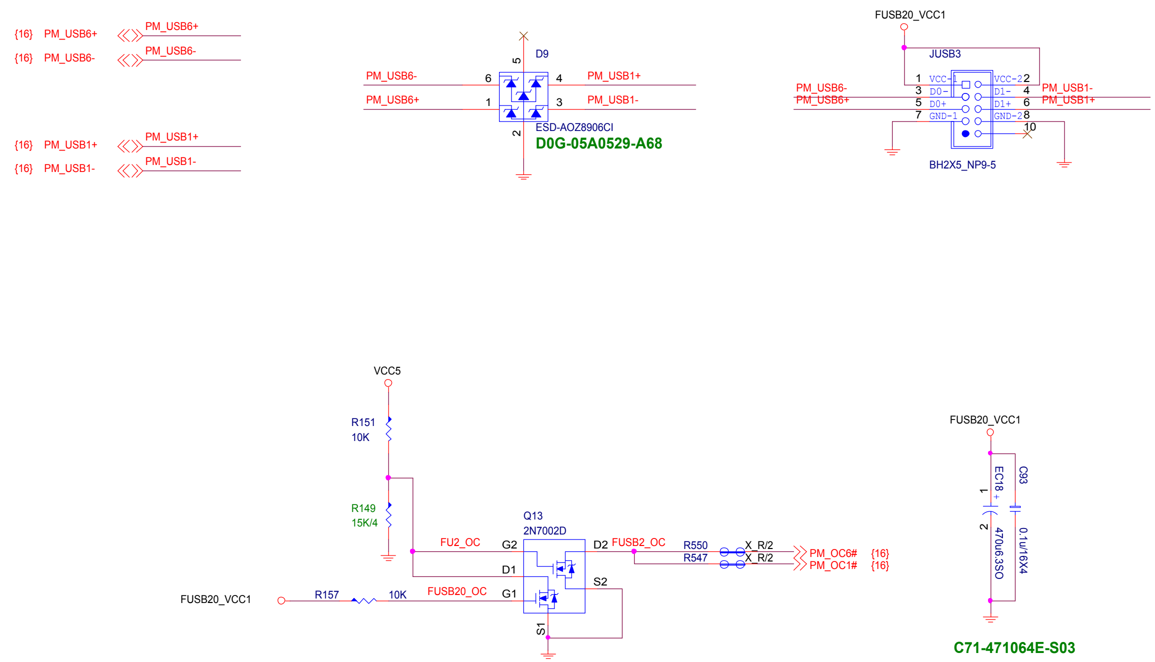
Front USB2.0(JUSB3)

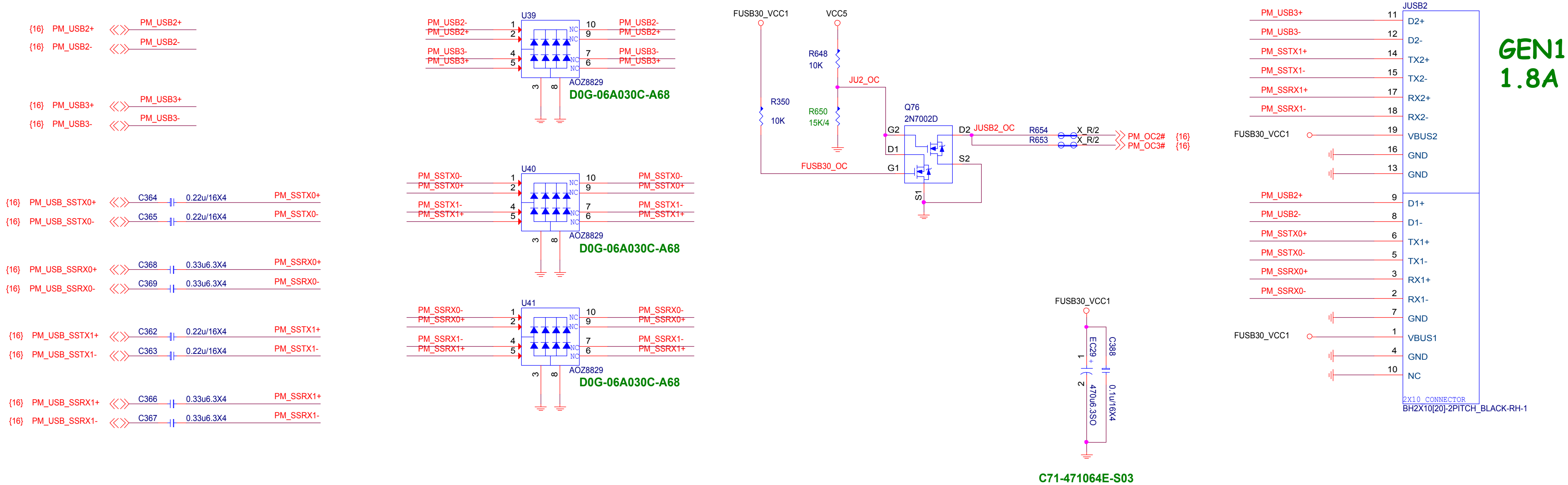
Form GL850G USB2.0 HUB

5V@1A

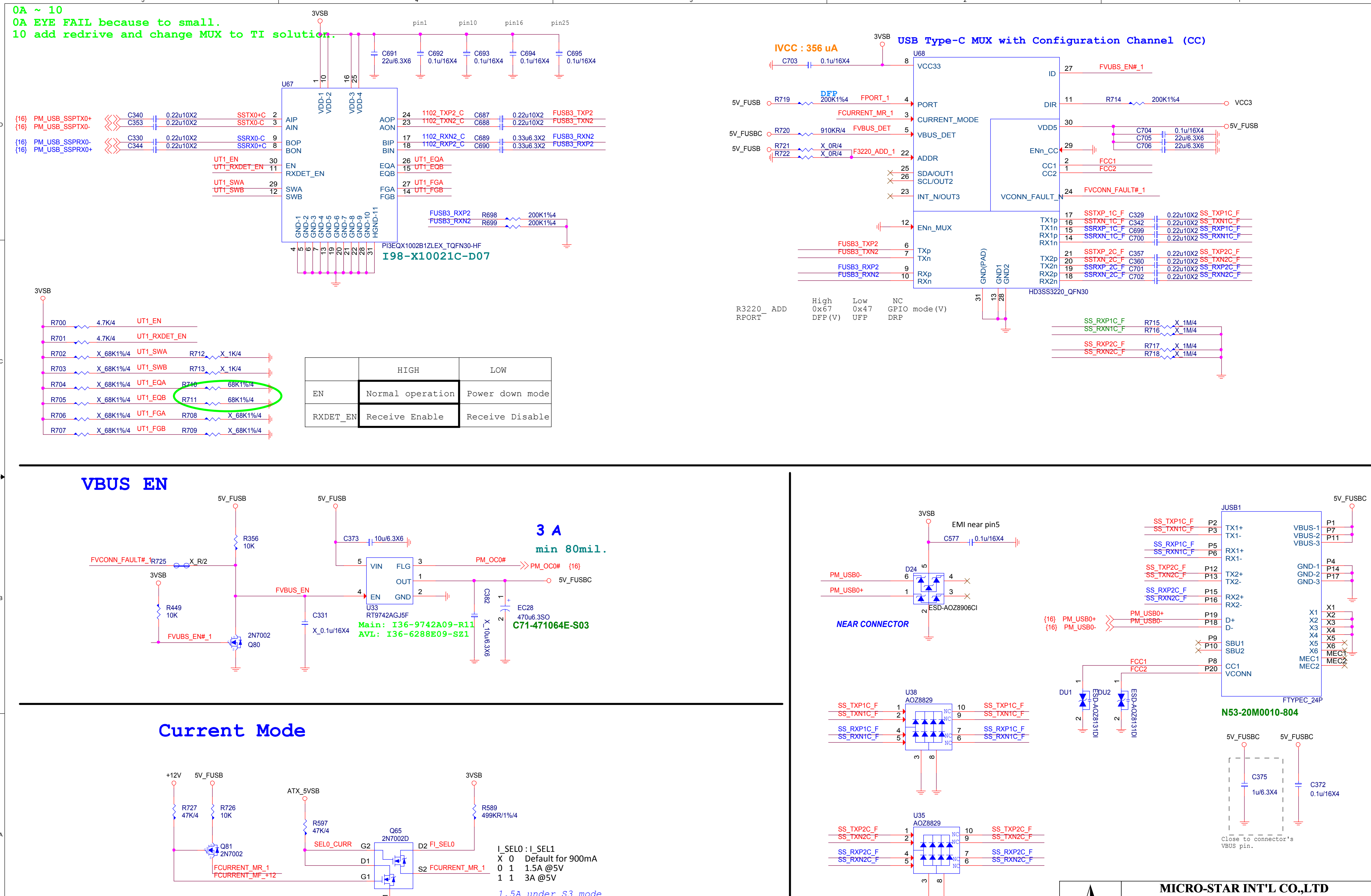


Front USB3 180° BOX Header(JUSB2)

5V@1.8A



MICRO-STAR INT'L CO.,LTD			
MS-7C92			
Size: Custom	Document Description: Front USB3.0 Header		Rev: 12
Date: Wednesday, July 01, 2020	Sheet 34 of 66		



	HIGH	LOW
EN	Normal operation	Power down mode
RXDET_EN	Receive Enable	Receive Disable

MICRO-STAR INT'L CO.,LTD

MS-7C92

Size: Custom

Document Description: Front USB3.1 Type C / M + R

Rev: 12

Date: Wednesday, July 01, 2020

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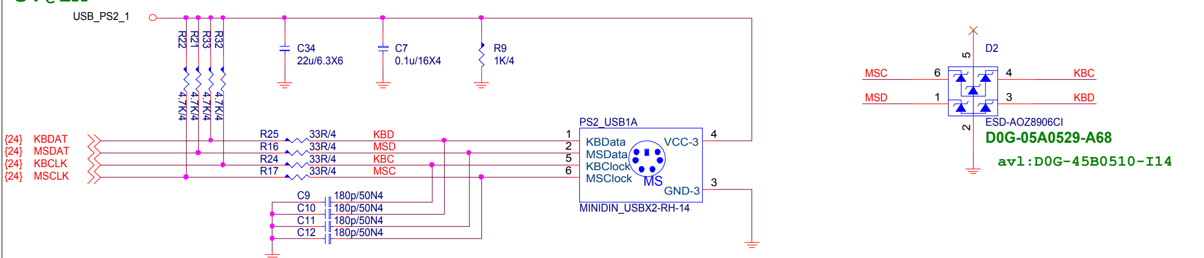
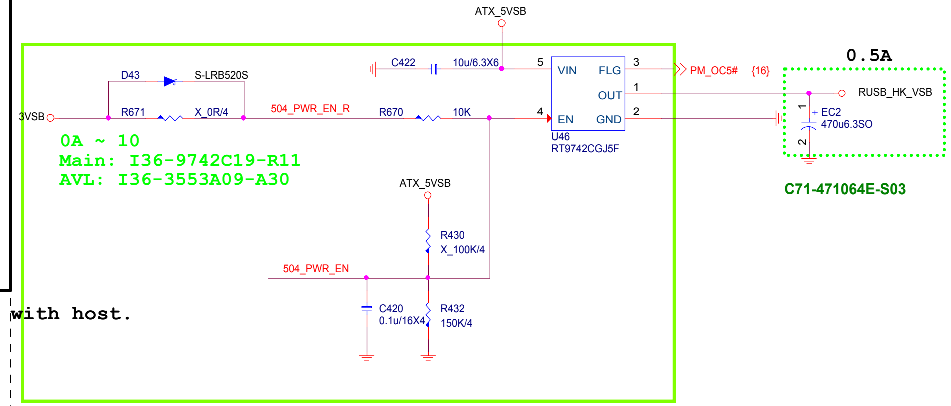
PS2+USB (USB2.0)

5V@1A

layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch



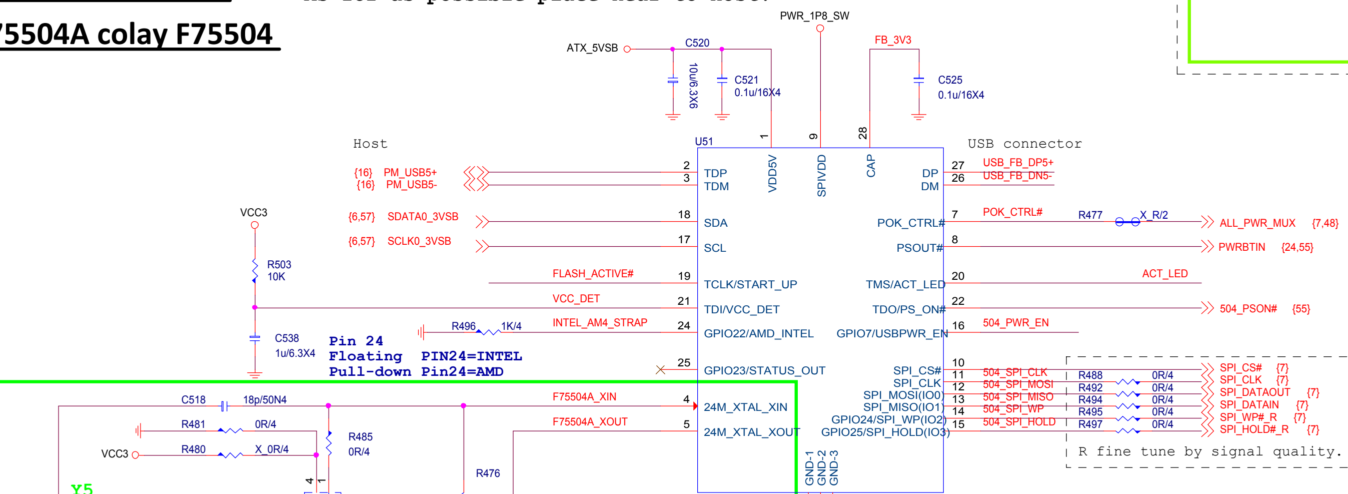
HOTKEY POWER

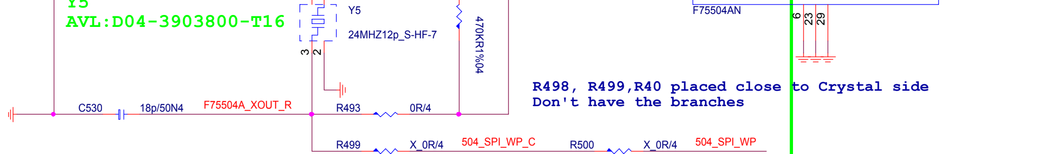


USB Flash BIOS

F75504A/F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.

F75504A colay F75504





R498, R499,R40 placed close to Crystal side
Don't have the branches

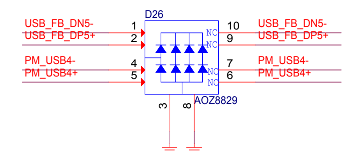
Stuff= O Unstuff= X	R495	R497
F75504A	O	O
F75504	X	X

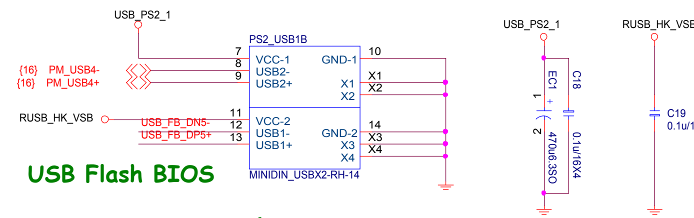
2019/06/17

R503 placed close R40

Stuff= O Unstuff= X	R485	R493	R499	R500	C518	R481	R480	R476	Y5
F75504A	O	O	X	X	10pF	0R	X	O	D04-3902700-F07
F75504	X	X	O	O	X	0.1uF	O	X	D05-1100600-F07

ESD close to connector.





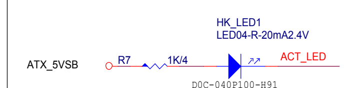
USB Flash BIOS

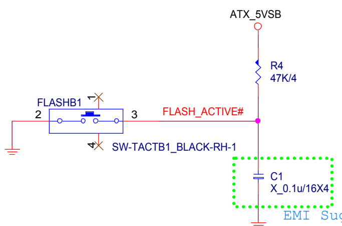
1A

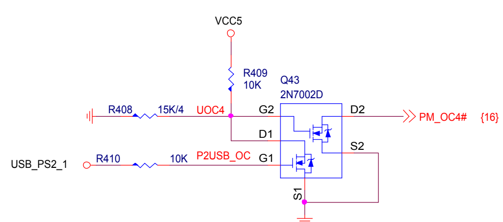
C71-471064E-S03

0A ~ 10
not support ALL LED OFF , remove 2n7002.

LED close to USB port

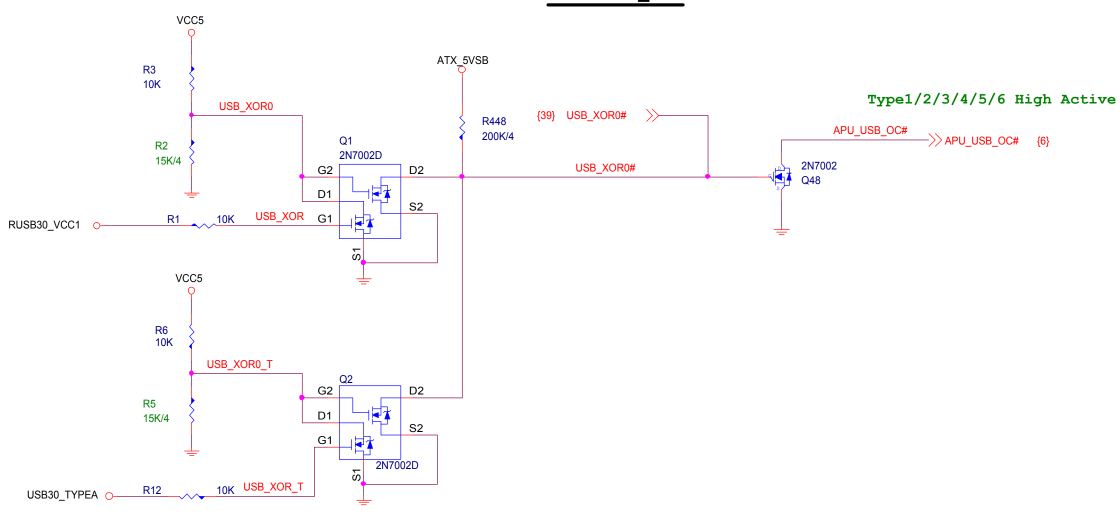




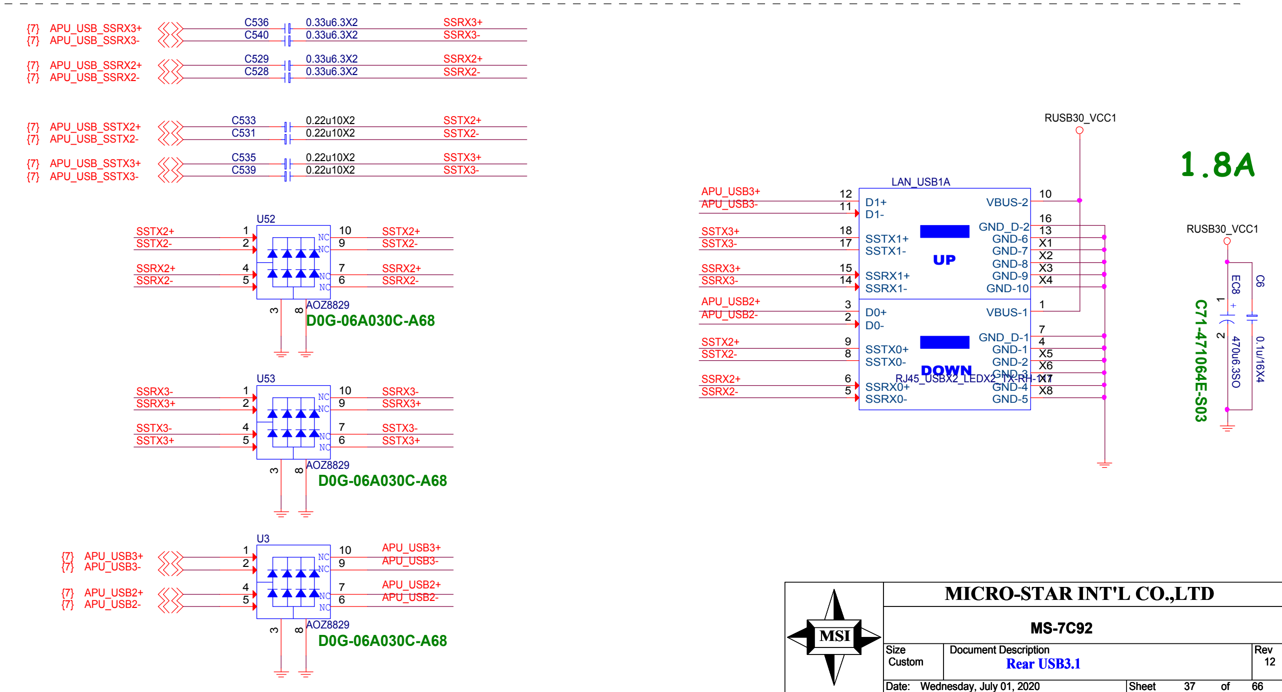


MICRO-STAR INT'L CO.,LTD		
MS-7C92		
Size: Custom	Document Description: Rear USB2.0+PS2+F75504A	Rev: 12
Date: Wednesday, July 01, 2020	Sheet 36 of 66	

CPU USB_OC



Rear USB3.1 GEN1 5V@1.8A



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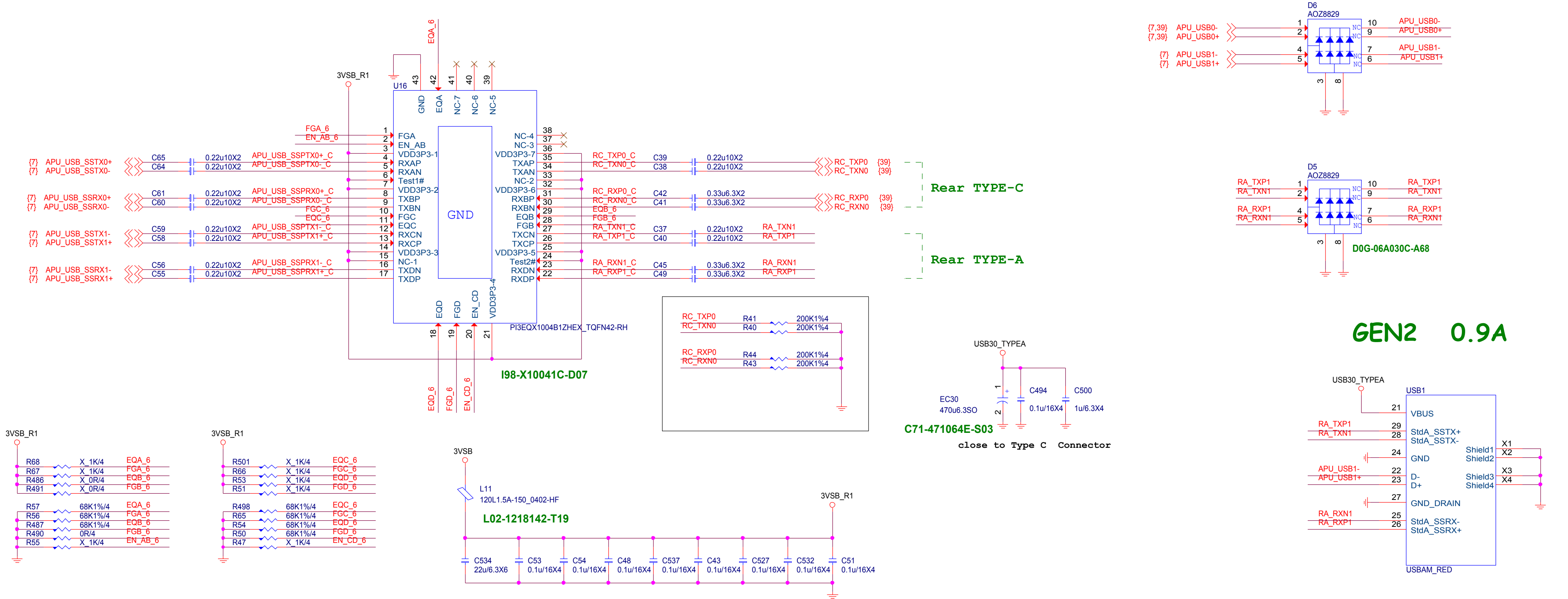
MS-7C92		
Size: Custom	Document Description: Rear USB3.1	Rev: 12
Date: Wednesday, July 01, 2020	Sheet 37 of 66	

TYPE-A PI3EQX1004 Redriver



EQ	dB	
0	10.9	0 to GND
R	6.7	68K to GND
F	8.9	NC
1	13.1	0 to VDD

		EQ	FG
USB3_TX4	A	R	F
USB3_RX4	B	R	L
USB3_TX3	C	R	F
USB3_RX3	D	R	L

FG	dB	
0	-3	0 to GND
R	-1.5	68K to GND
F	0	NC
1	2	0 to VDD

MICRO-STAR INT'L CO.,LTD

MS-7C92

Size	Document Description	Rev
Custom	Rear USB3.1 Type A / Redrive	12

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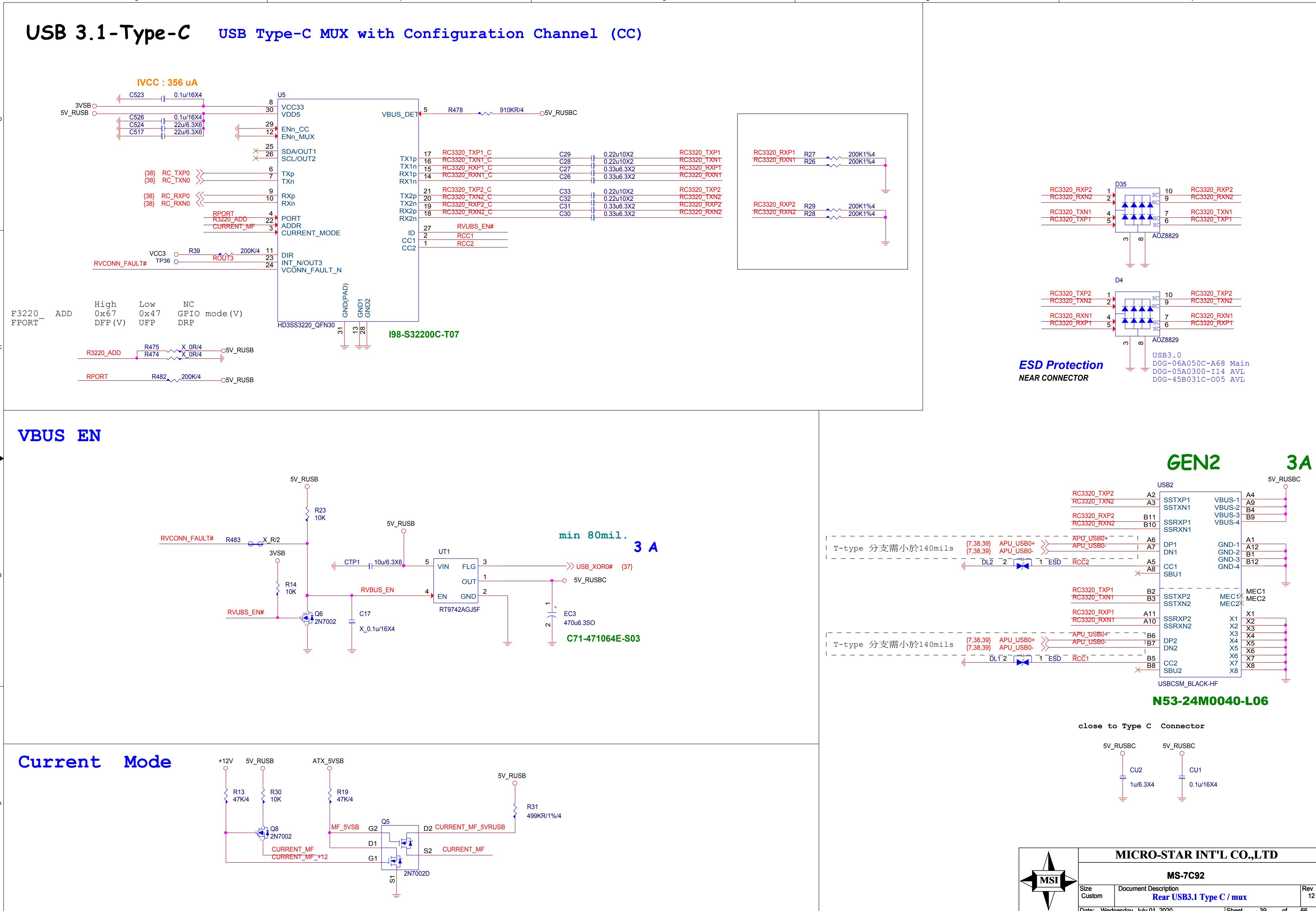

USB 3.1-Type-C
USB Type-C MUX with Configuration Channel (CC)
IVCC : 356 uA
3VSB
5V_RUSB
C523 0.1u/16X4
C526 0.1u/16X4
C524 22u/6.3X6
C517 22u/6.3X6
U5
VCC33
VDD5
ENn_CC
ENn_MUX
SDA/OUT1
SCL/OUT2
TXp
TXn
RXp
RXn
PORT
ADDR
CURRENT_MODE
DIR
INT_N/OUT3
VCONN_FAULT_N
VBUS_DET
TX1p
TX1n
RX1p
RX1n
TX2p
TX2n
RX2p
RX2n
ID
CC1
CC2
GND(PAD)
GND1
GND2
HD3SS3220_QFN30
I98-S32200C-T07
R478 910KR/4
5V_RUSBC
{38} RC_TXP0
{38} RC_TXN0
{38} RC_RXP0
{38} RC_RXN0
RPORT
R3220_ADD
CURRENT_MF
VCC3
R39 200K/4
TP36
ROUT3
RVCONN_FAULT#
RC3320_TXP1_C
RC3320_TXN1_C
RC3320_RXP1_C
RC3320_RXN1_C
RC3320_TXP2_C
RC3320_TXN2_C
RC3320_RXP2_C
RC3320_RXN2_C
RVUBS_EN#
RCC1
RCC2
C29 0.22u10X2
C28 0.22u10X2
C27 0.33u6.3X2
C26 0.33u6.3X2
C33 0.22u10X2
C32 0.22u10X2
C31 0.33u6.3X2
C30 0.33u6.3X2
RC3320_TXP1
RC3320_TXN1
RC3320_RXP1
RC3320_RXN1
RC3320_TXP2
RC3320_TXN2
RC3320_RXP2
RC3320_RXN2
R27 200K1%4
R26 200K1%4
R29 200K1%4
R28 200K1%4
F3220_ ADD High 0x67 Low 0x47 NC
FPORT DFP(V) UFP GPIO mode(V) DRP
R3220_ADD
R475 X_0R/4
R474 X_0R/4
RPORT
R482 200K/4
D35
D4
AOZ8829
ESD Protection
NEAR CONNECTOR
USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL
D0G-45B031C-O05 AVL
VBUS EN
R23 10K
RVCONN_FAULT#
R483 X_R/2
R14 10K
RVUBS_EN#
Q6 2N7002
C17 X_0.1u/16X4
RVBUS_EN
CTP1 10u/6.3X6
UT1
VIN
FLG
OUT
EN
GND
RT9742AGJ5F
min 80mil.
3 A
USB_XOR0# {37}
EC3 470u6.3SO
C71-471064E-S03
GEN2
3A
USB2
SSTXP1
SSTXN1
SSRXP1
SSRXN1
DP1
DN1
CC1
SBU1
SSTXP2
SSTXN2
SSRXP2
SSRXN2
DP2
DN2
CC2
SBU2
VBUS-1
VBUS-2
VBUS-3
VBUS-4
GND-1
GND-2
GND-3
GND-4
MEC1
MEC2
USBCSM_BLACK-HF
N53-24M0040-L06
T-type 分支需小於140mils
{7,38,39} APU_USB0+
{7,38,39} APU_USB0-
DL2 ESD
DL1 ESD
close to Type C Connector
CU2 1u/6.3X4
CU1 0.1u/16X4
Current Mode
+12V
ATX_5VSB
R13 47K/4
R30 10K
R19 47K/4
R31 499KR/1%/4
Q8 2N7002
Q5 2N7002D
MF_5VSB
CURRENT_MF_5VRUSB
CURRENT_MF
CURRENT_MF_+12
MICRO-STAR INT'L CO.,LTD
MSI
MS-7C92
Size Custom
Document Description
Rear USB3.1 Type C / mux
Rev 12
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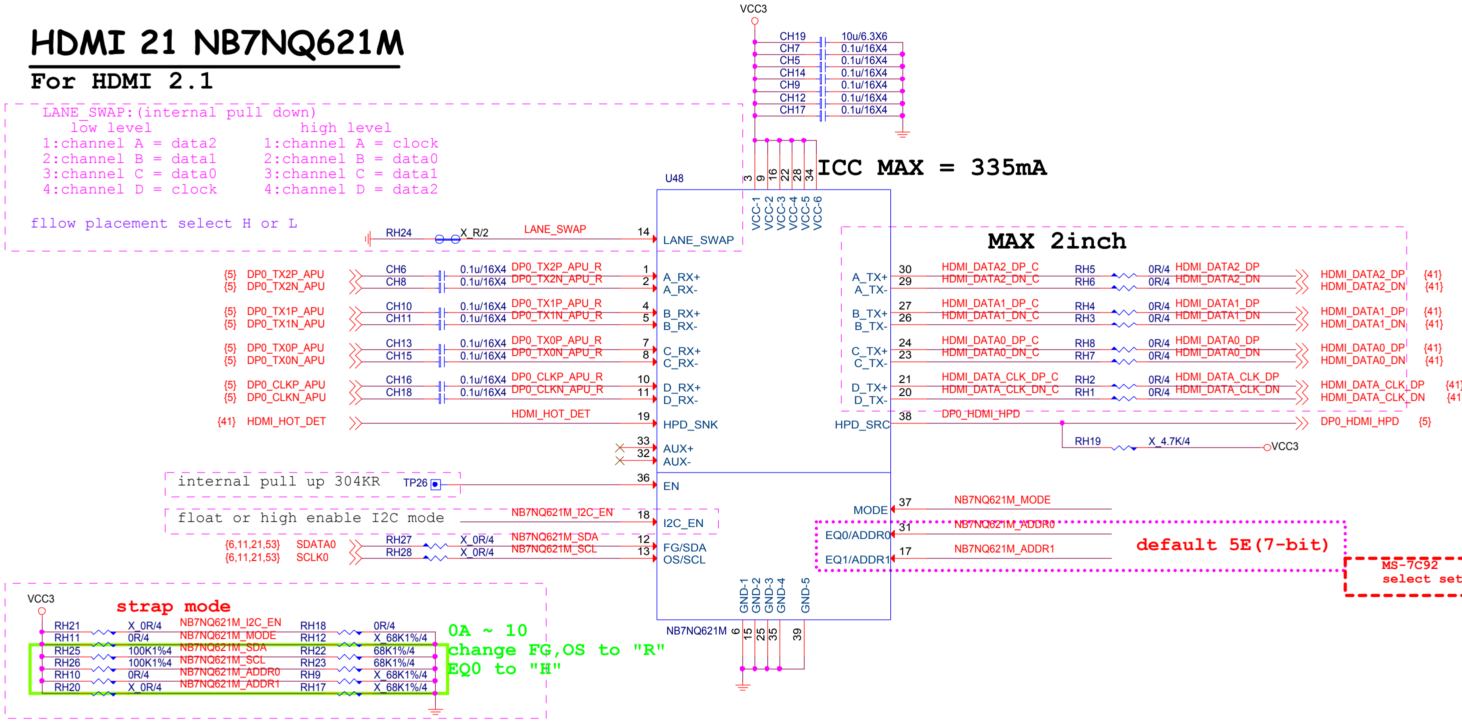
HDMI 21 NB7NQ621M

For HDMI 2.1



Pin Setting	Voltage	Level
mode	3.3	H
EQ0	3.3	H
FG	1.1	R
OS	1.1	R
EQ1	2.2	F
I2C	0	L

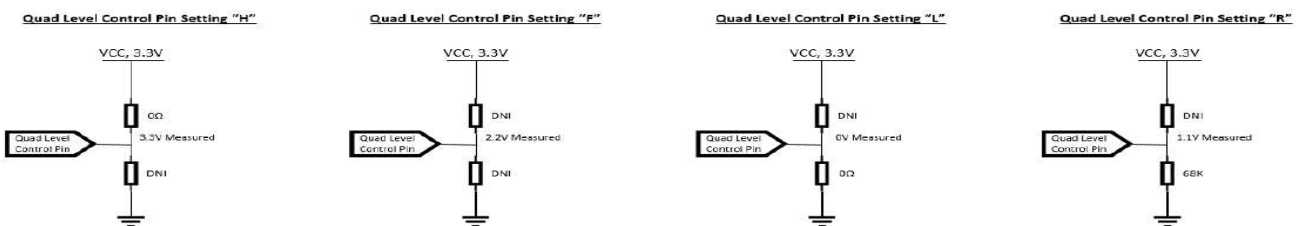


Figure 4. NB7NQ621M Required Implementation for Quad Level Pin Strapping
Pins: EQ0/ADDR0, EQ1/ADDR1, I2C_EN, and MODE

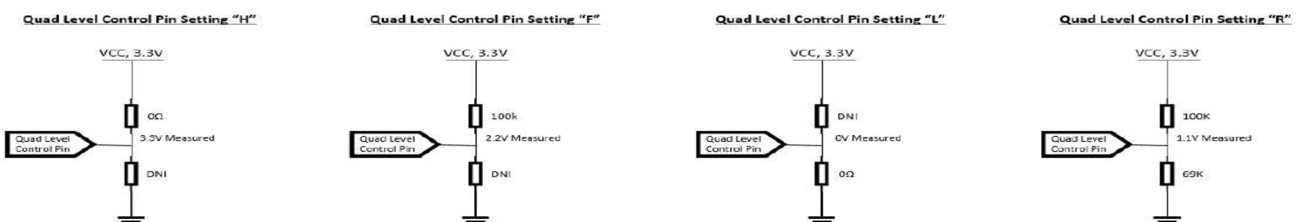


Figure 5. NB7NQ621M Required Implementation for Quad Level Pin Strapping
Pins: FG and OS

Table 9: GPIO Device Slave Address Settings

FOR MSI USE ONLY

Quad-Level Input ADDR1	ADDR0	7 Bit Slave Address							HEX Slave Address: (7-bit)	$\overline{W}$/R	HEX Address: ($\overline{W}$/R=0)	HEX Address: ($\overline{W}$/R=1)
L	L	1	0	1	0	1	0	0	54	0/1	A8	A9
L	R	1	0	1	0	1	0	1	55	0/1	AA	AB
L	F	1	0	1	0	1	1	0	56	0/1	AC	AD
L	H	1	0	1	0	1	1	1	57	0/1	AE	AF
R	L	1	0	1	0	0	0	0	50	0/1	A0	A1
R	R	1	0	1	0	0	0	1	51	0/1	A2	A3
R	F	1	0	1	0	0	1	0	52	0/1	A4	A5
R	H	1	0	1	0	0	1	1	53	0/1	A6	A7
F	L	1	0	1	1	1	0	0	5C	0/1	B8	B9
F	R	1	0	1	1	1	0	1	5D	0/1	BA	BB
F (Default)	**F (Default)**	**1**	**0**	**1**	**1**	**1**	**1**	**0**	**5E**	**0/1**	**BC**	**BD**
F	H	1	0	1	1	1	1	1	5F	0/1	BE	BF
H	L	1	0	1	1	0	0	0	58	0/1	B0	B1
H	R	1	0	1	1	0	0	1	59	0/1	B2	B3
H	F	1	0	1	1	0	1	0	5A	0/1	B4	B5
H	H	1	0	1	1	0	1	1	5B	0/1	B6	B7

Table 14. EQUALIZATION SETTINGS TABLE FOR PIN STRAP MODE 3 (Typical)

Equalization Setting #	EQ1	EQ0	EQ Gain [dB] @ 0.825 GHz	EQ Gain [dB] @ 1.7 GHz	EQ Gain [dB] @ 3 GHz
0	L	L	1.7	3.2	5.7
1	L	R	1.9	3.4	6.1
2	L	F	2.1	3.7	6.6
3	L	H	2.3	4.0	6.9
4	R	L	2.4	4.3	7.5
5	R	R	2.5	4.6	8.3
6	R	F	2.7	4.9	8.8
7	R	H	3.0	5.4	9.4
8	F	L	0.5	1.0	1.9
9	F	R	0.7	1.2	2.3
10 (Default)	F	F	0.9	1.6	2.8
11	F	H	1.0	2.0	3.6
12	H	L	1.2	2.3	4.1
13	H	R	1.3	2.5	4.4
14	H	F	1.4	2.7	4.8
15	H	H	1.6	2.9	5.2

MS-7C92
select setting 11

Table 10. MODE OF OPERATION SETTINGS TABLE FOR PIN STRAPPING

Mode of Operation	I2C_EN	MODE Pin	Standard	Configuration	Termination	Data Rate [Gbps]
0	L	L	HDMI	TMDS (DC Coupled Outputs)	High–Z, line to line	0.25 – 1.65
1	L	R	HDMI	TMDS (DC Coupled Outputs)	300 Ω, line to line	1.65 – 3.4
2	L	F	HDMI	TMDS (DC Coupled Outputs)	200 Ω, line to line	1.65 – 3.4
3	L	H	HDMI	TMDS (DC Coupled Outputs)	100 Ω, line to line	3.4 – 6
4	R	L	HDMI	FRL (DC Coupled Outputs)	100 Ω, line to line	3 – 12
5	R	F	HDMI	FRL (AC Coupled Outputs)	50 Ω to VCC	3 – 12
6	R	H	DisplayPort	ML (AC Coupled Outputs)	50 Ω to VCC	2.7 – 8.1
I^2C	F (Default)/H	X	I^2C is Enabled for these combinations. Pin Strap–Mode is Disabled.			

MS-7C92
select mode3

Table 20. FLAT GAIN, SETTINGS TABLE FOR PIN STRAP MODE 3–6 (Typical)

Setting #	Pin Strap Setting	Flat Gain @ 100 MHz
0 (Default)	L	–0.5 dB
1	R	2.4 dB
2	F	1.1 dB
3	H	4 dB

MS-7C92
setting 1

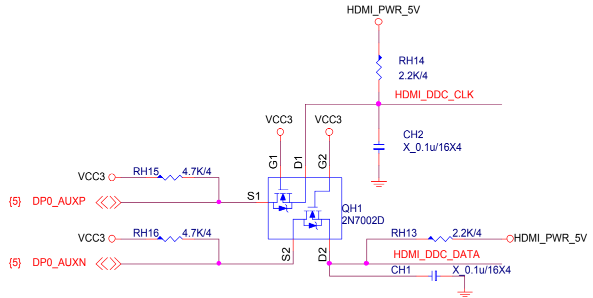
Table 21. OUTPUT SWING, SETTINGS TABLE FOR PIN STRAP MODE (Typical)

Setting #	Pin Strap Setting	Output Swing @ 100 MHz
0 (Default)	L	1000 mV
1	R	1200 mV
2	F	800 mV
3	H	1400 mV

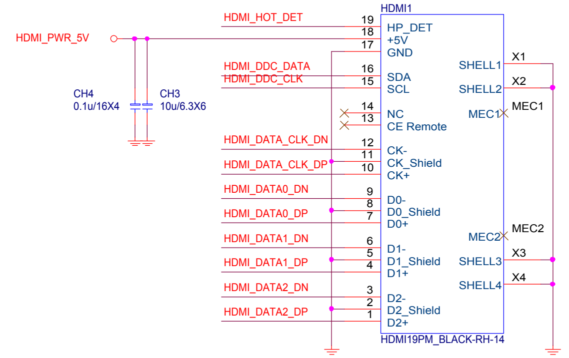
MS-7C92
setting 1

HDMI 2.1 Connector

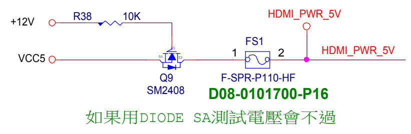
AUX Level Shifter



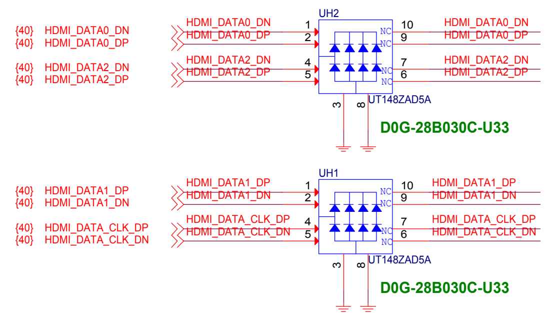
Connector



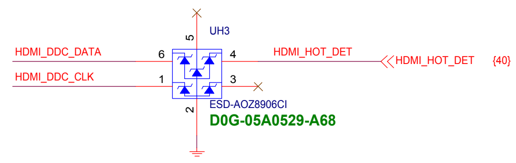
Connector Power



For EMI



注意:耐壓5V零件



MICRO-STAR INT'L CO.,LTD

MS-7C92

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Custom	HDMI 21 Connector	12

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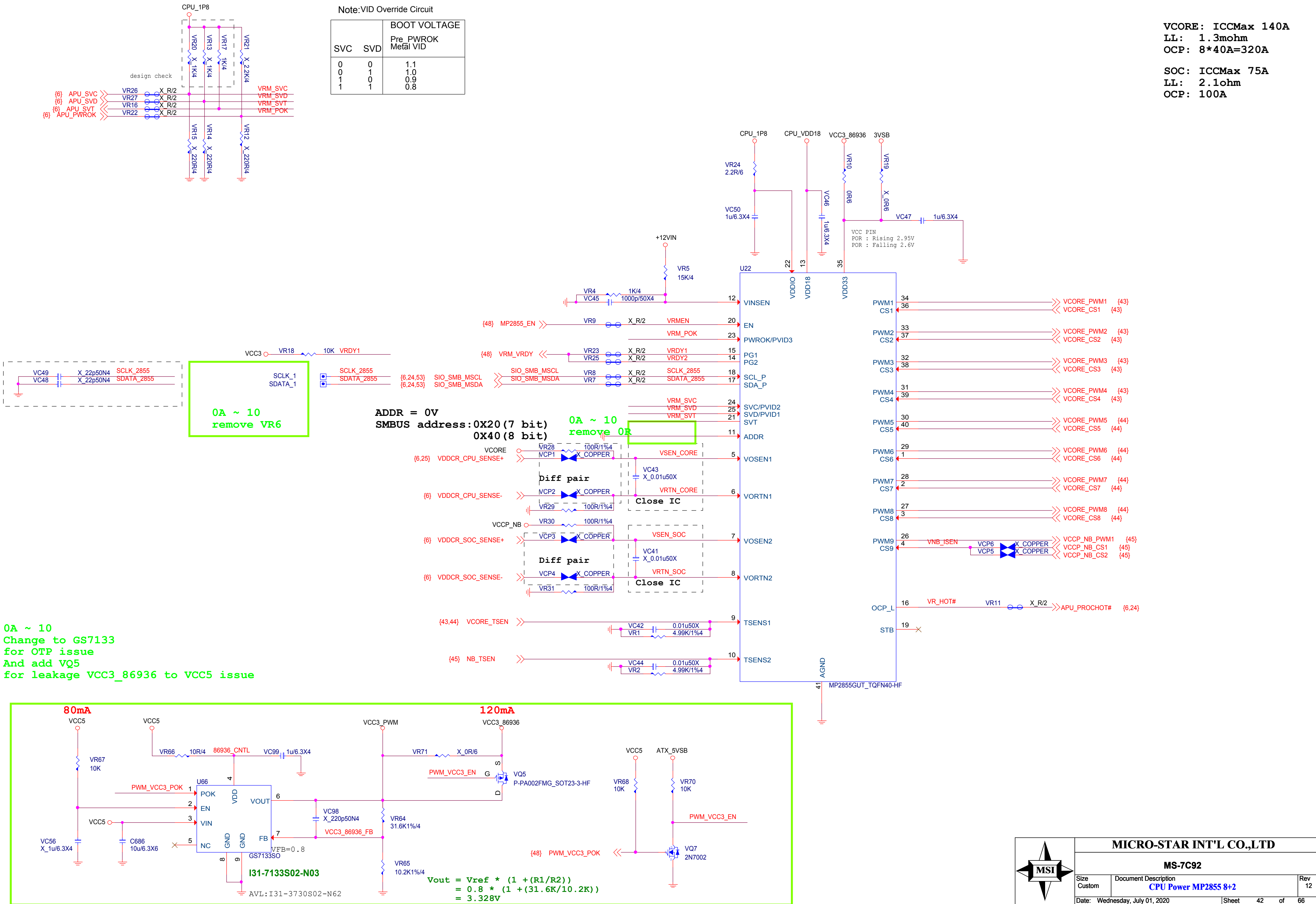

Note:VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VCORE: ICCMax 140A
LL: 1.3mohm
OCP: 8*40A=320A

SOC: ICCMax 75A
LL: 2.1ohm
OCP: 100A

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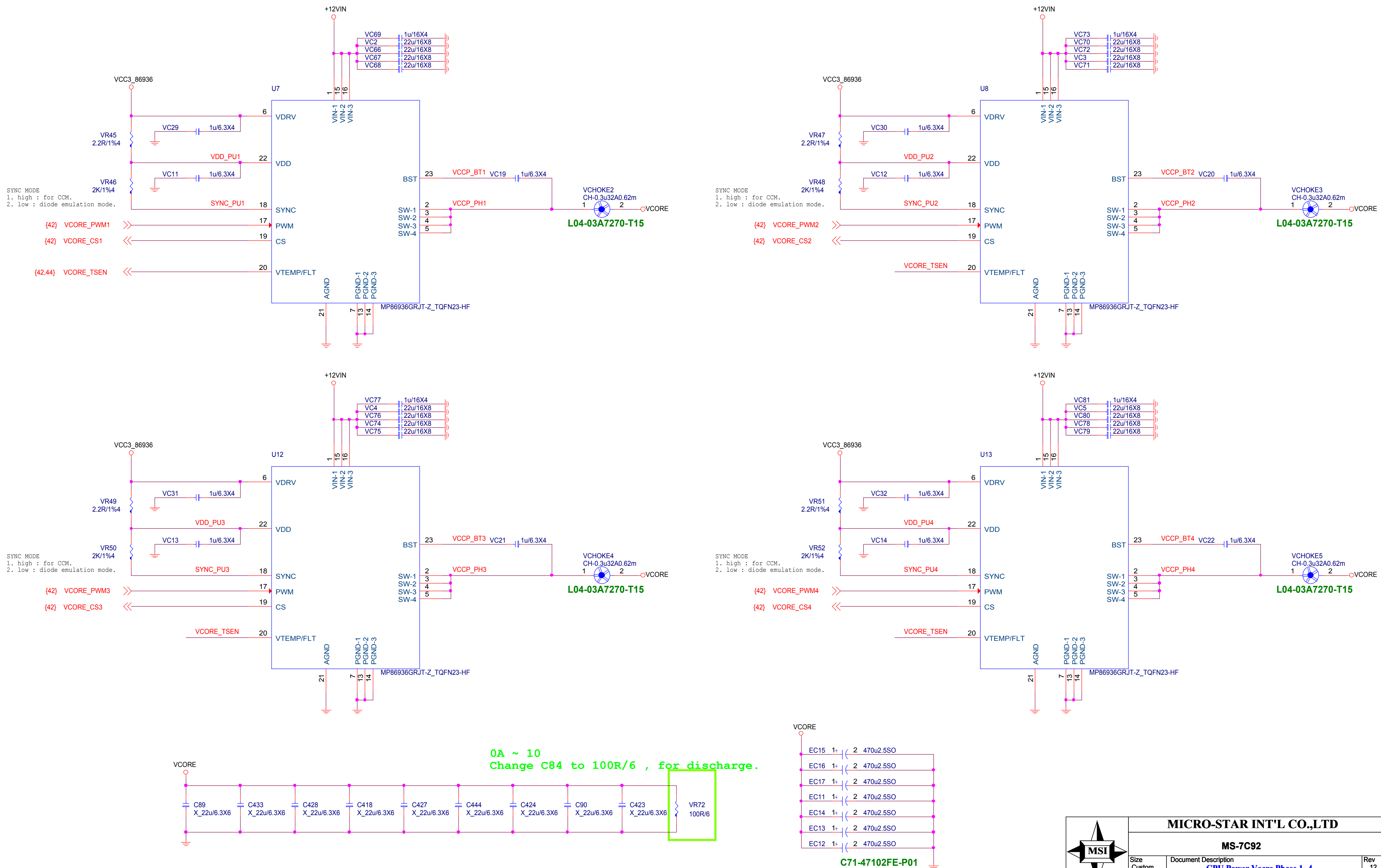
Vcore EDC Max 140A



MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: CPU Power Vocre Phase 1- 4	Rev: 12
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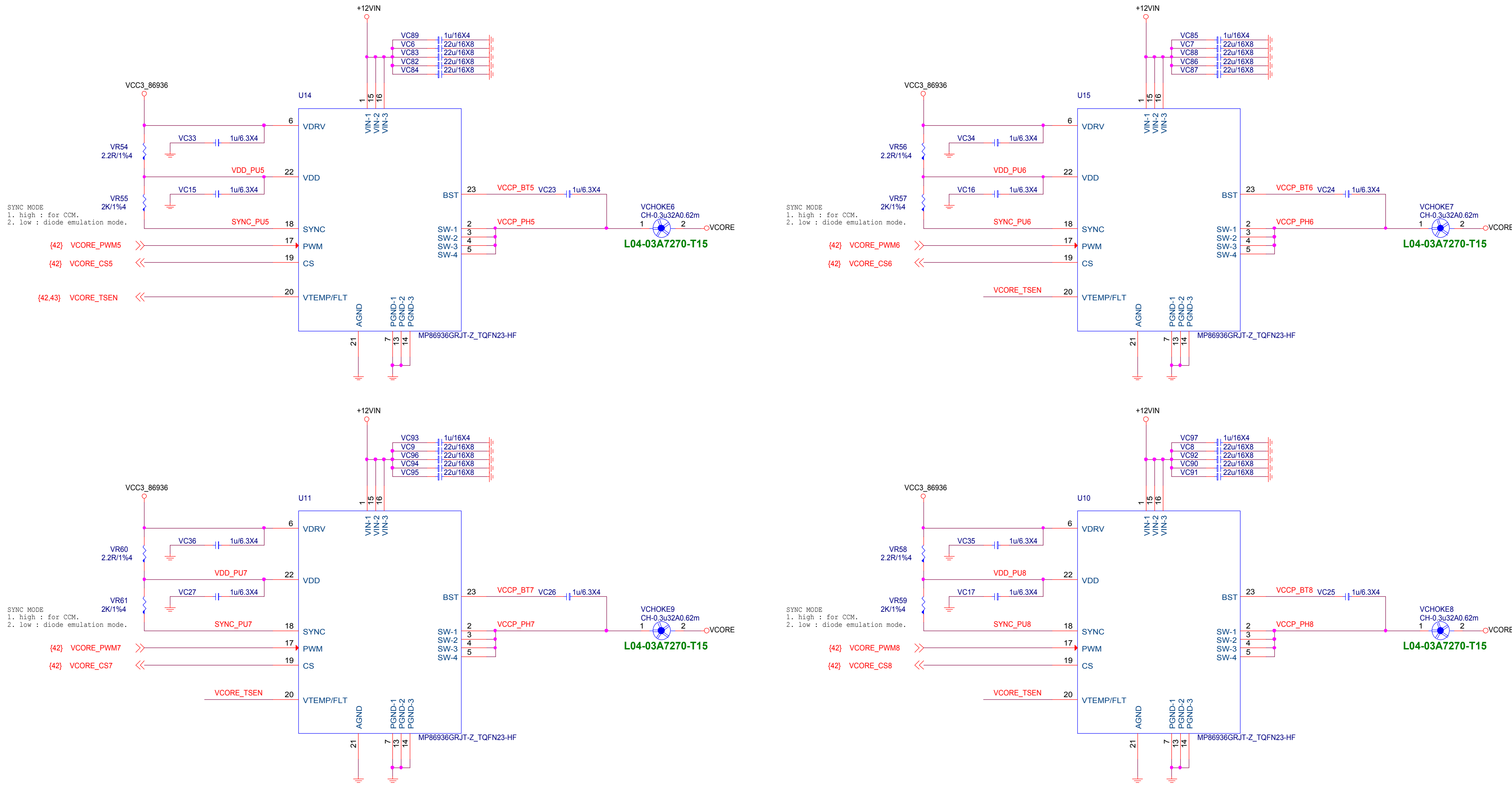
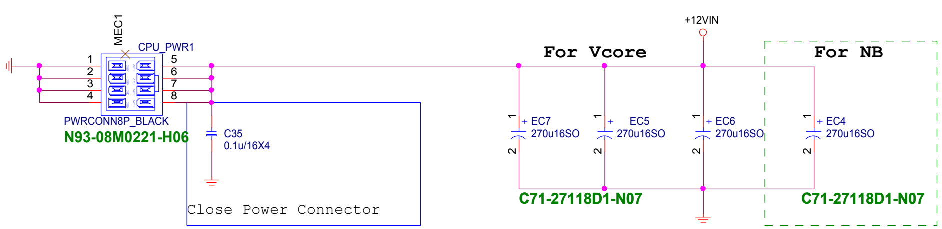


CPU POWER CONNECTOR



MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: CPU Power Vcore Phase 5 - 8	Rev: 12
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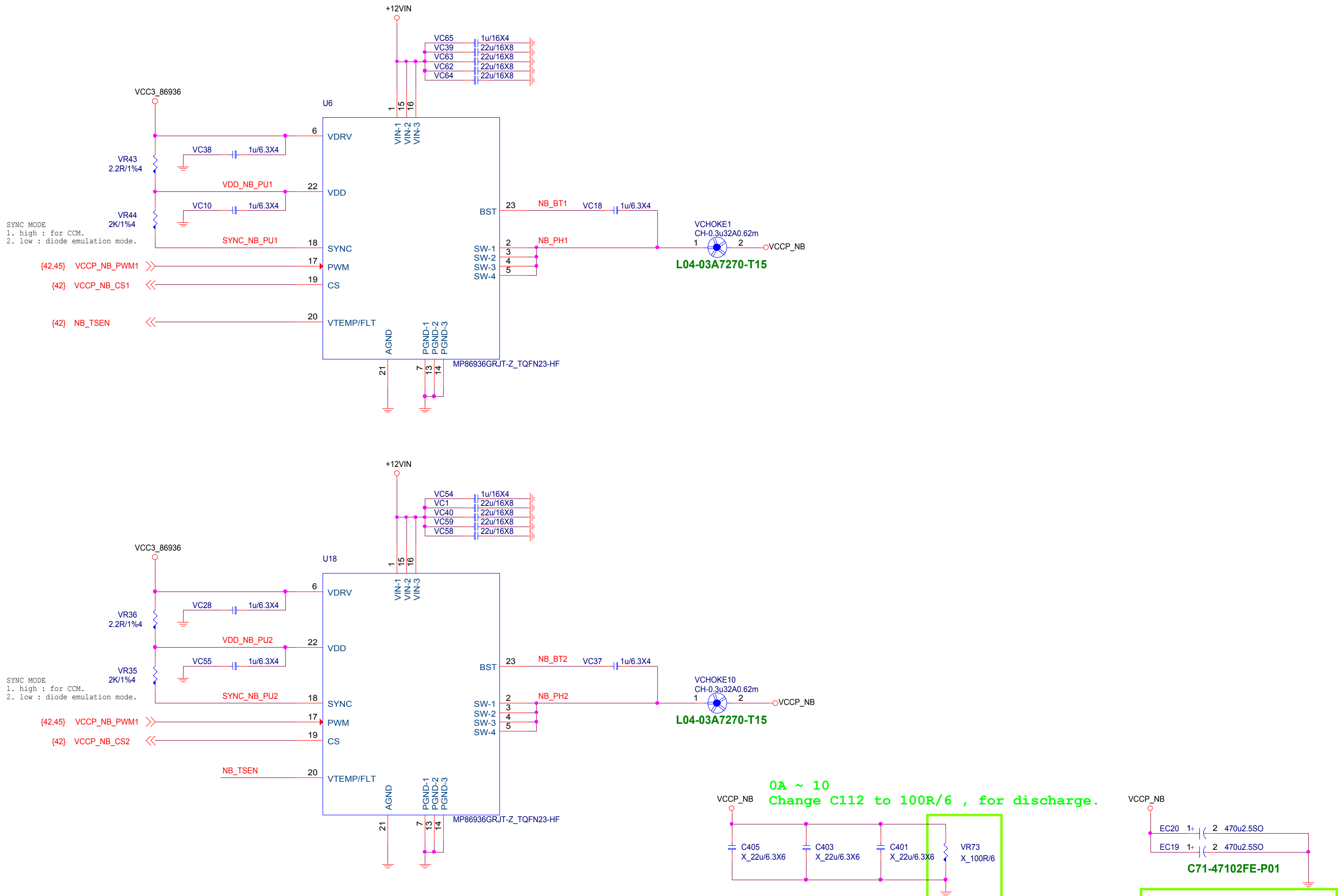
SOC EDC Max 75A



0A ~ 10
Change C112 to 100R/6 , for discharge.

0A ~ 10 remove EC21

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Size	Document Description	Rev
Custom	CPU Power NB Phase 1-2	12

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CPU 1.8V S5

Fix CCM

CPU 1.8V_S5@0.5A
CPU_VDDP_S5@1A
AUDIO1.8V@0.25A
For VCCP_NB_S5 @0.9A

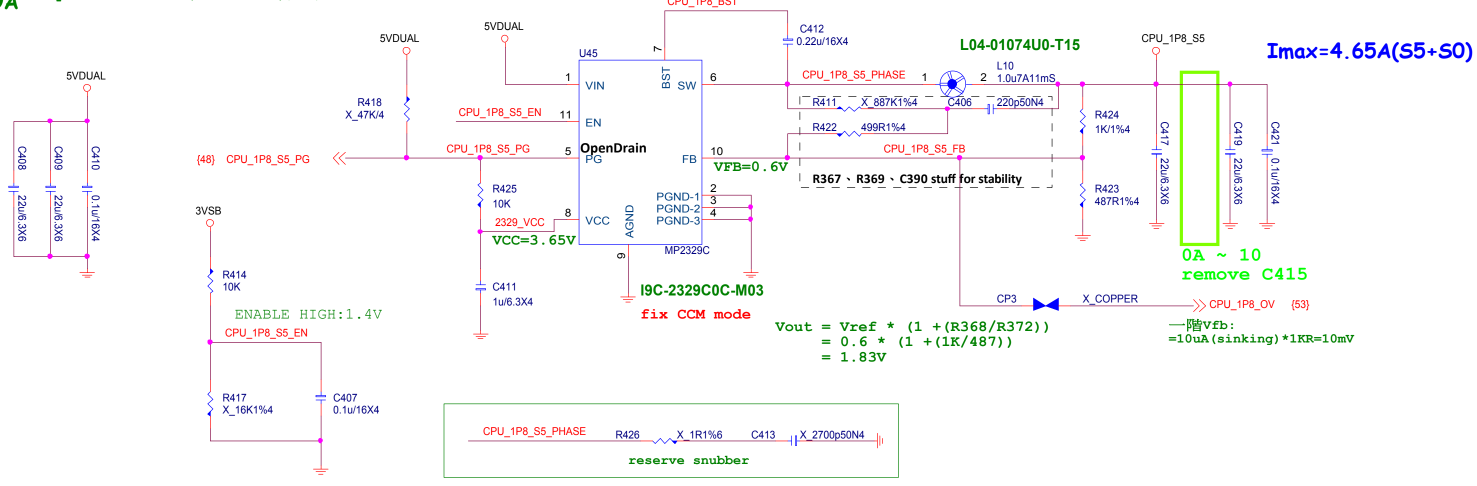
Input Current = (6.5A*1.8V)/5V/0.8 = 3A

Continuous Conduction Mode (CCM)

CPU_1P8_BST、CPU_1P8_BST_R >50 mils.

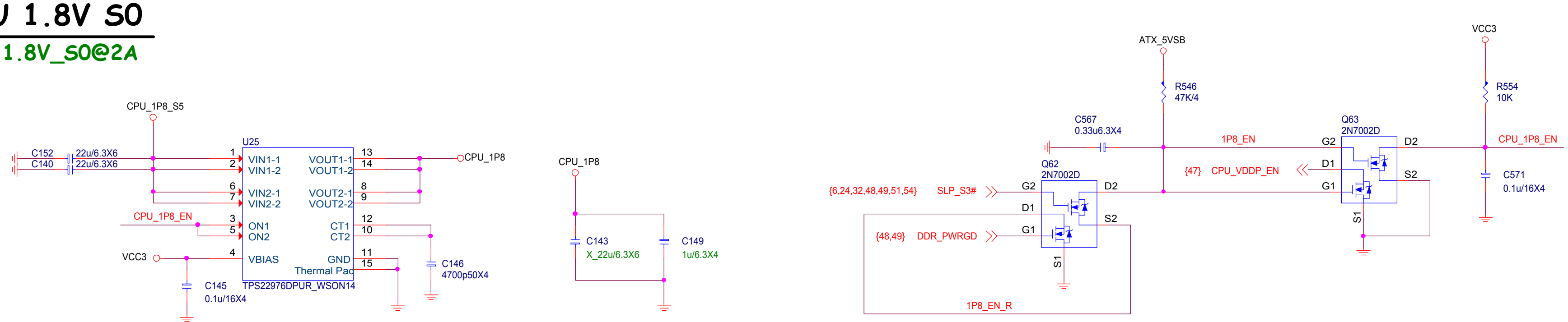
OCP = 6.5A

Imax=4.65A(S5+S0)

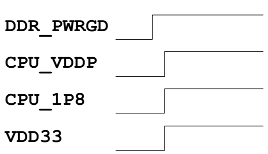


CPU 1.8V S0

CPU 1.8V_S0@2A



Adjustable Rise Time
SR = 0.42*CT+66
SR is the slew rate in (μs/V)
CT is constant value on CT pin (in pF)
The units for the constant 66 is in (μs/V)



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MS-7C92		
Size: Custom	Document Description: CPU Power 1.8_S0 / S5	Rev: 12
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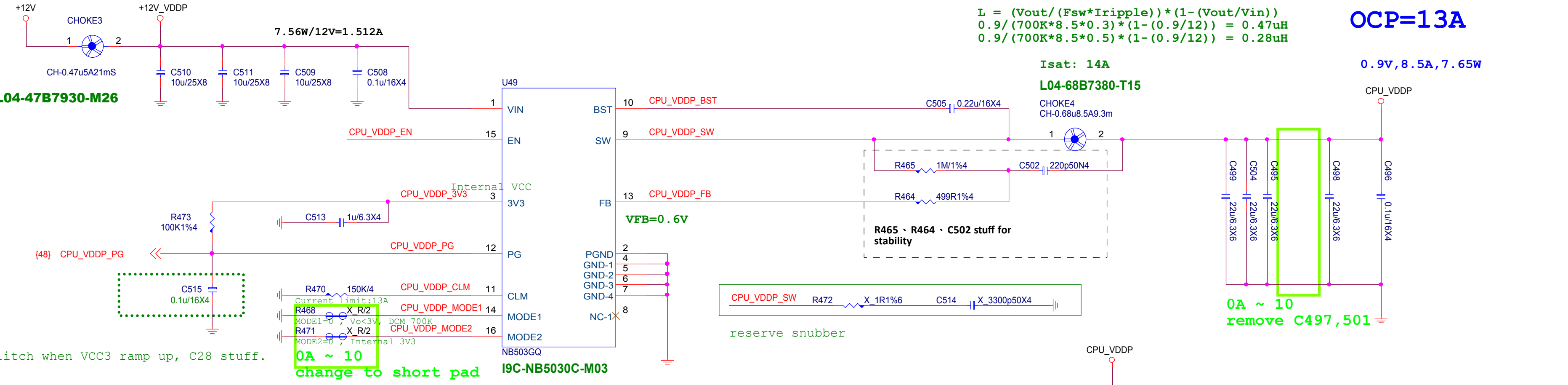
CPU_VDDP_S0

0.9V@S0:8.5A

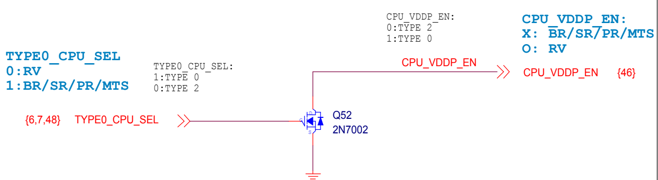
Input Current = (13A*0.9V)/12V/0.8 = 1.22A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=13*SQRT((0.9/12)*(1-(0.9/12))) = 3.42A
Choke Irms =5 A

L = (Vout/(Fsw*Iripple))*(1-(Vout/Vin))
0.9/(700K*8.5*0.3)*(1-(0.9/12)) = 0.47uH
0.9/(700K*8.5*0.5)*(1-(0.9/12)) = 0.28uH

OCP=13A

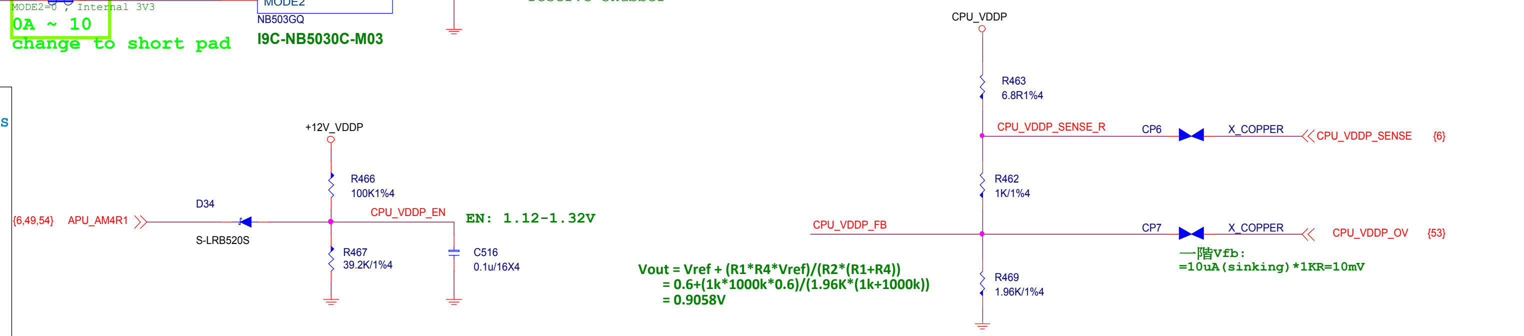


TYPE0_CPU_SEL
0:RV
1:BR/SR/PR/MTS



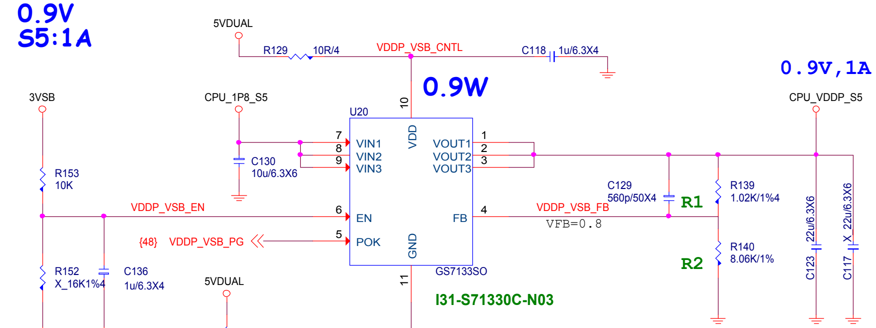
CPU_VDDP_EN:
X: BR/SR/PR/MTS
O: RV

CPU	TYPE	TYPE0_CPU_SEL	TYPE1_CPU_SEL	CPU_VDDP_EN
BR	~~0~~	~~1~~	~~0~~	~~1~~ SPEC no Support
NA	X	0	0	0
SR	2	1	CPU VDDP NOT SUPPORT TYPE2	0
RV/ZP	3	0	1	1
MTS	4	1	CPU VDDP NOT SUPPORT TYPE4/6	



CPU_VDDP_S5

0.9V
S5:1A



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(1.02K/8.06K))
= 0.9V

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Size: Custom	Document Description: CPU Power VDDP-NB503	Rev: 12
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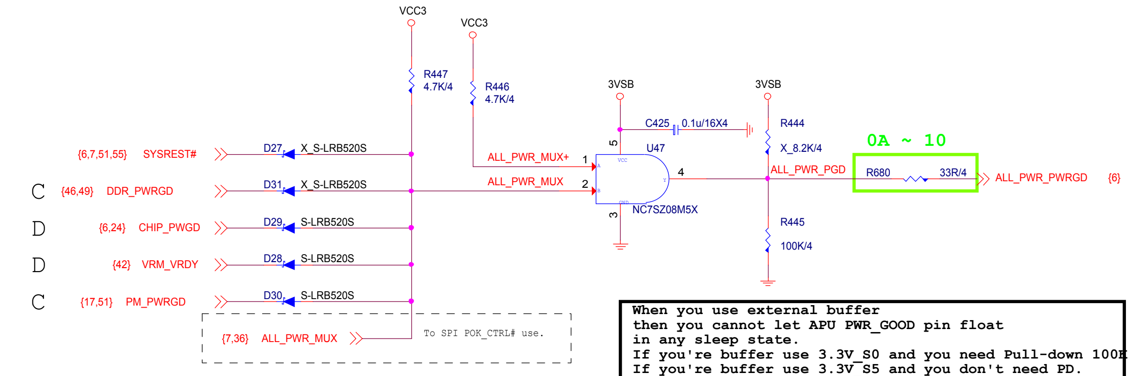
ALL POWER GOOD MUX

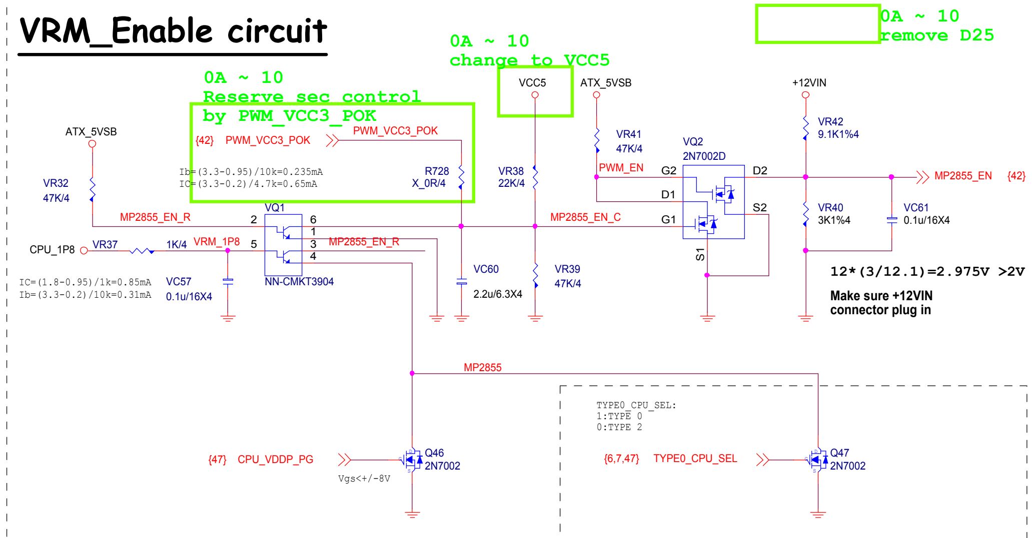
S0 PG

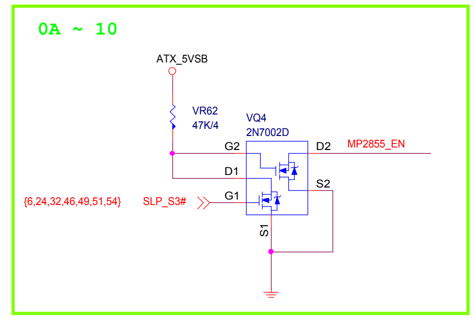


When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

For other PWR_GOOD keep High use

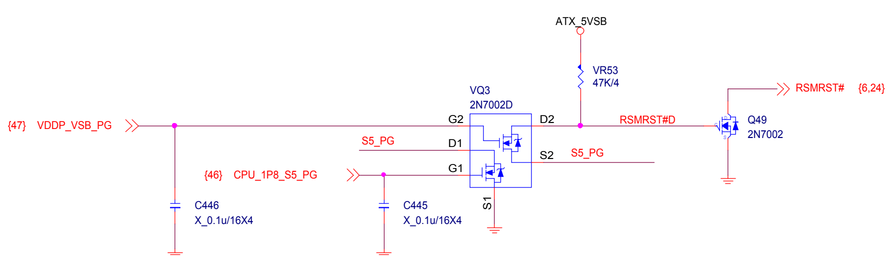
VRM_Enable circuit





CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
~~BR~~	~~0~~	~~0~~ SPEC no Support	~~1~~
NA	X	0	0
SR	2 CPU VDDP NOT SUPPORT TYPE2	1	1
RV/ZP	3	1	0
MTS	4 CPU VDDP NOT SUPPORT TYPE4	1	1

S5 PG



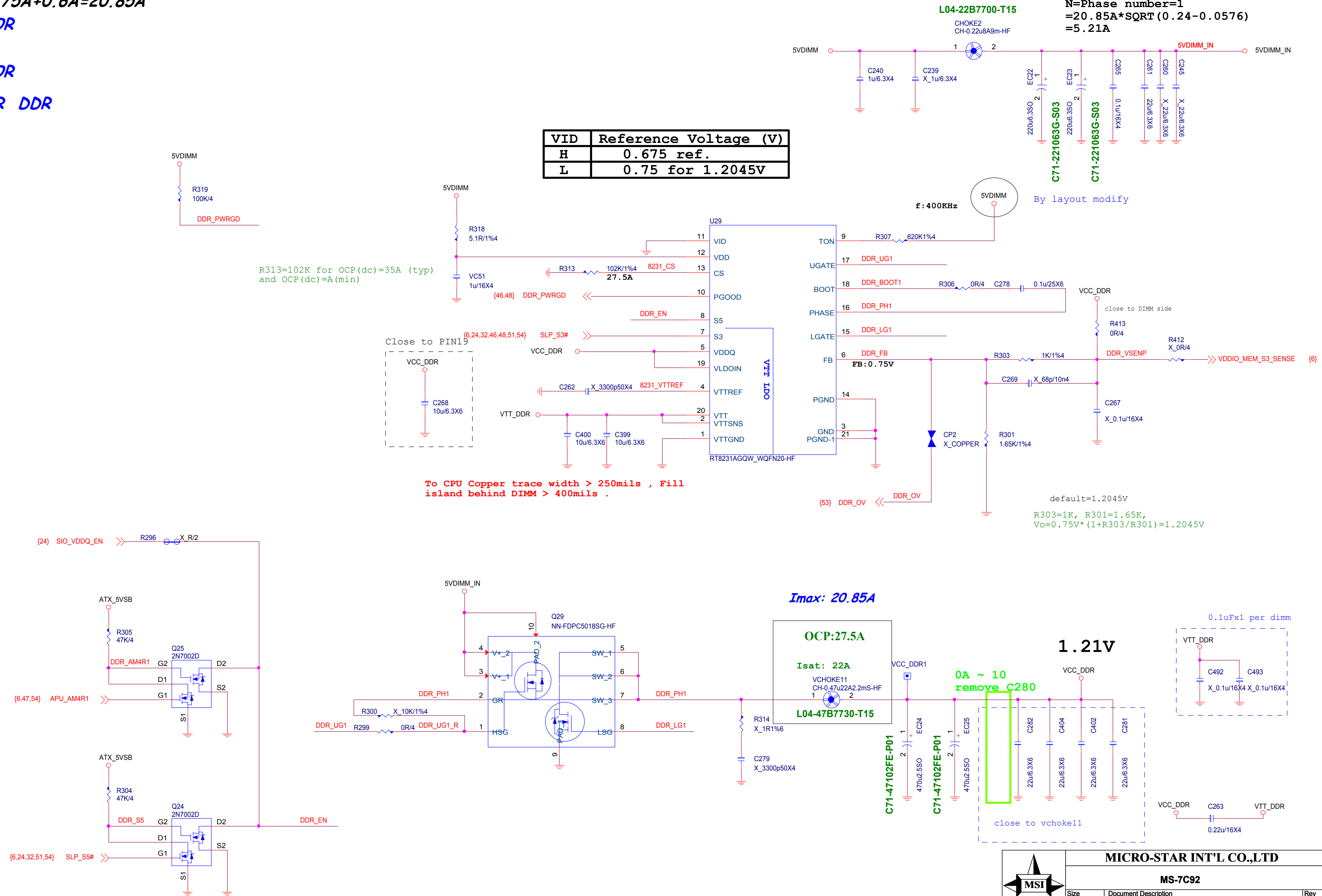
DDR4_1.2V
15.5A+4.75A+0.6A=20.85A

15.5A FOR CPU

4.75A FOR 2DIMM
0.6A FOR DDR VTT

Irms = Iout * SQRT{D/N- (D)^2]}
VCCDDR:
D=Vout/Vin=1.2/5=0.24
N=Phase number=1
=20.85A*SQRT(0.24-0.0576)
=5.21A

VID	Reference Voltage (V)
H	0.675 ref.
L	0.75 for 1.2045V



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Custom	DDR PWR - RT8231A	12

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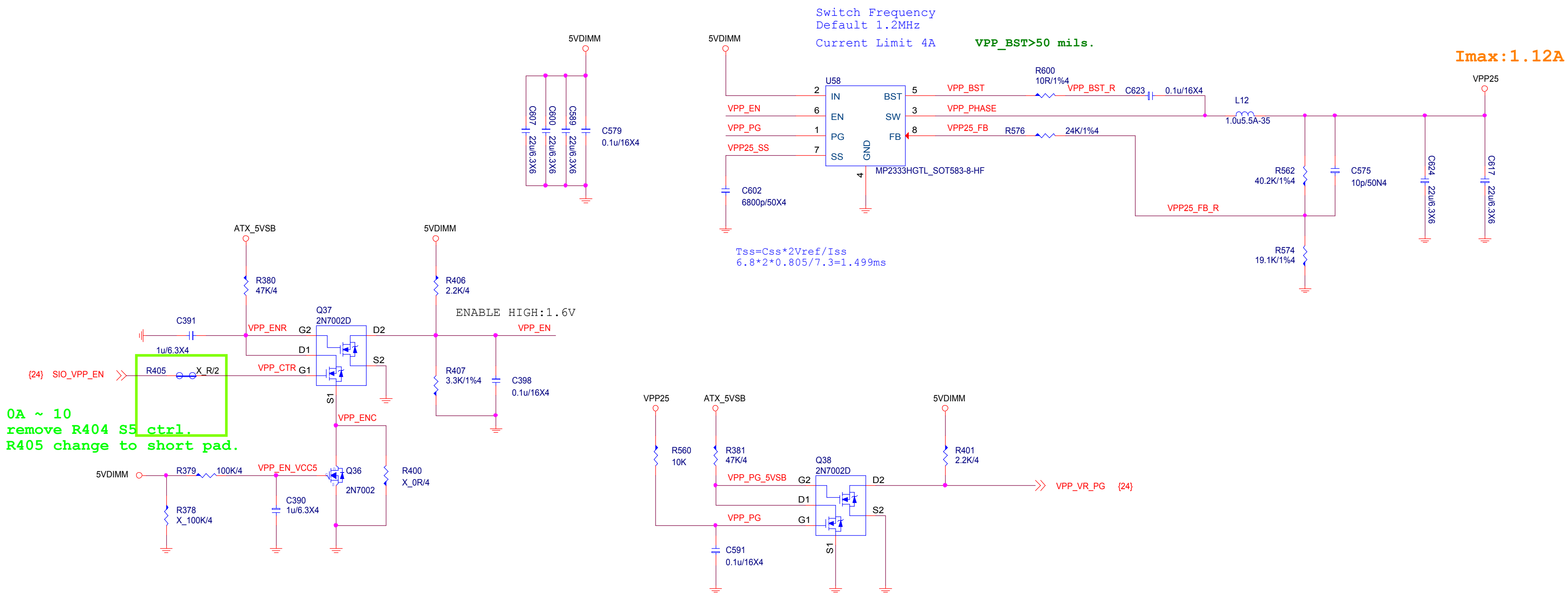
4DIMM : VPP25

2.5V@1.12A



MICRO-STAR INT'L CO.,LTD		
MS-7C92		
Size: Custom	Document Description: DDR PWR-MP2333HGTL-VPP25	Rev: 12
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FOR Promontory 1.05V_S0

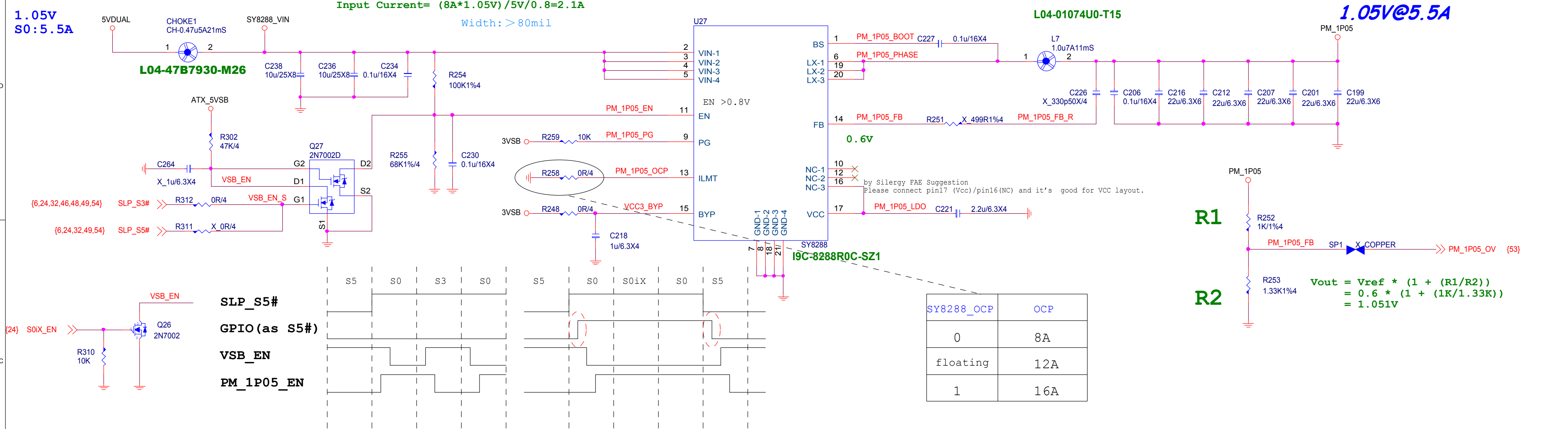
1.05V
S0:5.5A

Input Current= (8A*1.05V)/5V/0.8=2.1A

Isat: 12A

OCP=8A

1.05V@5.5A

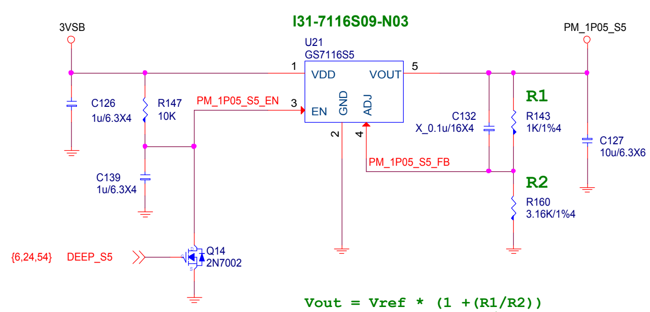


SY8288_OCP	OCP
0	8A
floating	12A
1	16A

Vout = Vref * (1 + (R1/R2))
= 0.6 * (1 + (1K/1.33K))
= 1.051V

FOR PROM PM_1P05_S5

1.05V@0.05A

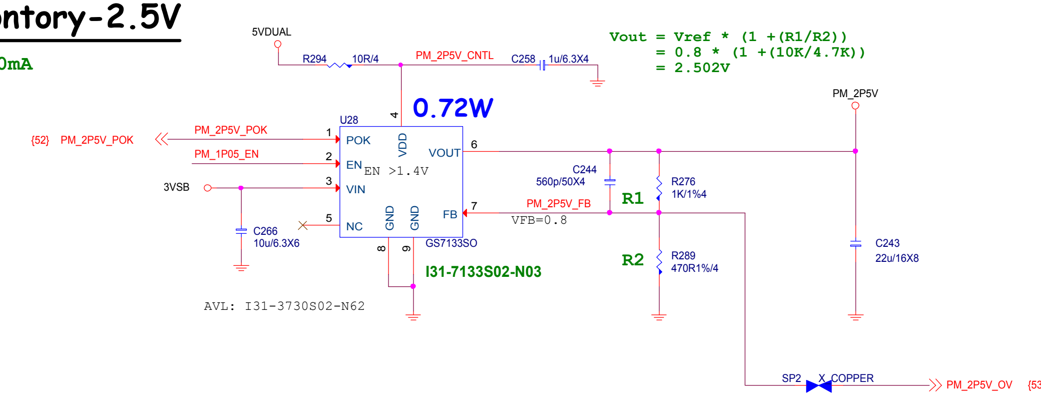


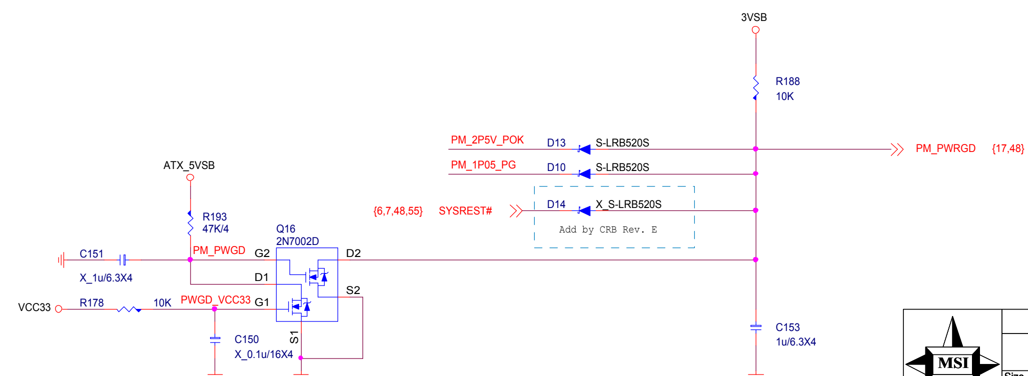
Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(1K/3.16K))
= 1.05V

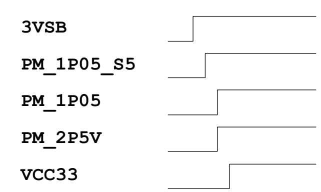
Promontory-2.5V

2.5V@900mA

Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/4.7K))
= 2.502V







MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	PM - SY8288/PM_1P05/PM_2P5V	12

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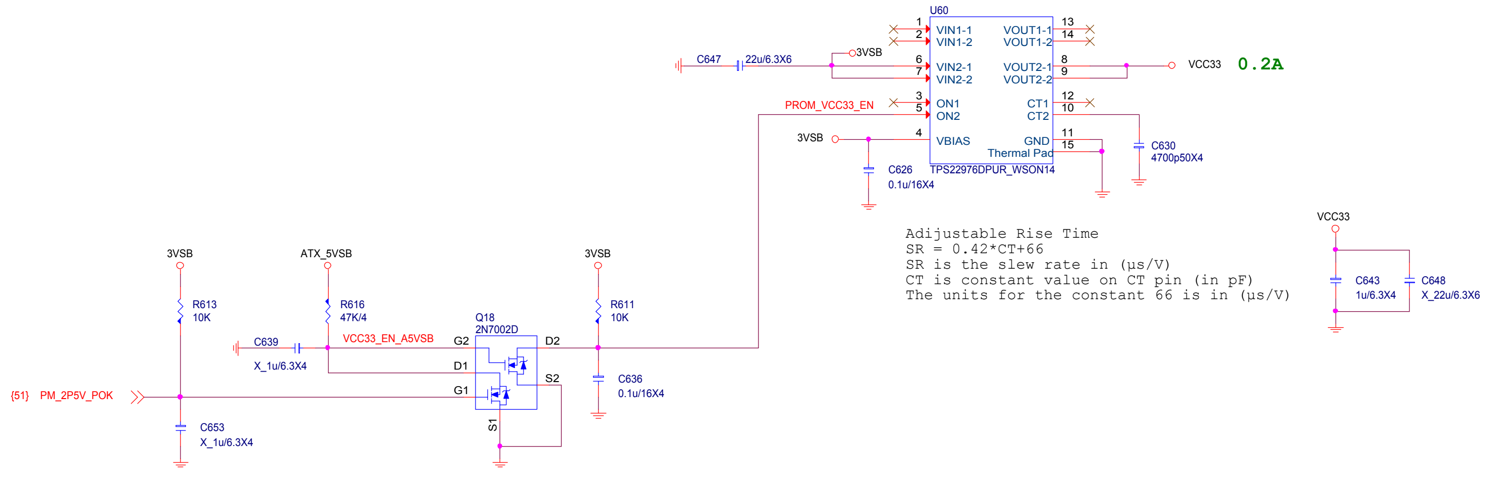
PROM VCC33

VCC33@0.2A



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Size: Custom	Document Description: PM -TPS22976DPUR_VCC33	Rev: 12
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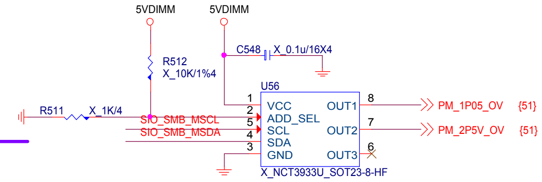
Over Voltage Control IC

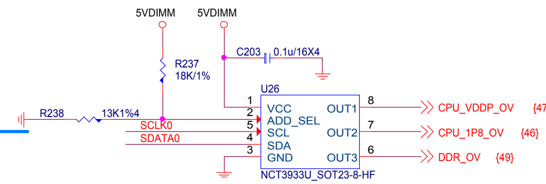
UPI VOLTAGE CONSOLE

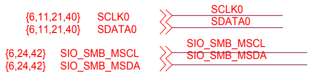
ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

0x20:RH=10K,RL=OPEN

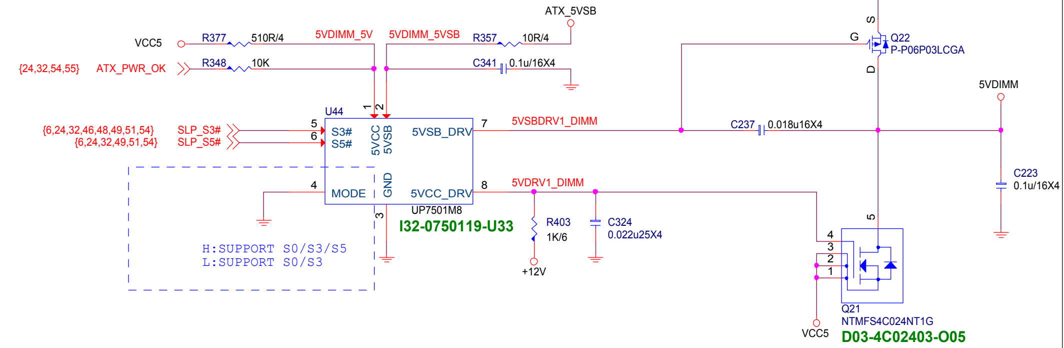


0x26:RH=18K,RL=13K



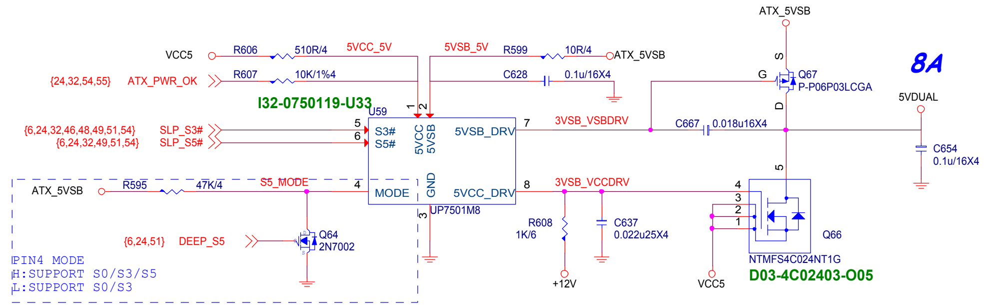


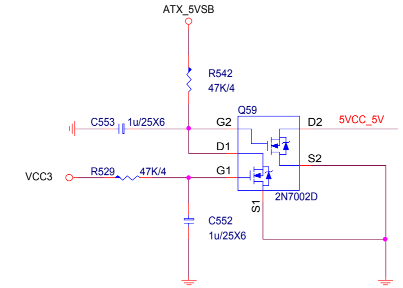
5VDIMM FOR DDR



5VDUAL For 3VSB/CPU1.8V/VDDP

LDOVDD=93.6mA
CPU_1P8_S5 VIN=3A
PM_1P05 VIN=1.44A
3VSB =3 A



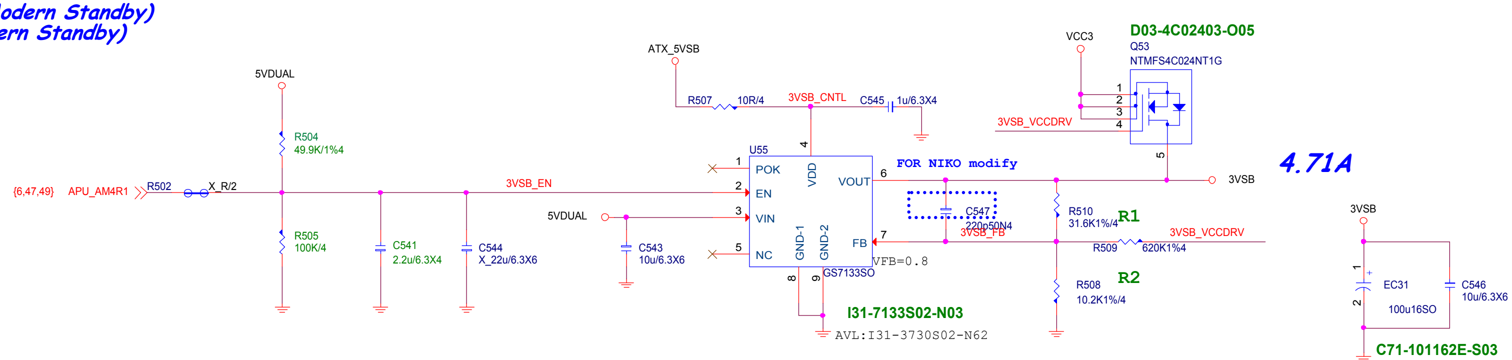


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

3VSB cost down

3.3V@4.71A

CPU:VDD_33_S5=0.25A
CHIP:VDD_33_S5=0.1A
PCIE=(375mA*6)=2.25A
M.2WIFI= 0.78A
LAN=0.18A
PM_1P05_S5 :0.05A
PM_2P5V :0.9A(Modern Standby)
VCC33 :0.2A(Modern Standby)



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(31.6K/10.2K))
= 3.328V

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Size: Custom	Document Description: ACPI - 3VSB / 5VDIMM		Rev: 12
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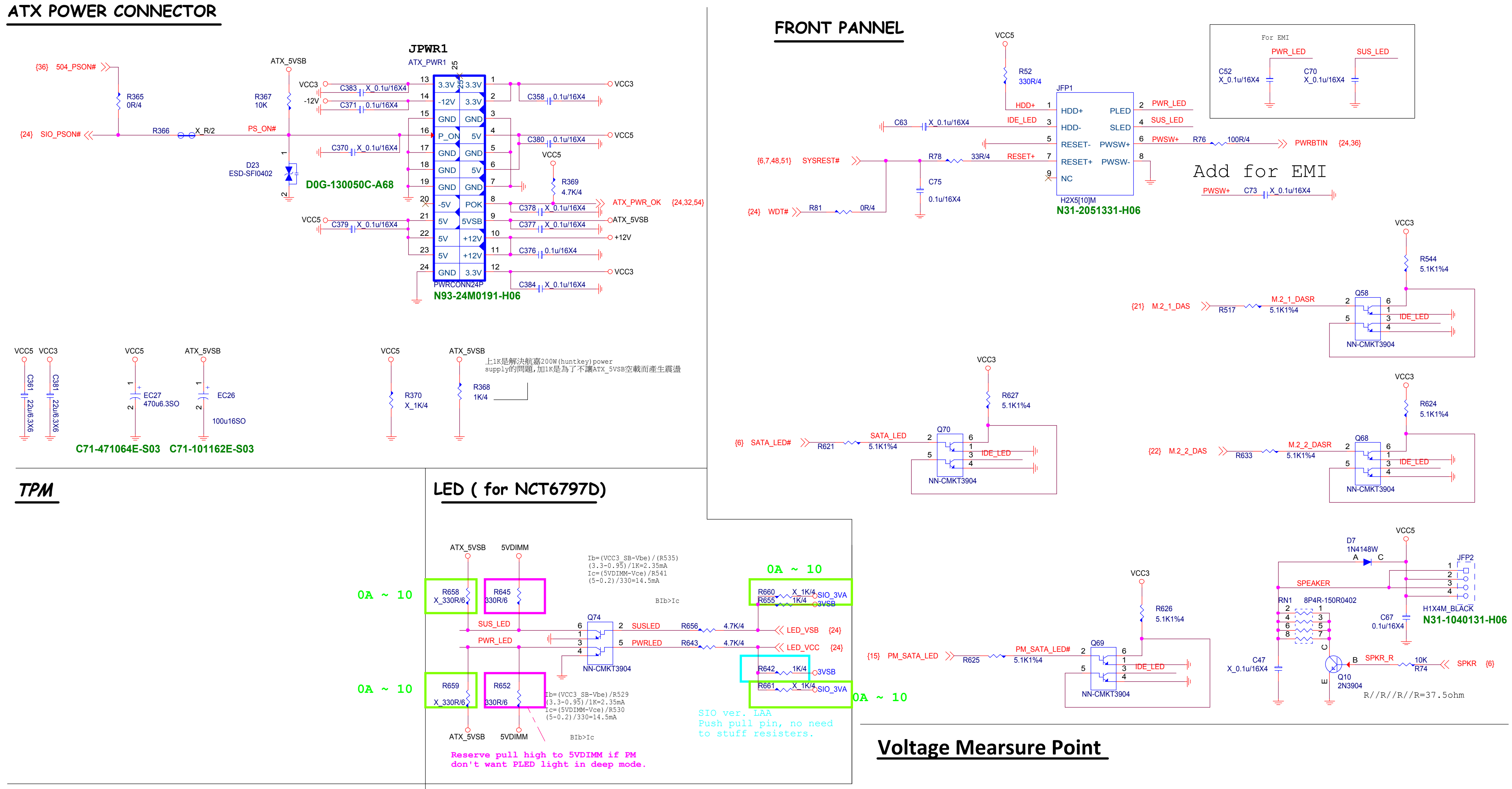

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Custom	ATX Power - FrontPanel / EMI	12

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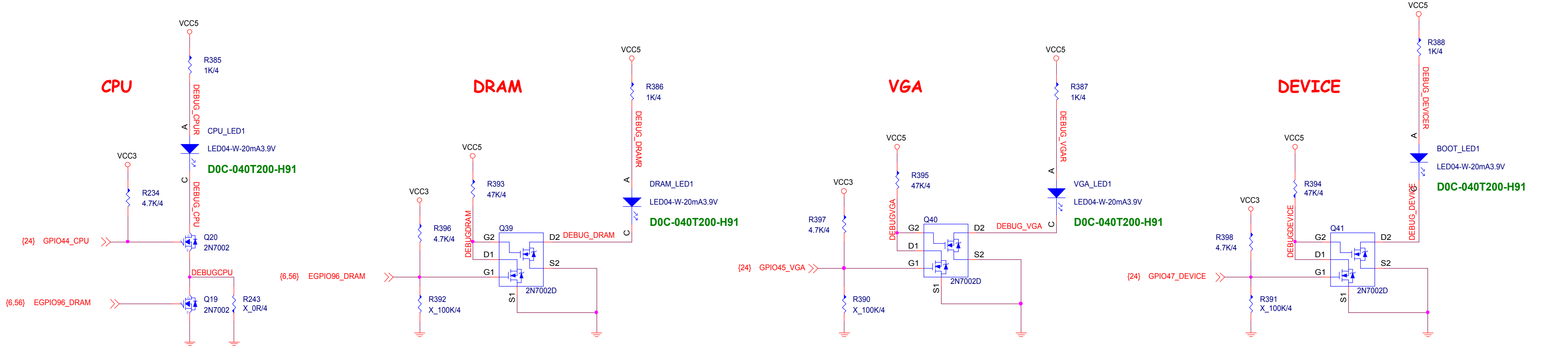
EZ Debug LED

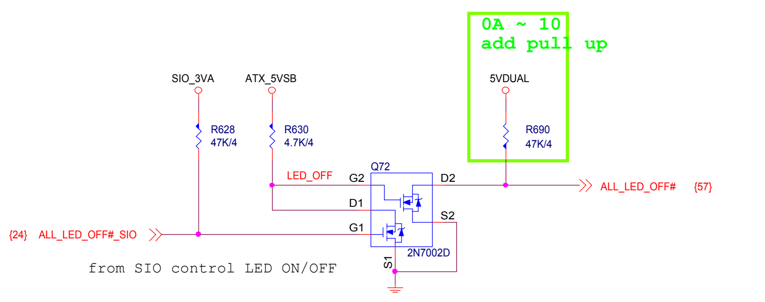


LED\GPIO	GPIO44_CPU	EGPIO96_DRAM	GPIO45_VGA	GPIO47_DEVICE
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

LED亮燈時同時將CPU LED關掉

ALL LED OFF

FORM SIO



from SIO control LED ON/OFF

AMD AMP Detect LED

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MS-7C92
Size: Custom
Document Description: LED - EZ DEBUG / AMP
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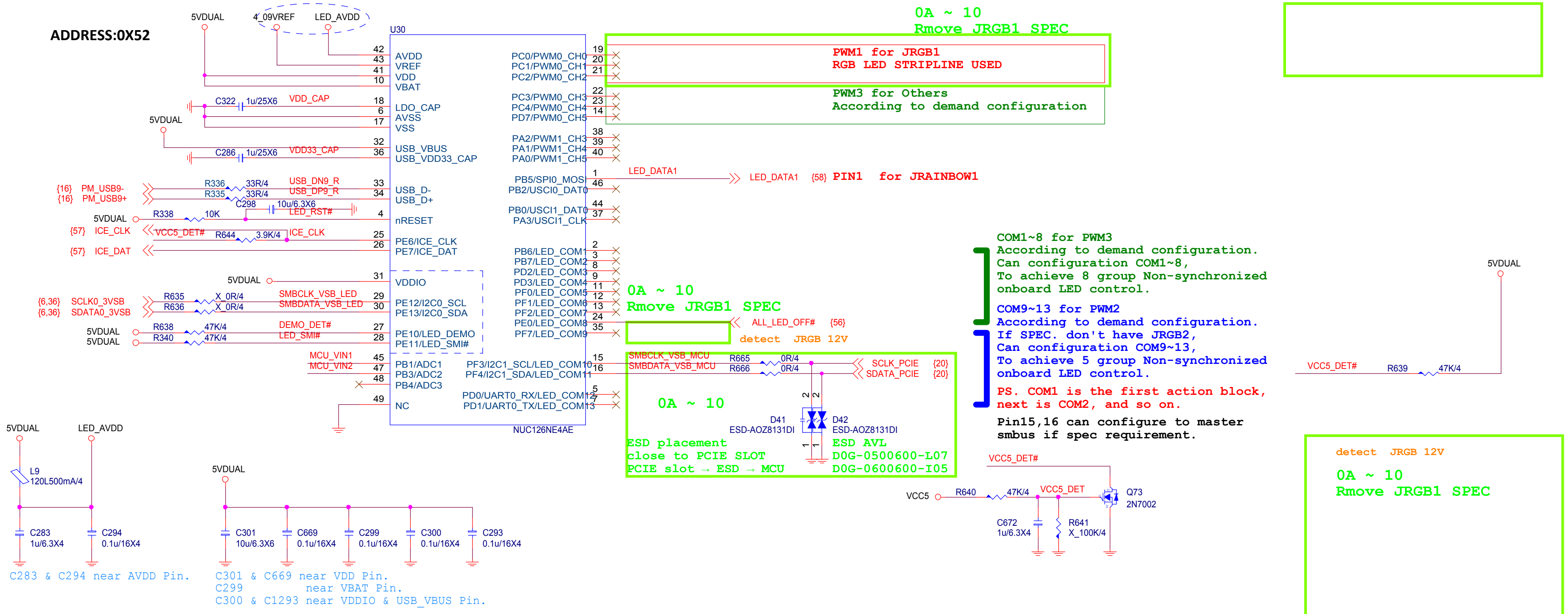
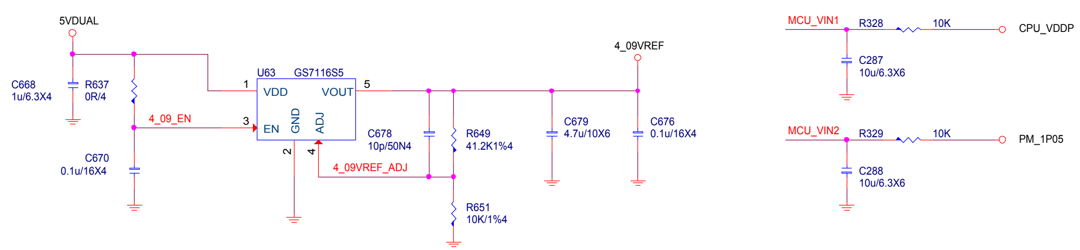
48 PIN LED MCU

If you use ADC function,need to separate VREF from AVDD and 4_09VREF stuff for VREF.

ADDRESS:0X52

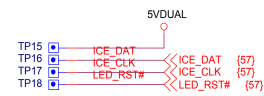


HW Reset MCU



Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~13	PWM2

JT1 for FW update



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Custom	MCU - LED Control	12

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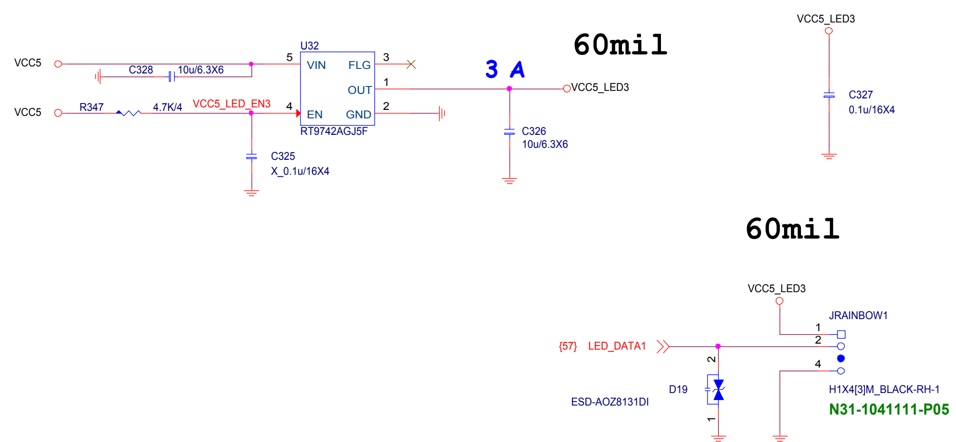
JRGB1

0A ~ 10
Rmove JRGB1 SPEC

JRAINBOW1



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C92	
Size: Custom	Document Description: LED - JRGB1_JRANBOW1	Rev: 12
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MS-7C92		
Size Custom	Document Description **BOM Option**	Rev 12
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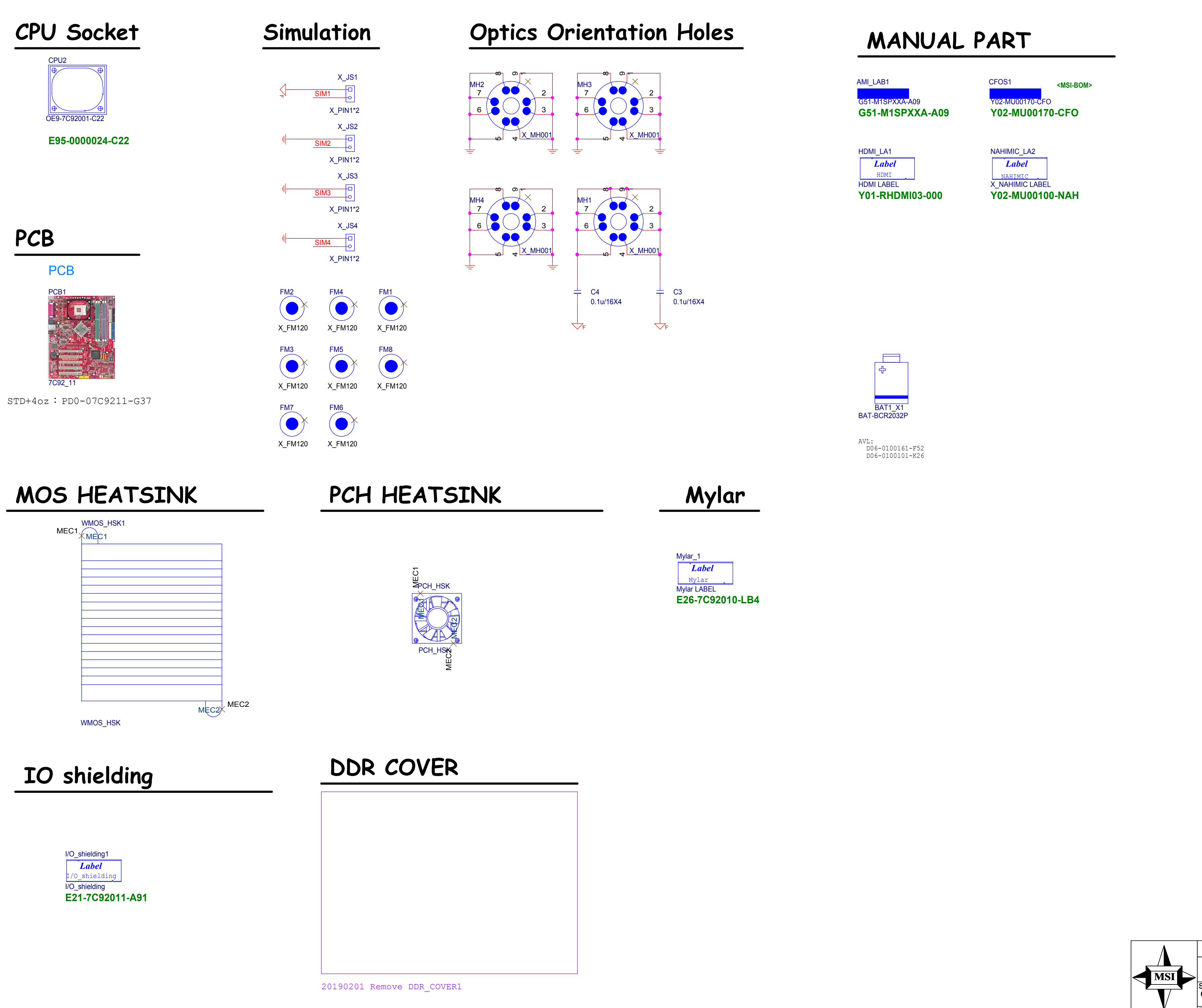

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MS-7C92

Size	Document Description	Rev
Custom	Manual Parts	12

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