AMD AM4

MICRO-STAR INT'L CO.,LTD

MS-7C92

Size: Custom | Document Description: Cover Sheet | Rev: 11

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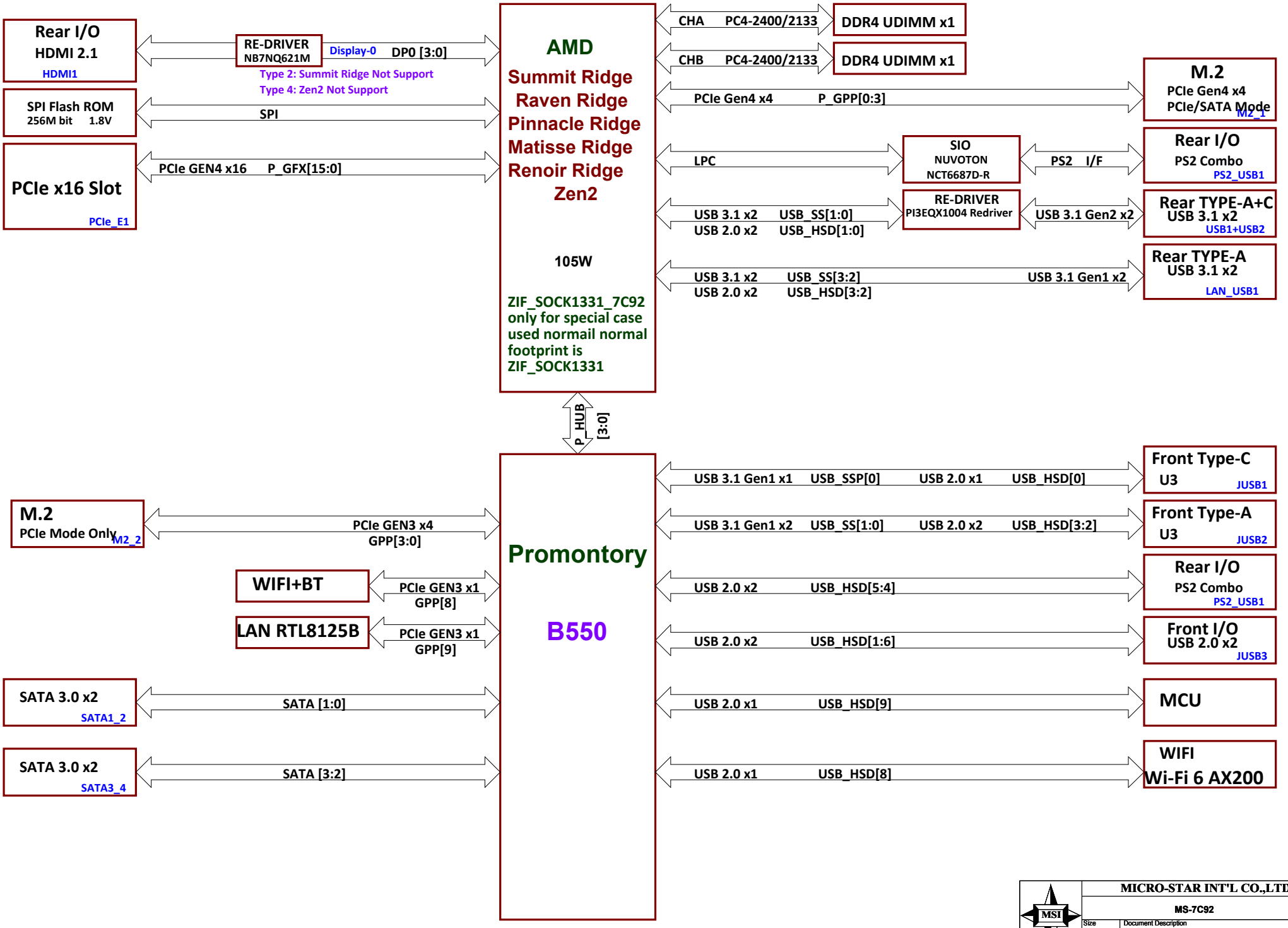

MICRO-STAR INT'L CO.,LTD

MS-7C92

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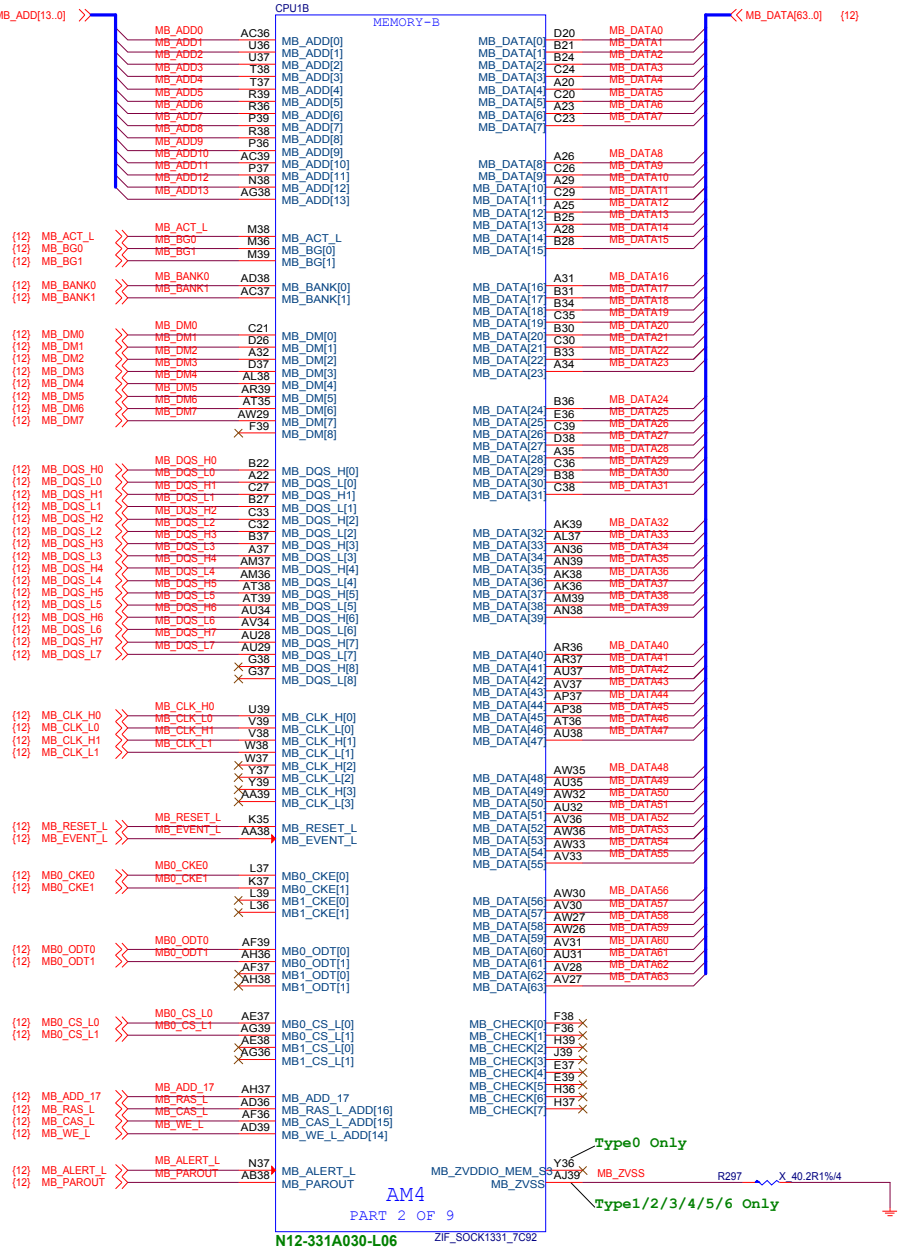
ZIF_SOCK1331_7C92 only for special case used
normal footprint is ZIF_SOCK1331



ZIF_SOCK1331_7C92 only for special case used
normal footprint is ZIF_SOCK1331

MICRO-STAR INT'L CO.,LTD

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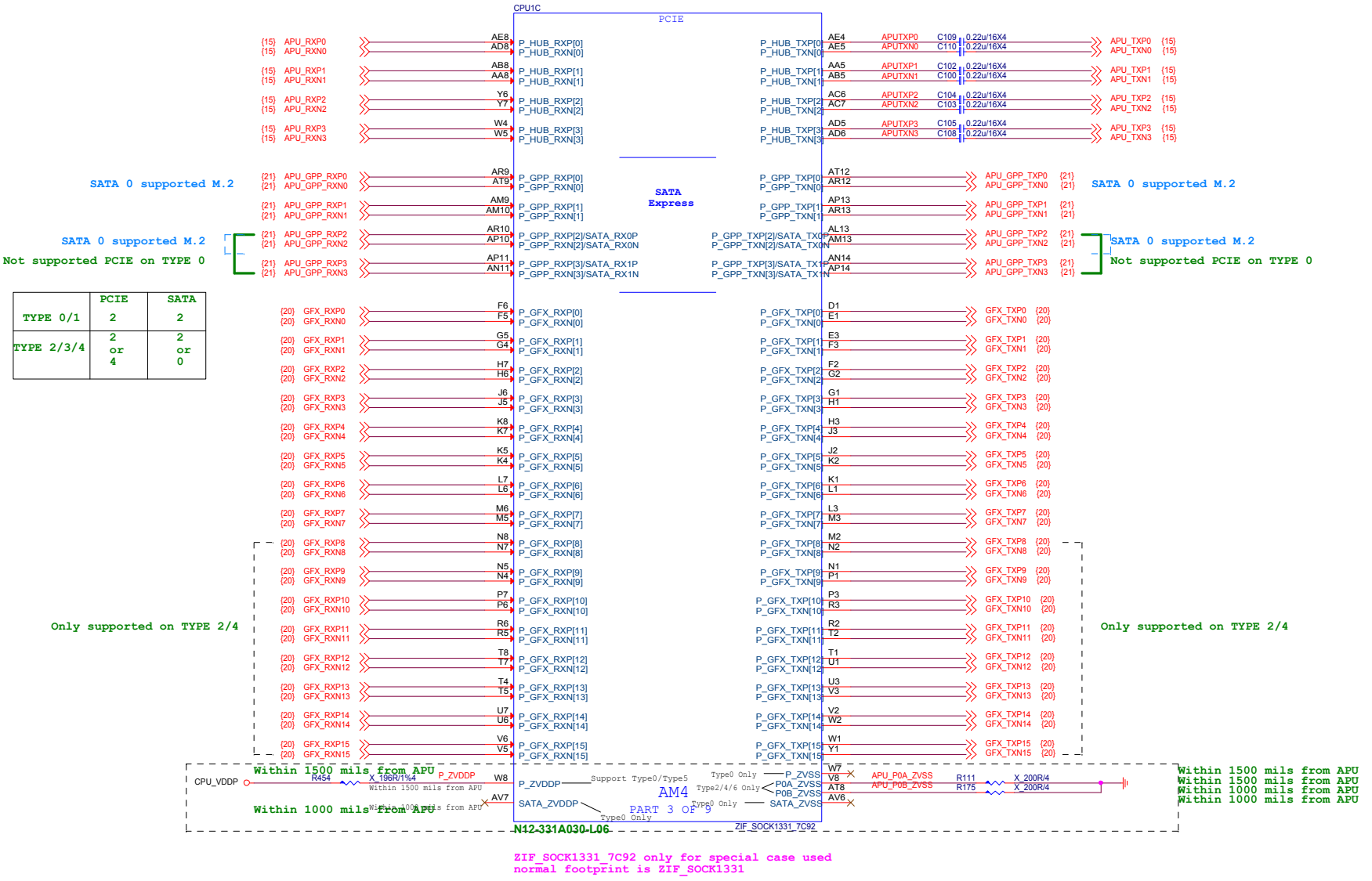

	PCIE	SATA
TYPE 0/1	2	2
TYPE 2/3/4	2 or 4	2 or 0

ZIF_SOCK1331_7C92 only for special case used
normal footprint is ZIF_SOCK1331

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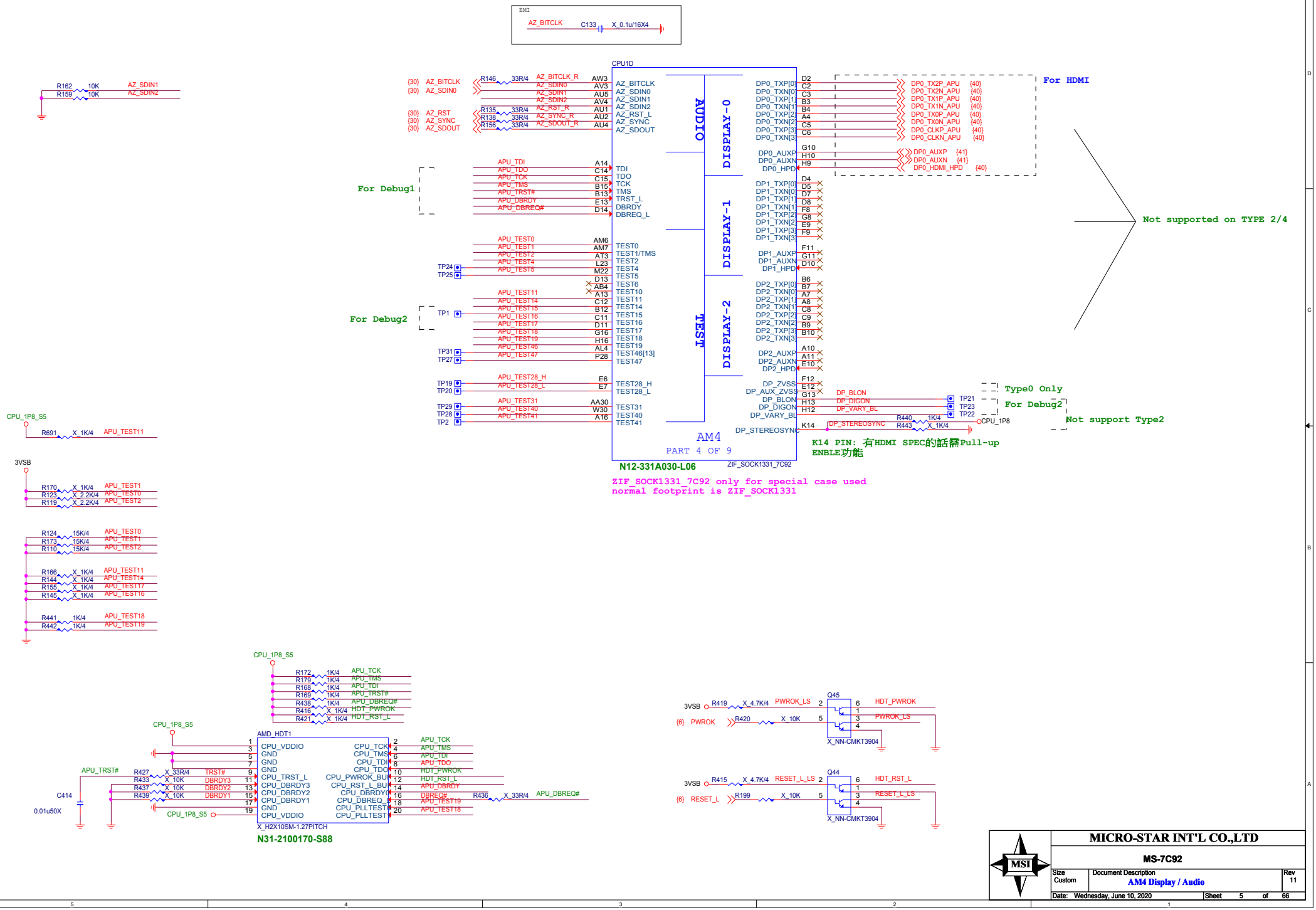

MICRO-STAR INT'L CO.,LTD

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Custom	AM4 Display / Audio	11

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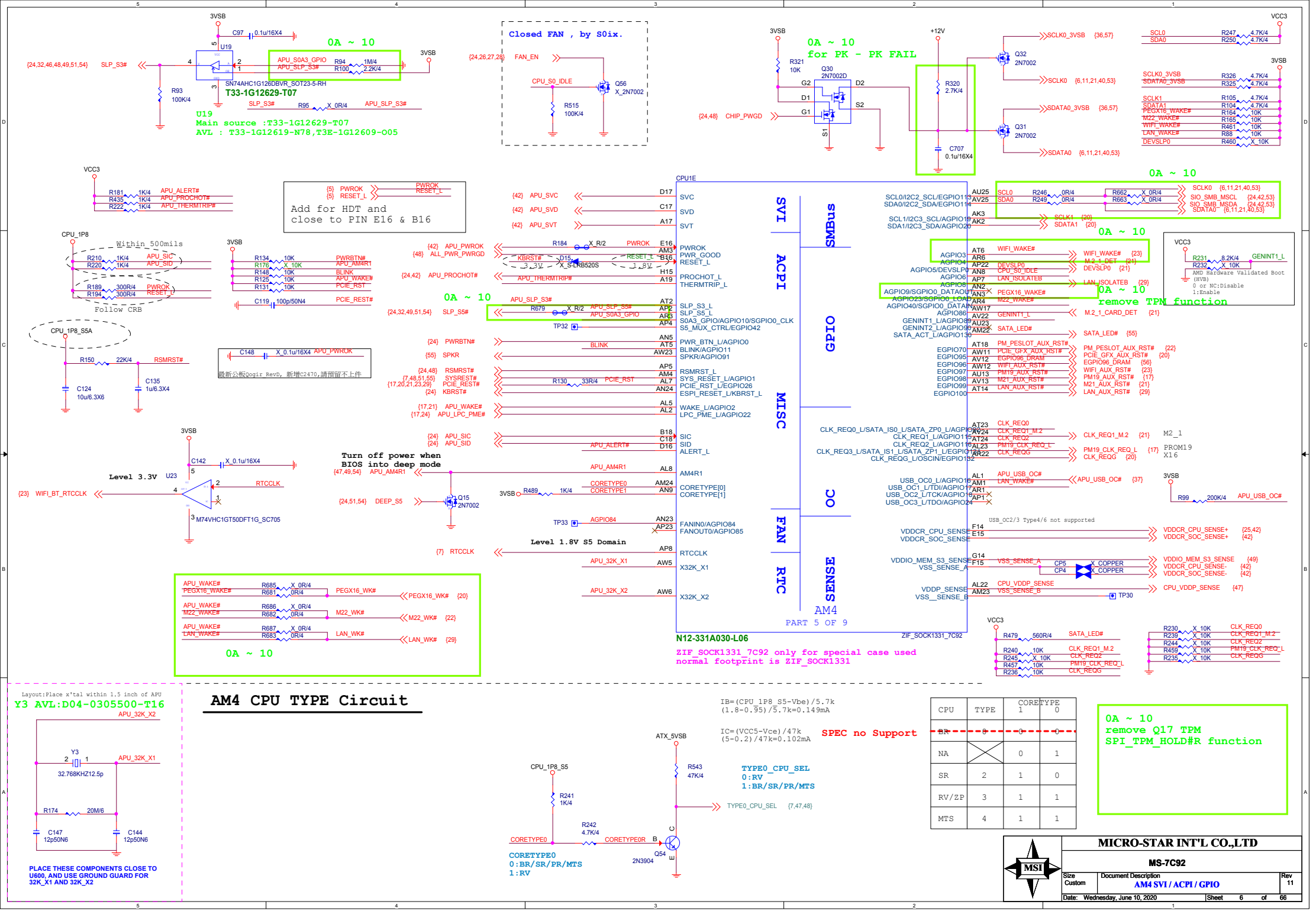
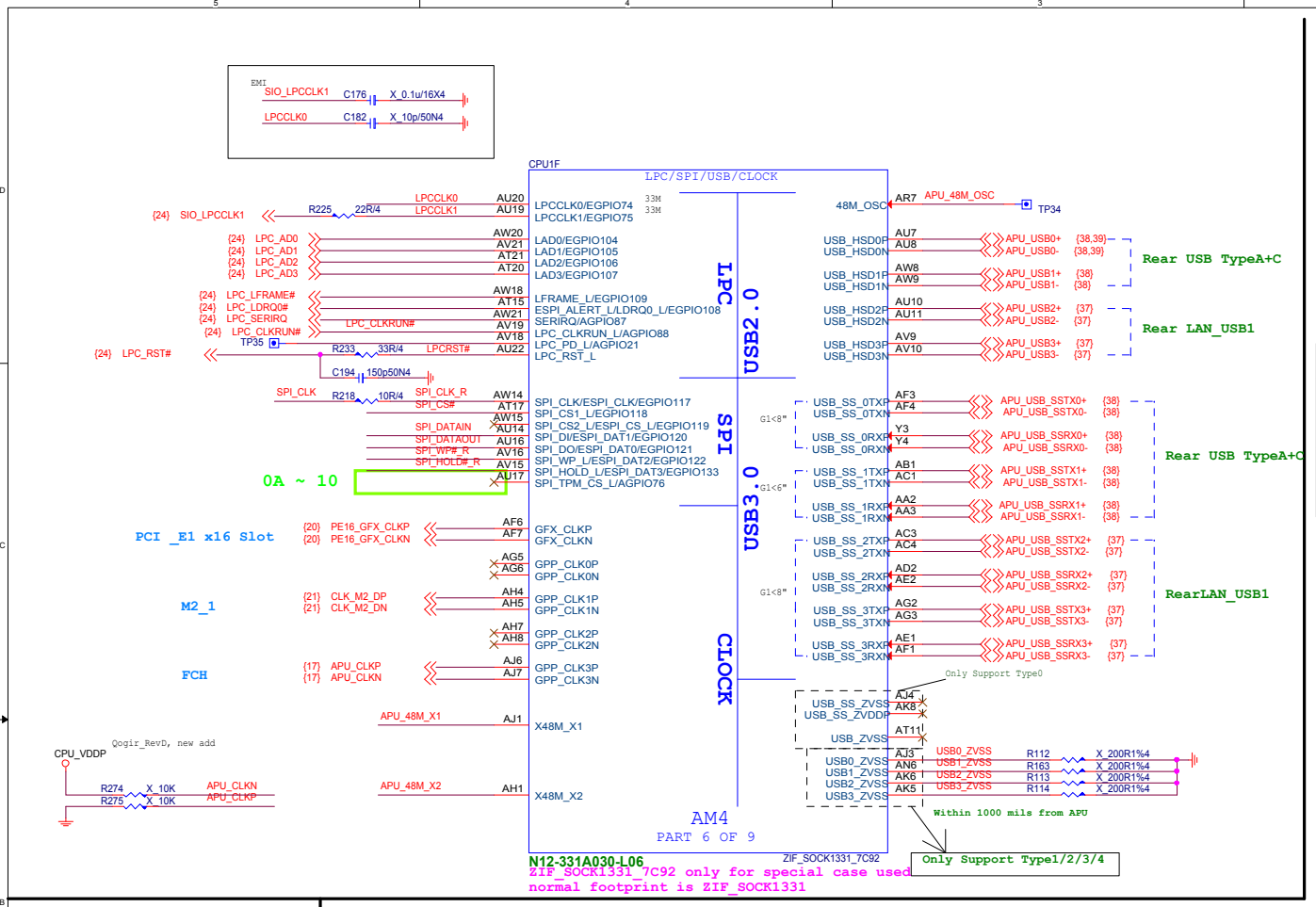
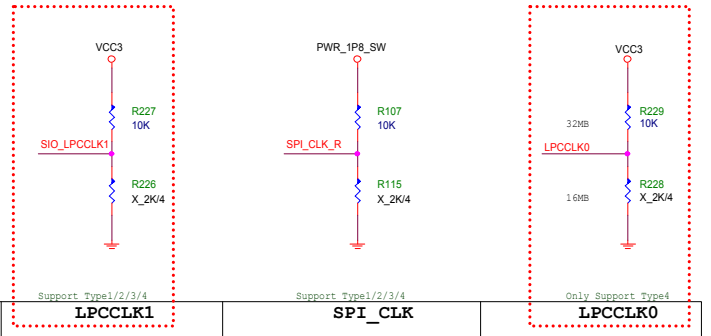


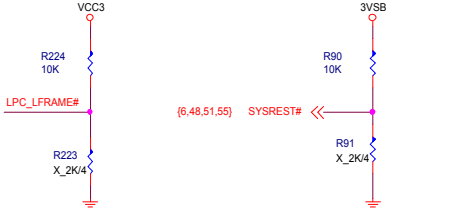
CPU	TYPE	CORETYPE 1	CORETYPE 0
~~BR~~	~~0~~	~~0~~	~~0~~
NA		0	1
SR	2	1	0
RV/ZP	3	1	1
MTS	4	1	1



Strapping Options

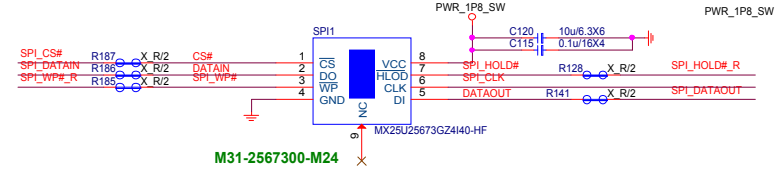


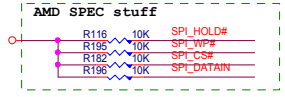
	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator **(Default)**	Use 48Mhz crystal clock and generate both internal and external clocks **(Default)**	PSP should modify SPI page register bits [25:24] to remap physical ROM to upper image **(Default)**
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	PSP should not modify SPI page register bits [25:24]

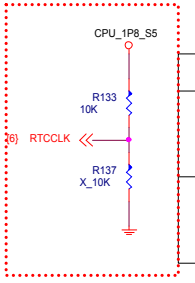


	AGPIO3	LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic **(Default)**	SPI ROM **(Default)**	Normal reset mode **(Default)**
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode

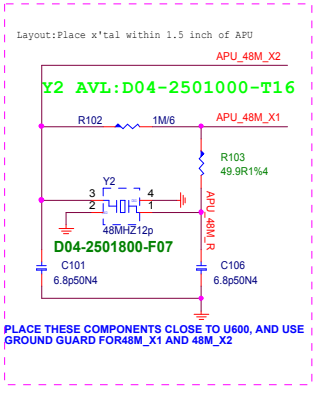
SPI ROM(1.8V)

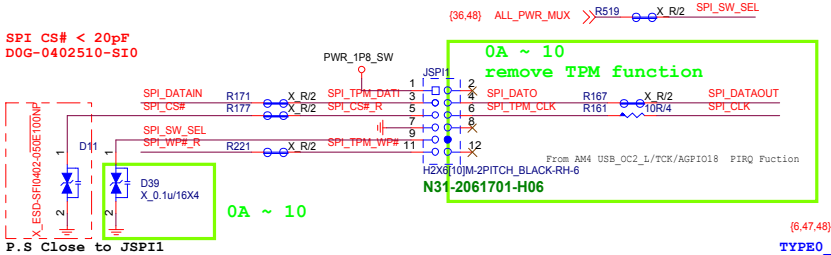


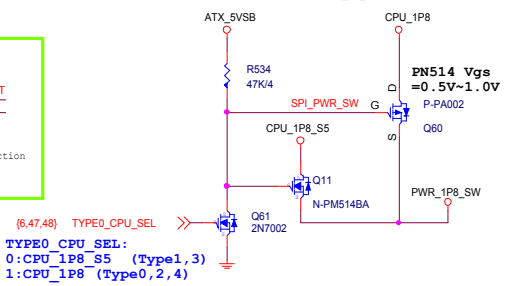




	RTCCLK
PULL HIGH	RTCCLK is input and is used as the bypass clock **(Default)**
PULL LOW	Normal Mode: Use 32Khz xtal as the source of RTC clock







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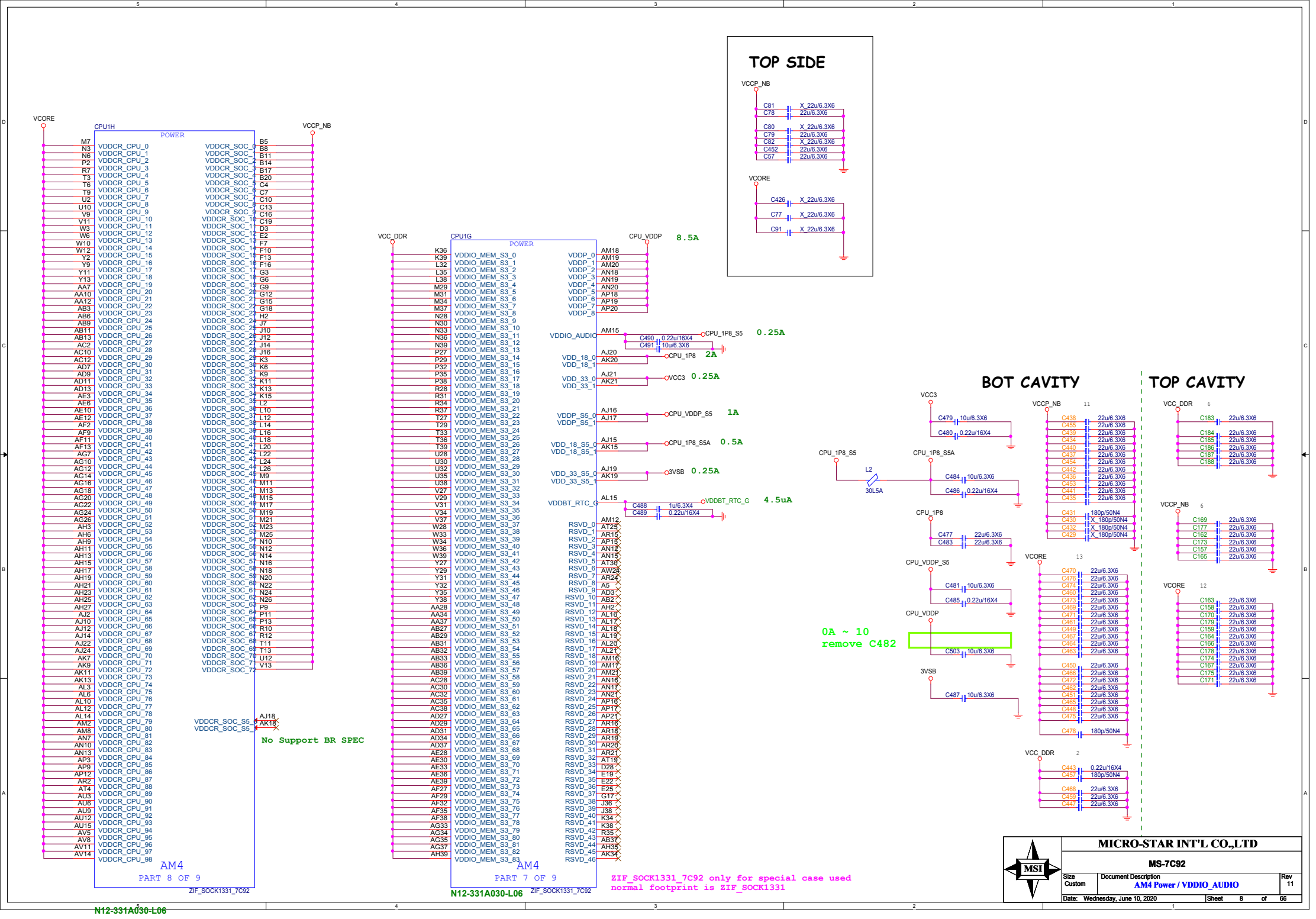
TOP SIDE
VCCP_NB
C81 X_22u/6.3X6
C78 22u/6.3X6
C80 X_22u/6.3X6
C79 22u/6.3X6
C82 X_22u/6.3X6
C452 22u/6.3X6
C57 22u/6.3X6
VCORE
C426 X_22u/6.3X6
C77 X_22u/6.3X6
C91 X_22u/6.3X6
VCORE
CPU1H
POWER
VCCP_NB
VDDCR_CPU_0 ... VDDCR_CPU_98
VDDCR_SOC_0 ... VDDCR_SOC_72
VDDCR_SOC_S5_0
VDDCR_SOC_S5_1
AJ18
AK18
No Support BR SPEC
AM4
PART 8 OF 9
ZIF_SOCK1331_7C92
VCC_DDR
CPU1G
POWER
CPU_VDDP 8.5A
VDDIO_MEM_S3_0 ... VDDIO_MEM_S3_83
VDDP_0 ... VDDP_8
VDDIO_AUDIO AM15
C490 0.22u/16X4
C491 10u/6.3X6
CPU_1P8_S5 0.25A
VDD_18_0 VDD_18_1 AJ20 AK20
CPU_1P8 2A
VDD_33_0 VDD_33_1 AJ21 AK21
VCC3 0.25A
VDDP_S5_0 VDDP_S5_1 AJ16 AJ17
CPU_VDDP_S5 1A
VDD_18_S5_0 VDD_18_S5_1 AJ15 AK15
CPU_1P8_S5A 0.5A
VDD_33_S5_0 VDD_33_S5_1 AJ19 AK19
3VSB 0.25A
VDDBT_RTC_G AL15
C488 1u/6.3X4
C489 0.22u/16X4
VDDBT_RTC_G 4.5uA
AM12
RSVD_0 ... RSVD_46
AM4
PART 7 OF 9
ZIF_SOCK1331_7C92
ZIF_SOCK1331_7C92 only for special case used
normal footprint is ZIF_SOCK1331
N12-331A030-L06
N12-331A030-L06
BOT CAVITY
TOP CAVITY
VCC3
C479 10u/6.3X6
C480 0.22u/16X4
CPU_1P8_S5
L2
30L5A
CPU_1P8_S5A
C484 10u/6.3X6
C486 0.22u/16X4
CPU_1P8
C477 22u/6.3X6
C483 22u/6.3X6
CPU_VDDP_S5
C481 10u/6.3X6
C485 0.22u/16X4
CPU_VDDP
C503 10u/6.3X6
3VSB
C487 10u/6.3X6
0A ~ 10
remove C482
VCCP_NB 11
C438 22u/6.3X6
C455 22u/6.3X6
C439 22u/6.3X6
C434 22u/6.3X6
C440 22u/6.3X6
C437 22u/6.3X6
C454 22u/6.3X6
C442 22u/6.3X6
C436 22u/6.3X6
C453 22u/6.3X6
C441 22u/6.3X6
C435 22u/6.3X6
C431 180p/50N4
C430 X_180p/50N4
C432 X_180p/50N4
C429 X_180p/50N4
VCORE 13
C470 22u/6.3X6
C476 22u/6.3X6
C474 22u/6.3X6
C460 22u/6.3X6
C473 22u/6.3X6
C469 22u/6.3X6
C471 22u/6.3X6
C461 22u/6.3X6
C449 22u/6.3X6
C467 22u/6.3X6
C464 22u/6.3X6
C463 22u/6.3X6
C450 22u/6.3X6
C466 22u/6.3X6
C472 22u/6.3X6
C462 22u/6.3X6
C451 22u/6.3X6
C465 22u/6.3X6
C448 22u/6.3X6
C475 22u/6.3X6
C478 180p/50N4
VCC_DDR 2
C443 0.22u/16X4
C457 180p/50N4
C468 22u/6.3X6
C459 22u/6.3X6
C447 22u/6.3X6
VCC_DDR 6
C183 22u/6.3X6
C184 22u/6.3X6
C185 22u/6.3X6
C186 22u/6.3X6
C187 22u/6.3X6
C188 22u/6.3X6
VCCP_NB 6
C169 22u/6.3X6
C177 22u/6.3X6
C162 22u/6.3X6
C173 22u/6.3X6
C157 22u/6.3X6
C165 22u/6.3X6
VCORE 12
C163 22u/6.3X6
C158 22u/6.3X6
C170 22u/6.3X6
C179 22u/6.3X6
C159 22u/6.3X6
C164 22u/6.3X6
C166 22u/6.3X6
C178 22u/6.3X6
C174 22u/6.3X6
C167 22u/6.3X6
C175 22u/6.3X6
C171 22u/6.3X6
MICRO-STAR INT'L CO.,LTD
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Size Custom
Document Description
AM4 Power / VDDIO_AUDIO
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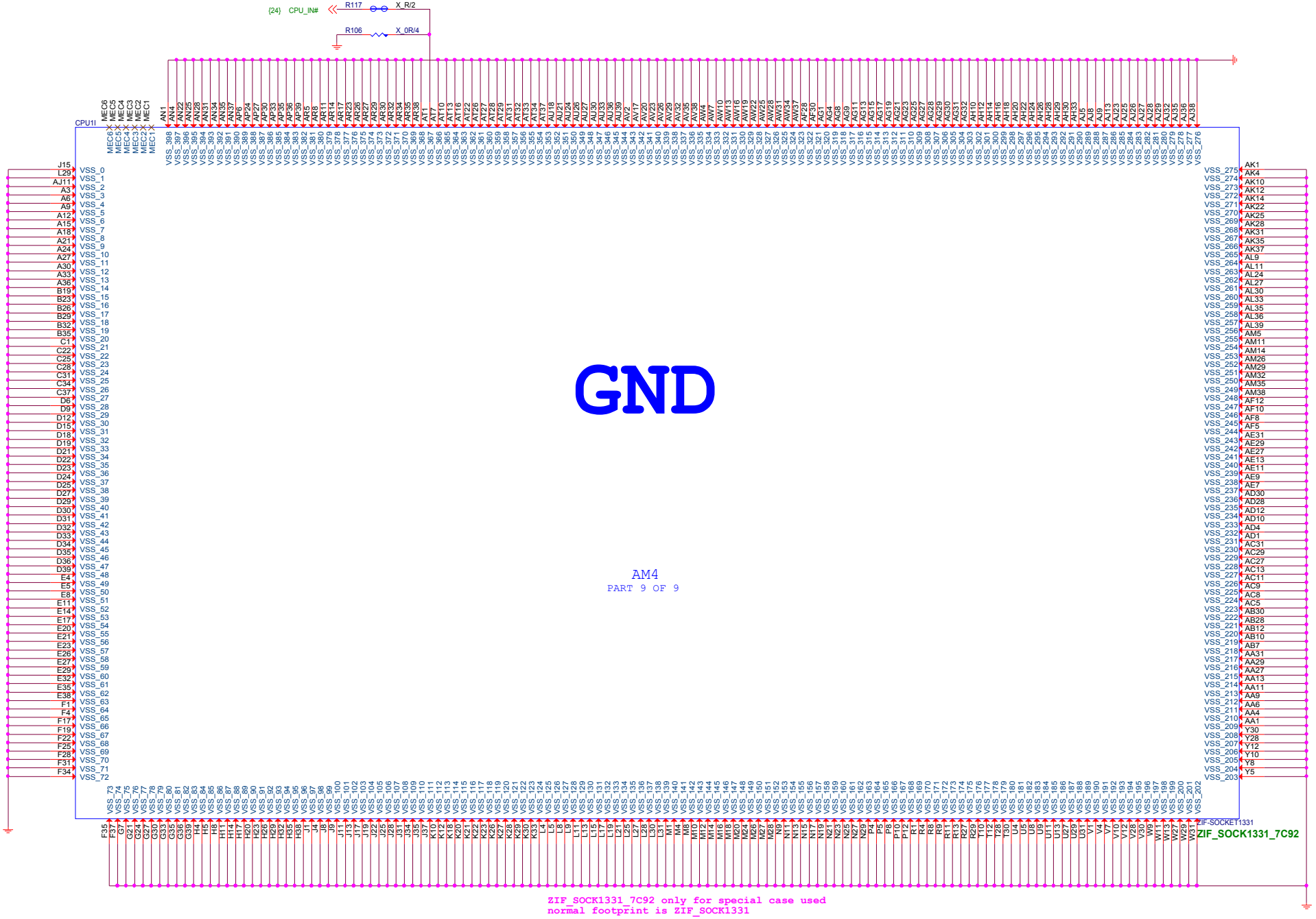

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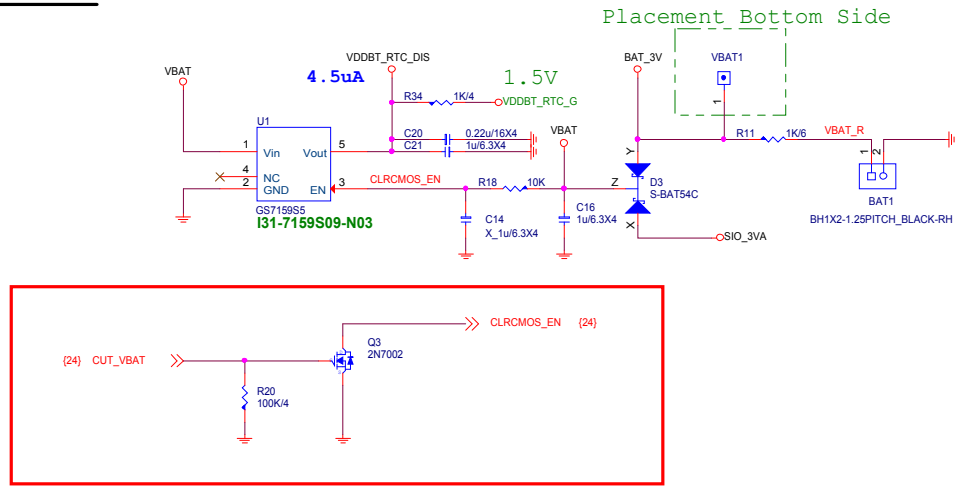
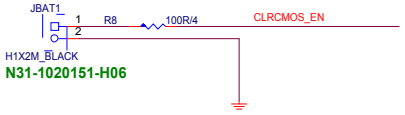
RTC & Clear CMOS Circuit



Clear CMOS button



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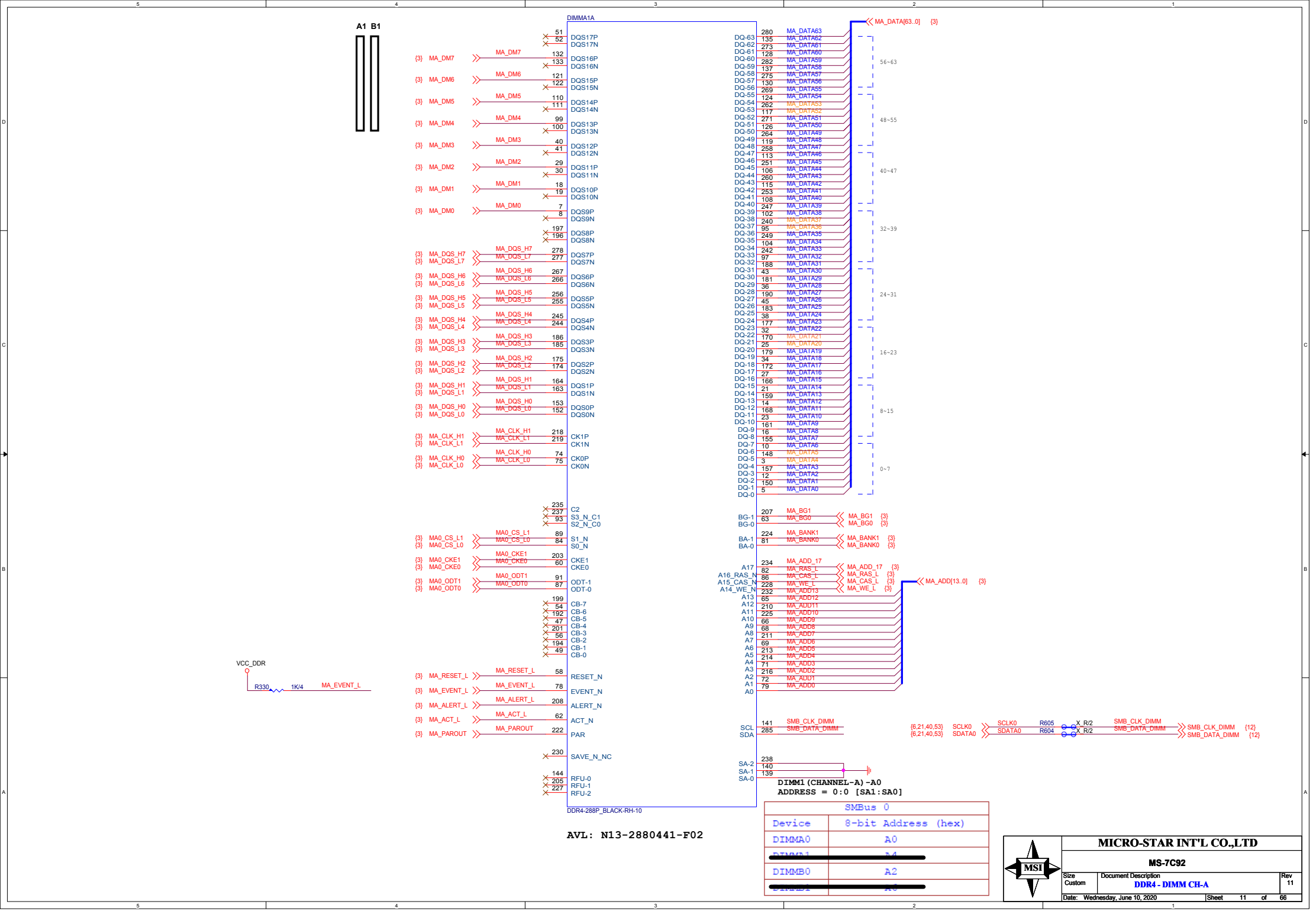
A1 B1
DIMMA1A
DDR4-288P_BLACK-RH-10
MA_DATA[63..0] {3}
MA_ADD[13..0] {3}
VCC_DDR
R330 1K/4 MA_EVENT_L
DIMM1(CHANNEL-A)-A0
ADDRESS = 0:0 [SA1:SA0]
AVL: N13-2880441-F02
SMBus 0
Device 8-bit Address (hex)
DIMMA0 A0
DIMMB0 A2
MICRO-STAR INT'L CO.,LTD
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DDR4 - DIMM CH-A
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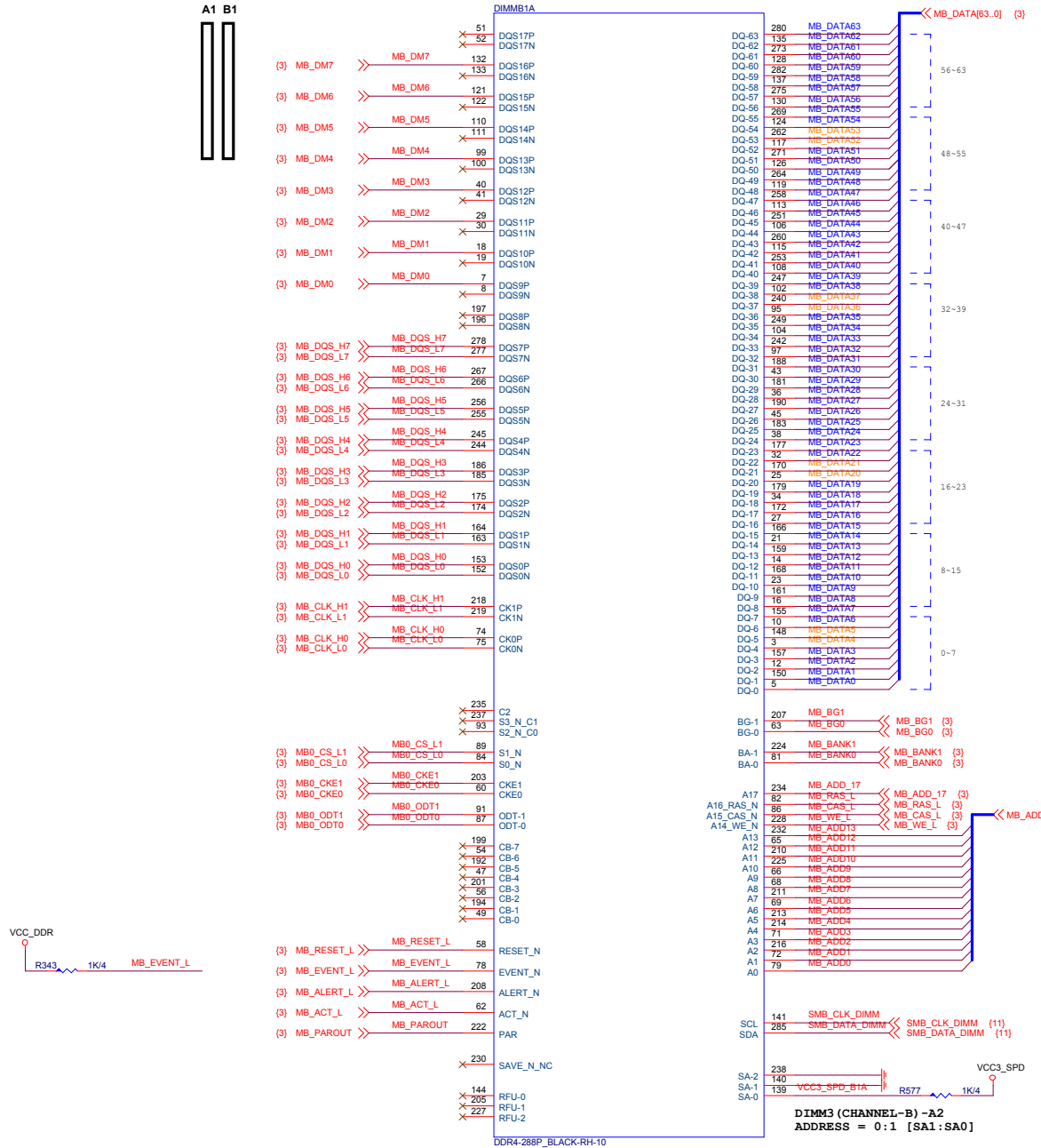

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avl:D08-0301100-B07

F6
VCC3 1 2 VCC3_SPD
F-SPR-P260T
D08-0301000-P16

DIMM SLOT PN BY SPEC

DIMMA1C
DDR4-288P_BLACK-RH-10

	1	12V3_NC_1	
	145	12V3_NC_145	
VCC3_SPD	284	VDDSPD	
VPP25	142	VPP-1	
	143	VPP-2	
	286	VPP-3	
	287	VPP-4	
	288	VPP-5	
VTT_DDR	77	VTT-1	
	221	VTT-2	
DIMM_CA_VREF_A	146	VREFCA	
MEC3		MEC3	
MEC2		MEC2	
MEC1		MEC1	

VCC_DDR

VDD-0	236	VDD-13	90
VDD-1	233	VDD-14	88
VDD-2	231	VDD-15	85
VDD-3	229	VDD-16	83
VDD-4	226	VDD-17	80
VDD-5	223	VDD-18	76
VDD-6	220	VDD-19	73
VDD-7	217	VDD-20	70
VDD-8	215	VDD-21	67
VDD-9	212	VDD-22	64
VDD-10	209	VDD-23	61
VDD-11	206	VDD-24	59
VDD-12	204	VDD-25	

VCC3_SPD — C321 0.1u/16X4

DIMM_CA_VREF_A — C395 2.2u/6.3X4, C394 0.1u/16X4

VTT_DDR — C318 0.1u/16X4

VPP25 — C616 0.1u/16X4, C632 0.1u/16X4

0A ~ 10
remove C506,507,512,519,522

VCC_DDR — C289 X_1u/6.3X4, C292 X_0.1u/16X4, C291 X_0.1u/16X4

DDR VREF

(place resistors close to DIMMs)

DIMM_CA_VREF_A — C312 0.1u/16X4 — VCC_DDR

DIMM_CA_VREF_A, VCC_DDR — R341 1K/1%4, C305 0.1u/16X4, C311 1000p/50X4, C310 0.1u/16X4, R342 1K/1%4

DIMMA1B
DDR4-288P_BLACK-RH-10

	2	VSS-93	
	4	VSS-92	
	6	VSS-91	
	9	VSS-90	
	11	VSS-89	
	13	VSS-88	
	15	VSS-87	
	17	VSS-86	
	20	VSS-85	
	22	VSS-84	
	24	VSS-83	
	26	VSS-82	
	28	VSS-81	
	31	VSS-80	
	33	VSS-79	
	35	VSS-78	
	37	VSS-77	
	39	VSS-76	
	42	VSS-75	
	44	VSS-74	
	46	VSS-73	
	48	VSS-72	
	50	VSS-71	
	53	VSS-70	
	55	VSS-69	
	57	VSS-68	
	94	VSS-67	
	96	VSS-66	
	98	VSS-65	
	101	VSS-64	
	103	VSS-63	
	105	VSS-62	
	107	VSS-61	
	109	VSS-60	
	112	VSS-59	
	114	VSS-58	
	116	VSS-57	
	118	VSS-56	
	120	VSS-55	
	123	VSS-54	
	125	VSS-53	
	127	VSS-52	
	129	VSS-51	
	131	VSS-50	
	134	VSS-49	
	136	VSS-48	
	138	VSS-47	

VSS-46	147	VSS-33	178
VSS-45	149	VSS-32	180
VSS-44	151	VSS-31	182
VSS-43	154	VSS-30	184
VSS-42	156	VSS-29	187
VSS-41	158	VSS-28	189
VSS-40	160	VSS-27	191
VSS-39	162	VSS-26	193
VSS-38	165	VSS-25	195
VSS-37	167	VSS-24	198
VSS-36	169	VSS-23	200
VSS-35	171	VSS-22	202
VSS-34	173	VSS-21	239
	176	VSS-20	241
		VSS-19	243
		VSS-18	246
		VSS-17	248
		VSS-16	250
		VSS-15	252
		VSS-14	254
		VSS-13	257
		VSS-12	259
		VSS-11	261
		VSS-10	263
		VSS-9	265
		VSS-8	268
		VSS-7	270
		VSS-6	272
		VSS-5	274
		VSS-4	276
		VSS-3	279
		VSS-2	281
		VSS-1	283
		VSS-0	

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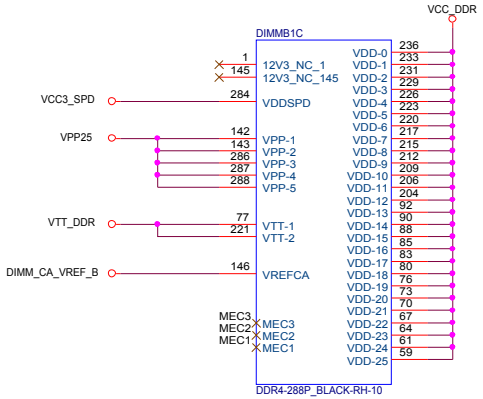
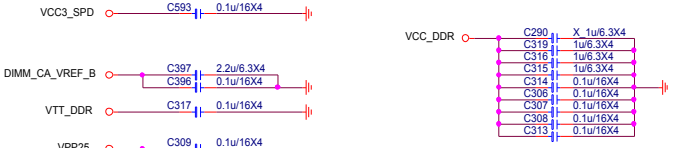
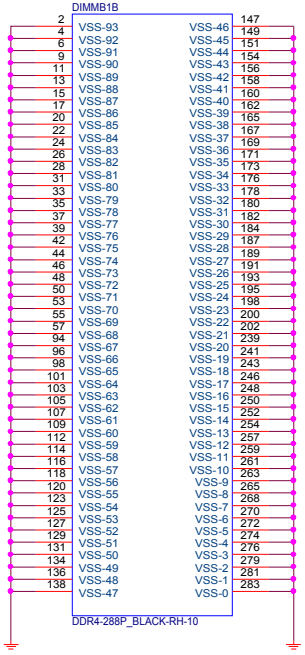
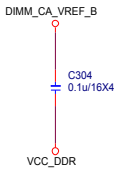


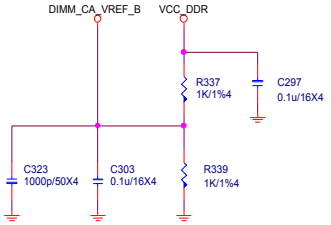




DDR VREF

(place resistors close to DIMMs)





MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C92	
Size: Custom	Document Description: DDR4 - POWER/GND-2	Rev: 11
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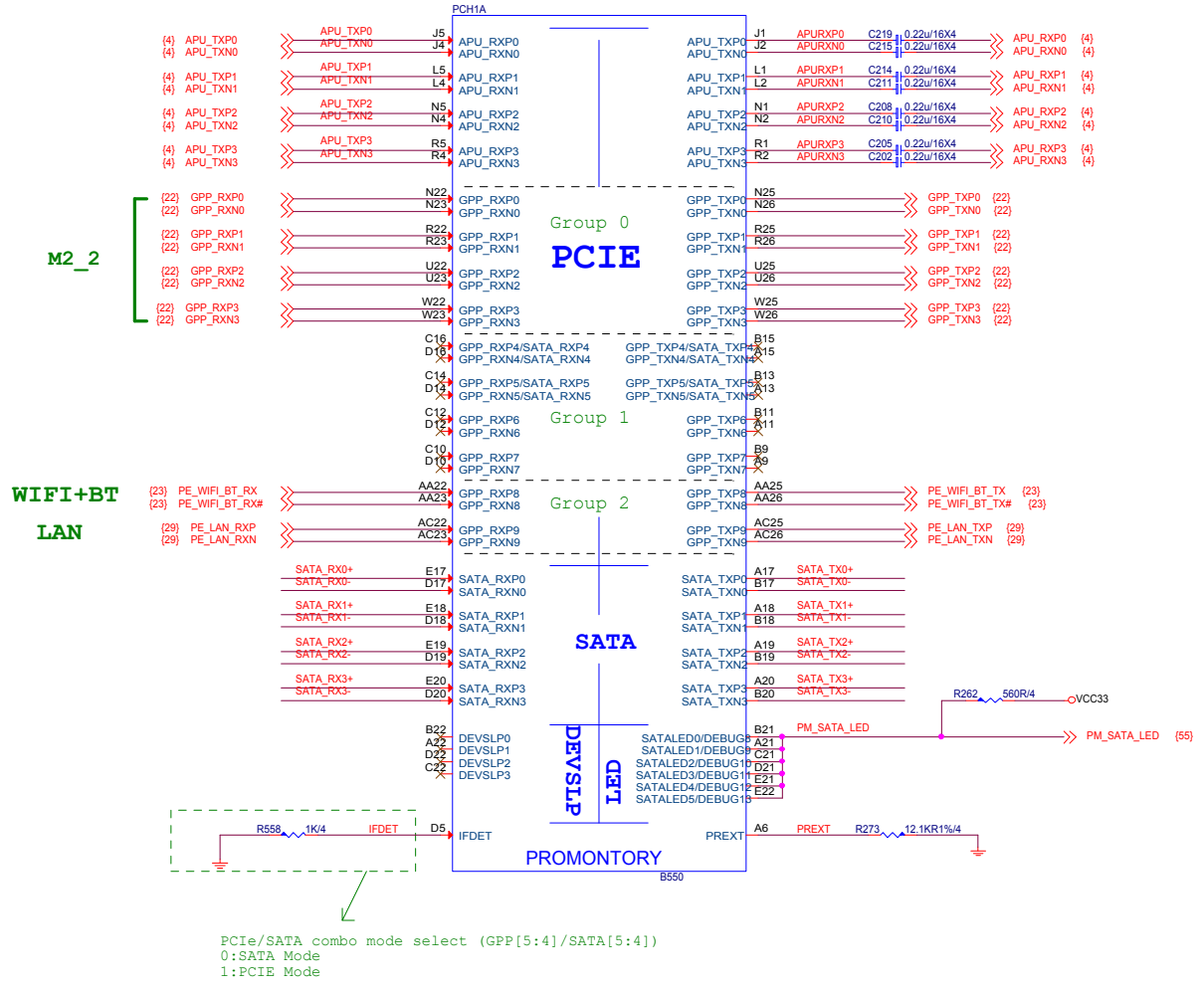
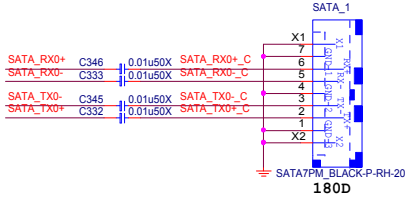
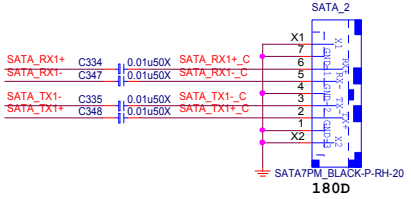


SATA Connector

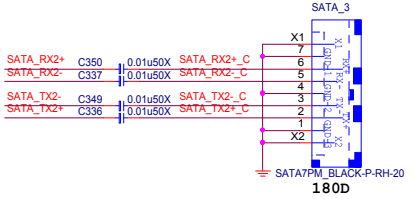
SATA1



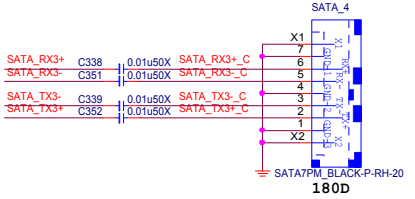
SATA2



SATA3



SATA4



MICRO-STAR INT'L CO.,LTD	
MS-7C92	
Size: Custom	Document Description: Premium - PCIE/SATA
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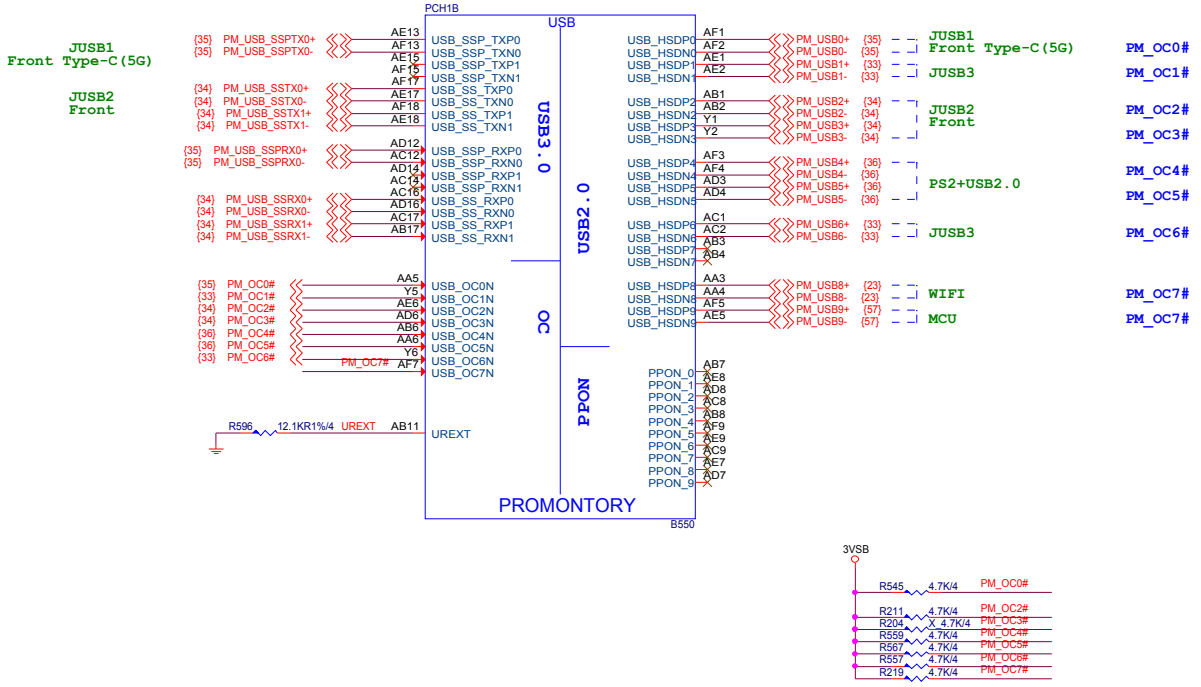
Date: Wednesday, June 10, 2020	Sheet 15 of 66



USB mapping

```
USB_SSP_TX/RX[0] + USB_HSDP/N[0] + USB_OC0N
USB_SSP_TX/RX[1] + USB_HSDP/N[1] + USB_OC1N

USB_SS_TX/RX[0] + USB_HSDP/N[2] + USB_OC2N
USB_SS_TX/RX[1] + USB_HSDP/N[3] + USB_OC3N
                  USB_HSDP/N[4] + USB_OC4N
                  USB_HSDP/N[5] + USB_OC5N
                  USB_HSDP/N[6] + USB_OC6N
                  USB_HSDP/N[7] + USB_OC7N
                  USB_HSDP/N[8] + USB_OC7N
                  USB_HSDP/N[9] + USB_OC7N
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MICRO-STAR INT'L CO.,LTD	
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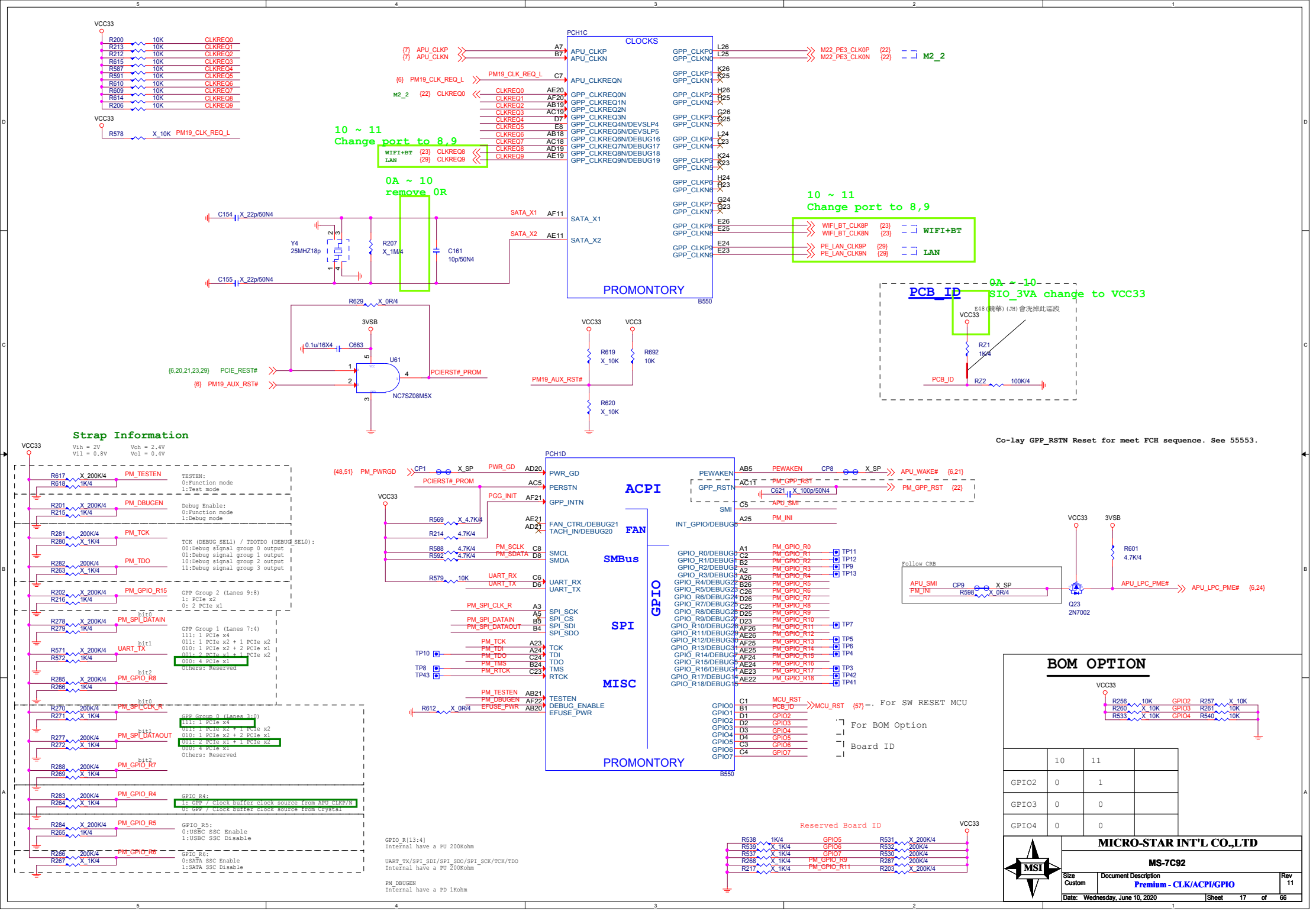
Size: Custom	Document Description: Premium - USB/OC
Rev: 11	
Date: Wednesday, June 10, 2020	Sheet 16 of 66


PCH1C
CLOCKS
PROMOTORY
B550
M2_2
WIFI+BT
LAN
10 ~ 11
Change port to 8,9
0A ~ 10
remove 0R
PCB_ID
0A ~ 10
SIO_3VA change to VCC33
Strap Information
PCH1D
ACPI
FAN
SMBus
SPI
GPIO
MISC
PROMOTORY
B550
Co-lay GPP_RSTN Reset for meet FCH sequence. See 55553.
For SW RESET MCU
For BOM Option
Board ID
Reserved Board ID
BOM OPTION
MICRO-STAR INT'L CO.,LTD
MS-7C92
Premium - CLK/ACPI/GPIO
Rev 11
Wednesday, June 10, 2020
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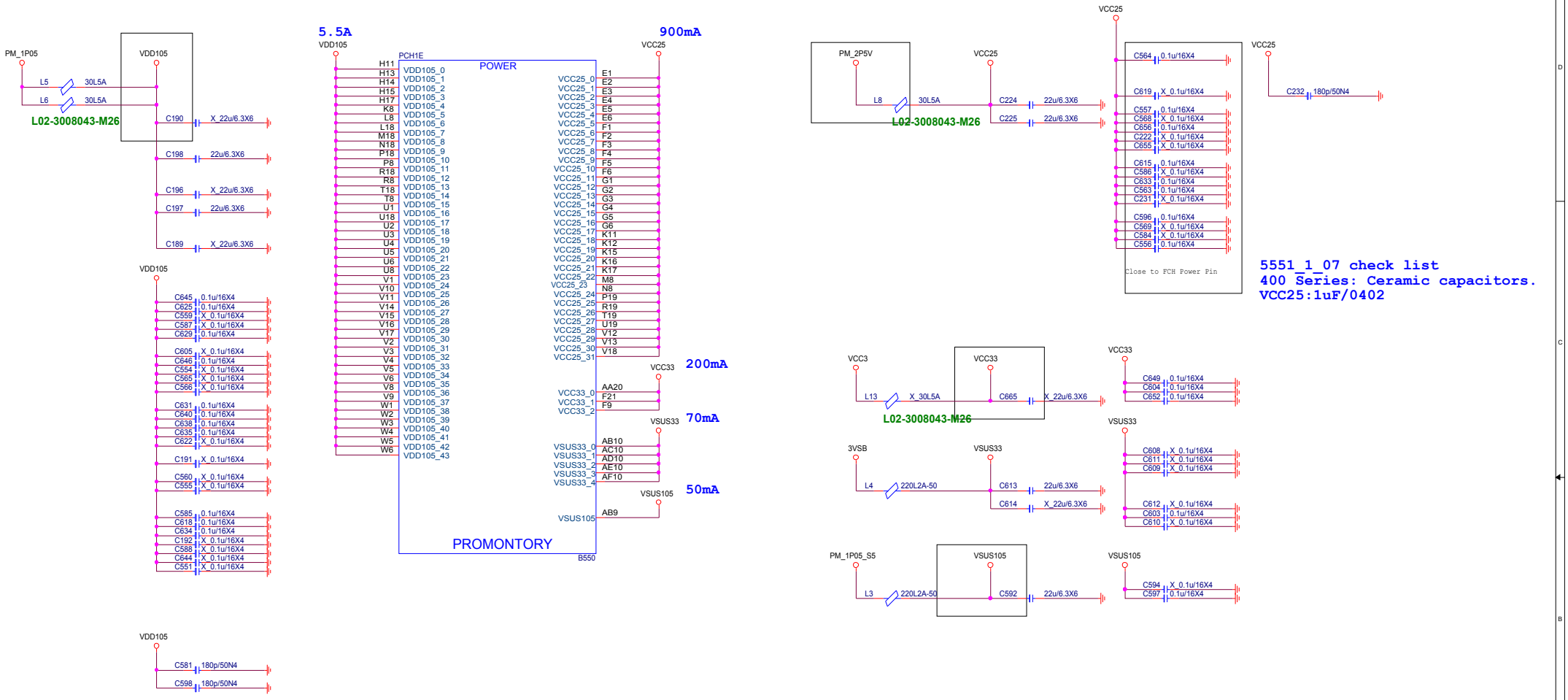
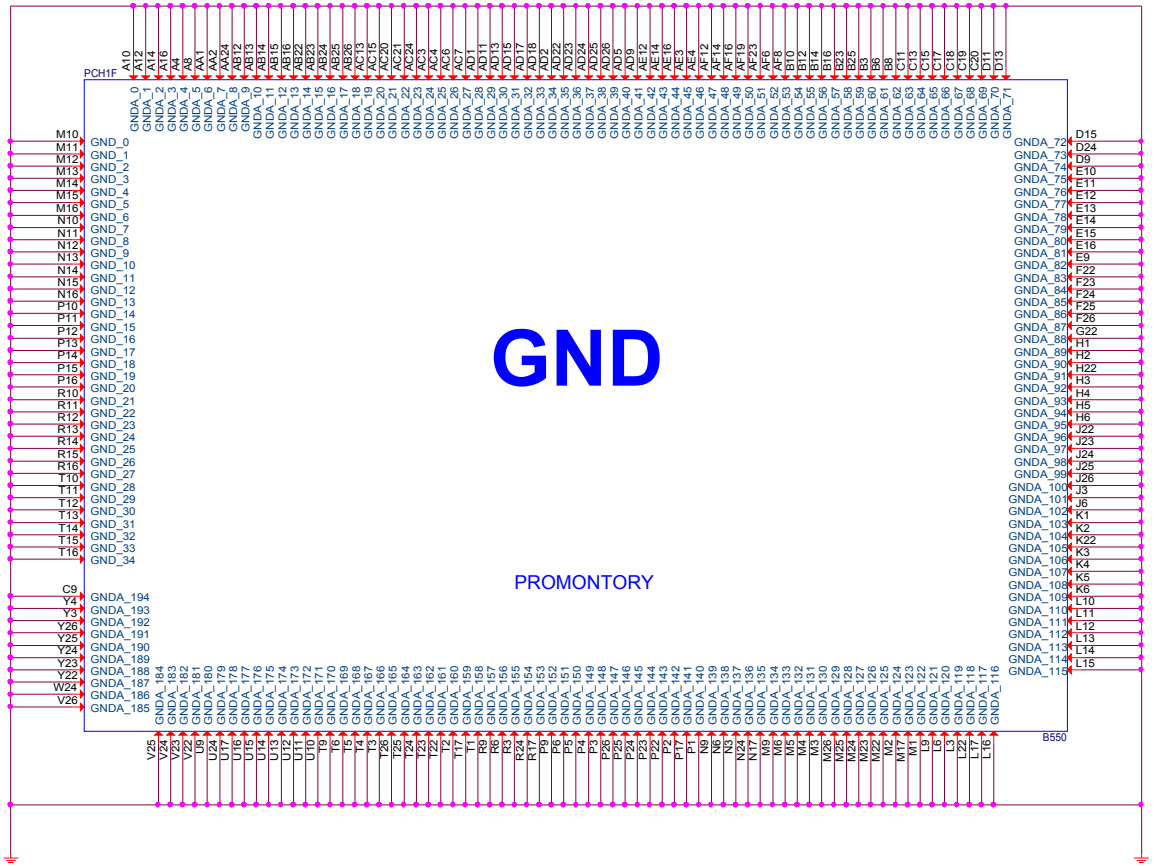


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C92	
Size: Custom	Document Description: Premium - Power	Rev: 11
Date: Wednesday, June 10, 2020	Sheet 18 of 66	



MICRO-STAR INT'L CO.,LTD	
MS-7C92	
Size: Custom	Document Description: Premium - GND
Rev: 11	
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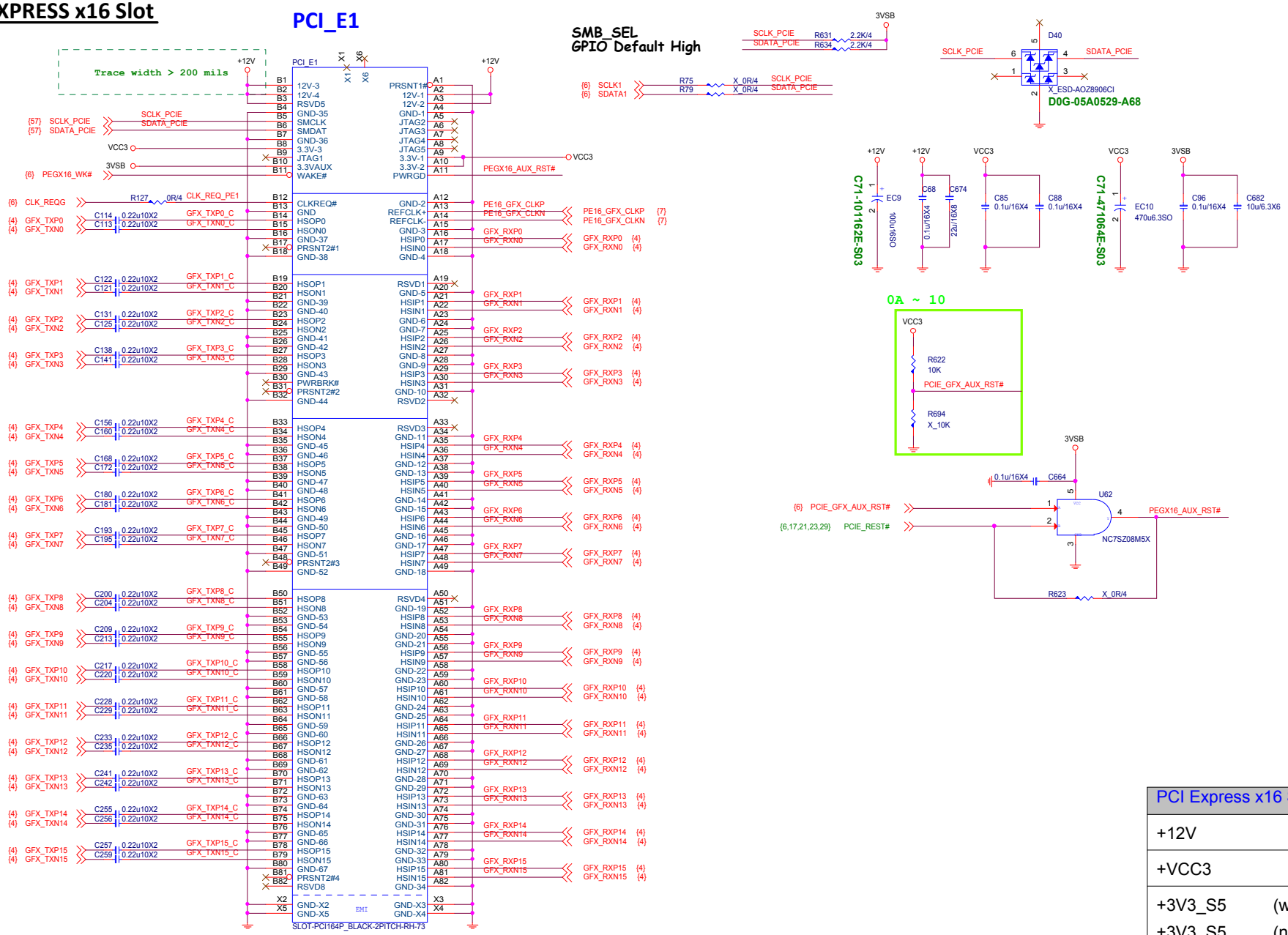
PCI EXPRESS x16 Slot



PCI Express x16 Slot		
+12V		- 5.5 A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

MICRO-STAR INT'L CO.,LTD	
MS-7C92	
Size: Custom	Document Description: PCI_E1 (X16)
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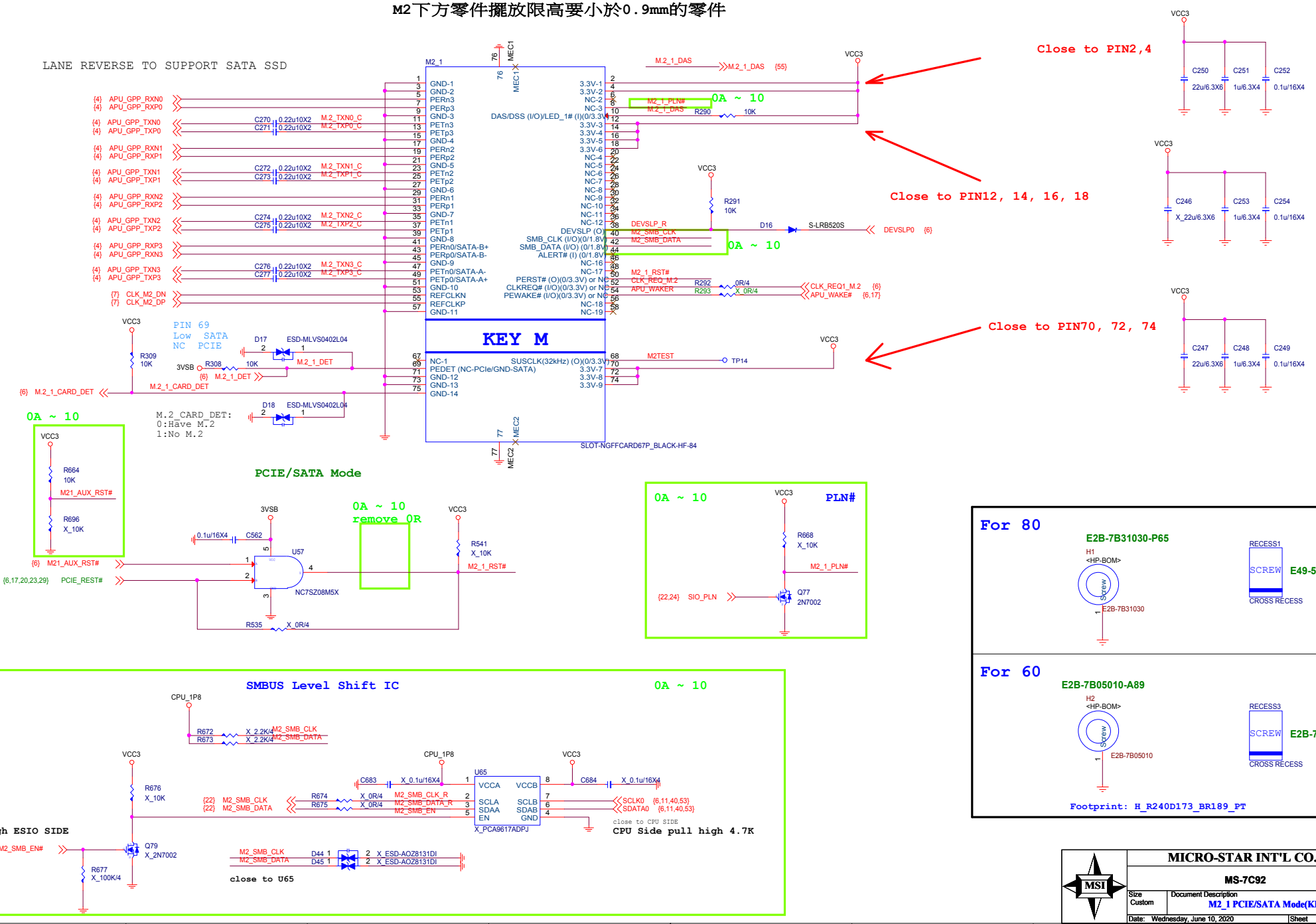
M.2_1 Connector

VCC3 4.25A
Max: 14W

M2下方零件擺放限高要小於0.9mm的零件



For 80

E2B-7B31030-P65

H1 <HP-BOM>

E2B-7B31030

RECESS1 SCREW CROSS RECESS E49-5303504-H75

For 60

E2B-7B05010-A89

H2 <HP-BOM>

E2B-7B05010

RECESS3 SCREW CROSS RECESS E2B-7984020-A89

Footprint: H_R240D173_BR189_PT

MICRO-STAR INT'L CO.,LTD	
MS-7C92	
Size: Custom	Document Description: M2_1 PCIE/SATA Mode(KEY_M)
Rev: 11	
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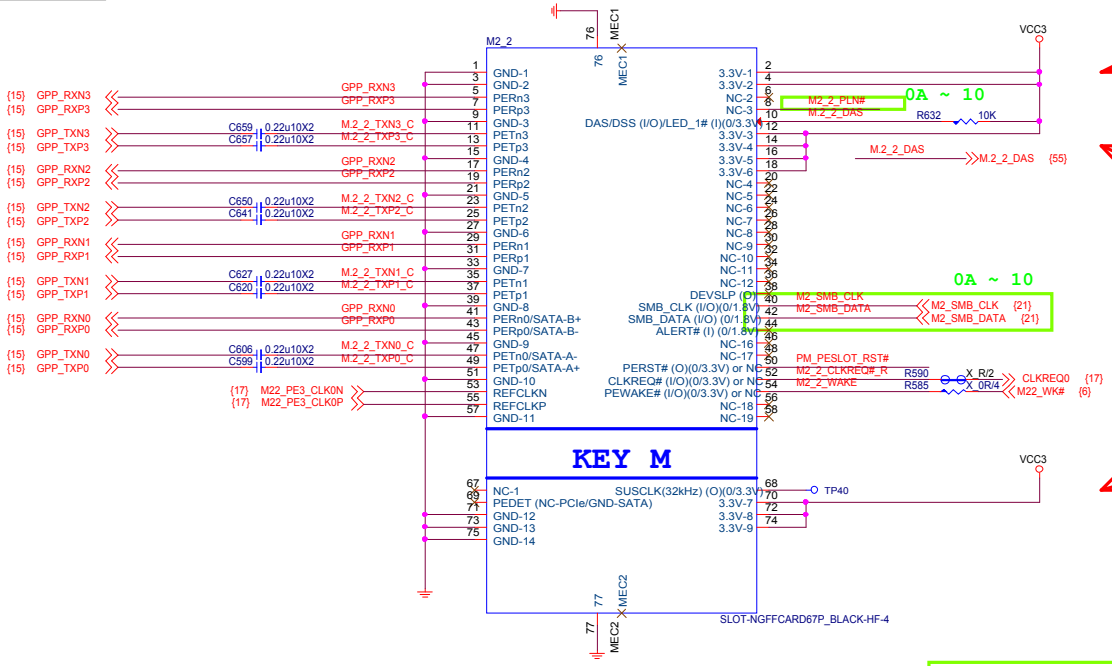
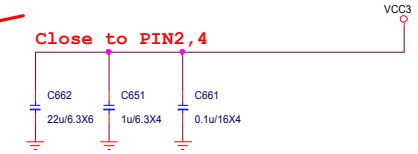
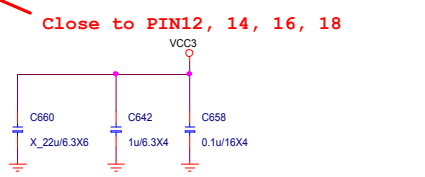
M.2_2 Connector

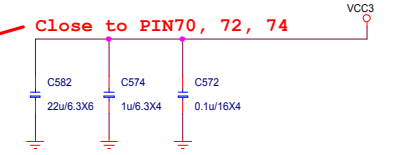
M2下方零件擺放限高要小於0.9mm的零件

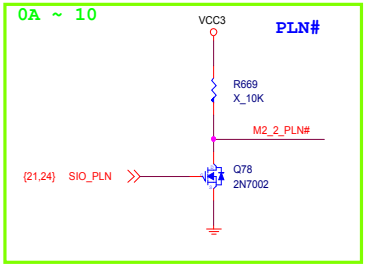
VCC3 4.25A
Max: 14W

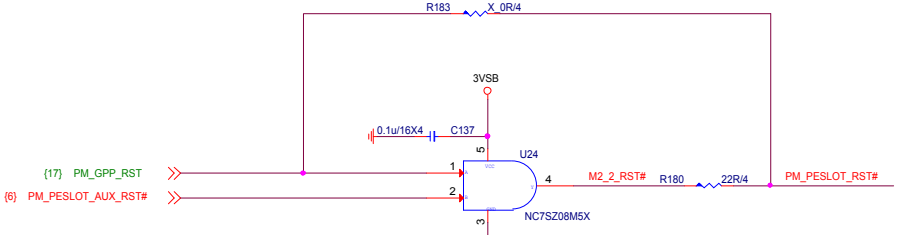


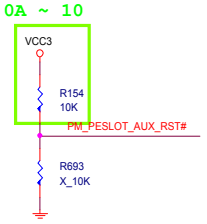


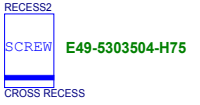












MICRO-STAR INT'L CO.,LTD

MS-7C92

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Custom	M2_2 PCIE Mode(KEY_M)	11

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EMI

NEAR CONNECTOR

{16} PM_USB8+

{16} PM_USB8-

U2

ESD-AOZ8906CI

3VSB C23 X_0.1u/16X4

780mA

M2_WIFI1 MEC2

PM_USB8+ PM_USB8-

GND-1 USB_D+ USB_D- GND-11 SDIO CLK SDIO CMD SDIO DATA0 SDIO DATA1 SDIO DATA2 SDIO DATA3 SDIO WAKE# SDIO RESET#

3.3V-1 3.3V-2 LED1# PCM_CLK / I2S SCK PCM_SYNC / I2S WS PCM_IN / I2S SD_IN PCM_OUT / I2S SD_OUT LED2# GND-2 UART WAKE# UART RXD

3VSB C24 1u/6.3X4 C22 10u/6.3X6 C25 0.01u50X

KEY E

GND-10 PETp0 PETn0 GND-9 PERp0 PERn0 GND-8 REFCLKP0 REFCLKN0 GND-7 CLKREQ0# PEWAKE0# GND-6 RESERVED / PETp1 RESERVED / PETn1 GND-5 RESERVED / PERp1 RESERVED / PERn1 GND-4 RESERVED / REFCLKP1 RESERVED / REFCLKN1 GND-3

UART TXD UART CTS UART RTS VENDOR DEFINED-1 VENDOR DEFINED-2 VENDOR DEFINED-3 COEX3 COEX2 COEX1 SUSCLK PERST0# W_DISABLE2# W_DISABLE1# I2C DATA I2C CLK ALERT# RESERVED UIM_SWP / PERST1# UIM_POWER_SNK / CLKREQ1# UIM_POWER_SRC/GPIO1 / PEWAKE1# 3.3V-3 3.3V-4

SLOT-NGFFCARD67P_BLACK-HF-46

N15-0670610-L06

{15} PE_WIFI_BT_TX 0.22u/16X4 C15 PE_WIFI_BT_TXC

{15} PE_WIFI_BT_TX# 0.22u/16X4 C13 PE_WIFI_BT_TX#C

{15} PE_WIFI_BT_RX

{15} PE_WIFI_BT_RX#

{17} WIFI_BT_CLK8P

{17} WIFI_BT_CLK8N

{17} CLKREQ8 R452 X_R/2 CLKREQ1_R

{6} WIFI_WAKE# {24,29} SIO_LAN_WAKE# D33 S-LRB520S D32 S-LRB520S WF_WAKE#

WIFI_BT_RTCCLK_R R15 0R/4 WIFI_BT_RTCCLK {6}

WIFI_RST#

BT_DISABLE_L# R453 3.3KR/4 3VSB

WIFI_DISABLE_L# R450 3.3KR/4

3VSB R451 10K WF_WAKE#

VCC3 0A ~ 10 R37 10K WIFI_AUX_RST# R695 X_10K

3VSB C456 0.01u50X C2 1u/6.3X4 C458 10u/6.3X6

10uF+0.1uF+0.01uF at one end of socket in support of 3.3 V3V pins 2 and 4.
10uF+0.1uF+0.01uF at the other end of the socket in support of 3.3 V3V pins 70 and 72.

3VSB C5 0.1u/16X4

U4 NC7SZ08M5X

{6} WIFI_AUX_RST# {6,17,20,21,29} PCIE_REST# M2_WIFI_RST R35 33R/4 WIFI_RST#

R36 X_0R/4

10 ~ 11 Change to 3VSB

ATX_5VSB 3VSB R458 47K/4 R513 47K/4 Q51 2N7002D BT_DISABLE G2 D1 G1 D2 BT_DISABLE_L# S2 S1 {24} WIFI_BTDIS# WIFI_BTDIS#

10 ~ 11 Change port to 8

10 ~ 11 Change port to 8

ATX_5VSB R455 47K/4 Q50 2N7002D WIFI_DISABLE G2 D1 G1 D2 WIFI_DISABLE_L# S2 S1 WIFI_BTDIS#

COVER1 VR Cover X1 X2 X_E21-4475020-RH

E21-4475020-C22

SCREW1 SCREW SCREW 鎖WiFi Module螺絲

E43-1204046-P65

SCREW2 SCREW SCREW 鎖WiFi Module螺絲

E43-1204046-P65

Wireless1 INTEL-AX200 Intel Wi-Fi 6 AX200

604-4475-010

MICRO-STAR INT'L CO.,LTD

MS-7C92

Size	Document Description	Rev
Custom	M2_WiFi1(KEY_E)	11

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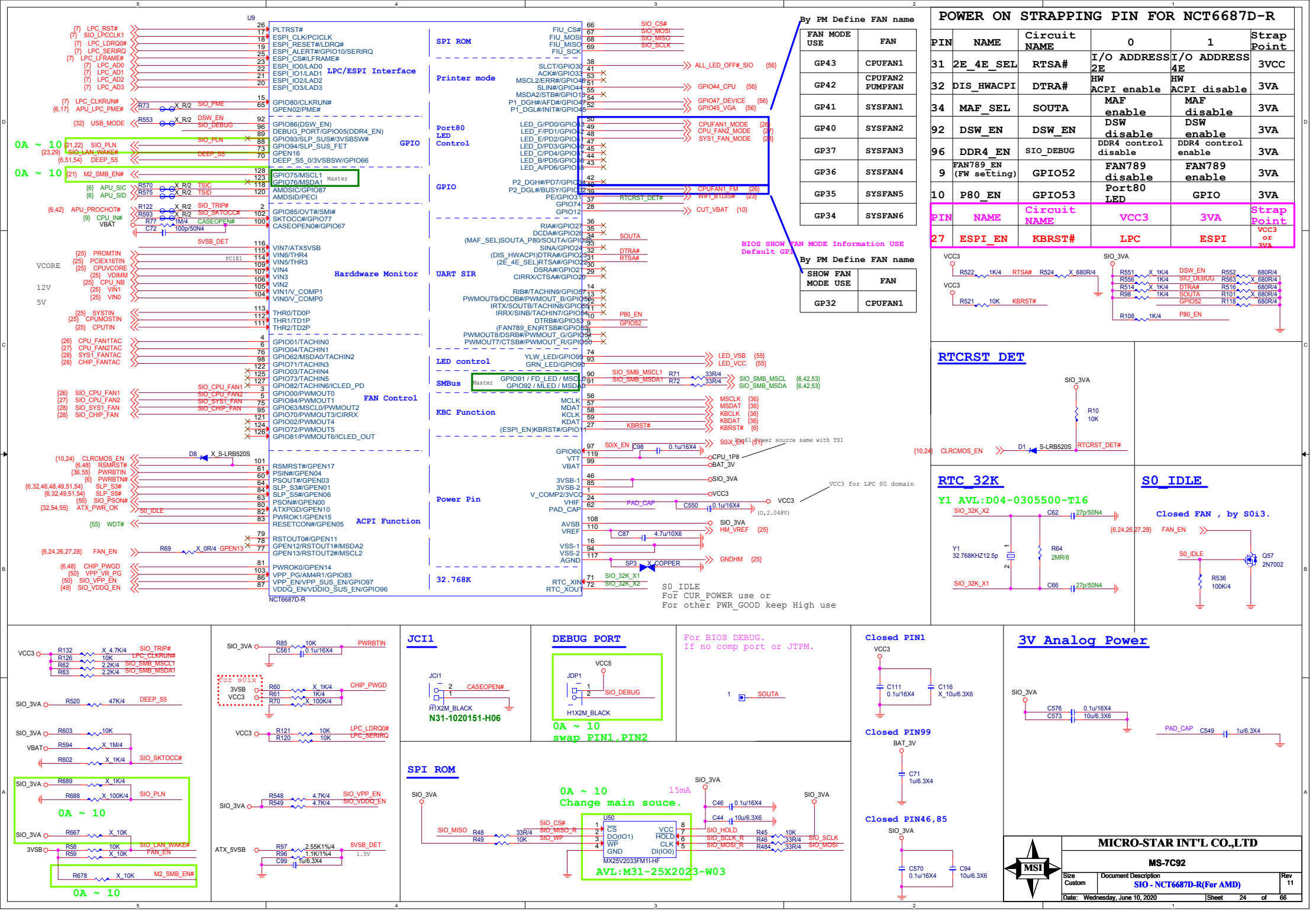
U9
NCT6687D-R
LPC/ESPI Interface
GPIO
Harddware Monitor
FAN Control
ACPI Function
SPI ROM
Printer mode
Port80 LED Control
UART SIR
LED control
SMBus
KBC Function
Power Pin
32.768K
0A ~ 10
0A ~ 10
VCORE
12V
5V
PCIE1
Master
S0_IDLE
For CUR_POWER use or
For other PWR_GOOD keep High use
By PM Define FAN name
FAN MODE USE
FAN
GP43 CPUFAN1
GP42 CPUFAN2 PUMPFAN
GP41 SYSFAN1
GP40 SYSFAN2
GP37 SYSFAN3
GP36 SYSFAN4
GP35 SYSFAN5
GP34 SYSFAN6
BIOS SHOW FAN MODE Information USE Default GPI
By PM Define FAN name
SHOW FAN MODE USE
FAN
GP32 CPUFAN1
POWER ON STRAPPING PIN FOR NCT6687D-R
PIN
NAME
Circuit NAME
0
1
Strap Point
31 2E_4E_SEL RTSA# I/O ADDRESS 2E I/O ADDRESS 4E 3VCC
32 DIS_HWACPI DTRA# HW ACPI enable HW ACPI disable 3VA
34 MAF_SEL SOUTA MAF enable MAF disable 3VA
92 DSW_EN DSW_EN DSW disable DSW enable 3VA
96 DDR4_EN SIO_DEBUG DDR4 control disable DDR4 control enable 3VA
9 FAN789_EN (FW setting) GPIO52 FAN789 disable FAN789 enable 3VA
10 P80_EN GPIO53 Port80 LED GPIO 3VA
PIN NAME Circuit NAME VCC3 3VA Strap Point
27 ESPI_EN KBRST# LPC ESPI VCC3 or 3VA
RTCRST_DET
RTC_32K
Y1 AVL:D04-0305500-T16
S0_IDLE
Closed FAN , by S0i3.
JCI1
N31-1020151-H06
DEBUG PORT
For BIOS DEBUG.
If no comp port or JTPM.
0A ~ 10
swap PIN1,PIN2
SPI ROM
0A ~ 10
Change main souce.
15mA
AVL:M31-25X2023-W03
Closed PIN1
Closed PIN99
Closed PIN46,85
3V Analog Power
MICRO-STAR INT'L CO.,LTD
MS-7C92
Size Custom
Document Description
SIO - NCT6687D-R(For AMD)
Rev 11
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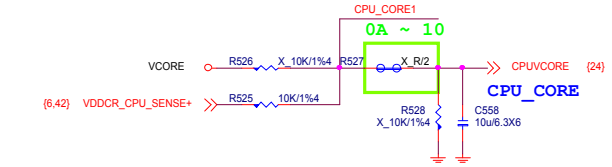
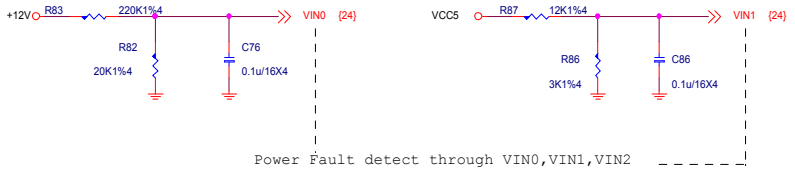
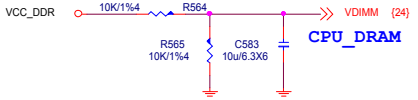
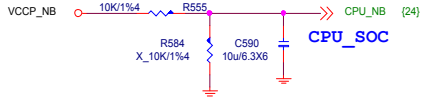
HW Monitor - Voltage

SIO HM Voltage over 2.048V will not detect

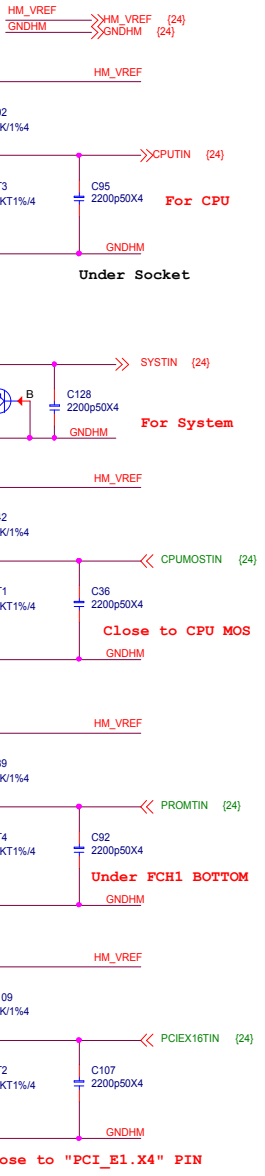








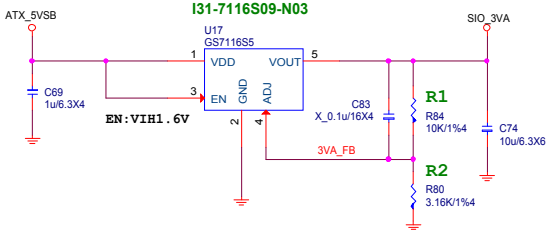
TEMP SENSOR



PM RESET

CPU RESET

SIO_3VA



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.16K))
= 3.33V

MICRO-STAR INT'L CO.,LTD	
MS-7C92	
Size: Custom	Document Description: SIO - HW Monitor
Rev: 11	
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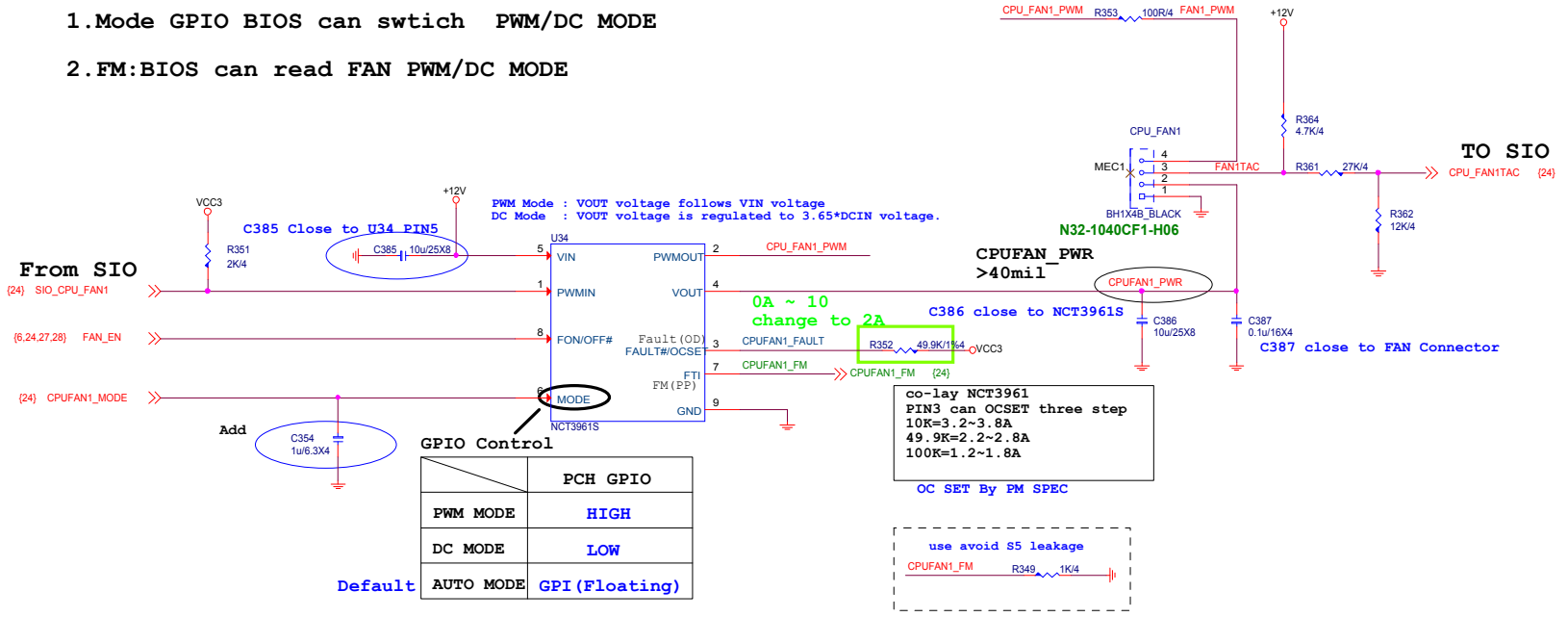
CPUFAN1 TYPE N : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

2.FM:BIOS can read FAN PWM/DC MODE



GPIO Control

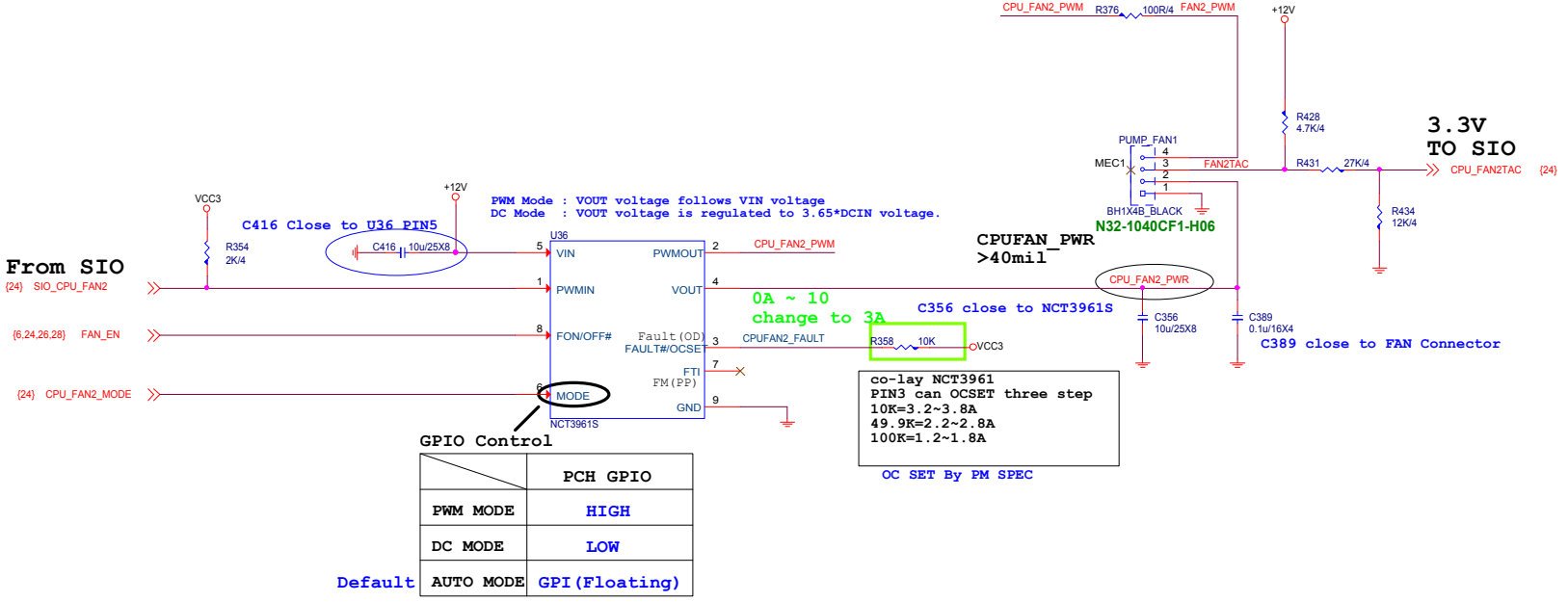
	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD			
MS-7C92			
Size: Custom	Document Description: FAN TYPE-N CPUFAN1		Rev: 11
Date: Wednesday, June 10, 2020		Sheet 26 of 66	

PUMPFAN1

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD	
MS-7C92	
Size: Custom	Document Description: FAN TYPE-M PUMPFAN1
Rev: 11	
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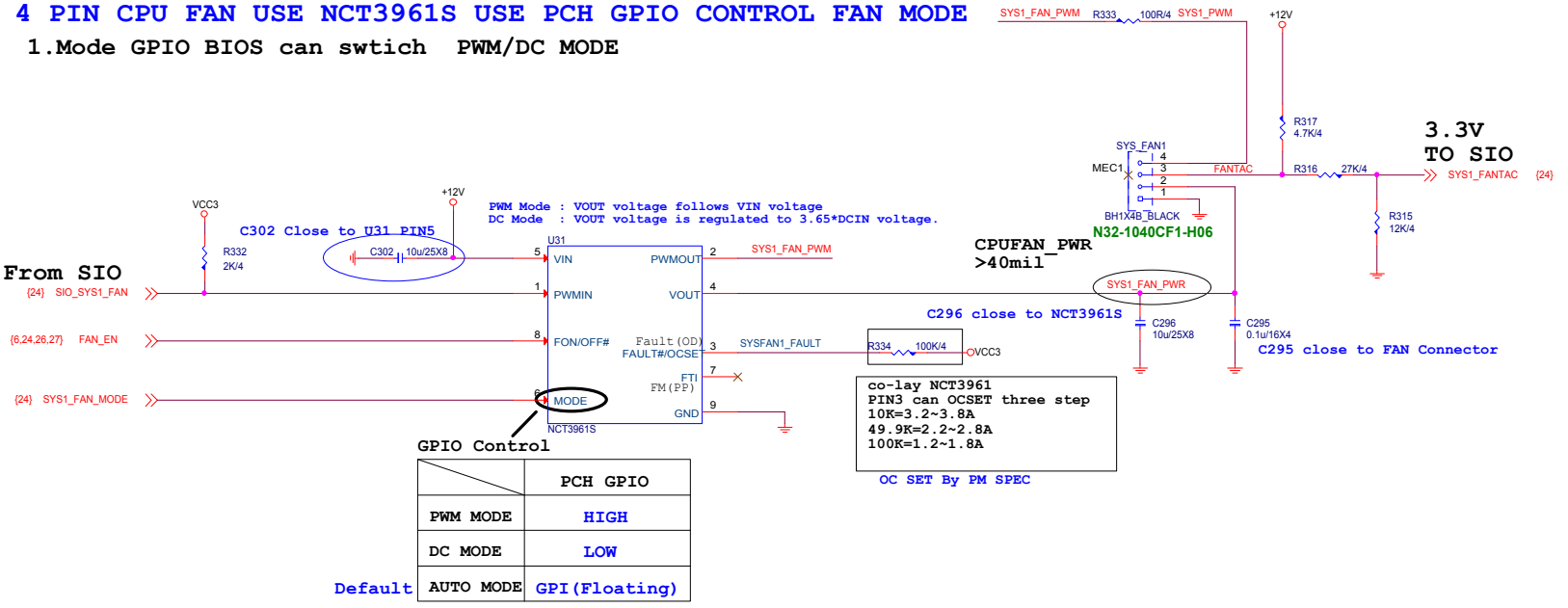
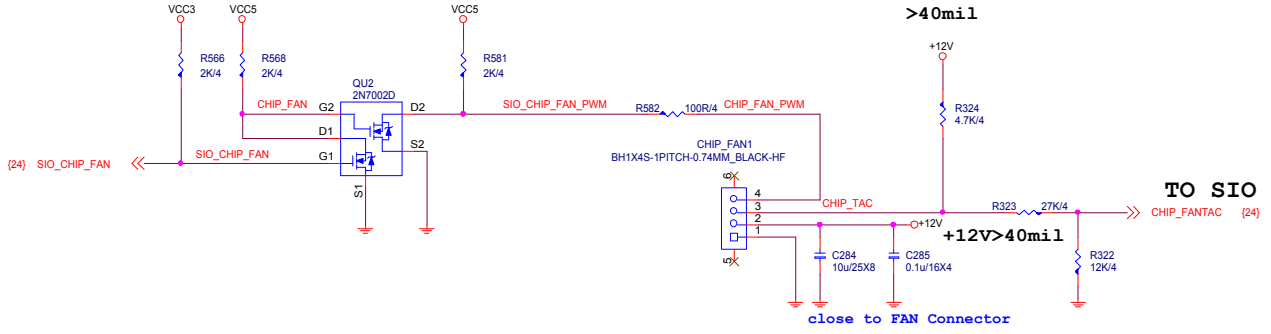
SYSFAN1

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)



MICRO-STAR INT'L CO.,LTD

MS-7C92

Size	Document Description	Rev
Custom	FAN TYPE-M SYSFAN1	11

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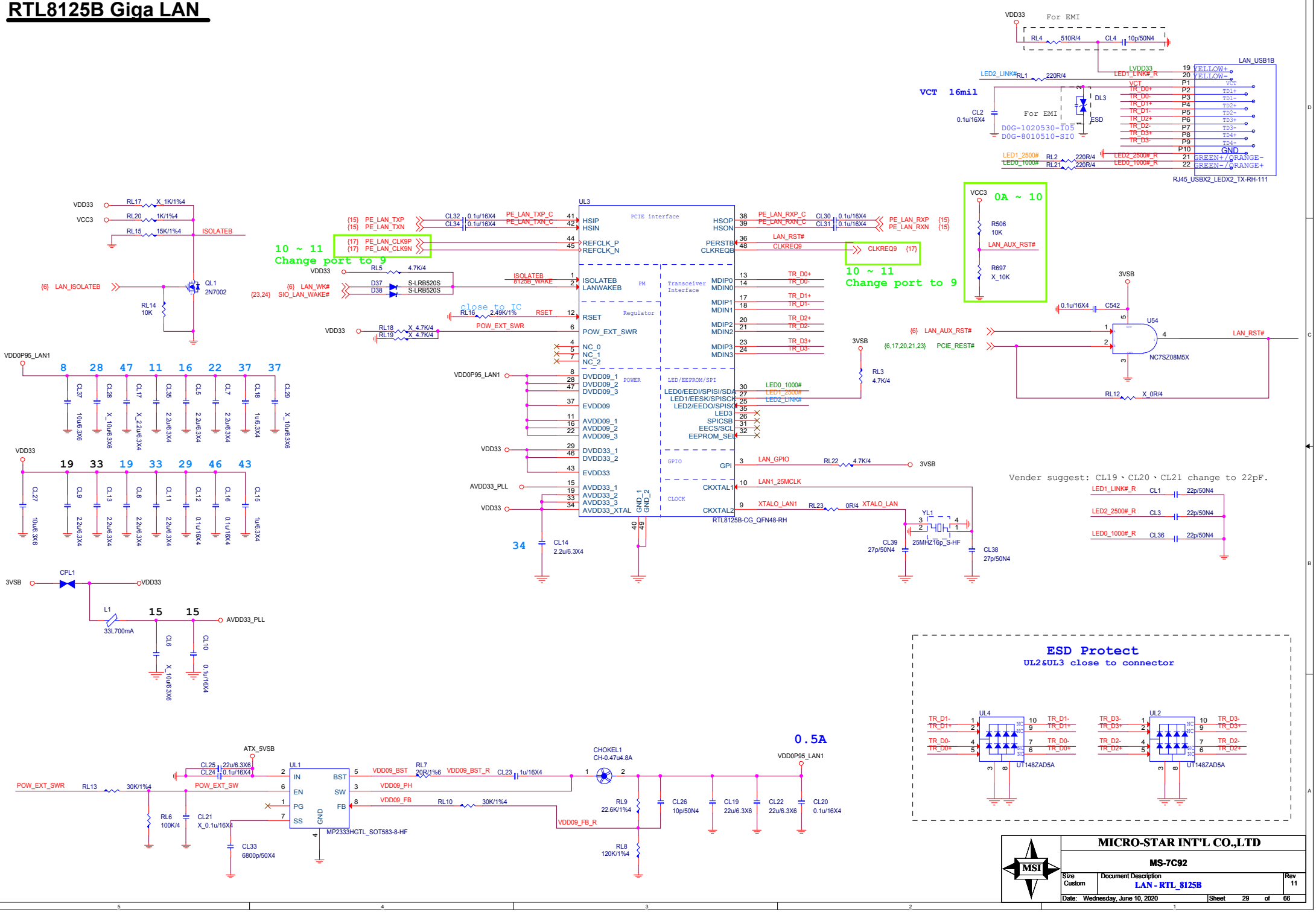
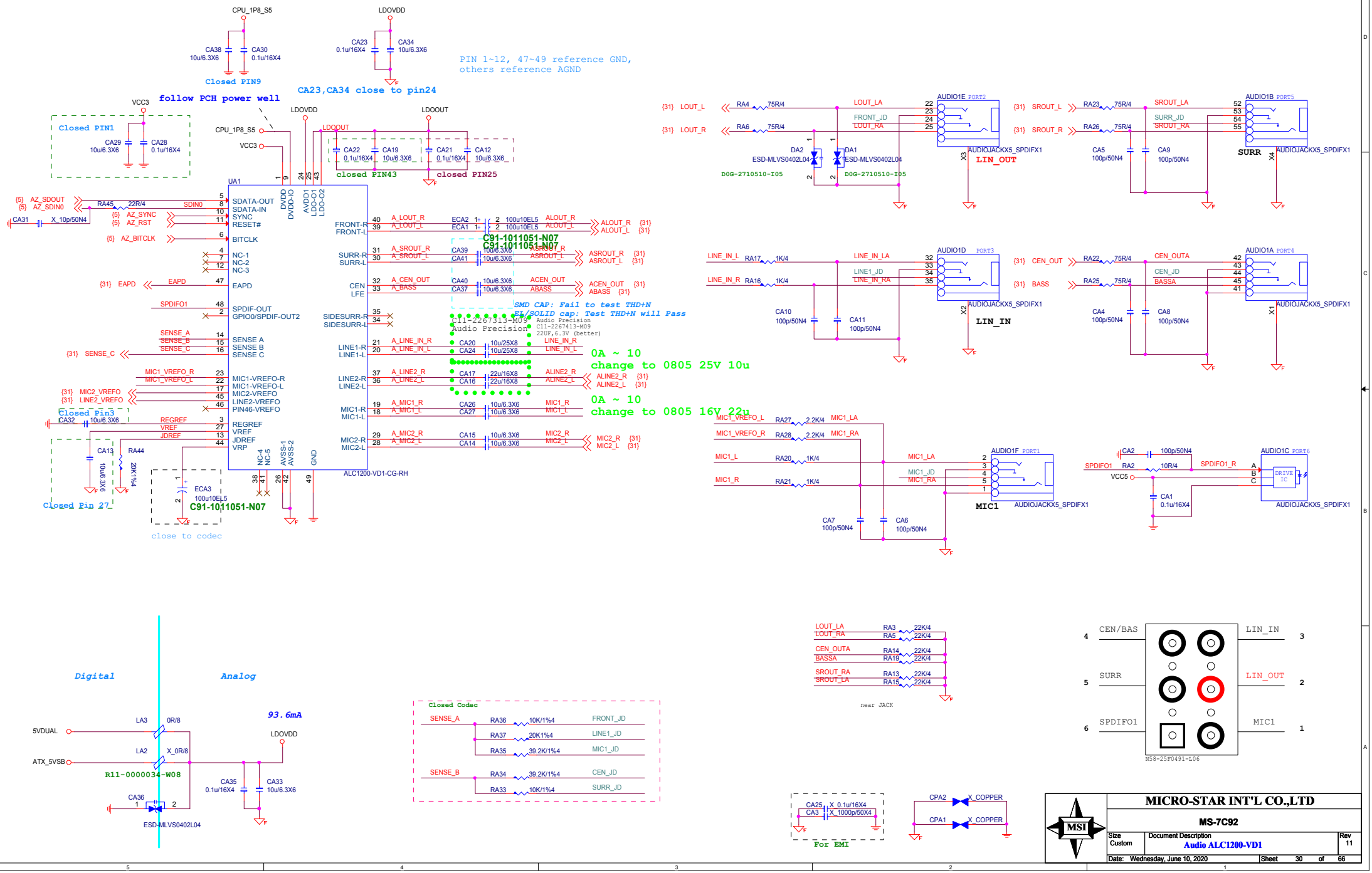
RTL8125B Giga LAN



ALC1200-VD1_48PIN



MICRO-STAR INT'L CO.,LTD

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Custom	Audio ALC1200-VD1	11

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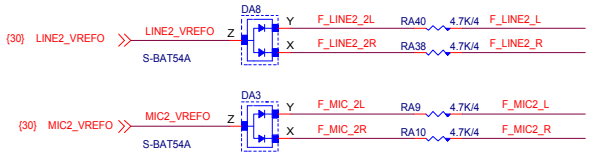
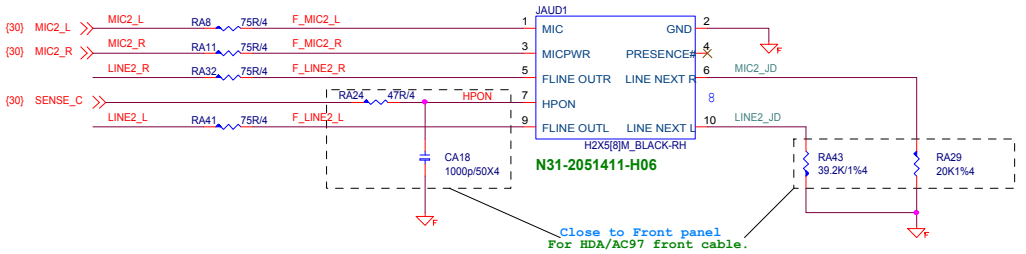
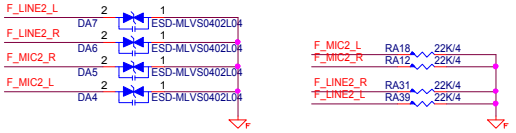




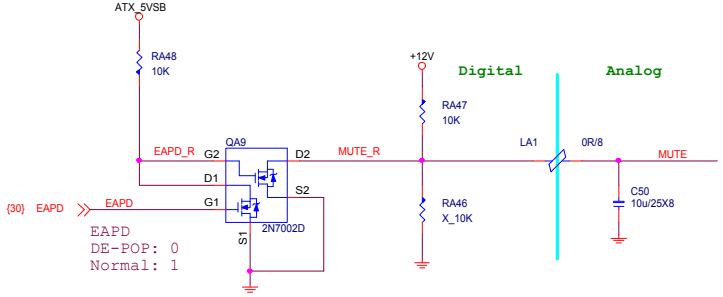
D0G-2710510-I05
Close to Front panel

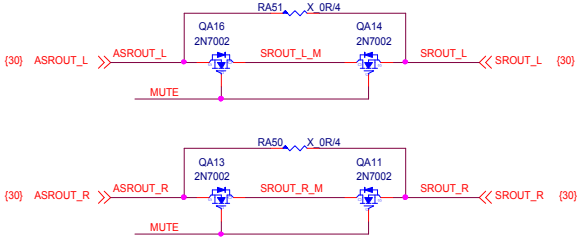
ESD protect

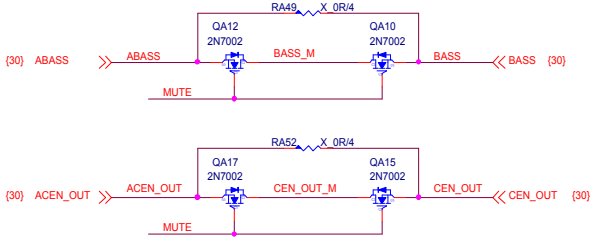
D0G-2710510-I05
AVL:D0G-2950500-SI0

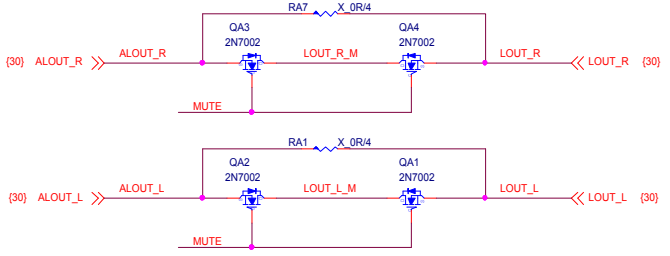


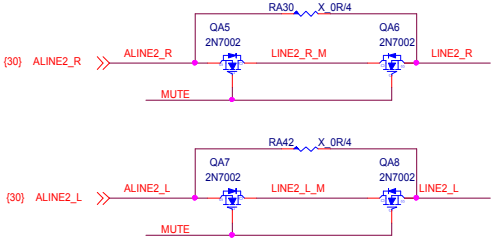
De-POP circuit











MICRO-STAR INT'L CO.,LTD

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Custom	Audio DePoP	11

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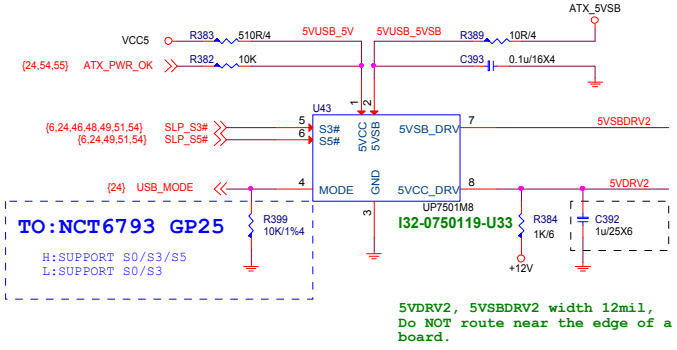
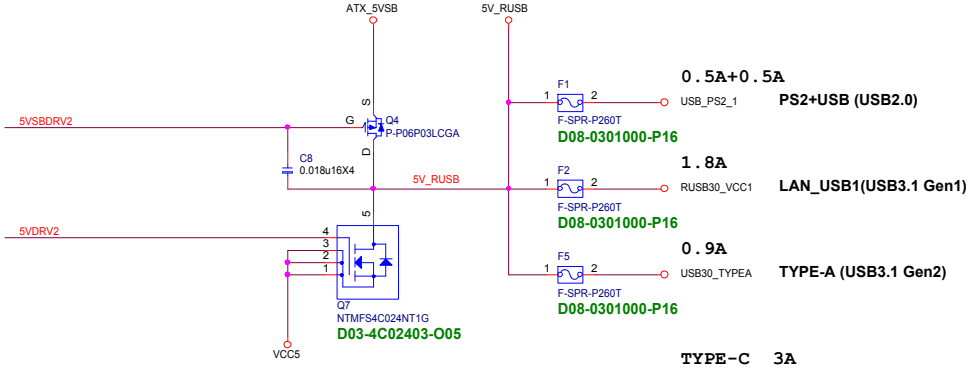
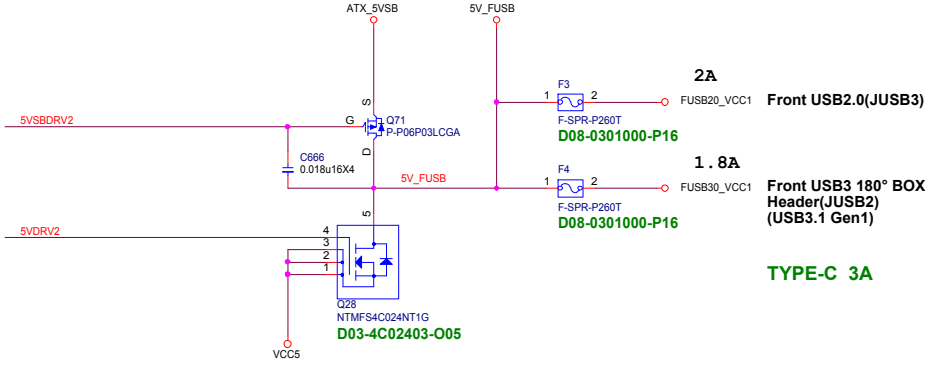
USB Power





Rear (7.2A)

Front (6.8A)



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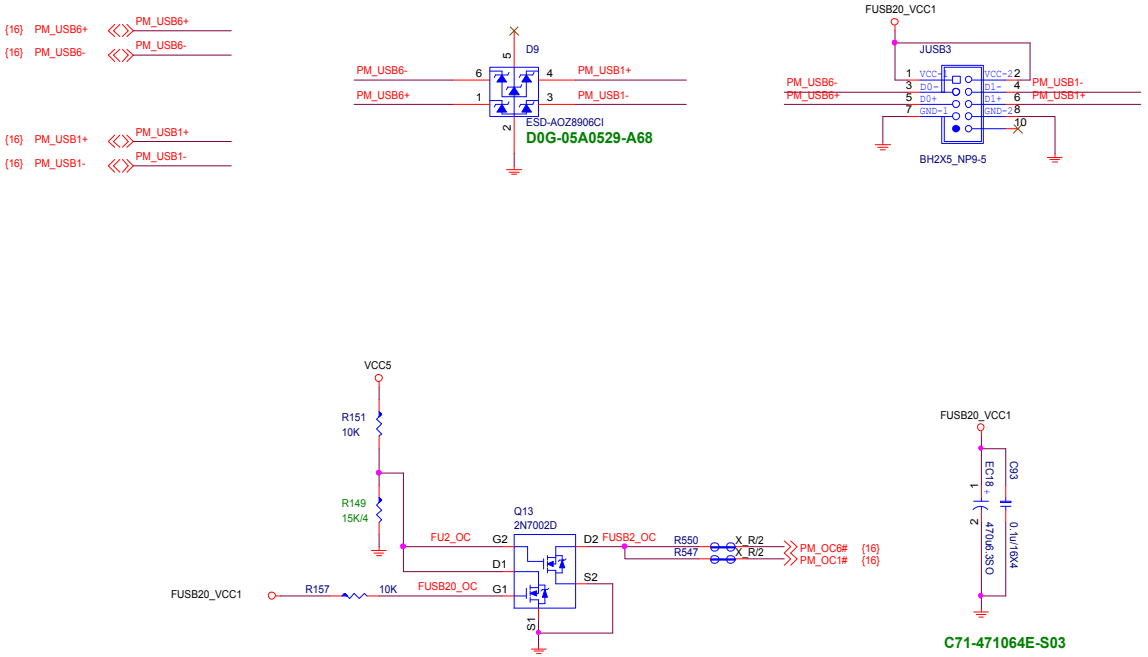
Front USB2.0(JUSB3)

Form GL850G USB2.0 HUB

5V@1A



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MS-7C92		
Size: Custom	Document Description: Front USB2.0 Header	Rev: 11
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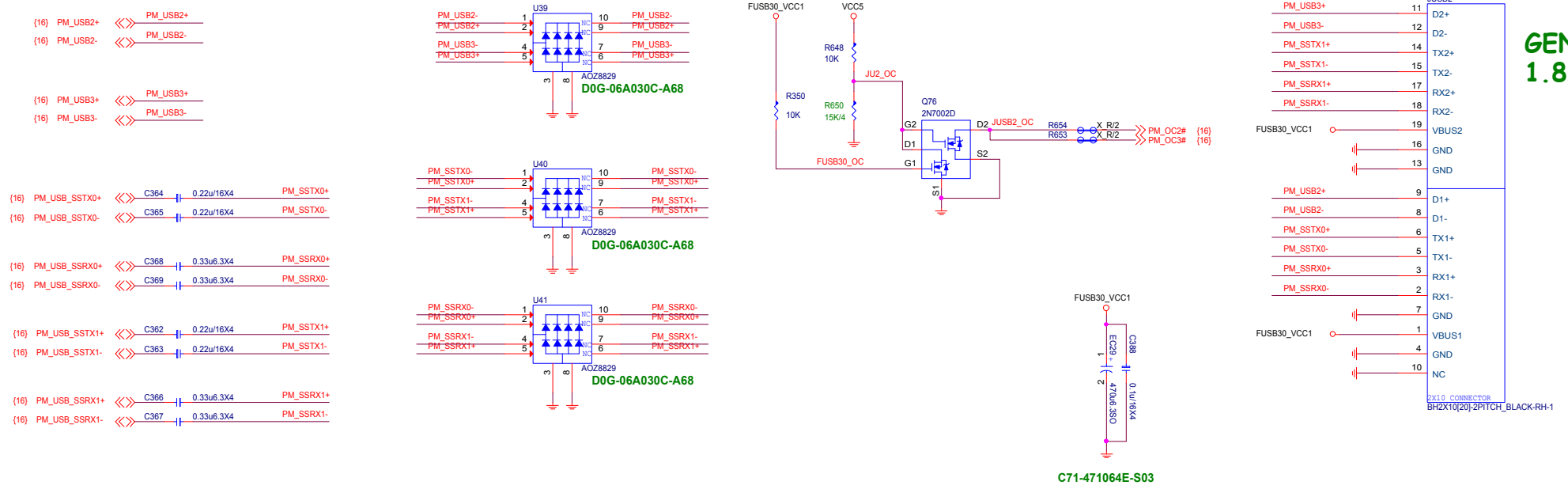
Front USB3 180° BOX
Header(JUSB2)
5V@1.8A



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MS-7C92	
Size: Custom	Document Description: Front USB3.0 Header
Rev: 11	
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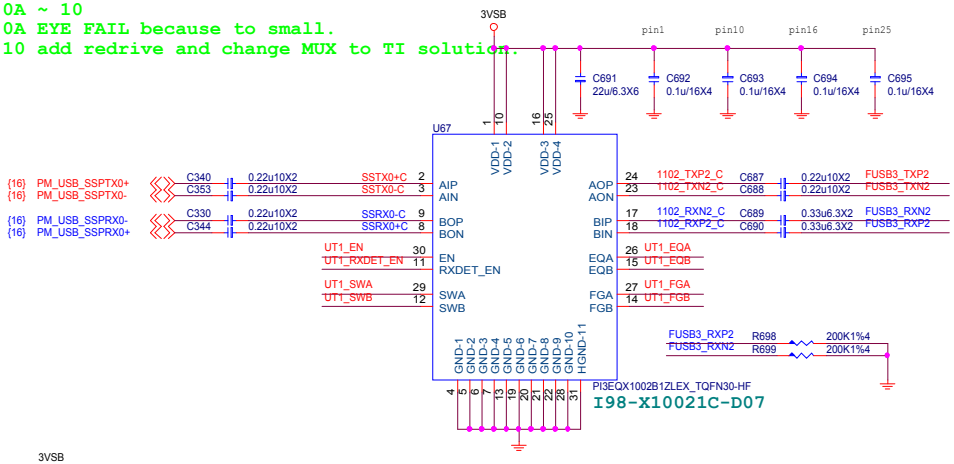
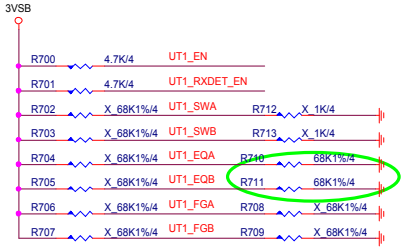
0A ~ 10
0A EYE FAIL because to small.
10 add redrive and change MUX to TI solution.

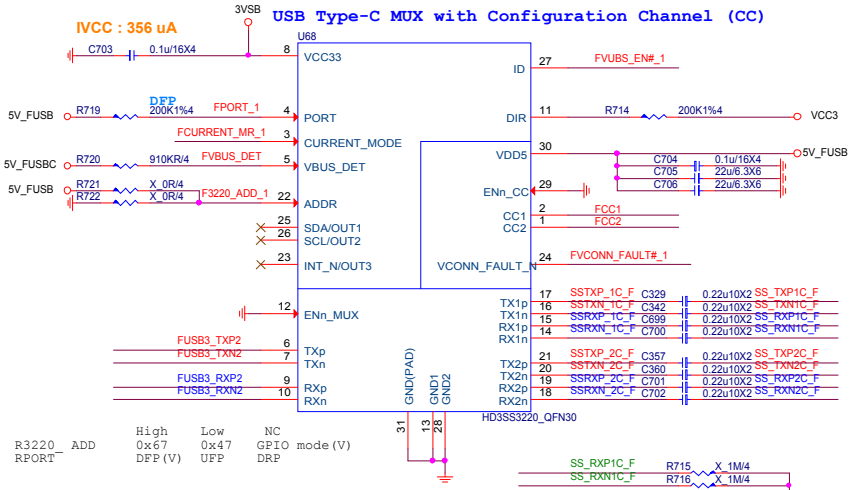




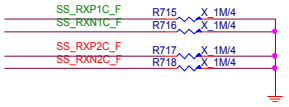
	HIGH	LOW
EN	Normal operation	Power down mode
RXDET_EN	Receive Enable	Receive Disable

IVCC : 356 uA

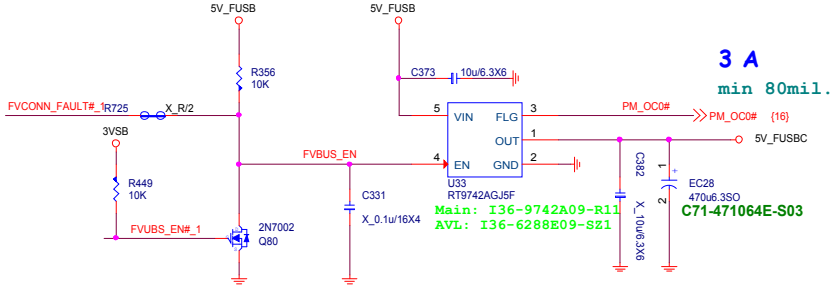
USB Type-C MUX with Configuration Channel (CC)



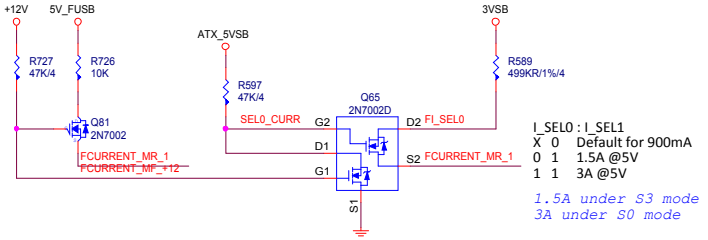
R3220_ ADD RPORT	High	Low	NC
	0x67	0x47	GPIO mode(V)
	DFP(V)	UFP	DRP

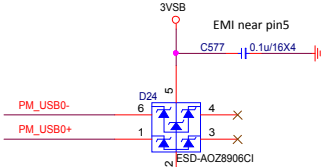


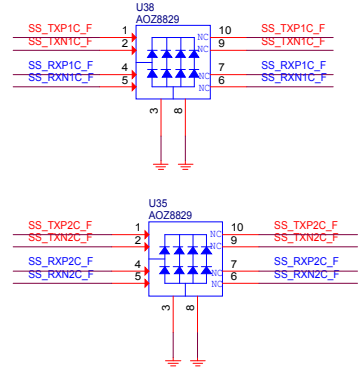
VBUS EN

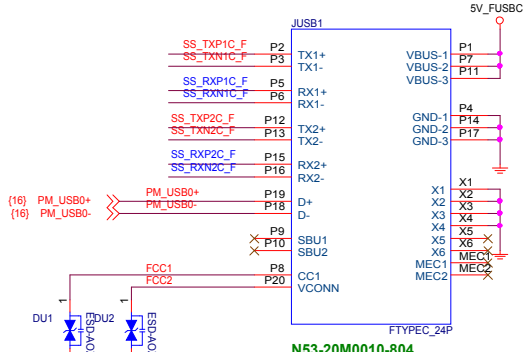


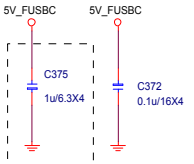
Current Mode











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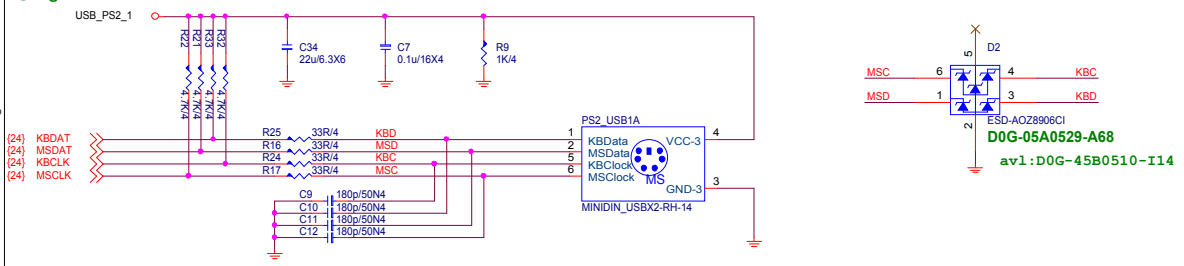
PS2+USB (USB2.0)

5V@1A

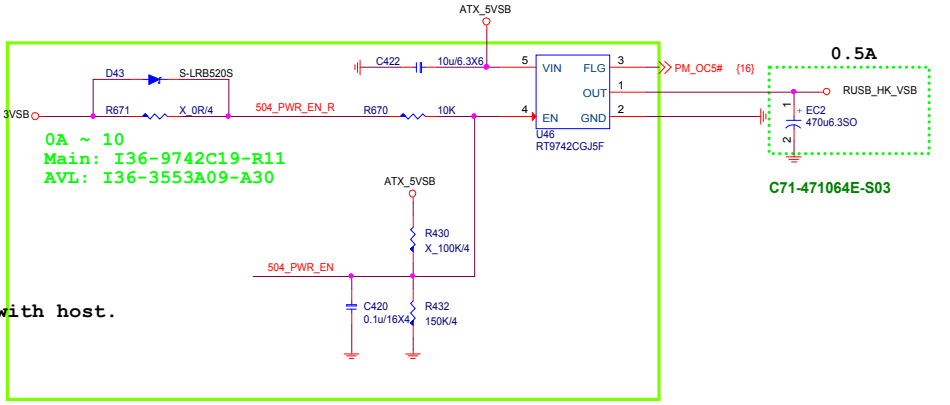
layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch



D0G-05A0529-A68

avl:D0G-45B0510-I14

HOTKEY POWER



0A ~ 10

Main: I36-9742C19-R11

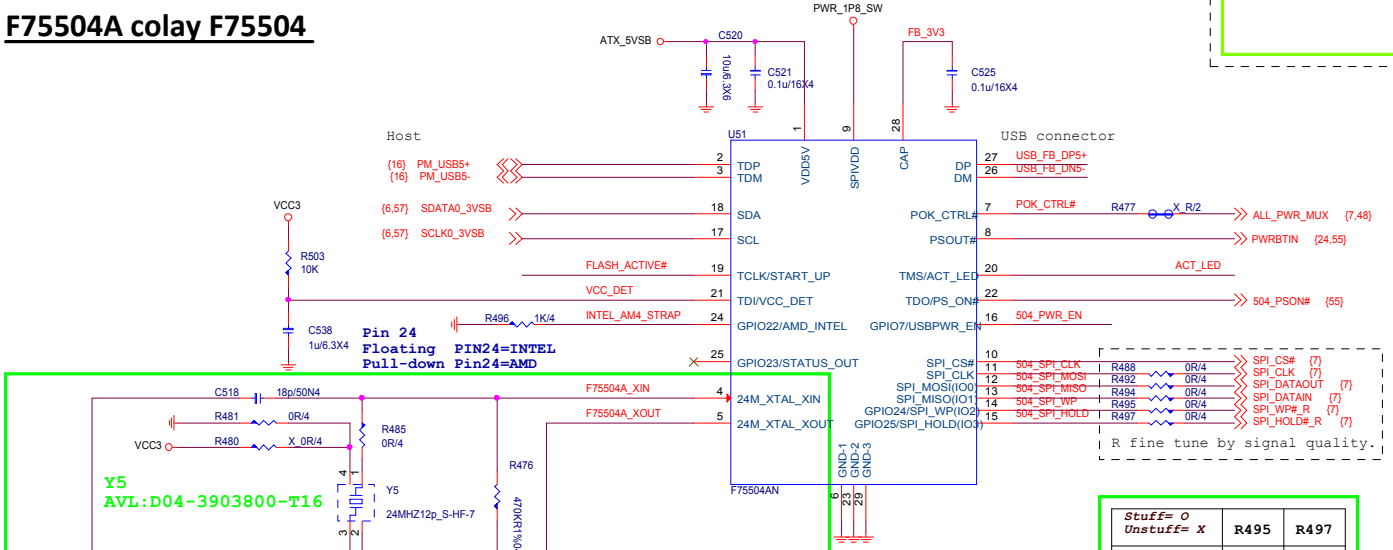
AVL: I36-3553A09-A30

C71-471064E-S03

USB Flash BIOS

F75504A colay F75504

F75504A/F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.



Pin 24 Floating PIN24=INTEL Pull-down Pin24=AMD

R fine tune by signal quality.

Y5

AVL:D04-3903800-T16

R498, R499,R40 placed close to Crystal side

Don't have the branches

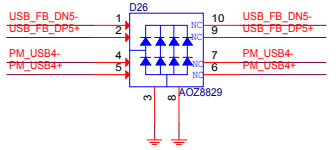
R503 placed close R40

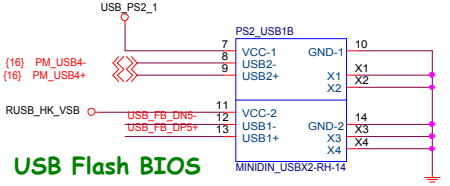
Stuff= O Unstuff= X	R485	R493	R499	R500	C518	R481	R480	R476	Y5
F75504A	O	O	X	X	10pF	0R	X	O	D04-3902700-F07
F75504	X	X	O	O	X	0.1uF	O	X	D05-1100600-F07

Stuff= O Unstuff= X	R495	R497
F75504A	O	O
F75504	X	X

2019/06/17

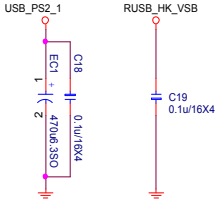
ESD close to connector.





USB Flash BIOS

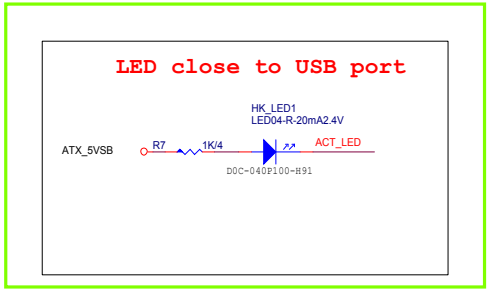
1A

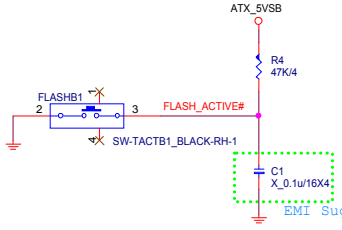


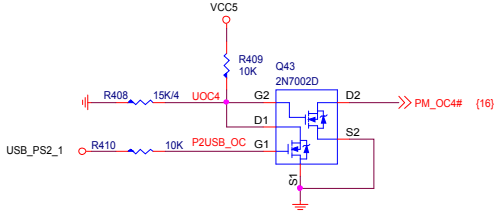
C71-471064E-S03

0A ~ 10

not support ALL LED OFF , remove 2n7002.







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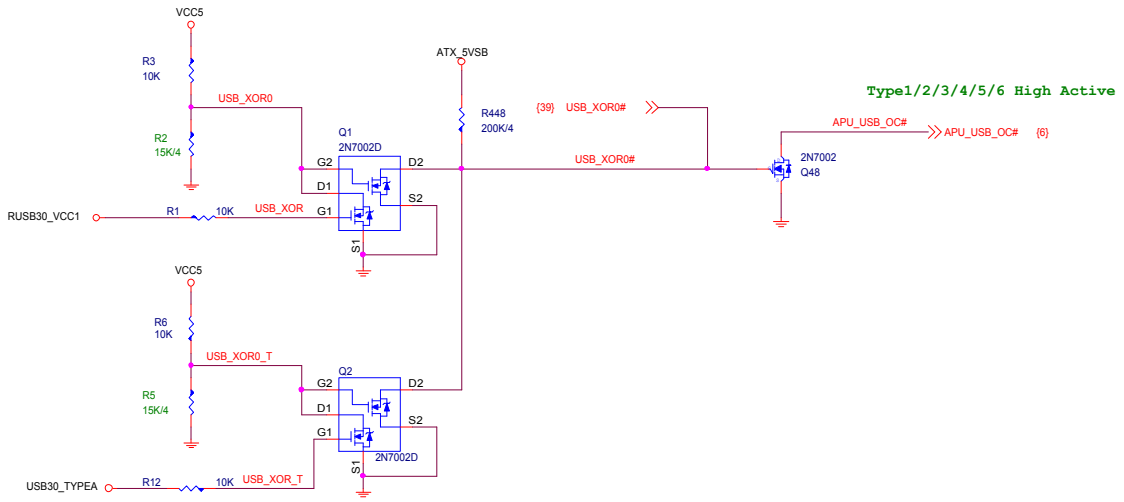
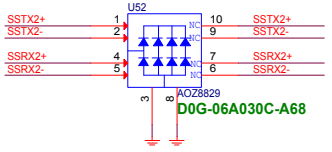
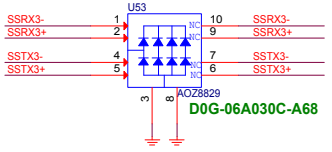
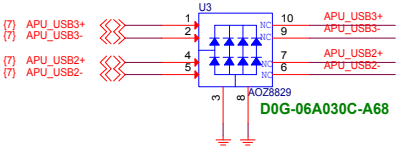
CPU USB_OC

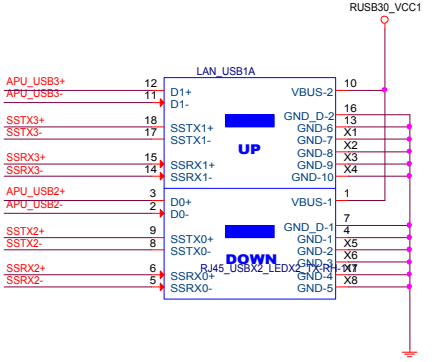


Rear USB3.1 GEN1 5V@1.8A

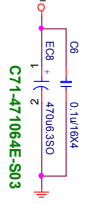








1.8A



MSI	MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: Rear USB3.1	Rev: 11
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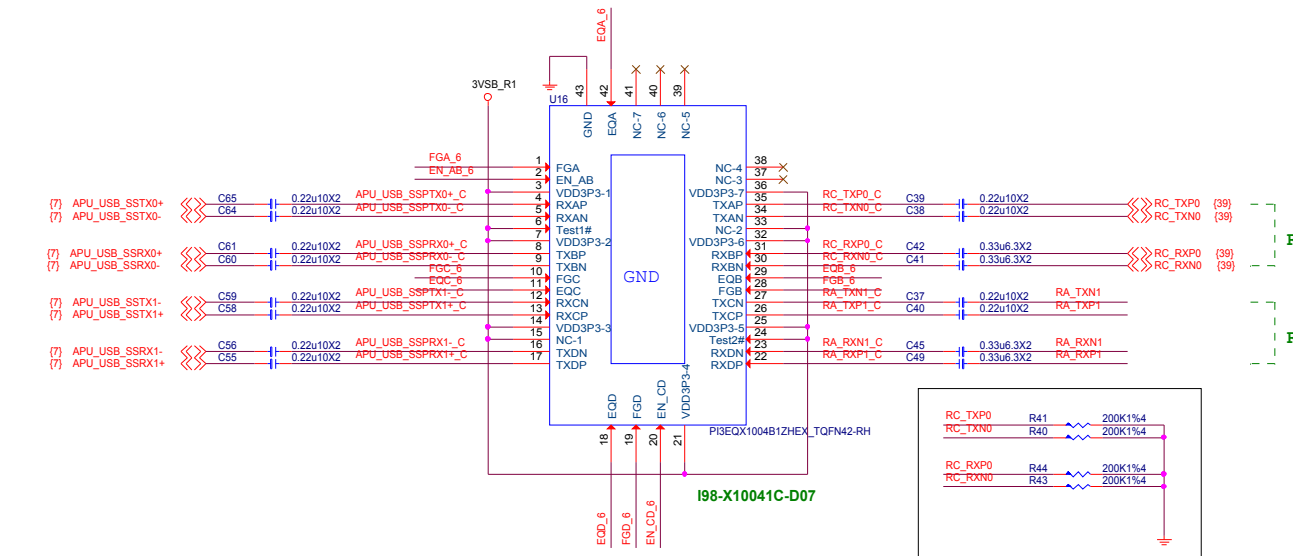
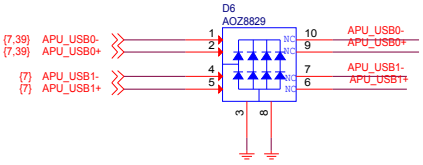
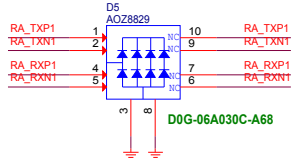
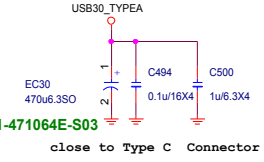
TYPE-A

PI3EQX1004 Redriver

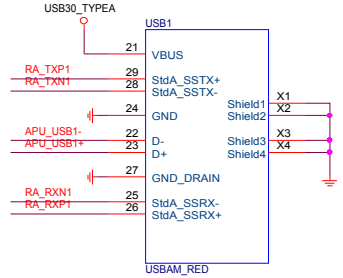


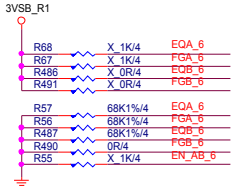


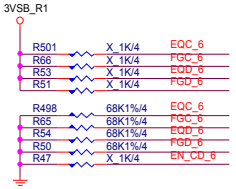


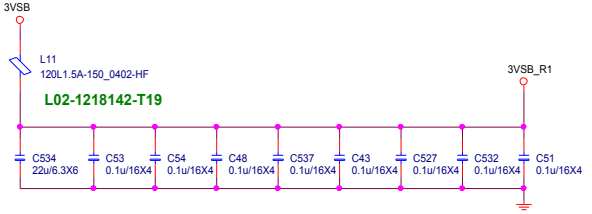


GEN2 0.9A









EQ	dB	
0	10.9	0 to GND
R	6.7	68K to GND
F	8.9	NC
1	13.1	0 to VDD

		EQ	FG
USB3_TX4	A	R	F
USB3_RX4	B	R	L
USB3_TX3	C	R	F
USB3_RX3	D	R	L

FG	dB	
0	-3	0 to GND
R	-1.5	68K to GND
F	0	NC
1	2	0 to VDD

MICRO-STAR INT'L CO.,LTD

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Custom	Rear USB3.1 Type A / Redrive	11

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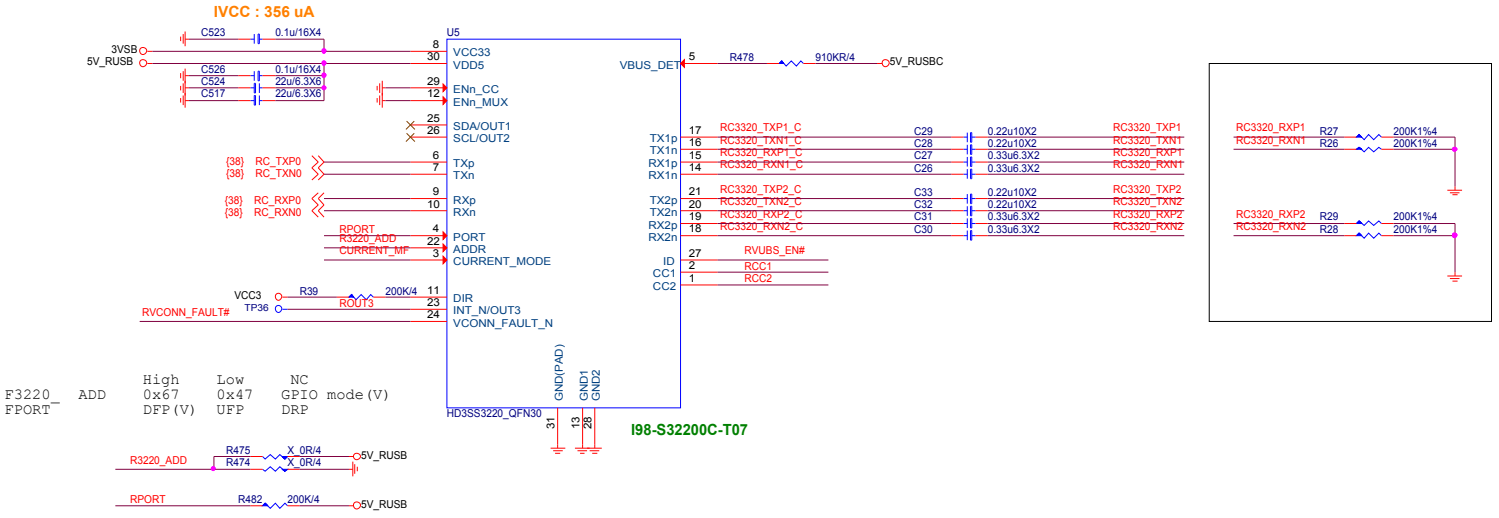
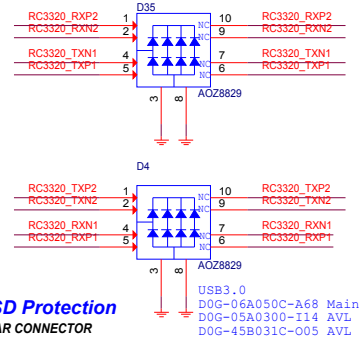
USB 3.1-Type-C

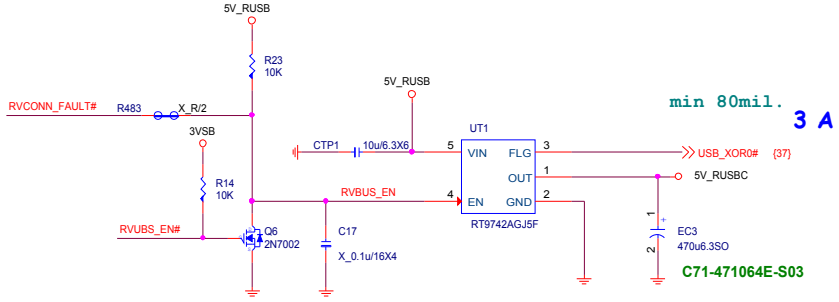
USB Type-C MUX with Configuration Channel (CC)



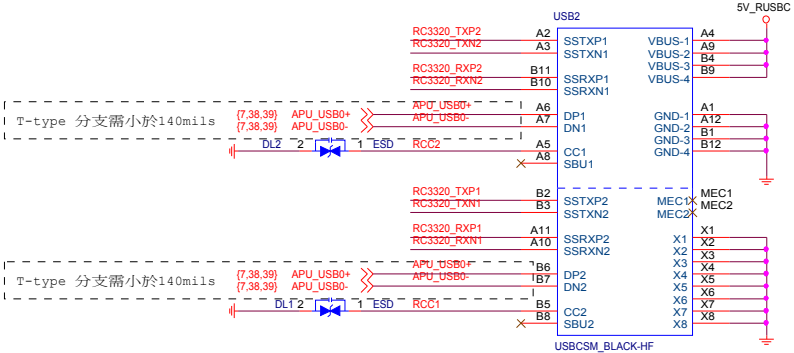


ESD Protection
NEAR CONNECTOR

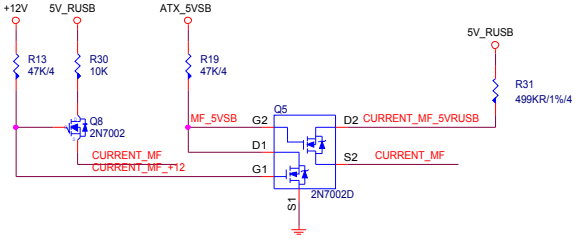
VBUS EN



GEN2 3A



Current Mode



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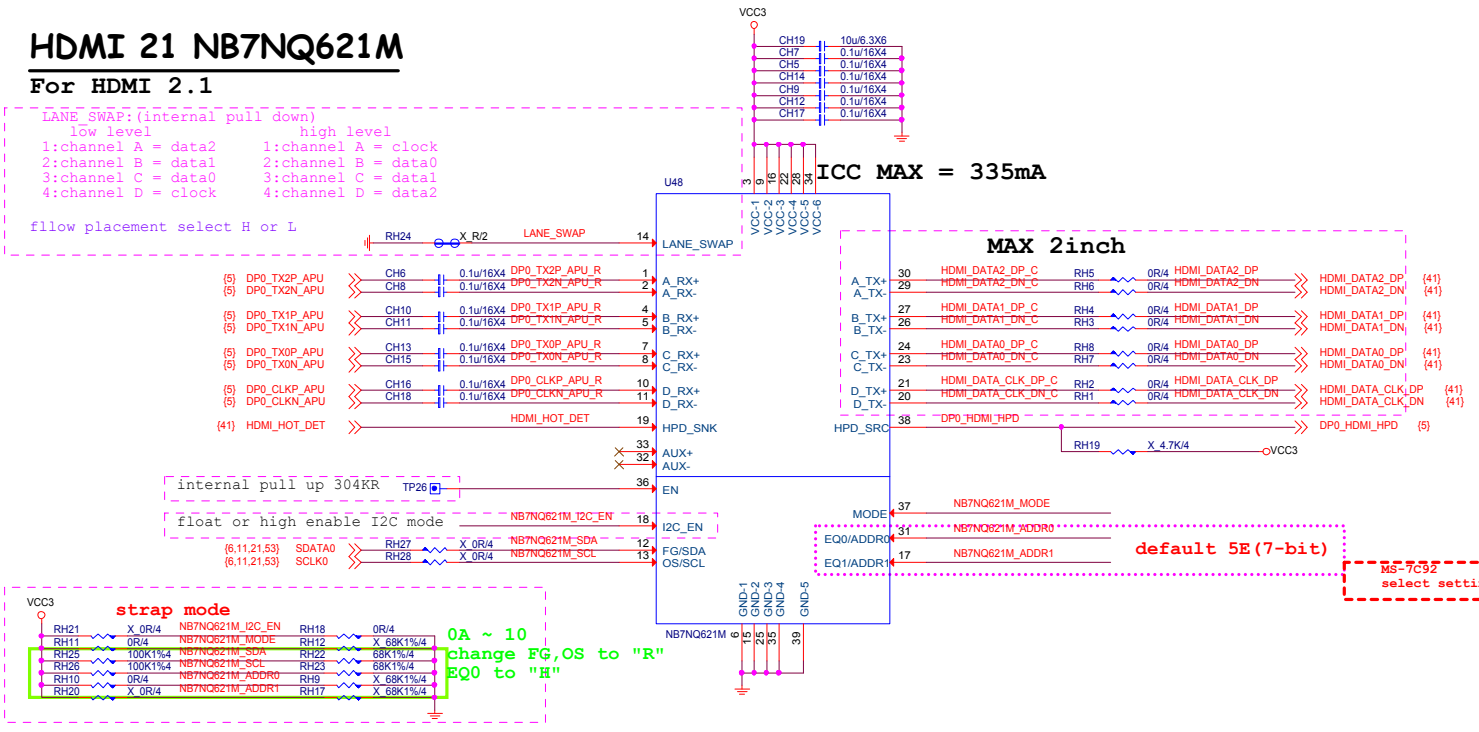
HDMI 21 NB7NQ621M

For HDMI 2.1



Pin Setting	Voltage	Level
mode	3.3	H
EQ0	3.3	H
FG	1.1	R
OS	1.1	R
EQ1	2.2	F
I2C	0	L

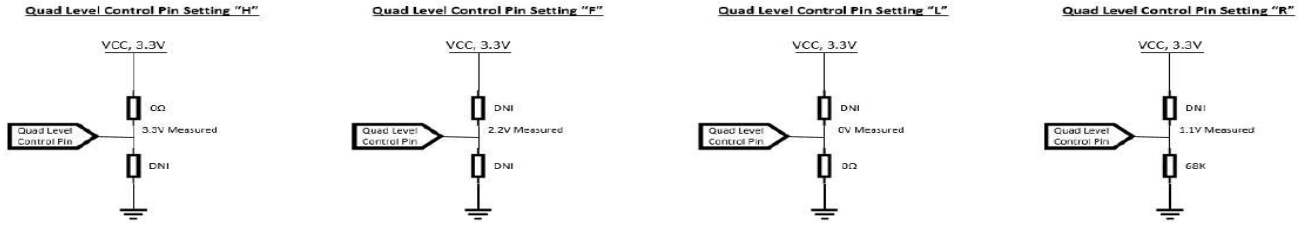


Figure 4. NB7NQ621M Required Implementation for Quad Level Pin Strapping Pins: EQ0/ADDR0, EQ1/ADDR1, I2C_EN, and MODE

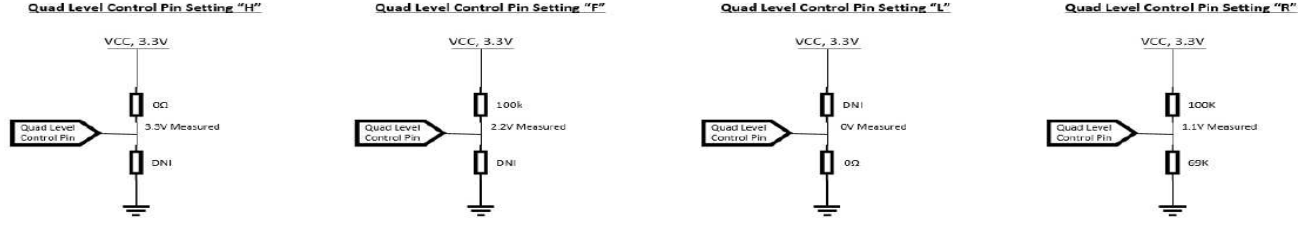


Figure 5. NB7NQ621M Required Implementation for Quad Level Pin Strapping Pins: FG and OS

Table 9: GPIO Device Slave Address Settings

Quad-Level Input ADDR1	Quad-Level Input ADDR0	7 Bit Slave Address							HEX Slave Address: (7-bit)	W/R	HEX Address: (W/R=0)	HEX Address: (W/R=1)
L	L	1	0	1	0	1	0	0	54	0/1	A8	A9
L	R	1	0	1	0	1	0	1	55	0/1	AA	AB
L	F	1	0	1	0	1	1	0	56	0/1	AC	AD
L	H	1	0	1	0	1	1	1	57	0/1	AE	AF
R	L	1	0	1	0	0	0	0	50	0/1	A0	A1
R	R	1	0	1	0	0	0	1	51	0/1	A2	A3
R	F	1	0	1	0	0	1	0	52	0/1	A4	A5
R	H	1	0	1	0	0	1	1	53	0/1	A6	A7
F	L	1	0	1	1	1	0	0	5C	0/1	B8	B9
F	R	1	0	1	1	1	0	1	5D	0/1	BA	BB
F (Default)	F (Default)	1	0	1	1	1	1	0	5E	0/1	BC	BD
F	H	1	0	1	1	1	1	1	5F	0/1	BE	BF
H	L	1	0	1	1	0	0	0	58	0/1	B0	B1
H	R	1	0	1	1	0	0	1	59	0/1	B2	B3
H	F	1	0	1	1	0	1	0	5A	0/1	B4	B5
H	H	1	0	1	1	0	1	1	5B	0/1	B6	B7

FOR MSI USE ONLY

Table 14. EQUALIZATION SETTINGS TABLE FOR PIN STRAP MODE 3 (Typical)

Equalization Setting #	EQ1	EQ0	EQ Gain [dB] @ 0.825 GHz	EQ Gain [dB] @ 1.7 GHz	EQ Gain [dB] @ 3 GHz
0	L	L	1.7	3.2	5.7
1	L	R	1.9	3.4	6.1
2	L	F	2.1	3.7	6.6
3	L	H	2.3	4.0	6.9
4	R	L	2.4	4.3	7.5
5	R	R	2.5	4.6	8.3
6	R	F	2.7	4.9	8.8
7	R	H	3.0	5.4	9.4
8	F	L	0.5	1.0	1.9
9	F	R	0.7	1.2	2.3
10 (Default)	F	F	0.9	1.6	2.8
11	F	H	1.0	2.0	3.6
12	H	L	1.2	2.3	4.1
13	H	R	1.3	2.5	4.4
14	H	F	1.4	2.7	4.8
15	H	H	1.6	2.9	5.2

MS-7C92 select setting 11

Table 10. MODE OF OPERATION SETTINGS TABLE FOR PIN STRAPPING

Mode of Operation	I2C_EN	MODE Pin	Standard	Configuration	Termination	Data Rate [Gbps]
0	L	L	HDMI	TMDS (DC Coupled Outputs)	High–Z, line to line	0.25 – 1.65
1	L	R	HDMI	TMDS (DC Coupled Outputs)	300 Ω, line to line	1.65 – 3.4
2	L	F	HDMI	TMDS (DC Coupled Outputs)	200 Ω, line to line	1.65 – 3.4
3	L	H	HDMI	TMDS (DC Coupled Outputs)	100 Ω, line to line	3.4 – 6
4	R	L	HDMI	FRL (DC Coupled Outputs)	100 Ω, line to line	3 – 12
5	R	F	HDMI	FRL (AC Coupled Outputs)	50 Ω to VCC	3 – 12
6	R	H	DisplayPort	ML (AC Coupled Outputs)	50 Ω to VCC	2.7 – 8.1
I²C	F (Default)/H	X	I²C is Enabled for these combinations. Pin Strap–Mode is Disabled.			

MS-7C92 select mode3

Table 20. FLAT GAIN, SETTINGS TABLE FOR PIN STRAP MODE 3–6 (Typical)

Setting #	Pin Strap Setting	Flat Gain @ 100 MHz
0 (Default)	L	0.5 dB
1	R	2.4 dB
2	F	1.1 dB
3	H	4 dB

MS-7C92 setting 1

Table 21. OUTPUT SWING, SETTINGS TABLE FOR PIN STRAP MODE (Typical)

Setting #	Pin Strap Setting	Output Swing @ 100 MHz
0 (Default)	L	1000 mV
1	R	1200 mV
2	F	800 mV
3	H	1400 mV

MS-7C92 setting 1

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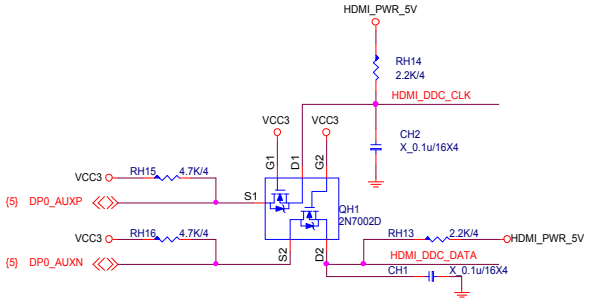
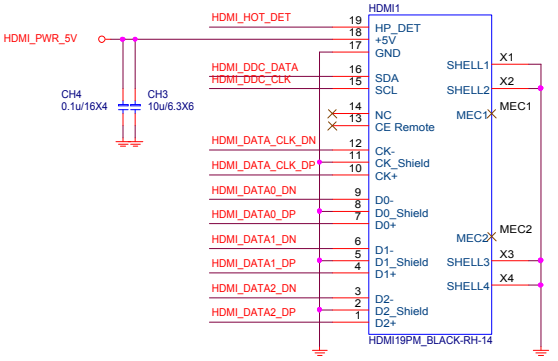
HDMI 2.1 Connector

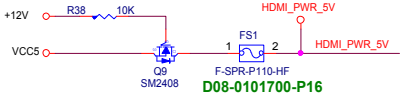
AUX Level Shifter



Connector



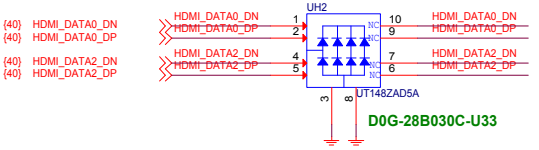
Connector Power



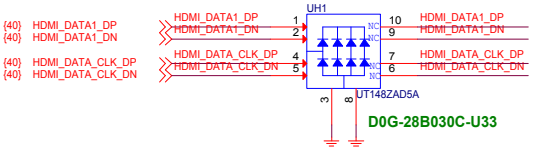
D08-0101700-P16

如果用DIODE SA測試電壓會不過

For EMI

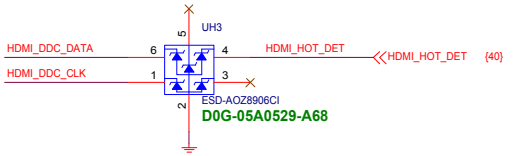


D0G-28B030C-U33



D0G-28B030C-U33

注意:耐壓5v零件



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Note:VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VCORE: ICCMax 140A
LL: 1.3mohm
OCP: 8*40A=320A

SOC: ICCMax 75A
LL: 2.1ohm
OCP: 100A

ADDR = 0V
SMBUS address:0X20(7 bit)
0X40(8 bit)

0A ~ 10
remove VR6

0A ~ 10
remove 0R

0A ~ 10
Change to GS7133
for OTP issue
And add VQ5
for leakage VCC3_86936 to VCC5 issue

80mA

120mA

I31-7133S02-N03

AVL:I31-3730S02-N62

Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(31.6K/10.2K))
= 3.328V

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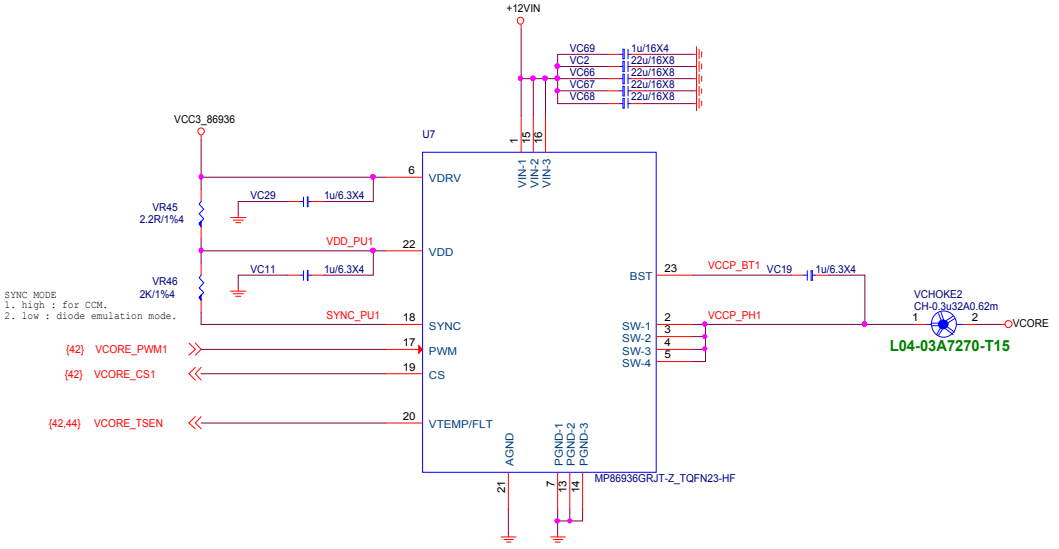
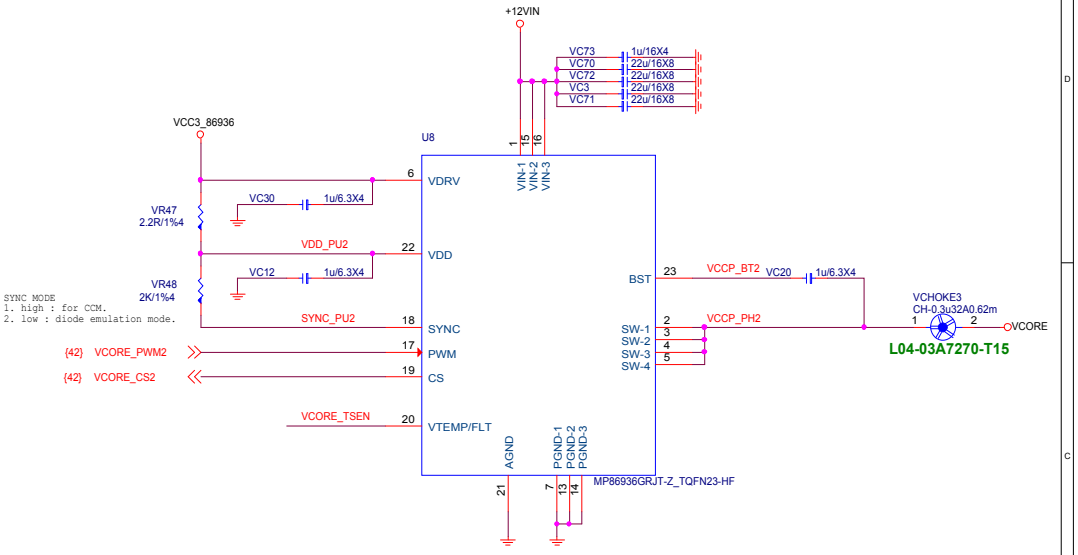
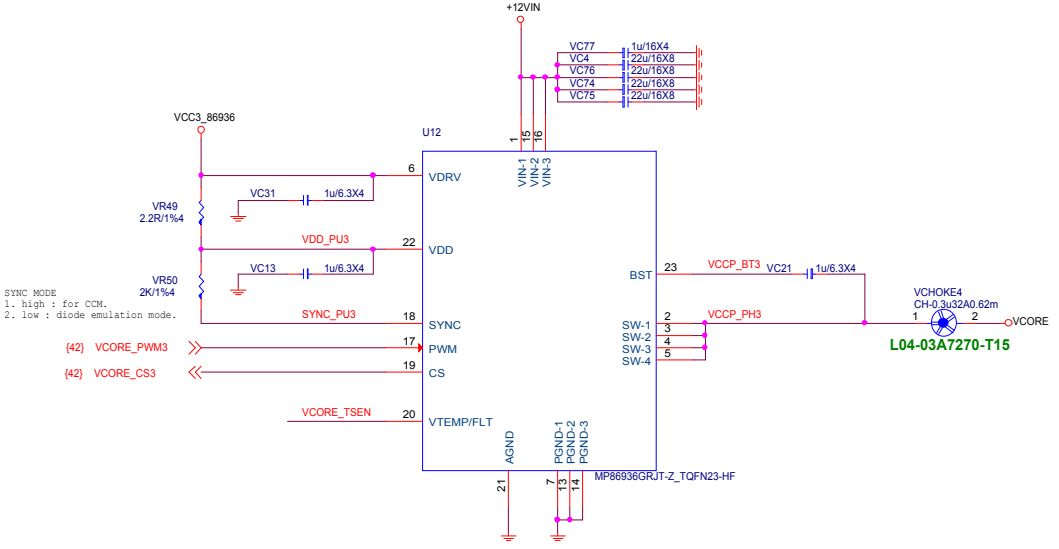
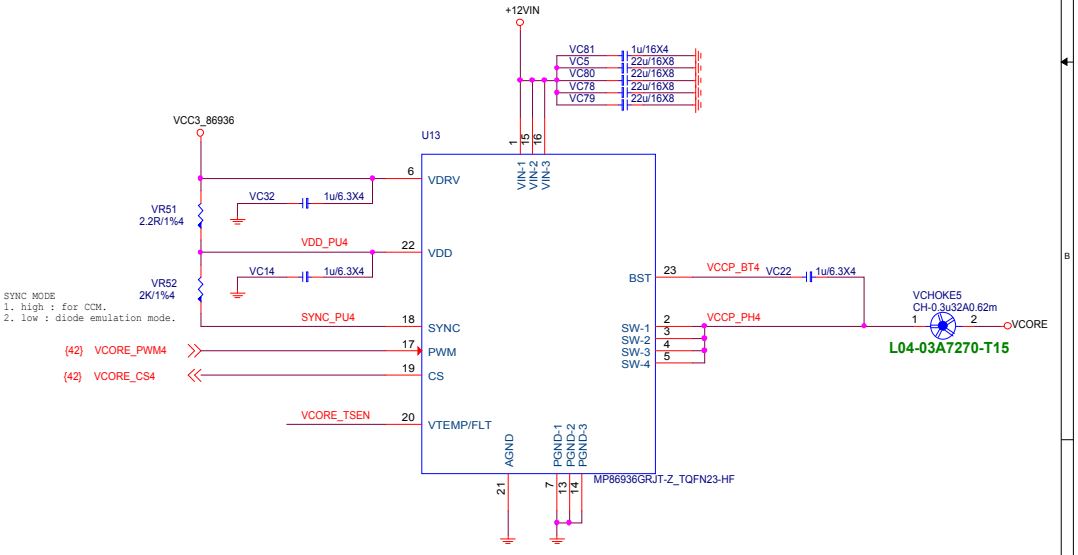
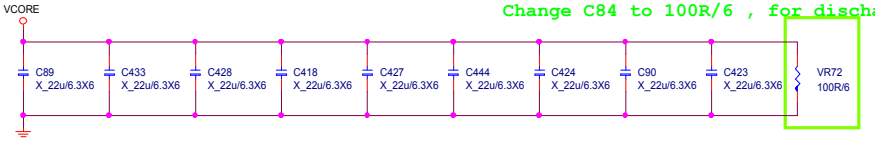
Vcore EDC Max 140A



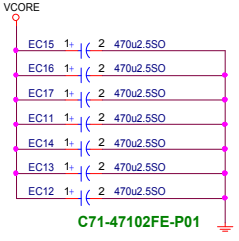








0A ~ 10
Change C84 to 100R/6 , for discharge.



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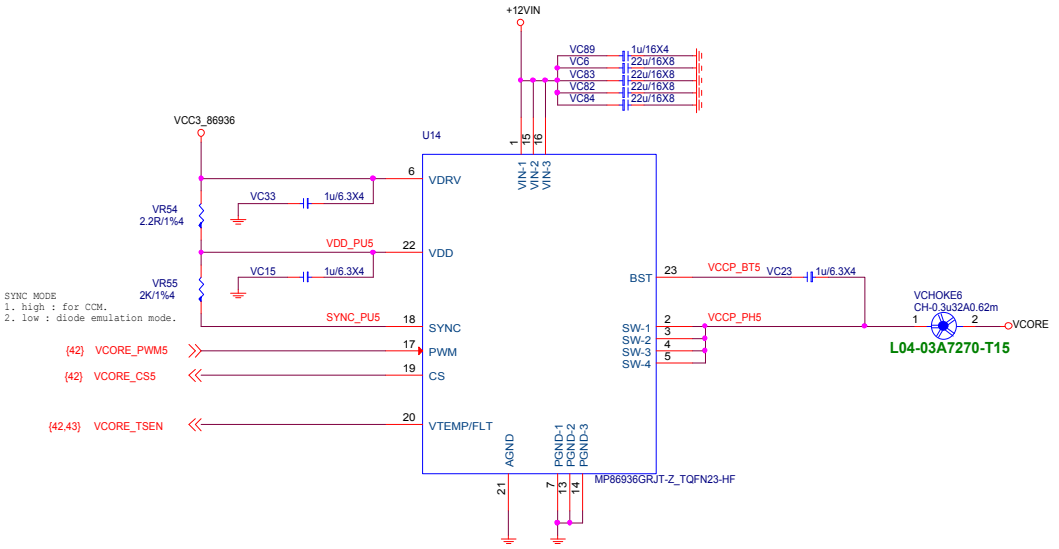
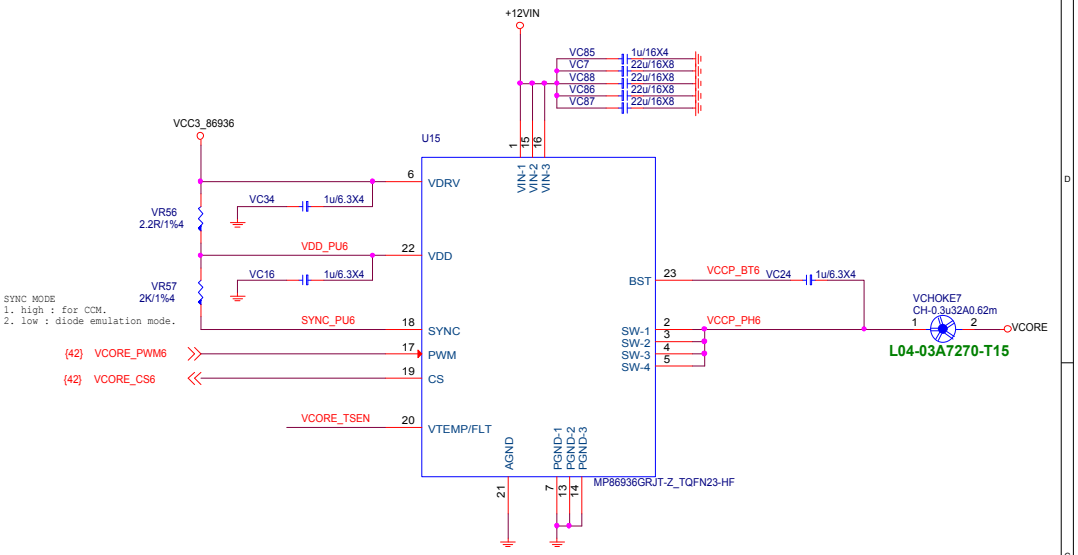
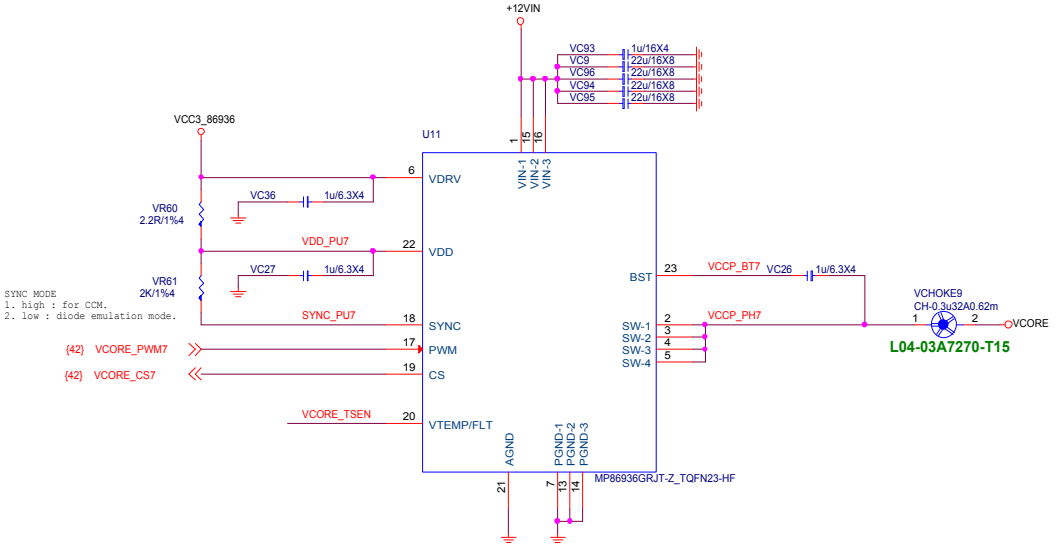
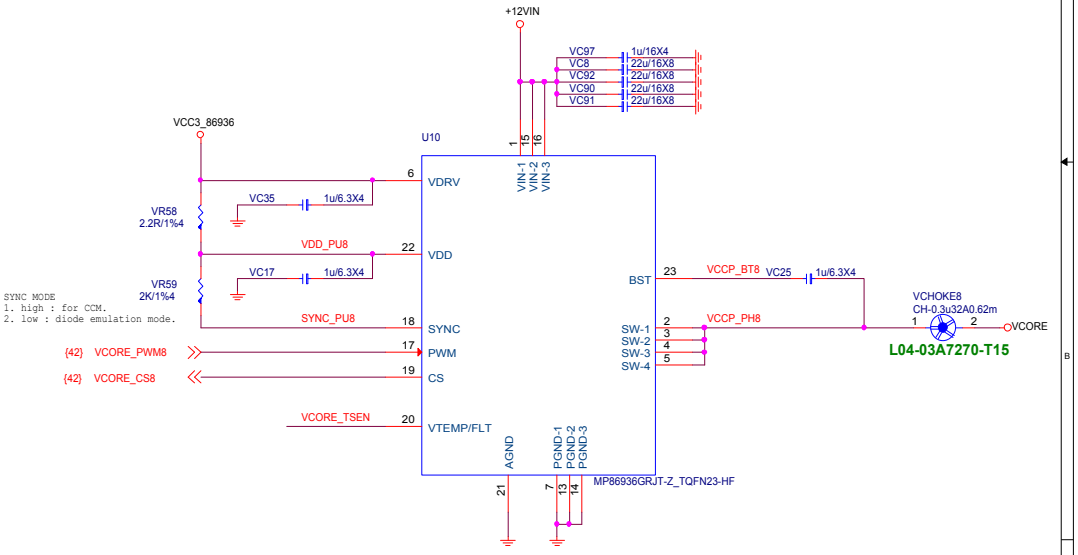
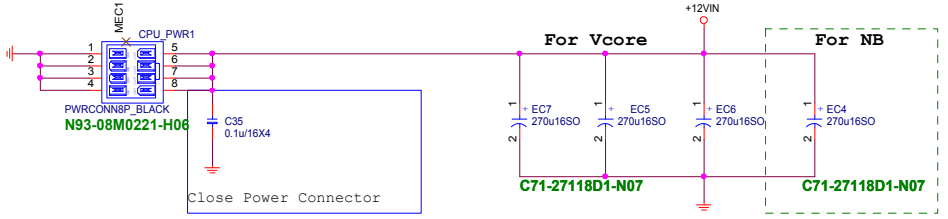








CPU POWER CONNECTOR



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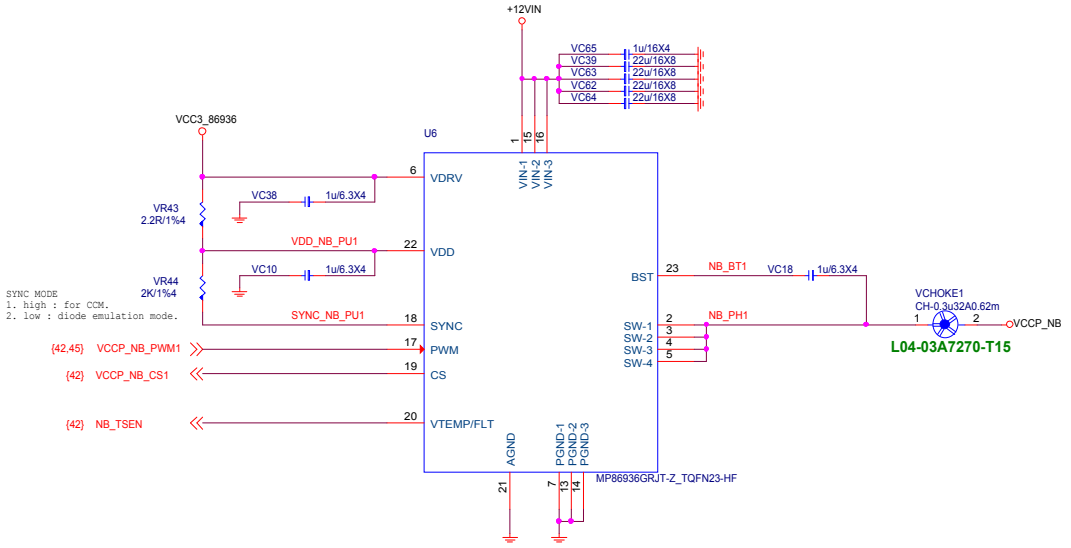
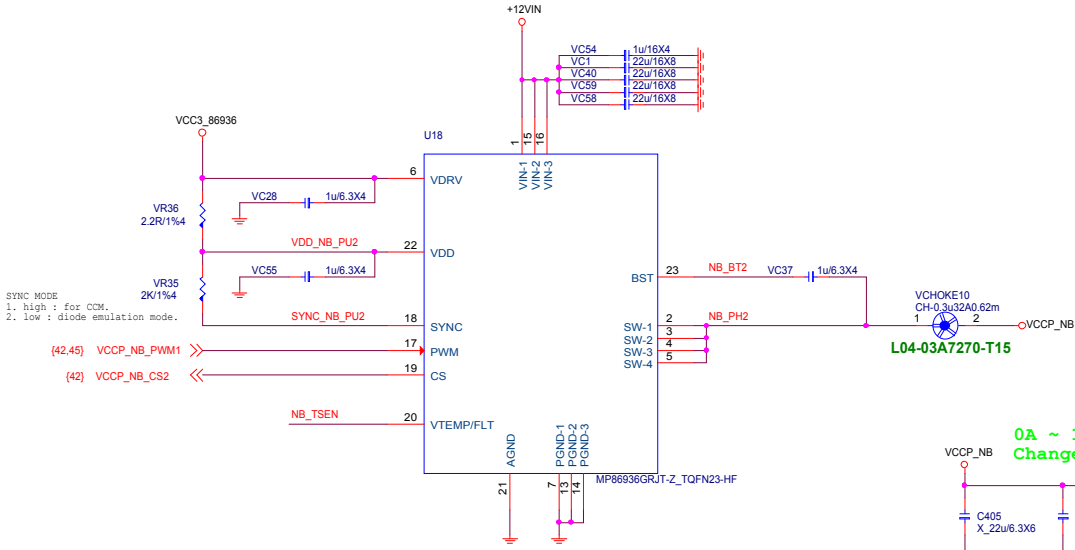
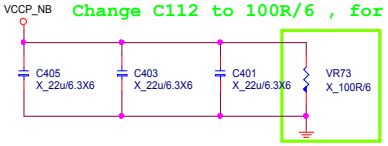
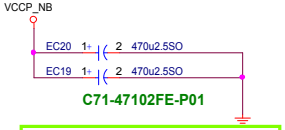
SOC EDC Max 75A





0A ~ 10
Change C112 to 100R/6 , for discharge.





0A ~ 10 remove EC21

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CPU 1.8V S5

Fix CCM

CPU 1.8V_S5@0.5A
CPU_VDDP_S5@1A
AUDIO1.8V@0.25A
For VCCP_NB_S5 @0.9A

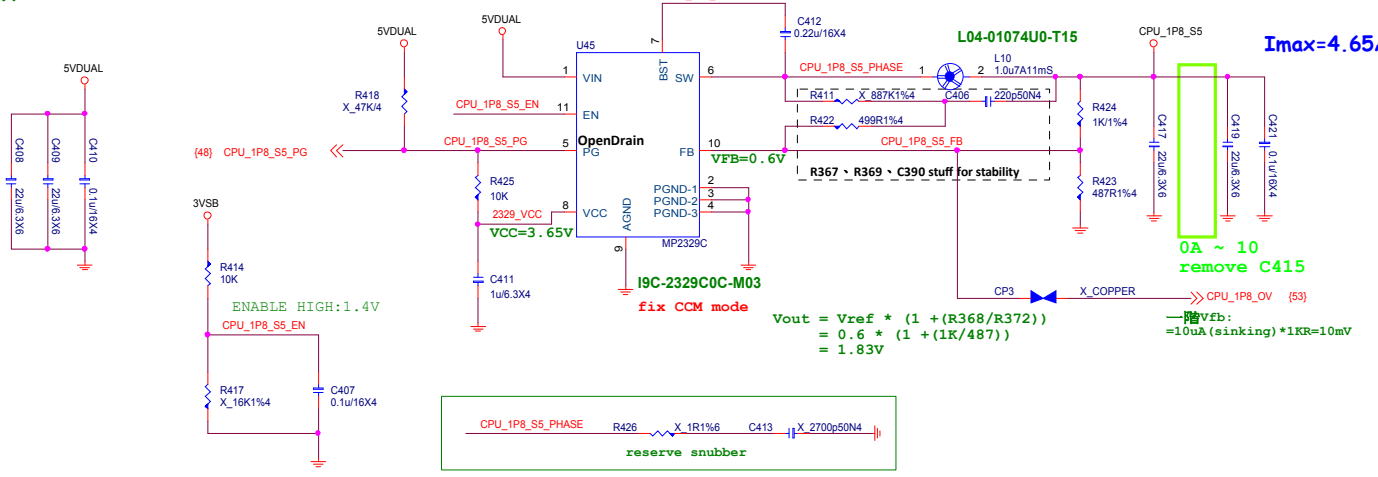
Input Current = (6.5A*1.8V)/5V/0.8 = 3A

Continuous Conduction Mode (CCM)

CPU_1P8_BST、CPU_1P8_BST_R >50 mils.

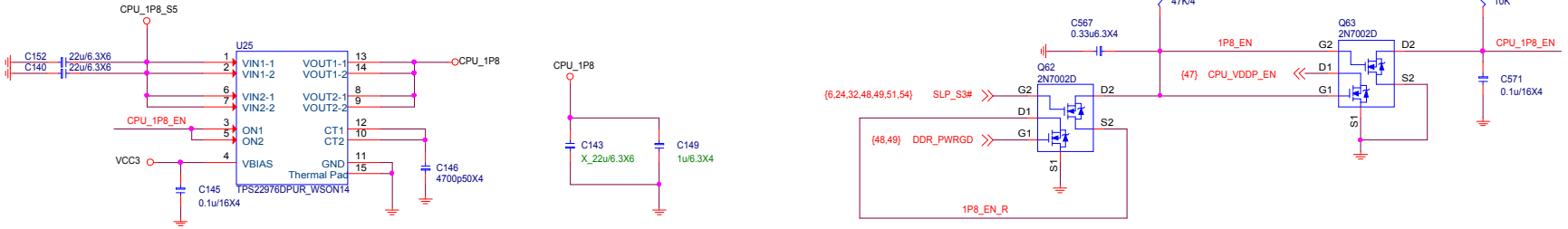
OCP = 6.5A

Imax=4.65A(S5+S0)

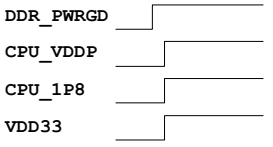


CPU 1.8V S0

CPU 1.8V_S0@2A



Adijustable Rise Time
SR = 0.42*CT+66
SR is the slew rate in (µs/V)
CT is constant value on CT pin (in pF)
The units for the constant 66 is in (µs/V)



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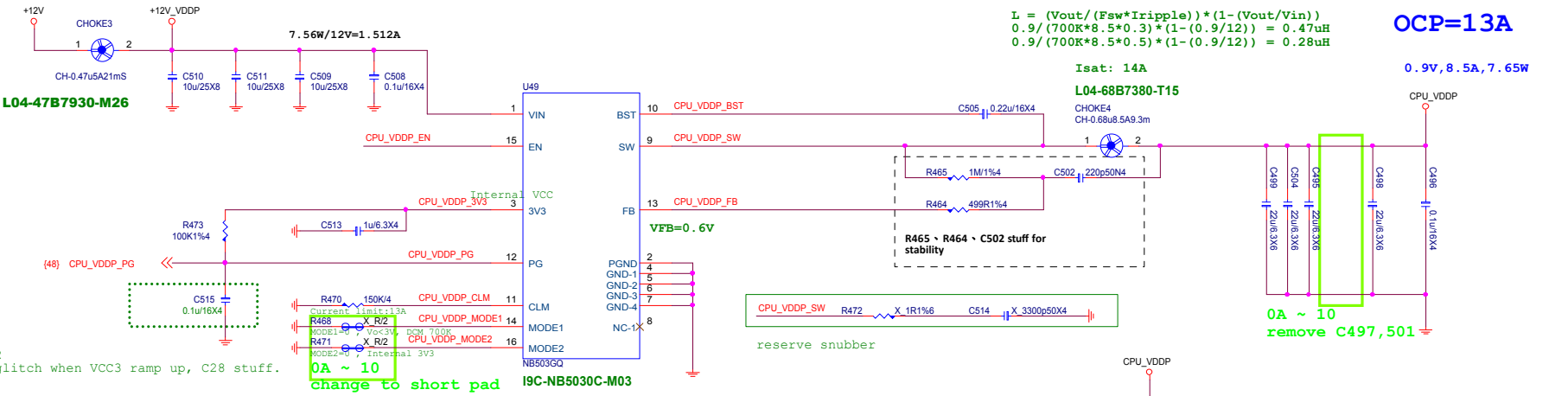
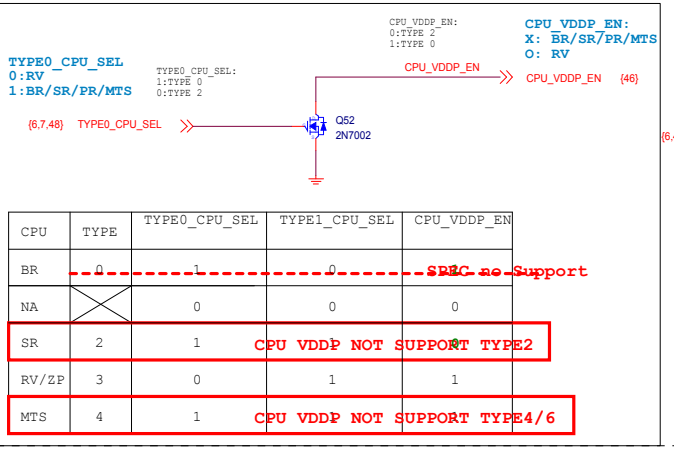
CPU_VDDP_S0

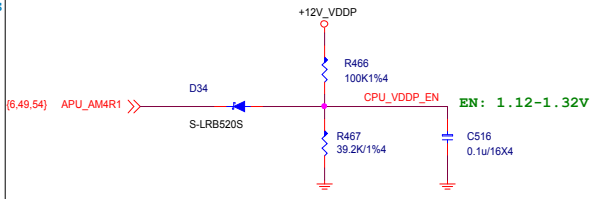
0.9V@S0:8.5A

```
Input Current = (13A*0.9V)/12V/0.8 = 1.22A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=13*SQRT((0.9/12)*(1-(0.9/12))) = 3.42A
Choke Irms =5 A
```

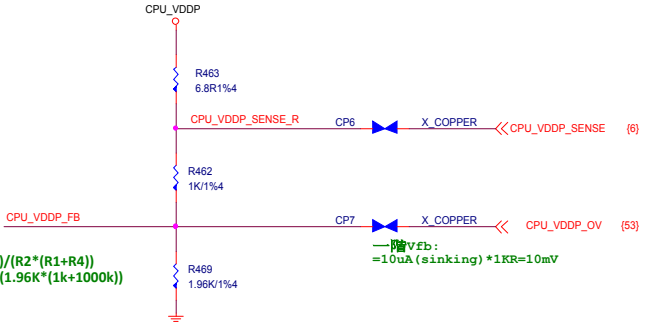




CPU	TYPE	TYPE0_CPU_SEL	TYPE1_CPU_SEL	CPU_VDDP_EN
BR	0	1	0	SPEC no Support
NA	X	0	0	0
SR	2	1	CPU VDDP NOT SUPPORT TYPE2	1
RV/ZP	3	0	1	1
MTS	4	1	CPU VDDP NOT SUPPORT TYPE4/6	

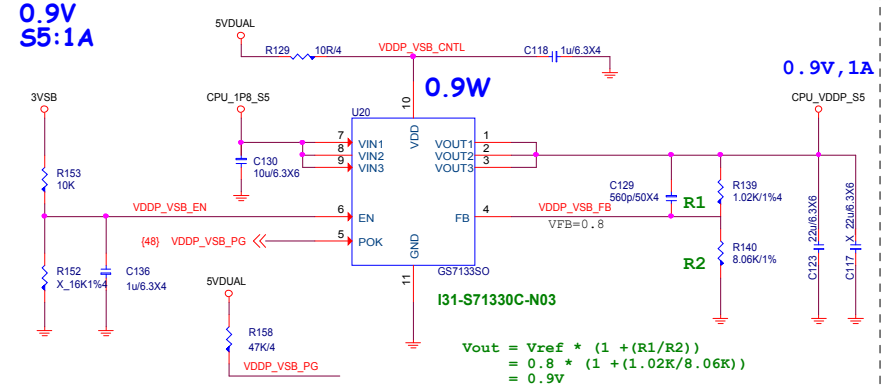



```
Vout = Vref + (R1*R4*Vref)/(R2*(R1+R4))
     = 0.6+(1k*1000k*0.6)/(1.96K*(1k+1000k))
     = 0.9058V
```



CPU_VDDP_S5

0.9V
S5:1A




```
Vout = Vref * (1 +(R1/R2))
     = 0.8 * (1 +(1.02K/8.06K))
     = 0.9V
```

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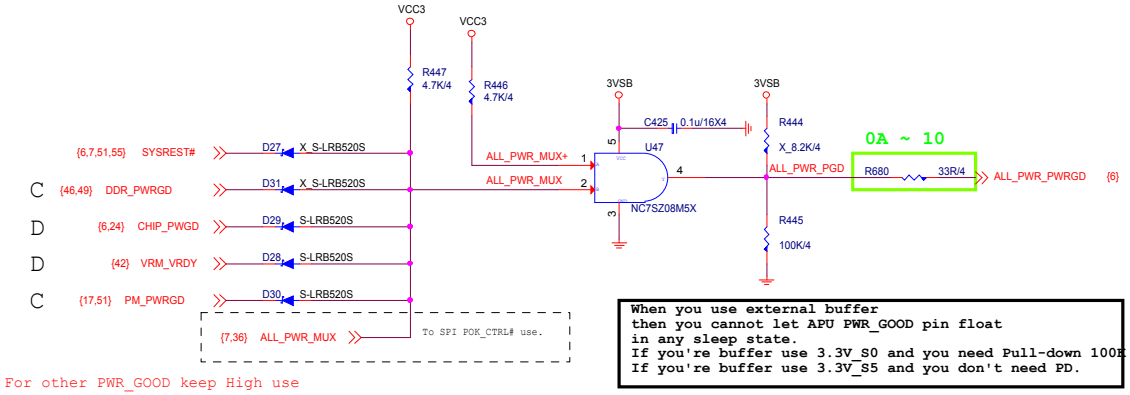
ALL POWER GOOD MUX

S0 PG



For other PWR_GOOD keep High use

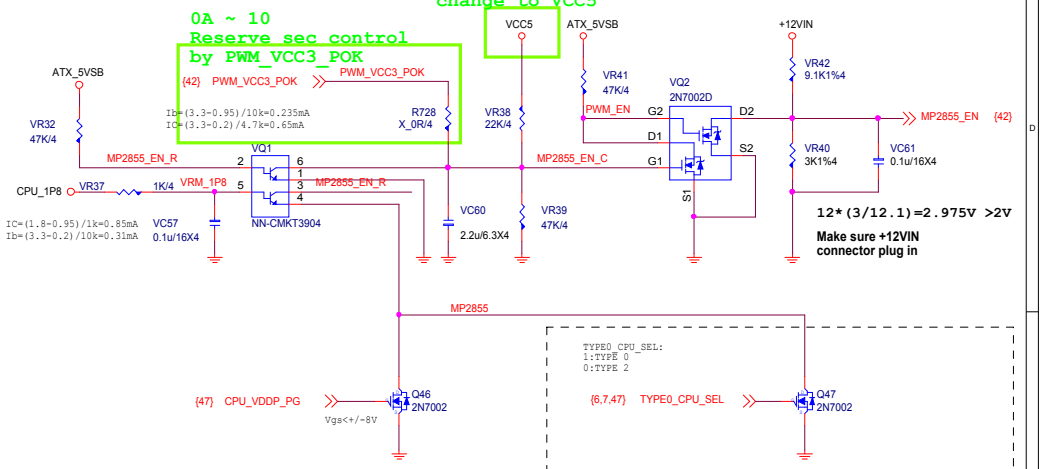
When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

VRM_Enable circuit

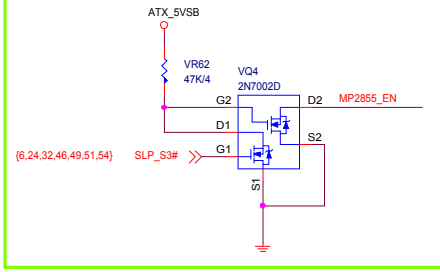
0A ~ 10
remove D25

0A ~ 10
change to VCC5

0A ~ 10
Reserve sec control
by PWM_VCC3_POK



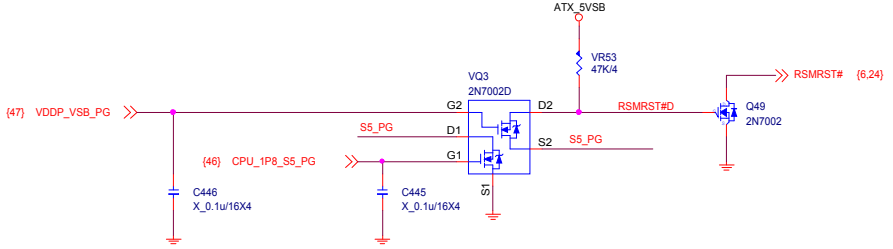
0A ~ 10



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
~~DR~~	~~0~~	~~0~~	~~1~~
NA		0	0
SR	2	CPU VDDP NOT SUPPORT TYPE2	
RV/ZP	3	1	0
MTS	4	CPU VDDP NOT SUPPORT TYPE4	

SPEC no Support

S5 PG



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DDR4_1.2V
15.5A+4.75A+0.6A=20.85A

15.5A FOR CPU

4.75A FOR 2DIMM
0.6A FOR DDR VTT

Irms = Iout * SQRT{D/N- (D)^2]}
VCCDDR:
D=Vout/Vin=1.2/5=0.24
N=Phase number=1
=20.85A*SQRT(0.24-0.0576)
=5.21A

L04-22B7700-T15
CHOKE2
CH-0.22u8A9m-HF

VID	Reference Voltage (V)
H	0.675 ref.
L	0.75 for 1.2045V

f:400KHz

By layout modify

R313=102K for OCP(dc)=35A (typ)
and OCP(dc)=A(min)

Close to PIN19

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

default=1.2045V

R303=1K, R301=1.65K,
Vo=0.75V*(1+R303/R301)=1.2045V

Imax: 20.85A

OCP:27.5A

Isat: 22A

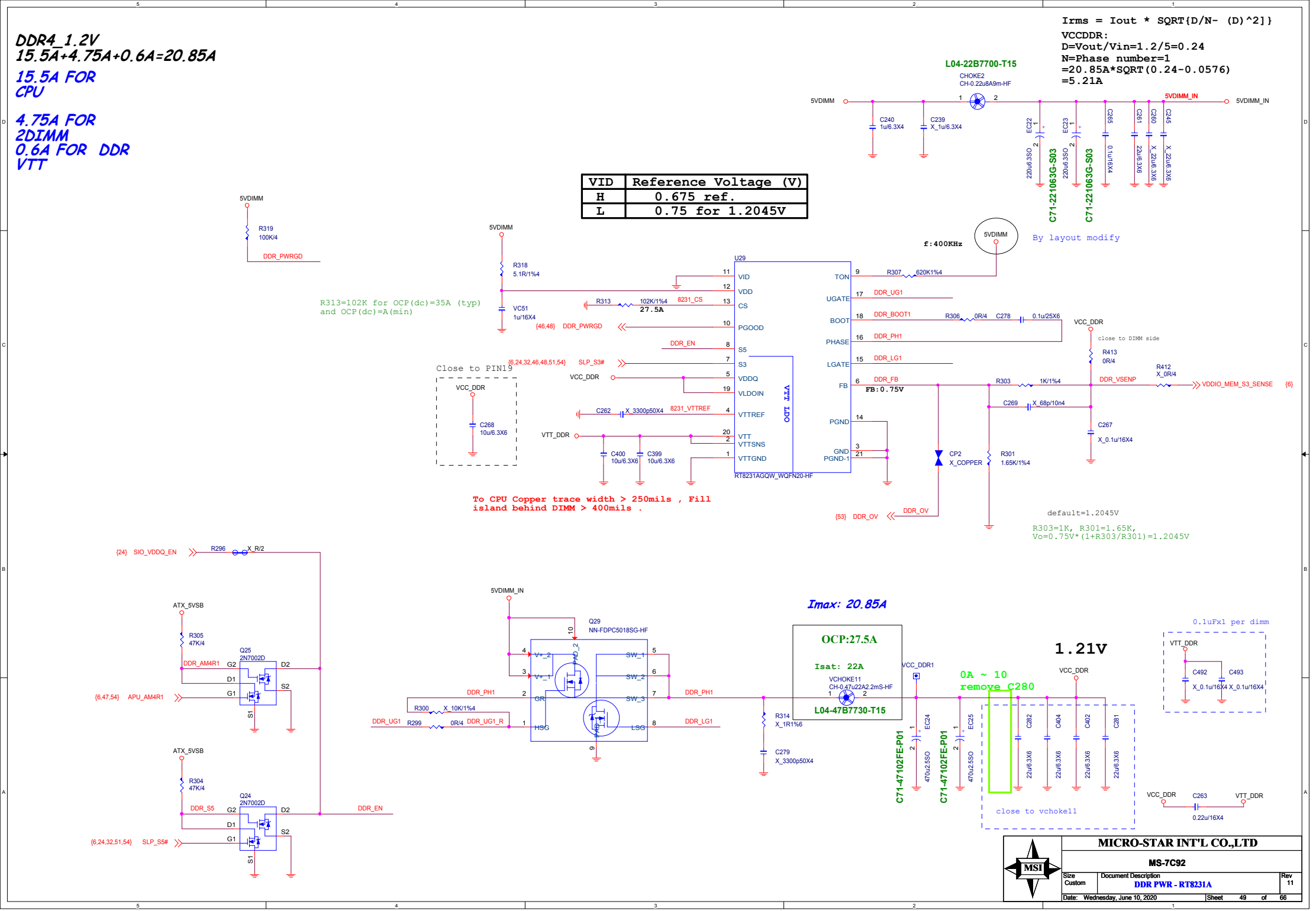
L04-47B7730-T15

1.21V

0A ~ 10
remove C280

0.1uFx1 per dimm

close to vchoke11



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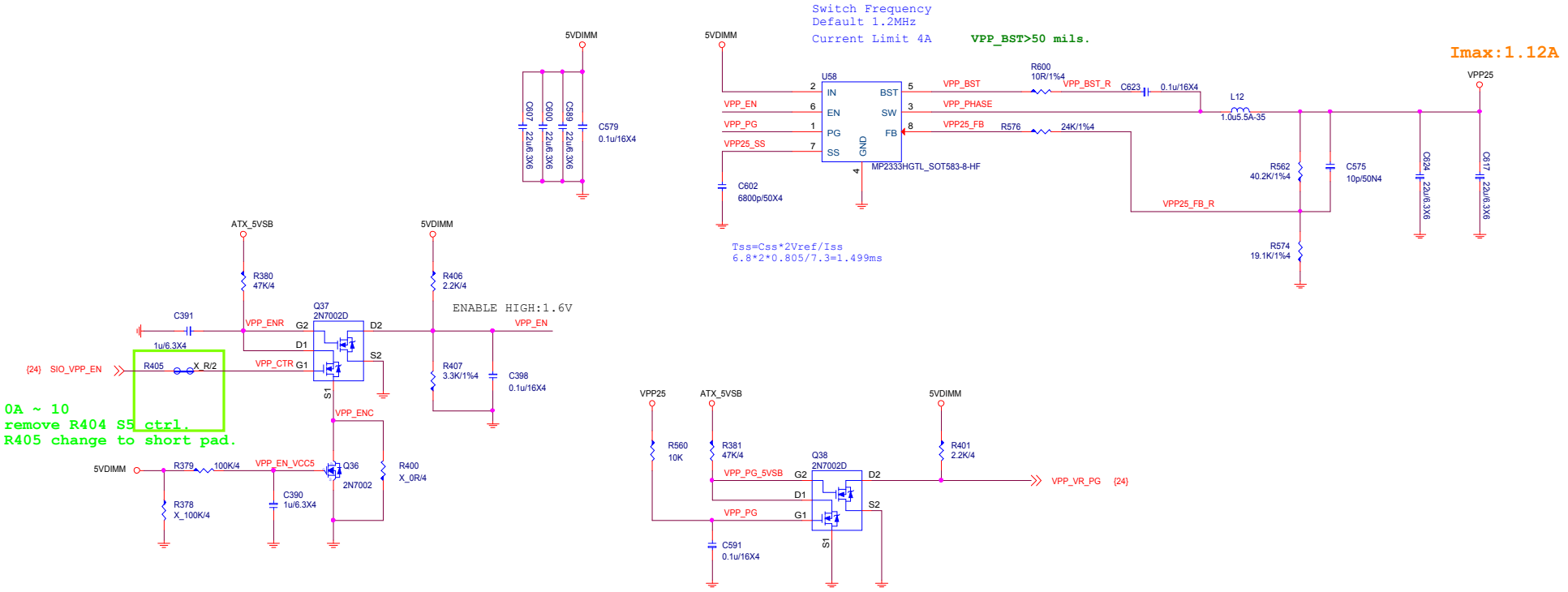
MS-7C92

Size	Document Description	Rev
Custom	DDR PWR - RT8231A	11

Date: Wednesday, June 10, 2020 Sheet 49 of 66

4DIMM : VPP25

2.5V@1.12A



MICRO-STAR INT'L CO.,LTD		
MS-7C92		
Size: Custom	Document Description: DDR PWR-MP2333HGTL-VPP25	Rev: 11
Date: Wednesday, June 10, 2020	Sheet 50 of 66	

FOR Promontory 1.05V_S0

1.05V
S0:5.5A

Input Current= (8A*1.05V)/5V/0.8=2.1A

Width:＞80mil

Isat: 12A

L04-01074U0-T15

OCP=8A

1.05V@5.5A

5VDUAL CHOKE1 CH-0.47u5A21mS SY8288_VIN

L04-47B7930-M26

C238 10u/25X8 C236 10u/25X8 C234 0.1u/16X4 R254 100K1%4

ATX_5VSB R302 47K/4 C264 X_1u/6.3X4 VSB_EN

Q27 2N7002D R255 68K1%/4 C230 0.1u/16X4

{6,24,32,46,48,49,54} SLP_S3# R312 0R/4 VSB_EN_S

{6,24,32,49,54} SLP_S5# R311 X_0R/4

U27

VIN-1 VIN-2 VIN-3 VIN-4 EN >0.8V EN PG ILMT BYP

3VSB R259 10K PM_1P05_PG

R258 0R/4 PM_1P05_OCP

3VSB R248 0R/4 VCC3_BYP C218 1u/6.3X4

BS PM_1P05_BOOT C227 0.1u/16X4

LX-1 LX-2 LX-3 PM_1P05_PHASE

L7 1.0u7A11mS

FB PM_1P05_FB R251 X_499R1%4 PM_1P05_FB_R

0.6V

C226 X_330p50X/4 C206 0.1u/16X4 C216 22u/6.3X6 C212 22u/6.3X6 C207 22u/6.3X6 C201 22u/6.3X6 C199 22u/6.3X6

PM_1P05

NC-1 NC-2 NC-3

by Silergy FAE Suggestion
Please connect pin17 (Vcc)/pin16(NC) and it's good for VCC layout.

VCC PM_1P05_LDO C221 2.2u/6.3X4

GND-1 GND-2 GND-3 GND-4

SY8288 I9C-8288R0C-SZ1

R1 R252 1K/1%4 PM_1P05_FB SP1 X_COPPER PM_1P05_OV {53}

R2 R253 1.33K1%4

Vout = Vref * (1 + (R1/R2))
= 0.6 * (1 + (1K/1.33K))
= 1.051V

VSB_EN Q26 2N7002 {24} S0iX_EN R310 10K

SLP_S5#
GPIO(as S5#)
VSB_EN
PM_1P05_EN

S5 S0 S3 S0 S5 S0 S0iX S0 S5

SY8288_OCP	OCP
0	8A
floating	12A
1	16A

FOR PROM PM_1P05_S5

1.05V@0.05A

3VSB I31-7116S09-N03 U21 GS7116S5 VDD VOUT EN GND ADJ PM_1P05_S5

C126 1u/6.3X4 R147 10K PM_1P05_S5_EN C139 1u/6.3X4 C132 X_0.1u/16X4

R1 R143 1K/1%4 C127 10u/6.3X6

PM_1P05_S5_FB R2 R160 3.16K/1%4

{6,24,54} DEEP_S5 Q14 2N7002

Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(1K/3.16K))
= 1.05V

Promontory-2.5V

2.5V@900mA

5VDUAL R294 10R/4 PM_2P5V_CNTL C258 1u/6.3X4

Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/4.7K))
= 2.502V

0.72W

U28 GS7133SO I31-7133S02-N03

{52} PM_2P5V_POK PM_2P5V_POK

PM_1P05_EN EN >1.4V

3VSB VIN C266 10u/6.3X6

NC VOUT VDD GND GND FB

C244 560p/50X4 PM_2P5V_FB VFB=0.8

R1 R276 1K/1%4

R2 R289 470R1%/4

PM_2P5V C243 22u/16X8

SP2 X_COPPER PM_2P5V_OV {53}

AVL: I31-3730S02-N62

3VSB R188 10K

PM_2P5V_POK D13 S-LRB520S

PM_1P05_PG D10 S-LRB520S

{6,7,48,55} SYSREST# D14 X_S-LRB520S

Add by CRB Rev. E

PM_PWRGD {17,48}

ATX_5VSB R193 47K/4 Q16 2N7002D

C151 X_1u/6.3X4 PM_PWGD

VCC33 R178 10K PWGD_VCC33

C150 X_0.1u/16X4

C153 1u/6.3X4

3VSB
PM_1P05_S5
PM_1P05
PM_2P5V
VCC33

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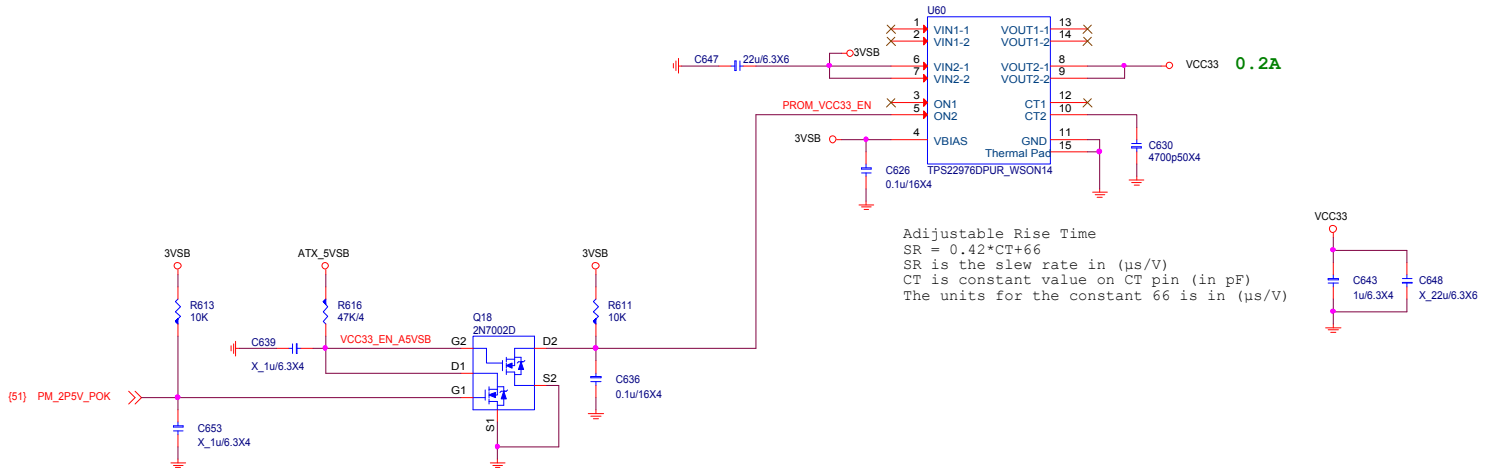
PROM_VCC33

VCC33@0.2A



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MS-7C92		
Size: Custom	Document Description: PM -TPS22976DPUR_VCC33	Rev: 11
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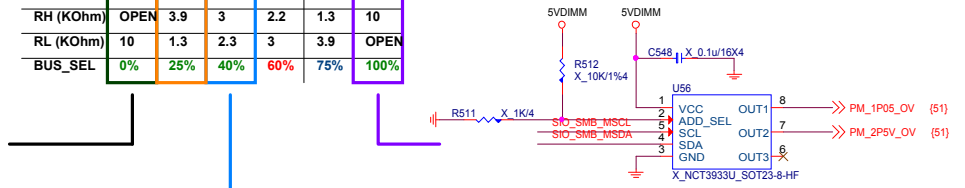
Over Voltage Control IC

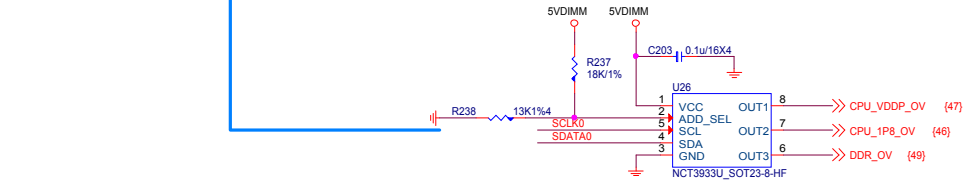
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

0x20:RH=10K,RL=OPEN



0x26:RH=18K,RL=13K



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MS-7C92

Size	Document Description	Rev
Custom	OV Control - NCT3933	11

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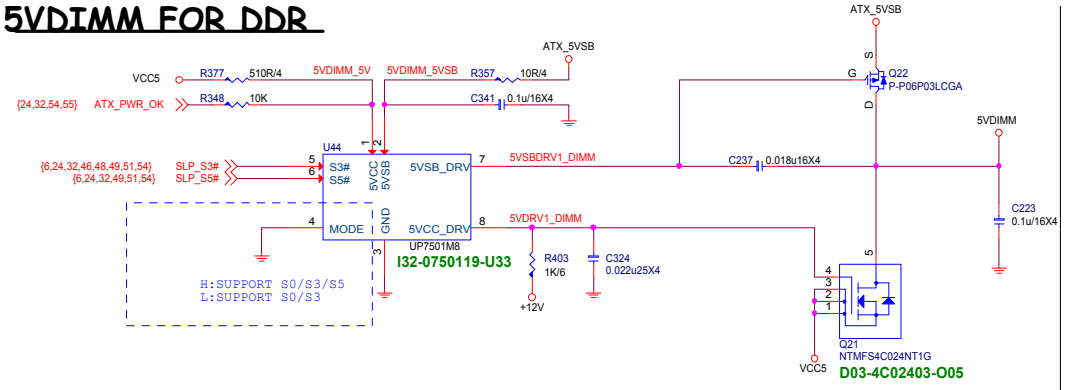
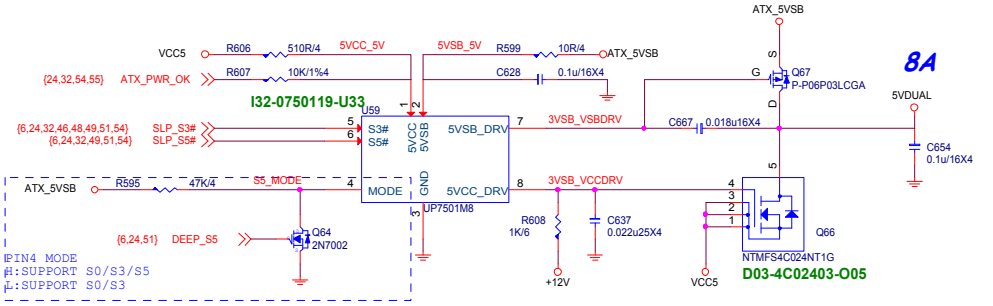
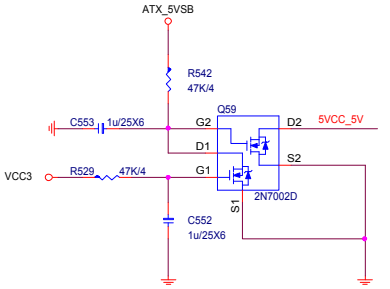
5VDIMM FOR DDR



5VDUAL For 3VSB/CPU1.8V/VDDP

LDOVDD=93.6mA
CPU_1P8_S5 VIN=3A
PM_1P05 VIN=1.44A
3VSB =3 A



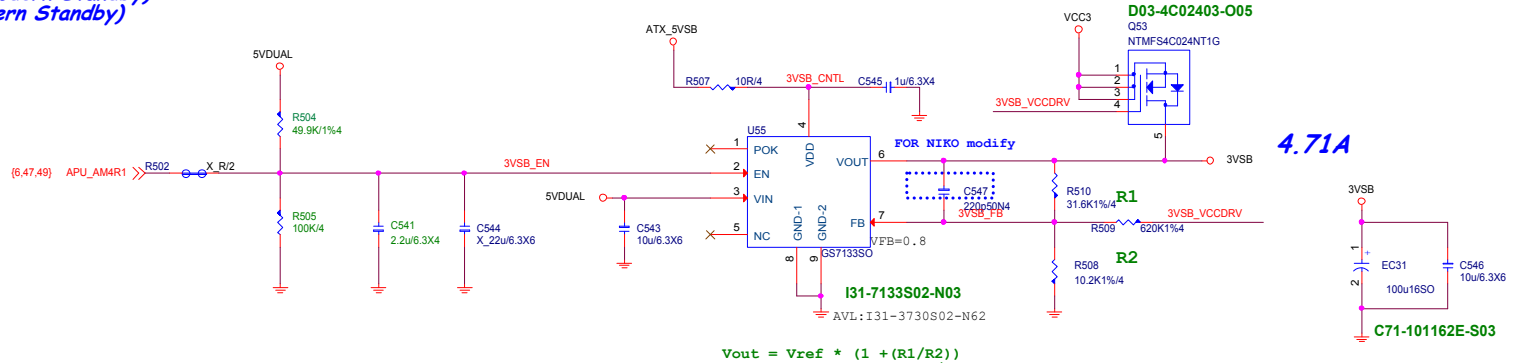


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

3VSB cost down

3.3V@4.71A

CPU:VDD_33_S5=0.25A
CHIP:VDD_33_S5=0.1A
PCIE=(375mA*6)=2.25A
M.2WIFI= 0.78A
LAN=0.18A
PM_1P05_S5 :0.05A
PM_2P5V :0.9A(Modern Standby)
VCC33 :0.2A(Modern Standby)



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(31.6K/10.2K))
= 3.328V

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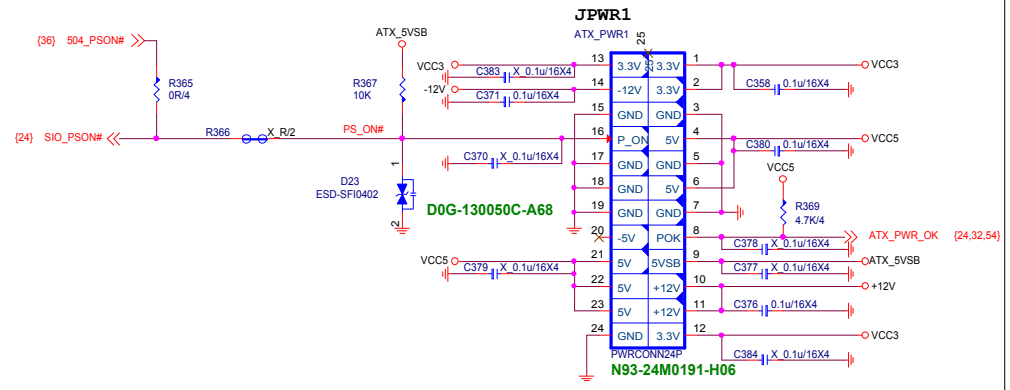
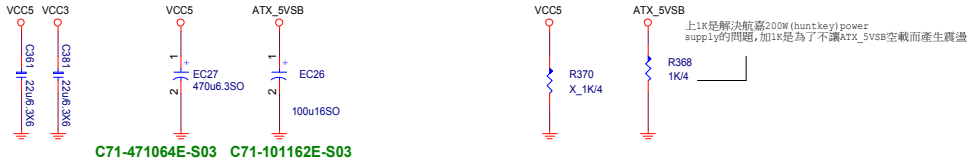
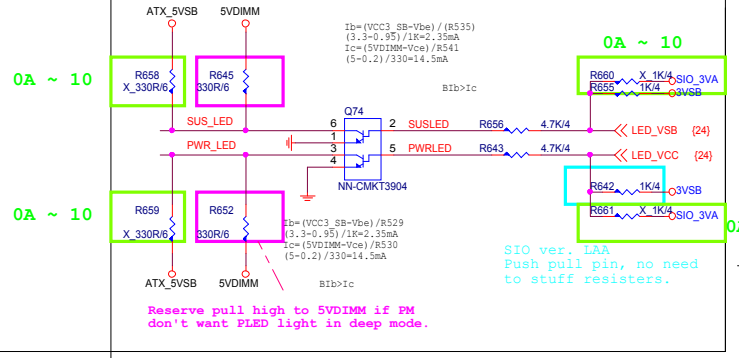
ATX POWER CONNECTOR



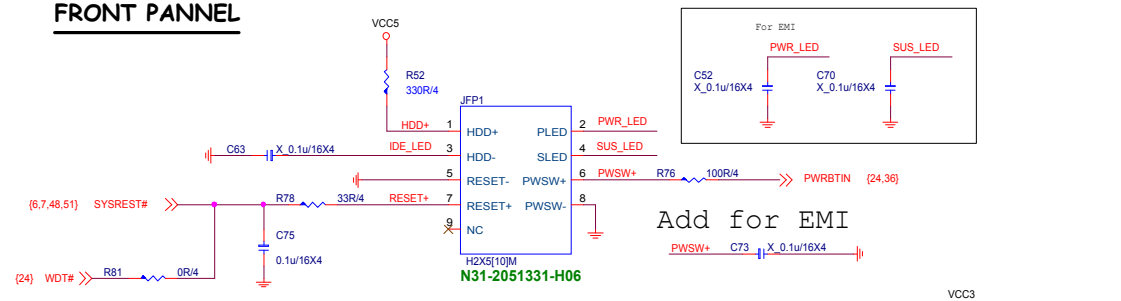


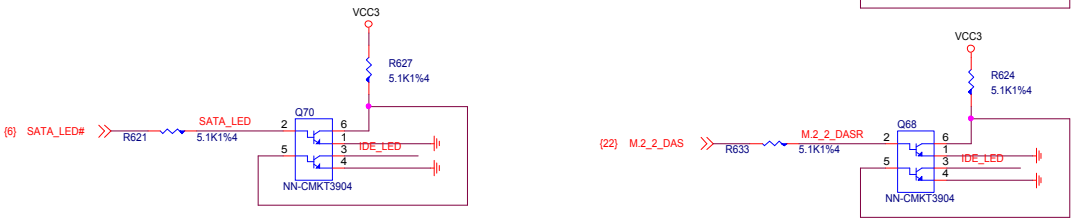
TPM

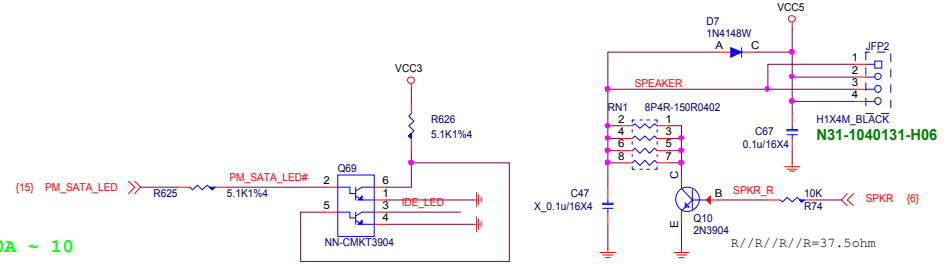
LED (for NCT6797D)



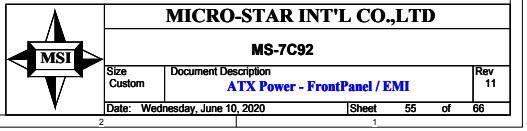
FRONT PANNEL



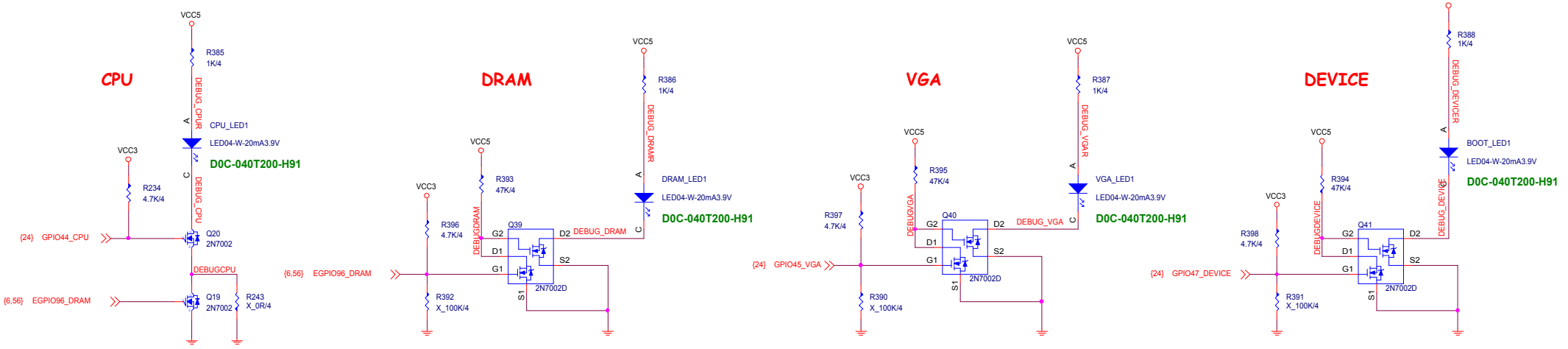




Voltage Mearsure Point



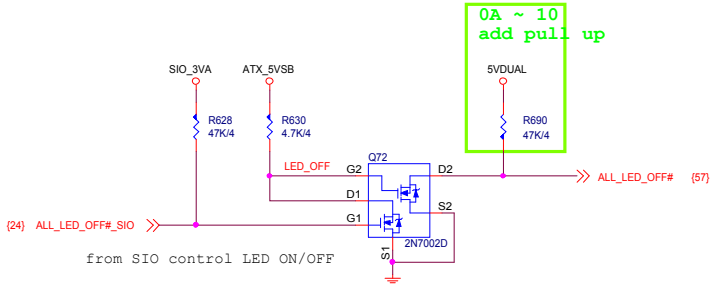
EZ Debug LED



LEDGPIO		GPIO44_CPU	EGPIO96_DRAM	GPIO45_VGA	GPIO47_DEVICE
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

LED亮燈時同時將CPU LED關掉

ALL LED OFF FORM SIO



AMD AMP Detect LED

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MS-7C92	
Size: Custom	Document Description: LED - EZ DEBUG / AMP
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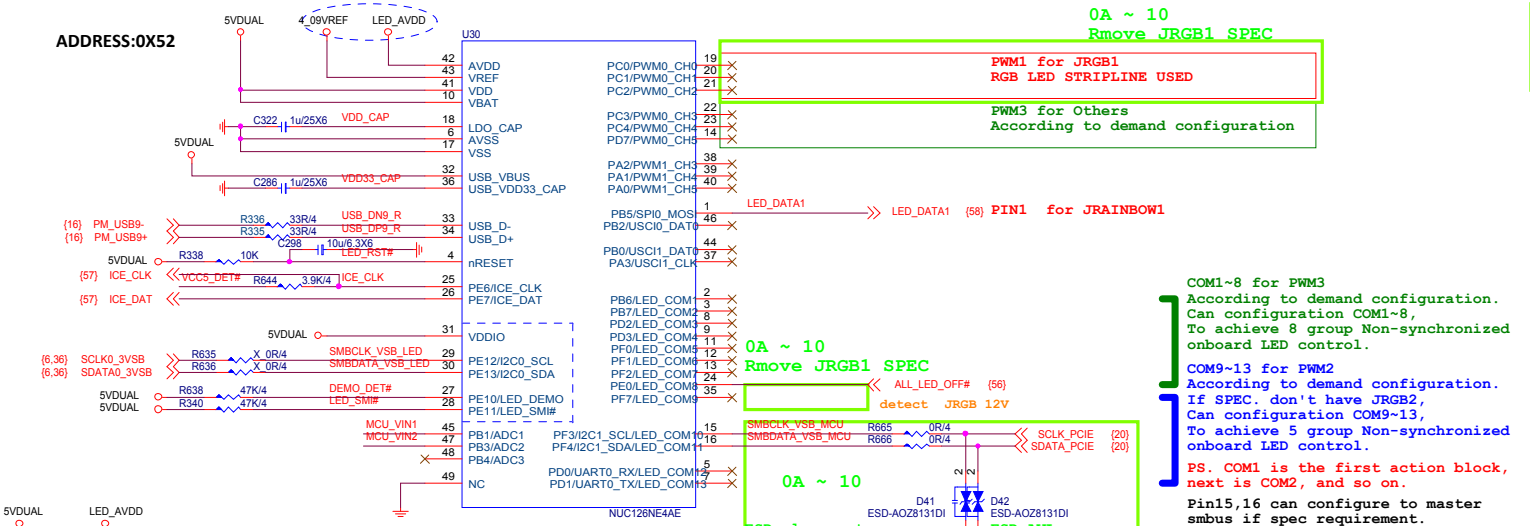
48 PIN LED MCU

If you use ADC function,need to separate VREF from AVDD and 4_09VREF stuff for VREF.

ADDRESS:0X52



0A ~ 10
Rmove JRGB1 SPEC

PWM1 for JRGB1
RGB LED STRIPLINE USED

PWM3 for Others
According to demand configuration

LED_DATA1 {58} PIN1 for JRAINBOW1

0A ~ 10
Rmove JRGB1 SPEC

ALL_LED_OFF# {56}

detect JRGB 12V

COM1~8 for PWM3
According to demand configuration.
Can configuration COM1~8,
To achieve 8 group Non-synchronized
onboard LED control.

COM9~13 for PWM2
According to demand configuration.
If SPEC. don't have JRGB2,
Can configuration COM9~13,
To achieve 5 group Non-synchronized
onboard LED control.

PS. COM1 is the first action block,
next is COM2, and so on.

Pin15,16 can configure to master
smbus if spec requirement.

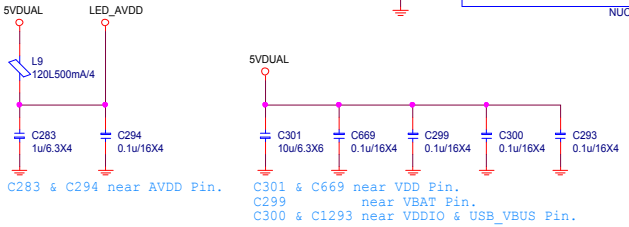
SMBCLK_VSB_MCU R665 0R/4 SCLK_PCIE {20}
SMBDATA_VSB_MCU R666 0R/4 SDATA_PCIE {20}

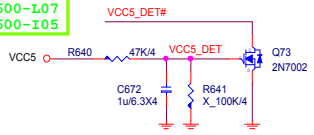
0A ~ 10

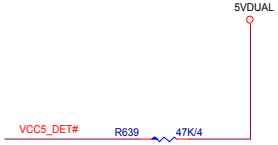
D41 ESD-AOZ8131DI
D42 ESD-AOZ8131DI

ESD placement
close to PCIE SLOT
PCIE slot → ESD → MCU

ESD AVL
D0G-0500600-L07
D0G-0600600-I05



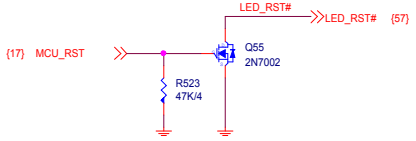




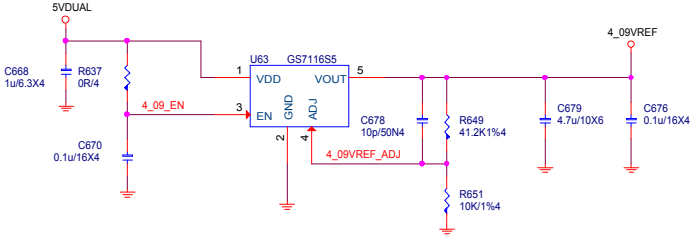
detect JRGB 12V

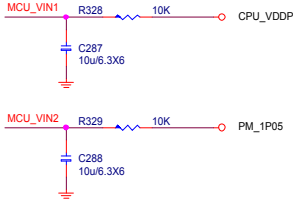
0A ~ 10
Rmove JRGB1 SPEC

HW Reset MCU

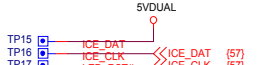


Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~13	PWM2





JT1 for FW update



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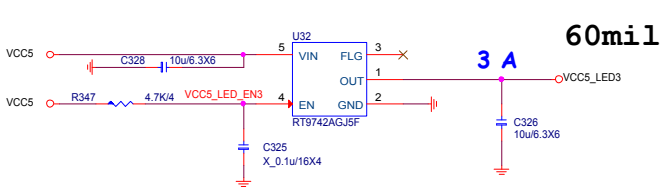
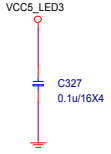
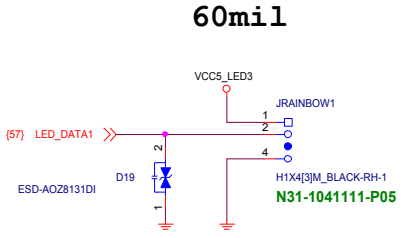
JRGB1

0A ~ 10
Rmove JRGB1 SPEC

JRAINBOW1







MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C92	
Size: Custom	Document Description: LED - JRGB1_JRANBOW1	Rev: 11
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MS-7C92	
Size: Custom	Document Description: BOM Option
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CPU Socket

CPU2

OE9-7C92001-C22

E95-0000024-C22

Simulation

X_JS1 — SIM1 — X_PIN1*2

X_JS2 — SIM2 — X_PIN1*2

X_JS3 — SIM3 — X_PIN1*2

X_JS4 — SIM4 — X_PIN1*2

FM2, FM4, FM1, FM3, FM5, FM8, FM7, FM6 — X_FM120

Optics Orientation Holes

MH2, MH3, MH4, MH1 — X_MH001

C4 0.1u/16X4

C3 0.1u/16X4

MANUAL PART

AMI_LAB1 — G51-M1SPXXA-A09

G51-M1SPXXA-A09

CFOS1 — Y02-MU00170-CFO — <MSI-BOM>

Y02-MU00170-CFO

HDMI_LA1 — Label — HDMI

HDMI LABEL

Y01-RHDMI03-000

NAHIMIC_LA2 — Label — NAHIMIC

X_NAHIMIC LABEL

Y02-MU00100-NAH

BAT1_X1

BAT-BCR2032P

AVL:
D06-0100161-F52
D06-0100101-K26

PCB

PCB

PCB1

7C92_11

STD+4oz : PD0-07C9211-G37

MOS HEATSINK

WMOS_HSK1 — MEC1

MEC2

WMOS_HSK

PCH HEATSINK

MEC1 — PCH_HSK — MEC2

Mylar

Mylar_1 — Label — Mylar

Mylar LABEL

E26-7C92010-LB4

IO shielding

I/O_shielding1 — Label — I/O_shielding

I/O_shielding

E21-7C92011-A91

DDR COVER

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