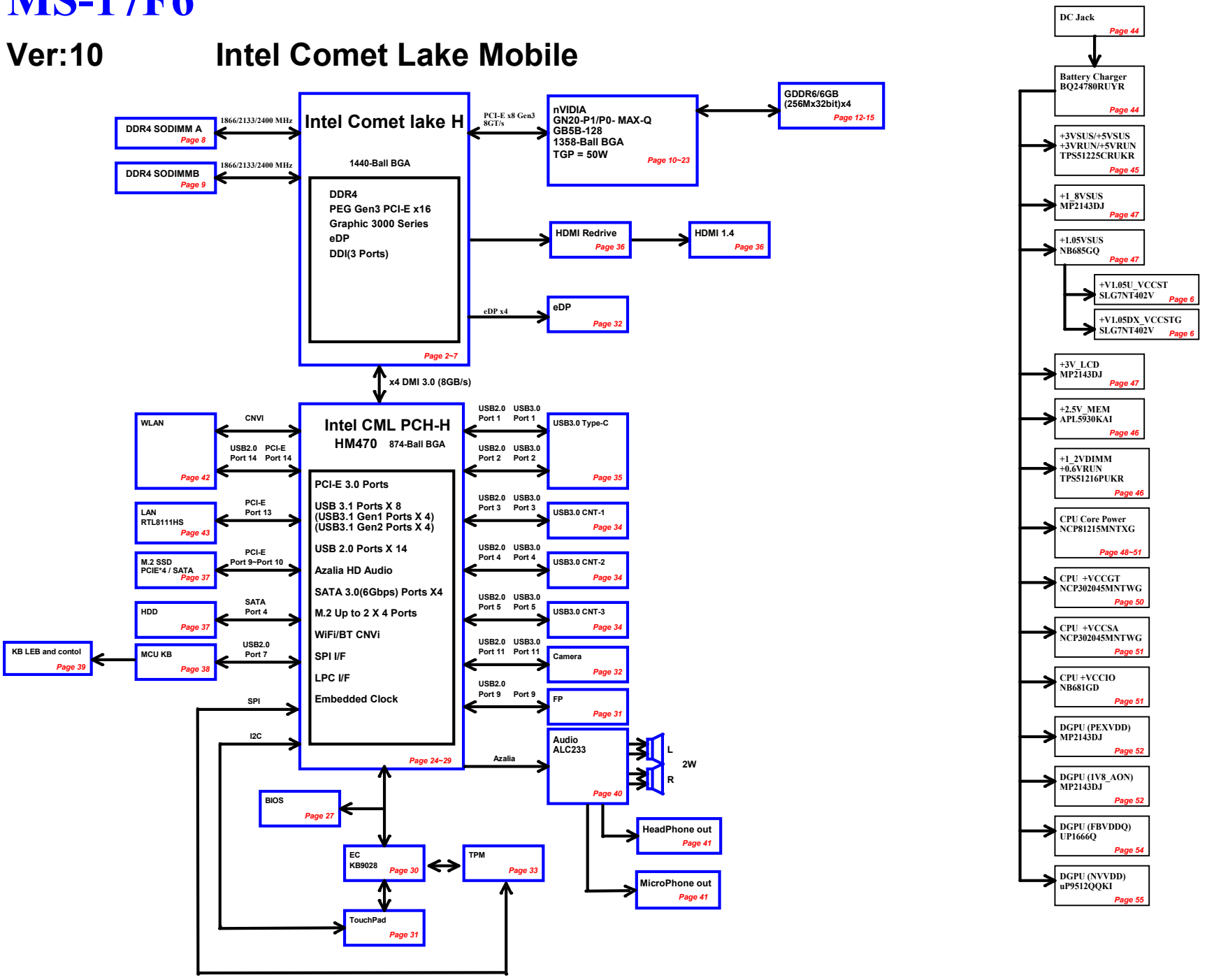
MS-17F6

Ver:10 Intel Comet Lake Mobile



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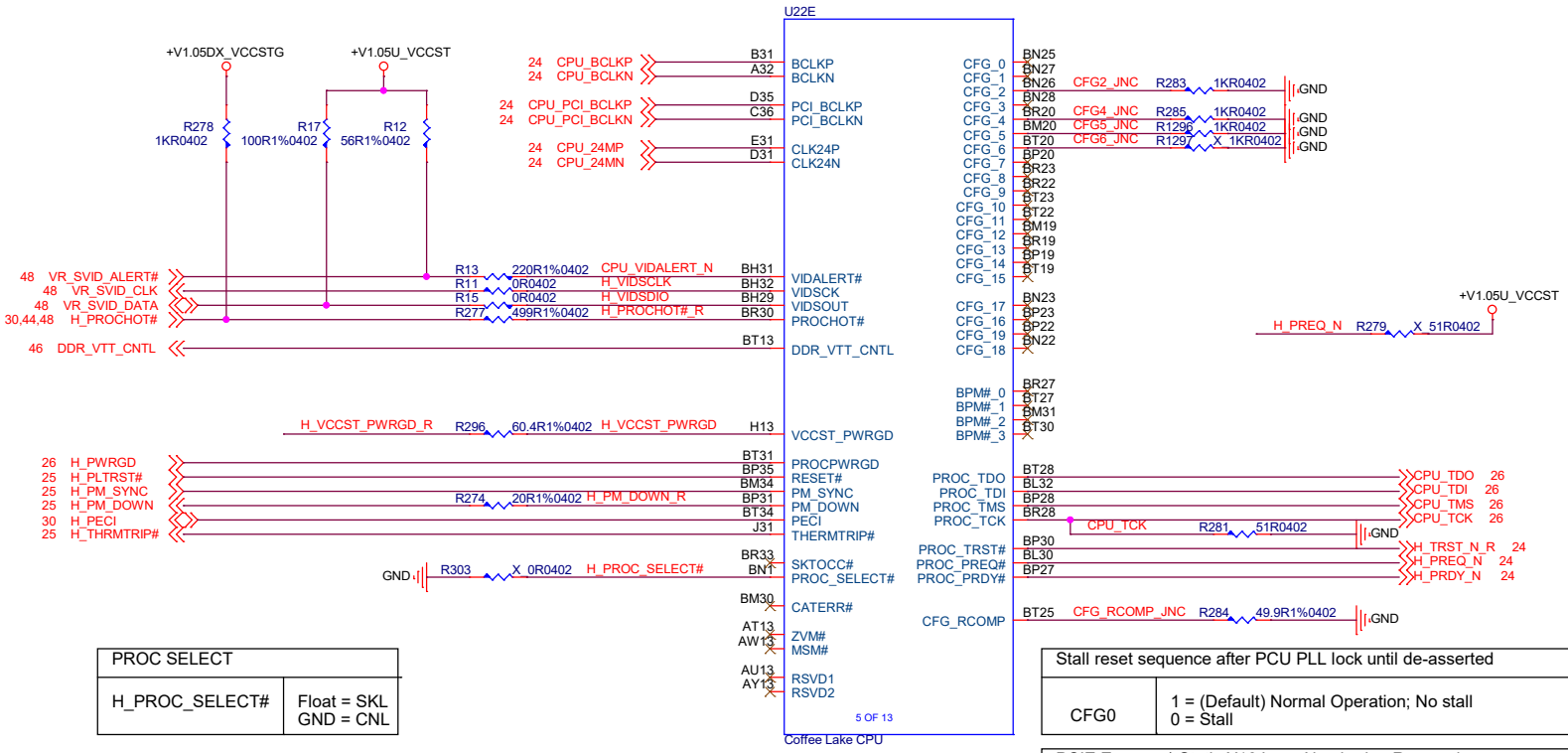
Block Diagram

MS-17F6

10



PROC SELECT	
H_PROC_SELECT#	Float = SKL GND = CNL

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	1 = (Default) Normal Operation; No stall 0 = Stall

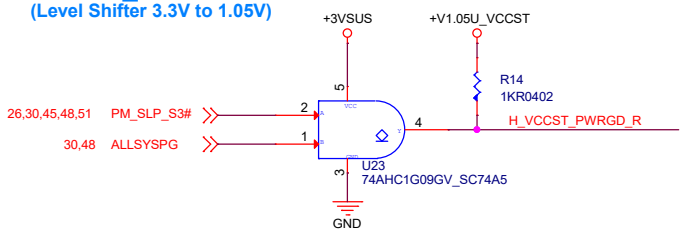
PCIE Express * Static X16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

eDP Enable	
CFG4	1 = Disabled 0 = Enabled

PCI Express* Bifurcation	
CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express*

PEG DEFER TRAINING	
CFG7	1: (default) PEG Train immediately following RESET# de assertion. 0: PEG Wait for BIOS for training

VCCST_PWRGD
(Level Shifter 3.3V to 1.05V)



i5-10300H

i5-10300H

A0C-1030005-I06

X_I5 QUAD CORE

i7-10750H

i7-10750H

A0D-1075005-I06

X_I7 6 core

i5-10200H

i5-10200H

A0C-1020005-I06

X_I5 QUAD core

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Title: **Comet lake(HOST)**

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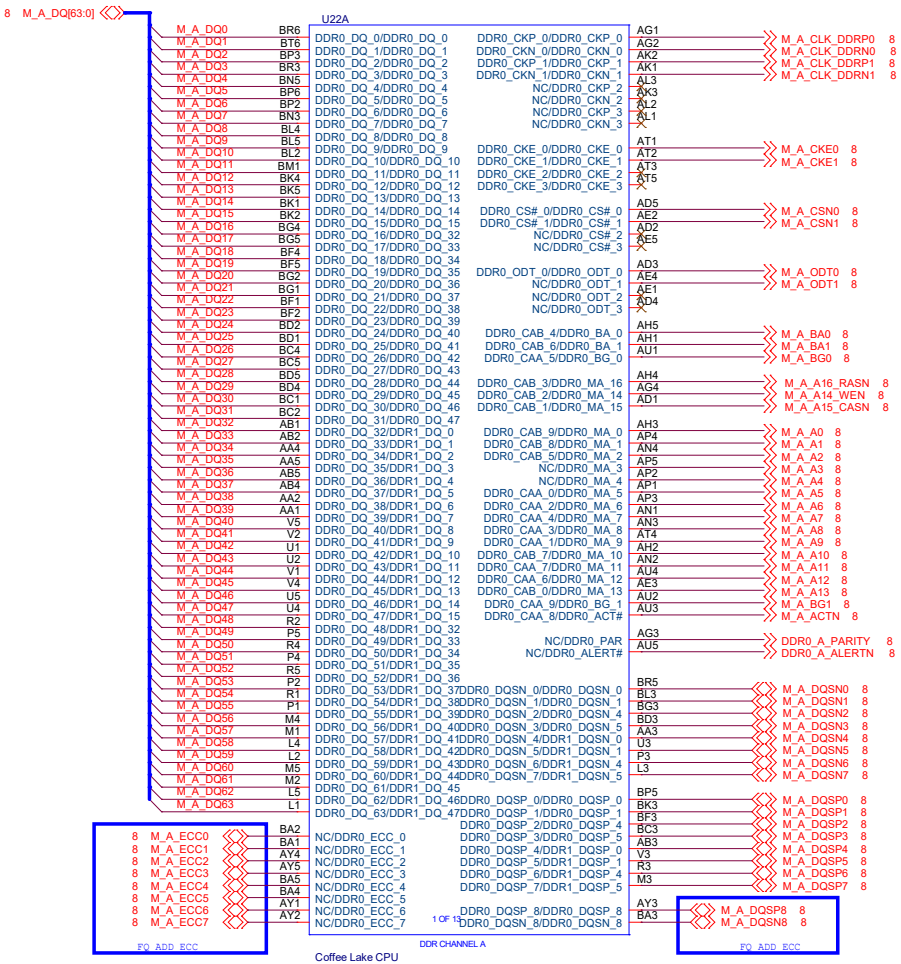
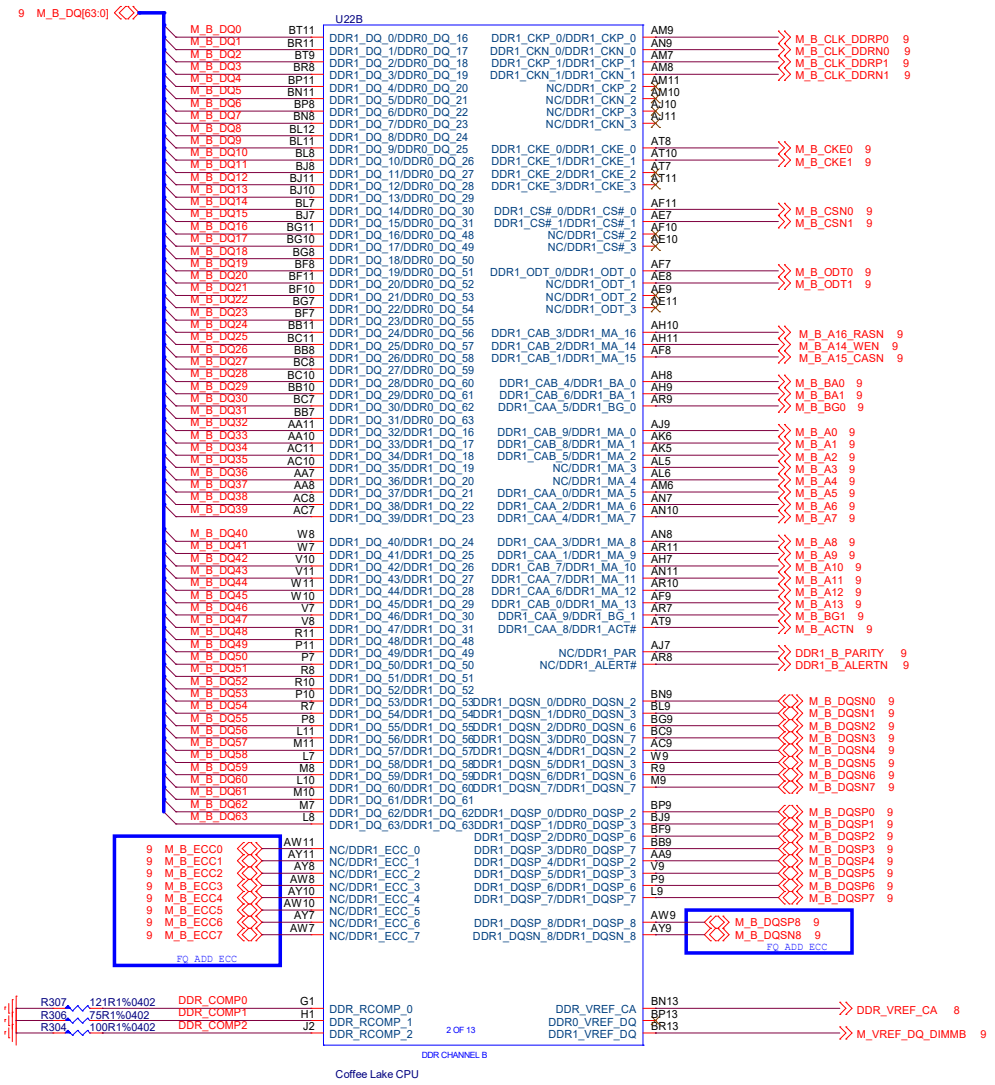
DDR Channel A



DDR Channel B



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Title: Comet lake(DDR4)			
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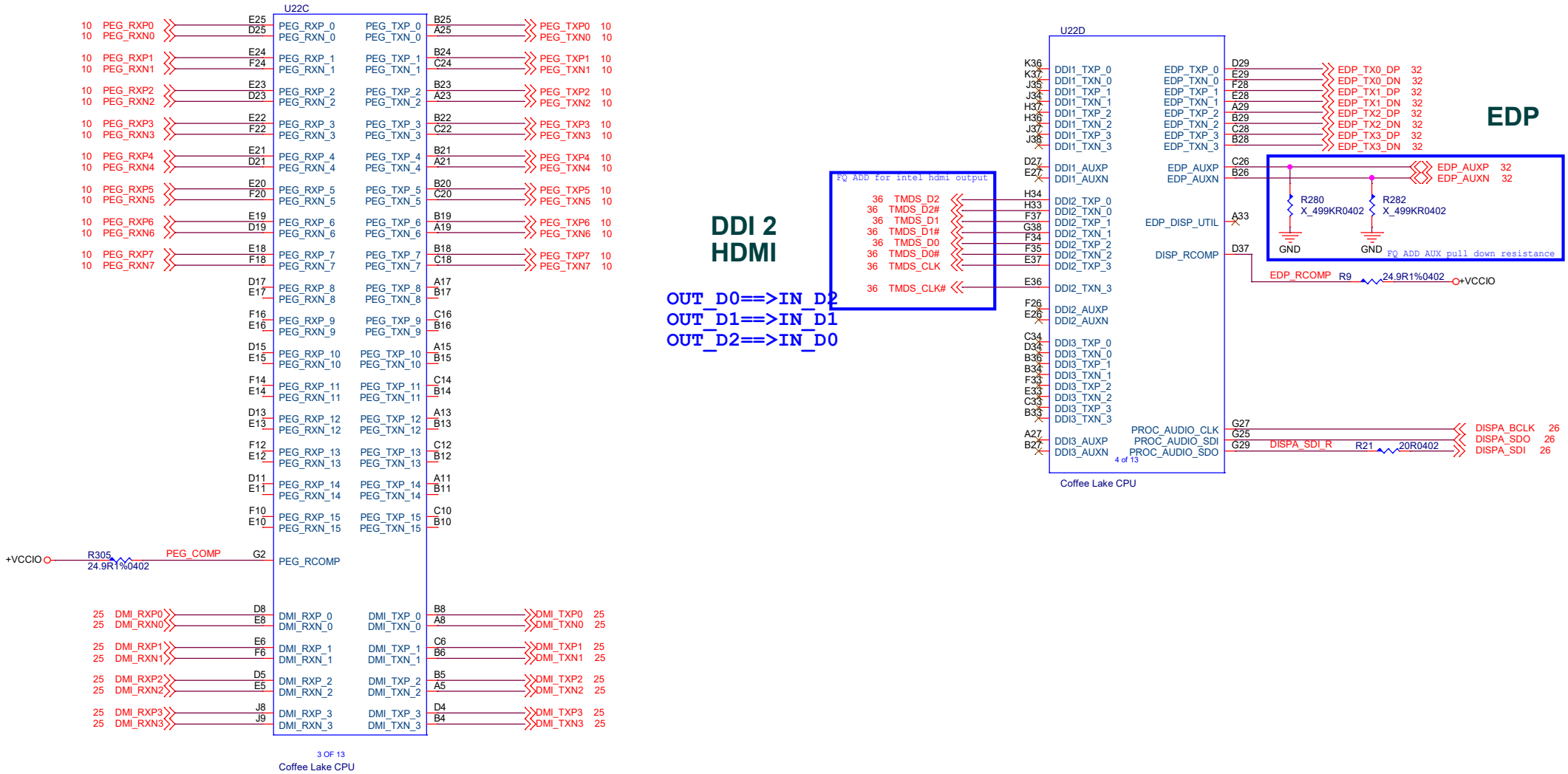

MSI	MICRO-STAR INT'L CO.,LTD.
Title	Comet lake(DMI/Display)
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+VCC_CORE
128A
U22I
VCC_SENSE
VSS_SENSE
VCORE_VCC_SEN 48
VCORE_VSS_SEN 48
9 OF 13
Coffee Lake CPU
U22J
10 OF 13
Coffee Lake CPU
FQ CHANGE 220UF TO 47UF/ADD 47UF X 6
+VCCCORE
DG:
20 x 47uF 0805
13 x 47uF 0603
32 x 10uF 0402
45 x 1uF 0402
MICRO-STAR INT'L CO.,LTD.
Comet lake(Power1)
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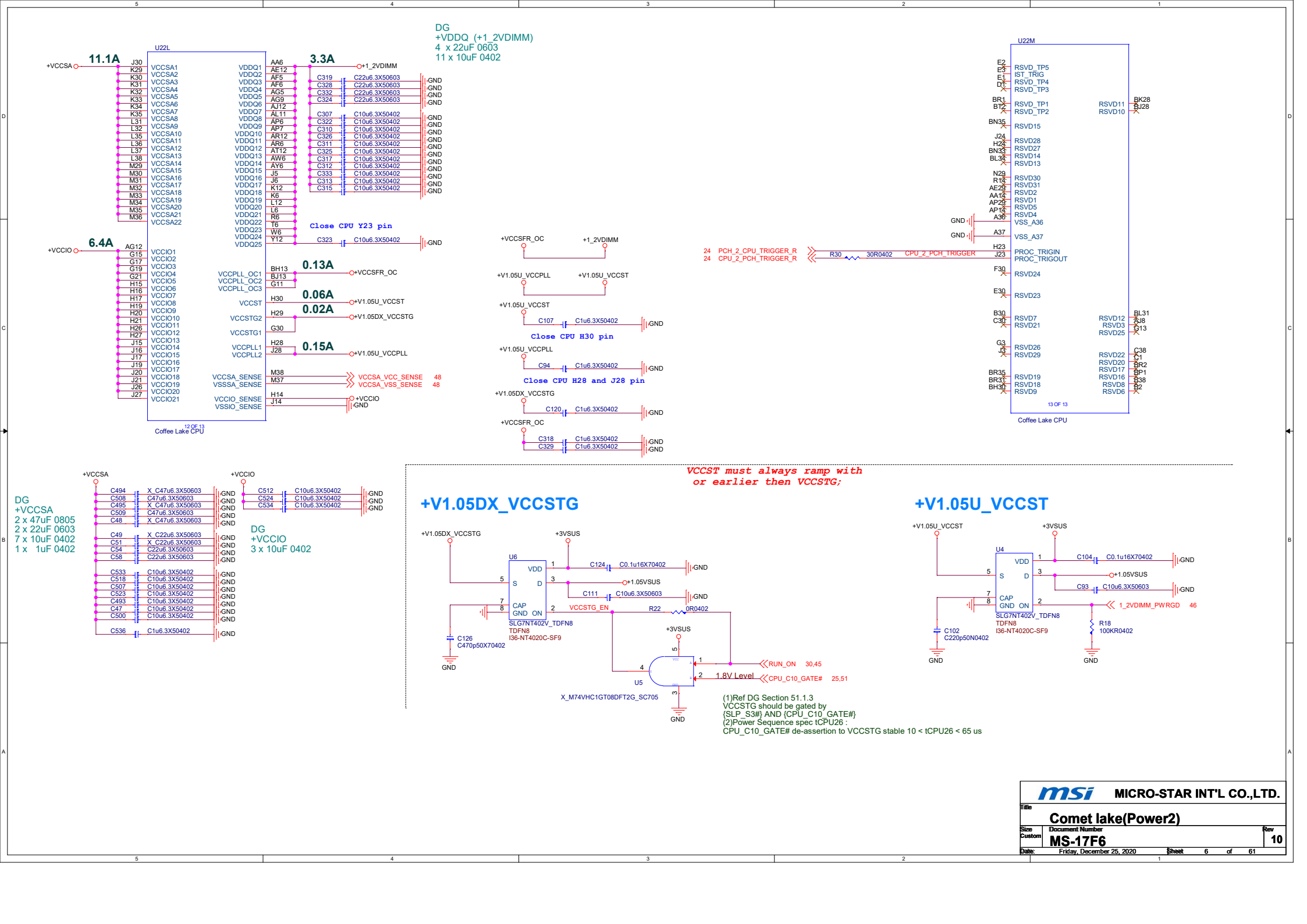
DG
+VDDQ (+1_2VDIMM)
4 x 22uF 0603
11 x 10uF 0402
11.1A
3.3A
6.4A
0.13A
0.06A
0.02A
0.15A
Close CPU Y23 pin
Close CPU H30 pin
Close CPU H28 and J28 pin
U22L
Coffee Lake CPU
U22M
Coffee Lake CPU
DG
+VCCSA
2 x 47uF 0805
2 x 22uF 0603
7 x 10uF 0402
1 x 1uF 0402
DG
+VCCIO
3 x 10uF 0402
VCCST must always ramp with or earlier then VCCSTG;
+V1.05DX_VCCSTG
+V1.05U_VCCST
SLG7NT402V_TDFN8
I36-NT4020C-SF9
X_M74VHC1GT08DFT2G_SC705
(1)Ref DG Section 51.1.3
VCCSTG should be gated by
{SLP_S3#} AND {CPU_C10_GATE#}
(2)Power Sequence spec tCPU26 :
CPU_C10_GATE# de-assertion to VCCSTG stable 10 < tCPU26 < 65 us
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Comet lake(Power2)
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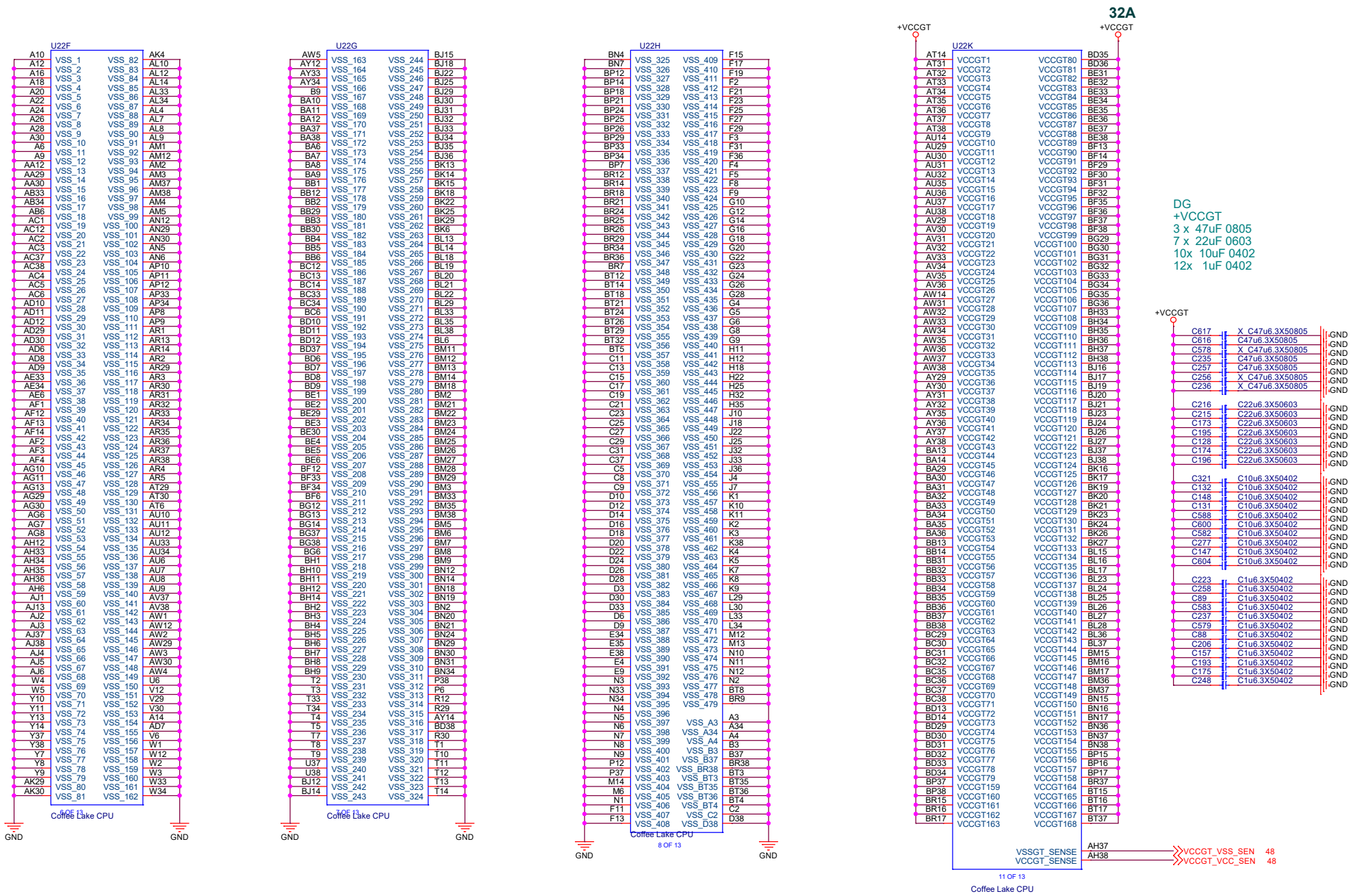

Title	Comet lake(Power3)
Size	Custom
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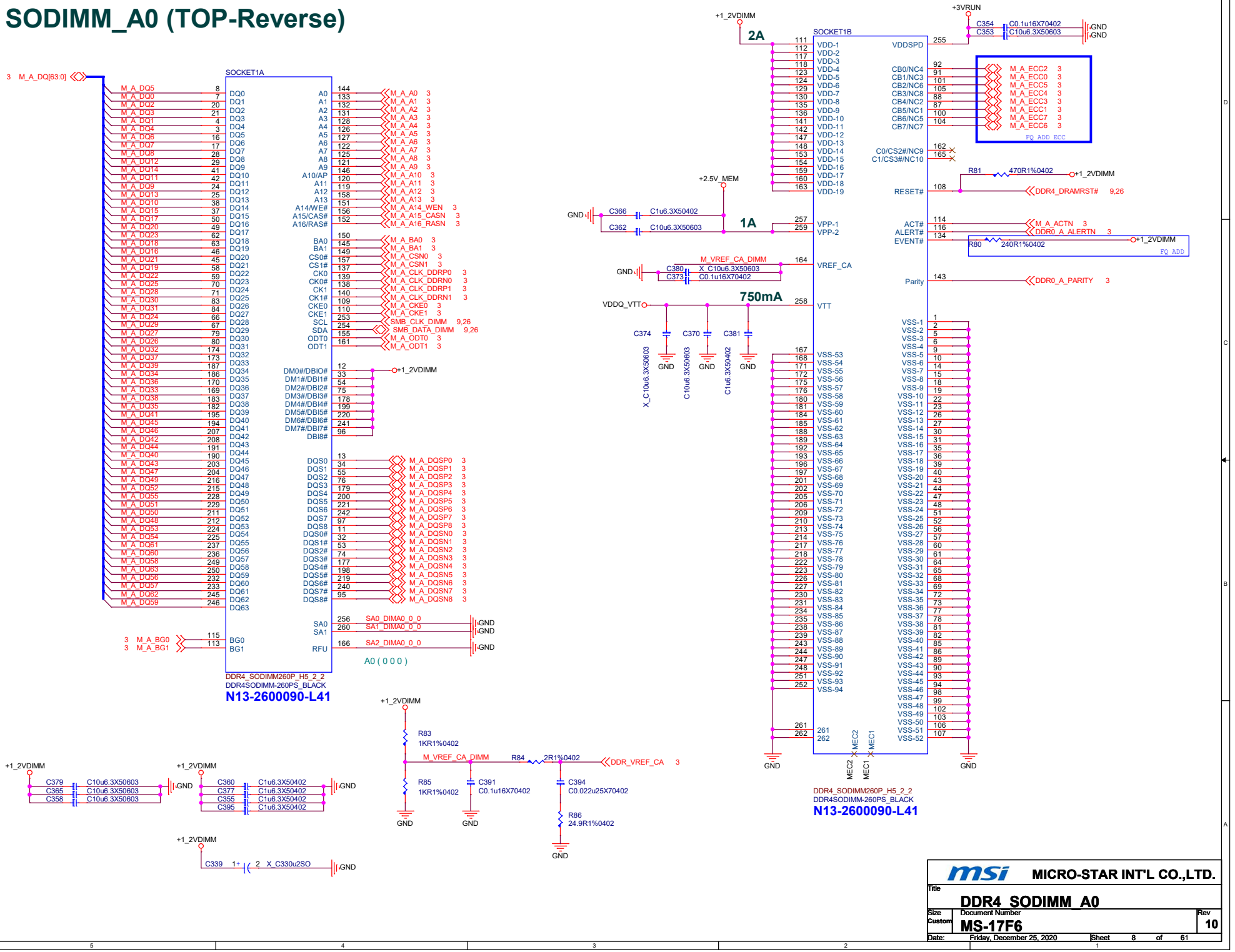
SODIMM_A0 (TOP-Reverse)



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Title	DDR4_SODIMM_A0
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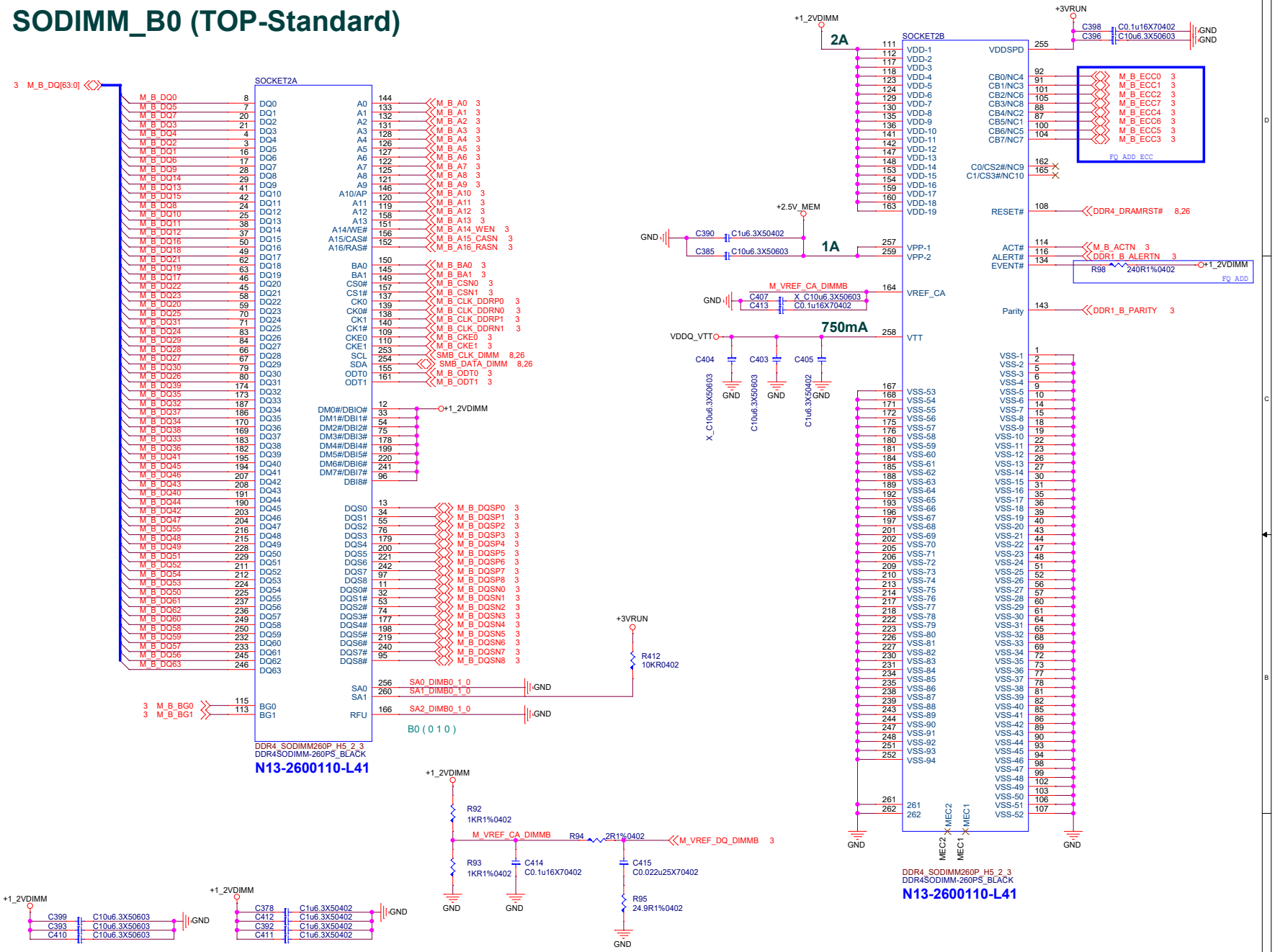
SODIMM_B0 (TOP-Standard)



Title	DDR4_SODIMM_B0
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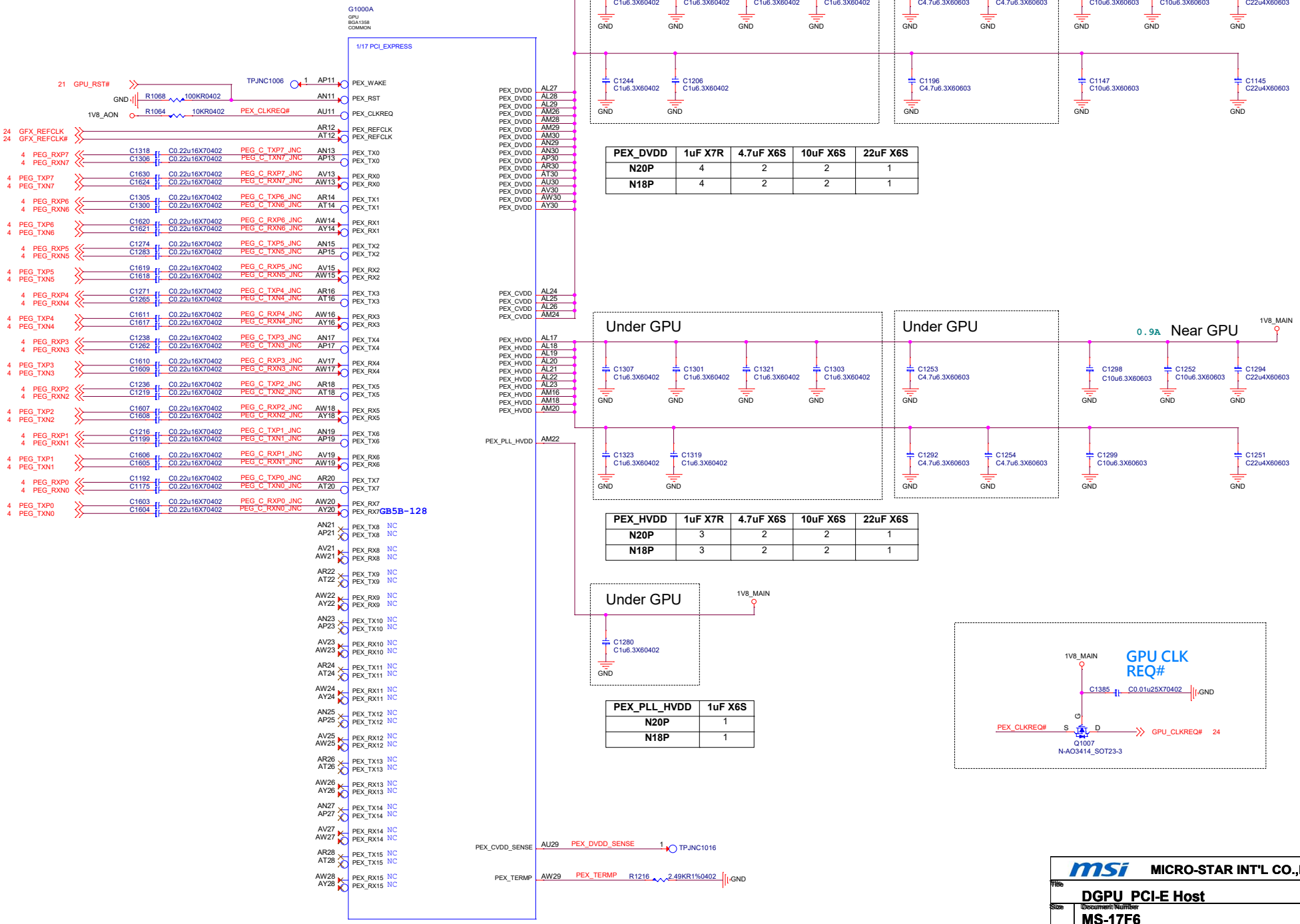
GPU PCI EXPRESS



PEX_DVDD	1uF X7R	4.7uF X6S	10uF X6S	22uF X6S
N20P	4	2	2	1
N18P	4	2	2	1

PEX_HVDD	1uF X7R	4.7uF X6S	10uF X6S	22uF X6S
N20P	3	2	2	1
N18P	3	2	2	1

PEX_PLL_HVDD	1uF X6S
N20P	1
N18P	1

MSI	MICRO-STAR INT'L CO.,LTD.		
Title	DGPU_PCI-E Host		
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GPU Frame Buffer Partition A/B

GDDR6 Command Mapping

	Channel A		Channel B	
	0~3	4~7	0~3	4~7
CMD0	CA8_A		CA8_A	
CMD1	CA0_A		CA0_A	
CMD2	CA9_A		CA9_A	
CMD3	RST*		RST*	
CMD4	CA9_B		CA9_B	
CMD5	CA0_B		CA0_B	
CMD6	CA8_B		CA8_B	
CMD7	CA2_B		CA2_B	
CMD8	CA4_B		CA4_B	
CMD9	CABI_B		CABI_B	
CMD10	CABI_A		CABI_A	
CMD11	CA4_A		CA4_A	
CMD12	CA2_A		CA2_A	
CMD13	CA1_A		CA1_A	
CMD14	CKE_A		CKE_A	
CMD15	CA5_A		CA5_A	
CMD16	CA5_B		CA5_B	
CMD17	CKE_B		CKE_B	
CMD18	CA1_B		CA1_B	
CMD19	CA7_B		CA7_B	
CMD20	CA3_B		CA3_B	
CMD21	CA6_B		CA6_B	
CMD22	CA6_A		CA6_A	
CMD23	CA7_A		CA7_A	
CMD24	CA3_A		CA3_A	
CMD25	N/A		N/A	
CMD26	N/A		N/A	
CMD27	DEBUG0		DEBUG0	
CMD28		CA8_B		CA8_B
CMD29		CA0_B		CA0_B
CMD30		CA9_B		CA9_B
CMD31		RST*		RST*
CMD32		CA9_A		CA9_A
CMD33		CA0_A		CA0_A
CMD34		CA8_A		CA8_A
CMD35		CA2_A		CA2_A
CMD36		CA4_A		CA4_A
CMD37		CABI_A		CABI_A
CMD38		CABI_B		CABI_B
CMD39		CA4_B		CA4_B
CMD40		CA2_B		CA2_B
CMD41		CKE_B		CKE_B
CMD42		CA5_B		CA5_B
CMD43		CA5_A		CA5_A
CMD44		CKE_A		CKE_A
CMD45		CA1_A		CA1_A
CMD46		CA3_A		CA3_A
CMD47		CA7_A		CA7_A
CMD48		CA6_A		CA6_A
CMD49		CA6_B		CA6_B
CMD50		CA3_B		CA3_B
CMD51		CA7_B		CA7_B
CMD52		CA1_B		CA1_B
CMD53	N/A		N/A	
CMD54	N/A		N/A	
CMD55	DBG1		DBG1	

PB_PLLVDD	1uF X6S
N20P	1
N18P	1

PB_PLLVDD	1uF X7R	4.7uF X6S	22uF X6S
N20P	1	2	1
N18P	1	2	1

FB_VREF	
N20P	2.49KR OHM pull-down
N18P	49.9R OHM pull-down

R11-499AT12-W08
49.9R1%0402

R11-2491T12-W08
2.49KR1%0402

Under GPU

Foe Partition A CMD Return Path

Foe Partition B CMD Return Path

Title	DGPU_MEM IF A/B
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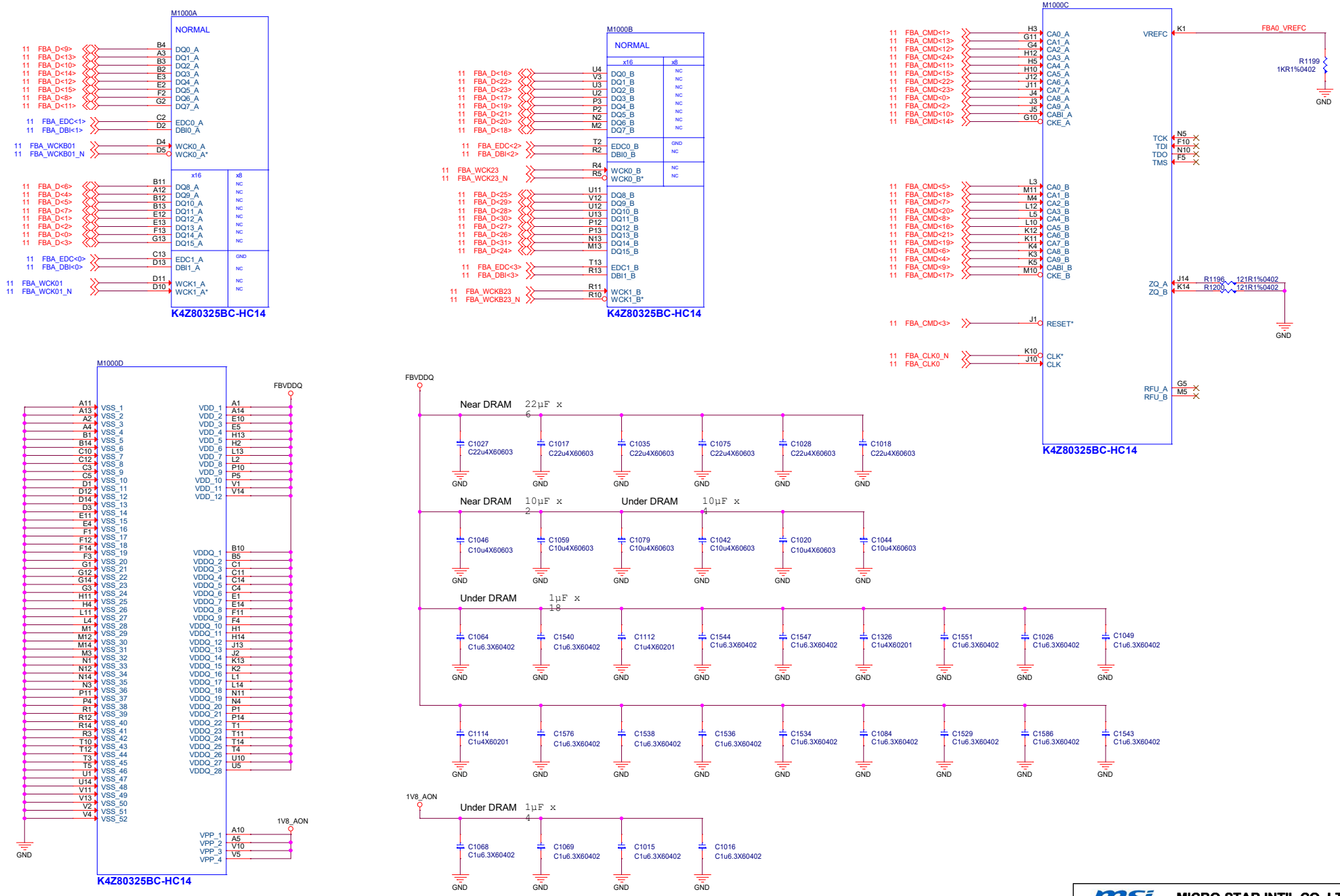
DGPU_GDDR6 FrameBuffer
A0



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Title	DGPU_GDDR6 FrameBuffer A0	
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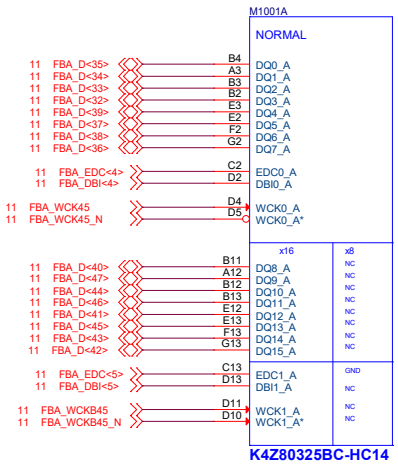
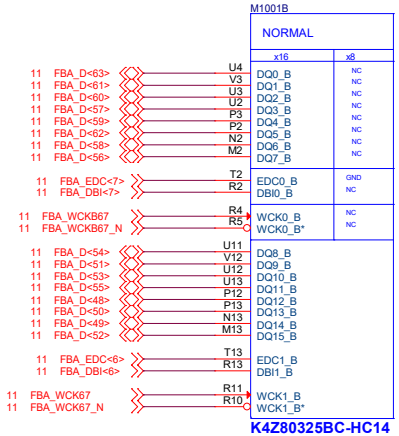
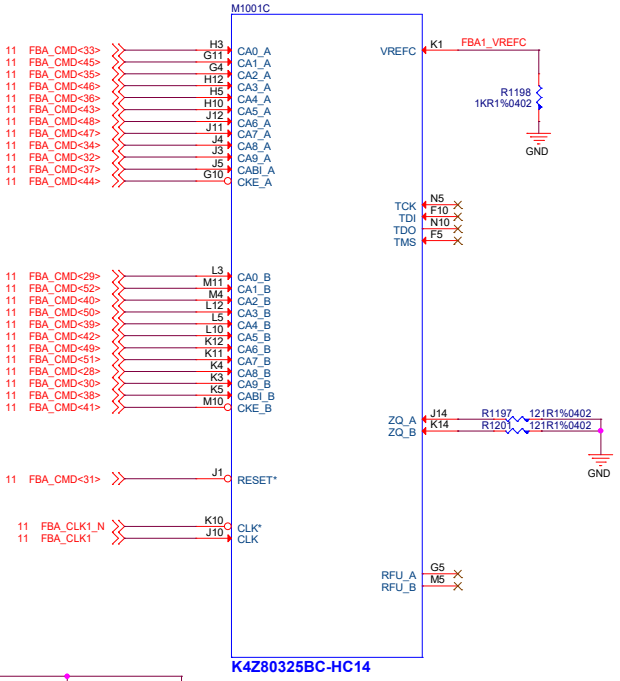
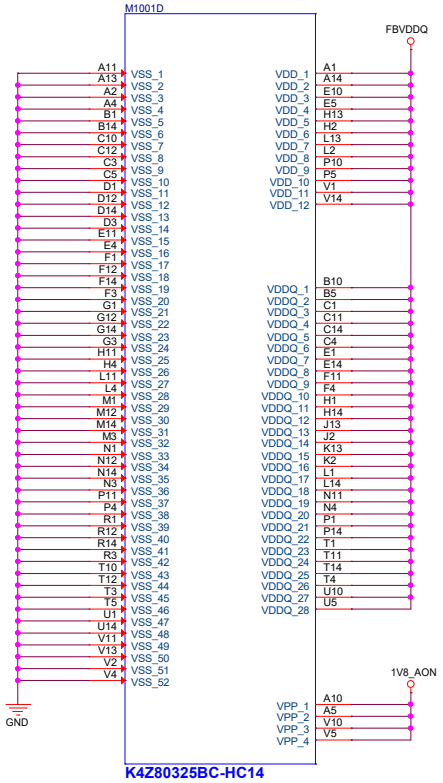
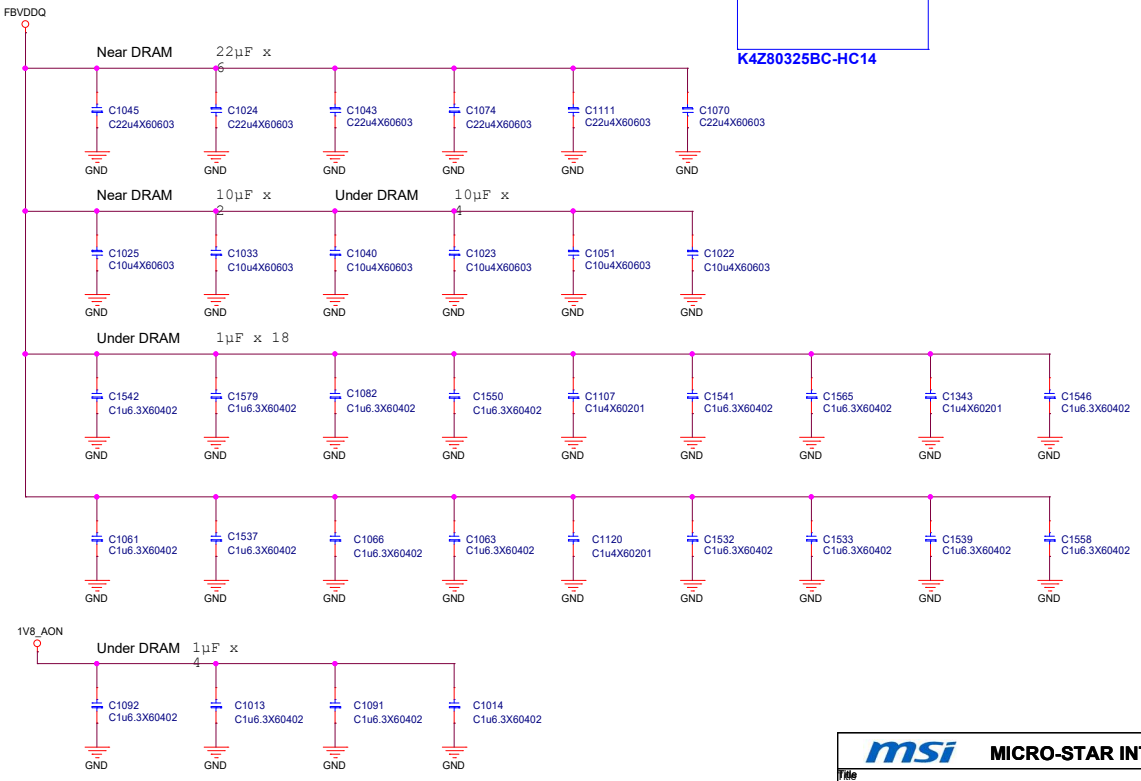
DGPU_GDDR6 FrameBuffer A1











MSI	MICRO-STAR INT'L CO.,LTD.		
Title	DGPU_GDDR6 FrameBuffer A1		
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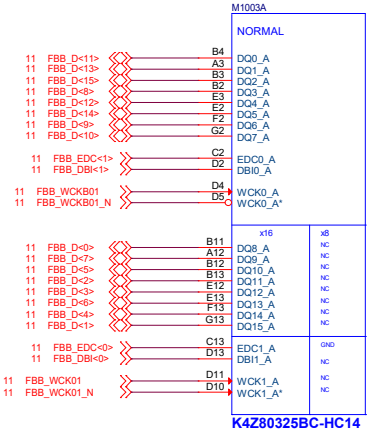
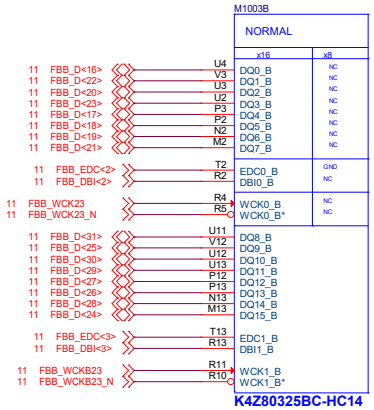
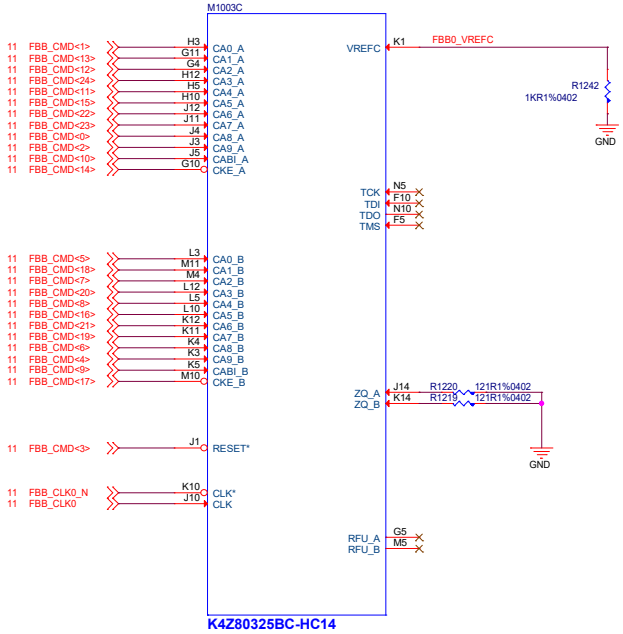
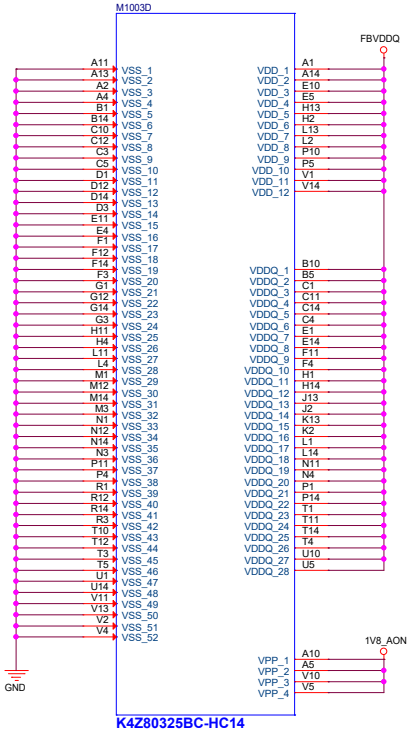
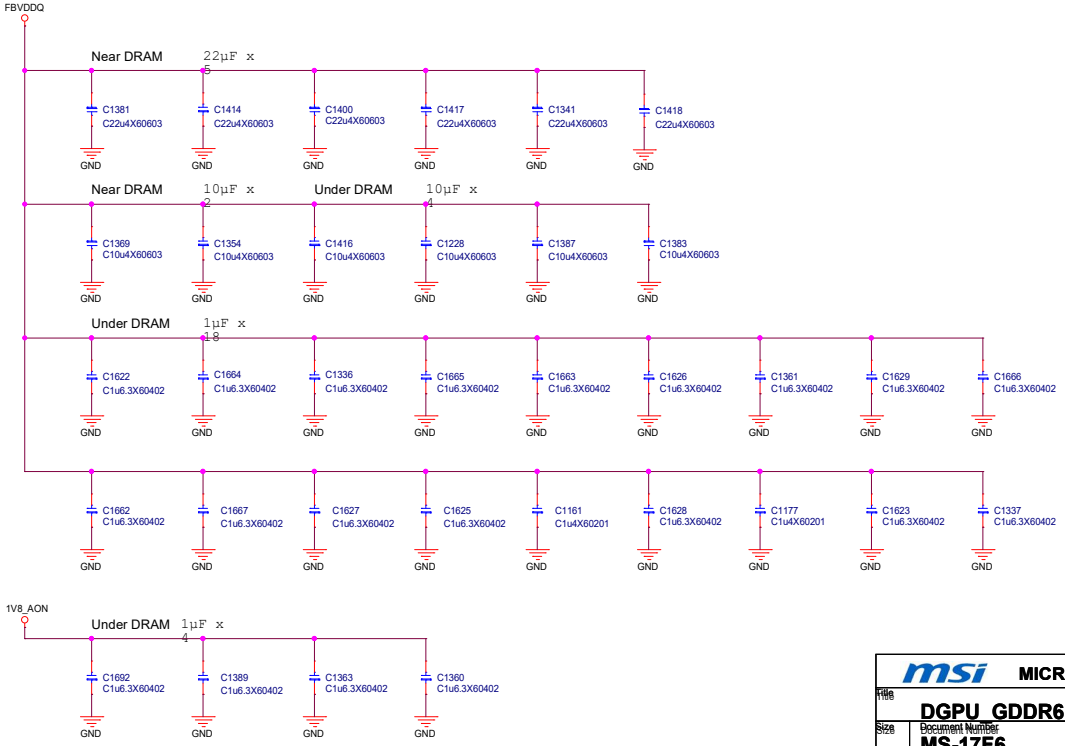
DGPU_GDDR6 FrameBuffer B0











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Title	DGPU_GDDR6 FrameBuffer B0	
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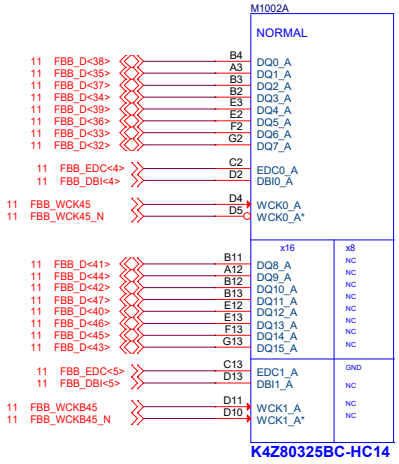
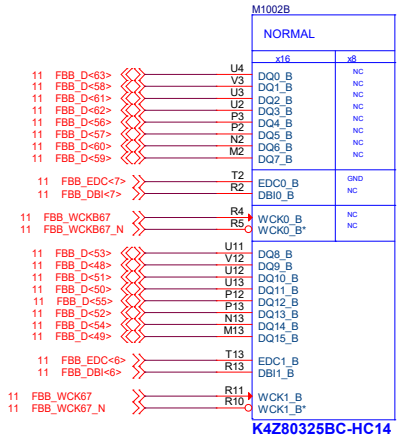
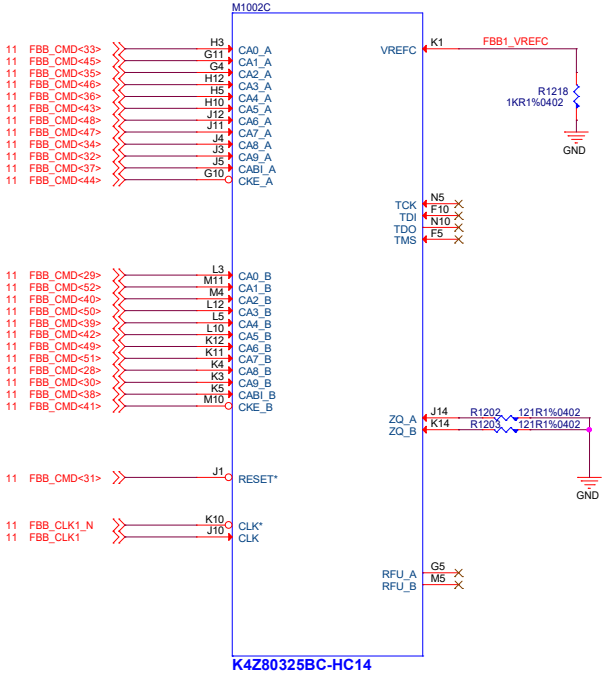
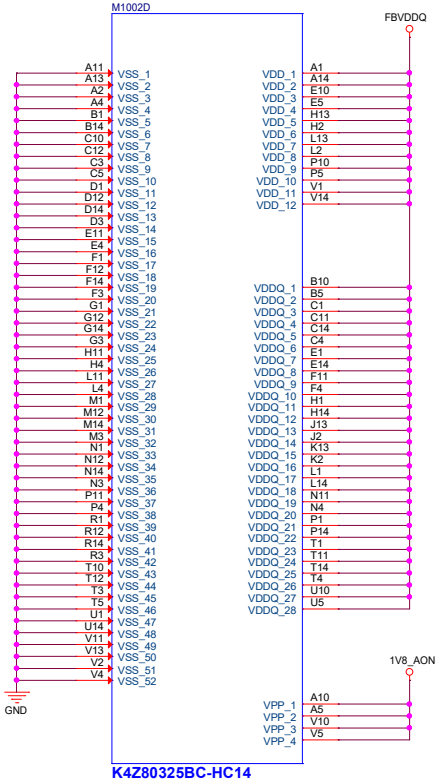
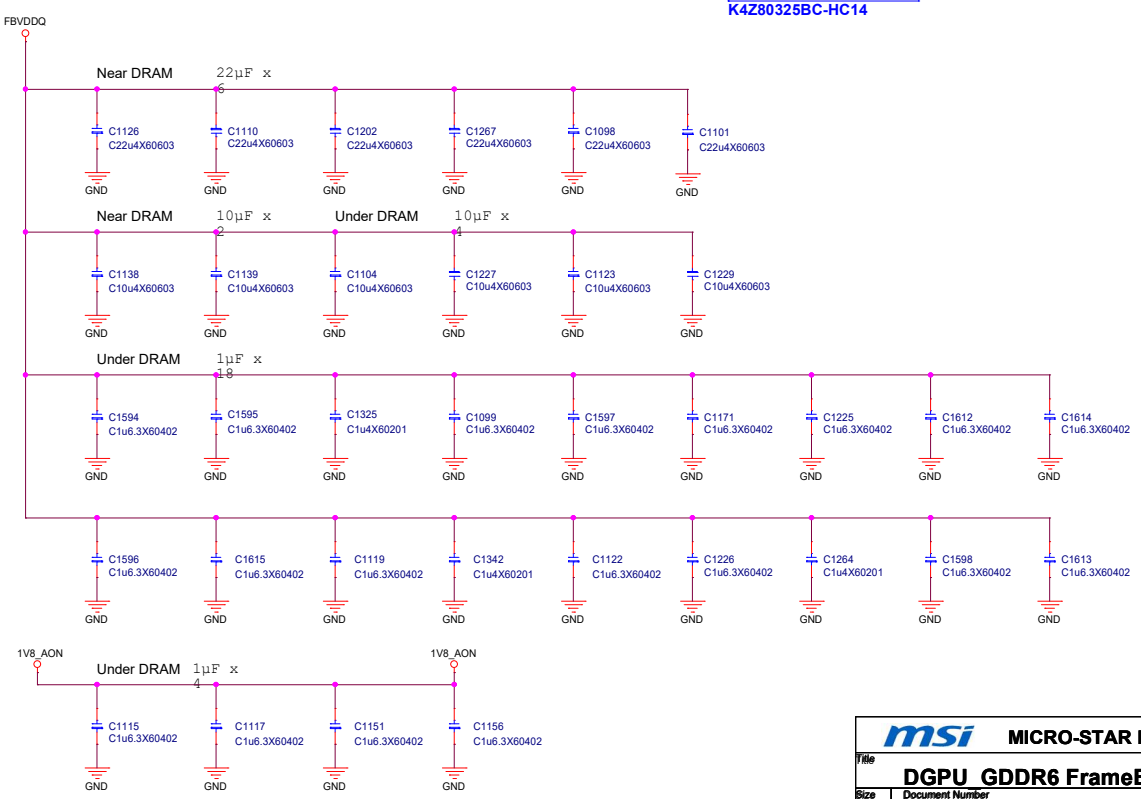
DGPU_GDDR6 FrameBuffer
B1











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Title: DGPU_GDDR6 FrameBuffer B1

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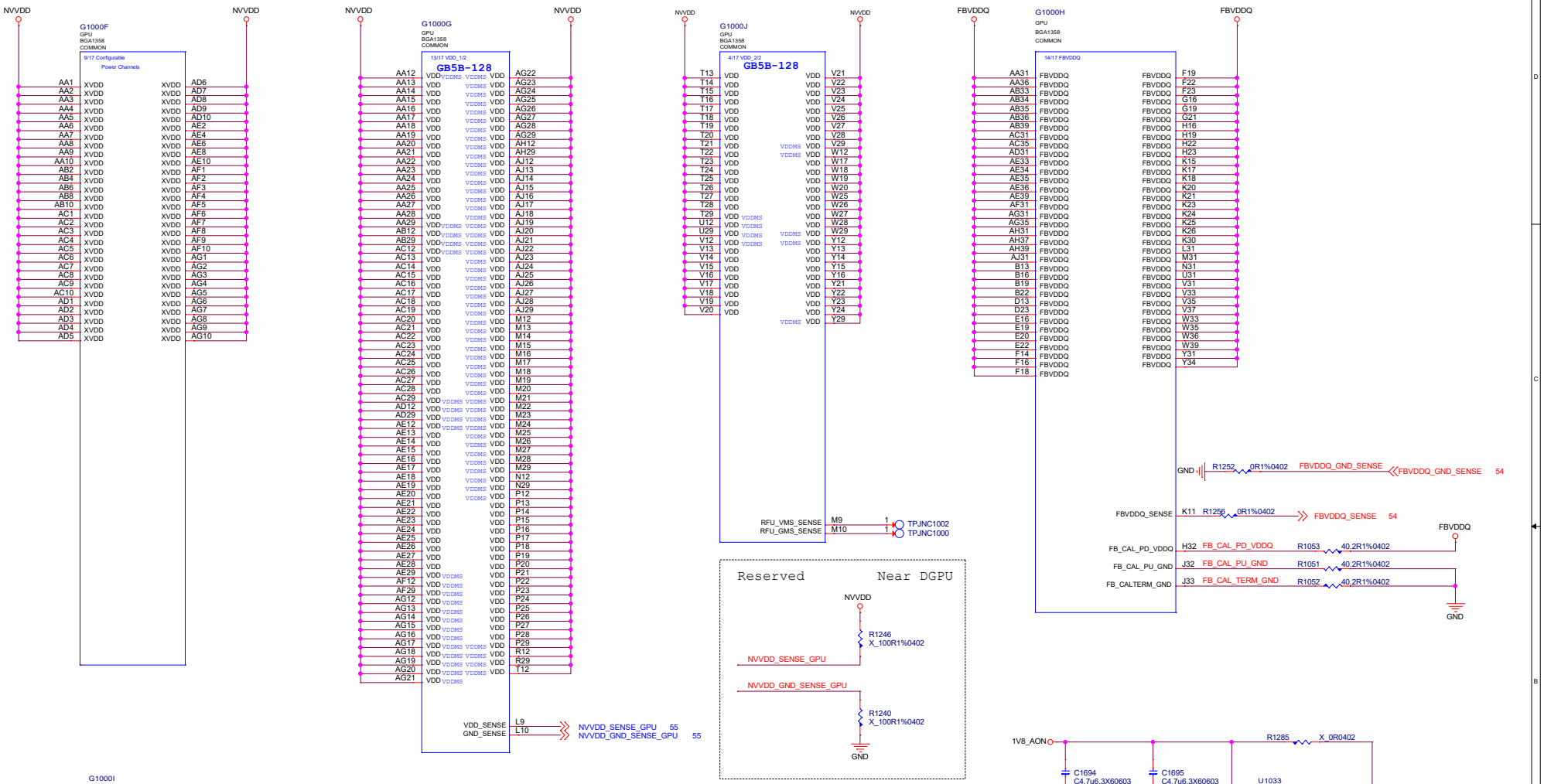
GPU NVVDD, FBVDDQ



1V8_AON	1uF X7R	4.7uF X6S
N20P	5	3
N18P	5	3

	FP_FUSE_EN
N20P	PEX_VDD_EN
N18P	GPIO26_FP_FUSE_EN

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Title: DGPU_POWER

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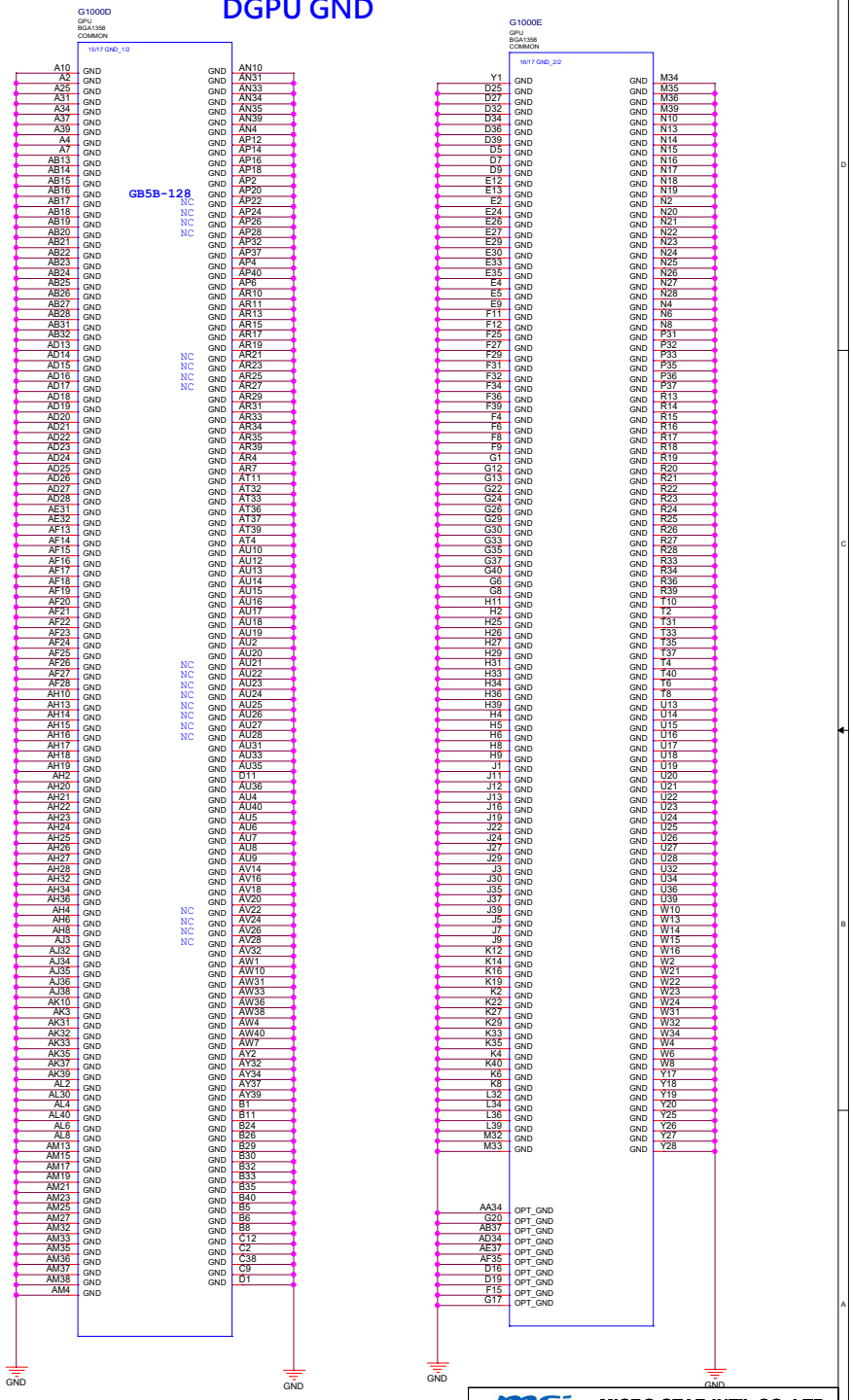
DGPU GND



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GPU DECOUPLING

NVVDD	1uF X7R	10uF X6S	22uF X6S	47uF X6S
N20P	13	34	15	4
N18P	13	34	15	

Design Guide: (P46)
NVVDD : 37 x 1uF (0402 X6S)
2 x 4.7uF(0603 X6S)
12 x 10uf (0603 X6S)
4 x 47uF (0805)

Co-layout : 3X330uF (7343)
OR
12 X 1uF
3 X 4.7uF
3 X10uF
16 X47uF

FBVDDQ	1uF X7R	10uF X6S	22uF X6S
N20P	12	6	5
N18P	12	6	5

NVVDD

Place Under to GPU 1uF*13pcs

C1371 C1u4X60201 | C1345 C1u6.3X60402 | C1214 C1u4X60201 | C1211 C1u4X60201 | C1279 C1u6.3X60402 | C1352 C1u4X60201 | C1302 C1u6.3X60402 → GND

C1235 C1u6.3X60402 | C1212 C1u4X60201 | C1313 C1u4X60201 | C1266 C1u6.3X60402 | C1213 C1u4X60201 | C1347 C1u4X60201 → GND

Place Under to GPU 10uF*34pcs

C1328 | C1296 | C1246 | C1289 | C1331 | C1288 | C1338 | C1315 | C1314 | C1194 C10u6.3X60603 → GND

C1346 | C1297 | C1242 | C1243 | C1348 | C1330 | C1351 | C1333 | C1291 | C1290 C10u6.3X60603 → GND

C1247 | C1249 | C1329 | C1316 | C1332 | C1322 | C1293 | C1245 | C1317 | C1327 C10u6.3X60603 → GND

C1295 | C1350 | C1248 | C1250 C10u6.3X60603 → GND

Place Under to GPU 22uF*10pcs

C1660 | C1384 | C1659 | C1396 | C1356 | C1368 | C1658 | C1657 | C1656 | C1409 C22u4X60603 → GND

Place Near to GPU 3 x 470UF 30x47UF

C1643 X_C470u2SO | C1650 | C1681 | C1685 | C1427 | C1674 | C1376 | C1687 | C1686 | C1399 | C1424 C47u4X60805 → GND

C1404 X_C470u2SO | C1402 | C1669 | C1634 | C1670 | C1428 | C1401 | C1426 | C1635 | C1661 | C1403 C47u4X60805 → GND

C1422 X_C470u2SO | C1390 | C1406 | C1393 | C1391 | C1410 | C1394 | C1359 | C1382 | C1408 | C1407 C47u4X60805 → GND

FBVDDQ

Partition A Place Under to GPU :2 X 10UF, 6 X 1UF

C1545 C1u6.3X60402 | C1105 C1u4X60201 | C1140 C1u4X60201 | C1552 C1u6.3X60402 | C1553 C1u6.3X60402 | C1312 C1u4X60201 → GND

C1037 C10u6.3X60603 | C1182 C10u6.3X60603 → GND

Partition B Place Under to GPU :2 X 10UF, 6X 1UF

C1304 C1u4X60201 | C1285 C1u4X60201 | C1311 C1u4X60201 | C1324 C1u4X60201 | C1273 C1u6.3X60402 | C1124 C1u4X60201 → GND

C1339 C10u6.3X60603 | C1320 C10u6.3X60603 → GND

Place Near to GPU 2 x 10UF 5 x 22UF

C1034 C10u6.3X60603 | C1340 C10u6.3X60603 | C1335 C22u4X60603 | C1334 C22u4X60603 | C1189 C22u4X60603 | C1031 C22u4X60603 | C1019 C22u4X60603 → GND

MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GPU DECOUPLING

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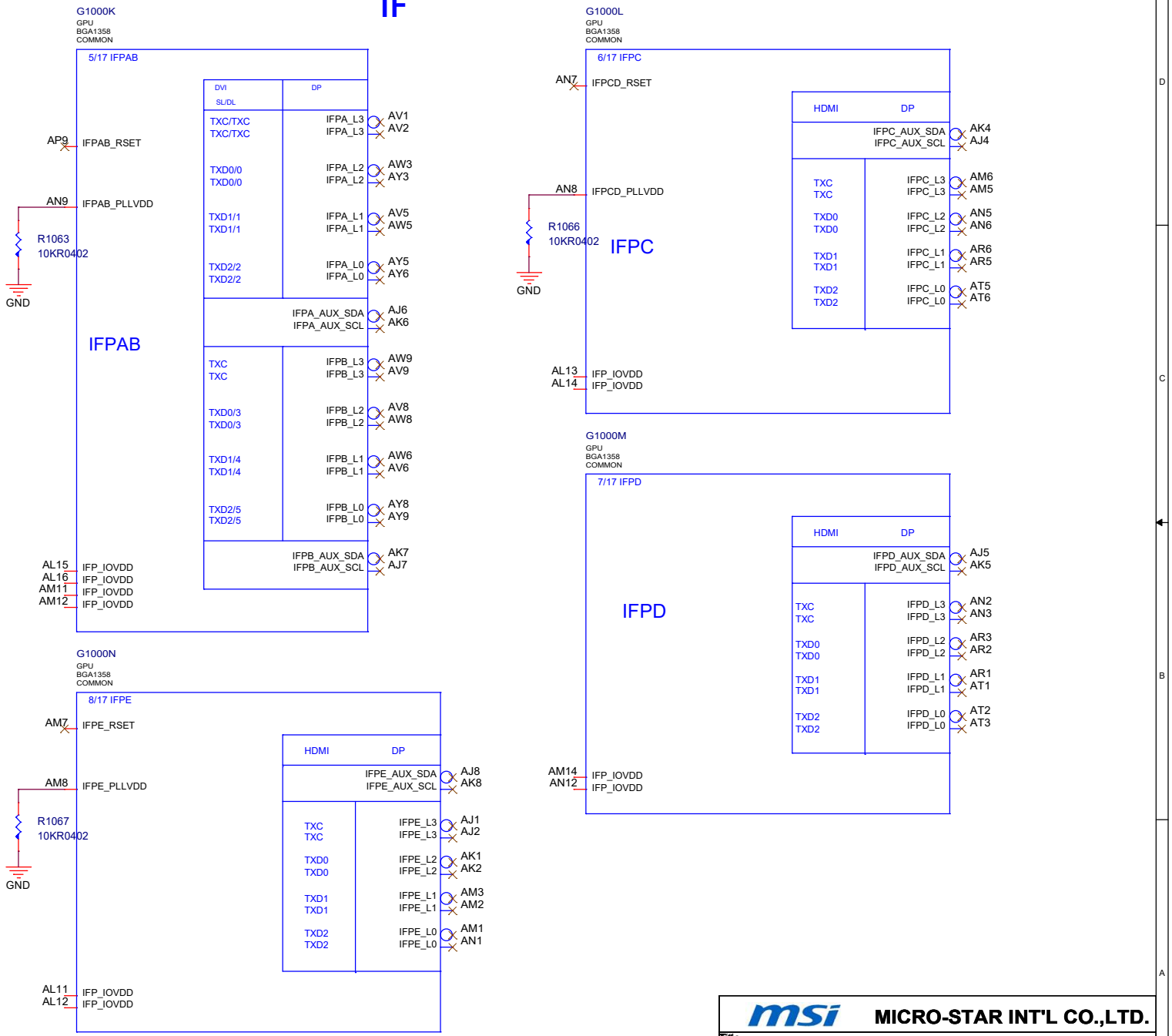
DACA,Display IF



MICRO-STAR INT'L CO.,LTD.		
Title: DGPU_Display IF		
Size	Document Number: MS-17F6	Rev: 10
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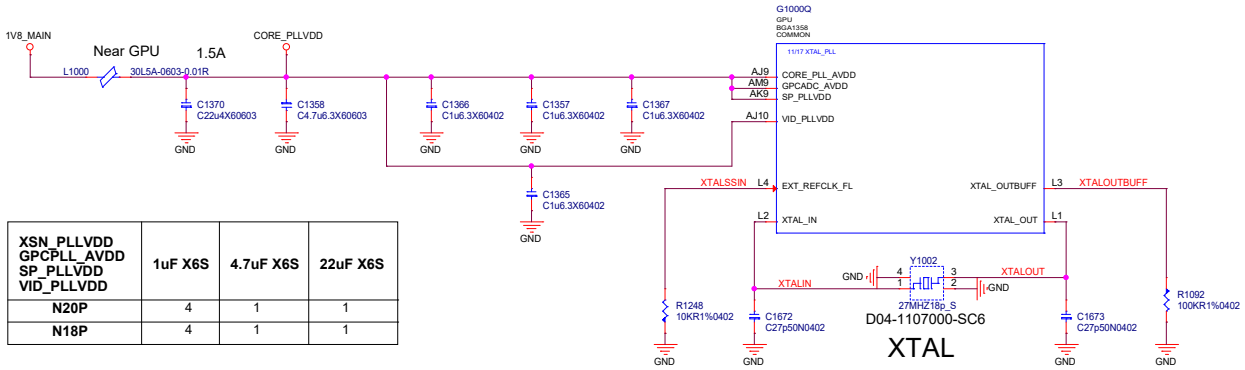
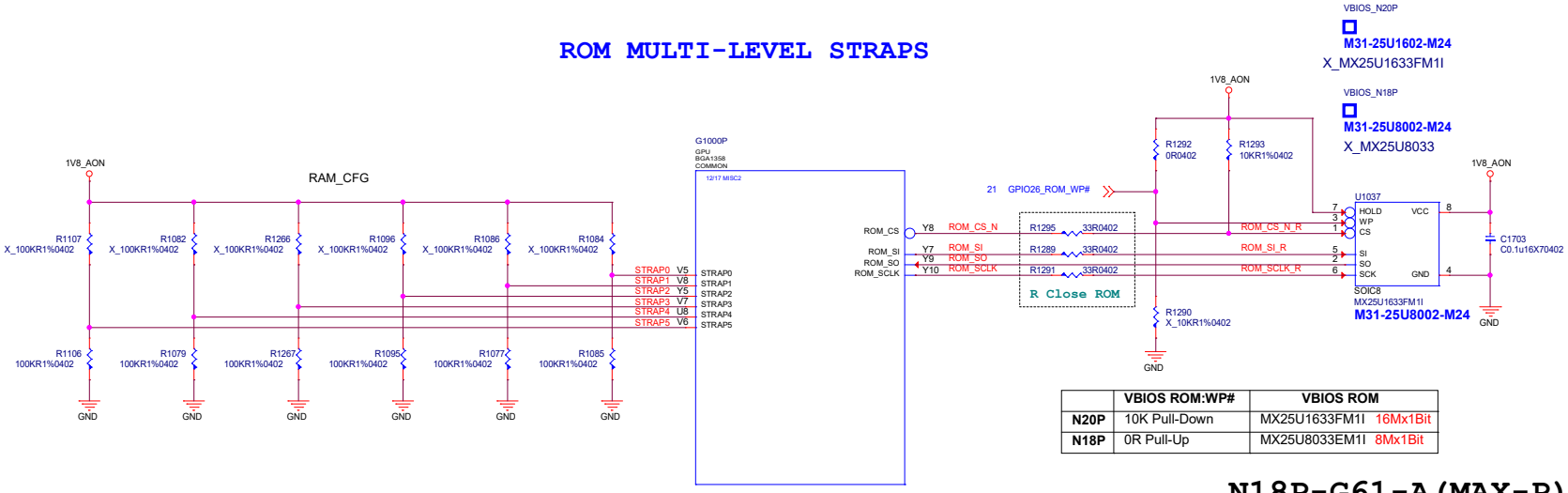
DGPU XTAL

Under GPU

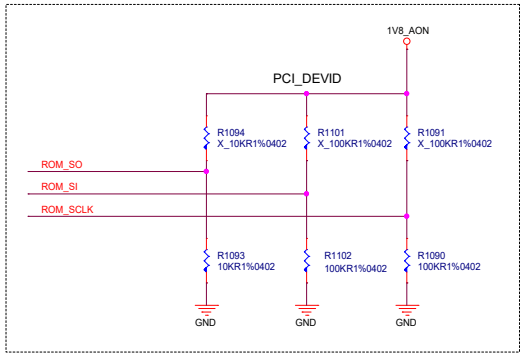


XSN_PLLVDD GPCPLL_AVDD SP_PLLVDD VID_PLLVDD	1uF X6S	4.7uF X6S	22uF X6S
N20P	4	1	1
N18P	4	1	1

ROM MULTI-LEVEL STRAPS



	VBIOS ROM:WP#	VBIOS ROM
N20P	10K Pull-Down	MX25U1633FM1I 16Mx1Bit
N18P	0R Pull-Up	MX25U8033EM1I 8Mx1Bit



STRAP 5	STRAP 4	STRAP 3	
L	L	L	Optimus
L	L	H	Discrete
H	L	H	Discrete with Gsync

STRAP 2	STRAP 1	STRAP 0		N18P-G61-A	GN20-P1/P0
L	L	L	0x0	Samsung K4Z80325BC-HC14	Samsung K4Z80325BC-HC14
L	L	H	0x1	Micron MT61K256M32JE-14:A	Micron MT61K256M32JE-14:A
L	H	L	0x2		Hynix H56C8H24AIR-S2C

			FS_OVERT# Function	
ROM_SO	ROM_SI	ROM_SCLK	N18P-G61-A	GN20-P1/P0
L	L	L	ENABLED	DISABLED
L	L	H	DISABLED	ENABLED
L	H	L	Invalid Do not configure	
L	H	H		
H	H	H		
H	H	M		

N18P-G61-A (MAX-P)

G1_N18P
OB3-16R5001-N08
X_N18P-G61-A (QS)

GN20-P0 (Max-Q)

G1000_GN20
OB3-14C5001-N08
X_GN20-P0 (P QS1)

GN20-P1 (Max-Q)

G1_GN20-P1
OB3-1591001-N08
X_GN20-P1

MICRO-STAR INT'L CO.,LTD.

Title: DGPU_XTAL/ROM/HW Straps

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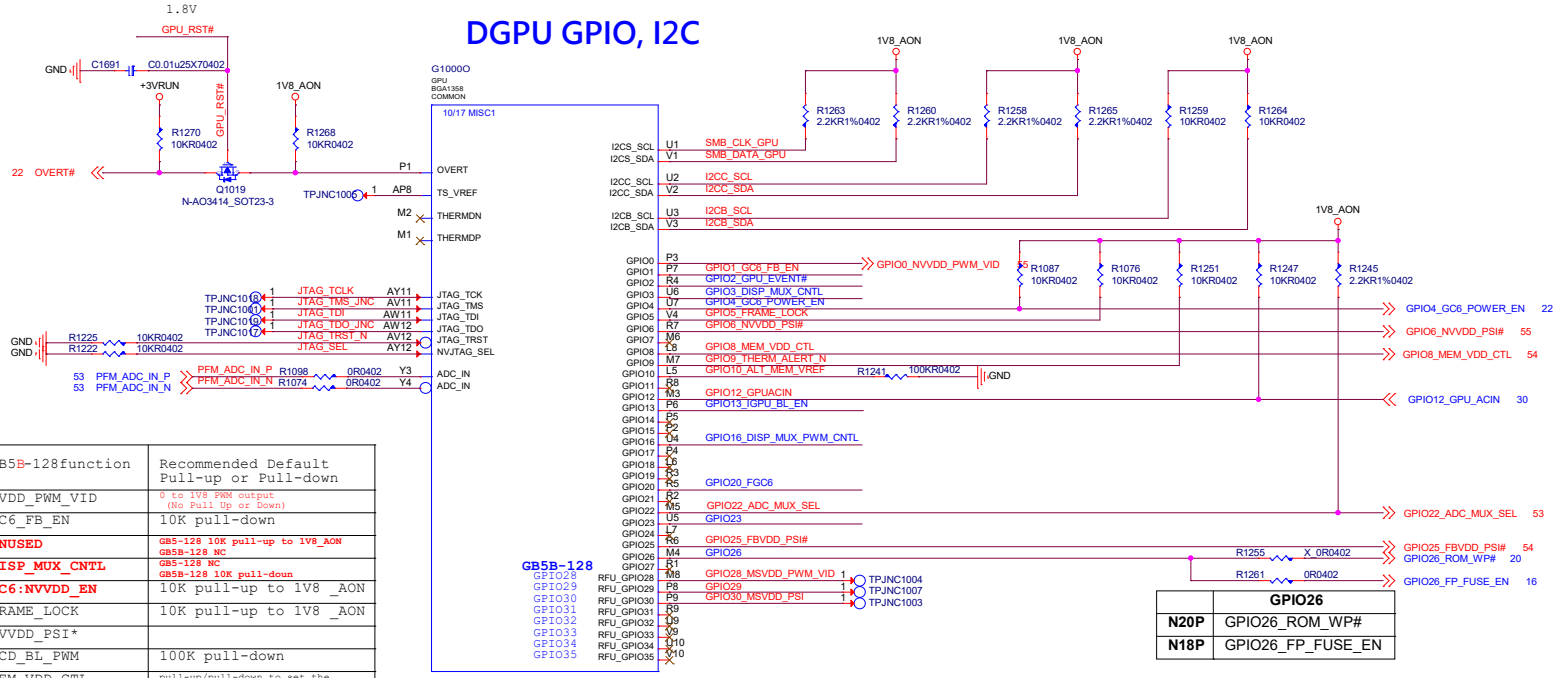
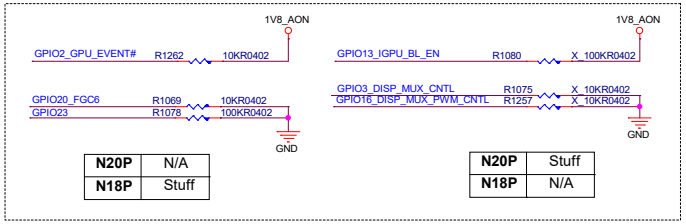
DGPU GPIO, I2C



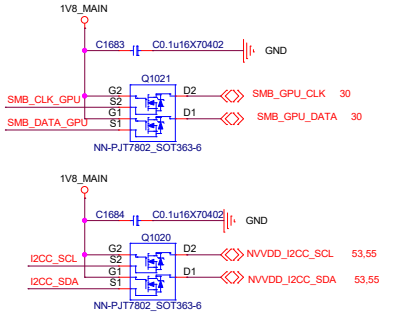
	GPIO26
N20P	GPIO26_ROM_WP#
N18P	GPIO26_FP_FUSE_EN

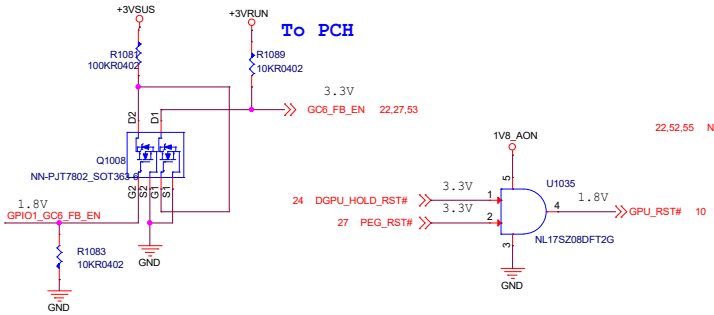
Pin Name	GB5-128function	GB5B-128function	Recommended Default Pull-up or Pull-down
GPIO0	NVDD_PWM_VID	NVDD_PWM_VID	0 to 1V8 PWM output (No Pull Up or Down)
GPIO1	GC6_FB_EN	GC6_FB_EN	10K pull-down
GPIO2	**GC6_GPU_EVENT**	**UNUSED**	GB5-128 10K pull-up to 1V8_AON GB5B-128 NC
GPIO3	**UNUSED**	**DISP_MUX_CNTL**	GB5-128 NC GB5B-128 10K pull-doun
GPIO4	**GC6:1V8_MAIN_EN**	**GC6:NVVDD_EN**	10K pull-up to 1V8 _AON
GPIO5	FRAME_LOCK	FRAME_LOCK	10K pull-up to 1V8 _AON
GPIO6	NVVDD_PSI*	NVVDD_PSI*	
GPIO7	LCD_BL_PWM	LCD_BL_PWM	100K pull-down
GPIO8	MEM_VDD_CTL	MEM_VDD_CTL	pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT*	THERM_ALERT*	10K pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	MEM_VREF_CTL	100K pull-down
GPIO11	LCD_VCC	LCD_VCC	100K pull-down
GPIO12	PWR_LEVEL	PWR_LEVEL	10K pull-up to 1V8_AON
GPIO13	**UNUSED**	**IGPU_BL_EN**	GB5-128 NC GB5B-128 100K pull-up to 1V8_AON
GPIO14	HPD_IFPA*	HPD_IFPA*	10K pull-up to 1V8_AON
GPIO15	HPD_IFPB*	HPD_IFPB*	10K pull-up to 1V8_AON
GPIO16	**UNUSED**	**DISP_MUX_PWN_CNTL**	GB5-128 NC GB5B-128 10K pull-down
GPIO17	HPD_IFPD*	HPD_IFPD*	10K pull-up to 1V8_AON
GPIO18	HPD_IFPE*	HPD_IFPE*	10K pull-up to 1V8_AON
GPIO19	**UNUSED**	**3D VISION/STEREO**	
GPIO20	**GC6_NB_GC6**	**UNUSED**	GB5-128 10K pull-doun(Reserve) GB5B-128 NC
GPIO21	LCD_BLEN	LCD_BLEN	100K pull-down
GPIO22	ADC_MUX_SEL	ADC_MUX_SEL	2.2K pull-up to 1V8_AON
GPIO23	**RESERVED**	**UNUSED**	GB5-128 100K pull-doun(Reserve) GB5B-128 NC
GPIO24	**UNUSED**	**HPD_IFPE***	GB5-128 NC GB5B-128 10K pull-up to 1V8_AON
GPIO25	FBVDD_PSI*	FBVDD_PSI*	
GPIO26	**FP_FUSE**	**ROM_WP***	FP_FUSE 10K pull-doun ROM_WP* 10K pull-down
GPIO27	HPD_IFPC*	HPD_IFPC*	10K pull-up to 1V8_AON
GPIO28	**N/A**	**MSVDD_PWM_VID**	0 to 1V8 PWM output (No Pull Up or Down)
GPIO29	**N/A**	**RESERVED**	
GPIO30	**N/A**	**MSVDD_PSI**	
GPIO31	**N/A**	**UNUSED**	
GPIO32	**N/A**	**UNUSED**	
GPIO33	**N/A**	**UNUSED**	
GPIO34	**N/A**	**UNUSED**	
GPIO35	**N/A**	**UNUSED**	

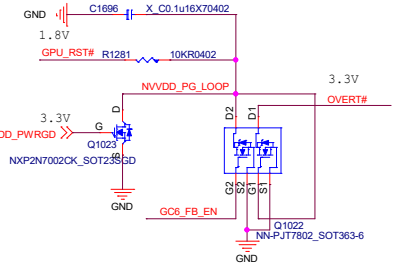


N20P	N/A
N18P	Stuff

N20P	Stuff
N18P	N/A







msi	MICRO-STAR INT'L CO.,LTD.		
Title	DGPU_GPIO/I2C		
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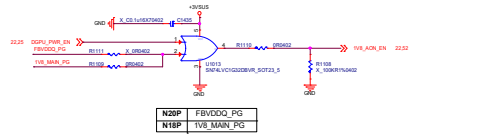
nVIDIA Power Sequence Control

N20P Power On = 1V8_AON -> NVVDD -> PEX_VDD -> FBVDDQ -> DGPUPWRGD
N18P Power On = 1V8_AON -> 1V8_MAIN -> NVVDD -> PEX_VDD -> FBVDDQ -> DGPUPWRGD

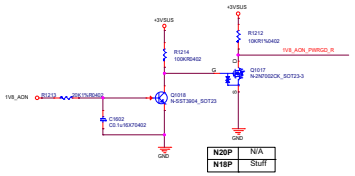
N20P Power Down = PEX_VDD -> NVVDD -> FBVDDQ -> 1V8_AON
N18P Power Down = PEX_VDD -> NVVDD -> FBVDDQ -> 1V8_MAIN -> 1V8_AON

1V8_AON



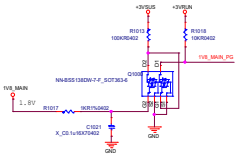
N20P	FBVDDQ_PG
N18P	1V8_MAIN_PG

1V8_AON POWER GOOD

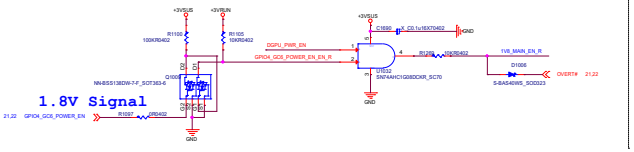


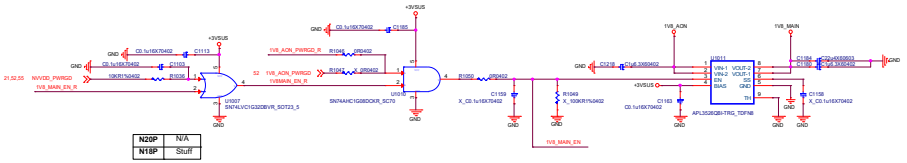
N20P	N/A
N18P	Stuff

1V8_MAIN POWER GOOD



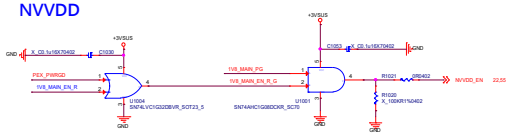
1V8_MAIN



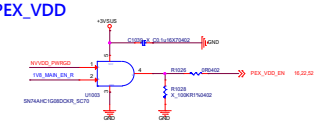


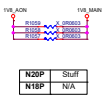
N20P	N/A
N18P	Stuff

NVVDD



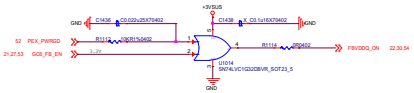
PEX_VDD



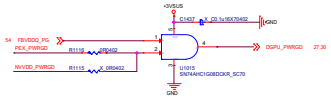


N20P	Stuff
N18P	N/A

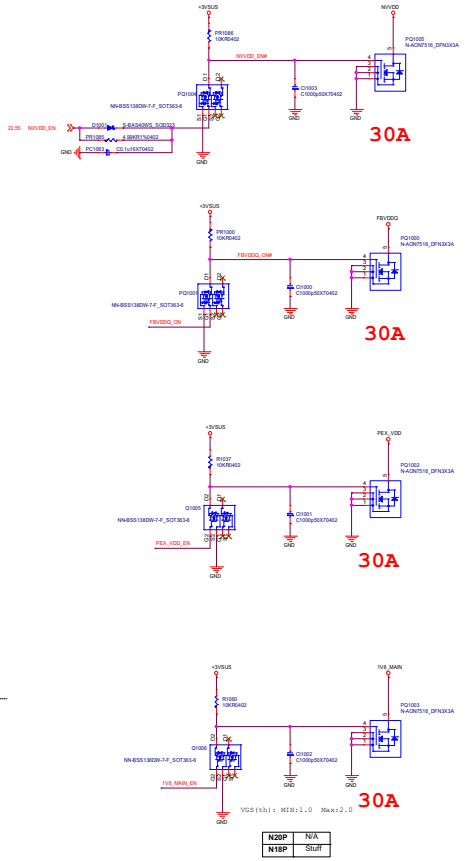
FBVDDQ



DGPU POWER GOOD



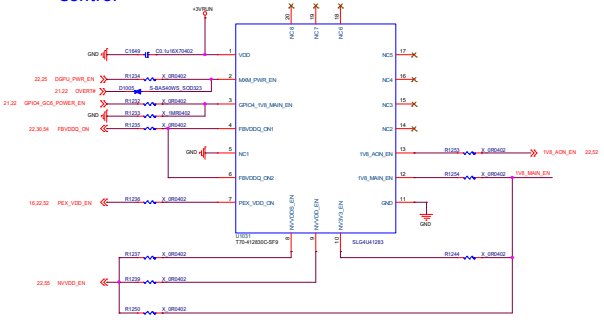
Discharge



VGS(th): MIN:1.0 Max:2.0

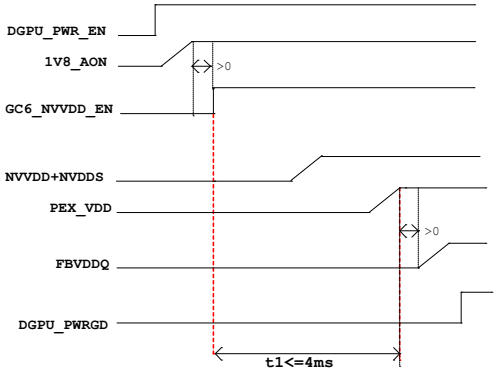
N20P	N/A
N18P	Stuff

Power Sequence Control



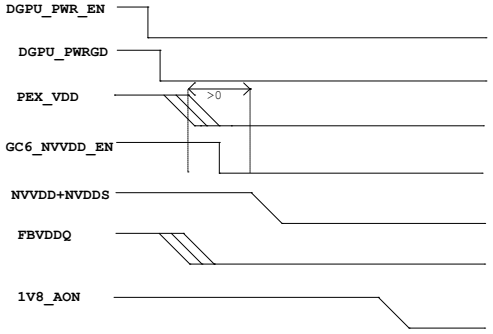
POWER UP Sequence

Power On = 1V8_AON -> NVVDD -> PEX_VDD -> FBVDDQ -> DGPUPWRGD

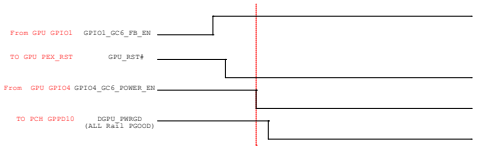


POWER Down Sequence

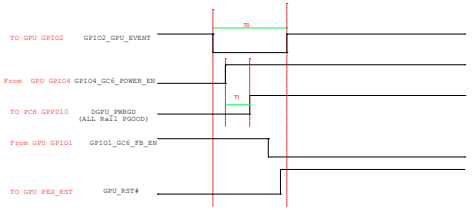
Power Down = PEX_VDD -> NVVDD -> FBVDDQ -> 1V8_AON



GC6 3.0 ENTRY SEQUENCE



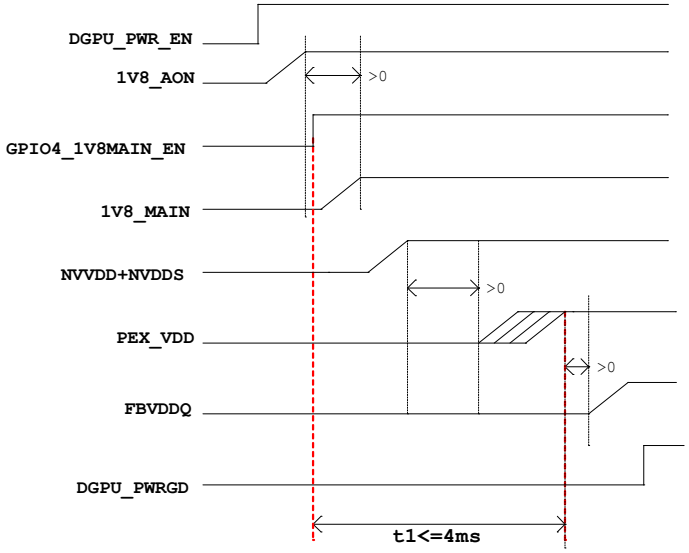
GC6 3.0 EXIT SEQUENCE



MICRO-STAR INT'L CO.,LTD.
Title: DGPU_POWER_Sequence_Control
Size: Document Number: MS-17F6 Rev: 1.0
Date: Friday, December 25, 2020 Sheet 22 of 57

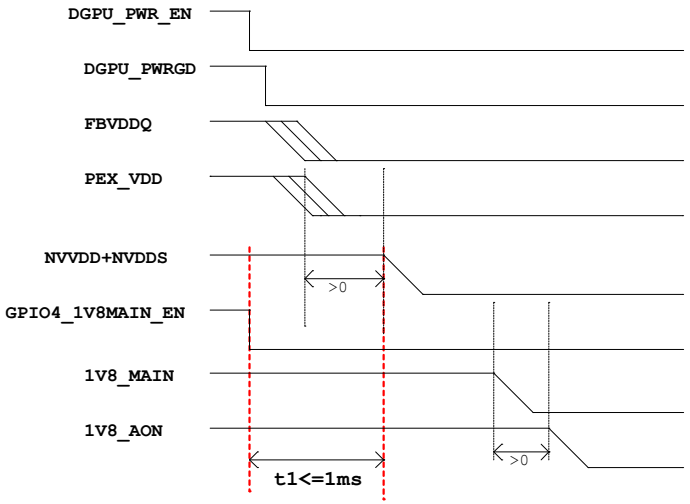
POWER UP Sequence

1V8_AON -> 1V8_MAIN->NV3V3 -> NVVDD -> NVVDDS / PEX_VDD -> FBVDDQ

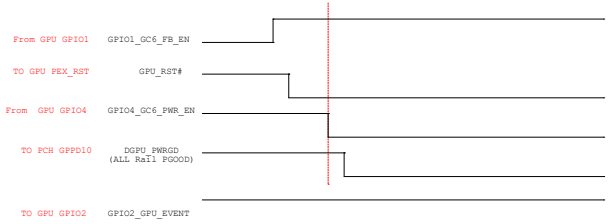


POWER Down Sequence

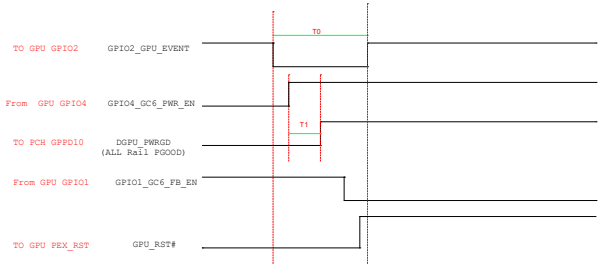
NVVDDS/PEX_VDD/FBVDDQ ->NVVDD/NV3V3->1V8_MAIN> 1V8_AON



GC6 2.1 ENTRY SEQUENCE



GC6 2.1 EXIT SEQUENCE



GC6 2.1 TIMING

	Min	Max	Unit	Description
T0	0.001	N/A	mS	GPU_EVENT# assertion
T1	0.04	4	mS	3V3_MAIN_EN assertion to all power rails up and stable

NOTES:

1. ALL RailPGOOD=1 represents all GPU power rails are ramped up and in regulation.
   If any GPU power rail cannot ge guaranteed in regulation this state should equal to 0.
2. During GC6 exit, the order of power rail ramp-up must follow the Power up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
3. All delays should be minimized to increase time spent in GC6 for maximum power saving.
4. The entire entry and exit sequence must complete within 200 ms.

MICRO-STAR INT'L CO.,LTD.

Title: DGPU_Power Sequence

Size: Custom | Document Number: MS-17F6 | Rev: 10

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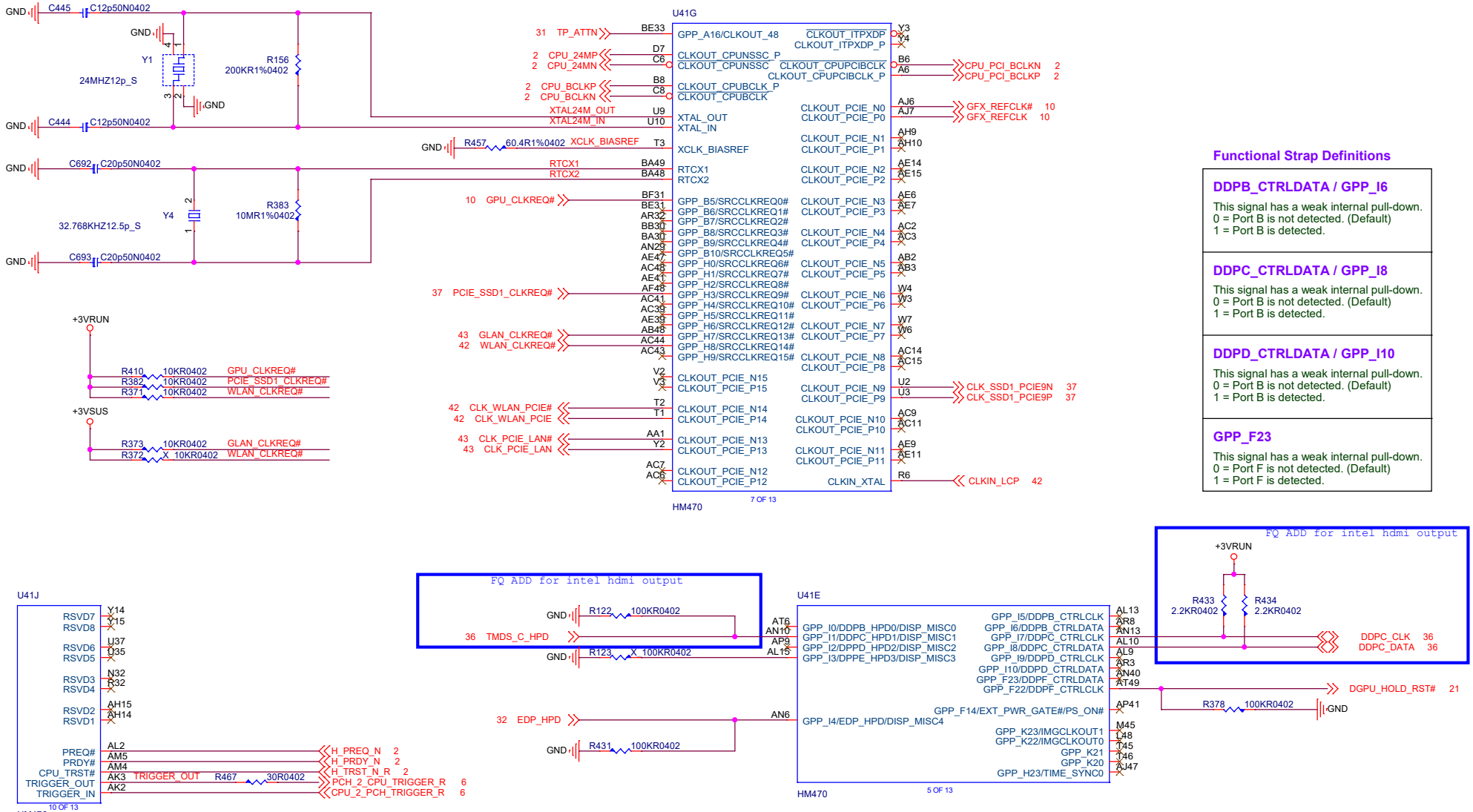
HM370 (RTC/PCIE_Clock/Clock/RSVD)



Functional Strap Definitions

DDPB_CTRLDATA / GPP_I6

This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

DDPC_CTRLDATA / GPP_I8

This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

DDPD_CTRLDATA / GPP_I10

This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

GPP_F23

This signal has a weak internal pull-down.
0 = Port F is not detected. (Default)
1 = Port F is detected.

MICRO-STAR INT'L CO.,LTD.

Title: PCH-1(CLK/DDI)

Size | Document Number: MS-17F6 | Rev: 10

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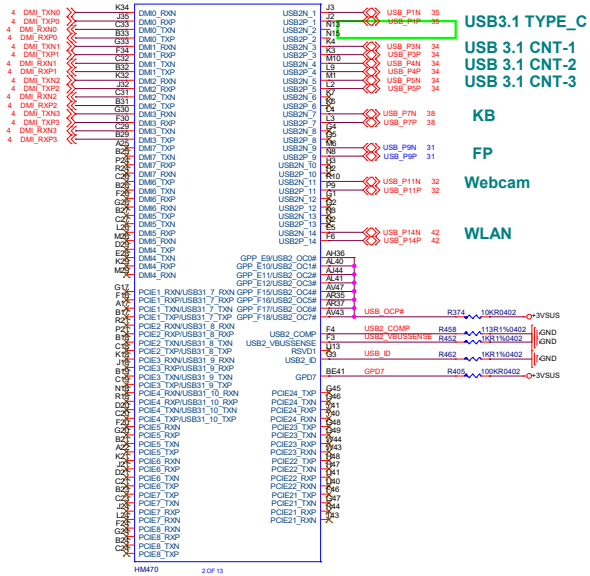
HM370 (DMI/PCIE/USB3.1/USB2.0/CNVi)

	GPP_K10
N18P_GPU	PULL HIGH
GN20_GPU	PULL LOW



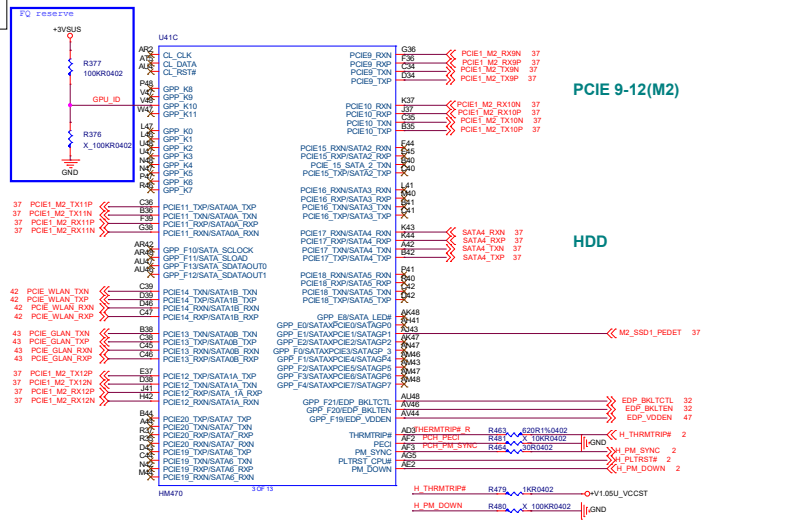
USB			
USB 2.0	USB 3.1	Device	Note
1	1	USB TYPE_C-1	
2	3	USB TYPE_C-2	
3	3	USB TYPE_A-1	
4	4	USB TYPE_A-2	
5	5	USB TYPE_A-3	
6			
7			
8			
9			
10			
11		WebCam	
12			
13			
14		WLAN	

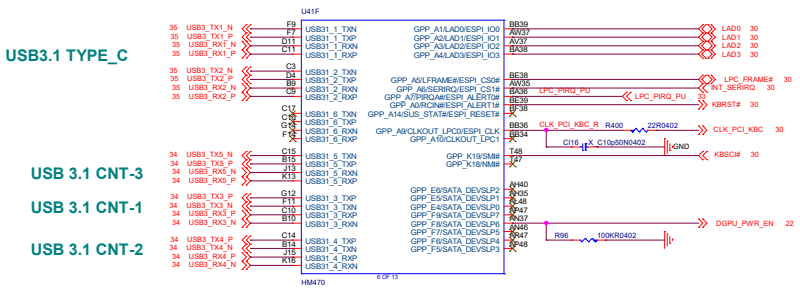
GPD7

External pull-up is required. Recommend 100K.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

High Speed I/O Ports			
	HM370		Device
1	USB3.1 Gen 1		NC
2	USB3.1 Gen 1		NC
3	N/A		NC
4	N/A		NC
5	INTEL LAN Only		NC
6	N/A		NC
7	N/A		NC
8	N/A		NC
9	PCIE/LAN	PICE Configurable M.2	M.2 SSD-1
10	PCIE		
11	PCIE/SATA0A		
12	PCIE/LAN/SATA1A		
13	PCIE/LAN/SATA0B		LAN
14	PCIE/SATA1B		WLAN
15	PCIE		NC
16	PCIE		NC
17	PCIE/SATA4		HDD
18	PCIE/SATA5		NC
19	PCIE		NC
20	PCIE		NC
21	PCIE		
22	PCIE		NC
23	PCIE		
24	PCIE		

SATA Lane 0 has the flexibility to be mapped to PCIE 11 or 13
SATA Lane 1 has the flexibility to be mapped to PCIE 12 or 14





GPP_A6

PCI Interrupt Request Ax
Note: An external Pull-up is required

GPP_A7

PCI Interrupt Request Ax
Note: An external Pull-up is required

GPP_A14

LPC Mode - Suspend Status:
This signal is asserted by the PCH to indicate that the system will be entering a low power state soon.

GPP_J4 / CNV_BRI_DT

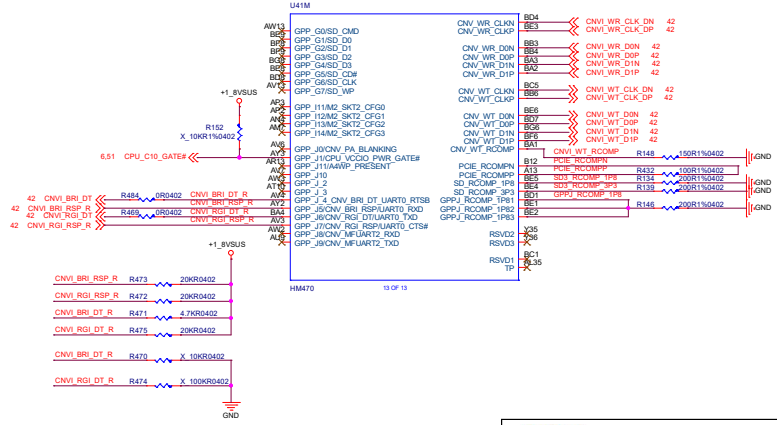
This signal has a weak internal pull-down.
An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.
0 = 38.4 XTAL frequency selected. (Default)
1 = 24MHz XTAL frequency selected.

GPP_J6 / CNV_RGI_DT

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

GPP_J9

The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail



MICRO-STAR INT'L CO.,LTD.			
Title: PCH-2(DMI/PCIE/USB/SATA)			
Size:	Document Number: MS-17F6		Rev: 10
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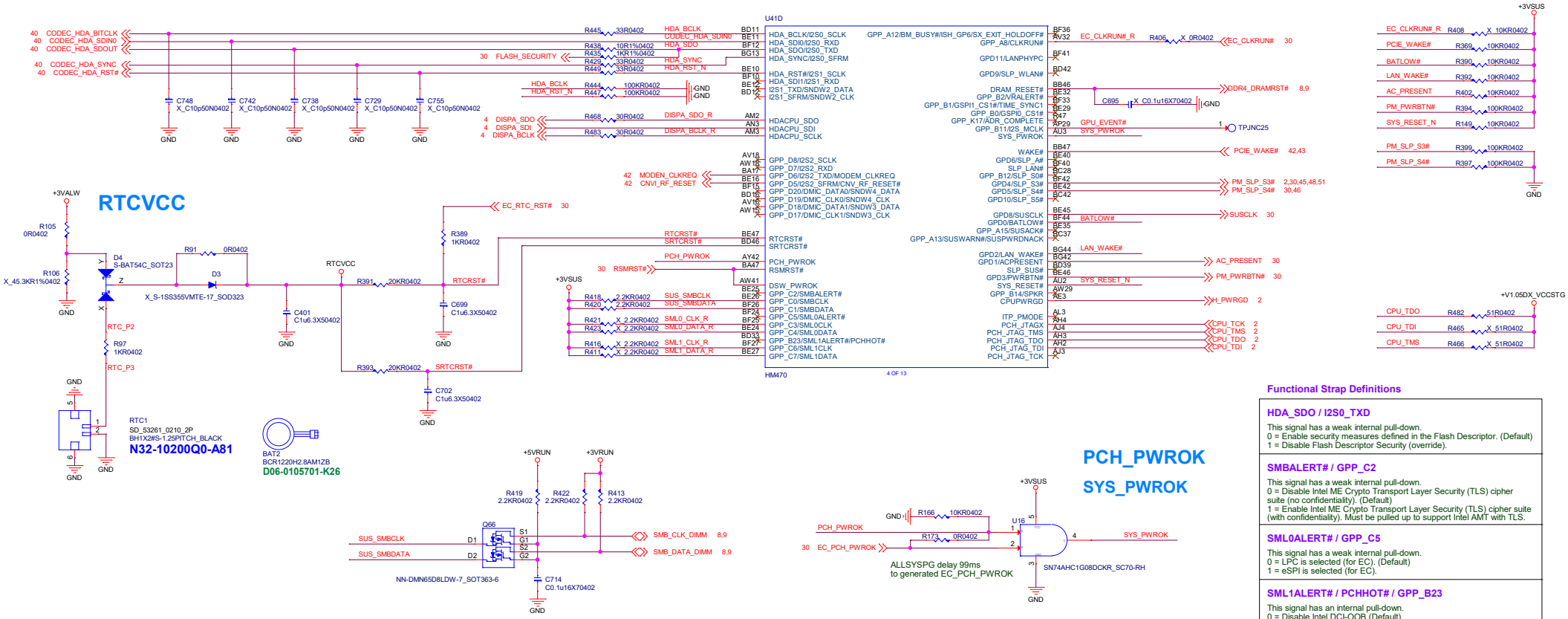
RTCVCC
+3VALW
+3VSUS
+5VRUN
+3VRUN
U41D
HM470
4 OF 13
RTC1
SD_53261_0210_2P
BH1X2#S-1.25PITCH_BLACK
N32-10200Q0-A81
BAT2
BCR1220H2.8AM1ZB
D06-0105701-K26
X_S-1SS355VMTE-17_SOD323
S-BAT54C_SOT23
NN-DMN65D8LDW-7_SOT363-6
SN74AHC1G08DCKR_SC70-RH
ALLSYSPG delay 99ms
to generated EC_PCH_PWROK
PCH_PWROK
SYS_PWROK
Functional Strap Definitions
HDA_SDO / I2S0_TXD
This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override).
SMBALERT# / GPP_C2
This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.
SML0ALERT# / GPP_C5
This signal has a weak internal pull-down.
0 = LPC is selected (for EC). (Default)
1 = eSPI is selected (for EC).
SML1ALERT# / PCHHOT# / GPP_B23
This signal has an internal pull-down.
0 = Disable Intel DCI-OOB (Default)
1 = Enable Intel DCI-OOB
SPKR / GPP_B14
The signal has a weak internal pull-down.
0 = Disable Top Swap mode. (Default)
1 = Enable Top Swap mode.
DG/ RTC Well Input Strap
RSMRST# & DSW_PWROK, PCH_PWROK : PD
RTCRST#, SRTCRST#, INTRUDER# : PU
MICRO-STAR INT'L CO.,LTD.
PCH-3(HDA/RTC/SMBUS)
Size: Custom
Document Number: MS-17F6
Rev: 10
Date: Friday, December 25, 2020
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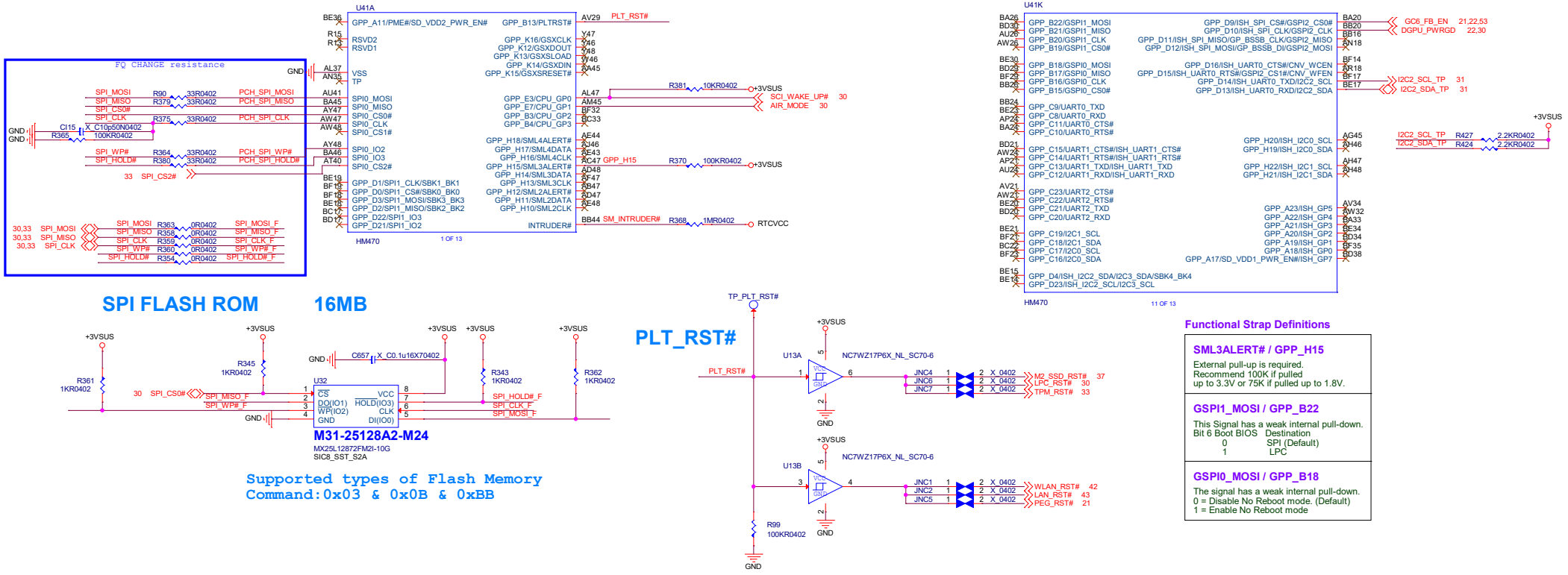
HM370 (UART/I2C/SPI)



SPI FLASH ROM 16MB

Supported types of Flash Memory
Command:0x03 & 0x0B & 0xBB

PLT_RST#

Functional Strap Definitions

SML3ALERT# / GPP_H15

External pull-up is required.
Recommend 100K if pulled
up to 3.3V or 75K if pulled up to 1.8V.

GSPI1_MOSI / GPP_B22

This Signal has a weak internal pull-down.

Bit 6 Boot BIOS	Destination
0	SPI (Default)
1	LPC

GSPI0_MOSI / GPP_B18

The signal has a weak internal pull-down.
0 = Disable No Reboot mode. (Default)
1 = Enable No Reboot mode

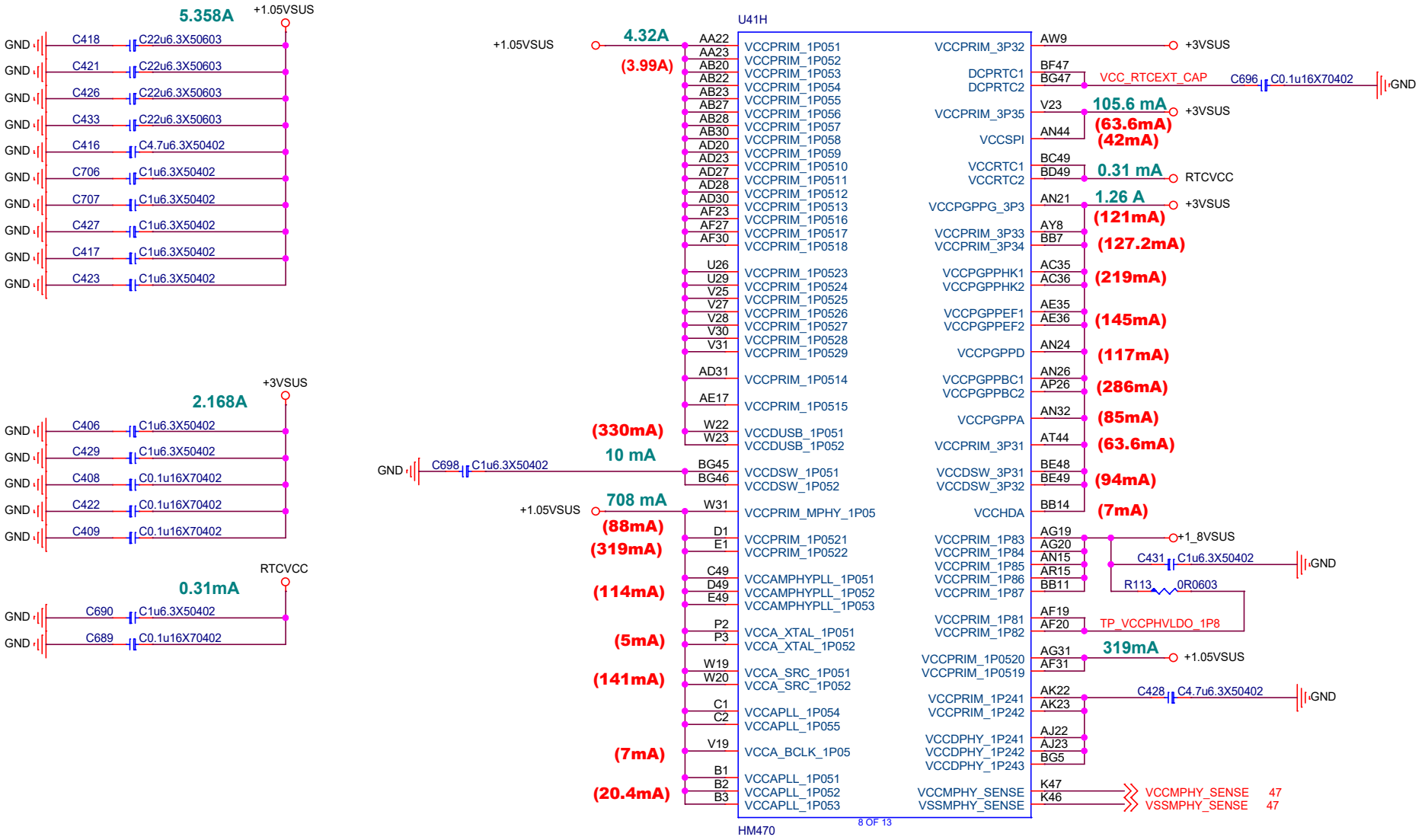
MICRO-STAR INT'L CO.,LTD.

Title: PCH-4(SPI/GPIO)

Size: | Document Number: MS-17F6 | Rev: 10

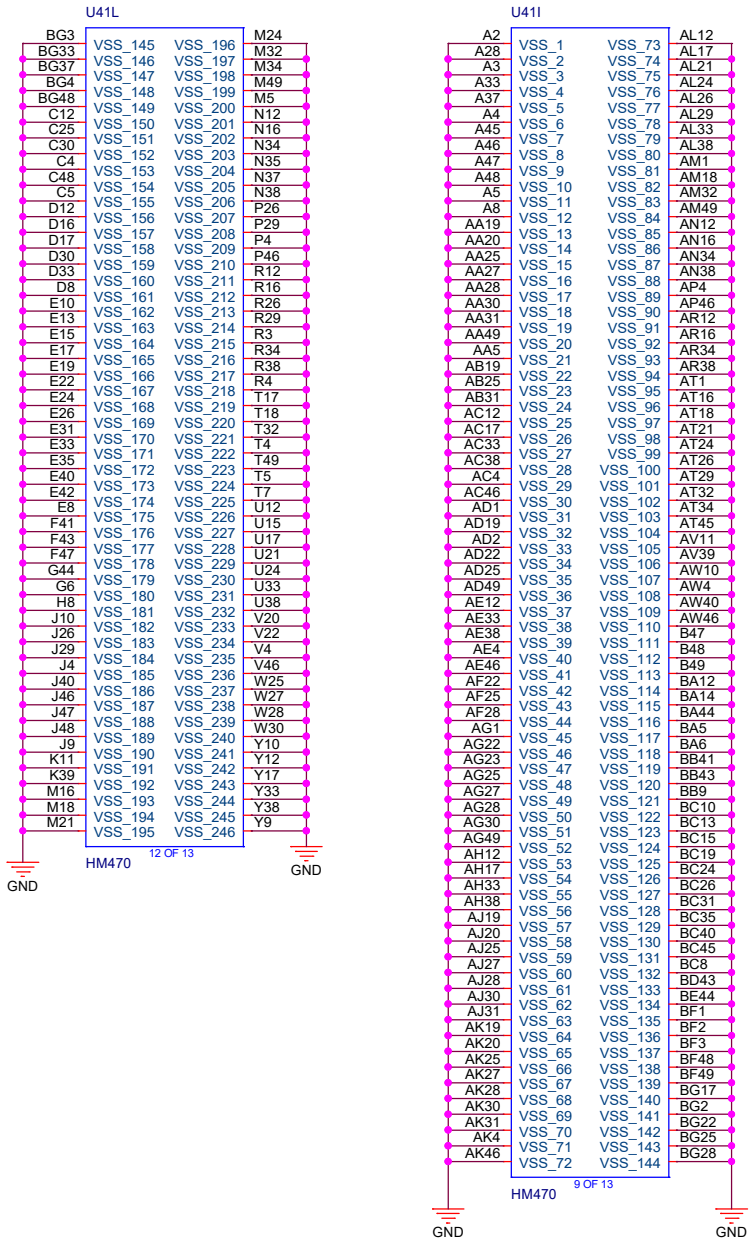
Date: Friday, December 25, 2020 Sheet 27 of 61

HM370 (Power)



MICRO-STAR INT'L CO.,LTD.			
Title: PCH-5(Power)			
Size: Custom	Document Number: MS-17F6		Rev: 10
Date: Friday, December 25, 2020		Sheet 28 of 61	

PCH-H(GND)



MICRO-STAR INT'L CO.,LTD.		
Title: PCH-6(GND)		
Size: Custom	Document Number: MS-17F6	Rev: 10
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KBC/EC/uP (ENE9028)

Hardware Reset

CN2
SWTA_S6_5_2X6_3_T
SW-TACTB1S
N71-0101630-D02

ESD-SFI0402-050E101NP

U15

LPC I/F
FAN&PWM
IKB
ESB
CIR
SPI FLASH
PS2 I/F
UART
POWER/GROUND
SMBUS
AD/DA
SDI
LED

KB9028Q-C

ALLSYSPG

Keyboard LED CONN

LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

FPC1
N5A-12F0190-A81
FPC_S12_1
FPC12P-T-0.5PITCH_WHITE

Pull Up/Pull Down

MB_ID

FQ ADD MB_ID_2

MB_ID_2	MB_ID_1	MB version
0	0	0A
0	1	1.0

For EMI

ESD-AOZ8829DI-03

CON1
N5A-26F0270-A81
FPC_26_C1470903
FPC26P-T-1PITCH_WHITE

MICRO-STAR INT'L CO.,LTD.	
Title:	EC(ENE9028)
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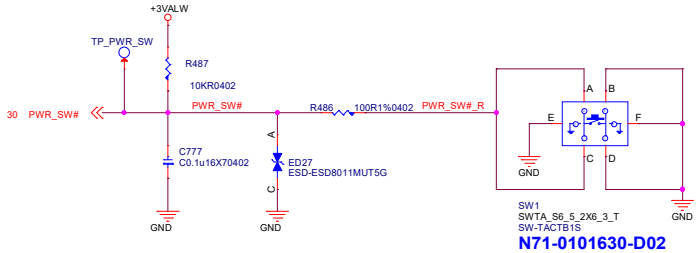
Power Switch /Touch Pad / LED

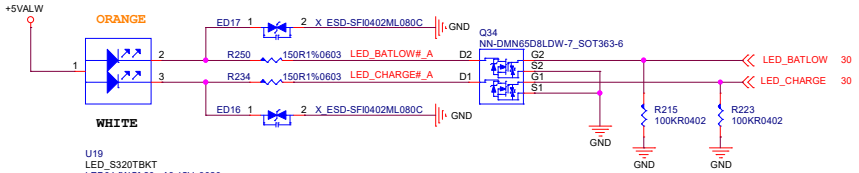
Bobchang 20180702

Power Switch



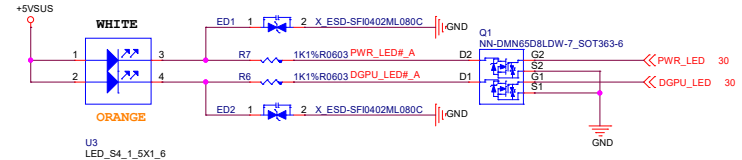
N71-0101630-D02

LED



U19
LED_S320TBKT
LED04-[WO]-20mA3.15V_3020

D0C-040M700-L05

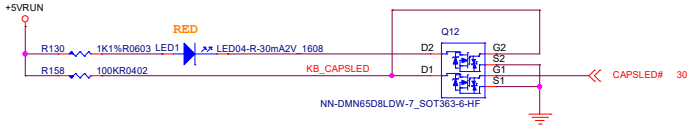


U3
LED_S4_1_5X1_6
LED04-WO-20mA3.15V30mA2.4V_1516

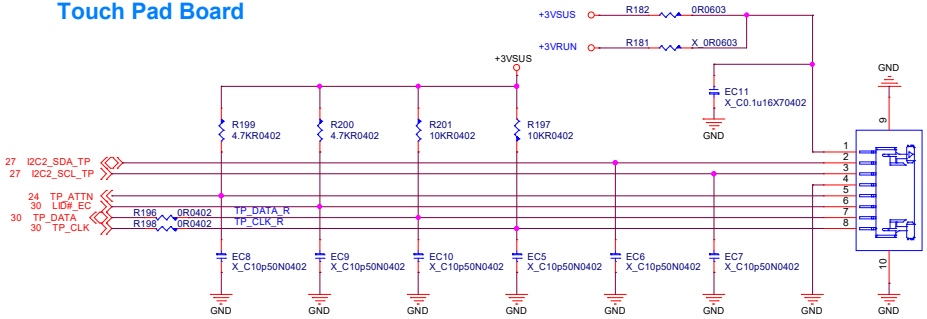
D0C-040H800-L05

17F1 LED2

CAPSLED

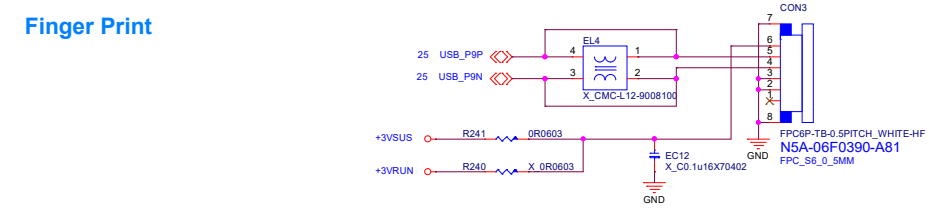


Touch Pad Board



N5A-08F0170-A81

Finger Print



MICRO-STAR INT'L CO.,LTD.

Title: Power Switch/FAN/Touch Pad/LED

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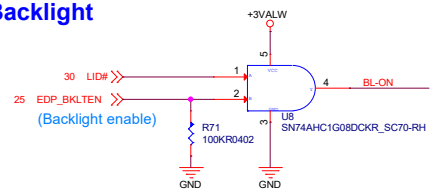
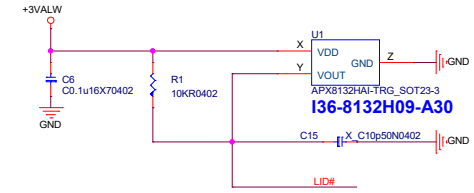
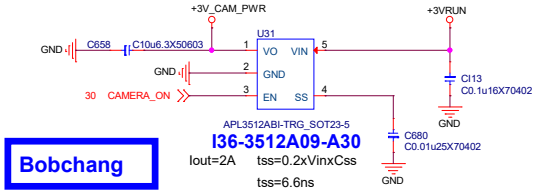
Backlight



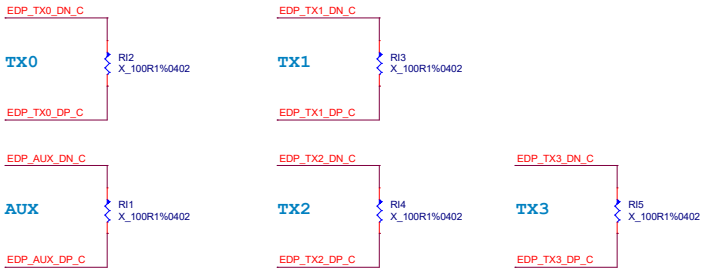
Hall Switch



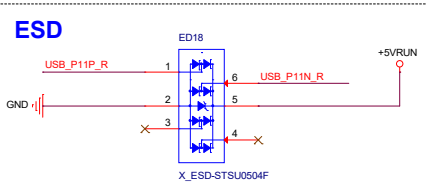
CAMERA Power



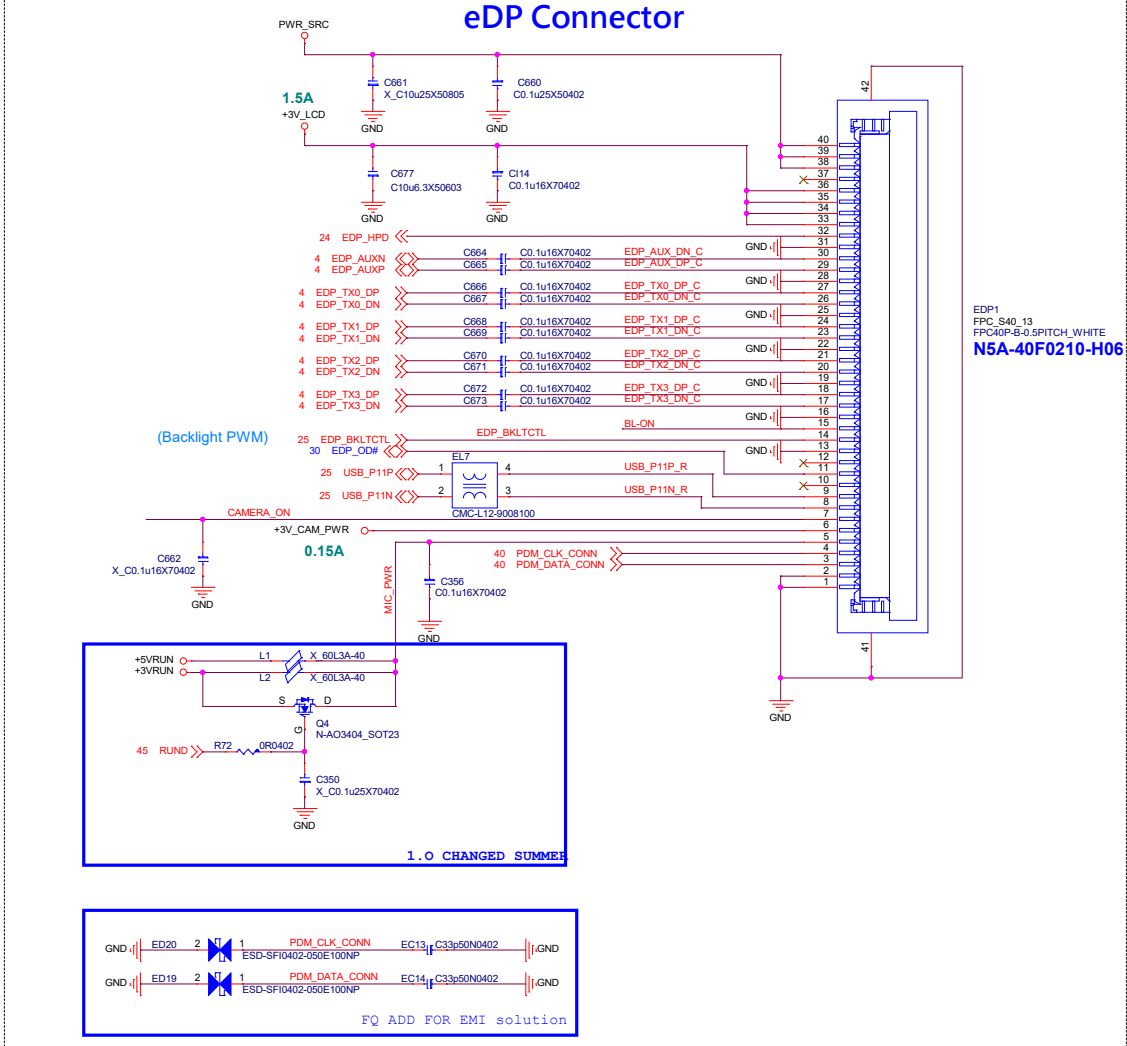
EMI Close Connector



ESD



eDP Connector



MICRO-STAR INT'L CO.,LTD.		
Title: eDP Connector/Camera/LID		
Size: Custom	Document Number: MS-17F6	Rev: 10
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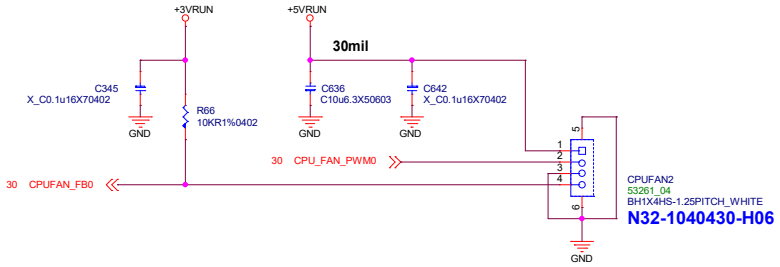
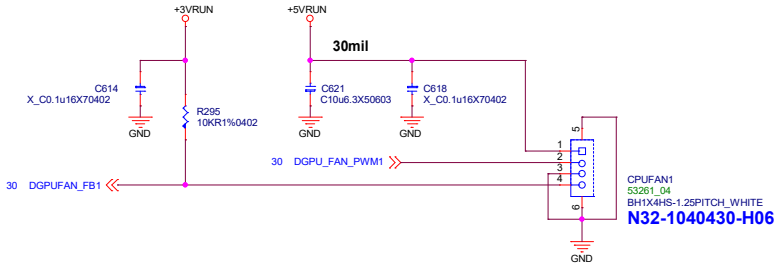
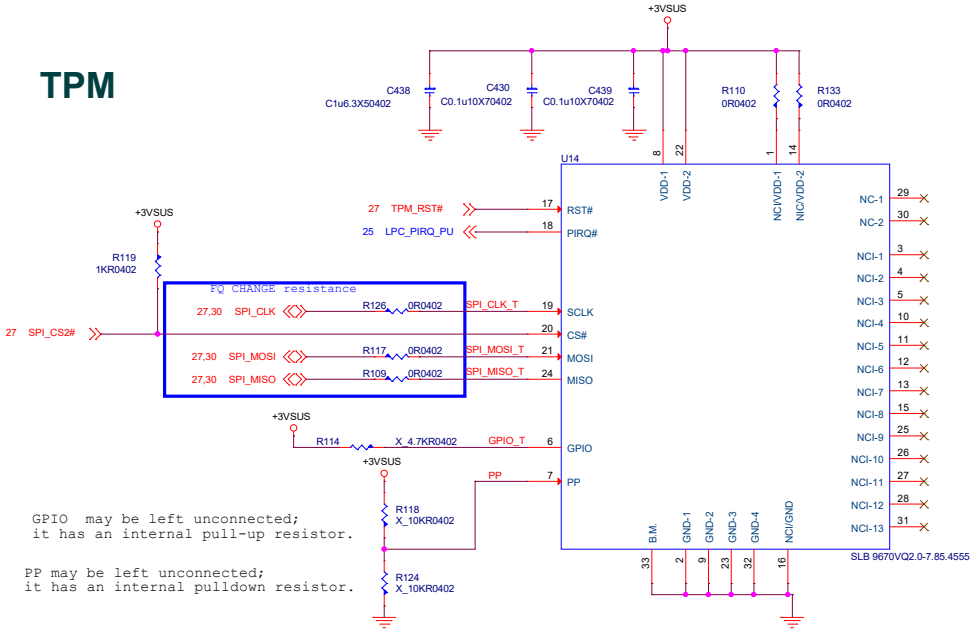
CPU FAN



DGPU FAN



TPM



MICRO-STAR INT'L CO.,LTD.

Title: FAN

Size: Custom | Document Number: MS-17F6 | Rev: 10

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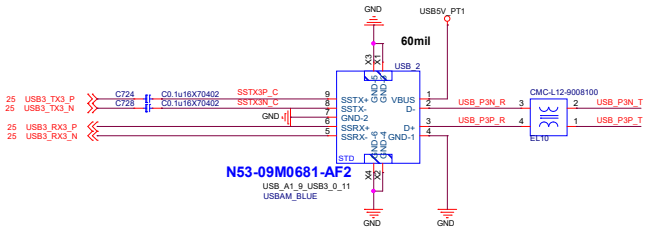
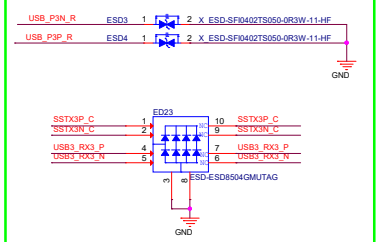
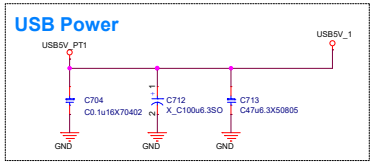
USB3.0 CNT-1

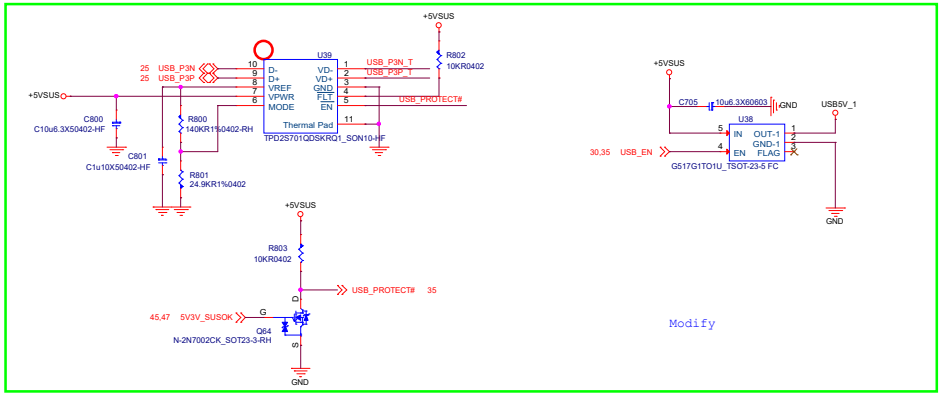


ESD

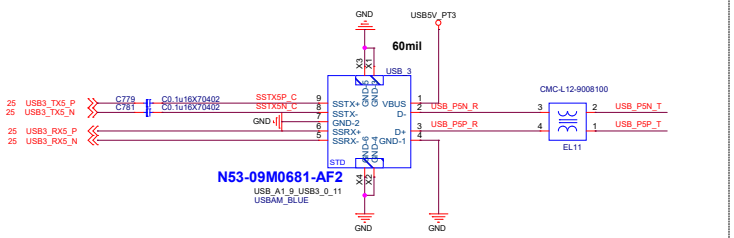


USB Power

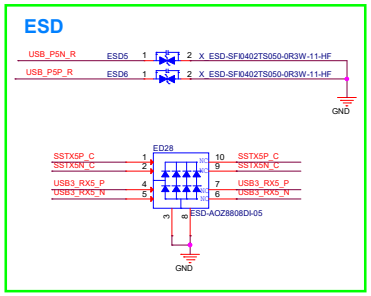




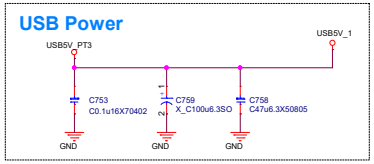
USB3.0 CNT-2

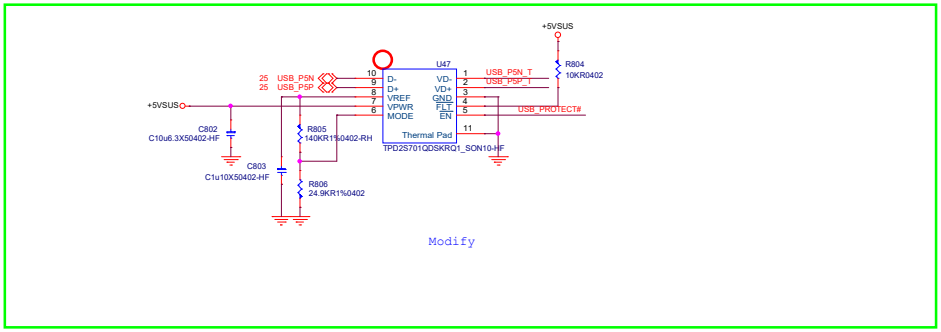


ESD

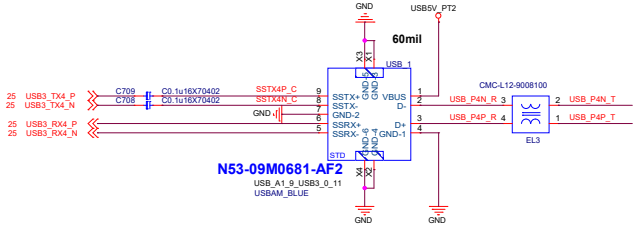


USB Power

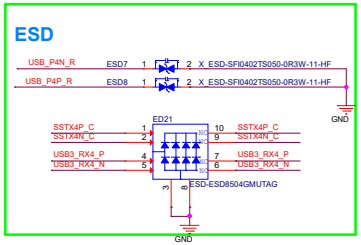




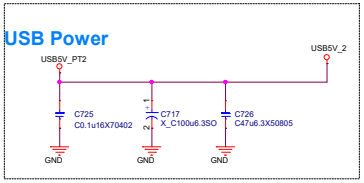
USB3.0 CNT-3

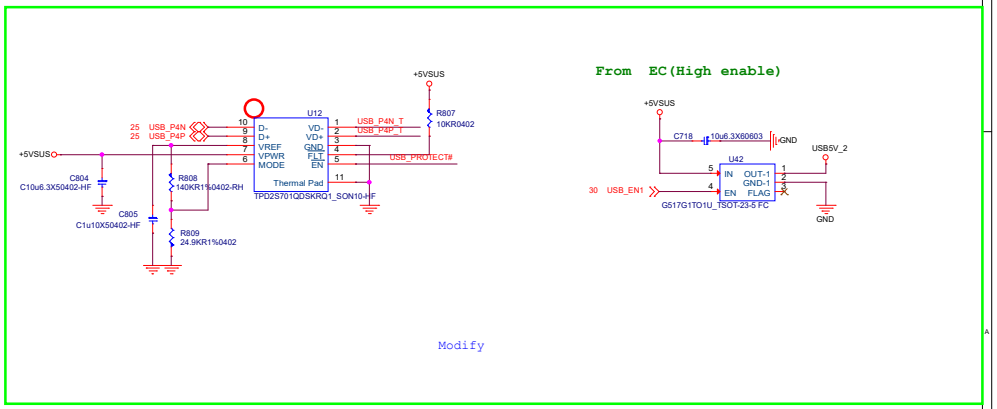


ESD



USB Power





MICRO-STAR INT'L CO.,LTD.

Title: USB 3.0 TYPE_A

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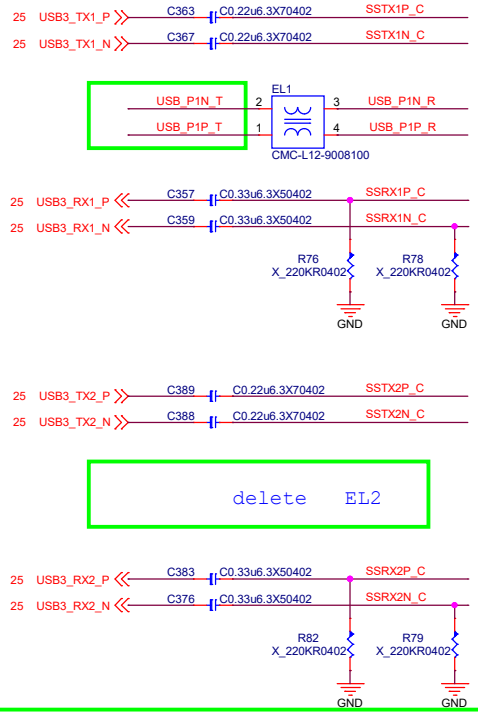
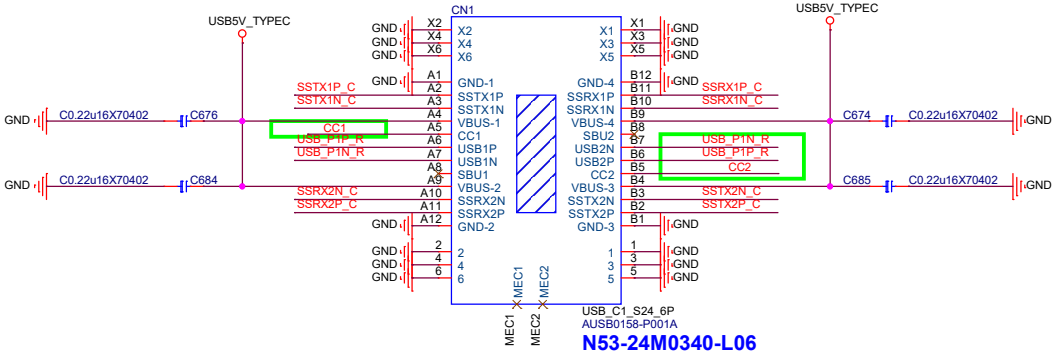
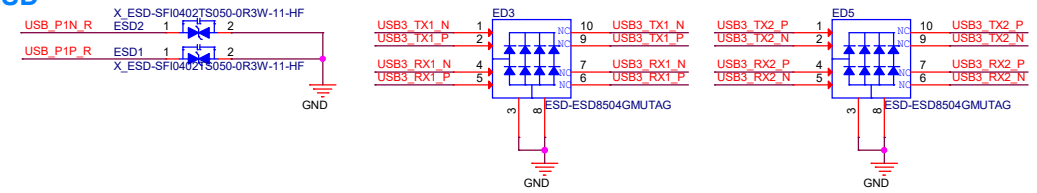
USB 3.0 TYPE_C

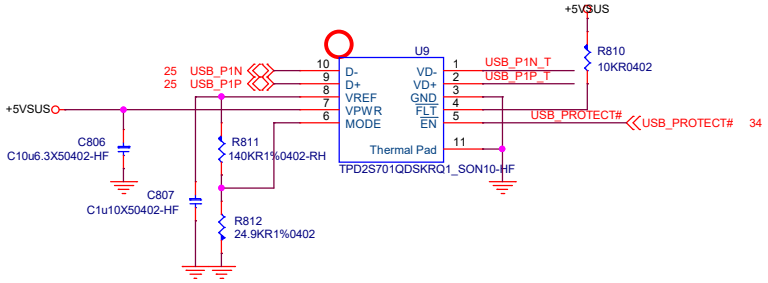


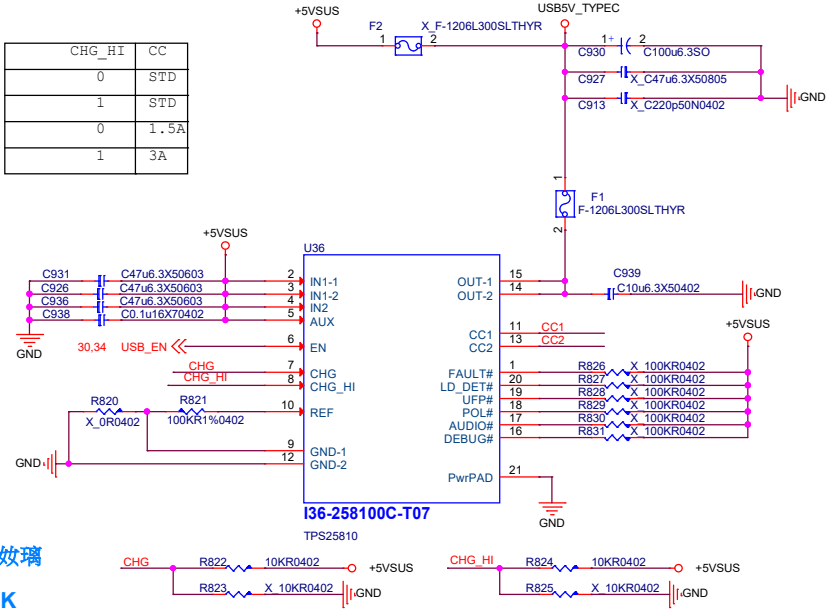


ESD



CHG_HI	CC
0	STD
1	STD
0	1.5A
1	3A





Modify

悟隱OR to GND 祥效璃
TI New datasheet
Pin9 Pin10蟈諉100K

msi	MICRO-STAR INT'L CO.,LTD.	
Title	USB 3.0 TYPE_C	
Size: Custom	Document Number: MS-17F6	Rev: 10
Date: Friday, December 25, 2020	Sheet 35 of 61	

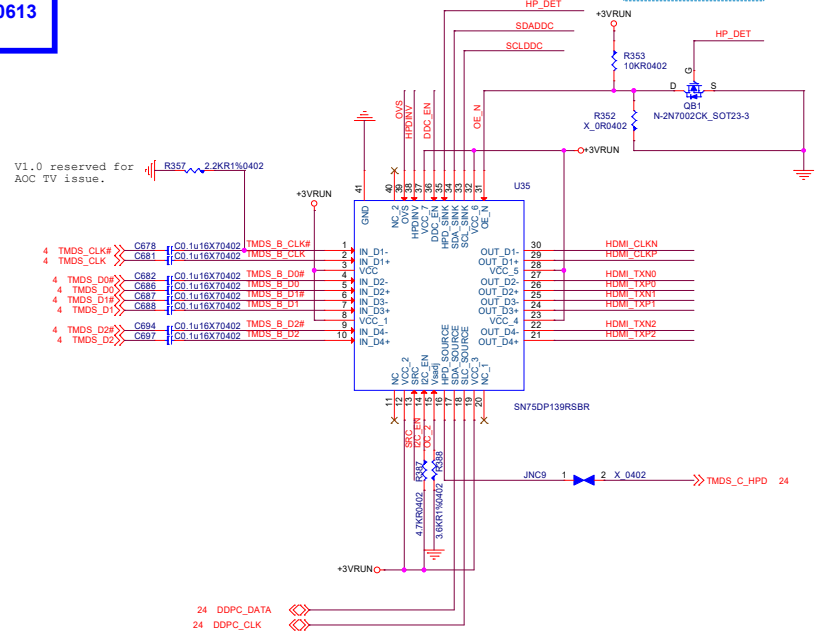
HDMI Level Shifter

Bobchang 20180613

HP_DET
PLUGGED 5V
UNPLUGGED 0V

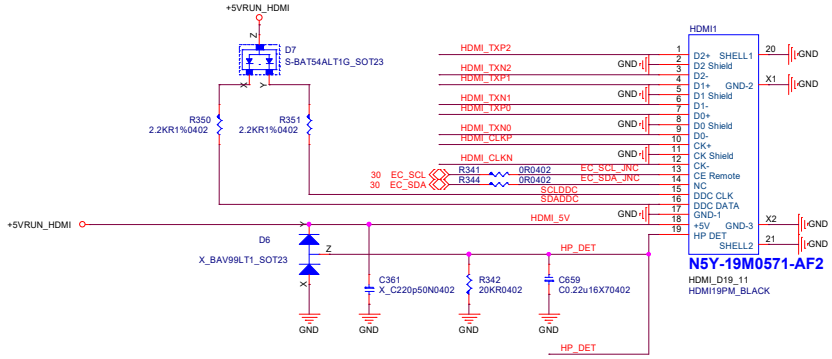
HPD_SNK Internal PD 130kohm

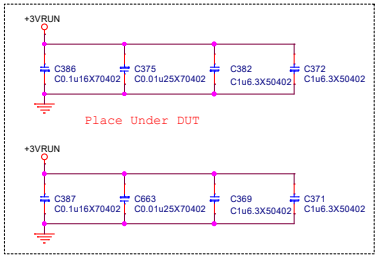
ESD 10KV



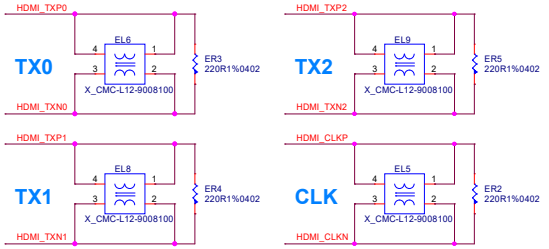
FQ REMOVE DGPU HDMI CLK/DATA levelshift

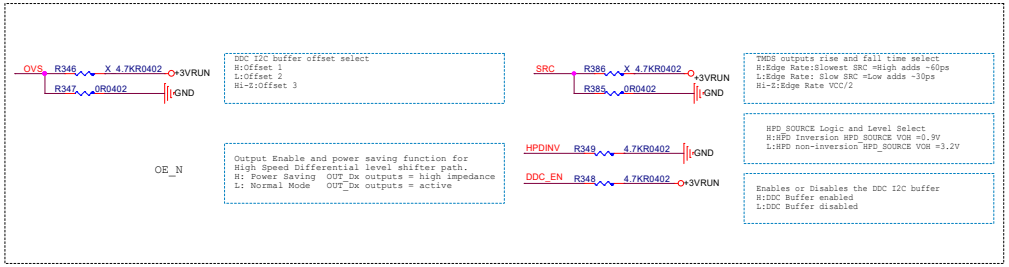
HDMI connector





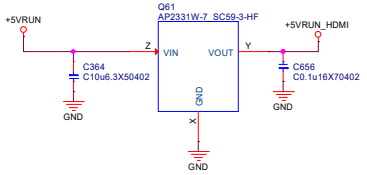
EMI Close Connector



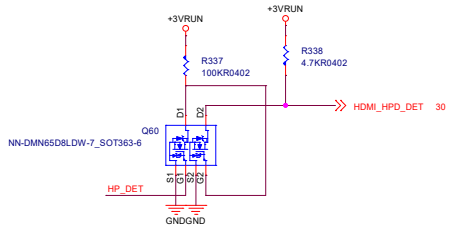


Avoid HDMI Leakage

W>20mils



HPD Level Shift 5V to 3V for Debug Card



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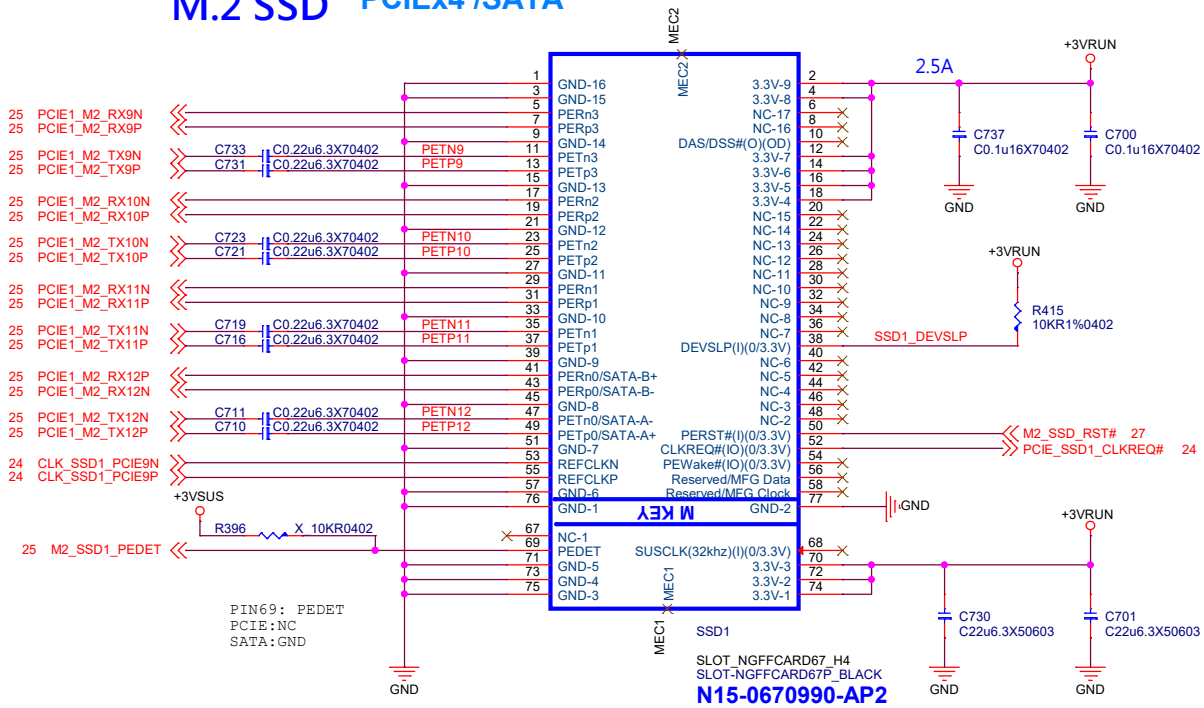
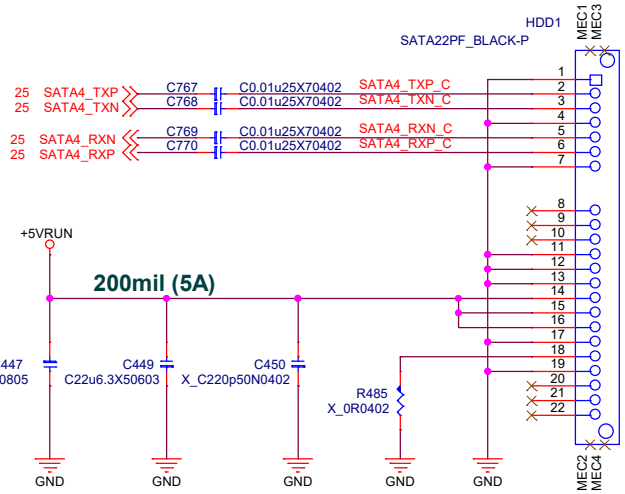
MICRO-STAR INT'L CO.,LTD.

M.2 SSD PCIEx4 /SATA



HDD



MICRO-STAR INT'L CO.,LTD.

Title: M.2 SSD/HDD

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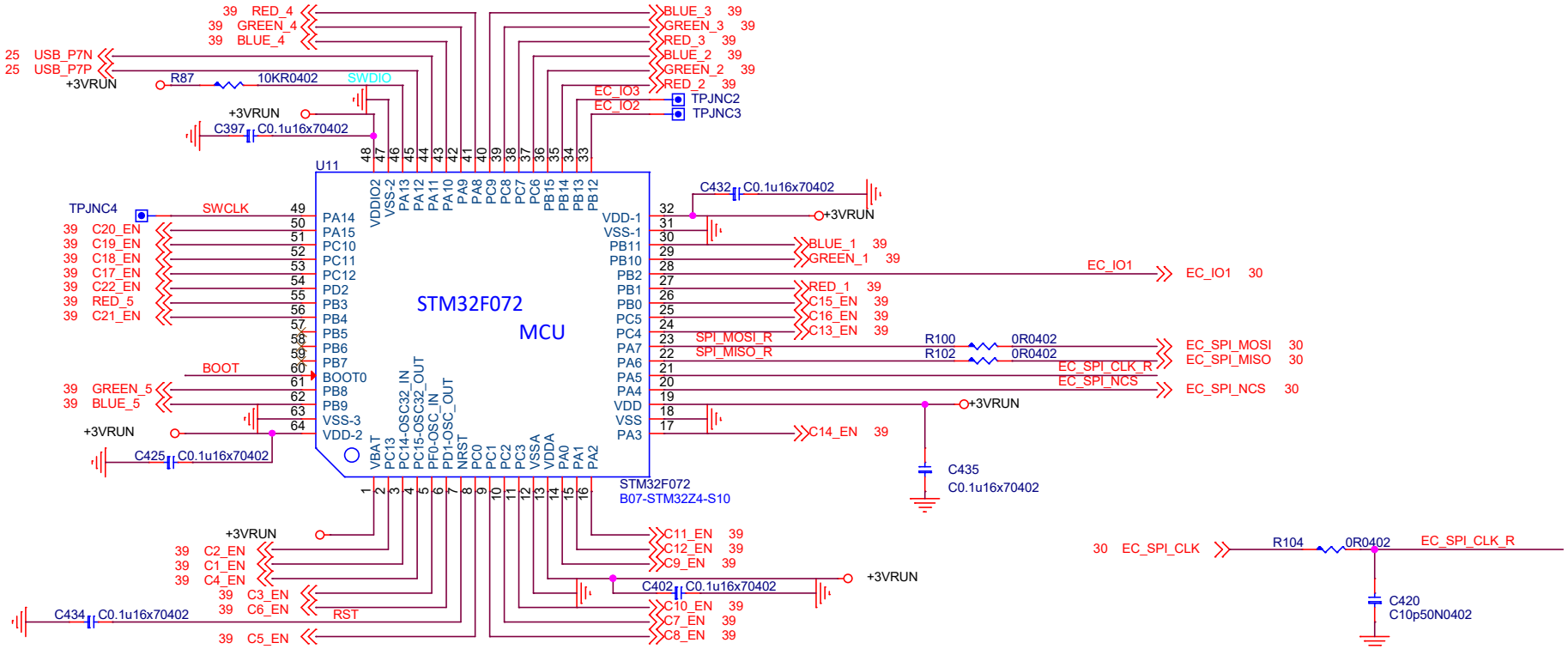
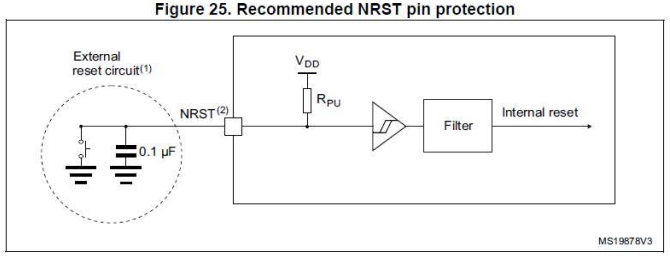


Figure 25. Recommended NRST pin protection



1. The external capacitor protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 56: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.

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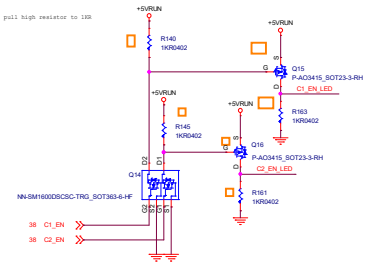
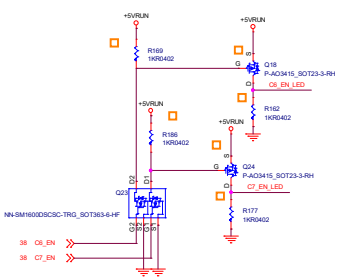
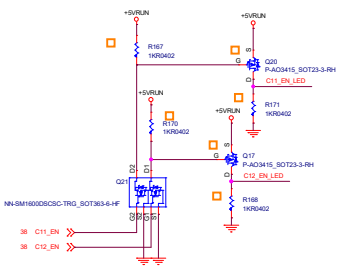
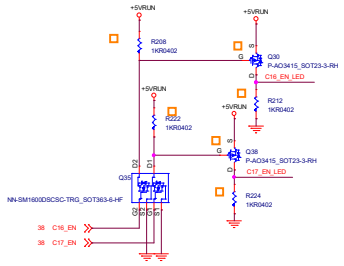
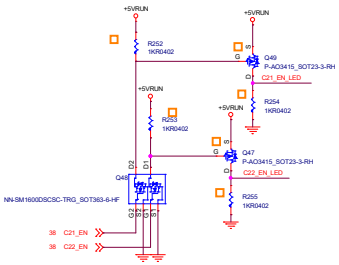
2016/12/01 modify all pull high resistor to 1KR

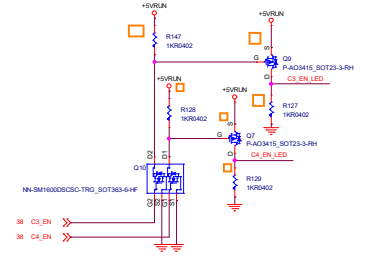


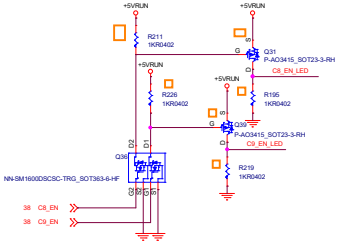


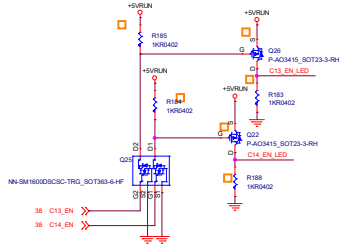


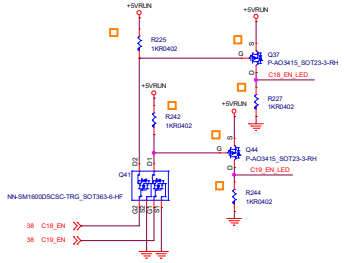










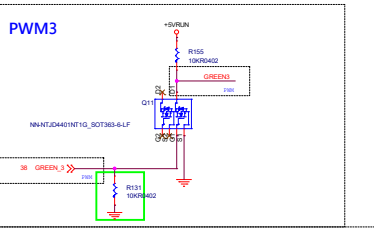


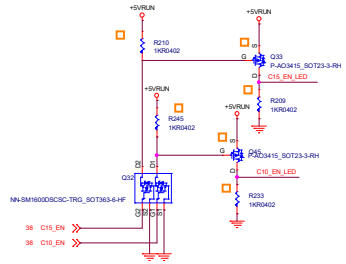
Modify R10,R11,R12,R13,R14,R19,R20,R22,R23, R24,R30,R31,R32,R33,R40,R41,R42,R43, R50,R51,R52,R56 3R to 1R

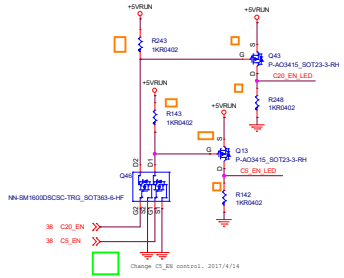
Modify R15,R16,R17,R18,R21,R25,R26,R27,R28, R29,R35,R36,R37,R38,R45,R46,R47,R48,R54, R55,R57,R59 3R to 1K

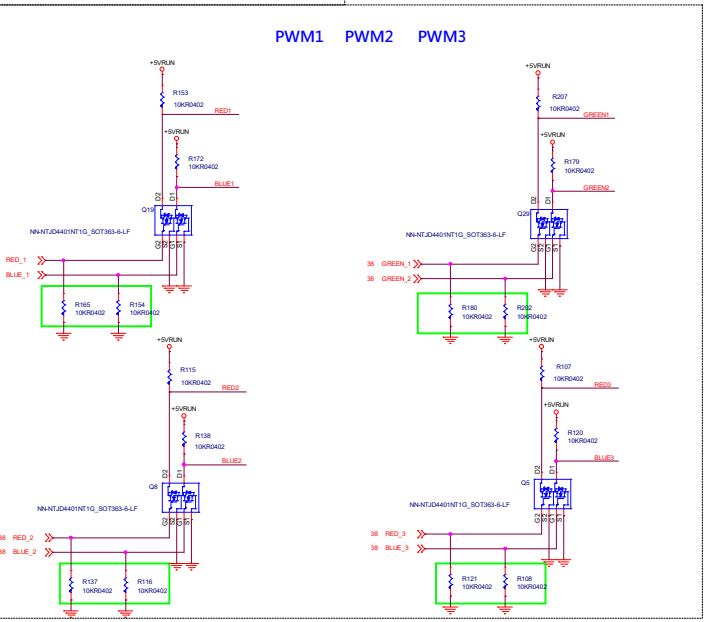
modify Q1,Q11,Q16,Q17,Q18,Q19,Q2,Q21,Q22,Q23, Q24,Q3,Q31,Q32,Q33,Q35,Q4,Q5,Q6,Q7,Q8,Q9 AO3078 to AO3415

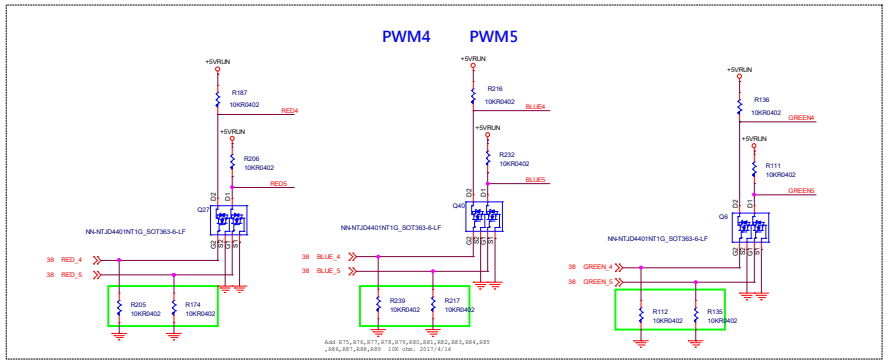
2017/04/19

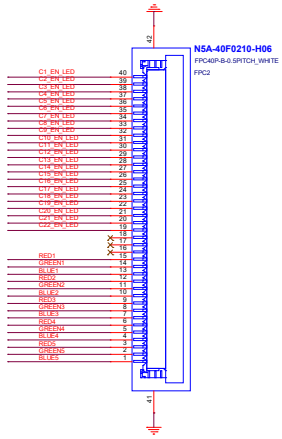












msi	MICRO-STAR INT'L CO.,LTD.	
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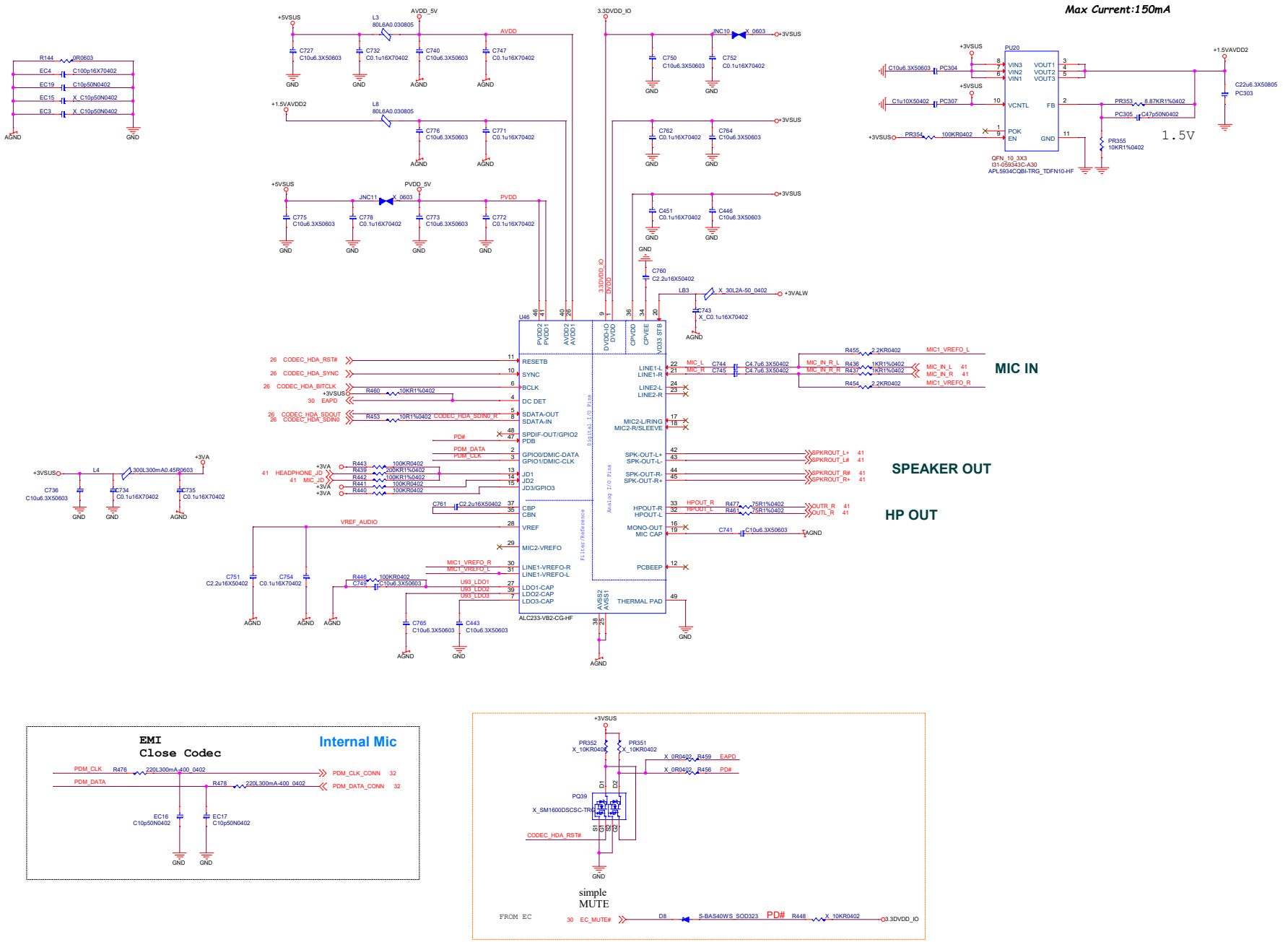
FOR ALC233-VB
have internal LDO



21K38jW2e

MICRO-STAR INT'L CO.,LTD.

Audio CODEC(ALC233)

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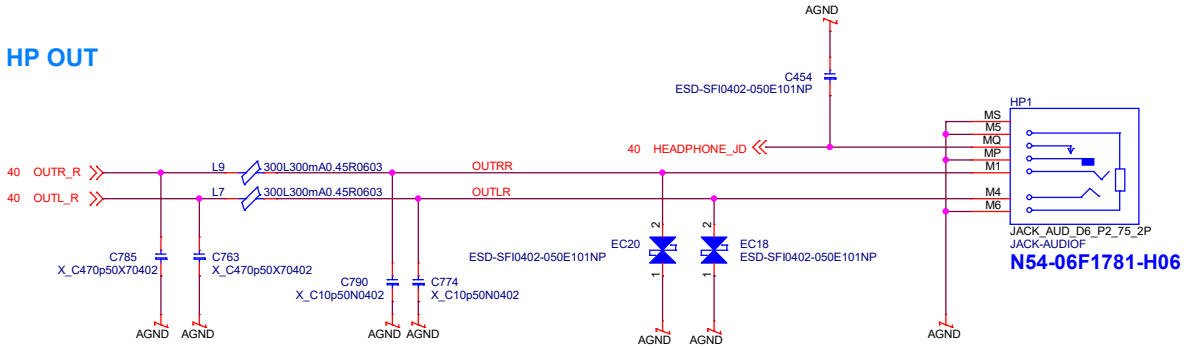
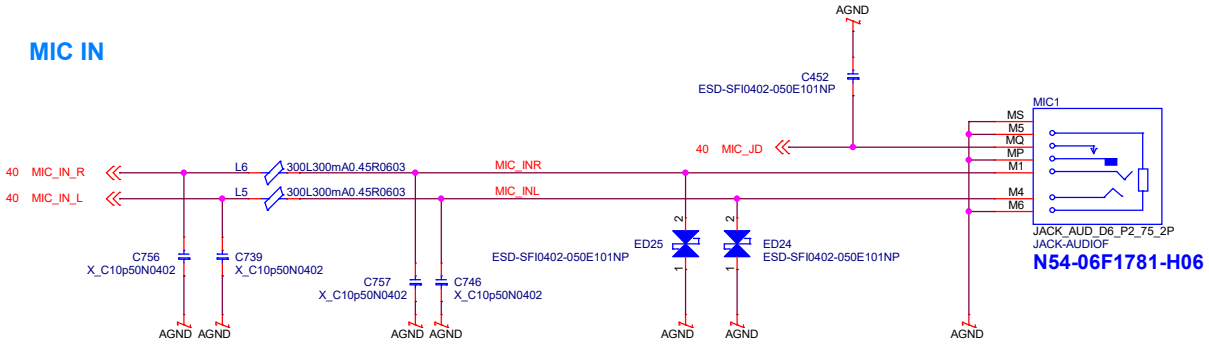
Audio CONN

HP OUT

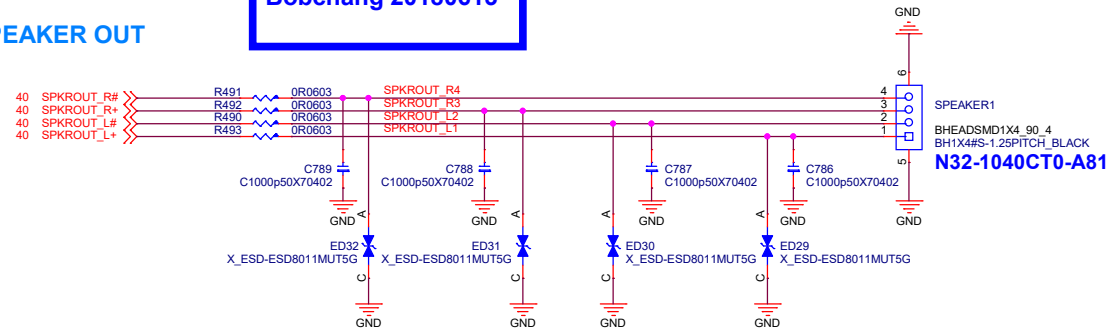


MIC IN



SPEAKER OUT

Bobchang 20180613



21K38jW2e

MICRO-STAR INT'L CO.,LTD.		
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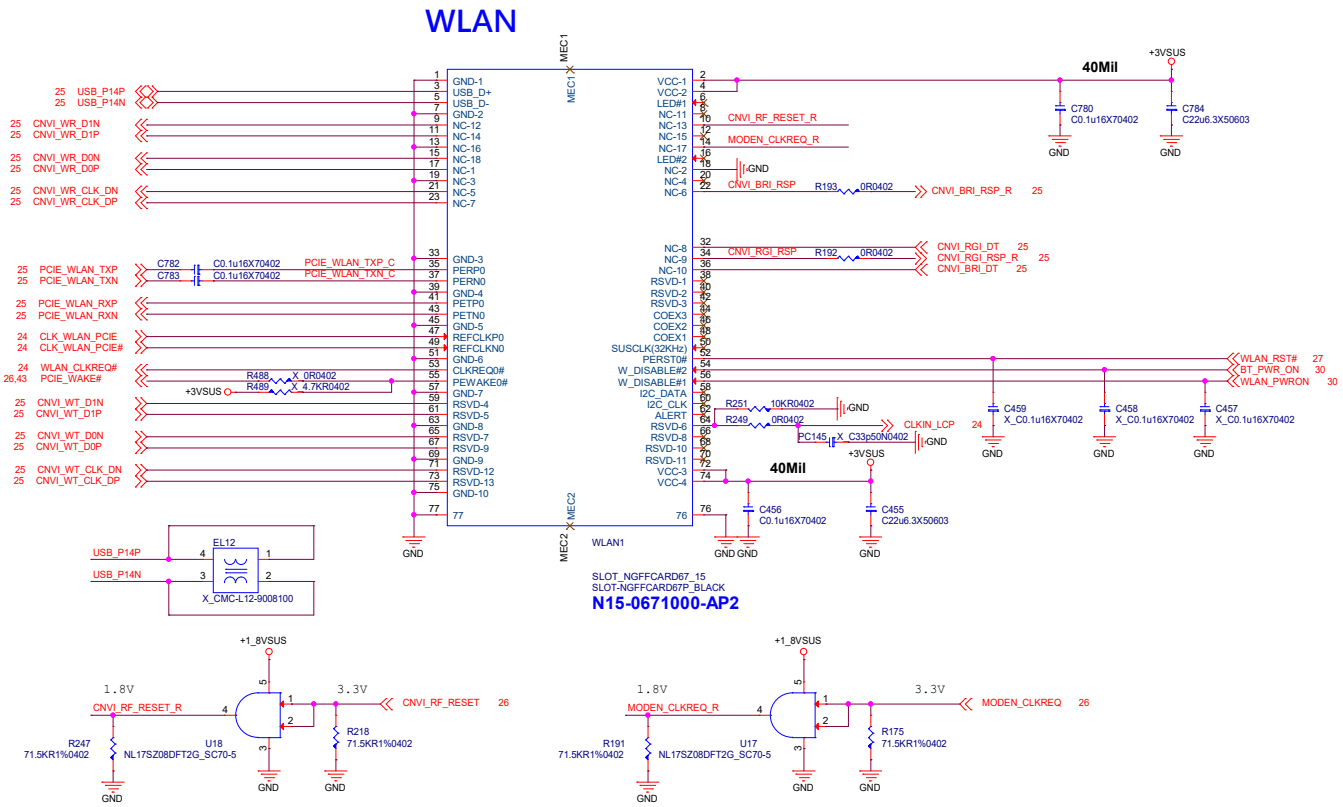

Pin #	M.2 WLAN	INTEL CNVi WLAN	Pin #	M.2 WLAN	INTEL CNVi WLAN
Pin 1	GND	GND	Pin 2	3.3V	3.3V
Pin 3	USB_D+	N/C	Pin 4	3.3V	3.3V
Pin 5	USB_D-	N/C	Pin 6	LED1#	LED1#
Pin 7	GND	GND	Pin 8	Module Key	N/C
Pin 9	Module Key	WGR_D1N	Pin 10	Module Key	RF_RESET_B(1.8V)
Pin 11	Module Key	WGR_D1P	Pin 12	Module Key	N/C
Pin 13	Module Key	GND	Pin 14	Module Key	CLKREQ0(1.8V)
Pin 15	Module Key	WGR_D0N	Pin 16	LED2#	LED2#
Pin 17	N/C	WGR_D0P	Pin 18	GND	GND
Pin 19	N/C	GND	Pin 20	N/C	N/C
Pin 21	N/C	WGR_CLKN	Pin 22	N/C	BRI_RSP(1.8V)
Pin 23	N/C	WGR_CLKP	Pin 24	Module Key	Module Key
Pin 25	Module Key	Module Key	Pin 26	Module Key	Module Key
Pin 27	Module Key	Module Key	Pin 28	Module Key	Module Key
Pin 29	Module Key	Module Key	Pin 30	Module Key	Module Key
Pin 31	Module Key	Module Key	Pin 32	N/C	RGI_DT(1.8V)
Pin 33	GND	GND	Pin 34	N/C	RGI_RSP(1.8V)
Pin 35	PERP0	N/C	Pin 36	N/C	BGI_DT(1.8V)
Pin 37	PERN0	N/C	Pin 38	N/C	N/C
Pin 39	GND	GND	Pin 40	N/C	N/C
Pin 41	PETP0	N/C	Pin 42	N/C	N/C
Pin 43	PETN0	N/C	Pin 44	N/C	N/C
Pin 45	GND	GND	Pin 46	N/C	N/C
Pin 47	REFCLKP0	N/C	Pin 48	N/C	N/C
Pin 49	REFCLKN0	N/C	Pin 50	SUSCLK (32KHz)	SUSCLK (32KHz)
Pin 51	GND	GND	Pin 52	PERST0#	N/C
Pin 53	CLKREQ0#	N/C	Pin 54	BT_EN (W_DISABLE2#)	BT_EN (W_DISABLE2#)
Pin 55	PEWAKE0#	N/C	Pin 56	WLAN_EN (W_DISABLE2#)	WLAN_EN (W_DISABLE2#)
Pin 57	GND	GND	Pin 58	N/C	N/C
Pin 59	N/C	WT_D1N	Pin 60	N/C	N/C
Pin 61	N/C	WT_D1P	Pin 62	N/C	N/C
Pin 63	GND	GND	Pin 64	Resever	REFCLK0(38.4MKz)
Pin 65	N/C	WT_D0N	Pin 66	N/C	N/C
Pin 67	N/C	WT_D0P	Pin 68	N/C	N/C
Pin 69	GND	GND	Pin 70	N/C	N/C
Pin 71	N/C	WT_CLKN	Pin 72	3.3V	3.3V
Pin 73	N/C	WT_CLKP	Pin 74	3.3V	3.3V
Pin 75	GND	GND			

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MICRO-STAR INT'L CO.,LTD.

Title: WLAN

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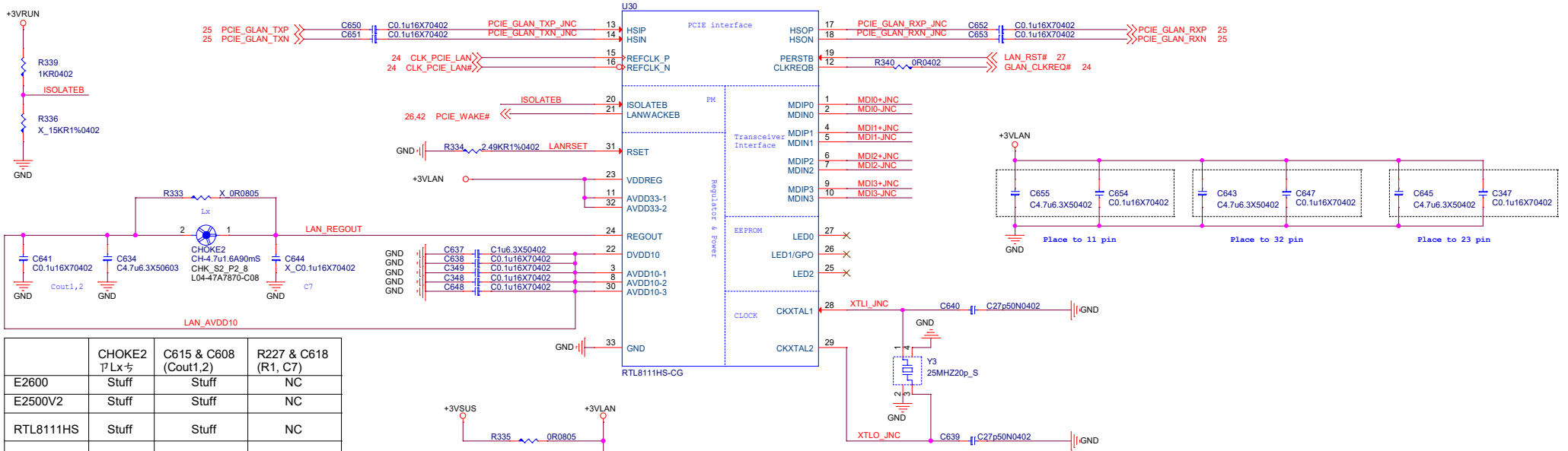
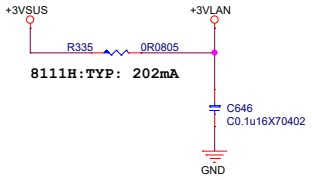
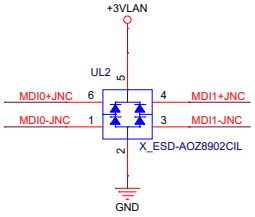
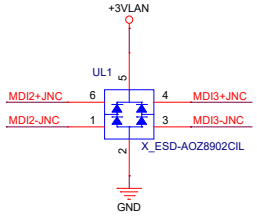
Consider VCC33 may be connected to Main Power
or chipset/BIOS's GPIO,the pull-low resistor R699
can be NC only when Main Power or chipset/BIOS's GPIO
can ensure to drive the ISOLATEB pin to a voltage
level ˜0.8V at the system state S3~S5 .
If the ISOLATEB pin can not be well-controlled to a voltage
level ˜0.8V at S3~S5 ,the pull-low resistor R699 is
needed to make sure the LAN chip is well isolated.

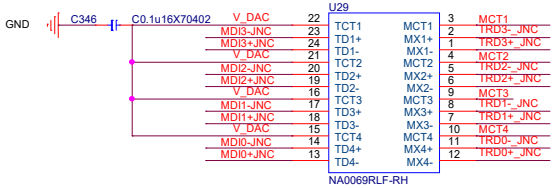


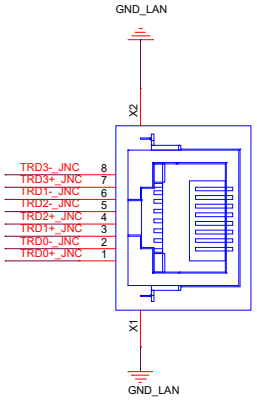
	CHOKE2 ｱLxｾ	C615 & C608 (Cout1,2)	R227 & C618 (R1, C7)
E2600	Stuff	Stuff	NC
E2500V2	Stuff	Stuff	NC
RTL8111HS	Stuff	Stuff	NC
RTL8111H	NC	NC	Stuff

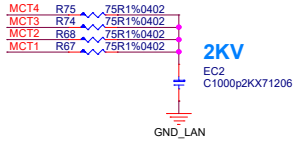


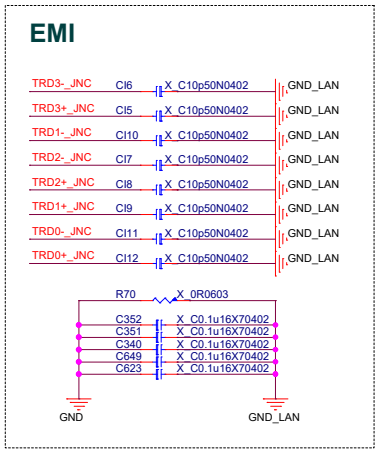












REALTEK RTL8111HS

RTL8111HS
B06-08111KC-R09
X_RTL8111HS-CG

REALTEK RTL8111H

RTL8111H
B06-08111CC-R09
X_RTL8111H-CG

Kill E2500V2

E2500V2
B06-E25002C-R54
X_E2500V2-CG

Kill E2600

E2600
B06-E26000C-R54
X_E2600-CG

MICRO-STAR INT'L CO.,LTD.

Title: GIGA_LAN(RTL8111HS)

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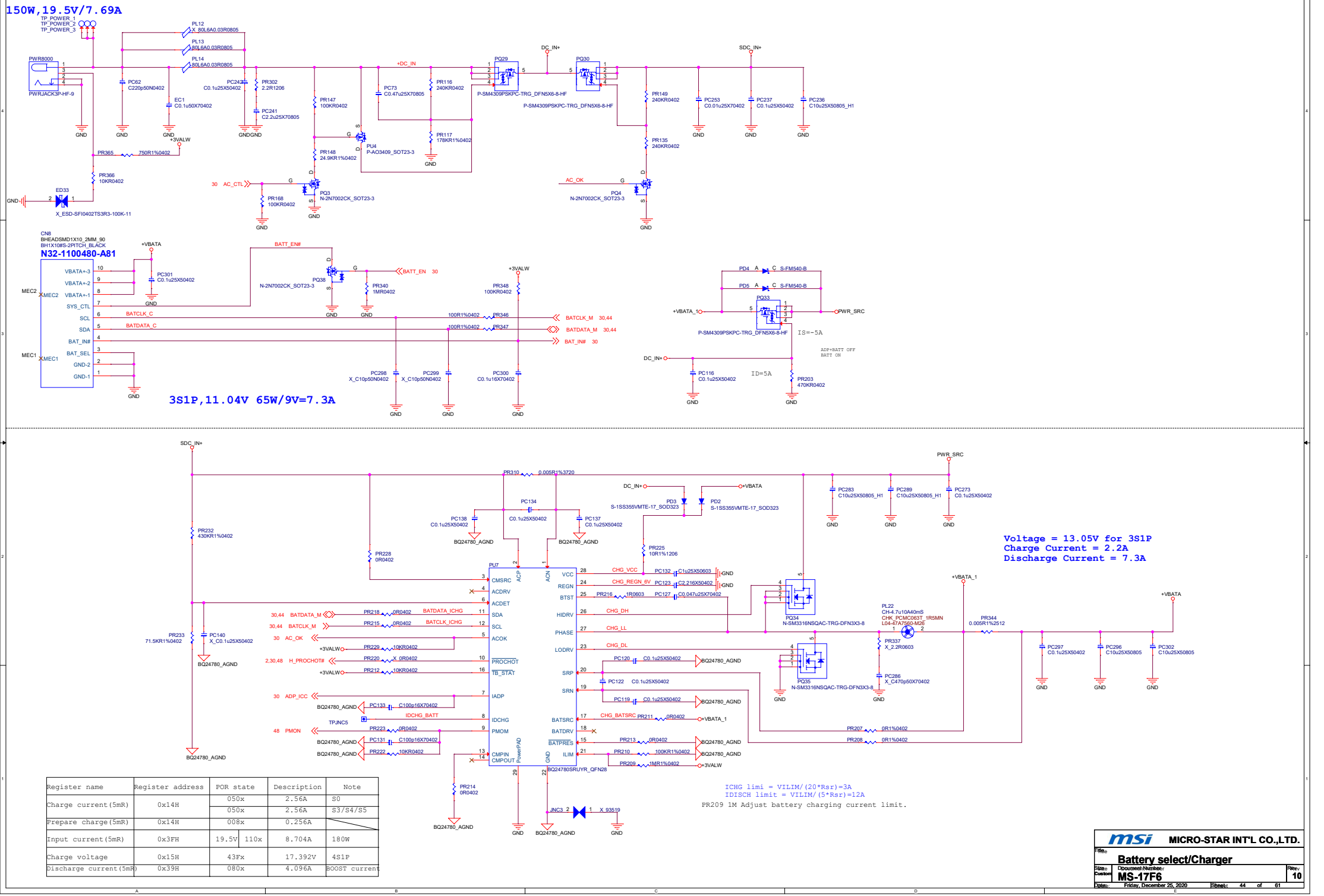

Register name	Register address	POR state	Description	Note
Charge current(5mR)	0x14H	050x	2.56A	S0
		050x	2.56A	S3/S4/S5
Prepare charge(5mR)	0x14H	008x	0.256A	
Input current(5mR)	0x3FH	19.5V 110x	8.704A	180W
Charge voltage	0x15H	43Fx	17.392V	4S1P
Discharge current(5mR)	0x39H	080x	4.096A	BOOST current

MICRO-STAR INT'L CO.,LTD.

Title: Battery select/Charger

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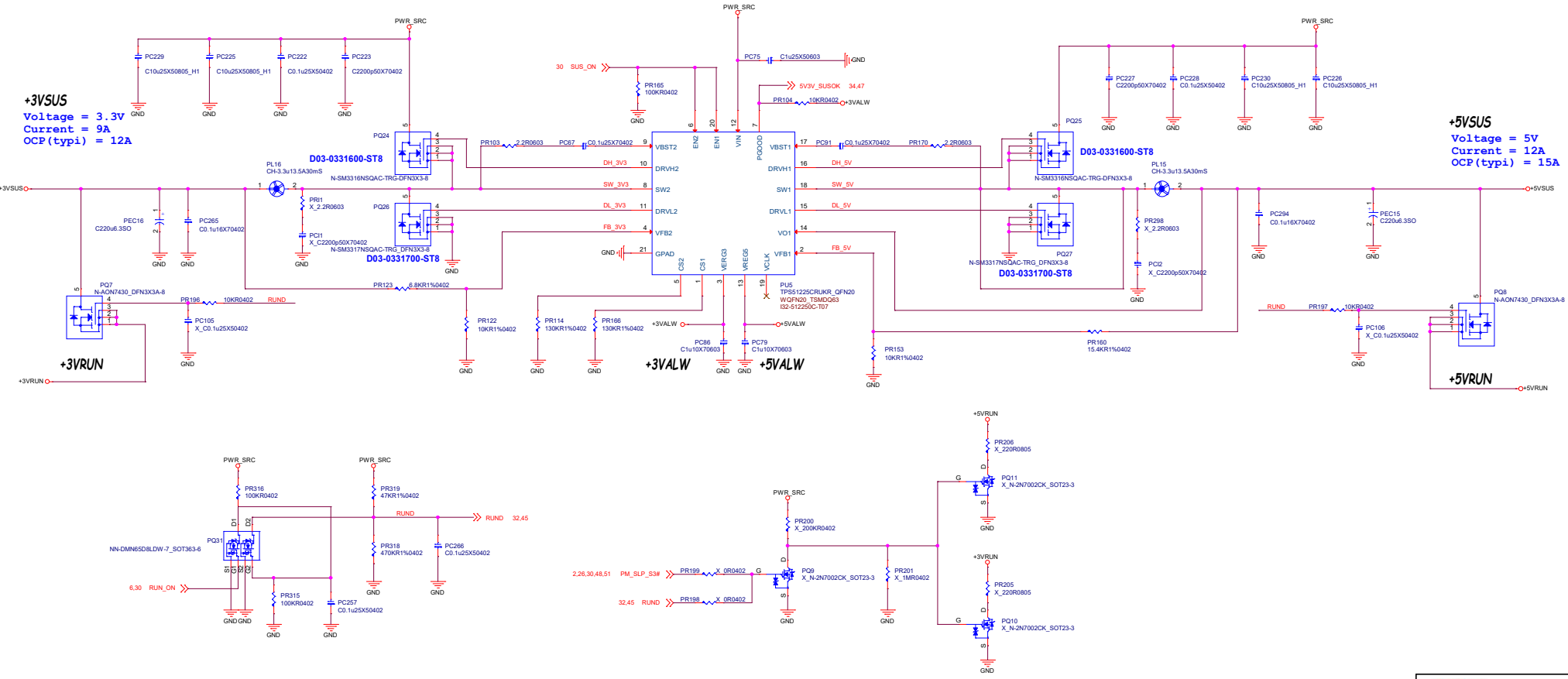
System Power



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Title: System Power			
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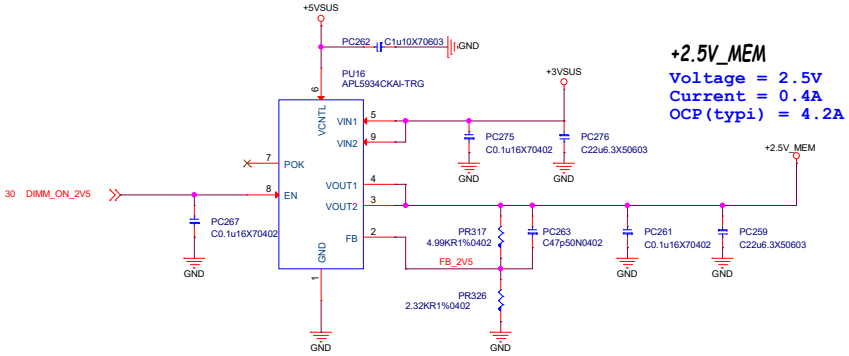
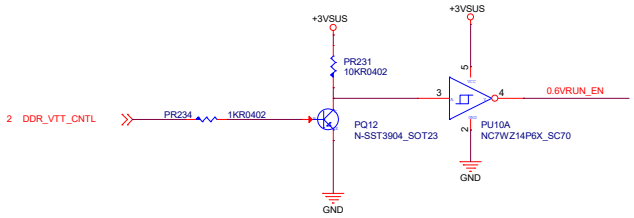
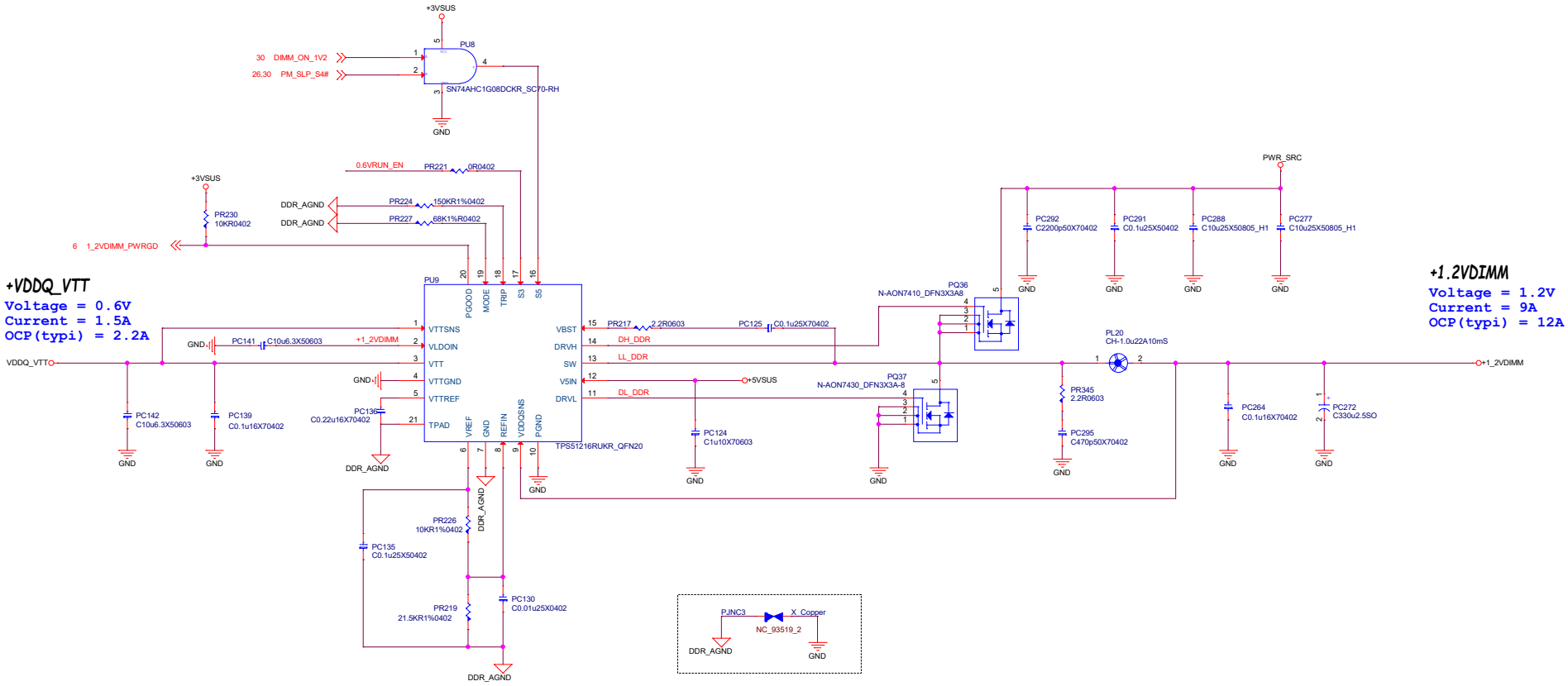
+2.5V_MEM



+2.5V_MEM
Voltage = 2.5V
Current = 0.4A
OCP(typi) = 4.2A



+1.2VDIMM / VDDQ_VTT(0.6V)



+VDDQ_VTT
Voltage = 0.6V
Current = 1.5A
OCP(typi) = 2.2A

+1.2VDIMM
Voltage = 1.2V
Current = 9A
OCP(typi) = 12A

MICRO-STAR INT'L CO.,LTD.			
Title: +2.5VMEM/+1.2VDIMM/VDDQ_VTT			
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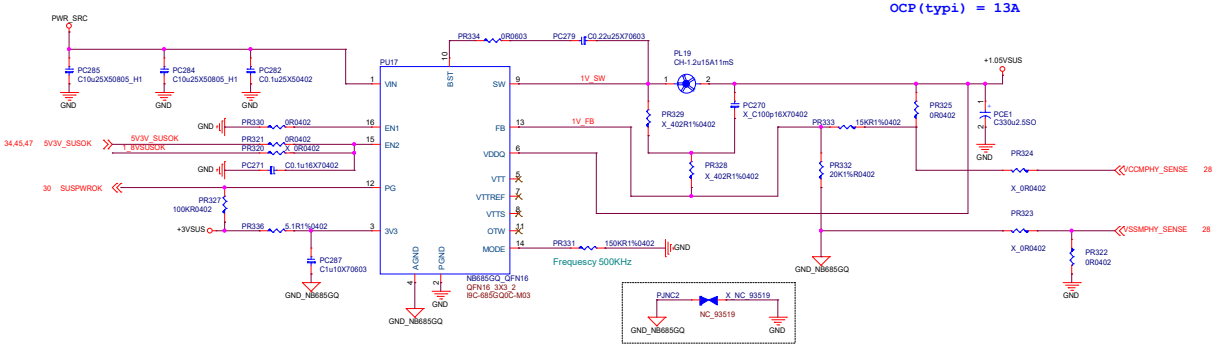
+1.05VSUS

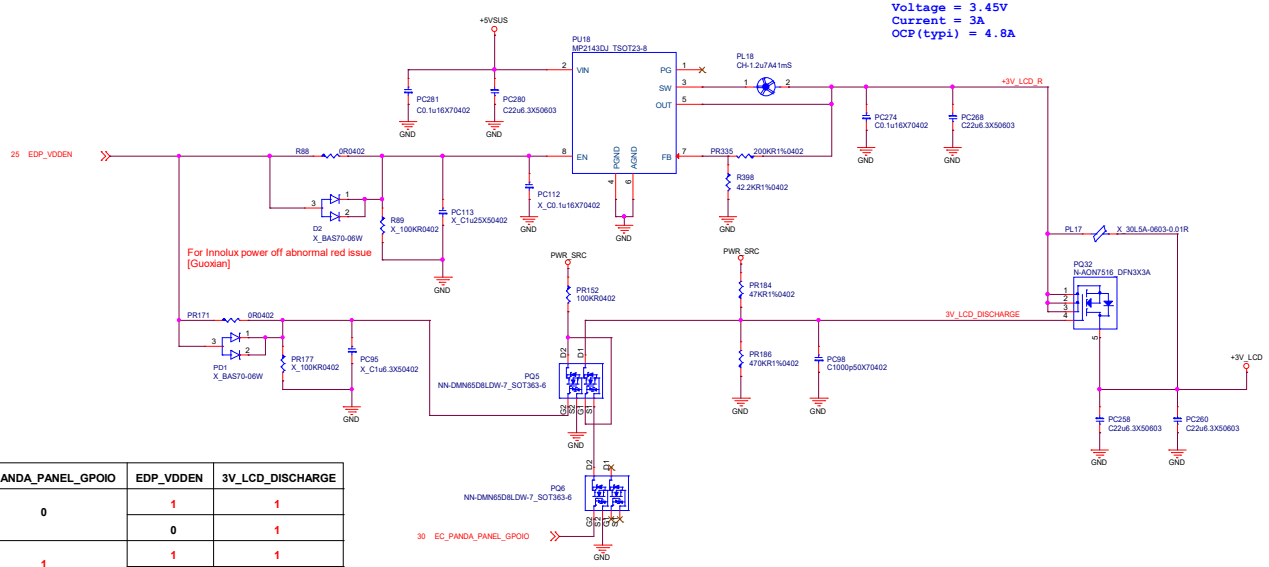
Voltage = 1.05V
Current = 10A
OCP(typi) = 13A



+3V_LCD

Pannel Device Logic Power

Voltage = 3.45V
Current = 3A
OCP(typi) = 4.8A

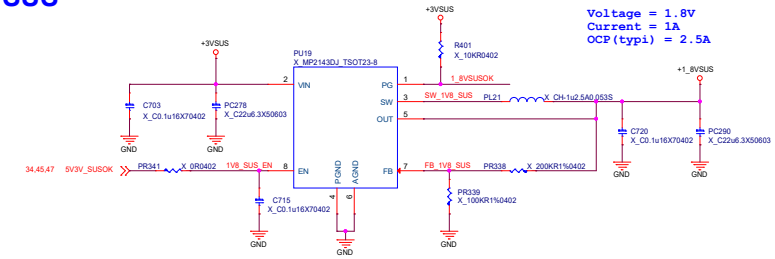


	EC_PANDA_PANEL_GPOIO	EDP_VDDEN	3V_LCD_DISCHARGE
Non-Panda Panel	0	1	1
		0	1
Panda Panel	1	1	1
		0	0

FQ ADD SUPPORT panda_panel

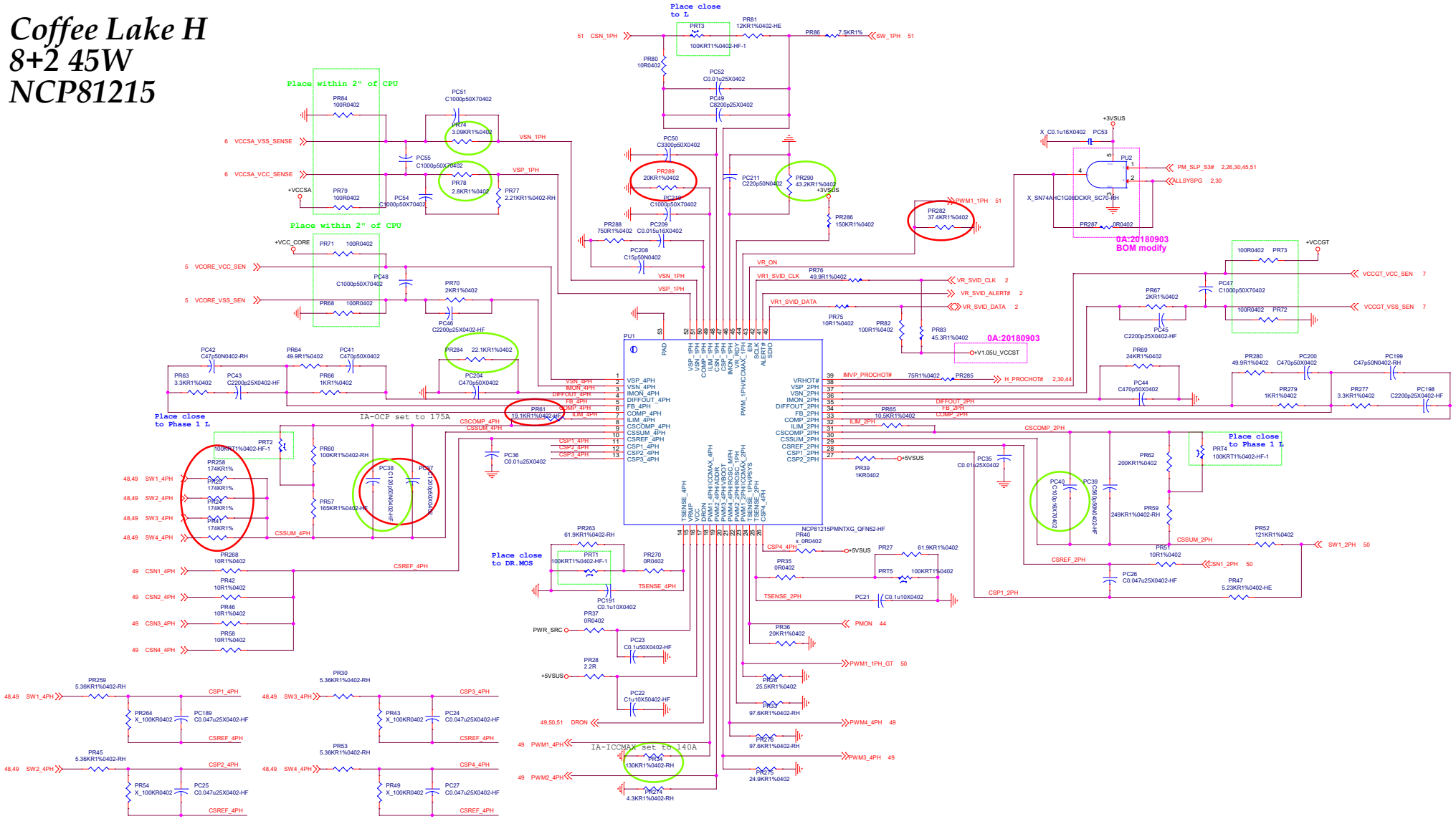
+1_8VSUS

Voltage = 1.8V
Current = 1A
OCP(typi) = 2.5A



MICRO-STAR INT'L CO.,LTD.		
Title	+1.05VSUS/+3V_LCD/+1_8VSUS	
Size: Custom	Document Number: MS-17F6	Rev: 10
Date: Friday, December 25, 2020	Sheet 47 of 61	

Coffee Lake H
8+2 45W
NCP81215

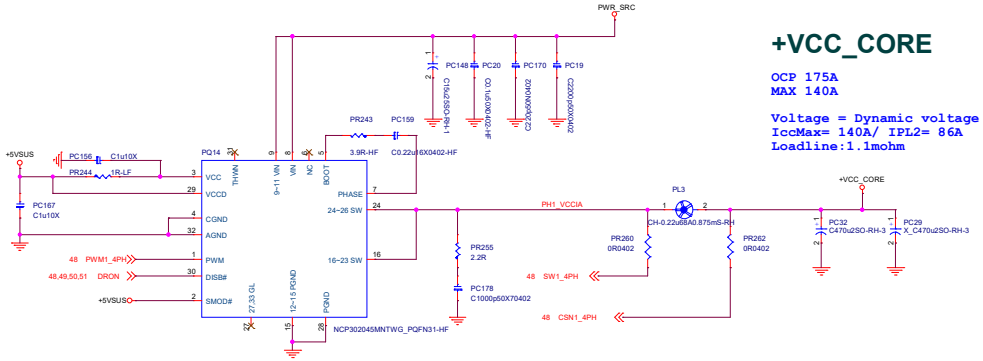


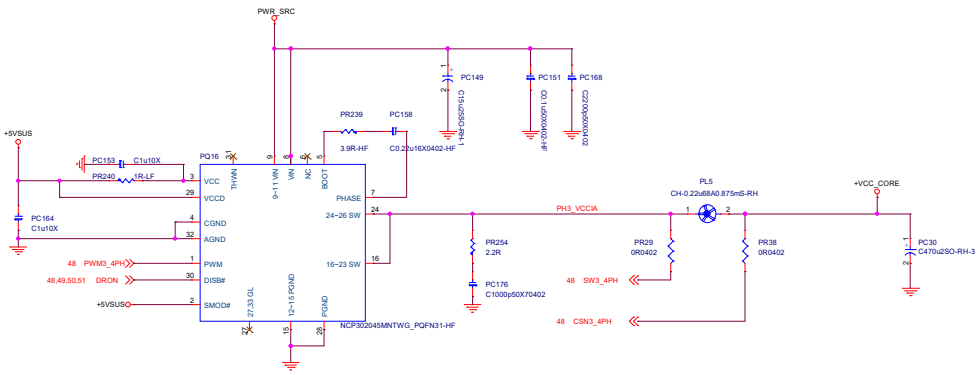
msi	MICRO-STAR INT'L CO.,LTD.		
Title	CPU POWER NCP81215		
Size: A3	Document Number: MS-17F6		Rev: 10
Date: Friday, December 25, 2020	Sheet 48 of 61		

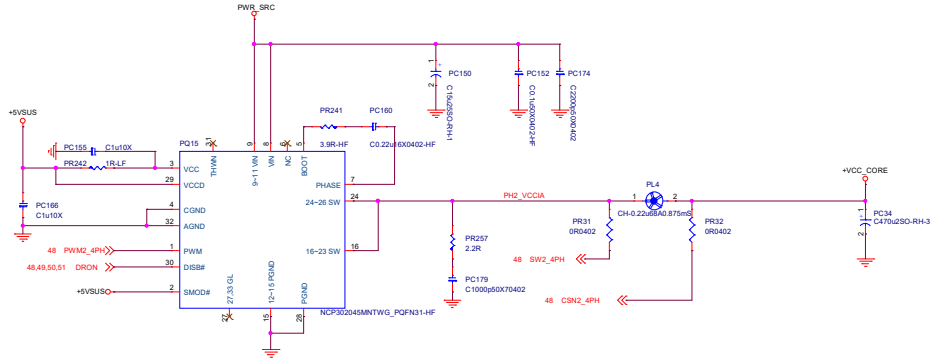
+VCC_CORE

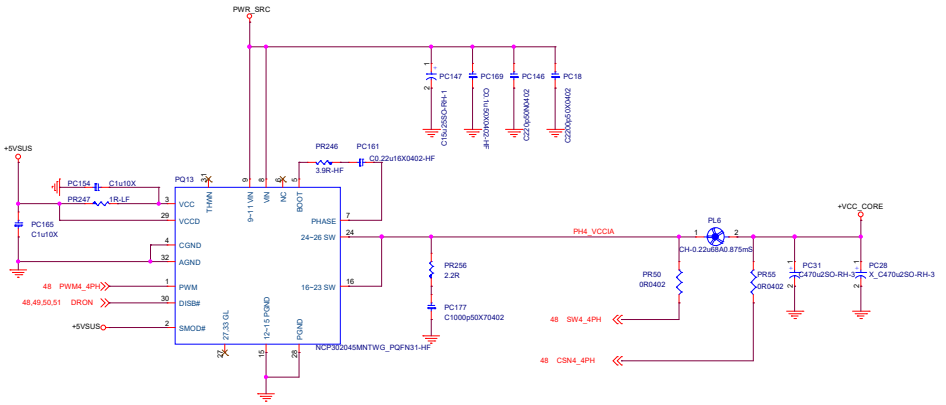
OCP 175A
MAX 140A

Voltage = Dynamic voltage
IccMax= 140A/ IPL2= 86A
Loadline:1.1mohm









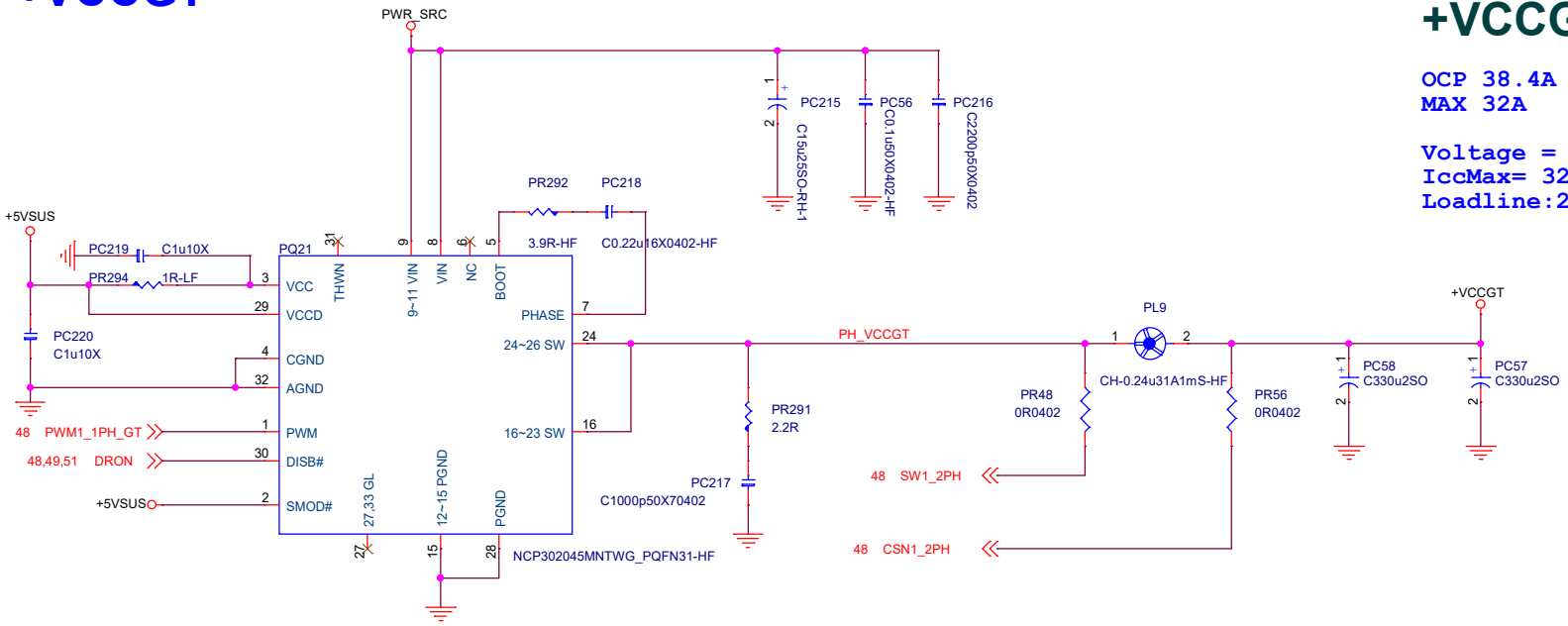
MICRO-STAR INT'L CO.,LTD.

Title: CPU Power (VCore)

Size: Custom | Document Number: MS-17F6 | Rev: 10

Date: Friday, December 25, 2020 | Sheet 49 of 61

+VCCGT



+VCCGT

OCP 38.4A
MAX 32A

Voltage = SVID
IccMax= 32A/ IPL2= 25A
Loadline:2.7mohm

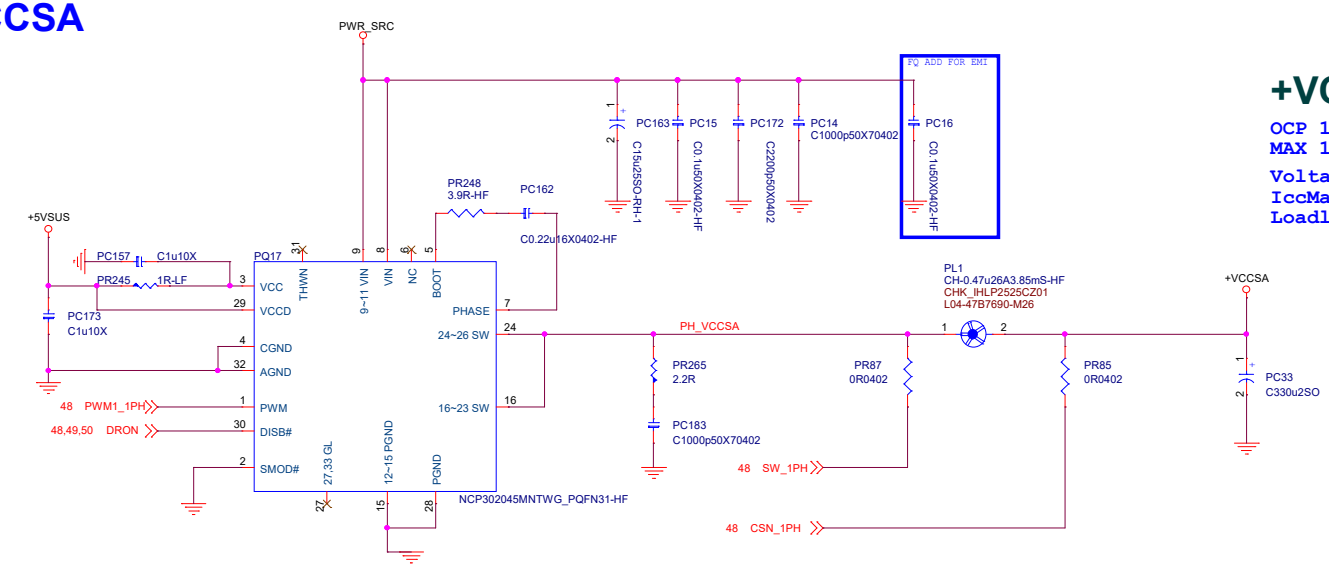
MICRO-STAR INT'L CO.,LTD.

Title: CPU Power (VCCGT)

Size: Custom | Document Number: MS-17F6 | Rev: 10

Date: Friday, December 25, 2020 | Sheet 50 of 61

+VCCSA

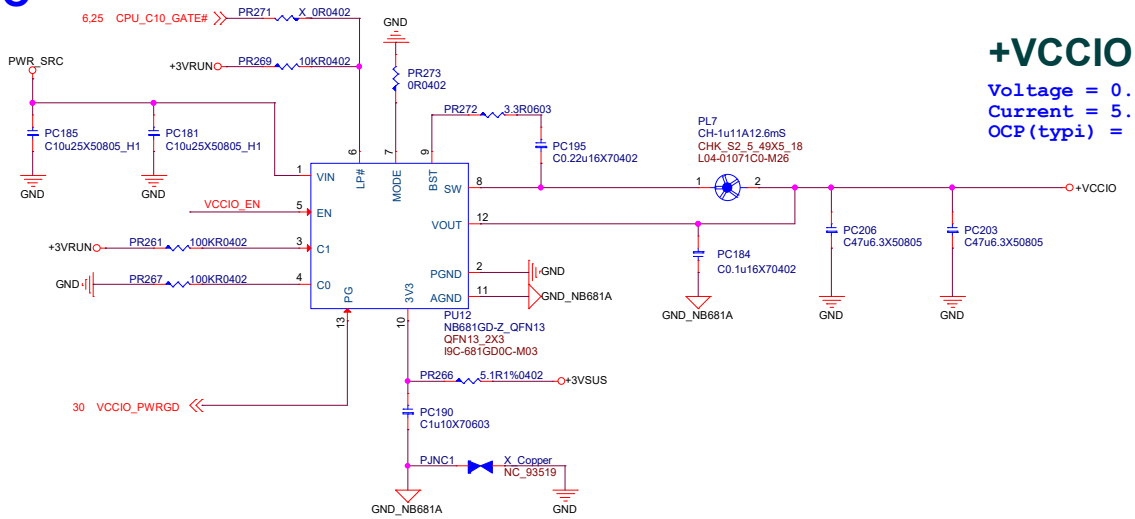


+VCCSA

OCP 13.3A
MAX 11.1A

Voltage = SVID
IccMax= 11.1A/ IPL2= 10A
Loadline:10.3mohm

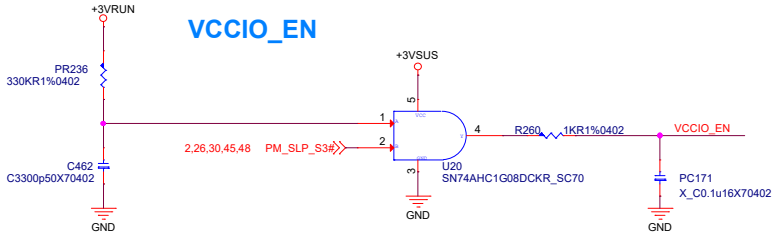
+VCCIO



+VCCIO

Voltage = 0.95V
Current = 5.5A
OCP(typi) = 7.5A

VCCIO_EN



MICRO-STAR INT'L CO.,LTD.	
Title: CPU Power (VCCSA/VCCIO)	
Size: Custom	Document Number: MS-17F6
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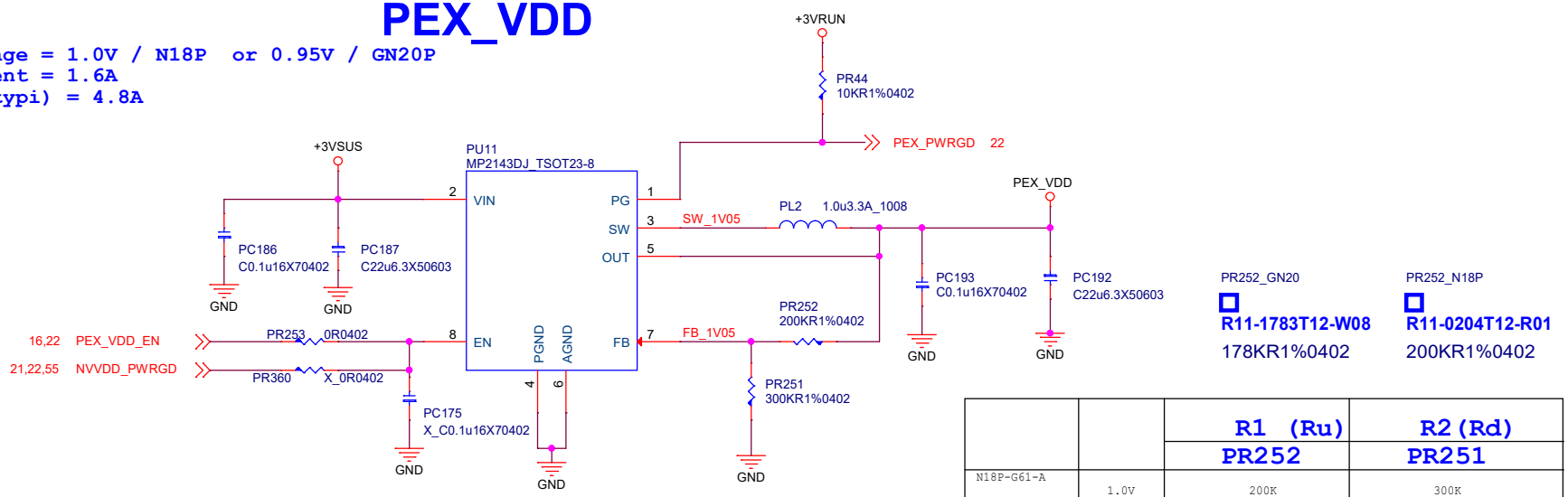
PEX_VDD

Voltage = 1.0V / N18P or 0.95V / GN20P
Current = 1.6A
OCP(typi) = 4.8A



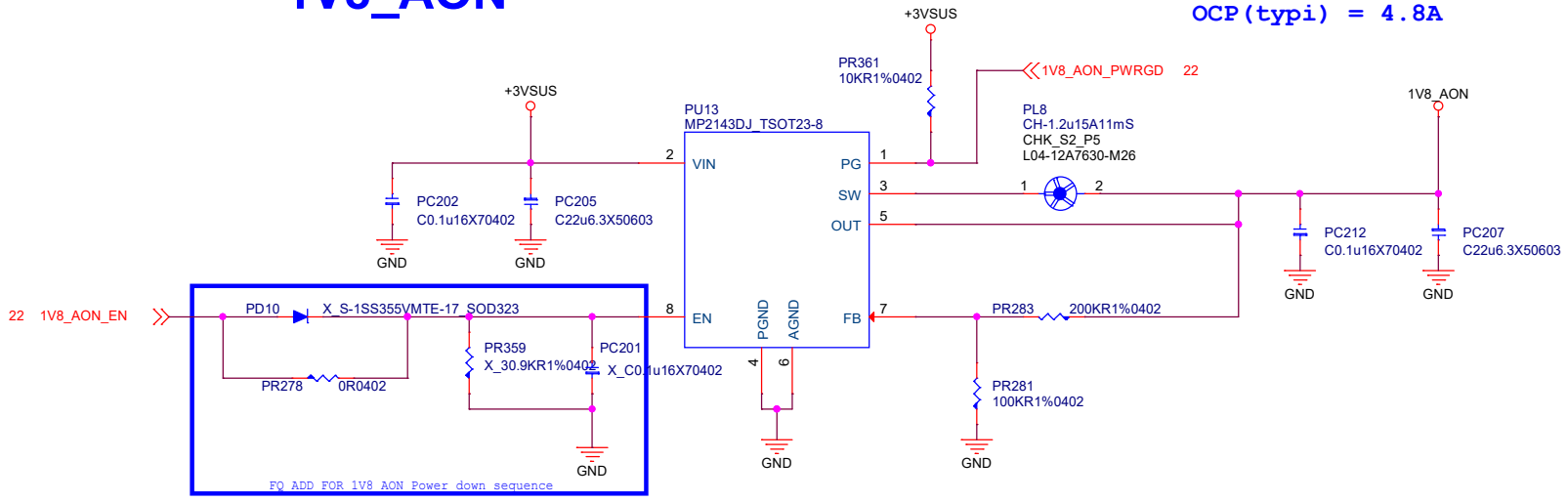
PR252_GN20
R11-1783T12-W08
178KR1%0402

PR252_N18P
R11-0204T12-R01
200KR1%0402

		R1 (Ru)	R2 (Rd)
		PR252	PR251
N18P-G61-A	1.0V	200K	300K
GN20-P	0.95V	178K	300K

1V8_AON

Voltage = 1.8V
Current = 1.7A
OCP(typi) = 4.8A



msi	MICRO-STAR INT'L CO.,LTD.		
Title	DGPU POWER PEX_VDD/1V8_AON		
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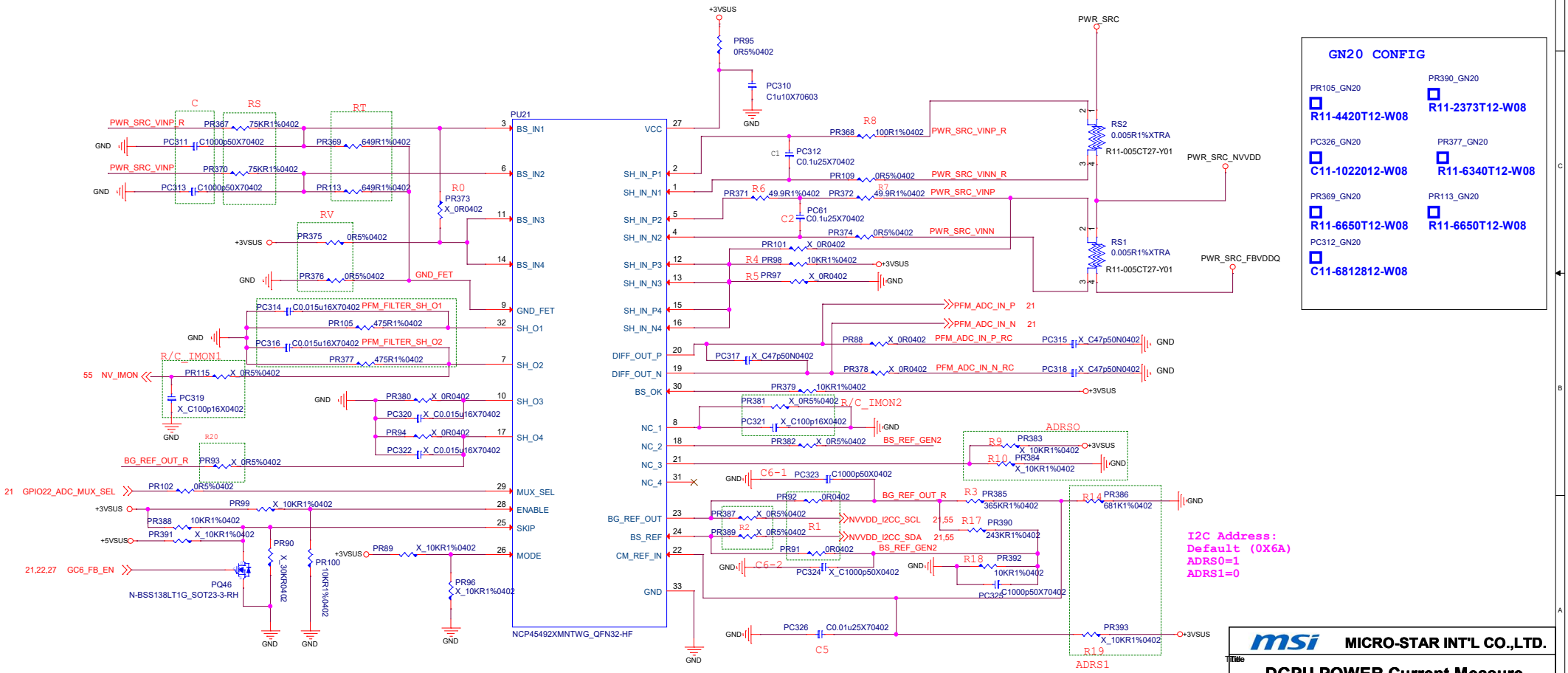
PU21
NCP45492XMNTWG_QFN32-HF
BS_IN1
BS_IN2
BS_IN3
BS_IN4
GND_FET
SH_O1
SH_O2
SH_O3
SH_O4
MUX_SEL
ENABLE
SKIP
MODE
VCC
SH_IN_P1
SH_IN_N1
SH_IN_P2
SH_IN_N2
SH_IN_P3
SH_IN_N3
SH_IN_P4
SH_IN_N4
DIFF_OUT_P
DIFF_OUT_N
BS_OK
NC_1
NC_2
NC_3
NC_4
BG_REF_OUT
BS_REF
CM_REF_IN
GND
+3VSUS
PR95 0R5%0402
PC310 C1u10X70603
PWR_SRC
PWR_SRC_NVVDD
PWR_SRC_FBVDDQ
RS2 0.005R1%XTRA
R11-005CT27-Y01
RS1 0.005R1%XTRA
R11-005CT27-Y01
PR368 100R1%0402 PWR_SRC_VINP_R
PR109 0R5%0402 PWR_SRC_VINN_R
PR372 49.9R1%0402 PWR_SRC_VINP
PR374 0R5%0402 PWR_SRC_VINN
PC312 C0.1u25X70402
PC61 C0.1u25X70402
PR101 X_0R0402
PR98 10KR1%0402
PR97 X_0R0402
PFM_ADC_IN_P 21
PFM_ADC_IN_N 21
PR88 X_0R0402 PFM_ADC_IN_P_RC
PR378 X_0R0402 PFM_ADC_IN_N_RC
PC315 X_C47p50N0402
PC318 X_C47p50N0402
PC317 X_C47p50N0402
PR379 10KR1%0402
PR381 X_0R5%0402
PC321 X_C100p16X0402
R/C_IMON2
PR382 X_0R5%0402
BS_REF_GEN2
ADRS0
R9 PR383 X_10KR1%0402
R10 PR384 X_10KR1%0402
C6-1 PC323 C1000p50X0402
PR92 0R0402
BG_REF_OUT_R
R3 PR385 365KR1%0402
R14 PR386 681K1%0402
PR387 X_0R5%0402
PR389 X_0R5%0402
NVVDD_I2CC_SCL 21,55
NVVDD_I2CC_SDA 21,55
R17 PR390 243KR1%0402
PR91 0R0402
BS_REF_GEN2
C6-2 PC324 X_C1000p50X0402
R18 PR392 10KR1%0402
PC325 C1000p50X70402
PC326 C0.01u25X70402
C5
PR393 X_10KR1%0402
R19
ADRS1
PR367 75KR1%0402
PR369 649R1%0402
PR370 75KR1%0402
PR113 649R1%0402
R0 PR373 X_0R0402
RV
PR375 0R5%0402
PR376 0R5%0402
GND_FET
PC314 C0.015u16X70402 PFM_FILTER_SH_O1
PR105 475R1%0402
PC316 C0.015u16X70402 PFM_FILTER_SH_O2
PR377 475R1%0402
R/C_IMON1
55 NV_IMON
PR115 X_0R5%0402
PC319 X_C100p16X0402
PR380 X_0R0402
PC320 X_C0.015u16X70402
PR94 X_0R0402
PC322 X_C0.015u16X70402
BG_REF_OUT_R
PR93 X_0R5%0402
21 GPIO22_ADC_MUX_SEL
PR102 0R5%0402
PR99 X_10KR1%0402
PR388 10KR1%0402
PR391 X_10KR1%0402
21,22,27 GC6_FB_EN
PQ46 N-BSS138LT1G_SOT23-3-RH
PR90 X_30KR0402
PR100 10KR1%0402
PR89 X_10KR1%0402
PR96 X_10KR1%0402
GN20 CONFIG
PR105_GN20
R11-4420T12-W08
PR390_GN20
R11-2373T12-W08
PC326_GN20
C11-1022012-W08
PR377_GN20
R11-6340T12-W08
PR369_GN20
R11-6650T12-W08
PR113_GN20
R11-6650T12-W08
PC312_GN20
C11-6812812-W08
I2C Address:
Default (0X6A)
ADRS0=1
ADRS1=0
MICRO-STAR INT'L CO.,LTD.
Title
DGPU POWER Current Measure
Size
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10
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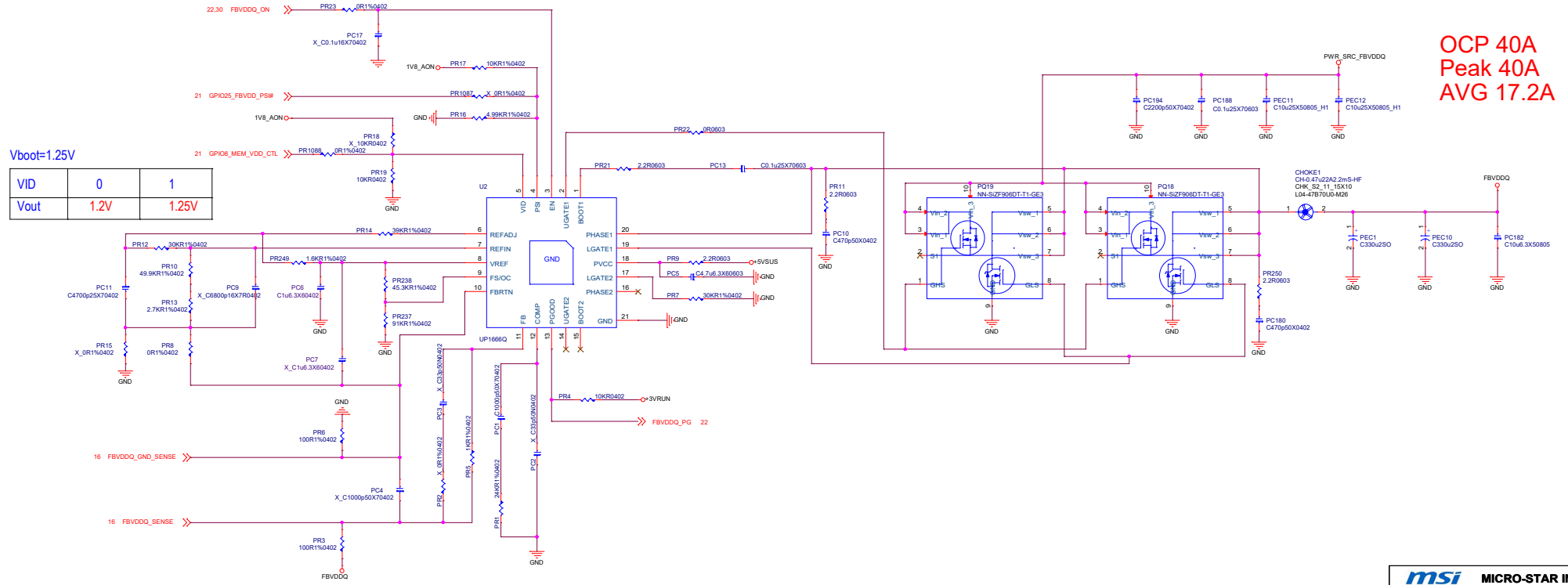
FBVDDQ



MICRO-STAR INT'L CO.,LTD.

Title: DGPU POWER FBVDDQ

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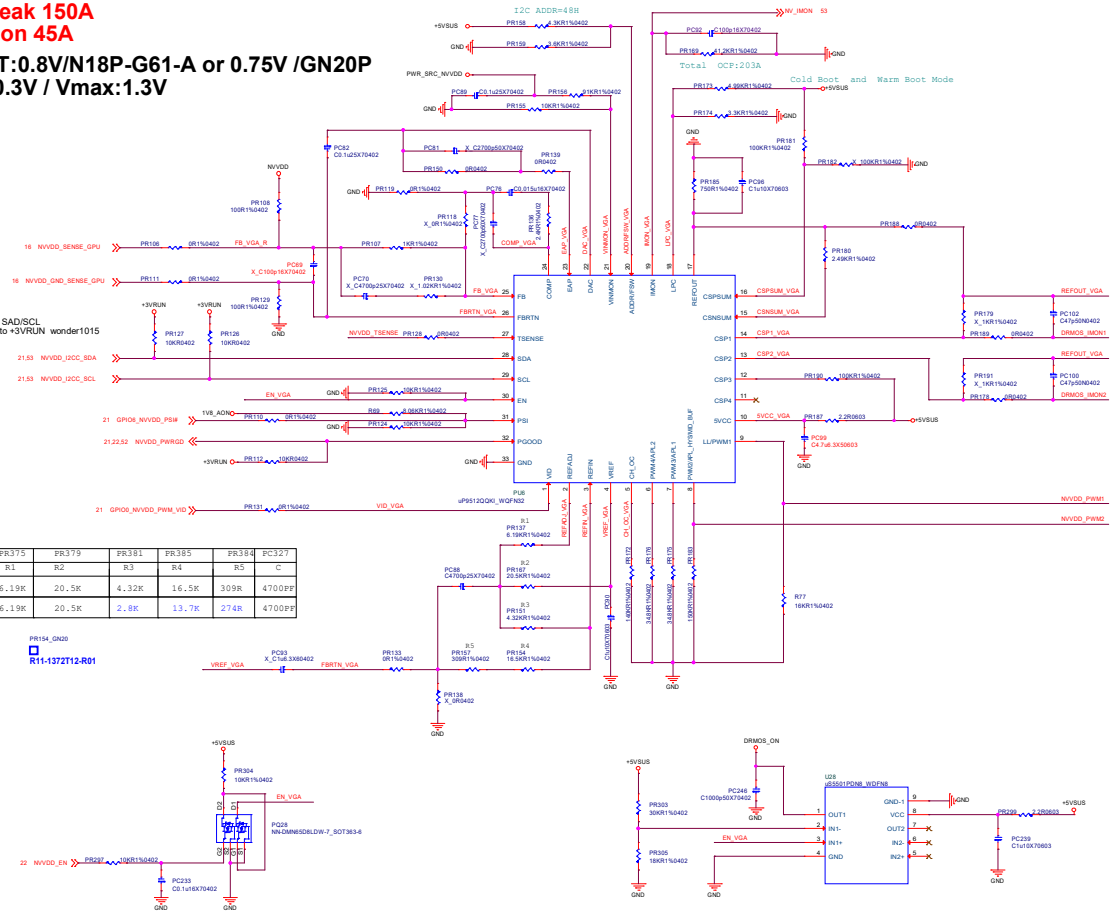
DGPU POWER NVVDD
UP9512Q

EDP-Peak 150A
EDP-Con 45A

VBOOT:0.8V/N18P-G61-A or 0.75V /GN20P
Vmin:0.3V / Vmax:1.3V

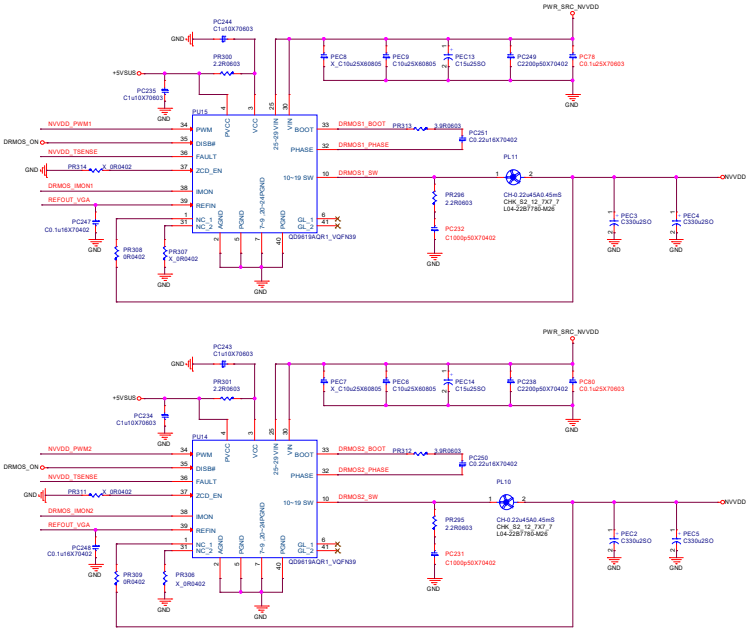


	PR375	PR379	PR381	PR385	PR384	PC327
CONFIG	R1	R2	R3	R4	R5	C
N18P-G61-A	6.19K	20.5K	4.32K	16.5K	309R	4700PF
GN20-P	6.19K	20.5K	2.8K	13.7K	274R	4700PF

PR151_GN20
R11-0282T12-Y01

PR154_GN20
R11-1372T12-R01

PR157_GN20
R11-2740T12-R01



MSI	MICRO-STAR INT'L CO.,LTD.
Title	DGPU POWER NVVDD
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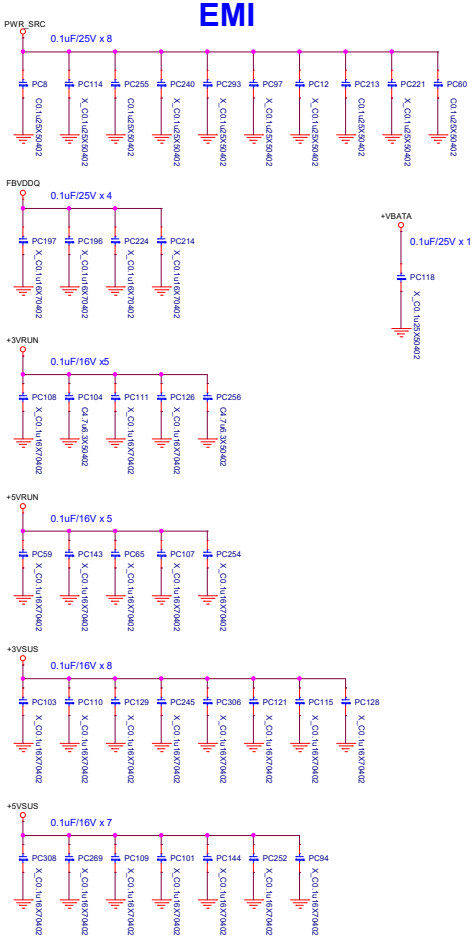
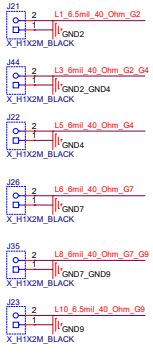
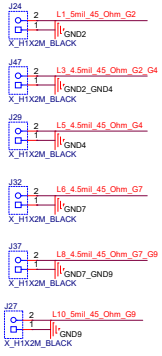
EMI



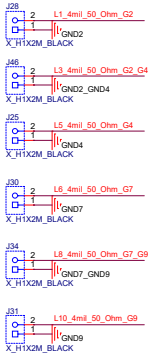
40 OHM Single-End



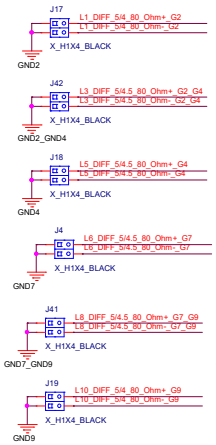
45 OHM Single-End



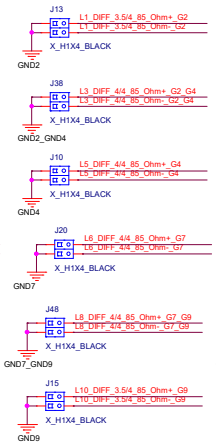
50 OHM Single-End



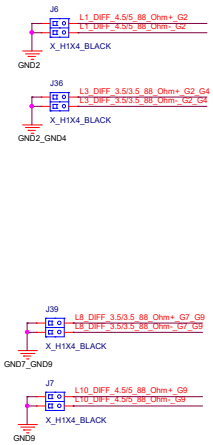
80 OHM Differential



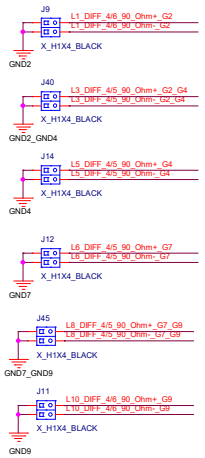
85 OHM Differential



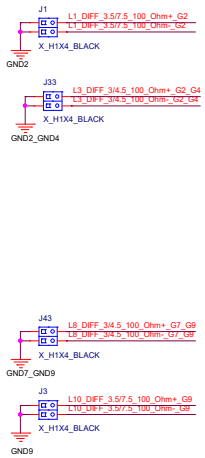
88 OHM Differential



90 OHM Differential



100 OOHM Differential



msi MICRO-STAR INT'L CO.,LTD.		
File: EMI/Impedance		
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DGPU Holes

MGPU2 H_R142D126BR197_MB_N X_CPU_HOLE — GND
MGPU1 H_R142D126BR197_MB_N X_CPU_HOLE — GND
MGPU4 H_R142D126BR197_MB_N X_CPU_HOLE — GND
MGPU3 H_R142D126BR197_MB_N X_CPU_HOLE — GND

CPU Holes

MCPU1 H_R142D126BR197_MB_N X_CPU_HOLE — GND
MCPU2 H_R142D126BR197_MB_N X_CPU_HOLE — GND
MCPU3 H_R142D126BR197_MB_N X_CPU_HOLE — GND

CPU/GPU BRACKET

UME3 CPU BKT — CPU BRACKET — 307-6R10111-HG0
UME4 GPU BKT — GPU BRACKET — 307-6P10212-HG0

SPONGE

UME23 POWER SPONGE — POWER SPONGE — E2Y-7F11111-G40
UME24 USB SPONGE — USB SPONGE — E2Y-7F11211-G40

EMI Gasket

UME22 LAN GASKET — LAN Gasket — E2Y-X036411-CA7

HDD SCREW

SCREW1 — HDD SCREW — E43-1204004-H29
SCREW2 — HDD SCREW — E43-1204004-H29

HDD WASHER

UME25 HDD WASHER — HDD WASHER — E2Y-Z001711-G40
UME26 HDD WASHER — HDD WASHER — E2Y-Z001711-G40

MYLAR

UME5 DDR MYLAR — DDR_MYLAR — E2P-0112911-G40
UME6 DDR MYLAR — DDR_MYLAR — E2P-0112911-G40
UME27 rubber — RUBEER — E2Y-3N12711-Y40
UME28 rubber — RUBEER — E2Y-3N12711-Y40
UME29 rubber — RUBEER — E2Y-3N12711-Y40

UME7 MB MYLAR — MB_MYLAR — E2P-6P11311-G40
UME8 MB MYLAR — MB_MYLAR — E2P-6P11311-G40
UME9 MB MYLAR — MB_MYLAR — E2P-6P11311-G40
UME10 MB MYLAR — MB_MYLAR — E2P-6P11311-G40
UME11 MB MYLAR — MB_MYLAR — E2P-6P11311-G40
UME12 MB MYLAR — MB_MYLAR — E2P-6P11311-G40
UME13 MB MYLAR — MB_MYLAR — E2P-6P11311-G40
UME14 MB MYLAR — MB_MYLAR — E2P-6P11311-G40
UME15 MB MYLAR — MB_MYLAR — E2P-6P11311-G40
UME16 MB MYLAR — MB_MYLAR — E2P-6P11311-G40

UME2 BIOS Lable — UEFI_CODE_BIOS_LABEL — G51-N1CO041-A09
UME1 HDMI Lable — HDMI ROYALTY — Y01-RHDMI03-000

PCB1 — PF0-17F6110-T53 — PF0-17F6110-T53

M.2 SSD STAND OFF

H7 Spacer Support — GND — E2B-16J1011-A89 H_R201D118_PTB_N — E2B-16J1010
H6 Spacer Support — GND — E2B-16J1010-A89 H_R201D118_PTB_N — X_E2B-16J1010

MB STAND OFF

H2 Spacer Support — GND — E2B-1P10021-A89 H_R240D150_PT_N — E2B-1P10020
H5 Spacer Support — GND — E2B-1P10021-A89 H_R240D150_PT_N — E2B-1P10020
H4 Spacer Support — GND — E2B-1P10021-A89 H_R240D150_PT_N — E2B-1P10020
H1 Spacer Support — GND — E2B-17F1011-A89 H_R240D150_PT_N — E2B-17F1010
H3 Spacer Support — GND — E2B-1P10021-A89 H_R240D150_PT_N — E2B-1P10020

EMI

E3 — X_HS-MS1011 — GND
E2 — X_HS-MS1011 — GND
E1 — X_HS-MS1011 — GND

MH1 NPTH_80 X_NPTH_80 — GND
MH10 NPTH_80 X_NPTH_80
MH2 H_R315D118_1_N X_H_R315D118_1_N — GND
MH4 H_R315D118_1_N X_H_R315D118_1_N — GND
MH7 H_R315D118_1_N X_H_R315D118_1_N — GND
MH3 H_R315D118_1_N X_H_R315D118_1_N — GND
MH9 H_R315D118_N X_H_R315D118_N — GND
MH8 H_R315D118_N X_H_R315D118_N — GND
MH5 H_R315D118_N X_H_R315D118_N — GND
MH6 H_R315D118_N X_H_R315D118_N — GND
XX4 NPTH118 X_NPTH118
XX3 NPTH118 X_NPTH118
XX1 NPTH118 X_NPTH118
XX2 NPTH118 X_NPTH118
XX5 NPTH118 X_NPTH118
XX6 NPTH118 X_NPTH118

FM24 FM20 FM12 FM23 FM5 — X_F_PAD_NB_2
FM9 FM4 FM17 — X_F_PAD_NB_2
FM13 FM6 FM2 FM1 FM8 — X_F_PAD_X
FM10 FM11 FM16 FM18 FM14 — X_F_PAD_X
FM7 FM19 FM3 FM15 FM22 — X_F_PAD_X
FM21 FM27 FM26 FM28 FM25 — X_F_PAD_X

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Title	Screw/ME		
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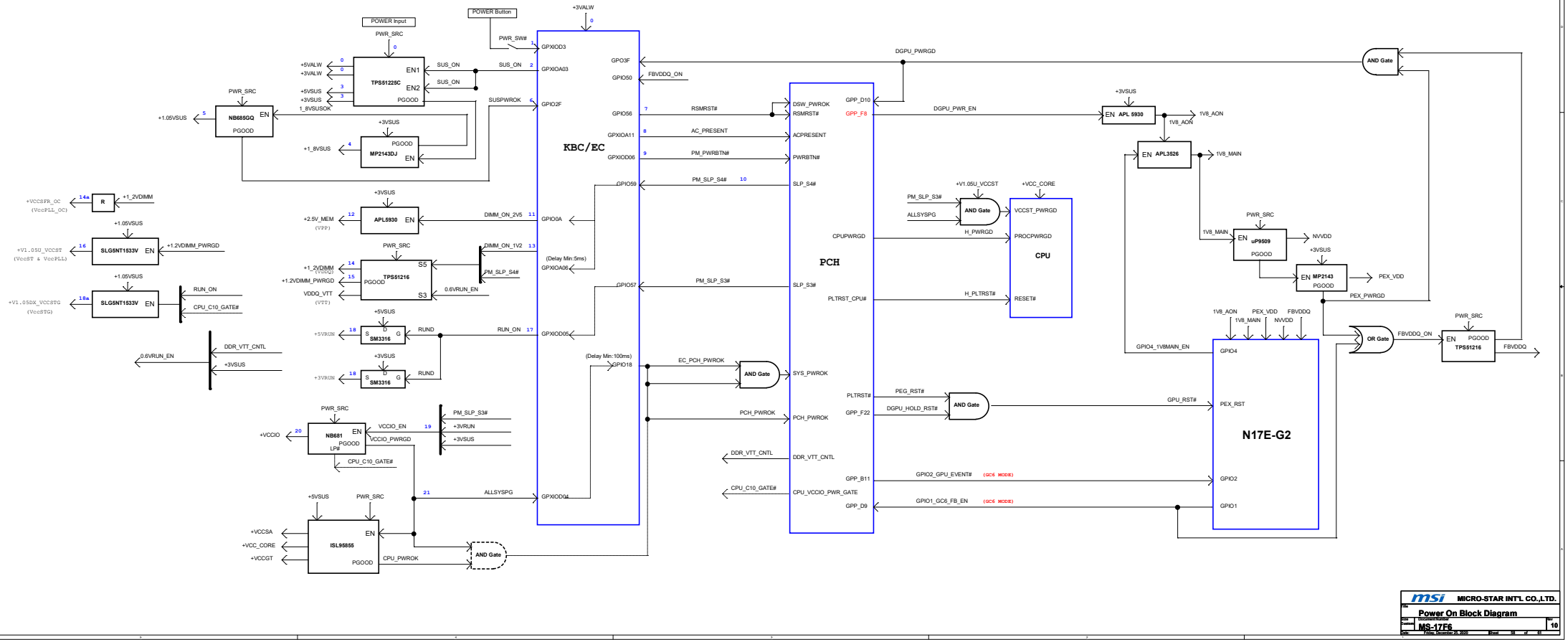
MS-16R1 Power on Block Diagram



msi	MICRO-STAR INT'L CO.,LTD.		
Title	Power On Block Diagram		
Size	Document Number		Rev
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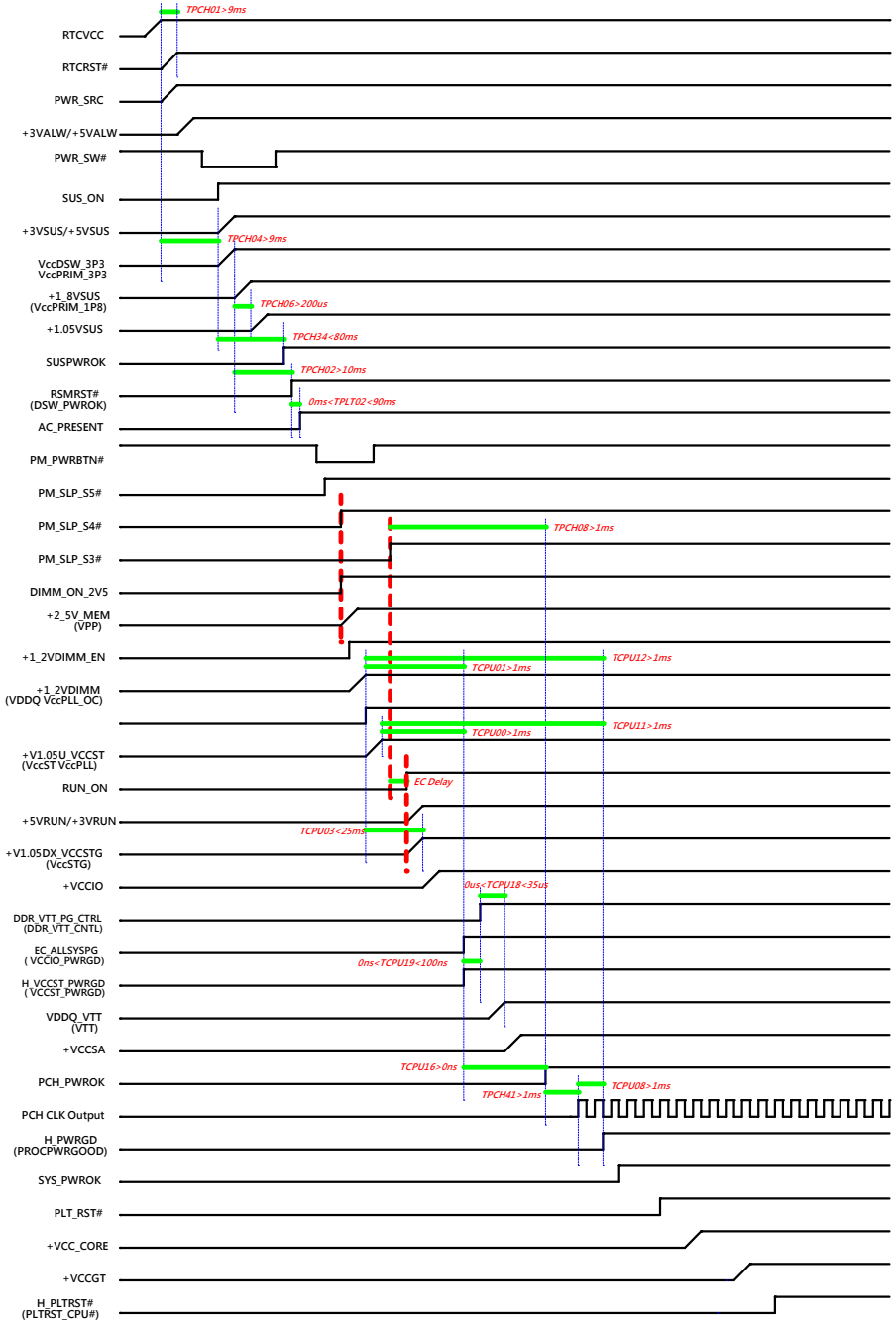
G3 -> S0



msi	MICRO-STAR INT'L CO.,LTD.	
Title: Power ON Block Diagram		
Size: Custom	Document Number: MS-17F6	Rev: 10
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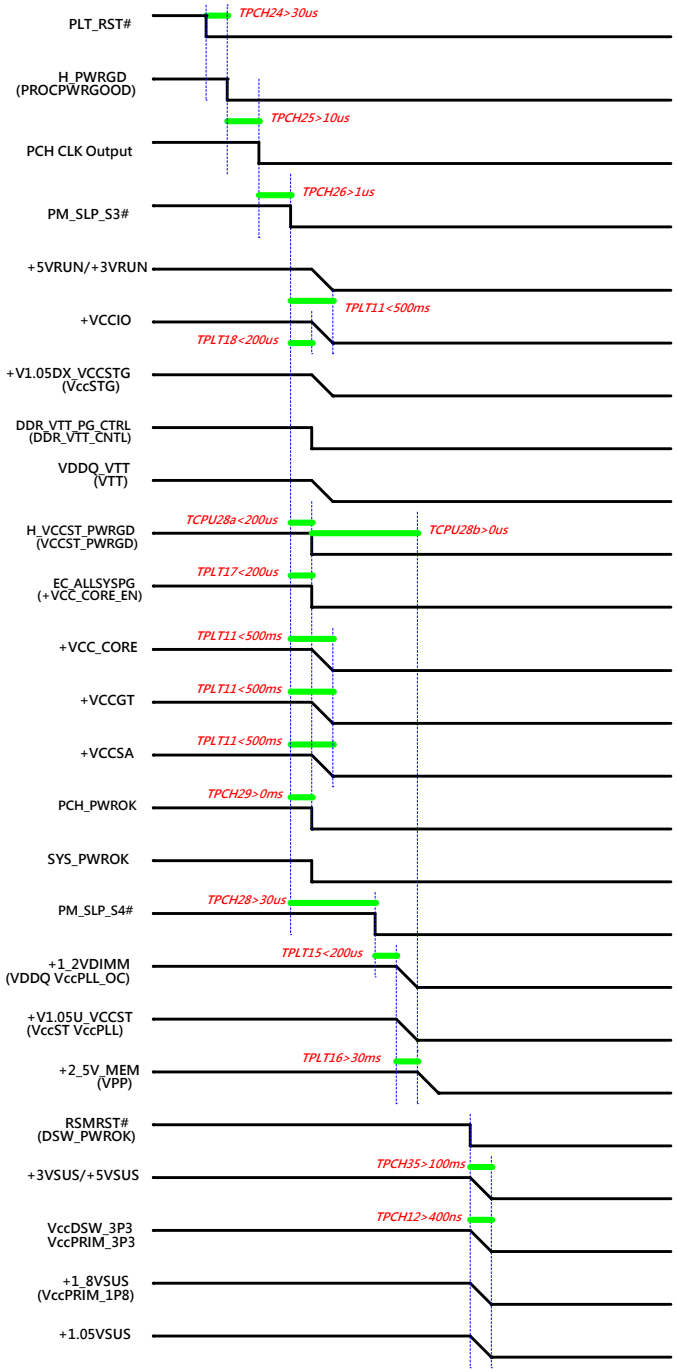
S0 -> G3



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History

DATE	PAGE	DESCRIPTION
2020.8.17		1.Base on 17F4-10 2.Modify CoverSheet 3.Add GPU Sch
2020.9.1		1.Follow Power team 8/28 mail , Modify 2. Change GPU Bracket P/N
2020.9.14		1.Remove FM29 2. ADD Test Point, Power, Power SW, Plt rst

DATE	PAGE	DESCRIPTION

DATE	PAGE	DESCRIPTION

DATE	PAGE	DESCRIPTION

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Title: History

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