Compal Confidential

EH5LP/AP Schematics Document

AMD Picasso Ridge Platform

AMD R19M-M18-70

LA-H801P REV:1.A

2019-03-29

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title	COVER PAGE		
Size: Custom	Document Number: EH5LP/AP_LA-H801P		Rev: 1.A
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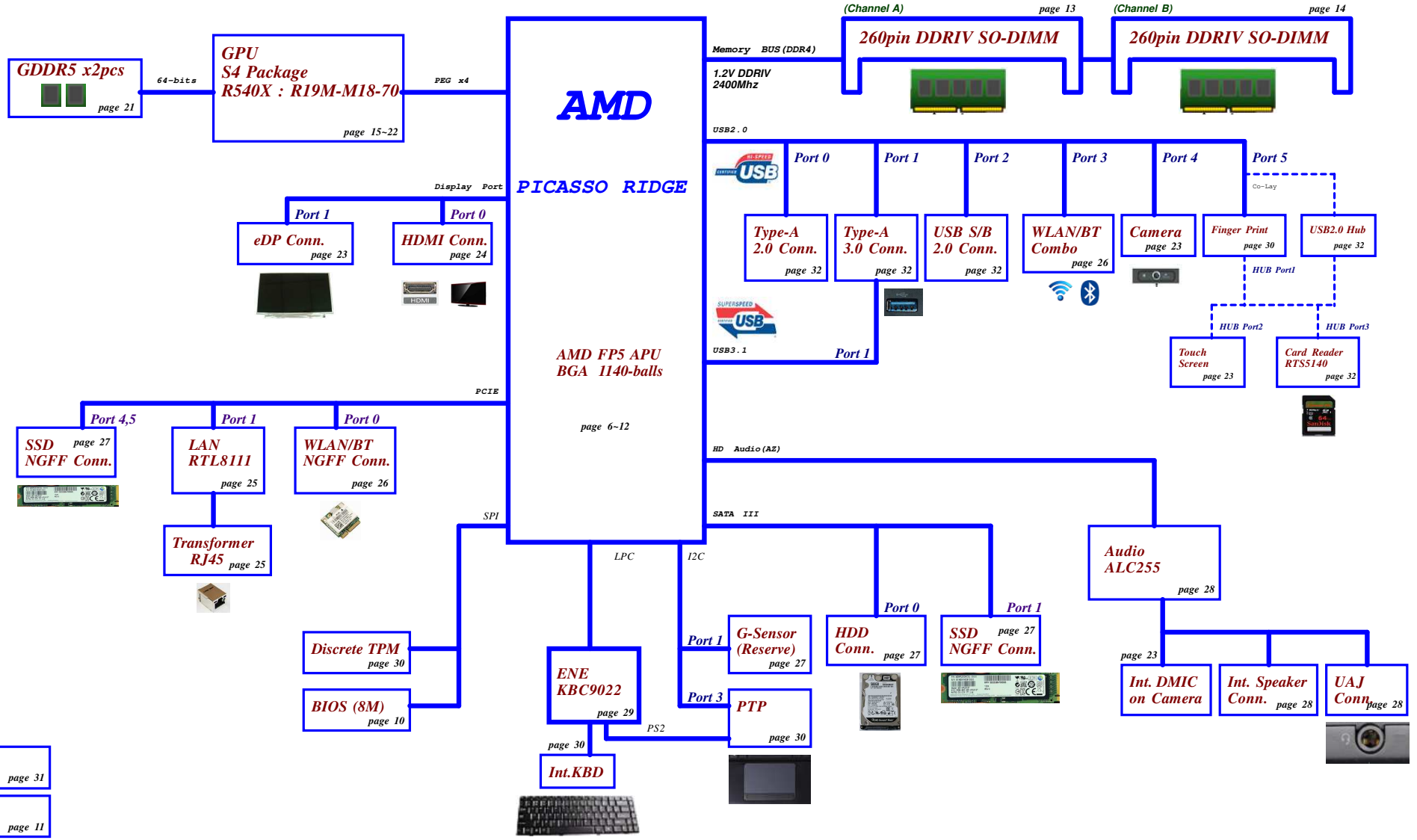
Model Name : EH5LP/AP



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Title	BLOCK DIAGRAMS		
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Voltage Rails

Power Plane	Description	S0	S3	S5
+19V_VIN	Adapter power supply (19V)	ON	ON	ON
+19VB	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+0.8VALW	0.8V always on power rail	ON	ON	OFF
+0.8VS	0.8V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail for APU and DDR	ON	ON	OFF
+1.2V	1.2V power rail for APU and DDR	ON	ON	OFF
+0.6VS	0.6V switched power rail for DDR terminator	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	AC:ON DC:OFF
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power	ON	ON	ON
+3V_LAN	3.3V LAN IC power	ON	ON	OFF
+TP_VCC	3.3V Touch Pad power	ON	ON	OFF
+3VSDGPU	VGA power	ON	OFF	OFF
+1.8VSDGPU	VGA power	ON	OFF	OFF
+VDDCI	VGA power	ON	OFF	OFF
+VGA_CORE	VGA power	ON	OFF	OFF
+FP_VCC	3.3V Finger Print power	ON	ON	OFF

APU SMBus/I2C Address Table

Master	Device	Address[7:1]	Address [7:0] Write	Address [7:0] Read
I2C Port 0 (+1.8VS)				
I2C Port 1 (+1.8VS)	G-Sensor (Reserver)	0001 1000b 18h	0011 0000b 30h	0011 0001b 31h
I2C Port 2 (+3VS)				
SBMus Port 0 (+3VS)	JDIMM1	0101 0000b 50h	1010 0000b A0h	1010 0001b A1h
	JDIMM2	0101 0001b 51h	1010 0010b A2h	1010 0011b A3h
I2C Port 3 (+3VALW)	PTP (Synaptics)	0010 1100b 2Ch	0101 1000b 58h	0101 1001b 59h
	PTP (ELAN)	0001 1111b 15h	0011 1110b 3Eh	0011 1111b 3Fh
SMBus Port 1 (+3VALW)				

EC SMBus Address Table

SMBus Port 1 (+3VALW)	Smart Battery	0000 1011b 0Bh	0001 0110b 16h	0001 0111b 17h
	Charger IC	0000 1001b 09h	0001 0010b 12h	0001 0011b 13h
SMBus Port 2 (+3VS)	APU Temp.	0100 1100b 4Ch	1001 1000b 98h	1001 1001b 99h
	GPU Temp.	0100 0001b 41h	1000 0010b 82h	1000 0011b 83h

BOARD ID Table

Board ID	PCB Revision
0	EVT
1	DVT
2	PVT
3	

ZZZ_@
DA60025X000
PCB 2MK LA-H801P REV0 MB 3

ZZZ_@
DAZ2MK00100
PCB EH5LP LA-H801P LS-H801P/H802P

ZZZ_PCB1A@
DAZ2MK00101
PCB EH5LP LA-H801P LS-H801P/H802P

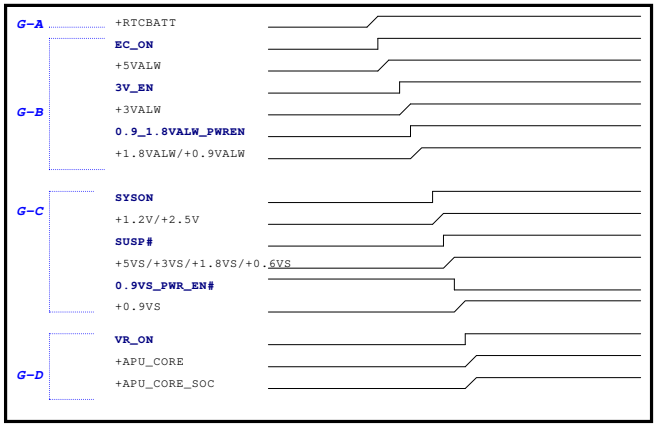
BOM Structure Table

BOM Structure	BTO Item
@	Unpop
EMC@/@EMC@	EMI/ESD Pop/Unpop
45@	HDMI Royalty
CONN@	Mechanical Connector
JP@	Jump
RS@	R-Short
TP@	Test Point
TPM@	TPM Circuits
PCIE@	PCIE SSD
SATA@	SATA SSD
GS@	G-Sensor Circuits
EH5LP@/EH5AP@	Aspire3/Aspire5 Config.
PAR@	SATA Redriver PARADE solution
CR@	Card Reader Config.
CHG@/NCHG@	USB Charger/Non-Charger
255@	Audio Codec AL255 Design
256@/256EMC@	Audio Codec AL256 Design
UMA@	UMA Config
R3/R5/R7APU@	APU PN Refer p.6
T1@/T2@	APU Type Config
DIS@	VGA Circuits
	GPU and VRAM Config Refer p.23
M1870	R19M-M18-70 GPU
HUB@/NHUB@	USB20 HUB/Non-HUB
FP@/FPEMC@/	Finger Print
HDT@	HDT Circuits

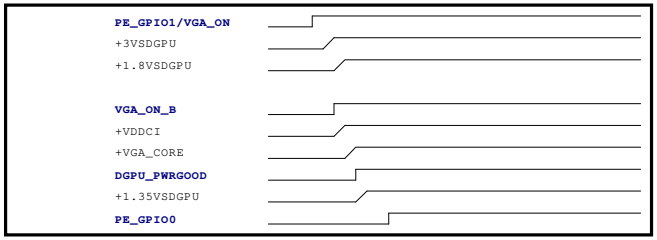
Board ID / SKU ID Table for AD channel

Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V		0xE7 - 0xFF

POWER SEQUENCE



VGA POWER SEQUENCE



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Title: NOTES LIST

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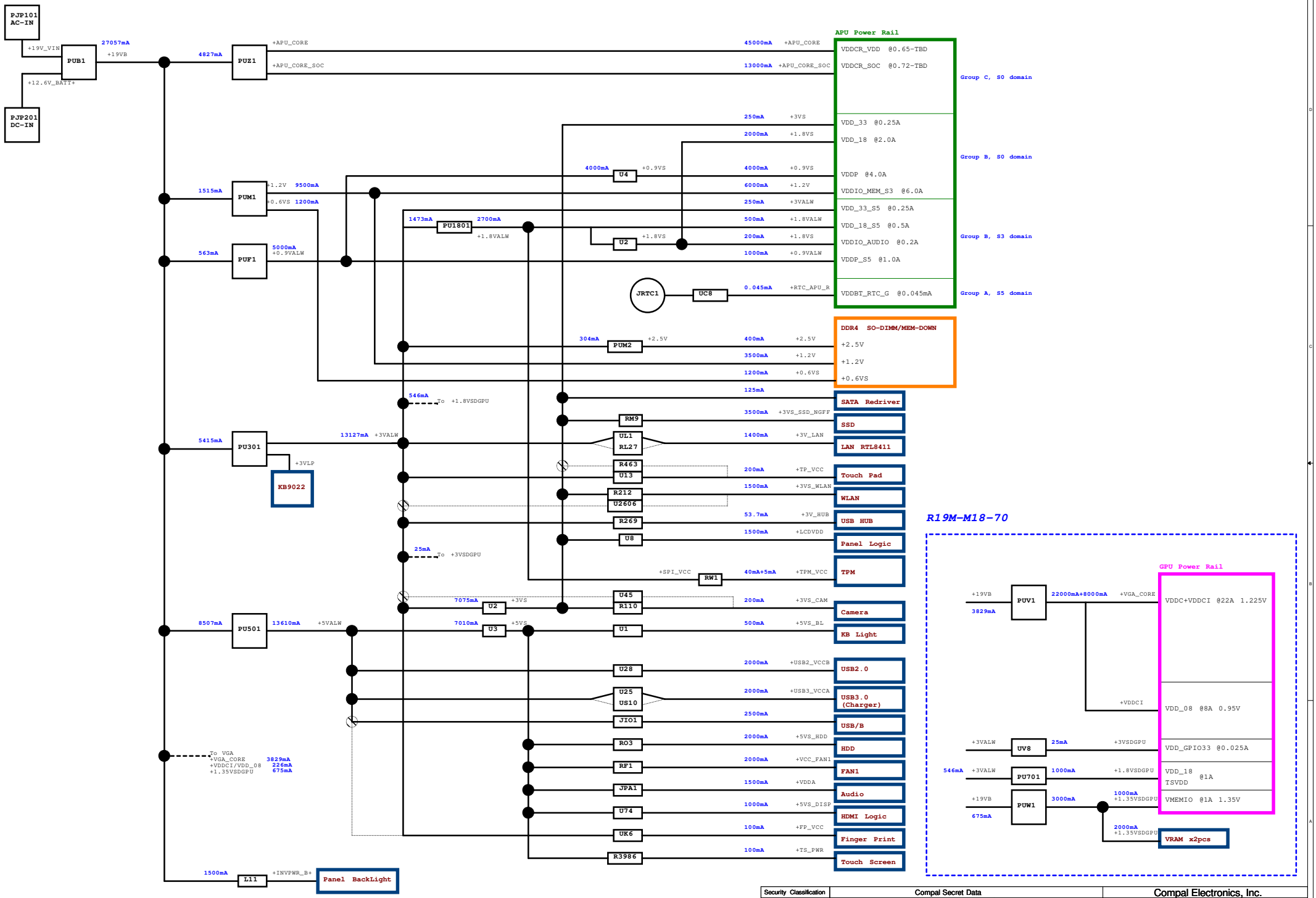

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Title: POWER MAP

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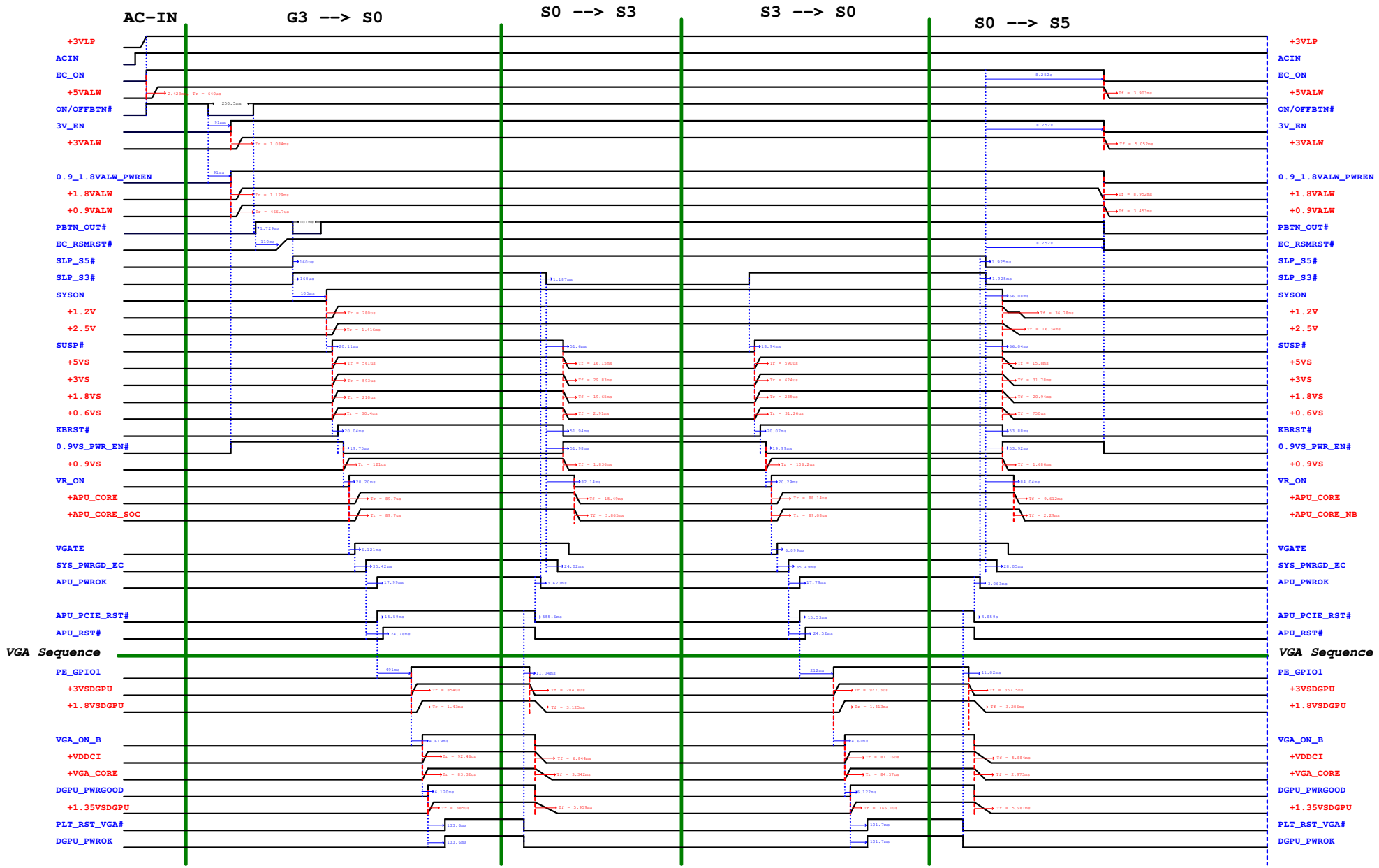
Picasso Ridge Platform Power Sequence



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Size: Custom	Document Number: EH5LP/AP_LA-H801P		Rev: 1.A
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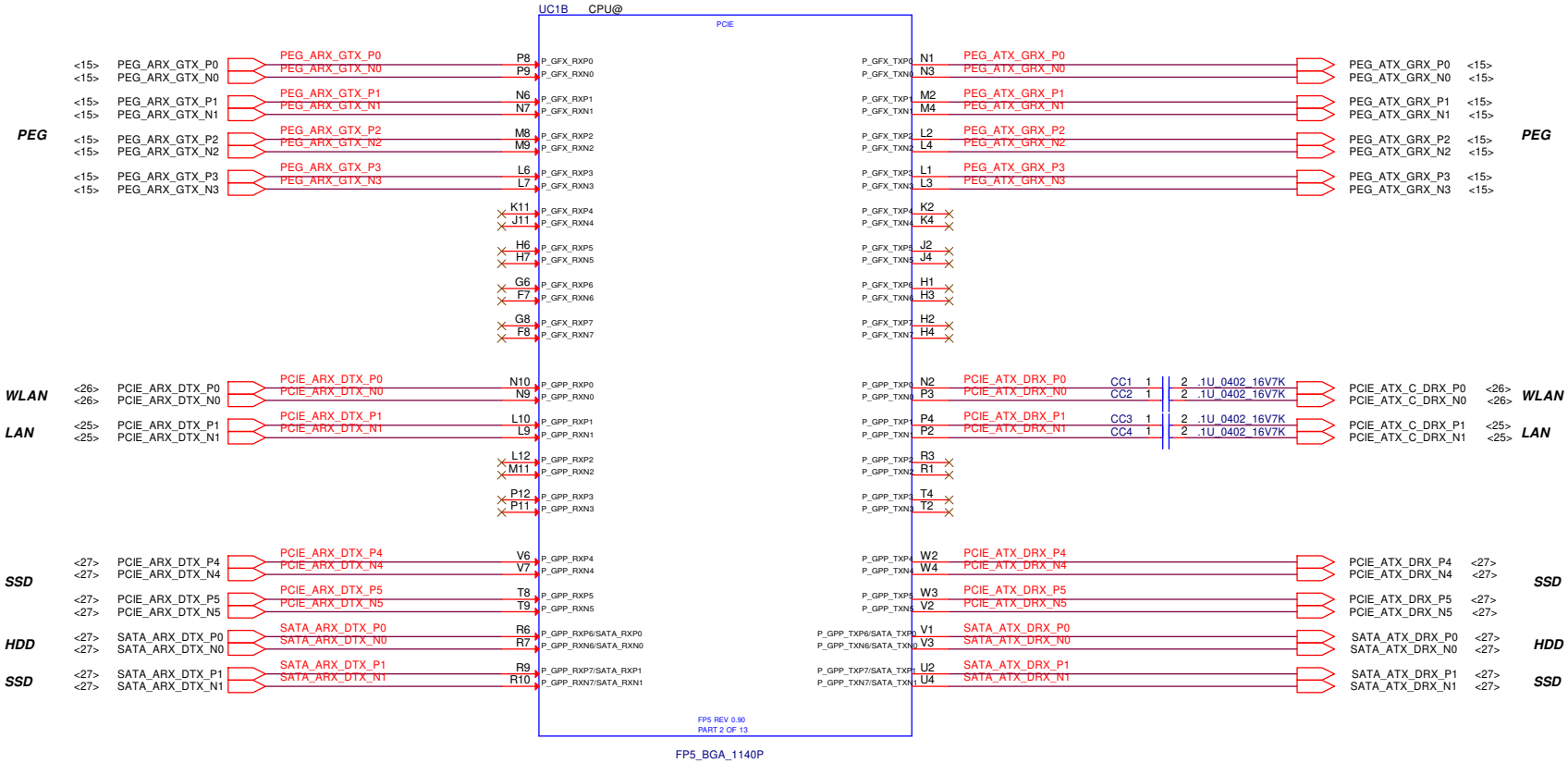
Main Func = CPU



APU PN Table

APU Platform	Customer PN	Customer PN	Customer PN	Customer PN	Customer PN	Compal PN
Picasso	UC1 R3APUDC@ S IC RYZEN3 YM3200C4T2OFG 2.6G BGA APU SA0000CCS20	UC1 R3APUQC@ S IC RYZEN3 YM3300C4T4MFG 2.1G BGA 1140 APU SA0000CCV10	UC1 R5APUQC@ S IC RYZEN5 YM3500C4T4MFG 2.1G BGA APU SA0000CCR20	UC1 R7APUQC@ S IC RYZEN7 YM3700C4T4MFG 2.3G BGA APU SA0000C7640	UC1 Athlon@ S IC ATHLON YM300UC4T2OFG 2.4G APU ABO! SA0000CFE40	

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Title: FP5_(1/7)_PEG/PCIE/SATA

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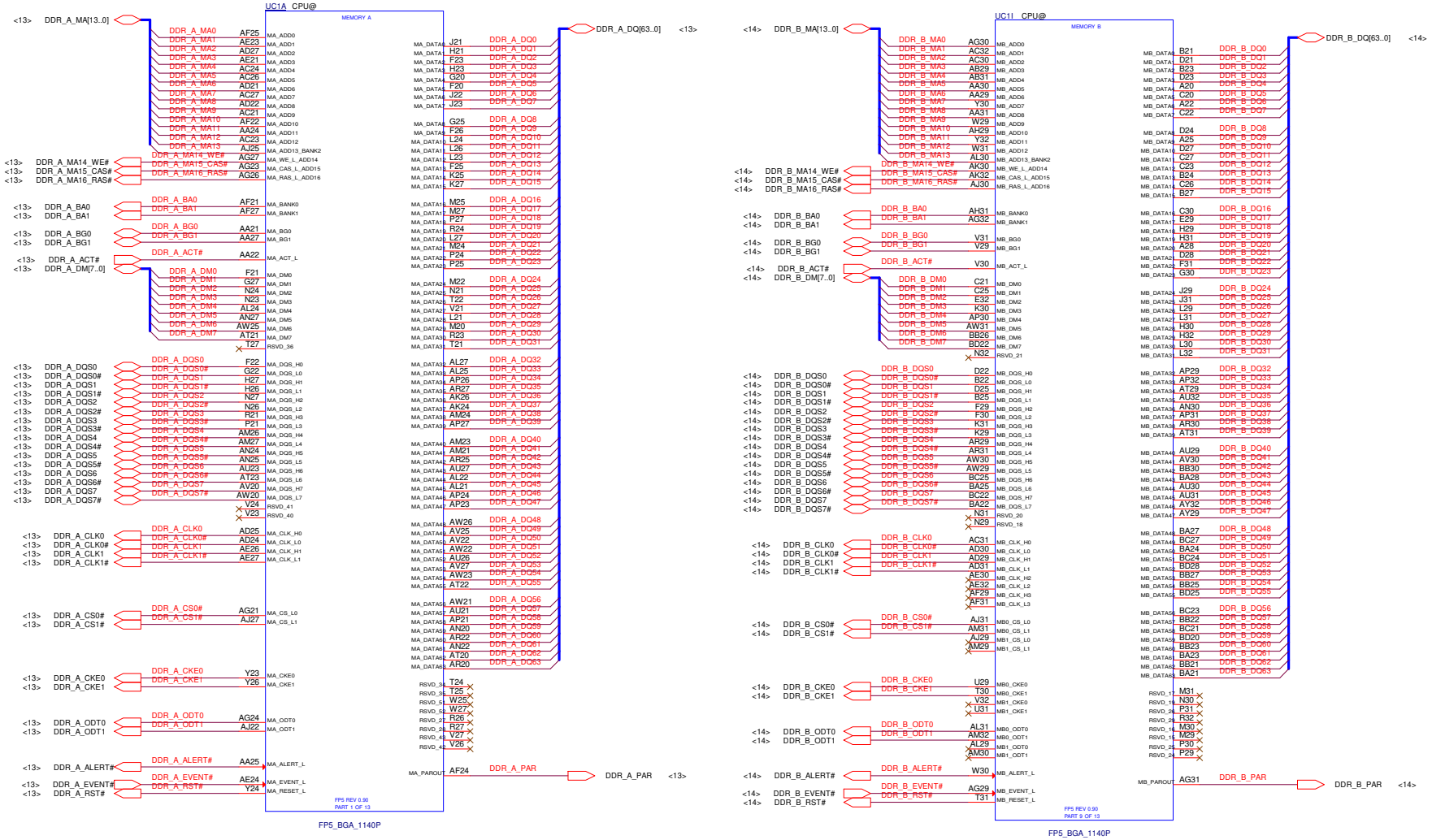
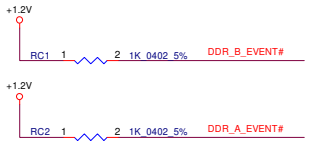
Main Func = CPU



EVENT# pull high



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Title: FP5_(2/7)_DDR4

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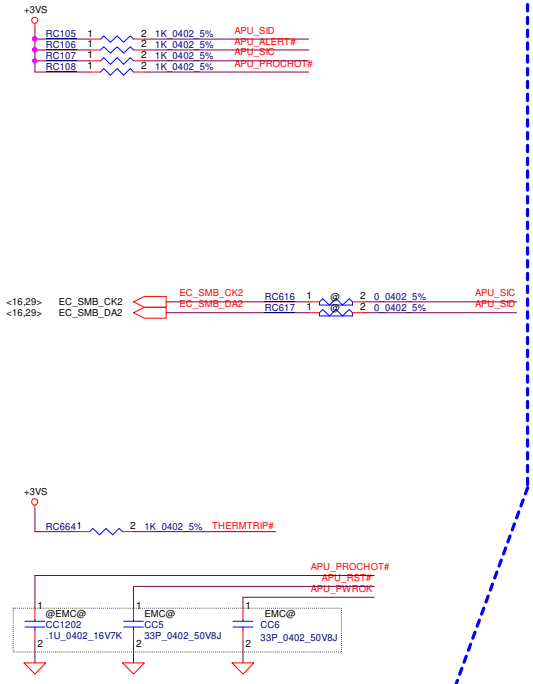
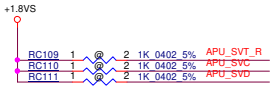
Main Func = CPU

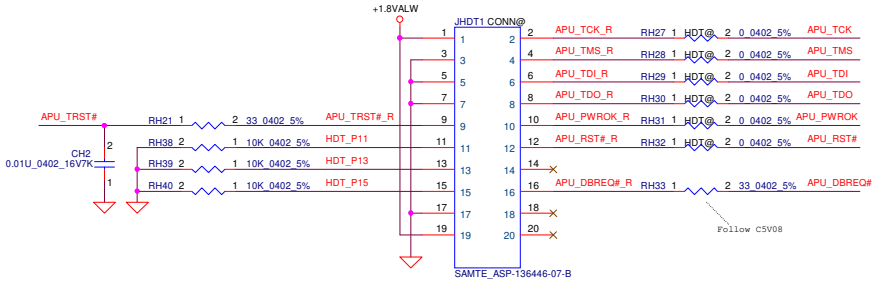
EC/THERM

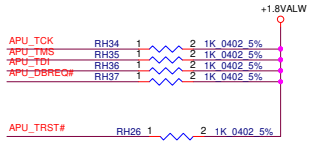


SVID

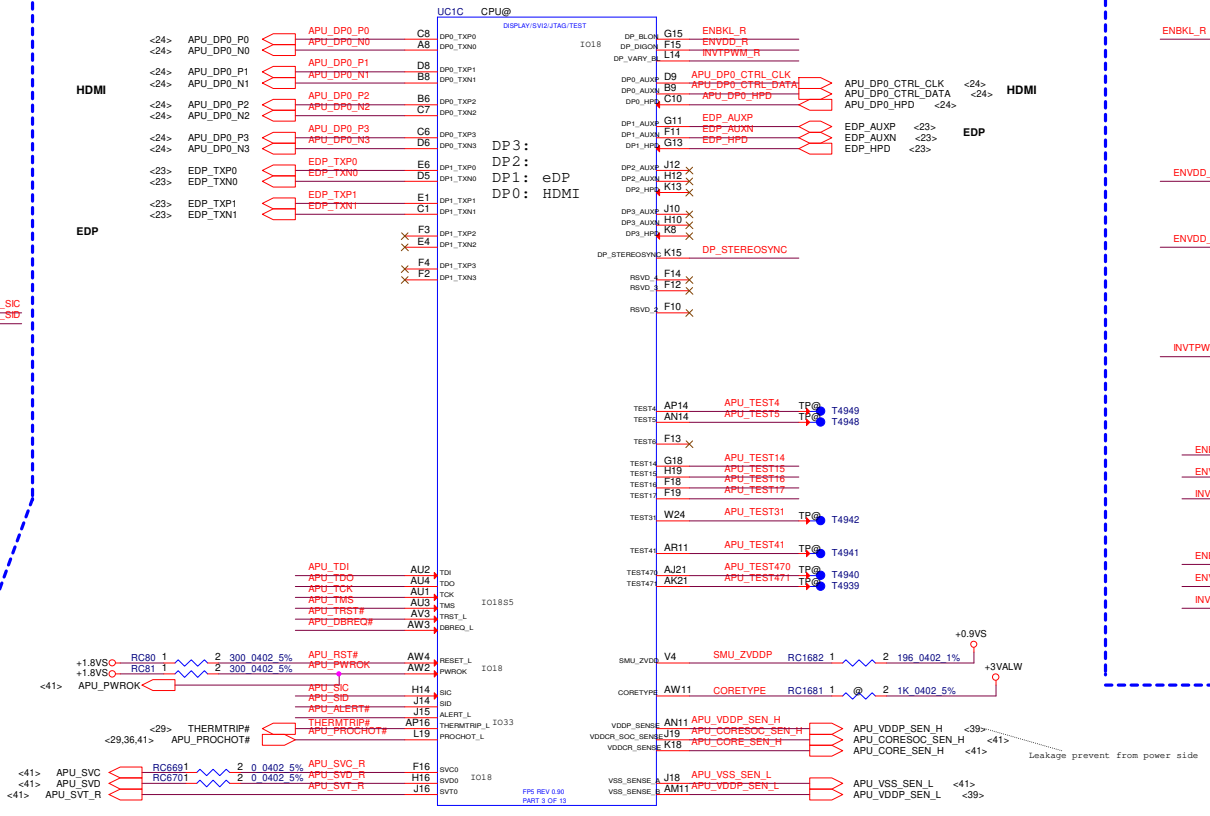


HDT+



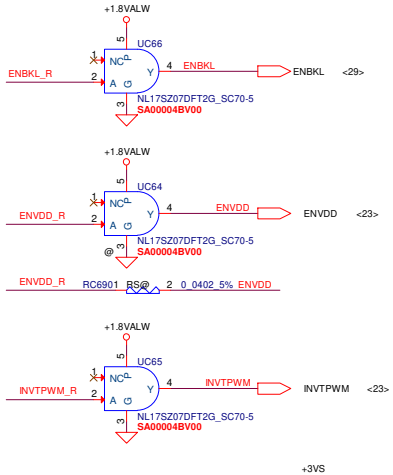


UC1C CPU@

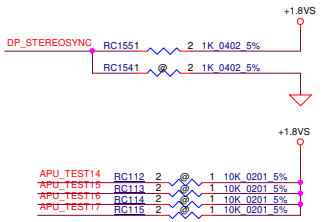


FP5_BGA_1140P

DISP



TESTPOINT



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Title: (3/7)_DISP/MISC/HDT

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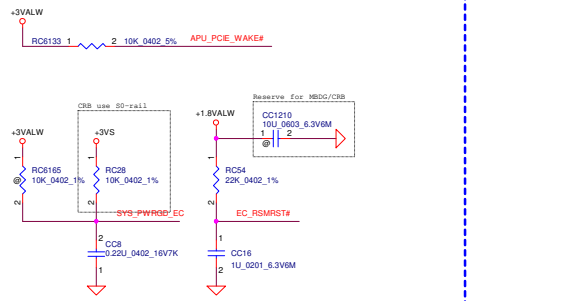
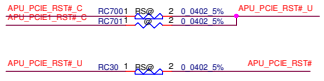
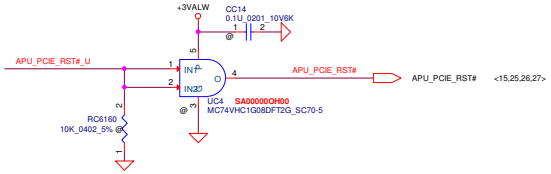
Main Func = CPU

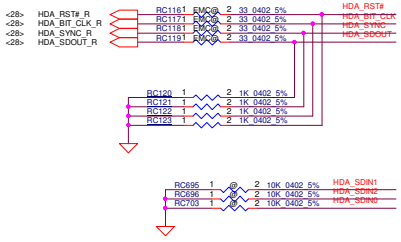
ACPI

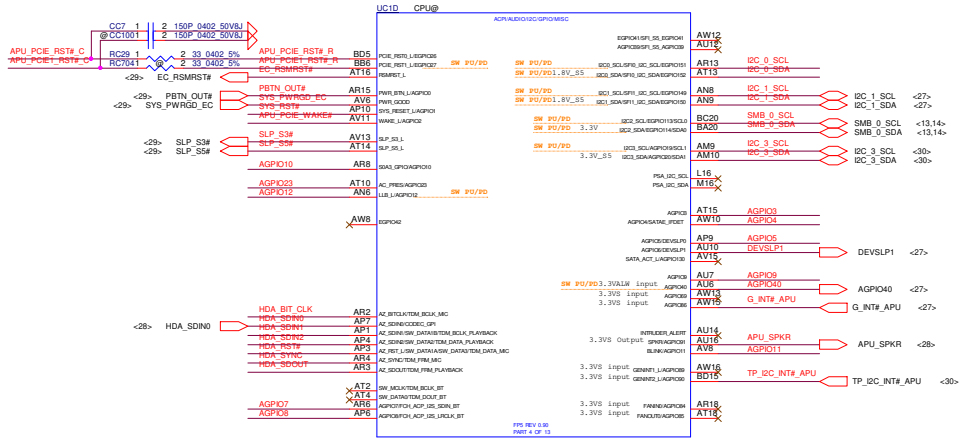


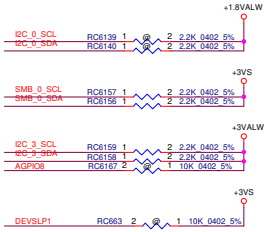




HDA

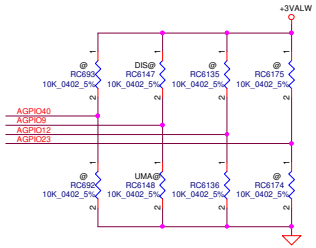






GPIO Table

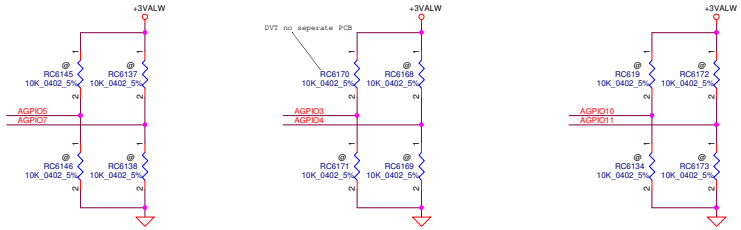
	AGPIO40	AGPIO9	AGPIO12	AGPIO23
H	PCIE RST SSD	DIS	RSV	RSV
L		UMA	RSV	RSV



AGPIO5	AGPIO7	

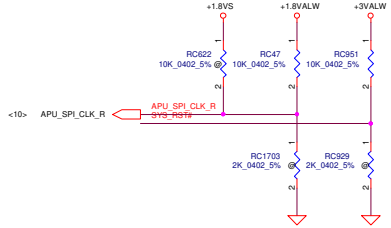
	AGPIO3	AGPIO4
H		
L		

AGPIO10	AGPIO11	



Strap Pin

	APU_SPI_CLK_R	SYS_RST#
H	USE 48MHZ CRYSTAL CLOCK (Default)	NORMAL RESET MODE (Default)
L	USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK	SHORT RESET MODE



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Title: FP5_(4/7)_GPIO/HDA/STRAP

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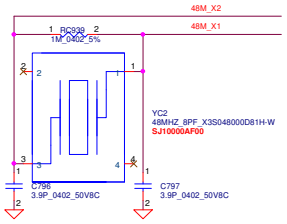
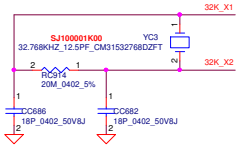
Main Func = CPU

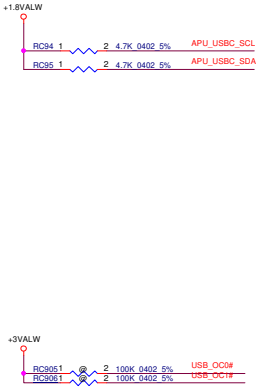
48MHz CRYSTAL

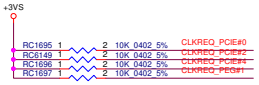


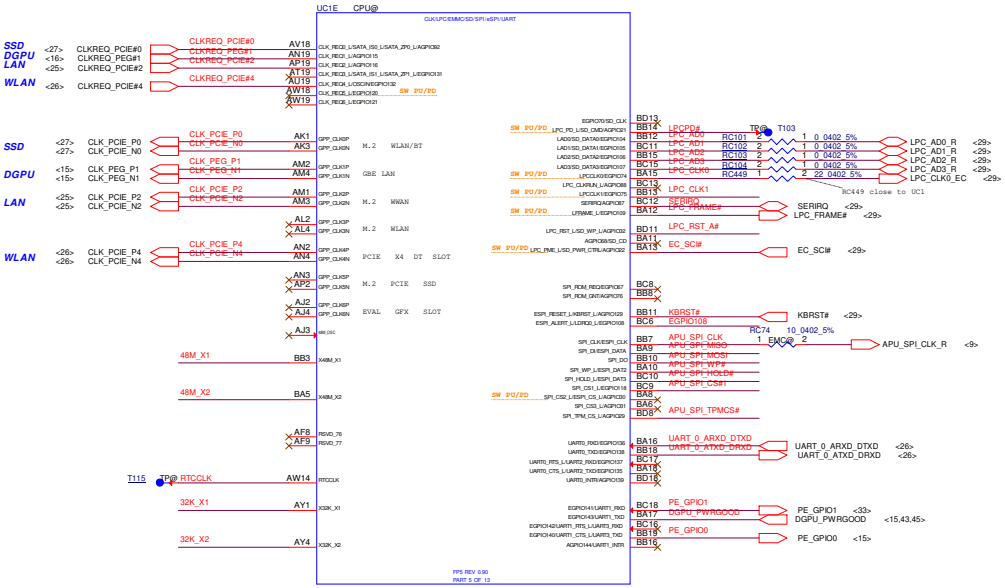
32.768KHz CRYSTAL

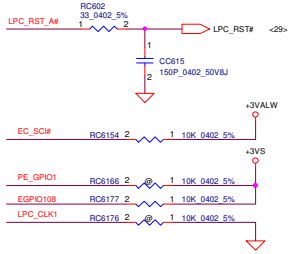


USB Function

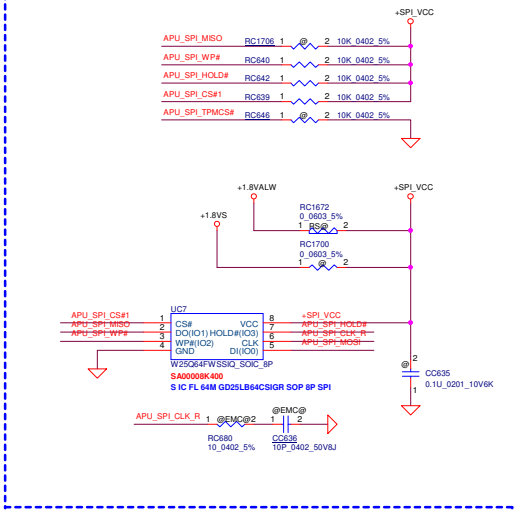


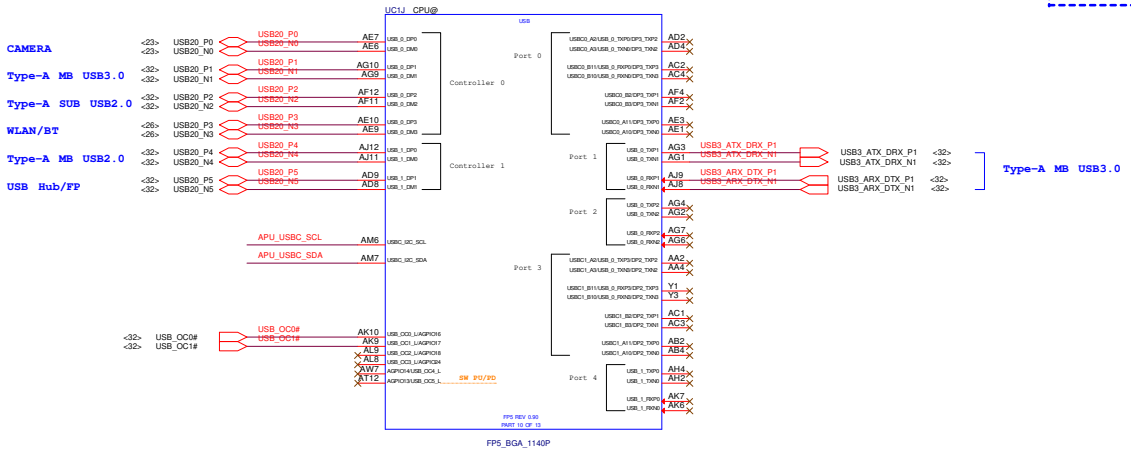






8MB SPI ROM





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Issued Date	2020/03/29	Deciphered Date 2020/03/29	Title: FP5_(5/7)_CLK/USB/SPI/LPC
			Size: Custom; Document Number: EH5LP/AP_LA-H801P; Rev: 1A
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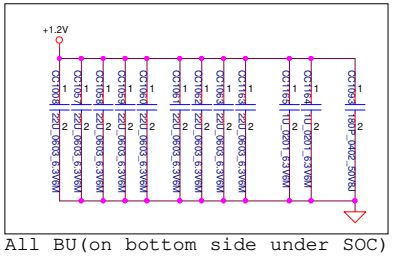
Main Func = CPU

+APU_CORE_SOC Cap
place at Power Side

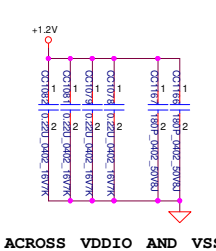
SCL/MBDG:
7*22uF (BU)
1*1uF (BU)
1*180pF (BU)

+APU_CORE Cap place at Power Side

SCL/MBDG:
16*22uF (BU)
1*180pF (BU)

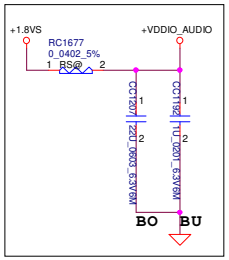


All BU(on bottom side under SOC)

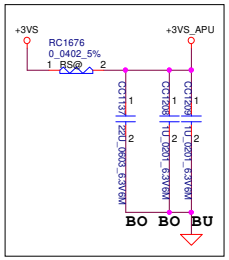


SCL/MBDG:
9*22uF (BU)
2*1uF (BU)
4*0.22uF
1*180pF (BU)
2*180pF

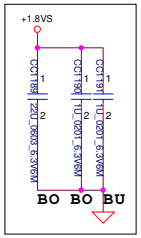
ACROSS VDDIO AND VSS SPLIT



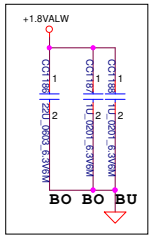
SCL/MBDG:
1 *22uF (BO)
1*1uF (BU)



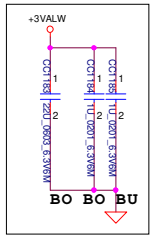
SCL/MBDG:
1 *22uF (BO)
2*1uF (BO+BU)



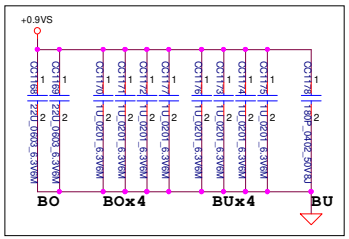
SCL/MBDG:
1 *22uF (BO)
2*1uF (BO+BU)



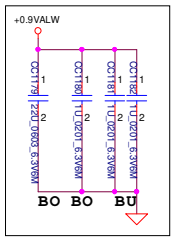
SCL/MBDG:
1 *22uF (BO)
2*1uF (BO+BU)



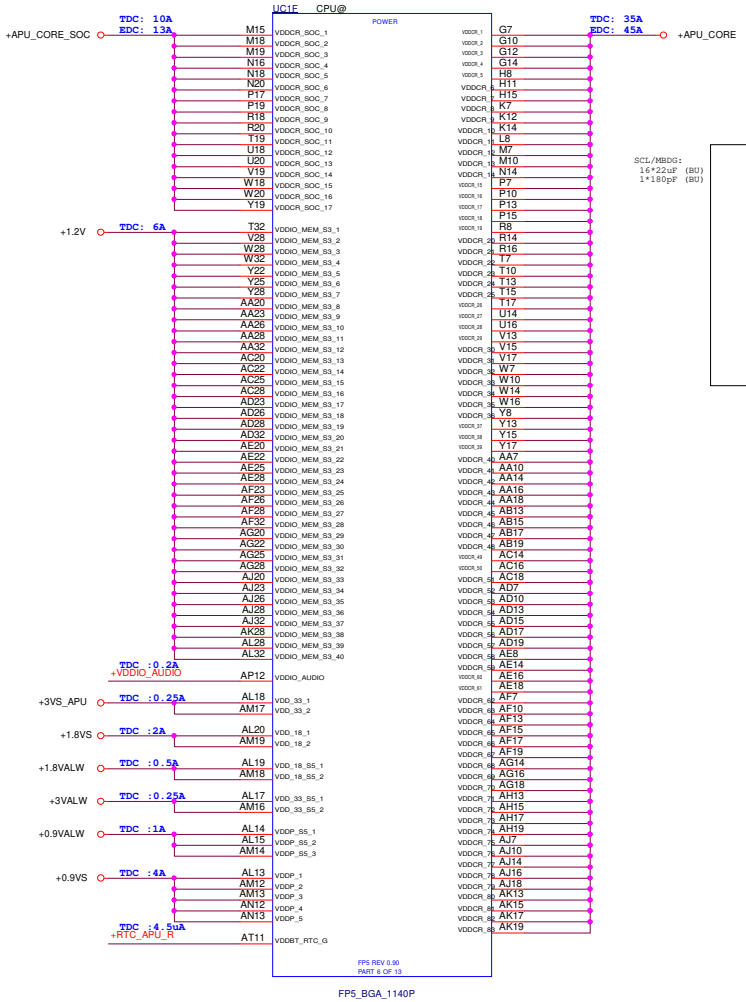
SCL/MBDG:
1 *22uF (BO)
2*1uF (BO+BU)



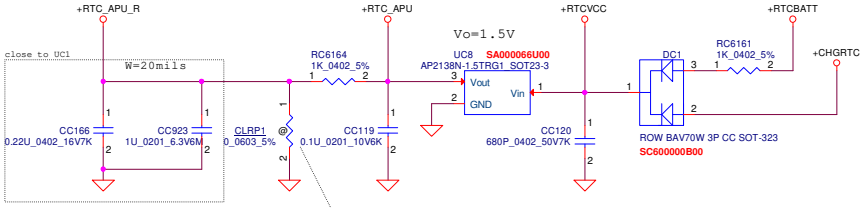
SCL/MBDG:
2 *22uF (BO)
8*1uF (BOx4+BUx4)
1*180pF (BU)

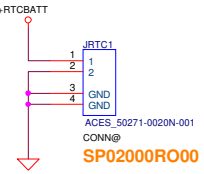


SCL/MBDG:
1 *22uF (BO)
3*1uF (BOx1+BUx2)



RTC OF APU





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Security Classification	Compal Secret Data		
Issued Date	2020/03/29	Deciphered Date	2020/03/29

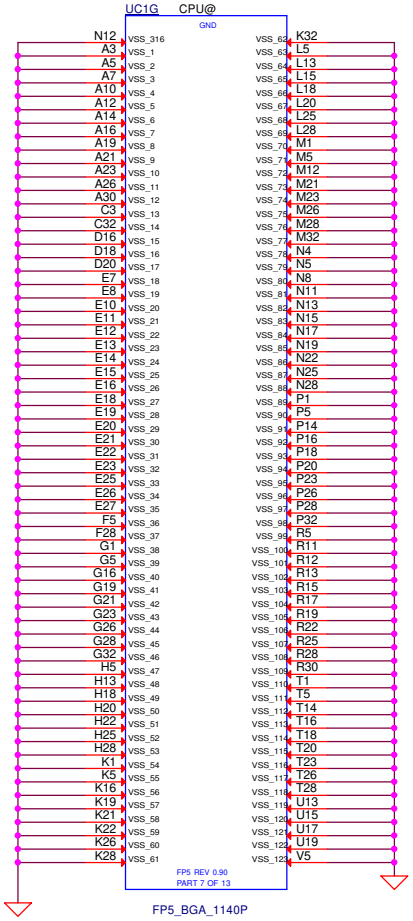
Compal Electronics, Inc.

Title: (6/7)_PWR

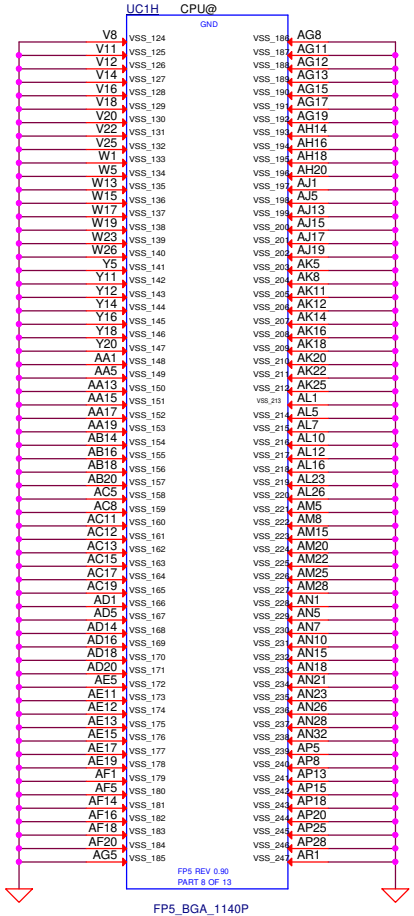
Size: Custom | Document Number: EH5LP/AP_LA-H801P | Rev: 1.A

Date: Friday, March 29, 2019 | Sheet 11 of 48

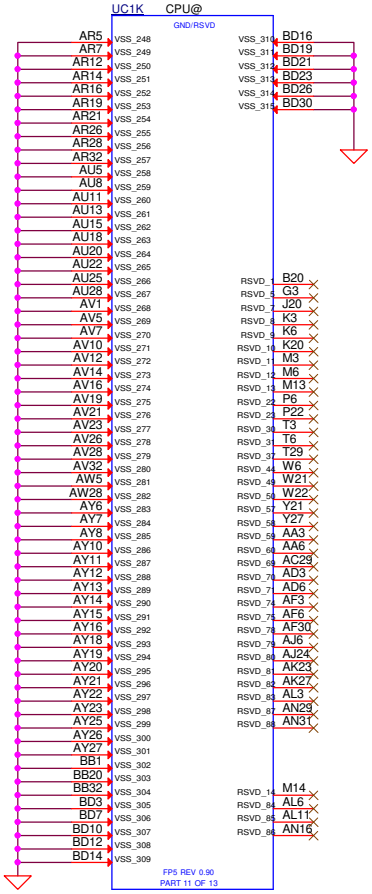
Main Func = CPU



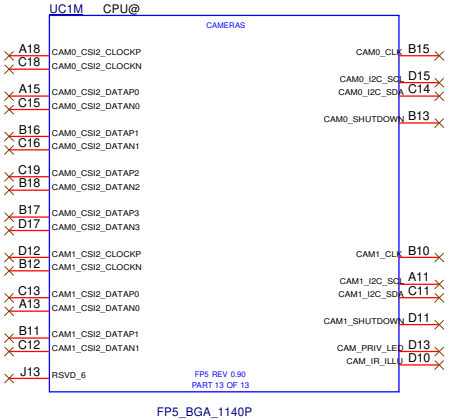
FP5_BGA_1140P



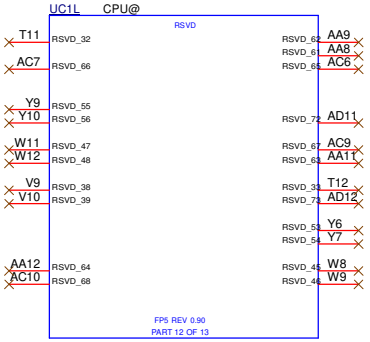
FP5_BGA_1140P



FP5_BGA_1140P



FP5_BGA_1140P



FP5_BGA_1140P

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Security Classification	Compal Secret Data		
Issued Date	2020/03/29	Deciphered Date	2020/03/29

Compal Electronics, Inc.

Title: FP5_(7/7)_GND/RSVD/CSI

Size	Document Number	Rev
Custom	EH5LP/AP_LA-H801P	1.A

Date: Friday, March 29, 2019 Sheet 12 of 48

Reverse Type

2-3A to 1 DIMMs/channel

Address : A0

+3VS

RD5 0_0402_5%@ RD6 0_0402_5%@ RD7 0_0402_5%@

DDR_A_SA2
DDR_A_SA1
DDR_A_SA0

RD8 0_0402_5%@ RD9 0_0402_5%@ RD10 0_0402_5%@

CD1 @EMC@ 1U_0402_16V7K

DDR_A_RST#

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

DDR4 support Even Parity check in DRAMs.

CRB use 0.1uF x12 (6 pop,6 unpop),180pF x1,100uF x2

+1.2V

CD2 CD3 CD4 CD5 CD6 CD7 1U_0201_6.3V6M

+1.2V

CD10 CD11 CD12 CD13 CD14 CD15 10U_0603_6.3V6M

Follow MA51

@ CD18 330U_D2_2V_Y

SGA00009S00
330U 2V H1.9
9mohm POLY

+1.2V

CD61 CD62 CD63 CD64 0.1U_0201_10V6K

CD65 180P_0402_50V8J

Layout Note:
Place near JDIMM1.257,259

CRB use 0.1uF x2,180pF x1

+2.5V

CD23 CD24 1U_0201_6.3V6M

Layout Note:
Place near JDIMM1.255

CRB use 1uF x1

+3VS

CD26 1U_0201_6.3V6M

JDIMM1A

REVERSE

<7> DDR_A_CLK0	DDR_A_CLK0	137	CK0(T)	DQ0	8 DDR_A_DQ0
<7> DDR_A_CLK0#	DDR_A_CLK0#	139	CK0#(C)	DQ1	7 DDR_A_DQ1
<7> DDR_A_CLK1	DDR_A_CLK1	138	CK1(T)	DQ2	20 DDR_A_DQ2
<7> DDR_A_CLK1#	DDR_A_CLK1#	140	CK1#(C)	DQ3	21 DDR_A_DQ3
				DQ4	4 DDR_A_DQ4
<7> DDR_A_CKE0	DDR_A_CKE0	109	CKE0	DQ5	3 DDR_A_DQ5
<7> DDR_A_CKE1	DDR_A_CKE1	110	CKE1	DQ6	16 DDR_A_DQ6
				DQ7	17 DDR_A_DQ7
<7> DDR_A_CS0#	DDR_A_CS0#	149	S0#	DQS0(T)	13 DDR_A_DQS0
<7> DDR_A_CS1#	DDR_A_CS1#	157	S1#	DQS0#(C)	11 DDR_A_DQS0#
		162	S2#/C0		
		165	S3#/C1		
				DQ8	28 DDR_A_DQ8
<7> DDR_A_ODT0	DDR_A_ODT0	155	ODT0	DQ9	29 DDR_A_DQ9
<7> DDR_A_ODT1	DDR_A_ODT1	161	ODT1	DQ10	41 DDR_A_DQ10
				DQ11	42 DDR_A_DQ11
<7> DDR_A_BG0	DDR_A_BG0	115	BG0	DQ12	24 DDR_A_DQ12
<7> DDR_A_BG1	DDR_A_BG1	113	BG1	DQ13	25 DDR_A_DQ13
<7> DDR_A_BA0	DDR_A_BA0	150	BA0	DQ14	38 DDR_A_DQ14
<7> DDR_A_BA1	DDR_A_BA1	145	BA1	DQ15	37 DDR_A_DQ15
				DQS1(T)	34 DDR_A_DQS1
<7> DDR_A_MA[13..0]	DDR_A_MA0	144	A0	DQS1#(C)	32 DDR_A_DQS1#
	DDR_A_MA1	133	A1		
	DDR_A_MA2	132	A2	DQ16	50 DDR_A_DQ16
	DDR_A_MA3	131	A3	DQ17	49 DDR_A_DQ17
	DDR_A_MA4	128	A4	DQ18	62 DDR_A_DQ18
	DDR_A_MA5	126	A5	DQ19	63 DDR_A_DQ19
	DDR_A_MA6	127	A6	DQ20	46 DDR_A_DQ20
	DDR_A_MA7	122	A7	DQ21	45 DDR_A_DQ21
	DDR_A_MA8	125	A8	DQ22	58 DDR_A_DQ22
	DDR_A_MA9	121	A9	DQ23	59 DDR_A_DQ23
	DDR_A_MA10	146	A10_AP	DQS2(T)	55 DDR_A_DQS2
	DDR_A_MA11	120	A11	DQS2#(C)	53 DDR_A_DQS2#
	DDR_A_MA12	119	A12		
	DDR_A_MA13	158	A13	DQ24	70 DDR_A_DQ24
<7> DDR_A_MA14_WE#	DDR_A_MA14_WE#	151	A14_WE#	DQ25	71 DDR_A_DQ25
<7> DDR_A_MA15_CAS#	DDR_A_MA15_CAS#	156	A15_CAS#	DQ26	83 DDR_A_DQ26
<7> DDR_A_MA16_RAS#	DDR_A_MA16_RAS#	152	A16_RAS#	DQ27	84 DDR_A_DQ27
				DQ28	66 DDR_A_DQ28
<7> DDR_A_ACT#	DDR_A_ACT#	114	ACT#	DQ29	67 DDR_A_DQ29
				DQ30	79 DDR_A_DQ30
<7> DDR_A_PAR	DDR_A_PAR	143	PARITY	DQ31	80 DDR_A_DQ31
<7> DDR_A_ALERT#	DDR_A_ALERT#	116	ALERT#	DQS3(T)	76 DDR_A_DQS3
<7> DDR_A_EVENT#	DDR_A_EVENT#	134	EVENT#	DQS3#(C)	74 DDR_A_DQS3#
<7> DDR_A_RST#	DDR_A_RST#	108	RESET#		
				DQ32	174 DDR_A_DQ32
				DQ33	173 DDR_A_DQ33
				DQ34	187 DDR_A_DQ34
				DQ35	186 DDR_A_DQ35
<9,14> SMB_0_SDA	SMB_0_SDA	254	SDA	DQ36	170 DDR_A_DQ36
<9,14> SMB_0_SCL	SMB_0_SCL	253	SCL	DQ37	169 DDR_A_DQ37
				DQ38	183 DDR_A_DQ38
	DDR_A_SA2	166	SA2	DQ39	182 DDR_A_DQ39
	DDR_A_SA1	260	SA1	DQS4(T)	179 DDR_A_DQS4
	DDR_A_SA0	256	SA0	DQS4#(C)	177 DDR_A_DQS4#
		92	CB0_NC	DQ40	195 DDR_A_DQ40
		91	CB1_NC	DQ41	194 DDR_A_DQ41
		101	CB2_NC	DQ42	207 DDR_A_DQ42
		105	CB3_NC	DQ43	208 DDR_A_DQ43
		88	CB4_NC	DQ44	191 DDR_A_DQ44
		87	CB5_NC	DQ45	190 DDR_A_DQ45
		100	CB6_NC	DQ46	203 DDR_A_DQ46
		104	CB7_NC	DQ47	204 DDR_A_DQ47
		97	DQS8(T)	DQS5(T)	200 DDR_A_DQS5
		95	DQS8#(C)	DQS5#(C)	198 DDR_A_DQS5#
<7> DDR_A_DM[7..0]	DDR_A_DM0	12	DM0#/DBI0#	DQ48	216 DDR_A_DQ48
	DDR_A_DM1	33	DM1#/DBI1#	DQ49	215 DDR_A_DQ49
	DDR_A_DM2	54	DM2#/DBI2#	DQ50	228 DDR_A_DQ50
	DDR_A_DM3	75	DM3#/DBI3#	DQ51	229 DDR_A_DQ51
	DDR_A_DM4	178	DM4#/DBI4#	DQ52	211 DDR_A_DQ52
	DDR_A_DM5	199	DM5#/DBI5#	DQ53	212 DDR_A_DQ53
	DDR_A_DM6	220	DM6#/DBI6#	DQ54	224 DDR_A_DQ54
	DDR_A_DM7	241	DM7#/DBI7#	DQ55	225 DDR_A_DQ55
		96	DM8#/DBI8#	DQS6(T)	221 DDR_A_DQS6
				DQS6#(C)	219 DDR_A_DQS6#
			DQ56		237 DDR_A_DQ56
			DQ57		236 DDR_A_DQ57
			DQ58		249 DDR_A_DQ58
			DQ59		250 DDR_A_DQ59
			DQ60		232 DDR_A_DQ60
			DQ61		233 DDR_A_DQ61
			DQ62		245 DDR_A_DQ62
			DQ63		246 DDR_A_DQ63
			DQS7(T)		242 DDR_A_DQS7
			DQS7#(C)		240 DDR_A_DQS7#

DEREN_40-42271-26001RHF

CONN@

SP07001CW00

<7> DDR_A_DQ[7..0]
<7> DDR_A_DQS0 / DDR_A_DQS0# / DDR_A_DQ[15..8]
<7> DDR_A_DQS1 / DDR_A_DQS1# / DDR_A_DQ[23..16]
<7> DDR_A_DQS2 / DDR_A_DQS2# / DDR_A_DQ[31..24]
<7> DDR_A_DQS3 / DDR_A_DQS3# / DDR_A_DQ[39..32]
<7> DDR_A_DQS4 / DDR_A_DQS4# / DDR_A_DQ[47..40]
<7> DDR_A_DQS5 / DDR_A_DQS5# / DDR_A_DQ[55..48]
<7> DDR_A_DQS6 / DDR_A_DQS6# / DDR_A_DQ[63..56]
<7> DDR_A_DQS7 / DDR_A_DQS7#

Follow CRB design

+1.2V

RD3 1K_0402_1%

RD4 1K_0402_1%

15mil

CD20 4.7U_0402_6.3V6M CD22 0.1U_0201_10V6K

+VREFA_CA

CD21 0.1U_0201_10V6K CD19 1000P_0402_50V7K

Place near to SO-DIMM connector.

+1.2V

JDIMM1B

REVERSE

111	VDD1	VDD11	141
112	VDD2	VDD12	142
117	VDD3	VDD13	147
118	VDD4	VDD14	148
123	VDD5	VDD15	153
124	VDD6	VDD16	154
129	VDD7	VDD17	159
130	VDD8	VDD18	160
135	VDD9	VDD19	163
136	VDD10		
255	VDDSPD	VTT	258
164	VREFCA	VPP1	257
		VPP2	259
1	VSS	VSS	99
2	VSS	VSS	102
5	VSS	VSS	103
6	VSS	VSS	106
9	VSS	VSS	107
10	VSS	VSS	167
14	VSS	VSS	168
15	VSS	VSS	171
18	VSS	VSS	172
19	VSS	VSS	175
22	VSS	VSS	176
23	VSS	VSS	180
26	VSS	VSS	181
27	VSS	VSS	184
30	VSS	VSS	185
31	VSS	VSS	188
35	VSS	VSS	189
36	VSS	VSS	192
39	VSS	VSS	193
40	VSS	VSS	196
43	VSS	VSS	197
44	VSS	VSS	201
47	VSS	VSS	202
48	VSS	VSS	205
51	VSS	VSS	206
52	VSS	VSS	209
56	VSS	VSS	210
57	VSS	VSS	213
60	VSS	VSS	214
61	VSS	VSS	217
64	VSS	VSS	218
65	VSS	VSS	222
68	VSS	VSS	223
69	VSS	VSS	226
72	VSS	VSS	227
73	VSS	VSS	230
77	VSS	VSS	231
78	VSS	VSS	234
81	VSS	VSS	235
82	VSS	VSS	238
85	VSS	VSS	239
86	VSS	VSS	243
89	VSS	VSS	244
90	VSS	VSS	247
93	VSS	VSS	248
94	VSS	VSS	251
98	VSS	VSS	252
262	GND	GND	261

+3VS +0.6VS +2.5V

CD31 1U_0201_6.3V6M

CRB use 1uF x1

Layout Note:
Place near JDIMM1.258

CRB use 4.7uF x1,0.1uF x1

+0.6VS

CD27 CD28 CD29 CD30 1U_0201_6.3V6M

Security Classification	Compal Secret Data		
Issued Date	2020/03/29	Deciphered Date	2020/03/29

Compal Electronics, Inc.

Title: **DDR4 DIMMA**

Size	Document Number	Rev
Custom	EH5LP/AP_LA-H801P	1.A

Date: Friday, March 29, 2019 Sheet 13 of 48

Standard Type

2-3A to 1 DIMMs/channel

Address : A2

Layout Note:
Place near JDIMM2

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

Layout Note:
Place near JDIMM2.257,259

Layout Note:
Place near JDIMM2.255

Layout Note:
Place near JDIMM2.258

Follow CRB design

15mil

Place near to SO-DIMM connector.

JDIMM2A
STD
FOX_AS0A821-H4SB-7H
CONN@
SP07001HW00
Symbol follow EH5AW (Lada)

JDIMM2B
STD

CRB use 0.1uF x12 (6 pop,6 unpop),180pF x1,100uF x2

CRB use 0.1uF x2,180pF x1

CRB use 1uF x1

CRB use 4.7uF x1,0.1uF x1

CRB use 1uF x1

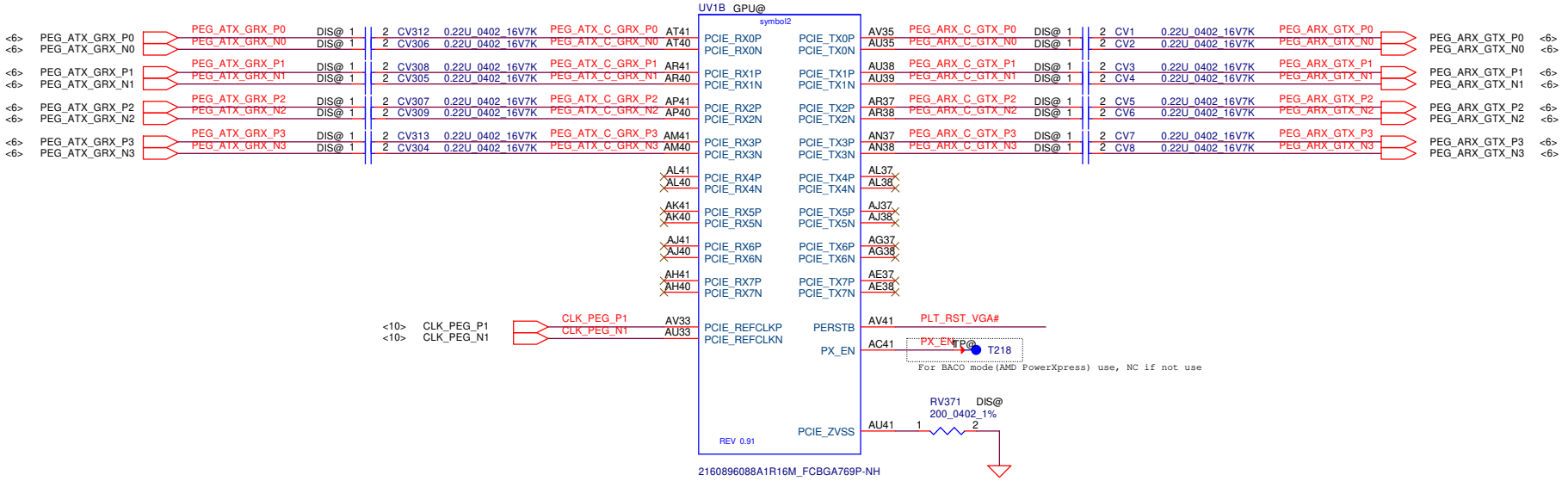
Security Classification	Compal Secret Data		
Issued Date	2020/03/29	Deciphered Date	2020/03/29

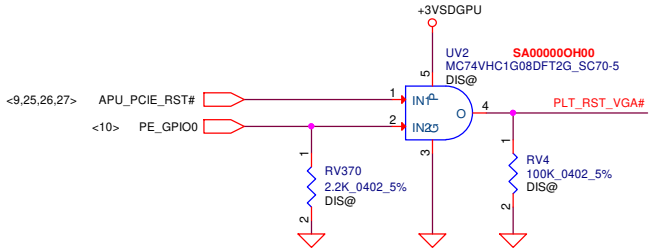
Compal Electronics, Inc.

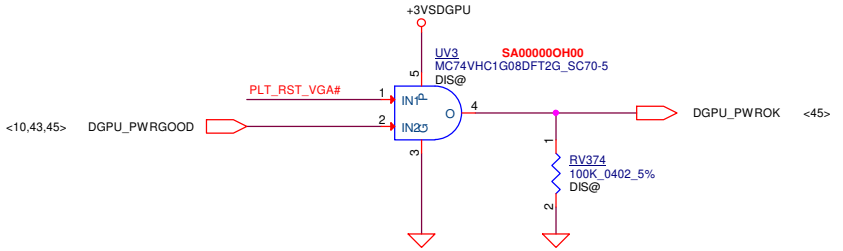
Title: DDR4 DIMMB

Size: Custom | Document Number: EH5LP/AP_LA-H801P | Rev: 1.A

Date: Friday, March 29, 2019 | Sheet 14 of 48







PLT_RST_VGA# RV1654 1 @ 2 0_0402_5% DGPU_PWROK

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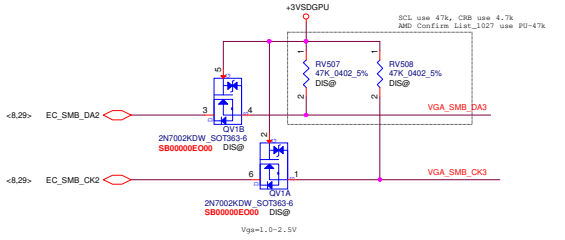
Security Classification	Compal Secret Data		
Issued Date	2020/03/29	Deciphered Date	2020/03/29

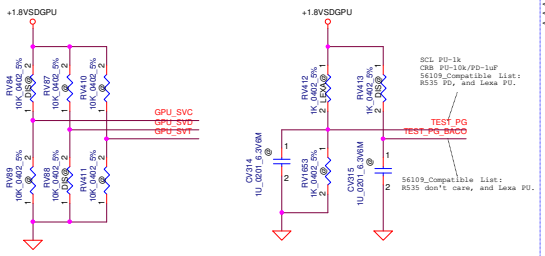
Compal Electronics, Inc.

Title: R19M-M18-70_(1/8)_PCIE

Size: Custom | Document Number: EH5LP/AP_LA-H801P | Rev: 1.A

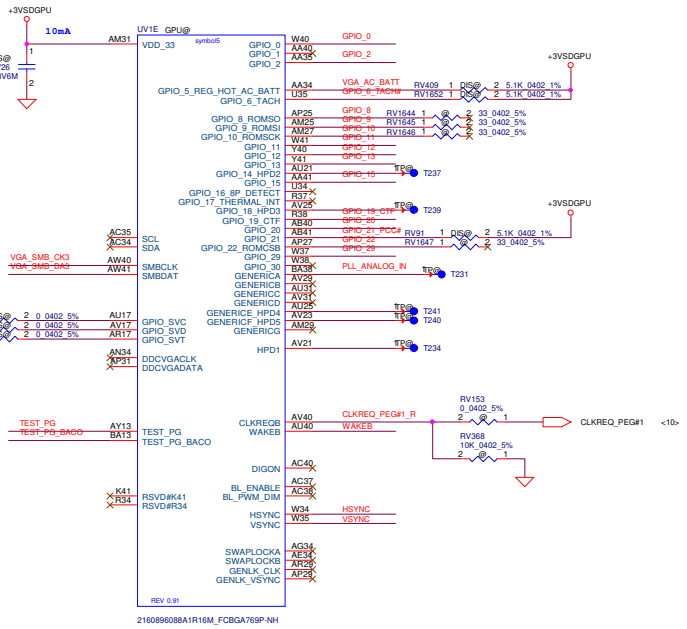
Date: Friday, March 29, 2019 | Sheet 15 of 48



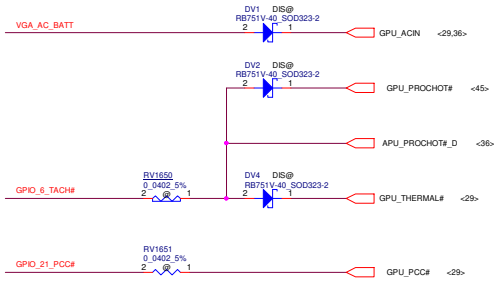


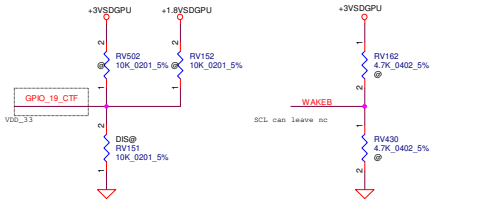
Boot-VID Code

SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



Function Support	Pin		R19M-M18-70
AC/DC Mode H:AC L:DC	GPIO5		Yes
Thermal VR_HOT# (Fan tachometer)	GPIO6		Yes
Peak Current Control	GPIO21		Yes





LEXA Strap

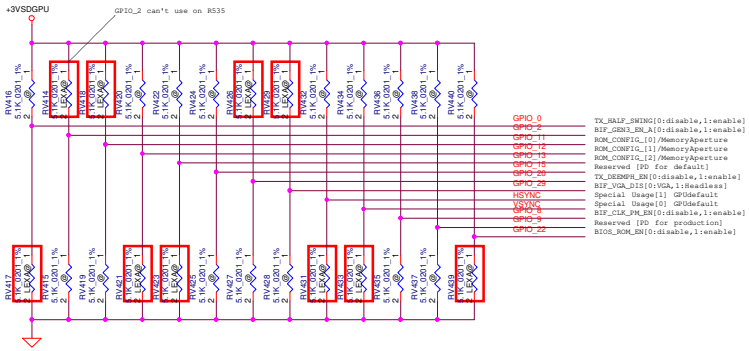


Table 3-27 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
8 GB	011
16 GB	100
1 GB	101
2 GB	110
4 GB	111

3.22.2 ROM Configurations

For designs that have a dedicated ROM device for the GPU video BIOS:

- Use the GPU default strap on GPIO_22_ROMCSB (i.e., 1).
- Use the GPU default straps on GPIO_13, GPIO_12, and GPIO_11 (i.e., 101).

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Title: R19M-M18-70_(2/8)_MSIC-1

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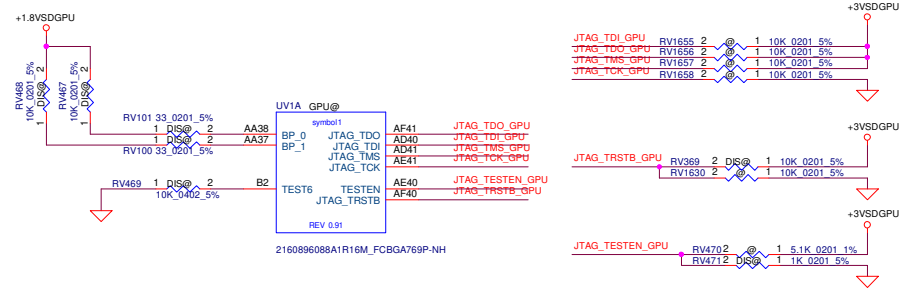

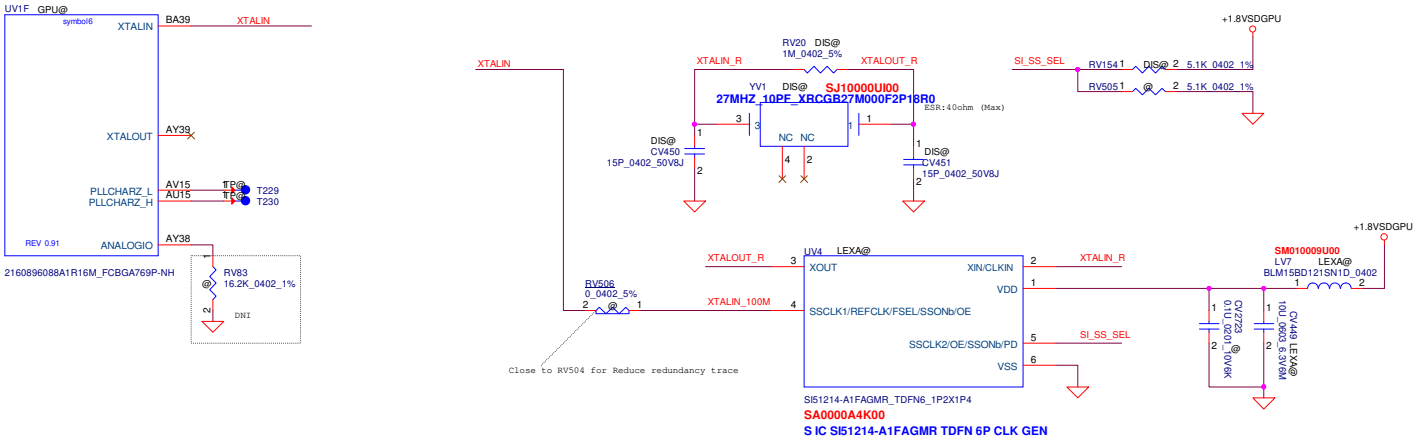

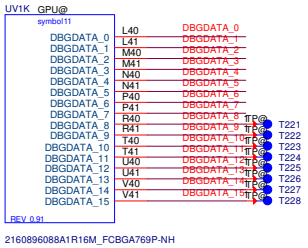

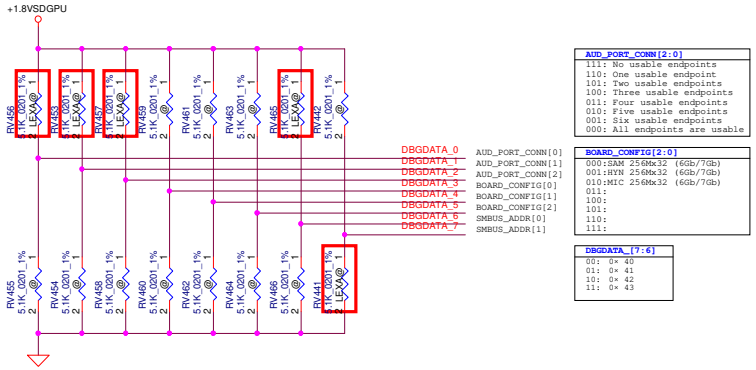

LEXA Memory ID

RV464 V4G_S@	RV462 V4G_S@	RV460 V4G_S@
S RES 1/20W 5.1K +-1% 0201 SD000008900	S RES 1/20W 5.1K +-1% 0201 SD000008900	S RES 1/20W 5.1K +-1% 0201 SD000008900
RV464 V4G_H@	RV462 V4G_H@	RV459 V4G_H@
S RES 1/20W 5.1K +-1% 0201 SD000008900	S RES 1/20W 5.1K +-1% 0201 SD000008900	S RES 1/20W 5.1K +-1% 0201 SD000008900
RV464 V4G_M@	RV461 V4G_M@	RV460 V4G_M@
S RES 1/20W 5.1K +-1% 0201 SD000008900	S RES 1/20W 5.1K +-1% 0201 SD000008900	S RES 1/20W 5.1K +-1% 0201 SD000008900

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Title: R19M-M18-70_(3/8)_MSIC-2

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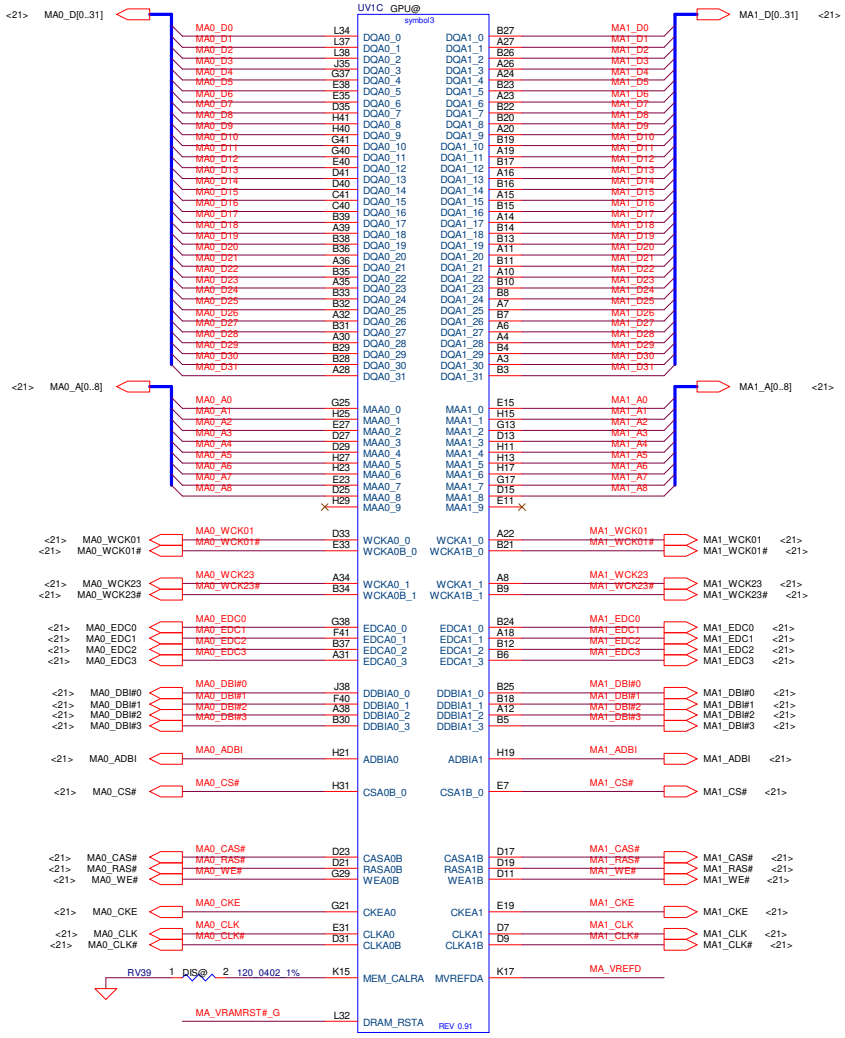

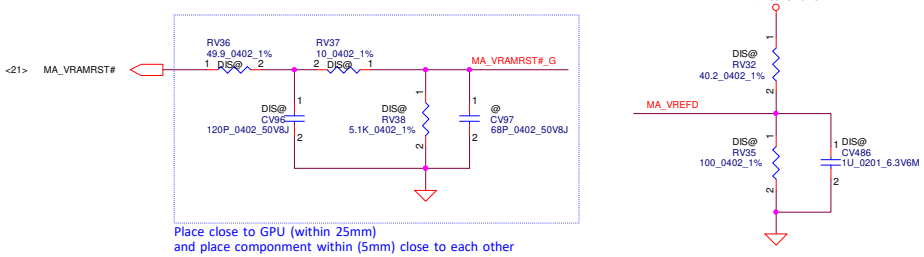

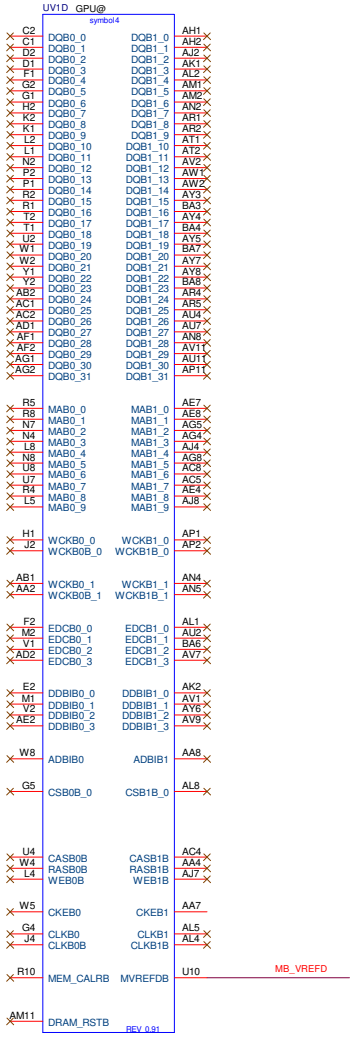

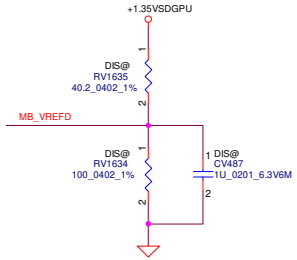

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Title: R19M-M18-70_(4/8)_MEM

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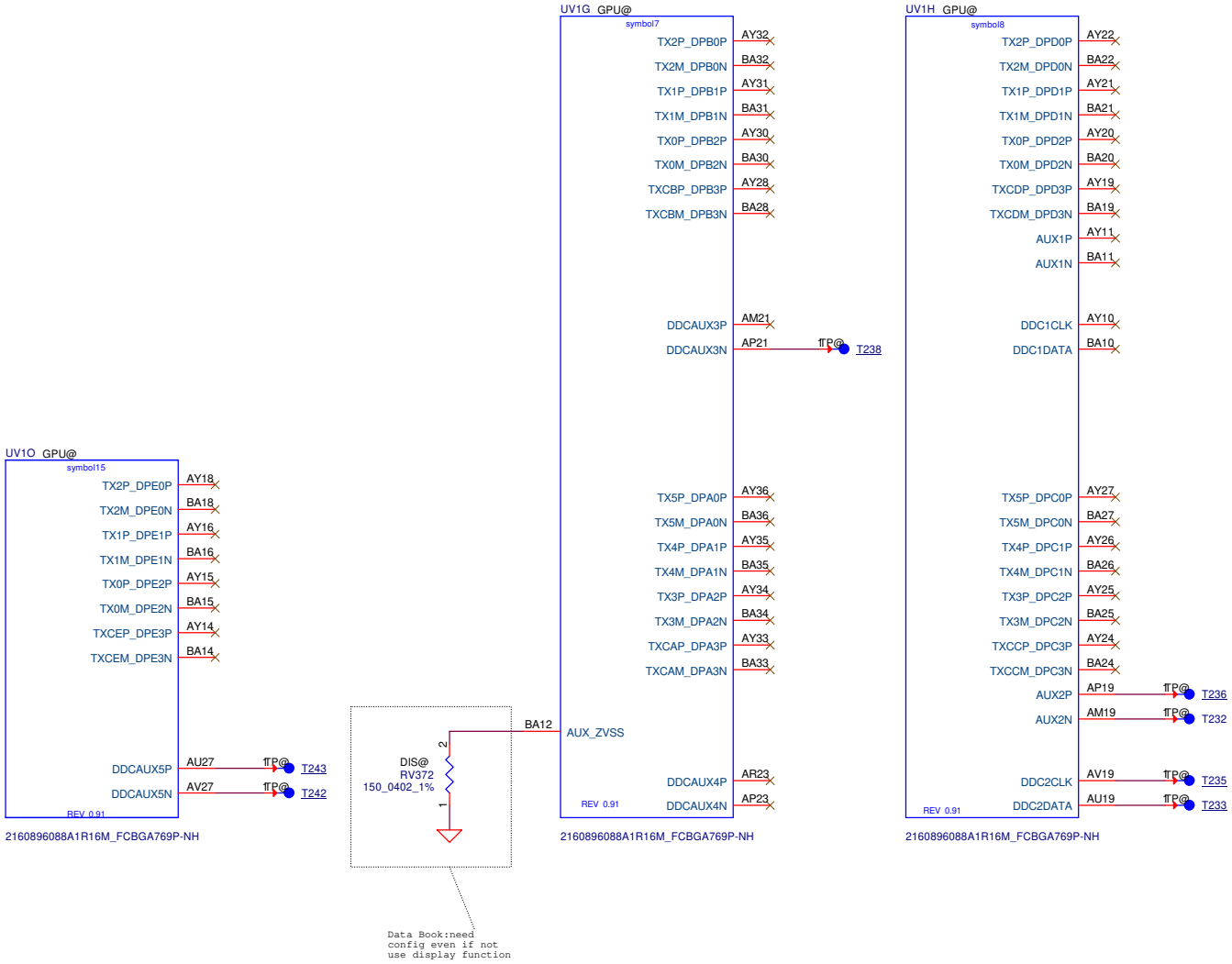

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Title: R19M-M18-70_(5/8)_DISP

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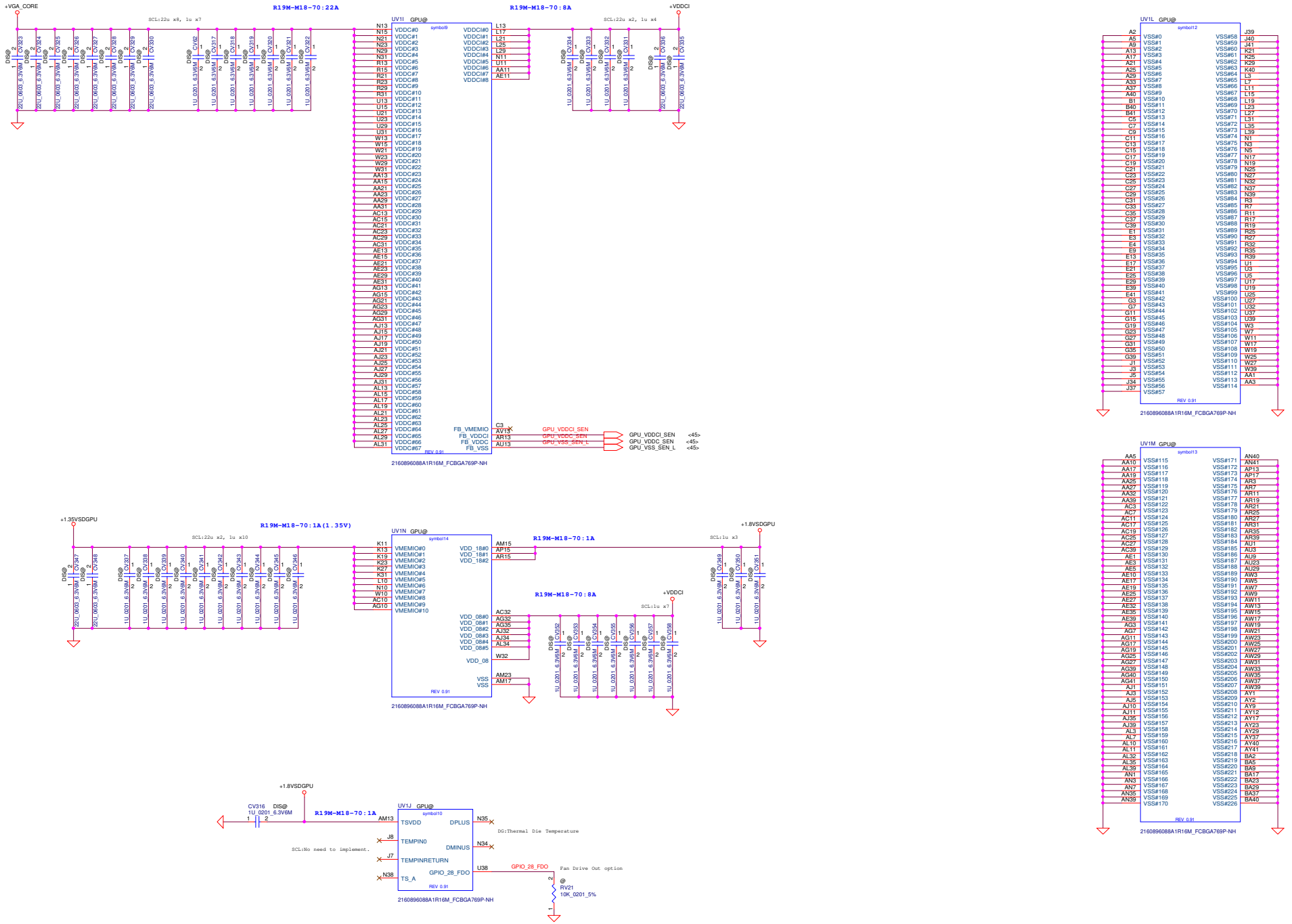

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Title: R19M-M18-70_(6/8)_PWR

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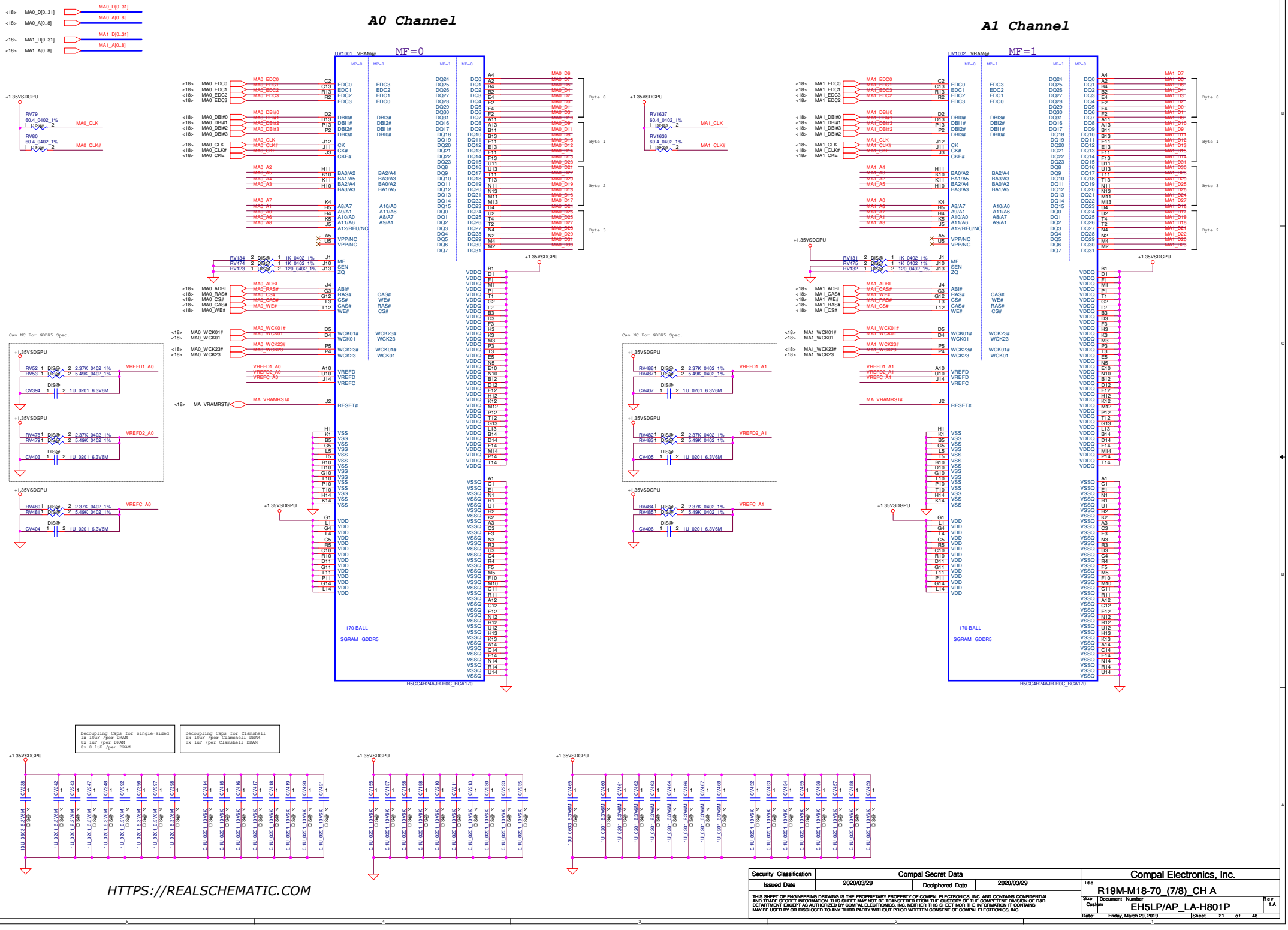
A0 Channel

A1 Channel



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Title: R19M-M18-70_(7/8)_CH A

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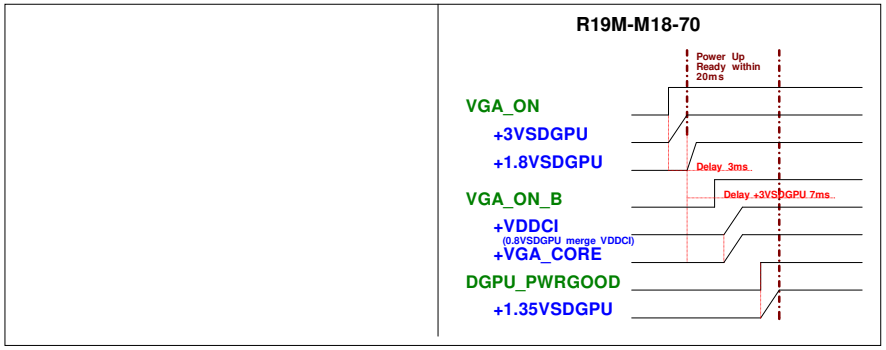
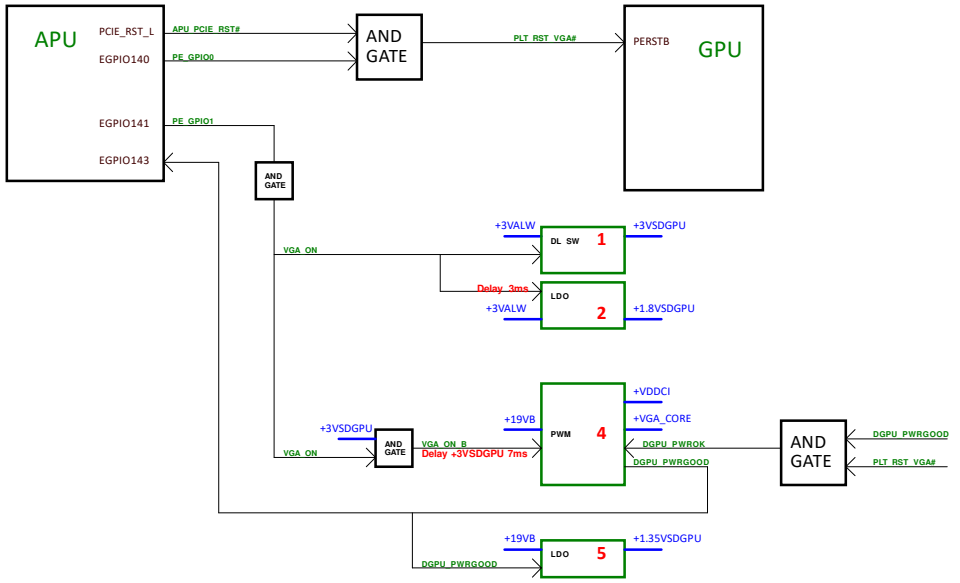
5.3 Power-up/down Sequence

"R19M-P25-50/R19M-P25-70/R19M-P18-50/R19M-M18-70" has the following requirements with regards to power-supply sequencing to avoid damaging the GPU:

- All the GPU supplies, except for VDD_33, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 20 mV/µs.
- It is recommended that the 3.3-V rail ramps up first.
- The 1.8 rail must reach its steady state at least 10 µs before VDDC, VDDCI, VDD_08, and VMEMIO start to ramp up.





For AMD R18M-M18-70 VRAM

Memory ID/Vendor/Size	Memory PN R3(ABO!) A0	Memory PN R3(ABO!) A1	Memory PN R3(ABO!) B0	Memory PN R3(ABO!) B1
000 SAMSUNG 256M x32	UV1001 V4G_S@ S IC D5 256M32 K4G80325FB-HC25 FBGA ABO! SA00009TA10	UV1002 V4G_S@ S IC D5 256M32 K4G80325FB-HC25 FBGA ABO! SA00009TA10		
001 HYNIX 256M x32	UV1001 V4G_H@ S IC D5 256M32 H5GC8H24AJR-R0C BGA ABO! SA00009U160	UV1002 V4G_H@ S IC D5 256M32 H5GC8H24AJR-R0C BGA ABO! SA00009U160		
100 MICRON 256M x32	UV1001 V4G_M@ S IC D5 256M32 MT51J256M32HF-70B ABO! SA00009TV50	UV1002 V4G_M@ S IC D5 256M32 MT51J256M32HF-70B ABO! SA00009TV50		

AMD GPU PN

R19M-M18-70 PN R3(ROH)
UV1 M1870@ S IC 216-0923020 R19M-M18-70 FCBGA 769P GPU 0FA SA0000CLW00

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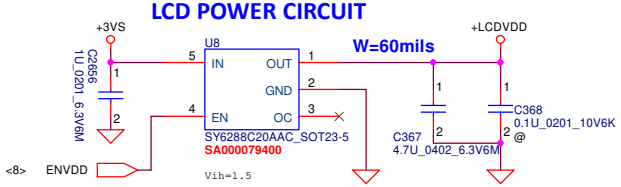
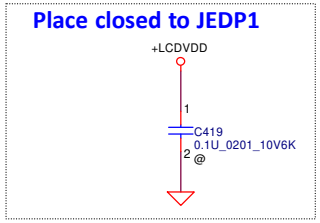
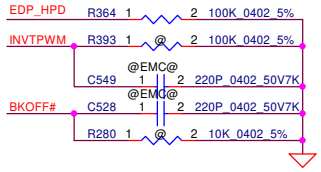
LCD POWER CIRCUIT

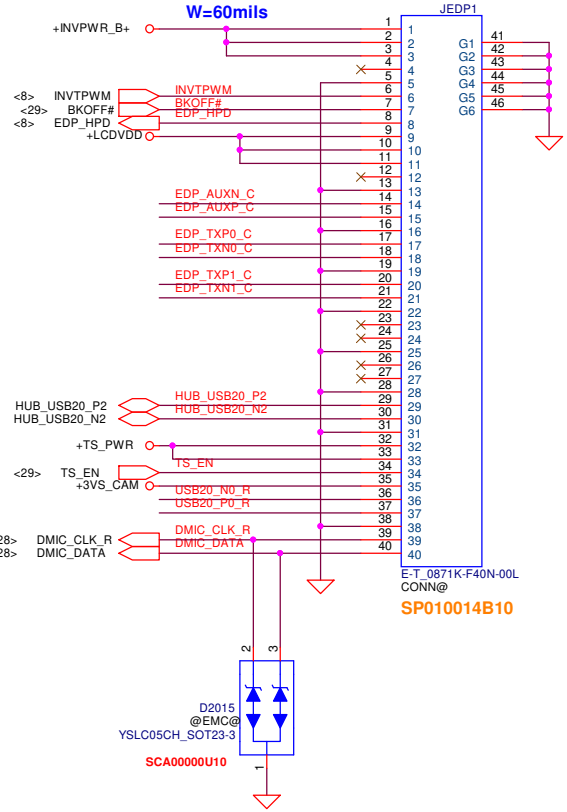


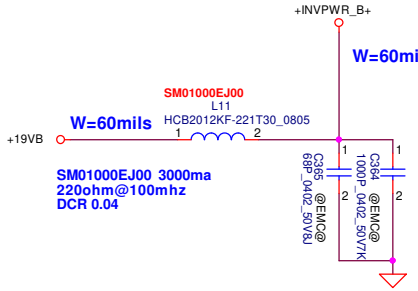
Place closed to JEDP1

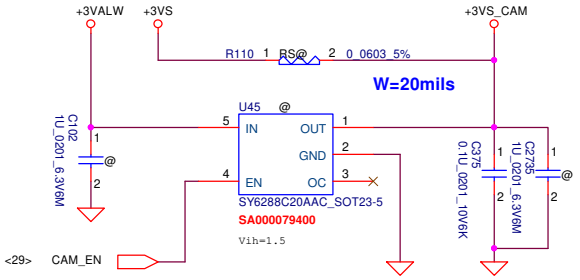




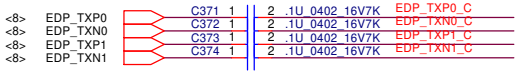
LED PANEL Conn.

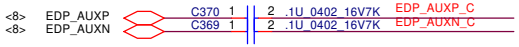




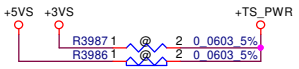


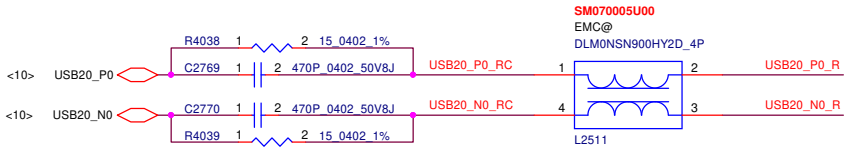
Place closed to JEDP1





Touch Screen





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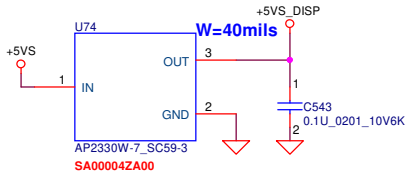
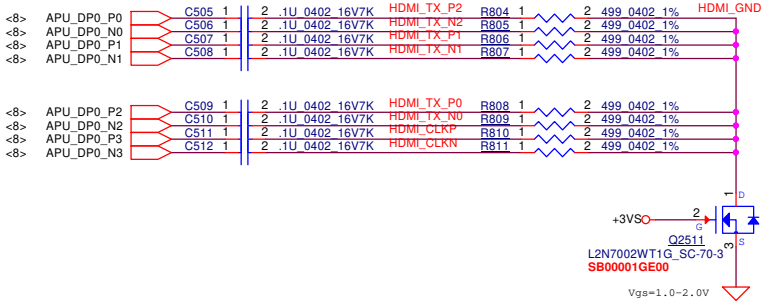
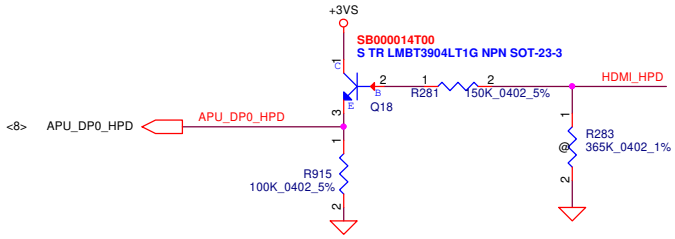
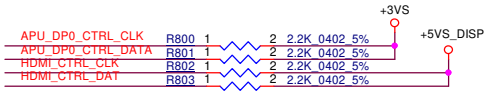
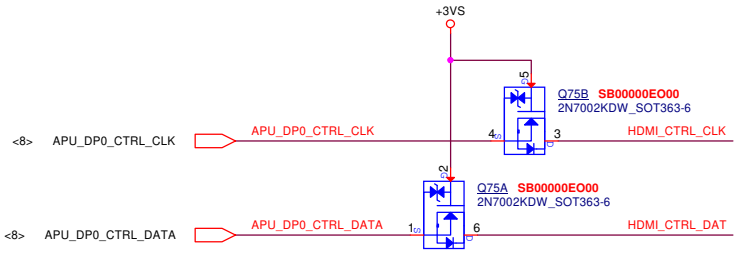
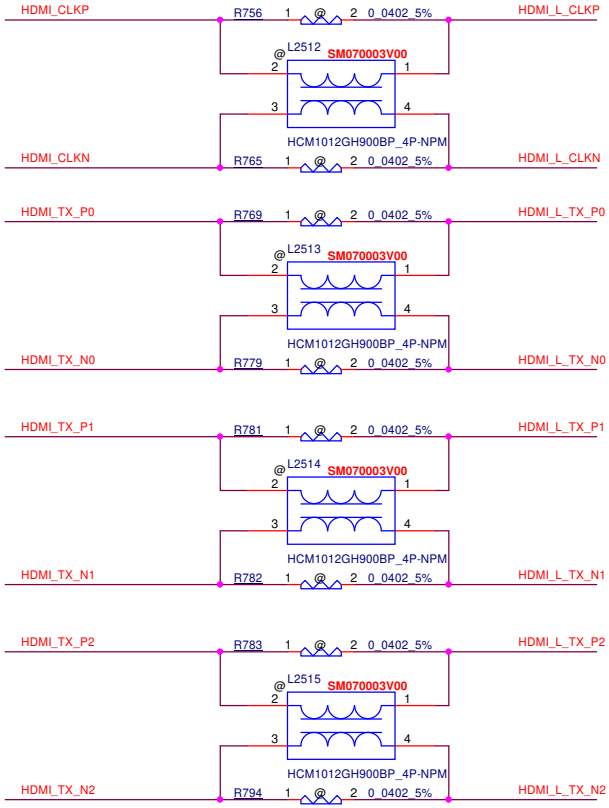


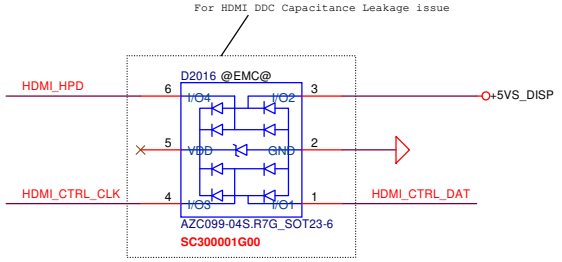


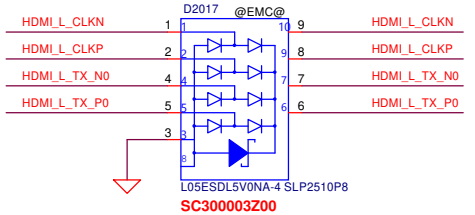


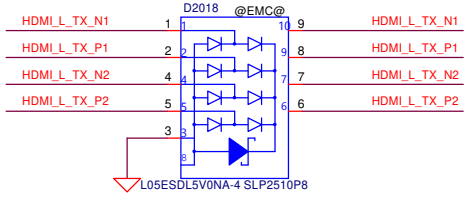




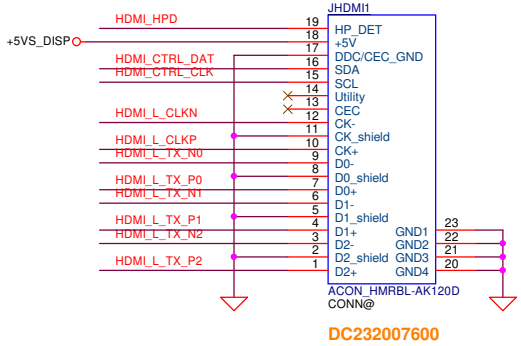








HDMI connector



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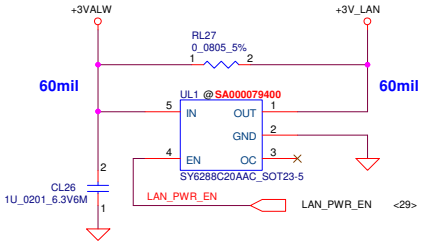

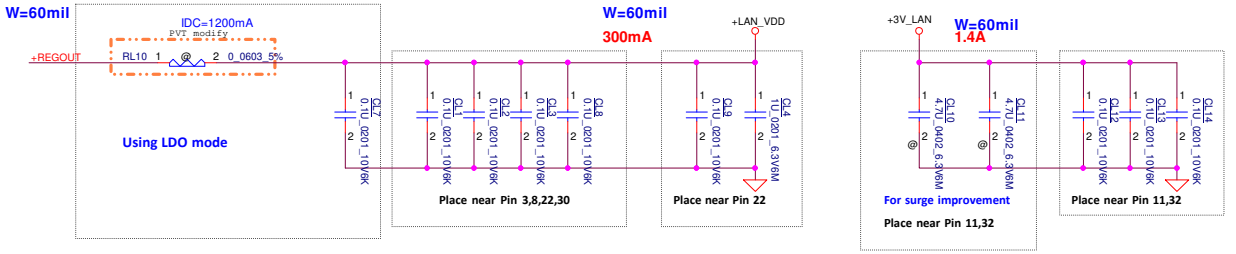

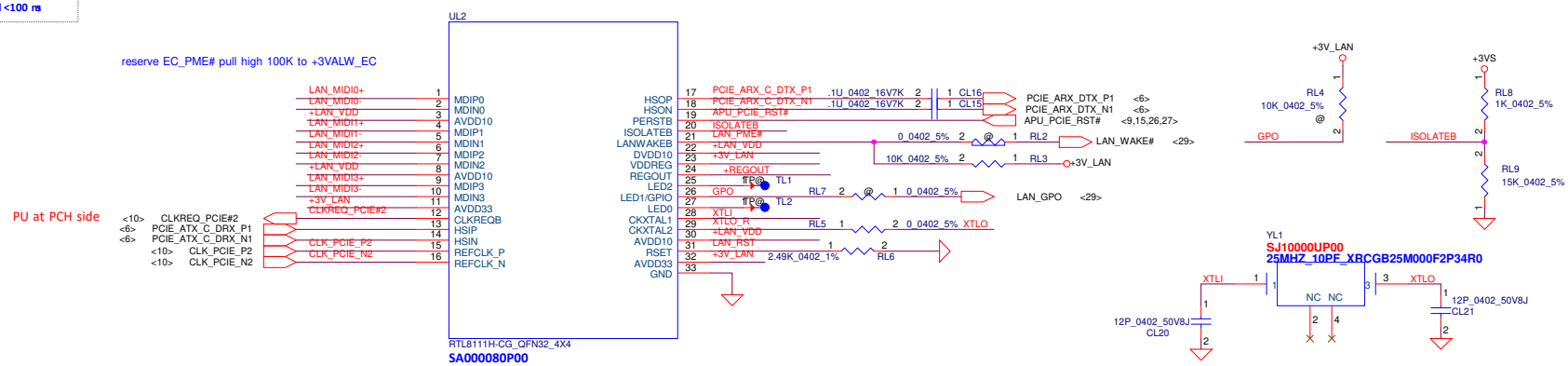

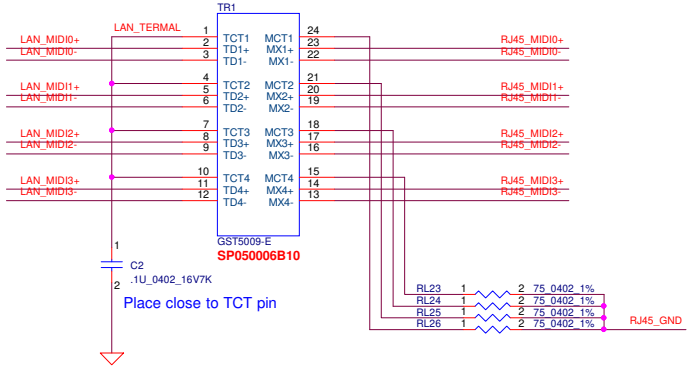

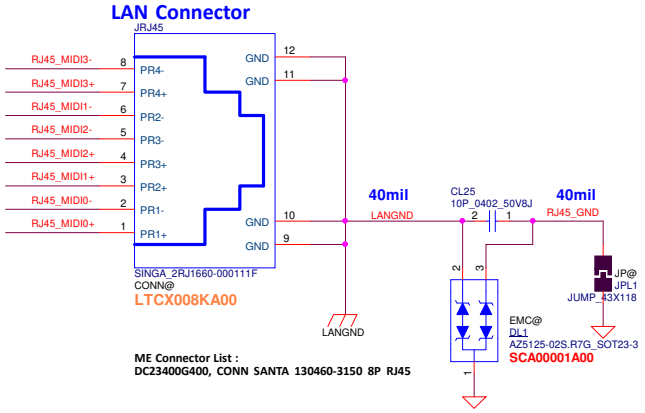

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Issued Date	2020/03/29	Deciphered Date	2020/03/29

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Title: LAN RTL8111H			
Size: Custom	Document Number: EH5LP/AP_LA-H801P		Rev: 1.A
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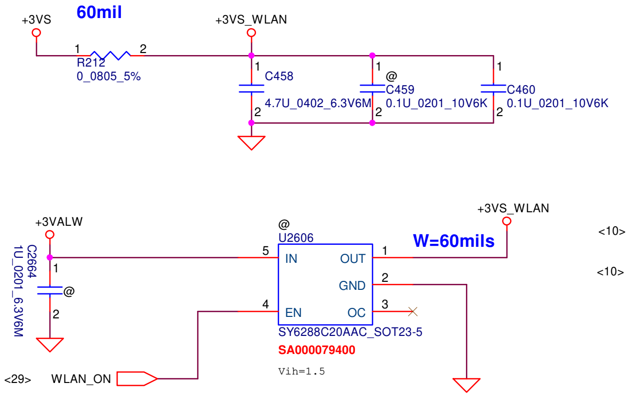
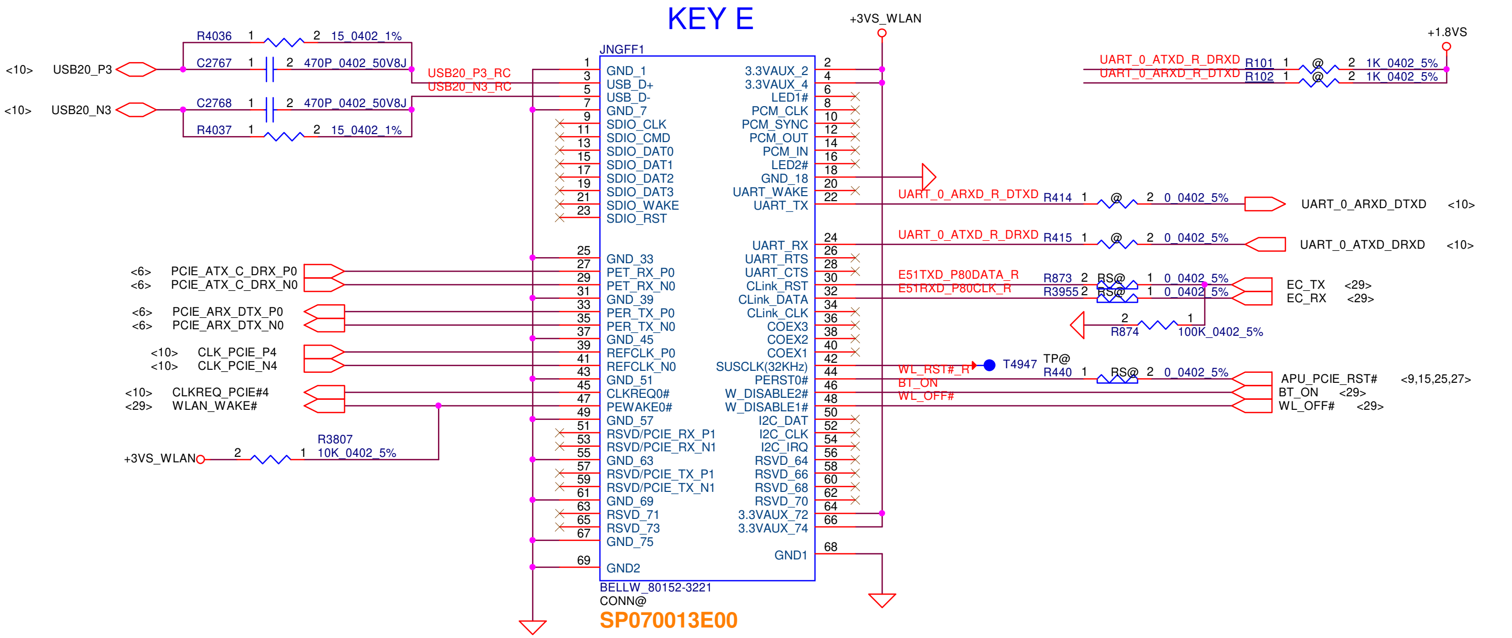
Wireless LAN





NGFF WL+BT (KEY E)

		GND	75
74	3.3V	RESERVED/REFCLKN1	73
72	3.3V	RESERVED/REFCLKP1	71
70	UIM_Power_SRC/GPIO1/PEWake1#	GND	69
68	UIM_Power_SNK/CLKREQ1#	Reserved/PERn1	67
66	UIM_SWP/PERST1#	Reserved/PERp1	65
64	RESERVED	GND	63
62	ALERT# (I)(0/3.3)	Reserved/PETn1	61
60	I2C CLK (O)(0/3.3)	Reserved/PETp1	59
58	I2C DATA (IO)(0/3.3)	GND	57
56	W_DISABLE#1 (O)(0/3.3V)	PEWake0# (IO)(0/3.3V)	55
54	Reserved/W_DISABLE#2 (O)(0/3.3V)	CLKREQ0# (IO)(0/3.3V)	53
52	PERST0# (O)(0/3.3V)	GND	51
50	SUSCLK(32kHz) (O)(0/3.3V)	REFCLKN0	49
48	COEX1 (I/O)(0/1.8V)	REFCLKP0	47
46	COEX2(I/O)(0/1.8V)	GND	45
44	COEX3(I/O)(0/1.8V)	PERn0	43
42	VENDOR DEFINED	PERp0	41
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	PETn0	37
36	UART RTS (O)(0/1.8V)	PETp0	35
34	UART CTS (I)(0/1.8V)	GND	33
32	UART Tx (O)(0/1.8V)	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	SDIO Reset# (O)(0/1.8V)	23
22	UART Rx (I)(0/1.8V)	SDIO Wake# (I)(0/1.8V)	21
20	UART Wake# (I)(0/3.3V)	SDIO DAT3(IO)(0/1.8V)	19
18	GND	SDIO DAT2(IO)(0/1.8V)	17
16	LED#2 (I)(OD)	SDIO DAT1(IO)(0/1.8V)	15
14	PCM_OUT/I2S SD_OUT (O)(0/1.8V)	SDIO DAT0(IO)(0/1.8V)	13
12	PCM_IN/I2S SD_IN (I)(0/1.8V)	SDIO CMD(IO)(0/1.8V)	11
10	PCM_SYNC/I2S WS (OI)(0/1.8V)	SDIO CLK(O)(0/1.8V)	9
8	PCM_CLK/I2S SCK (OI)(0/1.8V)	GND	7
6	LED#1 (I)(OD)	USB_D-	5
4	3.3V	USB_D+	3
2	3.3V	GND	1

HTTPS://REALSCHEMATIC.COM

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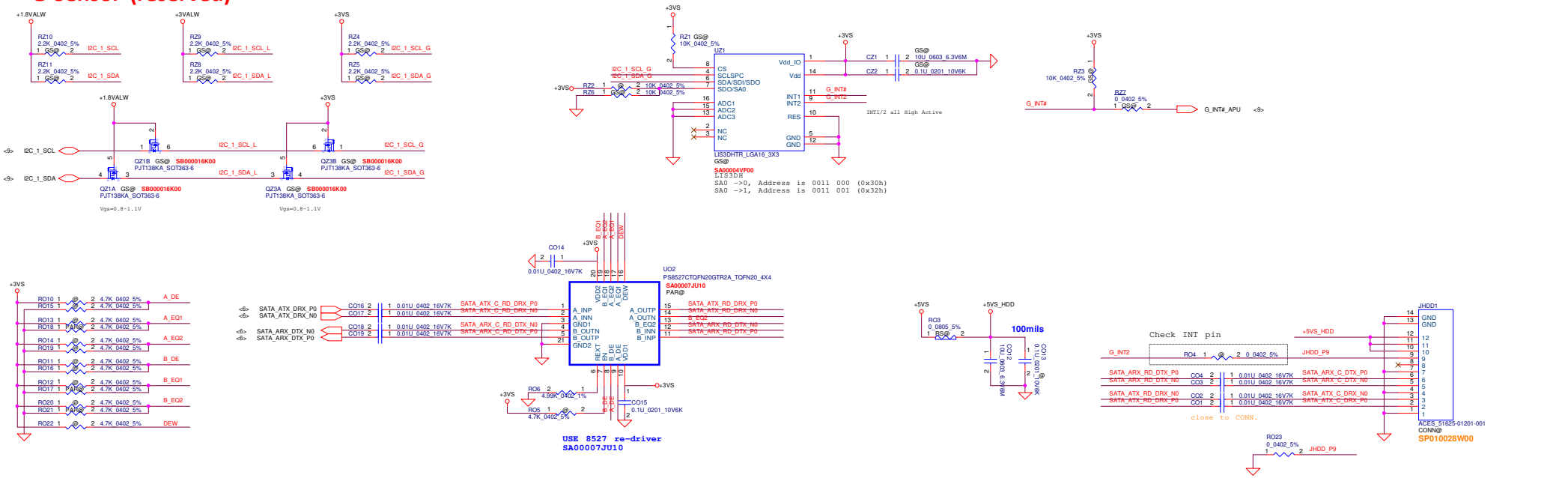
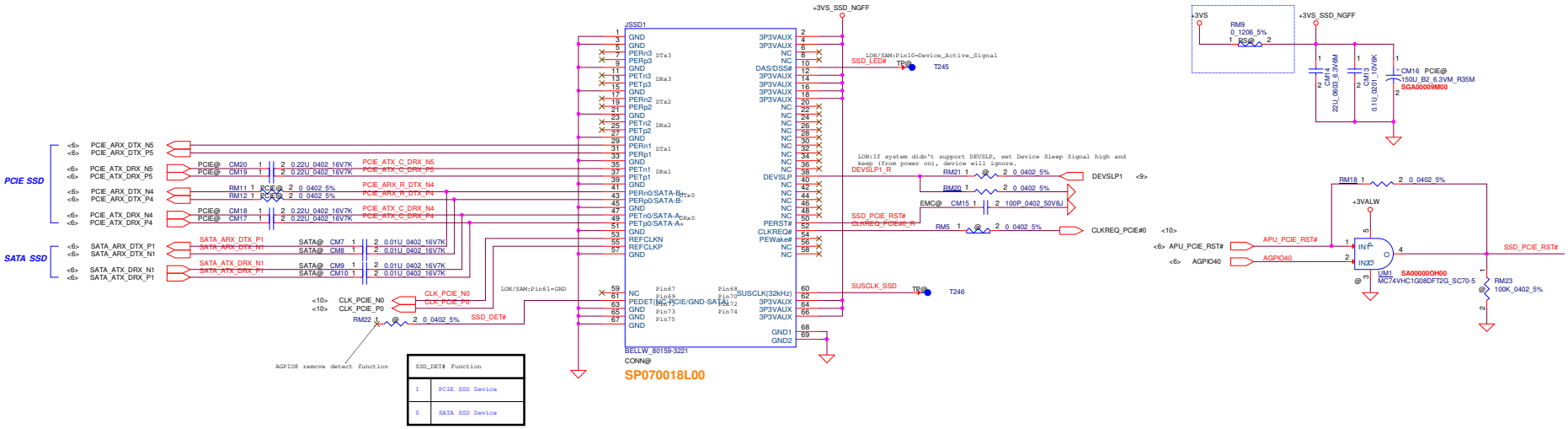
				Size: Custom; Document Number: EH5LP/AP_LA-H801P; Rev: 1.A
				Date: Friday, March 29, 2019; Sheet 26 of 48

SATA Re-Driver and cable HDD Conn.

G-Sensor (reserved)

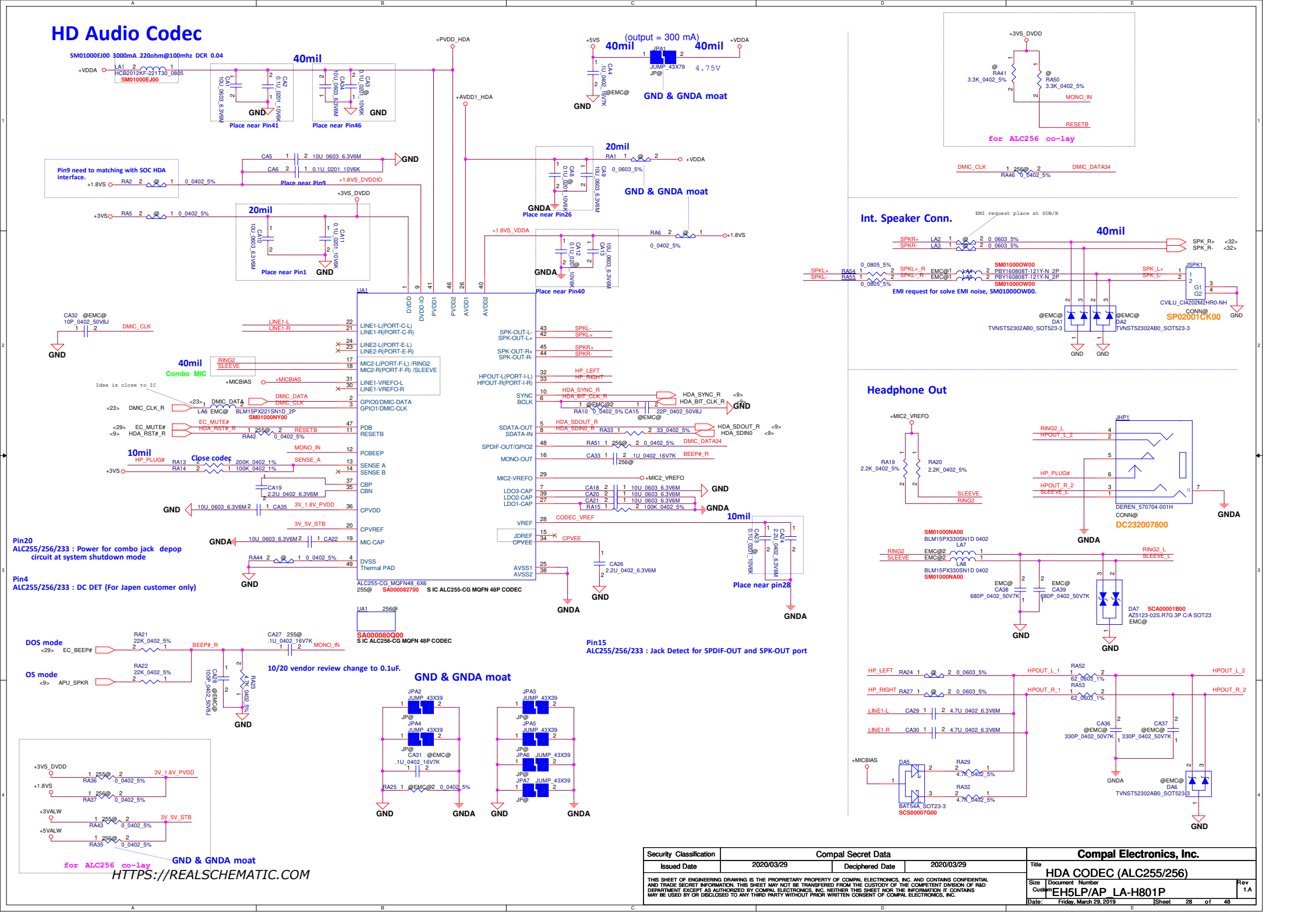


SATA NGFF SSD Conn.



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/29	Deciphered Date 2020/03/29	Title HDD/SSD
			Size Custom / Document Number EH5LP/AP_LA-H801P / Rev 1.A
			Date: Friday, March 29, 2019 / Sheet 27 of 48

HD Audio Codec



Int. Speaker Conn.

Headphone Out

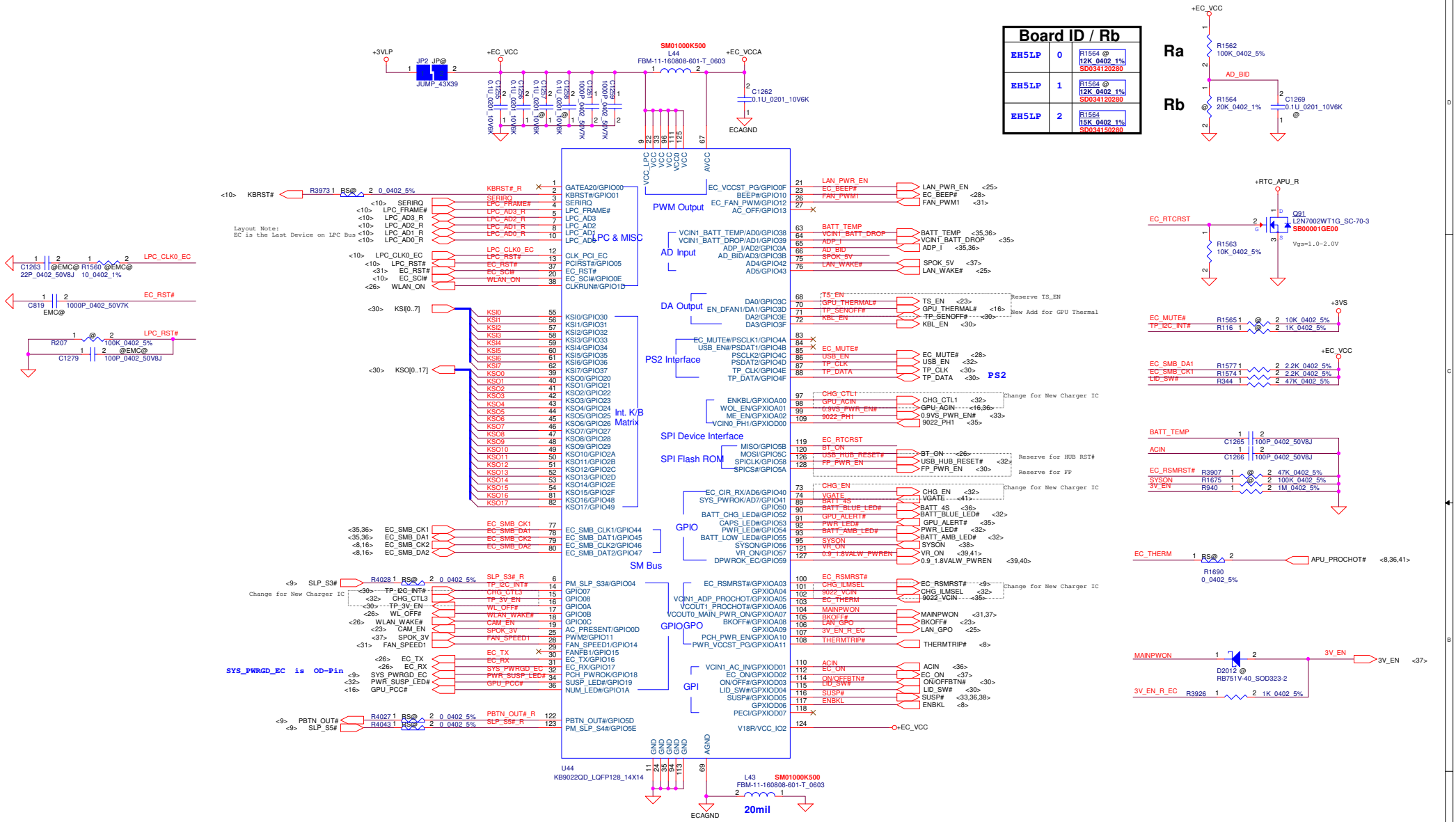
Security Classification	Compal Secret Data		
Issued Date	2020/03/29	Deciphered Date	2020/03/29

Compal Electronics, Inc.

Title: HDA CODEC (ALC255/256)

Size	Document Number	Rev
Custom	EH5LP/AP_LA-H801P	1.A

Date: Friday, March 29, 2019 | Sheet 28 of 48



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Security Classification	Compal Secret Data		
Issued Date	2020/03/29	Deciphered Date	2020/03/29

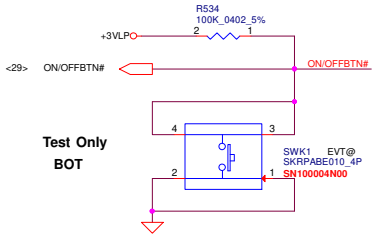
Compal Electronics, Inc.

Title: EC ENE-KB9022

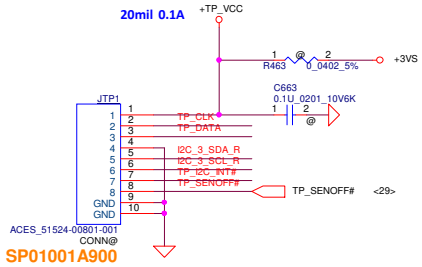
Size	Document Number	Rev
Custom	EH5LP/AP_LA-H801P	1.A

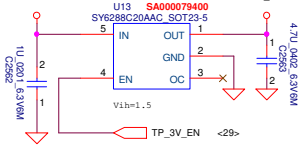
Date: Friday, March 29, 2019 Sheet 29 of 48

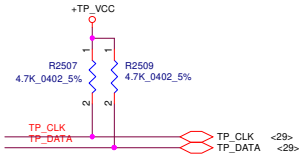
ON/OFF BTN

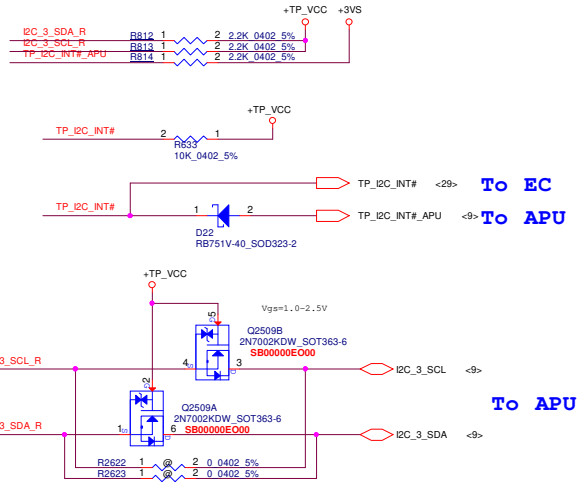


TP/B Conn.

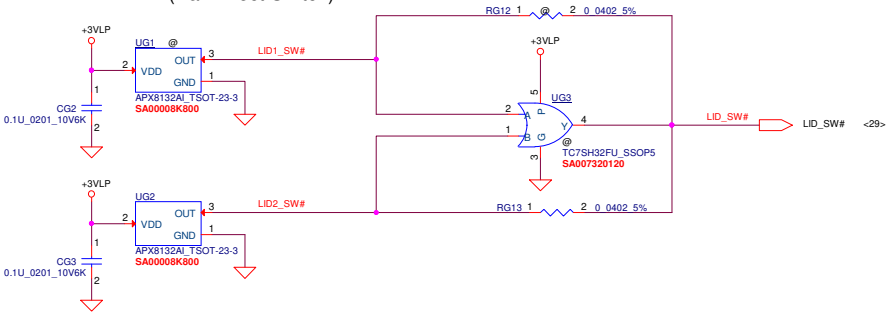




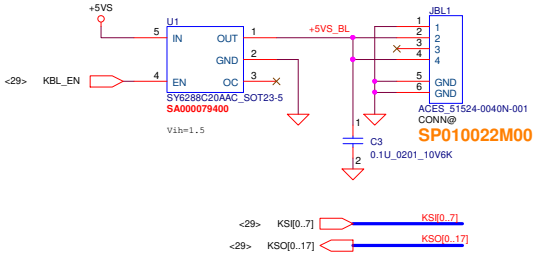




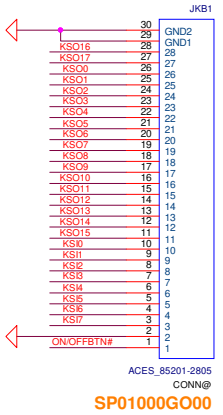
Lid Switch (Hall Effect Switch)



KB BackLight

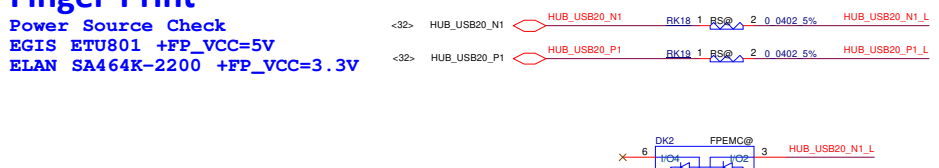


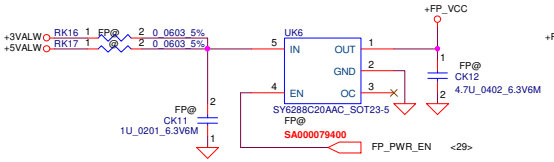
KB Conn.

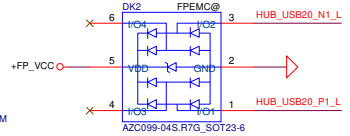


Finger Print

Power Source Check
EGIS ETU801 +FP_VCC=5V
ELAN SA464K-2200 +FP_VCC=3.3V

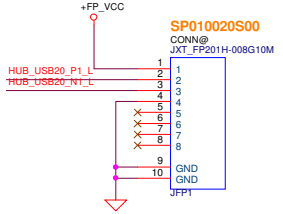






JFP1

PIN	SA464K-2200
1	+FP_VCC (3V)
2	D+
3	D-
4	GND
5	NC
6	NC
7	NC
8	NC



Security Classification	Compal Secret Data		
Issued Date	2020/03/29	Deciphered Date	2020/03/29

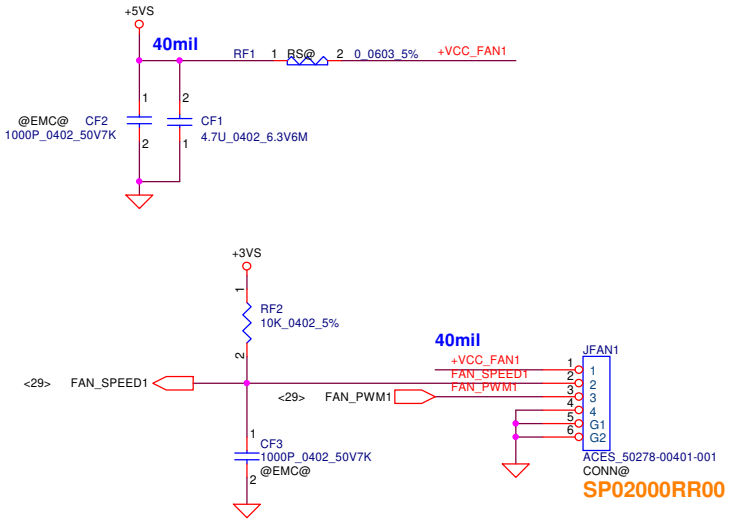
Compal Electronics, Inc.

Title: KB/TP/TPM/LID

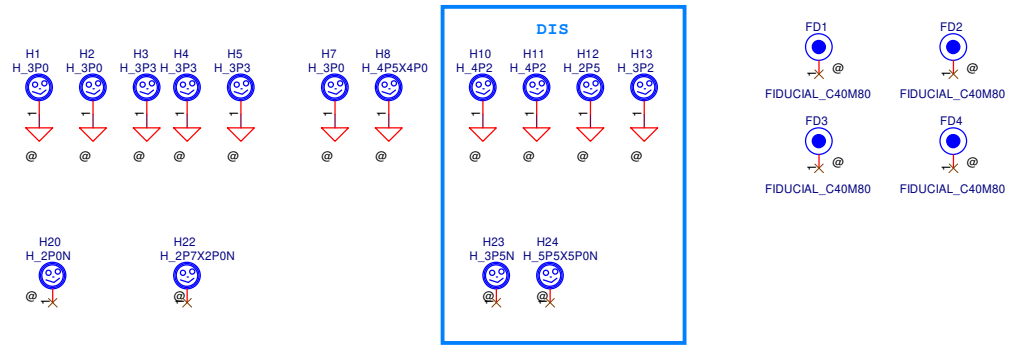
Size: Custom | Document Number: EH5LP/AP_LA-H801P | Rev: 1.A

Date: Friday, March 29, 2019 | Sheet 30 of 48

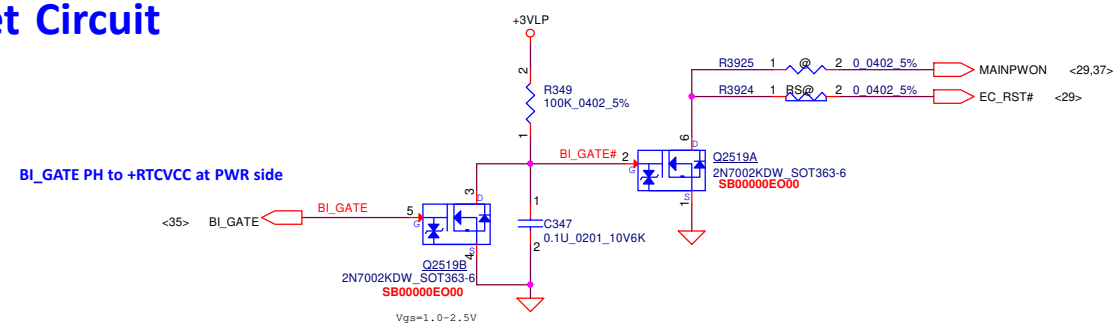
FAN Conn



Screw Hole

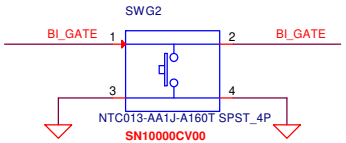


Reset Circuit



Reset But t on

Reset But t on



Security Classification	Compal Secret Data		
Issued Date	2020/03/29	Deciphered Date	2020/03/29

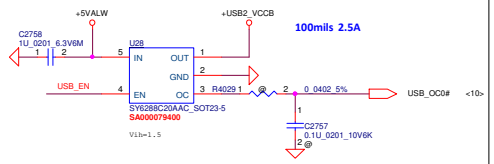
Compal Electronics, Inc.

Title: FAN/BATT RESET_DEGUB SW

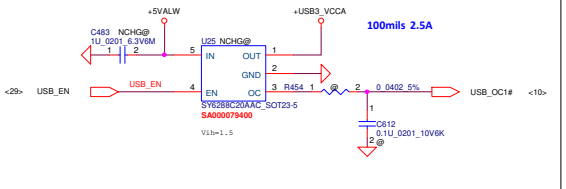
Size: Custom | Document Number: EH5LP/AP_LA-H801P | Rev: 1.A

Date: Friday, March 29, 2019 | Sheet 31 of 48

Power For USB2.0



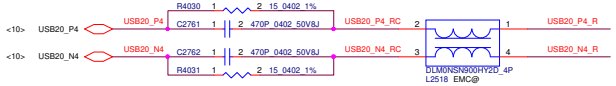
Non-Charger Co-lay

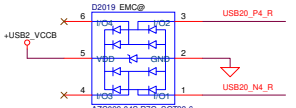


USB Host Charger Truth Table

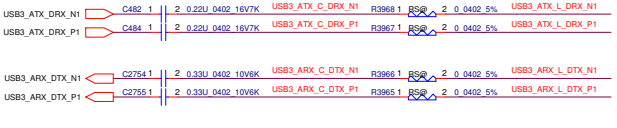
CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H	Data Lines Connected

USB2.0 (Port 0)

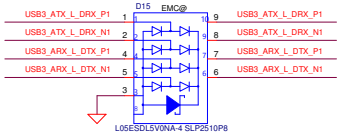


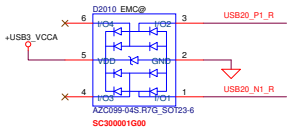


USB3.0 (Port 1)

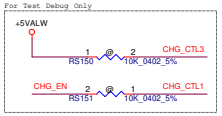


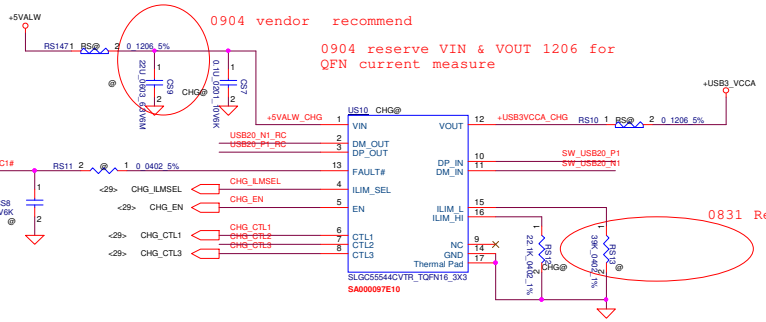
For ESD request

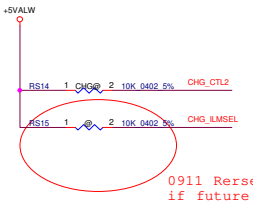




For Test Debug Only







0904 vendor recommend

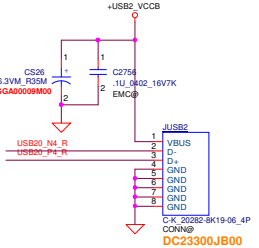
0904 reserve VIN & VOUT 1206 for QFN current measure

0831 Reserve ILIM_L R as vendor recommend

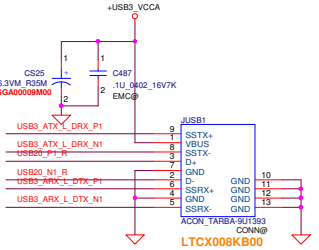
0911 Rerserve PU, vendor suggest to EC control if future need support SDP2

ILM R vaule
Ios(mA)=50250/R(Kohm)
ILIM_Hi=2273mA
ILIM_L=1288mA

USB2.0 Conn.

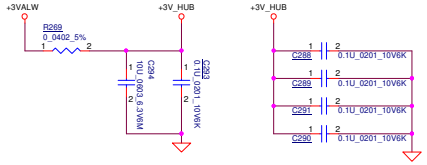


USB3.0 Conn.

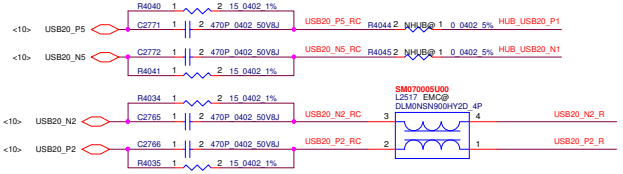


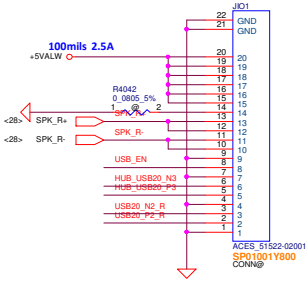
ME Connector List:
DC23300TT00, CONN ACON TCRAF-9V1391 9P USB3.0

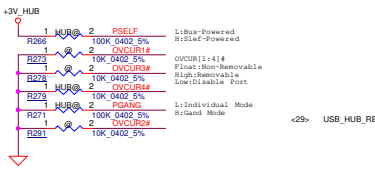
USB HUB

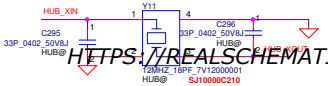


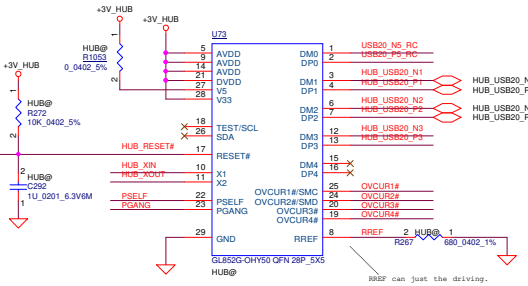
C279 close to U73 pin5
C280 close to U73 pin9
C283 close to U73 pin14
C284 close to U73 pin21











HUB_USB20_N1 <30>
HUB_USB20_P1 <30>
HUB_USB20_N2 <23>
HUB_USB20_P2 <23>

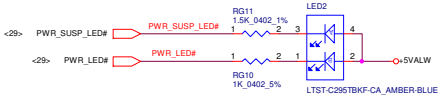
Finger Print
Touch Screen
Card Reader

(Single-TT) SA000066320, S IC GL850G-OHY50 QFN 28P USB2.0 HUB
(Multple-TT) SA000065710, S IC GL852G-OHY50 QFN 28P USBHUB

LED

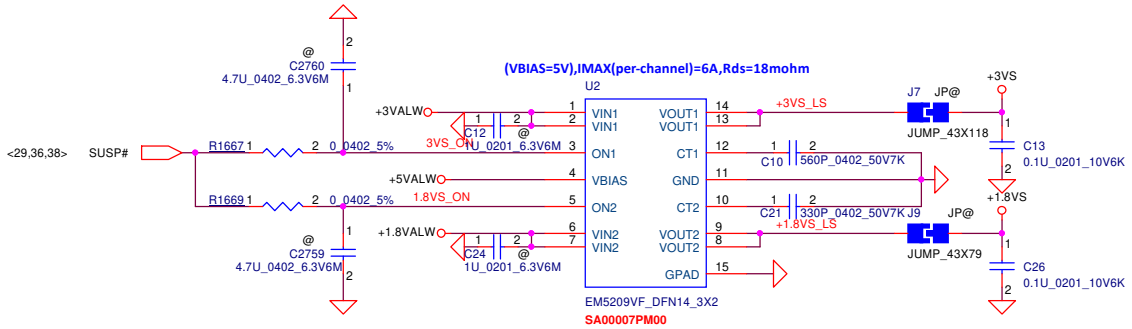
Battery LED

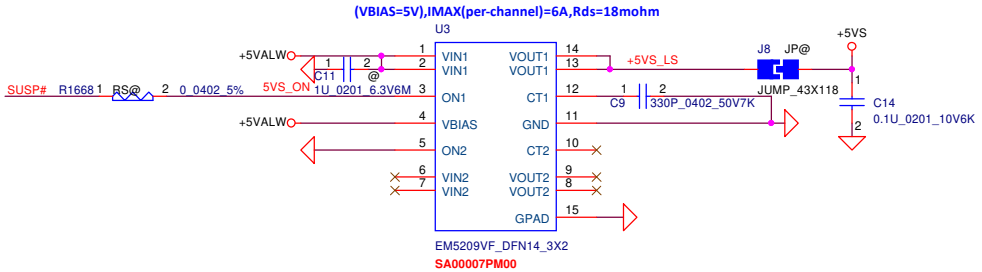
Power LED

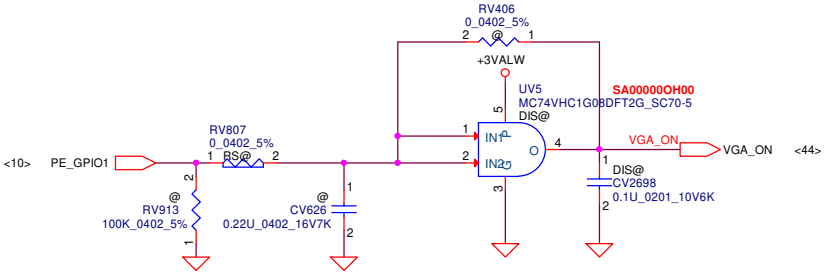


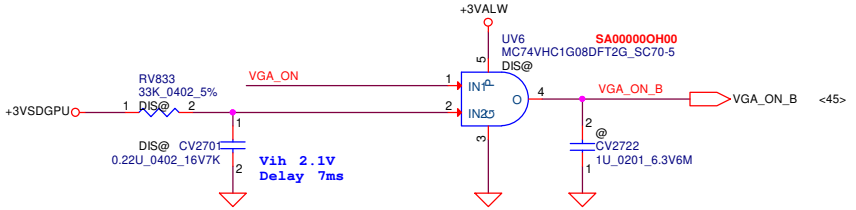
Security Classification	Compal Secret Data		
Issued Date	2020/03/29	Deciphered Date	2020/03/29

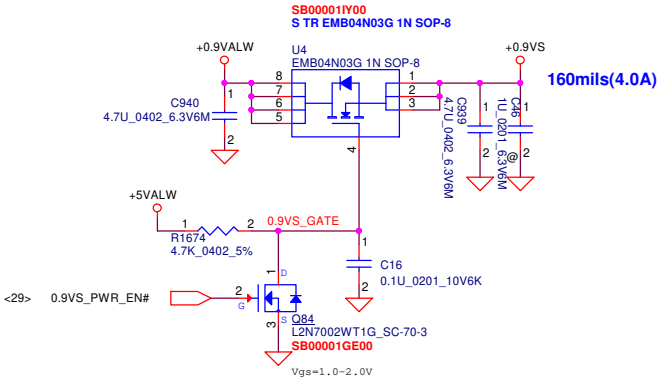
Compal Electronics, Inc.			
Title: USB30/USB HUB/LED			
Size: Custom	Document Number: EH5LP/AP_LA-H801P		Rev: 1.A
Date: Friday, March 29, 2019	Sheet 32 of 48		

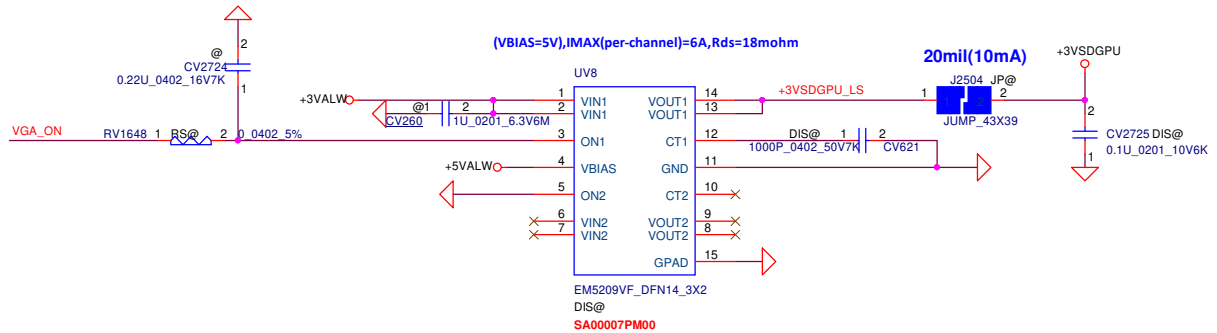












+3VALW TO +3VSDGPU

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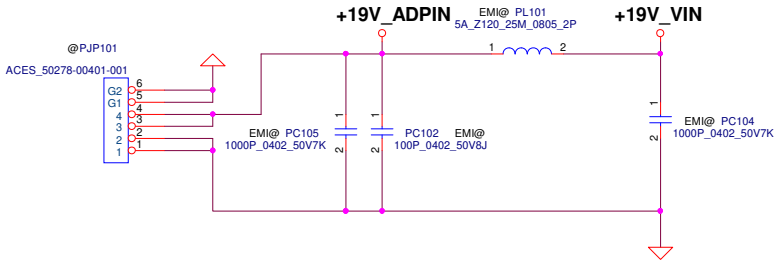
Security Classification	Compal Secret Data		
Issued Date	2020/03/29	Deciphered Date	2020/03/29

Compal Electronics, Inc.

Title: DC INTERFACE

Size	Document Number	Rev
Custom	EH5LP/AP_LA-H801P	1.A

Date: Friday, March 29, 2019 Sheet 33 of 48



Security Classification	Compal Secret Data		
Issued Date	2020/03/29	Deciphered Date	2020/03/29

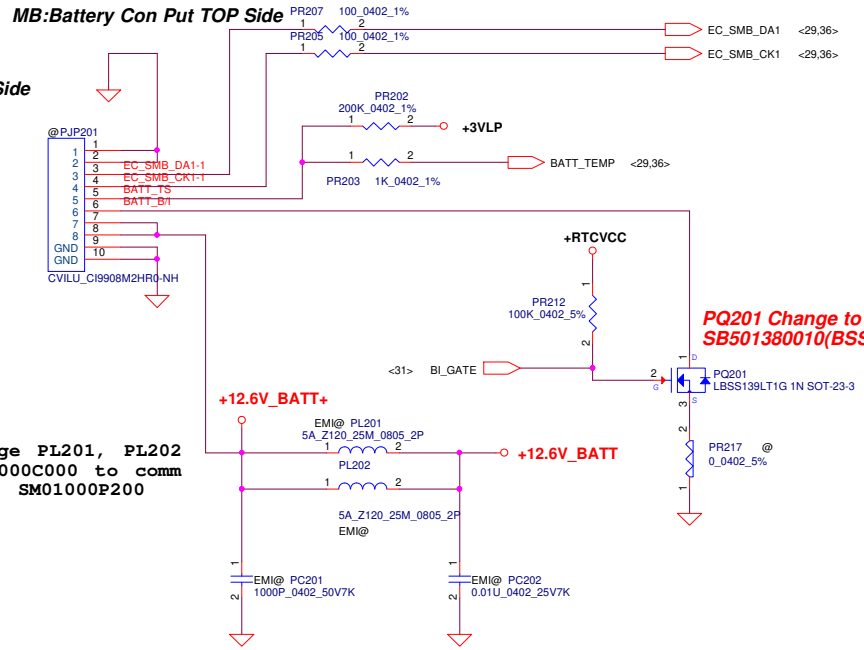
Compal Electronics, Inc.

Title: **PWR DCIN / Pre-charge**

Size	Document Number	Rev
Custom	EH5KP/AP_LA-H801P	0.1

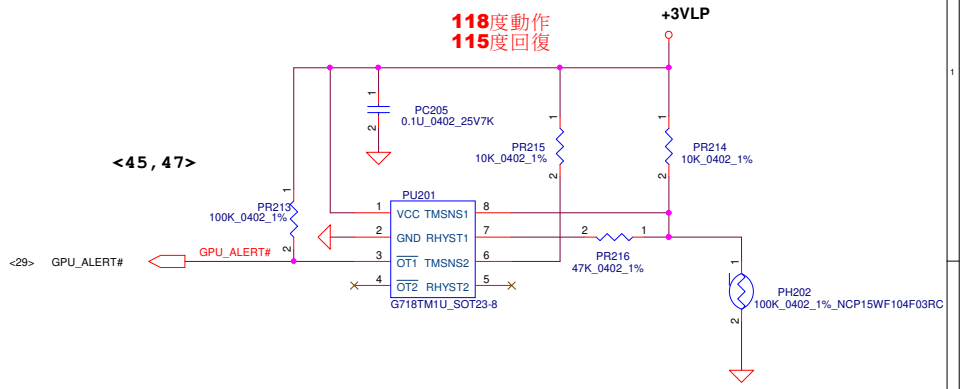
Date: Friday, March 29, 2019 Sheet 34 of 48

2013/07/23
change PC5 and PC6 function field from 37.1 to 47.1



PQ201 Change to SB00000QO00, SB501380010(BSS138LT1G Del)

change PL201, PL202 SM01000C000 to comm part SM01000P200

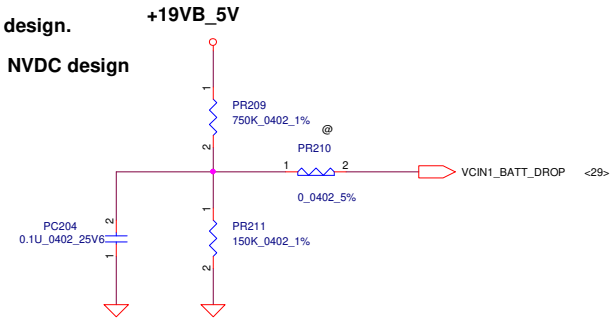


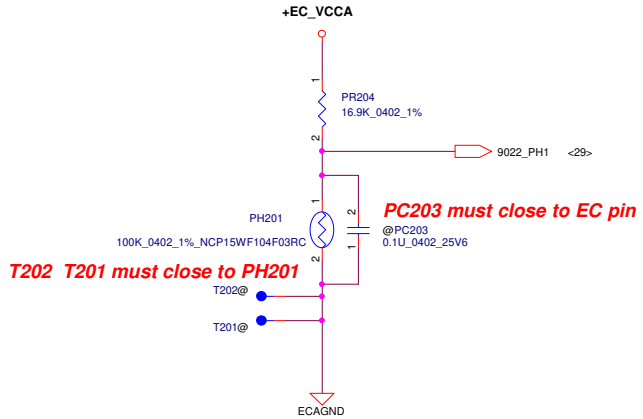
For KB9022 sense 10mΩ	Active	Recovery
		Active=recovery
		Active=recovery
PH1	2V	1V

PH1 under CPU botten side :
CPU thermal protection at 89 +-3 degree C
Recovery at 56 +-3 degree C

2013/06/07
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

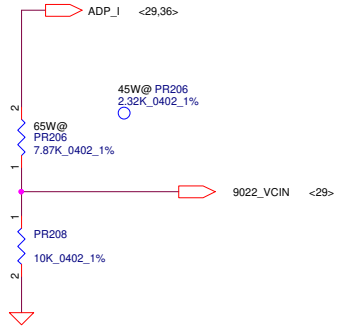
VAL50/ZAL20 Battery is 3-cell NVDC design.
B+=9V
Change PR12=50k if Battery is 2-cell NVDC design
B+=6V





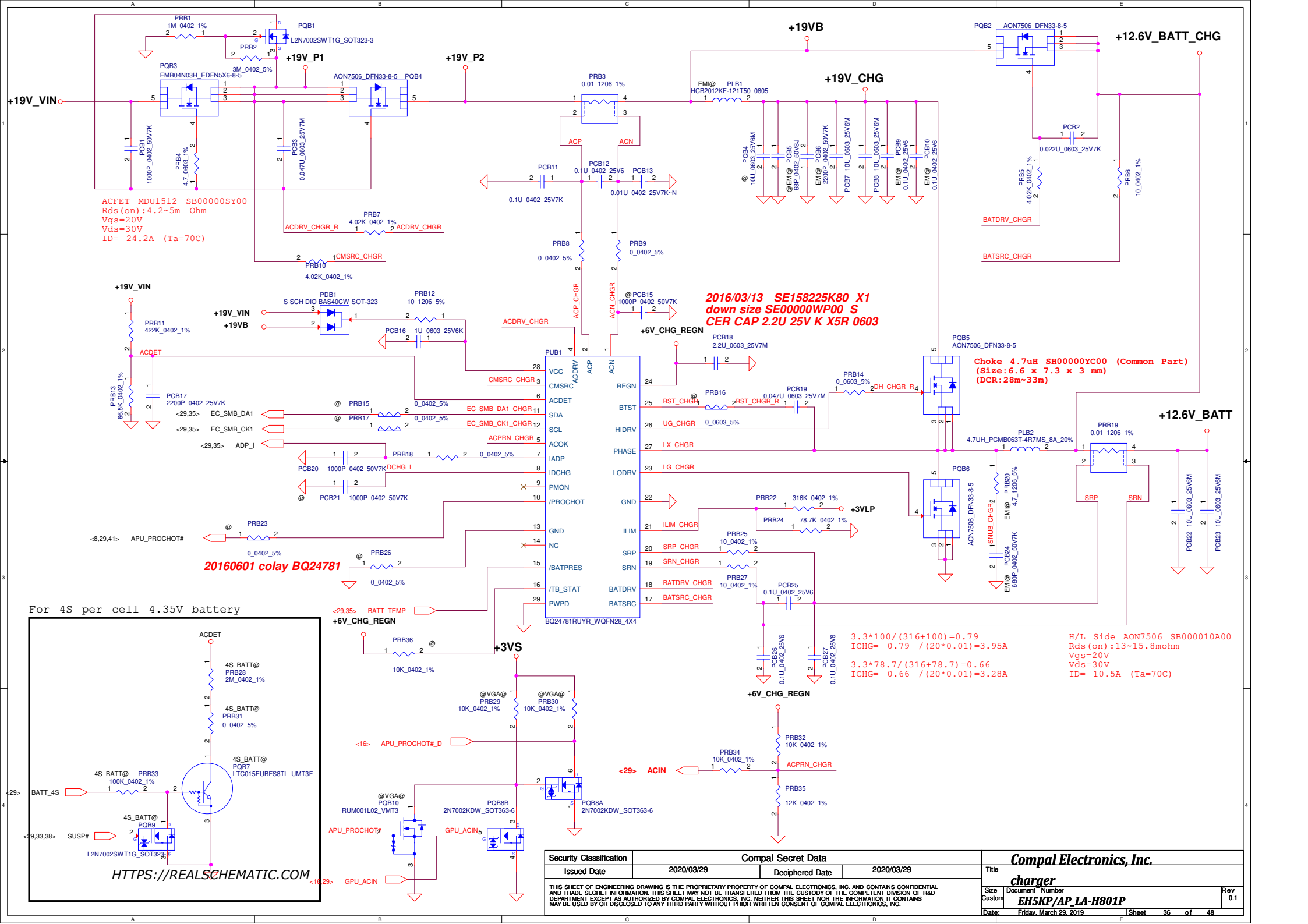
PC203 must close to EC pin

T202 T201 must close to PH201



Security Classification	Compal Secret Data		
Issued Date	2020/03/29	Deciphered Date	2020/03/29

Compal Electronics, Inc.			
Title	PWR-BATTERY CONN/OTP		
Size	Document Number		Rev
Custom	EH5KP/AP_LA-H801P		0.1
Date:	Friday, March 29, 2019	Sheet	35 of 48


+19V_VIN
+19V_P1
+19V_P2
+19VB
+19V_CHG
+12.6V_BATT_CHG
+12.6V_BATT
PQB1 L2N7002SWT1G_SOT323-3
PQB3 EMB04N03H_EDFN5X6-8-5
PQB4 AON7506_DFN33-8-5
PQB2 AON7506_DFN33-8-5
PRB1 1M_0402_1%
PRB2 3M_0402_5%
PRB3 0.01_1206_1%
PLB1 HCB2012KF-121T50_0805
ACFET MDU1512 SB00000SY00
Rds(on):4.2~5m Ohm
Vgs=20V
Vds=30V
ID= 24.2A (Ta=70C)
PRB7 4.02K_0402_1%
PRB10 4.02K_0402_1%
ACDRV_CHGR_R
ACDRV_CHGR
CMSRC_CHGR
PRB8 0_0402_5%
PRB9 0_0402_5%
ACP_CHGR
ACN_CHGR
PCB15 1000P_0402_50V7K
2016/03/13 SE158225K80 X1
down size SE00000WP00 S
CER CAP 2.2U 25V K X5R 0603
PDB1 S SCH DIO BAS40CW SOT-323
PRB12 10_1206_5%
PRB11 422K_0402_1%
PCB16 1U_0603_25V6K
ACDET
PCB17 2200P_0402_25V7K
PRB13 66.5K_0402_1%
+6V_CHG_REGN
PCB18 2.2U_0603_25V7M
PUB1
BQ24781RUYR_WQFN28_4X4
VCC
CMSRC
ACDET
SDA
SCL
ACOK
IADP
IDCHG
PMON
/PROCHOT
GND
NC
/BATPRES
/TB_STAT
PWPD
REGN
BTST
HIDRV
PHASE
LODRV
GND
ILIM
SRP
SRN
BATDRV
BATSRC
EC_SMB_DA1_CHGR
EC_SMB_CK1_CHGR
ACPRN_CHGR
DCHG_I
BST_CHGR
UG_CHGR
LX_CHGR
LG_CHGR
ILIM_CHGR
SRP_CHGR
SRN_CHGR
BATDRV_CHGR
BATSRC_CHGR
PRB14 0_0603_5%
DH_CHGR_R
PRB16
BST_CHGR_R
PCB19 0.047U_0603_25V7M
PQB5 AON7506_DFN33-8-5
Choke 4.7uH SH00000YC00 (Common Part)
(Size:6.6 x 7.3 x 3 mm)
(DCR:28m~33m)
PLB2 4.7UH_PCMB063T-4R7MS_8A_20%
PRB19 0.01_1206_1%
PQB6 AON7506_DFN33-8-5
PRB20 4.7_1206_5%
PCB24 680P_0402_50V7K
PRB22 316K_0402_1%
PRB24 78.7K_0402_1%
+3VLP
PRB25 10_0402_1%
PRB27 10_0402_1%
PCB25 0.1U_0402_25V6
PCB26 0.1U_0402_25V6
PCB27 0.1U_0402_25V6
PCB22 10U_0603_25V6M
PCB23 10U_0603_25V6M
PRB5 4.02K_0402_1%
PRB6 10_0402_1%
PCB2 0.022U_0603_25V7K
BATDRV_CHGR
BATSRC_CHGR
20160601 colay BQ24781
For 4S per cell 4.35V battery
4S_BATT@ PRB28 2M_0402_1%
4S_BATT@ PRB31 0_0402_5%
4S_BATT@ PQB7 LTC015EUBFS8TL_UMT3F
4S_BATT@ PRB33 100K_0402_1%
4S_BATT@ PQB9
L2N7002SWT1G_SOT323-3
BATT_4S
SUSP#
PRB36 10K_0402_1%
+3VS
@VGA@ PRB29 10K_0402_1%
@VGA@ PRB30 10K_0402_1%
APU_PROCHOT#_D
PRB34 10K_0402_1%
ACIN
ACPRN_CHGR
PRB32 10K_0402_1%
PRB35 12K_0402_1%
@VGA@ PQB10 RUM001L02_VMT3
PQB8B 2N7002KDW_SOT363-6
PQB8A 2N7002KDW_SOT363-6
APU_PROCHOT#
GPU_ACIN
3.3*100/(316+100)=0.79
ICHG= 0.79 /(20*0.01)=3.95A
3.3*78.7/(316+78.7)=0.66
ICHG= 0.66 /(20*0.01)=3.28A
H/L Side AON7506 SB000010A00
Rds(on):13~15.8mohm
Vgs=20V
Vds=30V
ID= 10.5A (Ta=70C)
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Compal Secret Data
Issued Date
2020/03/29
Deciphered Date
2020/03/29
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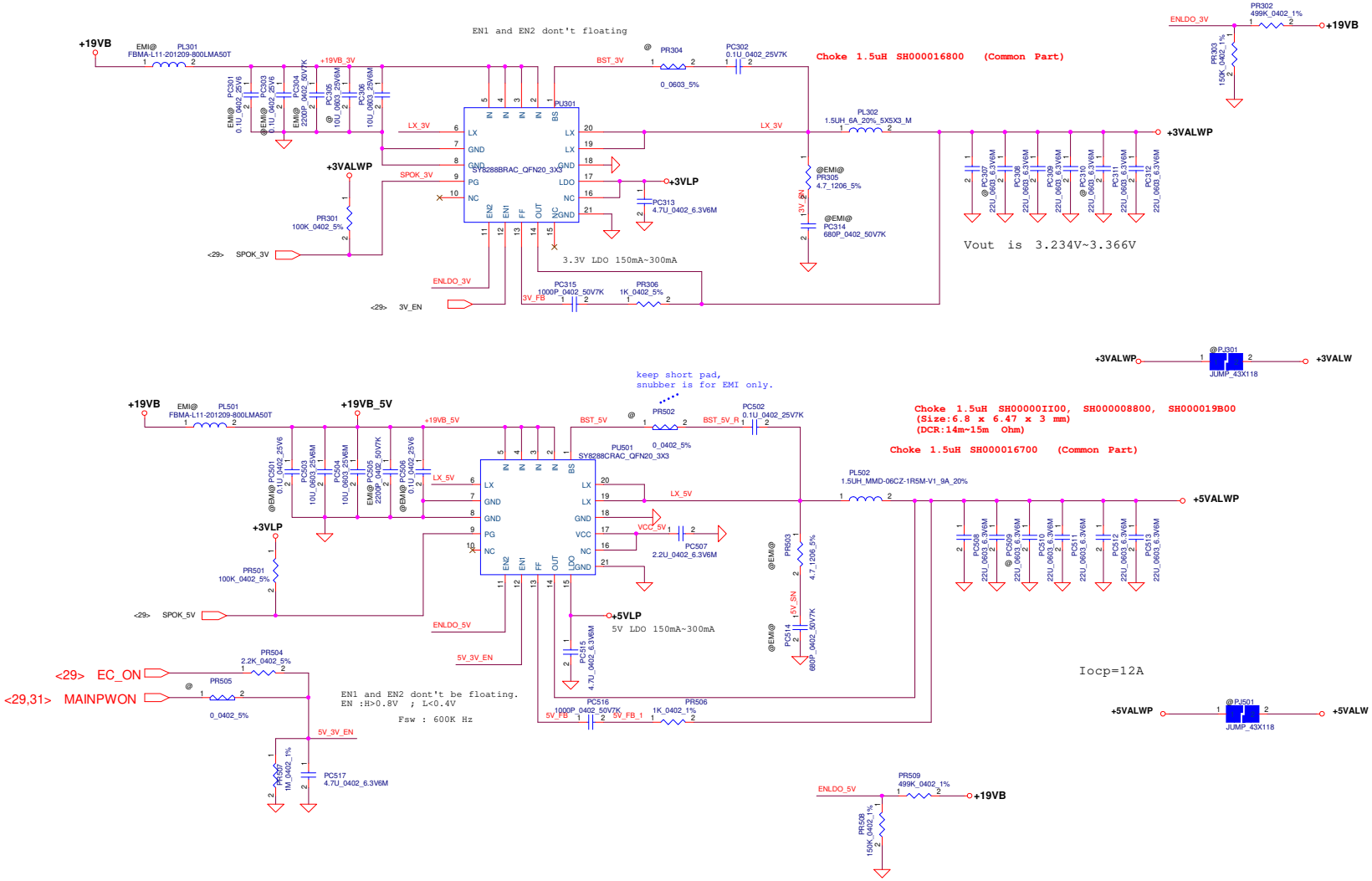
Compal Electronics, Inc.
Title
charger
Size Custom
Document Number
EH5KP/AP_LA-H801P
Rev 0.1
Date: Friday, March 29, 2019
Sheet 36 of 48



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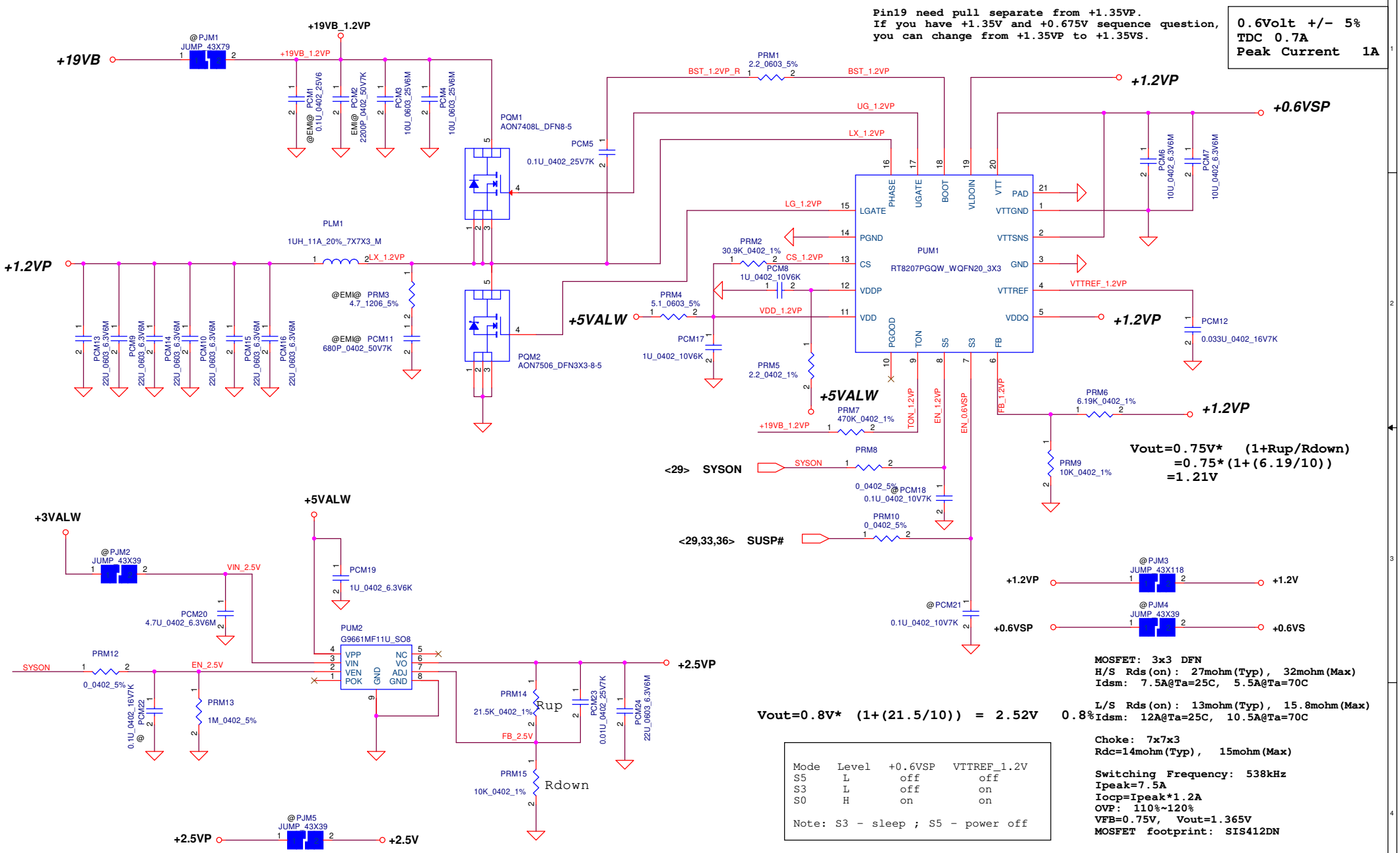
Issued Date	2020/03/29	Deciphered Date	2020/03/29

Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size	Document Number	Rev
Custom	EH5KP/AP_LA-H801P	0.1

Date: Friday, March 29, 2019 Sheet 37 of 48



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Issued Date	2020/03/29	Deciphered Date	2020/03/29

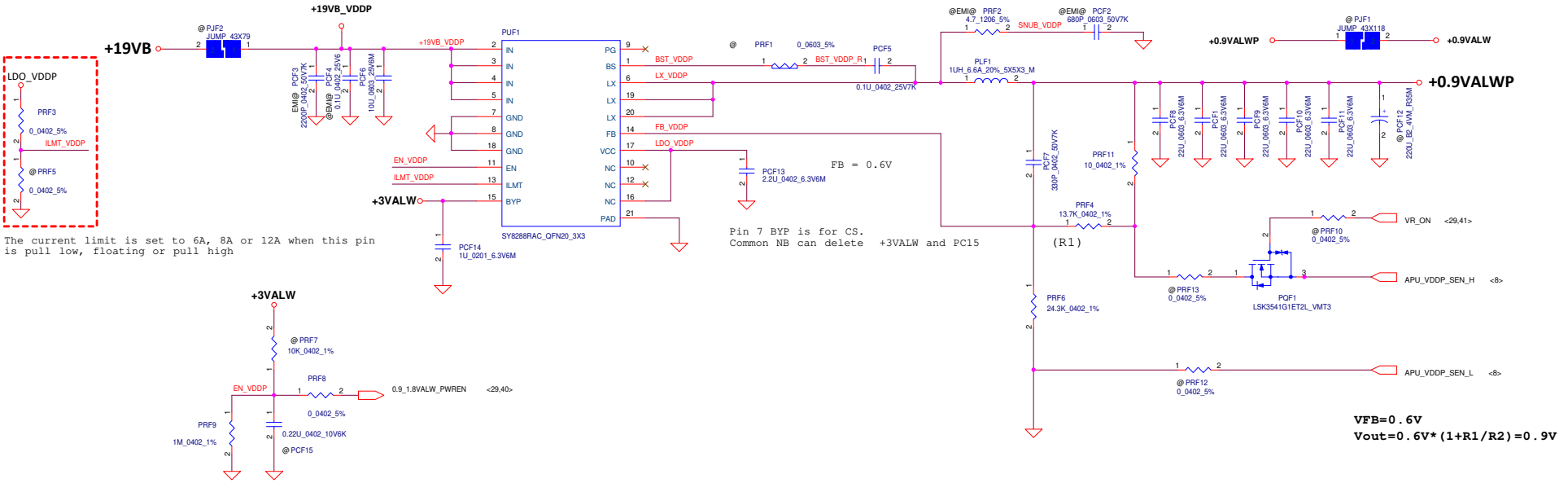
Compal Electronics, Inc.

Title: RT8207P

Size: Custom | Document Number: EH5KP/AP_LA-H801P | Rev: 0.1

Date: Friday, March 29, 2019 | Sheet 38 of 48

EN pin don't floating
If have pull down resistor at HW side, pls delete PR702



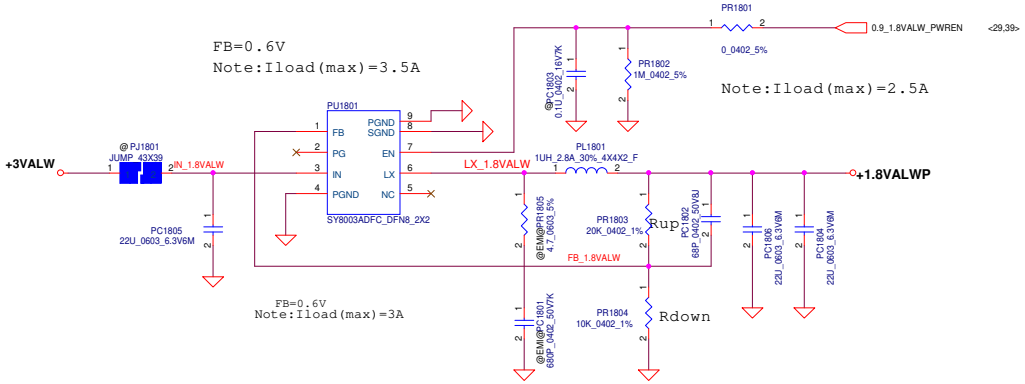
Security Classification	Compal Secret Data		
Issued Date	2020/03/29	Deciphered Date	2020/03/29

Compal Electronics, Inc.

Title: VCCP

Size	Document Number	Rev
C	EH5KP/AP_LA-H801P	0.1

Date: Friday, March 29, 2019 Sheet 39 of 48



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=[0.6V*(Rup+Rdown)/Rdown]
=1.8

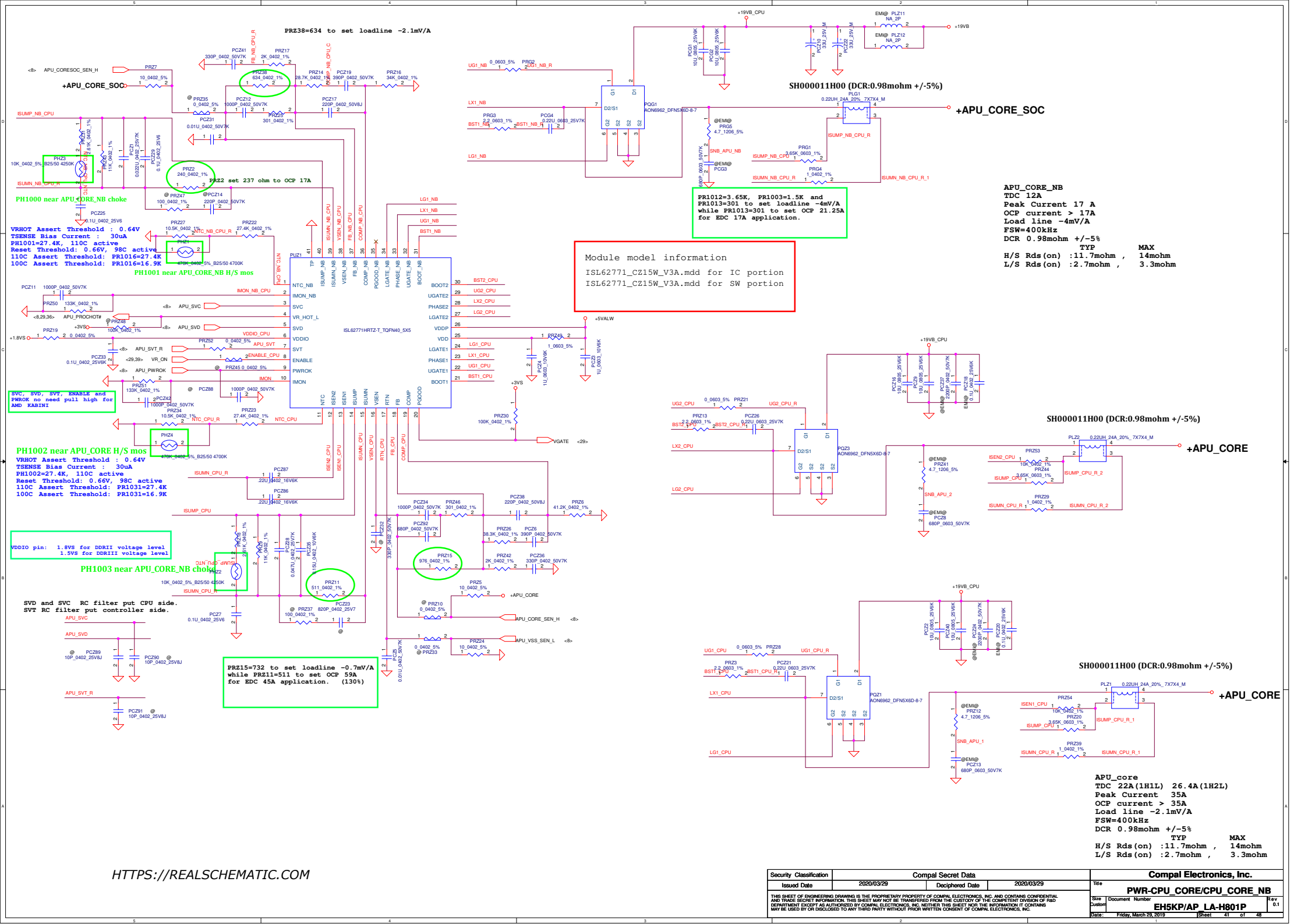
Security Classification	Compal Secret Data		
Issued Date	2020/03/29	Deciphered Date	2020/03/29

Compal Electronics, Inc.

Title: SY8032

Size	Document Number	Rev
C	EH5KP/AP_LA-H801P	0.1

Date: Friday, March 29, 2019 Sheet 40 of 48



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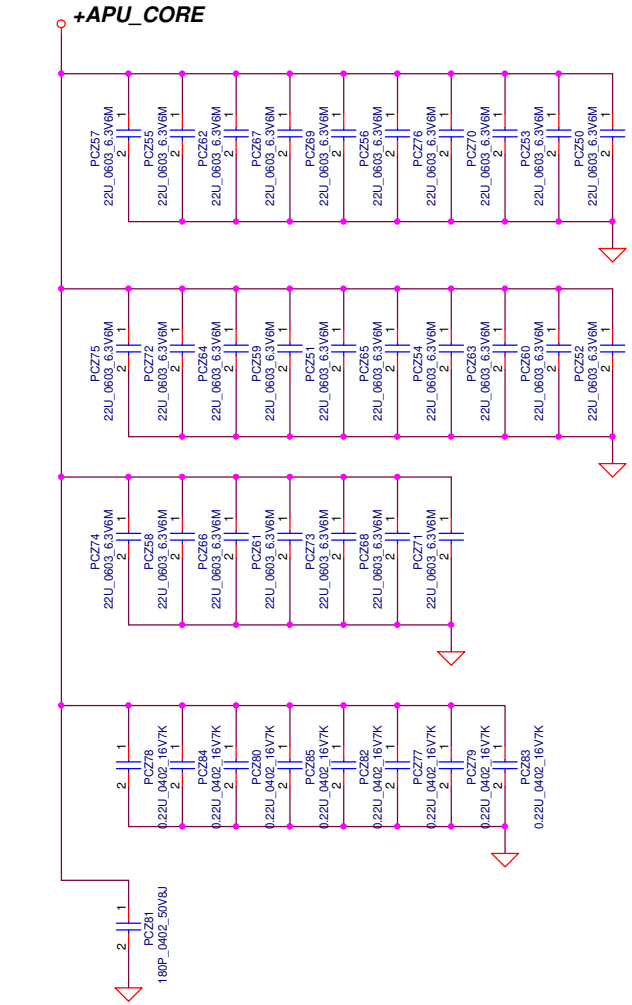
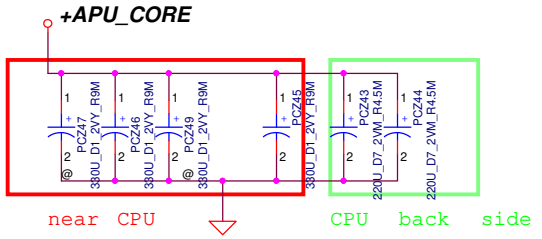
Issued Date	2020/03/29	Deciphered Date	2020/03/29

Compal Electronics, Inc.			
Title	PWR-CPU_CORE/CPU_CORE_NB		
Size: Custom	Document Number: EH5KP/AP_LA-H801P		Rev: 0.1
Date: Friday, March 29, 2019	Sheet 41 of 48		

+APU_CORE

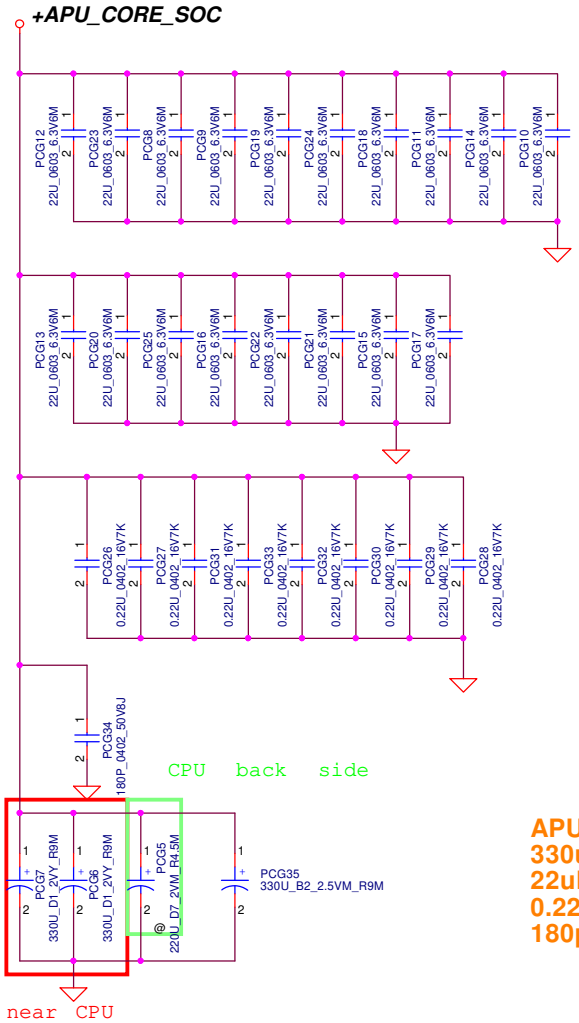




330u is common part SGA00009S00

APU_CORE
330uF*5
22uF*27
0.22uF*8
180pF*1

+APU_CORE_SOC



APU_CORE_SOC
330uF*2
22uF*18
0.22uF*8
180pF*1

330u is common part SGA00009S00

Security Classification	Compal Secret Data		
Issued Date	2020/03/29	Deciphered Date	2020/03/29

Compal Electronics, Inc.

Title: +APU_CORE Cap

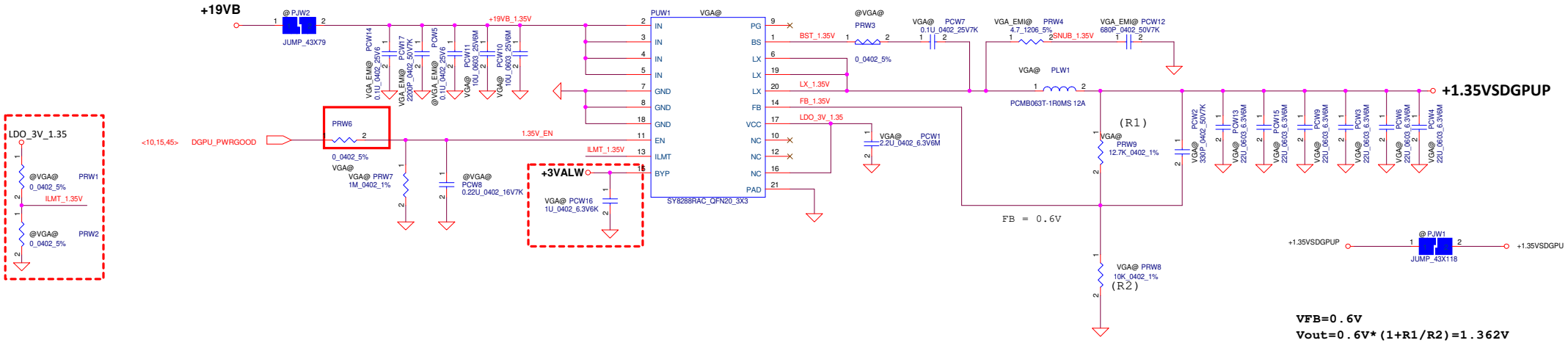
Size: Custom | Document Number: EH5KP/AP_LA-H801P | Rev: 0.1

Date: Friday, March 29, 2019 | Sheet 42 of 48

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2

Module model information

SY8208D_V1.mdd



VFB=0.6V
Vout=0.6V*(1+R1/R2)=1.362V

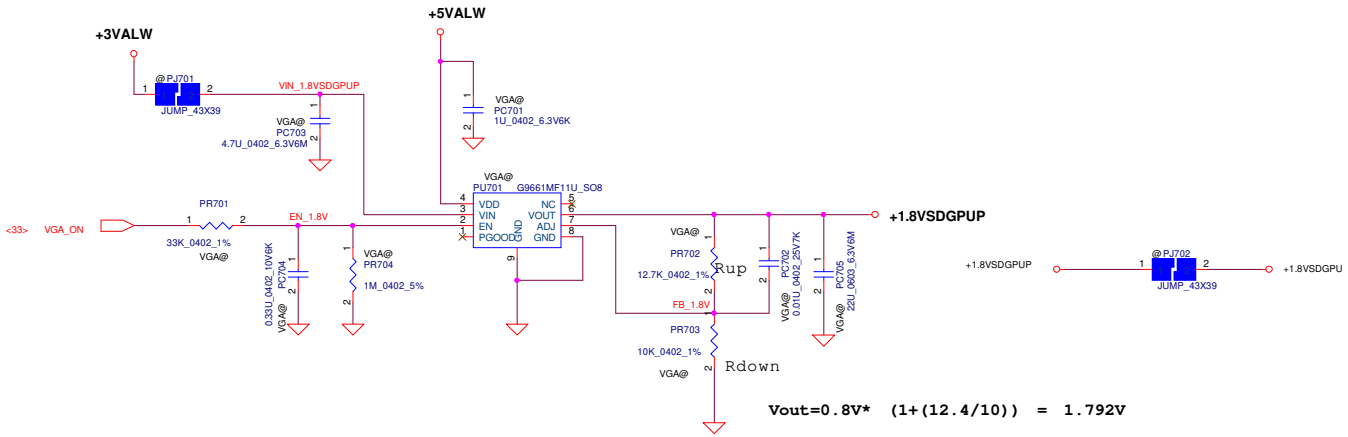
Security Classification	Compal Secret Data		
Issued Date	2020/03/29	Deciphered Date	2020/03/29

Compal Electronics, Inc.

Title: +GFX_CORE

Size	Document Number	Rev
Custom	EH5KP/AP_LA-H801P	0.1

Date: Friday, March 29, 2019 Sheet 43 of 48



Vout=0.8V* (1+(12.4/10)) = 1.792V

Vout=0.8V* (1+(12.7/10)) = 1.816V

Vout=0.8V* (1+(13/10)) = 1.84V

Security Classification	Compal Secret Data		
Issued Date	2020/03/29	Deciphered Date	2020/03/29

Compal Electronics, Inc.

Title: **RT8880CGQW**

Size	Document Number	Rev
		0.1

Date: Friday, March 29, 2019 | Sheet 44 of 48

Module model information

ISL62771_CZ_GFX35W_V3A.mdd for IC portion
ISL62771_CZ_GFX35W_V3B.mdd for SW portion

VR_ON
High > 1.6V
Low < 1V

PH1001 near APU_CORE_NB H/S mos

PH1002 near APU_CORE H/S mos
VRHOT Assert Threshold : 0.64V
TSENSE Bias Current : 30uA
PH1002=27.4K, 110C active
Reset Threshold: 0.66V, 98C active
110C Assert Threshold: PR1031=27.4K
100C Assert Threshold: PR1031=16.9K

PH1003 near GFX_CORE choke

PRV111 set 221 ohm to OCP 16A

PR1058=3.65K, PR1040=2.1K and
PR1046=604 to set loadline -2.1mV/A

PR1046 set 750 ohm to OCP 43.75A

SVD and SVC RC filter put VGA side.
SVT RC filter put controller side.

PRV22=768 to set loadline -0.6mV/A
while PRV8=619 to set OCP 82.5A

SH000011H00 (DCR:0.98mohm +/-5%)

GFX_core
TDC 30(1H1L)
Peak Current 45A
OCP current > 56A
Load line -2.1mV/A
FSW=400kHz
DCR 0.98mohm +/-5%

	TYP	MAX
H/S Rds(on)	:11.7mohm ,	14mohm
L/S Rds(on)	:2.7mohm ,	3.3mohm

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Issued Date	2020/03/29	Deciphered Date 2020/03/29	Title: PWR-CPU_GFX
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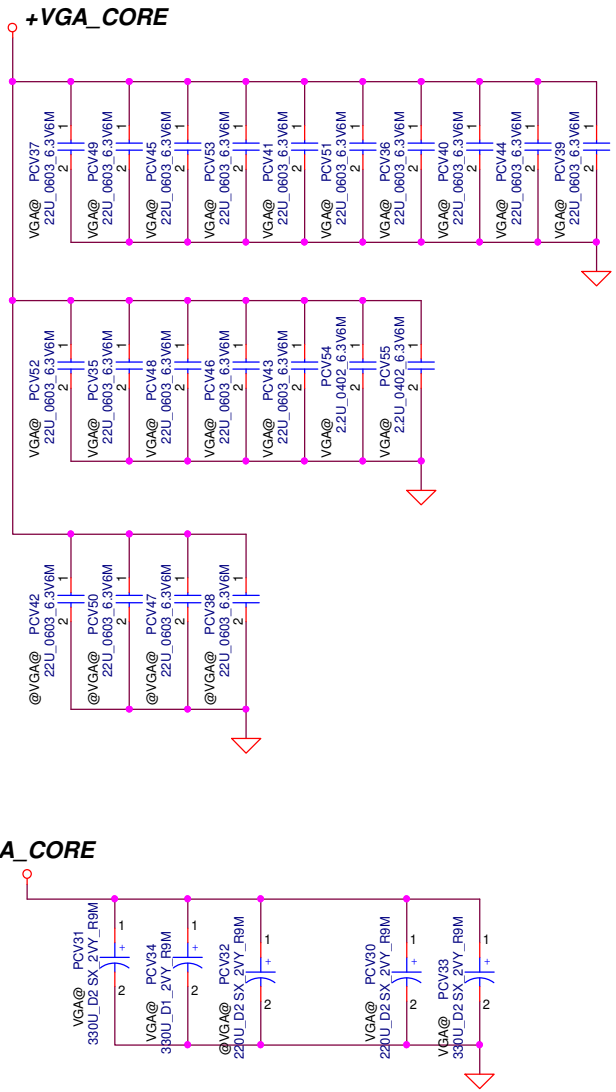
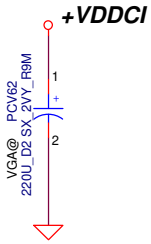
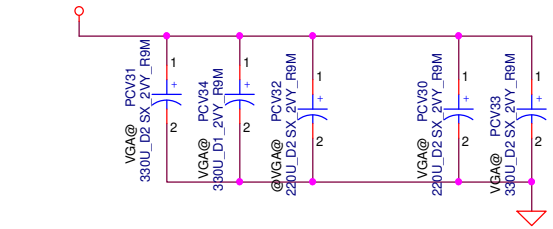
			Date: Friday, March 29, 2019 / Sheet 45 of 48







Security Classification	Compal Secret Data		
Issued Date	2020/03/29	Deciphered Date	2020/03/29

Compal Electronics, Inc.

Title: **VGA CORE CAP**

Size	Document Number	Rev
B	EH5KP/AP_LA-H801P	0.1

Date: Friday, March 29, 2019 Sheet 46 of 48

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01		CPU_CORE transient test		P41	<1>change bom: PRZ52 R0402_0OHMSD028000080-->0_0402_5%SD028000080 <2>Add & Smt: PRV45 PRV46 0_0402_5%SD028000080 <3>Add & unpop: PCZ89 PCZ90 PCZ91 C_0402SE00000F180 <4>Add & unpop: PCV63 PCV64 PCV65 C_0402SE00000F180 <5>Smt: PCZ43 220U_D7_2VM_R4.5MSGA0000AM00 <6>unpop: PCZ49 330U_D1_2VY_R9MSGA00009S00 <7>Add & Smt: PCG35 330U_B2_2.5VM_R9MSGA00007Z00 <8>change bom: PRZ15 732_0402_1%SD000001480->976_0402_1%SD000003280 <9>Smt: PRZ6 210K_0402_1%SD034210380 <10>Add & Smt: PCZ92 680P_0402_50V7KSE074681K80 <11>change bom: PRZ16 41.2K_0402_1%SD000009K00->34K_0402_1%SD034340280	20190201	EVT
02		VGA transient test & change to R-Short & 5V CHOKE Common Part			<1>PR101 PR217 PR210:0_0402_5% SD028000080->R0402_0ohm 0_0402_5% SD028000080 change to R-Short <2>PRB15 PRB17 PRB23 PRB26:0_0402_5% SD028000080 -> R0402_0ohm 0_0402_5% SD028000080 change to R-Short <3>PRB16 PR304 PRF1:0_0603_5% SD013000080 -> R0603_0ohm 0_0603_5% SD013000080 change to R-Short <4>PR502 PR505: 0_0402_5% SD028000080 -> R0402_0ohm 0_0402_5% SD028000080 change to R-Short <5>PRW3: 0_0402_5% SD028000080 -> R0402_0ohm 0_0402_5% SD028000080 change to R-Short <6>PCV31 PCV33: 220U 2V Y D2 SGA0000BT00 -> 330U 2V Y ESR9M SGA00009S00 BOM change <7>PCV32: 220U 2V Y D2 SGA0000BT00 -> Unpop BOM change <8>PL502: 7*7*3SH00000II00 -> 7*7*3 1.5uH SH000016700 BOM change->Common Part) <9>PC302 PC502 PCB11: 0.1U_0603_25V7K SE042104K80 ->0.1U_0402_25V7K SE00000W210 <10>PCW7: 0.1U_0603_25V7K SE042104K80 ->0.1U_0402_25V7K SE00000W210 <11>PCB1: 1000P_0603_50V7 SE025102K80 -> 1000P_0402_50V7K SE074102K80	20190212	EVT
03		CPUtransient test			PRZ26_137K_0402_1%_SD034137380_->_38.3K_0402_1%_SD034383280 PRZ6_210K_0402_1%_SD034210380_->_41.2K_0402_1%_SD000009K00 PRZ14_137K_0402_1%_SD034137380_->_28.7K_0402_1%_SD034287280 PCZ47_330U_D1_2VY_R9M_SGA00009S00_->UnPOP	20190325	DVT
13							
14							
15							
16							
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Version Change List (P. I. R. List)

Item	Page#	Date	Request Owner	Issue Description	Solution Description	Rev.
1		11/07				0.1
2		01/22		01.PCIE_CLK port change Port1=GPU Port2=LAN Port4=WLAN 02.Q18 change PN to SB000014T00 for EOL 03.U4 change PN to SB00001IY00 for EOL 04.USB Port0/Port4 swap 05.UG2,UG3 change to @ 06.RG12 change to pop 07.R1562 change to pop 08.JFP1 pin define reverse 09.R291 add to HUB@ for disable port 2 10.Combine power 11.R4042 remove, JIO2.14/15/16 change to +5VALW		
		01/24		01.OVCUR#1 change to PD with @ 02.R4042 add with @		1.0
		01/25		01.UC1 add Athlon APU PN (SA0000CFE40).		
		01/29		01.R4042 change to connect to GND.		
		01/31		01.Combine Power SCH.		
		02/01		01.Combine Power SCH.		
		02/12		01.R4040,R4041,C2771,C2772 change to pop 02.R4044,R4045 add to pop		
		02/13		01.Combine Power SCH.		
		02/15		01.Combine Power SCH. 02.CV450,CV451 change to 15pF (SE071150J80) 03.CL20,CL21 change to 12pF (SE071120J80) 04.RC6170 change to pop, RC6171 change to @ 05.PCB DAZ PN (DAZ2MK00100) add into SCH.	
3		03/12		(1)EGPIO108 add RC6177 with @ PU-10k (2)UG2,RG13 change to pop ; UG1,RG12 change to @ (3)UL2.28/29 swap net name (4)RL5 change to 1k.		
		03/18		(1)JIO1 update Symble (SP01001Y800).		
		03/19		(1)RL5 change to 0-ohm (2)RC616,RC617 change to R-short (3)RV1650 change to R-short (4)RV506 change to R-short (5)R1667,R1669 change to 0-ohm (6)R756,R765,R769,R779,R781,R782,R783,R794 change to R-short	1.A
		03/25		(1)Combine PWR SCH. (2)R1564 change to 15K_0402_1%		
		03/26		(1)remove AGPIO8 connection (2)UM1,RM23 add to SSD RST# sequence (3)RM18 change to 0 ohm (4)Add -NPM to L2512,L2513,L2514,L2515		
		03/28		(1)RC1677 change to pop (2)RC6147 change to DIS@,RC6148 change to UMA@		
		03/29		(1)C288,C289,C290,C291,C293,C294,R269 change to pop without HUB@		

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