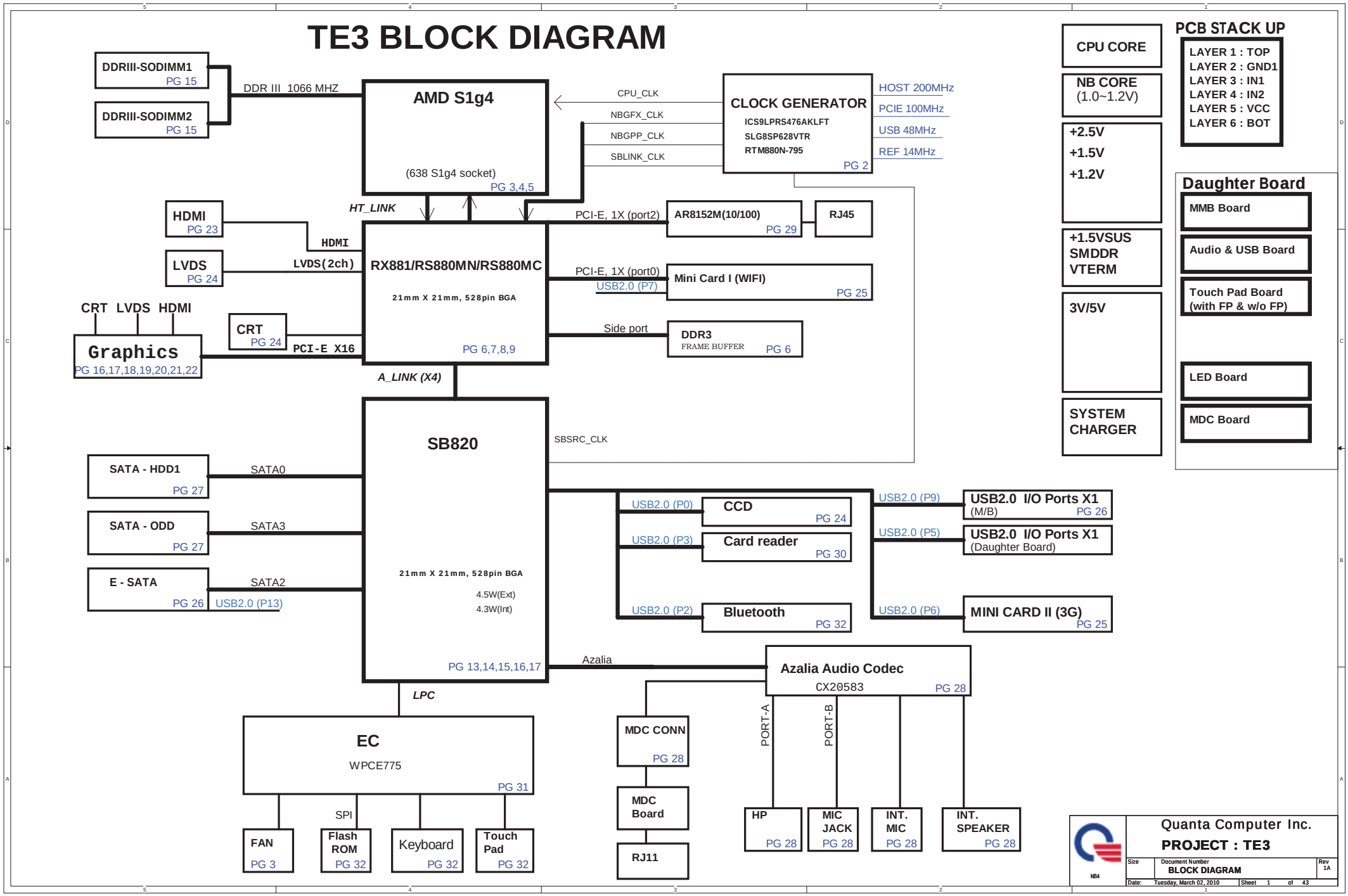
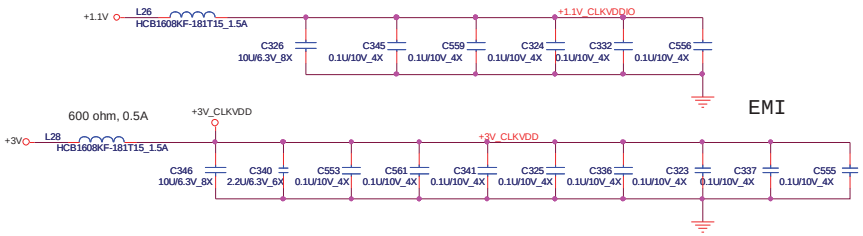
TE3 BLOCK DIAGRAM

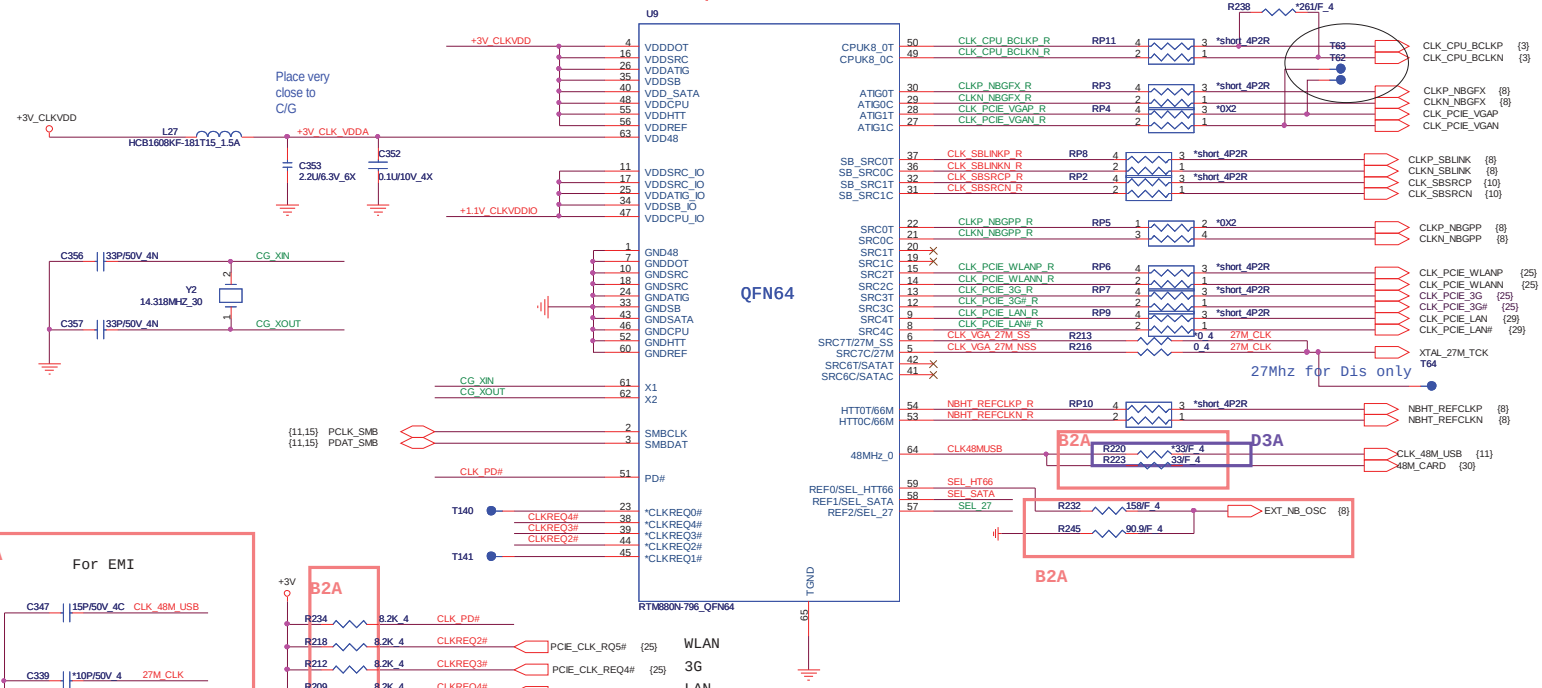


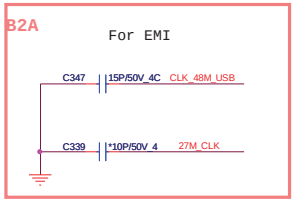
CLOCK GENERATOR

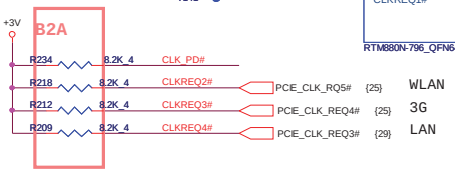
CLOCKS name	Discrete	Clock pin function
NBGFX_CLKP NBGFX_CLKN	RP48 STUFF	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP47 STUFF	to Park-S3 external reference clock -Discrete only
SBLINK_CLKP SBLINK_CLKN	RP43 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_SS CLK_VGA_27M_NSS	R213, R215 STUFF	To Park-S3 27Mhz - Discrete only

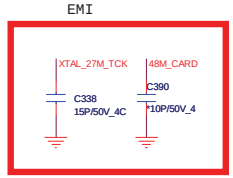


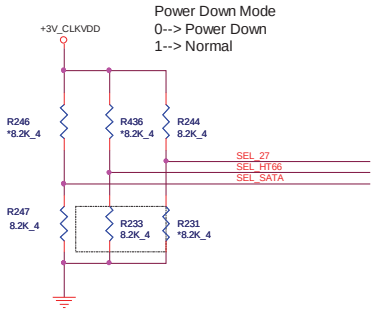
Need check the net name for the short pad











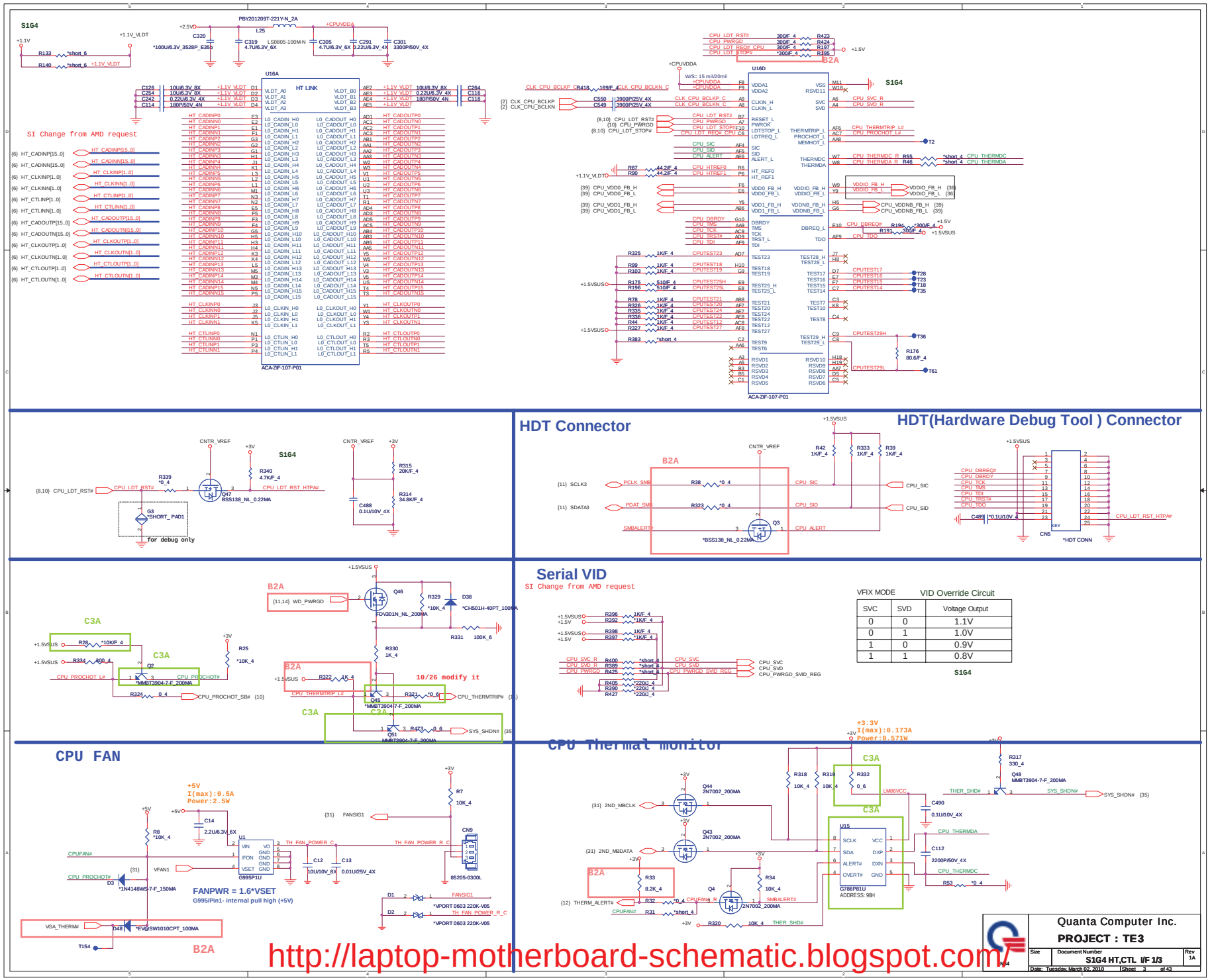
* default

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0 *	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0 *	100 MHz spreading differential SRC clock
SEL_27	1 *	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock

Quanta Computer Inc.
PROJECT : TE3

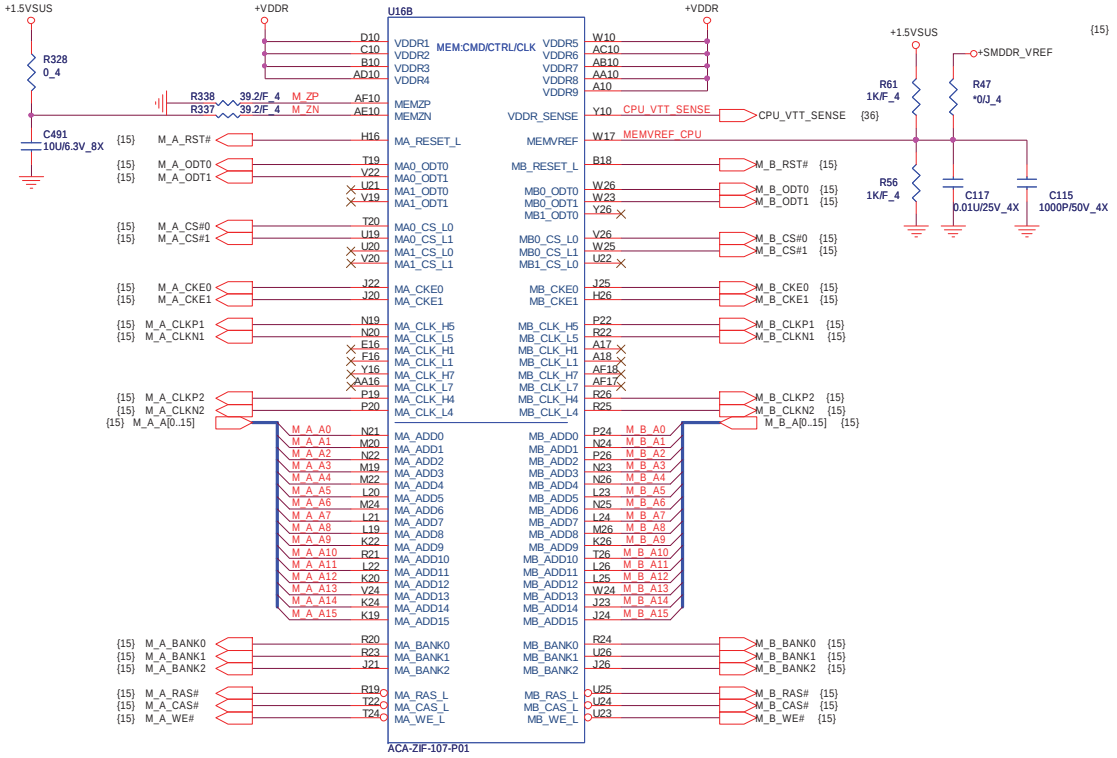
Size	Document Number	Rev
	Clock Generator	1A
Date: Thursday, March 04, 2010	Sheet 2 of 43	

NB4

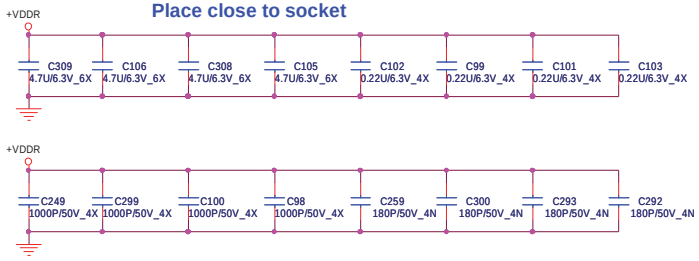


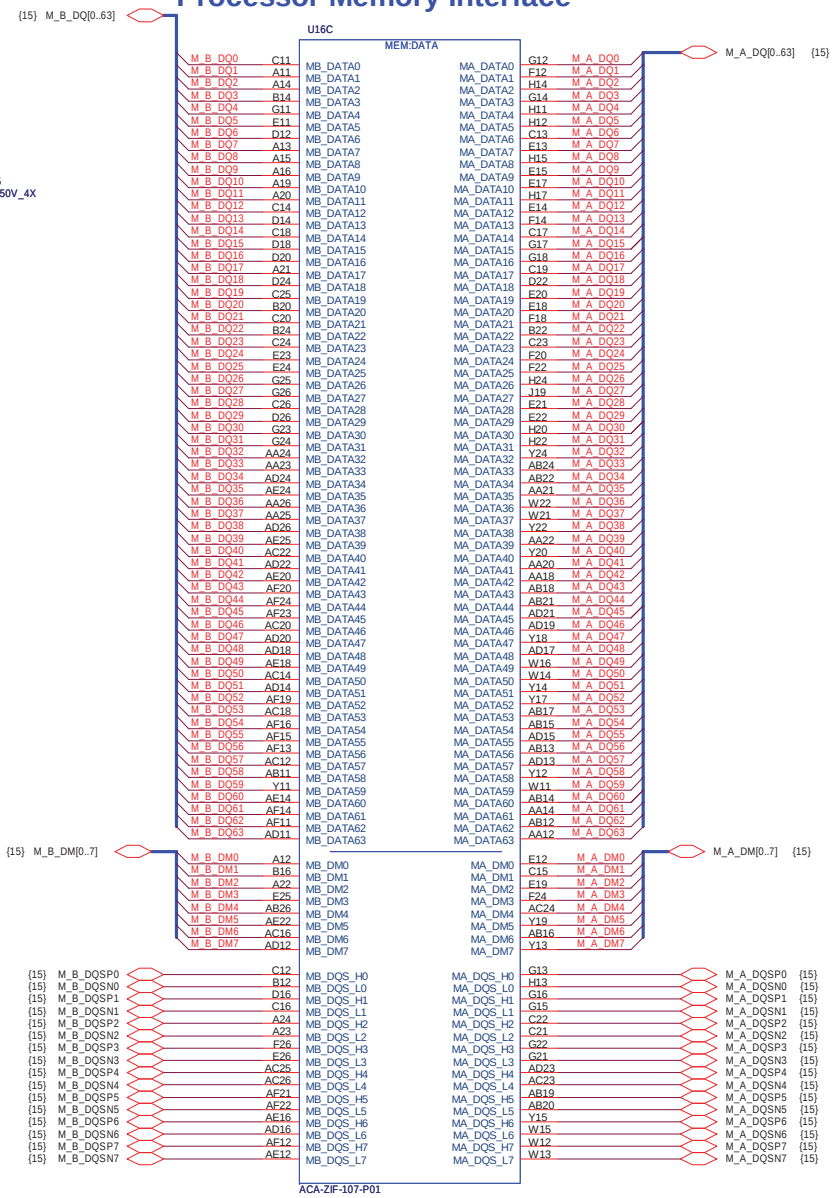
Processor Memory Interface

0.9V@1.5A



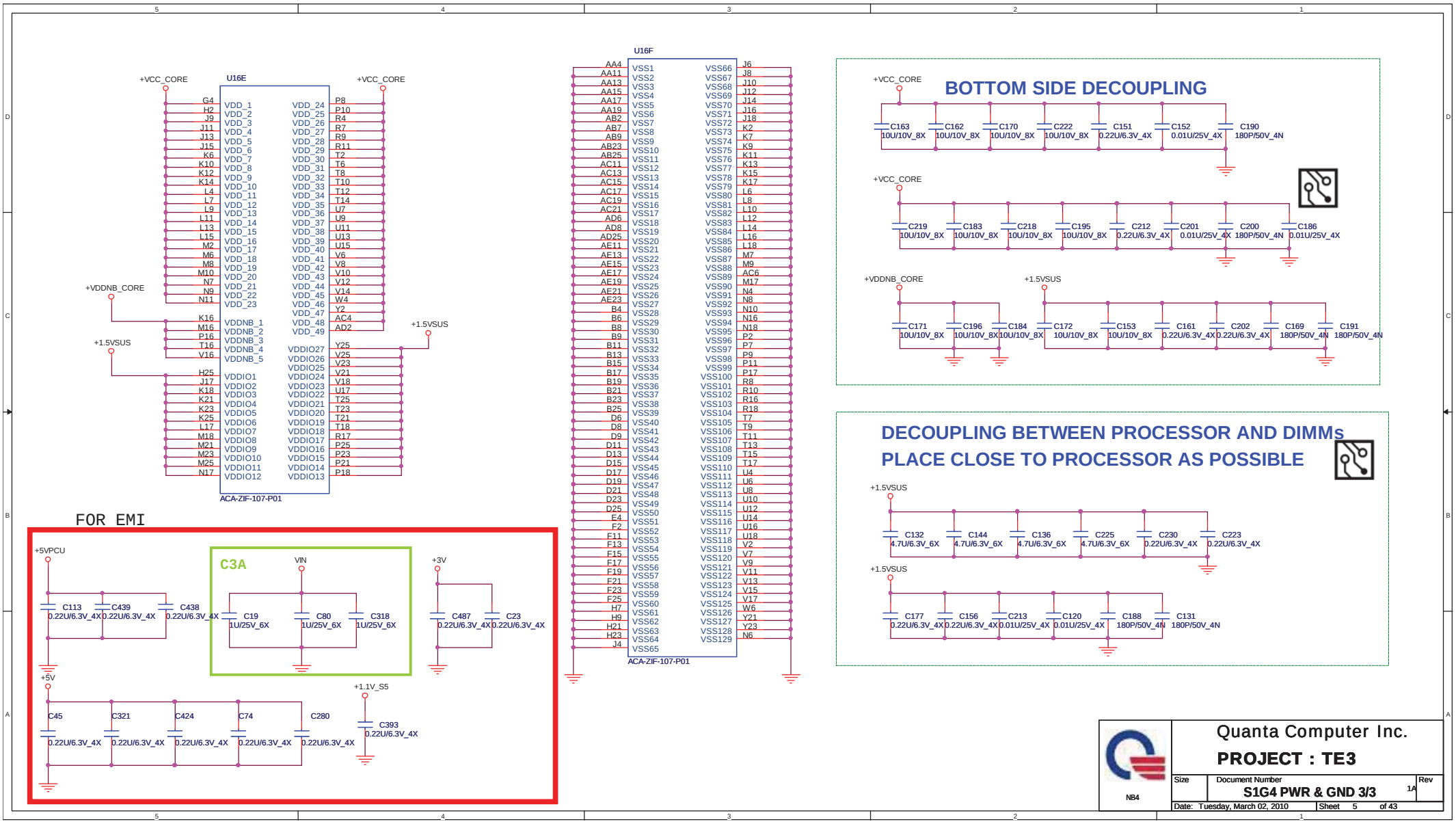
Place close to socket

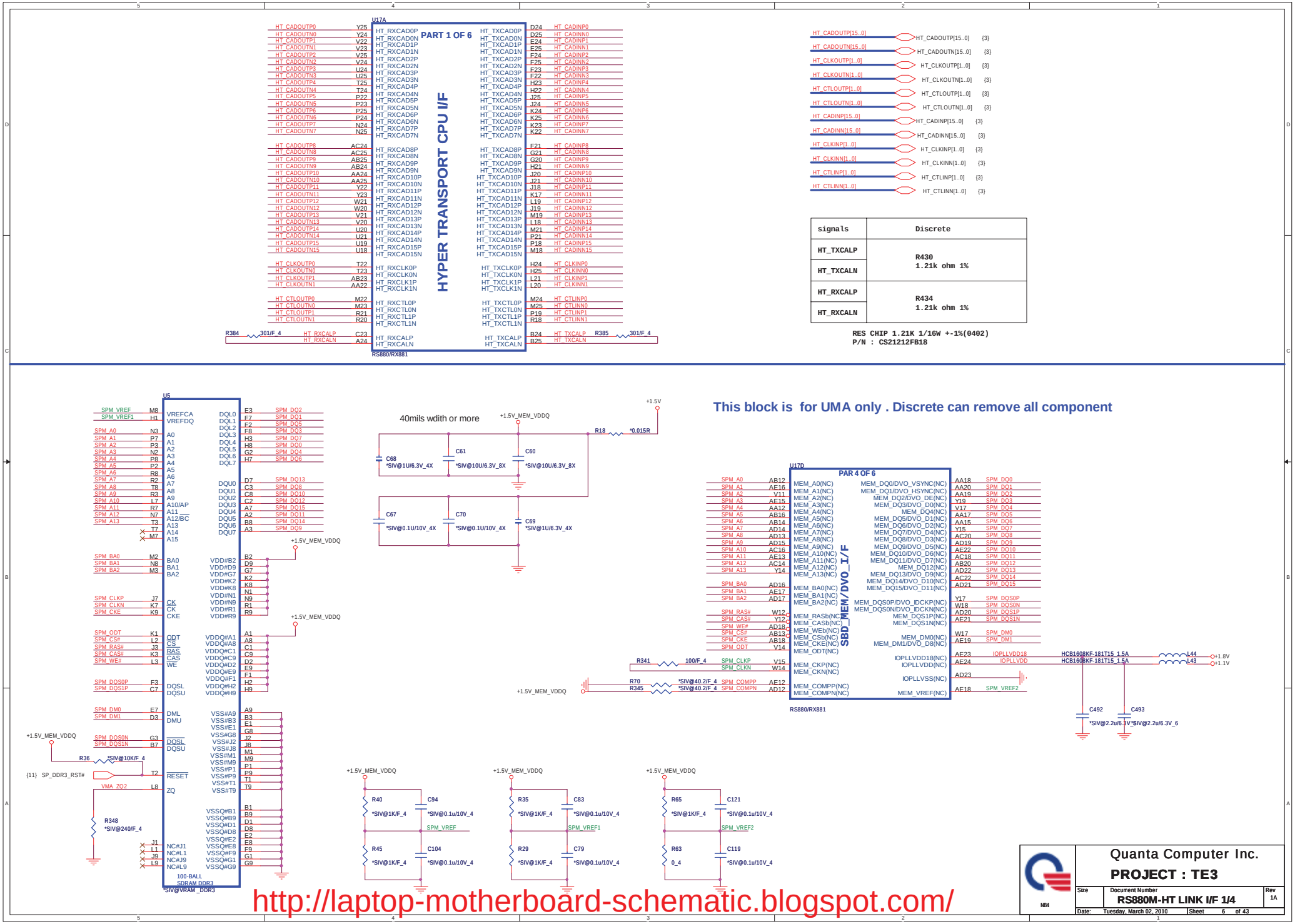


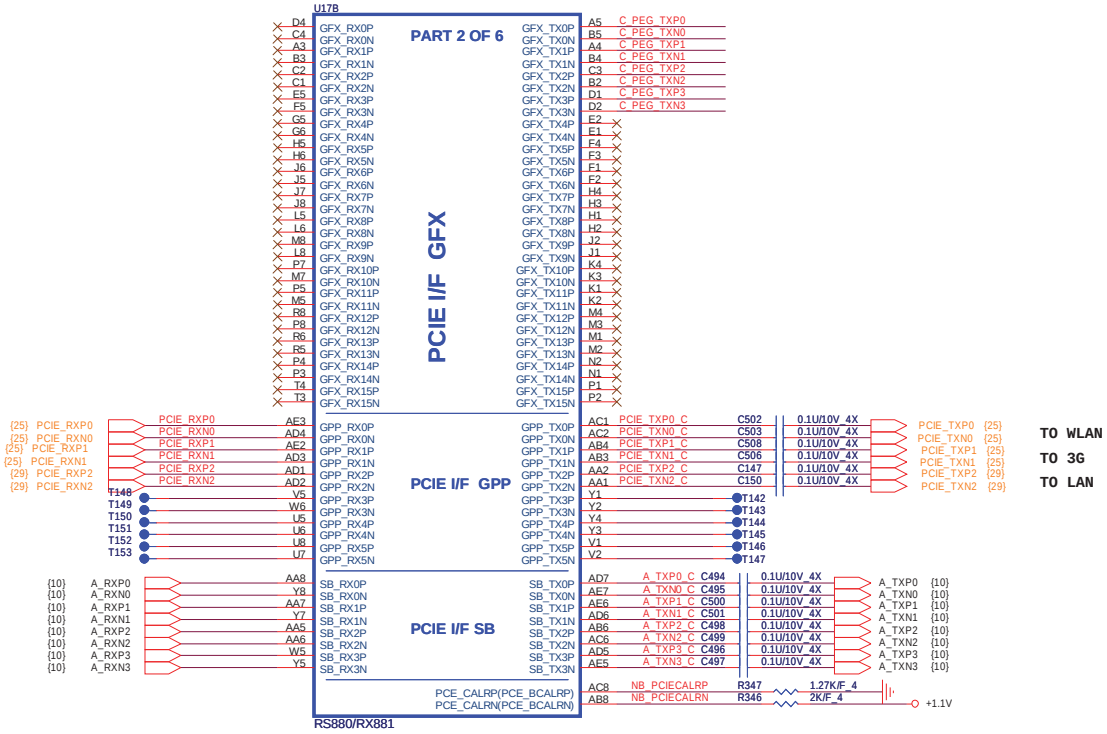


Quanta Computer Inc.			
PROJECT : TE3			
Size	Document Number		Rev
	S1G4 DDR MEMORY I/F 2/3		1A
Date: Tuesday, March 02, 2010		Sheet 4 of 43	

NB4







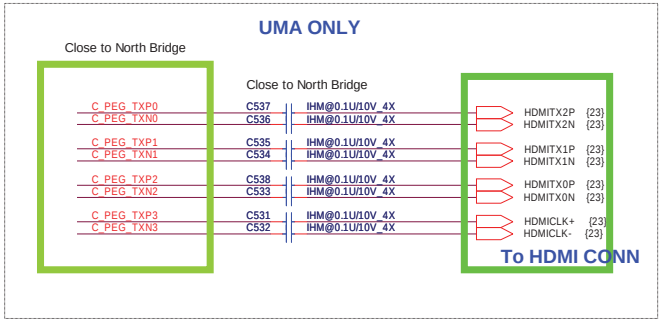
RS880 Display Port Support (muxed on GFX)

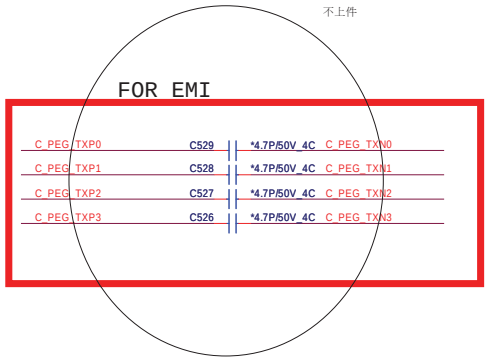
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

NOTE:
RS880MC no support Graphic / HDMI / DP

BOM Option Table

Reference	Description
IHM@	INT VGA & HDMI
IDP@	INT VGA & DP
EV@	EXT VGA





Quanta Computer Inc.
PROJECT : TE3

Size	Document Number	Rev
	RS880M-PCIE I/F 2/4	1A

Date: Tuesday, March 02, 2010 Sheet 7 of 43

RX780: Powered from the 1.8-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.
RS780: Powered from the 3.3-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA
IHM@	INT VGA & HDMI
IDP@	INT VGA & DP
ICRT@	INT VGA & CRT

[CLG]
[CLG]-IV@
[CRT]-ICRT@

RX881 {3,10} CPU_LDT_RST# R388 *0_4 NB_RST#_IN
RS880 {10,25,29,30,31} PLTRST# R401 0_4

North Bridge RESET

For Internal clock mode ONLY

R365 *4.7K_4 CLKP_NBGFX
R362 *4.7K_4 CLKN_NBGFX

RS880 Mobile Platforms: Two-level voltage scaling solution used; Pulled down through a 2-k? 5% resistor and connected to the Northbridge core power supply (circuit.don't need to do something for the RX881)

RX881

NB_CORE_ON R403 *10K/F_4 +3V
R402 2.2K_4

RS880

Debug Bus
0-->Enable
1-->Disable
INT_VSYNC R387 3K/F_4 +3V
R395 *3K/F_4

Sideport Enable
0-->Enable
1-->Disable
INT_HSYNC R386 3K/F_4 +3V
R394 *3K/F_4

EEPROM Strap
0-->Enable
1-->Disable
SUS_STAT# R138 3K/F_4 +3V
R148 *3K/F_4

U17C
PART 3 OF 6
RS880/RX881

CRT/TVOUT
110mA
AVDD1(NC) AVDD2(NC) AVDDD1(NC) AVSSDI(NC) AVDDQ(NC) AVSSQ(NC)
+3V_AVDD_NB
C_Pr(DFT_GPIO5) Y(DFT_GPIO2) COMP_Pb(DFT_GPIO4)
RED(DFT_GPIO0) REDb(NC) GREEN(DFT_GPIO1) GREENb(NC) BLUE(DFT_GPIO3) BLUEb(NC)
{24} CRT_RED R96 140/F_4
{24} CRT_GRE R107 150/F_4
{24} CRT_BLU R113 150/F_4
Length within 1"
DAC_HSYNC(PWM_GPIO4) DAC_VSYNC(PWM_GPIO6) DAC_SDA(PCE_TCALRN) DAC_SCL(PCE_RCALRN)
{24} CRT_HSYNC {24} CRT_VSYNC {24} CRT_DDCDAT {24} CRT_DDCCLK
INT_HSYNC INT_VSYNC INT_CRT_DDCDAT INT_CRT_DDCCLK
DAC_RSET(PWM_GPIO1)
R136 715/F_6 DAC_RSET_NB

PLL PWR
20mA
+1.8V_AVDDDI_NB
4mA
+1.8V_AVDDQ_NB
65mA
PLLVDD(NC) PLLVDD18(NC) PLLVSS(NC)
+1.1V_PLLVDD +1.8V_PLLVDD18
20mA
VDDA18HTPLL
+1.8V_VDDA18HTPLL
120mA
VDDA18PCIEPLL1 VDDA18PCIEPLL2
+1.8V_VDDA18PCIEPLL

LVTM
15mA
VDDLTP18(NC) VSSLTP18(NC)
+1.8V_VDDLTP18_NB
300mA
VDDLT18_1(NC) VDDLT18_2(NC) VDDLT33_1(NC) VDDLT33_2(NC)
+1.8V_VDDLT18_NB +3V_VDLT33_NB
VSSLT1(VSS) VSSLT2(VSS) VSSLT3(VSS) VSSLT4(VSS) VSSLT5(VSS) VSSLT6(VSS) VSSLT7(VSS)

PM
SYSRESETb POWERGOOD LDTSTOPb ALLOW_LDTSTOP
{14} NB_PWRGD_IN
NB_RST#_IN NB_PWRGD_IN NB_LDT_STOP# NB_ALLOW_LDTSTOP

CLOCKs
HT_REFCLKP HT_REFCLKN
{2} NBHT_REFCLKP {2} NBHT_REFCLKN
NBHT_REFCLKP NBHT_REFCLKN
REFCLK_P/OSCIN(OSCIN) REFCLK_N(PWM_GPIO3)
{2} EXT_NB_OSC
R139 *short_4 NB_REFCLK_P
R122 *short_4 NB_REFCLK_N
+1.1V R151 4.7K_4 RS880 RS880 R150 4.7K_4
CLKP_NBGFX CLKN_NBGFX
GFX_REFCLKP GFX_REFCLKN I/O
{2} CLKP_NBGFX {2} CLKN_NBGFX {2} CLKP_NBGPP {2} CLKN_NBGPP {2} CLKP_SBLINK {2} CLKN_SBLINK
GPP_REFCLKP GPP_REFCLKN I/O
GPPSB_REFCLKP(SB_REFCLKP) GPPSB_REFCLKN(SB_REFCLKN)

MIS.
I2C_DATA I2C_CLK DDC_DATA/AUXDN(NC) DDC_CLK/AUX0P(NC) AUX1P(NC) AUX1N(NC)
{24} LCD_EDIDDATA {24} LCD_EDIDCLK {23} HDMI_DDCDAT {23} HDMI_DDCCK
LCD_EDIDDATA LCD_EDIDCLK HDMI_DDCDAT HDMI_DDCCK
T39 T41
{37} NB_CORE_ON NB_CORE_ON
STRP_DATA
RSVD
R125 150/F_4 RS780_AUX_CAL AUX_CAL(NC)

TXOUT_L0P(NC) TXOUT_L0N(NC) TXOUT_L1P(NC) TXOUT_L1N(NC) TXOUT_L2P(NC) TXOUT_L2N(DBG_GPIO0) TXOUT_L3P(NC) TXOUT_L3N(DBG_GPIO2)
LCD_TXLOUT0+ {24} LCD_TXLOUT0- {24} LCD_TXLOUT1+ {24} LCD_TXLOUT1- {24} LCD_TXLOUT2+ {24} LCD_TXLOUT2- {24}
T124 T123
TXOUT_U0P(NC) TXOUT_U0N(NC) TXOUT_U1P(PCIE_RESET_GPIO3) TXOUT_U1N(PCIE_RESET_GPIO2) TXOUT_U2P(NC) TXOUT_U2N(NC) TXOUT_U3P(PCIE_RESET_GPIO5) TXOUT_U3N(NC)
T125 T121
TXCLK_LP(DBG_GPIO1) TXCLK_LN(DBG_GPIO3) TXCLK_UP(PCIE_RESET_GPIO4) TXCLK_UN(PCIE_RESET_GPIO1)
LCD_TXLCLKOUT+ {24} LCD_TXLCLKOUT- {24}
LVDS_DIGON(PCE_TCALRP) LVDS_BLON(PCE_RCALRP) LVDS_ENA_BL(PWM_GPIO2)
LVDS_DIGON {24} LVDS_BKL_PWM LVDS_BKL_EN
R393 *1.27K/F_4 R102 1.27K/F_4 R134 *1.27K/F_4
TMDS_HPD(NC) HPD(NC)
HDMI_HPD_R R137 *short_4 INT_HDMI_HPD {23}
TVCLKIN(PWM_GPIO5)
SUS_STAT#_NB R146 *short_4 SUS_STAT# {11}
THERMALDIODE_P THERMALDIODE_N
R_NB_THRMDA R_NB_THRMDC T84 T82
R147 *3K/J_4
TESTMODE
D13 TEST_EN R144 1.8K/F_4

C3A
+3V +15V
R186 *10K_4 R190 *10K_4
NB_LCD_CONTROL
Q14 *2N7002_200MA
NB_PWRGD_IN Q9 *BSS138_NL_0.22MA
VGS-TH<1.7V
support Vari-bridge,PWM duty cycle controlled by RS780M. Stuff Q22,R149.
NB_LCD_CONTROL
LVDS_BKL_EN Q12 *FDV301N_NL_200MA LVDS_BRIGHT {24}
R169 *4.7K_4
NB_LCD_CONTROL
LVDS_BKL_PWM Q13 *FDV301N_NL_200MA INT_LVDS_PWM {24}
R170 *4.7K_4
LVDS_BKL_EN R469 0_4 LVDS_BRIGHT {24}
LVDS_BKL_PWM R470 0_4 INT_LVDS_PWM {24}

RX881 PULL DOWN TO GND

at least 15 mil wide near source
L16 PBY160808T-221Y-N_2A +3V_AVDD_NB
C271 2.2U/6.3V_6X C20 10U/10V_8X
AVDD-DAC Analog not applicable to RX880

at least 15 mil wide
L46 PBY160808T-221Y-N_2A +1.1V_PLLVDD
C539 2.2U/6.3V_6X
PLLVDD - Graphics PLL not applicable to RX880

at least 15 mil wide
L17 PBY160808T-221Y-N_2A +1.8V_PLLVDD18
C298 10U/6.3V_8X C270 2.2U/6.3V_6X
PLLVDD18 - Graphics PLL not applicable to RX880

at least 15 mil wide
R153 0_6 +1.8V_AVDDDI_NB
C273 0.1U/10V_4X C21 10U/10V_8X
AVDDI-DAC Digital not applicable to RX880

L18 PBY160808T-221Y-N_2A +1.8V_AVDDQ_NB
C272 2.2U/6.3V_6X C22 10U/10V_8X
AVDDQ-DAC Bandgap Reference not applicable to RX880

at least 15 mil wide
L47 PBY160808T-221Y-N_2A +1.8V_VDDLTP18_NB
C540 2.2U/6.3V_6X
VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX880

L49 PBY201209T-121Y-N_3A +1.8V_VDDLT_18_NB
C543 4.7U/6.3V_6X C542 0.1U/10V_4X
VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX880

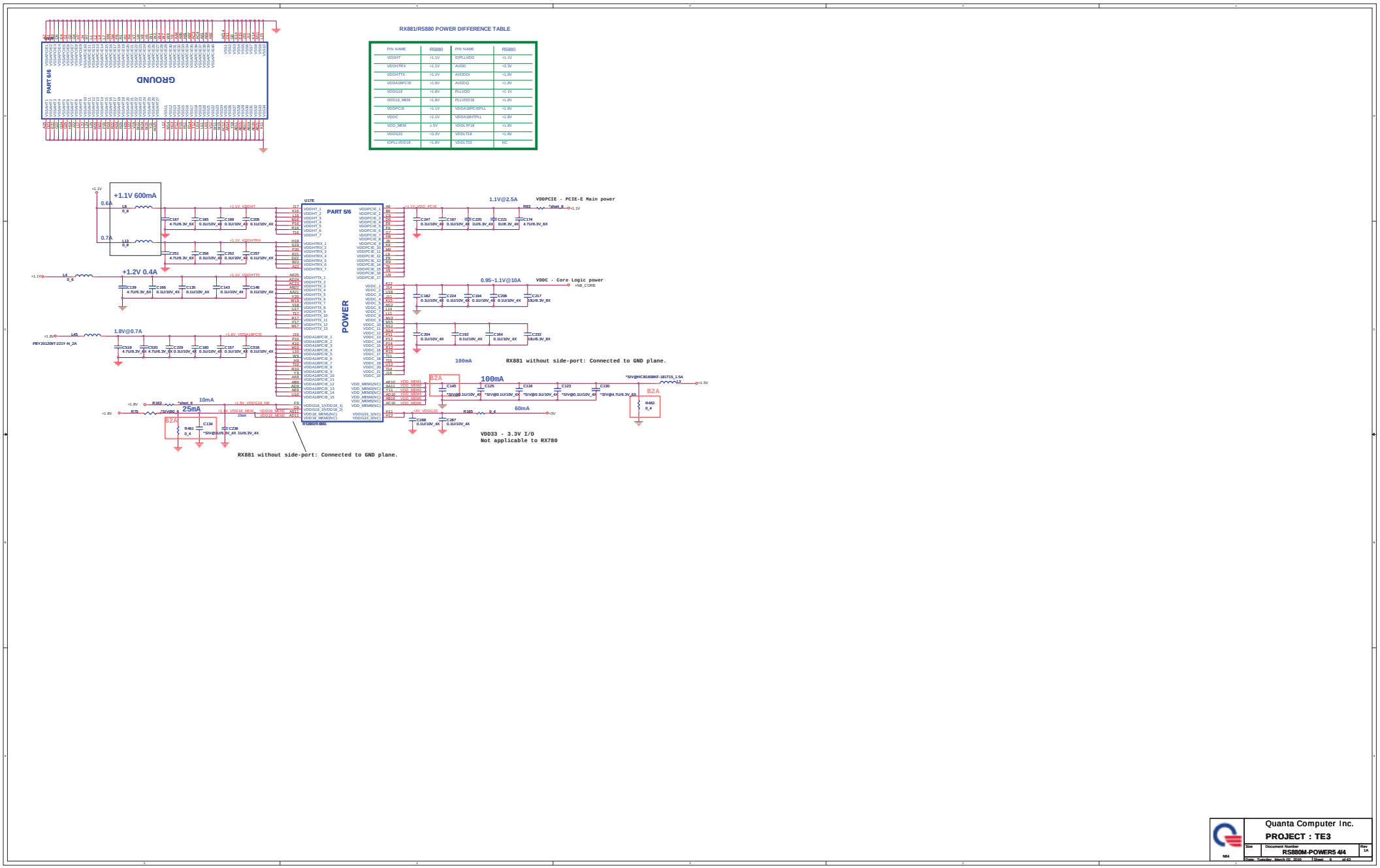
VDDA18PCIEPLL -PCIE PLL at least 15 mil wide
L11 20mils width +1.8V_VDDA18PCIEPLL PBY160808T-221Y-N_2A
C243 2.2U/6.3V_6X

VDDA18HTPLL -HT LINK PLL
L19 20mils width +1.8V_VDDA18HTPLL PBY160808T-221Y-N_2A
C274 2.2U/6.3V_6X

RS880
Q10 BSS138_NL_0.22MA {3,10} CPU_LDT_STOP# R166 2.2K_4 NB_LDT_STOP#
R167 *0_4
Q11 *BSS138_NL_0.22MA R404 1K_4 NB_ALLOW_LDTSTOP
R168 *0_4

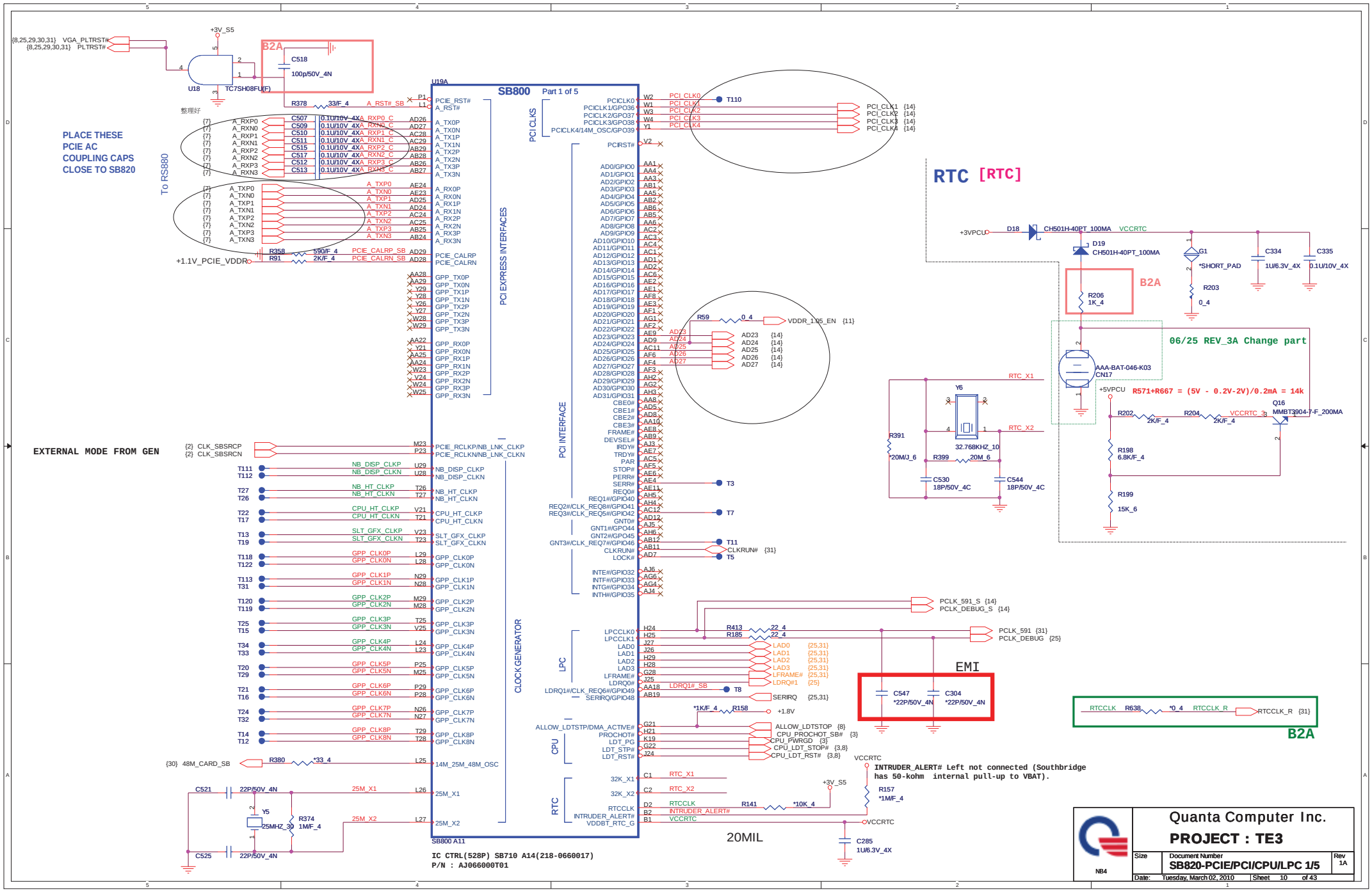
RX880 R182 *short_6 +VDDG_NB
RS880 R183 *0_6 +3V
at least 15 mil wide
L48 +3V_VDLT33_NB
*BLM21PG221SN1D_8 C541 *2.2u/6.3V_6

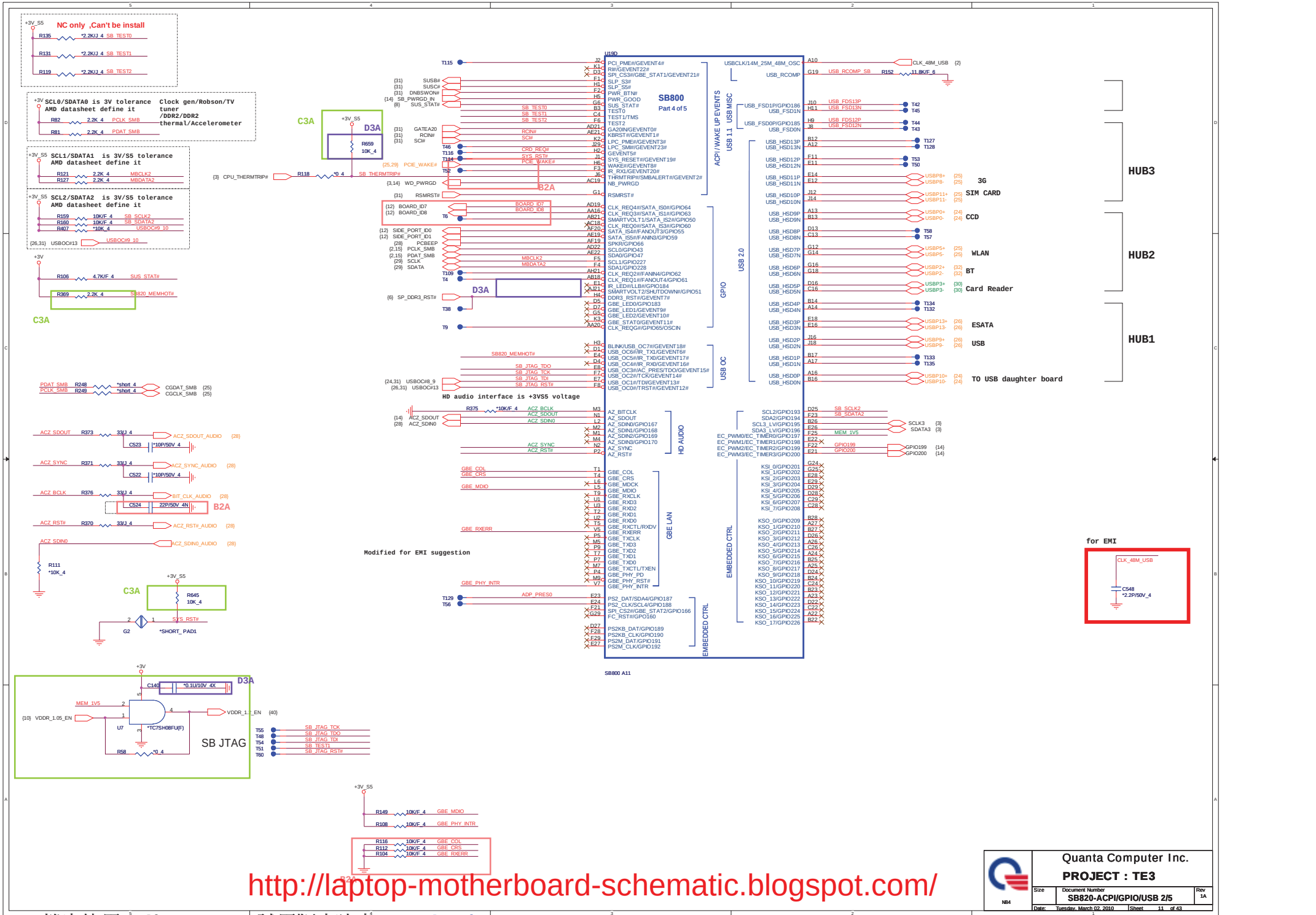
Quanta Computer Inc.
PROJECT : TE3
Size: NB4 | Document Number: RS880M-SYSTEM I/F 3/4 | Rev: 1A
Date: Tuesday, March 02, 2010 | Sheet 8 of 43



PIN NAME	RS880	PIN NAME	RS880
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC

Quanta Computer Inc.
PROJECT : TE3
RS880M-POWER5 4/4





Quanta Computer Inc.	
PROJECT : TE3	
Size	Document Number: SB820-ACPI/GPIO/USB 2/5 — Rev: 1A
Date: Tuesday, March 02, 2010	Sheet 11 of 43

SATA PORT 0,1,2,3
can support AHCI
mode

SATA HDD

E-SATA

SATA ODD

U19B

SB800
Part 2 of 5

SERIAL ATA

FLASH

HW MONITOR

SPI ROM

SB800 A11

PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB820

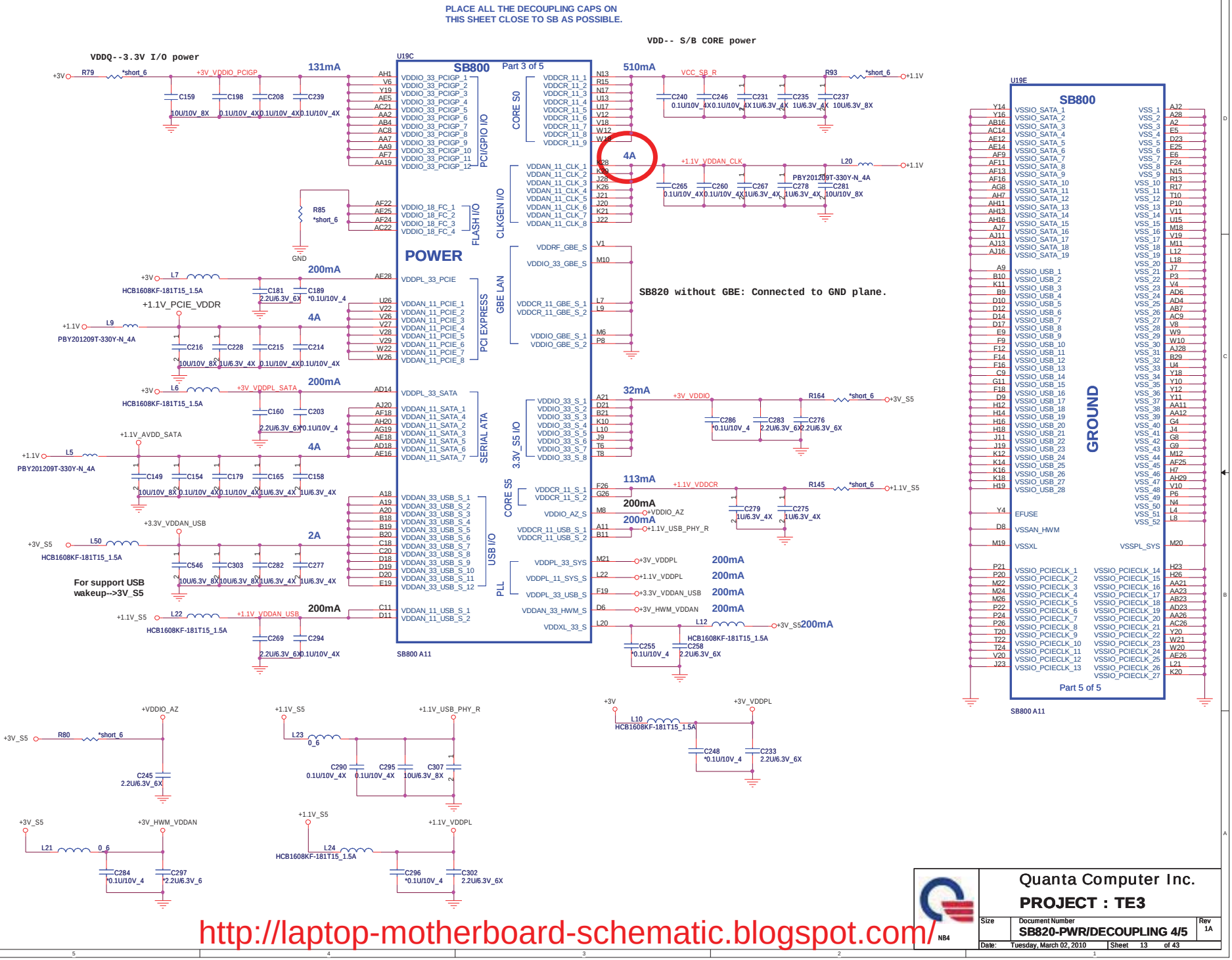
IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

ID1	ID0	Function
0	0	Samsung
0	1	Hynix
1	0	Reserve
1	1	No sideport support

BOARD ID SETTING

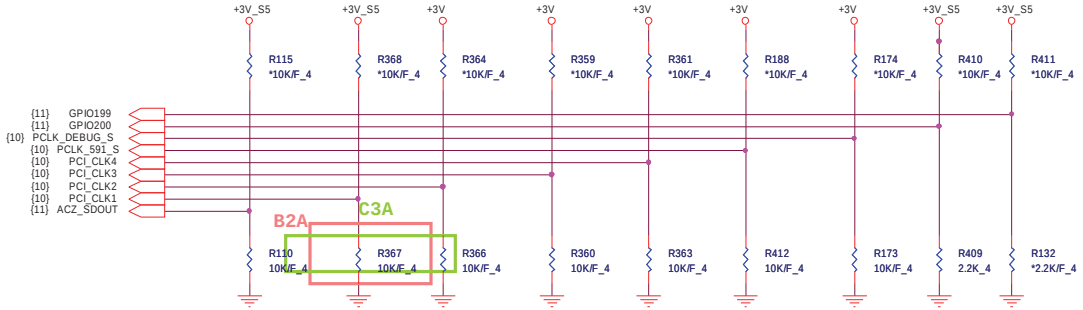
Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8
UMA SKU VGA SKU	H L							
W/ MDC W/O MDC		H L						
W/ HDMI W/O HDMI			H L					
W/O 3G W/ 3G				H L				
15" 14"					H L			
W/O BT W/ BT						H L		
13W 17W							H L	
W/ CF W/O CF								H L

Quanta Computer Inc.
PROJECT : TE3
Size | Document Number: SB820-SATA/IDE/HWM/SPI 3/5 | Rev: 1A
Date: Tuesday, March 02, 2010 | Sheet 12 of 43



REQUIRED STRAPS

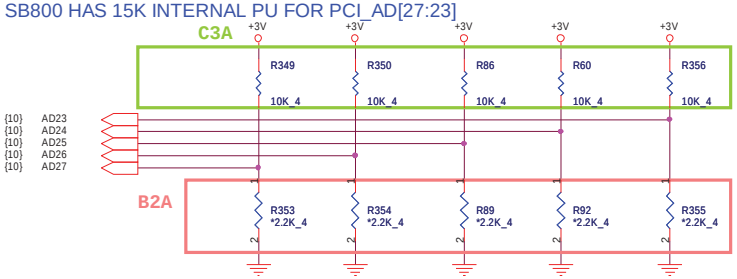
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 (PWM3) GPIO199 (PWM2)
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	GPIO199 (PWM2) GPIO200 (PWM3) H, H=Reserved H, L=SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L, H=LPC ROM DEFAULT L, L=FWH ROM

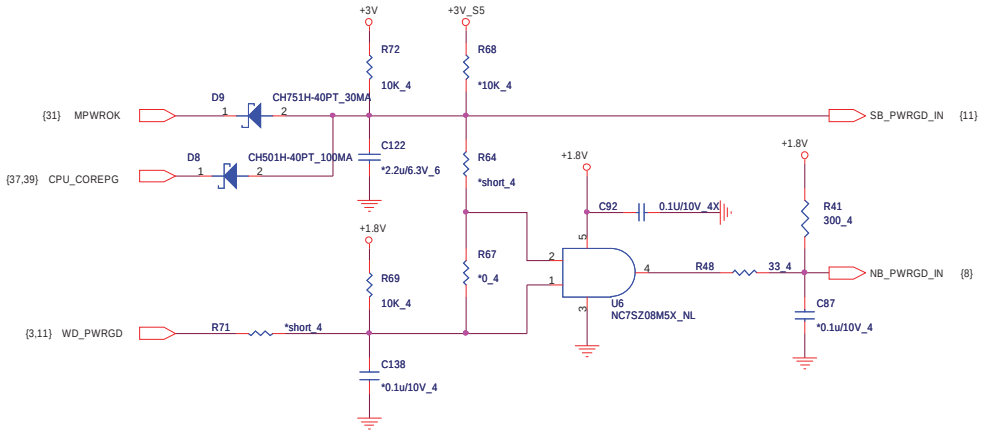
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

NB/SB POWER GOOD CIRCUIT



Quanta Computer Inc.

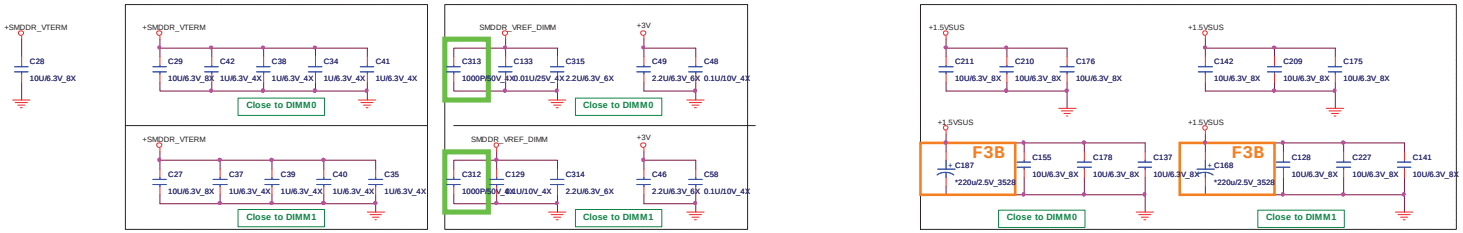
PROJECT : TE3

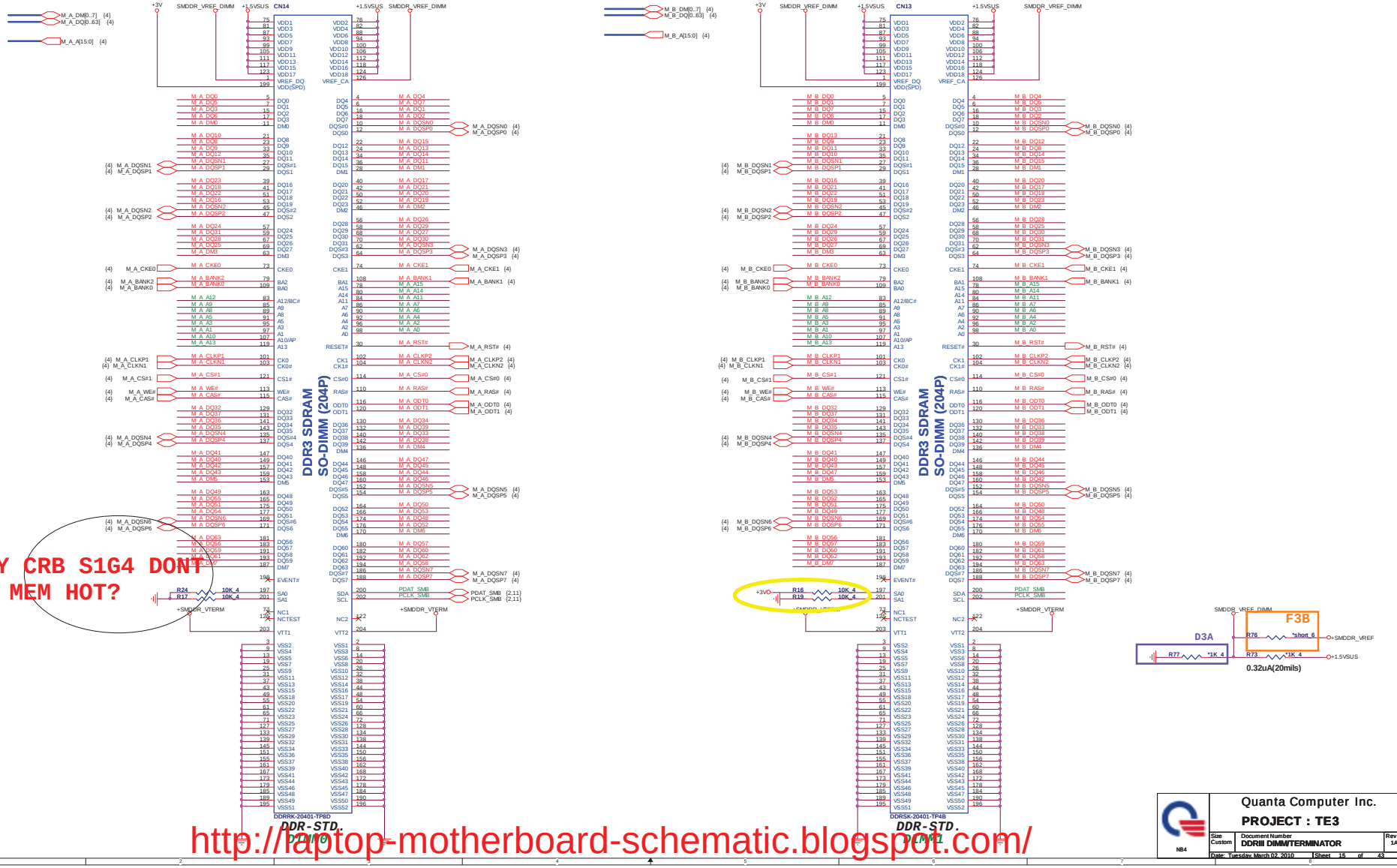
Size	Document Number	Rev
	SB820-STRAPS 5/5	1A
Date: Tuesday, March 02, 2010	Sheet 14 of 43	

DDRIII

TERMINATOR DECOUPLING CAPACITOR

9.12A(VCC plane from source)





Quanta Computer Inc.			
PROJECT : TE3			
Size: Custom	Document Number: DDRIII DIMMTERMINATOR		Rev: 1A
Date: Tuesday, March 02, 2010	Sheet 15 of 43		

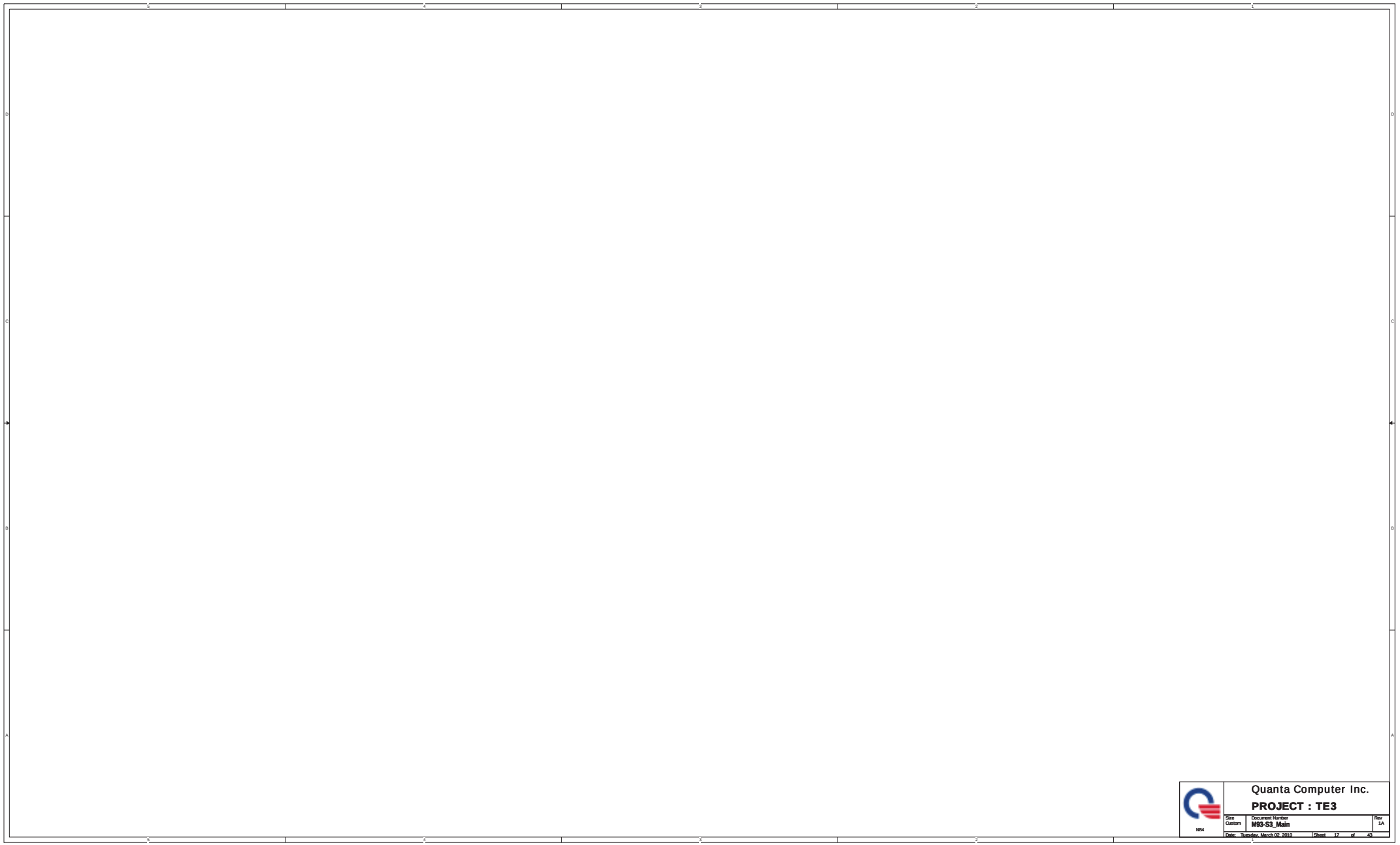
Quanta Computer Inc.

PROJECT : TE3

Size	Document Number	Rev
Custom	M93-S3_PCIE_Interface	1A

Date: Tuesday, March 02, 2010 Sheet 16 of 43

NB4



NB4	Quanta Computer Inc.	
	PROJECT : TE3	
Size: Custom	Document Number: M93-S3_GND / LVDS/ Straps	Rev: 1A
Date: Tuesday, March 02, 2010	Sheet 18 of 43	

Quanta Computer Inc.

PROJECT : TE3

Size	Document Number	Rev
Custom	M93-S3_Power_and_NC	1A

NB4

Date: Tuesday, March 02, 2010 Sheet 19 of 43

NB4	Quanta Computer Inc. PROJECT : TE3	
Size	Document Number M93-S3_HDMI_Thermal	Rev 1A
Date: Tuesday, March 02, 2010	Sheet 20 of 43	

NB4	Quanta Computer Inc.	
	PROJECT : TE3	
Size: Custom	Document Number: M93-S3_Interface	Rev: 1A
Date: Tuesday, March 02, 2010	Sheet 21 of 43	

	Quanta Computer Inc.
NB4	PROJECT : TE3
Size: Custom	Document Number: M93-S3 VRAM_A0,A1
Rev: 1A	
Date: Tuesday, March 02, 2010	Sheet 22 of 43

HDMI Conn [HDM]

D3A

FOR HDMI PAGE 23

Close to HDMI CONN

PLACE AC CAP CLOSE TO CONNECTOR

UMA RS880M
上 715 ohm CS17152FB17

DIS Park
上 499 ohm CS14992FB24

Close to HDMI Connector

C3A

30mils

D3A

C3A

HDMI INTERFACE

C3A

D3A

D3A

HDMI HPD SENSE

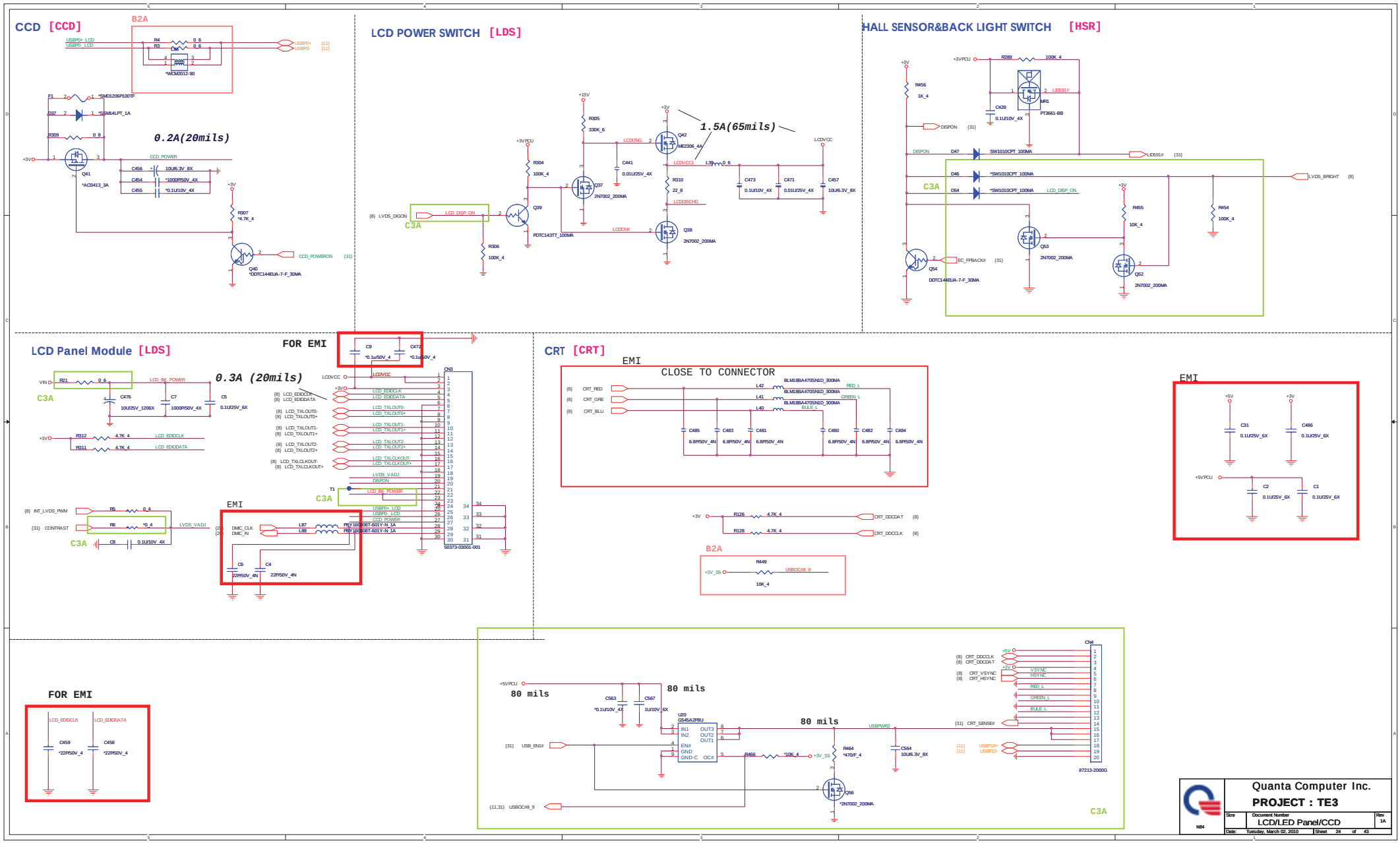
UMA ONLY

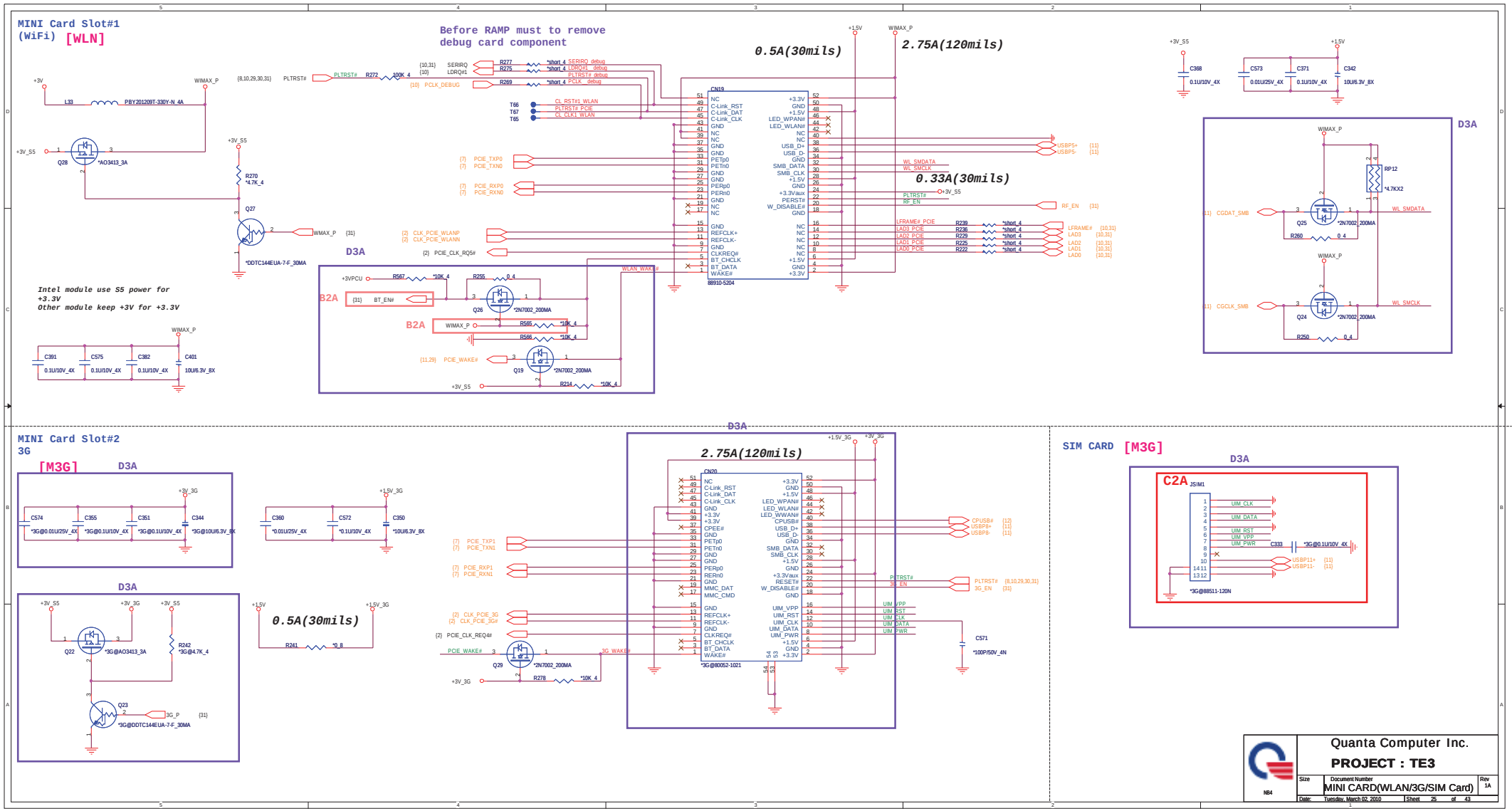
C3A

FOR EMI

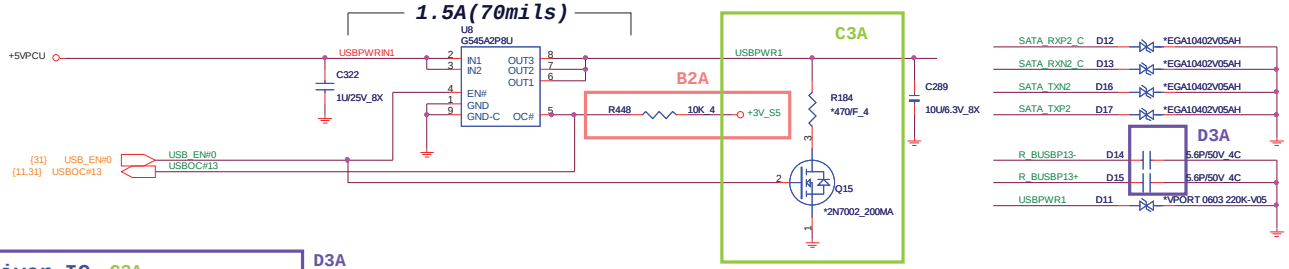
Close to connector

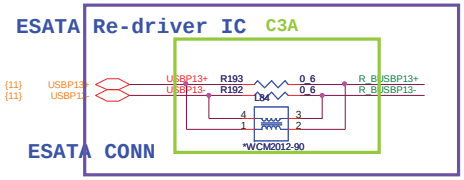
Quanta Computer Inc.
PROJECT : TE3
Size | Document Number: HDMI CONN | Rev 1A
Date: Tuesday, March 02, 2010 | Sheet 23 of 43



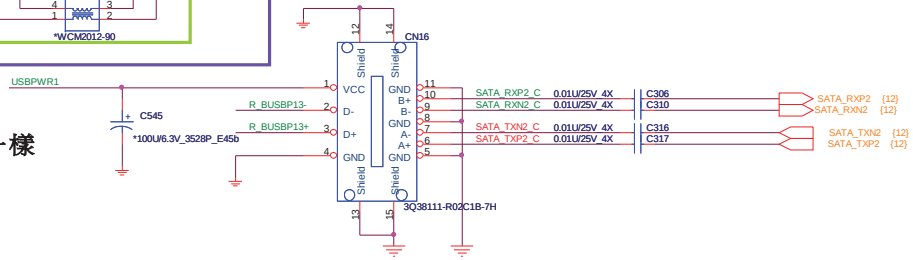


E-SATA [ESA]





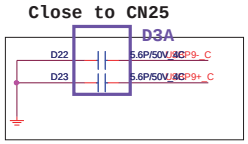
ESATA CONN

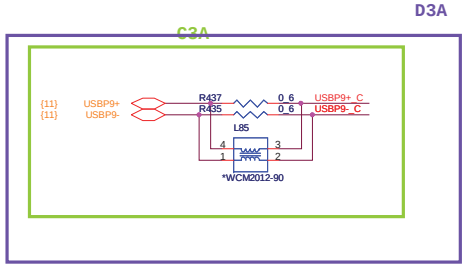


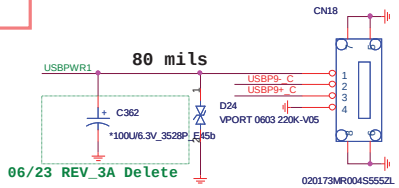
ESATA跟BL6一樣

USB MB SIDE

B2A







Quanta Computer Inc.
PROJECT : TE3

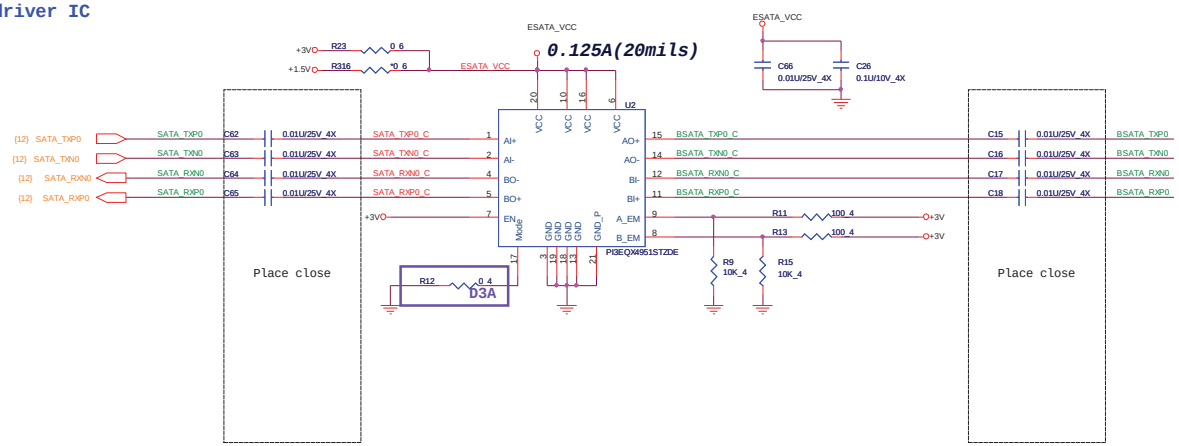
Size	Document Number	Rev
A3	TP/SW/ESATA/USB+Audio/LED	1A
Date: Thursday, March 04, 2010	Sheet 26 of 43	

SATA ODD

[ODD]

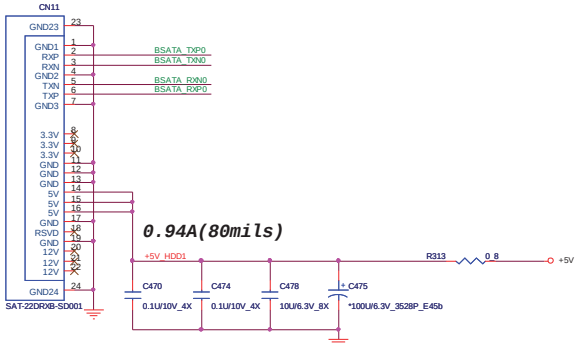
SATA HDD Re-driver IC

B2A

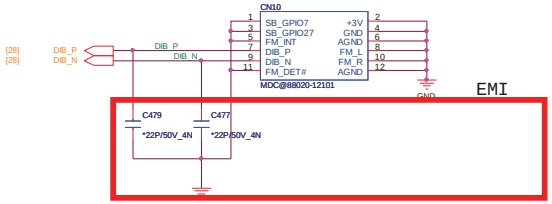


SATA HDD

[HDD]



MDC

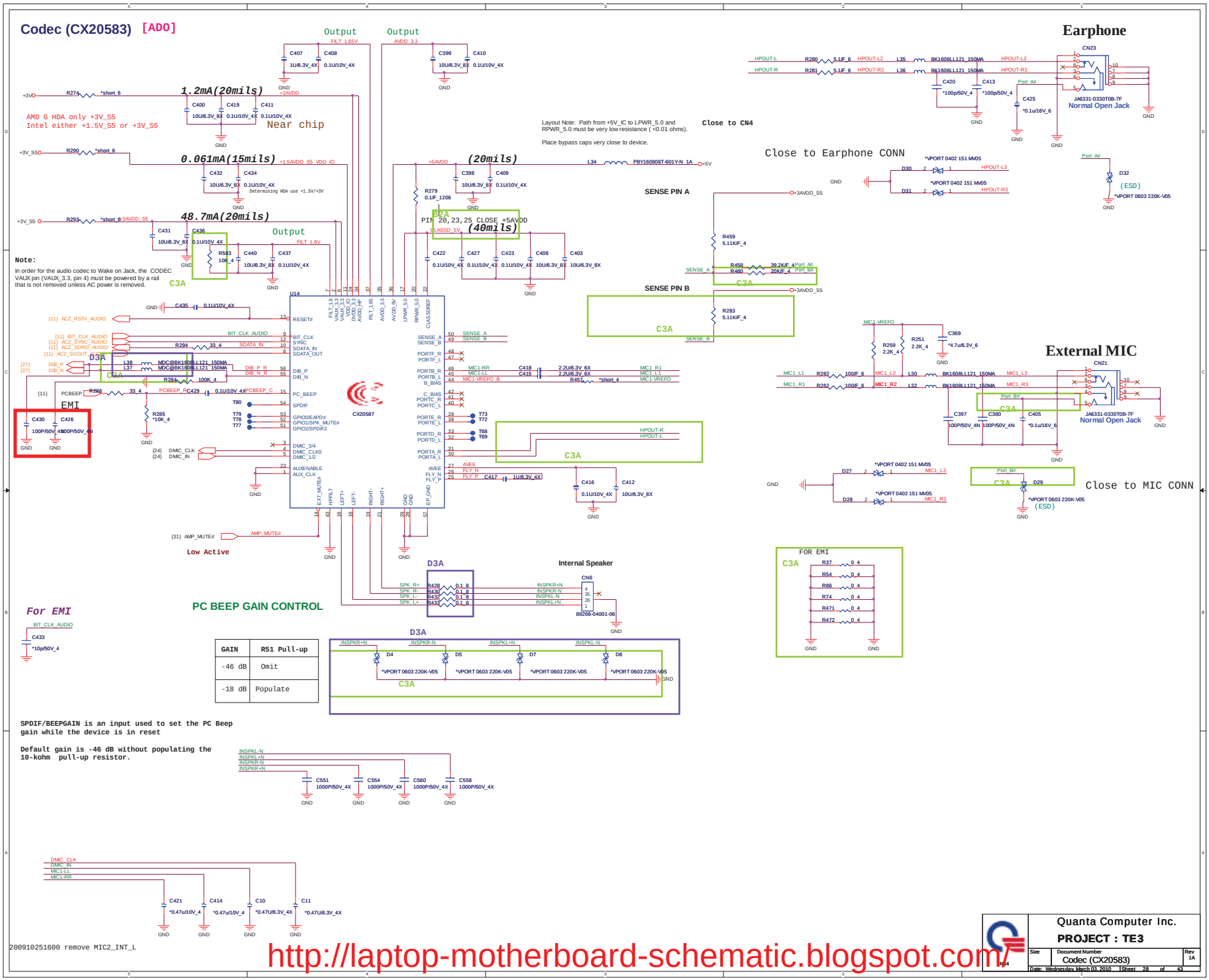


Quanta Computer Inc.

PROJECT : TE3

Size | Document Number: HDD/ODD | Rev: 1A

Date: Tuesday, March 02, 2010 | Sheet 27 of 43

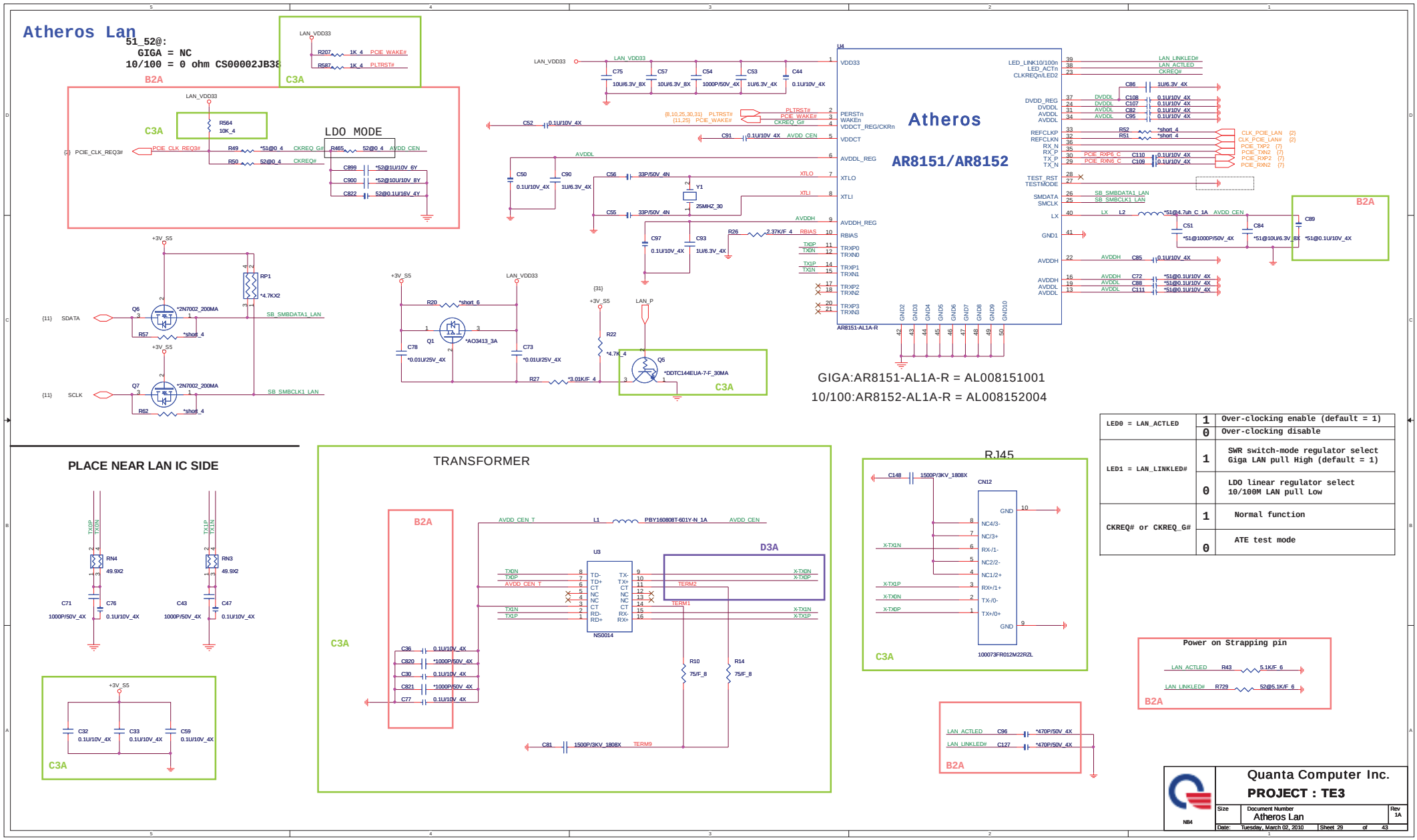


GAIN	R51 Pull-up
-46 dB	Omit
-18 dB	Populate

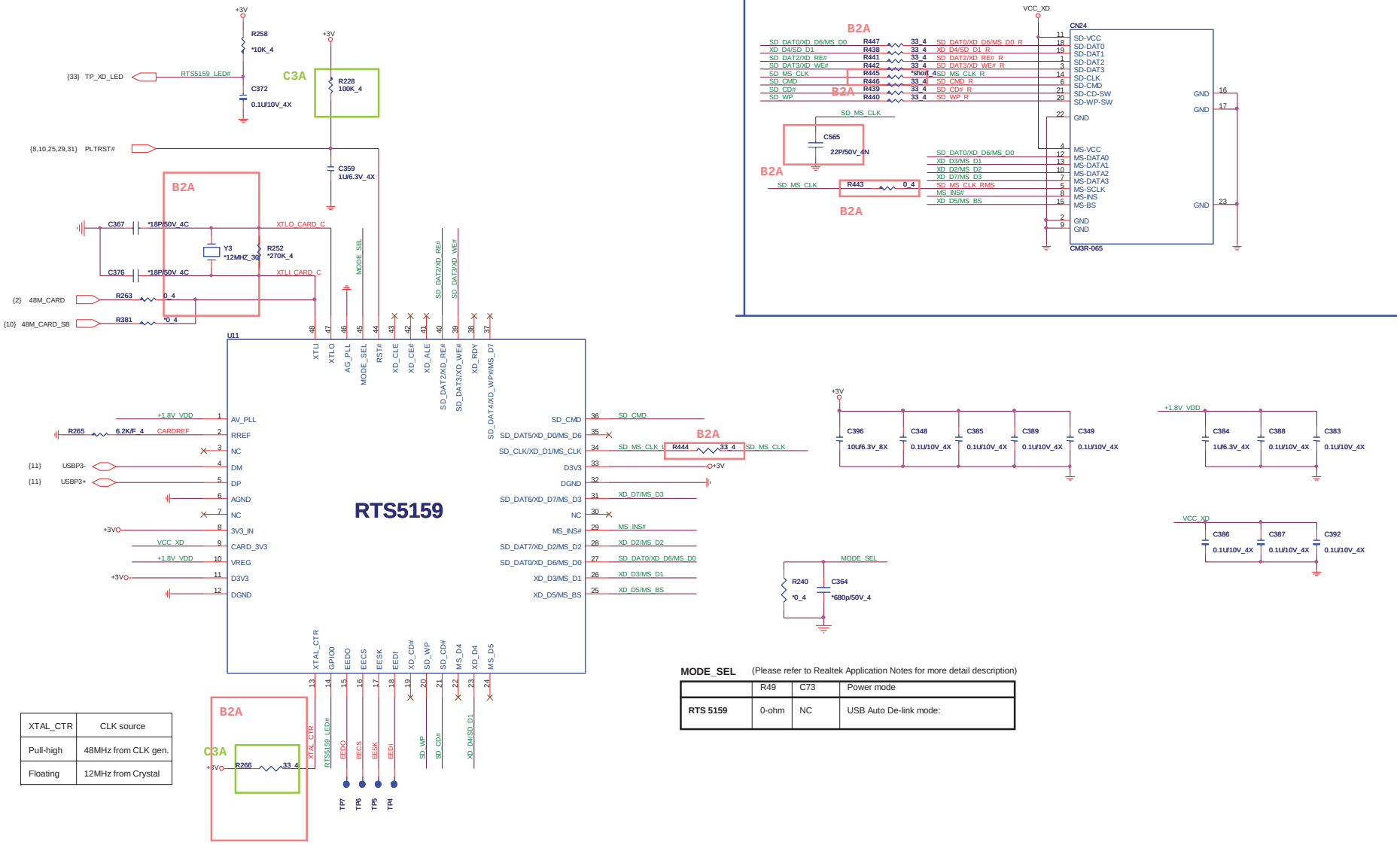
SPDIF/BEEPGAIN is an input used to set the PC Beep gain while the device is in reset

Default gain is -46 dB without populating the 10-kohm pull-up resistor.

200910251600 remove MIC2_INT_L



3 IN 1 CARD READER



XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal

MODE_SEL (Please refer to Realtek Application Notes for more detail description)

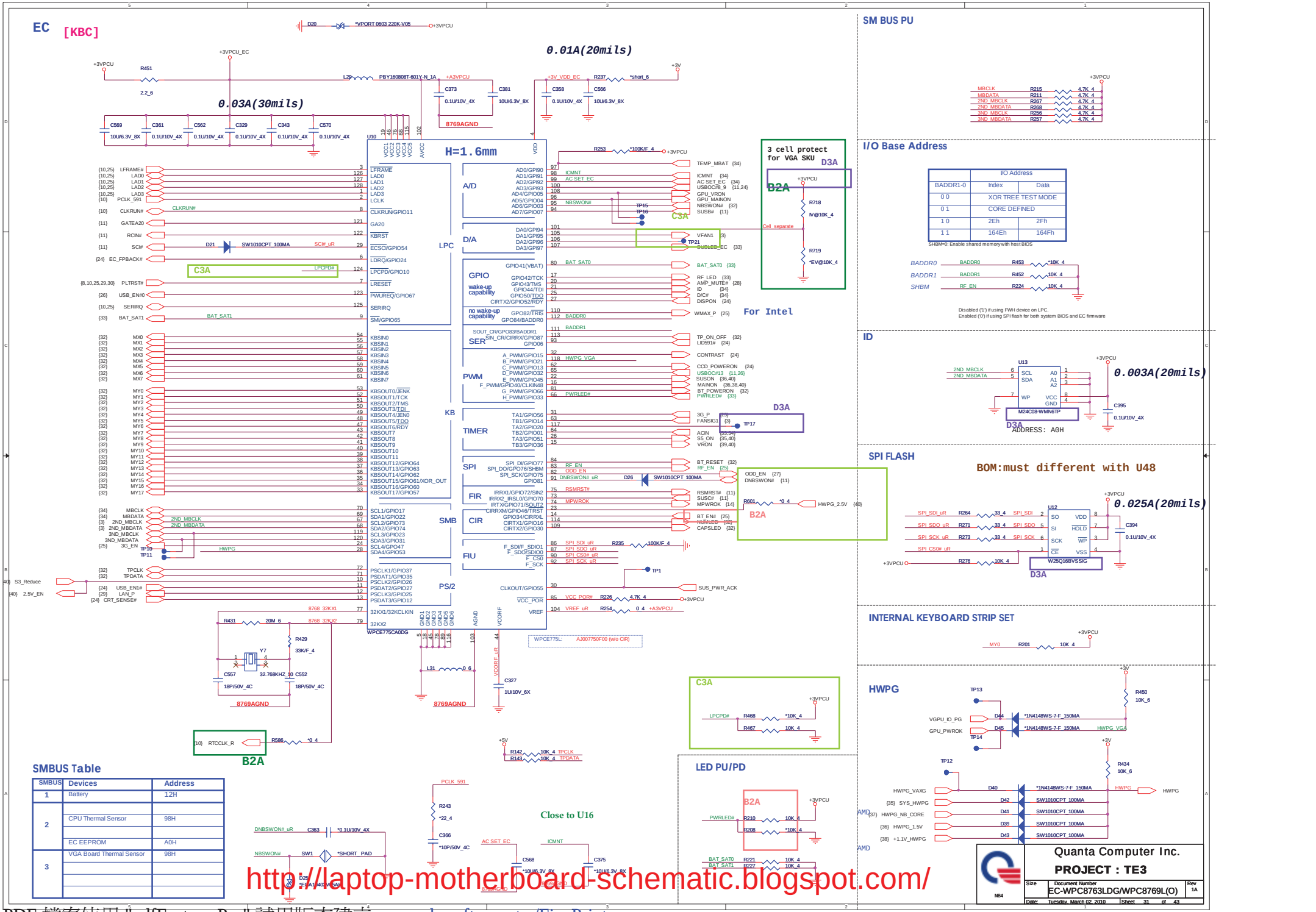
	R49	C73	Power mode
RTS 5159	0-ohm	NC	USB Auto De-link mode:

Quanta Computer Inc.

PROJECT : TE3

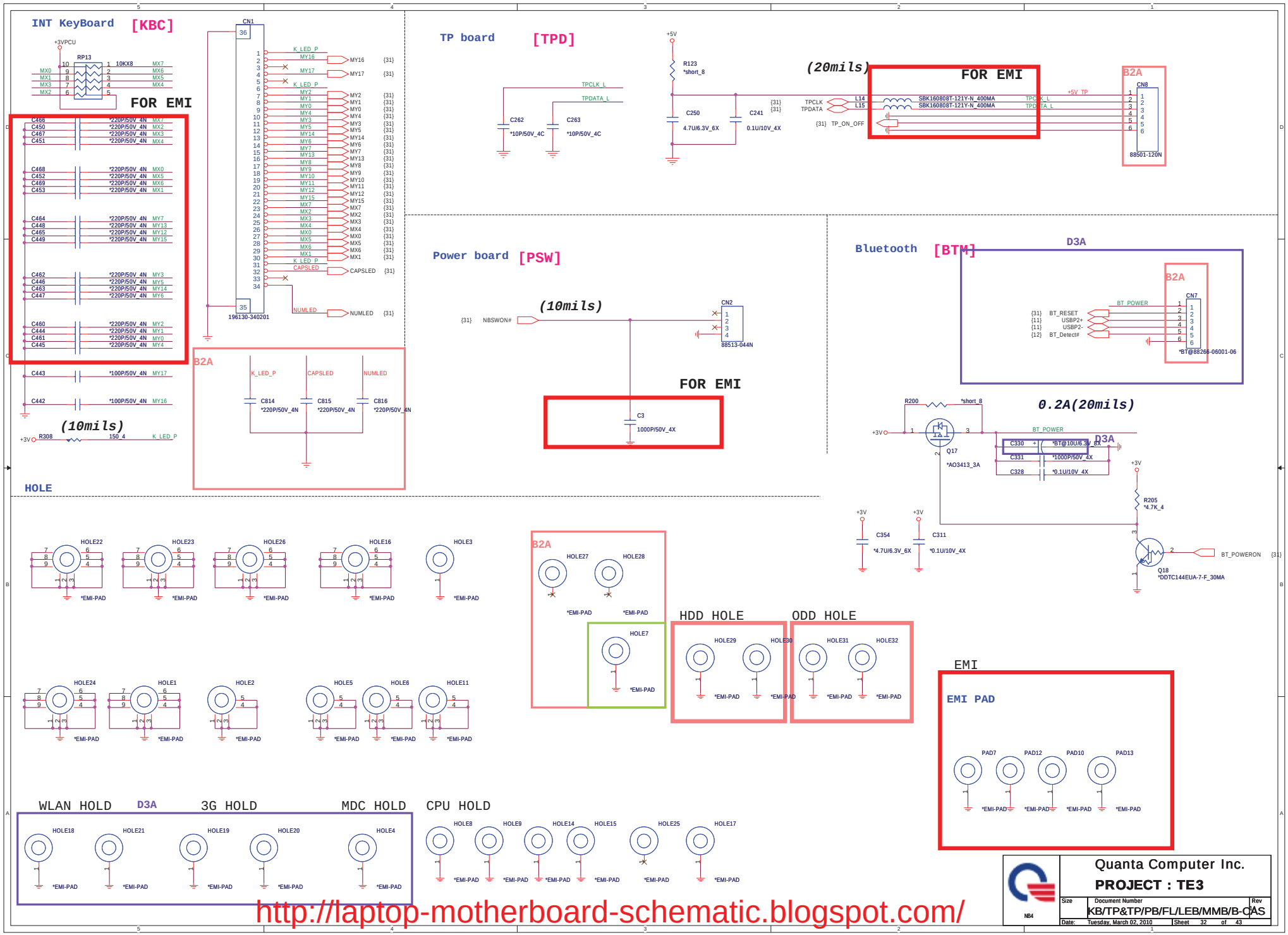
Size	Document Number	Rev
	RTS5159 (Card Reader)	1A
Date: Tuesday, March 02, 2010	Sheet 30 of 43	

NB4



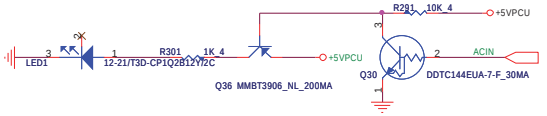
SMBUS Table

SMBUS	Devices	Address
1	Battery	12H
2	CPU Thermal Sensor	98H
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H

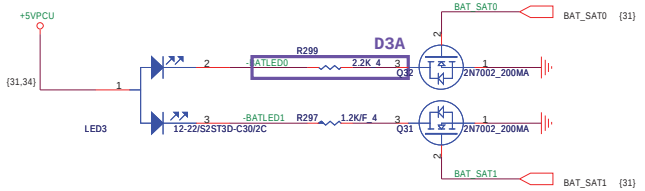


LED [LED]

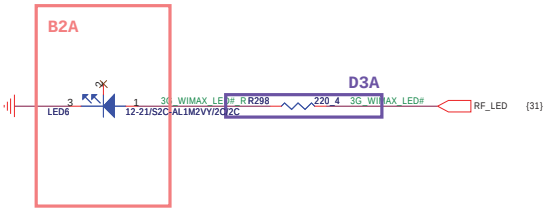
AC-IN



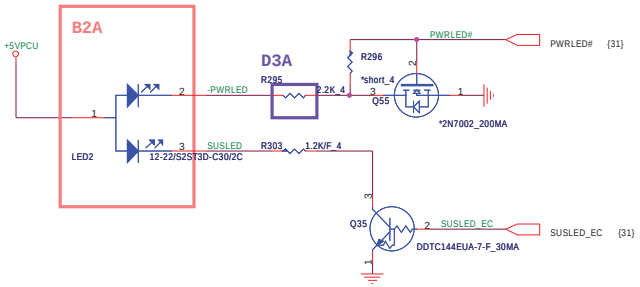
BATERRY



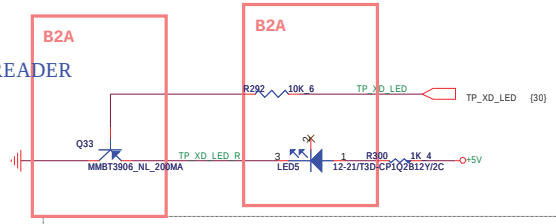
RF LED



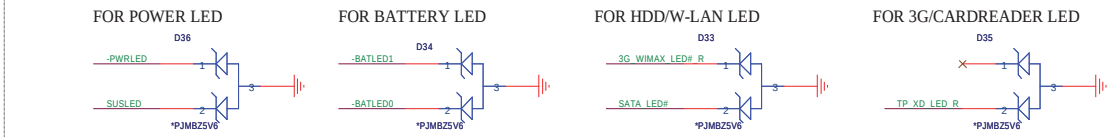
POWER



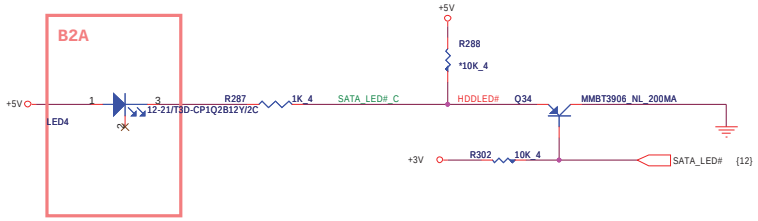
CARDREADER



ESD Protect



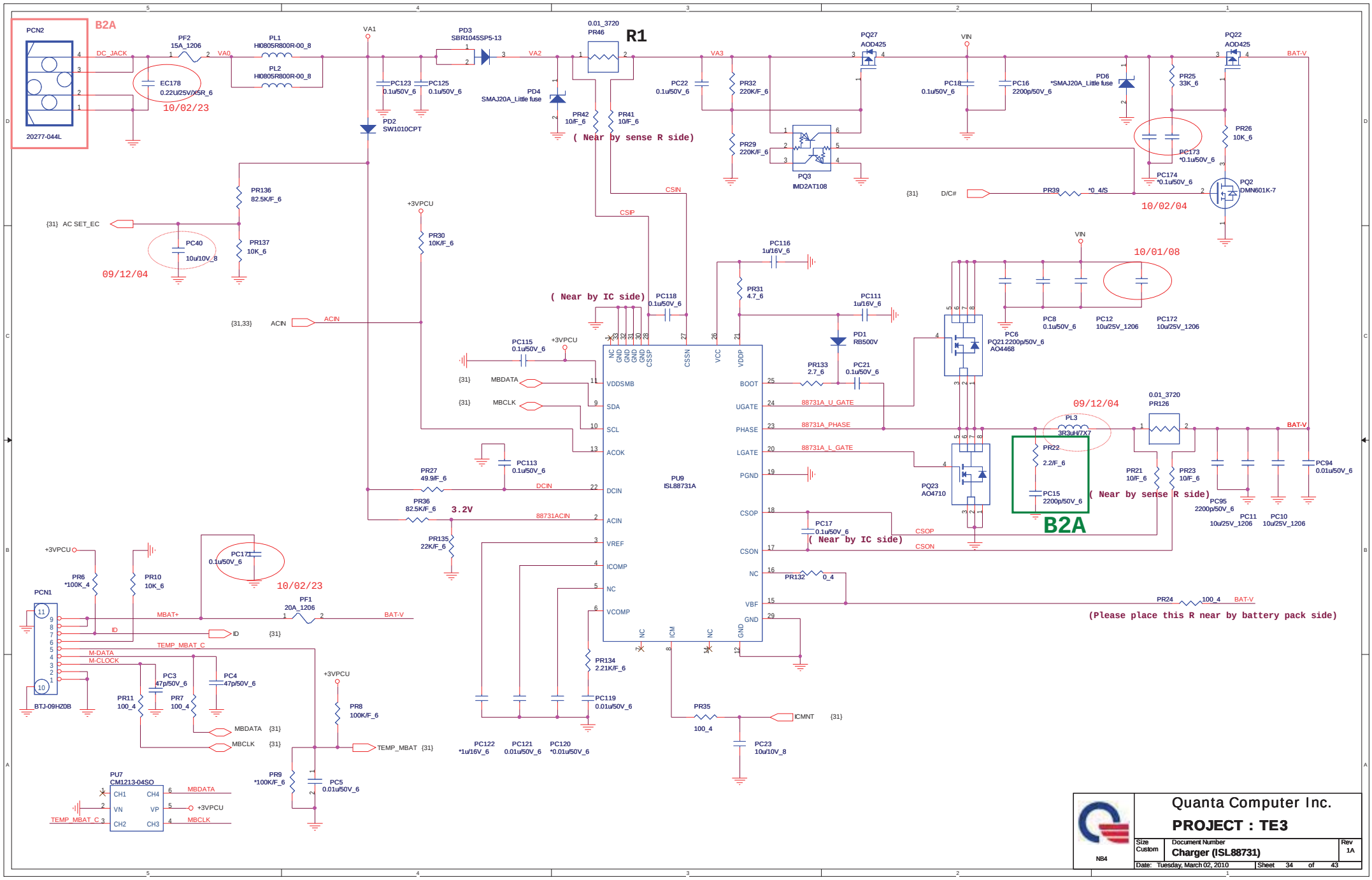
HDD/ODD

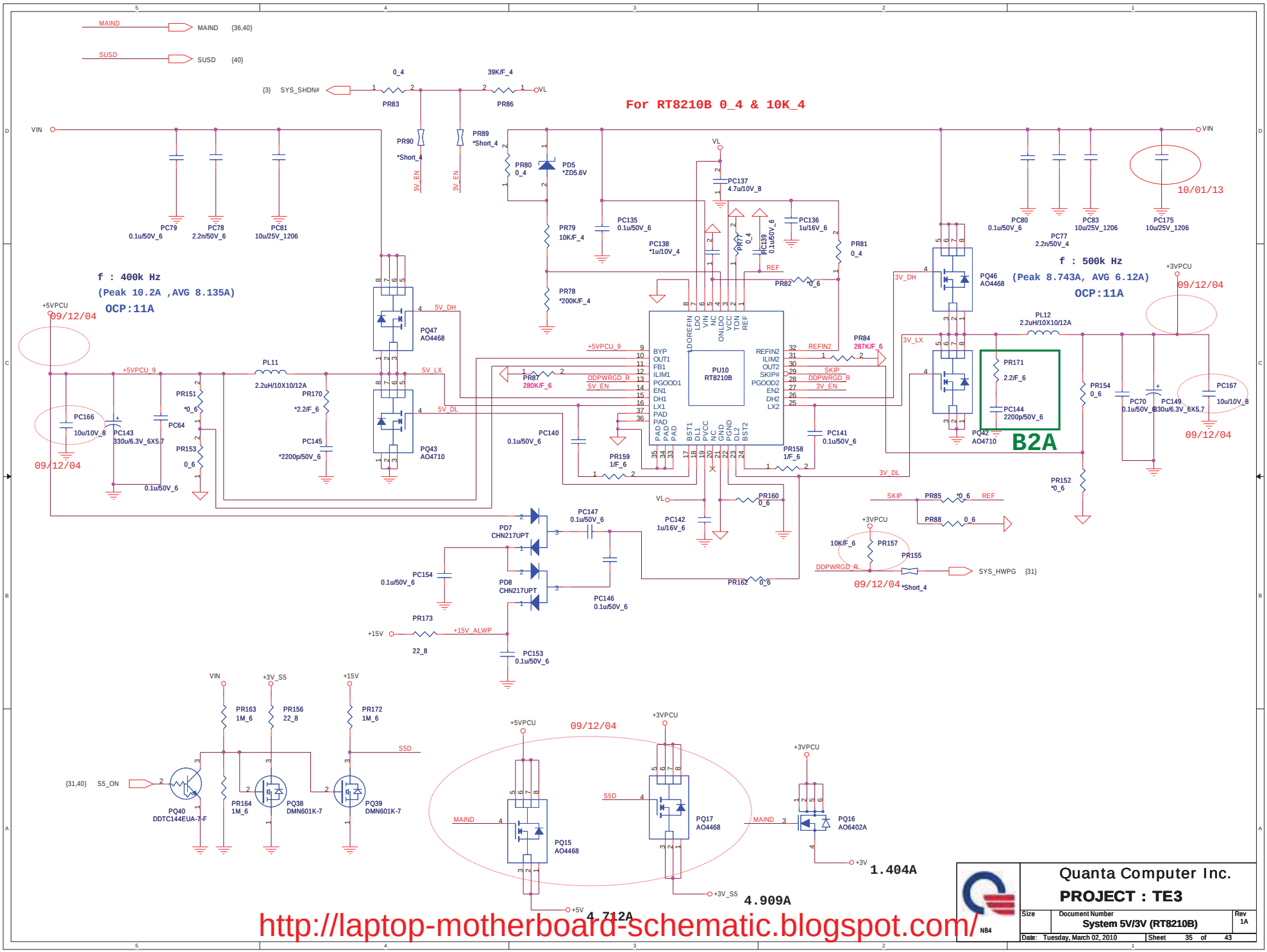


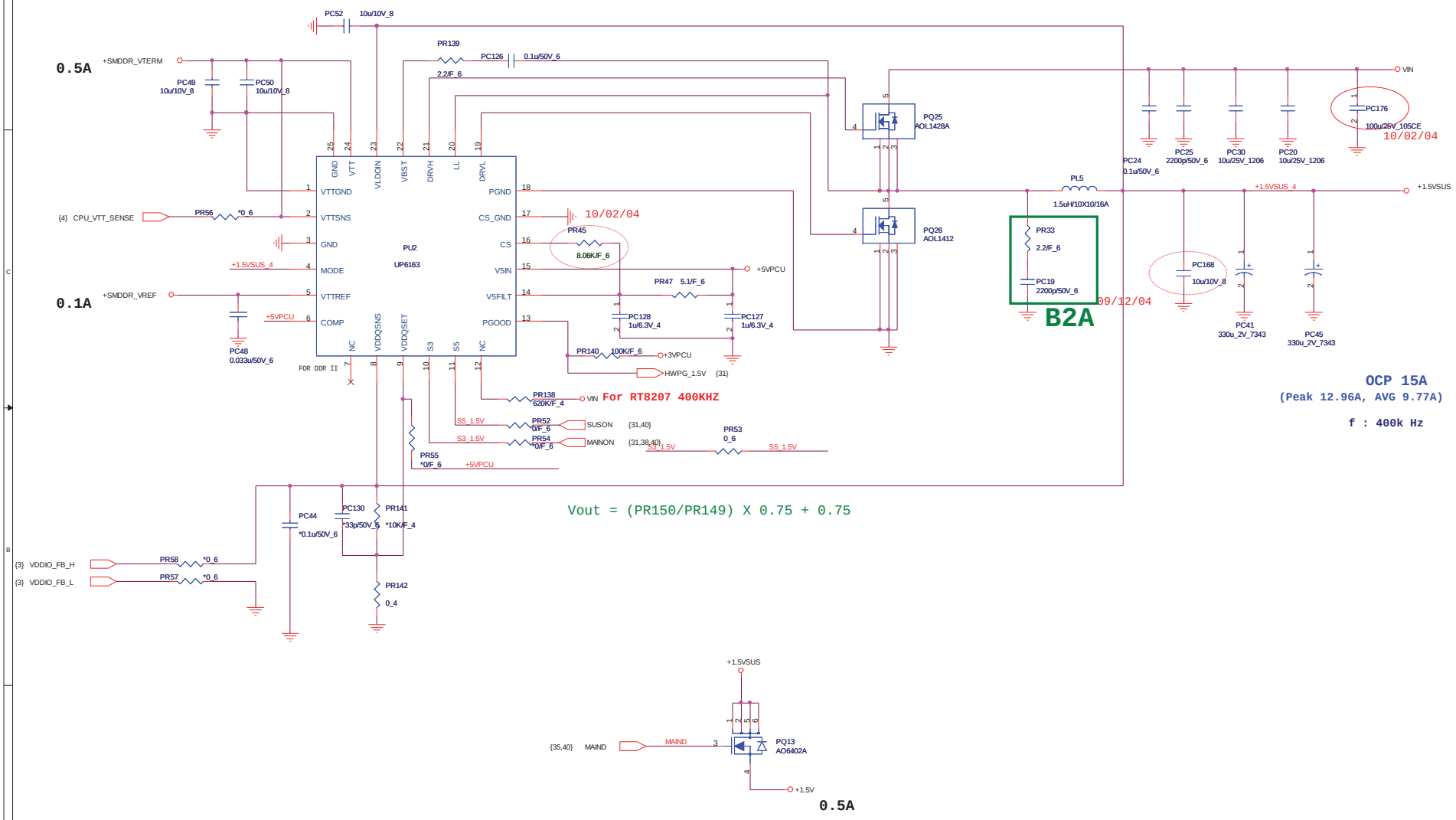
Quanta Computer Inc.
PROJECT : TE3

Size	Document Number	Rev
NB4	LED/HOLE	1A

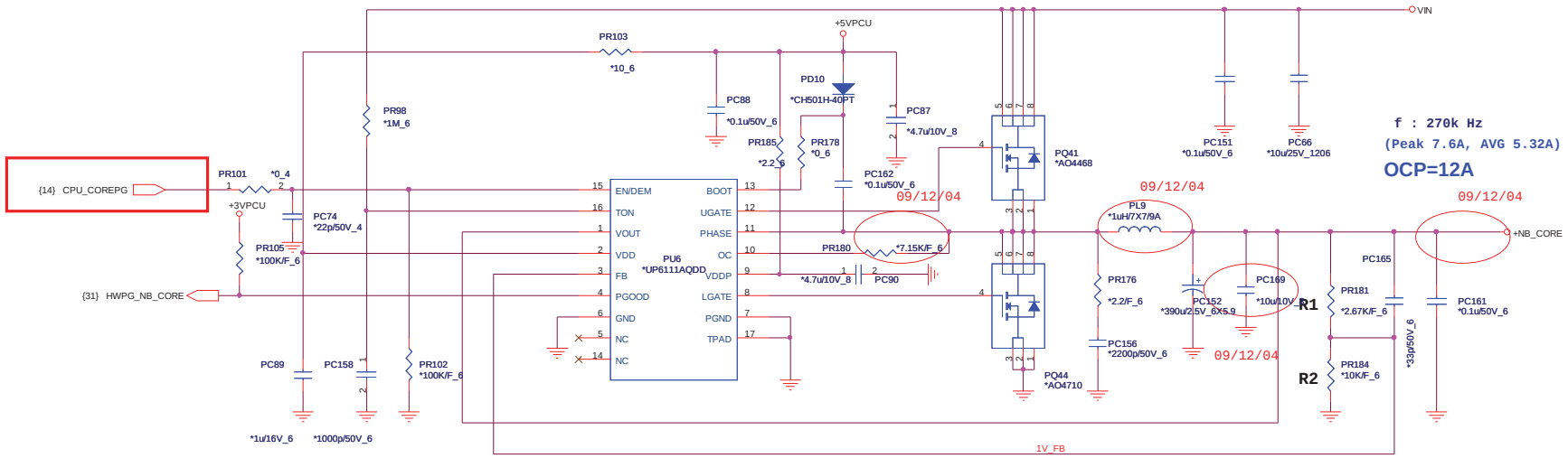
Date: Wednesday, March 03, 2010 Sheet 33 of 43

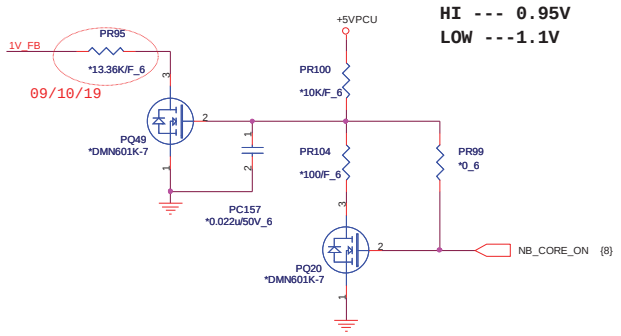






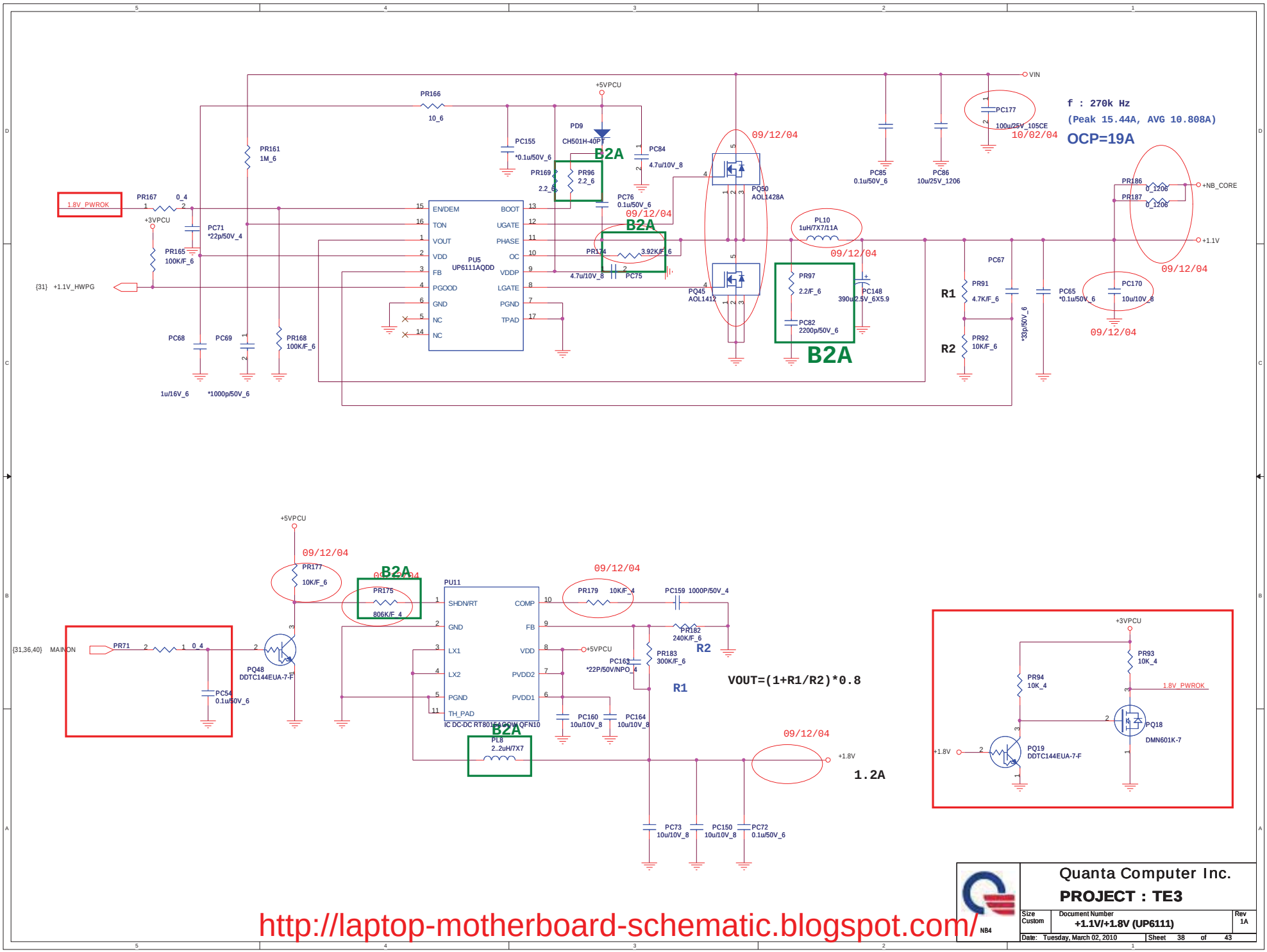
Quanta Computer Inc.
PROJECT : TE3
Size | Document Number: DDR 1.5V (UP6163) | Rev: 1A
Date: Tuesday, March 02, 2010 | Sheet 36 of 43

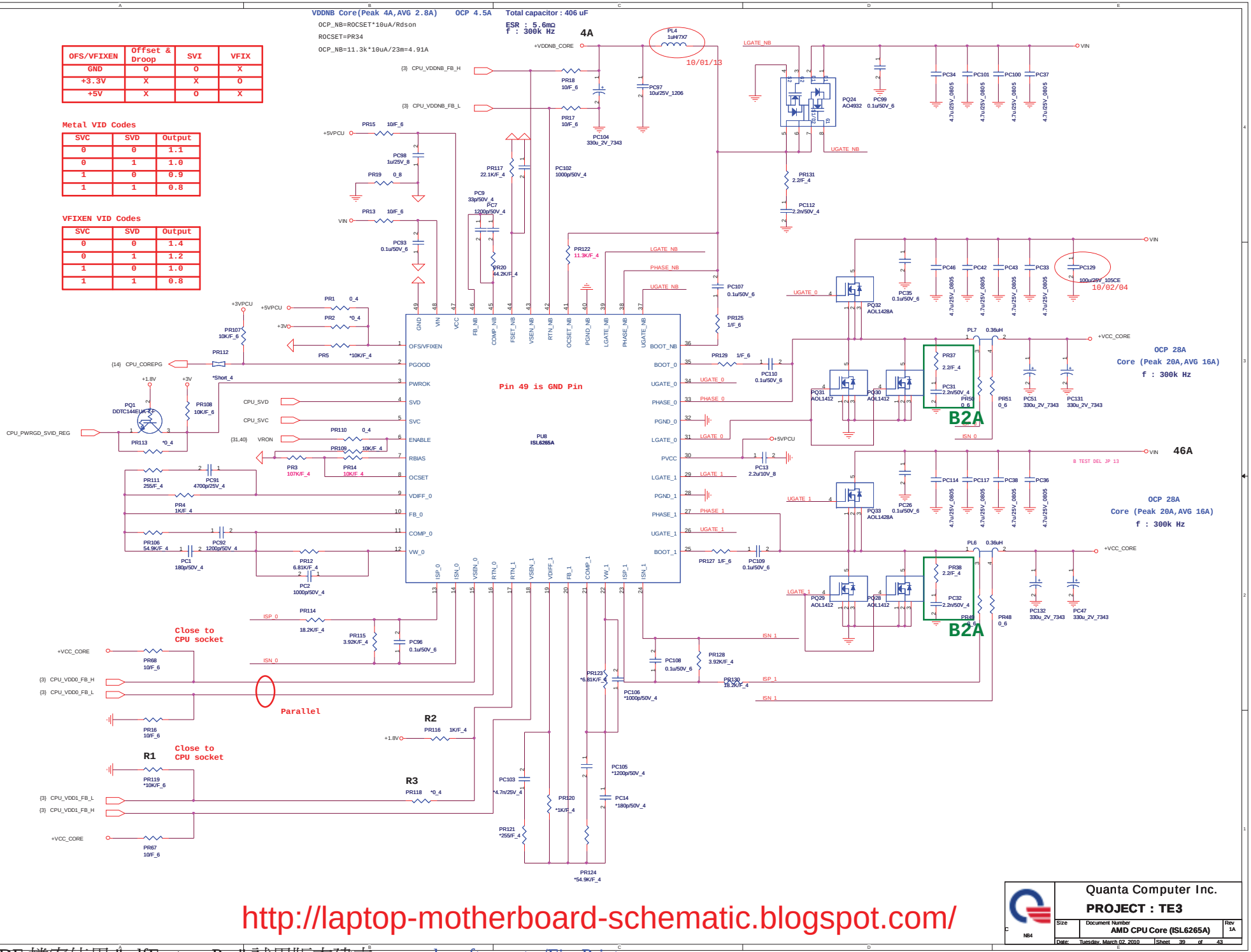




Quanta Computer Inc.
PROJECT : TE3

Size	Document Number	Rev
	NB_CORE (UP6111)	1A
Date: Tuesday, March 02, 2010	Sheet 37 of 43	



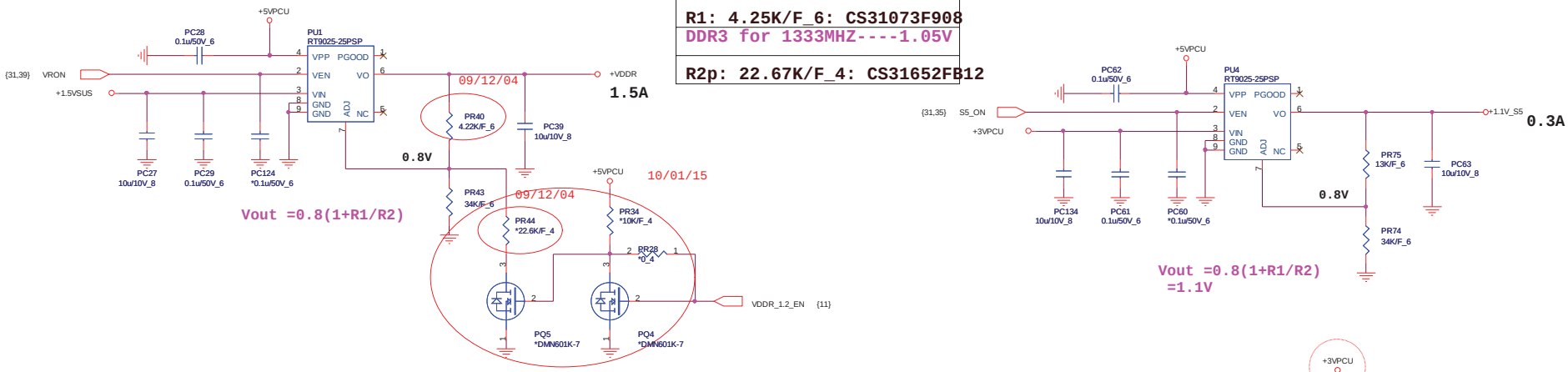


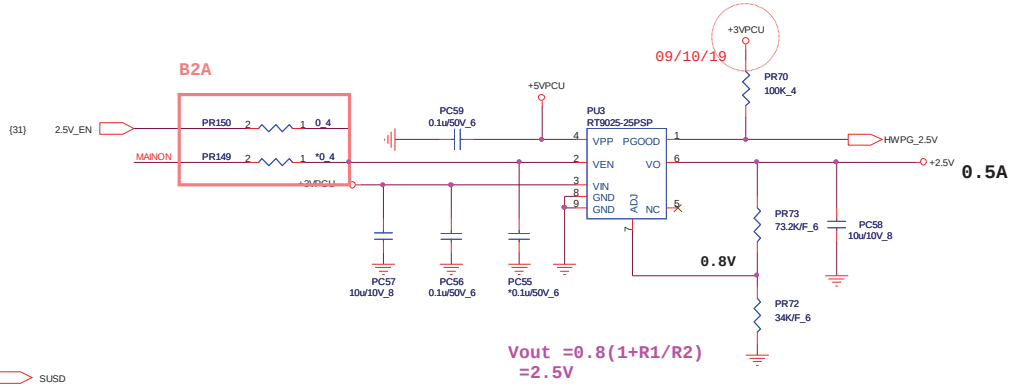
DDR3 for 1066MHZ----0.9V

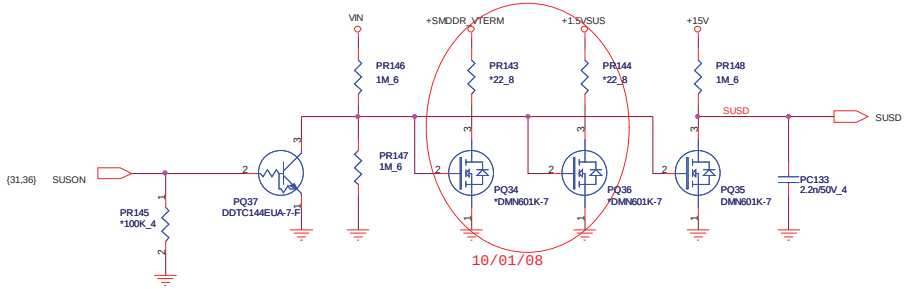
R1: 4.25K/F_6: CS31073F908

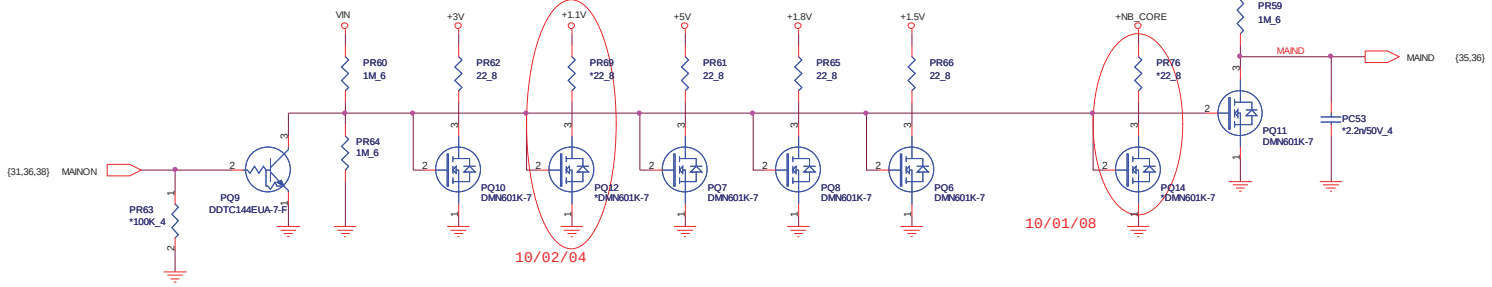
DDR3 for 1333MHZ----1.05V

R2p: 22.67K/F_4: CS31652FB12









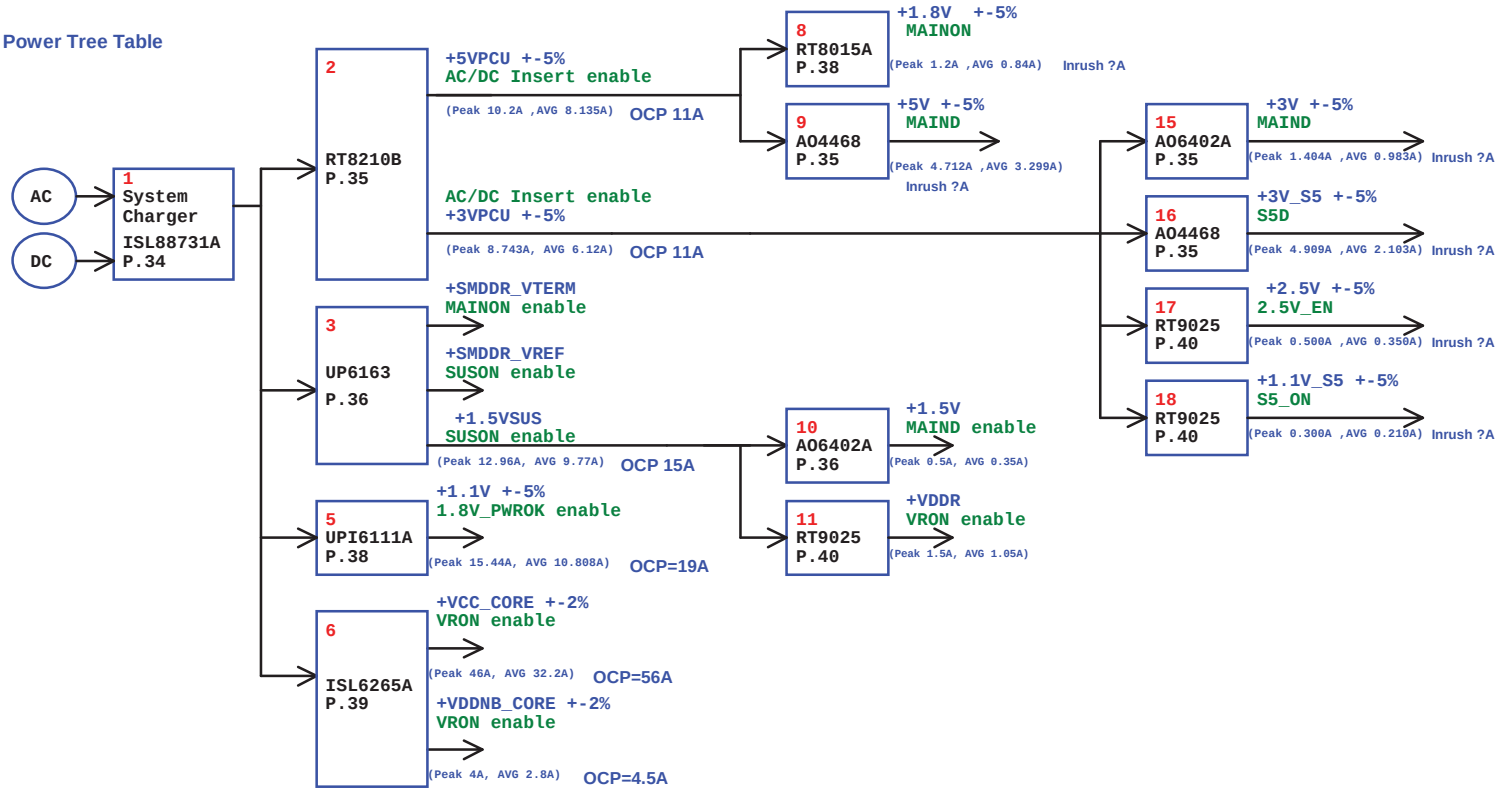
Quanta Computer Inc.

PROJECT : TE3

Size	Document Number	Rev
NB4	Discharge/2.5/1.1/VDDR	1A
Date: Tuesday, March 02, 2010	Sheet 40 of 43	

Quanta Computer Inc.
PROJECT : TE3
SIDE PORT FOR UMA

Power Tree Table



Power Distribution List

Power	Distribution

Quanta Computer Inc.
PROJECT : TE3
Size: Custom NB4 | Document Number: Power Tree Table | Rev: 1A
Date: Tuesday, March 02, 2010 | Sheet 42 of 43

Model	REV	CHANGE LIST
TE3 MB		
	1A	PAGE 2: (CLOCK GEN)--add C209,C218,C212,C3707 FOR PU 3V
		PAGE 12: (SB820M)-- ADD BOARD_ID7,BOARD_ID8
		PAGE 24: (ALL)--CO-LAY L86 Footprint FOR EMI
		PAGE 26: (ALL)--del F2,C564,C567,U20,R448,R449,Q51,C563, USB Swith power change from USBPWR2 to USBPWR1
		PAGE 26: (ALL)--CO-LAY L85,L84 Footprint FOR EMI
		PAGE 29: (ALL)--ADD R465,R729,R636,R637 FOR LAN 52
		PAGE 32: (ALL)--Change CN8 footprint to 88513-0601-6p-l-smt , CN7 footprint to 87213-0600-6P-L
		PAGE 33: (ALL)--change LED seat
		PAGE 39:(ALL)-- change PR174 to 3.92Kohm for OCP setting
		PAGE 39:(ALL)-- change PQ45 footprint for higher current requirement
		PAGE 39:(ALL)-- change PQ50 footprint for higher current requirement
		PAGE 39:(ALL)-- add PC170 for EMI
	2A	PAGE 3: (ALL)--add R33 FOR PU 3V,DEL R32
		PAGE 11: (ALL)--DEL U7
		PAGE 23: (ALL)--ADD Q57,Q58,R474,R475 FOR HDMI
		PAGE 28: (ALL)--CHANGE AUDIO IC FROM CX20583 TO CX20587

MODEL: TE3

PAGE	FROM	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	

DOC NO. 204					
PROJECT MODEL :	TE2A	APPROVED BY:	MAX WENG	DATE:	2009/11/13
PART NUMBER:		DRAWING BY:	MAX WENG	REVISON:	1A

Quanta Computer Inc.
PROJECT : TE3
Size | Document Number: Change list | Rev: 1A
Date: Tuesday, March 02, 2010 | Sheet 43 of 43