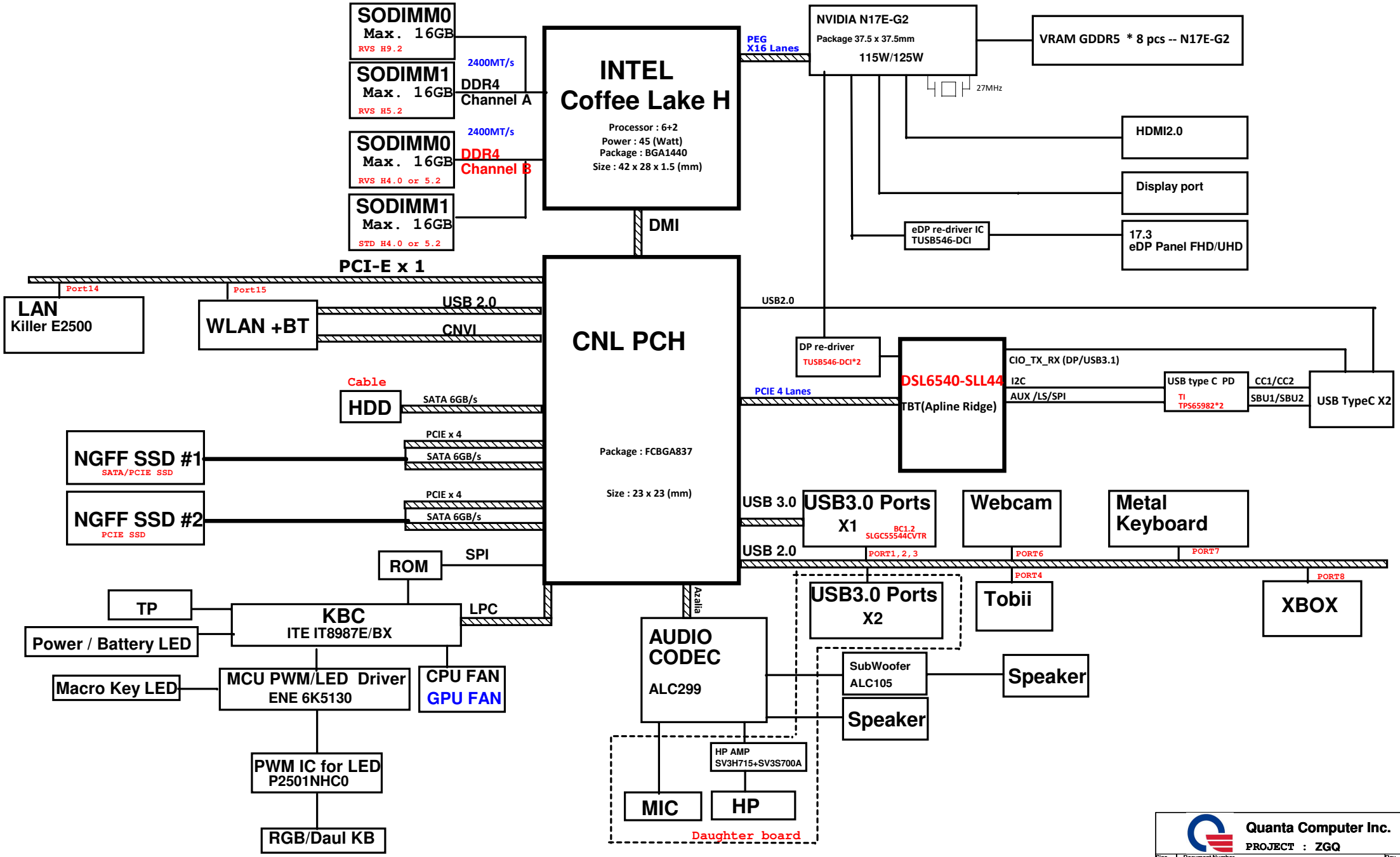
ZGQ CFL-H/K +1070 MAX-P SYSTEM DIAGRAM

01



Quanta Computer Inc.

PROJECT : ZGQ

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

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CFL-H Processor (CLK,MISC,JTAG)

02

For debug only remove from MV

Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impendence 85 ohm

EMI RESERVE

PROCPWRGD (50ohm)
Trace Length: 1~11.25 inches

PM_SYNC (50ohm)
Trace Length: 1~11.25 inches

CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

Design Note(CFG_RCOMP):
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

Processor pull-up (CPU)

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

Contiguration Signals: The CFG signals have a default value of '1' if not terminated
on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.
Intel recommends placing test points on the
board for CFG pins.
. CFG[0]:Stall reset sequence after PCU PLL lock until de-asserted:
-1=(Default) Normal Operation;
No stall.
-0=Stall.
.CFG[1]:Reserved configuration lane.
.CFG[2]:PCI Express*Static x16 Lane Numbering Reversal.
-1=Normal operation
-0=Lane numbers reversed.
.CFG[3]:Reserved configuration lane.
.CFG[4]:eDP enable:
-1=Disabled.
-0=Enabled.
.CFG[6:5]:PCI Express* Bifurcation
-00=1x8,2x4 PCI Express*
-01=reserved
-10=2x8 PCI Express*
-11=1x16 PCI Express*
.CFG[7]:PEG Training:
-1=(default) PEG Train immediately following RESET# de assertion.
-0=PEG Wait for BIOS for assertion.
.CFG[19:8]:Reserved configuration lanes.

CPU CORE SVID

Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.

PLACE THE PU RESISTORS CLOSE TO VR
PULL UP IS IN THE VR MODULE
Close to CPU
SVID CLK

CLOSE TO CPU
PLACE THE PU RESISTORS
Close to CPU
SVID ALERT

CLOSE TO CPU
PLACE THE PU RESISTORS
Close to CPU
SVID DATA

THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches

Ra Not install in SKL-H

Note: please keep plane is enough for VDDQ 2.8A
Placement close to CPU.

PROCHOT# (50ohm)
Trace Length <11 inches
Cb need placment near VR

Modify 8/10

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	CFL 1/7 (JTAG/MISC)		1A
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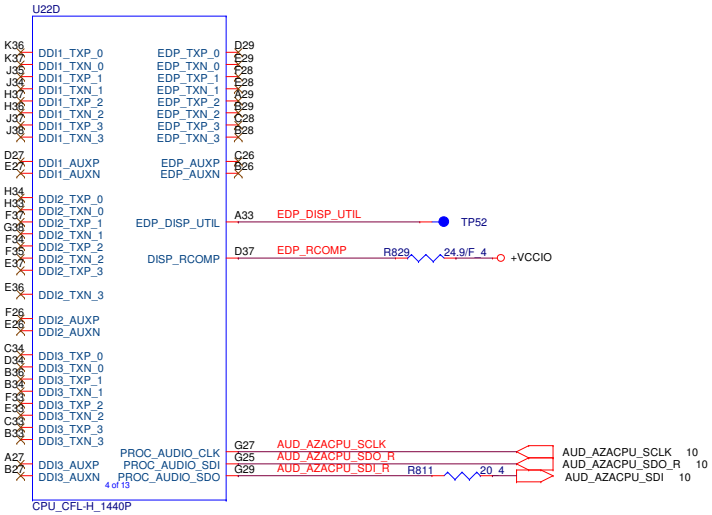
CFL Processor (DMI,PEG,FDI)

03



DP & PEG Compensation

eDP_RCOMP
Trace length < 100 Mils
Trace Width 5 Mils Trace Spacing 25 Mils

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_RCOMP
Trace length < 400 MILS
Trace width = 12 MILS
Trace spacing = 15 MILS

+1.2VSUS 2,6,10,14,17,18,19,20,60,71

+3V 2,9,10,11,13,17,18,19,20,26,35,36,37,38,39,40,44,45,46,47,48,49,50,51,52,56,58,59,60,61,64,69,70,71

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Size	Document Number	Rev
	CFL 2/7 (DMI/EDP/PEG)	1A
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CFL Processor (DDR4)

17,19 M_A_DQ[15:0]
17,19 M_A_DQ[31:16]
17,19 M_A_DQ[47:32]
17,19 M_A_DQ[63:48]

Interleave / Non-Interleave

U22A

M_A_DQ0	BR6	DDR0_DQ_0/DDR0_DQ_0	DDR0_CKP_0/DDR0_CKP_0	AG1	M_A_DIM0_CLKP0 17
M_A_DQ1	BT6	DDR0_DQ_1/DDR0_DQ_1	DDR0_CKN_0/DDR0_CKN_0	AG2	M_A_DIM0_CLKN0 17
M_A_DQ2	BP5	DDR0_DQ_2/DDR0_DQ_2	DDR0_CKP_1/DDR0_CKP_1	AK2	M_A_DIM0_CLKP1 17
M_A_DQ3	BR3	DDR0_DQ_3/DDR0_DQ_3	DDR0_CKN_1/DDR0_CKN_1	AK1	M_A_DIM0_CLKN1 17
M_A_DQ4	BN5	DDR0_DQ_4/DDR0_DQ_4	NC/DDR0_CKP_2	AL3	M_A_DIM1_CLKP0 19
M_A_DQ5	BP6	DDR0_DQ_5/DDR0_DQ_5	NC/DDR0_CKN_2	AK3	M_A_DIM1_CLKN0 19
M_A_DQ6	BP2	DDR0_DQ_6/DDR0_DQ_6	NC/DDR0_CKP_3	AL2	M_A_DIM1_CLKP1 19
M_A_DQ7	BN3	DDR0_DQ_7/DDR0_DQ_7	NC/DDR0_CKN_3	AL1	M_A_DIM1_CLKN1 19
M_A_DQ8	BL4	DDR0_DQ_8/DDR0_DQ_8		AT1	
M_A_DQ9	BL5	DDR0_DQ_9/DDR0_DQ_9	DDR0_CKE_0/DDR0_CKE_0	AT2	M_A_CKE0 17
M_A_DQ10	BL2	DDR0_DQ_10/DDR0_DQ_10	DDR0_CKE_1/DDR0_CKE_1	AT3	M_A_CKE1 17
M_A_DQ11	BM1	DDR0_DQ_11/DDR0_DQ_11	DDR0_CKE_2/DDR0_CKE_2	AT5	M_A_CKE2 19
M_A_DQ12	BK4	DDR0_DQ_12/DDR0_DQ_12	DDR0_CKE_3/DDR0_CKE_3	-	M_A_CKE3 19
M_A_DQ13	BK5	DDR0_DQ_13/DDR0_DQ_13		AD5	
M_A_DQ14	BK1	DDR0_DQ_14/DDR0_DQ_14	DDR0_CS#_0/DDR0_CS#_0	AE2	M_A_CS#0 17
M_A_DQ15	BK2	DDR0_DQ_15/DDR0_DQ_15	DDR0_CS#_1/DDR0_CS#_1	AD2	M_A_CS#1 17
M_A_DQ16	BG4	DDR0_DQ_16/DDR0_DQ_32	NC/DDR0_CS#_2	AE5	M_A_CS#2 19
M_A_DQ17	BG5	DDR0_DQ_17/DDR0_DQ_33	NC/DDR0_CS#_3	-	M_A_CS#3 19
M_A_DQ18	BF4	DDR0_DQ_18/DDR0_DQ_34		AD3	
M_A_DQ19	BF5	DDR0_DQ_19/DDR0_DQ_35	DDR0_ODT_0/DDR0_ODT_0	AE4	M_A_ODT0 17
M_A_DQ20	BG2	DDR0_DQ_20/DDR0_DQ_36	NC/DDR0_ODT_1	AE1	M_A_ODT1 17
M_A_DQ21	BG1	DDR0_DQ_21/DDR0_DQ_37	NC/DDR0_ODT_2	AD4	M_A_ODT2 19
M_A_DQ22	BF1	DDR0_DQ_22/DDR0_DQ_38	NC/DDR0_ODT_3	-	M_A_ODT3 19
M_A_DQ23	BF2	DDR0_DQ_23/DDR0_DQ_39		AH5	
M_A_DQ24	BD2	DDR0_DQ_24/DDR0_DQ_40	DDR0_CAB_4/DDR0_BA_0	AH1	M_A_BS#0 17,19
M_A_DQ25	BD1	DDR0_DQ_25/DDR0_DQ_41	DDR0_CAB_6/DDR0_BA_1	AU1	M_A_BS#1 17,19
M_A_DQ26	BC4	DDR0_DQ_26/DDR0_DQ_42	DDR0_CAA_5/DDR0_BG_0	-	M_A_BG#0 17,19
M_A_DQ27	BC5	DDR0_DQ_27/DDR0_DQ_43		AH4 M_A_A16	M_A_A[16:0] 17,19
M_A_DQ28	BD5	DDR0_DQ_28/DDR0_DQ_44	DDR0_CAB_3/DDR0_MA_16	AG4 M_A_A14	
M_A_DQ29	BD4	DDR0_DQ_29/DDR0_DQ_45	DDR0_CAB_2/DDR0_MA_14	AD1 M_A_A15	
M_A_DQ30	BC1	DDR0_DQ_30/DDR0_DQ_46	DDR0_CAB_1/DDR0_MA_15		
M_A_DQ31	BC2	DDR0_DQ_31/DDR0_DQ_47		AH3 M_A_A0	
M_A_DQ32	AB1	DDR0_DQ_32/DDR1_DQ_0	DDR0_CAB_9/DDR0_MA_0	AP4 M_A_A1	
M_A_DQ33	AB2	DDR0_DQ_33/DDR1_DQ_1	DDR0_CAB_8/DDR0_MA_1	AN4 M_A_A2	
M_A_DQ34	AA4	DDR0_DQ_34/DDR1_DQ_2	DDR0_CAB_5/DDR0_MA_2	AP5 M_A_A3	
M_A_DQ35	AA5	DDR0_DQ_35/DDR1_DQ_3	NC/DDR0_MA_3	AP2 M_A_A4	
M_A_DQ36	AB4	DDR0_DQ_36/DDR1_DQ_4	NC/DDR0_MA_4	AR1 M_A_A5	
M_A_DQ37	AB5	DDR0_DQ_37/DDR1_DQ_5	DDR0_CAA_0/DDR0_MA_5	AP3 M_A_A6	
M_A_DQ38	AA2	DDR0_DQ_38/DDR1_DQ_6	DDR0_CAA_2/DDR0_MA_6	AN1 M_A_A7	
M_A_DQ39	AA1	DDR0_DQ_39/DDR1_DQ_7	DDR0_CAA_4/DDR0_MA_7	AN3 M_A_A8	
M_A_DQ40	V5	DDR0_DQ_40/DDR1_DQ_8	DDR0_CAA_3/DDR0_MA_8	AT4 M_A_A9	
M_A_DQ41	V2	DDR0_DQ_41/DDR1_DQ_9	DDR0_CAA_1/DDR0_MA_9	AH2 M_A_A10	
M_A_DQ42	U1	DDR0_DQ_42/DDR1_DQ_10	DDR0_CAB_7/DDR0_MA_10	AN2 M_A_A11	
M_A_DQ43	U2	DDR0_DQ_43/DDR1_DQ_11	DDR0_CAA_7/DDR0_MA_11	AU4 M_A_A12	
M_A_DQ44	V1	DDR0_DQ_44/DDR1_DQ_12	DDR0_CAA_6/DDR0_MA_12	AE3 M_A_A13	
M_A_DQ45	V4	DDR0_DQ_45/DDR1_DQ_13	DDR0_CAB_0/DDR0_MA_13	AU2	M_A_BG#1 17,19
M_A_DQ46	U5	DDR0_DQ_46/DDR1_DQ_14	DDR0_CAA_9/DDR0_BG_1	AU3	DDRA_ACT# 17,19
M_A_DQ47	U4	DDR0_DQ_47/DDR1_DQ_15	DDR0_CAA_8/DDR0_ACT#	-	
M_A_DQ48	R2	DDR0_DQ_48/DDR1_DQ_32		AG3	DDR0_PAR 17,19
M_A_DQ49	R5	DDR0_DQ_49/DDR1_DQ_33	NC/DDR0_PAR	AU5	DDR0_ALERT# 17,19
M_A_DQ50	R4	DDR0_DQ_50/DDR1_DQ_34	NC/DDR0_ALERT#	-	
M_A_DQ51	P4	DDR0_DQ_51/DDR1_DQ_35		BR5 M_A_DQSN0	
M_A_DQ52	R5	DDR0_DQ_52/DDR1_DQ_36		BL3 M_A_DQSN1	
M_A_DQ53	P2	DDR0_DQ_53/DDR1_DQ_37	DDR0_DQSN_0/DDR0_DQSN_0	BG3 M_A_DQSN2	
M_A_DQ54	R1	DDR0_DQ_54/DDR1_DQ_38	DDR0_DQSN_1/DDR0_DQSN_1	BD3 M_A_DQSN3	
M_A_DQ55	P1	DDR0_DQ_55/DDR1_DQ_39	DDR0_DQSN_2/DDR0_DQSN_2	AA3 M_A_DQSN4	
M_A_DQ56	M4	DDR0_DQ_56/DDR1_DQ_40	DDR0_DQSN_3/DDR0_DQSN_5	U3 M_A_DQSN5	
M_A_DQ57	M1	DDR0_DQ_57/DDR1_DQ_41	DDR0_DQSN_4/DDR1_DQSN_0	P3 M_A_DQSN6	
M_A_DQ58	L4	DDR0_DQ_58/DDR1_DQ_42	DDR0_DQSN_5/DDR1_DQSN_1	L3 M_A_DQSN7	
M_A_DQ59	L2	DDR0_DQ_59/DDR1_DQ_43	DDR0_DQSN_6/DDR1_DQSN_4	-	
M_A_DQ60	M5	DDR0_DQ_60/DDR1_DQ_44	DDR0_DQSN_7/DDR1_DQSN_5	BP5 M_A_DQSP0	
M_A_DQ61	M2	DDR0_DQ_61/DDR1_DQ_45		BK3 M_A_DQSP1	
M_A_DQ62	L5	DDR0_DQ_62/DDR1_DQ_46	DDR0_DQSP_0/DDR0_DQSP_0	BF3 M_A_DQSP2	
M_A_DQ63	L1	DDR0_DQ_63/DDR1_DQ_47	DDR0_DQSP_1/DDR0_DQSP_1	BC3 M_A_DQSP3	
			DDR0_DQSP_2/DDR0_DQSP_4	AB3 M_A_DQSP4	
17,19 M_A_CB0	M_A_CB0	BA2	DDR0_DQSP_3/DDR0_DQSP_5	V3 M_A_DQSP5	
17,19 M_A_CB1	M_A_CB1	BA1	DDR0_DQSP_4/DDR1_DQSP_0	R3 M_A_DQSP6	
17,19 M_A_CB2	M_A_CB2	AY4	DDR0_DQSP_5/DDR1_DQSP_1	M3 M_A_DQSP7	
17,19 M_A_CB3	M_A_CB3	AY5	DDR0_DQSP_6/DDR1_DQSP_4	-	
17,19 M_A_CB4	M_A_CB4	BA5	DDR0_DQSP_7/DDR1_DQSP_5	AY3 M_A_DQSP8	
17,19 M_A_CB5	M_A_CB5	BA4		BA3 M_A_DQSN8	
17,19 M_A_CB6	M_A_CB6	AY1	DDR0_DQSP_8/DDR0_DQSP_8		
17,19 M_A_CB7	M_A_CB7	AY2	DDR0_DQSN_8/DDR0_DQSN_8		

NC/DDR0_ECC_0
NC/DDR0_ECC_1
NC/DDR0_ECC_2
NC/DDR0_ECC_3
NC/DDR0_ECC_4
NC/DDR0_ECC_5
NC/DDR0_ECC_6
NC/DDR0_ECC_7

1 OF 13

CPU_CFL-H_1440P DDR CHANNEL A

18,20 M_B_DQ[15:0]
18,20 M_B_DQ[31:16]
18,20 M_B_DQ[47:32]
18,20 M_B_DQ[48:63]

U22B

M_B_DQ0	BT11	DDR1_DQ_0/DDR0_DQ_16	DDR1_CKP_0/DDR1_CKP_0	AM9	M_B_DIM0_CLKP0 18
M_B_DQ1	BR11	DDR1_DQ_1/DDR0_DQ_17	DDR1_CKN_0/DDR1_CKN_0	AN9	M_B_DIM0_CLKN0 18
M_B_DQ2	BT9	DDR1_DQ_2/DDR0_DQ_18	DDR1_CKP_1/DDR1_CKP_1	AM7	M_B_DIM0_CLKP1 18
M_B_DQ3	BR8	DDR1_DQ_3/DDR0_DQ_19	DDR1_CKN_1/DDR1_CKN_1	AM8	M_B_DIM0_CLKN1 18
M_B_DQ4	BP11	DDR1_DQ_4/DDR0_DQ_20	NC/DDR1_CKP_2	AM11	M_B_DIM1_CLKP0 20
M_B_DQ5	BN11	DDR1_DQ_5/DDR0_DQ_21	NC/DDR1_CKN_2	AM10	M_B_DIM1_CLKN0 20
M_B_DQ6	BP8	DDR1_DQ_6/DDR0_DQ_22	NC/DDR1_CKP_3	AJ10	M_B_DIM1_CLKP1 20
M_B_DQ7	BN8	DDR1_DQ_7/DDR0_DQ_23	NC/DDR1_CKN_3	AJ11	M_B_DIM1_CLKN1 20
M_B_DQ8	BL12	DDR1_DQ_8/DDR0_DQ_24		AT8	
M_B_DQ9	BL11	DDR1_DQ_9/DDR0_DQ_25	DDR1_CKE_0/DDR1_CKE_0	AT10	M_B_CKE0 18
M_B_DQ10	BL8	DDR1_DQ_10/DDR0_DQ_26	DDR1_CKE_1/DDR1_CKE_1	AT7	M_B_CKE1 18
M_B_DQ11	BJ8	DDR1_DQ_11/DDR0_DQ_27	DDR1_CKE_2/DDR1_CKE_2	AT11	M_B_CKE2 20
M_B_DQ12	BJ11	DDR1_DQ_12/DDR0_DQ_28	DDR1_CKE_3/DDR1_CKE_3	-	M_B_CKE3 20
M_B_DQ13	BJ10	DDR1_DQ_13/DDR0_DQ_29		AF11	
M_B_DQ14	BL7	DDR1_DQ_14/DDR0_DQ_30	DDR1_CS#_0/DDR1_CS#_0	AE7	M_B_CS#0 18
M_B_DQ15	BJ7	DDR1_DQ_15/DDR0_DQ_31	DDR1_CS#_1/DDR1_CS#_1	AF10	M_B_CS#1 18
M_B_DQ16	BG11	DDR1_DQ_16/DDR0_DQ_48	NC/DDR1_CS#_2	AE10	M_B_CS#2 20
M_B_DQ17	BG10	DDR1_DQ_17/DDR0_DQ_49	NC/DDR1_CS#_3	-	M_B_CS#3 20
M_B_DQ18	BG8	DDR1_DQ_18/DDR0_DQ_50		AF7	
M_B_DQ19	BF8	DDR1_DQ_19/DDR0_DQ_51	DDR1_ODT_0/DDR1_ODT_0	AE8	M_B_ODT0 18
M_B_DQ20	BF11	DDR1_DQ_20/DDR0_DQ_52	NC/DDR1_ODT_1	AE9	M_B_ODT1 18
M_B_DQ21	BF10	DDR1_DQ_21/DDR0_DQ_53	NC/DDR1_ODT_2	AE11	M_B_ODT2 20
M_B_DQ22	BG7	DDR1_DQ_22/DDR0_DQ_54	NC/DDR1_ODT_3	-	M_B_ODT3 20
M_B_DQ23	BF7	DDR1_DQ_23/DDR0_DQ_55		AH10 M_B_A16	
M_B_DQ24	BB11	DDR1_DQ_24/DDR0_DQ_56	DDR1_CAB_3/DDR1_MA_16	AH11 M_B_A14	M_B_A16 18,20
M_B_DQ25	BC11	DDR1_DQ_25/DDR0_DQ_57	DDR1_CAB_2/DDR1_MA_14	AF8 M_B_A15	M_B_A14 18,20
M_B_DQ26	BB8	DDR1_DQ_26/DDR0_DQ_58	DDR1_CAB_1/DDR1_MA_15	-	M_B_A15 18,20
M_B_DQ27	BC8	DDR1_DQ_27/DDR0_DQ_59		AH8	
M_B_DQ28	BC10	DDR1_DQ_28/DDR0_DQ_60	DDR1_CAB_4/DDR1_BA_0	AH9	M_B_BS#0 18,20
M_B_DQ29	BB10	DDR1_DQ_29/DDR0_DQ_61	DDR1_CAB_6/DDR1_BA_1	AR9	M_B_BS#1 18,20
M_B_DQ30	BC7	DDR1_DQ_30/DDR0_DQ_62	DDR1_CAA_5/DDR1_BG_0	-	M_B_BG#0 18,20
M_B_DQ31	BB7	DDR1_DQ_31/DDR0_DQ_63		AJ9 M_B_A0	M_B_A[13:0] 18,20
M_B_DQ32	AA11	DDR1_DQ_32/DDR1_DQ_16	DDR1_CAB_9/DDR1_MA_0	AK6 M_B_A1	
M_B_DQ33	AA10	DDR1_DQ_33/DDR1_DQ_17	DDR1_CAB_8/DDR1_MA_1	AK5 M_B_A2	
M_B_DQ34	AC11	DDR1_DQ_34/DDR1_DQ_18	DDR1_CAB_5/DDR1_MA_2	AL5 M_B_A3	
M_B_DQ35	AC10	DDR1_DQ_35/DDR1_DQ_19	NC/DDR1_MA_3	AL6 M_B_A4	
M_B_DQ36	AA7	DDR1_DQ_36/DDR1_DQ_20	NC/DDR1_MA_4	AM6 M_B_A5	
M_B_DQ37	AA8	DDR1_DQ_37/DDR1_DQ_21	DDR1_CAA_0/DDR1_MA_5	AN7 M_B_A6	
M_B_DQ38	AC8	DDR1_DQ_38/DDR1_DQ_22	DDR1_CAA_2/DDR1_MA_6	AN10 M_B_A7	
M_B_DQ39	AC7	DDR1_DQ_39/DDR1_DQ_23	DDR1_CAA_4/DDR1_MA_7	-	
M_B_DQ40	W8	DDR1_DQ_40/DDR1_DQ_24	DDR1_CAA_3/DDR1_MA_8	AN8 M_B_A8	
M_B_DQ41	W7	DDR1_DQ_41/DDR1_DQ_25	DDR1_CAA_1/DDR1_MA_9	AR11 M_B_A9	
M_B_DQ42	Y10	DDR1_DQ_42/DDR1_DQ_26	DDR1_CAB_7/DDR1_MA_10	AH7 M_B_A10	
M_B_DQ43	V11	DDR1_DQ_43/DDR1_DQ_27	DDR1_CAA_7/DDR1_MA_11	AN11 M_B_A11	
M_B_DQ44	W11	DDR1_DQ_44/DDR1_DQ_28	DDR1_CAA_6/DDR1_MA_12	AR10 M_B_A12	
M_B_DQ45	W10	DDR1_DQ_45/DDR1_DQ_29	DDR1_CAB_0/DDR1_MA_13	AF9 M_B_A13	
M_B_DQ46	V7	DDR1_DQ_46/DDR1_DQ_30	DDR1_CAA_9/DDR1_BG_1	AR7	
M_B_DQ47	V8	DDR1_DQ_47/DDR1_DQ_31	DDR1_CAA_8/DDR1_ACT#	AT9	M_B_BG#1 18,20
M_B_DQ48	R11	DDR1_DQ_48/DDR1_DQ_48		-	DDRB_ACT# 18,20
M_B_DQ49	P11	DDR1_DQ_49/DDR1_DQ_49	NC/DDR1_PAR	AJ7	
M_B_DQ50	P7	DDR1_DQ_50/DDR1_DQ_50	NC/DDR1_ALERT#	AR8	DDR1_PAR 18,20
M_B_DQ51	R8	DDR1_DQ_51/DDR1_DQ_51		-	DDR1_ALERT# 18,20
M_B_DQ52	R10	DDR1_DQ_52/DDR1_DQ_52		BN9 M_B_DQSN0	
M_B_DQ53	P10	DDR1_DQ_53/DDR1_DQ_53	DDR1_DQSN_0/DDR0_DQSN_2	BL9 M_B_DQSN1	M_B_DQSN0 18,20
M_B_DQ54	R7	DDR1_DQ_54/DDR1_DQ_54	DDR1_DQSN_1/DDR0_DQSN_3	BG9 M_B_DQSN2	M_B_DQSN1 18,20
M_B_DQ55	P8	DDR1_DQ_55/DDR1_DQ_55	DDR1_DQSN_2/DDR0_DQSN_6	BC9 M_B_DQSN3	M_B_DQSN2 18,20
M_B_DQ56	L11	DDR1_DQ_56/DDR1_DQ_56	DDR1_DQSN_3/DDR0_DQSN_7	AC9 M_B_DQSN4	M_B_DQSN3 18,20
M_B_DQ57	M11	DDR1_DQ_57/DDR1_DQ_57	DDR1_DQSN_4/DDR1_DQSN_2	W9 M_B_DQSN5	M_B_DQSN4 18,20
M_B_DQ58	L7	DDR1_DQ_58/DDR1_DQ_58	DDR1_DQSN_5/DDR1_DQSN_3	R9 M_B_DQSN6	M_B_DQSN5 18,20
M_B_DQ59	M8	DDR1_DQ_59/DDR1_DQ_59	DDR1_DQSN_6/DDR1_DQSN_6	M9 M_B_DQSN7	M_B_DQSN6 18,20
M_B_DQ60	L10	DDR1_DQ_60/DDR1_DQ_60	DDR1_DQSN_7/DDR1_DQSN_7	-	M_B_DQSN7 18,20
M_B_DQ61	M10	DDR1_DQ_61/DDR1_DQ_61		BP9 M_B_DQSP0	
M_B_DQ62	M7	DDR1_DQ_62/DDR1_DQ_62	DDR1_DQSP_0/DDR0_DQSP_2	BJ9 M_B_DQSP1	M_B_DQSP0 18,20
M_B_DQ63	L8	DDR1_DQ_63/DDR1_DQ_63	DDR1_DQSP_1/DDR0_DQSP_3	BF9 M_B_DQSP2	M_B_DQSP1 18,20
			DDR1_DQSP_2/DDR0_DQSP_6	BB9 M_B_DQSP3	M_B_DQSP2 18,20
18,20 M_B_CB0	M_B_CB0	AW11	DDR1_DQSP_3/DDR0_DQSP_7	AA9 M_B_DQSP4	M_B_DQSP3 18,20
18,20 M_B_CB1	M_B_CB1	AY11	DDR1_DQSP_4/DDR1_DQSP_2	V9 M_B_DQSP5	M_B_DQSP4 18,20
18,20 M_B_CB2	M_B_CB2	AY8	DDR1_DQSP_5/DDR1_DQSP_3	P9 M_B_DQSP6	M_B_DQSP5 18,20
18,20 M_B_CB3	M_B_CB3	AW8	DDR1_DQSP_6/DDR1_DQSP_6	L9 M_B_DQSP7	M_B_DQSP6 18,20
18,20 M_B_CB4	M_B_CB4	AY10	DDR1_DQSP_7/DDR1_DQSP_7	-	M_B_DQSP7 18,20
18,20 M_B_CB5	M_B_CB5	AW10		AW9 M_B_DQSP8	
18,20 M_B_CB6	M_B_CB6	AY7	DDR1_DQSP_8/DDR1_DQSP_8	AY9 M_B_DQSN8	M_B_DQSP8 18,20
18,20 M_B_CB7	M_B_CB7	AW7	DDR1_DQSN_8/DDR1_DQSN_8	-	M_B_DQSN8 18,20

NC/DDR1_ECC_0
NC/DDR1_ECC_1
NC/DDR1_ECC_2
NC/DDR1_ECC_3
NC/DDR1_ECC_4
NC/DDR1_ECC_5
NC/DDR1_ECC_6
NC/DDR1_ECC_7

R818 121/F_4 SM_RCOMP_0 G1
R816 75/F_4 SM_RCOMP_1 H1
R815 100/F_4 SM_RCOMP_2 J2

DDR_RCOMP_0
DDR_RCOMP_1
DDR_RCOMP_2

2 OF 13

DDR_VREF_CA
DDR0_VREF_DQ
DDR1_VREF_DQ

BN13 SMDDR_VREF_CA
BP13 SMDDR_VREF_DQ0_M3
BR13 SMDDR_VREF_DQ1_M3

SMDDR_VREF_CA 17
TP60
SMDDR_VREF_DQ1_M3 18

CPU_CFL-H_1440P DDR CHANNEL B

Quanta Computer Inc.
PROJECT : ZGQ

Size	Document Number	Rev
	CFL 3/7 (DDR4 I/F)	1A

Date: Monday, March 12, 2018 Sheet 4 of 73

VCCGT

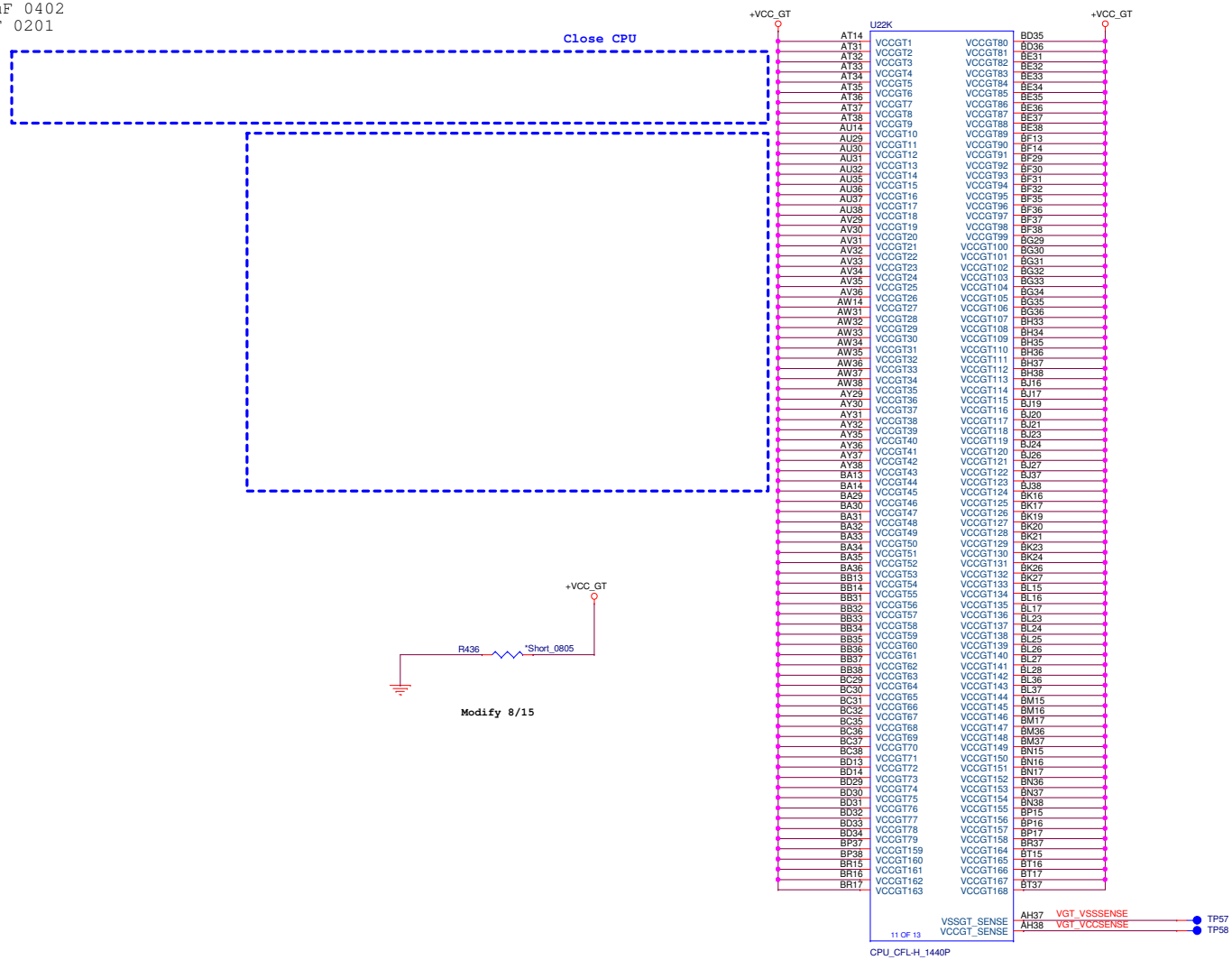
Edge cap
4x 47uF 0805
7x 22uF 0603

Backside cap
10x 10uF 0402
12x 1uF 0201

CFL Processor (POWER)

05

Close CPU



Quanta Computer Inc.		
PROJECT : ZGQ		
Size	Document Number: CFL 4/7 (POWER)	Rev: 1A
Date: Monday, March 12, 2018	Sheet 5 of 73	

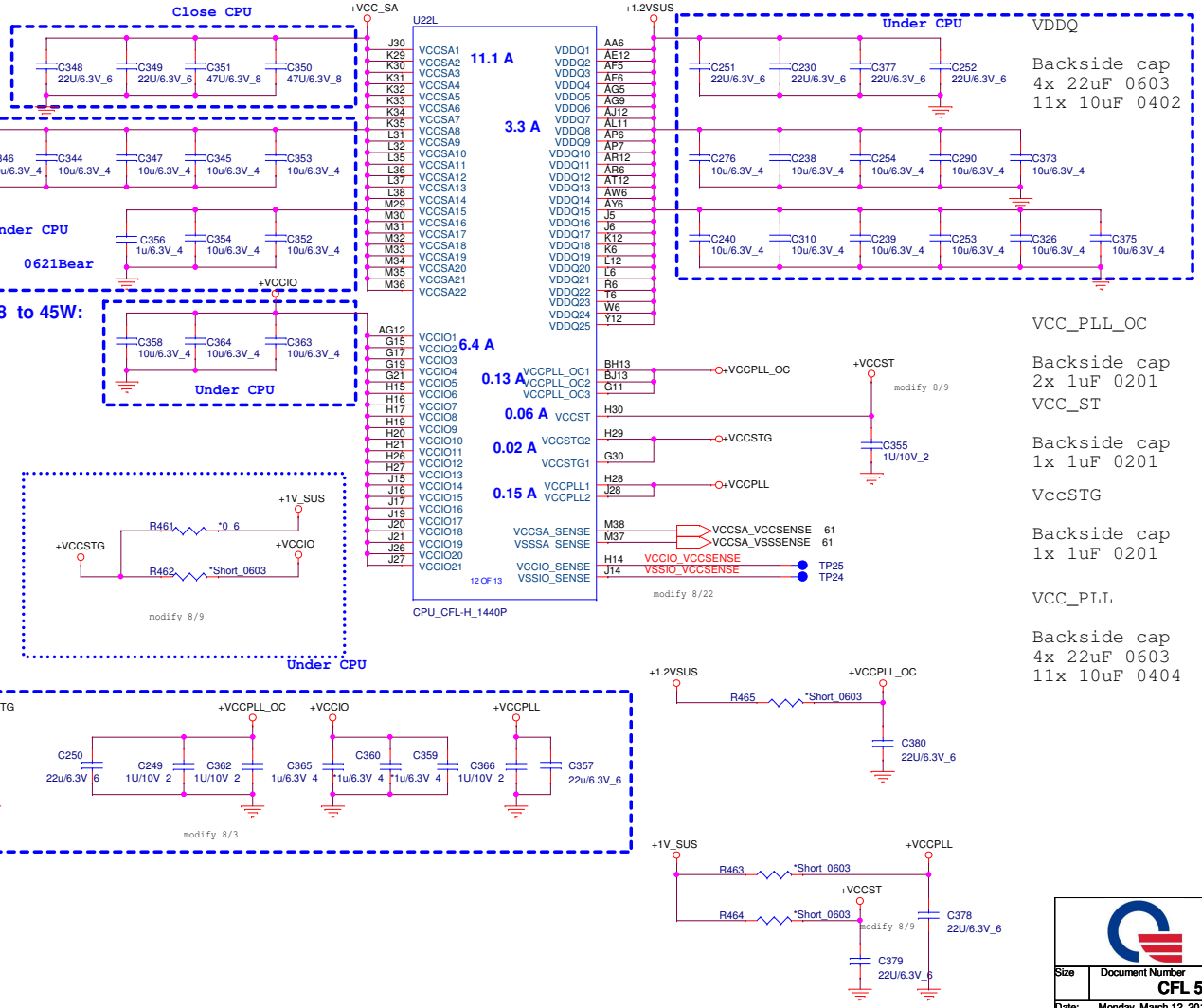
Follow CFL H EDS page 128 to 45W(GT2): VCCSA=11.1A

Follow CFL H EDS page 127 45W: VDDQ=3.3A (LPDDR4)

+VCC_SA

Edge cap
2x 47uF 0805
2x 22uF 0805

Backside cap
7x 10uF 0402



VDDQ

Backside cap
4x 22uF 0603
11x 10uF 0402

VCC_PLL_OC

Backside cap
2x 1uF 0201

VCC_ST

Backside cap
1x 1uF 0201

VccSTG

Backside cap
1x 1uF 0201

VCC_PLL

Backside cap
4x 22uF 0603
11x 10uF 0404

Follow CFL H EDS P128 to 45W: VCCIO, +VCCIO = 6.4A

+VCC_IO

Backside cap
3x 10uF 0402

Quanta Computer Inc.

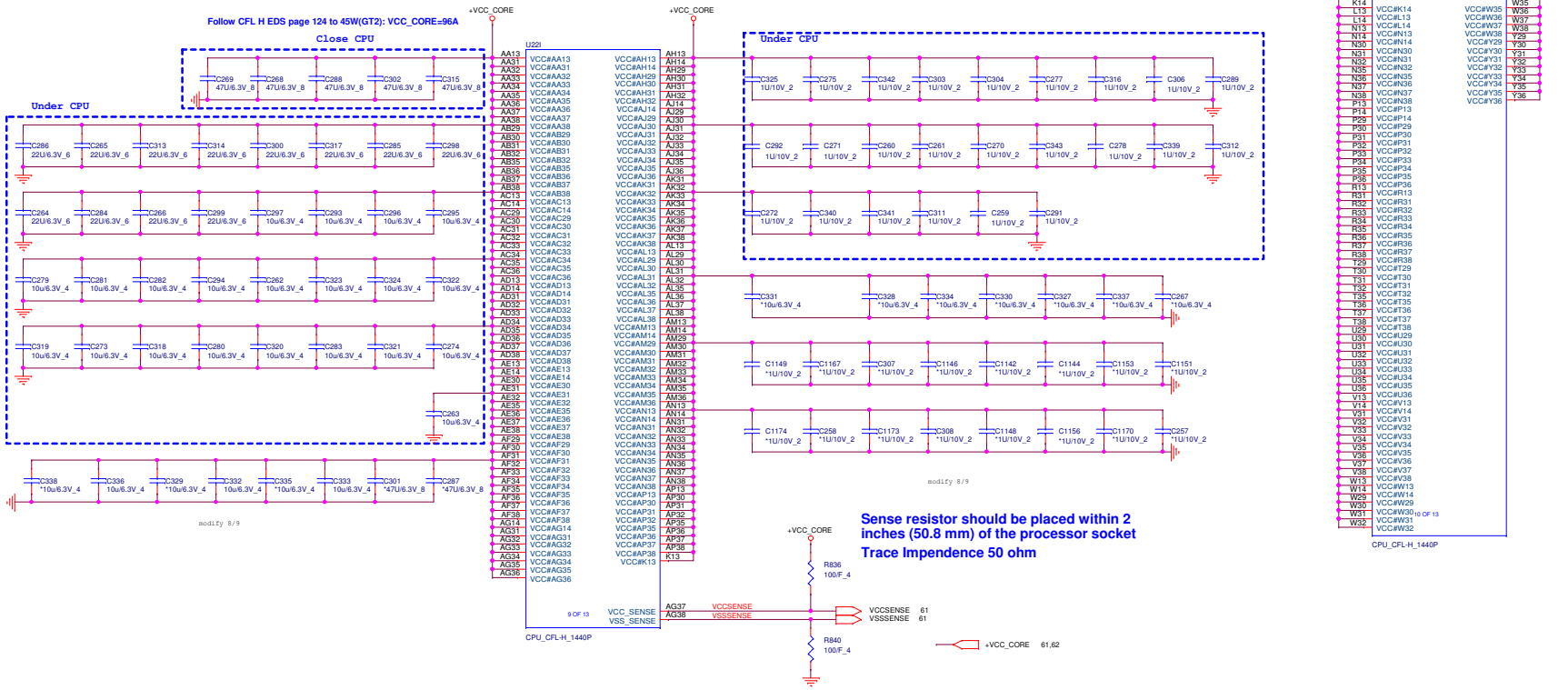
PROJECT : ZGQ

Size	Document Number	Rev
	CFL 5/7 (POWER&GND)	1A
Date: Monday, March 12, 2018	Sheet 6 of 73	

Vcc (VCC_CORE)

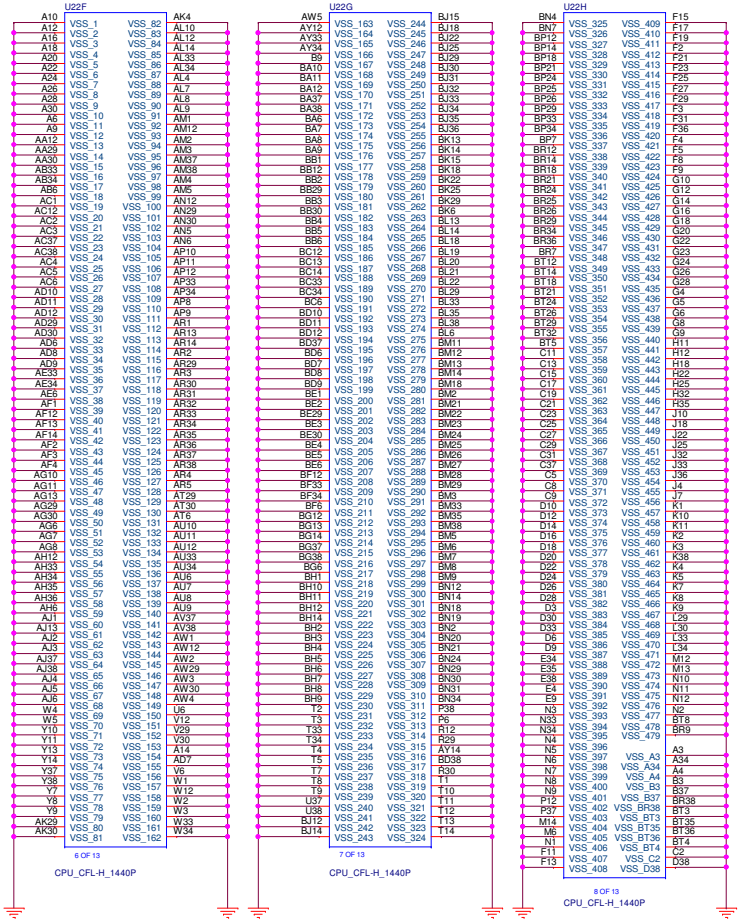
Edge cap
8 x 47uF 0805

Backside cap
12x 22uF 0603
42x 10uF 0402
48x 1uF 0201
24x 0201 (placeholder)

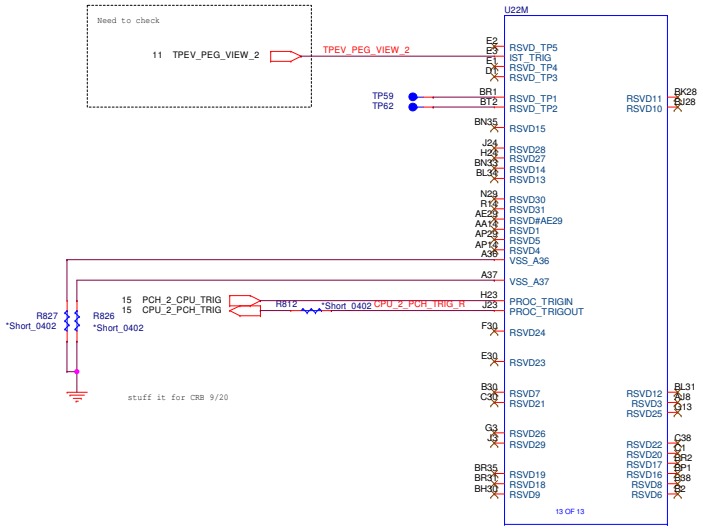


Quanta Computer Inc.			
PROJECT : ZGQ			
Size	Document Number		Rev
	CFL 6/7 (POWER&GND)		1A
Date: Monday, March 12, 2018	Sheet 7	of 73	

CFL-H Processor (GND)



CFL-H Processor (RESERVED, CFG)



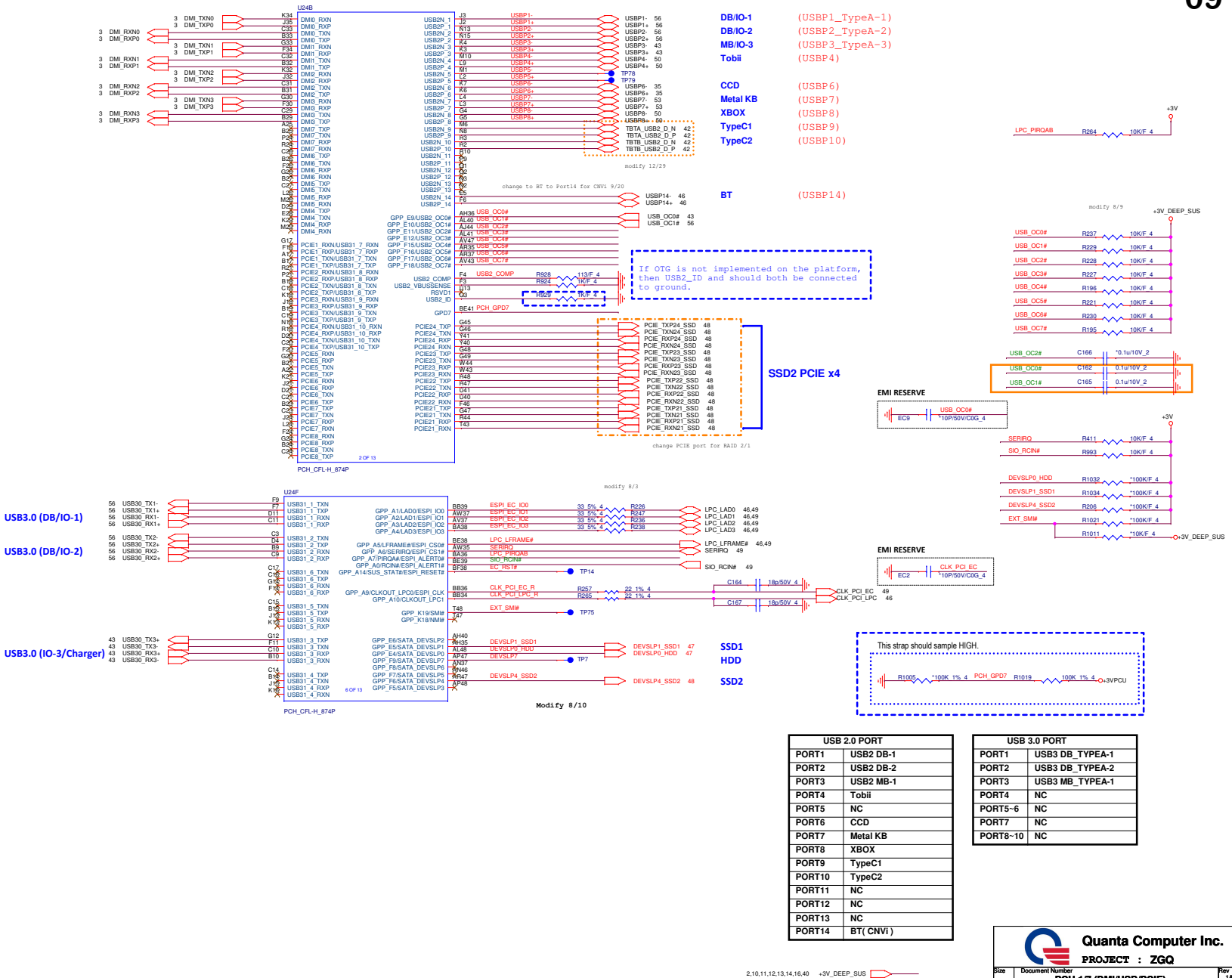
Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a OxM board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asseted x0 = PEG wait for BIOS fro training	

Quanta Computer Inc.

PROJECT : ZGQ

Size	Document Number	Rev
	CFL 7/7 (GND)	1A

Date: Monday, March 12, 2018 Sheet 8 of 73



USB 2.0 PORT	
PORT1	USB2 DB-1
PORT2	USB2 DB-2
PORT3	USB2 MB-1
PORT4	Tobii
PORT5	NC
PORT6	CCD
PORT7	Metal KB
PORT8	XBOX
PORT9	TypeC1
PORT10	TypeC2
PORT11	NC
PORT12	NC
PORT13	NC
PORT14	BT(CNVi)

USB 3.0 PORT	
PORT1	USB3 DB_TYPEA-1
PORT2	USB3 DB_TYPEA-2
PORT3	USB3 MB_TYPEA-1
PORT4	NC
PORT5~6	NC
PORT7	NC
PORT8~10	NC

2,10,11,12,13,14,16,40 +3V_DEEP_SUS

Quanta Computer Inc.
PROJECT : ZGQ

Size	Document Number	Rev
	PCH 1/7 (DMI/USB/PCIE)	1A
Date: Monday, March 12, 2018	Sheet 9 of 73	

HDA Bus(CLG)

C1207 *47p/50V_4 ACZ_BCLK

U24D

44 PCH_AZ_CODEC_BITCLK R936 33_4 ACZ_BCLK BD11
44 PCH_AZ_CODEC_SDIN0 R935 Short_0402 ACZ_SDIN0_R BE11
44 PCH_AZ_CODEC_SDOUT R940 33_4 ACZ_SDO BF12
44 PCH_AZ_CODEC_SYNC R941 33_4 ACZ_SYNC BG12
44 PCH_AZ_CODEC_RST# R934 33_4 ACZ_RST# BE10

HDA_BCLK/I2S0_SCLK
HDA_SDI0/I2S0_RXD
HDA_SDO/I2S0_TXD
HDA_SYNC/I2S0_SFRM
HDA_RST#/I2S1_SCLK
HDA_SDI1/I2S1_RXD
I2S1_TXD/SNDW2_DATA
I2S1_SFRM/SNDW2_CLK

3 AUD_AZACPU_SDO_R R908 30_4 AUD_AZACPU_SDO AM2
3 AUD_AZACPU_SDI R930 30_4 AUD_AZACPU_SDI_R AN3
3 AUD_AZACPU_SCLK AUD_AZACPU_SCLK_R AM3
HDACPU_SDO
HDACPU_SDI
HDACPU_SCLK

Modify 8/10

46 PCM_CLK R399 *0_4 I2S2_SCLK AV18
46 PCM_IN R423 *0_4 I2S2_RXD AW18
MODEM_CLKREQ_C AW17
CNV_RF_RESET#_C BA17
BE16
BF15
Add R1204 for CNV1 9/29 75K/F_4 R1204 BD15
AV15
AW15
GPP_D8/I2S2_SCLK
GPP_D7/I2S2_RXD
GPP_D6/I2S2_TXD/MODEM_CLKREQ
GPP_D5/I2S2_SFRM/CNV_RF_RESET#
GPP_D20/DMIC_DATA0/SNDW4_DATA
GPP_D19/DMIC_CLK0/SNDW4_CLK
GPP_D18/DMIC_DATA1/SNDW3_DATA
GPP_D17/DMIC_CLK1/SNDW3_CLK

16 RTC_RST# RTC_RST# BE47
SRTC_RST# BD46
RTCRST#
SRTCRST#

SYS_PWROK R211 *0_4 EC_PWROK_R AY42
16,49 RSMRST# R371 Short_0402 PCH_RSMRST# BA47
PCH_PWROK
RSMRST#
modify 8/9

PCH_RSMRST# R240 *Short_0402 DPWROK_R AW41
DSW_PWROK
SMBALERT# BE25
SMB_PCH_CLK BE26
SMB_PCH_DAT BF26
SMLOALERT# BF24
SMB_ME0_CLK BF25
SMB_ME0_DAT BE24
SMB1ALERT# BD33
SMB_ME1_CLK BF27
SMB_ME1_DAT BE27
GPP_C2/SMBALERT#
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C5/SML0ALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_B23/SML1ALERT#/PCHHOT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA

4 OF 13

PCH_CFL-H_874P

GPP_A12/BM_BUSY#/ISH_GP6/SX_EXIT_HOLDOFF#
GPP_A8/CLKRUN#
GPD11/LANPHYPC
GPD9/SLP_WLAN#
DRAM_RESET#
GPP_B2/VRALERT#
GPP_B1/GSPI1_CS1#/TIME_SYNC1
GPP_B0/GSPI0_CS1#
GPP_K17/ADR_COMPLETE
GPP_B11/I2S_MCLK
SYS_PWROK
WAKE#
GPD6/SLP_A#
SLP_LAN#
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
GPD8/SUSCLK
GPD0/BATLOW#
GPP_A15/SUSACK#
GPP_A13/SUSWARN#/SUSPWRDNACK
GPD2/LAN_WAKE#
GPD1/ACPRESENT
SLP_SUS#
GPD3/PWRBTN#
SYS_RESET#
GPP_B14/SPKR
CPUPWRGD
ITP_PMODE
PCH_JTAGX
PCH_JTAG_TMS
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TCK

BF36 CLKRUN# CLKRUN# 49
BF41 LAN_DIS# TP11
BD42 SLP_WLAN_N TP10
BB46 DDR_DRAMRST#_L R1020 *Short_0402 C1255 *0.1u/16V_4
BE32 GPP_B2 R984 *0_4 DDR_DRAMRST# 17,18,19,20
BF33 UART_WAKE_N 46
BE29
BD47
AP29 MPHY_EXT_PWR_GATE
AU3 SYS_PWROK_R R210 *Short_0402 SYS_PWROK TP9
modify 8/9
Modify 8/10
BB47 PCH_WAKE#_L R1031 *Short_0402 PCIE_WAKE# 39,46,55
BE40 SLP_A#_L R995 *Short_0402 SLP_A# 16
BF40 SLP_LAN# TP13
BC28 PCH_SLP_S0i#_L R982 *Short_0402 PCH_SLP_S0i# 16
BF42 SLP_S3#_L R998 *Short_0402 SUSB# 16,49
BE42 SLP_S4#_L R999 *Short_0402 SUSC# 16,49 change BOM 9/4
BC42 SLP_S5#_L R994 *Short_0402 SLP_S5# 16
BE45 SUSCLK32 R261 *0_4 SUSCLK 46
BF44 BATLOW# BATLOW# 39
BE35 SUSACK# R988 *Short_0402
BC37 SUSWARN#
BG44 LANWAKE_N R1002 *0_4 TP72
BG42 ACPRESENT ACPRESENT 49
BG39 PCH_SLP_SUS# TP12
BE46 DNBSWON# DNBSWON# 49
AU2 XDP_DBRESET# XDP_DBRESET# 16
AW29 ACZ_SPKR ACZ_SPKR 44
AE3 PROCPWRGD PROCPWRGD 2
AL3 ITP_PMODE ITP_PMODE 16
AH4 PCH_JTAGX R903 *Short_0402 H_TCK 2,16
AJ4 PCH_TMS R906 *Short_0402 H_TMS 2,16
AH3 PCH_TDO R904 *Short_0402 H_TDO 2,16
AH2 PCH_TDI R920 *Short_0402 H_TDI 2,16
AJ3 PCH_TCK R921 51_4
PCH_TCK 16

+1.2VSUS
DDR_DRAMRST# R837 470/F_4
+3V_DEEP_SUS
MPHY_EXT_PWR_GATE R293 200K/F_4
PCH_WAKE#_L R1007 4.7K/F_4 change R1007 to 4.7K for CNV1 9/29
GPP_B2 R985 4.7K/F_4 change R985 to 4.7K for CNV1 9/29
LANWAKE_N R1001 4.7K/F_4
SUSACK# R989 *10K/F_4
XDP_DBRESET# R931 10K/F_4
SUSCLK32 R258 *10K/F_4
SUSWARN# R990 *10K/F_4
BATLOW# R1040 10K/F_4
ACPRESENT R1000 100K/F_4
PCH_SLP_S0i#_L R975 100K/F_4
SMB_ME0_CLK R967 2.2K_5%_4
SMB_ME0_DAT R961 2.2K_5%_4
SMB_ME1_CLK R973 2.2K_5%_4
SMB_ME1_DAT R974 2.2K_5%_4
SMB_PCH_CLK R972 2.2K_5%_4
SMB_PCH_DAT R976 2.2K_5%_4
modify 8/9
+1.05V_DEEP_SUS
PCH_TDO R919 *51_4
+3V
CLKRUN# R310 10K/F_4

ME Lock

49 ME_WR# R939 1K/F_4 ACZ_SDO

0 = *Enable security in the Flash Description (iPD 20K)
1 = Disable Flash Descriptor Security (Override)

TLS CONFIDENTIALITY ENABLED
HIGH: Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.(CRB)
LOW: security measures defined in the Flash Descriptor. (Default)

+3V_DEEP_SUS
R353 *1K_1%_4
ME_WR#
R354 *1K_1%_4

2,9,11,12,13,14,16,40 +3V_DEEP_SUS

EC reset RTC

SRTC_RST#
49 CLR_CMOS
Q20 *2N7002KTB
R409 *100K_1%_4
RTC_RST#
CLR_CMOS
Q22 2N7002KTB

PCH/EC

+3V_DEEP_SUS
+3VPCU R1003 *4.7K/F_4
41,45,49,50 2ND_MBDATA
Q96
SMB_ME1_DAT
modify 8/9
+3VPCU R1008 *4.7K/F_4
41,45,49,50 2ND_MBCLK
SMB_ME1_CLK
2N7002KDW

XDP/DDR

+3V
+3V R403 4.7K/F_4
16,17,18,19,20 PCH_SMBDATA
Q33
SMB_PCH_DAT
modify 8/9
+3V R417 4.7K/F_4
16,17,18,19,20 PCH_SMBCLK
SMB_PCH_CLK
2N7002KDW

CNVi

+3V_DEEP_SUS +1.8V_DEEP_SUS
R1223 10K/F_4
R1221 4.7K/F_4
CNV_RF_RESET# 46
CNV_RF_RESET#_C
Q104A
Q104B
PJX138K
PJX138K

Modify the circuit 10/19
Add 10/18 Intel#571006
+3V_DEEP_SUS +1.8V_DEEP_SUS
R1222 10K/F_4
R1220 4.7K/F_4
MODEM_CLKREQ 46
MODEM_CLKREQ_C
Q103A
Q103B
PJX138K
PJX138K

GPP_C5/SML0ALERT#
0 = LPC is selected (for EC). (Default)
1 = eSPI is selected (for EC).

ESPI/LPC SELECT STRAP
HIGH:eSPI Is selected for EC.
LOW: LPC Is selected for EC. (Default)
+3V_DEEP_SUS
R970 *4.7K_1%_4
SML0ALERT#
R963 100K/F_4
modify 8/9

RTC Circuitry(RTC)

RTC Power trace width 20mils.
+3VPCU R978 1.5K/_4
R951 47K/F_4
+3V_RTC_0
+3V_RTC_0 R953 1K/F_4 +3V_RTC_1
+3V_RTC_2
30mils
+3V_RTC
BAT54CW D72
R979 27K_4
RTC_RST#
J1 *SOLDERJUMPER-2
C1217 1u/6.3V_4
R971 27K_4
SRTC_RST#
C1214 1u/6.3V_4
C1211 1u/6.3V_4
(20mils)
3 R947 4.7K_1%_4 R945 4.7K_1%_4 5VPCU
Q95 METR3904-G
R969 68.1K_1%_4
RTC_CONN DFHS02F5032 CON3
(20mils)
RTC_N03
R962 150K_1%_4
Correct pin defined 9/20
modify 8/9

SYSPWOK

+3V_DEEP_SUS
C163 *0.1u/10V_2
SYS_PWROK
EC_PWROK
EC_PWROK 49
IMVP_PWRGD 2,61
U8 *NL17SZ08DFT2G
R253 *0_5%_4
R224 *10K_1%_2
R239 0_5%_4
EC_PWROK_R R219 *Short_0402 PCH_PWROK 49
R212 *0_5%_4
SYS_PWROK_R R216 *0_5%_4 EC_PWROK

DP_PWROK

DPWROK_R R255 680K/F_4
SYS_PWROK_R R213 10K_1%_2
PCH_RSMRST# R248 *10K_1%_2
modify 8/9

TOP SWAP OVERRIDE STRAP
HIGH:TOP SWAP ENABLED (CRB)
LOW:TOP SWAP DISABLED(DEFAULT)
ACZ_SPKR
R276 20K/F_4

This signal has an internal pull-down.
0 = Disable IntelR DCI-OOB (Default)
1 = Enable IntelR DCI-OOB
+3V_DEEP_SUS
R277 150K/F_4
SMB1ALERT#
modify 8/9
R279 *20K_1%_4

TLS CONFIDENTIALITY ENABLED
HIGH:1 Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). (CRB)
LOW: Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
+3V_DEEP_SUS
R966 4.7K_1%_4
SMBALERT#
R968 *20K_1%_4

Quanta Computer Inc.
PROJECT : ZGQ
Size | Document Number: PCH 2/7 (HDA/SMBUS) | Rev: 1A
Date: Monday, March 12, 2018 | Sheet 10 of 73

HSIO MUX PORT	
PCIE1-8	NC
PCIE9-12	SSD1 SATA/PCIE * 4
PCIE13	HDD (SATA2)
PCIE14	LAN
PCIE15	WLAN
PCIE16	NC
PCIE17-20	Apline Ridge
PCIE21-24	SSD2 PCIE * 4

CNVi

Modify 8/10

EMI RESERVE

SSD1 PCIE x4

LAN

HDD SATA

SSD1 PCIE x4

modify it 9/20

TBT PCIE x4

2/5 modify

PCH_CFL-H_874P

SSD1 PCIE x4

WLAN

2/5 modify

TBT PCIE x4

EMI RESERVE

Add 12/19

SSD SATA I/F --> H

SSD PCIE I/F --> L

For SSD1 Det

modify 8/9

PLT_ID0 PU for REVE PCB 2/1

RESERVE

24-MHz Crystal Specifications (Sheet 2 of 2)

Parameter	Symbol	Recommended Value
Temperature Stability	Df/f_o	±30ppm
Aging	Df/f_o	±5ppm
Crystal Loading	C_{load}	18-20pF

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-H needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-H.

24MHZ+-20PPM

*DLP0NSN900HL2L

Crystal Components with Surrounding 10 mil Wide GND Shield Trace Break Out:4-10 mil Wide GND Shield Trace

RTC Clock 32.768KHz

Y5 32.768KHZ/20ppm

chang P/N to CS04872FB11 8/18

U24G

U24M

CNVI for WLAN

Swap SSD2 and TBT CLK for PCIE SSD RAID 2/1

Swap SSD2 and TBT REQ for PCIE SSD RAID 2/1

Close WiFi Connector

VCCIO Power Gate control for C10

stuff R1037 and unstuff R1039 for PCIE SSD RAID 2/1

Modify 8/10

PCH_CFL-H_874P

Quanta Computer Inc.

PROJECT : ZGQ

Size	Document Number	Rev
	PCH 3/7 (SATA/LPC/CLK)	1A

Date: Monday, March 12, 2018 Sheet 11 of 73

PCH Strap Pin

RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

+3V_DEEP_SUS
R235 *20K/F_4
PCH_SPI1_SO_L
R254 *4.7K/F_4

ESPI FLASH SHARING MODE

HIGH:SLAVE ATTACEHD FLASH SHARING
LOW: 0: MASTER ATTACHED FLASH SHARING
This strap should sample LOW.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

+3V_DEEP_SUS
R1025 *4.7K/F_4
SML2ALERT#
R1014 *30K_4

PLTRST#(CLG)

U24A
PCH_CFL-H_874P
1 OF 13

GPP_B13/PLTRST# — AV29 — PCI_PLTRST#
GPP_A11/PME#/SD_VDD2_PWR_EN# — BE36
RSVD#R15 — R15
RSVD#R13 — R13
VSS — AL37
TP#AN35 — AN35
SPI0_MOSI — AU41
SPI0_MISO — BA45
SPI0_CS0# — AV47
SPI0_CLK — AW47
SPI0_CS1# — AW48
SPI1_IO2 — AY48
SPI1_IO3 — BA46
SPI0_IO2 — AY48
SPI0_IO3 — BA46
SPI0_CS2# — AT40
GPP_D1/SPI1_CLK/SBK1_BK1 — BF19
GPP_D0/SPI1_CS#/SBK0_BK0 — BF19
GPP_D3/SPI1_MOSI/SBK3_BK3 — BF18
GPP_D2/SPI1_MISO/SBK2_BK2 — BE18
GPP_D22/SPI1_IO3 — BC17
GPP_D21/SPI1_IO2 — BD17
GPP_K16/GSXCLK — V47
GPP_K12/GSXDOUT — W6
GPP_K13/GSXSLOAD — W8
GPP_K14/GSXDIN — W46
GPP_K15/GSXSRESET# — AA45
GPP_E3/CPU_GP0 — AL47
GPP_E7/CPU_GP1 — AM45
GPP_B3/CPU_GP2 — BF32 — KBL_DET# — TP71
GPP_B4/CPU_GP3 — BC33
GPP_H18/SML4ALERT# — AE44
GPP_H17/SML4DATA — AJ46 — SMB_ME4_DAT
GPP_H16/SML4CLK — AE43 — SMB_ME4_CLK
GPP_H15/SML3ALERT# — AC47 — PCH_GPP_H15
GPP_H14/SML3DATA — AD48 — SMB_ME3_DAT
GPP_H13/SML3CLK — AF47 — SMB_ME3_CLK
GPP_H12/SML2ALERT# — AB47 — SML2ALERT#
GPP_H11/SML2DATA — AD47 — SMB_ME2_DAT
GPP_H10/SML2CLK — AE48 — SMB_ME2_CLK
INTRUDER# — BB44 — SM_INTRUDER# — R260 1M/F_4 — +3V_RTC

Modify 8/10

TP15, TP16, TP8, TP18, TP70, TP69, TP68, TP67

16 PCH_SPI1_SI
PCH_SPI1_SI R223 33_4 PCH_SPI1_SI_L
PCH_SPI1_SO R222 33_4 PCH_SPI1_SO_L
PCH_SPI_CS0# R1022 Short_0402 PCH_SPI_CS0#_L
PCH_SPI1_CLK R1012 33_4 PCH_SPI1_CLK_L
SPI_TPM_CS# R278 33_4 SPI_TPM_CS#_L
TS_SPI1_CLK R952 33_4 TS_SPI1_CLK_R
TS_SPI1_CS# R957 33_4 TS_SPI1_CS#_R
TS_SPI1_MISO R950 33_4 TS_SPI1_MOSI_R
TS_SPI1_MOSI R948 33_4 TS_SPI1_MISO_R

EMI RESERVE
EC6 PCH_SPI1_CLK *10P/50V/C0G_4

RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

modify 8/9
+3V_DEEP_SUS
SMB_ME4_CLK R263 1K/F_4
SMB_ME4_DAT R249 1K/F_4
SMB_ME3_CLK R250 1K/F_4
SMB_ME3_DAT R1023 1K/F_4
SMB_ME2_CLK R1012 1K/F_4
SMB_ME2_DAT R1013 1K/F_4

RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

update vlaue follow intel command 8/8
+3V_DEEP_SUS
R234 100K/F_4
PCH_SPI1_SI_L
R266 *4.7K/F_4

This strap should sample HIGH. follow intel command 8/8
R259 *100K/F_4 PCH_GPP_H15 R256 100K/F_4 +3V_DEEP_SUS

+3VPCU
KBL_DET# R983 *100K/F_4
C1221 *0.1U/16V_4
ESD

RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

update vlaue follow intel command 8/8
+3V_DEEP_SUS
R1028 100K/F_4
SPI1_IO2
R1009 *4.7K/F_4

RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

update vlaue follow intel command 8/8
+3V_DEEP_SUS
R1029 100K/F_4
SPI1_IO3
R1010 *100_4

PCH SPI ROM(CLG)

PCH 6*5mm WSON 32M SPI ROM Socket

+3V_DEEP_SUS
Follow VSPI level (1.8V or 3.3V)
R187 0_4 +SPI_VCC
C1258 1u/10V_4
R1035 4.7K/F_4
R208 *2.55K/F_4

2nd source AKE3DZN0Q02

U26
CE# VDD
SCK
SI
SO HOLD#
WP# VSS
BIOS SOCKET
AKE3DF-KN01

PCH_SPI_CS0#
PCH_SPI1_CLK
PCH_SPI1_SI
PCH_SPI1_SO
SPI1_IO2
16 XDP_SPI_IO2
R1038 0_4 SPI1_IO2 R1042 33_4 PCH_SPI_IO2
+SPI_VCC R1036 *1K_1%_4 Modify 8/10
+SPI_VCC R193 *1K_1%_4
C156 0.1u/16V_4
PCH_SPI_IO3 R194 33_4 SPI1_IO3

change U26 footprint name to soic8-7_9-1_27 10/03

Socket:DG008000011

EC

49 PCH_SPI_SI_EC R217 33_4 PCH_SPI1_SI
49 PCH_SPI_SO_EC R214 33_4 PCH_SPI1_SO
49 SPI_CS0#_UR_ME R1016 Short_0402 PCH_SPI_CS0#
49 PCH_SPI_CLK_EC R1039 33_4 PCH_SPI1_CLK

Modify 8/10

PLTRST#(CLG)

+3V_DEEP_SUS
C1381 0.1u/16V_4
PCI_PLTRST# — 2
U25 MC74VHC1G08DFT2G
4 PLTRST#
PLTRST# 21,39,46,47,48,49,50,55
R977 100K/F_4

Quanta Computer Inc.
PROJECT : ZGQ

Size	Document Number	Rev
	PCH 4/7 (GPIO/MISC)	1A
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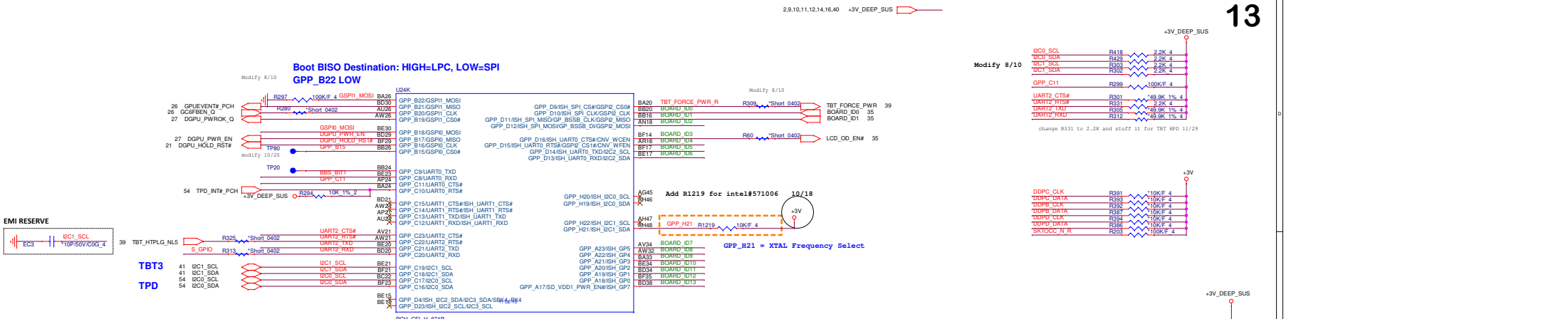
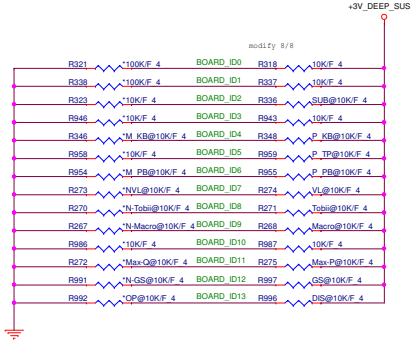
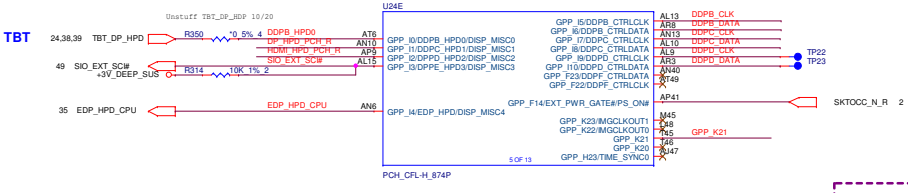
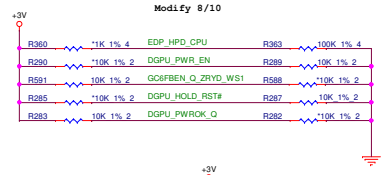
Boot BISO Destination: HIGH=LPC, LOW=SPI
GPP_B22 LOW

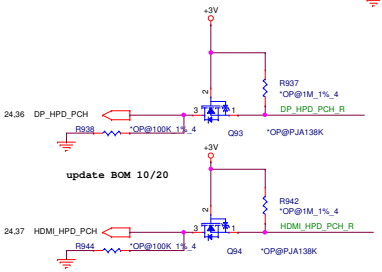


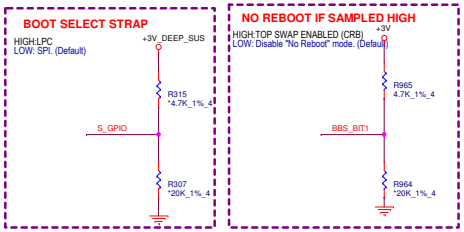
BOARD_ID0	BOARD_ID1	OD_EN	PWM pin	NSVR pin	Support panel
0	0	NC	Reserve	Reserve	Reserve
0	1	NC	NC	Y	NSVR
1	0	Y	Y	NC	DD
1	1	NC	Y	NC	Normal, DD, Freesync











ID.NO	Function	Low	High
BOARD_ID11	PCB	MAXQ	MAXP
BOARD_ID12	G-SYNC	Non-GS	GS
BOARD_ID13	VGA	Optimus	d-VGA

ID.NO	Function	Low	High
BOARD_ID8	EYE Trace	NO	YES
BOARD_ID9	Macro Key	NO	YES
BOARD_ID10	Touch Panel	YES	NO

ID.NO	Function	Low	High
BOARD_ID4	Keyboard	Metal	Plastic
BOARD_ID5	Touch PAD	Metal	Plastic
BOARD_ID6	Power Button	Metal	Plastic
BOARD_ID7	Battery Vin Boost	NO	YES

ID.NO	Function	Low	High
BOARD_ID0	LCD Panel	No Stuff	Default
BOARD_ID1	LCD Panel	No Stuff	Default
BOARD_ID2	Sub-Woofer	No	YES
BOARD_ID3	LCD OD_EN#	Enable	Default

Pin Name	Strap description	Sampled	Configuration	note
GPP_B18 (GSPI0_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (iPD 20K) 1 = Enable No Reboot Mode	+3V R288 *1K_1%_4 GSPI0_MOSI R286 100K/F_4
GPP_B22 (GSPI1_MOSI)	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = *SPI (iPD 20K) 1 = LPC	+3V R295 *1K_1%_4 GSPI1_MOSI

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PROJECT : ZGQ

Size	Document Number	Rev
	PCH 5/7 (GPIO)	1A

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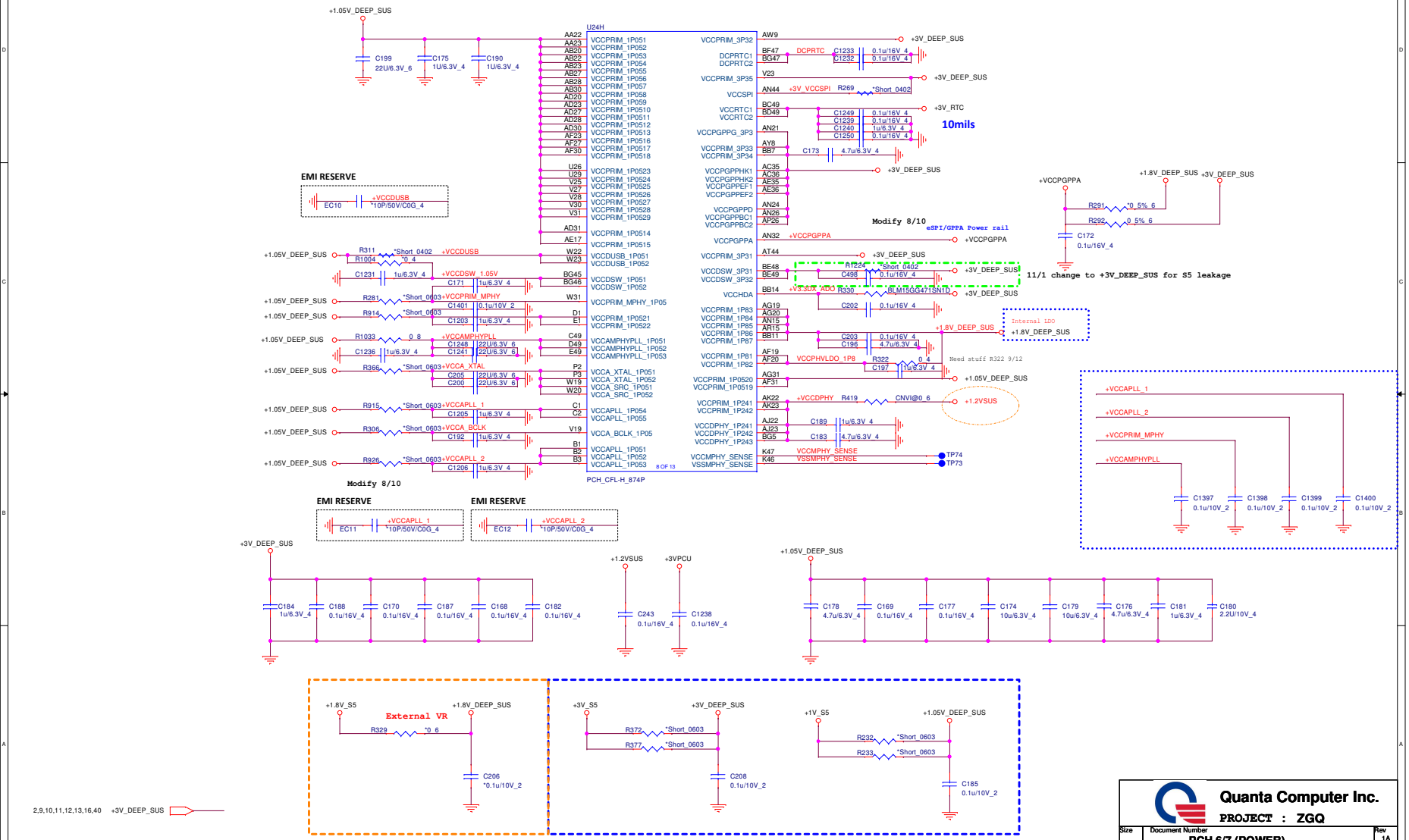
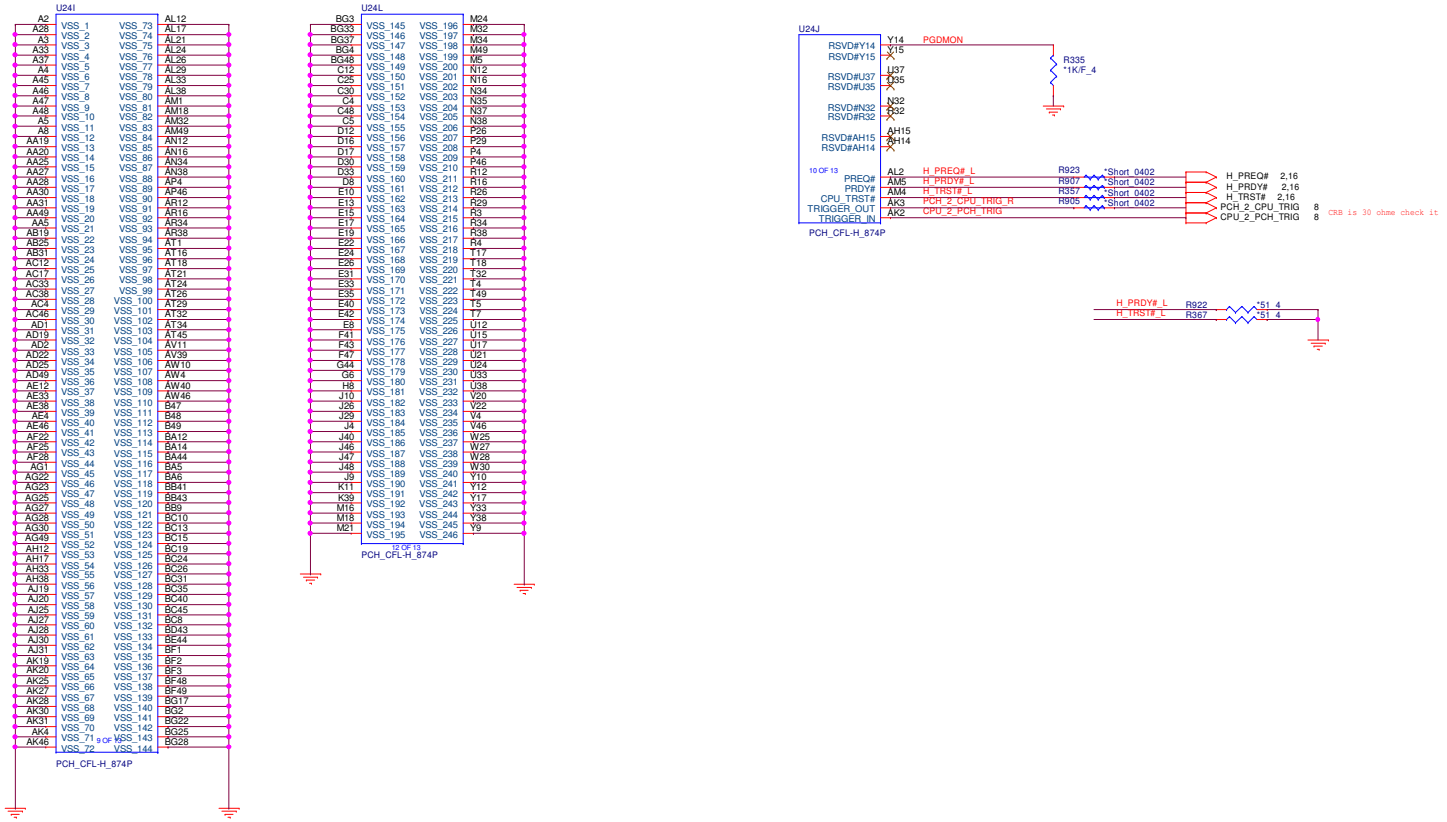
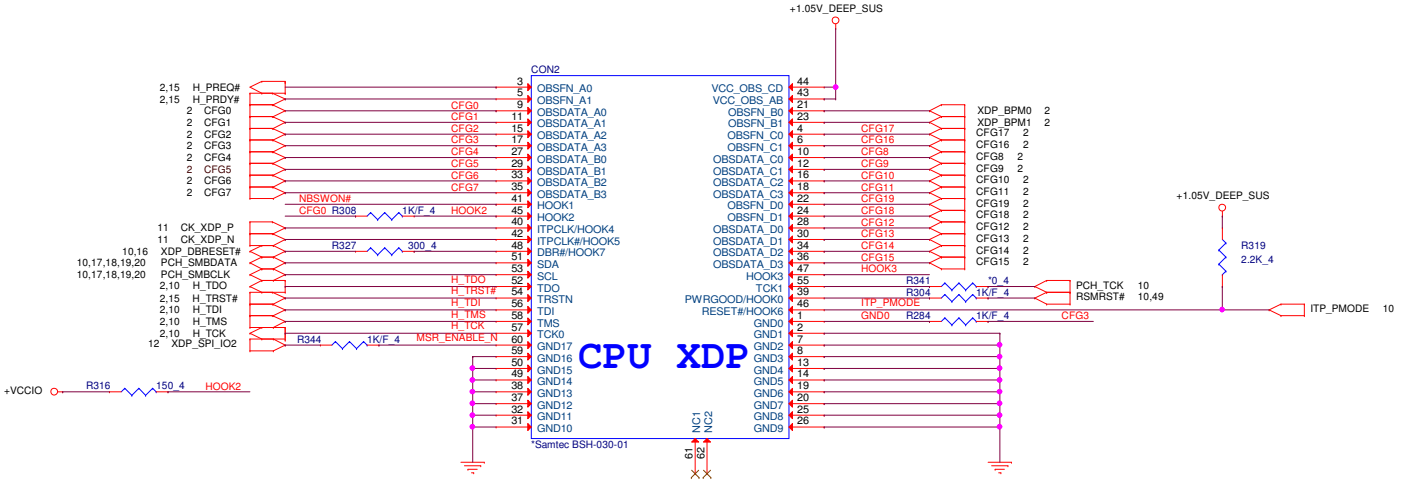
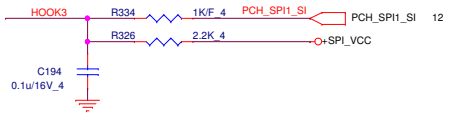


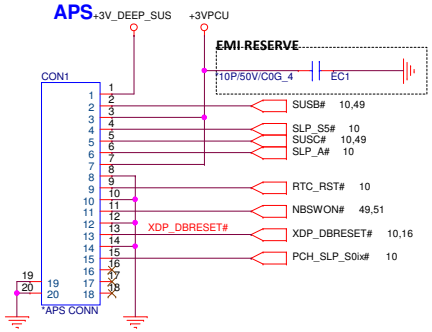
Quanta Computer Inc.		
PROJECT : ZGQ		
Size	Document Number: PCH 6/7 (POWER)	Rev: 1A
Date: Monday, March 12, 2018	Sheet 14 of 73	

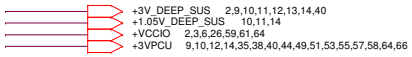


Quanta Computer Inc.		
PROJECT : ZGQ		
Size	Document Number: PCH 7/7 (GND)	Rev: 1A
Date: Monday, March 12, 2018	Sheet 15 of 73	









Quanta Computer Inc.		
PROJECT : ZGQ		
Size	Document Number: XDP & APS	Rev: 1A
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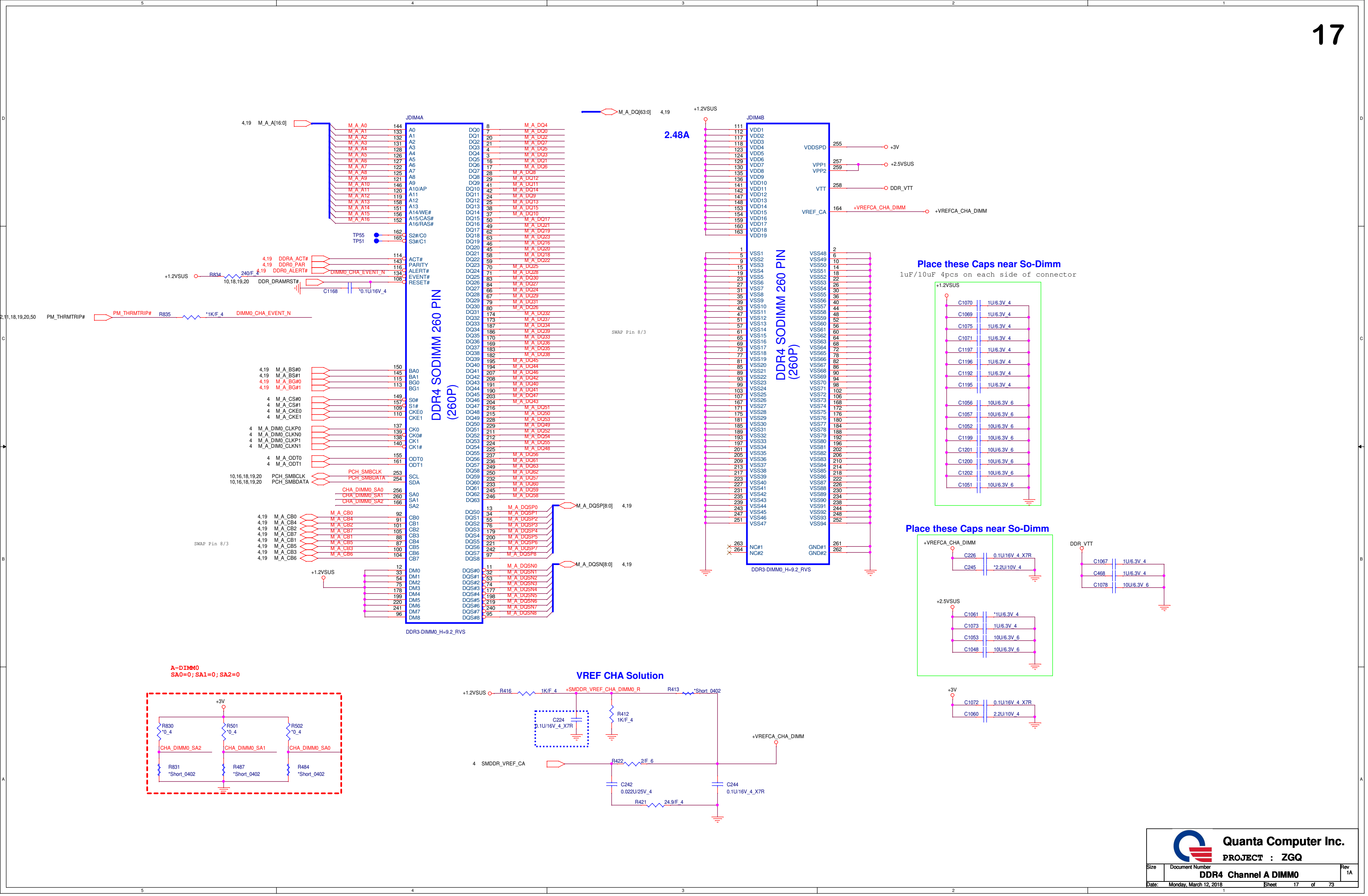
17
DDR4 SODIMM 260 PIN (260P)
JDIM4A
JDIM4B
2.48A
DDR3-DIMM0_H=9.2_RVS
Place these Caps near So-Dimm
1uF/10uF 4pcs on each side of connector
VREF CHA Solution
A-DIMM0
SA0=0;SA1=0;SA2=0
SWAP Pin 8/3
+1.2VSUS
+2.5VSUS
+3V
DDR_VTT
+VREFCA_CHA_DIMM
SMDDR_VREF_CA
PM_THRMTRIP#
DIMM0_CHA_EVENT_N
M_A_DQ[63:0]
M_A_DQSP[8:0]
M_A_DQSN[8:0]
M_A_A[16:0]
Quanta Computer Inc.
PROJECT : ZGQ
DDR4 Channel A DIMM0
Rev 1A
Date: Monday, March 12, 2018
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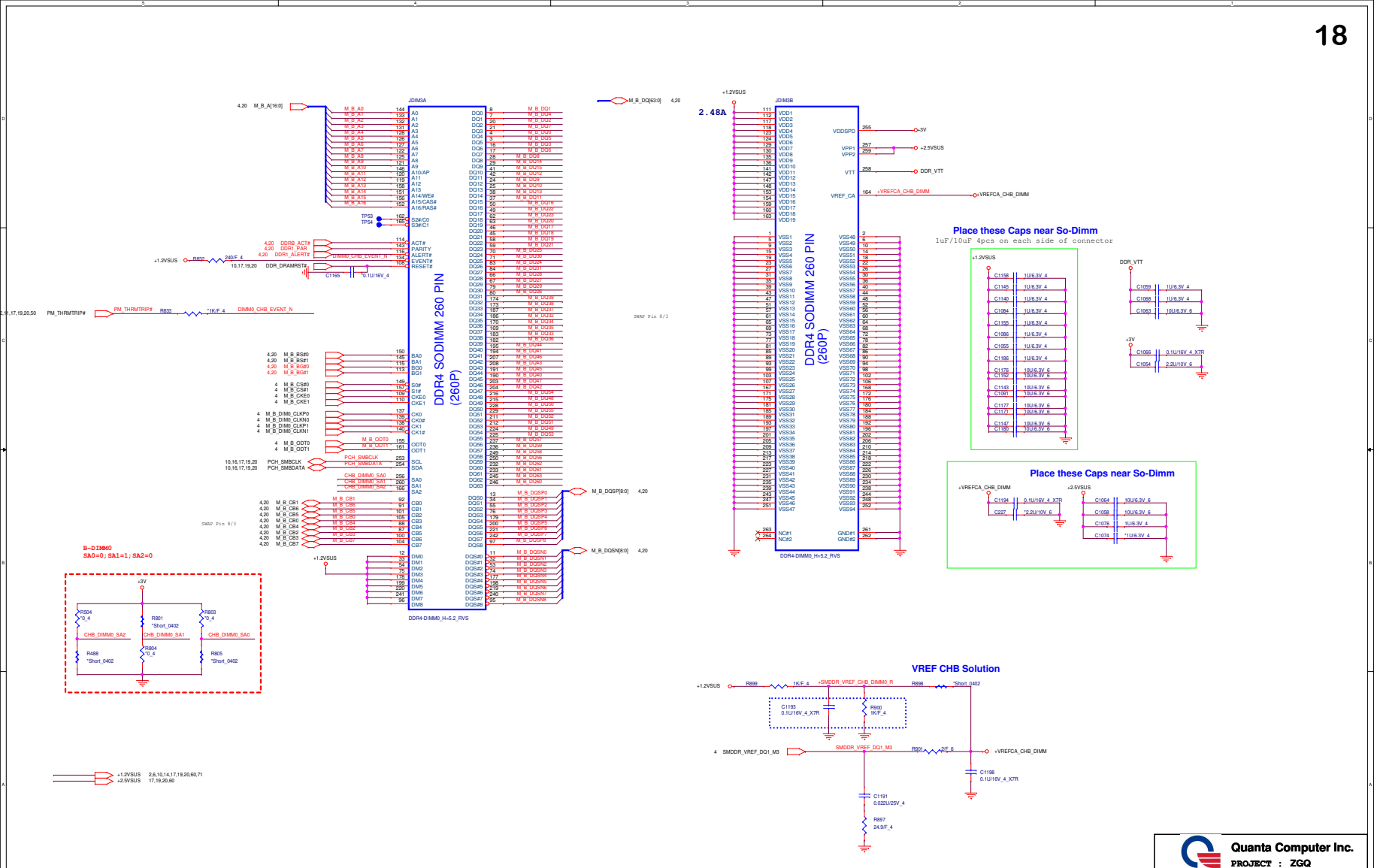
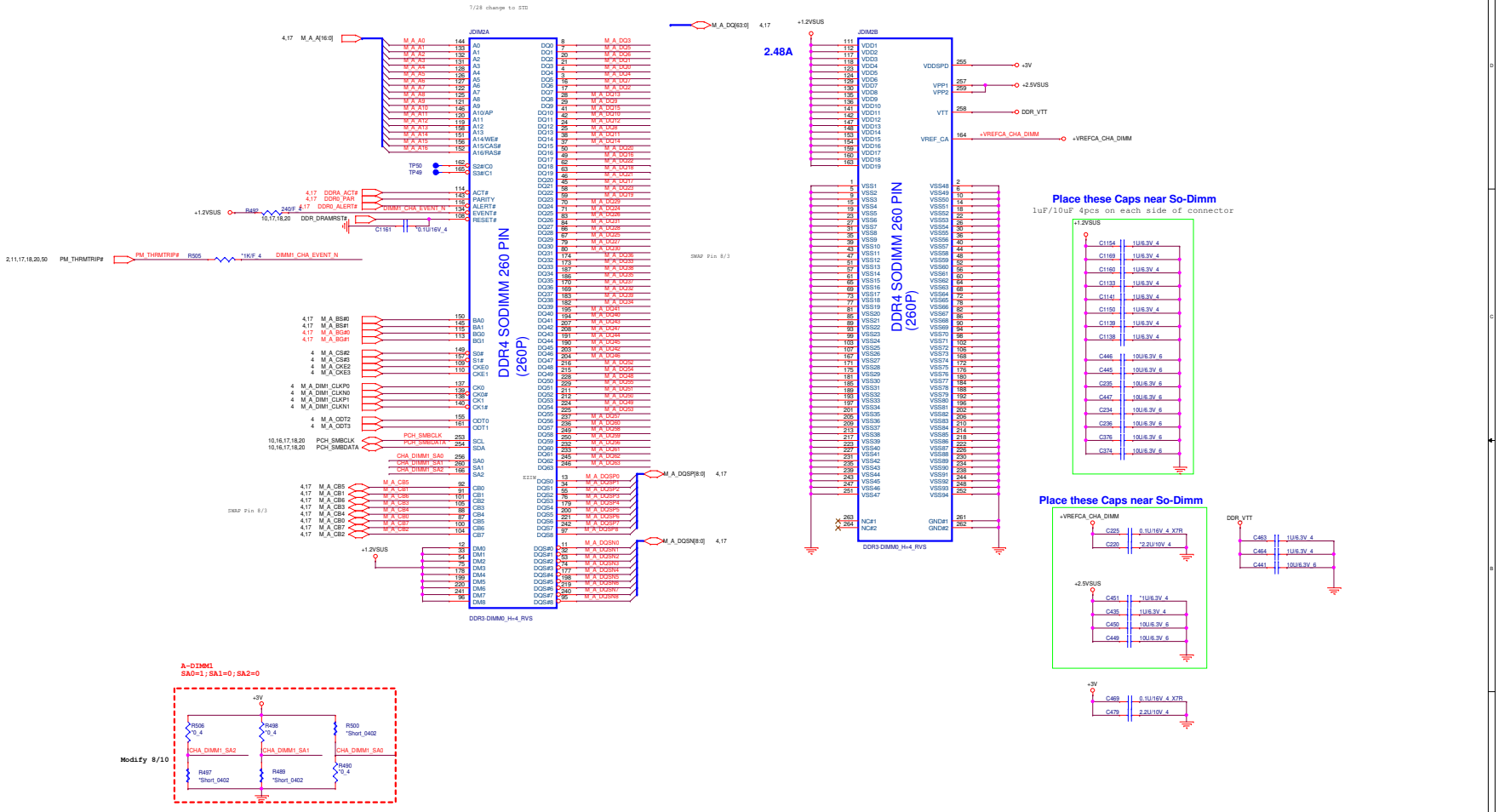

JDIM3A
DDR4 SODIMM 260 PIN
(260P)
DDR4-DIMM0_H=5.2_RVS
JDIM3B
DDR4 SODIMM 260 PIN
(260P)
DDR4-DIMM0_H=5.2_RVS
Place these Caps near So-Dimm
1uF/10uF 4pcs on each side of connector
Place these Caps near So-Dimm
VREF CHB Solution
B-DIMM0
SA0=0;SA1=1;SA2=0
2.48A



Quanta Computer Inc.			
PROJECT : ZGQ			
Size	Document Number		Rev
	DDR4 Channel A DIMM1		1A
Date: Monday, March 12, 2018		Sheet 19 of 73	

7/28 change RVS

JDIM1A

DDR4 SODIMM 260 PIN (260P)

DDR4-DIMM0_H=4_STD

JDIM1B

DDR4 SODIMM 260 PIN (260P)

DDR4-DIMM0_H=4_STD

2.48A

SNAP Pin 8/3

B-DIMM1
SA0=1;SA1=1;SA2=0

Modify 9/14

Place these Caps near So-Dimm
1uF/10uF 4pcs on each side of connector

Place these Caps near So-Dimm

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PROJECT : ZGQ

Size	Document Number	Rev
	DDR4 Channel B DIMM1	1A
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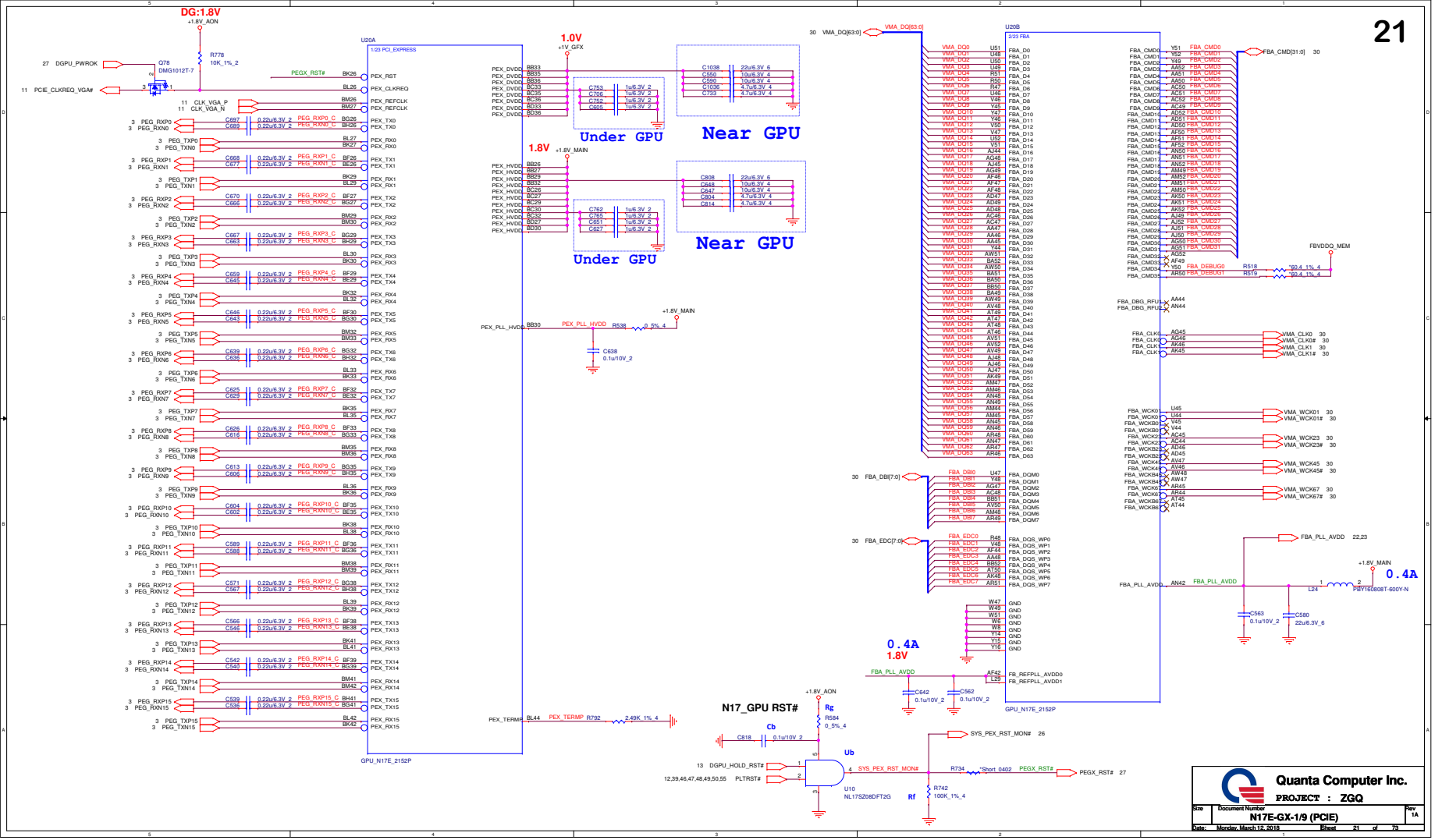
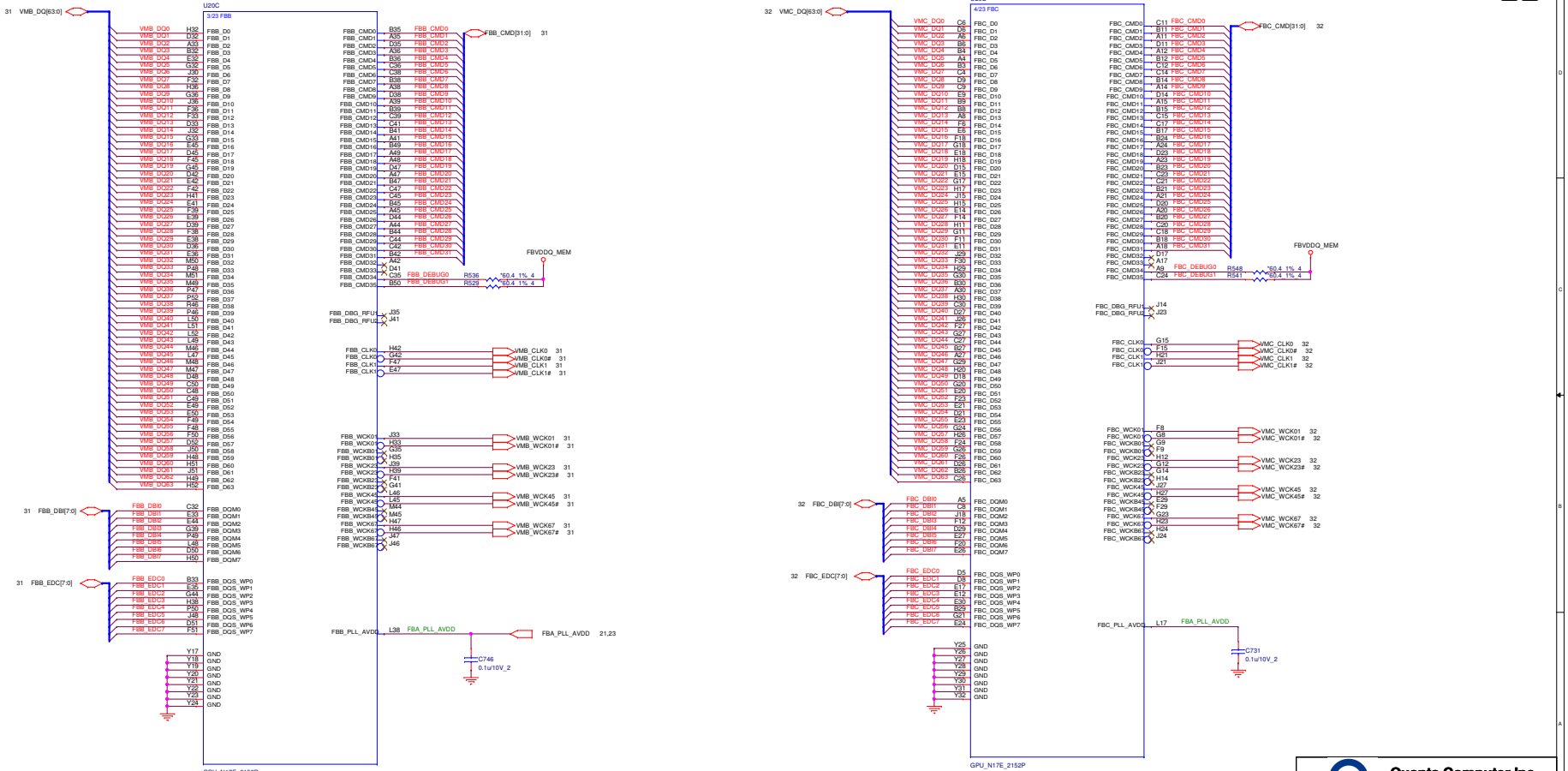


Quanta Computer Inc.

PROJECT : ZGQ

Size	Document Number	Rev
	N17E-GX-1/9 (PCIE)	1A
Date: Monday, March 12, 2018	Sheet 21 of 79	

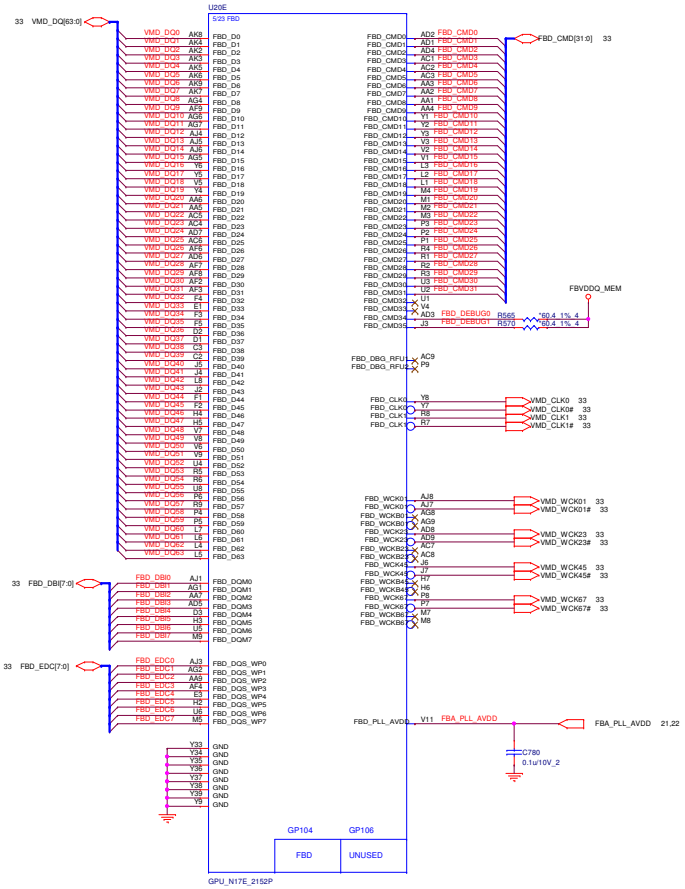


Quanta Computer Inc.

PROJECT : ZGQ

Size	Document Number	Rev
	N17E-GX-2/9 (Memory)_1	1A

Date: Monday, March 12, 2018 Sheet 22 of 73



Quanta Computer Inc.		
PROJECT : ZGQ		
Size	Document Number: N17E-GX-3/9 (Memory)_2	Rev: 1A
Date: Monday, March 12, 2018	Sheet 23 of 73	

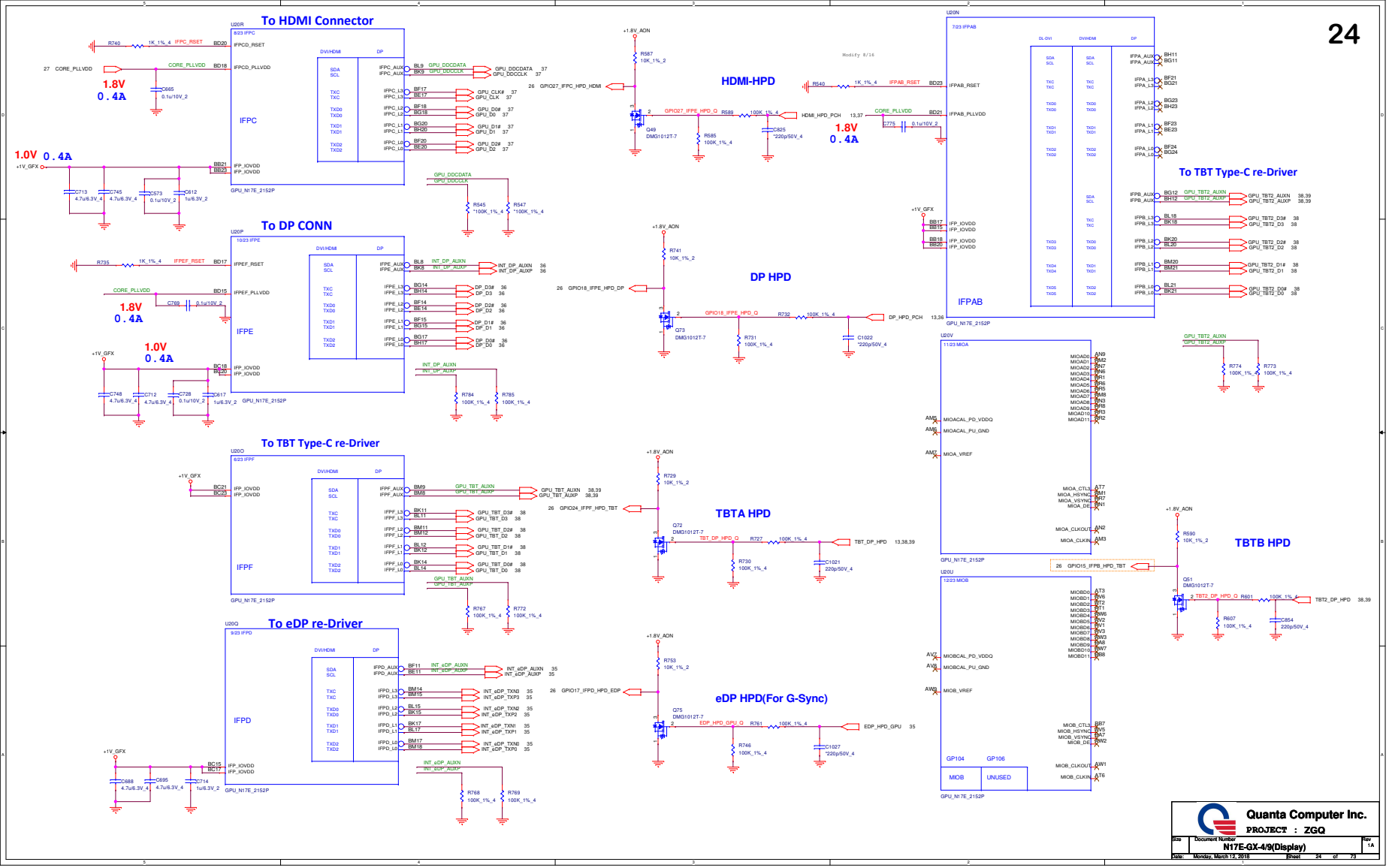

To HDMI Connector
To DP CONN
To TBT Type-C re-Driver
To eDP re-Driver
HDMI-HPD
DP HPD
TBTA HPD
eDP HPD(For G-Sync)
To TBT Type-C re-Driver
TBTB HPD
IFPC
IFPE
IFPF
IFPD
IFPAB
1.8V 0.4A
1.0V 0.4A
GPU_N17E_2152P
Q49 DMG1012T-7
Q73 DMG1012T-7
Q72 DMG1012T-7
Q75 DMG1012T-7
Q51 DMG1012T-7
MIOB
UNUSED
Quanta Computer Inc.
PROJECT : ZGQ
N17E-GX-4/9(Display)
Monday, March 12, 2018
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Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)

VRAM Table

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	Quanta P/N		
0x0	GDDR5 256Mx32 8 GHz	Samsung B die	K4G80325FB-HC25	AKG58WWT509		
0x1	GDDR5 256Mx32 8 GHz	Micron A die	MT51J256M32HF-80:A	AKG5QGUTL14		
0x2	GDDR5 256Mx32 8 GHz	Hynix M die	H5GQ8H24MJR-R4C	AKG5RF0TW06		

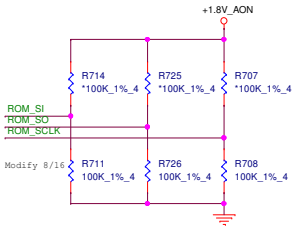
Table 4. N17E-G3 GDDR5X Recommended Memories

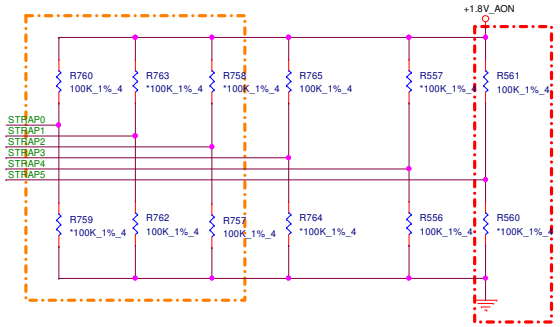
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V	Micron	MT58K256M32 -100:A	A-die	0x0	10 Gbps	N/A	Full	Production ready

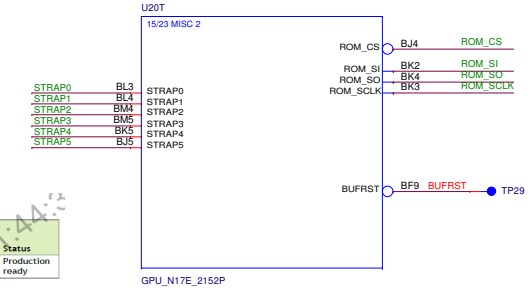
Table 1. N17E-G1/-G2 GDDR5 Recommended Memories

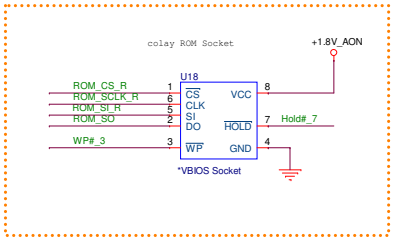
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.55V[2]	Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.5V[2]	Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V[2]	Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	Full	Post production candidate

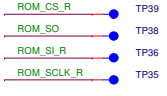
Notes:
1. For N17E-Gx, the maximum allowable memory case temperature is 95 °C, as these are our highest end flagship GPUs.
2. N17E-Gx runs WCLK up to 3000 MHz with FBVDD=1.35V. DVS is required to run WCLK > 3000 MHz.



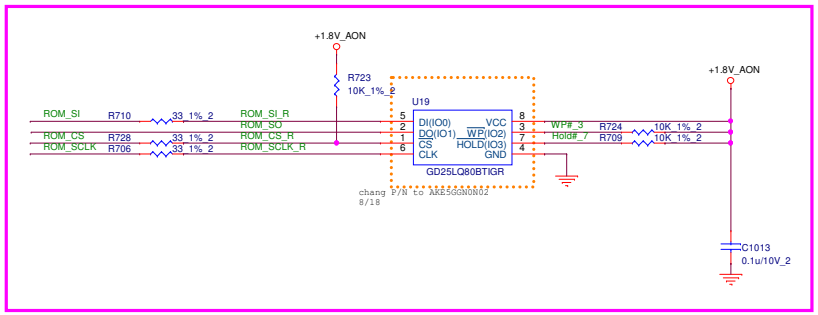








For ICT test



	STRAP5
G-SYNC	100K PU
None G-SYNC	100K PD

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	N17E-GX-5/9(Strap)	1A

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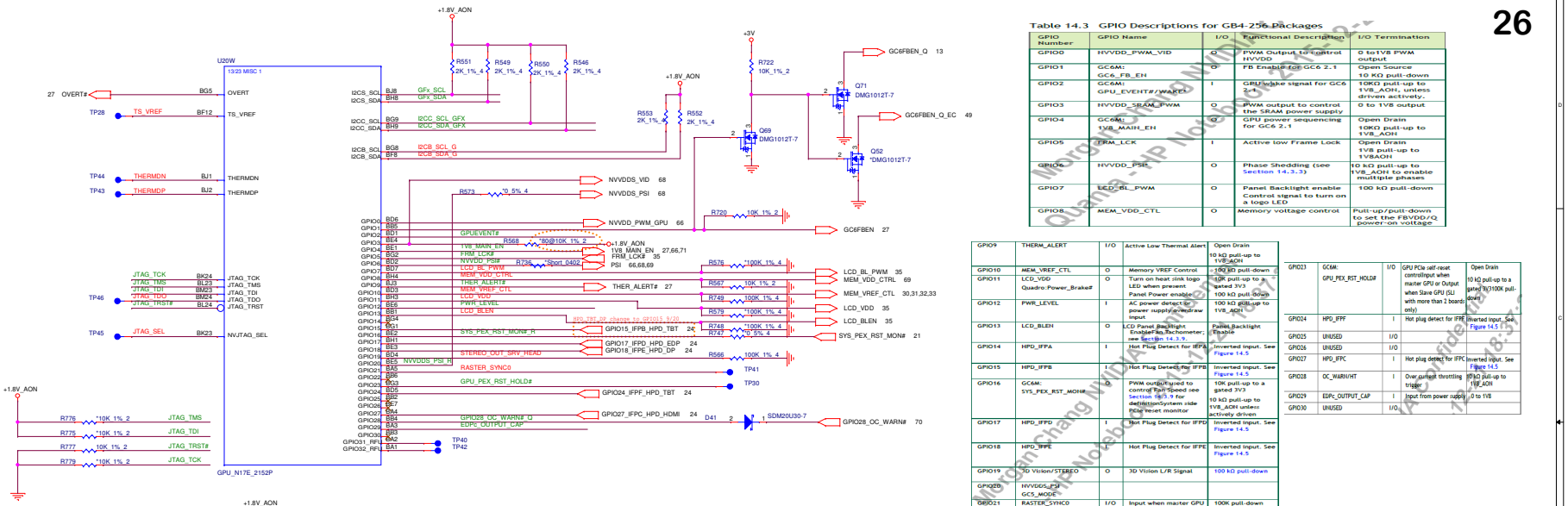


Table 14.3 GPIO Descriptions for GB4-256 Packages

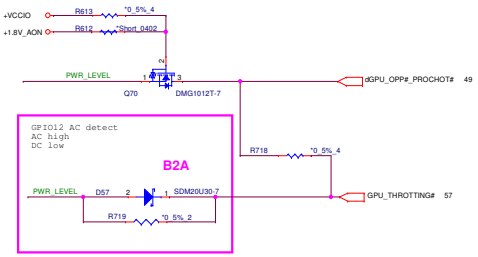
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	0 to1V8 PWM output
GPIO1	GC6M: GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source 10 KΩ pull-down
GPIO2	GC6M: GPU_EVENT#/WAKE#	I	GPU wake signal for GC6 2.1	10KΩ pull-up to 1V8_AON, unless driven actively.
GPIO3	NVVDD_SRAM_PWM	O	PWM output to control the SRAM power supply	0 to 1V8 output
GPIO4	GC6M: 1V8_MAIN_EN	O	GPU power sequencing for GC6 2.1	Open Drain 10KΩ pull-up to 1V8_AON
GPIO5	FRM_LCK	I	Active low Frame Lock	Open Drain 1V8 pull-up to 1V8AON
GPIO6	NVVDD_PSI	O	Phase Shedding (see Section 14.3.3)	10 kΩ pull-up to 1V8_AON to enable multiple phases
GPIO7	LCD_BL_PWM	O	Panel Backlight enable Control signal to turn on a logo LED	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q power-on voltage

GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LCD_VDD Quadro Power_Brake#	O	Turn on heat sink logo LED when present Panel Power enable	10K pull-up to 3 gated 3V3 100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply/redraw input	100 kΩ pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	LCD Panel Backlight Enable/Tachometer, see Section 14.3.9.	Panel Backlight Enable
GPIO14	HPD_IFPA	I	Hot Plug Detect for IFPA	Inverted input. See Figure 14.5
GPIO15	HPD_IFPB	I	Hot Plug Detect for IFPB	Inverted input. See Figure 14.5
GPIO16	GC6M: SYS_PEX_RST_MON#	O	PWM output tuned to control Fan Speed see Section 14.3.4 for definitionSystem side PCIe reset monitor	10K pull-up to a gated 3V3 10 kΩ pull-up to 1V8_AON unless actively driven
GPIO17	HPD_IFPD	I	Hot Plug Detect for IFPD	Inverted input. See Figure 14.5
GPIO18	HPD_IFPE	I	Hot Plug Detect for IFPE	Inverted input. See Figure 14.5
GPIO19	3D Vision/STEREO	O	3D Vision L/R Signal	100 kΩ pull-down
GPIO20	NVVDDS_PSI GC5_MODE			
GPIO21	RASTER_SYNC0	I/O	Input when master GPU or Output when Slave GPU	100K pull-down
GPIO22	SWAP_RDY0 or SWAPRDY_IN	I/O	SLI SWAP READY OUT	

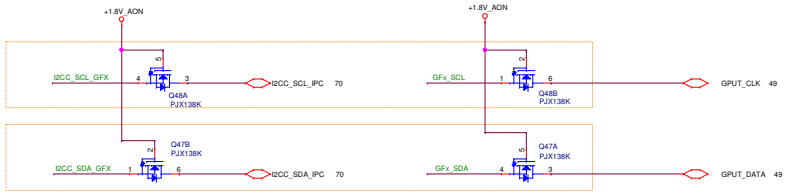
GPIO23	GC6M: GPU_PEX_RST_HOLD#	I/O	GPU PCIe self-reset control/input when master GPU or Output when Slave GPU (SLI with more than 2 boards only)	Open Drain 10 kΩ pull-up to a gated 3V3100K pull-down
GPIO24	HPD_IFPF	I	Hot plug detect for IFPF	Inverted input. See Figure 14.5
GPIO25	UNUSED	I/O		
GPIO26	UNUSED	I/O		
GPIO27	HPD_IFPC	I	Hot plug detect for IFPC	Inverted input. See Figure 14.5
GPIO28	OC_WARN/HT	I	Over current throttling trigger	10 kΩ pull-up to 1V8_AON
GPIO29	EDPc_OUTPUT_CAP	I	Input from power supply	0 to 1V8
GPIO30	UNUSED	I/O		

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AON

Throttle



Event



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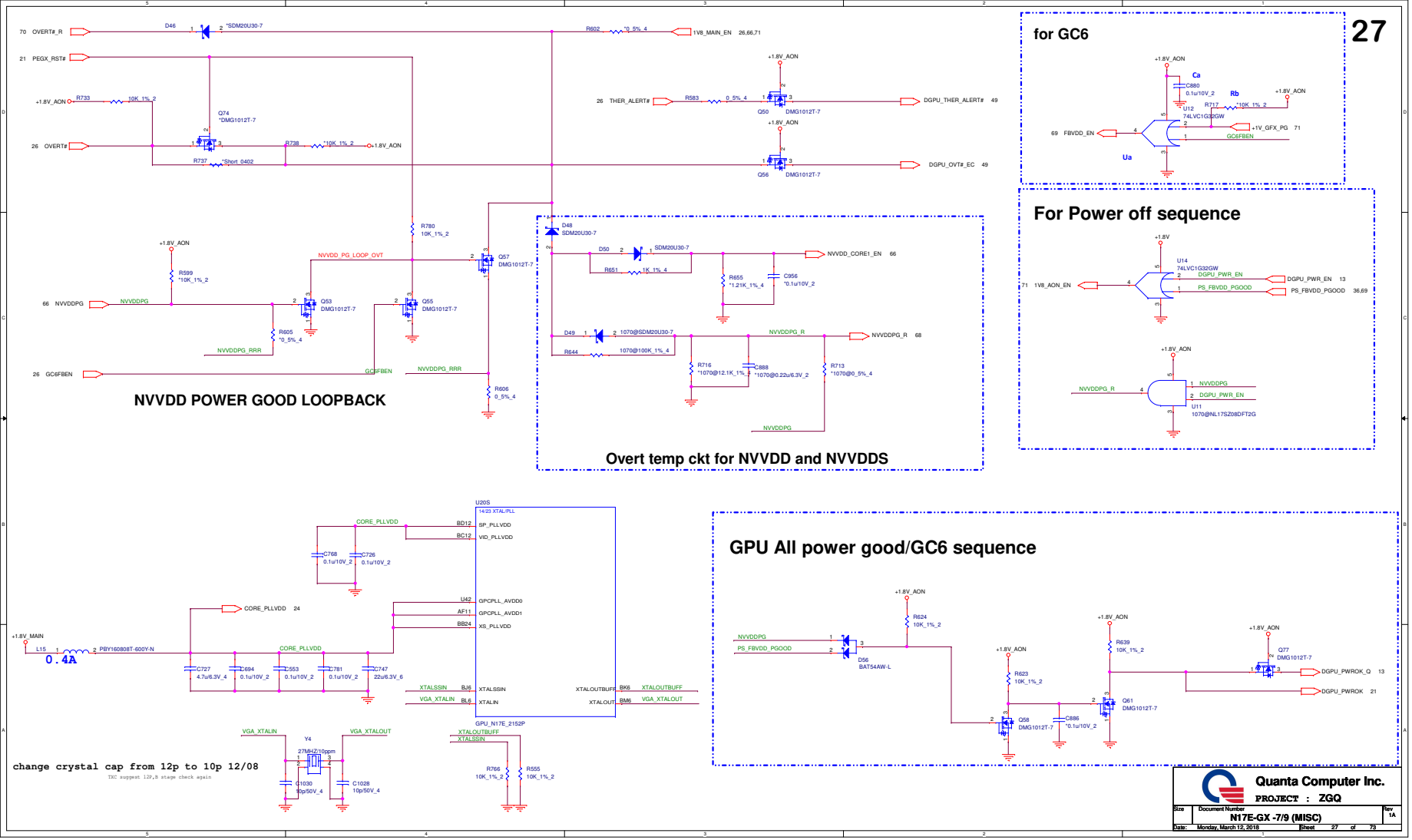
NVVDD POWER GOOD LOOPBACK
Overt temp ckt for NVVDD and NVVDDS
for GC6
For Power off sequence
GPU All power good/GC6 sequence
change crystal cap from 12p to 10p 12/08
TXC suggest 12P,B stage check again
0.4A
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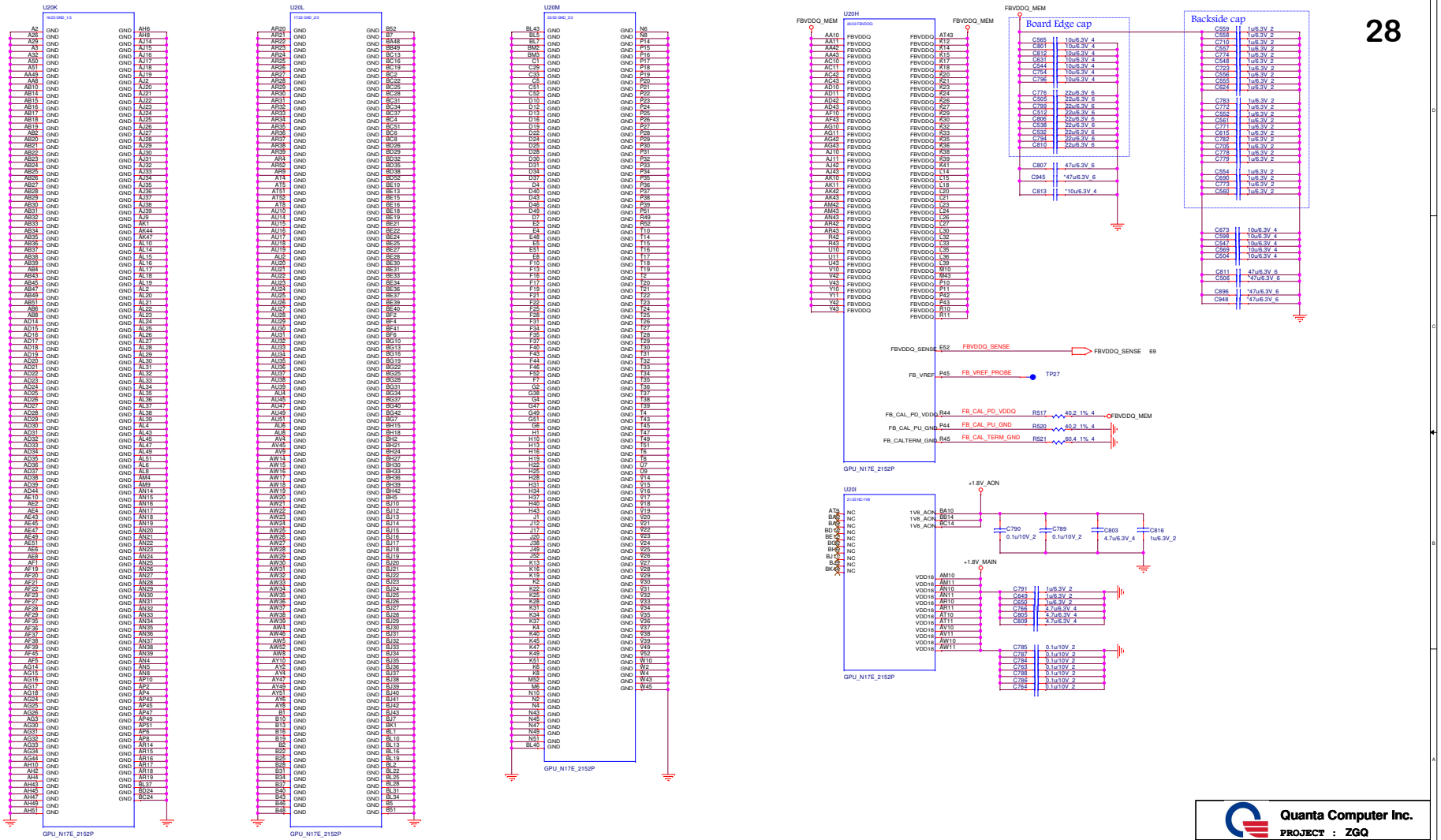

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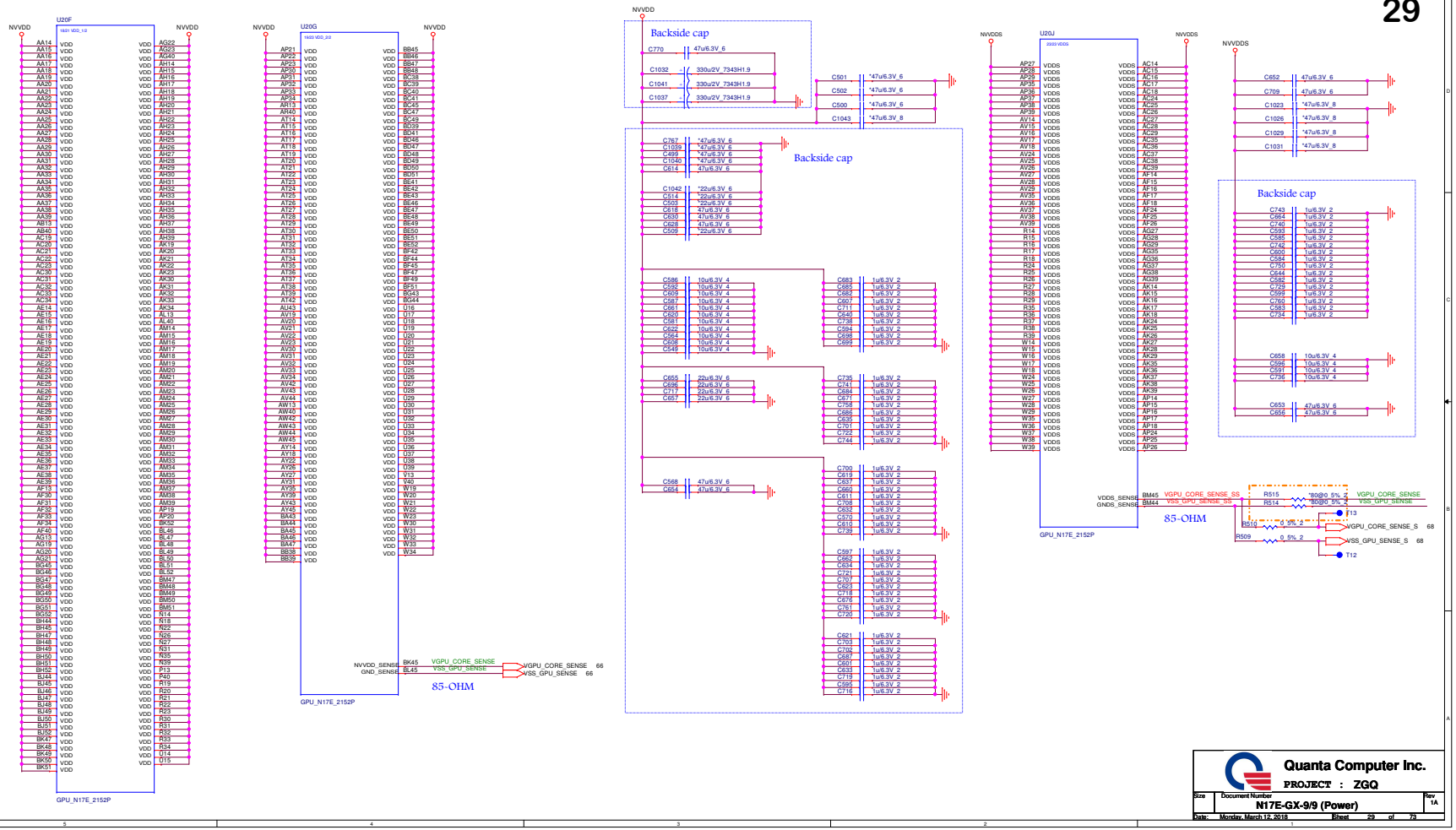

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	N17E-GX-9/9 (Power)	1A

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CHANNEL A: 2G/4G GDDR5

Channel 0 <0-31>
MF=1 mirrored

QD0~7

QD8~15

QD16~23

QD24~31

Channel 1 <32-63>
MF=0 Non-mirrored

QD56~63

QD48~55

QD40~47

QD32~39

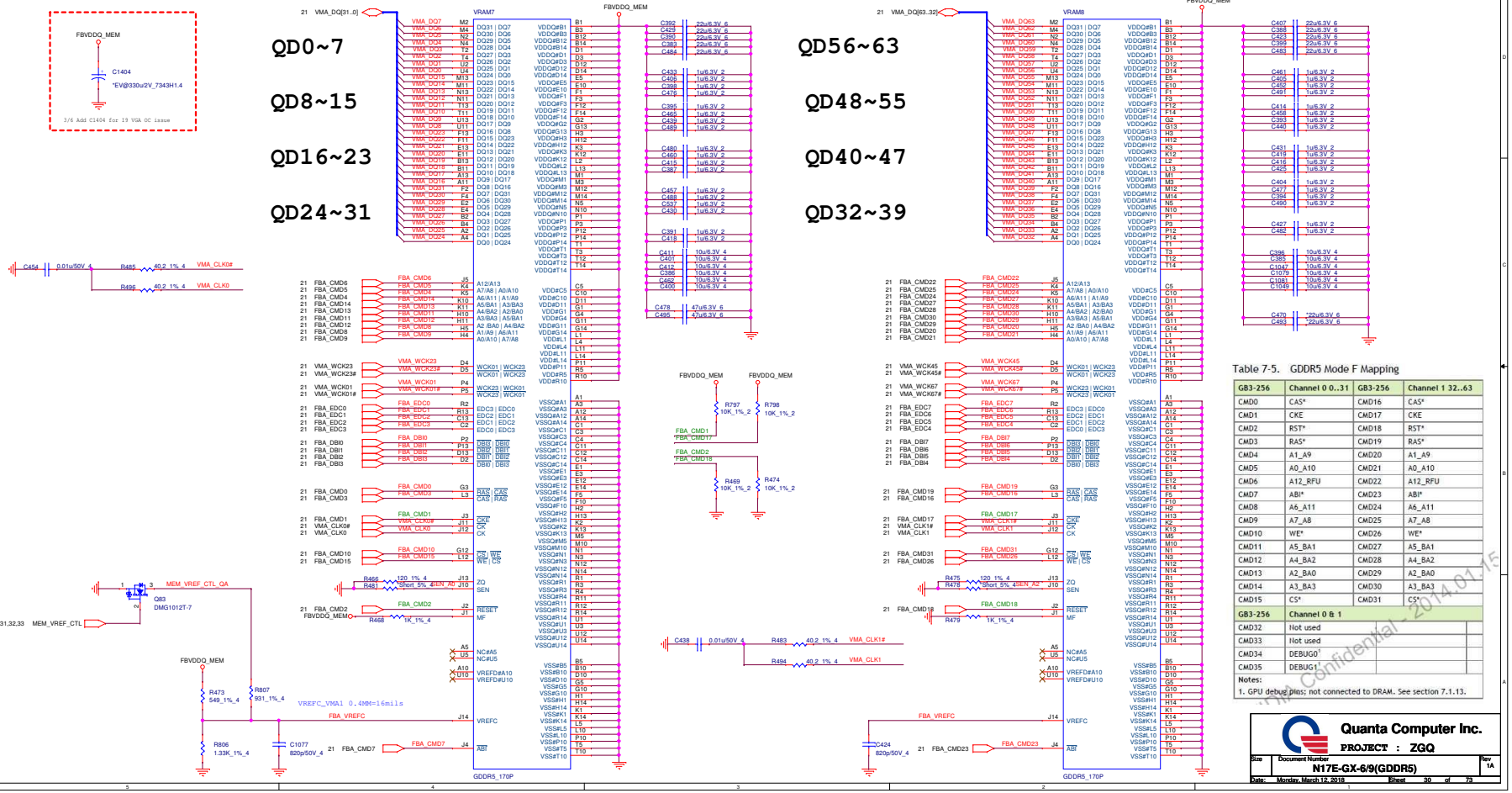

Table 7-5. GDDR5 Mode F Mapping

GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
CMD0	CAS*	CMD16	CAS*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RAS*	CMD19	RAS*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	ABI*	CMD23	ABI*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
GB3-256	Channel 0 & 1		
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG0		
CMD35	DEBUG1		

Notes:
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

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CHANNEL B: 2G/4G GDDR5

Channel 0 <0-31>
MF=1 mirrored

Channel 1 <0-31>
MF=0 Non-mirrored

QD0~7

QD8~15

QD16~23

QD24~31

QD56~63

QD48~55

QD40~47

QD32~39

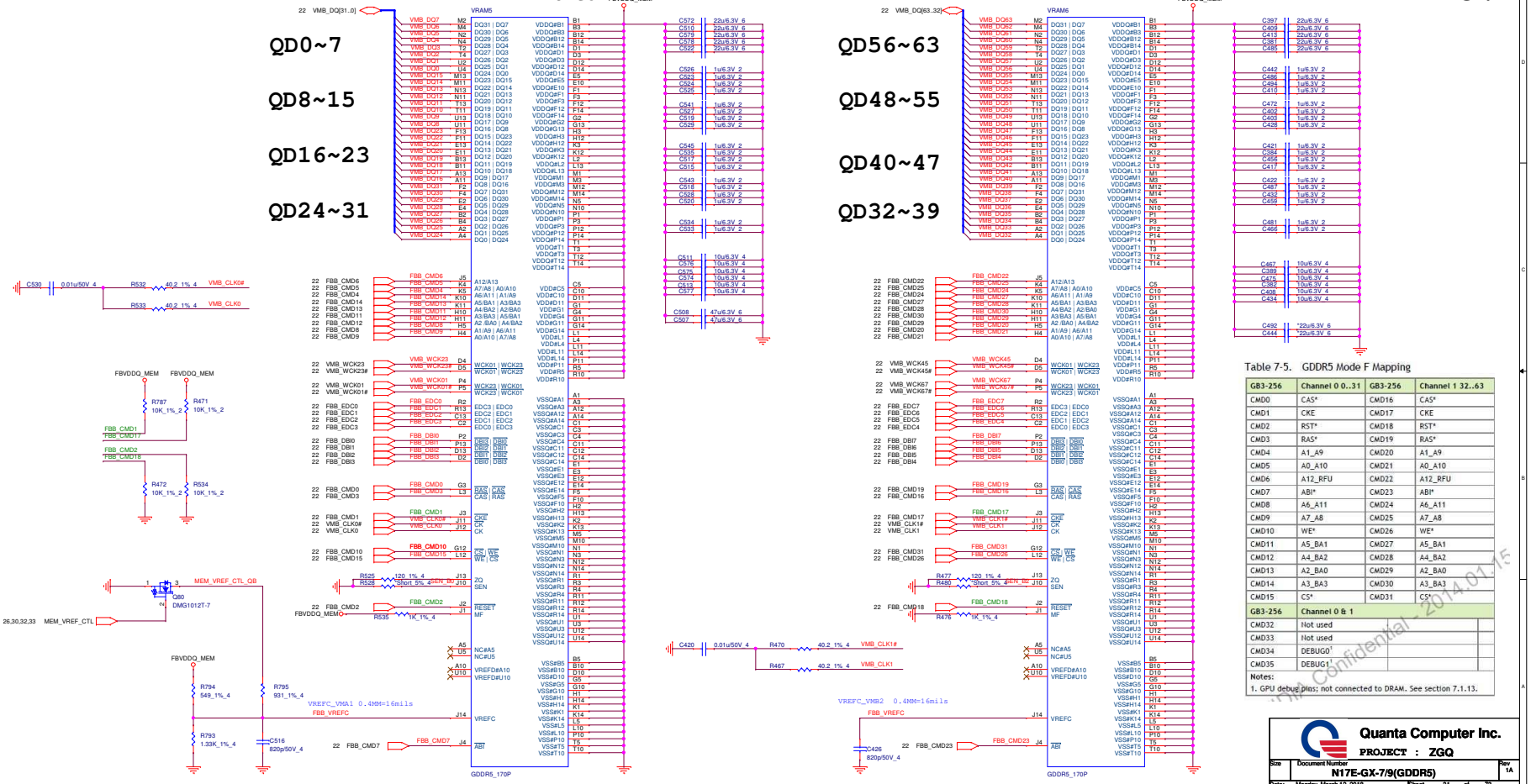

Table 7-5. GDDR5 Mode F Mapping

GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
CMD0	CAS*	CMD16	CAS*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RAS*	CMD19	RAS*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	ABI*	CMD23	ABI*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
GB3-256	Channel 0 & 1		
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG0[1]		
CMD35	DEBUG1[1]		

Notes:
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

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CHANNEL C: 2G/4G GDDR5

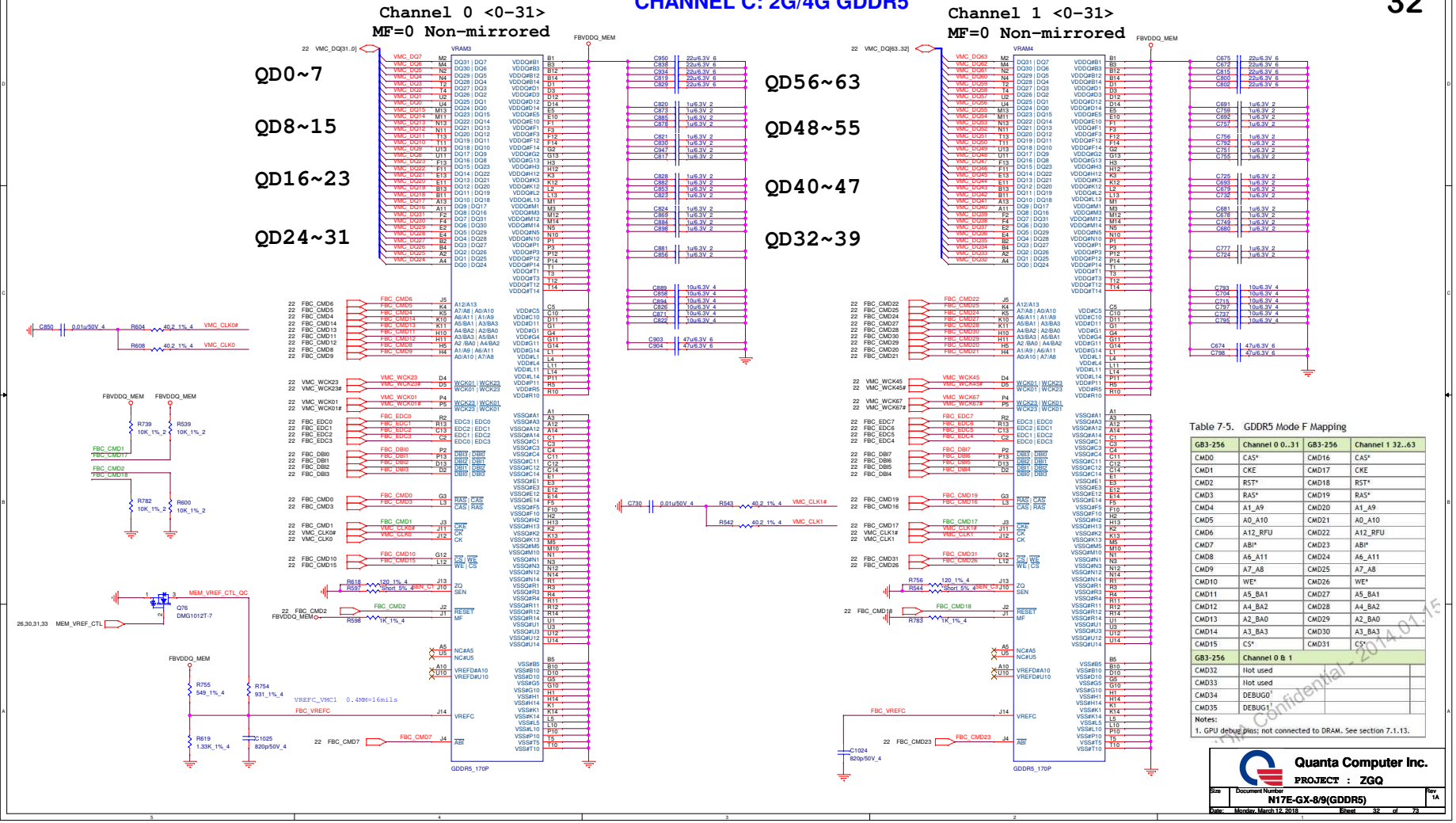

Table 7-5. GDDR5 Mode F Mapping

GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
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CMD2	RST*	CMD18	RST*
CMD3	RAS*	CMD19	RAS*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	ABI*	CMD23	ABI*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
GB3-256	Channel 0 & 1		
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG0[1]		
CMD35	DEBUG1[1]		

Notes:
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

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CHANNEL D: 2G/4G GDDR5

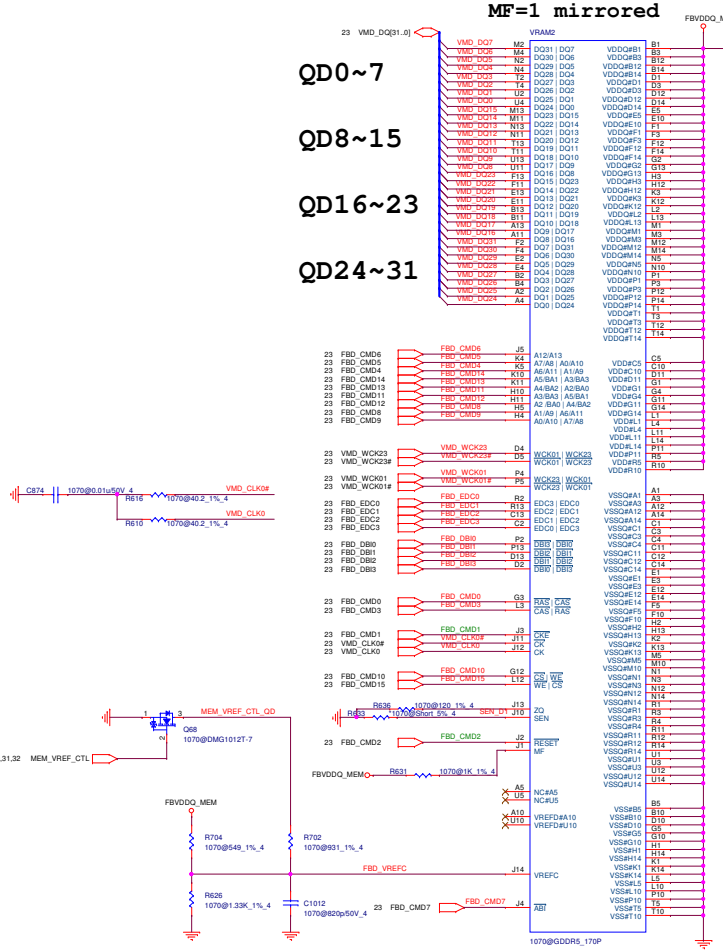
Channel 0 <0-31>
MF=1 mirrored

QD0~7

QD8~15

QD16~23

QD24~31

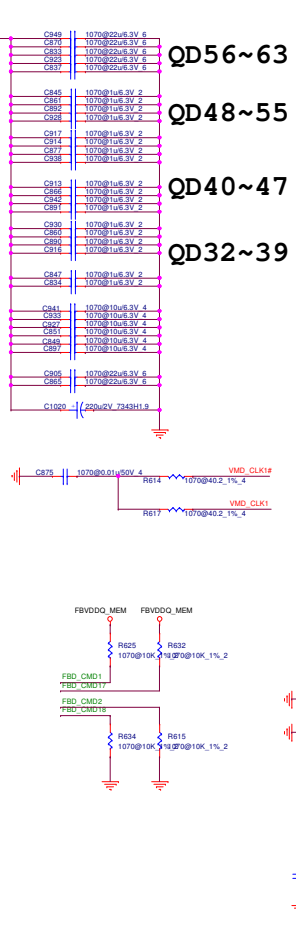


QD56~63

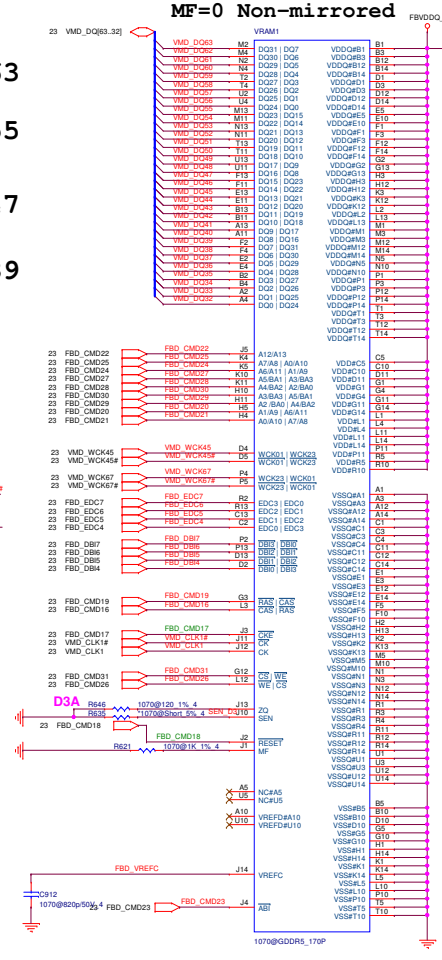
QD48~55

QD40~47

QD32~39



Channel 1 <0-31>
MF=0 Non-mirrored



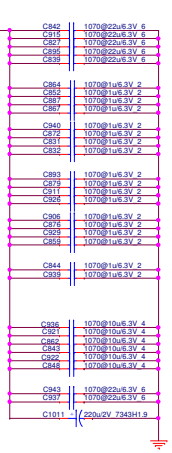


Table 7-5. GDDR5 Mode F Mapping

GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
CMD0	CA*	CMD16	CA*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RAS*	CMD19	RAS*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	ABI*	CMD23	ABI*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
GB3-256	Channel 0 & 1		
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG0[1]		
CMD35	DEBUG1[1]		

Notes:
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

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EDP Discrete

LCD CONNECTOR

LCD Power

Backlight

LCD OD EN

eDP Redriver

BOARD_ID0	BOARD_ID1	OD_EN	PWM pin	NSVR pin	Support panel
0	0	NC	Reserve	Reserve	Reserve
0	1	NC	NC	Y	NSVR
1	0	Y	Y	NC	DD
1	1	NC	Y	NC	Normal, DD, Freesync

Function	Enable	Disable
LCD OD_EN_R	Hi or Open	Default

I2C Programming or pin strap programming select.
I2C is only disable when this pin is '0'
0 : Pin Strap(I2C disable)(Default)
R : T1 test mode(I2C enable at 3.3V)
F : I2C enabled at 1.8V
1 : I2C enabled at 3.3V

SSEQ0,SSEQ1 : DSB receiver equalizer gain for upstream facing SSTXP/N
F,F(Default)
When I2C_EN is not '0' SSEQ0 sets I2C adress

DPEQ0,DPEQ1 : DP Receiver equalization gain
F,F(Default)
When I2C_EN is not '0' DPEQ0 sets I2C adress

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PROJECT : ZGQ
eDP Panel/CCD/Hall Sensor

U9 UP7553PMA5-15 — +3V, R456 *Short_0603, R457 *Short_0402, C367 0.1u/10V_2, C369 0.1u/10V_2, R458 *Short_0603, +3V_miniDP
modify 9/26
change value for safety

13,24 DP_HPD_PCH — R820 *short_0201 — DP_HPD — C1094 220p/50V_4

NVIdia

CN14 3VD11201-D7AC-7H

24 DP_D0 — C1137 0.1u/10V_2 — C_OUT_DP_TXP0
24 DP_D0# — C1136 0.1u/10V_2 — C_OUT_DP_TXN0
24 DP_D1 — C1135 0.1u/10V_2 — C_OUT_DP_TXP1
24 DP_D1# — C1134 0.1u/10V_2 — C_OUT_DP_TXN1
24 DP_D2 — C1132 0.1u/10V_2 — C_OUT_DP_TXP2
24 DP_D2# — C1131 0.1u/10V_2 — C_OUT_DP_TXN2
24 DP_D3 — C1129 0.1u/10V_2 — C_OUT_DP_TXP3
24 DP_D3# — C1127 0.1u/10V_2 — C_OUT_DP_TXN3
R819 1M_1%_4, R824 5.1M_5%_4, CAD_SNK
C_INT_DP_AUXP
C_INT_DP_AUXN
DP_HPD
+3V_miniDP — C372 10u/6.3V_4, C371 0.1u/10V_2

change Footprint 10/23
7/27 change P/N & footprint

support dual mode /0525

+3V_miniDP — R460 100K_5%_4 — C_INT_DP_AUXN — C_INT_DP_AUXP — R459 100K_5%_4

24 INT_DP_AUXN — HDMI DAT — C370 0.1u/10V_2 — C_INT_DP_AUXN
Q44A PJX8838, Q44B PJX8838
C1128 0.01u/50V_4
C1130 0.01u/50V_4
R453 10K_1%_2, R455 10K_1%_2, R454 10K_1%_2
Q39 2N7002KTB, Q40 2N7002KTB, Q41 2N7002KTB, Q42 2N7002KTB
PS_FBVDD_PGOOD 27,69
Q43A PJX8838, Q43B PJX8838
24 INT_DP_AUXP — HDMI CLK — C368 0.1u/10V_2 — C_INT_DP_AUXP

To support dual mode (DP++) over DisplayPort through Dongle for HDMI, the circuit shown below is required to be implemented on the motherboard.

ESD1 *AZ1045-04F.R7G
C_INT_DP_AUXP, C_INT_DP_AUXN, DP_HPD, CAD_SNK
Line-1, Line-2, GND#1, Line-3, Line-4, NC#4, NC#3, NC#2, NC#1

C_OUT_DP_TXP0 D70, C_OUT_DP_TXN0 D69, C_OUT_DP_TXP1 D68, C_OUT_DP_TXN1 D67, C_OUT_DP_TXP2 D66, C_OUT_DP_TXN2 D65, C_OUT_DP_TXP3 D64, C_OUT_DP_TXN3 D63
*PESD5V0H1BSF

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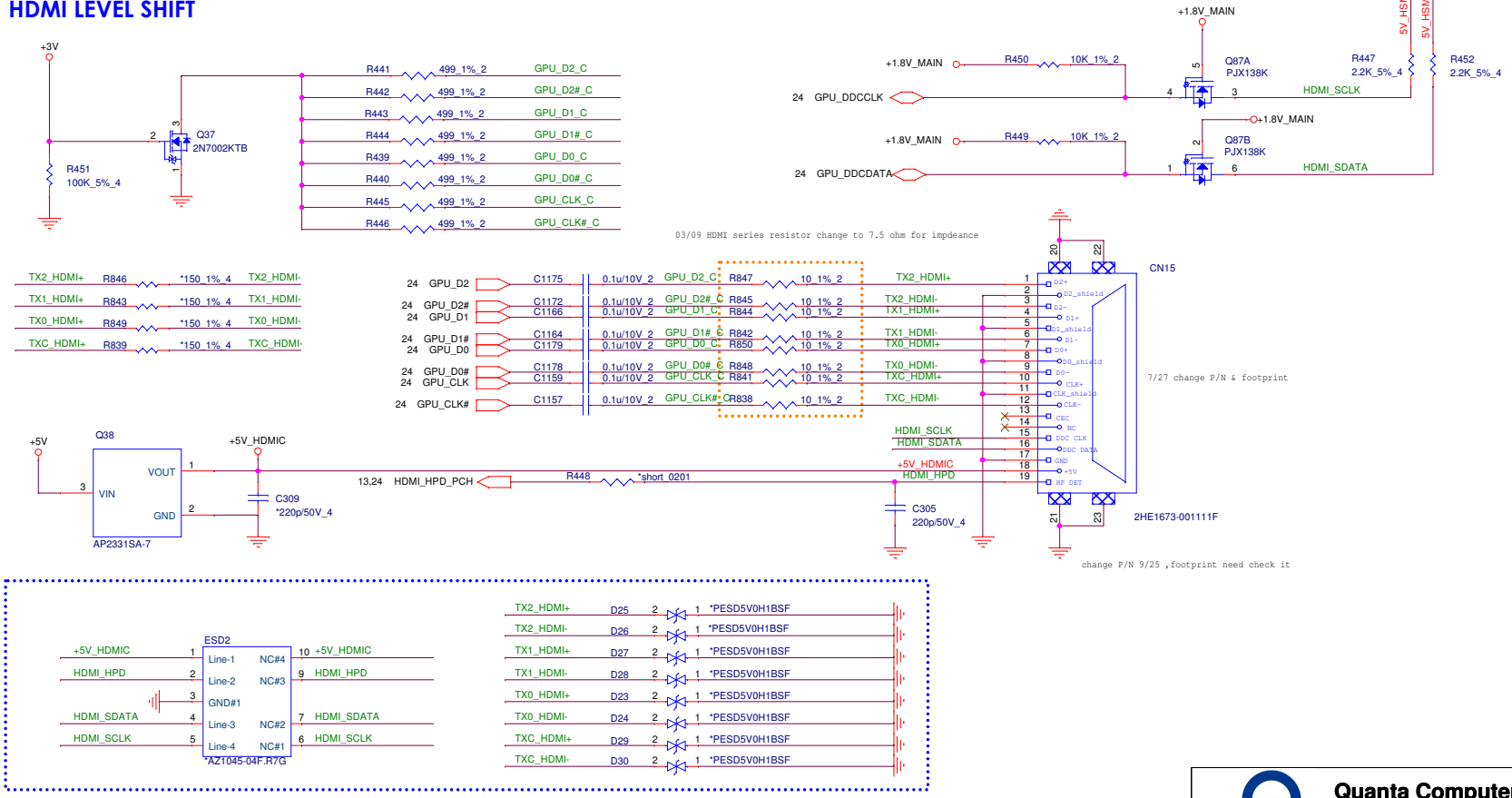
HDMI

HDMI LEVEL SHIFT



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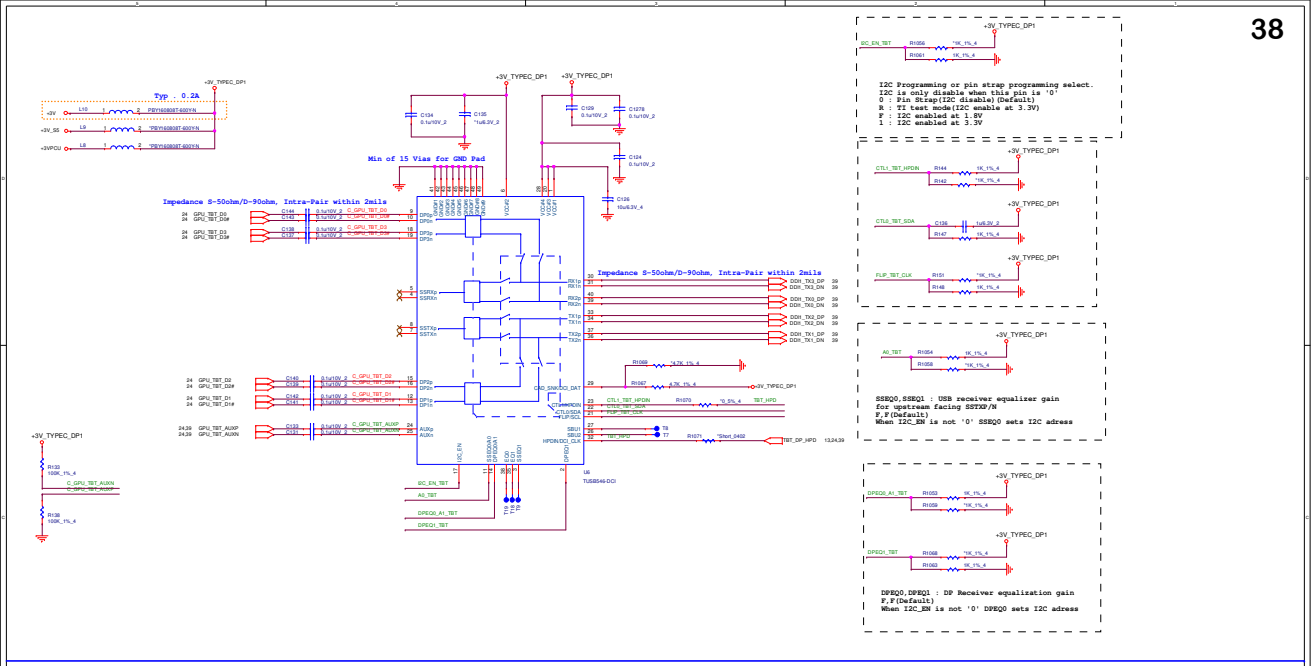

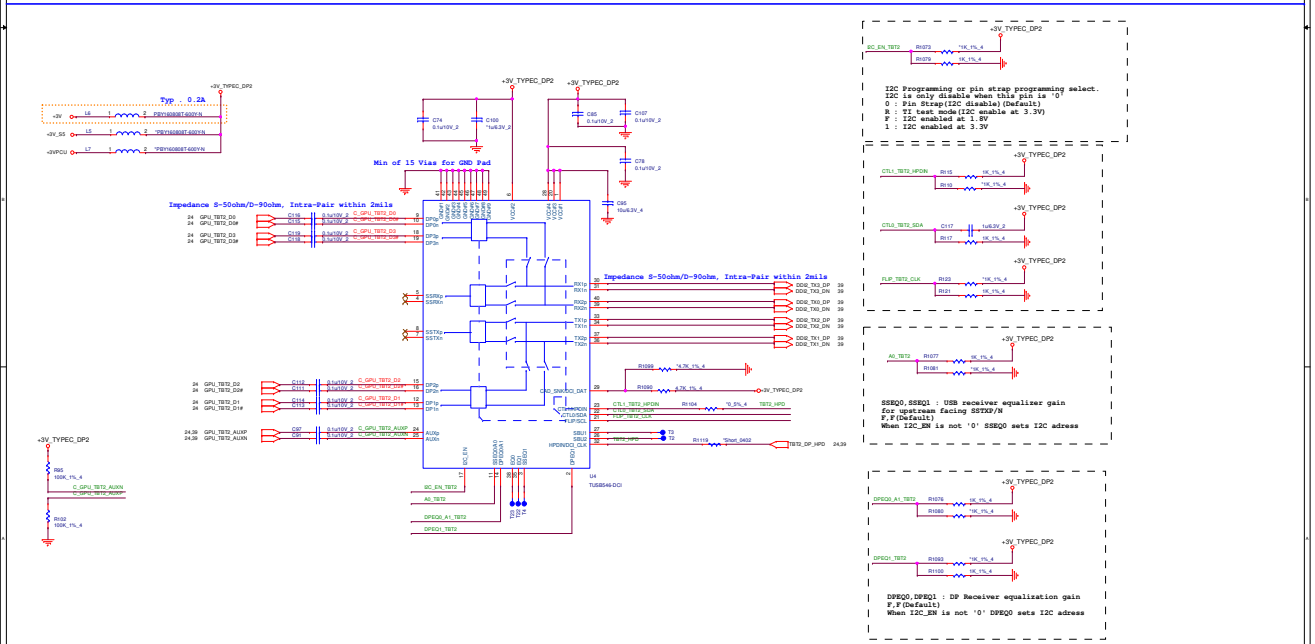

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PROJECT : ZGQ			
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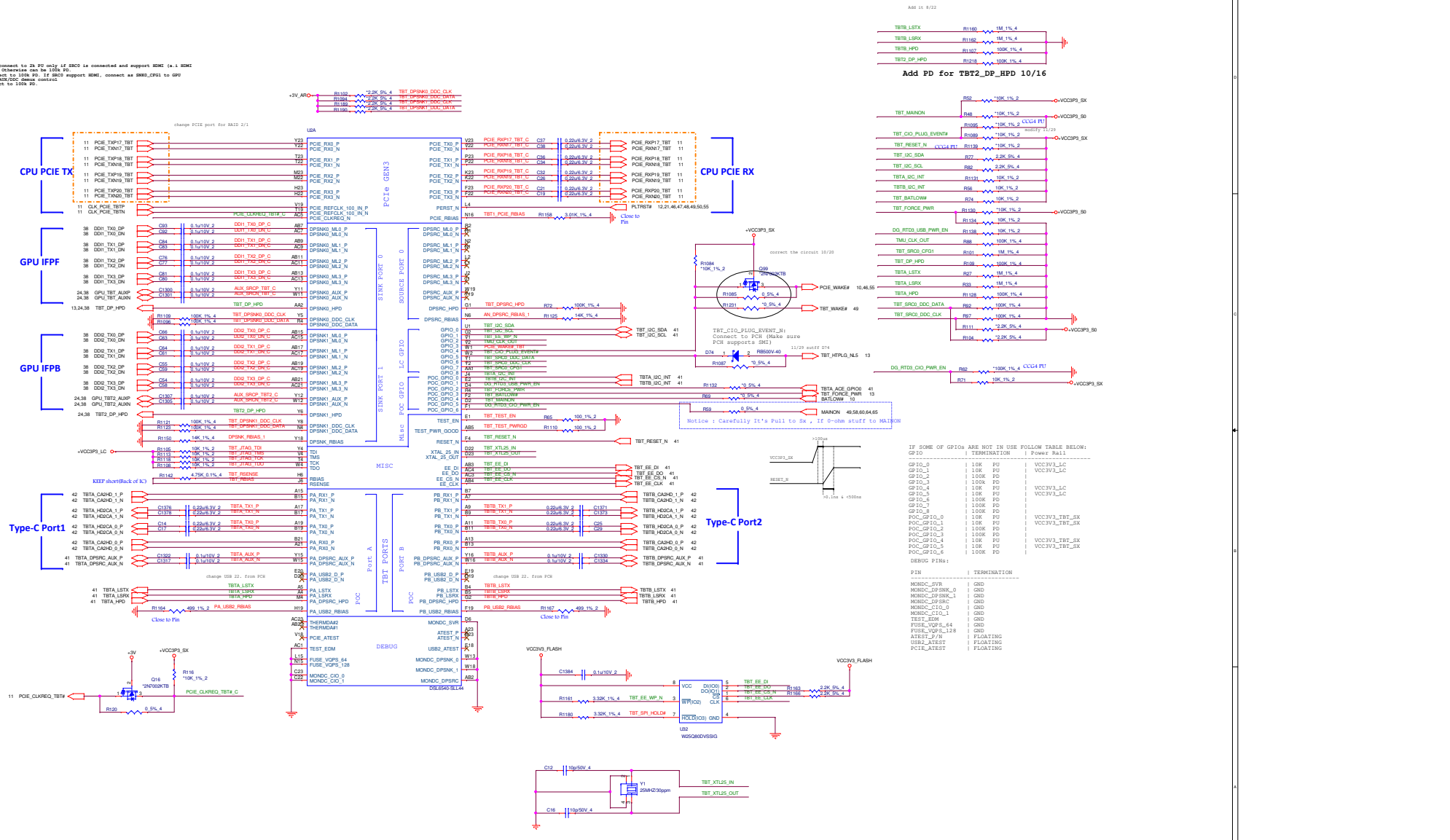

Quanta Computer Inc.

PROJECT : ZGQ

TBT(Apline Ridge)

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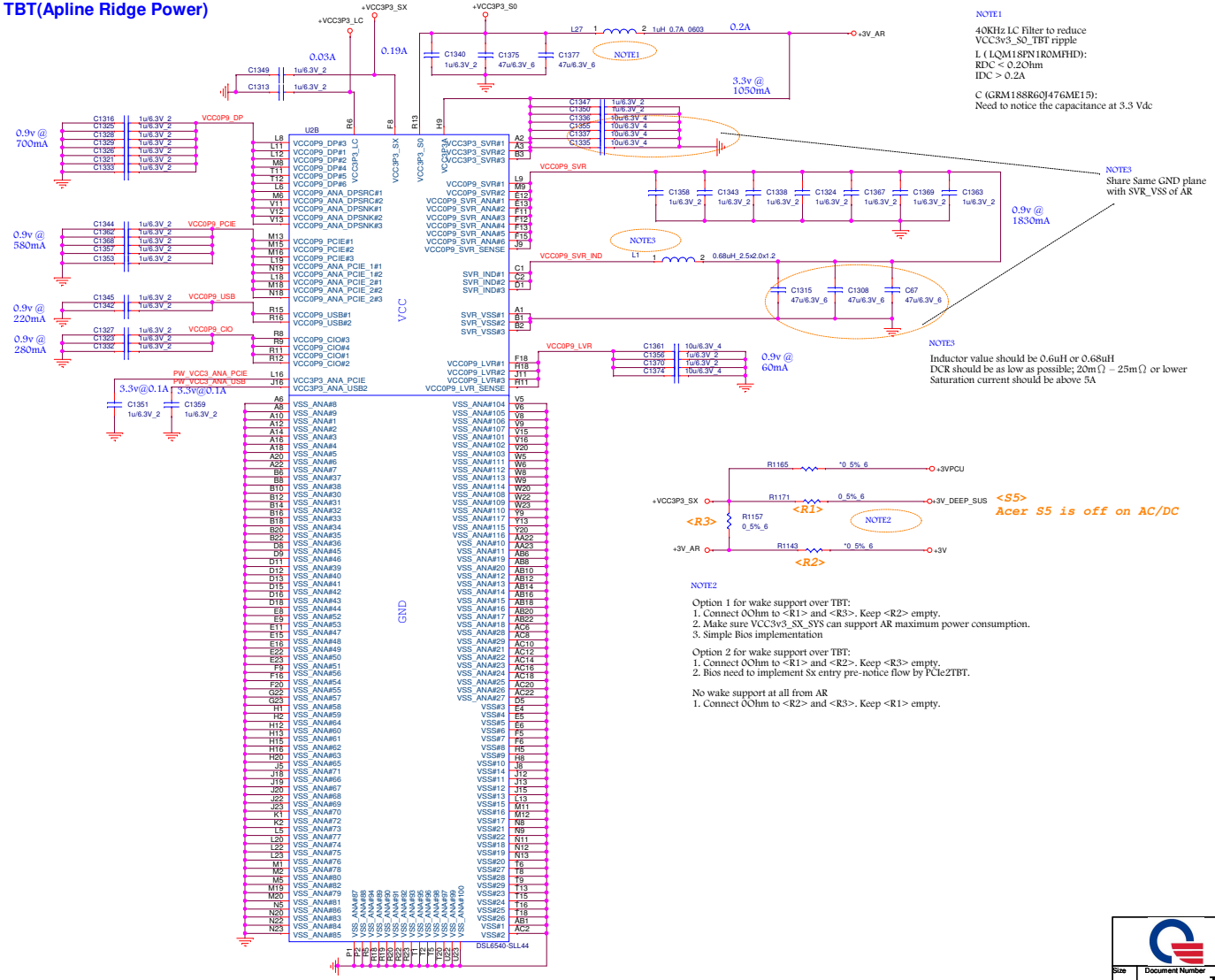
TBT(Apline Ridge Power)



NOTE1

40KHz LC Filter to reduce VCC3v3_S0_TBT ripple

L (LQM18PN1R0MFHD):
RDC < 0.2Ohm
IDC > 0.2A

C (GRM188R60J476ME15):
Need to notice the capacitance at 3.3 Vdc

NOTE3

Share Same GND plane with SVR_VSS of AR

NOTE3

Inductor value should be 0.6uH or 0.68uH
DCR should be as low as possible; 20mΩ – 25mΩ or lower
Saturation current should be above 5A

NOTE2

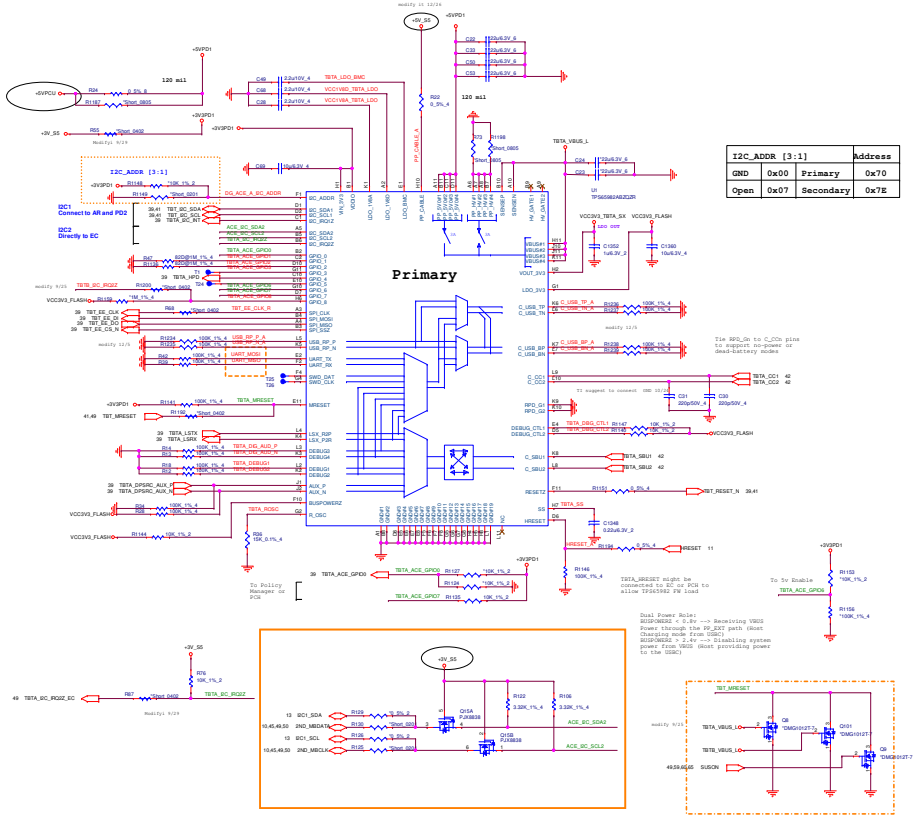
Option 1 for wake support over TBT:
1. Connect 0Ohm to <R1> and <R3>. Keep <R2> empty.
2. Make sure VCC3v3_SX_SYS can support AR maximum power consumption.
3. Simple Bios implementation

Option 2 for wake support over TBT:
1. Connect 0Ohm to <R1> and <R2>. Keep <R3> empty.
2. Bios need to implement Sx entry pre-notice flow by PCIe2TBT.

No wake support at all from AR
1. Connect 0Ohm to <R2> and <R3>. Keep <R1> empty.

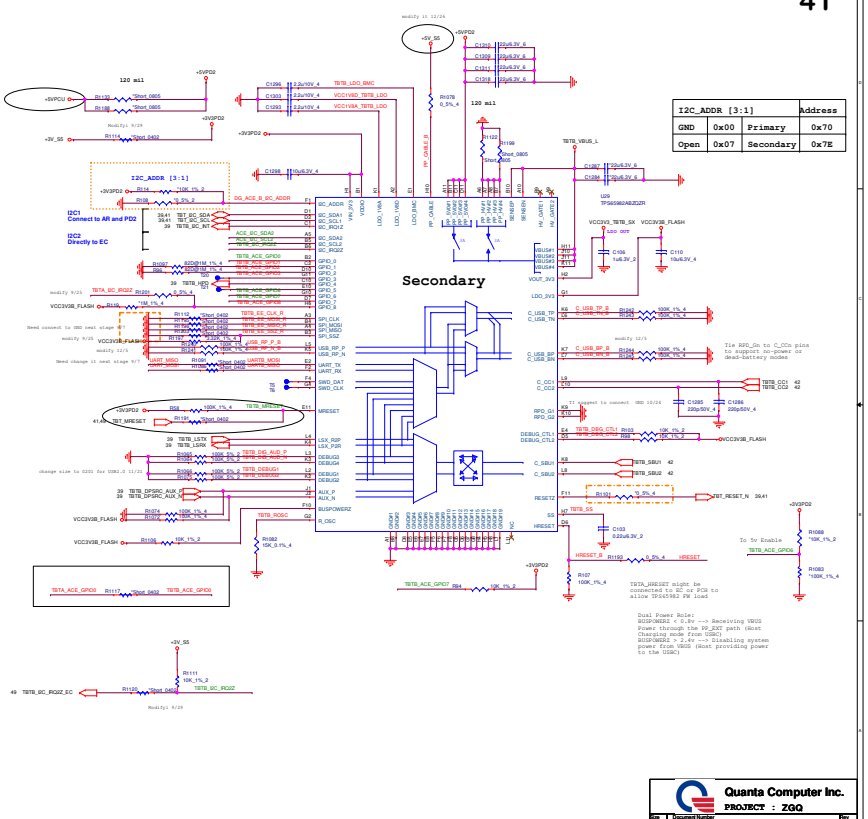
Quanta Computer Inc.			
PROJECT : ZGQ			
Size	Document Number	TBT(Apline Ridge Power)	Rev 1A
Date: Monday, March 12, 2018	Sheet 40 of 73		

Port 1 USB3.1 PD Controller -TPS65982



I2C_ADDR [3:1]		Address
GND	0x00	Primary	0x70
Open	0x07	Secondary	0x7E

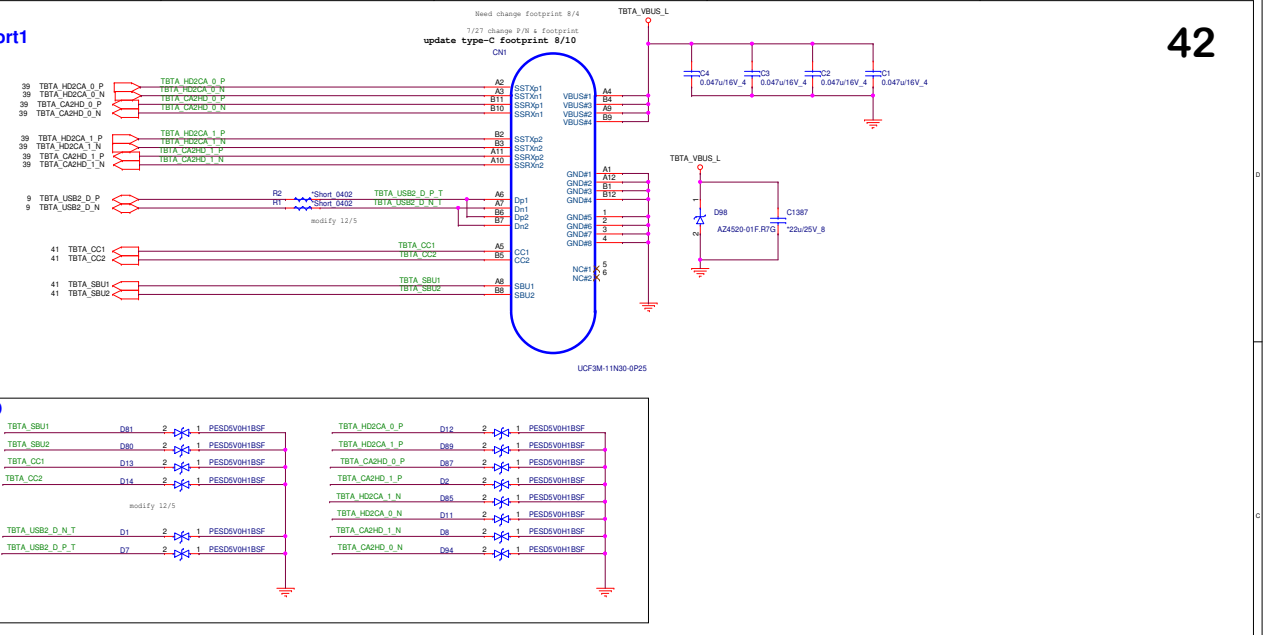
Port 2 USB3.1 PD Controller -TPS65982



I2C_ADDR [3:1]		Address
GND	0x00	Primary	0x70
Open	0x07	Secondary	0x7E

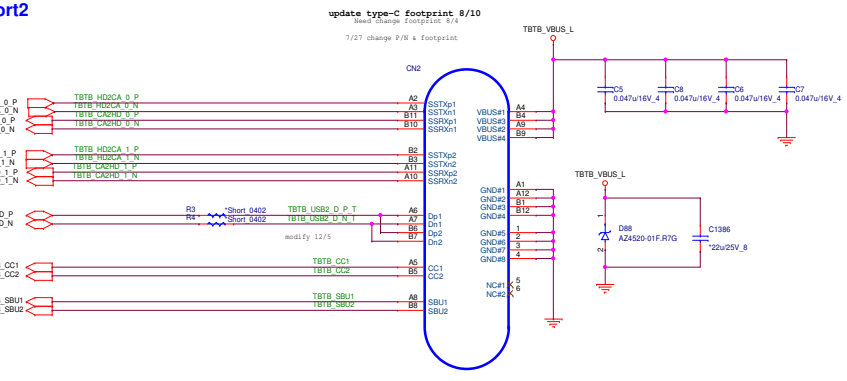
Quanta Computer Inc.
PROJECT : ZGQ
TI TPS65982

TypeC-Port1

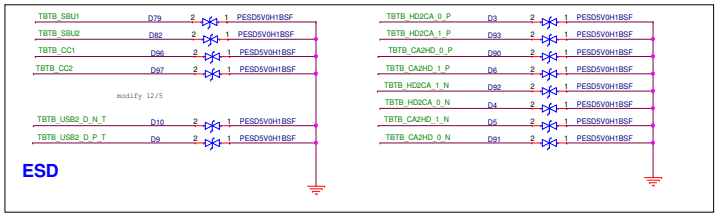


ESD

TypeC-Port2



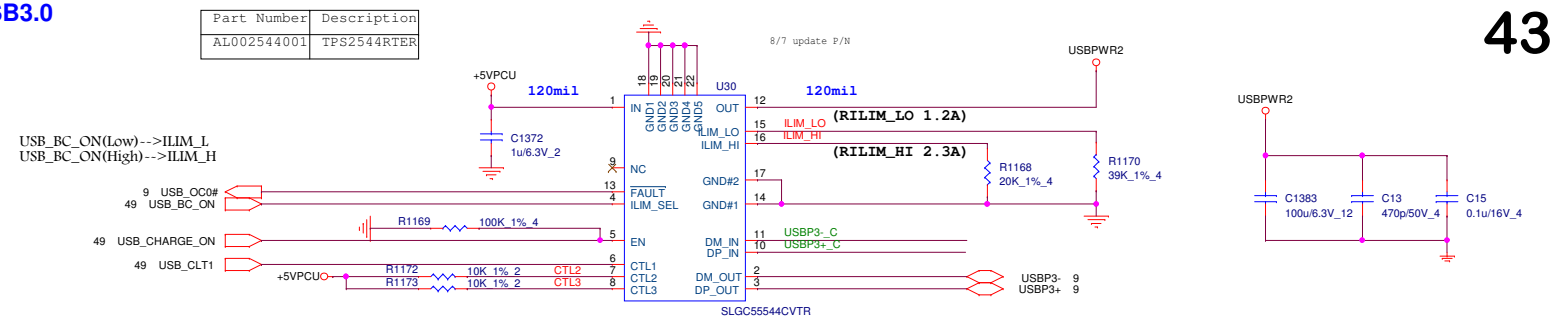
ESD



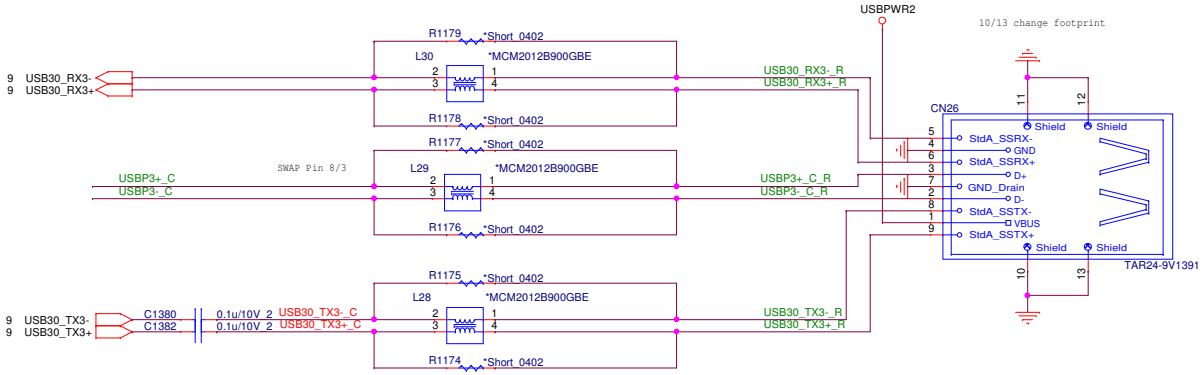
Quanta Computer Inc.		
PROJECT : ZGQ		
Size	Document Number: Type C(USB3.1/DP) *2	Rev 1A
Date: Monday, March 12, 2018	Sheet 42 of 73	

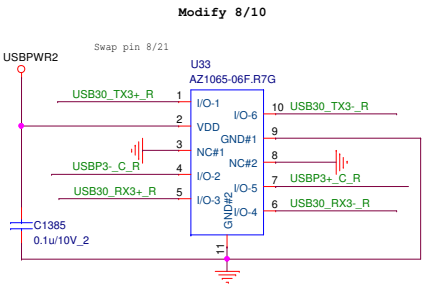
BC1.2 -USB3.0

Part Number	Description
AL002544001	TPS2544RTER



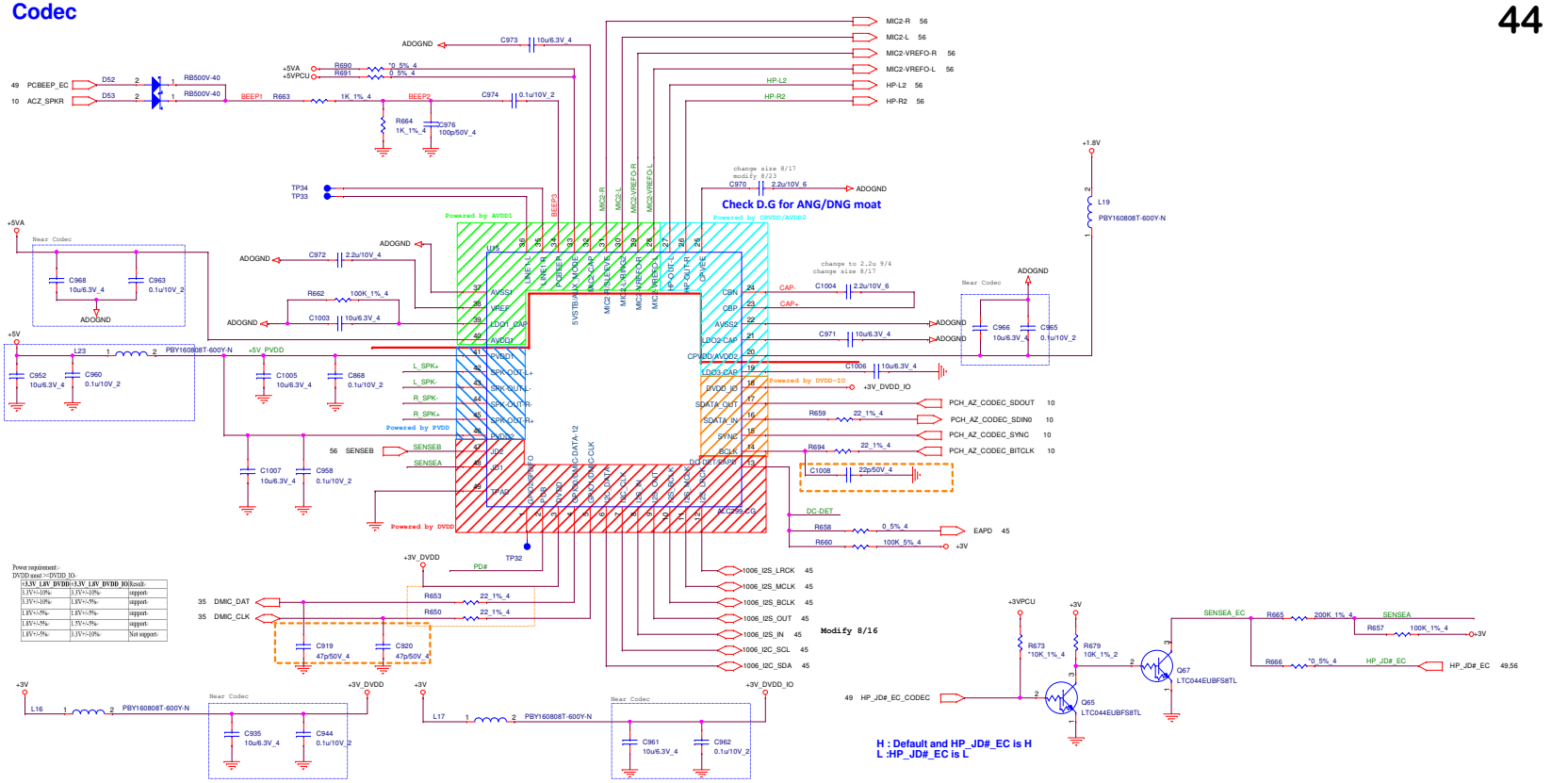
USB 3.0(UB3)



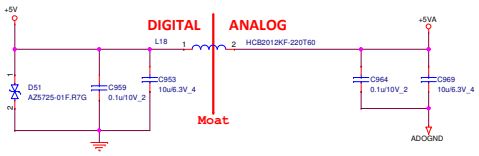


Quanta Computer Inc.		
PROJECT : ZGQ		
Size	Document Number: USB2.0*1/USB3.0*3/BC1.2	Rev: 1A
Date: Monday, March 12, 2018	Sheet 43 of 73	

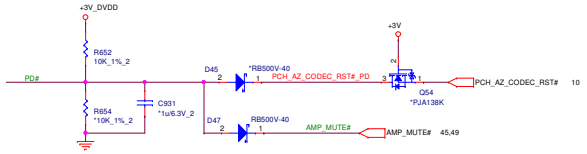
Codec



Codec PWR 5V(ADO)

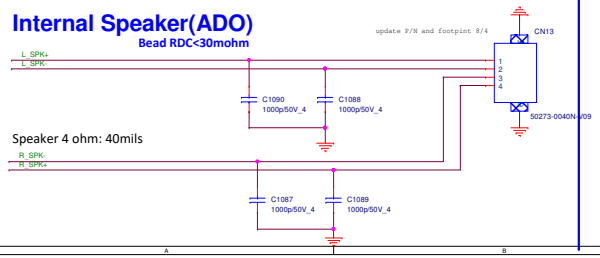


Mute(ADO)

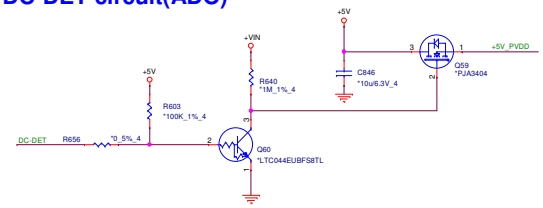


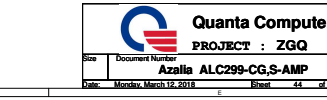
Internal Speaker(ADO)

Bead RDC<30mohm

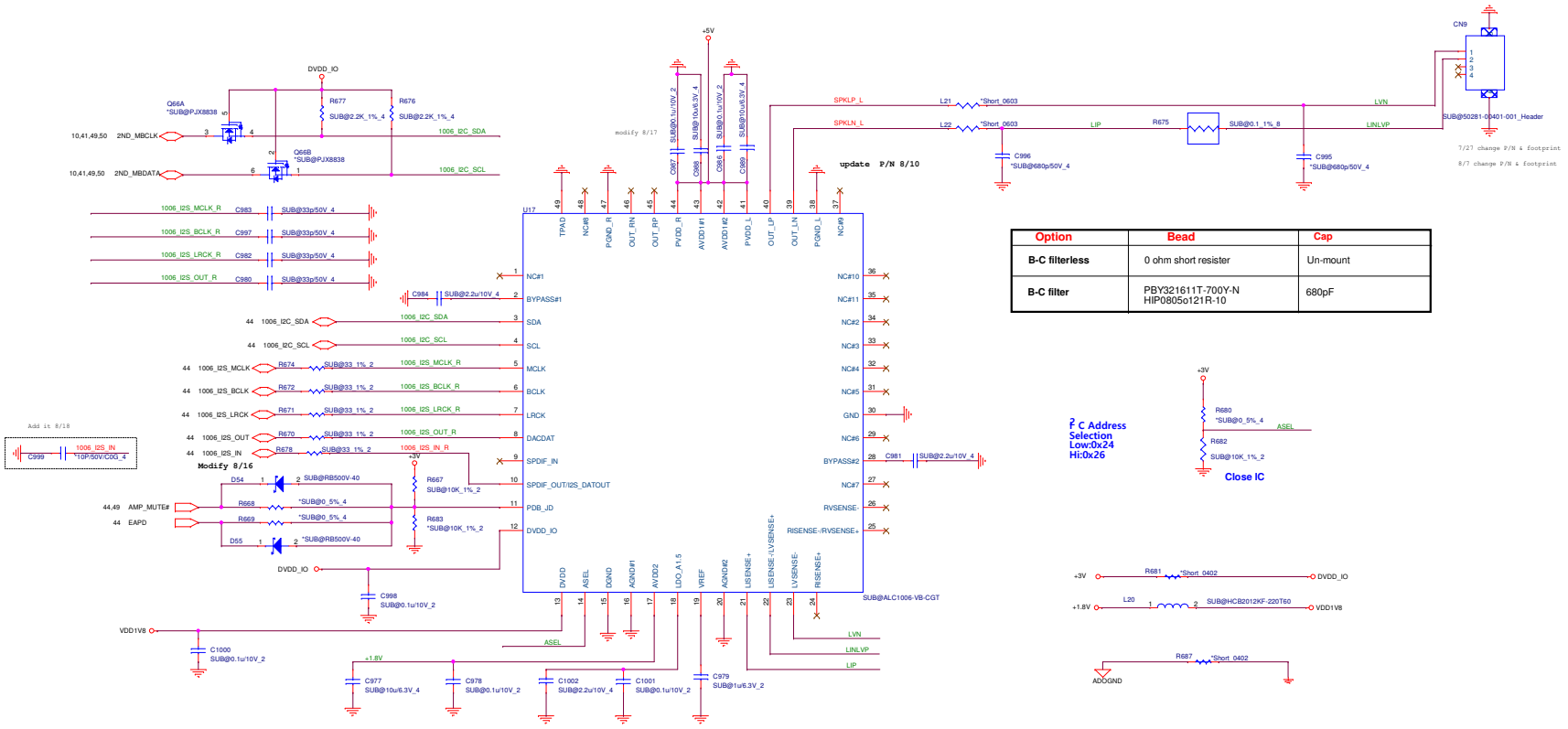


DC-DET circuit(ADO)





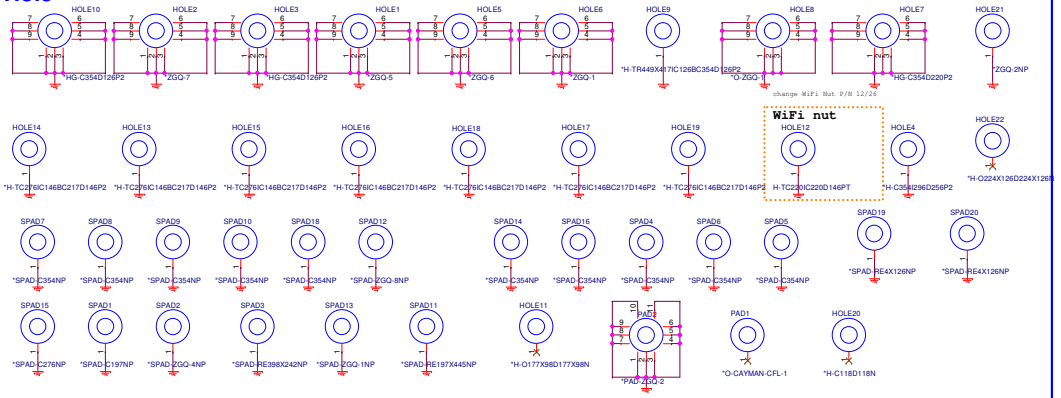
SubWoofer



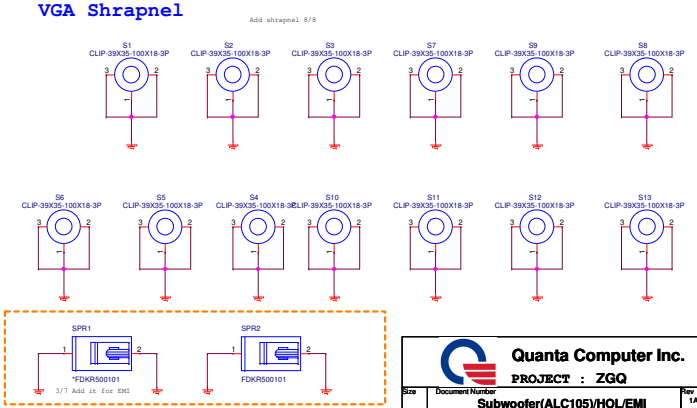
Option	Bead	Cap
B-C filterless	0 ohm short resister	Un-mount
B-C filter	PBY321611T-700Y-N HIP0805o121R-10	680pF

change U17 Pin16~Pin20 to GND 10/16

Hole



VGA Shrapnel



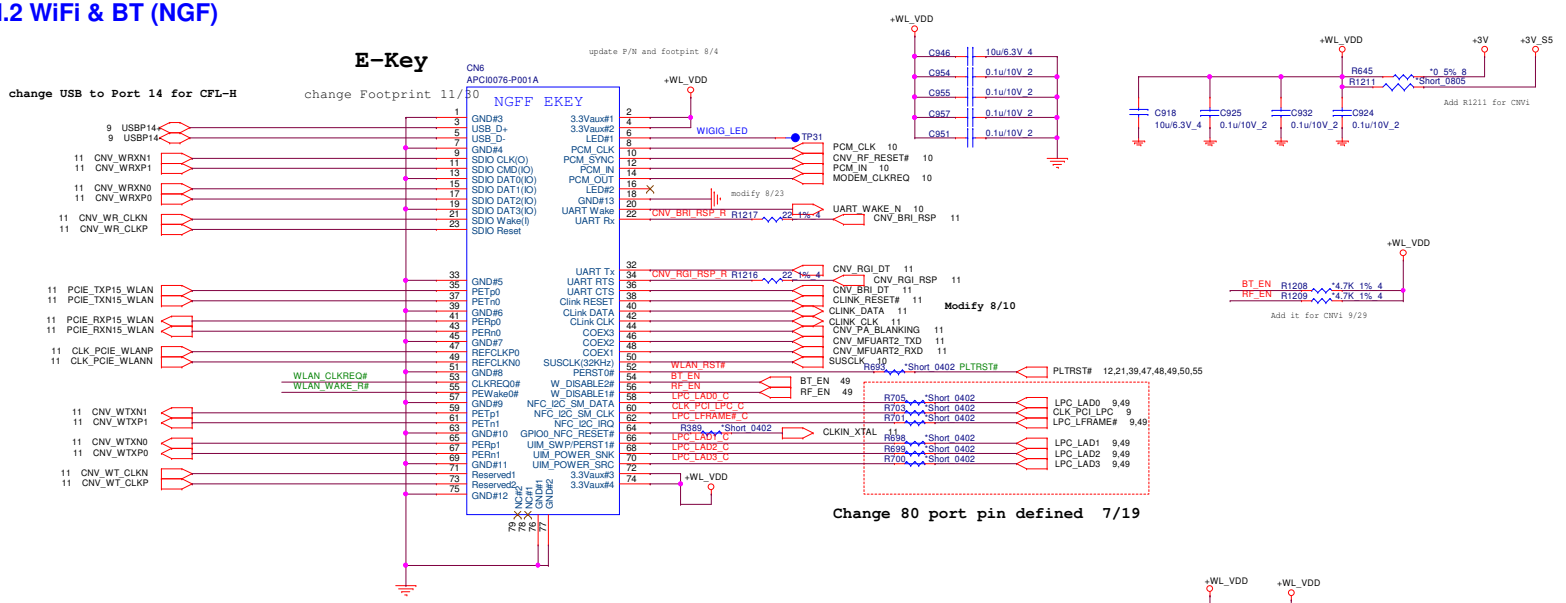
Quanta Computer Inc.

PROJECT : ZGQ

Size	Document Number	Rev
	Subwoofer(ALC105)/HOL/EMI	1A

Date: Monday, March 12, 2018 Sheet 45 of 73

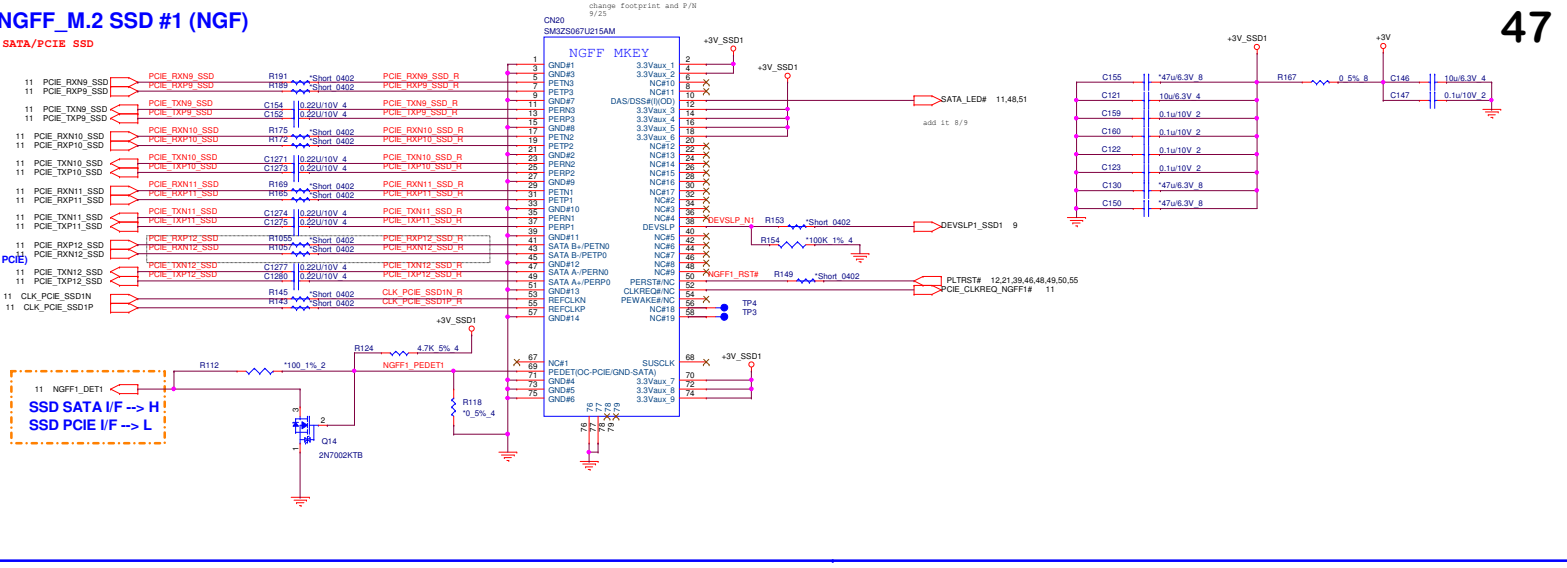
NGFF_M.2 WiFi & BT (NGF)



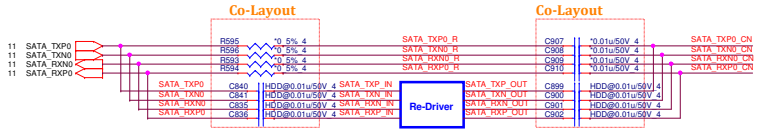
Quanta Computer Inc.			
PROJECT : ZGQ			
Size	Document Number		Rev
	NGFF WiFi & BT		1A
Date: Monday, March 12, 2018	Sheet 46 of 73		

NGFF_M.2 SSD #1 (NGF)

SATA/PCIE SSD



HDD



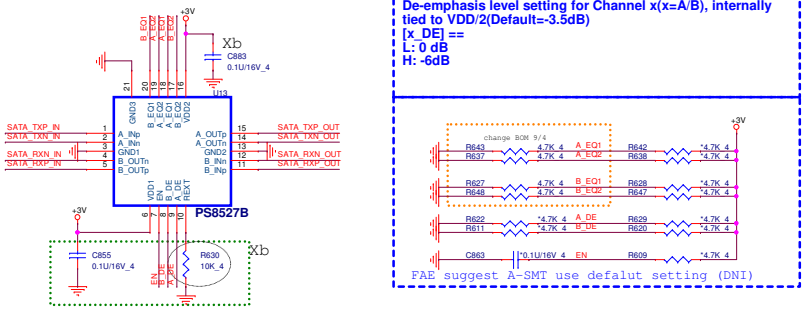
HDD Re-driever

SATA re-driver IC
stuff Rb,Cb,Xb , unstuff Ra,Ca

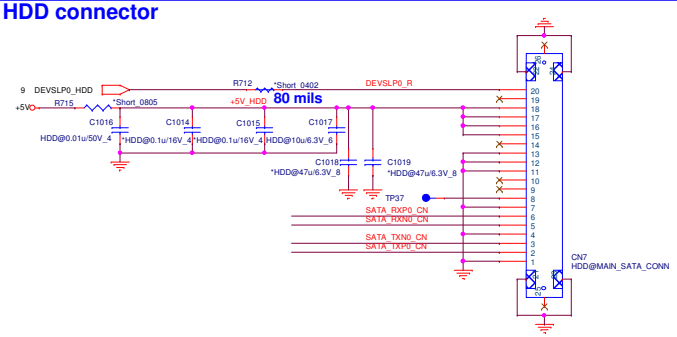
Normal
stuff Ra,Ca , unstuff Rb,Cb

Equalization level setting for Channel x(x=A/B),internally tied to VDD/2 (default:12.2dB)
[x_EQ2, x_EQ1] ==
L/L: for channel loss up to 7.4dB
L/H: for channel loss up to 14.4dB
H/L: for channel loss up to 11.2dB
H/H: for channel loss up to 5dB

De-emphasis level setting for Channel x(x=A/B), internally tied to VDD/2(Default=-3.5dB)
[x_DE] ==
L: 0 dB
H: -6dB



HDD connector



Quanta Computer Inc.
PROJECT : ZGQ

Size	Document Number	Rev
	NGFF SSD #1 / HDD	1A
Date: Monday, March 12, 2018	Sheet 47 of 73	

NGFF_M.2 SSD #2 (NGF)

Only for PCIE SSD

change footprint and P/N
9/25

CN23
SM3ZS067U215AM

NGFF MKEY

1	GND#1	3.3Vaux_1	2
3	GND#3	3.3Vaux_2	4
5	PETN3	NC#10	6
7	PETP3	NC#11	8
9	GND#7	DAS/DSS#(I)(OD)	10
11	PERN3	3.3Vaux_3	12
13	PERP3	3.3Vaux_4	14
15	GND#8	3.3Vaux_5	16
17	PETN2	3.3Vaux_6	18
19	PETP2	NC#12	20
21	GND#2	NC#13	22
23	PERN2	NC#14	24
25	PERP2	NC#15	26
27	GND#9	NC#16	28
29	PETN1	NC#17	30
31	PETP1	NC#2	32
33	GND#10	NC#3	34
35	PERN1	NC#4	36
37	PERP1	DEVSLP	38
39	GND#11	NC#5	40
41	SATA B+/PETN0	NC#6	42
43	SATA B-/PETP0	NC#7	44
45	GND#12	NC#8	46
47	SATA A-/PERN0	NC#9	48
49	SATA A+/PERP0	PERST#/NC	50
51	GND#13	CLKREQ#/NC	52
53	REFCLKN	PEWAKE#/NC	54
55	REFCLKP	NC#18	56
57	GND#14	NC#19	58
67	NC#1	SUSCLK	68
69	PEDET(OC-PCIE/GND-SATA)		70
71	GND#4	3.3Vaux_7	72
73	GND#5	3.3Vaux_8	74
75	GND#6	3.3Vaux_9	76
77			78
79			

+3V_SSD2
+3V_SSD2
+3V_SSD2

SATA_LED# 11,47,51

add it 8/9

DEVSLP_N2 R31 *Short_0402 DEVSLP4_SSD2 9
R32 *100K_1%_4

NGFF2_RST# R25 *Short_0402 PLTRST# 12,21,39,46,47,49,50,55
PCIE_CLKREQ_NGFF2# 11

TP2
TP1

9 PCIE_RXN24_SSD	PCIE_RXN24_SSD	R90	*Short_0402	PCIE_RXN24_SSD_R
9 PCIE_RXP24_SSD	PCIE_RXP24_SSD	R80	*Short_0402	PCIE_RXP24_SSD_R
9 PCIE_TXN24_SSD	PCIE_TXN24_SSD	C1299	0.22U/10V_4	PCIE_TXN24_SSD_R
9 PCIE_TXP24_SSD	PCIE_TXP24_SSD	C1302	0.22U/10V_4	PCIE_TXP24_SSD_R
9 PCIE_RXN23_SSD	PCIE_RXN23_SSD	R70	*Short_0402	PCIE_RXN23_SSD_R
9 PCIE_RXP23_SSD	PCIE_RXP23_SSD	R61	*Short_0402	PCIE_RXP23_SSD_R
9 PCIE_TXN23_SSD	PCIE_TXN23_SSD	C1312	0.22U/10V_4	PCIE_TXN23_SSD_R
9 PCIE_TXP23_SSD	PCIE_TXP23_SSD	C1314	0.22U/10V_4	PCIE_TXP23_SSD_R
9 PCIE_RXN22_SSD	PCIE_RXN22_SSD	R46	*Short_0402	PCIE_RXN22_SSD_R
9 PCIE_RXP22_SSD	PCIE_RXP22_SSD	R41	*Short_0402	PCIE_RXP22_SSD_R
9 PCIE_TXN22_SSD	PCIE_TXN22_SSD	C1331	0.22U/10V_4	PCIE_TXN22_SSD_R
9 PCIE_TXP22_SSD	PCIE_TXP22_SSD	C1339	0.22U/10V_4	PCIE_TXP22_SSD_R
9 PCIE_RXP21_SSD	PCIE_RXP21_SSD	R35	*Short_0402	PCIE_RXP21_SSD_R
9 PCIE_RXN21_SSD	PCIE_RXN21_SSD	R29	*Short_0402	PCIE_RXN21_SSD_R
9 PCIE_TXN21_SSD	PCIE_TXN21_SSD	C1354	0.22U/10V_4	PCIE_TXN21_SSD_R
9 PCIE_TXP21_SSD	PCIE_TXP21_SSD	C1364	0.22U/10V_4	PCIE_TXP21_SSD_R
11 CLK_PCIE_SSD2N	R23	*Short_0402	CLK_PCIE_SSD2N_R	
11 CLK_PCIE_SSD2P	R20	*Short_0402	CLK_PCIE_SSD2P_R	

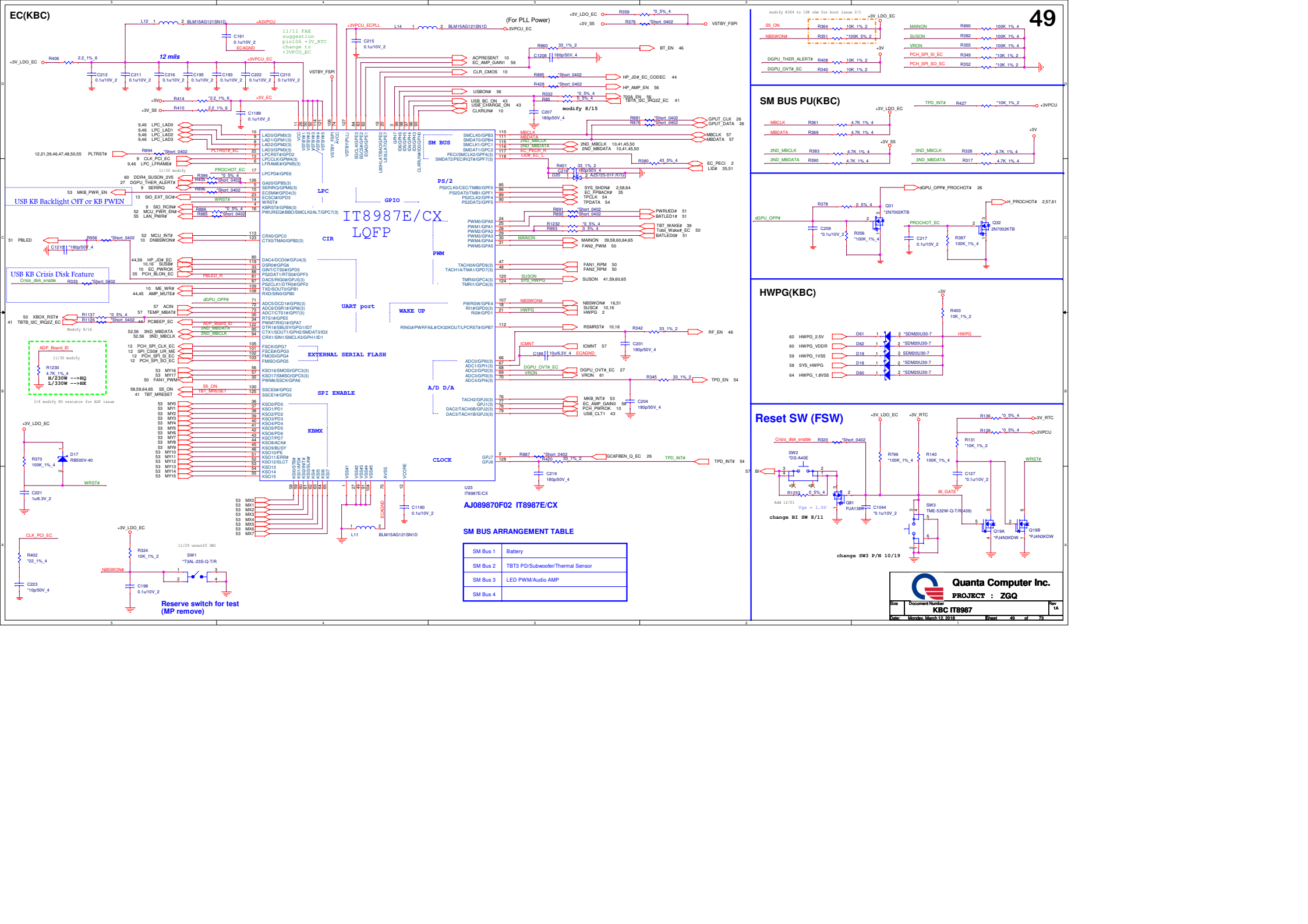
Del SSD detcet circuit for PCIE SSD RAID 2/1

+3V_SSD2
+3V

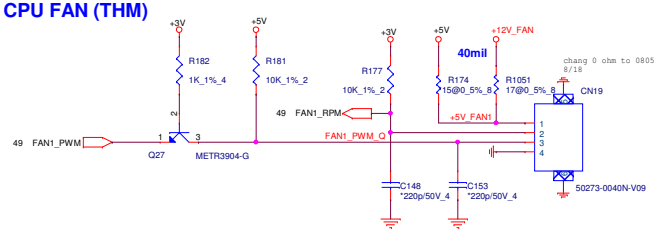
C35	*47u/6.3V_8	R44	0_5%_8	C48 10u/6.3V_4
C27	10u/6.3V_4			C47 0.1u/10V_2
C20	0.1u/10V_2			
C88	0.1u/10V_2			
C82	0.1u/10V_2			
C18	0.1u/10V_2			
C62	*47u/6.3V_8			
C75	*47u/6.3V_8			

Quanta Computer Inc.
PROJECT : ZGQ

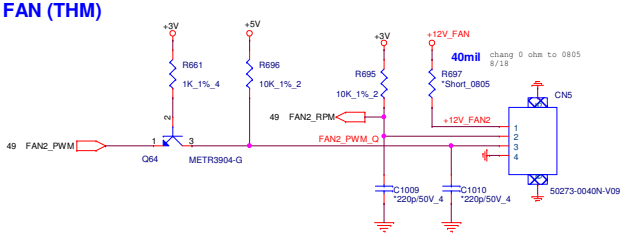
Size	Document Number	Rev
	NGFF SSD #2	1A
Date: Monday, March 12, 2018	Sheet 48 of 73	


EC(KBC)
(For PLL Power)
IT8987E/CX
LQFP
LPC
GPIO
SM BUS
PS/2
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
USB KB Backlight OFF or KB PWEN
USB KB Crisis Disk Feature
Reserve switch for test
(MP remove)
AJ089870F02 IT8987E/CX
SM BUS ARRANGEMENT TABLE
SM Bus 1 Battery
SM Bus 2 TBT3 PD/Subwoofer/Thermal Sensor
SM Bus 3 LED PWM/Audio AMP
SM Bus 4
SM BUS PU(KBC)
HWPG(KBC)
Reset SW (FSW)
change BI SW 8/11
change SW3 P/N 10/19
Quanta Computer Inc.
PROJECT : ZGQ
KBC IT8987
Monday, March 12, 2018
49

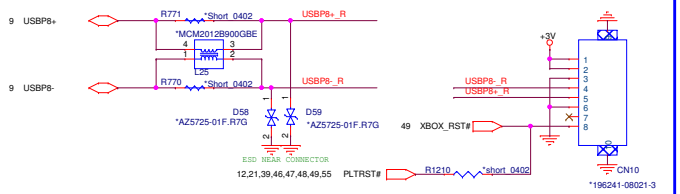
CPU FAN (THM)



GPU FAN (THM)

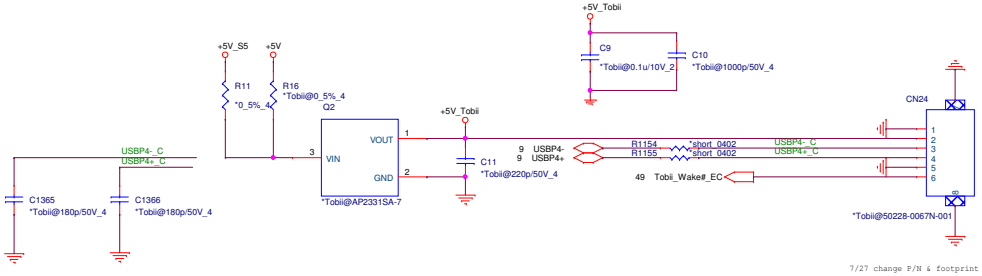


Xbox



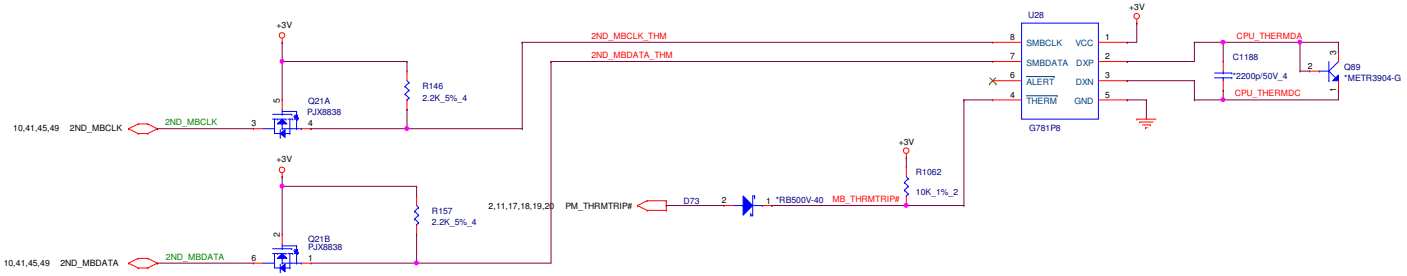
mirror CN10 pin defined 10/5

Tobii



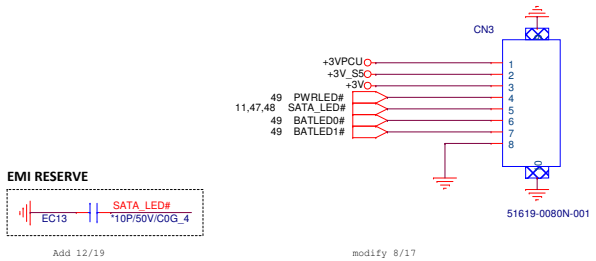
7/27 change P/N & footprint

CPU Thermal Sensor,Local CPU Thermal Sensor

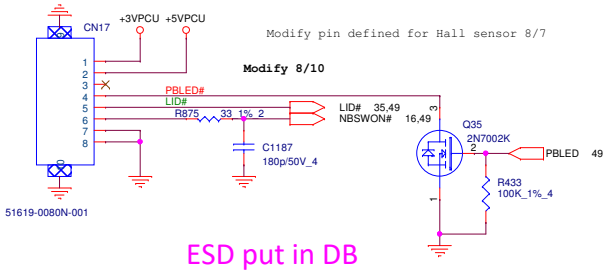


Quanta Computer Inc.			
PROJECT : ZGQ			
Size	Document Number		Rev
	FAN,Thermal,FAN LED		1A
Date: Monday, March 12, 2018		Sheet 50 of 73	

UIF LED(UIF)



Power BUTTON



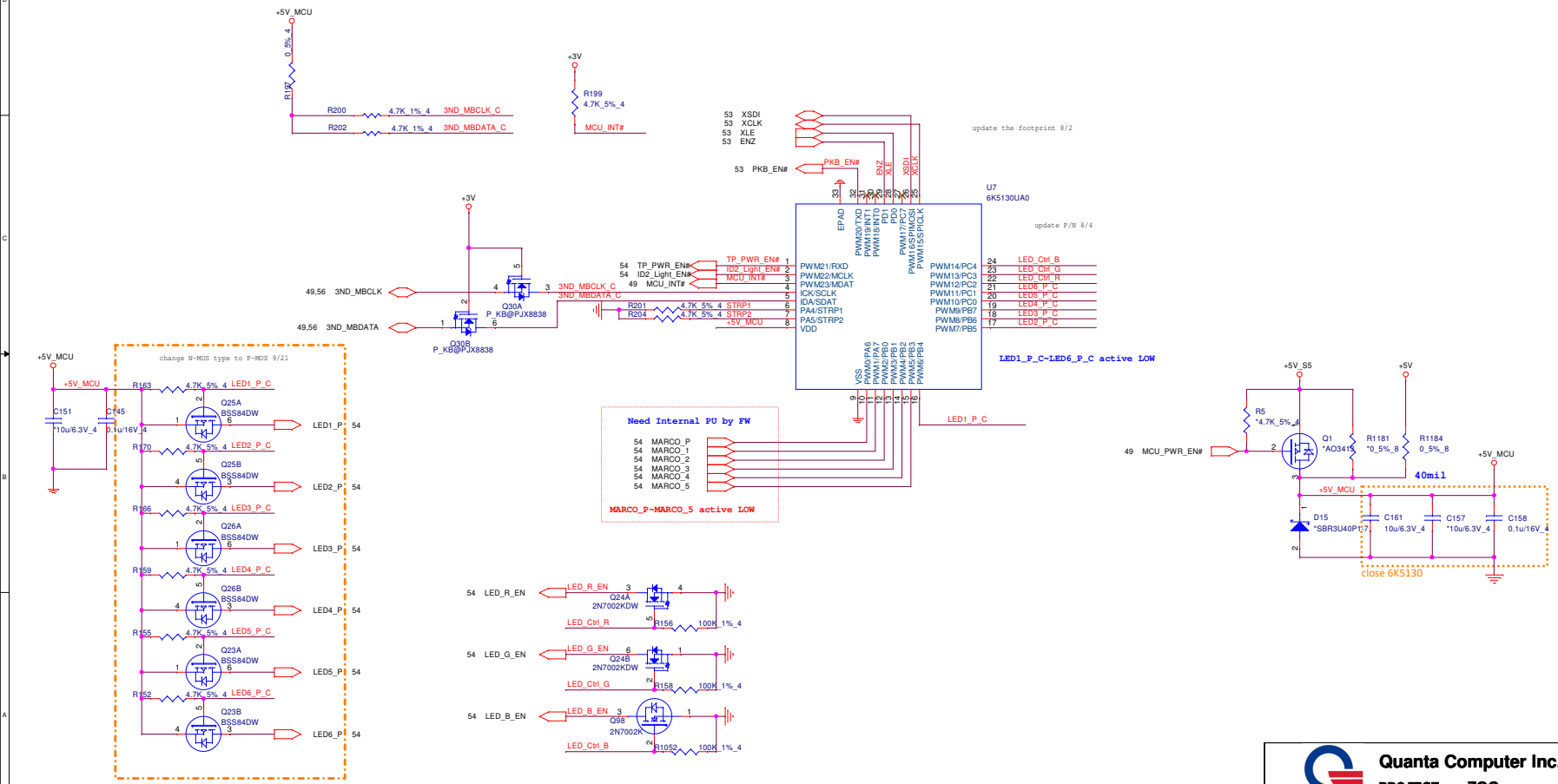
ESD put in DB

Quanta Computer Inc.

PROJECT : ZGQ

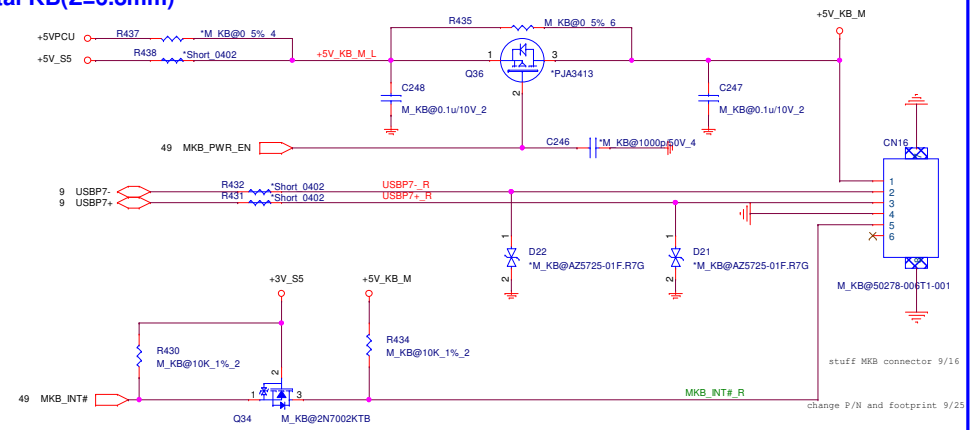
Size	Document Number	Rev
	Power Board / UIF LED	1A

Date: Monday, March 12, 2018 Sheet 51 of 73

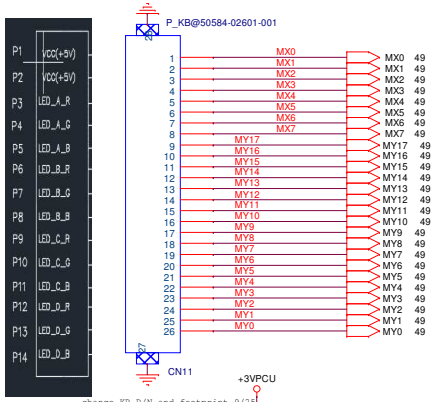


Quanta Computer Inc.			
PROJECT : ZGQ			
Size	Document Number		Rev
	MCU PWM/LED Driver		1A
Date: Monday, March 12, 2018		Sheet 52 of 73	

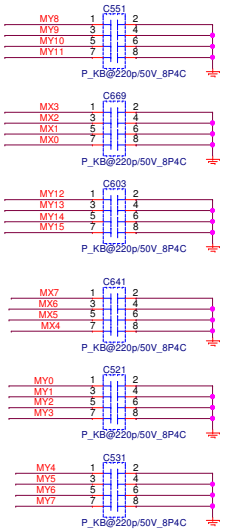
Metal KB(Z=6.8mm)



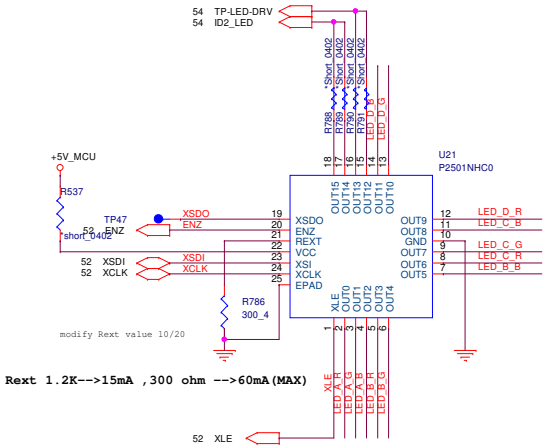
Plastic KB(Z=5.8mm)

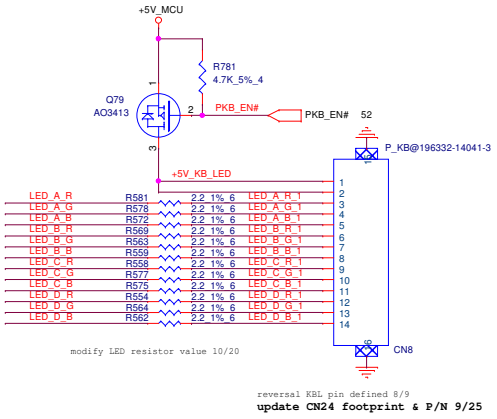


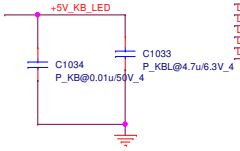
Swap pin 8/21

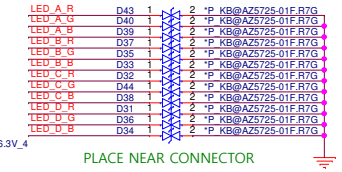


Plastic KB(Z=5.8mm)







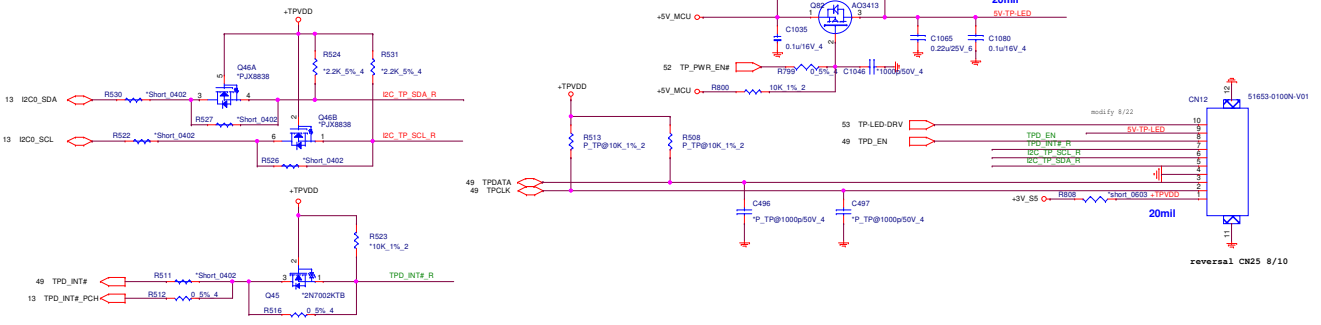


Quanta Computer Inc.

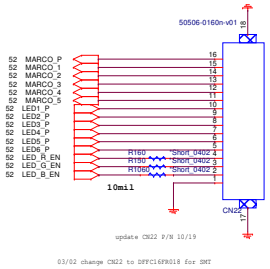
PROJECT : ZGQ

Size	Document Number	Rev
	KeyBoard	1A
Date: Monday, March 12, 2018	Sheet 53 of 73	

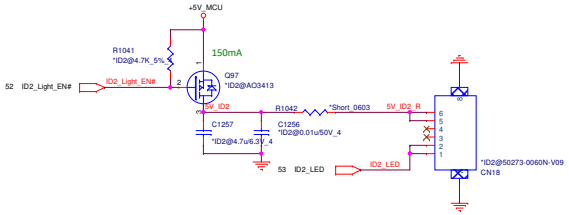
Plastic-Touch PAD



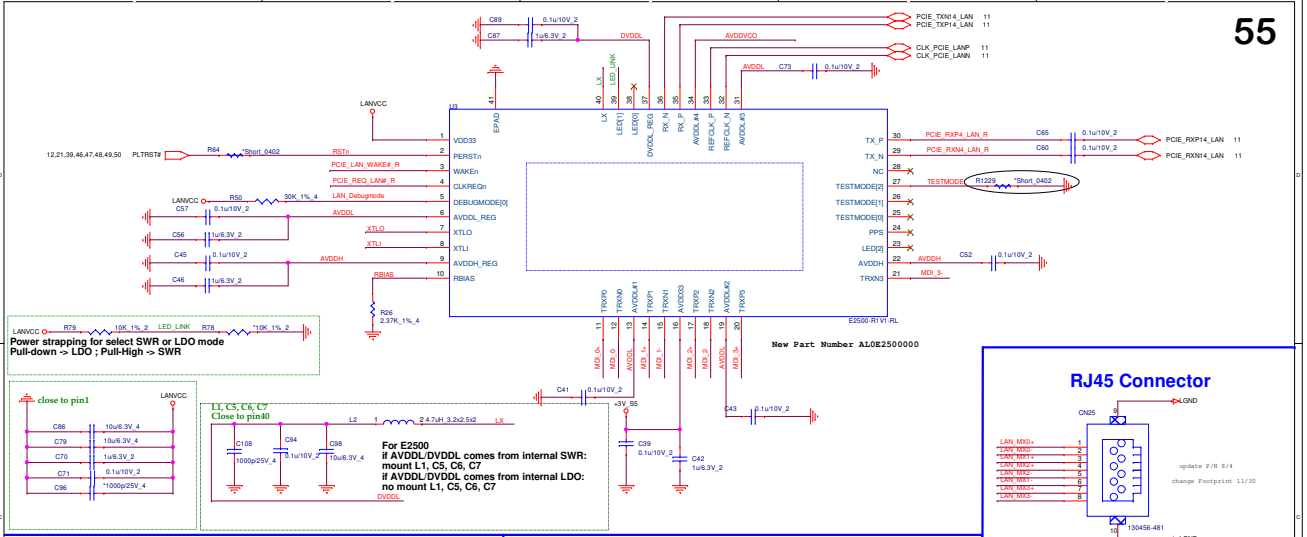
Macro Key LED



Base backlight for ID2

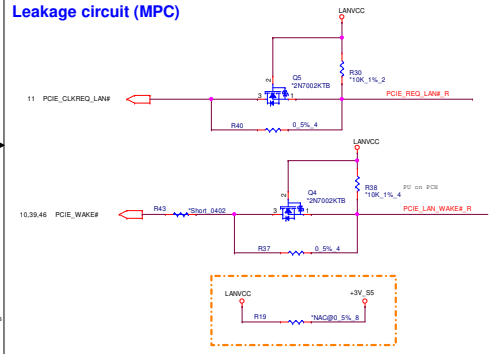


Quanta Computer Inc.		
PROJECT : ZGQ		
Size	Document Number: Macro key/LCD Cover/TP	Rev: 1A
Date: Monday, March 12, 2018	Sheet 54 of 73	



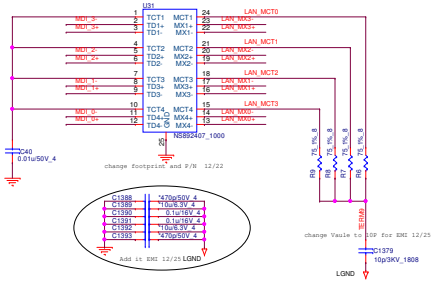
RJ45 Connector

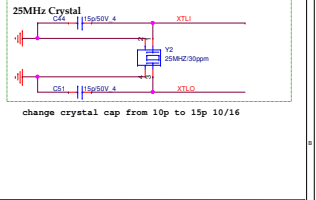
Leakage circuit (MPC)

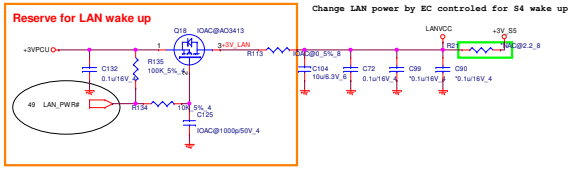


Tramsformer

DB0LL1LAN00 --> Main
DB0Z06LAN00 --> 2'nd

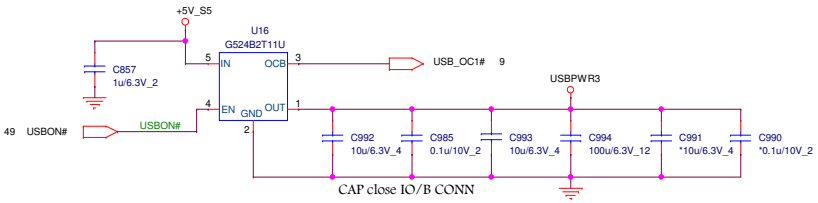






Quanta Computer Inc.			
PROJECT : ZGQ			
Size	Document Number: LAN E2500		Rev: 1A
Date: Monday, March 12, 2018	Sheet 55 of 73		

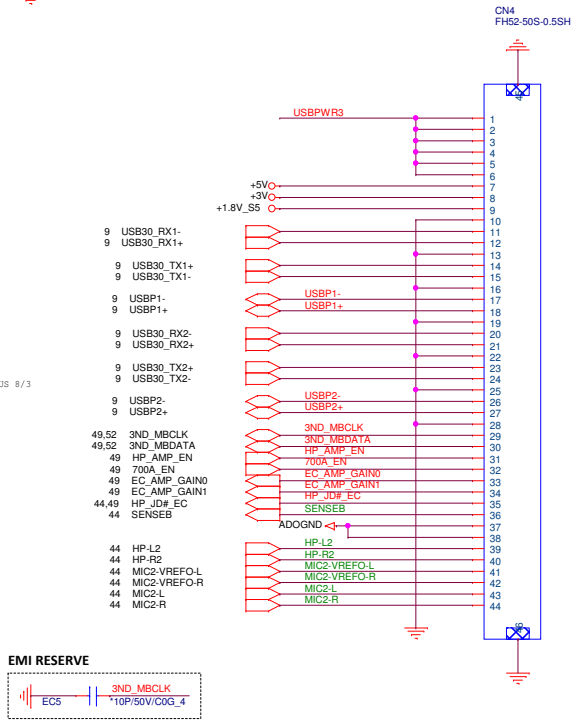
update footprint 8/4



CAP close IO/B CONN

change to 3nd SMBUS 8/3

Modify 9/26



change footprint to 51540-05001-v01-50p-1 8/16

EMI RESERVE

Quanta Computer Inc.

PROJECT : ZGQ

Size	Document Number	Rev
	IO/B	1A
Date: Monday, March 12, 2018	Sheet 56 of 73	

ADP (MAX) =330W

EMI requirement

PD=3W

EMI requirement

PD=3W

Vin <9.72 ==> prochot is low for 3S1P

RAMP 0307

V_ PMON=K*Total*R
1.2V=1uA*Total*R

CS32262FB15RES CHIP 22.6K 1/16W +-1%(0402) for 330W

RAMP 0307

Double Check if BI pin PU Low

RAMP 0307

2017/3/6 Adds Co-lay BATT Connector

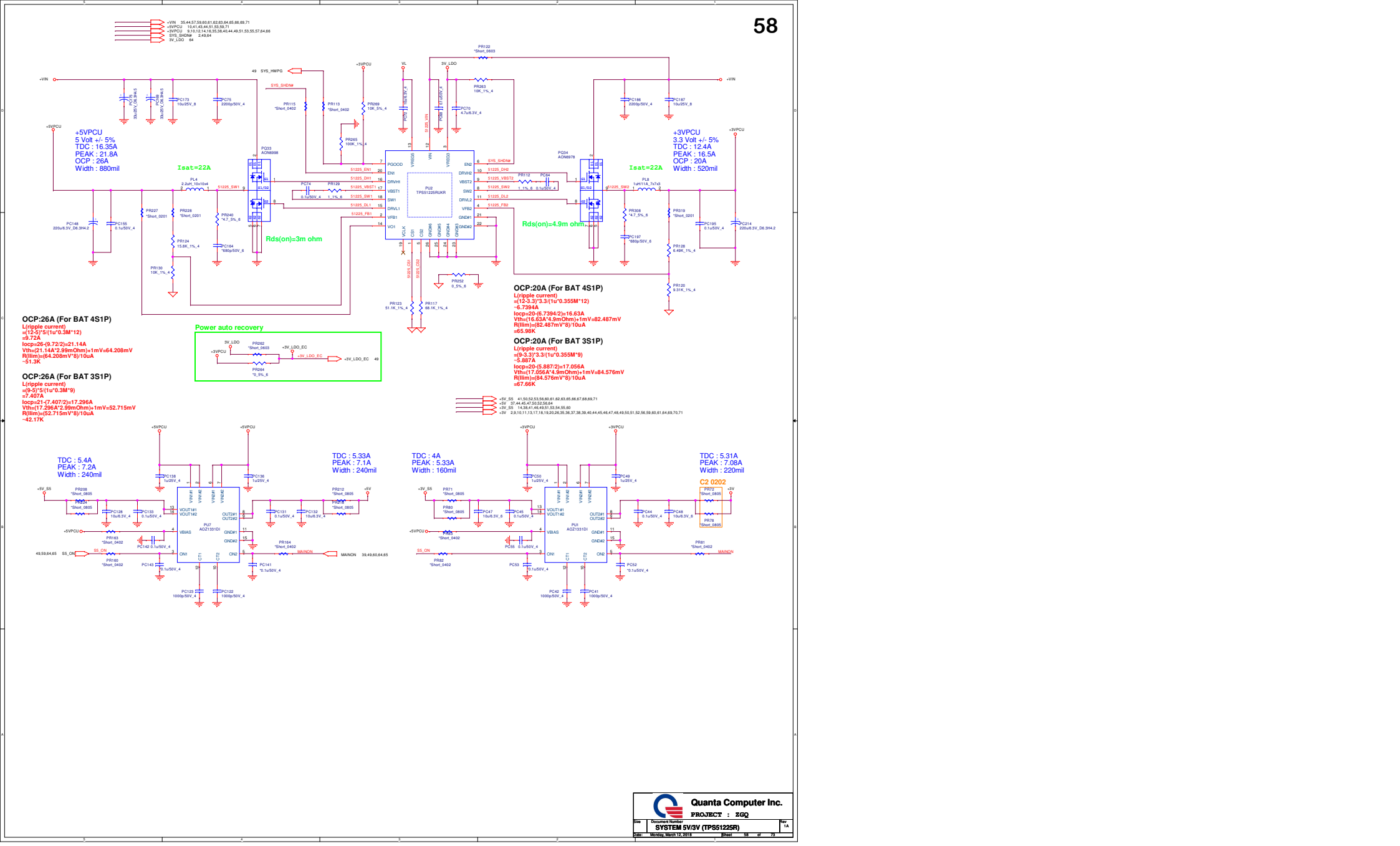
C2 0202

C2 0202

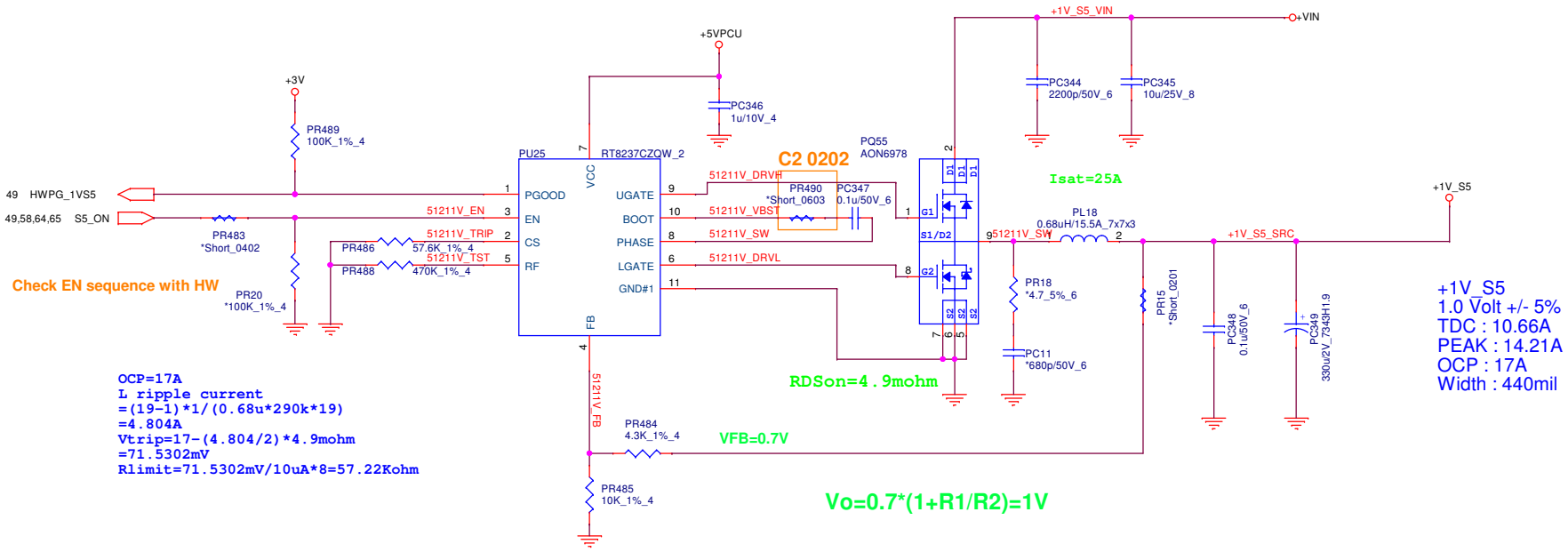
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 7.93A current limit

ILIM=0.793V
Rsr = 0.01ohm

Quanta Computer Inc.			
PROJECT : ZGQ			
Size	Document Number		Rev
	Charger (BQ24780S)		1A
Date: Monday, March 12, 2018	Sheet 57 of 73		

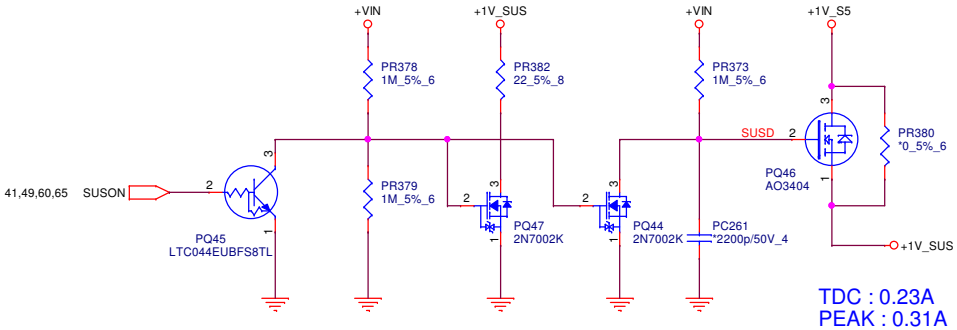

+5VPCU
5 Volt +/- 5%
TDC : 16.35A
PEAK : 21.8A
OCP : 26A
Width : 880mil
Isat=22A
Rds(on)=3m ohm
+3VPCU
3.3 Volt +/- 5%
TDC : 12.4A
PEAK : 16.5A
OCP : 20A
Width : 520mil
Isat=22A
Rds(on)=4.9m ohm
TPS51225RUKR
OCP:26A (For BAT 4S1P)
L(ripple current)
=(12-5)*5/(1u*0.3M*12)
=9.72A
Iocp=26-(9.72/2)=21.14A
Vth=(21.14A*2.99mOhm)+1mV=64.208mV
R(Ilim)=(64.208mV*8)/10uA
~51.3K
OCP:26A (For BAT 3S1P)
L(ripple current)
=(9-5)*5/(1u*0.3M*9)
=7.407A
Iocp=21-(7.407/2)=17.296A
Vth=(17.296A*2.99mOhm)+1mV=52.715mV
R(Ilim)=(52.715mV*8)/10uA
~42.17K
OCP:20A (For BAT 4S1P)
L(ripple current)
=(12-3.3)*3.3/(1u*0.355M*12)
~6.7394A
Iocp=20-(6.7394/2)=16.63A
Vth=(16.63A*4.9mOhm)+1mV=82.487mV
R(Ilim)=(82.487mV*8)/10uA
=65.98K
OCP:20A (For BAT 3S1P)
L(ripple current)
=(9-3.3)*3.3/(1u*0.355M*9)
~5.887A
Iocp=20-(5.887/2)=17.056A
Vth=(17.056A*4.9mOhm)+1mV=84.576mV
R(Ilim)=(84.576mV*8)/10uA
=67.66K
Power auto recovery
TDC : 5.4A
PEAK : 7.2A
Width : 240mil
TDC : 5.33A
PEAK : 7.1A
Width : 240mil
TDC : 4A
PEAK : 5.33A
Width : 160mil
TDC : 5.31A
PEAK : 7.08A
Width : 220mil
C2 0202
Quanta Computer Inc.
PROJECT : ZGQ
SYSTEM 5V/3V (TPS51225R)
Monday, March 12, 2018

+VIN 35,44,57,58,60,61,62,63,64,65,66,69,71
+1V_S5 14
+5VPCU 10,41,43,44,51,53,58,71
+3V 2,9,10,11,13,17,18,19,20,26,35,36,37,38,39,40,44,45,46,47,48,49,50,51,52,56,58,60,61,64,69,70,71
+1V_SUS 6
+VCCIO 2,3,6,16,26,61,64

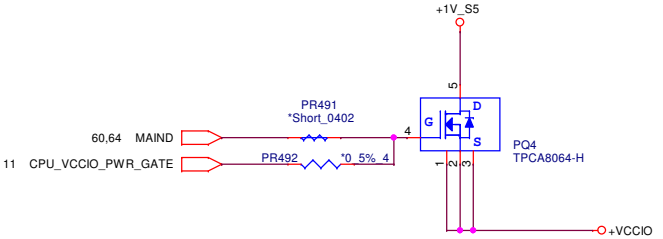


OCP=17A
L ripple current
=(19-1)*1/(0.68u*290k*19)
=4.804A
Vtrip=17-(4.804/2)*4.9mohm
=71.5302mV
Rlimit=71.5302mV/10uA*8=57.22Kohm

+1V_S5
1.0 Volt +/- 5%
TDC : 10.66A
PEAK : 14.21A
OCP : 17A
Width : 440mil



TDC : 0.23A
PEAK : 0.31A
Width : 20mil



TDC : 4.8A
PEAK : 6.4A
Width : 200mil

Quanta Computer Inc.
PROJECT : ZGQ

Size	Document Number	Rev
	+1V_S5 (RT8237CZQW_2)	1A
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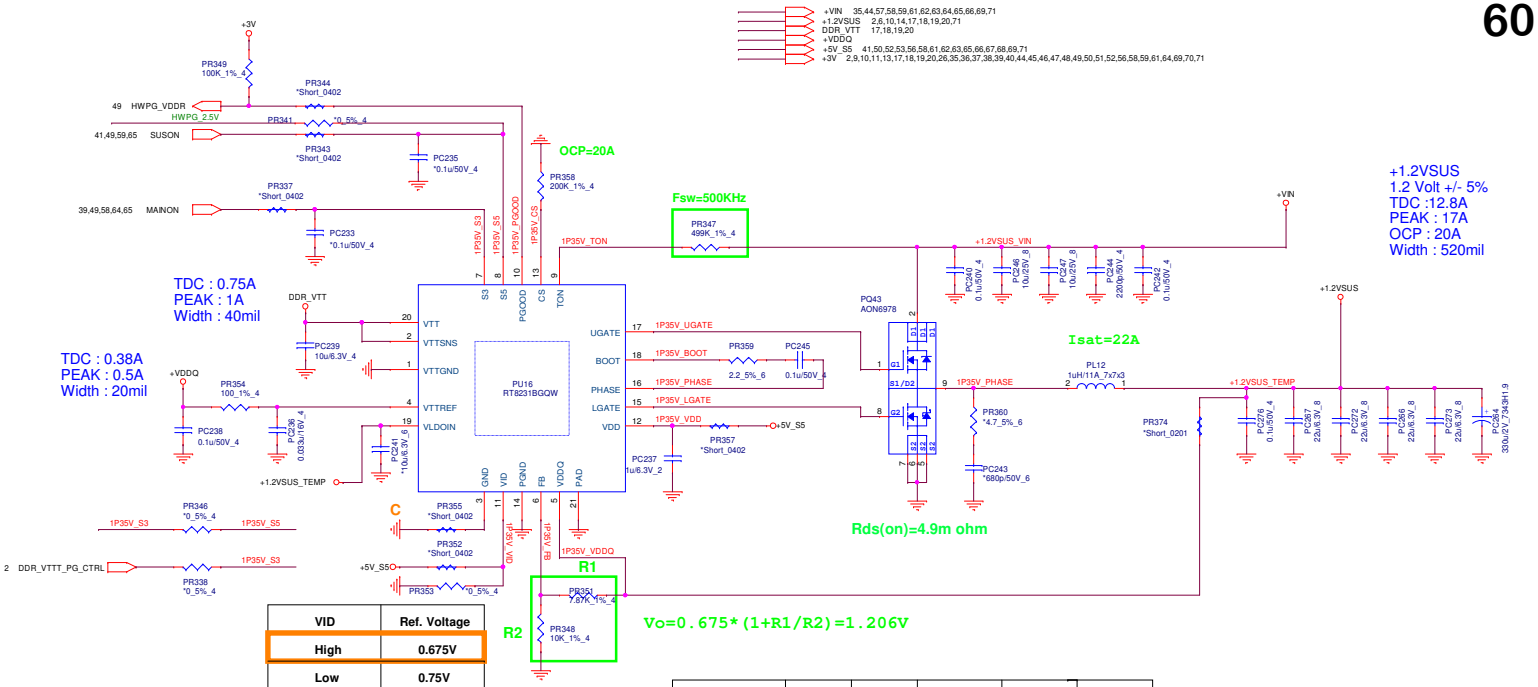


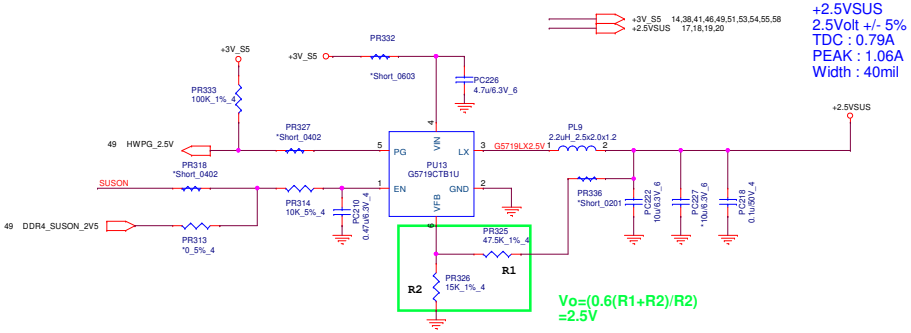
VID	Ref. Voltage
High	0.675V
Low	0.75V

OCP=18A
L ripple current
=(19-1.2)*1.2/(1u*500k*19)
=2.248A
Vtrip=18-(2.248/2)*4.9mohm
=82.691mV
Rlimit=82.691mV/5uA*10=165.38Kohm

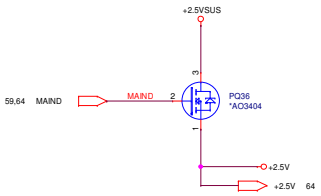
DDR=1.2V
R1=7.87K/F_4
R2=10K/F_4

	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

+2.5VSUS Power Rail For DDR4



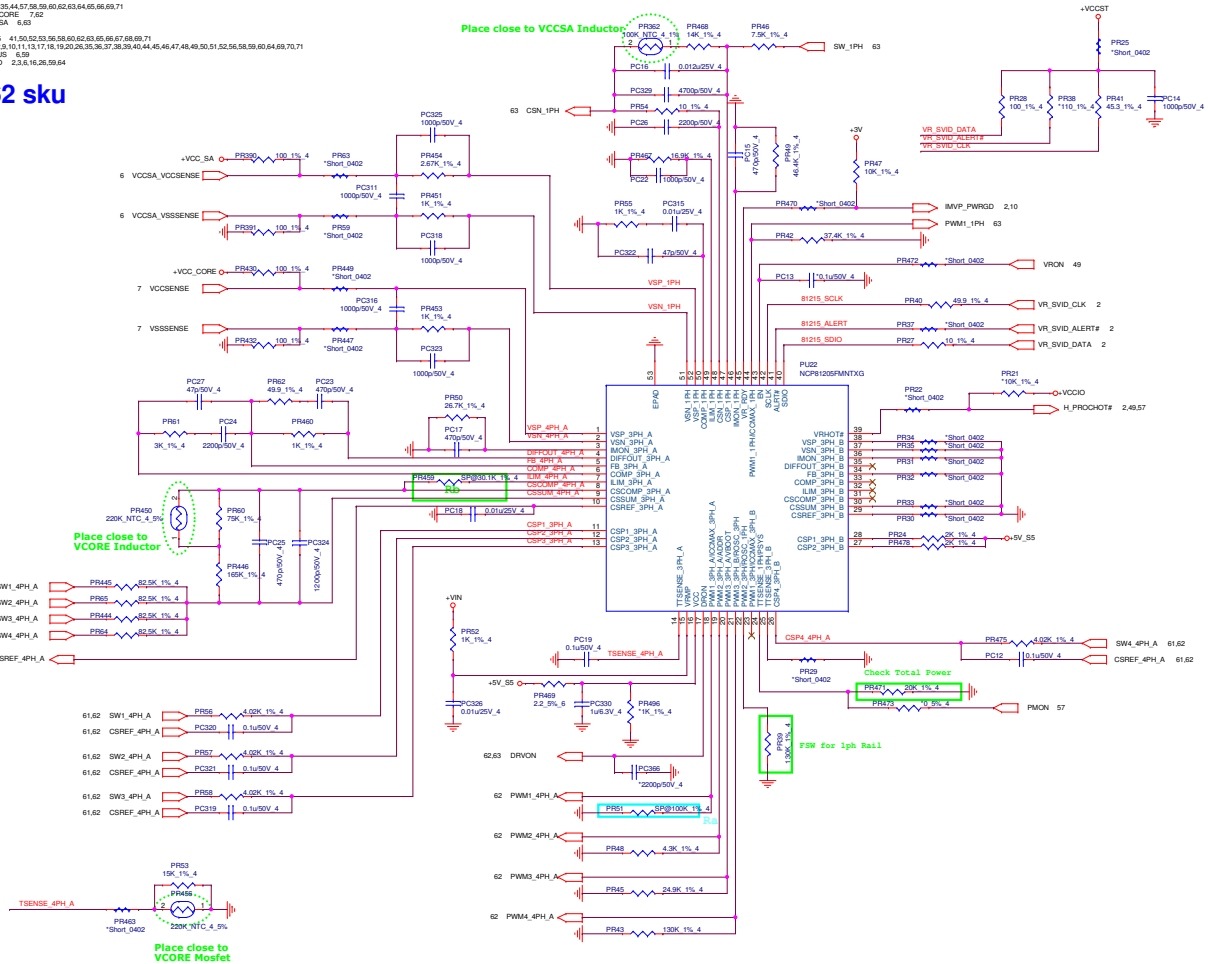
Reserve +2.5V for DDR4 VDDSPD



Quanta Computer Inc.	PROJECT : ZGQ			
Size	Document Number: DDR4_+1.2VSUS (RT8231BGQW)			Rev: 1A
Date: Monday, March 12, 2018	Sheet 60 of 73			

+VIN 35,44,57,58,59,60,62,63,64,65,66,69,71
+VCC_CORE 7,62
+VCC_SA 6,63
+5V_S5 41,50,52,53,56,58,60,62,63,65,66,67,68,69,71
+3V 2,9,10,11,13,17,18,19,20,26,35,36,37,38,39,40,44,45,46,47,48,49,50,51,52,56,58,59,60,64,69,70,71
+1V_SUS 6,59
+VCCIO 2,3,6,16,26,59,64

For H62 sku



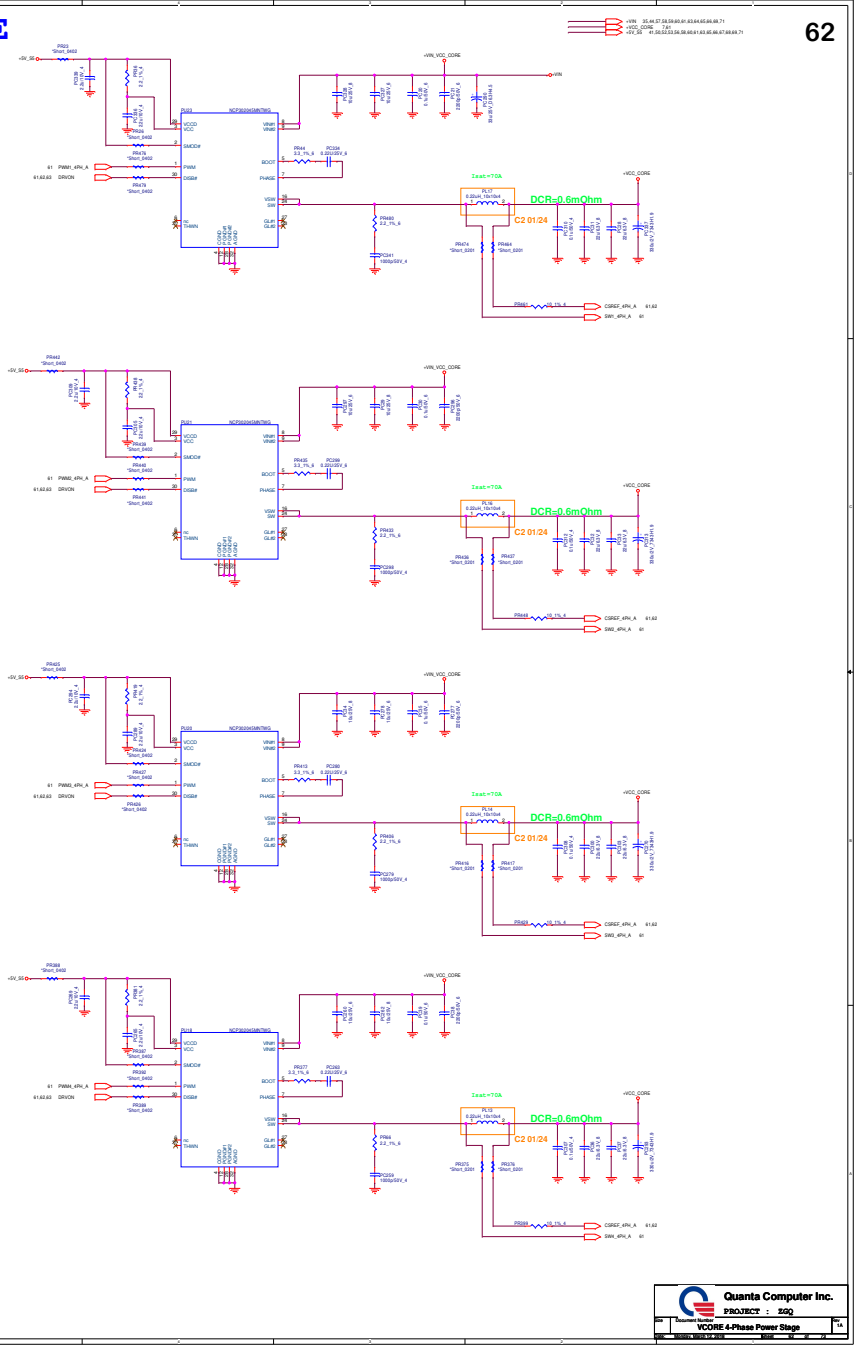
CFL-H62 & (K SKU= H62*1.25) (4+1 Phase)

VCORE	VCCSA
Icc TDC：96A (K=100A)	Icc TDC：10A
Icc Max：128A (K=160A)	Icc Max：11.1A
OCP：166A(K=208A)	OCP：14A
VCORE L/L：	**VCORE L/L：**
R_DC_LL：1.8mV/A	R_DC_LL：10.3mV/A
R_AC_LL：1.8mV/A	R_AC_LL：10.3mV/A

Item	Location	K SKU
Ra	PR51	CS41272FB19 *127K ohm*
Rb	PR459	CS33742FB17 *37.4K ohm*

Quanta Computer Inc.
PROJECT : ZGQ
Size | Document Number: CPU VR IC (NCP81215MNTXG) | Rev 1A
Date: Monday, March 12, 2018 | Sheet 61 of 73

VCORE

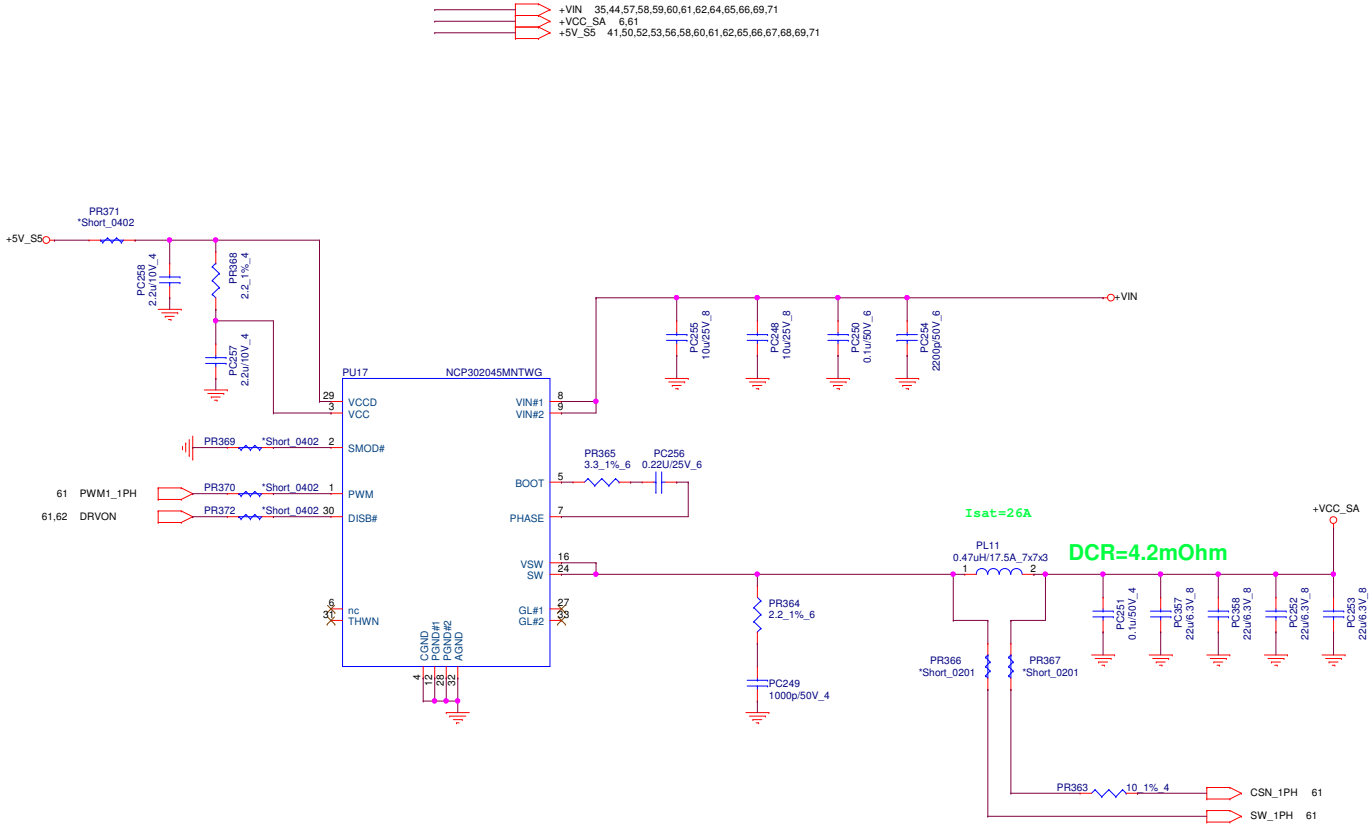


Quanta Computer Inc.

PROJECT : ZGQ

Size	Document Number	Rev
	VCORE 4-Phase Power Stage	1A

VCCSA

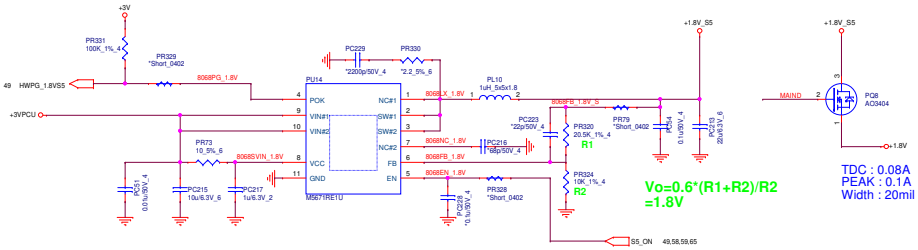


Quanta Computer Inc.		
PROJECT : ZGQ		
Size	Document Number: VCCSA 1-Phase Power Stage	Rev: 1A
Date: Monday, March 12, 2018	Sheet 63 of 73	

+3VPCU 9,10,12,14,16,35,38,40,44,49,51,53,55,57,58,66
+1.8V_S5 14,56,71
+1.8V 27,35,44,45
+3V 2,8,10,11,13,17,18,19,20,26,35,36,37,38,39,40,44,45,46,47,48,49,50,51,52,56,58,59,60,61,69,70,71
3V_LDO 58

+VIN 35,44,57,58,59,60,61,62,63,65,66,69,71
+5V 37,44,45,47,50,52,56,58
+VCCIO 2,3,6,16,26,59,61
+2.5V 60

+1.8V_S5
1.8Volt +/- 5%
TDC : 3A
PEAK : 4A
Width : 120mil

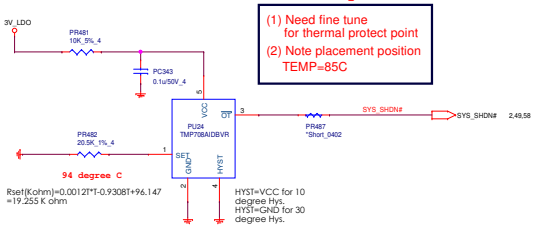


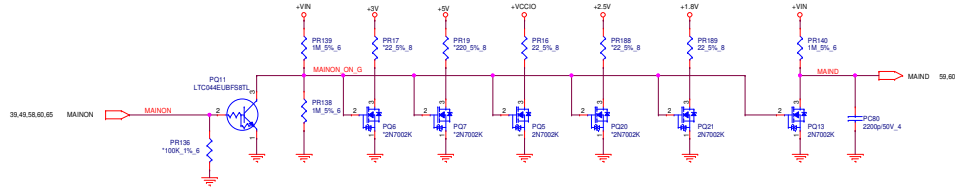
Vo=0.6*(R1+R2)/R2
=1.8V

TDC : 0.08A
PEAK : 0.1A
Width : 20mil

Thermal protection

(1) Need fine tune for thermal protect point
(2) Note placement position TEMP=85C





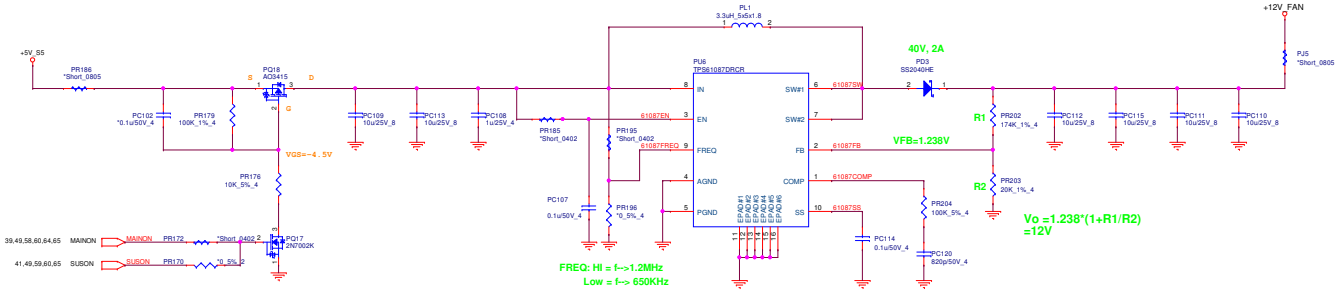
Quanta Computer Inc.
PROJECT : ZGQ

Size	Document Number	Rev
	+1.8V_S5/Thermal Protect	1A
Date: Monday, March 12, 2018	Sheet 64 of 79	

FAN POWER (TPS61087)

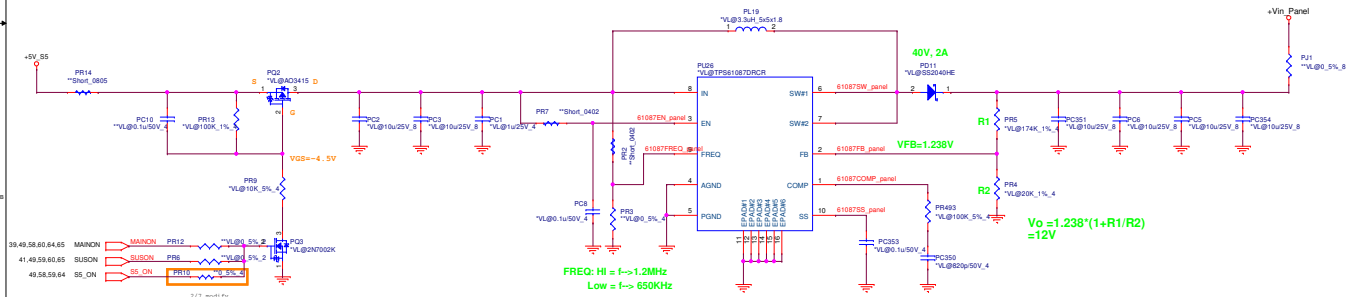
41,50,52,53,56,58,60,61,62,63,66,67,68,69,71 +5V_S5
50 +12V_FAN
35,44,57,58,59,60,61,62,63,64,66,69,71 +VIN

+12V_FAN
12 Volt +/- 5%
Width : 60mil

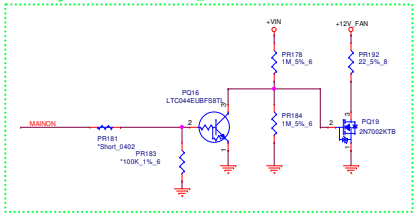


Panel POWER (TPS61087)

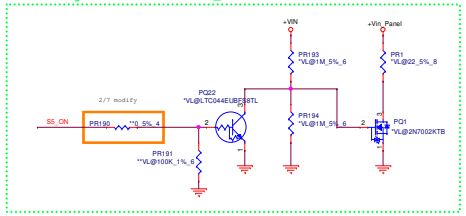
+Vin_Panel
12 Volt +/- 5%
Width : 40mil



Discharge Circuit For +12V_FAN



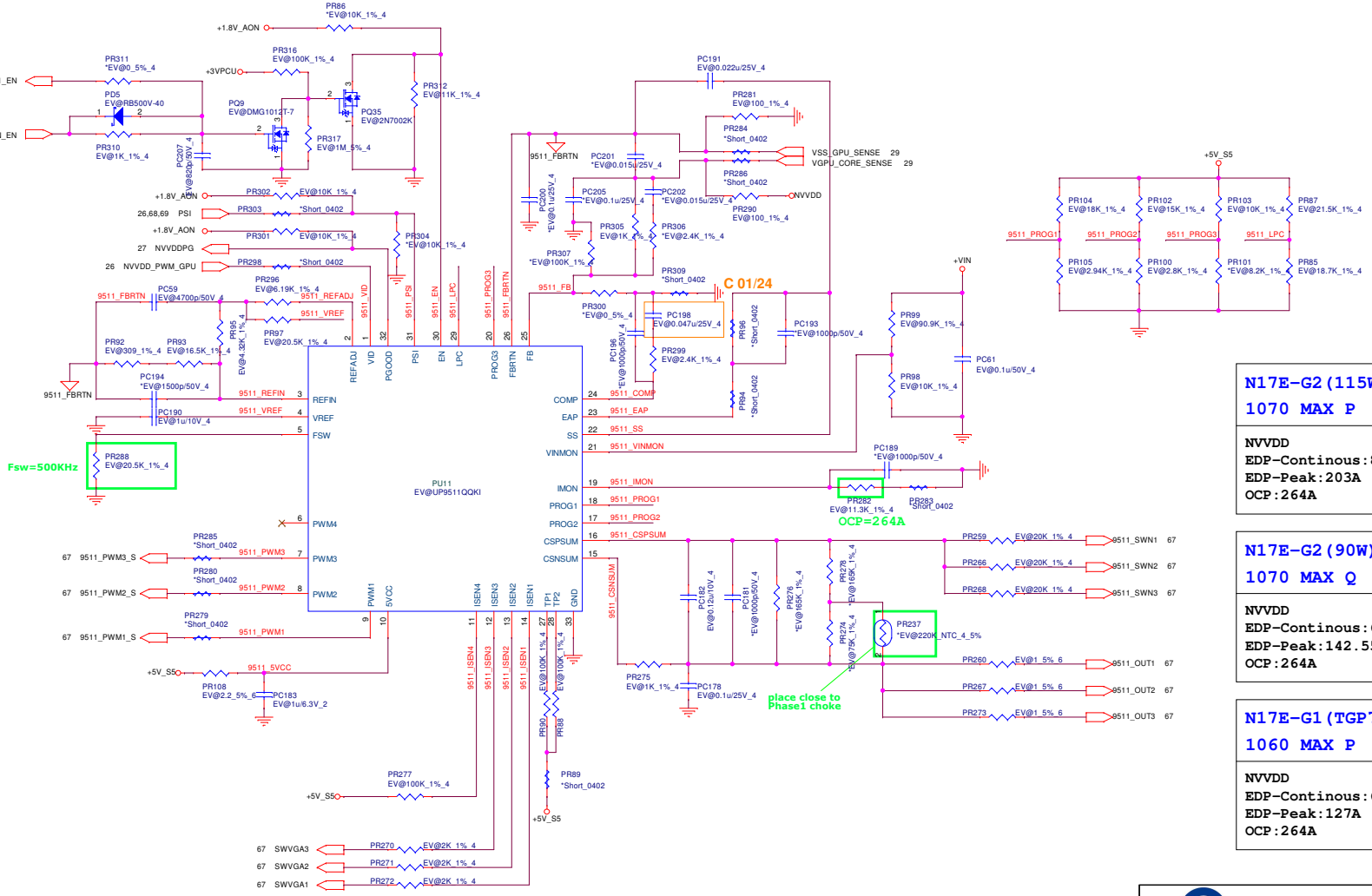
Discharge Circuit For +Vin_Panel



Quanta Computer Inc.			
PROJECT : ZGQ			
Size	Document Number		Rev
	LED Panel (TPS61087)		1A
Date: Monday, March 12, 2018		Sheet 65 of 73	

VGA Core – NVVDD/NVDDS

+VIN 35,44,57,58,59,60,61,62,63,64,65,69,71
NVVDD 29,67
+5V_S5 41,50,52,53,56,58,60,61,62,63,65,67,68,69,71
+1.8V_AON 21,24,25,26,27,28,68,69,71
+3VPCU 9,10,12,14,16,35,38,40,44,49,51,53,55,57,58,64



N17E-G2(115W)
1070 MAX P

NVVDD
EDP-Continous:85A
EDP-Peak:203A
OCP:264A

N17E-G2(90W)
1070 MAX Q

NVVDD
EDP-Continous:66.12A
EDP-Peak:142.55A
OCP:264A

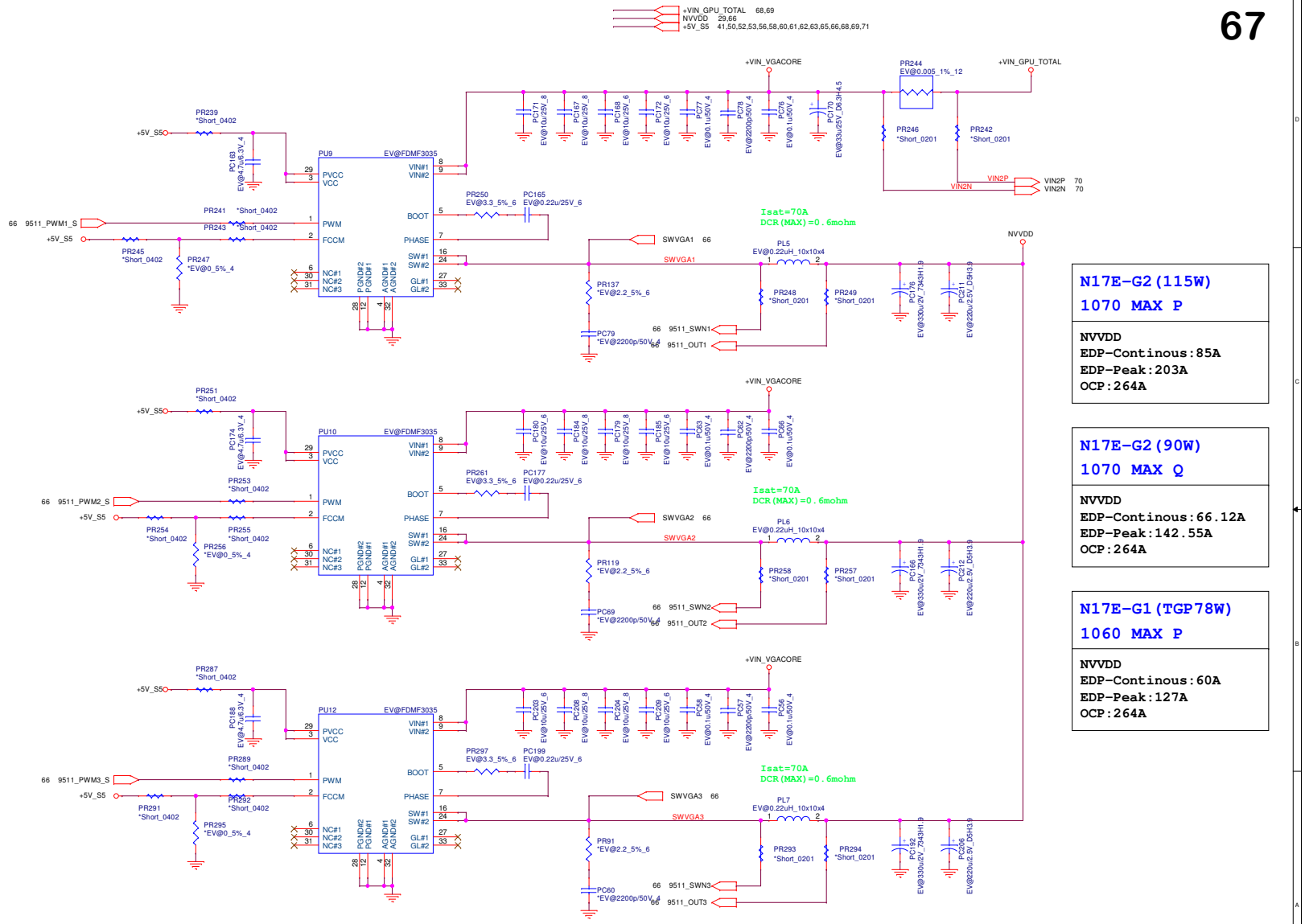
N17E-G1(TGP78W)
1060 MAX P

NVVDD
EDP-Continous:60A
EDP-Peak:127A
OCP:264A

Quanta Computer Inc.
PROJECT : ZGQ

Size	Document Number	Rev
	+VGPU (uP9511QQKI)	1A

Date: Monday, March 12, 2018 Sheet 66 of 73



N17E-G2(115W)
1070 MAX P

NVVDD
EDP-Continous:85A
EDP-Peak:203A
OCP:264A

N17E-G2(90W)
1070 MAX Q

NVVDD
EDP-Continous:66.12A
EDP-Peak:142.55A
OCP:264A

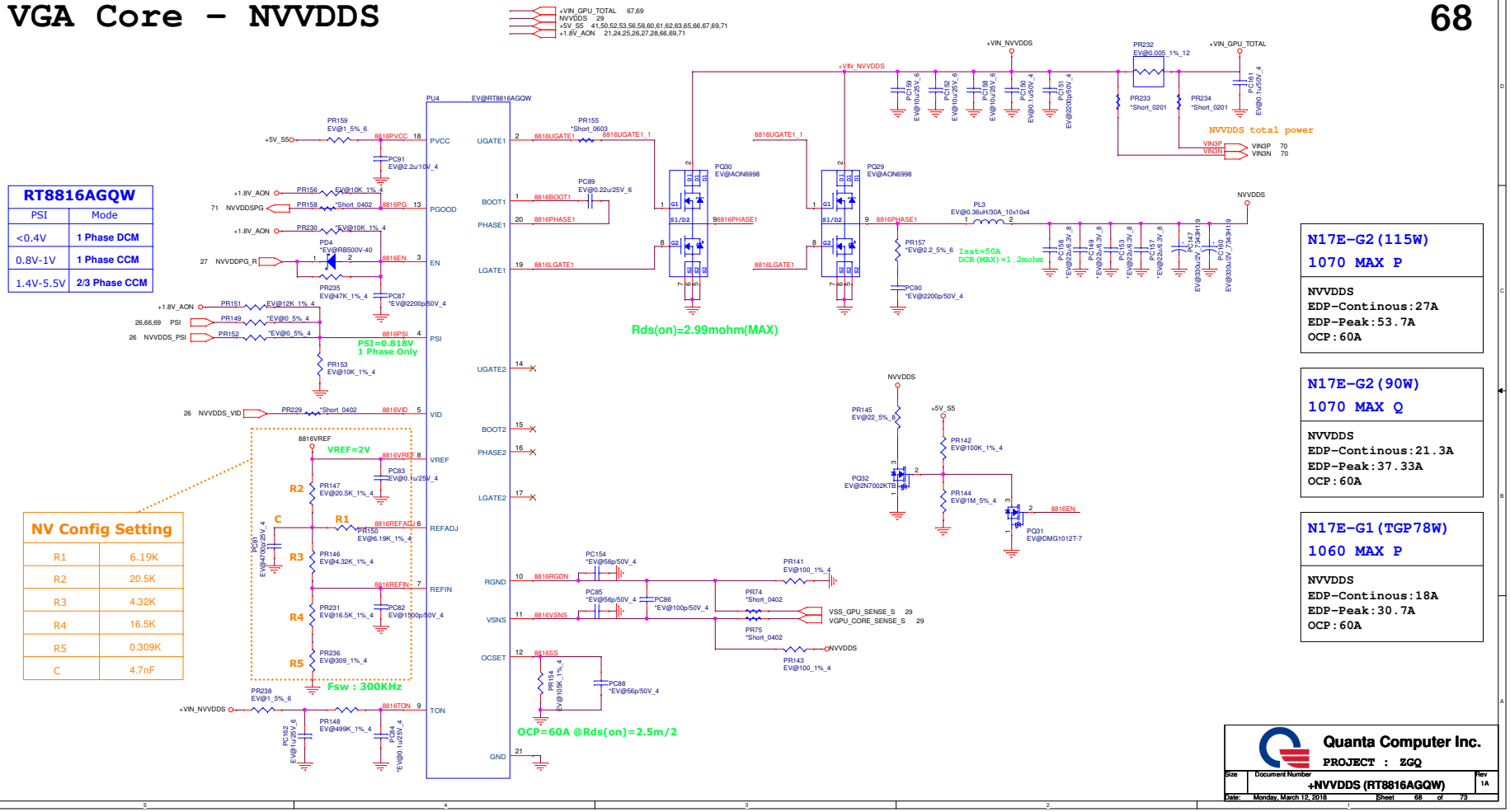
N17E-G1(TGP78W)
1060 MAX P

NVVDD
EDP-Continous:60A
EDP-Peak:127A
OCP:264A

Quanta Computer Inc.
PROJECT : ZGQ

Size	Document Number	Rev
	+VGPU (uP9511QQKI)	1A
Date: Monday, March 12, 2018	Sheet 67 of 73	

VGA Core – NVVDDS



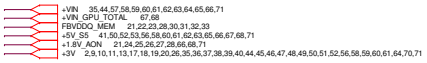
Quanta Computer Inc.

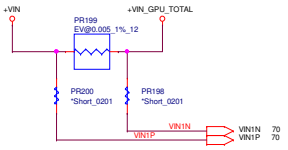
PROJECT : ZGQ

Size	Document Number	Rev
	+NVVDDS (RT8816AGQW)	1A

Date: Monday, March 12, 2018 Sheet 68 of 73

VGA Core - FBVDDQ_MEM

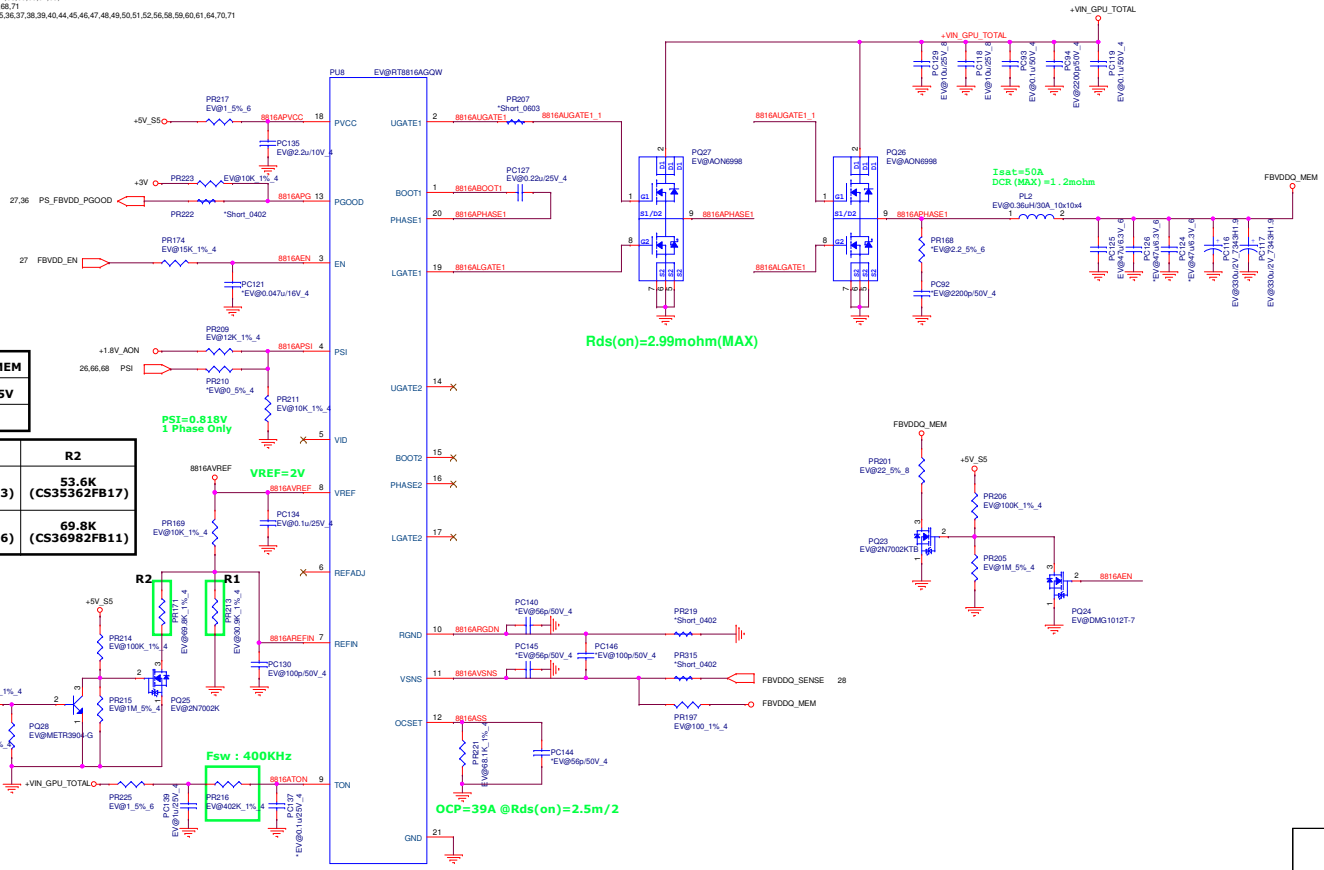




RT8816AGQW	
PSI	Mode
<0.4V	1 Phase DCM
0.8V-1V	1 Phase CCM
1.4V-5.5V	2/3 Phase CCM

MEM_VDD_CTRL	FBVDDQ_MEM
1	1.55V/1.5V
0	1.35V

FBVDDQ_MEM	R1	R2
1.55V	35.7K (CS33572FB13)	53.6K (CS35362FB17)
1.5V	30.9K (CS33092FB06)	69.8K (CS36982FB11)



N17E-G2(115W)
1070 MAX P
FBVDDQ_MEM EDP-Continous:25A EDP-Peak:30.6A OCP:39A

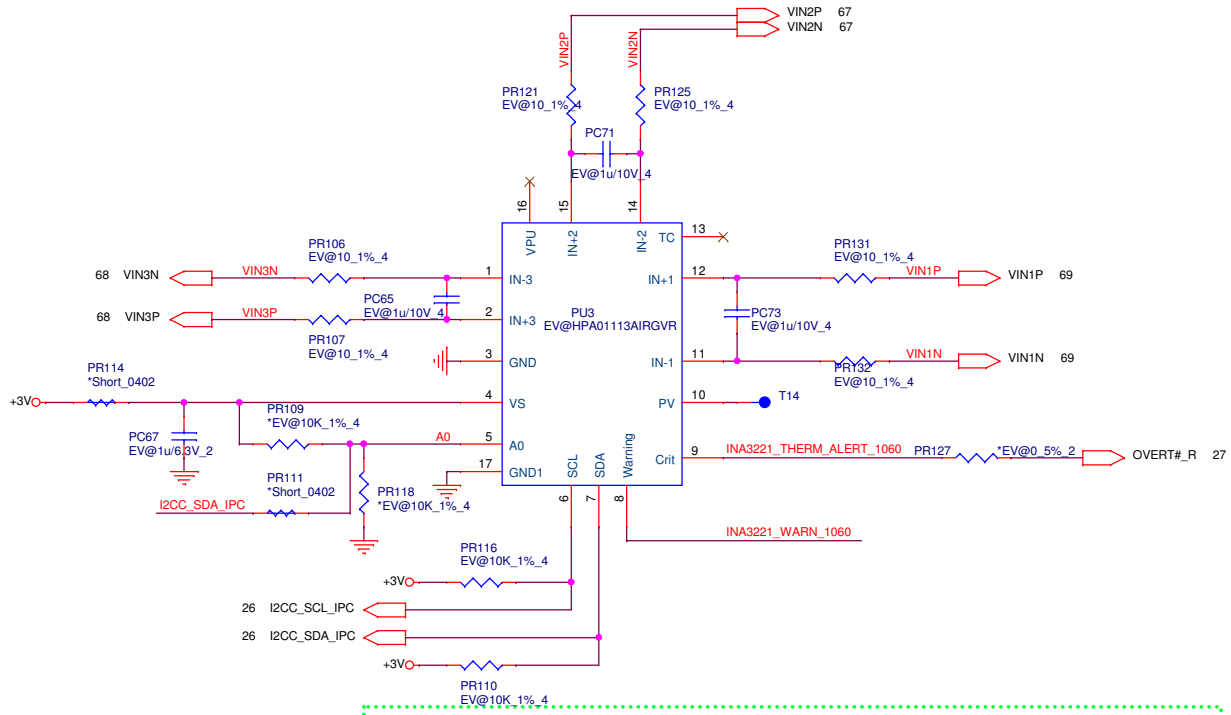
N17E-G2(90W)
1070 MAX Q
FBVDDQ_MEM EDP-Continous:25A EDP-Peak:30.6A OCP:39A

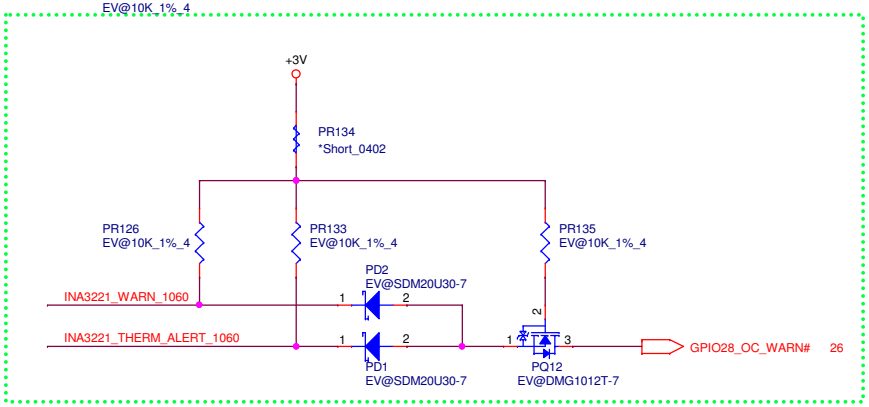
N17E-G1(TGP78W)
1060 MAX P
FBVDDQ_MEM EDP-Continous:19.8A EDP-Peak:32.2A OCP:39A

Quanta Computer Inc.
PROJECT : ZGQ

Size	Document Number	Rev
	+FBVDDQ_MEM (RT8816AGQW)	1A
Date: Monday, March 12, 2018	Sheet 69 of 73	

+3V 2,9,10,11,13,17,18,19,20,26,35,36,37,38,39,40,44,45,46,47,48,49,50,51,52,56,58,59,60,61,64,69,71





Request from Nvidia

Quanta Computer Inc.

PROJECT : ZGQ

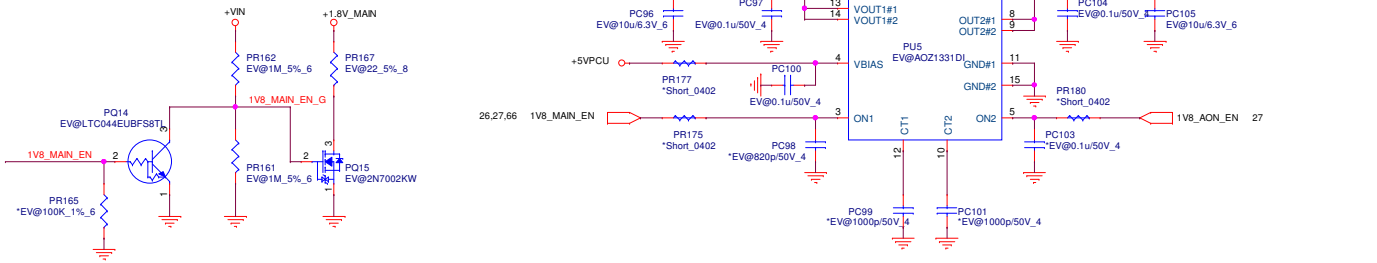
Size	Document Number	Rev
	Current Sense	1A
Date: Monday, March 12, 2018	Sheet 70 of 73	

+1.8V_S5 14,56,64
+1.8V_MAIN 21,27,28,37
+1.8V_AON 21,24,25,26,27,28,66,68,69
+5VPCU 10,41,43,44,51,53,58,59

TDC : 0.08A
PEAK : 0.1A
Width : 20mil

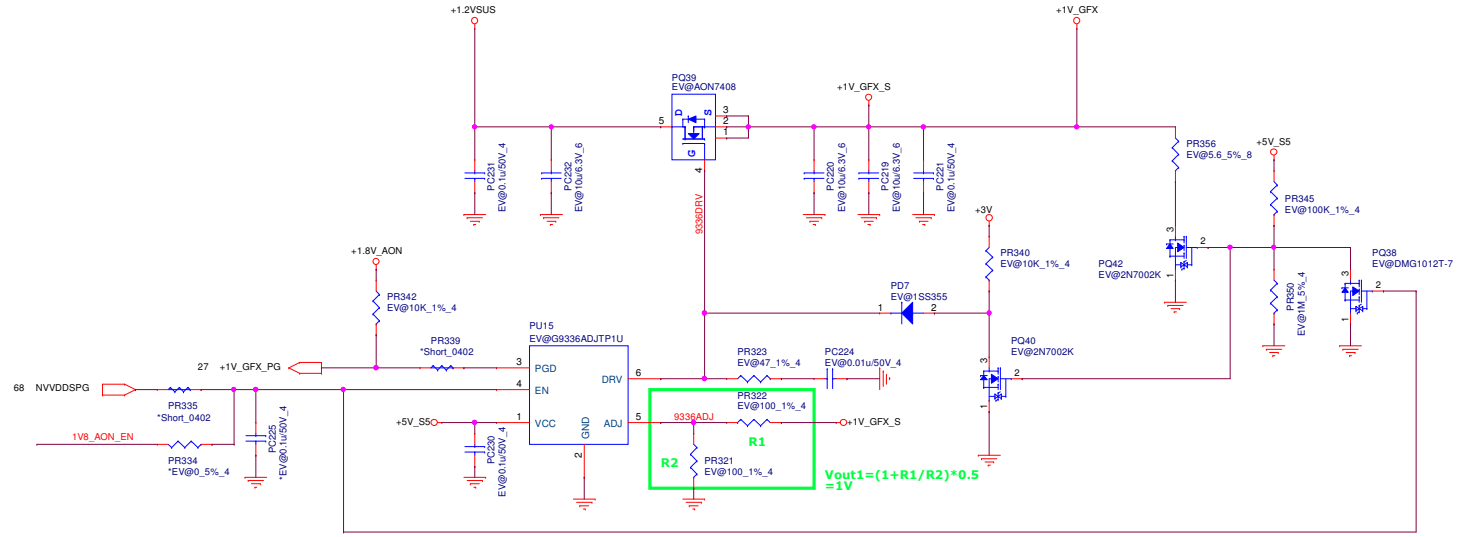
C2 0202

TDC : 2.21A
PEAK : 2.95A
Width : 100mil

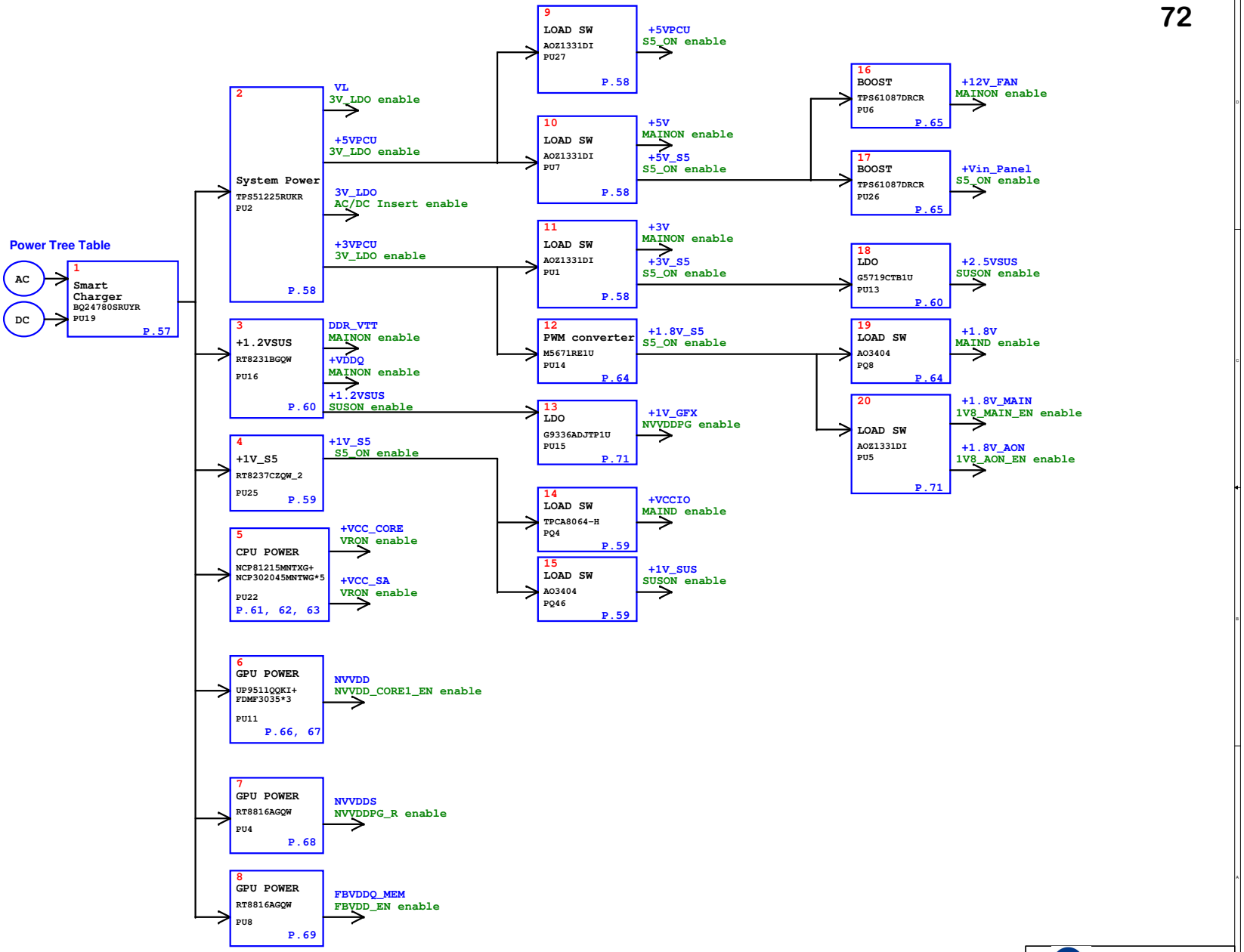


+1.2VSUS 2,6,10,14,17,18,19,20,60
+1V_GFX 21,24
+5V_S5 41,50,52,53,56,58,60,61,62,63,65,66,67,68,69
+3V 2,9,10,11,13,17,18,19,20,26,35,36,37,38,39,40,44,45,46,47,48,49,50,51,52,56,58,59,60,61,64,69,70

TDC : 1.52A
PEAK : 2.02A
Width : 80mil



Quanta Computer Inc.		
PROJECT : ZGQ		
Size	Document Number: +1.8V_AON (AOZ1331DI)	Rev: 1A
Date: Monday, March 12, 2018	Sheet 71 of 73	



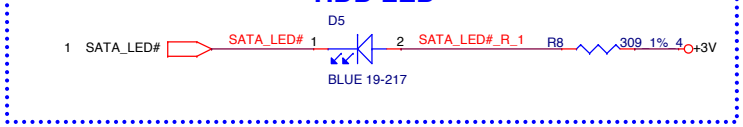
Quanta Computer Inc.
PROJECT : ZGQ
Size | Document Number: POWER TREE TABLE | Rev: 1A
Date: Monday, March 12, 2018 | Sheet 72 of 73

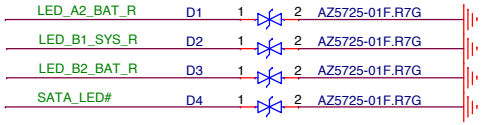
Model	Date	CHANGE LIST
ZGQ REV:A	8/29	1. FIRST RELEASED
ZGQ REV:B	9/20	1.page8 stuff R827 and R826 follow CRB 2.page9/46 change to BT to Port14 for CNVi 3.page10 stuff R998 and R999 for BOM issue , mirror CON3 to correct pin defined 4.page11 Del unnecessary parts,C1216,C1218,C1219,C1210,C1209,C1212,C1212,C1213,C1215,C1228,C1229,C1226,C1227,C1235,C1237,C1230,C1234,R586,R592 and net PLT_ID2 5.page14 stuff R322 for internal LDO1.8V mode 6.page20 unstuff R507,R486 and stuff R495,R503 for DIMM B1 identify issue 7.page26 change to GPIO15 for Nvidia GPIO table 8.page57-72 update power circuit 9/20 9.page35 MIC_VCC change to 3.3V
	9/22	1.page52 LED Keyboard N-MOS type change N-MOS type to P-MOS 9/21 to P-MOS
	9/25	1.page39/40 update TBT P/N to AJSLLSN0U04 2.page26 correct VGA GPIO15 and GPIO18 3.page62 change PC327 to 0603 size 4.page41 Modify TBT3 PD control circuit 5.page47/48 update CN20/CN23 footrpint and P/N 6.page53 update CN16/CN11/CN8 footrpint and P/N
	9/26	1.page56 Change I/O board pin defined and connector to 44pin 2.page36 chnage U9 EN pin to +3V 3.page60 DEL PJ14
	9/29	1.page10/11/46 Modify CNVi circuit for Intel checklist
	10/03	1.page12 change U26 footprint name to soic8-7_9-1_27 2.page50 Add R1210 for XBOX RSEST 3.page46 Add R1211 for CNVi 4.page57-72 update power circuit
	10/05	1.page50 Mirror CN10 pin defined 2.Add cap for ESD sensitive Nets 3.page57-72 update power circuit 4.page11/46 Add R1214/R1212/R1216/R1217 for CNVi BT
	10/13	1.page45 Add 4 VGA Shrapnel 2.page57-72 update power circuit 3.page43 update USB connector P/N and footprint
	10/16	1.page39 Add PD for TBT2_DP_HPD 2.page55 change crystal cap from 10p to 15p 3.page27 change crystal cap from 18p to 12p 4.page45 change U17 Pin16~Pin20 to GND and Modify Hole
	10/17	1.page45 Del SPAD17 and modify Hole13~19 2.page58 Change PR224 from input to output for +5V_S5,Change PR218 from input to output for +5V,Change PR80 from input to output for +3V_S5, Change PR78 from input to output for +3V and Change PR494 from input to output for +5V_S5_TYPEC
	10/18	1.page13 Add R1219 for intel#571006 2.page10 Add R1220,R1221 and Q102 for CNVi intel#571006
	10/19	1.page10 Modify level shift circuit for CNVi 2.page49 Change SW3 P/N 3.page54 Change CN22 P/N
	10/20	1.page39 correct the WAKE circuit for TBT 2.page10/11 change HRESET to 1.8V GPP_J10 3.page53 change LED resistor to 2.2 ohm 4.page16 connect NBSWON# to APS connector
	10/21	1.page36 change DP connector footprint
	10/24	1.page41 TI suggest RPD_G1/RPD_G2 to GND directly 2.page49 Change R364 and R351 to 100K ohm for S5 leakage
	10/25	1.BOM update
ZGQ REV:C	11/15	1.page14 change VCCDSW to +3V_DEEP_SUS for S5 leakage 2.page9/41 change Typec USB2.0 to PD control
	11/29	1.BOM update 2.page13/39 stuff R331 and D74 ,unstuff R1087 and R1089 for TBT PLUG EVENT
	11/30	1.page49 U23 pin 122 change to ADP_Board_ID and DDR4_SUSON_2V5 move to pin126
	12/01	1.page49 Add R1233 for DFM REVIEW
	12/04	1.page9 Remove Resistor of Typec USB2.0 for layout 2.page1-8 change CPU footprint to bga1440-intel-crl-h
	12/05	1.page9/41 change USB2.0 directly from PCH to Typec connector
	12/07	1.BOM update
ZGQ REV:D	12/08	1.page27 change Y4 cap to 10P for vendor request 2.page53 Stuff C551,C669,C603,C641,C521 and C531 for KB ESD
	12/19	1.page11 Add D99 for ESD
	12/25	1.page55 Add circuit for EMI
	12/26	1.Change some 0ohm to short pad 2.Change WiFi nuts to MBXK5001010 for ME
	12/29	1.update BOM 2.update the Block Diagram 3.page2 Add C1396 for Acer requrest 4.page35 Add R1246/R1247/C1394/C1395 for Acer requrest 5.page14 Correct TBT USB2.0
	01/05	1.stuff 47u at C709,C653,C652,C656,C628,C614,C618,C630 for VGA
	01/10	1.page39 stuff R1085 and unstuff R1231 for TBT_WAKE#
	01/25	1.page62 Change PL13, PL14, PL16, PL17 to CV+22^0MZ17 (panasonic) for EMI issue. 2.page66 Change PC198 to CH3474K1B04 (0.047U 25V +-10% X7R 0402) for system hang up
ZGQ REV:E	02/01	1.page49 modify R364 to 10K ohm for boot issue and unstuff R351 for cost down 2.page9/11/39/48 Swap PCIE port between TBT3 and PICE SSD2 for PCIE RAID issue 3.page57 Reserve PR497 and PR498 for battery 3S1P test
	02/02	1.Change some 0ohm to short pad
	02/05	1.page10 change CON3 footprint to bat-aaa-bat-046-k03-2p-smt 2.Change 0 ohm to short pad: PR490, PR187, PR72, PR78, PR422
	02/07	1.page65 change PR10 and PR190 from short pad to 0 ohm
	02/09	1.page65 change PU6 and PU26 from AL061087000 to AL061087001
ZGQ REV:F	03/02	1.page37 HDMI series resistor change to 10 ohm for impdeance 2.page54 change CN22 to DFFC16FR018 for SMT
	03/05	1.page35 Add C1402 and C1403 for EMI 2.page44 change C919 and C920 to 33p for EMI 3.page10/44 change C1008 and C1207 to 47p for EMI
	03/06	1.page49 modify R1230 PD resistor to 4.7K for ADP issue 2.page44 change C919 and C920 to 47p for EMI
	03/07	1.page45 Add SPR1 and SPR2 for EMI 1.page57 Reserve PR500 & PR499 for 3S1P plug out issue
	03/12	1.page45 Add SPR1 and SPR2 for EMI

Quanta Computer Inc.
PROJECT : ZGQ
Change list

update P/N & footprint 8/8

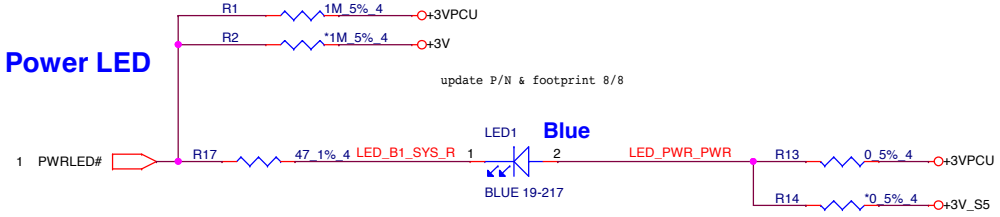
HDD LED

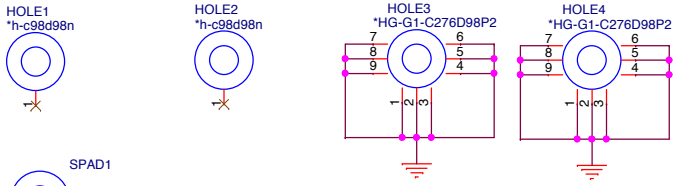


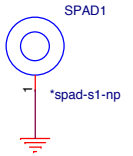


Power LED

update P/N & footprint 8/8



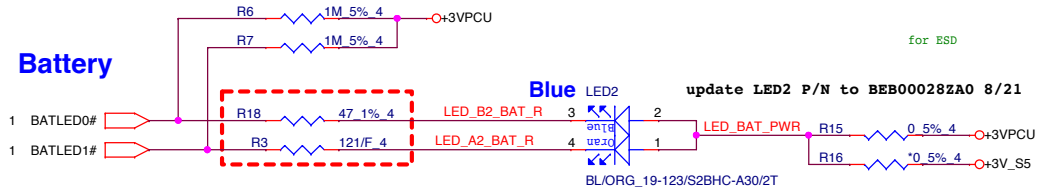




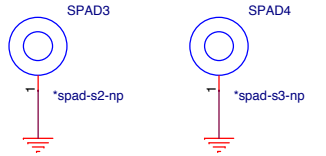
Battery

for ESD

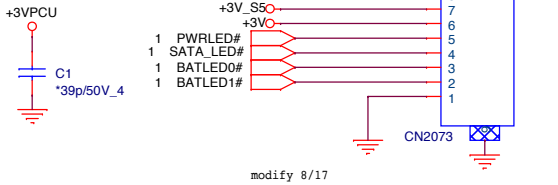
update LED2 P/N to BEB00028ZA0 8/21



Orange



Mirror to MB 51619-0080N-001



modify 8/17

Quanta Computer Inc. PROJECT : ZGQ		
Size	Document Number: ZGQ LED Board	Rev: 1A
Date: Tuesday, December 26, 2017	Sheet 1 of 2	

Model	Date	CHANGE LIST
ZGQ REV:A	8/29	1. FIRST RELEASED
ZGQ REV:B	10/17	1.page1 Unstuff D1,D2,D3 and D4
	11/28	1.page1 Change Resistor from 0603 to 0402
	11/29	1.page1 Del SPAD2
	12/05	1.page1 stuff D1,D2,D3 and D4
	12/26	1.page1 change SPAD4 for ESD

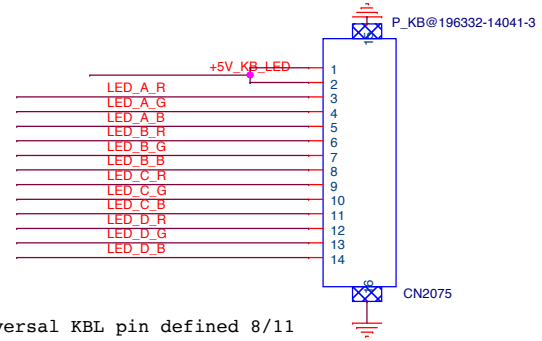
Quanta Computer Inc.
PROJECT : ZGQ

Size	Document Number	Rev
	Change list	1A

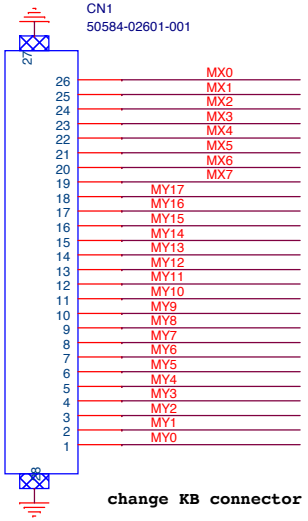
Date: Tuesday, December 26, 2017 Sheet 2 of 2

update CN2075 P/N 10/18

update CN2075 P/N and footprint 10/12

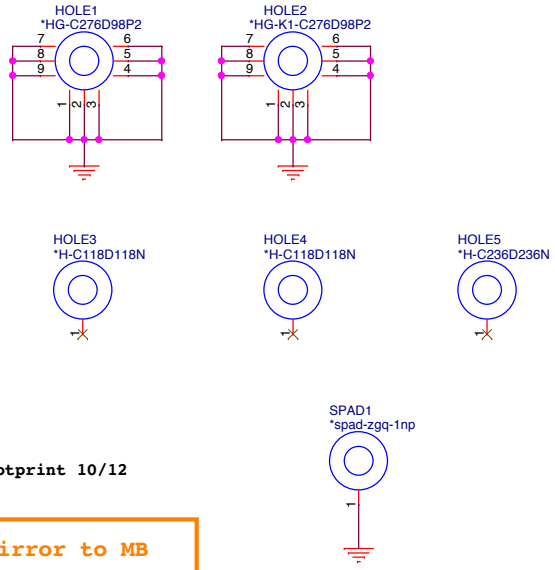


reversal KBL pin defined 8/11

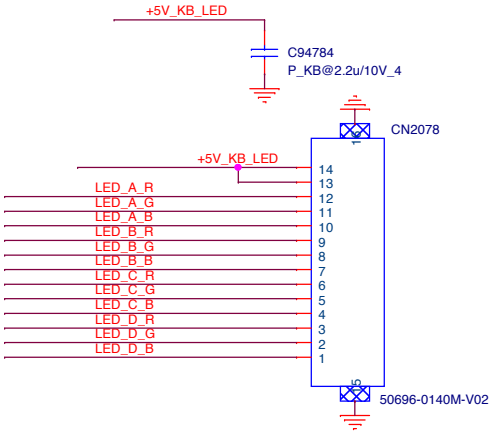


change KB connector P/N and footprint 10/12

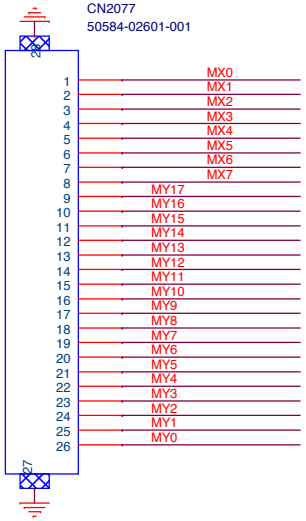
change KB connector P/N 10/18



Mirror to MB



reversal KBL pin defined 8/11



Quanta Computer Inc.

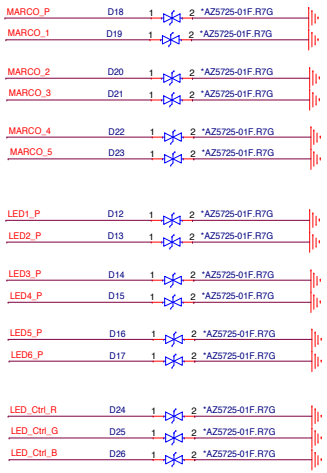
PROJECT : ZGQ

Size	Document Number	Rev
	ZGQ KB TRAS\B	1A
Date: Friday, October 20, 2017	Sheet 1 of 2	

Model	Date	CHANGE LIST
ZGQ REV:A	8/29	1. FIRST RELEASED
ZGQ REV:B	10/16	1.page1 change CN1,CN2077,CN2075 P/N and footprint
	10/17	1.page1 Add SPAD1
	10/20	1.page1 change SPAD1 footprint

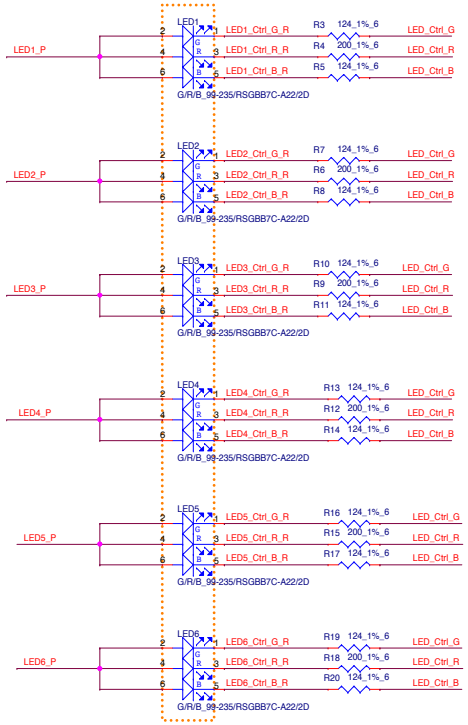
Quanta Computer Inc.
PROJECT : ZGQ

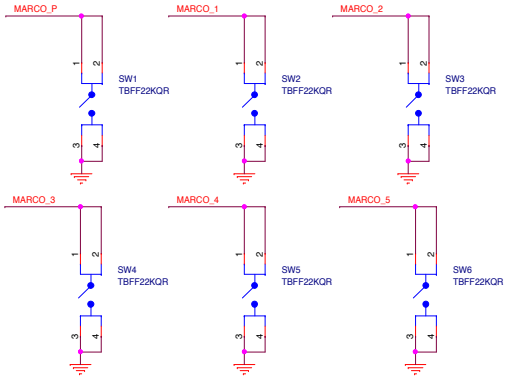
Size	Document Number	Rev
	Change list	1A
Date: Friday, October 20, 2017	Sheet 2 of 2	



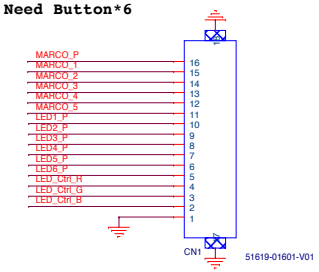
Add LED10/12

Modify cirucit 10/18



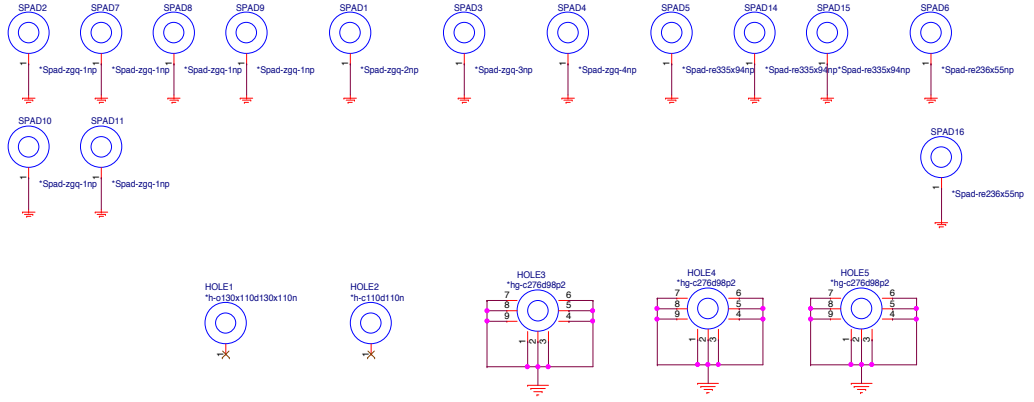


Need Button*6



update Connector P/N 10/18

Hole

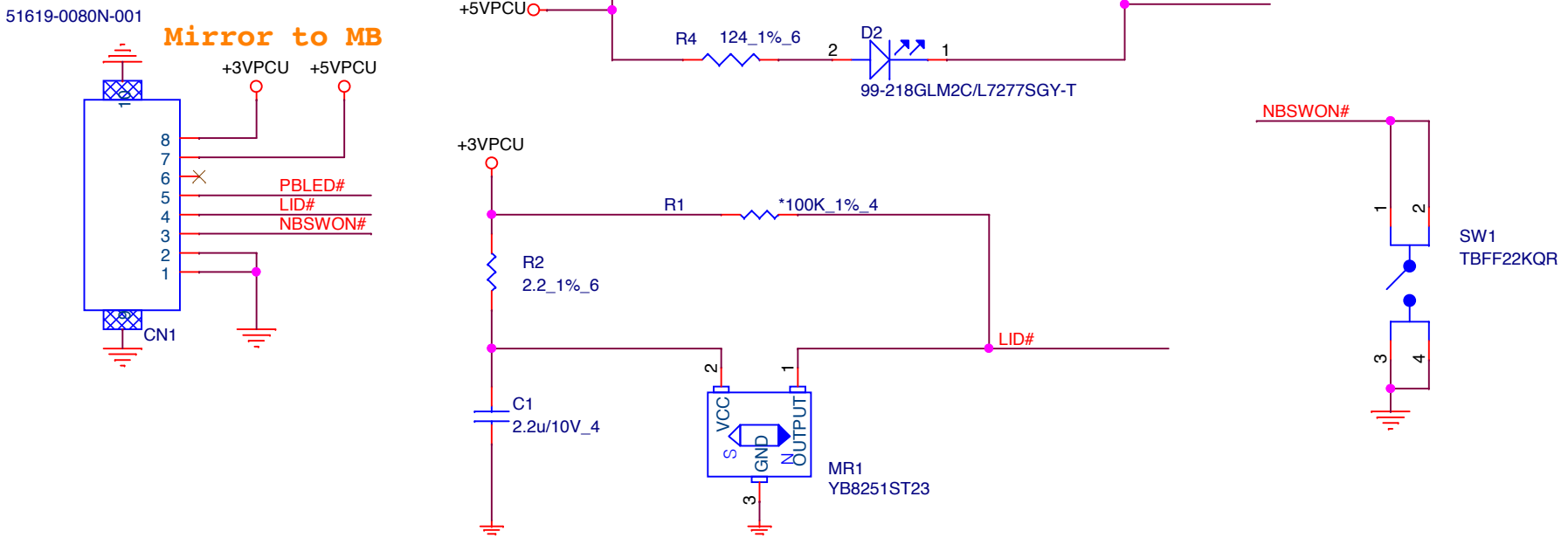


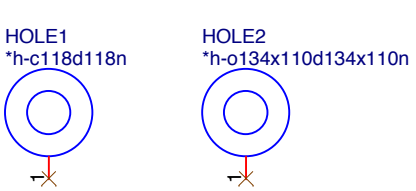
Quanta Computer Inc.		
PROJECT : ZGQ/ZGX		
Size	Document Number: Cayman Marco Key Board	Rev 1A
Date: Thursday, December 28, 2017	Sheet 1 of 2	

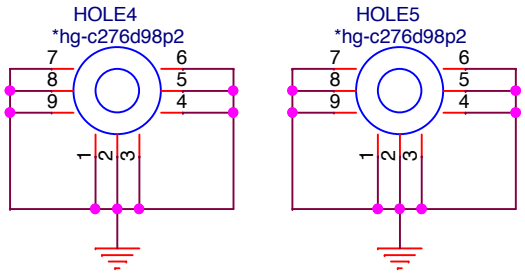
Model	Date	CHANGE LIST
ZGQ REV:A	8/29	1. FIRST RELEASED
ZGQ REV:B	10/18	1.page1 Modify LED circuit
	10/19	1.page1 Modify Hole
	10/20	1.page1 Modify Hole
ZGQ REV:C	12/26	1.Remove LED7-12 circuit for ME

Quanta Computer Inc.
PROJECT : ZGQ

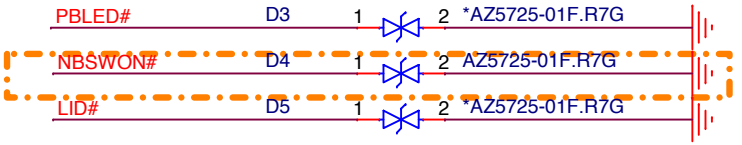
Size	Document Number	Rev
	Change list	1A
Date: Thursday, December 28, 2017	Sheet 2 of 2	

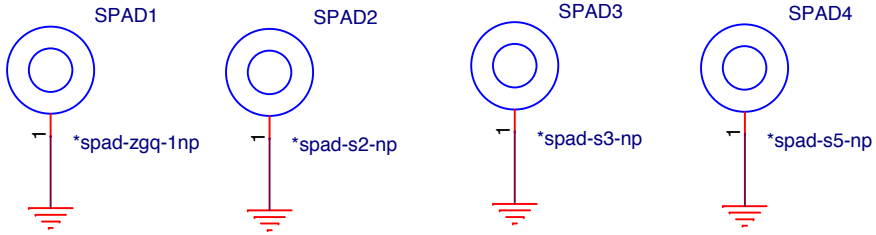






stuff D4 for ZGX ESD 12/29





Quanta Computer Inc.

PROJECT : ZGQ

Size	Document Number	Rev
	Cayman Power Board	1A
Date: Friday, December 29, 2017	Sheet 1 of 1	

Model	Date	CHANGE LIST
ZGQ REV:A	8/29	1. FIRST RELEASED
ZGQ REV:B	10/18	1.page1 Modify LED circuit
	10/20	1.page1 Modify Hole
ZGQ REV:C	12/27	1.page1 Del Hole3
	12/29	1.page1 stuff D4 for ZGX ESD

Quanta Computer Inc.
PROJECT : ZGQ

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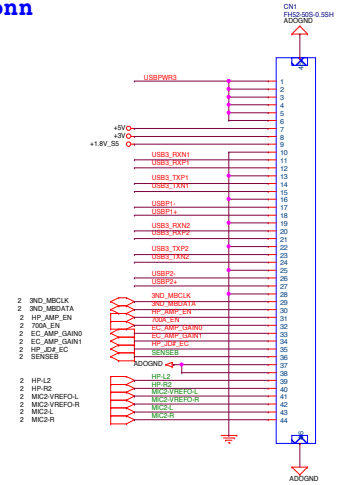
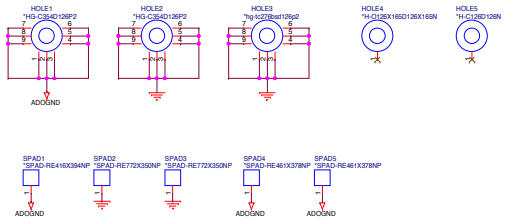
Audio/USB Board Conn

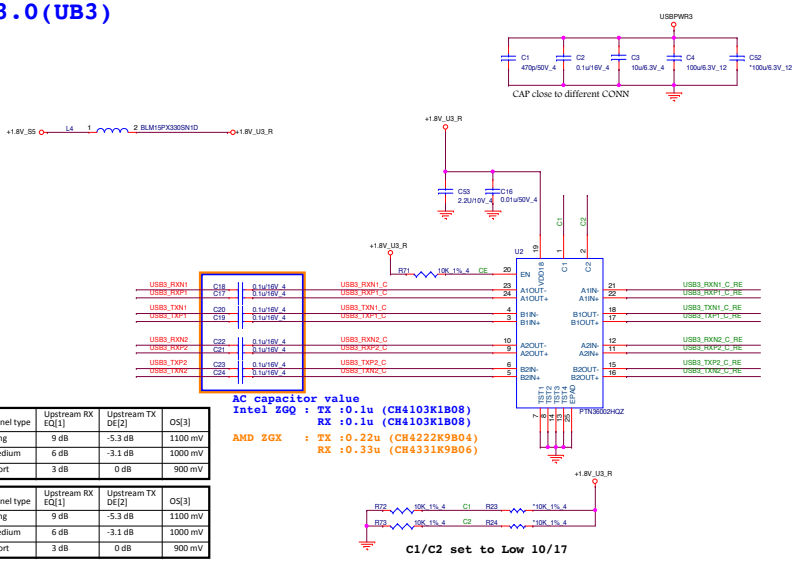


change IO connector P/N and footprint 10/12

Hole (OTH)



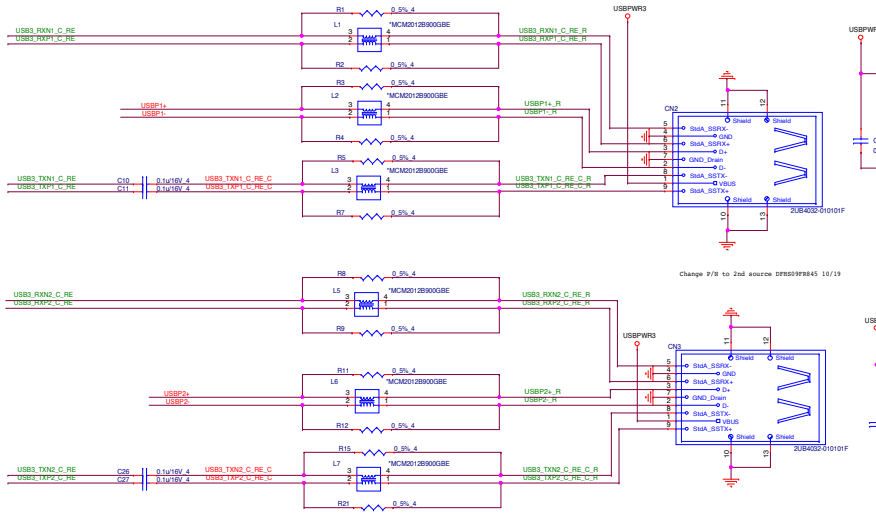
USB 3.0(UB3)

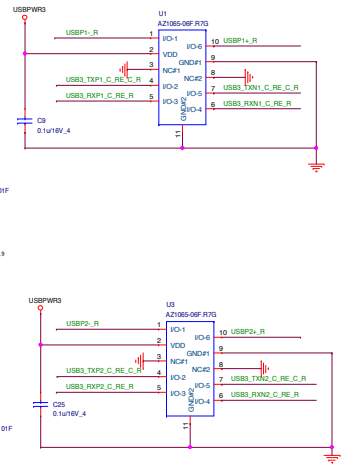


C1 State	Channel type	Upstream RX EQ[1]	Upstream TX DE[2]	OS[3]
HIGH	Long	9 dB	-5.3 dB	1100 mV
OPEN	Medium	6 dB	-3.1 dB	1000 mV
LOW	Short	3 dB	0 dB	900 mV

C2 State	Channel type	Upstream RX EQ[1]	Upstream TX DE[2]	OS[3]
HIGH	Long	9 dB	-5.3 dB	1100 mV
OPEN	Medium	6 dB	-3.1 dB	1000 mV
LOW	Short	3 dB	0 dB	900 mV

[1] EQ is the input receiver equalization gain
[2] DE is the transmit output signal de-emphasis gain
[3] OS is the transmit output differential voltage





Quanta Computer Inc.	
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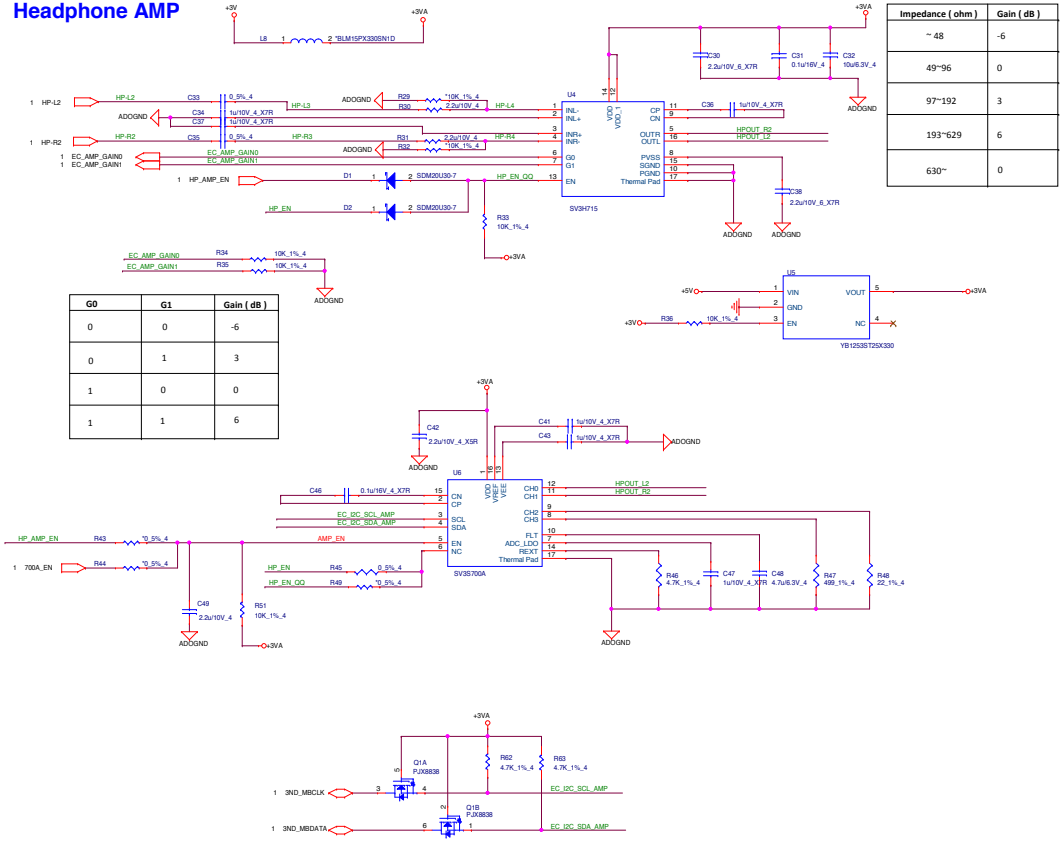
Headphone AMP

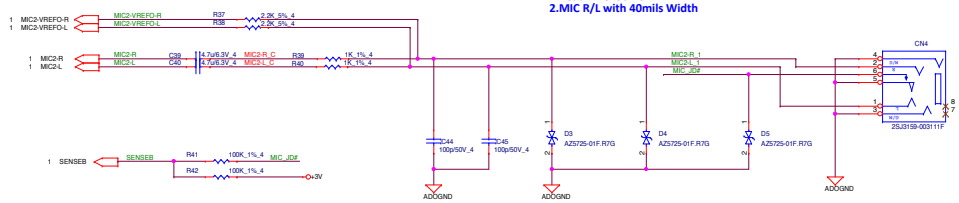


Impedance (ohm)	Gain (dB)
~ 48	-6
49~96	0
97~192	3
193~629	6
630~	0

G0	G1	Gain (dB)
0	0	-6
0	1	3
1	0	0
1	1	6

MIC

1.Bead RDC<30mohm
2.MIC R/L with 40mils Width

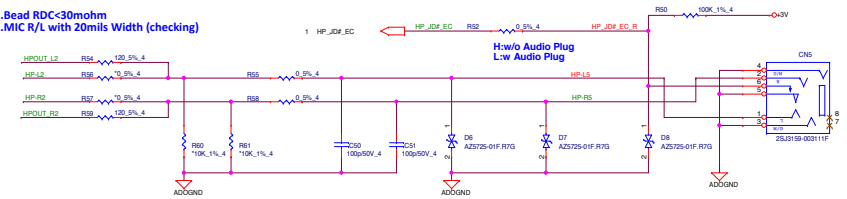


change Audio jack P/N and footprint

H.P

1.Bead RDC<30mohm
2.MIC R/L with 20mils Width (checking)

H:w/o Audio Plug
L:w Audio Plug



Quanta Computer Inc.			
PROJECT : ZGQ			
Size	Document Number		Rev
	Azalia ALC299-CG,S-AMP		1A
Date: Thursday, January 25, 2018		Sheet 2 of 3	

Model	Date	CHANGE LIST
ZGQ REV:A	8/29	1. FIRST RELEASED
ZGQ REV:B	10/16	1.page1 change CN1 to 44 pin for cost down 2.page2 change CN4/CN5 P/N and footprint 3.Page1 change CN1 pin45/46 to AGND
	10/17	1.page1 stuff R72 and R73 for USB issue
ZGQ REV:C	10/17	1.page2 stuff R70 for EMI
	4/8	1. R54 and R59 change to 120R for S3 S4 Restart headset bobo issue. 2. C33 and C35 change to 0R for S3 S4 Restart headset bobo issue. 3. R30 and R31 change to 2.2U for S3 S4 Restart headset bobo issue. 4. R29 and R32 change to NC for S3 S4 Restart headset bobo issue. 5. R70 change to 0.1u for Headset have high frequency noise when system copy file copy file from LAN to USB.

Quanta Computer Inc.
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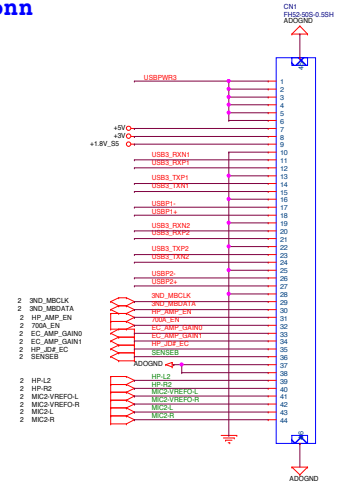
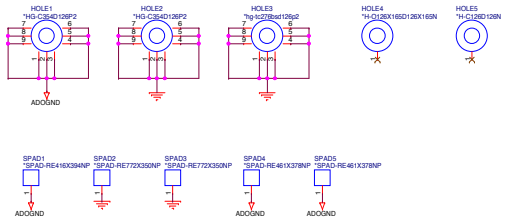
Audio/USB Board Conn

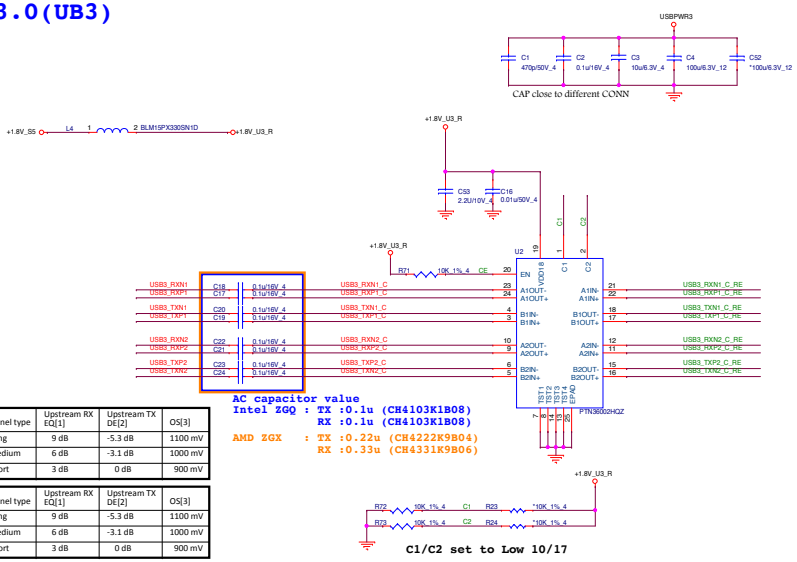


change IO connector P/N and footprint 10/12

Hole (OTH)



USB 3.0(UB3)



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C2 State	Channel type	Upstream RX EQ[1]	Upstream TX DE[2]	OS[3]
HIGH	Long	9 dB	-5.3 dB	1100 mV
OPEN	Medium	6 dB	-3.1 dB	1000 mV
LOW	Short	3 dB	0 dB	900 mV

[1] EQ is the input receiver equalization gain
[2] DE is the transmit output signal de-emphasis gain
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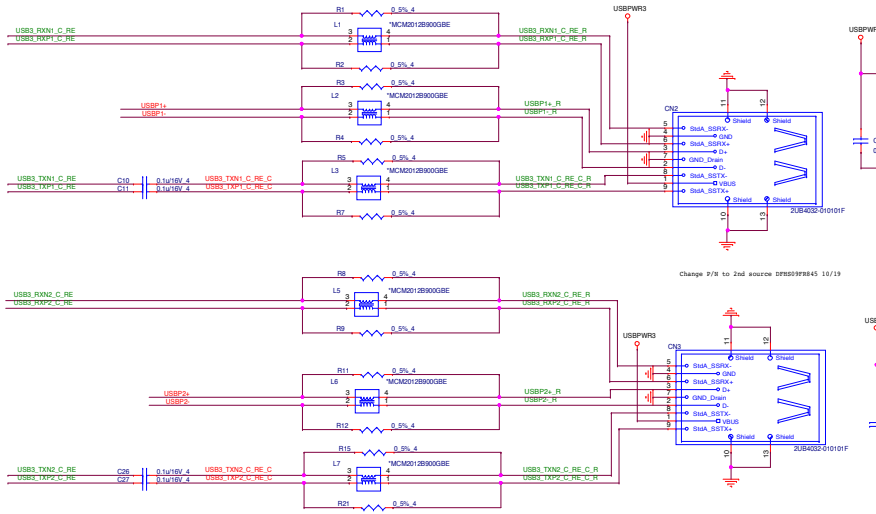

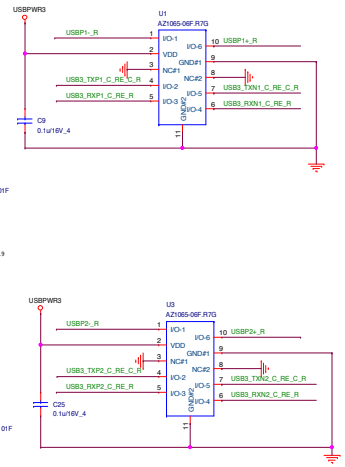

Quanta Computer Inc.	
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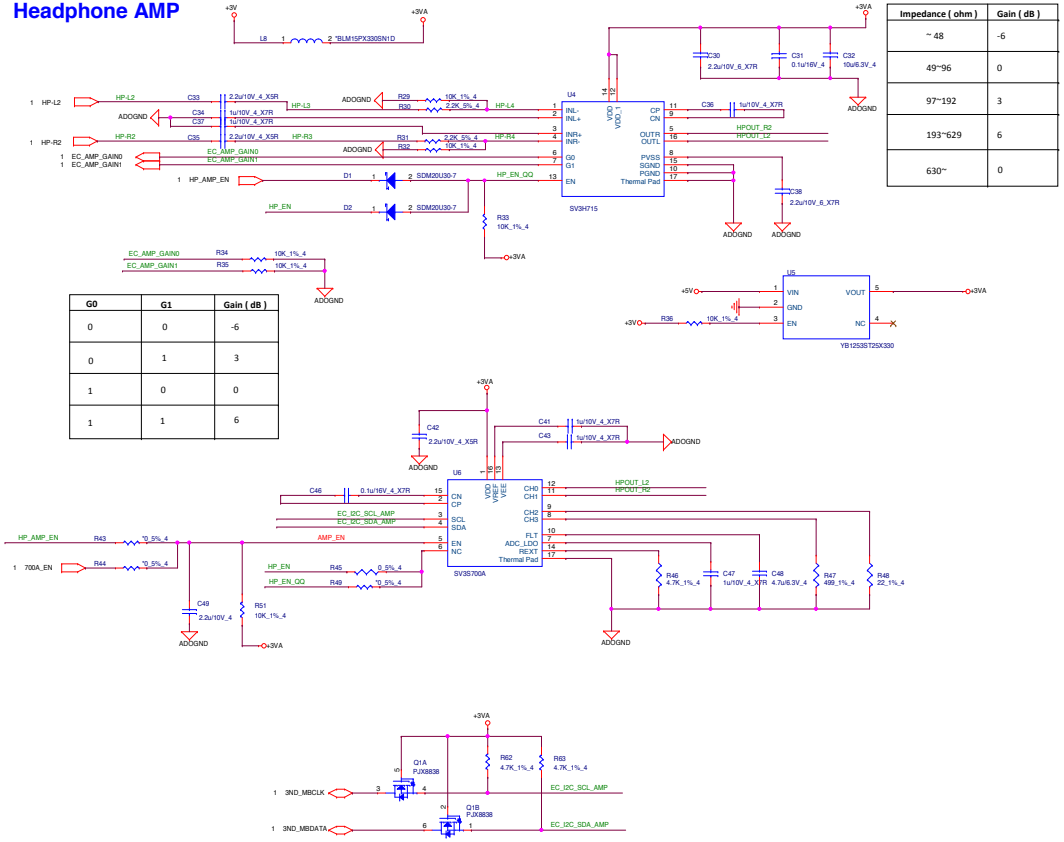
Headphone AMP



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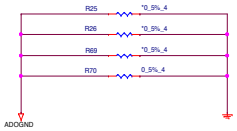
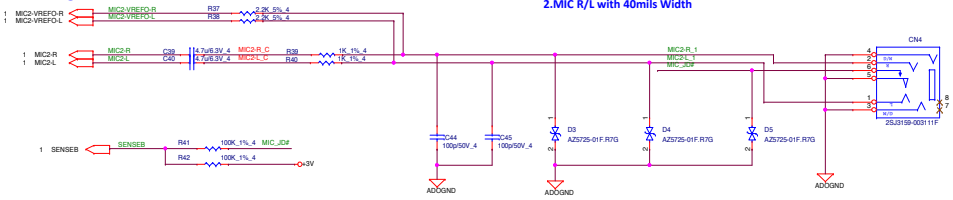


MIC

1.Bead RDC<30mohm
2.MIC R/L with 40mils Width

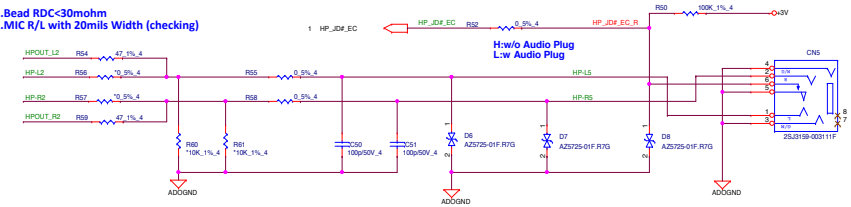


change Audio jack P/N and footprint

H.P

1.Bead RDC<30mohm
2.MIC R/L with 20mils Width (checking)

H:w/o Audio Plug
L:w Audio Plug



Quanta Computer Inc.			
PROJECT : ZGQ			
Size	Document Number		Rev
	Azalia ALC299-CG,S-AMP		1A
Date: Wednesday, December 27, 2017	Sheet 2 of 3		

Model	Date	CHANGE LIST
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Quanta Computer Inc.
PROJECT : ZGQ

Size	Document Number	Rev
	Change list	1A
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