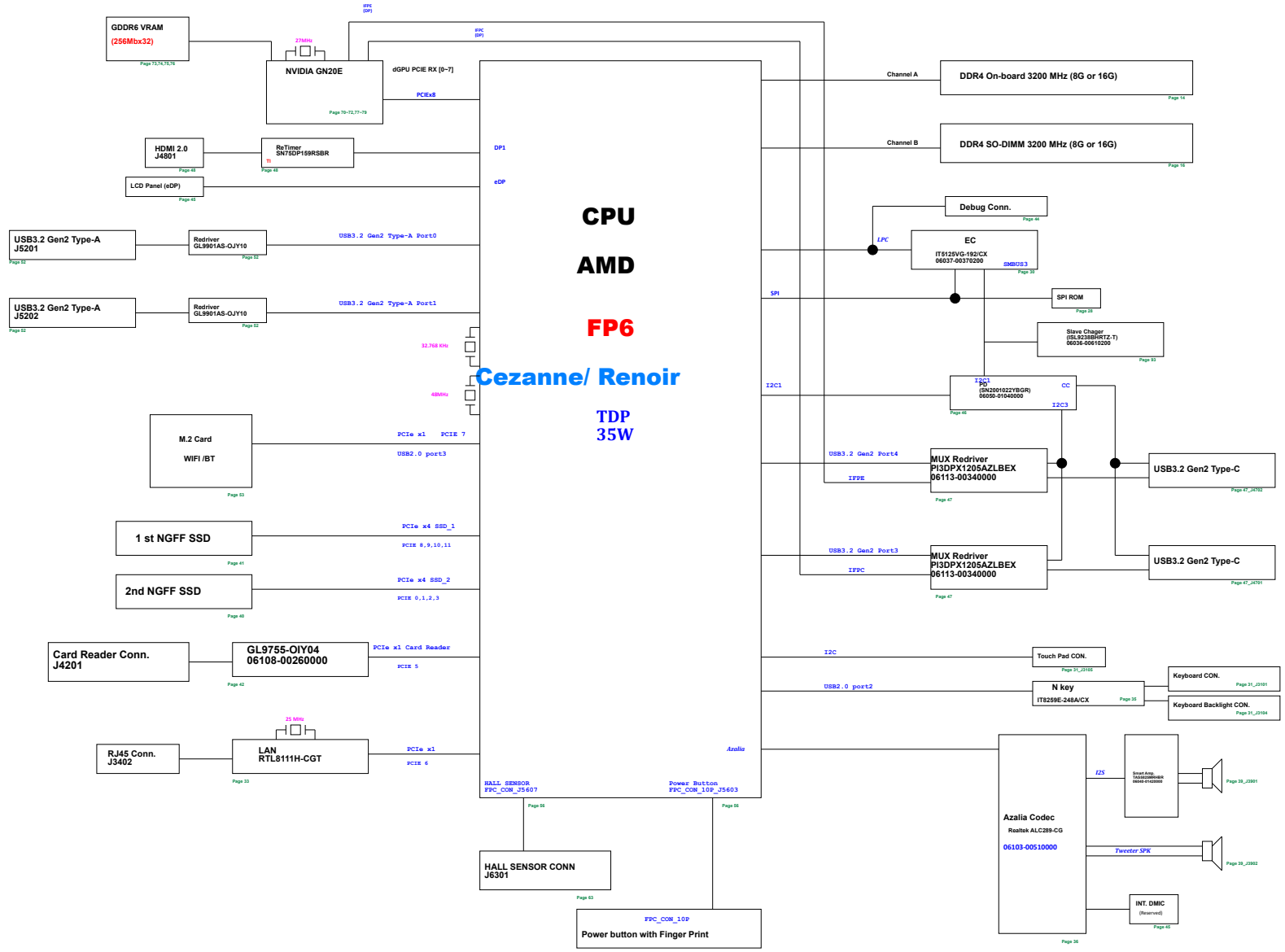
GA503QS AMD+NVIDIA Block Diagram

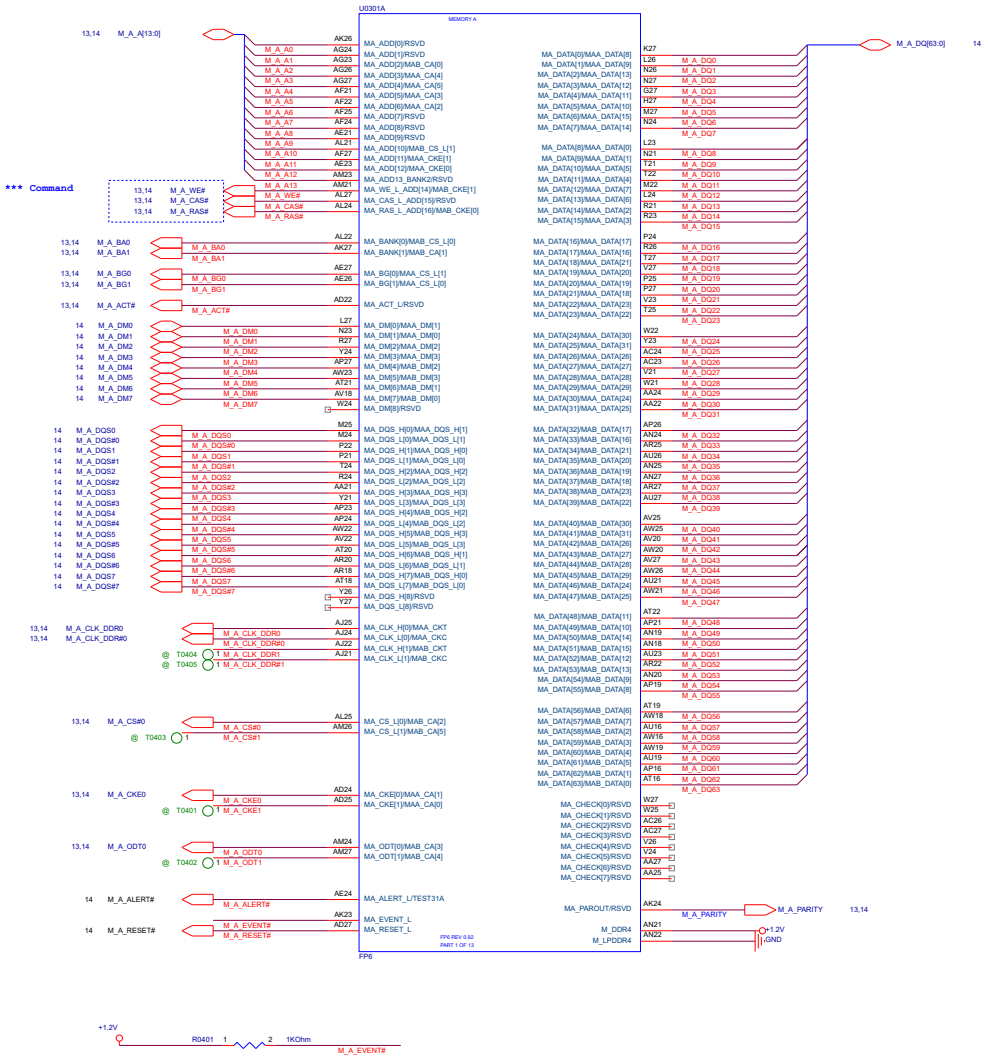


Project Name	GA503QS
Title	CFL-H_Block Diagram_R1.3B
Dept.	
Engineer	NB1 RD2 EE1
Date	Tuesday, October 15, 2019

Memory Channel A

On Board DDR4

MA/B_
I/O-IOMEM-S/D VDDIO_MEM_S3 (S0_1.2)_FP6 (FDS)

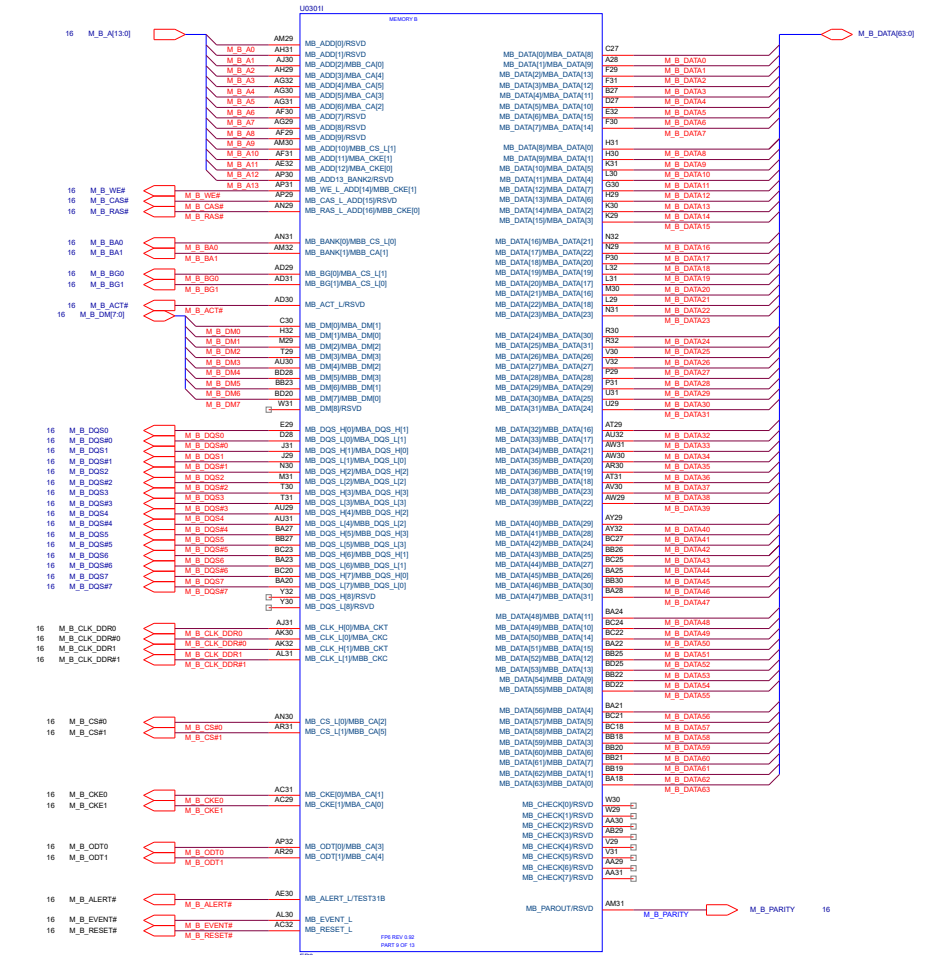


20200509 mount R0403

Memory Channel B

Main Board

SO-DIMM DDR4

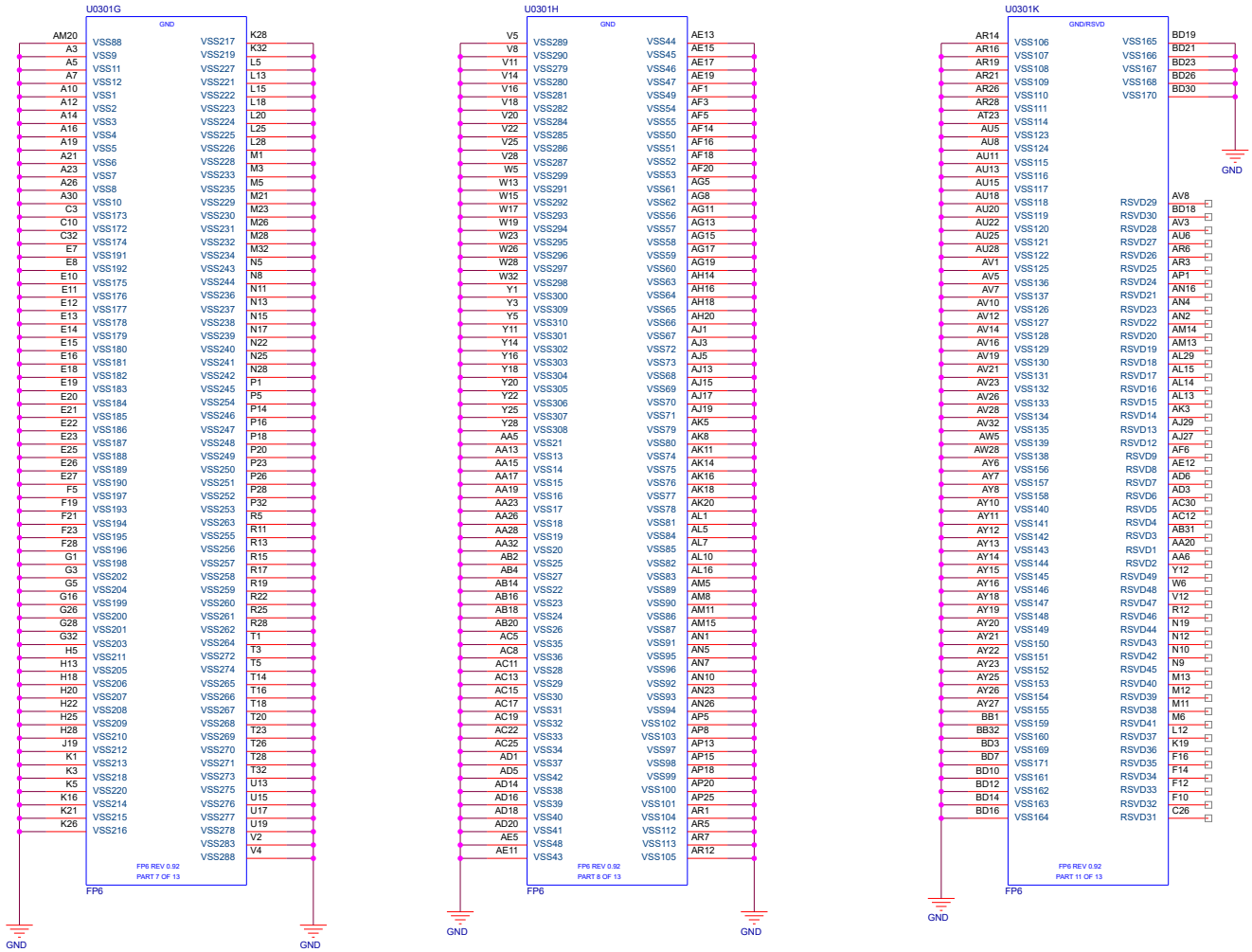


EVENT# 對接pull-H +1.2V (FP6 CRB)

RESET# only對接 (FP6 CRB)

ASUS	Project Name: GA503QS		Rev: R1.0
Title : AMD_CPU_DDR4			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD EE	
Date: Tuesday, October 13, 2020	Sheet 4 of 104		

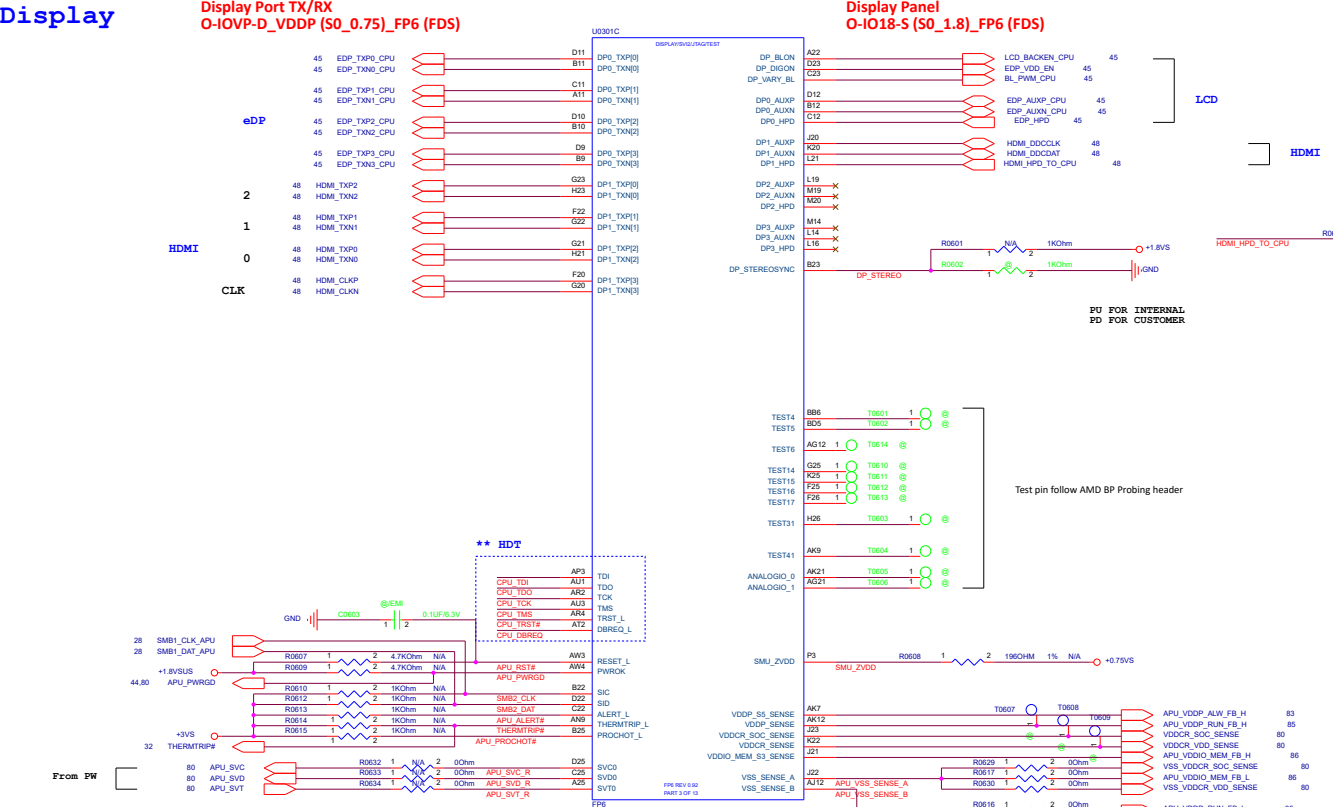
CPU_GND



Project Name: GA503QS		Rev: R1.0
Title : AMD_CPU_GND		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: RD2 EE3	
Date: Tuesday, October 13, 2020	Sheet 5 of 104	

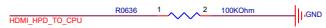
Display

Display Port TX/RX
O-IOVP-D_VDDP (S0_0.75)_FP6 (FDS)

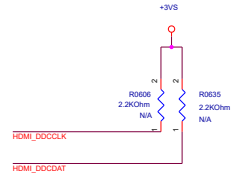


Display Panel
O-IO18-S (S0_1.8)_FP6 (FDS)

Display Port HPD
I-IO33-S (S0_3.3)_FP6 (FDS)

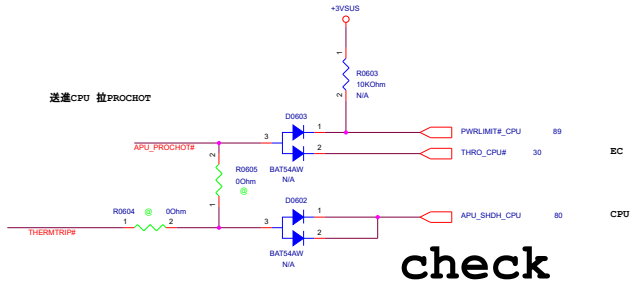


PU FOR INTERNAL
PD FOR CUSTOMER



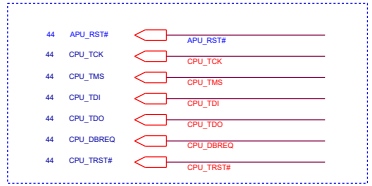
Test pin follow AMD BP Probing header

T0607~T0609 Has an accessible probing point near the APU.



check

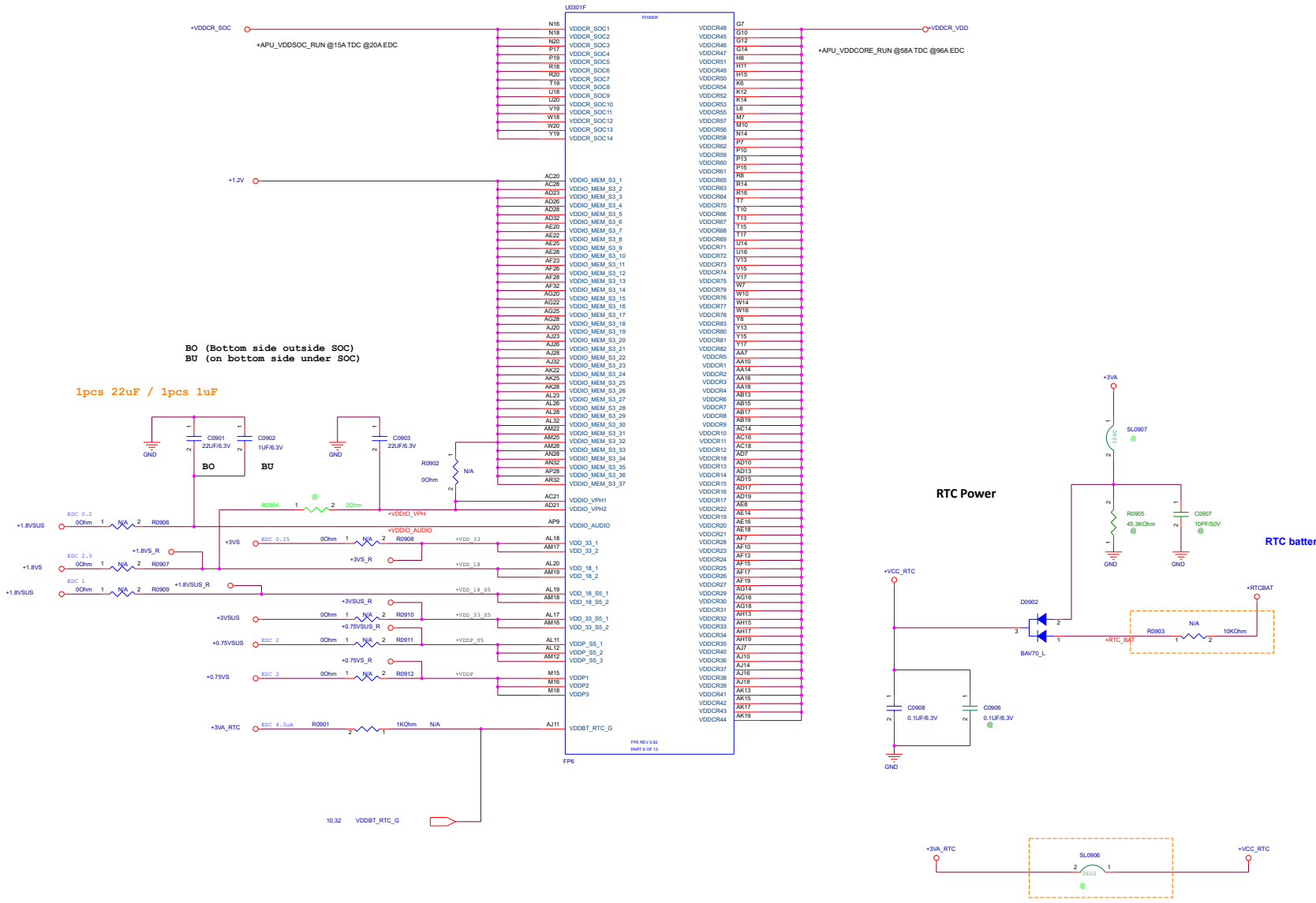
** HDT Remove P44



<Variant Name>

ASUS	Project Name: GA503QS	Rev: R1.0
Title :		
Size: Custom	Dept.: NB-ASUSTeK COMPUTER IN	Engineer:
Date: Tuesday, October 13, 2020	Sheet 6 of 104	

CPU_Power

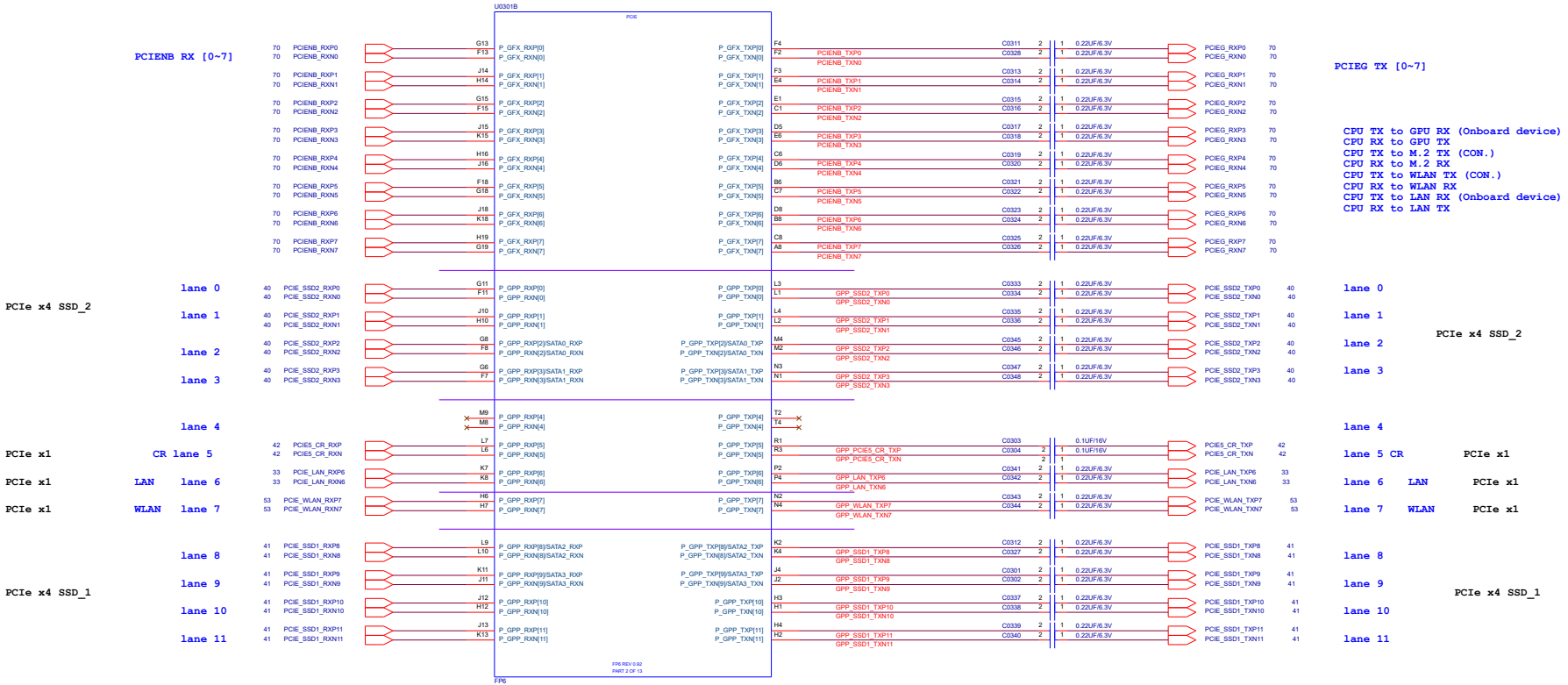


Project Name: GA503QS			Rev: R1.0
Title: CFL-H_CPU_PWR(1)_R1.3B			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD EE3	
Date: Tuesday, October 13, 2020	Sheet 9 of 104		

PCIE/WLAN/LAN/SSD

RX Side

TX Side



Project Name: GA503QS			Rev: R1.0
Title: CFL-H_CPU_DMI,PEG,FDI,eDP,DDI_R1.3B			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1	
Date: Tuesday, October 13, 2020	Sheet 3 of 104		

	Project Name GA503QS	Rev 1.0

Title : PD_TPS65993AC

Size Custom	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Design IP

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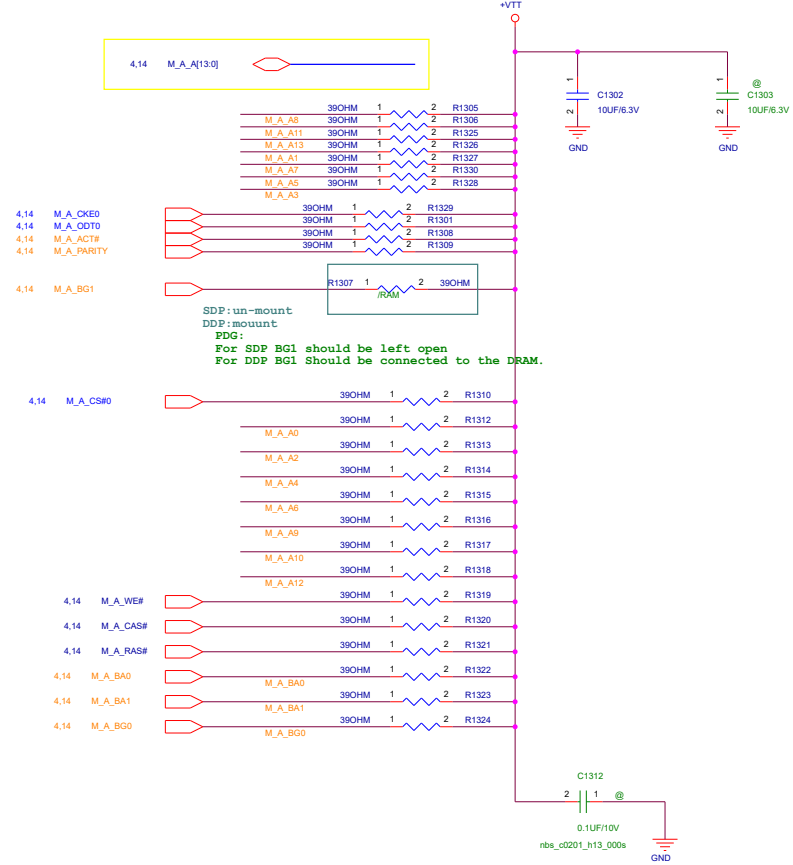


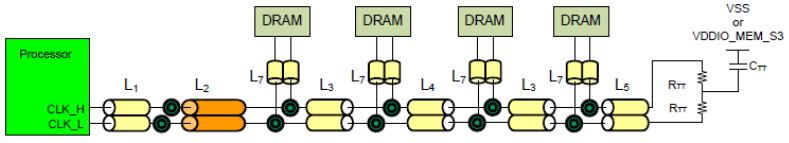
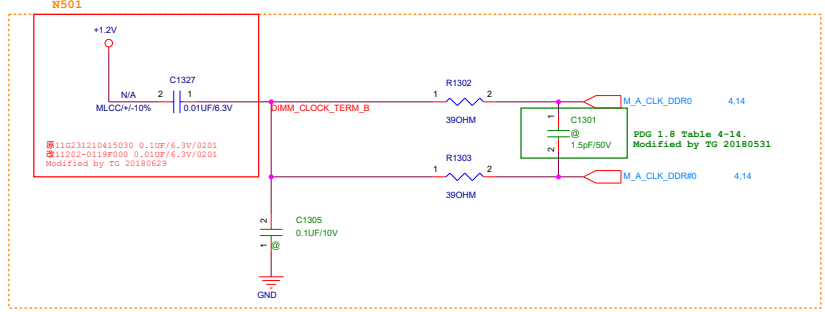


Figure 57. CLK Routing Model (DDR4 x16 DRAM Down)

The termination component values for MA_CLK are listed in Table 40.

Table 40. Component Table—DDR4 x16 CLK Termination

Ref	Value	Tolerance	Package	Comments
R_{TT}	39Ω	5%	0402	CLK termination
C_{TT}	0.1 µF	5%	0402	CLK termination to VSS or VDDIO_MEM_S3. CLK termination must match the CLK reference plane.



Clock Pull up power change from +0.6V to +1.2V (CFL PDG) 20820601

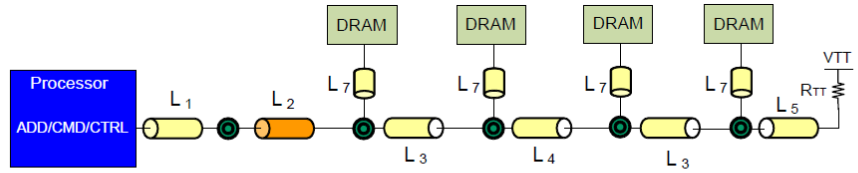


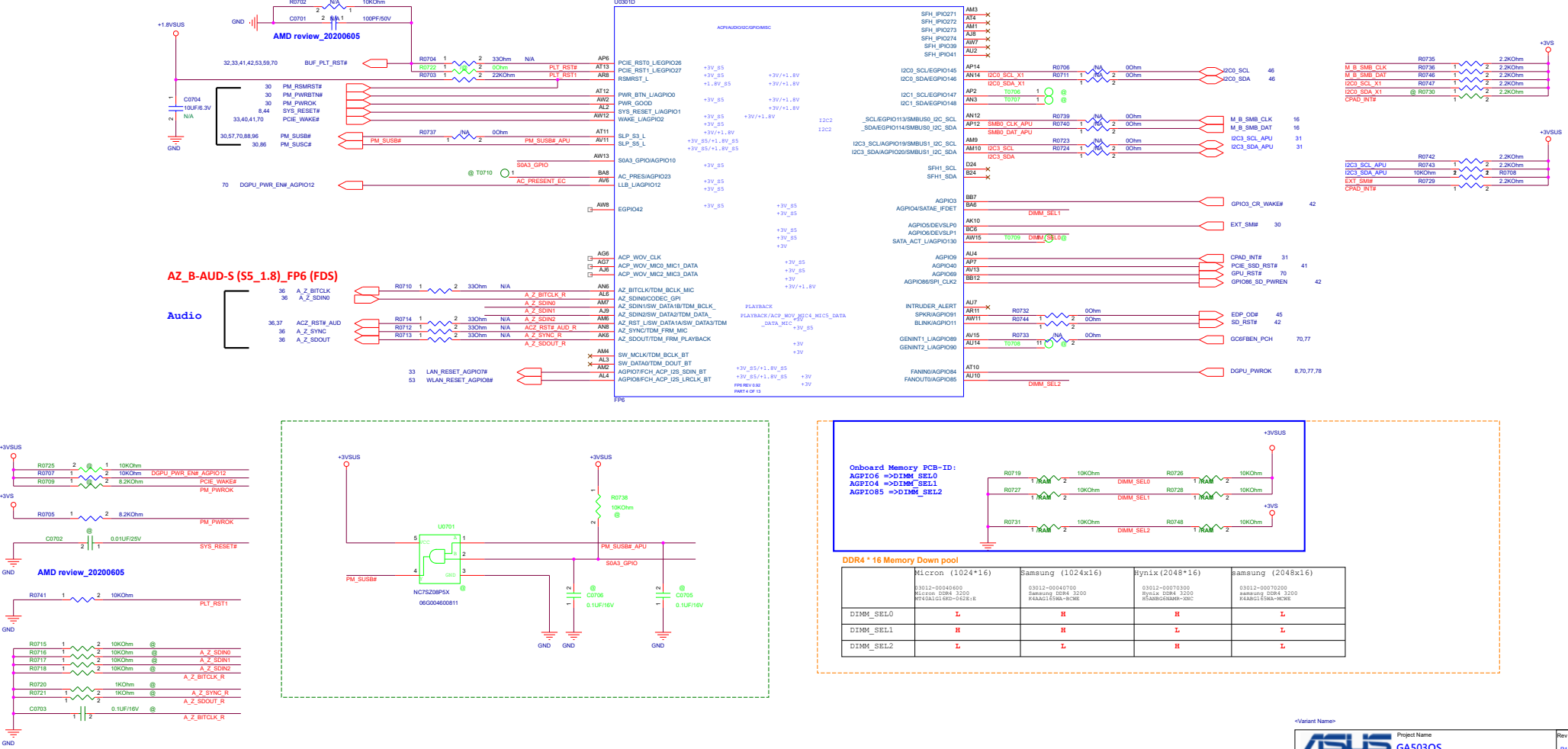
Figure 58. ADD/CMD/CTL Routing Model (DDR4 x16 DRAM Down)

The termination component values for ADD/CMD/CTL are listed in Table 42.

Table 42. Component Table—DDR4 x16 ADD/CMD/CTL Termination

Ref	Value	Tolerance	Package	Comments
R_{TT}	39Ω	5%	0402	ADD/CMD/CTL termination to VTT

Title <Title>		
Size A	Document Number GA503QS	Rev <RevCode>
Date: Tuesday, October 13, 2020	Sheet 15 of 104	



	Micron (1024*16)	Samsung (1024x16)	Hynix(2048*16)	samsung (2048x16)
	03012-00040600 Micron DDR4 3200 MT40A1G16KD-062E:E	03012-00040700 Samsung DDR4 3200 K4AAG165WA-BCWE	03012-00070300 Hynix DDR4 3200 H5ANBG6NAMR-XNC	03012-00070200 samsung DDR4 3200 K4ABG165WA-MCWE
DIMM_SEL0	L	H	H	L
DIMM_SEL1	H	H	L	L
DIMM_SEL2	L	L	H	L

<Variant Name>

ASUS	Project Name GA503QS	Rev R1.0
Title :		
Size Custom	Dept.: NASUSTeK COMPUTER INC	Engineer:
Date: Tuesday, October 13, 2020	Sheet 7 of 104	

Title <Title>		
Size A	Document Number GA503QS	Rev <RevCode>
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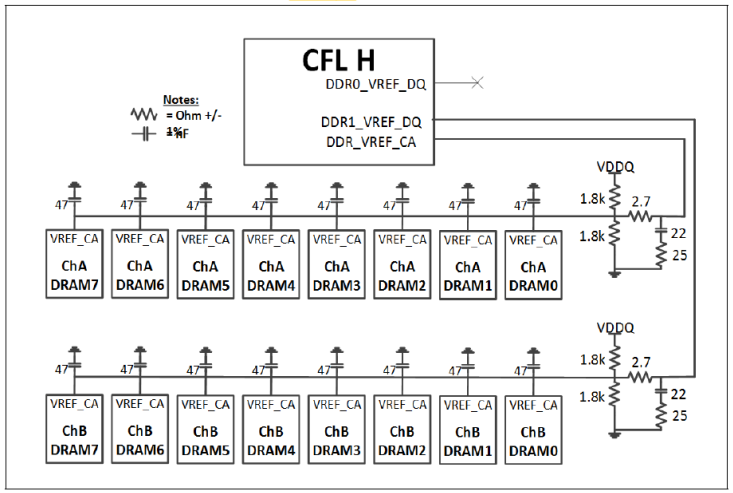
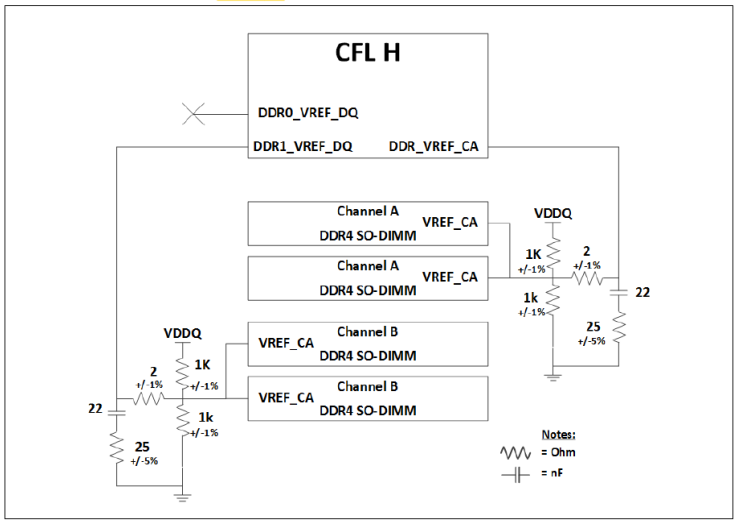
Memory Down Vref

Figure 4-24. CFL-H DDR4 x8 Memory Down V_{REF-CA} Overview



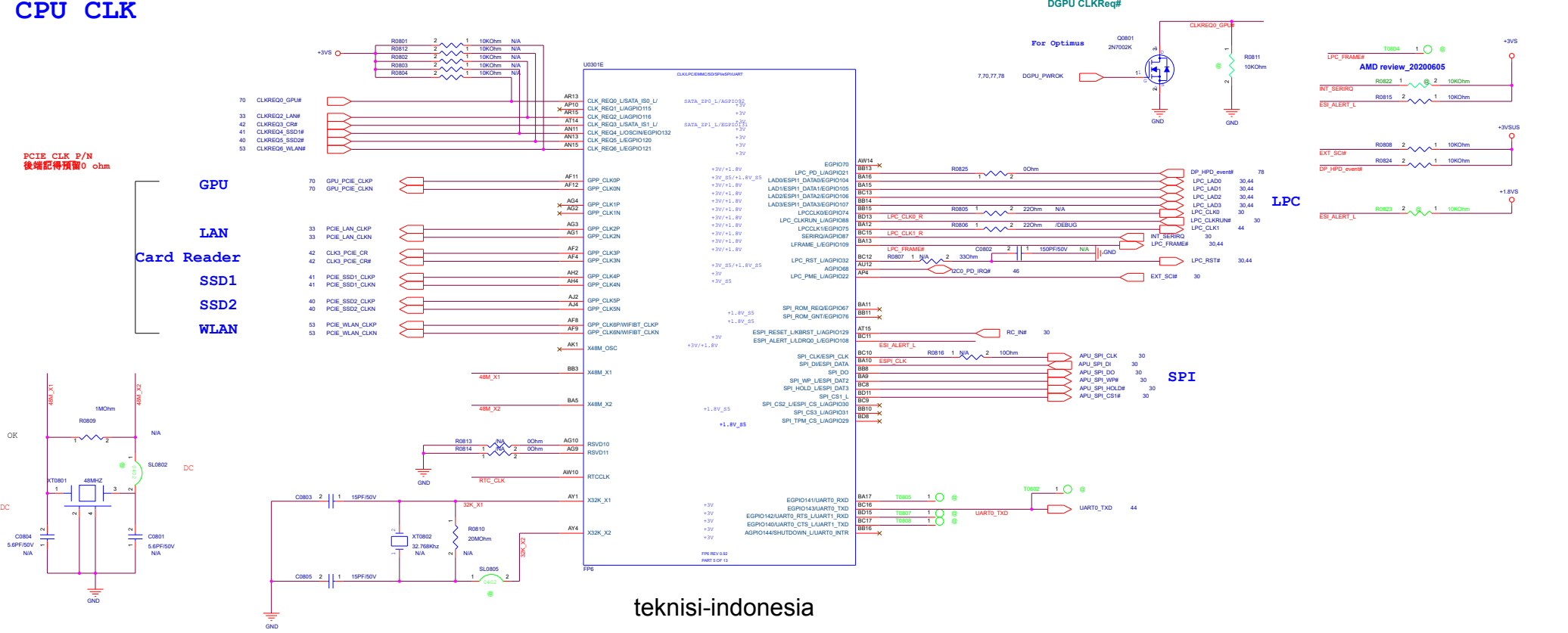
SO-DIMM1 Vref

Figure 4-22. CFL-H DDR4 SO-DIMM V_{REF-CA} Overview

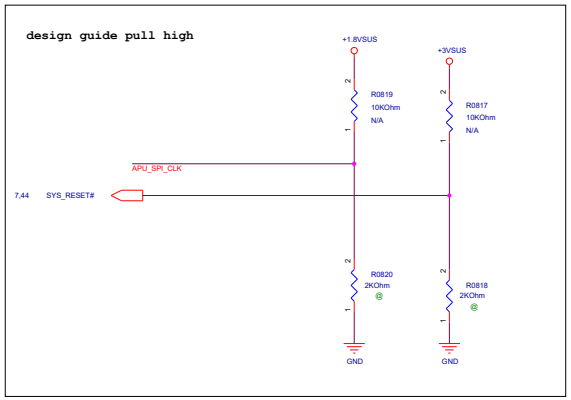


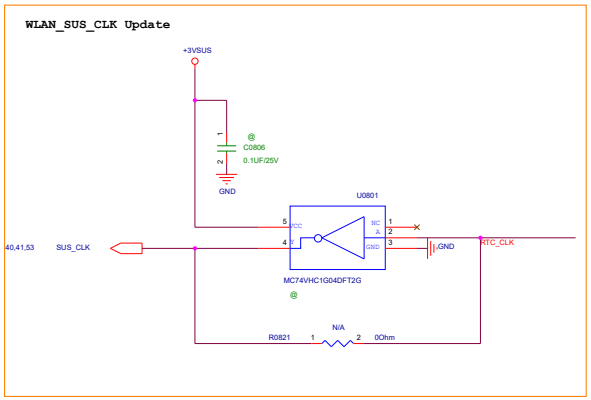
Project Name: GA503QS		Rev: 1.0
Title : DIM_CA/DQ Voltage		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Tuesday, October 13, 2020	Sheet 18 of 104	

CPU CLK



teknisi-indonesia





<variant_name>

ASUS	Project Name: GA503QS	Rev: R1.0
Title :		
Size: Custom	Dept.: NB-ASUSTeK COMPUTER IN	Engineer:
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Project Name: GA503QS		Rev: 1.0
Title : DIM_CA/DQ Voltage		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
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PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	RCIN#	Native	RC_IN#		PU 10K	+3VS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_KBCPCI_PCH_X1			
GPP_A10	CLKOUT_LPC1	Native	CLK_DEBUG_X1			
GPP_A11	PME#	GPO	(N.C)			
GPP_A12	GPI	GPO	(N.C)			
GPP_A13	SUSWANRN#	Native	ME_SusPwrDnAck		PU 10K(@)	+3VSUS
GPP_A14	SUS_STAT#	Native	PCH_SUS_STAT#			
GPP_A15	SUS_ACK#	Native	PM_SUSACK#			
GPP_A16	Native/GPI	GPO	(N.C)			
GPP_A17	GPI	GPO	(N.C)			
GPP_A18	GPI	GPO	(N.C)			
GPP_A19	GPI	GPO	(N.C)			
GPP_A20	GPI	GPO	(N.C)			
GPP_A21	GPI	GPO	TBTA_MRESET(Reserved)			
GPP_A22	GPI	GPO	PCH_RTD3_CIO_PWR_EN		PU 10K	+VCC3V3_SX
GPP_A23	GPI	GPO	PCH_RTD3_USB_PWR_EN		PD 100K	

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	(N.C)			
GPP_B1	GPI	GPI	TBT_I2C_INT_PCH		PU 10K	+3VSUS
GPP_B2	GPI	GPO	(N.C)			
GPP_B3	GPI	GPO	(N.C)			
GPP_B4	GPI	GPO	(N.C)			
GPP_B5	GPI	Native	CLK_REQ0#/CLKREQ0_PEGA#		PU 10K	+3VSUS
GPP_B6	GPI	Native	CLK_REQ1#		PU 10K(@)	+3VSUS
GPP_B7	GPI	Native	CLK_REQ2#/CLKREQ2_WLAN_AC#		PU 10K	+3VSUS
GPP_B8	GPI	Native	CLK_REQ3#		PU 10K(@)	+3VSUS
GPP_B9	GPI	Native	CLK_REQ4#/CLKREQ4_GLAN#		PU 10K	+3VSUS
GPP_B10	GPI	Native	CLK_REQ5#/CLKREQ5_TBT #		PU 10K	+3VSUS
GPP_B11	GPO	GPO	(N.C)			
GPP_B12	SLP_S0#	Native	SLP_S0#			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPPB14	PD		
GPP_B15	GPI	GPI	PCH_GPPB15/KB_LANG_ID0		PU 10K	+3VS
GPP_B16	GPI	GPI	PCH_GPPB16/KB_LANG_ID1		PU 10K	+3VS
GPP_B17	GPI	GPO	PCH_GPPB17/XBOX_WRST		PD 10K	
GPP_B18	GPO	Strap	PCH_GPPB18	PD		
GPP_B19	GPI	GPO	PCH_GPPB19/BT_ON_PCH		PD 10K(@)	
GPP_B20	GPI	GPO	PCH_GPPB20/GPUEVENT#_PCH		PU 10K	+3VSUS
GPP_B21	GPI	GPI	PCH_GPPB21/GC6FBEN_PCH		PU 10K(@)	+3VS
GPP_B22	GPO	Strap	PCH_GPPB22	PD		
GPP_B23	GPO	Native	SML1ALERT#	PD	PU 150K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		PU 2.2K	+3VSUS
GPP_C2	GPO	GPI	GPP_C2_BT_UART_WAKE_N	PD	PU 4.7K	+3VSUS
GPP_C3	SML0CLK	Native	SML0_CLK (Reserved)		PU 2.2K	+3VSUS
GPP_C4	SML0DATA	Native	SML0_DAT (Reserved)		PU 2.2K	+3VSUS
GPP_C5	GPO	Strap	PCH_GPPC5	PD		
GPP_C6	SML1CLK	Native	SML1_CLK		PU 2.2K	+3VSUS
GPP_C7	SML1DATA	Native	SML1_DAT		PU 2.2K	+3VSUS
GPP_C8	GPI	GPO	(N.C)			
GPP_C9	GPI	GPO	(N.C)			
GPP_C10	GPI	GPO	(N.C)			
GPP_C11	GPI	GPO	(N.C)			
GPP_C12	GPI	GPI	DIMM_SEL0			
GPP_C13	GPI	GPI	DIMM_SEL1			
GPP_C14	GPI	GPI	DIMM_SEL2			
GPP_C15	GPI	GPI	NFC_ID		PU 10K	+3VSUS
GPP_C16	GPI	Native	TBT_I2C_SDA_PCH		PU 2.2K	+3VSUS
GPP_C17	GPI	Native	TBT_I2C_SCL_PCH		PU 2.2K	+3VSUS
GPP_C18	GPI	Native	I2C1_SDA		PU 2.2K	+3VS
GPP_C19	GPI	Native	I2C1_SCL		PU 2.2K	+3VS
GPP_C20	GPI	GPI	PCH_GPPC20/DGPU_PWROK		PU 10K	+3VS_NV
GPP_C21	GPI	GPO	PCH_GPPC21/GPU_RST#		PD 10K	
GPP_C22	GPI	GPO	(N.C)			
GPP_C23	GPI	GPI	CPAD_INT#		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GPI	GPO	(N.C)			
GPP_D1	GPI	GPO	(N.C)			
GPP_D2	GPI	GPO	(N.C)			
GPP_D3	GPI	GPO	(N.C)			
GPP_D4	GPI	GPO	(N.C)			
GPP_D5	GPI	Native3	PCH_GPPD5/M.2_BT_PCMFRM_CRF_RST_N		PD 75K	
GPP_D6	GPI	Native3	PCH_GPPD6/M.2_BT_PCMOUT_CLKREQ0		PD 75K(@)	
GPP_D7	GPI	GPO	PCH_GPPD7/M.2_BT_PCMIN		PD 100K(@)	
GPP_D8	GPI	GPO	PCH_GPPD8/M.2_BT_PCMCLK			
GPP_D9	GPI	GPO	(N.C)			
GPP_D10	GPI	GPO	(N.C)			
GPP_D11	GPI	GPO	(N.C)			
GPP_D12	GPI	GPO	(N.C)			
GPP_D13	GPI	GPO	(N.C)			
GPP_D14	GPI	GPO	(N.C)			
GPP_D15	GPI	GPO	(N.C)			
GPP_D16	GPI	GPO	(N.C)			
GPP_D17	GPI	GPO	(N.C)			
GPP_D18	GPI	GPO	(N.C)			
GPP_D19	GPI	GPO	(N.C)			
GPP_D20	GPI	GPO	(N.C)			
GPP_D21	GPI	GPO	(N.C)			
GPP_D22	GPI	GPO	(N.C)			
GPP_D23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	GPI	Native	SATAPCIE_DET0		PU 10K(@)	+3VS
GPP_E1	GPI	Native	SATAPCIE_DET1		PU 10K	+3VS
GPP_E2	GPI	Native	SATAPCIE_DET2		PU 10K(@)	+3VS
GPP_E3	GPI	GPI	EXT_SMI#		PU 10K	+3VS
GPP_E4	GPI	Native	SATA0_HDD1_DEVSLP		PU 10K(@)	+3VS
GPP_E5	GPI	Native	SATA1_NGFF3_DEVSLP		PU 10K(@)	+3VS
GPP_E6	GPI	Native	NGFF3_DEVSLP		PU 10K(@)	+3VSUS
GPP_E7	GPI	GPI	EXT_SCI#		PU 10K	+3VS
GPP_E8	GPI	Native	SATA_LED#		PU 10K	+3VS
GPP_E9	GPI	Native	USB_OC#0		PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1		PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2		PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3		PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	GPI	Native	SATAPCIE_DET3		PU 10K(@)	+3VS
GPP_F1	GPI	Native	SATAPCIE_DET4		PU 10K	+3VS
GPP_F2	GPI	GPO	(N.C)			
GPP_F3	GPI	GPO	(N.C)			
GPP_F4	GPI	GPO	(N.C)			
GPP_F5	GPI	GPO	(N.C)			
GPP_F6	GPI	GPO	(N.C)			
GPP_F7	GPI	GPO	(N.C)			
GPP_F8	GPI	GPO	(N.C)			
GPP_F9	GPI	GPO	(N.C)			
GPP_F10	GPI	GPO	(N.C)			
GPP_F11	GPI	GPO	(N.C)			
GPP_F12	GPI	GPO	(N.C)			
GPP_F13	GPI	GPO	(N.C)			
GPP_F14	GPI	GPO	(N.C)			
GPP_F15	GPI	Native	USB_OC#4		PU 10K	+3VSUS
GPP_F16	GPI	Native	USB_OC#5		PU 10K	+3VSUS
GPP_F17	GPI	Native	USB_OC#6		PU 10K	+3VSUS
GPP_F18	GPI	Native	USB_OC#7		PU 10K	+3VSUS
GPP_F19	GPI	GPO	(N.C)			
GPP_F20	GPI	GPO	(N.C)			
GPP_F21	GPI	GPO	(N.C)			
GPP_F22	GPI	GPO	(N.C)			
GPP_F23	GPI	GPO	PCH_GPPF23		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_G0	GPI	GPO	(N.C)			
GPP_G1	GPI	GPO	(N.C)			
GPP_G2	GPI	GPO	(N.C)			
GPP_G3	GPI	GPO	(N.C)			
GPP_G4	GPI	GPO	(N.C)			
GPP_G5	GPI	GPO	(N.C)			
GPP_G6	GPI	GPO	(N.C)			
GPP_G7	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	GPI	Native	CLK_REQ6#/CLKREQ6_NGFF1#		PU 10K	+3VSUS
GPP_H1	GPI	Native	CLK_REQ7#/CLKREQ7_NGFF2#		PU 10K	+3VSUS
GPP_H2	GPI	Native	CLK_REQ8#/CLKREQ8_NGFF3#		PU 10K	+3VSUS
GPP_H3	GPI	Native	CLK_REQ9#		PU 10K(@)	+3VSUS
GPP_H4	GPI	Native	CLK_REQ10#		PU 10K(@)	+3VSUS
GPP_H5	GPI	Native	CLK_REQ11#		PU 10K(@)	+3VSUS
GPP_H6	GPI	Native	CLK_REQ12#		PU 10K(@)	+3VSUS
GPP_H7	GPI	Native	CLK_REQ13#		PU 10K(@)	+3VSUS
GPP_H8	GPI	Native	CLK_REQ14#		PU 10K(@)	+3VSUS
GPP_H9	GPI	Native	CLK_REQ15#		PU 10K(@)	+3VSUS
GPP_H10	GPI	GPO	(N.C)			
GPP_H11	GPI	GPO	(N.C)			
GPP_H12	GPO	GPO	(N.C)	PD	PD 20K(@)	
GPP_H13	GPI	GPO	(N.C)			
GPP_H14	GPI	GPO	(N.C)			
GPP_H15	GPI	GPO	SML3ALERT#		PU 100K	+3VSUS
GPP_H16	GPI	GPI	KBID_0			
GPP_H17	GPI	GPI	KBID_1			
GPP_H18	GPI	GPI	KBID_2			
GPP_H19	GPI	GPO	(N.C)			
GPP_H20	GPI	GPO	(N.C)			
GPP_H21	GPI	GPO	(N.C)			
GPP_H22	GPI	GPO	(N.C)			
GPP_H23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GPI	GPO	(N.C)			
GPP_I1	GPI	GPO	(N.C)			
GPP_I2	GPI	GPO	(N.C)			
GPP_I3	GPI	GPO	(N.C)			
GPP_I4	GPI	GPO	EDP_HPD		PD 100K	
GPP_I5	GPI	GPO	(N.C)			
GPP_I6	GPO	GPO	(N.C)			
GPP_I7	GPI	GPO	(N.C)			
GPP_I8	GPO	GPO	(N.C)			
GPP_I9	GPI	GPO	(N.C)			
GPP_I10	GPO	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_J0	GPI	GPO	(N.C)			
GPP_J1	CPU_VCCIO_PWR_GATE#	Native	CPU_C10_GATE#_PCH		PU 100K	+1.8VSUS
GPP_J2	GPI	GPO	(N.C)			
GPP_J3	GPI	GPO	(N.C)			
GPP_J4	CNV_BRI_DT	Native	CNV_BRI_DT		PU 4.7K	+1.8VSUS
GPP_J5	CNV_BRI_RSP	Native	CNV_BRI_RSP		PU 20K(@)	+1.8VSUS
GPP_J6	CNV_RGI_DT	Native	CNV_RGI_DT		PD 75K	
GPP_J7	CNV_RGI_RSP	Native	CNV_RGI_RSP		PU 20K(@)	+1.8VSUS
GPP_J8	GPI	GPO	(N.C)			
GPP_J9	GPO	GPO	(N.C)			
GPP_J10	GPI	GPO	(N.C)			
GPP_J11	A4WP_PRESENT	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_K0	GPI	GPO	GPIO_3_FORCE_PWR		PD 100K	
GPP_K1	GPI	GPI	PCB_ID0		PD 10K	
GPP_K2	GPI	GPI	PCB_ID1		PD 10K	
GPP_K3	GPI	GPO	GPP_K3/WLAN_BT_LED		PD 100K	
GPP_K4	GPI	GPO	GPP_K4/WLAN_LED		PD 100K	
GPP_K5	GPI	GPO	VOL_DOWN#(N.C)			
GPP_K6	GPI	GPO	VOL_UP#(N.C)			
GPP_K7	GPI	GPO	GPP_K7/TBT_HPD#		PU 10K	+3VS
GPP_K8	GPI	GPO	GPP_K8/DGPU_PWR_EN#		PU 10K(@)	+3VS
GPP_K9	GPI	GPO	WLAN_ON#		PD 100K	
GPP_K10	Reserved	GPO	GPP_K10/HDMI_HPD#		PU 10K	+3VS
GPP_K11	Reserved	GPO	GPP_K11/DP_HPD#		PU 10K	+3VS
GPP_K12	GPI	GPO	(N.C)			
GPP_K13	GPI	GPO	(N.C)			
GPP_K14	GPI	GPO	(N.C)			
GPP_K15	GPI	GPO	(N.C)			
GPP_K16	GPI	GPO	(N.C)			
GPP_K17	GPI	GPO	(N.C)			
GPP_K18	GPI	GPO	(N.C)			
GPP_K19	GPI	GPO	(N.C)			
GPP_K20	Reserved	GPO	(N.C)			
GPP_K21	Reserved	GPO	(N.C)			
GPP_K22	GPI	GPO	(N.C)			
GPP_K23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	PM_BATLOW#		PU 10K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_X1		PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	LAN_WAKE#(N.C)		PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#		PU 10K(@)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#		PD 100K	
GPD5	SLP_S4#	Native	SLP_S4#		PD 100K	
GPD6	SLP_A#	Native	SLP_A# (N.C)			
GPD7	GPO	GPO	PCH_GPD7		PU 10K	+3VA_DSW
GPD8	SUSCLK	Native	SUS_CLK#			
GPD9	SLP_WLAN#	Native	SLP_WLAN# (N.C)			
GPD10	SLP_S5#	Native	SLP_S5# (N.C)			
GPD11	LANPHYPC	GPO	LAN_PWREN (N.C)		PU 10K(@)	+3VA_DSW

IT8225VG-128/BX GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	O	GPO	PWR_LED	PD 1M	
GPA1	OD	GPO	CHG_LED#		
GPA2	OD	GPO	CHG_FULL_LED#		
GPA3	Alt	PWM	FAN2_PWM		
GPA4	O	GPO	EC_GPA4(N.C)		
GPA5	Alt	PWM	FAN1_PWM		
GPA6	Alt	GPO	EC_GPA6(N.C)		
GPA7	O	GPO	EC_GPA7(N.C)		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_OC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	EC_GPB2(N.C)		
GPB3	Alt	GPI	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PS_ON_EC		
GPB5	O	GPO	EC_GPB5/NKey_WRST	PD 10K	
GPB6	OD	GPO	RC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	O	GPO	EC_GPC0		
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	O	GPO	PM_PWRBTN#	PU 10K(@)	+3VSUS
GPC4	I	GPI	EC_GPC4/PM_SUSB#	PD 100K	
GPC5	I	GPI	PM_SUSC#	PD 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PD 100K	
GPC7	O	GPO	EC_GPC7/NKEY_PWR_EN	PD 10K(@)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPO	EC_GPD0/EC_OV_DDR		
GPD1	O	GPO	EC_GPD1/ME_AC_PRESENT		
GPD2	Alt	GPI	BUF_PLT_RST#	PD 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	O	GPO	EC_GPD5/OP_SD#		
GPD6	Alt	GPI	FAN1_TACH	PU 10K	+3VS
GPD7	Alt	GPI	FAN2_TACH	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PD 4.7K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PD 4.7K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO	5VSUS_ON	PD 1M & PU 100K	+3VA_EC
GPE4	O	GPO	VSUS_ON	PD 1M & PU 100K	+3VA_EC
GPE5	I	GPO	3VADSW_ON	PU 100K	+3VA_EC
GPE6	OD	GPO	WLAN_PWR_EN	PD 100K	
GPE7	OD	GPO	THRO_CPU#	PU 10K	+3VA_DSW

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	CAP_LED#		
GPF1	O	GPO	NUM_LED#		
GPF2	Alt	SMBus	P_SMB0_CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB0_DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	PECI	EC_PECI	PD 10K(@)	
GPF7	O	GPO	PCH_SPI_OV		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	O	GPO	PCH_SUSACK#		
GPG2	I	GPI	EC_GPG2	PU 100K	+3VA_EC
GPG6	O	GPO	EC_GPG6(N.C)		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB3_CLK/TBT_I2C_SCL_EC	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB3_DAT/TBT_I2C_SDA_EC	PU 4.7K	+3VA_EC
GPH3	O	GPO	PM_RSMRST#	PD 10K	
GPH4	O	GPO	DPWROK_EC	PD 10K	
GPH5	O	GPO	PM_PWROK	PD 10K	
GPH6	O	GPO	PM_SYSPWROK	PD 10K	
GPH7	O	GPO	LCD_BACKOFF#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_SUS#	PD 100K(@)	
GPI1	I	GPI	3VSUS_PWRGD	PU 100K	+3VSUS
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3VS
GPI3	I	GPI	IMVP8_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD_EC	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#	PU 10K(@)	+3VSUS
GPI6	Alt	AD	A/D_MAX_POWER		
GPI7	Alt	AD	MB_MAX_POWER	PU 100K&PD 270K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	O	GPO	EC_GPJ0		
GPJ1	O	GPI	GC6FBEN_PCH	PU 10K(@)	+3VS
GPJ2	Alt	GPI	EC_GPJ2/TBTA_I2C_INT_EC		
GPJ3	O	GPO	EC_GPJ3/USB_BC1.2_OFF#		
GPJ4	Alt	GPO	EC_GPJ4/USB30_5VBUS		
GPJ5	O	GPI	EC_GPJ5/MB_DOCK_JACK_DETECT	PU 100K(@)	+3VA
GPJ6	I	GPI	NKEY_INT#	PU 10K	+3VA_DSW_NKeyPWR
GPJ7	O	GPO	USB_CHARGE_ON#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/EIO0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/EIO1		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/EIO2		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/EIO3		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/ESCK		CLK_KBCPCI_PCH		
GPM5	LFRAME#/ECS#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

G703GI Source:

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	SM-Bus Address
SO-DIMM A(0)	A0h
SO-DIMM B(0)	A4h
SO-DIMM A(1)	A2h
SO-DIMM B(1)	A6h
EC Master (SMB1)	SM-Bus Address
SM-Bus Device	
GPU INT. Thermal sensor	9Eh, 9Ch
CPU Thermal Sensor	90h
TI_TAS5766M*2	98h, 9Ah
ASM1562	66h
GPU (Thermistor sense)	74h
PWR(Thermistor sense)	7Eh, 7Ch, 7Ah, 78h, 76h

Device Identification

CPU Thermal Senser		
1st	06G023123010	NCT7717U
2nd		

GPU Thermistor		
1st	06021-00260000	APL6002A8I-TRG
2nd		

USB3.0/PCIE/SATA Setting		
1	USB3#1	
2	USB3#2	
3	USB3#3	USB Port1
4	USB3#4	
5	USB3#5	USB Port3
6	USB3#6	USB Port4
7	USB3#7	Card Reader
8	PCIE#2	
9	PCIE#3	
10	PCIE#4	
11	PCIE#5	ThunderBolt x4
12	PCIE#6	
13	PCIE#7	
14	PCIE#8	
15	PCIE#9	PCIE3.0 x 4 SSD
16	PCIE#10	
17	PCIE#11	
18	PCIE#12	
19	PCIE#13(SATA0B)	SATA HDD
20	PCIE#14(SATA1B)	
21	PCIE#15	GLAN
22	PCIE#16	WLAN_11AC
23	PCIE#17	PCIE3.0 x 4 SSD
24	PCIE#18	
25	PCIE#19	
26	PCIE#20	
27	PCIE#21	PCIE3.0 x 4 SSD
28	PCIE#22	
29	PCIE#23	
30	PCIE#24	

USB2.0 Setting		
1	USB2#1	
2	USB2#2	
3	USB2#3	USB Port1
4	USB2#4	
5	USB2#5	USB Port3
6	USB2#6	USB Port4
7	USB2#7	Card Reader
8	USB2#8	XBOX WLAN
9	USB2#9	Camera
10	USB2#10	N-Key
11	USB2#11	
12	USB2#12	Tobii IS4
13	USB2#13	TBT
14	USB2#14	BT

HSIO	HM370			QM370			CM246			IRST			Devices Assign			
0	USB3.1 Gen1/Gen2 #1			USB3.1 Gen1/Gen2 #1			USB3.1 Gen1/Gen2 #1						(port1) USB3.1 Typc C			
1	USB3.1 Gen1/Gen2 #2			USB3.1 Gen1/Gen2 #2			USB3.1 Gen1/Gen2 #2						(port2) USB3.1 Typc C			
2	USB3.1 Gen1/Gen2 #3			USB3.1 Gen1/Gen2 #3			USB3.1 Gen1/Gen2 #3						(port1) USB3.0 Typc A / USB3.1 Typc A			
3	USB3.1 Gen1/Gen2 #4			USB3.1 Gen1/Gen2 #4			USB3.1 Gen1/Gen2 #4						(port2) USB3.0 Typc A / USB3.1 Typc A			
4	USB3.1 Gen1 #5			USB3.1 Gen1/Gen2 #5			USB3.1 Gen1/Gen2 #5						(port3) USB3.0 Typc A / USB3.1 Typc A	only for QM370 / CM246		
5	USB3.1 Gen1 #6			USB3.1 Gen1/Gen2 #6			USB3.1 Gen1/Gen2 #6						(port4) USB3.0 Typc A / USB3.1 Typc A	only for QM370 / CM246		
6	USB3.1 Gen1 #7			USB3.1 Gen1 #7			USB3.1 Gen1 #7	PCIE #1		NO	x4	x2	CR (USB3.0 / PCIE)			
7	USB3.1 Gen1 #8			USB3.1 Gen1 #8			USB3.1 Gen1 #8	PCIE #2								
8	NA			USB3.1 Gen1 #9			USB3.1 Gen1 #9	PCIE #3				x2				
9	NA			USB3.1 Gen1 #10			USB3.1 Gen1 #10	PCIE #4								
10	NA		GbE	PCIE #5		GbE	PCIE #5		GbE	NO	x4	x2	Thunderbolt (priority 1)			
11	NA			PCIE #6			PCIE #6									
12	NA			PCIE #7			PCIE #7					x2				
13	NA			PCIE #8			PCIE #8									
14	PCIE #9		GbE	PCIE #9		GbE	PCIE #9		GbE	Yes	x4	x2	1st M.2 SSD (PCIE*4 / SATA#1a) (PCIE*4, optane)	1st M.2 SSD (PCIE*2, optane)		
15	PCIE #10			PCIE #10			PCIE #10									
16	PCIE #11	SATA #0a		PCIE #11	SATA #0a		PCIE #11	SATA #0a				x2				
17	PCIE #12	SATA #1a	GbE	PCIE #12	SATA #1a	GbE	PCIE #12	SATA #1a	GbE							
18	PCIE #13	SATA #0b	GbE	PCIE #13	SATA #0b	GbE	PCIE #13	SATA #0b	GbE	NO	x4	x2	HDD (SATA#0b)			
19	PCIE #14	SATA #1b		PCIE #14	SATA #1b		PCIE #14	SATA #1b					ODD (SATA#1b)			
20	PCIE #15			PCIE #15			PCIE #15	SATA #2				x2	GLAN			
21	PCIE #16			PCIE #16			PCIE #16	SATA #3					WLAN			
22	PCIE #17	SATA #4		PCIE #17	SATA #4		PCIE #17	SATA #4		Yes	x4	x2	2nd M.2 SSD (PCIE*4 / SATA#4) (PCIE*4, optane)	2nd M.2 SSD (PCIE*2, optane)		
23	PCIE #18	SATA #5		PCIE #18	SATA #5		PCIE #18	SATA #5								
24	PCIE #19			PCIE #19			PCIE #19	SATA #6				x2				
25	PCIE #20			PCIE #20			PCIE #20	SATA #7								
26	PCIE #21			PCIE #21			PCIE #21			Yes	x4	x2	3rd M.2 SSD (PCIE*4) (PCIE*4, optane)	3rd M.2 SSD (PCIE*2, optane)	10G LAN (PCIE*4) optional	Thunderbolt (priority 2)
27	PCIE #22			PCIE #22			PCIE #22									
28	PCIE #23			PCIE #23			PCIE #23					x2				
29	PCIE #24			PCIE #24			PCIE #24									

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Figure 14-1. High Speed I/O (HSIO) Lane Multiplexing in PCH-H

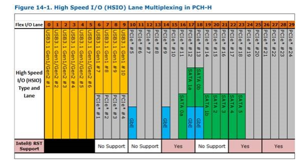

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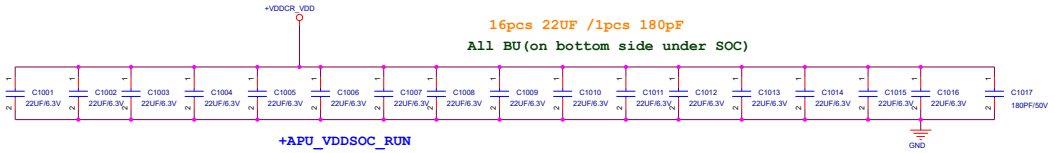
Table 1-7. PCH HSIO Detail (SKU 9-11of 11)

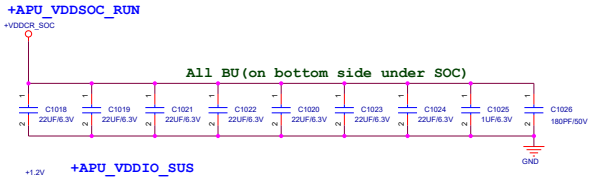
Flex I/O Lane	SKU		
	HM370	QM370	CM246
0	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
3	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
4	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
5	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
6	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
7	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
8	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
9	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
10	GbE	PCIe*, GbE	PCIe*, GbE
11	N/A	PCIe*	PCIe*
12	N/A	PCIe*	PCIe*
13	N/A	PCIe*	PCIe*
14	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
15	PCIe*	PCIe*	PCIe*
16	PCIe*, SATA 0A	PCIe*, SATA 0A	PCIe*, SATA 0A
17	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A
18	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B
19	PCIe*, SATA 1B	PCIe*, SATA 1B	PCIe*, SATA 1B
20	PCIe*	PCIe*	PCIe*, SATA 2
21	PCIe*	PCIe*	PCIe*, SATA 3
22	PCIe*, SATA 4	PCIe*, SATA 4	PCIe*, SATA 4
23	PCIe*, SATA 5	PCIe*, SATA 5	PCIe*, SATA 5
24	PCIe*	PCIe*	PCIe*, SATA 6
25	PCIe*	PCIe*	PCIe*, SATA 7
26	PCIe*	PCIe*	PCIe*
27	PCIe*	PCIe*	PCIe*
28	PCIe*	PCIe*	PCIe*
29	PCIe*	PCIe*	PCIe*

CPU_CAP

+APU_VDDCORE_RUN

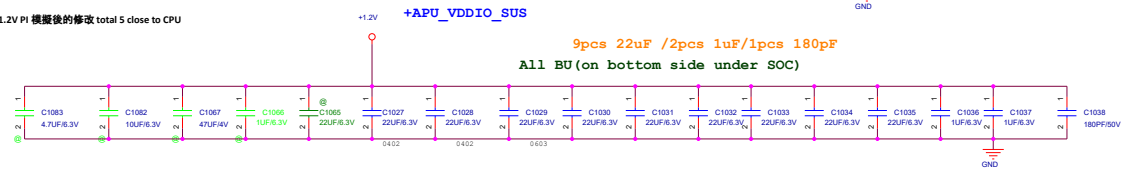


+APU_VDDSOC_RUN

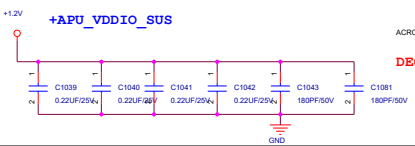


+1.2V PI 模擬後的修改 total 5 close to CPU

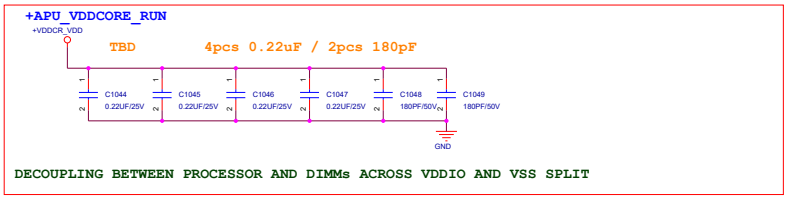
+APU_VDDIO_SUS



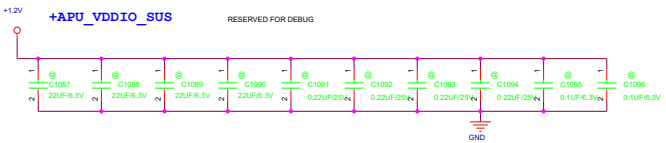
+APU_VDDIO_SUS



+APU_VDDCORE_RUN

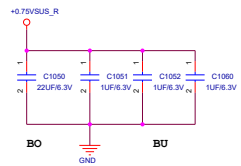


+APU_VDDIO_SUS

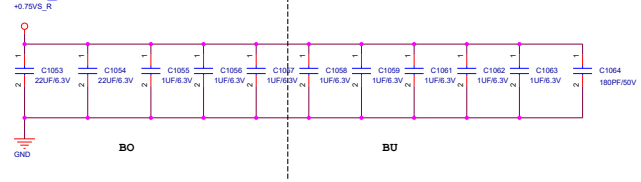


If the VSS plane is cut to create a VDDIO_MEM_S3 plane, ceramic capacitors with NP0 or C0G dielectric are connected across the VDDIO_MEM_S3 and VSS plane split.

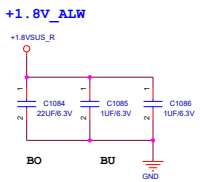
+VDDP_ALW



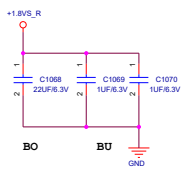
+VDDP_RUN



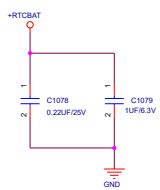
+1.8V_ALW

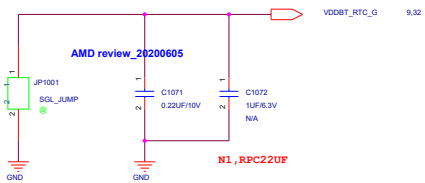


+1.8V_RUN

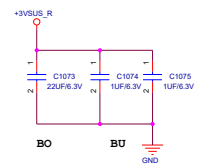


+VDDBT_RTC

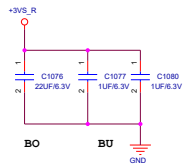




+3.3V_ALW



+3.3V_RUN



Project Name: GA503QS		Rev: R1.0
Title: CFL-H_CPU_PWR(1)_R1.3B		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD EE3
Date: Tuesday, October 13, 2020	Sheet 10 of 104	

Title <Title>		
Size A	Document Number GA503QS	Rev <RevCode>
Date: Tuesday, October 13, 2020	Sheet 20 of 104	

Title <Title>		
Size A	Document Number GA503QS	Rev <RevCode>
Date: Tuesday, October 13, 2020	Sheet 23 of 104	

Title <Title>		
Size A	Document Number GA503QS	Rev <RevCode>
Date: Tuesday, October 13, 2020	Sheet 24 of 104	

Title <Title>		
Size A	Document Number GA503QS	Rev <RevCode>
Date: Tuesday, October 13, 2020	Sheet 26 of 104	

	Project Name GA503QS	Rev 2.0

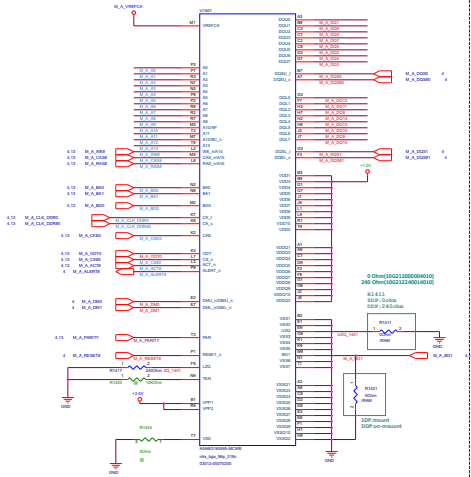
Title : USB3.1 TYPE-C+TI 1046A

Size Custom	Dept.: ASUSTeK COMPUTER INC. NB1	Engineer: Design IP

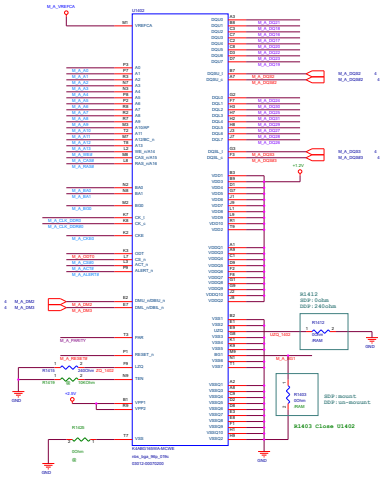
Date: Tuesday, October 13, 2020	Sheet	11	of	104

Title <Title>		
Size A	Document Number GA503QS	Rev <RevCode>
Date: Tuesday, October 13, 2020	Sheet 29 of 104	

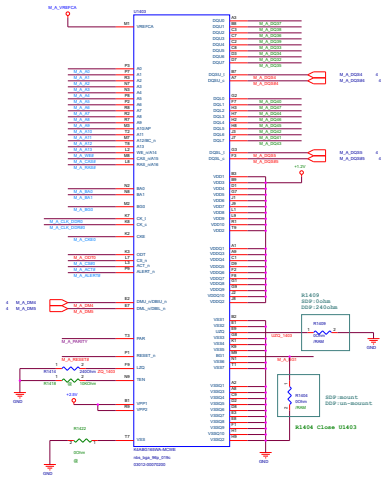
DQS0~DQS1(DQ0~DQ15)



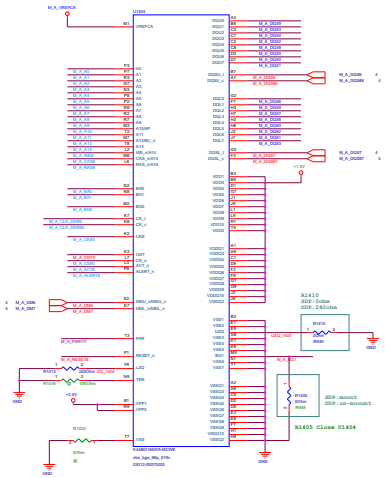
DQS2~DQS3(DQ16~DQ31)



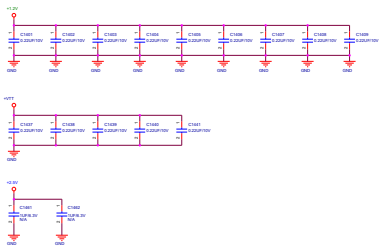
DQS4~DQS5(DQ32~DQ47)



DQS6~DQS7(DQ48~DQ63)



Close U1401



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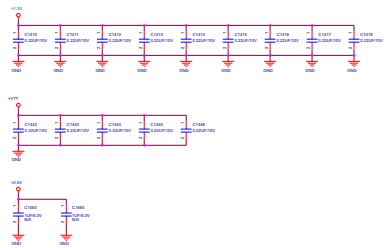

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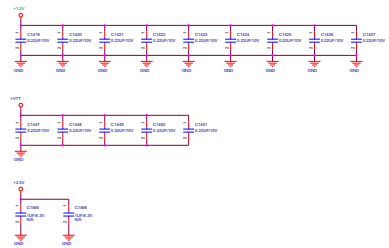
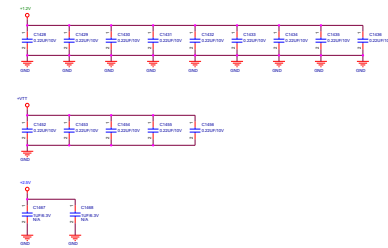


Close U1404



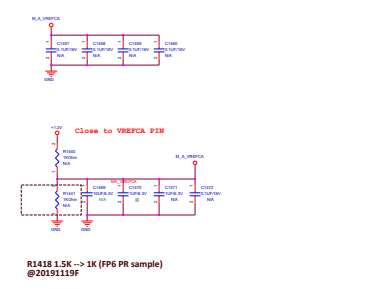
CHANNEL A and B						
MEM VREFCA	Vref Source	Connected to the center of a 50% VDDIO voltage divider network, comprised of:	2	1 k	Ω	1%
VDDIO[1]	Channel A and B Decoupling	Ceramic capacitors connected to VSS.	36	0.22	µF	0402
VTT[1]		Ceramic capacitors connected to VSS and VDDIO.	20	0.22	µF	0402
VREF_CA[1]		Ceramic capacitors connected to VDDIO.	4	0.1	µF	0402

Note: *1. Double the capacitor quantity for DRx16 configuration.*

X16 DDP

7	8	9
UDQS_c	VSSQ	VDDQ
UDQS_t	UDQ1	VDD
UDQ3	UDQ5	VSSQ
UDQ7	VSSQ	VDDQ
LDM_n/LDBI_n	VSSQ	UZQ
LDQ1	VDDQ	LZQ
VDD	VSS	VDDQ
LDQ3	LDQ5	VSSQ
LDQ7	VDDQ	VDD
CK_t	CK_c	VSS
CS_n	RAS_n/A16	VDD
A12/BC_n	CAS_n/A15	BG1
A3	BA1	TEN
A1	A5	ALERT_n
A9	A7	VPP
VSS	A13	VDD

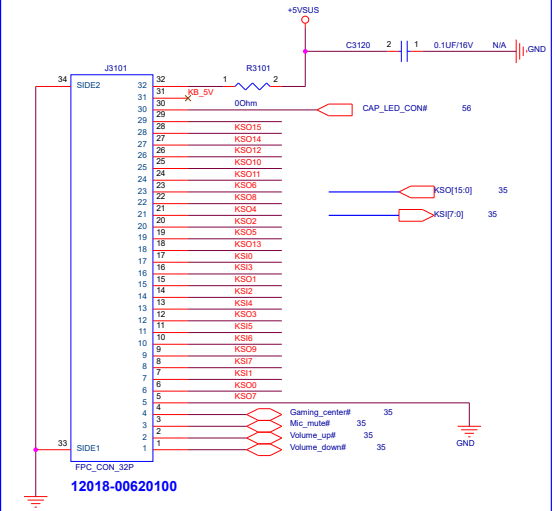
X16 SDP



R1418 1.5K --> 1K (FP6 PR sample)
@20191119F

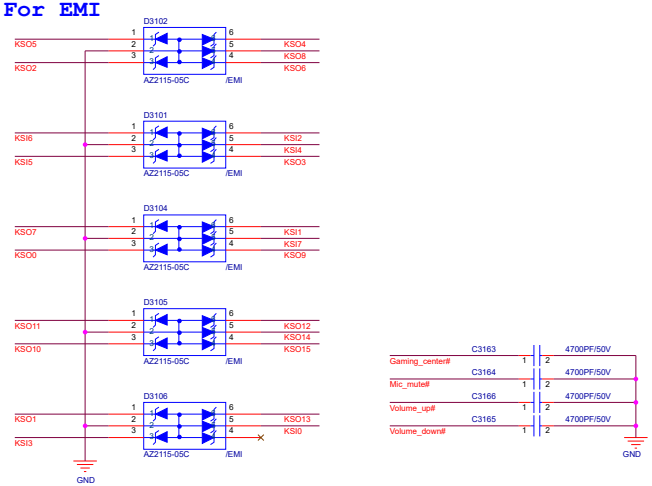
Title : DDR4_ON-BOARD_A1
Engineer: EE
GX5G2GX

Keyboard Connector(GU503)



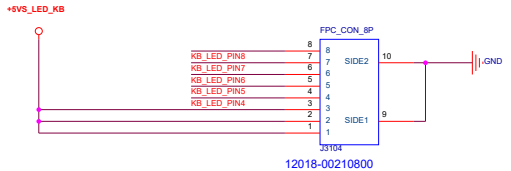
12018-00620100

For EMI

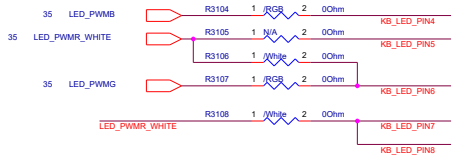


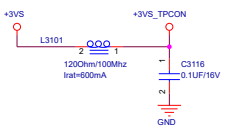
Keyboard Backlight

WHITE

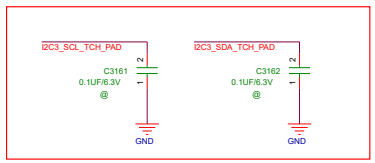


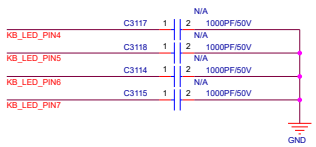
12018-00210800





EMI Reserve
如要上件請確認容值(選擇Pico等級)

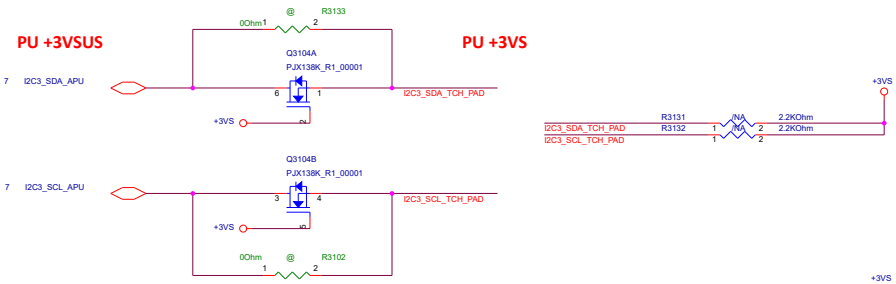




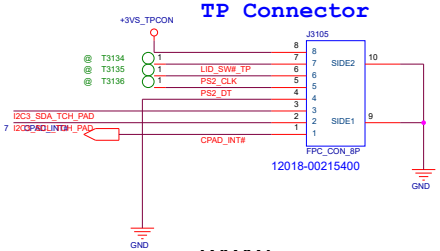
	White	RGB
R3104	@	N/A
R3106	N/A	@
R3107	@	N/A
R3108	N/A	@

PU +3VSUS

PU +3VS



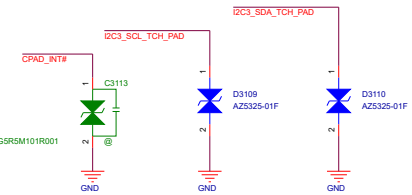
TP Connector

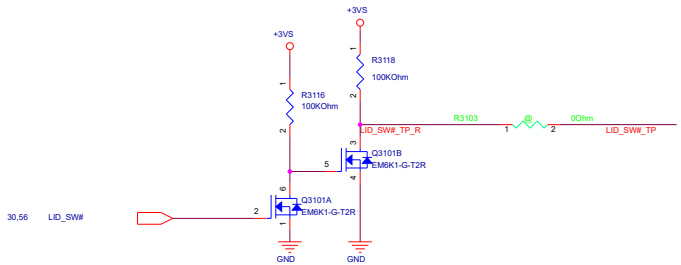


12018-00215400

WWW

	White	RGB
PIN 8	White	NC
PIN 7	White	NC
PIN 6	White	Cathode LED1 Green
PIN 5	White	Cathode LED1 Red
PIN 4	NC	Cathode LED1 Blue
PIN 3	VCC	VCC Blue
PIN 2	VCC	VCC Red
PIN 1	VCC	VCC Green





<Core Design>

ASUSTeK COMPUTER

Title : KBC_KB & TP

Engineer: EE

Size	Project Name	Rev
Custom	GA503QS	R1.2

TP Connector

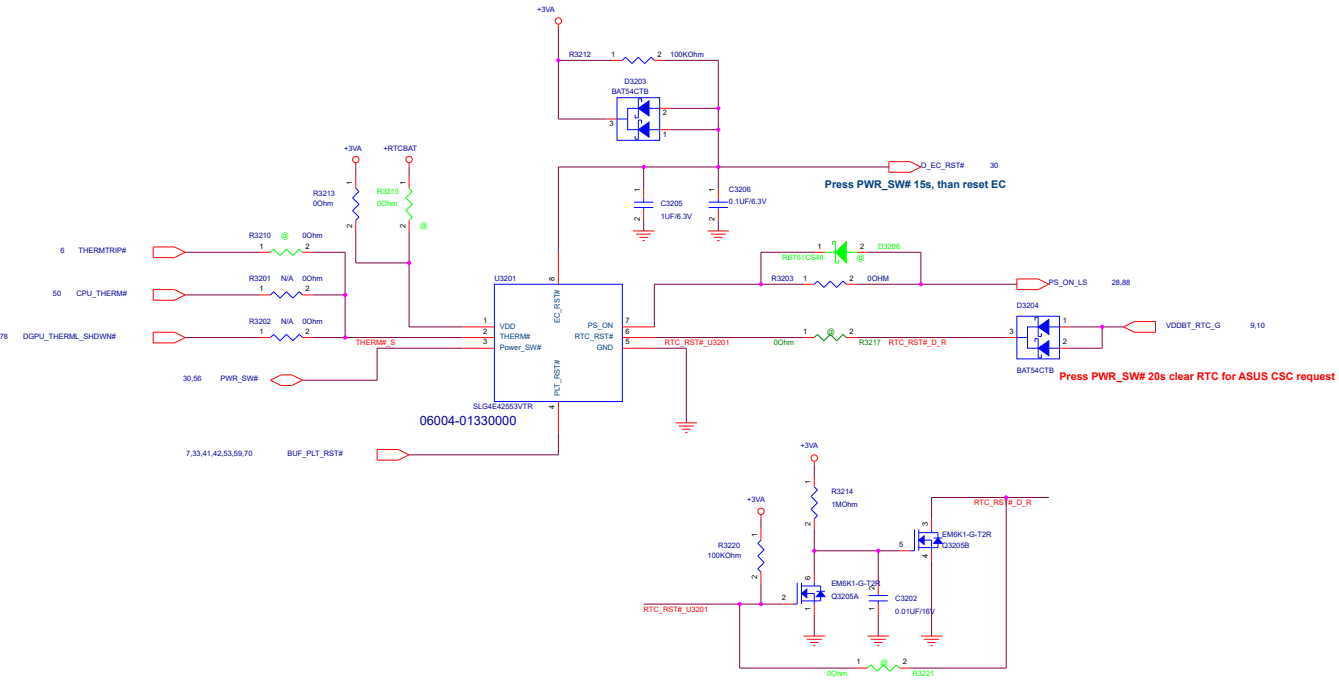
Date: Tuesday, October 13, 2020 Sheet 31 of 104

Modern standby project should use Silego solution for EC/RTC reset (Microsoft hardware requirements)

6.6.2 Power button behavior

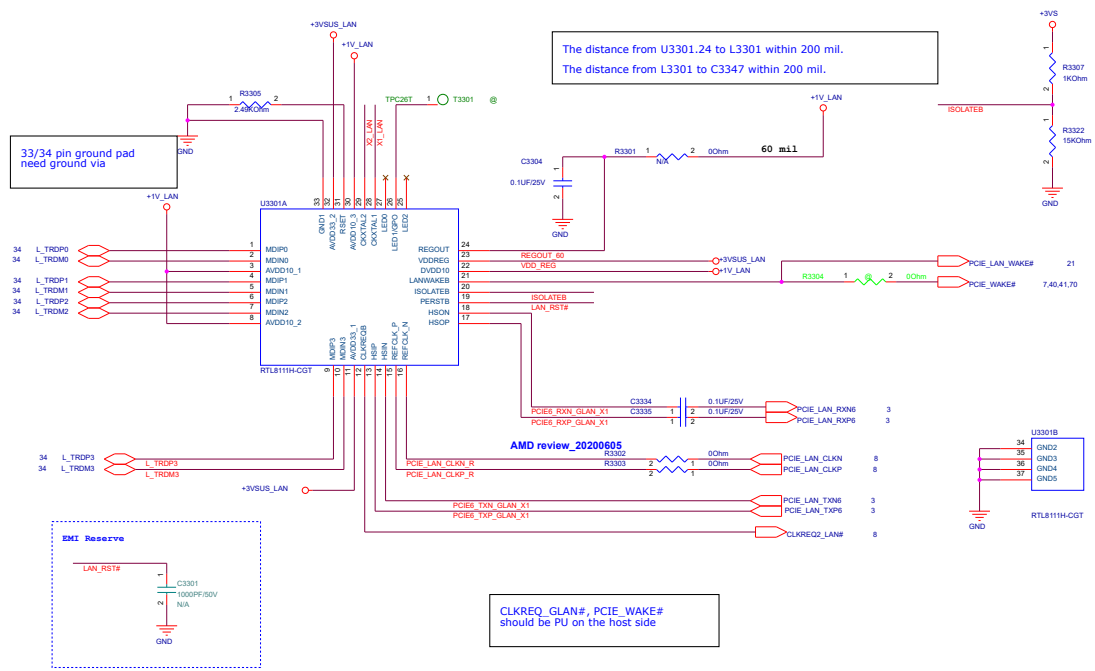
https://docs.microsoft.com/en-us/windows-hardware/design/minimum/minimum-hardware-requirements-overview#section-60---shared-minimum-hardware-requirements-for-components

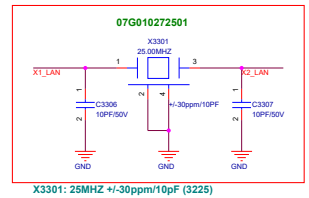
UX362FA R1.3 board will verify this circuit 7/E



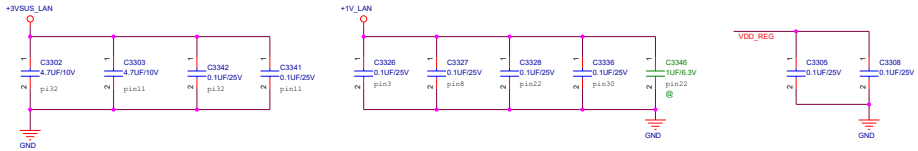
<Variant Name>

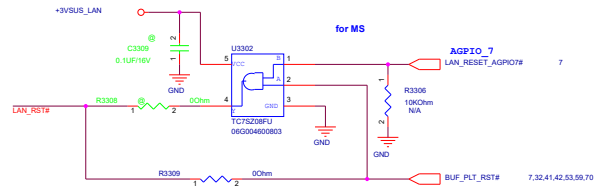
ASUSTeK COMPUTER INC. NB4	Title : RST_Reset Circuit	
	Engineer: SZNB1	
Size: C	Project Name: GA503QS	Rev: R1.0
Date: Tuesday, October 13, 2020	Sheet 32 of 104	





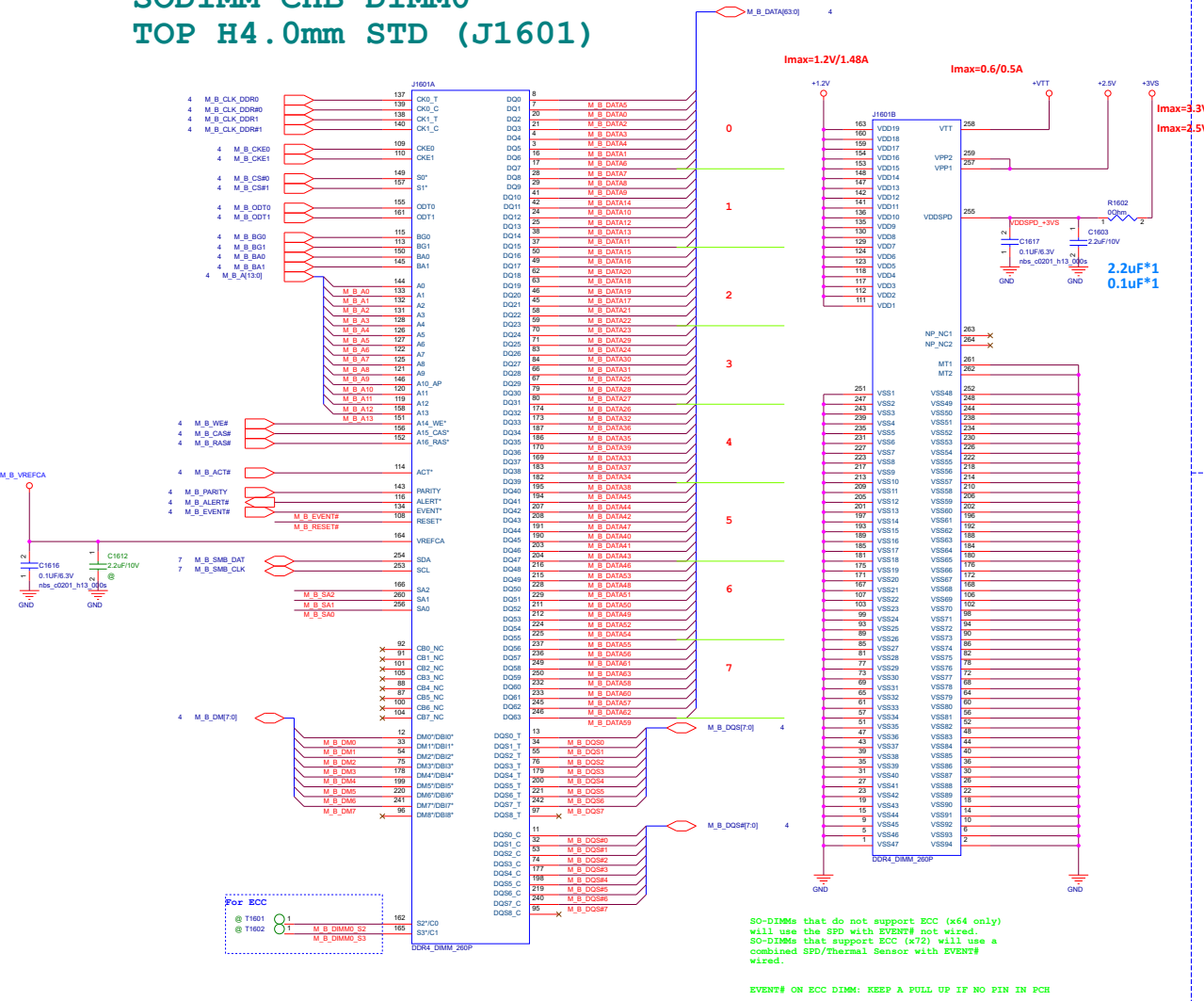
Realtek suggests 3V_LAN raise time >1ms

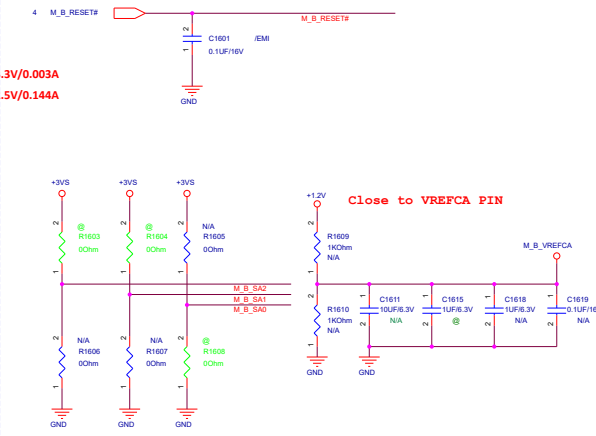


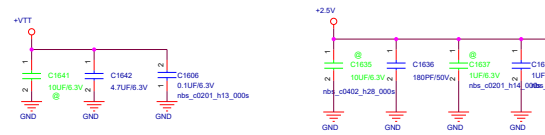


Project Name	GA503QS
Rev	R1.2
Title :	LAN RTL8111GUX-CG
Size	C
Dept.:	ASUSTeK COMPUTER
Engineer:	EE
Date:	Tuesday, October 13, 2020
Sheet	33 of 104

SODIMM CHB-DIMM0
TOP H4.0mm STD (J1601)

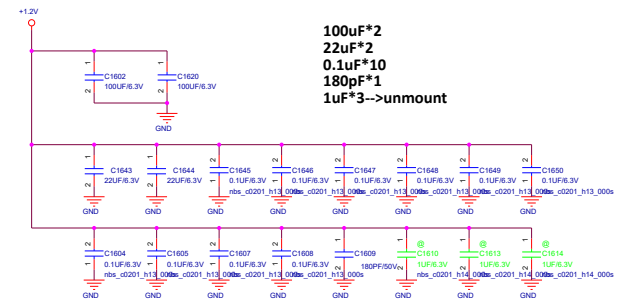






10uF*1-->unmount
0.1uF*1
4.7uF*1

10uF*1-->unmount
1uF*2-->*1 unmount
0.1uF*2
180pF*1

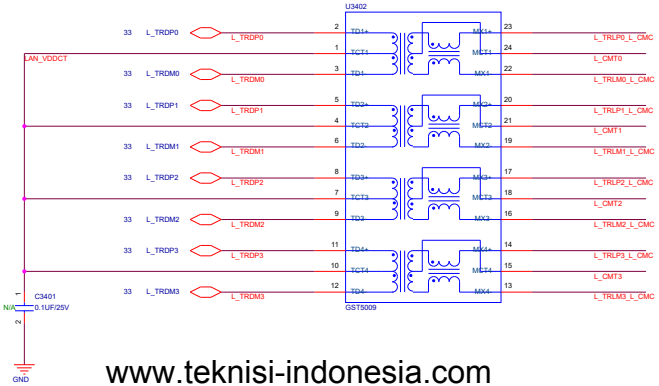


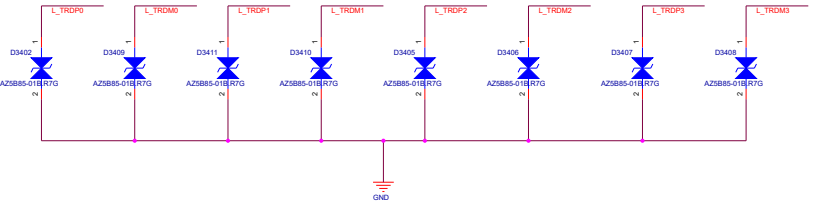
100uF*2
22uF*2
0.1uF*10
180pF*1
1uF*3-->unmount

Table 4-24. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM **1DPC**	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Placed on VTT plane close to DIMM, 1 cap stuffed, 1 placeholder	2x 10µF (0603)	
		Placed on VTT plane close to DIMM	4x 1µF (0402)	
	VPP	DIMM Pin side, 1 per DIMM	2x 10µF (0603)	
		DIMM Pin side, 1 per DIMM	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	2x 0.1µF (0402)	
		Place close to DIMM	2x 2.2µF (0402)	

DDR4 - 2666MHz (8G)
1st : Hynix - 03A08-00051400
2nd : Samsung - 03A08-00051300
DDR4 - 2666MHz (16G)
1st : Hynix - 03A08-00061400
2nd : Samsung - 03A08-00061500

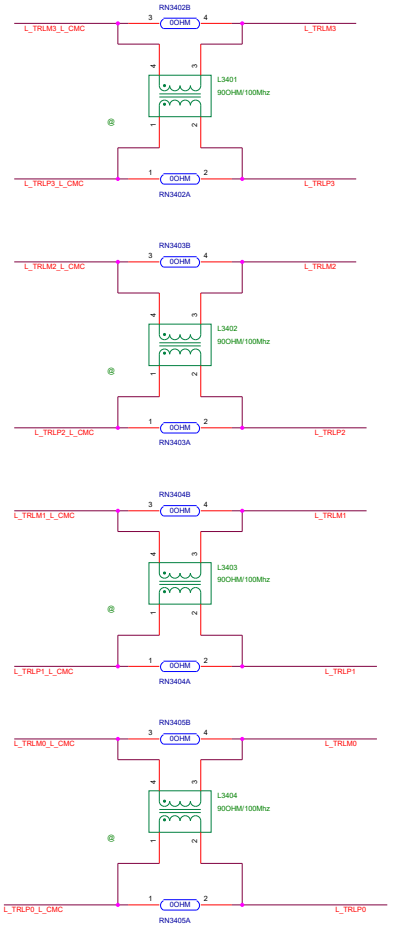


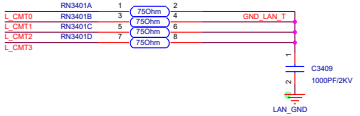


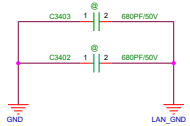
D3401,D3402 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

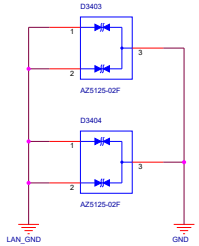
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D



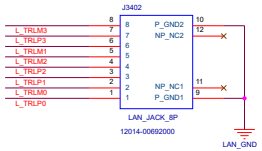




Place near chassis GND



LAN Connector



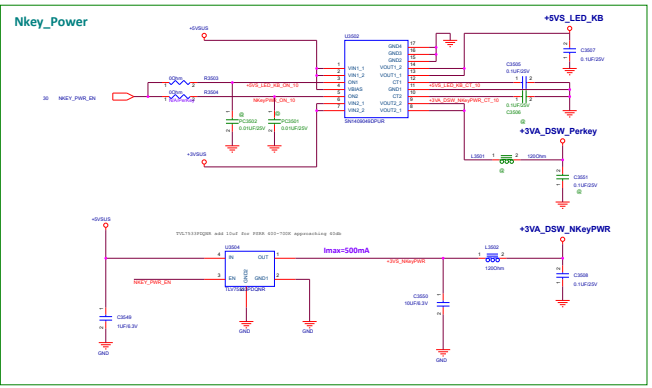
Project Name: GU502DU			Rev: 1.0
Title : LAN_RJ45_CON			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: NB1 RD2 EE1	
Date: Tuesday, October 13, 2020	Sheet 34 of 104		

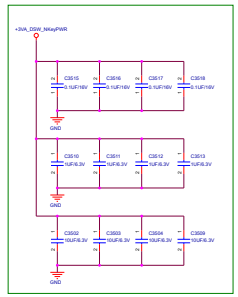
N_KEY_IT8299E

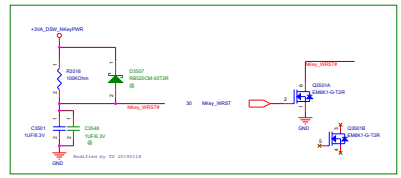
Nkey_Power_Cap

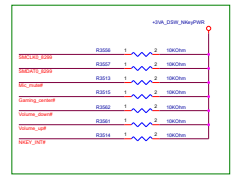
For EC Reset N_key

Pull up

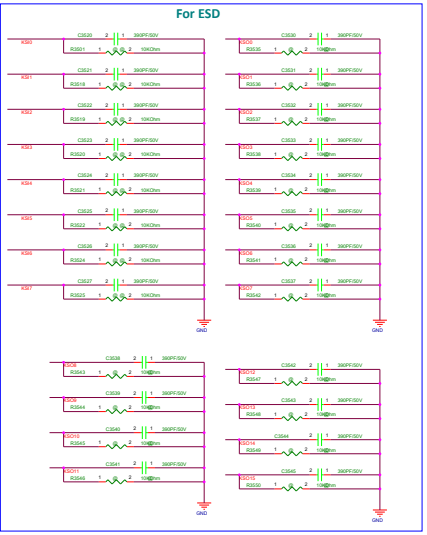


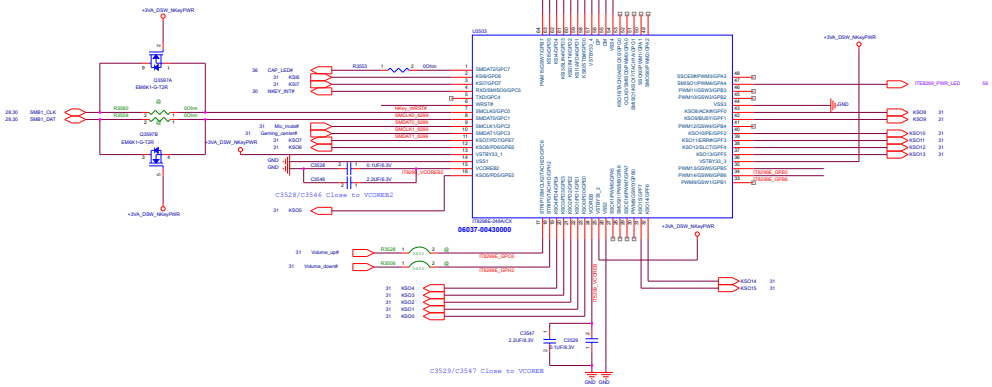


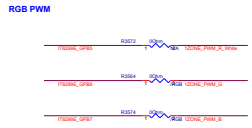


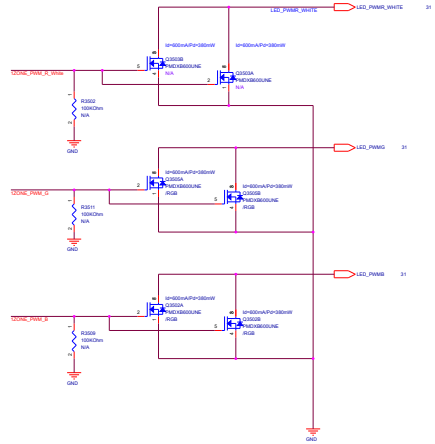


IT8259E-248A/CX
P/N:06037-00430000









*** POWER

** [R.88] +3VS
** [R.87] +3VSUS
** [R.87] +1.8VS
** [R.84] +1.8VSUS
** [R.88] +5VS
** [R.87] +5VSUS
** [R.87] +12VS
** [R.87]
+3VA_EC

*** SINGAL

** PCH Control

7 A_Z_BITCLK
7 A_Z_SYNC
7 A_Z_SDIN0
7 A_Z_SDOUT

** EC Control

30 AMP_SLEEP#
30 OP_SD#

** Jack Control

37 EAPD#
37 TOU_CON_L

*** To EXT. Amp.

39 I2S_Codec_SDIN
39 I2S_Codec_SDOUT
39 I2S_BCLK
39 I2S_LRCLK

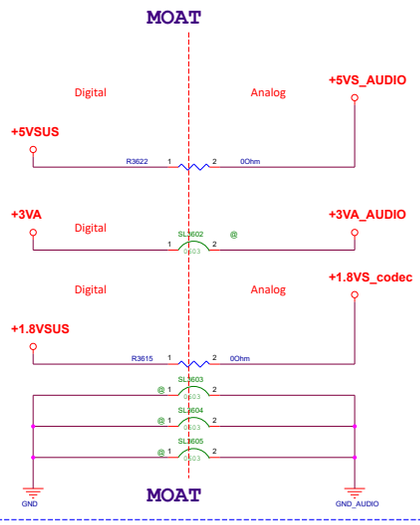
*** Headset Connection

37 LINE1_R
37 LINE1_L
37 MIC2_R_SLEEVE
37 MIC2_L_RING2
37 MIC2_VREFO_R
37 MIC2_VREFO_L
37 HPOUT_L
37 HPOUT_R

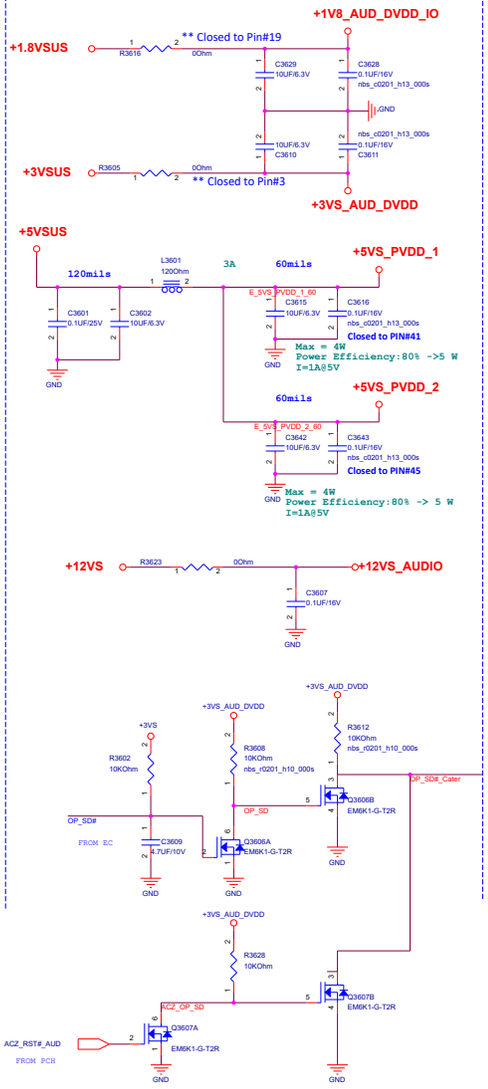
*** Tweeter AMP CONN Connection

39 H_SPK2L+_CON
39 H_SPK2L-_CON
39 H_SPK2R-_CON
39 H_SPK2R+_CON

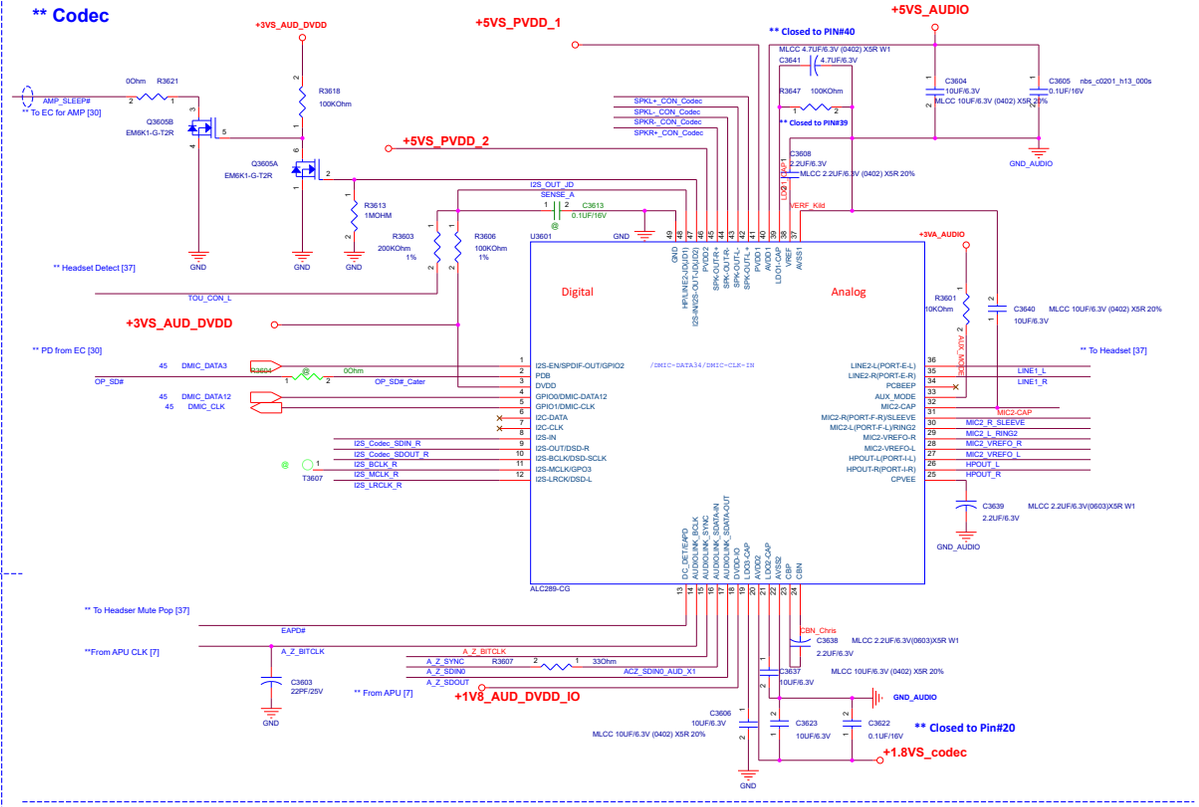
** PWR DISTRIBUTION (ANALOG)



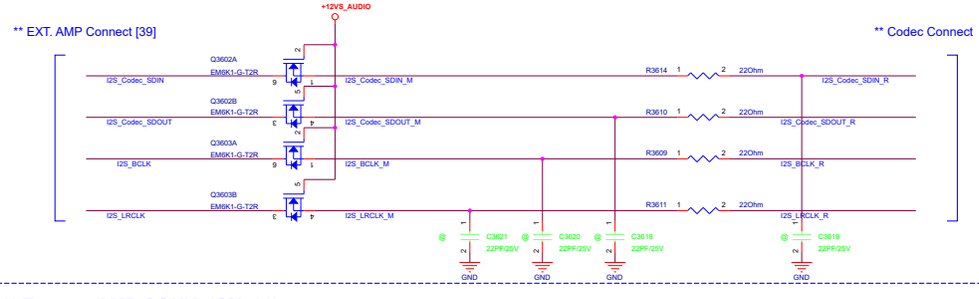
** PWR DISTRIBUTION (DIGITAL)



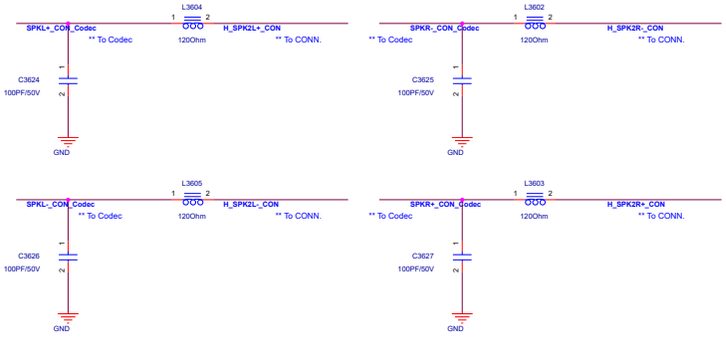
** Codec



** EXT. AMP Connection



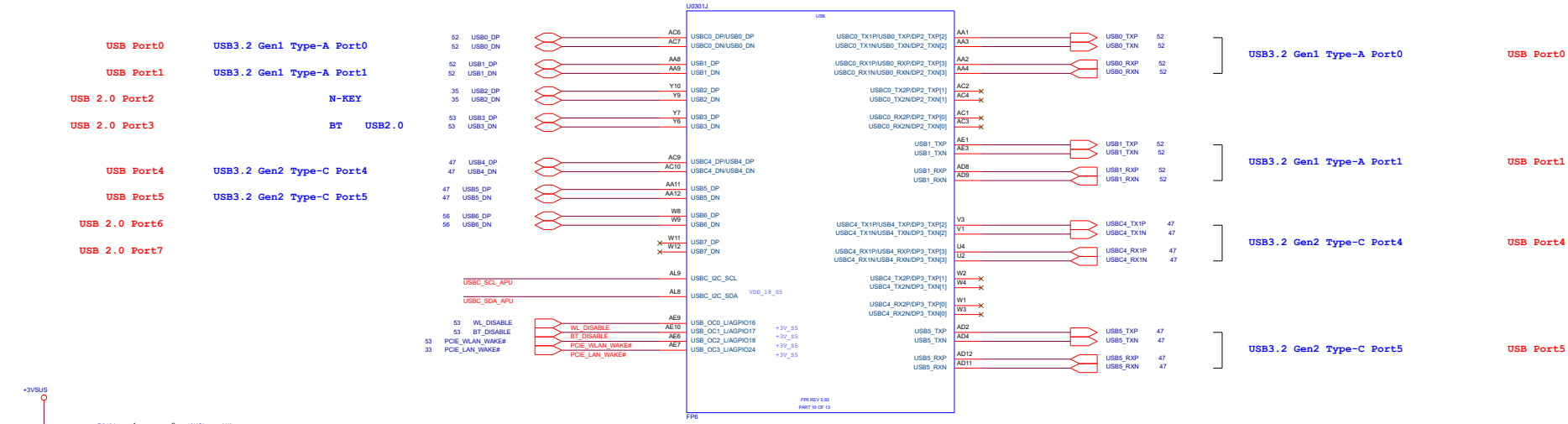
** Tweeter AMP CONN. (GU502)



<Core Design>

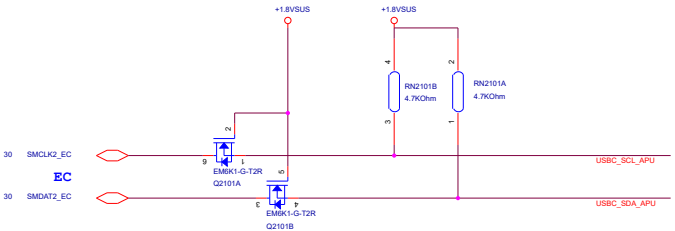
ASUS	Project Name: GA503QS	Rev: R1.3
Title : AUD-ALC285		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1
Date: Tuesday, October 13, 2020	Sheet 36 of 104	

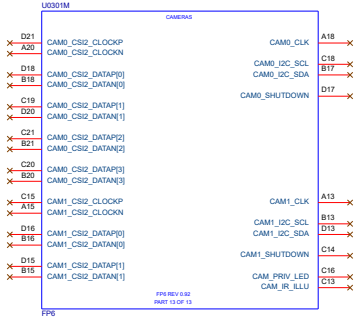
CPU_USB



AMD Design check

AGPIO13. If unused, enable internal pull down by software.





<Variant Name>

ASUS	Project Name: GA503QS	Rev: R1.0
Title :		
Size: Custom	Dept.: ASUSTeK COMPUTER INC. Engineer:	
Date: Tuesday, October 13, 2020	Sheet 21 of 104	

Title <Title>		
Size A	Document Number GA503QS	Rev <RevCode>
Date: Tuesday, October 13, 2020	Sheet 22 of 104	

Title <Title>		
Size A	Document Number GA503QS	Rev <RevCode>
Date: Tuesday, October 13, 2020	Sheet 25 of 104	

<Variant Name>

Title <Title>		
Size B	Document Number GA503QS	Rev <RevCode>
Date: Tuesday, October 13, 2020	Sheet 27 of 104	

*** POWER

** [P.36] +12VS_AUDIO

** [P.30] +3VA_EC

** [P.36] +1V8_AUD_DVDD_IO

*** SINGAL

** Line to Codec [36]

36 LINE1_R
36 LINE1_L

** Headset from Codec [36]

36 HPOUT_R
36 HPOUT_L
36 MIC2_VREFO_L
36 MIC2_L_RING2
36 MIC2_R_SLEEVE
36 MIC2_VREFO_R

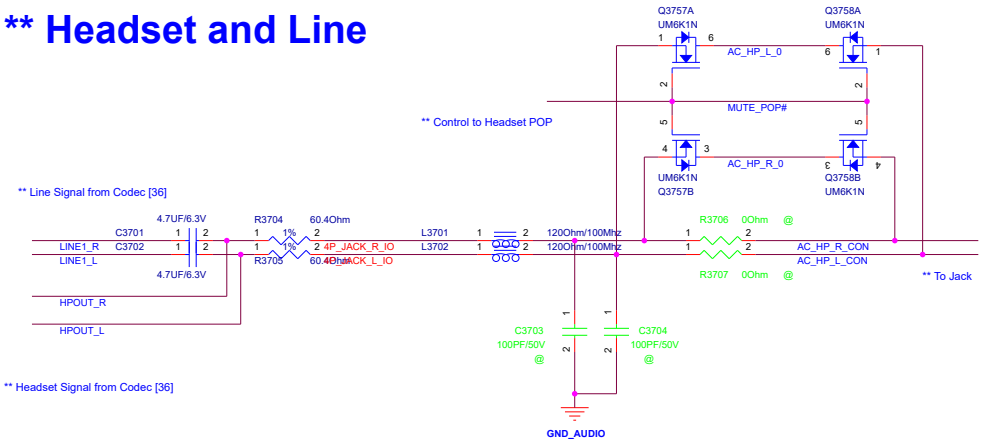
** Control Pin from Codec [36]

36 EAPD#
36 TOU_CON_L

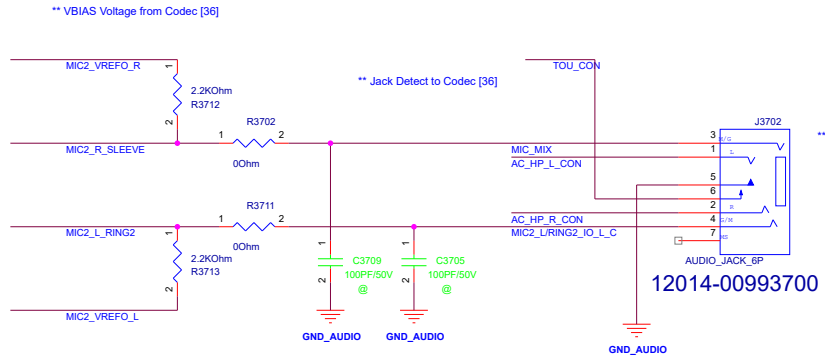
** Control Pin from APU [7]

7,36 ACZ_RST#_AUD

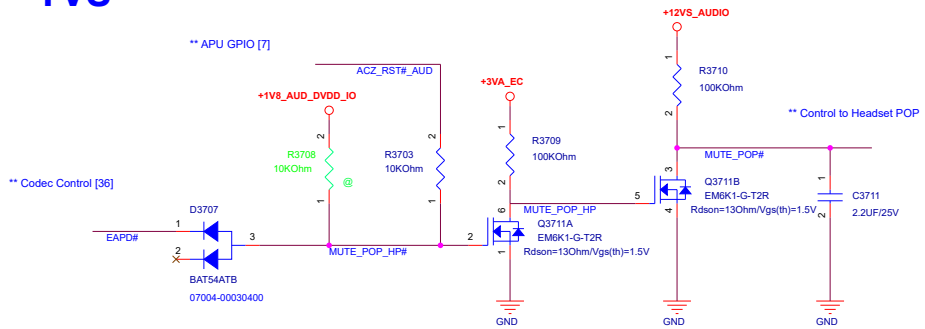
** Headset and Line



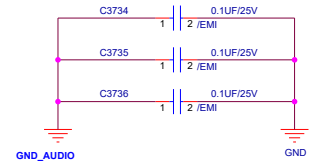
** Jack and MIC



** TVS



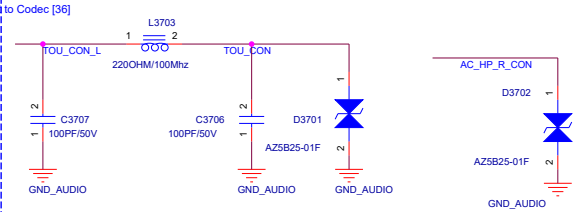
** A_GND / GND



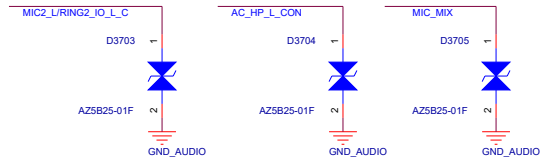
** TVS

HP & MIC Connector

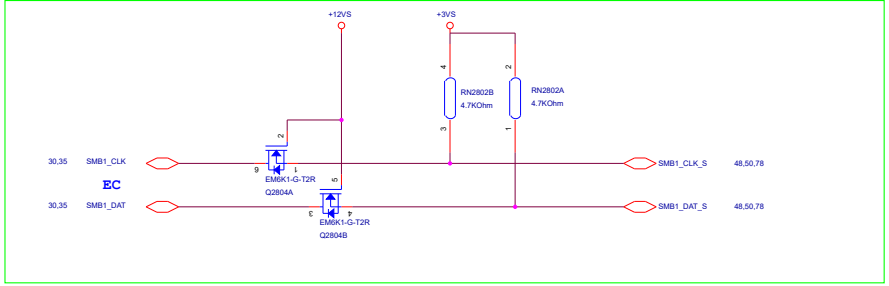
HP ESD Protect

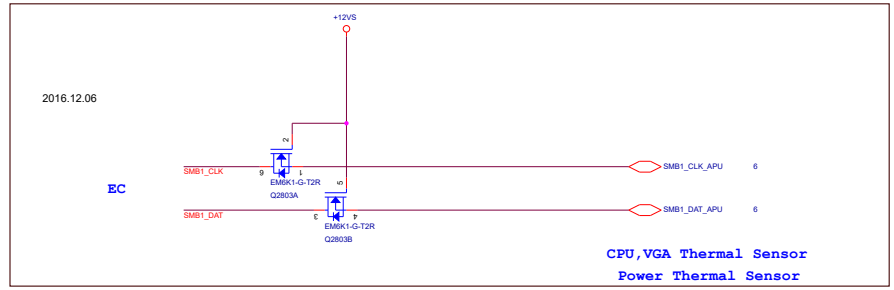


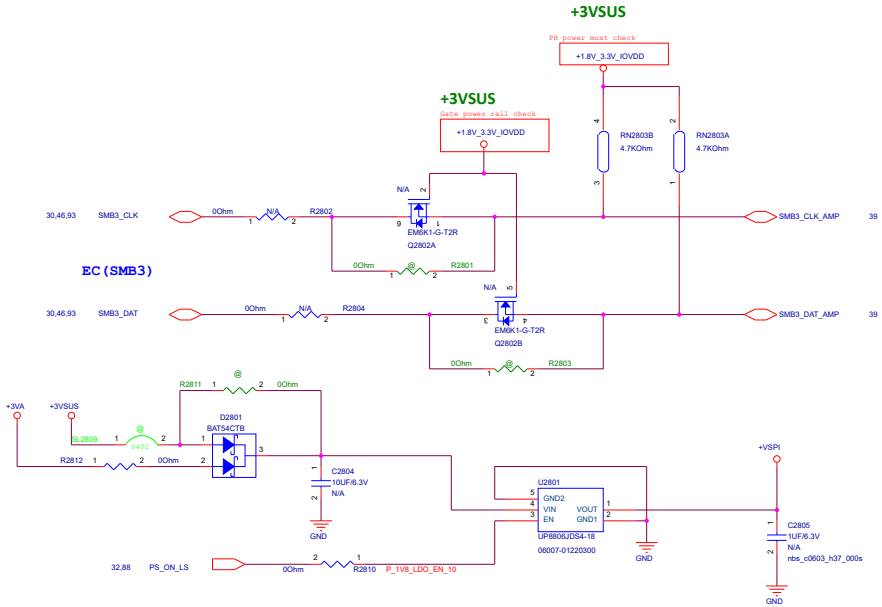
EXTERNAL MICROPHONE

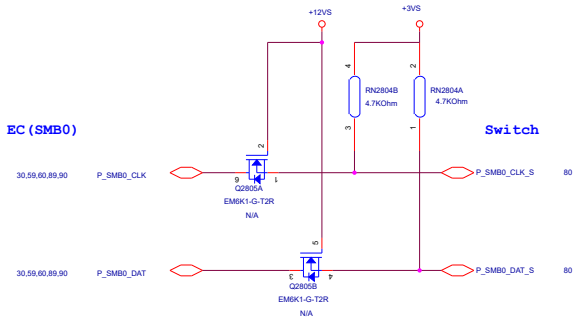


ASUS	Project Name: GA503QS	Rev: R1.2
Title : AUD_EXT Jack		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Date: Tuesday, October 13, 2020	Sheet 37 of 104	









NKEY_預留0 OHM對接

EC_PU +3VA

EC (SMB1) —— Isolation —— +3VS

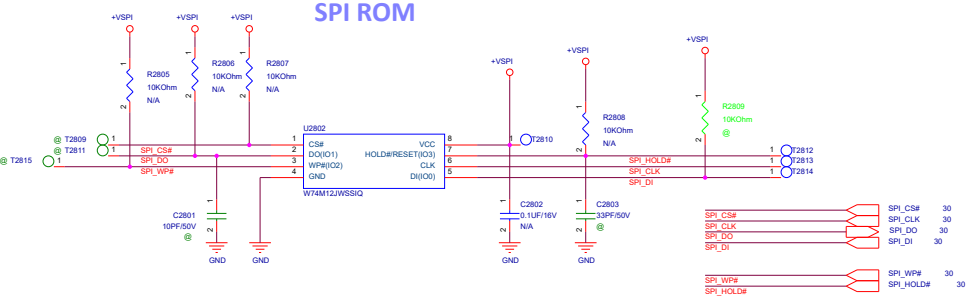
GPU sensor

VRAM sensor

CPU sensor

HDMI_預留

SPI ROM



APU I2C3_PU +3VSUS

DDR4 SO-DIMM_對接

EC (SMB3)

Type-C PD

Slave charger

EC (SMB3) —— Isolation —— +3VSUS

M_B_SMB_DAT —— SMB3_CLK_AMP

Audio AMP

ASUS	Project Name: GA503QS		Rev: 1.0
Title : PCH-SPI ROM,OTH			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Tuesday, October 13, 2020	Sheet 28 of 104		

<Core Design>

Title : Aud_HP Jack, MIC

ASUSTeK COMPUTER INC. NB1

Engineer: EE

Size	Project Name	Rev
Custom	GA503QS	1.0

Date:	Tuesday, October 13, 2020	Sheet	38	of	104

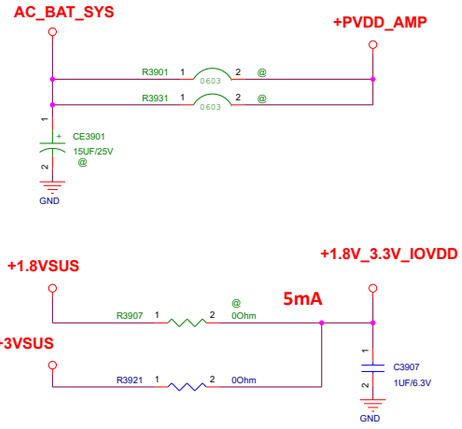
*** POWER

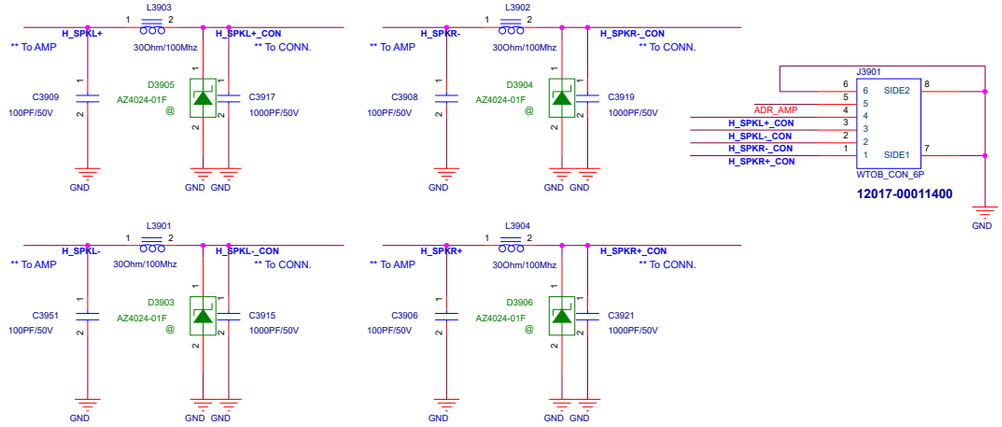
AC_BAT_SYS

+1.8VSUS

+3VSUS

** PWR DISTRIBUTION





*** SINGAL

** from EC [36]

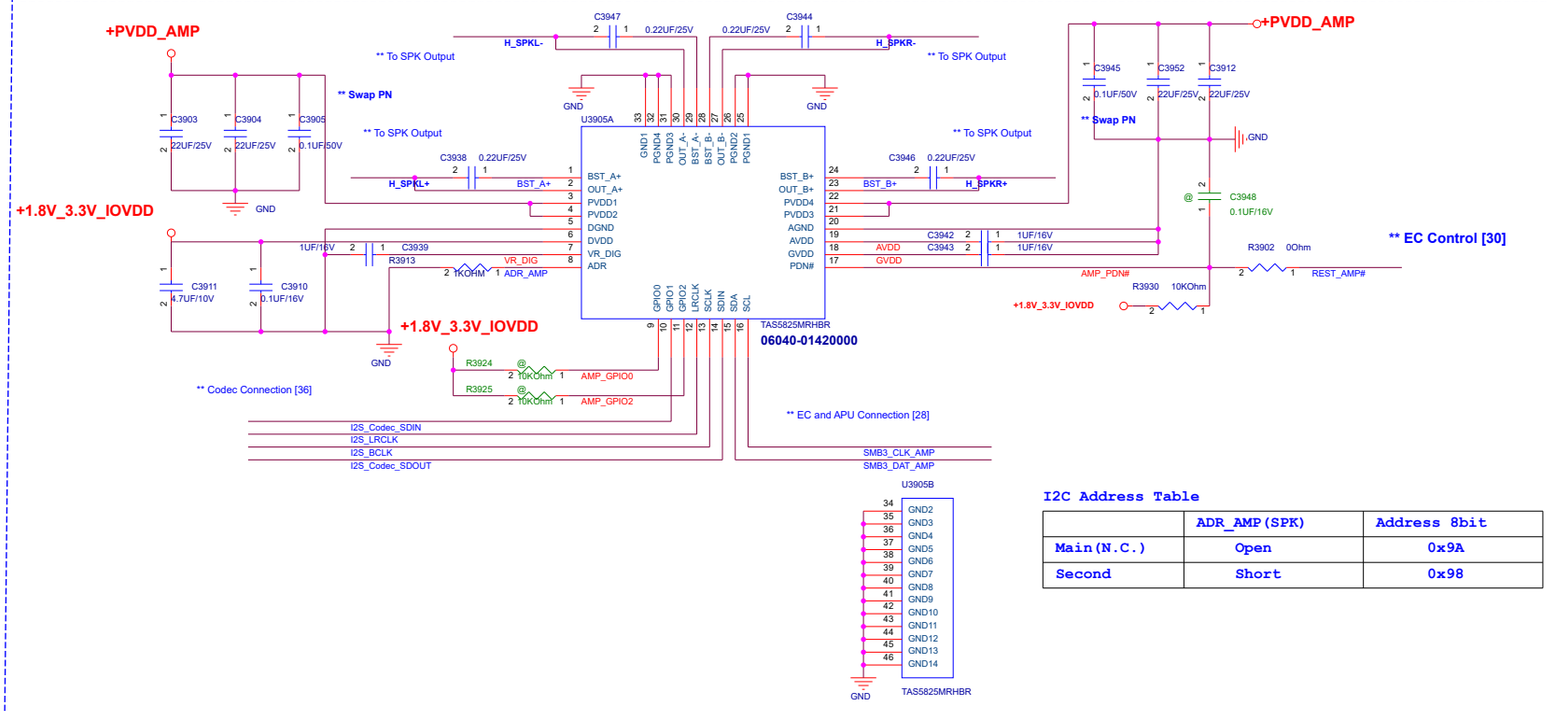
30 REST_AMP# → REST_AMP#

** from Codec [36]

36 I2S_Codec_SDIN → I2S_Codec_SDIN
36 I2S_LRCLK → I2S_LRCLK
36 I2S_BCLK → I2S_BCLK
36 I2S_Codec_SDOUT → I2S_Codec_SDOUT

** from EC and APU [28]

28 SMB3_CLK_AMP → SMB3_CLK_AMP
28 SMB3_DAT_AMP → SMB3_DAT_AMP



I2C Address Table

	ADR_AMP(SPK)	Address 8bit
Main(N.C.)	Open	0x9A
Second	Short	0x98

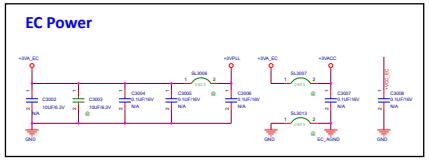
Tweeter SPK

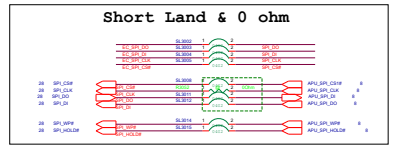
** from Codec smart AMP

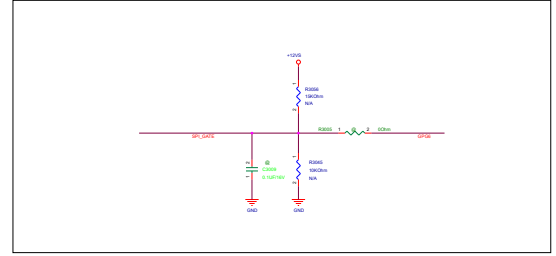
36 H_SPK2L+_CON
36 H_SPK2L-_CON
36 H_SPK2R-_CON
36 H_SPK2R+_CON

ASUS	Project Name: GA503QS		Rev: R1.2
Title : AUD_INT SPK			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE	
Date: Tuesday, October 13, 2020	Sheet 39 of 104		

EC Chip - IT8225







VCC => +3VS system power ; LPC

VSTBY=>+3VA_EC ;Power supply of EC power

+3VACC==+3VA_EC
+3VAPLL==+3VA_EC_0906

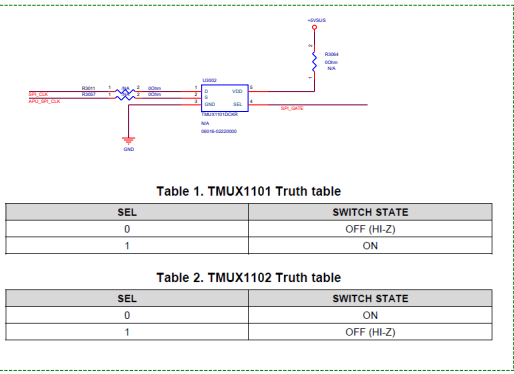
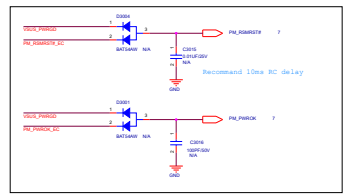


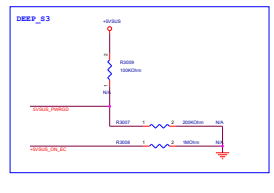
Table 1. TMUX1101 Truth table

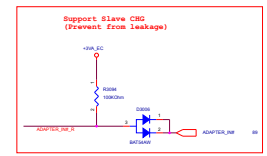
SEL	SWITCH STATE
0	OFF (HI-Z)
1	ON

Table 2. TMUX1102 Truth table

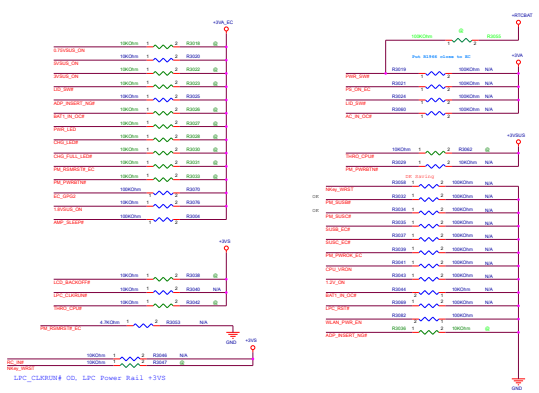
SEL	SWITCH STATE
0	ON
1	OFF (HI-Z)

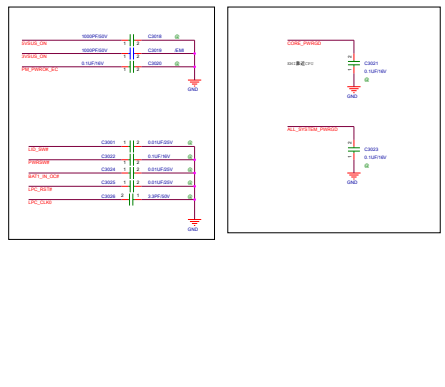


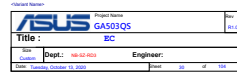


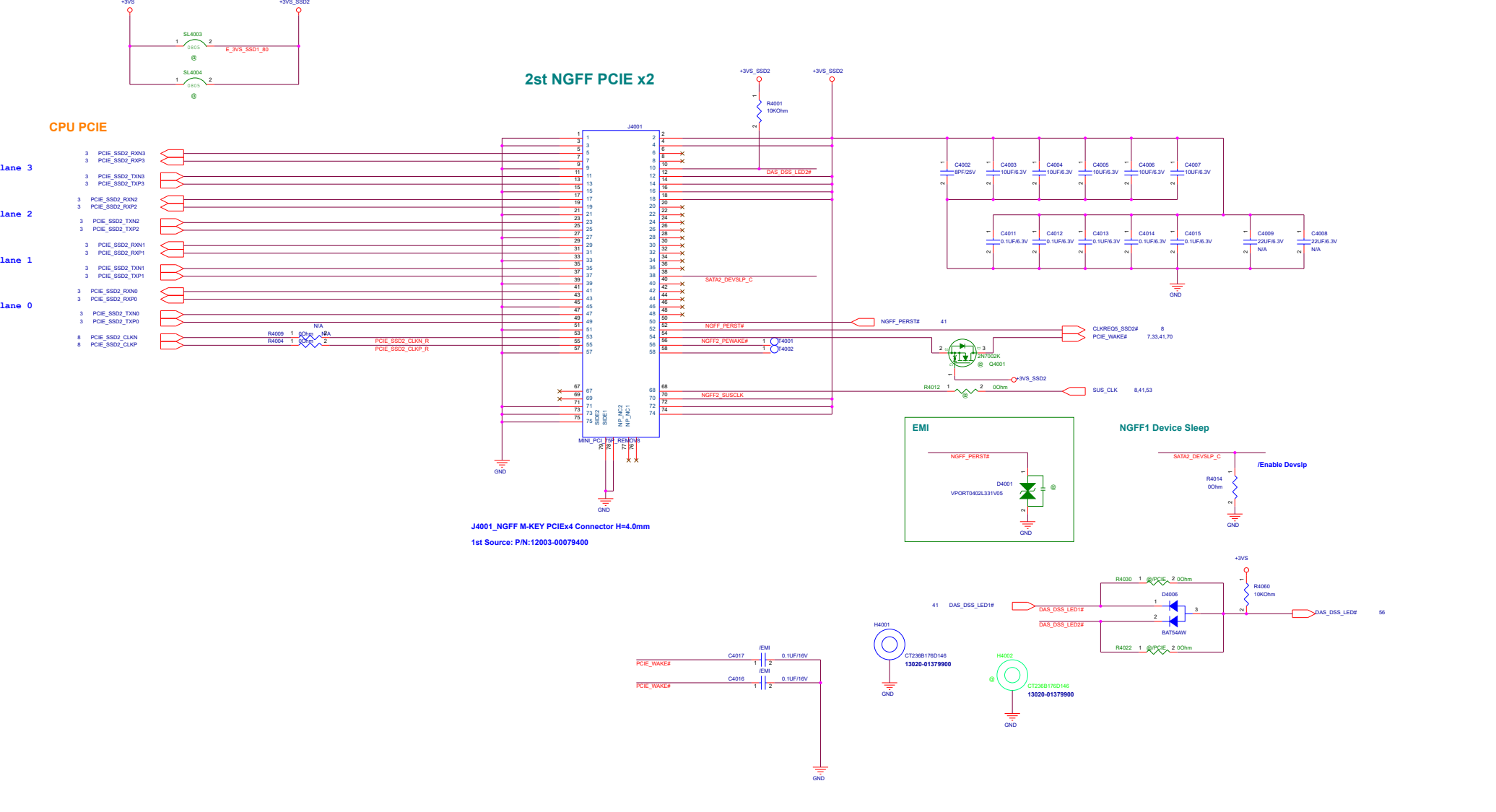


for load code



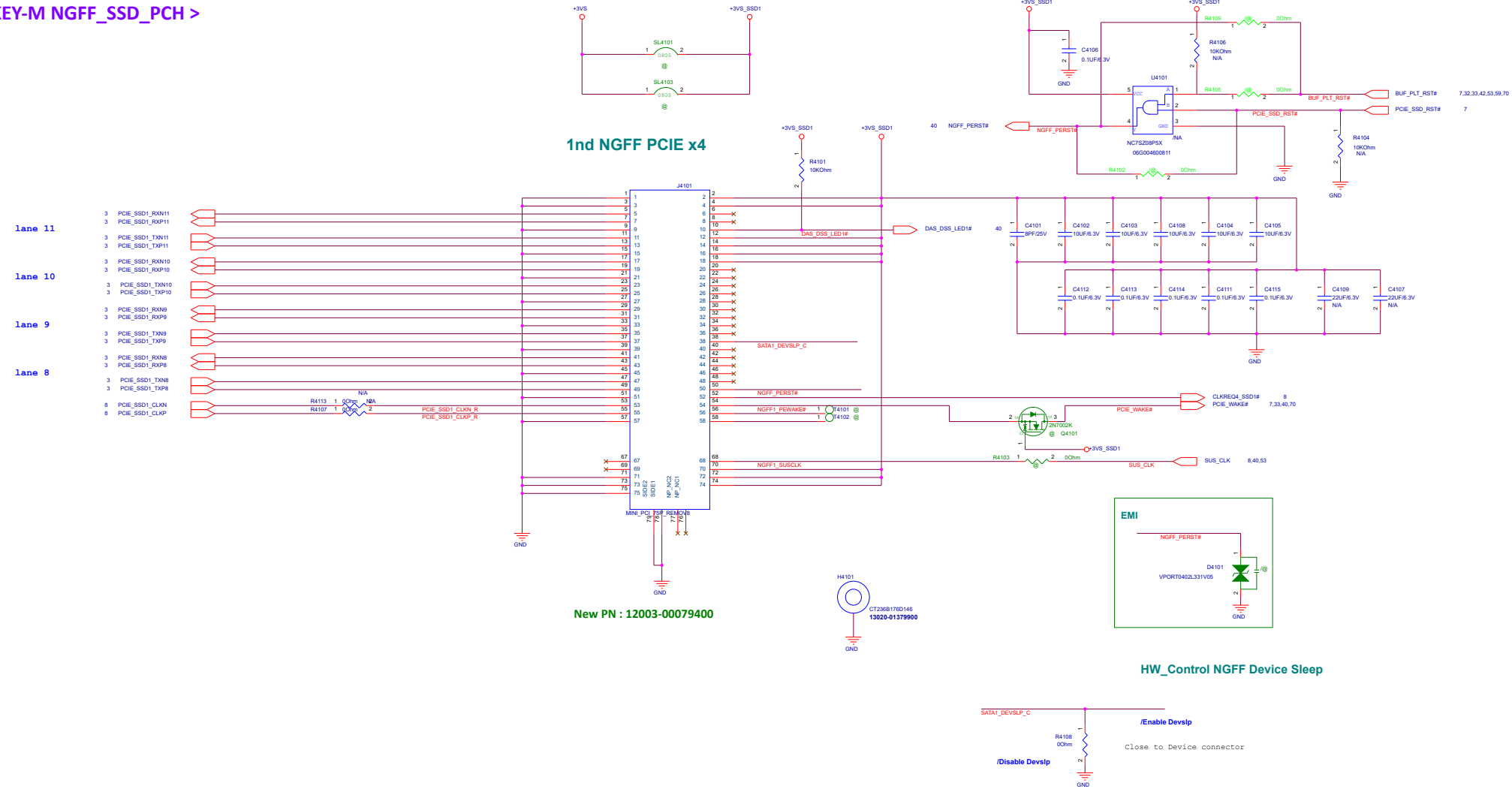






Project Name: GA503QS		Rev: 1.0
Title: NGFF_SSD_PCIE_CON		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: NB1 RD2 EE1
Date: Tuesday, October 13, 2020	Sheet 40 of 104	

< KEY-M NGFF_SSD_PCH >



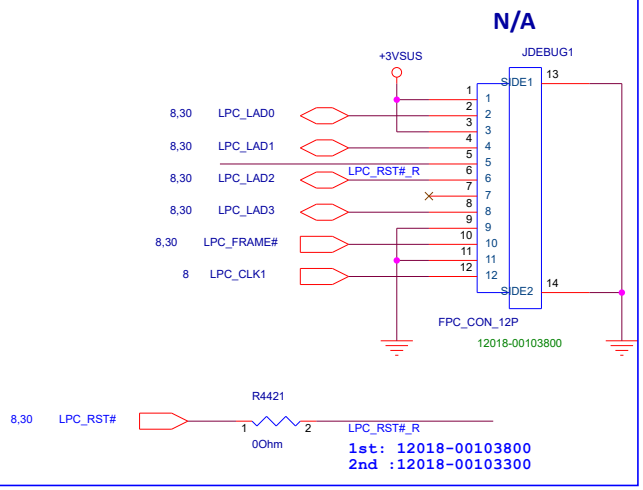
<Core Design>

ASUSTeK COMPUTER	Title : NGFF_SSD_CPU	
	Engineer: EE	
Size: C	Project Name: GA503QS	Rev: 1.0
Date: Tuesday, October 13, 2020	Sheet 41 of 104	

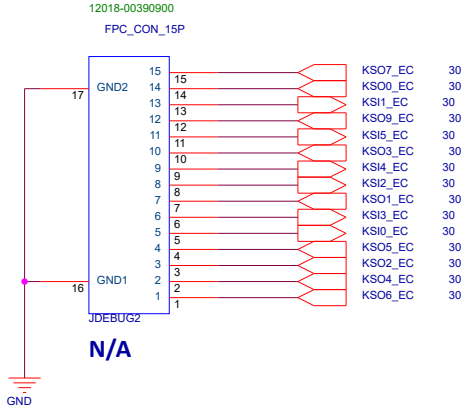
HDMI Switch

ASUS	Project Name: GA503QS	Rev: 1.0
Title : CB_CON		
Size: A3	Dept.: ADULTINK COMPUTER	Engineer: EE
Date: Tuesday, October 13, 2020	Sheet 43 of 104	

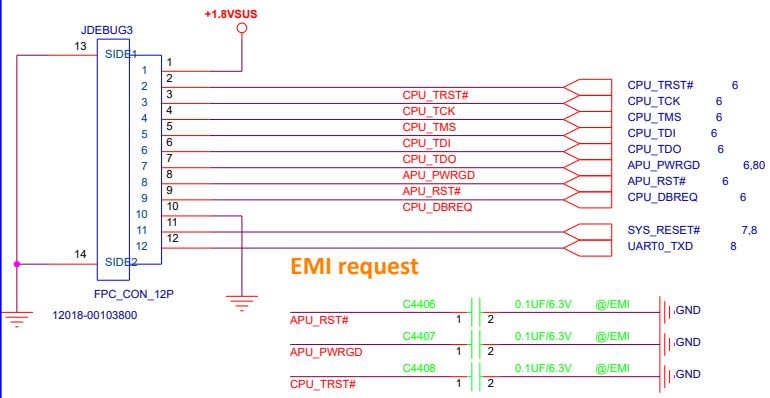
LPC Debug Port



Flash BIOS



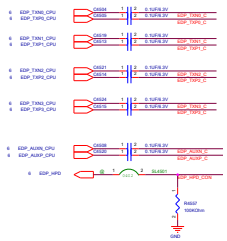
HDT + UART Debug



<Core Design>

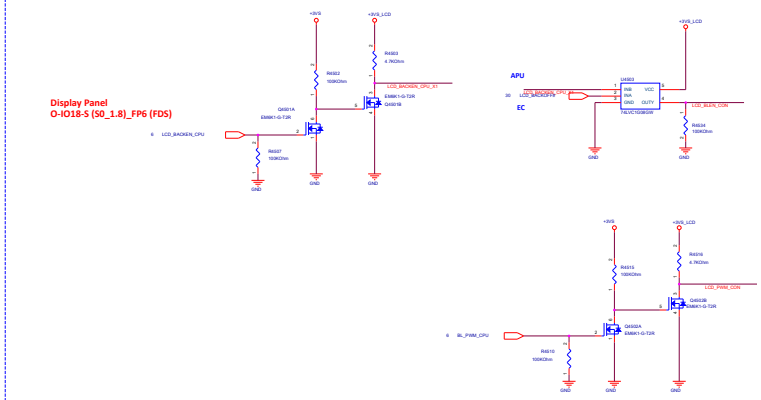
ASUSTeK COMPUTER	Title : DEBUG_LPC	
	Engineer: EE	
Size: B	Project Name: GA503QS	Rev: 1.0
Date: Tuesday, October 13, 2020	Sheet 44 of 104	

eDP from CPU

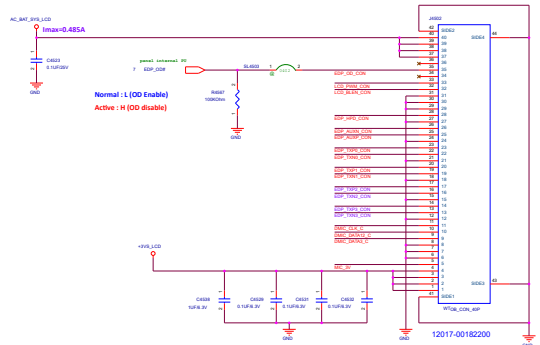


eDP BL_EN/BL_PWM

Display Panel
O-IO18-5 (S0_1.8)_FP6 (FDS)

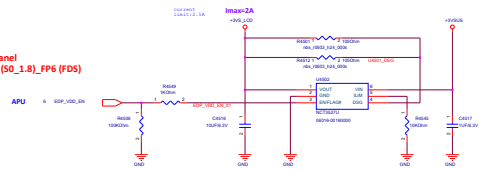


eDP Panel Conn.

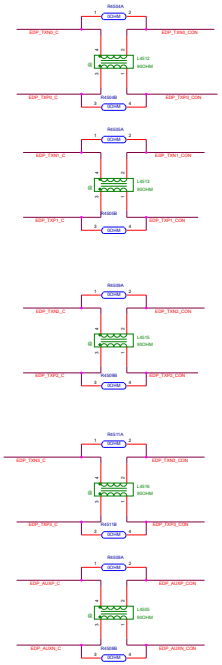


LCD Power switch

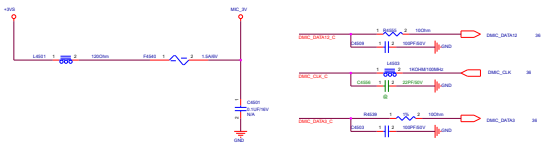
Display Panel
O-IO18-5 (S0_1.8)_FP6 (FDS)



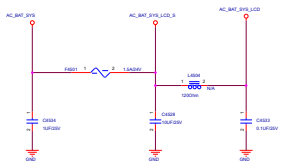
For EMI



MIC

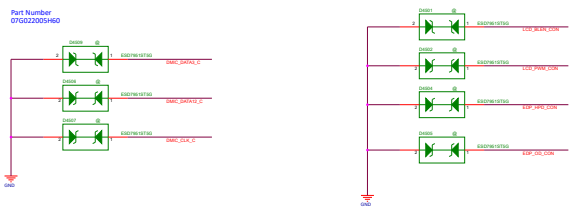


Panel BL Power



ESD Protection

Part Number
07G022005H60



<Core Design>

	Project Name **GA503QS**	Rev 1.0

Title : ANT

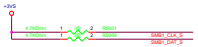
Size C	**Dept.:** ASUSTeK COMPUTER	**Engineer:** EE

Date: Tuesday, October 13, 2020	Sheet	49	of	104

Thermal Sensor : SN170027

ALERT/SDA/SCL: Open-drain output; pullup resistor 5Kohm

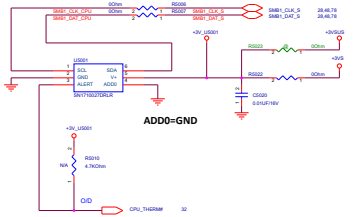
Pin function Supply voltage.: 1.62 V to 3.6 V



power rail : 3.3V

SMBUS1 to EC

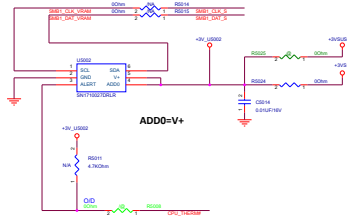
CPU



Near CPU

SMBUS addr=10010000 (90)

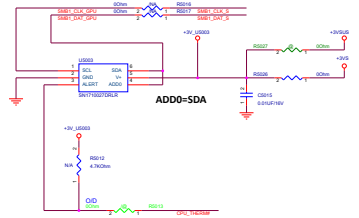
VRAM



Near VRAM

SMBUS addr=10010001 (92)

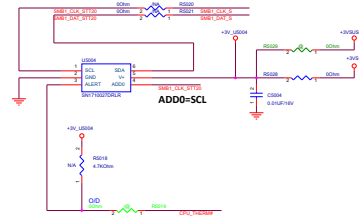
GPU



Near GPU

SMBUS addr=10010010 (94)

AMD STT2.0

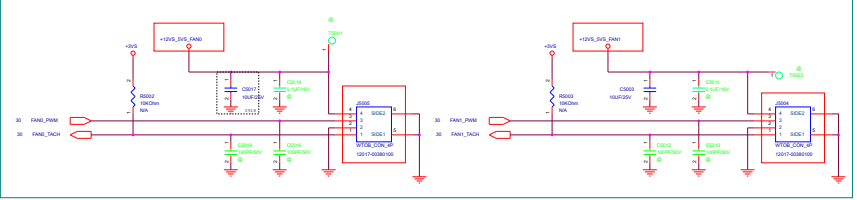


Near GPU

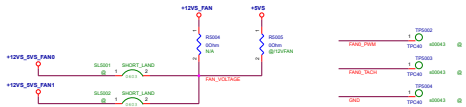
SMBUS addr=10010010 (96)

CPU&GPU FAN

Note : connector and power are by project design

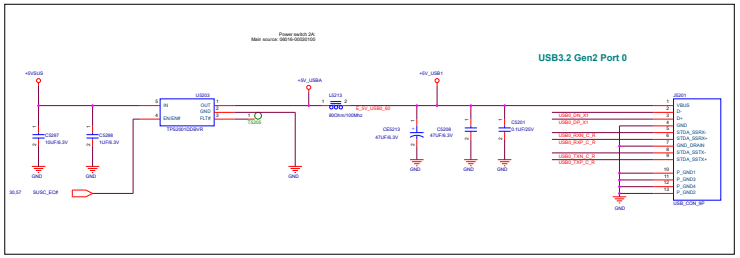


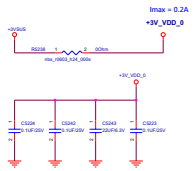
ADD0: Address select. Connect to GND, SDA, SCL, or V+



TYPE-C USB3.1

USB3.2 Port 0





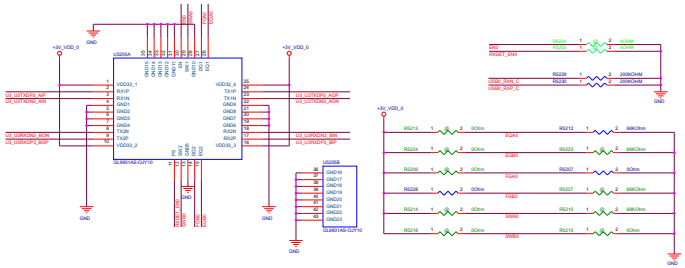
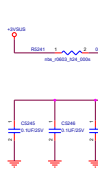
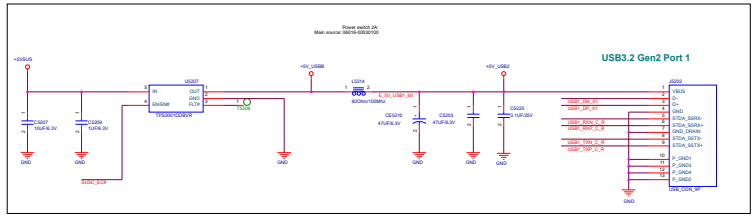


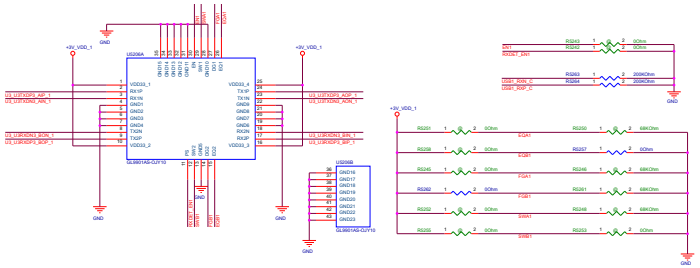
Table 4.1 - 4-leve Control Pin Settings

Setting Level	Connecting Condition
0	Tie to GND
R	Tie 68K R to GND
F	Float (Leave open)
1	Tie to VDD

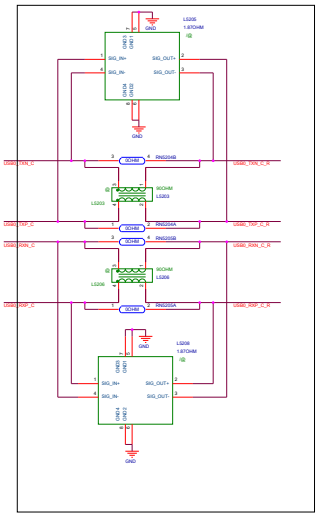
USB3.2 Port 1





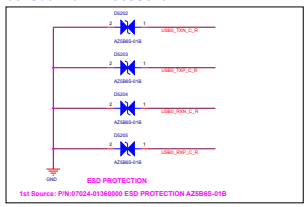


USB3.0 EMI-Protection

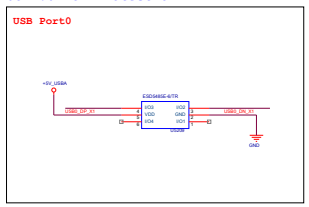


USB3.2 Gen 2_Port0

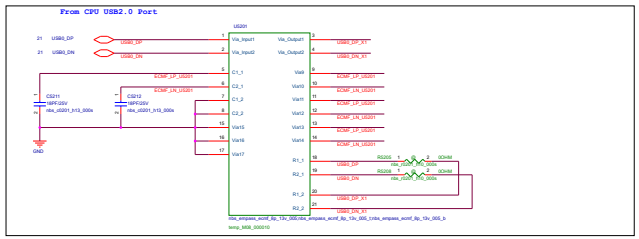
USB3.0 ESD-Protection



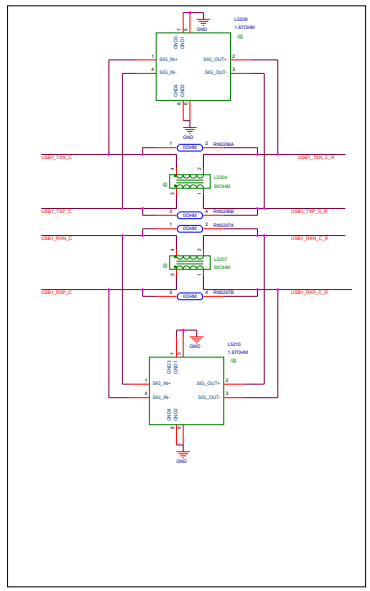
USB2.0 ESD-Protection



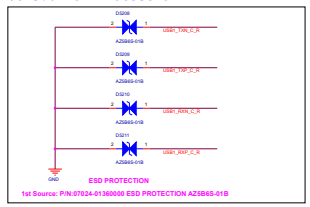
USB2.0 EMI-Protection With ECMF(PCB 1.05mm_10Layer)



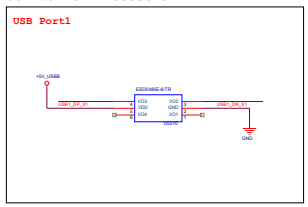
USB3.0 EMI-Protection



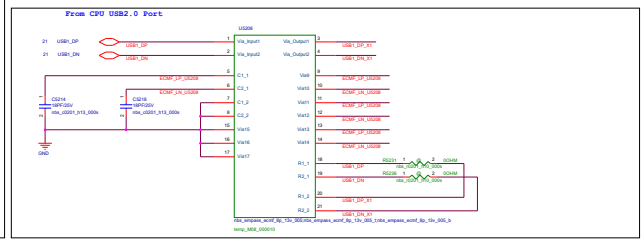
USB3.0 ESD-Protection



USB2.0 ESD-Protection



USB2.0 EMI-Protection With ECMF(PCB 1.05mm_10Layer)



< Fine tune table for Pericom (One port Gen2) >

< EQ table for Pericom 1002B >

EQ[A:B]	Gen 1 @2.5GHz(dB)	Gen 2 @5GHz(dB)
0 : 0 Ω to GND	5.1	10.9
R : Rext to GND	1.9	6.7
F : Leave Open	3.5(Default)	8.9(Default)
1 : 0 Ω to VDD	6.8	13.1

Note : With internal 100Kohm pull-up Rup and 200Kohm pull-down Rdown.
Rext = 68Kohm

< FG table for Pericom 1002B >

FG[A:B]	Flat Gain (dB)
0 : 0 Ω to GND	-3.0
R : Rext to GND	-1.5
F : Leave Open	0 (Default)
1 : 0 Ω to VDD	+2.0

< SW table for Pericom 1002B >

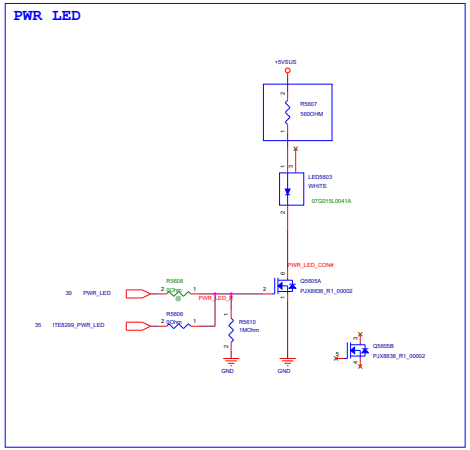
SW[A:B]	Output Linear Swing (mV)
0 : 0 Ω to GND	800
R : Rext to GND	1200
F : Leave Open	1000 (Default)
1 : 0 Ω to VDD	1100

< Channel / Receiver setting for Pericom 1002B >

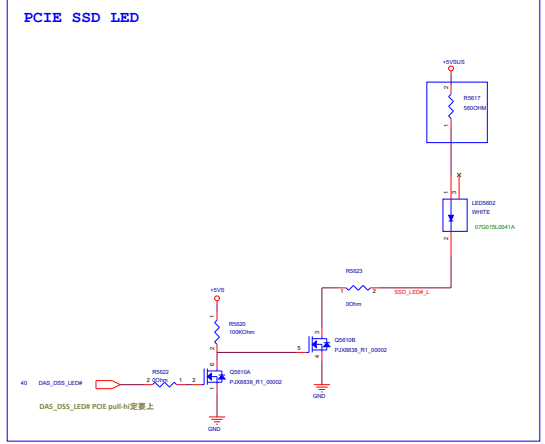
Setting	Channel Enable [EN]	Receiver Detection [RXDET_EN]
0 : 0 Ω to GND	Disable	Disable
1 : 0 Ω to VDD	Enable(Default)	Enable(Default)
Note	Channel Enable / Receiver detection with internal 300K pull-up R.	

ASUS	Project Name: GA503QS	Rev: R1.0
Title: USB3.0 1 Port		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Design IP
Date: Tuesday, October 13, 2020	Sheet: 52 of 104	

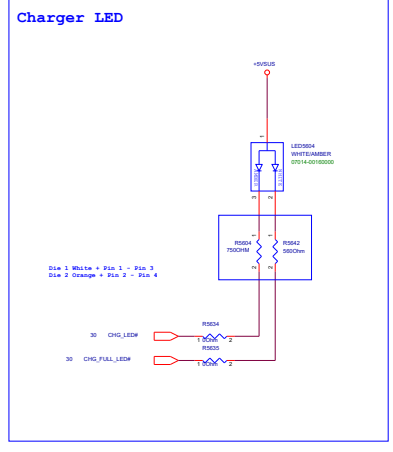
PWR LED



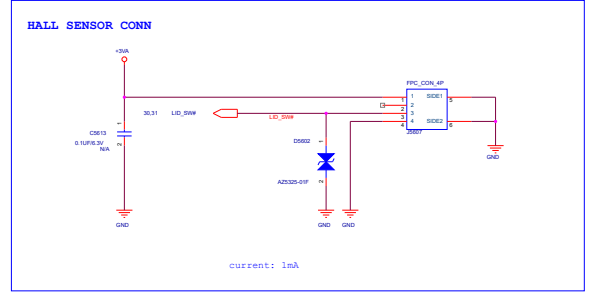
PCIE SSD LED



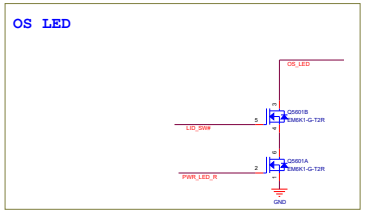
Charger LED

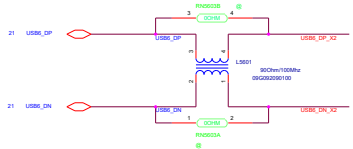


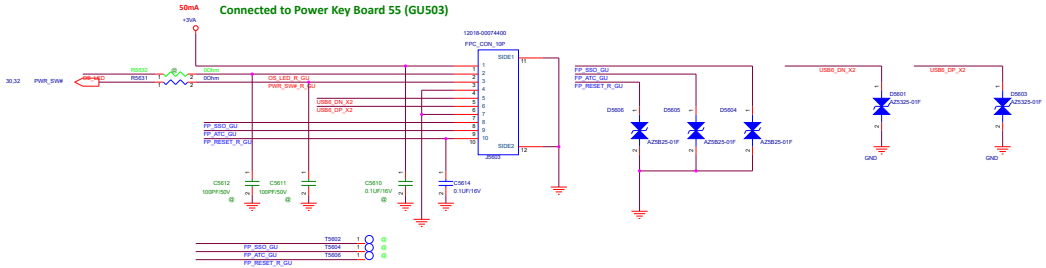
HALL SENSOR CONN

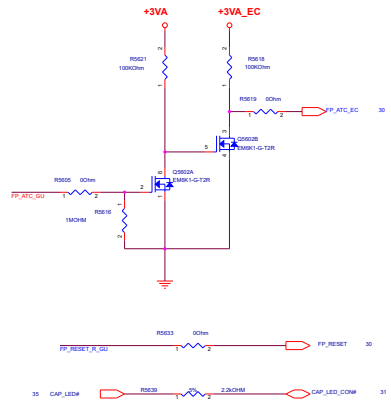


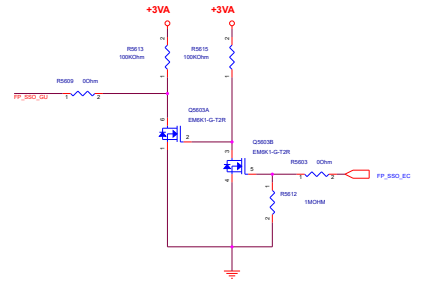
OS LED











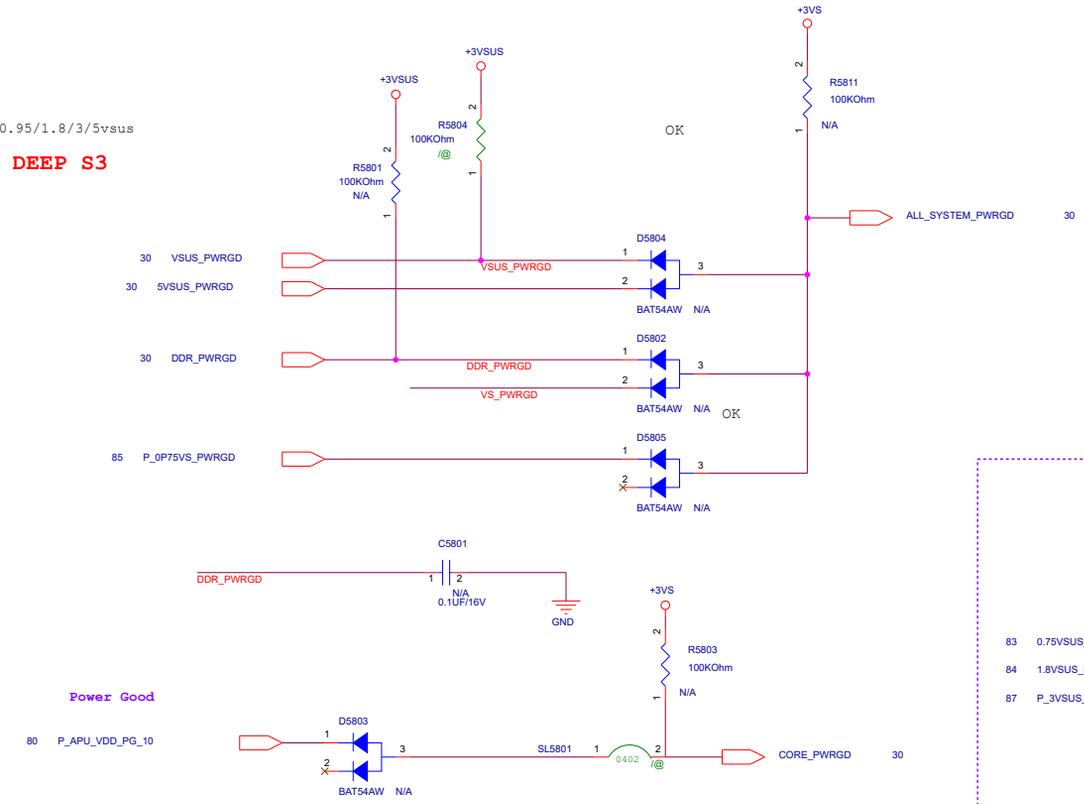
Title : LED & LID

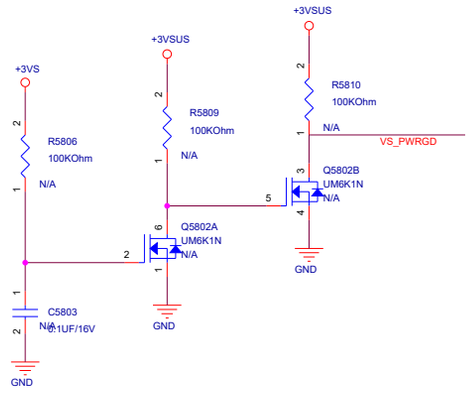
Engineer: EE

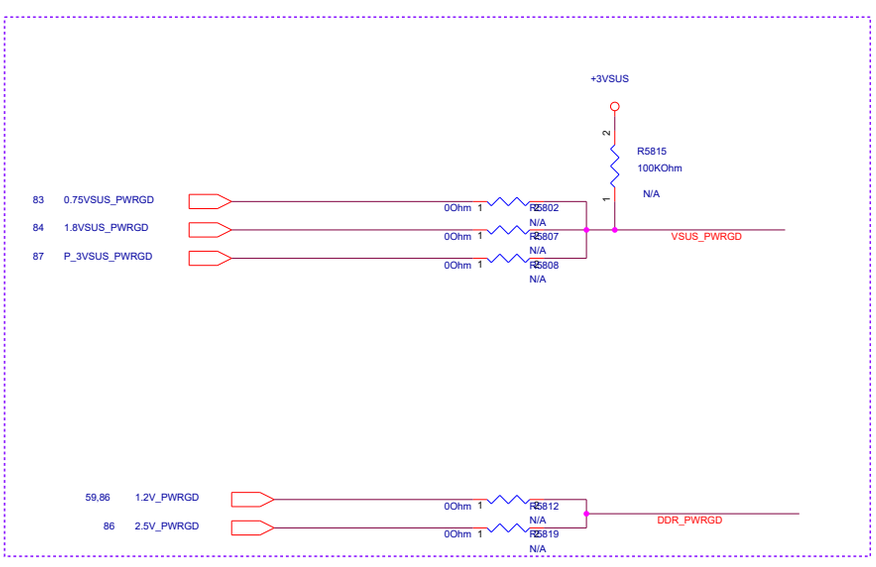
Size	Project Name	Rev
Custom	GA503QS	R1.2

Date: Tuesday, October 13, 2020 Sheet 56 of 104

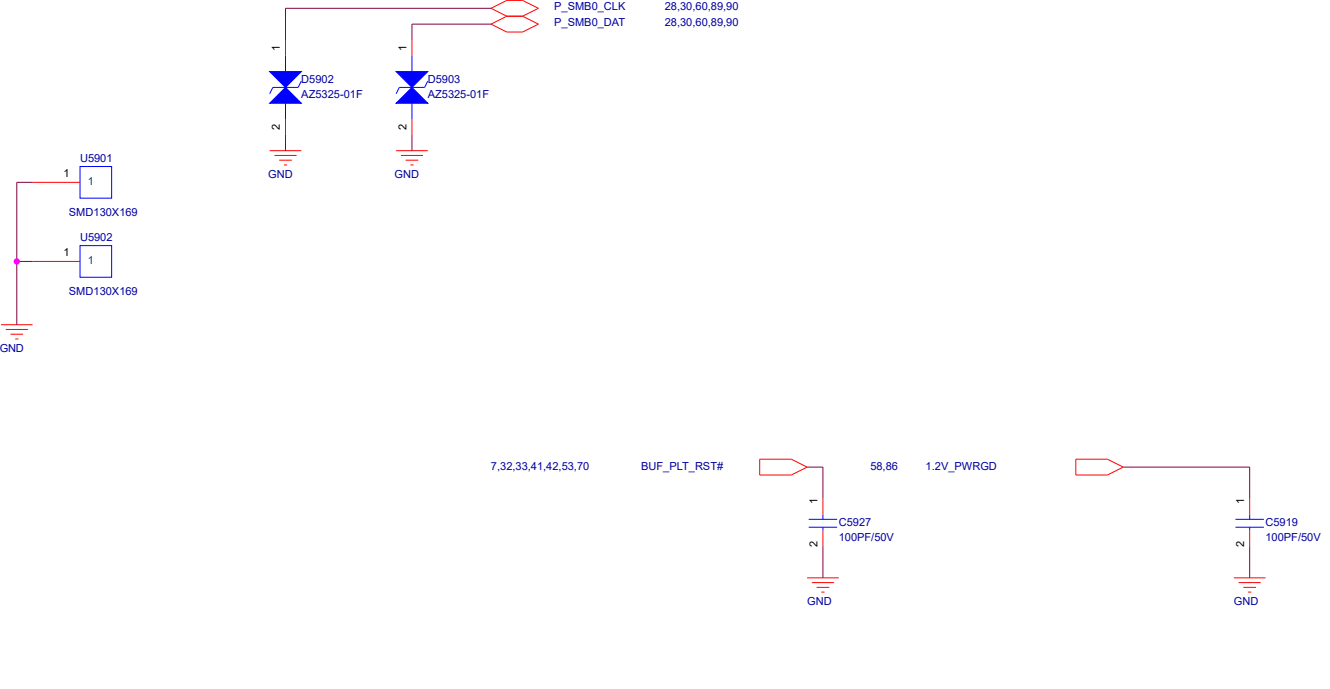
POWER GOOD DETECTER







Project Name: GA503QS		Rev: R1.0
Title : POWER GOOD DETECTER		
Size: Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: RD2 EE3	
Date: Tuesday, October 13, 2020	Sheet 58 of 104	

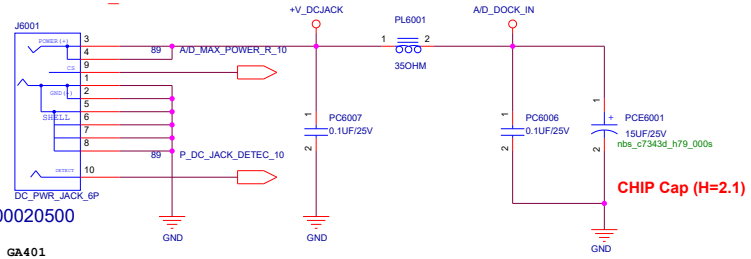


ASUSTeK COMPUTER	Title : OTH_EMI	
	Engineer: EE	
Size: B	Project Name: GA503QS	Rev: 1.0
Date: Tuesday, October 13, 2020	Sheet 59 of 104	

DC-IN Connector

DC Jack使用請詢用River_Hsu

New 6 Phi 4 Pin DC_Jack

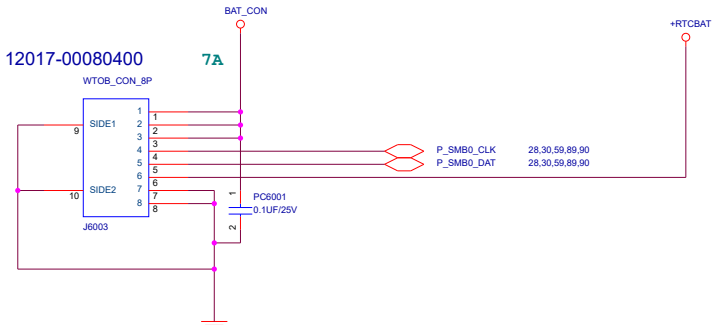


12033-00020500

leverage GA401

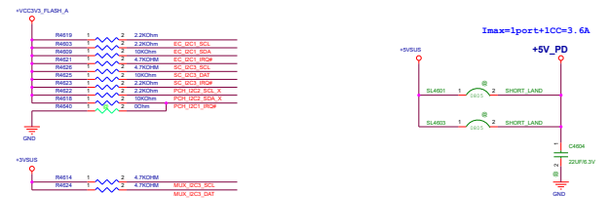
J6001	3.4CH	1.55CH
	12033-00020200	12033-00020300

Battery Connector



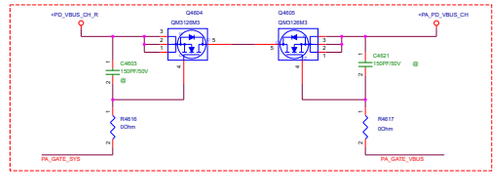
Note:Battery Connector 正確性與BAT1_IN_OC#是否預留!

ASUS	Project Name: GA503QS		Rev: R1.0
Title : DC & BAT IN			
Size: A3	Dept.: NB_Power team	Engineer: Benson	
Date: Tuesday, October 13, 2020	Sheet 60 of 103		

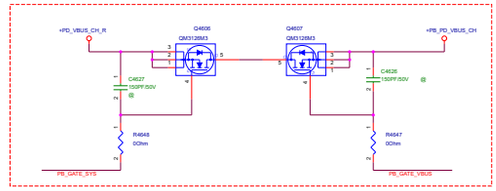


Imax=1port+1CC=3.6A

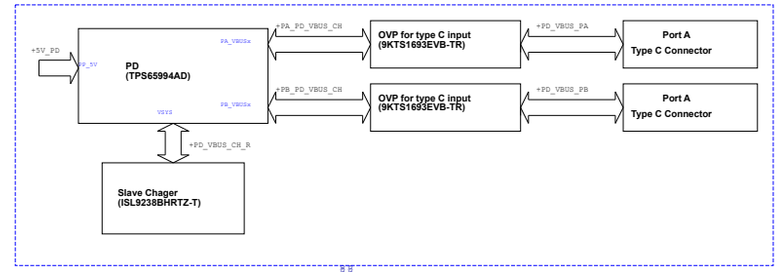
Port A Dual N MOS



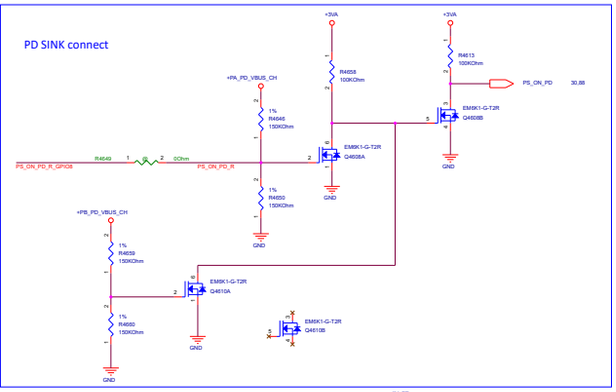
Port B Dual N MOS



Power Flow Chart

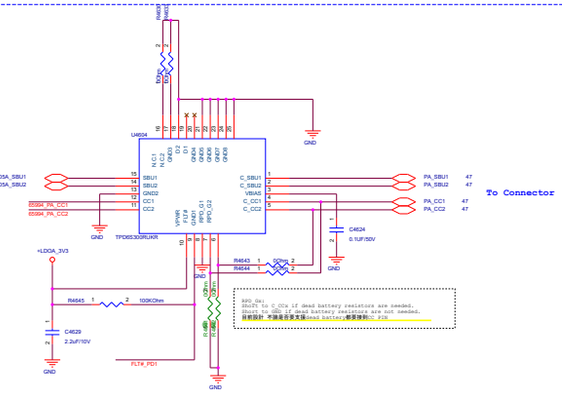


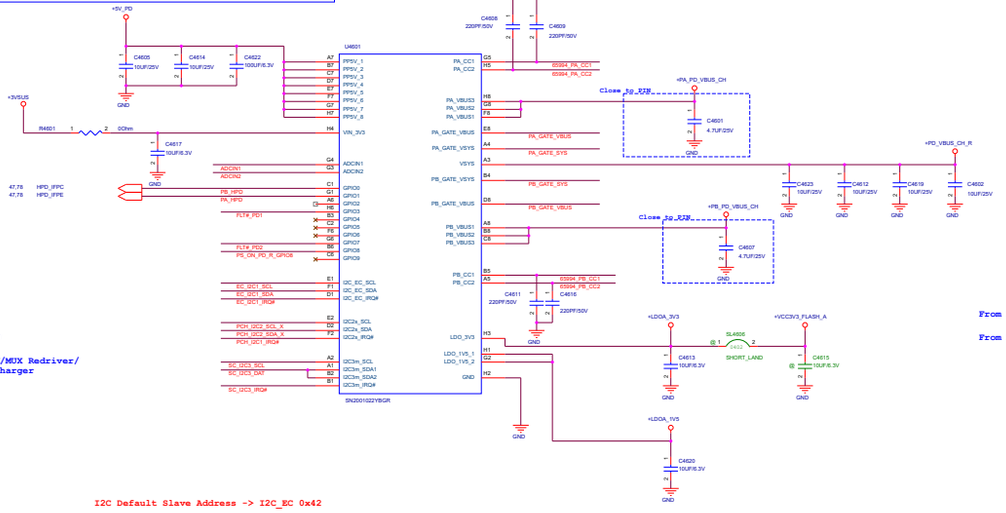
PD SINK connect



From 1205A

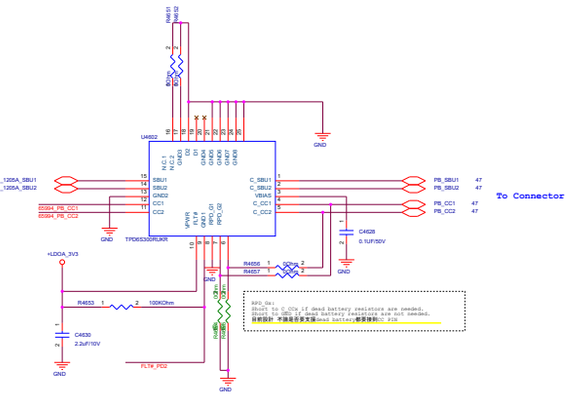
From PD





From 1205A

From PD



EC

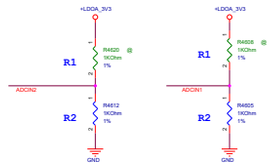
PCH/APU

I2C ROM/MUX Redriver/ Slave Charger

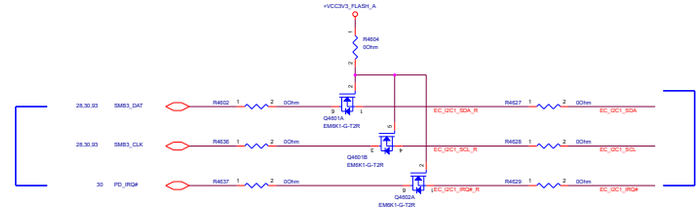
Supported Slave Charger

	W/O I2C ROM	W/ I2C ROM
R4620	4.7K ohm	umount
R4612	1K ohm	1K ohm
R4608	4.7K ohm	umount
R4605	1K ohm	1K ohm

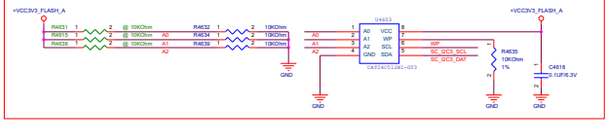
I2C Default Slave Address -> I2C_EC 0x42



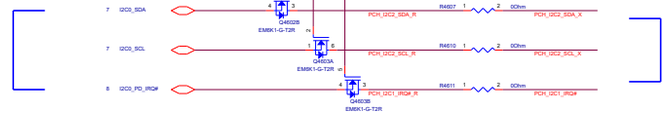
EC & Slave Charger



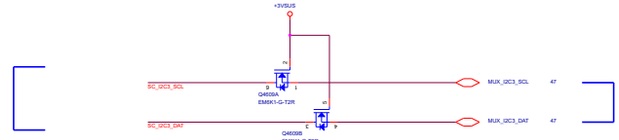
I2C ROM



Udpaye FW from PCH/APU



PD I2C ROM'



ASUS	Project Name: Type-C_ALT_USB3-10G + DP + PD + Slave_Charger_T1		Rev: 1.0
Title :	PD_TPS65993AC		
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: Design IP	
Date: Tuesday, October 13, 2020	Sheet: 46 of 103		

Title : BT_Bluetooth

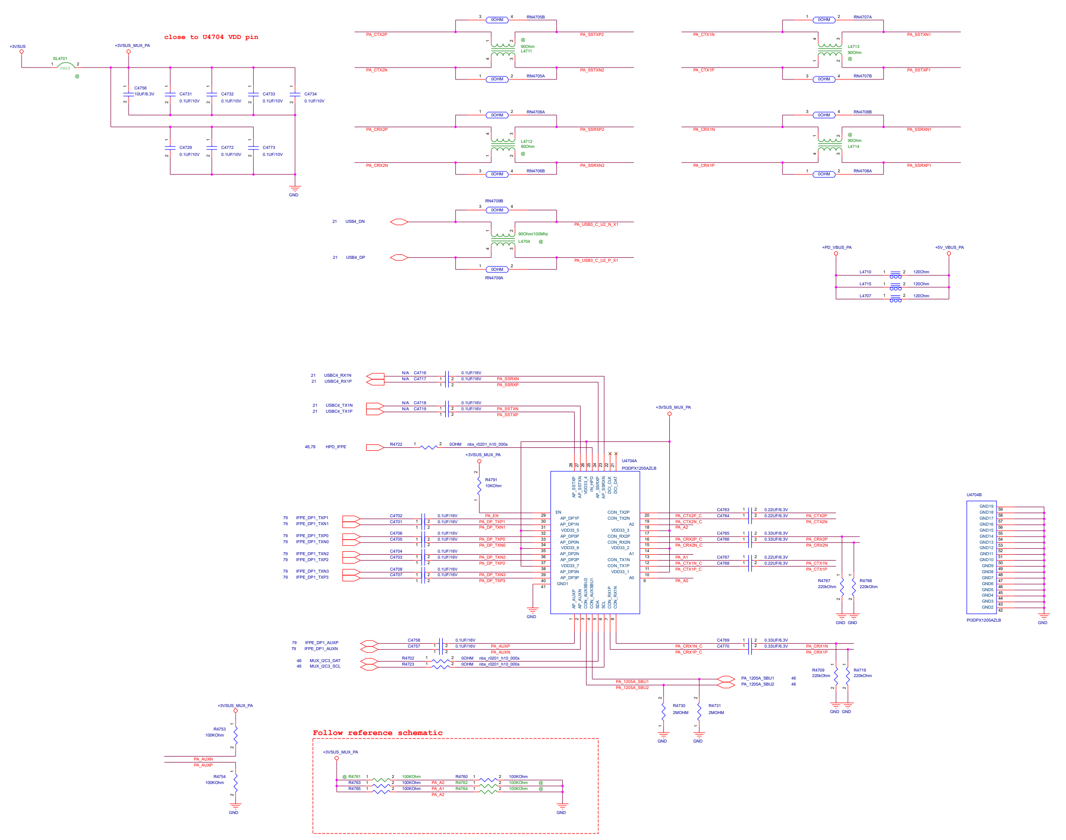
ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
C	GA503QS	1.0

Date:	Tuesday, October 13, 2020	Sheet	61	of	104

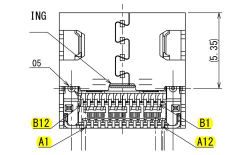
USB EMI-Protection

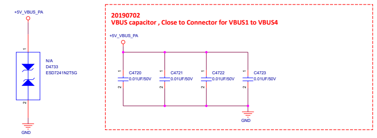


NOTE 8.PIN ASSIGNMENT (FRONT VIEW)

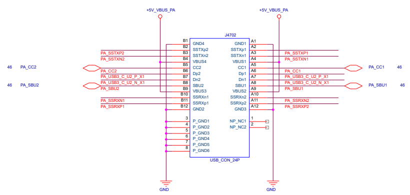
Pin No.	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
	GND	TX1+	TX1-	V_{BUS}	CC1	D+	D-	SBU1	V_{BUS}	RX2-	RX2+	GND
	GND	RX1+	RX1-	V_{BUS}	SBU2	D-	D+	CC2	V_{BUS}	TX2-	TX2+	GND
Pin No.	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

NOTE 9.LASER WELD POINTS MAY BE DISCOLORED.

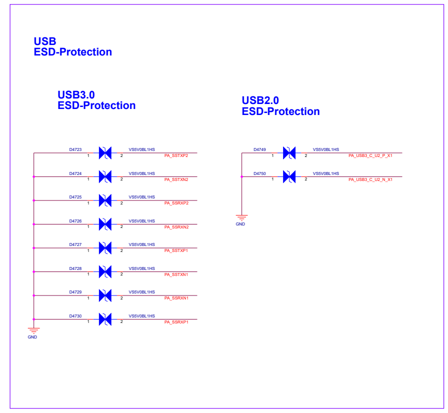




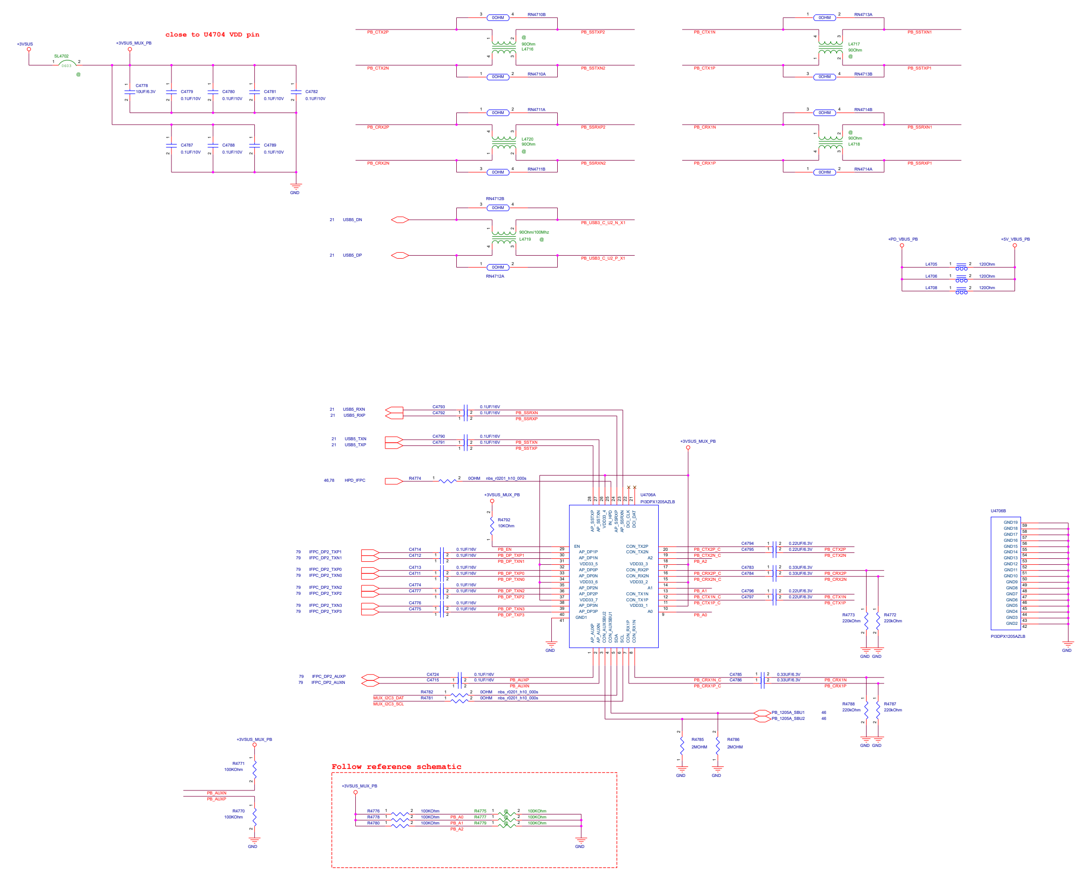
TYPE-C Connector



12013-00175600



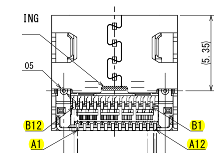
USB EMI-Protection

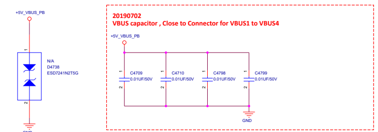


NOTE 8.PIN ASSIGNMENT (FRONT VIEW)

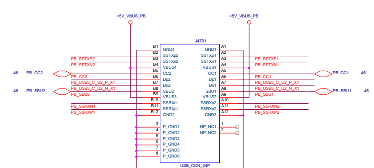
Pin No.	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
	GND	TX1+	TX1-	V_{BUS}	CC1	D+	D-	SBU1	V_{BUS}	RX2-	RX2+	GND
	GND	RX1+	RX1-	V_{BUS}	SBU2	D-	D+	CC2	V_{BUS}	TX2-	TX2+	GND
Pin No.	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

NOTE 9.LASER WELD POINTS MAY BE DISCOLORED.

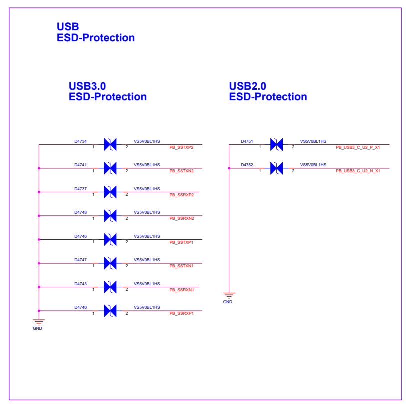




TYPE-C Connector Port B



12013-00175600



ASUS	Project Name: TYPE-C_ALT_USB3-10G + DP + PD_TI	Rev 1.0
Title : USB3.1_TYPE-C_MUX_TI_1046A		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Design IP
Date: Tuesday, October 13, 2020	Sheet 47 of 105	

Title : EC_BD

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
C	GA503QS	1.0

Date:	Tuesday, October 13, 2020	Sheet	62	of	104

Main Board

HDMI Active-Level Shift

to APU

FromAPU

Q4801只用07005-00660200與07005-00950000

06106-00390100

SN75DP159RSBT

HDMI PWR_+5VS_HDMI

Remove SL4802 (20180927)

HDMI Conn.

12022-00135300

HDMI EMI

LX4801~LX4803, LX4805
footprint 過大更改為hh_choke_4p_39x49_mura

09G092090400

HDMI LDO 1.1VS

Imax = 0.35A

TLV75511PDQNR

AZ1045-04F

AZ5525-01F.R7G

Slew rate control when I2C_EN/PIN = Low.
SLEW_CTL = H, fastest data rate
SLEW_CTL = L, 5 ps slow
SLEW_CTL = No Connect, 10 ps slow

HDMI_SEL when I2C_EN/PIN = Low
HDMI_SEL = High: Device configured for DVI
HDMI_SEL = Low: Device configured for HDMI

Input Receive Equalization pin strap when I2C_EN/PIN = Low
EQ_SEL = L: Fixed EQ at 7.5 dB
EQ_SEL = No Connect: Adaptive EQ
EQ_SEL = H: Fixed at 14 dB

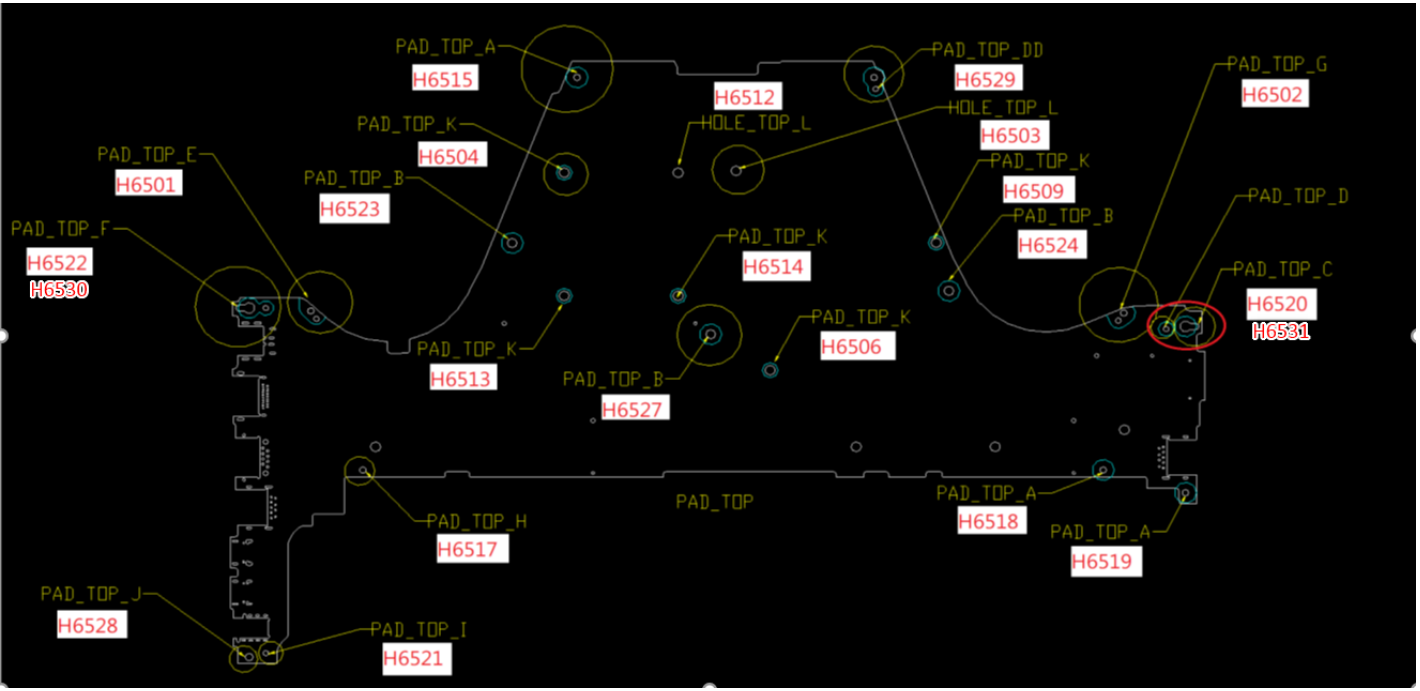
De-emphasis pin strap when I2C_EN/PIN = Low.
PRE_SEL = L: - 2 dB de-emphasis level
PRE_SEL = No Connect: 0 dB
PRE_SEL = H: Reserved

2
0
1
CLK

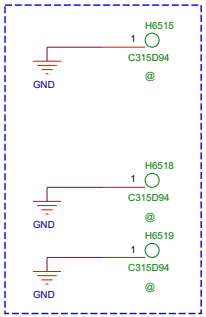
I2C_EN/PIN = High; puts device into I2C control mode
I2C_EN/PIN = Low; puts device into pin strap mode

Operation enable/reset pin
OE = L: Power-down mode OE = H: Normal operation
Internal weak pullup: Resets device when transitions from H to L

Project Name	GA503QS
Rev	0.1A
Title :	HDMI ReTimer_Revision History_R0.1A
Size	Custom
Dept.:	ASUSTeK COMPUTER
Engineer:	EE
Date:	Tuesday, October 13, 2020
Sheet	48 of 104

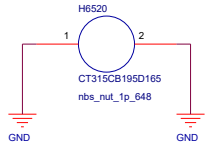


A

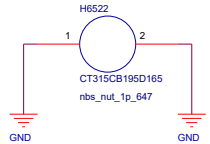


B

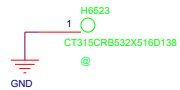
C



E

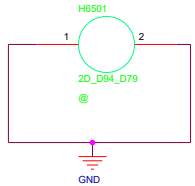


F

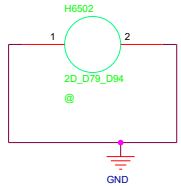


G

I



J

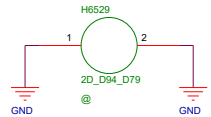


K

L

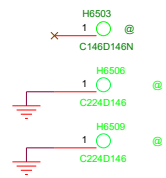
M

N



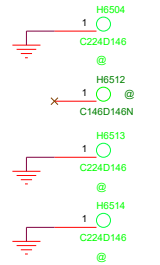
CPU

TOP 3.7/6.5, BOT 3.7/4.7



GPU

TOP 3.7/6.5, BOT 3.7/4.7



<Core Design>

ASUSTeK COMPUTER	Title : I/O board FUNC key	
	Engineer: EE	
Size: B	Project Name: GA503QS	Rev: 1.0
Date: Tuesday, October 13, 2020	Sheet 65 of 104	

Title :

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
A	**GA503QS**	1.0

Title : ME_Screw Hole & Nut

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
A	GA503QS	1.0

Date:	Tuesday, October 13, 2020	Sheet	67	of	104

<Core Design>

ASUSTeK COMPUTER	Title : OTH_for test only	
	Engineer: EE	
Size: A	Project Name: GA503QS	Rev: 1.0
Date: Tuesday, October 13, 2020	Sheet 68 of 104	

<Core Design>

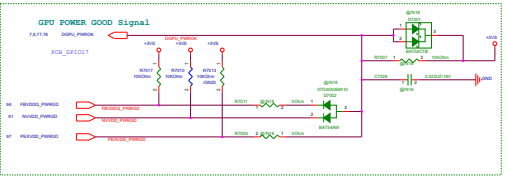
Title : I/O_Main board Conn.

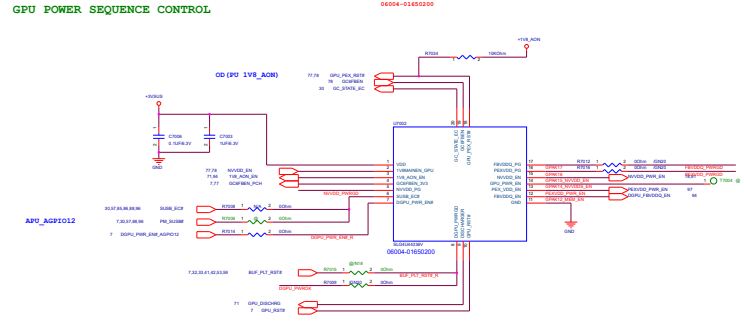
ASUSTeK COMPUTER

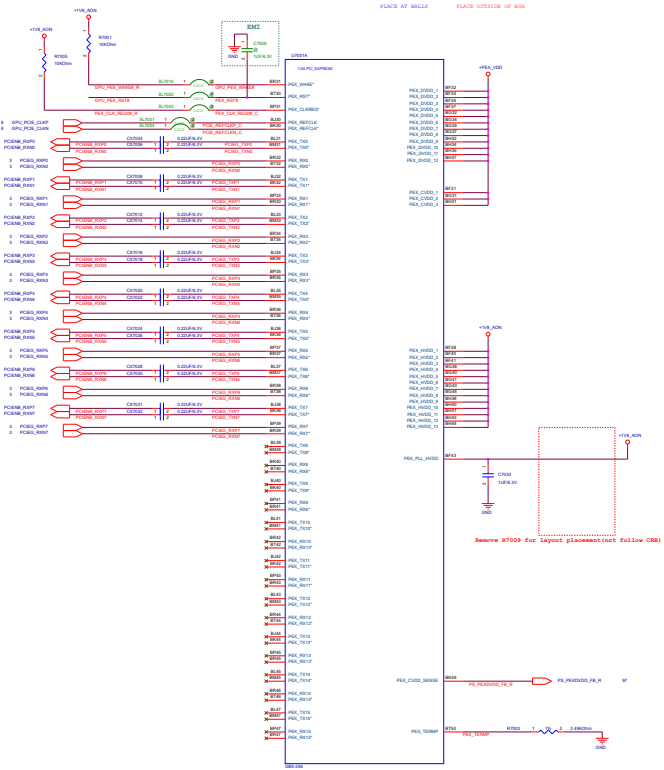
Engineer: EE

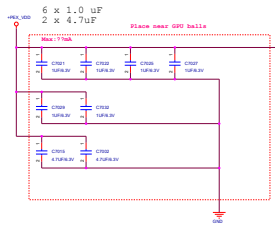
Size	Project Name	Rev
A	GA503QS	1.0

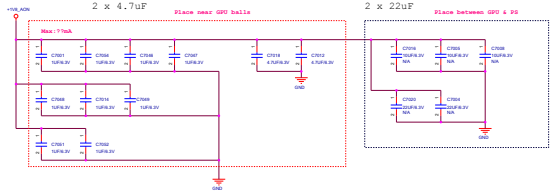
Date:	Tuesday, October 13, 2020	Sheet	69	of	104

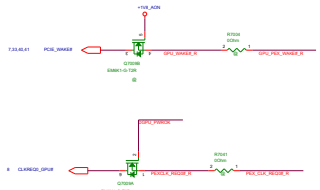








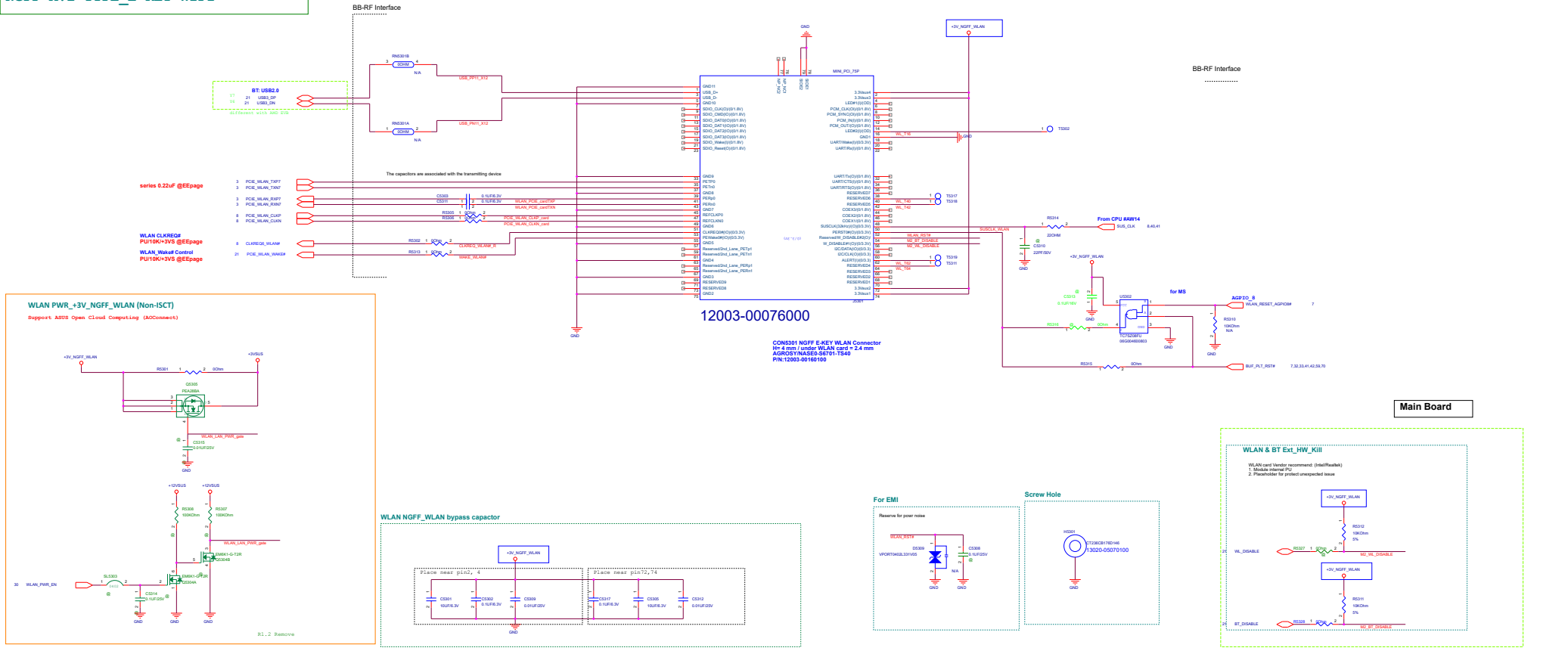




ASUS	Project Name: GA503QS		Rev: 2.0
Title: GPU_PCIE IF			
Size: Custom	Dept.:	Engineer:	
Date: Tuesday, October 15, 2019	Sheet 70 of 104		

AMD-1.0

NGFF M.2 TYPE_E-KEY WIFI



WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)

Support ASUS Open Cloud Computing (AOConnect)

WLAN NGFF_WLAN bypass capactor

For EMI

Reserve for power noise

Screw Hole

Main Board

WLAN & BT Ext_HW_Kill

WLAN card Vendor recommend: (Intel/Realtek)
1. Module internal PU
2. Placeholder for protect unexpected issue

<Variant Name>

ASUSTeK COMPUTER	Title: NGFF Type_WLAN&BT	
	Engineer: RF	
Size: Custom	Project Name: GA502IV	Rev: R1.0
Date: Tuesday, October 13, 2020	Sheet 53 of 104	

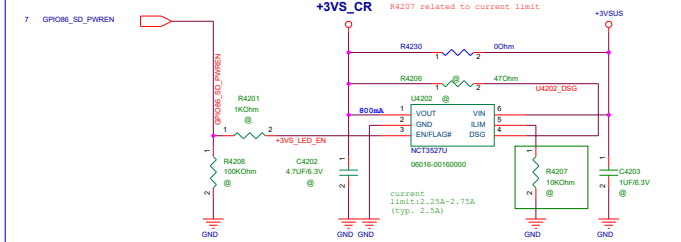
Power_3.3V

for RTD3
for layout placement

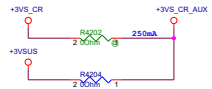
SD3.0 DDR +3VS_CR : 99mA(IC)+800mA(Card)=899mA
SD7.0 +3VS_CR : TBD

Current Limit vs. R_{ILIM} Values

R_{ILIM} (Ω)	Min. Current Limit (mA)	Typ. Current Limit (mA)	Max. Current Limit (mA)
6.98k	2700	3000	3300
7.68k	2430	2700	2970
8.25k	2250	2500	2750
9.53k	1980	2200	2420
10.5k	1800	2000	2200
11.5k	1620	1800	1980
14.3k	1350	1500	1650
17.4k	1080	1200	1320
21k	900	1000	1100

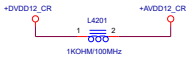


Power_3.3V

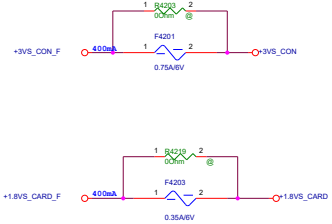


RTD3	Support	No Support
R4202	Unmount	Mount
R4204	Mount	Unmount

Power_1.2V

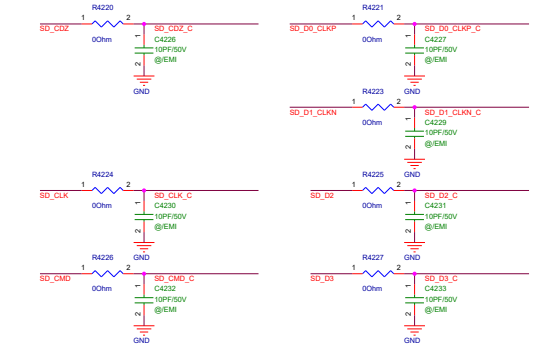


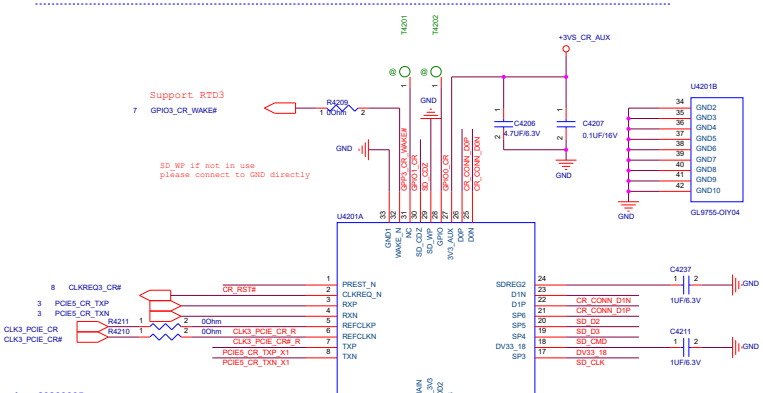
Safety



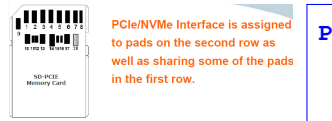
EMI

close to connector





AMD review_20200605

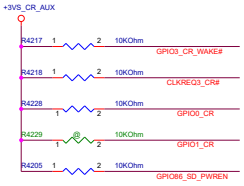


PCIe/NVMe Interface is assigned to pads on the second row as well as sharing some of the pads in the first row.

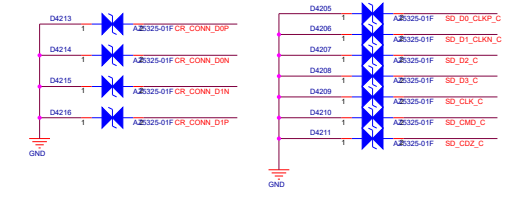
Pin #	Name	Type	Description
1	PERST#	Input signal (active low)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.
4	VDD1	Supply voltage	2.7V to 3.6V
7	REFCLK+	Differential Signaling Input	Clock Input
8	REFCLK-	Differential Signaling Input	Clock Input
9	CLKREQ#	I/O (active low, open drain)	Reference clock request signal. Also used by L1 PM substates
10	VSS3	Ground	
11	PCIe TX+	Differential Signaling	Card Input
12	PCIe TX-	Differential Signaling	Card Input
13	VSS4	Ground	
14	VDD2	Supply Voltage 2	1.70V to 1.95V
15	PCIe RX-	Differential Signaling	Card Output
16	PCIe RX+	Differential Signaling	Card Output
17	VSS5	Ground	
18*	VDD3	Supply Voltage 3	1.14v to 1.30v

(*) reserved for future optional VDD3 power

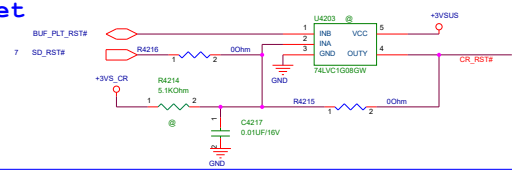
Pull UP



ESD

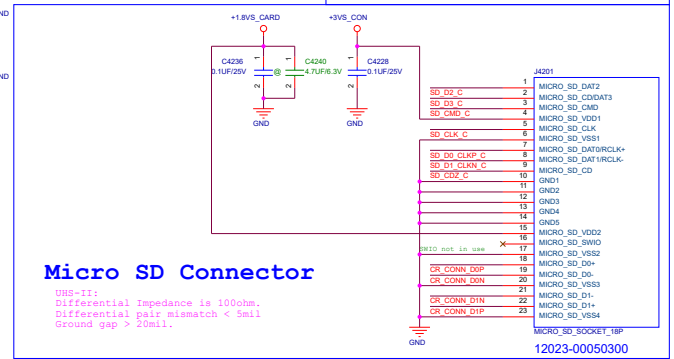


Reset



PCIE

Micro SD Connector



UHS-II:
Differential Impedance is 100ohm.
Differential pair mismatch < 5mil
Ground gap > 20mil.

12023-00050300

ASUS	Project Name: GA503QS	Rev: R1.0
Title : CR_GL9755		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: TG_Wei
Date: Tuesday, October 13, 2020	Sheet 42 of 104	

Title <Title>		
Size A	Document Number GA503QS	Rev <RevCode>
Date: Tuesday, October 13, 2020	Sheet 54 of 104	

<Core Design>

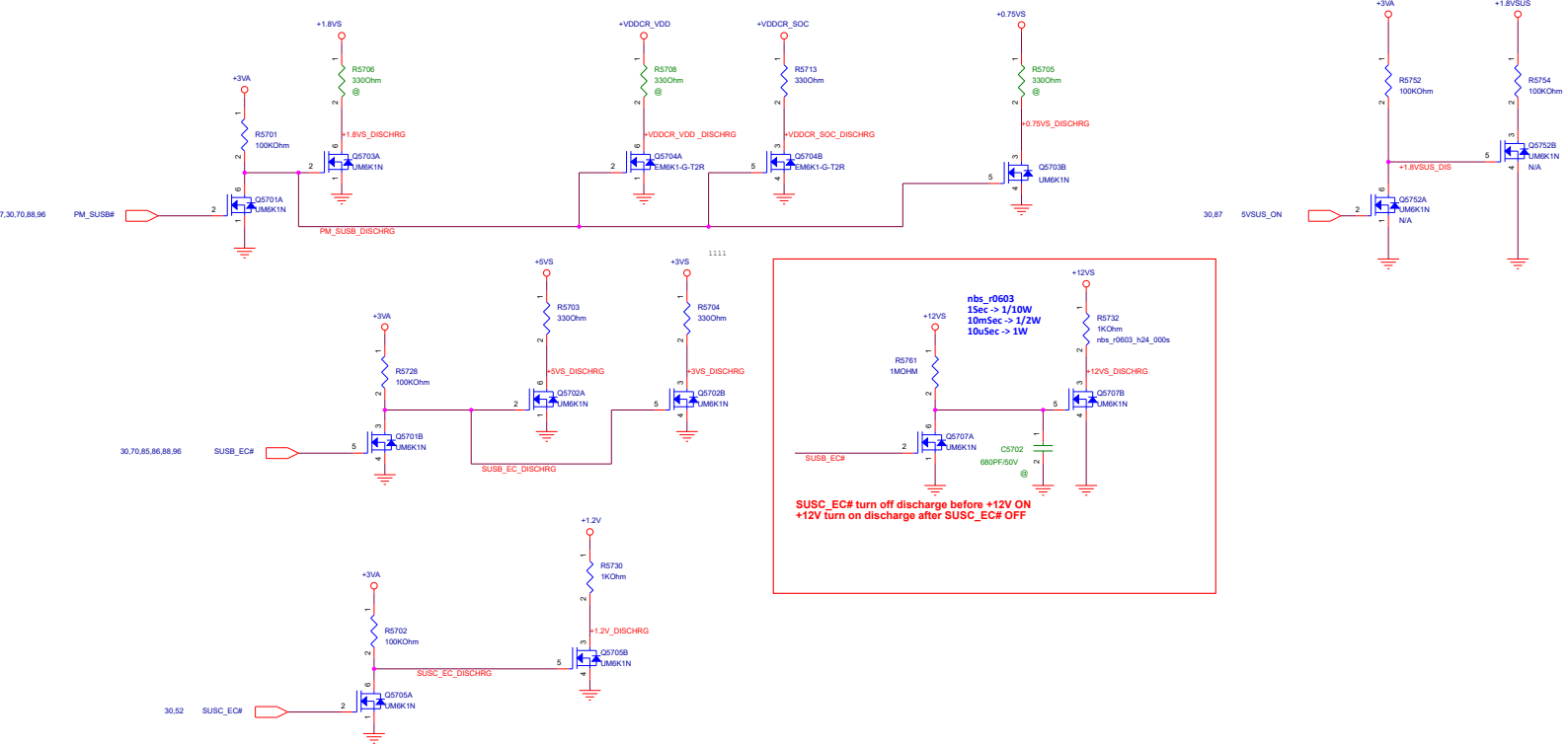
Title :

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
A	**GA503QS**	1.0

Date:	Tuesday, October 13, 2020	Sheet	55	of	104



<Core Design>

ASUSTeK COMPUTER	Title : DSG_Discharge	
	Engineer: EE	
Size: Custom	Project Name: GA503QS	Rev: 1.0
Date: Tuesday, October 13, 2020	Sheet 57 of 104	

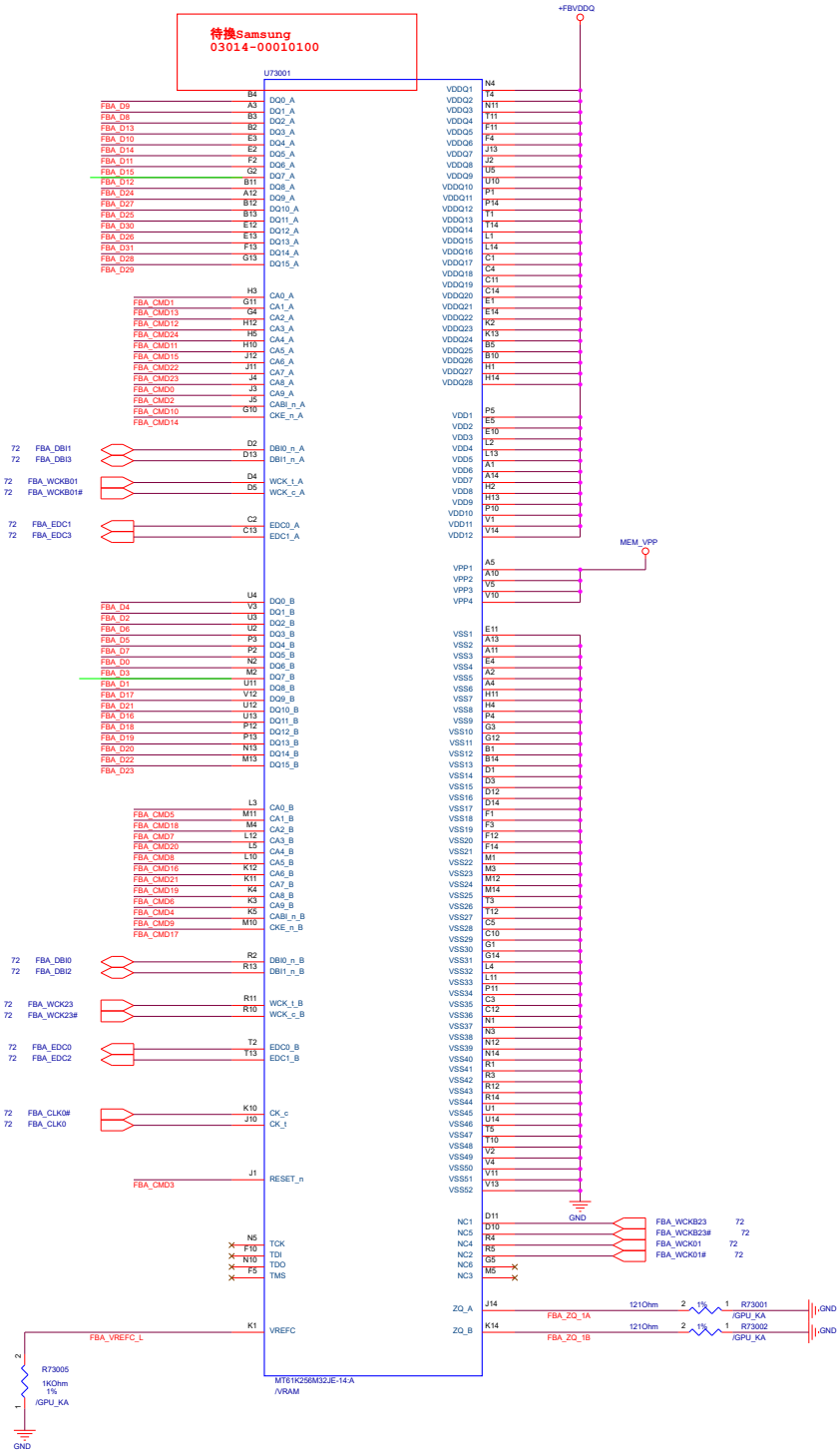
72 FBA_D[31..0]

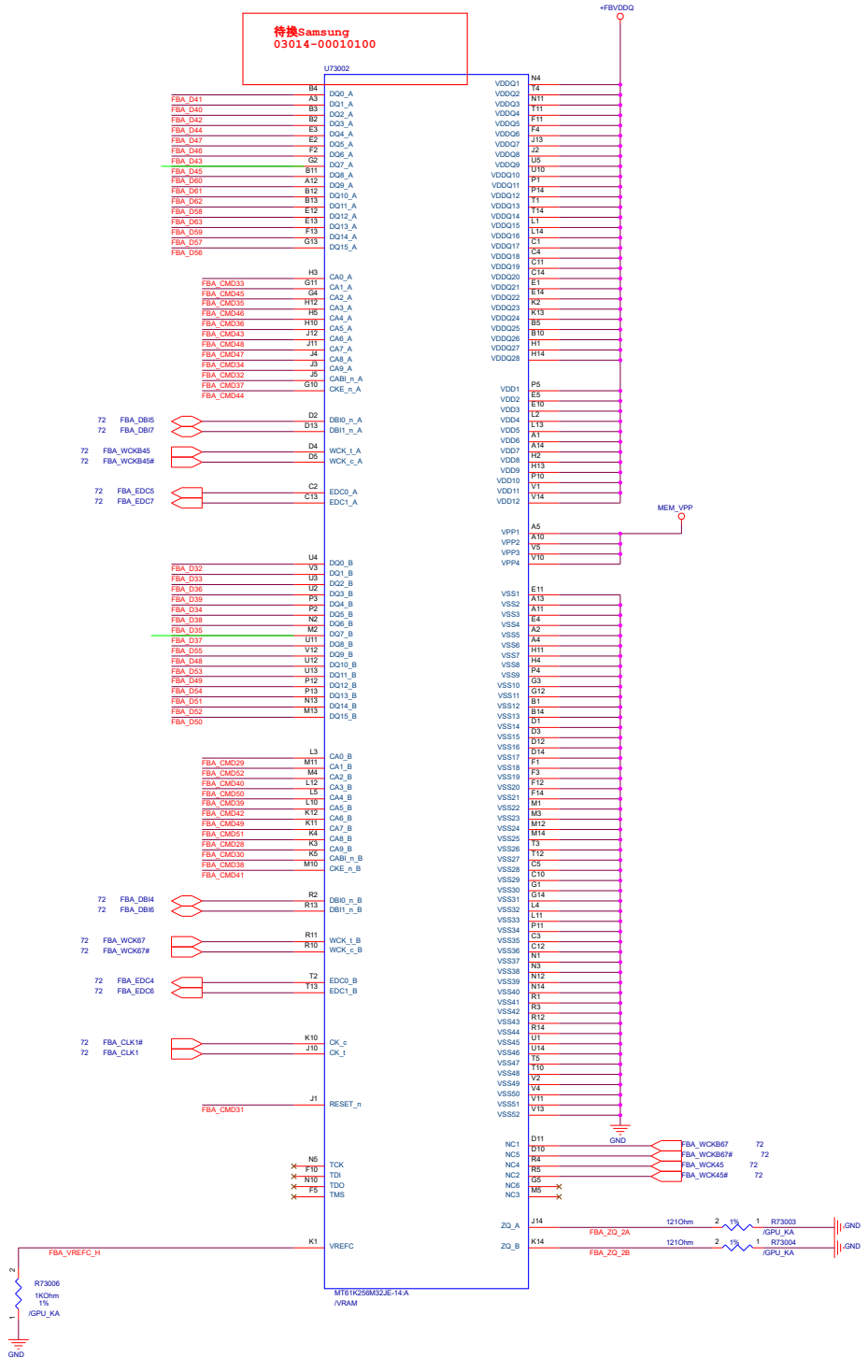
72 FBA_CMD[52..0]

40 OHm_NET
FBA_Partition 31..0
MF=1 Mirror

72 FBA_D[63..32]

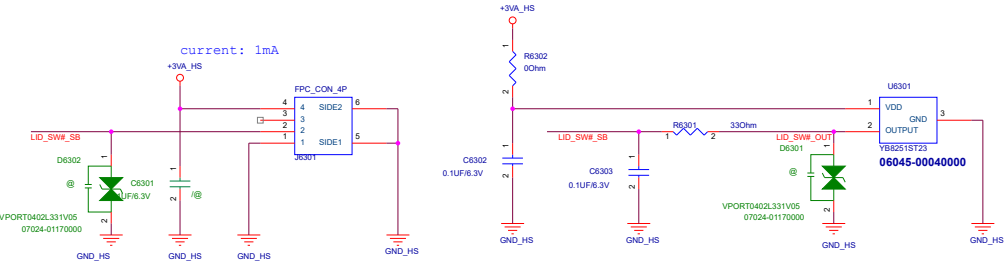
40 OHm_NET
FBA_Partition 64..32
MF=0 Normal





ASUS	Project Name: GX502GX		Rev: R1.2
Title : VRAM_Channel_A			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer:	
Date: Tuesday, October 13, 2020		Sheet 73 of 101	

HALL SENSOR



ASUS	Project Name: Mothership		Rev: R1.1
Title : Power Button_IO_BD			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1	
Date: Tuesday, October 13, 2020		Sheet 63 of 103	

72 FBD_D[31..0]

72 FBD_CMD[52..0]

40 OHm_NET
FBD Partition 31..0
MF=1 Mirror

待換Samsung
03014-00010100

U76003

+FBVDDQ

MEM_VPP

MT61K256M32JE-14:A
/VRAM

72 FBD_D[63..32]

40 OHm_NET
FBDPartition 64..32
MF=0 Normal

待換Samsung
03014-00010100

U76004

+FBVDDQ

MEM_VPP

MT61K256M32JE-14:A
/VRAM

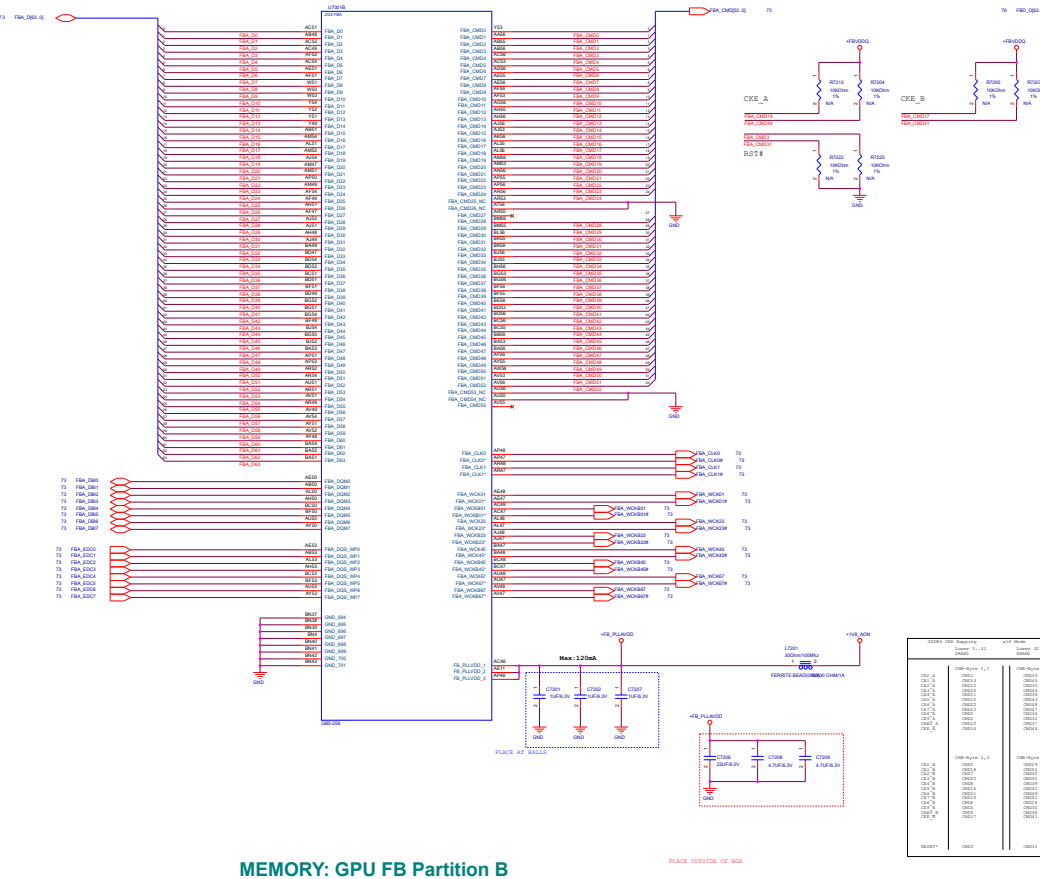
Project Name	Rev
GX502GX	R1.2

Title : VRAM_Channel_D

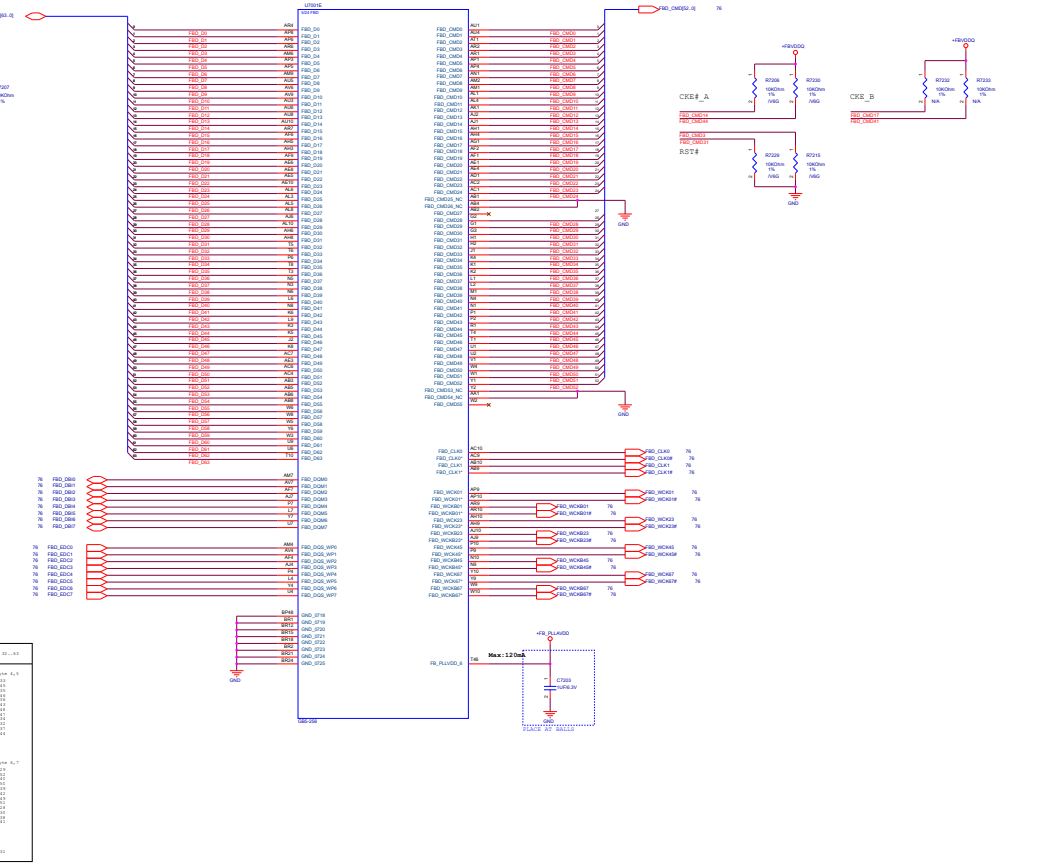
Size	Dept.:	Engineer:
Custom	ASUSTeK COMPUTER INC.	

Date: Tuesday, October 13, 2020 Sheet 76 of 101

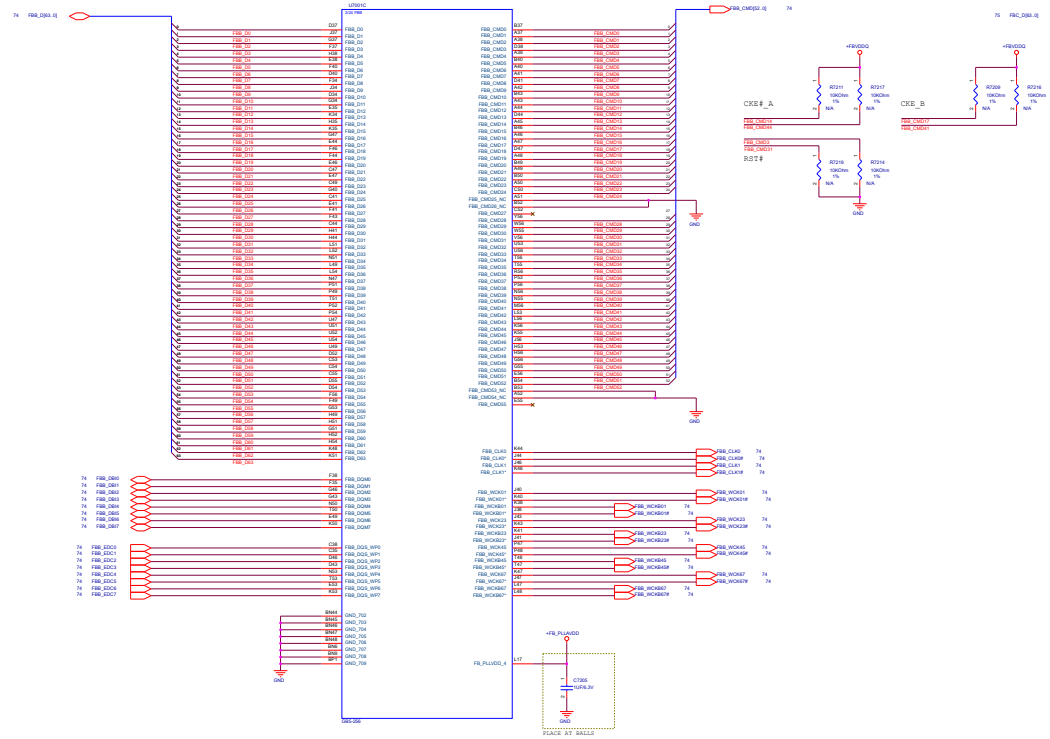
MEMORY: GPU FB Partition A



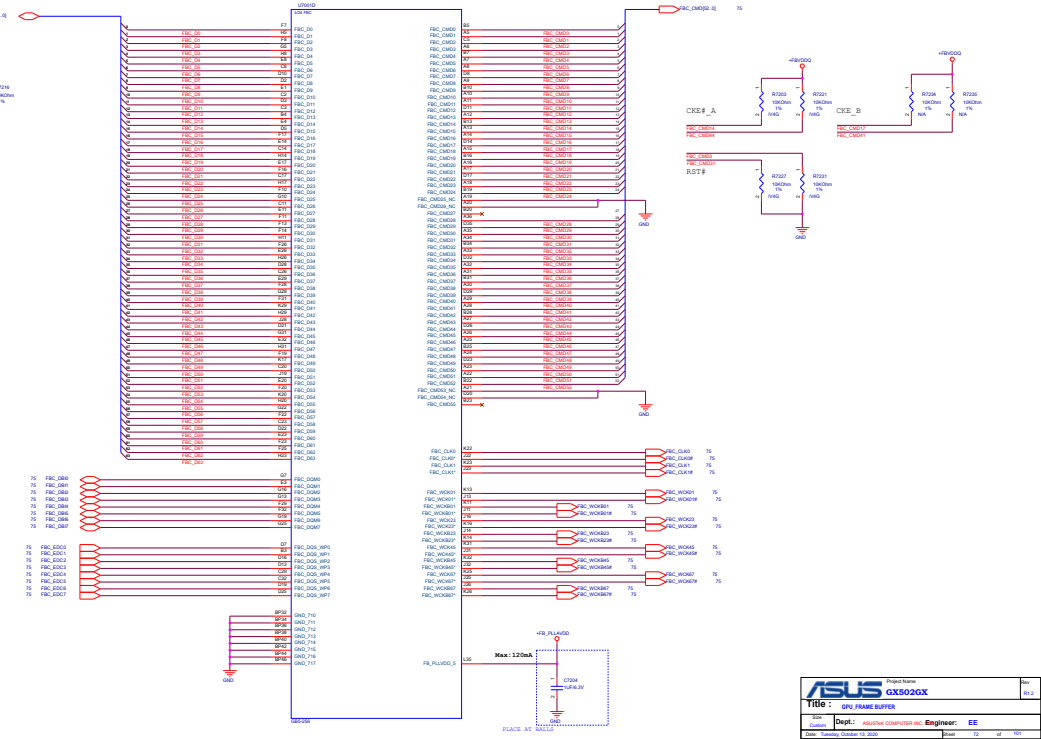
MEMORY: GPU FB Partition D



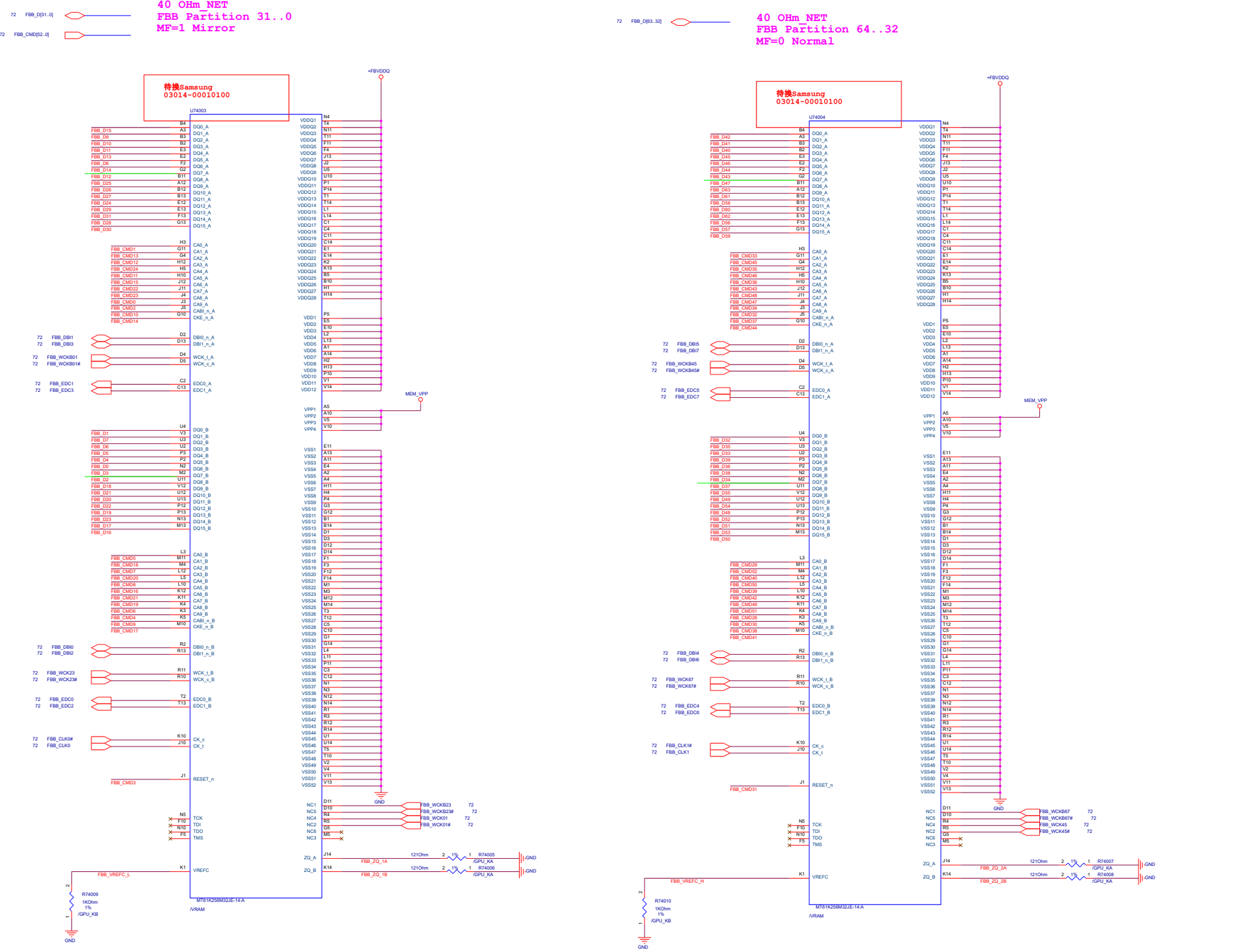
MEMORY: GPU FB Partition B



MEMORY: GPU FB Partition C

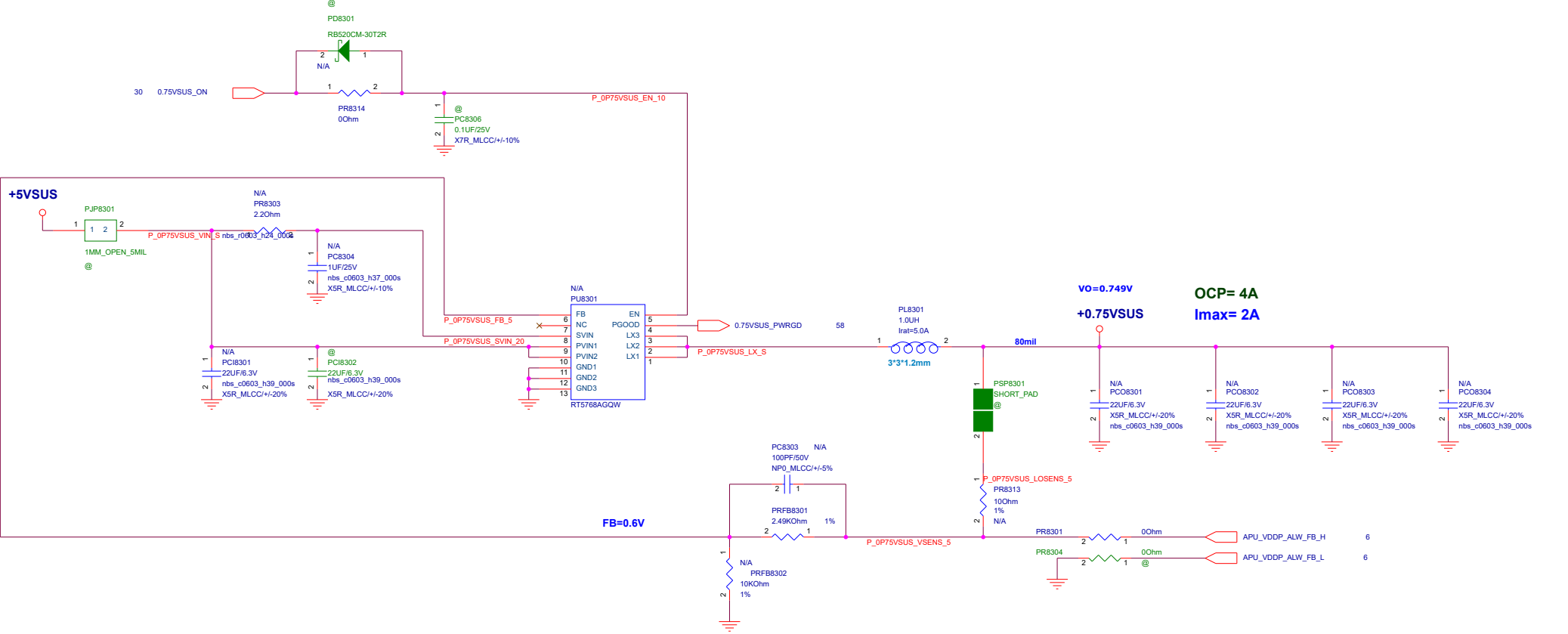


ASUS	Project Name: GX502GX		Rev: R1.0
Title :	GPU_FRAME BUFFER		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE	
Date: Tuesday, October 13, 2020		Sheet 72 of 161	



teknisi-indonesia

ASUS	Project Name: GX502GX		Rev: R1.2
Title : VRAM_Channel_B			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer:	
Date: Tuesday, October 13, 2020		Sheet 74 of 101	



<Variant Name>

Project Name: GA503QS		Rev: R1.0
Title : PW_+0.75VSUS		
Size: A3	Dept.: NB Power team	Engineer: CS Lin
Date: Tuesday, October 13, 2020	Sheet 83 of 104	

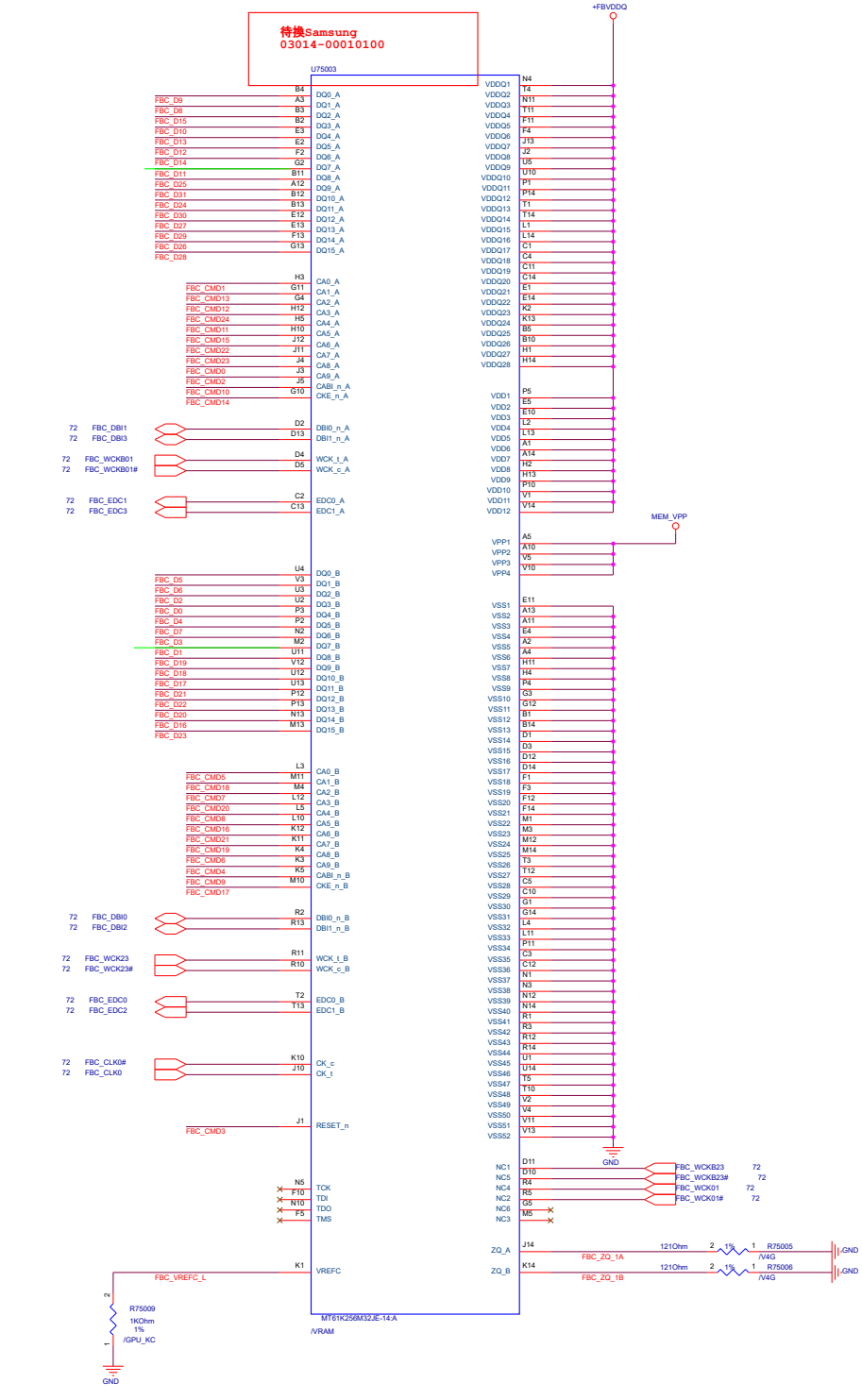
72 FBC_D[31..0]

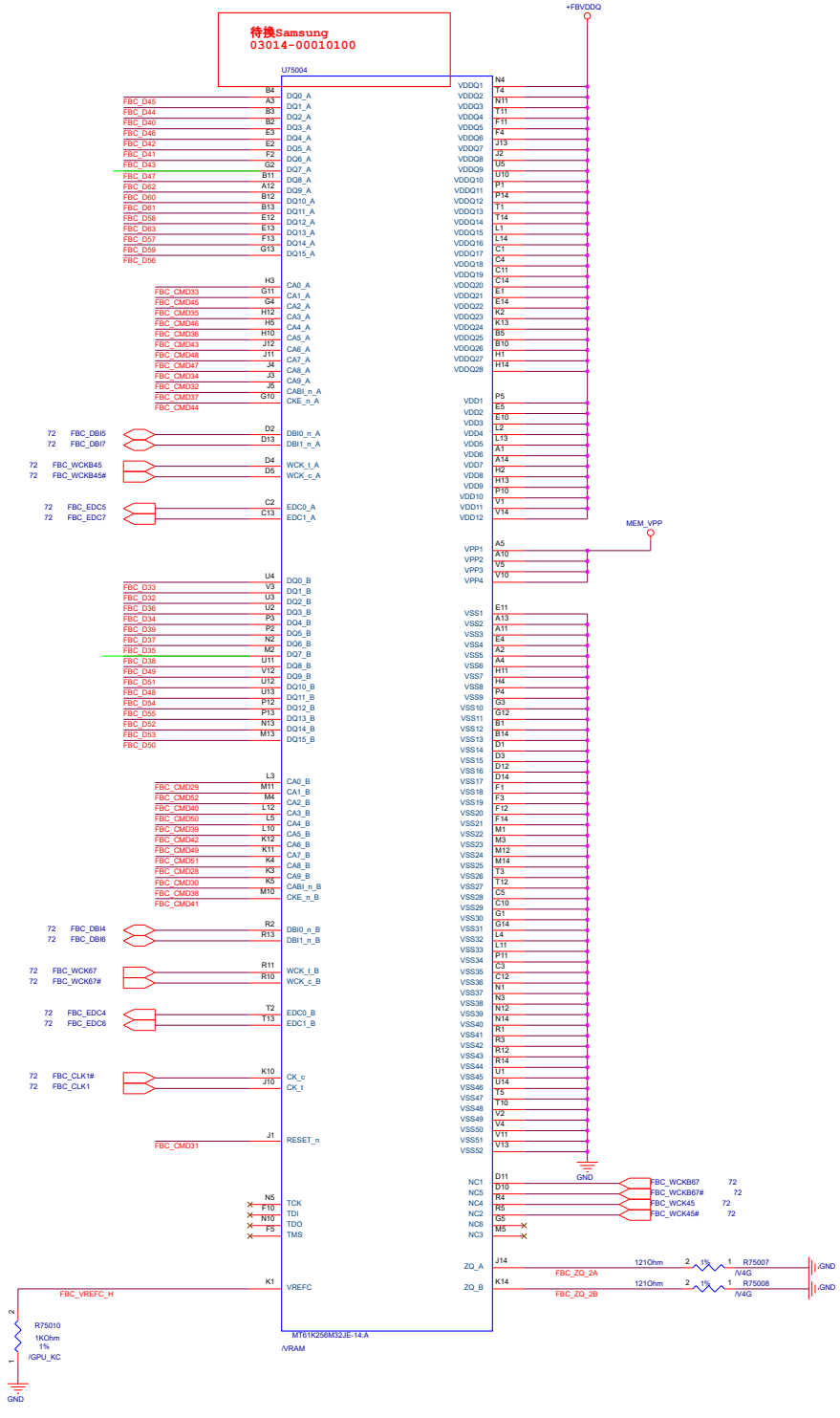
72 FBC_CMD[52..0]

40 OHm_NET
FBC Partition 31..0
MF=1 Mirror

72 FBC_D[63..32]

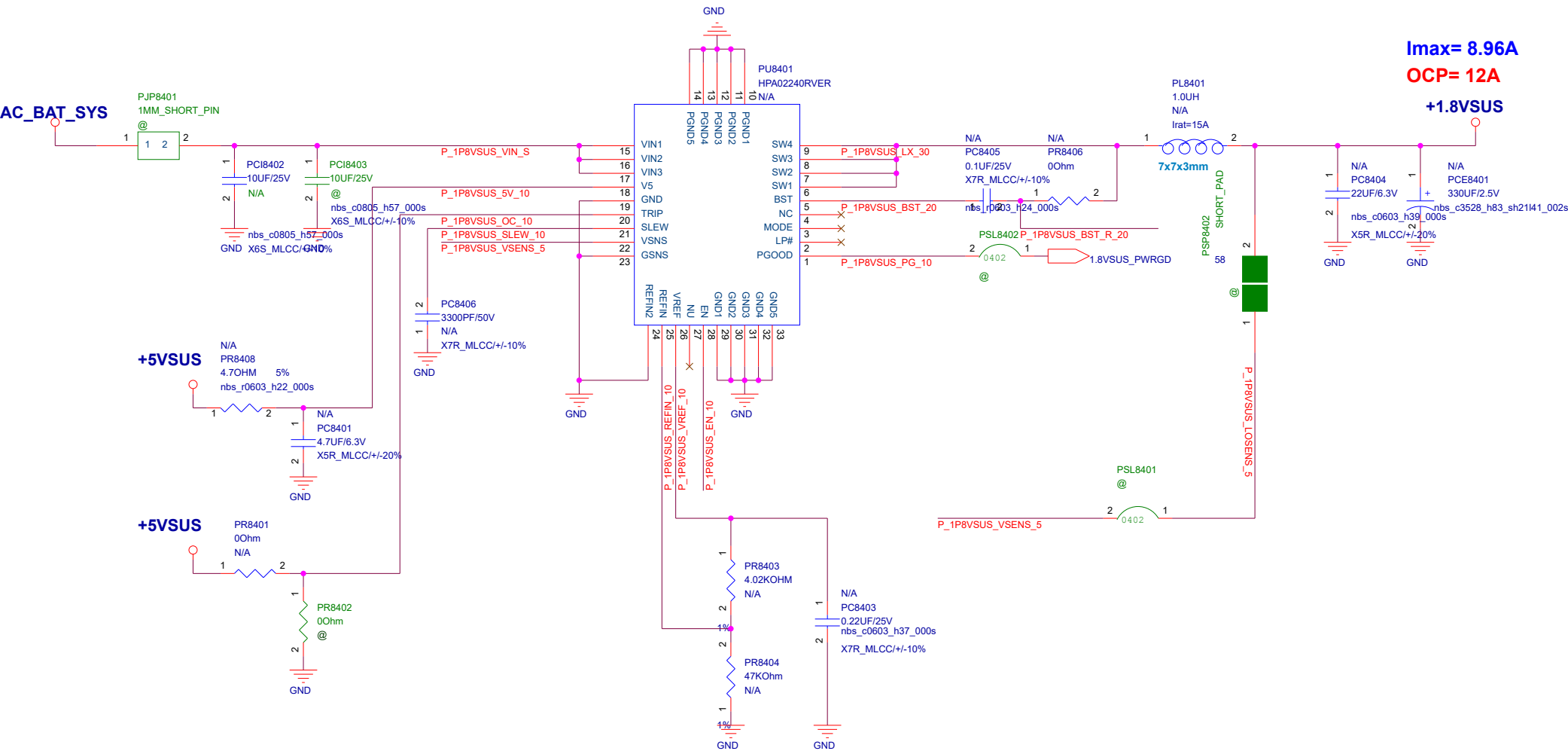
40 OHm_NET
FBC Partition 64..32
MF=0 Normal

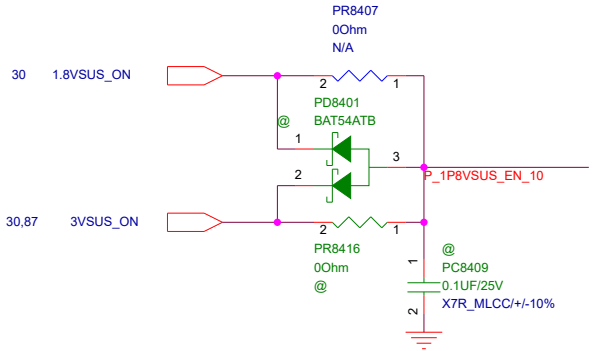




ASUS GX502GX	Project Name		Rev R1.2
Title : VRAM_Channel_C			
Size Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer:	
Date: Tuesday, October 13, 2020	Sheet 75 of 101		

+1.8VSUS [For PCH]

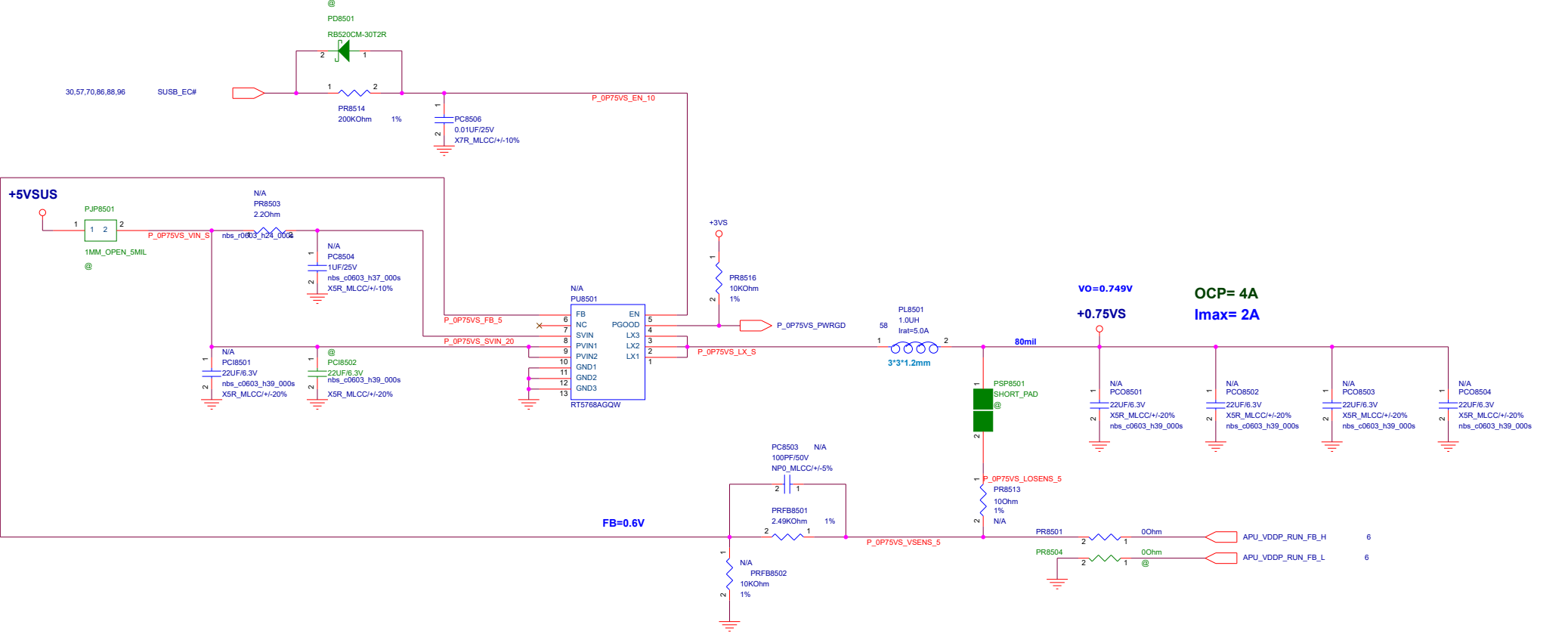




PT840* 請放置 PU8401旁;並請放置Trace 上!

<Variant Name>

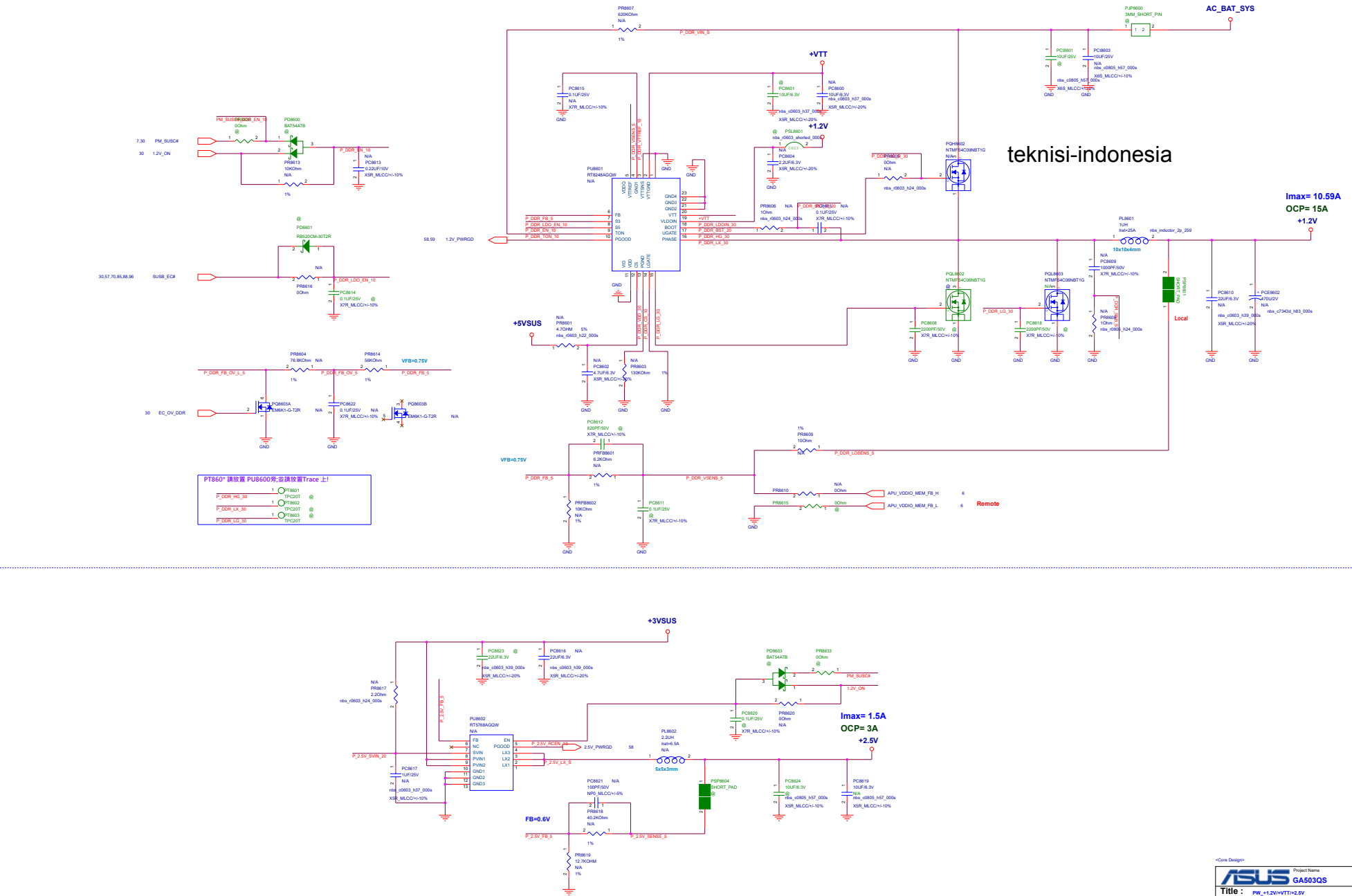
Project Name: GA503QS		Rev: R1.0
Title : PW_+1.8VSUS		
Size: A4	Dept.: NB Power team	Engineer: Power RD
Date: Tuesday, October 13, 2020	Sheet 84 of 103	



<Variant Name>

Project Name: GA503QS		Rev: R1.0
Title : PW_+0.75VS		
Size: A3	Dept.: NB Power team	Engineer: CS Lin
Date: Tuesday, October 13, 2020	Sheet 85 of 104	

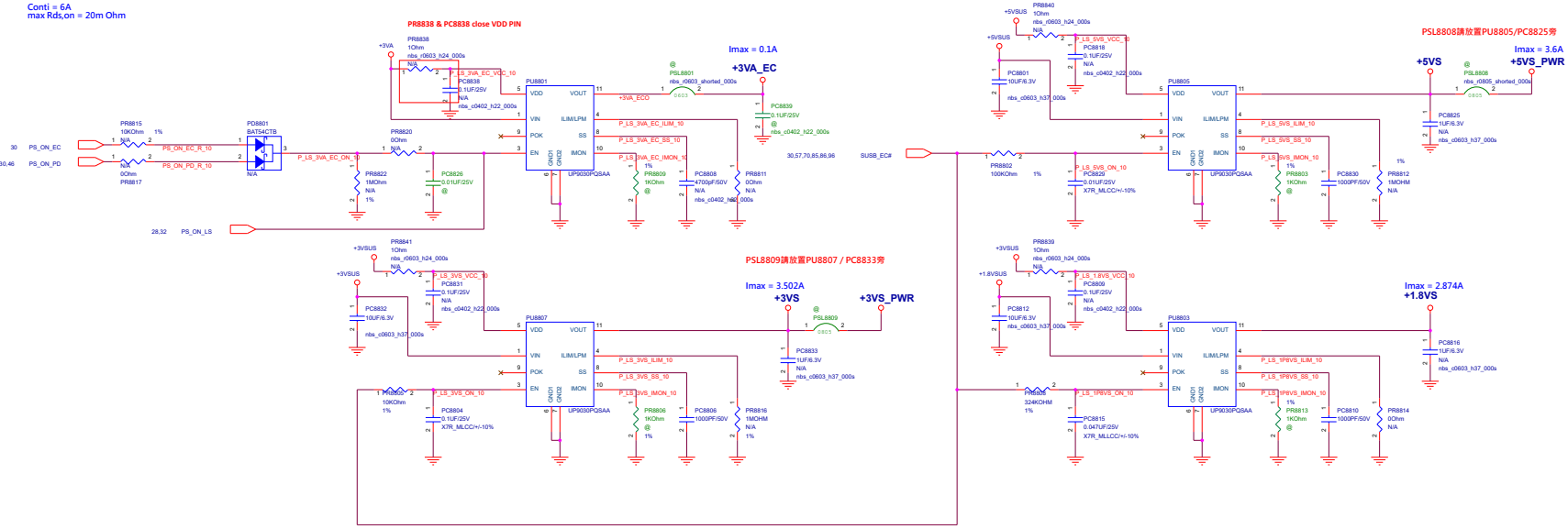
+1.2V / +VTT / +2.5V[For Memory]



uP9030 ILIM/LPM Setting 對應表

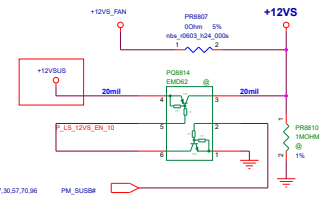
ILIM PIN	LPM	LIMIT Current
GND	Off	3A
1M to GND	Off	5A
Float/VDD	On	8A

Conti = 6A
max Rds,on = 20m Ohm

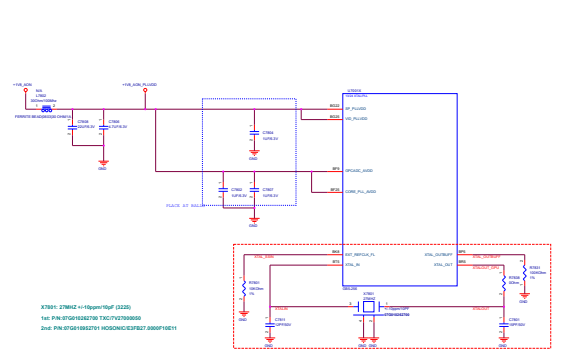


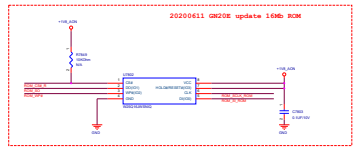
+12VS 的 Vin 對應 BOM 表

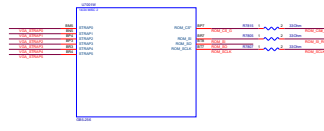
	+12VS_FAN	+12VSUS
PR8807	N/A	@
PR8810	@	N/A
PQ8814	@	N/A

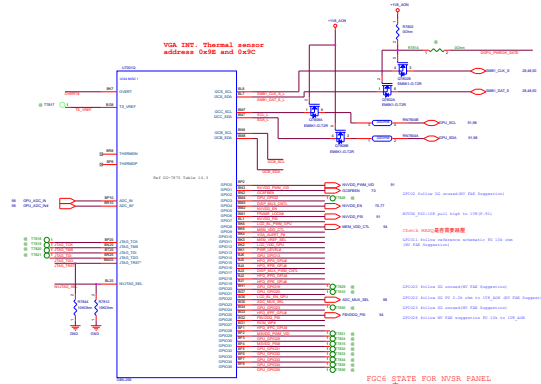


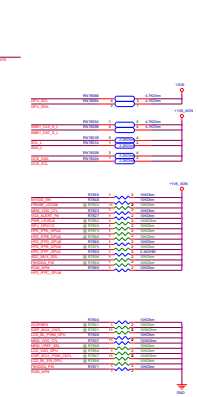
Project Name: GA503QS		Rev: R1.0
Title: PW_LOAD SWITCH		
Size: A2	Dept.: NB Power Team	Engineer: CS Lin
Date: Tuesday, October 13, 2020	Sheet 88 of 104	











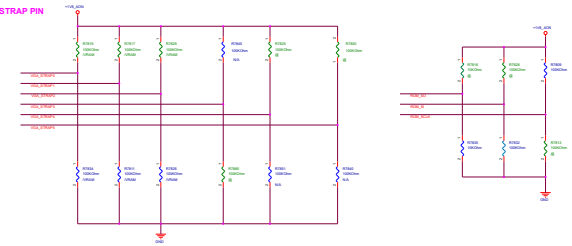


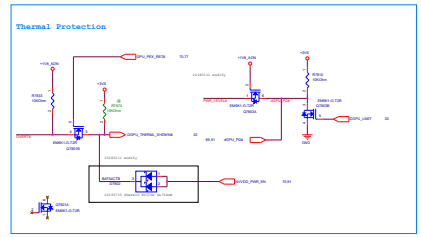
Table 9.1 Ternary Strap Levels

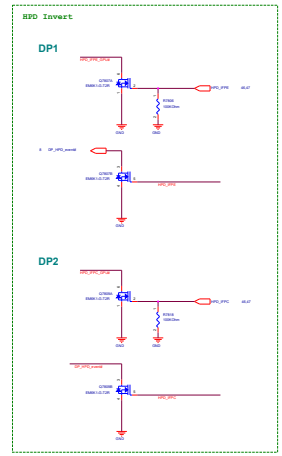
Physical Configuration		
Level Option	Pull-Up to 1.8V via resistor Note 1	Pull-Down to GND via resistor Note 1
1.8V / HIGH 1 Level	Populate	No Stuff
0.9V / MIDDLE 0 Level	Populate	Populate
GND / LOW 1 Level	No Stuff	Populate

Note 1: Resistor should be 100K Ohms. 1.8V rail and GND rail levels within 5% is acceptable.

Table 9.4 FS_OVERT* Strap Enablement

Strap Pins see Note 1			FS_OVERT* Function
ROM_SO see Note 2	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function DISABLED
L	L	H	FS_OVERT* function ENABLED (default)
all other configurations			(invalid, do not configure)





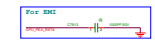


Table 1. GN20-E7 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
16 Gb	2Chx512Mx16	1.35V 1.25V 1.2V[4]	Samsung	K4ZAF325BM-HC14	M-die	0x7	14 Gbps	2028	Full	Production candidate
8 Gb	2Chx256Mx16	1.35V 1.25V 1.2V[4]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001[2]	Full	Production candidate

Table 2. GN20-E5 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.35V	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001[2]	Full	Production candidate
		1.25V	Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate
		1.2V [4]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940 [3]	Full	Production candidate

Table 3. GN20-E3 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.35V	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001[2]	Full	Production candidate
		1.25V	Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate
		1.2V [4]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940 [3]	Full	Production candidate

Table 9.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVI, for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)

Table 9.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVI, for memory configs corresponding to these numbers)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

Table 9.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	M	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

Assorted Configuration Straps:
1. SMB_ALT_ADDR Enable - "0" signal SMB conflicting I2C address 0x9E, "1" load GPU with 0x9E address and 0x9C, read address assumed GPU
2. DEVID_SEL: G-sync function – "0" normal GPU ID, "1" support G-sync GPU ID.
3. PCIE_CFG: PCIE Swing – "0" PCIE Swing default, "1" PCIE swing reduce.
4. VGA_DEVICE: Graphics circuit – "0" MS-Hybrid, "1" Discrete.

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

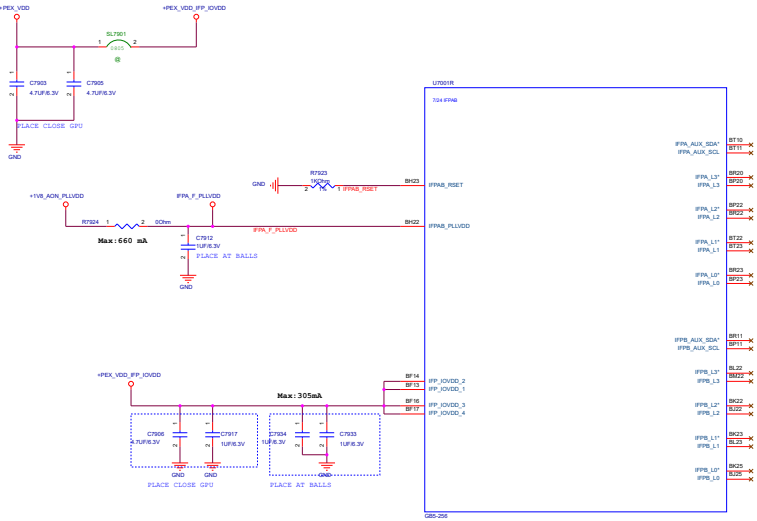
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

DEFULT : L L H

Title :	GPU_CLOCK/STRAP/GPIO					
Size :	Document Number :		Rev :			
Date :	Sheet : of :					



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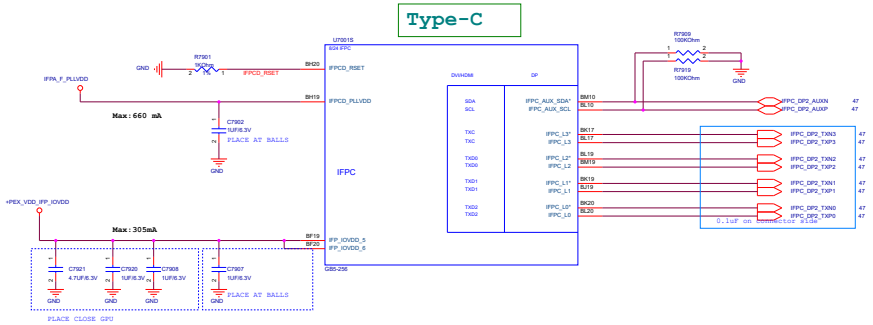
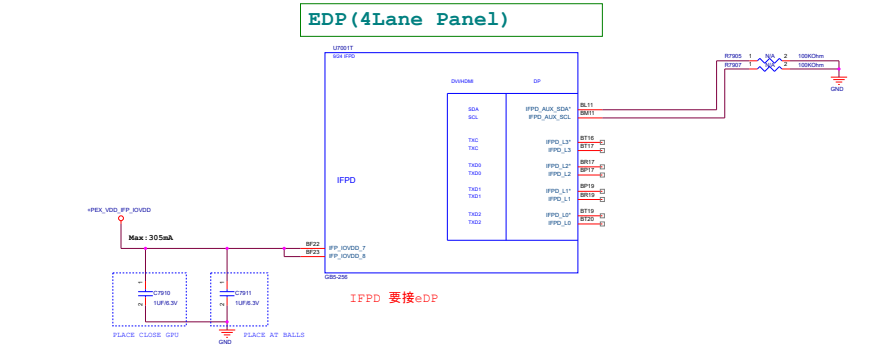
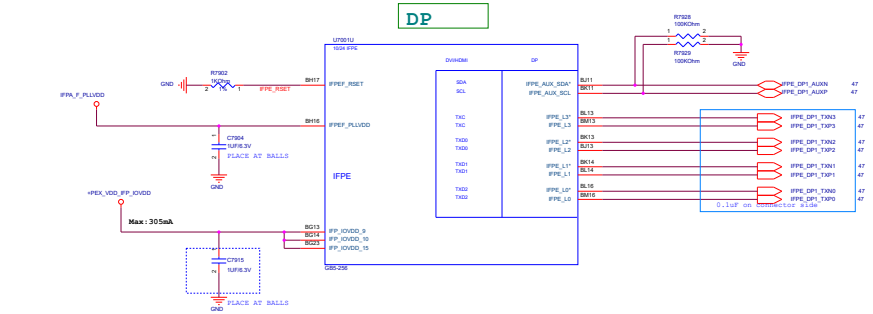


EDP(4Lane Panel)

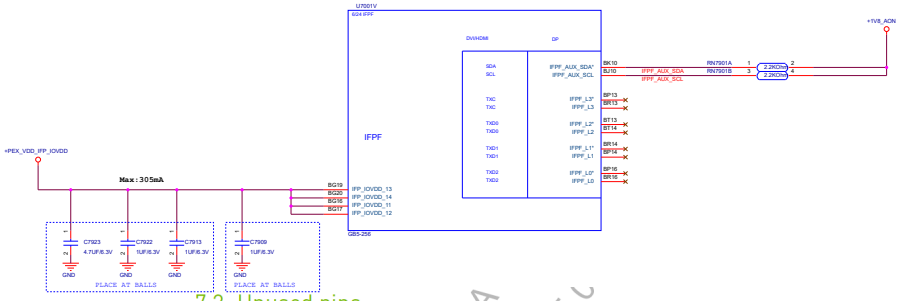


IFPD 要接eDP

DP



IFPF(not used)

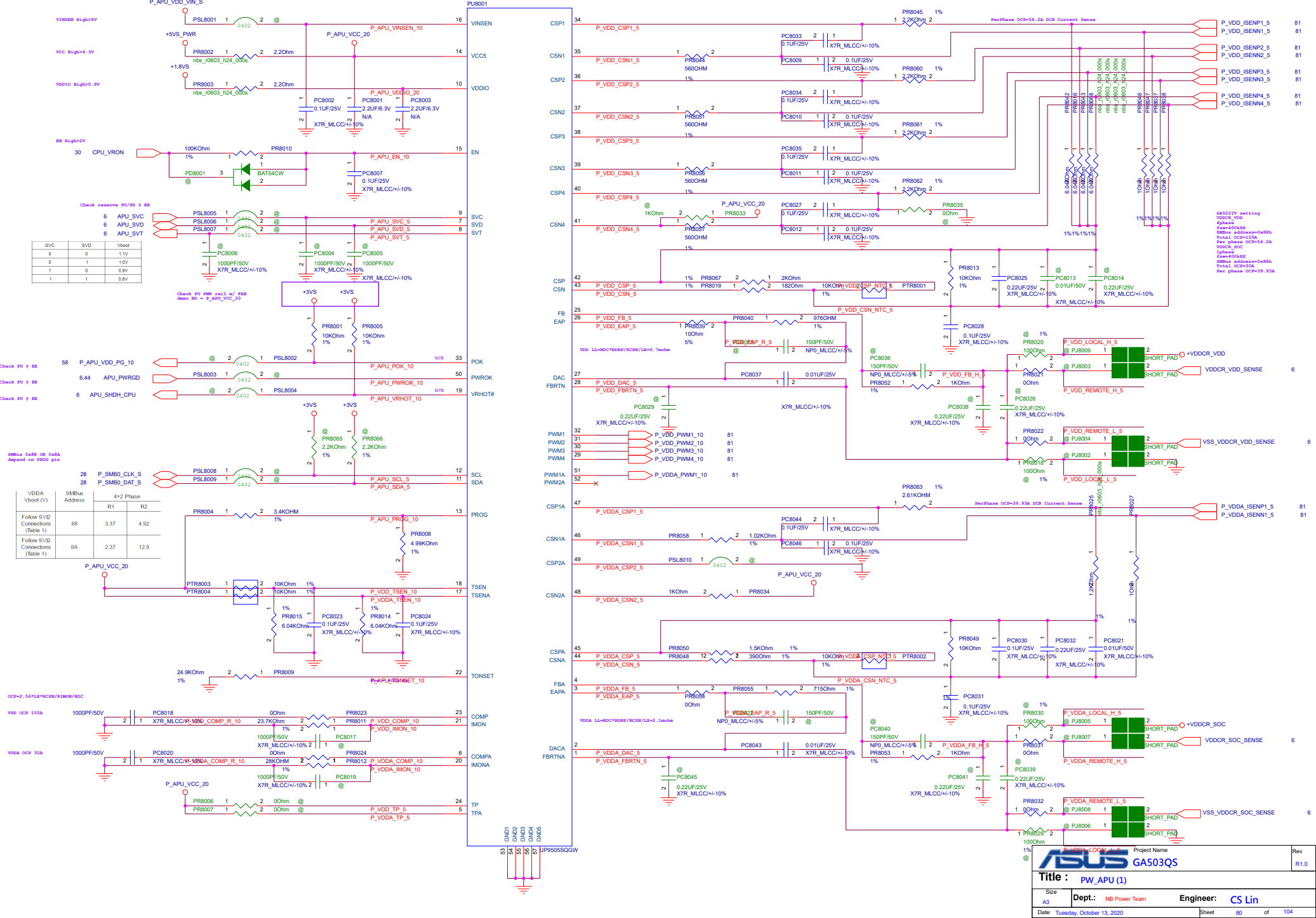


7.2 Unused pins

If an IFP link is unused, in general it should be left unconnected. This includes Main and Aux links. IFPxy_RSET and IFPxy_PLLVDD (xy = AB,CD,EF) can be left unconnected if neither of IFPx / IFPy is in use. For example, if neither link of the IFPA/IFPB macro is to be used, then IFPAB_PLLVDD and IFPAB_RSET should be left unconnected, and all signals and references associated with Link A and Link B should also be left unconnected.

IFP_IOVDD rail can be left unconnected if no IFP link is used. If any IFP is used; all IFP_IOVDD balls must be connected to power rail.

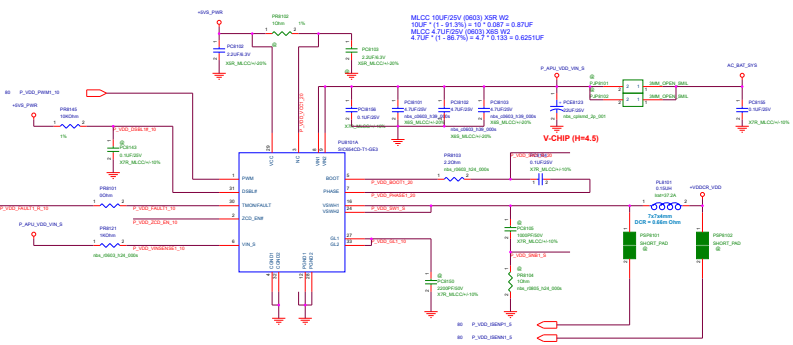
ASUS	Project Name: GA503QS		Rev: IR1.3
Title :	GPU_DP/EDP/HDMI/LVDS/CRT		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1	
Date: Tuesday, October 13, 2020	Sheet 79 of 104		

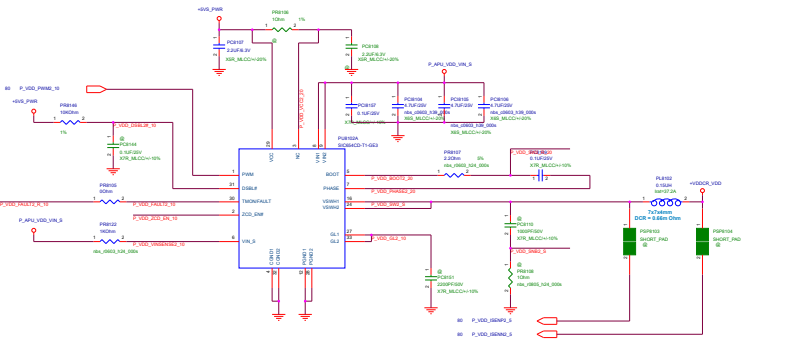


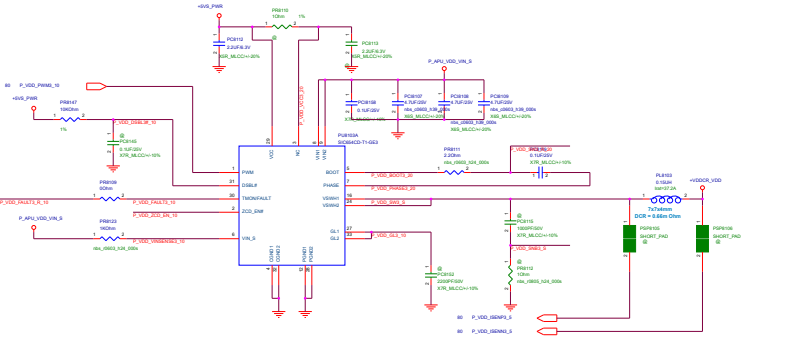
SVC	SVD	Vboot
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

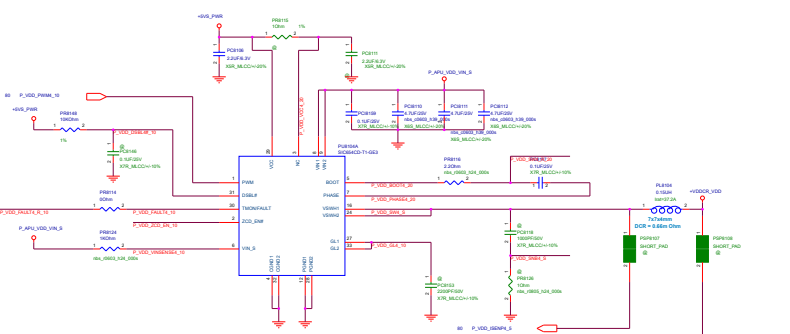
VDDA Vboot (V)	SMBus Address	4+2 Phase	
		R1	R2
Follow SVI2 Connections (Table 1)	88	3.37	4.92
Follow SVI2 Connections (Table 1)	8A	2.37	12.8

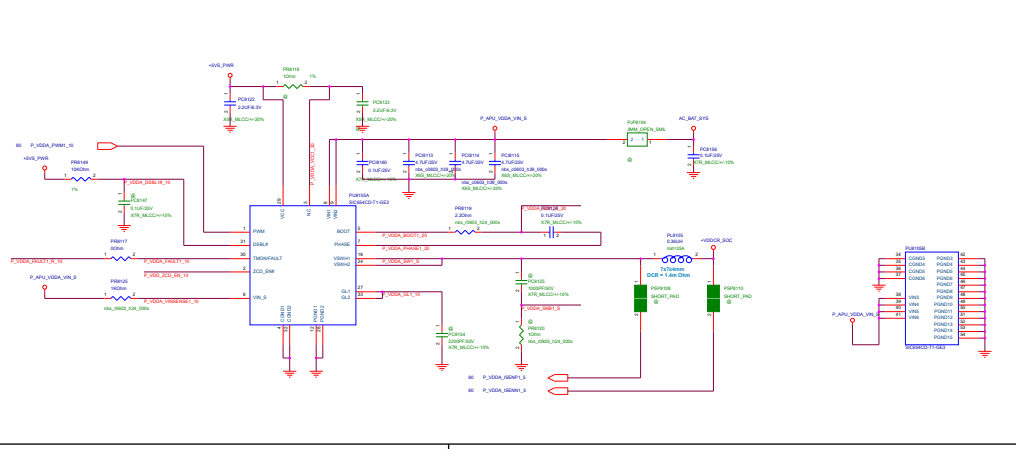
Project Name	GA503QS		Rev R1.0
Title :	PW_APU (1)		
Size A3	Dept.: NB Power Team	Engineer: CS Lin	
Date: Tuesday, October 13, 2020	Sheet 80 of 104		



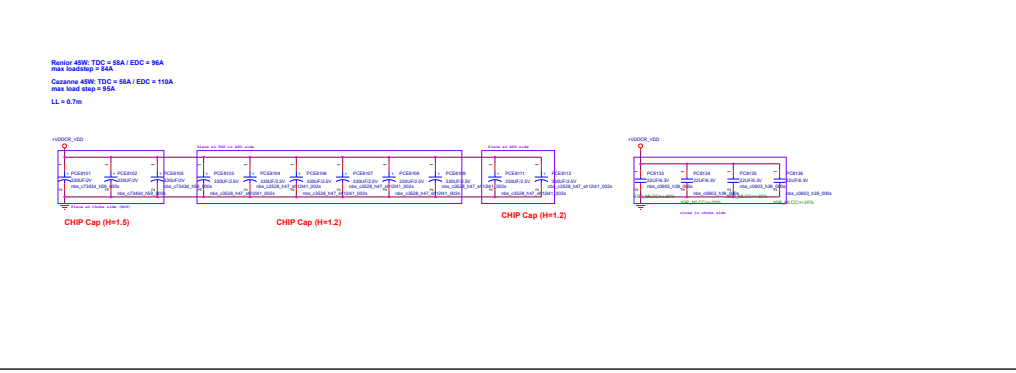


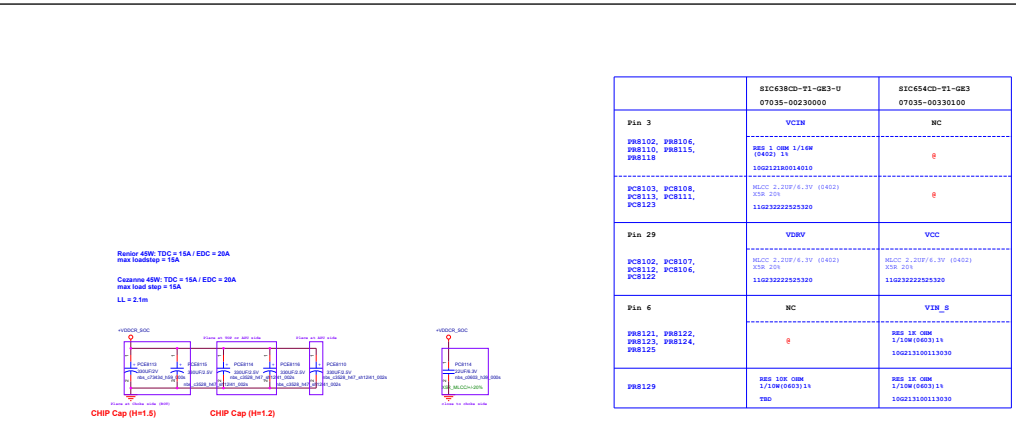






teknisi-indonesia

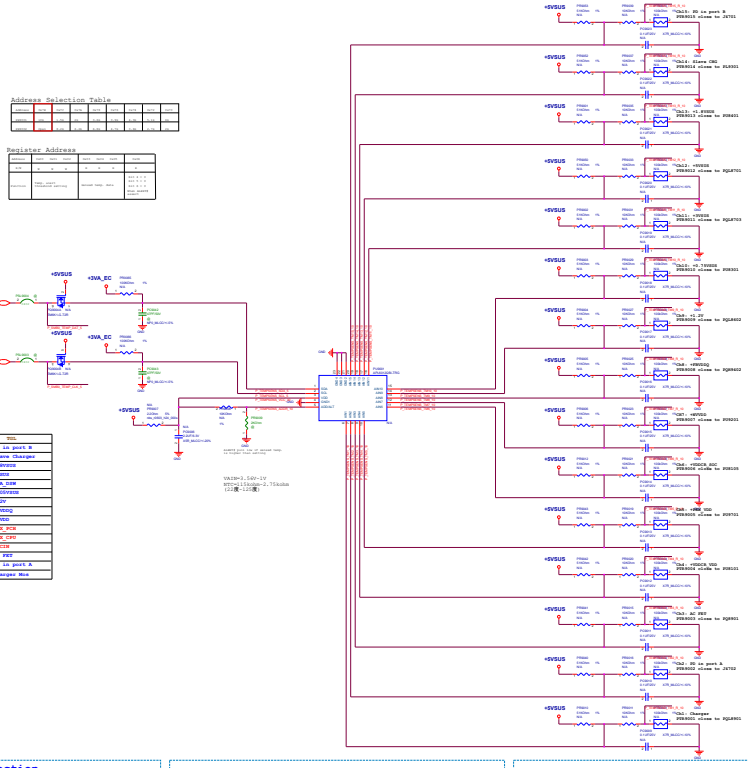




	SIC638CD-T1-GE3-U 07035-00230000	SIC654CD-T1-GE3 07035-00330100
Pin 3 PR8102, PR8106, PR8110, PR8115, PR8118	VCIN RES 1 OHM 1/16W (0402) 1% 10G2121800140l0	NC @
PC8103, PC8108, PC8113, PC8111, PC8123	MLCC 2.2UF/6.3V (0402) X5R 20% 11G2322225253z0	@
Pin 29 PC8102, PC8107, PC8112, PC8106, PC8122	VDRV MLCC 2.2UF/6.3V (0402) X5R 20% 11G2322225253z0	VCC MLCC 2.2UF/6.3V (0402) X5R 20% 11G2322225253z0
Pin 6 PR8121, PR8122, PR8124, PR8125	NC @	VIN_S RES 1K OHM 1/10W(0603)1% 10G2131001130z0
PR8129	RES 10K OHM 1/10W(0603)1% TBD	RES 1K OHM 1/10W(0603)1% 10G2131001130z0

Project Name	GA503QS		Rev 0.0
Title :	PW_APU (2)		
Size: A1	Dept.: NB Power Team	Engineer: CS Lin	
Date: Tuesday, October 13, 2020	Sheet 61 of 104		

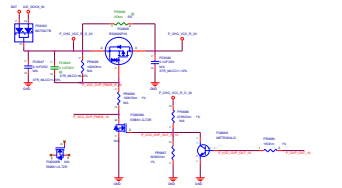
P90_PROTECTION



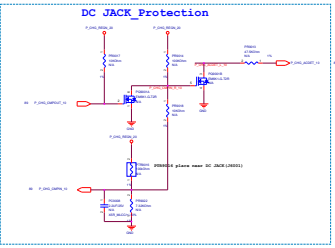
MISC	CHG	THOL
CH15	PD in port B	PD in port B
CH14	Slave Charger	Slave Charger
CH13	1.8V5DS	1.8V5DS
CH12	3V5DS	3V5DS
CH11	3VA_DSW	3VA_DSW
CH10	1.05V5DS	1.05V5DS
CH09	1.2V	1.2V
CH08	PWV5DQ	PWV5DQ
CH07	3V5DQ	3V5DQ
CH06	Vsa	AOZ_PCH
CH05	VGT	AOZ_CPU
CH04	VCC5S	VCC5S
CH03	AC_PRT	AC_PRT
CH02	PD in port A	PD in port A
CH01	Charger Mux	Charger Mux

MISC	ABC
CH15	PD in port B
CH14	Slave Charger
CH13	1.8V5DS
CH12	3V5DS
CH11	3VA_DSW
CH10	0.75V5DS
CH09	1.2V
CH08	PWV5DQ
CH07	3V5DS
CH06	VSOCH_SDC
CH05	PDC_VCC
CH04	VSOCH_VSS
CH03	AC_PRT
CH02	PD in port A
CH01	Charger Mux

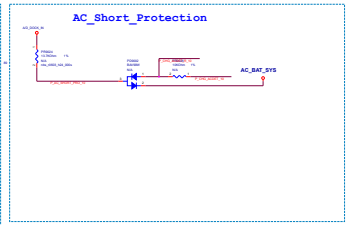
VCC pin OVP Protection circuit 24V



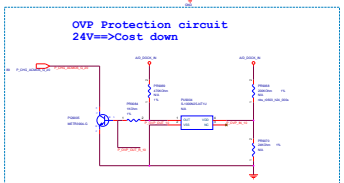
DC_JACK_Protection



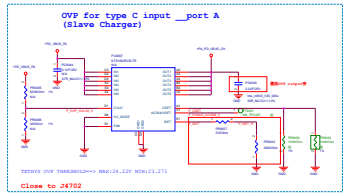
AC_Short_Protection



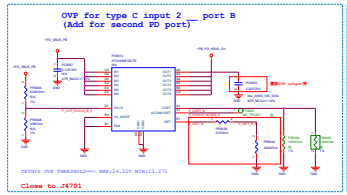
OVP Protection circuit 24V==>Cost down



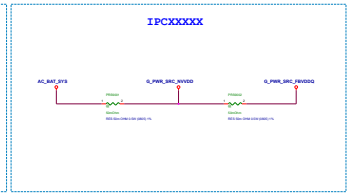
OVP for type C input __port A (Slave Charger)



OVP for type C input 2___ port B (Add for second PD port)

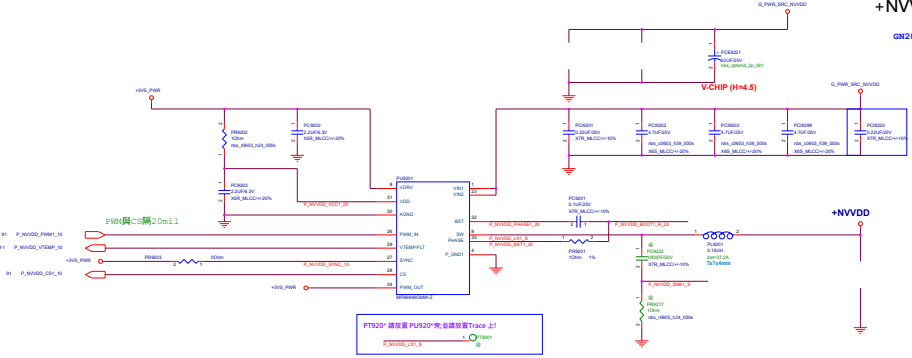


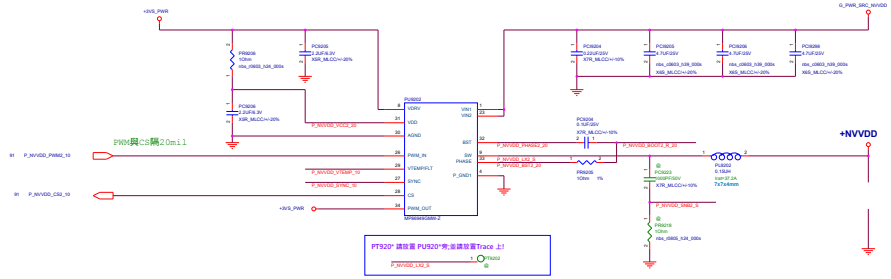
IPCXXXXX

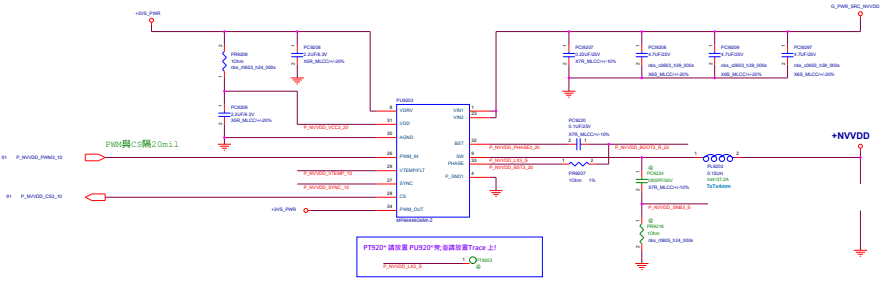


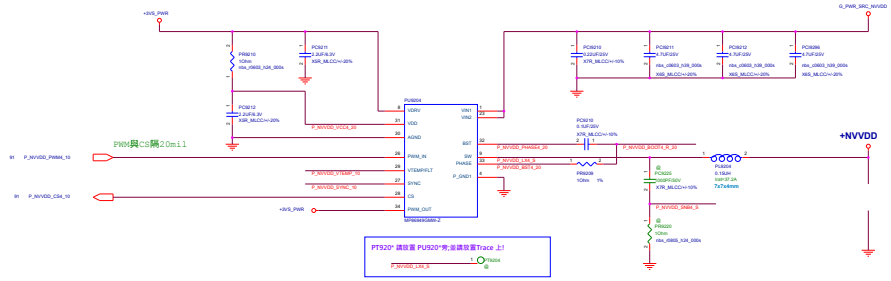
Title :	P90_PROTECTION
Size : A0	Project : All Project Type
Engineer :	0525120926
Date : Monday, October 19, 2020	Sheet 1 of 1

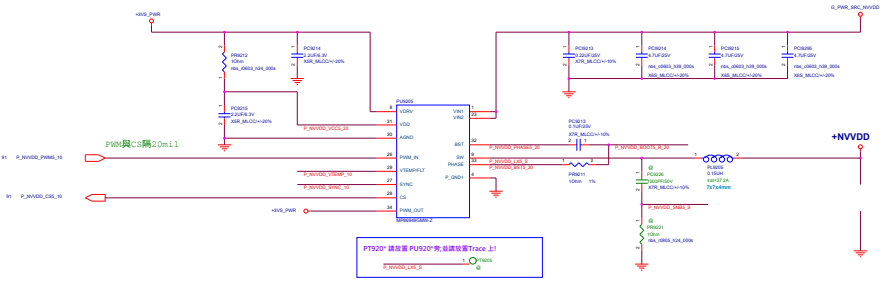
Title <Title>		
Size A3	Document Number GA503QS	Rev <RevCode>
Date: Tuesday, October 13, 2020	Sheet 82 of 104	

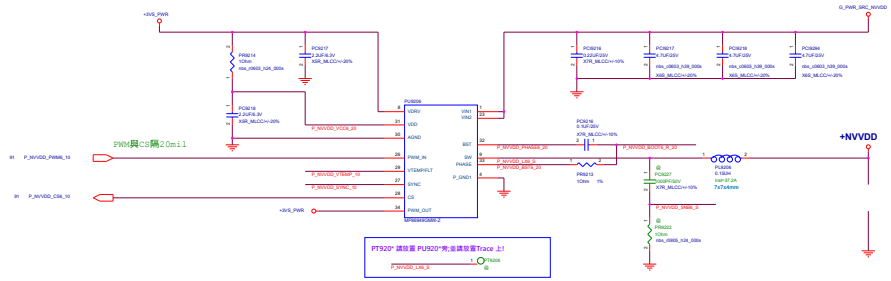


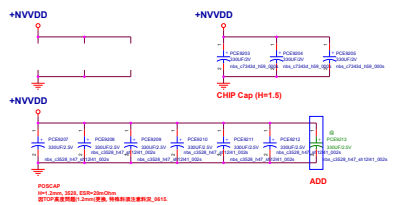












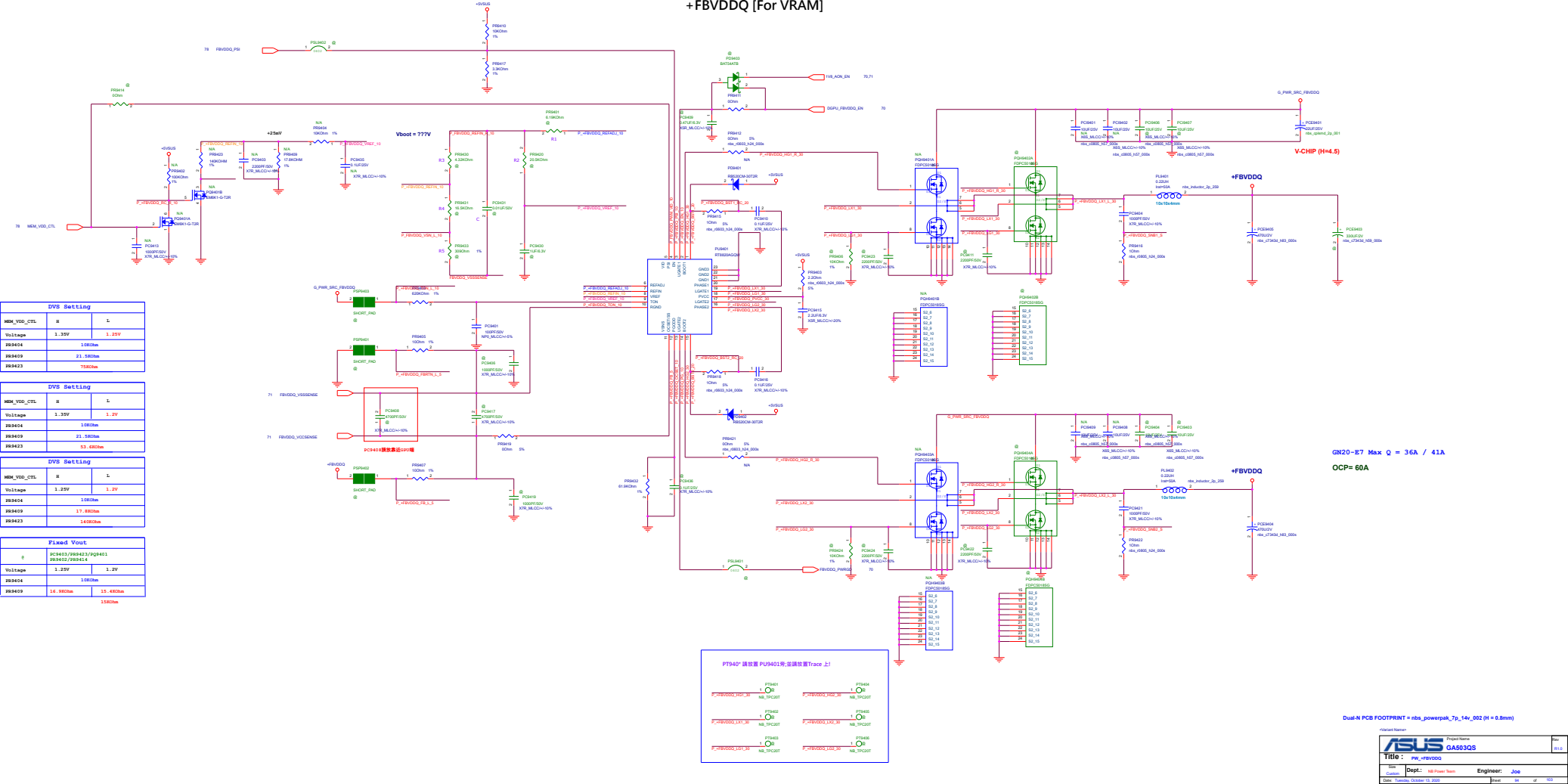
+NVVDD [For DGPU]

GN20-E7 Max Q = 86A / 300A (OCP = xxxA)

<Core Design>

Project Name GU603H/GX703H	Rev R1.0
Title : PW_+NVVDD (2)	
Size D	Dept.: NB Power team Engineer: Power
Date: Tuesday, October 13, 2020	Sheet 92 of 104

+FBVDDQ [For VRAM]



DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.35V	1.25V
PR9404	10KOhm	
PR9409	21.5KOhm	
PR9423	75KOhm	

DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.35V	1.2V
PR9404	10KOhm	
PR9409	21.5KOhm	
PR9423	53.6KOhm	

DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.25V	1.2V
PR9404	10KOhm	
PR9409	17.8KOhm	
PR9423	140KOhm	

Fixed Vout	
@	PC9403/PR9423/PQ9401 PR9422/PR9414
Voltage	1.25V / 1.2V
PR9404	10KOhm
PR9409	16.9KOhm / 15.4KOhm
	150Ohm

PC9408請放最近GPU端

PT940* 請放置 PU9401旁;並請放置Trace 上!

Vboot = 777V

+25mV

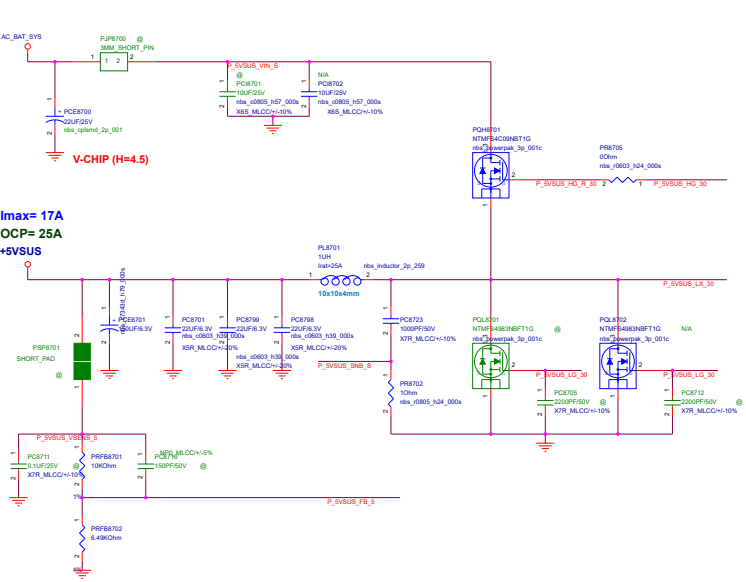
GN20-E7 Max Q = 36A / 41A

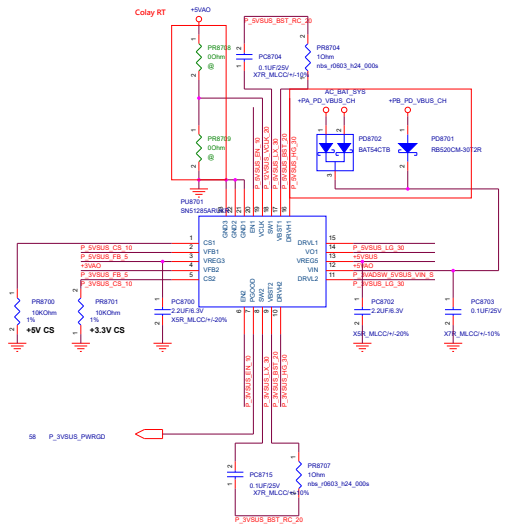
OCP= 60A

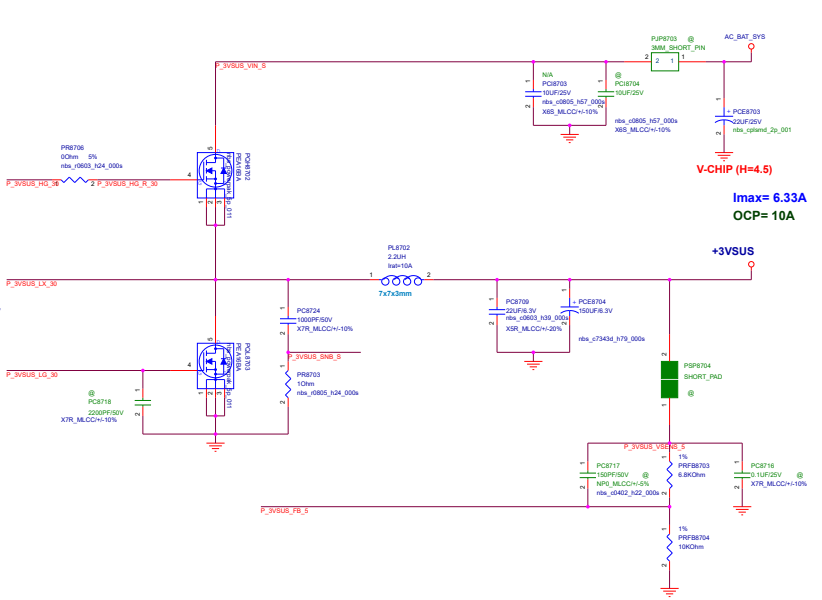
Dual-N PCB FOOTPRINT = nbs_powerpak_7p_14v_002 (H = 0.8mm)

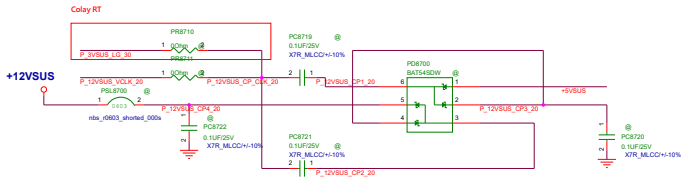
ASUS
Project Name: GA503QS
Rev: R1.0
Title : PW_+FBVDDQ
Size: Custom
Dept.: NB Power Team
Engineer: Joe
Date: Tuesday, October 13, 2020
Sheet 84 of 103

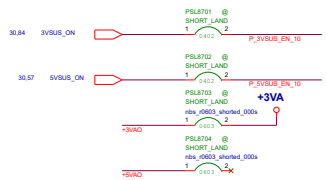
+3VA_DSW / +5VSUS [System Power]











請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm

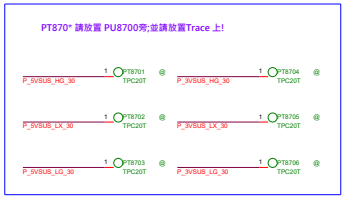
Adaptor Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0

PT870* 請放置 PU8700旁;並請放置Trace 上!



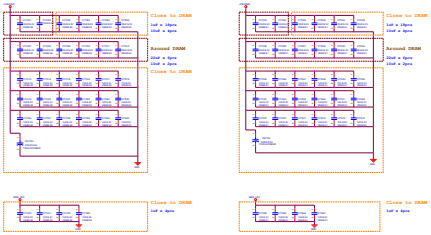
<Variant Name>

ASUS	Project Name: GA503QS	Rev: R1.0
Title : PW_+3VSUS/+5VSUS		
Size: A2	Dept.: NB Power team	Engineer: Joe
Date: Tuesday, October 13, 2020	Sheet 87 of 103	

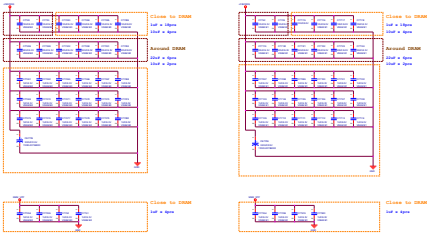
FBVDDQ
VRAM side

FBVDDQ
GPU side

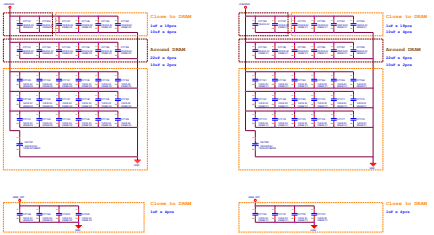
Channel A



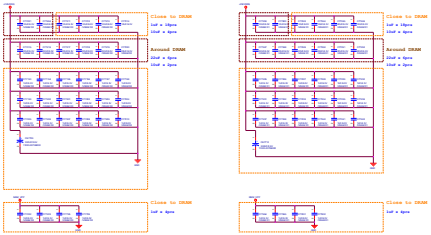
Channel B



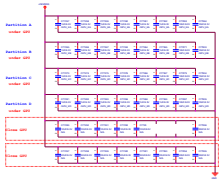
Channel C



Channel D



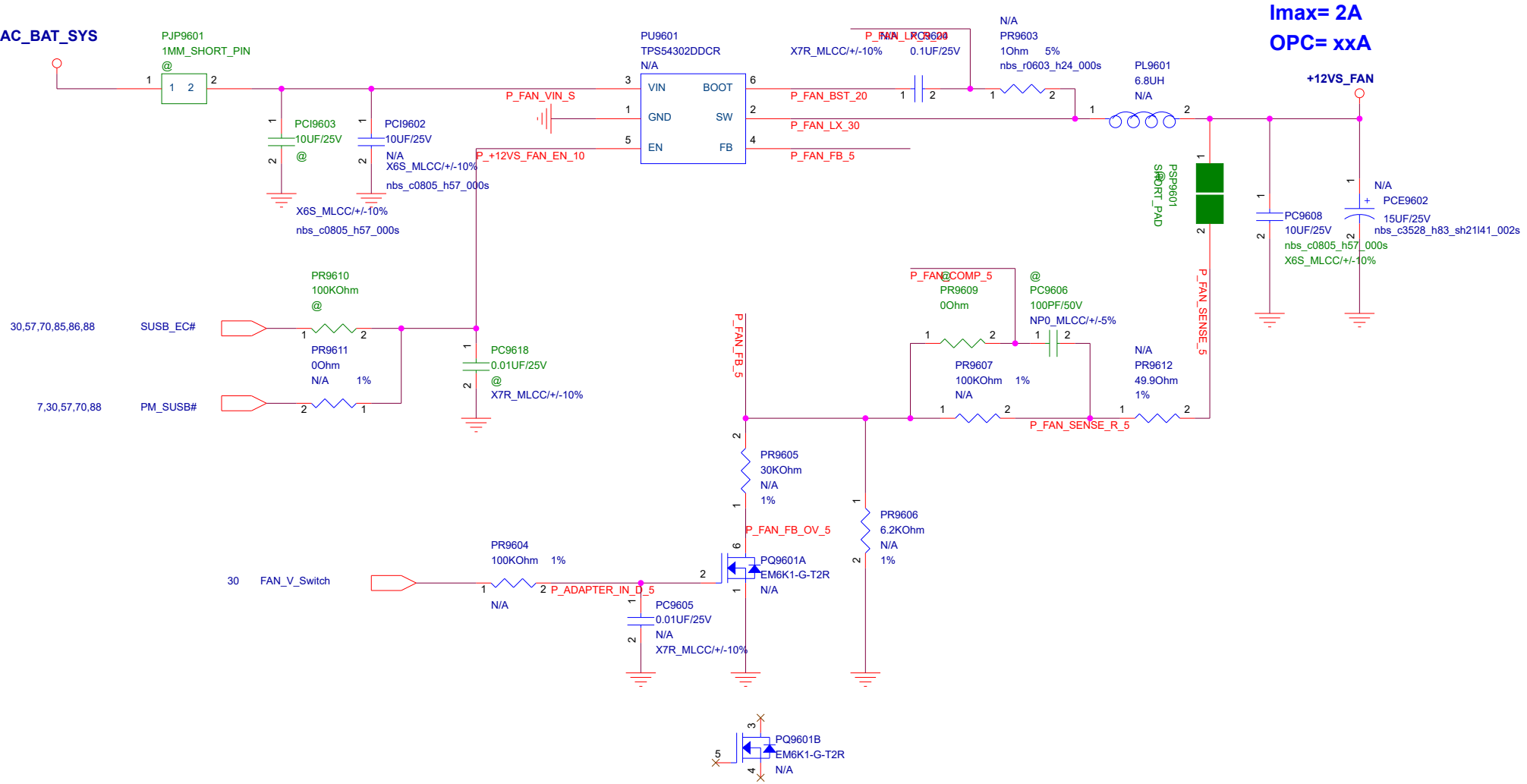
VRAM PWR_FBVDDQ



For power sequence measurement

Title <Title>		
Size A	Document Number GA503QS	Rev <RevCode>
Date: Tuesday, October 13, 2020	Sheet 95 of 104	

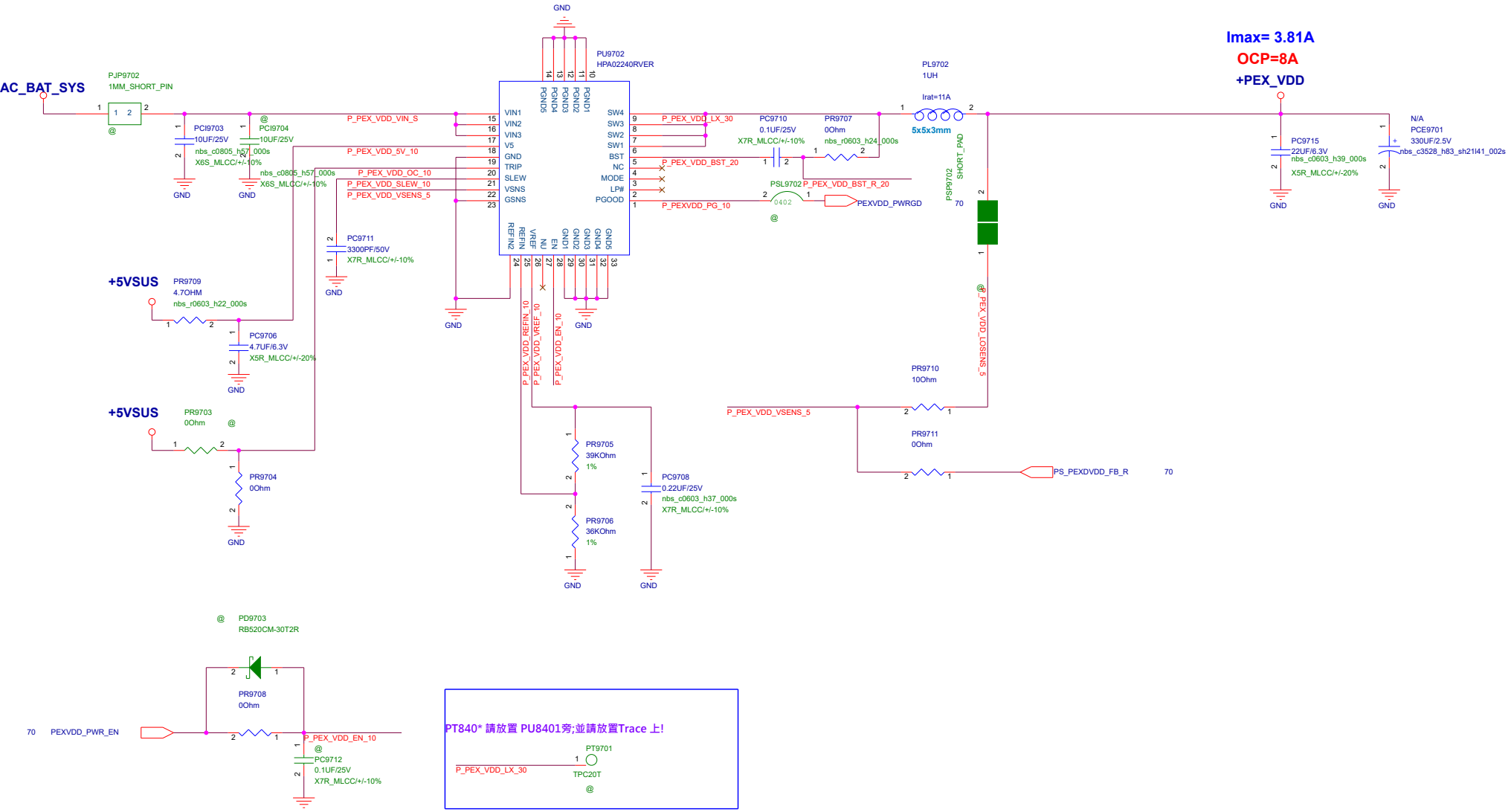
+12VS_FAN [For FAN]



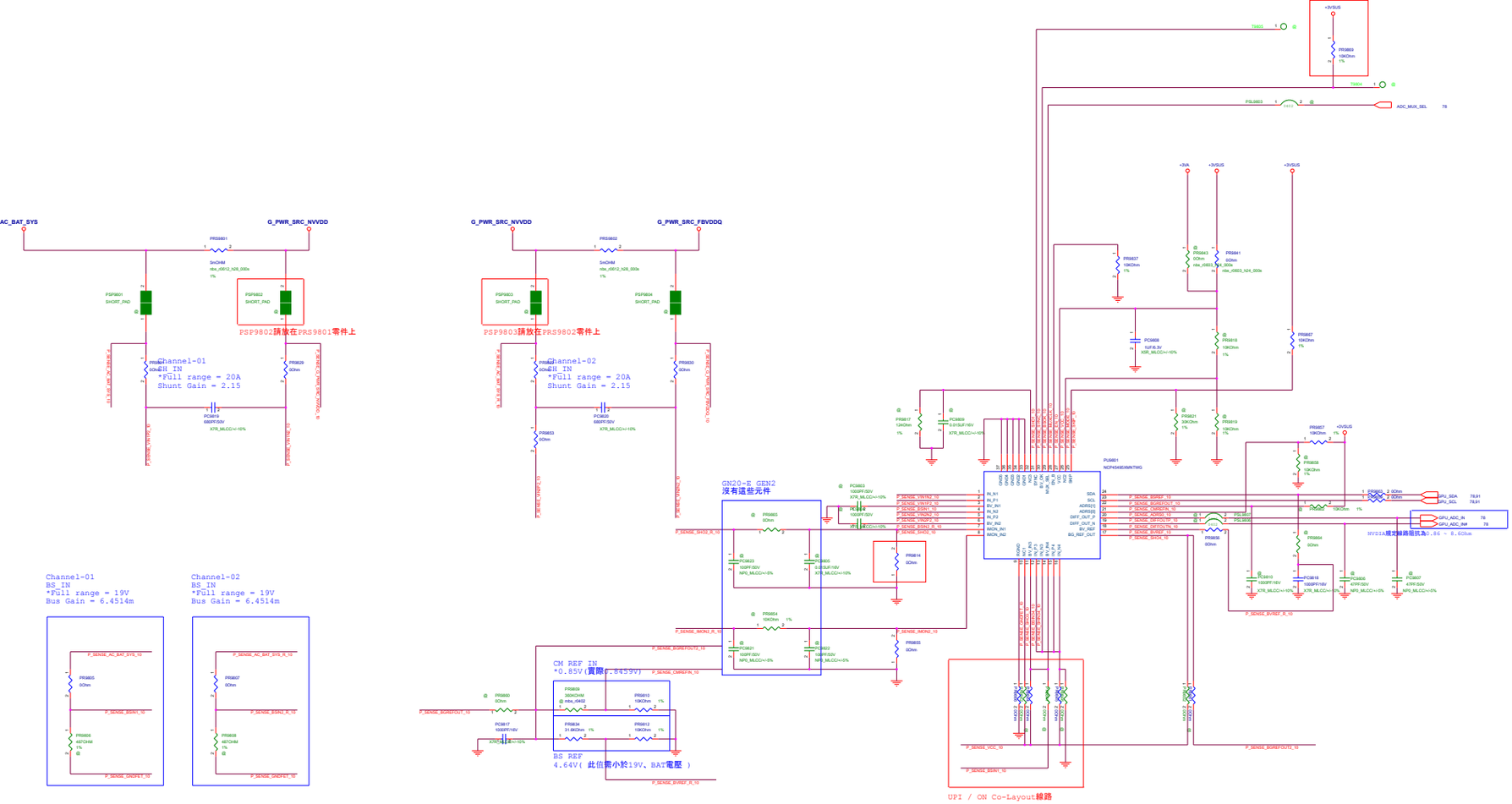
<Variant Name>

Project Name: GA503QS		Rev: R1.0
Title : PW_+12VS_FAN		
Size: A4	Dept.: NB Power team	Engineer: Power RD
Date: Tuesday, October 13, 2020	Sheet 96 of 103	

PEX_VDD [For GPU]



Project Name: **Project Name**		Rev: R1.0
Title : *****		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: Power RD	
Date: Tuesday, October 13, 2020	Sheet 97 of 103	



	PU9801	PR9805	PR9807	PC9803	PC9804	PC9805	PR9814	PR9855	PR9822
GN20	NCP45495XMNTWG 06129-00220000	0 Ohm 10G212000004030	0 Ohm 10G212000004030	@	@	@	0 Ohm 10G212000004030	0 Ohm 10G212000004030	0 Ohm 10G212000004030
N18P-G1	UP9026QQKI 06129-00110100	75KOhm 10G212750214010	75KOhm 10G212750214010	1000PF/50V 11G232110214321	1000PF/50V 11G232110214321	0.015UF/16V 11G232115311360	357Ohm 10G212357014010	@	49.9Ohm 10G21249R914010

	PC9810	PR9860	PR9809	PR9810	PR9834	PR9863	PR9859	PC9809	PR9808
GN20	@	@	@	10KOhm 10G212100214010	31.6KOhm 10G212316214010	0 Ohm 10G212000004030	0 Ohm 10G212000004030	@	@
N18P-G1	1000PF/16V 11G232110211030	0 Ohm 10G212000004030	360KOhm 10G212364004010	680KOhm 10G212680314010	324KOhm 10G212324314010	@	@	0.015UF/16V 11G232115311360	487Ohm 10G212487014010

	PR9806	PR9861	PR9864	PR9857	PR9801	PR9853	PR9817	PR9844/PR9845	PR9846/PR9847
GN20	@	0 Ohm 10G212000004030	@	10KOhm 10G212100214010	0 Ohm 10G212000004030	0 Ohm 10G212000004030	@	0 Ohm 10G212000004030	@
N18P-G1	487Ohm 10G212487014010	@	0Ohm 10G212000004030	@	100hm 10G212100014010	49.9Ohm 10G21249R914010	357Ohm 10G212357014010	@	0 Ohm 10G212000004030

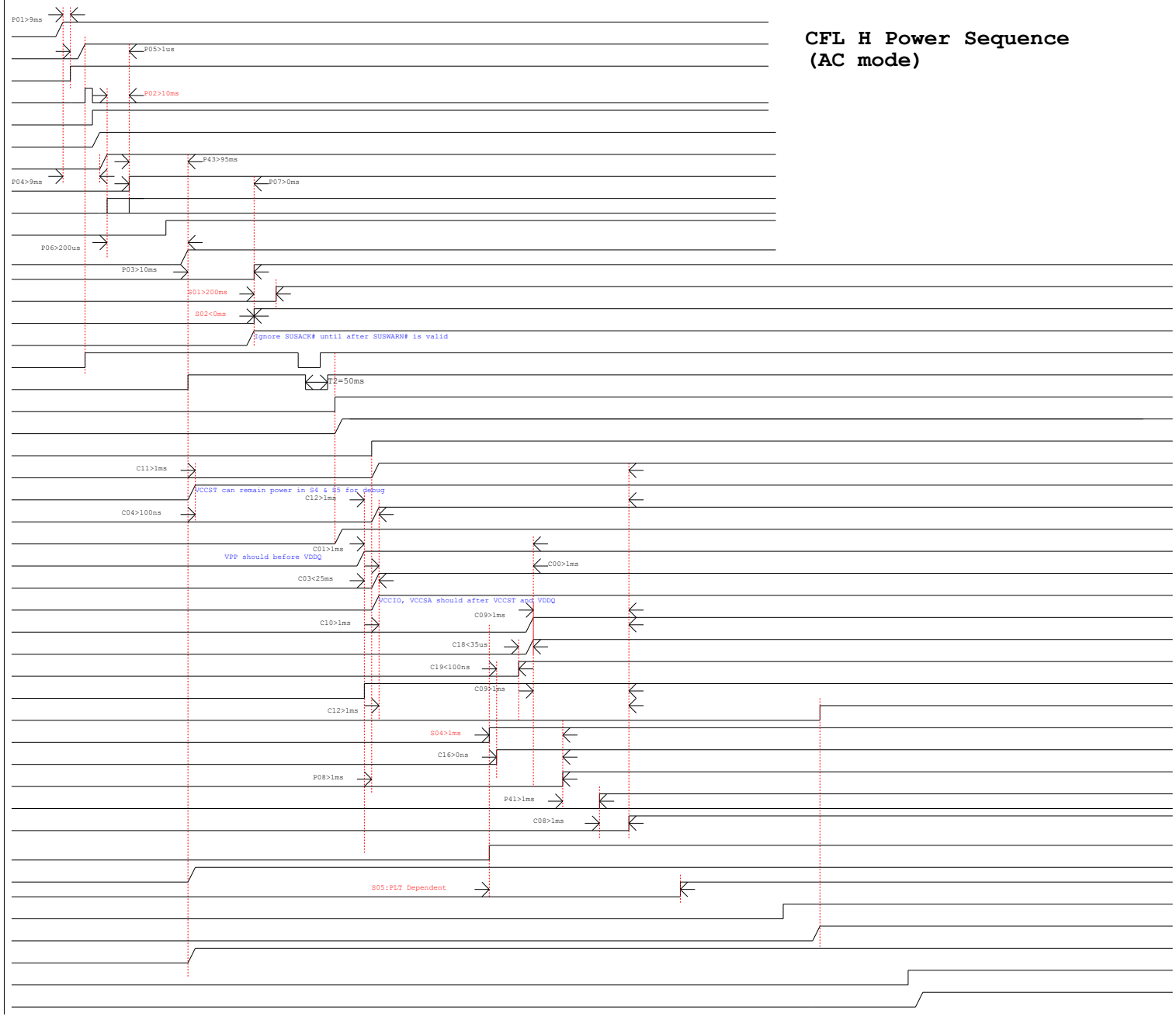
	PR9866	PR9818/PR9819	PR9821	PC9820
GN20	0 Ohm 10G212000004030	@	@	680PF/50V 11G232168114030
N18P-G1	@	10KOhm 10G212100214030	30KOhm 10G212300214010	0.1UF/25V 11203-0087F000

AC-IN Mode

CFL H Power Sequence (AC mode)

C:CPU
P:PCH
S:PLT
Power
Signal

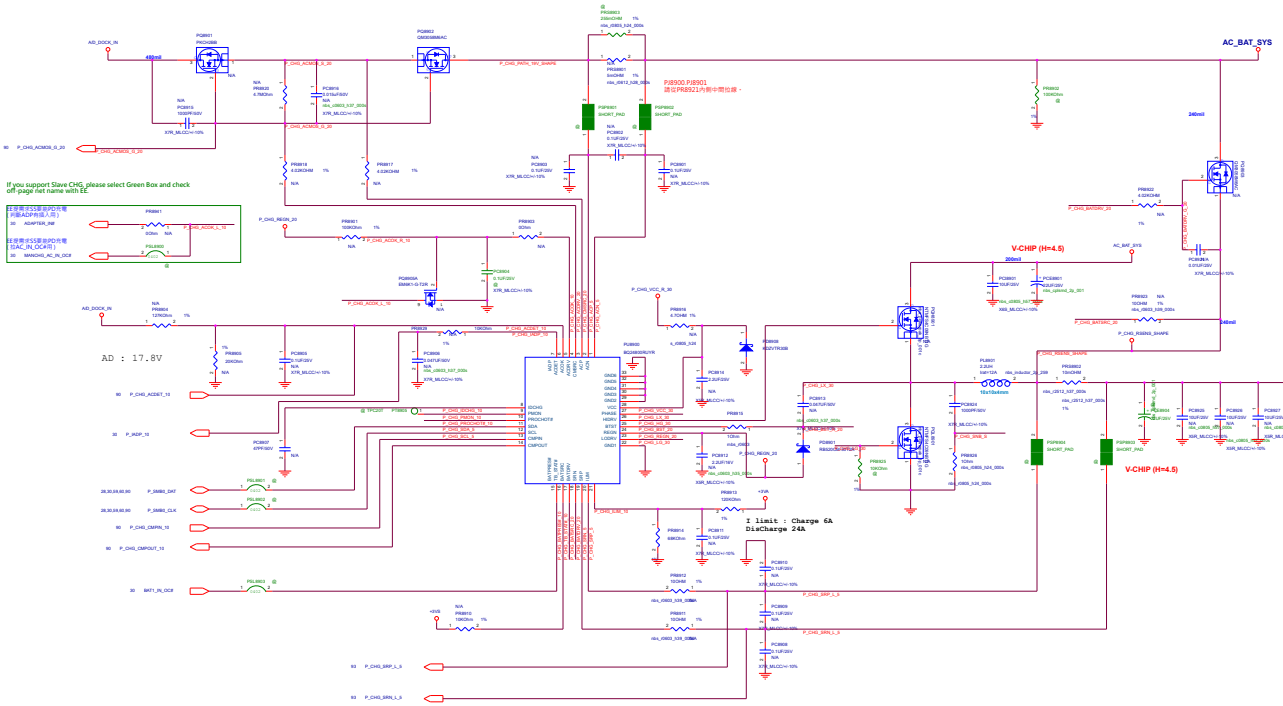
(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#) +12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#) +12VS/+5VS/+3VS
(SUSB_EC#) +1.0V_VCCST, VCCPLL
(SUSB_EC#) +VCCIO, (+12VS) +VCCSTG
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
(+12VS) +VCCPLL_OC
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL) +0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT



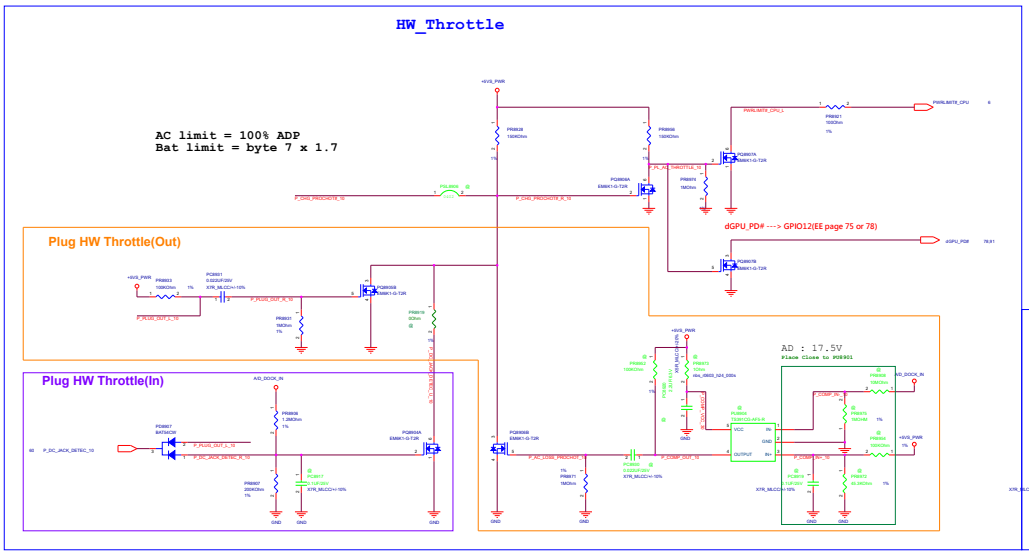
ASUS	Project Name: GA503QS		Rev: 1.0
Title : Power On Timing--AC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1	
Date: Tuesday, October 13, 2020	Sheet 100 of 104		

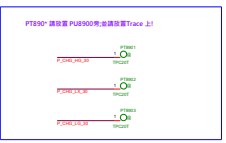
Main Board

PRS8901	ADP<120W	ADP<=230W	ADP>230W	ADP>330W
	TBD	5m	5m	2m
	TBD	10125-0008B100	10108-0006B000	10108-0008B000

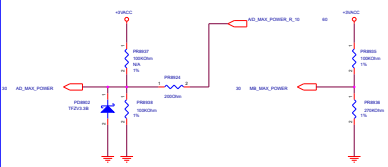


teknisi-indonesia





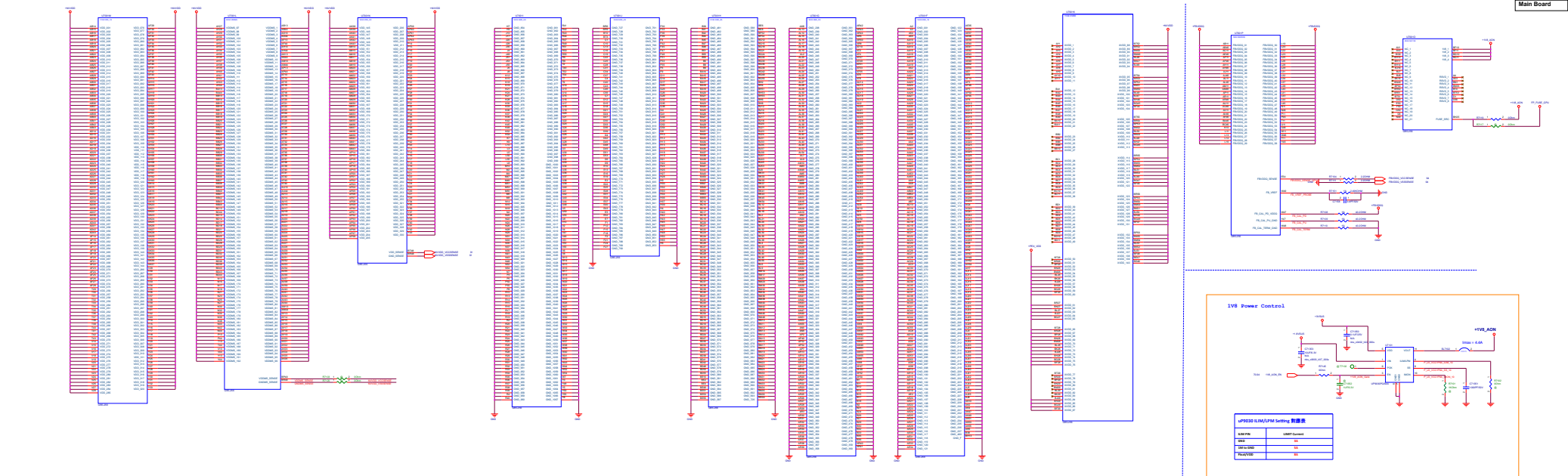
Adaptor select
total power = 90% ADP



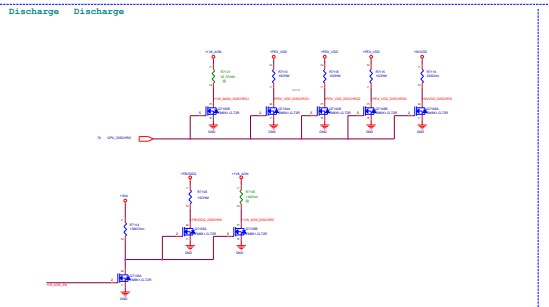
Adaptor select

PRS8901		X Series 10m	X Series 5m
PR8936			
14K (1002121401403)	0.4V	45W	120W
31.6K (1002121401403)	0.8V	150W	150W
56K (1002121401403)	1.2V	180W	180W
93.1K (1002121401403)	1.6V	65W	230W
150K (1002121501403)	2.0V	NA	280W
270K (1002121701403)	2.4V	90W	200W
560K (1002121901403)	2.8V	120W	240W

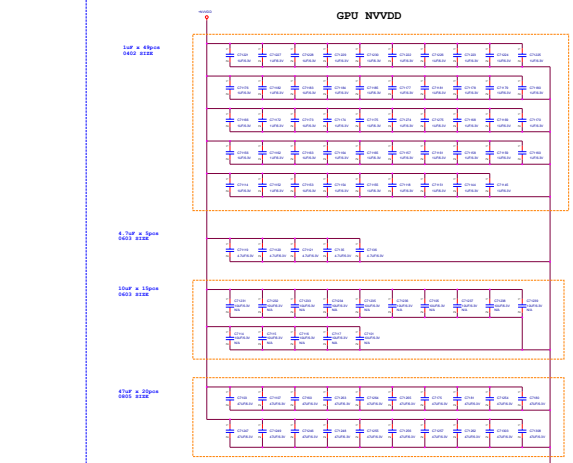
ASUS	Project Name: GA503QS		Rev: R1.0
Title: PW_CHARGER			
Size: A3	Dept.: MB Power Team	Engineer: Benson	
Date: Tuesday, October 13, 2020	Sheet: 89	of: 100	



Main Board



Discharge Discharge



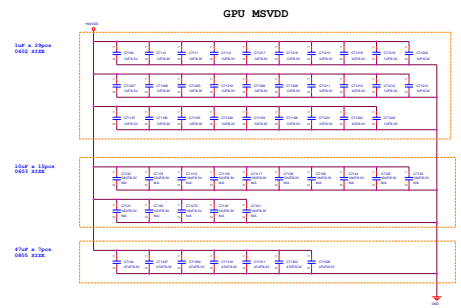
GPU NVVDD

1uF x 49pcs
0402 SIZE

4.7uF x 5pcs
0603 SIZE

10uF x 15pcs
0603 SIZE

47uF x 20pcs
0805 SIZE

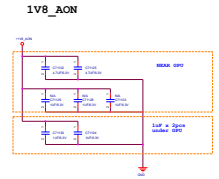


GPU MSVDD

1uF x 29pcs
0402 SIZE

10uF x 15pcs
0603 SIZE

47uF x 7pcs
0805 SIZE



1V8_AON

MEAR GPU

1uF x 2pcs
under GPU

1V8 Power Control

+1V8_AON

TPS54 = 6.6A

uP9530 ILIM/LFM Setting 對應表

ILIM PIN	LIMIT Current
GND	NA
SW to GND	NA
VLDO/VDD	NA

ER unmount

Title: GPU_POWER

Project Name: GA503QS

Engineer: Ashton_yang

Rev	Date	Description
1.0	2020.05.25	P66 reserve R6414/R6646 to P_SIO_OV9
	2020.05.25	P75/P79 combine MOS(Q7801/Q7803)
	2020.05.25	P90 Power schematic add SMD OV9 CIRCUIT
	2020.05.25	P56 R6407/R6417 0603 change to 0402
	2020.05.25	P14 C1401/C1402 R=1.9 change to R=1.5
	2020.05.25	P73 type-c DP2 IPPW change to IPTC
	2020.05.26	P39 CK3901/CK3902 change to 11020-00088100 for Reliability issue
	2020.05.26	P39 remove smart AMP TAS5629BRSMR, using codec internal AMP for tweeter speaker
	2020.05.26	P46/P41 add R88-2230 MUT, R6002/R6102
	2020.05.26	P77 add MEM_VPP 0201 3pcs, +VPWRDG 0201 20pcs
	2020.05.26	P34 R3481/5261 change to 23402/03404-03411 (07024-00820100) L3401-13404 change to 09022-00011600
	2020.05.26	P32 add SMC reference symbol
1.1	2020.05.26	P30 unmount L3501/C3551
	2020.05.26	P31 add level shift I2C3_SDA_TCH_PAD/I2C3_SCL_TCH_PAD
	2020.05.26	P70 mount R7006, unmount R7004
	2020.05.26	P51 add WLAN_PWR_EN schematic
	2020.05.27	P52 remove R5269/R5256/R5246/R5259/R5247/ R5254/R5222/R6319/R6325/R5235/R5217
1.2	2020.05.27	P38 U3402 transformer SWAP(1/4, 2/3)
	2020.05.27	modify RTC Power name(+RTCBAT)
	2020.05.27	R6517/R6521 floating
	2020.05.27	P44 unmount R4002/R4102
	2020.05.27	P36 U3402 transformer SWAP again (1/4, 2/3)
	2020.05.27	P52 SWAP U3801.0 EMI-Protection
2.0	2020.05.27	P47 J47501/J47502 change to TH74 P/N: 12013-00175600
	2020.05.28	P66 add hall sensor small board
	2020.05.28	P52 add L5205/L5208/L5209/L5210
	2020.05.29	P58 @ 增加 100Ω/100MHz@100mA@10 SMC choke: 09B0909C301
	2020.05.29	P32 Remove RL3302,RL3303
	2020.06.01	P14 change to R=1.9 PCIE15_TXN_C0_R 1> PCIE6_TXN_C0_R1 PCIE15_TXP_C0_R 1> PCIE6_TXP_C0_R1 PCIE15_RXN_C0_R 1> PCIE6_RXN_C0_R1 PCIE15_RXP_C0_R 1> PCIE6_RXP_C0_R1
	2020.05.29	P66 add Port B Dual M.2(E)
	2020.05.29	P77 add7605/add7207/add7208/add7108 CHANGE TO hv1.5
	2020.05.29	P23 modify keyboard backlight pin define
	2020.06.01	P66 add R6601
	2020.06.01	P66 remove L6502
	2020.06.01	P26 remove R3619/R3612/R3602/R3620/R3608 2020.06.01 P26 change J3902 pin define
	2020.06.01	P7 SH7065_CR_WAKEZ change to GPIO3
	2020.06.01	P7 add SIGNM_EN12 to SH7065, add R6731/R6748
	2020.06.01	P37 S3701/C3706/C3707/D3703/D3702/D3704 change to GND_AUDIO
	2020.06.01	P46 C6608/C6609/c6611/c6616 change to 0201 del R6624 R4401/C6701,C6407 change to 0402
	2020.06.01	P46 R6619/R6603/R6609/R6621/R6626/R6625 R6623/R6622/R6618/R6640 change to 0201
	2020.06.01	P46 C6610/C6606 0603_10uF change to 0402_4.7uF
	2020.06.01	P66 EMI change to small package
	2020.06.02	P36 del c3404/c3405
	2020.06.02	P31 TP COMM change pin define
	2020.06.02	P35 c3913 change to 15k ohm
	2020.06.02	P56 J5603 pin10 change pull high power +3VA
	2020.06.02	P37 modify audio jack p/n:12016-00969700
	2020.06.02	P66 modify J6301 hall sensor pin define
	2020.06.03	P66 modify J5403 pin define
	2020.06.03	P66 HDMI EMI SWAP
	2020.06.03	P36 add OF_HDF schematic
	2020.06.03	P37 +12VS_AUDIO, +12VSUS change to +12V8
	2020.06.03	P21 del S3303/R3079(LAN_RSTF_EC)
	2020.06.04	P31 del C3550/C3551
	2020.06.04	P35301 change ARSOURCE COMM p/n: 12003-00076000
	2020.06.04	P7 add (c77854~c77866) (c77867~c77876)
	2020.06.04	P7 ac7106-ac7108 change P/N: 11020-00738000
	2020.06.04	P66 modify set name A/D_MIX_POWER change to AD_MIX_POWER
	2020.06.04	P77 del (c77857~c77866) (c77867~c77876)
	2020.06.04	P77 del c77857/c77856
	2020.06.04	P32/P53 add MS schematic
	2020.06.04	P33 modify keyboard back light pin define
	2020.06.04	P34 03402/03404-03411 change to 07024-01480000 L3401-13404 change to P/N: 09B0929090100
	2020.06.05	P46 L6801/L6803/L6805/L6807 change small package: 0909R0909301
	2020.06.05	P46 L4719 RM4712 SMAP/RM5403 L5401 SMAP/RM4709 L4704
	2020.06.05	P35 unmount pogo45 all sed
	2020.06.05	P46/P68 swap RM5403/RM4712/RM4709/RM6802 RM6803/RM6804/RM6805/L6807
	2020.06.05	P7 mount c0701, R0741 change to 10k ohm(AMD review)
	2020.06.05	P8 mount C0802, unmount R0822 (AMD review)
	2020.06.05	P10 C1071 change to 0.22uF (AMD review)
	2020.06.05	P22 add R3302/R3303 Ohm (AMD review)
	2020.06.05	P22 add R4210/R4211 Ohm (AMD review)
	2020.06.05	P62 U6203 change P/N: 1TH237(06037-00350100)?
	2020.06.05	P36 C3609 change to 4.7uF
	2020.06.05	P38 unmount R3604, AC3_RST2_AUD delay schematic
	2020.06.08	P46 del c6606/c6610, c6601/c6607 change to 0603
	2020.06.08	P7/P42 change GPIO3_CR_WAKEZ# net name
	2020.06.08	P23 03402/03404-03411 change to 07024-01480000
	2020.06.08	P34 L3401-13404 change to P/N:09B0929090100
	2020.06.08	P34 L3401-13404 change to P/N:09022-00011600
	2020.06.08	P56 J5603 modify pin define, unmount R5432
	2020.06.08	P42 unmount R4205
	2020.06.08	P47 del R4749/R4786, add R14701/R14702
	2020.06.09	P66 add 03901-05905
	2020.06.09	P66 SMAP W09301
	2020.06.09	P7 remove T4701~T4704
	2020.06.09	P31 add LID_EN# echo

Rev	Date	Description
	2020.06.09	P56 del 05903~05905
	2020.06.10	P46 DELL b4102
	2020.06.11	P77 DELL Q7702/R7702/R7703/R7707/R7708 R7710/R7711/R7704/R7705
	2020.06.11	P62 J6202 change P/N: 12012-00022800
	2020.06.11	P47 R4733,R4731,R4745,R4746 change P/N: 10101-02241000
	2020.06.11	P7 add c77857 to +PWYDCQ
R1.1	2020.06.15	1.Based on GA503QR_R101 to modify R1.1 version 2.Update Power schematic GA503_SH3_PWR_DMOS_M_0413A for SM20
	2020.06.16	3.P71,P77, follow GU503 change decoupling cap to meet SM20 reference schematic
	2020.06.16R	4.P70, Change power rail decoupling cap size(follow CRB) 5.P1~P65, follow GA503QR_R102 update ROM
	2020.06.17	6.P71, Connect PINK_SRC power rail to 1V8_ACM directly (follow HY PWR suggestion) 7.P49, Change HDMI common choke footprint to meet R1.0 version PCB
	2020.06.18	8.P71, Change 1V8_ACM power soultion to 06014-02340000 9.P78, unmount Q7810, R7814, R7857 10.P78, follow design guide and check list unmount R7813, mount R7809 11.P78, follow design guide GPIO2 unused in GM20, remove R7854, R7801, R7753 12.P78, Add R7841 for GPIO3 pull down 10k ohm follow GM20 design guide 13.P73~P76, R7305L, R7405L, R7505L, R7605L follow reference schematic pull down 1k ohm 14.P78, reserved R7853 for GPIO13 PU 1V8_ACM (follow DG) 15.P78, reserved R7854 for GPIO16 PD(follow DG) 16.P78, reserved R7856 for GPIO16 PD(follow DG) 17.P70,P71, P77 change decoupling capacitor footprint to 8X 18.P70, Add VGS off para for PG VGS sense pin(PG_VSCEVCC_PG_S) 19.P73~P76, Add R73006, R74015, R75010, R76010(Follow CRB) 20.P78, delete Q7810, R7814, R7857 (follow gu603) 21.P78, change Q7811(SOD05 pin 2) to GPIO6 (follow VC GA401QM) 22.P30, remove NVDD_SMB_EN1 off page and R3071(power request) 23.update power schematicSA503_SH3_PWR_DMOS_0418C for DeMOS 24.P70, remove R7046, G7005 to meet power requirement
	2020.06.19	25.P72, remove R7248, R7249, R7250, R7251, R7252, R7253, R7255, R7256 , follow CRB and compatible design. 26.P71, Change R7151 footprint to 8X 27.P71, Add R7153, R7154(C check list) (P70 check list) 28.P79, Remove R7824, R7830, R7843, C7805, C7810(follow CRB) 29.P78, C7804, C7802, C7807, C7808, C7806 change footprint to 8X (follow CRB) 30.P79, follow CRB to change capsitor size and location 31.P50, Change J5004, J5005 to 12017-00380100 32.P47, mount R4743, R4745, unmount R4742, R4744 to change U4704 address 33.P71, remove unused Q7152, R7107, R7112 34.update power schematicSA503_SH3_PWR_DMOS_0419C
	2020.06.19C	35.P3, change C3303, C3304 to 0.1uF(follow AMD DG support PCIE gen2)
	2020.06.19D	36.update power schematicSA503_SH3_PWR_DMOS_0419D
	2020.06.19E	37.P78, Change RM7903 from 2.2k ohm to 4.7k ohm(follow CRB)
	2020.06.22A	38.P70~P79, Change power enable GPU_PWR_EN to 1V8_ACM_EN 39.P73~P76, follow GU603 part reference for compact design
	2020.06.22B	40.P72, Add VCC Battery circuit D5982 M3923 M390 for Without RTC Can't boot issue
	2020.06.22C	41.update power schematicSA503_SH3_PWR_DMOS_0422A 42.update power schematicSA503_SH3_PWR_DMOS_0422B
	2020.06.22D	43.P79, follow GU603 part reference for compact design 44.P77, change C77002, C77189, C77214 footprint from 0603 to 0402(MB) for layout placement 45.P73~P76, follow CRB,remove C73001, C73002, C7401, C74003, C7501, C75003, C7601, C76003 46.P50, Add M50021, M50031, M50038, M5004 for AMD ST72.0 47.P78, change V7810, V7815, V7817, V7824, V7826, V7829, V7830, V7831, V7832, V7833, V7834, V7835, V7836 footprint from TPCP8 to TPCl2Z for layout placement 48.P78, remove V7837 for layout placement 49.P34,P53, update GA503QR_R1 20200622_RF schematic for RF requirement 50.P50, correct SMBus net name for thermal sensor 51.P71, change R7151, R7108, R7109, R7110 footprint to 8X for compact design(follow GU603)
	2020.06.23A	52.P77, Change C77115 footprint from 0603 to 0402 for layout placement
	2020.06.23B	53.P77, Change CK7703, CK7704, CK7705, CK7706, CK7707, CK7708, CK7709 , CK7710 from 11020-01000600(7643) to 11020-00738000(3908) for layout placement
	2020.06.23C	54.P72 Remove R7201, change C7206 footprint from 0805 to 0603 for layout placement
	2020.06.23D	55.P70, P79, P79, change C7002, C7012, C7101 C7018, C7135, C7136, C7501 , C7503, C7504, C7511, C7512, C7513, C7514, L7201,L7202 , C7123 , C7125 to 11020334701520(11d2233247520)(11d2233247520)(無此物料)
		56.P70,follow CRB remove C7045
		57.P70, remove R7009 for layout placement and routing(not follow CRB)
	2020.06.23E	58.P78, change T7818, T7819, T7820, T7821, T7822, T7823 footprint from TPCP8 to TPCl2Z
	2020.06.23F	59.P46, Add R6624, D6601, remove R6613 for PD charger lost issue (follow GU603)
	2020.06.23G	60.P71, Connect NVDD to NVVDD, PEX_VDD power rail
	2020.06.29A	61.P70, change Q7009A gate set to DSPD_PMEM# (follow HY PWR suggestion) 62.P78, Add R7802, R7814 to reversered I2C3 mosfet gate control for DSPD_PMEM(Follow HY PWR suggestion) 63.P45, update zone hold
	2020.06.29B	64.P78, remove T7822, T7823 for layout power plane routing 65.P71, change NVDD to NC for layout routing 66.update power schematicSA503_SH3_PWR_DMOS_0429A
	2020.06.29C	67.update power schematicSA503_SH3_PWR_DMOS_0429B
	2020.06.29D	68.P71, change PEX_VDD dummy ball to NC for layout routing
	2020.06.29E	69.P16, remove net name MA_VREFCA

Rev	Date	Description
	2020.06.30A	70.Change R6523, R6524 to meet DSP
	2020.06.30B	71.update power schematicSA503_SH3_PWR_DMOS_0430A
	2020.06.30C	72.P65, update screw hold 73.update power schematicSA503_SH3_PWR_DMOS_0430C
	2020.06.30D	74.Change U3503 to ITE8258E-248A/CE (G4037-00430000)
		75.P65, update screw hold GA503QR_R104_HOLE_UPDATE_20200430D1
		76.P65, Change R6529 to CR4094R
		77.P46, Add T6602 for test
		78.update power schematicSA503_SH3_PWR_DMOS_0430D
	2020.06.30E	79.P46, remove T6601, change T6602 to 5pc12t
	2020.06.30F	80.P45, remove R6503 SMD
	2020.07.02A	81.update power schematicSA503_SH3_PWR_DMOS_0430D_ROM_R
	2020.07.03A	82.P52, Mount R5212, R5207, R5228, R5252 , unmount R5223, R5215, R5253, change R5257 to 0 ohm for VR 2 phase tuning
	2020.07.08A	83.P46, Change R6421, R6424 from 2.2k to 4.7k for I2C fixture programing
	2020.07.10A	84.P39, unmount CK3901 (follow design IP)
	2020.07.10B	85.P46, Change Q6406, Q6407 to QM3129M3 (07005-A1110000)
	2020.07.13A	86.P88, update power schematicSA503_SH3_PWR_DMOS_0430D_ROM_R_0713A_EX
	2020.07.14A	87.P92, update power schematicSA503_SH3_PWR_DMOS_0430D_ROM_R_0714A_EX
R1.2	2020.07.14A	88.P46, add PS_ON_PD_R connect to GPIO8 and mount Q6408, R6458, R6413 89.P57, Remove +3VA_EC discharger circuit(Q5767, R5721, R5722) 90.P32, Modify PS_ON net name to PS_ON_L#
		91.P42, update design IP schematicSTS5_20200701 change R6214 PU power to +3VS_CR_ASW, change C6237 from 0.1uF to 1uF
		92.P45, Change eDP pin define(follow Design IP) 93.P30, Remove R3078, R3077, G3007, add R3071 and change PM_PWRBTN# to GPIO (follow VC GA401QM)
		94.P30, Add off page for PG ESM6 (follow VC GA401QM) 95.P30, Change 1.8VSUS_CR to GPIO3(follow VC GA401QM)
		96.P30, Change ADP_INSERT_N#8 to GPIO1(follow VC GA401QM) 97.P30, Change GPIO1(SOD05 pin 2) to GPIO6 (follow VC GA401QM)
		98.P30, Remove R3004, add T3008 (follow VC GA401QM)
		99.P30, Change AMP_SLEEP# from GPA7 to GPP5, add T3009, R3004(follow VC GA401QM)
		100.P71, unmount T7102, R7149, C71266, R7152 for FUSE_ESC connect 1V8_AON directly
		101.P53, Change M5301 from 11020-01179900 to 11020-00570100(follow component list G707)
		102.P30, remove R3073, add T5010 for reserved
	2020.07.17A	103.P91,92,98, Update Power Schematic GA503_SH4_PWR_DMOS_0716B
	2020.07.17B	104.P56 Follow Connect list G707 Add R6530/R6531
		105.P53 Remove NET LAN_PWR_EN, Add P30 T3011
		106.P53 Unmount R5303/C5315/R5307/R5306/Q5304/C5314 Remove AOConnect function
		107.P4 Remove NET Connect JO602 and Circuit P44 Add JSHSRD4603 FPC Connect For KDI + UART Debug
	2020.07.17B	108.P4 Unmount R7614
		109.Update Power Schematic GA503_SH4_PWR_DMOS_0717B
	2020.07.20A	110.Update Power Schematic GA503_SH4_PWR_DMOS_0720A
	2020.07.20B	111.Update Power Schematic (Design IP Update)GA503_SH4_PWR_DMOS_0720B
	2020.07.24	112.Update Power Schematic (Design IP Update)GA503_SH4_PWR_DMOS_0721A 113.P42, Follow design ip G29755 schematic R1.7, Remove R4215 Add C4202 ,M4205
		114.P66, Remove D6601, R6624, C6625, connect PLTF_PG1 to GPIO3, PLTF_PG2 to GPIO7, (follow TI FAE suggestion) P66,P67, Remove R6789,R6793 and unused GPIO PA_MIX_I2SSA_EN, PA_MIX_I2SSA_EN for optimized schematic
	2020.07.27A	115.P59, Add VCC Battery circuit D5982 M3923 M390 for Without RTC Can't boot issue 116.P09, P13,P14 Update DDR4 SPEC from Memory Down s8 Change to DDR4 *16
	2020.07.27B	117.P78 Modify M7834 Optional from /VRAM to N/A
		118.P14 M1409/R1410/R1411/R1412 /U1402/U1403/U1404/U1405 Optional Change to /RAM
		119.P14 Remove DIM Thermal Sensor Circuit U1401/U1402/U1403/U1410
	2020.07.29C	120.P14 Follow GA503QR R1.1 Modify DDR4 Cap Number 121.P9 P42 Updated GL9755 Schematic R1.8_Add GPIO221_80_EOTF
		122.P14 Update Memory Design ip V728 .Modify MLCC Follow AMD SPEC 123.Update Power Schematic GA503_SH4_PWR_DMOS_0729A
	2020.07.31A	124. P34 DDR4 Unmount U3402 Dp SWAP 125. P14 Update DDR4 U1402/U1403/U1404/U1405 DDP Symbol
		126. P78 Rename R7871 PG 1V8ON for PG
		127. P14 Update Memory Design IP V730 .Add R1603 R1604 R1605 .Modify DDR Footprint
	2020.07.31B	128. Update Power Schematic (Design IP Update) GA503_SH4_PWR_DMOS_0732A
	2020.07.31C	129. P30 Follow EC Pulsigink V1.4 .Modify AMP_SLEEP# from GPP5 to GPJ4 P7.Remove GPIO23 AC_PRESENT #C Change Test Point
	2020.08.03A	130. P78 HV Suggest GPIO24 change to 10K PD, Unmount R7853, Mount R7871
		131. P4 M_A_ALERT# SO403 follow AMD Review check PU 1K to 1.2V
		132. P48, HDMI Protocol 2.0 fail Modify R4847/R4848 to 3.3K Ohm
	2020.08.04A	133. P42 +3VS_CR_AUX Power Source Change +3VS to +3V8ON for AMD S0i3
		134. Update Power Schematic (PWVDDQ Modify) GA503_SH4_PWR_DMOS_0804C
	2020.08.04B	135. P78, Follow HY CRT .R7838 Modify to 0 Ohm 136. P70. Remove R7011 Avoid Power on sequence leakage issue
R1.3	2020.08.10A	137. P46, add Q6409 for PD load code on dead battery mode
	2020.08.10B	138. P45, Change R4502, R4503, R4516 PU power to +3VS for eDP sequence 139. Update power schematic GA503_SH_PWR_DMOS_0810A
	2020.08.10C	140. P28, add Q2801 for slave charger dead battery mode
	2020.08.11A	141.P45, Change R4503, R4516 pin2 power to +3V8_LCD for eDP sequence 142.P45, Change R4503 from 100k to 4.7k(follow AMD CRB) 143.P45, Mount R4507 for eDP power sequence 144.P70, Reserved R7009, R7012, R7014, R7017, remove T7003, T7004 for next generation CPLD co-lay(SPS sequence)
	2020.08.11B	145.P46, correct Q6409 gate's control power to +3V8ON

Rev	Date	Description
	2020.09.13A	146.P46, Change debug connector part reference to JDEBUG1, JDEBUG2, JDEBUG3 147.P7, P8, remove R0730, R0745, add R0826, R0825, change DP1_HPD_sources# and DP2_HPD_sources# from ASPD2 01 to ASPD2 21 for ME issue (ASPD's power domain should be S5, follow VC GA401QM)
		148.P7, P8, P78,merge DP1_HPD_sources# and DP2_HPD_sources# to DP_HPD_sources#
		149.P7, P8, add R7742 and change ED_RST to ASPD111 follow VC GA401QM
		150.P7, reserved T0709
		151.P7, Change EDP_CSB to ASPD1901(follow VC GA401QM)
	2020.09.13B	152.P42, Follow Genesys Datasheet is S013 . Change +3V8 to +3V8ON For AMD S0i3 Sequence Request 153.P42, Change R3 Cold to 03 Not .Unmount R4208/R4201/R4202/C4202/R4207/C4203 add R4230 short to +3V8ON
		154.P42, Unmount C4203 add R4216 for Genesys S013 Power Sequence. SD Reset should be keep high
		155.P70, change PWRDDQ_PWRGD to G7002 pin 1 for GPU power sequence
		156.P71, Change Q7106R for PEX_VDD discharge path to meet GPU power off sequence
		157.P71, Change R7113, R7118, R7115 to 10 ohm for GPU power off sequence
	2020.09.13C	158.P46, remove R6414, R6646, R6650, R6649 (follow Fwr SD suggestion)
		159. Update power schematic GA503_SH_PWR_DMOS_0813A
	2020.09.17A	160.P70, Change C7005, C7008, C7014 footprint to 0603 for layout placement
		161. Update power schematic GA503_SH_PWR_DMOS_0817A
	2020.09.18A	162.P50, reserved resistor R5023, R5024, R5025, R5026, R5027, R5028, R5029 for modern standby
	2020.09.18B	163.P50, Change U5001-U5004 alert pin PU power plane for +3V8 and +3V8ICH co-lay
	2020.09.18C	164.P70, corrected PU twice _mount M7017, unmount M7013
		165. Update power schematic GA503_SH_PWR_DMOS_0818A
	2020.09.19A	166. Update power schematic GA503QR_R13_20200819A
	2020.09.19B	167. Update power schematic GA503_SH_PWR_DMOS_0819B
	2020.09.24A	168.P70 unmount M7011, M7003, G7002, G7001, M7007, C7026, M7015, mount M7009, M7012, M7013, M7010 for SMSC CPLD 169.P36, Change H13602, H13603, H13604, H13605 optional to @ 170.P48, mount U4803, U4804, RM4802, unmount L26801 for HDMI electrical tuning 171.P78, unmount M7870 for unused GPU's GPIO(follow HV check list)
	2020.09.25A	172.P70, Change G7002 part number to 04004-01650200
	2020.09.25B	173.P48, Change L26801 part number to 0909G0906400
		174.P48, unmount L26802, L26803, L26805, mount RM4803, RM4804, RM4805
	2020.09.27A	175.P48, mount L26802, L26803, L26805, unmount RM4803, RM4804, RM4805 176.P48, Change L26802, L26803, L26805 part number to 0909G0906400 for electrical tuning 177.P36, Change L3602, L3603, L3604, L3605 part number to 09002-00130300 (暫時) 178. Update power schematic GA503_SH_PWR_DMOS_0824A P48P60 change from 127k to 130k
	2020.09.27B	179.P70, change G7002 part for GM20
	2020.09.31A	180.P65, Change R6520, R6522 optional from @ to N/A
A2.0	2020.09.23A	181.P30, add R3063 for PS_ON_R on dead barrey mode 182.P46, add R6414, R6424 for Mux redriver I2C PU 183.P39, Change CK3901 part number to 11020-00084000(2.1 mm) 184.P65, Change R6520, R6522 footprint for MOT(follow GA503QE G917A) 185.P68, unmount R6803, R6804 for HDMI TDR 186.P71, Change R7104 from 60.2 ohm(0603) to 15 ohm(0603) ,(follow SC313_GPU_SNUBOK_R1.20) 187.P28, Change SPI ROM LDO power to page 29, and change U2801 Vin to +3V8ST/+3VA for type-C dead battery mode 188.P46, add R6646 for PS_ON_PU default value on dead battery mode 189. Update power schematic GA503_SH_PWR_DMOS_0922A 190.P9, unmount R0905 for optimized schematic 191.P7, reserved R0730 for touchpad int pin to avoid leakage(follow GA401QM R11 G925) 192.P7, Change DIMM_SB12 pull up power to 3V8 prevent leakage (follow GA401 M8 0916)
	2020.09.29A	193.P48, Change L26801, L26802, L26803, L26805 footprint for HDMI electrical
	2020.10.06A	194.P42, Change R4220, R4221, R4223, R4224, R4225, R4226, R4227 from 22 ohm to 0 ohm for compatibility issue 195.P46, Add R6649, R6650 for RCM less on dead battery mode behavior
	2020.10.07A	196.P31, P35, Add I2ose RCM ES co-lay schematic
	2020.10.07B	197.P57, modify Q5752 Pin3 +3V8ST to 1.8VST0 discharge schematic (follow GA401QM ESD_R12_1007)
		198.P56, mount C5623 for HMI ESD request
		199.P56 Change D5622 to 07024-00640000 for HMI ESD request
	2020.10.08A	200.P46, Add Q6410, R6446, R6450, R6458, R6460 for dead battery mode behavior
		201.P79, Add C7814, R7880, R7881 for GPU I2C level shift
	2020.10.12A	202.P79, unmount C7814, R7880, R7881 for reserved
	2020.10.12B	203.P29, reserved R2811, R2812 for SPI ROM power optimized
		203.P31, mount C3114, C3115, C3117, C3118 for EMI request
	2020.10.13A	204. Update power schematic GA503_SH_PWR_DMOS_1013A 1.RS480P = 16.5K => 17.8K 2.3528 CAP change footprint to sza_002x (PC8R401 / PC8Y301 / PC8X002 / PC8Y602 / PC8Y701)
	2020.10.13A	205.P52, remove C5209, C5210, add C52213, C5208, C52210, C5203 for noise

EE PART

GA503QS

			CPU	Power	DIMM	VRAM			
Option	PCB	SKU							

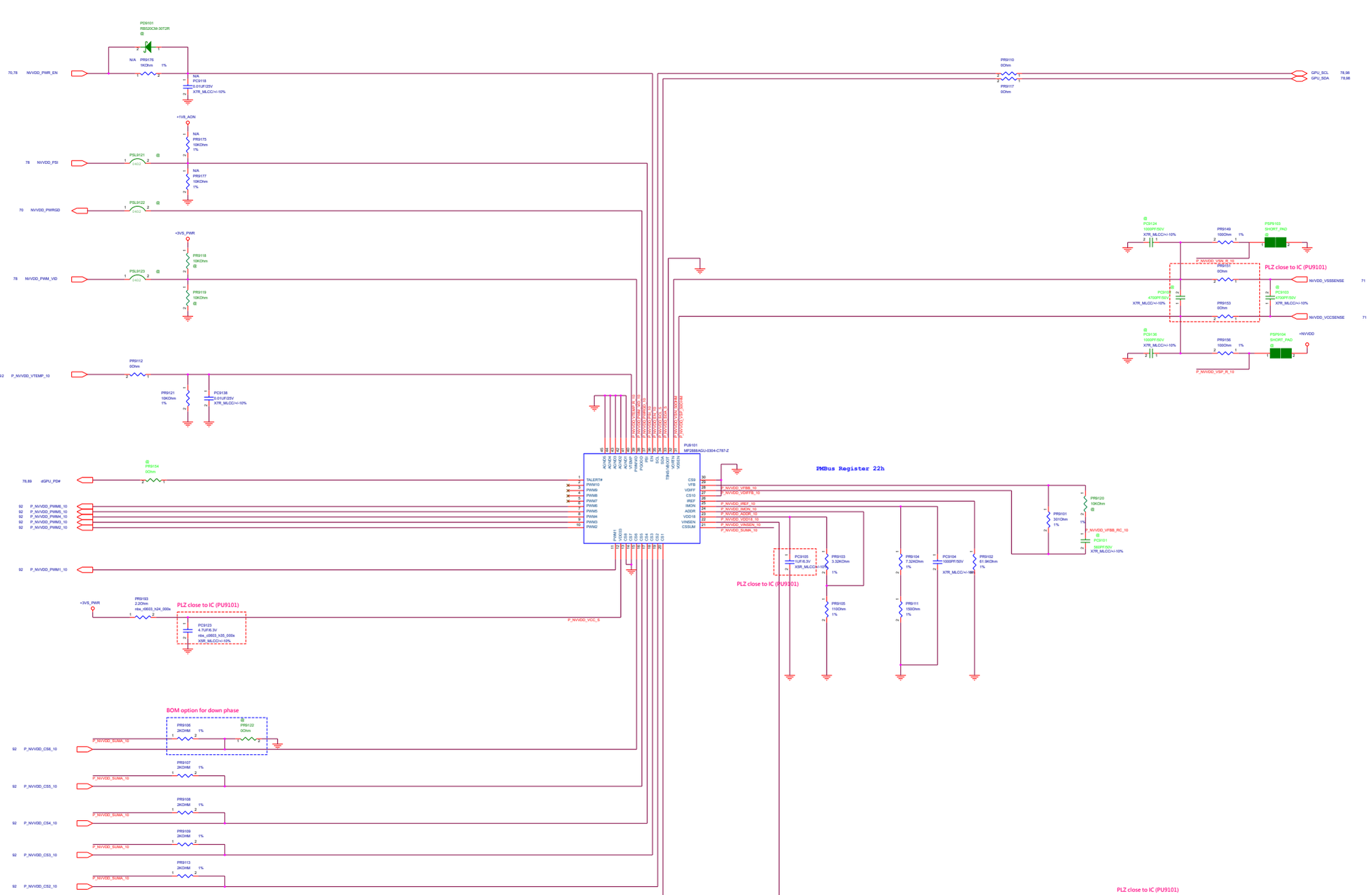
9. Card Reader: AU6435--02G630002400 (Page42)

10. USB Charger IC: (Page52) Silego SLG55584AVTR -- 06016-00040000
MAXIM MAX14566AEETA+ -- 06G016196011

11. USB3.0 Repeater IC:(Page67)
Parade : PS8710B -- 06053-00200000
Maxim : MAX14972CTG+ -- 06053-00030000

13. Audio Codec : 02043-00130000 (663-VA4)

+NVVDD [For DGPU]



< SW Auto-Phase setting > TBD...SR4
PWM2 : APL_Hys = 16A
PWM3 : VAPL1 = 17A (1 Phase)
PWM4 : VAPL2 = 34A (2 Phase)
PWM5 : VAPL3 = 68A (4 Phase)
PWM6 : VAPL4 = 102A(6 Phase)

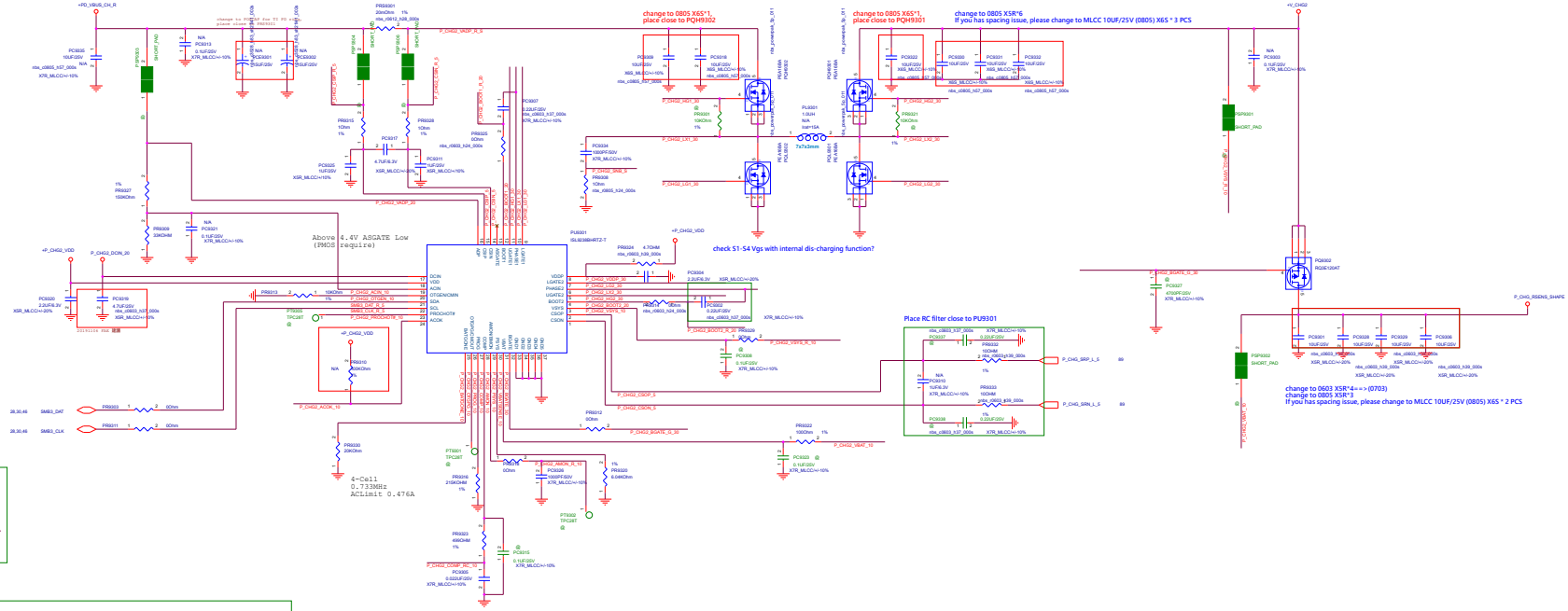
< HW Strap Function setting >.....SR3
PWM2 : APL_Hys = 13.1A
PWM3 : VAPL1 = 16.4A (1 Phase)
PWM4 : VAPL2 = 32.8A (2 Phase)
PWM5 : VAPL3 = 65.7A (4 Phase)

<Variant Name>

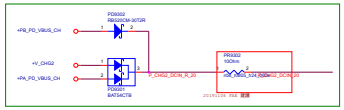
ASUS	Project Name: GU603H/GX703H		Rev: R1.0
Title : PW_+NVVDD (1)			
Size: Custom	Dept.: NB Power team	Engineer: Power	
Date: Tuesday, October 13, 2020	Sheet: 91 of 104		

Charger ISL9238 (NVDC)

	65W	100W
PL9301	INDUCTOR 1.0UH/11A 20% 09016-00012800	INDUCTOR 1.0UH/15A 20% 09016-00012600
PCE9302	@	N/A

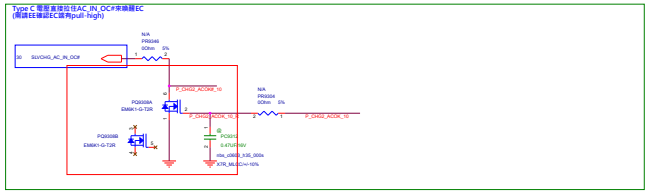


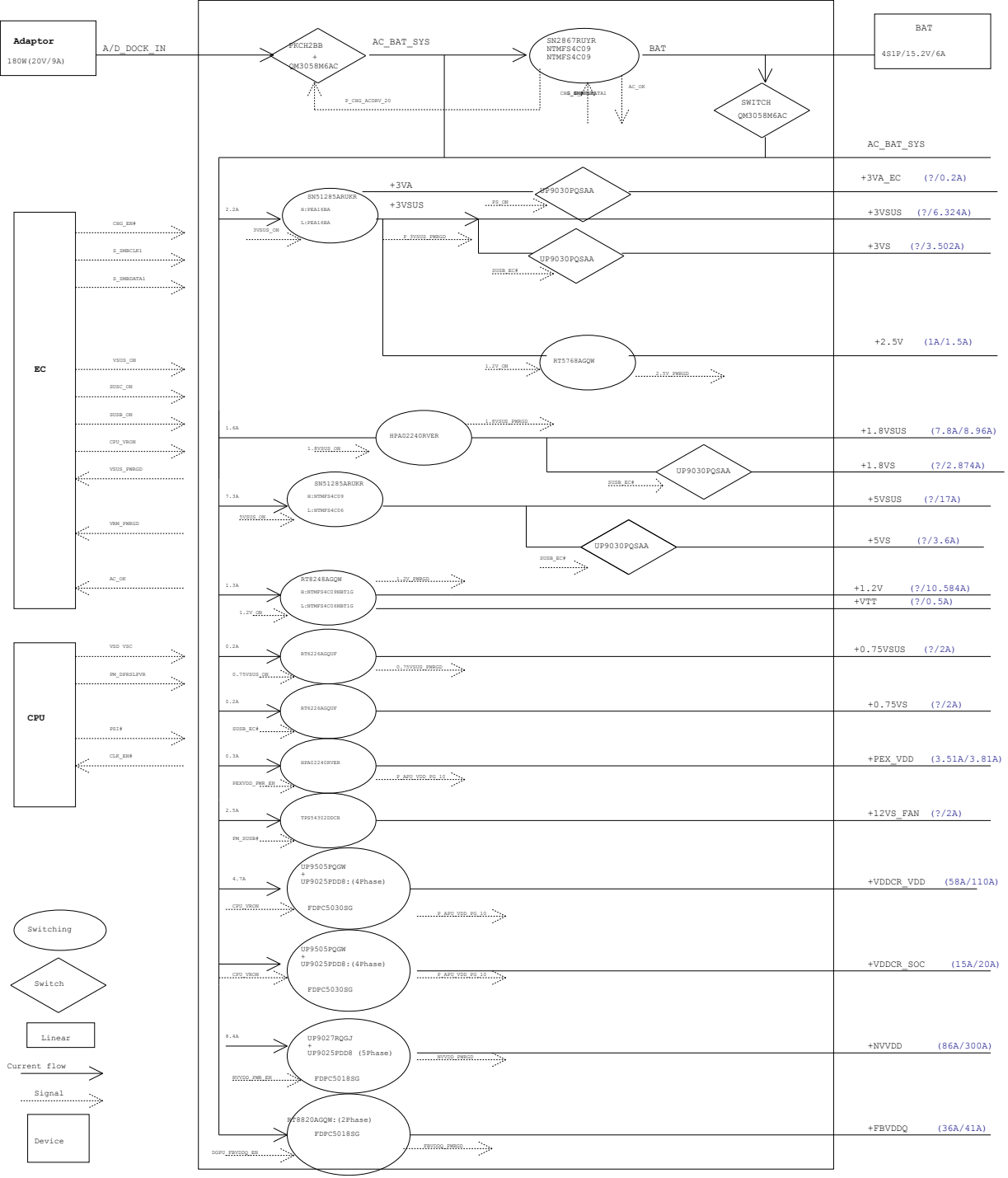
Check operating current(light /havey load-->15mA)

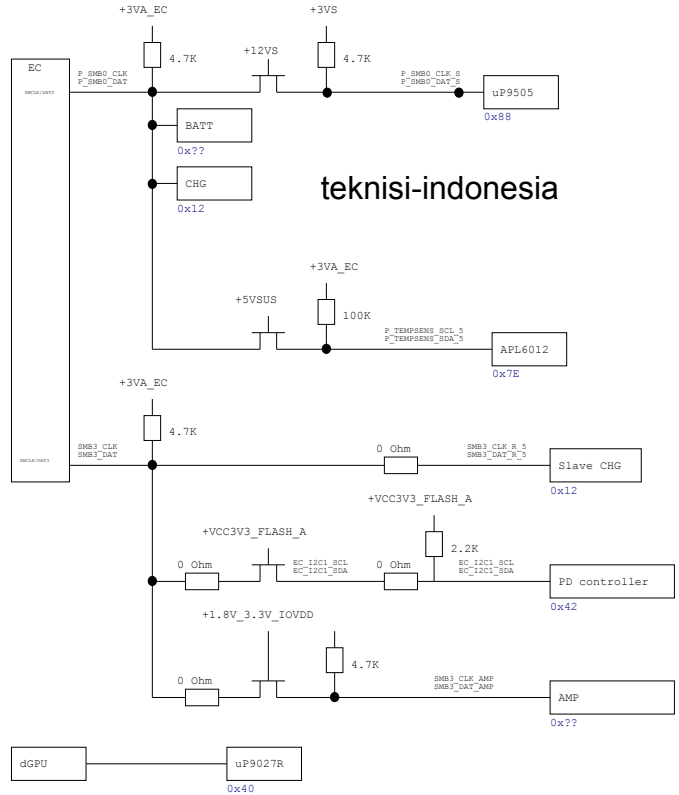


For power state S5, wake-up EC by PD plug-in AC_IN_OC#

Type C 電源直接拉往AC_IN_OC#來喚醒EC
(兩顆EE確認EC腳有pull-high)







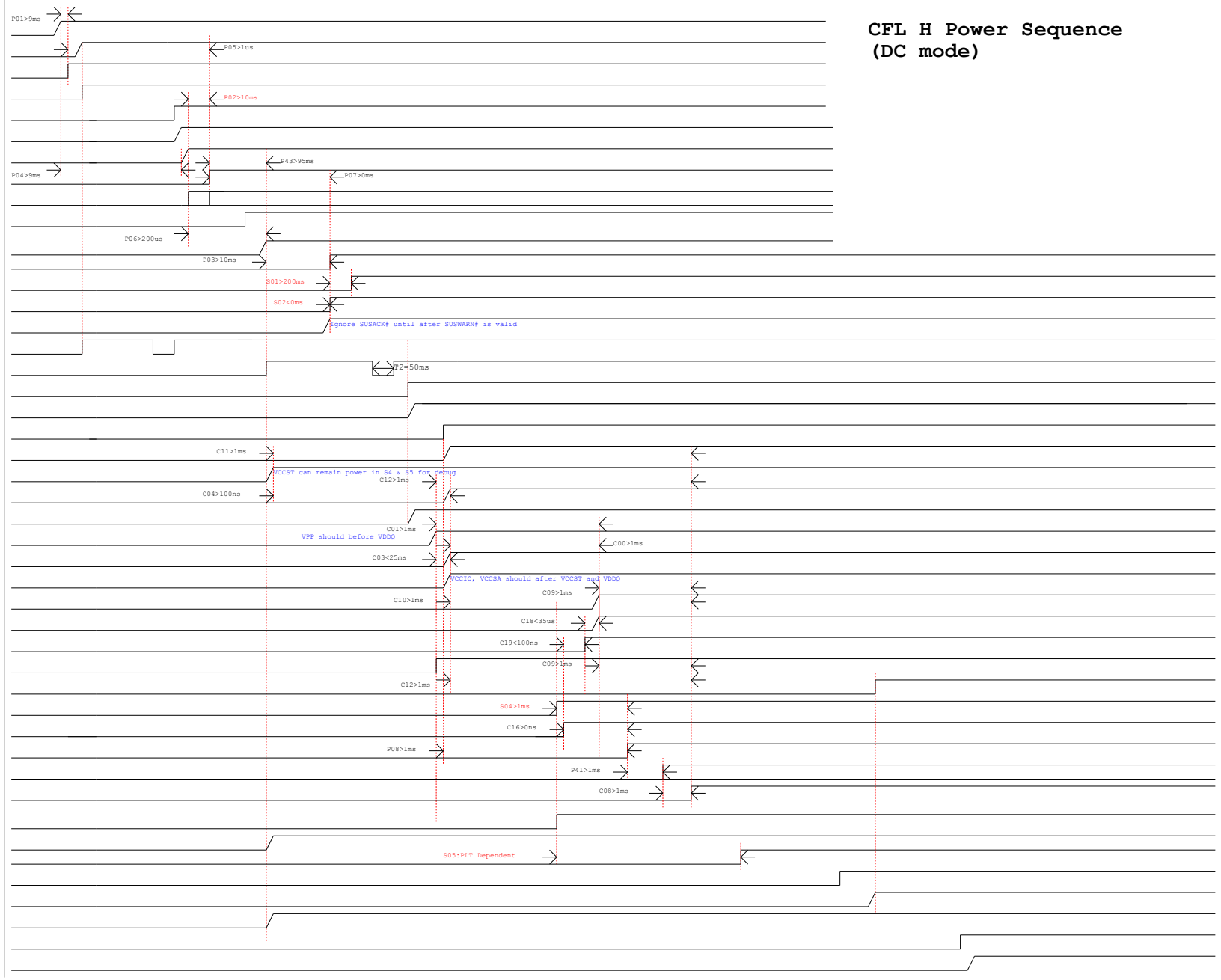
<Variant Name>
Project Name: GA503QS
Rev: R1.0
Title : PW_FLOWCHART
Size: Custom
Dept.: NB Power team
Engineer: CS Lin
Date: Tuesday, October 13, 2020
Sheet 99 of 104

CFL H Power Sequence (DC mode)

DC-IN Mode

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#) +12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#) +12VS/+5VS/+3VS
(VSUS_ON) +1.0V_VCCST,VCCPLL (VCCST_PWRGD)
(+VCCIO) +VCCSTG
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
(+12VS) +VCCPLL_OC
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL) +0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT



ASUS	Project Name: GA503QS		Rev: 1.0
Title : Power On Timing-DC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: NB1 RD2 EE1	
Date: Tuesday, October 13, 2020	Sheet 101 of 104		

9. Card Reader: AU6435--02G630002400 (Page42)

10. USB Charger IC: (Page52) Silego SLG55584AVTR -- 06016-00040000
MAXIM MAX14566AEETA+ -- 06G016196011

11. USB3.0 Repeater IC:(Page67)
Parade : PS8710B -- 06053-00200000
Maxim : MAX14972CTG+ -- 06053-00030000

13. Audio Codec : 02043-00130000 (663-VA4)