Lenovo M90a/M838z Schematic Rev:1.0

Model Name:IQ470SV

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TITLE: M90a/M838z INDEX

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Block Diagram - M90a/M838z

M90a/M838z : 23.8"

M90a: 17AA/3193
M838z: 17AA/3179

For GPU Sku M=0 M=1

GDDR5 CHA 8Gb(256MX32)

GDDR5 CHA 8Gb(256MX32)

*Samsung K4G80325FC-HC25
*Micron MT51J256M32HF-80 :B

DQ 0~31 1500MHZ

DQ 32~64 1500MHZ

AMD GPU GB2b-64
R19M-M25-50
(25W)

PCI Express 3.0 X8

Intel
CML-S 10+2 Processor
65W
TDP: 65w 6+2(8+2 and 10+2 suppor by SW setting)
LGA1200

VCCCORE — IMVP8 4 Phase
VCCGTS — IMVP8 1 Phase
VCCSA — 1 Phase

LVDS CONN — RTD2136N-CG — eDP

DP CONN (colay HDMI) — DDI3

DDR4 2400/2666 — CHA SO-DIMM

DDR4 2400/2666 — CHB SO-DIMM

DMI X4(Gen 3)

Intel 400
CML-S
PCH
Q470 for M90a, H470 for M838z
TDP<= 6W

P21~24:x4
P17~20:x4
P7:x1

Voltage: V3.3A,V1.0A,VCCDSW_3p3
Clock: 32.768K/14/33/48/96/100MHz

*68-455123-01 -INTEL Q470_QS PCH for M90A QU1Y
*68-455122-01 -INTELH470_QS PCH for M838Z QRL9

SATA HDD*1 — SATA3.0

SATA ODD*1 — SATA3.0

M.2 Socket1 -RST Slot M KEY — PCIE

*UMA SKU
M.2 Socket2 Slot M KEY(RESERVE) — PCIE

M.2 Socket Slot E KEY — CNVi / PCIE / USB2.0 P14

P2:G2 only For M90a

USB3.1 Gen2 — SIDE USB CONN P1~P2

USB3.1 Gen1 — SIDE USB TYPE-C(P3)

USB3.1 Gen1 — Rear USB CONN*2Ports(P4~P5)

USB3.1 Gen1 — Rear USB CONN*2Ports(P6~P7)

RGBIR only for M90a

USB2.0 P8 — Web Camera+RGBIR

USB2.0 P9 — Multi-Touch Connector For M90a

USB2.0 P10 — RTS5170-GR | Card Reader

SPI — SPI Flash ROM
32M+16M(M90a)
16M+8M(M838z)

SPI — TPM

*M90a SKU

HDA — Audio Codec ALC233-VB2-CG

eSPI — IT8638E_BX eSIO

EP BTN HD For M90a

COM HD*1(Rear)

FAN Header*1

SPI(1MB)*1

PCI Express 2.0

Intel JACKSONVILLE(M90a)
REALTEK RTL8111K
(M838z)

RJ45 CONN *1

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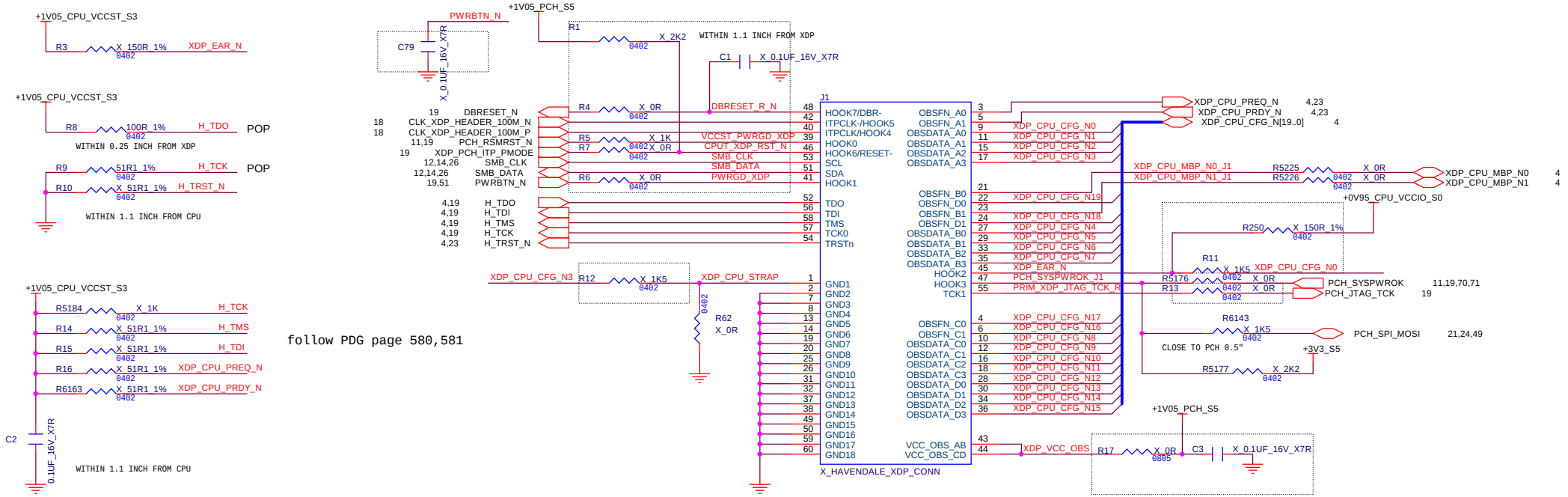
CPU DEBUG CONN



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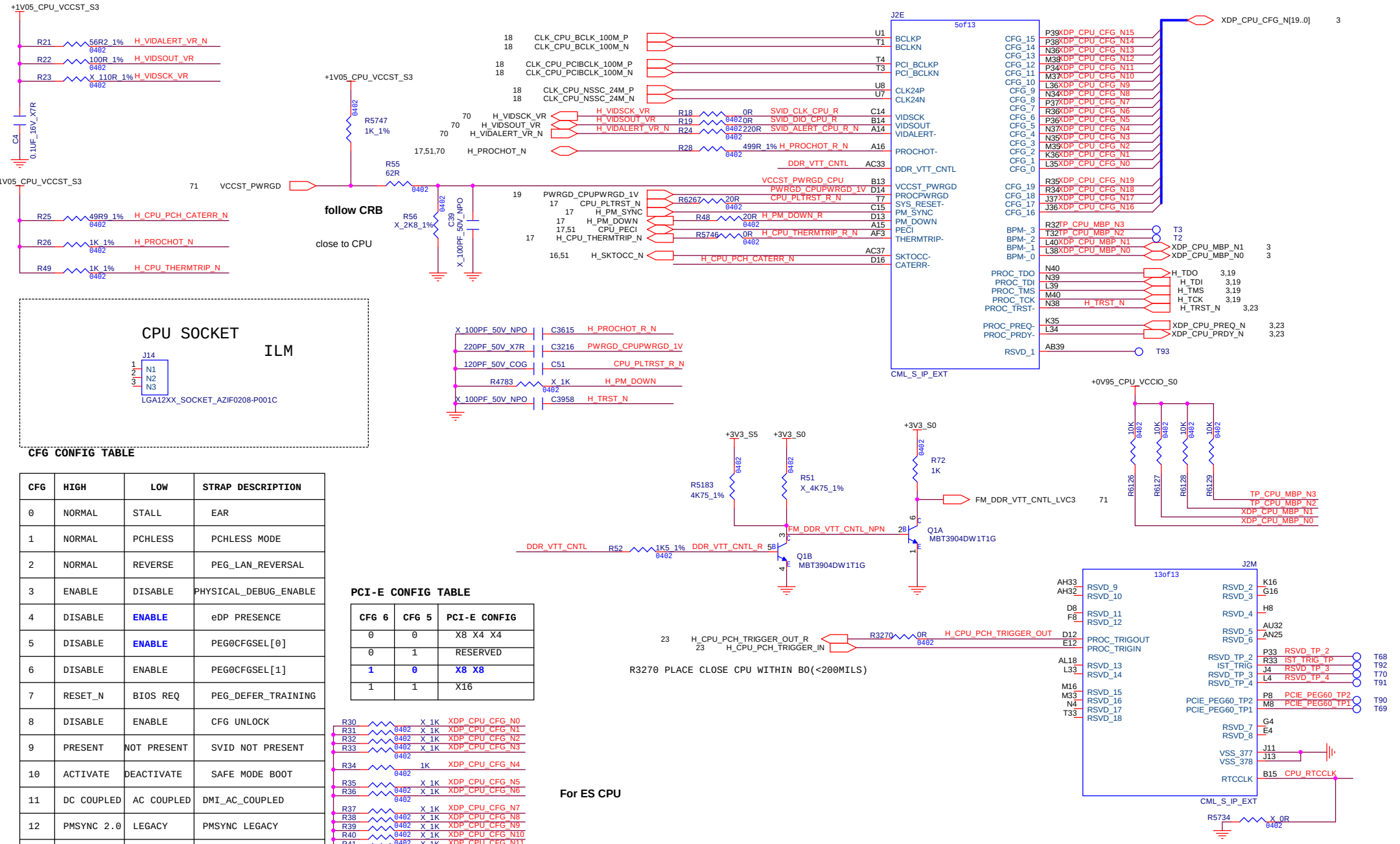

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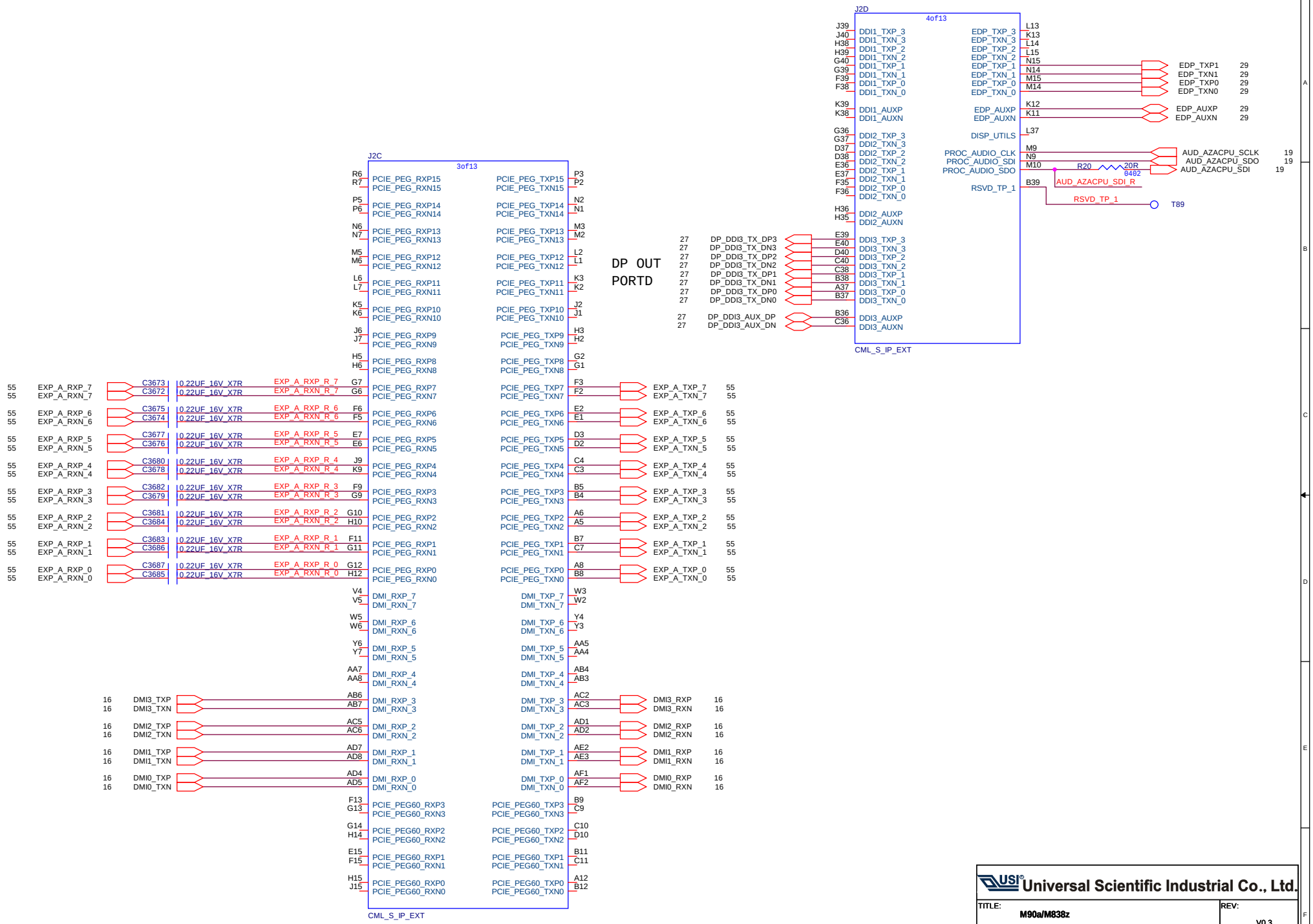

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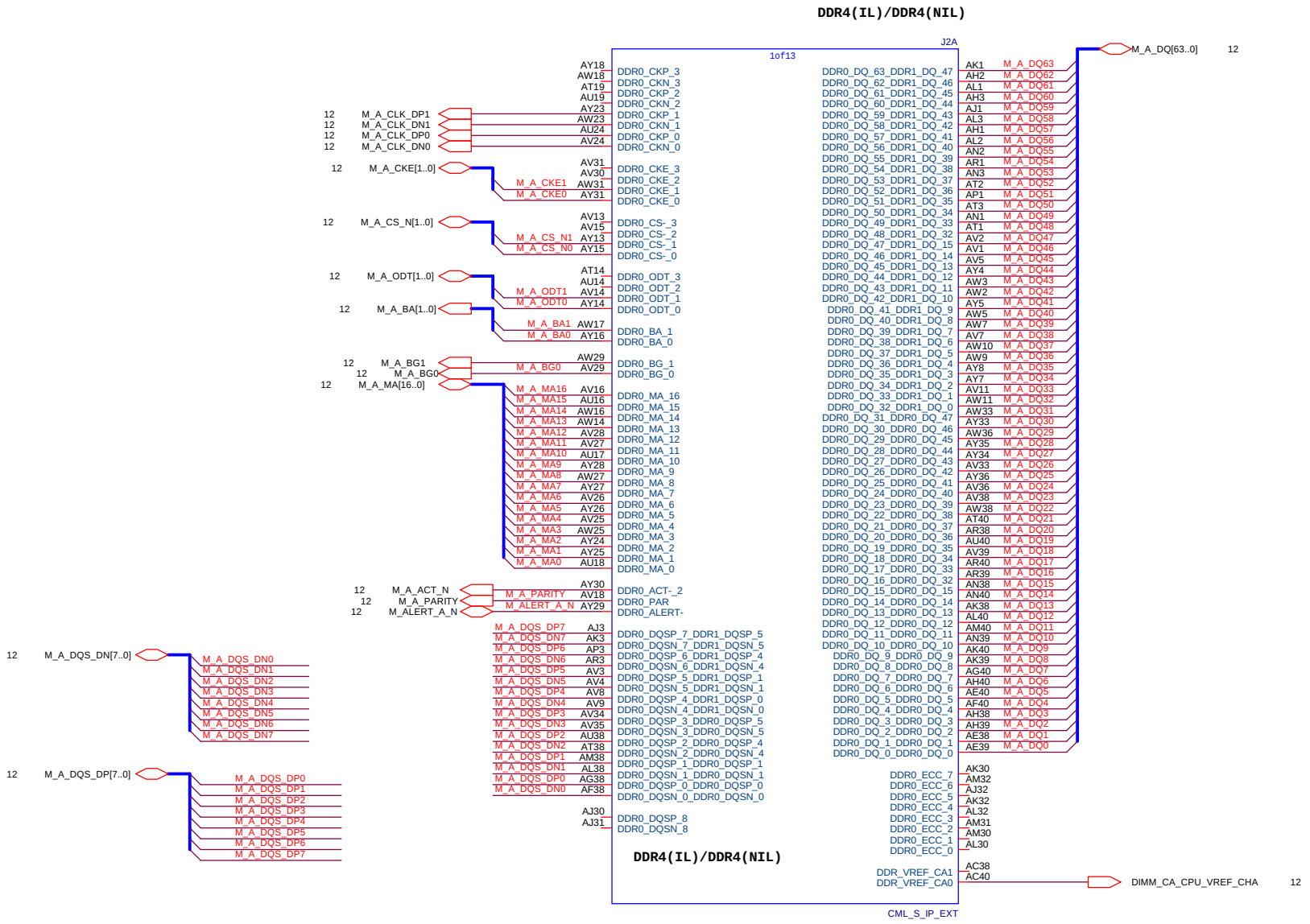

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Document Number : <Doc>	
Prepared by : KERRY HUANG	
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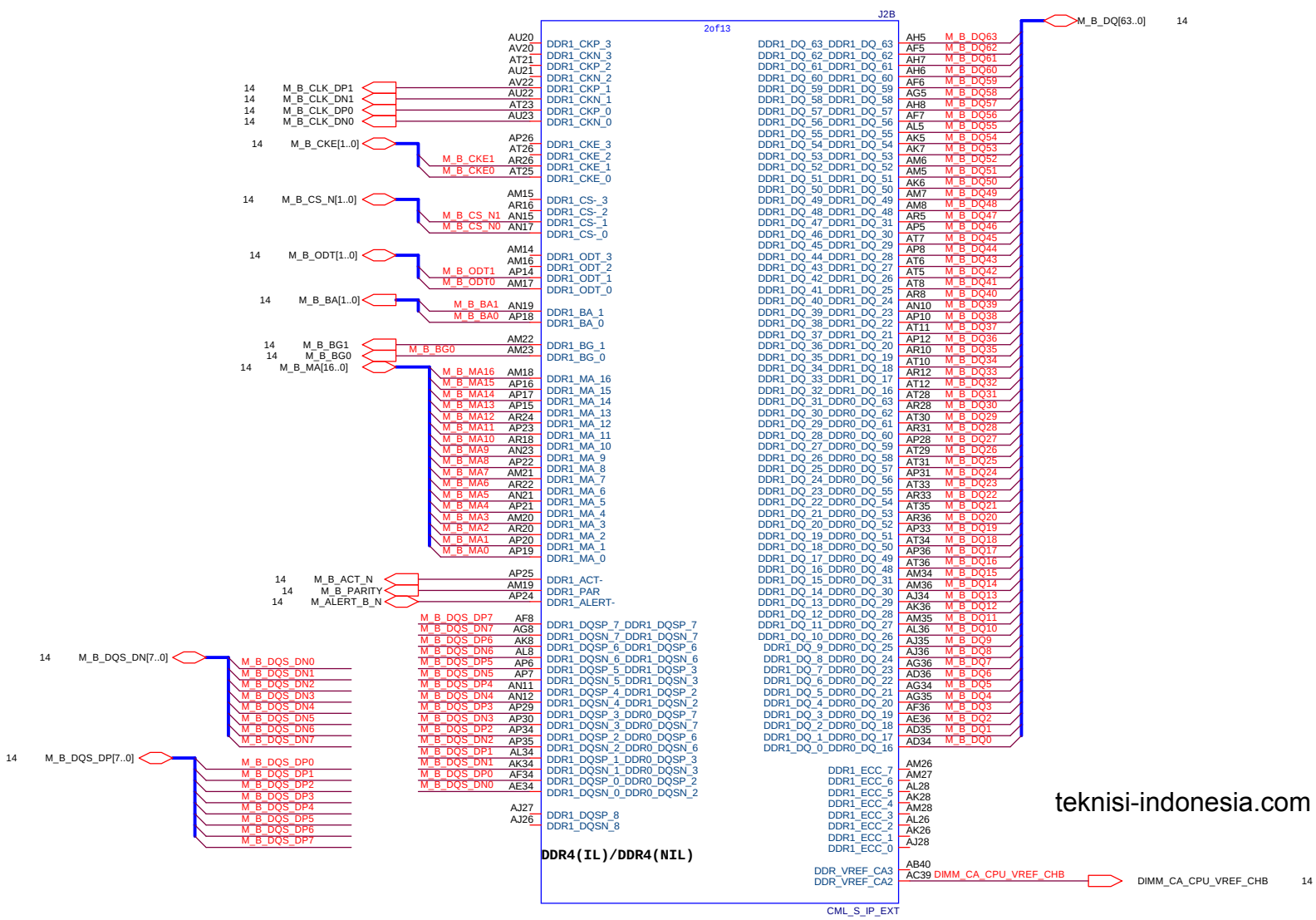

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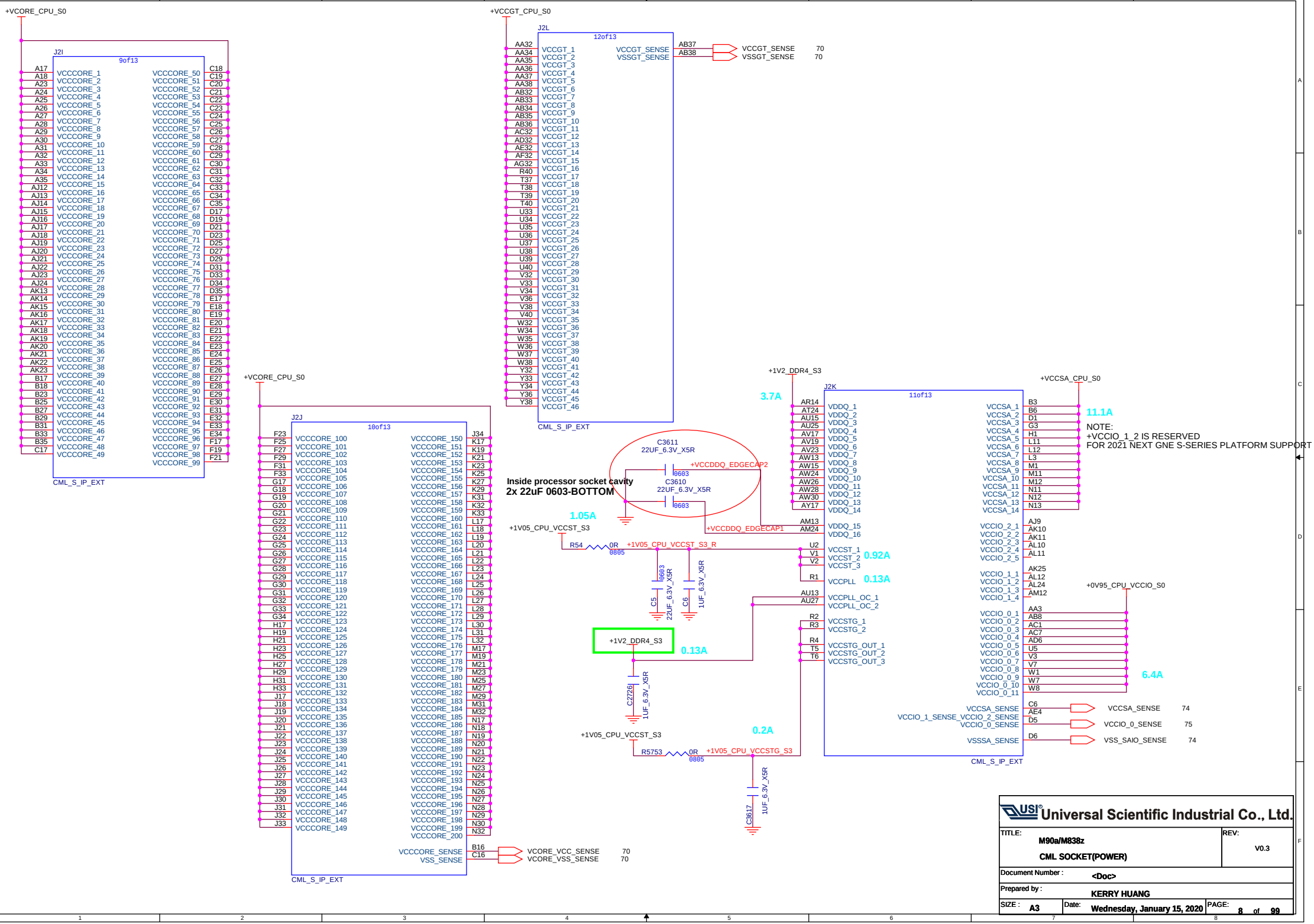
+VCORE_CPU_S0
J2I
9of13
CML_S_IP_EXT
+VCCGT_CPU_S0
J2L
12of13
VCCGT_SENSE
VSSGT_SENSE
VCCGT_SENSE 70
VSSGT_SENSE 70
CML_S_IP_EXT
+VCORE_CPU_S0
J2J
10of13
VCCCORE_SENSE
VSS_SENSE
VCORE_VCC_SENSE 70
VCORE_VSS_SENSE 70
CML_S_IP_EXT
Inside processor socket cavity
2x 22uF 0603-BOTTOM
C3611
22UF_6.3V_X5R
0603
C3610
22UF_6.3V_X5R
0603
+VCCDDQ_EDGECAP2
+VCCDDQ_EDGECAP1
+1V2_DDR4_S3
3.7A
J2K
11of13
VDDQ_1
VDDQ_2
VDDQ_3
VDDQ_4
VDDQ_5
VDDQ_6
VDDQ_7
VDDQ_8
VDDQ_9
VDDQ_10
VDDQ_11
VDDQ_12
VDDQ_13
VDDQ_14
VDDQ_15
VDDQ_16
1.05A
+1V05_CPU_VCCST_S3
R54
0R
0805
+1V05_CPU_VCCST_S3_R
C5
22UF_6.3V_X5R
0603
C6
1UF_6.3V_X5R
VCCST_1
VCCST_2
VCCST_3
0.92A
VCCPLL
0.13A
VCCPLL_OC_1
VCCPLL_OC_2
+1V2_DDR4_S3
0.13A
C2726
1UF_6.3V_X5R
VCCSTG_1
VCCSTG_2
VCCSTG_OUT_1
VCCSTG_OUT_2
VCCSTG_OUT_3
+1V05_CPU_VCCST_S3
R5753
0R
0805
+1V05_CPU_VCCSTG_S3
0.2A
C3617
1UF_6.3V_X5R
+VCCSA_CPU_S0
11.1A
NOTE:
+VCCIO_1_2 IS RESERVED
FOR 2021 NEXT GNE S-SERIES PLATFORM SUPPORT
VCCSA_1
VCCSA_2
VCCSA_3
VCCSA_4
VCCSA_5
VCCSA_6
VCCSA_7
VCCSA_8
VCCSA_9
VCCSA_10
VCCSA_11
VCCSA_12
VCCSA_13
VCCSA_14
VCCIO_2_1
VCCIO_2_2
VCCIO_2_3
VCCIO_2_4
VCCIO_2_5
VCCIO_1_1
VCCIO_1_2
VCCIO_1_3
VCCIO_1_4
+0V95_CPU_VCCIO_S0
6.4A
VCCIO_0_1
VCCIO_0_2
VCCIO_0_3
VCCIO_0_4
VCCIO_0_5
VCCIO_0_6
VCCIO_0_7
VCCIO_0_8
VCCIO_0_9
VCCIO_0_10
VCCIO_0_11
VCCSA_SENSE
VCCIO_1_SENSE_VCCIO_2_SENSE
VCCIO_0_SENSE
VSSSA_SENSE
VCCSA_SENSE 74
VCCIO_0_SENSE 75
VSS_SAIO_SENSE 74
CML_S_IP_EXT
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TITLE:
M90a/M838z
CML SOCKET(POWER)
REV:
V0.3
Document Number :
<Doc>
Prepared by :
KERRY HUANG
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A3
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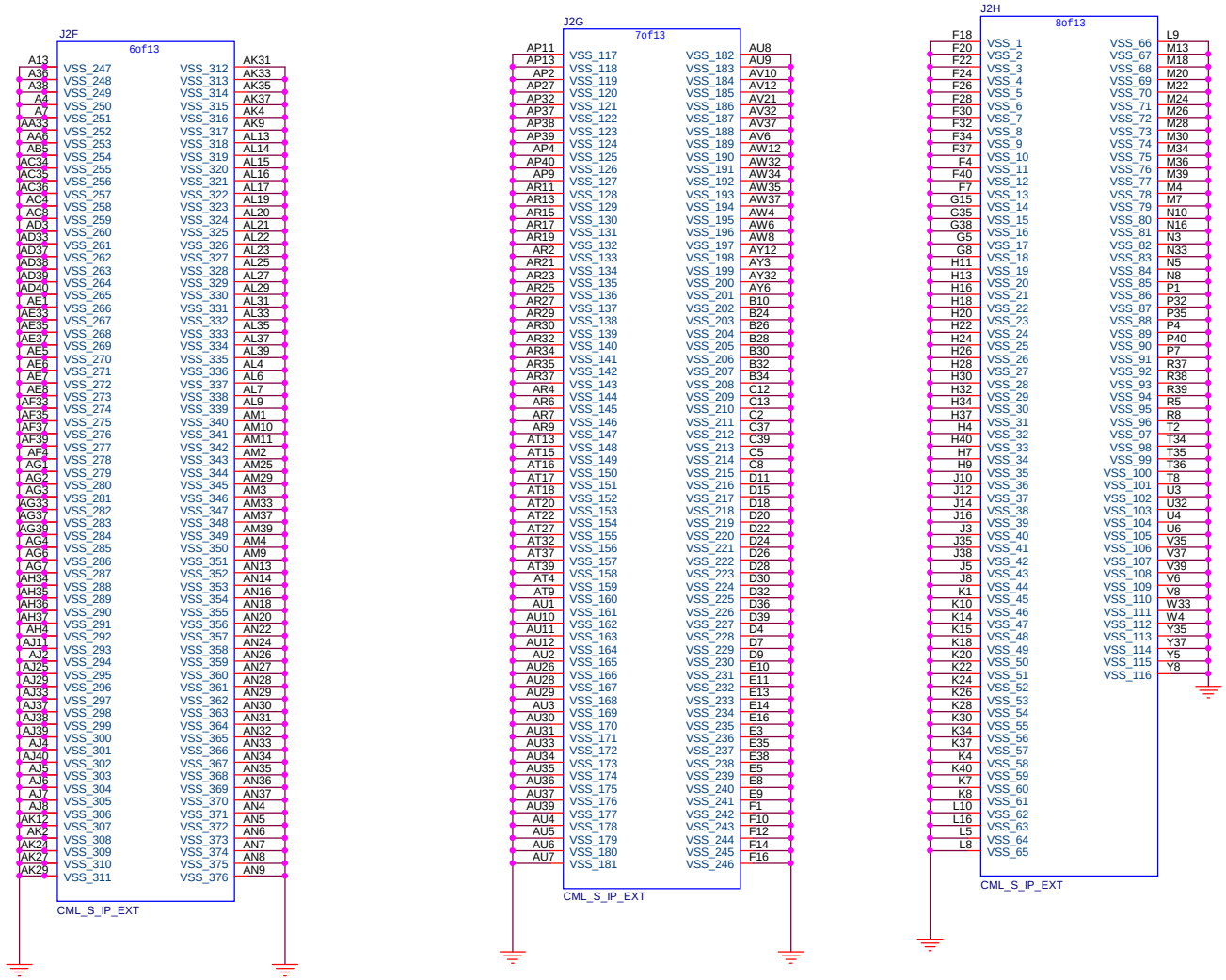

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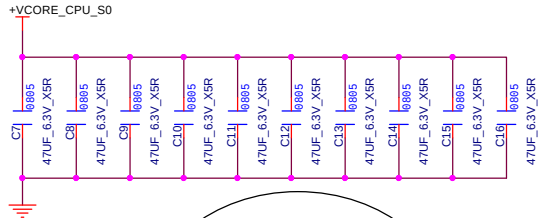
CPU DECOUPLING

Inside processor socket cavity

0805 X12 -TOP



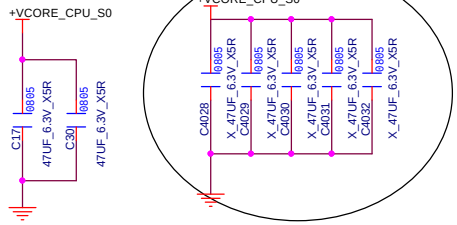
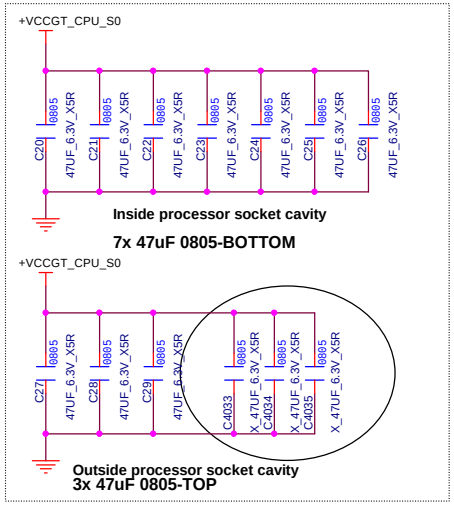
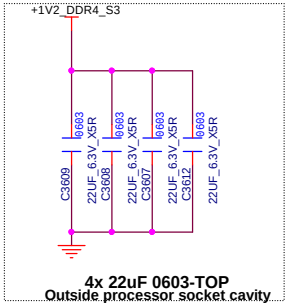
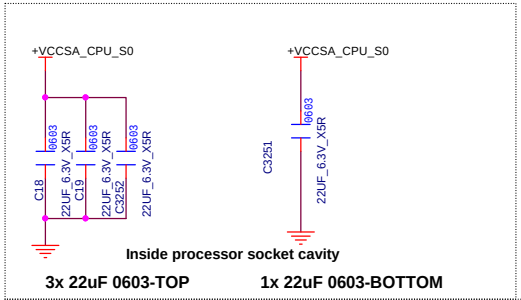


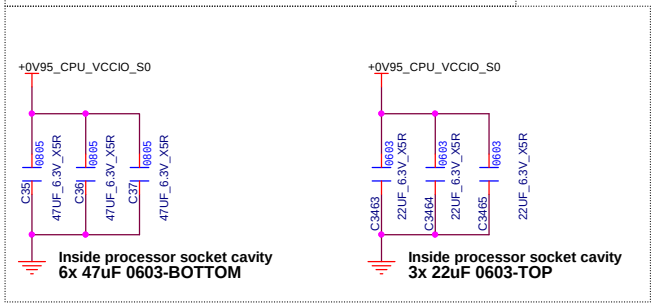
Table 318. Decoupling Requirements for CML S 6+2 Processor

Domain	Cavity cap	Outside Socket Cap	Topside/ Bottom Side	Placement Guideline and Notes
Vcc	12x 47uF 0805		Top	
		5x 47uF 0805	Top	
VccGT	7x 47uF 0805		Bottom	
		3x 47uF 0805	Top	
VccSA	3x 22uF 0603		Top	
		2x 22uF 0603	Top	
		6x 47uF 0805	Top	
	1x 22uF 0603		Bottom	
VDDQ		4x 22uF 0603	Top	
	2x 22uF 0603		Bottom	Connect caps to VDDQ_EdgeCap LGA's only. No need to connect to VDDQ plane.
VccIO	3x 22uF 0603		Top	
	3x 47uF 0805		Bottom	
VccST		1x 22uF 0805	Top	Merged with VccPLL; 0805 capacitors placed as close to processor as possible, outside the socket cavity.
		1x 1uF 0402	Top	
Vcc_{STG}		1x 1uF 0402	Top	
Vcc_{PLL_OC}		1x 1uF 0402	Top	Required if VCCPLL_OC LGA is isolated and routed to a different VR. Else short to VDDQ.









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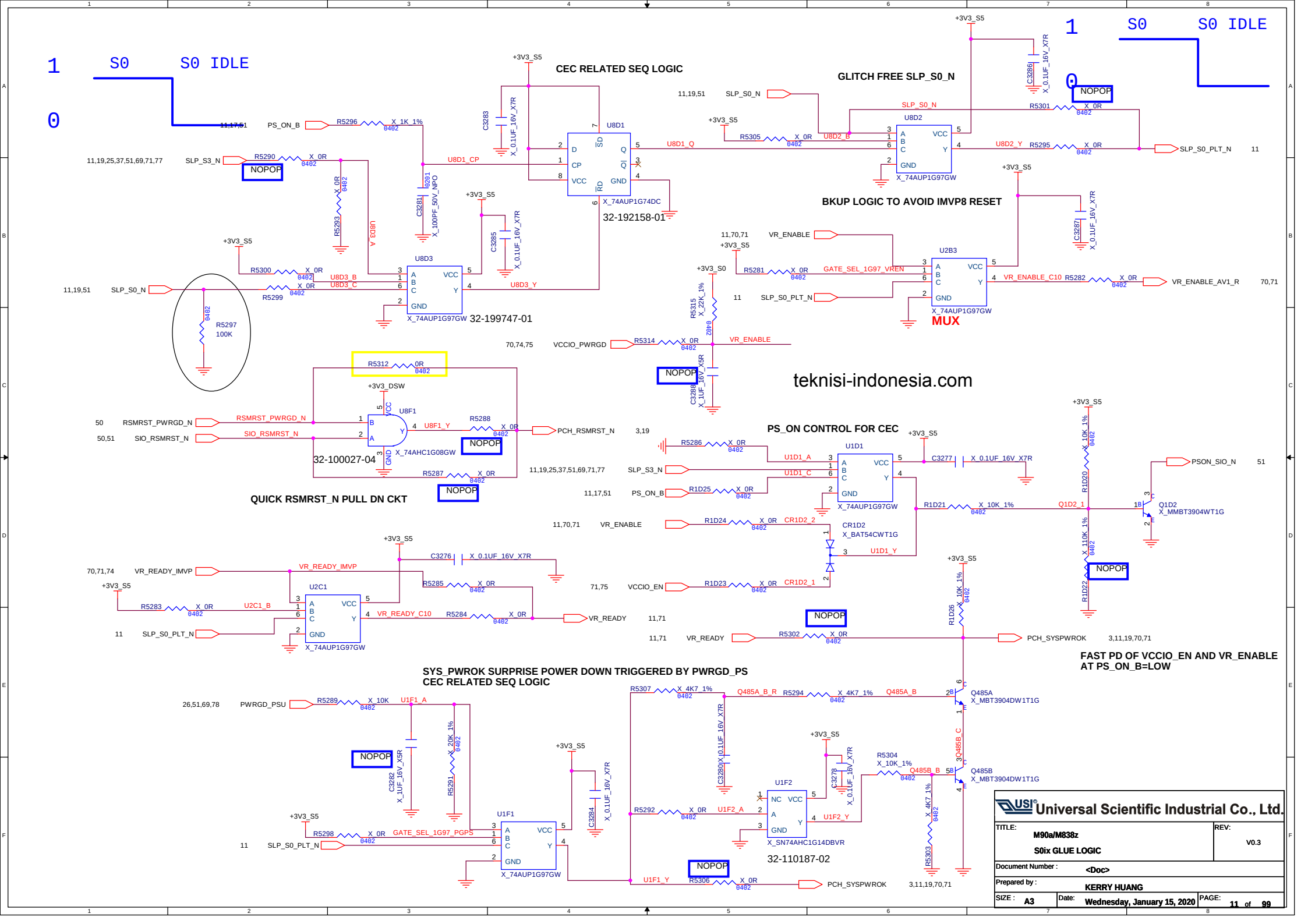
1 S0 S0 IDLE
0
CEC RELATED SEQ LOGIC
GLITCH FREE SLP_S0_N
BKUP LOGIC TO AVOID IMVP8 RESET
MUX
QUICK RSMRST_N PULL DN CKT
PS_ON CONTROL FOR CEC
SYS_PWROK SURPRISE POWER DOWN TRIGGERED BY PWRGD_PS
CEC RELATED SEQ LOGIC
FAST PD OF VCCIO_EN AND VR_ENABLE AT PS_ON_B=LOW
32-192158-01
32-199747-01
32-100027-04
32-110187-02
NOPOP
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TITLE: M90a/M838z
S0ix GLUE LOGIC
REV: V0.3
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DDR4 SO-DIMM CHANNEL A

CHANNEL A
ADDRESS:0XA0 000

DIMM1

CAD Note:
all signal should have
10 mil trace width

Data bit swapping within a byte lane

FOR ECC

FOR ECC

DDR4SODIMM260_STD_ADDR0069-P039

DDR4SODIMM260_STD_ADDR0069-P039

4.0H

CAD NOTE:
PLACE RESISTORS
CLOSE TO CH_A DIMMS
ON DIMM_VREF_A

PLACE NEAR DIMM AREA

NC
For Intel MOW

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TITLE: M90a/M838z DDR4 SO-DIMM CHANNEL A	REV: V0.3
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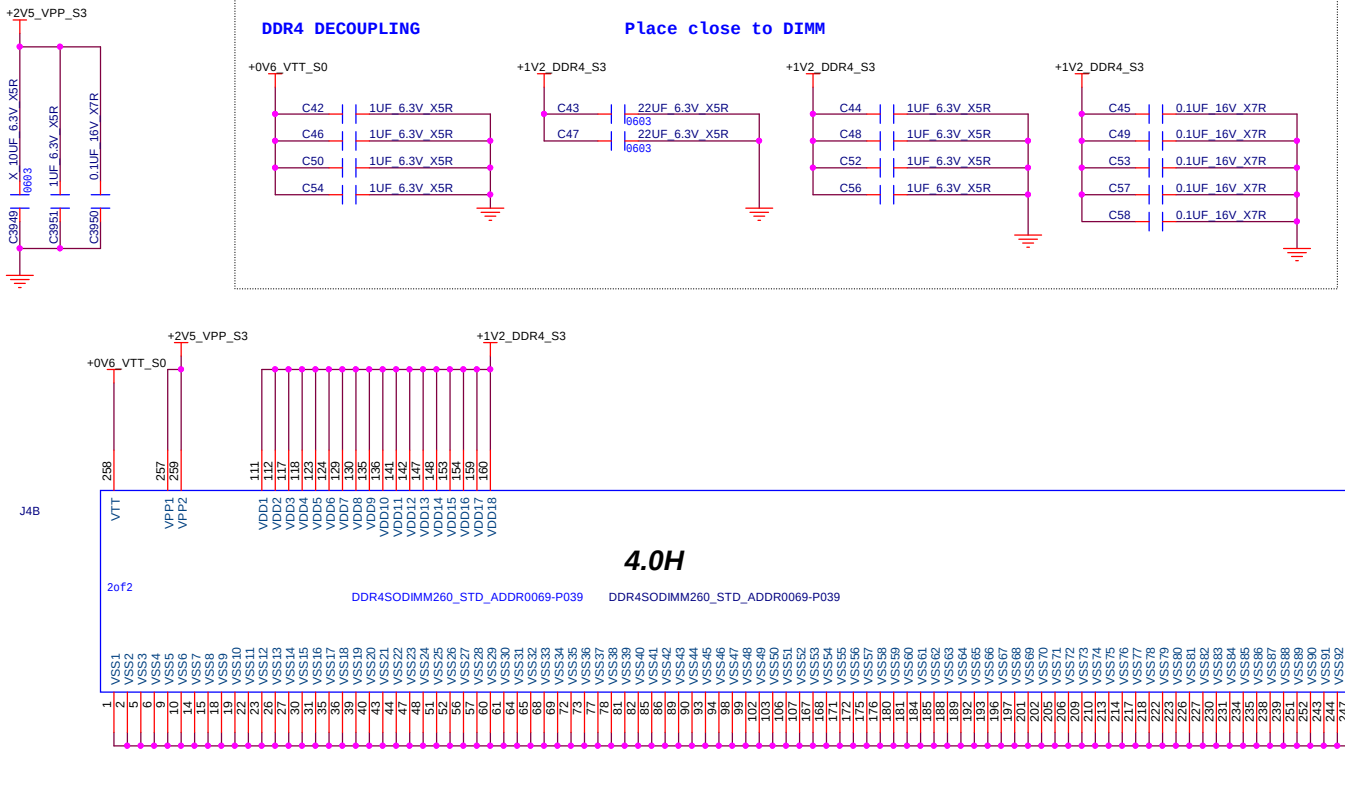
DDR4 SO-DIMM CHANNEL A



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TITLE: M90a/M838z DDR4 SO-DIMM CHANNEL A POWER		REV: V0.3
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DDR4 SO-DIMM CHANNEL B

CHANNEL B
ADDRESS:0XA4 010

DIMM2

CAD Note:
all signal should have
10 mil trace width

Data bit swapping within a byte lane

FOR ECC

FOR ECC

J3A

1of2

DDR4SODIMM260_STD_ADDR0205-P023

DDR4SODIMM260_STD_ADDR0205-P023

8.0H

CAD NOTE:
PLACE RESISTORS
CLOSE TO CH_B DIMMS
ON DIMM_VREF_B

PLACE NEAR DIMM AREA

M_RESET_N

C59
X_220PF_50V_NPO

NC
For Intel MOW

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TITLE: M90a/M838z DDR4 SO-DIMM CHANNEL B	REV: V0.3
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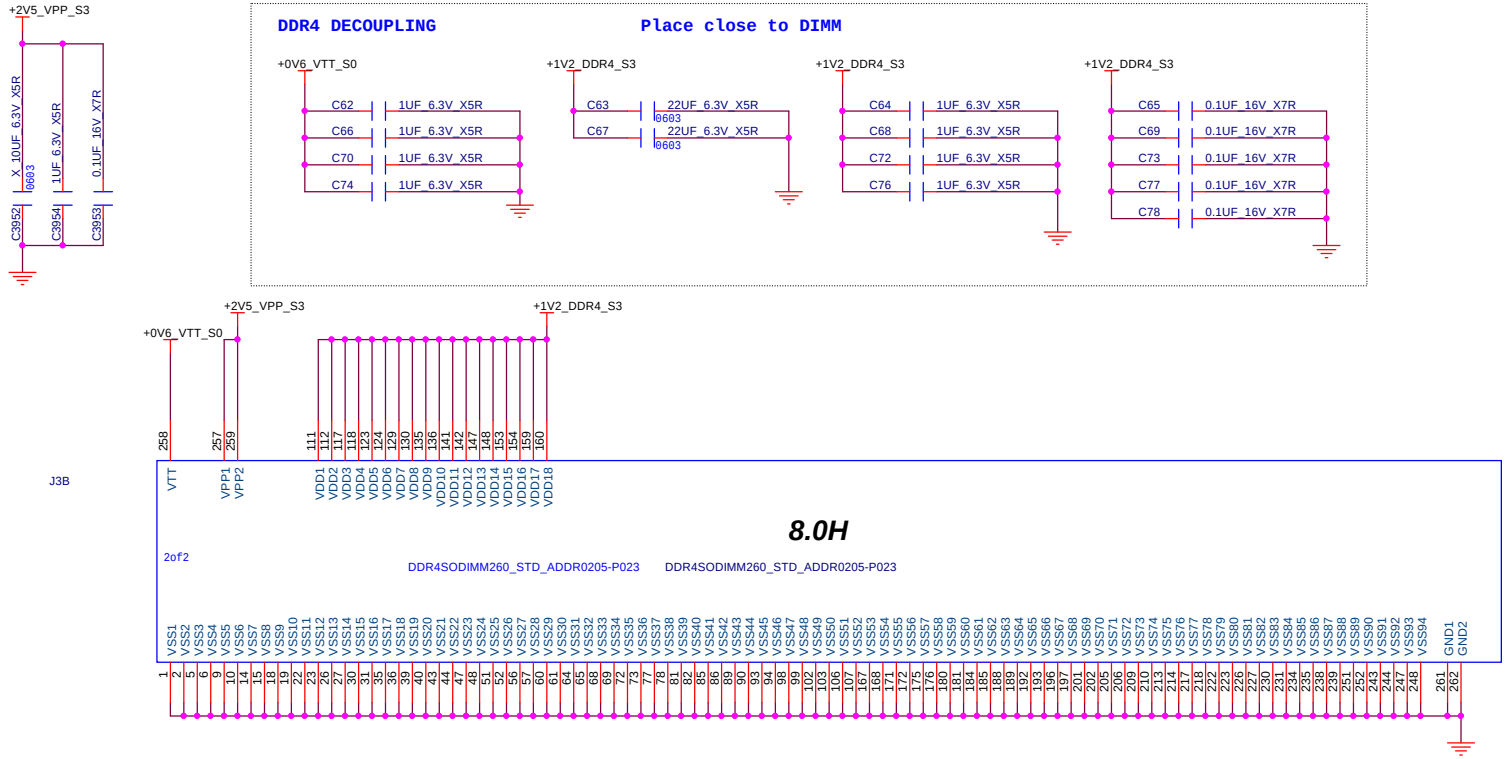
DDR4 SO-DIMM CHANNEL B



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C10 GATE LEVEL SHIFTER

+1V8_PCH_S5 +3V3_S5

C3616 X_0.1UF_16V_X7R

R5752 X_10K 0402

U316 X_SN74LVC1G07DCKRG4

16,75 CPU_C10_GATE_N → CPU_VCCIO_PWR_GATEB 75

REAR USB3.1 G1

+1V8_PCH_S5

R5343 20K 0402 CNV_BRI_RSP

+1V8_PCH_S5

R5342 20K 0402 CNV_RGI_RSP

+1V8_PCH_S5

R4991 4K7 0402

R4986 X_10K 0402 CNV_BRI_DT

STRAP:XTAL FREQ. SELECTION
1:24MHZ
0:38.4/19.2MHZ
PCH HAS INTERNAL 20K PD

+1V8_PCH_S5

R5349 X_10K 0402 CNVI_EN_N

+1V8_PCH_S5

R4990 20K 0402

R4989 X_10K 0402 CNV_RGI_DT

STRAP:M.2 CNV Mode
1 = Integrated CNVi disable.
0 = Integrated CNVi enable.
An external pull-up or pull-down is required.

+1V8_PCH_S5

R4985 X_10K 0402

R4984 X_10K 0402 CNV_MFUART2_TXD

STRAP:SELECT THE SPI FLASH INTERFERENCE OPERATING VOLTAGE
1:VCCSPI IS CONNECTED TO 1.8V RAIL
PCH HAS INTERNAL 20K PD
0:VCCSPI IS CONNECTED TO 3.3V RAIL-DEFAULT
PCH HAS INTERNAL 20K PD

U1B 2of13 — CML_PCH_H_IP_EXT

5 DMI0_RXN	K34	DMI0_RXN
5 DMI0_RXP	J35	DMI0_RXP
5 DMI0_TXN	C33	DMI0_TXN
5 DMI0_TXP	B33	DMI0_TXP
5 DMI1_RXN	G33	DMI1_RXN
5 DMI1_RXP	F34	DMI1_RXP
5 DMI1_TXN	C32	DMI1_TXN
5 DMI1_TXP	B32	DMI1_TXP
5 DMI2_RXN	K32	DMI2_RXN
5 DMI2_RXP	J32	DMI2_RXP
5 DMI2_TXN	C31	DMI2_TXN
5 DMI2_TXP	B31	DMI2_TXP
5 DMI3_RXN	G30	DMI3_RXN
5 DMI3_RXP	F30	DMI3_RXP
5 DMI3_TXN	C29	DMI3_TXN
5 DMI3_TXP	B29	DMI3_TXP
	A25	RSVD_A25
	B25	RSVD_B25
	P24	RSVD_P24
	R24	RSVD_R24
	C26	RSVD_C26
	B26	RSVD_B26
	F26	RSVD_F26
	G26	RSVD_G26
	B27	RSVD_B27
	C27	RSVD_C27
	L26	RSVD_L26
	M26	RSVD_M26
	D29	RSVD_D29
	E28	RSVD_E28
	K29	RSVD_K29
	M29	RSVD_M29

USB2N_1	J3	USB2N_1 43
USB2P_1	J2	USB2P_1 43
USB2N_2	N13	USB2N_2 43
USB2P_2	N15	USB2P_2 43
USB2N_3	K4	USB2N_3 44
USB2P_3	K3	USB2P_3 44
USB2N_4	M10	USB2N_4 45
USB2P_4	L9	USB2P_4 45
USB2N_5	M1	USB2N_5 45
USB2P_5	L2	USB2P_5 45
USB2N_6	K7	USB2N_6 51
USB2P_6	K6	USB2P_6 51
USB2N_7	L4	USB2N_7 46
USB2P_7	L3	USB2P_7 46
USB2N_8	G4	USB2N_8 39
USB2P_8	G5	USB2P_8 39
USB2N_9	M6	USB2N_9 40
USB2P_9	N8	USB2P_9 40
USB2N_10	H3	USB2N_10 32
USB2P_10	H2	USB2P_10 32
USB2N_11	R10	
USB2P_11	P9	
USB2N_12	G1	
USB2P_12	G2	
USB2N_13	N3	
USB2P_13	N2	
USB2N_14	E5	USB2N_14 34
USB2P_14	F6	USB2P_14 34

GPP_E9_USB2_OC0-	AH36	USB31_OCP#12 43
GPP_E10_USB2_OC1-	AL40	USB31_OCP#3 44
GPP_E11_USB2_OC2-	AJ44	USB31_OCP#45 45
GPP_E12_USB2_OC3-	AL41	USB31_OCP#6 46
GPP_F15_USB2_OC4-	AV47	USB31_OCP#7 46
GPP_F16_USB2_OC5-	AR35	USB2_OCP#5
GPP_F17_USB2_OC6-	AR37	USB2_OCP#6
GPP_F18_USB2_OC7-	AV43	USB2_OCP#7

USB2_COMP	F4	A_USB2_COMP R3482 113R_1% 0402
USB2_VBUSSENSE	F3	PD_USB2_VBUSSENSE R73 0402 10K 0402
RSVD1	U13	
USB2_ID	G3	TP_USB2_ID R74 10K 0402
GPD7	BE41	GPD_7

PCIE24_TXP	G45	M.2_SSD1_PCIE24_TXP 35
PCIE24_TXN	G46	M.2_SSD1_PCIE24_TXN 35
PCIE24_RXP	Y41	M.2_SSD1_PCIE24_RXP 35
PCIE24_RXN	Y40	M.2_SSD1_PCIE24_RXN 35
PCIE23_TXP	G48	M.2_SSD1_PCIE23_TXP 35
PCIE23_TXN	G49	M.2_SSD1_PCIE23_TXN 35
PCIE23_RXP	W44	M.2_SSD1_PCIE23_RXP 35
PCIE23_RXN	W43	M.2_SSD1_PCIE23_RXN 35
PCIE22_TXP	H48	M.2_SSD1_PCIE22_TXP 35
PCIE22_TXN	H47	M.2_SSD1_PCIE22_TXN 35
PCIE22_RXP	U41	M.2_SSD1_PCIE22_RXP 35
PCIE22_RXN	U40	M.2_SSD1_PCIE22_RXN 35
PCIE21_TXP	F46	M.2_SSD1_PCIE21_TXP 35
PCIE21_TXN	G47	M.2_SSD1_PCIE21_TXN 35
PCIE21_RXP	R44	M.2_SSD1_PCIE21_RXP 35
PCIE21_RXN	T43	M.2_SSD1_PCIE21_RXN 35

46 USB31_7_RXN	G17	PCIE1_RXN_USB31_7_RXN
46 USB31_7_RXP	F16	PCIE1_RXP_USB31_7_RXP
46 USB31_7_TXN	A17	PCIE1_TXN_USB31_7_TXN
46 USB31_7_TXP	B17	PCIE1_TXP_USB31_7_TXP
	R21	PCIE2_RXN_USB31_8_RXN
	P21	PCIE2_RXP_USB31_8_RXP
	B18	PCIE2_TXN_USB31_8_TXN
	C18	PCIE2_TXP_USB31_8_TXP
	K18	PCIE3_RXN_USB31_9_RXN
	J18	PCIE3_RXP_USB31_9_RXP
	B19	PCIE3_TXN_USB31_9_TXN
	C19	PCIE3_TXP_USB31_9_TXP
	N18	PCIE4_RXN_USB31_10_RXN
	R18	PCIE4_RXP_USB31_10_RXP
	D20	PCIE4_TXN_USB31_10_TXN
	C20	PCIE4_TXP_USB31_10_TXP
	F20	PCIE5_RXN
	G20	PCIE5_RXP
	B21	PCIE5_TXN
	A22	PCIE5_TXP
	K21	
	J21	PCIE6_RXN
	D21	PCIE6_RXP
	C21	PCIE6_TXN
	B23	PCIE6_TXP
	C23	PCIE7_TXP
	J24	PCIE7_TXN
	L24	PCIE7_RXP
	F24	PCIE7_RXN
	G24	PCIE8_RXN
	B24	PCIE8_RXP
	C24	PCIE8_TXN
		PCIE8_TXP

C3589 0.1UF_16V_X7R USB31_7_TXN_C
C3590 0.1UF_16V_X7R USB31_7_TXP_C

48 GLAN_PCIE5_RXN		
48 GLAN_PCIE5_RXP		
48 GLAN_PCIE5_TXN	C3591 0.1UF_6.3V_X7R	GLAN_PCIE5_TXN_C
48 GLAN_PCIE5_TXP	C3592 0201 0.1UF_6.3V_X7R 0201	GLAN_PCIE5_TXP_C

34 M.2_WIFI_PCIE7_TXP		
34 M.2_WIFI_PCIE7_TXN		
34 M.2_WIFI_PCIE7_RXP		
34 M.2_WIFI_PCIE7_RXN		

STRAP:
XTAL INPUT MODE
HIGH:XTAL INPUT IS DIFFERENTIAL
LOW:XTAL INPUT IS SINGLE-ENDED
PCH HAS INTERNAL 20K PD

+3V3_DSW

GPD_7 R4981 100K 0402

R4983 X_1K 0402

+3V3_S5

USB31_OCP#12	R5204	10K 0402
USB31_OCP#3	R5205	10K 0402
USB31_OCP#45	R5206	10K 0402
USB31_OCP#6	R5207	10K 0402
USB31_OCP#7	R6090	10K 0402
USB2_OCP#5	R4784	10K 0402
USB2_OCP#6	R4237	10K 0402
USB2_OCP#7	R4721	10K 0402

+3V3_S5

H_SKTOCC_N R4206 10K 0402

For descrete WIFI and CNVi detection

4,51 H_SKTOCC_N → H_SKTOCC_N R5230 0R H_SKTOCC_N_R 0402

R5228 47K_1% 0402

16,75 CPU_C10_GATE_N
34 CNVI_EN_N → CNVI_EN_N

34 CNV_BRI_DT_R R5744 22R 0402 CNV_BRI_DT
34 CNV_BRI_RSP CNV_BRI_RSP
34 CNV_RGI_DT_R R5743 22R 0402 CNV_RGI_DT
34 CNV_RGI_RSP CNV_RGI_RSP

CNV_MFUART2_TXD

HIGH:VCCPSI=1.8V
***LOW:VCCPSPI=3.3V**
INTERNAL 20K PD

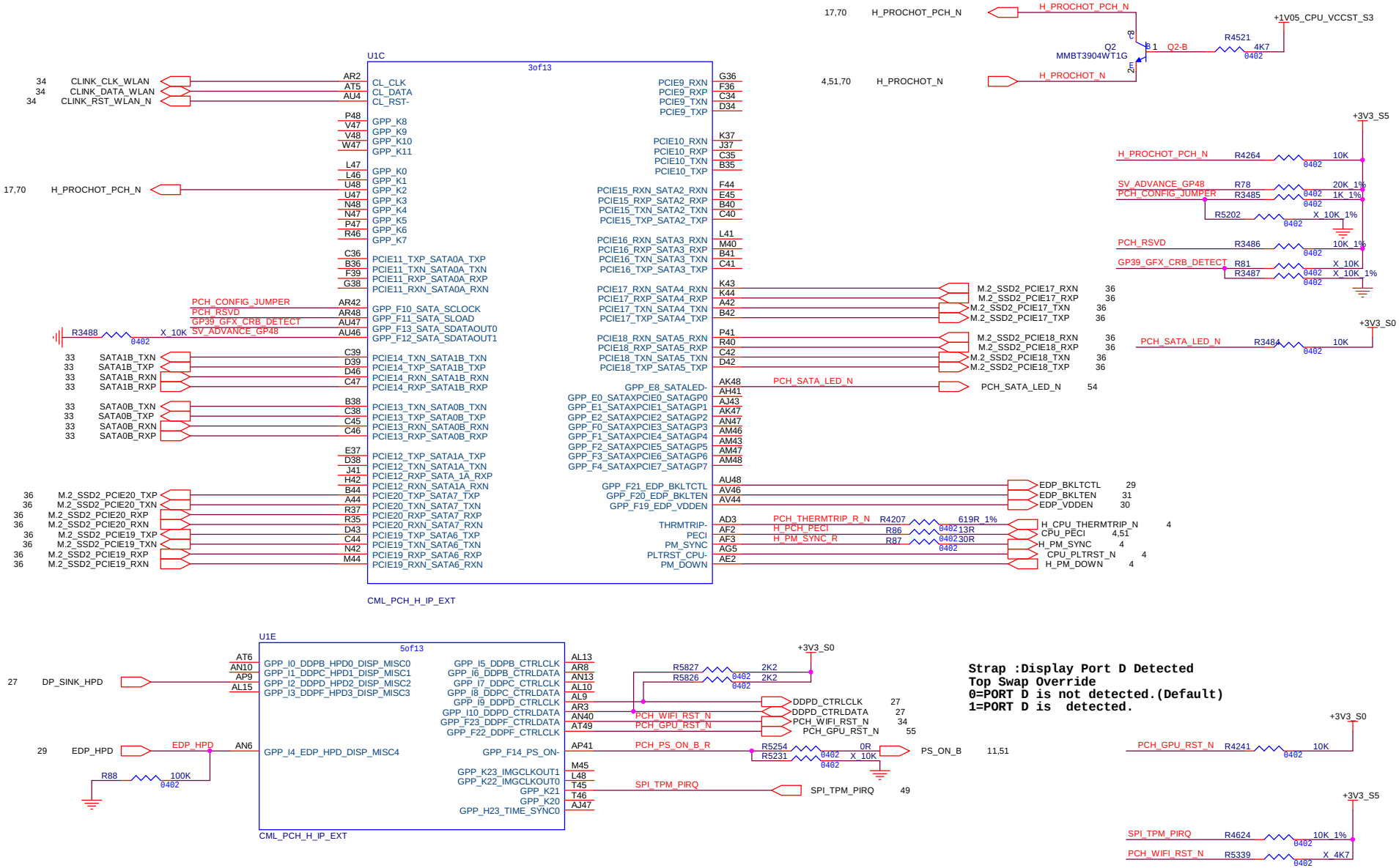
1.8V level

U1M 13of13 — CML_PCH_H_IP_EXT

	AW13	GPP_G0_SD_CMD
	BE9	GPP_G1_SD_DATA0
	BF8	GPP_G2_SD_DATA1
	BF9	GPP_G3_SD_DATA2
	BG8	GPP_G4_SD_DATA3
	BE8	GPP_G5_SD_CD-
	BD8	GPP_G6_SD_CLK
	AV13	GPP_G7_SD_WP
	AP3	GPP_I11_M2_SKT2_CFG0
	AP2	GPP_I12_M2_SKT2_CFG1
	AN4	GPP_I13_M2_SKT2_CFG2
	AM7	GPP_I14_M2_SKT2_CFG3
	AV6	GPP_J0_CNV_PA_BLANKING
	AY3	GPP_J1_CPU_C10_GATE-
	AR13	GPP_J11_A4WP_PRESENT
	AV7	GPP_J10
	AW3	GPP_J2
	AT10	GPP_J3
	AV4	GPP_J4_CNV_BRI_DT_UART0B_RTS-
	AY2	GPP_J5_CNV_BRI_RSP_UART0B_RXD
	BA4	GPP_J6_CNV_RGI_DT_UART0B_TXD
	AV3	GPP_J7_CNV_RGI_RSP_UART0B_CTS-
	AW2	GPP_J8_CNV_MFUART2_RXD
	AU9	GPP_J9_CNV_MFUART2_TXD

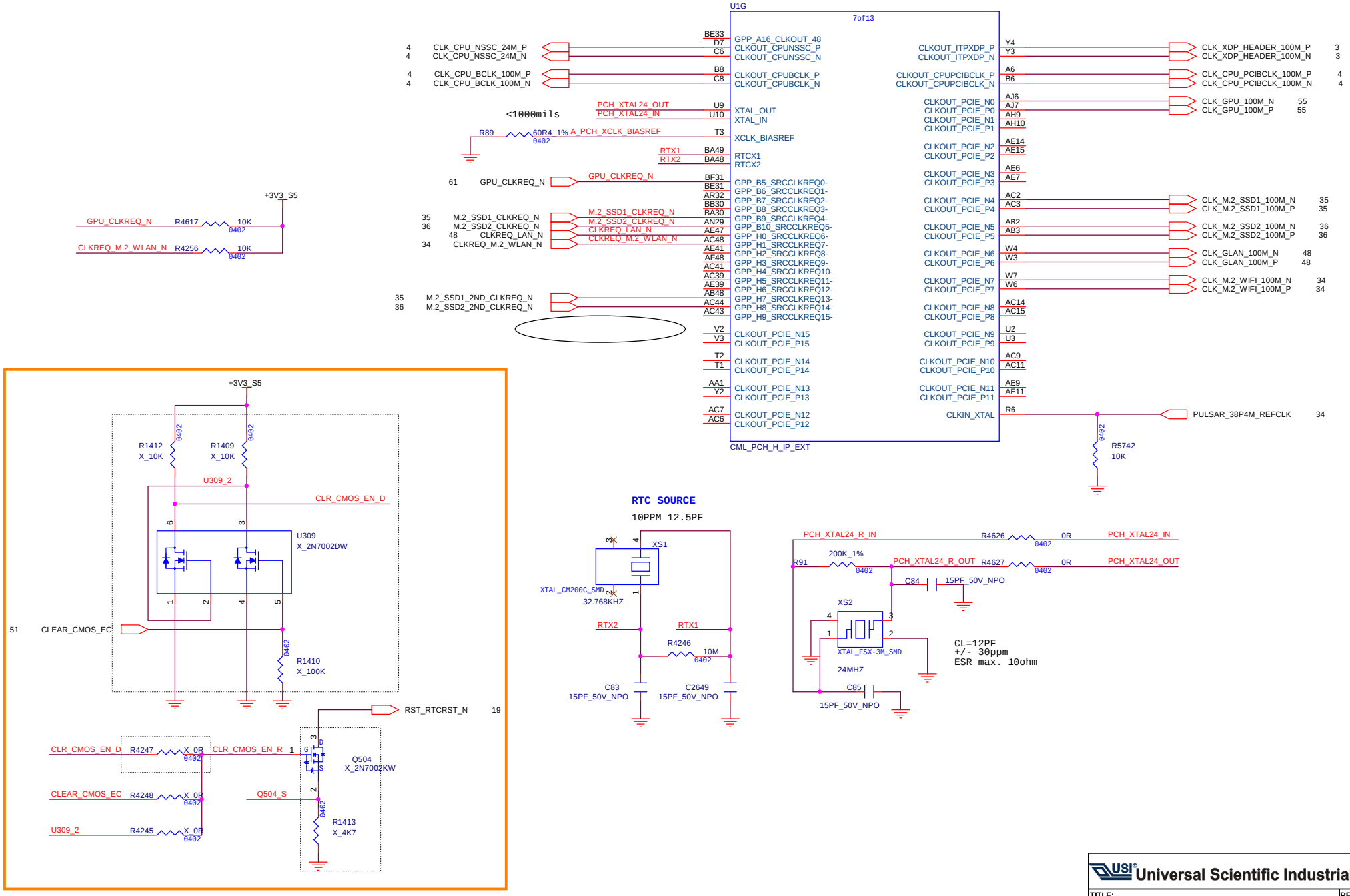
CNV_WR_CLKN	BD4	CNV_WR_CLK_DN 34
CNV_WR_CLKP	BE3	CNV_WR_CLK_DP 34
CNV_WR_D0N	BB3	CNV_WR_0_DN 34
CNV_WR_D0P	BB4	CNV_WR_0_DP 34
CNV_WR_D1N	BA3	CNV_WR_1_DN 34
CNV_WR_D1P	BA2	CNV_WR_1_DP 34
CNV_WT_CLKN	BC5	CNV_WT_CLK_DN 34
CNV_WT_CLKP	BB6	CNV_WT_CLK_DP 34
CNV_WT_D0N	BE6	CNV_WT_0_DN 34
CNV_WT_D0P	BD7	CNV_WT_0_DP 34
CNV_WT_D1N	BG6	CNV_WT_1_DN 34
CNV_WT_D1P	BF6	CNV_WT_1_DP 34
CNV_WT_RCOMP	BA1	CNV_WT_RCOMP R4654 150R_1% 0402
PCIE_RCOMPN	B12	MPHY_RCOMPN R4655 100R_1% 0402
PCIE_RCOMPP	A13	MPHY_RCOMPP
SD_1P8_RCOMP	BE5	SD3_GPPJ_RCOMP R4656 200R_1% 0402
SD_3P3_RCOMP	BE4	
GPPJ_RCOMP_1P81	BD1	
GPPJ_RCOMP_1P82	BE1	
GPPJ_RCOMP_1P83	BE2	
	Y35	
RSVD2	Y36	
RSVD3		
RSVD1	BC1	TP_RSVS_PCH T76VIA20_22B_10H_26B_AT28_TP
TP	AL35	TP_AL35 T64VIA20_22B_10H_26B_AT28_TP

Universal Scientific Industrial Co., Ltd.	
TITLE: M90a/M838z PCH DMI_PCIE_CNVI_U2_U3	REV: V0.3
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Wednesday, January 15, 2020 PAGE: 16 of 99



Universal Scientific Industrial Co., Ltd.	
TITLE: M90a/M838z PCH PCIE_SATA_DDC_CLINK	REV: V0.3
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Wednesday, January 15, 2020
PAGE: 17 of 99	

PCH CLOCK



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TITLE: M90a/M838z PCH CLOCK	REV: V0.3
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Wednesday, January 15, 2020 PAGE: 18 of 99

CLOSE TO PCH

CLOSE TO DIMM

STUFF R130 FOR NON SUPPORT HANDSHAKE MECHANISM.

1.8V level

*No test point on SRTCRST_N

POP after bring-up

follow PDG page 580,581

PLACE CLOSE TO PCH WITHIN 1.1INCH

Strap :
DCI ENABLE STRAP ENABLED IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PD

To enable Direct Connect Interface (DCI)

Strap :
Top Swap Override
0=Disable "Top Swap" mode.((W/ WEAK PD)
1=Enable "Top Swap" mode.

POP after bring-up

CLS CMOS& ME DISABLE HEADER

Strap :Flash Descriptor Security Override

1-2: ME DIS

HIGH:Disable ME in Manufacturing Mode

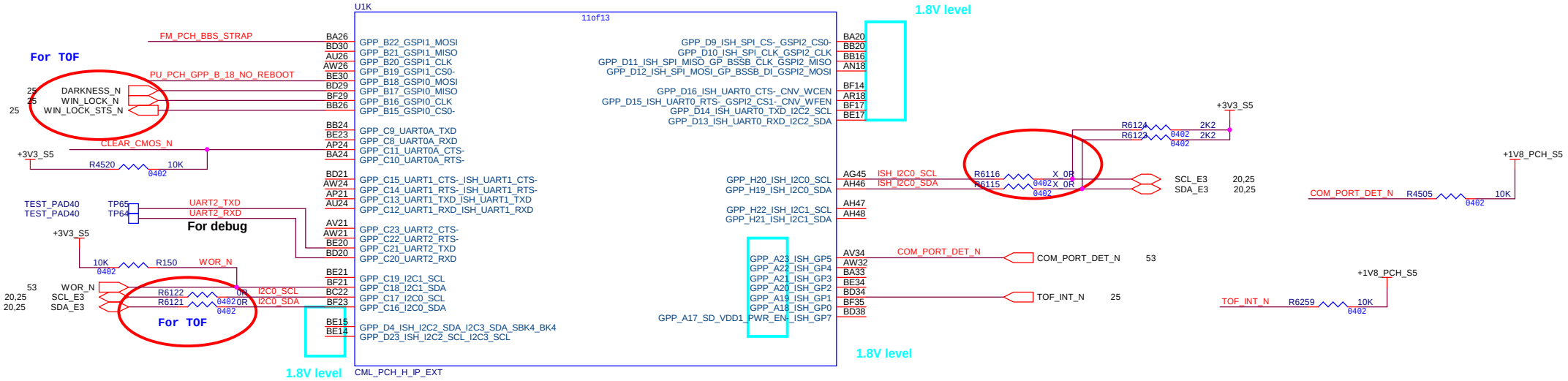
FLASH SECURITY OVERRIDE

Strap :
TLS Confi-dentiality
0:Disable(W/ WEAK PD)
1:Enable

Strap :
eSPI or LPC
0:LPC is selected for EC (W/ WEAK PD)
1:eSPI is selected for EC

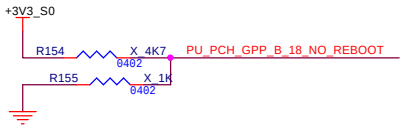
Warning: If this strap is configured to '0' (eSPI is disabled), the eSPI Flash Sharing Mode strap must be configured to '0' as well (SAFS is disabled)

Universal Scientific Industrial Co., Ltd.	
TITLE: M90a/M838z PCH HDA_SMB_MISC.	REV: V0.3
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Sunday, January 19, 2020
PAGE: 19 of 99	



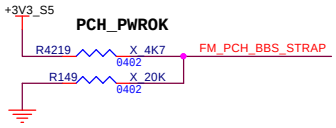
Strap :
No Reboot
0=Disable "No Reboot" mode(W/ WEAK PD)
1=Enable "No Reboot" mode

PCH_PWROK

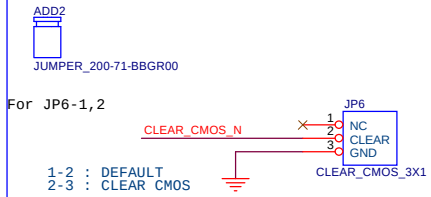


Strap :
Boot BIOS Strap Bit 10 BBS
0:SPI (W/ WEAK PD)
1:LPC

PCH_PWROK



CLEAR CMOS



Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z PCH GPIO_CLRCMOS			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 20 of 99	

1.8V:eSPI

1.8V level

U1F
6of13

51 ESPI0 R4628 33R 0402 ESPI0_PCH_AD0 BB39 GPP_A1_LAD0_ESPI_IO0
51 ESPI1 R4629 33R 0402 ESPI1_PCH_AD1 AW37 GPP_A2_LAD1_ESPI_IO1
51 ESPI2 R4630 33R 0402 ESPI2_PCH_AD2 AV37 GPP_A3_LAD2_ESPI_IO2
51 ESPI3 R4631 33R 0402 ESPI3_PCH_AD3 BA38 GPP_A4_LAD3_ESPI_IO3

51 ESPI_CS0_N R4632 0R 0402 ESPI_CS0_PCH_N BE38 GPP_A5_LFRAME-_ESPI_CS0-
ESPI_ALERT0_N AW35 GPP_A6_SERIRQ_ESPI_CS1-
KBRST_N BA36 GPP_A7_PIRQA-_ESPI_ALERT0-
BE39 GPP_A0_RCIN-_ESPI_ALERT1-
51 ESPI_RESET BF38 GPP_A14_SUS_STAT-_ESPI_RESET-
51 ESPI_CLK R167 33R 0402 ESPI_CLK_R BB36 GPP_A9_CLKOUT_LPC0_ESPI_CLK
BB34 GPP_A10_CLKOUT_LPC1
51 SIO_SCI_N SIO_SCI_N T48 GPP_K19_SMI-
T47 GPP_K18_NMI-

40 MULTI_TOUCH_DET_N MULTI_TOUCH_DET_N AH40 GPP_E6_SATA_DEVSLP2
39 CAMERA_DET_N CAMERA_DET_N AH35 GPP_E5_SATA_DEVSLP1
32 CARD_READER_DET CARD_READER_DET AL48 GPP_E4_SATA_DEVSLP0
62,66 PCH_GPU_PWR_GD PCH_GPU_PWR_GD AP47 GPP_F9_SATA_DEVSLP7
62,65 PCH_GPU_PWR_EN PCH_GPU_PWR_EN AN37 GPP_F8_SATA_DEVSLP6
AN46 GPP_F7_SATA_DEVSLP5
AR47 GPP_F6_SATA_DEVSLP4
AP48 GPP_F5_SATA_DEVSLP3

For GPU Optimus

USB31_1_TXN F9 USB31_1_TXN_C C3347 0.1UF_6.3V_X7R 0201 USB31_1_TXN 43
USB31_1_TXP F7 USB31_1_TXP_C C3348 0.1UF_6.3V_X7R 0201 USB31_1_TXP 43
USB31_1_RXN D11 USB31_1_RXN 43
USB31_1_RXP C11 USB31_1_RXP 43
USB31_2_TXN C3 USB31_2_TXN_C C3480 0.1UF_6.3V_X7R 0201 USB31_2_TXN 43
USB31_2_TXP D4 USB31_2_TXP_C C3479 0.1UF_6.3V_X7R 0201 USB31_2_TXP 43
USB31_2_RXN B9 USB31_2_RXN 43
USB31_2_RXP C9 USB31_2_RXP 43

SIDE USB3.1 G2

SIDE USB3.1 G2

USB31_6_TXN C17 USB31_6_TXN_C C3704 0.1UF_16V_X7R USB31_6_TXN 46
USB31_6_TXP C16 USB31_6_TXP_C C3703 0.1UF_16V_X7R USB31_6_TXP 46
USB31_6_RXN G14 USB31_6_RXN 46
USB31_6_RXP F14 USB31_6_RXP 46
USB31_5_TXN C15 USB31_5_TXN_C C3706 0.1UF_16V_X7R USB31_5_TXN 45
USB31_5_TXP B15 USB31_5_TXP_C C3705 0.1UF_16V_X7R USB31_5_TXP 45
J13 USB31_5_RXN 45
USB31_5_RXP K13 USB31_5_RXP 45

REAR USB3.1 G1

REAR USB3.1 G1

USB31_3_TXP G12 USB31_3_TXP_C R5361 0R USB31_3_TXP 44
USB31_3_TXN F11 USB31_3_TXN_C R5362 0R 0402 USB31_3_TXN 44
USB31_3_RXN C10 USB31_3_RXN 44
USB31_3_RXP B10 USB31_3_RXP 44

SIDE Type-C

USB31_4_TXP C14 USB31_4_TXP_C C3708 0.1UF_16V_X7R USB31_4_TXP 45
USB31_4_TXN B14 USB31_4_TXN_C C3707 0.1UF_16V_X7R USB31_4_TXN 45
J15 USB31_4_RXP 45
USB31_4_RXN K16 USB31_4_RXN 45

REAR USB3.1 G1

CML_PCH_H_IP_EXT

+1V8_PCH_S5
R6095 X_10K 0402 ESPI_CS0_PCH_N
R6094 X_10K 0402 ESPI_ALERT0_N
R5692 X_10K 0402 SER_IRQ
R6093 X_10K 0402 KBRST_N

+3V3_S5
10K 0402 R4243 CAMERA_DET_N
10K 0402 R4244 MULTI_TOUCH_DET_N

+3V3_S0
10K 0402 R4242 CARD_READER_DET

+1V8_PCH_S5
10K 0402 R160 SIO_PME_N

+3V3_S0
R5242 10K 0402 PCH_GPU_PWR_EN
100K 0402 R4258 PCH_GPU_PWR_GD

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JTAG ODT DISABLE STRAP

+3V3_S5
R5153 100K 0402
GPP_H_15
R5152 X_20K 0402

JTAG ODT DISABLED WHEN LOW(DEFAULT)
JTAG ODT ENABLED WHEN HIGH

1.8V level

U1A
1of13

51 SIO_PME_N SIO_PME_N BE36 GPP_A11_PME-_SD_VDD2_PWR_EN-
R15 RSVD2
R13 RSVD1
VIA20_22B_10H_26B_AT28_TPT72 TP_AL37 AL37 VSS_AL37
AN35 TP

3,24,49 PCH_SPI_MOSI PCH_SPI_MOSI AU41 SPI0_MOSI
24,49 PCH_SPI_MISO PCH_SPI_MISO BA45 SPI0_MISO
24 PCH_SPI_CS0_N PCH_SPI_CS0_N AY47 SPI0_CS0-
24,49 PCH_SPI_CLK PCH_SPI_CLK AW47 SPI0_CLK
24 PCH_SPI_CS1_N AW48 SPI0_CS1-

24 PCH_SPI_IO2 PCH_SPI_IO2 AY48 SPI0_IO2
24 PCH_SPI_IO3 PCH_SPI_IO3 BA46 SPI0_IO3
49 PCH_SPI_CS2_N PCH_SPI_CS2_N AT40 SPI0_CS2-
BE19 GPP_D1_SPI1_CLK_SBK1_BK1
BF19 GPP_D0_SPI1_CS-_SBK0_BK0
BF18 GPP_D3_SPI1_MOSI_SBK3_BK3
BE18 GPP_D2_SPI1_MISO_SBK2_BK2
BC17 GPP_D22_SPI1_IO3
BD17 GPP_D21_SPI1_IO2

R6264 100K 0402 PCH_SPI_CLK

R5201 X_100K 0402
GPP_B13_PLTRST- AV29 PLTRST_N 34,35,36,48,51,55

GPP_K16_GSXCLK Y47 BRD_ID4 26
GPP_K12_GSXDOUT Y46 BRD_ID0 26
GPP_K13_GSXSLOAD Y48 BRD_ID1 26
GPP_K14_GSXDIN W46 BRD_ID2 26
GPP_K15_GSXSRESET- AA45 BRD_ID3 26

GPP_E3_CPU_GP0 AL47
GPP_E7_CPU_GP1 AM45
GPP_B3_CPU_GP2 BF32 M.2_DISABLE2_N M.2_DISABLE2_N 34
GPP_B4_CPU_GP3 BC33 M.2_DISABLE1_N M.2_DISABLE1_N 34,51

GPP_H18_SML4ALERT- AE44
GPP_H17_SML4DATA AJ46
GPP_H16_SML4CLK AE43
GPP_H15_SML3ALERT- AC47 GPP_H_15
GPP_H14_SML3DATA AD48
GPP_H13_SML3CLK AF47
GPP_H12_SML2ALERT- AB47 FM_ESPI_FLASH_MODE
GPP_H11_SML2DATA AD47
GPP_H10_SML2CLK AE48
INTRUDER- BB44 INTRUDER_HDR_N

+3V3_VBAT
R506 1M 20mil
C3557 0.1UF_16V_X7R
L273 FB_120R_100MHZ_5000MA
C4022 100PF_50V_NPO
JP38 1 2 H1 H2
CASE_INTRUDER_HEADER
BOX_HD_1X2_1.25MM_W2431_SMD

CML_PCH_H_IP_EXT

STRAP:ESPI FLASH SHARING MODE
0:MAFS
1:SAFS

PCH HAS INTERNAL 20K PD
Warning: This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC strap is configured to '0' (eSPI is disabled)

+3V3_S5
R178 X_4K7 0402
FM_ESPI_FLASH_MODE
R4992 X_20K 0402

JTAG ODT DISABLE STRAP

+3V3_S5
R179 X_20K 0402
PCH_SPI_MISO
R176 X_4K7 0402

JTAG ODT DISABLED WHEN LOW
JTAG ODT ENABLED WHEN HIGH (DEFAULT)
PCH INTERNAL PULL-UP

BOOT HALT STRAP (DFX)
REFER TO PCH XDP PAGE AS WELL

+3V3_S5
R4230 100K 0402
PCH_SPI_MOSI
R180 X_4K7 0402

BOOT HALT DISABLED WHEN HIGH (DEFAULT)
BOOT HALT ENABLED WHEN LOW
PCH INTERNAL PULL-UP

CONSENT STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU

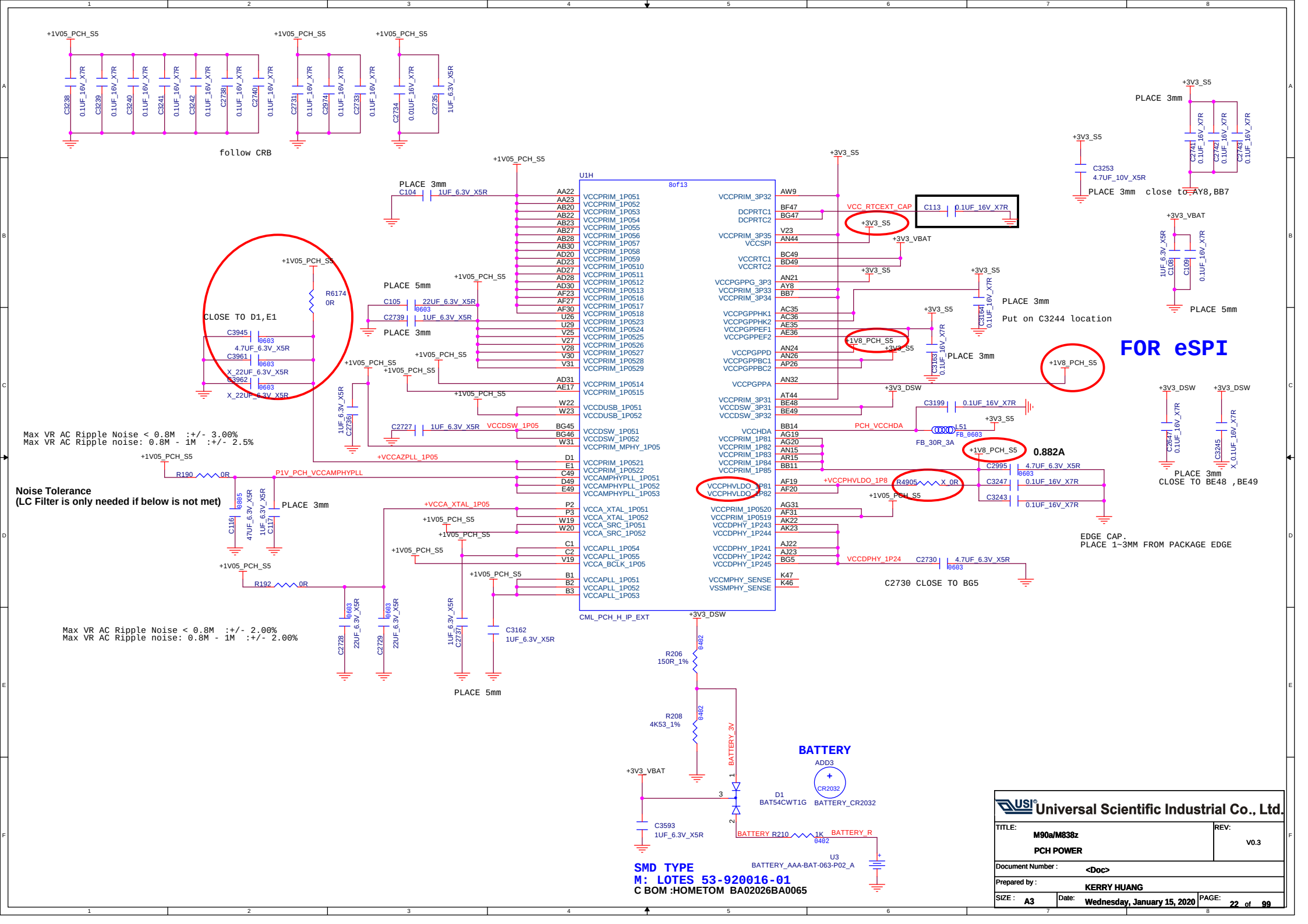
+3V3_S5
R181 100K 0402
PCH_SPI_IO2
R4226 X_4K7 0402

PESONALITY STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU

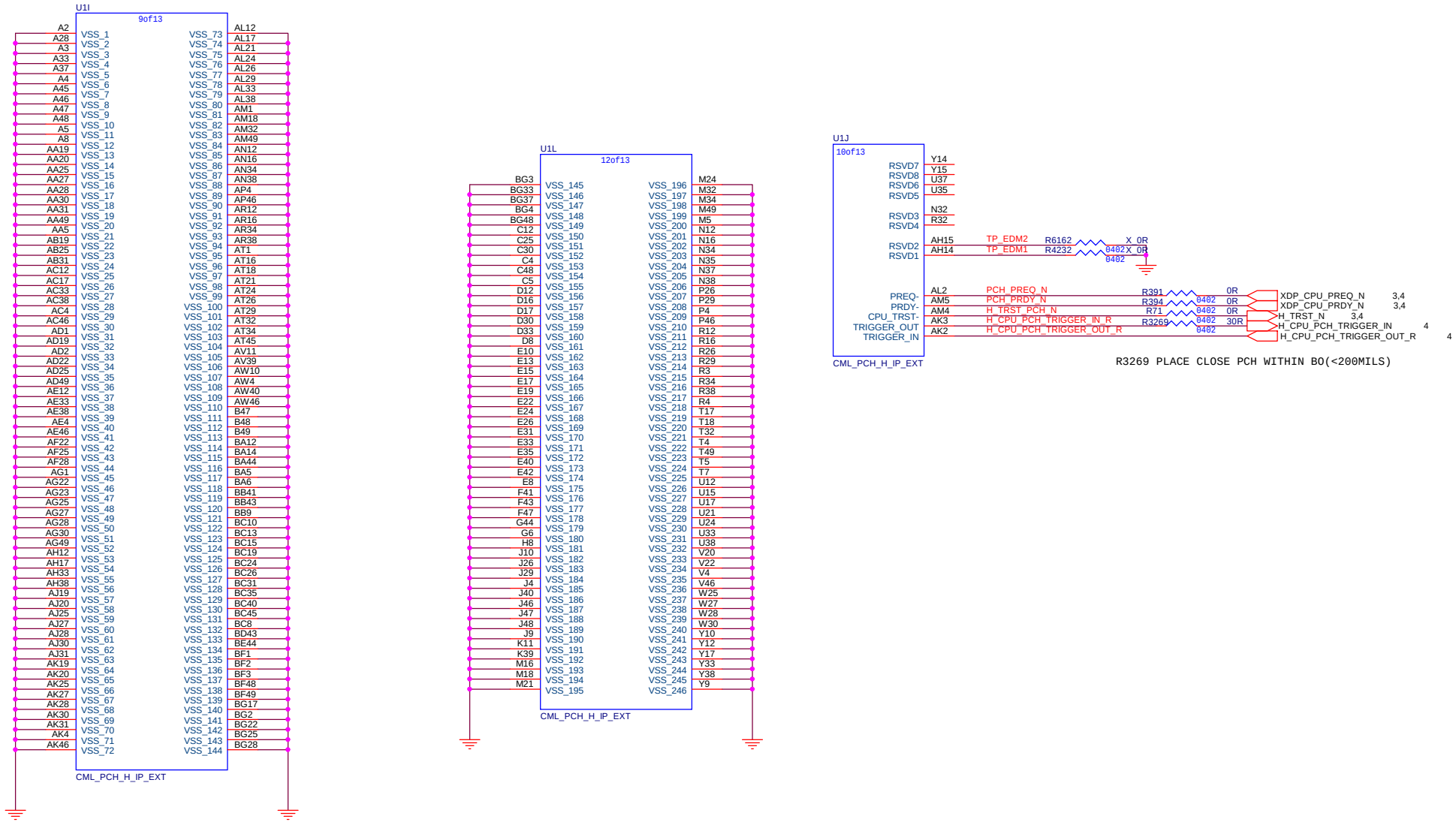
+3V3_S5
R182 100K 0402
PCH_SPI_IO3
R184 X_4K7 0402

Universal Scientific Industrial Co., Ltd.

TITLE: M90a/M838z PCH eSPI_LPC_SPI_U3_U2		REV: V0.3
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 21 of 99

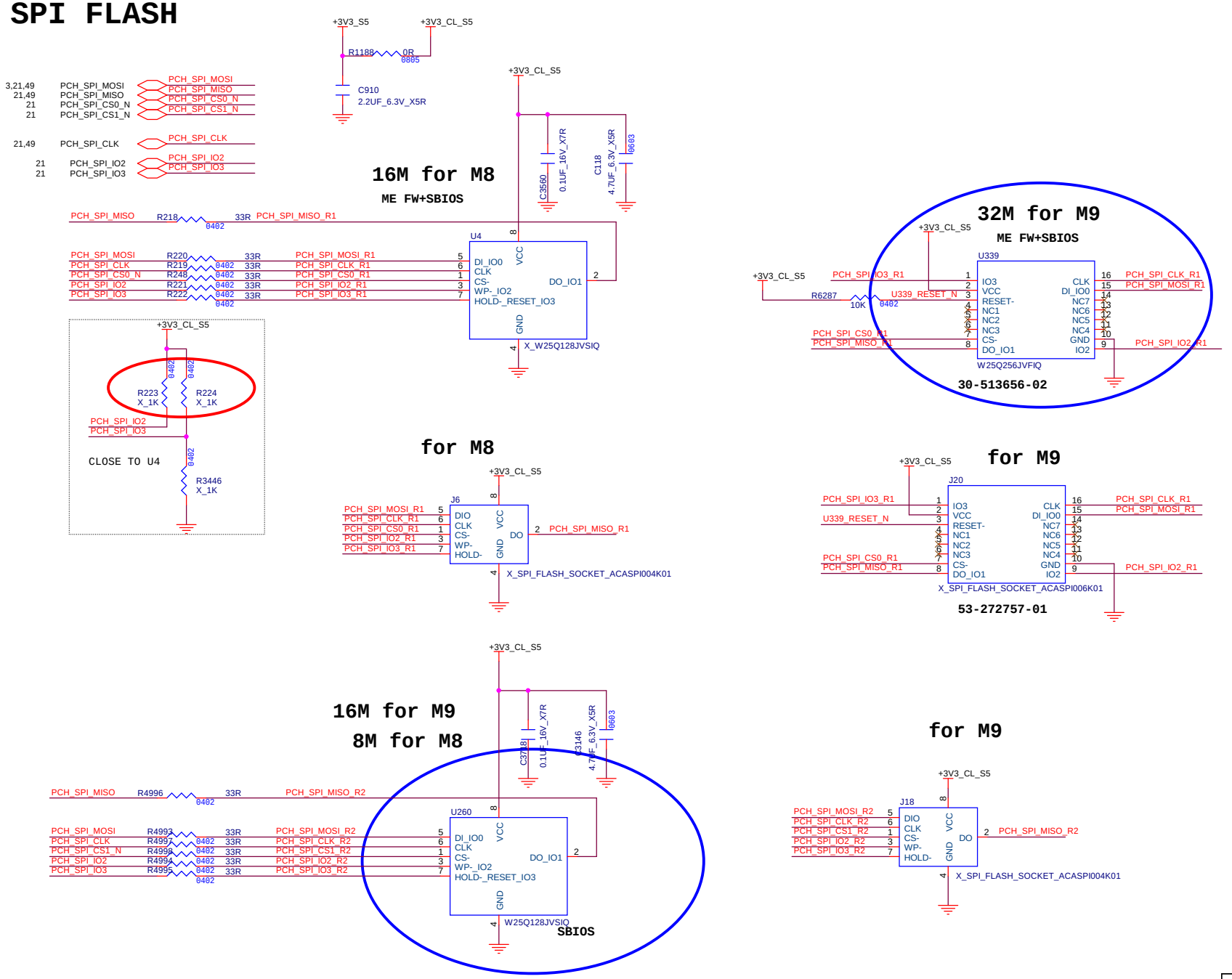


Universal Scientific Industrial Co., Ltd.	
TITLE: M90a/M838z PCH POWER	REV: V0.3
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Wednesday, January 15, 2020
PAGE: 22 of 99	

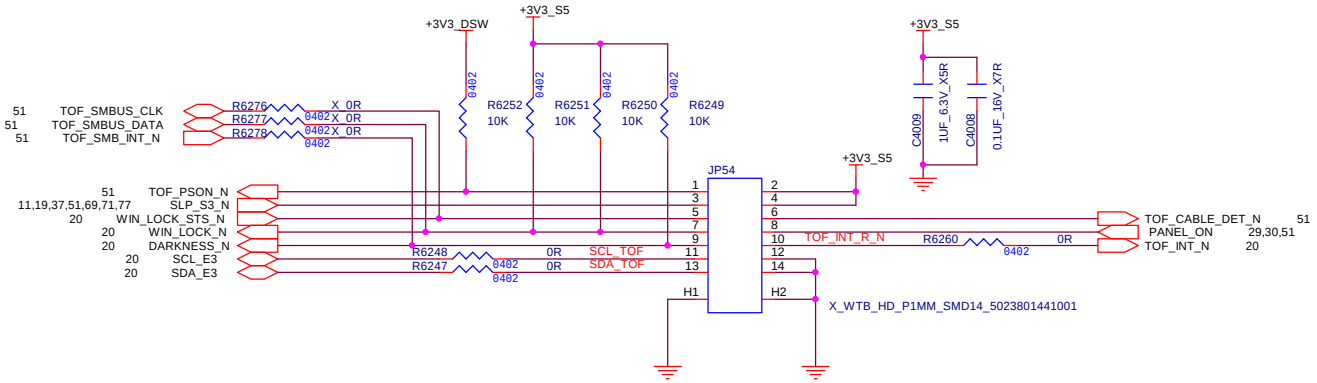


Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z PCH GND			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 23 of 99	

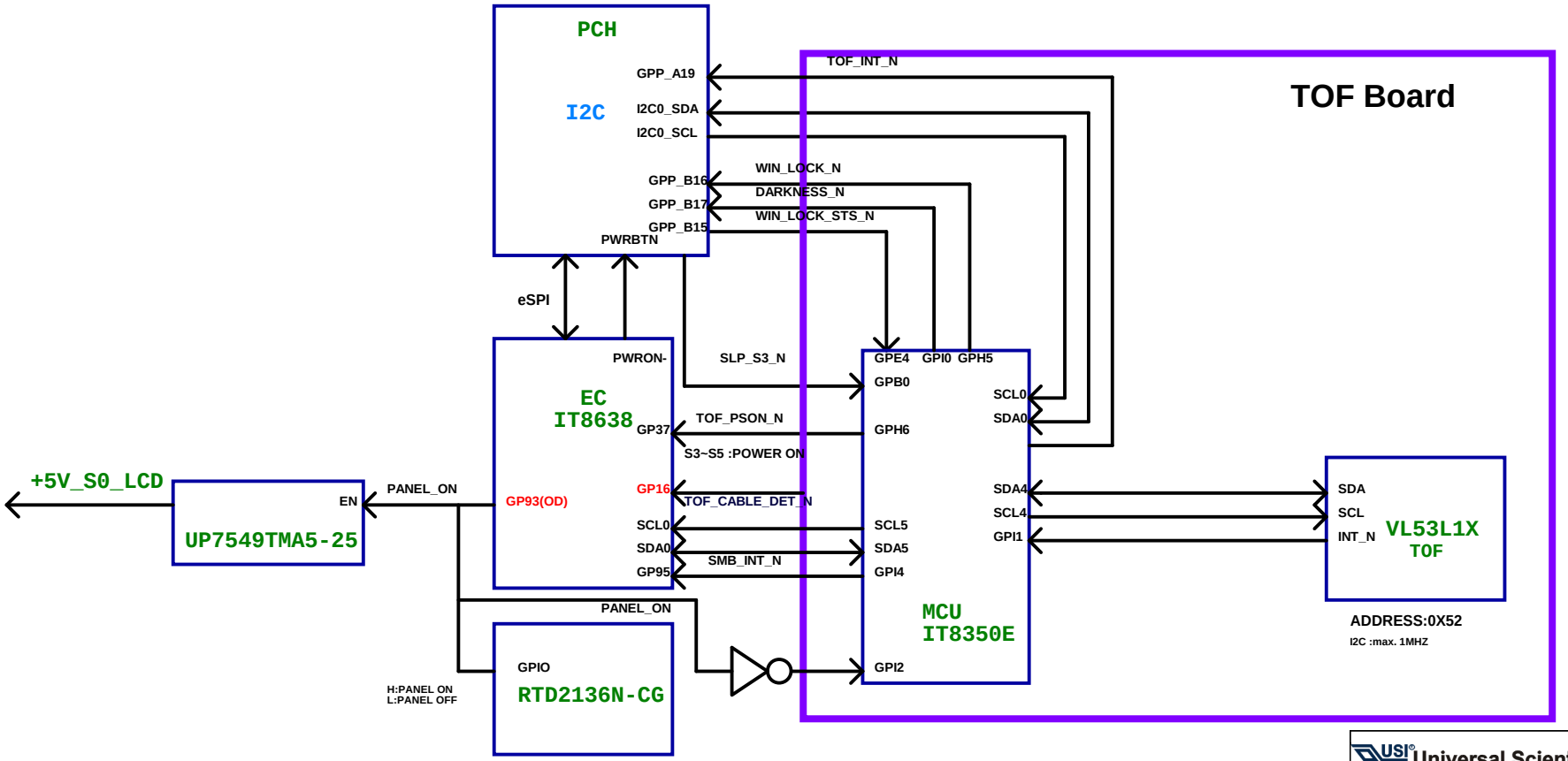
SPI FLASH



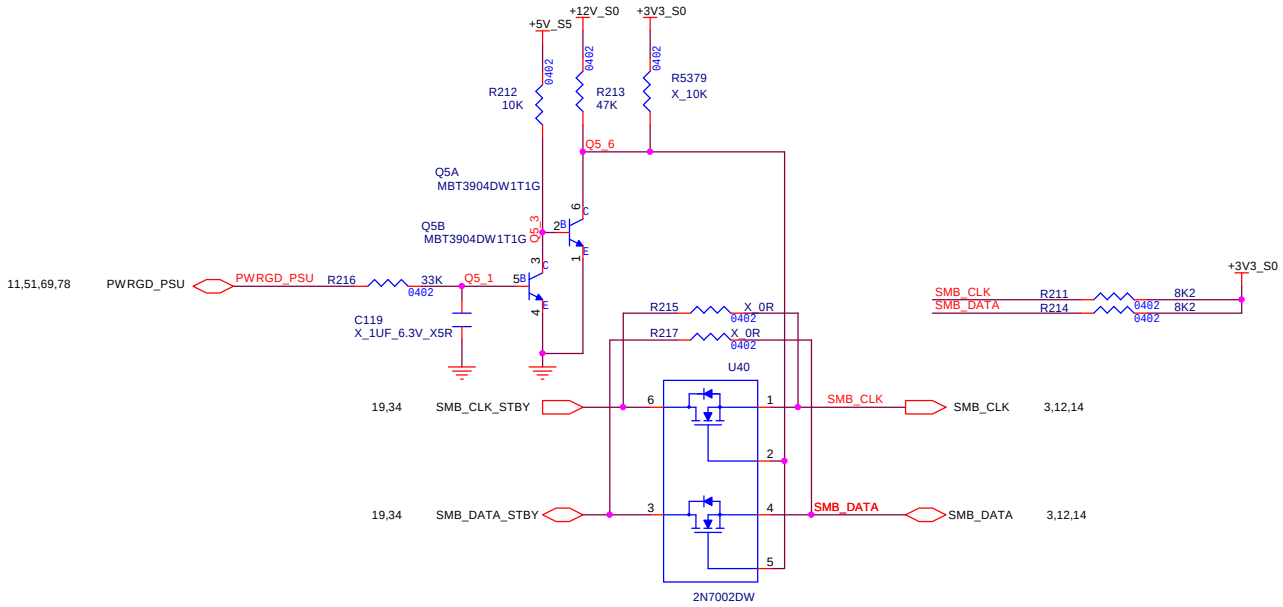
Universal Scientific Industrial Co., Ltd.	
TITLE: M90a/M838z SPI & SMBUS & BOARD ID	REV: V0.3
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Wednesday, January 15, 2020 PAGE: 24 of 99



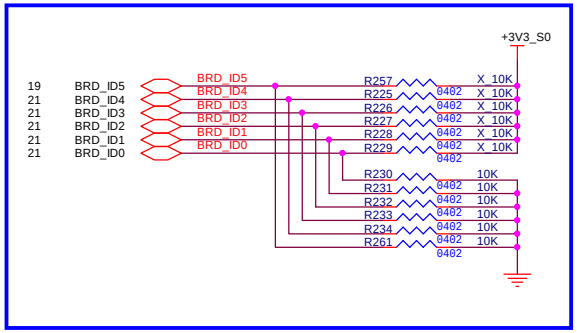
V0.3



Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z TOF HD			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 25 of 99	



BOARD ID



BOARD ID MAP	ID5	ID4	ID3	ID2	ID1	ID0	
(1)M90a w/GPU TPM w/ computrace --Q470 LI	0	0	0	0	0	0	default
(2)M90a UMA TPM w/ computrace --Q470 LI	0	0	0	0	0	1	
(3)M838z W/GPU w/o TPM w/o computrace -H470 LC	0	0	0	0	1	0	
(4)M90a w/GPU w/o TPM w/o computrace --Q470 LC	0	0	0	0	1	1	
	0	0	0	1	0	0	
	0	0	0	1	0	1	
	0	0	0	1	1	0	

Universal Scientific Industrial Co., Ltd.

TITLE: M90a/M838z BOARD ID_SMBUS LS	REV: V0.3
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3 / Date: Wednesday, January 15, 2020	PAGE: 26 of 99

DISPLAY PORT

Vout	3.467V
PDmax	1.33W
PD	0.85W
ILIM	3.5A

DPC_CAD	OA	OD	
1	DDPD_CTRLDATA	DDPD_CTRLCLK	HDMI
0	DPOUT_AUX_DN	DPOUT_AUX_DP	DP

NOPOP FOR HDMI
SOURCE

NOPOP FOR HDMI

NOPOP FOR HDMI

Keep 25mil

Keep 25mil

set 3.467V

APL5932BKAI-TRG-B BOM
UP8803PSW8- C BOM

VREF=0.8V

POP FOR HDMI

PREVENT DRIVING HPD IN POWER OFF

NOPOP R5740 FOR HDMI
POP R5864 FOR HDMI
NOPOP R5867 FOR HDMI
NOPOP R5756 FOR HDMI
POP R5859 FOR HDMI
NOPOP R5860 FOR HDMI

POP R5862 FOR HDMI
NOPOP R390 FOR HDMI

NOPOP R6147 R6148 for HDMI

POP when U335 pop

POP when U153 NOPOP

POP 20K FOR HDMI

POP R5866 FOR HDMI
NOPOP R5865 5860 FOR HDMI

POP FOR HDMI

POP FOR HDMI
HDMI Cost Reduced Level Shifter

Power

Universal Scientific Industrial Co., Ltd.	
TITLE: M90a/M838z DP PORT	REV: V0.3
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Wednesday, January 15, 2020 PAGE: 27 of 99

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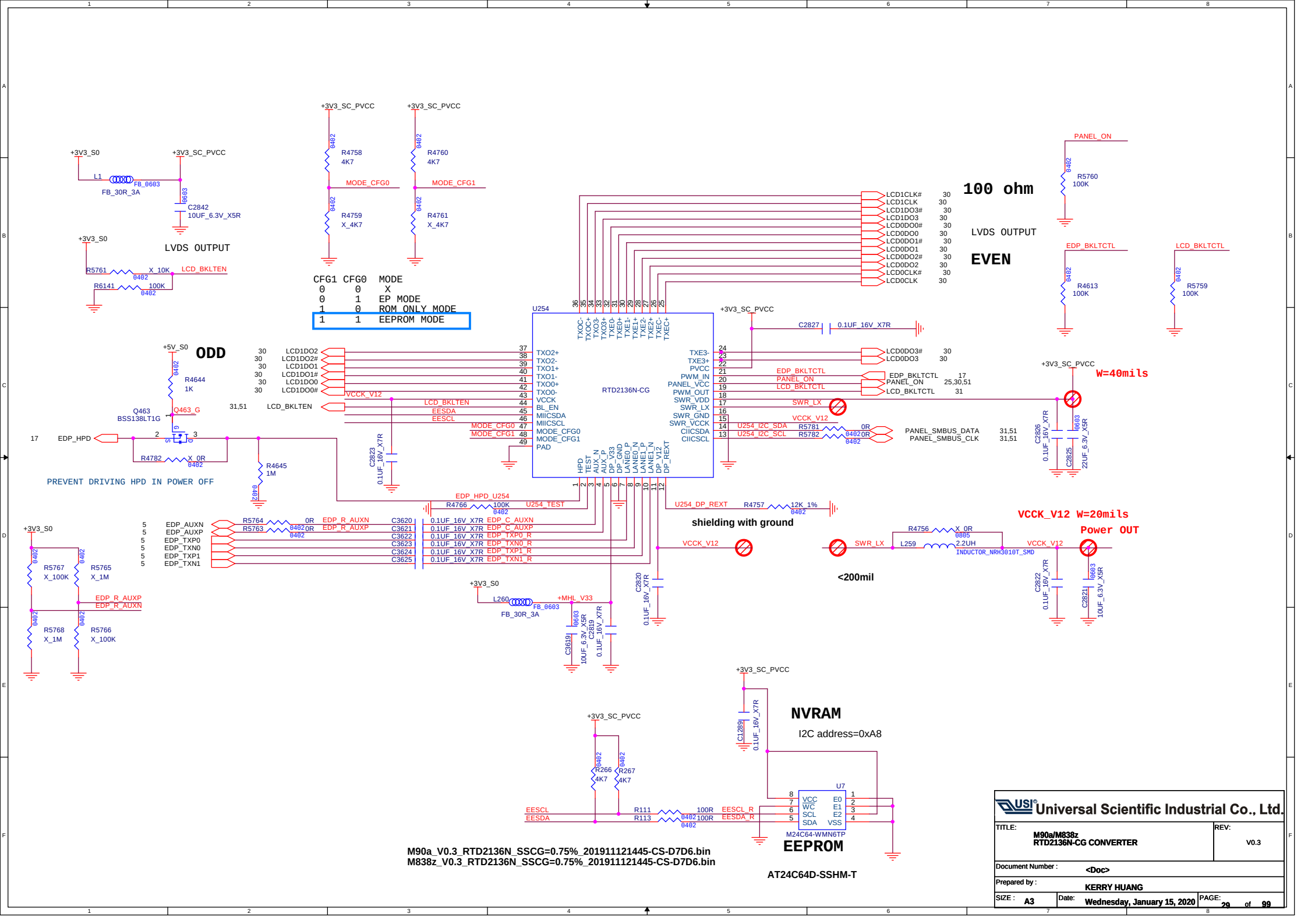
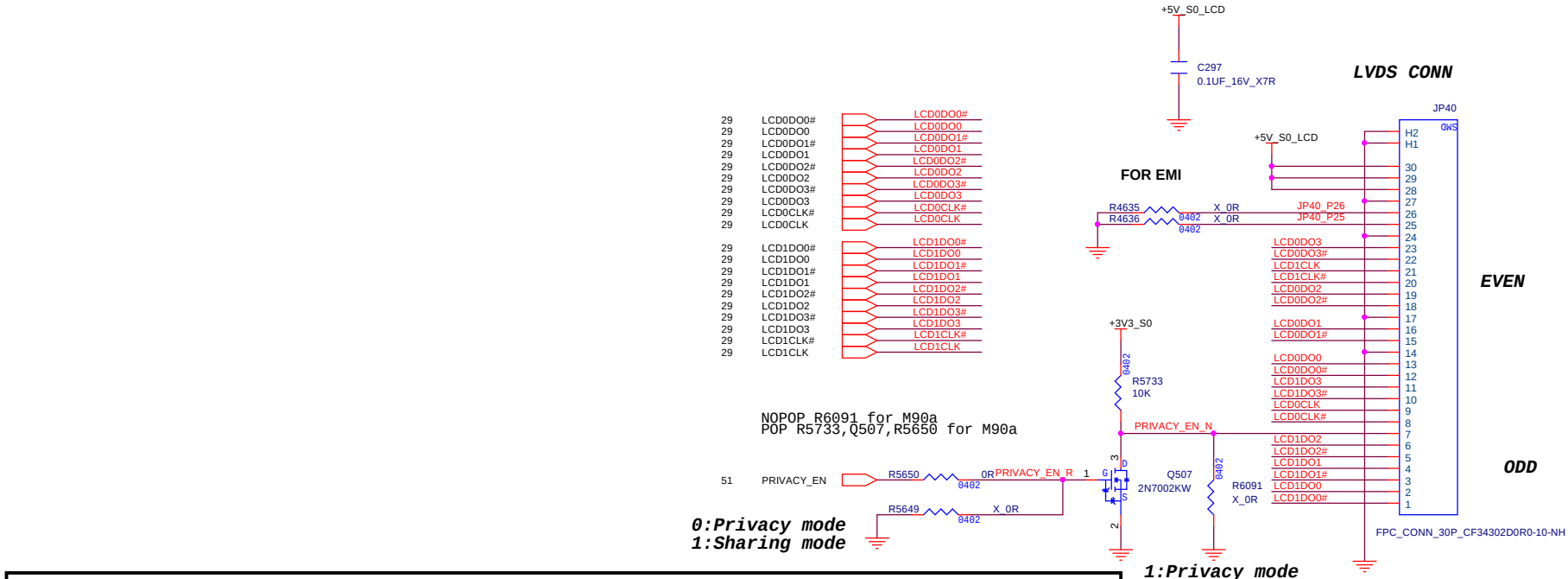
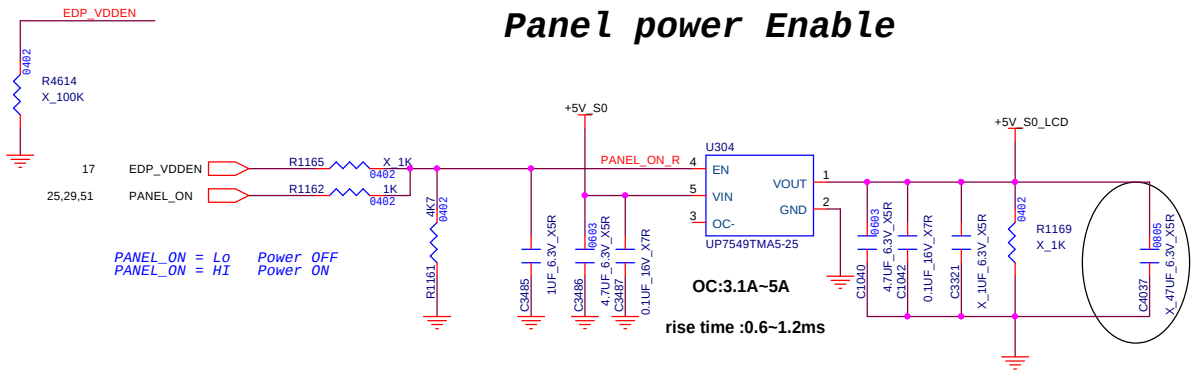
Universal Scientific Industrial Co., Ltd.		
TITLE: M90a/M838z BLANK		REV: V0.3
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A2	Date: Wednesday, January 15, 2020	PAGE: 28 of 99


100 ohm
LVDS OUTPUT
EVEN
LVDS OUTPUT
ODD
CFG1 CFG0 MODE
0 0 X
0 1 EP MODE
1 0 ROM_ONLY_MODE
1 1 EEPROM MODE
RTD2136N-CG
U254
PREVENT DRIVING HPD IN POWER OFF
shielding with ground
VCCK_V12 W=20mils
Power OUT
W=40mils
<200mil
NVRAM
I2C address=0xA8
EEPROM
AT24C64D-SSHM-T
M24C64-WMN6TP
M90a_V0.3_RTD2136N_SSCG=0.75%_201911121445-CS-D7D6.bin
M838z_V0.3_RTD2136N_SSCG=0.75%_201911121445-CS-D7D6.bin
Universal Scientific Industrial Co., Ltd.
TITLE: M90a/M838z RTD2136N-CG CONVERTER
REV: V0.3
Document Number : <Doc>
Prepared by : KERRY HUANG
SIZE : A3
Date: Wednesday, January 15, 2020
PAGE: 29 of 99



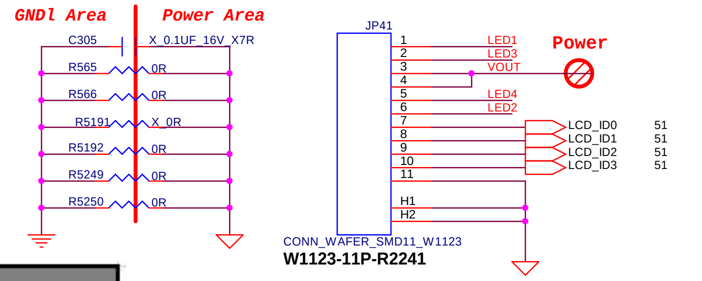
Panel power Enable



LM238WF2(NON-TOUCH) :Imax: 0.762A
LM238WF5(TOUCH) :Imax: 0.788A
LTM238HL06 NON-TOUCH) :Imax: 0.715A
M238HCR(NON-TOUCH)-EP :Imax: 0.948A

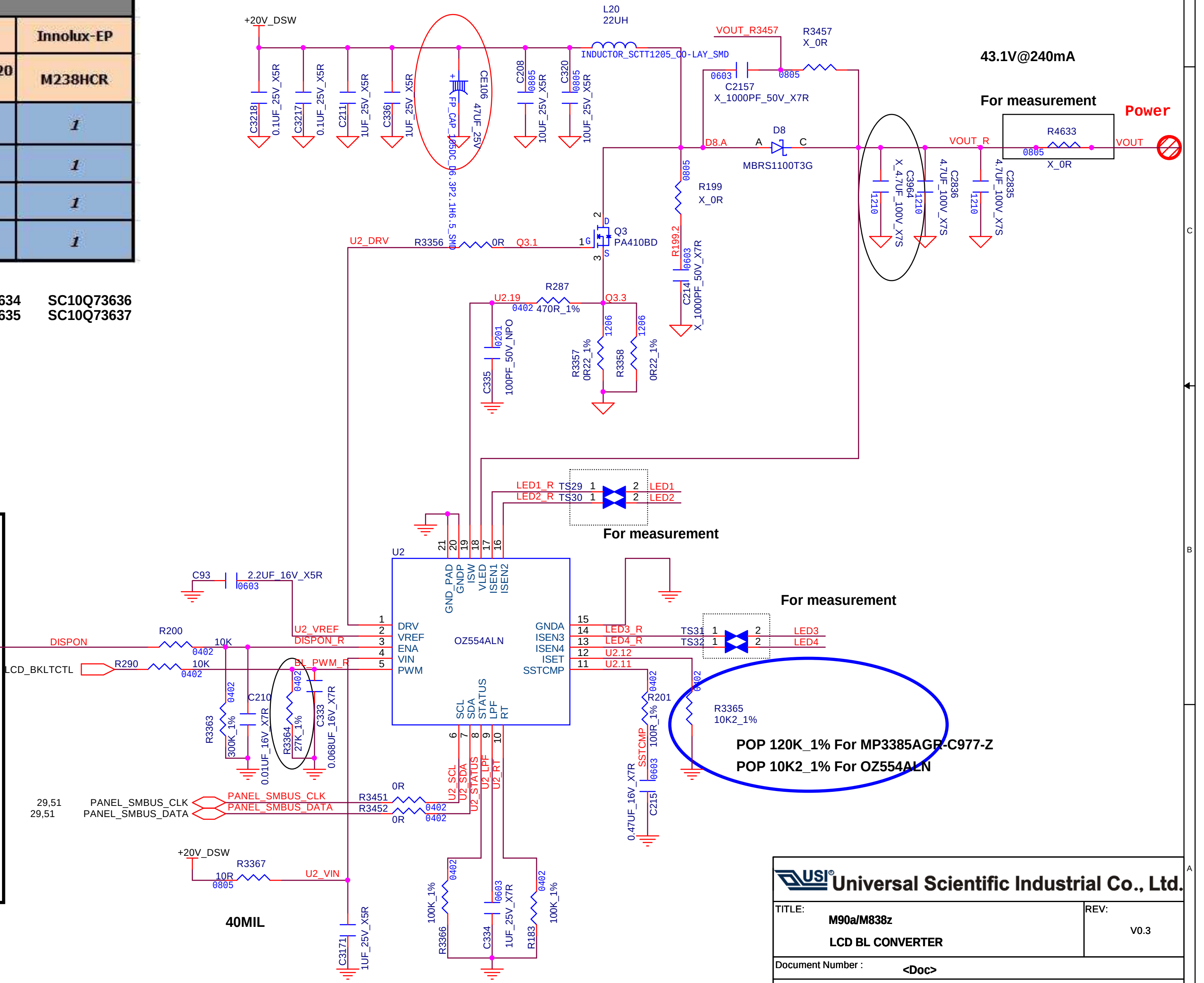
Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z LVDS CONN			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Sunday, January 19, 2020	PAGE: 30 of 99	

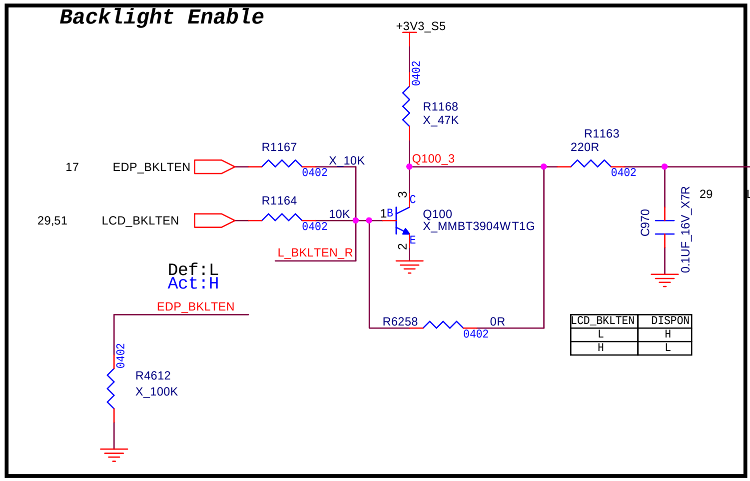
Panel Backlight Brightness Control



AIO Panel ID Definition					
		LG Non-Touch	LG Touch	BOE	Innolux-EP
Cable PN	SIO GPIO	LM238WF2-SSM1 ES8.0	LM238WF5	MV238FHM-N20 ES8.0	M238HCR
PIN 7	GPIO76 - LCD_ID0	0	0	1	1
PIN 8	GPIO75- LCD_ID1	1	1	1	1
PIN 9	GPIO74- LCD_ID2	1	1	1	1
PIN 10	GPIO73- LCD_ID3	0	1	0	1

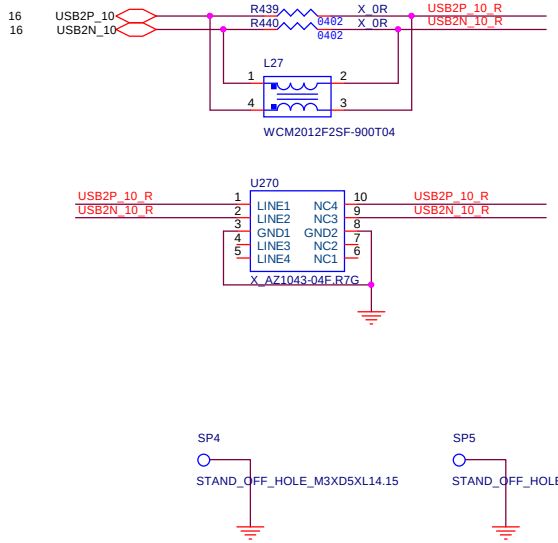
SC10Q73638 SC10Q73639 | SC10Q73640 SC10Q73641 | SC10Q73634 SC10Q73635 | SC10Q73636 SC10Q73637

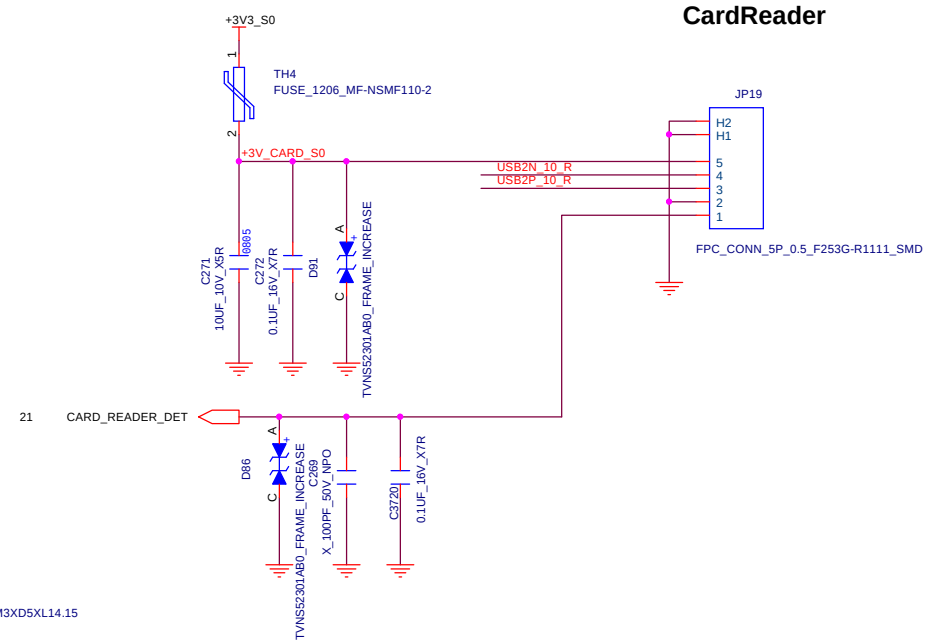




USI Universal Scientific Industrial Co., Ltd.	
TITLE: M90a/M838z LCD BL CONVERTER	REV: V0.3
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3 Date: Monday, January 20, 2020	PAGE: 31 of 99

CardReader





CR STAND-OFF
A,B BOM:48-957728-03
C BOM: 48-957728-02

www.teknisi-indonesia.com

Universal Scientific Industrial Co., Ltd.		
TITLE: M90a/M838z CARD READER HD		REV: V0.3
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 32 of 99

SATA CONN

SATA 3.0

PDG:2"~6"

SP7

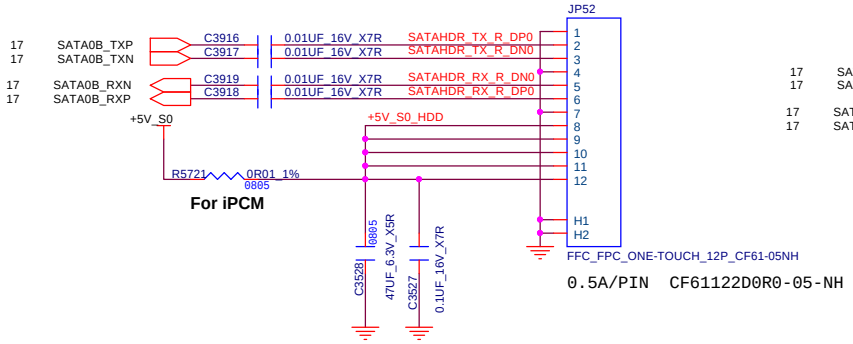
SP10

STAND_OFF_HOLE_D6XL1.5_0.8_8.45

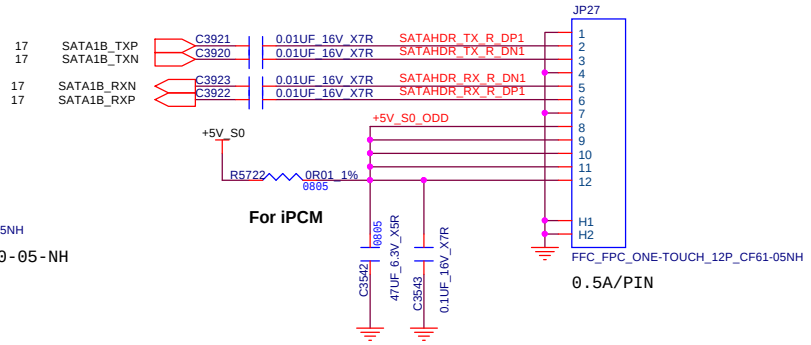
STAND_OFF_HOLE_D6XL1.5_0.8_8.45

HDD STAND-OFF 48-957747-01

HDD



ODD



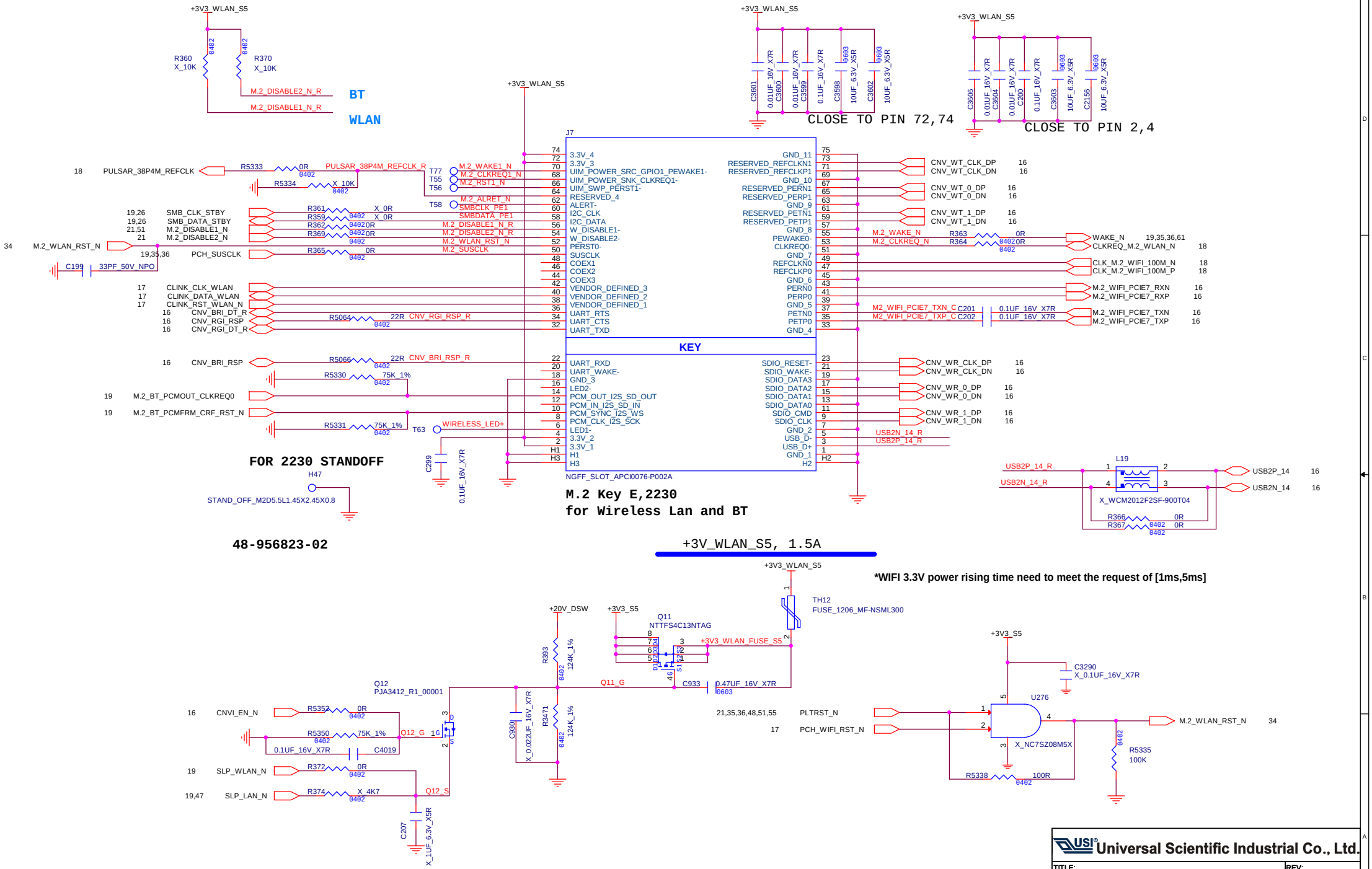
	2.5" HDD			3.5" HDD		
	Spin up Max Current(A)	Normal Working Max Current(A)	Voltage Tolerance	Spin up Max Current(A)	Continuous R/W (50%) Current(A)	Voltage Tolerance
12V	-	-	-	2.8	0.85	±10%
5V	1.1	0.5	±5%	1	0.7	±5%

	Slim ODD(Super Multi)			HH ODD		
	Start up Max Current(A)	Normal Working Max Current(A)	Voltage Tolerance	Start up Max Current(A)	Normal Working Max Current(A)	Voltage Tolerance
12V	-	-	-	2.5	2.5	±10%
5V	2.5	1.2	±5%	2	1.6	±5%

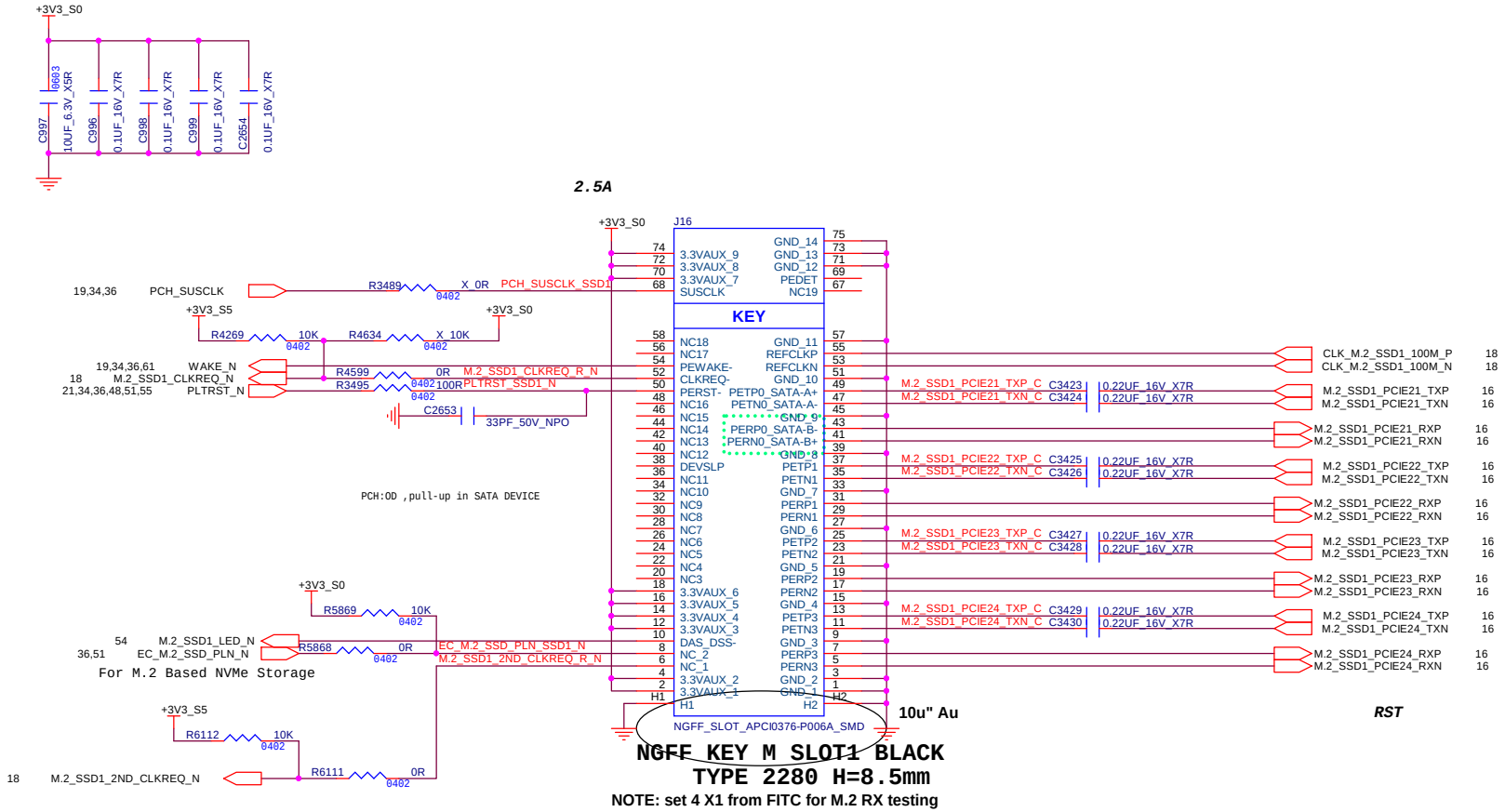
	2.5" SSD			M.2 SSD		
	Start with in-rush Current(A)	Read/Write Max Current(A)	Voltage Tolerance	Start with in-rush Current(A)	Read/Write Max Current(A)	Voltage Tolerance
5V	1.6	1.6	±5%,(-8% at startup)	-	-	-
3.3V	-	-	-	2.5	2.5	±5%,(-8% at startup)

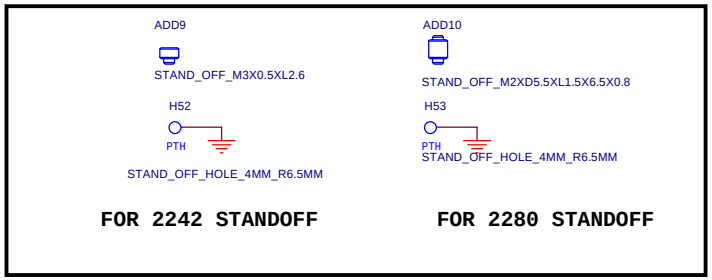
Universal Scientific Industrial Co., Ltd.

TITLE: M90a/M838z SATA 3.0 CONN		REV: V0.3
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 33 of 99



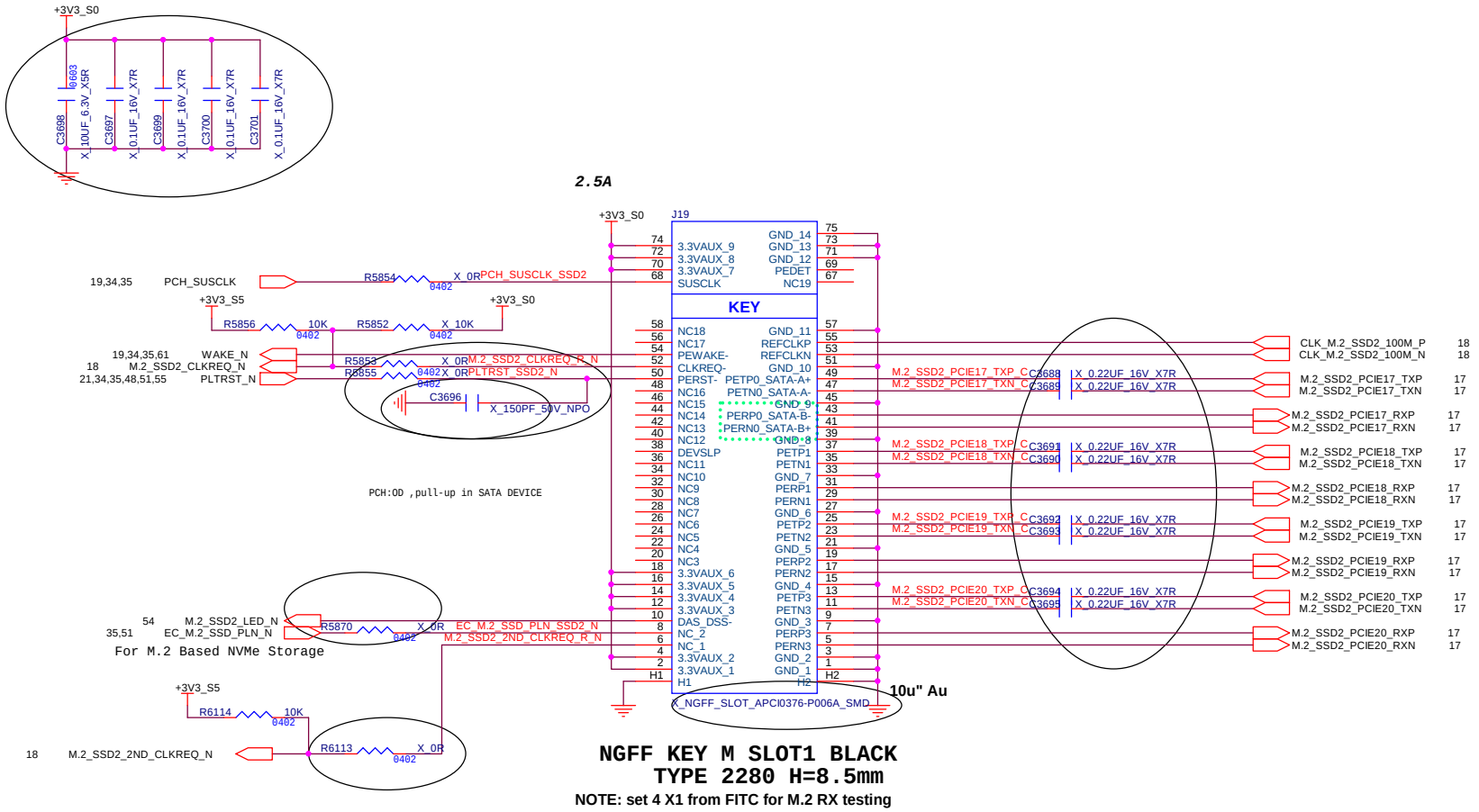
Universal Scientific Industrial Co., Ltd.	
TITLE: M90a/M838z M.2 Socket-WLAN	REV: V0.3
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Wednesday, January 15, 2020
PAGE: 34 of 99	



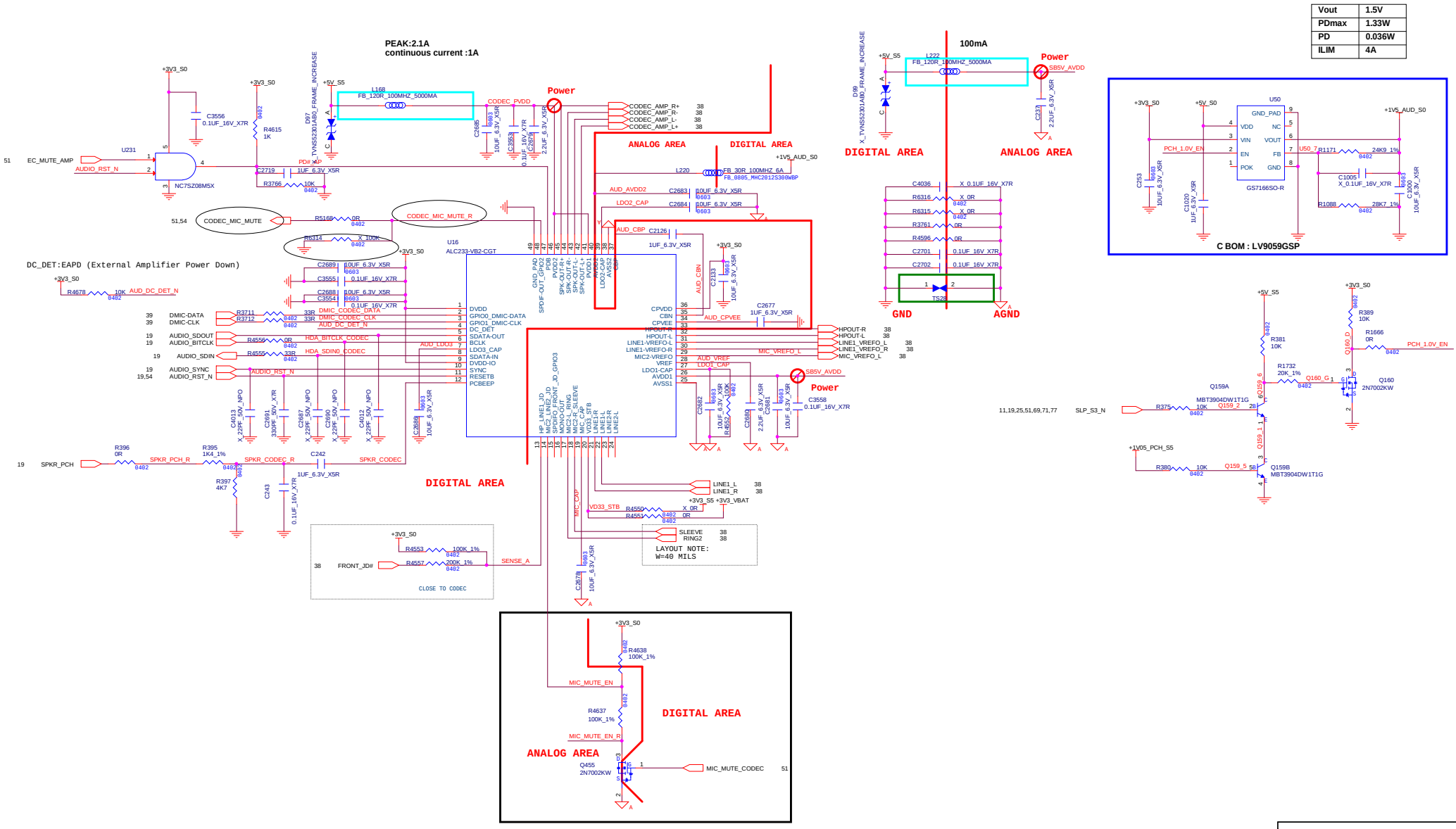


Universal Scientific Industrial Co., Ltd.

TITLE: M90a/M838z M.2 SOCKET-SSD1		REV: V0.3
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 35 of 99



Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z M.2 SOCKET-SSD2			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 36 of 99	

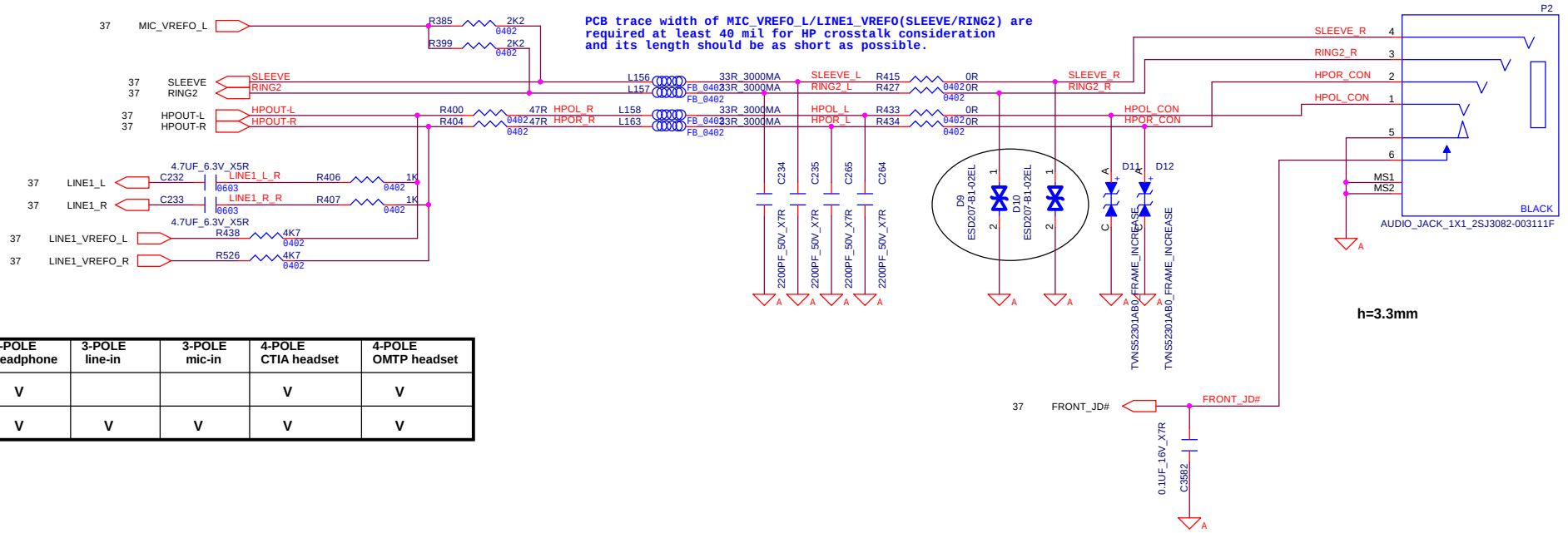


Vout	1.5V
PDmax	1.33W
PD	0.036W
ILIM	4A

Universal Scientific Industrial Co., Ltd.

TITLE:	M90a/M838z AUDIO CODEC ALC233	REV: V0.3
Document Number :	<Doc>	
Prepared by :	KERRY HUANG	
SIZE : Custom	Date: Friday, January 17, 2020	PAGE: 37 of 99

Combo Audio Jack

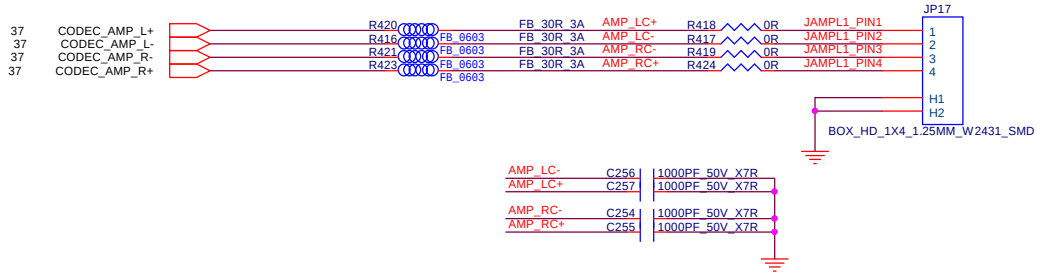


	3-POLE headphone	3-POLE line-in	3-POLE mic-in	4-POLE CTIA headset	4-POLE OMTP headset
GHS	V			V	V
UAJ	V	V	V	V	V

4Ω +-15%
Rated Power :3W
Max. Power:5W

Required at least 40 mil

SPEAKER

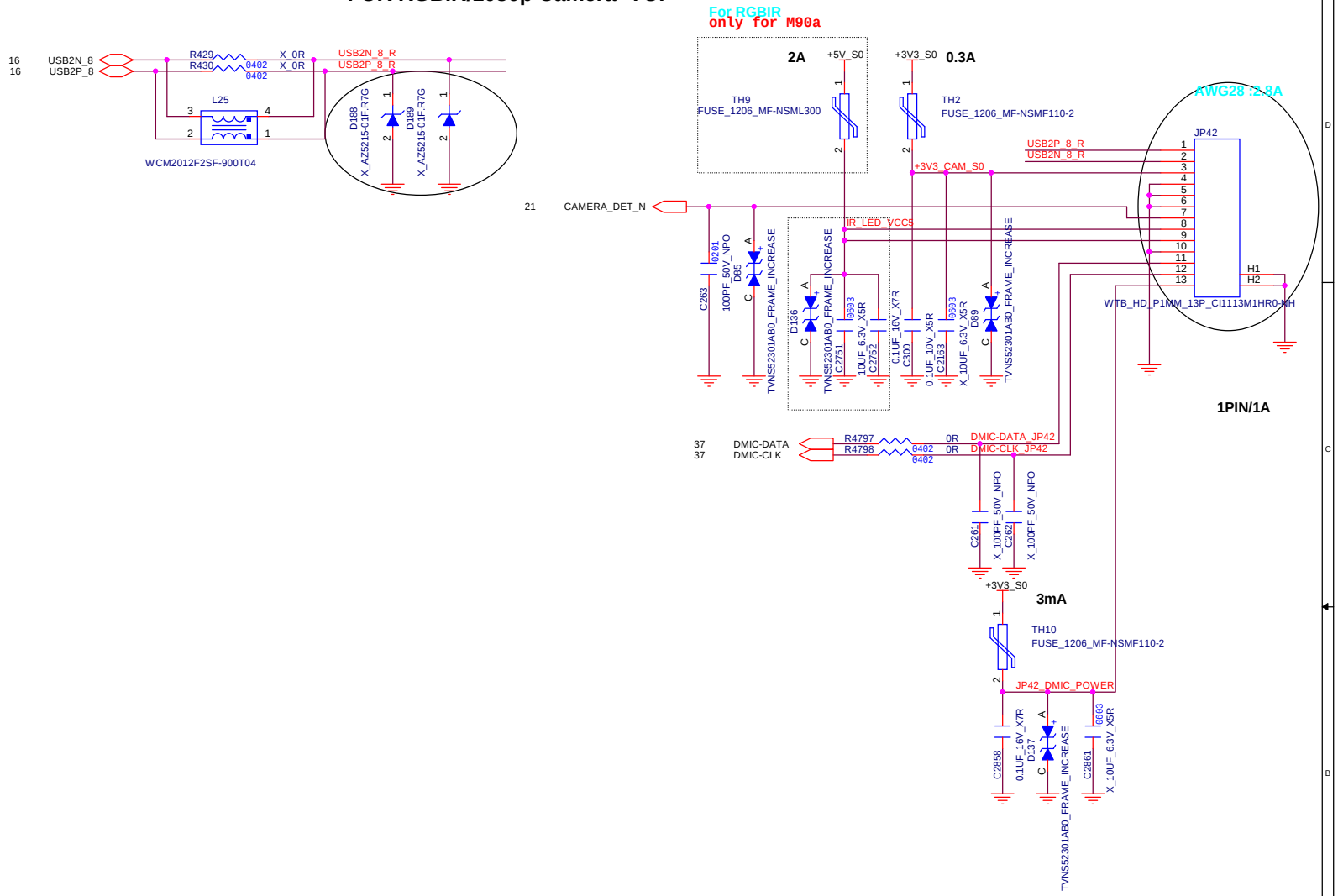


AMP_LC-	C256	1000PF_50V_X7R
AMP_LC+	C257	1000PF_50V_X7R
AMP_RC-	C254	1000PF_50V_X7R
AMP_RC+	C255	1000PF_50V_X7R

Universal Scientific Industrial Co., Ltd.

TITLE: M90a/M838z AUDIO JACK			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Thursday, January 16, 2020		PAGE: 38 of 99

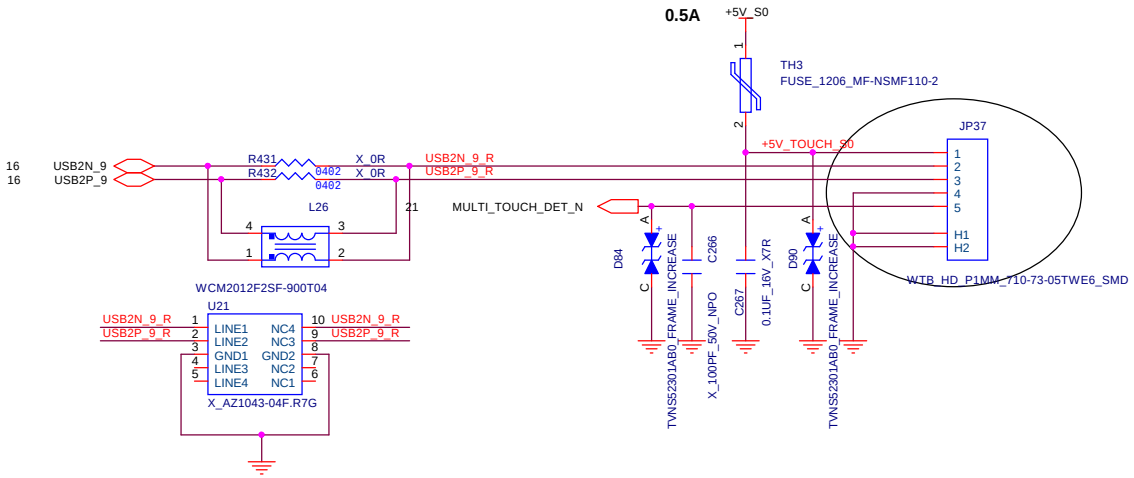
FOR RGBIR/1080p Camera -TOP



Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z RGBIR_HD			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020		PAGE: 39 of 99

Multi-Touch

only for M90a



Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z TOUCH_HD			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 40 of 99	

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Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z BLANK			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 41 of 99	

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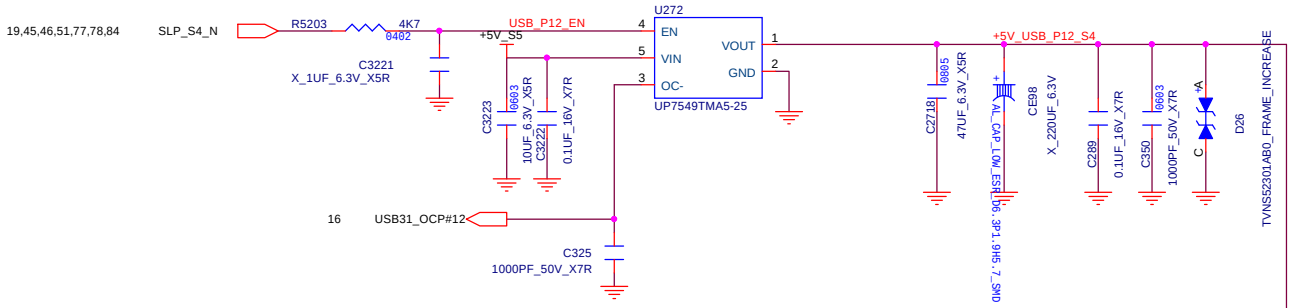
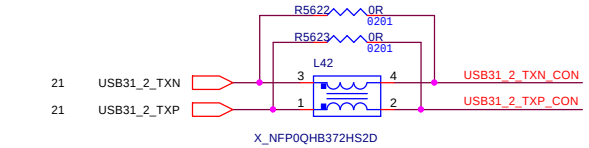
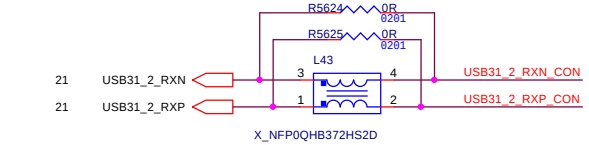
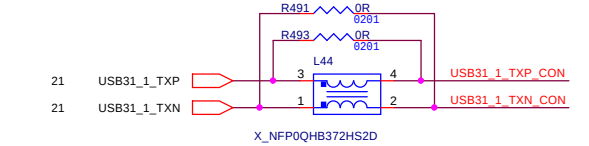
Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z BLANK			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 42 of 99	

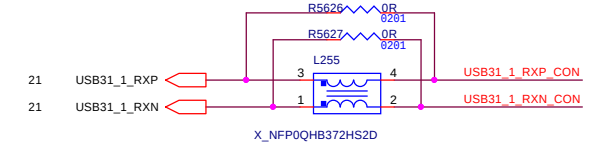


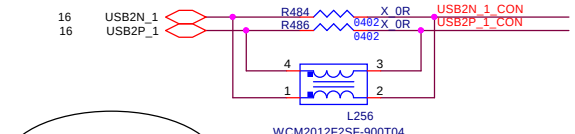
up7549 co-lay with AX87X3B
co-lay TPS2001D & LV9742 & GS7632& APL3553

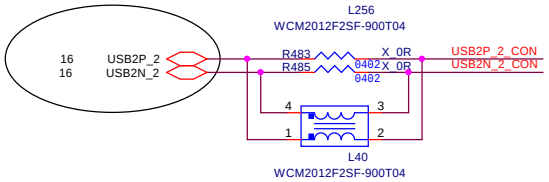


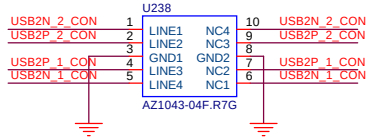


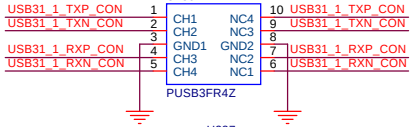


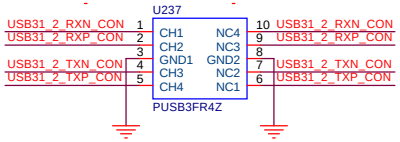




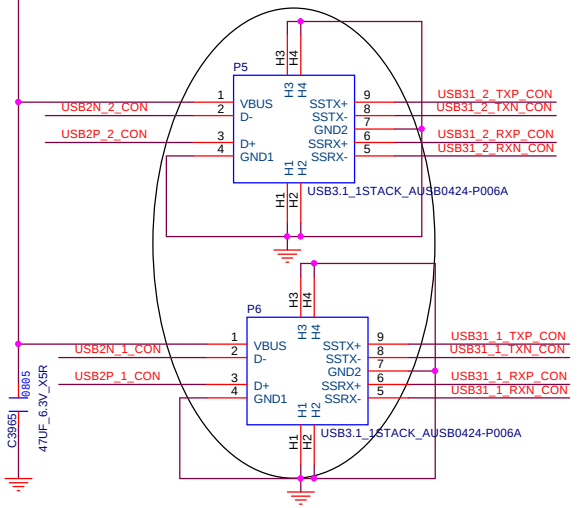






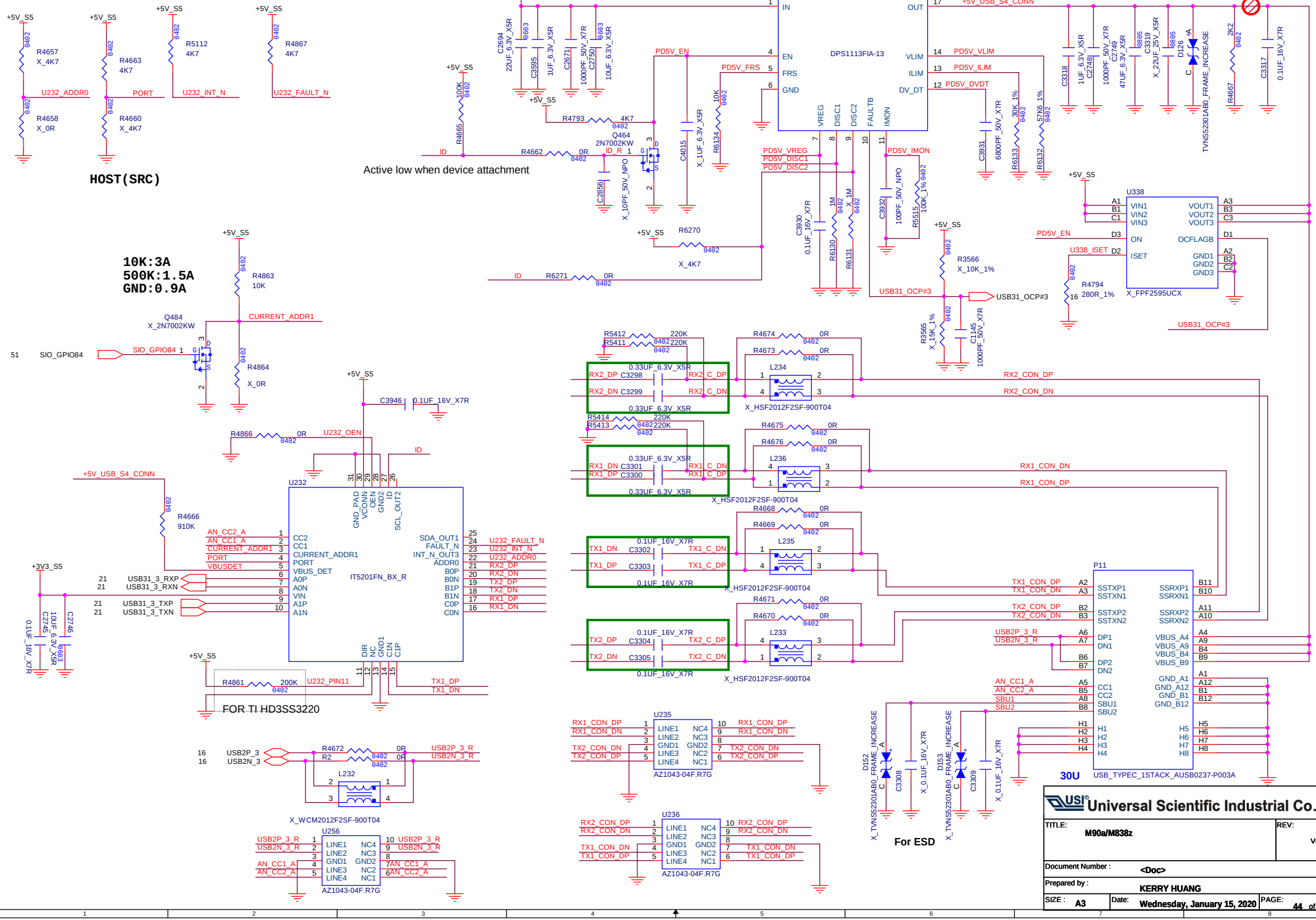


Tongue Color:USB3.1 Gen2 BLACK

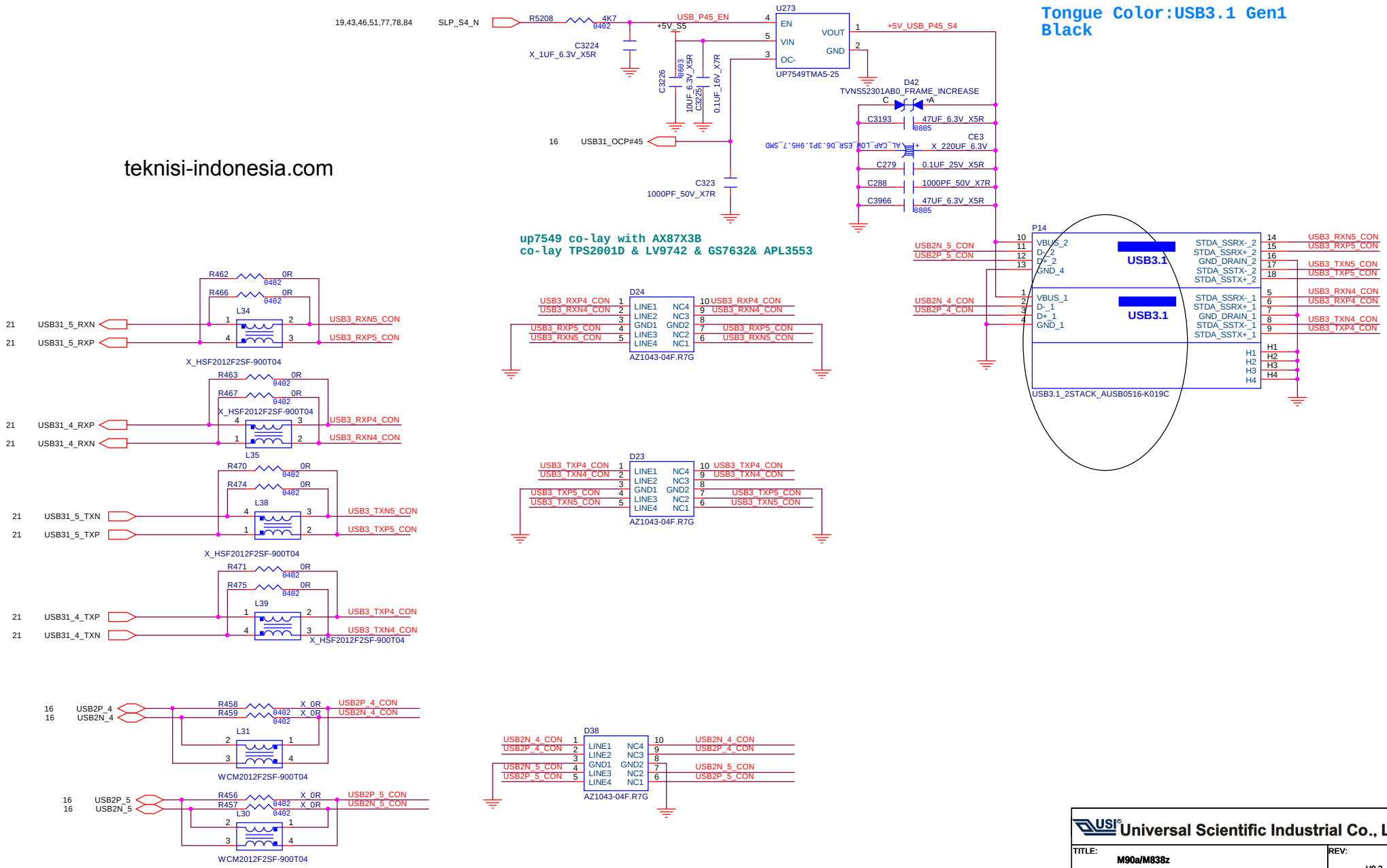


Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z SIDE USB3.1 G2 PORTX2			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 43 of 99	

USB TYPE-C CONN



REAR USB3.0 X 4



Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z REAR USB3.1 G1 PORTX2		REV: V0.3	
Document Number :			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 45 of 99	

WL_CHARGER_EN

	ENABLE WL_CHARGER_EN (DEFAULT)	DISENABLE WL_CHARGER_EN
S0~S4	1	1
S4~S5	1	0

USB_PO_EN

	ENABLE USB POWER ON (DEFAULT)	DISENABLE USB POWER ON
S0~S4	1	1
S4~S5	1	0

POP FOR WL_CHARGER

POP FOR WL_CHARGER

POP FOR WL_CHARGER

POP 100K FOR WL_CHARGER

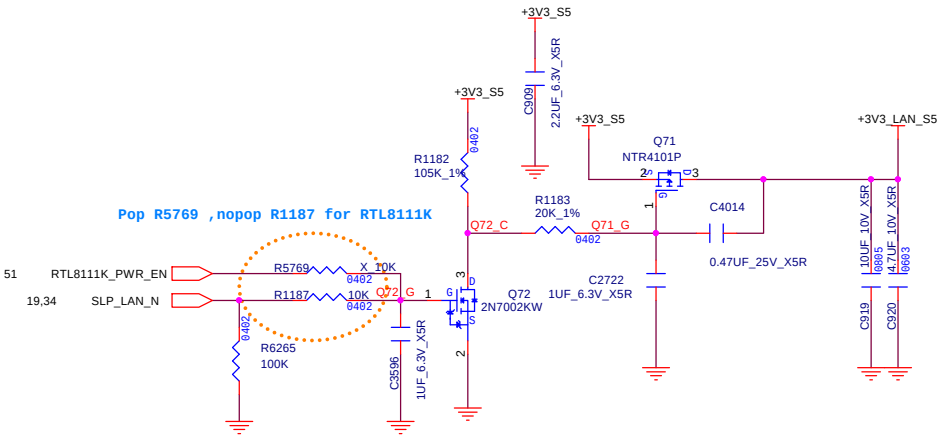
Tongue Color:USB3.1 Gen1 Black

USB POWER ON
(Key ALT+P to power on system)

USB Debug

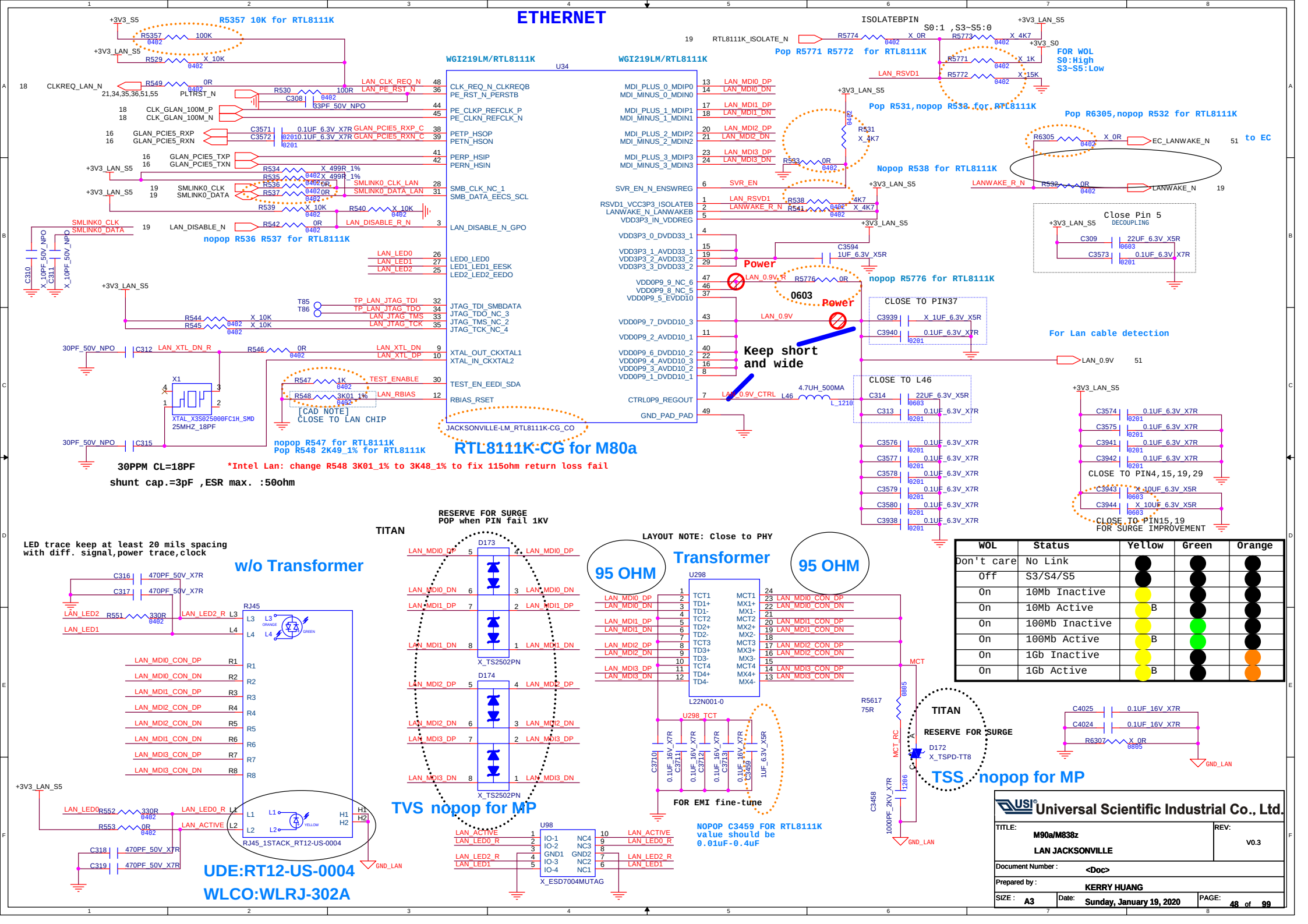
TITLE:	M90a/M838z REAR USB3.1 G1 PORTX2
REV:	V0.3
Document Number :	<Doc>
Prepared by :	KERRY HUANG
SIZE :	A3
Date:	Wednesday, January 15, 2020
PAGE:	46 of 99

Universal Scientific Industrial Co., Ltd.



Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z +3V3_LAN_S5			REV: V0.3
Document Number :			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 47 of 99	

ETHERNET



WOL	Status	Yellow	Green	Orange
Don't care	No Link	●	●	●
Off	S3/S4/S5	●	●	●
On	10Mb Inactive	●	●	●
On	10Mb Active	B	●	●
On	100Mb Inactive	●	B	●
On	100Mb Active	B	B	●
On	1Gb Inactive	●	●	B
On	1Gb Active	B	●	B

Universal Scientific Industrial Co., Ltd.

TITLE: M90a/M838z
LAN JACKSONVILLE

REV: V0.3

Document Number : <Doc>

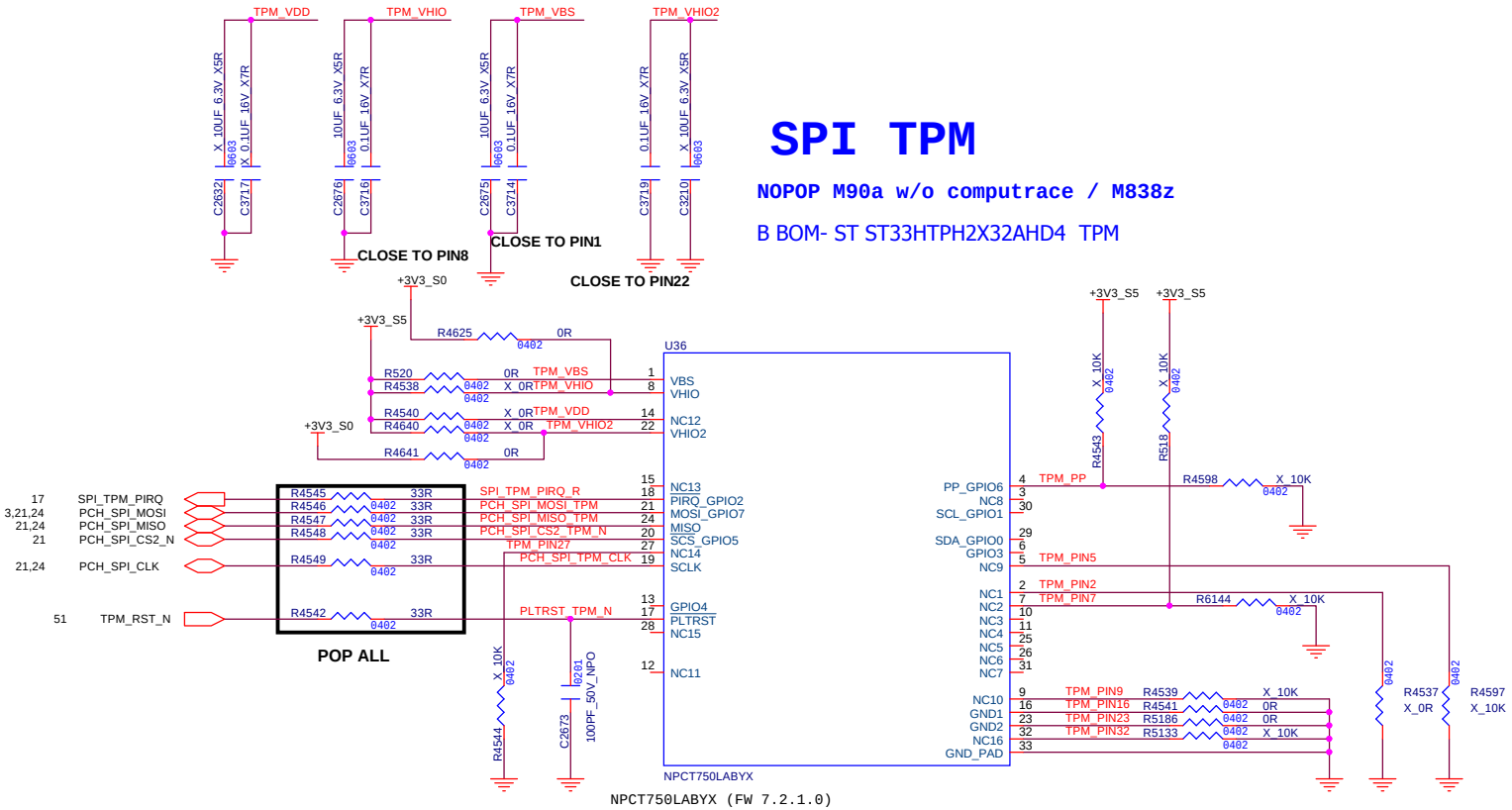
Prepared by : KERRY HUANG

SIZE : A3 | Date: Sunday, January 19, 2020 | PAGE: 48 of 99

SPI TPM

NOPOP M90a w/o computrace / M838z

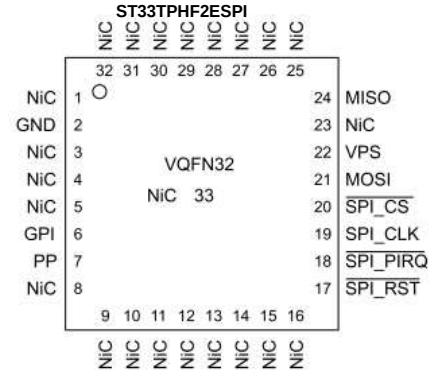
B BOM- ST ST33HTPH2X32AHD4 TPM

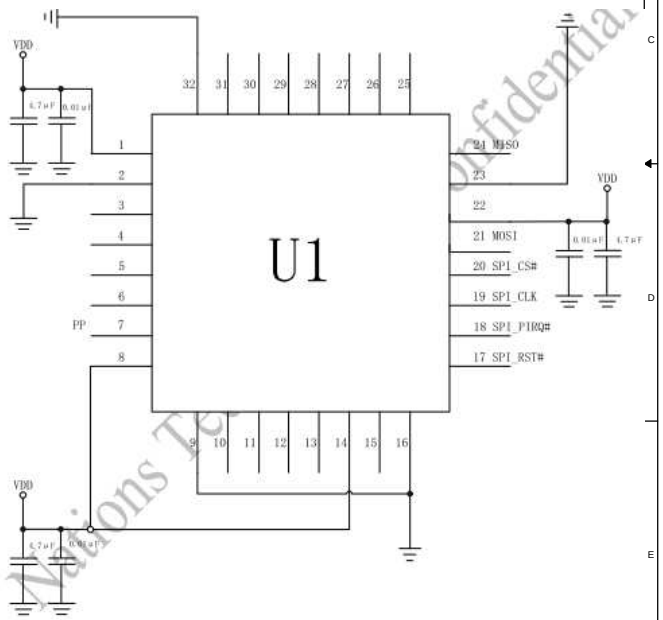


NPCT750LABYX (FW 7.2.1.0)

ST ST33HTPH2X32AHD4 (FW75.00)

NationZ Z32H330TC(FW 7.51)





	STUFF	EMPTY
NPCT750LAAYX	R520,R4541,R4625,R4641,C2673	R518,R4543,R4537,R4597,R4598,R4539,R5133,R4640,R4540, R4538,R4544,C3717,C2632
ST33TPHF2ESPI	R4537,R5133,R4640,C2673,C3210	R4625,R520,R4543,R518,R4538,R4539,R4540,R4541,R4544 ,C2632,CB162,C2676,CB161,C2675,CB101,R4597,R4598,R4641,R5186,R5133
Z32H330TC	R520,C2675,C3714,R4537,R4538,C2676, C3716,R4537(0R),R4540,R4541,C2673, R4640,C3210,C3719,R5186,R5133(0R), C2632,C3717	R4543,R4598,R4597,R518,C2632,C3717,R4544

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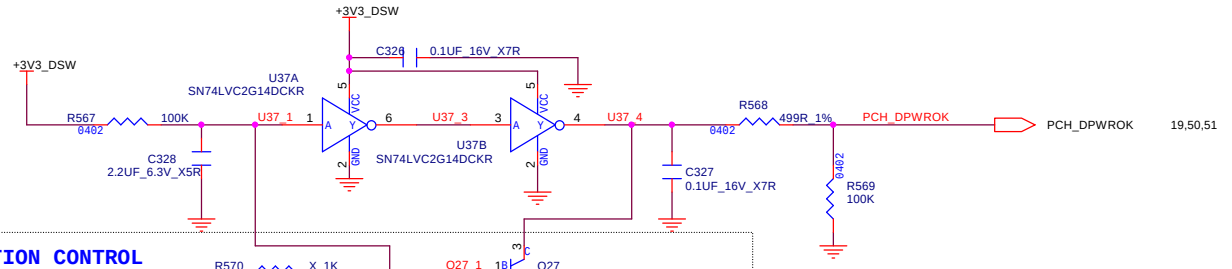
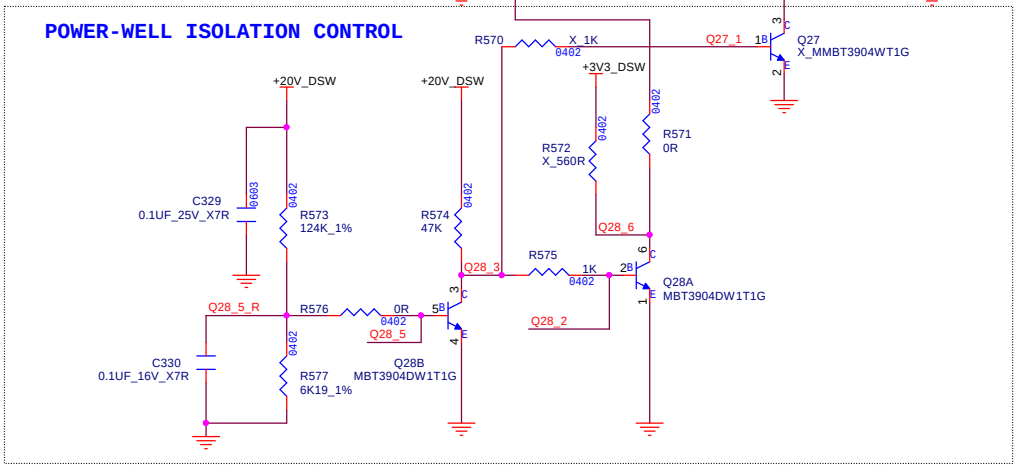
TITLE: M90a/M838z TPM		REV: V0.3
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 49 of 99

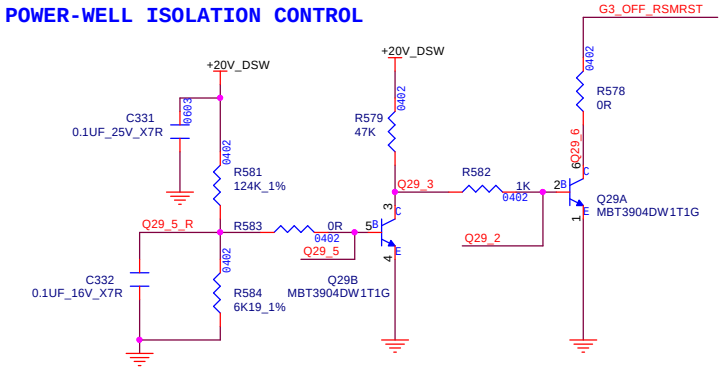
DPWROK LOGIC

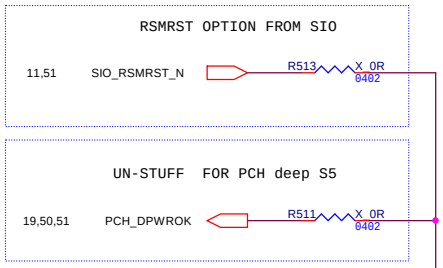


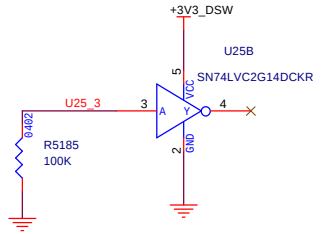
POWER-WELL ISOLATION CONTROL



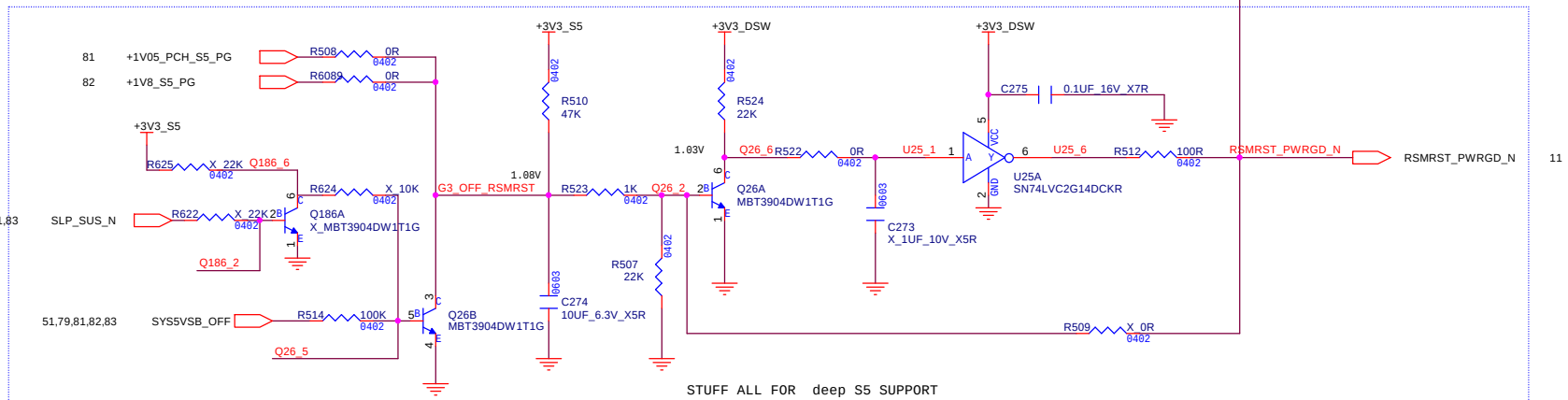
POWER-WELL ISOLATION CONTROL



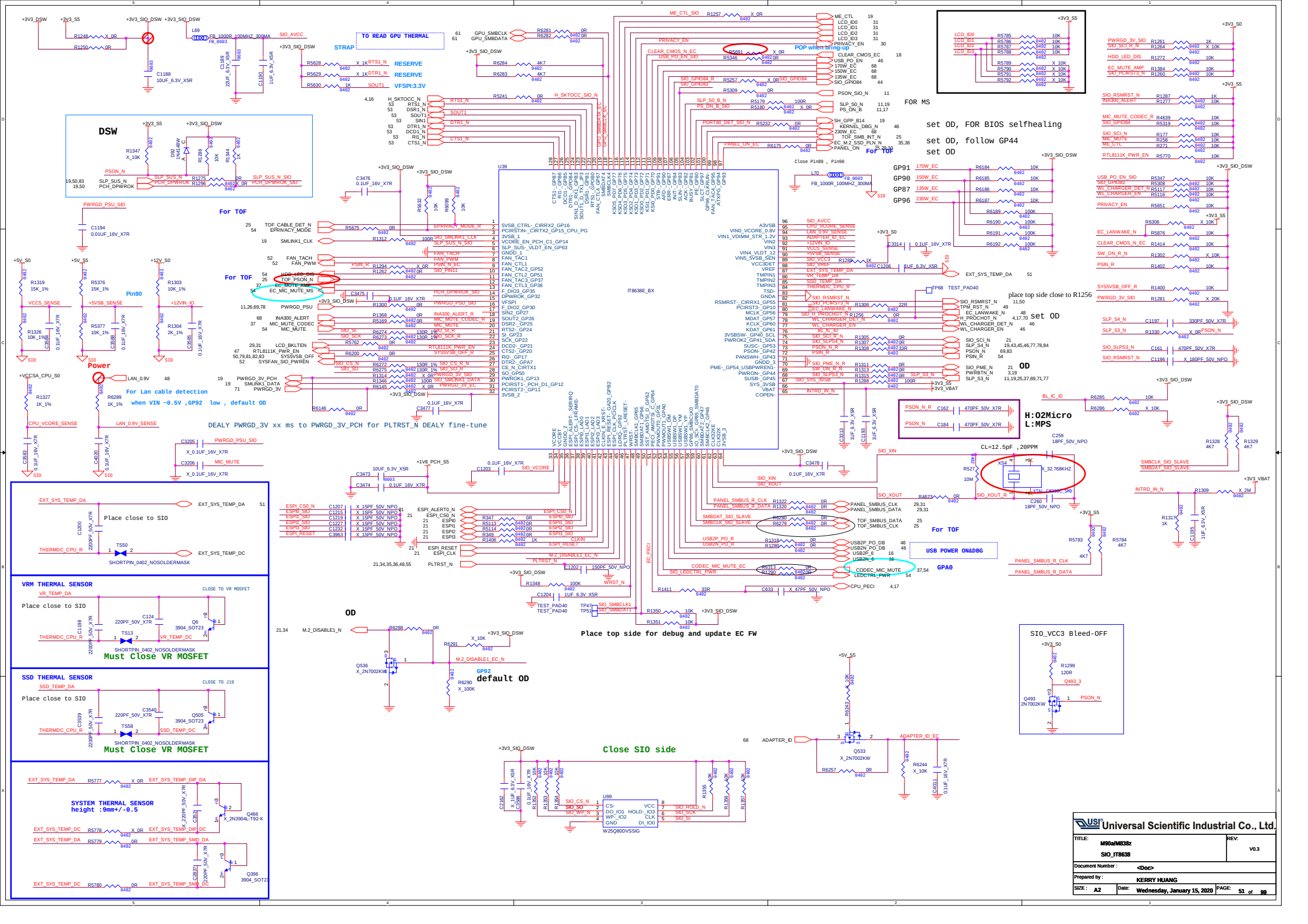




RSMRST LOGIC

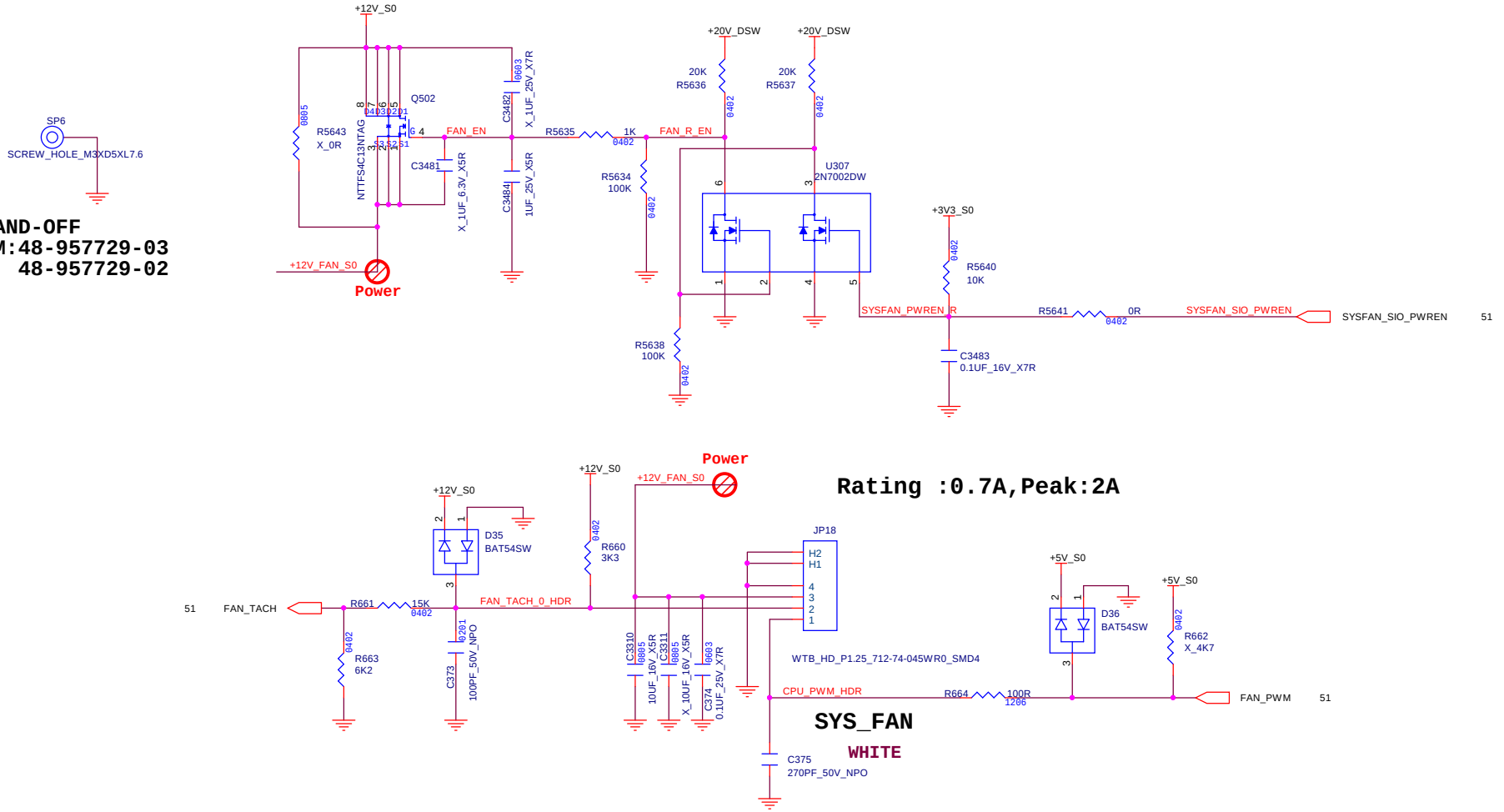


Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z RSMRST LOGIC			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 50 of 99	


DSW
TO READ GPU THERMAL
STRAP
RESERVE
RESERVE
VFSPI:3.3V
FOR MS
set OD, FOR BIOS selfhealing
set OD, follow GP44
set OD
For TOF
For TOF
For TOF
For TOF
Pin90
Power
For Lan cable detection
when VIN ~0.5V ,GP92 low , default OD
DEALY PWRGD_3V xx ms to PWRGD_3V_PCH for PLTRST_N DEALY fine-tune
place top side close to R1256
Set OD
OD
H:O2Micro
L:MPS
CL=12.5pF ,20PPM
POP when bring-up
Close Pin89 , Pin90
Close SIO side
Place top side for debug and update EC FW
default OD
GP92
Place close to SIO
Place close to SIO
Place close to SIO
VRM THERMAL SENSOR
Must Close VR MOSFET
SSD THERMAL SENSOR
Must Close VR MOSFET
SYSTEM THERMAL SENSOR
height :9mm+/-0.5
SIO_VCC3 Bleed-OFF
USB POWER ON&DBG
GPA0
OD
Universal Scientific Industrial Co., Ltd.
TITLE: M90a/M838z
SIO_IT8638
REV: V0.3
Document Number : <Doc>
Prepared by : KERRY HUANG
SIZE : A2
Date: Wednesday, January 15, 2020
PAGE: 51 of 99

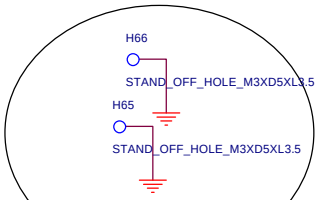
FOR MSB

ONLY FOR M90a UMA

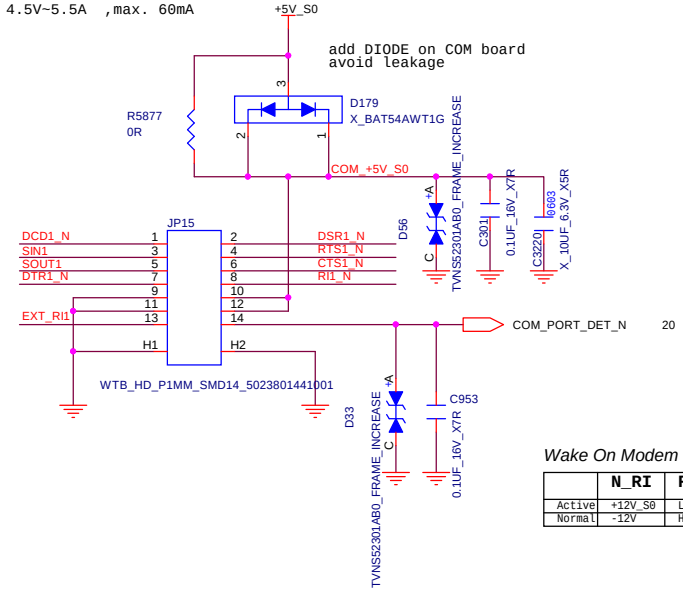


Universal Scientific Industrial Co., Ltd.	
TITLE: M90a/M838z FAN	REV: V0.3
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Wednesday, January 15, 2020
PAGE: 52 of 99	

SERIAL PORT 1

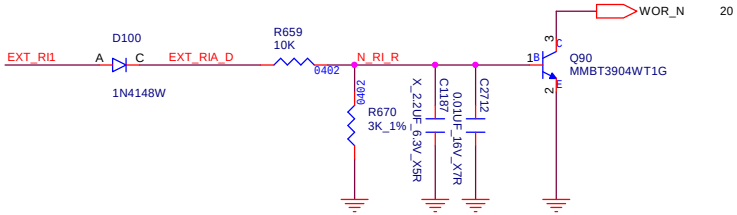


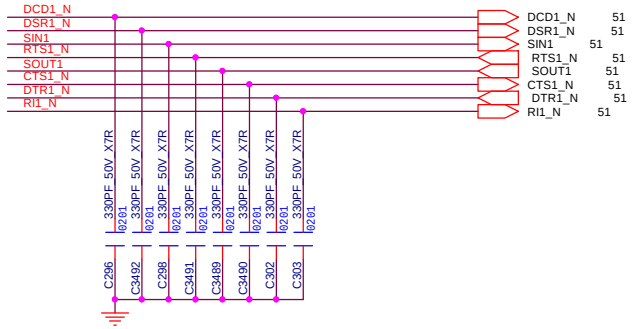
COM STAND-OFF
A,B BOM:48-957751-03
C BOM: 48-957751-02



Wake On Modem Header

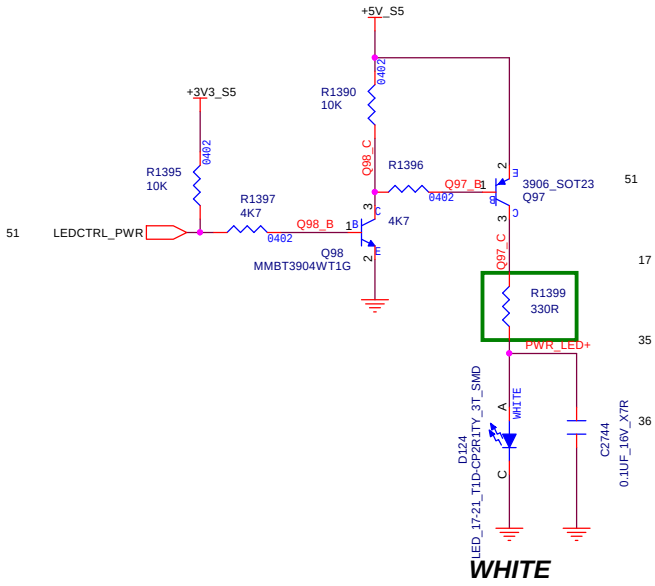
	N_RI	RI#
Active	+12V_S0	Low
Normal	-12V	High





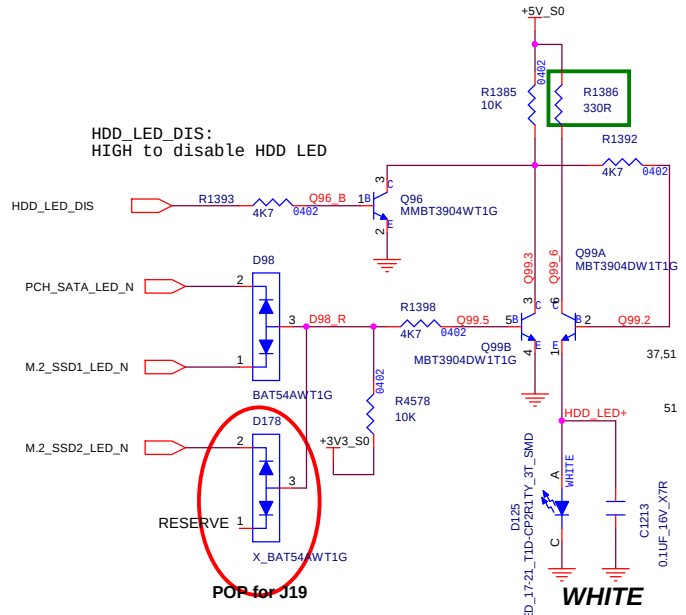
Universal Scientific Industrial Co., Ltd.	
TITLE: M90a/M838z COM	REV: V0.3
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Wednesday, January 15, 2020 PAGE: 53 of 99

Power LED



WHITE

HDD LED

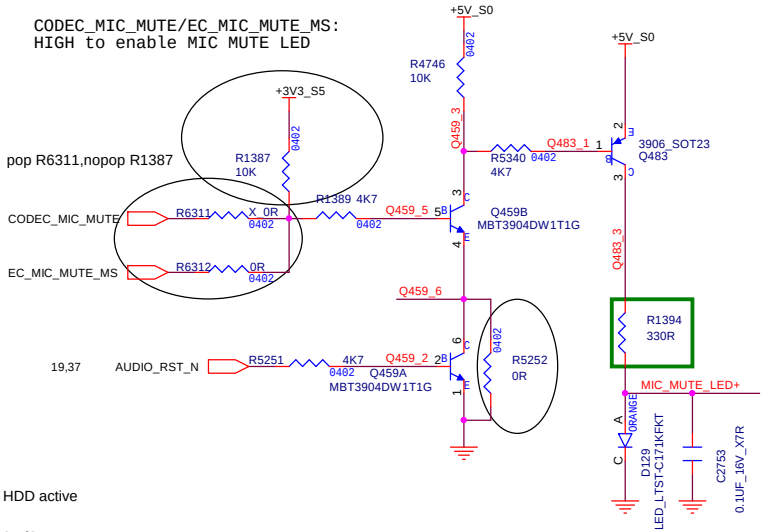


POP for J19

WHITE

HDD LED Behavior: Blink when HDD active

MIC MUTE LED



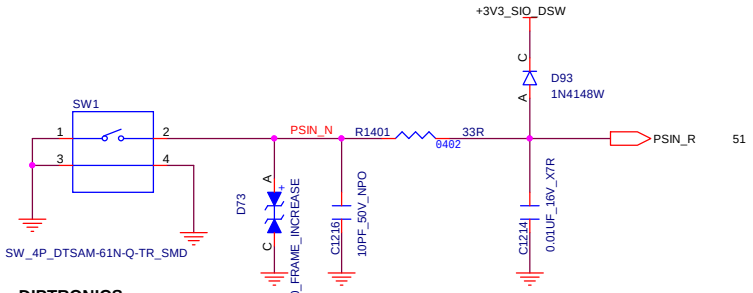
Orange (Amber 611nm)

42-141613-01 - LED GREEN 0805 17-21/G6C-BM1N2B/3T

Power LED Behavior:
- System on: On
- System in Standby
  Gradual 1s On, Gradual 1s OFF, 3s OFF
- Initial Connection of Power (e.g. via AC adaptor or AC-in) Blink 3 Times (0.25 s On/ 0.25 s Off , repeat x 3)
- System entering hibernation Blink (0.25 s On/ 0.25 s Off)
- System off OFF

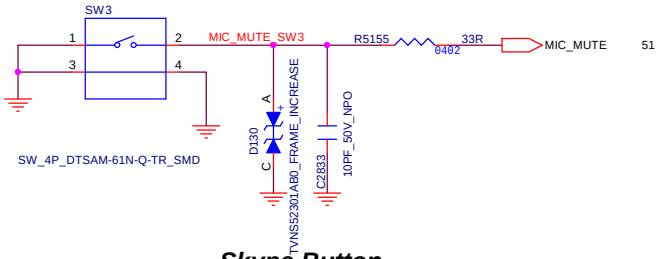
Mic mute LED Behavior:
ON when muted; OFF when un-muted
S3/S4/S5 will be off
Will keep last state when next reboot or re-power on
The shipping default for Mic mute led is off (after preload in MFG, Mic mute is off)

Power Button



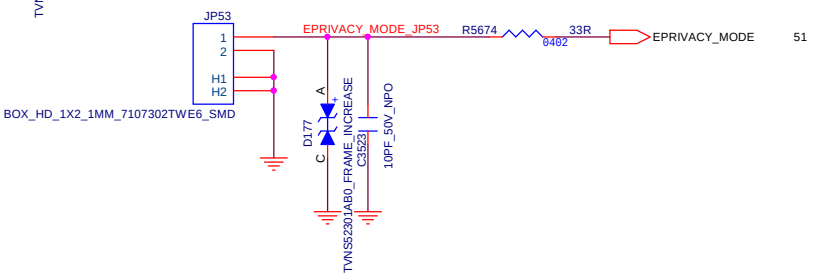
DIPTRONICS

MIC Mute Button



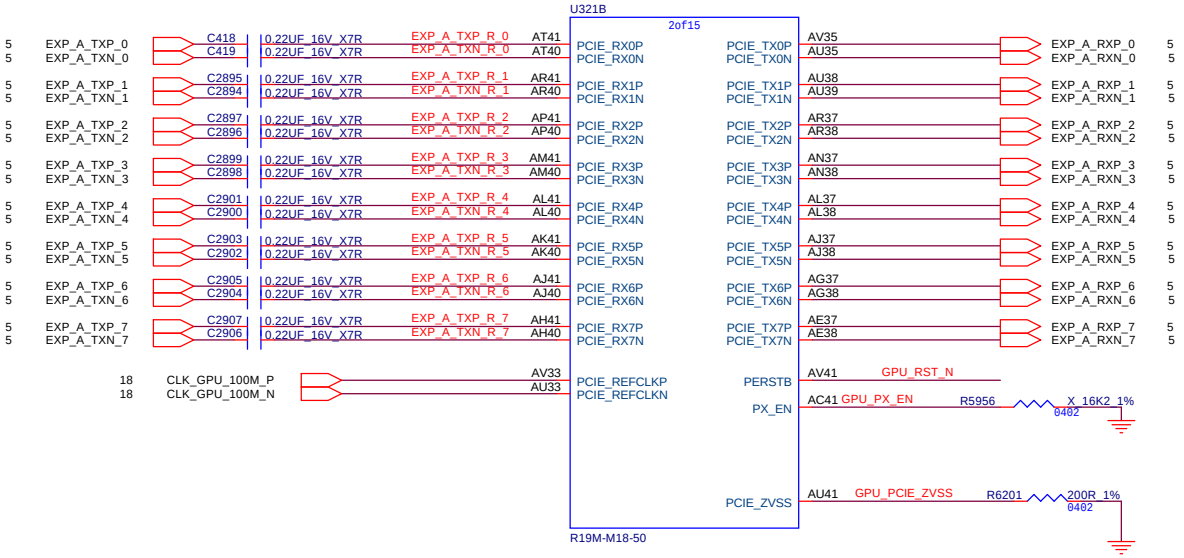
Eprivacy Button HD

ONLY FOR M90a

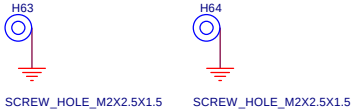


Skype Button

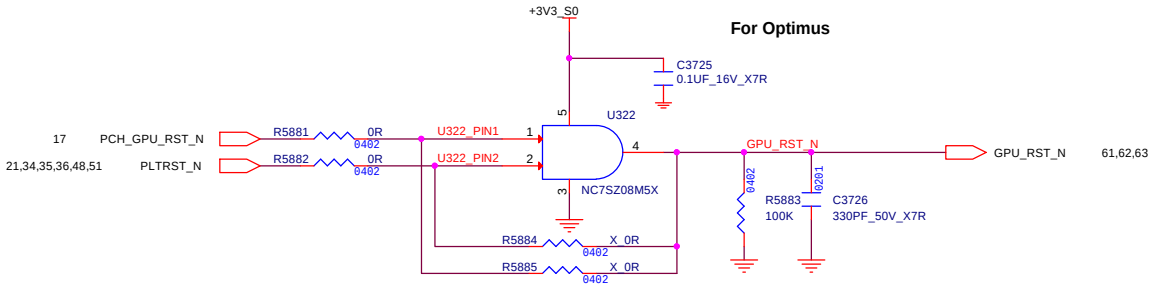
Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z FUNCTION BUTTON			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020		PAGE: 54 of 99



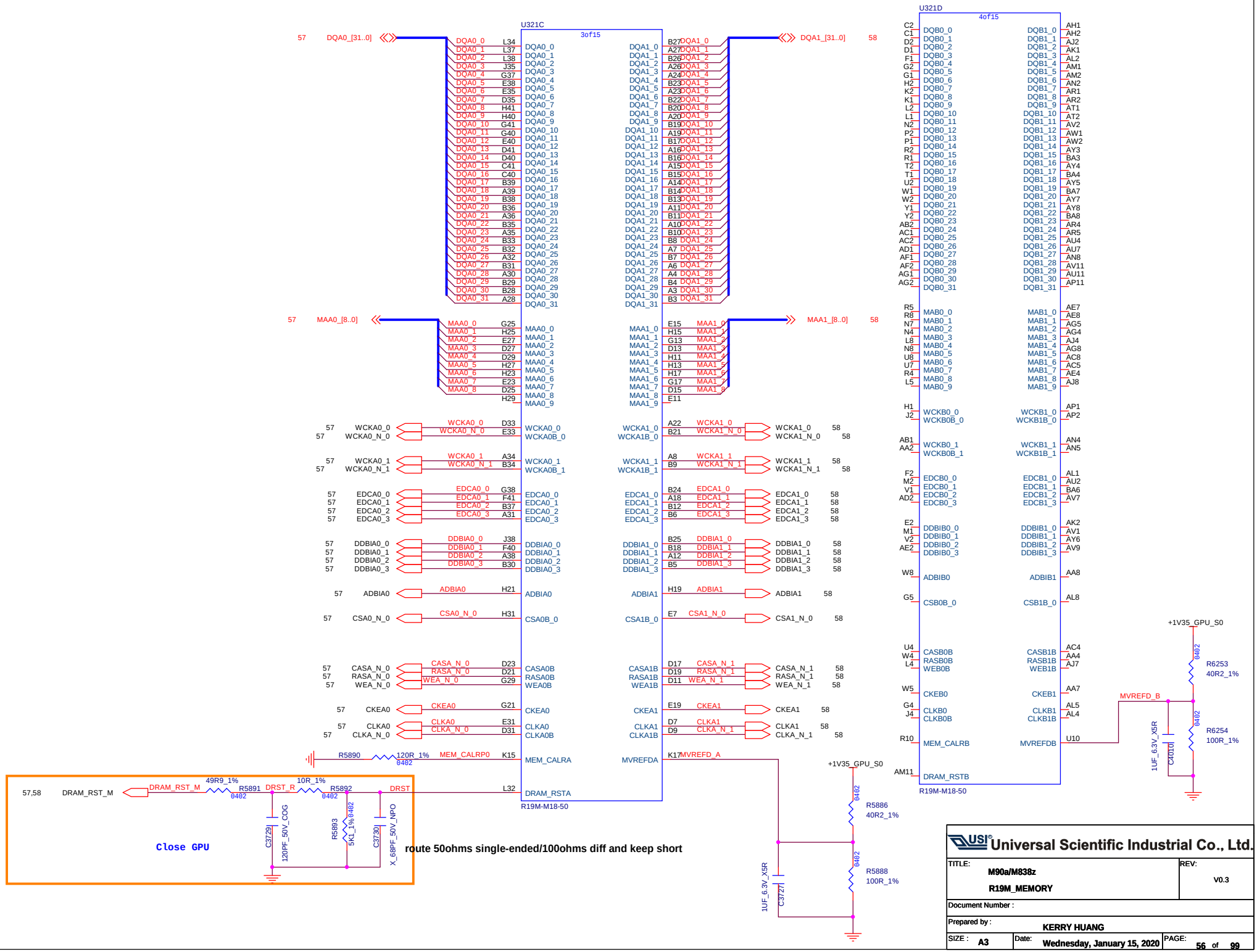
FOR GPU
HEAT PIPE SCREW HOLES



48-956602-01 -SO-RND,M2.0*D4*2.5,CU,SN,hole seal -LONG FEI
48-956602-02 -SO-RND,M2.0*D4*2.5,CU,SN,hole seal -SCREWTECH



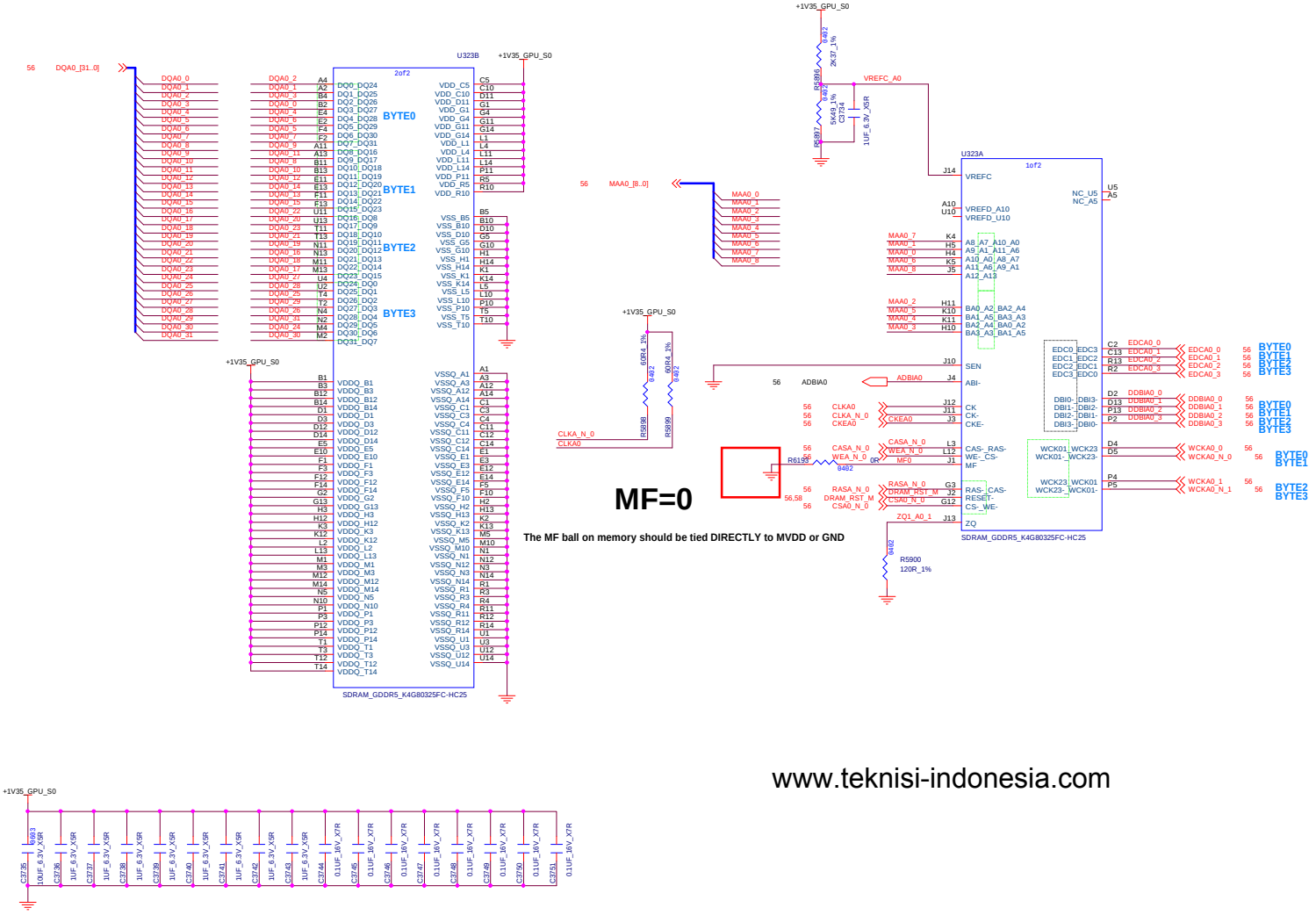
Universal Scientific Industrial Co., Ltd.	
TITLE: M90a/M838z R19M_PCIE	REV: V0.3
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Wednesday, January 15, 2020
PAGE: 55 of 99	



Universal Scientific Industrial Co., Ltd.	
TITLE: M90a/M838z R19M_MEMORY	REV: V0.3
Document Number :	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Wednesday, January 15, 2020
PAGE: 56 of 99	

GDDR5 Memory Channel A x32 mode
MF=0

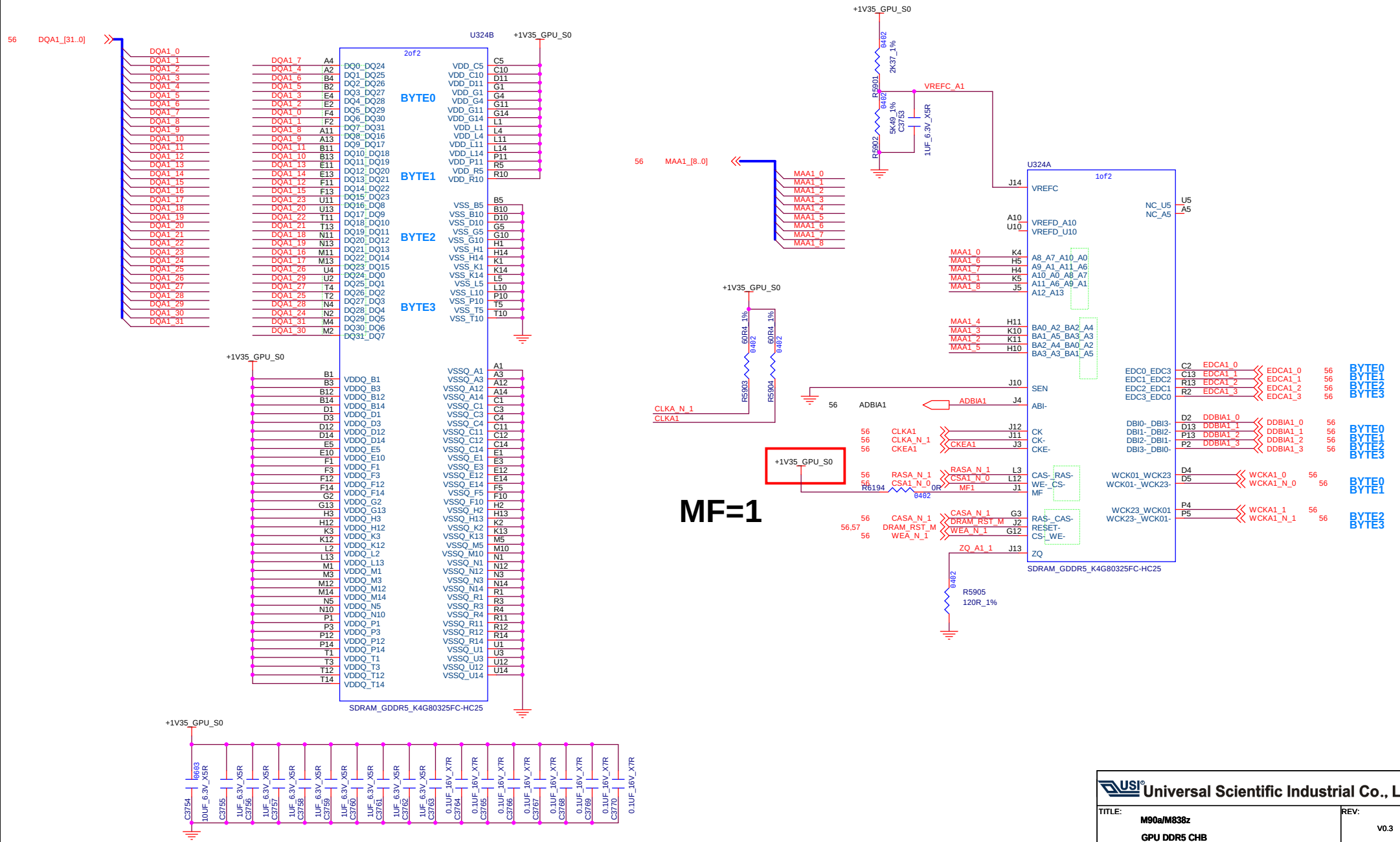
*DQ bit swapping is allowed within a byte lane.



Universal Scientific Industrial Co., Ltd.	
TITLE: M90a/M838z GPU DDR5 CHA	REV: V0.3
Document Number :	
Prepared by : KERRY HUANG	
SIZE : A2	Date: Wednesday, January 15, 2020 PAGE: 57 of 99

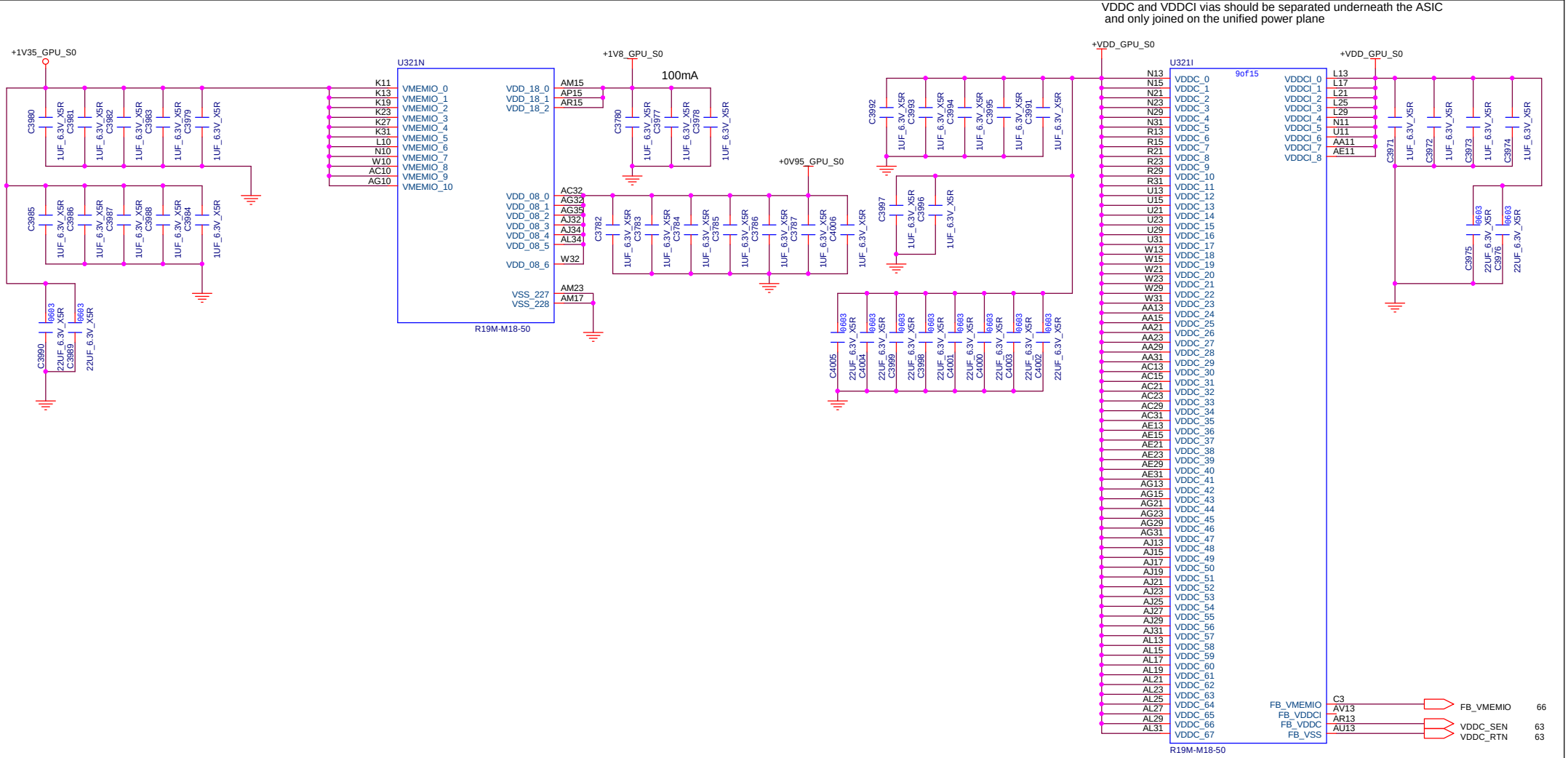
GDDR5 Memory Channel B x32 mode

MF=1

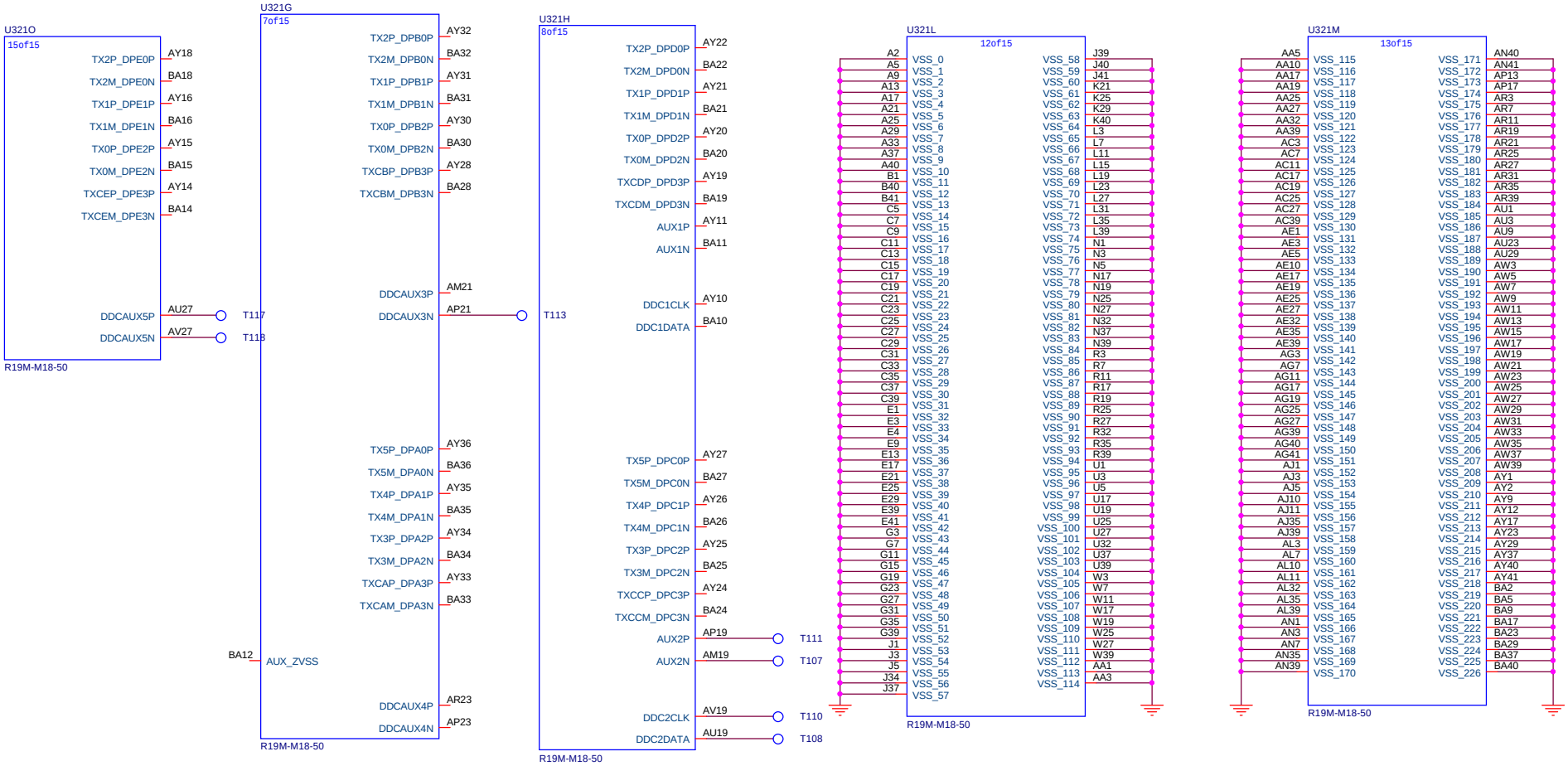


TITLE:	M90a/M838z GPU DDR5 CHB
REV:	V0.3
Document Number :	<Doc>
Prepared by :	KERRY HUANG
SIZE :	A3
Date:	Wednesday, January 15, 2020
PAGE:	58 of 99

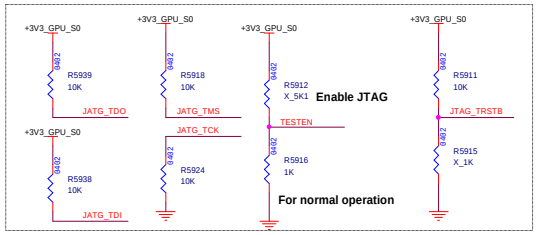
Universal Scientific Industrial Co., Ltd.

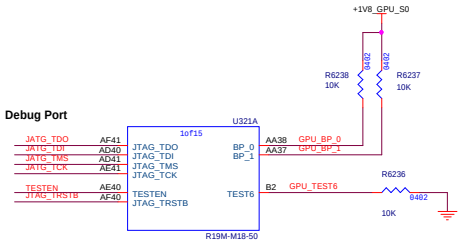


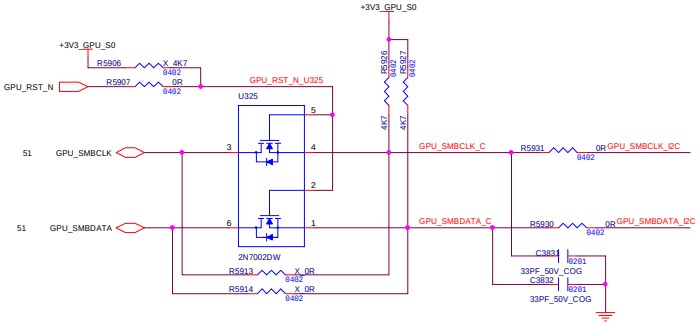
Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z R19M_POWER		REV: V0.3	
Document Number :			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 59 of 99	



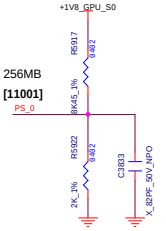
Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z R19M_POWER			REV: V0.3
Document Number :			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 60 of 99	



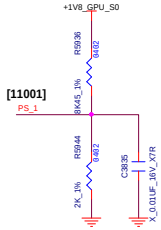




SMBUS slave address (0x41).



Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128MB	000
256MB	001
64MB	010
Reserved	011



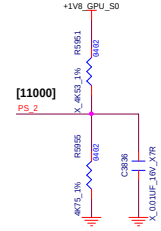
Bit 5:Tx deemphasis enabled

Bit 4:The transmitter full-swing is enabled

Bit 3:N/A

Bit 2: The CLKREQB power management capability is disabled

Bit 1:PCIe GEN3 is supported.



Bit 5:N/A 1

Bit 4:N/A 1

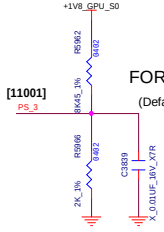
Bit 3: Disable the external BIOS ROM device.

Bit 2: N/A 0

Bit 1:N/A 0

Resitor Divider Lookup Table

R_PU	R_PD	Bits[3:1]
NC	4K75	000
8K45	2K	001
4K53	2K	010
6K98	4K99	011
4K53	4K99	100
3K24	5K62	101
3K4	10K	110
4K75	NC	111



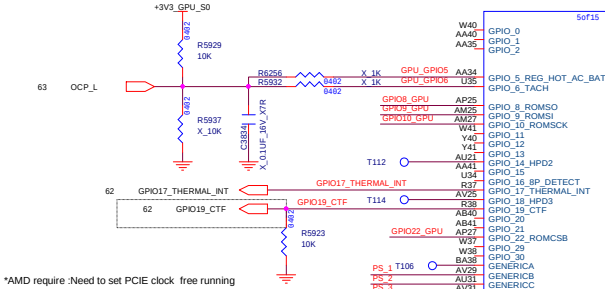
FOR Samsung

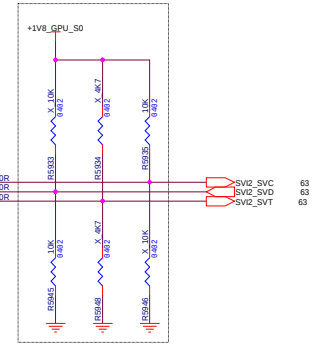
(Default)

Cap. Lookup Table

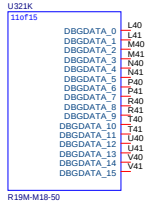
Cap. Value(nF)	Bits[5:4]
680	00
82	01
10	10
NC	11

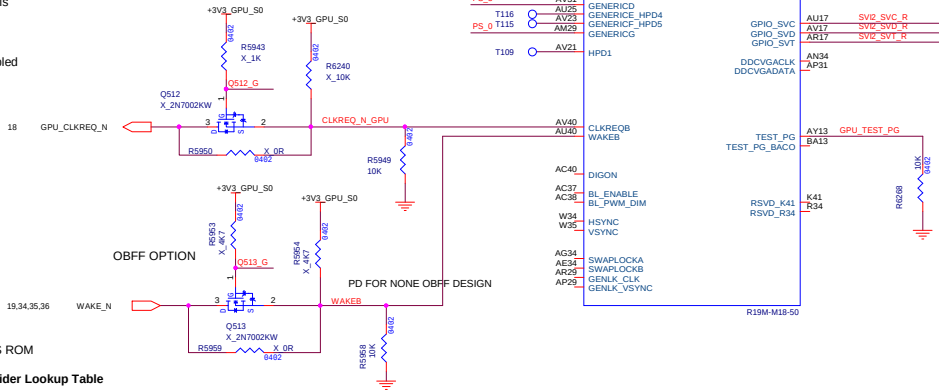
MEMORY CONFIG	PS_3[3:1]	DESCRIPTION
MICRON 8Gb	000	MICRON-MT51J256M32HF-80 :B
SAMSUNG 8Gb	001	SAMSUNG-K4G80325FC-HC25

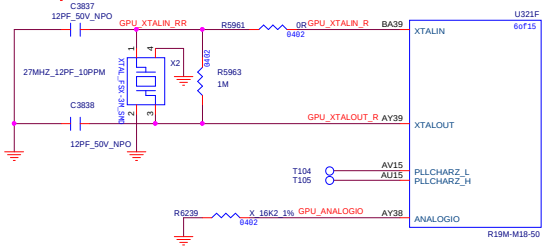


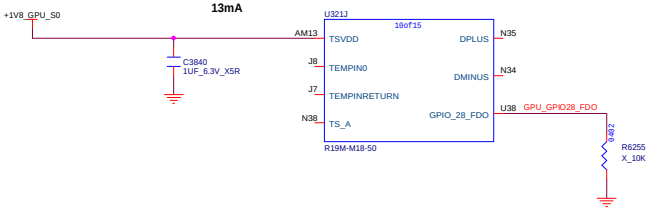


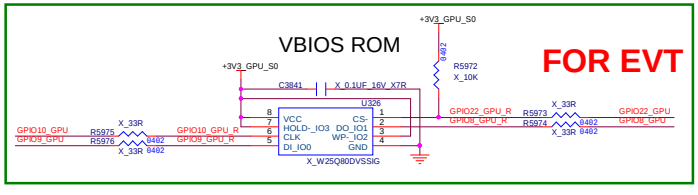
SVC	SVD	Voltage Selected(V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8





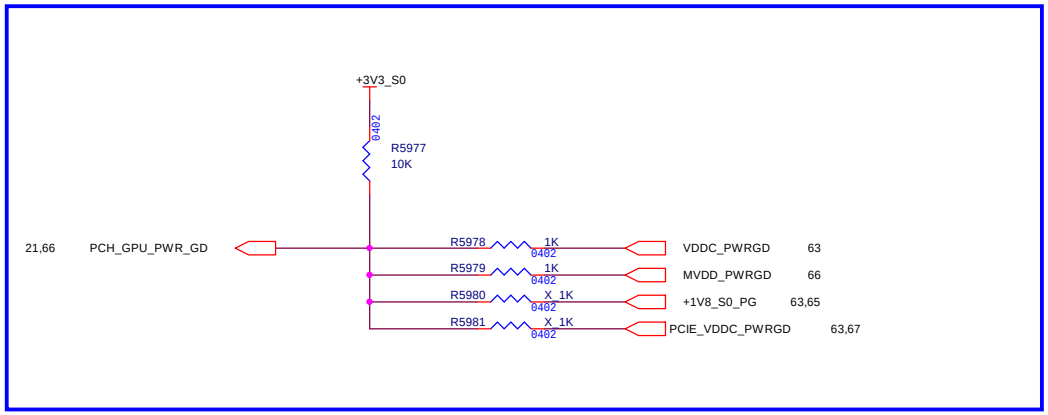


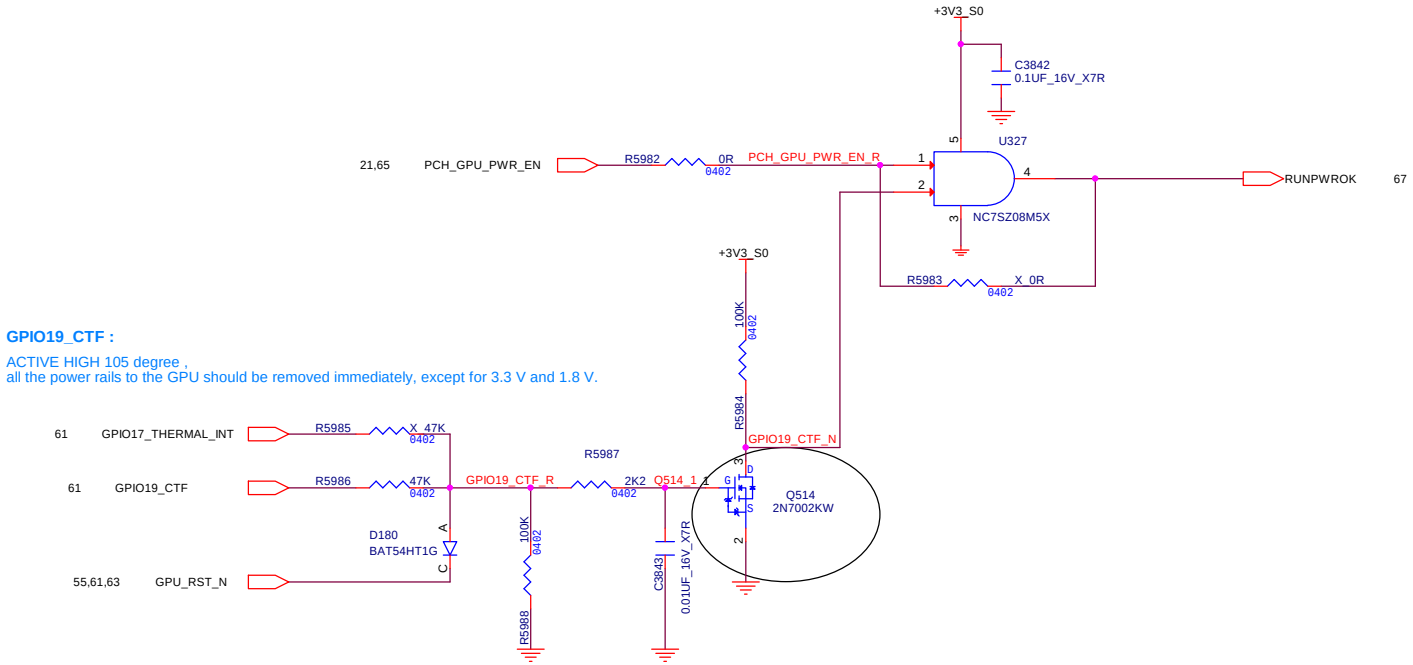




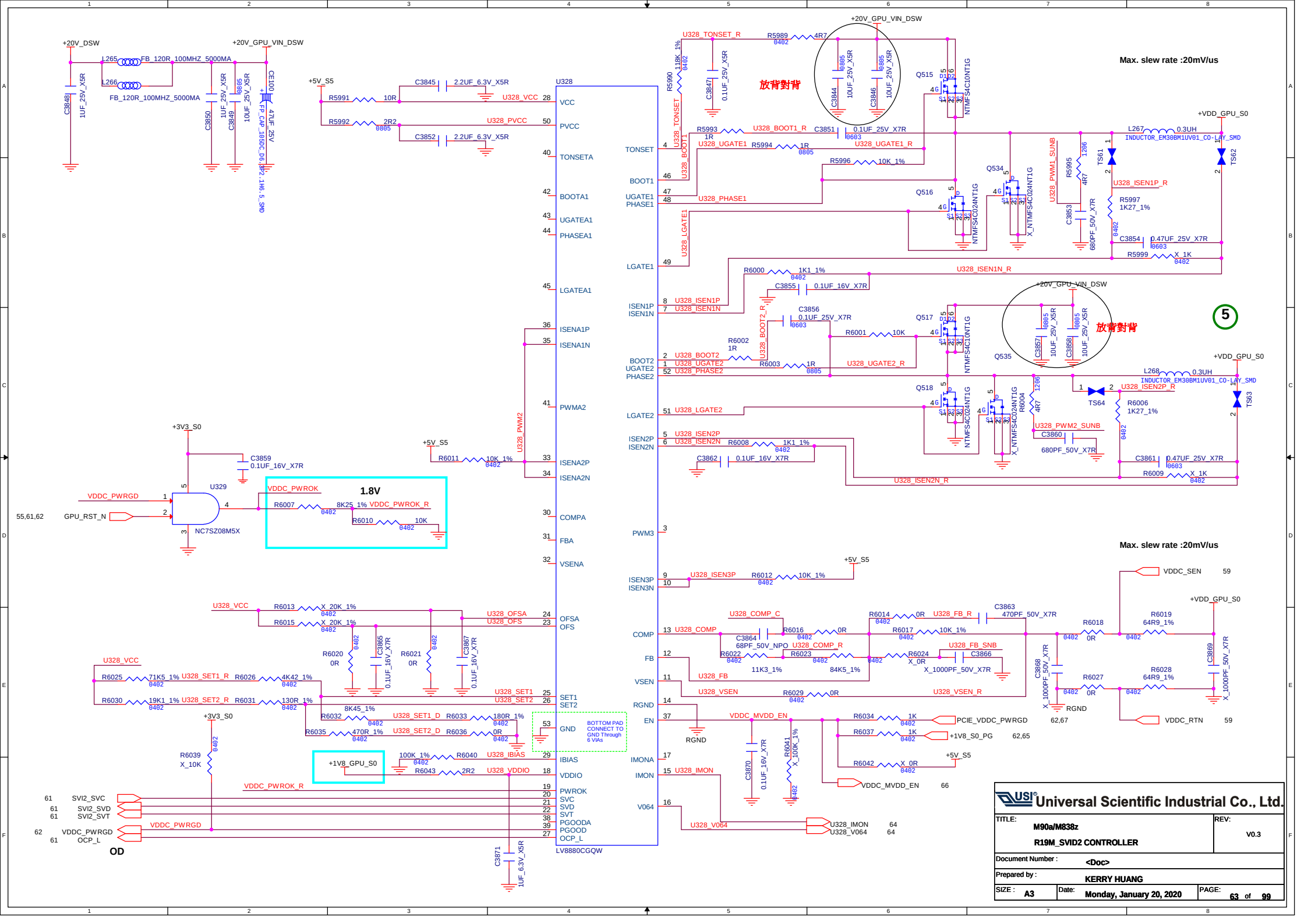
Universal Scientific Industrial Co., Ltd.

TITLE: M90a/M838z R19M_XTAL_STRAP	REV: V0.3
Document Number :	
Prepared by : KERRY HUANG	
SIZE : A2	Date: Wednesday, January 15, 2020 PAGE: 61 of 99





Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z R19M_TIMING CONTROL LOGIC			REV: V0.3
Document Number :			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 62 of 99	


+20V_DSW
+20V_GPU_VIN_DSW
FB_120R_100MHZ_5000MA
U328
LV8880CGQW
Max. slew rate :20mV/us
放背對背
1.8V
OD
Universal Scientific Industrial Co., Ltd.
TITLE:
M90a/M838z
R19M_SVID2 CONTROLLER
REV:
V0.3
Document Number :
<Doc>
Prepared by :
KERRY HUANG
SIZE :
A3
Date:
Monday, January 20, 2020
PAGE:
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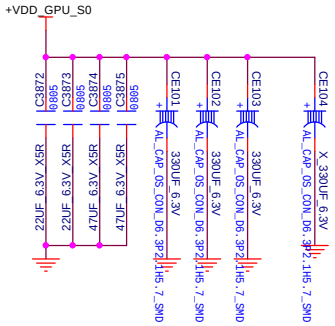
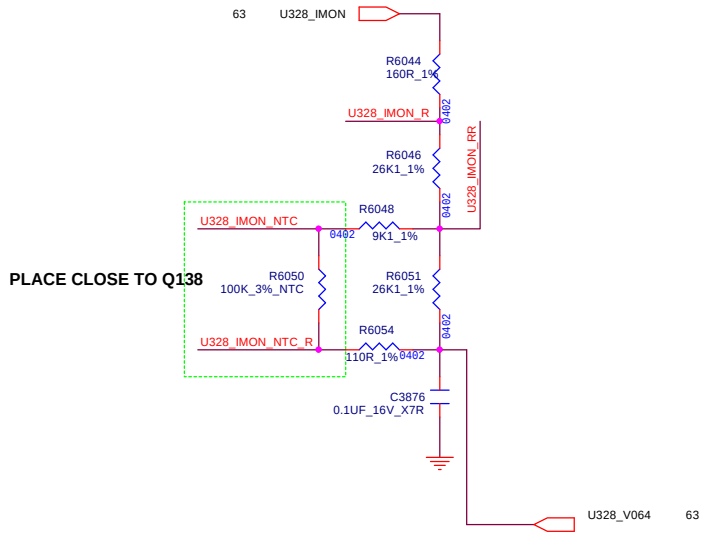




PLACE CLOSE TO Q138

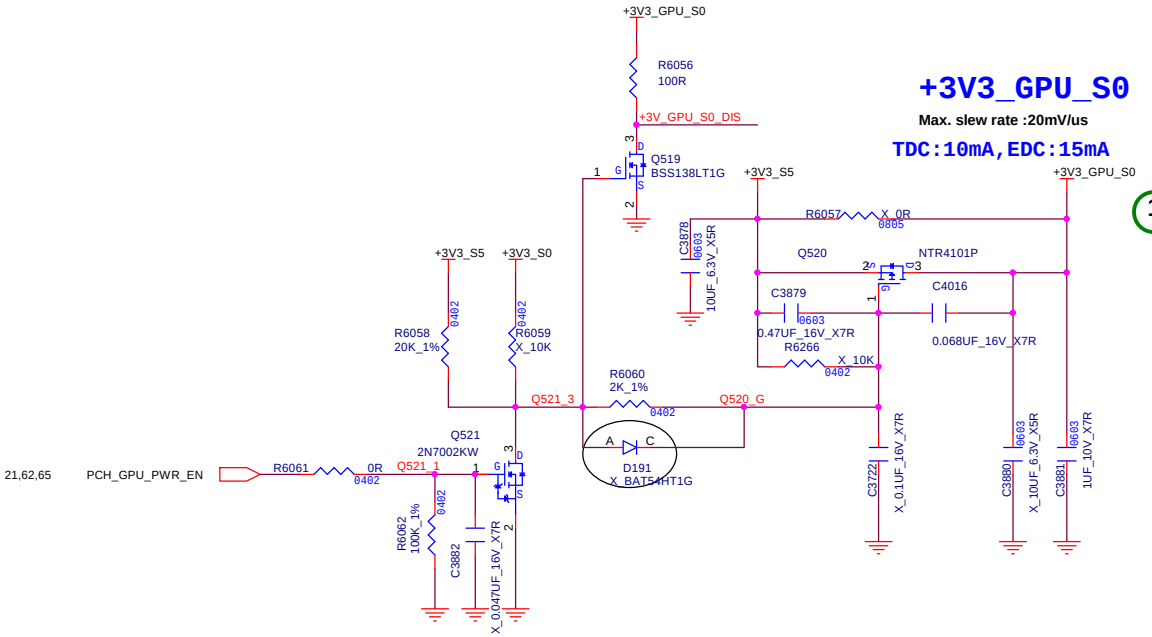
TDC :18A , EDC:60A, LL:1mOHM

+VDD_GPU_S0

Parameter	Value
Iout.max	42A Per-phase : 21A
OCP set point	63A Per-phase : 31.5A
OCP formula	IL = (3.19375-0.64)/DCR*(Rcsx/RIMON)
Switching Frequency	350kHz
Input ripple current	5.03A
Output ripple current	10.9A
Choke_size(L*W*H)(mm)	11.5*8.05*5.5
Choke_Isat	63A
Choke_DCR	0.65mΩ
Choke_LIR	51.9%
Input capacitance	10UF_25V_X5R_1206*4
Output capacitance (Near GPU side)	330UF_6.3V*4 22UF_6.3V_X5R_0805*2

Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z R19M OUTPUT			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020		PAGE: 64 of 99

+3V3_GPU_S0 DISCHARGE

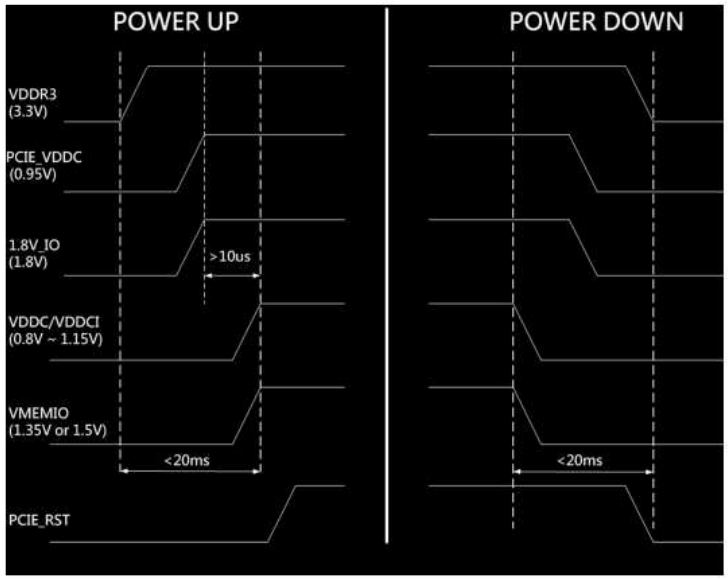


+3V3_GPU_S0

Max. slew rate :20mV/us

TDC:10mA,EDC:15mA

1



+1V8_GPU_S0

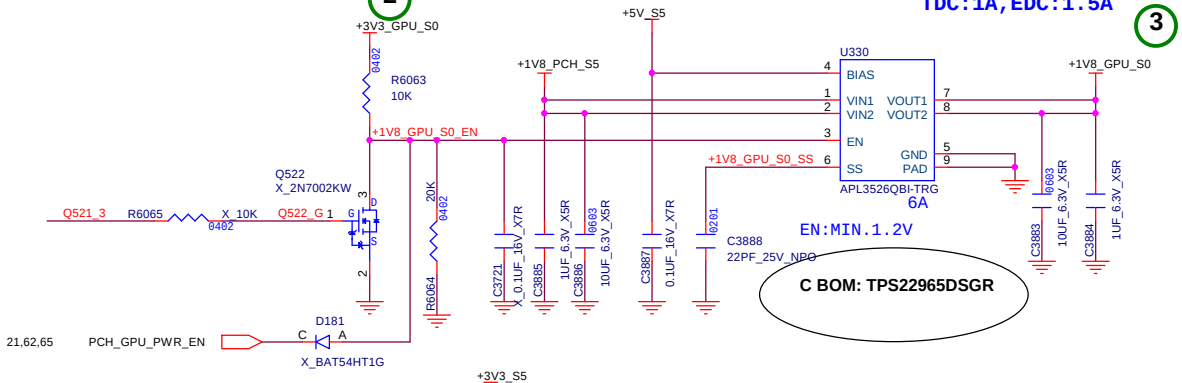
Max. slew rate :20mV/us

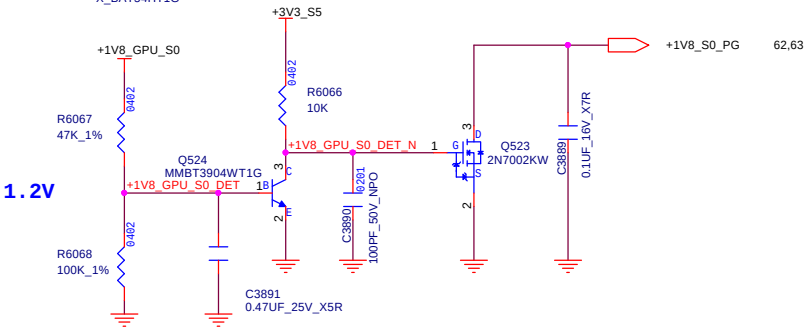
0.5A-TDC

2

TDC:1A,EDC:1.5A

3





Parameter	Value
Vin	3.3V
Vout	1.8V
Iout(max)	0.5A
Pd	0.75W
JA	75℃/W
TJ(nom)	125℃
TA(max)	68℃
Pd(max)	0.76W

Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z +3V3_GPU_S0/+1V8_GPU_S0			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
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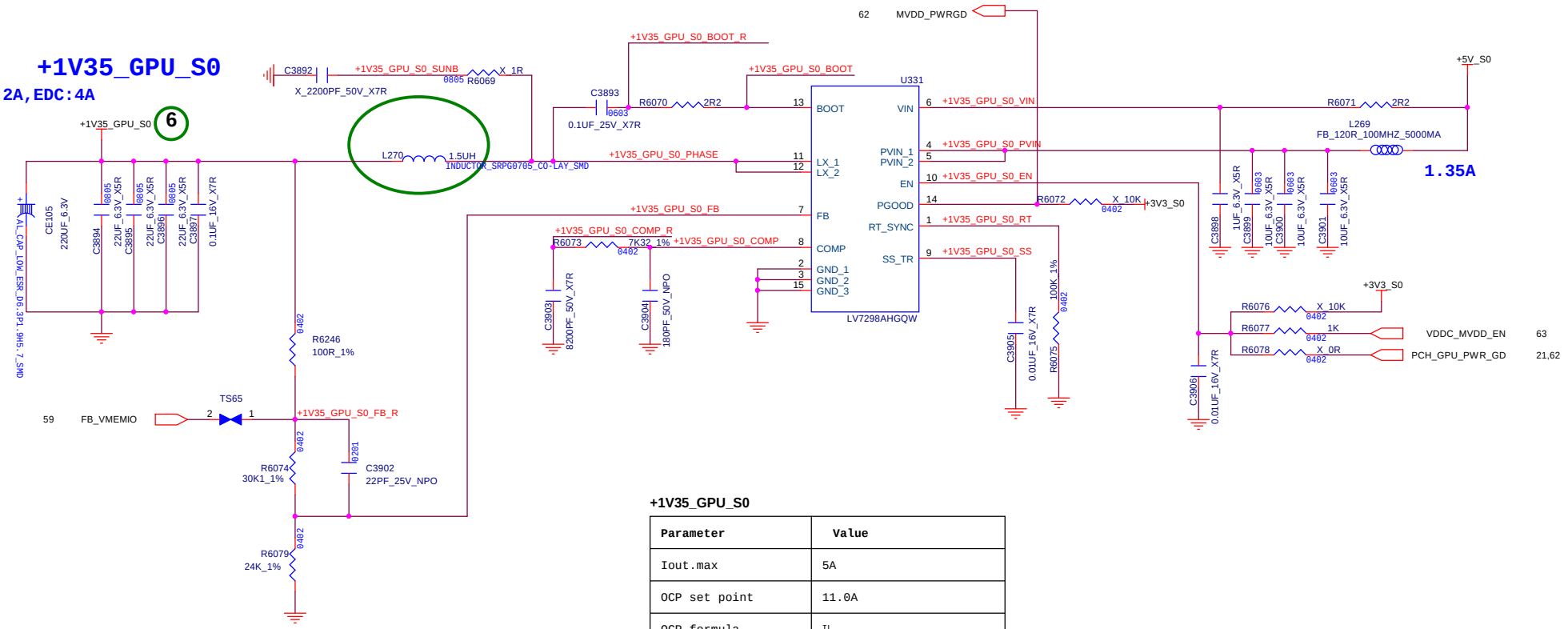
GDDR :

8Gb GD5 8Gbps Samsung K4G80325FC-HC25: 0.9A x2 =1.8A
8Gb GD5 8Gbps Micron MT51J256M32HF-80 :B : 1.06A x2 =2.12A

GPU: 2A

+1V35_GPU_S0

TDC:2A,EDC:4A



+1V35_GPU_S0

Parameter	Value
Iout.max	5A
OCP set point	11.0A
OCP formula	IL = (3.19375-0.64)/DCR*(Rcsx/RIMONA)
Switching Frequency	450kHz
Input ripple current	1.26A
Output ripple current	1.865A
Choke_size(L*W*H)(mm)	7.0*8.3*5.0
Choke_Isat	11A
Choke_DCR	5.1mΩ
Choke_LIR	37.3%
Input capacitance	10UF_25V_X5R_1206*2
Output capacitance (Near GPU side)	330UF_6.3V*1 22UF_6.3V_X5R_0805*3

Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z +1V35_GPU_S0			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020		PAGE: 66 of 99

27-094232-02CHIP COIL 1.5uH 20% 48mR 4*4*1.8MM SMD2 MAGIC WQPIG4018L-1R5M

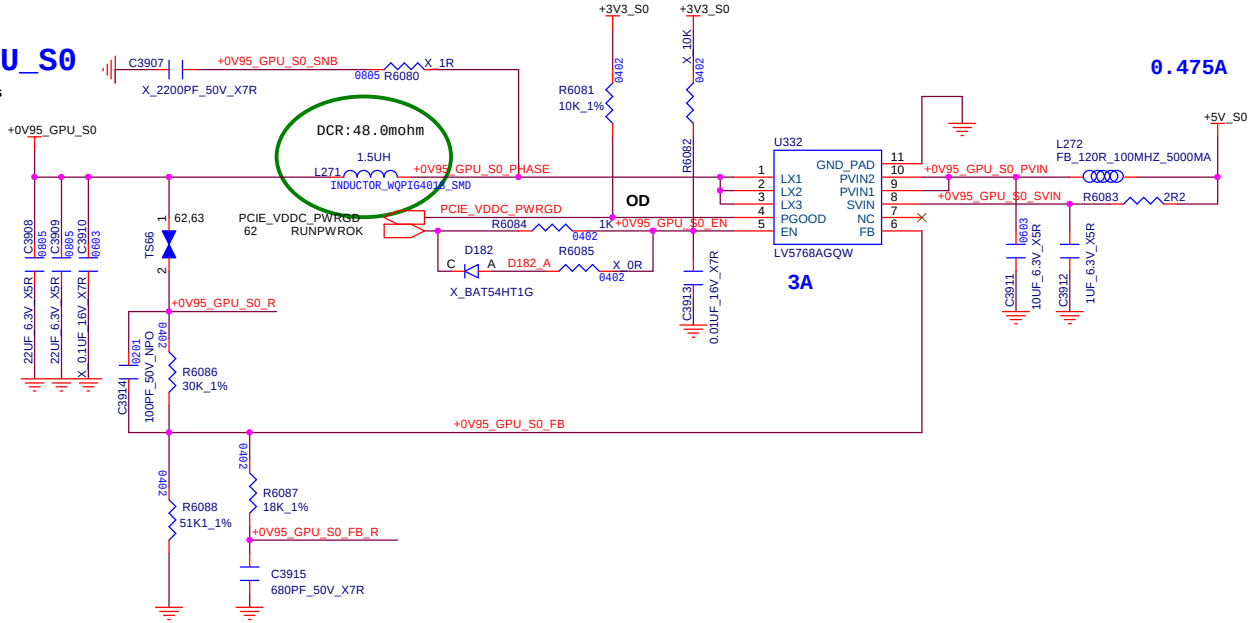
+0V95_GPU_S0

Max. slew rate :20mV/us

TDC:2A, EDC:3A

4

0.475A



Parameter	Value
Iout.max	2.0A
OCP set point	4A
OCP formula	IC controlled
Switching Frequency	1MHz
Input ripple current	0.91A
Output ripple current	0.46A
Choke_size(L*W*H)(mm)	4.3*4.3*2.1
Choke_Isat	3.3A
Choke_DCR	48.00mΩ
Choke_LIR	22.6%
Input capacitance	10UF_6.3V_X5R_0603*1
Output capacitance	22UF_6.3V_X5R_0805*2

Universal Scientific Industrial Co., Ltd.

TITLE: M90a/M838z +0V95_GPU_S0		REV: V0.3
Document Number : <Doc>		
Prepared by : KERRY HUANG		
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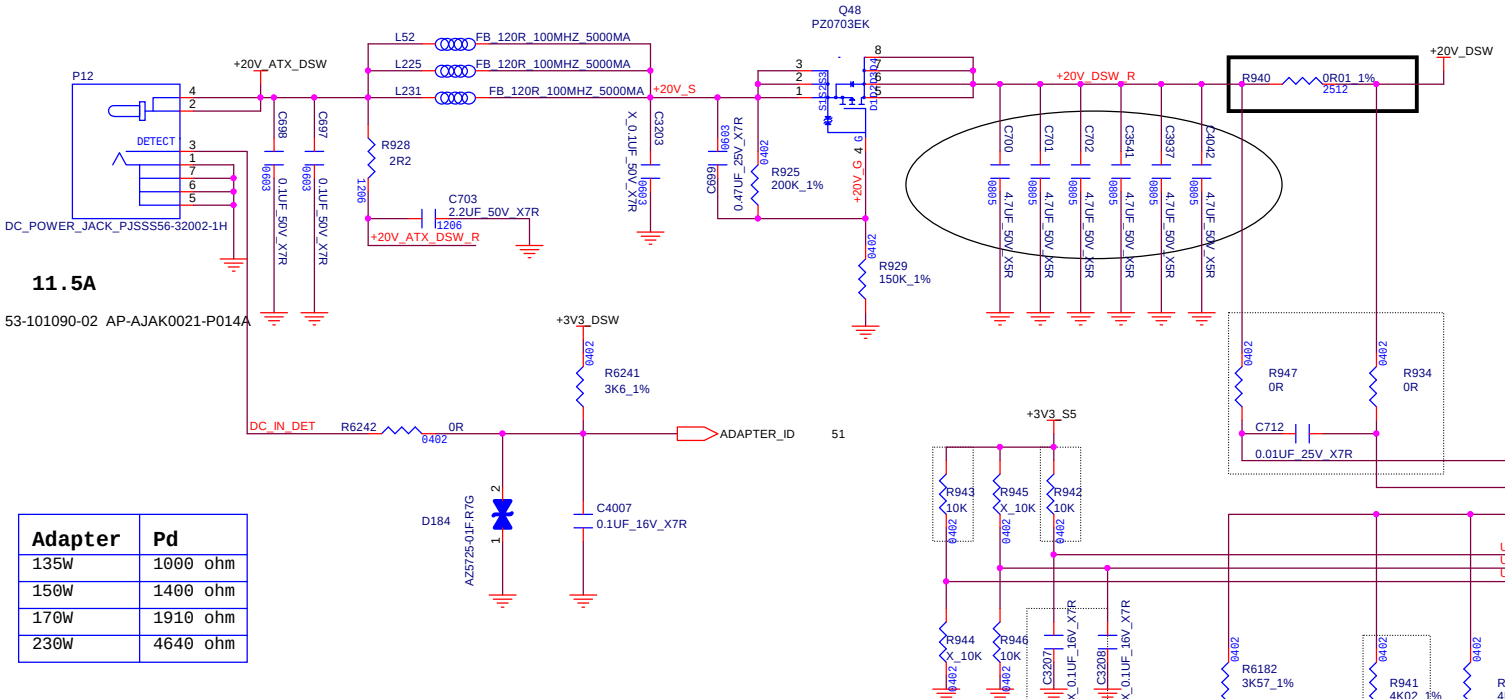
ADP 20V POWER



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POWER METER (INA300)

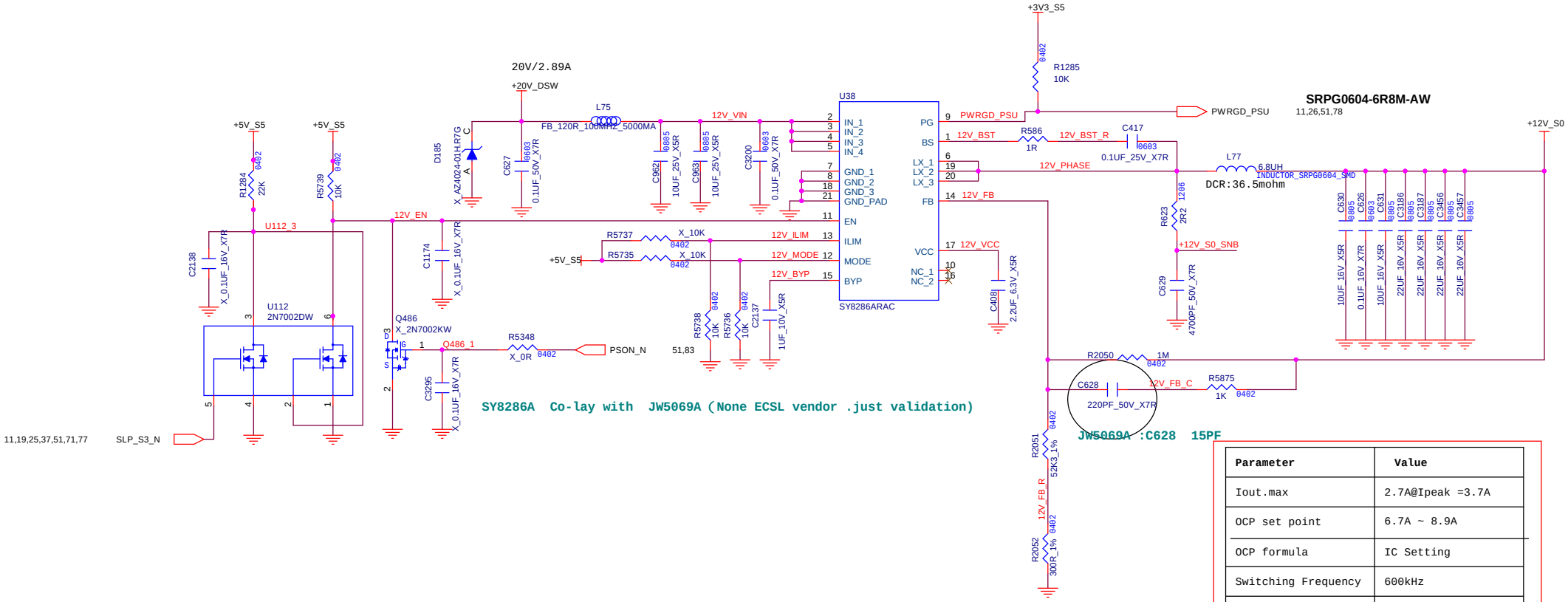
Adapter	Pd
135W	1000 ohm
150W	1400 ohm
170W	1910 ohm
230W	4640 ohm

Adapter	230W	170W	150W	135W
Rating Current	11.5A	8.5A	7.5A	6.75A
Peak Current	12.65A	9.35A	9A	7.5A
Pd	4640 ohm	1910 ohm	1400 ohm	1000 ohm
EC Detection Voltage	1.85V	1.14V	0.92V	0.71V
Indication by Power Manager	230W	170W	150W	135W
OBP Trigger Point	12.6A	9A	8A	7A

35-330292-01N FET ENHANCEMENT PM5Q2EA SOT23

For 230W current limit
For 170W current limit
For 150W current limit (default)
For 135W current limit

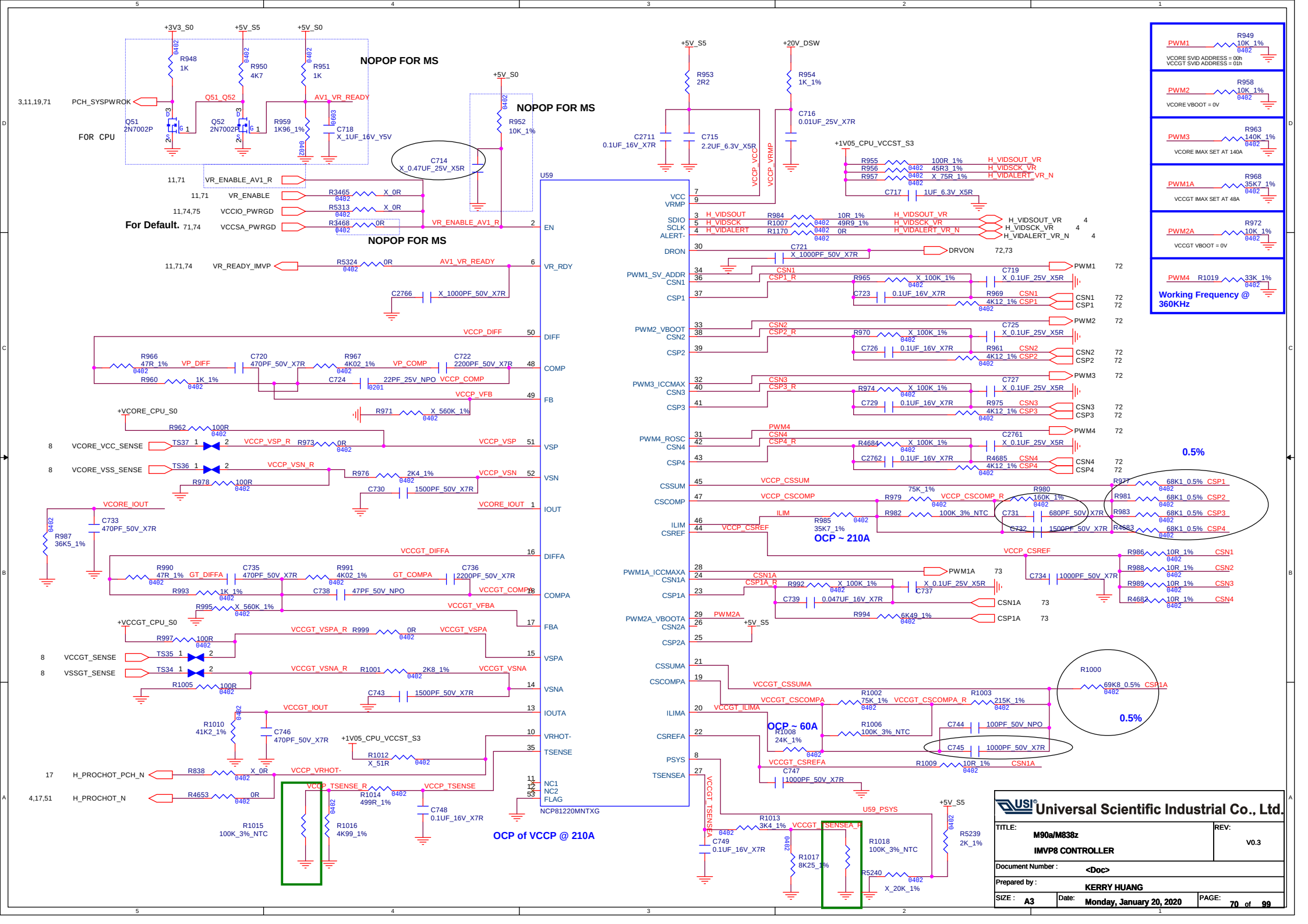
Universal Scientific Industrial Co., Ltd.	
TITLE: M90a/M838z DC IN	REV: V0.3
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Monday, January 20, 2020
PAGE: 68 of 99	



Parameter	Value
Iout.max	2.7A@Ipeak =3.7A
OCP set point	6.7A ~ 8.9A
OCP formula	IC Setting
Switching Frequency	600kHz
Input ripple current	1.82A
Output ripple current	1.18A
Choke_size(L*W*H)(mm)	7.6*6.9*4.0
Choke_Isat	10A
Choke_DCR	37mΩ
Choke_LIR	31.8%
Input capacitance	10UF_25V_X5R_1206*2
Output capacitance	22UF_16V*4 10UF_16V_X5R_0805*2

Universal Scientific Industrial Co., Ltd.

TITLE: M90a/M838z 20V TO 12V			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 69 of 99	


NOPOP FOR MS
NOPOP FOR MS
NOPOP FOR MS
FOR CPU
For Default.
Q51_Q52
AV1_VR_READY
VR_ENABLE_AV1_R
VR_ENABLE
VCCIO_PWRGD
VCCSA_PWRGD
VR_READY_IMVP
VCCP_DIFF
VCCP_COMP
VCCP_VFB
VCCP_VSP
VCCP_VSN
VCORE_IOUT
VCCGT_DIFFA
VCCGT_COMP
VCCGT_VFBA
VCCGT_VSPA
VCCGT_VSNA
VCCGT_IOUT
VCCP_VRHOT-
VCCP_TSENSE
VCCP_CSSUM
VCCP_CSCOMP
VCCP_CSREF
VCCGT_CSSUMA
VCCGT_CSCOMPA
VCCGT_ILIMA
VCCGT_CSREFA
VCCGT_TSENSEA
U59_PSYS
OCP ~ 210A
OCP ~ 60A
OCP of VCCP @ 210A
0.5%
0.5%
Working Frequency @ 360KHz
NCP81220MNTXG
Universal Scientific Industrial Co., Ltd.
M90a/M838z
IMVP8 CONTROLLER
V0.3
<Doc>
KERRY HUANG
Monday, January 20, 2020
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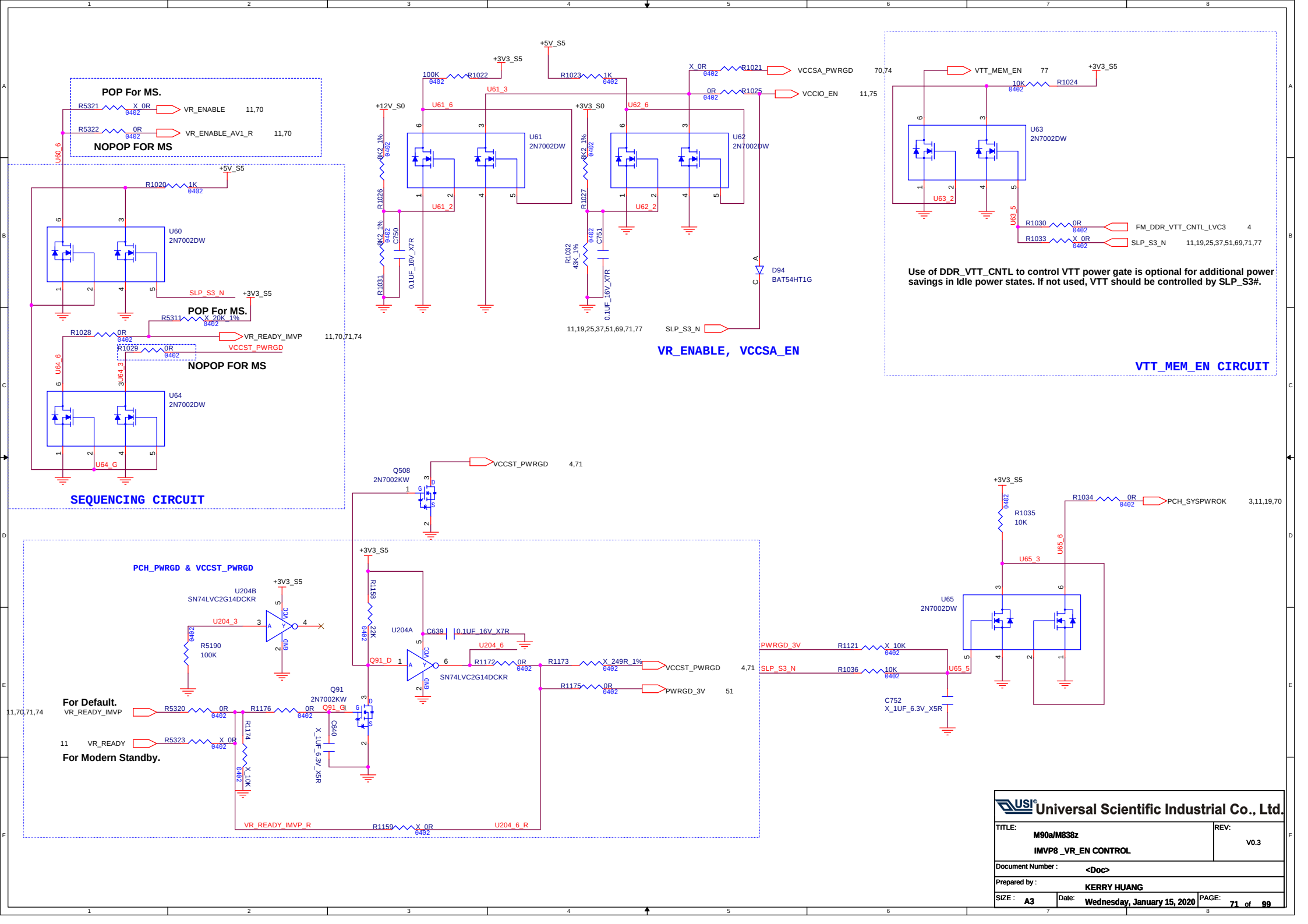
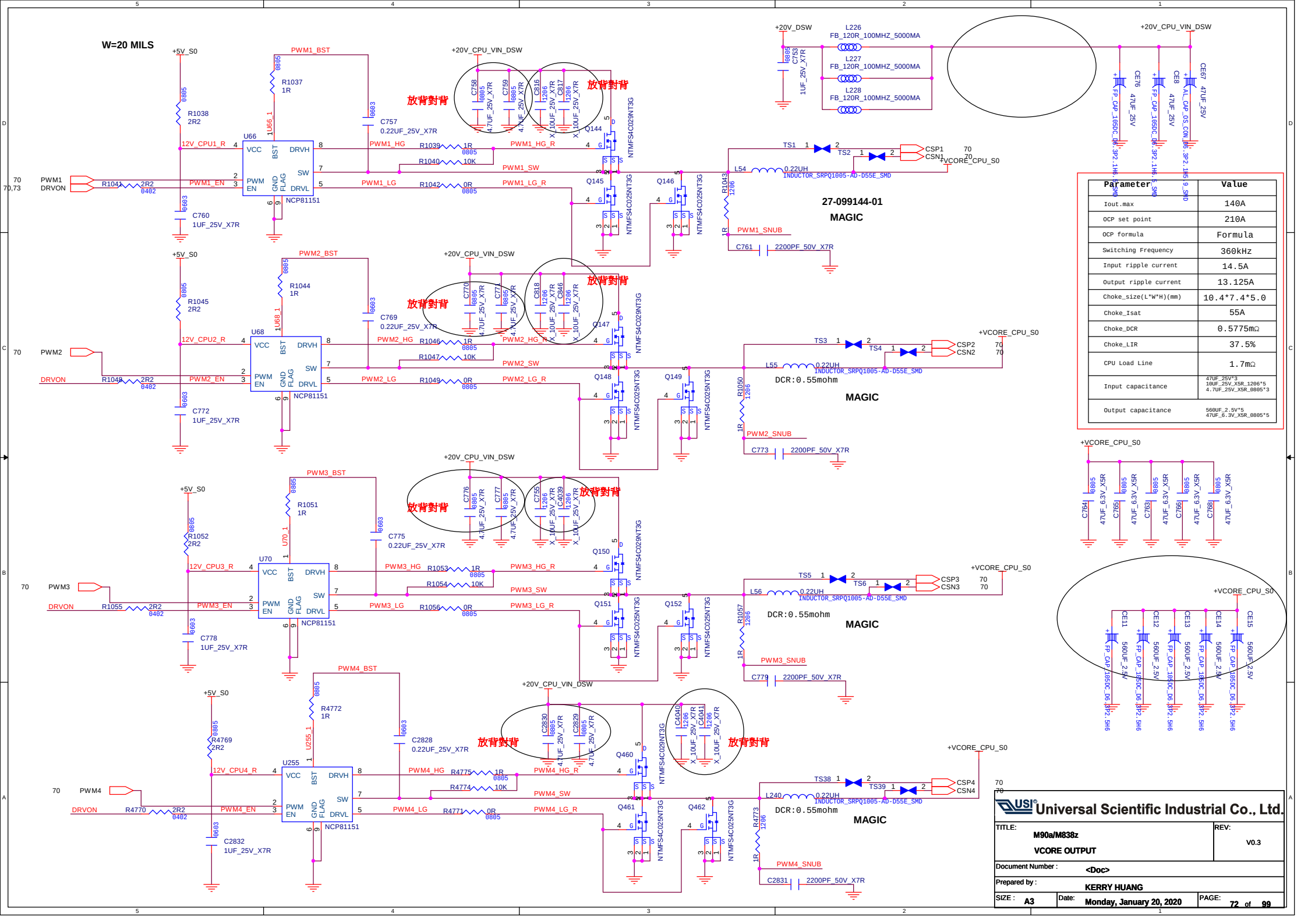

POP For MS.
R5321 X_0R 0402 VR_ENABLE 11,70
R5322 0R 0402 VR_ENABLE_AV1_R 11,70
NOPOP FOR MS
U60_6
+5V_S5
R1020 1K 0402
U60 2N7002DW
SLP_S3_N
+3V3_S5
POP For MS.
R5311 X_20K_1% 0402
R1028 0R 0402 VR_READY_IMVP 11,70,71,74
R1029 0R 0402 VCCST_PWRGD
NOPOP FOR MS
U64_6
U64_3
U64 2N7002DW
U64_G
SEQUENCING CIRCUIT
+5V_S5
+3V3_S5
100K R1022 0402
R1023 1K 0402
X_0R 0402 R1021 VCCSA_PWRGD 70,74
0R 0402 R1025 VCCIO_EN 11,75
U61_3
+12V_S0
U61_6
+3V3_S0
U62_6
U61 2N7002DW
U62 2N7002DW
8K2_1% 0402 R1026
8K2_1% 0402 R1027
U61_2
U62_2
C750 0.1UF_16V_X7R
R1031
R1032 43K_1%
C751 0.1UF_16V_X7R
D94 BAT54HT1G
11,19,25,37,51,69,71,77
SLP_S3_N
VR_ENABLE, VCCSA_EN
VTT_MEM_EN 77
+3V3_S5
10K 0402 R1024
U63 2N7002DW
U63_2
U63_5
R1030 0R 0402 FM_DDR_VTT_CNTL_LVC3 4
R1033 X_0R 0402 SLP_S3_N 11,19,25,37,51,69,71,77
Use of DDR_VTT_CNTL to control VTT power gate is optional for additional power savings in Idle power states. If not used, VTT should be controlled by SLP_S3#.
VTT_MEM_EN CIRCUIT
Q508 2N7002KW
VCCST_PWRGD 4,71
PCH_PWRGD & VCCST_PWRGD
U204B SN74LVC2G14DCKR
U204_3
R5190 100K
U204A
C639 0.1UF_16V_X7R
U204_6
R1158 27K
Q91_D
R1172 0R 0402
R1173 X_249R_1% 0402 VCCST_PWRGD 4,71
R1175 0R 0402 PWRGD_3V 51
SN74LVC2G14DCKR
Q91 2N7002KW
Q91_G
For Default.
VR_READY_IMVP
11,70,71,74
R5320 0R 0402
R1176 0R 0402
11 VR_READY
R5323 X_0R 0402
R1174 X_10K 0402
C640 X_1UF_6.3V_X5R
For Modern Standby.
VR_READY_IMVP_R
R1159 X_0R 0402
U204_6_R
PWRGD_3V
R1121 X_10K 0402
SLP_S3_N
R1036 10K 0402
U65_5
C752 X_1UF_6.3V_X5R
U65 2N7002DW
U65_3
U65_6
R1035 10K
R1034 0R 0402 PCH_SYSPWROK 3,11,19,70
Universal Scientific Industrial Co., Ltd.
TITLE: M90a/M838z
IMVP8 _VR_EN CONTROL
REV: V0.3
Document Number : <Doc>
Prepared by : KERRY HUANG
SIZE : A3
Date: Wednesday, January 15, 2020
PAGE: 71 of 99



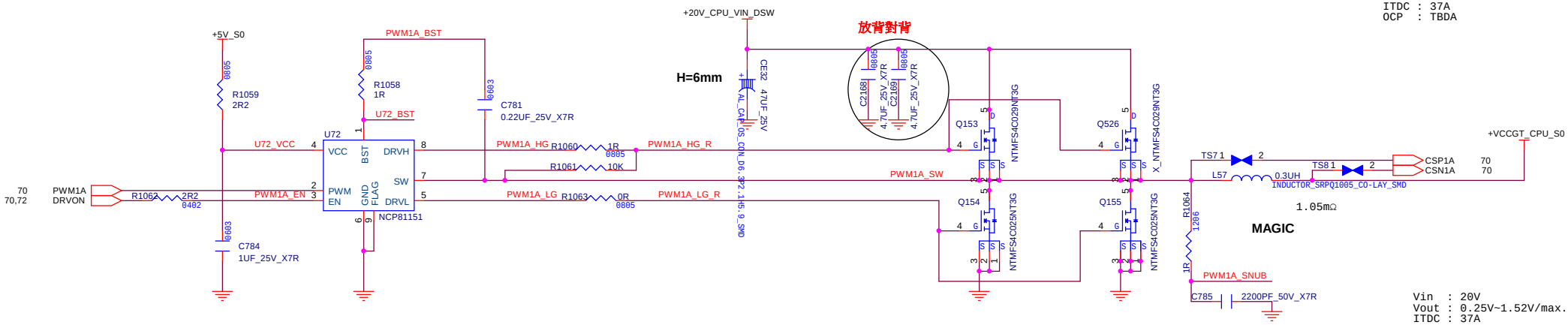
Parameter	Value
Iout.max	140A
OCP set point	210A
OCP formula	Formula
Switching Frequency	360kHz
Input ripple current	14.5A
Output ripple current	13.125A
Choke_size(L*W*H)(mm)	10.4*7.4*5.0
Choke_Isat	55A
Choke_DCR	0.5775mΩ
Choke_LIR	37.5%
CPU Load Line	1.7mΩ
Input capacitance	47UF_25V*3 10UF_25V_X5R_1206*5 4.7UF_25V_X5R_0805*3
Output capacitance	560UF_2.5V*5 47UF_6.3V_X5R_0805*5

Universal Scientific Industrial Co., Ltd.

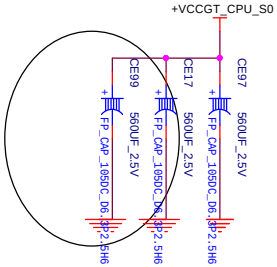
TITLE: M90a/M838z VCORE OUTPUT		REV: V0.3
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Monday, January 20, 2020	PAGE: 72 of 99

+VCCGT_CPU_S0

Vin : 20V
Vout : 0.25V~1.52V/max. 51A
ITDC : 37A
OCP : TBDA



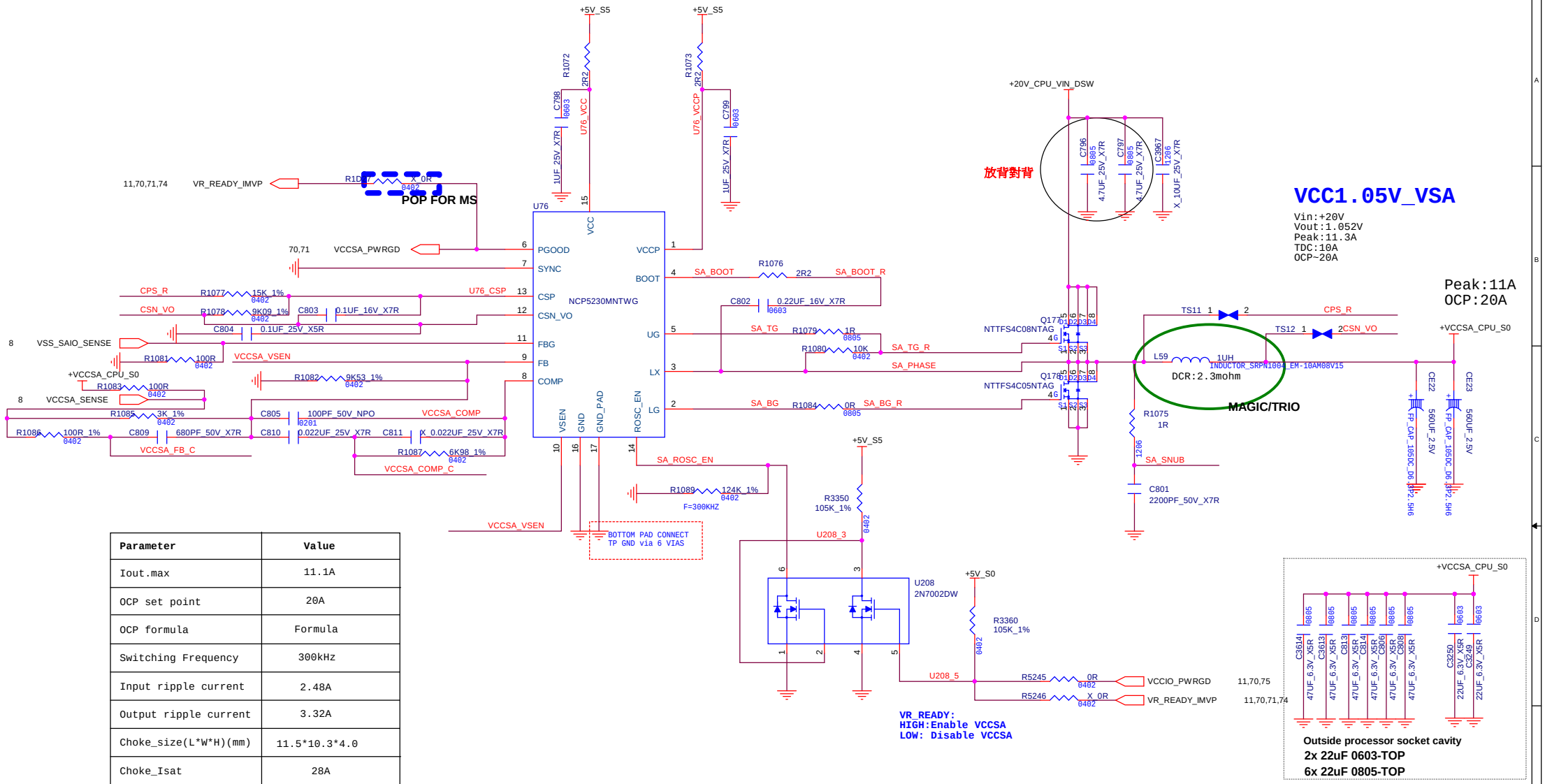
Vin : 20V
Vout : 0.25V~1.52V/max. 51A
ITDC : 37A
OCP : TBDA



Parameter	Value
Iout.max	35A
OCP set point	60A
OCP formula	Formula
Switching Frequency	360kHz
Input ripple current	7.45A
Output ripple current	11.43A
Choke_size(L*W*H)(mm)	10.4*7.4*5.0
Choke_Isat	55A
Choke_DCR	1.05mΩ
Choke_LIR	32.6%
CPU GT Load Line	4.0mΩ
Input capacitance	4.7UF_25V_X5R_0805*2 10UF_25V_X5R_1206*1
Output capacitance	560UF_2.5V*3

Universal Scientific Industrial Co., Ltd.

TITLE: M90a/M838z VCCGT OUTPUT		REV: V0.3
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Monday, January 20, 2020	PAGE: 73 of 99



Parameter	Value
Iout.max	11.1A
OCP set point	20A
OCP formula	Formula
Switching Frequency	300kHz
Input ripple current	2.48A
Output ripple current	3.32A
Choke_size(L*W*H)(mm)	11.5*10.3*4.0
Choke_Isat	28A
Choke_DCR	2.3mΩ +- 7%
Choke_LIR	29.9%
Input capacitance	10UF_25V_X5R_1206*1
Output capacitance	560UF_2.5V*2 47UF_6.3V_X5R_0805*6 22UF_6.3V_X5R_0603*2

Universal Scientific Industrial Co., Ltd.	
TITLE: M90a/M838z VCCSA OUTPUT	REV: V0.3
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Monday, January 20, 2020
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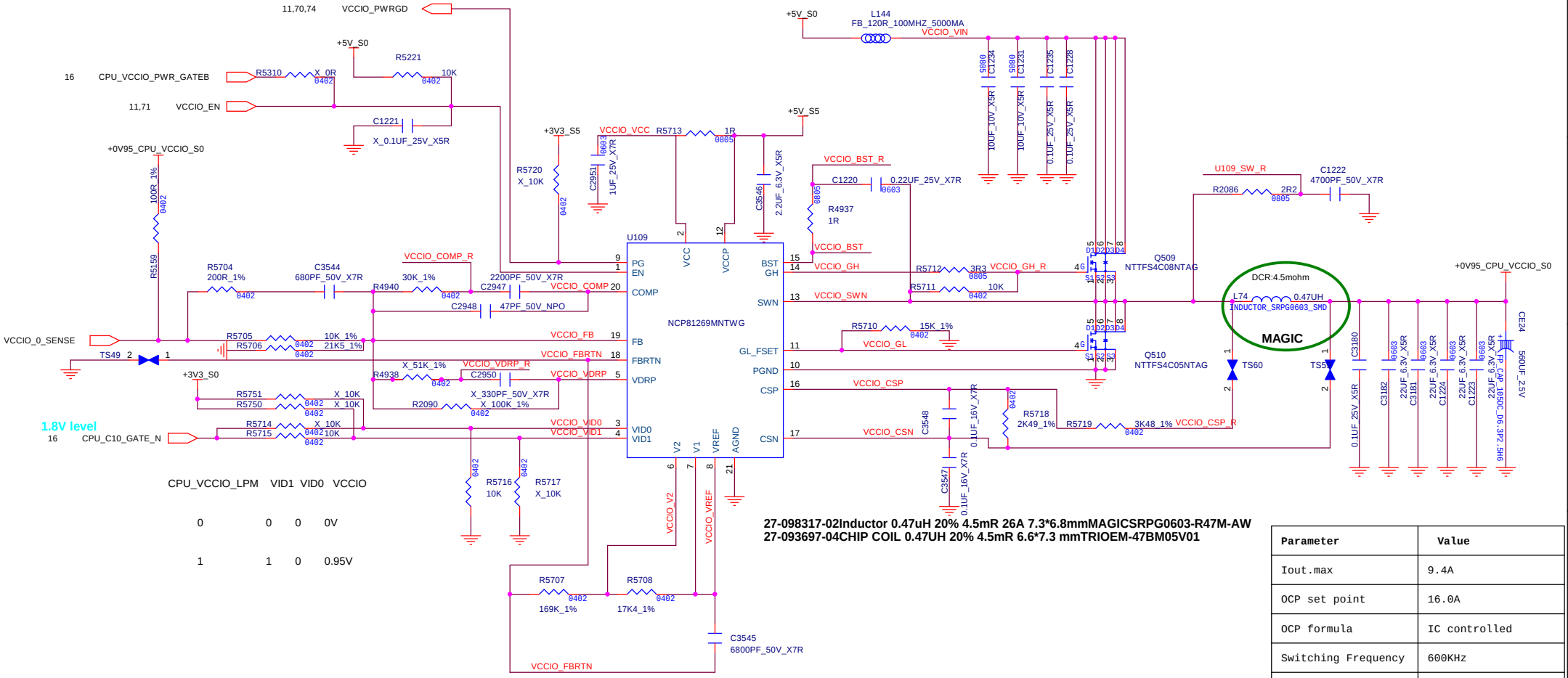
EN:PU VDD 1M35



CPU_VCCIO_LPM	VID1	VID0	VCCIO
0	0	0	0V
1	1	0	0.95V

27-098317-02Inductor 0.47uH 20% 4.5mR 26A 7.3*6.8mmMAGICSRPG0603-R47M-AW
27-093697-04CHIP COIL 0.47UH 20% 4.5mR 6.6*7.3 mmTRIOEM-47BM05V01

Parameter	Value
Iout.max	9.4A
OCP set point	16.0A
OCP formula	IC controlled
Switching Frequency	600KHz
Input ripple current	2.51A
Output ripple current	1.49A
Choke_size(L*W*H)(mm)	7.6*7.1*3.1
Choke_Isat	26.0A
Choke_DCR	4.50mΩ
Choke_LIR	29.0%
Input capacitance	10UF_10V_X5R_0805*2
Output capacitance	560UF_2.5V*1 22UF_6.3V_X5R_0805*4

Universal Scientific Industrial Co., Ltd.

TITLE: M90a/M838z VCCIO		REV: V0.3
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 75 of 99

BLANK

Universal Scientific Industrial Co., Ltd.		
TITLE: M90a/M838z BLANK		REV: V0.3
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 76 of 99

DDR4 1.2V

Vin : 20V
Vout : 1.2V/max. TBDA
ITDC : TBDA
OCP : 16.32A

Parameter	Value
Iout.max	9.6A
OCP set point	16.32A
OCP formula	ILIMIT=RLIMIT/ RDS(ON)* 5μA/10
Switching Frequency	400kHz
Input ripple current	2.28A
Output ripple current	2.82A
Choke_size(L*W*H)(mm)	8.894*8.256*5.0
Choke_Isat	19A
Choke_DCR	3.85mΩ
Choke_LIR	29.4%
Input capacitance	10UF_25V_X5R_1206*3
Output capacitance	560UF_6.3V*2 22UF_6.3V_X5R_0805*4

colayout 27-015726-01 TRIO EM-10AM34V01
DCR:3.85mohm

Rds:2.2~2.8mohm

MAGIC

S0/S1/S3

S4/S5

0.6V DDRVTT

Vin : 1.2V
Vout : 0.6V/ max.0.75A
ITDC :TBDA

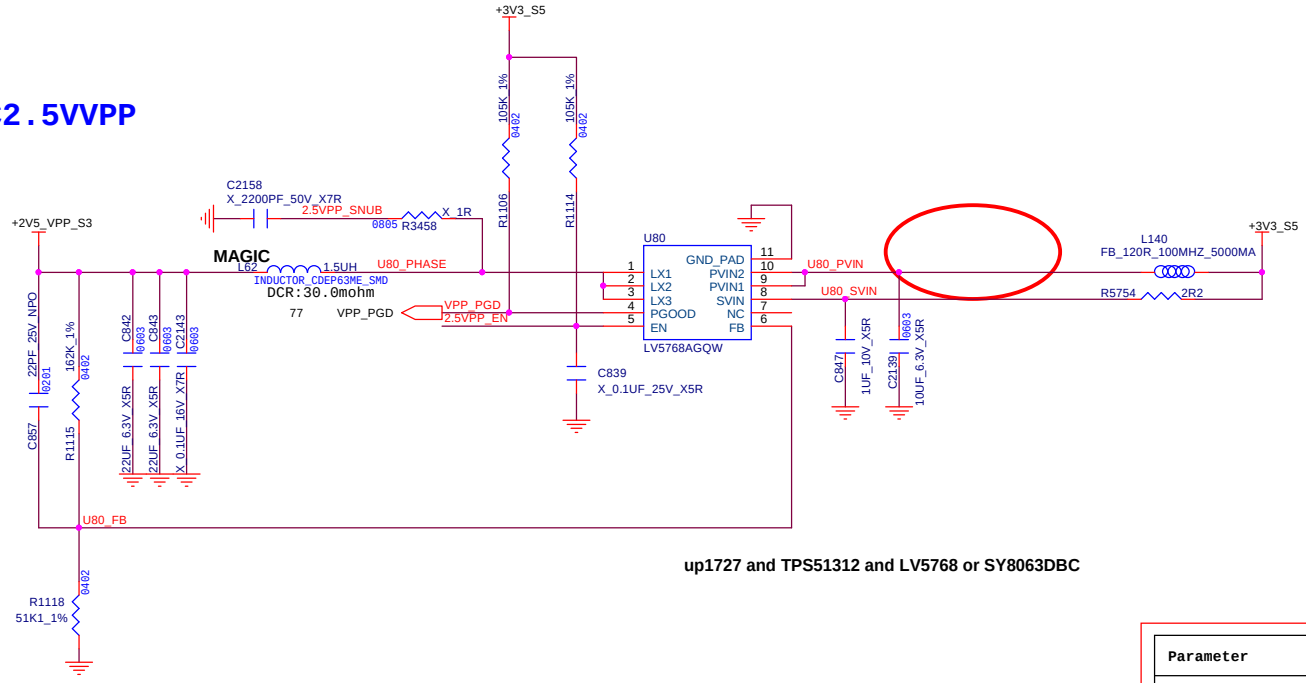
S0/S1

S3/S4/S5

Parameter	Value
Output voltage	0.6V
Maximum output current	0.75A
IC current limit	1.6A ~ 3.6A
Max. PD(theoretically)	0.45W
Rja	30°C/W
Enable condition	"+3V_S5" ON

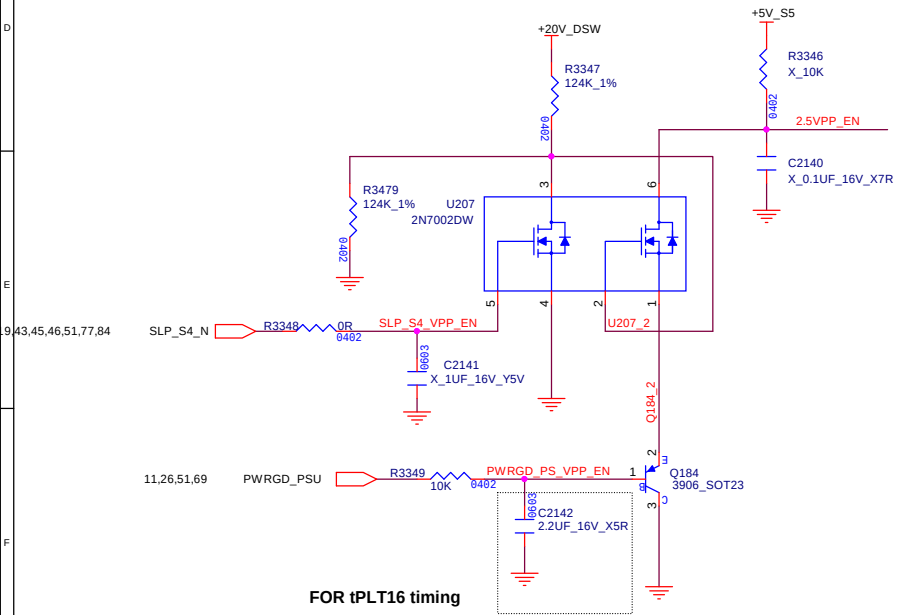
Universal Scientific Industrial Co., Ltd.	
TITLE: M90a/M838z System DDR4 VR	REV: V0.3
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Wednesday, January 15, 2020
PAGE: 77 of 99	

VCC2.5VPP



up1727 and TPS51312 and LV5768 or SY8063DBC

227-094232-02CHIP COIL 1.5uH 20% 48mR 4*4*1.8MM SMD2 MAGIC WQPIG4018L-1R5M



FOR tPLT16 timing

Parameter	Value
Iout.max	2.0A
OCP set point	4A
OCP formula	IC controlled
Switching Frequency	1MHz
Input ripple current	0.72A
Output ripple current	0.40A
Choke_size(L*W*H)(mm)	4.3*4.3*2.1
Choke_Isat	3.3A
Choke_DCR	48.0mΩ
Choke_LIR	20.2%
Input capacitance	10UF_6.3V_X5R_0603*1
Output capacitance	22UF_6.3V_X5R_0805*2

Universal Scientific Industrial Co., Ltd.

TITLE: M90a/M838z VCC2.5V_VPP		REV: V0.3	
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 78 of 99	

Enable	Disable
EN1,EN2 > 1.4 V	EN1,EN2 < 0.4 V

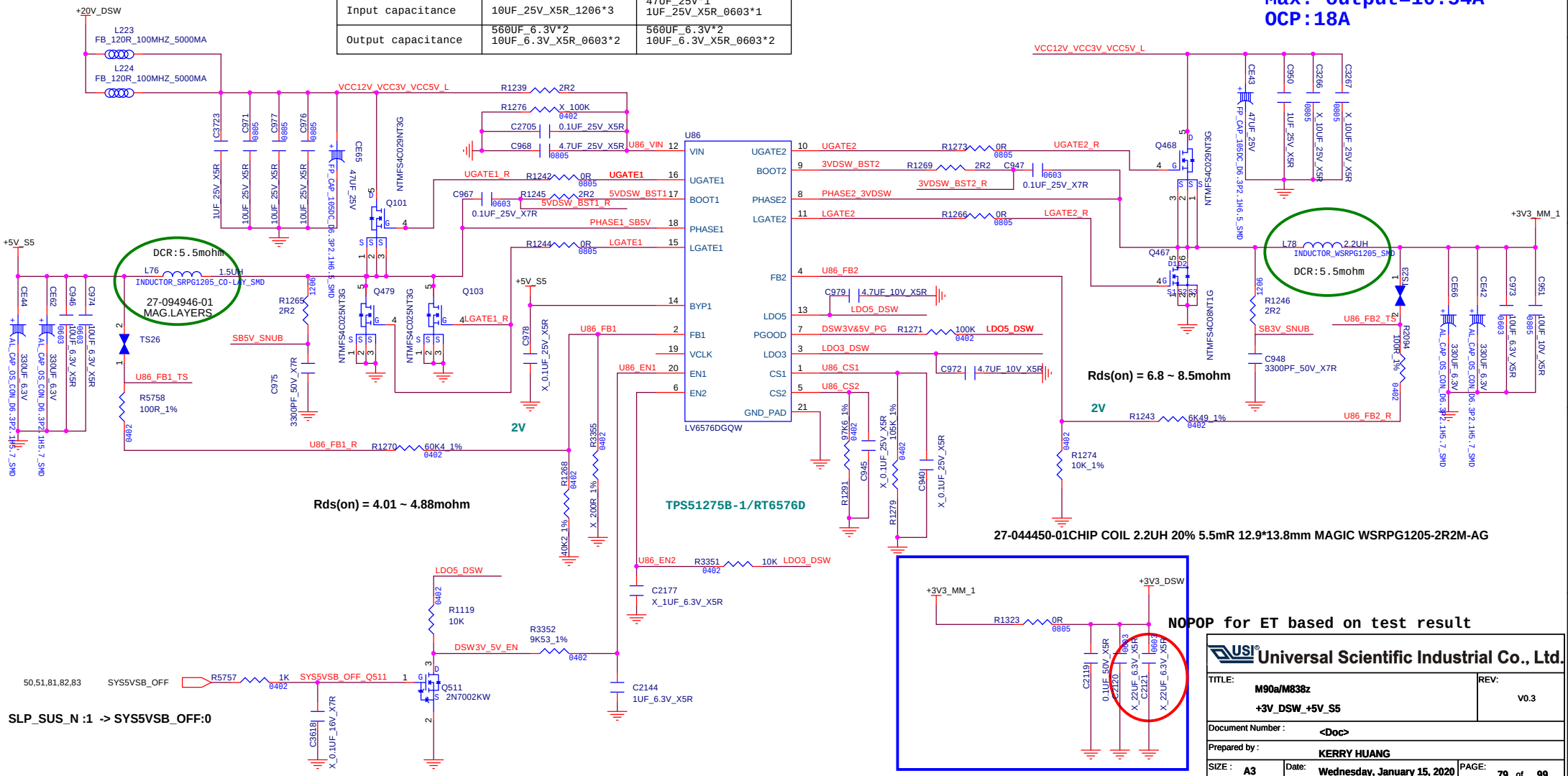
+5V_S5/+3V3_MM_1

VCC3 , VCC5 total Power is 139.8W

Parameter	+5V_S5	+3V_MM_1
Iout.max	21A	10.54A
OCP set point	32.73A	17.94A
OCP formula	RLIMIT=(ILIMITxRDS(ON))x8/10μA	RLIMIT=(ILIMITxRDS(ON))x8/10μA
Switching Frequency	300kHz	355kHz
Input ripple current	9.09A	3.91A
Output ripple current	8.34A	3.53A
Choke_size(L*W*H)(mm)	13.8*12.9*5	13.8*12.9*5
Choke_Isat	48A	32A
Choke_DCR	4.1mΩ	5.5mΩ
Choke_LIR	39.7%	33.5%
Input capacitance	10UF_25V_X5R_1206*3	47UF_25V*1 1UF_25V_X5R_0603*1
Output capacitance	560UF_6.3V*2 10UF_6.3V_X5R_0603*2	560UF_6.3V*2 10UF_6.3V_X5R_0603*2

+5V_S5
Max. output=19.5A
OCP:32A

+3V_MM_1
Max. output=10.54A
OCP:18A



Universal Scientific Industrial Co., Ltd.	
TITLE: M90a/M838z +3V_DSW_+5V_S5	REV: V0.3
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Wednesday, January 15, 2020
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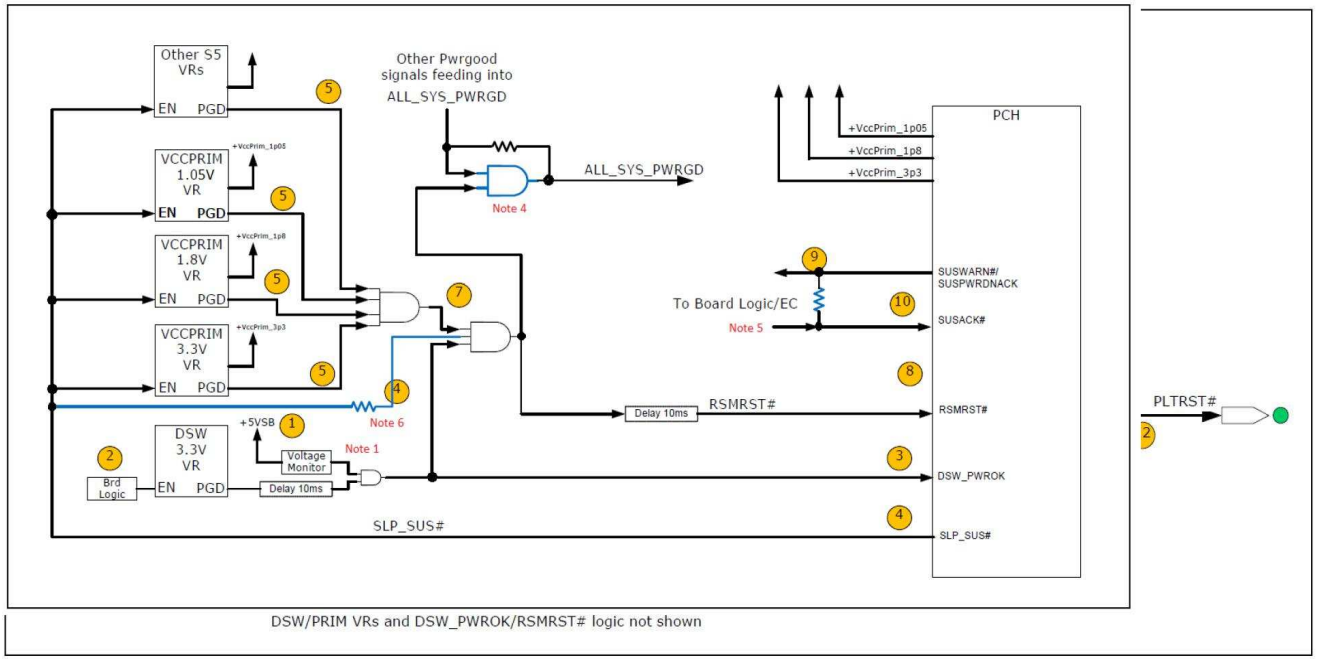
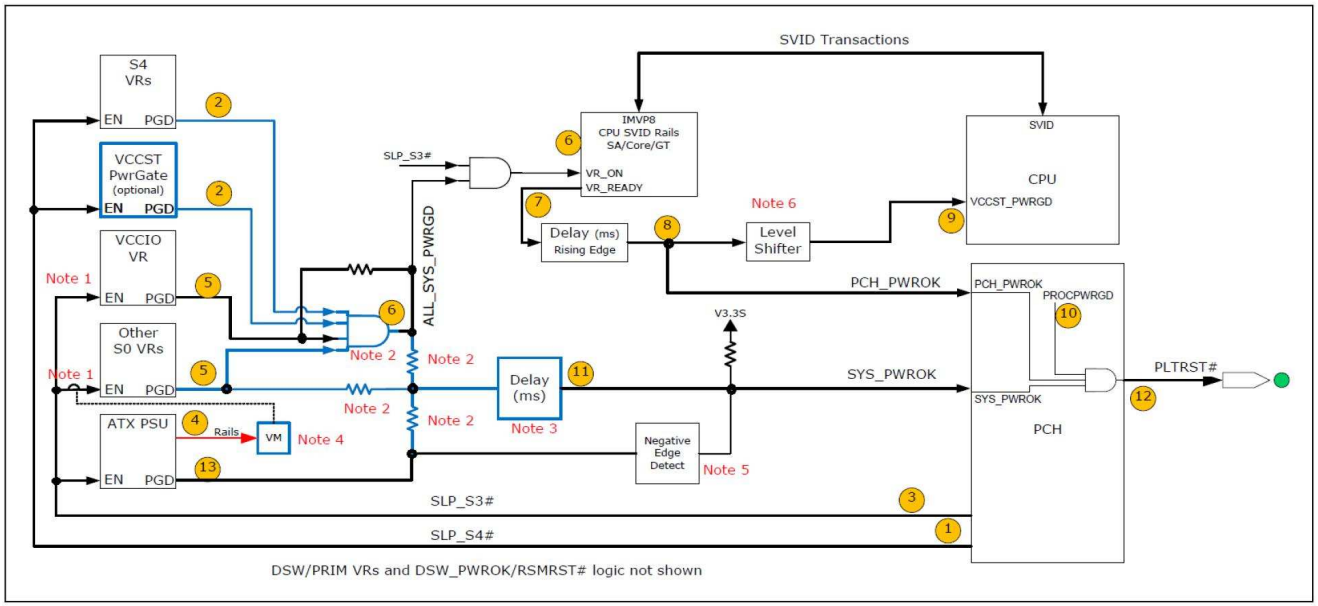
Flow Diagram for RSMRST# Generation



DSW/PRIM VRs and DSW_PWROK/RSMRST# logic not shown

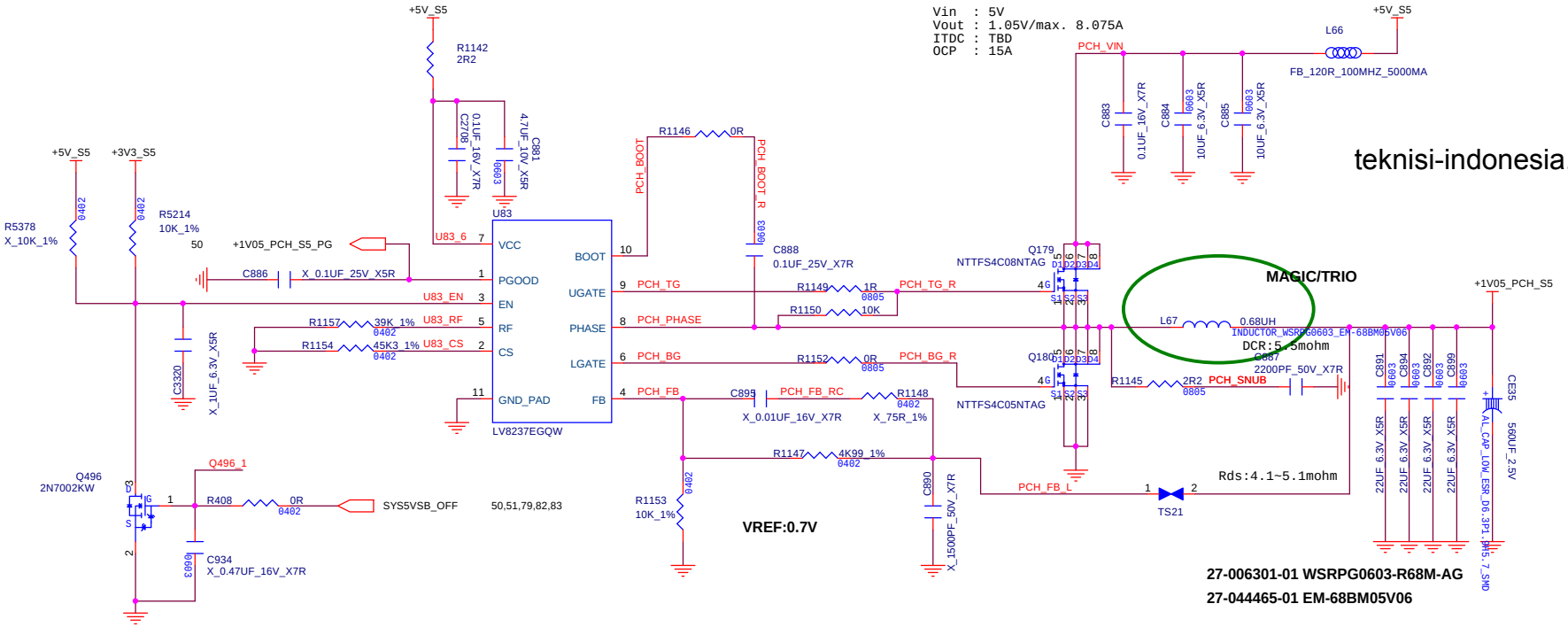
Figure 349. Flow Diagram for SYS_PWROK/PCH_PWROK Generation



DSW/PRIM VRs and DSW_PWROK/RSMRST# logic not shown

Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z BLANK			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 80 of 99	

+1V05_PCH_S5



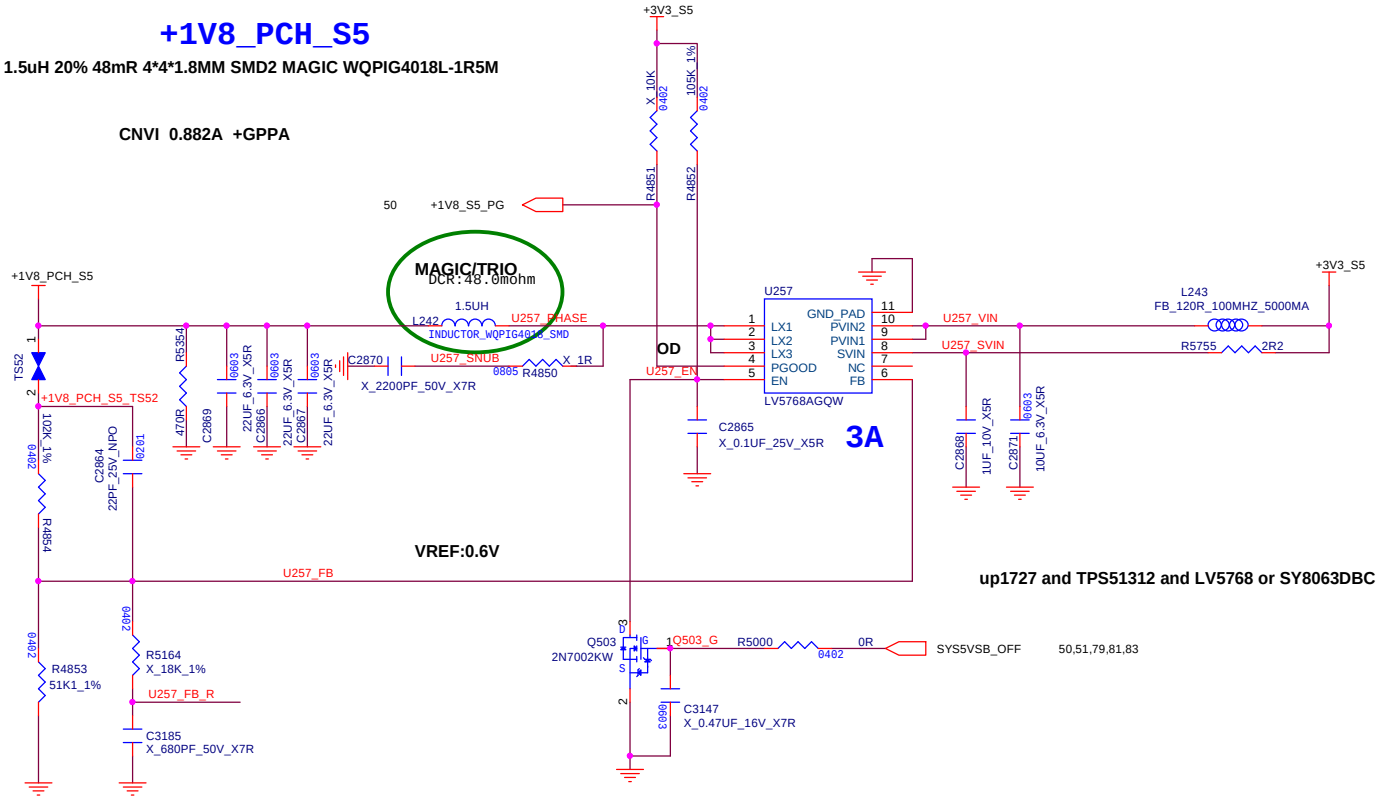
Parameter	Value
Iout.max	9.45A
OCP set point	15A
OCP formula	Iocp=10uA*Rcs/(8*Rdson) +Iripple/2
Switching Frequency	430kHz
Input ripple current	3.85A
Output ripple current	2.84A
Choke_size(L*W*H)(mm)	7.6*6.8*3.2
Choke_Isat	25A
Choke_DCR	5.5mΩ
Choke_LIR	30.0%
Input capacitance	10UF_6.3V_X5R_0603*2
Output capacitance	560UF_2.5V*1 22UF_6.3V_X5R_0805*4

Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z V1P05_PCH			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020		PAGE: 81 of 99

+1V8_PCH_S5

27-094232-02CHIP COIL 1.5uH 20% 48mR 4*4*1.8MM SMD2 MAGIC WQPIG4018L-1R5M

CNVI 0.882A +GPPA

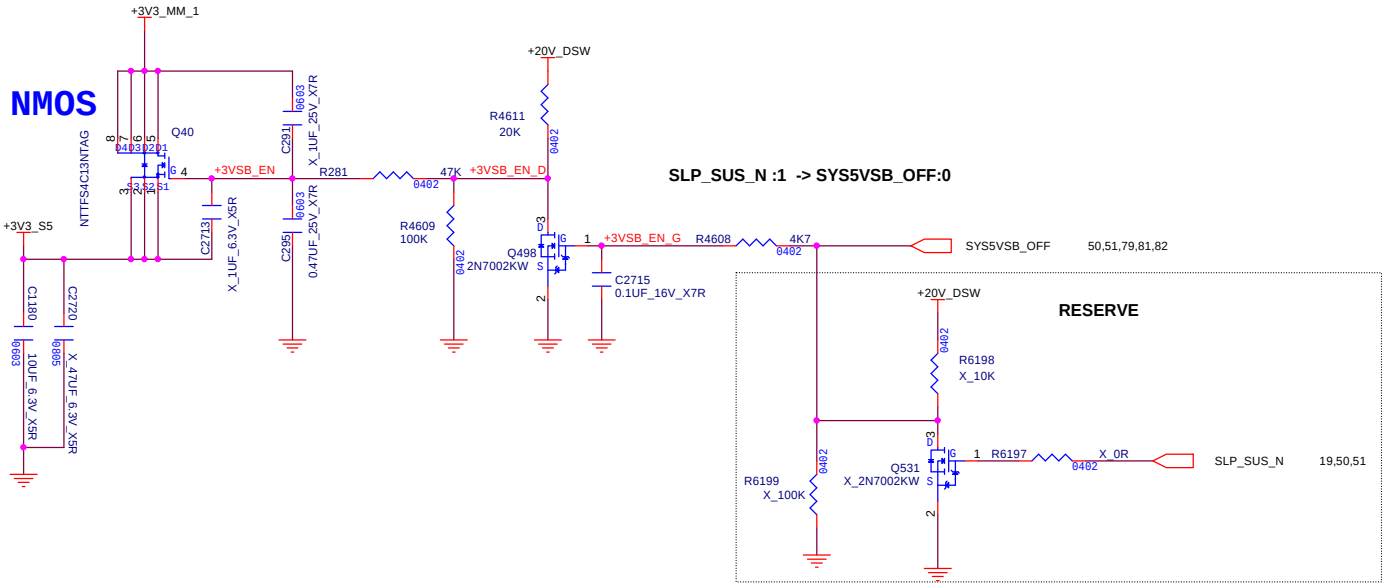


Parameter	Value
Iout.max	1.4A
OCP set point	4A
OCP formula	IC controlled
Switching Frequency	1MHz
Input ripple current	0.7A
Output ripple current	0.66A
Choke_size(L*W*H)(mm)	4.3*4.3*2.1
Choke_Isat	3.3A
Choke_DCR	48.0mΩ
Choke_LIR	39.0%
Input capacitance	10UF_6.3V_X5R_0603*1
Output capacitance	22UF_6.3V_X5R_0805*2

Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z V1P8_PCH			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 82 of 99	

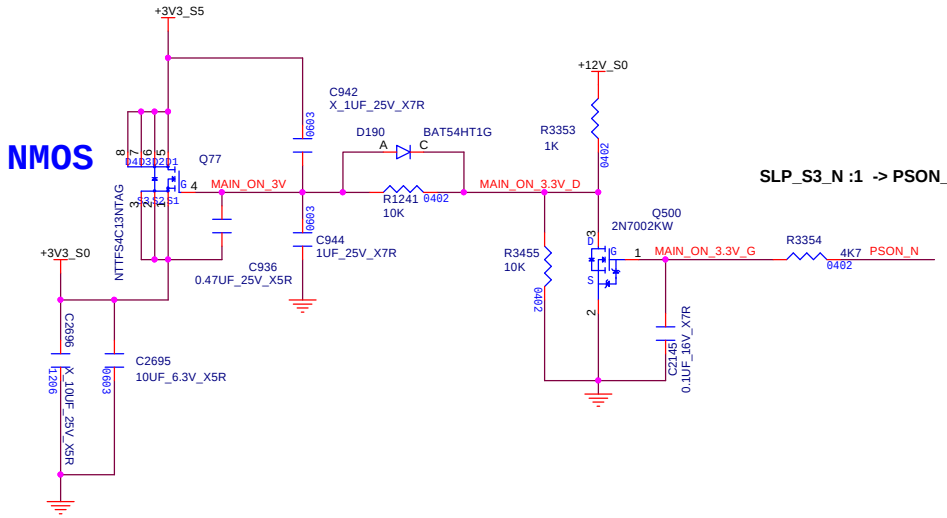
STANDBY POWER CONTROL

+3V3_S5

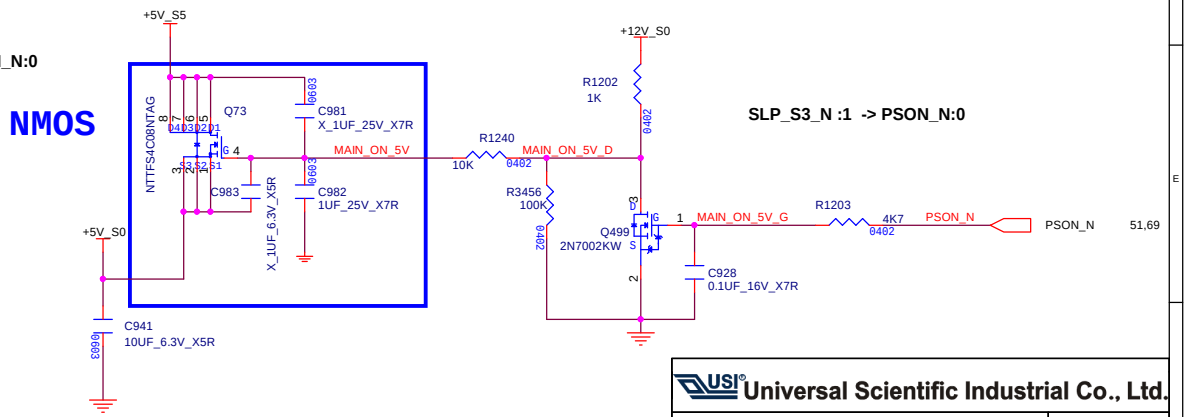


SYSTEM POWER CONTROL

+3V3_S0



+5V_S0

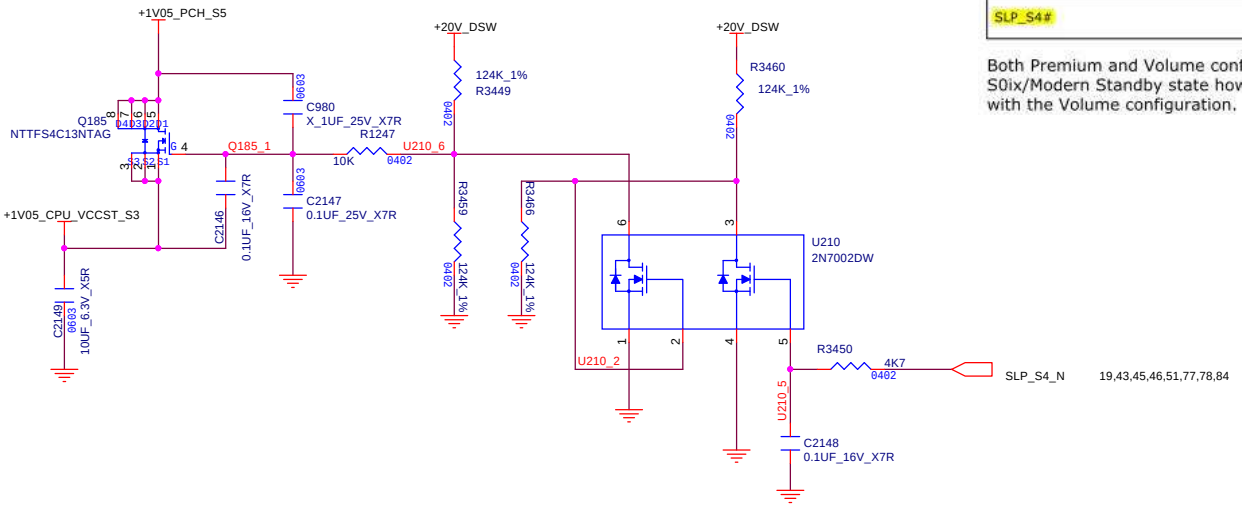


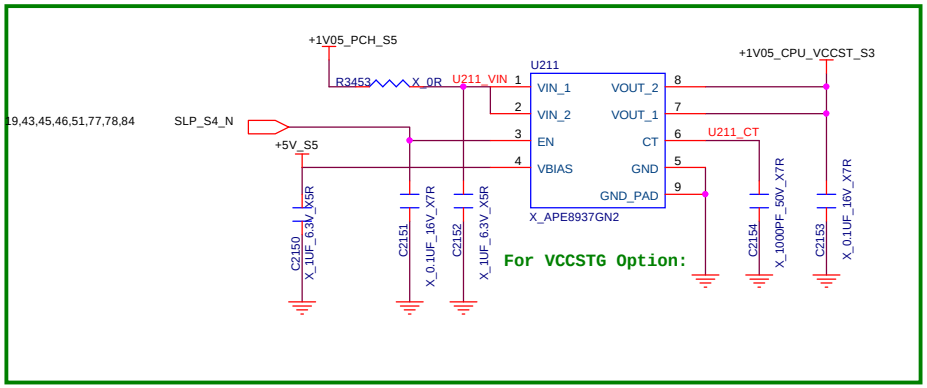
Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z VCC3/5V			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 83 of 99	

Enable Signal Implementations for VccST and VccPLL_OC

VccST Load Switch Enable	Supported VccPLL_OC Load Switch Enables
SLP_S3#	SLP_S3#, or {SLP_S3# AND CPU_C10_GATE#}
SLP_S4#	No gating required (tied to VDDQ), or SLP_S3#, or {SLP_S3# AND CPU_C10_GATE#}

Both Premium and Volume configurations can be used for systems that support the S0ix/Modern Standby state however power may be significantly higher in that state with the Volume configuration.



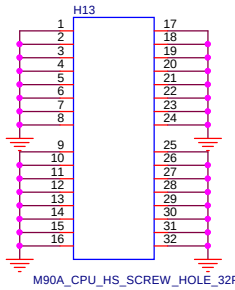


Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z VCCST			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 84 of 99	

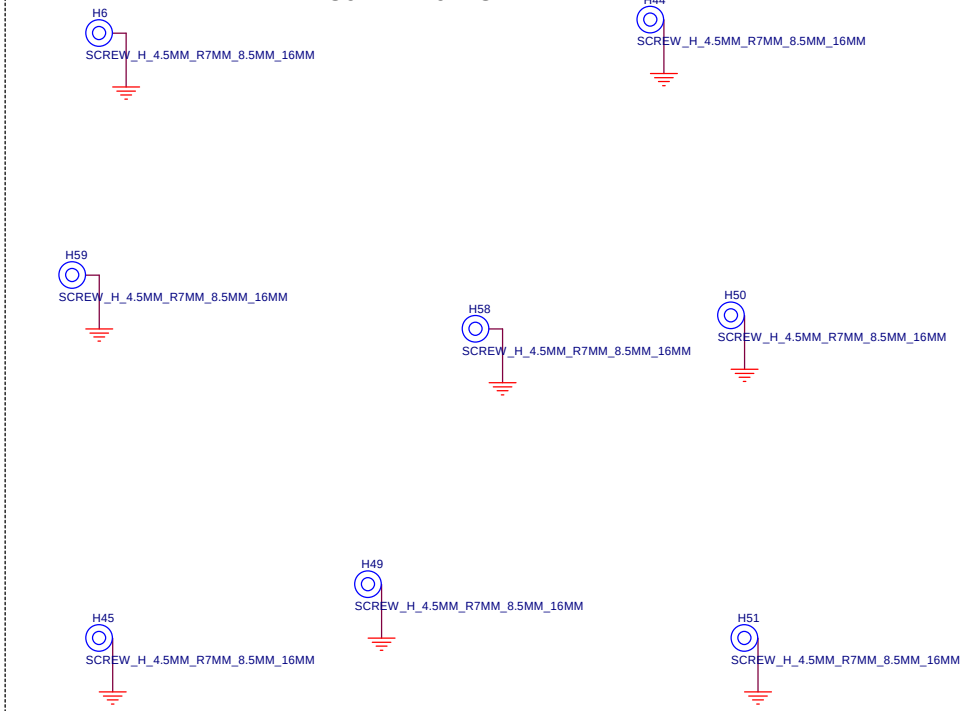
PCB SIZE: TOLERANCE +/-0.20 mm

FOR CPU

HEAT PIPE SCREW HOLES



SCREW HOLES



PCB SIZE: +/- 0.2 mm

Universal Scientific Industrial Co., Ltd.

TITLE: M90a/M838z HOLE_HEATSINK		REV: V0.3
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 85 of 99

Flexible IO Assign

2nd M.2 SSD

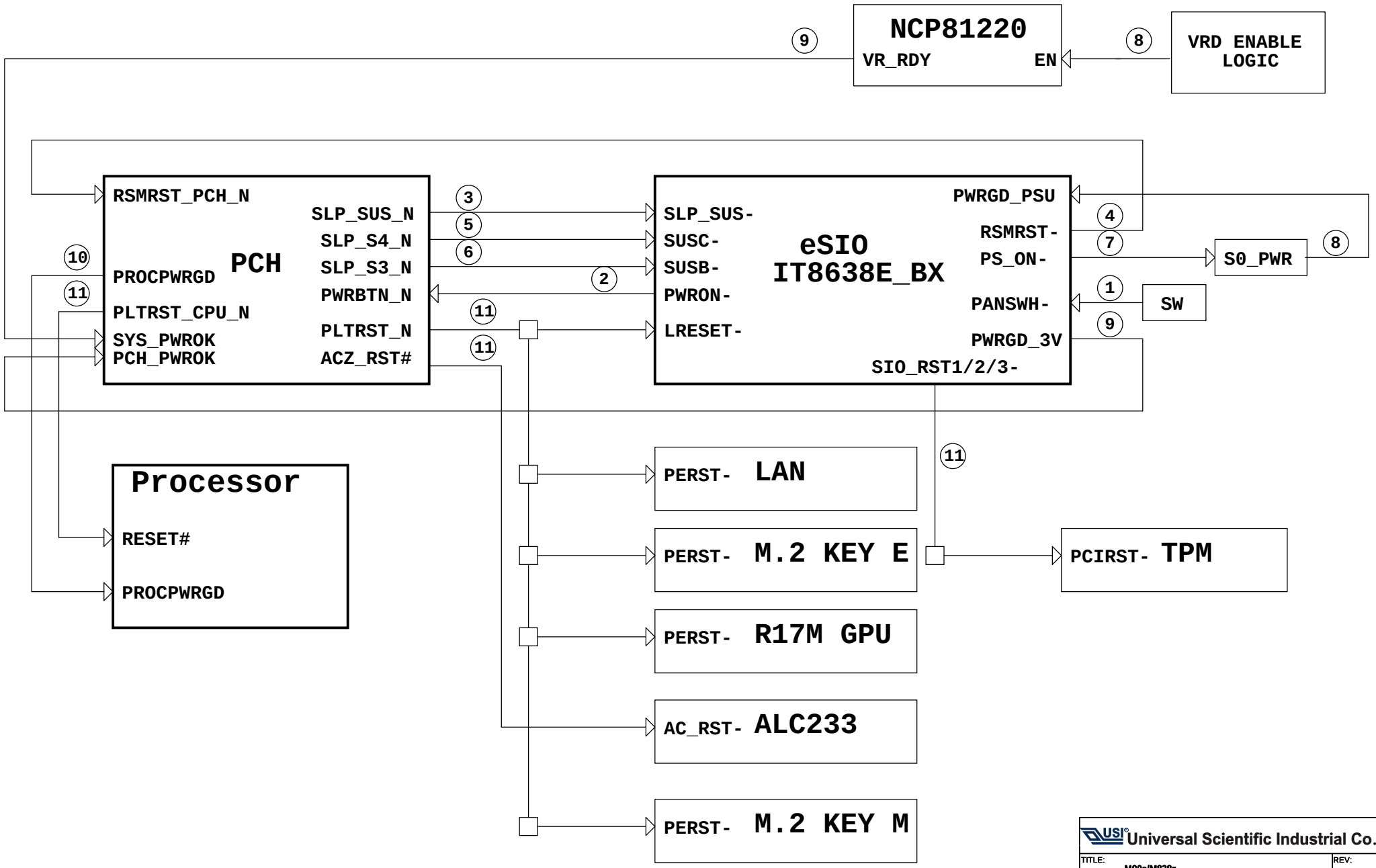
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
USB3.1# 1-GEN2	USB3.1# 2-GEN2 for M90a,GEN1 for M838z	USB3.1# 3-GEN1(TYPE-C)	USB3.1# 4-GEN1	USB3.1# 5-GEN1	USB3.1# 6-GEN1	USB3.0# 7	USB3.0# 8	USB3.0# 9	USB3.0#10	PCIe #5	PCIe #6	PCIe #7(M.2 WiFI)	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12	PCIe #13	PCIe #14	PCIe #15	PCIe #16	PCIe #17	PCIe #18	PCIe #19	PCIe #20
						PCIe #1	PCIe #2	PCIe #3	PCIe #4	GbE				GbE		SATA #0a	SATA #1a	SATA #0b	SATA #1b	SATA #2	SATA #3	SATA #4	SATA #5		
						X4				X4				X4				X4				X4			
						X2		X2		X2		X2		X2		X2		X2		X2		X2		X2	
						No Remapping								Intel PCIe Storage Device #1								Intel PCIe Storage Device #2			

1st M.2 SSD

27	28	29	30
PCIe #21	PCIe #22	PCIe #23	PCIe #24
X4			
X2		X2	
Intel PCIe Storage Device #3			

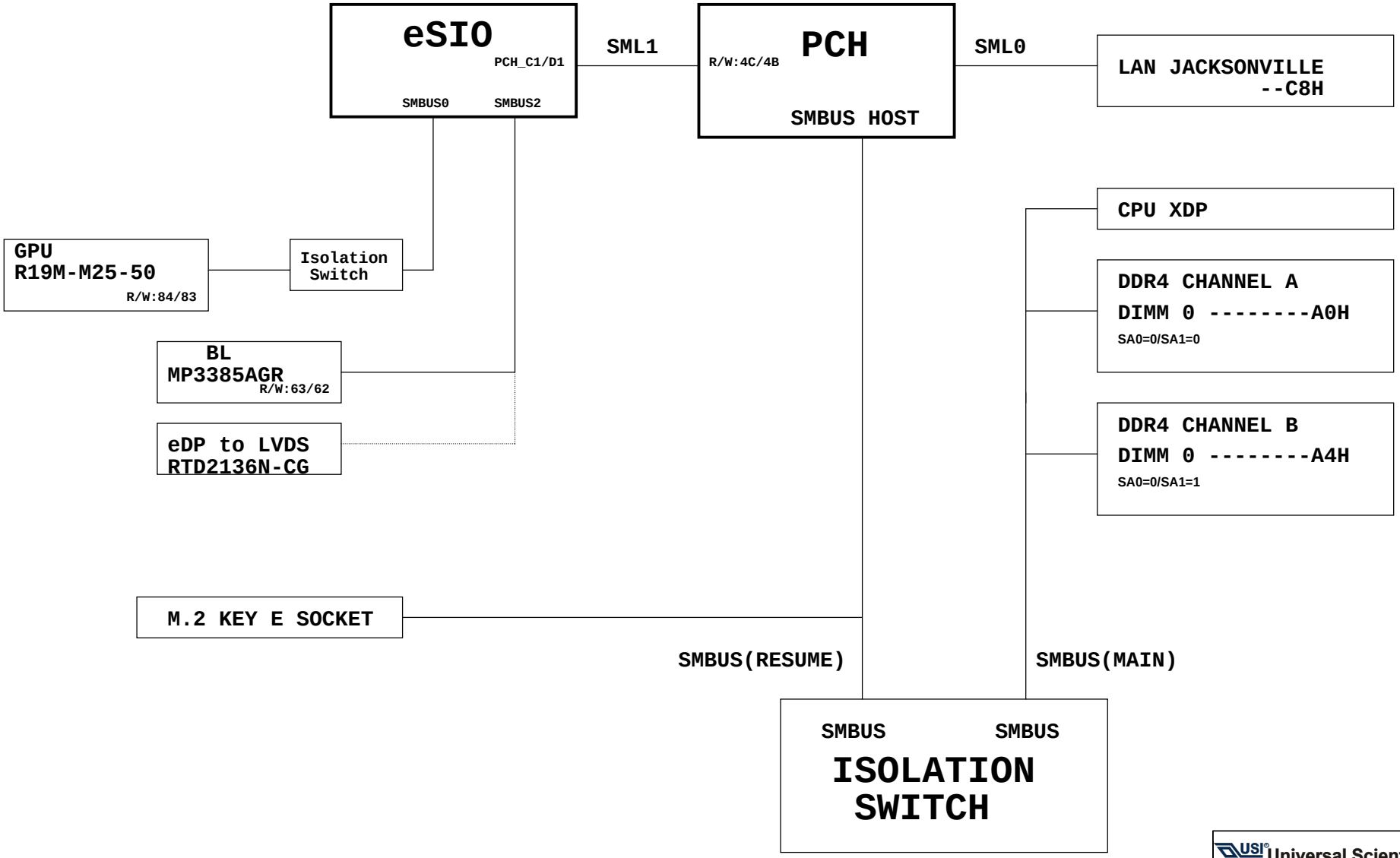
Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z FLEX. IO			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020		PAGE: 86 of 99

RESET MAP



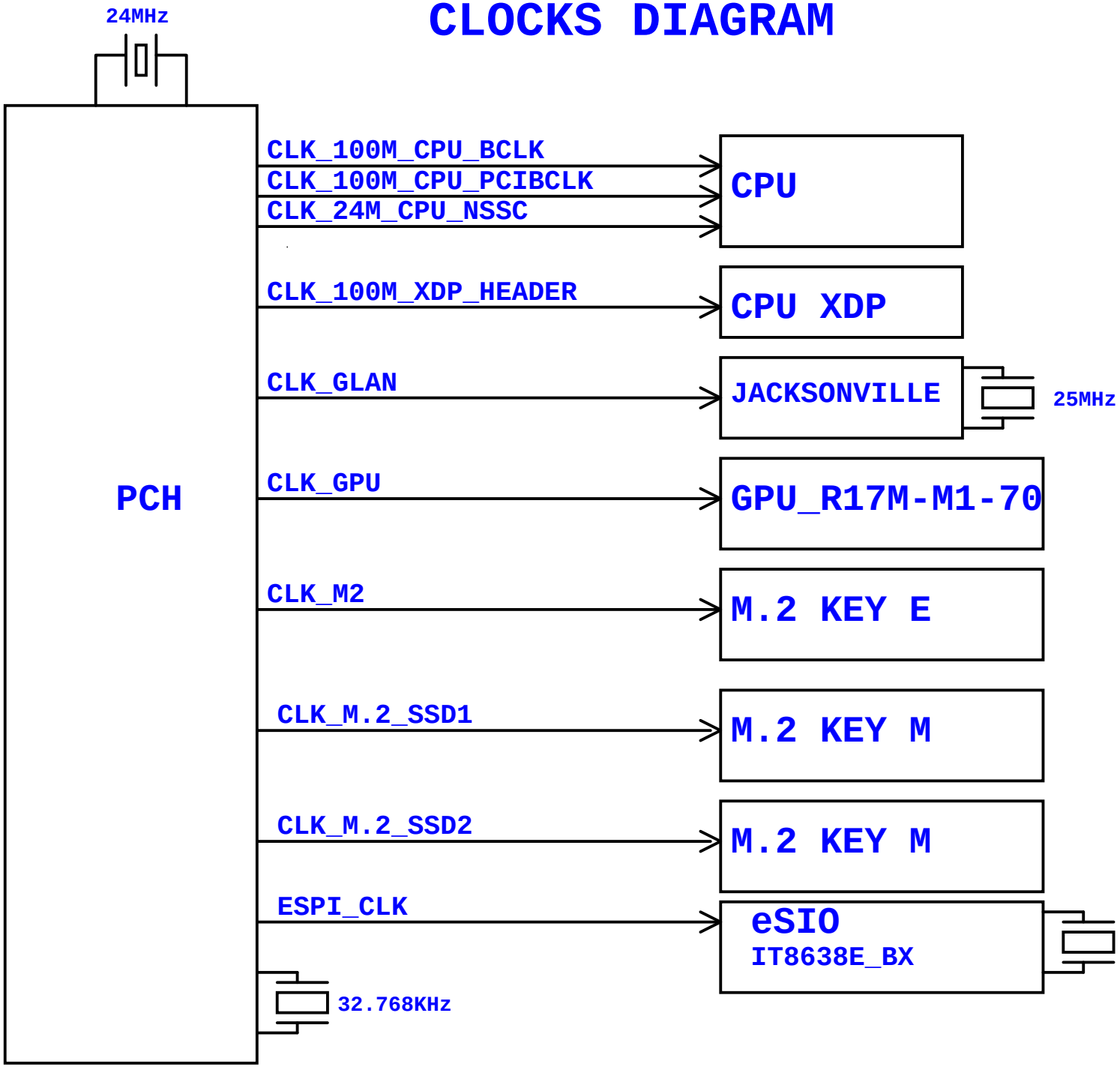
Universal Scientific Industrial Co., Ltd.			
TITLE: M90a/M838z RESET MAP			REV: V0.3
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Wednesday, January 15, 2020		PAGE: 87 of 99

SMBUS MAP



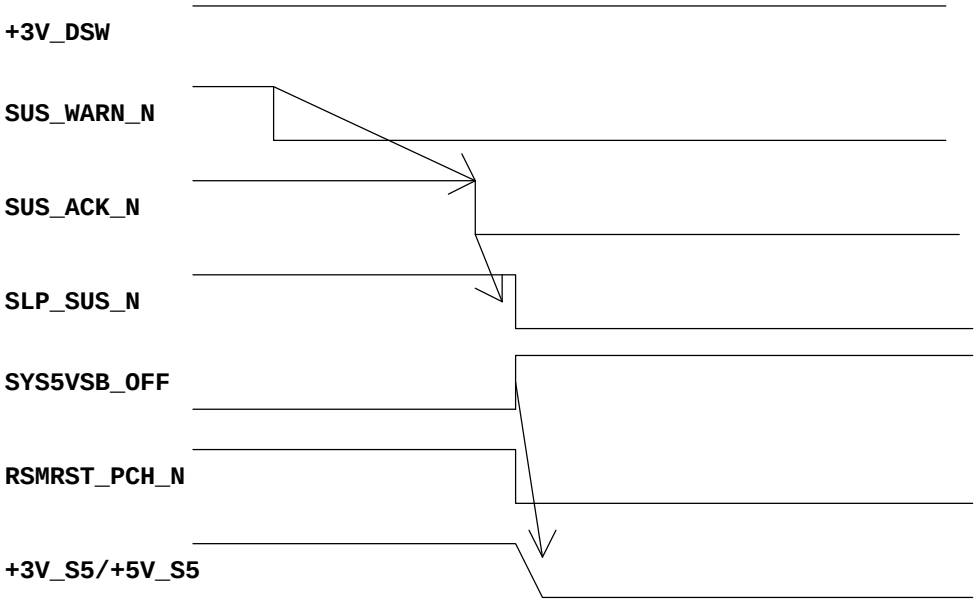
Universal Scientific Industrial Co., Ltd.		
TITLE: M90a/M838z SMBUS MAP		REV: V0.3
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 88 of 99

CLOCKS DIAGRAM

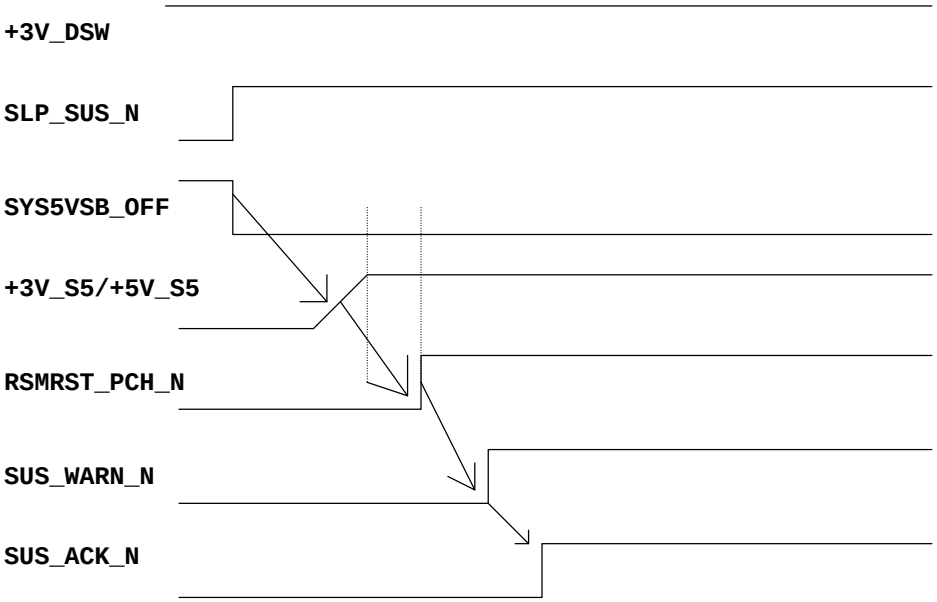


Universal Scientific Industrial Co., Ltd.		
TITLE: M90a/M838z CLOCK DISTRIBUTION		REV: V0.3
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Wednesday, January 15, 2020	PAGE: 89 of 99

Enter DSW State timing diagram



Exit DSW State timing diagram



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TITLE: M90a/M838z DSW SEQUENCING			REV: V0.3
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Prepared by : KERRY HUANG			
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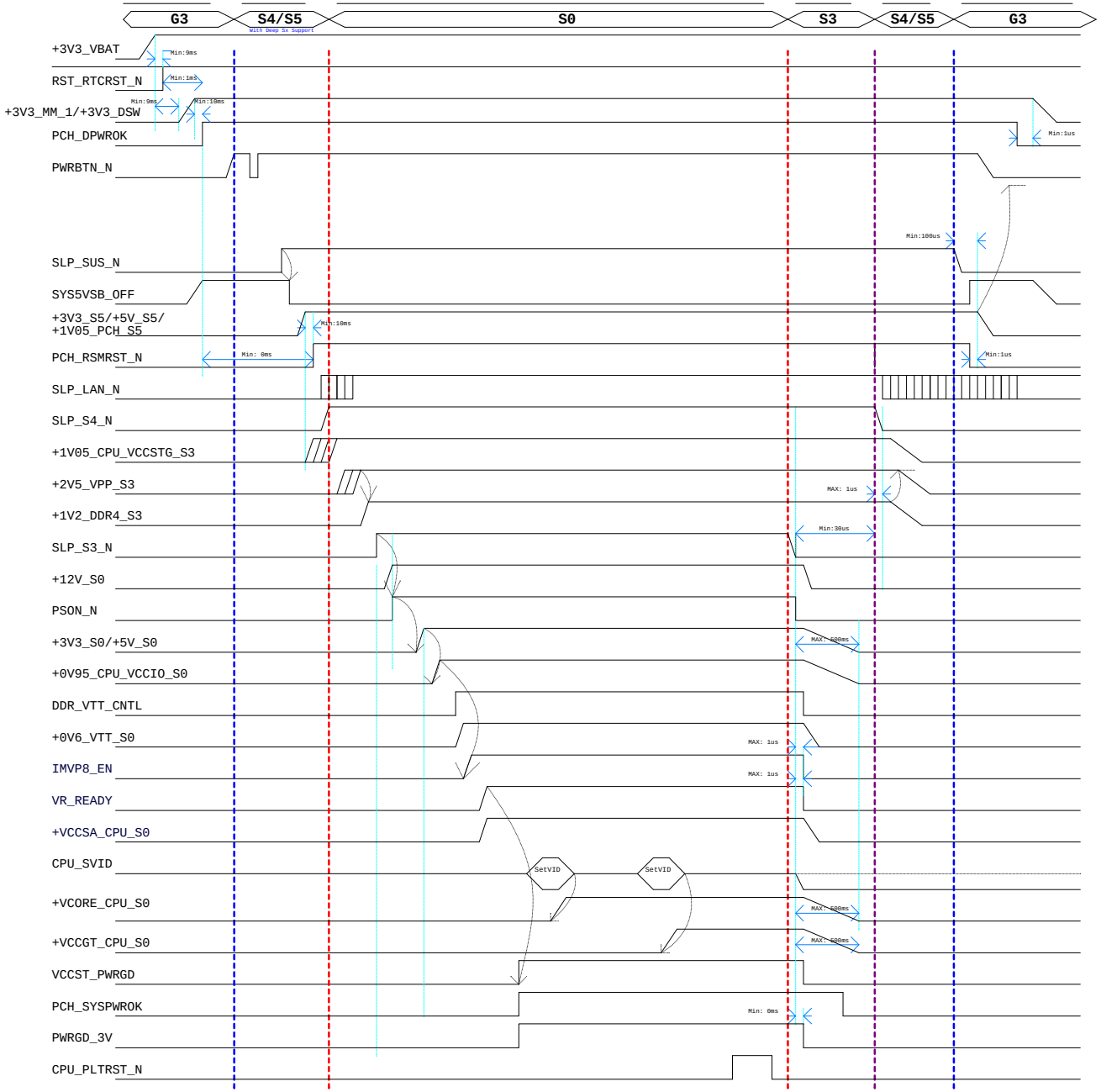

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TITLE: M90a/M838z POWER SEQUENCING		REV: V0.3
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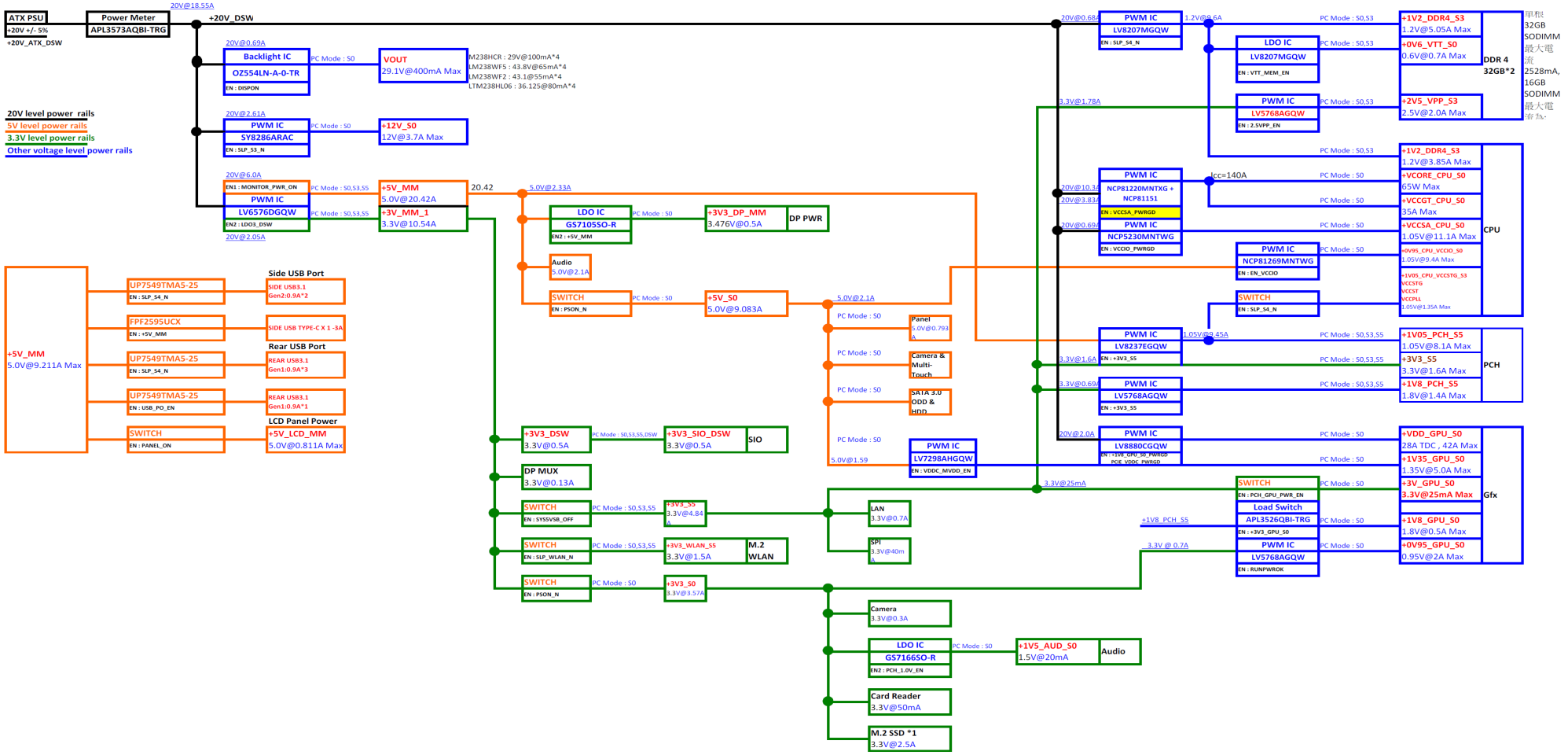
ATX PSU
+20V +/- 5%
+20V_ATX_DSW
Power Meter
APL3573AQBI-TRG
20V@18.55A
+20V_DSW
20V level power rails
5V level power rails
3.3V level power rails
Other voltage level power rails
20V@0.69A
Backlight IC
OZ554LN-A-0-TR
EN : DISPON
PC Mode : S0
VOUT
29.1V@400mA Max
M238HCR : 29V@100mA*4
LM238WF5 : 43.8V@65mA*4
LM238WF2 : 43.1@55mA*4
LTM238HL06 : 36.125@80mA*4
20V@2.61A
PWM IC
SY8286ARAC
EN : SLP_S3_N
PC Mode : S0
+12V_S0
12V@3.7A Max
20V@6.0A
EN1 : MONITOR_PWR_ON
PWM IC
LV6576DGQW
EN2 : LDO3_DSW
PC Mode : S0,S3,S5
+5V_MM
5.0V@20.42A
+3V_MM_1
3.3V@10.54A
20V@2.05A
20.42
5.0V@2.33A
LDO IC
GS7105SO-R
EN2 : +5V_MM
PC Mode : S0
+3V3_DP_MM
3.476V@0.5A
DP PWR
Audio
5.0V@2.1A
SWITCH
EN : PSON_N
PC Mode : S0
+5V_S0
5.0V@9.083A
5.0V@2.1A
PC Mode : S0
Panel
5.0V@0.793A
Camera & Multi-Touch
SATA 3.0 ODD & HDD
5.0V@1.59
PWM IC
LV7298AHGQW
EN : VDDC_MVDD_EN
+5V_MM
5.0V@9.211A Max
UP7549TMA5-25
EN : SLP_S4_N
SIDE USB3.1
Gen2:0.9A*2
Side USB Port
FPF2595UCX
EN : +5V_MM
SIDE USB TYPE-C X 1 -3A
UP7549TMA5-25
EN : SLP_S4_N
REAR USB3.1
Gen1:0.9A*3
Rear USB Port
UP7549TMA5-25
EN : USB_PO_EN
REAR USB3.1
Gen1:0.9A*1
SWITCH
EN : PANEL_ON
+5V_LCD_MM
5.0V@0.811A Max
LCD Panel Power
+3V3_DSW
3.3V@0.5A
PC Mode : S0,S3,S5,DSW
+3V3_SIO_DSW
3.3V@0.5A
SIO
DP MUX
3.3V@0.13A
SWITCH
EN : SYSSVSB_OFF
PC Mode : S0,S3,S5
+3V3_S5
3.3V@4.84A
SWITCH
EN : SLP_WLAN_N
PC Mode : S0,S3,S5
+3V3_WLAN_S5
3.3V@1.5A
M.2 WLAN
SWITCH
EN : PSON_N
PC Mode : S0
+3V3_S0
3.3V@3.57A
LAN
3.3V@0.7A
SPI
3.3V@40mA
Camera
3.3V@0.3A
LDO IC
GS7166SO-R
EN2 : PCH_1.0V_EN
PC Mode : S0
+1V5_AUD_S0
1.5V@20mA
Audio
Card Reader
3.3V@50mA
M.2 SSD *1
3.3V@2.5A
20V@0.68A
PWM IC
LV8207MGQW
EN : SLP_S4_N
1.2V@0.6A
LDO IC
LV8207MGQW
EN : VTT_MEM_EN
PC Mode : S0,S3
+1V2_DDR4_S3
1.2V@5.05A Max
+0V6_VTT_S0
0.6V@0.7A Max
DDR 4
32GB*2
3.3V@1.78A
PWM IC
LV5768AGQW
EN : 2.5VPP_EN
+2V5_VPP_S3
2.5V@2.0A Max
單根32GB SODIMM最大電流2528mA, 16GB SODIMM最大電流為
20V@10.3A
20V@3.83A
PWM IC
NCP81220MNTXG + NCP81151
EN : VCCSA_PWRGD
Icc=140A
+1V2_DDR4_S3
1.2V@3.85A Max
+VCORE_CPU_S0
65W Max
+VCCGT_CPU_S0
35A Max
+VCCSA_CPU_S0
1.05V@11.1A Max
+0V95_CPU_VCCIO_S0
1.05V@9.4A Max
+1V05_CPU_VCCSTG_S3
VCCSTG
VCCST
VCCPLL
1.05V@1.35A Max
CPU
20V@0.69A
PWM IC
NCP5230MNTWG
EN : VCCIO_PWRGD
PWM IC
NCP81269MNTWG
EN : EN_VCCIO
SWITCH
EN : SLP_S4_N
1.05V@9.45A
PWM IC
LV8237EGQW
EN : +3V3_S5
+1V05_PCH_S5
1.05V@8.1A Max
+3V3_S5
3.3V@1.6A Max
+1V8_PCH_S5
1.8V@1.4A Max
PCH
3.3V@1.6A
3.3V@0.69A
PWM IC
LV5768AGQW
EN : +3V3_S5
20V@2.0A
PWM IC
LV8880CGQW
EN : +1V8_GPU_S0_PWRGD
PCIE_VDDC_PWRGD
+VDD_GPU_S0
28A TDC , 42A Max
+1V35_GPU_S0
1.35V@5.0A Max
+3V_GPU_S0
3.3V@25mA Max
+1V8_GPU_S0
1.8V@0.5A Max
+0V95_GPU_S0
0.95V@2A Max
Gfx
3.3V@25mA
SWITCH
EN : PCH_GPU_PWR_EN
Load Switch
APL3526QBI-TRG
EN : +3V3_GPU_S0
PWM IC
LV5768AGQW
EN : RUNPWROK
+1V8_PCH_S5
3.3V @ 0.7A
PC Mode : S0
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TITLE:
M90a/M83Bz
POWER DELIVERY
REV:
V0.3
Document Number :
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Prepared by :
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Signal	Usage	When Sampled	Internal PU/PD	Definition		M90a/M838z Setting
				Set To	Description	
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	Weak PD	0	Disable “Top Swap” mode (Default)	0 (No external PD)
				1	Enable “Top Swap” mode	
GSPI0_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	Weak PD	0	Disable “No Reboot” mode	0 (PD R116 1K)
				1	Enable “No Reboot” mode	
SMBALERT# / GPP_C2	TLS Confidentiality	Rising edge of RSMRST#	Weak PD	0	Disable Intel ME Crypto Transport	1 (PU R499 4K7)
				1	Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality)	
GSPI1_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	Weak PD	0	SPI	0 (No external PD)
				1	LPC	
SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	Weak PD	0	LPC Is selected for EC	1 (PU R145 4K7)
				1	eSPI Is selected for EC	
SPI0_MOSI	BOOT HALT	Rising edge of RSMRST#	Weak PU	0	ENABLE	1 (No external PU)
				1	DISABLED	
GPP_H15 / SML3ALERT#	JTAG ODT	Rising edge of PCH_PWROK		0	ODT DISABLE	1 (PU R5153 100k)
				1	ODT ENABLE	
SPI0_MISO	JTAG ODT	Rising edge of PCH_PWROK	Weak PU	0	ODT DISABLE	1 (no external PD)
				1	ODT ENABLE	
GPP_B23 / SML1ALERT# /	Intel® DCI-OOB	Rising edge of RSMRST#	Weak PD	0	Disable Intel® DCI-OOB (Default)	1 (PU R97 4K7)
				1	Enable Intel® DCI-OOB	
SPI0_IO2	Reserved(CONSENT)	Rising edge of RSMRST#	Weak PU	0	ENABLE	1 (PU R223 1K)
				1	DISABLE	
SPI0_IO3	PESONALITY	Rising edge of RSMRST#	Weak PU	0	ENABLE	1 (PU R224 1K)
				1	DISABLE	
HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	Weak PD	0	Enable security measures defined in the Flash Descriptor	0 (No external PD)
				1	Disable Flash Descriptor Security (override)	
GPP_H12 / SML2ALERT#	eSPI Flash Sharing Mode	Rising edge of RSMRST#	Weak PD	0	MAFS	0 (No external PD)
				1	SAFS	
DDPB_CTRLDATA / GPP_I6	Display Port B Detected	Rising edge of PCH_PWROK	Weak PD	0	Port B is not detected	0 (No external PD)
				1	Port B is detected	
DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	Weak PD	0	Port C is not detected	0 (No external PD)
				1	Port C is detected	
DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	Weak PD	0	Port D is not detected	1 (PU R593 2K2)
				1	Port D is detected	
GPP_F23	Display Port F Detected	Rising edge of PCH_PWROK	Weak PD	0	Port D is not detected	0 (No external PD)
				1	Port D is detected	
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	Weak PD	0	38.4 XTAL frequency selected. (Default)	1 (PU R4991 4K7)
				1	24MHz XTAL frequency selected.	
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#		0	Integrated CNVi enable.	1 (PU R4990 20K)
				1	Integrated CNVi disable	
GPP_J9	1.8V VCCPSPI	Rising edge of RSMRST#	Weak PD	0	VCCSPI is connected to 3.3V rail	0 (No external PD)
				1	VCCSPI is connected to 1.8V rail	
GPD7	Reserved	Rising edge of DSW_PWROK	Weak PD	0	XTAL INPUT IS SINGLE-ENDED	1 (PU R4981 1K)
				1	XTAL IMPUT IS DIFFERENTIAL	

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Document Number : <Doc>		
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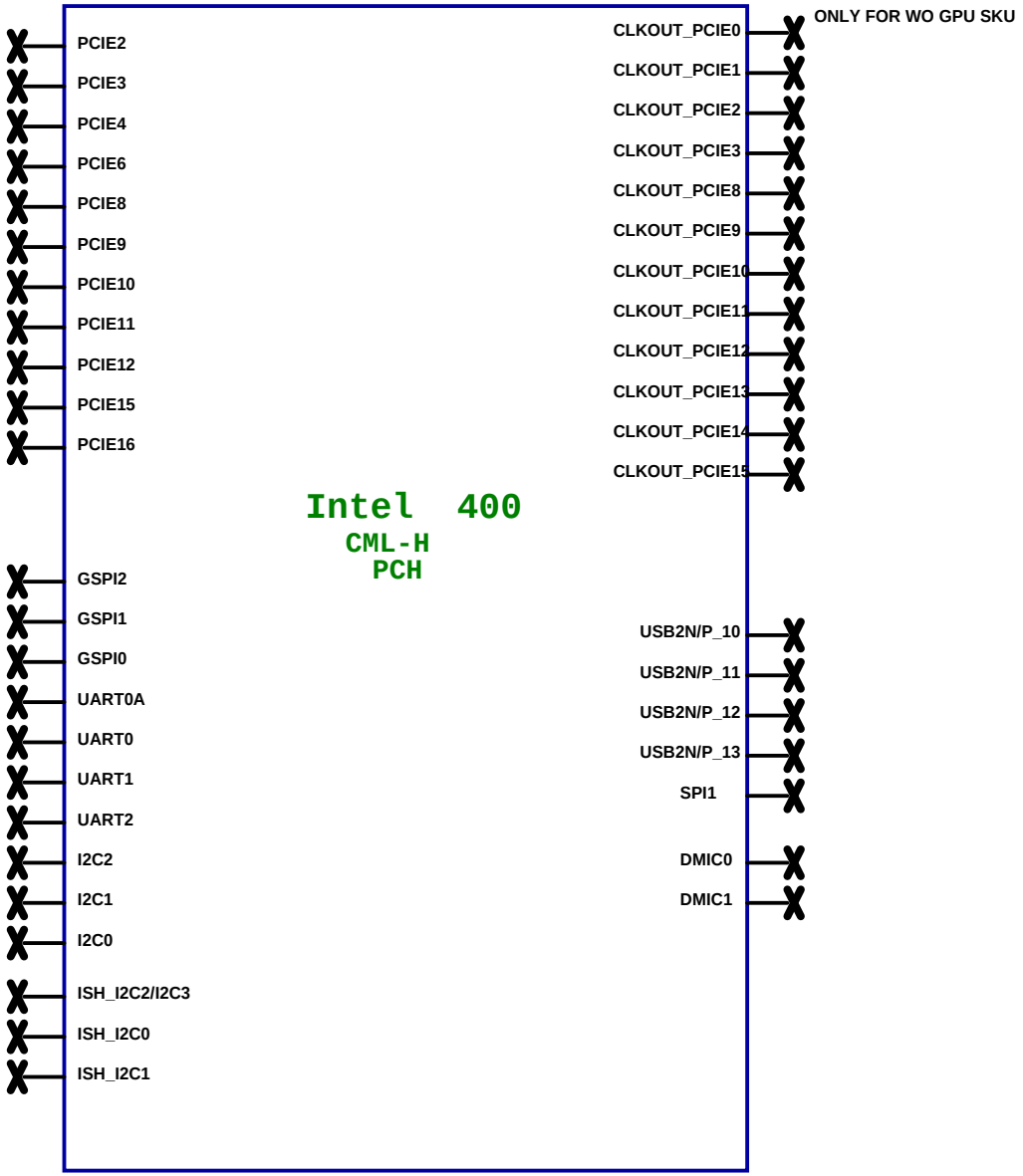

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TITLE: M90a/M838z UNUSED I/F		REV: V0.3
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V0.15 to V0.2 CHAGNE LIST

page04:nopop C51 100pFand R6267 20R to plan fix Monotonic for CPU_PLTRST_N
page04:nopop R35 1K to set PEG x16 *1 for PEG X8 X8 CPU ES issue
page04:nopop R51 and pop R5183
page16:change C3591 C3592 from 0402 to 0201 size for placement
page19:add R6261 ,R6262,R6263 100K PD to follow PDG requirement
page19:change R142 R146 from 10K toi 100K to follow PDG requirement
page19:change R109,R110 from 33R to 0R to fix slew rate fail
page21:add R6264 100K PD to follow PDG requirement
page21:change C3347 C3348 C3480 C3479 from 0402 to 0201 size for better G2 RX
page21:R4628,R4629,R4630,R4631 from 0R to 33R to fix undershoot fail
page22:change C3253 from 1uF to 4.7uF to fix +3V3_S5 drop
page33:change HDD stand-off type for AVC requriement
page34:change R5338 0R to 100R ,C199 from 220pF to 33pF for slew rate finetune >50mV/ns
page35:change R3495 0R->100R ,C2653 from 1000pF to 33 pF for slew rate finetune >50mV/ns
page36:remove 2nd M.2 SSD for GPU sku.
page36:change C3696 from 1000pF to 150pF for slew rate finetune >50mV/ns
page44:reserve U338 TYPE-C load switch for second source
page47:add R6265 100K PD to follow PDG requirement
page47:add C4014 0.47uF to fix +3V3_LAN_S5 drop fail
page48change C3571 C3572 C3940 C313 C3576~C3580,C3538,C3537,C3574 C3575 C3941 C3942 from 0402 to 0201 size for better placement
page48:change R530 0R->100R ,C308 from 220pF to 33 pF for slew rate finetune >50mV/ns
page48:change R5618 R5619 R5620 R5621 75R to 0R ,R5617 0R to 75R for better surger protection
page51:change C1202 from 680pF to 150pF for slew rate finetune >50mV/ns
page51:nopop XS4 32.768KHZ crystal confirmed OK from ITE
page61:pop R6268 10K to follow AMD requirement
page63:reserve Q534,Q535 for +VDD_GPU_S0
page65:change C3891 from 1UF to 0.47UF to finetune GPU power timing
page65:add C4016 0.47uF for +3V3_GPU_S0 SS
page68:change R940 from 1mohm to 2mohm for INA300 voltage limit
page68:change R6183 6K98->4K22,R153 5K23->3K16,R941 4K53->2K74,R6182 4K12->2K49 for OBP finetune
page69:pop C629 4700pF 0402 for +12V_S0 component stress fine-tune
page70:C731 330pF for Vcore LL fine-tune
page70:R980 160Kohm for Vcore LL fine-tune
page70:R1001 2.8Kohm for VCCGT LL fine-tune
page70:R1003 215Kohm for VCCGT LL fine-tune
page70:C744 100pF for VCCGT LL fine-tune
page79:nopop C3618 to fix +5V_S5 glitch
page75:change C1222 2200PF to 4700pF , R5712 from 1R to 3R3 to fix +0V95_CPU_VCCIO_S0, Driver voltage stress, Boost-Phase are Fail
page81:R1154 --> 45K3 1% 0402 for +1V05_PCH_S5 OCP fine-tune
page83:C936 --> 0.47uF for +3V3_S0 switch soft-start

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V0.1 to V0.15 CHAGNE LIST

page18:change R91 from 1M to 200K to follow CRB design.
page20:add GPP_B15~17 for TOF
page25:add JP54 TOF header for Lenovo requirement
page30: remove reserve CMC for LVDS connector placement to meet AVC requirement
page31: nopop Q100,R1168 and add R6258 0R to change LCD_BKLTEN from low to high active to avoid "unable to turn off BL converter issue".
page34: remove CNVI series 0R to decrease via number
page51:add GP37 for TOF for Lenovo requirement
page51:reserve Q533 for adapter detection for Lenovo requirement
page52:change JP18 from vertical to R/A type for AVC requirement
page53:add two COM port stand-off for AVC requirement
page30: remove SW4 spype button for Lenovo requirment
page55~64: change GPU from R17M* to R19M* for Lenovo requirement
page68: add adapter detection circuit for Lenovo requirement
page72: change R6173 from 10mohm to 2mohm for iPCM
page81: nopop C3320 1UF to fix +1V05_PCH_S5 rising time too slow
page83: change R281 from 10k to 47K to fix G3->S5 +3V3_S5 glitch

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V0.2 to V0.3 CHAGNE LIST

page03:nopop XDP connector
page04:pop C51 120pF to fix CPU_PLTRST_R_N overshoot
page11:pop R5297 100K to fix SLP_S0_N no-montonic
page12:change C2175 4.7U->10UF and R59 R63 2K->1K to fix DIMM_CA_VREF_A ripple fail
page14:change C2176 4.7UF-> 10UF and R60 R64 2K->1K to fix DIMM_CA_VREF_B ripple fail
page20:nopop R6115 R6116 0R due to no use ISH
page24:add R6287 10K,U339 16pin 32MB SPI BIOS and socket for M90a
page24:nopop R1169 1K due to U304 with discharge function
page31:change R3364 300K->33K,C333 1000PF->0.068UF to fix INNLUX min. brightness fail
page40:change JP37 touch HD from R/A to vertical for AVC requirement
page43:change P5,P6 connector from yellow to black color for Lenovo requirement
page45:change P14 connector from yellow to black color for Lenovo requirement
page46:change P13 connector from yellow to black color for Lenovo requirement
page46:reserve U340 FPF2595UCX and related circuit for 15W wireless charger for P13 top USB port
page48: remove R5618~R5621 0R and change R5617 from 0402 to 0805 for better LAN surge protection
page48: change C4024 C4025 0.1uF for EMI
page51:change R6272,R6273,R6274,R6275 33R to 100R to fix EC SPI flash overshoot
page51:reserve Q536 2N7002,R6290 100K and add R6288 0R ,R6289 1K_1%, C4020 0.1UF for auto disable M.2_DISABLE1_N
page51:connect TOF_CABLE_DET_N to U39 PIN1 for TOF
page51:change GPU SMBUS from SMBUS0 to SMBUS4 and add R6281 R6282 0R,R6283 R6284 4K7 for TOF
page51:nopop R1335 R1336 0R ,add R6279 R6280 0R and add TOF_SMBUS_DATA/CLK to SMBUS0 for TOF
page51:add R6285 10K,R6286 X_10K for BL_IC_ID
page51:connect PANEL_ON to U39 PIN97 for TOF
page51:change R5179 from 0R to 100R to fix SLP_S0_N overshoot fail
page51:change R6272,R6273,R6274,R6275 100R->130R to fix SI overshoot fail.
page54:change JP53 EP HD type to avoid mix with C2 header
page62:change Q514 from 3904 to 2N7002 to fix C BOM GB 60 degree fail
page63:change L268,L267 from 0.22UH to 0.3UH and R6019,R6028 110R to 64R9 ,R5993 R6002 2R2->1R to fix +VDD_GPU_S0 efficiency fail
page65:change R6056 470R->100R and C4016 0.47uF ->68nF,nopop C3722,R6064 100K to 20K for GPU power down timing
page66: add CE105 220UF,change R6073 1K to 7K32 to fix +1V35_GPU_S0 ripple fail
page66:reserve D185 for surge protection
page68:add R6299 R6300 R6301 R6302 for OBP fine-tune
page68:change R6183 6k34_1% ,R153 4k53_1%,R941 4k02_1%,R6182 3k571% for OBP fine-tune
page68:change Q529 Q527 Q528 Q530 from 2N7002 to PM5Q2EA with lower Rds(on) for better OBP precision
page68:change P12 DC-IN connector from yellow to black color for Lenovo requirement
page68:change R940 from 2m ohm to 10m ohm for better OBP precision
page70:nopop C714 0.47UF to fix rising timing too slow
~~page77:pop C3236 0.047uF to fix tPLT20 timing fail~~
page77:nopop C3236 0.047uF and pop C3237 0.047uF to fix tCPU18 timing fail (DDR_VTT_VCNTL to DDR VTT max. 35us)) and MSB fail
page83: change C295 from 1U to 0.47U to fix +3V3_WLAN_S5 rising time fail ,spec: <10ms
page97: connect net PANEL_ON to TOF header JP54 pin6

8845-510780-00	8845-510781-00	8845-510790-00	8845-510860-00	8845-510850-00	8845-510870-00
M90a w/ GPU	M90a w/ GPU	M90a w/o GPU	M838z w/ GPU	M90a w/o GPU- B BOM	M838z w/ GPU- C BOM
~~GD25B256DFIR~~	W25Q256JVFIQ	GD25B256DFIR	MX25L12872FM2I-10G	MX25L25673GMI-08G	W25Q128JVSIQ
GD25B127DSIGR	W25Q128JVSIQ	GD25B127DSIGR	MX25L6473FM2I-08G	MX25L12872FM2I-10G	W25Q64JVSSIQ
SAMSUNG	Micron		Micron		SAMSUNG
GDDR					
w/ BIOS socket J20/J18		w/ BIOS socket J20/J18		w/ BIOS socket J20/J18	

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V0.3 to V1.0 CHAGNE LIST

page10: reserve C4028~C4032 47uF for +VCORE_CPU_S0 , reserve C4033~C4035 47uF for +VCCGT_CPU_S0 due to intel Gen5 VRTT tool updated

page31:change R3364 from 33K_1% to 27k_1% to fix INNLUX min. brightness 30 nits fail --ED057483

page31: add CE106 47 uF to fix 600HZ modulation EE noise fail -ED057514

page38: change D9,D10 from TVNS52301AB0 to ESD207-B1-02EL for better ESD protection-ED057483

page39:change JP42 from 16 pin to 13pin for better cable routing -ED057366

page39:remove reserve U19 ESD and add reserve D188 D189 ESD for better USB2.0 routing-N/A

page51:add net EC_MIC_MUTE_MS to EC GP36 and EC_MIC_MUTE to EC GPA0 to avoid MUTE LED off when audio enters D3-N/A

page54:pop R1387 10K ,R6312 0R ,R5252 0R to to avoid MUTE LED off when audio enters - D3ED057366

page68: change C700 C701 C702 from 10uF 1206 to 4.7uF 0805 and add C3541 C3937 C4042 4.7uF 0805 to fix SPL EE noise -ED057514

page68: change +20V_CPU_VIN_DSW MLCC from 10uF 1206 to 4.7uF 0805 size to fix SPL EE noise -ED057514

page70:change R977,R981,R983,R4683 from 1% to 0.5% ,C731 from 330pF to 680pF for +VCORE_CPU_S0 AC LL fine-tune（new fast slew VRTT） -ED057514

page70:change R1000 from 54K9_1% to 69K8_0.5%,C745 from 1200pF to 1000pF +VCCGT_CPU_S0 AC LL fine-tune（new fast slew VRTT） -ED057514

page73:pop CE99 560uF for +VCCGT_CPU_S0 AC LL（new fast slew VRTT） -ED057514

page73: remove C782 1uF 0805,C783 10uF 1206 to fix SPL EE noise -ED057514

page74: change C796 1UF 0805->4.7UF 0805,C797 10UF 1206 ->4.7UF 0805 to fix SPL EE noise -ED057514

page77:nopop C3236 0.047uF and pop C3237 0.047uF to fix tCPU18 timing fail (DDR_VTT_VCNTL to DDR VTT max. 35us)) and MSB fail -ED057366

USI P/N	4551-510790-00	4551-000780-00	4551-000781-00	4551-000770-00
SKU	M90a UMA MB	M90A_LI w/ GPU MB	M90A_LC w/ GPU MB	M838z MB W/GP
GDDR	N/A	SAMSUNG	MICRON	MICRON
FLASH	32M+16M	32M+16M	16M+16M	16M+8M
TPM	TPM	TPM	N/A	N/A

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