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Project Code & Schematics Subject:

PCB P/N:

P. Leader	Check by	Design by

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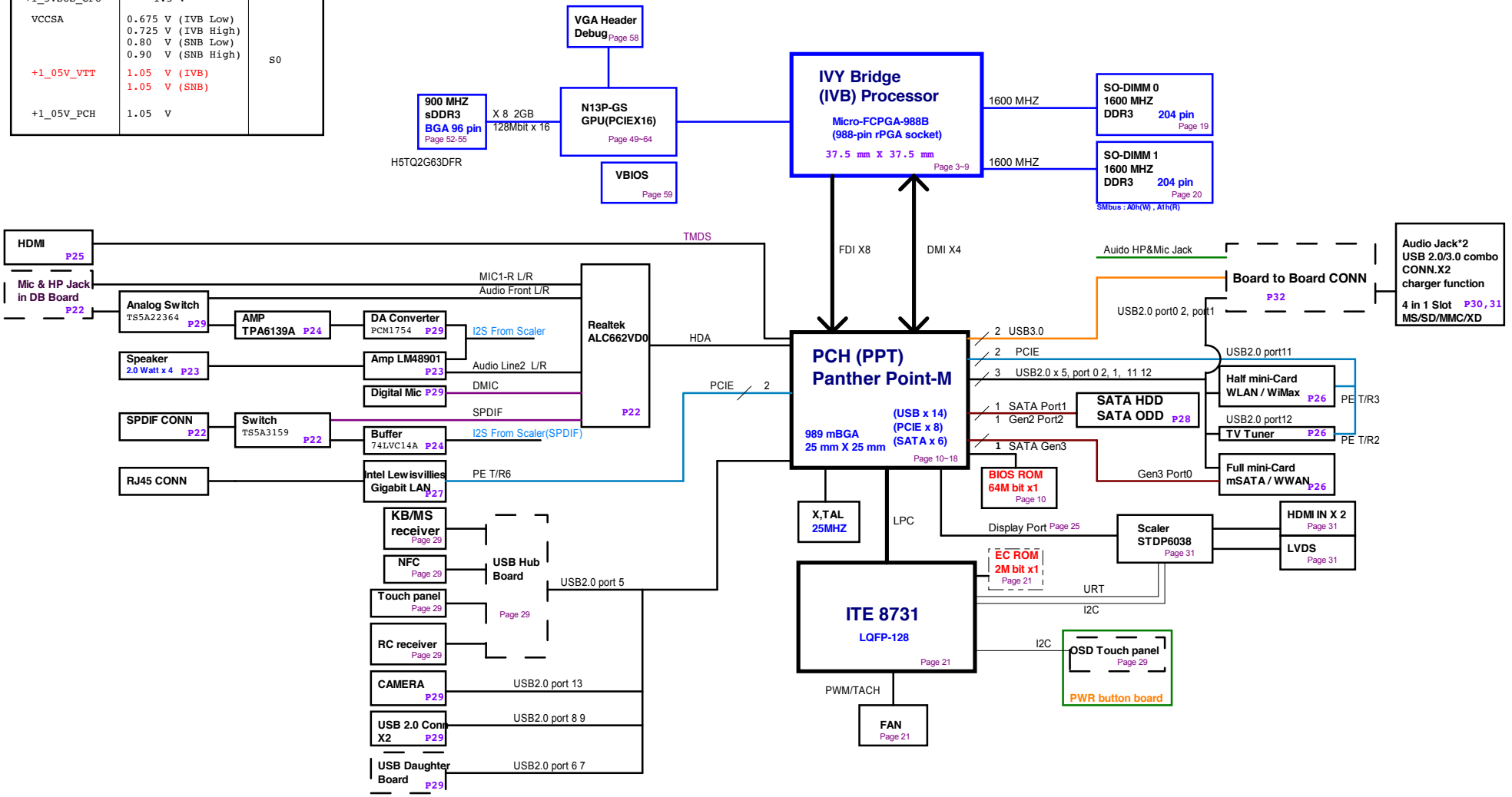
Everest Chief River Platform

POWER PLANE	Voltage	Voltage Rials Actice In
+1_5VSUS_CPU	1.5 V	
VCCSA	0.675 V (IVB Low) 0.725 V (IVB High) 0.80 V (SNB Low) 0.90 V (SNB High)	S0
+1_05V_VTT	1.05 V (IVB) 1.05 V (SNB)	
+1_05V_PCH	1.05 V	



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Title: BLOCK DIAGRAM

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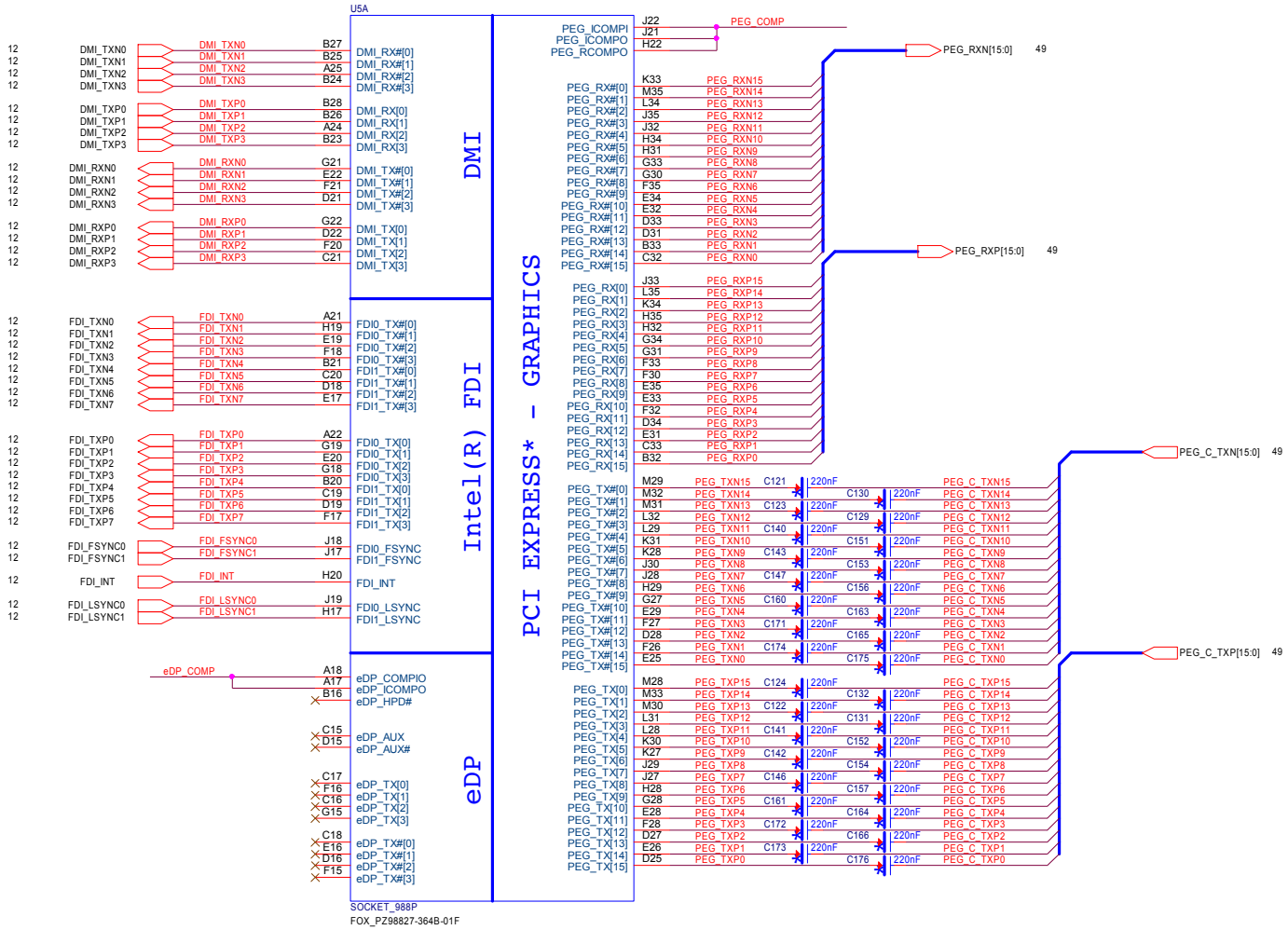
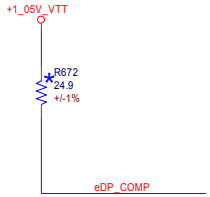


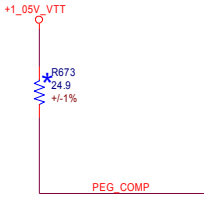
7/13 [TA00 DVT] Change to 988B socket.

DP Compensation



Layout NOTE: DP_COMPIO and ICOMPO signals should be shorted near balls and routed with
- typical impedance < 25 mohms

PEG Compensation



Layout NOTE: PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils
- typical impedance = 43 mohms

PEG_ICOMPO signals should be routed with
- max length = 500 mils
- typical impedance = 14.5 mohms

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Title: IVB (DMI,PEG,FDI)			
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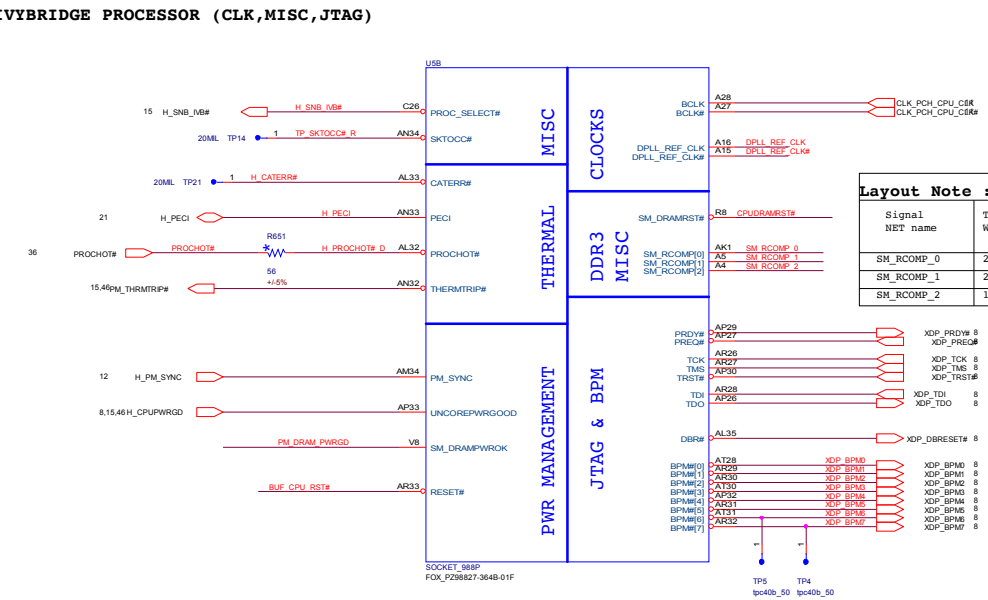
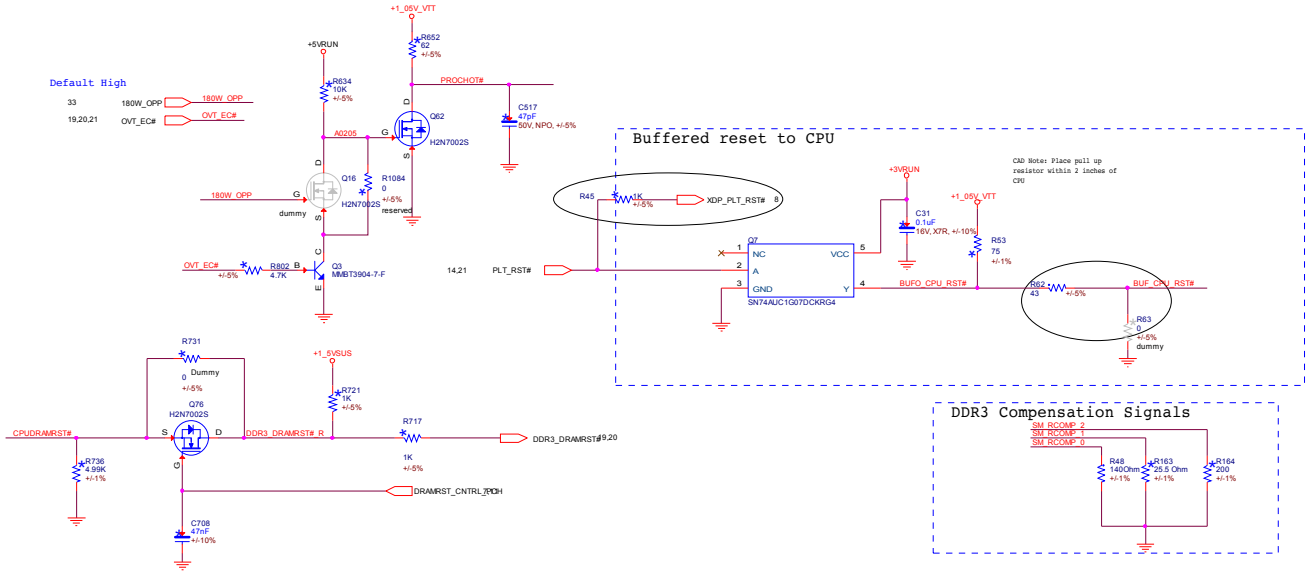
IVYBRIDGE PROCESSOR (CLK,MISC,JTAG)



Layout Note : SM_RCOMP

Signal NET name	Trace Width	Isolation Spacing	Resistor Value (Pull Down to GND)	Length
SM_RCOMP_0	20 mils	20 mils	140ohm within 1%	Max = 500 mils
SM_RCOMP_1	20 mils	20 mils	25.5ohm within 1%	Max = 500 mils
SM_RCOMP_2	15 mils	20 mils	200ohm within 1%	Max = 500 mils

Intel Updated PM_DRAM_PWRGD



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Title	IVB (CLK,MISC,JTAG)	
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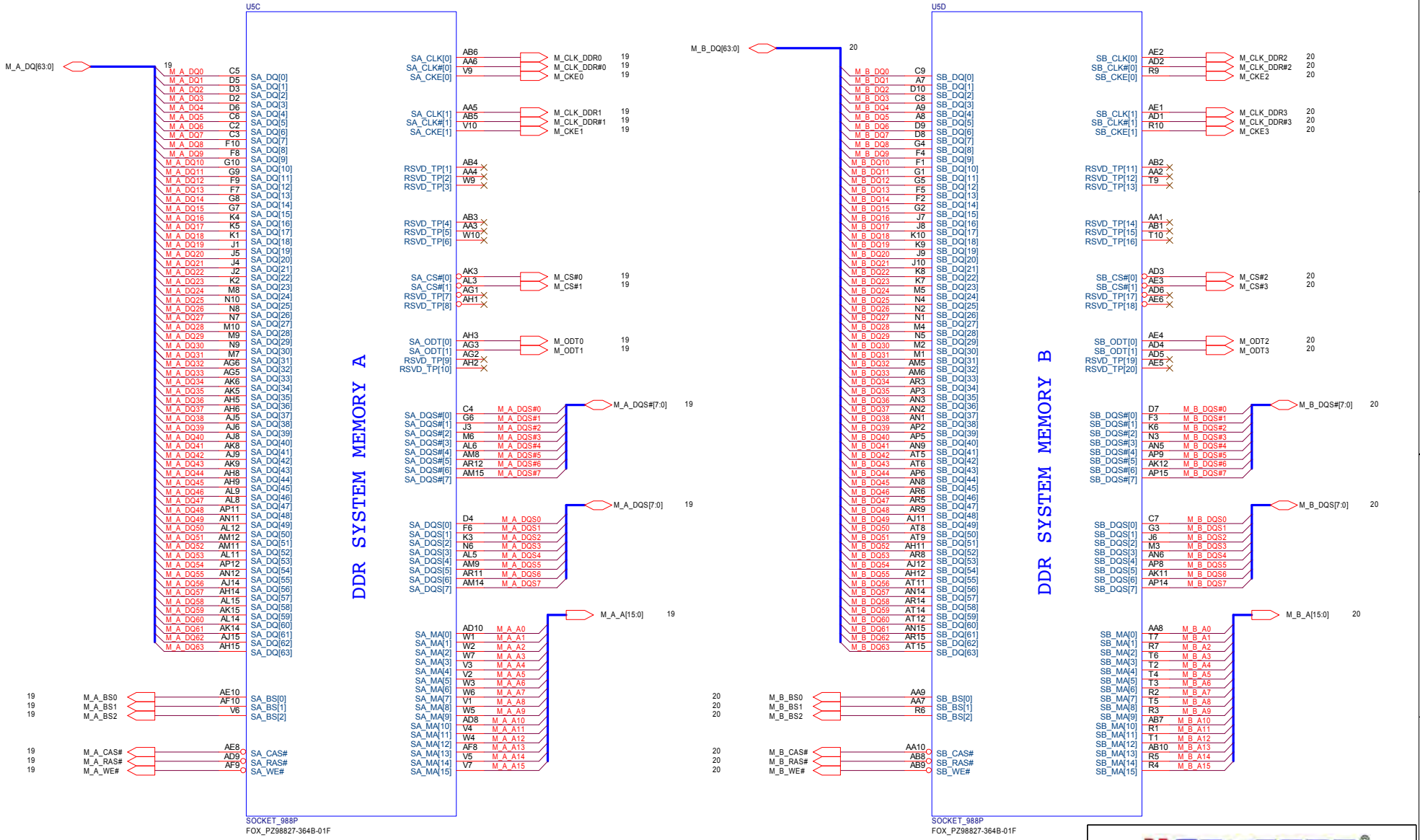

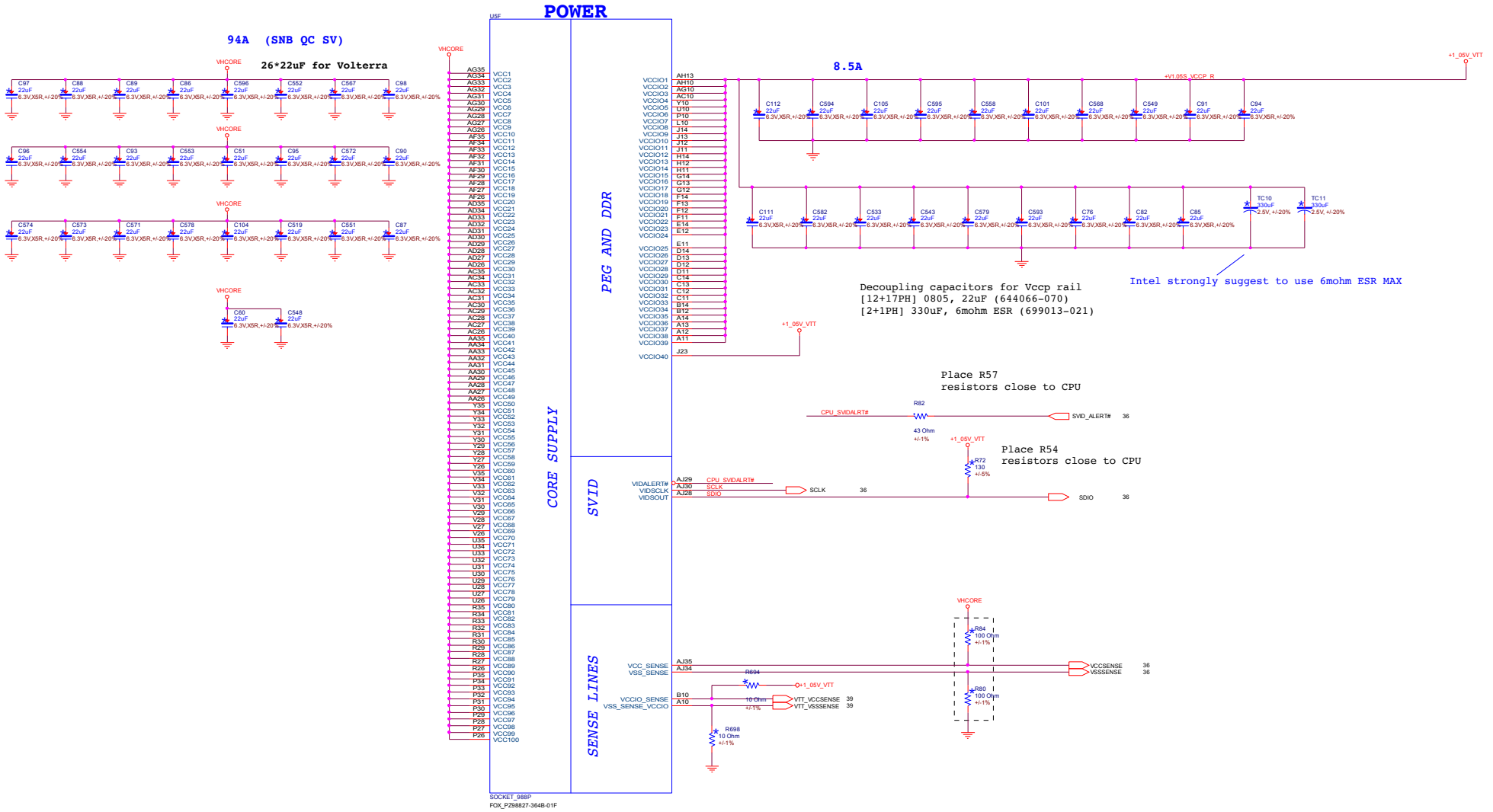

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Title: IVB (DDR3)

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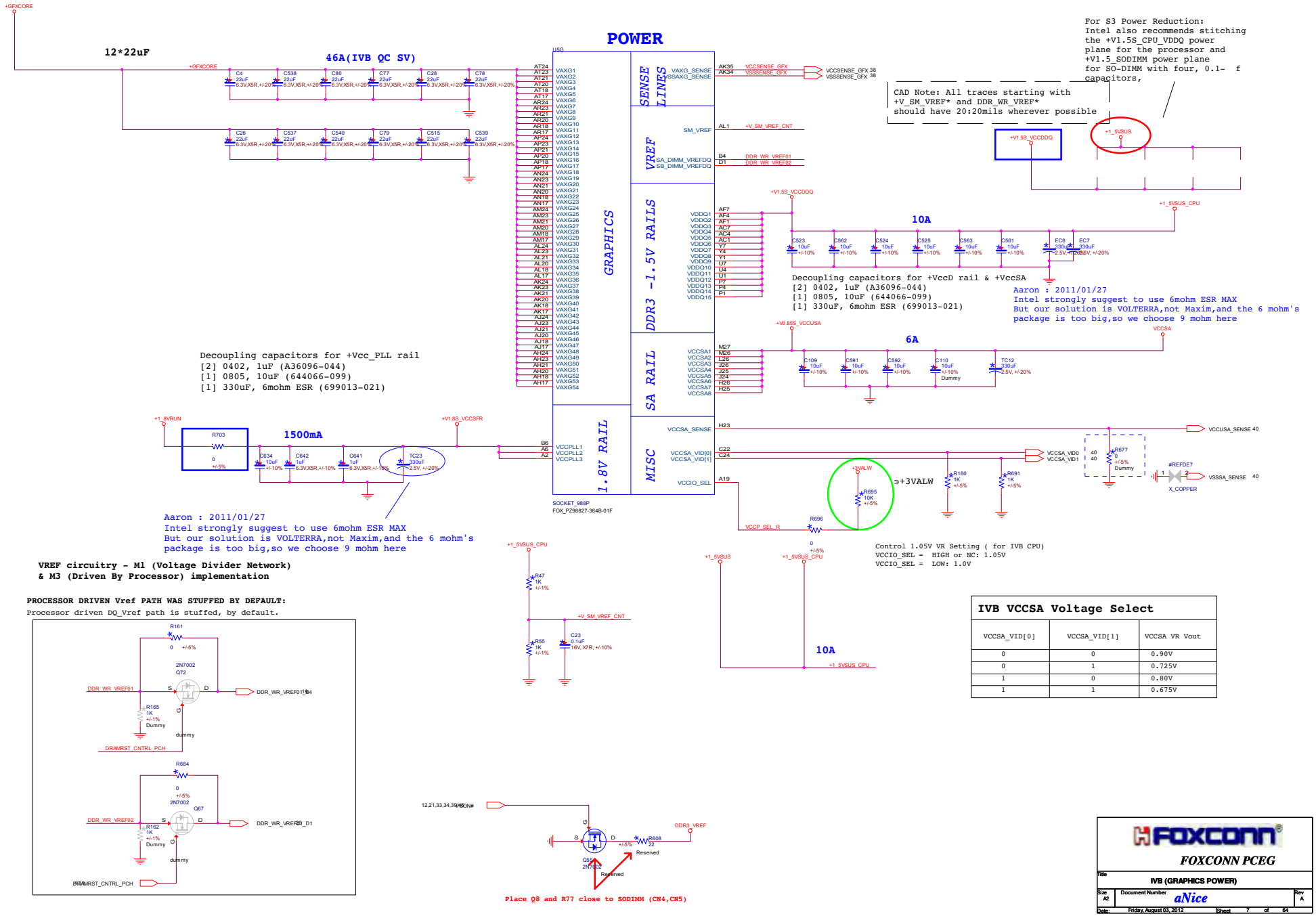
POWER



IVB VCCSA Voltage Select

VCCSA_VID[0]	VCCSA_VID[1]	VCCSA VR Vout
0	0	0.90V
0	1	0.725V
1	0	0.80V
1	1	0.675V

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Title: IVB (GRAPHICS POWER)

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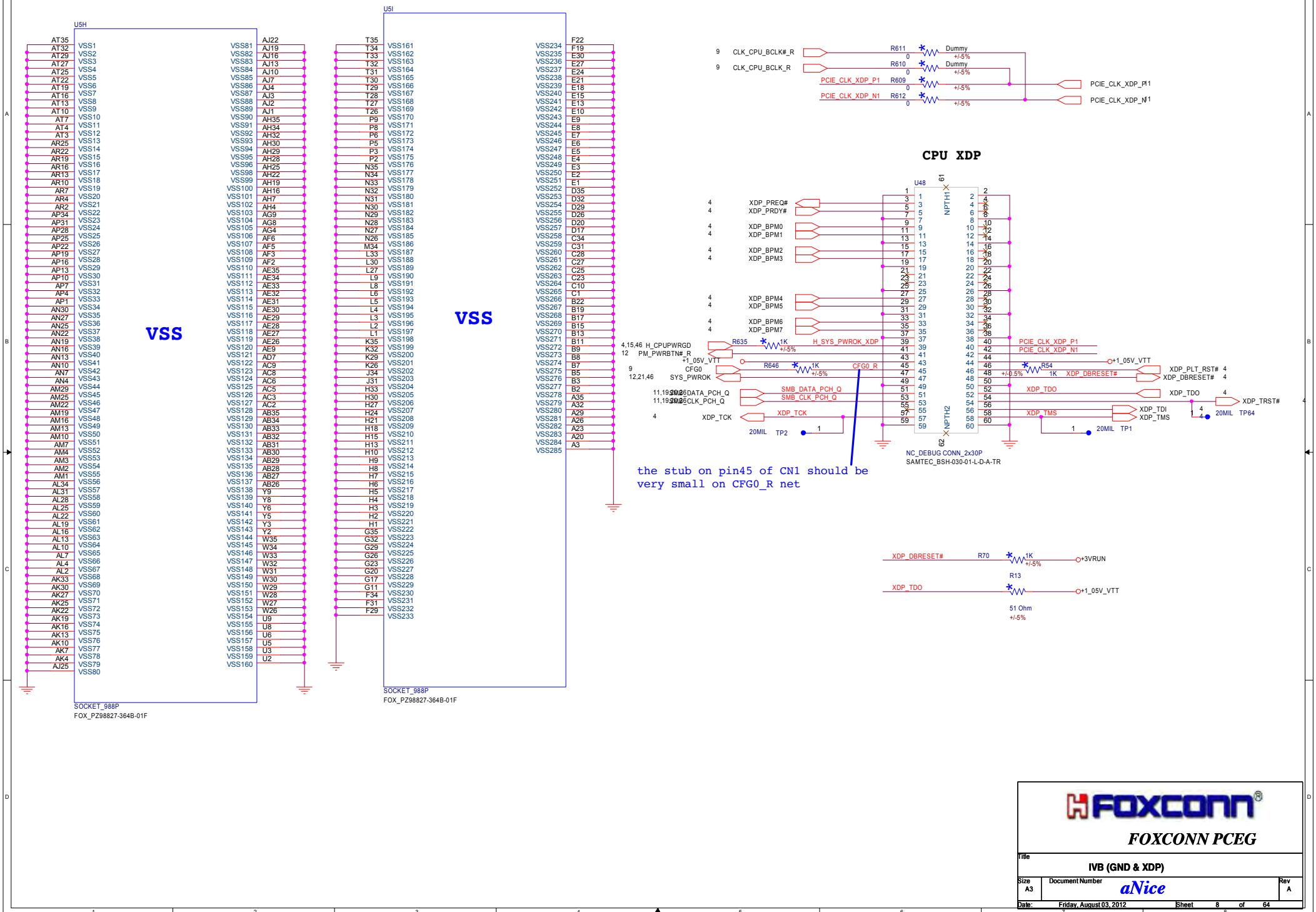
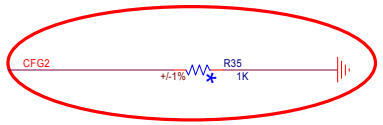


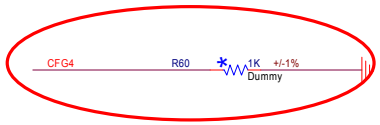
Note: <For PWR IFDIM 代刚>
TP代骾TP1007 TP1008≒疗
ぃ璶砆诀篤郎≅ . 砼 癸
紡琍differential紡, キ≪i紡,
ぃ i秈 耑跋.

PEG Lane reversal

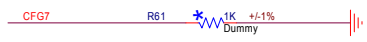


PEG static Lane Reversal - CFG2 is for 16X		
CFG2	0	LANE Reversed
	1	(Default)Normal Operation

ENABLE EDP

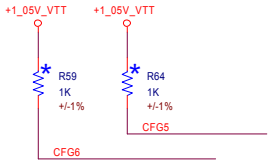


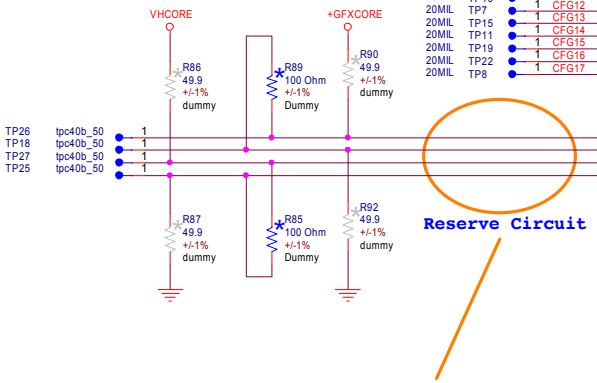
Display Port Presence Strap		
CFG4	0	Enabled eDP
	1	(Default)Disabled eDP

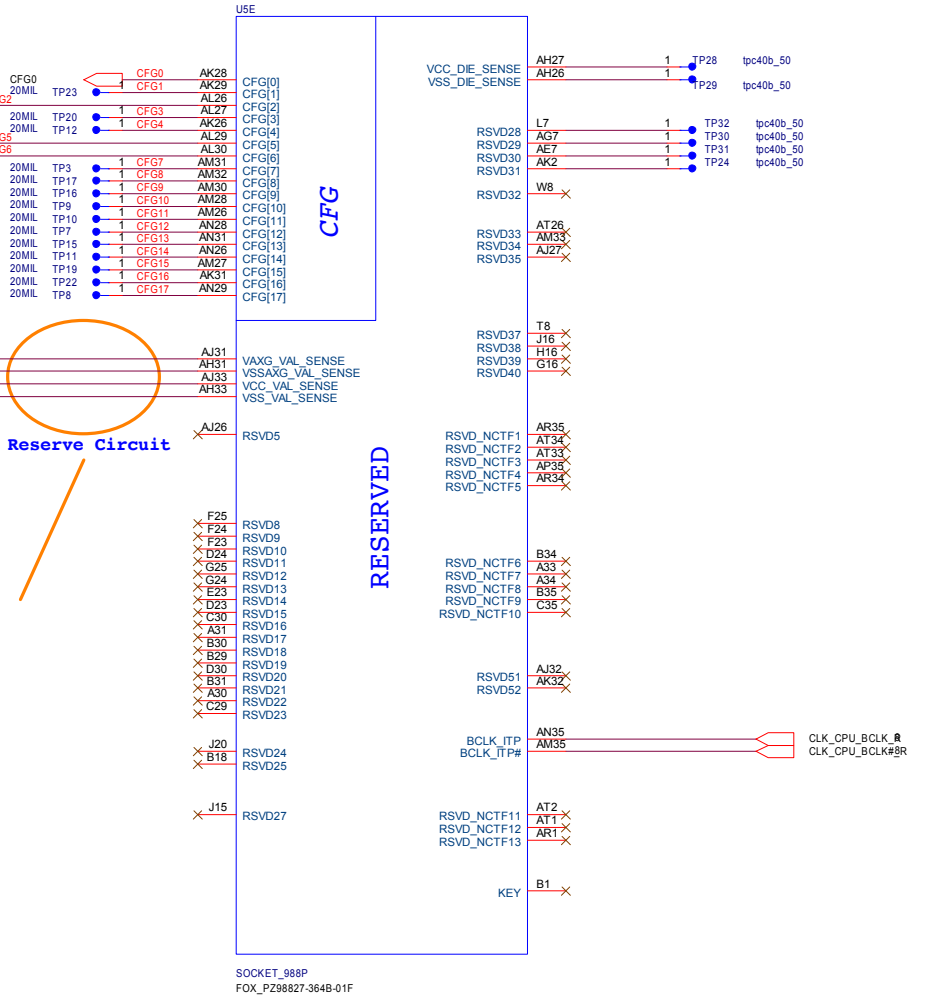


PEG DFER Training		
CFG7	0	PEG Wait for Bios for Training
	1	(DefaultPEG Train immediately following xxResetB Deassetion

PCIE Port Bifurcation Straps		
CFG[6:5]	11	(Default)16X
	10	X8 X8
	01	Reserved
	00	X8 X4 X4







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Title: IVB (RESERVED)

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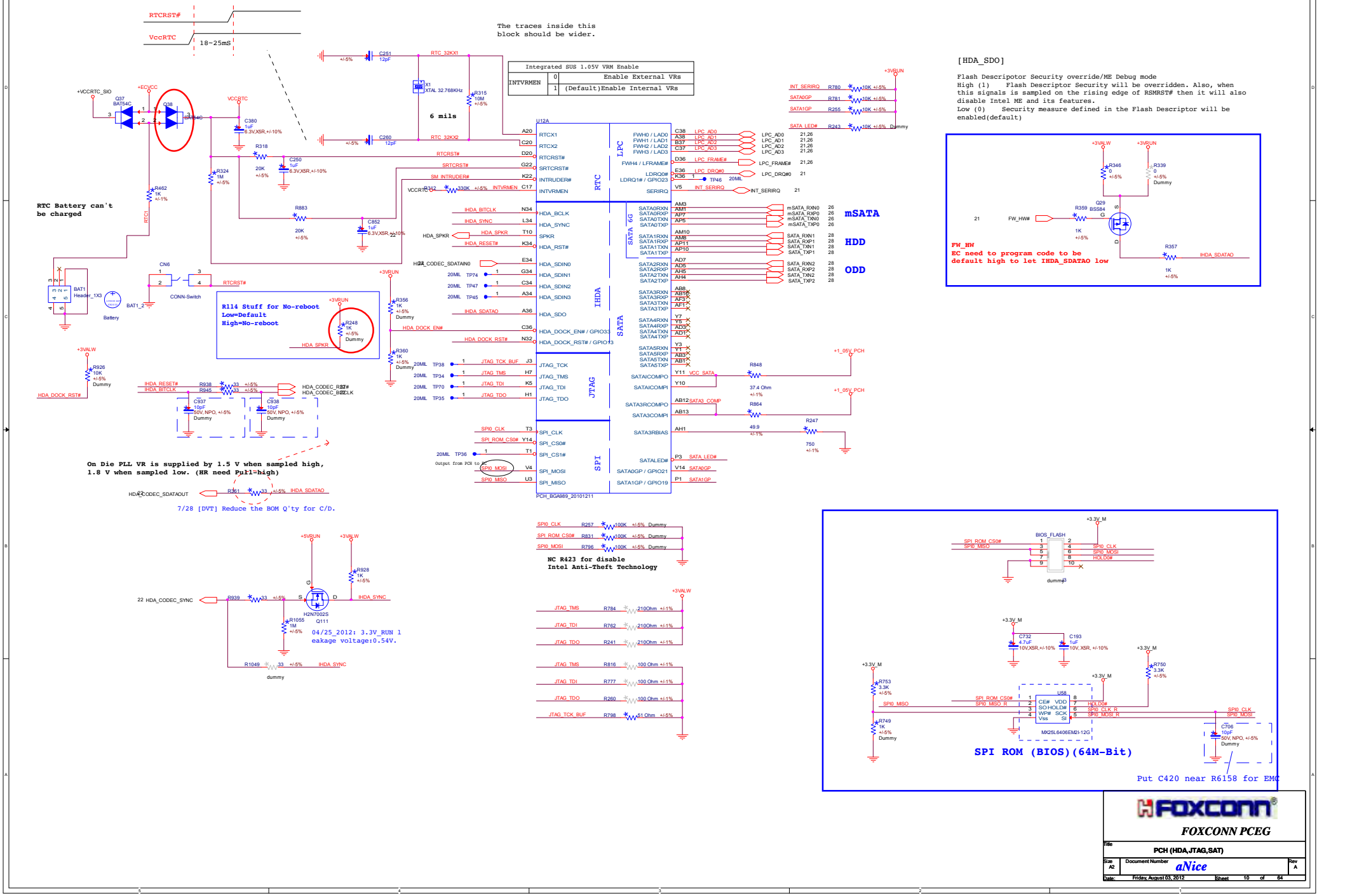
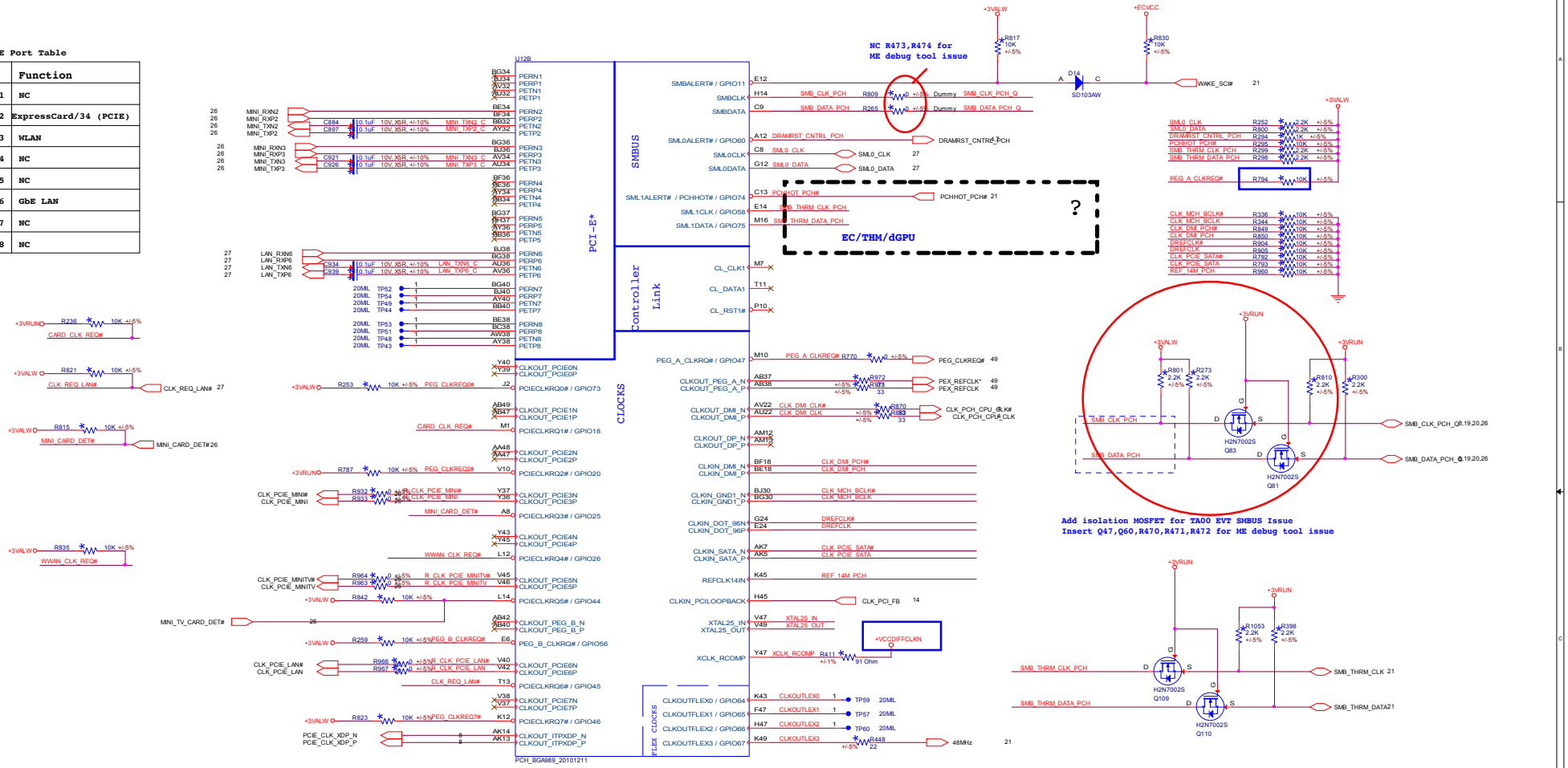


PCI-E Port Table

Port	Function
Port1	NC
Port2	ExpressCard/34 (PCIE)
Port3	WLAN
Port4	NC
Port5	NC
Port6	GbE LAN
Port7	NC
Port8	NC



CPET HW track P.28
GPIO[65,67] can set as Clock output
1.14.318 MHZ
2.27 MHZ (SSC/No SSC)
3.48 MHZ
4.24 MHZ
5.Not set as 33MHZ

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Title: PCH (PCI-E,SMBUS,CLK)

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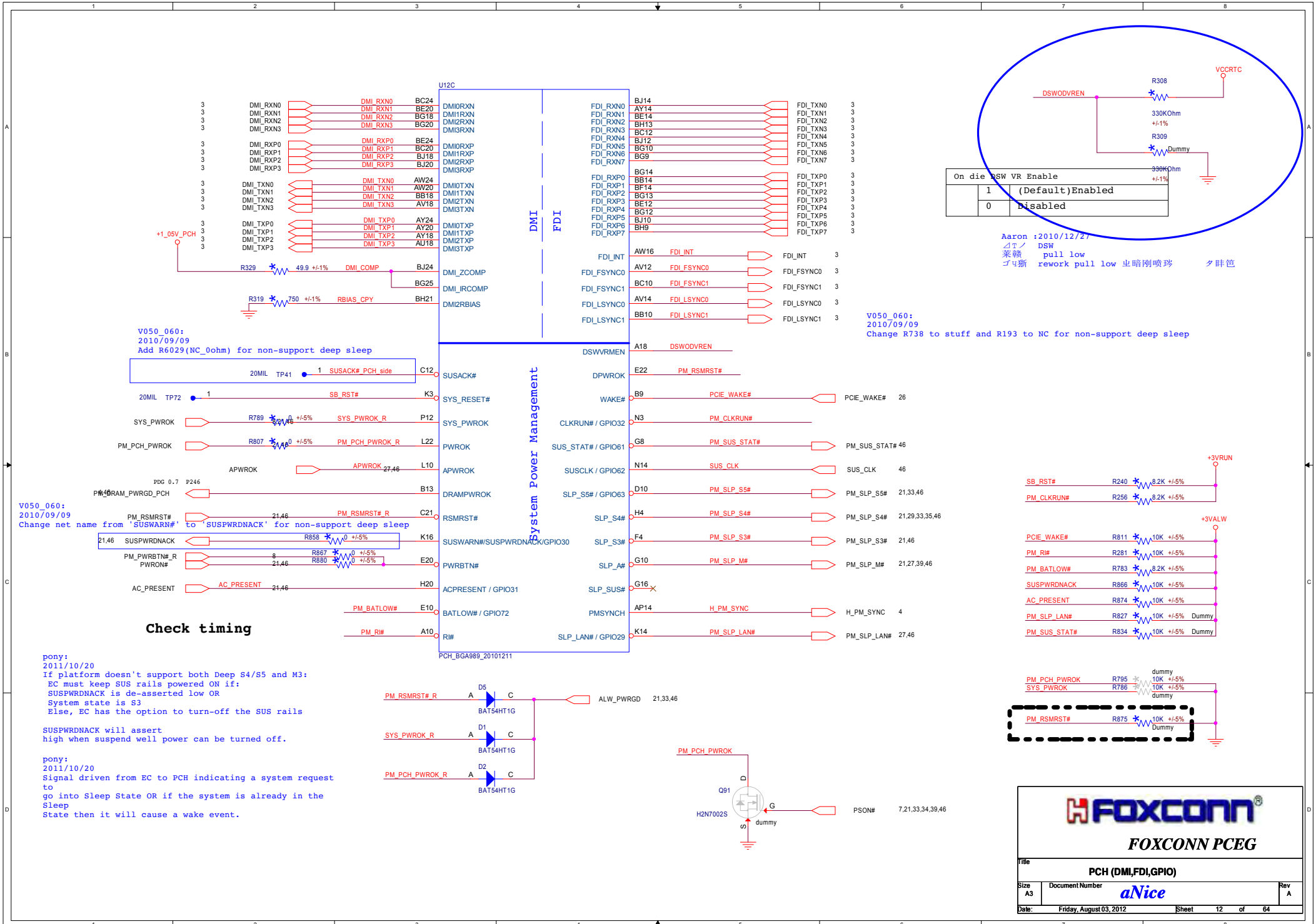

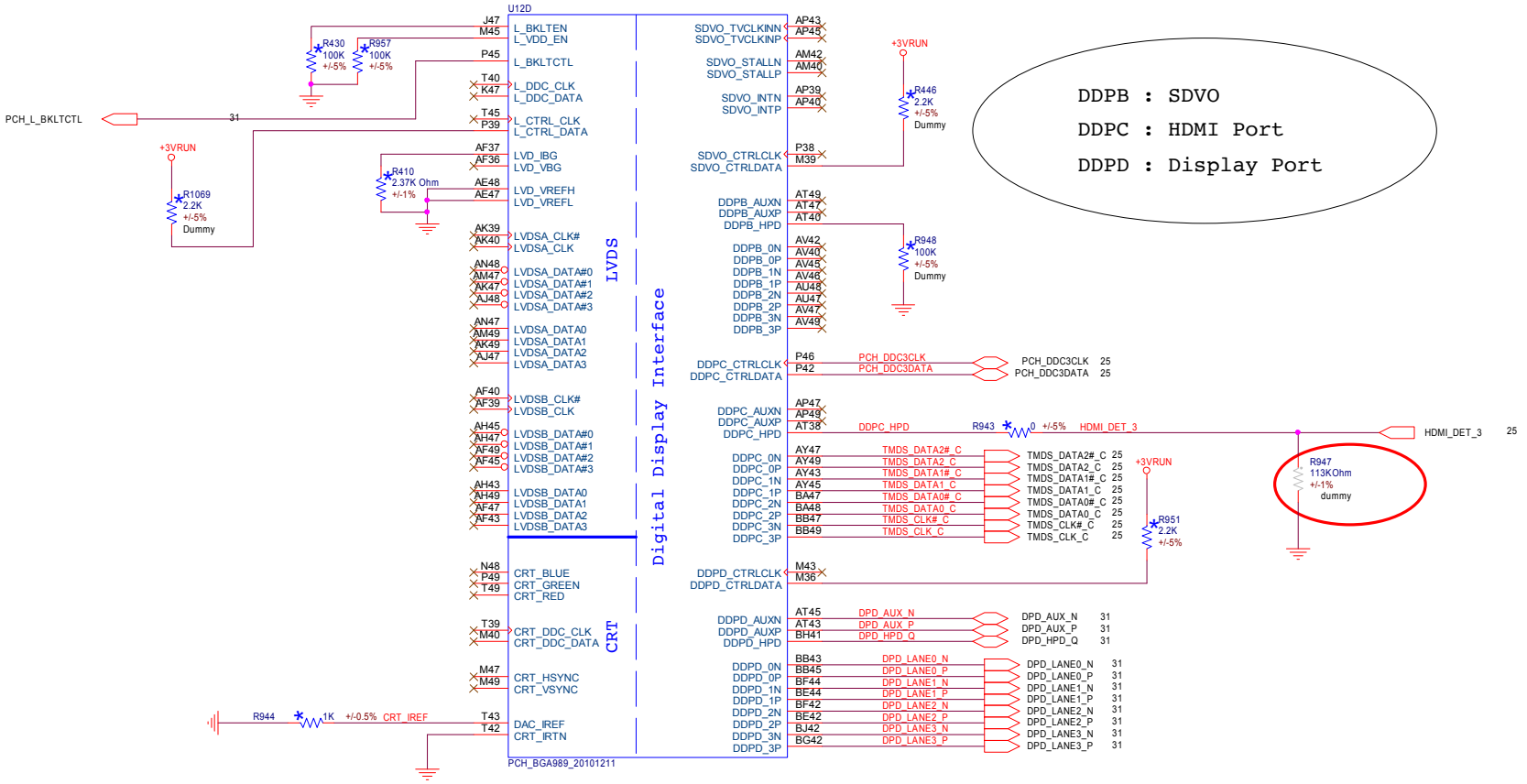

FOXCONN PCEG

Title: PCH (LVDS,DDI)			
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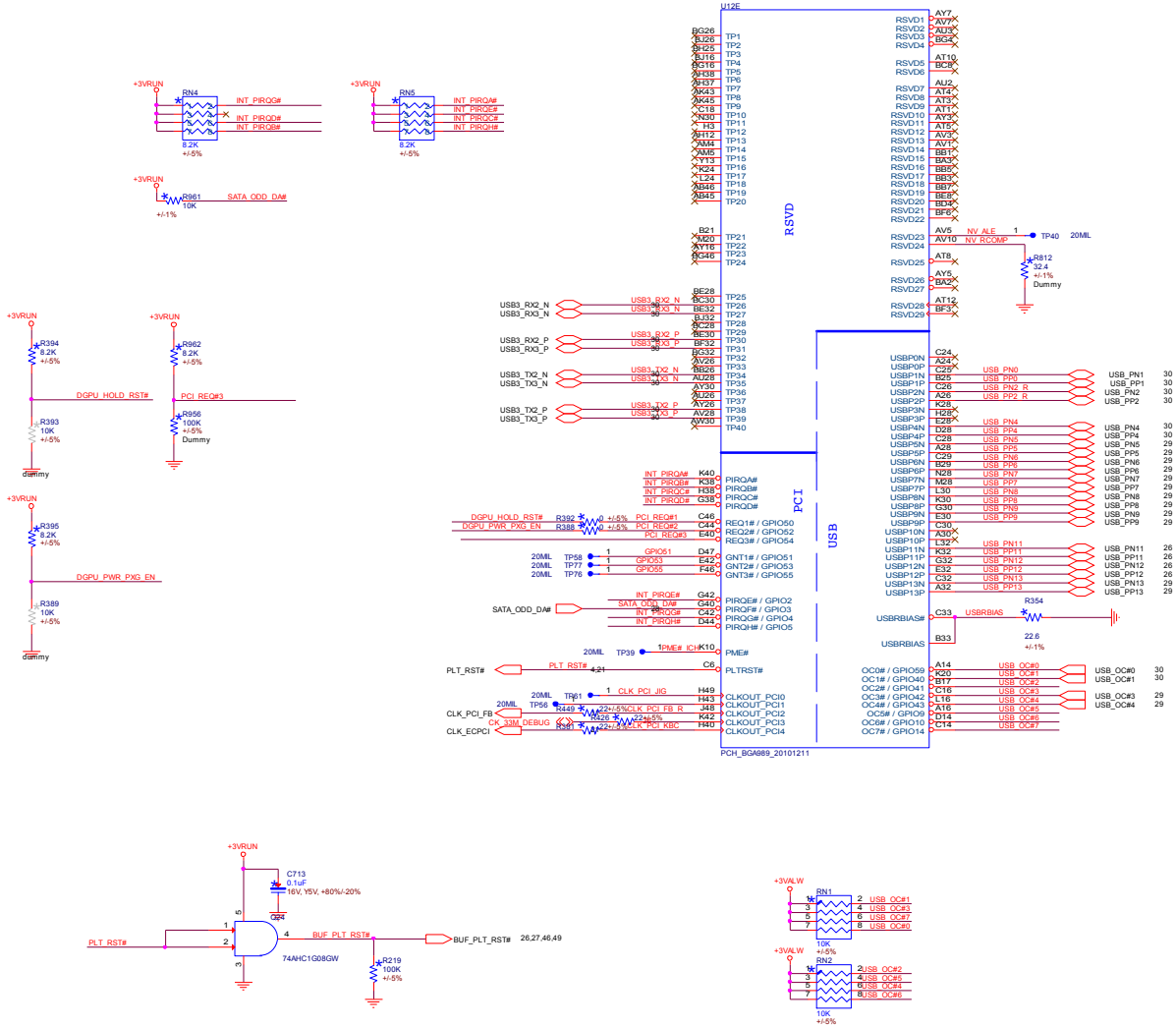
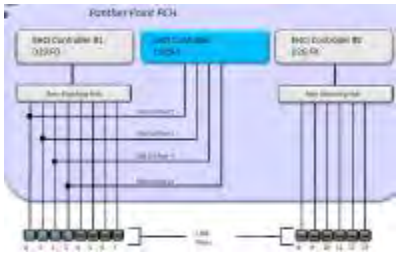


RC receiver
Touch panel NFC
KB/MS receiver

USB PORT	Function
PORT-0	External Port-0 (USB 3.0)
PORT-1	Card Reader
PORT-2	External Port-2 (USB 3.0)
PORT-3	
PORT-4	
PORT-5	USB Hub (USB 2.0)
PORT-6	DB Port-0 (USB 2.0)
PORT-7	DB Port-0 (USB 2.0)
PORT-8	MB Port-0 (USB 2.0)
PORT-9	MB Port-0 (USB 2.0) / debug port
PORT-10	
PORT-11	mini_PCIE-2 (WLAN+BT)
PORT-12	mini_PCIE-3 (TV)
PORT-13	Camera + MIC

USB 3.0/2.0 Port Pairing

USB 3.0 PORT	USB 2.0 PORT
PORT-1	PORT-0
PORT-2	PORT-1
PORT-3	PORT-2
PORT-4	PORT-3



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Title: PCH (PCI,USB,NVRAM)

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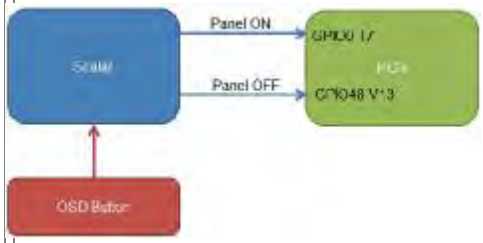

GPIO 22 不pull-high
BIOS recovery
1.disable
0.enable

Follow CRB

For Intel PDG 0.9

PLL ON DIE VR ENABLE		
GP28	0	disable
	1	Enable(Default)

DMI & FDI Termination Voltage		
NV_CLE	0	Set to Vss when LOW (IVB,GNDed on package)
	1	Set to Vcc when HIGH(SNB,default)

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Title: PCH (GPIO,VSS_NCTF,RSVD)

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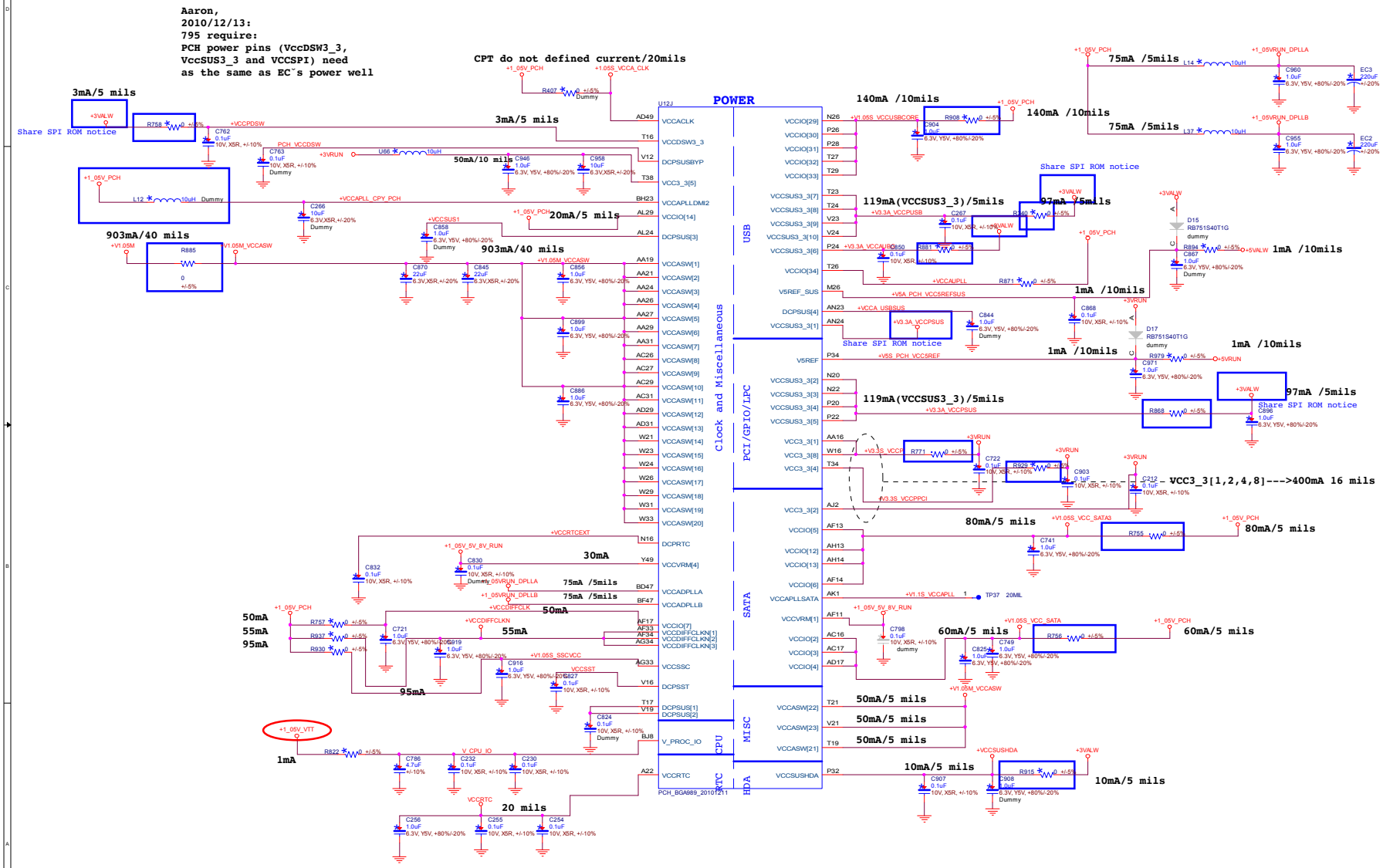

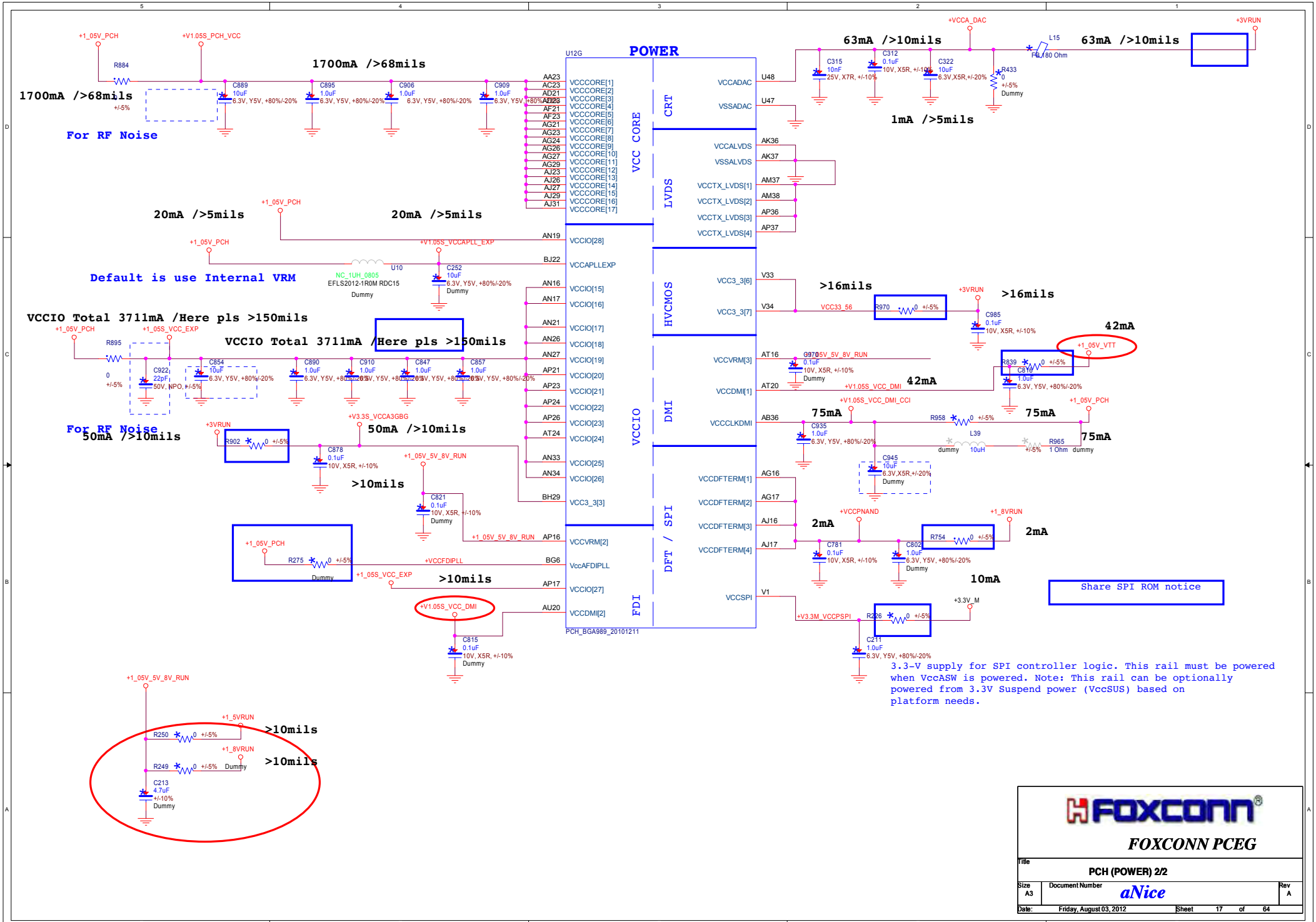

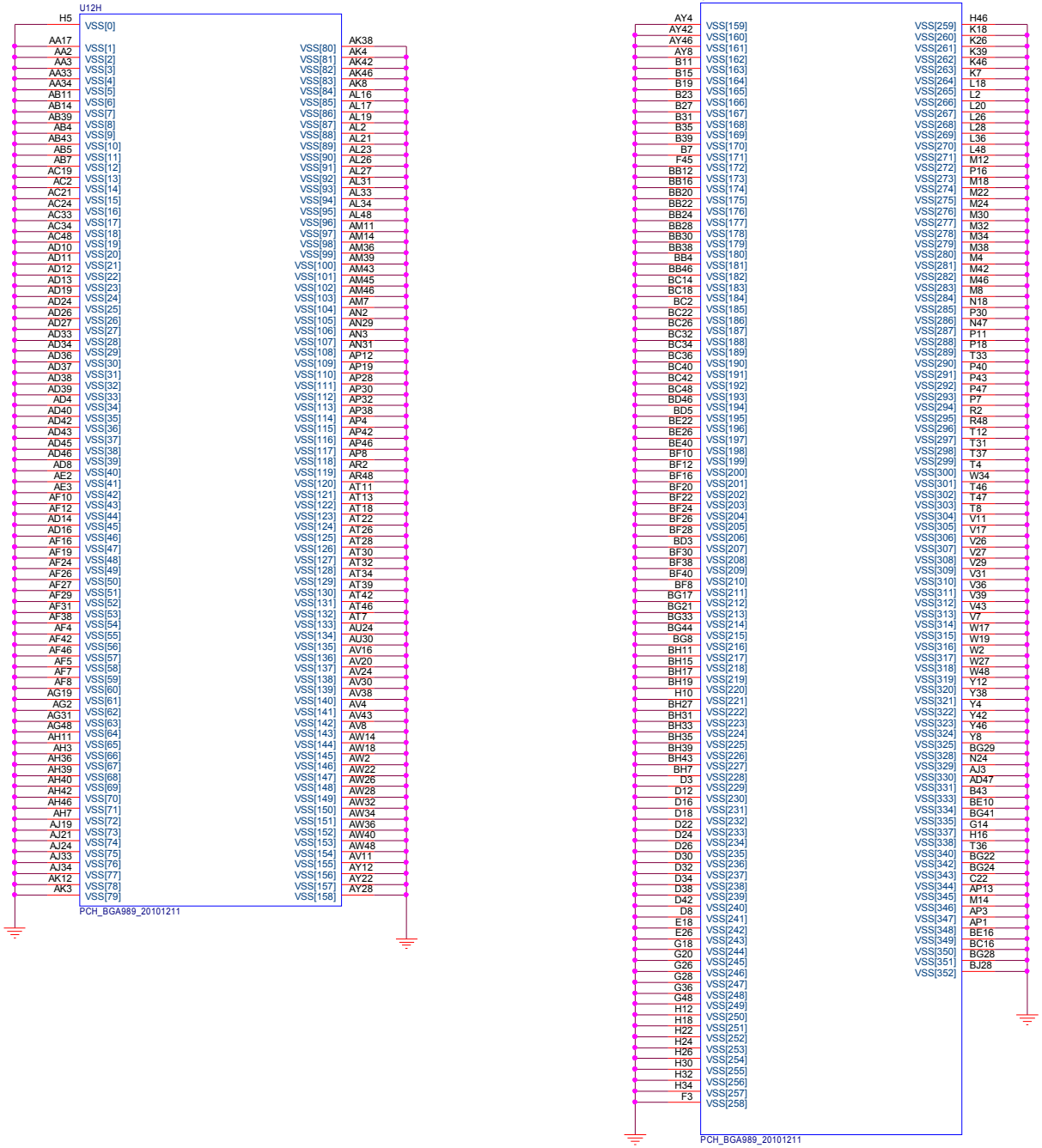

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Title: PCH (VSS)

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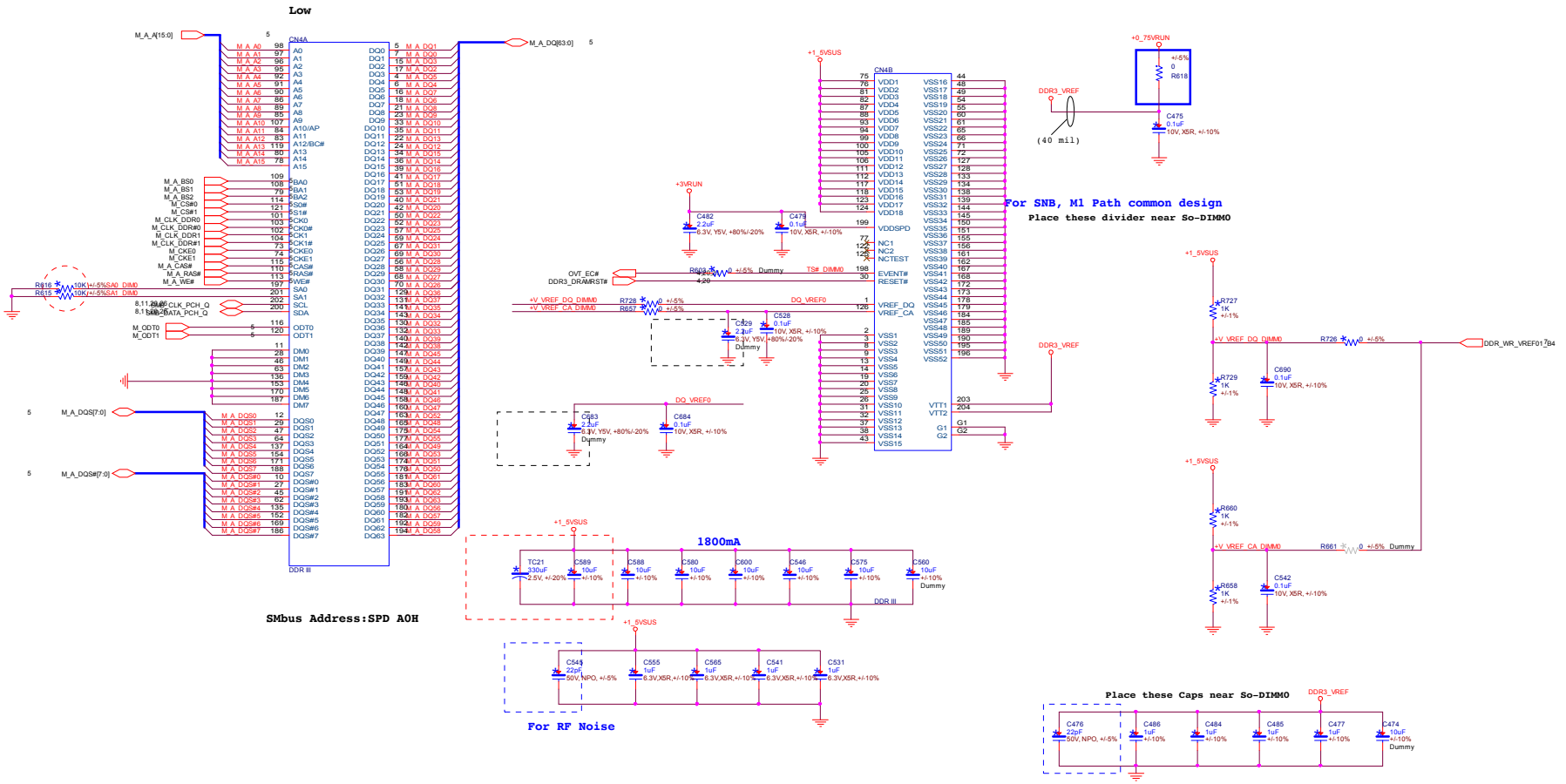

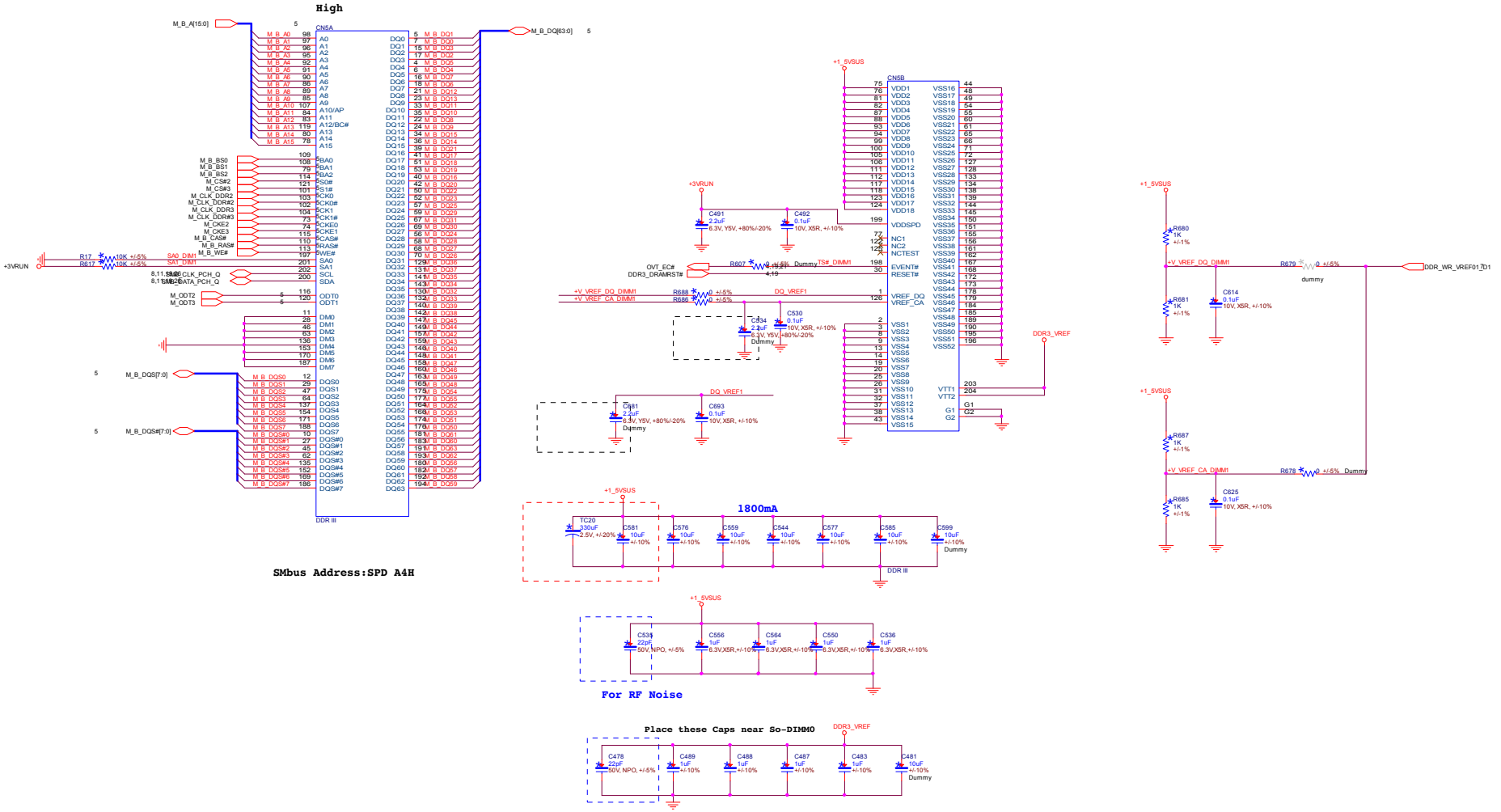

IT8731 Power On Strapping Options

Symbol		value	Description
JP6	AMD SVID_EN	1	Disabled SVID Output pin
Pin 29		0	Enable SVD(Pin3)/SVC(Pin31) output pins
JP4	K8PWR_EN	1	K8 power sequence function is disabled
Pin 126		0	K8 power sequence function is enabled
JP3	FAN_CTL_SEL	1	The default value of EC Index 15h/16h/17h is 80h
Pin 124		0	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)

Voltage Monitor

```
If without use these pins, Please pull-up to 3.3V.
Don't let it floating
1.Pin 19:ATXPG
2.Pin 71:SUS8#
3.Pin 77:SUSC#
4.Power On Strapping Options pin
```

LPC Pull-ups

Note:
Most pull-ups are provided on system main-board.

Thermal Controller

Thermal Resistor Mode

For Intel 4 PIN FAN
Don't remove R102 100 ohm.

Layout Note: D8 must near Fan Connector J5.

SPI Interface

1. layout trace is as far as possible short
2. Pull-up resistor 1Kohm near SPI Flash

LPC I/F

To Intel PCH SMBus

PCH side have pull high to +3VALW

Note:
*Place C7, C8 close to IT8731

Note:
*Place C10,C11 close to IT8731
*Recommended net "3.3VSB" minimum trace width 12mils.

Tantalum cap.
(Spare for battery installation glitch)
Layout Note:
*Recommended net "VBAT" minimum trace width 12mils.
*Isolated the VBAT pin-69 & ICH's VCCRTC pin
*Suggest not clear SIO's VBAT

APC POWER BUTTOM

To ATX power connector pin14 PSON#

SMBUS1 for EC debug

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Title: EC+SPI ROM 1/2

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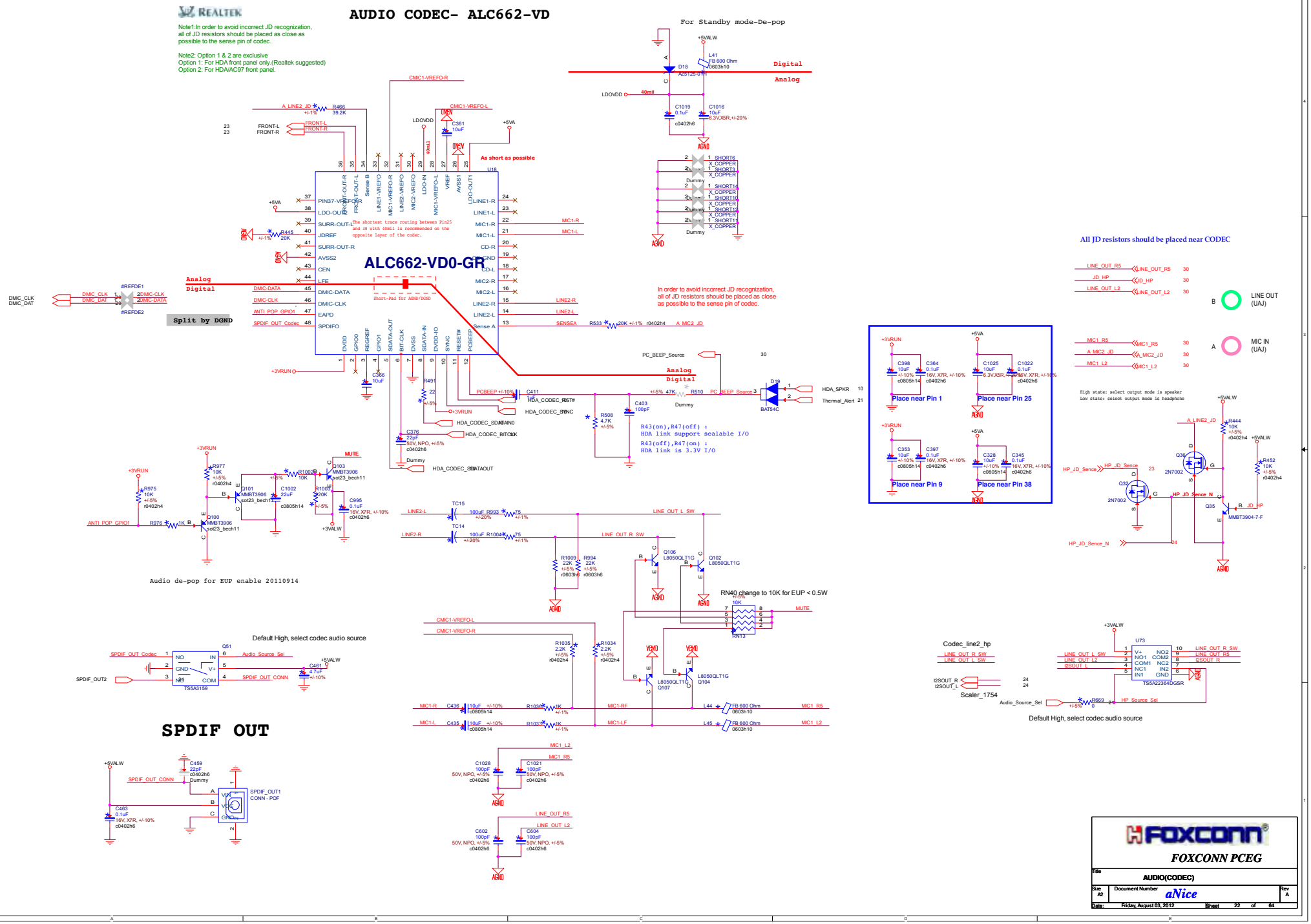
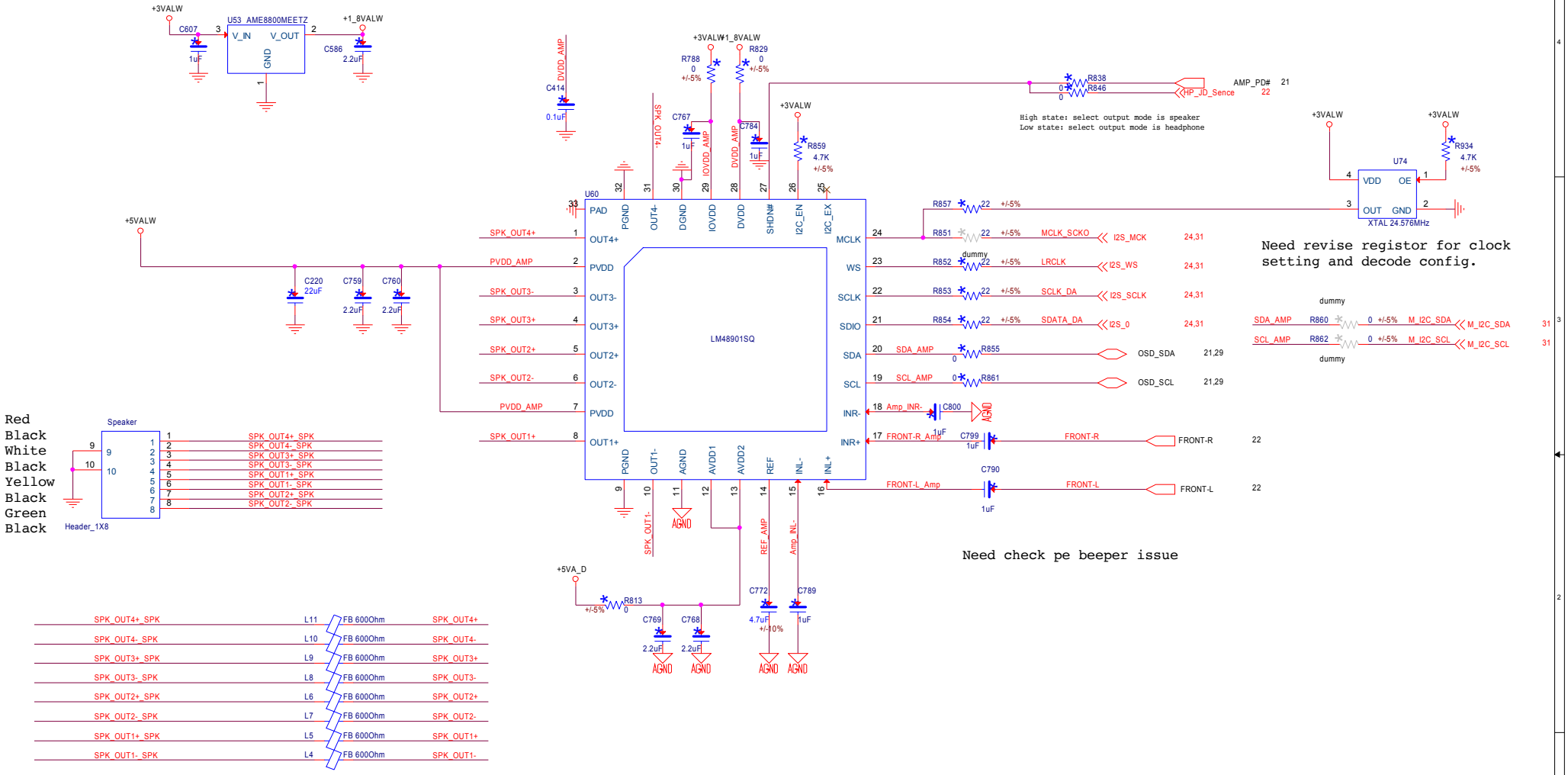
AUDIO CODEC- ALC662-VD





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Title	Audio Speaker(6W)	
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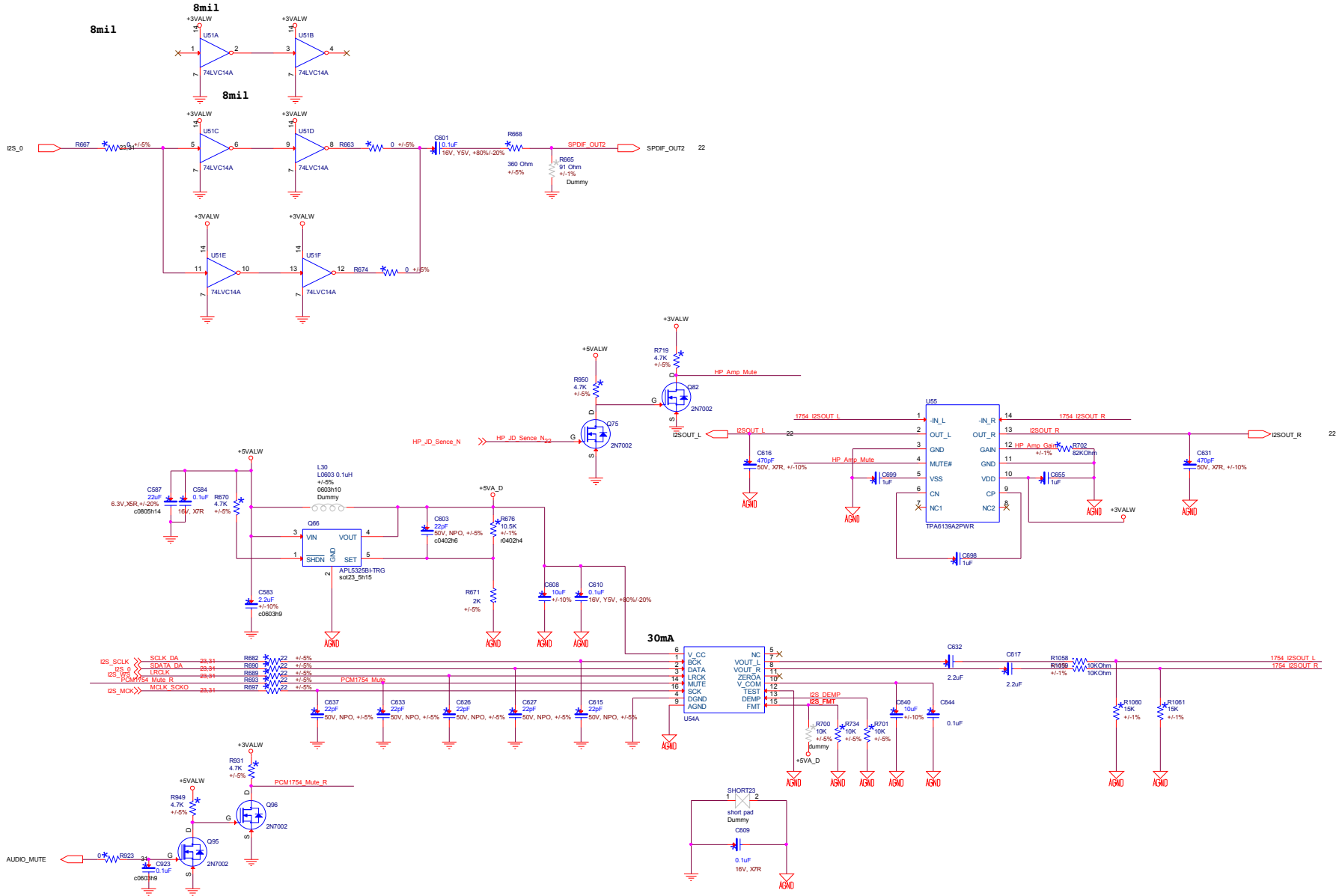
SPDIF INPUT



FOXCONN PCEG

Title	FAN & Debug Port	
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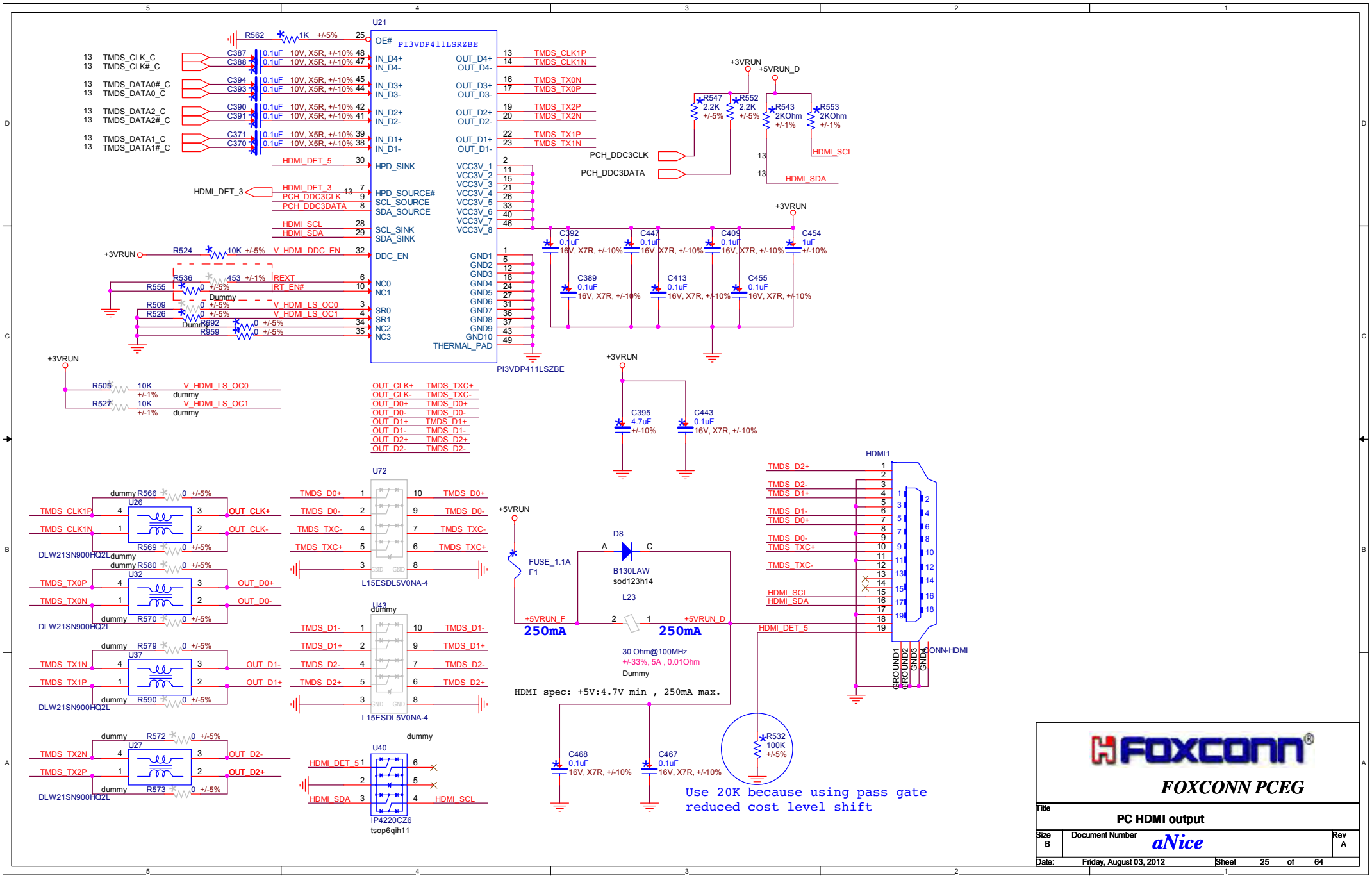

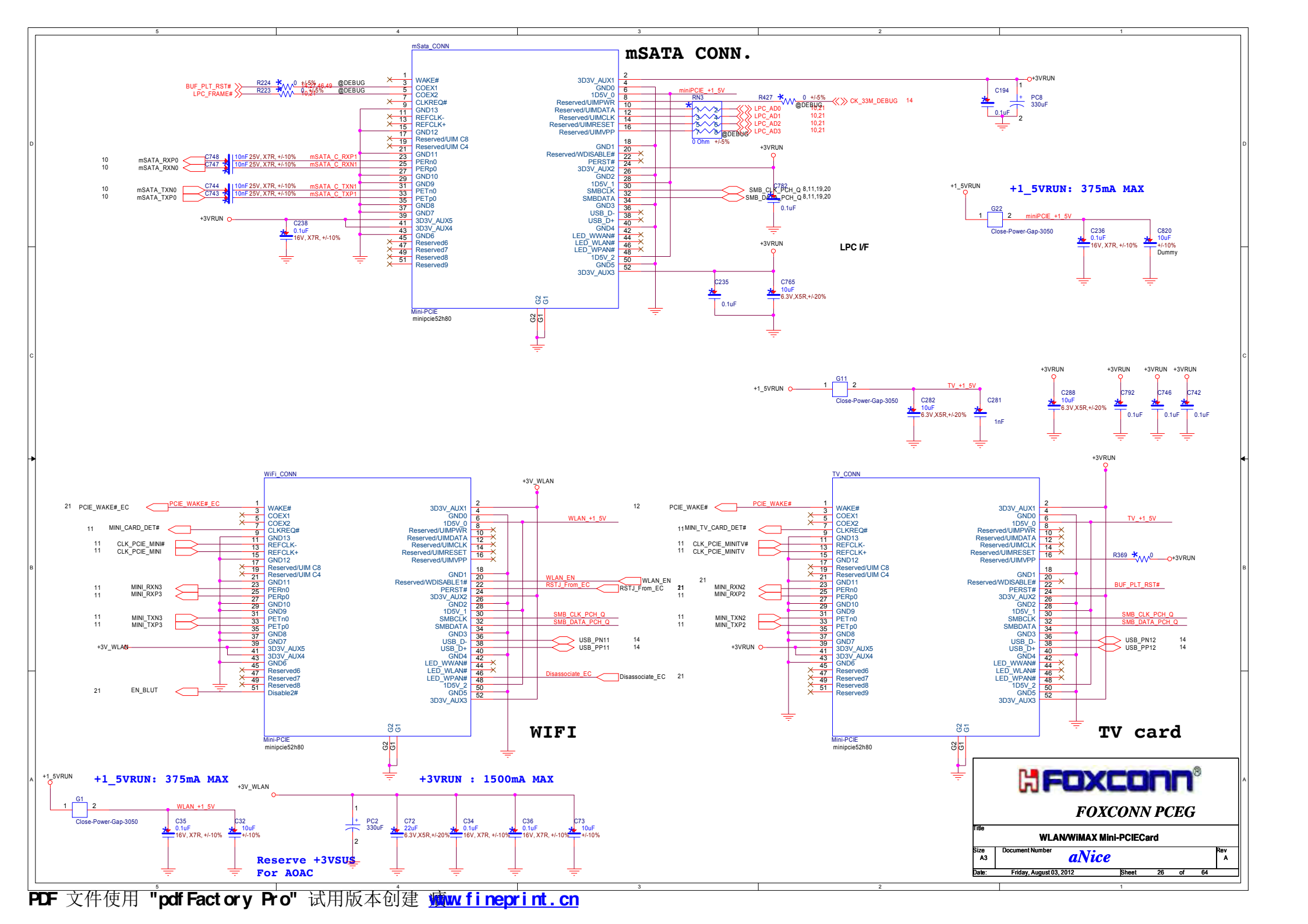

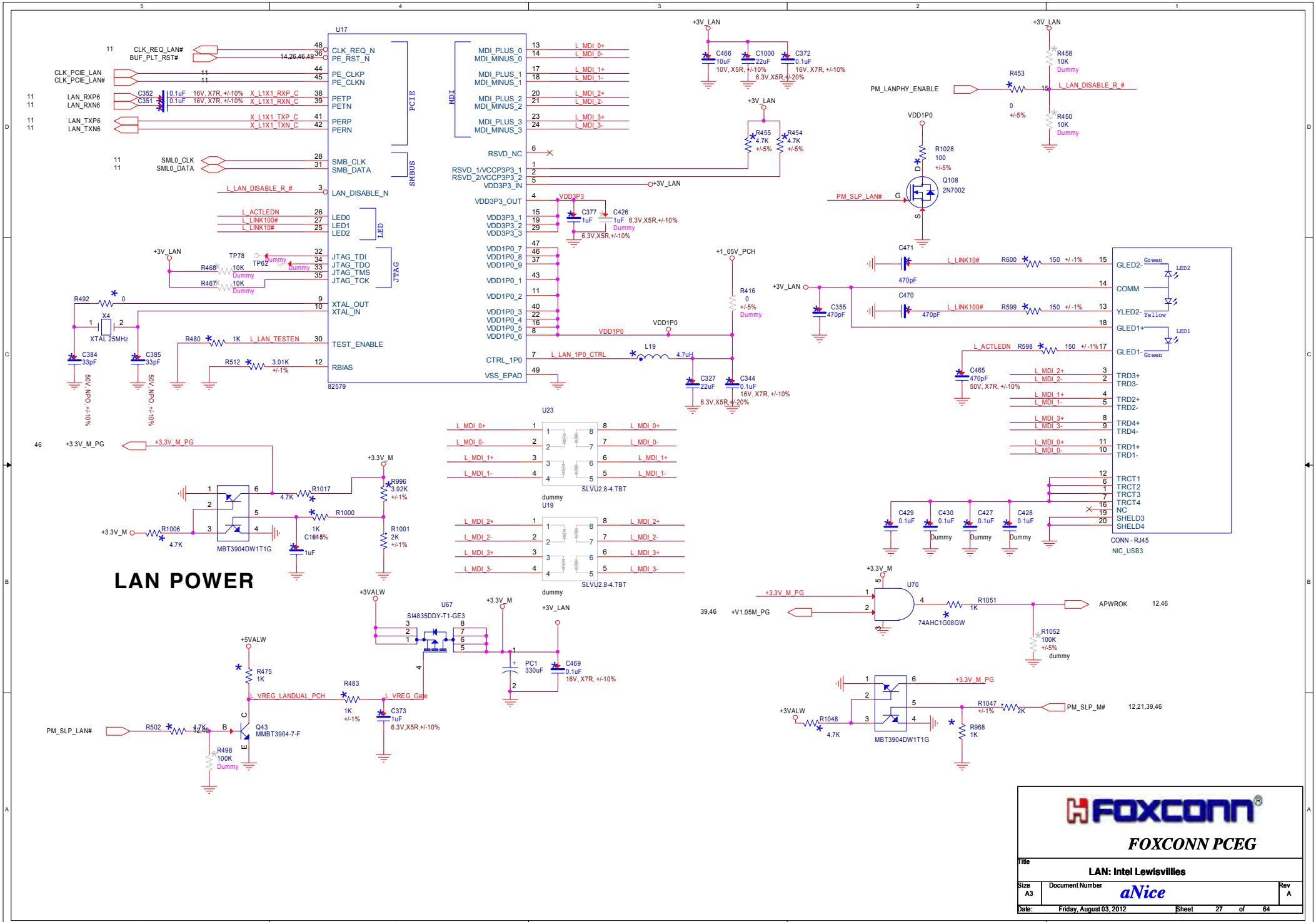

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Title	LAN: Intel Lewisvillies	
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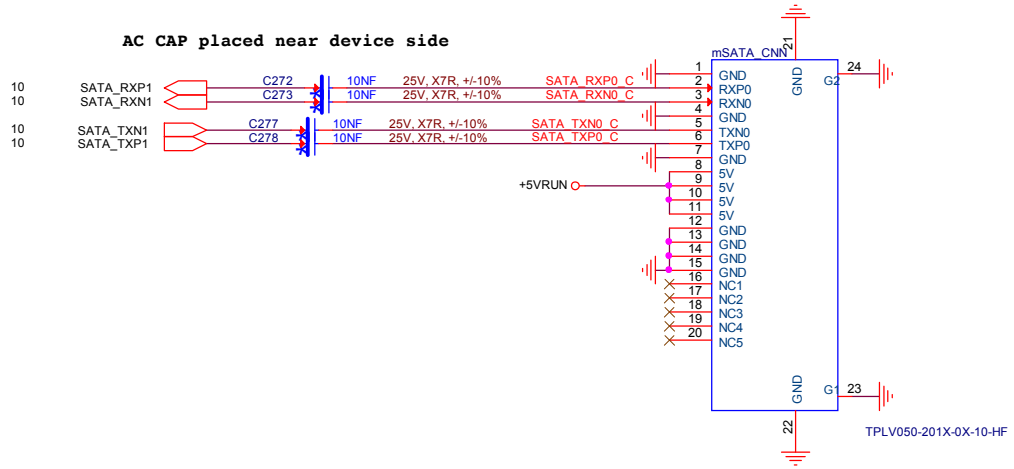
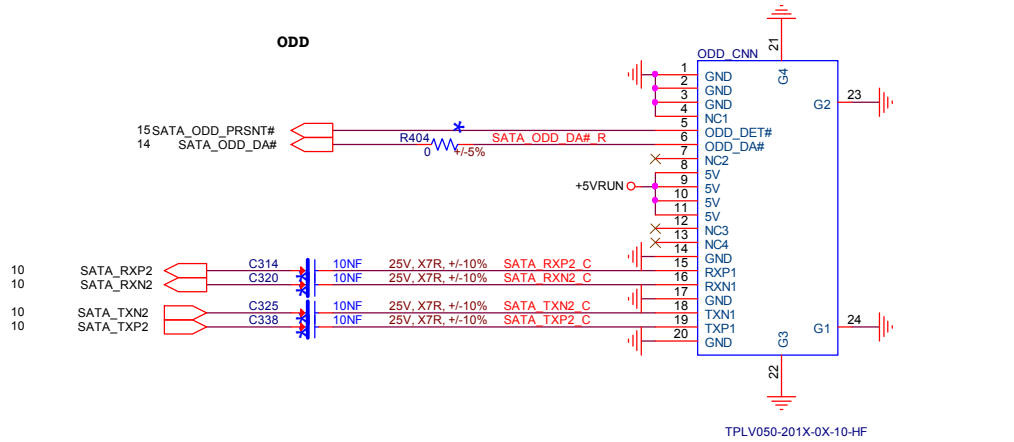
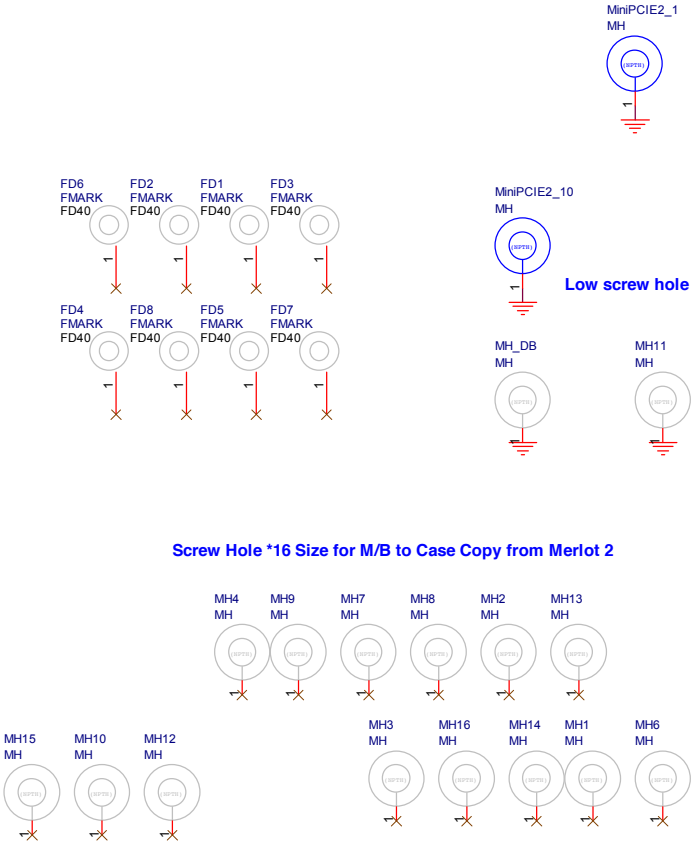
SATA HDD

AC CAP placed near device side



ODD





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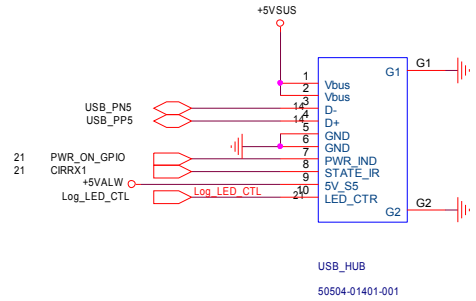
Title: SATA HDD/ODD		
Size: B	Document Number: aNice	Rev: A
Date: Friday, August 03, 2012	Sheet 28 of 64	



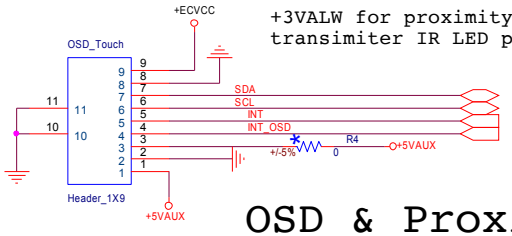
Touch panel

RC receiver

KB/MS receiver

NFC

PWR_IND indicates the power state from EC. It is used for RF module to decide the key code pass thru USB or STATE_IR. Detail definition will be defined by Suyi and ITE EC team.

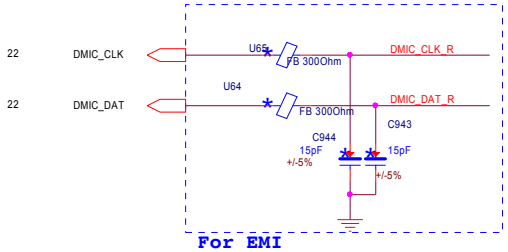


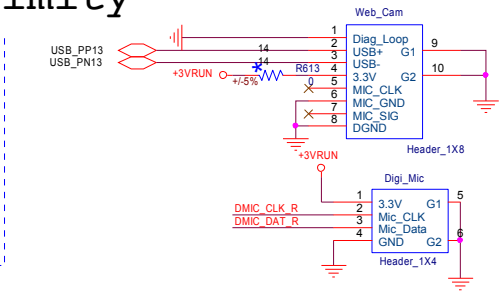
+3VALW for proximity transimiter IR LED power

+EVCC for proximity IC and OSD touch IC power

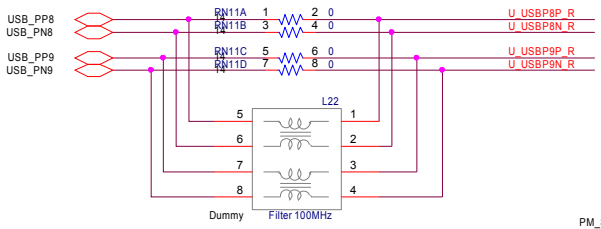
+5VAUX for OSD touch LED power.

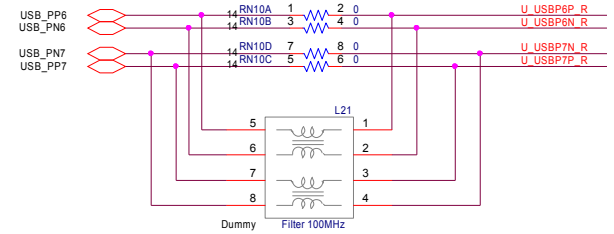
OSD & Proximity

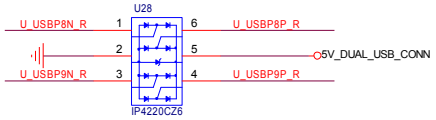


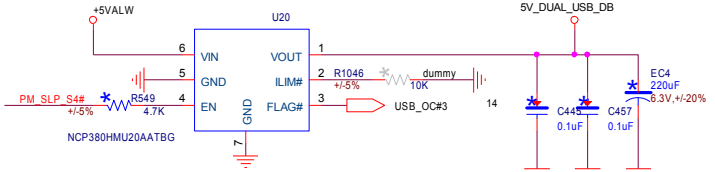


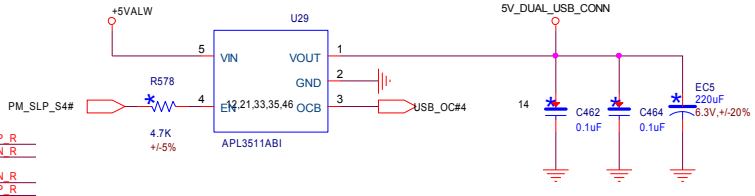
Web cam & Digital MIC

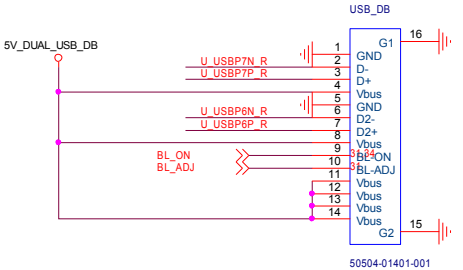


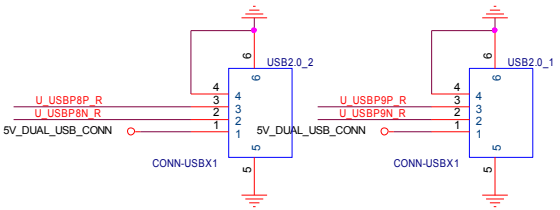












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Title: H/W Thermal Protect		
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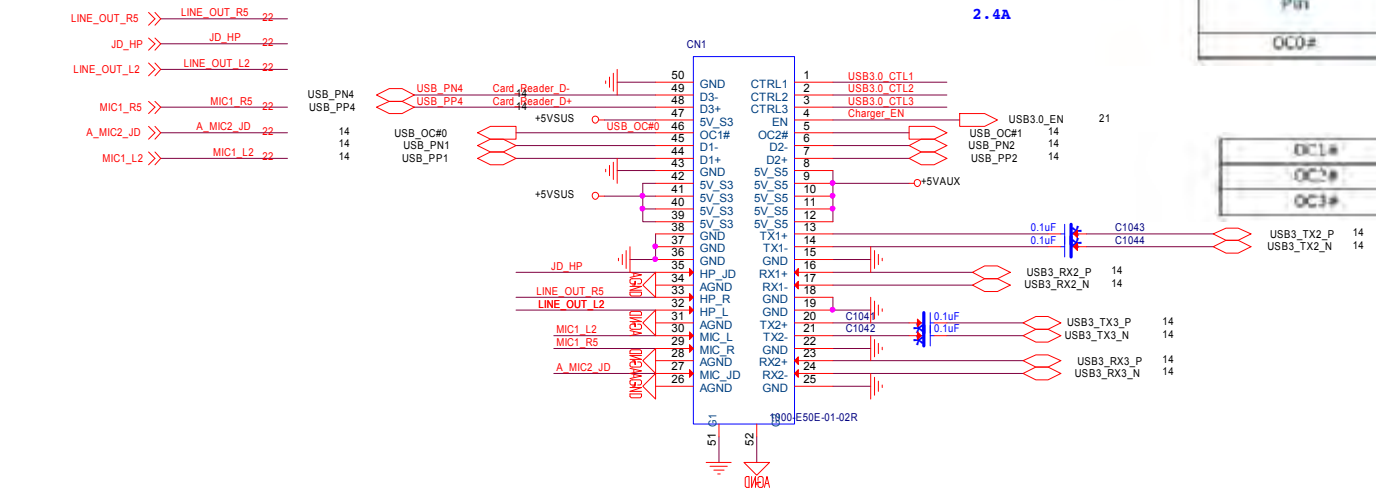


2.4A

Table 3-122.USB 2.0 Overcurrent Pin Default Usage

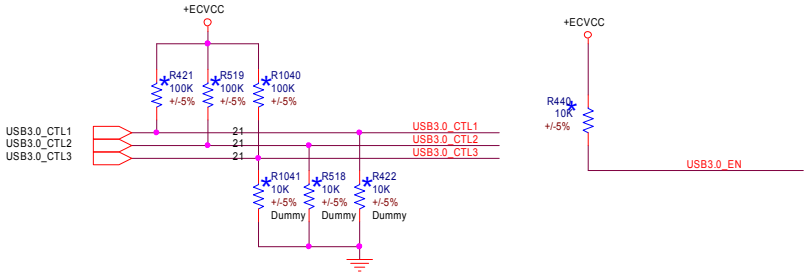
Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 9, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

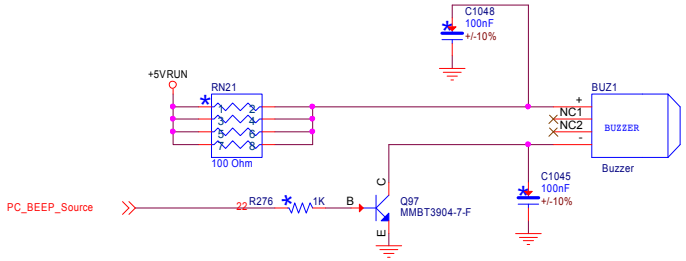
USB 2.0 Port 0&2 protect

USB 3.0 Port 1&3 protect

USB 3.0/2.0 Port Pairing

USB 3.0 PORT	USB 2.0 PORT
PORT-1	PORT-0
PORT-2	PORT-1
PORT-3	PORT-2
PORT-4	PORT-3





For charging USB devices at S0/S3/S4/S5
(Charger current = min 1.5A)

CTL1	CTL2	CTL3	MODE
0	0	0	OUT discharge, power switch OFF.
0	X	1	Dedicated charging port, auto-detect.
X	1	0	Standard downstream port, USB 2.0 Mode.
1	0	0	Dedicated charging port, BC1.2(draft) only.
1	0	1	Dedicated charging port, Divider Mode only.
1	1	1	Charging downstream port, BC1.2(draft).

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FOXCONN PCEG

Title: USB2.0_3.0 x 2

Size: A3 | Document Number: aNice | Rev: A

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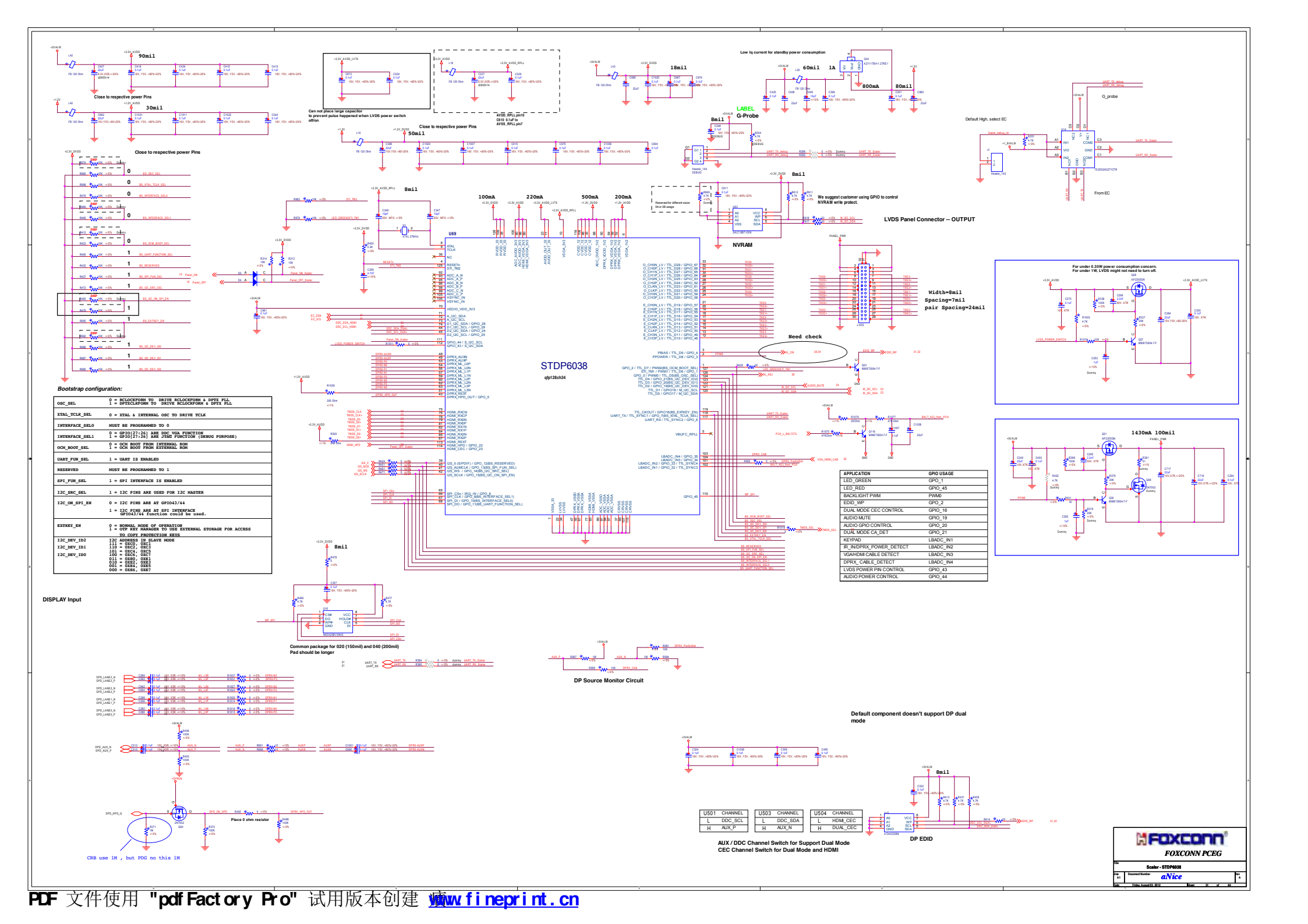
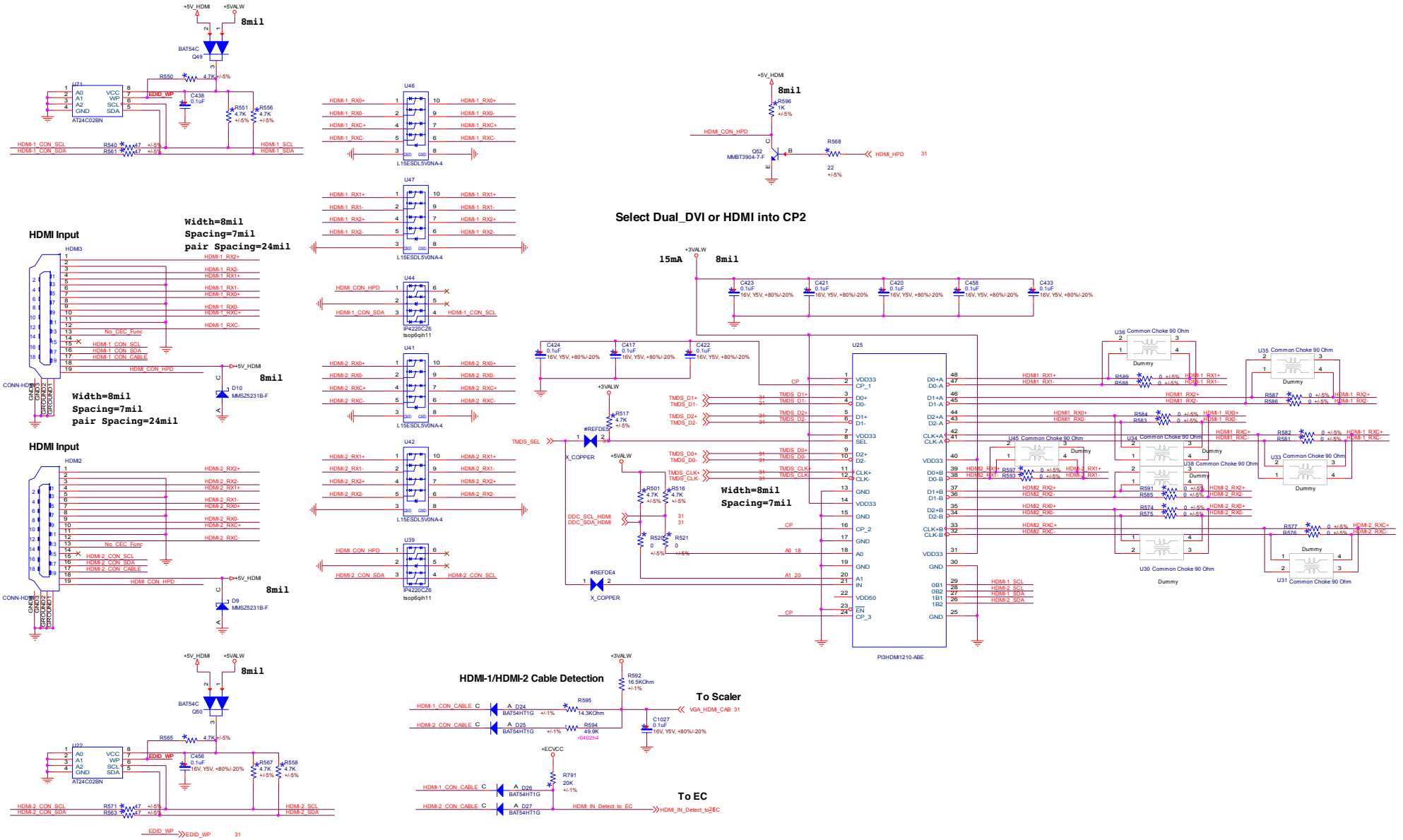
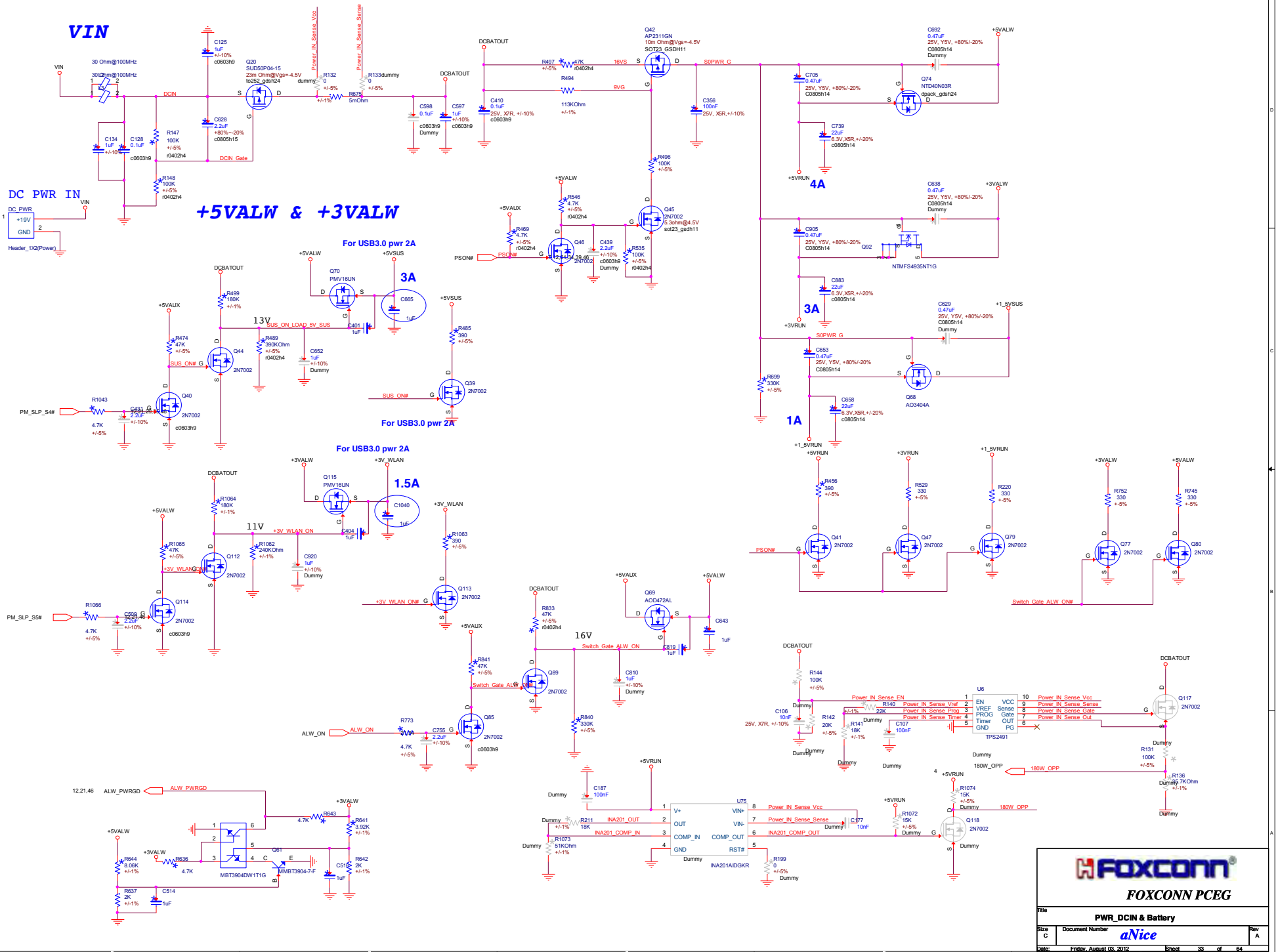
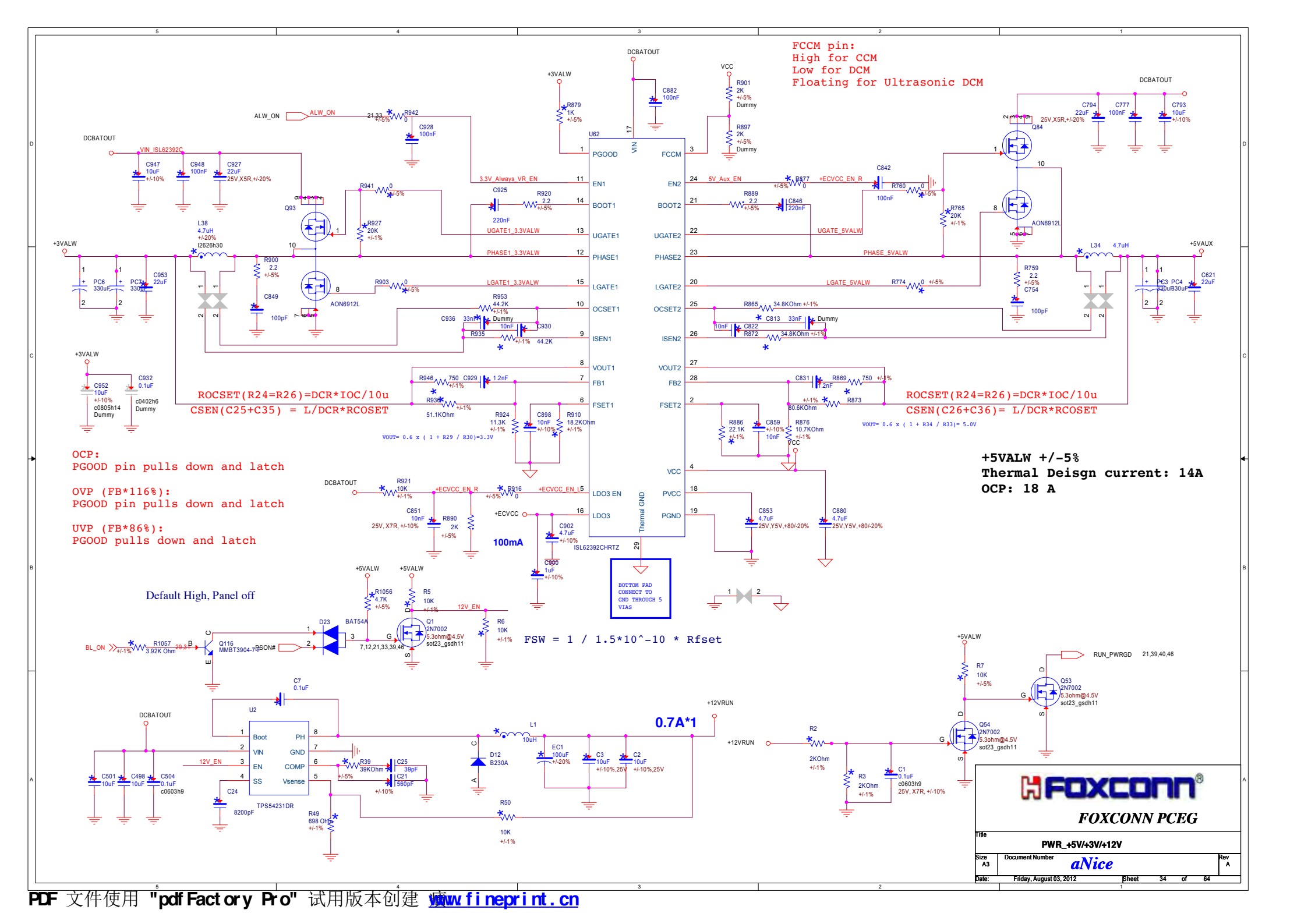


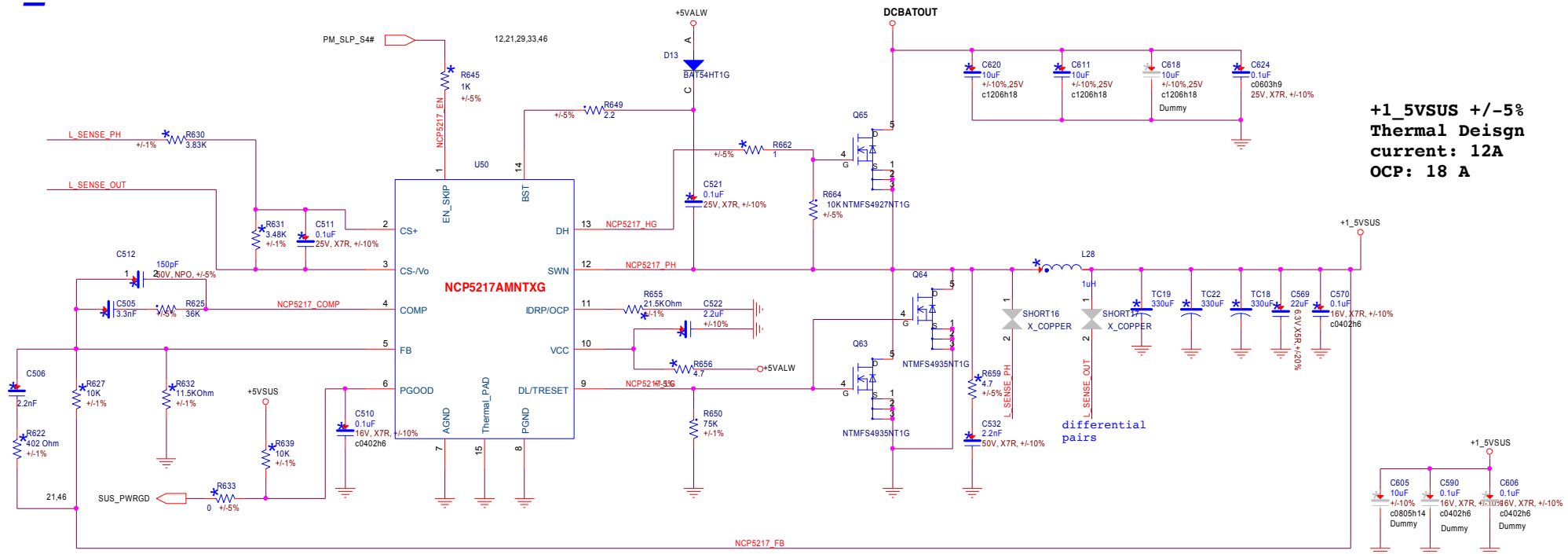
APPLICATION	GPIO USAGE
LED_GREEN	GPIO_1
LED_RED	GPIO_45
BACKLIGHT PWM	PWMD
EDID_WP	GPO_2
DUAL MODE CEC CONTROL	GPIO_16
AUDIO MUTE	GPIO_19
AUDIO GPIO CONTROL	GPIO_20
DUAL MODE CA_DET	GPIO_21
KEYPAD	LBADC_IN1
IR_IN/DPRX_POWER_DETECT	LBADC_IN2
VGA/HDMI CABLE DETECT	LBADC_IN3
DPRX_CABLE_DETECT	LBADC_IN4
LVDS POWER PIN CONTROL	GPIO_43
AUDIO POWER CONTROL	GPIO_44





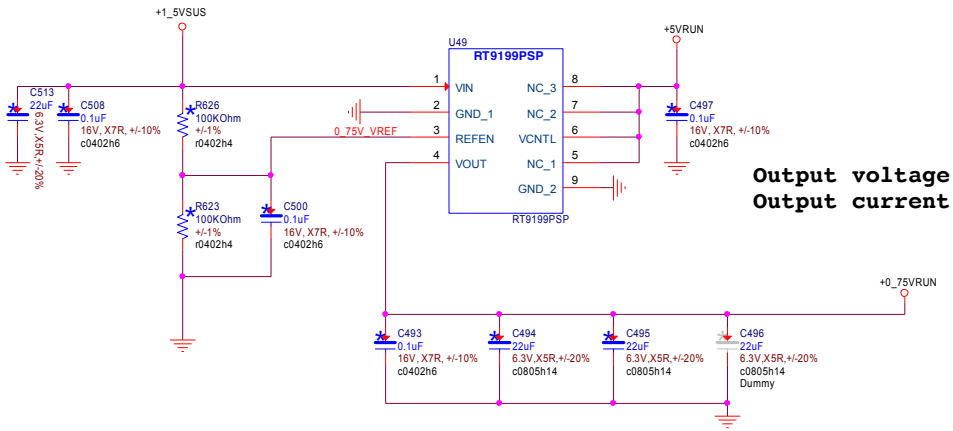


VCC_DDR



+1_5VSUS +/-5%
Thermal Deisgn current: 12A
OCP: 18 A

VTT_DDR



Output voltage: +0_75VRUN +/-5%
Output current: 1.5A

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Title: PWR_+1_5V/+0_75V			
Size: A3	Document Number: aNice		Rev: A
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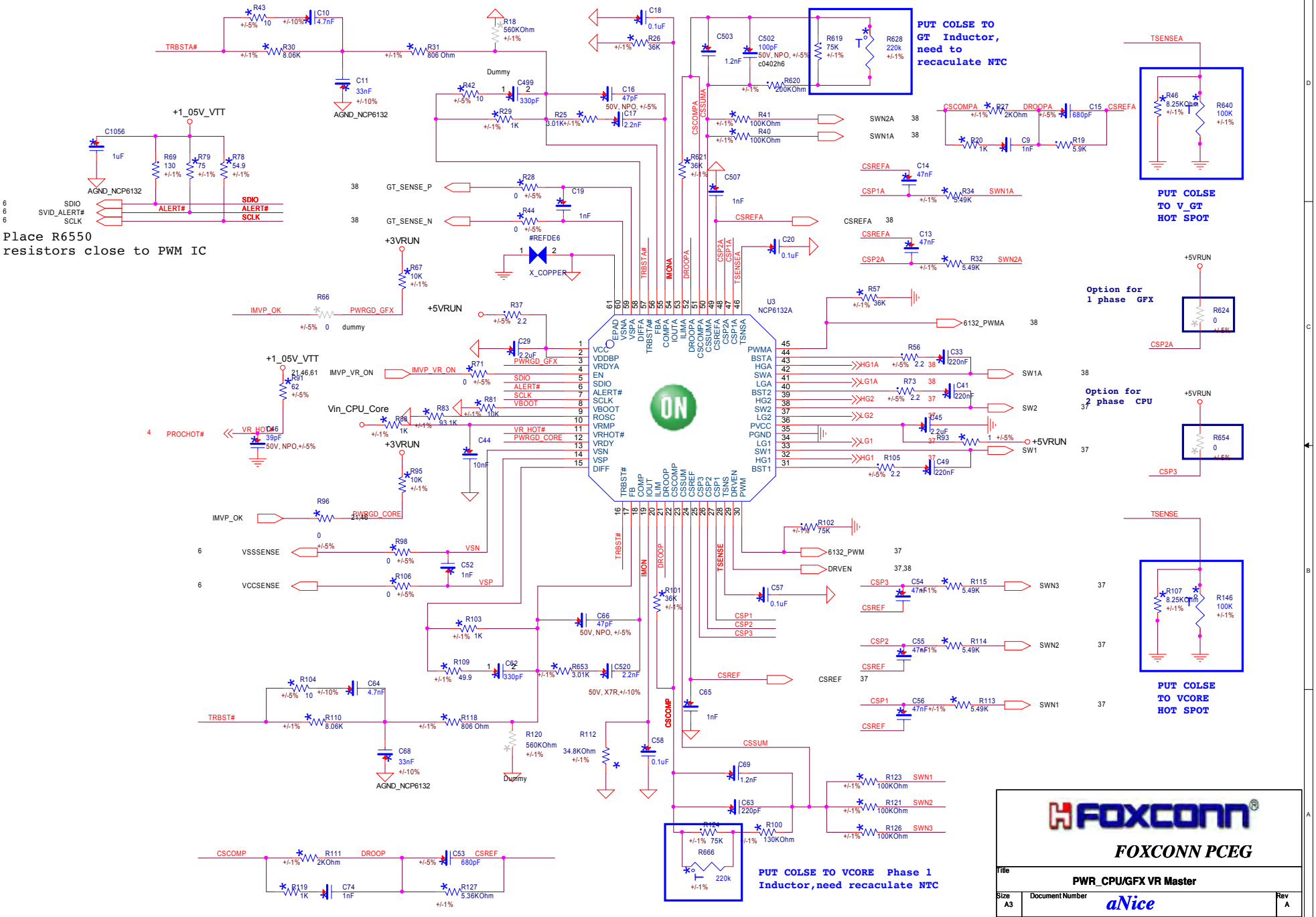

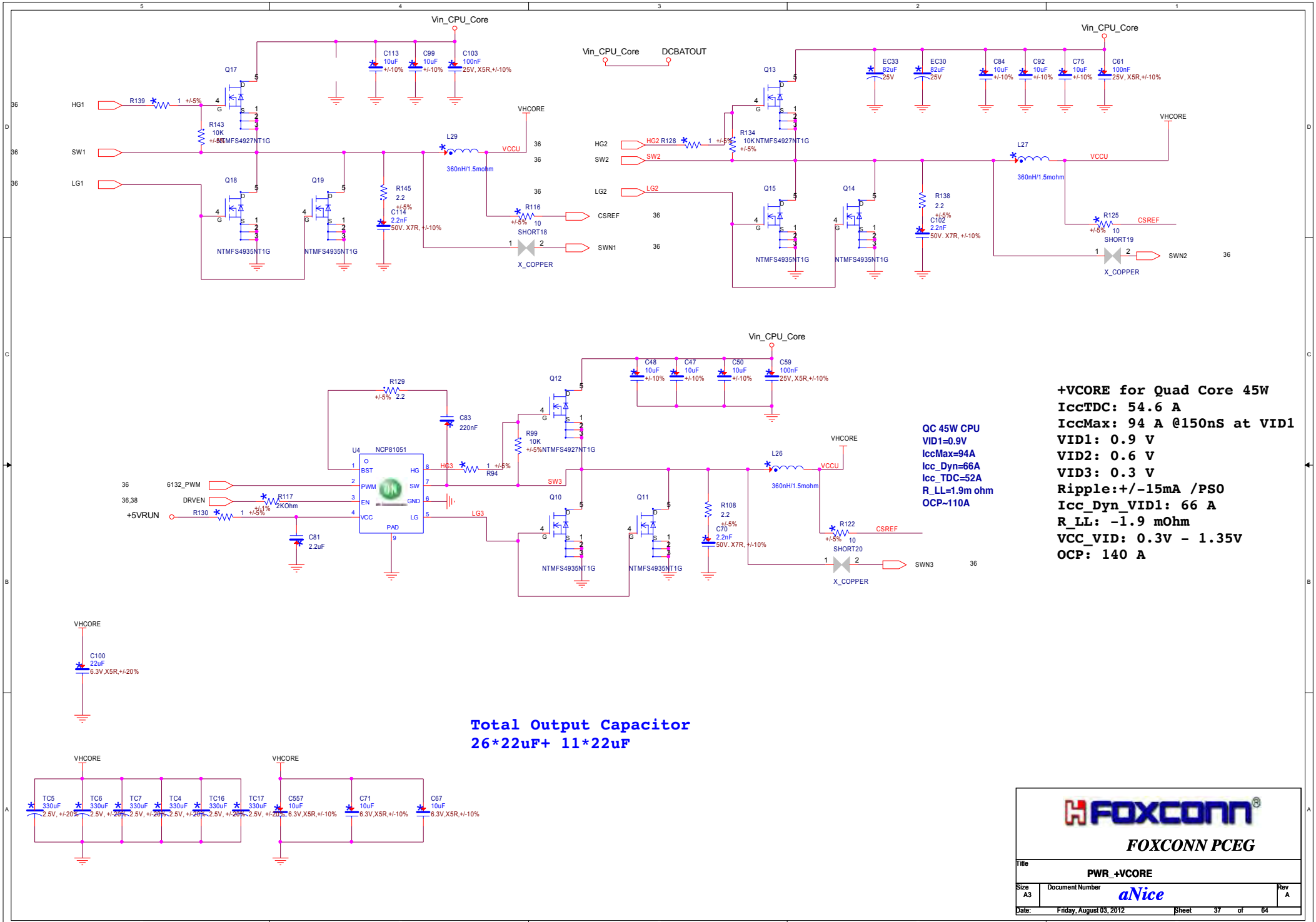

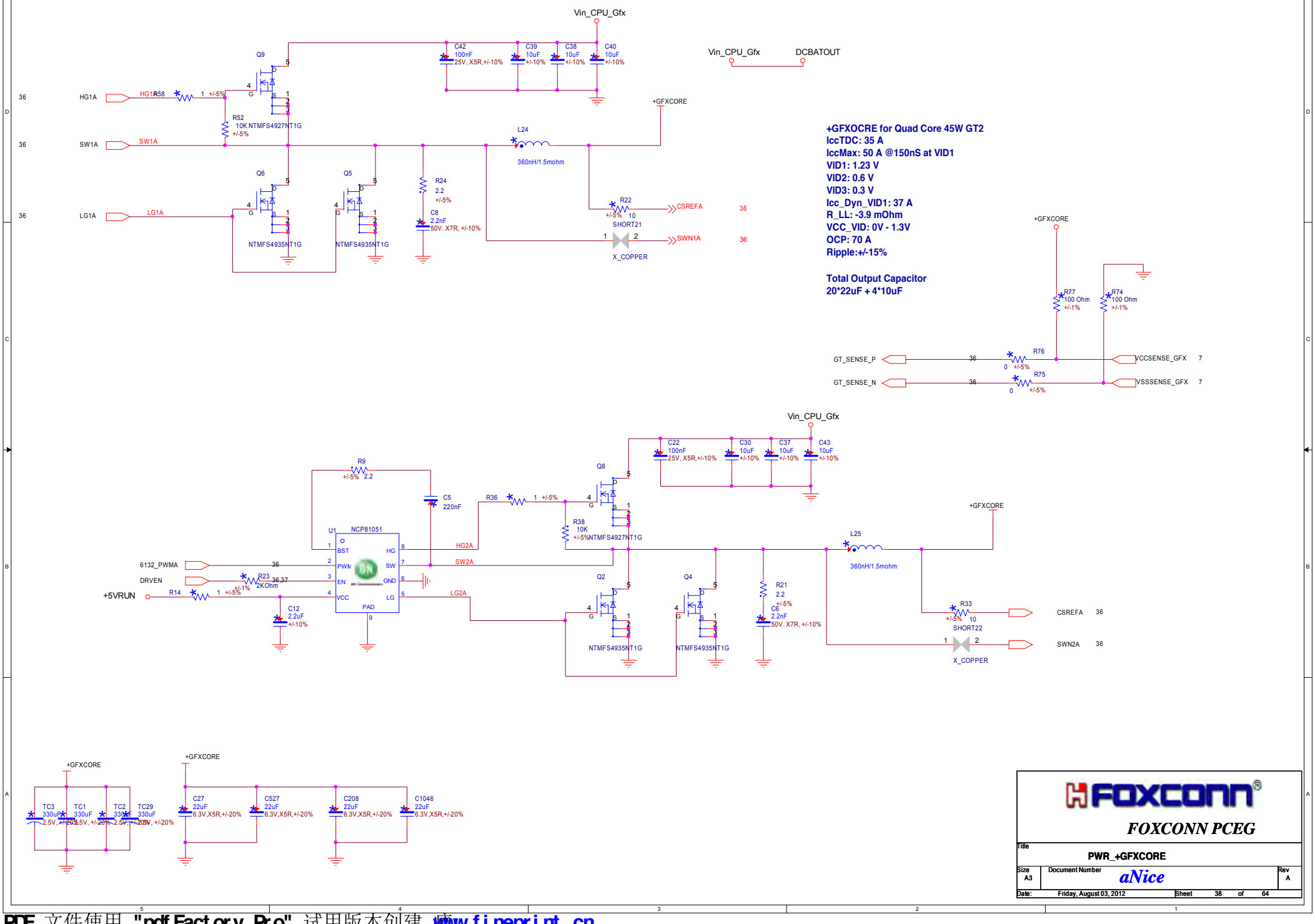

1.05V_PCH&VCCIO

Intel XE & SV

VID0	VID1	Vout
0	0	
0	1	
1	0	
1	1	0.675V

VCCIO has 1 select pin from the CPU which MUST be ignored (no connect). The Chief River platform will support a 1.05V VCCIO, and the selection of this voltage must be done on the board. From Doc#458544 PDDG, Page 78

Meet Intel spec.
DC+ripple:+-2%
AC:+/-3%
OCP:23A
Frequency: 300K

VCCIO_CPU 8.5A
+ PCH 6.75A

Output Voltage Need to Set to 1.05V Fixed.

15A
OCP-A

1D8V

+1_8VRUN +/-5%
Thermal Design Current: 1.2A
OCP: ? A

V_1P05_ME

VccASW Imax 0.803A

FOXCONN PCEG

Title: PWR_+1_05V_VTT/+1_8V
Size: A3
Document Number: aNice
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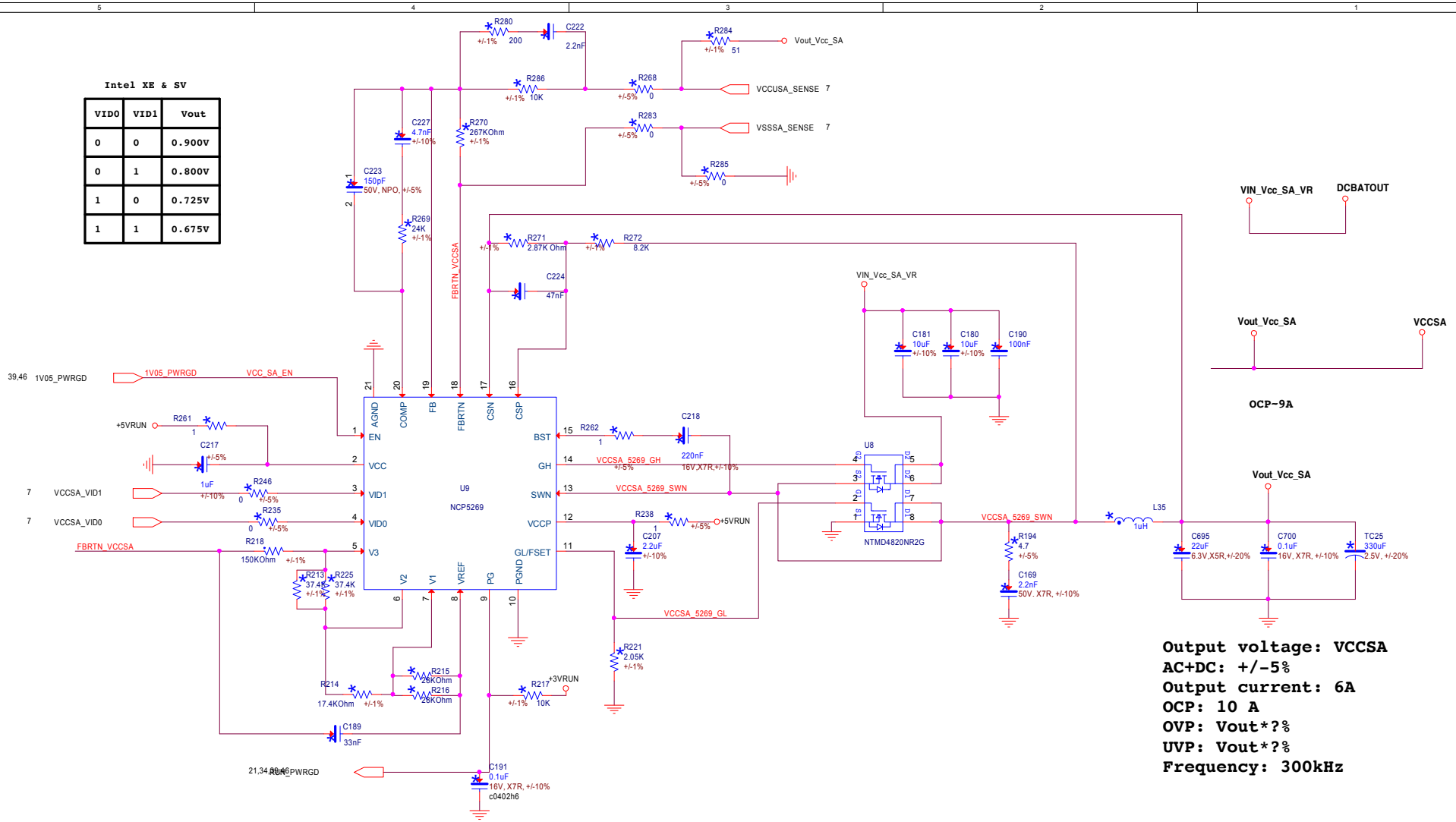

VID control table for VCCSA:

Function	VCCSA_VID0	VCCSA_VID1	Vout
SNB HIGH	0	0	0.9V
IVB HIGH	0	1	0.8V (Mode =open)
	0	1	0.85V (Mode =33k)
SNB LOW	1	0	0.725V
IVB LOW	1	1	0.675V

0.8V for 2011 SV processor and
0.85V for 2011 LV/ULV processor

FOXCONN PCEG

Title	PWR_VCCSA/+1_05V_PCH		
Size A3	Document Number aNice		Rev A
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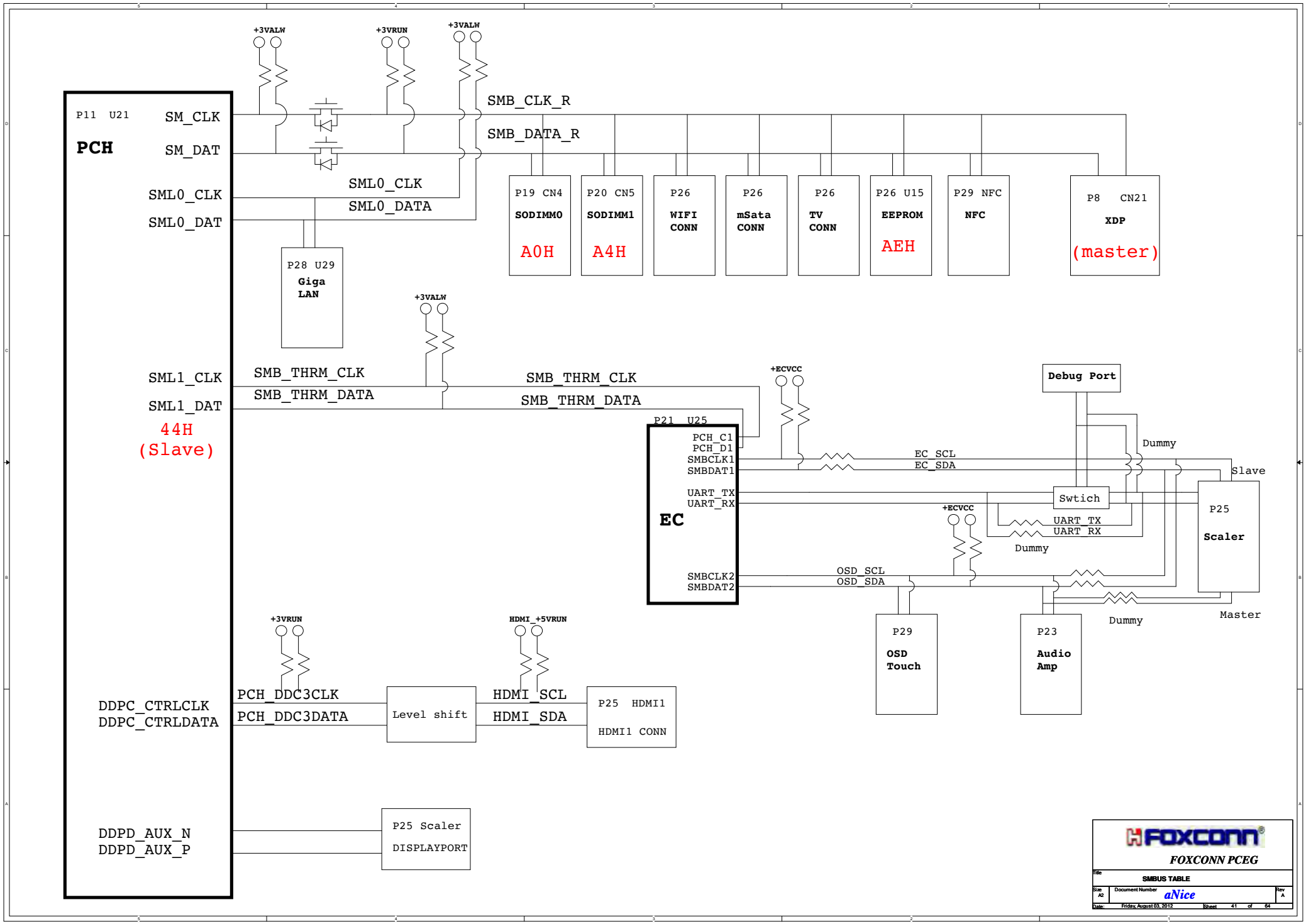

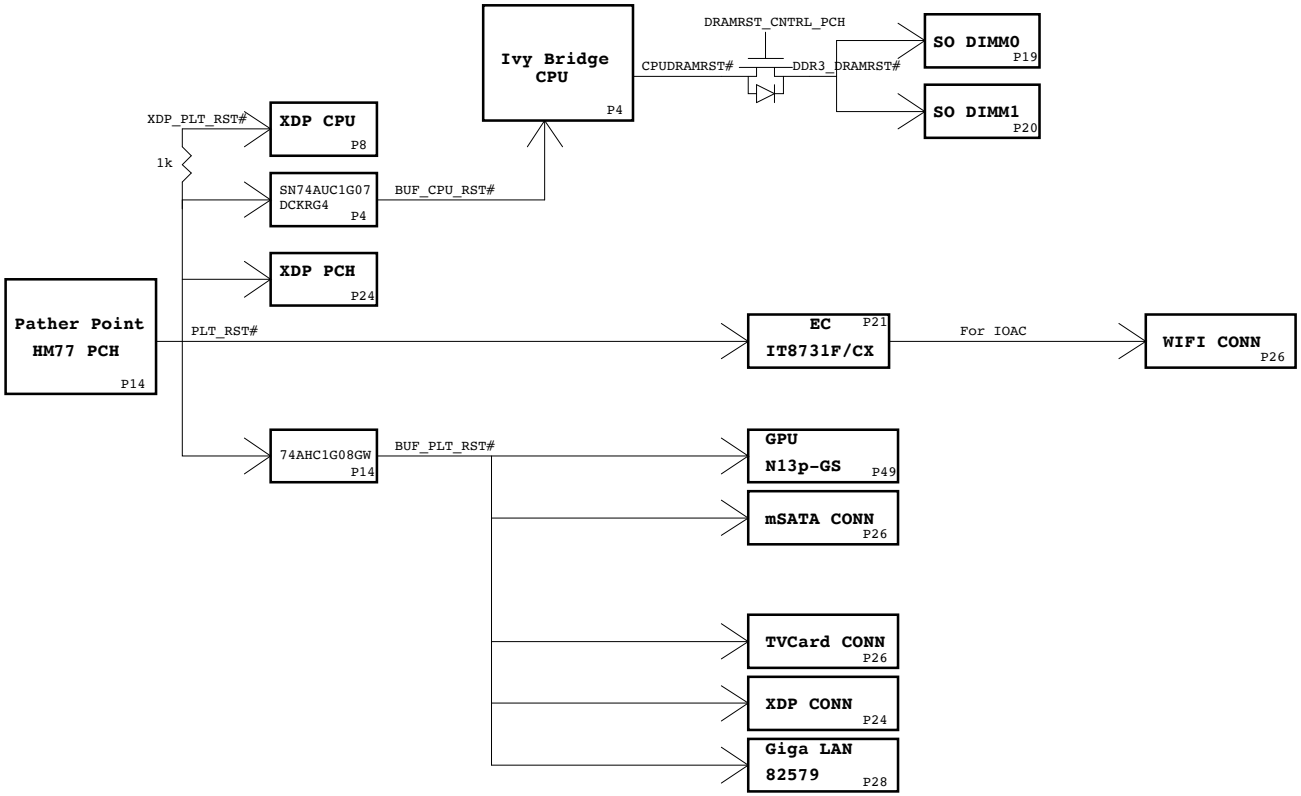

FOXCONN PCEG

Title: Reset Map

Size: A2 | Document Number: aNice | Rev: A

Date: Friday, August 03, 2012 | Sheet 42 of 64

	CPU Ivy Bridge	PCH Pather Point	DDR3	GPU N13P-GS /GL	EC IT8731/CX	USB Charger TPS2540RTE	RC Receiver	OSD Touch Panel Proximity	Scaler Board	NFC	Touch Panel	KB/MS Receiver	Camera & Digital Mic	Audio: CODEC ALC662	Audio: AMP LM48901SQ	Audio: SPDIF//I2C DIR9001PW	Audio: I2C//IS2S PCM1754	HDMI PI3VDP411 LSRZBE	Mini PCIE: mSATA	Mini PCIE: WIFI	Mini PCIE: TV Card	Card Reader RTS5209-GR	LAN 82579	USB2.0 &USB3.0 CONN	SATA &ODD	FAN
S0	VHCORE +GFXCORE VCCSA +1_8VRUN +1_5VSUS	+1_05V_PCH +1_05V_VTT +V1_5VRUN +1_8VRUN +3VRUN +5VRUN +5VALW	DDR3_VREF +1_5VSUS +3VRUN	NVVDD FBVDD FBVDDQ PEX_VDD PEX_PLLVDD 3V3_NV 1V8_NV LVDS_PP	+3VRUN +3VALW +ECVCC	+5VALW	+5VALW	+3VALW +5VALW	+3VALW +5VALW	+5VSUS	+5VSUS	+5VSUS	+3VRUN	+3VRUN +5VSUS	+3VALW +5VALW 1.8VALW	+3VALW	+5VALW	+3VRUN +5VRUN	+3VRUN +V1_5VRUN	+3VALW +V1_5VRUN	+3VRUN +V1_5VRUN	+5VSUS	+3V_LAN	+5VSUS	+5VRUN	+12VRUN
S3	+1_5VSUS	+3VALW +5VALW	+1_5VSUS		+3VALW +ECVCC	+5VALW	+5VALW	+3VALW +5VALW	+3VALW +5VALW	+5VSUS	+5VSUS	+5VSUS		+5VSUS	+3VALW +5VALW 1.8VALW	+3VALW	+5VALW			+3VALW		+5VSUS	+3V_LAN	+5VSUS		
S4/S5 with WOL		+3VALW +5VALW			+3VALW +ECVCC	+5VALW	+5VALW	+3VALW +5VALW	+3VALW +5VALW						+3VALW +5VALW 1.8VALW	+3VALW	+5VALW			+3VALW			+3V_LAN			
S4/S5 without WOL		+3VALW +5VALW			+3VALW +ECVCC	+5VALW	+5VALW	+3VALW +5VALW	+3VALW +5VALW						+3VALW +5VALW 1.8VALW	+3VALW	+5VALW			+3VALW						
EUP6					+ECVCC	+5VAUX		+3VAUX +5VAUX																	

FOXCONN PCEG

Title: Device Power Status Table

Size: Custom | Document Number: aNice | Rev: A

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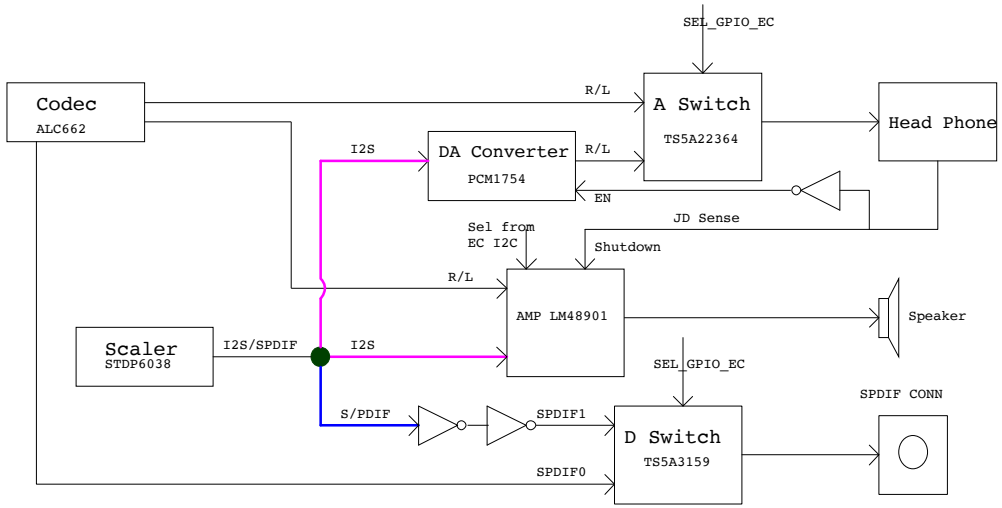

PC Mode		
Headphone	ON	OFF
Speaker	OFF	ON/OFF
SPDIF	ON/OFF	ON/OFF

HDMI INPUT Mode			
Headphone	ON	OFF	OFF
Speaker	OFF	ON	OFF
SPDIF	OFF	OFF	ON

FOXCONN PCEG

Title: Audio MAP

Size: C | Document Number: aNice | Rev: A

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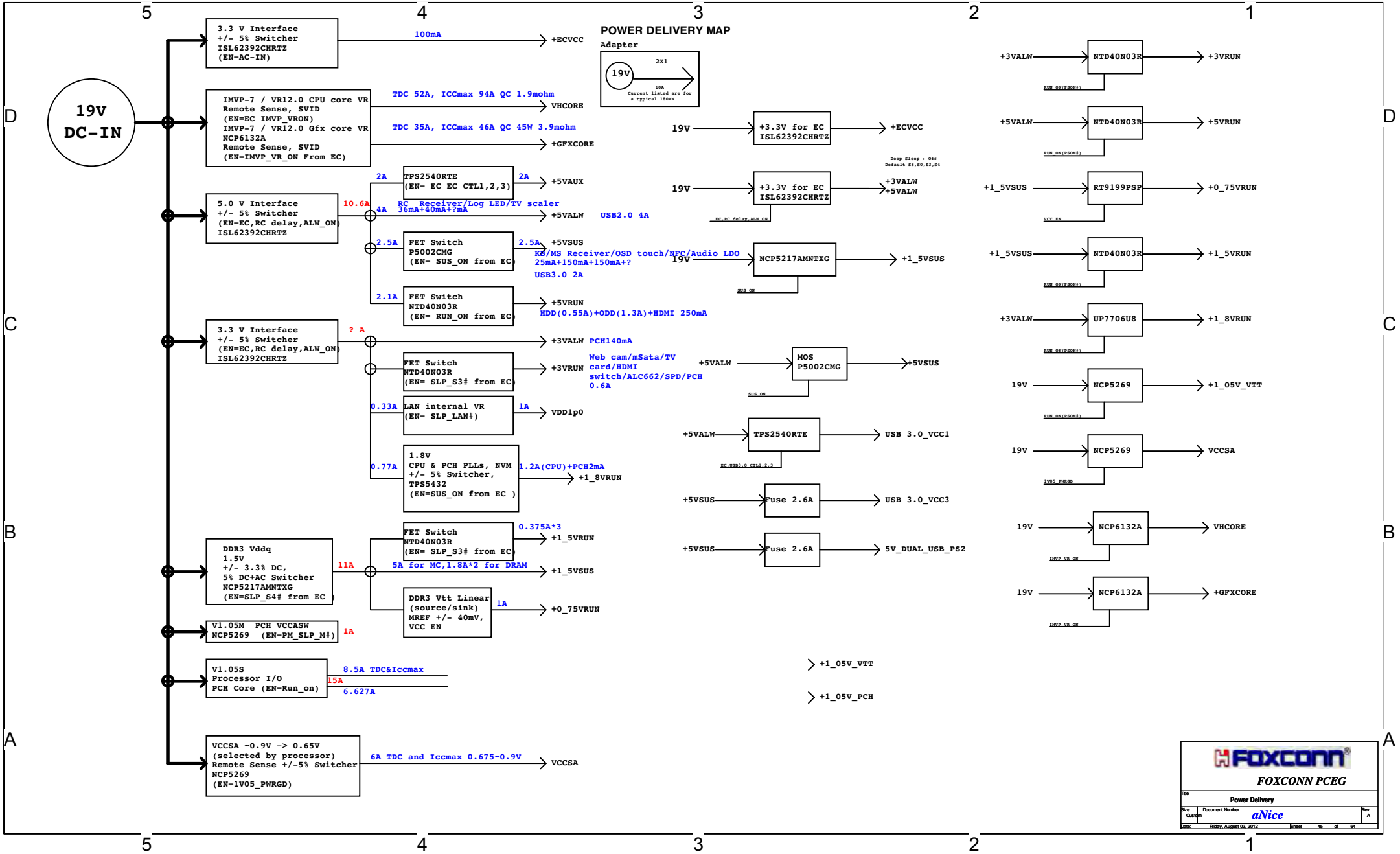
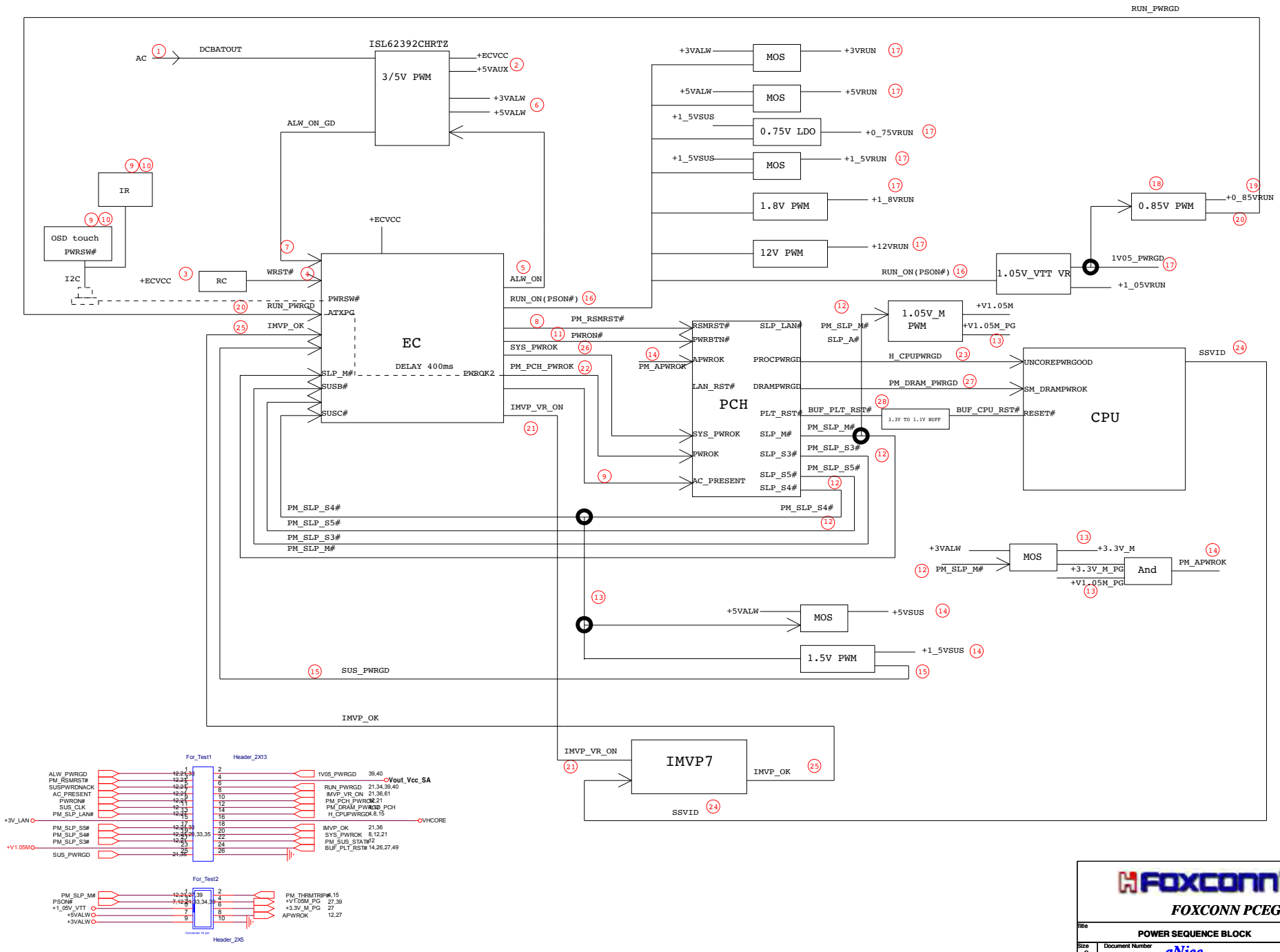




FOXCONN PCEG

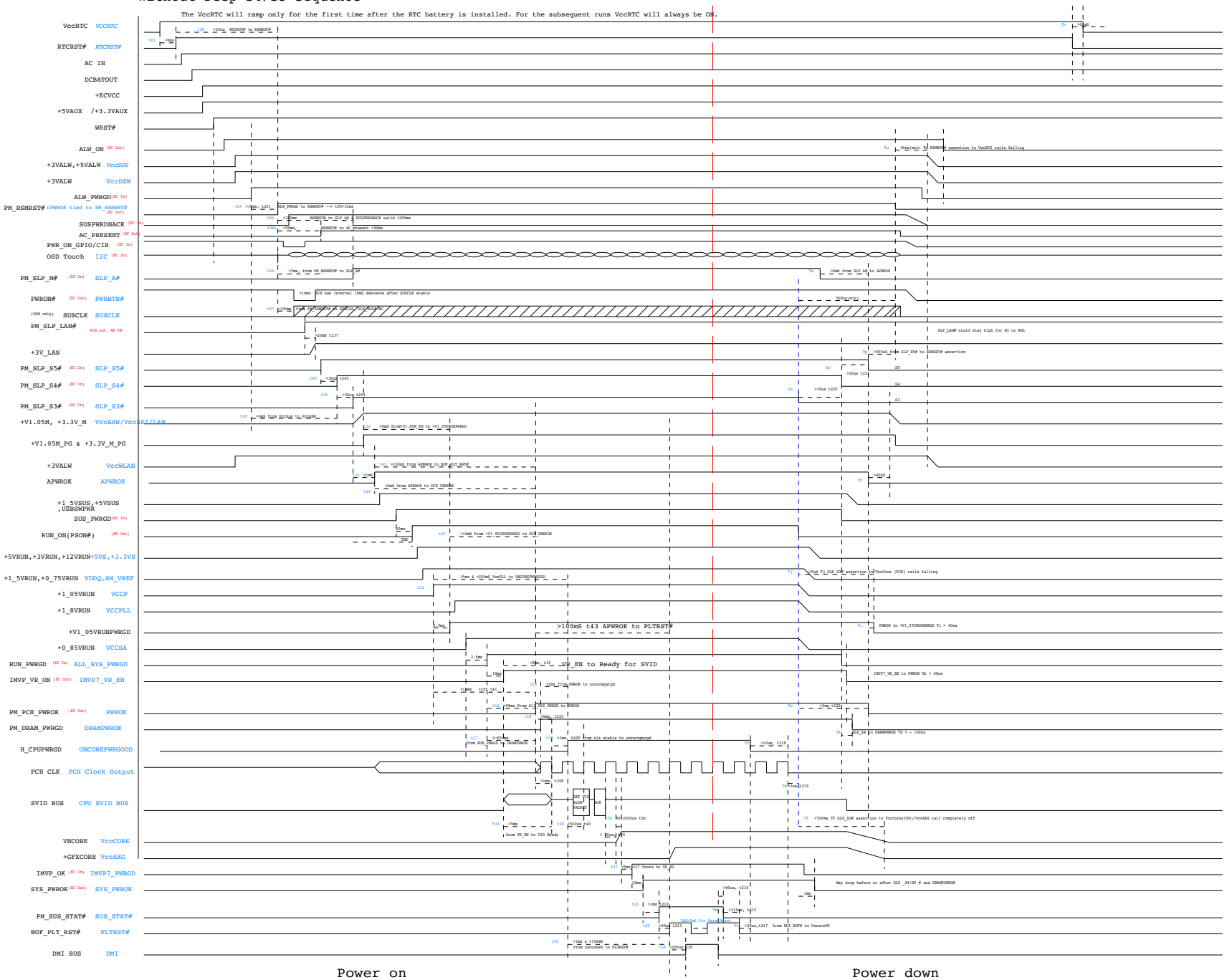
Title: POWER SEQUENCE BLOCK

Size: C | Document Number: aNice | Rev: A

Date: Friday, August 03, 2012 | Sheet 46 of 64

Without Deep S4/S5 sequence

The VccRTC will ramp only for the first time after the RTC battery is installed. For the subsequent runs VccRTC will always be ON.



FOXCONN PCEG

Title	POWER SEQUENCE	
Size: Custom	Document Number: aNice	Rev: A
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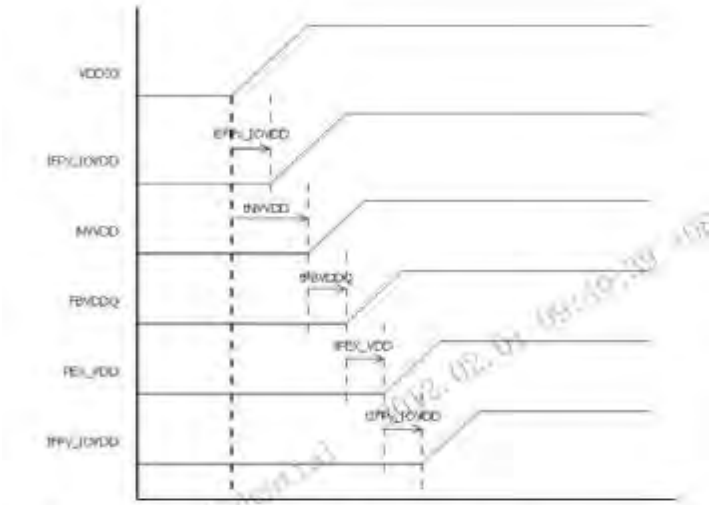

Figure 17. Recommended Power On Sequencing Order

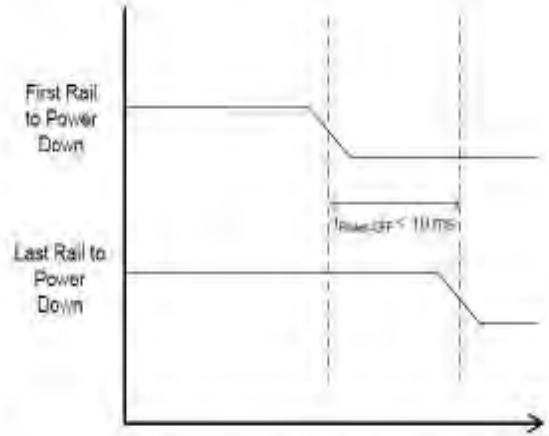

Figure 18. Recommended Power Off Sequencing Order

Table 72. DVI Power Rails

Power Rails	Voltage	Max. Current Draw[1]
IFPx_IOVDD (x= E, F)	1.05 V ±30 mV	72 mA each
IFPy_PLLVDD (y= EF)	3.3 V ± 5%	190 mA each

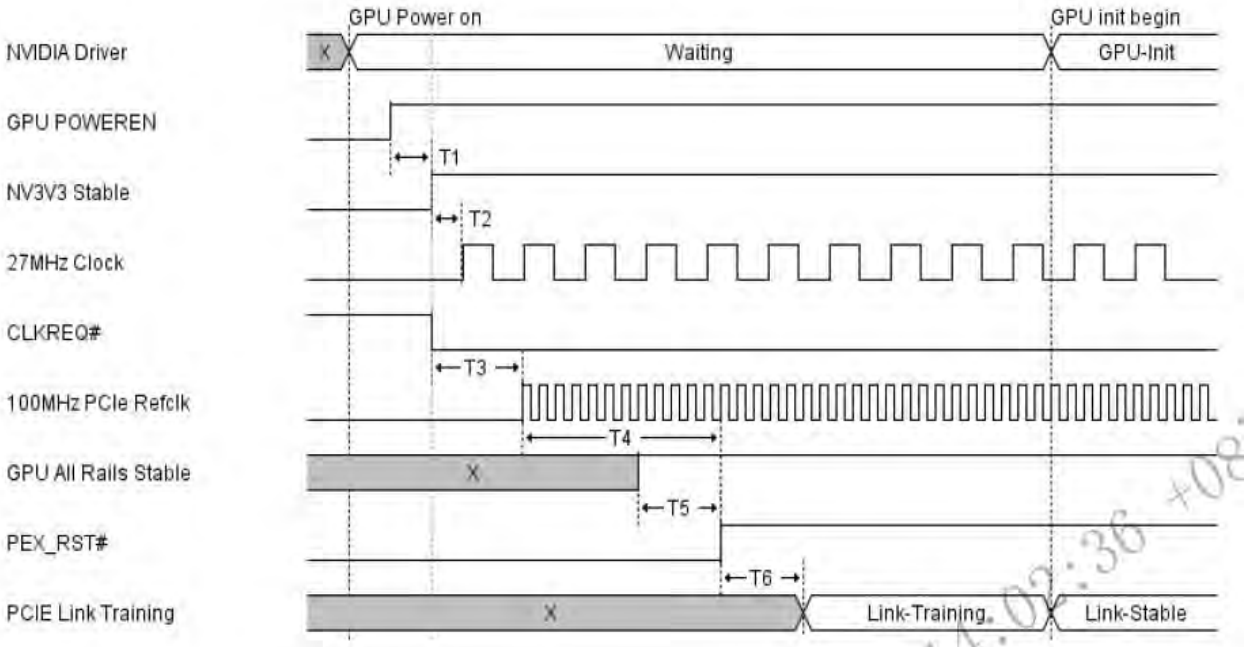

Figure 2. Typical Power-Up Sequence

FOXCONN PCEG

Title: GPU Sequence

Size: B | Document Number: aNice | Rev: A

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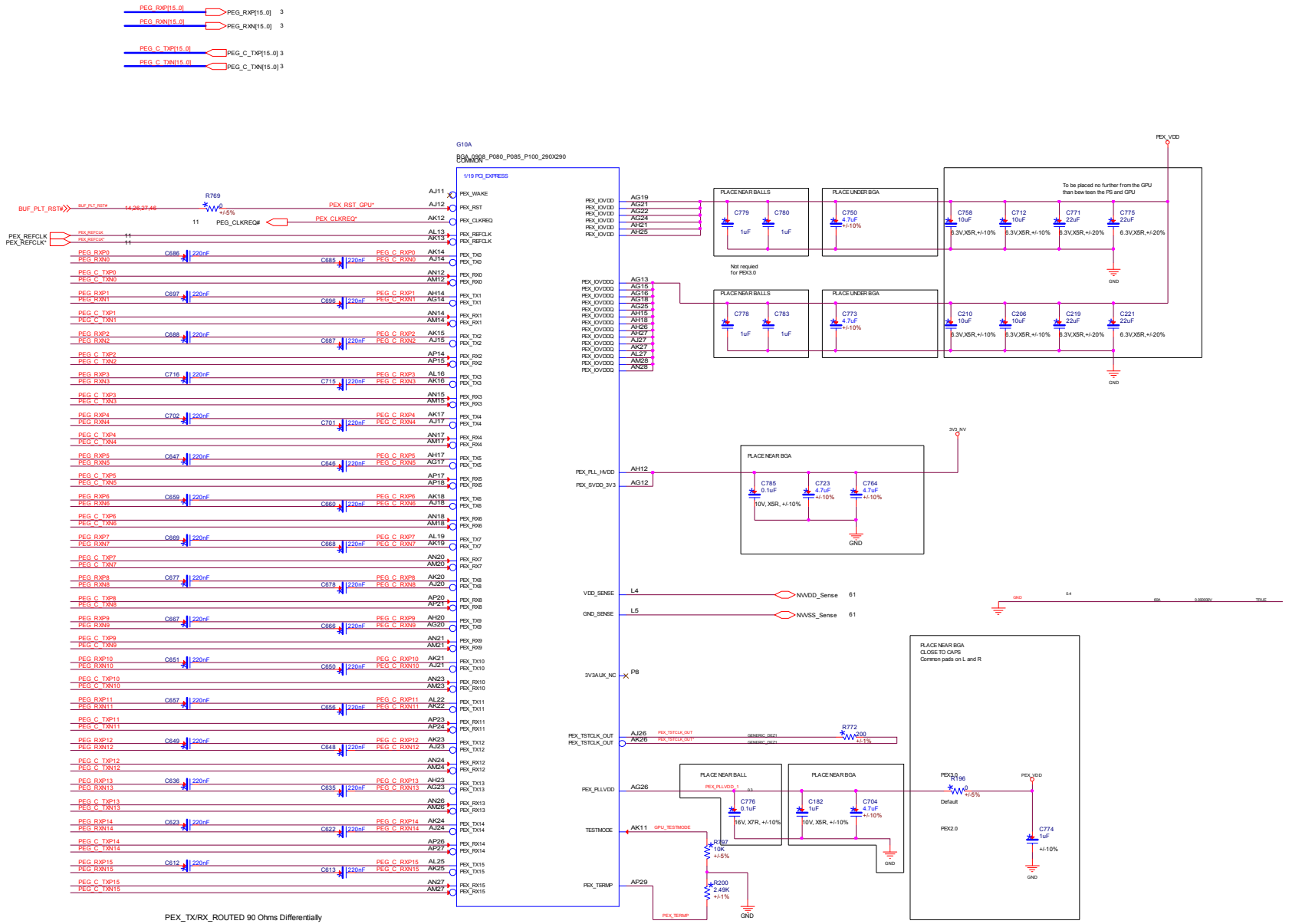
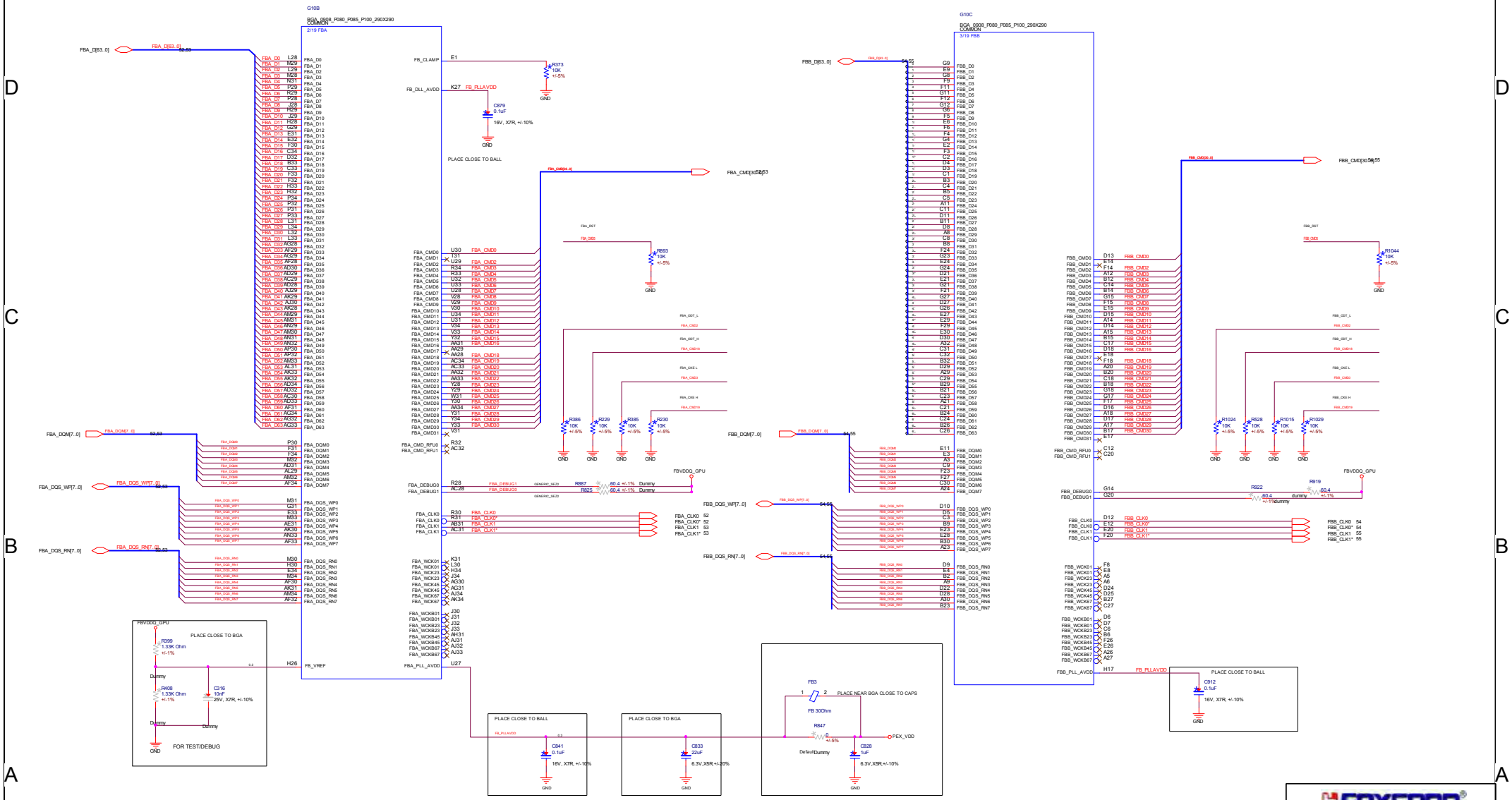


Frame Buffer Partitions A/B



FOXCONN PCEG

Title: Frame Buffer Partitions A/B

Size: Custom | Document Number: aNice | Rev: A

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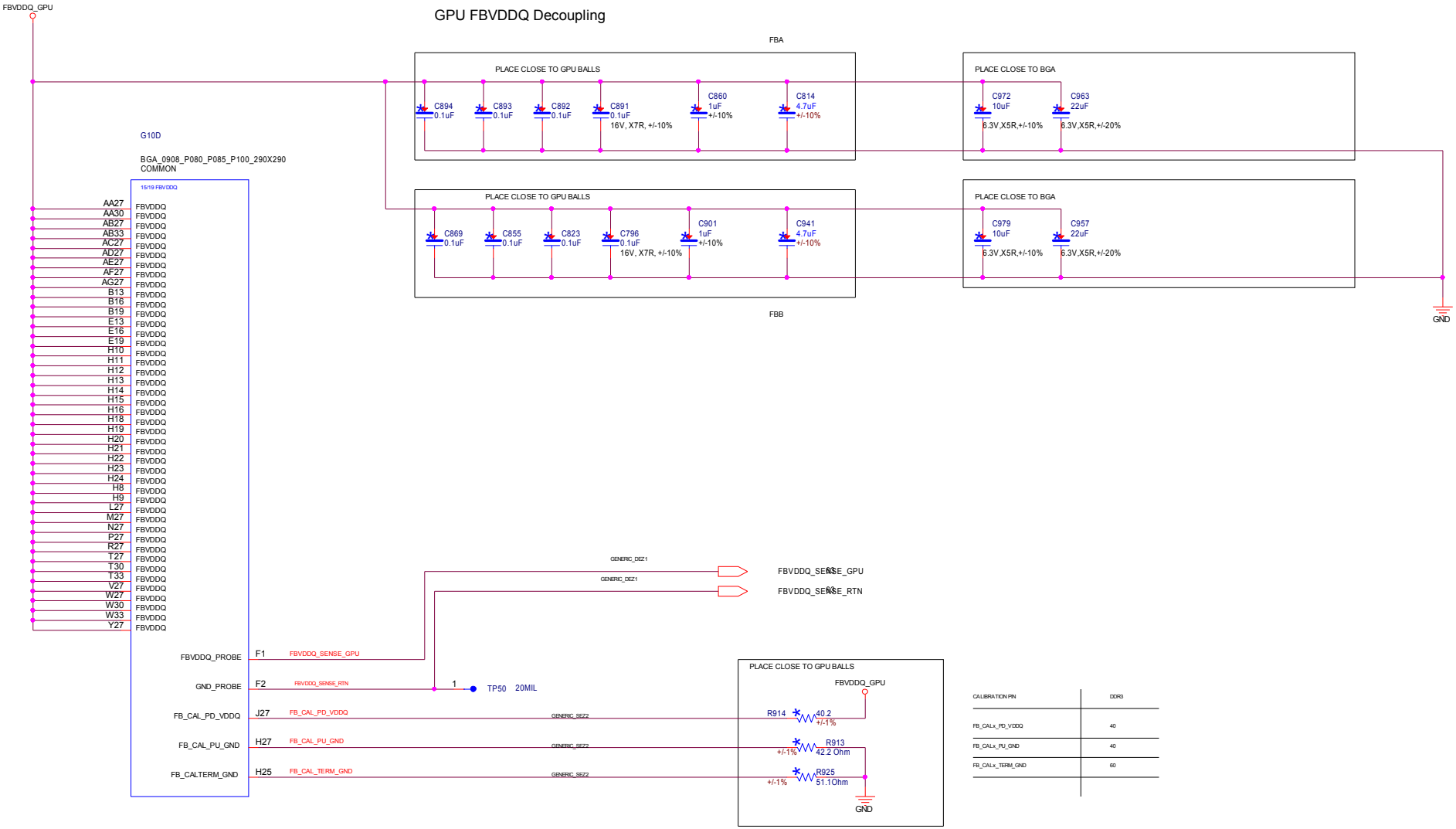
Frame Buffer FBVDDQ Power/Decoupling/Calibration



FOXCONN PCEG

Title: Frame Buffer FBVDDQ Power/Decoupling/Calibration

Size	Document Number	Rev
A3	aNice	A

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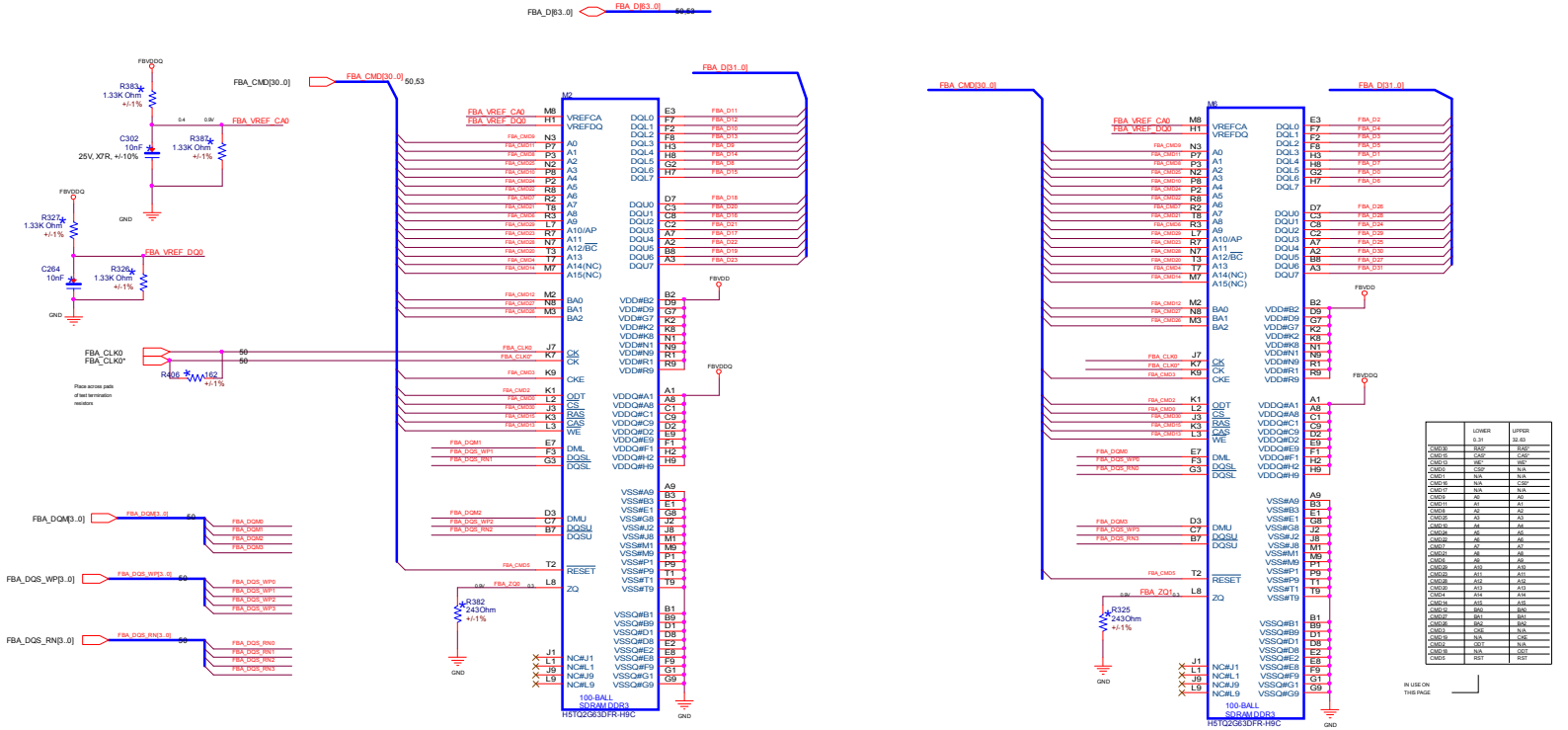
Memory Lower Partition A



	LOWER	UPPER
	0..31	32..63
CMD16	RAS*	RAS*
CMD15	CAS*	CAS*
CMD13	WE*	WE*
CMD0	CS0*	N/A
CMD1	N/A	N/A
CMD16	N/A	CS0*
CMD17	N/A	N/A
CMD9	A0	A0
CMD11	A1	A1
CMD8	A2	A2
CMD5	A3	A3
CMD10	A4	A4
CMD6	A5	A5
CMD4	A6	A6
CMD7	A7	A7
CMD14	A10	A10
CMD12	BA0	BA0
CMD17	BA1	BA1
CMD26	BA2	BA2
CMD3	A9	A9
CMD19	N/A	CKE
CMD2	ODT	N/A
CMD18	N/A	ODT
CMD0	RST	RST

IN USE ON THIS PAGE

FBA_CLK/* 80DEZ

FBA_DQS_WP/RN 80DEZ

FBA_DQ/M_WP/RN 45SEZ

FBA_CMD 45SEZ

FOXCONN PCEG

Title: Memory Lower Partition A

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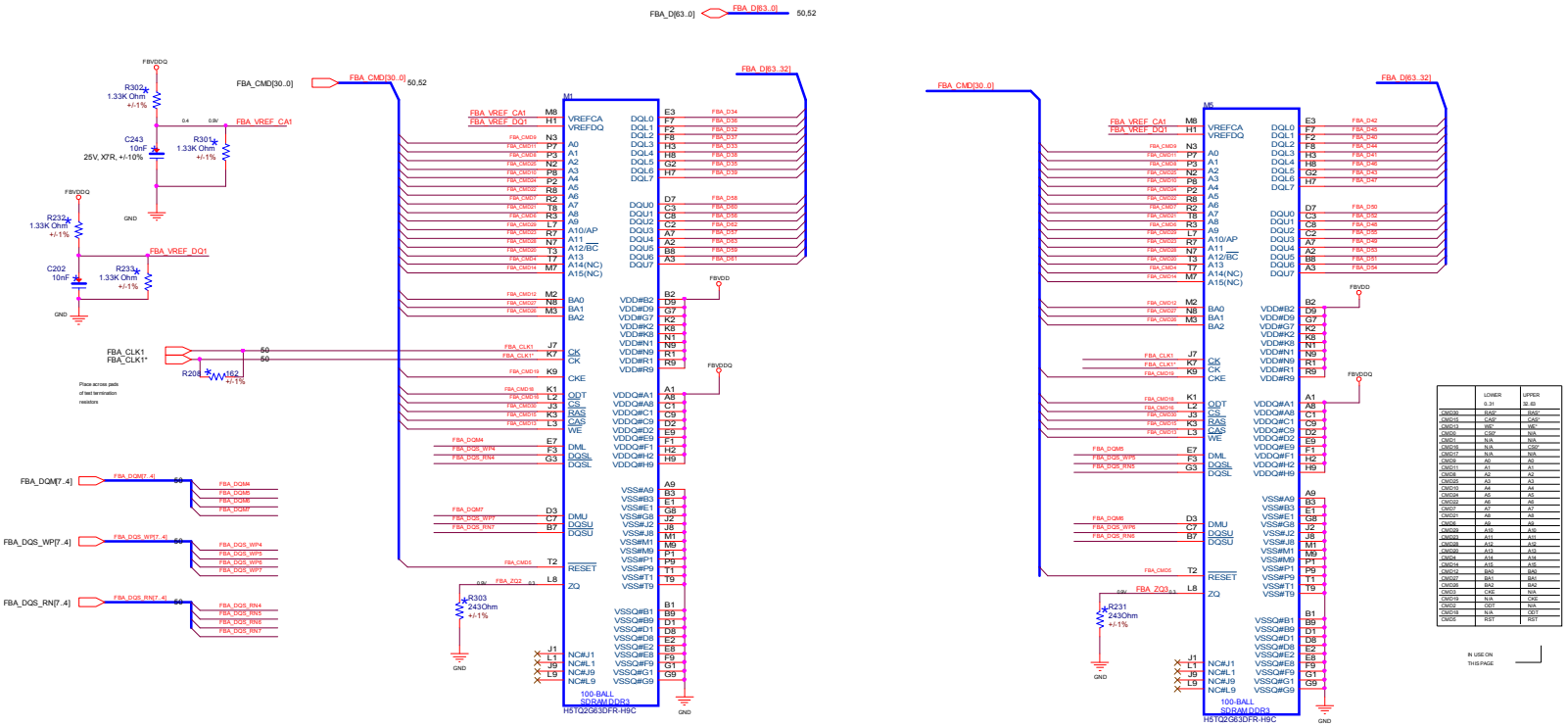

FOXCONN PCEG

Title: Memory Upper Partition A

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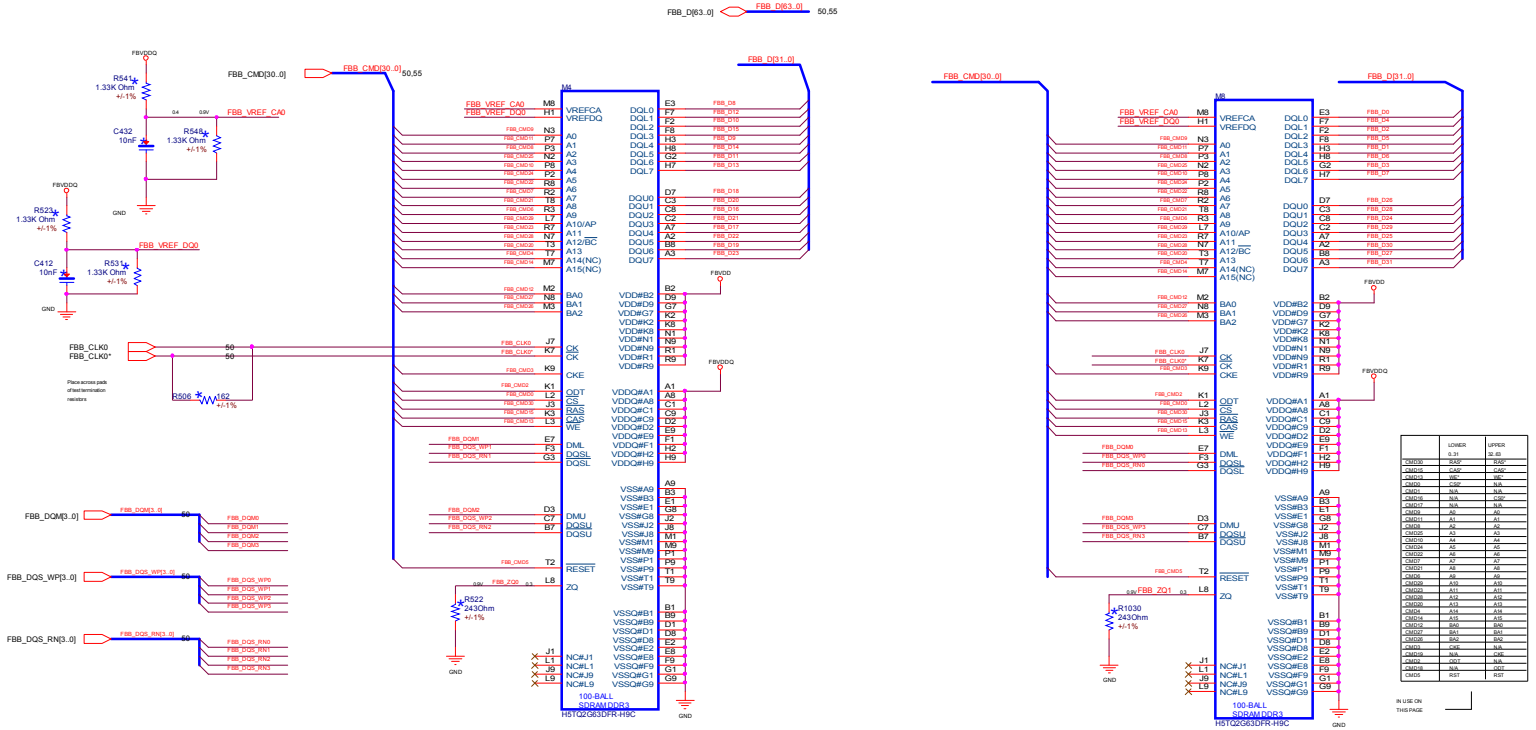
Memory Lower Partition B



FOXCONN PCEG

Title: Memory Lower Partition B

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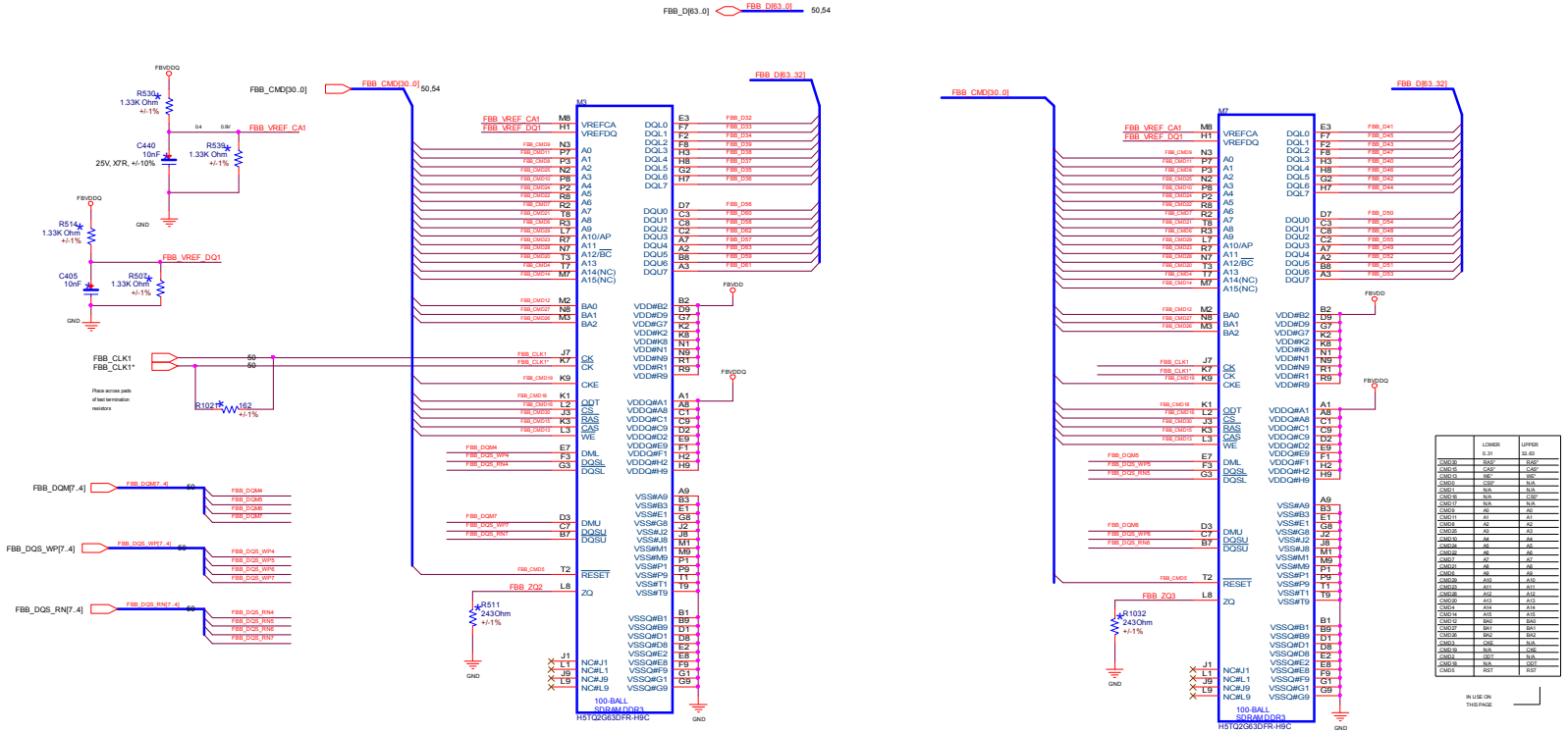
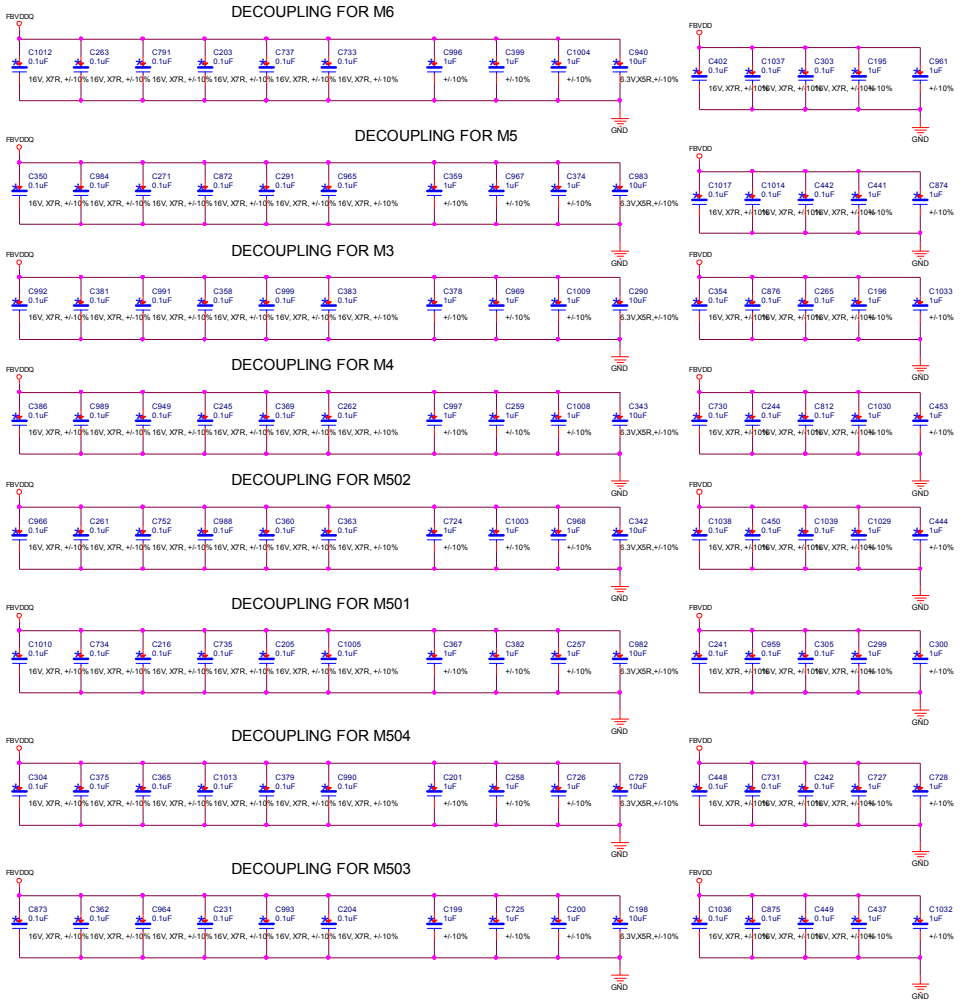
Memory Upper Partition B



Memory FBVDD/Q Decoupling



FOXCONN PCEG

Title	Memory FBVDD/Q Decoupling	
Size A2	Document Number aNice	Rev A
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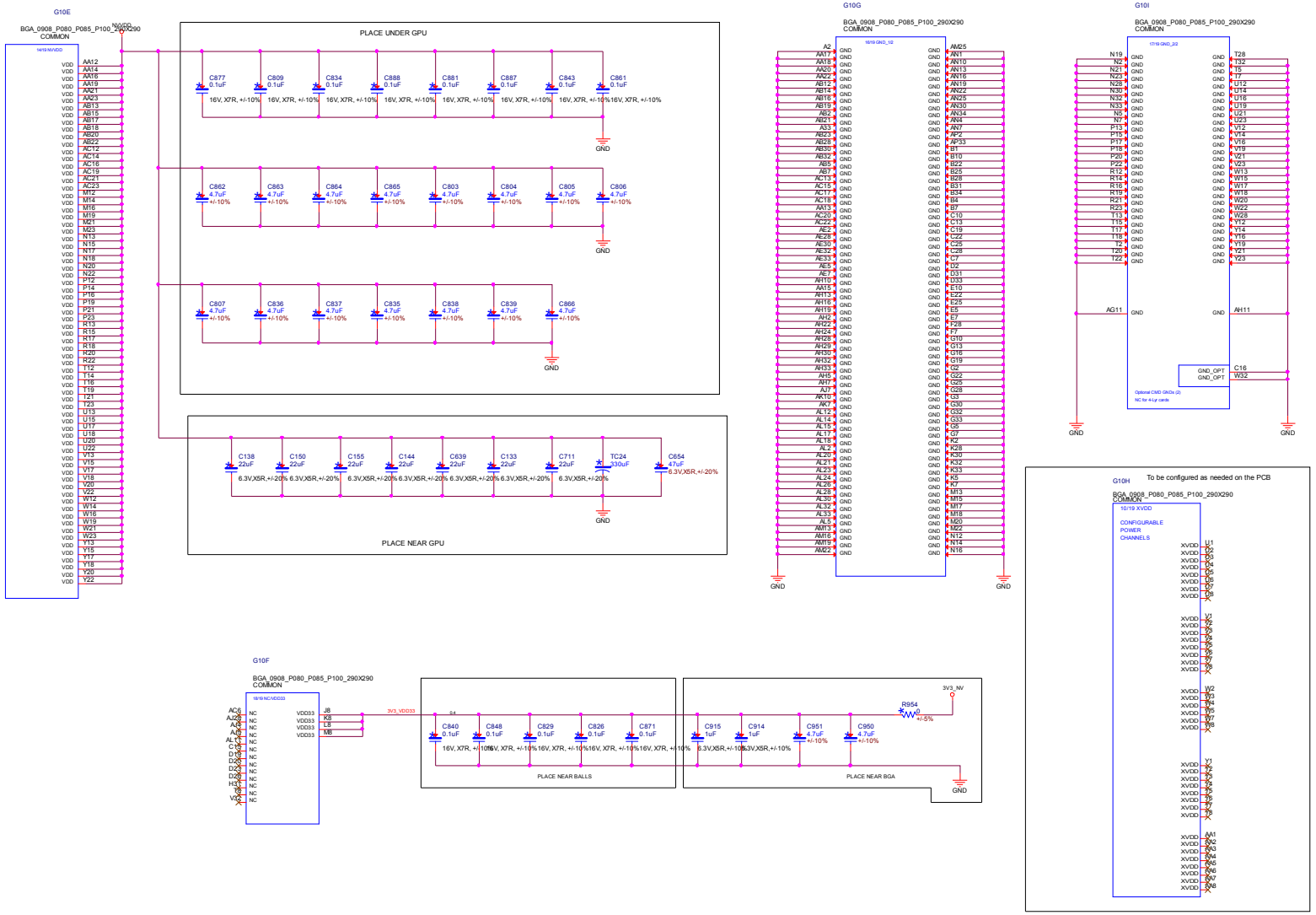
Power/Decoupling: NVVDD,3V3_NV,GRND,and Optional



FOXCONN PCEG

Title: Power/Decoupling: NVVDD,3V3_NV,GRND,and Optional

Size: Custom | Document Number: aNice | Rev: A

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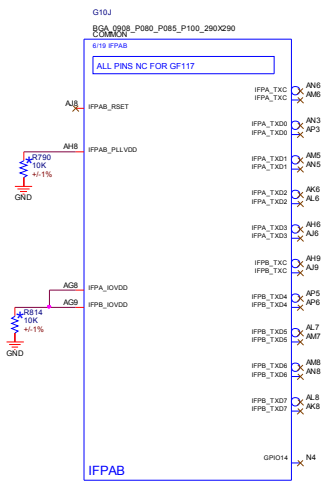
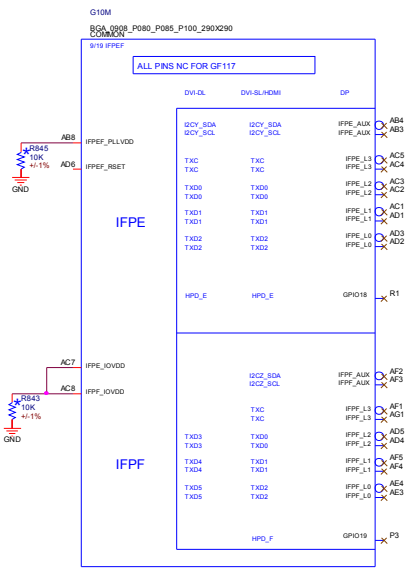
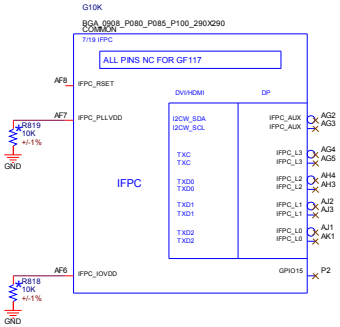
IFPA/B LVDS Dual Link



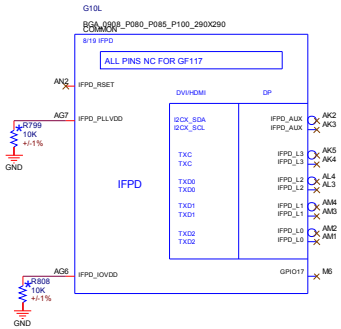
IFPE/F Dual Link TMDS DVI-I



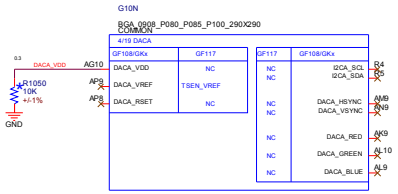
IFPC NATIVE HDMI OR DP



IFPD DUAL MODE DP



DAC_A VGA



FOXCONN PCEG

Title	GPU I/O		
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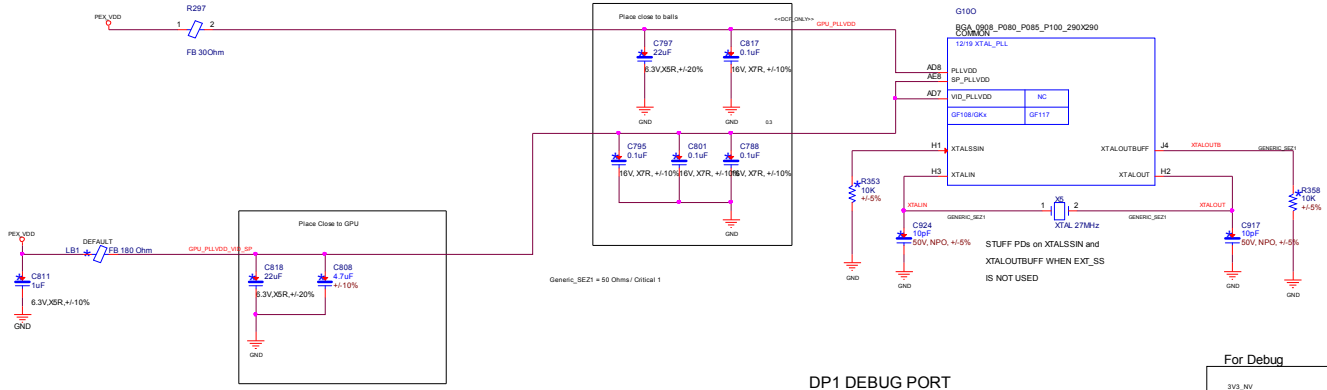
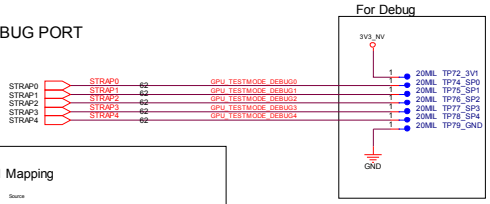
BIOS, External SS, and Mechanical Components



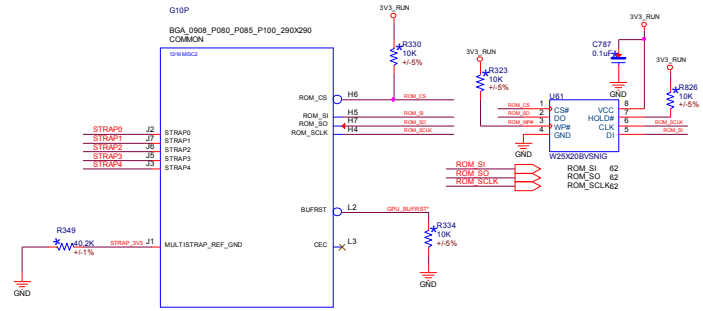
DP1 DEBUG PORT



Debug Port_1 Mapping

Debug[x]	Source
DEUG_PORT[0]	STRAP0
DEUG_PORT[1]	STRAP1
DEUG_PORT[2]	STRAP2
DEUG_PORT[3]	STRAP3
DEUG_PORT[4]	STRAP4
DEUG_PORT[5]	Gpio[0]
DEUG_PORT[6]	Gpio[1]
DEUG_PORT[7]	GPIO[12]

BIOS ROM



MECHANICAL COMPONENTS

GF117/GK10X STRAPPING MODE TABLE

PIN NAME	MULTI-LEVEL	BINARY PRODUCTION	BINARY BRINGPUP
MULTI_STRAP_REF_GND	40.2K TO GND	NOT SUPPORTED	NO STUFF

FOXCONN PCEG

Title: BIOS, External SS, and Mechanical Components

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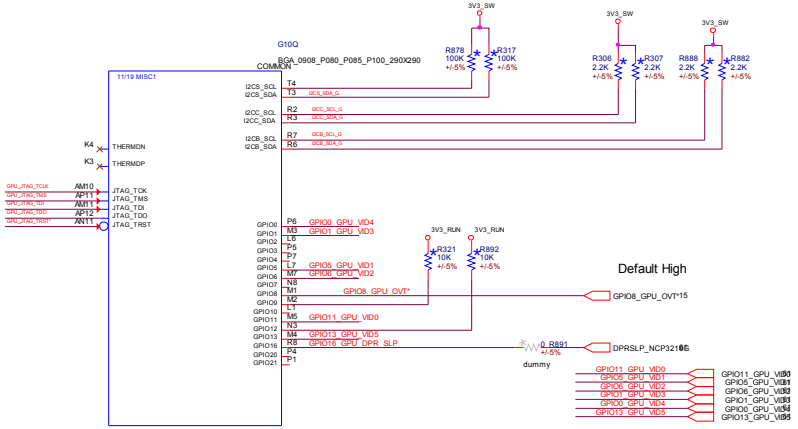
GPIOs, Thermal Sensor, I2C/GPIO Expanders

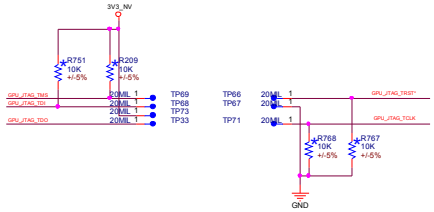
TEMP SENSOR

Route THERMDA/DC at 0.125mm spacing with 0.125mm gmd guard traces

Place close to GPU near thermal diode balls



JTAG CONNECTOR



GPIO	Function		GPIO	Function
GPIO 0	Debug/Service Header/Alt_Fan PWM			I2C PORT C
GPIO 1	VID 2		EXPND 0	Level Shifter Error Correction
GPIO 2	LCD brightness control (BL PWM)		EXPND 1	NVGEM GPIO EXP1/ PS_Margin*
GPIO 3	LCD Power enable (PPEN)		EXPND 2	NVGEM GPIO EXP2/PS_MR*
GPIO 4	LCD Backlight enable (BLEN)		EXPND 3	GPIO_DEBUG_SERVICE HEADER
GPIO 5	VID 0			
GPIO 6	VID 1			SMBUS
GPIO 7	3D STEREO		EXPND 4	GPU_PS_EN
GPIO 8	GPU Overtemp		EXPND 5	RSVD
GPIO 9	GPU thermal Alert		EXPND 6	PEX_RST
GPIO 10	FB Vref Control (not used sDDR3)		EXPND 7	RSVD
GPIO 11	FBVDD/Q VID (Reserved)			
GPIO 12	PWR_Level AC Detect			
GPIO 13	PS1 Vprgm Enable			
GPIO 14	HPD for IFP AB (not used)			
GPIO 15	HPD for IFP C (HDMI/DP)			
GPIO 16	Fan PWM control			
GPIO 17	HPD for IFP D (DP)			
GPIO 18	HPD for IFP E (DVI-I DL)			
GPIO 19	HPD for IFP F (not used)			
GPIO 20	NVGEM Debug GPIO13			
GPIO 21	NVGEM Debug GPIO14			

FOXCONN PCEG

Title: GPIOs, Thermal Sensor, I2C/GPIO Expanders

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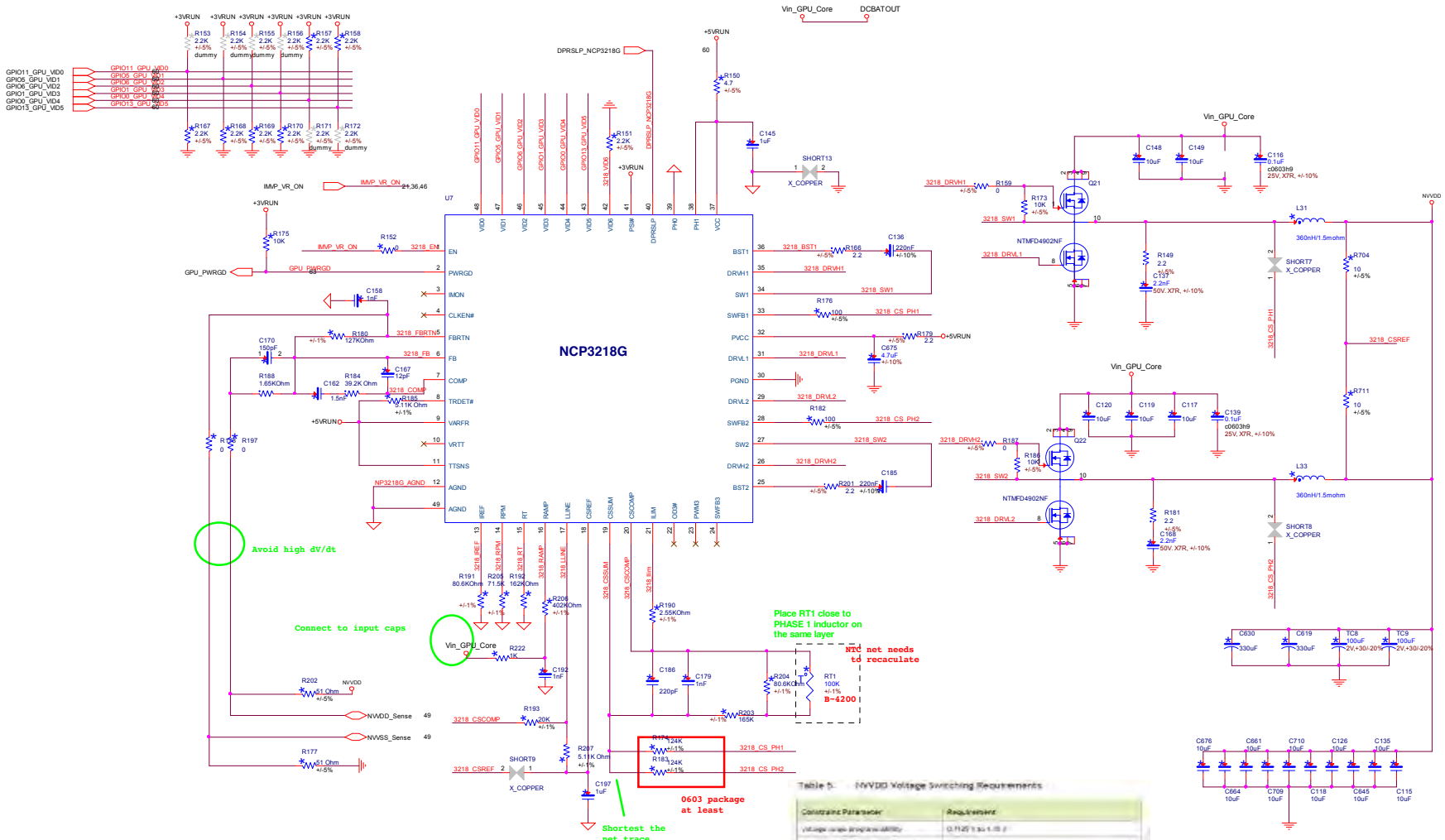
NVVDD (PS1)PHASE 1&2 DRIVERS/FBVDD (PS2)



GPU 28W
IccTDC: 22A
Icc_continuous:24.42A
IccMax: 33A
VID: 0.7125V-1.15V
DC Ripple:+/2.5%
Transient:
Vpp,150mV(20M), 200mV(1G)
Icc_Dyn_VID1: 21.2A, 9.9A/uS
R_LL: ? mOhm
H/W Boot VID: 0.9V
OCP: 50A

FOXCONN PCEG

Title	NVVDD (PS1)PHASE 1&2 DRIVERS/FBVDD (PS2)
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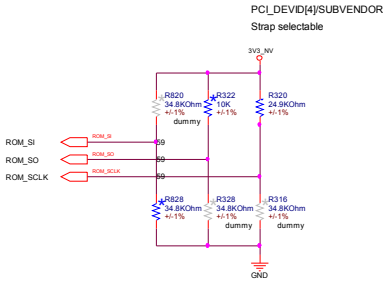
Straps



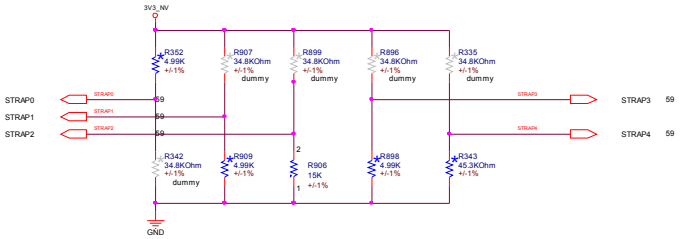


TABLE 1: STRAP DECODE ACCORDING TO TERMINATION RESISTANCE/VOLTAGE

TERMINATION RESISTANCE	TERMINATION VOLTAGE 3V3 [3:0]	TERMINATION VOLTAGE GND [3:0]
5K	1000 8	0000 0
10K	1001 9	0001 1
15K	1010 A	0010 2
20K	1011 B	0011 3
25K	1100 C	0100 4
30K	1101 D	0101 5
35K	1110 E	0110 6
45K	1111 F	0111 7

GF117/GK10X STRAP PIN MODE TABLE

PIN NAME	MULTI-LEVEL bit [3:0]	BINARY PRODUCTION	BINARY BRINGUP
STRAP0	USER[3:0]		3GIO_PADCFG_LUT_ADR0
STRAP1	3GIO_PADCFG_ADR[3:0]		3GIO_PADCFG_LUT_ADR1
STRAP2	PCI_DEVID[3:0]		3GIO_PADCFG_LUT_ADR2
STRAP3	SOR[3:0]_EXPOSED		3GIO_PADCFG_LUT_ADR3
STRAP4	RSV, RSV, PCIE_MAX_SPEED, DP_PLL_VDD33V		PCIE_MAX_SPEED
ROM_SCLK	DEVID[4], SUB_VENDOR, DEVID[5], PEX_PLL_EN_TERM		SMB_ALT_ADDR
ROM_SI	RAMCFG[3:0]		SUB_VENDOR
ROM_SO	FB[1]_BAR_SIZE, FB[0]_BS, SMB_ALT_ADDR, VGA_DEVICE		VGA_DEVICE

NOTE 2: See table 1 for the correct value/location of the strap resistor for the desired modes

NOTE 3: Bring-up SKU(s) have jumper configurable subvendor and DEVID_4 settings see the ROM_SCLK STRAP

FOXCONN PCEG

Title: Straps

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FBVDDQ (PS3) FBVDD (PS2) DRIVER(Optional/Debug)

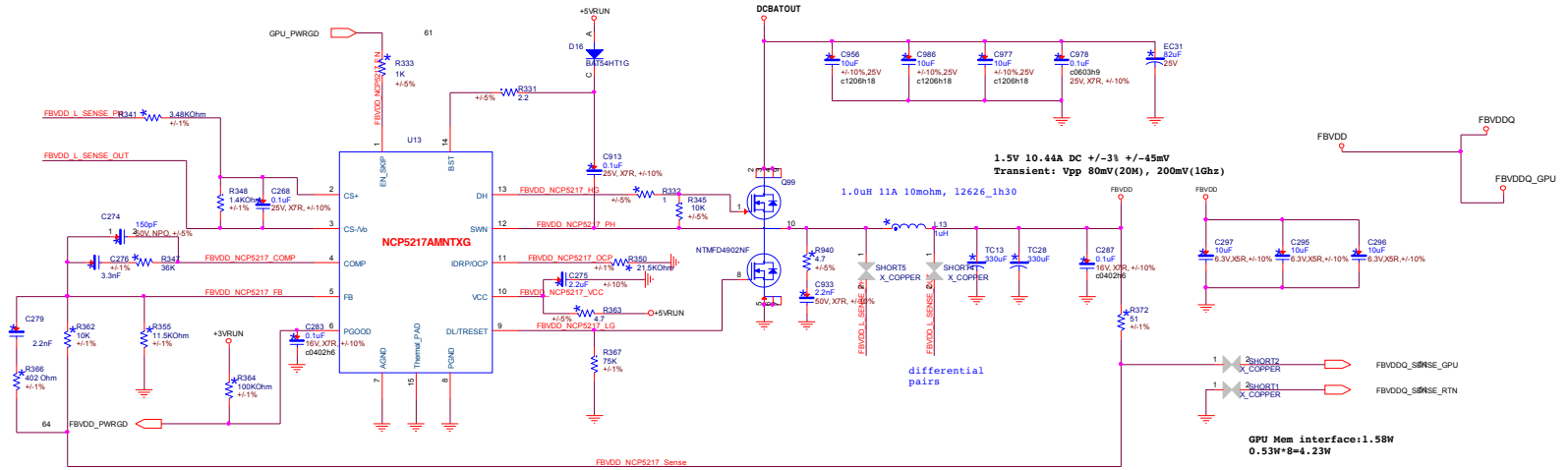

Table 23. Power Rail Requirements for DDR3 Frame Buffer Interface

Command Parameter	Requirement
FBVDDQ/FBVDD	1.5 V
DC tolerance	± 3%
AC tolerance	Transient noise tolerance: 80 mV pk-pk within 20 MHz BW, typ Frequency noise tolerance: 200 mV pk-pk within 1 GHz BW
GPU FBVREF	Internal VREF
Memory FBVREF	0.5 x FBVDDQ

Notes: Since the GPU internal Vref is used, the FBVref pin on the GPU can be left unconnected

FOXCONN PCEG

Title: FBVDDQ (PS3) FBVDD (PS2) DRIVER(Optional/Debug)

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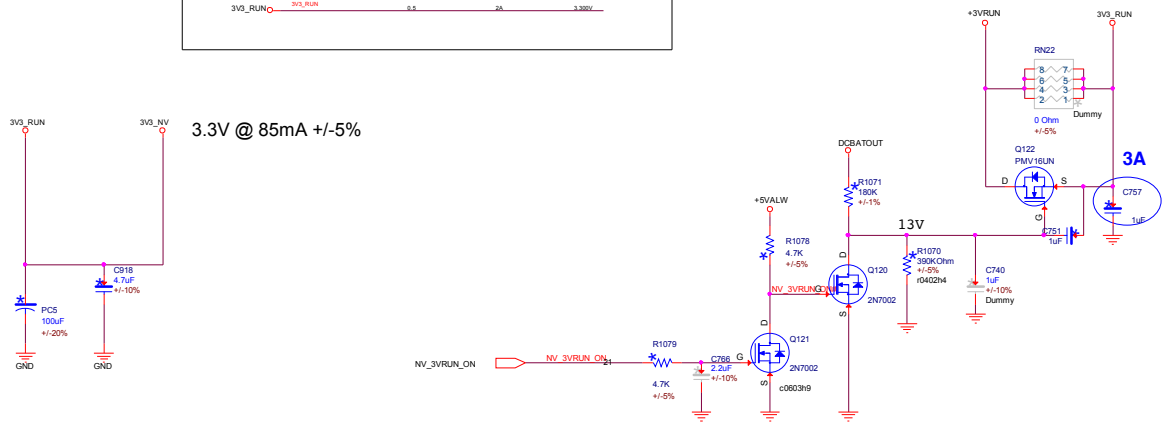
VBATT TO 3V3 SWITCHER

GLOBAL POWER CONSTRAINTS

NET	MIN_LINE_WIDTH	MAX_CURRENT	VOLTAGE
3V3_RUN	3V3_RUN	2A	3.30V

3.3V @ 85mA +/-5%

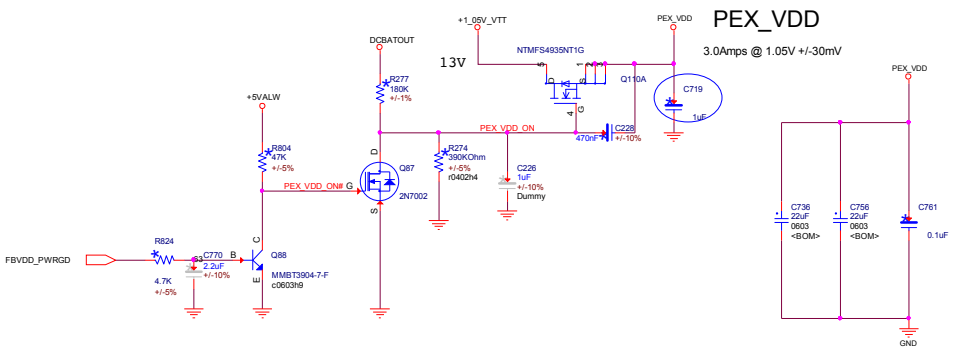


PEX_VDD Switcher (PS5) and Miscellaneous Voltage Rails

changed to AOS MOSFET

PEX_VDD

3.0Amps @ 1.05V +/-30mV



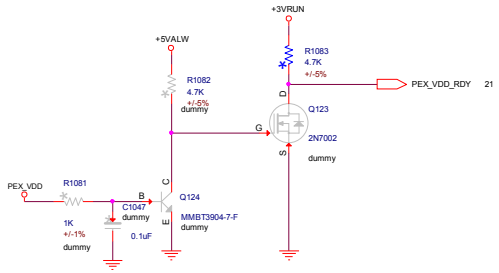


Table 27. GPU Frame Buffer PLL Power Rail Delivery

Power Rails	N13x Voltage Tolerance	Max Current Draw
FBx_PLL_AVDD + FB_DLL_AVDD	1.05 V ± 30 mV	66 mA per partition on FBx_PLLAVDD 35 mA on FB_DLL_AVDD

Note: The current values are estimated and are preliminary. Refer to the GPU-specific Electrical and Thermal Design Guidelines application note for further details.

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Title: 5V/3.3V (PS4) Dual Switcher and 1V8 LDO (PS7)

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EC GPIO Map

Pin	Pin definition	Pin Net name	I/O Status	Memo
2	PSI_L/FAN_TC4/CIRRX2/GP16	PCHHOT_PCH#		
3	SVD_O/PCIRSTIN#/CIRTX2/GP15	SUSPWRDNACK		
6	GP63	AMP_PD#		
10	FAN_TAC2/GP52	SYS_PWROK_EC		
11	FAN_CTL2/GP51	Thermal_Alert		
12	FAN_CTL3/GP37	Audio_Source_Sel		
13	FAN_TAC3/GP36	EXTSMI#		
14	GP35	PM_SLP_S5#		
15	GP34	FW_HW#		
16	SVC_I/GP33	PM_SLP_S4#		
17	SVD_I/GP32	PM_SLP_S3#		
18	CORE_TYPE//GP31	SUS_PWRGD		
19	ATXPG/VID0/GP30	RUN_PWRGD		
20	SIN2/GP27	UART_TX		
21	SOUT2/GP26	UART_RX		
22	DSR2#/GP25	IMVP_OK		
23	RTS2#/GP24	Log_LED_CTL		
24	SI/GP23	SI		
25	SCK/GP22	SCK		
26	DCD2#/GP21	GPIO8_GPU_OVT*	NC	
27	CTS2#/GP20	IMVP_VR_ON		
28	R12#/GP17	USB3.0_CTL3		
31	PCH_C1/SVC_0/GP14	PCH_C1		
32	PWROK1/GP13	ALW_ON		
33	PCIRTS1#/GP12	AC_PRESENT		
34	PCIRTS2#/GP11	ALW_PWRGD		
45	KRST#/GP62	H_RCIN#_D		
48	SO/GP50	SO		
56	GP76	OVT_EC#		
57	GP75	INT_Proximity		
58	GP74	PM_SLP_M#		
59	GP73	INT_OSD		
60	GP72	WAKE_SCI#		
61	GP71	WLAN_EN		
62	GP70	PWR_ON_GPIO		
63	GP87	Disassociate_EC		
64	GP86	PCIE_WAKE#_EC		
65	IO_SCI#/GP85	RUNTIME_SCI#		
66	D_TX0/SMBDAT2/IRTX/GP47	SMBDAT2		
70	D_RX0/SMBCLK2/GP46/IRRX	SMBCLK2		
72	PWRON#/GP44	PWRON#		
73	PME#/GP54	USB3.0_EN		
75	PANSHW#/GP43	PANSHW#		
76	PSON#/GP42	PSON#		
77	SUSC#/GP53	EN_BLUT		
78	PWROK2/GP41	PM_PCH_PWROK		
79	3VSBSW#/GP40	RSTJ_From_EC_L		
80	KDAT/GP61	KDAT		
81	KCLK/GP60	KCLK		
82	MDAT/GP57	MDAT		
83	MCLK/GP56	MCLK		
84	PCIRST3#/GP10	RSMRST#		
85	RSMRST#/CIRRX1/GP55	CIRRX		
100	GP92/ADC2	NC		
101	GP93/ADC3	NC		
102	GP94/ADC4	NC		
103	GP95/ADC5	NC		

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Title: EC GPIO MAP

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