Model Name:GA-EP43-UD3L REV 1.3

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03	BLOCK DIAGRAM
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11	GMCH-Eaglelake_PCI E, DMI
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SHEET	TITLE
28	AZALIA ALC888
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31	DISCRETE1 POWER,FAN CTRL
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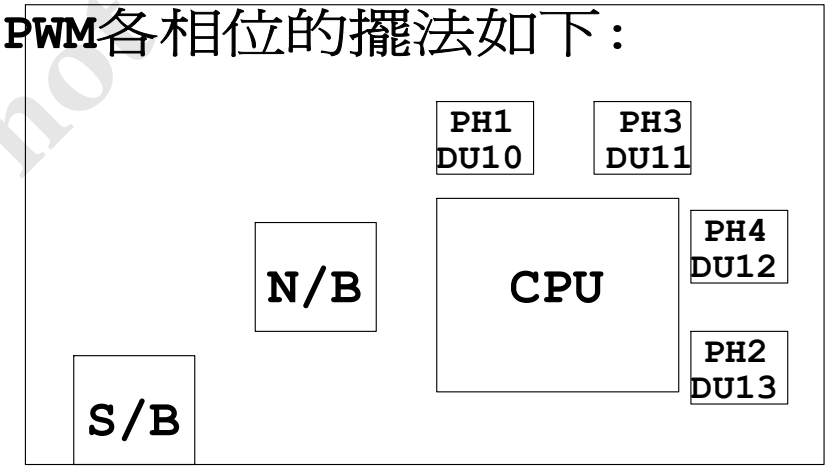
33	JMicron JMB368
34	LAN REALTEK RTL8111C
35	FRONT PANEL,FUSB,FDD
36	TPM I/F-1.2

PWM各相位的擺法如下：



Gigabyte Technology

Title: Cover Sheet

Size: Custom | Document Number: GA-EP43-UD3L | Rev: 1.3

Date: Monday, April 26, 2010 | Sheet 1 of 36

Model Name: GA-EP43-UD3L
Rev:.1.3

Component value change history

Data	Change Item	Reason
97/04/01 EBOM:01A	1. P43 CHIPSET E-BOM	
97/04/15 EBOM:02	1. 修改LED的POWER及阻值;DEL R484,DR78. ADD DR79,,R348	
	2. ADD DR80,R300 10-->49.9,C158,LBC43 0ohm-->100PF for EMI	
	3. del Q3,Q4,BC11,BC9,R42,R15,PCI_BT1,PCI_BT2,R166,R168	
97/04/28 EBOM:10A	1. DDR2 VOLTAGE 1.83 --> 1.9V --> 2.0V --> 2.1V .....-->2.5V	
97/05/09 PBOM:10B	1. DR59,DR60 14K---->549ohm,del DR69	
	2. ADD U9(uP6262),R436,BC133 FOR CPU 超頻	
97/05/21 PBOM:10C	1.ICH,MCH PCI-E ,JM368的RX,TX串電容BOM 0.1U/Y5V-->0.1U/X7R,RTC RTCVDD -->X7R	
	2.ADD U6 FOR DDR TURN ON 2.1V ISSUE	
97/06/4 PBOM:10D	1.DEL Q107,R620,ADD R621 2.Q49(BAT54C) 限用 DII	
97/06/18 PBOM:10E	1.ADD MB_ID R283,DEL R282,Q87,Q91,R452,R498,R499,R500 FOR VTT_GMCH 1.2V	
	2.C197 0.1U/Y5V--->X7R 3.R300 49.9--->100 ohm ,C158 Y5V--->X7R for USB	
	4.DC20 0.01u--->1nf FOR CPU PSI ISSUE	
97/08/07 EBOM:20A	1.CPU 改爲SMART FAN 2.L4,L7 CHOKE Footprint Change "CHOKE1U2-20A-1PQN"	
	3.獨立南橋1.1V 的電壓 4. ADD GPIO37 FOR LOAD LINE CALIBRATION	
	5.J368 改爲1.8V;R209=100 OHM, ADD R640 FOR MB_ID2	
97/08/08 EBOM:30A	1.J368 改爲1.8V;47--->44.2 2.TO252---改爲POWER PACK	
97/10/01 PBOM:10A	FOR EP45-UD3L-1.0	
	1.R183 18K-->9.09K;R184 9.76K--->4.3K 2.DR56 1.74K-->1.87K;DR81 1K--->590 OHM	
	3.DR38 487--->549 ohm 4.R369 2.26K--->1.5K;R378 13.7K--->15.8K	
	4.NB,SB CHANGE HEAT SINK for UD series; PCIEX1 SLOT改爲白色	
	5.RQ3 由BJT改爲 BAT54A FOR -HDLED ISSUE	
97/11/17 EBOM:10A	FOR EP43-UD3L-1.0 1.P43 CHIP,HEAT SINK,UPI	
97/12/05 PBOM:10B	1.P-BOM,修改HEATSINK,調整部份阻值	
98/02/24 PBOM:10C	1.100UF 統一料號	
98/03/26 PBOM:11A	1.僅變更NB,SB heatshink料號金色改灰色	
98/05/13 PBOM:11B	1.Backup bios R56 pull-high 1k--->330 ohm; 移除SST BIOS	
98/11/06 EBOM:12A	1.FOR GA-EP43-UD3L-1.2 98/12/01 PBOM:12A 1.FOR GA-EP43-UD3L-1.2,轉P-BOM ADD PACKAGE	
99/04/16 PBOM:13A	1.F4,F5 1.6A--->3.5A 2.R348,R86,R87,R336,R337,R338 1K--->8.2K FOR PHASE LED	

Circuit or PCB layout change for next version

DATE	Change Item	Reason
97/04/01 PCB:0.1	1.P43-DS3L	
97/04/23 PCB:1.0	1. CE3位置請移至EC24左邊	
	2. 增加 upi6262 VCC Power (R620,R621,Q107)	
	3. 增加R622,R623 FOR DDR18V_OV3	
97/07/23 PCB:2.0	1.由1.0 修改,直接改成2.0	
	2.PCIEX16 和PCIEX1_2對調位置	
	3. DDR2_1~DDR2_4往左移,盡量讓MCH的位置在DDR SLOT中間	
	4.ADD CPU SMART FAN CONTROL	
97/07/23 PCB:3.0	1.由2.0 修改	
	2. cpu Vcore MOS TO252改爲POWER PACK	
97/09/16 PCB:1.0	1.由3.0 修改,改文字面 EP45-UD3L ,ULTRA DURABLE 3,NB /SB 框內文字修改	
97/11/06 PCB:1.0	1.由EP45-UD3L改文字面成EP43-UD3L	
	2.DEL ICH CORE 1.1線路,NET DDR18V_OV2與LAN_DSM互換FOR DDR超壓ISSUE	
	3.UPDATE LL1 ,LGA775 FOOTPRINT	
98/03/27 PCB:1.1	1.TO CHANGE PCB VERSION FOR 1.1	
98/11/04 PCB:1.2	1.add EUP function,audio co-lay 892	
99/04/15 PCB:1.3	1.FOR USB 3倍力,修改ERP READY文字面	

Gigabyte Technology

Title: BOM & PCB MODIFY HISTORY

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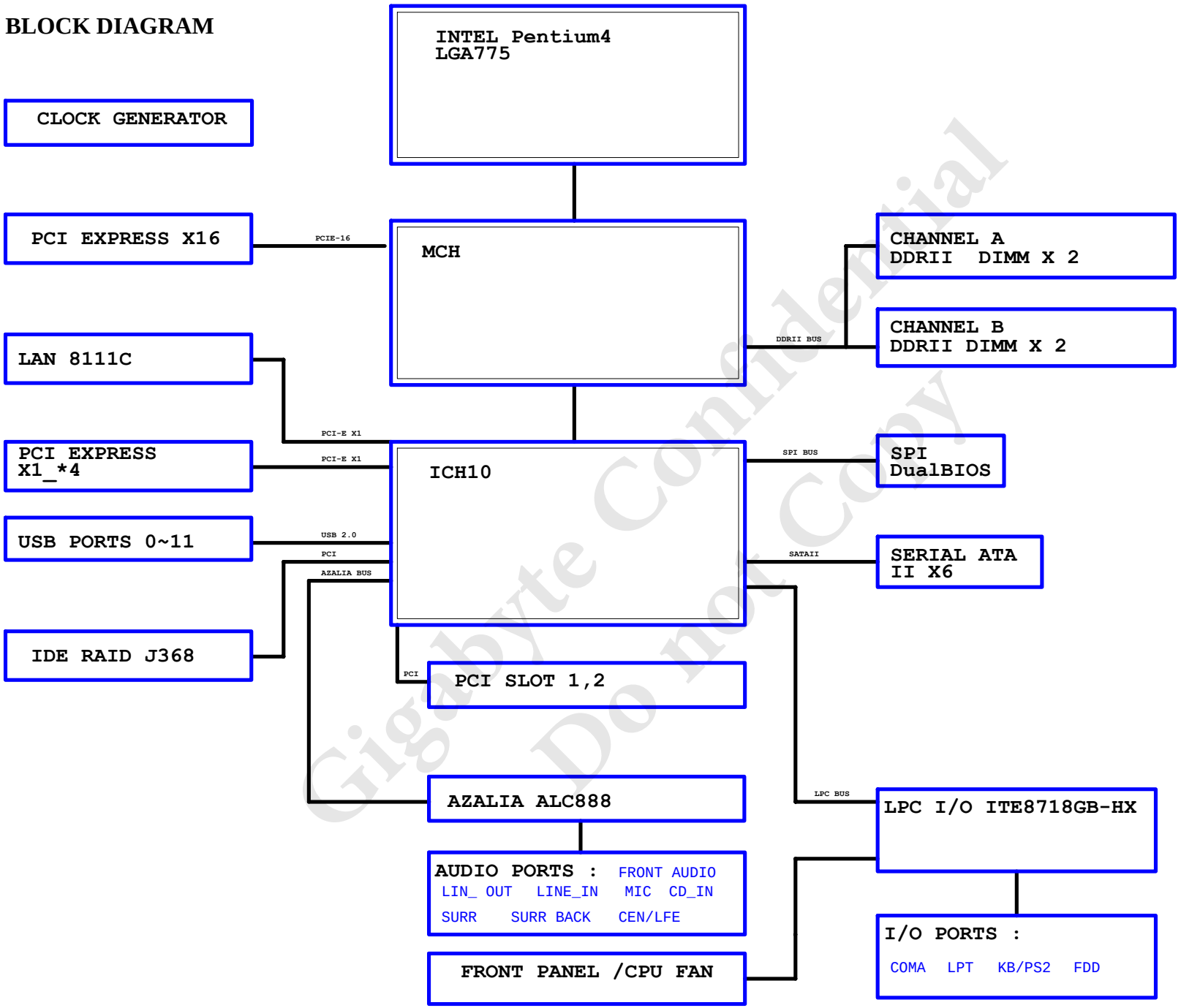
BLOCK DIAGRAM



Gigabyte Technology

Title	BLOCK DIAGRAM	
Size: Custom	Document Number: GA-EP43-UD3L	Rev: 1.3
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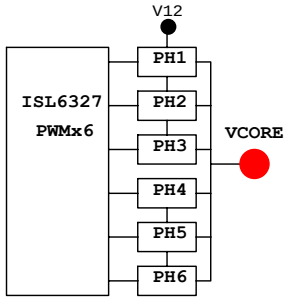
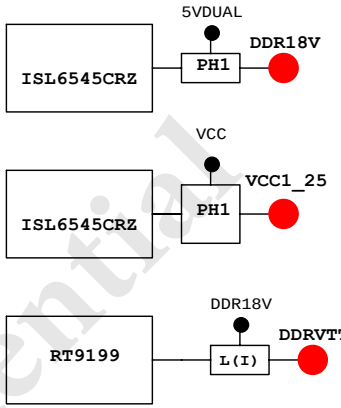
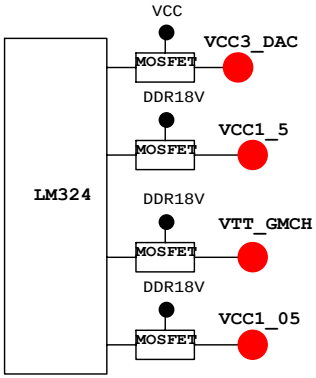
ICH8 GPIO LIST TABLE

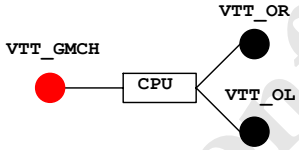
PIN NAME	PWR WELL	AFTER/ PLTRST	USAGE	NOTE
GP0	MAIN	IN	-ACZ_DET	P/U 8.2K VCC3
GP1/TACH1	MAIN	IN	ICH_FAN_TACH1	P/U 8.2K VCC3
GP2/PIRQE#	MAIN	IN	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN	IN	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN	IN	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN	IN	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN	IN	ICH_FAN_TACH2	P/U 8.2K VCC3
GP7/TACH3	MAIN	IN	ICH_FAN_TACH3	P/U 8.2K VCC3
GP8	STBY	IN	GPIO8(DUALBIOS_INPUT)	P/U 8.2K 3VDUAL
GP9	STBY	OUT	WOL_ONLY	P/D 100K GND
GP10	STBY	IN	CLGPIO1	P/U 8.2K 3VDUAL
GP11/SMBALERT#	STBY	OUT	-SMBALRT	P/U 8.2K 3VDUAL
GP12	STBY	IN	MB_ID0	P/U 8.2K 3VDUAL
GP13	STBY	IN	-LPCPME	P/U 8.2K 3VDUAL
GP14	STBY	IN	CLGPIO2	P/U 8.2K 3VDUAL
GP15	STBY	OUT	LAN_DISABLE(STP_PCI-)	N/A
GP16	MAIN	OUT/LOW	RESET	N/A
GP17/TACH0	MAIN	IN	ICH_FAN_TACH0	P/U 8.2K VCC3
GP18	MAIN	OUT	MB_ID1	P/U 8.2K VCC3
GP19	MAIN	IN	SATA1GP	P/U 8.2K VCC3
GP20	MAIN	OUT	-SPI_WP0	P/U 1K 3VCL
GP21	MAIN	IN	SATA0GP	P/U 8.2K VCC3
GP22	MAIN	IN	SCLOCK	P/U 8.2K VCC3
GP23	MAIN	OUT	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	OUT	CLGPIO0	P/U 8.2K 3VDUAL
GP25	STBY	IN	MB_ID2(STP_CPU-)	P/U 8.2K 3VDUAL
GP26/S4_STATE#	STBY	OUT	S4_STATE#	P/U 8.2K 3VDUAL
GP27	STBY	OUT/LOW	GPIO27(EL_STATE0)	P/U 8.2K 3VDUAL
GP28	STBY	OUT/LOW	PWR_LED(EL_STATE1)	N/A
GP29/OC5#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP30/OC6#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP31/OC7#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP32	MAIN	OUT	DUAL_BIOS	P/U 100K+1M VCC3
GP33	MAIN	OUT	DUAL_BIOS	P/U 8.2K VCC3
GP34	MAIN	OUT/LOW	GPIO34/SMB_RST	N/A
GP35	MAIN	OUT	SATACLKREQ#	N/A
GP36	MAIN	IN	SATA2GP	P/U 8.2K VCC3
GP37	MAIN	IN	SATA3GP	P/U 8.2K VCC3
GP38	MAIN	IN	SLOAD	P/U 8.2K VCC3
GP39	MAIN	IN	GPIO39	P/D 8.2K GND
GP48	MAIN	IN	GPIO48	P/U 8.2K VCC3
GP49	MAIN	IN	CPUPWROK	P/U 100 VTT_OL

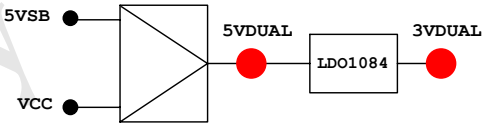
VCORE:6 PHASE PWM--ISL6327CRZ











Gigabyte Technology		
Title: TABLE LIST		
Size: B	Document Number: GA-EP43-UD3L	Rev: 1.3
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0.667 X VTT FOR LGA775 PIN H2/F2

0.635 X VTT FOR LGA775 PIN H1/G10

HA/REQ:50歐姆+-15% [4/11]

ADSTB:50歐姆+-15% [4/14]

SP-CAP X 3PCS

Impedance=50 +- 15% for 4 -layer

CPU GTLREF RATIO

GTLREF_UV0	GTLREF_UV1	Ratio Set
HIGH	HIGH	0.67
LOW	HIGH	0.65
HIGH	LOW	0.63
LOW	LOW	0.615

Gigabyte Technology

Title: P4_LGA775-A

Size: Custom | Document Number: GA-EP43-UD3L | Rev: 1.3

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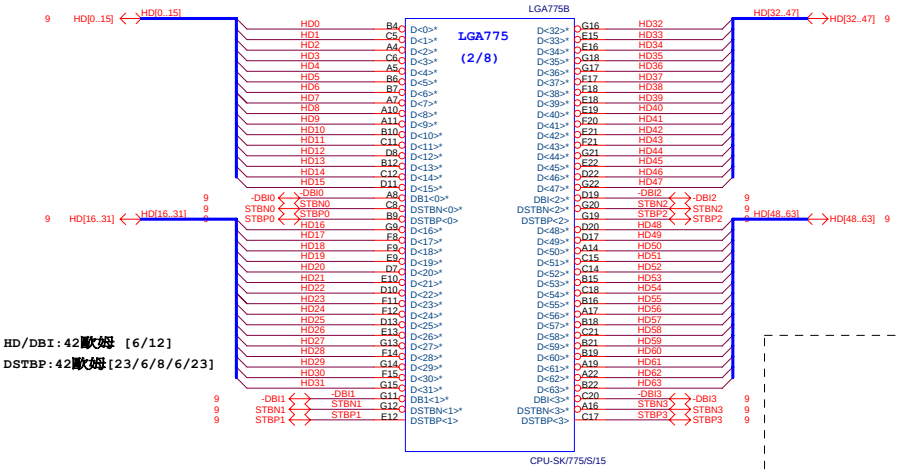
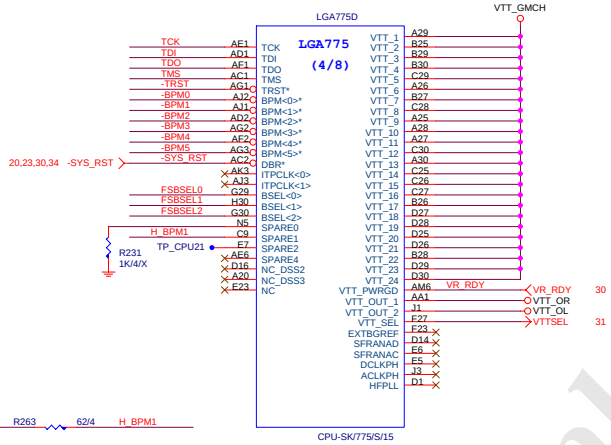
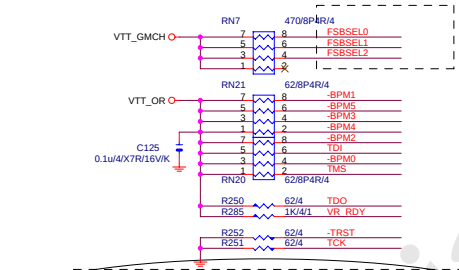
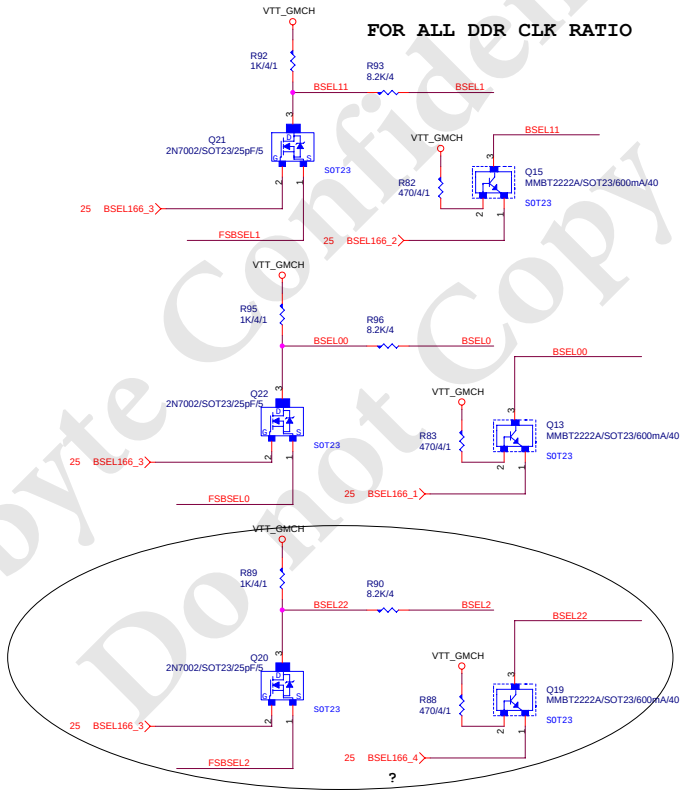


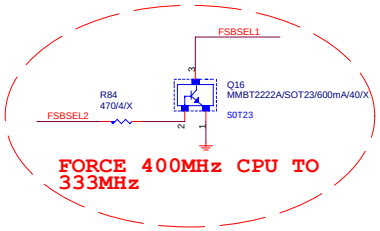
HD/DBI:42歐姆 [6/12]

DSTBP:42歐姆[23/6/8/6/23]









4X Length Guidelines for Quad core processors
Signal Name ATX Layer Pin to Pin
D[15:0]#, DBI0#, DSTBP0#, DSTBN0# Layer 1 2.2" - 2.7"
D[31:16]#, DBI1#, DSTBP1#, DSTBN1# Layer 4 3.0" - 3.5
D[47:32]#, DBI2#, DSTBP2#, DSTBN2# Layer 4 3.6" - 4.3
D[63:48]#, DBI3#, DSTBP3#, DSTBN3# Layer 1 2.4" - 3.0

	FSA	FSB	FSC		
	FSBSEL0	FSBSEL1	FSBSEL2	Clock	
?	1	0	1	100MHz	
?	1	0	0	133MHz	3/4
G33	0	1	0	200MHz	2/2.66/3.33/4+
G33	0	0	0	266MHz	2/2.5/3/4~
G33	0	0	1	333MHz	2/2.4/3.2/4#
	0	1	1	400MHz	

400/533
400/533/667/800
533/667/800/1066
667/800/1066/1333

Gigabyte Technology		
Title	P4_LGA775-B,D	
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Note:

VCCA & VCOREPLL define doesn't same as old P4 design kit

Trace width doesn't less than 12 Mil

As close as possible to CPU socket

VTT_GMCH L2 10UH/8/S/[10LI2-12100A-13R_10LI2-12100A-02R]

C22 1u/6/X7R/16V/K

R102 MASK-30 0/6/SHT-30/MASK/X

VCCA

VSSA

C21 1u/6/Y5V/10V/Z/X

VCOREPLL

L1 10UH/8/S/[10LI2-12100A-13R_10LI2-12100A-02R]

LGA775C

LGA775 (3/8)

CPU-SK/775/S/15

-STPCLK C98 33p/4/NPO/50V/J/X

VID[0..7] 30

VRD_SEL 30 CPUCLK 23 -CPUCLK 23 -SKTOCC 20

CPU_TEMP 25,27 THERMDC 25 R173 R174 0/4/SHT/X

C69 1n/4/X7R/50V/K/X C66 1n/4/X7R/50V/K

VCC_SENSE 26 VSS_SENSE 26 VCORE

TP_CPU11 TP_CPU14 TP_CPU16 R262 62/4

PECI 21,25

-SMI 21 -A20M 21 -FERR 21 INTR 21 NMI 21 -IGNNE 21 -STPCLK 21

H_DPSLP_N 20 TESTHI_M PM_SLP_N -FORCEPR CPUPWROK -PROCHOT -THRMTRIP COMP0 COMP1 COMP2 COMP3 COMP4 PM_DPRSTP 12,20 COMP6 R217 0/4/SHT/X -PSI COMP7 COMP8 H_BPM0 TESTHI_M R100 1K/4/X TP_CPU10 GTLREF2 GTLREF3 MSID1 R245 MSID0 R246 R247 62/4 62/4 62/4/X TP_CPU13 TP_CPU15

Pop to disable old Prescott CPU

COMP4~7 可以不上

Place outside of CPU socket

VTT_OL R222 49.9/4/1/X PM_DPRSTP; R213 49.9/4/1/X COMP4; R211 49.9/4/1 COMP2; R215 49.9/4/1 COMP3; R130 49.9/4/1 COMP0; R216 49.9/4/1 COMP1; C97 0.1u/4/X7R/16V/K

VTT_OR R218 1K/4/1 COMP6; R223 49.9/4/1/X COMP7; R128 24.9/4/1 COMP8; C100 0.1u/4/X7R/16V/K

VTT_GMCH R99 62/4 TESTHI2_7; R240 62/4 -THRMTRIP; R214 62/4 -FERR; R98 62/4 TESTHI0; C13 0.1u/4/X7R/16V/K

VTT_OL R210 51/4/X PM_SLP_N; R243 62/4 TESTHI1; R242 51/4/X H_DPSLP_N; R241 100/4/1/X CPUPWROK; C99 1n/4/X7R/50V/K/X; R212 62/4 H_BPM0; R244 62/4 TESTHI_M

VTT_OR RN22 680/8P4R/4 VID3 VID2 VID5 VID4; RN23 680/8P4R/4 VID6 VID7 VID1 VID0 30; R265 1K/4/1 VRD_SEL; R248 130/4/1 -FORCEPR; R249 130/4/1 -PROCHOT

VTT_OR R259 49.9/4/1/X GTLREF2 GTLREF2 5; R258 100/4/1/X C102 1u/6/Y5V/10V/Z

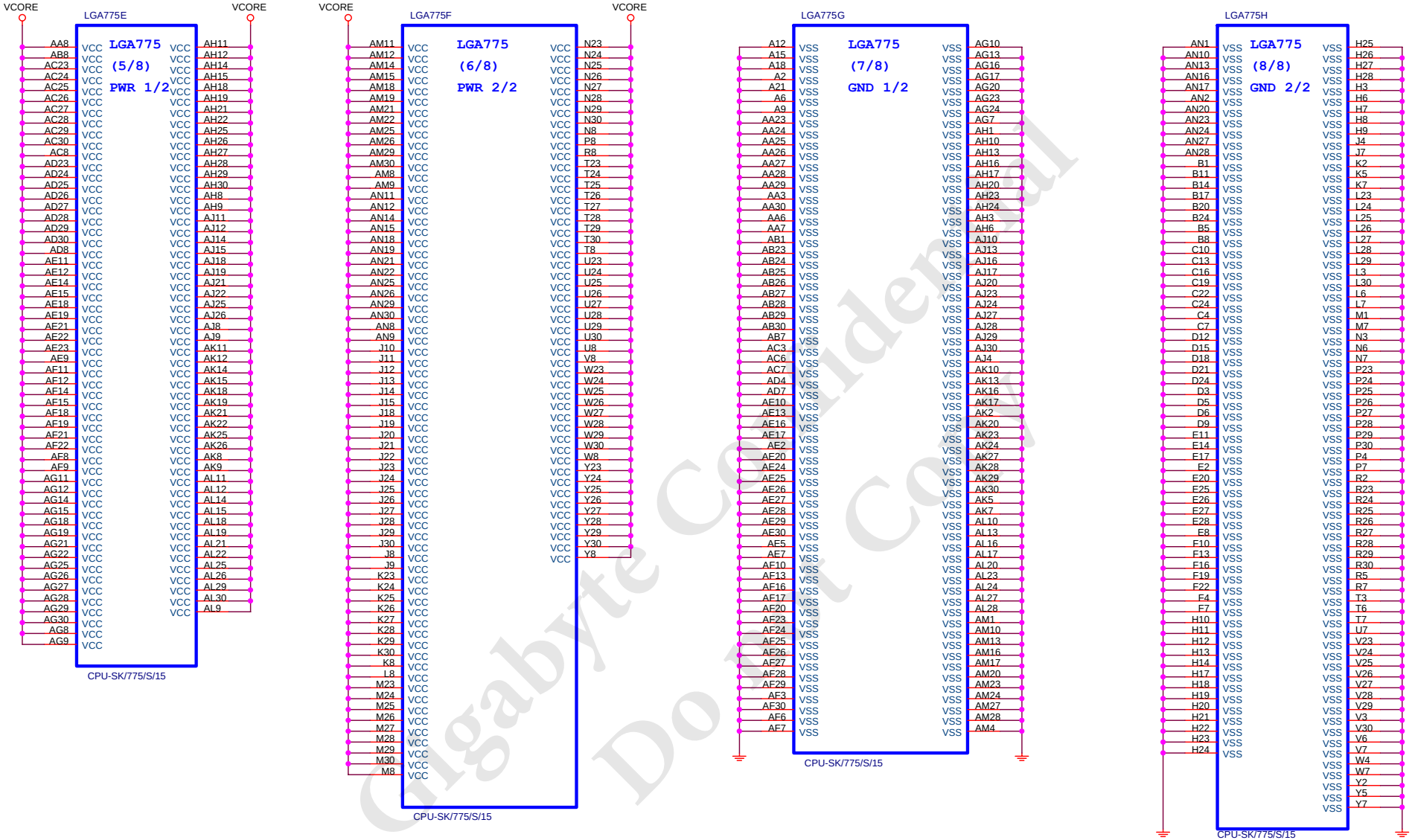
VTT_OR R268 49.9/4/1/X GTLREF3 GTLREF3 5; R267 100/4/1/X C123 1u/6/Y5V/10V/Z

FB1 MASK-50

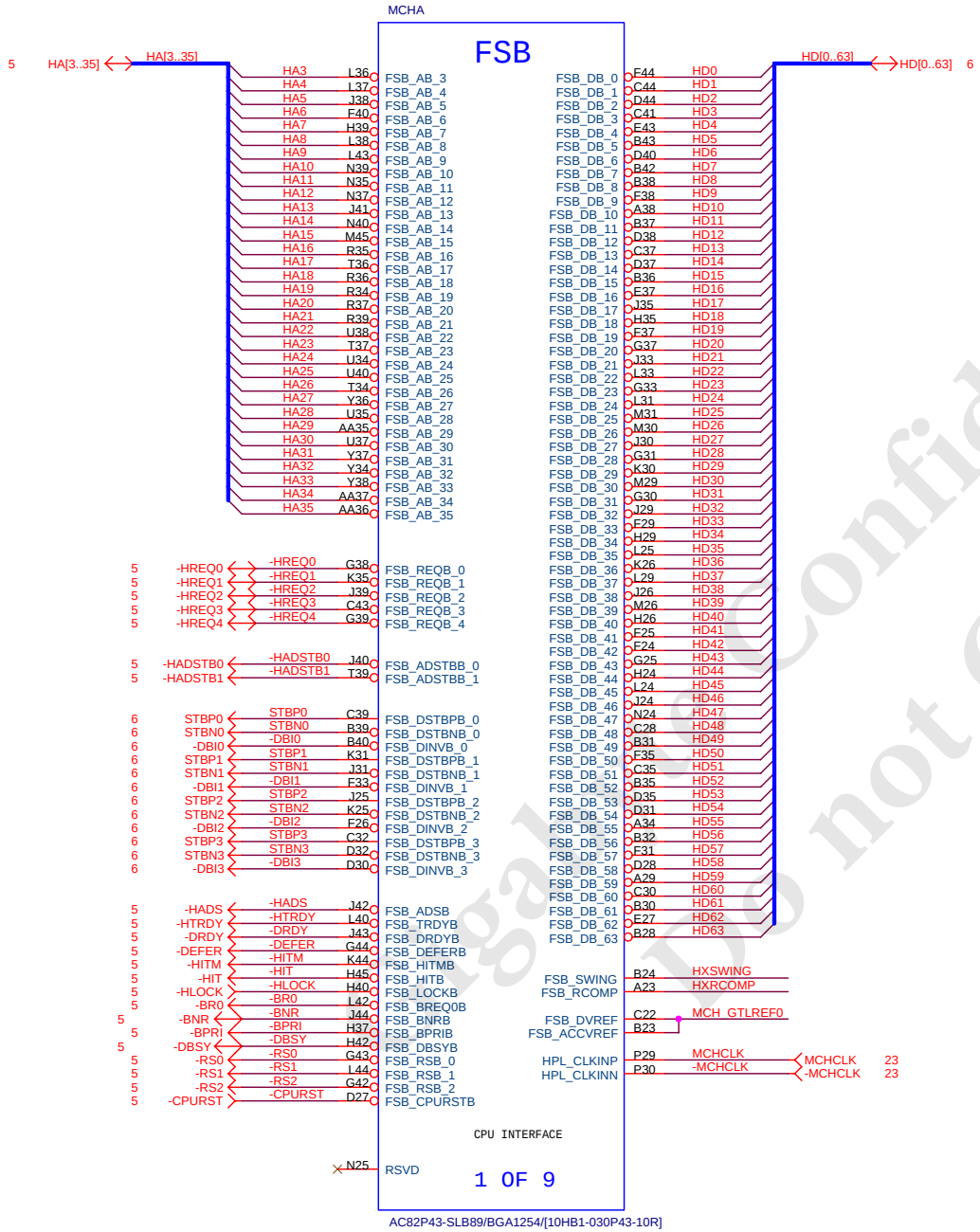
VCC_PLL1 VCC_PLL VCC_PLL 0/8/SHT-50/MASK/X C15 1u/6/X7R/16V/K C16 0.1u/4/X7R/16V/K

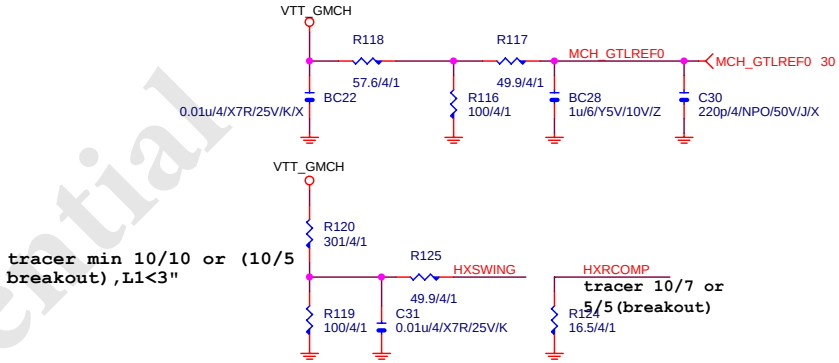
PECI:Platform Environment Control Interface

Gigabyte Technology		
Title: P4_LGA775-C		
Size: B	Document Number: GA-EP43-UD3L	Rev: 1.3
Date: Monday, April 26, 2010	Sheet 7 of 36	



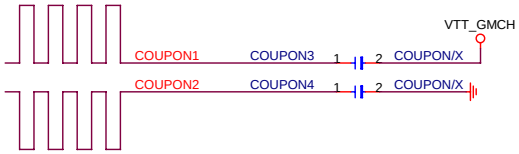
Gigabyte Technology		
Title: P4_LGA775-E,F,G,H		
Size: B	Document Number: GA-EP43-UD3L	Rev: 1.3
Date: Monday, April 26, 2010	Sheet 8 of 36	



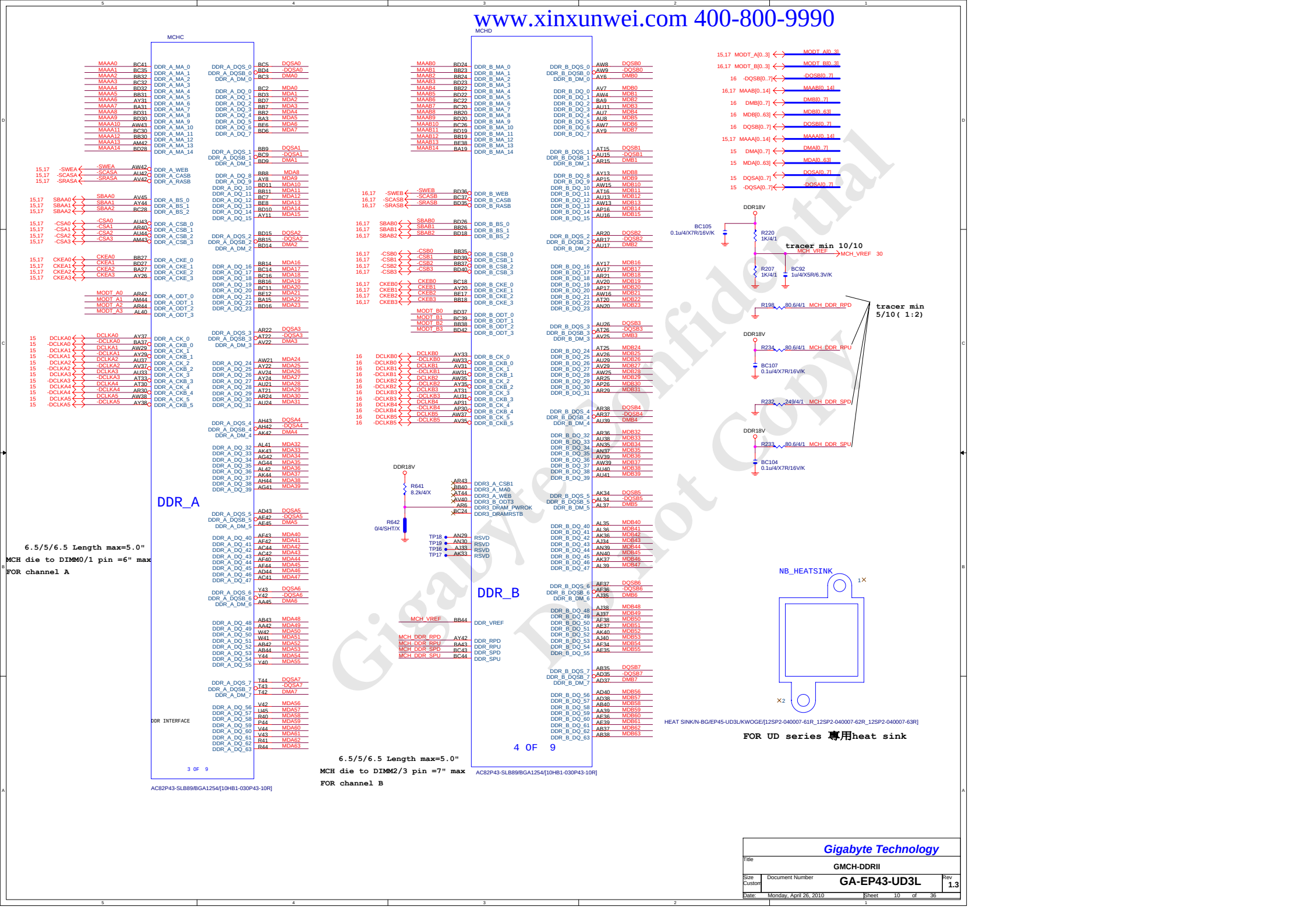


tracer min 10/10 or (10/5 breakout),L1<3"

tracer 10/7 or 5/5(breakout)



Gigabyte Technology			
Title: GMCH-HOST			
Size: Custom	Document Number: GA-EP43-UD3L		Rev: 1.3
Date: Monday, April 26, 2010		Sheet 9 of 36	



Gigabyte Technology		
Title	GMCH-DDRII	
Size: Custom	Document Number: GA-EP43-UD3L	Rev: 1.3
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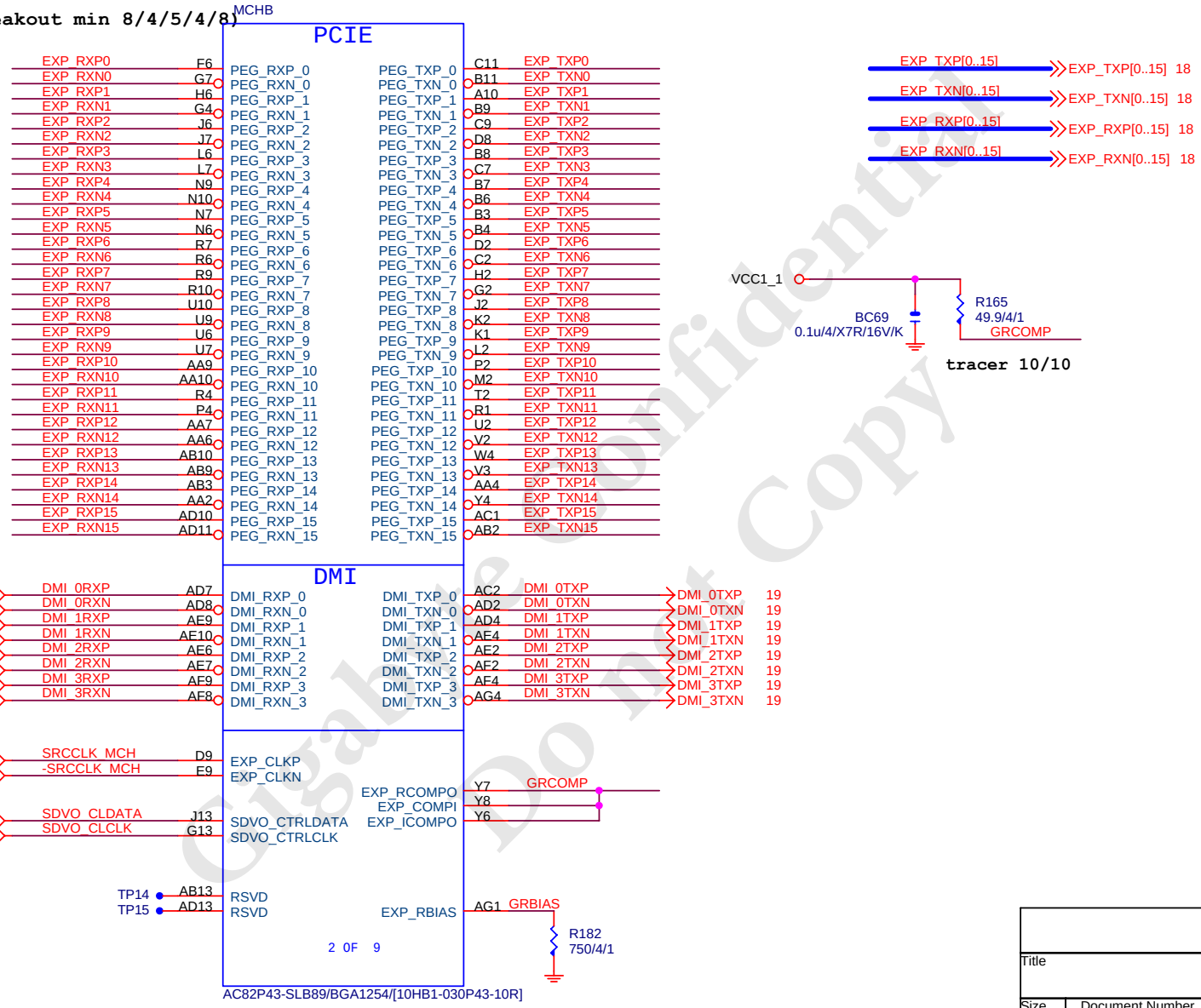
PCIEX16:16/5/5/5/5/16(breakout min 8/4/5/4/8)

Impedance=85 +- 17.5%

DMI:12/4/8/4/12

Impedance=95 +- 17.5%



Gigabyte Technology			
Title: GMCH-PCI E & DMI			
Size: Custom	Document Number: GA-EP43-UD3L		Rev: 1.3
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EXP_SM
0:SDVO OR PCIE
1:BOTH SDVO AND PCIE

EXP_SLR:
0:BTX PCIE are reversed
1:ATX PCIE normal

ITPM:
0:ENABLE ITPM
1:DISABLE ITPM

CEN:
0:DISABLE TLS
1:ENABLE TLS

CL_VREF:4/10
0.349V

MCHE

VGA

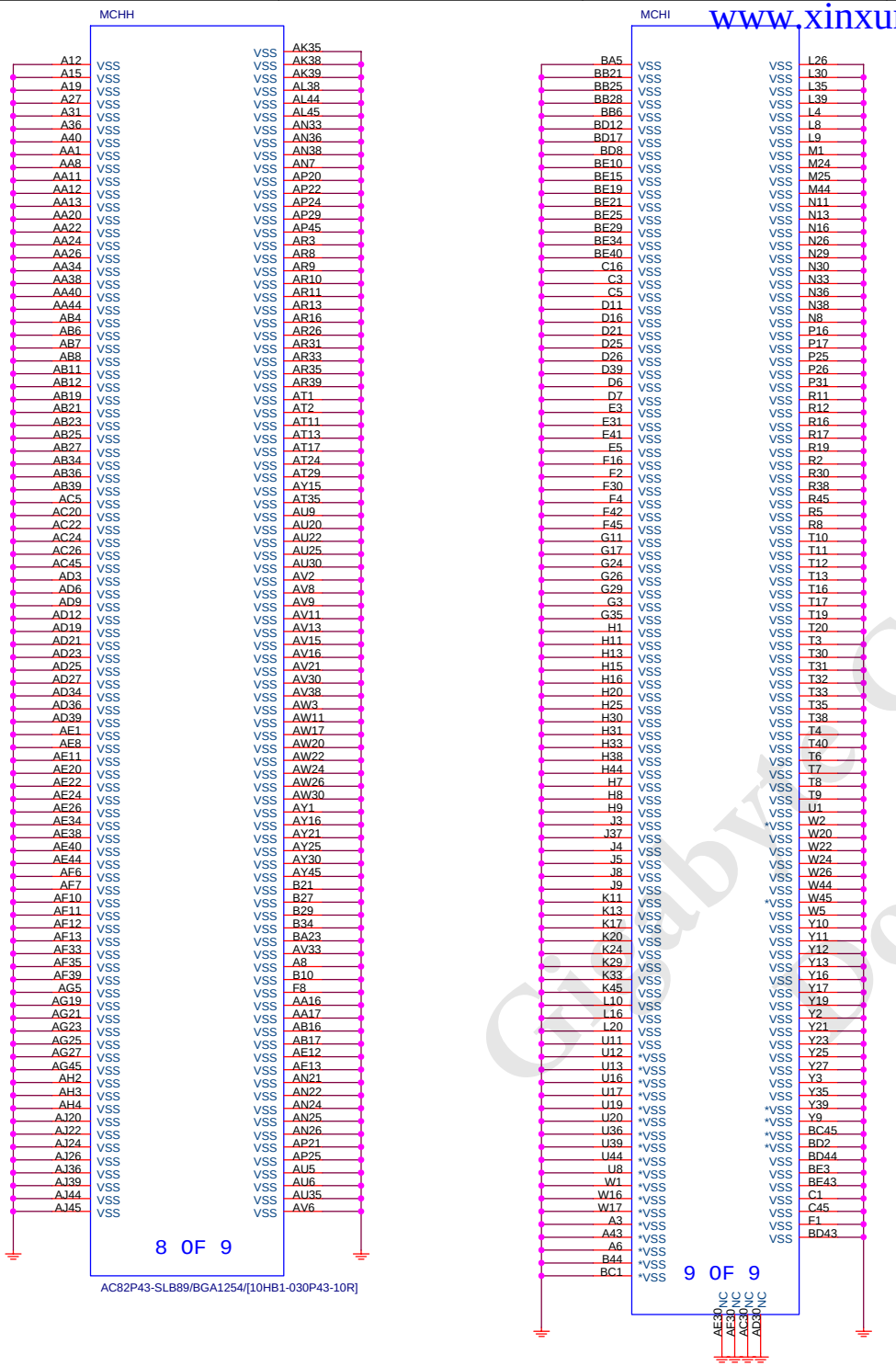
MISC

5 OF 9

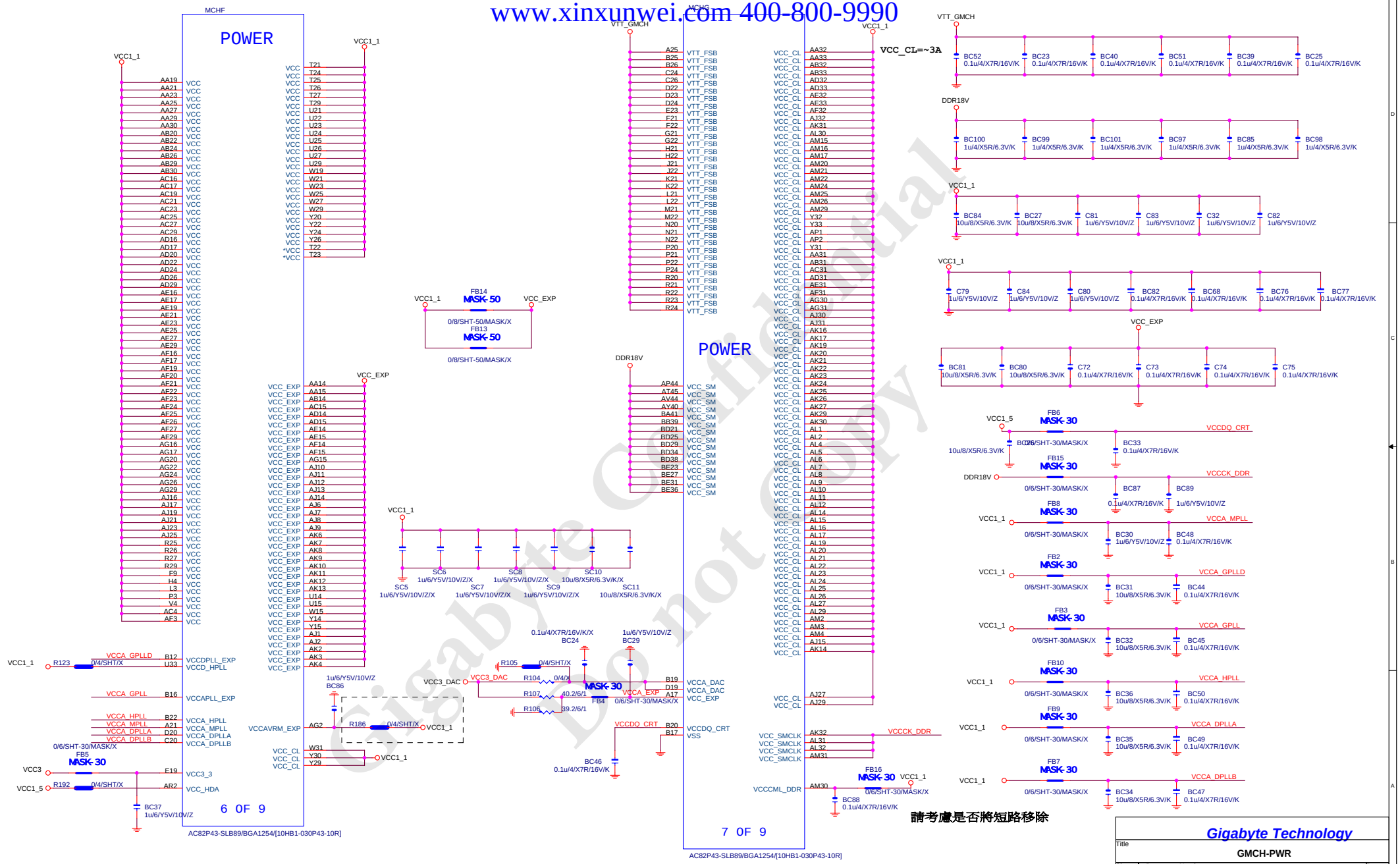
AC82P43-SLB89/BGA1254/[10HB1-030P43-10R]

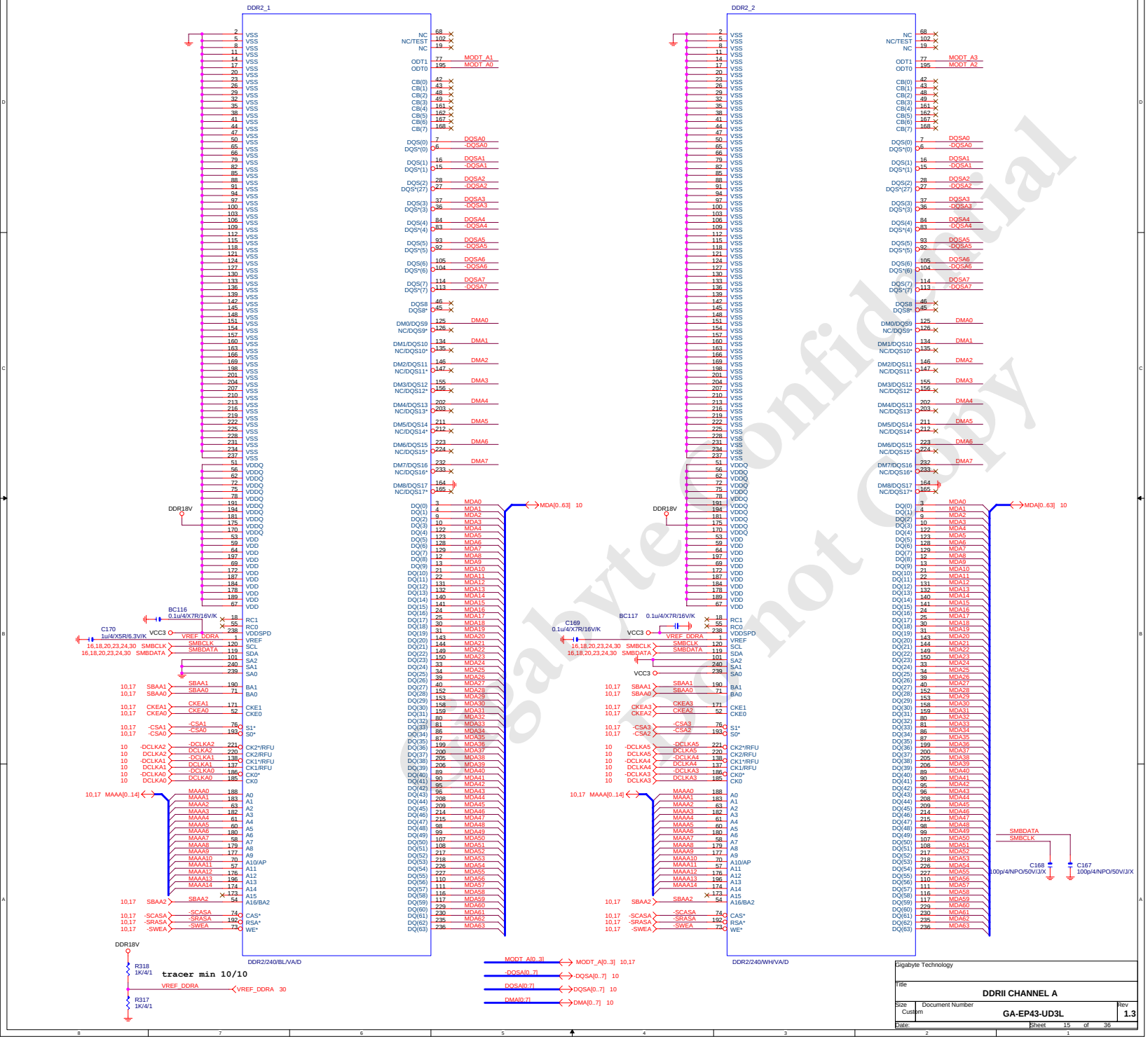
BW+ICH8 不要上(SAMPLE)
BW+ICH7 要上

Gigabyte Technology			
Title: GMCH-INTERNAL VGA			
Size: Custom	Document Number: GA-EP43-UD3L		Rev: 1.3
Date: Monday, April 26, 2010	Sheet 12 of 36		

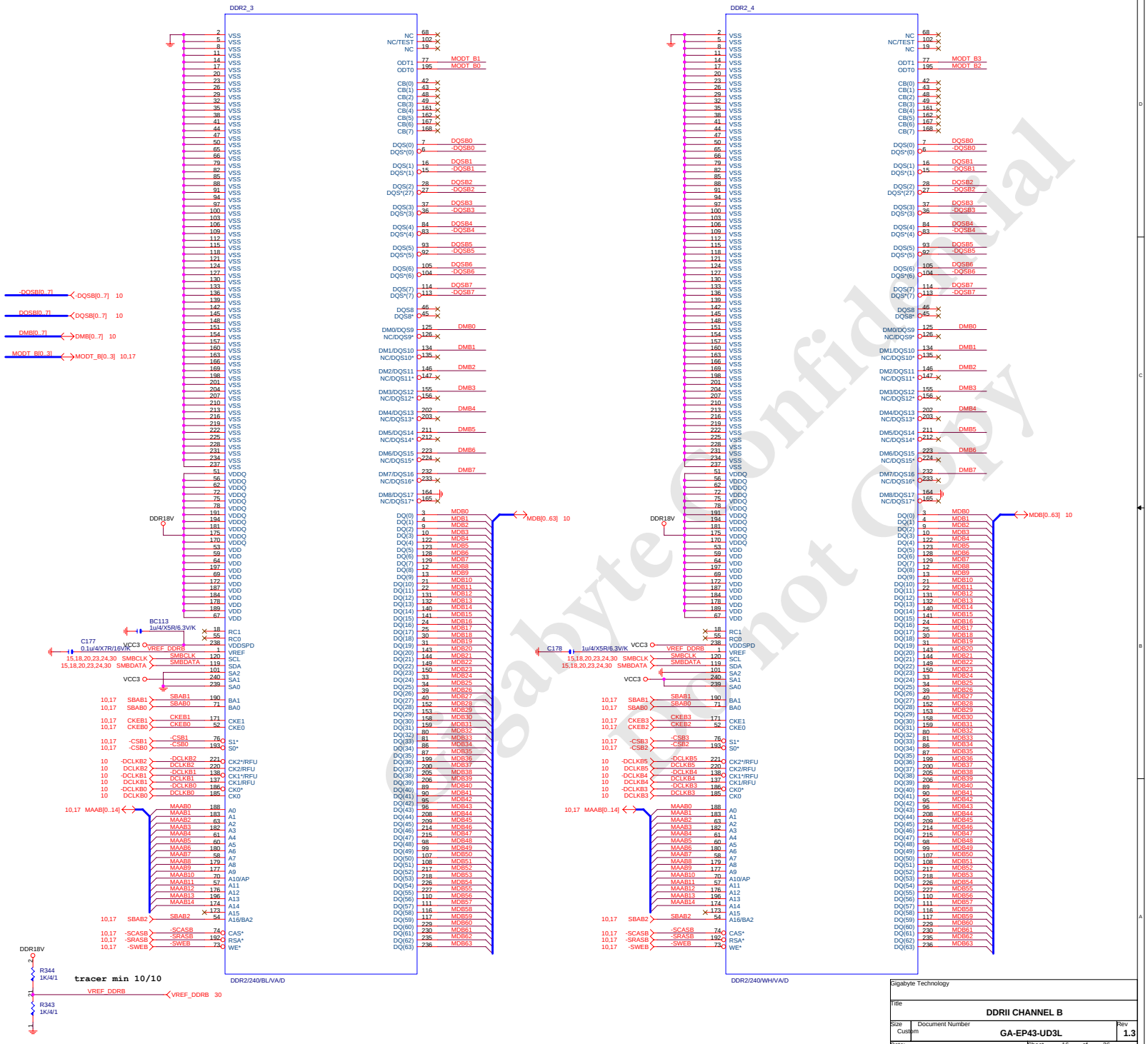


Gigabyte Technology		
Title: GMCH-GND		
Size: Custom	Document Number: GA-EP43-UD3L	Rev: 1.3
Date: Monday, April 26, 2010	Sheet 13 of 36	





Gigabyte Technology		
Title: DDRII CHANNEL A		
Size: Custom	Document Number: GA-EP43-UD3L	Rev: 1.3
Date:	Sheet 15 of 36	



Gigabyte Technology

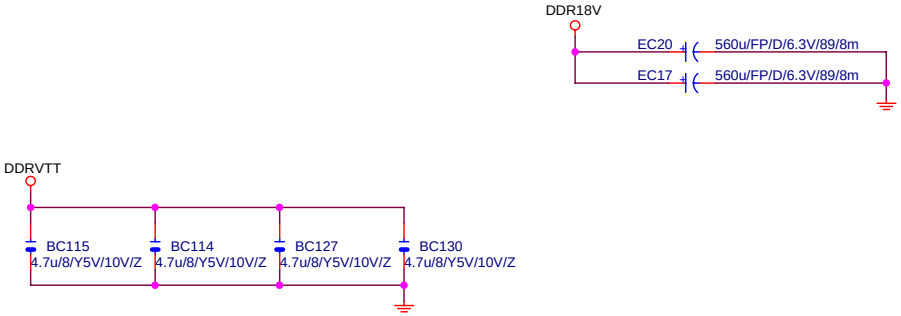
Title: **DDRII CHANNEL B**

Size	Document Number	Rev
Custom	GA-EP43-UD3L	1.3

Date: Sheet 16 of 36

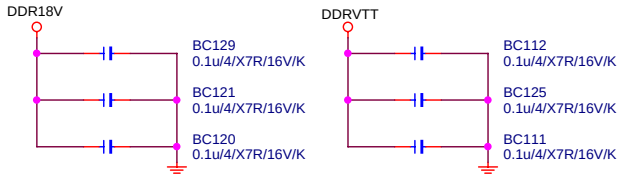
DDR TERMINATION CHANNEL A

DDRVTT Decouple



DDR18V Decouple

DDRVTT Decouple



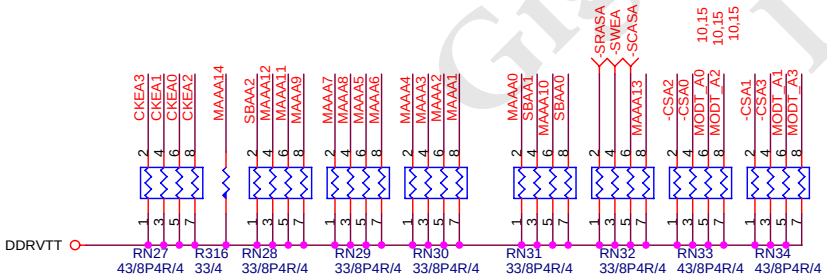
SBAA[0..2] SBAA[0..2] 10,15

-CSA[0..3] -CSA[0..3] 10,15

CKEA[0..3] CKEA[0..3] 10,15

MAAA[0..14] MAAA[0..14] 10,15

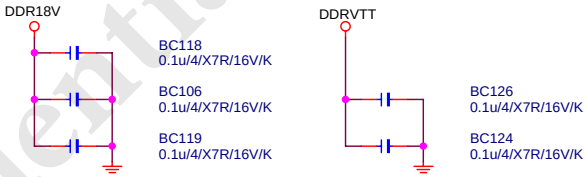
MODT_A[0..3] MODT_A[0..3] 10,15



DDR TERMINATION CHANNEL B

DDR18V Decouple

DDRVTT Decouple



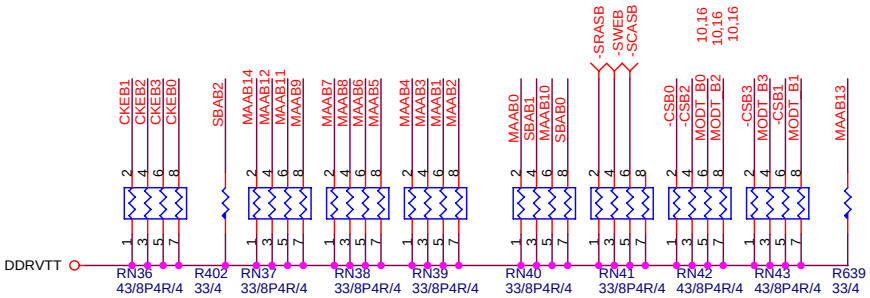
MODT_B[0..3] MODT_B[0..3] 10,16

SBAB[0..2] SBAB[0..2] 10,16

-CSB[0..3] -CSB[0..3] 10,16

CKEB[0..3] CKEB[0..3] 10,16

MAAB[0..14] MAAB[0..14] 10,16

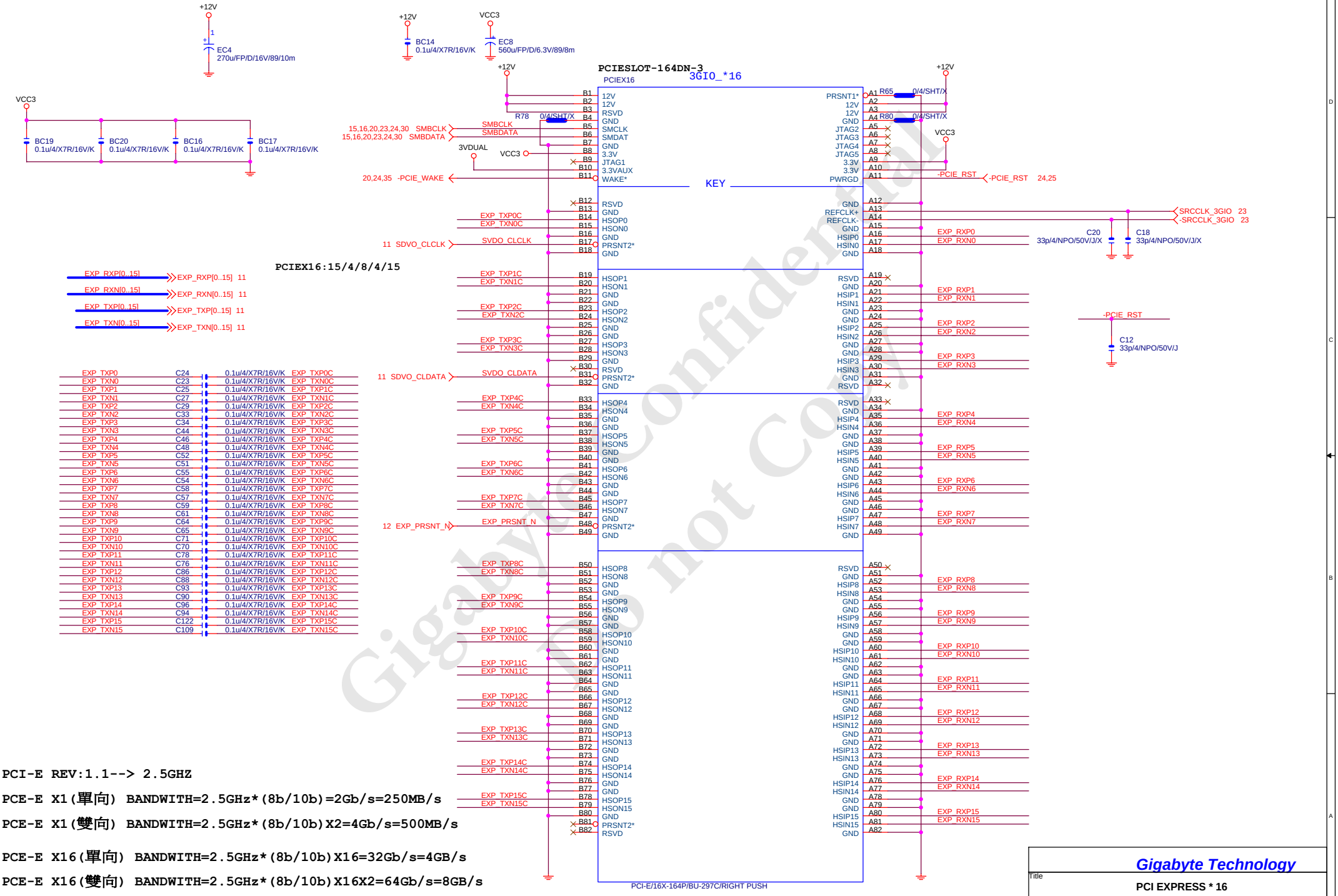


Gigabyte Technology

Title: DDRII TERMINATOR

Size: Custom | Document Number: GA-EP43-UD3L | Rev: 1.3

Date: Monday, April 26, 2010 | Sheet 17 of 36



PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWITH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

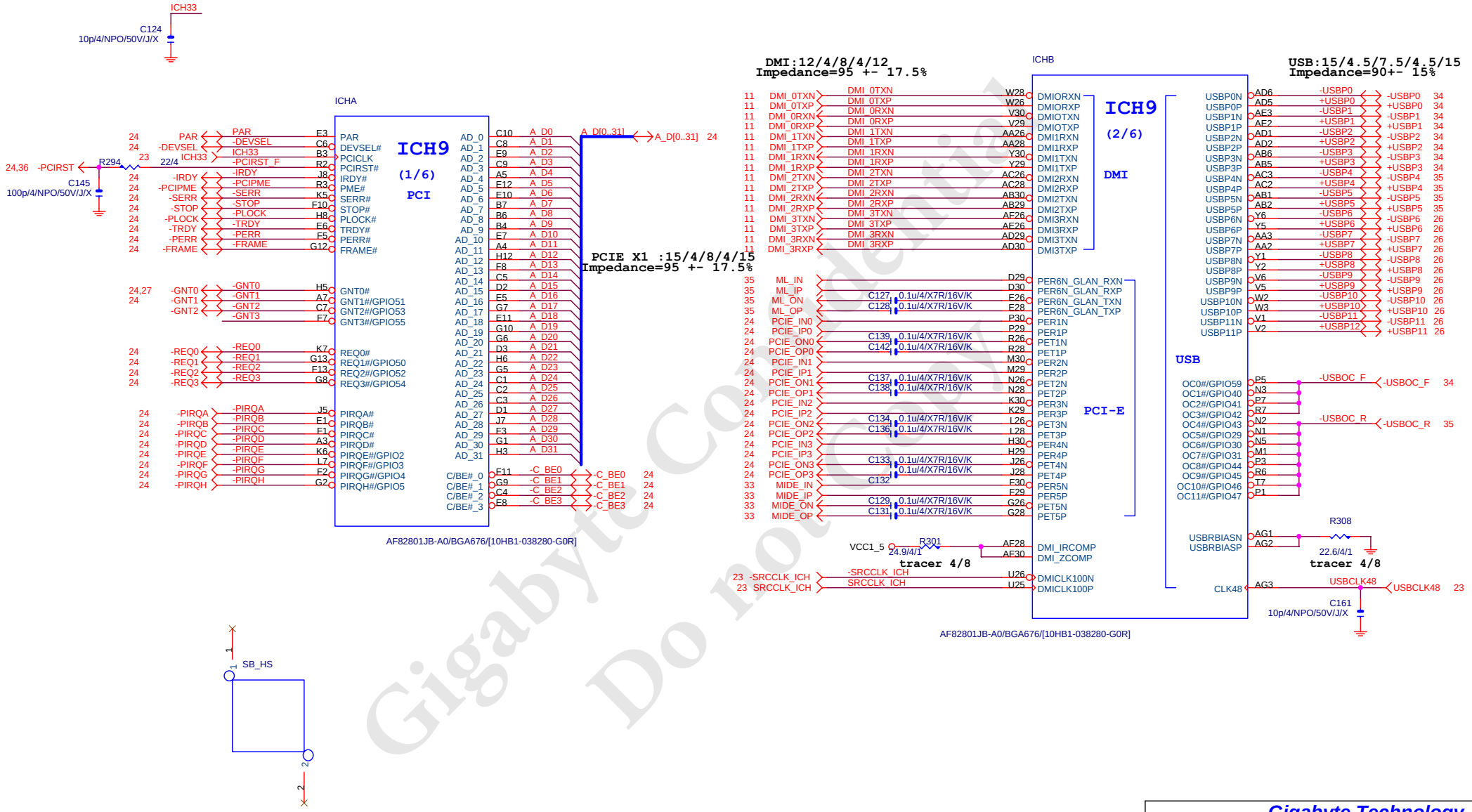
PCE-E X1(雙向) BANDWITH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWITH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWITH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s

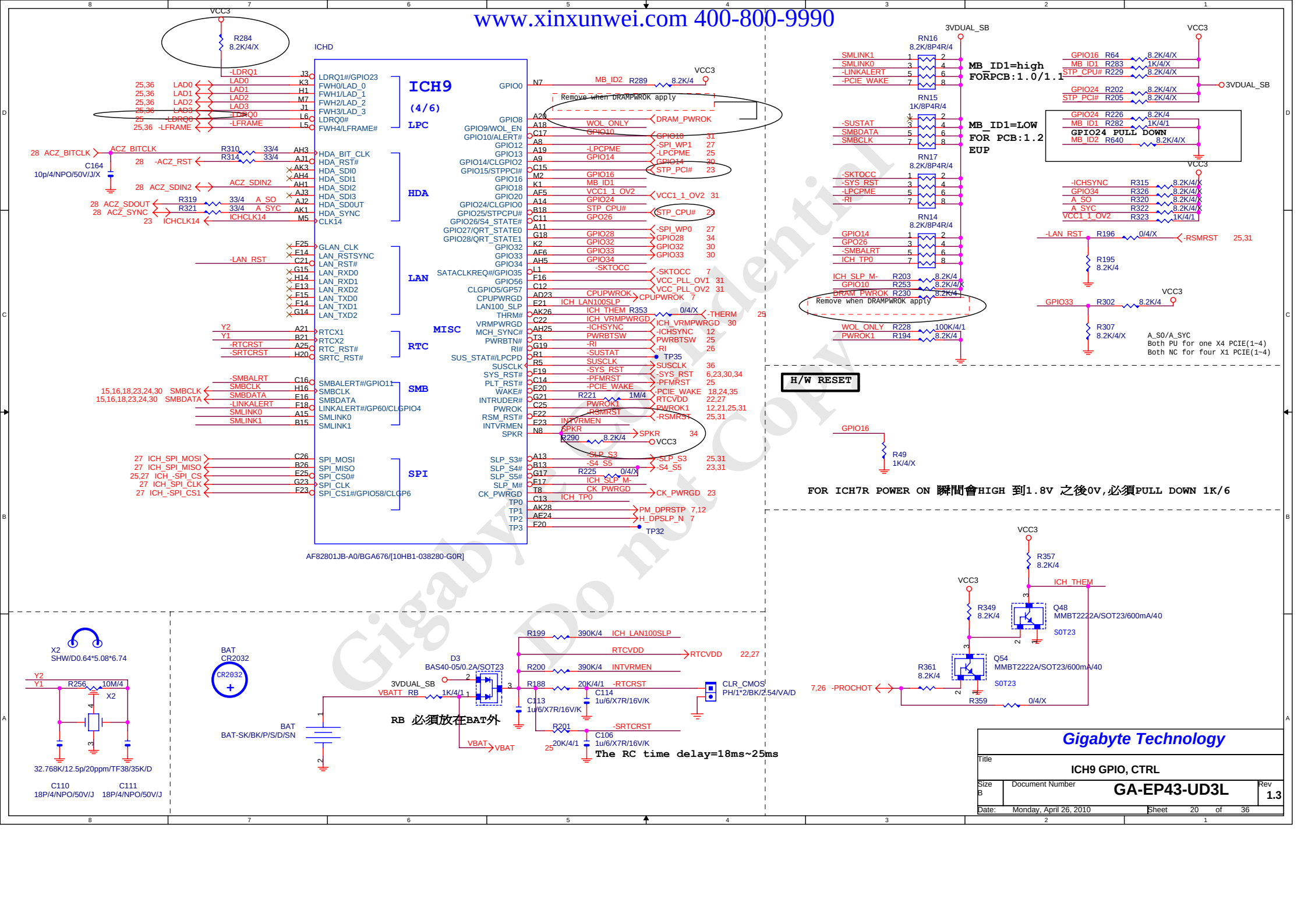
PCI-E REV:2.0--> 5GHZ

Gigabyte Technology		
Title: PCI EXPRESS * 16		
Size: Custom	Document Number: GA-EP43-UD3L	Rev: 1.3
Date: Monday, April 26, 2010	Sheet 18 of 36	



FOR UD series 專用heat sink

Gigabyte Technology		
Title: ICH9-PCI, DMI, LAN, USB		
Size: B	Document Number: GA-EP43-UD3L	Rev: 1.3
Date: Monday, April 26, 2010	Sheet 19 of 36	



CL_VREF:4/10
0.405V

VCC1_5
R257 24.9/6/1
ICHC

VCC3
R197 3.24K/4/1
R206 453/4/1
C95 0.1u/4/X7R/16V/K

12 CL_CLK → CL_CLK → G22 CL_CLK0
TP29
12 CL_DATA → CL_DATA → H21 CL_DATA0
TP31 → E19 TP4
R254 0/4/X S_VREF_ICH → C27 CL_VREF0
12,20,25,31 PWROK1 → A16 TP6 → T6 CLPWROK
TP30 → B16 TP7
12 -CL_RST → -CL_RST → G20 CL_RST0#

ICH9
(3/6)

A29 GLAN_COMPO
B29 GLAN_COMPI

31 ICH_FAN_PWM0 → ICH_FAN_PWM0 → AJ21 PWM0
31 ICH_FAN_PWM1 → ICH_FAN_PWM1 → AJ22 PWM1
31 ICH_FAN_PWM2 → ICH_FAN_PWM2 → AK22 PWM2

31 ICH_FAN_TACH0 → ICH_FAN_TACH0 → AH21 GPIO17/TACH0
31 ICH_FAN_TACH1 → ICH_FAN_TACH1 → AK21 GPIO1/TACH1
31 ICH_FAN_TACH2 → ICH_FAN_TACH2 → AH22 GPIO6/TACH2
ICH_FAN_TACH3 → AK23 GPIO7/TACH3

25 SST_IO → R255 0/4/SHT/X → C19 SST

31 VTT_GMCH_UV1 → AJ24 GPIO22/SCLOCK
31 VTT_GMCH_UV2 → AK24 GPIO38/SLOAD
R329 8.2K/4 GPIO39 → AH23 GPIO39/SDATAOUT0
VCC3 30 PSI_CTL → R335 8.2K/4/X → AD20 GPIO48/SDATAOUT1
R332 0/4/X → AJ25 GPIO49

GPIO49/DMI Termination Voltage
:LOW FOR DESKTOP

GPIO48 : Lo For Media BIOS
Hi For Disty BIOS

SATA

SATA0RXN AK17 SATA0RXN
SATA0RXP AJ17 SATA0RXP
SATA0TXN AK19 SATA0TXN
SATA0TXP AJ19 SATA0TXP
SATA1RXN AJ15 SATA1RXN
SATA1RXP AK15 SATA1RXP
SATA1TXN AH16 SATA1TXN
SATA1TXP AF16 SATA1TXP
SATA2RXN AJ13 SATA2RXN
SATA2RXP AK13 SATA2RXP
SATA2TXN AH14 SATA2TXN
SATA2TXP AF14 SATA2TXP
SATA3RXN AJ11 SATA3RXN
SATA3RXP AK11 SATA3RXP
SATA3TXN AF12 SATA3TXN
SATA3TXP AH12 SATA3TXP
SATA4RXN AJ9 SATA4RXN
SATA4RXP AK9 SATA4RXP
SATA4TXN AF10 SATA4TXN
SATA4TXP AH9 SATA4TXP
SATA5RXN AJ7 SATA5RXN
SATA5RXP AK7 SATA5RXP
SATA5TXN AF8 SATA5TXN
SATA5TXP AH7 SATA5TXP
SATACLKN AF18 -SRCCLK_SATA → -SRCCLK_SATA 23
SATACLKP AF19 SRCCLK_SATA → SRCCLK_SATA 23

ICH9R

SATA:15/4/8/4/15
Impedance=95 +- 17.5%

SATALED# AE7 -SATALED → -SATALED 34
SATARBIASN AK6 R327 24.9/4/1
SATABIASP AJ6

SATARBIASN=4MIL

GPIO21/SATA0GP AK25 → VTT_GMCH_OV1 31
GPIO19/SATA1GP AE20 → VTT_GMCH_OV2 31
GPIO36/SATA2GP AE21 VCC1_1_ICH_OV1 → VCC1_1_OV1 31
GPIO37/SATA3GP AE22 ICH_GPIO37 → ICH_GPIO37 30
SATA4GP AF22 SATA4GP
SATA5GP AD21 SATA5GP

HOST

A20GATE P8 A20GATE → A20GATE 25
A20M# AJ28 -A20M → -A20M 7

IGNNE# AC22 -IGNNE → -IGNNE 7
INIT3_3V# M3 -FWHINIT → TP34
INIT# AE23 -HINIT → -HINIT 5
INTR AH27 INTR → INTR 7
FERR# AJ27 -FERR → -FERR 7
NMI AF24 NMI → NMI 7
RCIN# L3 -KBRST → -KBRST 25
SERIRQ N6 SERIRQ → SERIRQ 25,36
SMI# AH26 -SMI → -SMI 7
STPCLK# AJ29 -STPCLK → -STPCLK 7
THRMTRIP# AD24 -THRMTRIP → -THRMTRIP 7
PECI AC23 SB_PECI → PECI 7,25

R364 0/4/X

AF82801JB-A0/BGA676/[10HB1-038280-G0R]

5VSB
R366 8.2K/4
25 PECI_CTL → R365 1K/4/1
Q59 2N7002/SOT23/25pF/5
PECI
SB_PECI

3VDUAL_SB
R204 3.24K/4/1
R227 453/4/1
S_VREF_ICH

ICH10 remove after verify

Can't SWAP PIN

VCC3
RN26 8.2K/8P4R/4
25,36 SERIRQ
SERIRQ
A20GATE
-KBRST
RN35 1K/8P4R/4
VTT_GMCH_OV1
SATA4GP
VTT_GMCH_OV2
SATA5GP
ICH_FAN_TACH0 R333 8.2K/4/X
VCC1_1_OV1 R328 8.2K/4
ICH_GPIO37 R334 8.2K/4
VTT_GMCH_UV1 R331 8.2K/4
VTT_GMCH_UV2 R330 8.2K/4

The ICH8 integrated GbE LAN test mode is activated any time the ICH8 GPIO39 signal is not at a low logic level.

Workaround
Under investigation. Possible workaround is to use a weak pulldown resistor on GPIO39 to ensure signal is always low

SATA:15/4/8/4/15
Impedance=95 +- 17.5%

SATA2_0
SATA0TXP 0.01u/4/X7R/25V/K C233 SATA0TXPC
SATA0TXN 0.01u/4/X7R/25V/K C230 SATA0TXNC
SATA0RXN 0.01u/4/X7R/25V/K C227 SATA0RXNC
SATA0RXP 0.01u/4/X7R/25V/K C224 SATA0RXPC
GND A+ A- GND B- B+ GND
SATA2/7/BU/H/OP/VA/D/1/B

SATA2_1
GND B+ B- GND A- A+ GND
SATA1RXPC C208 0.01u/4/X7R/25V/K SATA1RXP
SATA1RXNC C209 0.01u/4/X7R/25V/K SATA1RXN
SATA1TXNC C214 0.01u/4/X7R/25V/K SATA1TXN
SATA1TXPC C218 0.01u/4/X7R/25V/K SATA1TXP
SATA2/7/BU/H/OP/VA/D/1/B

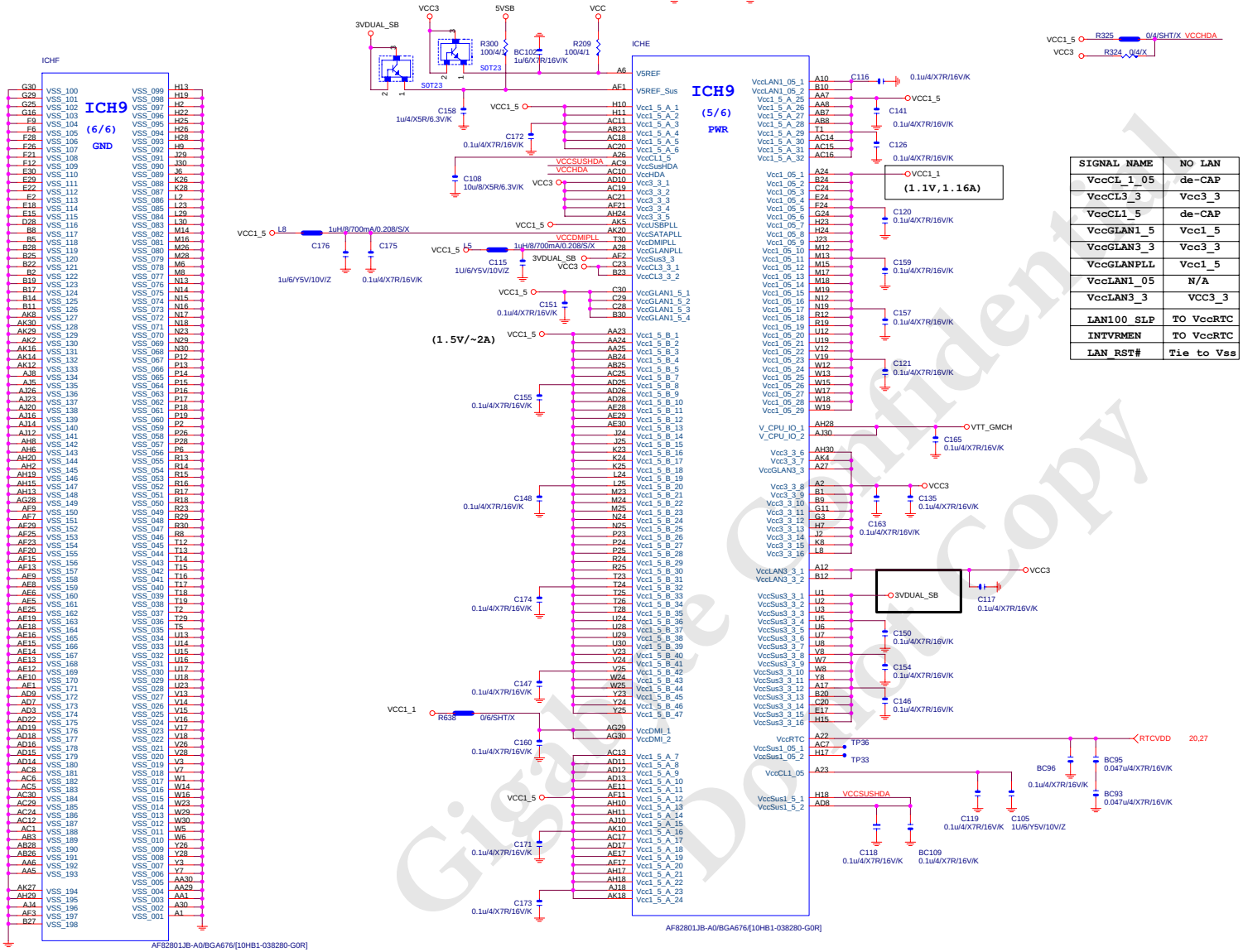
SATA2_4
SATA4TXP 0.01u/4/X7R/25V/K C188 SATA4TXPC
SATA4TXN 0.01u/4/X7R/25V/K C186 SATA4TXNC
SATA4RXN 0.01u/4/X7R/25V/K C183 SATA4RXNC
SATA4RXP 0.01u/4/X7R/25V/K C181 SATA4RXPC
GND A+ A- GND B- B+ GND
SATA2/7/BU/H/OP/VA/D/1/B

SATA2_5
GND B+ B- GND A- A+ GND
SATA5RXPC C190 0.01u/4/X7R/25V/K SATA5RXP
SATA5RXNC C193 0.01u/4/X7R/25V/K SATA5RXN
SATA5TXNC C194 0.01u/4/X7R/25V/K SATA5TXN
SATA5TXPC C195 0.01u/4/X7R/25V/K SATA5TXP
SATA2/7/BU/H/OP/VA/D/1/B

SATA2_2
SATA2TXP 0.01u/4/X7R/25V/K C229 SATA2TXPC
SATA2TXN 0.01u/4/X7R/25V/K C226 SATA2TXNC
SATA2RXN 0.01u/4/X7R/25V/K C221 SATA2RXNC
SATA2RXP 0.01u/4/X7R/25V/K C217 SATA2RXPC
GND A+ A- GND B- B+ GND
SATA2/7/BU/H/OP/VA/D/1/B

SATA2_3
GND B+ B- GND A- A+ GND
SATA3RXPC C184 0.01u/4/X7R/25V/K SATA3RXP
SATA3RXNC C187 0.01u/4/X7R/25V/K SATA3RXN
SATA3TXNC C189 0.01u/4/X7R/25V/K SATA3TXN
SATA3TXPC C191 0.01u/4/X7R/25V/K SATA3TXP
SATA2/7/BU/H/OP/VA/D/1/B

Gigabyte Technology			
Title: ICH9- SATA, FAN CTRL			
Size: Custom	Document Number: GA-EP43-UD3L		Rev: 1.3
Date: Monday, April 26, 2010	Sheet 21 of 36		



SIGNAL NAME	NO LAN
VccCL_1_05	de-CAP
VccCL3_3	Vcc3_3
VccCL1_5	de-CAP
VccGLAN1_5	Vcc1_5
VccGLAN3_3	Vcc3_3
VccGLANPLL	Vcc1_5
VccLAN1_05	N/A
VccLAN3_3	VCC3_3
LAN100_SLP	TO VccRTC
INTVRMEN	TO VccRTC
LAN_RST#	Tie to Vss

Gigabyte Technology			
Title: ICH9-PWR & GND			
Size: C	Document Number: GA-EP43-UD3L		Rev: 1.3
Date: Monday, April 26, 2010	Sheet 22 of 36		

CLK GEN CK505

U2

ICS9LPRS914[10HL6-180914-20R]

50歐姆:[18/4/10/4/18]

50歐姆:[18/4/10/4/18]

50歐姆:[18/4/10/4/18]

50歐姆:[4/10]

50歐姆:[4/10]

50歐姆:[4/10]

3VDUAL

CKVDD

VCC3

GSEL=1,96Mhz from 14/15,SATACLK from 17/18
GSEL=0,SATACLK from 14/15,PCIECLK from 17/18

SEL_48=1, 24Mhz from pin10
SEL_48=0, 48Mhz from pin10

Trusted Mode

overclocking

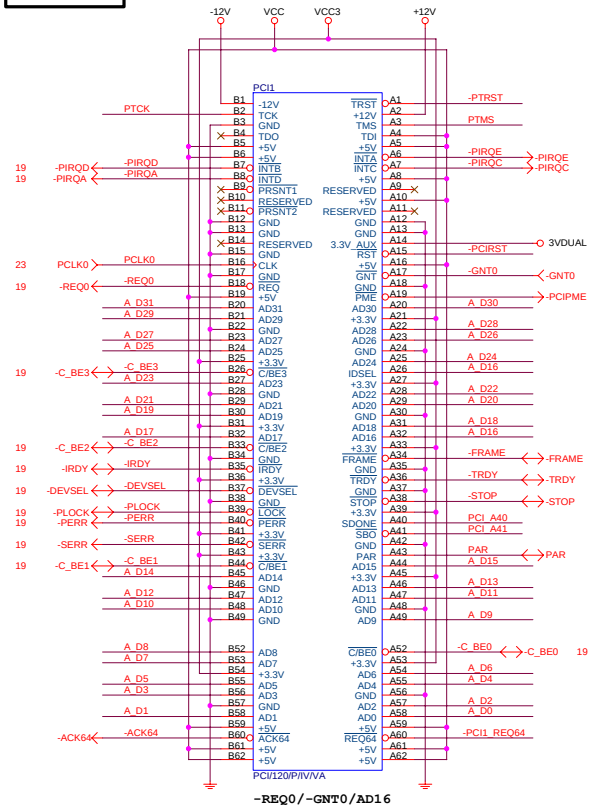
for EMI

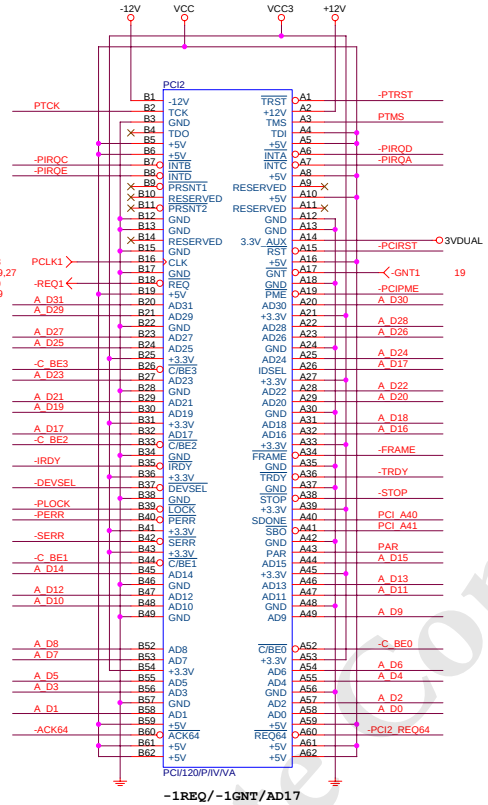
EUP

Gigabyte Technology

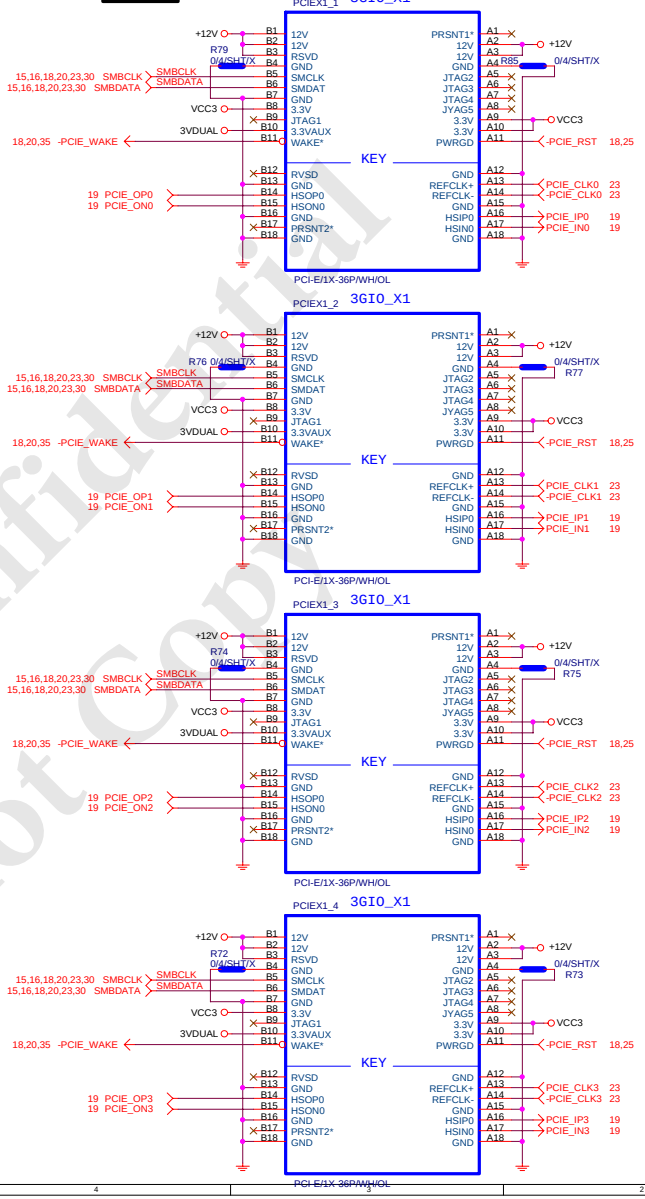
Title	CK505 CLK GEN	
Size: Custom	Document Number: GA-EP43-UD3L	Rev: 1.3
Date: Monday, April 26, 2010	Sheet 23 of 36	

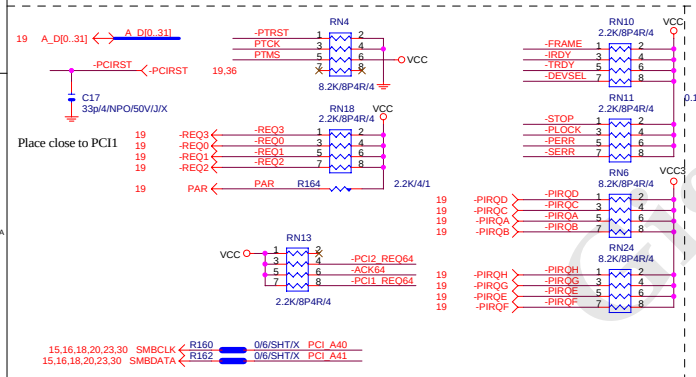
PCI1,2 SLOT





PCIE*1





Gigabyte Technology			
Title	PCI SLOT 1, 2/PCIEX1		
Size: Custom	Document Number: GA-EP43-UD3L		Rev: 1.3
Date: Monday, April 26, 2010	Sheet 24 of 36		

IT8712F LPC I/O

改版要注意:
1.DDR GPIO PIN要選用main power的pin
2.VIN PIN如不用,要8.2K PULL HI TO VCC

U1 — IT8718F-S/LX(GB)/S

-RST_BTN
P.U一定要指定用1K到VCC

如果BSEL0/1 直接拉TO N/B,R1768/R1769 不上

JP7 : HIGH DUAL BIOS ENABLE
LOW DUAL BIOS DISABLE

RTS2- ==LOW CPU FAN 50%
==HIGH 100%

1.2V or 3.3V tolerance select.
1.2V OUTPUT 接 VTT_GMCH
3.3V OUTPUT 接3.3V
LPCPD#=VIDVCC

VTT_GMCH/VCC3/VIDVCC 請走20~30

SOUT2	1	VID pins threshold voltage select: Vih / Vil : 2.0 / 0.8V
	0	VID pins threshold voltage select: Vih / Vil : 0.8 / 0.4V
DTR2-	1	Open Drain pin:Driving 較弱
	0	Push-pull Pin :Driving 較強
RTS2-	1	CPU FAN 100%
	0	CPU FAN 50%

Gigabyte Technology

Title: ITE 8712 LPC IO

Size: B | Document Number: GA-EP43-UD3L | Rev: 1.3

Date: Monday, April 26, 2010 | Sheet 25 of 36

COMA

AU1 GD75232/TSSOP20

25	RI1-	19	RY1	RA1	2	NRIA-
25	CTS1-	18	RY2	RA2	3	NCTSA-
25	DSR1-	17	RY3	RA3	4	NDSRA-
25	RTS1-	16	DA1	DY1	5	NRTSA-
25	DTR1-	15	DA2	DY2	6	NDTRA-
25	RXD1	14	RY4	RA4	7	NSINA
25	TXD1	13	DA3	DY3	8	NSOUTA
25	DCD1-	12	RY5	RA5	9	NDCDA-
		11	GND	5V	20	
-12V		10	-12V	12V	1	VCC / +12V

ABC3 0.1u/4/X7R/16V/K · ABC1 0.1u/4/X7R/16V/K · ABC2 0.1u/4/X7R/16V/K

COM RI

REV:0.1 驗證

Q5 MMBT2222A/SOT23/600mA/40

NRIA- — D2 CD4148WP/1206/300mA — R71 75K/4/1 — R67 8.2K/4 — S0T23 — -RI → -RI 20

COMA

COMA BH/2*5K10/IV/2.54/VA/COM

NDCDA-	1 2	NSINA
NSOUTA	3 4	NDTRA-
	5 6	NDSRA-
NRTSA-	7 8	NCTSA-
NRIA-	9 10	

ACN2 180p/8P4C/6/NPO/50V/K

NDTRA-	7 8	
NSINA	5 6	
NSOUTA	3 4	
NDCDA-	1 2	

ACN1 180p/8P4C/6/NPO/50V/K

NRIA-	7 8	
NCTSA-	5 6	
NDSRA-	3 4	
NRTSA-	1 2	

FUSEVCC / FUSEVCC / FUSEVCC1 — R_USB_1 / R_USB_2 / R_USB_3

19	-USBP10	-USBP11	19	-USBP8	-USBP9	19	19	-USBP6	-USBP7	19
19	+USBP10	+USBP11	19	+USBP8	+USBP9	19	19	+USBP6	+USBP7	19

USB/A/O/BLACK/GF/2/RA/D

LPT PORT

PRN6 33/8P4R/4

25	STB-	STB-	1 2	LPT1
25	AFD-	AFD-	3 4	LPT14
25	INIT-	INIT-	5 6	LPT16
25	SLIN-	SLIN-	7 8	LPT17

PRN4 33/8P4R/4

PD3	1 2	LPT5
PD2	3 4	LPT4
PD1	5 6	LPT3
PD0	7 8	LPT2

PRN2 33/8P4R/4

PD7	1 2	LPT9
PD6	3 4	LPT8
PD5	5 6	LPT7
PD4	7 8	LPT6

25	ERR-	ERR-
25	ACK-	ACK-
25	BUSY	BUSY
25	PE	PE
25	SLCT	SLCT
25	PD[0..7]	PD[0..7]

PD1 CD4148WP/1206/300mA · VCC · PBC1 0.1u/4/X7R/16V/K · PC1 1u/6/Y5V/10V/Z/X

PRN3 2.2K/8P4R/4

		LPT4
		LPT5
		LPT3
		LPT17

PRN1 2.2K/8P4R/4

		LPT8
		LPT9
		LPT6
		ACK-

PRN5 2.2K/8P4R/4

		LPT16
		LPT1
		ERR-
		LPT2

PRN7 2.2K/8P4R/4

		LPT7
		SLCT
		PE
		BUSY

PR1 2.2K/4/1 — LPT14

DYNAMIC CURRENT OC

+12V

7	VCC_SENSE	DR76 5.1K/4/1	DU6A LM324DR/SO14	DU6B LM324DR/SO14	
7	VSS_SENSE	DR71 5.1K/4/1	DR75 5.1K/4/1	DR72 5.1K/4/1	DR74 453K/4/1	DR73 10K/4/1	DR77 10K/4/1	DU6C LM324DR/SO14	FB 30
									CURRENT_OUT_V 27

DR78 453K/4/1

-PROHOT

asserted at 129 degree

deasserted at 116 degree

RS2 CLOSE CPU VR MOSFET

LPT

LPT1	1 2	LPT14
LPT2	3 4	ERR-
LPT3	5 6	LPT16
LPT4	7 8	LPT17
LPT5	9 10	
LPT6	11 12	
LPT7	13 14	
LPT8	15 16	
LPT9	17 18	
ACK-	19 20	
BUSY	21 22	
PE	23 24	
SLCT	25 26	

BH/2*13K24/WH/2.54/VA/[11NH3-000213-31R]

+12V — R383 10K/4/1 — R369 1.96K/4/1 — R370 1K/4/1 — RS2 100K/1/4/S — C199 0.1u/4/X7R/16V/K/X

R378 34K/4/1 — R379 0/4/X — DU6D LM324DR/SO14 — TSM_5 — TSM_6 — TSM_7 — R? CLOSE Q32

VR_HOT 30 — -PROCHOT 7,20 — Q52 2N7002/SOT23/25pF/5 — S0T23 — -FORCEPR — -FORCEPR 7 — Q56 2N7002/SOT23/25pF/5 — S0T23

CLOSE PWM HOT MOSFET

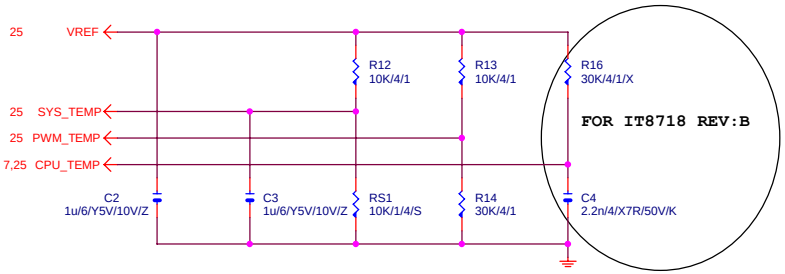
Gigabyte Technology

Title: COM & LPT PORT

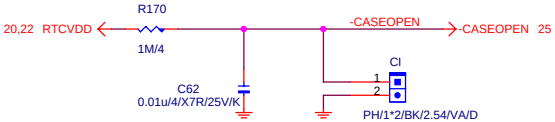
Size: Custom | Document Number: GA-EP43-UD3L | Rev: 1.3

Date: Monday, April 26, 2010 | Sheet 26 of 36

TEMP H/W MONITOR

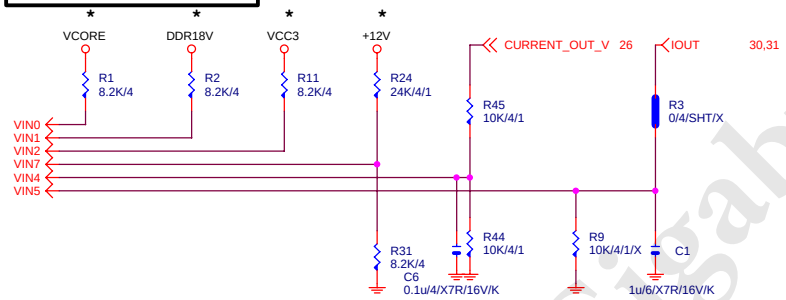


CASE OPEN

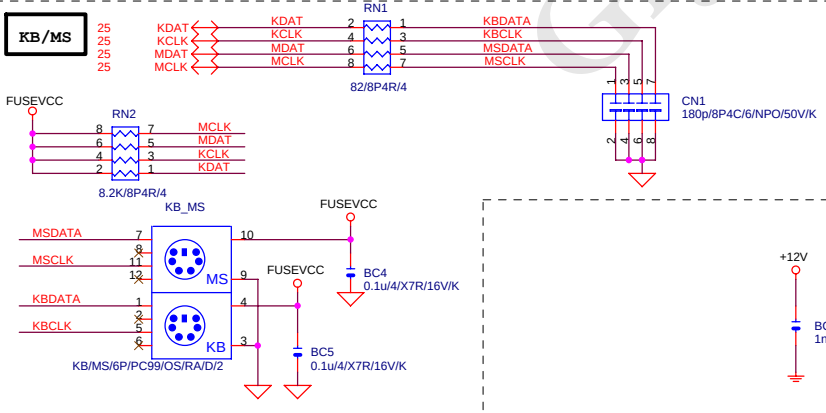


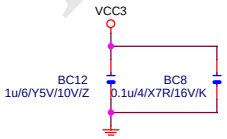
Case Open Circuits

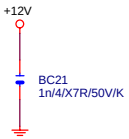
VOLTAGE-- H/W MONITOR

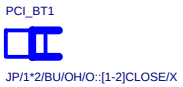


KB/MS









Gigabyte Technology		
Title: BIOS/HW-MONITOR/CI/KB/MS		
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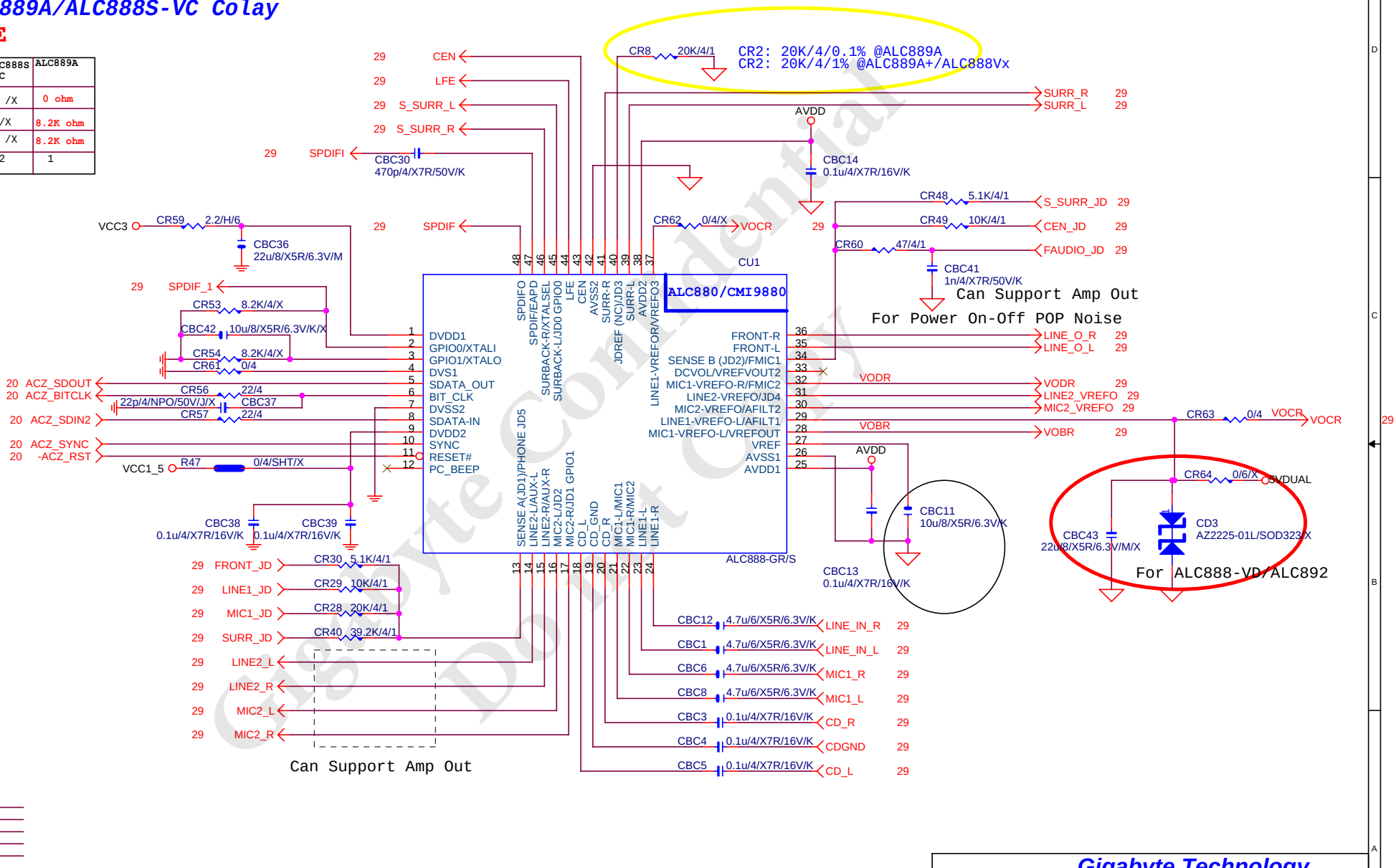
AZALIA CODEC

ALC888/ALC889A/ALC888S-VC Colay

BOM TABLE

	ALC888	ALC888S-VC	ALC889A
CR61	0 ohm	/X	0 ohm
CR53(SPDIF2)	/X	/X	8.2K ohm
CR54	/X	/X	8.2K ohm
SPDIF組數	1	2	1



Gigabyte Technology		
Title: ALC888		
Size: Custom	Document Number: GA-EP43-UD3L	Rev: 1.3
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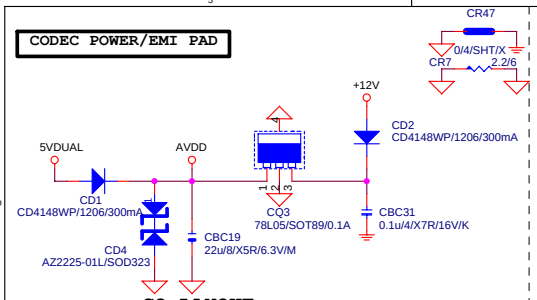
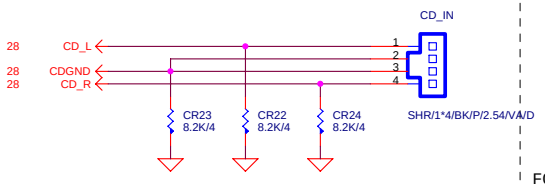
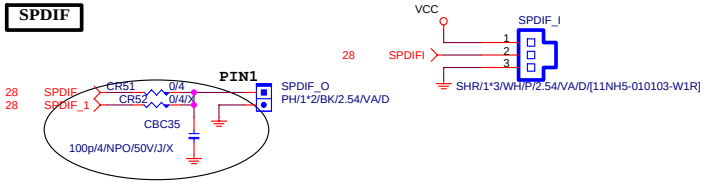
CODEC POWER/EMI PAD



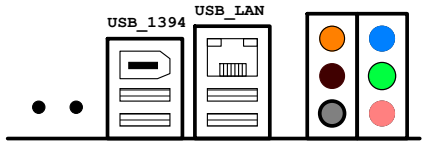
CD IN

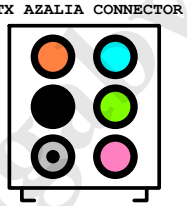


SPDIF



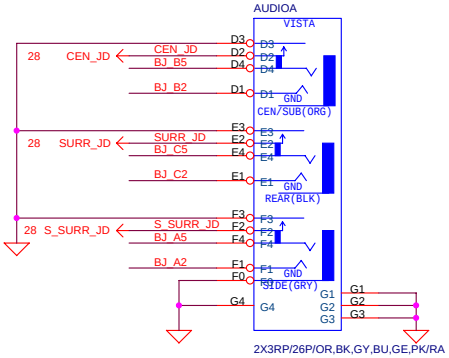
AZALIA JACK

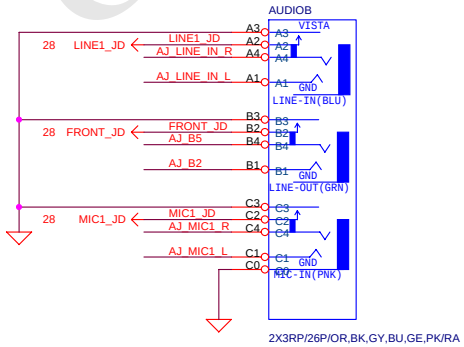




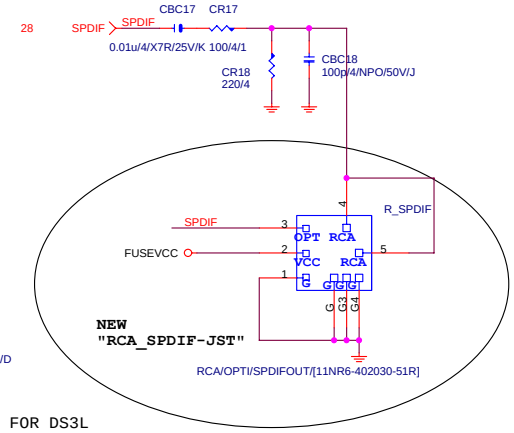
3RP/26P/OR,BK,GY,BU,GE,PK/RA/D/1/B

VISTA規範:REAR-->BLK,CEN/SUB-->ORG





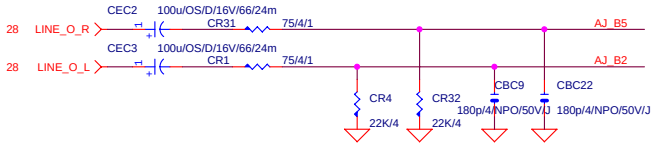
Fpr
EMI



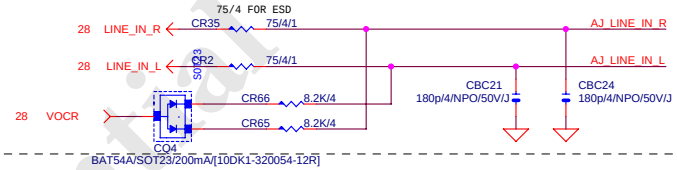
FOR DS3L
11NR6-402030-41R(無鐵殼)11NR6-402030-51R/52R(鐵殼)

FOR S3L 11NR6-501004-G1R ONLY support RCA

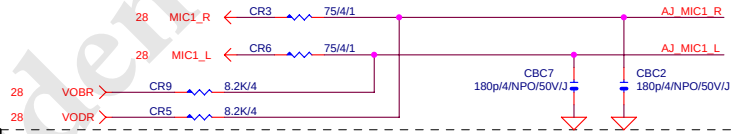
LINE-OUT



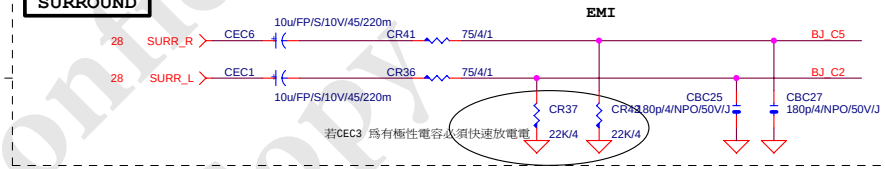
LINE-IN



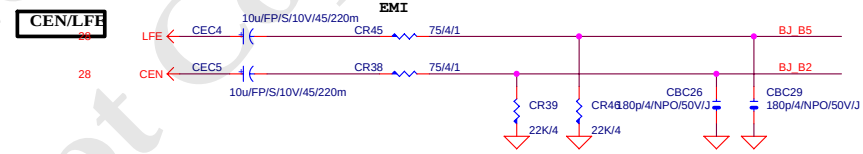
MIC-IN



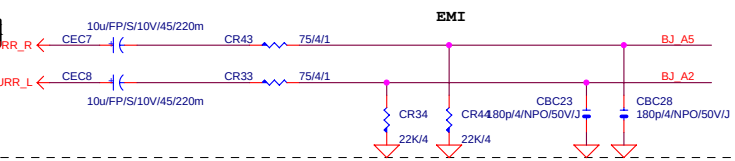
SURROUND



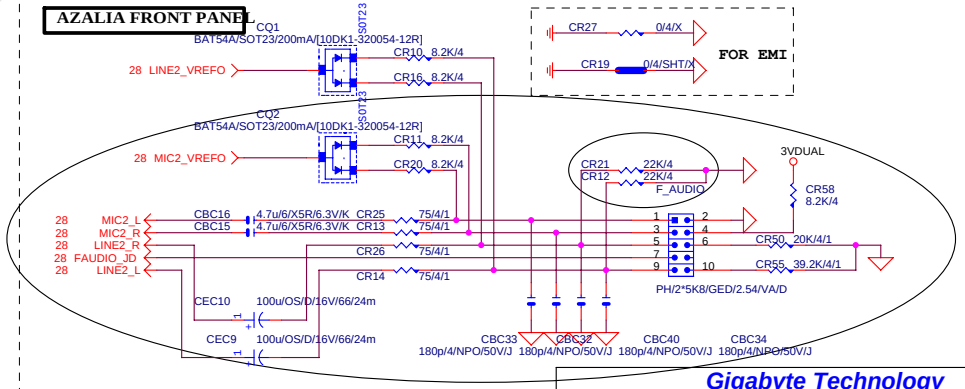
CEN/LFE



SURR BACK

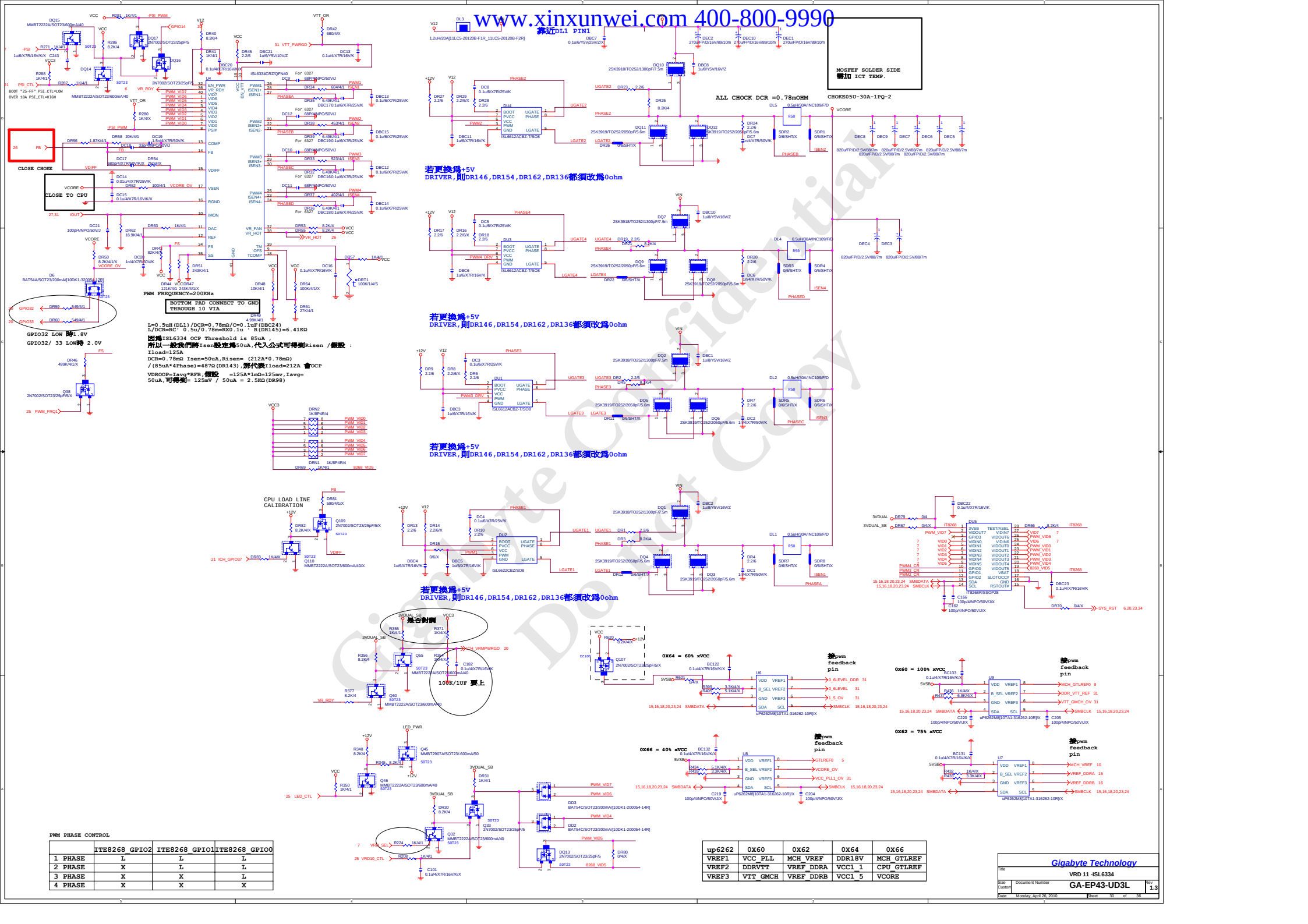


AZALIA FRONT PANEL



Gigabyte Technology

Title	AUDIO JACK	
Size: Custom	Document Number: GA-EP43-UD3L	Rev: 1.3
Date: Monday, April 26, 2010	Sheet 29 of 36	



PWM PHASE CONTROL

	ITE8268_GPIO2	ITE8268_GPIO1	ITE8268_GPIO0
1 PHASE	L	L	L
2 PHASE	X	L	L
3 PHASE	X	X	L
4 PHASE	X	X	X

up6262	0X60	0X62	0X64	0X66
VREF1	VCC_PLL	MCH_VREF	DDR18V	MCH_GTLREF
VREF2	DDRVTT	VREF_DDRA	VCC1_1	CPU_GTLREF
VREF3	VTT_GMCH	VREF_DDRB	VCC1_5	VCORE

Gigabyte Technology

Title	VRD 11 -ISL6334	
Size: Custom	Document Number: GA-EP43-UD3L	Rev: 1.3
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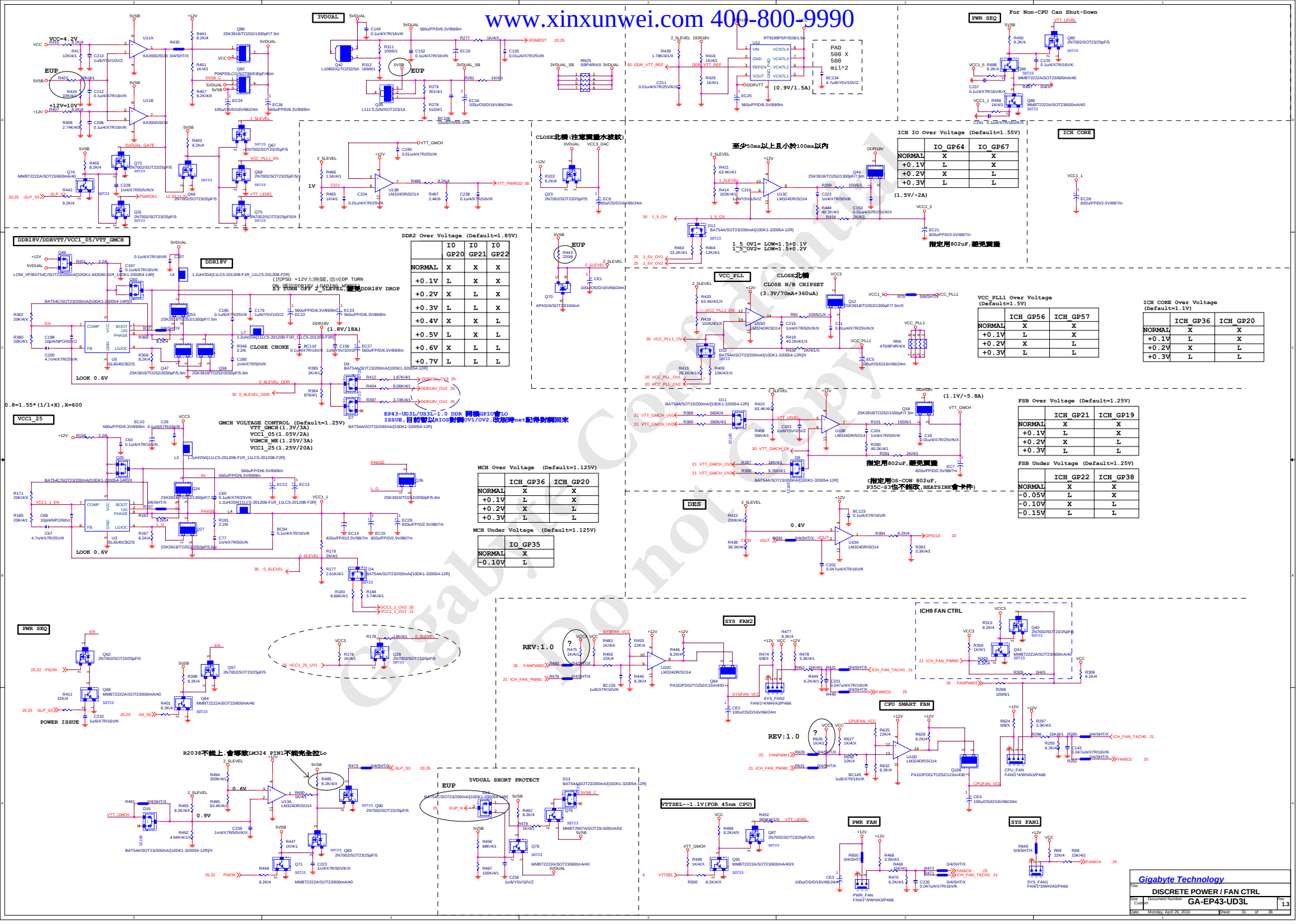
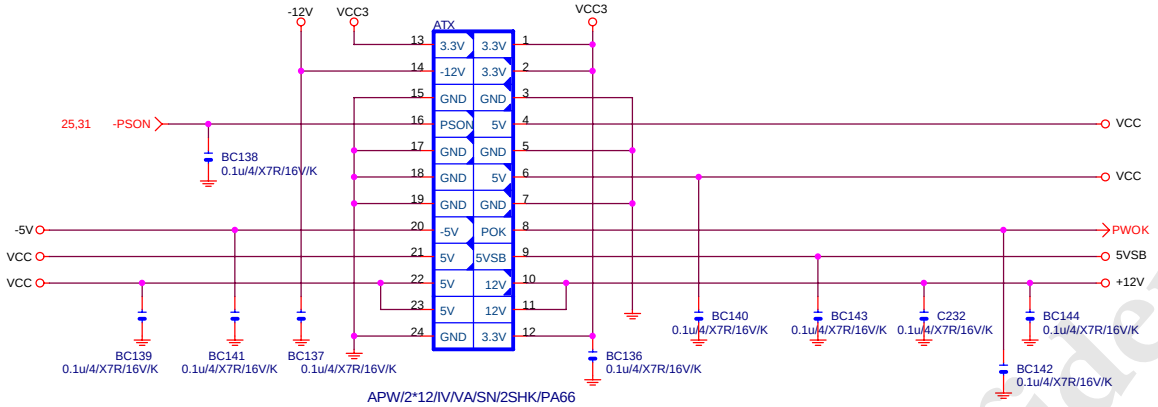
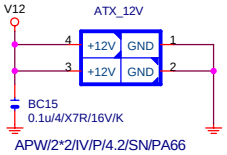
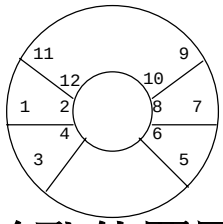
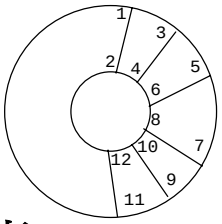


ATX POWER CONNECTOR

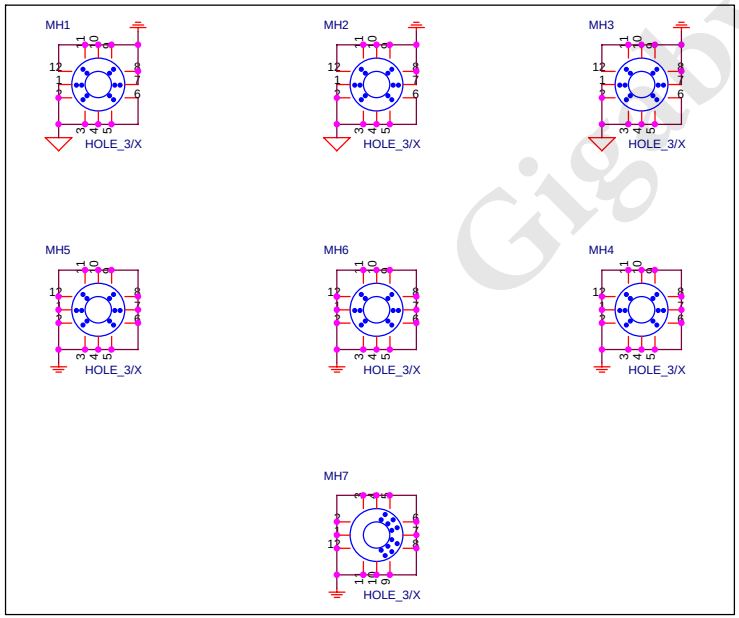


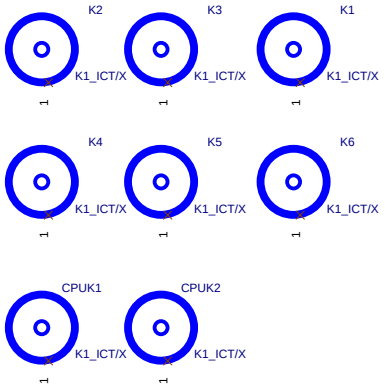


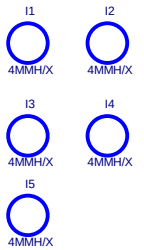




螺絲孔位置圖 (注意Footprint不同)







Gigabyte Technology		
Title: ATX POWER CONNECTOR		
Size: B	Document Number: GA-EP43-UD3L	Rev: 1.3
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3.3V to 1.8V Voltage Regulator

L1117LG/N/SOT223/1A

RQ1 — VCC_1.8V → VCC3

RR1 100/4/1

RR2 44.2/4/1

68/4/1 FOR JMB368
VCC1.8V=2.1V

44.2/4/1 FOR JMB368
VCC1.8V=1.8V

RBC6 0.1u/4/X7R/16V/K

RBC1 10u/8/X5R/6.3V/K

REC2 100u/OS/D/16V/66/24m

25,35 -PFMRST2 → -PFMRST2

RC1 100P/4/N/50V/X

RU1 — JMB368 — JM368/LQFP40

DMARQA	37	XIDMRAQA	
DD15A	38	ZIDD15A	
VCC3	39	DV33	
GND	40	XSMBCLK	
GND	41	XSMBDAT	
-PFMRST2	42	XRSTn	
DD0A	43	ZIDD0A	
DD14A	44	ZIDD14A	
DD1A	45	ZIDD1A	
DD13A	46	ZIDD13A	
DD2A	47	ZIDD2A	
DD12A	48	ZIDD12A	

		ZIDD3A	24 DD3A
		ZIDD11A	23 DD11A
		DV33	22 VCC3
		ZIDD4A	21 DD4A
		ZIDD10A	20 DD10A
		ZIDD5A	19 DD5A
		ZIDD9A	18 DD9A
		ZIDD6A	17 DD6A
		ZIDD8A	16 DD8A
		ZIDD7A	15 DD7A
		YROMCSn	14
		XTEST	13 GND

DMACKnA, IORDYA, DIORnA, DIOWnA, DVDD_1.8V, INTRQA, PDIAGnA, DA1A, DA0A, DA2A, CS0nA, CS1nA

YIDMACKnA, YIIORDYA, YIDIORnA, YIDIOWnA, DV18, XINTRQA, XICBLIDA, YIDA1A, YIDA0A, YIDA2A, YICS0nA, YICS1nA

DGND33, ACPLKN, ACPLKP, APV18, APG18, APREXT, APRXP, APRXN, APV18, APG18, APTXN, APTXP

GND, -SRCCLK_IDE, SRCCLK_IDE, APVDD_1.8V, GND, PCIE_REXT1, MIDE_OP, MIDE_ON, APVDD_1.8V, GND, PCIE_TXN, PCIE_TXP

RC2 0.1u/4/X7R/16V/K → MIDE_IP 19
RC3 0.1u/4/X7R/16V/K → MIDE_IN 19
MIDE_ON 19
MIDE_OP 19
SRCCLK_IDE 23
-SRCCLK_IDE 23

VCC → RR7 1K/4/1 → PH_RESETnA

VCC3 → RR3 8.2K/4

RQ2 MMBT2222A/SOT23/600mA/40 S0T23

-PFMRST2 → OLNY FOR JMB368

PH_DD7 DD7A
PH_DD8 DD8A
PH_DD6 DD6A
PH_DD9 DD9A

PH_DD5 DD5A
PH_DD4 DD4A
PH_DD10 DD10A
PH_DD11 DD11A

PH_DD3 DD3A
PH_DD12 DD12A
PH_DD2 DD2A
PH_DD13 DD13A

PH_DD1 DD1A
PH_DD0 DD0A
PH_DD14 DD14A
PH_DD15 DD15A

PH_DIOW_N DIOWnA
PH_DIOR_N DIORnA
PH_DMACK_N DMACKnA
PH_DA1 DA1A
PH_DA0 DA0A
PH_CS0_N CS0nA
PH_DA2 DA2A
PH_CS1_N CS1nA

PH_IORDY IORDYA
PH_DMARQ DMARQA
PH_INTRQ INTRQA
PH_CBLID_N PDIAGnA

VCC3 → RBC7 0.1u/4/X7R/16V/K, RBC5 0.1u/4/X7R/16V/K

close to IC

VCC3, VCC3, VCC3 → RBC3 10u/8/X5R/6.3V/K, RBC2 0.1u/4/X7R/16V/K, REC1 100u/OS/D/16V/66/24m

Close to pin22 and pin39

PCIE_REXT1 → RR9 8.06K/4/1 Near to PIN

VCC3 → RR12 1K/4/X → RQ3 → -HDLED → -HDLED 34

DASPnXA → RC4 180P/4/N/50V/X

RR11 0/4/X

BAT54A/SOT23/200mA/[10DK1-320054-12R]

VCC_1.8V, DVDD_1.8V → RBC9 0.1u/4/X7R/16V/K

VCC_1.8V, APVDD_1.8V → RBC10 0.1u/4/X7R/16V/K, RBC8 10u/8/X5R/6.3V/K

CLOSE TO pin22

VCC_1.8V, APVDD_1.8V → RBC11 10u/8/X5R/6.3V/K, RBC4 0.1u/4/X7R/16V/K

close to pin17

VCC3 → PH_IORDY RR4 1K/4/1

CSELA RR10 0/4/SHT/X

PH_DMARQ RR6 8.2K/4

PH_INTRQ RR5 8.2K/4

DD7A RR8 8.2K/4

IDE Connector

IDE

PH_RESETnA	1	2	
PH_DD7	3	4	PH_DD8
PH_DD6	5	6	PH_DD9
PH_DD5	7	8	PH_DD10
PH_DD4	9	10	PH_DD11
PH_DD3	11	12	PH_DD12
PH_DD2	13	14	PH_DD13
PH_DD1	15	16	PH_DD14
PH_DD0	17	18	PH_DD15
	19		(#20 key-pin)
PH_DMARQ	21	22	
PH_DIOW_N	23	24	
PH_DIOR_N	25	26	(#28 CSEL)
PH_IORDY	27	28	CSELA
PH_DMACK_N	29	30	
PH_INTRQ	31	32	(#32 IOCS16)
PH_DA1	33	34	PH_CBLID_N
PH_DA0	35	36	PH_DA2
PH_CS0_N	37	38	PH_CS1_N
DASPnXA	39	40	

BH/2*20K20/WH/SHN/2.54/VA/PA46

Gigabyte Technology		
Title: JMR363		
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FRONT USB1

5VDUAL
SMD1812P350SLR/S
F5
EC18
560u/FP/D/6.3V/89/8m
F_USB1
BC103
0.1u/4/X7R/16V/K

19 +USBP0 +USBP0
19 -USBP0 -USBP0
19 +USBP1 +USBP1
19 -USBP1 -USBP1

-USBP0 +USBP0 -USBP1 +USBP1

BH/2*5K9/BU/ON/2.54/VA/D/GF

FOR EMI

VCC C85 1000P/4/X7R/25V/K/X VCC3

FRONT USB2

5VDUAL
F4
SMD1812P350SLR/S
F_USB2
BC90
0.1u/4/X7R/16V/K

19 +USBP2 +USBP2
19 -USBP2 -USBP2
19 +USBP3 +USBP3
19 -USBP3 -USBP3

-USBP2 +USBP2 -USBP3 +USBP3

BH/2*5K9/BU/ON/2.54/VA/D/GF

FOR EMI

VCC C89 1000P/4/X7R/25V/K/X VCC3

FRONT USB OC

SOT23
D5
BAT54A/SOT23/200mA/[10DK1-320054-12R]
5VDUAL
R270 150K/4
-USBOC_F -USBOC_F 19
R273 270K/4

FLOPPY

VCC
RN3 470/8P4R/4
R53 470/4/1
FDD

DENSEL- DENSEL- 25
INDEX- INDEX- 25
MOTEA- MOTEA- 25
DRVA- DRVA- 25
DIR- DIR- 25
STEP- STEP- 25
WDATA- WDATA- 25
WGATE- WGATE- 25
TK00- TK00- 25
WPT- WPT- 25
RDATA- RDATA- 25
SIDE1- SIDE1- 25
DSKCHG- DSKCHG- 25

BH/2*17K5/WH/SHN/2.54/VA/PA46

SATA LED

VCC3
R374 1K/4/1
-HDLED
C192 180p/4/NPO/50V/J/X
R373 1K/4/1
R367 8.2K/4
21 -SATALED -SATALED
S0T23 S0T23
Q63 MMBT2222A/SOT23/600mA/40
Q61 MMBT2222A/SOT23/600mA/40

VCC
D14 CD4148WP/1206/300mA
SPK- R425 75/4/1
R418 75/4/1
VCC R481 1K/4/1 Q77 MMBT2222A/SOT23/600mA/40
Q76 MMBT2222A/SOT23/600mA/40
Q85 MMBT2222A/SOT23/600mA/40
R482 8.2K/4
R480 1K/4/1
S0T23 S0T23
BEEP- BEEP- 25
SPKR SPKR 20

INTEL FRONT PANEL

PWR_LED
MPD+
PH/1*3/BK/2.54/VA/D

3 PIN POWER LED
LAYOUT PLACE CLOSE
TO F_PANEL

VCC
R363 330/6
BC128 0.01u/4/X7R/25V/K/X
F_PANEL
HD+
33 -HDLED -HDLED
5VSB R396 8.2K/4/X
R400 0/4/SHT/X
6,20,23,30 -SYS_RST
Q72
BAT54C/SOT23/200mA/[10DK1-200054-14R]/X

HD+ MSG/PD+ MPD+
HD- MSG/PD-
GND PW+
RESET PW-
RSV
GD+ SP+ VCC
GD- NC
GN+ NC
GN- SP- SPK-

BH/2*10K10,11,12,13,15,17,19/BK/2.54/VA/PA/[]11NH3-000210-B1R_11NH3-000210-B2R

VCC
R360 330/6
MPD+
Q51 MMBT2222A/SOT23/600mA/40
S0T23
R352 1K/4/1
GPIO28 20

5VSB
R385 8.2K/4
R382 33/4
-PWRBTSW -PWRBTSW 25
C196 0.01u/4/X7R/25V/K
Q65 BAV99/SOT23/300mA
5VSB

USB POWER

FUSEVCC1
F1
SMD1812P260/6V
EC2
560u/FP/D/6.3V/89/8m
160MILS
320MILS
5VDUAL
F2
FUSEVCC
EC1
SMD1812P260/6V
560u/FP/D/6.3V/89/8m
BC2
0.1u/4/X7R/16V/K

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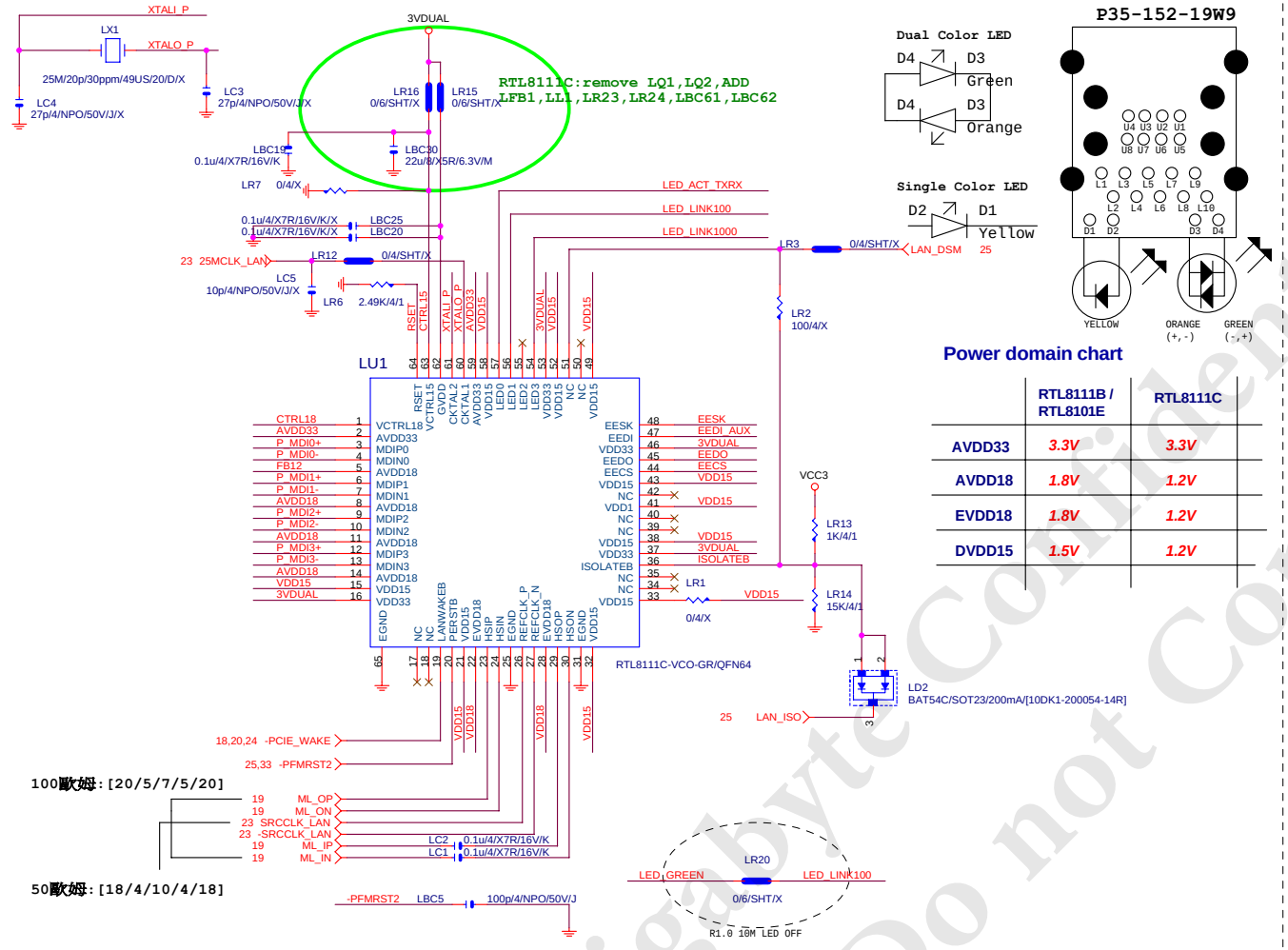
PCIE-1G LAN



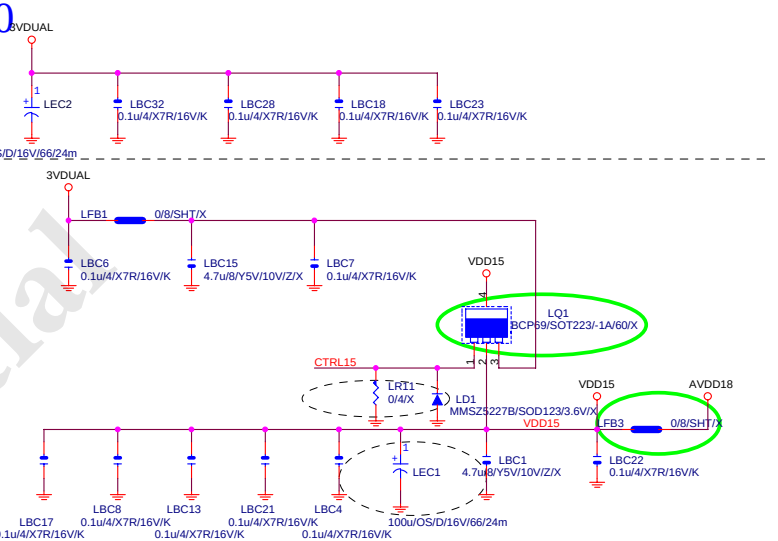
Dual Color LED

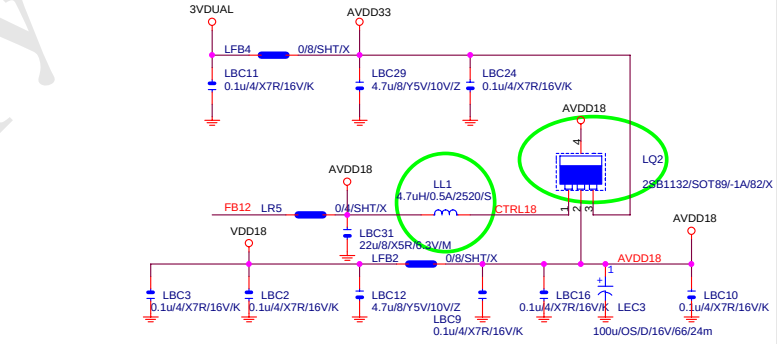
Single Color LED

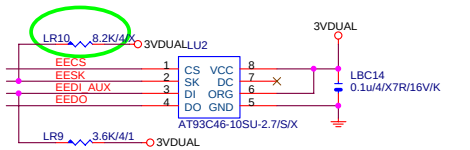
P35-152-19W9

Power domain chart

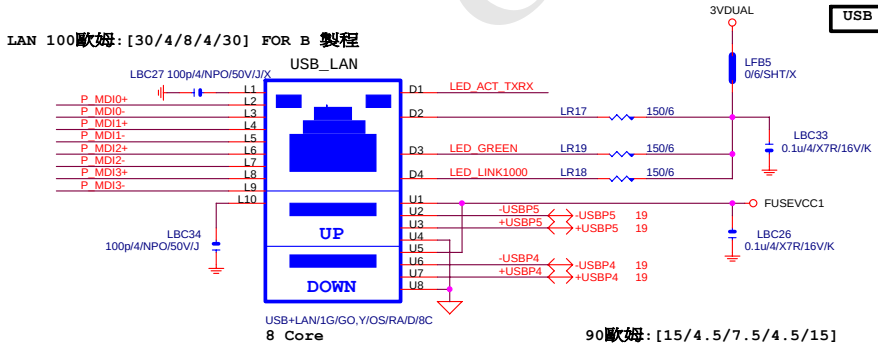
	RTL8111B / RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
DVDD15	1.5V	1.2V





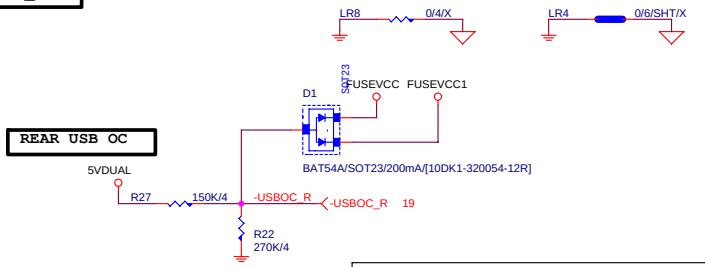


USB_LAN CONNECTOR



USB POWER

USB_LAN



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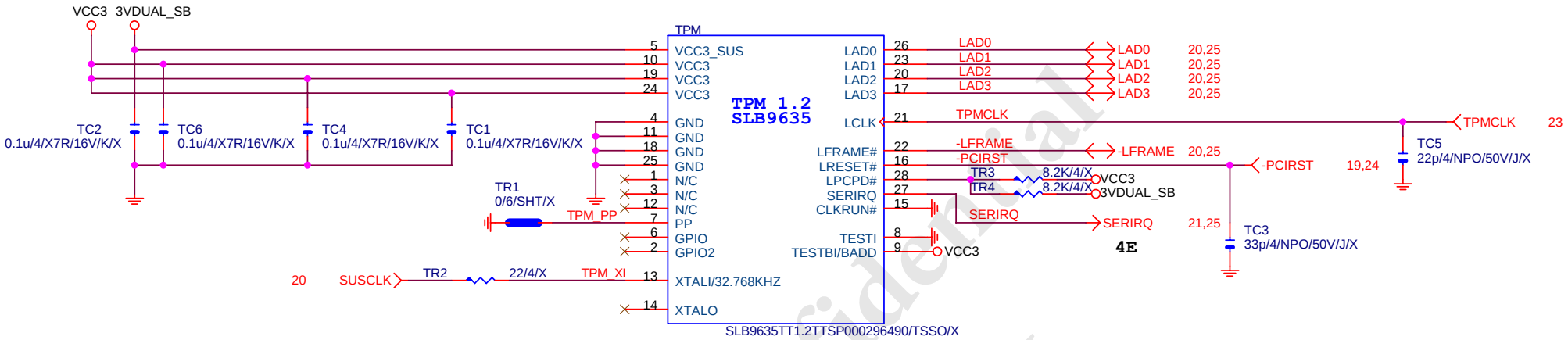

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