Model Name:GA-EP43-UD3L REV 1.2

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SHEET	TITLE
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29	AUDIO JACK
30	VCORE PWM ISL6334CRZ
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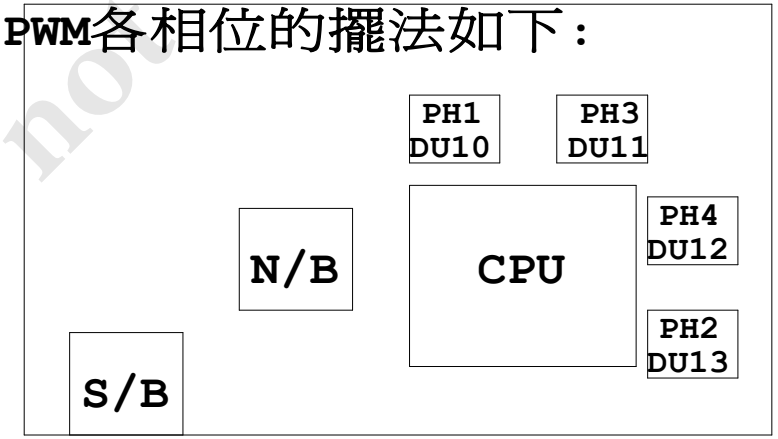
32	ATX POWER
33	JMicron JMB368
34	LAN REALTEK RTL8111C
35	FRONT PANEL,FUSB,FDD
36	TPM I/F-1.2

PWM各相位的擺法如下：



Gigabyte Technology

Title: Cover Sheet

Size: Custom | Document Number: GA-EP43-UD3L | Rev: 1.2

Date: Tuesday, December 01, 2009 | Sheet 1 of 36

Model Name: GA-EP43-UD3L
Rev:.1.2

Component value change history

Data	Change Item	Reason
97/04/01 EBOM:01A	1. P43 CHIPSET E-BOM	
97/04/15 EBOM:02	1. 修改LED的OWER及阻值;DEL R484,DR78. ADD DR79,,R348	
	2. ADD DR80,R300 10-->49.9,C158,LBC43 0ohm-->100PF for EMI	
	3. del Q3,Q4,BC11,BC9,R42,R15,PCI_BT1,PCI_BT2,R166,R168	
97/04/28 EBOM:10A	1. DDR2 VOLTAGE 1.83 --> 1.9V --> 2.0V --> 2.1V .....-->2.5V	
97/05/09 PBOM:10B	1. DR59,DR60 14K---->549ohm,del DR69	
	2. ADD U9(uP6262),R436,BC133 FOR CPU 超頻	
97/05/21 PBOM:10C	1.ICH,MCH PCI-E ,JM368的RX,TX串電容BOM 0.1U/Y5V-->0.1U/X7R,RTC RTCVDD -->X7R	
	2.ADD U6 FOR DDR TURN ON 2.1V ISSUE	
97/06/4 PBOM:10D	1.DEL Q107,R620,ADD R621	
	2.Q49(BAT54C) 限用 DII	
97/06/18 PBOM:10E	1.ADD MB_ID R283,DEL R282,Q87,Q91,R452,R498,R499,R500 FOR VTT_GMCH 1.2V	
	2.C197 0.1U/Y5V--->X7R	
	3.R300 49.9--->100 ohm ,C158 Y5V--->X7R for USB	
	4.DC20 0.01u--->1nf FOR CPU PSI ISSUE	
97/08/07 EBOM:20A	1.CPU 改爲SMART FAN	
	2.L4,L7 CHOKE Footprint Change "CHOKE1U2-20A-1PQN"	
	3.獨立南橋1.1V 的電壓	
	4. ADD GPIO37 FOR LOAD LINE CALIBRATION	
	5.J368 改爲1.8V;R209=100 OHM, ADD R640 FOR MB_ID2	
97/08/08 EBOM:30A	1.J368 改爲1.8V;47--->44.2 2.TO252---改爲POWER PACK	
97/10/01 PBOM:10A	FOR EP45-UD3L-1.0	
	1.R183 18K-->9.09K;R184 9.76K--->4.3K 2.DR56 1.74K-->1.87K;DR81 1K--->590 OHM	
	3.DR38 487--->549 ohm 4.R369 2.26K--->1.5K;R378 13.7K--->15.8K	
	4.NB,SB CHANGE HEAT SINK for UD series; PCIEX1 SLOT改爲白色	
	5.RQ3 由BJT改爲 BAT54A FOR -HDLED ISSUE	
97/11/17 EBOM:10A	FOR EP43-UD3L-1.0 1.P43 CHIP,HEAT SINK,UPI	
97/12/05 PBOM:10B	1.P-BOM,修改HEATSINK,調整部份阻值	
98/02/24 PBOM:10C	1.100UF 統一料號	
98/03/26 PBOM:11A	1.僅變更NB,SB heatshink料號金色改灰色	
98/05/13 PBOM:11B	1.Backup bios R56 pull-high 1k--->330 ohm; 移除SST BIOS	
98/11/06 EBOM:12A	1.FOR GA-EP43-UD3L-1.2	98/12/01 PBOM:12A 1.FOR GA-EP43-UD3L-1.2,轉P-BOM ADD PACKAGE

Circuit or PCB layout change for next version

DATE	Change Item	Reason
97/04/01 PCB:0.1	1.P43-DS3L	
97/04/23 PCB:1.0	1. CE3位置請移至EC24左邊	
	2. 增加 upi6262 VCC Power (R620,R621,Q107)	
	3. 增加R622,R623 FOR DDR18V_OV3	
97/07/23 PCB:2.0	1.由1.0 修改,直接改成2.0	
	2.PCIEX16 和PCIEX1_2對調位置	
	3. DDR2_1~DDR2_4往左移,盡量讓MCH的位置在DDR SLOT中間	
	4.ADD CPU SMART FAN CONTROL	
97/07/23 PCB:3.0	1.由2.0 修改	
	2. cpu Vcore MOS TO252改爲POWER PACK	
97/09/16 PCB:1.0	1.由3.0 修改,改文字面 EP45-UD3L ,ULTRA DURABLE 3,NB /SB 框內文字修改	
97/11/06 PCB:1.0	1.由EP45-UD3L改文字面成EP43-UD3L	
	2.DEL ICH CORE 1.1線路,NET DDR18V_OV2與LAN_DSM互換FOR DDR超壓ISSUE	
	3.UPDATE LL1 ,LGA775 FOOTPRINT	
98/03/27 PCB:1.1	1.TO CHANGE PCB VERSION FOR 1.1	
98/11/04 PCB:1.2	1.add EUP function,audio co-lay 892	

Gigabyte Technology

Title: BOM & PCB MODIFY HISTORY

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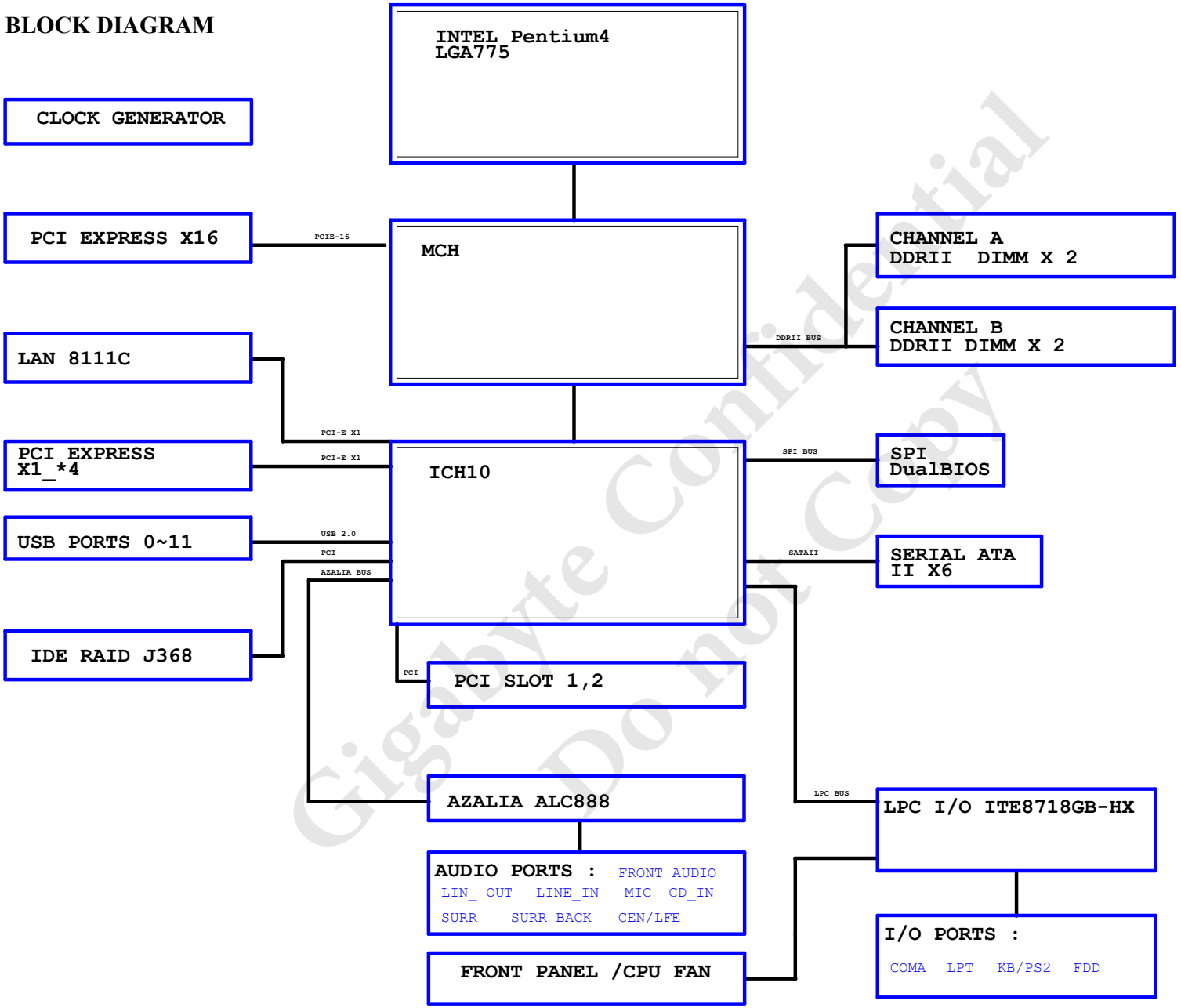
BLOCK DIAGRAM



Gigabyte Technology		
Title: BLOCK DIAGRAM		
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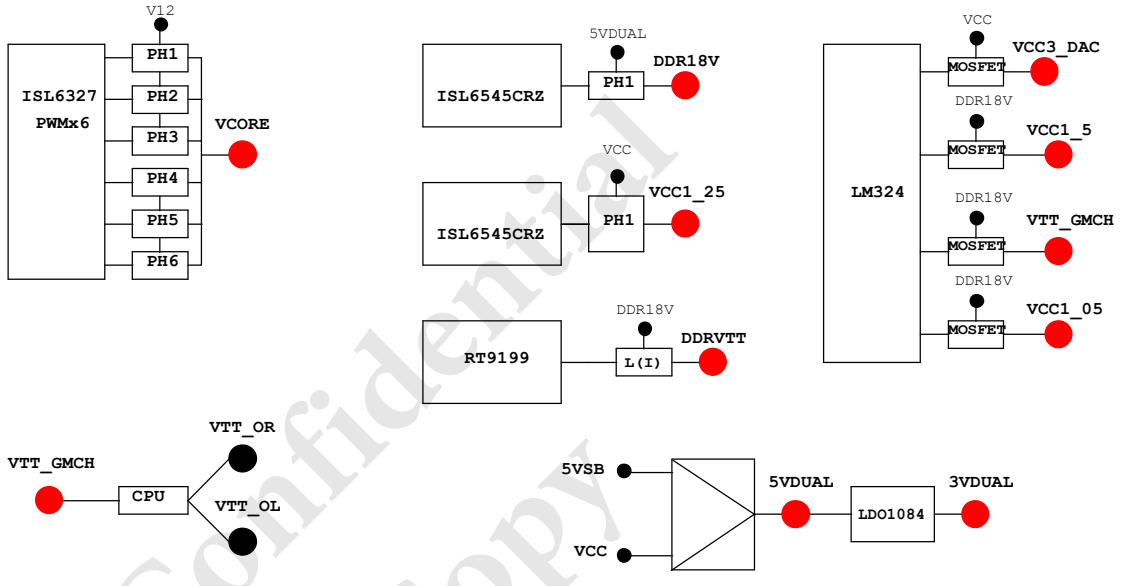
ICH8 GPIO LIST TABLE

PIN NAME	PWR WELL	AFTER/ PLTRST	USAGE	NOTE
GP0	MAIN	IN	-ACZ_DET	P/U 8.2K VCC3
GP1/TACH1	MAIN	IN	ICH_FAN_TACH1	P/U 8.2K VCC3
GP2/PIRQE#	MAIN	IN	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN	IN	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN	IN	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN	IN	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN	IN	ICH_FAN_TACH2	P/U 8.2K VCC3
GP7/TACH3	MAIN	IN	ICH_FAN_TACH3	P/U 8.2K VCC3
GP8	STBY	IN	GPIO8(DUALBIOS_INPUT)	P/U 8.2K 3VDUAL
GP9	STBY	OUT	WOL_ONLY	P/D 100K GND
GP10	STBY	IN	CLGPIO1	P/U 8.2K 3VDUAL
GP11/SMBALERT#	STBY	OUT	-SMBALRT	P/U 8.2K 3VDUAL
GP12	STBY	IN	MB_ID0	P/U 8.2K 3VDUAL
GP13	STBY	IN	-LPCPME	P/U 8.2K 3VDUAL
GP14	STBY	IN	CLGPIO2	P/U 8.2K 3VDUAL
GP15	STBY	OUT	LAN_DISABLE(STP_PCI-)	N/A
GP16	MAIN	OUT/LOW	RESET	N/A
GP17/TACH0	MAIN	IN	ICH_FAN_TACH0	P/U 8.2K VCC3
GP18	MAIN	OUT	MB_ID1	P/U 8.2K VCC3
GP19	MAIN	IN	SATA1GP	P/U 8.2K VCC3
GP20	MAIN	OUT	-SPI_WP0	P/U 1K 3VCL
GP21	MAIN	IN	SATA0GP	P/U 8.2K VCC3
GP22	MAIN	IN	SCLOCK	P/U 8.2K VCC3
GP23	MAIN	OUT	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	OUT	CLGPIO0	P/U 8.2K 3VDUAL
GP25	STBY	IN	MB_ID2(STP_CPU-)	P/U 8.2K 3VDUAL
GP26/S4_STATE#	STBY	OUT	S4_STATE#	P/U 8.2K 3VDUAL
GP27	STBY	OUT/LOW	GPIO27(EL_STATE0)	P/U 8.2K 3VDUAL
GP28	STBY	OUT/LOW	PWR_LED(EL_STATE1)	N/A
GP29/OC5#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP30/OC6#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP31/OC7#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP32	MAIN	OUT	DUAL_BIOS	P/U 100K+1M VCC3
GP33	MAIN	OUT	DUAL_BIOS	P/U 8.2K VCC3
GP34	MAIN	OUT/LOW	GPIO34/SMB_RST	N/A
GP35	MAIN	OUT	SATACLKREQ#	N/A
GP36	MAIN	IN	SATA2GP	P/U 8.2K VCC3
GP37	MAIN	IN	SATA3GP	P/U 8.2K VCC3
GP38	MAIN	IN	SLOAD	P/U 8.2K VCC3
GP39	MAIN	IN	GPIO39	P/D 8.2K GND
GP48	MAIN	IN	GPIO48	P/U 8.2K VCC3
GP49	MAIN	IN	CPUPWROK	P/U 100 VTT_OL

VCORE:6 PHASE PWM--ISL6327CRZ



Gigabyte Technology			
Title: TABLE LIST			
Size: B	Document Number: GA-EP43-UD3L		Rev: 1.2
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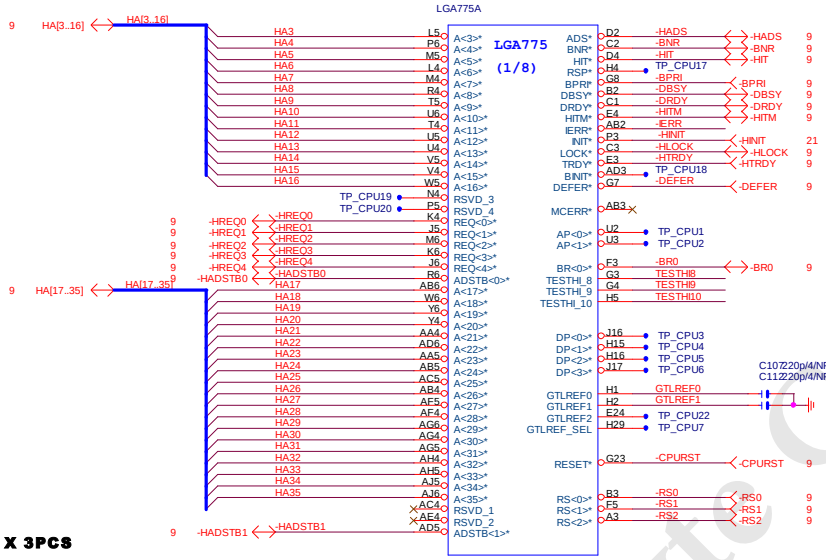
0.667 X VTT FOR LGA775 PIN H2/F2

0.635 X VTT FOR LGA775 PIN H1/G10

HA/REQ:50歐姆+-15% [4/11]

ADSTB:50歐姆+-15% [4/14]



SP-CAP X 3PCS

Impedance=50 +- 15% for 4 -layer

CPU GTLREF RATIO

GTLREF_UV0	GTLREF_UV1	Ratio Set
HIGH	HIGH	0.67
LOW	HIGH	0.65
HIGH	LOW	0.63
LOW	LOW	0.615

CR
CPU RETAINTION/X

Gigabyte Technology

Title: P4_LGA775-A

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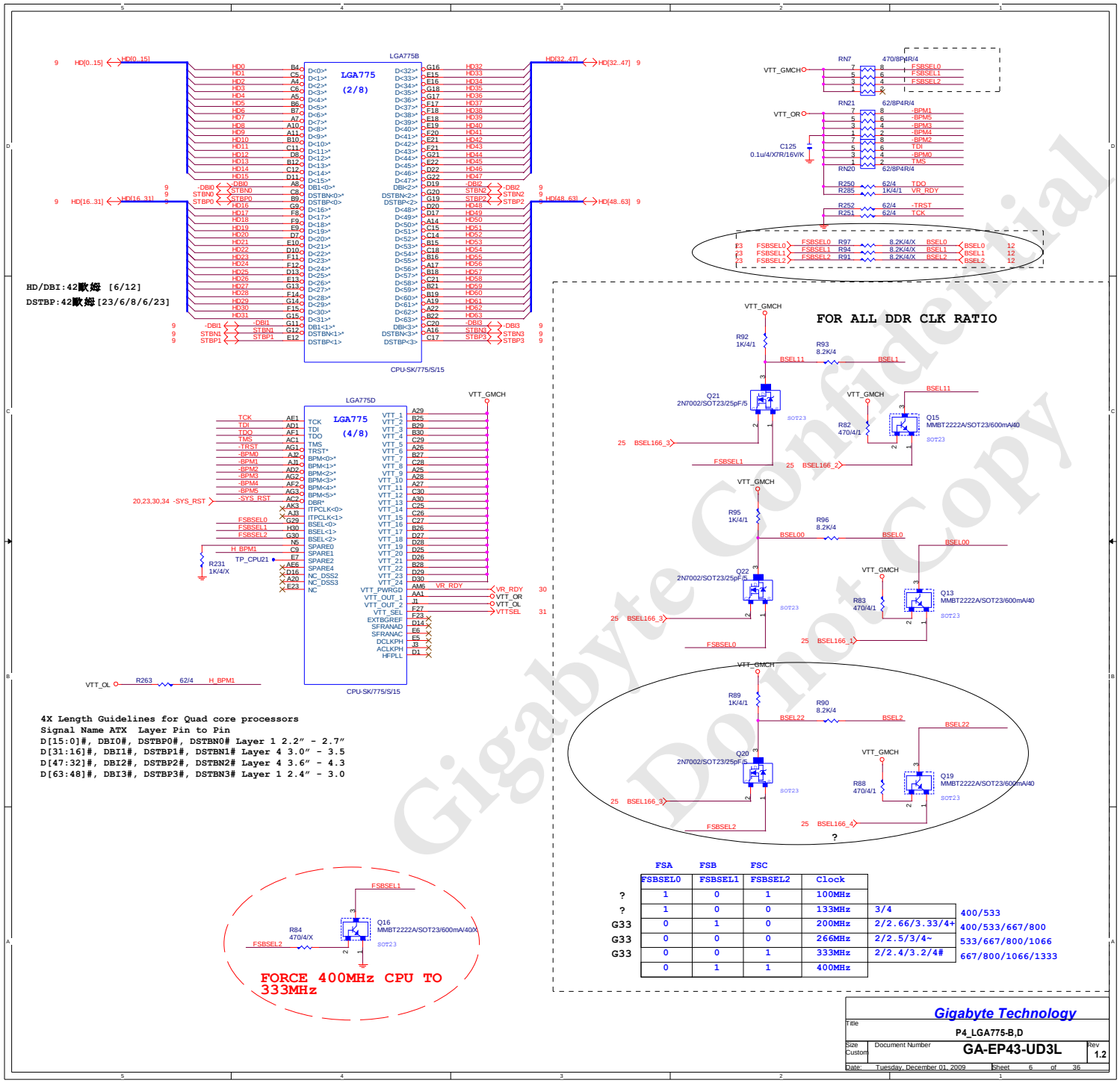

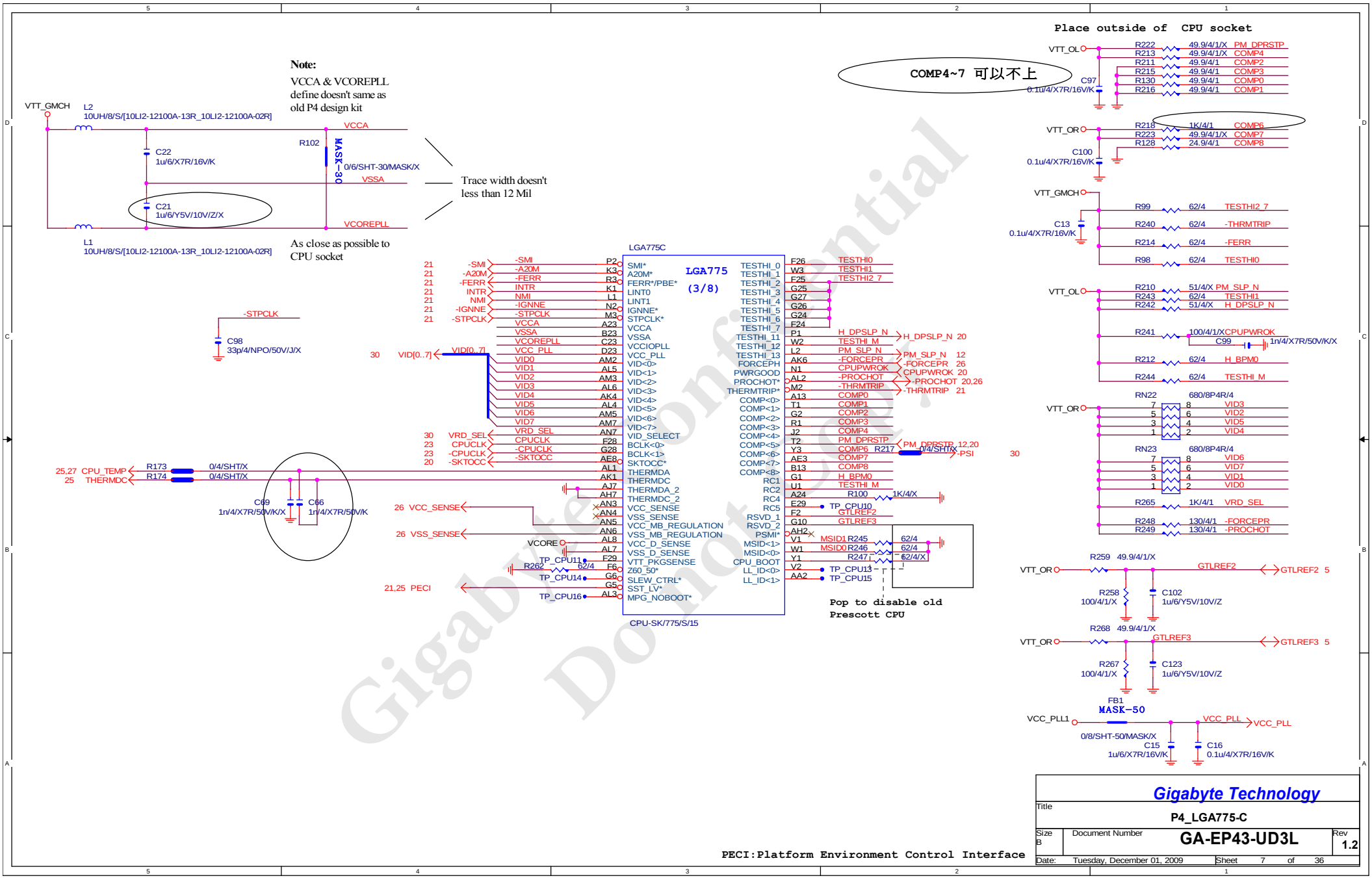

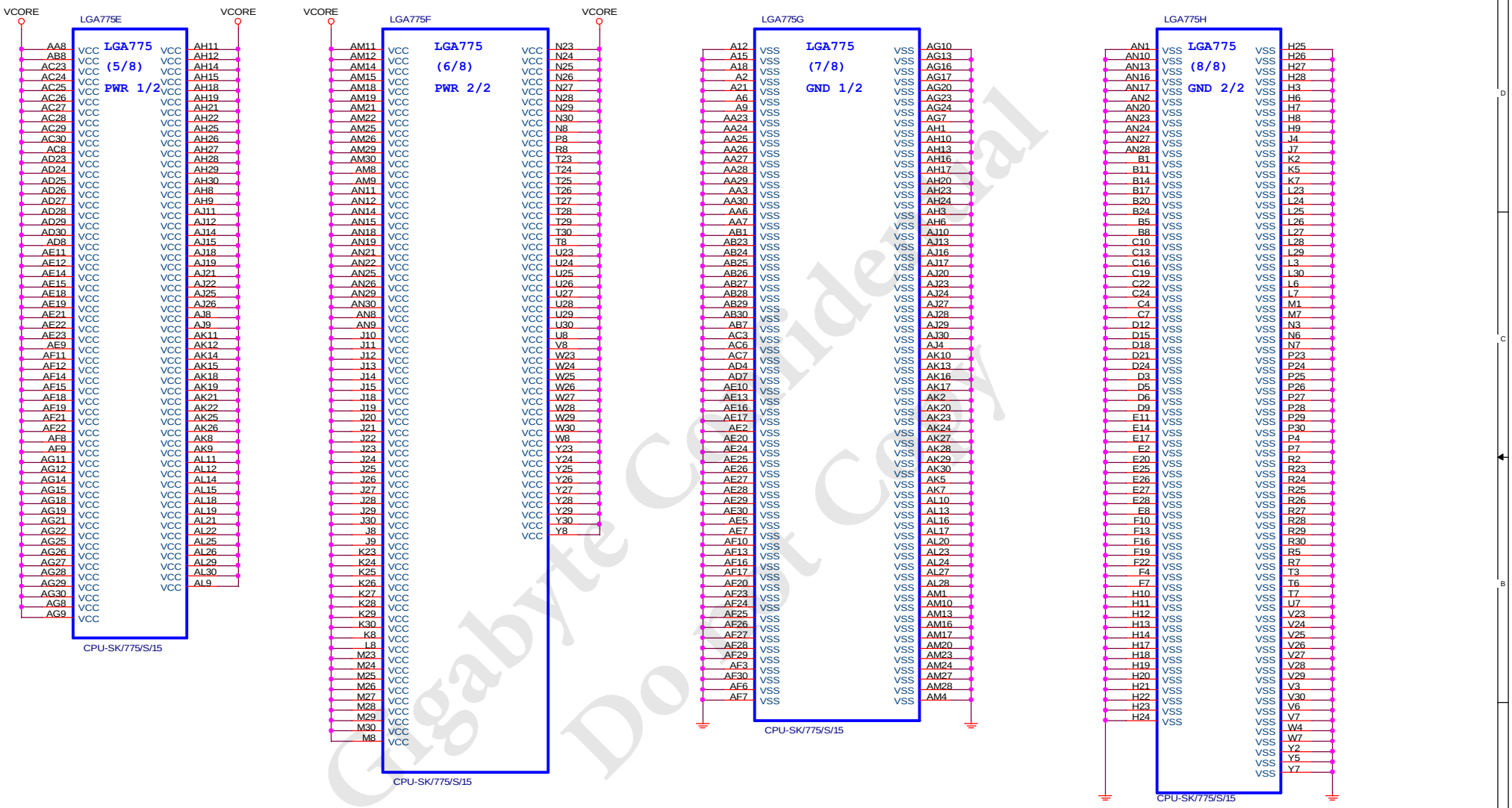

Gigabyte Technology		
Title	P4_LGA775-E,F,G,H	
Size B	Document Number GA-EP43-UD3L	Rev 1.2
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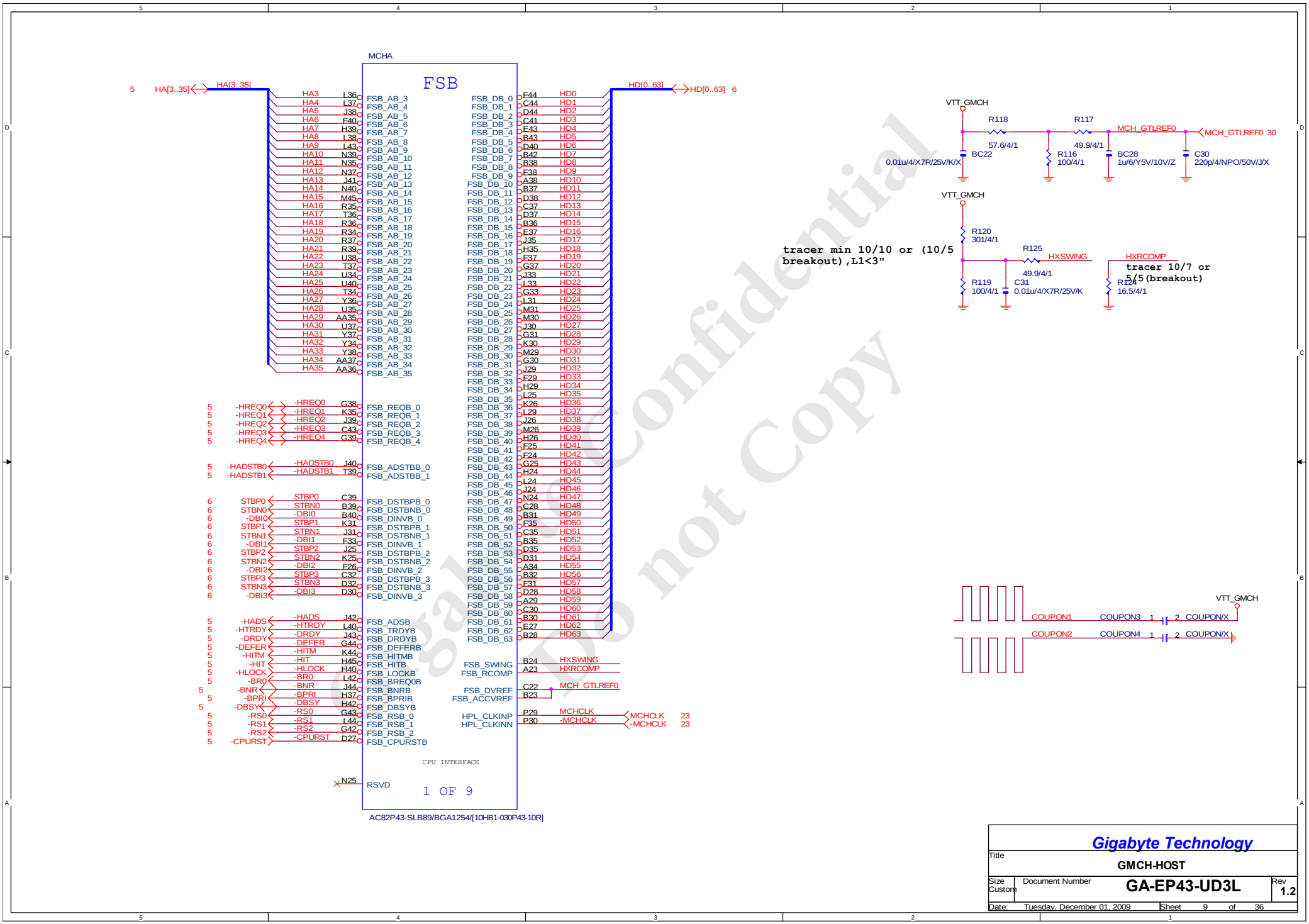
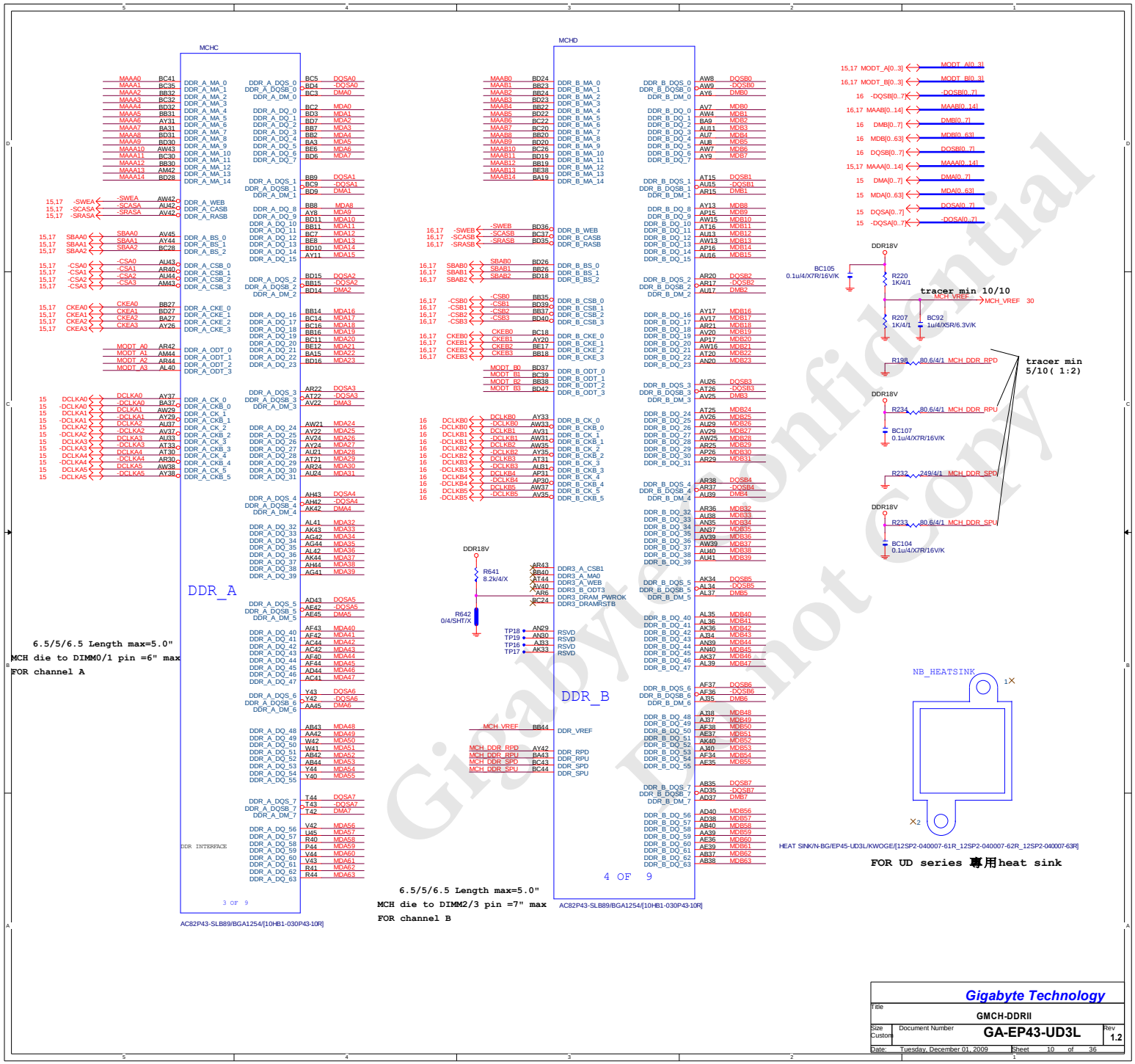
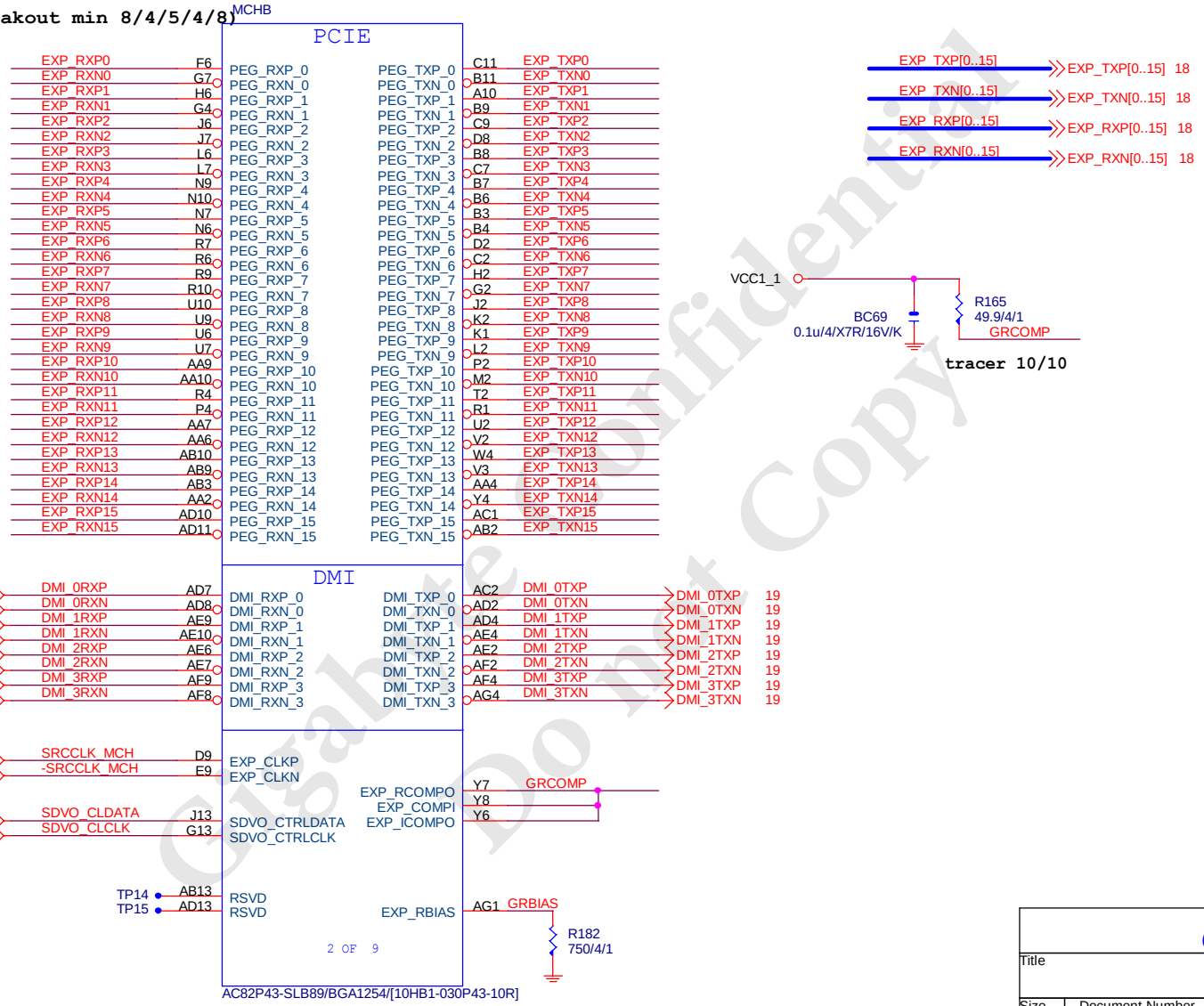




PCIEX16:16/5/5/5/16(breakout min 8/4/5/4/8)
Impedance=85 +- 17.5%

DMI:12/4/8/4/12
Impedance=95 +- 17.5%



Gigabyte Technology		
Title: GMCH-PCI E & DMI		
Size: Custom	Document Number: GA-EP43-UD3L	Rev: 1.2
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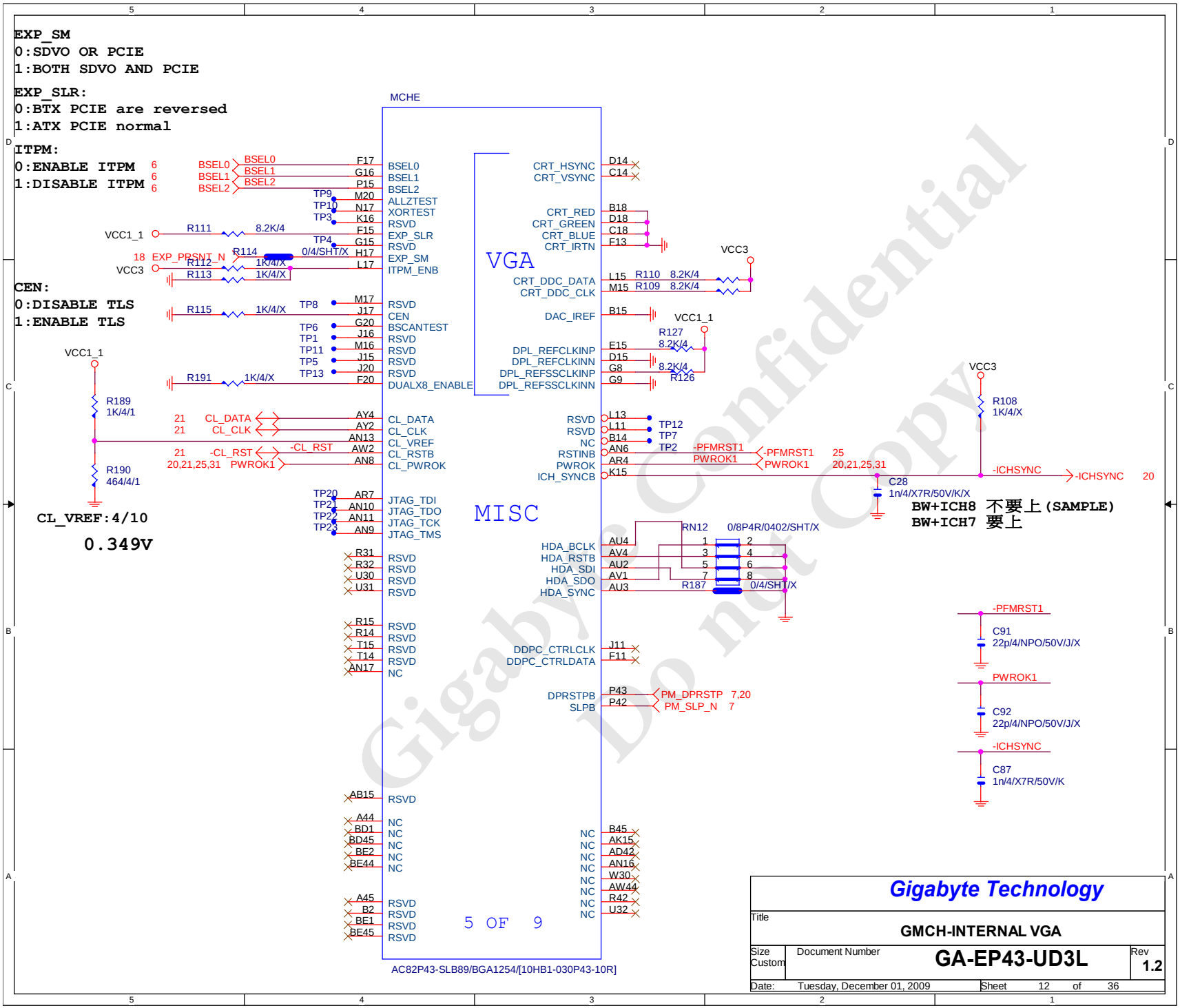
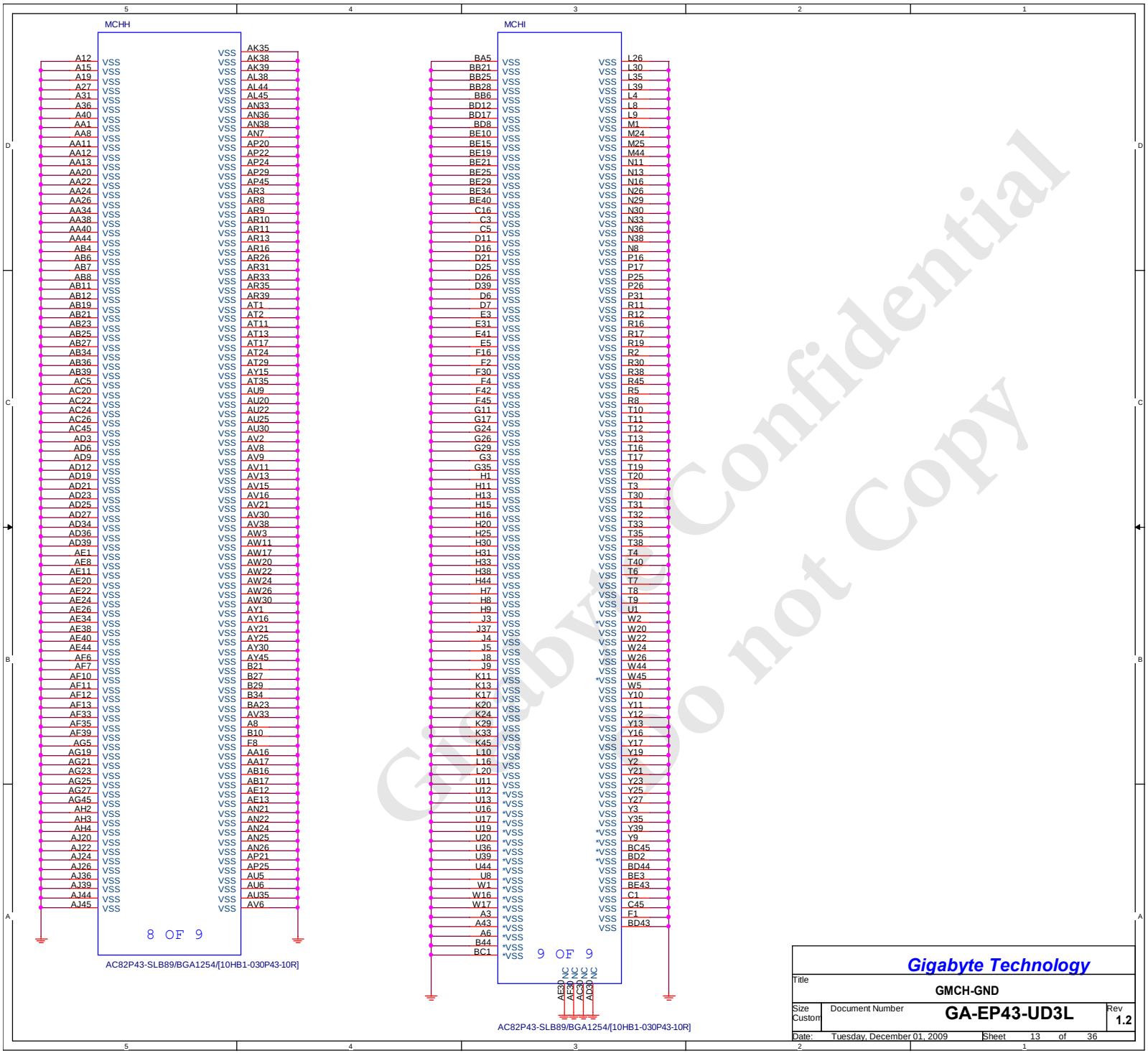
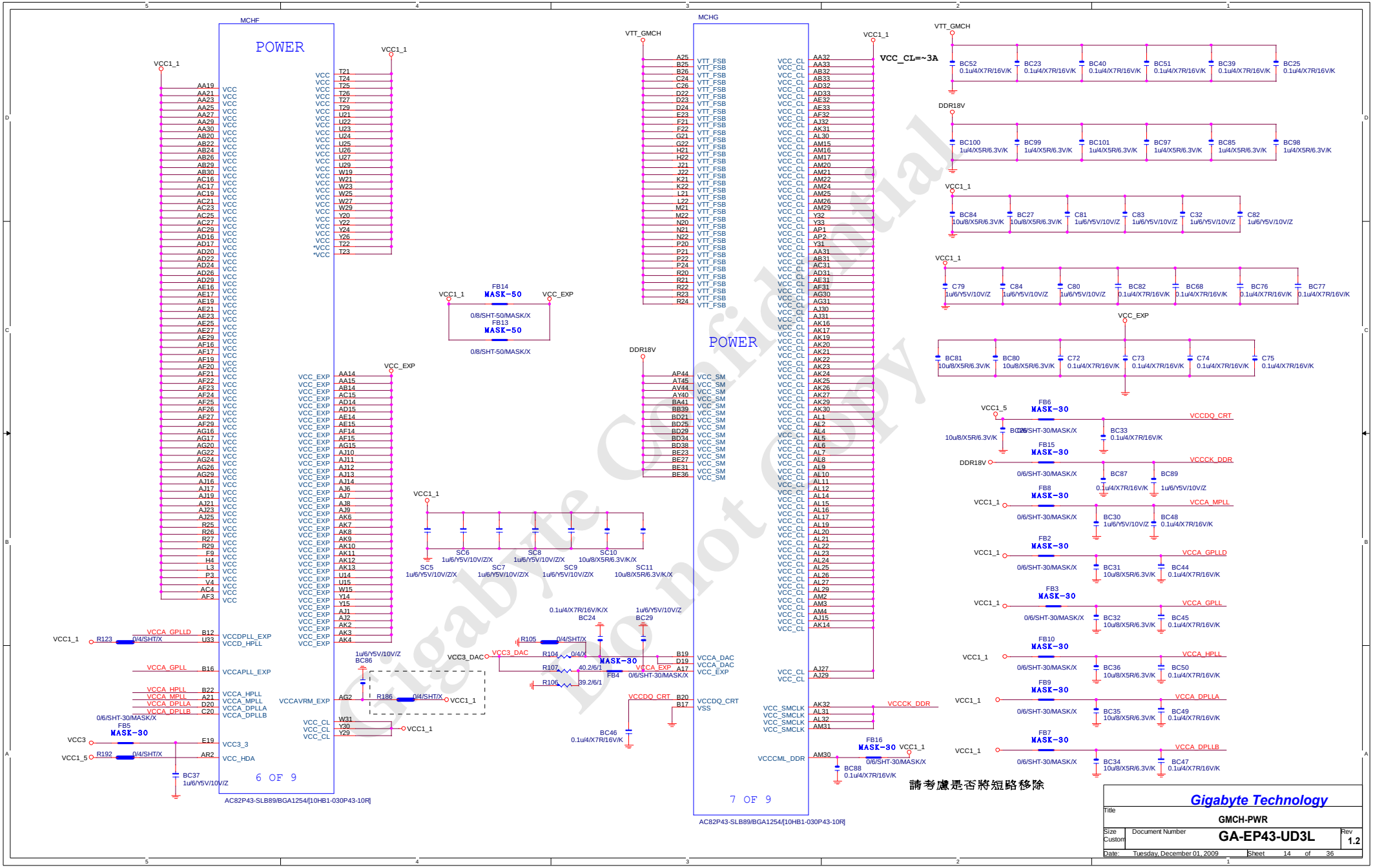
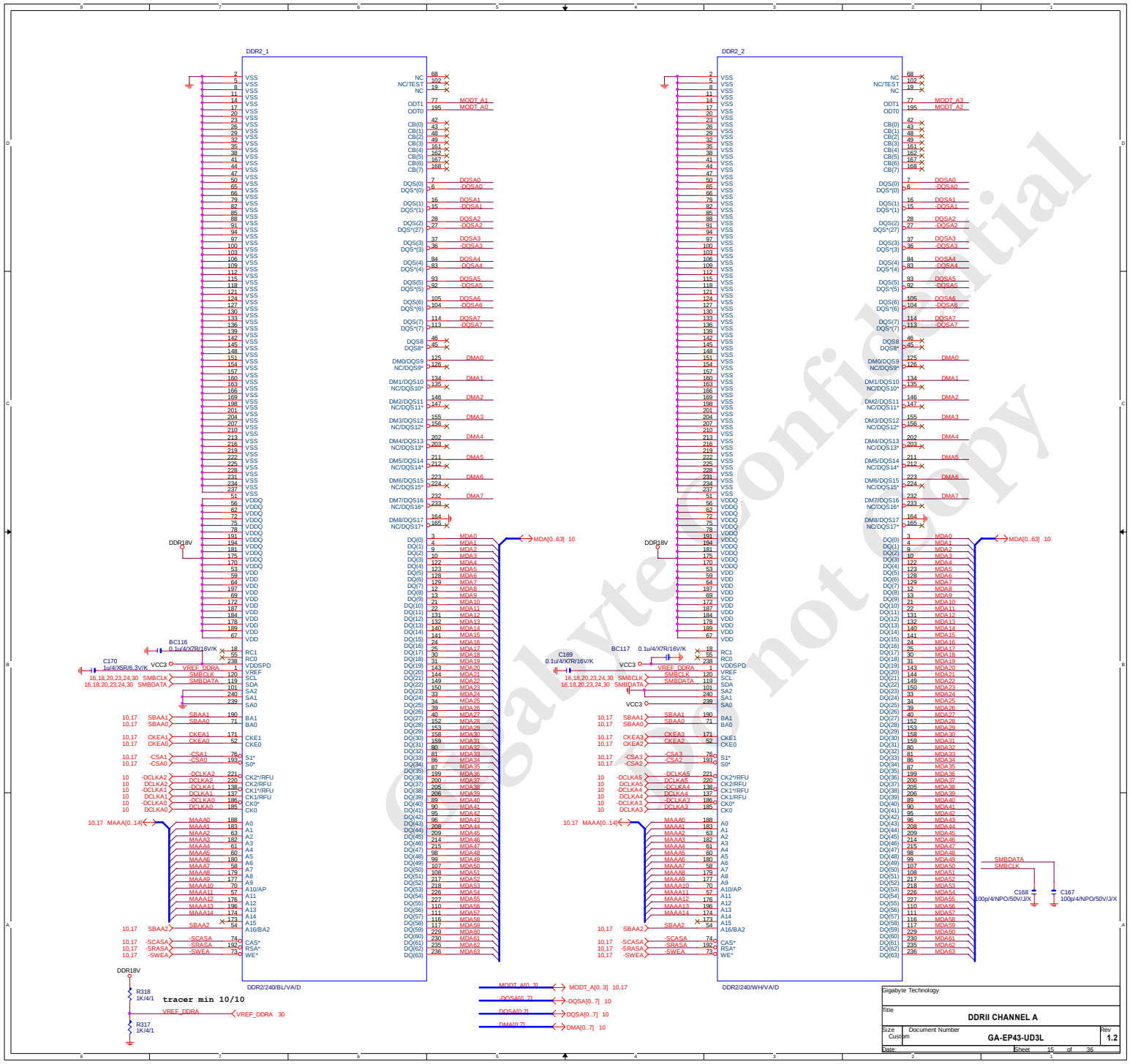
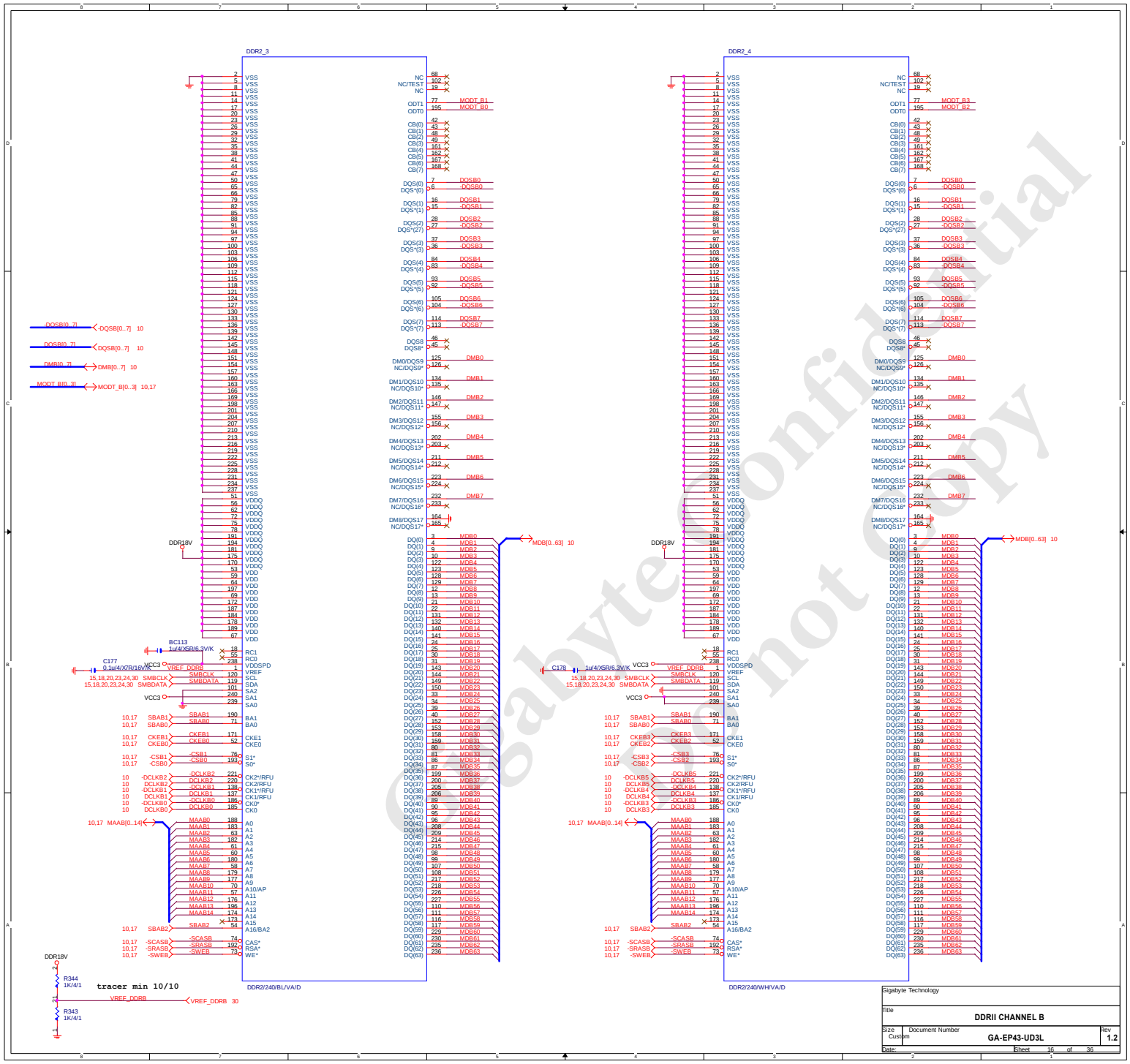




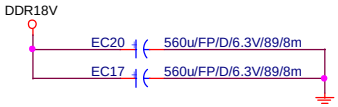


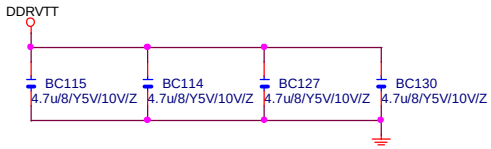




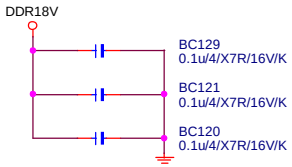
DDR TERMINATION CHANNEL A

DDRVTT Decouple





DDR18V Decouple



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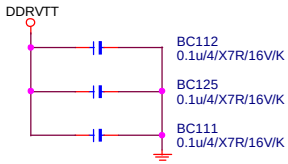
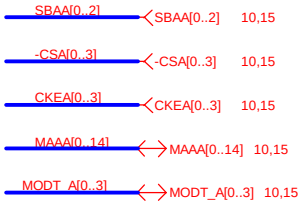
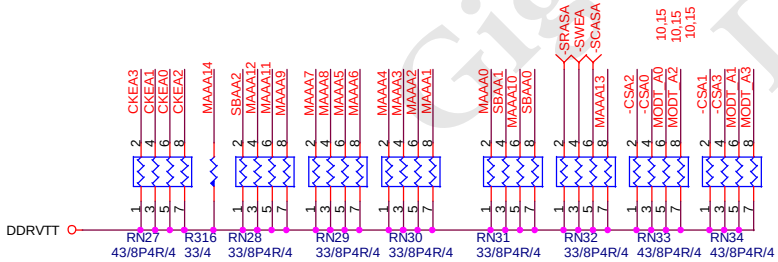
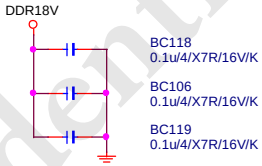




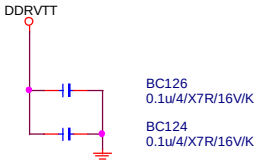


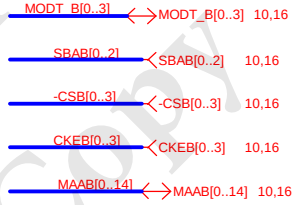
DDR TERMINATION CHANNEL B

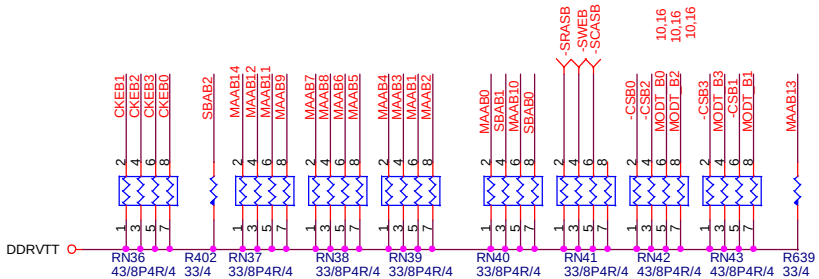
DDR18V Decouple



DDRVTT Decouple







Gigabyte Technology		
Title: DDRII TERMINATOR		
Size: Custom	Document Number: GA-EP43-UD3L	Rev: 1.2
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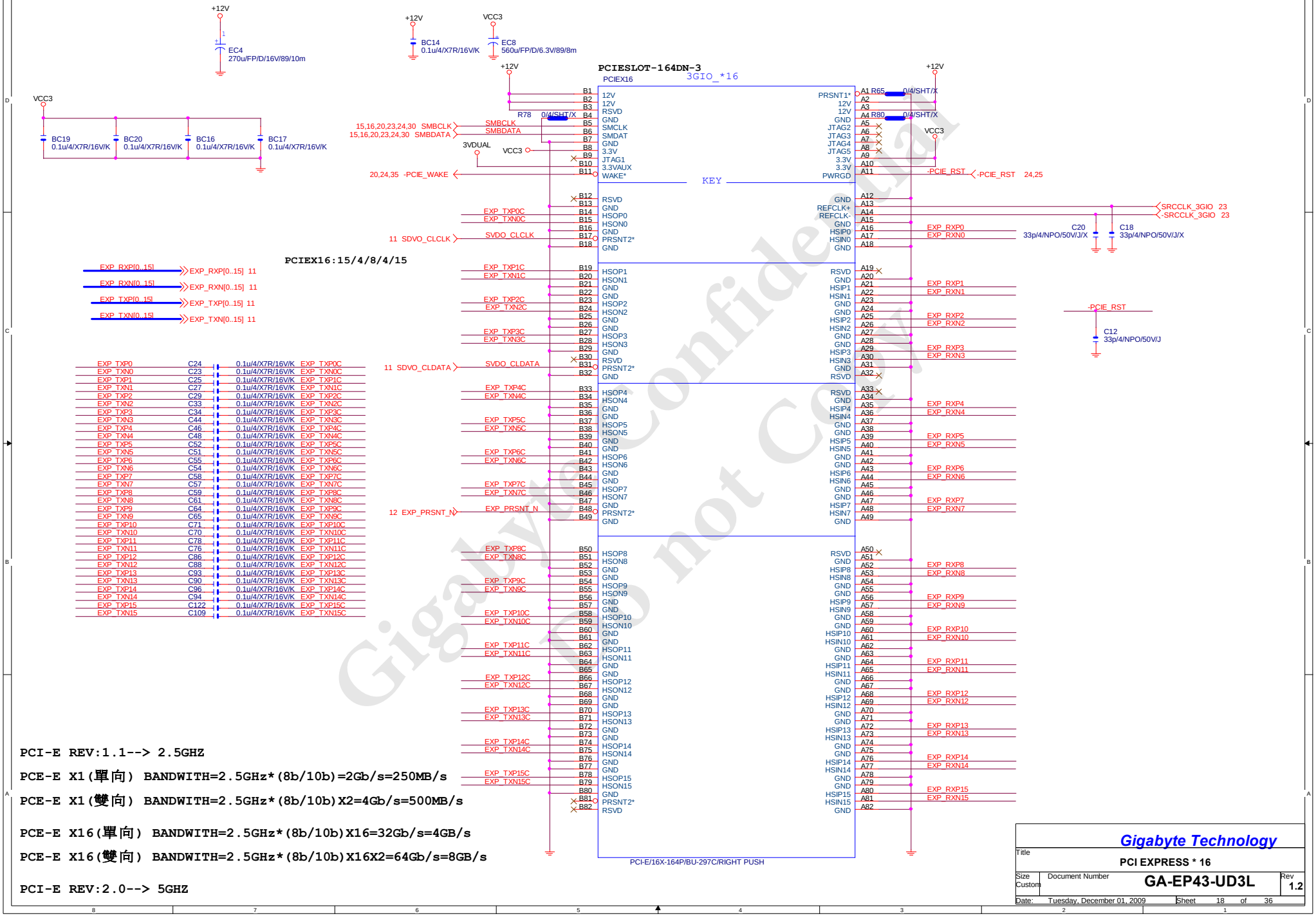
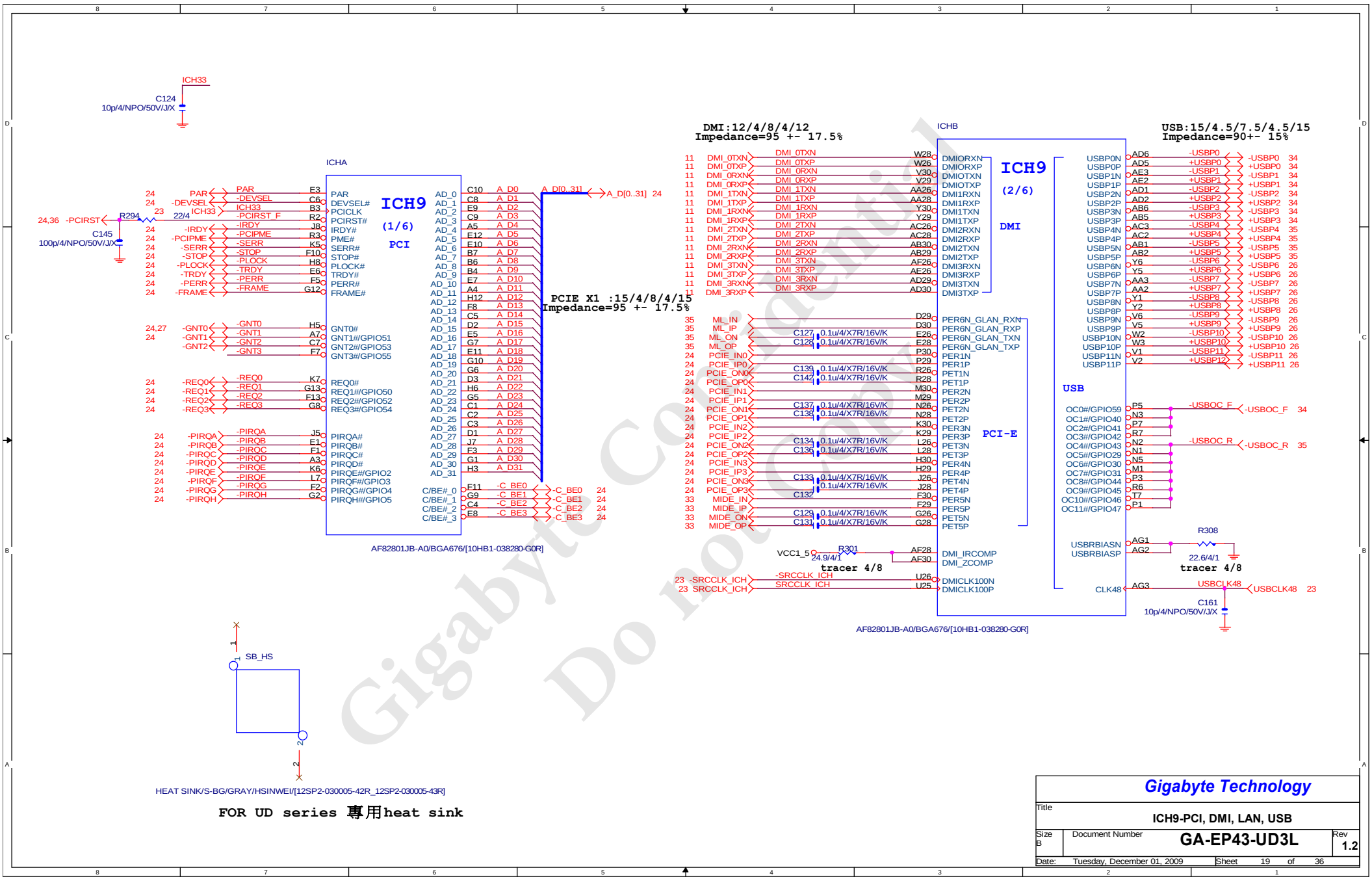
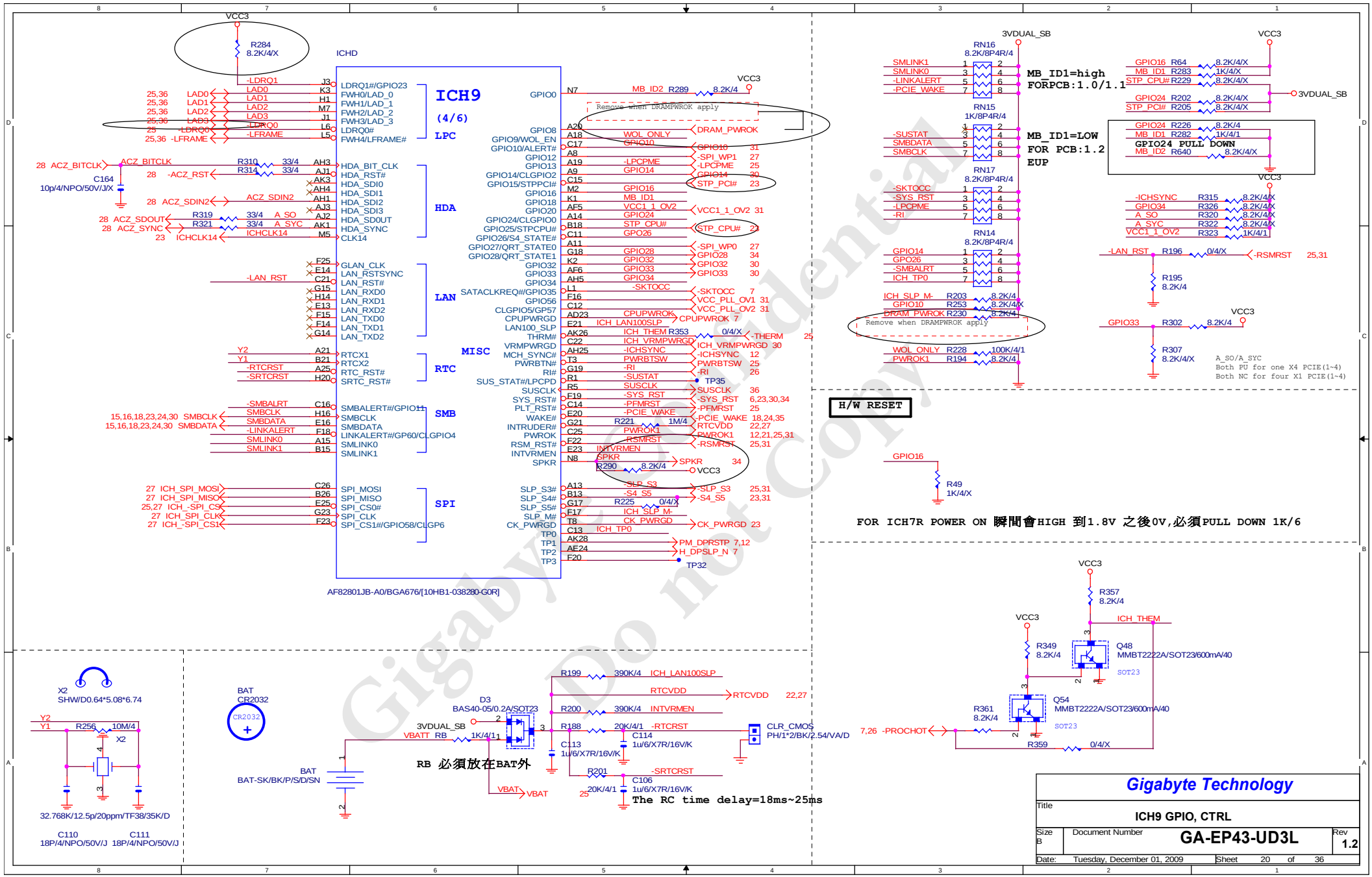
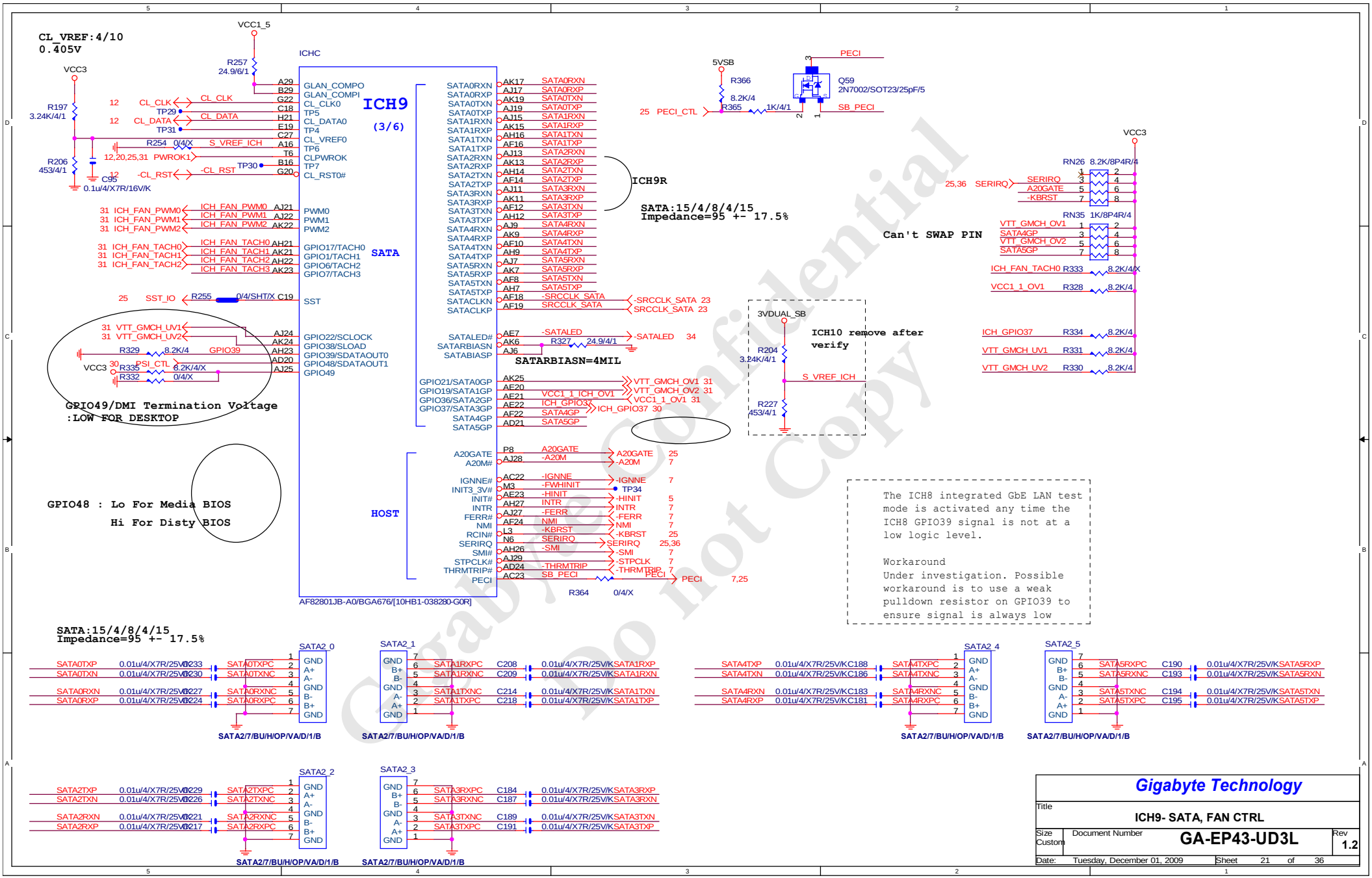
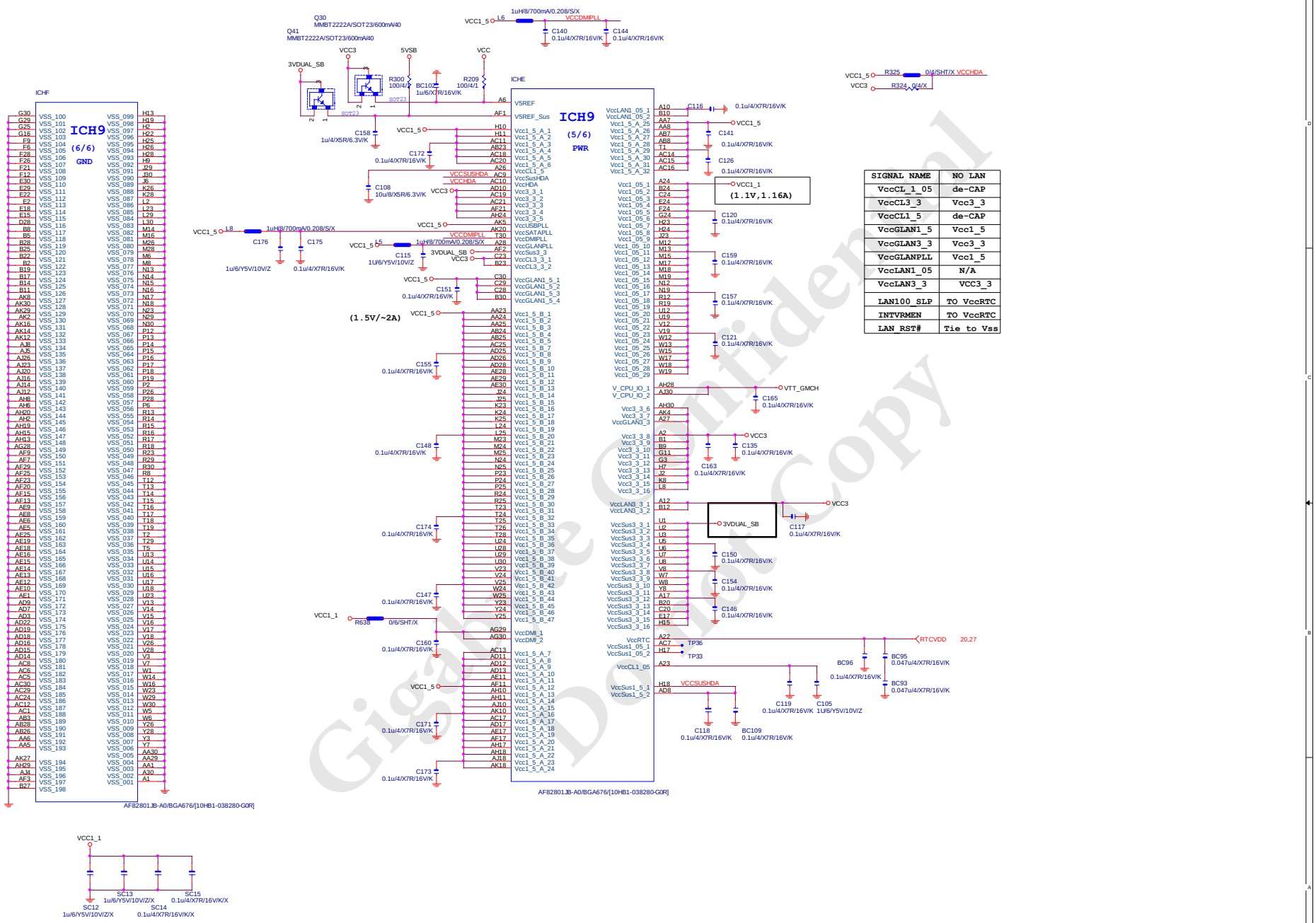
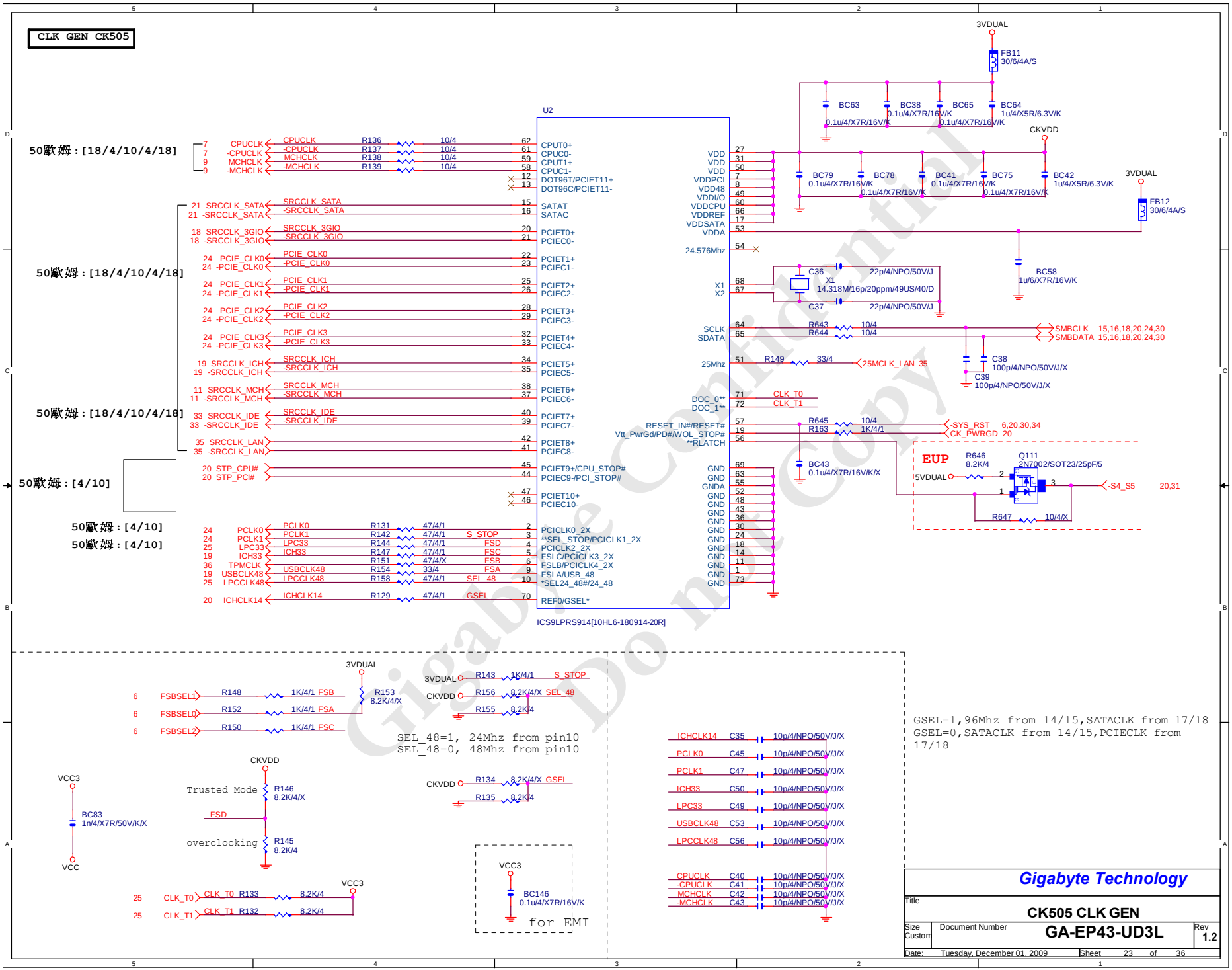


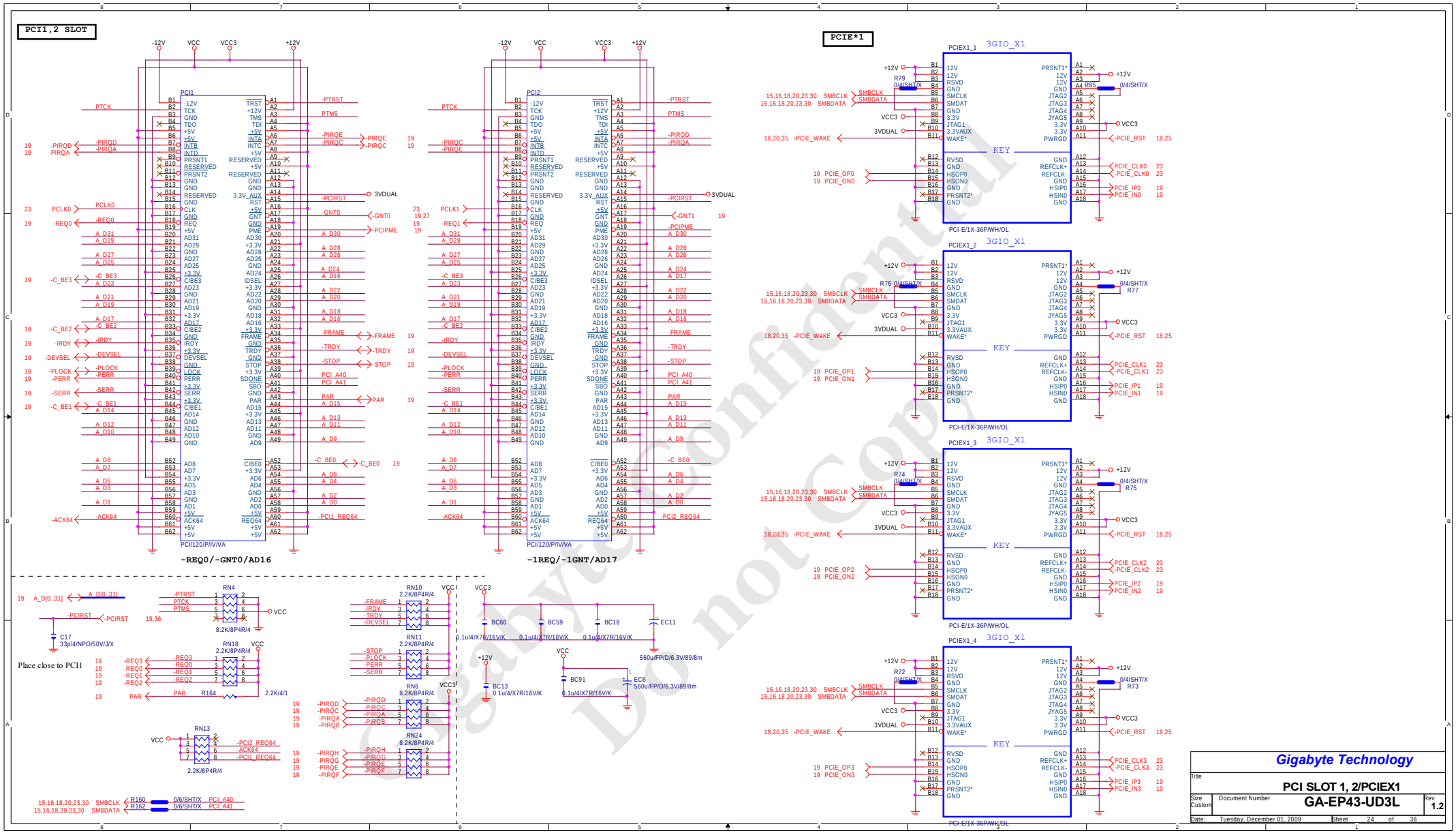


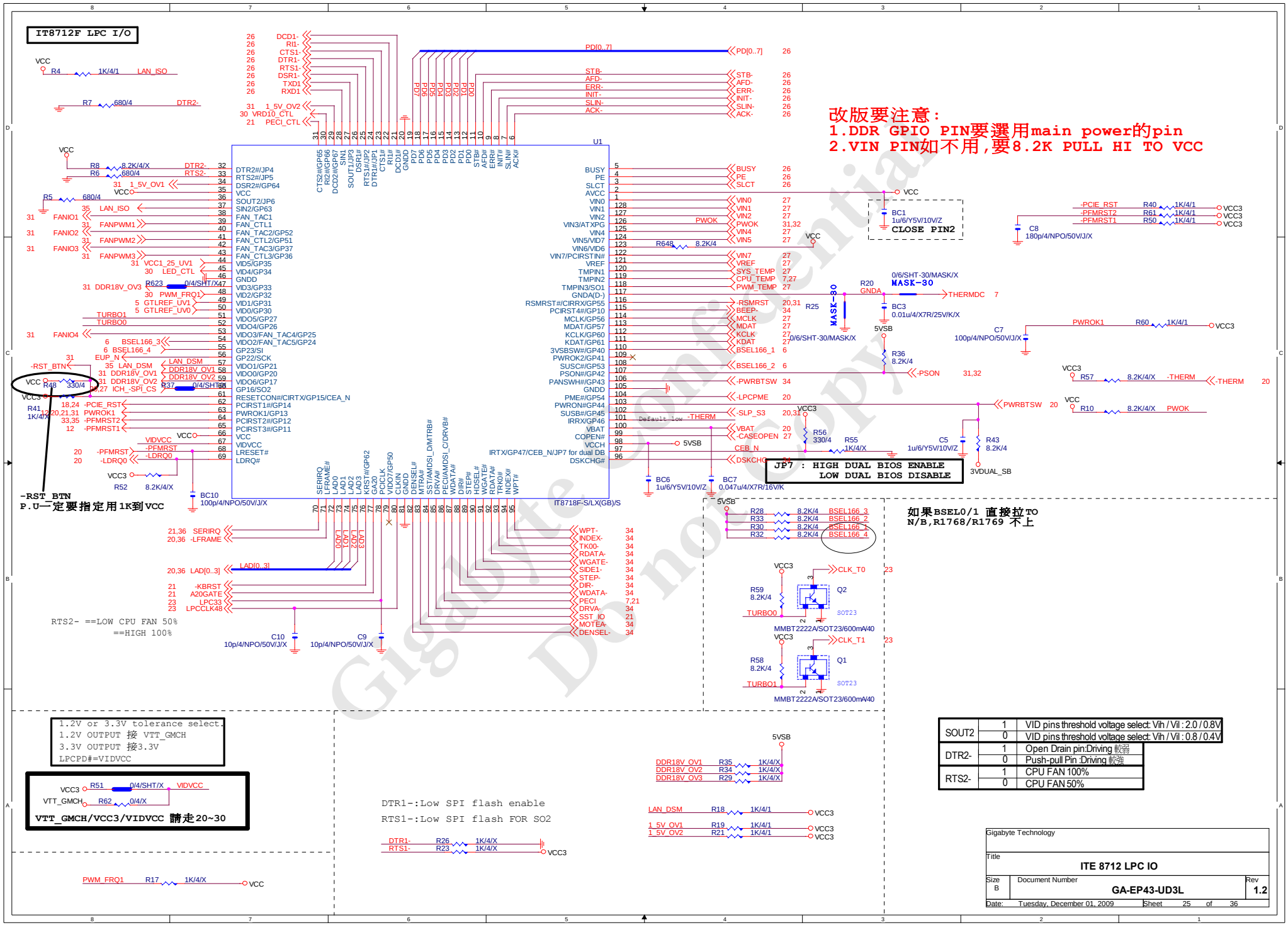


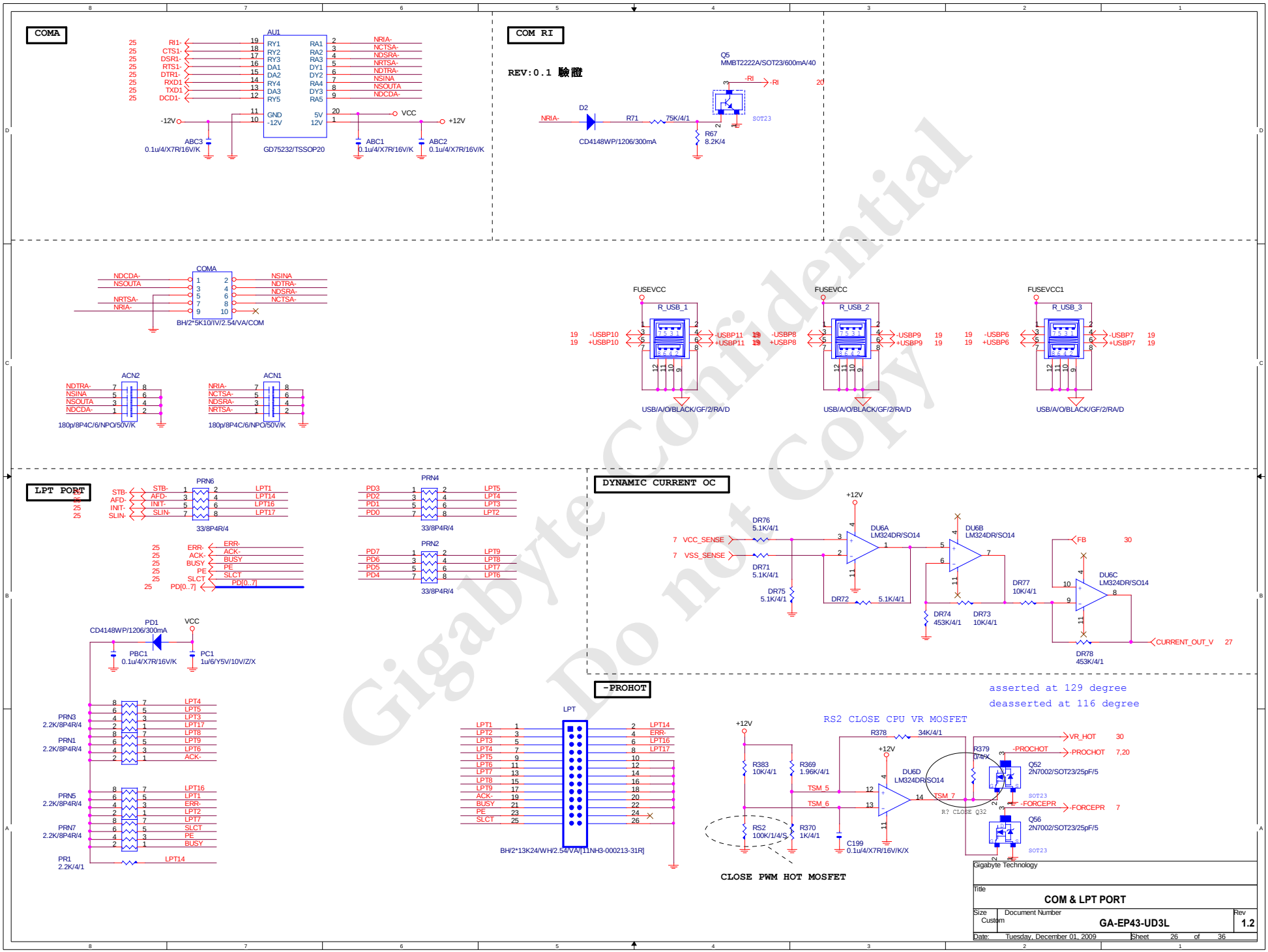


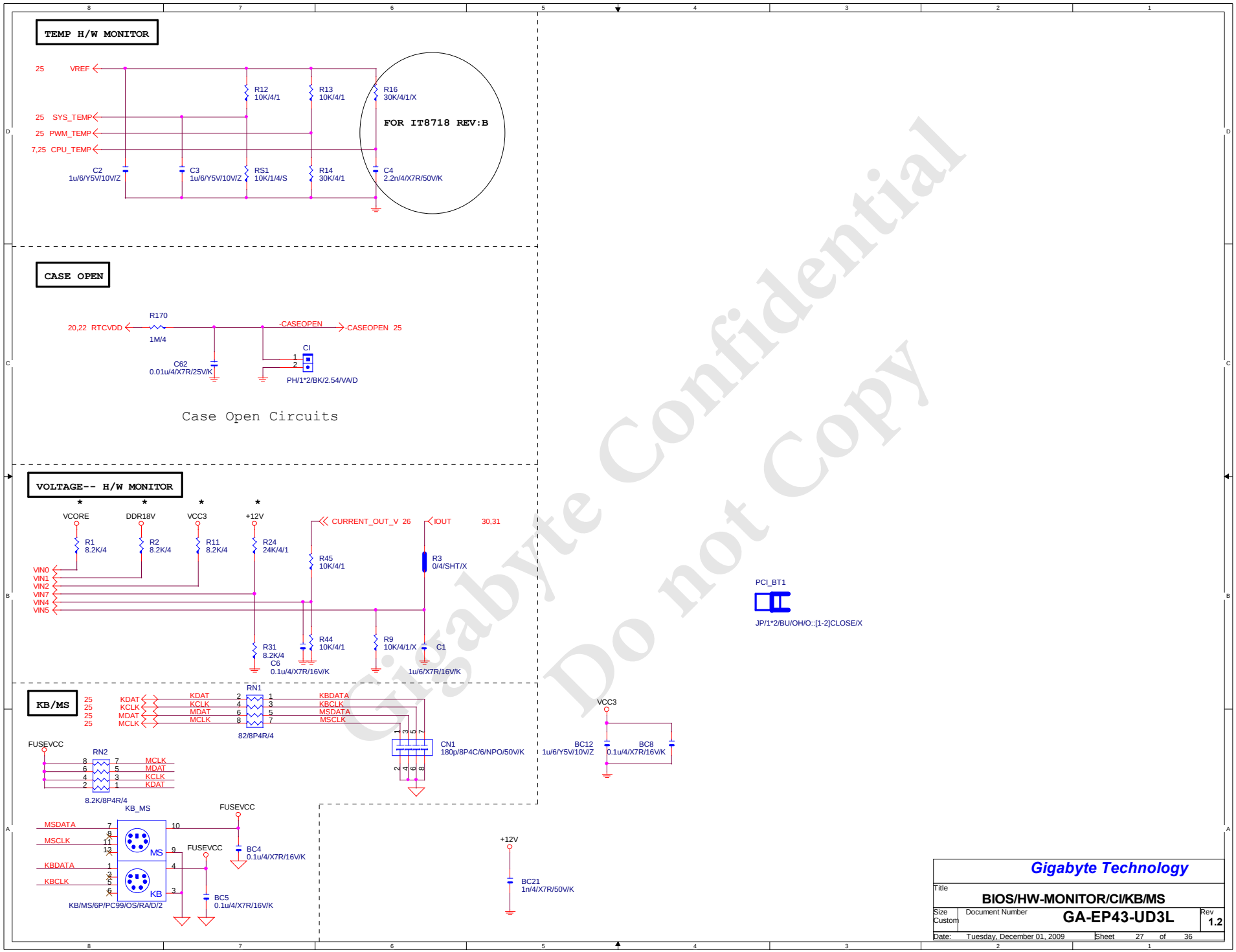










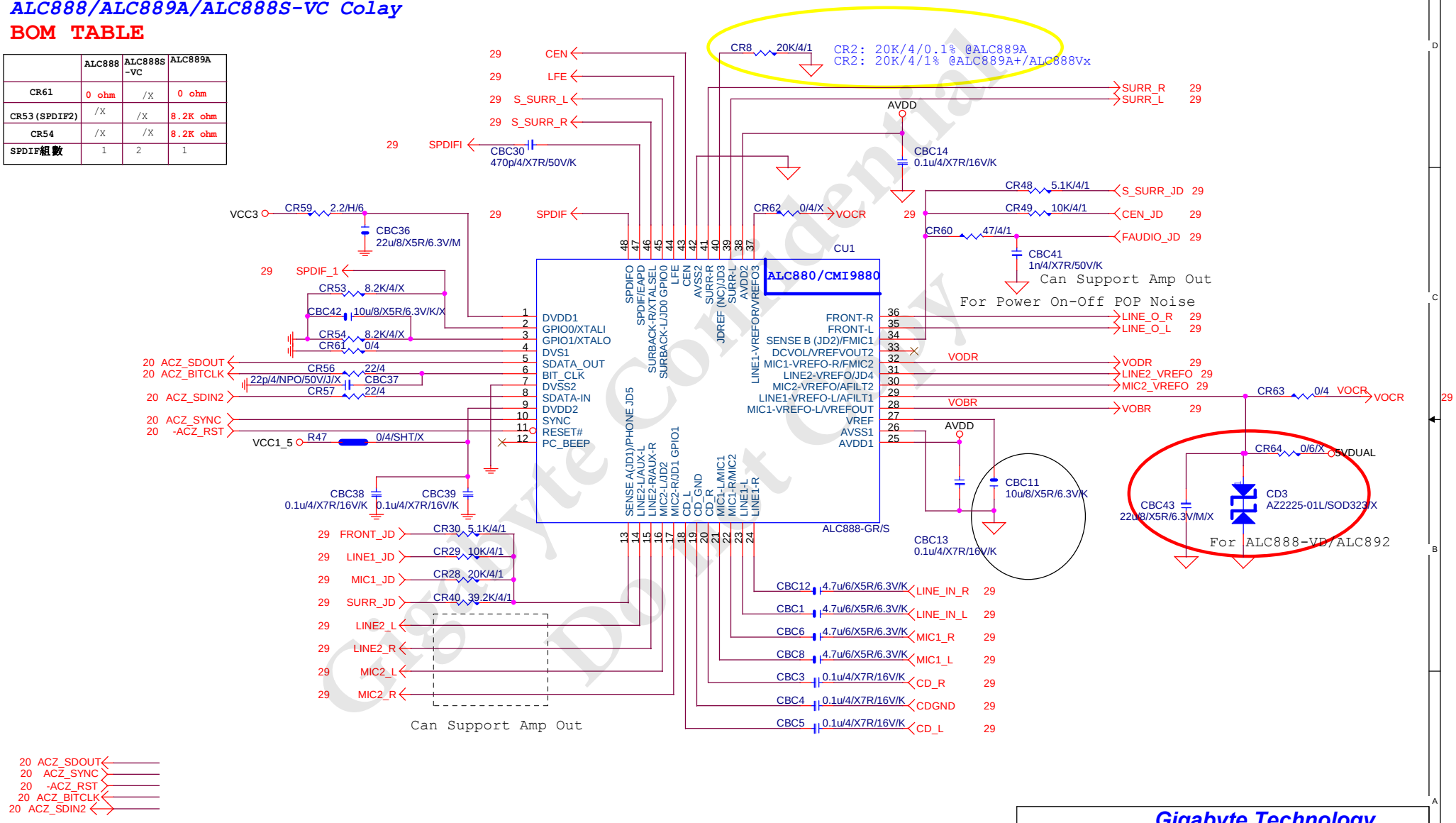


AZALIA CODEC

ALC888/ALC889A/ALC888S-VC Colay

BOM TABLE

	ALC888	ALC888S-VC	ALC889A
CR61	0 ohm	/X	0 ohm
CR53(SPDIF2)	/X	/X	8.2K ohm
CR54	/X	/X	8.2K ohm
SPDIF組數	1	2	1



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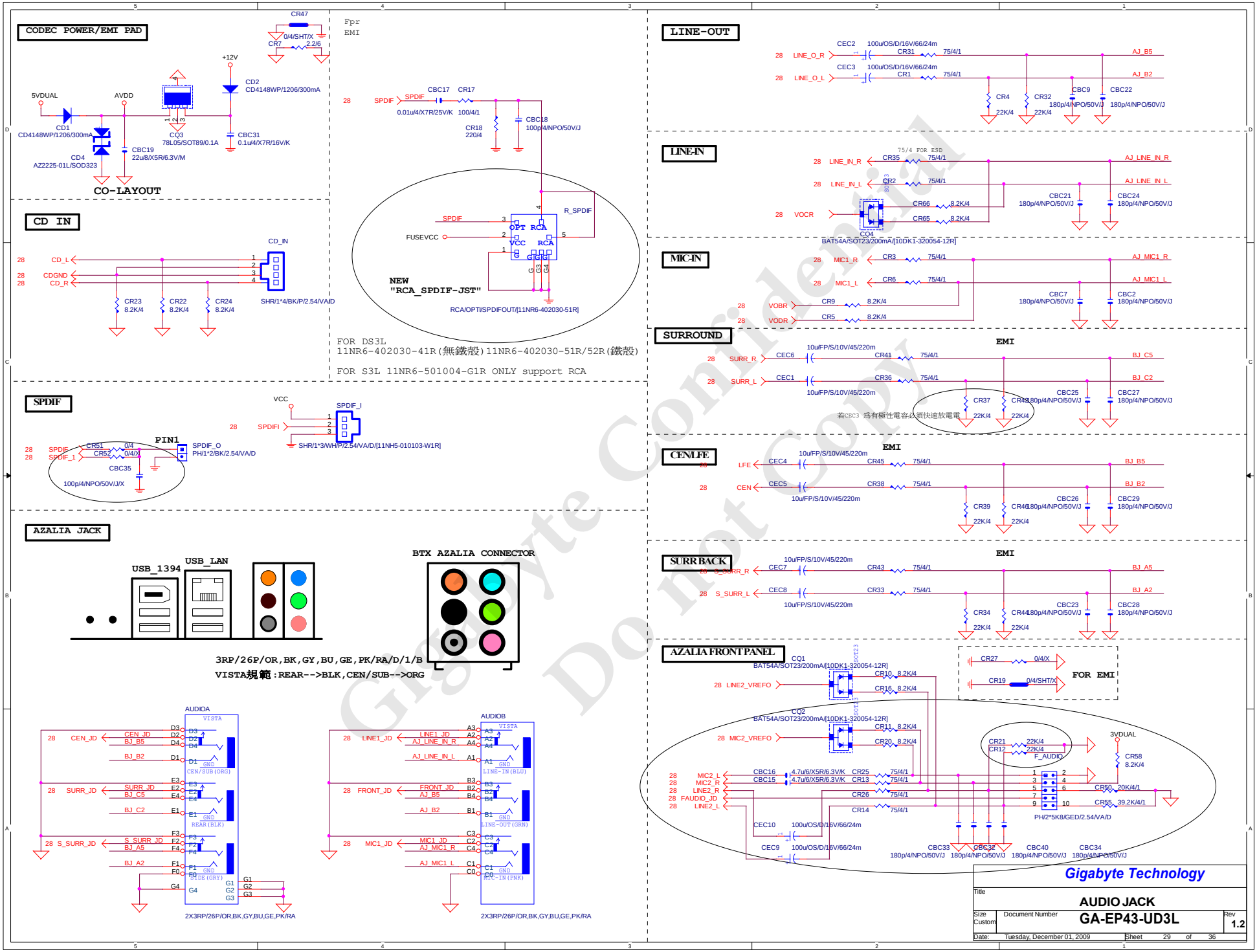
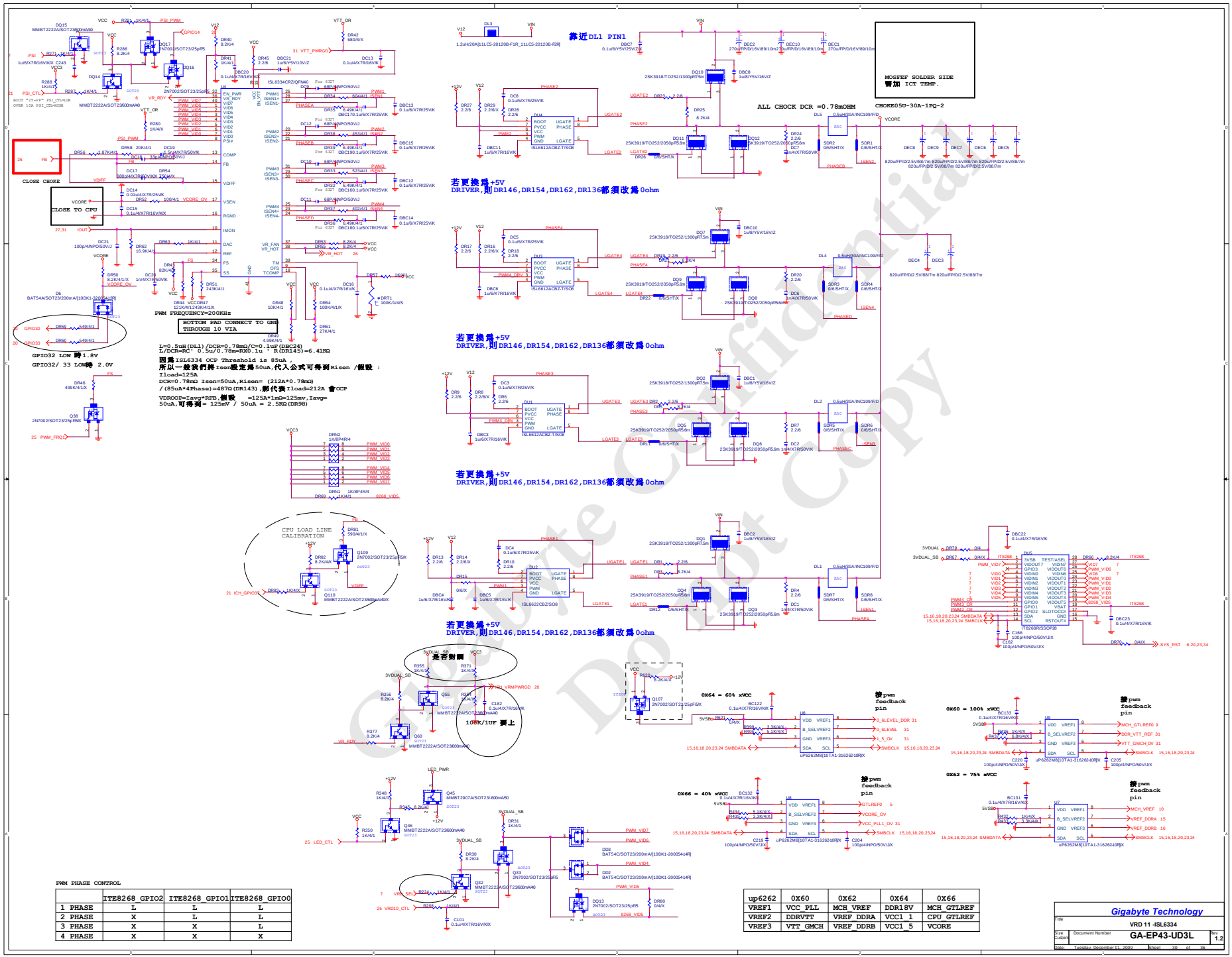
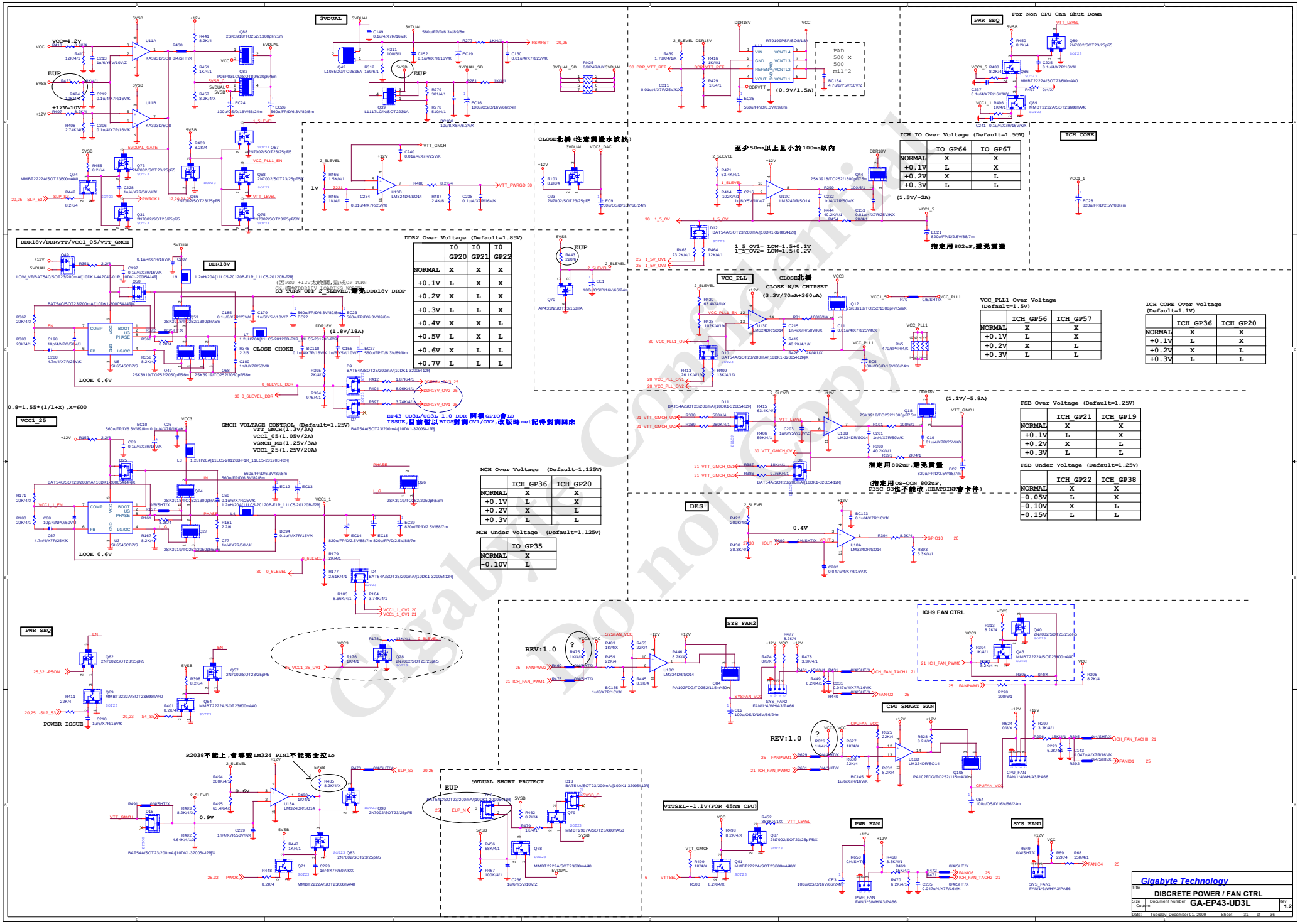


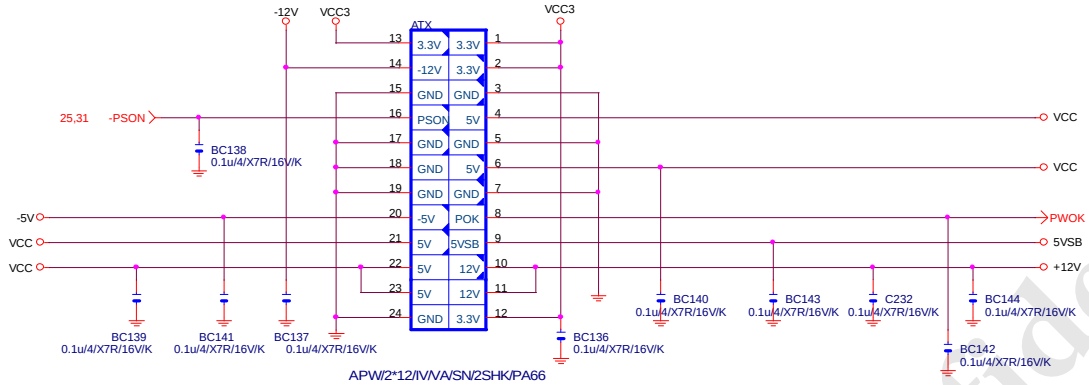


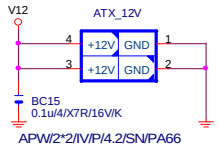
	ITE8268_GPIO2	ITE8268_GPIO1	ITE8268_GPIO0
1 PHASE	L	L	L
2 PHASE	X	L	L
3 PHASE	X	X	L
4 PHASE	X	X	X

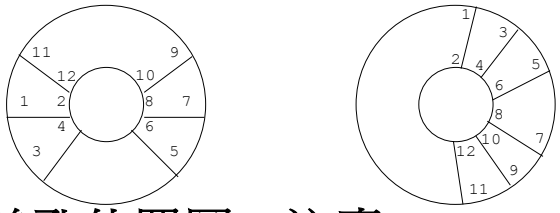
up6262	0X60	0X62	0X64	0X66
VREF1	VCC_PLL	MCH_VREF	DDR18V	MCH_GTLREF
VREF2	DDRVTT	VREF_DDRA	VCC1_1	CPU_GTLREF
VREF3	VTT_GMCH	VREF_DDRB	VCC1_5	VCORE



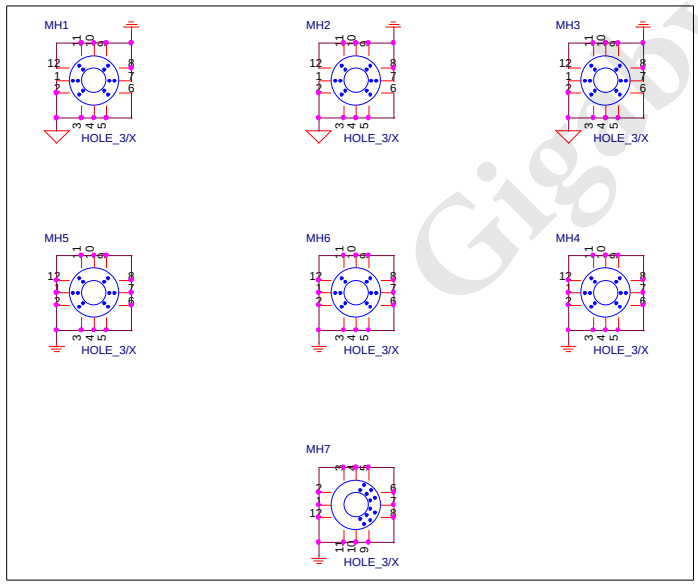
ATX POWER CONNECTOR

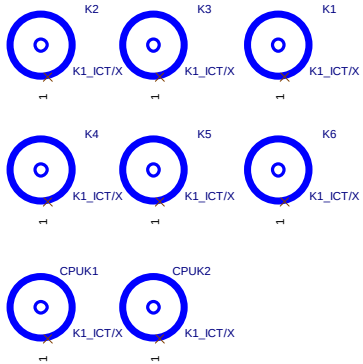


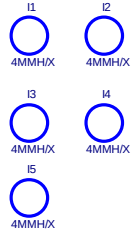




螺絲孔位置圖 （注意Footprint不同）







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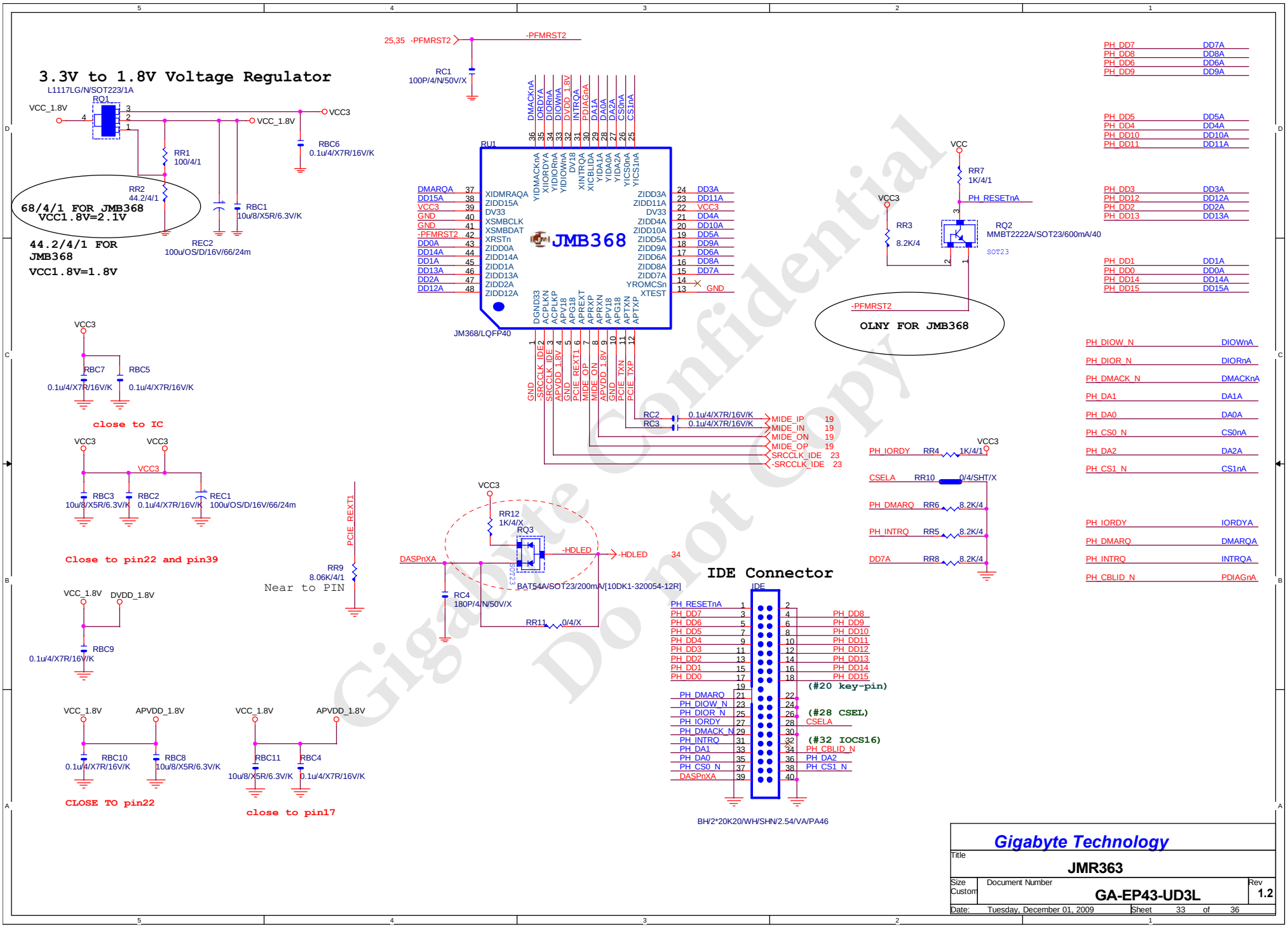

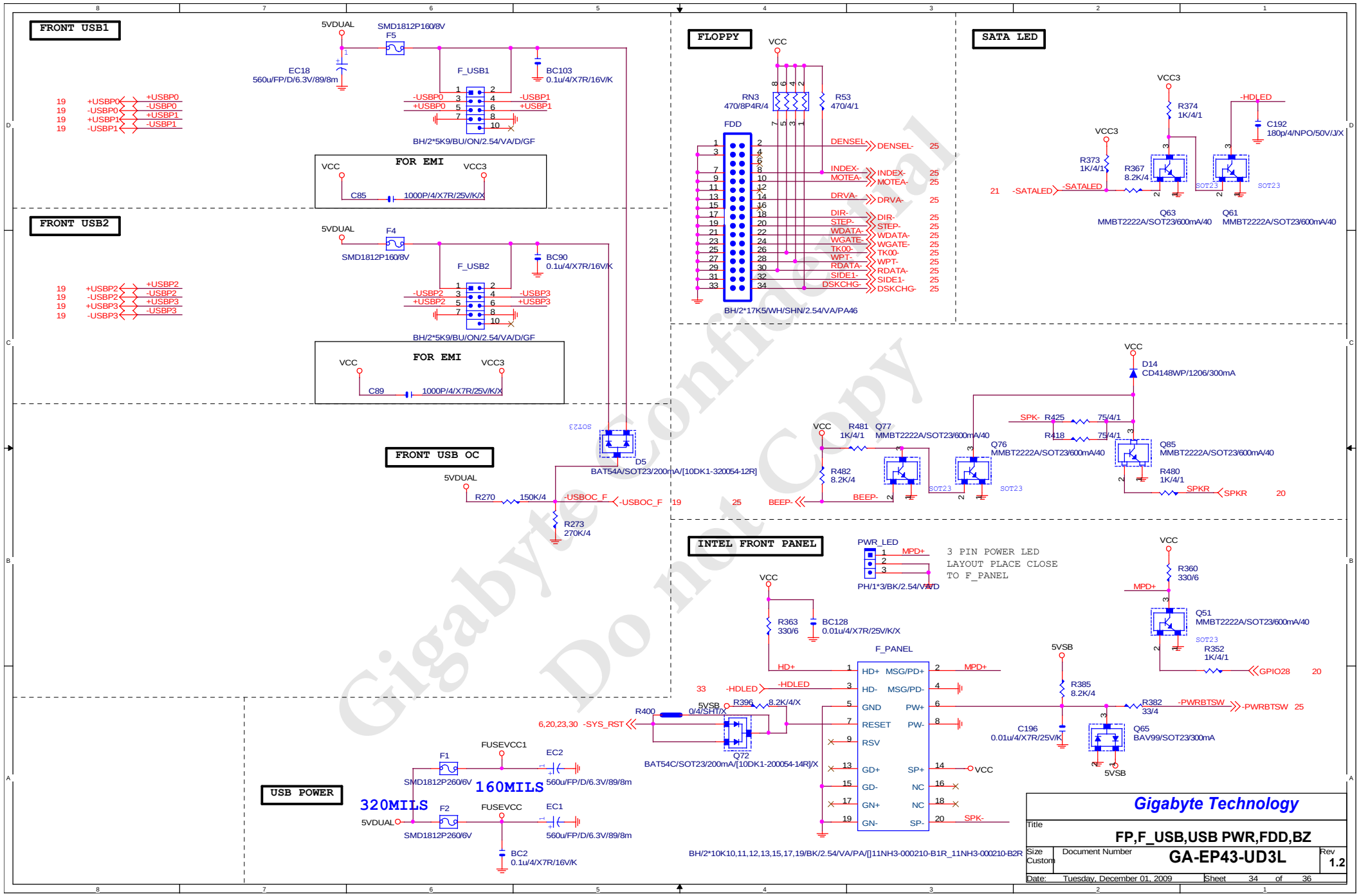

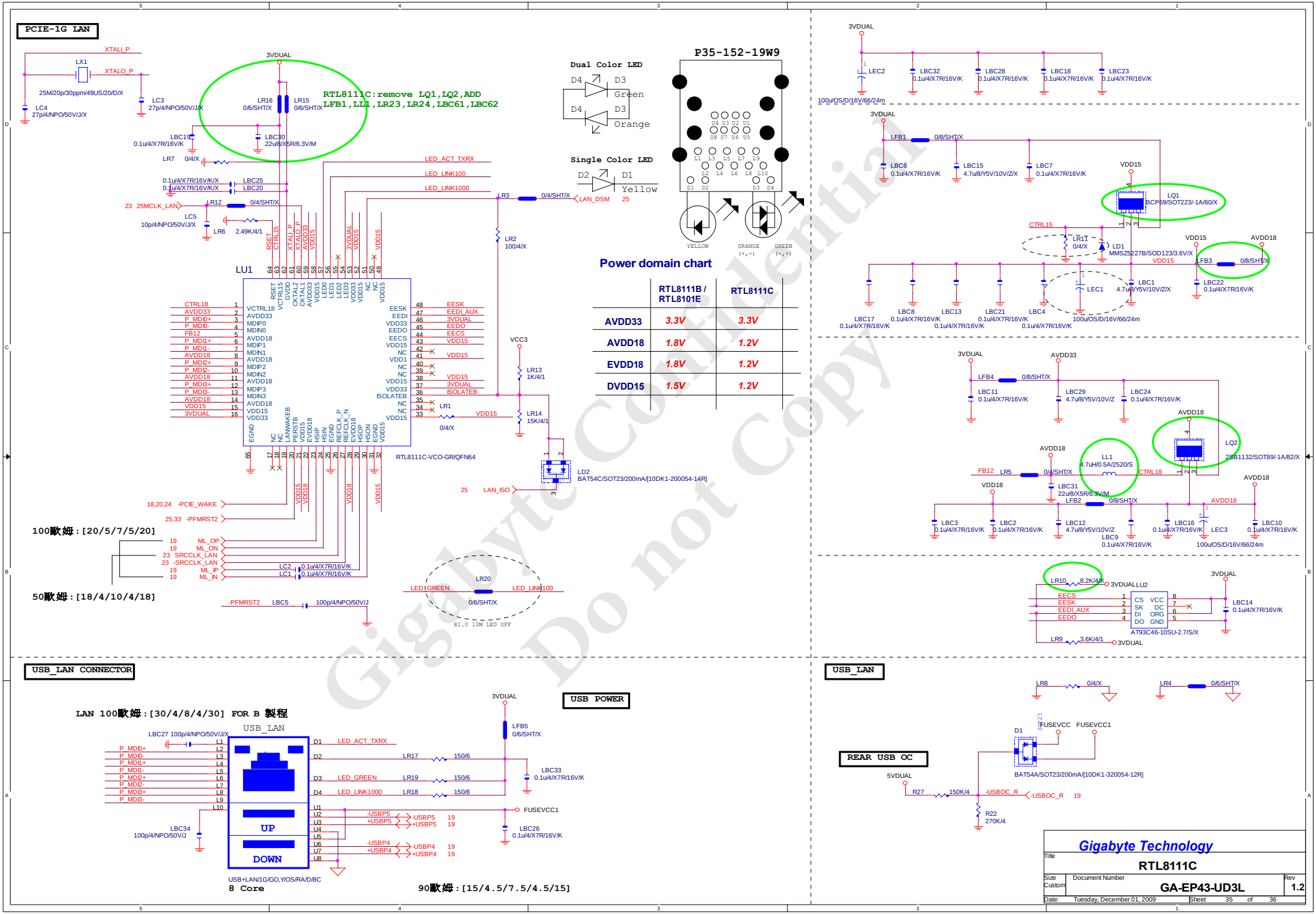

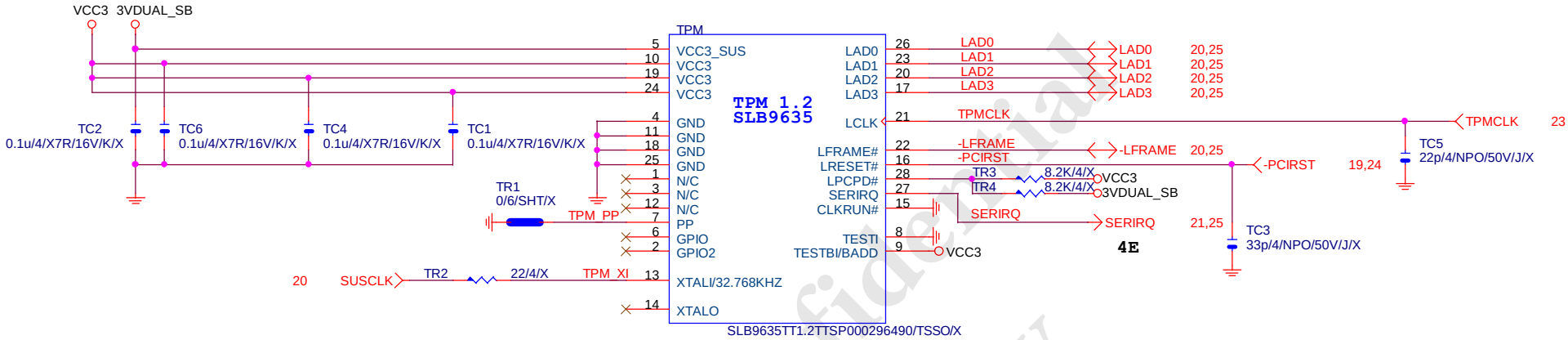

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