Model Name: GA-EP43-UD3L

REV 1.1

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02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	TABLE LIST
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06	P4_LGA775_B,D
07	P4_LGA775_C
08	P4_L775_E,F,G,H
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10	GMCH-Eaglelake_DDRII
11	GMCH-Eaglelake_PCI E, DMI
12	GMCH-Eaglelake_INT VGA
13	GMCH-Eaglelake_GND
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17	DDRII TERMINATION
18	PCI EXPRESS*16 SLOT
19	ICH10 DMI, PCI, USB
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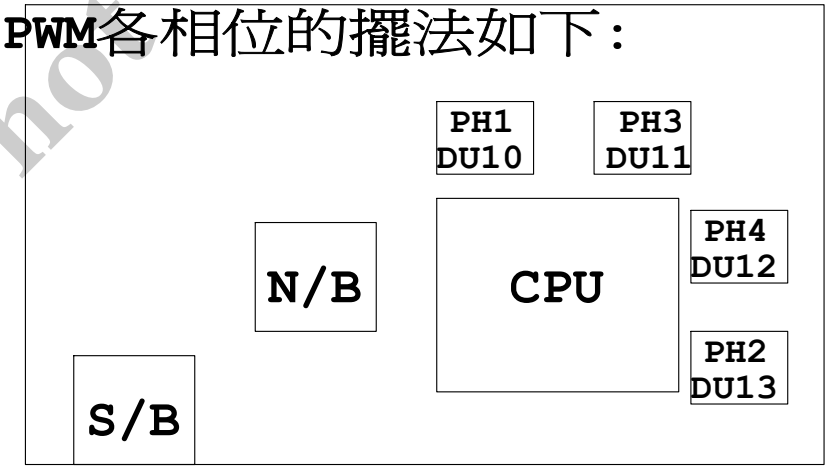
SHEET	TITLE
28	AZALIA ALC888
29	AUDIO JACK
30	VCORE PWM_ISL6334CRZ
31	DISCRETE1 POWER,FAN CTRL
32	ATX POWER
33	JMicron JMB368
34	LAN REALTEK RTL8111C
35	FRONT PANEL,FUSB,FDD
36	TPM I/F-1.2

PWM各相位的擺法如下：



Gigabyte Technology

Title	Cover Sheet	
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Date: Friday, April 24, 2009	Sheet 1 of 36	

Model Name: GA-EP43-UD3L
Rev:.1.1

Component value change history

Data	Change Item	Reason
97/04/01 EBOM:01A	1. P43 CHIPSET E-BOM	
97/04/15 EBOM:02	1. 修改LED的POWER及阻值;DEL R484,DR78. ADD DR79,,R348	
	2. ADD DR80,R300 10-->49.9,C158,LBC43 0ohm-->100PF for EMI	
	3. del Q3,Q4,BC11,BC9,R42,R15,PCI_BT1,PCI_BT2,R166,R168	
97/04/28 EBOM:10A	1. DDR2 VOLTAGE 1.83 --> 1.9V --> 2.0V --> 2.1V .....-->2.5V	
97/05/09 PBOM:10B	1. DR59,DR60 14K---->549ohm,del DR69	
	2. ADD U9(uP6262),R436,BC133 FOR CPU 超頻	
97/05/21 PBOM:10C	1.ICH,MCH PCI-E ,JM368的RX,TX串電容BOM 0.1U/Y5V-->0.1U/X7R,RTC RTCVDD -->X7R	
	2.ADD U6 FOR DDR TURN ON 2.1V ISSUE	
97/06/4 PBOM:10D	1.DEL Q107,R620,ADD R621	
	2.Q49(BAT54C) 限用 DII	
97/06/18 PBOM:10E	1.ADD MB_ID R283,DEL R282,Q87,Q91,R452,R498,R499,R500 FOR VTT_GMCH 1.2V	
	2.C197 0.1U/Y5V--->X7R	
	3.R300 49.9--->100 ohm ,C158 Y5V--->X7R for USB	
	4.DC20 0.01u--->1nf FOR CPU PSI ISSUE	
97/08/07 EBOM:20A	1.CPU 改爲SMART FAN	
	2.L4,L7 CHOKE Footprint Change "CHOKE1U2-20A-1PQN"	
	3.獨立南橋1.1V 的電壓	
	4. ADD GPIO37 FOR LOAD LINE CALIBRATION	
	5.J368 改爲1.8V;R209=100 OHM, ADD R640 FOR MB_ID2	
97/08/08 EBOM:30A	1.J368 改爲1.8V;47--->44.2 2.TO252---改爲POWER PACK	
97/10/01 PBOM:10A	FOR EP45-UD3L-1.0	
	1.R183 18K-->9.09K;R184 9.76K--->4.3K 2.DR56 1.74K-->1.87K;DR81 1K--->590 OHM	
	3.DR38 487--->549 ohm 4.R369 2.26K--->1.5K;R378 13.7K--->15.8K	
	4.NB,SB CHANGE HEAT SINK for UD series; PCIEX1 SLOT改爲白色	
	5.RQ3 由BJT改爲 BAT54A FOR -HDLED ISSUE	
97/11/17 EBOM:10A	FOR EP43-UD3L-1.0 1.P43 CHIP,HEAT SINK,UPI	
97/12/05 PBOM:10B	1.P-BOM,修改HEATSINK,調整部份阻值	
98/02/24 PBOM:10C	1.100UF 統一料號	
98/03/26 PBOM:11A	1.值變更NB,SB heatshink料號金色改灰色	

Circuit or PCB layout change for next version

DATE	Change Item	Reason
97/04/01 PCB:0.1	1.P43-DS3L	
97/04/23 PCB:1.0	1. CE3位置請移至EC24左邊	
	2. 增加 upi6262 VCC Power (R620,R621,Q107)	
	3. 增加R622,R623 FOR DDR18V_OV3	
97/07/23 PCB:2.0	1.由1.0 修改,直接改成2.0	
	2.PCIEX16 和PCIEX1_2對調位置	
	3. DDR2_1~DDR2_4往左移,盡量讓MCH的位置在DDR SLOT中間	
	4.ADD CPU SMART FAN CONTROL	
97/07/23 PCB:3.0	1.由2.0 修改	
	2. cpu Vcore MOS TO252改爲POWER PACK	
97/09/16 PCB:1.0	1.由3.0 修改,改文字面 EP45-UD3L ,ULTRA DURABLE 3,NB /SB 框內文字修改	
97/11/06 PCB:1.0	1.由EP45-UD3L改文字面成EP43-UD3L	
	2.DEL ICH CORE 1.1線路,NET DDR18V_OV2與LAN_DSM互換FOR DDR超壓ISSUE	
	3.UPDATE LL1 ,LGA775 FOOTPRINT	
98/03/27 PCB:1.1	1.TO CHANGE PCB VERSION FOR 1.1	

Gigabyte Technology

Title: BOM & PCB MODIFY HISTORY

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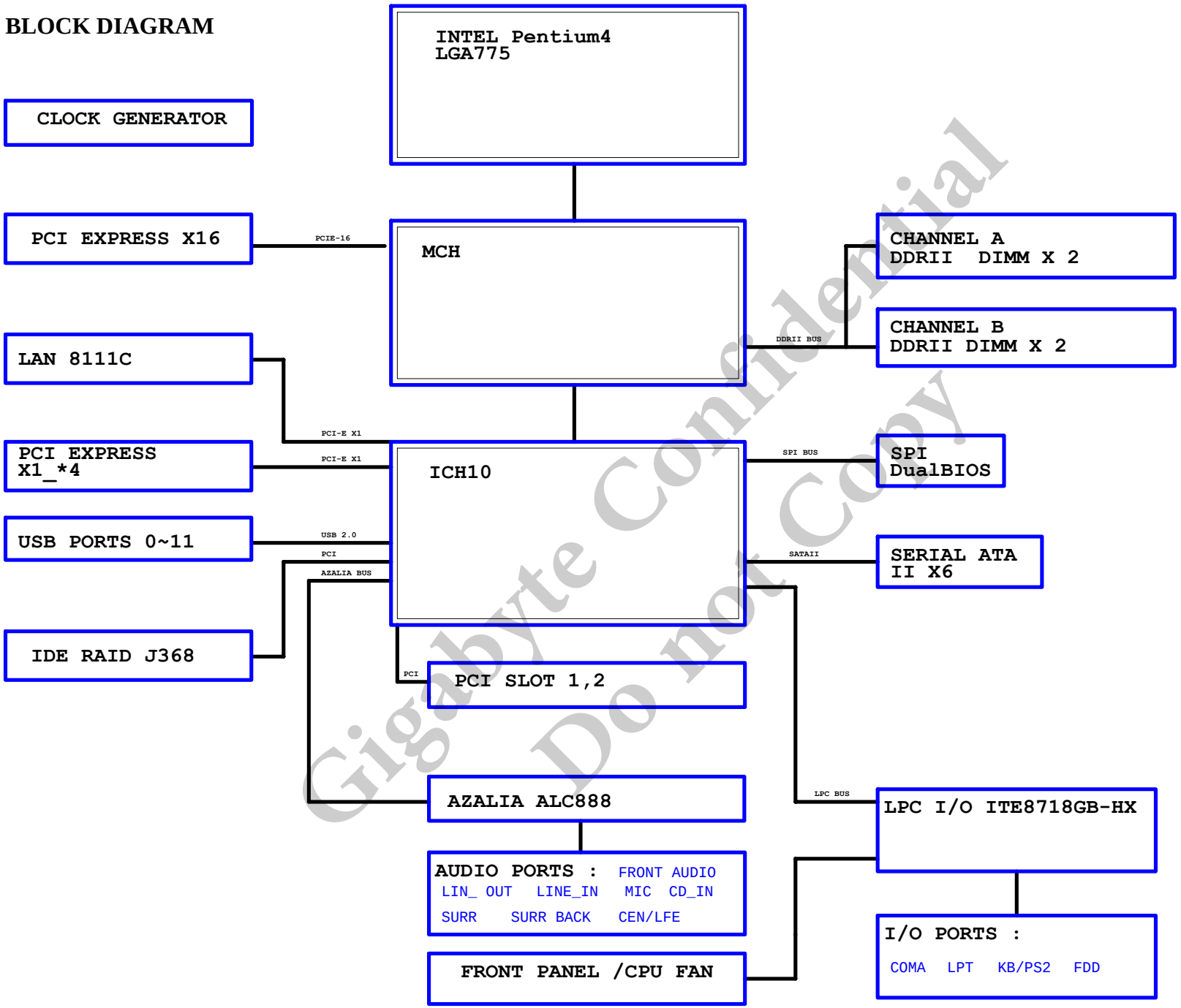
BLOCK DIAGRAM



Gigabyte Technology

Title	BLOCK DIAGRAM	
Size: Custom	Document Number: GA-EP43-UD3L	Rev: 1.1
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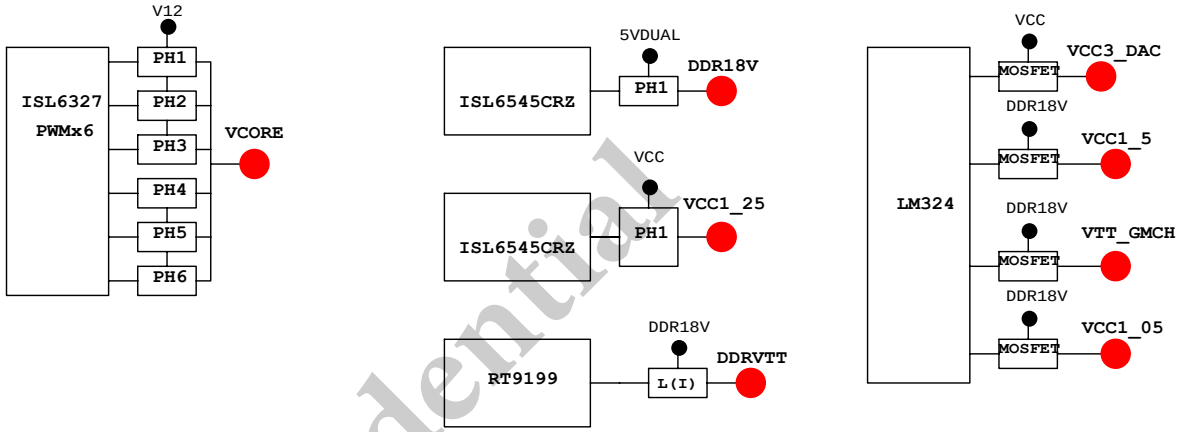
ICH8 GPIO LIST TABLE

PIN NAME	PWR WELL	AFTER/ PLTRST	USAGE	NOTE
GP0	MAIN	IN	-ACZ_DET	P/U 8.2K VCC3
GP1/TACH1	MAIN	IN	ICH_FAN_TACH1	P/U 8.2K VCC3
GP2/PIRQE#	MAIN	IN	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN	IN	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN	IN	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN	IN	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN	IN	ICH_FAN_TACH2	P/U 8.2K VCC3
GP7/TACH3	MAIN	IN	ICH_FAN_TACH3	P/U 8.2K VCC3
GP8	STBY	IN	GPIO8(DUALBIOS_INPUT)	P/U 8.2K 3VDUAL
GP9	STBY	OUT	WOL_ONLY	P/D 100K GND
GP10	STBY	IN	CLGPIO1	P/U 8.2K 3VDUAL
GP11/SMBALERT#	STBY	OUT	-SMBALRT	P/U 8.2K 3VDUAL
GP12	STBY	IN	MB_ID0	P/U 8.2K 3VDUAL
GP13	STBY	IN	-LPCPME	P/U 8.2K 3VDUAL
GP14	STBY	IN	CLGPIO2	P/U 8.2K 3VDUAL
GP15	STBY	OUT	LAN_DISABLE(STP_PCI-)	N/A
GP16	MAIN	OUT/LOW	RESET	N/A
GP17/TACH0	MAIN	IN	ICH_FAN_TACH0	P/U 8.2K VCC3
GP18	MAIN	OUT	MB_ID1	P/U 8.2K VCC3
GP19	MAIN	IN	SATA1GP	P/U 8.2K VCC3
GP20	MAIN	OUT	-SPI_WP0	P/U 1K 3VCL
GP21	MAIN	IN	SATA0GP	P/U 8.2K VCC3
GP22	MAIN	IN	SCLOCK	P/U 8.2K VCC3
GP23	MAIN	OUT	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	OUT	CLGPIO0	P/U 8.2K 3VDUAL
GP25	STBY	IN	MB_ID2(STP_CPU-)	P/U 8.2K 3VDUAL
GP26/S4_STATE#	STBY	OUT	S4_STATE#	P/U 8.2K 3VDUAL
GP27	STBY	OUT/LOW	GPIO27(EL_STATE0)	P/U 8.2K 3VDUAL
GP28	STBY	OUT/LOW	PWR_LED(EL_STATE1)	N/A
GP29/OC5#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP30/OC6#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP31/OC7#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP32	MAIN	OUT	DUAL_BIOS	P/U 100K+1M VCC3
GP33	MAIN	OUT	DUAL_BIOS	P/U 8.2K VCC3
GP34	MAIN	OUT/LOW	GPIO34/SMB_RST	N/A
GP35	MAIN	OUT	SATACLKREQ#	N/A
GP36	MAIN	IN	SATA2GP	P/U 8.2K VCC3
GP37	MAIN	IN	SATA3GP	P/U 8.2K VCC3
GP38	MAIN	IN	SLOAD	P/U 8.2K VCC3
GP39	MAIN	IN	GPIO39	P/D 8.2K GND
GP48	MAIN	IN	GPIO48	P/U 8.2K VCC3
GP49	MAIN	IN	CPUPWROK	P/U 100 VTT_OL

VCORE:6 PHASE PWM--ISL6327CRZ



Gigabyte Technology			
Title: TABLE LIST			
Size: B	Document Number: GA-EP43-UD3L		Rev: 1.1
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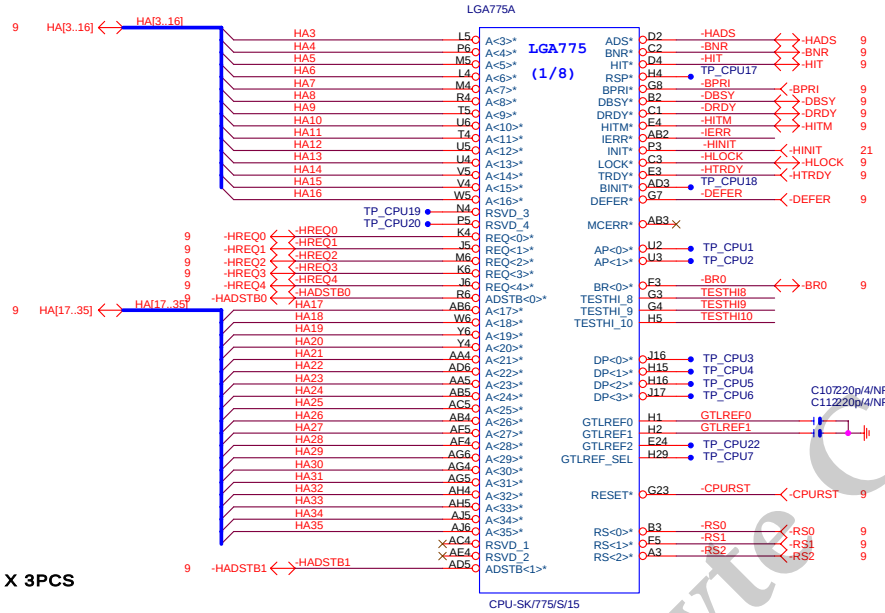
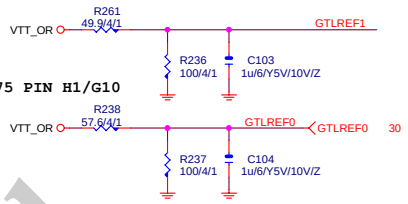
0.667 X VTT FOR LGA775 PIN H2/F2

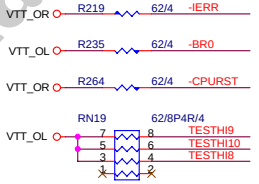
0.635 X VTT FOR LGA775 PIN H1/G10

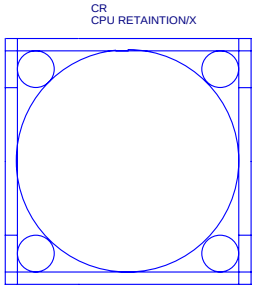
HA/REQ:50歐姆+-15% [4/11]

ADSTB:50歐姆+-15% [4/14]

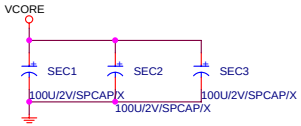




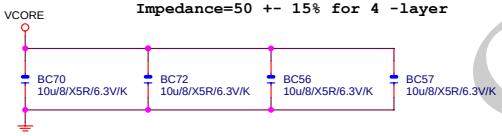


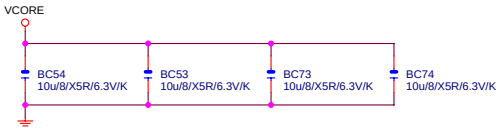


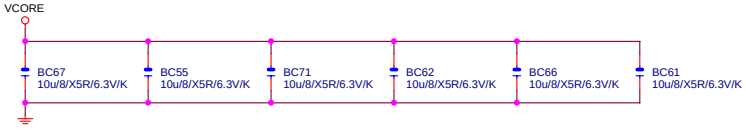
SP-CAP X 3PCS

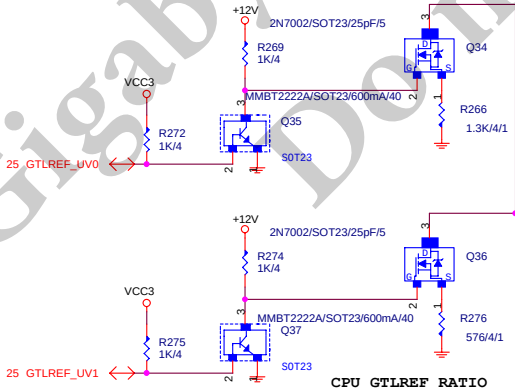


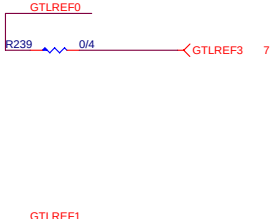
Impedance=50 +- 15% for 4 -layer











CPU GTLREF RATIO

GTLREF_UV0	GTLREF_UV1	Ratio Set
HIGH	HIGH	0.67
LOW	HIGH	0.65
HIGH	LOW	0.63
LOW	LOW	0.615

Gigabyte Technology

Title: P4_LGA775-A

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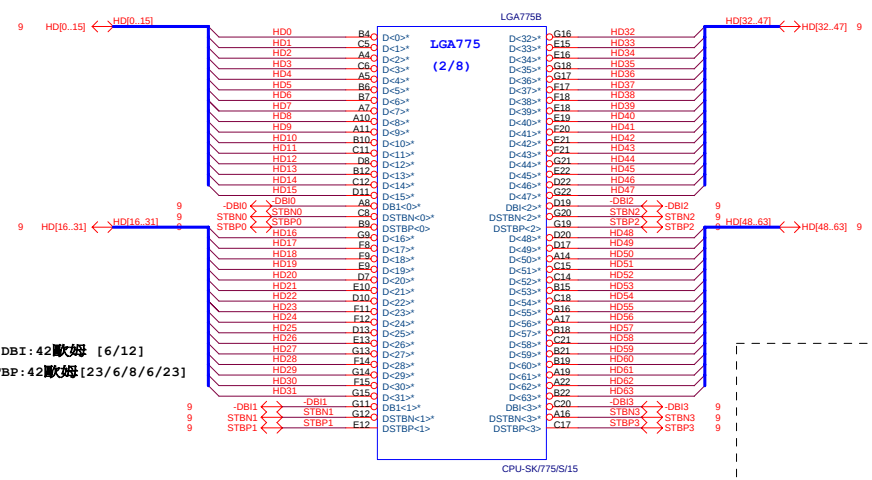
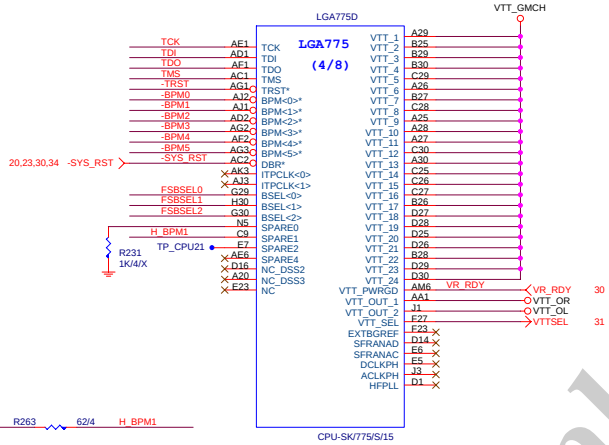
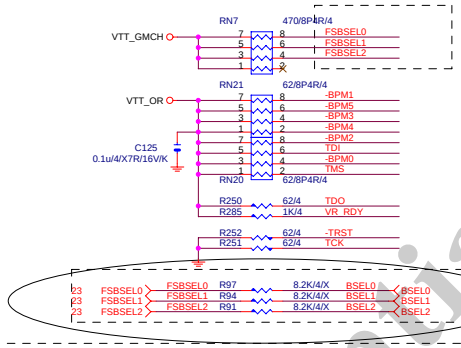
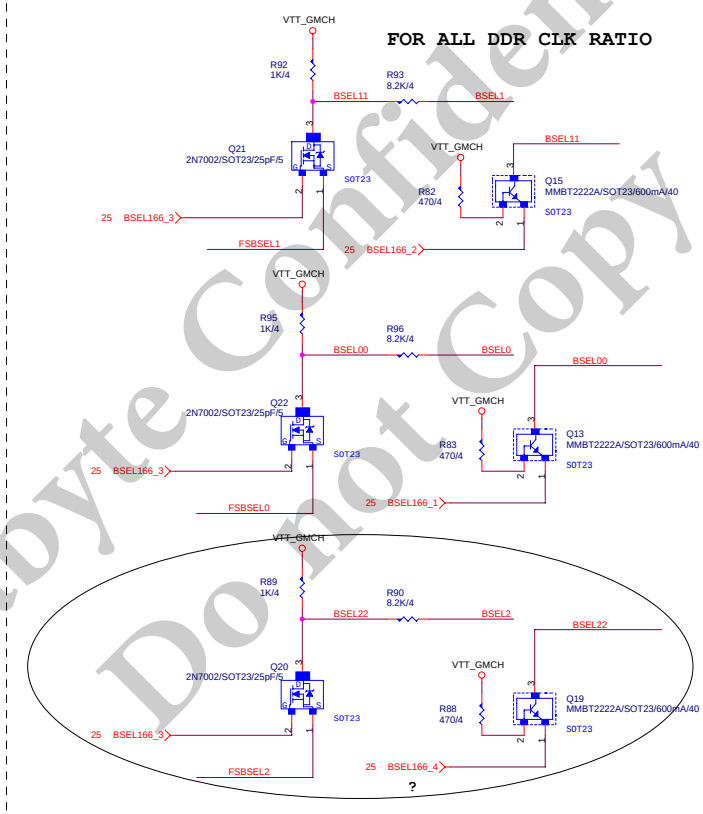


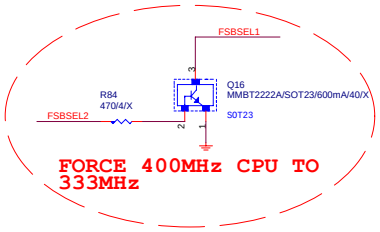
HD/DBI:42歐姆 [6/12]

DSTBP:42歐姆[23/6/8/6/23]









	FSA	FSB	FSC		
	FSBSEL0	FSBSEL1	FSBSEL2	Clock	
?	1	0	1	100MHz	
?	1	0	0	133MHz	3/4
G33	0	1	0	200MHz	2/2.66/3.33/4+
G33	0	0	0	266MHz	2/2.5/3/4~
G33	0	0	1	333MHz	2/2.4/3.2/4#
	0	1	1	400MHz	

400/533

400/533/667/800

533/667/800/1066

667/800/1066/1333

4X Length Guidelines for Quad core processors
Signal Name ATX Layer Pin to Pin
D[15:0]#, DBI0#, DSTBP0#, DSTBN0# Layer 1 2.2" - 2.7"
D[31:16]#, DBI1#, DSTBP1#, DSTBN1# Layer 4 3.0" - 3.5
D[47:32]#, DBI2#, DSTBP2#, DSTBN2# Layer 4 3.6" - 4.3
D[63:48]#, DBI3#, DSTBP3#, DSTBN3# Layer 1 2.4" - 3.0

Gigabyte Technology	
Title	P4_LGA775-B,D
Size: Custom	Document Number: GA-EP43-UD3L
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Note:

VCCA & VCOREPLL define doesn't same as old P4 design kit

Trace width doesn't less than 12 Mil

As close as possible to CPU socket

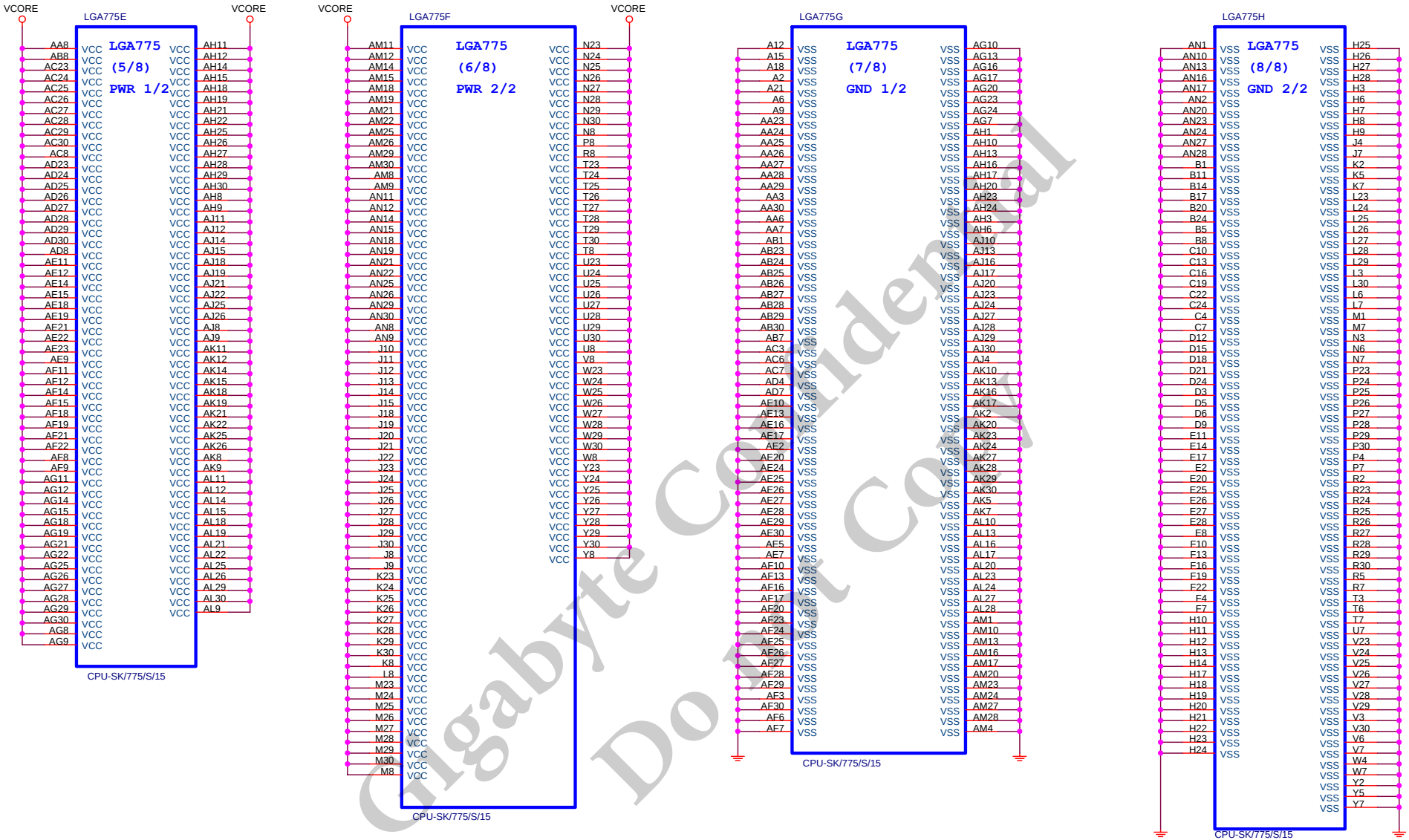
Place outside of CPU socket

COMP4~7 可以不上

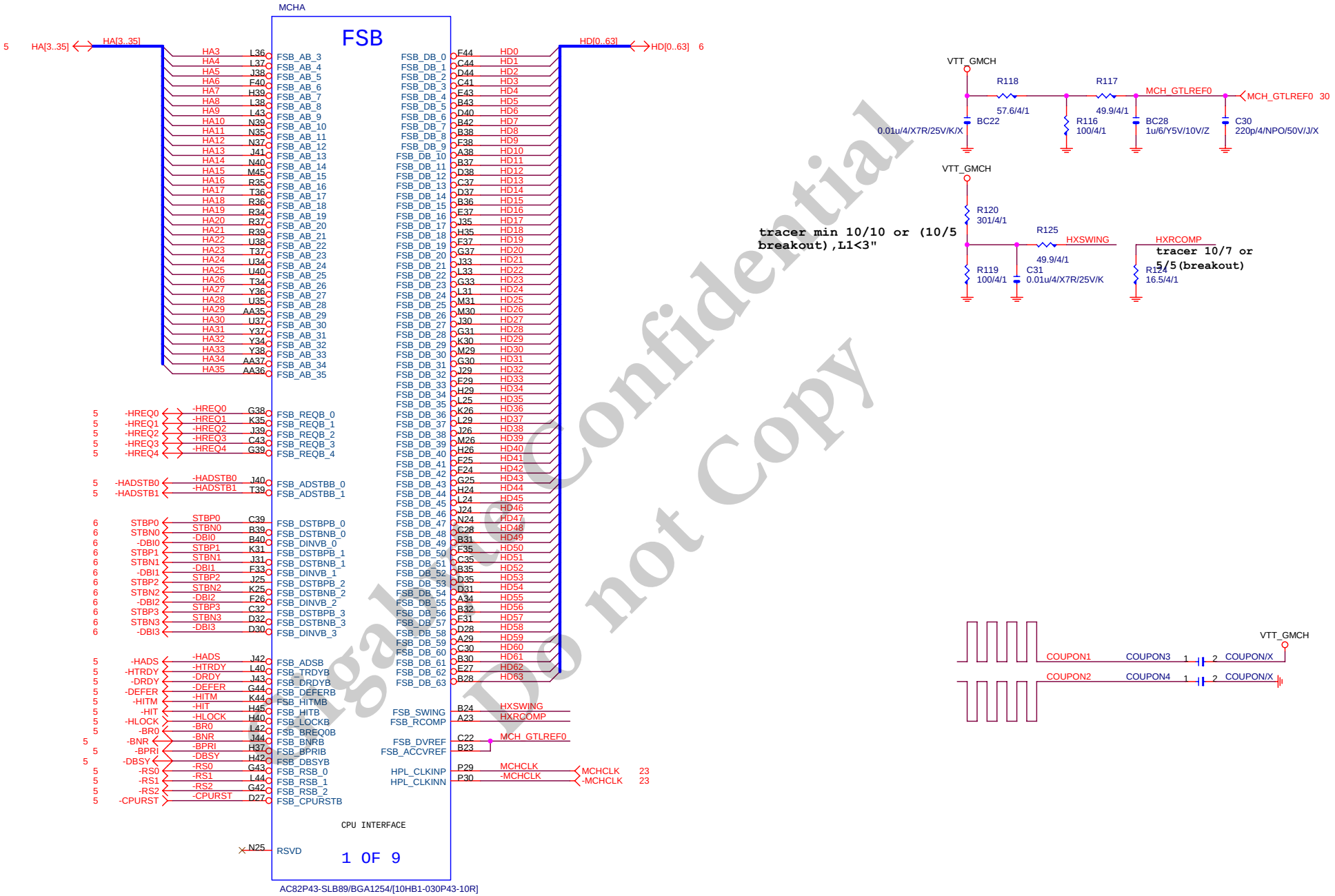
Pop to disable old Prescott CPU

PECI:Platform Environment Control Interface

Gigabyte Technology			
Title: P4_LGA775-C			
Size: B	Document Number: GA-EP43-UD3L	Rev: 1.1	
Date: Friday, April 24, 2009	Sheet 7 of 36		



Gigabyte Technology			
Title: P4_LGA775-E,F,G,H			
Size: B	Document Number: GA-EP43-UD3L		Rev: 1.1
Date: Friday, April 24, 2009	Sheet 8 of 36		



Gigabyte Technology			
Title: GMCH-HOST			
Size: Custom	Document Number: GA-EP43-UD3L		Rev: 1.1
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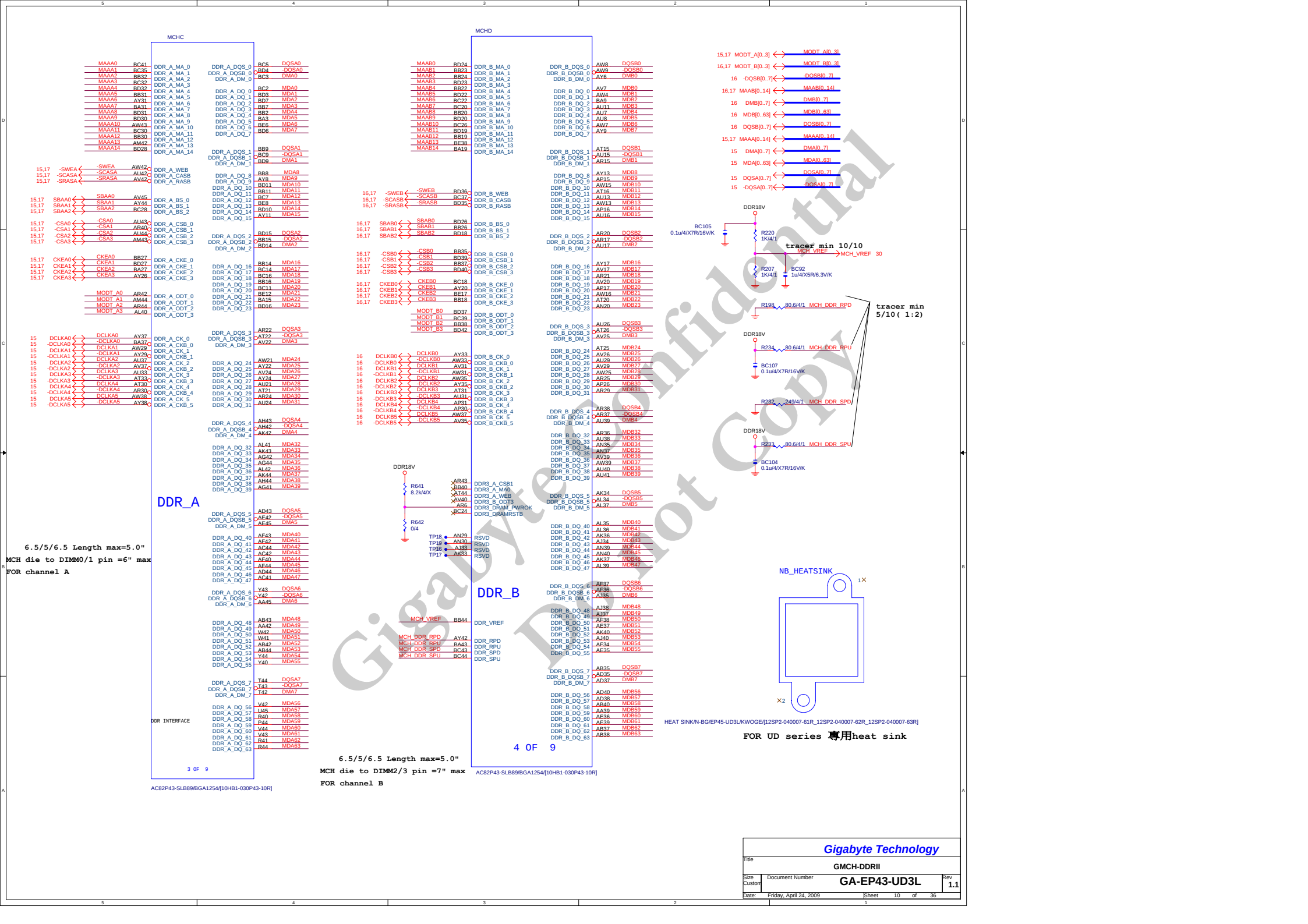

Gigabyte Technology	
Title	GMCH-DDRII
Size: Custom	Document Number: GA-EP43-UD3L
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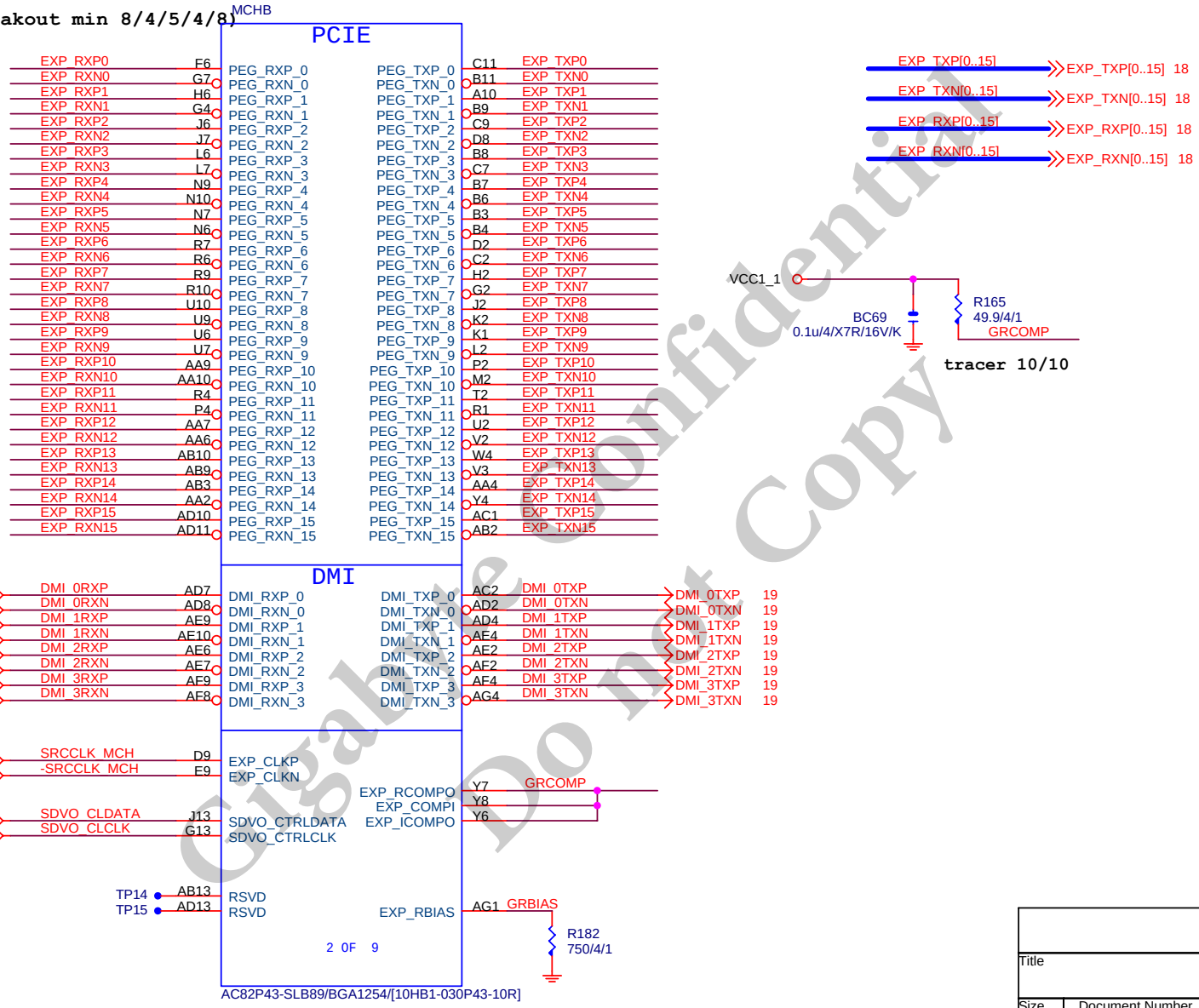
PCIEX16:16/5/5/5/5/16(breakout min 8/4/5/4/8)

Impedance=85 +- 17.5%

DMI:12/4/8/4/12

Impedance=95 +- 17.5%



Gigabyte Technology		
Title: GMCH-PCI E & DMI		
Size: Custom	Document Number: GA-EP43-UD3L	Rev: 1.1
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EXP_SM
0:SDVO OR PCIE
1:BOTH SDVO AND PCIE

EXP_SLR:
0:BTX PCIE are reversed
1:ATX PCIE normal

ITPM:
0:ENABLE ITPM
1:DISABLE ITPM

CEN:
0:DISABLE TLS
1:ENABLE TLS

CL_VREF:4/10
0.349V

MCHE

VGA

MISC

5 OF 9

AC82P43-SLB89/BGA1254/[10HB1-030P43-10R]

BW+ICH8 不要上(SAMPLE)
BW+ICH7 要上

Gigabyte Technology

Title: GMCH-INTERNAL VGA

Size: Custom | Document Number: GA-EP43-UD3L | Rev: 1.1

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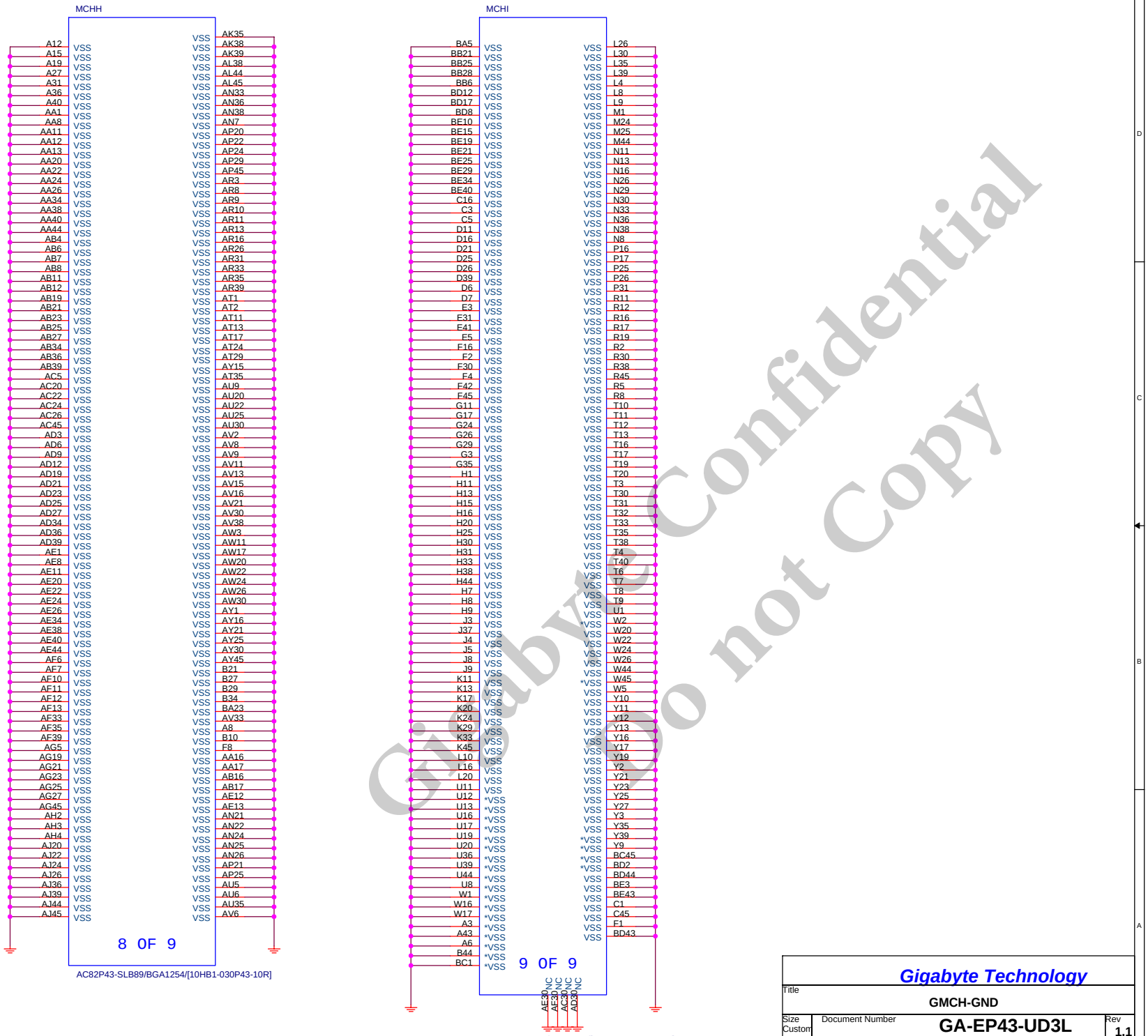

Gigabyte Technology		
Title	GMCH-GND	
Size: Custom	Document Number: GA-EP43-UD3L	Rev: 1.1
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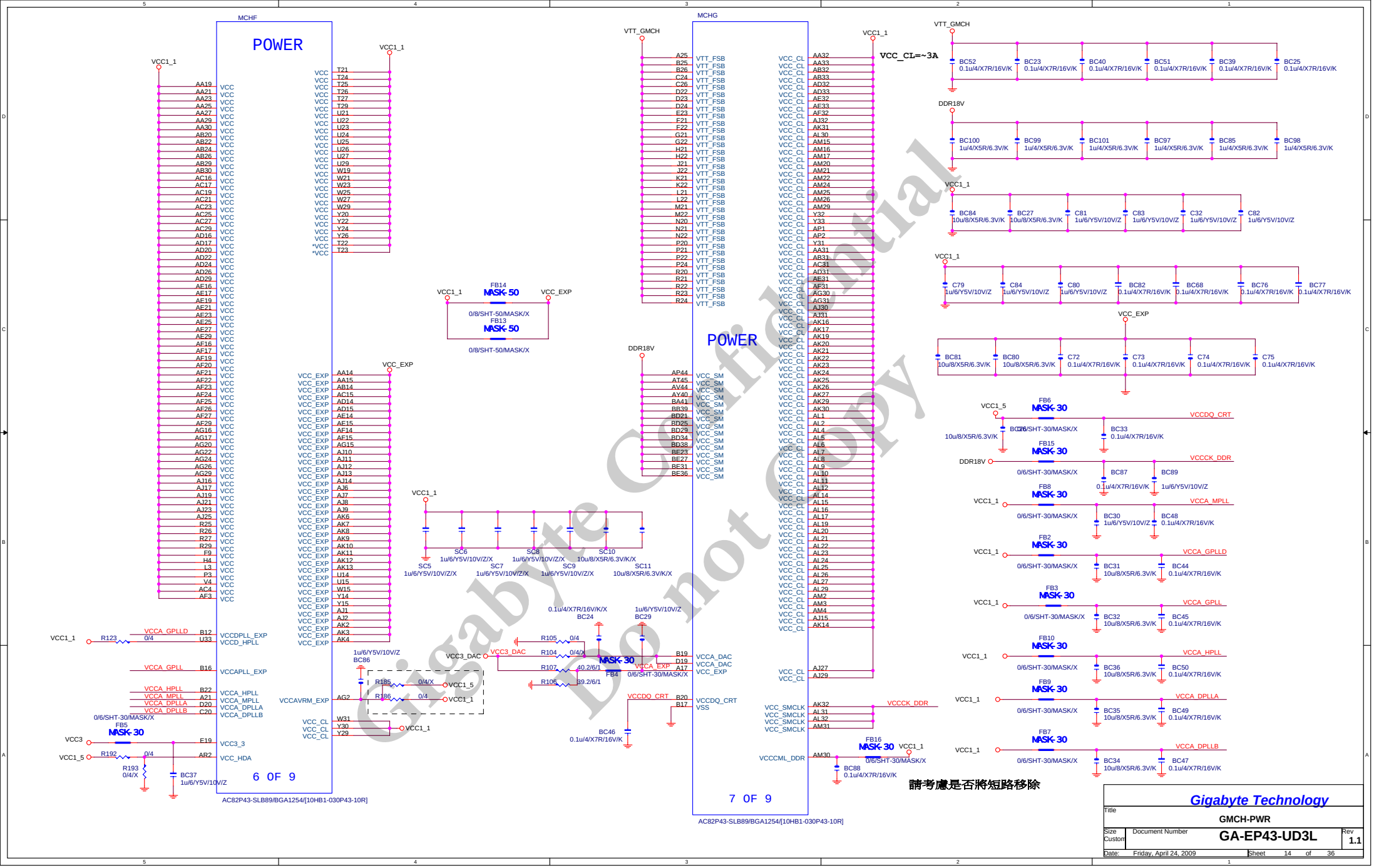
MCHF
POWER
6 OF 9
AC82P43-SLB89/BGA1254/[10HB1-030P43-10R]
MCHG
POWER
7 OF 9
AC82P43-SLB89/BGA1254/[10HB1-030P43-10R]
VCC_CL=~3A
請考慮是否將短路移除
Gigabyte Technology
GMCH-PWR
GA-EP43-UD3L
1.1
Friday, April 24, 2009
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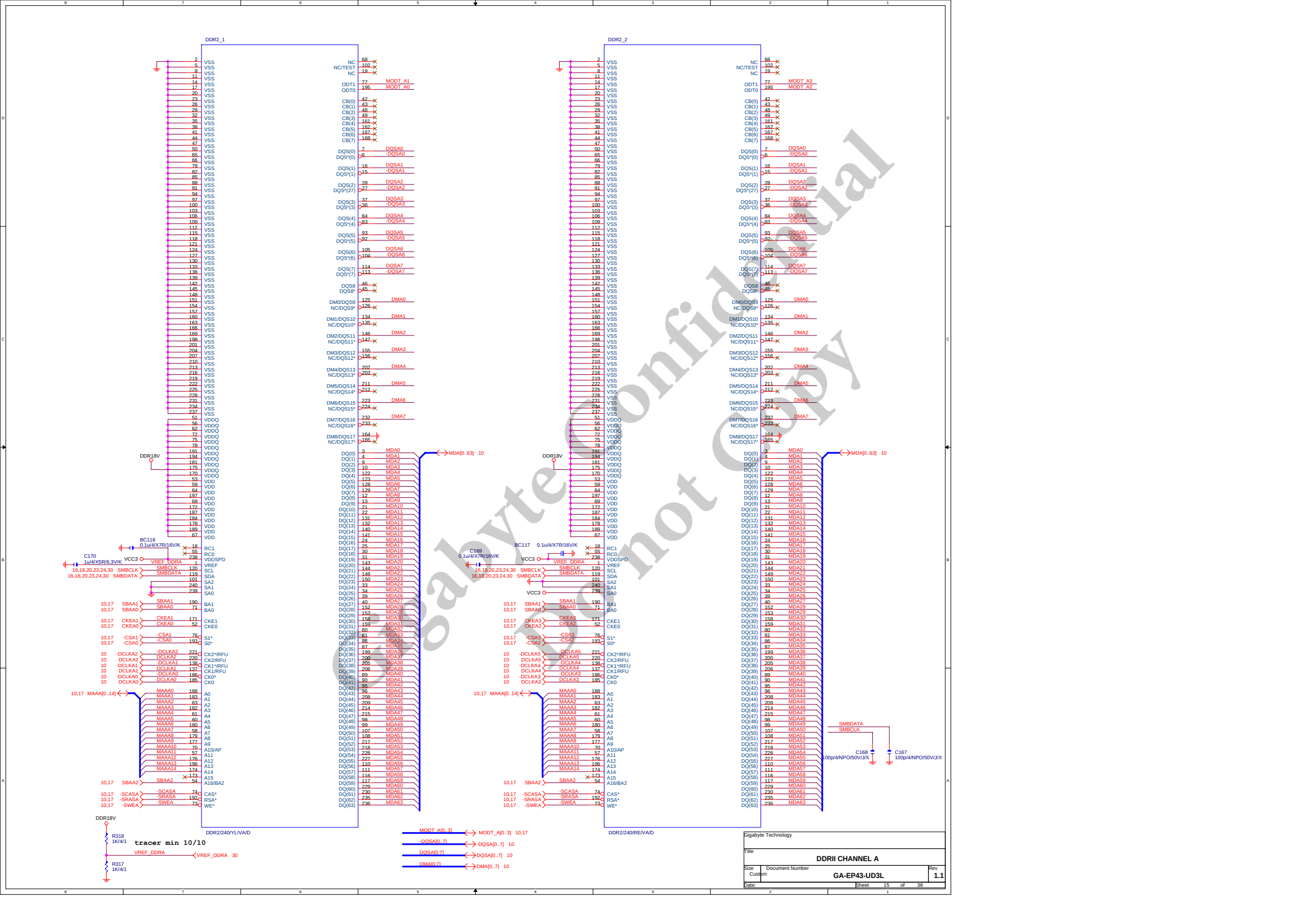
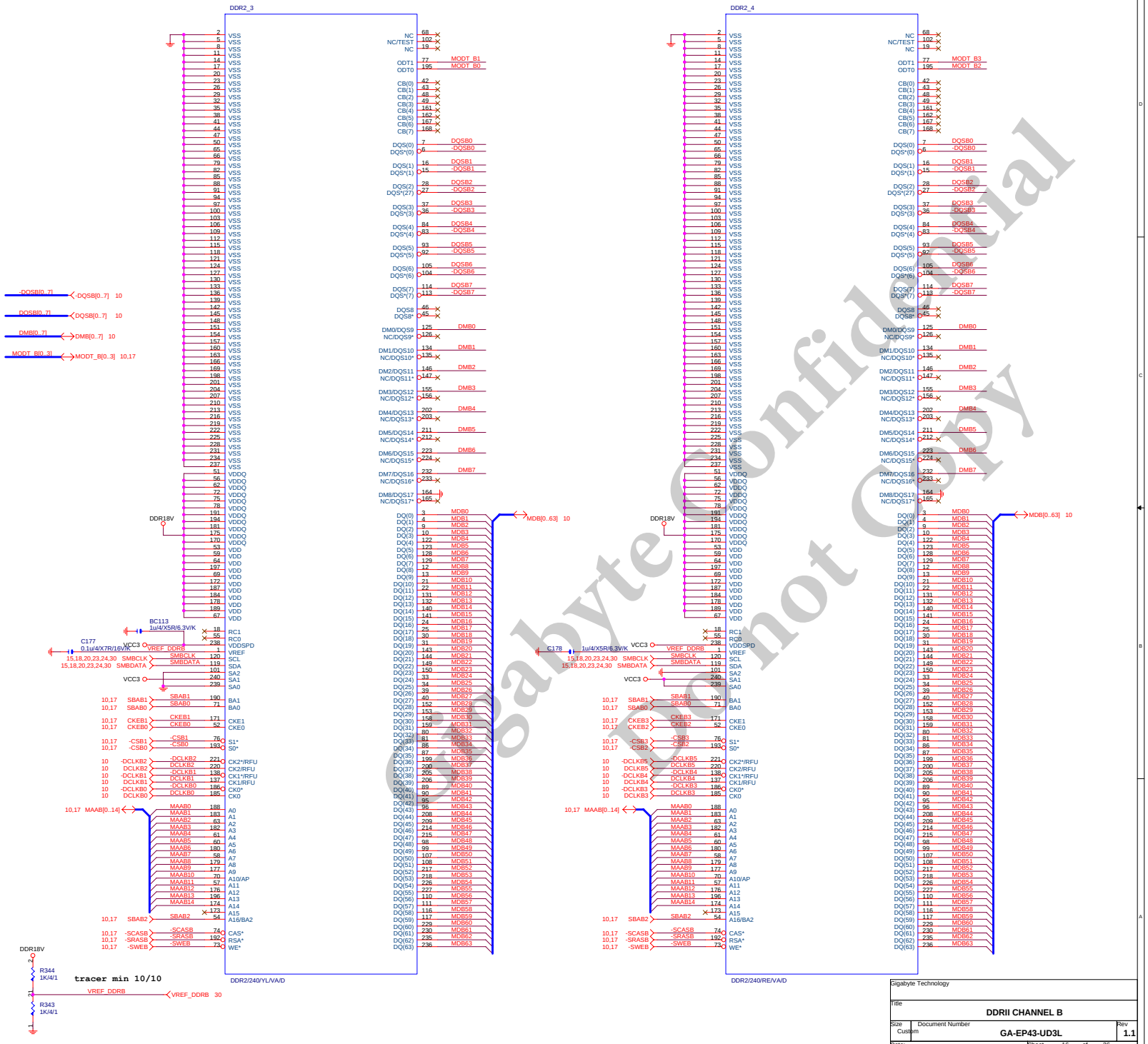
Do not Copy

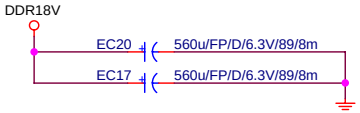


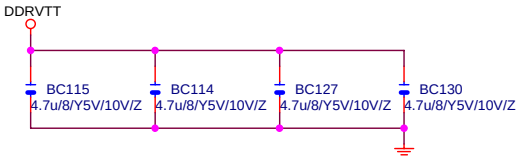


Gigabyte Technology	
Title	DDRII CHANNEL B
Size: Custom	Document Number: GA-EP43-UD3L
Rev	1.1
Date:	Sheet 16 of 36

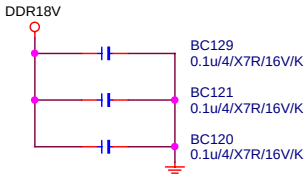
DDR TERMINATION CHANNEL A

DDRVTT Decouple

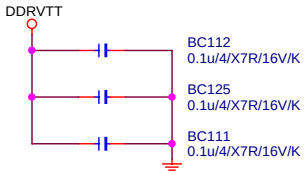


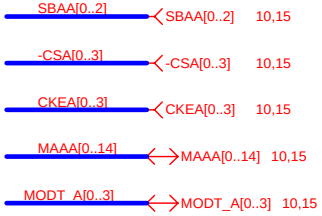


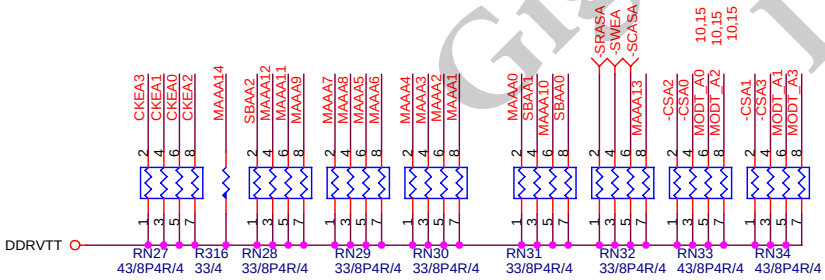
DDR18V Decouple



DDRVTT Decouple

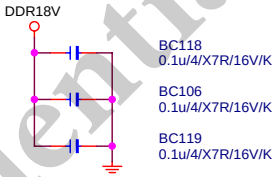




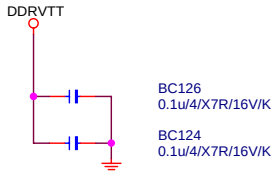


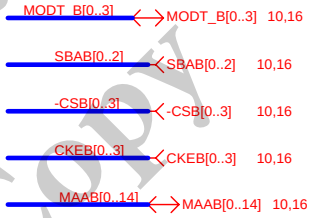
DDR TERMINATION CHANNEL B

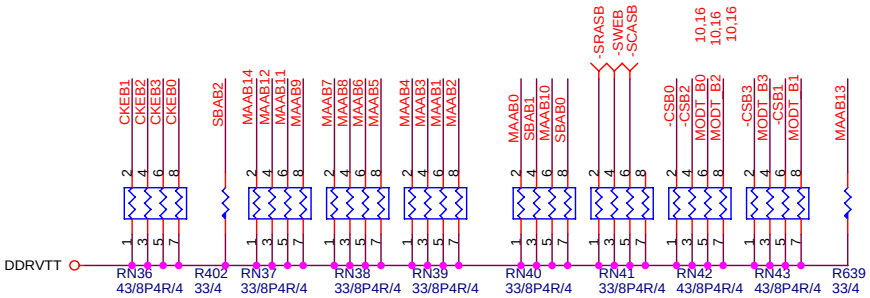
DDR18V Decouple



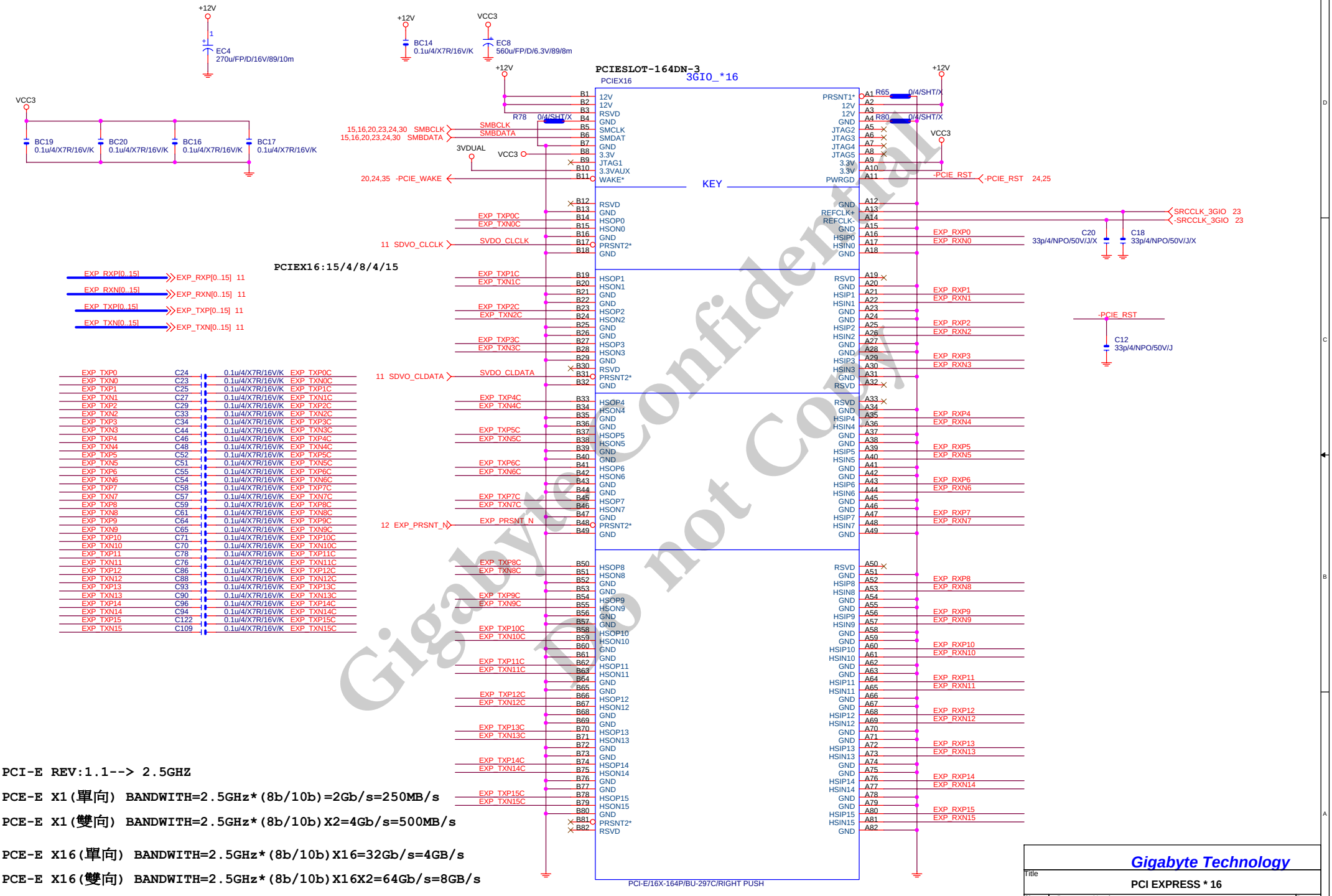
DDRVTT Decouple







Gigabyte Technology		
Title: DDRII TERMINATOR		
Size: Custom	Document Number: GA-EP43-UD3L	Rev: 1.1
Date: Friday, April 24, 2009	Sheet 17 of 36	



PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWITH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

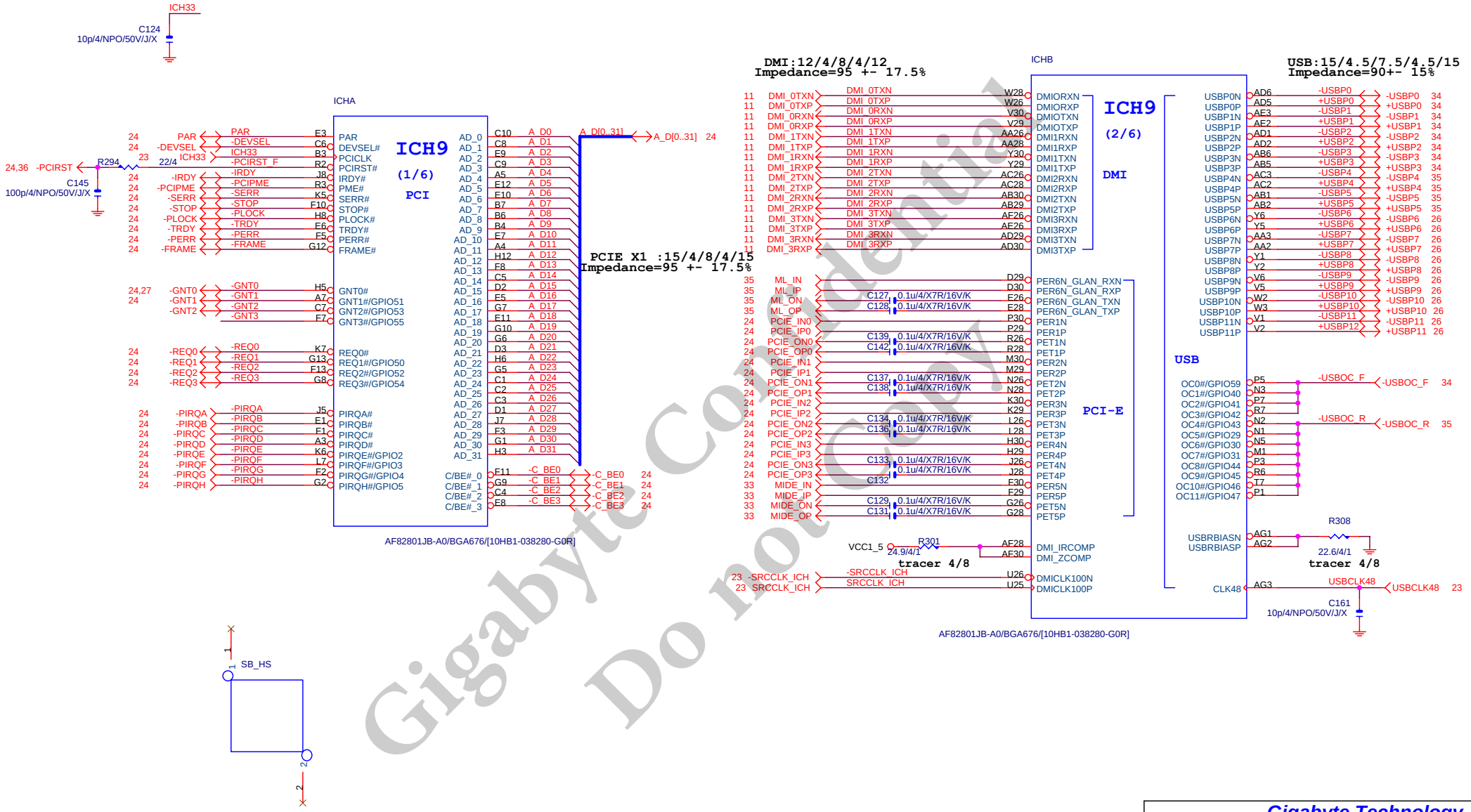
PCE-E X1(雙向) BANDWITH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWITH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s

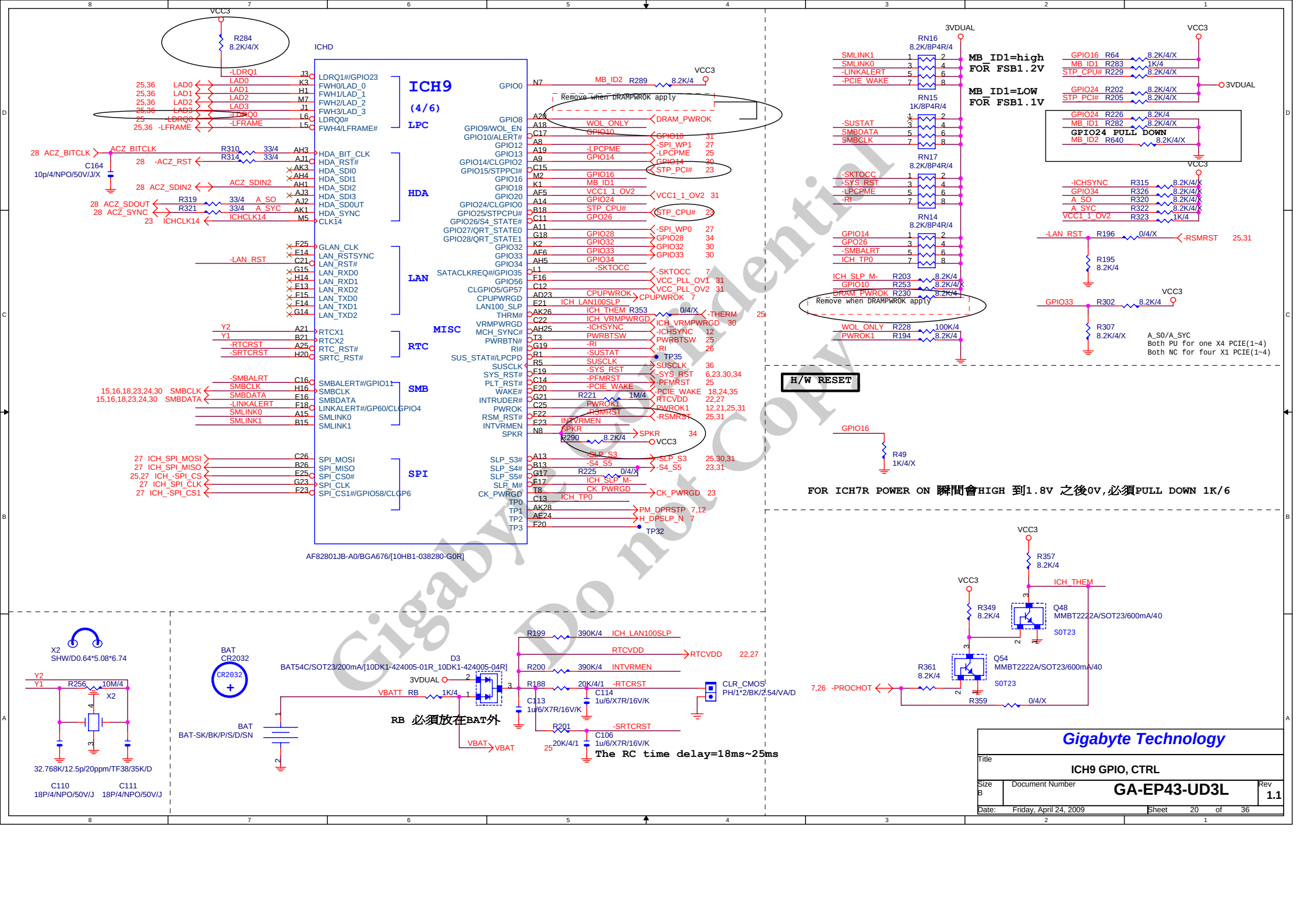
PCE-E X16(雙向) BANDWITH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

Gigabyte Technology		
Title	PCI EXPRESS * 16	
Size: Custom	Document Number: GA-EP43-UD3L	Rev: 1.1
Date: Friday, April 24, 2009	Sheet 18 of 36	



Gigabyte Technology		
Title	ICH9-PCI, DMI, LAN, USB	
Size B	Document Number GA-EP43-UD3L	Rev 1.1
Date: Friday, April 24, 2009	Sheet 19 of 36	


ICH9
(4/6)
LPC
HDA
LAN
RTC
SMB
SPI
MISC
ICHD
AF82801JB-A0/BGA676/[10HB1-038280-G0R]
3VDUAL
MB_ID1=high
FOR FSB1.2V
MB_ID1=LOW
FOR FSB1.1V
GPIO24 PULL DOWN
H/W RESET
FOR ICH7R POWER ON 瞬間會HIGH 到1.8V 之後0V,必須PULL DOWN 1K/6
RB 必須放在BAT外
The RC time delay=18ms~25ms
Remove when DRAMPWROK apply
A_SO/A_SYC
Both PU for one X4 PCIE(1~4)
Both NC for four X1 PCIE(1~4)
Gigabyte Technology
ICH9 GPIO, CTRL
GA-EP43-UD3L
Rev 1.1
Friday, April 24, 2009
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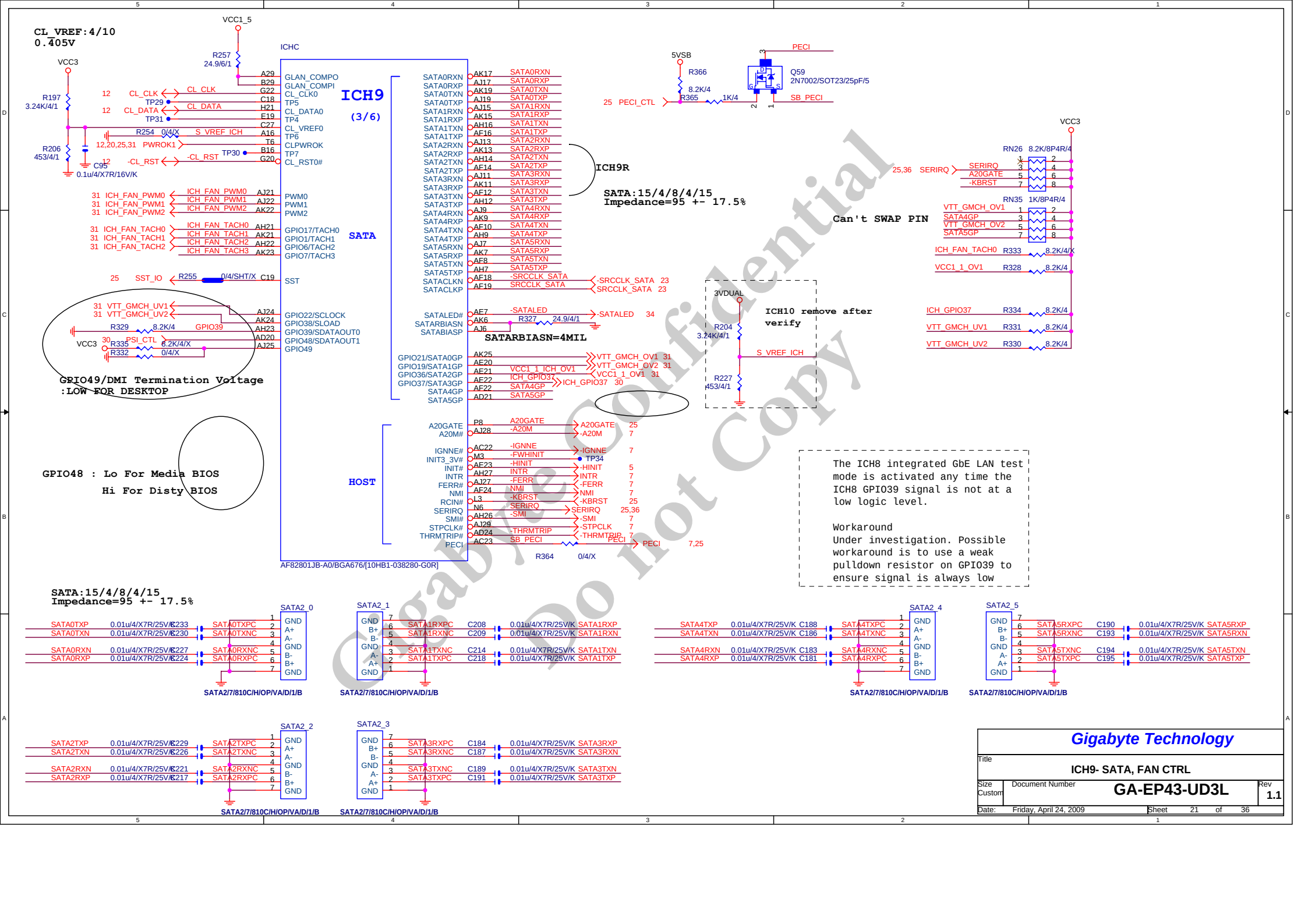
Do not Copy


CL_VREF:4/10
0.405V
ICHC
ICH9
(3/6)
ICH9R
SATA:15/4/8/4/15
Impedance=95 +- 17.5%
Can't SWAP PIN
SATA
HOST
SATARBIASN=4MIL
ICH10 remove after verify
GPIO49/DMI Termination Voltage
:LOW FOR DESKTOP
GPIO48 : Lo For Media BIOS
Hi For Disty BIOS
The ICH8 integrated GbE LAN test mode is activated any time the ICH8 GPIO39 signal is not at a low logic level.
Workaround
Under investigation. Possible workaround is to use a weak pulldown resistor on GPIO39 to ensure signal is always low
AF82801JB-A0/BGA676/[10HB1-038280-G0R]
SATA2/7/810C/H/OP/VA/D/1/B
Gigabyte Technology
ICH9- SATA, FAN CTRL
GA-EP43-UD3L
Rev 1.1
Friday, April 24, 2009
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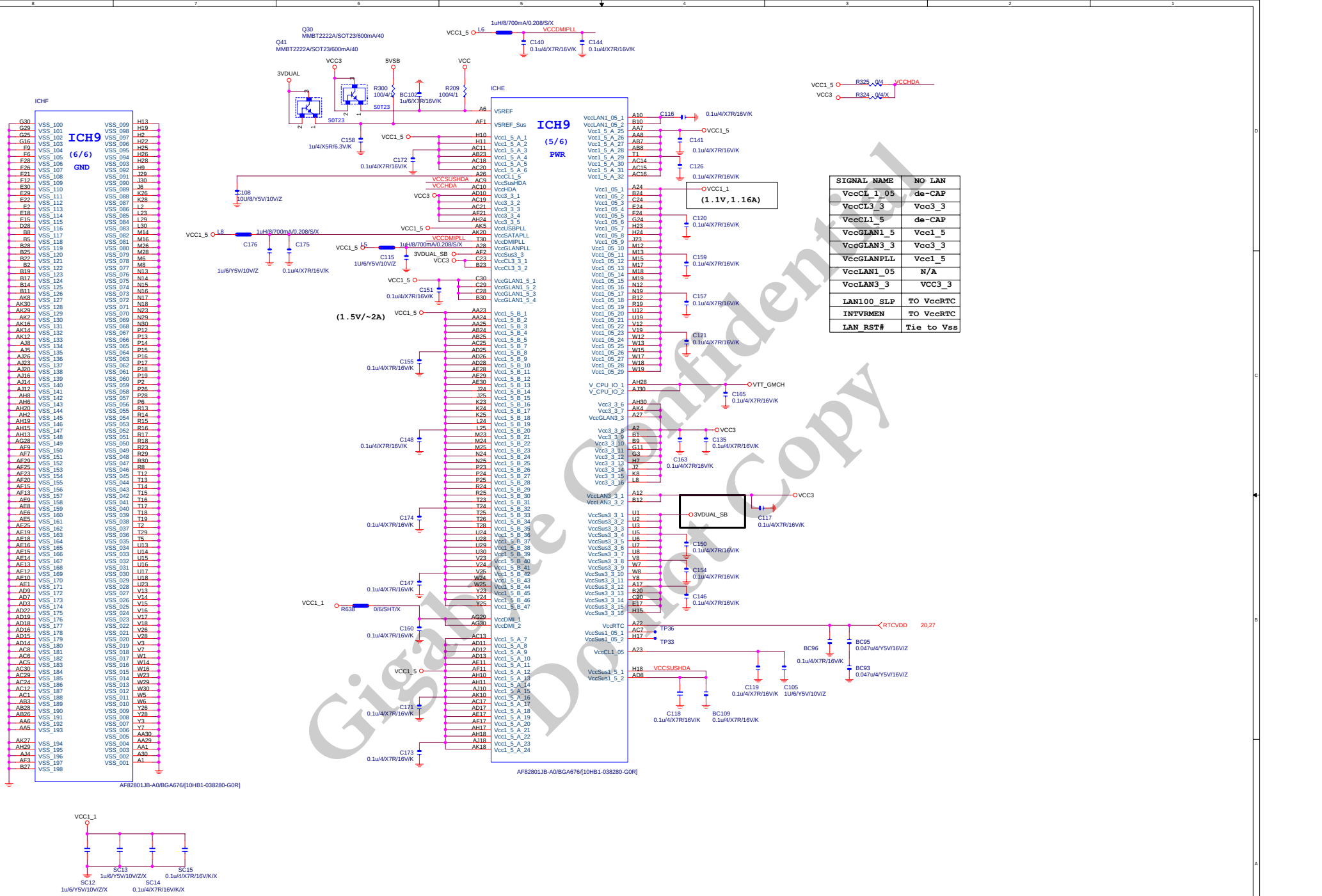
Do not Copy


ICH9
(6/6)
GND
ICHF
AF82801JB-A0/BGA676/[10HB1-038280-G0R]
ICH9
(5/6)
PWR
ICHE
AF82801JB-A0/BGA676/[10HB1-038280-G0R]
(1.5V/~2A)
(1.1V,1.16A)
Q30
MMBT2222A/SOT23/600mA/40
Q41
MMBT2222A/SOT23/600mA/40
3VDUAL
VCC3
5VSB
VCC
VCC1_5
VCC1_1
VCCDMIPLL
VCCSUSHDA
VCCHDA
VCCDMIPLL
3VDUAL_SB
VTT_GMCH
RTCVDD
20,27
SIGNAL NAME | NO LAN
VccCL1_05 | de-CAP
VccCL3_3 | Vcc3_3
VccCL1_5 | de-CAP
VccGLAN1_5 | Vcc1_5
VccGLAN3_3 | Vcc3_3
VccGLANPLL | Vcc1_5
VccLAN1_05 | N/A
VccLAN3_3 | VCC3_3
LAN100_SLP | TO VccRTC
INTVRMEN | TO VccRTC
LAN_RST# | Tie to Vss
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Gigabyte Technology
Title
ICH9-PWR & GND
Size C
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GA-EP43-UD3L
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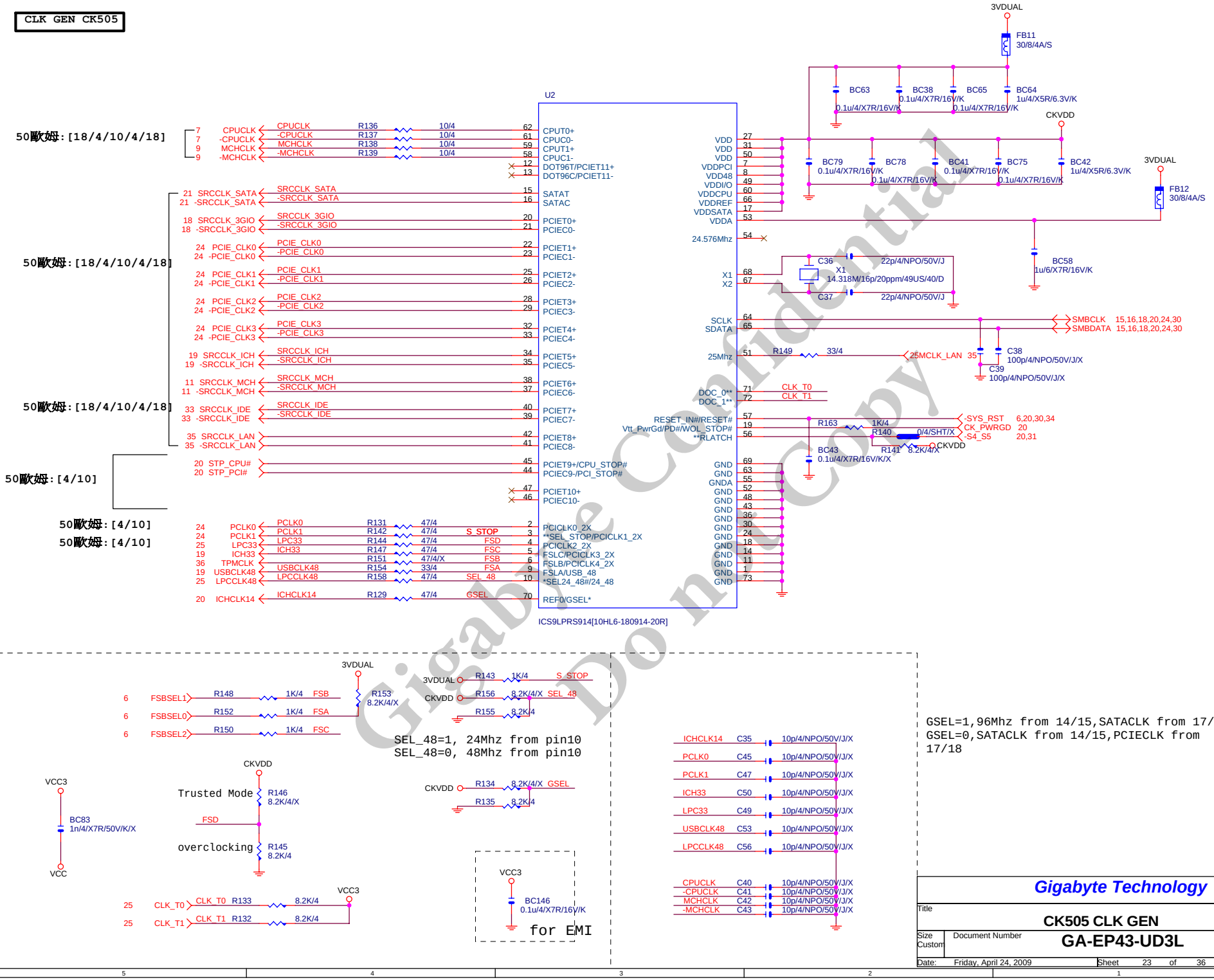
CLK GEN CK505



GSEL=1,96Mhz from 14/15,SATACLK from 17/18
GSEL=0,SATACLK from 14/15,PCIECLK from 17/18

Gigabyte Technology

Title	CK505 CLK GEN	
Size: Custom	Document Number: GA-EP43-UD3L	Rev: 1.1
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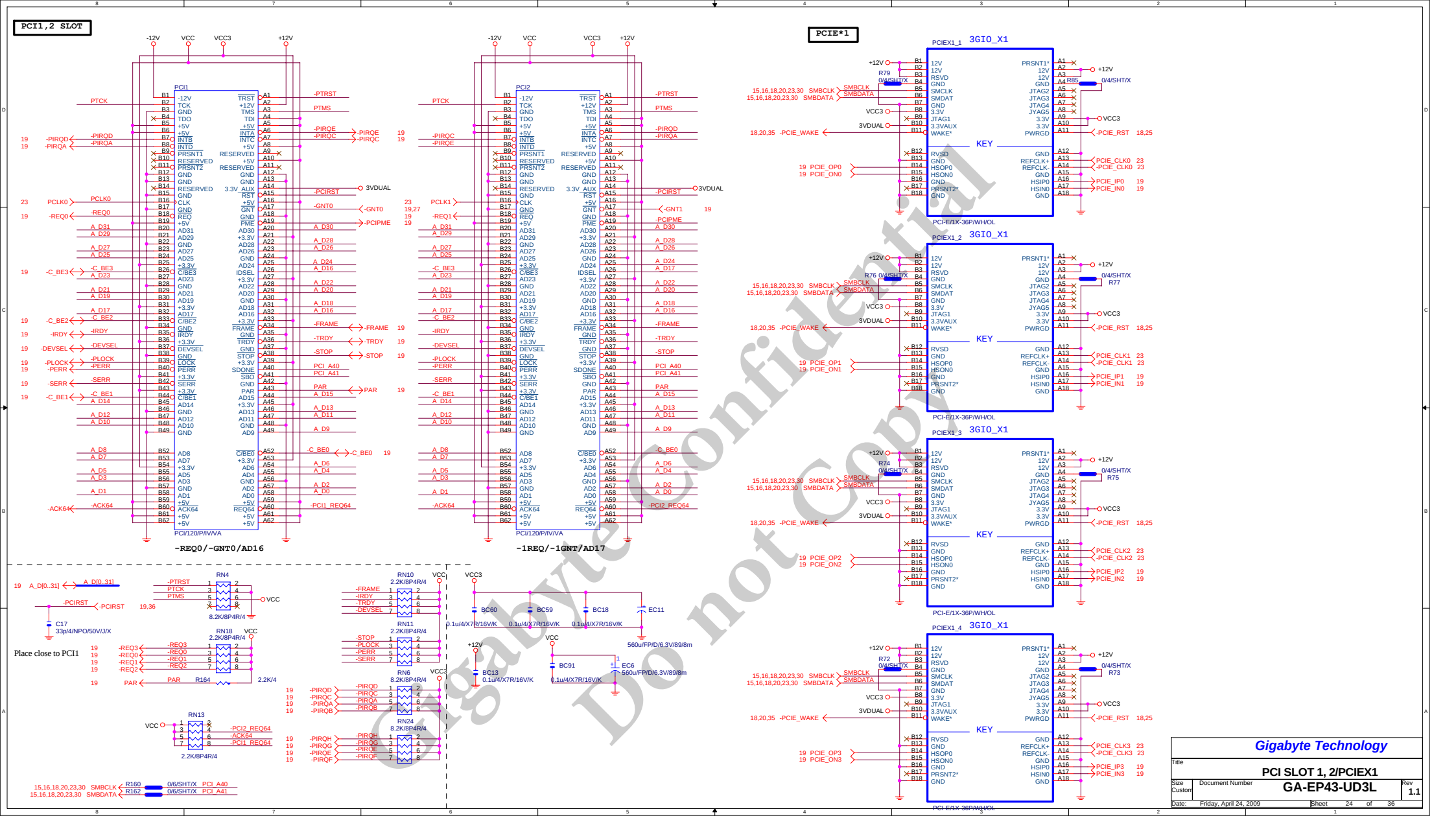
PCI1,2 SLOT
PCI1
PCI2
PCI120/P/IV/VA
-REQ0/-GNT0/AD16
-1REQ/-1GNT/AD17
PCIE*1
PCIEX1_1 3GIO_X1
PCIEX1_2 3GIO_X1
PCIEX1_3 3GIO_X1
PCIEX1_4 3GIO_X1
PCI-E/1X-36P/WH/OL
KEY
Place close to PCI1
Gigabyte Technology
PCI SLOT 1, 2/PCIEX1
GA-EP43-UD3L
Rev 1.1
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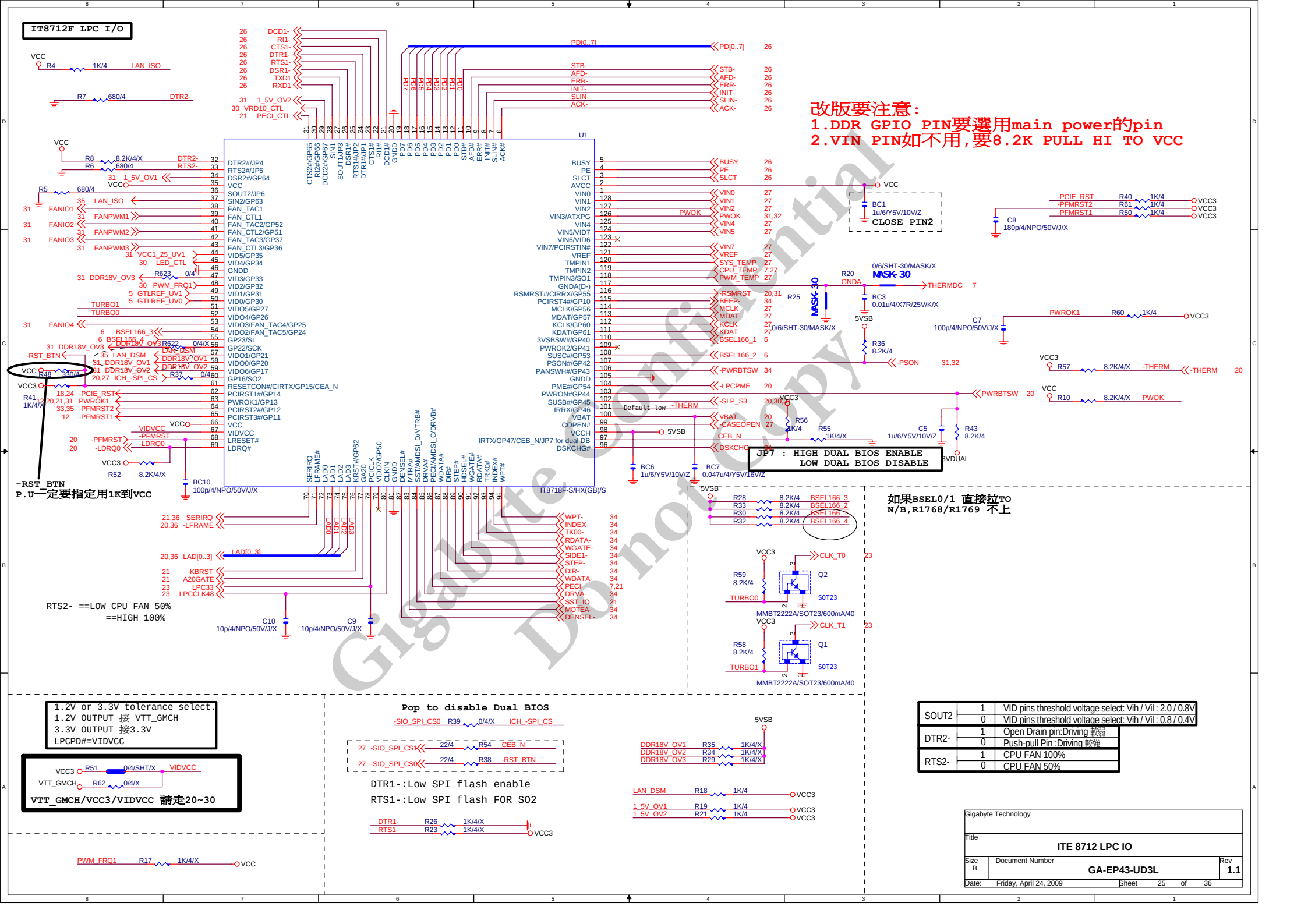
Do not Copy


IT8712F LPC I/O
改版要注意:
1.DDR GPIO PIN要選用main power的pin
2.VIN PIN如不用,要8.2K PULL HI TO VCC
U1
IT8718F-S/HX(GB)/S
CLOSE PIN2
JP7 : HIGH DUAL BIOS ENABLE
LOW DUAL BIOS DISABLE
-RST_BTN
P.U一定要指定用1K到VCC
如果BSEL0/1 直接拉TO
N/B,R1768/R1769 不上
RTS2- ==LOW CPU FAN 50%
==HIGH 100%
1.2V or 3.3V tolerance select.
1.2V OUTPUT 接 VTT_GMCH
3.3V OUTPUT 接3.3V
LPCPD#=VIDVCC
VTT_GMCH/VCC3/VIDVCC 請走20~30
Pop to disable Dual BIOS
DTR1-:Low SPI flash enable
RTS1-:Low SPI flash FOR SO2
SOUT2
DTR2-
RTS2-
Gigabyte Technology
ITE 8712 LPC IO
GA-EP43-UD3L
1.1
Friday, April 24, 2009
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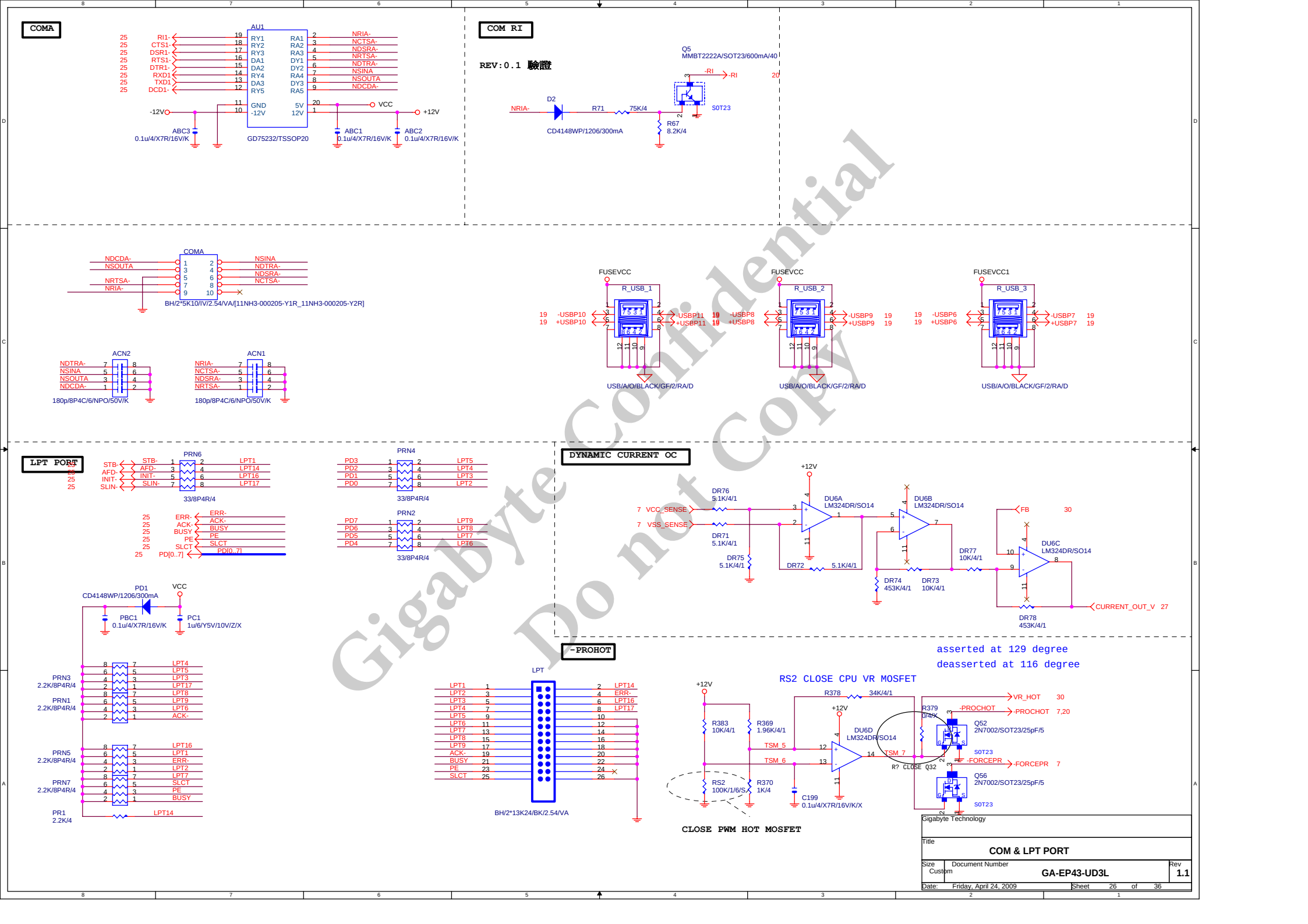
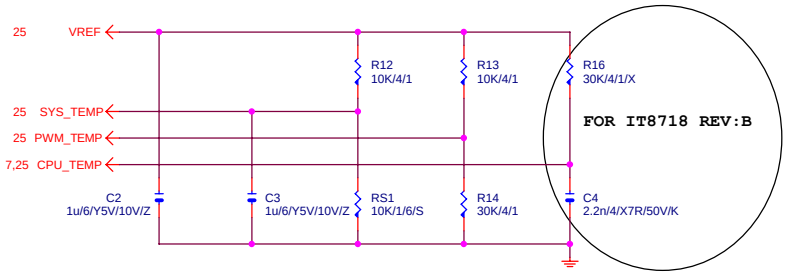
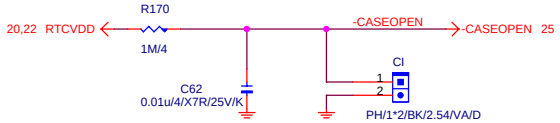
Gigabyte Confidential
Do not Copy



TEMP H/W MONITOR

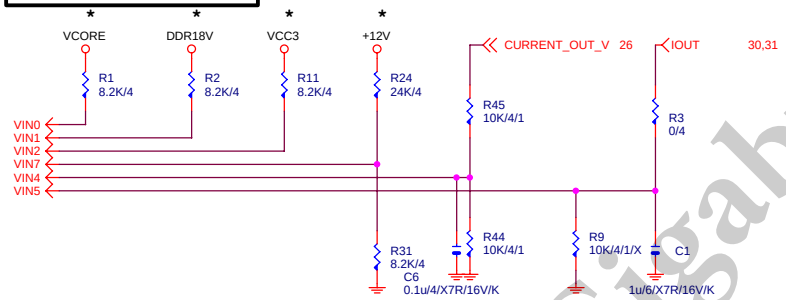


CASE OPEN

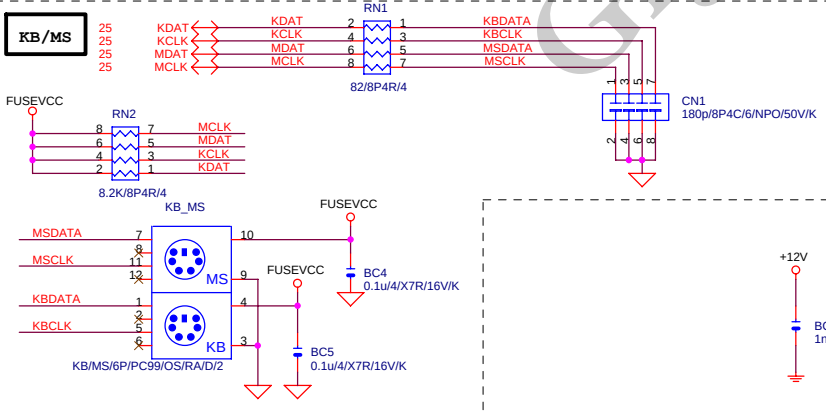


Case Open Circuits

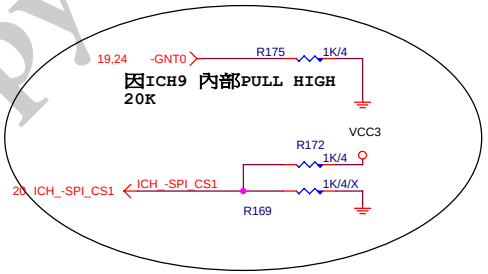
VOLTAGE-- H/W MONITOR

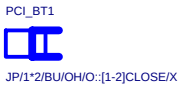


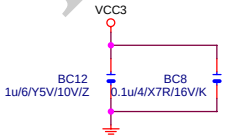
KB/MS

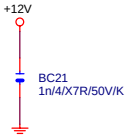


BOOT DEVICE	GNT0	CS1
SPI	0	1
PCI	1	0
FWH	1	1









Gigabyte Technology

Title: BIOS/HW-MONITOR/CI/KB/MS

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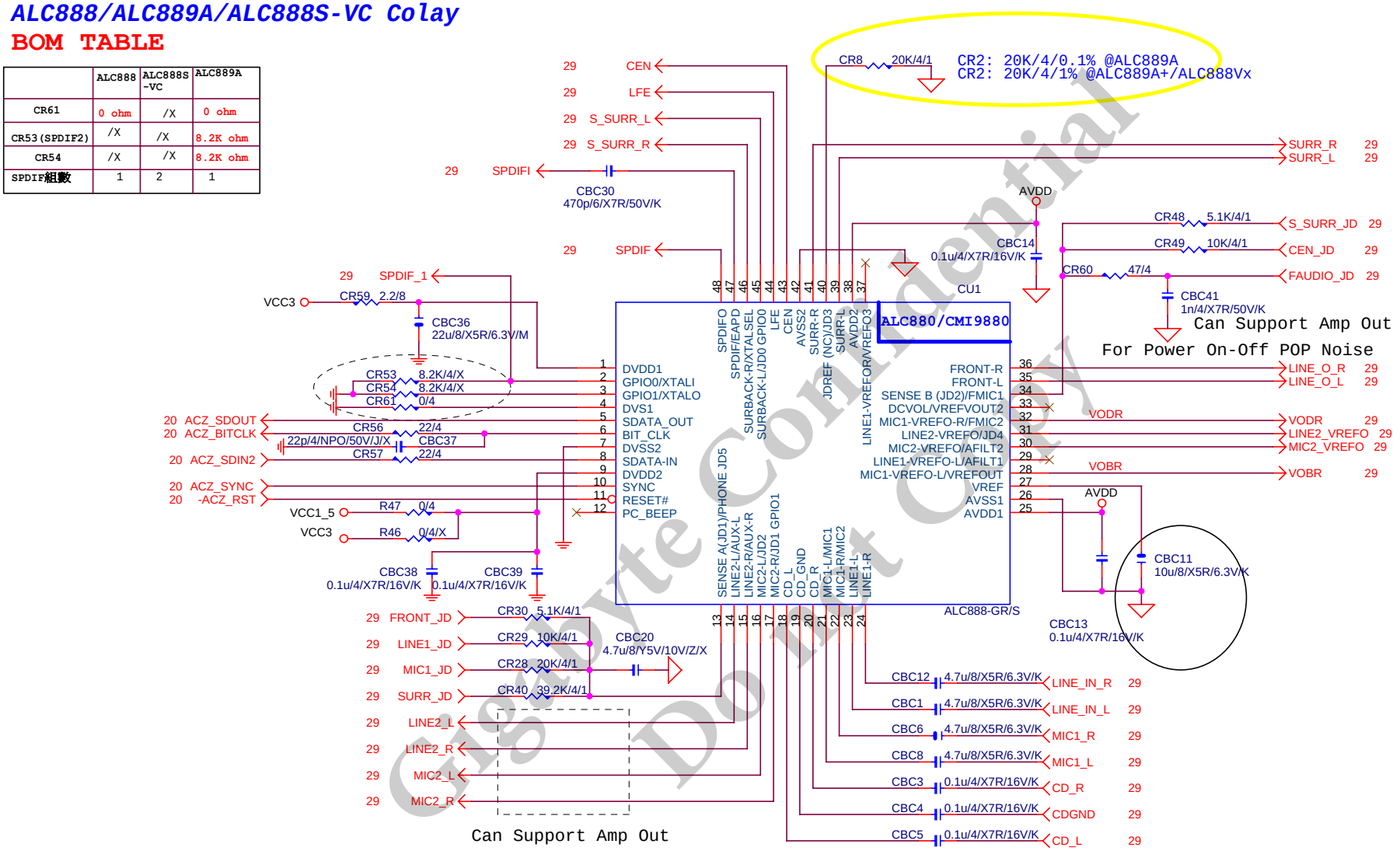
AZALIA CODEC

ALC888/ALC889A/ALC888S-VC Colay

BOM TABLE

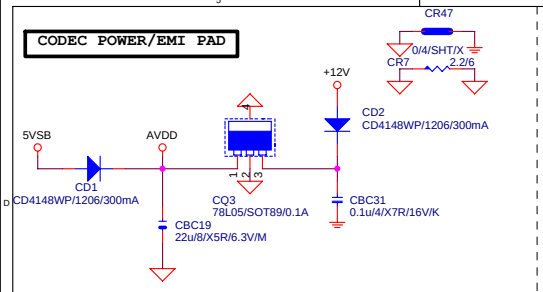
	ALC888	ALC888S-VC	ALC889A
CR61	0 ohm	/X	0 ohm
CR53(SPDIF2)	/X	/X	8.2K ohm
CR54	/X	/X	8.2K ohm
SPDIF組數	1	2	1



20 ACZ_SDOUT
20 ACZ_SYNC
20 -ACZ_RST
20 ACZ_BITCLK
20 ACZ_SDIN2

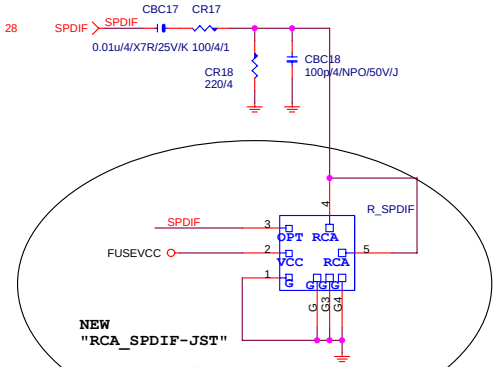
Gigabyte Technology			
Title: ALC888			
Size: Custom	Document Number: GA-EP43-UD3L		Rev: 1.1
Date: Friday, April 24, 2009		Sheet 28 of 36	

CODEC POWER/EMI PAD



CO-LAYOUT

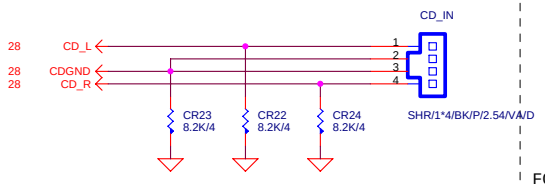
Fpr
EMI



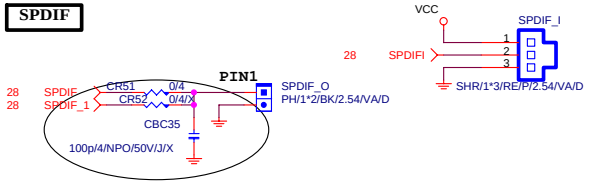
FOR DS3L
11NR6-402030-41R(無鐵殼)11NR6-402030-51R/52R(鐵殼)

FOR S3L 11NR6-501004-G1R ONLY support RCA

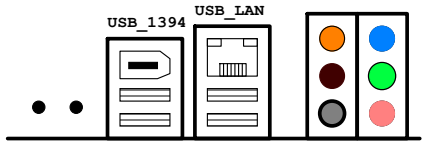
CD IN



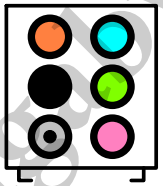
SPDIF



AZALIA JACK

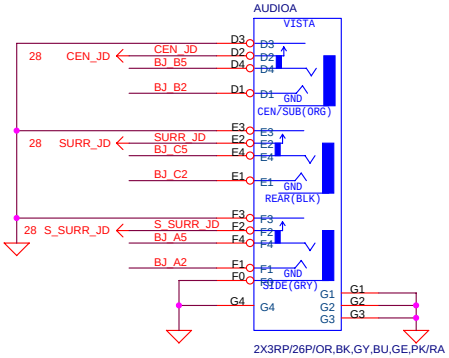


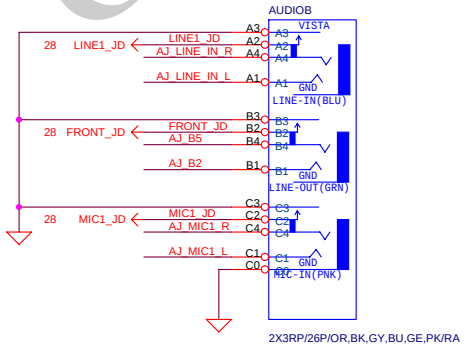
BTX AZALIA CONNECTOR



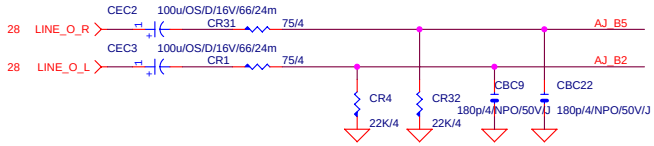
3RP/26P/OR,BK,GY,BU,GE,PK/RA/D/1/B

VISTA規範:REAR-->BLK,CEN/SUB-->ORG

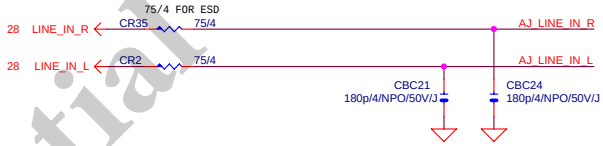




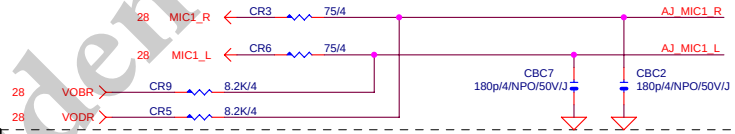
LINE-OUT



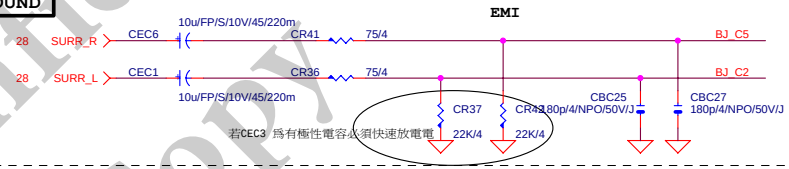
LINE-IN



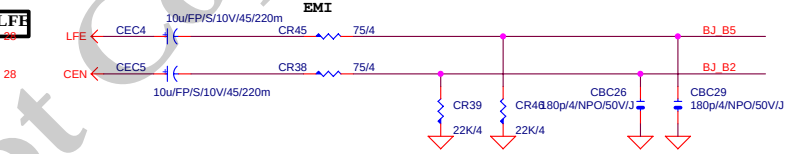
MIC-IN



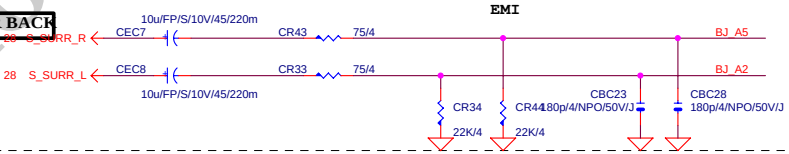
SURROUND



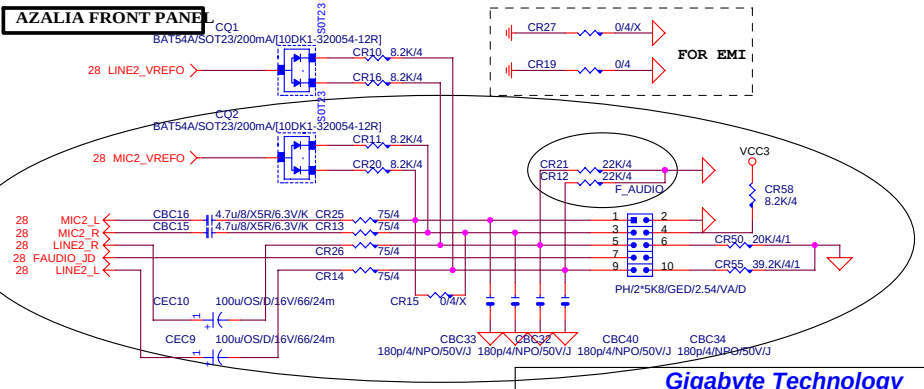
CEN/LFE



SURR BACK

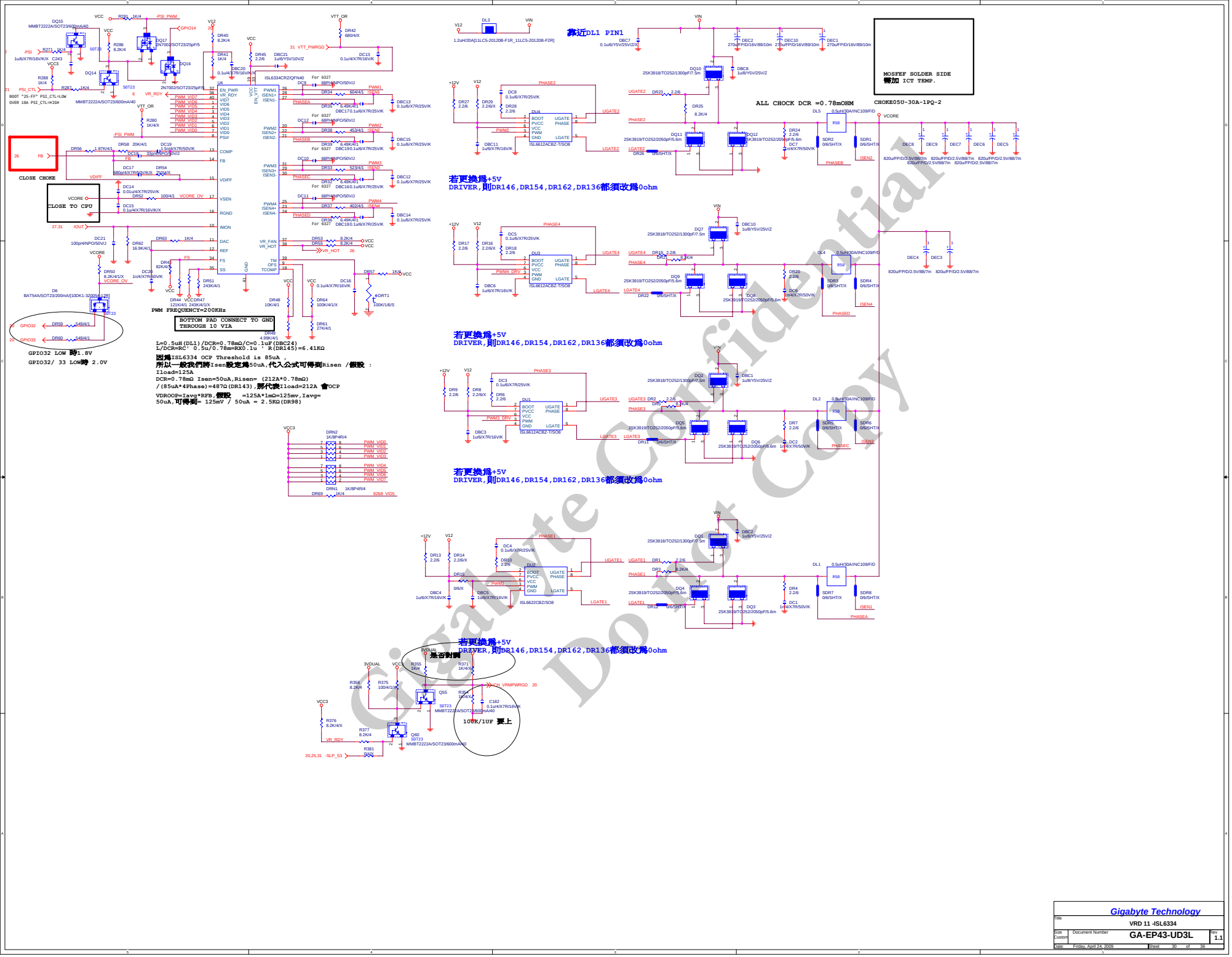


AZALIA FRONT PANEL



Gigabyte Technology

Title	AUDIO JACK	
Size: Custom	Document Number: GA-EP43-UD3L	Rev: 1.1
Date: Friday, April 24, 2009	Sheet 29 of 36	



Gigabyte Technology			
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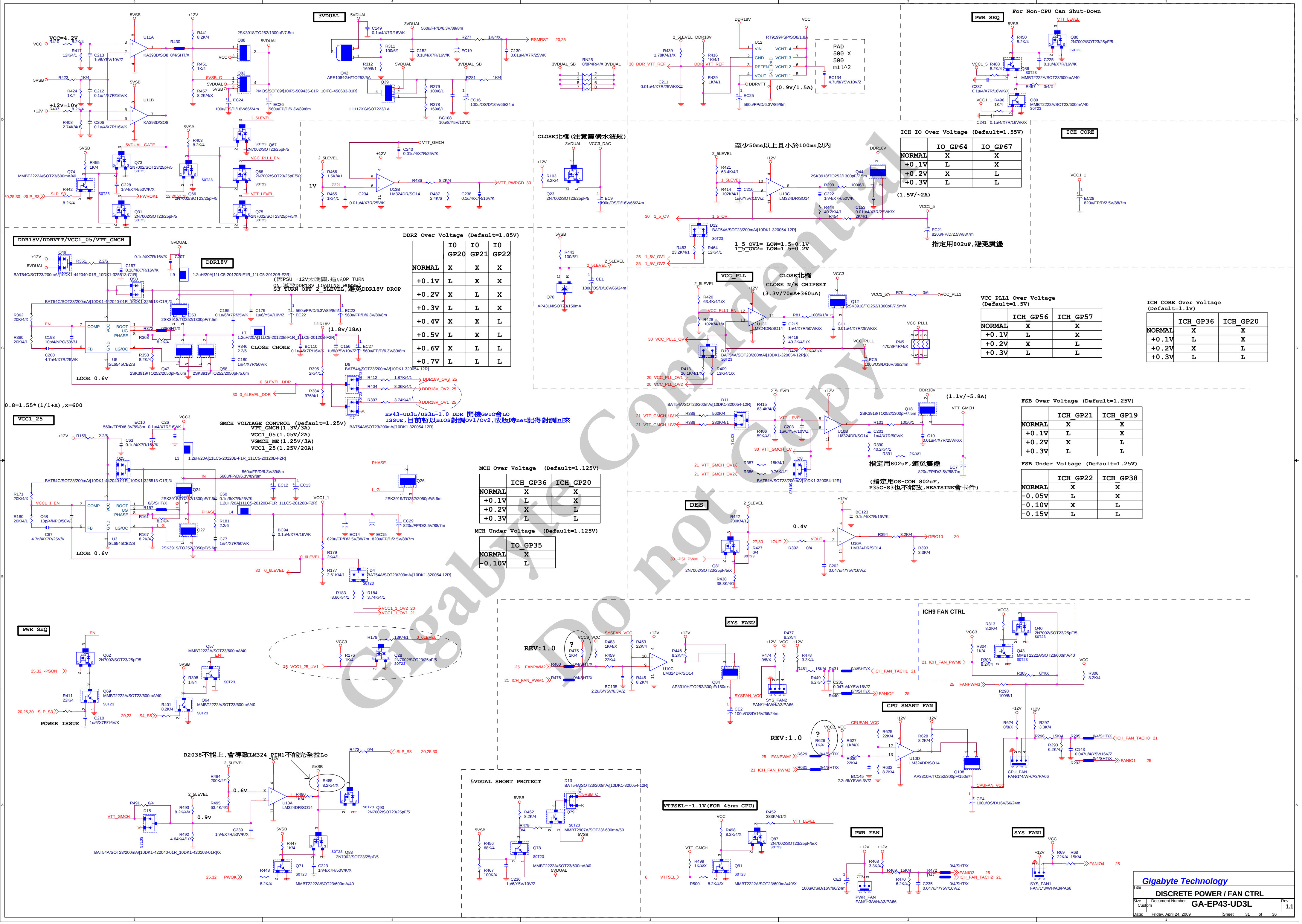
Size: Custom	Document Number: GA-EP43-UD3L		Rev: 1.1
Date: Friday, April 24, 2009	Sheet 30 of 36		



DDR2 Over Voltage (Default=1.85V)

	IO GP20	IO GP21	IO GP22
NORMAL	X	X	X
+0.1V	L	X	X
+0.2V	X	L	X
+0.3V	L	L	X
+0.4V	X	X	L
+0.5V	L	X	L
+0.6V	X	L	L
+0.7V	L	L	L

ICH IO Over Voltage (Default=1.55V)

	IO_GP64	IO_GP67
NORMAL	X	X
+0.1V	L	X
+0.2V	X	L
+0.3V	L	L

VCC_PLL1 Over Voltage (Default=1.5V)

	ICH_GP56	ICH_GP57
NORMAL	X	X
+0.1V	L	X
+0.2V	X	L
+0.3V	L	L

ICH CORE Over Voltage (Default=1.1V)

	ICH_GP36	ICH_GP20
NORMAL	X	X
+0.1V	L	X
+0.2V	X	L
+0.3V	L	L

MCH Over Voltage (Default=1.125V)

	ICH_GP36	ICH_GP20
NORMAL	X	X
+0.1V	L	X
+0.2V	X	L
+0.3V	L	L

MCH Under Voltage (Default=1.125V)

	IO_GP35
NORMAL	X
-0.10V	L

FSB Over Voltage (Default=1.25V)

	ICH_GP21	ICH_GP19
NORMAL	X	X
+0.1V	L	X
+0.2V	X	L
+0.3V	L	L

FSB Under Voltage (Default=1.25V)

	ICH_GP22	ICH_GP38
NORMAL	X	X
-0.05V	L	X
-0.10V	X	L
-0.15V	L	L

Gigabyte Technology

Title: DISCRETE POWER / FAN CTRL

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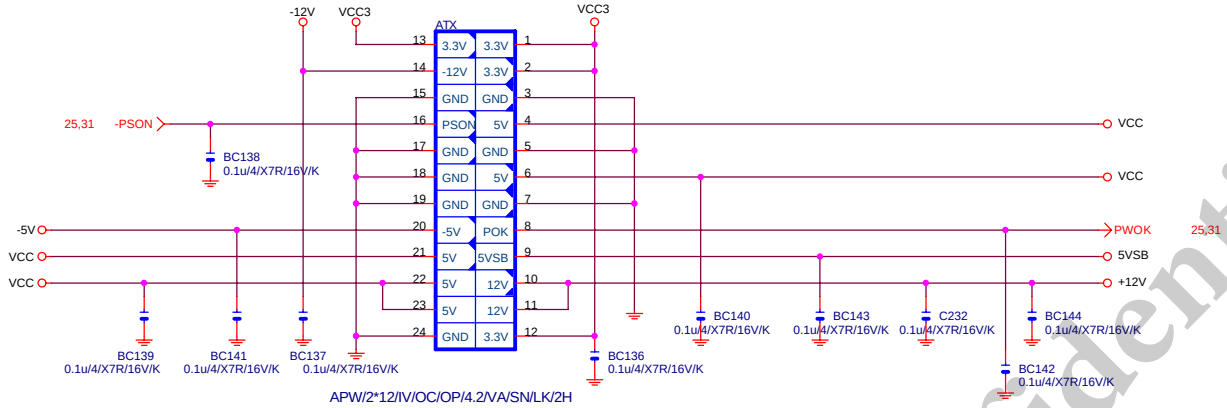
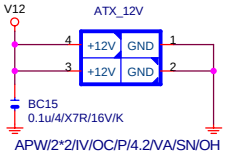
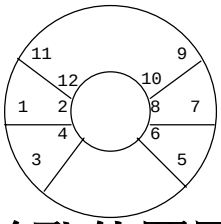
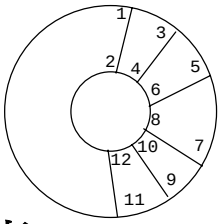
ATX POWER CONNECTOR

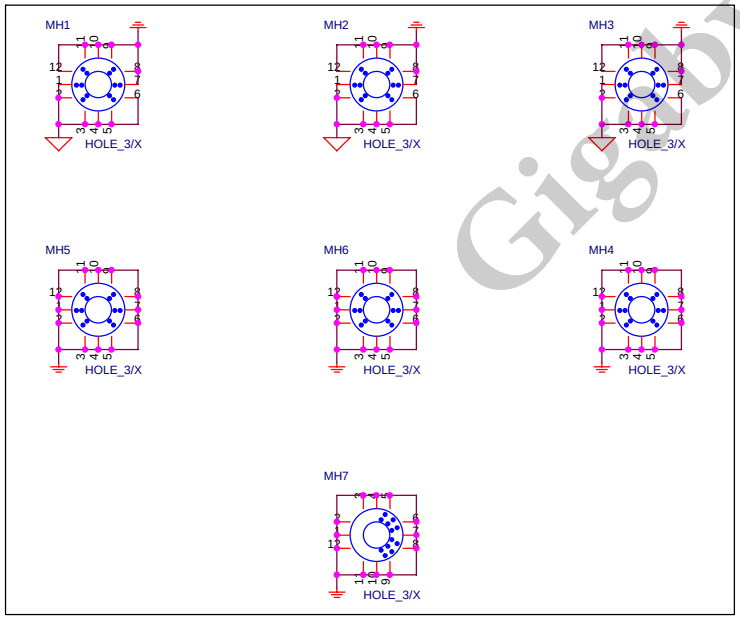


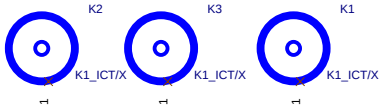


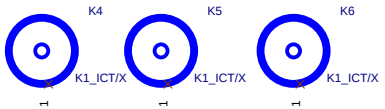


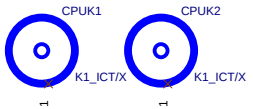


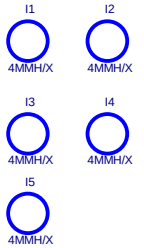
螺絲孔位置圖 (注意Footprint不同)











Gigabyte Technology			
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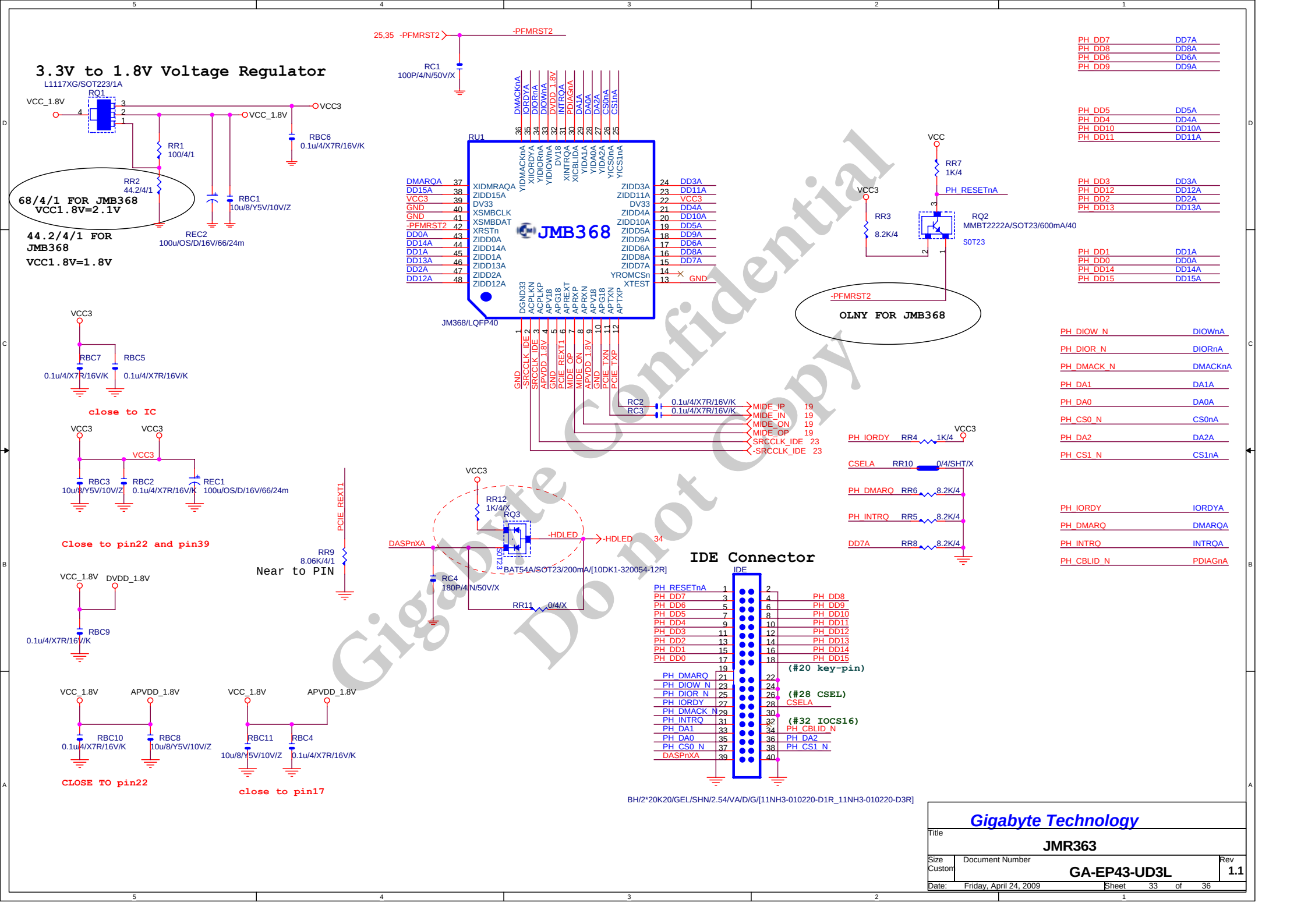
3.3V to 1.8V Voltage Regulator
L1117XG/SOT223/1A
RQ1
VCC_1.8V
VCC3
RR1 100/4/1
RR2 44.2/4/1
RBC6 0.1u/4/X7R/16V/K
RBC1 10u/8/Y5V/10V/Z
REC2 100u/OS/D/16V/66/24m
68/4/1 FOR JMB368
VCC1.8V=2.1V
44.2/4/1 FOR JMB368
VCC1.8V=1.8V
25,35 -PFMRST2
RC1 100P/4/N/50V/X
RU1
JMB368
JM368/LQFP40
DMARQA
DD15A
VCC3
GND
-PFMRST2
DD0A
DD14A
DD1A
DD13A
DD2A
DD12A
XIDMRAQA
ZIDD15A
DV33
XSMBCLK
XSMBDAT
XRSTn
ZIDD0A
ZIDD14A
ZIDD1A
ZIDD13A
ZIDD2A
ZIDD12A
ZIDD3A
ZIDD11A
ZIDD4A
ZIDD10A
ZIDD5A
ZIDD9A
ZIDD6A
ZIDD8A
ZIDD7A
YROMCSn
XTEST
DD3A
DD11A
DD4A
DD10A
DD5A
DD9A
DD6A
DD8A
DD7A
GND
VCC
RR7 1K/4
PH_RESETnA
RR3 8.2K/4
RQ2 MMBT2222A/SOT23/600mA/40
S0T23
OLNY FOR JMB368
PH_DD7 DD7A
PH_DD8 DD8A
PH_DD6 DD6A
PH_DD9 DD9A
PH_DD5 DD5A
PH_DD4 DD4A
PH_DD10 DD10A
PH_DD11 DD11A
PH_DD3 DD3A
PH_DD12 DD12A
PH_DD2 DD2A
PH_DD13 DD13A
PH_DD1 DD1A
PH_DD0 DD0A
PH_DD14 DD14A
PH_DD15 DD15A
RBC7 0.1u/4/X7R/16V/K
RBC5 0.1u/4/X7R/16V/K
close to IC
RBC3 10u/8/Y5V/10V/Z
RBC2 0.1u/4/X7R/16V/K
REC1 100u/OS/D/16V/66/24m
Close to pin22 and pin39
RR9 8.06K/4/1
Near to PIN
PCIE_REXT1
RC2 0.1u/4/X7R/16V/K
RC3 0.1u/4/X7R/16V/K
MIDE_IP 19
MIDE_IN 19
MIDE_ON 19
MIDE_OP 19
SRCCLK_IDE 23
-SRCCLK_IDE 23
PH_IORDY RR4 1K/4
CSELA RR10 0/4/SHT/X
PH_DMARQ RR6 8.2K/4
PH_INTRQ RR5 8.2K/4
DD7A RR8 8.2K/4
PH_DIOW_N DIOWnA
PH_DIOR_N DIORnA
PH_DMACK_N DMACKnA
PH_DA1 DA1A
PH_DA0 DA0A
PH_CS0_N CS0nA
PH_DA2 DA2A
PH_CS1_N CS1nA
PH_IORDY IORDYA
PH_DMARQ DMARQA
PH_INTRQ INTRQA
PH_CBLID_N PDIAGnA
RR12 1K/4/X
RQ3
-HDLED
DASPnXA
RC4 180P/4/N/50V/X
RR11 0/4/X
BAT54A/SOT23/200mA/[10DK1-320054-12R]
IDE Connector
IDE
PH_RESETnA
PH_DD7
PH_DD6
PH_DD5
PH_DD4
PH_DD3
PH_DD2
PH_DD1
PH_DD0
PH_DD8
PH_DD9
PH_DD10
PH_DD11
PH_DD12
PH_DD13
PH_DD14
PH_DD15
(#20 key-pin)
PH_DMARQ
PH_DIOW_N
PH_DIOR_N
PH_IORDY
PH_DMACK_N
PH_INTRQ
PH_DA1
PH_DA0
PH_CS0_N
DASPnXA
(#28 CSEL)
CSELA
(#32 IOCS16)
PH_CBLID_N
PH_DA2
PH_CS1_N
BH/2*20K20/GEL/SHN/2.54/VA/D/G/[11NH3-010220-D1R_11NH3-010220-D3R]
RBC9 0.1u/4/X7R/16V/K
RBC10 0.1u/4/X7R/16V/K
RBC8 10u/8/Y5V/10V/Z
CLOSE TO pin22
RBC11 10u/8/Y5V/10V/Z
RBC4 0.1u/4/X7R/16V/K
close to pin17
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Title
JMR363
Size Custom
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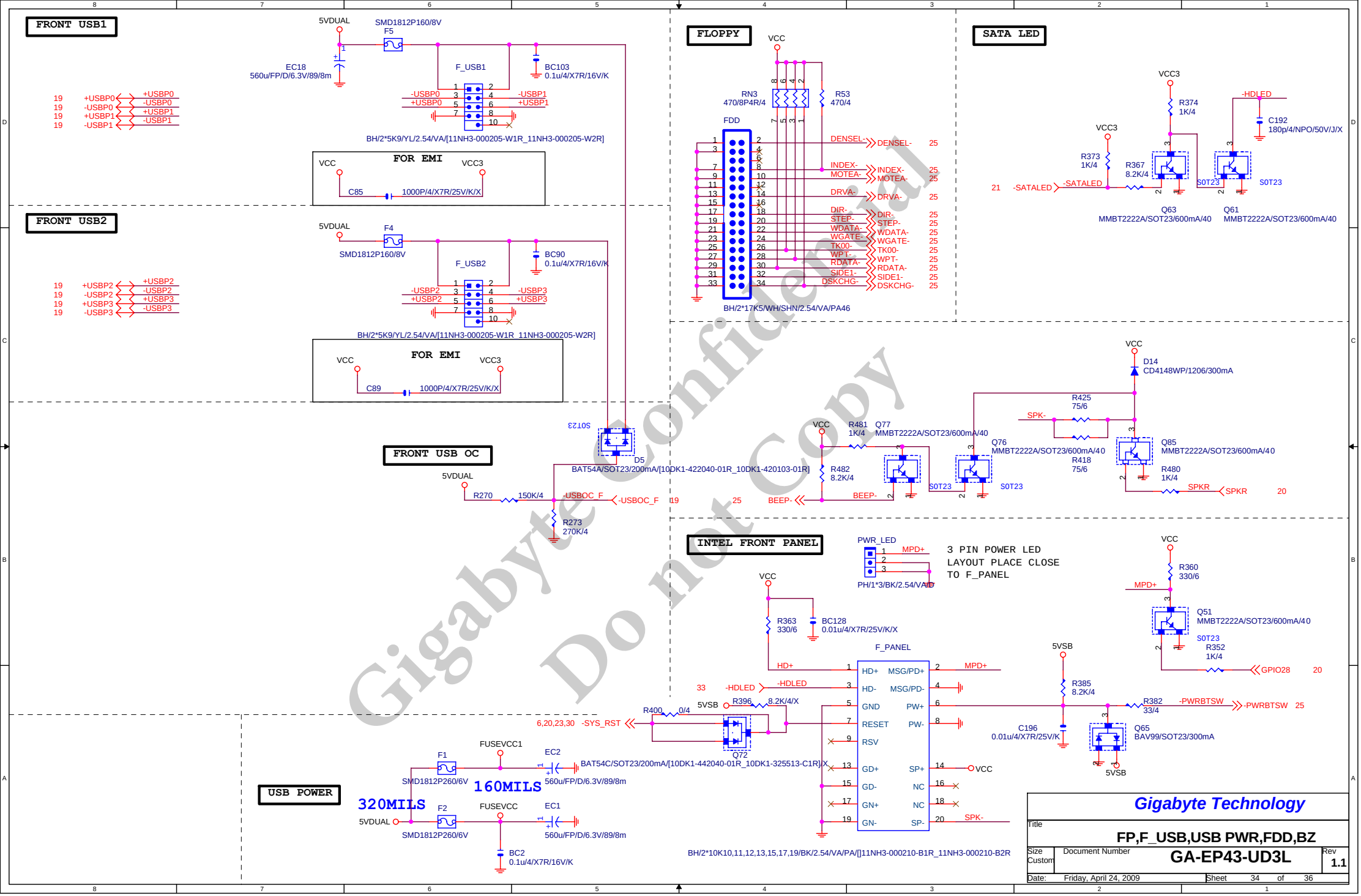

PCIE-1G LAN

XTALI_P
LX1
XTALO_P
25M/20p/30ppm/49US/20/D/X
LC4 27p/4/NPO/50V/J/X
LC3 27p/4/NPO/50V/J/X
3VDUAL
LR16 0/6
LR15 0/6
RTL8111C:remove LQ1,LQ2,ADD LFB1,LL1,LR23,LR24,LBC61,LBC62
LBC19 0.1u/4/X7R/16V/K
LBC30 22u/8/X5R/6.3V/M
LR7 0/4/X
0.1u/4/X7R/16V/K/X
LBC25
0.1u/4/X7R/16V/K/X
LBC20
23 25MCLK_LAN
LR12 0/4
LC5 10p/4/NPO/50V/J/X
LR6 2.49K/4/1
LED_ACT_TXRX
LED_LINK100
LED_LINK1000
LAN_DSM 25
LR3 0/4
LR2 100/4/X
LU1
RTL8111C-VCO-GR/QFN64
CTRL18
AVDD33
P_MDI0+
P_MDI0-
FB12
P_MDI1+
P_MDI1-
AVDD18
P_MDI2+
P_MDI2-
AVDD18
P_MDI3+
P_MDI3-
AVDD18
VDD15
3VDUAL
EGND
EESK
EEDI_AUX
3VDUAL
EEDO
EECS
VDD15
VDD15
VDD15
3VDUAL
ISOLATEB
VDD15
LR1 0/4/X
VCC3
LR13 1K/4
LR14 15K/4
LD2 BAT54C/SOT23/200mA/[10DK1-442040-01R_10DK1-325513-C1R]
25 LAN_ISO
18,20,24 -PCIE_WAKE
25,33 -PFMRST2
100歐姆:[20/5/7/5/20]
19 ML_OP
19 ML_ON
23 SRCCLK_LAN
23 -SRCCLK_LAN
19 ML_IP
19 ML_IN
LC2 0.1u/4/X7R/16V/K
LC1 0.1u/4/X7R/16V/K
50歐姆:[18/4/10/4/18]
-PFMRST2
LBC5 100p/4/NPO/50V/J
LED_GREEN
LR20 0/6/SHT/X
LED_LINK100
R1.0 10M LED OFF

Dual Color LED
D4 D3 Green
D4 D3 Orange
Single Color LED
D2 D1 Yellow

P35-152-19W9
U4 U3 U2 U1
U8 U7 U6 U5
L1 L3 L5 L7 L9
L2 L4 L6 L8 L10
D1 D2 D3 D4
YELLOW
ORANGE (+,-)
GREEN (-,+)

Power domain chart

	RTL8111B / RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
DVDD15	1.5V	1.2V

3VDUAL
LEC2 100u/OS/D/16V/66/24m
LBC32 0.1u/4/X7R/16V/K
LBC28 0.1u/4/X7R/16V/K
LBC18 0.1u/4/X7R/16V/K
LBC23 0.1u/4/X7R/16V/K

3VDUAL
LFB1 0/8/SHT/X
LBC6 0.1u/4/X7R/16V/K
LBC15 4.7u/8/Y5V/10V/Z/X
LBC7 0.1u/4/X7R/16V/K
VDD15
LQ1 BCP69/SOT223/-1A/60/X
CTRL15
LRT1 0/4/X
LD1 MMSZ5227B/SOD123/3.6V/X
VDD15
AVDD18
LFB3 0/8
LEC1 100u/OS/D/16V/66/24m
LBC1 4.7u/8/Y5V/10V/Z/X
LBC22 0.1u/4/X7R/16V/K
LBC17 0.1u/4/X7R/16V/K
LBC8 0.1u/4/X7R/16V/K
LBC13 0.1u/4/X7R/16V/K
LBC21 0.1u/4/X7R/16V/K
LBC4 0.1u/4/X7R/16V/K

3VDUAL
AVDD33
LFB4 0/8/SHT/X
LBC11 0.1u/4/X7R/16V/K
LBC29 4.7u/8/Y5V/10V/Z
LBC24 0.1u/4/X7R/16V/K
AVDD18
LQ2 25B1132/SOT89/-1A/82/X
AVDD18
LR5 0/4
LL1 4.7uH/0.5A/2520/S
FB12
CTRL18
VDD18
LBC31 22u/8/X5R/6.3V/M
LFB2 0/8
AVDD18
LBC3 0.1u/4/X7R/16V/K
LBC2 0.1u/4/X7R/16V/K
LBC12 4.7u/8/Y5V/10V/Z
LBC9 0.1u/4/X7R/16V/K
LBC16 0.1u/4/X7R/16V/K
LEC3 100u/OS/D/16V/66/24m
LBC10 0.1u/4/X7R/16V/K

LR10 8.2K/4/X
3VDUAL
LU2
EECS
EESK
EEDI_AUX
EEDO
CS VCC
SK DC
DI ORG
DO GND
AT93C46-10SU-2.7/S/X
LBC14 0.1u/4/X7R/16V/K
LR9 3.6K/4
3VDUAL

USB_LAN CONNECTOR

LAN 100歐姆:[30/4/8/4/30] FOR B 製程
USB_LAN
LBC27 100p/4/NPO/50V/J/X
P_MDI0+
P_MDI0-
P_MDI1+
P_MDI1-
P_MDI2+
P_MDI2-
P_MDI3+
P_MDI3-
L1 L2 L3 L4 L5 L6 L7 L8 L9 L10
UP
DOWN
LBC34 100p/4/NPO/50V/J
D1 LED_ACT_TXRX
D2 LR17 150/6
D3 LED_GREEN LR19 150/6
D4 LED_LINK1000 LR18 150/6
U1 U2 U3 U4 U5 U6 U7 U8
-USBP5 +USBP5 -USBP5 19 +USBP5 19
-USBP4 +USBP4 -USBP4 19 +USBP4 19
USB+LAN/1G/GO,Y/OS/RA/D/8C
8 Core

USB POWER

3VDUAL
LFB5 0/6/SHT/X
LBC33 0.1u/4/X7R/16V/K
FUSEVCC1
LBC26 0.1u/4/X7R/16V/K
90歐姆:[15/4.5/7.5/4.5/15]

USB_LAN

LR8 0/4/X
LR4 0/6/SHT/X
SOT23
FUSEVCC FUSEVCC1
D1
BAT54A/SOT23/200mA/[10DK1-422040-01R_10DK1-420103-01R]

REAR USB OC

5VDUAL
R27 150K/4
-USBOC_R
-USBOC_R 19
R22 270K/4

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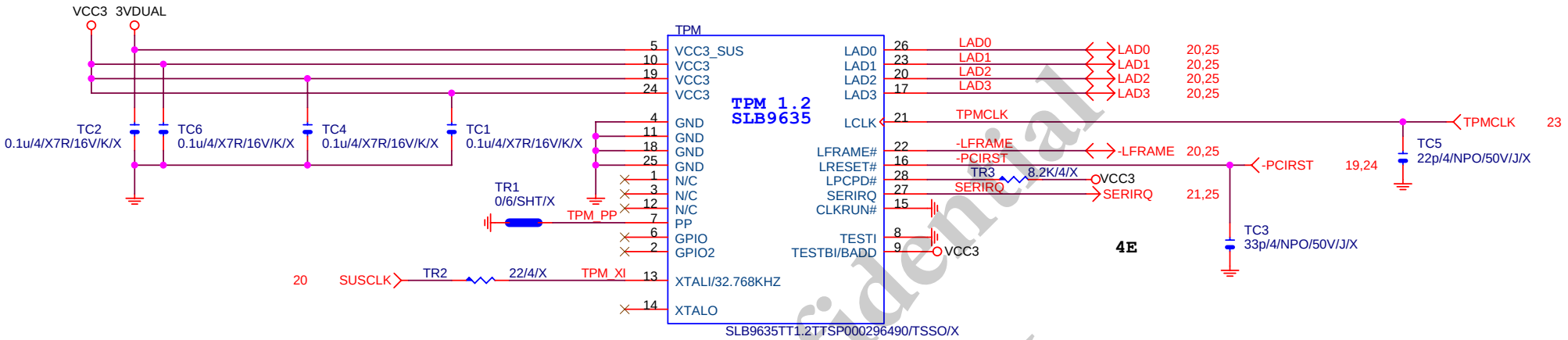

GIGABYTE THCHNOLOGIES		
Title: TPM I/F-SLB 9635 TT 1.2		
Size: Custom	Document Number: GA-EP43-UD3L	Rev: 1.1
Date: Friday, April 24, 2009	Sheet 36 of 36	