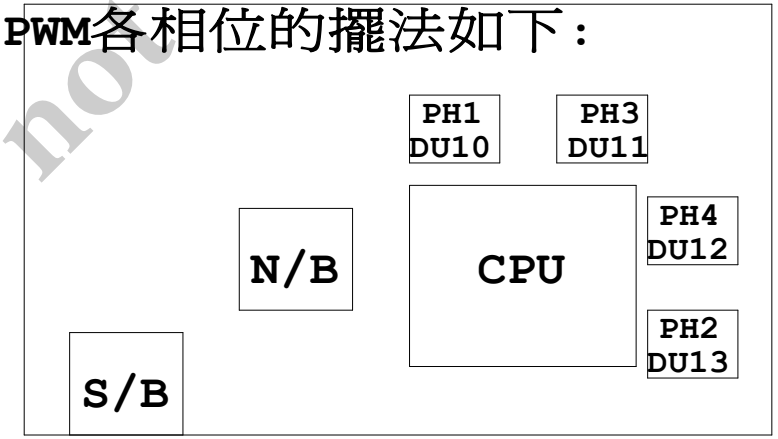
Model Name: EP43-UD3L REV 1.0

SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	TABLE LIST
05	P4_LGA775_A
06	P4_LGA775_B,D
07	P4_LGA775_C
08	P4_L775_E,F,G,H
09	GMCH-Eaglelake_HOST
10	GMCH-Eaglelake_DDRII
11	GMCH-Eaglelake_PCI E, DMI
12	GMCH-Eaglelake_INT VGA
13	GMCH-Eaglelake_GND
14	GMCH-Eaglelake_PWR
15	DDRII CHANNEL A 1,2
16	DDRII CHANNEL B 1,2
17	DDRII TERMINATION
18	PCI EXPRESS*16 SLOT
19	ICH10 DMI, PCI, USB
20	ICH10 GPIO, CTRL
21	ICH10 SATA, FAN PWM
22	ICH10 VCC, GND
23	CLOCK-ICS9LPRS914
24	PCI SLOT 1, 2, PCIEX1_1~4
25	ITE8718/GB,RESET DRIVE
26	COM_LPT, -PROHOT,DYNAMIC,RUSB
27	BIOS,CI,HWM,KB/MS

SHEET	TITLE
28	AZALIA ALC888
29	AUDIO JACK
30	VCORE PWM ISL6334CRZ
31	DISCRETE1 POWER,FAN CTRL
32	ATX POWER
33	JMicron JMB368
34	LAN REALTEK RTL8111C
35	FRONT PANEL,FUSB,FDD
36	TPM I/F-1.2

PWM各相位的擺法如下：



Gigabyte Technology

Title: Cover Sheet

Size: Custom | Document Number: EP43-UD3L | Rev: 1.0

Date: Friday, December 05, 2008 | Sheet 1 of 36

Model Name: GA-EP43-UD3L
Rev:.1.0

Component value change history

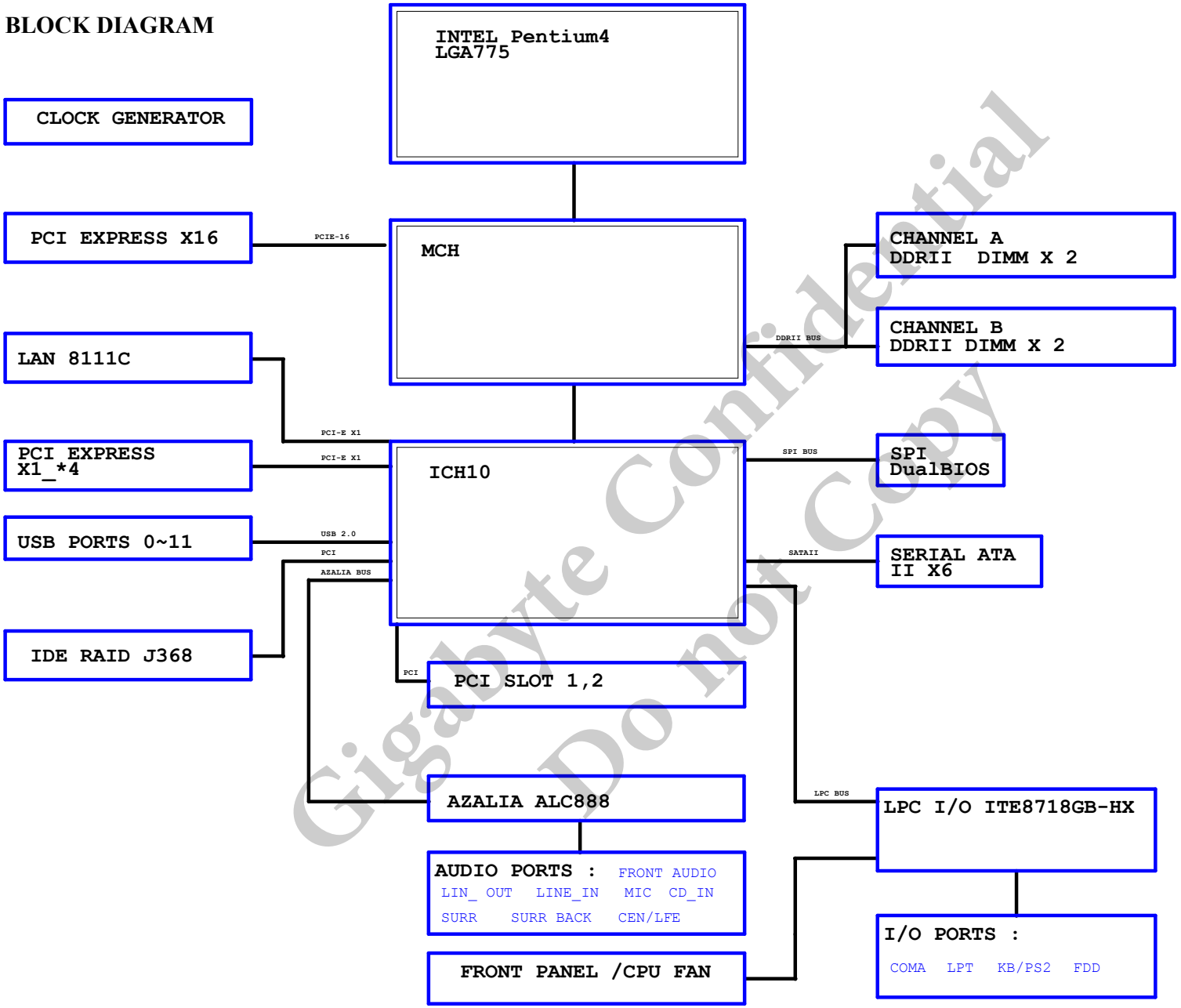
Data	Change Item	Reason
97/04/01 EBOM:01A	1. P43 CHIPSET E-BOM	
97/04/15 EBOM:02	1. 修改LED的OWER及阻值;DEL R484,DR78. ADD DR79,,R348	
	2. ADD DR80,R300 10-->49.9,C158,LBC43 0ohm-->100PF for EMI	
	3. del Q3,Q4,BC11,BC9,R42,R15,PCI_BT1,PCI_BT2,R166,R168	
97/04/28 EBOM:10A	1. DDR2 VOLTAGE 1.83 --> 1.9V --> 2.0V --> 2.1V .....-->2.5V	
97/05/09 PBOM:10B	1. DR59,DR60 14K---->549ohm,del DR69	
	2. ADD U9(uP6262),R436,BC133 FOR CPU 超頻	
97/05/21 PBOM:10C	1.ICH,MCH PCI-E ,JM368的RX,TX串電容BOM 0.1U/Y5V-->0.1U/X7R,RTC RTCVDD -->X7R	
	2.ADD U6 FOR DDR TURN ON 2.1V ISSUE	
97/06/4 PBOM:10D	1.DEL Q107,R620,ADD R621	
	2.Q49(BAT54C) 限用 DII	
97/06/18 PBOM:10E	1.ADD MB_ID R283,DEL R282,Q87,Q91,R452,R498,R499,R500 FOR VTT_GMCH 1.2V	
	2.C197 0.1U/Y5V--->X7R	
	3.R300 49.9--->100 ohm ,C158 Y5V--->X7R for USB	
	4.DC20 0.01u--->1nf FOR CPU PSI ISSUE	
97/08/07 EBOM:20A	1.CPU 改爲SMART FAN	
	2.L4,L7 CHOKE Footprint Change "CHOKE1U2-20A-1PQN"	
	3.獨立南橋1.1V 的電壓	
	4. ADD GPIO37 FOR LOAD LINE CALIBRATION	
	5.J368 改爲1.8V;R209=100 OHM, ADD R640 FOR MB_ID2	
97/08/08 EBOM:30A	1.J368 改爲1.8V;47--->44.2 2.TO252---改爲POWER PACK	
97/10/01 PBOM:10A	FOR EP45-UD3L-1.0	
	1.R183 18K-->9.09K;R184 9.76K--->4.3K 2.DR56 1.74K-->1.87K;DR81 1K--->590 OHM	
	3.DR38 487--->549 ohm 4.R369 2.26K--->1.5K;R378 13.7K--->15.8K	
	4.NB,SB CHANGE HEAT SINK for UD series; PCIEX1 SLOT改爲白色	
	5.RQ3 由BJT改爲 BAT54A FOR -HDLED ISSUE	
97/11/06 PBOM:10A	FOR EP43-UD3L-1.0	
	1.P43 CHIP,HEAT SINK,UPI	

Circuit or PCB layout change for next version

DATE	Change Item	Reason
97/04/01 PCB:0.1	1.P43-DS3L	
97/04/23 PCB:1.0	1. CE3位置請移至EC24左邊	
	2. 增加 upi6262 VCC Power (R620,R621,Q107)	
	3. 增加R622,R623 FOR DDR18V_OV3	
97/07/23 PCB:2.0	1.由1.0 修改,直接改成2.0	
	2.PCIEX16 和PCIEX1_2對調位置	
	3. DDR2_1~DDR2_4往左移,盡量讓MCH的位置在DDR SLOT中間	
	4.ADD CPU SMART FAN CONTROL	
97/07/23 PCB:3.0	1.由2.0 修改	
	2. cpu Vcore MOS TO252改爲POWER PACK	
97/09/16 PCB:1.0	1.由3.0 修改,改文字面 EP45-UD3L ,ULTRA DURABLE 3,NB /SB 框內文字修改	
97/11/06 PCB:1.0	1.由EP45-UD3L改文字面成EP43-UD3L	
	2.DEL ICH CORE 1.1線路,NET DDR18V_OV2與LAN_DSM互換FOR DDR超壓ISSUE	
	3.UPDATE LL1 ,LGA775 FOOTPRINT	

Gigabyte Technology		
Title: BOM & PCB MODIFY HISTORY		
Size: Custom	Document Number: EP43-UD3L	Rev: 1.0
Date: Friday, December 05, 2008	Sheet 2 of 36	

BLOCK DIAGRAM

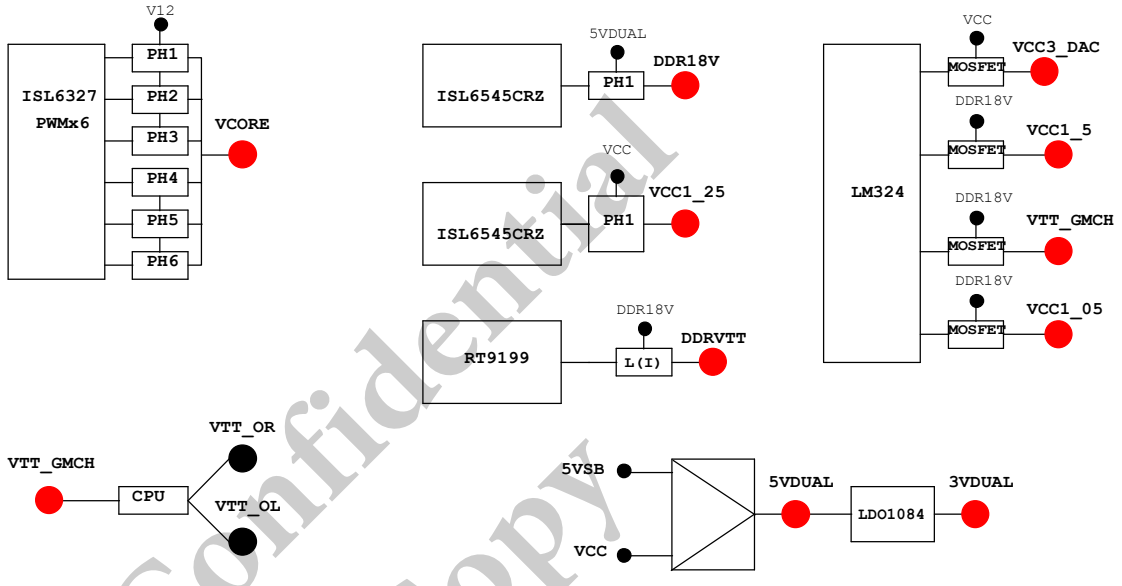


Gigabyte Technology		
Title: BLOCK DIAGRAM		
Size: Custom	Document Number: EP43-UD3L	Rev: 1.0
Date: Friday, December 05, 2008	Sheet 3 of 36	

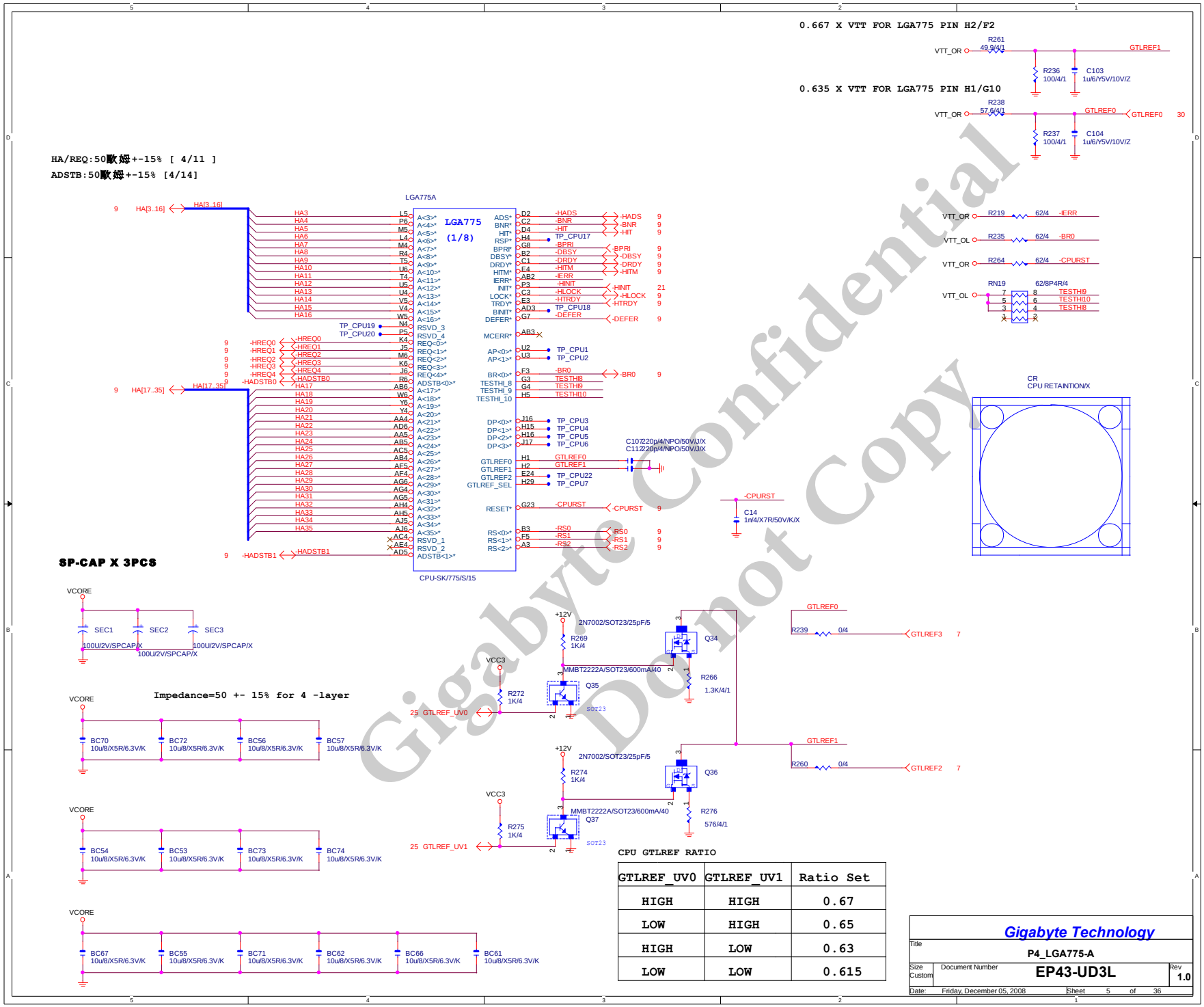
ICH8 GPIO LIST TABLE

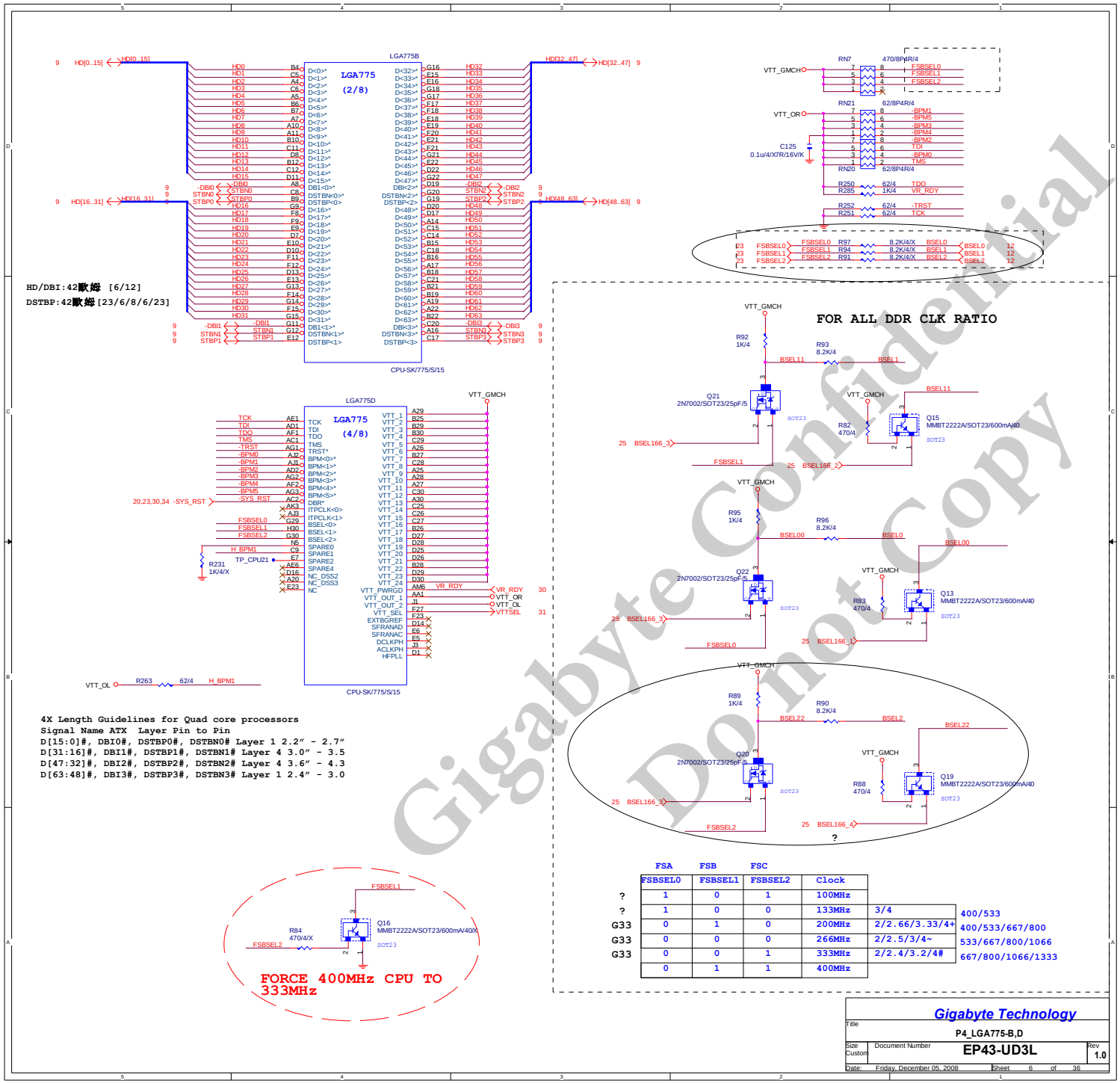
PIN NAME	PWR WELL	AFTER/ PLTRST	USAGE	NOTE
GP0	MAIN	IN	-ACZ_DET	P/U 8.2K VCC3
GP1/TACH1	MAIN	IN	ICH_FAN_TACH1	P/U 8.2K VCC3
GP2/PIRQE#	MAIN	IN	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN	IN	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN	IN	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN	IN	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN	IN	ICH_FAN_TACH2	P/U 8.2K VCC3
GP7/TACH3	MAIN	IN	ICH_FAN_TACH3	P/U 8.2K VCC3
GP8	STBY	IN	GPIO8(DUALBIOS_INPUT)	P/U 8.2K 3VDUAL
GP9	STBY	OUT	WOL_ONLY	P/D 100K GND
GP10	STBY	IN	CLGPIO1	P/U 8.2K 3VDUAL
GP11/SMBALERT#	STBY	OUT	-SMBALRT	P/U 8.2K 3VDUAL
GP12	STBY	IN	MB_ID0	P/U 8.2K 3VDUAL
GP13	STBY	IN	-LPCPME	P/U 8.2K 3VDUAL
GP14	STBY	IN	CLGPIO2	P/U 8.2K 3VDUAL
GP15	STBY	OUT	LAN_DISABLE(STP_PCI-)	N/A
GP16	MAIN	OUT/LOW	RESET	N/A
GP17/TACH0	MAIN	IN	ICH_FAN_TACH0	P/U 8.2K VCC3
GP18	MAIN	OUT	MB_ID1	P/U 8.2K VCC3
GP19	MAIN	IN	SATA1GP	P/U 8.2K VCC3
GP20	MAIN	OUT	-SPI_WP0	P/U 1K 3VCL
GP21	MAIN	IN	SATA0GP	P/U 8.2K VCC3
GP22	MAIN	IN	SCLOCK	P/U 8.2K VCC3
GP23	MAIN	OUT	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	OUT	CLGPIO0	P/U 8.2K 3VDUAL
GP25	STBY	IN	MB_ID2(STP_CPU-)	P/U 8.2K 3VDUAL
GP26/S4_STATE#	STBY	OUT	S4_STATE#	P/U 8.2K 3VDUAL
GP27	STBY	OUT/LOW	GPIO27(EL_STATE0)	P/U 8.2K 3VDUAL
GP28	STBY	OUT/LOW	PWR_LED(EL_STATE1)	N/A
GP29/OC5#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP30/OC6#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP31/OC7#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP32	MAIN	OUT	DUAL_BIOS	P/U 100K+1M VCC3
GP33	MAIN	OUT	DUAL_BIOS	P/U 8.2K VCC3
GP34	MAIN	OUT/LOW	GPIO34/SMB_RST	N/A
GP35	MAIN	OUT	SATACLKREQ#	N/A
GP36	MAIN	IN	SATA2GP	P/U 8.2K VCC3
GP37	MAIN	IN	SATA3GP	P/U 8.2K VCC3
GP38	MAIN	IN	SLOAD	P/U 8.2K VCC3
GP39	MAIN	IN	GPIO39	P/D 8.2K GND
GP48	MAIN	IN	GPIO48	P/U 8.2K VCC3
GP49	MAIN	IN	CPUPWROK	P/U 100 VTT_OL

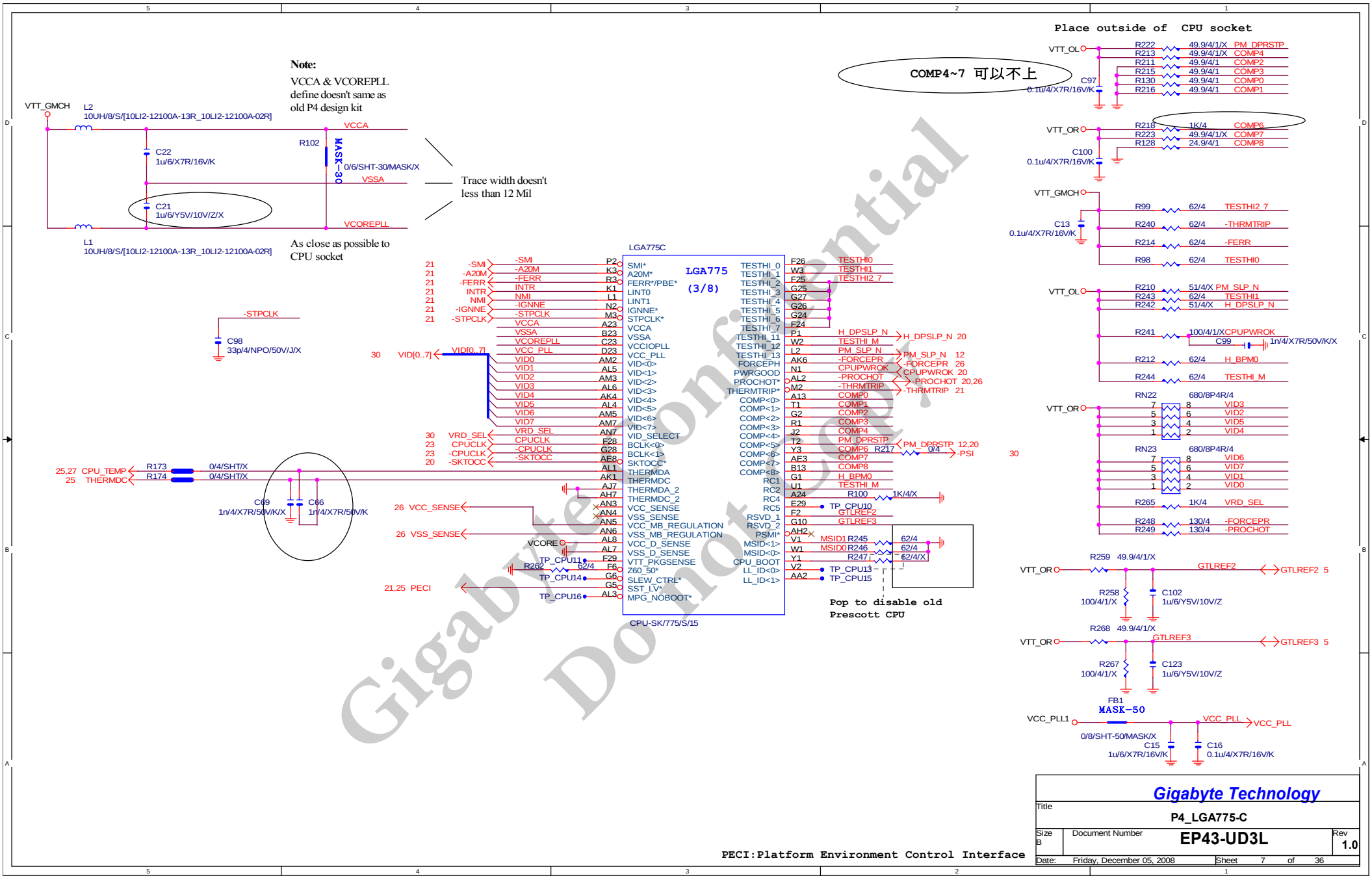
VCORE:6 PHASE PWM--ISL6327CRZ

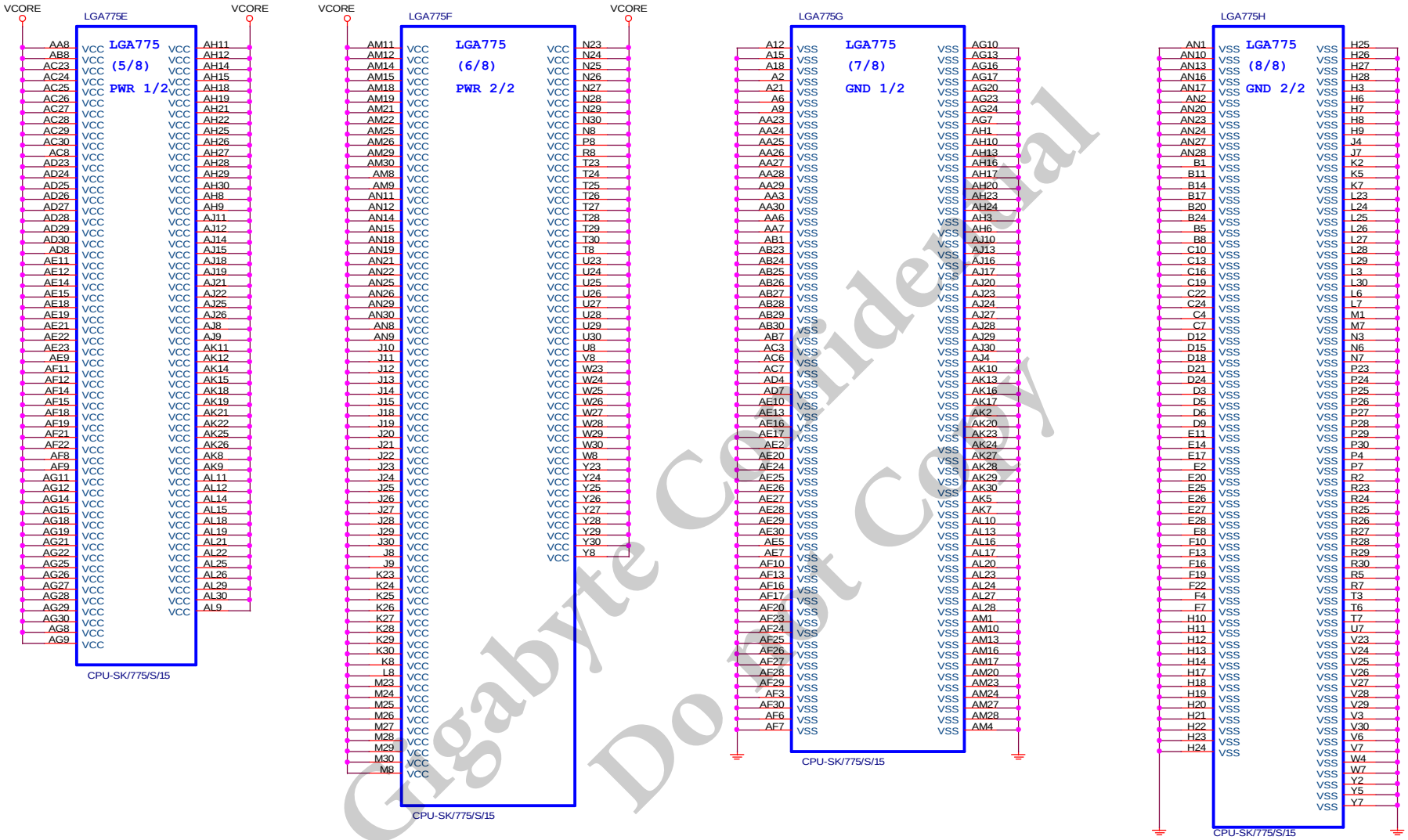


Gigabyte Technology		
Title: TABLE LIST		
Size: B	Document Number: EP43-UD3L	Rev: 1.0
Date: Friday, December 05, 2008	Sheet 4 of 36	

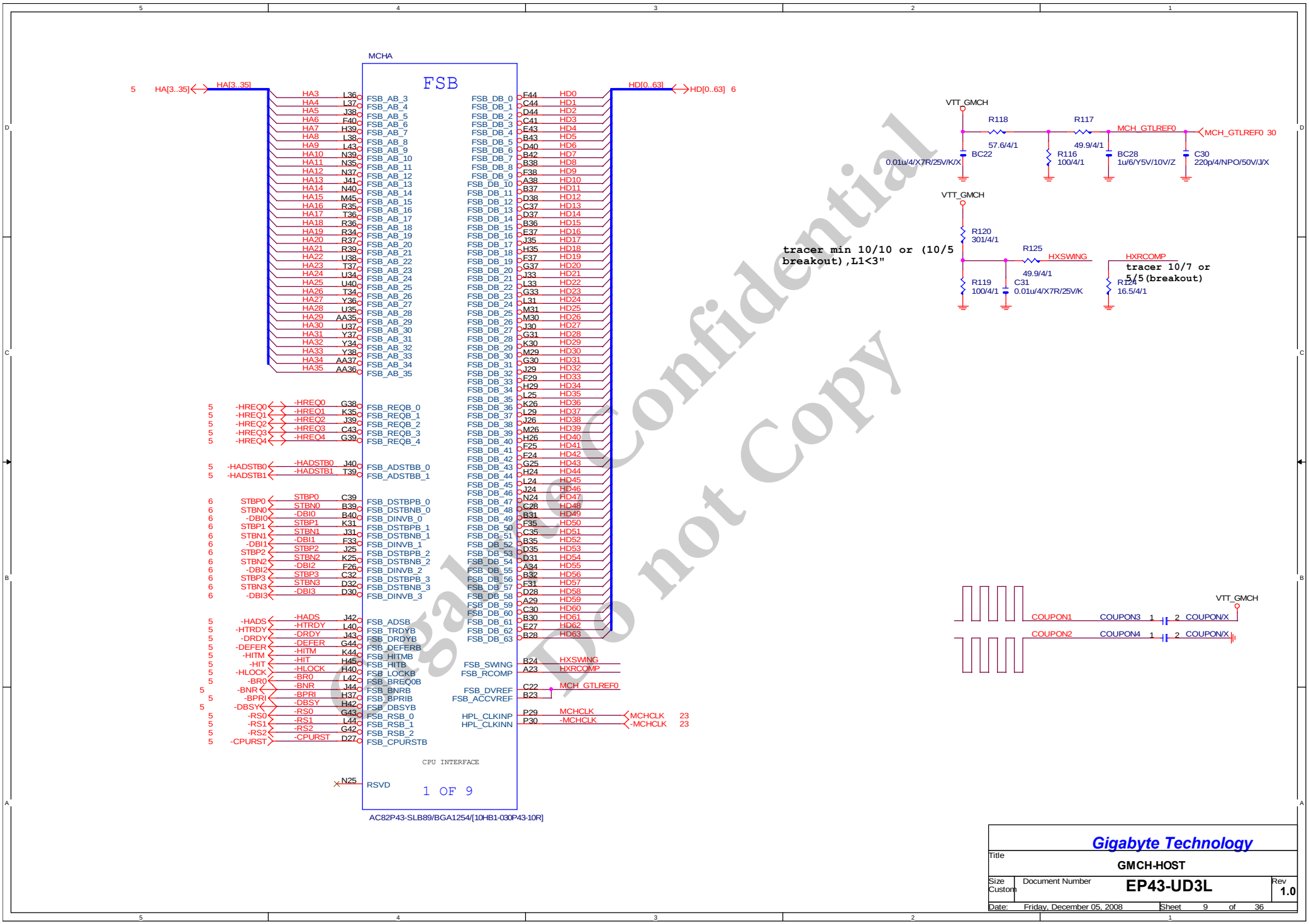


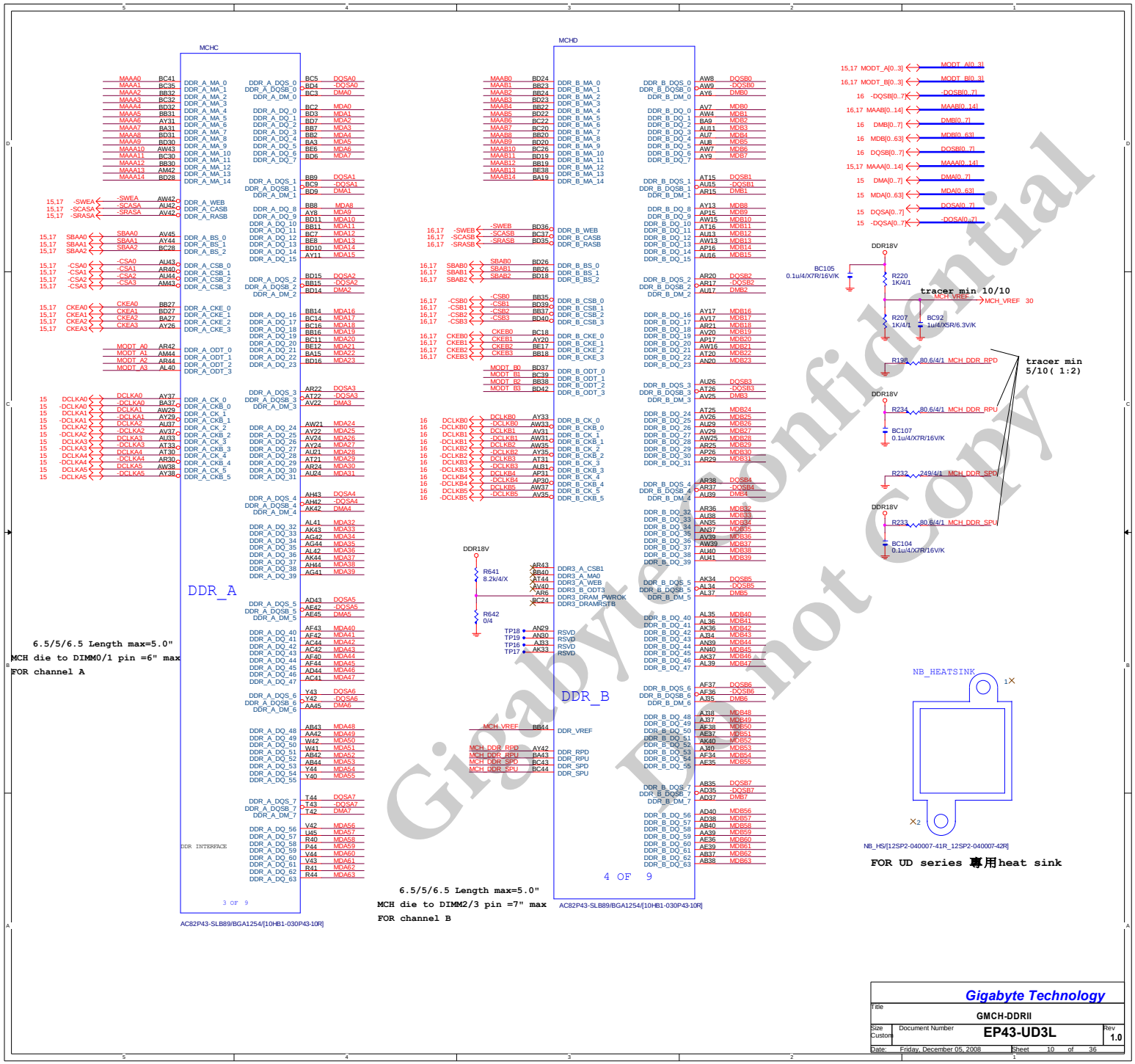






Gigabyte Technology			
Title: P4_LGA775-E,F,G,H			
Size: B	Document Number: EP43-UD3L		Rev: 1.0
Date: Friday, December 05, 2008	Sheet 8 of 36		





PCIEX16:16/5/5/5/16(breakout min 8/4/5/4/8)
Impedance=85 +- 17.5%

DMI:12/4/8/4/12
Impedance=95 +- 17.5%

MCHB

PCIE

EXP_RXP0	F6	PEG_RXP_0	PEG_TXP_0	C11	EXP_TXP0
EXP_RXN0	G7	PEG_RXN_0	PEG_TXN_0	B11	EXP_TXN0
EXP_RXP1	H6	PEG_RXP_1	PEG_TXP_1	A10	EXP_TXP1
EXP_RXN1	G4	PEG_RXN_1	PEG_TXN_1	B9	EXP_TXN1
EXP_RXP2	J6	PEG_RXP_2	PEG_TXP_2	C9	EXP_TXP2
EXP_RXN2	J7	PEG_RXN_2	PEG_TXN_2	D8	EXP_TXN2
EXP_RXP3	L6	PEG_RXP_3	PEG_TXP_3	B8	EXP_TXP3
EXP_RXN3	L7	PEG_RXN_3	PEG_TXN_3	C7	EXP_TXN3
EXP_RXP4	N9	PEG_RXP_4	PEG_TXP_4	B7	EXP_TXP4
EXP_RXN4	N10	PEG_RXN_4	PEG_TXN_4	B6	EXP_TXN4
EXP_RXP5	N7	PEG_RXP_5	PEG_TXP_5	B3	EXP_TXP5
EXP_RXN5	N6	PEG_RXN_5	PEG_TXN_5	B4	EXP_TXN5
EXP_RXP6	R7	PEG_RXP_6	PEG_TXP_6	D2	EXP_TXP6
EXP_RXN6	R6	PEG_RXN_6	PEG_TXN_6	C2	EXP_TXN6
EXP_RXP7	R9	PEG_RXP_7	PEG_TXP_7	H2	EXP_TXP7
EXP_RXN7	R10	PEG_RXN_7	PEG_TXN_7	G2	EXP_TXN7
EXP_RXP8	U10	PEG_RXP_8	PEG_TXP_8	J2	EXP_TXP8
EXP_RXN8	U9	PEG_RXN_8	PEG_TXN_8	K2	EXP_TXN8
EXP_RXP9	U6	PEG_RXP_9	PEG_TXP_9	K1	EXP_TXP9
EXP_RXN9	U7	PEG_RXN_9	PEG_TXN_9	L2	EXP_TXN9
EXP_RXP10	AA9	PEG_RXP_10	PEG_TXP_10	P2	EXP_TXP10
EXP_RXN10	AA10	PEG_RXN_10	PEG_TXN_10	M2	EXP_TXN10
EXP_RXP11	R4	PEG_RXP_11	PEG_TXP_11	T2	EXP_TXP11
EXP_RXN11	P4	PEG_RXN_11	PEG_TXN_11	R1	EXP_TXN11
EXP_RXP12	AA7	PEG_RXP_12	PEG_TXP_12	U2	EXP_TXP12
EXP_RXN12	AA6	PEG_RXN_12	PEG_TXN_12	V2	EXP_TXN12
EXP_RXP13	AB10	PEG_RXP_13	PEG_TXP_13	W4	EXP_TXP13
EXP_RXN13	AB9	PEG_RXN_13	PEG_TXN_13	V3	EXP_TXN13
EXP_RXP14	AB3	PEG_RXP_14	PEG_TXP_14	AA4	EXP_TXP14
EXP_RXN14	AA2	PEG_RXN_14	PEG_TXN_14	Y4	EXP_TXN14
EXP_RXP15	AD10	PEG_RXP_15	PEG_TXP_15	AC1	EXP_TXP15
EXP_RXN15	AD11	PEG_RXN_15	PEG_TXN_15	AB2	EXP_TXN15

EXP_TXP[0..15] → EXP_TXP[0..15] 18
EXP_TXN[0..15] → EXP_TXN[0..15] 18
EXP_RXP[0..15] → EXP_RXP[0..15] 18
EXP_RXN[0..15] → EXP_RXN[0..15] 18

VCC1_1
BC69 0.1u/4/X7R/16V/K
R165 49.9/4/1 GRCOMP

tracer 10/10

DMI

19 DMI_0RXP	DMI_0RXP	AD7	DMI_RXP_0	DMI_TXP_0	AC2	DMI_0TXP 19 DMI_0TXP
19 DMI_0RXN	DMI_0RXN	AD8	DMI_RXN_0	DMI_TXN_0	AD2	DMI_0TXN 19 DMI_0TXN
19 DMI_1RXP	DMI_1RXP	AE9	DMI_RXP_1	DMI_TXP_1	AD4	DMI_1TXP 19 DMI_1TXP
19 DMI_1RXN	DMI_1RXN	AE10	DMI_RXN_1	DMI_TXN_1	AE4	DMI_1TXN 19 DMI_1TXN
19 DMI_2RXP	DMI_2RXP	AE6	DMI_RXP_2	DMI_TXP_2	AE2	DMI_2TXP 19 DMI_2TXP
19 DMI_2RXN	DMI_2RXN	AE7	DMI_RXN_2	DMI_TXN_2	AF2	DMI_2TXN 19 DMI_2TXN
19 DMI_3RXP	DMI_3RXP	AF9	DMI_RXP_3	DMI_TXP_3	AF4	DMI_3TXP 19 DMI_3TXP
19 DMI_3RXN	DMI_3RXN	AF8	DMI_RXN_3	DMI_TXN_3	AG4	DMI_3TXN 19 DMI_3TXN

23 SRCCLK_MCH → SRCCLK_MCH → D9 EXP_CLKP
23 -SRCCLK_MCH → -SRCCLK_MCH → E9 EXP_CLKN

18 SDVO_CLDATA → SDVO_CLDATA → J13 SDVO_CTRLDATA
18 SDVO_CLCLK → SDVO_CLCLK → G13 SDVO_CTRLCLK

EXP_RCOMPO Y7 GRCOMP
EXP_COMPI Y8
EXP_ICOMPO Y6

TP14 AB13 RSVD
TP15 AD13 RSVD

EXP_RBIAS AG1 GRBIAS
R182 750/4/1

2 OF 9

AC82P43-SLB89/BGA1254/[10HB1-030P43-10R]

Gigabyte Technology		
Title	GMCH-PCI E & DMI	
Size: Custom	Document Number: EP43-UD3L	Rev: 1.0
Date: Friday, December 05, 2008	Sheet 11 of 36	

EXP_SM
0:SDVO OR PCIE
1:BOTH SDVO AND PCIE

EXP_SLR:
0:BTX PCIE are reversed
1:ATX PCIE normal

ITPM:
0:ENABLE ITPM
1:DISABLE ITPM

CEN:
0:DISABLE TLS
1:ENABLE TLS

CL_VREF:4/10
0.349V

MCHE

VGA

MISC

5 OF 9

AC82P43-SLB89/BGA1254/[10HB1-030P43-10R]

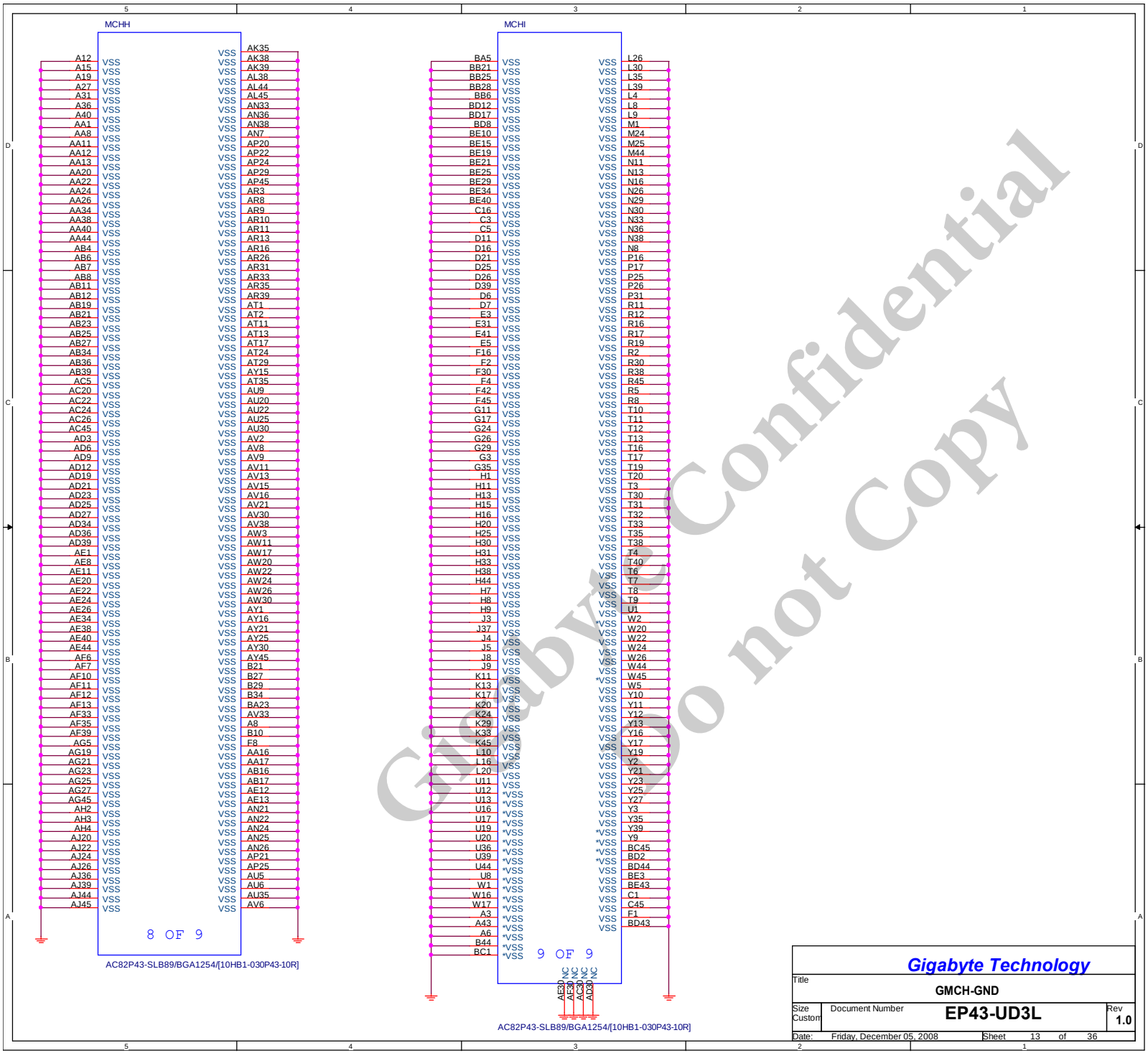
BW+ICH8 不要上(SAMPLE)
BW+ICH7 要上

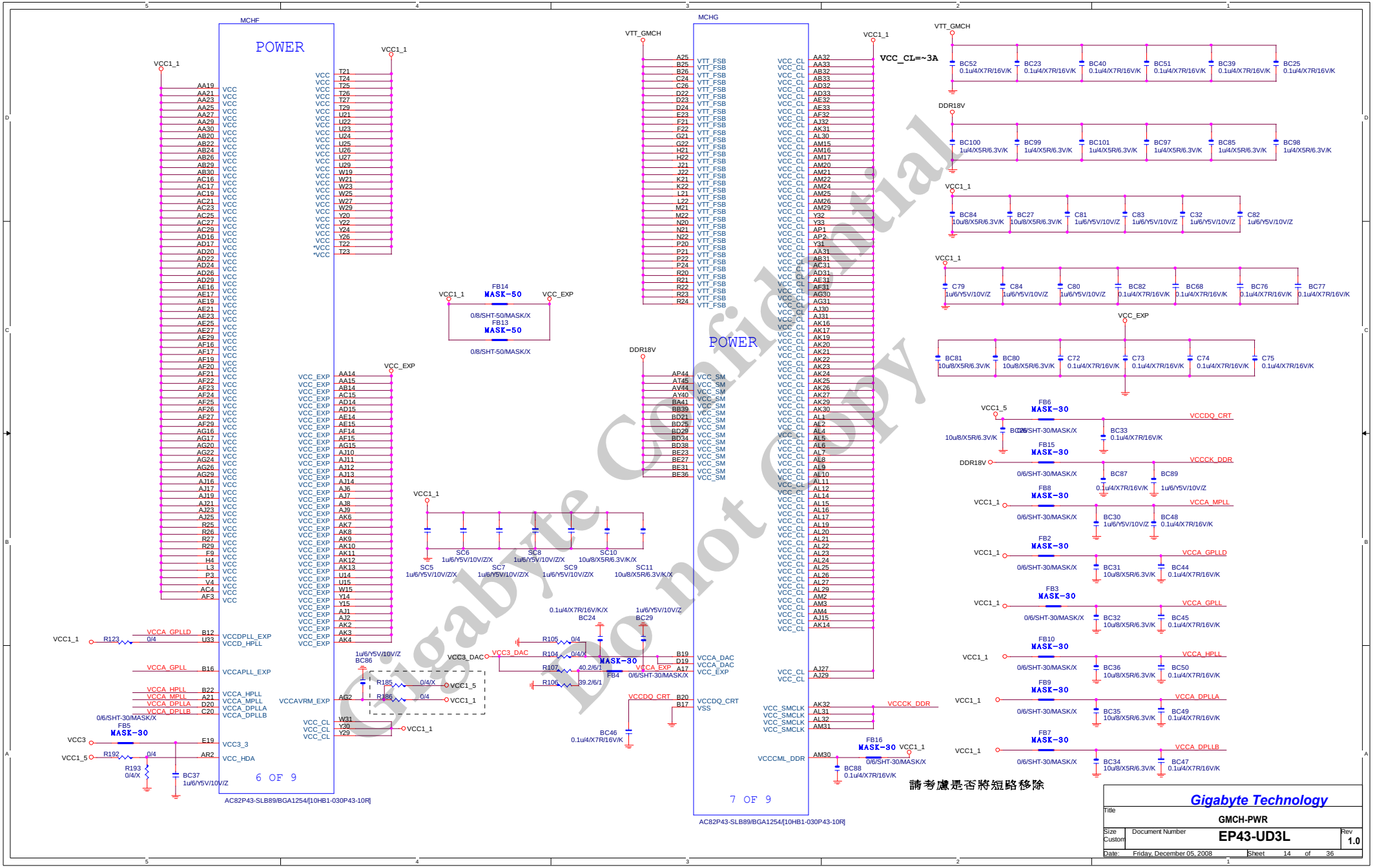
Gigabyte Technology

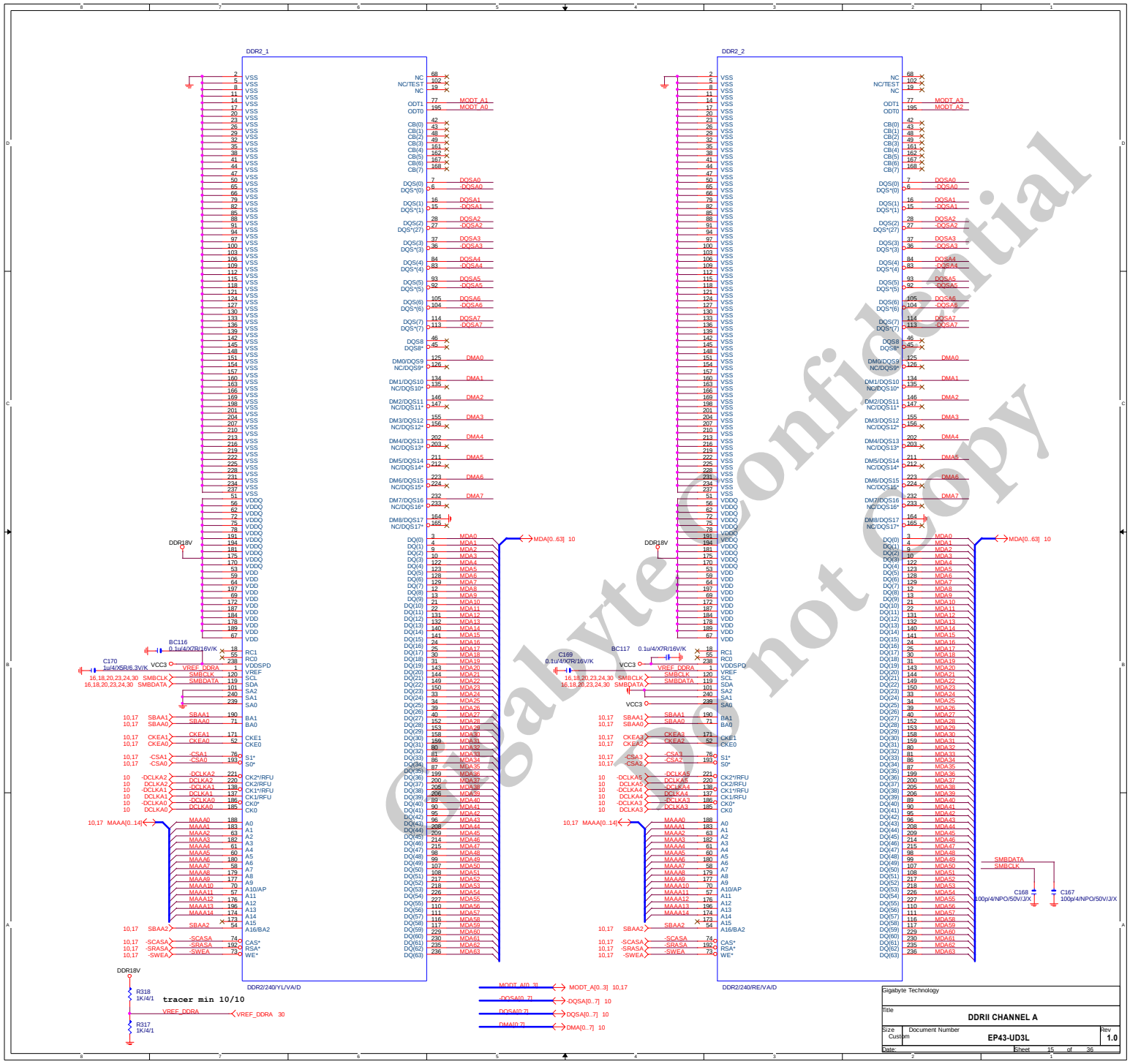
Title: GMCH-INTERNAL VGA

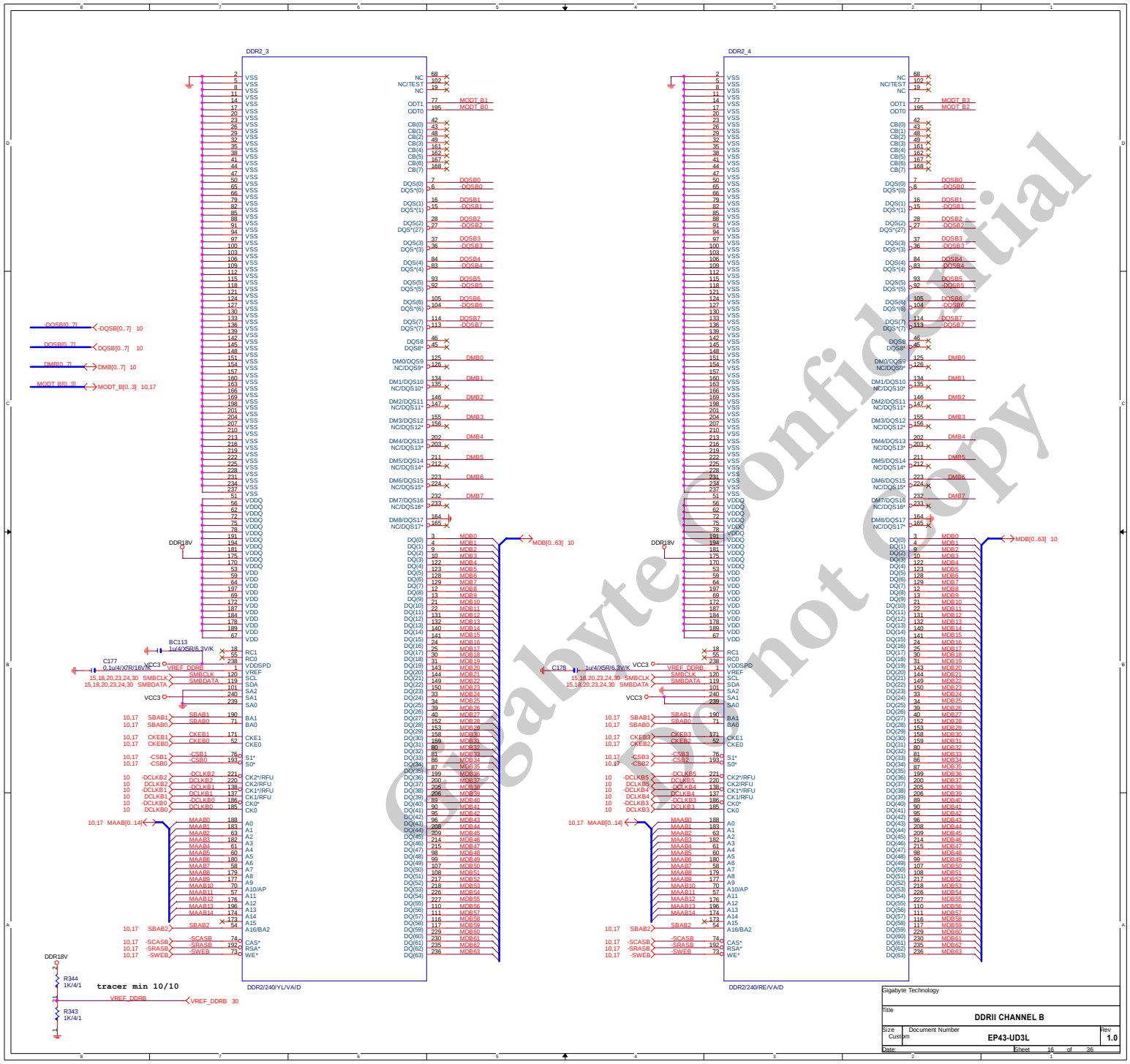
Size: Custom | Document Number: EP43-UD3L | Rev: 1.0

Date: Friday, December 05, 2008 | Sheet 12 of 36



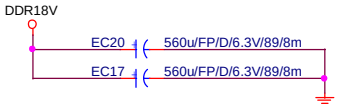


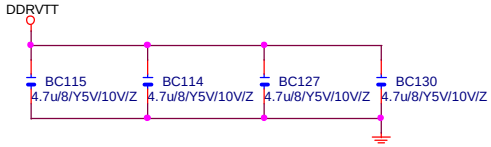




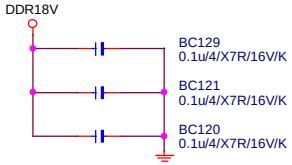
DDR TERMINATION CHANNEL A

DDRVTT Decouple

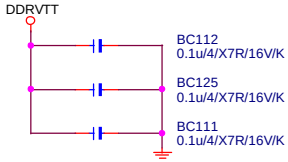


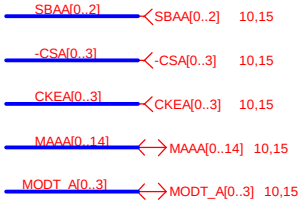


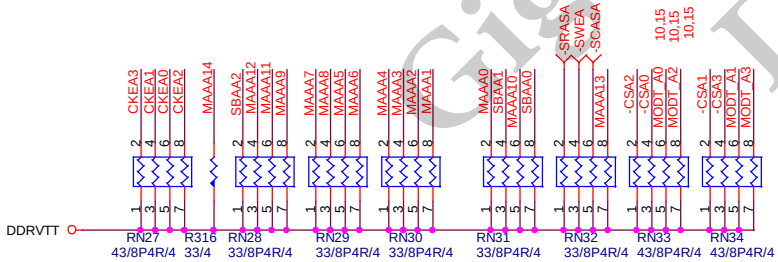
DDR18V Decouple



DDRVTT Decouple

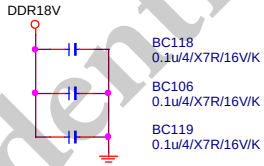




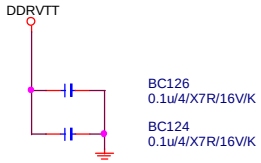


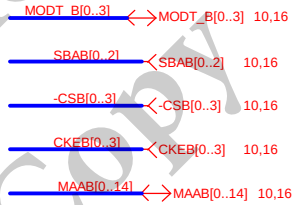
DDR TERMINATION CHANNEL B

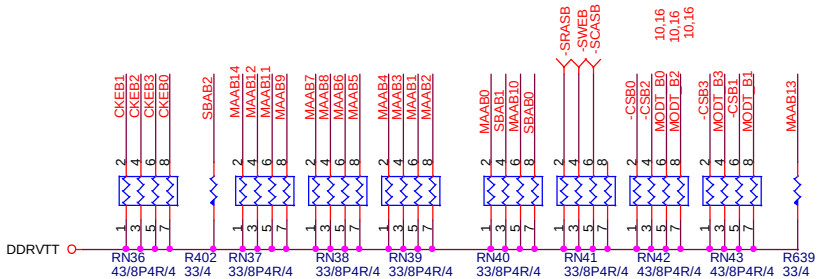
DDR18V Decouple



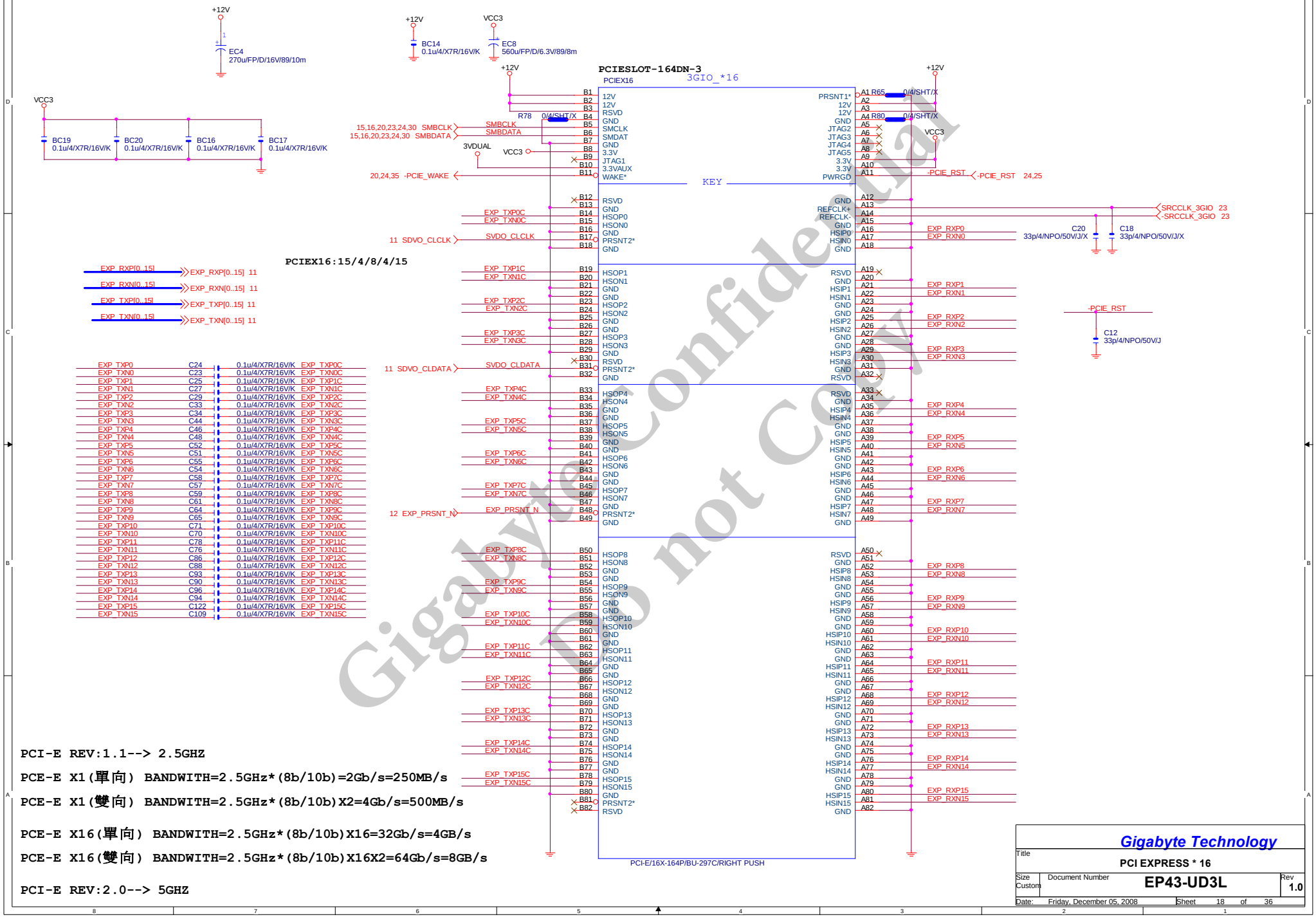
DDRVTT Decouple

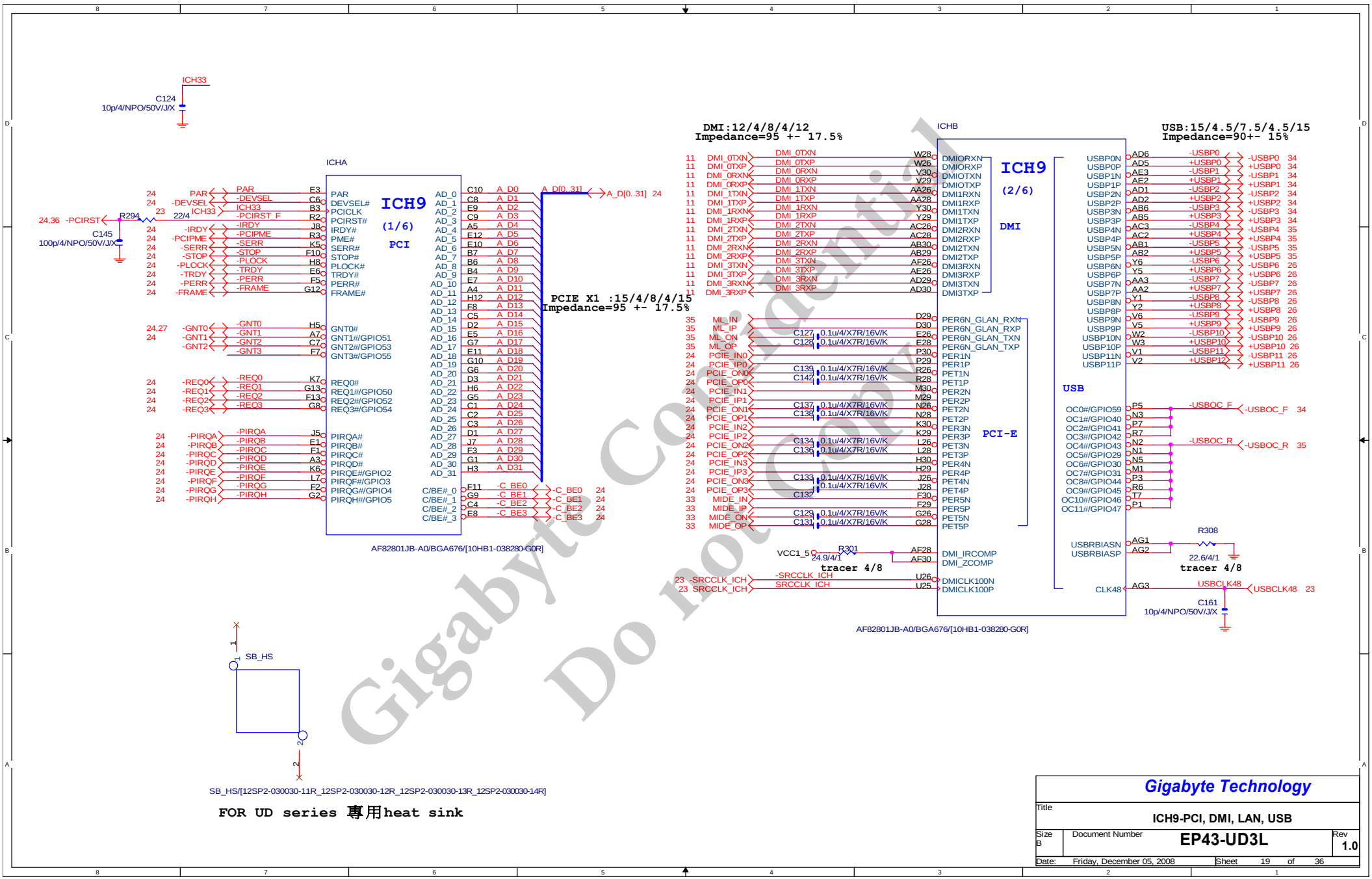




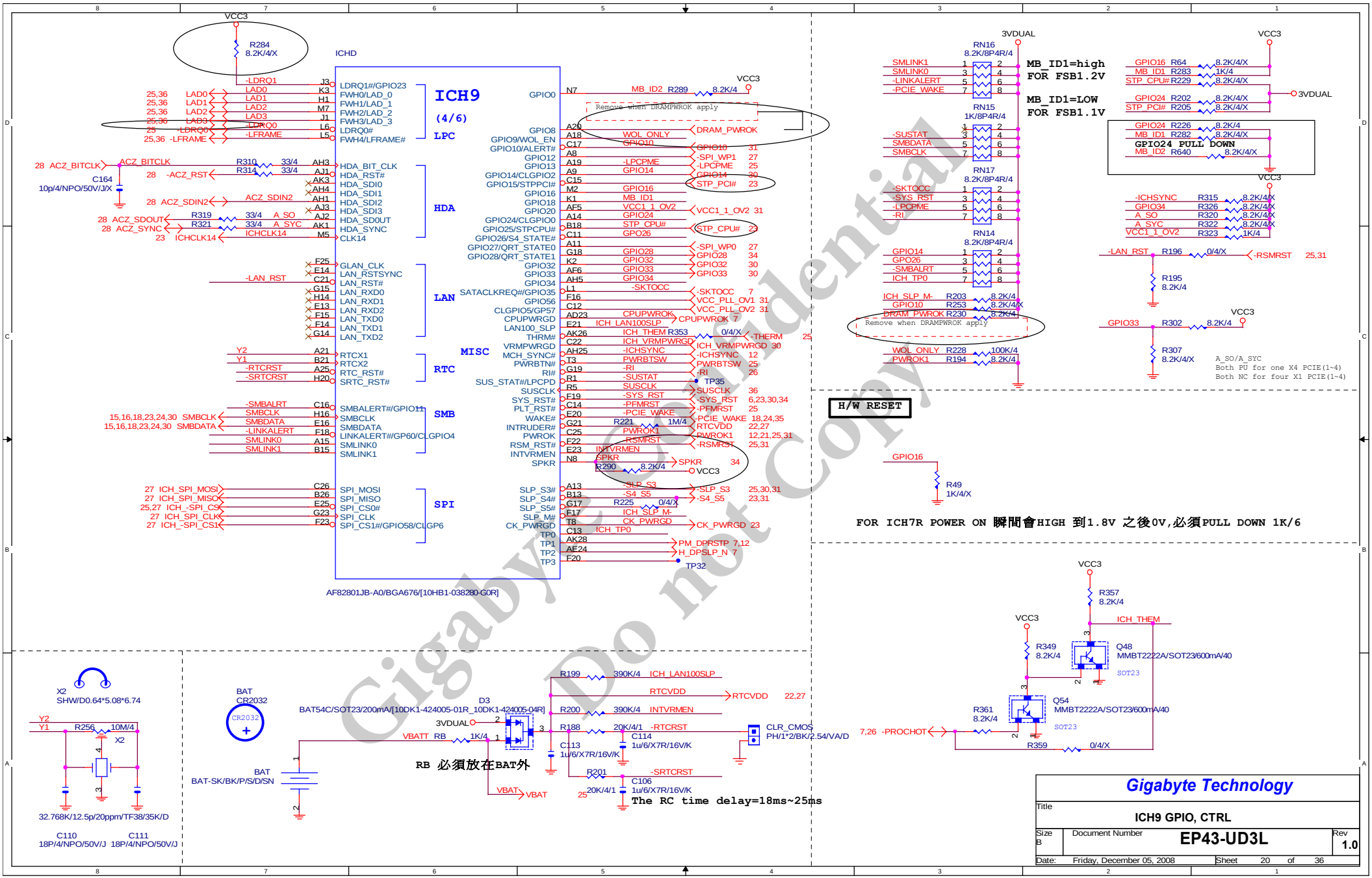


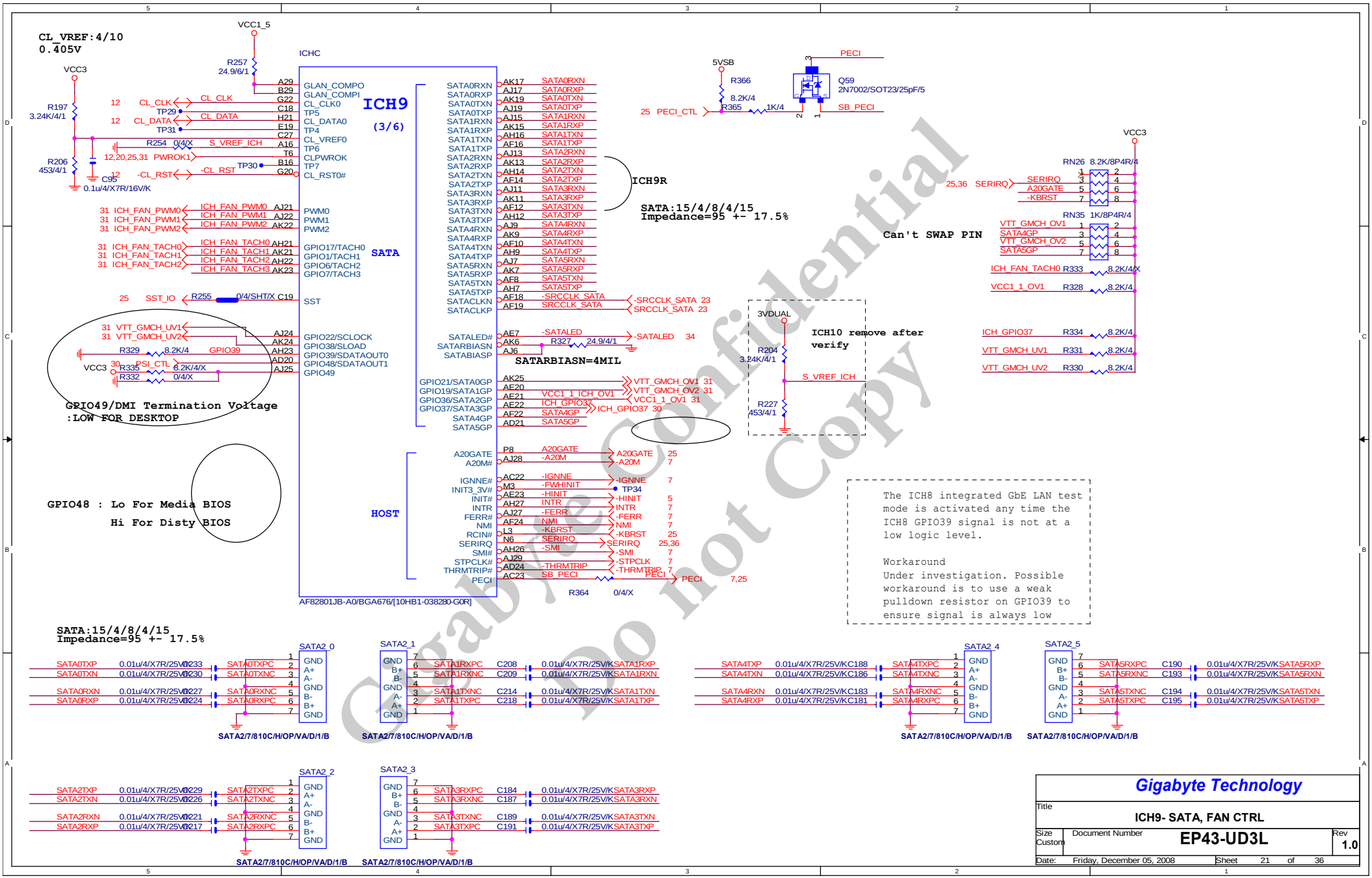
Gigabyte Technology		
Title: DDRII TERMINATOR		
Size: Custom	Document Number: EP43-UD3L	Rev: 1.0
Date: Friday, December 05, 2008	Sheet 17 of 36	

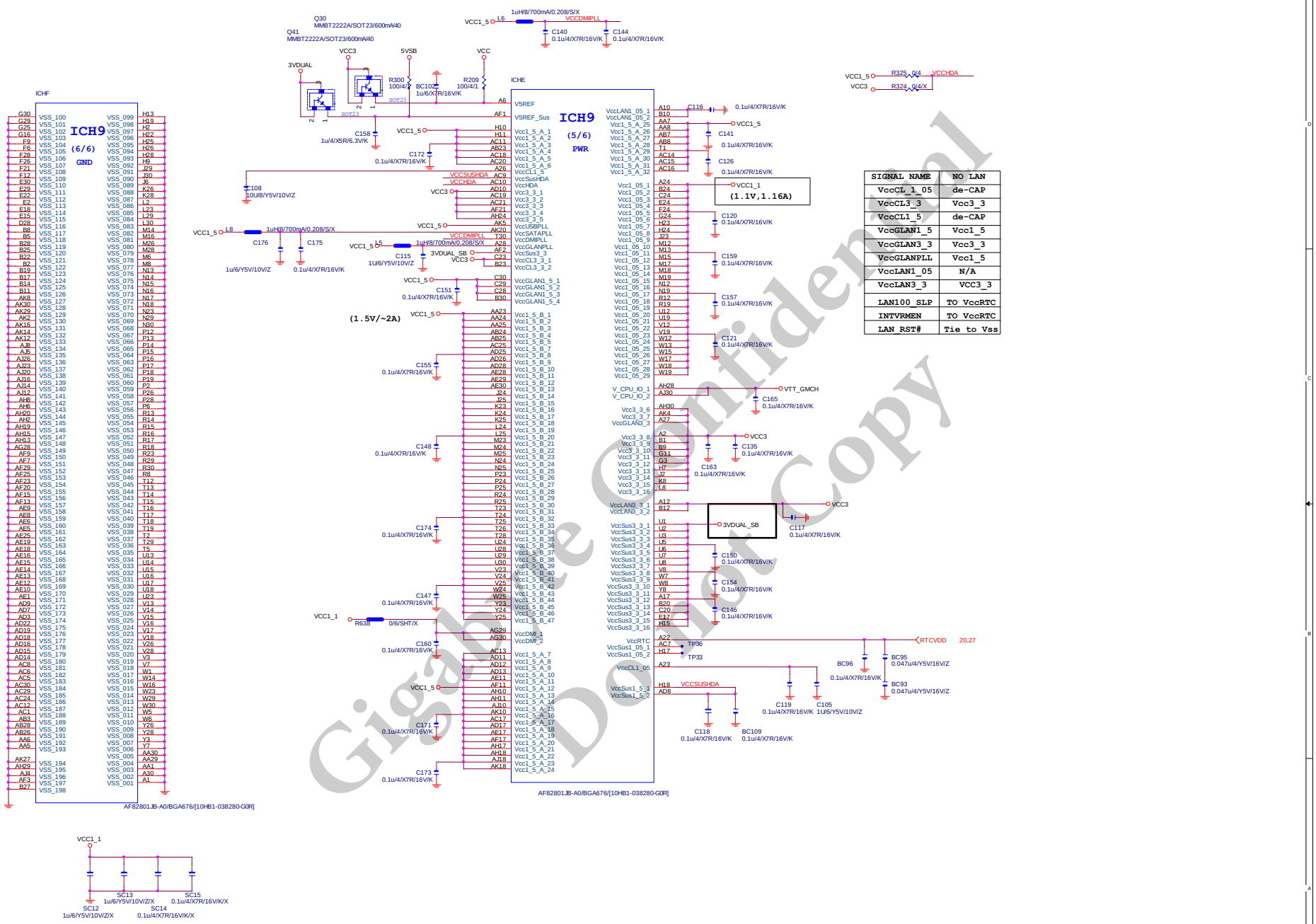




Gigabyte Technology		
Title	ICH9-PCI, DMI, LAN, USB	
Size B	Document Number EP43-UD3L	Rev 1.0
Date: Friday, December 05, 2008	Sheet 19 of 36	

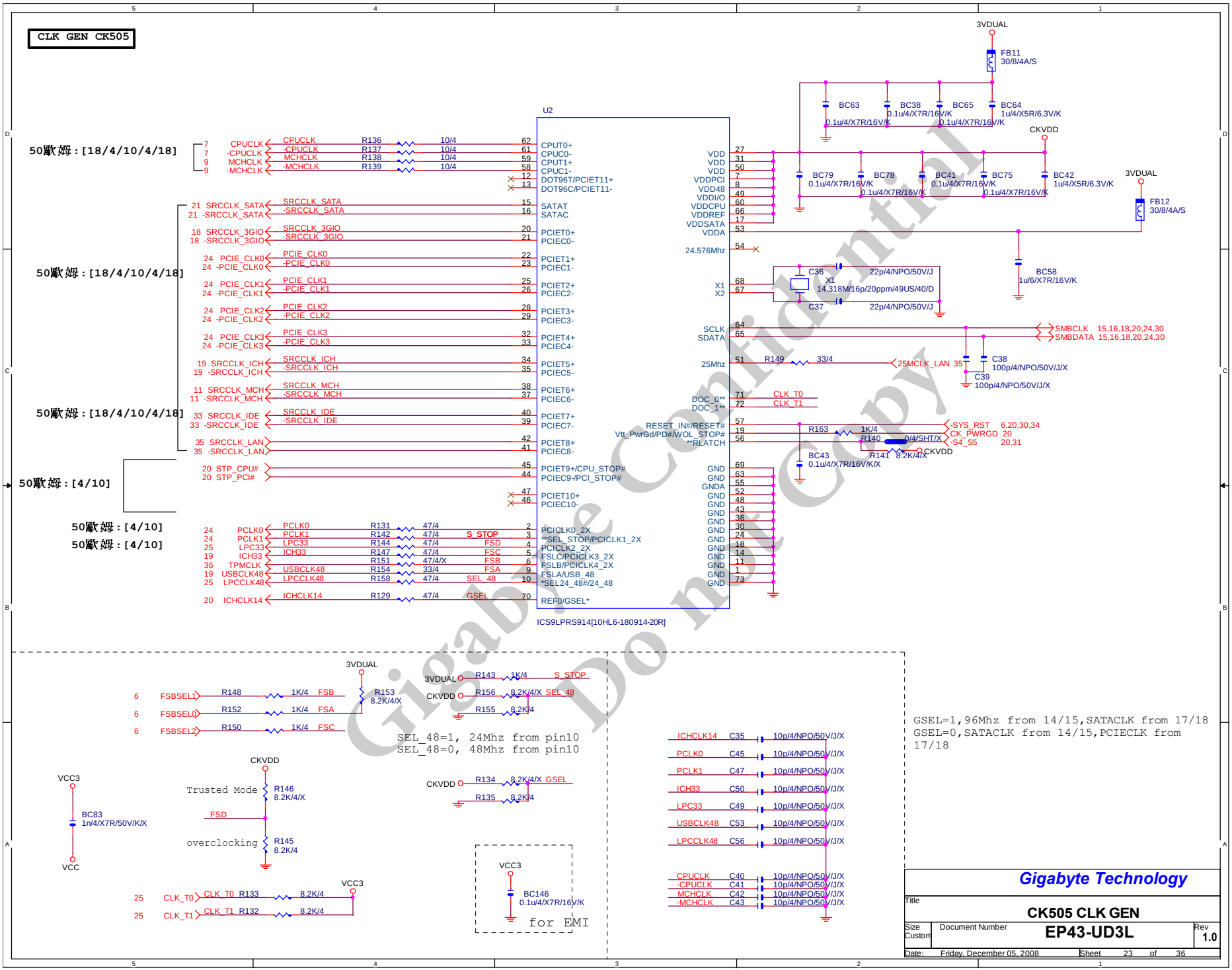


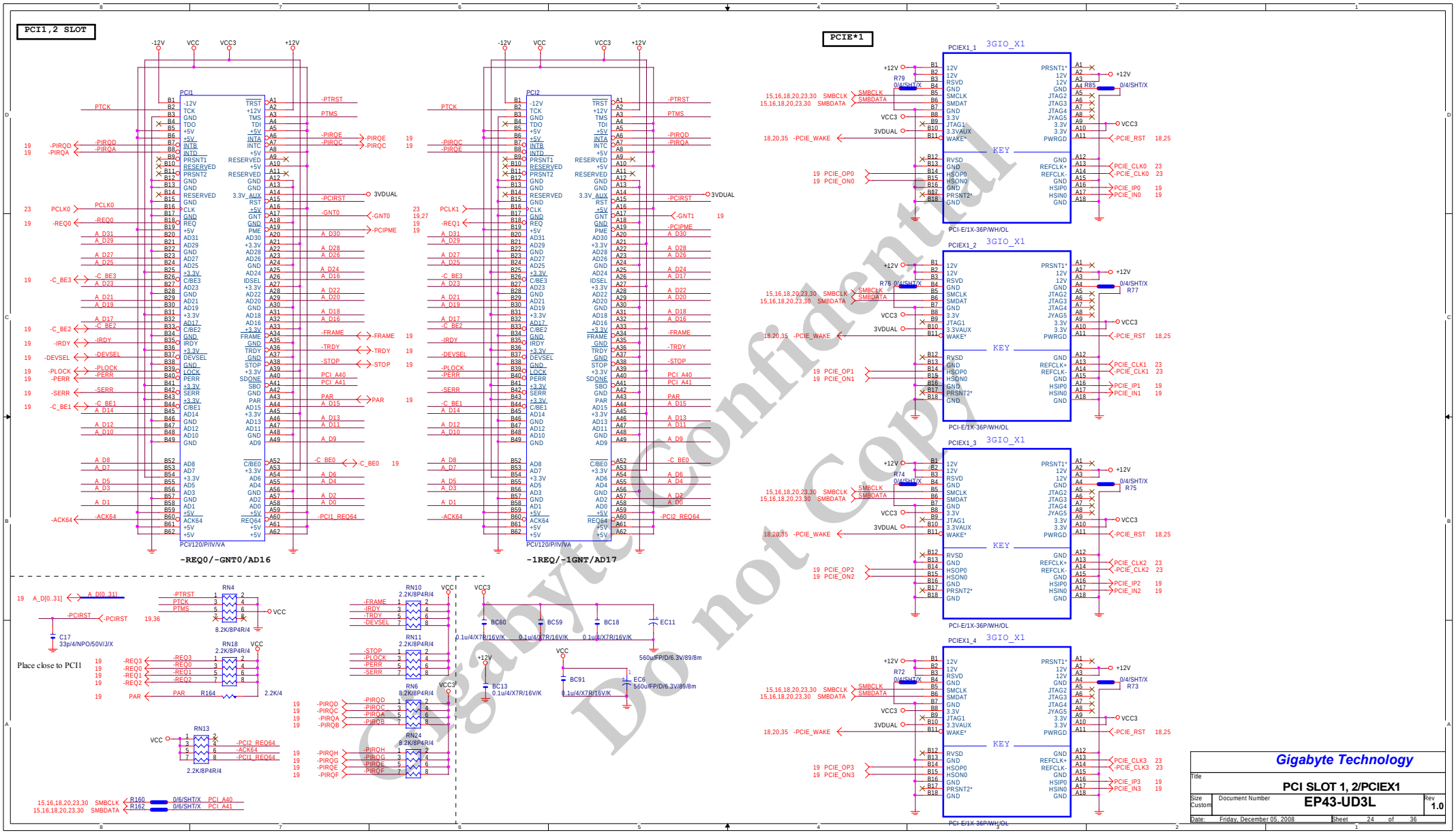


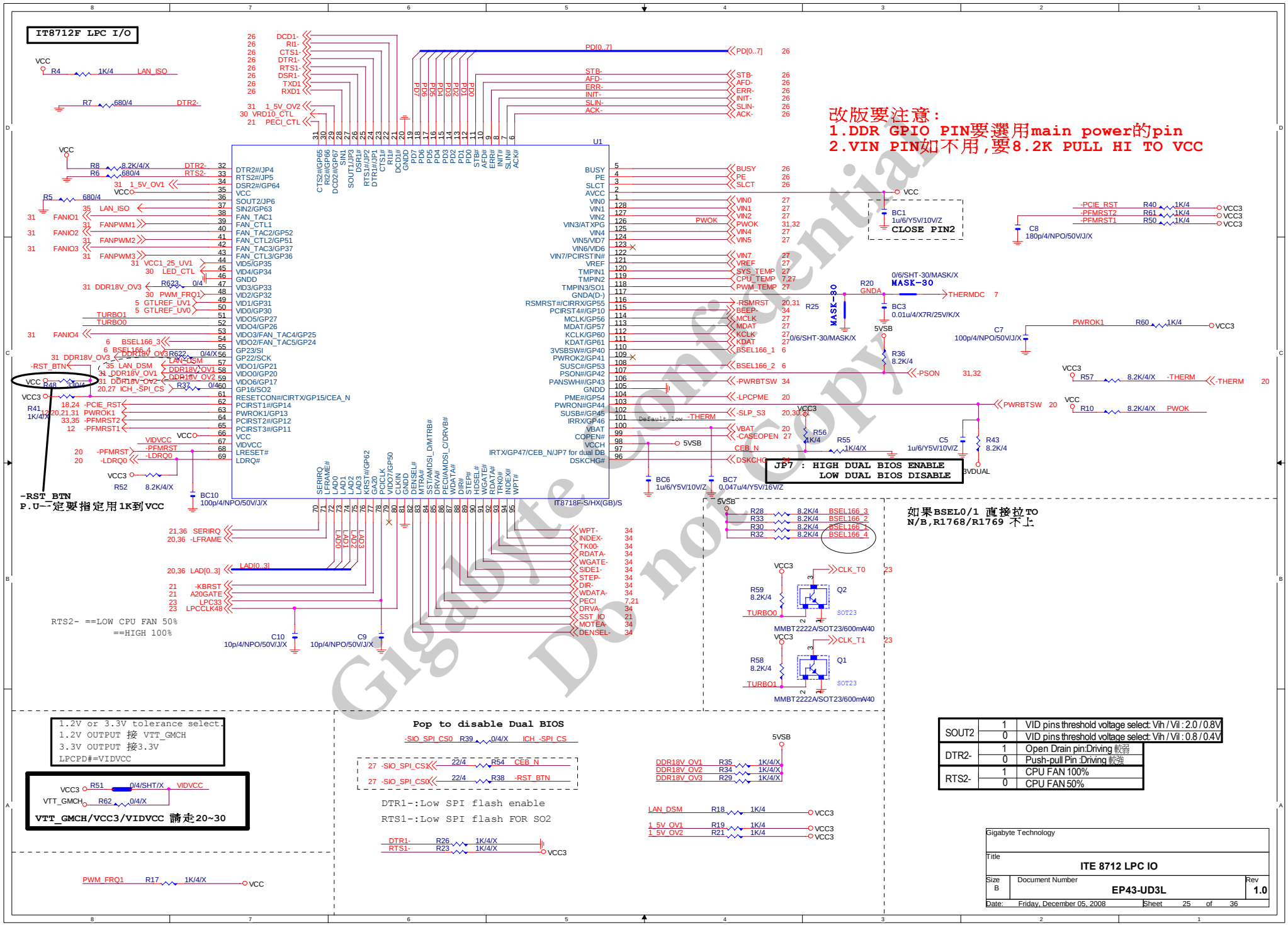


SIGNAL_NAME	NO_LAN
VccCL_1_05	de-CAP
VccCL3_3	Vcc3_3
VccCL1_5	de-CAP
VccGLAN1_5	Vcc1_5
VccGLAN3_3	Vcc3_3
VccGLANPLL	Vcc1_5
VccLAN1_05	N/A
VccLAN3_3	VCC3_3
LAN100_SLP	TO VccRTC
INTVRMEN	TO VccRTC
LAN_RST#	Tie to Vss

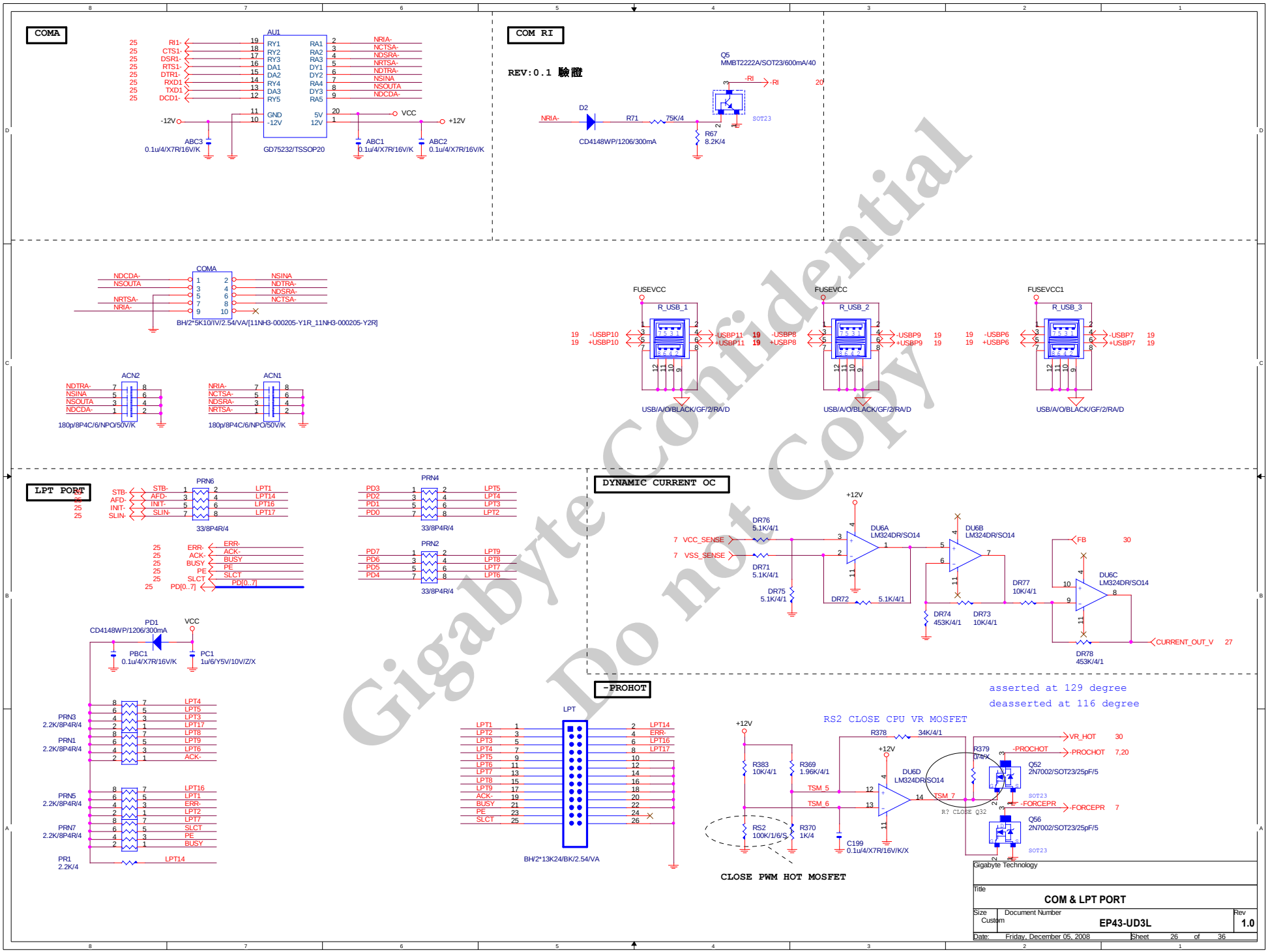
Gigabyte Technology		
Title: ICH9-PWR & GND		
Size: C	Document Number: EP43-UD3L	Rev: 1.0
Date: Friday, December 05, 2008	Sheet 22 of 36	

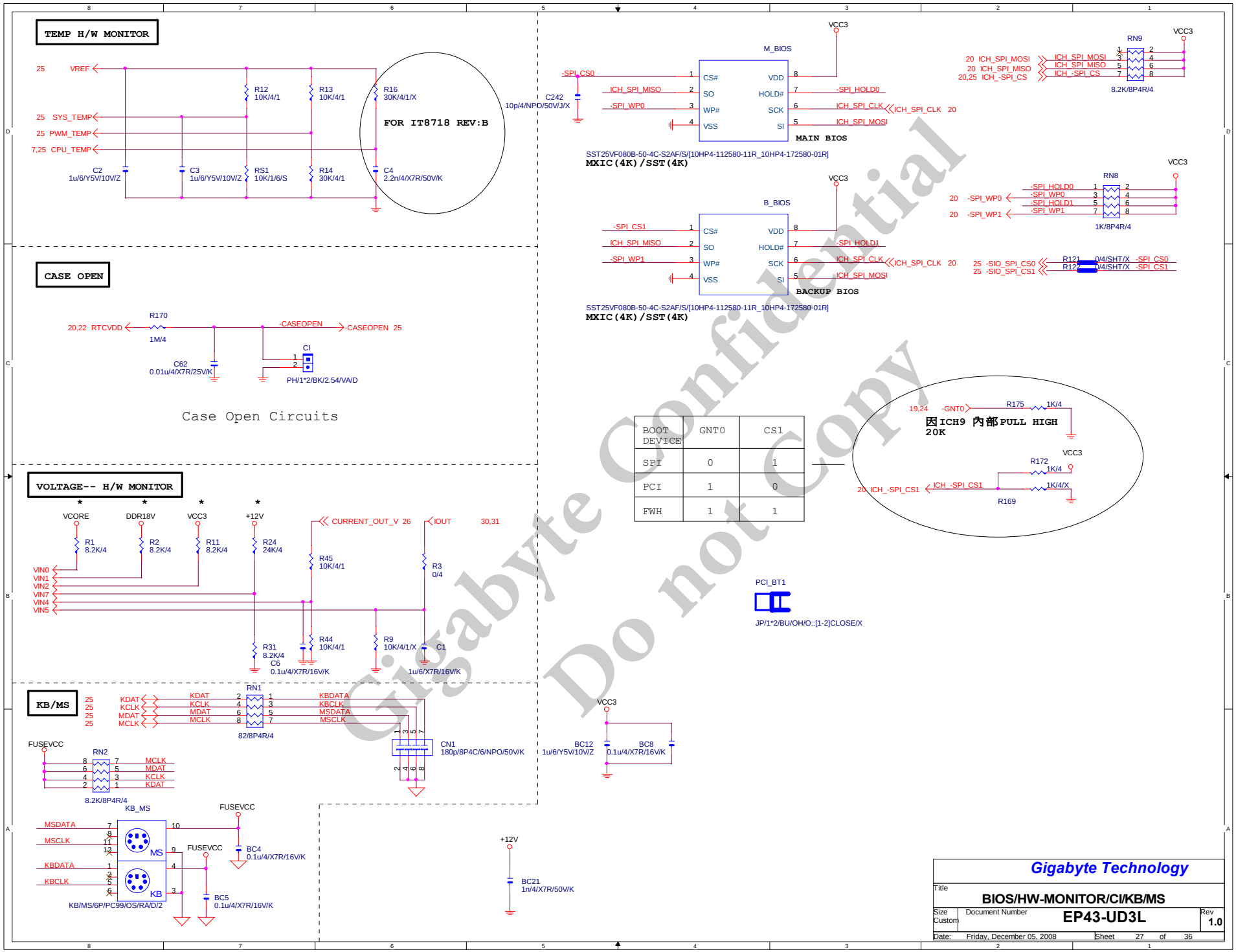






SOUT2	1	VID pins threshold voltage select: Vih / Vil : 2.0 / 0.8V
	0	VID pins threshold voltage select: Vih / Vil : 0.8 / 0.4V
DTR2-	1	Open Drain pin:Driving 較弱
	0	Push-pull Pin :Driving 較強
RTS2-	1	CPU FAN 100%
	0	CPU FAN 50%



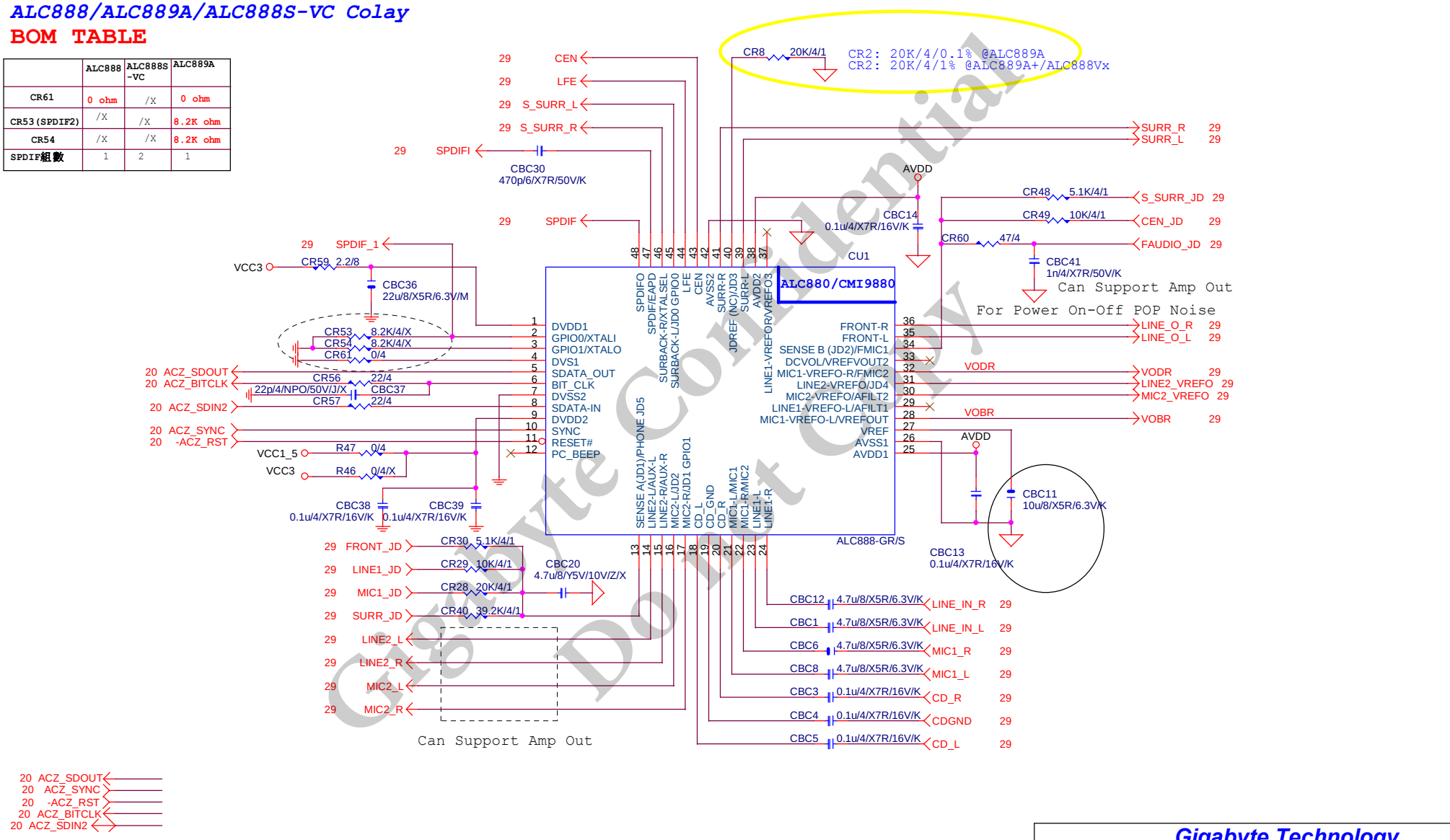


AZALIA CODEC

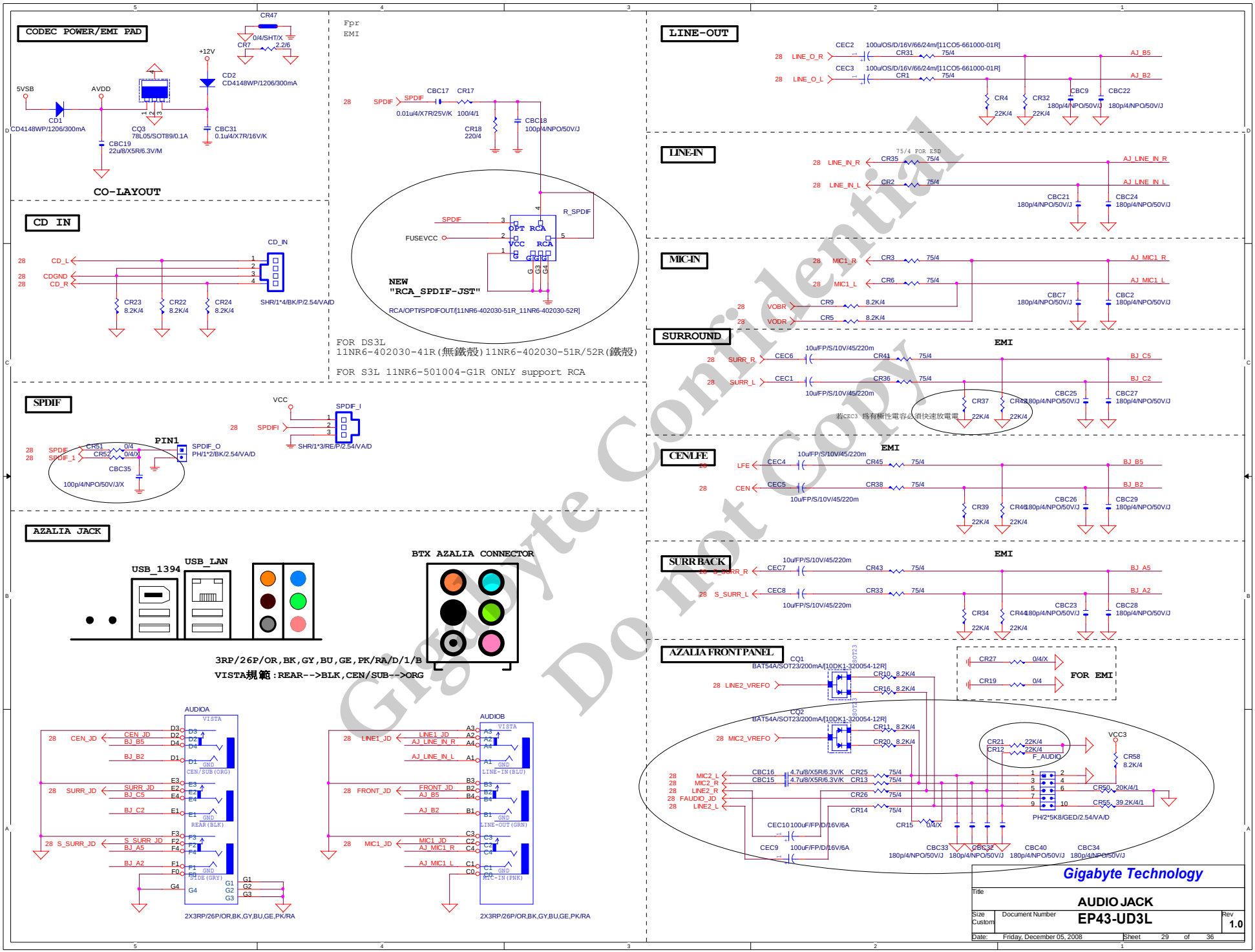
ALC888/ALC889A/ALC888S-VC Colay

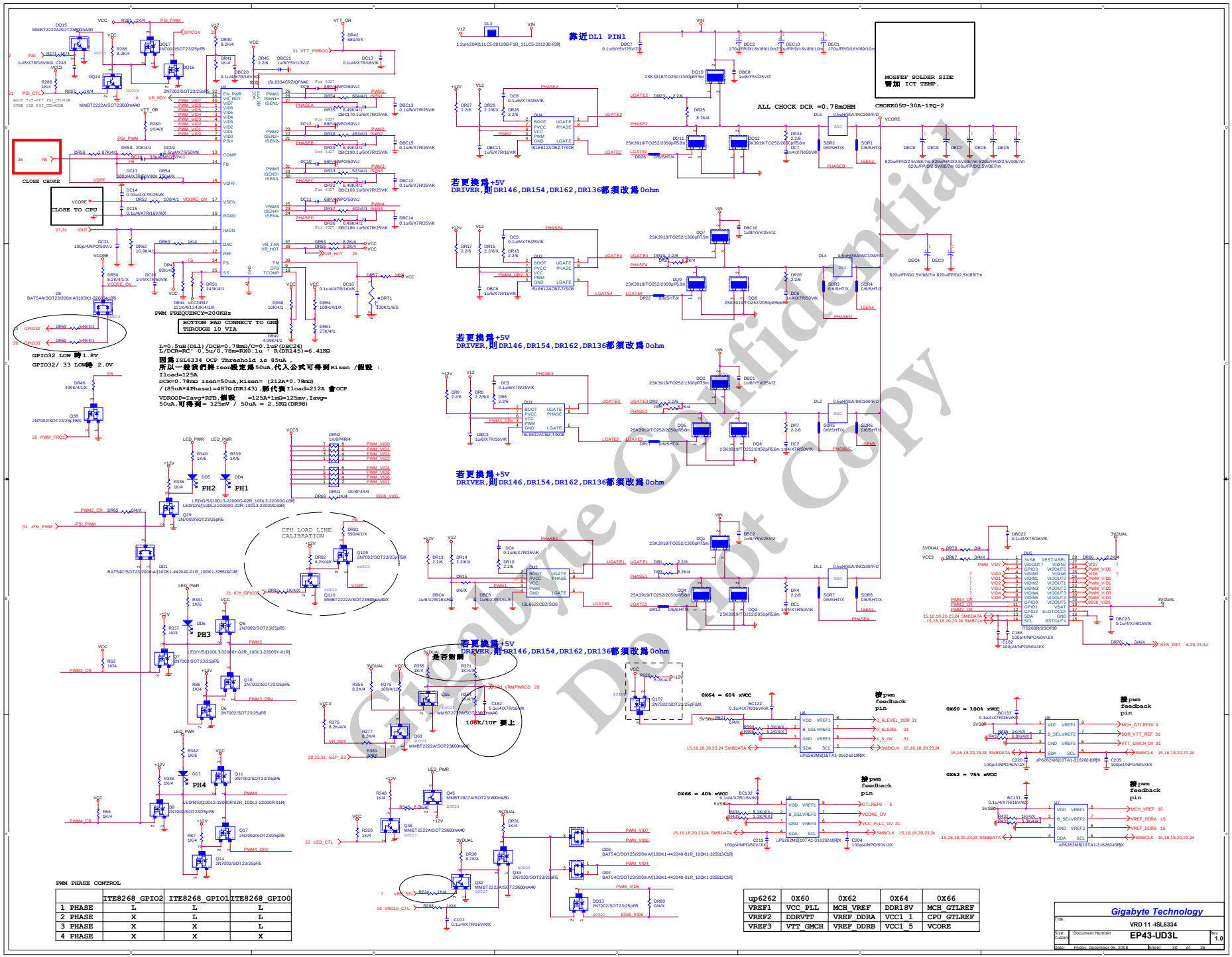
BOM TABLE

	ALC888	ALC888S-VC	ALC889A
CR61	0 ohm	/X	0 ohm
CR53(SPDIF2)	/X	/X	8.2K ohm
CR54	/X	/X	8.2K ohm
SPDIF組數	1	2	1



Gigabyte Technology			
Title: ALC888			
Size: Custom	Document Number: EP43-UD3L		Rev: 1.0
Date: Friday, December 05, 2008	Sheet 28 of 36		





	ITE8268_GPIO2	ITE8268_GPIO1	ITE8268_GPIO0
1 PHASE	L	L	L
2 PHASE	X	L	L
3 PHASE	X	X	L
4 PHASE	X	X	X

up6262	0X60	0X62	0X64	0X66
VREF1	VCC_PLL	MCH_VREF	DDR18V	MCH_GTLREF
VREF2	DDRVTT	VREF_DDRA	VCC1_1	CPU_GTLREF
VREF3	VTT_GMCH	VREF_DDRB	VCC1_5	VCORE

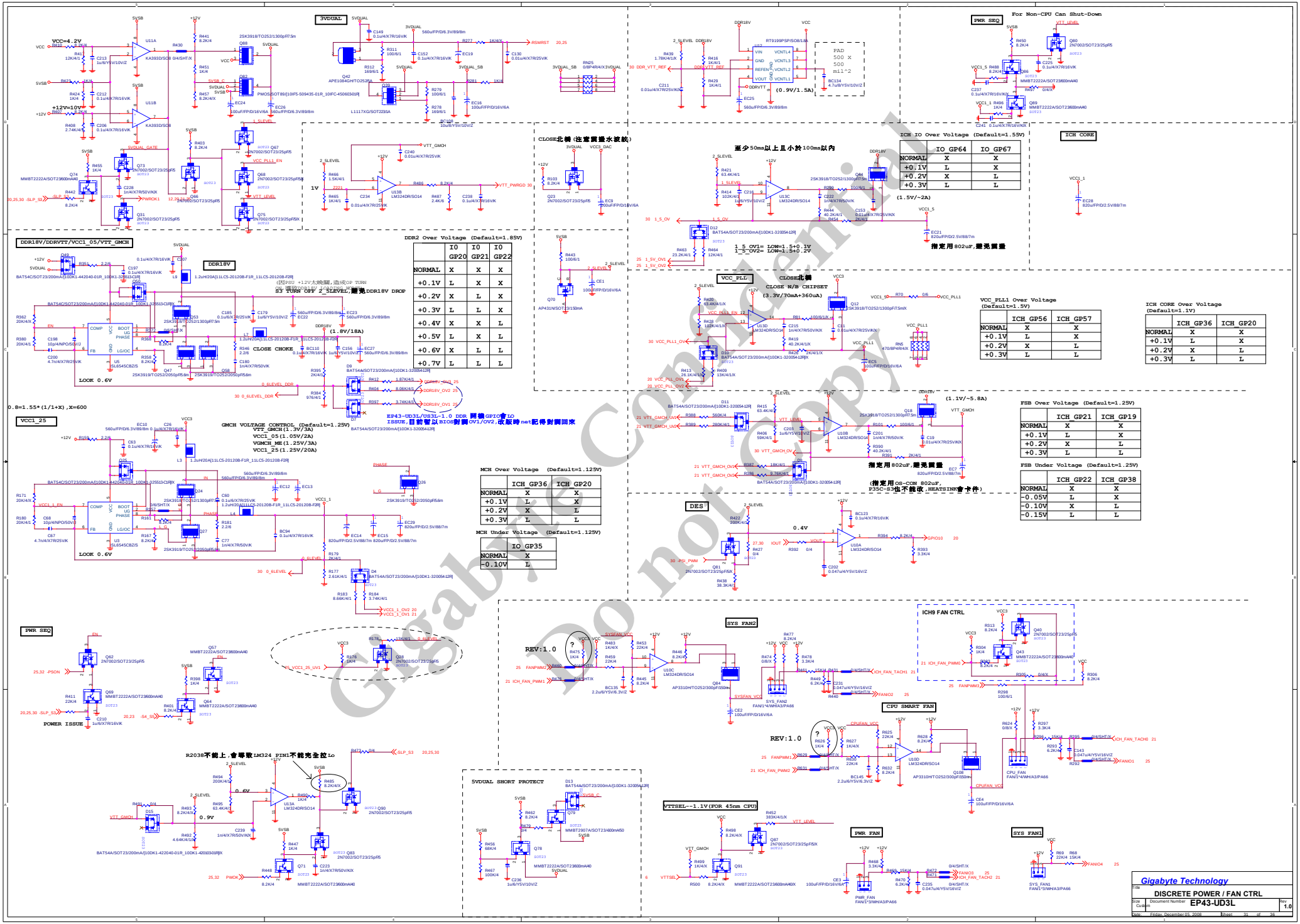
Gigabyte Technology

VRD 11 -ISL6334

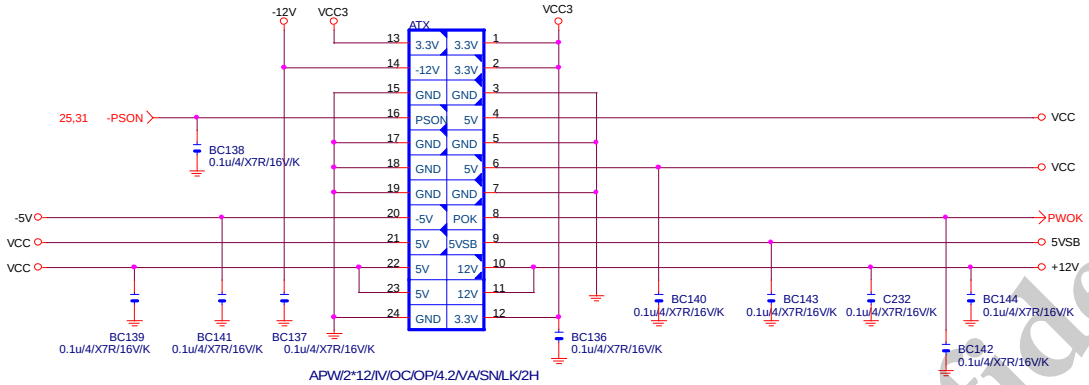
EP43-UD3L

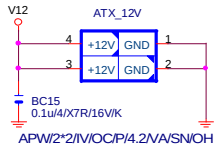
Rev 1.0

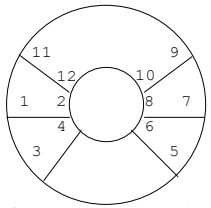
Friday, December 05, 2008

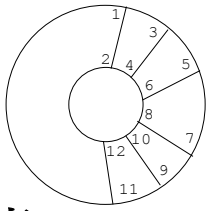


ATX POWER CONNECTOR

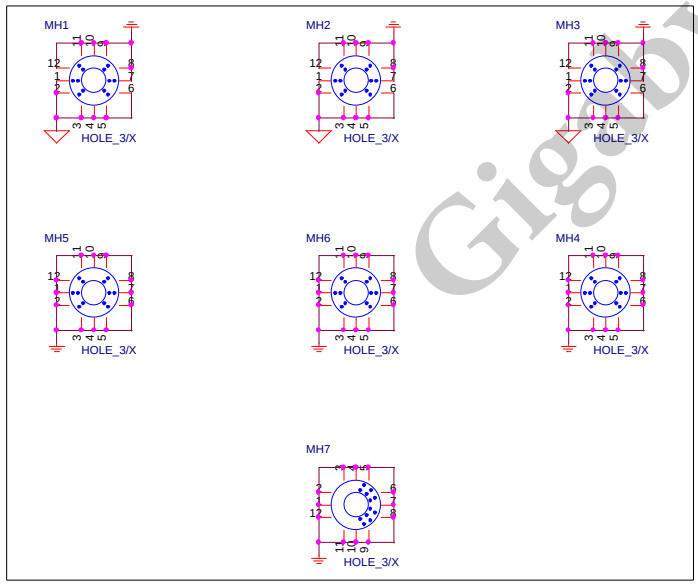


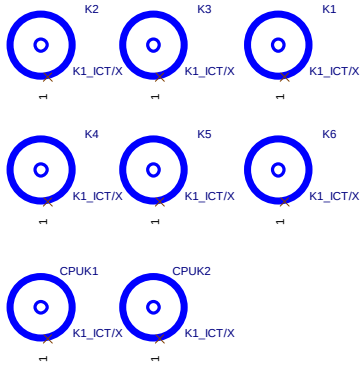


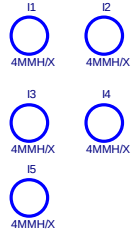




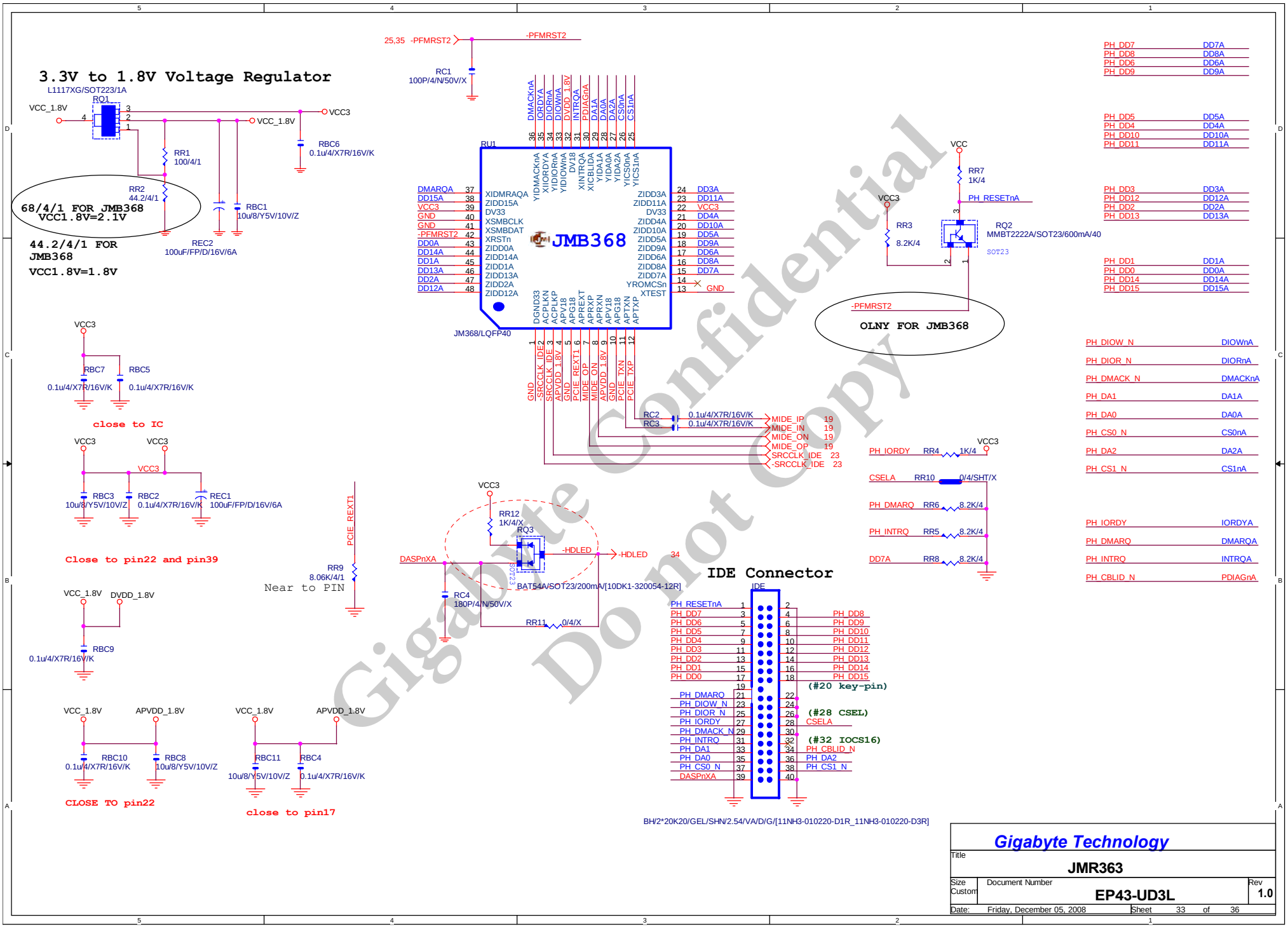
螺絲孔位置圖 (注意Footprint不同)

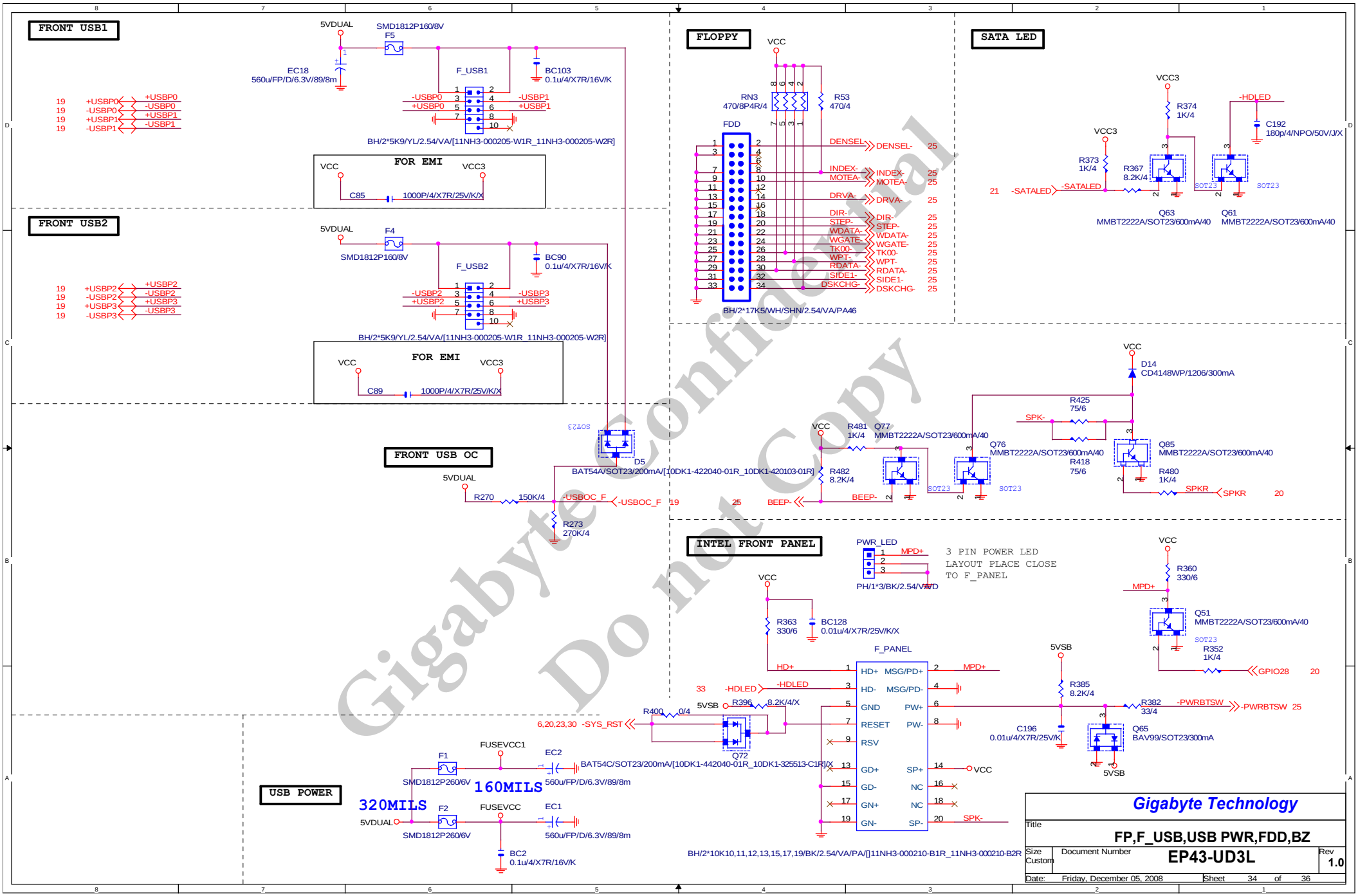


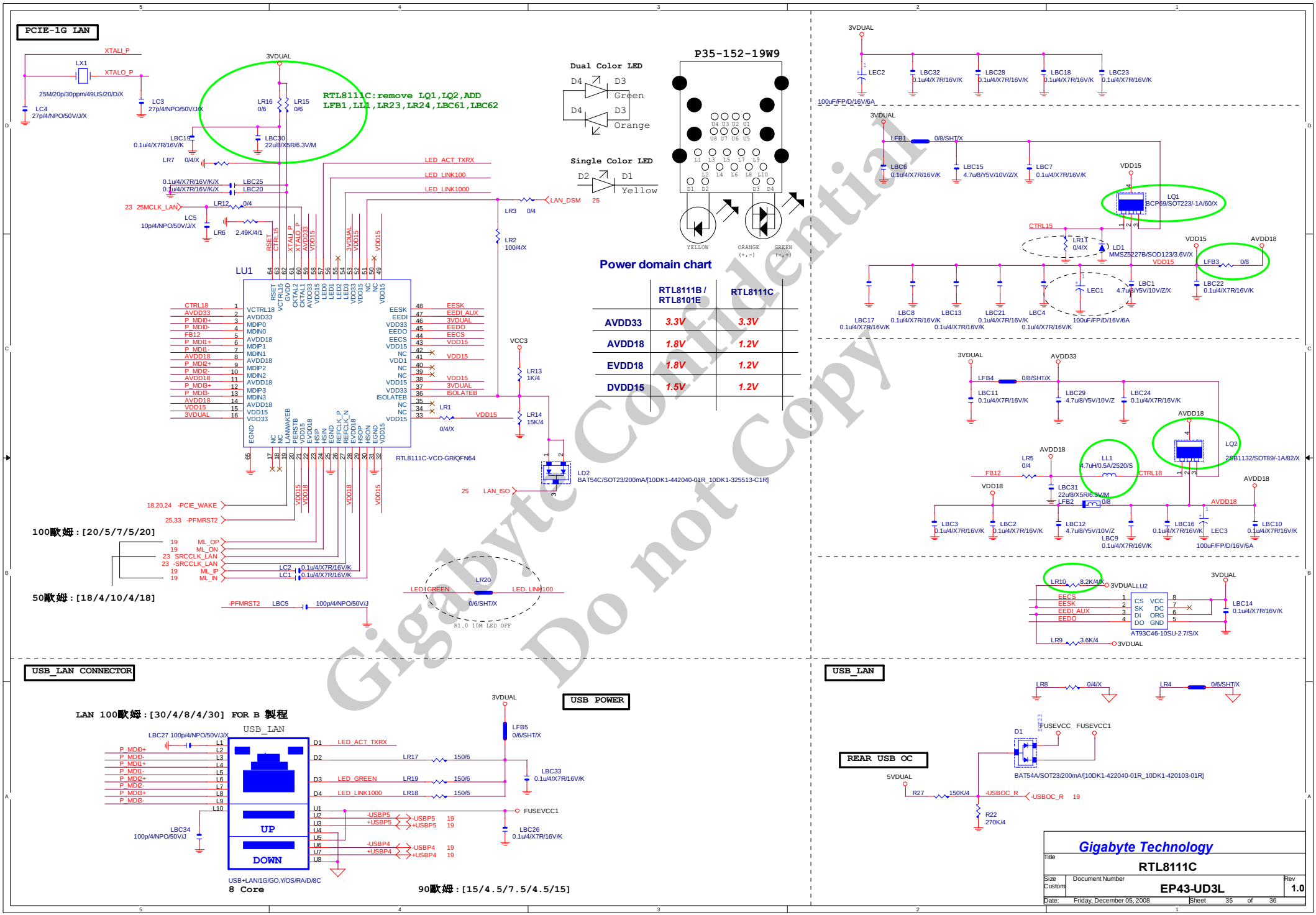


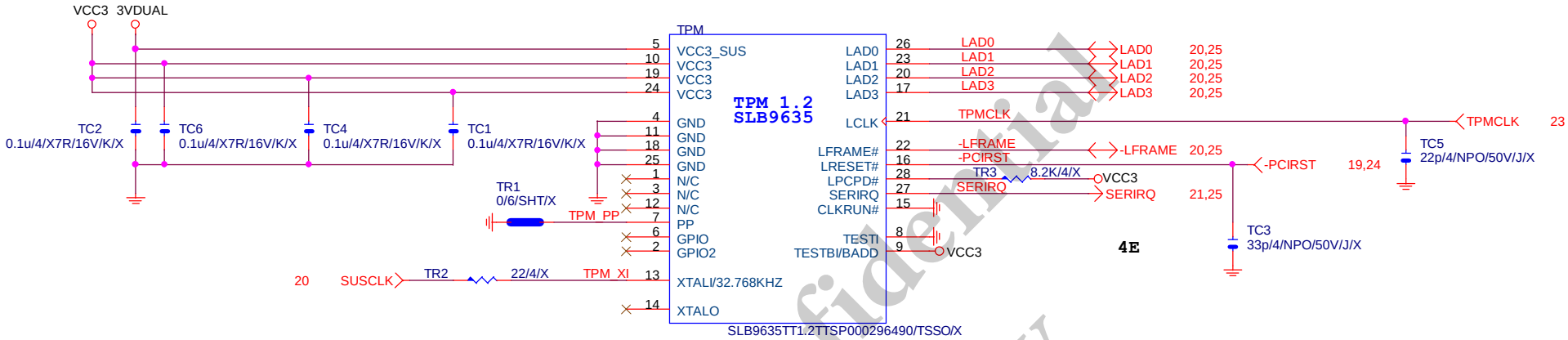


Gigabyte Technology		
Title: ATX POWER CONNECTOR		
Size: B	Document Number: EP43-UD3L	Rev: 1.0
Date: Friday, December 05, 2008	Sheet 32 of 36	









GIGABYTE THCHNOLOGIES		
Title: TPM I/F-SLB 9635 TT 1.2		
Size: Custom	Document Number: EP43-UD3L	Rev: 1.0
Date: Friday, December 05, 2008	Sheet 36 of 36	