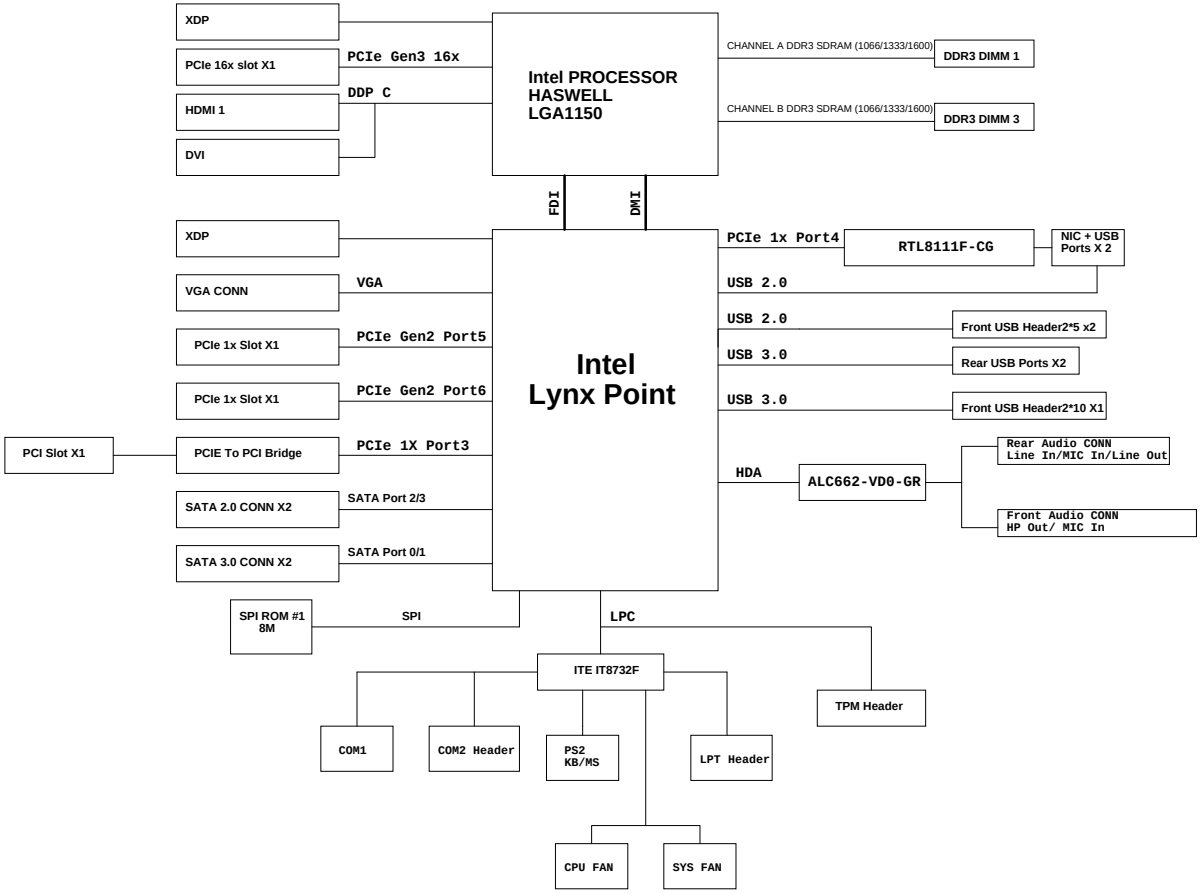
B85M01

FAB:A



FOXCONN PCEG

Title: Index / Block diagram

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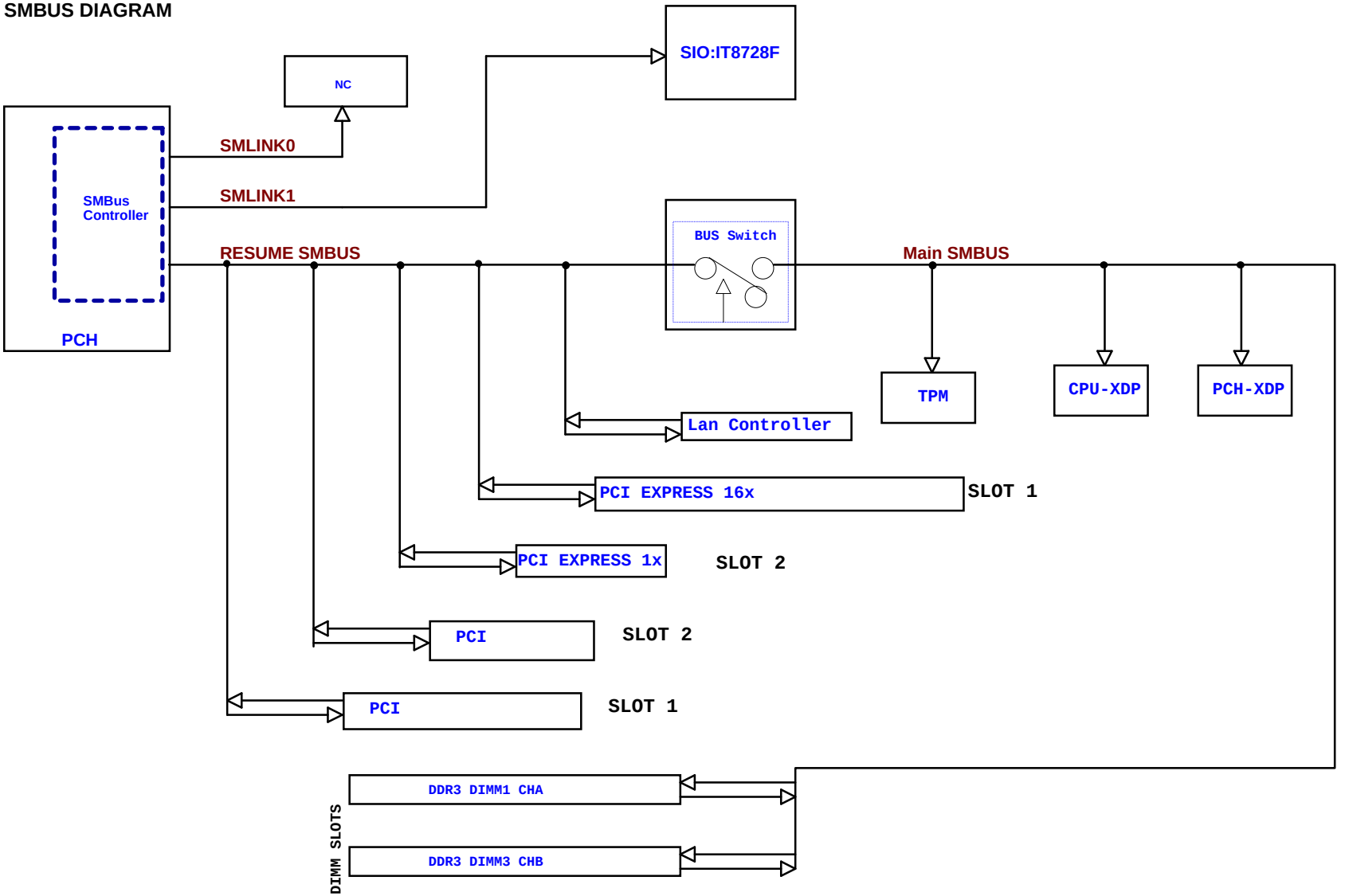
SMBUS DIAGRAM



FOXCONN PCEG

Title: SMBus MAP

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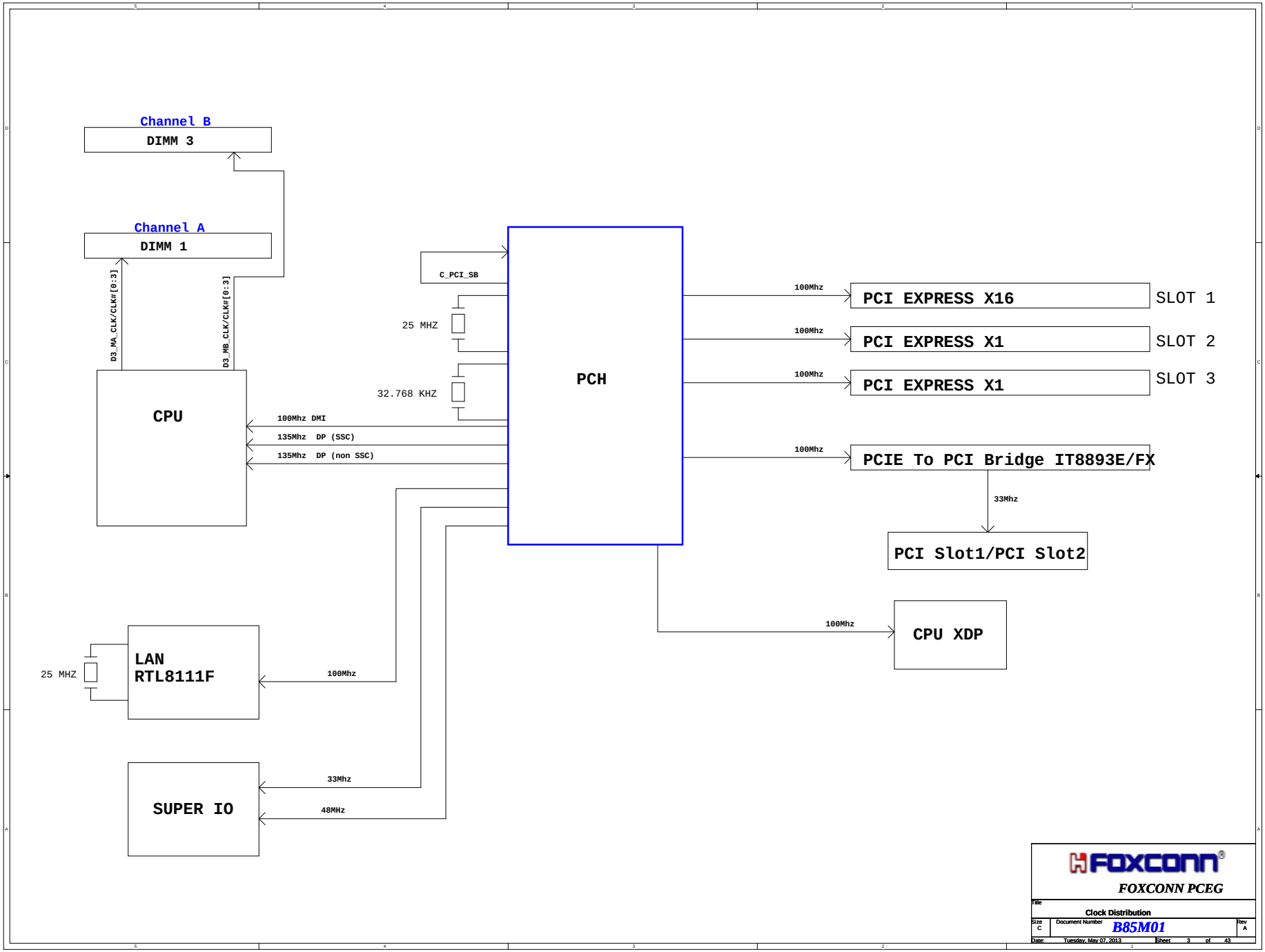
Channel B
DIMM 3
Channel A
DIMM 1
D3_MA_CLK/CLK#[0:3]
D3_MB_CLK/CLK#[0:3]
CPU
C_PCI_SB
25 MHZ
32.768 KHZ
PCH
100Mhz DMI
135Mhz DP (SSC)
135Mhz DP (non SSC)
100Mhz
PCI EXPRESS X16
SLOT 1
100Mhz
PCI EXPRESS X1
SLOT 2
100Mhz
PCI EXPRESS X1
SLOT 3
100Mhz
PCIE To PCI Bridge IT8893E/FX
33Mhz
PCI Slot1/PCI Slot2
100Mhz
CPU XDP
25 MHZ
LAN
RTL8111F
100Mhz
33Mhz
SUPER IO
48MHz
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Clock Distribution
Size
C
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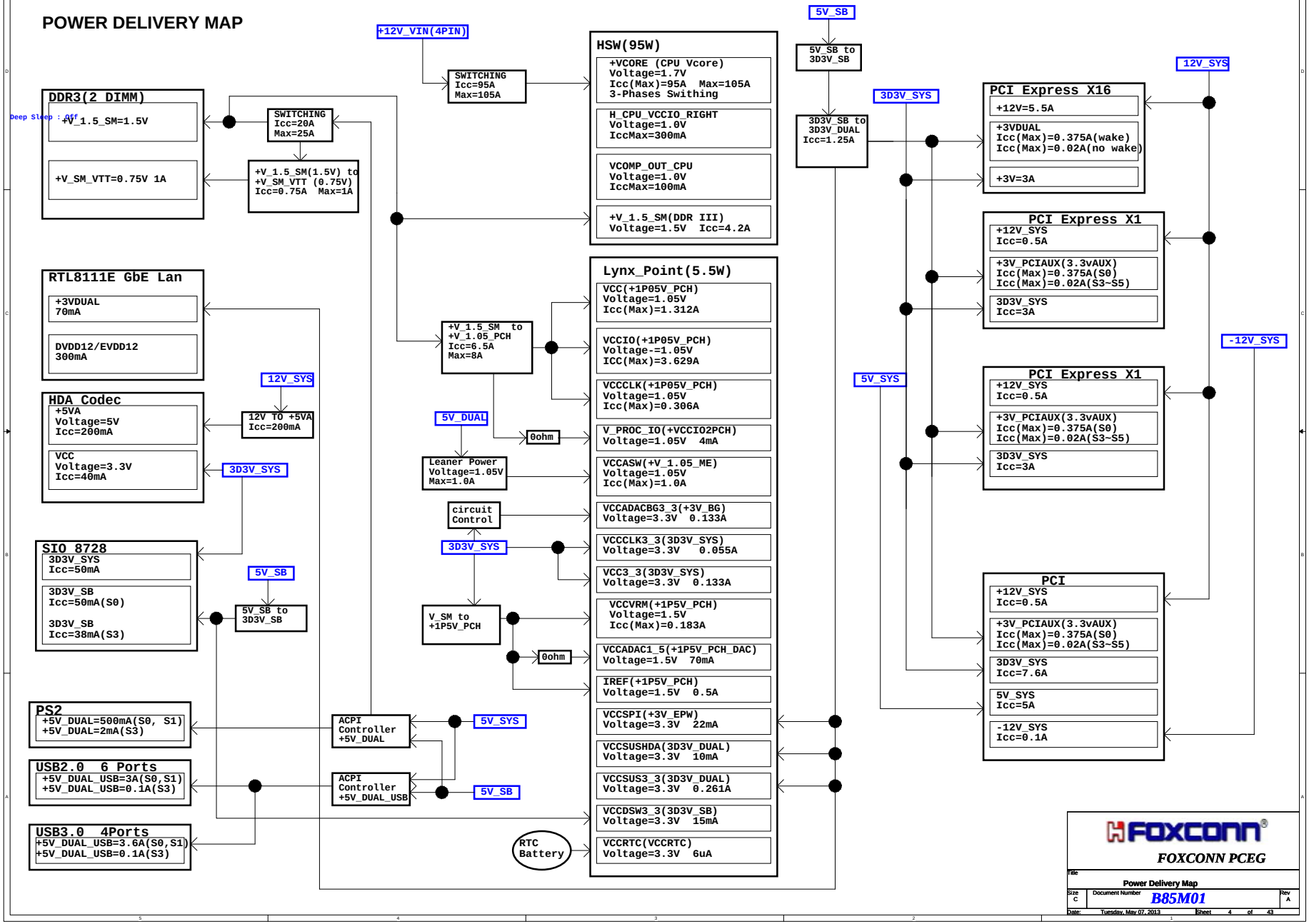
POWER DELIVERY MAP



FOXCONN PCEG

Title: Power Delivery Map

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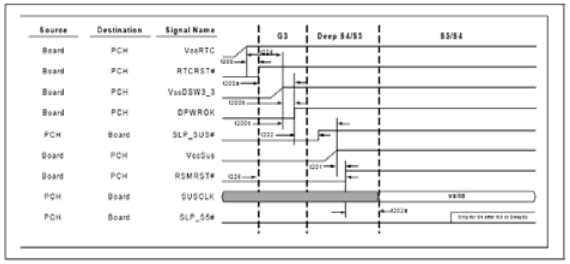
Figure 8-1. G3 w/RTC Loss to S4/S5 (With Deep Sx Support) Timing Diagram



Note: VCCSUS rail ramps up later in comparison to VCCDSW due to assumption that SLP_SUS# is used to control power to VCCSUS.

Figure 8-2. G3 w/RTC Loss to S4/S5 (Without Deep Sx Support) Timing Diagram

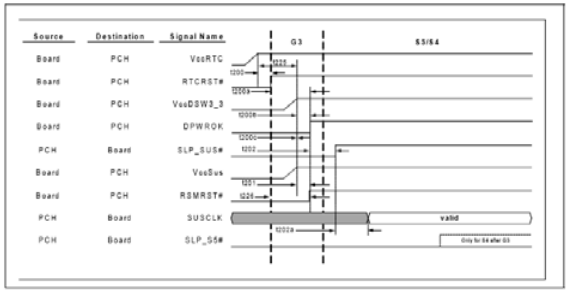
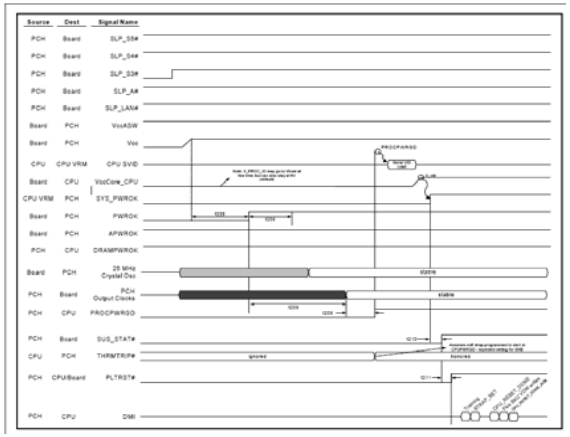


Figure 8-4. S3/M3 to S0 Timing Diagram



S5/Moff - S5/M3 Timing Diagram

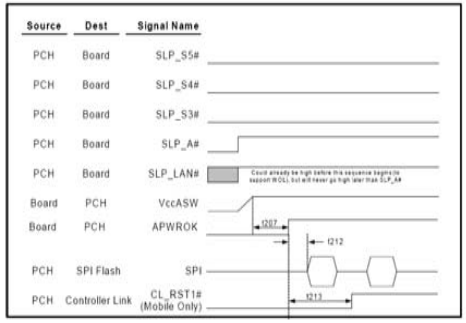
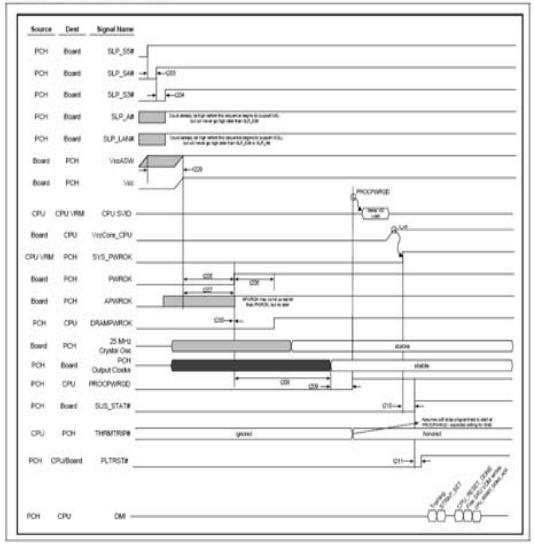
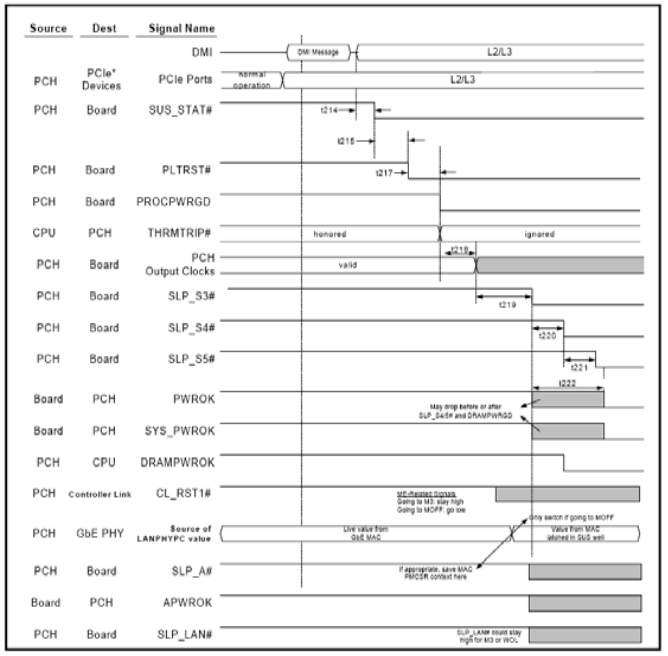


Figure 8-3. S5 to S0 Timing Diagram



S0 to S5 Timing Diagram



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Title: Power On Sequence

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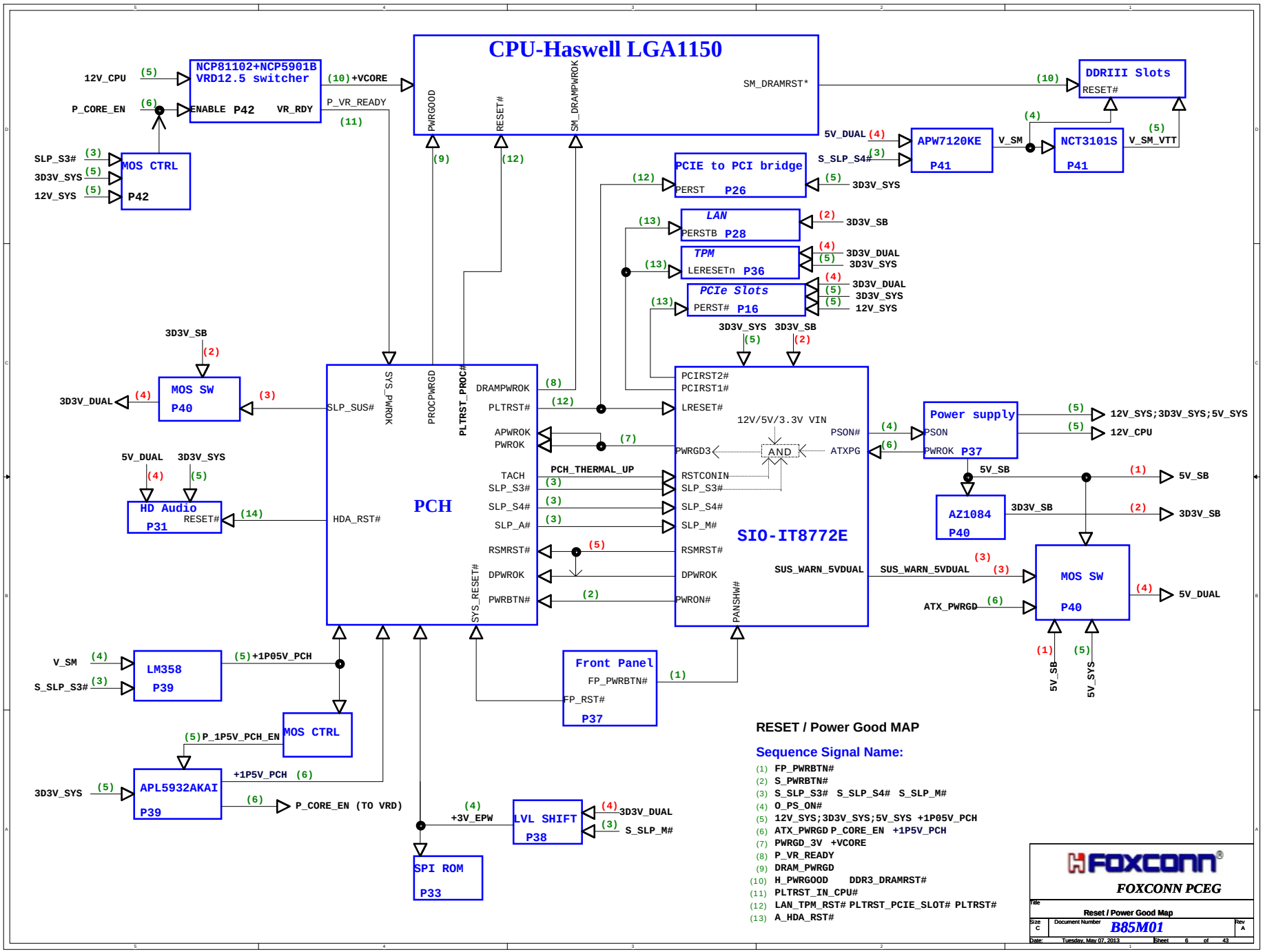

RESET / Power Good MAP

Sequence Signal Name:

(1) FP_PWRBTN#
(2) S_PWRBTN#
(3) S_SLP_S3# S_SLP_S4# S_SLP_M#
(4) O_PS_ON#
(5) 12V_SYS;3D3V_SYS;5V_SYS +1P05V_PCH
(6) ATX_PWRGD P_CORE_EN +1P5V_PCH
(7) PWRGD_3V +VCORE
(8) P_VR_READY
(9) DRAM_PWRGD
(10) H_PWRGOOD DDR3_DRAMRST#
(11) PLTRST_IN_CPU#
(12) LAN_TPM_RST# PLTRST_PCIE_SLOT# PLTRST#
(13) A_HDA_RST#

FOXCONN PCEG

Title: Reset / Power Good Map
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STRAPPING Table

CPU side

CFG[17:0]	Description	
[2]	PCI Express static x16 lane numbering reversal	1: normal Default 0: lane numbers reversed
[6:5]	PCI Express Bifurcation	00: 1x8, 2x4 PCI Express 01: reserved 10: 2x8 PCI Express 11: 1x16 PCI Express Default

Strapping Options Flash

value	SATA1GP/GPIO19	Routing
0	0	Flash Cycles Routed to LPC
1	0	Flash Cycles Routed to PCI
0	1	Flash Cycles Routed to SPI

Table 34-6. PCH Digital Display Strapping Signals

Checklist Item	Recommendations	Direction	Comments
DDPx_CTRLDATA	Straps for digital port B, C and D. For DisplayPort* - Should be pulled to 3.3V through a 2.2K W resistor to configure digital port. For DVI/HDMI configuration, the signal should be routed through the level shifter to the display connector. The signal is pulled to 3V before the level shifter and 5V before the display connector through a 2.2KW resistor. This signal should always be routed longer than DDPC_CTRLCLK by an inch. For DVI/HDMI configuration with the Cost Reduced level shifter, the signal should be routed through the pass gate sourced from 3.3V voltage. The signal is pulled to 3V before the pass gate and 5V before the display connector through a 2.2KW resistor and a Schottky diode. This signal should always be routed longer than DDPC_CTRLCLK by an inch. Also ensure schottky diode is not shared with DDPC_CTRLCLK.	BI	

Table 36-18. Strapping Signals (Sheet 1 of 2)

Name	Type	Recommendations	Reason/Impact
SPKR	I	**Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2k-10k Ohm weak pull-up resistor.	
INIT3_3V#	I	Do not pull low.	
GPIO55	I/O	**Default Mode:** Internal pull-up. **Top Block Swap Mode:** Connect to ground with 4.7k Ohm weak pull-down resistor.	
SATA1GP/ GPIO19, GPIO51	I/O	**Default (SPI)** Left both SATA1GP/GPIO19 and GPIO51 floating. No pull up required. **Boot from PCI** Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor. Leave GPIO51 Floating. **Boot from LPC** Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.	If LPC is selected BIOS may still be placed on LPC, but all platforms with PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN.
GPIO53	I/O	Do not pull low. Connect to ground with 1k Ohm pull-down resistor.	ESI strap for server platform ONLY
HDA_SDO	I/O	**Default** Do not pull high. **Disable ME in Manufacturing Mode** Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.	Flash descriptor Override
SPI_MOSI	I/O	Internal weak pull down.Do not pull high.	DMI RX Termination Voltage
SAAT3GP/ GPIO37	I/O	**Enable TLS:** Pull up with 1k Ohm to VccSus3.3. **Default (Disable TLS):** Leave NC. Internal pull down.	TLS confidentiality
GPIO8	I/O	Internal weak pull up.Do not pull low.	

Table 36-18. Strapping Signals (Sheet 2 of 2)

Name	Type	Recommendations	Reason/Impact
GPIO62/ SUSCLK	I/O	Internal weak pull up. Do not pull low.	On die PLL voltage regulator
GPIO36	I/O	Internal weak pull down. Do not pull high.	
DDPB_CTRL_DATA DDPC_CTRL_DATA DDPD_CTRL_DATA		Straps for digital ports B, C and D. For DisplayPort* - Should be pulled to 3.3V through a 2.2K ohms resistor to configure digital port. For DVI/HDMI configuration, the signal should be routed through the level shifter to the display connector. The signal is pulled to 3V before the level shifter and 5V before the display connector through a 2.2k ohms resistor. This signal should always be routed longer than SDVO/ DDPC_CTRLCLK by an inch. For DVI/HDMI configuration with the Cost Reduced level shifter, the signal should be routed through the pass gate sourced from 3.3V voltage to the display connector. The signal is pulled to 3V before the pass gate and 5V before the display connector through a 2.2k ohmsresistor. This signal should always be routed longer than SDVO/DDPC_CTRLCLK by an inch.	

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Title: Strap/IRQ/IDSel Table

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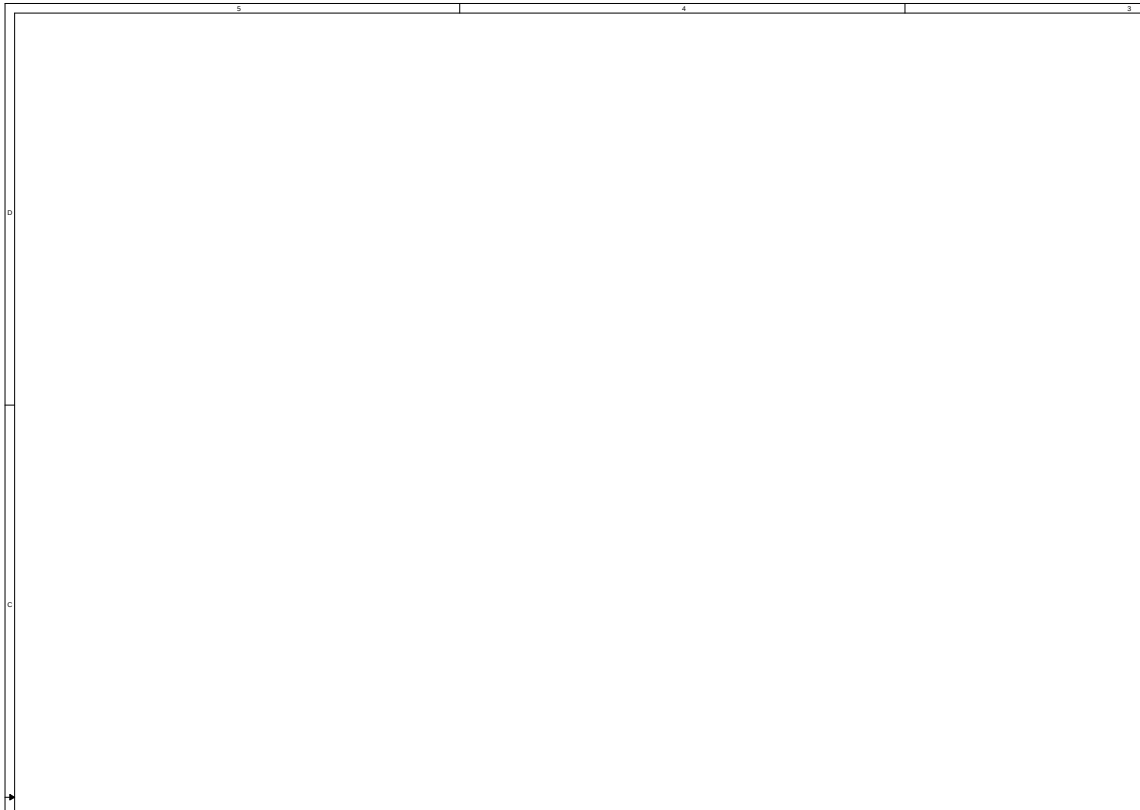
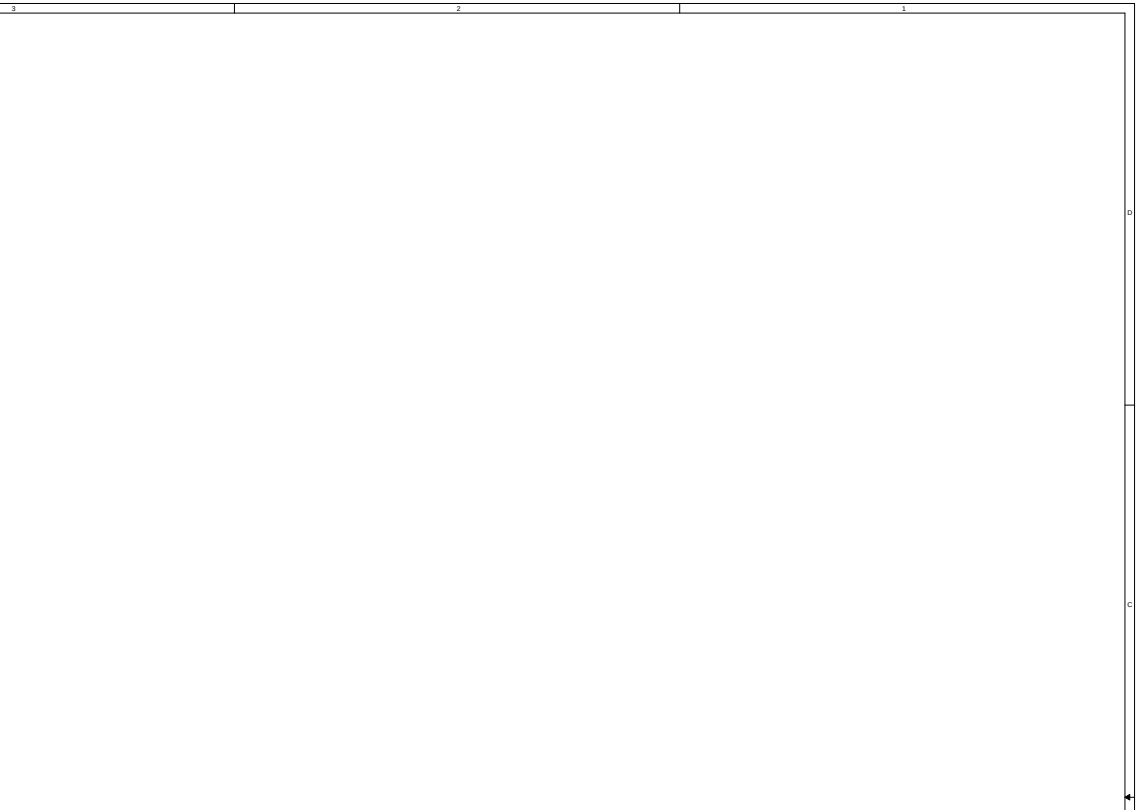

5
4
3
D
C


3
2
1
D
C

B

A

5

4

3

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Title: GPIO Table

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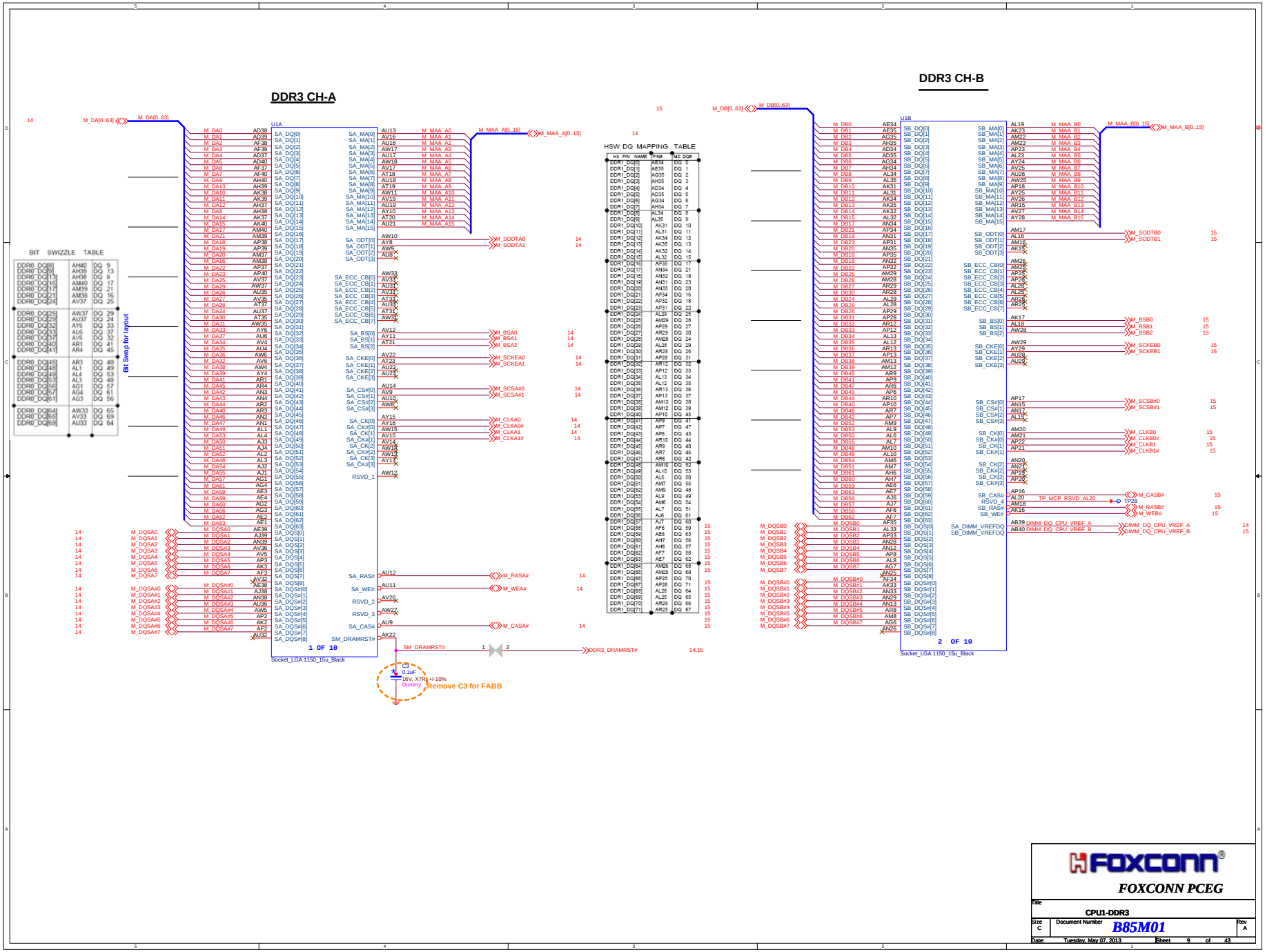

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Title	CPU1-DDR3		
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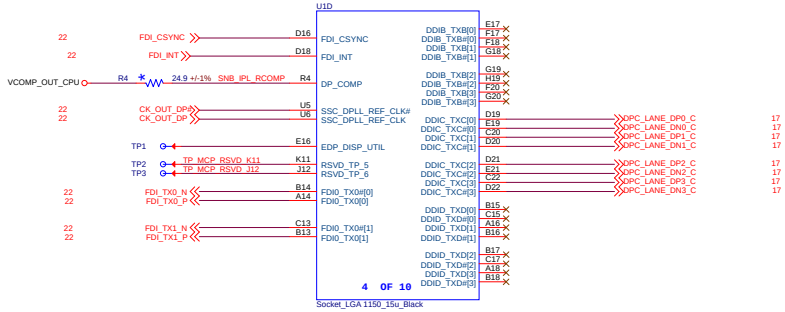

HDMI 1

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Title: CPU2-PEGX16/DMI/FDI/DDI

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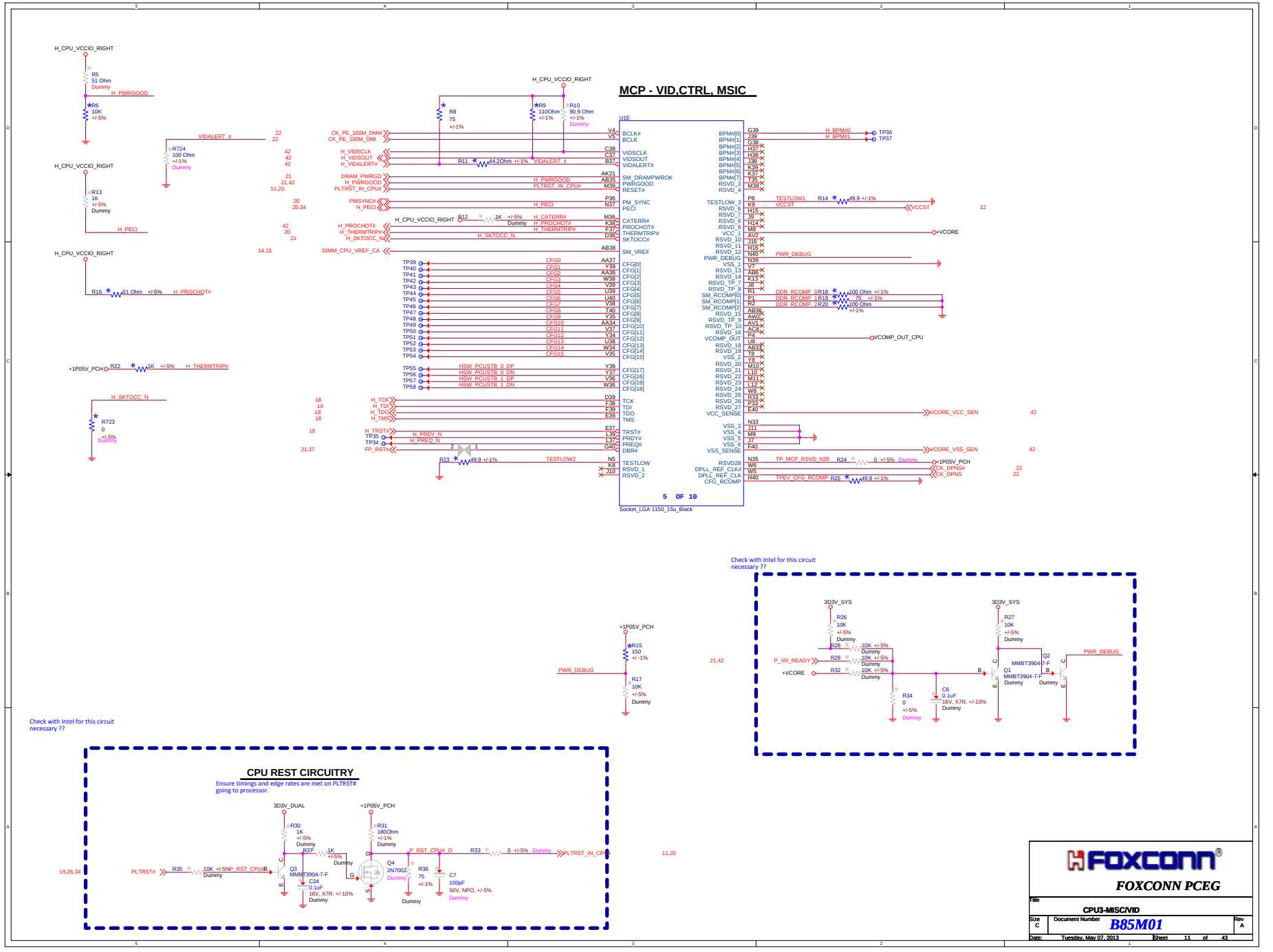
MCP - VID,CTRL, MSIC
U1E
5 OF 10
Socket_LGA 1150_15u_Black
H_CPU_VCCIO_RIGHT
H_PWRGOOD
VIDALERT_#
H_PECI
H_SKTOCC_N
H_PROCHOT#
+1P05V_PCH
H_THERMTRIP#
TESTLOW2
PWR_DEBUG
VCCST
+VCORE
VCOMP_OUT_CPU
VCORE_VCC_SEN
VCORE_VSS_SEN
TP_MCP_RSVD_N35
TPEV_CFG_RCOMP
DDR_RCOMP_0
DDR_RCOMP_1
DDR_RCOMP_2
CK_DPNS#
CK_DPNS
Check with Intel for this circuit necessary ??
CPU REST CIRCUITRY
Ensure timings and edge rates are met on PLTRST# going to processor.
3D3V_DUAL
3D3V_SYS
P_VR_READY
P_RST_CPU#
PLTRST#
PLTRST_IN_CPU
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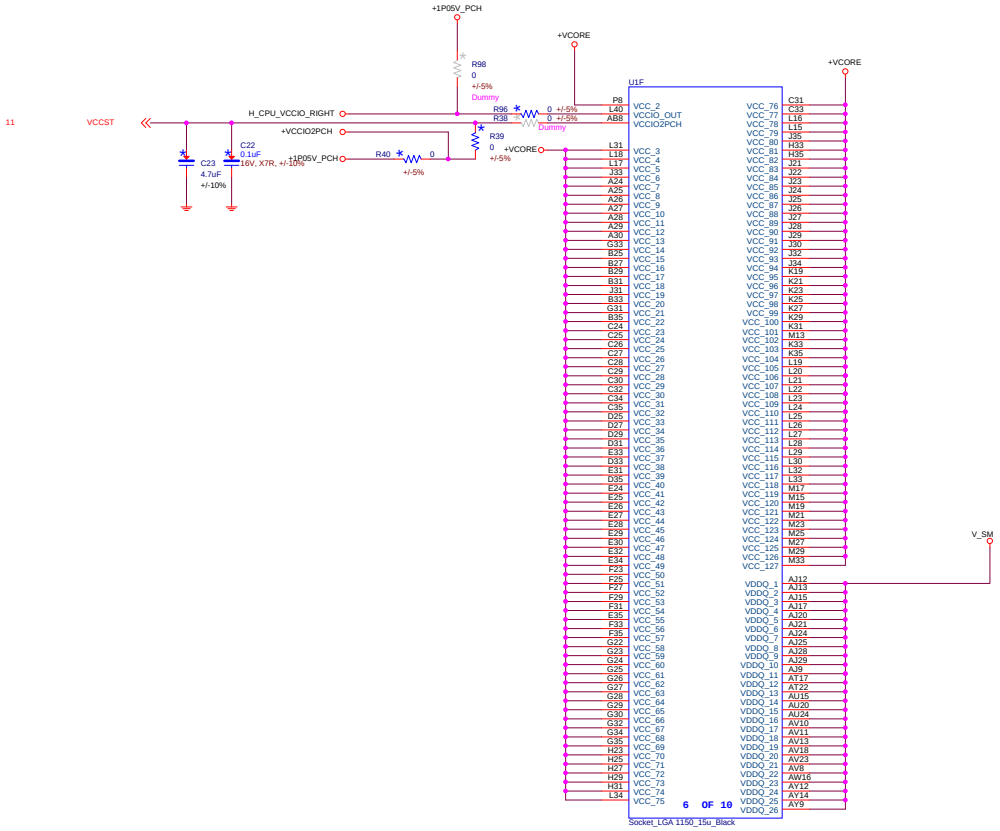

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Title: CPU4-Vcore

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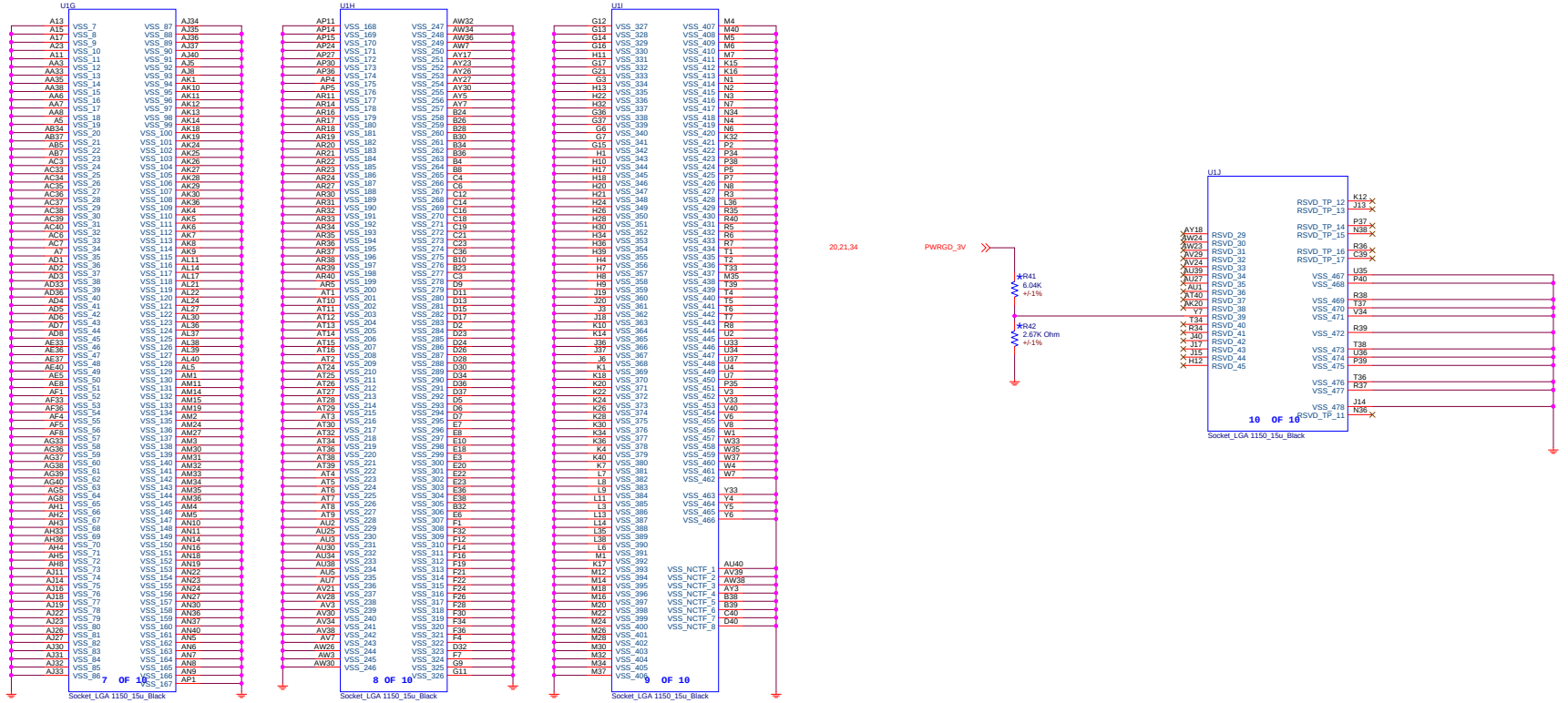
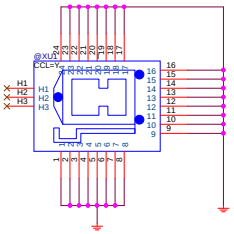
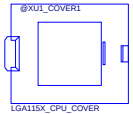


CPU_Loding Module (DIP)

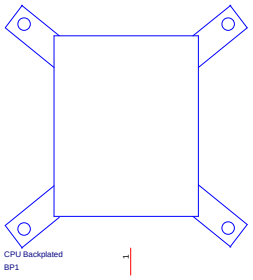


CPU_Plastic Cover (DIP)

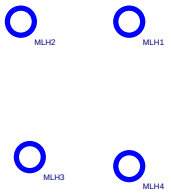


CPU_FAN Back plate (DIP)

Non-PTH Hole



mylar PAD for CPU_FAN back plate



FOXCONN

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Title: CPU5-GND

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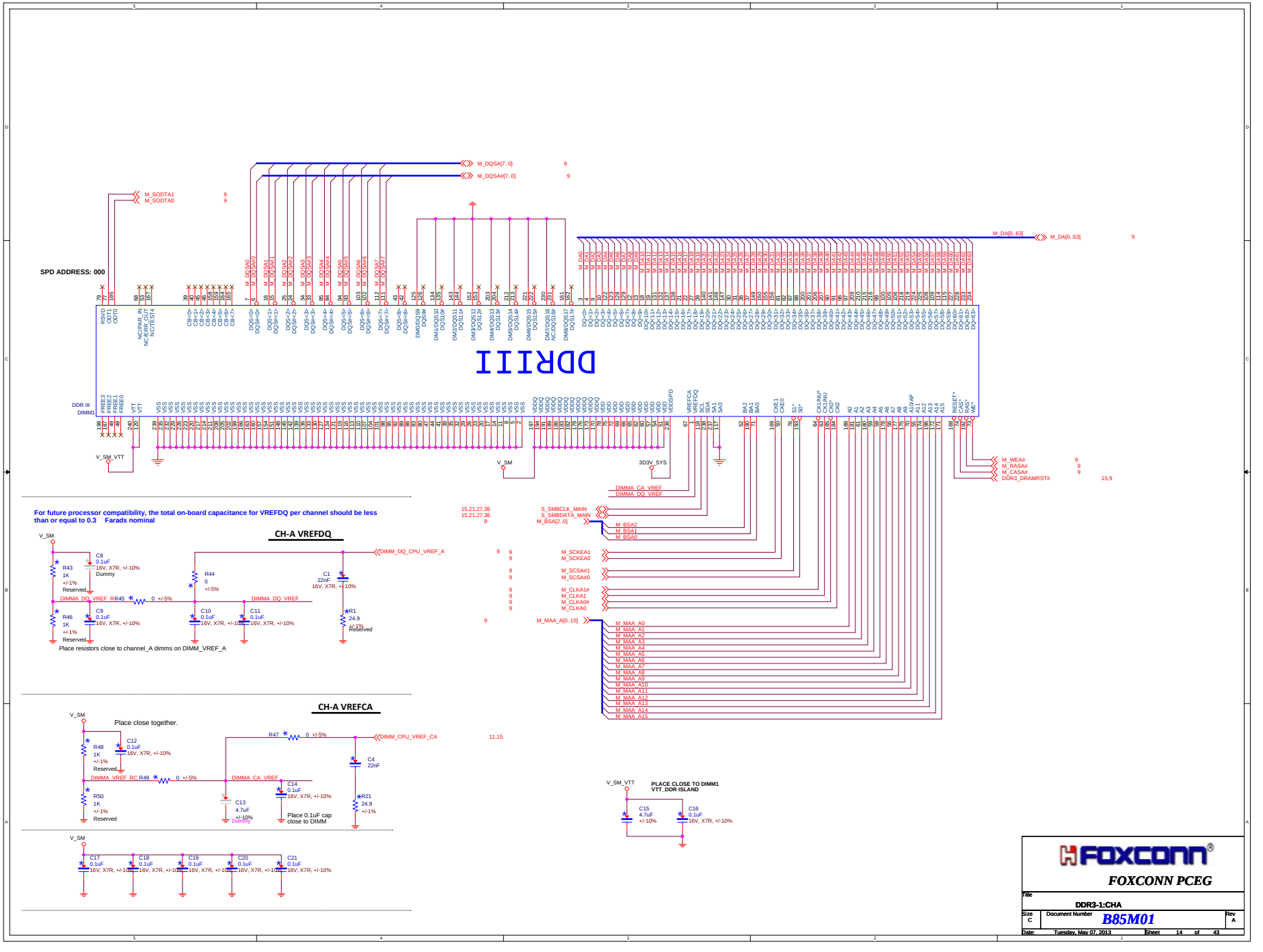

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Title: DDR3-1:CHA

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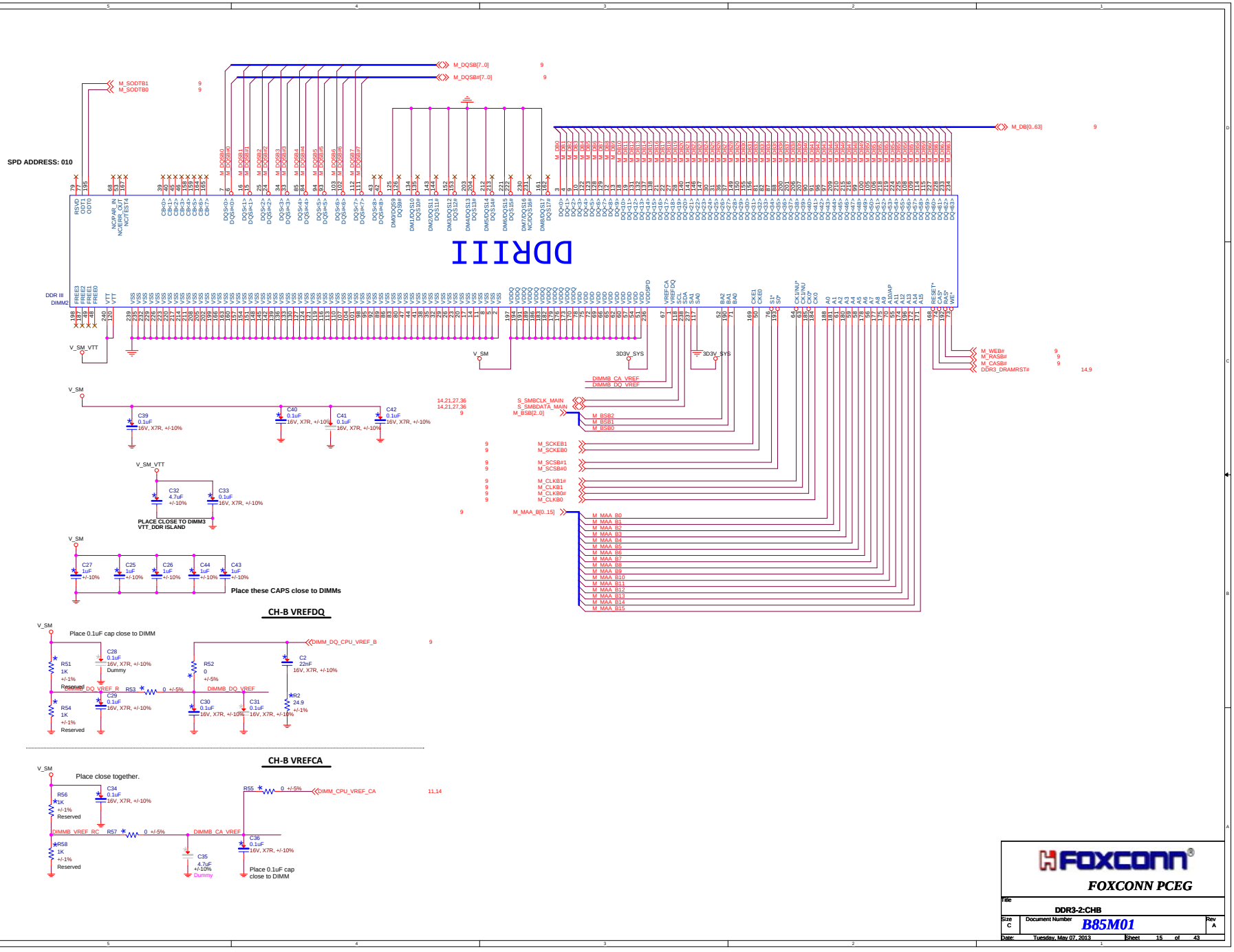
SPD ADDRESS: 010
DDRIII
DDR III DIMM2
M_SODTB1
M_SODTB0
M_DQSB[7..0]
M_DQSB#[7..0]
M_DB[0..63]
V_SM_VTT
V_SM
3D3V_SYS
DIMMB_CA_VREF
DIMMB_DQ_VREF
S_SMBCLK_MAIN
S_SMBDATA_MAIN
M_BSB[2..0]
M_SCKEB1
M_SCKEB0
M_SCSB#1
M_SCSB#0
M_CLKB1#
M_CLKB1
M_CLKB0#
M_CLKB0
M_MAA_B[0..15]
M_WEB#
M_RASB#
M_CASB#
DDR3_DRAMRST#
PLACE CLOSE TO DIMM3 VTT_DDR ISLAND
Place these CAPS close to DIMMs
CH-B VREFDQ
Place 0.1uF cap close to DIMM
DIMM_DQ_CPU_VREF_B
DIMMB_DQ_VREF_R
CH-B VREFCA
Place close together.
DIMM_CPU_VREF_CA
DIMMB_VREF_RC
Place 0.1uF cap close to DIMM
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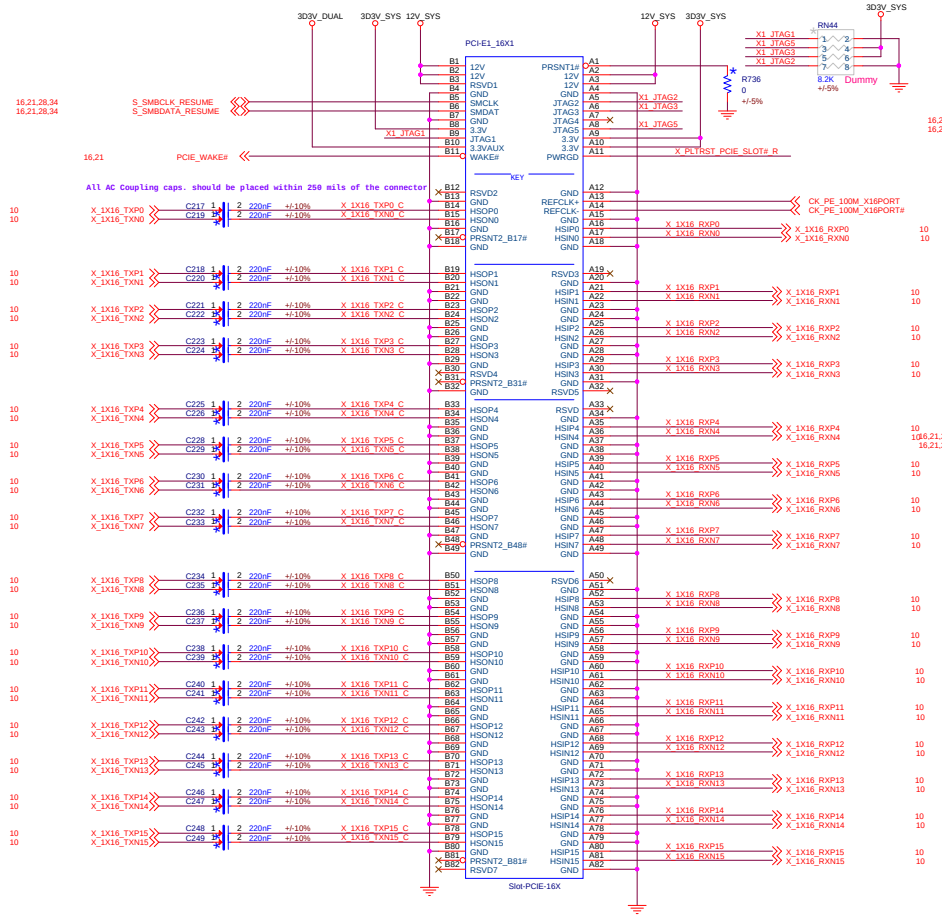
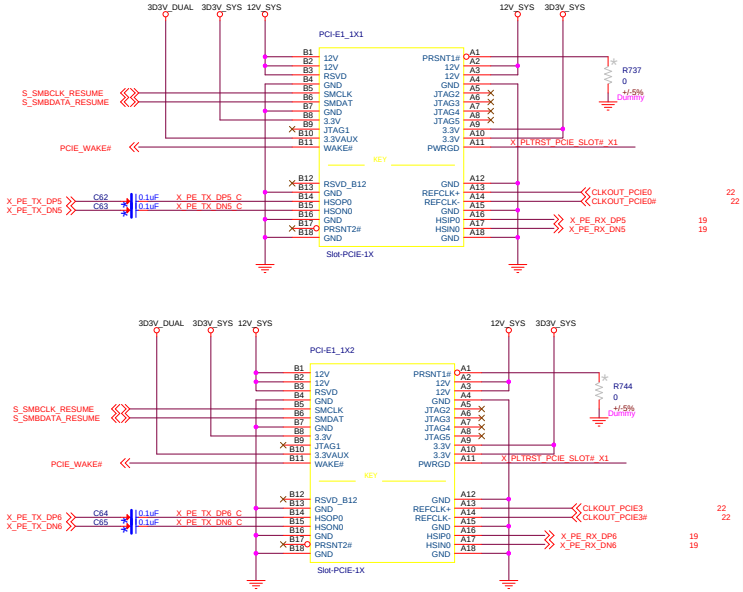
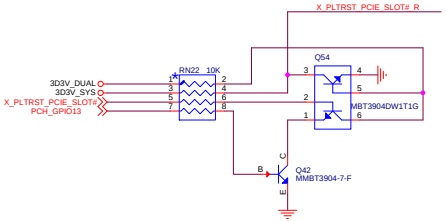
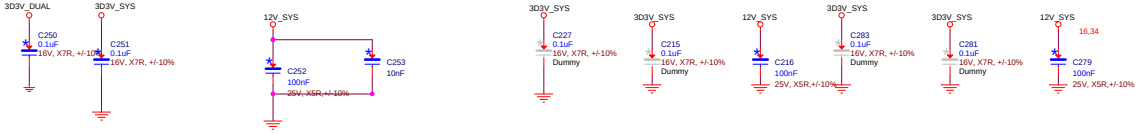
PCI EXPRESS x16 SLOT



PCI EXPRESS X1 SLOT1







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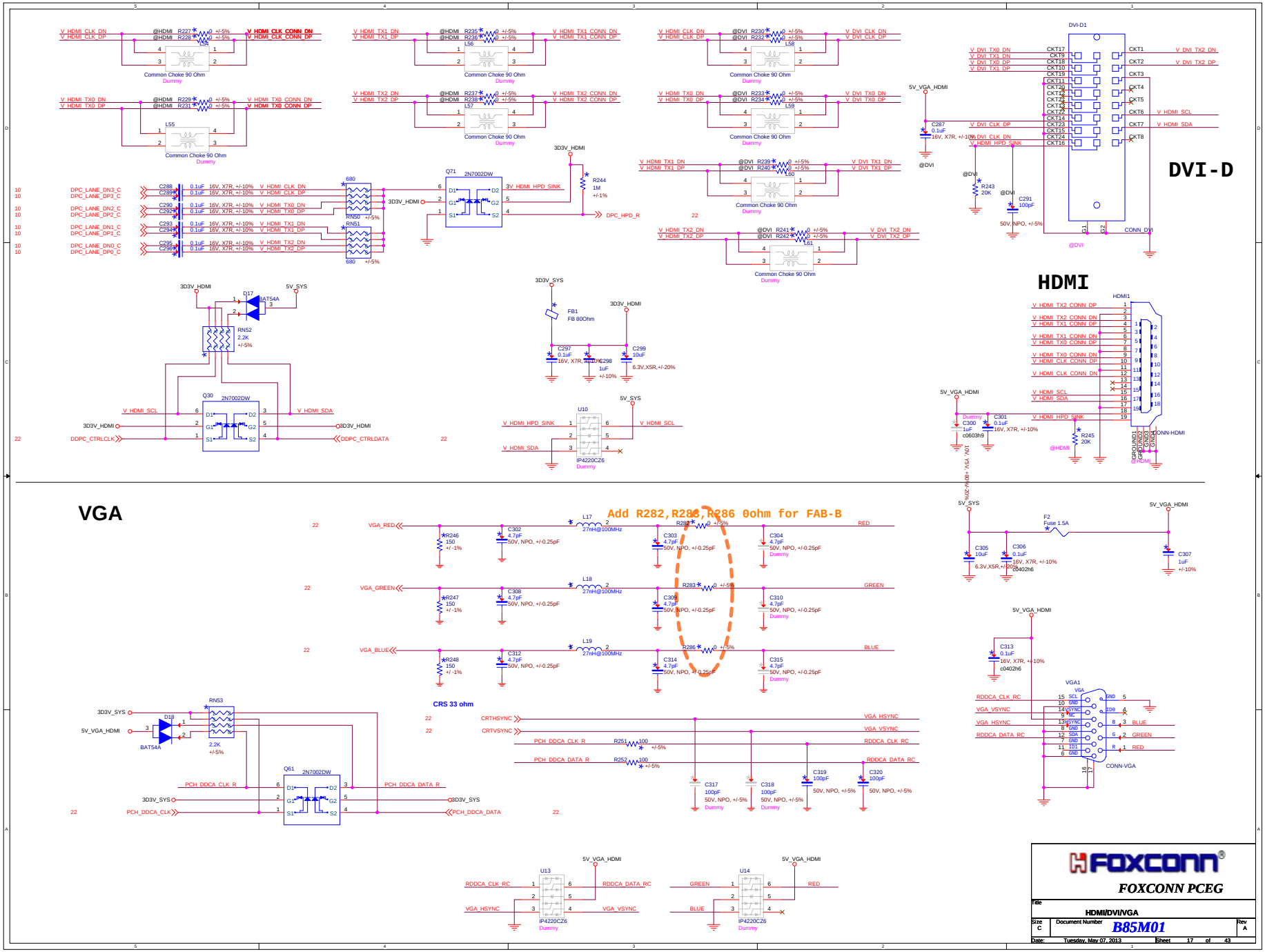
DVI-D
HDMI
VGA
Add R282,R285,R286 0ohm for FAB-B
CRS 33 ohm
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HDMI/DVI/VGA
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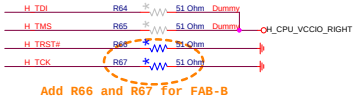
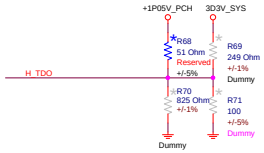
Intel CPU XDP Debug Connector



Add R66 and R67 for FAB-B



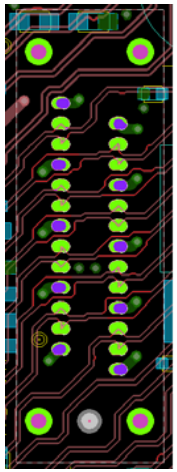
Intel DMI LAI Footprint

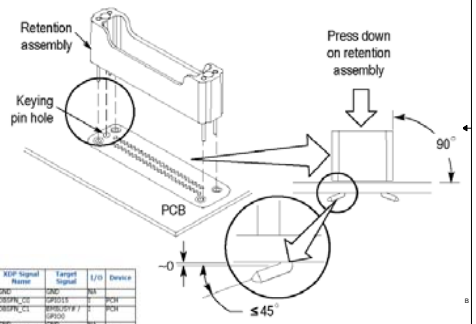
Table 3-1. Processor XDP Connector Pinout

Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	GND	GND	NA		2	GND	GND	NA	
3	OBSFN_A0	PREQ#	I/O	processor	4	OBSFN_C0	CFG[16]	I/O	Processor
5	OBSFN_A1	PRDY#	I/O	processor	6	OBSFN_C1	CFG[17]	I/O	Processor
7	GND	GND	NA		8	GND	GND	NA	
9	OBSDATA_A0	BPM#[0]	I/O	processor	10	OBSDATA_C0	CFG[0]	I/O	Processor
11	OBSDATA_A1	BPM#[1]	I/O	processor	12	OBSDATA_C1	CFG[1]	I/O	Processor
13	GND	GND	NA		14	GND	GND	NA	
15	OBSDATA_A2	BPM#[2]	I/O	processor	16	OBSDATA_C2	CFG[2]	I/O	Processor
17	OBSDATA_A3	BPM#[3]	I/O	processor	18	OBSDATA_C3	CFG[3]	I/O	Processor
19	GND	GND	NA		20	GND	GND	NA	
21	OBSFN_B0	CFG[10]	I/O	Processor	22	OBSFN_D0	CFG[8]	I/O	Processor
23	OBSFN_B1	CFG[11]	I/O	Processor	24	OBSFN_D1	CFG[9]	I/O	Processor
25	GND	GND	NA		26	GND	GND	NA	
27	OBSDATA_B0	BPM#[4] / CFG[12]	I/O	processor	28	OBSDATA_D0	CFG[4]	I/O	Processor
29	OBSDATA_B1	BPM#[5] / CFG[13]	I/O	processor	30	OBSDATA_D1	CFG[5]	I/O	Processor
31	GND	GND	NA		32	GND	GND	NA	
33	OBSDATA_B2	BPM#[6] / CFG[14]	I/O	processor	34	OBSDATA_D2	CFG[6]	I/O	Processor
35	OBSDATA_B3	BPM#[7] / CFG[15]	I/O	processor	36	OBSDATA_D3	CFG[7]	I/O	Processor
37	GND	GND	NA		38	GND	GND	NA	
39	HOOK0	PWRGOOD	I	system	40	ITPCLK/HOOK4	BCLK_ITP	I	processor
41	HOOK1	BP_PWRGD_RST#	O	system	42	ITPCLK#/ HOOK5	BCLK_ITP#	I	processor
43	VCC_OBS_AB	VCCP Voltage of the processor	I		44	VCC_OBS_CD	VCCP Voltage of the processor	I	
45	HOOK2	CFG[0]	O	processor	46	HOOK6/ RESET#	RESET#	I	processor
47	HOOK3	VR_READY/ SYS_PWROK	O	System	48	HOOK7/DBR#	DBR#	O	processor
49	GND	GND	NA		50	GND	GND	NA	
51	SDA	SDA	I/O	system	52	TDO	TDO	O	processor
53	SCL	SCL	I/O	system	54	TRSTn	TRST#	O	processor
55	TCK1	Open	NA		56	TDI	TDI	O	processor
57	TCK0	TCK	O	processor	58	TMS	TMS	O	processor
59	GND	GND	NA		60	GND	GND (or XDP_PRESENT# if required)	NA	

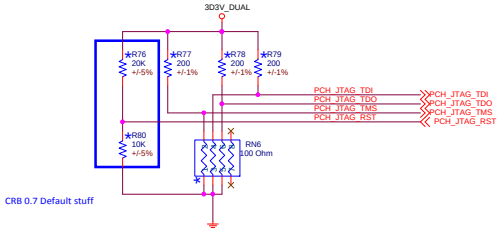
This is footprint only . BOM is Dummy

Change for FAB-B





Intel PCH XDP Debug Connector



CRB 0.7 Default stuff

21
21
21
21

Change for FAB-B

Change for FAB-B

Table 4-1. PCH XDP Connector Pinout

Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	GND	GND	NA		2	GND	GND	NA	
3	OBSFN_A0	Open	NA		4	OBSFN_C0	GPIO19	I	PCH
5	OBSFN_A1	Open	NA		6	OBSFN_C1	BMBUSY# / GPIO20	I	PCH
7	GND	GND	NA		8	GND	GND	NA	
9	OBSDATA_A0	OCP# / GPIO59	I	PCH	10	OBSDATA_C0	HOOK0 / GPIO58	I	PCH
11	OBSDATA_A1	OCP# / GPIO40	I	PCH	12	OBSDATA_C1	GPIO35	I	PCH
13	GND	GND	NA		14	GND	GND	NA	
15	OBSDATA_A2	OCP# / GPIO41	I	PCH	16	OBSDATA_C2	SATA2GP / GPIO21	I	PCH
17	OBSDATA_A3	OCP# / GPIO42	I	PCH	18	OBSDATA_C3	SATA1GP / GPIO19	I	PCH
19	GND	GND	NA		20	GND	GND	NA	
21	OBSFN_B0	Open	NA		22	OBSFN_D0	Open	NA	
23	OBSFN_B1	Open	NA		24	OBSFN_D1	Open	NA	
25	GND	GND	NA		26	GND	GND	NA	
27	OBSDATA_B0	OCP# / GPIO43	I	PCH	28	OBSDATA_D0	SATA3GP / GPIO36	I	PCH
29	OBSDATA_B1	TCK# / GPIO9	I	PCH	30	OBSDATA_D1	SATA3GP / GPIO37	I	PCH
31	GND	GND	NA		32	GND	GND	NA	
33	OBSDATA_B2	OCP# / GPIO33	I	PCH	34	OBSDATA_D2	SATA5GP / GPIO14	I	PCH
35	OBSDATA_B3	OCP# / GPIO14	I	PCH	36	OBSDATA_D3	SATA5GP / GPIO49	I	PCH
37	GND	GND	NA		38	GND	GND	NA	
39	HOOK3	RSHIST#	I	PCH	40	ITPCLKHOOK4	Open	NA	
41	HOOK1	BP_PWRGD_RST#	O	system	42	ITPCLK#/ HOOK5	Open	NA	
43	VCC_OBS_AB	VCCGIO_3	NA		44	VCC_OBS_CD	VCCGIO_3	NA	
45	HOOK2	Open	I		46	HOOK6/ RESET#	RSMRST#	I	PCH
47	HOOK3	Open	NA		48	HOOK7/DBR#	SYS_RESET#	O	PCH
49	GND	GND	NA		50	GND	GND	NA	
51	SDA	SDA	I/O	system	52	TDO	JTAG_TDO	O	PCH
53	SCL	SCL	I/O	system	54	TRSTn	Open	NA	
55	TCK1	Open	NA		56	TDI	JTAG_TDI	O	PCH
57	TCK0	JTAG_TCK	O	PCH	58	TMS	JTAG_TMS	O	PCH
59	GND	GND	NA		60	GND	GND (or XDP_PRESENT# if required)	NA	

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Title: XDP/DMI_LAI

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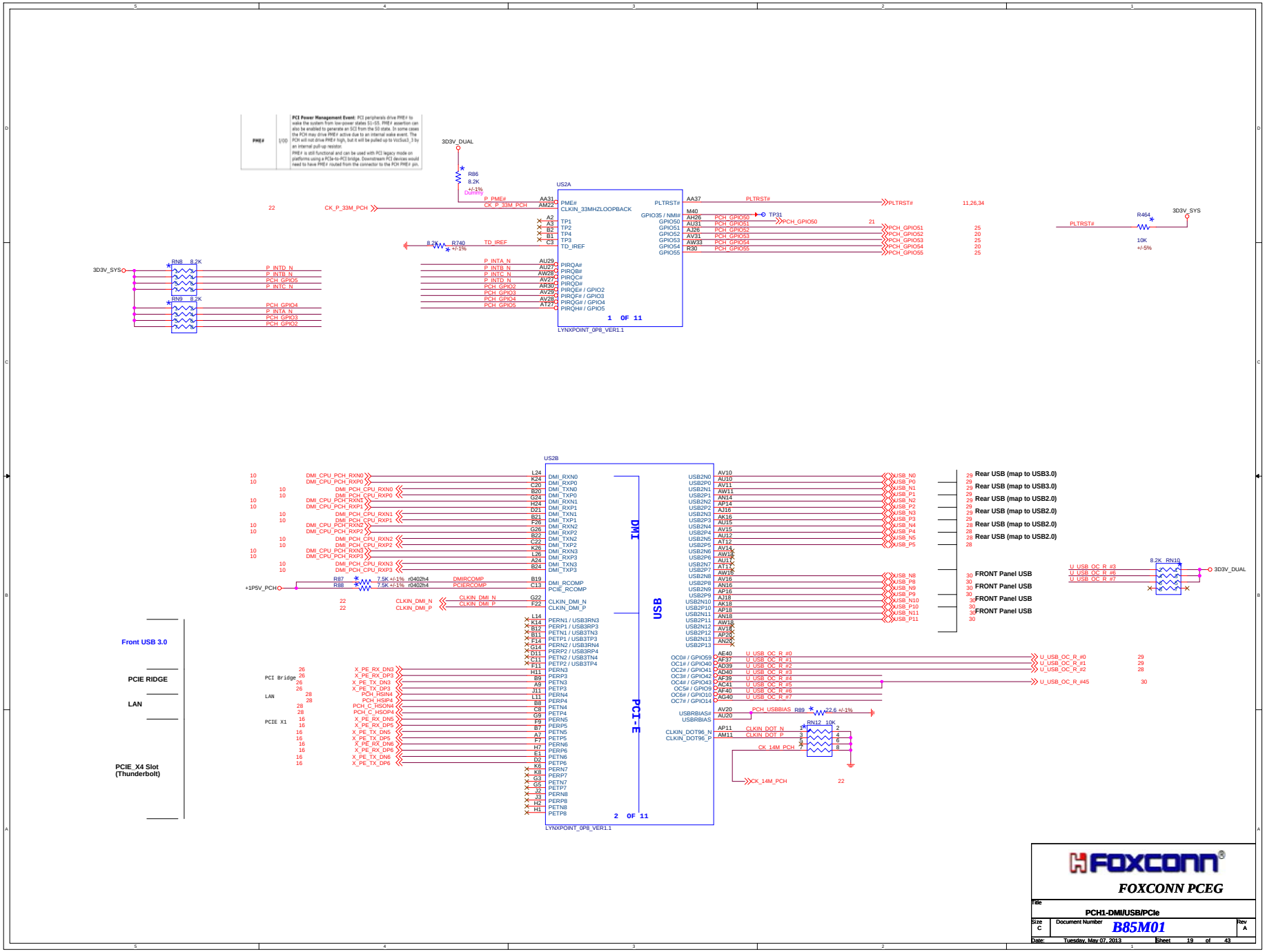
PME#
PCI Power Management Event: PCI peripherals drive PME# to wake the system from low-power states S1-S5. PME# assertion can also be enabled to generate an SCI from the S0 state. In some cases the PCH may drive PME# active due to an internal wake event. The PCH will not drive PME# high, but it will be pulled up to VccSus3_3 by an internal pull-up resistor.
PME# is still functional and can be used with PCI legacy mode on platforms using a PCIe-to-PCI bridge. Downstream PCI devices would need to have PME# routed from the connector to the PCH PME# pin.
3D3V_DUAL
R86
8.2K
+/-1%
Dummy
US2A
P_PME#
CK_P_33M_PCH
CK_P_33M_PCH
CLKIN_33MHZLOOPBACK
TP1
TP2
TP4
TP3
TD_IREF
R740
8.2K
+/-1%
PLTRST#
TP31
GPIO35 / NMI#
GPIO50
GPIO51
GPIO52
GPIO53
GPIO54
GPIO55
PCH_GPIO50
PCH_GPIO51
PCH_GPIO52
PCH_GPIO53
PCH_GPIO54
PCH_GPIO55
R464
10K
+/-5%
3D3V_SYS
RN8
8.2K
P_INTD_N
P_INTB_N
PCH_GPIO5
P_INTC_N
PCH_GPIO4
P_INTA_N
PCH_GPIO3
PCH_GPIO2
P_INTA_N
P_INTB_N
P_INTC_N
P_INTD_N
PCH_GPIO2
PCH_GPIO3
PCH_GPIO4
PCH_GPIO5
PIRQA#
PIRQB#
PIRQC#
PIRQD#
PIRQE# / GPIO2
PIRQF# / GPIO3
PIRQG# / GPIO4
PIRQH# / GPIO5
1 OF 11
LYNXPOINT_0P8_VER1.1
US2B
DMI_RXN0
DMI_RXP0
DMI_TXN0
DMI_TXP0
DMI_RXN1
DMI_RXP1
DMI_TXN1
DMI_TXP1
DMI_RXN2
DMI_RXP2
DMI_TXN2
DMI_TXP2
DMI_RXN3
DMI_RXP3
DMI_TXN3
DMI_TXP3
DMI_RCOMP
PCIE_RCOMP
CLKIN_DMI_N
CLKIN_DMI_P
PERN1 / USB3RN3
PERP1 / USB3RP3
PETN1 / USB3TN3
PETP1 / USB3TP3
PERN2 / USB3RN4
PERP2 / USB3RP4
PETN2 / USB3TN4
PETP2 / USB3TP4
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6
PERP6
PETN6
PETP6
PERN7
PERP7
PETN7
PETP7
PERN8
PERP8
PETN8
PETP8
DMI
USB
PCI-E
2 OF 11
LYNXPOINT_0P8_VER1.1
DMIRCOMP
PCIERCOMP
R87
R88
7.5K +/-1%
r0402h4
+1P5V_PCH
USB2N0
USB2P0
USB2N1
USB2P1
USB2N2
USB2P2
USB2N3
USB2P3
USB2N4
USB2P4
USB2N5
USB2P5
USB2N6
USB2P6
USB2N7
USB2P7
USB2N8
USB2P8
USB2N9
USB2P9
USB2N10
USB2P10
USB2N11
USB2P11
USB2N12
USB2P12
USB2N13
USB2P13
USB_N0
USB_P0
USB_N1
USB_P1
USB_N2
USB_P2
USB_N3
USB_P3
USB_N4
USB_P4
USB_N5
USB_P5
USB_N8
USB_P8
USB_N9
USB_P9
USB_N10
USB_P10
USB_N11
USB_P11
Rear USB (map to USB3.0)
Rear USB (map to USB3.0)
Rear USB (map to USB2.0)
Rear USB (map to USB2.0)
Rear USB (map to USB2.0)
Rear USB (map to USB2.0)
FRONT Panel USB
FRONT Panel USB
FRONT Panel USB
FRONT Panel USB
RN10
8.2K
U_USB_OC_R_#3
U_USB_OC_R_#6
U_USB_OC_R_#7
OC0# / GPIO59
OC1# / GPIO40
OC2# / GPIO41
OC3# / GPIO42
OC4# / GPIO43
OC5# / GPIO9
OC6# / GPIO10
OC7# / GPIO14
U_USB_OC_R_#0
U_USB_OC_R_#1
U_USB_OC_R_#2
U_USB_OC_R_#3
U_USB_OC_R_#4
U_USB_OC_R_#5
U_USB_OC_R_#6
U_USB_OC_R_#7
U_USB_OC_R_#45
USBRBIAS#
USBRBIAS
R89
22.6 +/-1%
RN12
10K
CLKIN_DOT96_N
CLKIN_DOT96_P
CLKIN_DOT_N
CLKIN_DOT_P
CK_14M_PCH
Front USB 3.0
PCIE RIDGE
LAN
PCIE_X4 Slot (Thunderbolt)
PCI Bridge
LAN
PCIE X1
X_PE_RX_DN3
X_PE_RX_DP3
X_PE_TX_DN3
X_PE_TX_DP3
PCH_HSIN4
PCH_HSIP4
PCH_C_HSON4
PCH_C_HSOP4
X_PE_RX_DN5
X_PE_RX_DP5
X_PE_TX_DN5
X_PE_TX_DP5
X_PE_RX_DN6
X_PE_RX_DP6
X_PE_TX_DN6
X_PE_TX_DP6
FOXCONN PCEG
Title
PCH1-DMI/USB/PCIe
Size C
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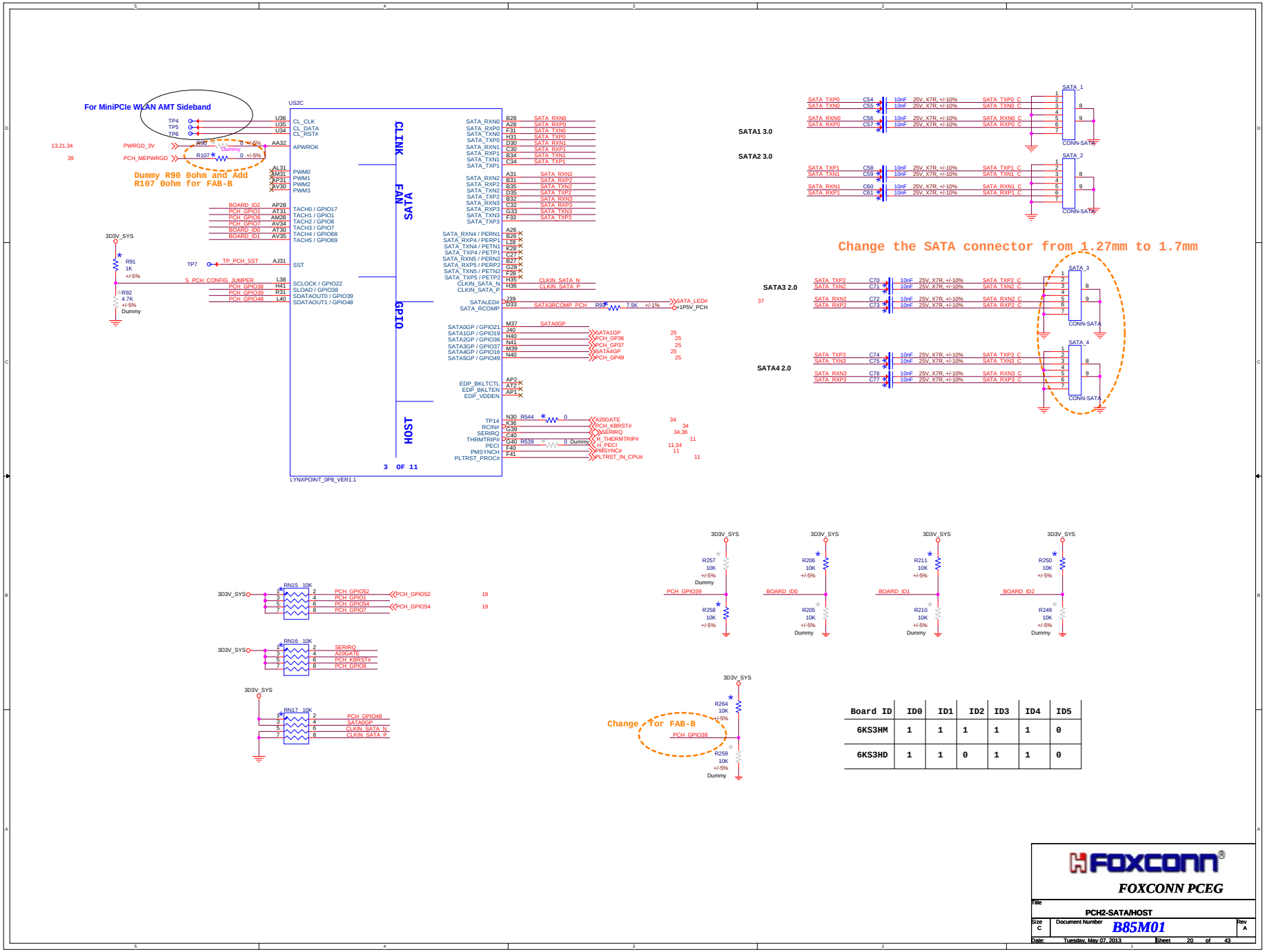
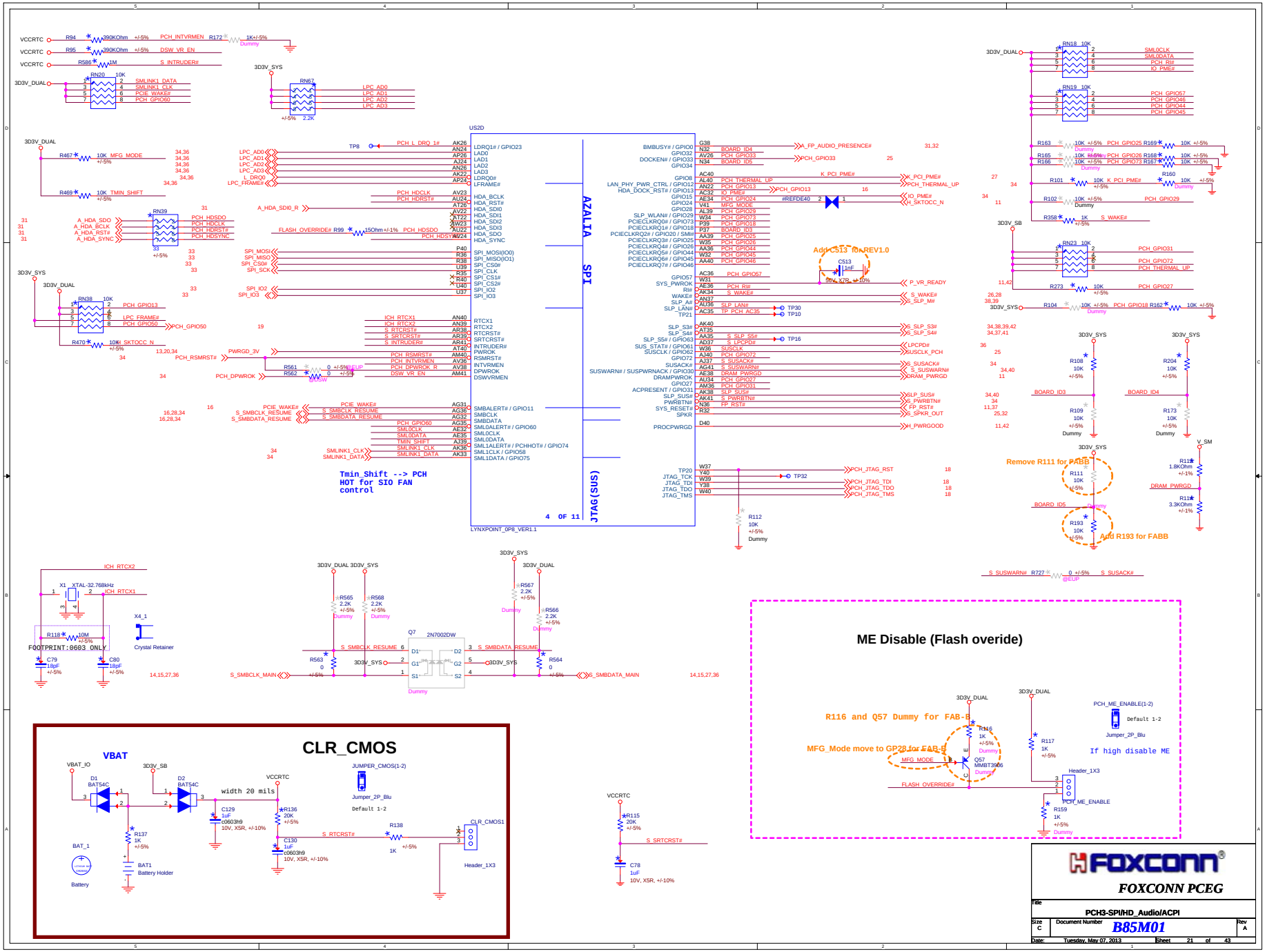


Board ID	ID0	ID1	ID2	ID3	ID4	ID5
6KS3HM	1	1	1	1	1	0
6KS3HD	1	1	0	1	1	0


US2D
AZALIA
SPI
JTAG(SUS)
4 OF 11
LYNXPOINT_0P8_VER1.1
Tmin_Shift --> PCH
HOT for SIO FAN
control
Add C513 for REV1.0
Remove R111 for FABB
Add R193 for FABB
ME Disable (Flash overide)
R116 and Q57 Dummy for FAB-B
MFG_Mode move to GP28 for FAB-B
If high disable ME
CLR_CMOS
VBAT
width 20 mils
FOXCONN PCEG
PCH3-SPI/HD_Audio/ACPI
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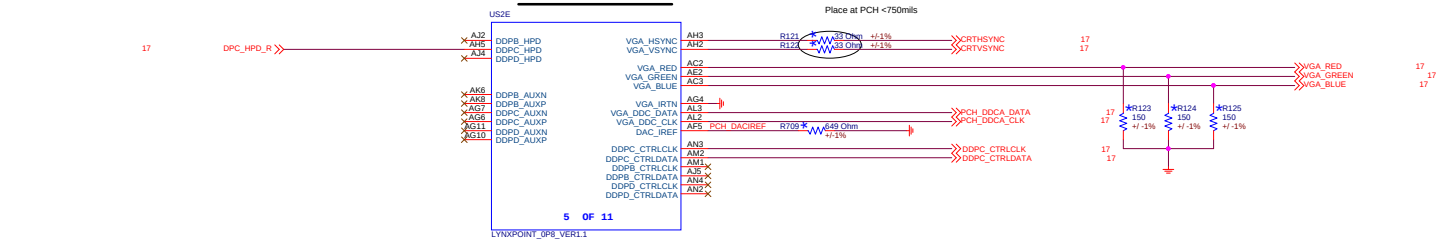
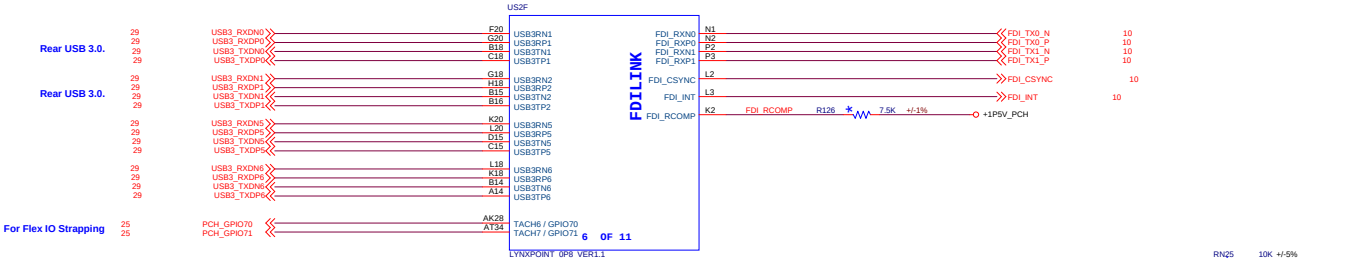
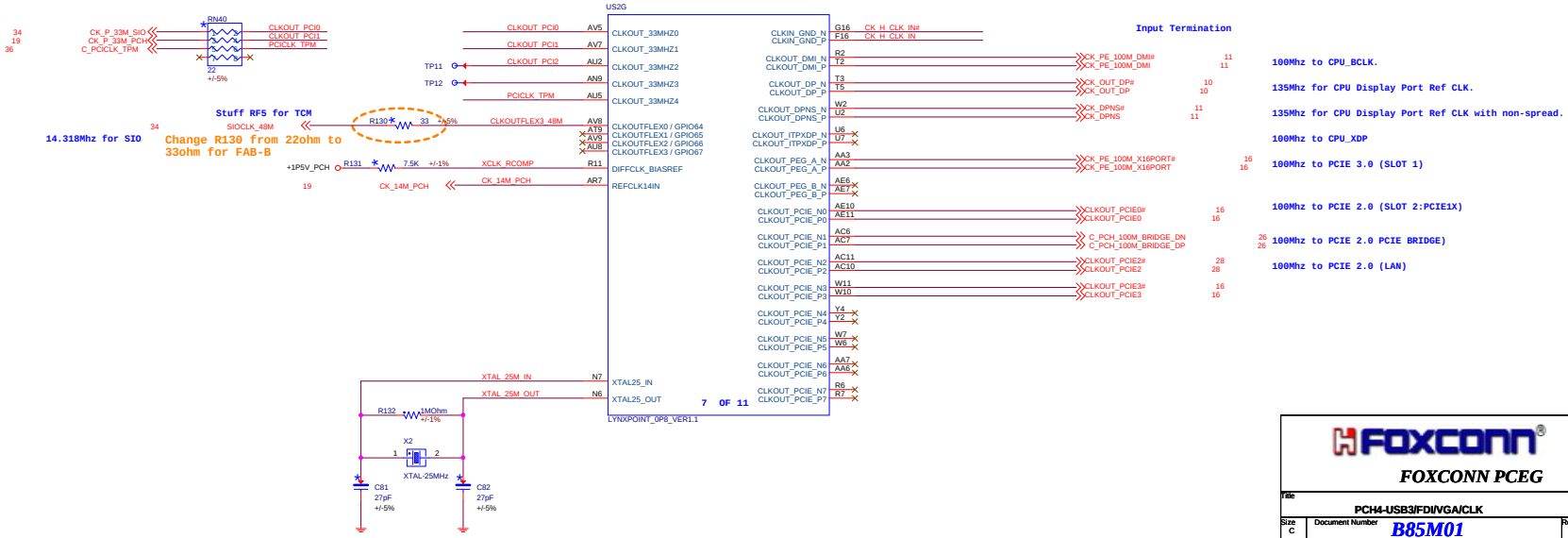
PCH - DP AND RGB





PCH - CLOCK DISTRIBUTION



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Title: PCH4-USB3/FDI/VGA/CLK

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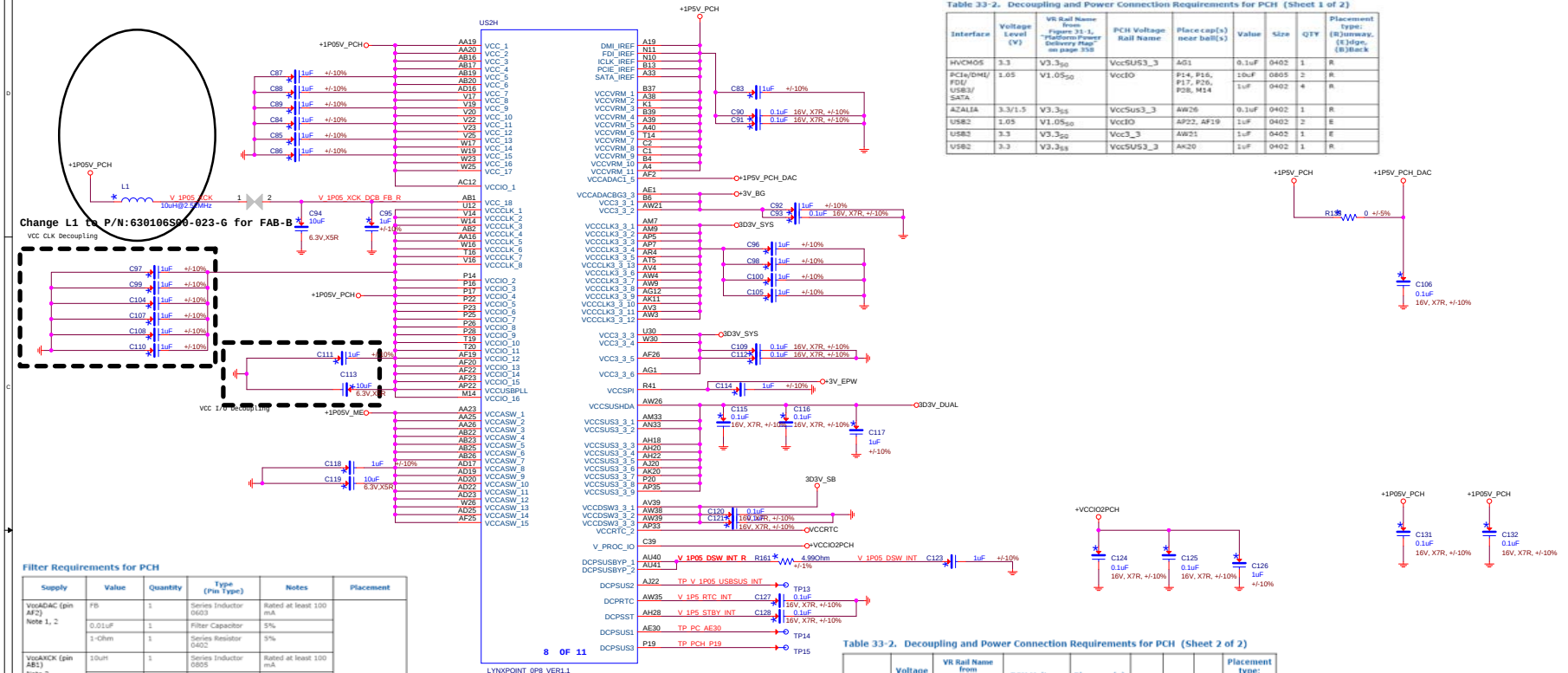

Table 33-2. Decoupling and Power Connection Requirements for PCH (Sheet 1 of 2)

Interface	Voltage Level (V)	VR Rail Name from Figure 31-1, "Platform Power Delivery Map" on page 358	PCH Voltage Rail Name	Place cap(s) near ball(s)	Value	Size	QTY	Placement type: (R)unway, (E)dge, (B)Back
HVCMOS	3.3	$V3.3_{SO}$	VccSUS3_3	AG1	0.1uF	0402	1	R
PCIe/DMI/FDI/USB3/SATA	1.05	$V1.05_{SO}$	VccIO	P14, P16, P17, P26, P28, M14	10uF	0805	2	R
					1uF	0402	4	R
AZALIA	3.3/1.5	$V3.3_{SS}$	VccSus3_3	AW26	0.1uF	0402	1	R
USB2	1.05	$V1.05_{SO}$	VccIO	AP22, AF19	1uF	0402	2	E
USB3	3.3	$V3.3_{SO}$	Vcc3_3	AW21	1uF	0402	1	E
USB2	3.3	$V3.3_{SS}$	VccSUS3_3	AK20	1uF	0402	1	R

Filter Requirements for PCH

Supply	Value	Quantity	Type (Pin Type)	Notes	Placement
VccADAC (pin AF2) Note 1, 2	FB	1	Series Inductor 0603	Rated at least 100 mA	< 100 mils (2.54 mm) from PCH
	0.01uF	1	Filter Capacitor	5%	
	1-Ohm	1	Series Resistor 0402	5%	
VccAXCK (pin AB1) Note 2	10uH	1	Series Inductor 0805	Rated at least 100 mA	
	10uF	1	Filter Capacitor	5%	
	0-Ohm	1	Series Resistor 0402	5%	
VccACLK (pin T14) Note 3	10uH	1	Series Inductor 0805	Rated at least 100 mA	
	10uF	1	Filter Capacitor	5%	
	1-Ohm	1	Series Resistor 0402	5%	
VccAFDIPLL (pin K1) Note 3	1uH	1	Series Inductor 1210	Rated at least 100 mA	
	10uF	1	Filter Capacitor	5%	
VccADMIPLL (pin B37) Note 3	1uH	1	Series Inductor 0805	Rated at least 100 mA	
	10uF	1	Filter Capacitor	5%	
VccAUSBPLL (pin C2) Note 3	1uH	1	Series Inductor 0805	Rated at least 100 mA	
	10uF	1	Filter Capacitor	5%	
VccASATAPLL (pin B39) Note 3	10uH	1	Series Inductor 0805	Rated at least 100 mA	
	10uF	1	Filter Capacitor	5%	

Table 33-2. Decoupling and Power Connection Requirements for PCH (Sheet 2 of 2)

Interface	Voltage Level (V)	VR Rail Name from Figure 31-1, "Platform Power Delivery Map" on page 358	PCH Voltage Rail Name	Place cap(s) near ball(s)	Value	Size	QTY	Placement type: (R)unway, (E)dge, (B)Back
GPIO/LPC/USB3	3.3	$V3.3_{SS}$	VccSUS3_3	AN33	0.1uF	0402	1	R
GPIO/LPC	3.3	$V3.3_{DSW}$	VccDSW3_3	AW39	0.1uF	0402	1	E
GPIO/LPC	-	PCH Internal VRM	DcpSST	AH28	0.1uF	0402	1	E
GPIO/LPC	3.3	$V3.3_{SO}$	VccCore3_3	W30	0.1uF	0402	1	R
GPIO/LPC	1.05	$V1.05_{DSW}$	DcpSusByP	AU40	1uF	0402	1	R
					5ohm	0402	1	Series
RTC	coin bat	V3.3RTC	VccRTC	AP33	1uF	0402	1	R
					0.1uF	0402	1	E
RTC		PCH Internal VRM	DcpRTC	AW35	0.1uF	0402	1	R
RTC	3.3	$V3.3_{SS}$	VccRTC	AP35	1uF	0402	1	R
CPU	1.0/1.05	VCCIO	Vcc_PROC_1p0	C39	1uF	0603	1	E
					0.1uF	0402	2	E
SPI	3.3	$V3.3_{SPIEPW}$	VccSPI	R41	1uF	0402	1	R
Fuse	3.3	$V3.3_{SO}$	Vcc3_3	AF26	1uF	0402	1	E
CORE	1.05	$VCCIO\_ME_{H}$	VccASW	AD17, AD19	1uF	0402	1	E
					10uF	0805	1	E
Clock integration	3.3	$V3.3_{SO}$	VccCLK3_3	AV4, AR4, AT5, AP5	1uF	0402	4	R
	1.05	$V1.05_{SO}$	VccCLK	U12, W14, AB2, AA16, V16, W16	1uF	0402	6	R
Thermal	3.3	$V3.3_{SO}$	Vcc3_3	B6	0.1uF	0402	1	E
Core (Note 1)	-	PCH External VRM	DcpSus	AE30, P19, AJ22	1uF	0402	3	E

PCH HEATSINK

FOXCONN PCEG

Title: PCH5-PWR

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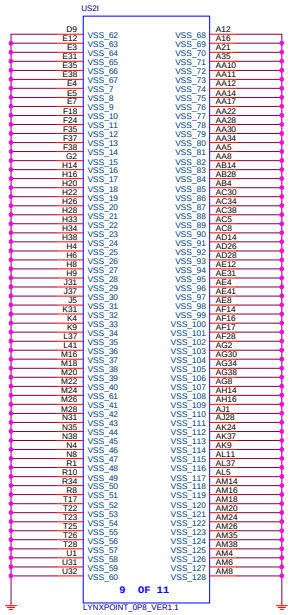

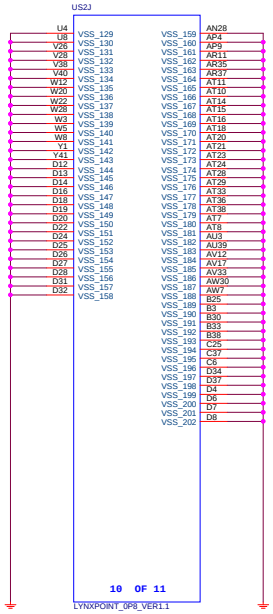

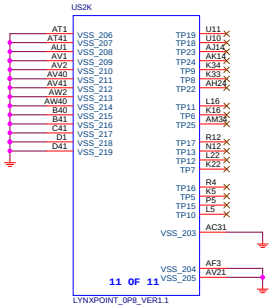

FOXCONN PCEG

Title: PCH6-GND

Size	Document Number	Rev
C	B85M01	A

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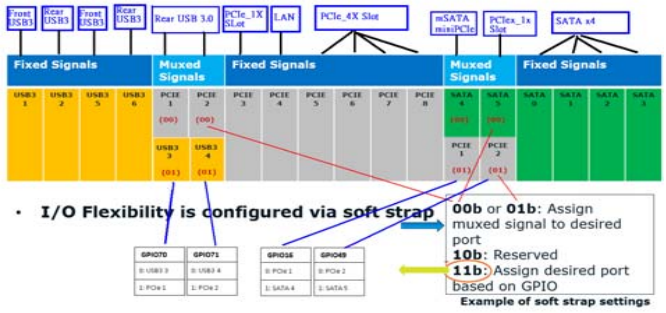
Lynx Point I/O Flexibility

- New architecture allows some I/O Ports to be configured at time of system design

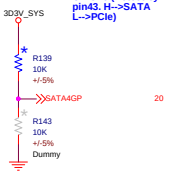


- I/O Flexibility is configured via soft strap

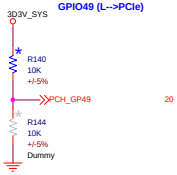
00b or **01b**: Assign muxed signal to desired port
10b: Reserved
11b: Assign desired port based on GPIO

Example of soft strap settings

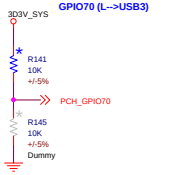
GPIO16 (Detect by pin43. H-->SATA L-->PCIe)



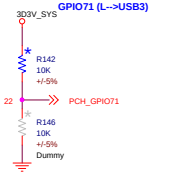
GPIO49 (L-->PCIe)

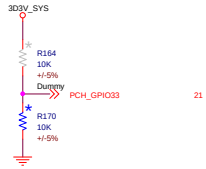


GPIO70 (L-->USB3)



GPIO71 (L-->USB3)



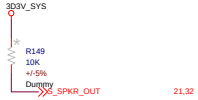


DMI AC COUPLING FULL VOLTAGE MODE WHEN SAMPLED LOW

No Reboot Mode

SPKR (IN-PD)	Description
High	No reboot mode: Enable
Low	No reboot mode: Disable

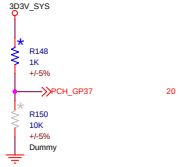
DEFAULT



TLS Confidentiality

GPIO37 (IN-PD)	Description
High	ME Crypto TLS cipher suite with confidentiality
Low	ME Crypto TLS cipher suite with no confidentiality

DEFAULT



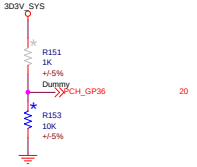
Topblock Swap Mode

GPIO55 (IN-PU)	Description
High	Topblock swap mode: Disable
Low	Topblock swap mode: Enable

DEFAULT

DMI Rx Termination

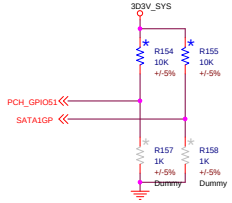
GPIO36 (IN-PD)	Description
Low	DMI Rx Termination Voltage



Boot BIOS Destination Selection

GPIO51 (IN-PU)	SATA1GP/GP19 (IN-PU)	Description
Low	Low	Flash cycle routed to LPC
High	Low	Flash cycle routed to PCI
High	High	Flash cycle routed to SPI

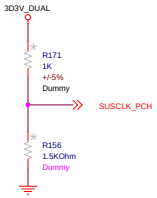
19
20
DEFAULT



On-Die PLL Voltage Regulator

GPIO62/SUSCLK (IN-PU)	Description
High	Regulator is enabled.
Low	Regulator is disabled.

DEFAULT



21

FOXCONN PCEG

Title: PCH7-Strapping Option

Size	Document Number	Rev
C	B85M01	A

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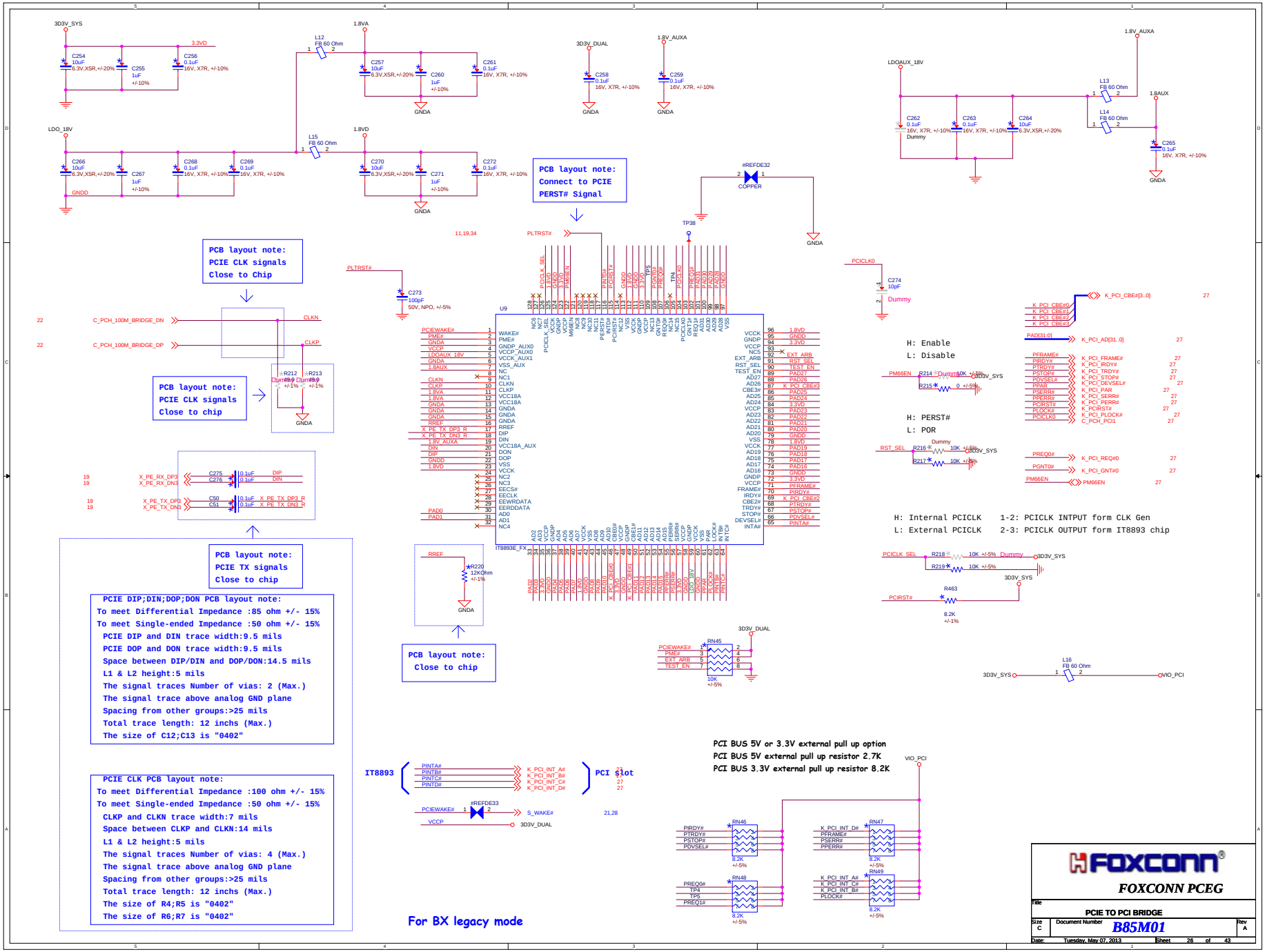
PCB layout note:
PCIE CLK signals
Close to Chip
PCB layout note:
PCIE CLK signals
Close to chip
PCB layout note:
PCIE TX signals
Close to chip
PCB layout note:
Connect to PCIE
PERST# Signal
PCB layout note:
Close to chip
PCIE DIP;DIN;DOP;DON PCB layout note:
To meet Differential Impedance :85 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
PCIE DIP and DIN trace width:9.5 mils
PCIE DOP and DON trace width:9.5 mils
Space between DIP/DIN and DOP/DON:14.5 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 2 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inches (Max.)
The size of C12;C13 is "0402"
PCIE CLK PCB layout note:
To meet Differential Impedance :100 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
CLKP and CLKN trace width:7 mils
Space between CLKP and CLKN:14 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 4 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inches (Max.)
The size of R4;R5 is "0402"
The size of R6;R7 is "0402"
For BX legacy mode
H: Enable
L: Disable
H: PERST#
L: POR
H: Internal PCICLK 1-2: PCICLK INTPUT form CLK Gen
L: External PCICLK 2-3: PCICLK OUTPUT form IT8893 chip
PCI BUS 5V or 3.3V external pull up option
PCI BUS 5V external pull up resistor 2.7K
PCI BUS 3.3V external pull up resistor 8.2K
IT8893
PCI Slot
FOXCONN PCEG
PCIE TO PCI BRIDGE
B85M01
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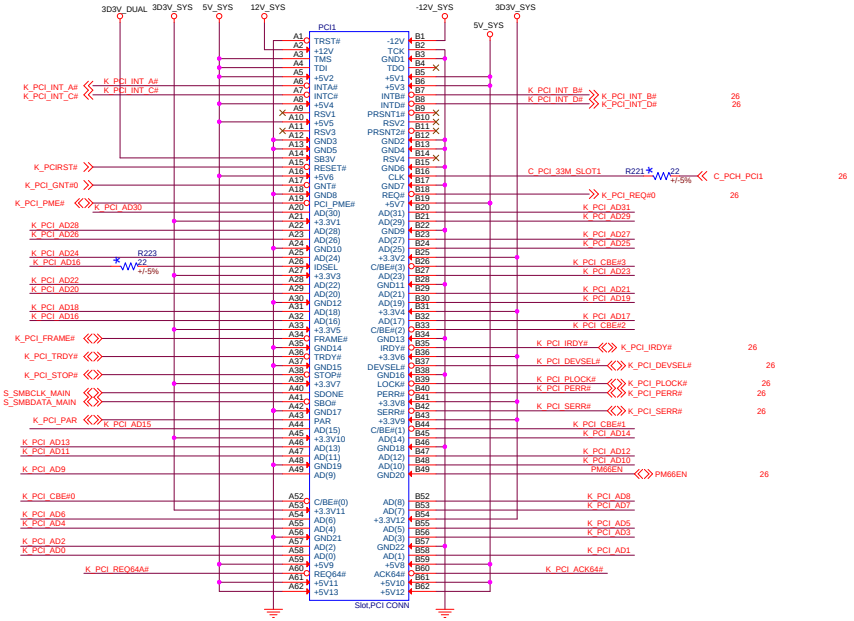
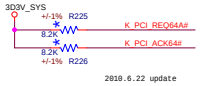
PCI 1



IRQ: A B C D
IDSEL: AD16
REQ/GNT: 0

PCI BUS if use 5V external pull up resistor is 2.7K

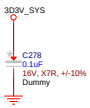


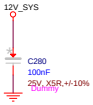
2010.6.22 update

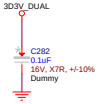
K_PCI_AD[31..0]

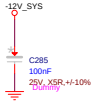
K_PCI_CBE[3..0]

K_PCI_CBE#0
K_PCI_CBE#1
K_PCI_CBE#2
K_PCI_CBE#3









FOXCONN PCEG

Title: PCI SLOT X2

Size	Document Number	Rev
C	B85M01	A

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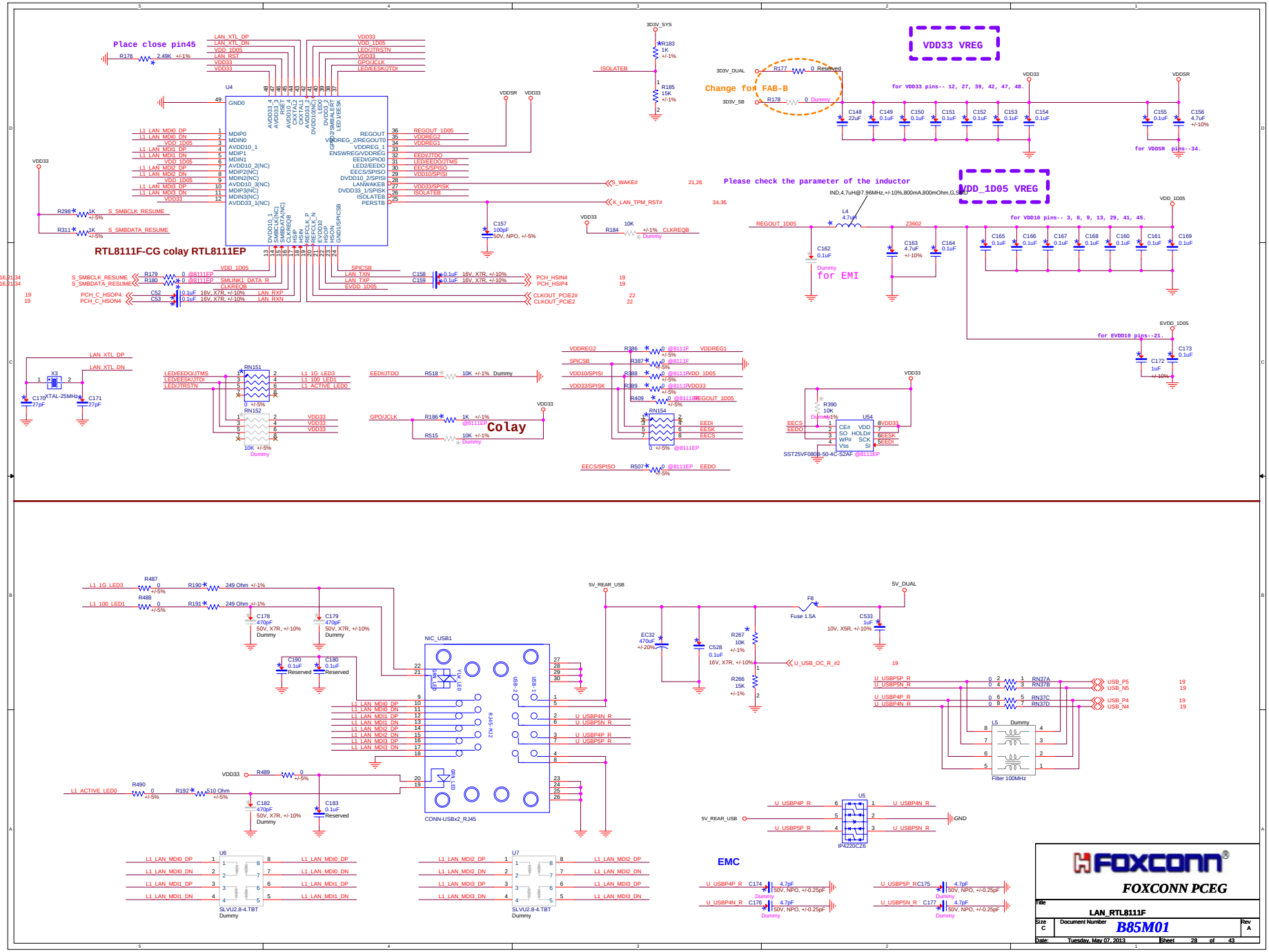
Place close pin45
RTL8111F-CG colay RTL8111EP
VDD33 VREG
Change for FAB-B
Please check the parameter of the inductor
VDD_1D05 VREG
for EMI
Colay
EMC
FOXCONN PCEG
LAN_RTL8111F
B85M01
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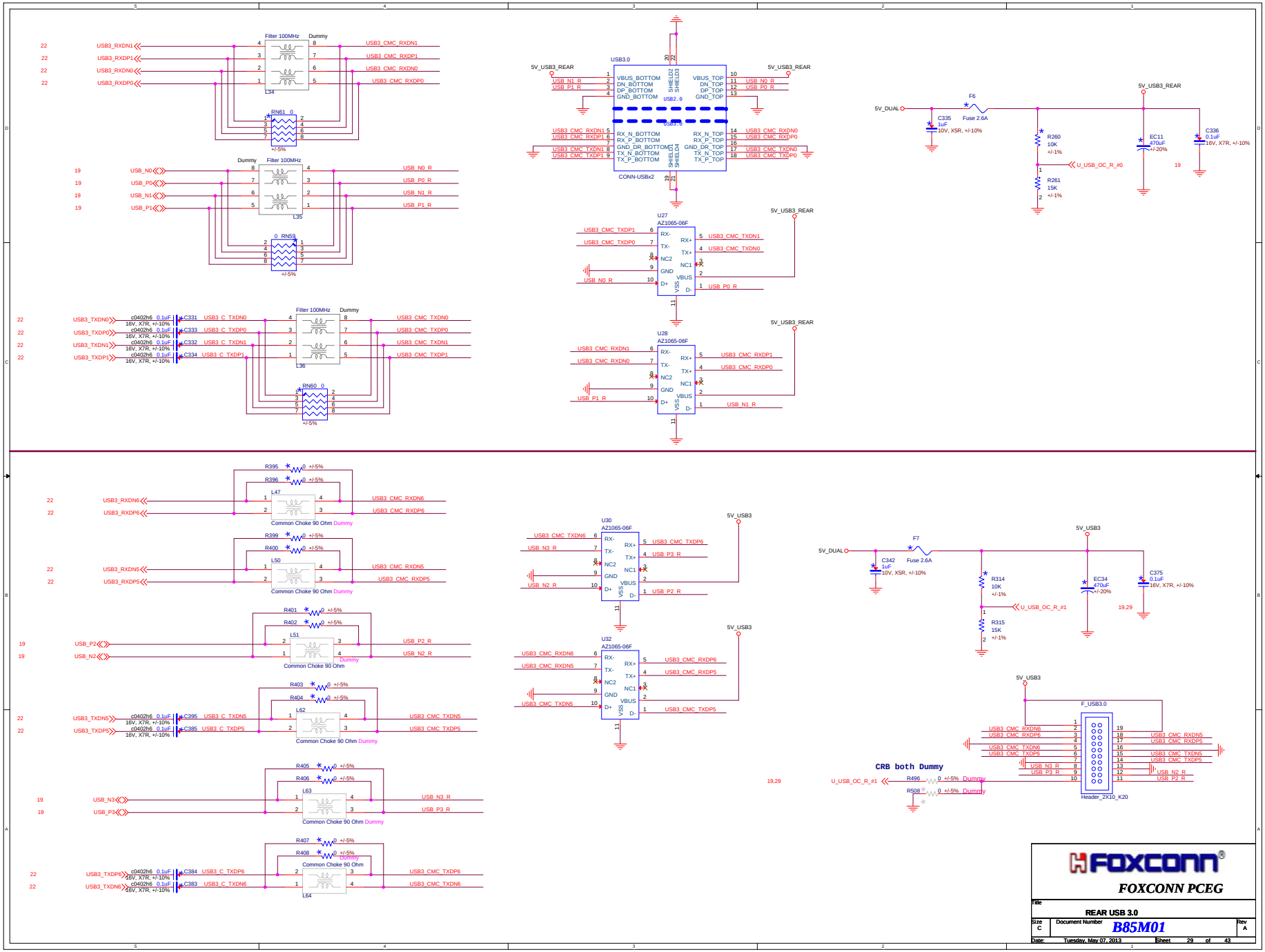
USB3_RXDN1
USB3_RXDP1
USB3_RXDN0
USB3_RXDP0
Filter 100MHz
Dummy
USB3_CMC_RXDN1
USB3_CMC_RXDP1
USB3_CMC_RXDN0
USB3_CMC_RXDP0
L34
RN61 0
+/-5%
USB_N0
USB_P0
USB_N1
USB_P1
USB_N0_R
USB_P0_R
USB_N1_R
USB_P1_R
L35
0 RN59
USB3_TXDN0
USB3_TXDP0
USB3_TXDN1
USB3_TXDP1
c0402h6 0.1uF
16V, X7R, +/-10%
C331 USB3_C_TXDN0
C333 USB3_C_TXDP0
C332 USB3_C_TXDN1
C334 USB3_C_TXDP1
USB3_CMC_TXDN0
USB3_CMC_TXDP0
USB3_CMC_TXDN1
USB3_CMC_TXDP1
L36
RN60 0
USB3.0
5V_USB3_REAR
VBUS_BOTTOM
DN_BOTTOM
DP_BOTTOM
GND_BOTTOM
SSRX1_N_BOTTOM
SSRX1_P_BOTTOM
GND_DR_BOTTOM
SSTX1_N_BOTTOM
SSTX1_P_BOTTOM
USB2.0
SSTX1
SSRX1
VBUS_TOP
DN_TOP
DP_TOP
GND_TOP
SSRX2_N_TOP
SSRX2_P_TOP
GND_DR_TOP
SSTX2_N_TOP
SSTX2_P_TOP
SHIELD1
SHIELD2
SHIELD3
SHIELD4
CONN-USBx2
U27
AZ1065-06F
RX-
TX-
NC2
GND
D+
RX+
TX+
NC1
VBUS
D-
VSS
U28
F6
Fuse 2.6A
5V_DUAL
C335
1uF
10V, X5R, +/-10%
R260
10K
+/-1%
R261
15K
+/-1%
U_USB_OC_R_#0
EC11
470uF
+/-20%
C336
0.1uF
16V, X7R, +/-10%
R395
R396
L47
Common Choke 90 Ohm Dummy
R399
R400
L50
R401
R402
L51
R403
R404
L62
R405
R406
L63
R407
R408
L64
U30
U32
5V_USB3
F7
C342
R314
10K
R315
15K
EC24
C375
F_USB3.0
Header_2X10_K20
CRB both Dummy
R496
R508
U_USB_OC_R_#1
FOXCONN PCEG
REAR USB 3.0
B85M01
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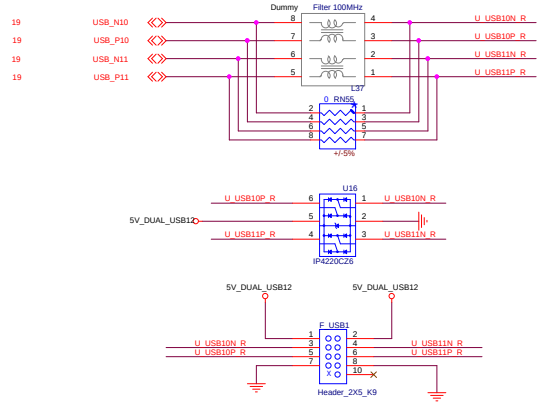
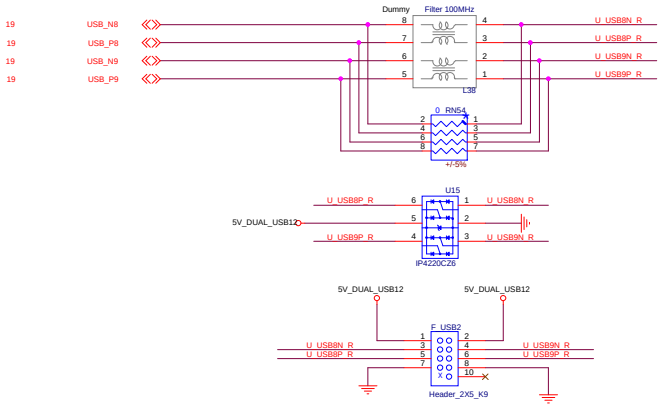
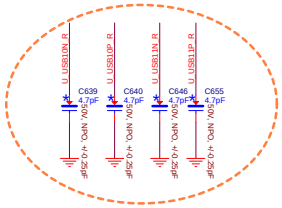
Front_USB1



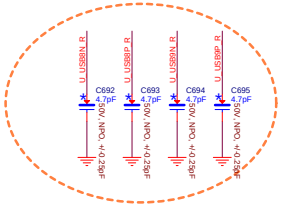
Front_USB2

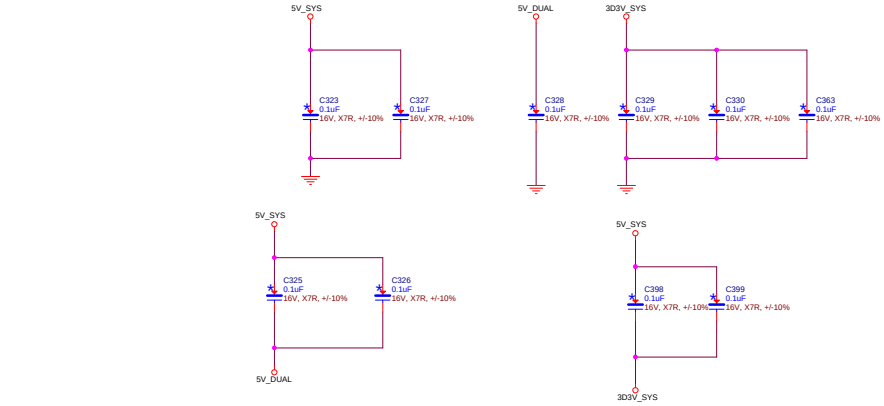


From Dummy to Reserved with EMC require for FAB-B



From Dummy to Reserved with EMC require for FAB-B





FOXCONN PCEG

Title: FRONT USB2.0 Header

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C	B85M01	A

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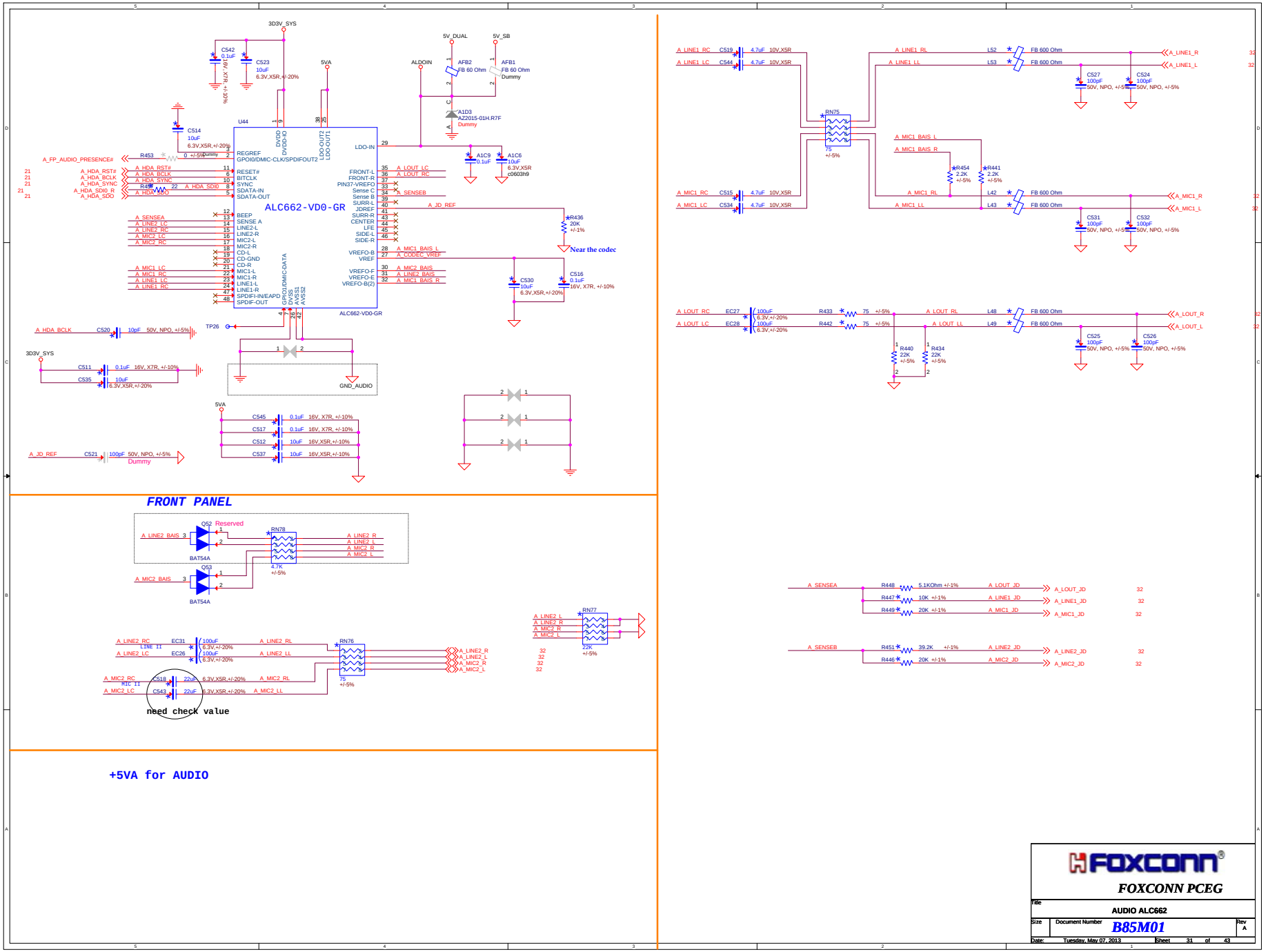
ALC662-VD0-GR
Near the codec
FRONT PANEL
need check value
+5VA for AUDIO
FOXCONN PCEG
AUDIO ALC662
B85M01
Tuesday, May 07, 2013
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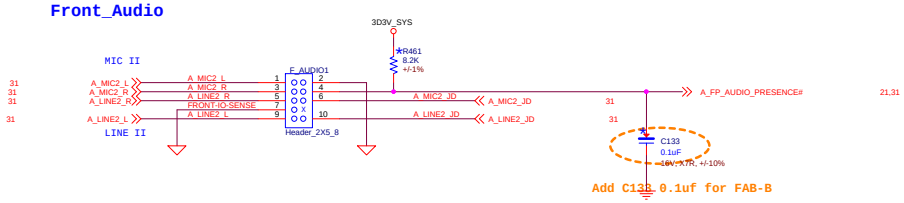
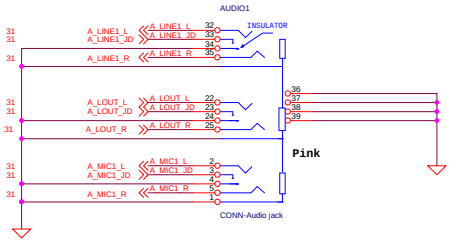
Front_Audio



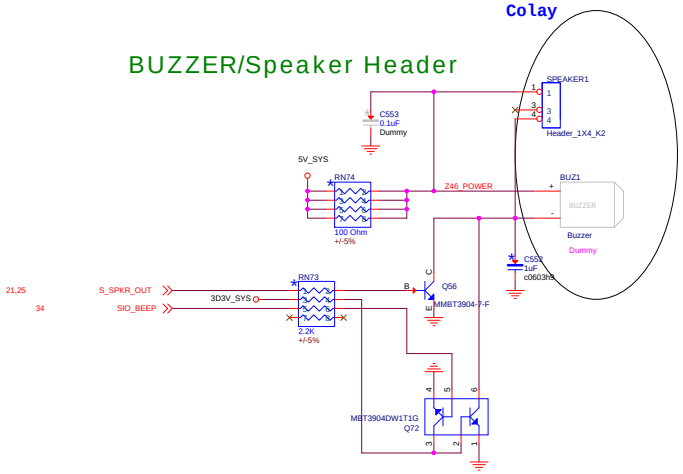
Add C133 0.1uf for FAB-B

Audio Jack



Colay

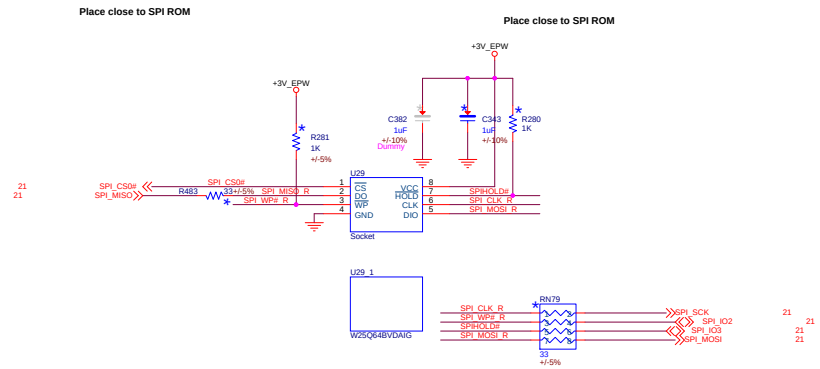
BUZZER/Speaker Header



FOXCONN PCEG

Title: AUDIO CONN/HEADER		
Size: C	Document Number: B85M01	Rev: A
Date: Tuesday, May 07, 2013	Sheet 32 of 43	

SPI SOCKET Primary



Support Quad Read I/O Rom parts. (Beaware of 2nd source need to be support Quad I/O read)

SPI ROMs (move to BOM DIP for factory process)

3. PIN CONFIGURATION SOIC 150 / 208-MIL

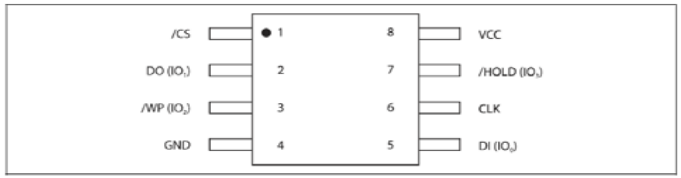


Figure 1a. W25Q16CV Pin Assignments, 8-pin SOIC 150 / 208-mil (Package Code SN & SS)

PIN DESCRIPTION SOIC 150/208-MIL, PDIP 300-MIL AND WSON 6X5-MM

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)*1
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)*2
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)*1
6	CLK	I	Serial Clock Input
7	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)*2
8	VCC		Power Supply

*1 IO0 and IO1 are used for Standard and Dual SPI instructions

*2 IO0 – IO3 are used for Quad SPI instructions

FOXCONN PCEG

Title: SPI_Socket_ROM

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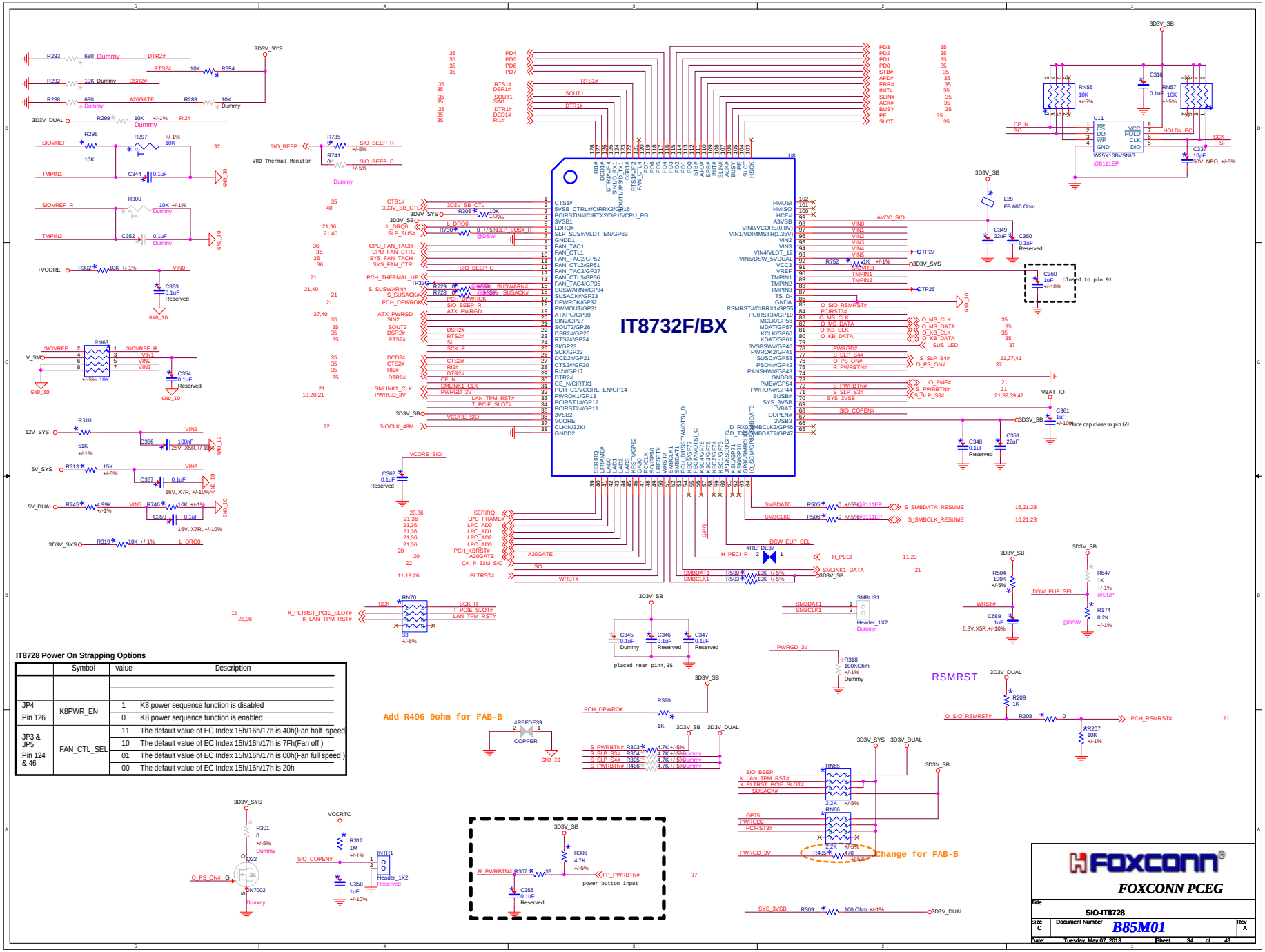

IT8728 Power On Strapping Options

	Symbol	value	Description
JP4 Pin 126	K8PWR_EN	1	K8 power sequence function is disabled
		0	K8 power sequence function is enabled
JP3 & JP5 Pin 124 & 46	FAN_CTL_SEL	11	The default value of EC Index 15h/16h/17h is 40h(Fan half speed)
		10	The default value of EC Index 15h/16h/17h is 7Fh(Fan off)
		01	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
		00	The default value of EC Index 15h/16h/17h is 20h

FOXCONN PCEG

Title: SIO-IT8728

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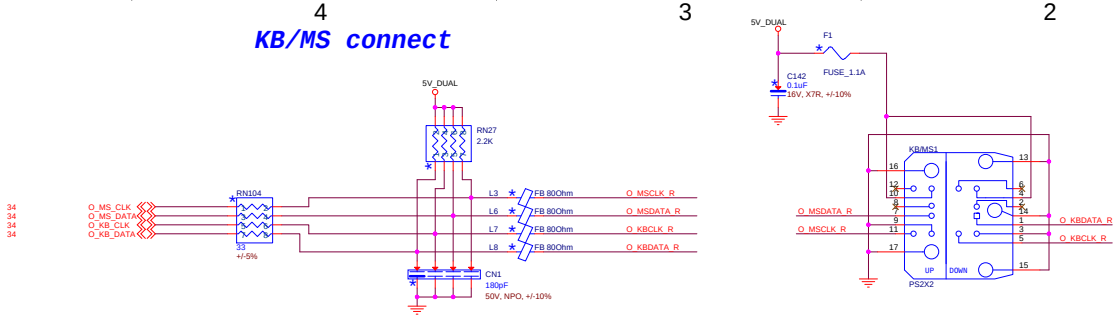
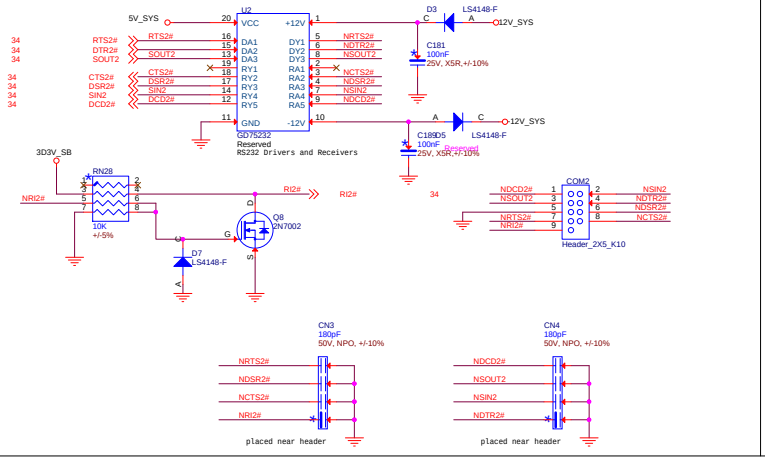
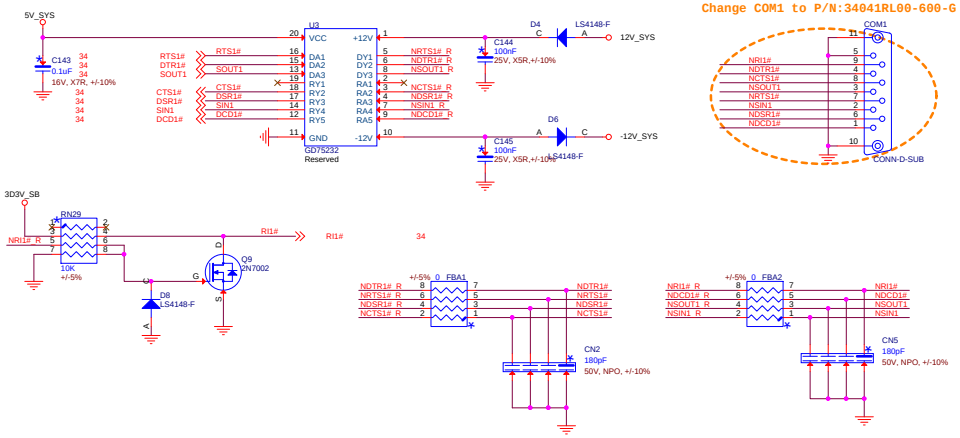
KB/MS connect



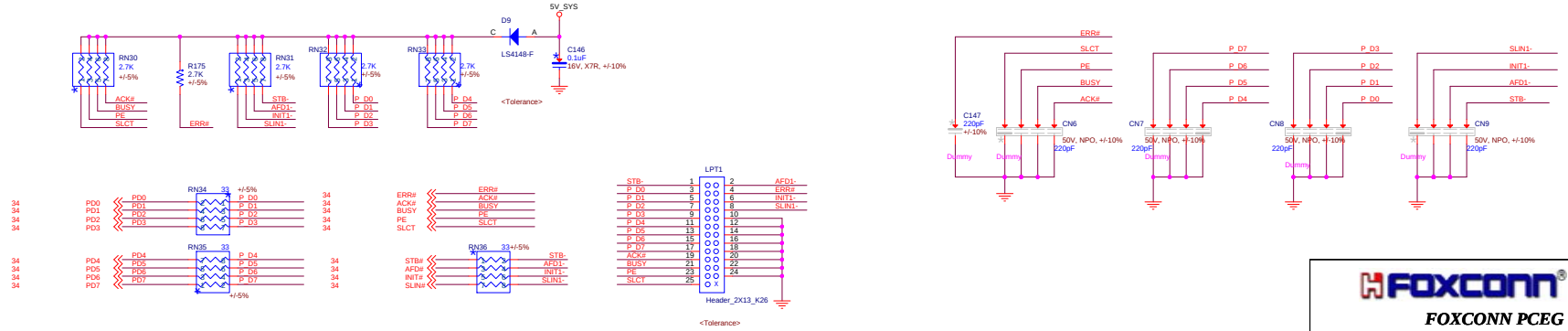
COM HEADER



COM PORT



LPT PORT



FOXCONN PCEG

Title: PS2/COM/LPT

Size: C | Document Number: B85M01 | Rev: A

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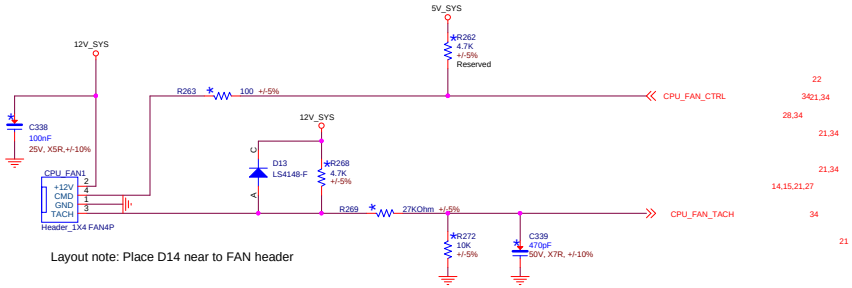
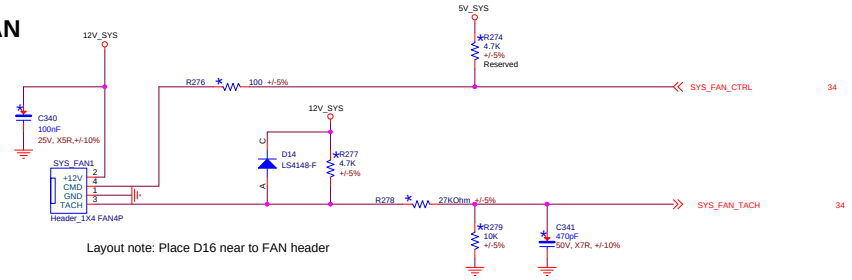
CPU FAN



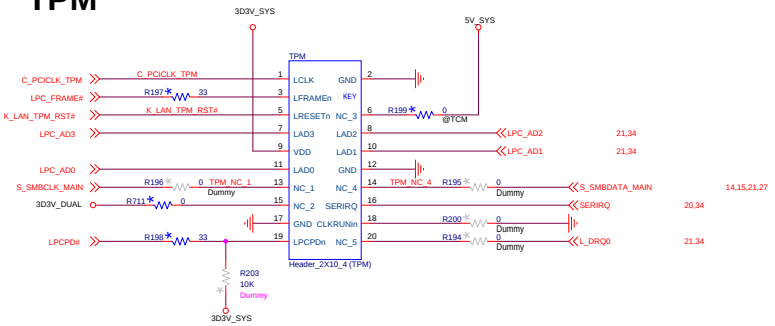
Layout note: Place D14 near to FAN header

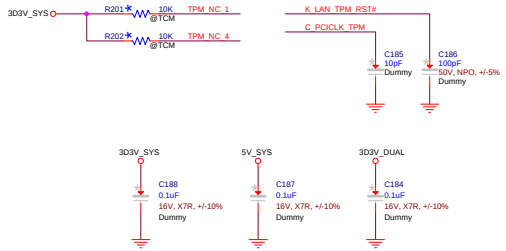
SYS FAN



Layout note: Place D16 near to FAN header

TPM





FOXCONN PCEG

Title: FAN Connector

Size	Document Number	Rev
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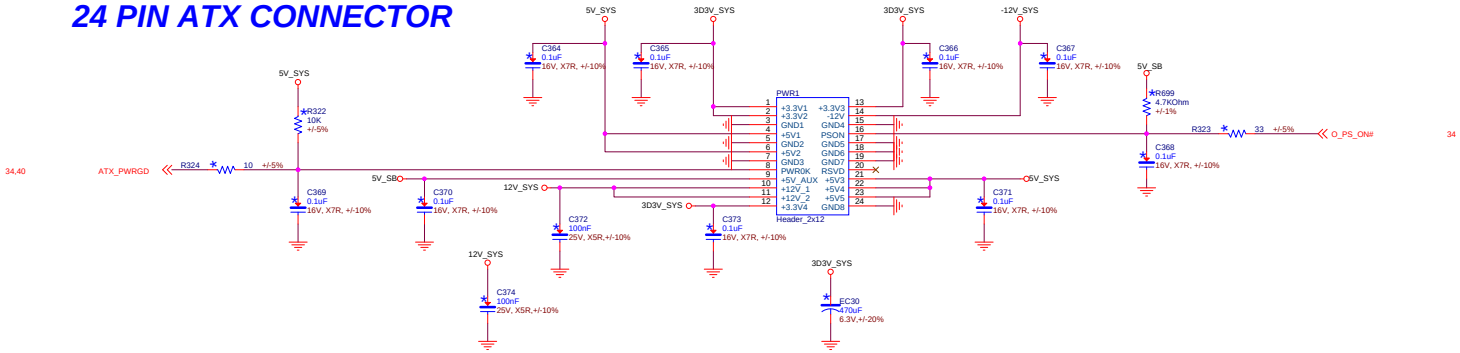
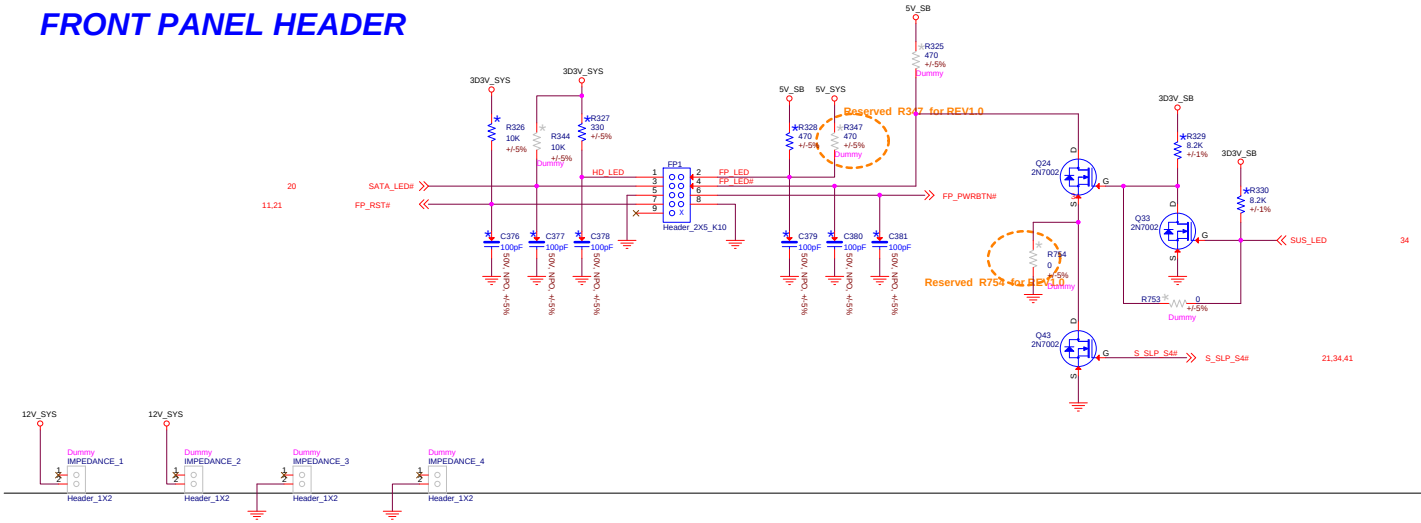
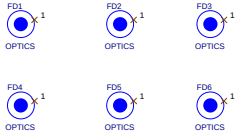
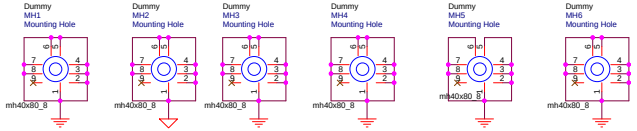
24 PIN ATX CONNECTOR



FRONT PANEL HEADER







FOXCONN

FOXCONN PCEG

Title: ATX CONN/FP PANEL

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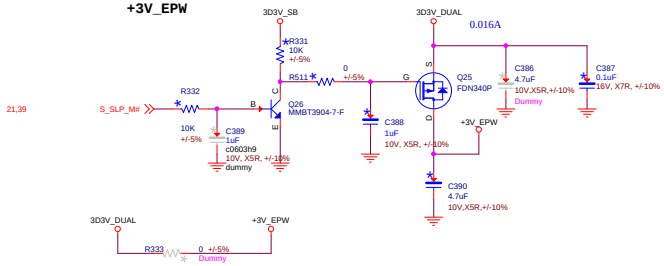
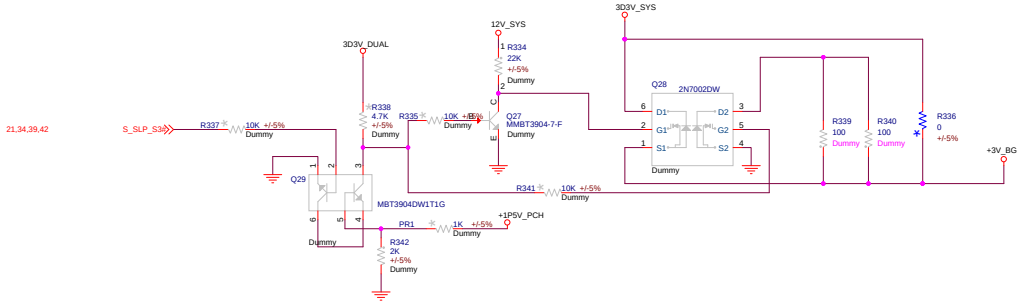
+3V_EPW



+3V_BG



FOXCONN PCEG

Title: Linear Power

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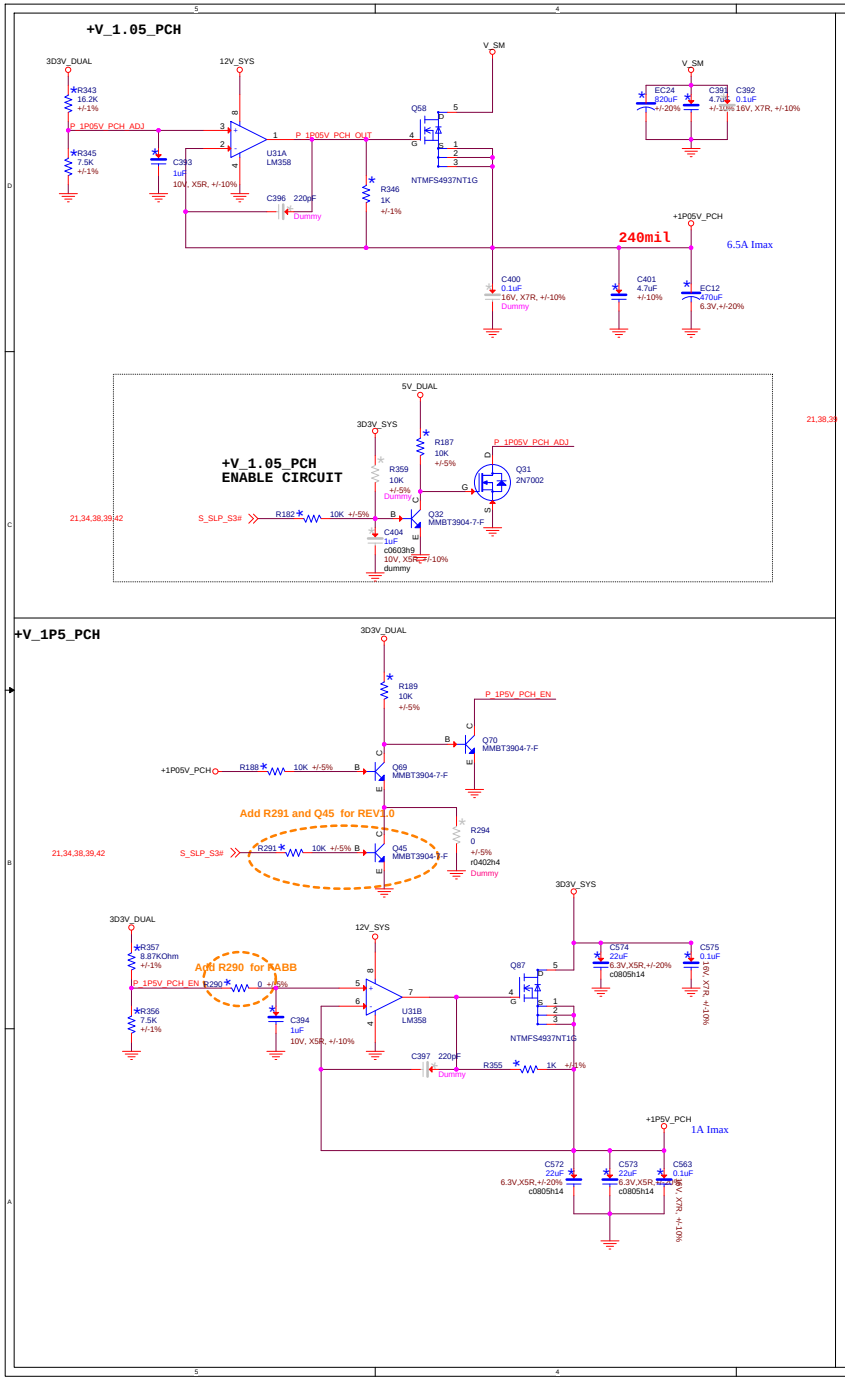
+V_1.05_PCH
3D3V_DUAL
12V_SYS
V_SM
R343 16.2K +/-1%
R345 7.5K +/-1%
P_1P05V_PCH_ADJ
C393 1uF 10V, X5R, +/-10%
U31A LM358
P_1P05V_PCH_OUT
C396 220pF Dummy
R346 1K +/-1%
Q58
NTMFS4937NT1G
EC24 220uF +/-20%
C391 4.7uF +/-10%
C392 0.1uF 16V, X7R, +/-10%
+1P05V_PCH
240mil
6.5A Imax
C400 0.1uF 16V, X7R, +/-10% Dummy
C401 4.7uF +/-10%
EC12 470uF 6.3V,+/-20%
+V_1.05_PCH ENABLE CIRCUIT
5V_DUAL
3D3V_SYS
R187 10K +/-5%
R359 10K +/-5% Dummy
P_1P05V_PCH_ADJ
Q31 2N7002
21,34,38,39,42
S_SLP_S3#
R182 10K +/-5%
Q32 MMBT3904-7-F
C404 1uF c0603h9 10V, X5R, +/-10% dummy
21,38,39
+V_1P5_PCH
3D3V_DUAL
R189 10K +/-5%
P_1P5V_PCH_EN
Q70 MMBT3904-7-F
+1P05V_PCH
R188 10K +/-5%
Q69 MMBT3904-7-F
Add R291 and Q45 for REV1.0
R294 0 +/-5% r0402h4 Dummy
21,34,38,39,42
S_SLP_S3#
R291 10K +/-5%
Q45 MMBT3904-7-F
3D3V_SYS
12V_SYS
3D3V_DUAL
R357 8.87KOhm +/-1%
P_1P5V_PCH_EN
R290 0 +/-5%
Add R290 for RABB
R356 7.5K +/-1%
C394 1uF 10V, X5R, +/-10%
U31B LM358
Q87
NTMFS4937NT1G
C574 22uF 6.3V,X5R,+/-20% c0805h14
C575 0.1uF 16V, X7R, +/-10%
C397 220pF Dummy
R355 1K +/-1%
+1P5V_PCH
1A Imax
C572 22uF 6.3V,X5R,+/-20% c0805h14
C573 22uF 6.3V,X5R,+/-20% c0805h14
C563 0.1uF 16V, X7R, +/-10%
3D3V_DUAL
R821 5.6K +/-1%
PCH_MEPWRGD
20,39
+1P05V_ME
R497 30.1KOhm +/-1%
C565 0.1uF 16V, X7R, +/-10%
R820 33K +/-5%
Q34
MBT3904DW1T1G
R498 301KOhm +/-1%
C564 0.47uF 10V, X5R, +/-10%
C788 100pF 50V, NPO, +/-5%
PCH_MEPWRGD
20,39
3D3V_DUAL
5V_ME
S_SLP_M#
RN21 10K
1D05_ME_EN
Q49
MBT3904DW1T1G
C696 0.1uF Dummy 16V, X7R, +/-10%
R751 0 +/-5%
3D3V_DUAL
R828 10K +/-5% Dummy
1D05_ME_EN
Q86 MMBT3904-7-F
C698 0.1uF Dummy 16V, X7R, +/-10%
21,38,39
S_SLP_M#
R825 10K +/-5% Dummy
Q83 MMBT3904-7-F Dummy
C697 0.1uF Dummy 16V, X7R, +/-10%
5V_SB
5V_ME
RN149 0 Dummy +/-5%
5V_DUAL
RN150 0 +/-5%
+1P05V_ME
+1P05V_PCH
RN148 0 +/-5% Dummy
20120830
Support Intel Small Business Advantage
Platforms that support M3 power states without the ability to communicate with Intel ME via LAN
20120829 Change ME Power IC
S5
S0
S_SLP_M#
S_SLP_M#--L Q107导通
S_SLP_M#--H Q107截止
1D05_ME_EN
1D05_ME_EN--H UP2--Shutdown
1D05_ME_EN--L UP2--Work
20120914 For ME Reserved
+V_1.05_PCH/1A
5V_ME
PC95 0.1uF 16V, X7R, +/-10%
PC93 0.1uF 16V, X7R, +/-10%
PC94 22uF 6.3V,X5R,+/-20% c0805h14
+1P05V_ME
1.05V
1A Imax
UP4
VIN
VOUT
EN
ADJ
VDD
PGOOD
GND1
GND2
NC
RT9018B18PSP
1D05_ME_EN
R710 3.16K +/-1%
C571 100pF 50V, NPO, +/-5% Dummy
R501 10K +/-1%
C569 22uF 6.3V,X5R,+/-20% c0805h14
C570 22uF 6.3V,X5R,+/-20% c0805h14
PC96 0.1uF 16V, X7R, +/-10%
+1P05V_ME
R502 100KOhm +/-1%
P_1P5V_PCH_PG
R750 0 +/-5% Dummy
PCH_MEPWRGD
20120830 1.05V_ME UP2 Change from RT8068 to RT8015AGQW
1.5V_PCH UP8 Change from APL5932AKAI-TRG to RT9045GSP
FOXCONN PCEG
Title
1.05V_PCH/ME
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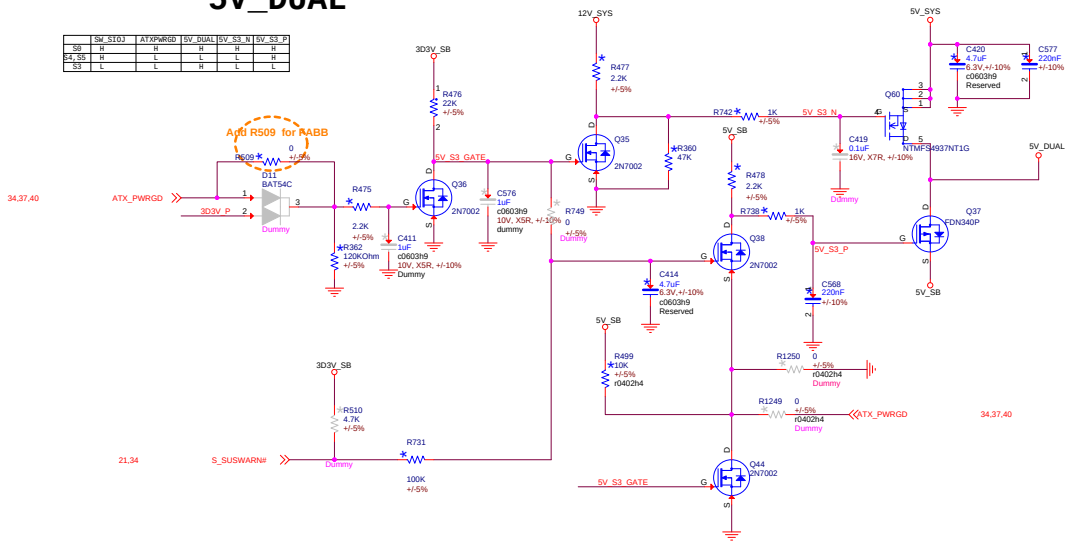
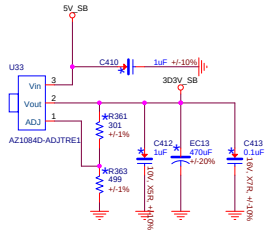
5V_DUAL

	SW_SIOJ	ATXPWRGD	5V_DUAL	5V_S3_N	5V_S3_P
S0	H	H	H	H	H
S4,S5	H	L	L	L	H
S3	L	L	H	L	L



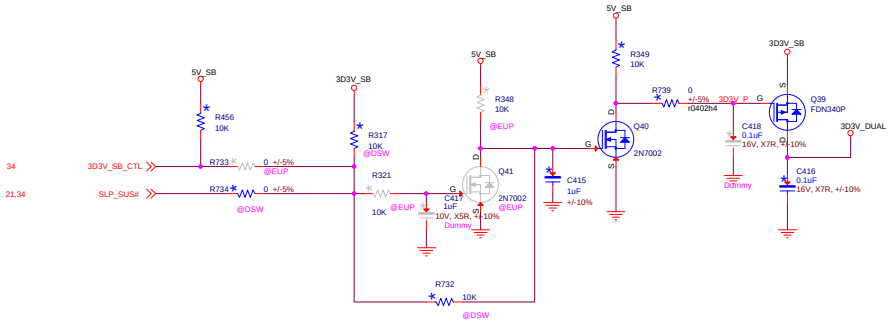
3D3V_SB

Max. output current = 3A



Vout=Vref(1+R2/R1)+IadjR2
R1 is Up Resistor.
Iadj=50UA
Vref=1.25V

3D3V_DUAL



FOXCONN PCEG

Title: 5V_DUAL/3D3V_DUAL

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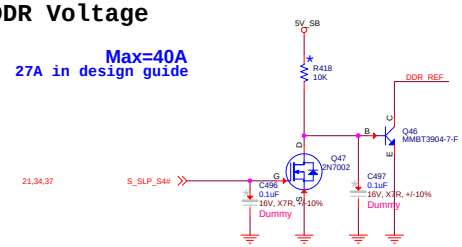
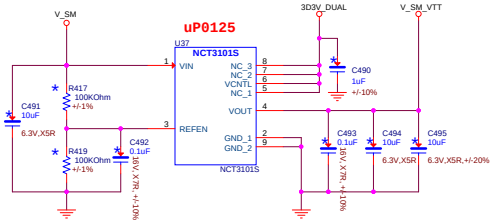
DDR POWER

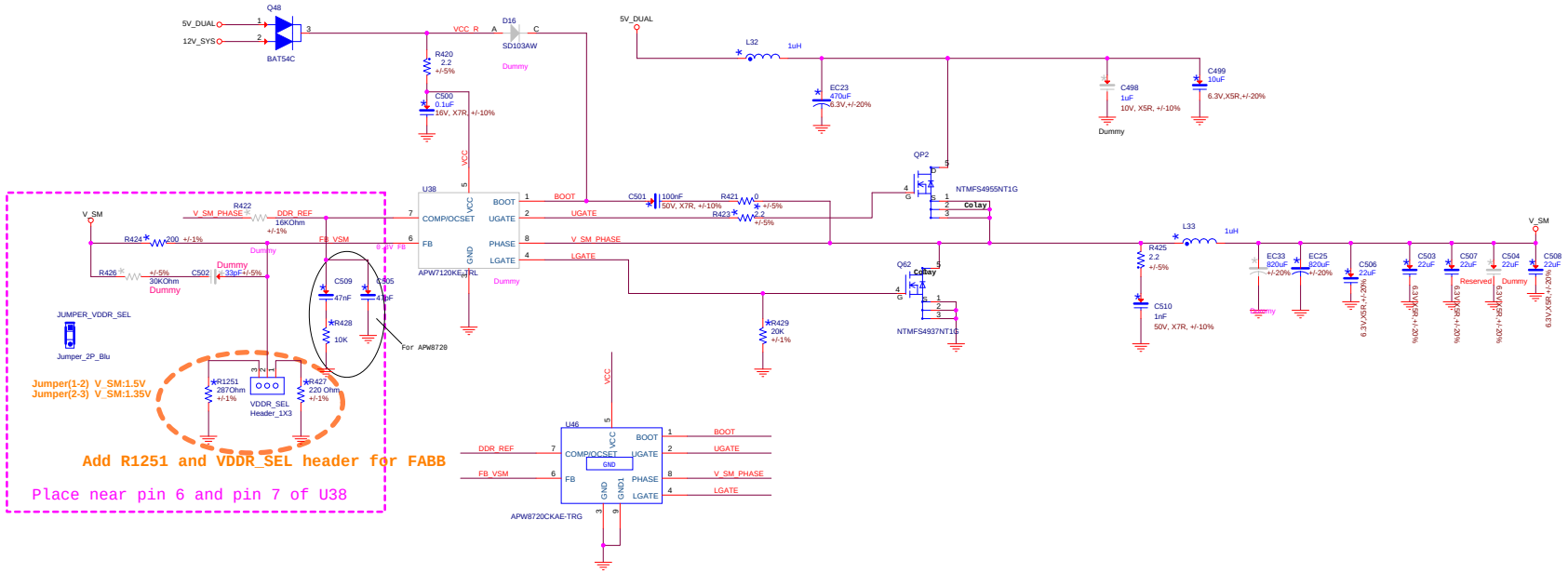
DDR Voltage

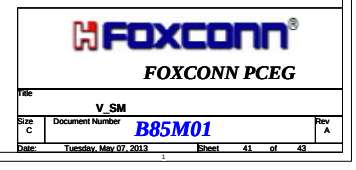
Max=40A
27A in design guide

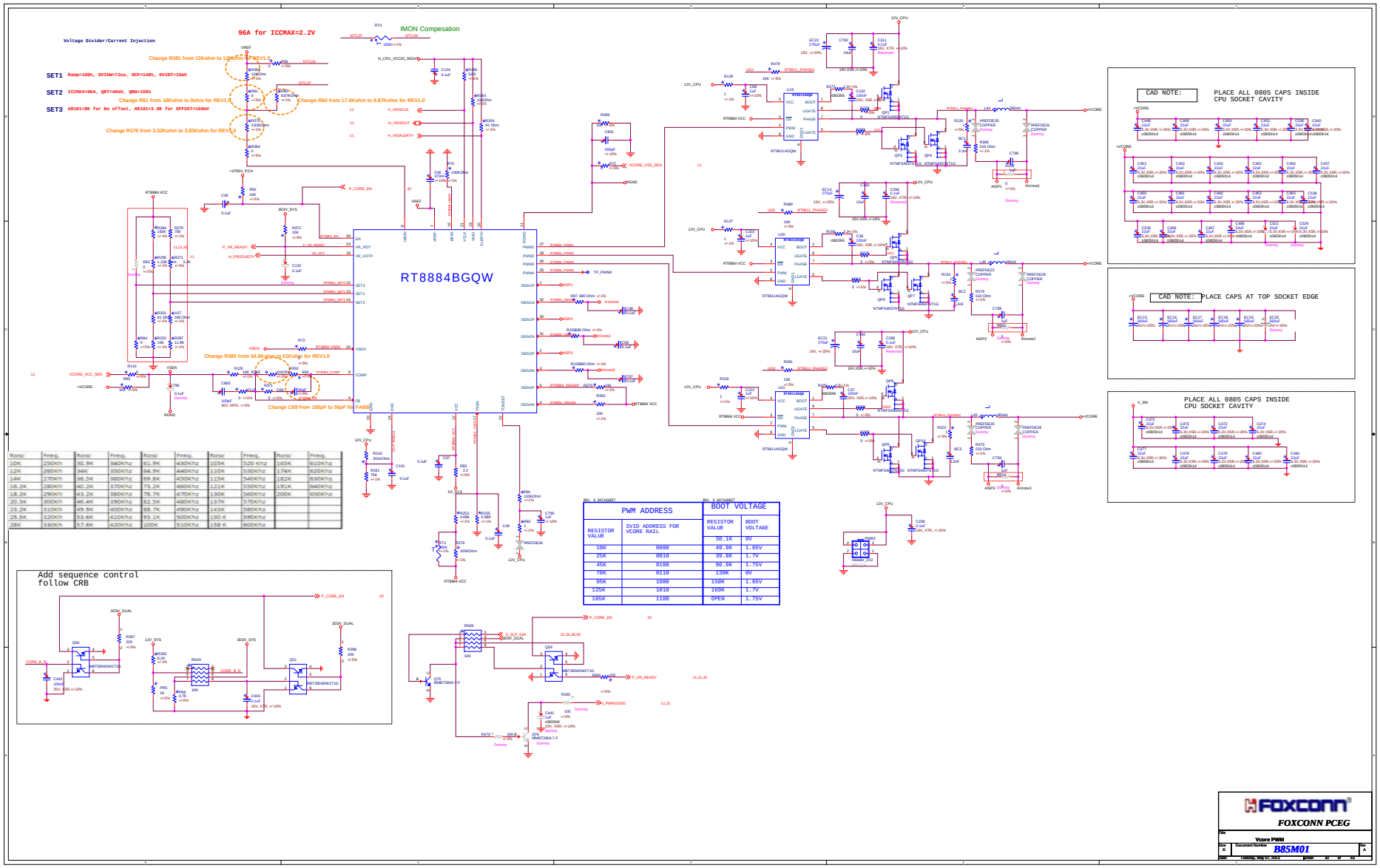




Output voltage: +0_75VRUN +/-5%
Output current: 1.5A







RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL
10K	0000
25K	0010
45K	0100
70K	0110
95K	1000
125K	1010
165K	1100

RESISTOR VALUE	BOOT VOLTAGE
30.1K	0V
49.9K	1.65V
39.8K	1.7V
90.9K	1.75V
130K	0V
150K	1.65V
169K	1.7V
OPEN	1.75V

FOXCONN PCEG

Title: Vcore Driver

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