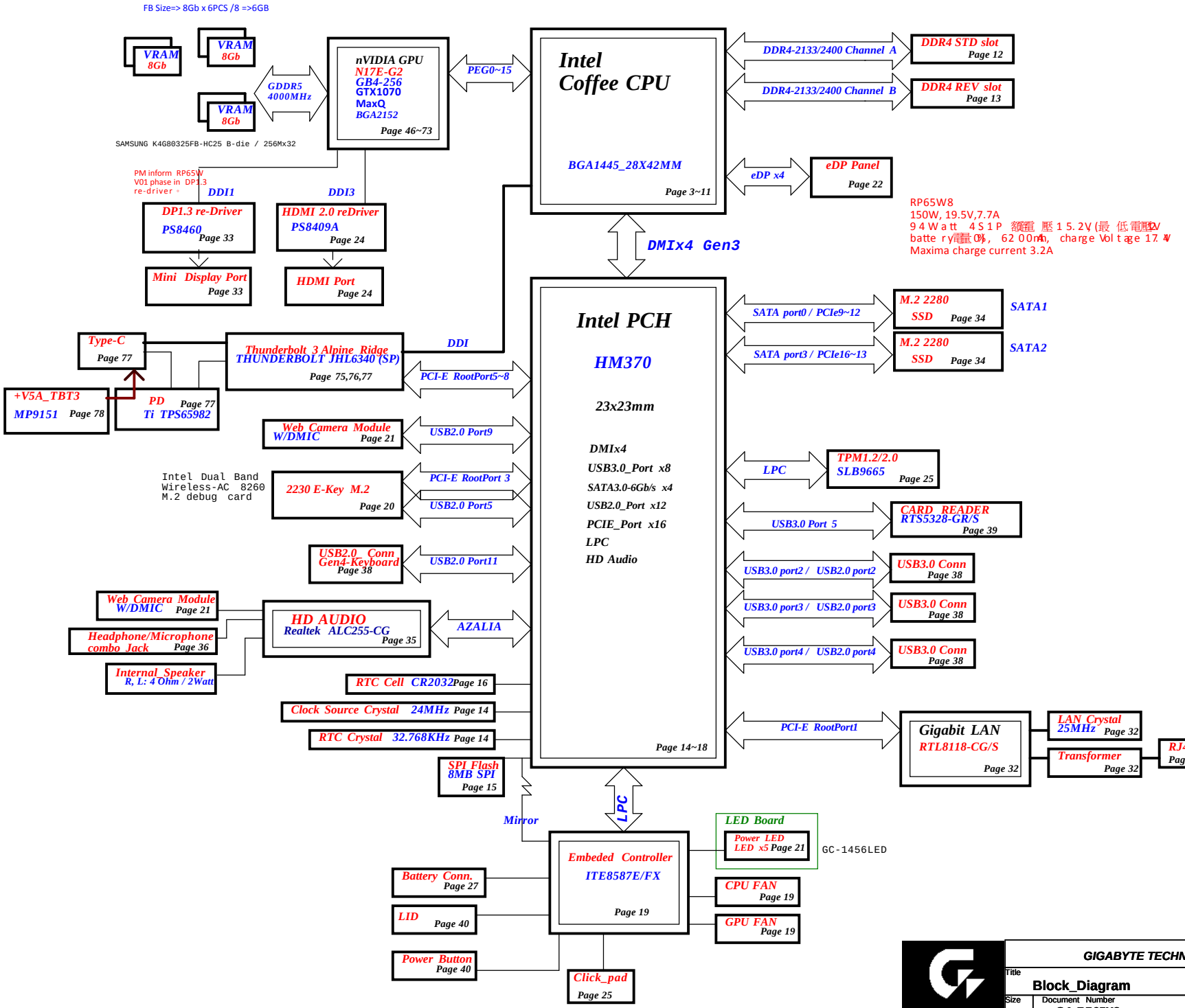

Note:

ALC255 copy from RP64

GIGABYTE TECHNOLOGY COPORATION

Title: Block_Diagram

Size | Document Number: GA-RP65X8 | Rev: 1.0

Date: Thursday, February 01, 2018 | Sheet 1 of 78

Circuit, PCB, Layout ..etc Change Note

Rev.	Page	Change Item	Reason	Layout
0.1	32	RTL8118AS-CG change to RTL8118-CG del L1012,C1249 and C1243 add R711296 and C8007		L
	15	PCIE 20 and 19 port P & N change		L
	6	del CR66,CR27 ADD CR67,CR39,CR16 CR 23 change to 20 ohm		
	14	PR1475 pull high +V3.3A_DSW		L
	6	del CR68,CR69		L
	6	Del RT9018A-25PSP ; Add RT8068AZQW		
1.0	15	PR6 , PR7 , PR8 , PR10 , PR11 , PR13 Resistor from 15 ohm change to 0 ohm		
	17	Remove RP161 , RP165 , RP170		
	27	CHR26 Resistor from 232K ohm change to 165K ohm		
	38	R711285 , R711289 , R711293 Resistor from 47K change to 52.3K Remove R71317 , R71319 , R71315 , R71321 , R711364 , R711362 R71313 add resistor 0 ohm		
	28	R71201 mount 100 ohm and Q7120 mount QN7002 MOS.		
	41	IR47 and IR6 resistor from 3.83K change to 7.15K		

Rev.	Page	Change Item	Reason	Layout

GIGABYTE

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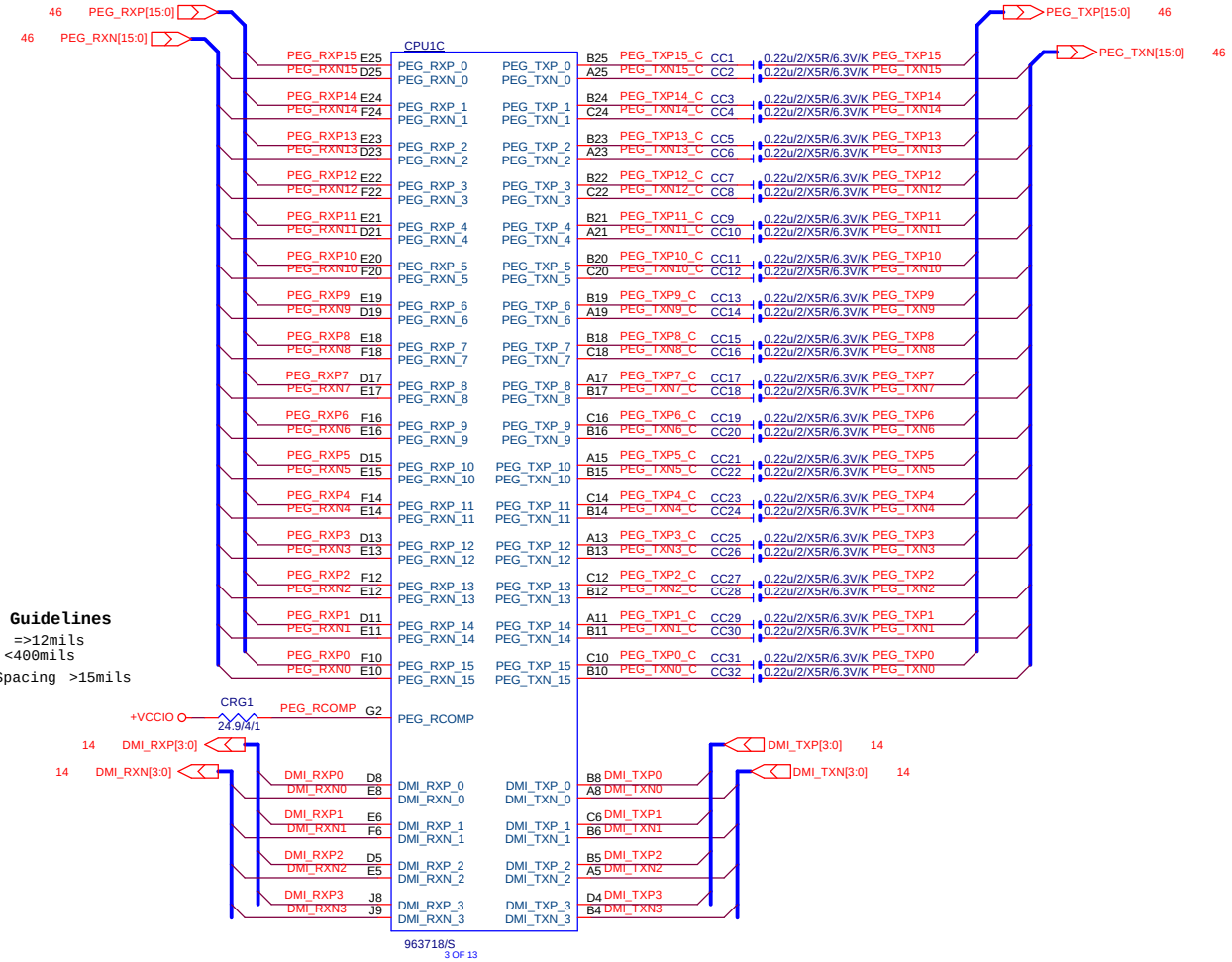
Title: Change_Note

Size | Document Number: GA-RP65X8 | Rev: 1.0

Date: Thursday, February 01, 2018 | Sheet 2 of 78

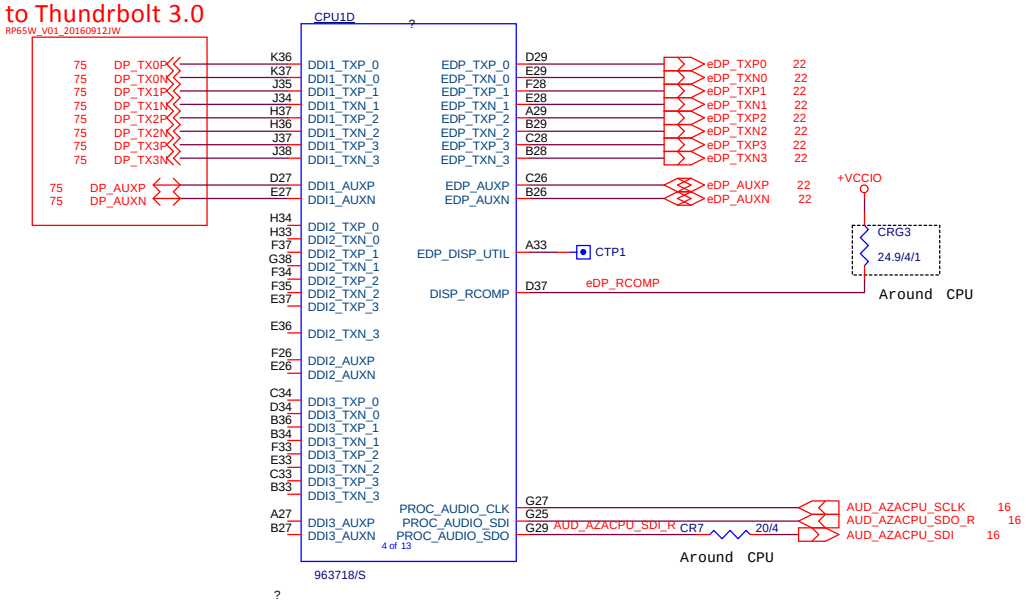


PEG_RCOMP Guidelines

Trace Width =>12mils
Max Length <400mils

Min Trace Spacing >15mils

GIGABYTE TECHNOLOGY COPORATION	
Title	CPU_1-PEG
Size	Document Number: GA-RP65X8 — Rev: 1.0
Date: Thursday, February 01, 2018	Sheet 3 of 78



eDP_RCOMP Guidelines

Trace Width =>12mils
Max Length <100mils
Min Trace Spacing >25mils

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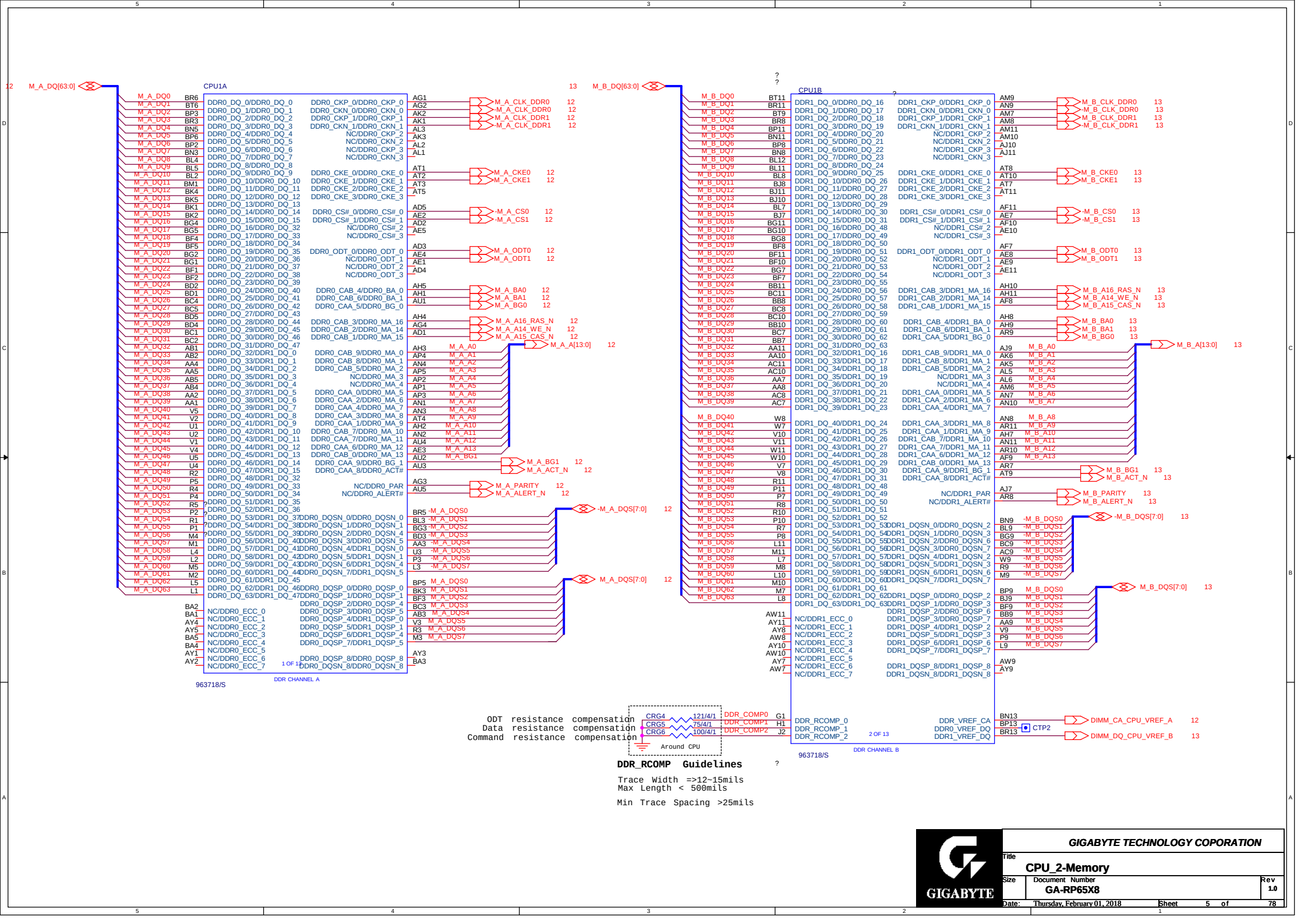
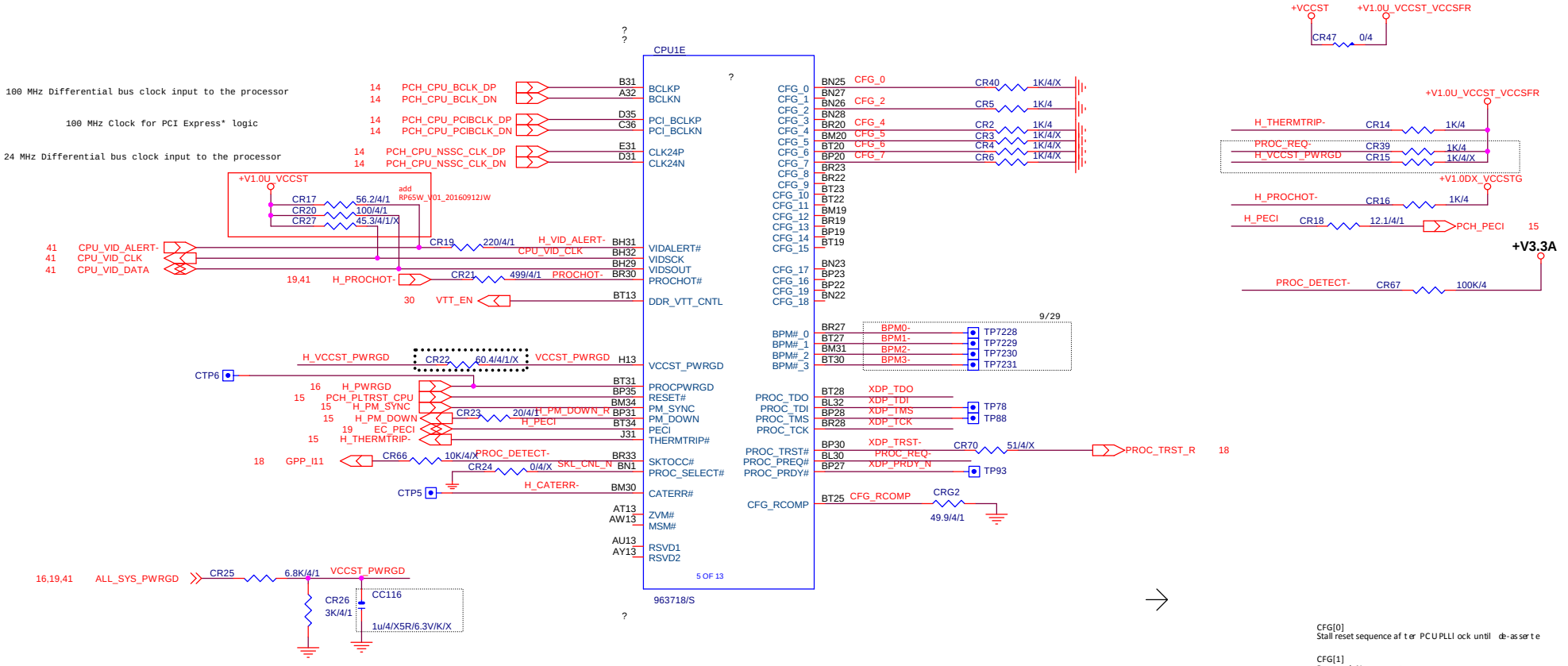
GIGABYTE TECHNOLOGY COPORATION

Title	CPU_3-DDI	
Size	Document Number: GA-RP65X8	Rev: 1.0
Date: Thursday, February 01, 2018	Sheet 4 of 78	


M_A_DQ[63:0]
CPU1A
DDR_CHANNEL_A
963718/S
1 OF 13
M_B_DQ[63:0]
CPU1B
DDR_CHANNEL_B
963718/S
2 OF 13
ODT resistance compensation
Data resistance compensation
Command resistance compensation
Around CPU
DDR_RCOMP Guidelines
Trace Width =>12~15mils
Max Length < 500mils
Min Trace Spacing >25mils
GIGABYTE TECHNOLOGY COPORATION
CPU_2-Memory
GA-RP65X8
Thursday, February 01, 2018

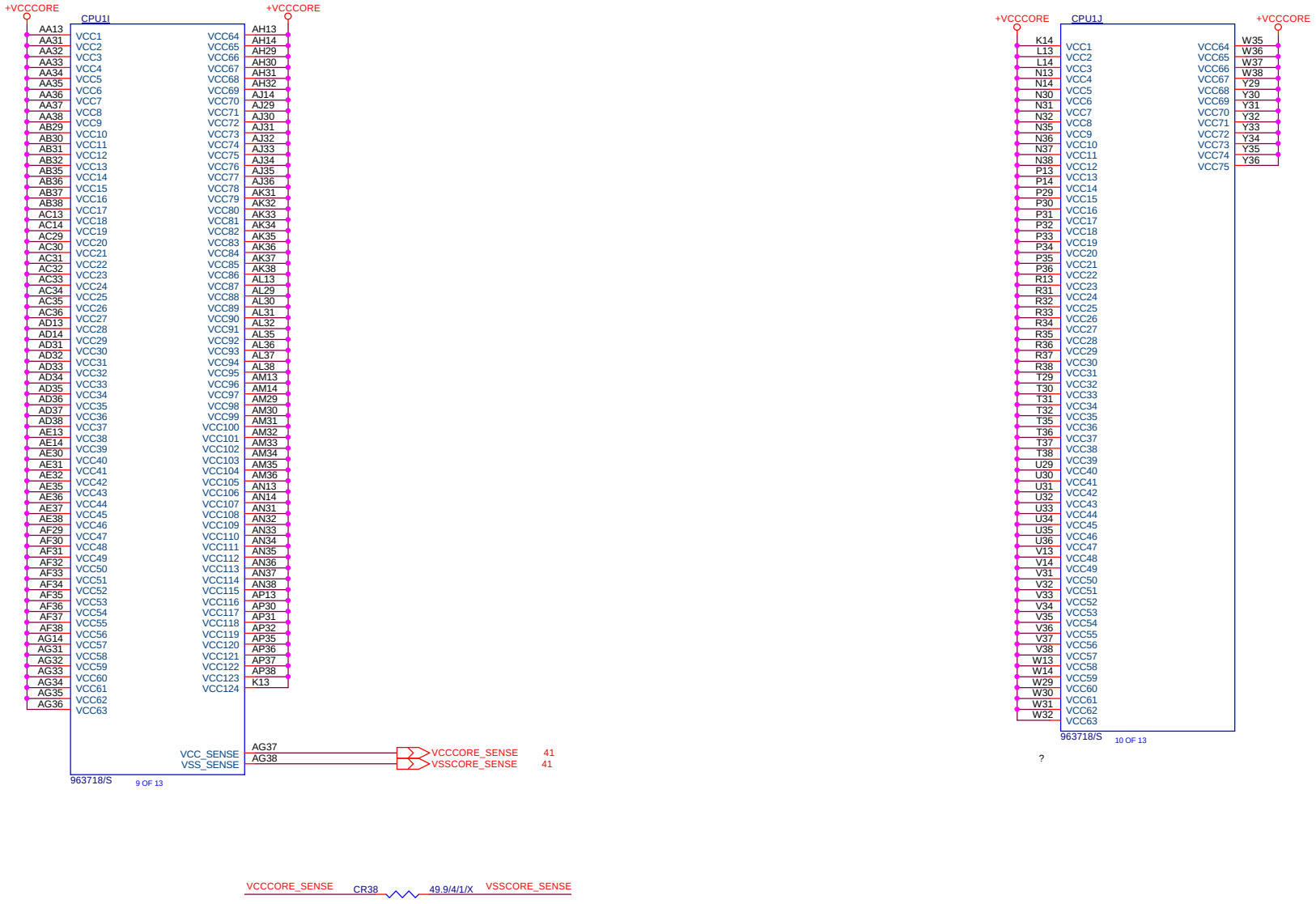


GIGABYTE TECHNOLOGY COPORATION

Title: CPU_3-NOA/JTAG/MISC

Size: Document Number: GA-RP65X8 Rev: 1.0

Date: Thursday, February 01, 2018 Sheet 6 of 78



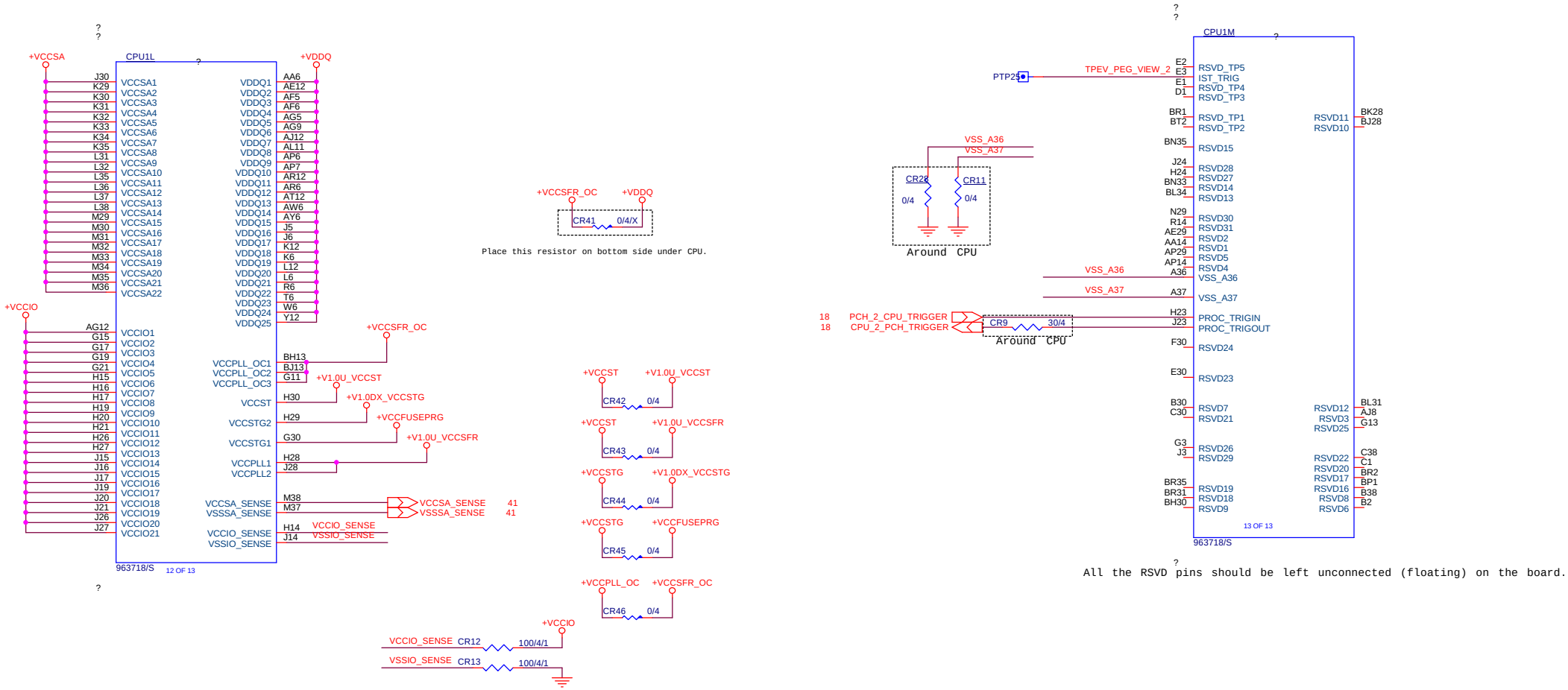
[PAGE_TITLE=CPU SYMBOL - 7 ,10 OF 11 (CPU POWER- 1 OF 3)]

GIGABYTE TECHNOLOGY COPORATION

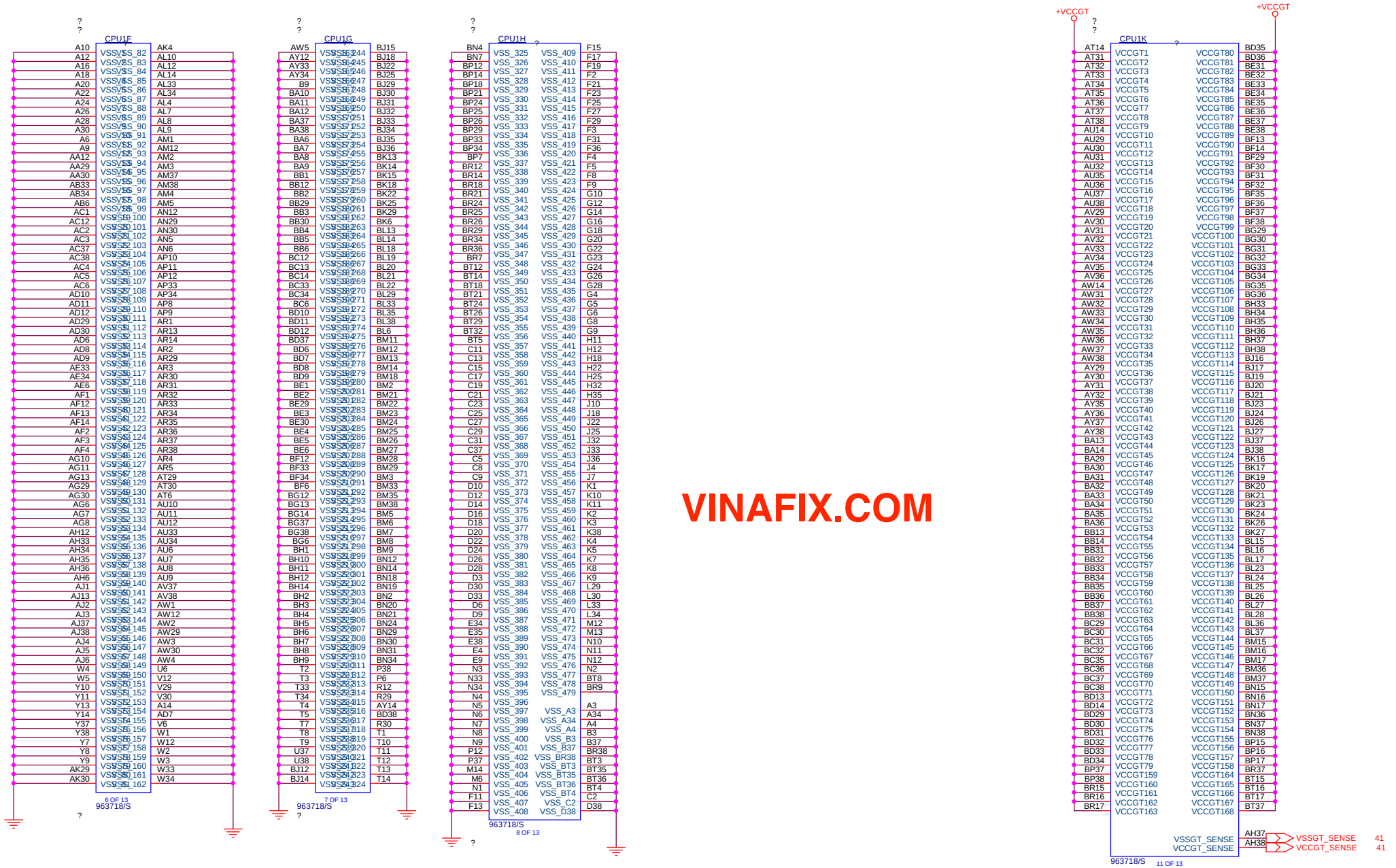
Title: CPU_4-VCC/VDDQ

Size | Document Number: GA-RP65X8 | Rev: 1.0

Date: Thursday, February 01, 2018 | Sheet 7 of 78



GIGABYTE	GIGABYTE TECHNOLOGY COPORATION	
	Title: CPU_6-POWER 2 OF 3	
	Size	Document Number: GA-RP65X8 — Rev: 1.0
	Date: Thursday, February 01, 2018	Sheet 8 of 78

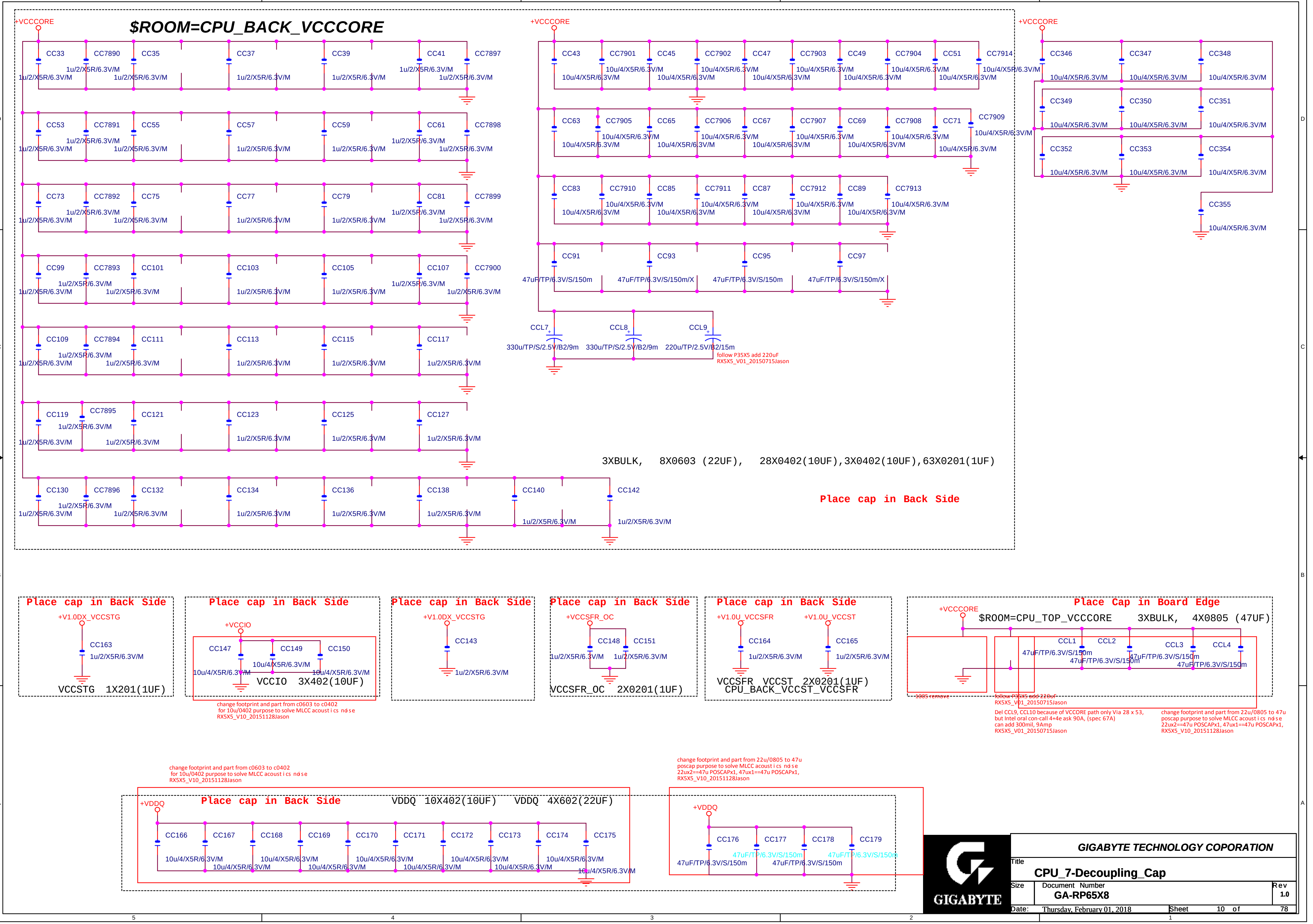


GIGABYTE TECHNOLOGY COPORATION

Title: CPU_7-POWER 3 OF3

Size | Document Number: GA-RP65X8 | Rev: 1.0

Date: Thursday, February 01, 2018 | Sheet 9 of 78


$ROOM=CPU_BACK_VCCCORE
+VCCCORE
CC33 CC7890 CC35 CC37 CC39 CC41 CC7897
CC53 CC7891 CC55 CC57 CC59 CC61 CC7898
CC73 CC7892 CC75 CC77 CC79 CC81 CC7899
CC99 CC7893 CC101 CC103 CC105 CC107 CC7900
CC109 CC7894 CC111 CC113 CC115 CC117
CC119 CC7895 CC121 CC123 CC125 CC127
CC130 CC7896 CC132 CC134 CC136 CC138 CC140 CC142
1u/2/X5R/6.3V/M
CC43 CC7901 CC45 CC7902 CC47 CC7903 CC49 CC7904 CC51 CC7914
CC63 CC7905 CC65 CC7906 CC67 CC7907 CC69 CC7908 CC71 CC7909
CC83 CC7910 CC85 CC7911 CC87 CC7912 CC89 CC7913
10u/4/X5R/6.3V/M
CC91 CC93 CC95 CC97
47uF/TP/6.3V/S/150m
47uF/TP/6.3V/S/150m/X
CCL7 CCL8 CCL9
330u/TP/S/2.5V/B2/9m
220u/TP/2.5V/B2/15m
follow P35X5 add 220uF
RX5X5_V01_20150715Jason
CC346 CC347 CC348
CC349 CC350 CC351
CC352 CC353 CC354
CC355
3XBULK, 8X0603 (22UF), 28X0402(10UF),3X0402(10UF),63X0201(1UF)
Place cap in Back Side
Place cap in Back Side
+V1.0DX_VCCSTG
CC163
1u/2/X5R/6.3V/M
VCCSTG 1X201(1UF)
Place cap in Back Side
+VCCIO
CC147 CC149 CC150
10u/4/X5R/6.3V/M
VCCIO 3X402(10UF)
change footprint and part from c0603 to c0402
for 10u/0402 purpose to solve MLCC acoustic noise
RX5X5_V10_20151128Jason
Place cap in Back Side
+V1.0DX_VCCSTG
CC143
1u/2/X5R/6.3V/M
Place cap in Back Side
+VCCSFR_OC
CC148 CC151
1u/2/X5R/6.3V/M
VCCSFR_OC 2X0201(1UF)
Place cap in Back Side
+V1.0U_VCCSFR +V1.0U_VCCST
CC164 CC165
1u/2/X5R/6.3V/M
VCCSFR VCCST 2X0201(1UF)
CPU_BACK_VCCST_VCCSFR
Place Cap in Board Edge
+VCCCORE
$ROOM=CPU_TOP_VCCCORE 3XBULK, 4X0805 (47UF)
CCL1 CCL2 CCL3 CCL4
47uF/TP/6.3V/S/150m
X085 remove
follow P35X5 add 220uF
RX5X5_V01_20150715Jason
Del CCL9, CCL10 because of VCCORE path only Via 28 x 53,
but Intel oral con-call 4+4e ask 90A, (spec 67A)
can add 300mil, 9Amp
RX5X5_V01_20150715Jason
change footprint and part from 22u/0805 to 47u
poscap purpose to solve MLCC acoustic noise
22ux2==47u POSCAPx1, 47ux1==47u POSCAPx1,
RX5X5_V10_20151128Jason
change footprint and part from c0603 to c0402
for 10u/0402 purpose to solve MLCC acoustic noise
RX5X5_V10_20151128Jason
Place cap in Back Side VDDQ 10X402(10UF) VDDQ 4X602(22UF)
+VDDQ
CC166 CC167 CC168 CC169 CC170 CC171 CC172 CC173 CC174 CC175
10u/4/X5R/6.3V/M
change footprint and part from 22u/0805 to 47u
poscap purpose to solve MLCC acoustic noise
22ux2==47u POSCAPx1, 47ux1==47u POSCAPx1,
RX5X5_V10_20151128Jason
+VDDQ
CC176 CC177 CC178 CC179
47uF/TP/6.3V/S/150m
GIGABYTE
GIGABYTE TECHNOLOGY COPORATION
Title
CPU_7-Decoupling_Cap
Size Document Number Rev
GA-RP65X8 1.0
Date: Thursday, February 01, 2018 Sheet 10 of 78

1X0805(47UF), 7X0402(10UF), 3X0201(1UF)

Place cap in Back Side

+VCCSA

CC180 47uF/TP/6.3V/S/150m

CC181 47uF/TP/6.3V/S/150m

CC183 47uF/TP/6.3V/S/150m/X

CC185 10u/4/X5R/6.3V/M

CC187 10u/4/X5R/6.3V/M

CC188 1u/2/X5R/6.3V/M

CC189 1u/2/X5R/6.3V/M

CC190 1u/2/X5R/6.3V/M

20150612 AE informs ISL95855 量產測項(Change the output capvalue is for intel VTT DMM 調整設定的切換頻率較高(2MHZ), pcap放電太慢要改MLCC)建議修改+VCCGT & +VCCSA電容輔較應速度較快, change ICL19 330uF to 47uF x2, ICL18 330uF to 220uF ICL15 330uF to 220uF CC181 10uF to 22uF, CC183 10uF to 22uF RX5K5_V01_20150617Jason

change footprint and part from c0603 to c0402 for 10u/0402 purpose to solve MLCC acoustics noise RX5X5_V10_20151128Jason

change footprint and part from 22u/0603 to 47u poscap purpose to solve MLCC acoustics noise 22ux2==47u POSCAPx1 47ux1==47u POSCAPx1 RX5X5_V10_20151128Jason

Place Cap in Board Edge

$ROOM=CPU_TOP_VCCSA

CCL14 47uF/TP/6.3V/S/150m

1005 remove

change footprint and part from 22u/0805 to 47u poscap purpose to solve MLCC acoustics noise 22ux2==47u POSCAPx1, 47ux1==47u POSCAPx1, RX5X5_V10_20151128Jason

2XBULK , 1X0805(22UF)

CC356 CC357 CC358 CC359 10u/4/X5R/6.3V/M

add more 4EA for common circuit RX5X6_V02_20160427J

remove 4+4e RX5X5_N17_V01_20160125

change footprint and part from 22u/0805 to 47u poscap purpose to solve MLCC acoustics noise 22ux2==47u POSCAPx1, 47ux1==47u POSCAPx1, RX5X5_V10_20151128Jason

Place Cap in Board Edge

CCL16 330u/TP/S/2.5V/B2/9m

CCL17 330u/TP/S/2.5V/B2/9m

CC215 CC216 CC217 CC218 CC219 CC220 47uF/TP/6.3V/S/150m

4XBULK, 6X0805(47UF)

change +VCCGT cap NA, discrete no need RX5X6_V10_20160702J

add +VCCGT cap components back RX5X6_V10_BOM10D_20160810J

add +VCCGT cap components back RX5X6_V10_BOM10D_20160810J

change +VCCGT cap NA, discrete no need RX5X6_V10_20160702J

3XBULK (SMC7343D), 8X0603(22UF), 35X0402 (10UF), 68X0201 (1UF)

+VCCGT

CC226 CC228 CC230 CC232 CC234 1u/4/X5R/6.3V/K

CC246 CC248 CC250 CC252 CC254 1u/4/X5R/6.3V/K

CC266 CC268 CC270 CC272 CC274 1u/4/X5R/6.3V/K

Place cap in Back Side

+VCCGT

CC236 CC238 CC240 CC242 CC244 10u/4/X5R/6.3V/M

CC256 CC258 CC260 CC262 CC264 10u/4/X5R/6.3V/M

CC291 CC293 CC295 CC297 47uF/TP/6.3V/S/150m 47uF/TP/6.3V/S/150m/X 47uF/TP/6.3V/S/150m 47uF/TP/6.3V/S/150m/X

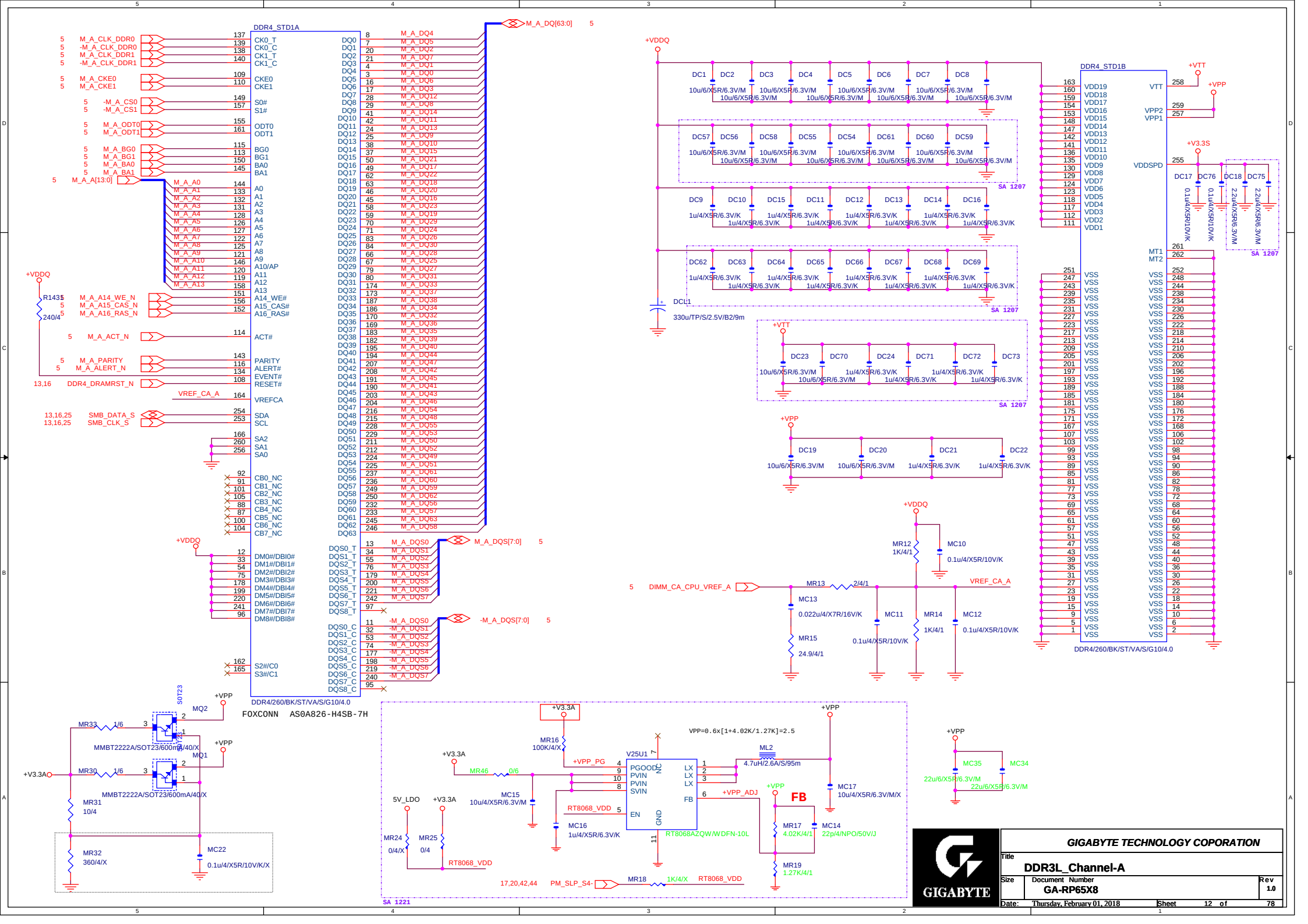
change footprint and part from 22u/0805 to 47u poscap purpose to solve MLCC acoustics noise 22ux2==47u POSCAPx1, 47ux1==47u POSCAPx1, RX5X5_V10_20151128Jason

GIGABYTE TECHNOLOGY COPORATION

Title: CPU_8-Decoupling_Cap

Size | Document Number: GA-RP65X8 | Rev: 1.0

Date: Thursday, February 01, 2018 | Sheet 11 of 78

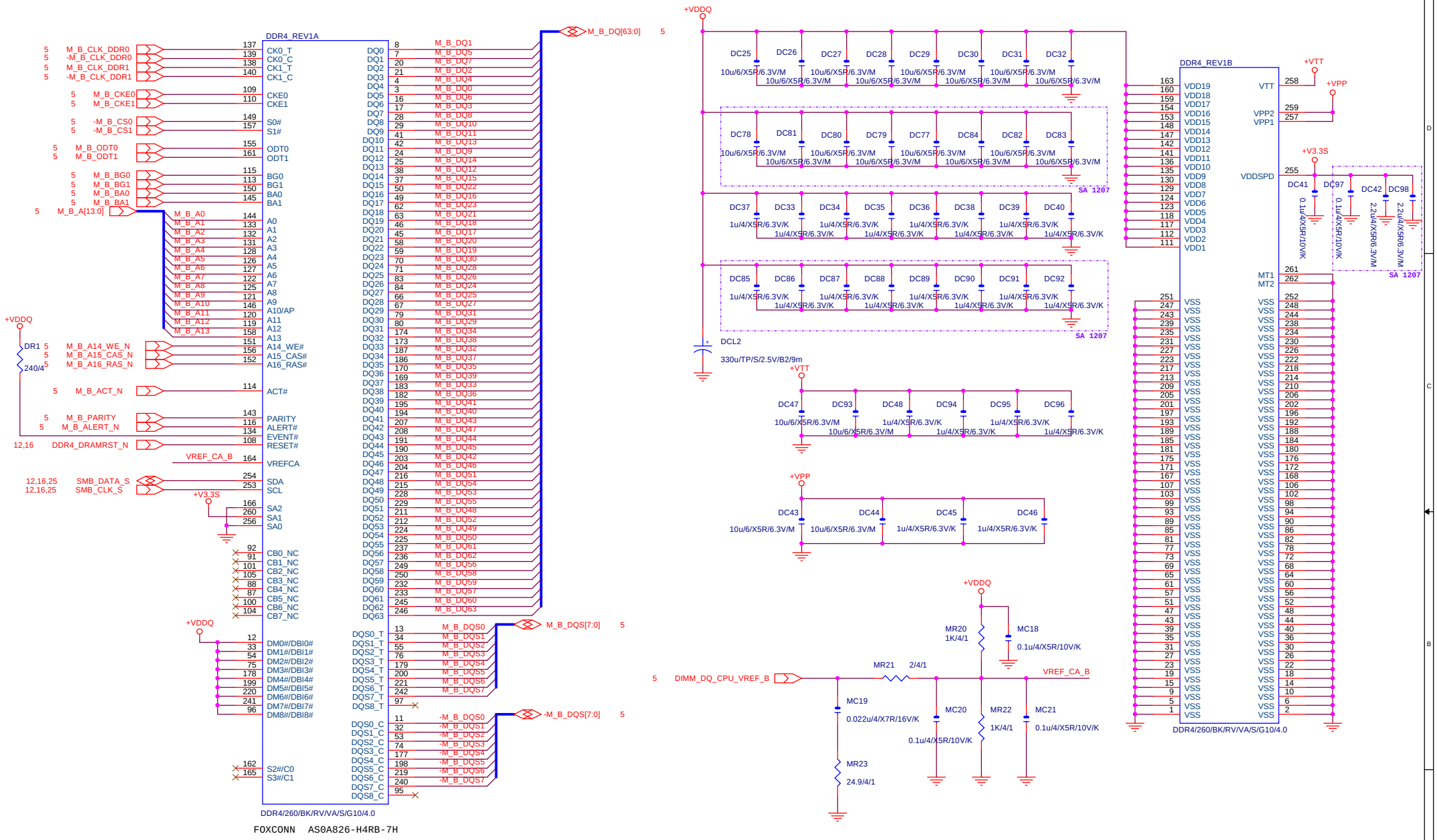


GIGABYTE TECHNOLOGY COPORATION

Title: DDR3L_Channel-A

Size: Document Number: GA-RP65X8 Rev: 1.0

Date: Thursday, February 01, 2018 Sheet 12 of 78

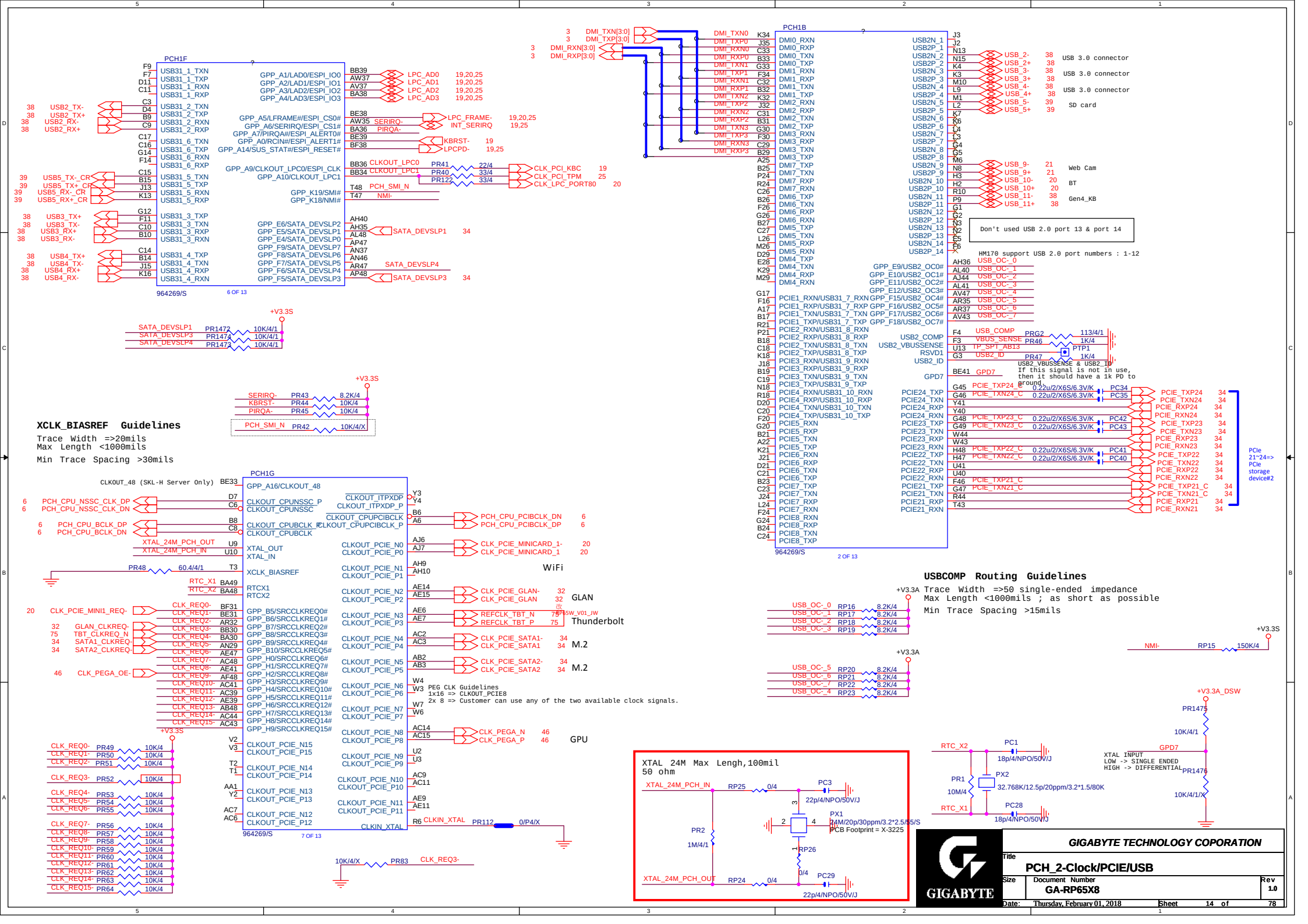


GIGABYTE TECHNOLOGY COPORATION

Title: DDR3L_Channel-B

Size | Document Number: GA-RP65X8 | Rev: 1.0

Date: Thursday, February 01, 2018 | Sheet 13 of 78


PCH1F
964269/S
6 OF 13
PCH1B
964269/S
2 OF 13
PCH1G
964269/S
7 OF 13
XCLK_BIASREF Guidelines
Trace Width =>20mils
Max Length <1000mils
Min Trace Spacing >30mils
USBCOMP Routing Guidelines
+V3.3A Trace Width =>50 single-ended impedance
Max Length <1000mils ; as short as possible
Min Trace Spacing >15mils
HM170 support USB 2.0 port numbers : 1-12
Don't used USB 2.0 port 13 & port 14
USB2_VBUSSENSE & USB2_ID
If this signal is not in use,
then it should have a 1k PD to
ground.
USB 3.0 connector
USB 3.0 connector
USB 3.0 connector
SD card
Web Cam
BT
Gen4_KB
WiFi
GLAN
Thunderbolt
M.2
M.2
GPU
PEG CLK Guidelines
1x16 => CLKOUT_PCIE8
2x 8 => Customer can use any of the two available clock signals.
XTAL 24M Max Lengh,100mil
50 ohm
PCB Footprint = X-3225
XTAL INPUT
LOW -> SINGLE ENDED
HIGH -> DIFFERENTIAL
GIGABYTE TECHNOLOGY COPORATION
PCH_2-Clock/PCIE/USB
GA-RP65X8
Rev 1.0
Thursday, February 01, 2018
Sheet 14 of 78

Place AC caps closer to the PCIe* connector.

Place AC caps closer to the PCIe* connector.

PCH1C

PCIe 9~12 =>PCIe storage device#1

PCIe 9~12 =>PCIe storage device#1

WiFi

GLAN

SATAGP: Hi=>SATA ; Lo=>PCIe

BIOS1 16MB 128M/Q/SPI/SO8/S

SB 0122

PCH1A

SPI0_IO2 & SPI0_IO3 has an internal pull-up.

964269/S

1 OF 13

3 OF 13

HM370

Company	GIGABYTE TECHNOLOGY COPORATION
Title	PCH_1-RTC/SATA/HDA/SPI/L
Size	
Document Number	GA-RP65X8
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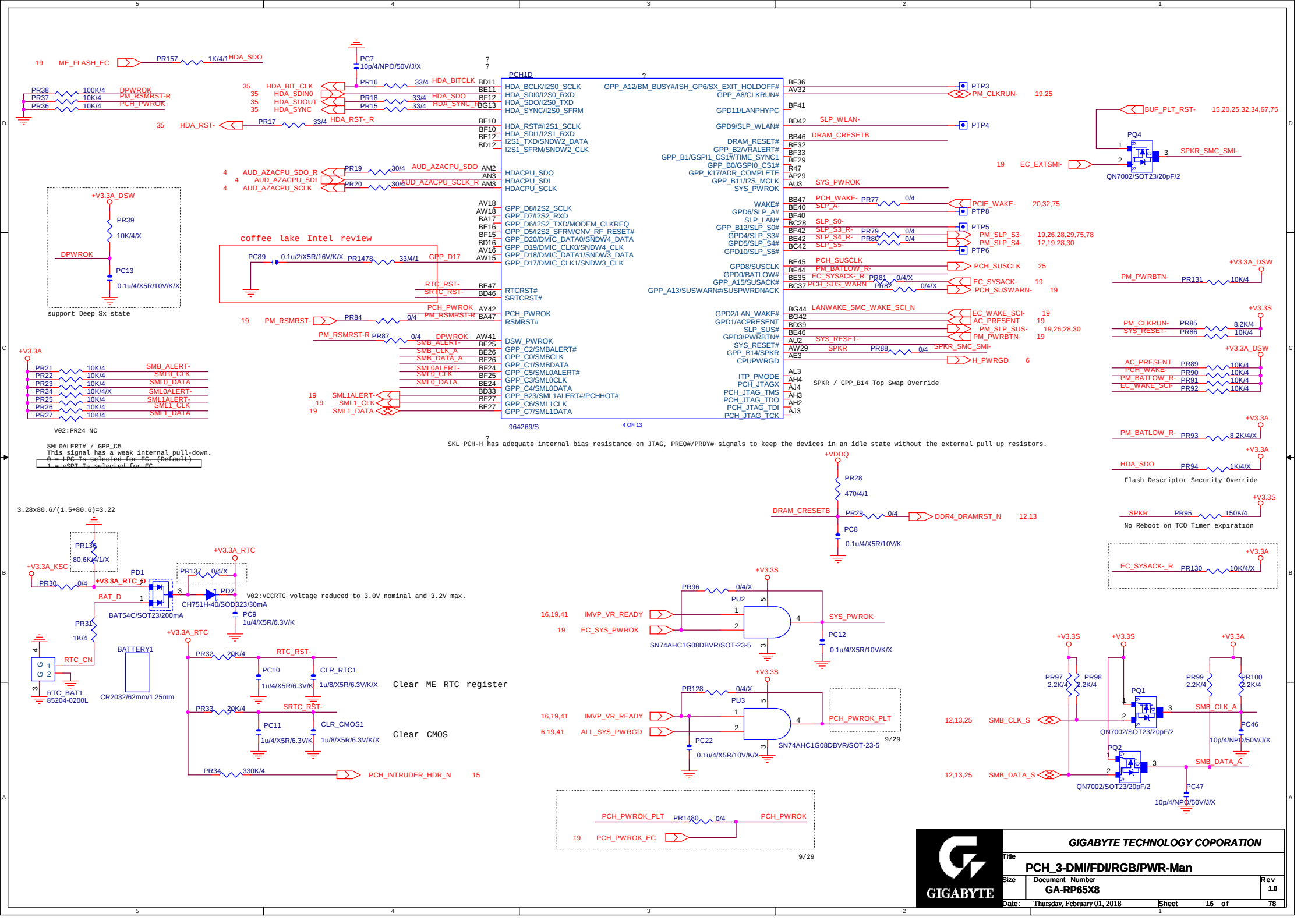
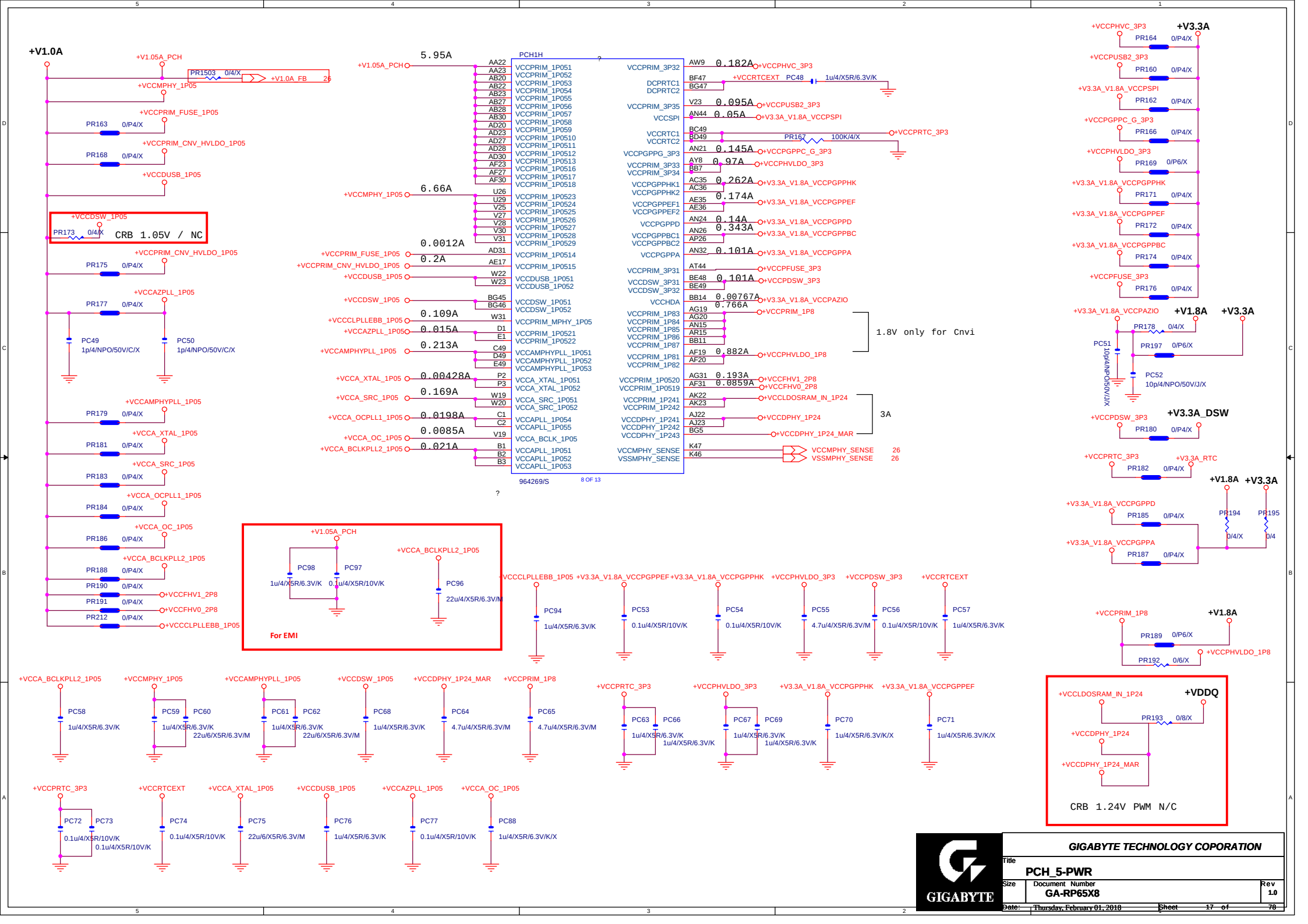
Date:	Thursday, February 01, 2018
Sheet	15 of 78



Company	GIGABYTE TECHNOLOGY COPORATION
Title	PCH_3-DMI/FDI/RGB/PWR-Man
Size	
Document Number	GA-RP65X8
Rev	1.0
Date:	Thursday, February 01, 2018
Sheet	16 of 78


+V1.0A
+V1.05A_PCH
PR1503 0/4/X
+V1.0A_FB 26
+VCCMPHY_1P05
+VCCPRIM_FUSE_1P05
PR163 0/P4/X
+VCCPRIM_CNV_HVLDO_1P05
PR168 0/P4/X
+VCCDUSB_1P05
+VCCDSW_1P05
PR173 0/4/X
CRB 1.05V / NC
+VCCPRIM_CNV_HVLDO_1P05
PR175 0/P4/X
+VCCAZPLL_1P05
PR177 0/P4/X
PC49 1p/4/NPO/50V/C/X
PC50 1p/4/NPO/50V/C/X
+VCCAMPHYPLL_1P05
PR179 0/P4/X
+VCCA_XTAL_1P05
PR181 0/P4/X
+VCCA_SRC_1P05
PR183 0/P4/X
+VCCA_OCPLL1_1P05
PR184 0/P4/X
+VCCA_OC_1P05
PR186 0/P4/X
+VCCA_BCLKPLL2_1P05
PR188 0/P4/X
PR190 0/P4/X
PR191 0/P4/X
PR212 0/P4/X
+VCCFHV1_2P8
+VCCFHV0_2P8
+VCCCLPLLEBB_1P05
PCH1H
964269/S
8 OF 13
5.95A
6.66A
0.0012A
0.2A
0.109A
0.015A
0.213A
0.00428A
0.169A
0.0198A
0.0085A
0.021A
VCCPRIM_1P051
VCCPRIM_1P052
VCCPRIM_1P053
VCCPRIM_1P054
VCCPRIM_1P055
VCCPRIM_1P056
VCCPRIM_1P057
VCCPRIM_1P058
VCCPRIM_1P059
VCCPRIM_1P0510
VCCPRIM_1P0511
VCCPRIM_1P0512
VCCPRIM_1P0513
VCCPRIM_1P0516
VCCPRIM_1P0517
VCCPRIM_1P0518
VCCPRIM_1P0523
VCCPRIM_1P0524
VCCPRIM_1P0525
VCCPRIM_1P0526
VCCPRIM_1P0527
VCCPRIM_1P0528
VCCPRIM_1P0529
VCCPRIM_1P0514
VCCPRIM_1P0515
VCCDUSB_1P051
VCCDUSB_1P052
VCCDSW_1P051
VCCDSW_1P052
VCCPRIM_MPHY_1P05
VCCPRIM_1P0521
VCCPRIM_1P0522
VCCAMPHYPLL_1P051
VCCAMPHYPLL_1P052
VCCAMPHYPLL_1P053
VCCA_XTAL_1P051
VCCA_XTAL_1P052
VCCA_SRC_1P051
VCCA_SRC_1P052
VCCAPLL_1P054
VCCAPLL_1P055
VCCA_BCLK_1P05
VCCAPLL_1P051
VCCAPLL_1P052
VCCAPLL_1P053
VCCPRIM_3P32
DCPRTC1
DCPRTC2
VCCPRIM_3P35
VCCSPI
VCCRTC1
VCCRTC2
VCCPGPPG_3P3
VCCPRIM_3P33
VCCPRIM_3P34
VCCPGPPHK1
VCCPGPPHK2
VCCPGPPEF1
VCCPGPPEF2
VCCPGPPD
VCCPGPPBC1
VCCPGPPBC2
VCCPGPPA
VCCPRIM_3P31
VCCDSW_3P31
VCCDSW_3P32
VCCHDA
VCCPRIM_1P83
VCCPRIM_1P84
VCCPRIM_1P85
VCCPRIM_1P86
VCCPRIM_1P87
VCCPRIM_1P81
VCCPRIM_1P82
VCCPRIM_1P0520
VCCPRIM_1P0519
VCCPRIM_1P241
VCCPRIM_1P242
VCCDPHY_1P241
VCCDPHY_1P242
VCCDPHY_1P243
VCCMPHY_SENSE
VSSMPHY_SENSE
AW9 0.182A +VCCPHVC_3P3
BF47 +VCCRTCEXT PC48 1u/4/X5R/6.3V/K
BG47
V23 0.095A +VCCPUSB2_3P3
AN44 0.05A +V3.3A_V1.8A_VCCPSPI
BC49
BD49 PR167 100K/4/X +VCCPRTC_3P3
AN21 0.145A +VCCPGPPC_G_3P3
AY8 0.97A +VCCPHVLDO_3P3
BB7
AC35 0.262A +V3.3A_V1.8A_VCCPGPPHK
AC36
AE35 0.174A +V3.3A_V1.8A_VCCPGPPEF
AE36
AN24 0.14A +V3.3A_V1.8A_VCCPGPPD
AN26 0.343A +V3.3A_V1.8A_VCCPGPPBC
AP26
AN32 0.101A +V3.3A_V1.8A_VCCPGPPA
AT44 +VCCPFUSE_3P3
BE48 0.101A +VCCPDSW_3P3
BE49
BB14 0.00767A +V3.3A_V1.8A_VCCPAZIO
0.766A
AG19 +VCCPRIM_1P8
AG20
AN15
AR15
BB11
1.8V only for Cnvi
AF19 0.882A +VCCPHVLDO_1P8
AF20
AG31 0.193A +VCCFHV1_2P8
AF31 0.0859A +VCCFHV0_2P8
AK22 +VCCLDOSRAM_IN_1P24
AK23
AJ22 +VCCDPHY_1P24
AJ23
BG5 +VCCDPHY_1P24_MAR
3A
K47 VCCMPHY_SENSE 26
K46 VSSMPHY_SENSE 26
For EMI
+V1.05A_PCH
PC98 1u/4/X5R/6.3V/K
PC97 0.1u/4/X5R/10V/K
+VCCA_BCLKPLL2_1P05
PC96 22u/4/X5R/6.3V/M
+VCCCLPLLEBB_1P05
PC94 1u/4/X5R/6.3V/K
+V3.3A_V1.8A_VCCPGPPEF
PC53 0.1u/4/X5R/10V/K
+V3.3A_V1.8A_VCCPGPPHK
PC54 0.1u/4/X5R/10V/K
+VCCPHVLDO_3P3
PC55 4.7u/4/X5R/6.3V/M
+VCCPDSW_3P3
PC56 0.1u/4/X5R/10V/K
+VCCRTCEXT
PC57 1u/4/X5R/6.3V/K
+VCCA_BCLKPLL2_1P05
PC58 1u/4/X5R/6.3V/K
+VCCMPHY_1P05
PC59 1u/4/X5R/6.3V/K
PC60 22u/6/X5R/6.3V/M
+VCCAMPHYPLL_1P05
PC61 1u/4/X5R/6.3V/K
PC62 22u/6/X5R/6.3V/M
+VCCDSW_1P05
PC68 1u/4/X5R/6.3V/K
+VCCDPHY_1P24_MAR
PC64 4.7u/4/X5R/6.3V/M
+VCCPRIM_1P8
PC65 4.7u/4/X5R/6.3V/M
+VCCPRTC_3P3
PC63 1u/4/X5R/6.3V/K
PC66 1u/4/X5R/6.3V/K
+VCCPHVLDO_3P3
PC67 1u/4/X5R/6.3V/K
PC69 1u/4/X5R/6.3V/K
+V3.3A_V1.8A_VCCPGPPHK
PC70 1u/4/X5R/6.3V/K/X
+V3.3A_V1.8A_VCCPGPPEF
PC71 1u/4/X5R/6.3V/K/X
+VCCPRTC_3P3
PC72 0.1u/4/X5R/10V/K
PC73 0.1u/4/X5R/10V/K
+VCCRTCEXT
PC74 0.1u/4/X5R/10V/K
+VCCA_XTAL_1P05
PC75 22u/6/X5R/6.3V/M
+VCCDSUB_1P05
PC76 1u/4/X5R/6.3V/K
+VCCAZPLL_1P05
PC77 0.1u/4/X5R/10V/K
+VCCA_OC_1P05
PC88 1u/4/X5R/6.3V/K/X
+V3.3A
+VCCPHVC_3P3
PR164 0/P4/X
+VCCPUSB2_3P3
PR160 0/P4/X
+V3.3A_V1.8A_VCCPSPI
PR162 0/P4/X
+VCCPGPPC_G_3P3
PR166 0/P4/X
+VCCPHVLDO_3P3
PR169 0/P6/X
+V3.3A_V1.8A_VCCPGPPHK
PR171 0/P4/X
+V3.3A_V1.8A_VCCPGPPEF
PR172 0/P4/X
+V3.3A_V1.8A_VCCPGPPBC
PR174 0/P4/X
+VCCPFUSE_3P3
PR176 0/P4/X
+V3.3A_V1.8A_VCCPAZIO
+V1.8A
PR178 0/4/X
PR197 0/P6/X
PC51 10p/4/NPO/50V/J/X
PC52 10p/4/NPO/50V/J/X
+V3.3A_DSW
+VCCPDSW_3P3
PR180 0/P4/X
+VCCPRTC_3P3
PR182 0/P4/X
+V3.3A_RTC
+V3.3A_V1.8A_VCCPGPPD
PR185 0/P4/X
PR194 0/4/X
PR195 0/4
+V3.3A_V1.8A_VCCPGPPA
PR187 0/P4/X
+VCCPRIM_1P8
PR189 0/P6/X
PR192 0/6/X
+VCCPHVLDO_1P8
+VCCLDOSRAM_IN_1P24
+VDDQ
PR193 0/8/X
+VCCDPHY_1P24
+VCCDPHY_1P24_MAR
CRB 1.24V PWM N/C
GIGABYTE TECHNOLOGY COPORATION
Title
PCH_5-PWR
Size
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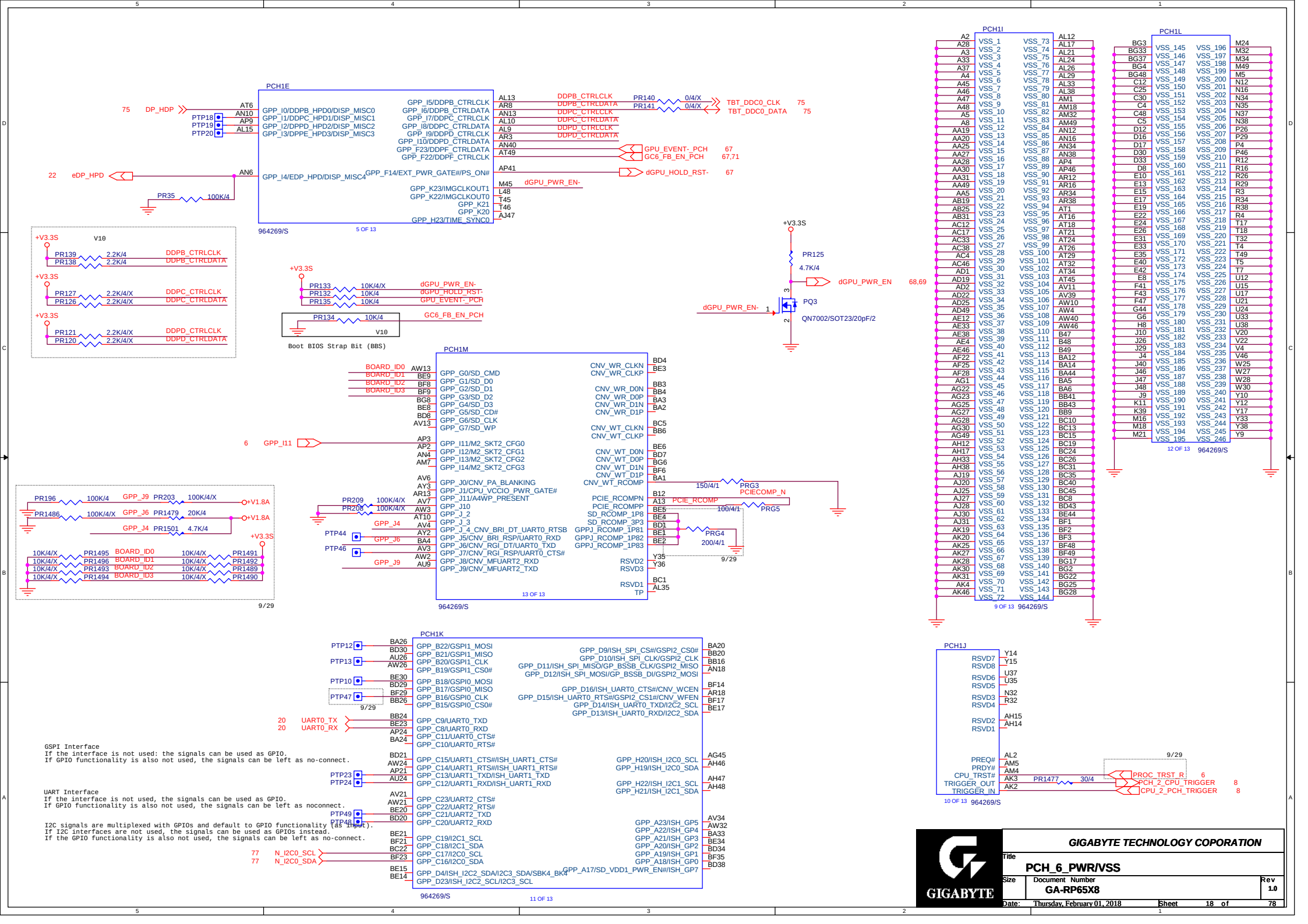
PCH1E
PCH1I
PCH1L
PCH1M
PCH1K
PCH1J
964269/S
5 OF 13
9 OF 13
10 OF 13
11 OF 13
12 OF 13
13 OF 13
DP_HDP
eDP_HPD
Boot BIOS Strap Bit (BBS)
GSPI Interface
If the interface is not used: the signals can be used as GPIO.
If GPIO functionality is also not used, the signals can be left as no-connect.
UART Interface
If the interface is not used, the signals can be used as GPIO.
If GPIO functionality is also not used, the signals can be left as noconnect.
I2C signals are multiplexed with GPIOs and default to GPIO functionality (as input).
If I2C interfaces are not used, the signals can be used as GPIOs instead.
If the GPIO functionality is also not used, the signals can be left as no-connect.
GIGABYTE TECHNOLOGY COPORATION
PCH_6_PWR/VSS
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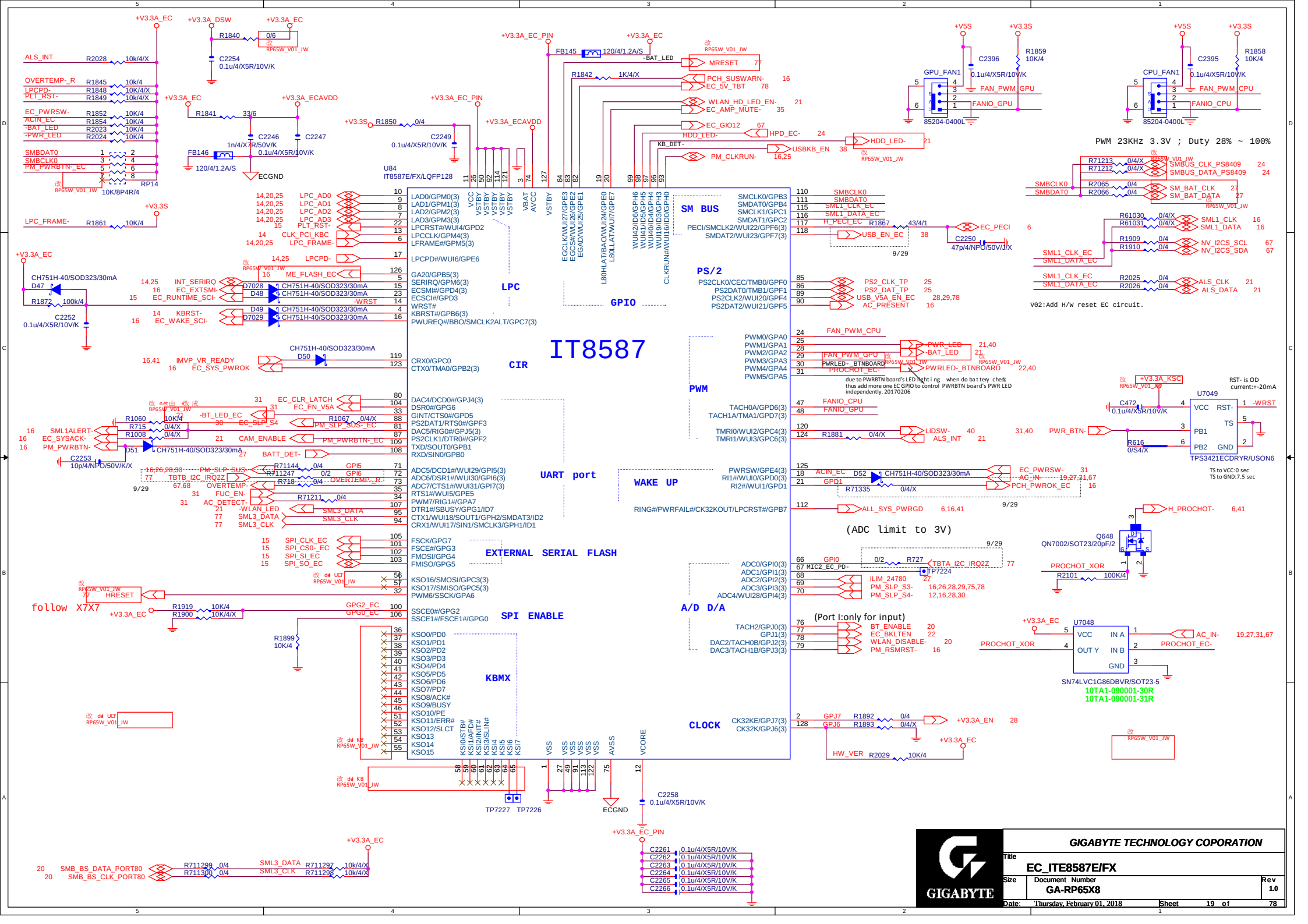
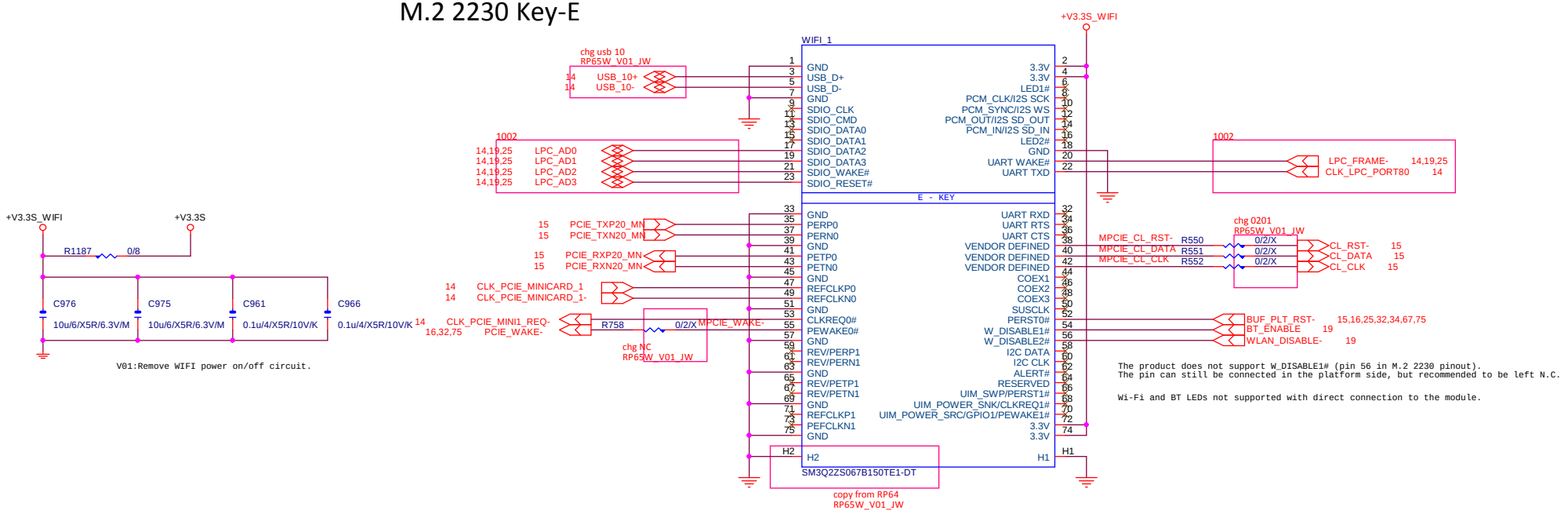
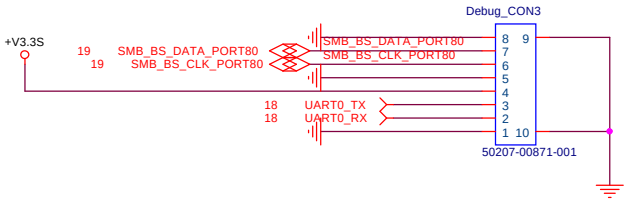

IT8587
SM BUS
PS/2
LPC
GPIO
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
(ADC limit to 3V)
(Port I:only for input)
PWM 23KHz 3.3V ; Duty 28% ~ 100%
follow X7X7
V02:Add H/W reset EC circuit.
GIGABYTE TECHNOLOGY COPORATION
EC_ITE8587E/FX
GA-RP65X8
Thursday, February 01, 2018

M.2 2230 Key-E



MB Side



GIGABYTE TECHNOLOGY COPORATION

Title: WiFi

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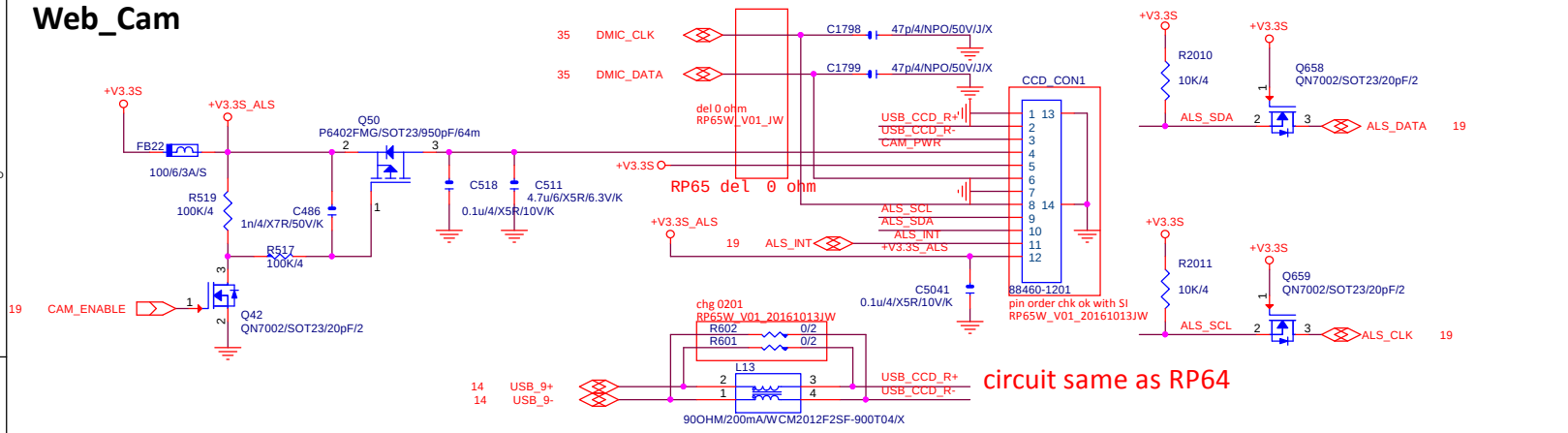
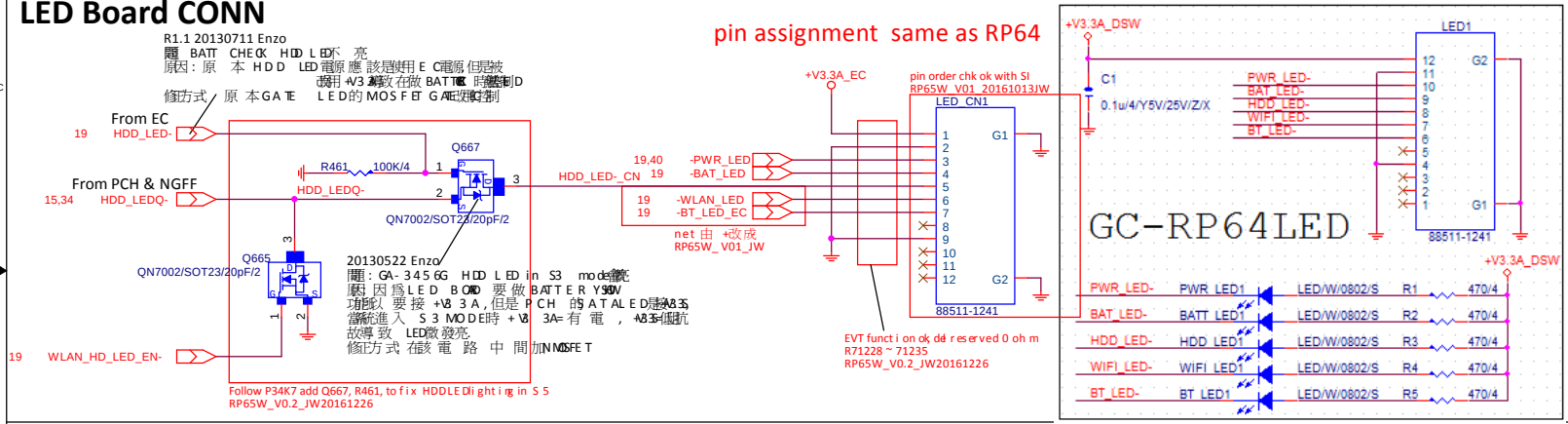
Web_Cam



del gen1 K.B.
RP65W_V01_20160901JW

LED Board CONN



RP65 改
20160901 RP65
del gen1 K.B.

RP65 改
20160901 RP65
del MKBK_CTRL

GIGABYTE TECHNOLOGY COPORATION

Title: Board_Connectors

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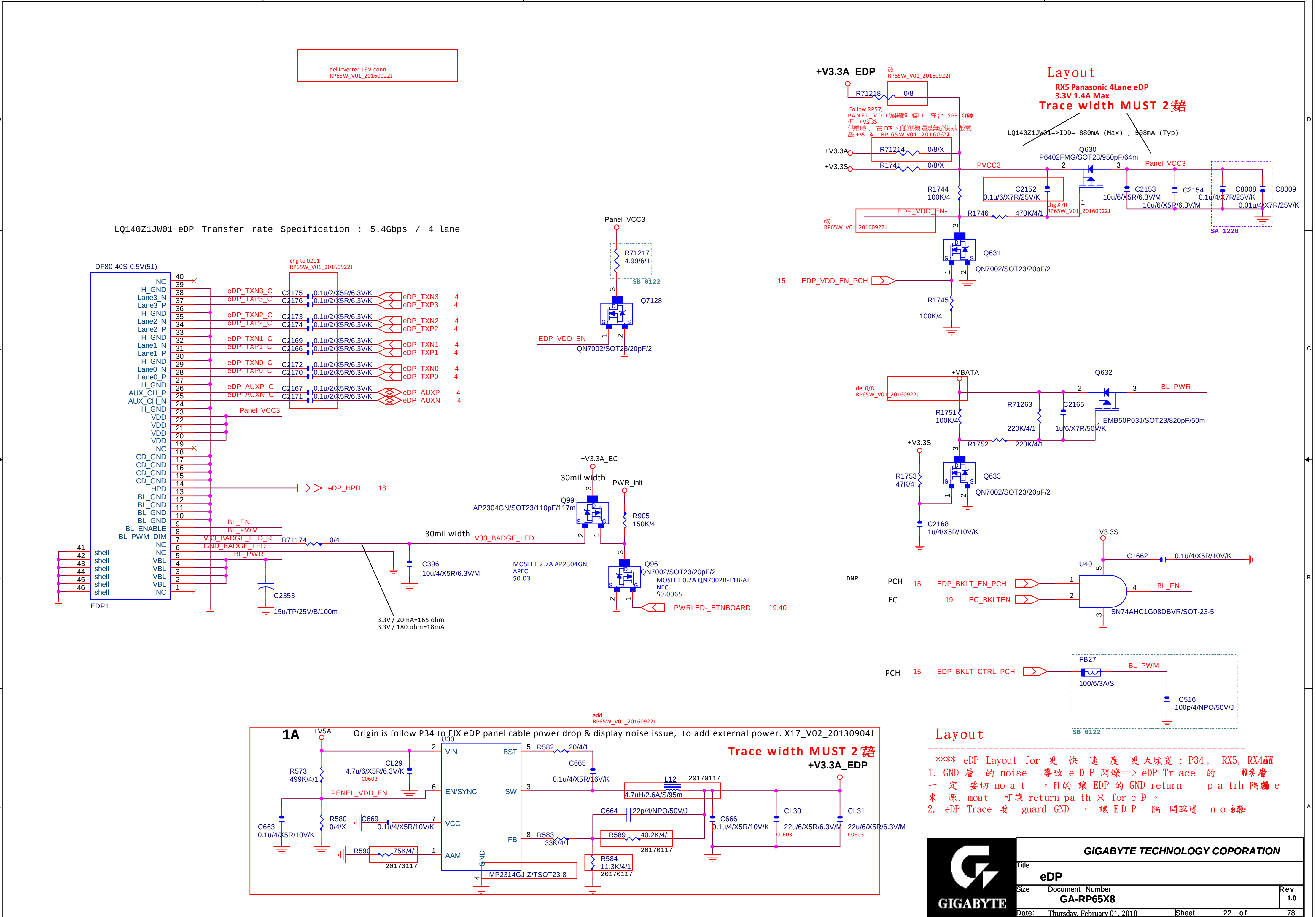
del inverter 19V conn
RP65W_V01_20160922J
LQ140Z1JW01 eDP Transfer rate Specification : 5.4Gbps / 4 lane
DF80-40S-0.5V(51)
EDP1
NC
H_GND
Lane3_N
Lane3_P
Lane2_N
Lane2_P
Lane1_N
Lane1_P
Lane0_N
Lane0_P
AUX_CH_P
AUX_CH_N
VDD
LCD_GND
HPD
BL_GND
BL_ENABLE
BL_PWM_DIM
VBL
shell
chg to 0201
RP65W_V01_20160922J
eDP_TXN3_C
eDP_TXP3_C
eDP_TXN2_C
eDP_TXP2_C
eDP_TXN1_C
eDP_TXP1_C
eDP_TXN0_C
eDP_TXP0_C
eDP_AUXP_C
eDP_AUXN_C
C2175
C2176
C2173
C2174
C2169
C2166
C2172
C2170
C2167
C2171
0.1u/2/X5R/6.3V/K
eDP_TXN3
eDP_TXP3
eDP_TXN2
eDP_TXP2
eDP_TXN1
eDP_TXP1
eDP_TXN0
eDP_TXP0
eDP_AUXP
eDP_AUXN
Panel_VCC3
eDP_HPD 18
BL_EN
BL_PWM
V33_BADGE_LED_R
GND_BADGE_LED
BL_PWR
R71174 0/4
30mil width
V33_BADGE_LED
C396 10u/4/X5R/6.3V/M
C2353 15u/TP/25V/B/100m
3.3V / 20mA=165 ohm
3.3V / 180 ohm=18mA
Panel_VCC3
R71217 4.99/6/1
SB 0122
Q7128
EDP_VDD_EN-
QN7002/SOT23/20pF/2
+V3.3A_EC
30mil width
PWR_init
Q99
AP2304GN/SOT23/110pF/117m
R905 150K/4
Q96
QN7002/SOT23/20pF/2
MOSFET 2.7A AP2304GN
APEC
$0.03
MOSFET 0.2A QN7002B-T1B-AT
NEC
$0.0065
PWRLED-_BTNBOARD 19,40
+V3.3A_EDP
改
RP65W_V01_20160922J
R71218 0/8
Follow RP57,
PANEL_VDD 電路, 讓T11 符合 SPEC
Layout
RX5 Panasonic 4Lane eDP
3.3V 1.4A Max
Trace width MUST 2
LQ140Z1JW01=>IDD= 880mA (Max) ; 508mA (Typ)
+V3.3A
+V3.3S
R71214 0/8/X
R1741 0/8/X
PVCC3
Q630
P6402FMG/SOT23/950pF/64m
Panel_VCC3
R1744 100K/4
C2152 0.1u/6/X7R/25V/K
chg X7R
RP65W_V01_20160922J
C2153 10u/6/X5R/6.3V/M
C2154 10u/6/X5R/6.3V/M
C8008 0.1u/4/X7R/25V/K
C8009 0.01u/4/X7R/25V/K
SA 1220
EDP_VDD_EN-
R1746 470K/4/1
Q631
QN7002/SOT23/20pF/2
15 EDP_VDD_EN_PCH
R1745 100K/4
+VBATA
del 0/8
RP65W_V01_20160922J
Q632
BL_PWR
R71263 220K/4/1
C2165 1u/6/X7R/50V/K
EMB50P03J/SOT23/820pF/50m
R1751 100K/4
R1752 220K/4/1
+V3.3S
R1753 47K/4
Q633
QN7002/SOT23/20pF/2
C2168 1u/4/X5R/10V/K
+V3.3S
C1662 0.1u/4/X5R/10V/K
U40
DNP
PCH 15 EDP_BKLT_EN_PCH
EC 19 EC_BKLTEN
BL_EN
SN74AHC1G08DBVR/SOT-23-5
PCH 15 EDP_BKLT_CTRL_PCH
FB27 100/6/3A/S
BL_PWM
C516 100p/4/NPO/50V/J
SB 0122
add
RP65W_V01_20160922J
1A
+V5A
Origin is follow P34 to FIX eDP panel cable power drop & display noise issue, to add external power. X17_V02_20130904J
Trace width MUST 2
+V3.3A_EDP
U30
VIN
BST
EN/SYNC
SW
VCC
FB
AAM
GND
MP2314GJ-Z/TSOT23-8
R573 499K/4/1
CL29 4.7u/6/X5R/6.3V/K C0603
PENEL_VDD_EN
C663 0.1u/4/X5R/10V/K
R580 0/4/X
C669 0.1u/4/X5R/10V/K
R590 75K/4/1 20170117
R582 20/4/1
C665 0.1u/4/X5R/16V/K
L12 4.7uH/2.6A/S/95m 20170117
C664 22p/4/NPO/50V/J
R583 33K/4/1
R589 40.2K/4/1 20170117
R584 11.3K/4/1 20170117
C666 0.1u/4/X5R/10V/K
CL30 22u/6/X5R/6.3V/M C0603
CL31 22u/6/X5R/6.3V/M C0603
Layout
**** eDP Layout for 更快速度更大頻寬：P34, RX5, RX4參考
1. GND 層的 noise 導致 eDP 閃爍==> eDP Trace 的參考層一定要切 moat，目的讓 EDP 的 GND return path 隔離來源，moat 可讓 return path 只 for eDP。
2. eDP Trace 要 guard GND。讓 EDP 隔開臨邊 noise。
GIGABYTE
GIGABYTE TECHNOLOGY COPORATION
Title
eDP
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5 4 3 2 1

D C B A

GIGABYTE

	GIGABYTE TECHNOLOGY COPORATION
Title	**PCH_5-PWR**
Size	Document Number **GA-RP65X8** Rev **1.0**
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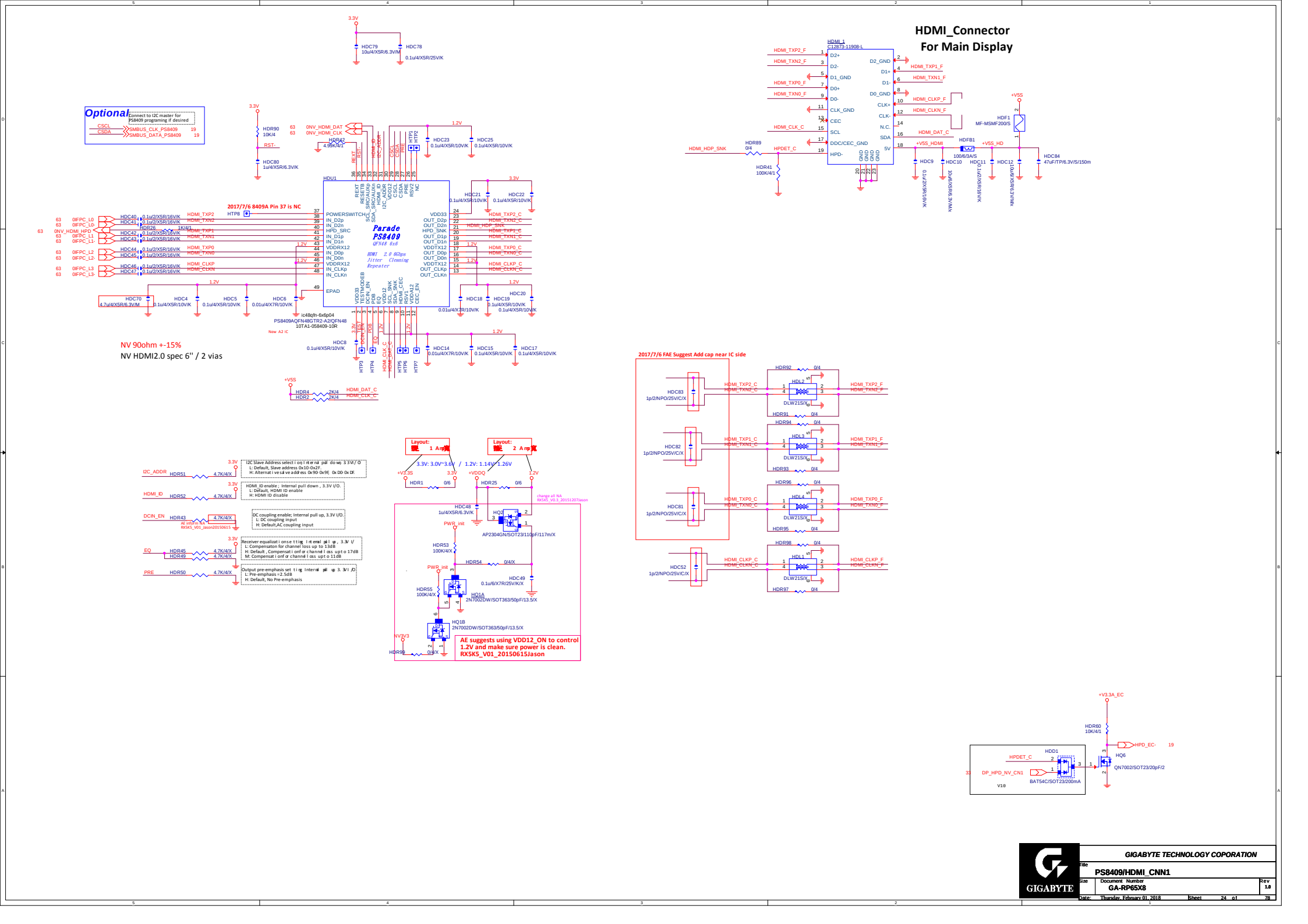
HDMI_Connector
For Main Display
Optional
Connect to I2C master for PS8409 programing if desired
CSCL
CSDA
SMBUS_CLK_PS8409
SMBUS_DATA_PS8409
Parade
PS8409
QFN48 8x8
HDMI 2.0 6Gbps
Jitter Cleaning
Repeater
2017/7/6 8409A Pin 37 is NC
NV 90ohm +-15%
NV HDMI2.0 spec 6'' / 2 vias
2017/7/6 FAE Suggest Add cap near IC side
Layout: 1 Amp
Layout: 2 Amp
3.3V: 3.0V~3.6V / 1.2V: 1.14V~1.26V
AE suggests using VDD12_ON to control 1.2V and make sure power is clean.
RX5K5_V01_20150615Jason
GIGABYTE TECHNOLOGY COPORATION
PS8409/HDMI_CNN1
GA-RP65X8
Rev 1.0
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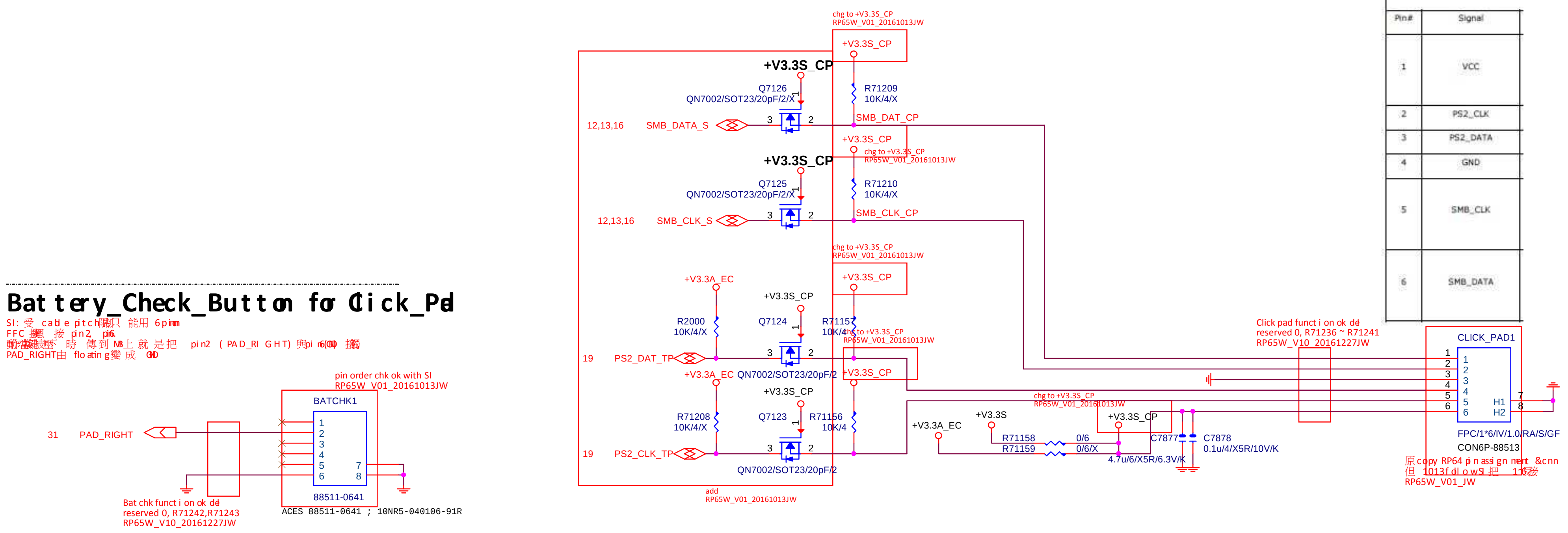
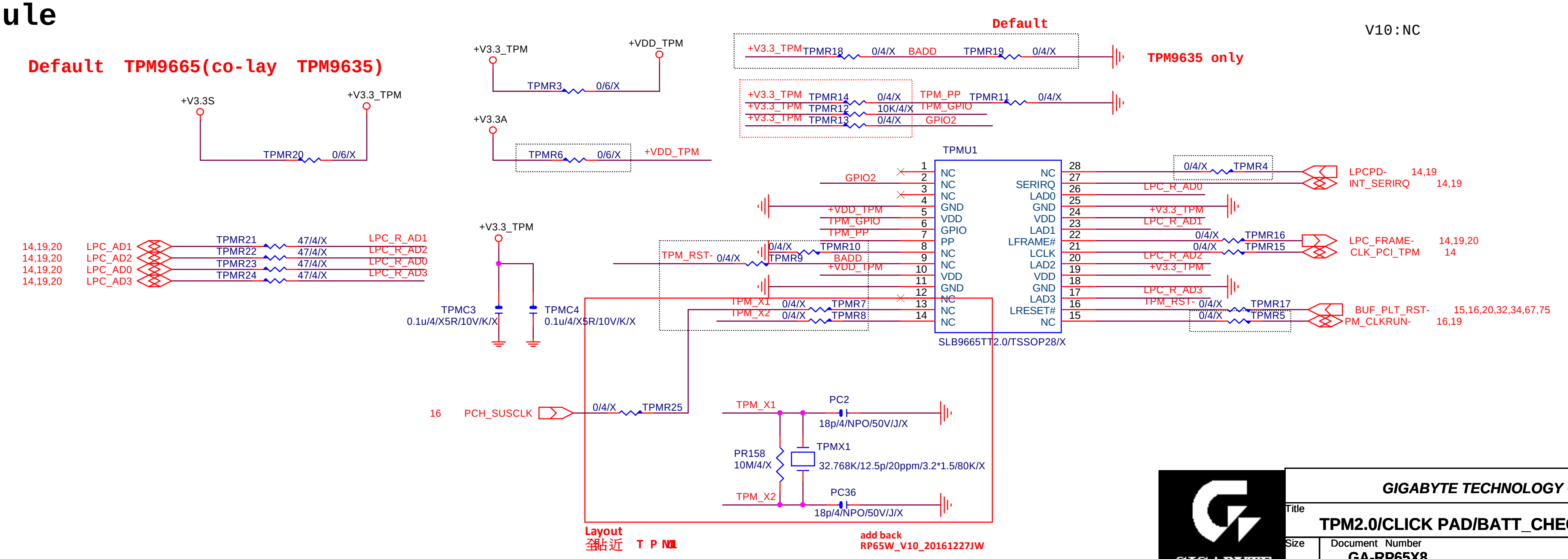
Click Pad

SA469A-32H2 Pin Assignment

Pin#	Signal
1	VCC
2	PS2_CLK
3	PS2_DATA
4	GND
5	SMB_CLK
6	SMB_DATA



TPM Module



GIGABYTE TECHNOLOGY COPORATION

Title: TPM2.0/CLICK PAD/BATT_CHECK

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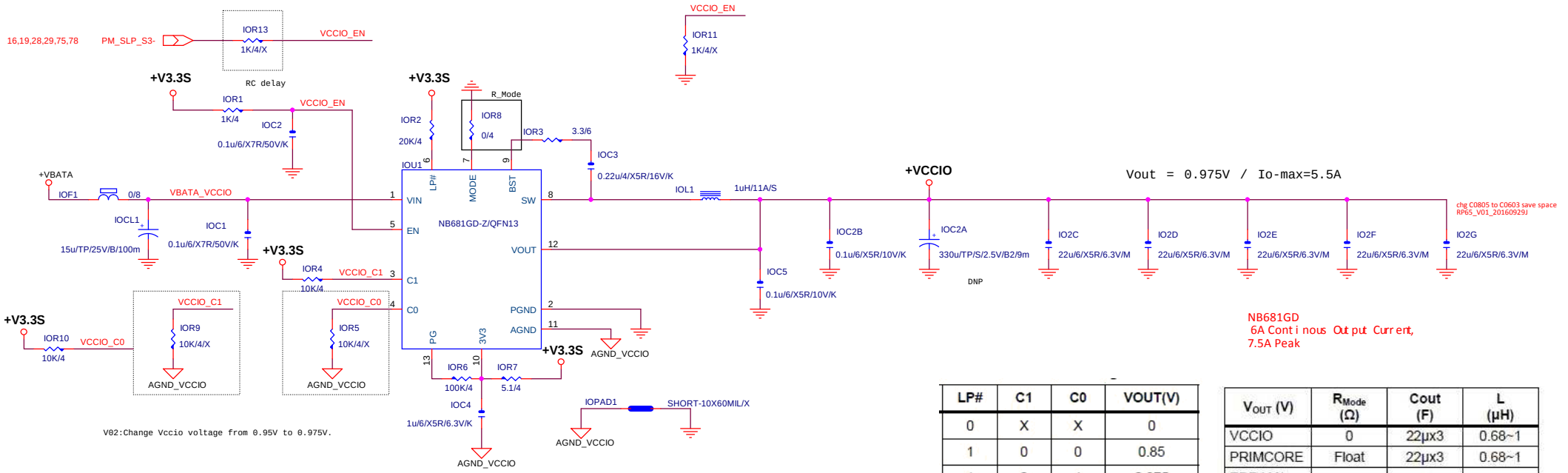
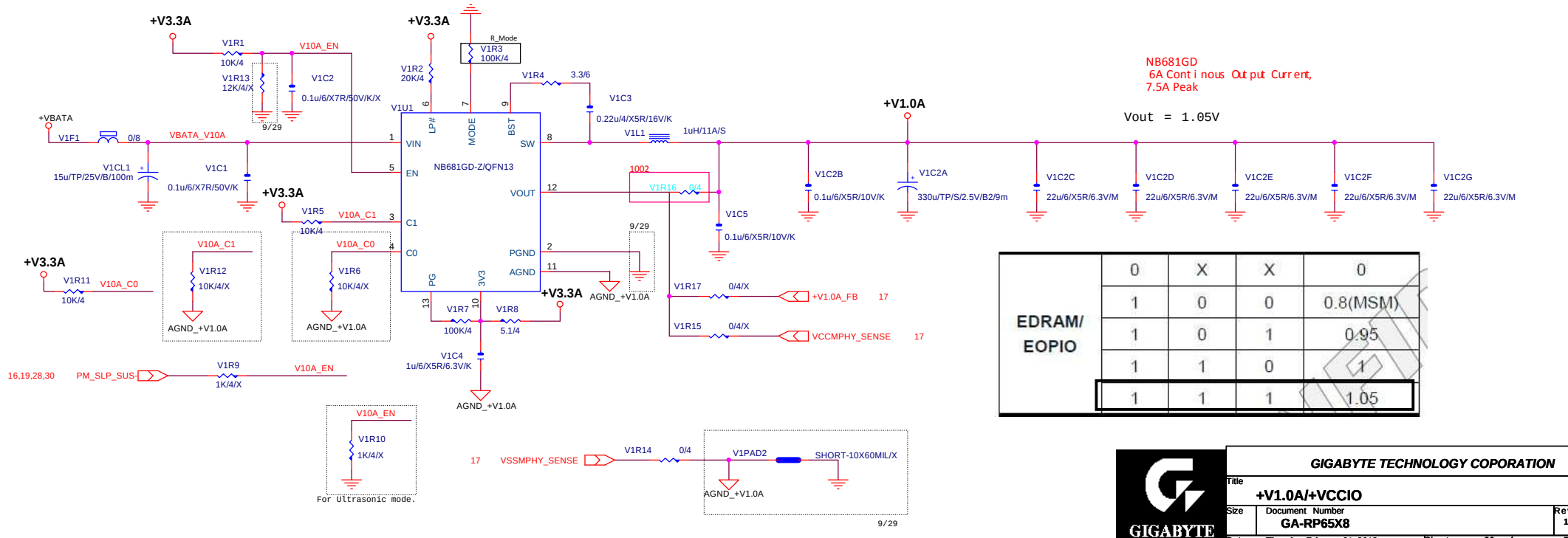


LP#	C1	C0	VOUT(V)
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975

V_{OUT} (V)	R_{Mode} (Ω)	Cout (F)	L (μH)
VCCIO	0	22μx3	0.68~1
PRIMCORE	Float	22μx3	0.68~1
EDRAM/ EOPIO/ V1.0A	100K	22μx3	0.68~1
Other	150K	22μx3	0.68~1



EDRAM/ EOPIO	0	X	X	0
	1	0	0	0.8(MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05

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Title: +V1.0A/+VCCIO

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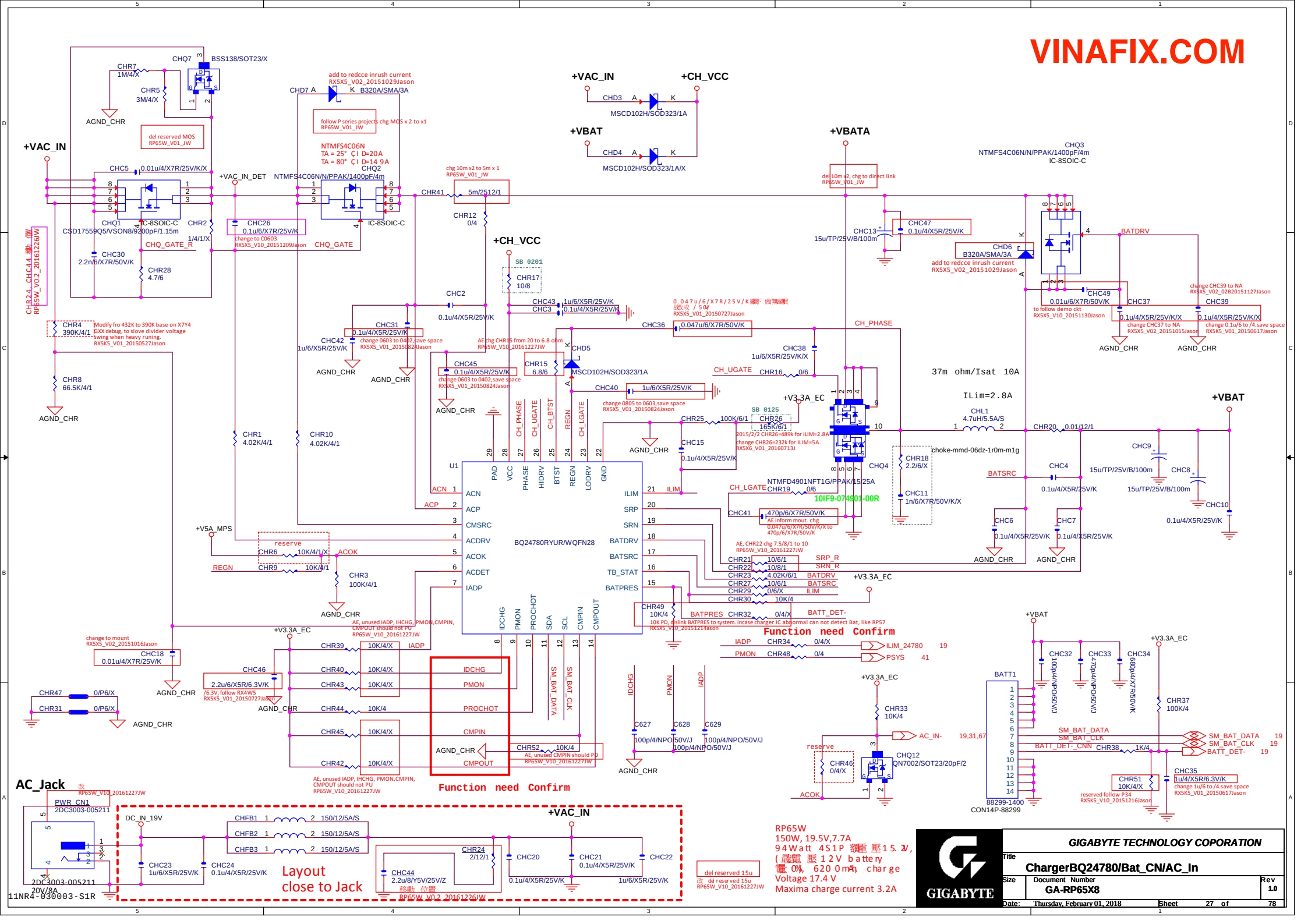
+VAC_IN
+CH_VCC
+VBAT
+VBATA
+V3.3A_EC
+V5A_MPS
AGND_CHR
BQ24780RYUR/WQFN28
Function need Confirm
AC_Jack
PWR_CN1
2DC3003-005211
DC_IN_19V
Layout close to Jack
RP65W
150W, 19.5V,7.7A
94Watt 4S1P 額電壓15.2V,
(讓電壓12V battery
電0%, 620 0mA charge
Voltage 17.4 V
Maxima charge current 3.2A
GIGABYTE TECHNOLOGY COPORATION
ChargerBQ24780/Bat_CN/AC_In
GA-RP65X8
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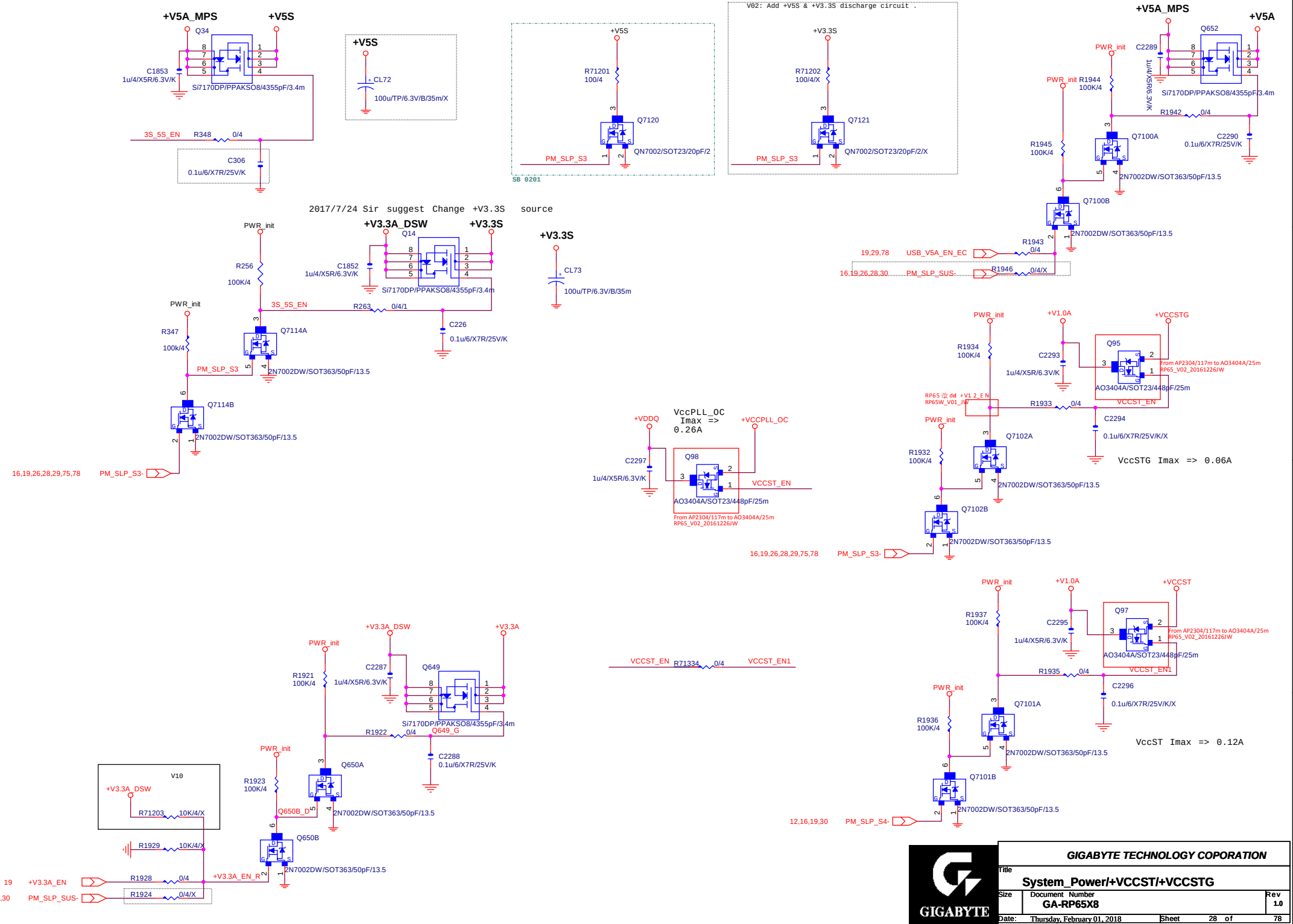
+V5A_MPS
+V5S
Q34
C1853
1u/4/X5R/6.3V/K
Si7170DP/PPAKSO8/4355pF/3.4m
3S_5S_EN
R348
0/4
C306
0.1u/6/X7R/25V/K
+V5S
CL72
100u/TP/6.3V/B/35m/X
+V5S
R71201
100/4
Q7120
PM_SLP_S3
QN7002/SOT23/20pF/2
SB 0201
V02: Add +V5S & +V3.3S discharge circuit .
+V3.3S
R71202
100/4/X
Q7121
PM_SLP_S3
QN7002/SOT23/20pF/2/X
+V5A_MPS
+V5A
Q652
PWR_init
C2289
1u/4/X5R/6.3V/K
Si7170DP/PPAKSO8/4355pF/3.4m
R1944
100K/4
R1942
0/4
R1945
100K/4
Q7100A
C2290
0.1u/6/X7R/25V/K
2N7002DW/SOT363/50pF/13.5
Q7100B
2N7002DW/SOT363/50pF/13.5
19,29,78
USB_V5A_EN_EC
R1943
0/4
16,19,26,28,30
PM_SLP_SUS-
R1946
0/4/X
2017/7/24 Sir suggest Change +V3.3S source
PWR_init
+V3.3A_DSW
+V3.3S
Q14
C1852
1u/4/X5R/6.3V/K
Si7170DP/PPAKSO8/4355pF/3.4m
R256
100K/4
3S_5S_EN
R263
0/4/1
C226
0.1u/6/X7R/25V/K
+V3.3S
CL73
100u/TP/6.3V/B/35m
PWR_init
R347
100k/4
Q7114A
PM_SLP_S3
2N7002DW/SOT363/50pF/13.5
Q7114B
2N7002DW/SOT363/50pF/13.5
16,19,26,28,29,75,78
PM_SLP_S3-
+VDDQ
VccPLL_OC
Imax =>
0.26A
+VCCPLL_OC
C2297
1u/4/X5R/6.3V/K
Q98
VCCST_EN
AO3404A/SOT23/448pF/25m
From AP2304/117m to AO3404A/25m
RP65_V02_20161226JW
PWR_init
+V1.0A
+VCCSTG
R1934
100K/4
C2293
1u/4/X5R/6.3V/K
Q95
From AP2304/117m to AO3404A/25m
RP65_V02_20161226JW
AO3404A/SOT23/448pF/25m
RP65 改 del +V1_2_EN
RP65W_V01_JW
R1933
0/4
VCCST_EN
C2294
0.1u/6/X7R/25V/K/X
PWR_init
R1932
100K/4
Q7102A
2N7002DW/SOT363/50pF/13.5
Q7102B
2N7002DW/SOT363/50pF/13.5
16,19,26,28,29,75,78
PM_SLP_S3-
VccSTG Imax => 0.06A
+V3.3A_DSW
+V3.3A
PWR_init
R1921
100K/4
C2287
1u/4/X5R/6.3V/K
Q649
Si7170DP/PPAKSO8/4355pF/3.4m
R1922
0/4
Q649_G
C2288
0.1u/6/X7R/25V/K
PWR_init
R1923
100K/4
Q650A
Q650B_D
2N7002DW/SOT363/50pF/13.5
Q650B
2N7002DW/SOT363/50pF/13.5
V10
+V3.3A_DSW
R71203
10K/4/X
R1929
10K/4/X
19
+V3.3A_EN
R1928
0/4
+V3.3A_EN_R
16,19,26,28,30
PM_SLP_SUS-
R1924
0/4/X
VCCST_EN
R71334
0/4
VCCST_EN1
PWR_init
+V1.0A
+VCCST
R1937
100K/4
C2295
1u/4/X5R/6.3V/K
Q97
From AP2304/117m to AO3404A/25m
RP65_V02_20161226JW
AO3404A/SOT23/448pF/25m
R1935
0/4
VCCST_EN1
C2296
0.1u/6/X7R/25V/K/X
PWR_init
R1936
100K/4
Q7101A
2N7002DW/SOT363/50pF/13.5
Q7101B
2N7002DW/SOT363/50pF/13.5
12,16,19,30
PM_SLP_S4-
VccST Imax => 0.12A
GIGABYTE
GIGABYTE TECHNOLOGY COPORATION
Title
System_Power/+VCCST/+VCCSTG
Size
Document Number
GA-RP65X8
Rev
1.0
Date:
Thursday, February 01, 2018
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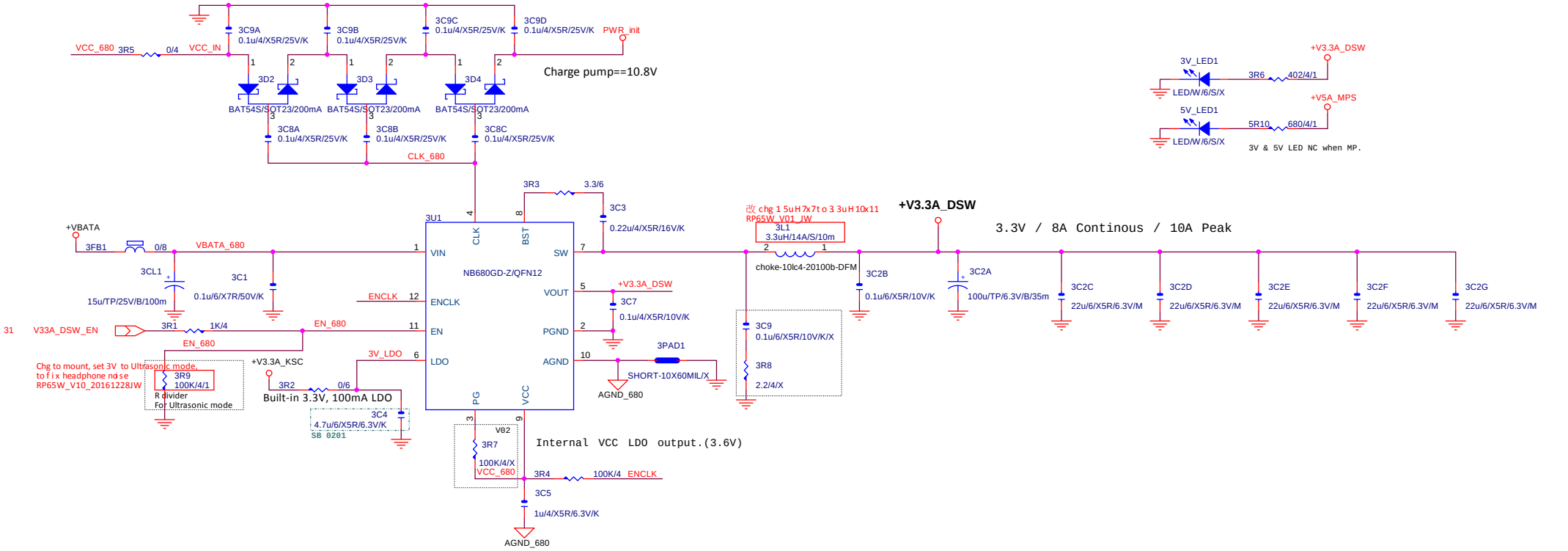
28
of
78



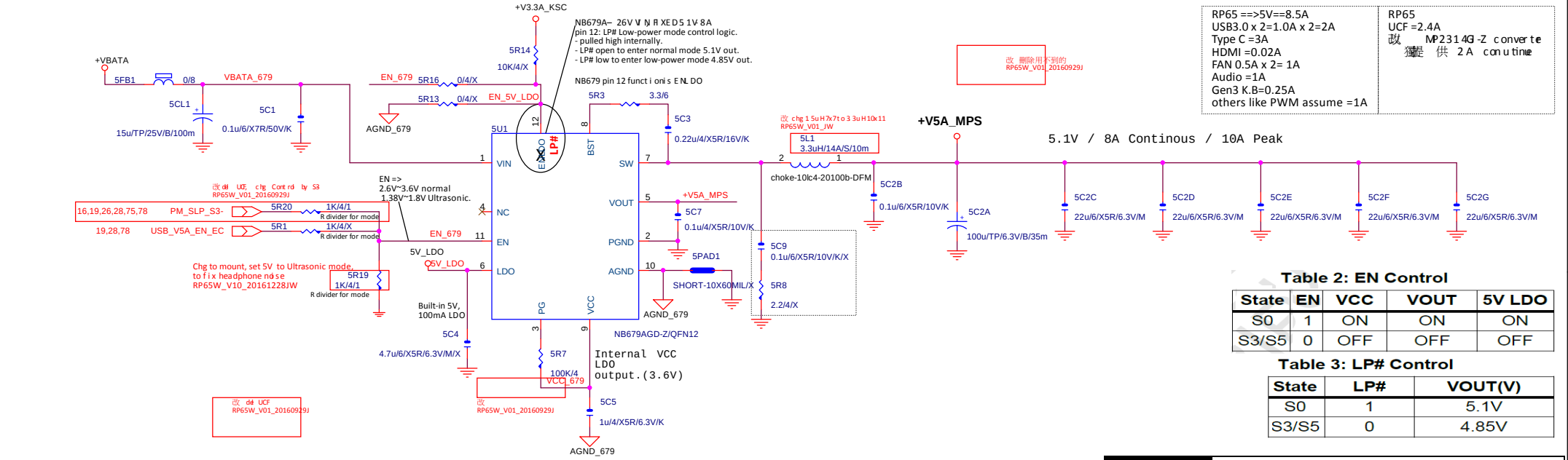


Table 2: EN Control

State	EN	VCC	VOUT	5V LDO
S0	1	ON	ON	ON
S3/S5	0	OFF	OFF	OFF

Table 3: LP# Control

State	LP#	VOUT(V)
S0	1	5.1V
S3/S5	0	4.85V

GIGABYTE TECHNOLOGY COPORATION

Title: +V3.3A_DSW/+V5A_MPS

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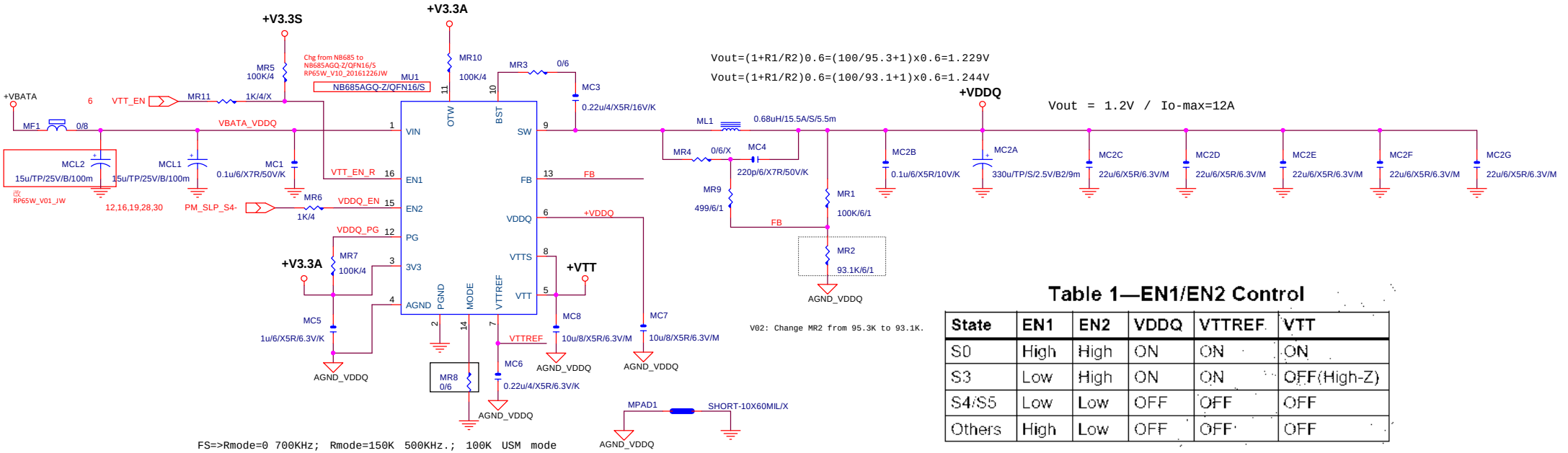


Vout=(1+R1/R2)0.6=(100/95.3+1)x0.6=1.229V

Vout=(1+R1/R2)0.6=(100/93.1+1)x0.6=1.244V

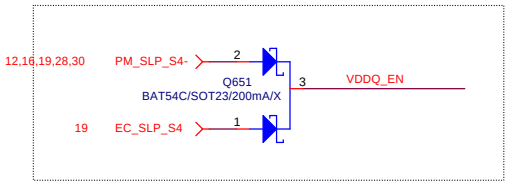
Vout = 1.2V / Io-max=12A

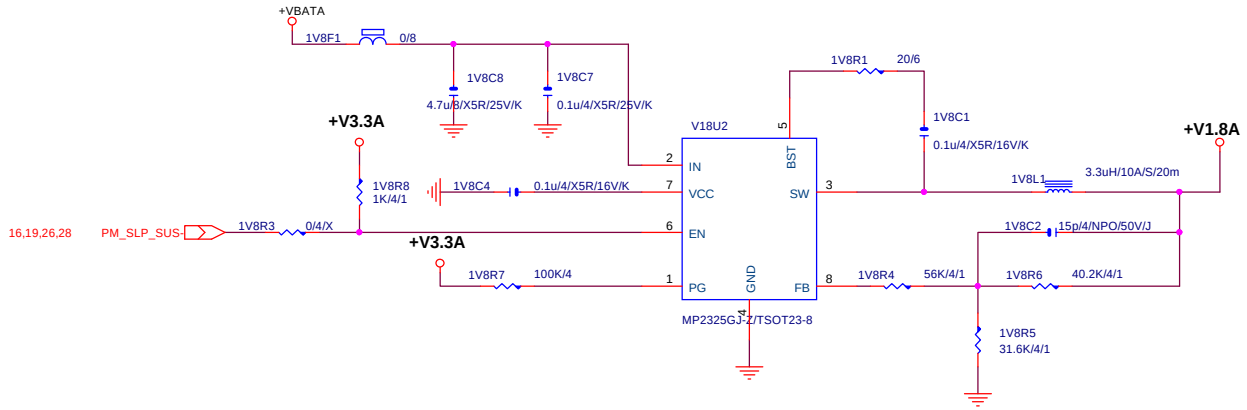
V02: Change MR2 from 95.3K to 93.1K.

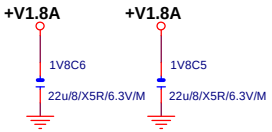
FS=>Rmode=0 700KHz; Rmode=150K 500KHz.; 100K USM mode

Table 1—EN1/EN2 Control

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF







GIGABYTE TECHNOLOGY COPORATION

Title: +VDDQ/+VTT

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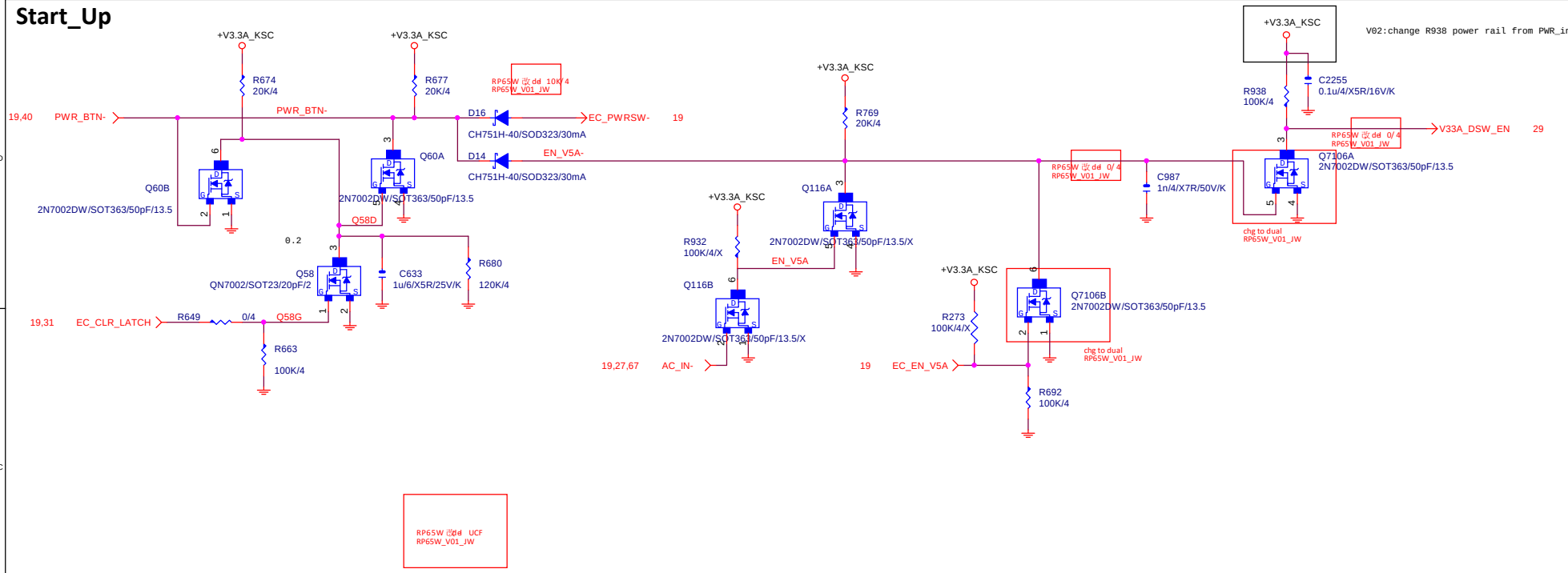
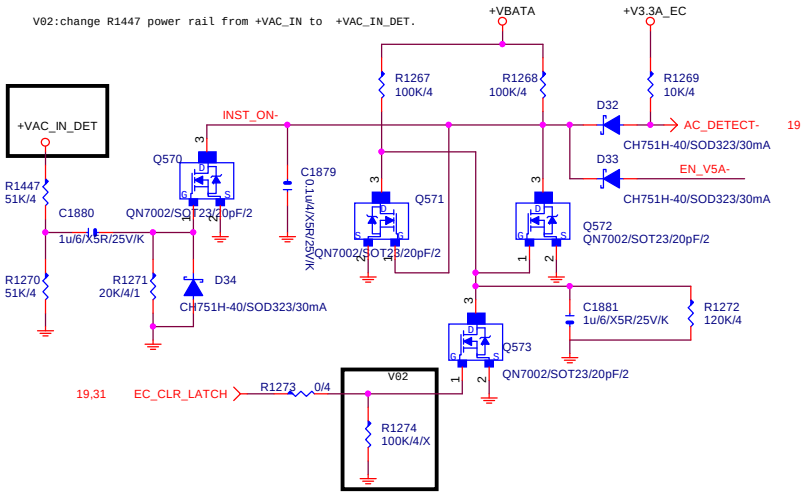
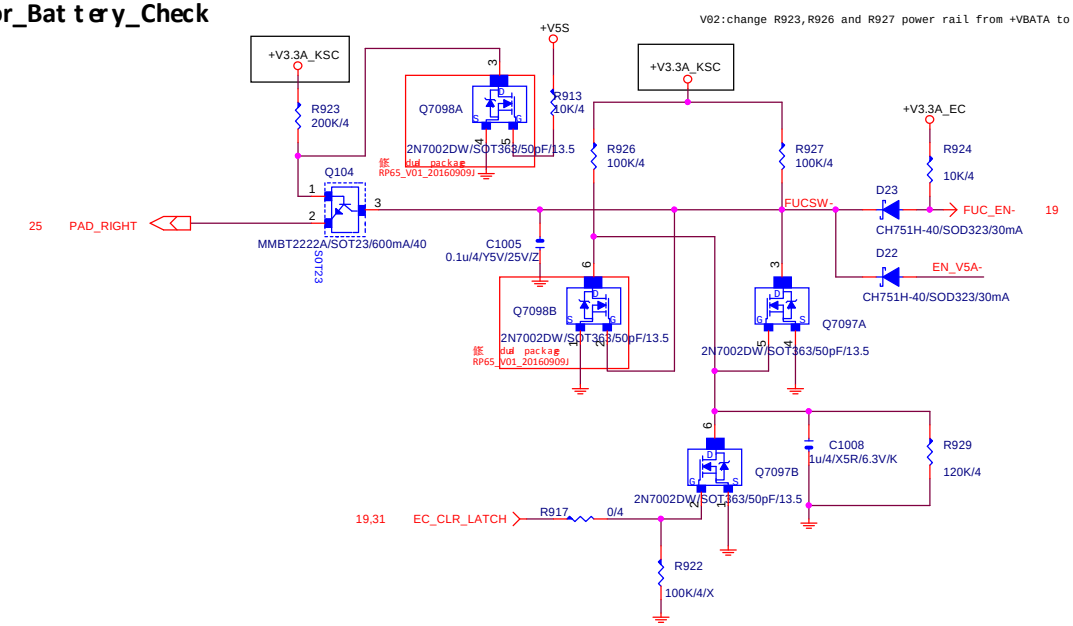
Start_Up



AC_Plug_to_wake_up_EC_from_0.5Wat t_St at us



For_Bat t ery_Check



GIGABYTE	GIGABYTE TECHNOLOGY COPORATION		
	Title: Start_Up/Latch		
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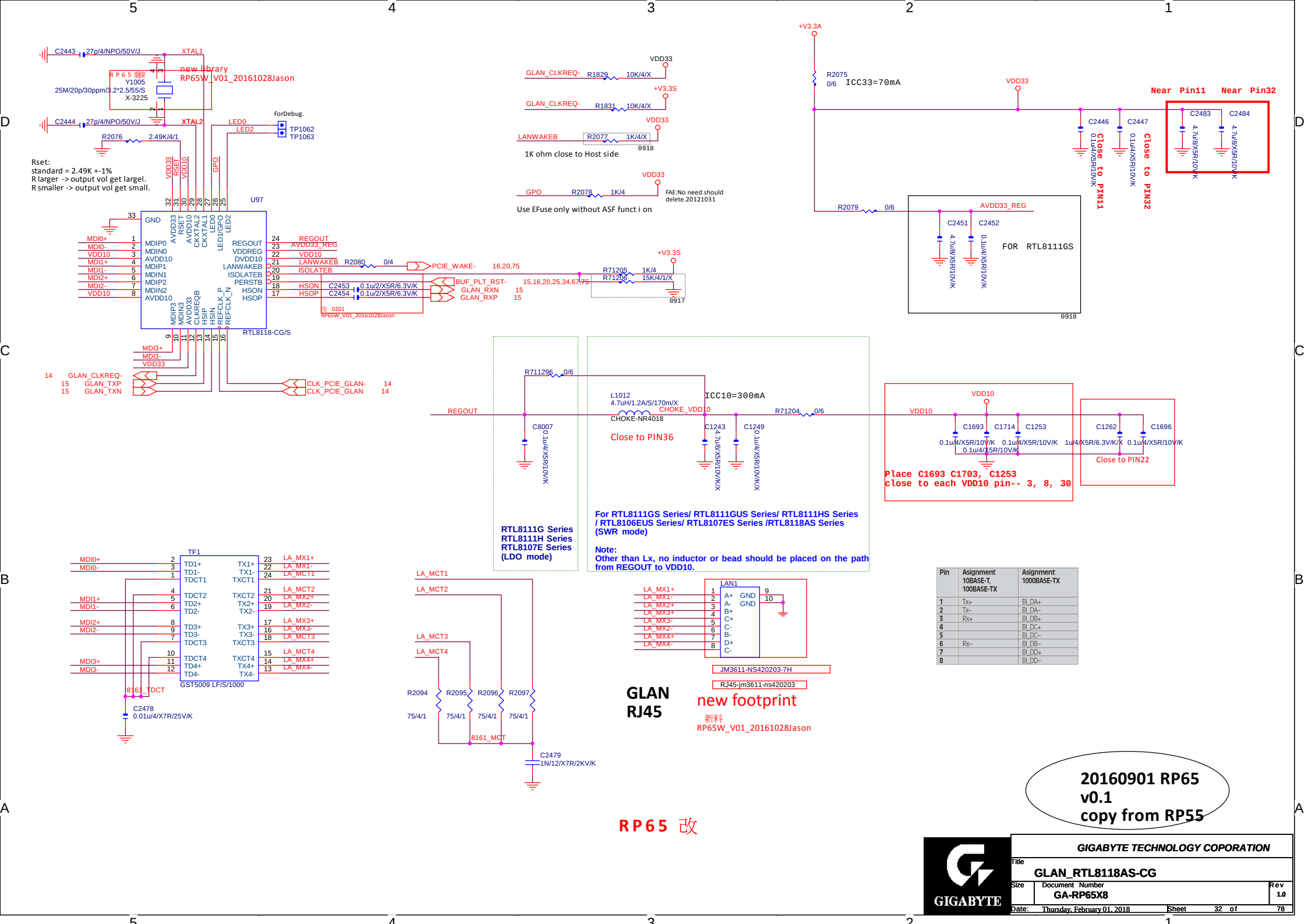

Pin	Asignment 10BASE-T, 100BASE-TX	Asignment 1000BASE-TX
1	Tx+	BI_DA+
2	Tx-	BI_DA-
3	Rx+	BI_DB+
4		BI_DC+
5		BI_DC-
6	Rx-	BI_DB-
7		BI_DD+
8		BI_DD-

GIGABYTE TECHNOLOGY COPORATION

Title: GLAN_RTL8118AS-CG

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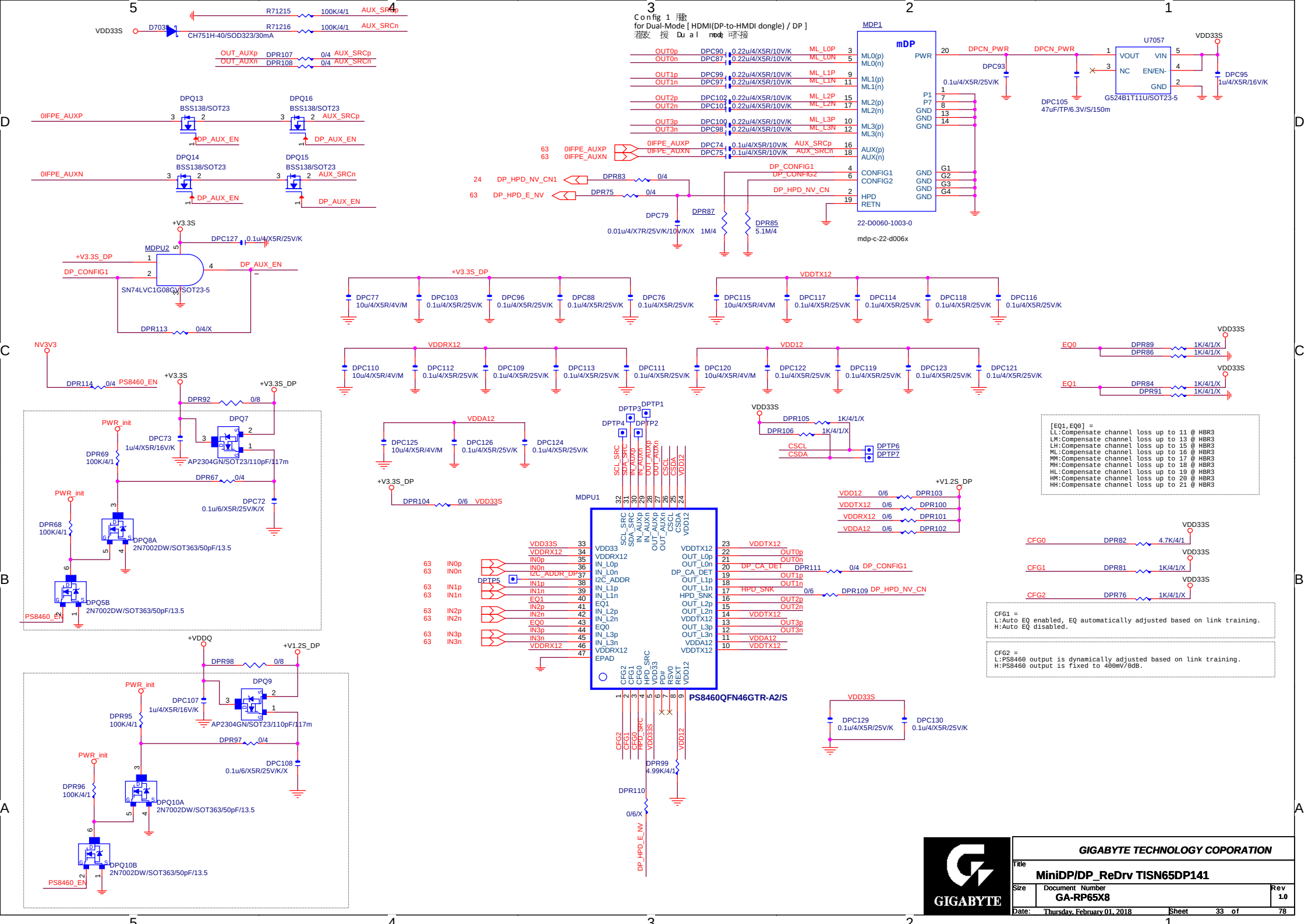
Date: Thursday, February 01, 2018 | Sheet 32 of 78



GIGABYTE TECHNOLOGY COPORATION	
Title	MiniDP/DP_ReDrv TISN65DP141
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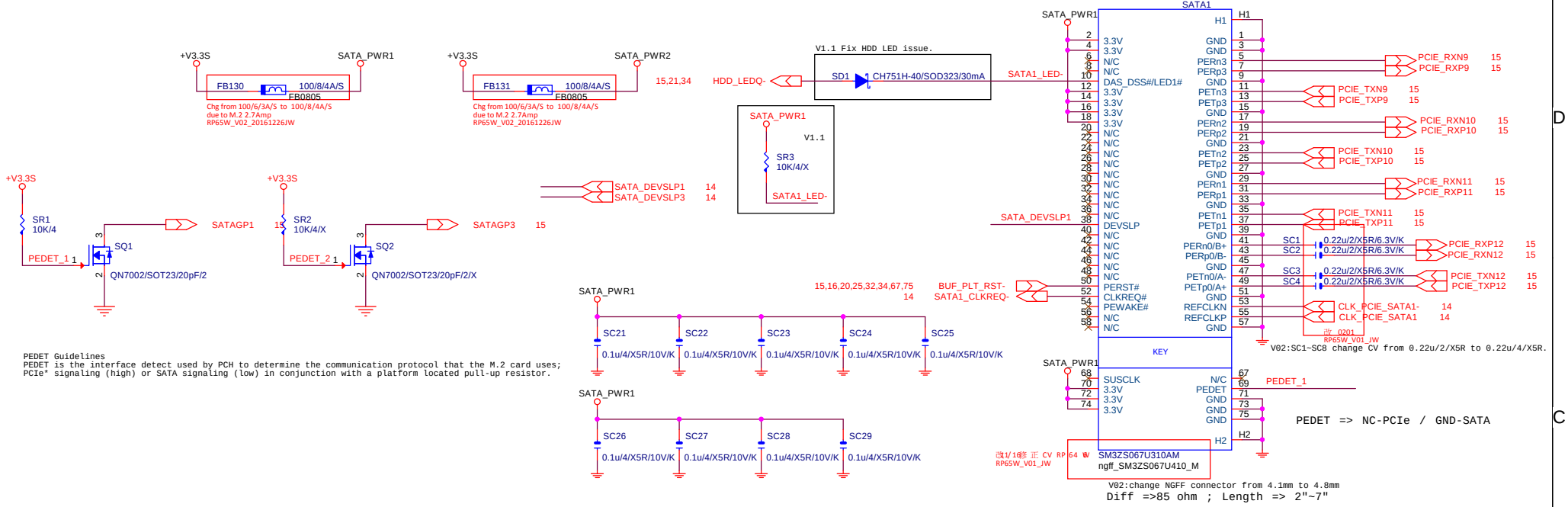
Place PCIe TX AC caps closer to the PCIe* connector.



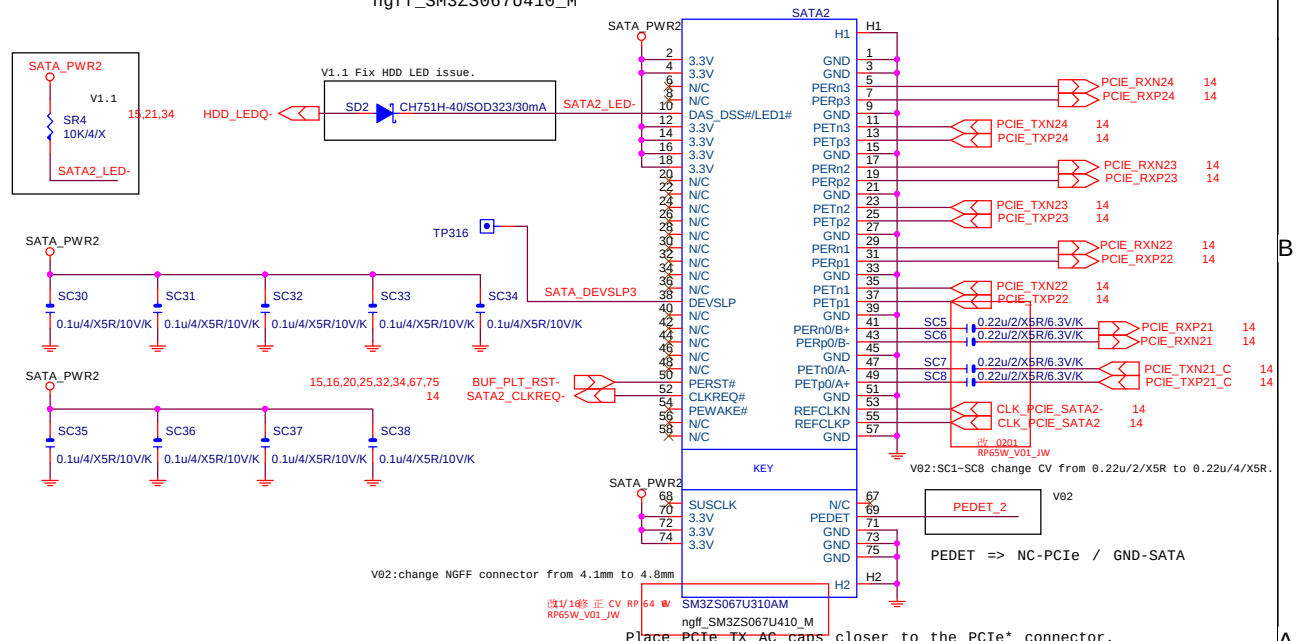
V02:SC1~SC8 change CV from 0.22u/2/X5R to 0.22u/4/X5R.

PEDET => NC-PCIe / GND-SATA

Diff =>85 ohm ; Length => 2"~7"

PEDET Guidelines
PEDET is the interface detect used by PCH to determine the communication protocol that the M.2 card uses; PCIe* signaling (high) or SATA signaling (low) in conjunction with a platform located pull-up resistor.

ngff_SM3ZS067U410_M



V02:SC1~SC8 change CV from 0.22u/2/X5R to 0.22u/4/X5R.

PEDET => NC-PCIe / GND-SATA

Place PCIe TX AC caps closer to the PCIe* connector.

SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

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Title: NGFF (Socket 3)

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Analog
Digital

+V1.5S_AZ

1.5V(Or 1.8V) power rail should be supplied by linear regulator, not switching regulator. if switching regulator is unavoidable, Please make sure that switching frequency operates at out- band(Over 20KHz).

+V5S_PVDD

Add this Filter to avoid other components/chips be influenced

Follow Follow P35,chg to 47uF x2 to filter power noise. RP65W_V02_20161226JW

Follow X5K6 add to filter power noise. RP65W_V02_20161226JW

HPOUT-R
HPOUT-L
MIC2_VREF0

100K is used to speed up the discharge for LDO1. It could solve the pop sound during system boot up and reboot.

Place close to Pin 26

+V5S_AUD

C4 = 10uF for Desktop Applicaiton
C4 = 2.2uF for Laptop Application

REALTEK
ALC255-CG/QFN48/S
(Include Thermal pad)
QFN48 (6x6)

place close audio codec

Analog
Digital

Grounding circuit for combo jack SLEEVE pin

Coin battery is all et osd vet he background noise when system is at S3/S4/S5 and G3.

RESERVED THIS CIRCUIT
ALC255 has already integrated this grounding circuit inside the pin20

R1.1 20130711 ENZO
Fix Audio signal quality fail issue

af ter debug chg 0.01u/4/X7R/25V/K to 0 to reduce headphone noise RP65W_V02_20161226JW

Follow P34, chg to 0 to fix headphone noise RP65W_V02_20161226JW

PD# Control Method 1
(Only for 3.3V HDA-LINK)

If HD_RESET# high level is 1.5V
(The signal level of HDA_Link are 1.5V) , please follow "PD# Control Method 2" circuit.

<<Attention>>
For power on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on , please let EC_MUTE# High.
2. If your design want to system make warning signal, for example No CPU or Memory installation or Bad BIOS, please change to OR Gate or contact our local FAEs for more details about the control circuit

Place close to pin 1

DMIC interface

Place close to pin 9

Demodulation Filter Placement near Audio Codec

AME8800LEETZ/SOT23/0.3A

copy from RP64

Speaker => 4 OHM / 2W

GIGABYTE TECHNOLOGY COPORATION	
Title: ALC255 Universal Jack	
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GIGABYTE TECHNOLOGY COPORATION

Title: empty_____

Size | Document Number: GA-RP65X8 | Rev: 1.0

Date: Thursday, February 01, 2018 | Sheet 36 of 78

GIGABYTE TECHNOLOGY COPORATION

Title: empty_____

Size | Document Number: GA-RP65X8 | Rev: 1.0

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USB_Connector

For Gen4 Keyboard

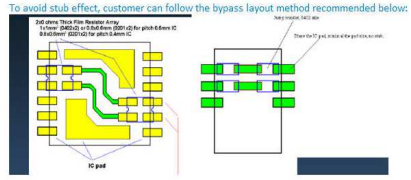
40 mils

85ohm

10TA1-080524-10R

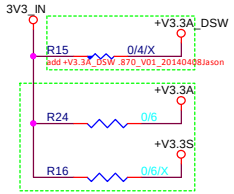
改
RP65W_V01_2016JW

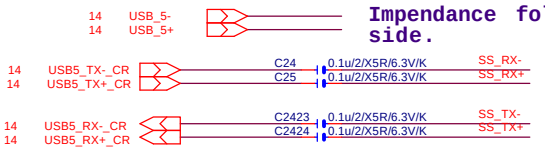
FOR CO-LAY



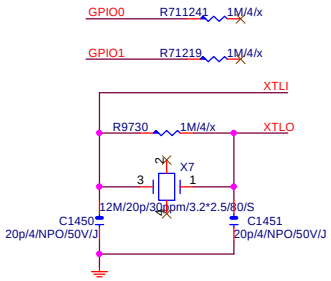
GIGABYTE TECHNOLOGY COPORATION	
Title	USB3.0x3/Gen4_KB
Size	Document Number: GA-RP65X8 — Rev: 1.0
Date: Thursday, February 01, 2018	Sheet 38 of 78

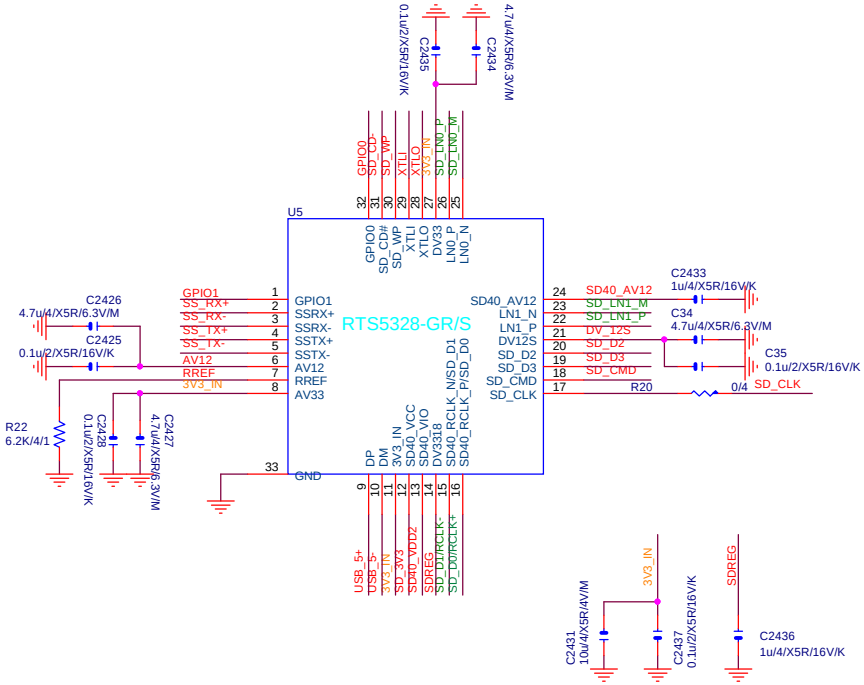
From System's USB3.0 interface

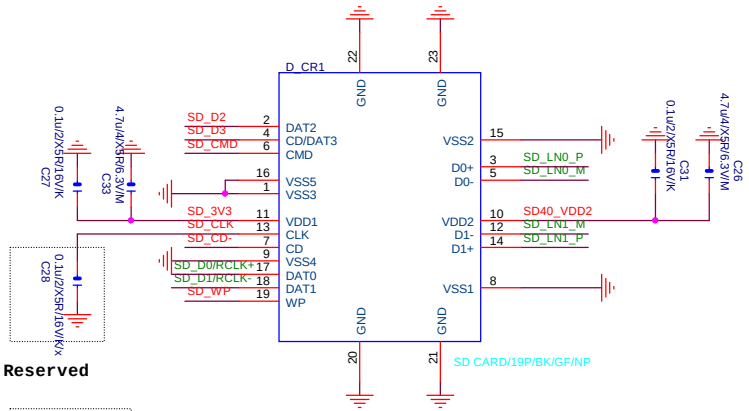




Impendance folllowed as source side.







Reserved

SD_D0/RCLK+
SD_D1/RCLK-

Differentail air 100 ohm

SD_LN0_P
SD_LN0_M
SD_LN1_P
SD_LN1_M

Differentail air 100 ohm

SD UHS-I/UHS-II card socket

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Title: Card Reader		
Size: A3	Document Number: GA-RP65X8	Rev: 1.0
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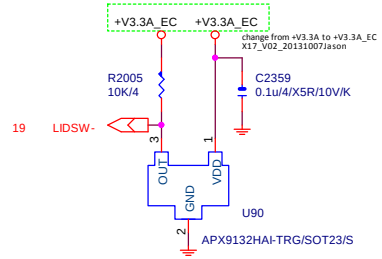
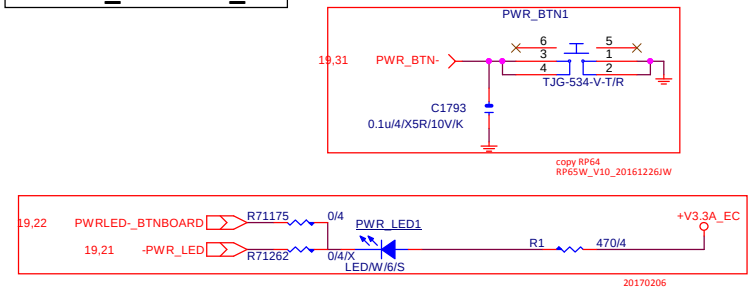
Hall Effect Micro Switch IC



Power_Button_SW



RP65 del touch pad
RP65W_V10_20161226JW

HOLE276_118 x 12

HS5 HOLE236_118/X
HS29 HOLE276_118/X
HS26 HOLE276_118/X
HS6 HOLE276_118/X
HS24 HOLE276_118/X
HS8 HOLE276_118/X
HS31 HOLE260_118/X
HS30 HOLE276_118/X
HS4 HOLE276_118/X
HS2 HOLE276_118/X
HS27 HOLE276_118/X
HS7 HOLE276_118/X

For M.2
M2.0 x H1.2mm stand of f
HS33
STD/INSIDE/D4H1.2M2
HOLE197_138TD

GPU
M2.0 x H1.2mm stand of f
HS43
STD/INSIDE/D4H1.2M2
HOLE197_138TD
HS44
STD/INSIDE/D4H1.2M2
HOLE197_138TD
HS45
STD/INSIDE/D4H1.2M2
HOLE197_138TD
HS46
STD/INSIDE/D4H1.2M2
HOLE197_138TD

For FAN
HS22
STD/INSIDE/D4H1.2M2
HOLE197_138TD
HS23
STD/INSIDE/D4H1.2M2
HOLE197_138TD
follow M.E. Chg from 1.0 to 1.2
RP65W_V10_20161226JW

PCB
PCB1
10PMRP65W-TX-S01L

For CPU
M2.0 x H1.2mm stand of f
HS37
STD/INSIDE/D4H1.2M2
HOLE197_138TD
follow M.E. Chg from 3.0 to 1.2
RP65W_V02_20161226JW
HS38
STD/INSIDE/D4H1.2M2
HOLE197_138TD
HS39
STD/INSIDE/D4H1.2M2
HOLE197_138TD
follow M.E. Chg from 3.0 to 1.2
RP65W_V02_20161226JW

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Title: Lid/PWRBTN/ScrewHole

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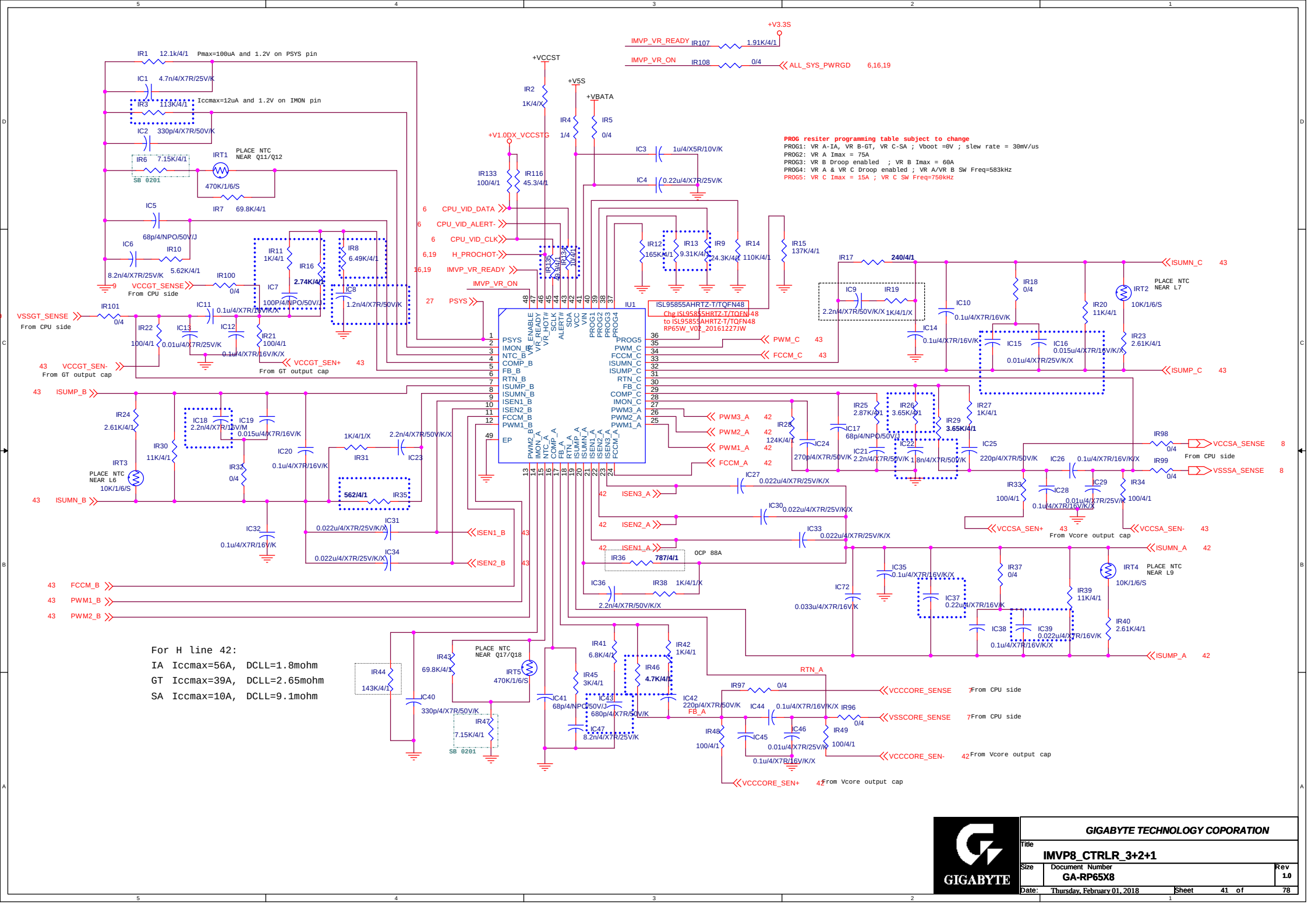
PROG resiter programming table subject to change
PROG1: VR A-IA, VR B-GT, VR C-SA ; Vboot =0V ; slew rate = 30mV/us
PROG2: VR A Imax = 75A
PROG3: VR B Droop enabled ; VR B Imax = 60A
PROG4: VR A & VR C Droop enabled ; VR A/VR B SW Freq=583kHz
PROG5: VR C Imax = 15A ; VR C SW Freq=750kHz
ISL95855AHRTZ-T/TQFN48
Chg ISL95855HRTZ-T/TQFN48
to ISL95855AHRTZ-T/TQFN48
RP65W_V02_20161227JW
Pmax=100uA and 1.2V on PSYS pin
Iccmax=12uA and 1.2V on IMON pin
PLACE NTC NEAR Q11/Q12
PLACE NTC NEAR L6
PLACE NTC NEAR L7
PLACE NTC NEAR L9
PLACE NTC NEAR Q17/Q18
OCP 88A
From CPU side
From GT output cap
From Vcore output cap
For H line 42:
IA Iccmax=56A, DCLL=1.8mohm
GT Iccmax=39A, DCLL=2.65mohm
SA Iccmax=10A, DCLL=9.1mohm
GIGABYTE TECHNOLOGY COPORATION
IMVP8_CTRLR_3+2+1
GA-RP65X8
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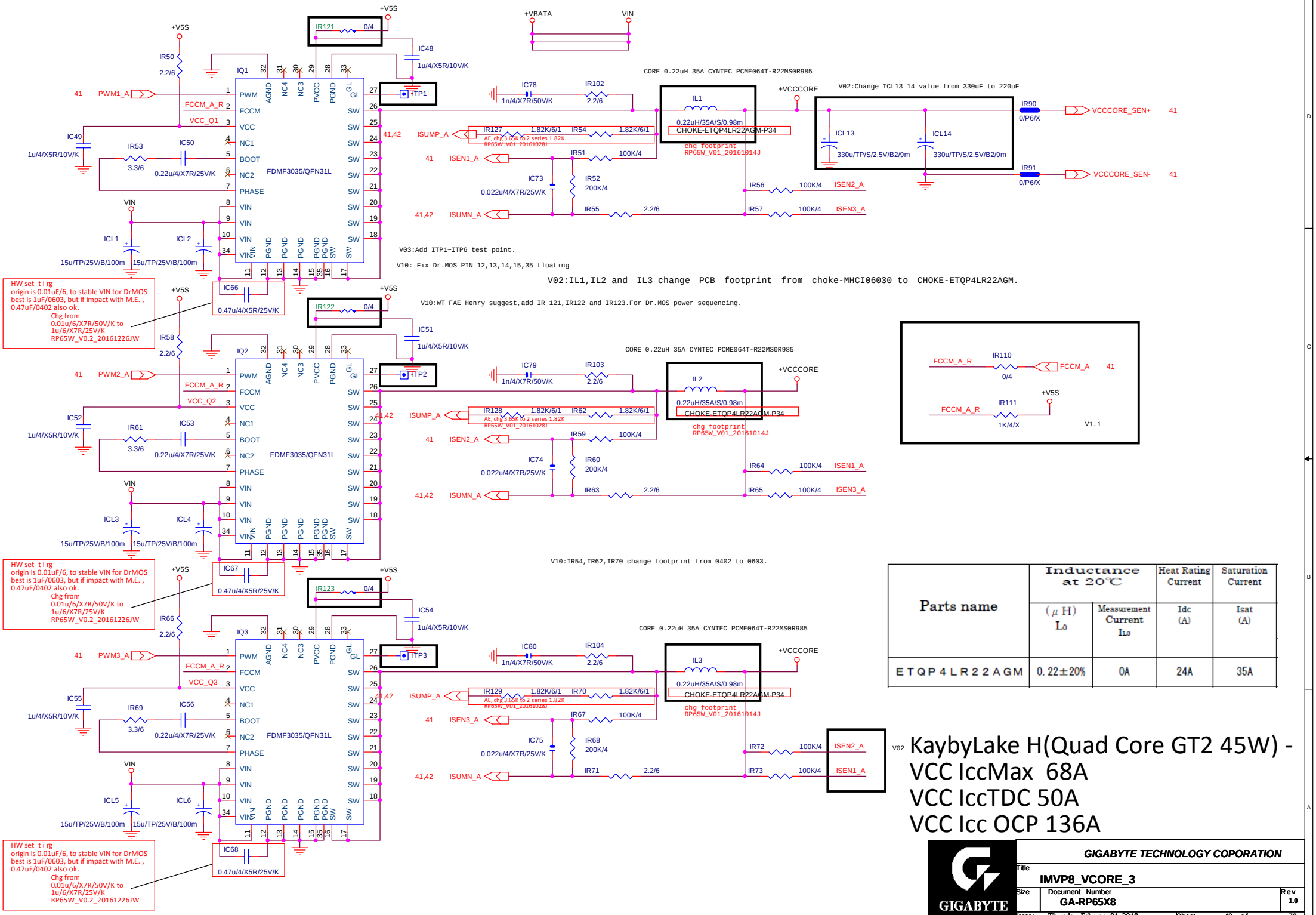

Parts name	Inductance at 20°C		Heat Rating Current	Saturation Current
	(μH) L_0	Measurement Current I_{L0}	Idc (A)	Isat (A)
ETQP4LR22AGM	0.22±20%	0A	24A	35A

V02 KaybyLake H(Quad Core GT2 45W) -
VCC IccMax 68A
VCC IccTDC 50A
VCC Icc OCP 136A

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Title	IMVP8_VCORE_3		
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KaybyLake H(Quad Core GT2 45W) - VCCGT IccMax 55A
IccTDC 25A
IccOCP 82.5A

V10:WT FAE Henry suggest,add IR 124,IR125 and IR126.For Dr.MOS power sequencing.

CORE 0.22uH 35A CYNTEC PCME064T-R22MS0R985

V02:Change ICL15 16 value from 330uF to 220uF

V10: Fix Dr.MOS PIN 12,13,14,15,35 floating

V02:IL4,IL5 and IL6 change PCB footprint from choke-MHCI06030 to CHOKE-ETQP4LR22AGM.

V10:IR88,IR84,IR76 change footprint from 0402 to 0603.

KaybyLake H(Quad Core GT2 45W) - VCCSA IccMax 11.1A
IccTDC 10A
IccOCP 16.65A

V02:Change ICL18 value from 220uF to 330uF ; ICL19 suf

HW set ting
origin is 0.01uF/6, to stable VIN for DrMOS
best is 1uF/0603, but if impact with M.E. ,
0.47uF/0402 also ok.
Chg from
0.01u/6/X7R/50V/K to
1u/6/X7R/25V/K
RP65W_V0.2_20161226JW

V1.1

GIGABYTE TECHNOLOGY COPORATION

Title	IMVP8_VGT_VSA_2+1	
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GIGABYTE TECHNOLOGY COPORATION

Title: empty_____

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GIGABYTE TECHNOLOGY COPORATION

Title: empty_____

Size | Document Number: GA-RP65X8 | Rev: 1.0

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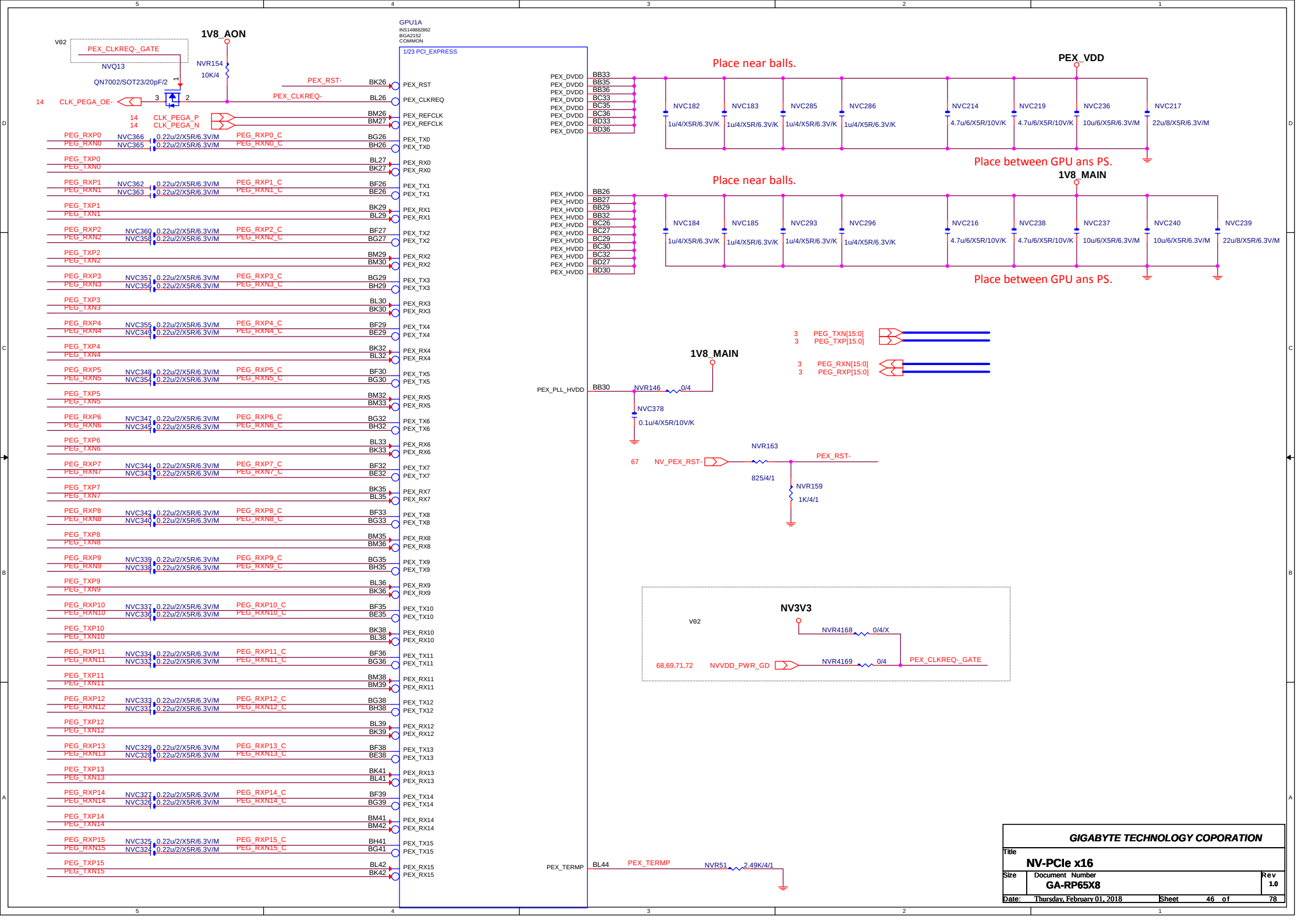
GPU1A
INS148882862
BGA2152
COMMON
1/23 PCI_EXPRESS
1V8_AON
V02
PEX_CLKREQ-_GATE
NVQ13
NVR154
10K/4
QN7002/SOT23/20pF/2
14 CLK_PEGA_OE-
PEX_RST-
PEX_CLKREQ-
14 CLK_PEGA_P
14 CLK_PEGA_N
PEX_RST
PEX_CLKREQ
PEX_REFCLK
PEX_VDD
Place near balls.
Place between GPU ans PS.
1V8_MAIN
PEX_HVDD
PEX_PLL_HVDD
NVR146
0/4
NVC378
0.1u/4/X5R/10V/K
3 PEG_TXN[15:0]
3 PEG_TXP[15:0]
3 PEG_RXN[15:0]
3 PEG_RXP[15:0]
67 NV_PEX_RST-
NVR163
825/4/1
NVR159
1K/4/1
NV3V3
NVR4168
0/4/X
68,69,71,72 NVVDD_PWR_GD
NVR4169
0/4
PEX_CLKREQ-_GATE
PEX_TERMP
BL44
NVR51
2.49K/4/1
GIGABYTE TECHNOLOGY COPORATION
Title
NV-PCIe x16
Size
Document Number
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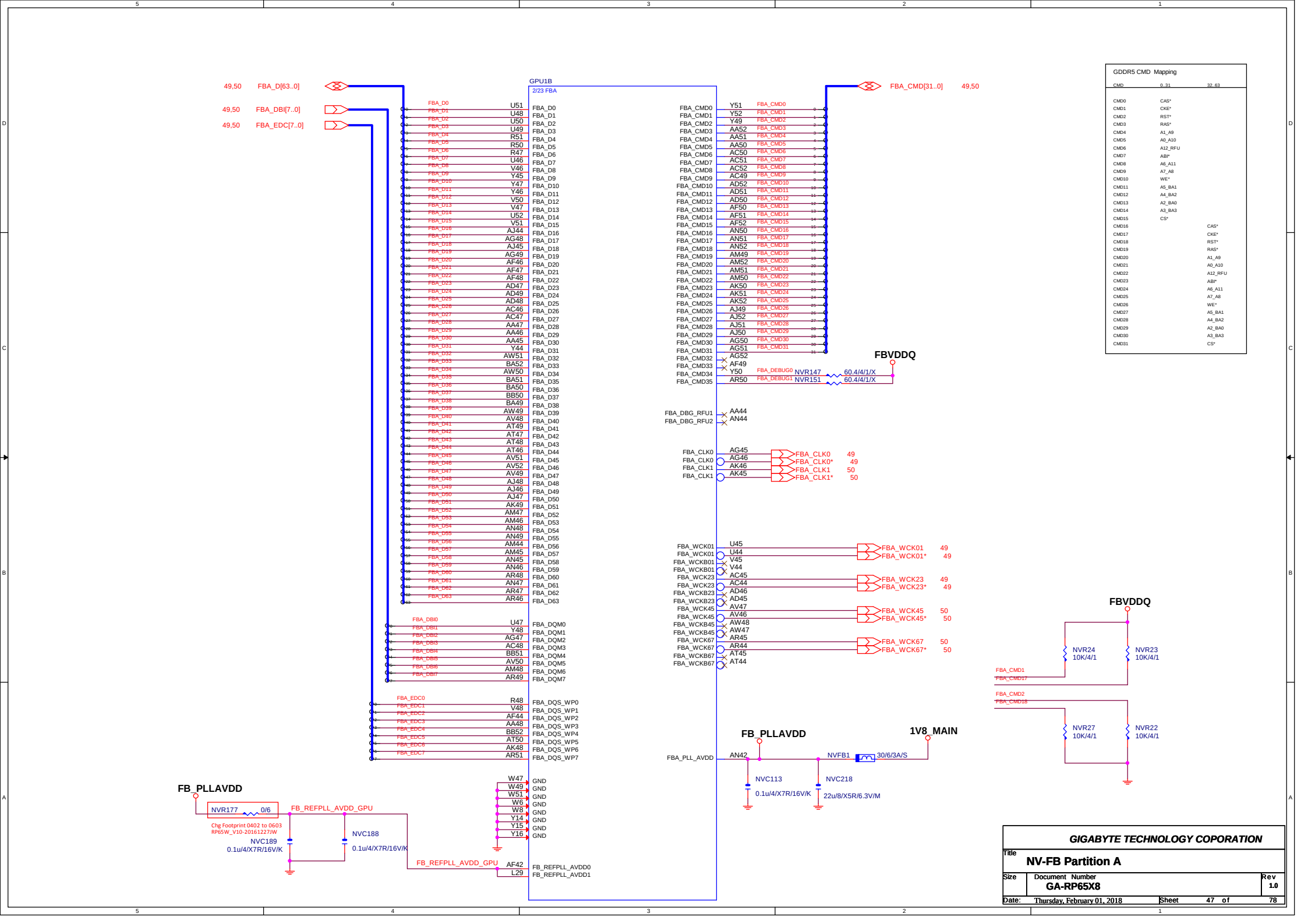
GPU1B
2/23 FBA
49,50 FBA_D[63..0]
49,50 FBA_DBI[7..0]
49,50 FBA_EDC[7..0]
FBA_CMD[31..0] 49,50
GDDR5 CMD Mapping
FBVDDQ
FB_PLLAVDD
1V8_MAIN
NVR177 0/6
Chg Footprint 0402 to 0603
RP65W_V10-20161227JW
FB_REFPLL_AVDD_GPU
NVC188
0.1u/4/X7R/16V/K
NVC189
0.1u/4/X7R/16V/K
NVC113
0.1u/4/X7R/16V/K
NVC218
22u/8/X5R/6.3V/M
NVFB1 30/6/3A/S
NVR147 60.4/4/1/X
NVR151 60.4/4/1/X
NVR24 10K/4/1
NVR23 10K/4/1
NVR27 10K/4/1
NVR22 10K/4/1
GIGABYTE TECHNOLOGY COPORATION
Title
NV-FB Partition A
Size
Document Number
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1.0
Date: Thursday, February 01, 2018
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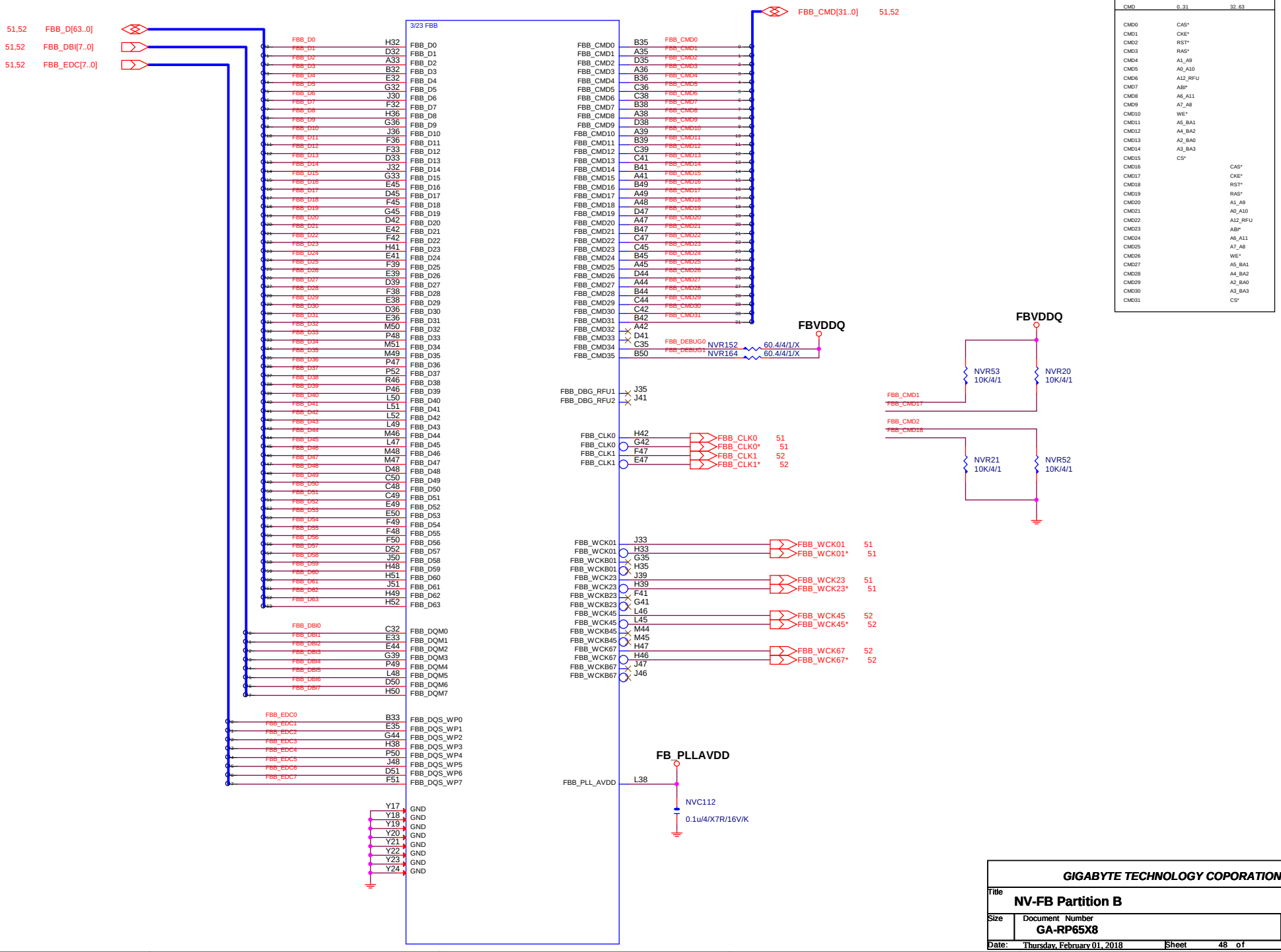
GPU1C
INS148885799
BGA2152
COMMON
3/23 FBB
51,52 FBB_D[63..0]
51,52 FBB_DBI[7..0]
51,52 FBB_EDC[7..0]
FBB_CMD[31..0] 51,52
FBB_D0 H32
FBB_D1 D32
FBB_D2 A33
FBB_D3 B32
FBB_D4 E32
FBB_D5 G32
FBB_D6 J30
FBB_D7 F32
FBB_D8 H36
FBB_D9 G36
FBB_D10 J36
FBB_D11 F36
FBB_D12 F33
FBB_D13 D33
FBB_D14 J32
FBB_D15 G33
FBB_D16 E45
FBB_D17 D45
FBB_D18 F45
FBB_D19 G45
FBB_D20 D42
FBB_D21 E42
FBB_D22 F42
FBB_D23 H41
FBB_D24 E41
FBB_D25 F39
FBB_D26 E39
FBB_D27 D39
FBB_D28 F38
FBB_D29 E38
FBB_D30 D36
FBB_D31 E36
FBB_D32 M50
FBB_D33 P48
FBB_D34 M51
FBB_D35 M49
FBB_D36 P47
FBB_D37 P52
FBB_D38 R46
FBB_D39 P46
FBB_D40 L50
FBB_D41 L51
FBB_D42 L52
FBB_D43 L49
FBB_D44 M46
FBB_D45 L47
FBB_D46 M48
FBB_D47 M47
FBB_D48 D48
FBB_D49 C50
FBB_D50 C48
FBB_D51 C49
FBB_D52 E49
FBB_D53 E50
FBB_D54 F49
FBB_D55 F48
FBB_D56 F50
FBB_D57 D52
FBB_D58 J50
FBB_D59 H48
FBB_D60 H51
FBB_D61 J51
FBB_D62 H49
FBB_D63 H52
FBB_DBI0 C32
FBB_DBI1 E33
FBB_DBI2 E44
FBB_DBI3 G39
FBB_DBI4 P49
FBB_DBI5 L48
FBB_DBI6 D50
FBB_DBI7 H50
FBB_EDC0 B33
FBB_EDC1 E35
FBB_EDC2 G44
FBB_EDC3 H38
FBB_EDC4 P50
FBB_EDC5 J48
FBB_EDC6 D51
FBB_EDC7 F51
Y17 GND
Y18 GND
Y19 GND
Y20 GND
Y21 GND
Y22 GND
Y23 GND
Y24 GND
FBB_CMD0 B35
FBB_CMD1 A35
FBB_CMD2 D35
FBB_CMD3 A36
FBB_CMD4 B36
FBB_CMD5 C36
FBB_CMD6 C38
FBB_CMD7 B38
FBB_CMD8 A38
FBB_CMD9 D38
FBB_CMD10 A39
FBB_CMD11 B39
FBB_CMD12 C39
FBB_CMD13 C41
FBB_CMD14 B41
FBB_CMD15 A41
FBB_CMD16 B49
FBB_CMD17 A49
FBB_CMD18 A48
FBB_CMD19 D47
FBB_CMD20 A47
FBB_CMD21 B47
FBB_CMD22 C47
FBB_CMD23 C45
FBB_CMD24 B45
FBB_CMD25 A45
FBB_CMD26 D44
FBB_CMD27 A44
FBB_CMD28 B44
FBB_CMD29 C44
FBB_CMD30 C42
FBB_CMD31 B42
A42
D41
C35
B50
FBB_DEBUG0
FBB_DEBUG1
NVR152 60.4/4/1/X
NVR164 60.4/4/1/X
FBVDDQ
FBB_DBG_RFU1 J35
FBB_DBG_RFU2 J41
FBB_CLK0 H42
FBB_CLK0 G42
FBB_CLK1 F47
FBB_CLK1 E47
FBB_CLK0 51
FBB_CLK0* 51
FBB_CLK1 52
FBB_CLK1* 52
FBB_WCK01 J33
FBB_WCK01 H33
FBB_WCK01 G35
FBB_WCK01 H35
FBB_WCK23 J39
FBB_WCK23 H39
FBB_WCK23 F41
FBB_WCK23 G41
FBB_WCK45 L46
FBB_WCK45 L45
FBB_WCK45 M44
FBB_WCK45 M45
FBB_WCK67 H47
FBB_WCK67 H46
FBB_WCK67 J47
FBB_WCK67 J46
FBB_WCK01 51
FBB_WCK01* 51
FBB_WCK23 51
FBB_WCK23* 51
FBB_WCK45 52
FBB_WCK45* 52
FBB_WCK67 52
FBB_WCK67* 52
FB_PLLAVDD
FBB_PLL_AVDD L38
NVC112
0.1u/4/X7R/16V/K
FBVDDQ
NVR53 10K/4/1
NVR20 10K/4/1
NVR21 10K/4/1
NVR52 10K/4/1
FBB_CMD1
FBB_CMD17
FBB_CMD2
FBB_CMD18
GDDR5 CMD Mapping
CMD 0..31 32..63
CMD0 CAS*
CMD1 CKE*
CMD2 RST*
CMD3 RAS*
CMD4 A1_A9
CMD5 A0_A10
CMD6 A12_RFU
CMD7 ABI*
CMD8 A6_A11
CMD9 A7_A8
CMD10 WE*
CMD11 A5_BA1
CMD12 A4_BA2
CMD13 A2_BA0
CMD14 A3_BA3
CMD15 CS*
CMD16 CAS*
CMD17 CKE*
CMD18 RST*
CMD19 RAS*
CMD20 A1_A9
CMD21 A0_A10
CMD22 A12_RFU
CMD23 ABI*
CMD24 A6_A11
CMD25 A7_A8
CMD26 WE*
CMD27 A5_BA1
CMD28 A4_BA2
CMD29 A2_BA0
CMD30 A3_BA3
CMD31 CS*
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Title
NV-FB Partition B
Size
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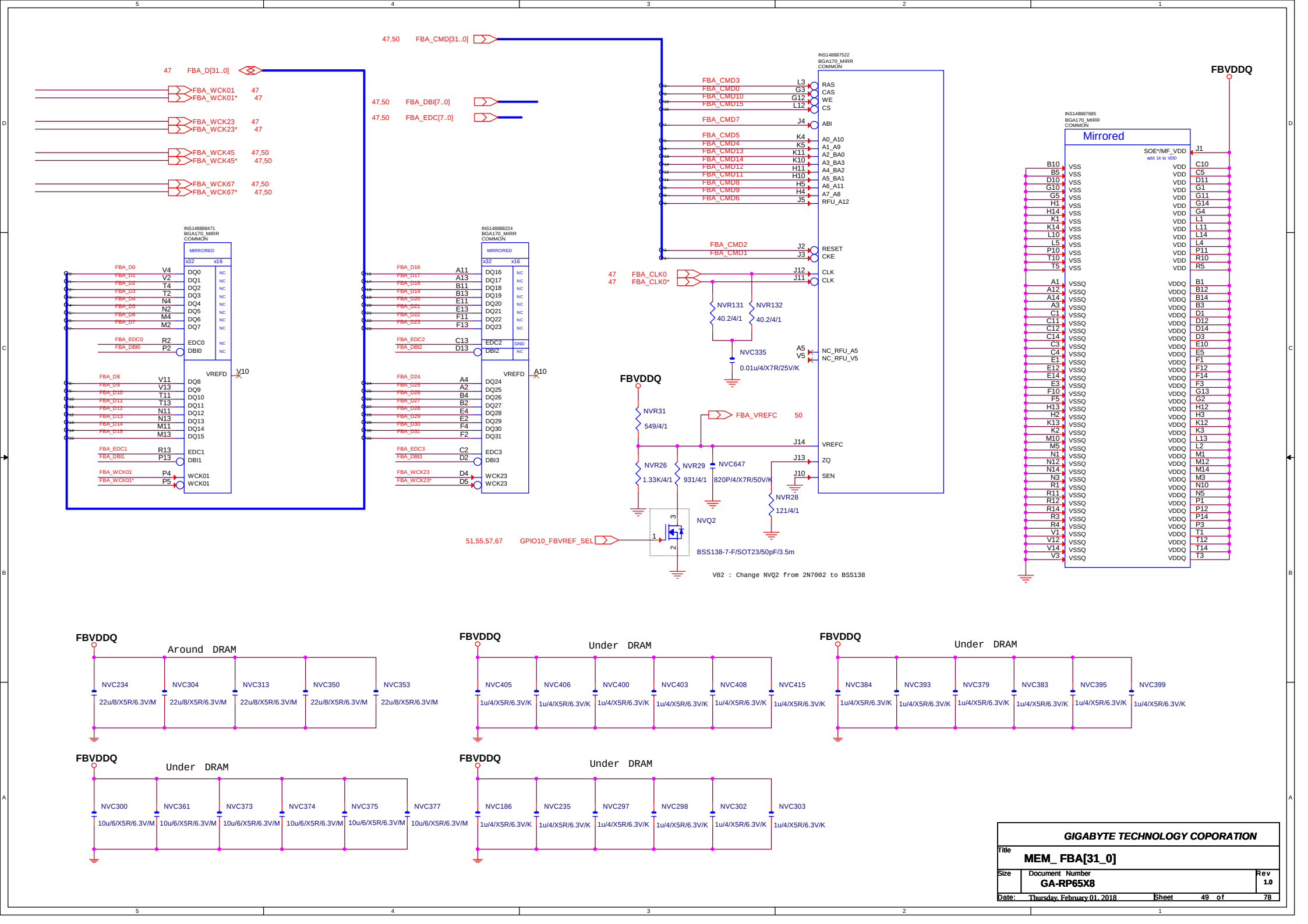

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Title: MEM_ FBA[31_0]

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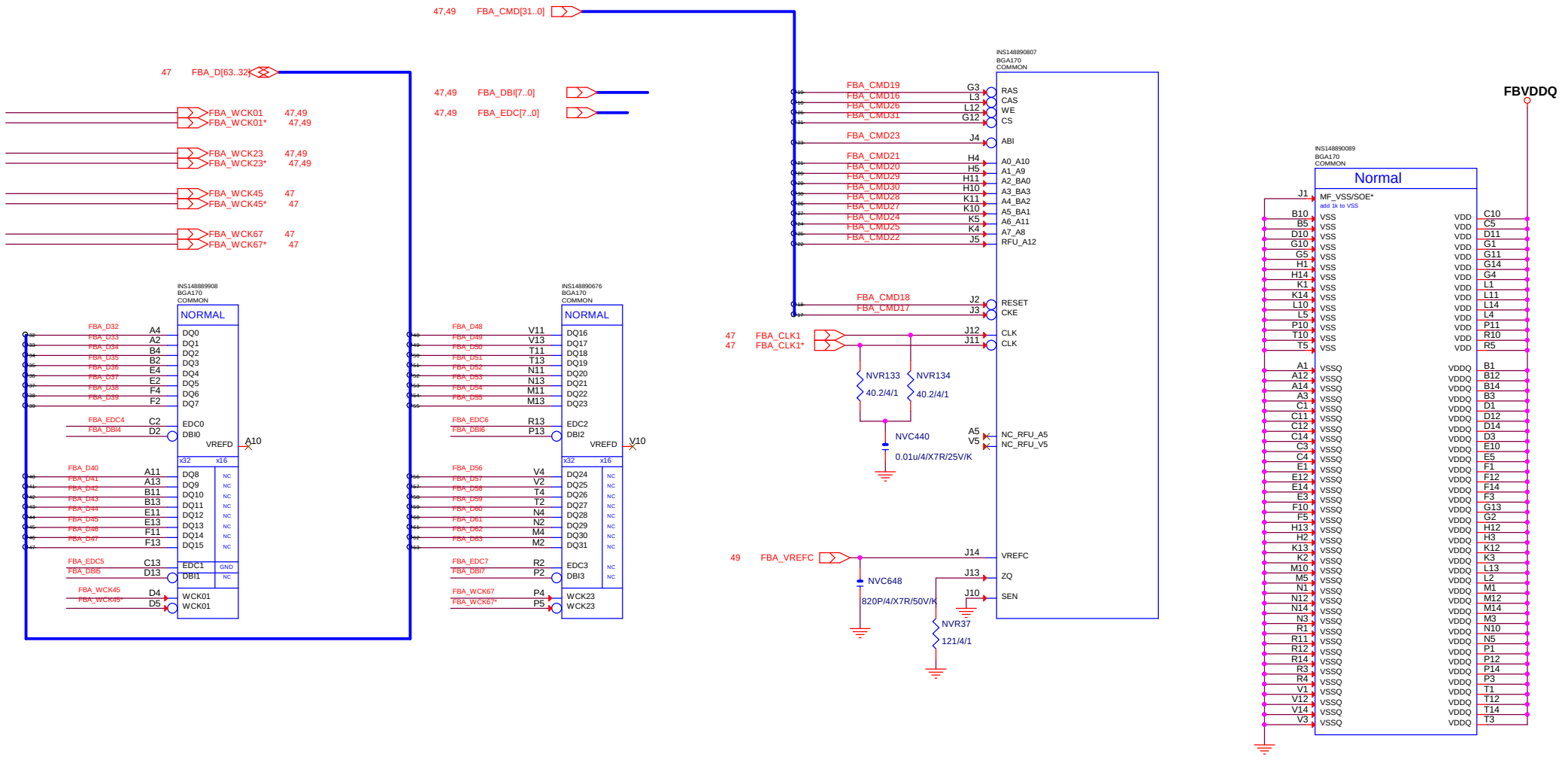

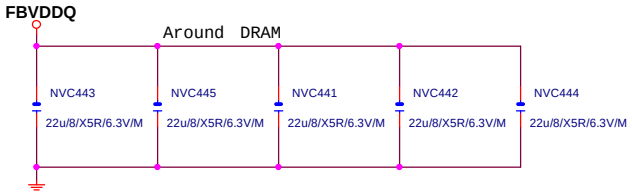

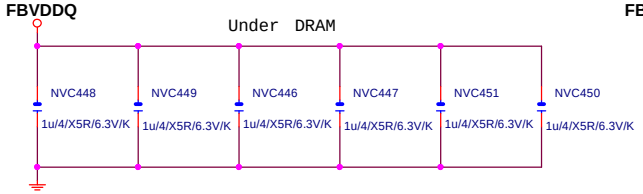

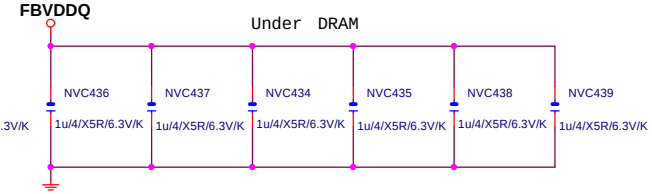

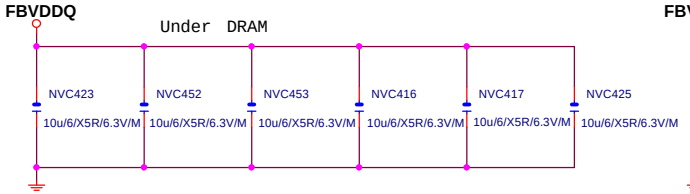

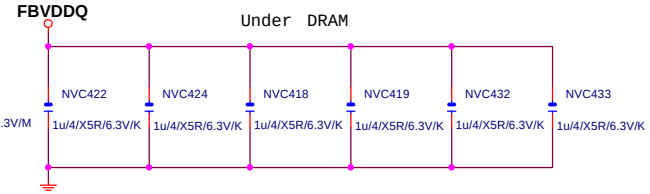

GIGABYTE TECHNOLOGY COPORATION			
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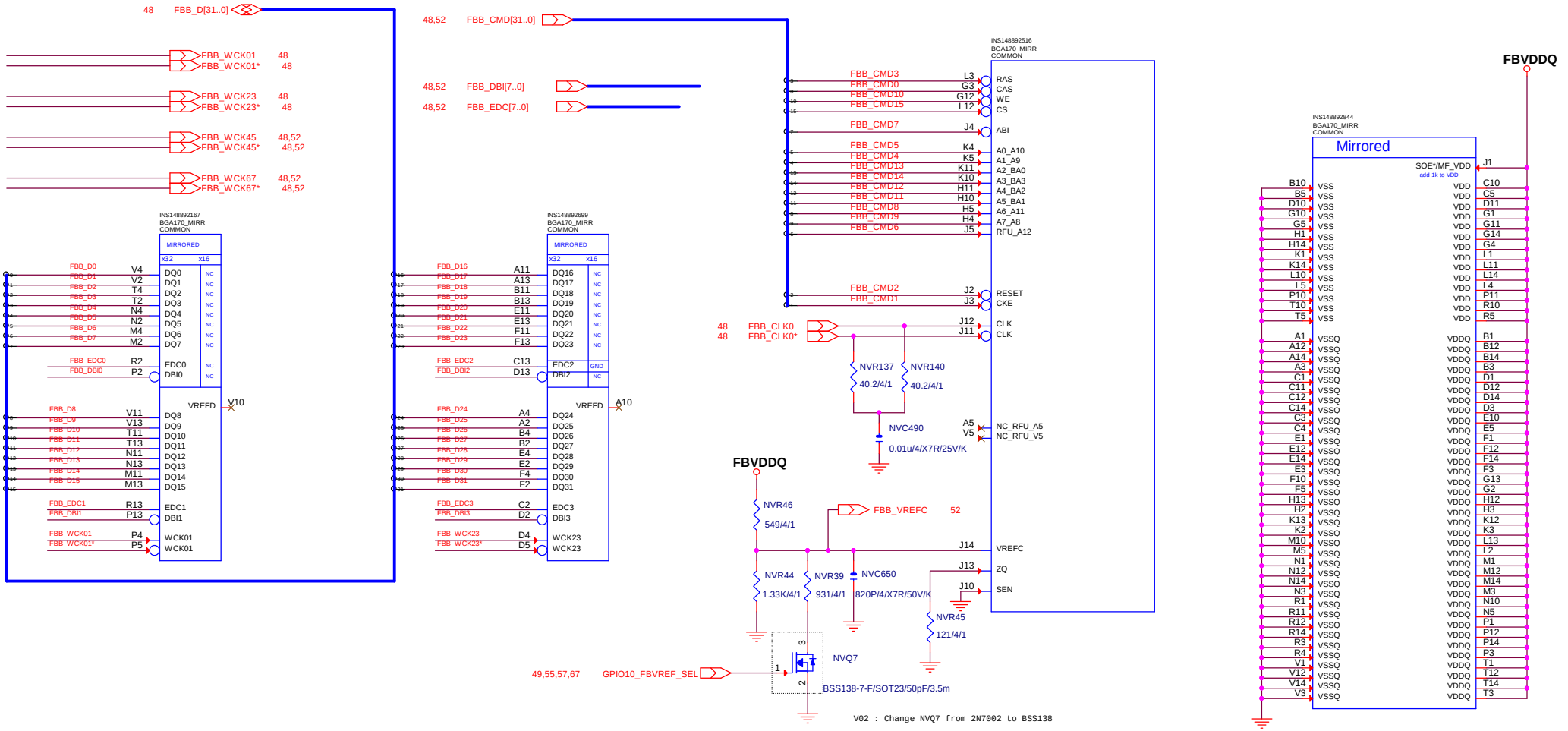
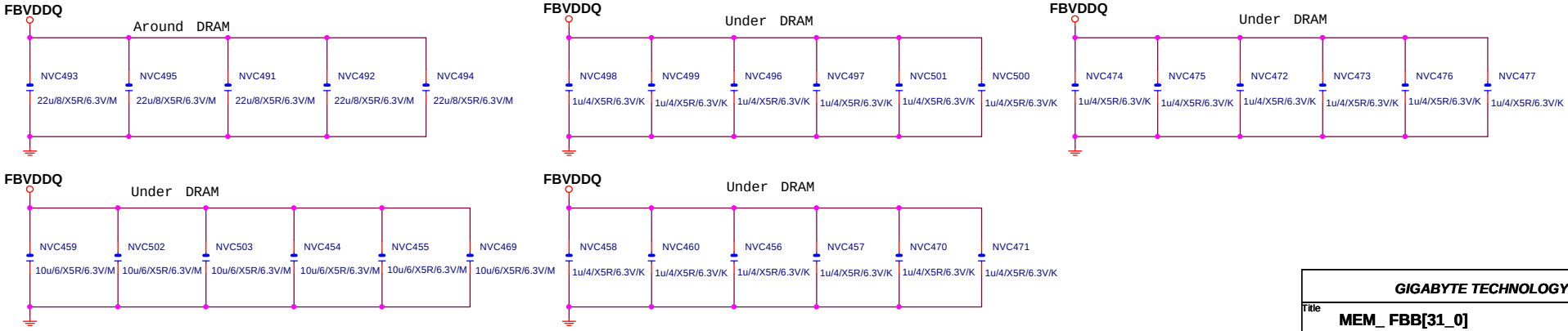
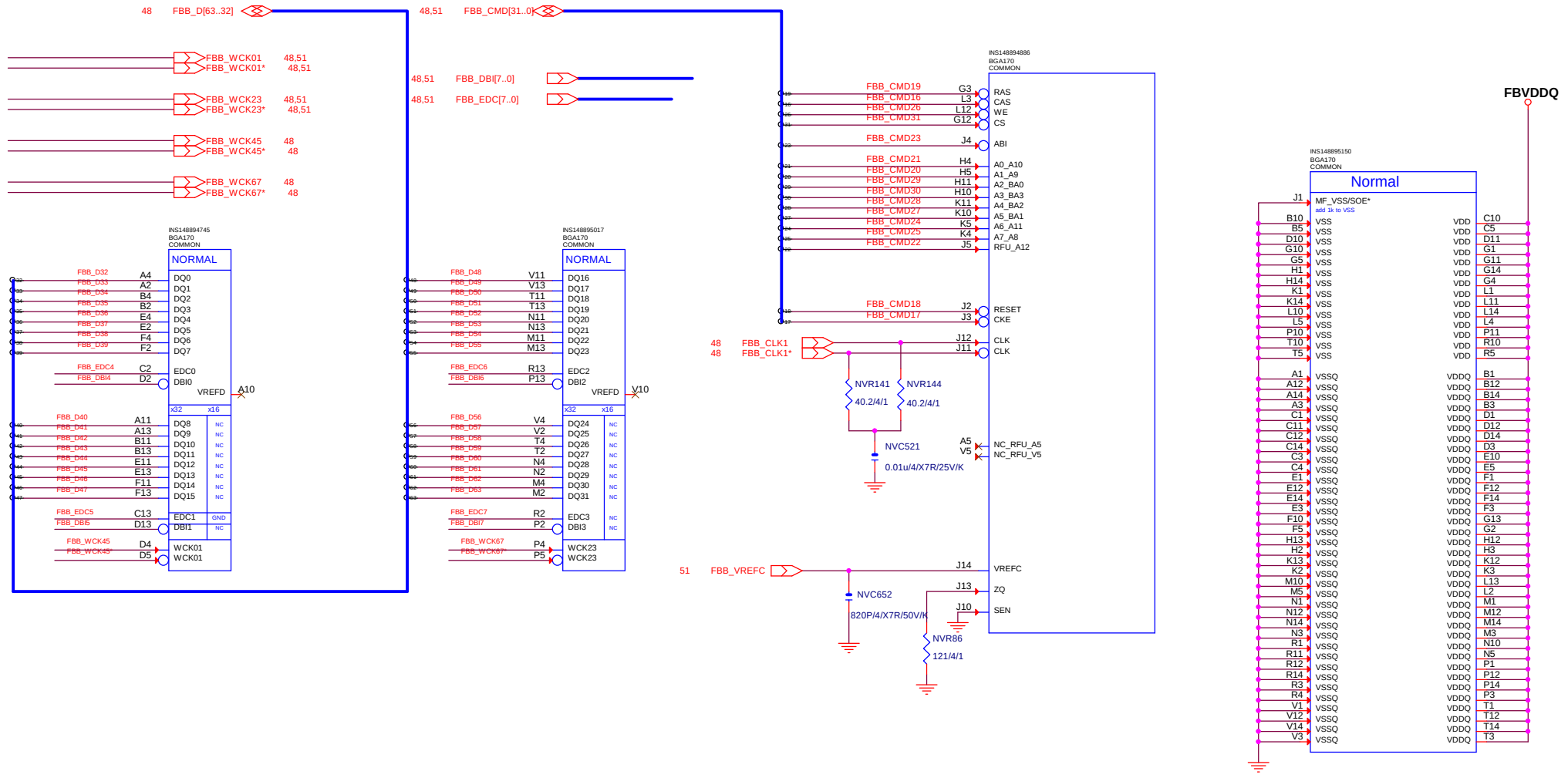




GIGABYTE TECHNOLOGY COPORATION		
Title: MEM_ FBB[31_0]		
Size	Document Number: GA-RP65X8	Rev: 1.0
Date: Thursday, February 01, 2018	Sheet 51 of 78	



GIGABYTE TECHNOLOGY COPORATION

Title: MEM_ FBB[63_32]

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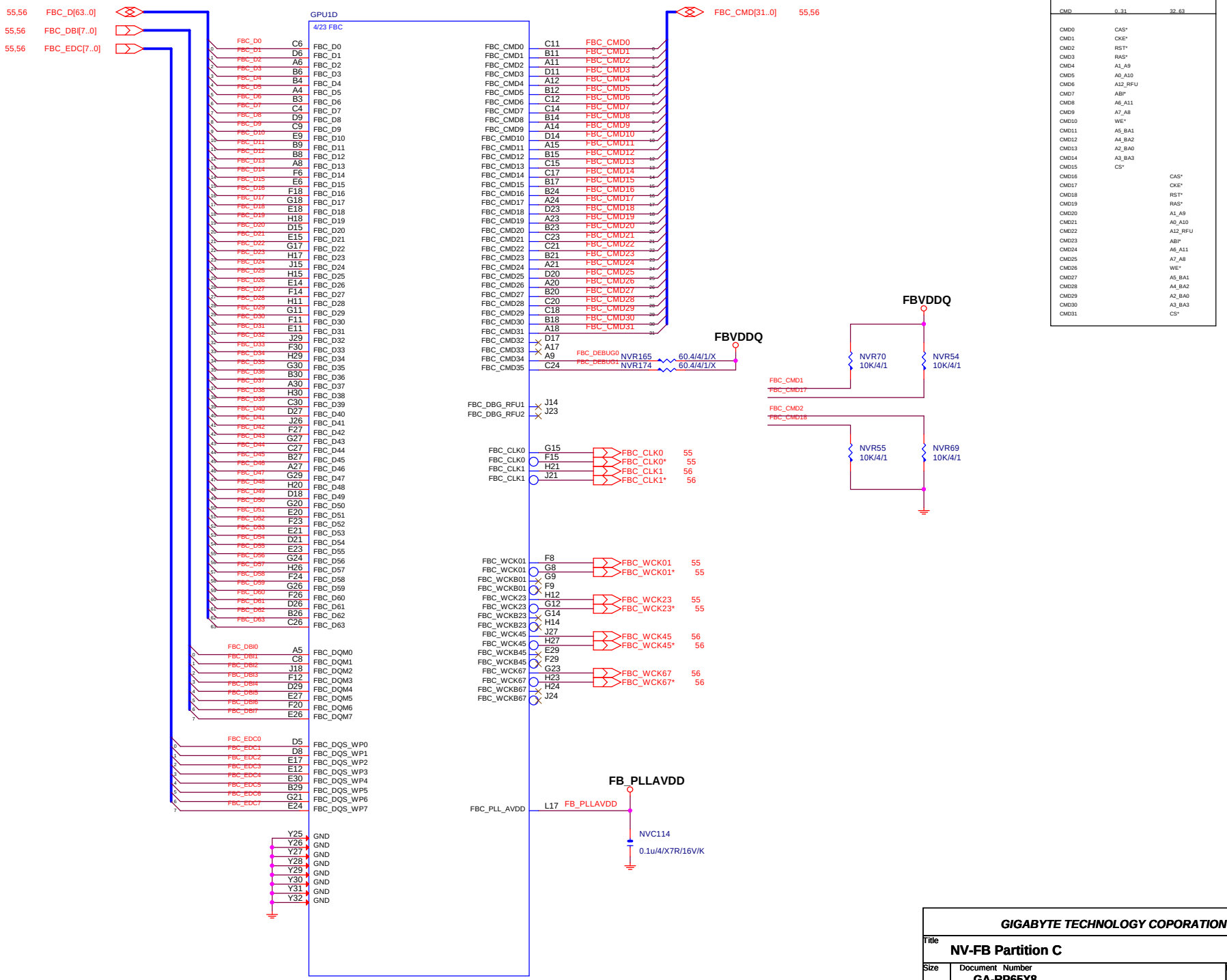

GIGABYTE TECHNOLOGY COPORATION			
Title: NV-FB Partition C			
Size	Document Number: GA-RP65X8		Rev: 1.0
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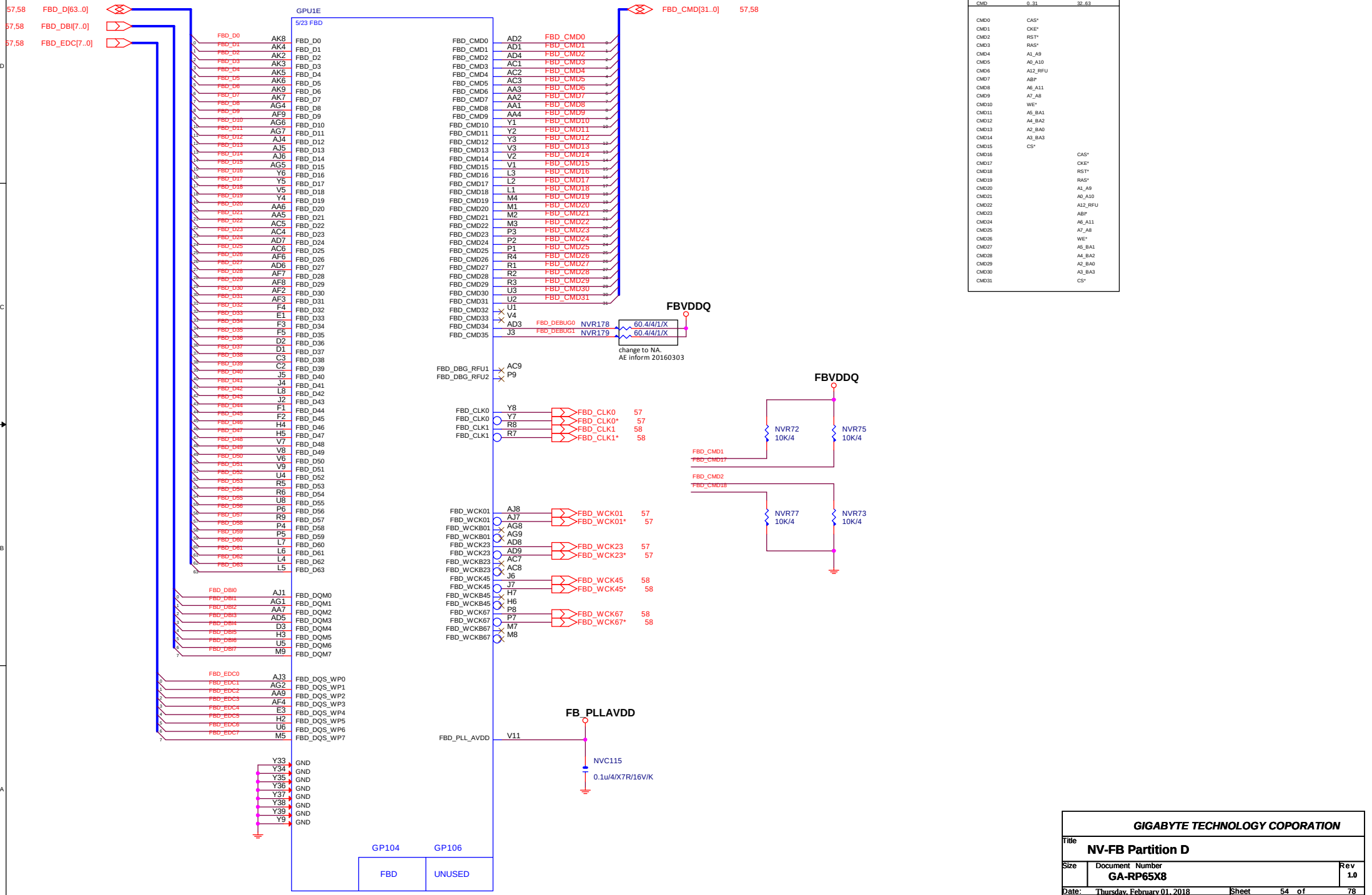

GDDR5 CMD Mapping

CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

GIGABYTE TECHNOLOGY COPORATION		
Title: NV-FB Partition D		
Size	Document Number: GA-RP65X8	Rev: 1.0
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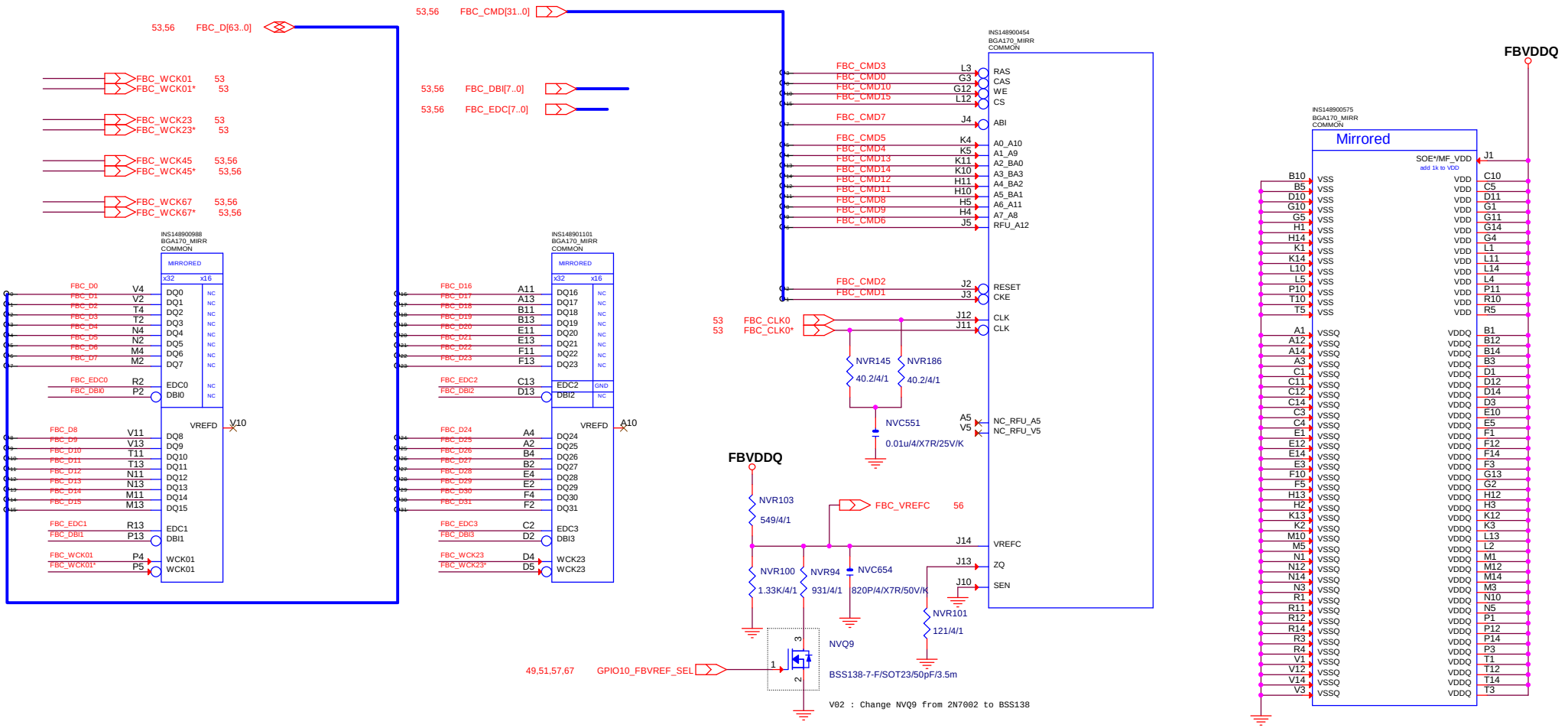

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Title: MEM_ FBC[31_0]

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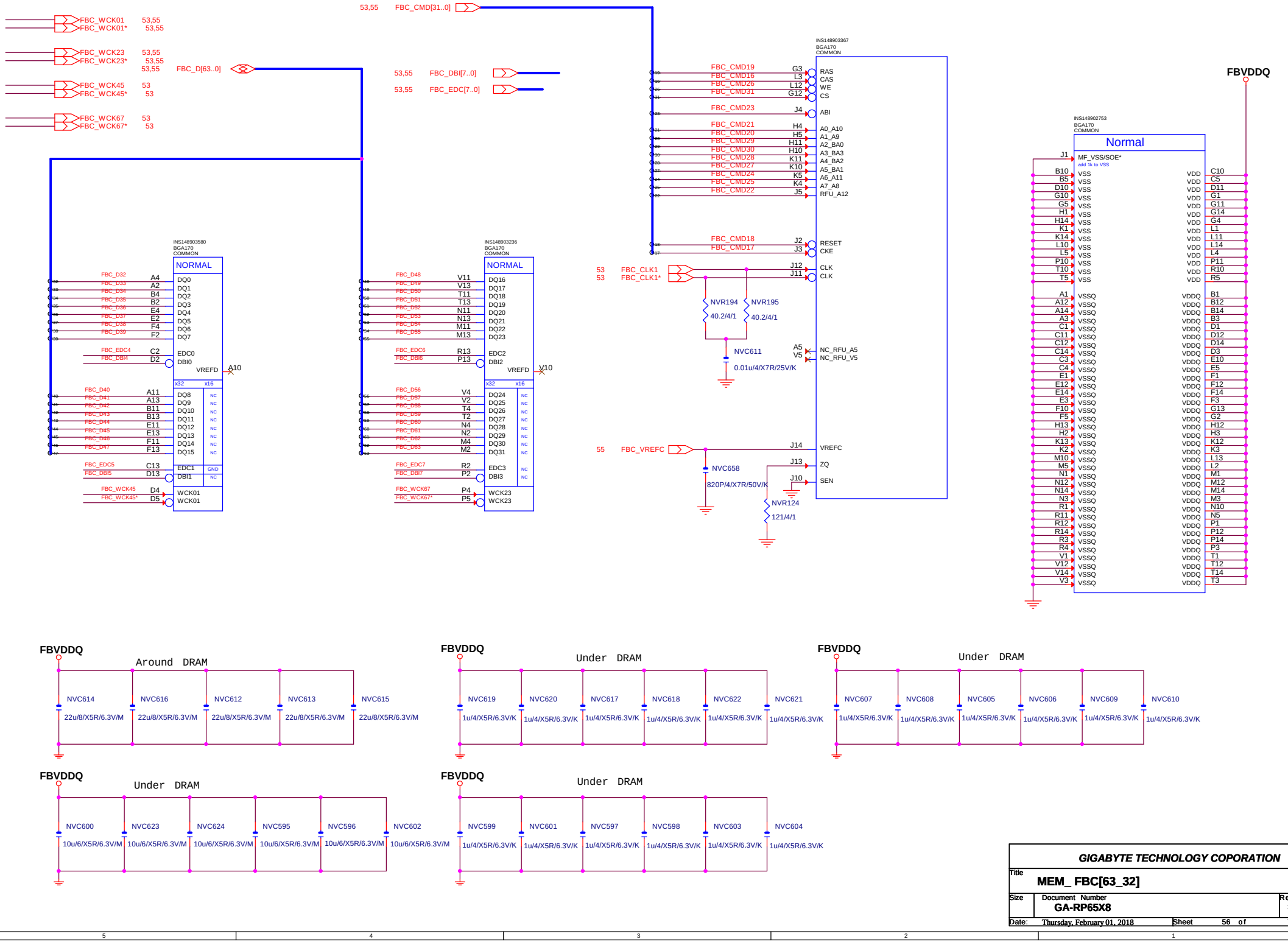

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Title: MEM_ FBC[63_32]		
Size	Document Number: GA-RP65X8	Rev: 1.0
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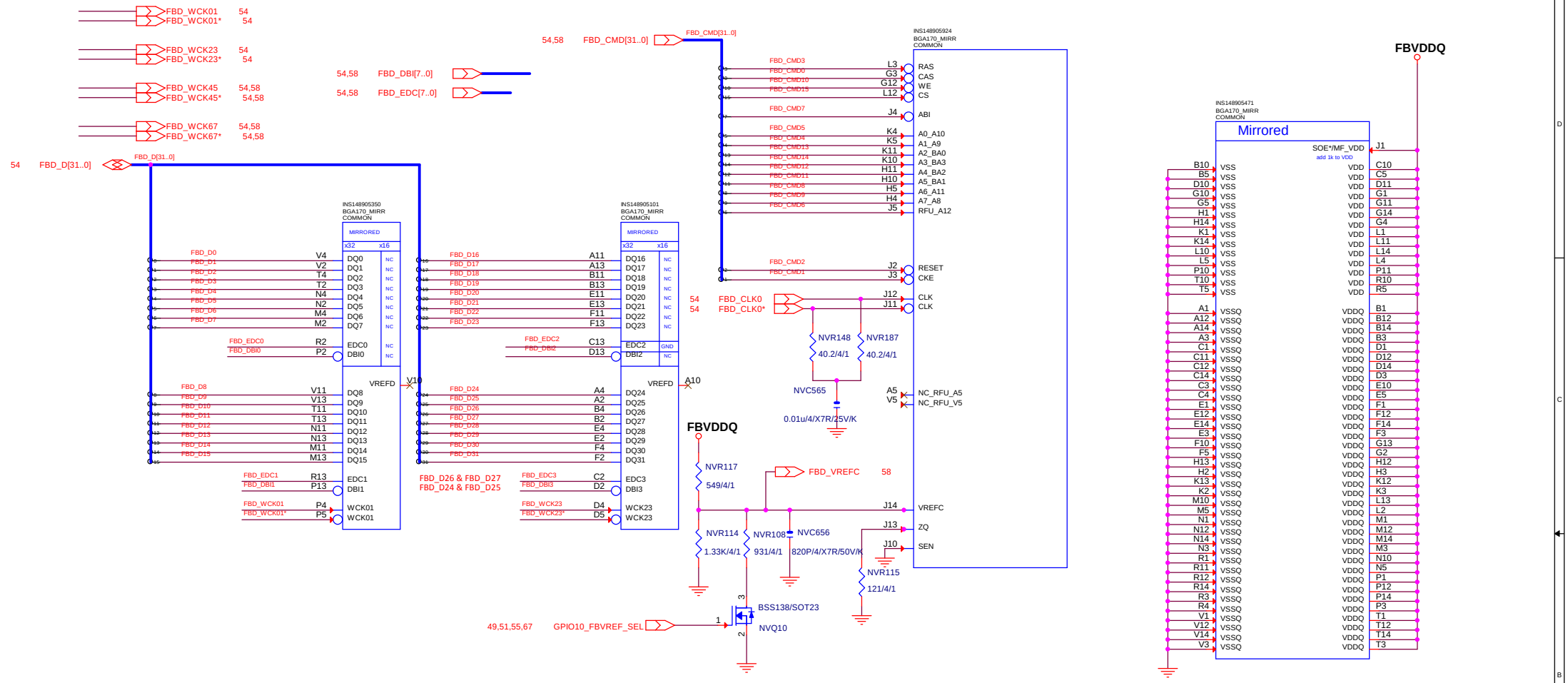
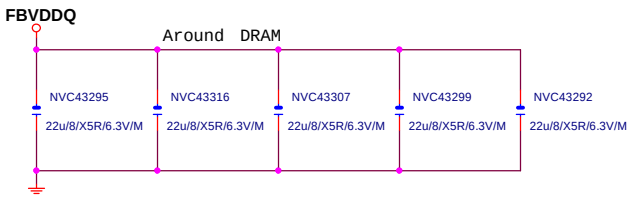
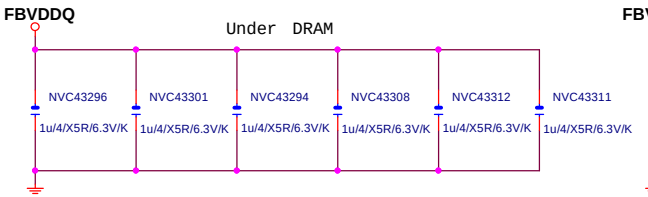
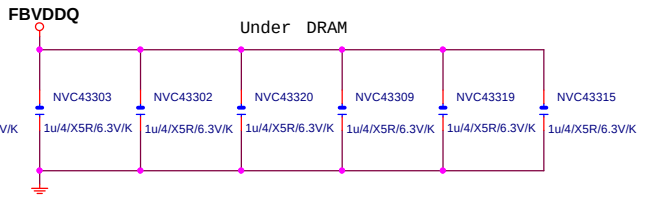
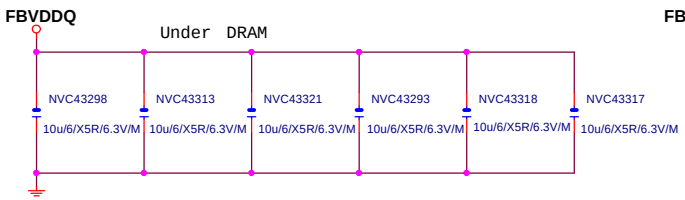
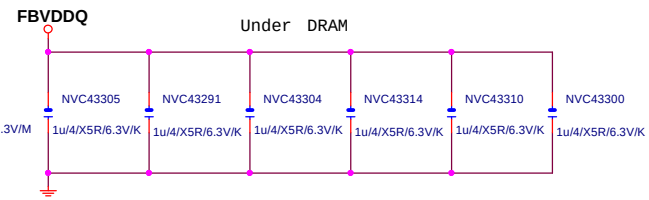




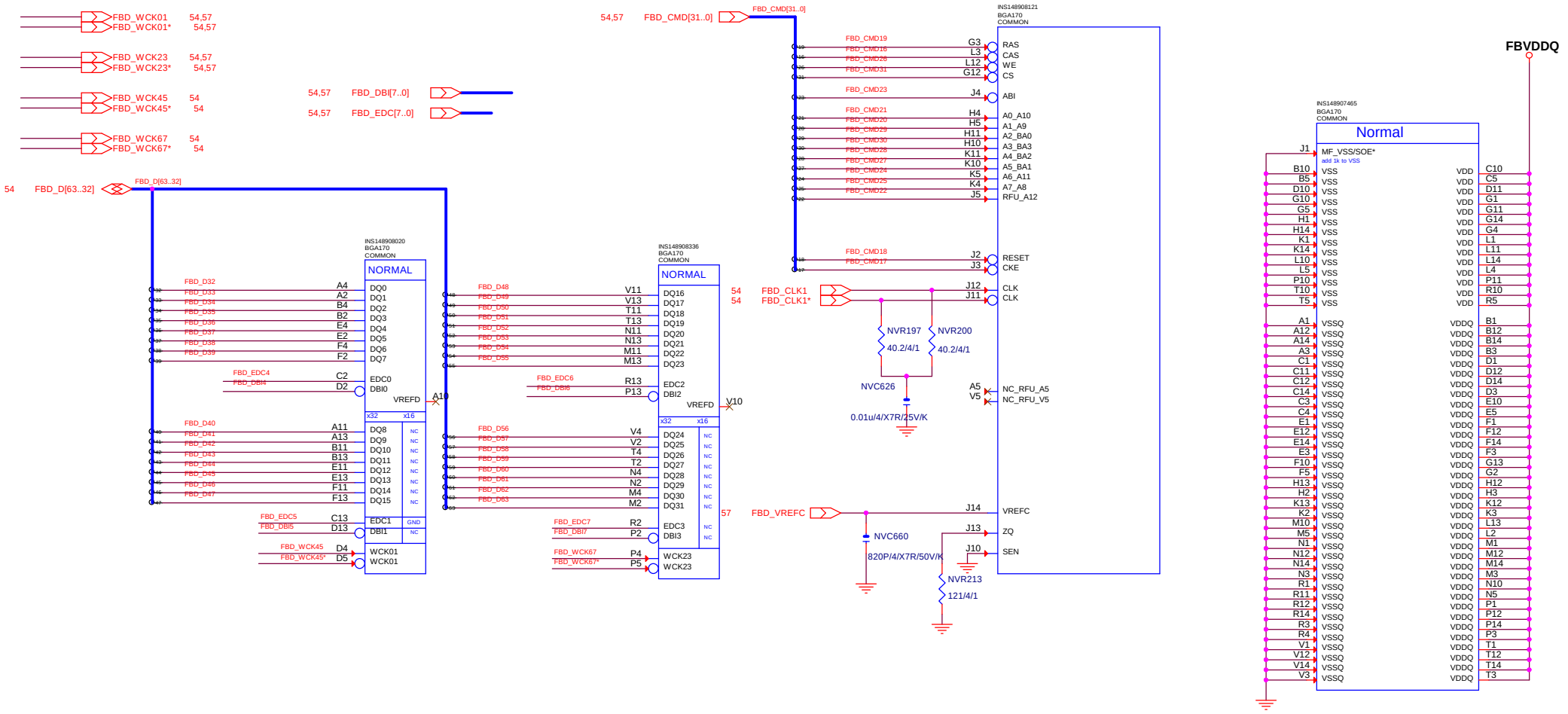


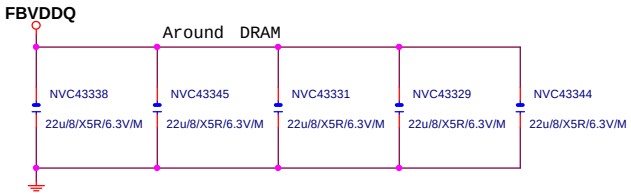


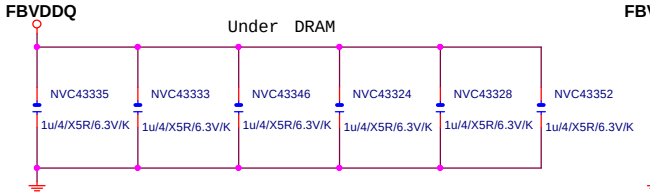


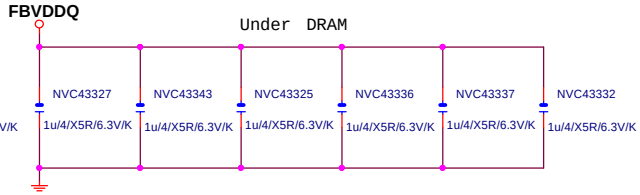


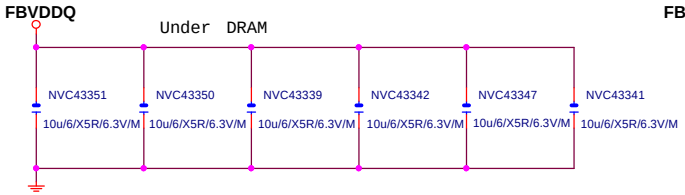
GIGABYTE TECHNOLOGY COPORATION		
Title: MEM_ FBD[31_0]		
Size	Document Number: GA-RP65X8	Rev: 1.0
Date: Thursday, February 01, 2018	Sheet 57 of 78	

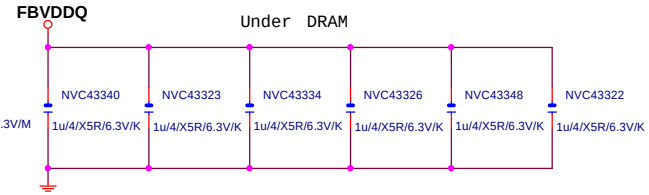




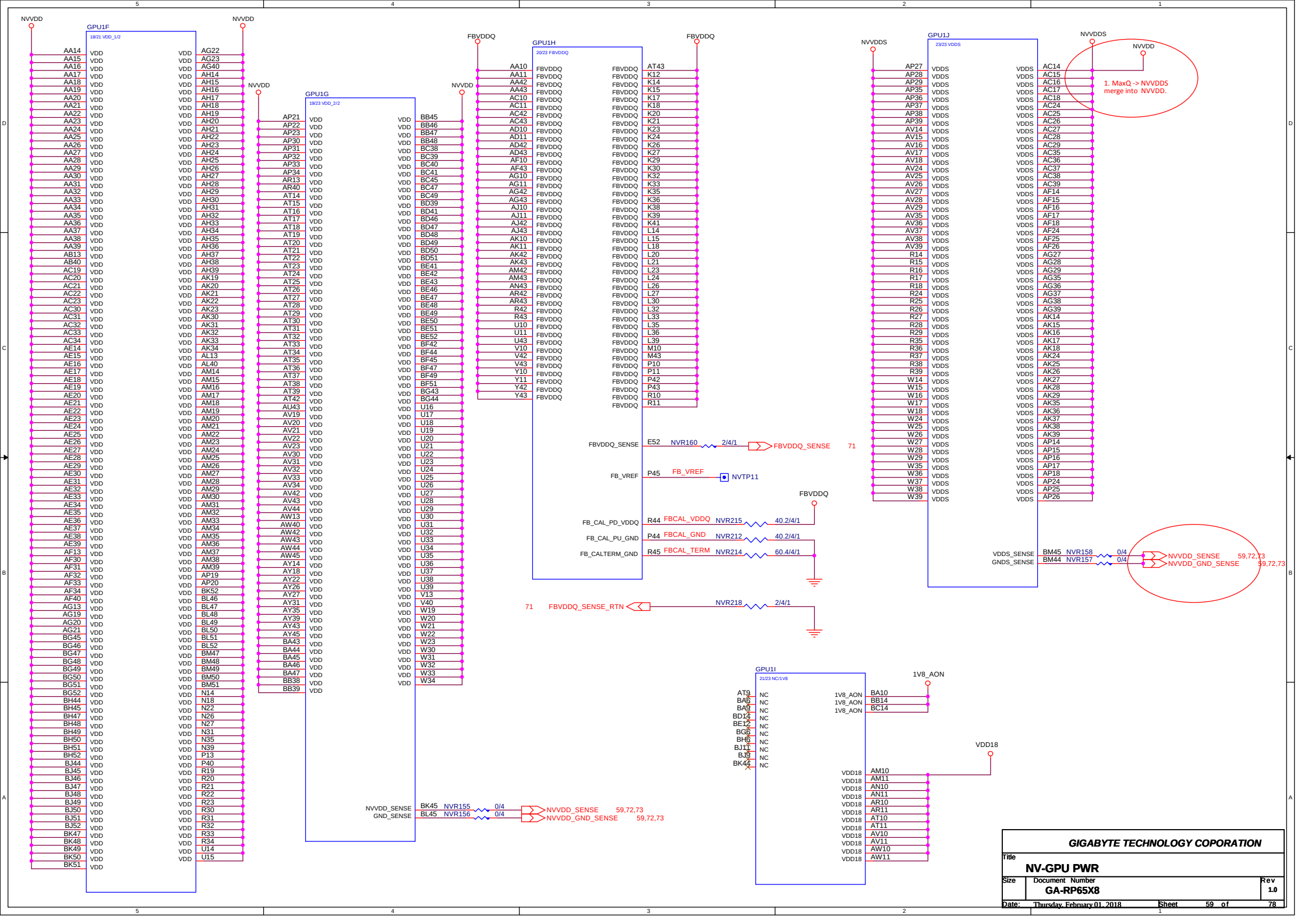




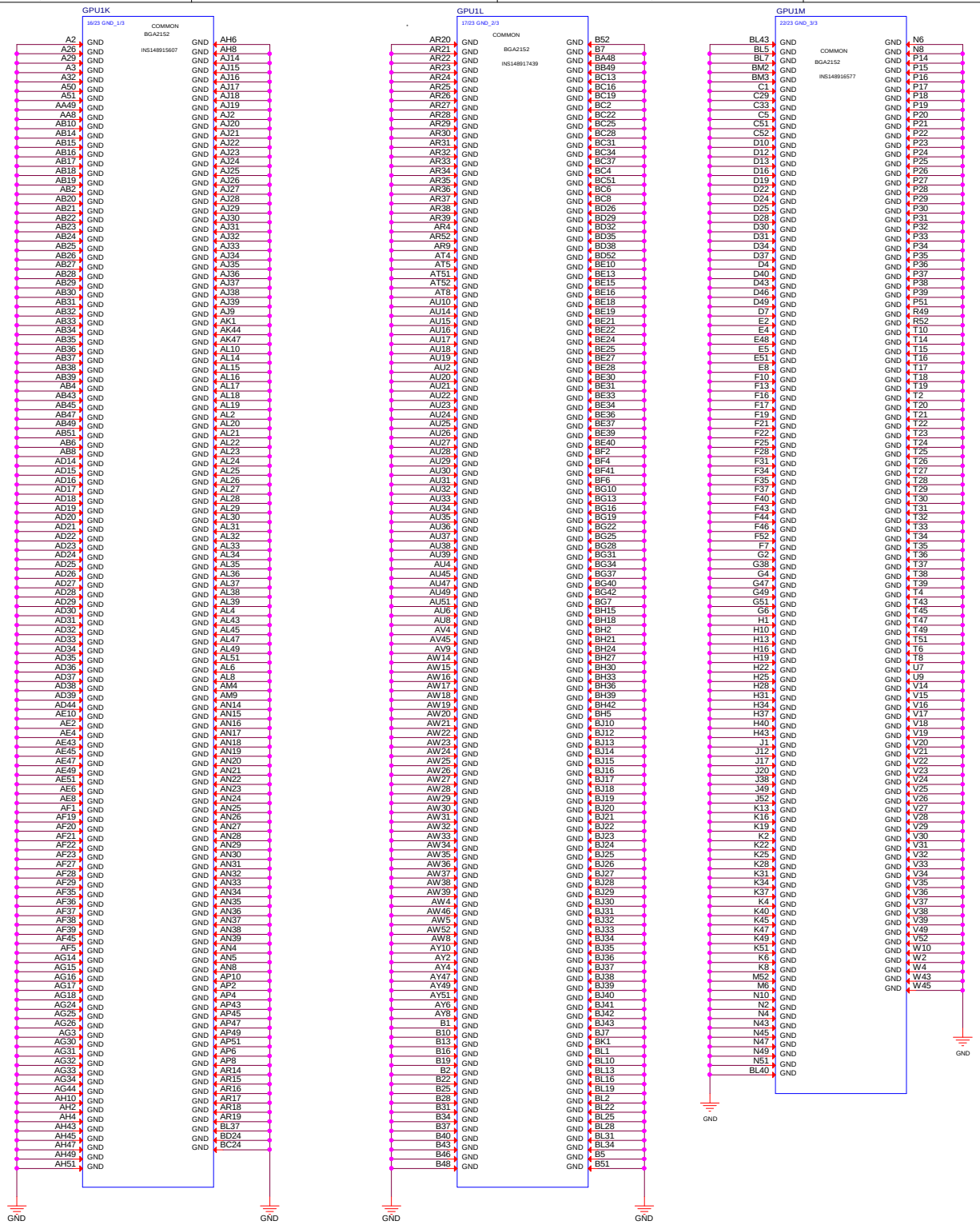




GIGABYTE TECHNOLOGY COPORATION		
Title: MEM_ FBD[63_32]		
Size	Document Number: GA-RP65X8	Rev: 1.0
Date: Thursday, February 01, 2018	Sheet 58 of 78	



GIGABYTE TECHNOLOGY COPORATION	
Title	**NV-GPU PWR**
Size	Document Number **GA-RP65X8** Rev **1.0**
Date:	Thursday, February 01, 2018 Sheet 59 of 78



GIGABYTE TECHNOLOGY COPORATION	
Title	NV-GPU GND
Size	Document Number: GA-RP65X8 — Rev: 1.0
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GPU DECOUPLING

FBVDDQ

Partition A 2 x 10uF / 6 x 1uF — Under GPU

NVC187 NVC190 NVC198 NVC199 NVC200 NVC201 NVC288 NVC287
1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M

Partition B 2 x 10uF / 6 x 1uF — Under GPU

NVC291 NVC295 NVC202 NVC203 NVC290 NVC294 NVC292 NVC289
1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M

Partition C 2 x 10uF / 6 x 1uF — Under GPU

NVC307 NVC310 NVC299 NVC301 NVC306 NVC309 NVC308 NVC305
1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M

Partition D 2 x 10uF / 6 x 1uF — Under GPU

NVC316 NVC319 NVC311 NVC312 NVC315 NVC318 NVC317 NVC314
1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M

Place close to GPU 4 x 10uF

NVC37 NVC36 NVC76 NVC34
10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M

Place close to GPU 9 x 10uF

NVC39 NVC38 NVC77 NVC35 NVC43
22u/6/X5R/6.3V/M 22u/6/X5R/6.3V/M 22u/6/X5R/6.3V/M 22u/6/X5R/6.3V/M 22u/6/X5R/6.3V/M

Place close to GPU

NVC41 NVC40 NVC78 NVC42
22u/6/X5R/6.3V/M 22u/6/X5R/6.3V/M 22u/6/X5R/6.3V/M 22u/6/X5R/6.3V/M

Place close to GPU

NVVDDS
NVC55 47u/8/X5R/6.3V/M
NVCT3 330u/TP/S/2.5V/B2/9m
NVVDD
1. MaxQ -> NVVDDS merge into NVVDD.

NVVDD
NVCT11 330u/TP/S/2.5V/B2/9m

NVVDD
NVCT12 330u/TP/S/2.5V/B2/9m

NVVDDS

Under GPU

NVC86 NVC60 NVC698 NVC85
10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M

Under GPU

NVC323 NVC341 NVC320 NVC321 NVC322 NVC330 NVC346 NVC351
1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K

Under GPU

NVC369 NVC370 NVC359 NVC367 NVC364 NVC368 NVC371 NVC352
1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K

NVVDDS
16 x 1uF
4 x 10uF

NVVDD

Under GPU

NVC61 NVC58 NVC57 NVC84
10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M

Under GPU

NVC45 NVC46 NVC82 NVC47 NVC44 NVC54
47u/8/X5R/6.3V/M 47u/8/X5R/6.3V/M 22u/6/X5R/6.3V/M 22u/6/X5R/6.3V/M 22u/6/X5R/6.3V/M 22u/6/X5R/6.3V/M

Under GPU

NVC49 NVC50 NVC83 NVC51 NVC48 NVC52 NVC53
10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M

49 x 1uF
11 x 10uF
4 x 22uF
2 x 47uF
2 x 330uF

NVVDD
NVCT2 330u/TP/S/2.5V/B2/9m

NVVDD
NVCT1 330u/TP/S/2.5V/B2/9m

x49 1uF X7R 0402

Under GPU

NVC241 NVC244 NVC243 NVC245 NVC220 NVC222 NVC215 NVC242 NVC221 NVC223
1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K

Under GPU

NVC251 NVC254 NVC253 NVC255 NVC247 NVC249 NVC246 NVC252 NVC248 NVC250
1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K

Under GPU

NVC261 NVC264 NVC263 NVC265 NVC257 NVC259 NVC256 NVC262 NVC258 NVC260
1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K

Under GPU

NVC233 NVC232 NVC231 NVC230 NVC229 NVC228 NVC227 NVC226 NVC225
1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K

Under GPU

NVC213 NVC212 NVC211 NVC210 NVC209 NVC208 NVC207 NVC206 NVC205 NVC204
1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K

VDD18

NVC66 NVC68 NVC67 NVC69
4.7u/6/X5R/10V/K 1u/4/X5R/6.3V/K 0.1u/4/X7R/16V/K 0.1u/4/X7R/16V/K

VDD18

NVC70 NVC72 NVC71 NVC73
4.7u/6/X5R/10V/K 1u/4/X5R/6.3V/K 0.1u/4/X7R/16V/K 0.1u/4/X7R/16V/K

1V8_MAIN — NVR273 0/8 — VDD18

1V8_AON
place 1 x 0.1uF cap near BA10

NVC62 NVC63 NVC65 NVC64
4.7u/6/X5R/10V/K 1u/4/X5R/6.3V/K 0.1u/4/X7R/16V/K 0.1u/4/X7R/16V/K

VDD18

NVC74 NVC79 NVC75 NVC80 NVC81
4.7u/6/X5R/10V/K 1u/4/X5R/6.3V/K 0.1u/4/X7R/16V/K 0.1u/4/X7R/16V/K 0.1u/4/X7R/16V/K

place 1 x 0.1uf cap for BB14 and BC14 to share

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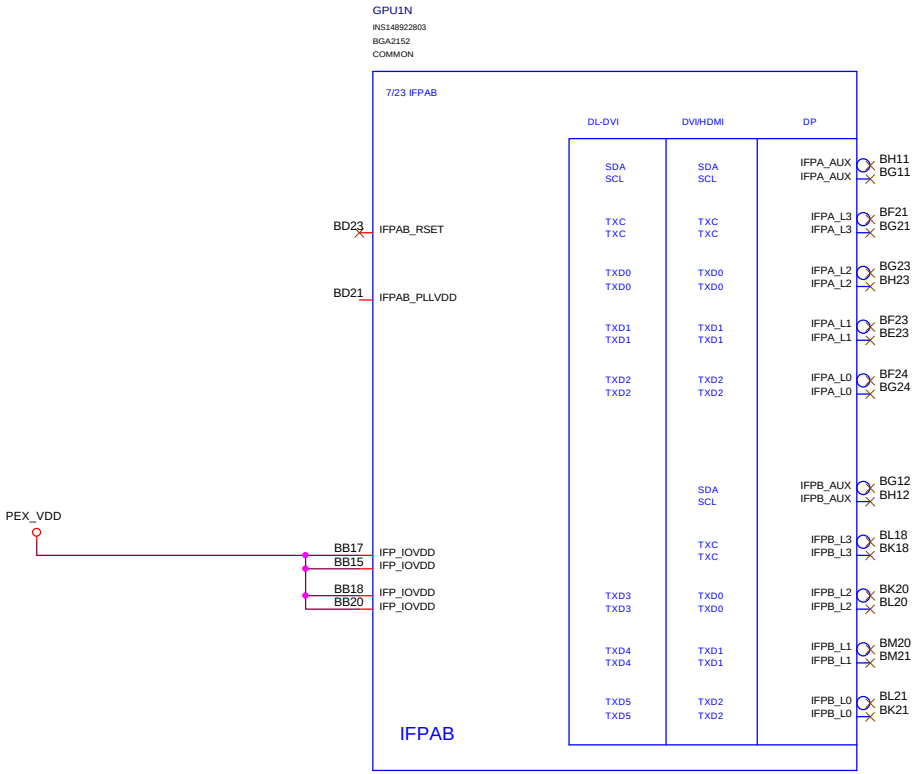

Table 10. NVVDD Voltage Regulator Requirements

Feature	Guidance
Regulator Solution Index	• N17E-G3: OVR4+ 4ph-2xDualFET/ph L=13x13x4 Lsat=70A or better • N17E-G2: OVR2+ 3ph-DualFET/ph L=10x10x4 Lsat=68A/ph or better • N17E-G1: OVR2+ 3ph-DualFET/ph L=10x10x4 Lsat=68A/ph or better
Load line	No
Low Power Mode	AutoPSI integrated in OVR4+ and OVR2+
PDN Specification (DC)	TBD
Overall Efficiency	• N17E-G3: 80% or better at EDPc = 121A • N17E-G2: 80% or better at EDPc = 80A • N17E-G1: 80% or better at EDPc = 62A

Table 11. NVVDDS Voltage Regulator Requirements

Feature	Guidance
Regulator Solution Index	• N17E-G3: OVR2+ 2ph-DualFET/ph L=10x10x4 Lsat=68A/ph or better • N17E-G2: OVR2+ 1ph-DualFET/ph L=10x10x4 Lsat=68A/ph or better • N17E-G1: OVR2+ 1ph-DualFET/ph L=10x10x4 Lsat=68A/ph or better
Load line	No
Low Power Mode	AutoPSI integrated in OVR4+ and OVR2+
PDN Specification (DC)	TBD
Overall Efficiency	• N17E-G3: 80% or better at EDPc = 37A • N17E-G2: 80% or better at EDPc = 26A • N17E-G1: 80% or better at EDPc = 21A

Table 12. FBVDD Voltage Regulator Requirements

Feature	Guidance
Regulator Solution Index	• N17E-G3: 1ph-DualFET/ph or better • N17E-G2: 1ph-DualFET/ph or better • N17E-G1: 1ph-DualFET/ph or better
PDN for FBVDD Power plane	TBD
Overall Efficiency	• N17E-G3: 80% or better at EDPc = 30A • N17E-G2: 80% or better at EDPc = 29A • N17E-G1: 80% or better at EDPc = 26A

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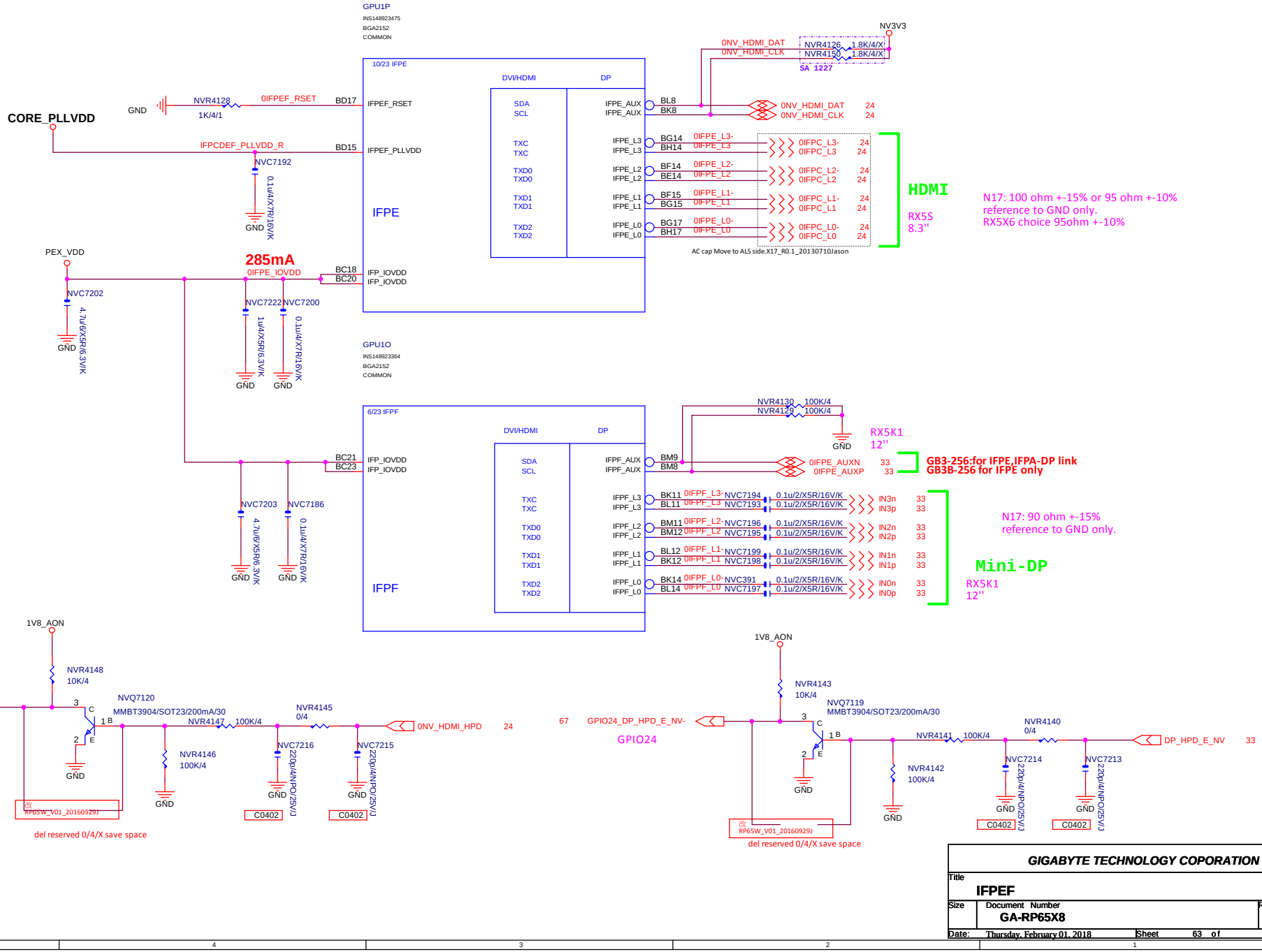
GB4-256 Split Mode EF	
Link AB	Not Connected
Link C	DisplayPort, HDMI
Link D	DisplayPort/eDP
Link E	DisplayPort, HDMI, DVI (Single Link or Dual Link)
Link F	DisplayPort/eDP, DVI (Single Link or Dual Link)
1. Only four independent display heads supported.	



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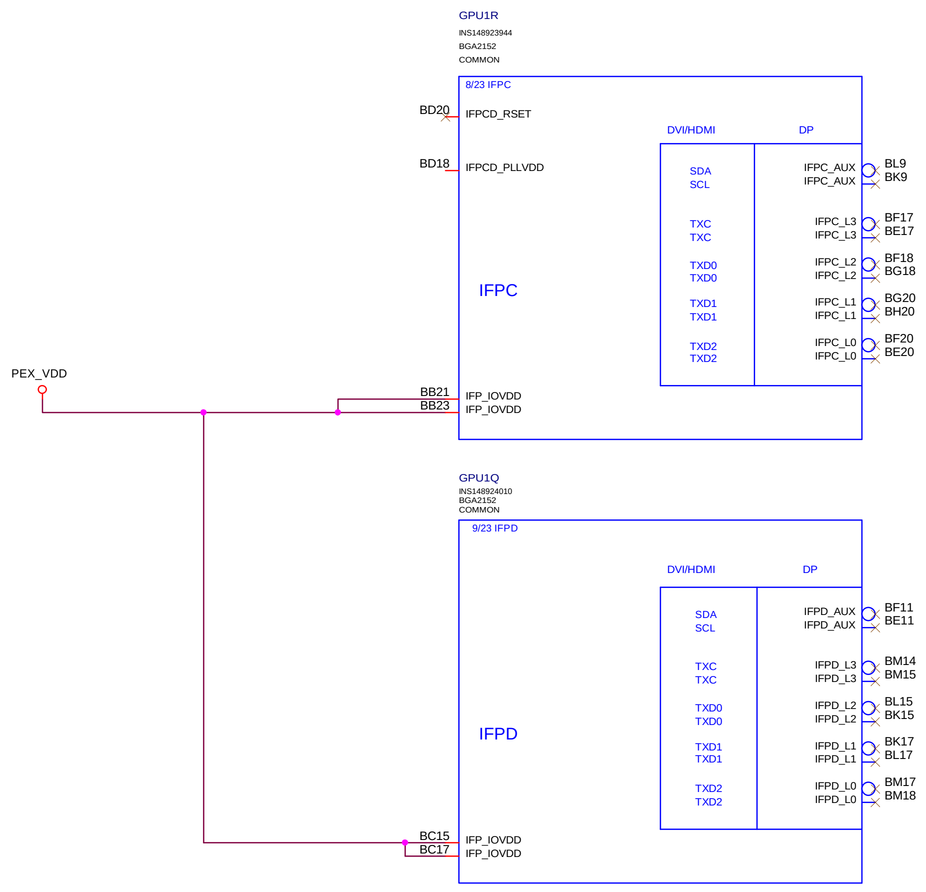

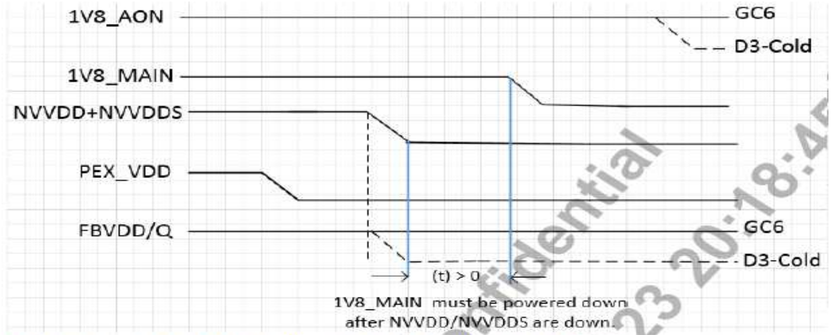

Figure 2. Example of Power-Down Sequencing Order

- NVDD, NVVDS, and PEX_VDD must power down before 1V8_MAIN, all other power rails can power down together with 1V8_MAIN.
- The propagation delay between 1V8_MAIN_EN and the NVVDD_EN pin needs to be less than 300 µs during both power up and power down.
- For GDDR5X, VPP must be equal to or higher than FBVDD/Q at all times; use gate logic and discharge circuit as needed.
- All 3.3V devices that connect to the GPU must be ramp down before 1V8_AON; GPU can NOT have any 3.3V leakage path after 1.8V_AON and 1.8V_MAIN power down.
- Power down 3V3 must be less than 10 percent before 1V8_AON can start ramp down

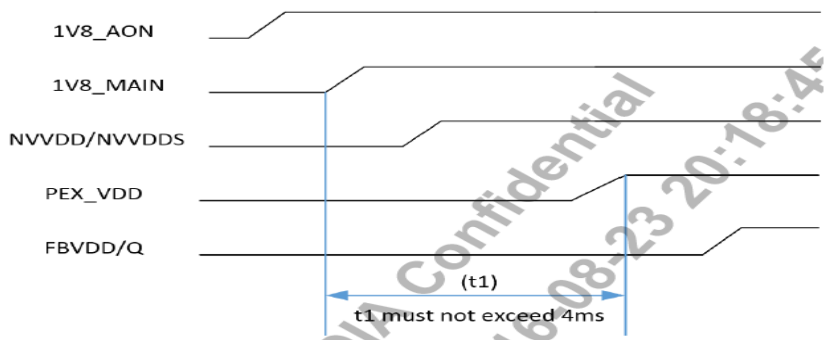

Figure 1. Example of Power-Up Sequencing Order

- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2 ms.
- t1 (from 1V8_MAIN_EN to PEX_VDD_Pgood) must *not* exceed 4 ms.
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- Power up NVVDD+NVVDDS must be 90 percent before PEX_VDD can start ramp up.
- Power up 1V8_AON must be 90 percent before 3V3 ramp up
- All 3.3V devices that connect to the GPU must be powered after 1V8_AON; GPU can NOT have any 3.3V leakage path before 1V8_AON present.
- No signal should be applied to the GPU before the power rails are fully ramped
- Refer to the JEDEC Memory Specification for memory related power sequencing.
- The propagation delay between 1V8_MAIN_EN and the NVVDD_EN pin needs to be less than 300 µs during both power up and power down.
- FBVDD/Q and 1V8_AON don't need power cycle for GC6 2.1

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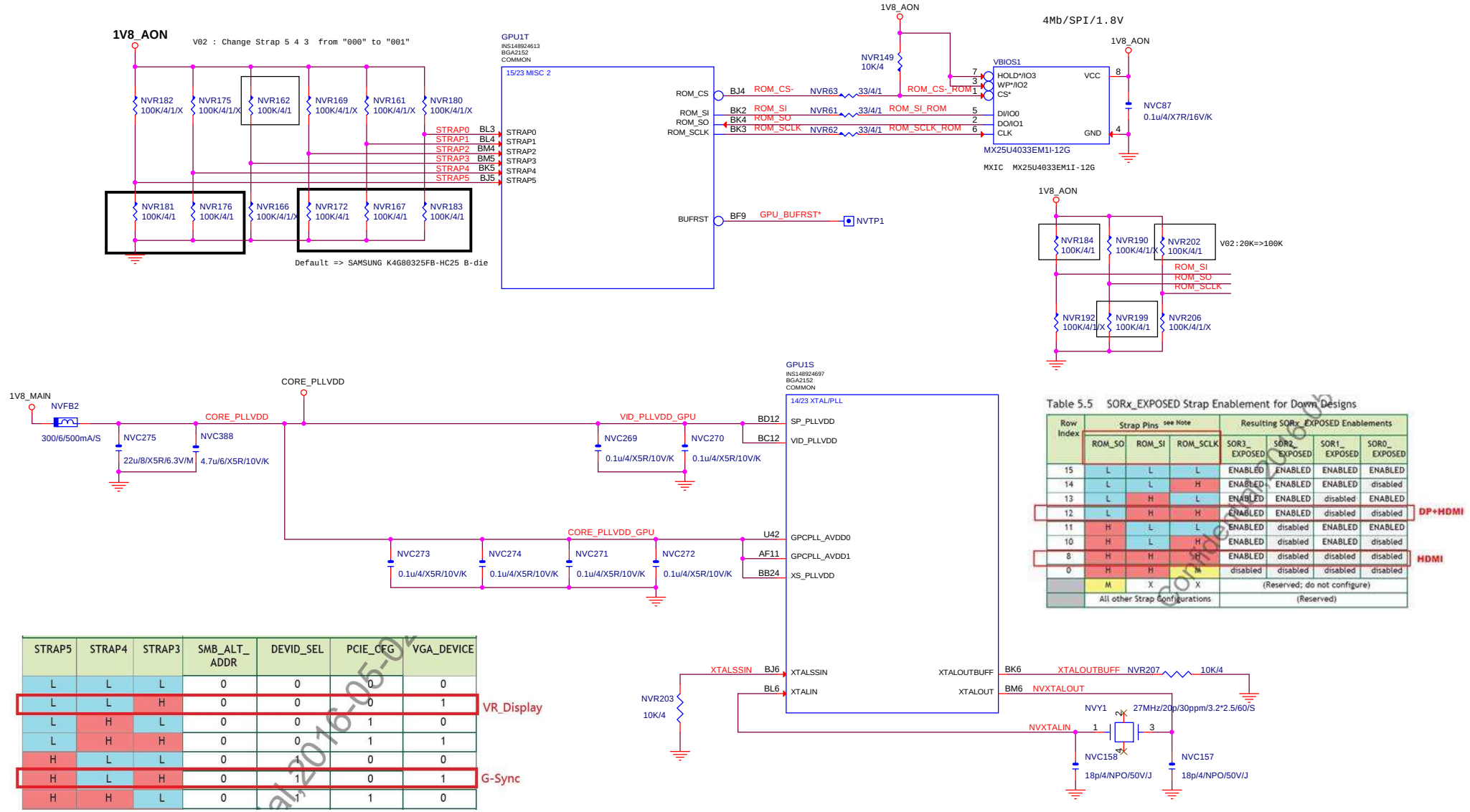

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements				
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED	
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled	
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED	
12	L	H	H	ENABLED	ENABLED	disabled	disabled	DP+HDMI
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED	
10	H	L	H	ENABLED	disabled	ENABLED	disabled	
8	H	H	L	ENABLED	disabled	disabled	disabled	HDMI
0	H	H	M	disabled	disabled	disabled	disabled	
	M	X	X	(Reserved; do not configure)				
	All other Strap Configurations			(Reserved)				

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
L	L	L	0	0	0	0	
L	L	H	0	0	0	1	VR_Display
L	H	L	0	0	1	0	
L	H	H	0	0	1	1	
H	L	L	0	1	0	0	
H	L	H	0	1	0	1	G-Sync
H	H	L	0	1	1	0	

Memory Type	FBVDD/ FBVDDQ	Memory Density	Allowed Memory Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V/ 1.35V and 1.55V/ 1.55V See Note 2	8 Gb	256Mx32	Samsung	K4G80325FB-HC25	B-die	0x0	4000	N/A	Production candidate
				Micron	MT51J256M32HF-80:A	A-die	0x1	4000	N/A	Production candidate
				Hynix	H5GQ8H24MJR-R4C	M-die	0x2	4000	N/A	Post-production candidate

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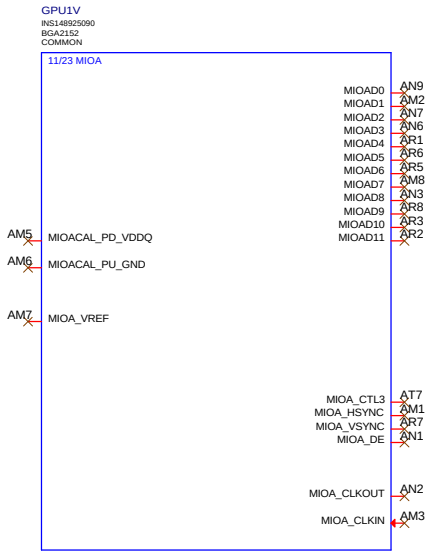

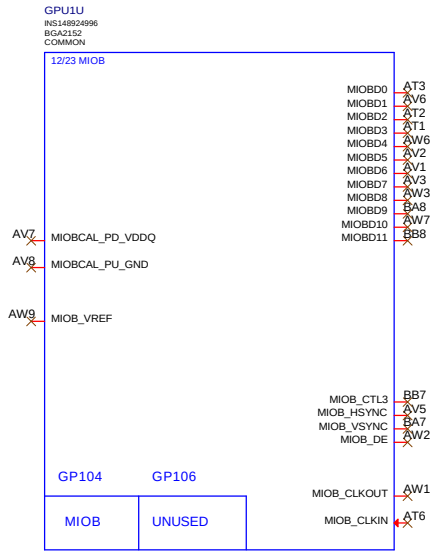

	GIGABYTE TECHNOLOGY COPORATION	
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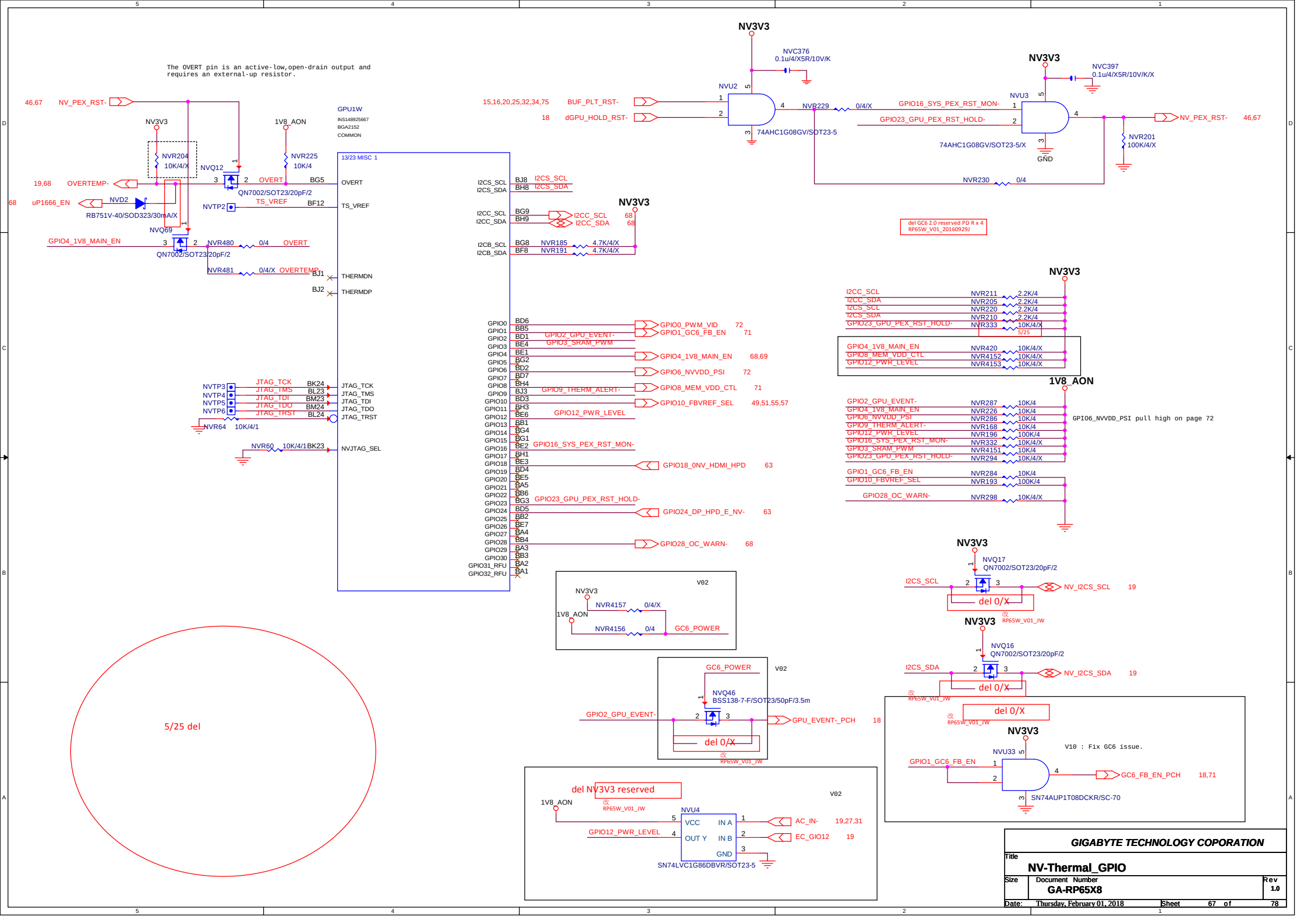
The OVERT pin is an active-low,open-drain output and requires an external-up resistor.
GPU1W
INS148925667
BGA2152
COMMON
13/23 MISC 1
NV3V3
1V8_AON
NVR204 10K/4/X
NVR225 10K/4
NVQ12
QN7002/SOT23/20pF/2
NVP2
RB751V-40/SOD323/30mA/X
NVD2
NVQ69
NVR480 0/4
NVR481 0/4/X
NVP3
NVP4
NVP5
NVP6
NVR64 10K/4/1
NVR60 10K/4/1
NVJTAG_SEL
NVC376 0.1u/4/X5R/10V/K
NVU2
74AHC1G08GV/SOT23-5
NVR229 0/4/X
NVC397 0.1u/4/X5R/10V/K/X
NVU3
74AHC1G08GV/SOT23-5/X
GND
NVR201 100K/4/X
NVR230 0/4
del GC6 2.0 reserved PD R x 4
RP65W_V01_20160929J
NVR211 2.2K/4
NVR205 2.2K/4
NVR220 2.2K/4
NVR210 2.2K/4
NVR333 10K/4/X
5/25
NVR420 10K/4/X
NVR4152 10K/4/X
NVR4153 10K/4/X
NVR287 10K/4
NVR226 10K/4
NVR286 10K/4
NVR168 10K/4
NVR196 100K/4
NVR332 10K/4/X
NVR4151 10K/4
NVR294 10K/4/X
NVR284 10K/4
NVR193 100K/4
NVR298 10K/4/X
GPIO6_NVVDD_PSI pull high on page 72
NVR185 4.7K/4/X
NVR191 4.7K/4/X
NVR4157 0/4/X
NVR4156 0/4
GC6_POWER
V02
NVQ46
BSS138-7-F/SOT23/50pF/3.5m
del 0/X
NVQ17
NVQ16
NVU4
VCC
IN A
IN B
OUT Y
GND
SN74LVC1G86DBVR/SOT23-5
del NV3V3 reserved
NVU33
SN74AUP1T08DCKR/SC-70
V10 : Fix GC6 issue.
5/25 del
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NV-Thermal_GPIO
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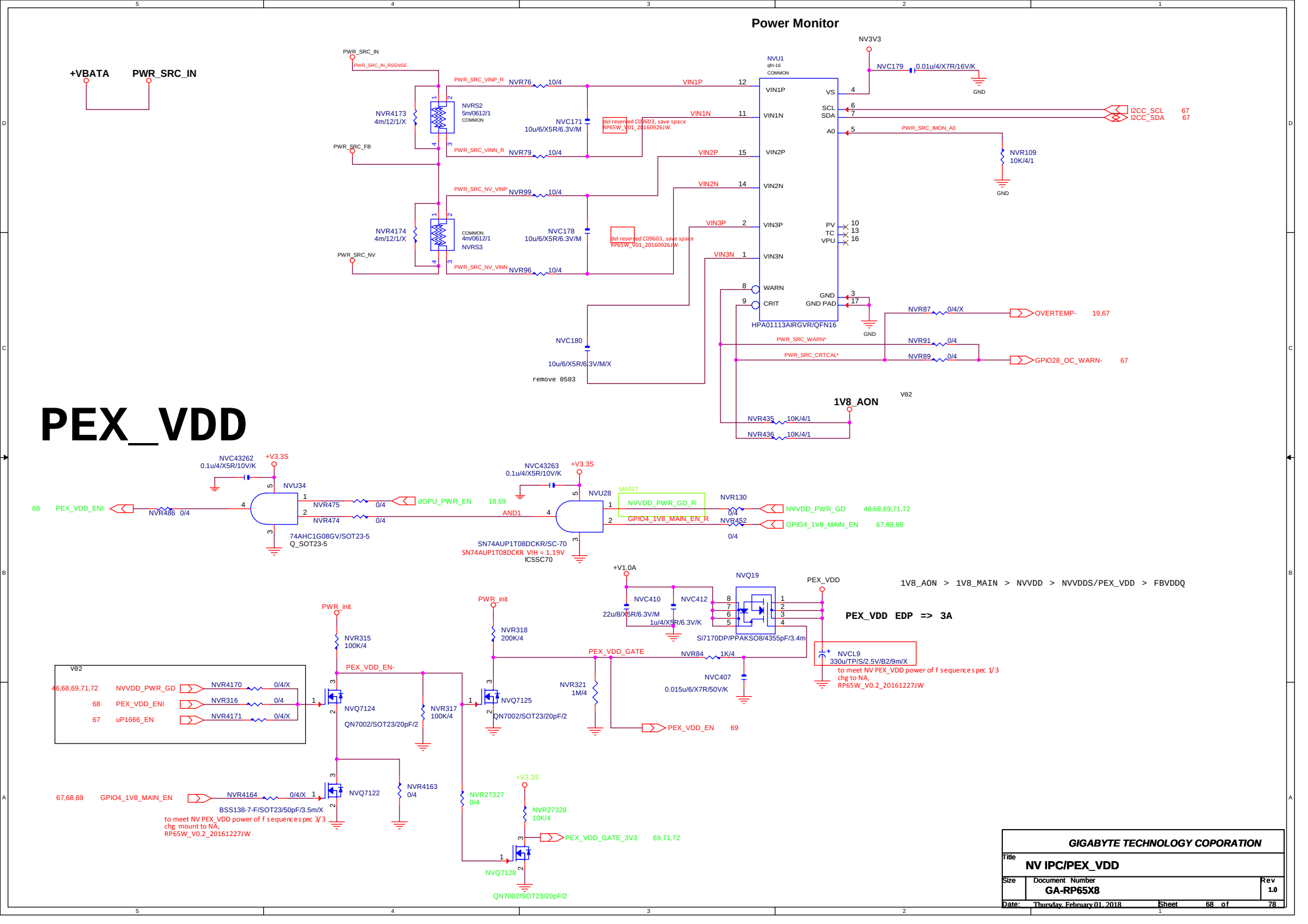
Power Monitor
+VBATA
PWR_SRC_IN
PWR_SRC_IN
PWR_SRC_IN_RSENSE
PWR_SRC_VINP_R
NVR76 10/4
NVRS2
5m/0612/1
COMMON
NVR4173
4m/12/1/X
NVC171
10u/6/X5R/6.3V/M
del reserved C09603, save space
RP65W_V01_20160926JW
PWR_SRC_VINN_R
NVR79 10/4
PWR_SRC_FB
PWR_SRC_NV_VINP
NVR99 10/4
NVR4174
4m/12/1/X
COMMON
4m/0612/1
NVRS3
NVC178
10u/6/X5R/6.3V/M
PWR_SRC_NV
PWR_SRC_NV_VINN
NVR96 10/4
NVU1
qfn-16
COMMON
VIN1P
VIN1N
VIN2P
VIN2N
VIN3P
VIN3N
WARN
CRIT
VS
SCL
SDA
A0
PV
TC
VPU
GND
GND PAD
HPA01113AIRGVR/QFN16
NV3V3
NVC179 0.01u/4/X7R/16V/K
GND
I2CC_SCL 67
I2CC_SDA 67
PWR_SRC_IMON_A0
NVR109
10K/4/1
NVR87 0/4/X
OVERTEMP- 19,67
PWR_SRC_WARN*
NVR91 0/4
PWR_SRC_CRTCAL*
NVR89 0/4
GPIO28_OC_WARN- 67
NVC180
10u/6/X5R/6.3V/M/X
remove 0503
V02
1V8_AON
NVR435 10K/4/1
NVR436 10K/4/1
PEX_VDD
NVC43262
0.1u/4/X5R/10V/K
+V3.3S
NVU34
68 PEX_VDD_ENI
NVR486 0/4
NVR475 0/4
NVR474 0/4
dGPU_PWR_EN 18,69
AND1
74AHC1G08GV/SOT23-5
Q_SOT23-5
NVC43263
0.1u/4/X5R/10V/K
NVU28
SA1027
NVVDD_PWR_GD_R
GPIO4_1V8_MAIN_EN_R
NVR130
NVR452
0/4
NVVDD_PWR_GD 46,68,69,71,72
GPIO4_1V8_MAIN_EN 67,68,69
SN74AUP1T08DCKR/SC-70
SN74AUP1T08DCKR VIH = 1.19V
IC5SC70
1V8_AON > 1V8_MAIN > NVVDD > NVVDDS/PEX_VDD > FBVDDQ
PEX_VDD EDP => 3A
+V1.0A
NVC410
22u/8/X5R/6.3V/M
NVC412
1u/4/X5R/6.3V/K
NVQ19
Si7170DP/PPAKSO8/4355pF/3.4m
NVCL9
330u/TP/S/2.5V/B2/9m/X
to meet NV PEX_VDD power of f sequences pec 1/3
chg to NA,
RP65W_V0.2_20161227JW
PWR_init
NVR315
100K/4
PEX_VDD_EN-
NVR318
200K/4
PEX_VDD_GATE
NVR84 1K/4
NVC407
0.015u/6/X7R/50V/K
NVR321
1M/4
PEX_VDD_EN 69
V02
46,68,69,71,72 NVVDD_PWR_GD NVR4170 0/4/X
68 PEX_VDD_ENI NVR316 0/4
67 uP1666_EN NVR4171 0/4/X
NVQ7124
QN7002/SOT23/20pF/2
NVR317
100K/4
NVQ7125
QN7002/SOT23/20pF/2
67,68,69 GPIO4_1V8_MAIN_EN
NVR4164 0/4/X
NVQ7122
BSS138-7-F/SOT23/50pF/3.5m/X
to meet NV PEX_VDD power of f sequences pec 3/3
chg mount to NA,
RP65W_V0.2_20161227JW
NVR4163
0/4
+V3.3S
NVR27327
0/4
NVR27328
10K/4
PEX_VDD_GATE_3V3 69,71,72
NVQ7128
QN7002/SOT23/20pF/2
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NV IPC/PEX_VDD
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PEX_VDD

1.8V Total= 0.9A

67,68,69 GPIO4_1V8_MAIN_EN
PWR_init
NVR78 100K/4
1V8_MAIN_EN
BSS138-7-F/SOT23/50pF/3.5m
NVQ5
GPIO4_1V8_MAIN_EN NVR4172 0/4
NVC7233 0.047u/4/X7R/16V/K/X
NVR74 100K/4
PWR_init
NVR82 100K/4
NVQ29
NVR80 1M/4/1
QN7002/SOT23/20pF/2
1V8_MAIN_EN_GATE 72
1V8_AON
1V8_MAIN
Si7170DP/PPAKSO8/4355pF/3.4m
NVQ4
NVC149 1u/4/X5R/6.3V/K
NVR189 10K/4/1
NVC431 10u/6/X5R/6.3V/M
NVC381 1n/6/X7R/50V/K
V10: NVC381 1nF; fix ramp up <40uS.
68,71,72 PEX_VDD_GATE_3V3
NVR422 0/4/X
NVQ33
QN7002/SOT23/20pF/2
NVC721 0.1u/6/X5R/10V/K
46,68,71,72 NVVDD_PWR_GD
NVR425 0/4

+V3.3S
NVC386 0.1u/4/X5R/10V/K
Disable 1V8_AON when over temp.
VPP=0.8x[(12.7+10)/10]=1.816
1V8_AON
V18R1 10K/4
1V8_AON_PG
V18U1
PGD GND EN ADJ VIN VOUT VDD GND NC
uP0104PSU8/SOP8/3A
V18C1 0.1u/4/Y5V/25V/Z/X
1V8_AON_ADJ
V18R2 12.7K/4/1
V18R4 10K/4/1
NVU8
18,68 dGPU_PWR_EN
NV3V3_PG
74AHC1G32DBVR/SOT23-5
V18R3 1K/4
1V8_AON_EN
V18C2 0.1u/4/Y5V/25V/Z/X
+V3.3A
+V5A
V18C3 10u/6/X5R/6.3V/M
V18C4 1u/6/X5R/6.3V/K
dGPU_PWR_EN V18R5 0/4/X
V18C5 47u/6/X5R/6.3V/M
V18C8 47u/6/X5R/6.3V/M
V18C7 100u/TAN/S/6.3V/B2

Power ON: 1V8_AON -> NV3V3 -> 1V8_MAIN -> NVVDD -> {NVVDDS / PEX_VDD} -> FBVDDQ
Power OFF : NVVDDS -> (PEX_VDD, NVVDD, FBVDDQ, 1V8_MAIN, NV3V3 ->1V8_AON)

NVVDD
PWR_init
NVR260 100K/4
NVQ25
QN7002/SOT23/20pF/2
dGPU_PWR_EN NVR295 0/4/X
NVR258 1M/4
NVC420 0.1u/4/Y5V/25V/Z
68 PEX_VDD_EN NVR296 0/4
GPIO4_1V8_MAIN_EN 67,68,69 NVR27392 0/4/X
NVR277 10/6/X
RP65W_V01_20151018J
NVQ24
QN7002/SOT23/20pF/2/X
1V8_MAIN
V10
NVR266 10/6
NVQ21
QN7002/SOT23/20pF/2
3. MaxQ -> NVVDDS merge into NVVDD. del NVVDDS discharge
PEX_VDD
PEX_VDD EDP => 3A
NVR280 4.7/12
NVQ26
Si7170DP/PPAKSO8/4355pF/3.4m
Chg R from 0402 to 1206, MOS to SOP8, to large current path RP65W_V0.2_20161227JW
FBVDDQ
PWR_init
NVR259 100K/4
NVR269 0/4/X
NVR279 10/6
Chg from 0402 to 0603, to large current path RP65W_V0.2_20161227JW
NVQ22
QN7002/SOT23/20pF/2
NVQ20
QN7002/SOT23/20pF/2
NVR267 1M/4/X
71 FBVDDQ_EN
NVC421 0.1u/4/Y5V/25V/Z/X
NVR257 10K/4/X

NV3V3
NVC389 0.1u/4/X5R/10V/K
NVU9
NVR415 1K/4
NV3V3_PG
NVC387 0.22u/4/X5R/10V/K
74AHC1G08GV/SOT23-5
V02:0.1uF=>0.22uF

+V3.3S
NVC7234 0.1u/4/X5R/10V/K
NVU32
GPIO4_1V8_MAIN_EN
NV3V3
1V8_MAIN_EN
SN74AUP1T08DCKR/SC-70/X
V10 : Change NVU32,38,29 footprint from Q_SOT23-5 to IC5SC70.

AE update new power sequence.
20161013

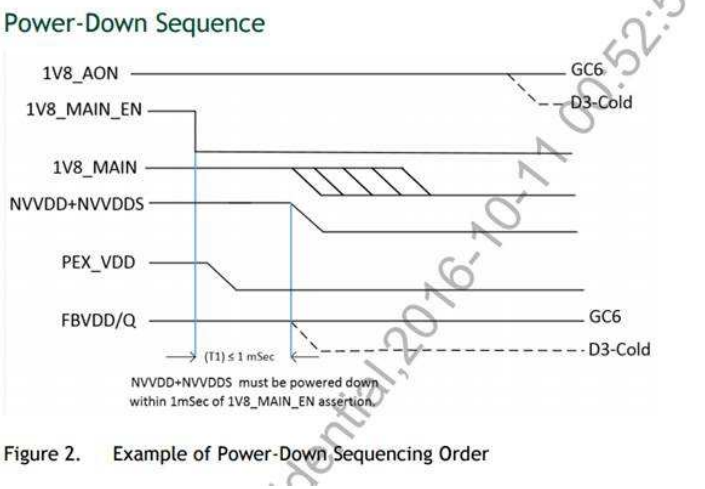

Figure 2. Example of Power-Down Sequencing Order

+V3.3S
NVC7224 0.1u/4/X5R/10V/K
NVU29
1V8_AON_PG
dGPU_PWR_EN
1V8_AON_PG_R
SN74AUP1T08DCKR/SC-70
1V8_AON_PG
NVR337 0/4/X
1V8_AON_PG_R
PWR_init
NVR334 100K/4
NVC382 1u/4/X5R/6.3V/K
NV3V3
NVQ49
AO3404A/SOT23/448pF/25m
NVR335 10K/4
NVC385 1n/6/X7R/50V/K
V10: NVC385 1nF. fix ramp up <40uS.
This cap is reserved for delay NV3V3 timing.
PWR_init
NVR336 100K/4
NVQ48A
BSS138DW-7-F/SOT363/3.5
NVQ48B
BSS138DW-7-F/SOT363/3.5
dGPU_PWR_EN
NVQ32
QN7002/SOT23/20pF/2/X
NVR413 0/4

Power ON: 1V8_AON -> NV3V3 -> 1V8_MAIN -> NVVDD -> {NVVDDS / PEX_VDD} -> FBVDDQ
Power OFF : NVVDDS -> (PEX_VDD, NVVDD, FBVDDQ, 1V8_MAIN, NV3V3 ->1V8_AON)

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Title	**NVVDDS**
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Power ON: 1V8_AON -> NV3V3 -> 1V8_MAIN -> NVVDD -> {NVVDDS / PEX_VDD} -> FBVDDQ

Power OFF : NVVDDS -> (PEX_VDD, NVVDD, FBVDDQ, 1V8_MAIN, NV3V3 ->1V8_AON)

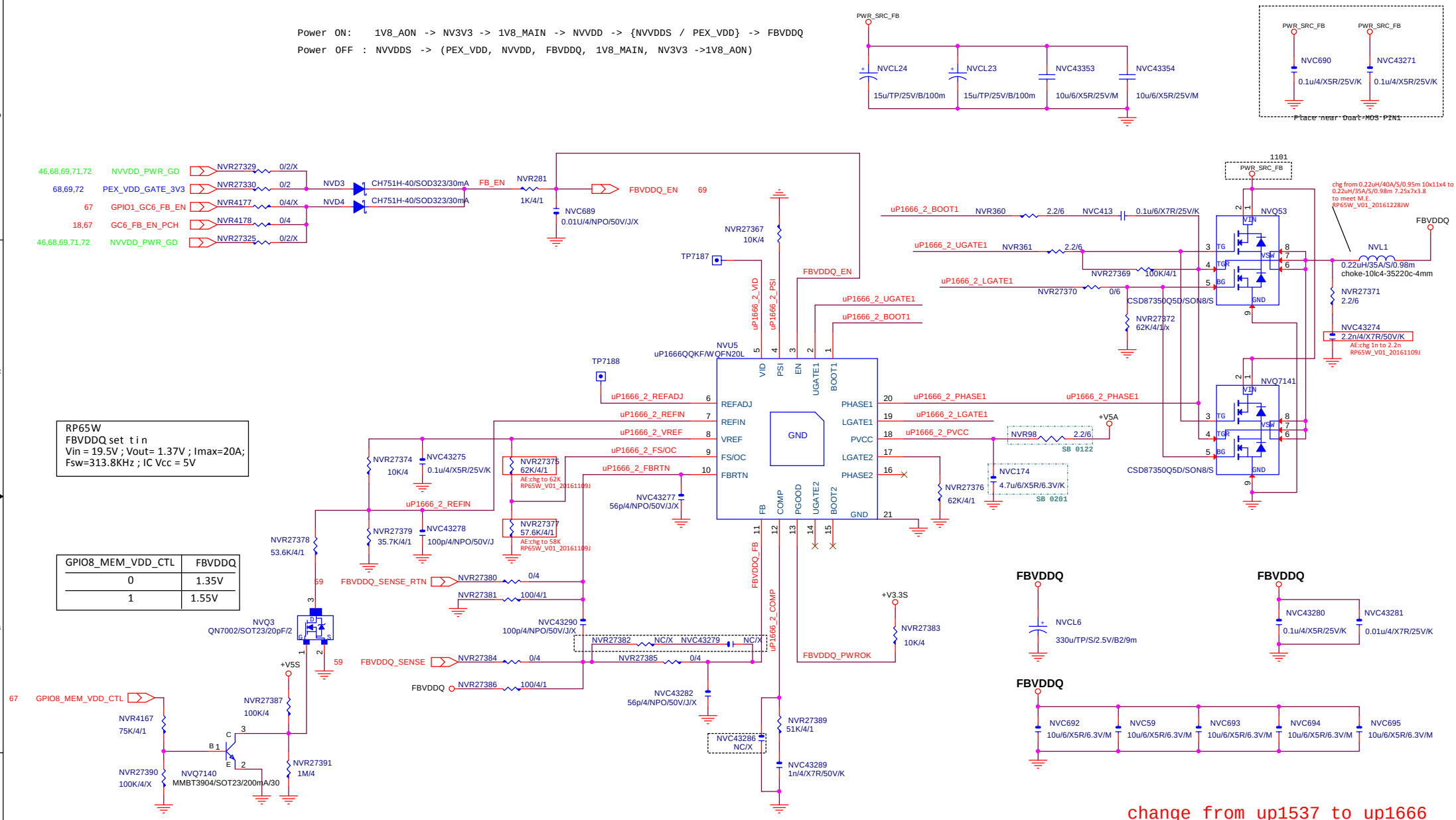

Table 11. Output EDP-Continuous

Product	TGP (W)	NVVDD NVVDDS - (A)	GPU FBIO (A)	FB TOTAL[5] (A)	1.0V Total[1] 1.0V[4] (A)	1.8V Total[2] 1.8V[4] (A)
N17E-G3 MAX-Q	80	76.4	17.1	32.8	0.8	1.6
N17E-G2 MAX-Q	80	79.1	14.6	25.0	0.8	1.6
N17E-G1 MAX-Q	60	62.8	12.6	19.8	0.8	1.6

Table 12. Output EDP-Peak

Product	TGP (W)	NVVDD NVVDDS - (A)	GPU FBIO (A)	FB TOTAL[5] (A)	1.0V Total[1] 1.0V[4] (A)
N17E-G3 MAX-Q	80	180	20.9	47.3	1.1
N17E-G2 MAX-Q	80	180	15.7	30.6	1.1
N17E-G1 MAX-Q	60	160	15.0	32.2	1.1

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Title: FBVDDQ

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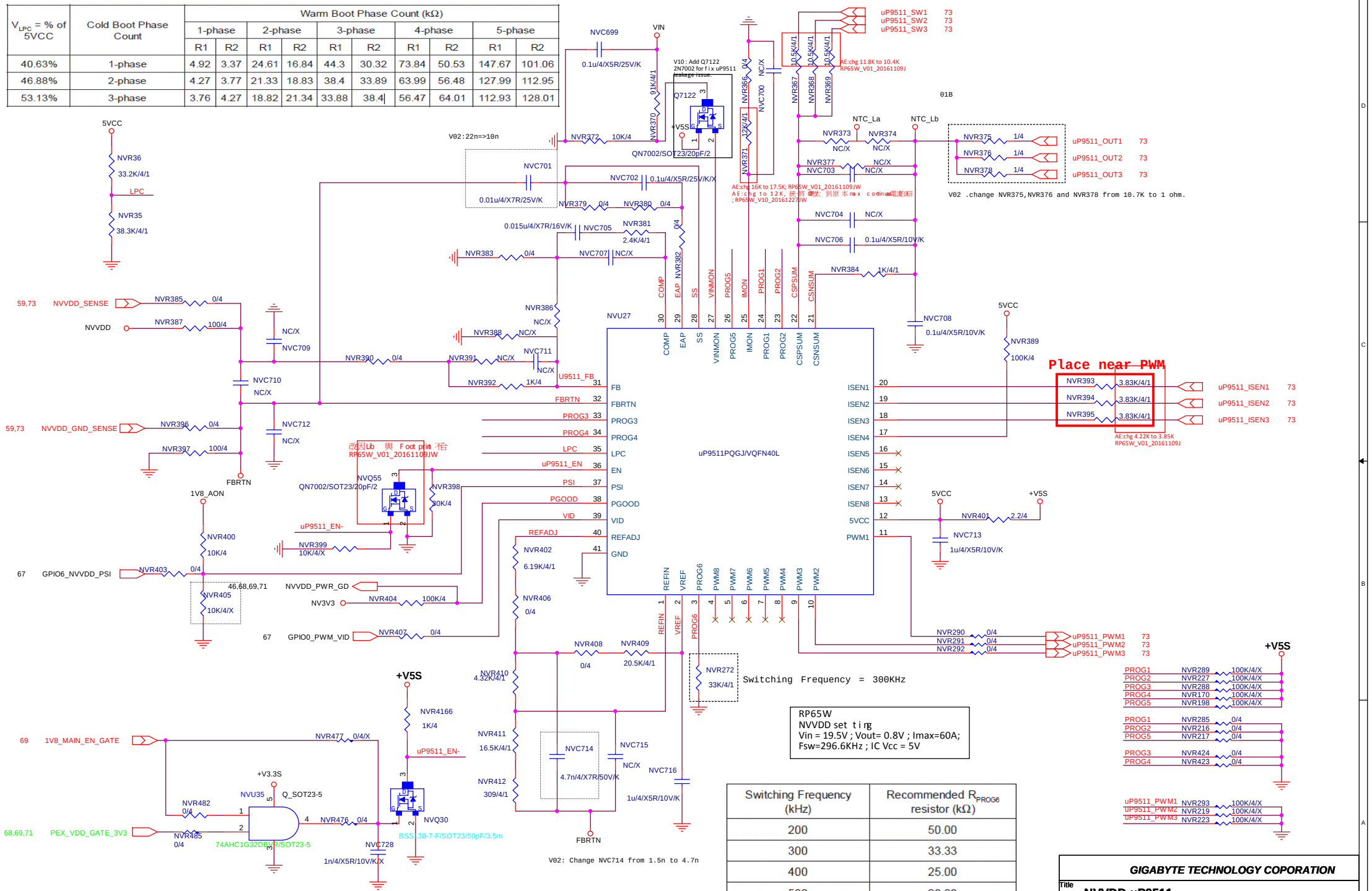
V_{LPC} = % of 5VCC	Cold Boot Phase Count	Warm Boot Phase Count (kΩ)									
		1-phase		2-phase		3-phase		4-phase		5-phase	
		R1	R2	R1	R2	R1	R2	R1	R2	R1	R2
40.63%	1-phase	4.92	3.37	24.61	16.84	44.3	30.32	73.84	50.53	147.67	101.06
46.88%	2-phase	4.27	3.77	21.33	18.83	38.4	33.89	63.99	56.48	127.99	112.95
53.13%	3-phase	3.76	4.27	18.82	21.34	33.88	38.4	56.47	64.01	112.93	128.01



Switching Frequency (kHz)	Recommended R_{PROG6} resistor (kΩ)
200	50.00
300	33.33
400	25.00
500	20.00
600	16.67

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Title: NVVDD-uP9511

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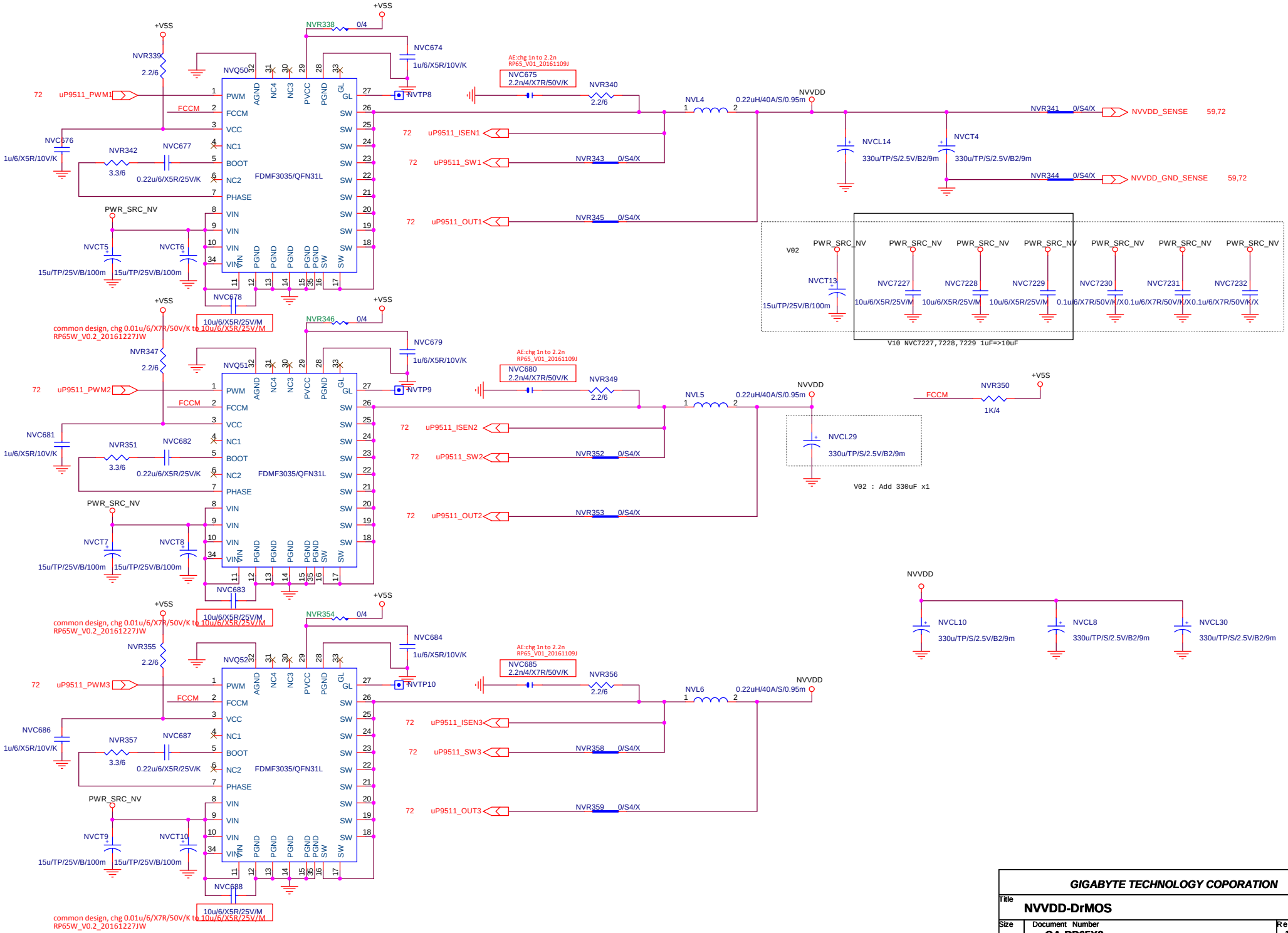

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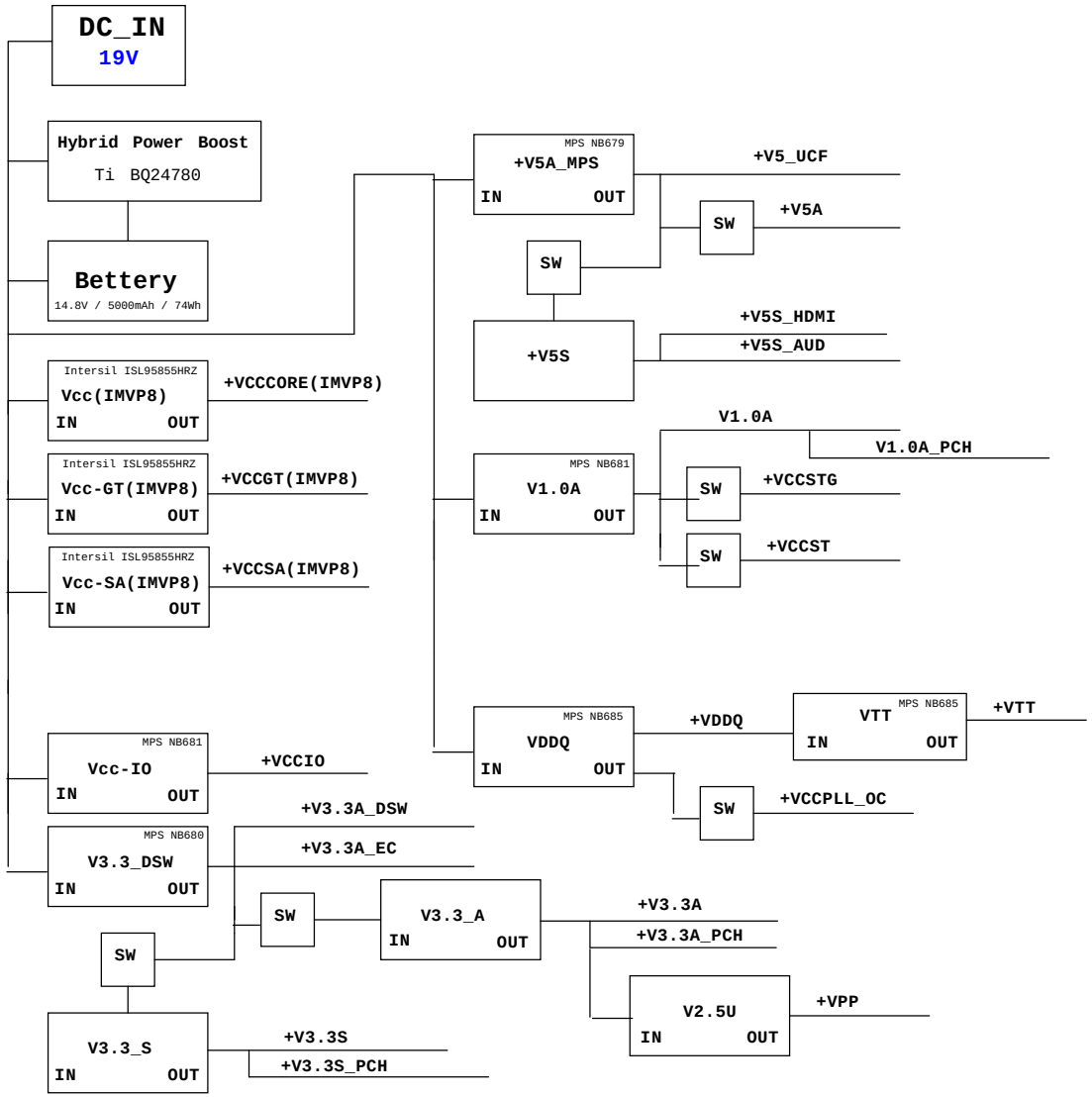
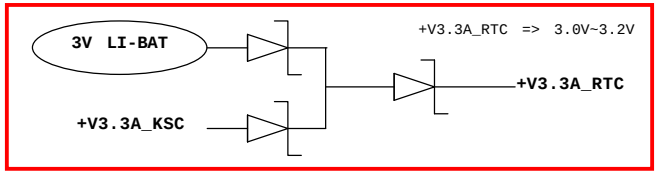
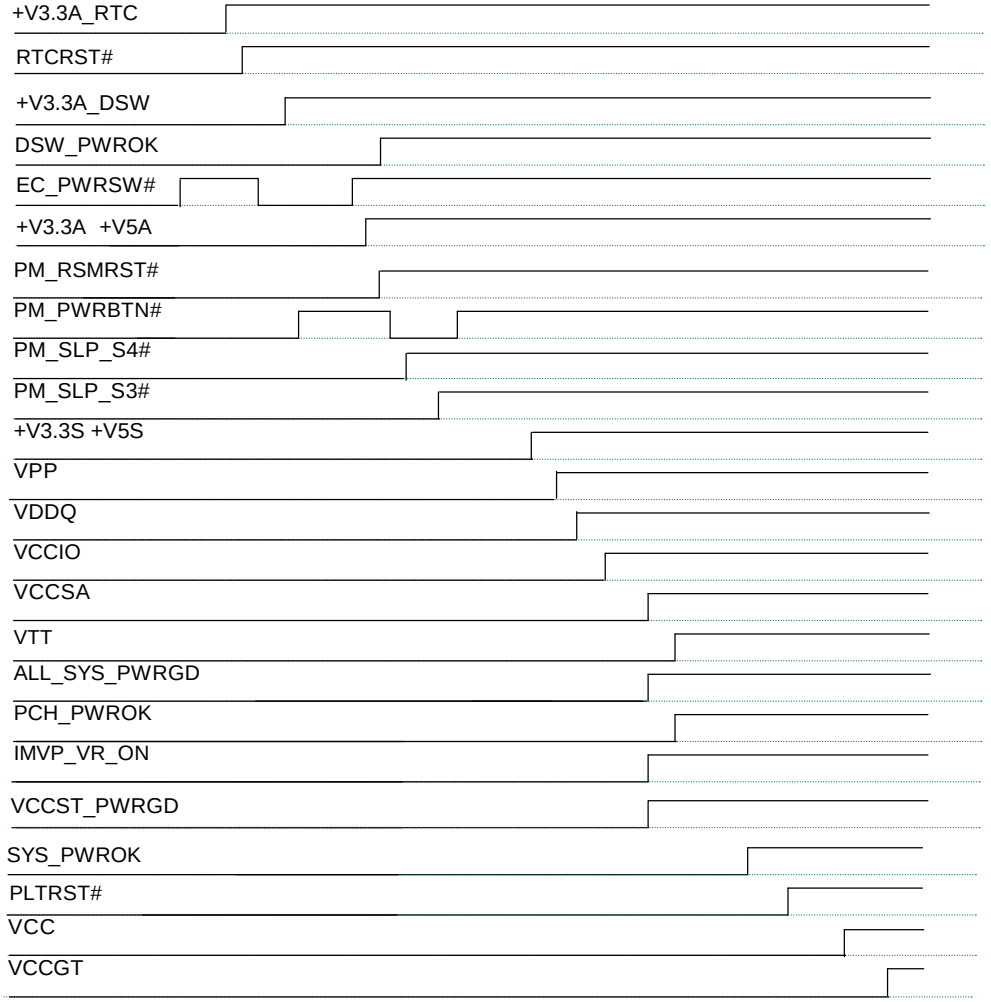
Powerup Sequence







GIGABYTE TECHNOLOGY COPORATION

Title: Change_Note

Size | Document Number: GA-RP65X8 | Rev: 1.0

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INTEL AR C version module (TBT + U31A) SCH 0.3 (2016/07/17) 4 Layers

Base on INTEL AR reference SCH 1.7 (2016/05/24)

PCIE X4

PCIE GEN3

CLKREQ should be checked again

EX DP Input (DP + AUX)

RP65 改 Footprint

SINK PORT 0

SINK PORT 1

SOURCE PORT 0

LC GPIO

POC GPIO

MISC

TBT PORTS

PORT A

PORT B

POC

DEBUG

PCIE_RBIAS THR20 should be placed as close as Alpine Ridge and keep traces as short as possible.

DP differential 100 ohm

Assemble THR72 if DPSRC NOT in USE

Assemble THR25 if DPSRC NOT in USE

TBT_CIO_PLUG_EVENT_N uses PCH GPIO with SMI#

GPIO Link for
- Plug Event
- Force Power Board Link for
- PCIE Wake
- S3

* 1211

* 0811

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For INTEL IDC Certification uesd, MP remove!!

THU1A
JHL6340/FCCSP/S
THUNDERBOLT JHL6340 INTEL
10HB2-G06340-21R

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Title	ALPINE RIDGE CIO & DP
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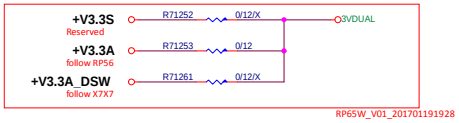
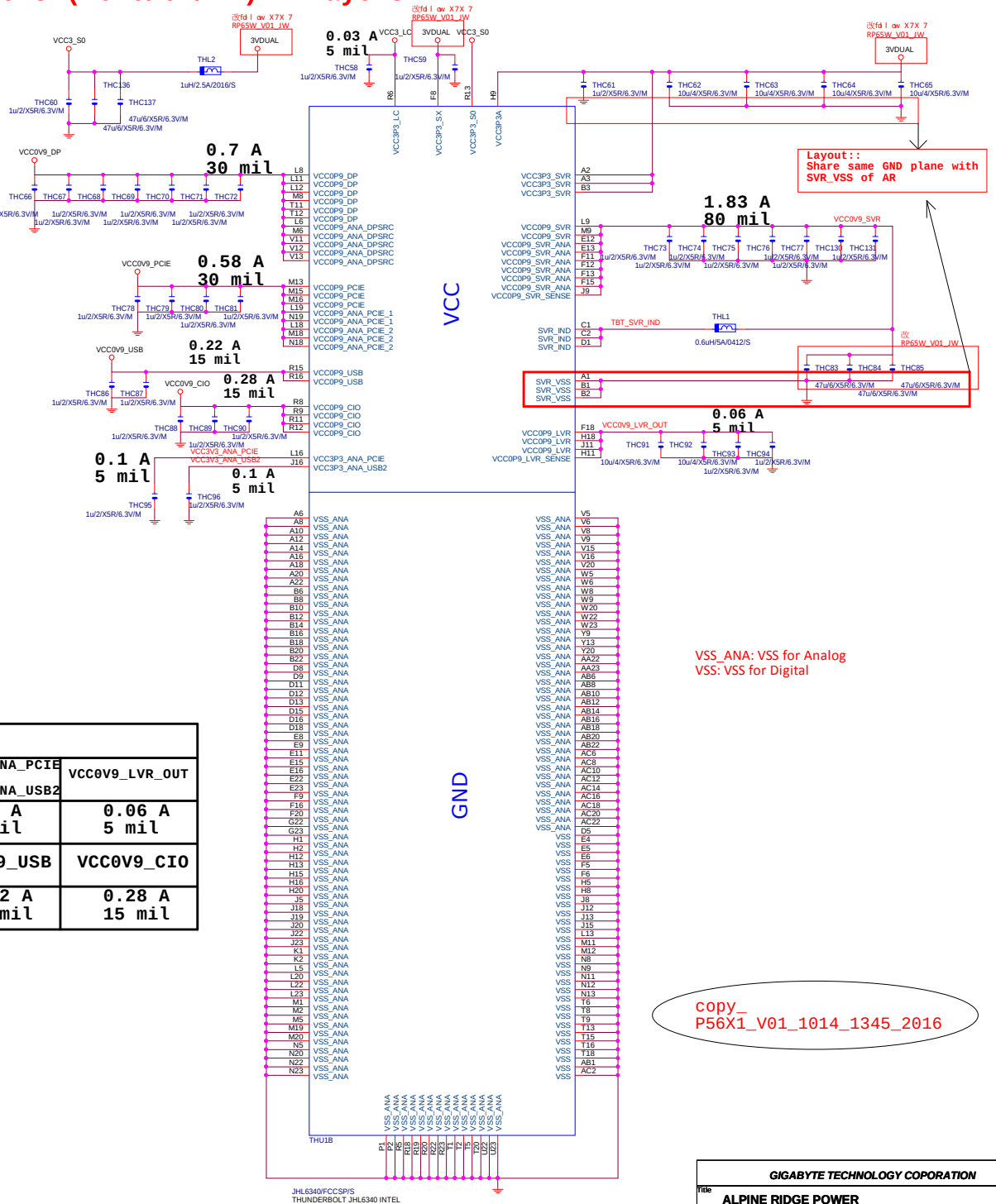
INTEL AR C version module (TBT + U31A) SCH 0.3 (2016/07/17) 4 Layers

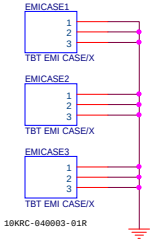
Base on INTEL AR reference SCH 1.7 (2016/05/24)





Power Consumption Table

	VCC3	3VDUAL	VCC3_LC	VCC3V3_ANA_PCIE VCC3V3_ANA_USB2	VCC0V9_LVR_OUT
Max Current(A)	1.05 A 40 mil	0.19 A 10 mil	0.03 A 5 mil	0.1 A 5 mil	0.06 A 5 mil
	VCC0V9_SVR	VCC0V9_DP	VCC0V9_PCIE	VCC0V9_USB	VCC0V9_CIO
Max Current(A)	1.83 A 80 mil	0.7 A 30 mil	0.58 A 30 mil	0.22 A 15 mil	0.28 A 15 mil



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GIGABYTE TECHNOLOGY COPORATION		
Title: ALPINE RIDGE POWER		
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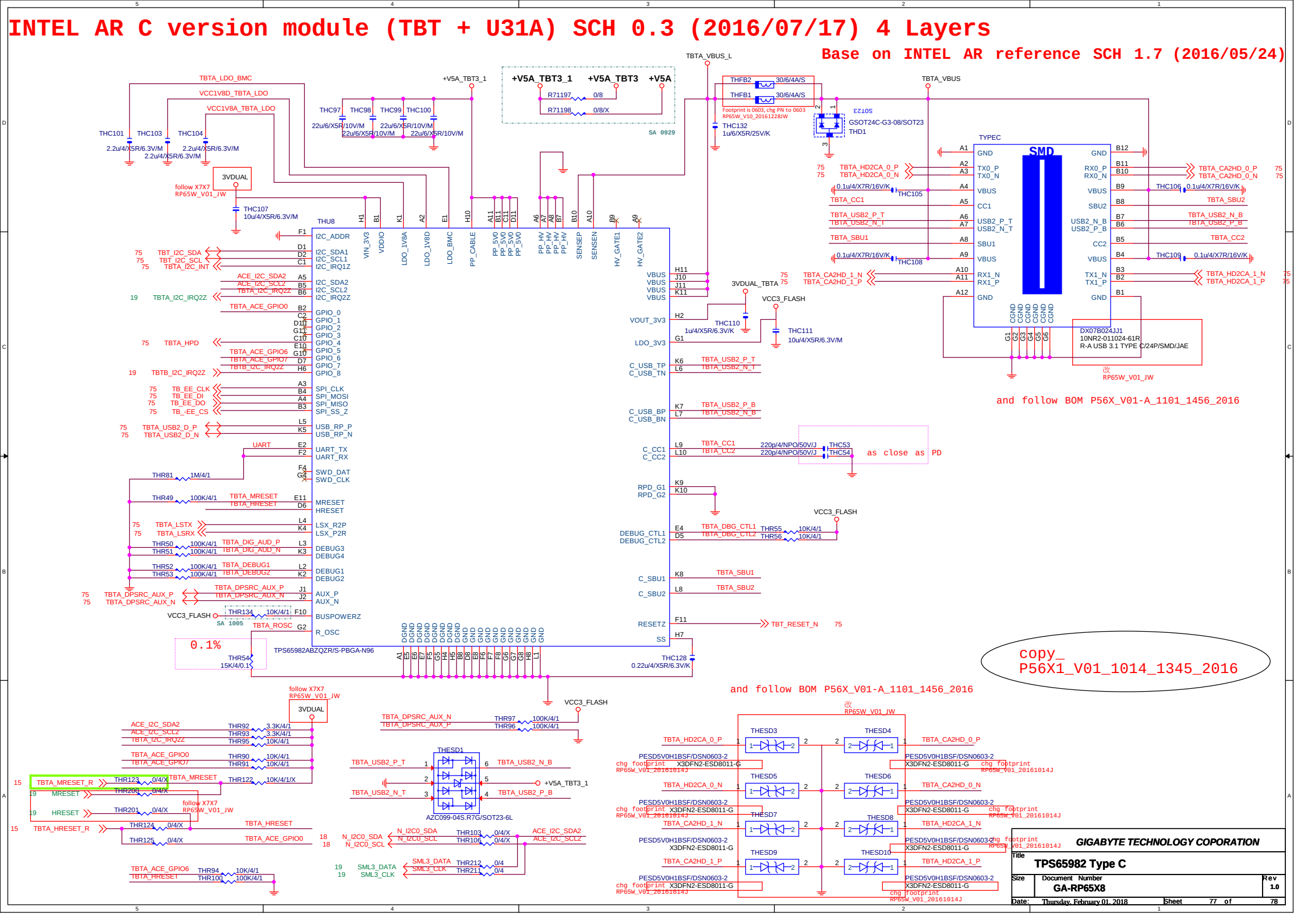
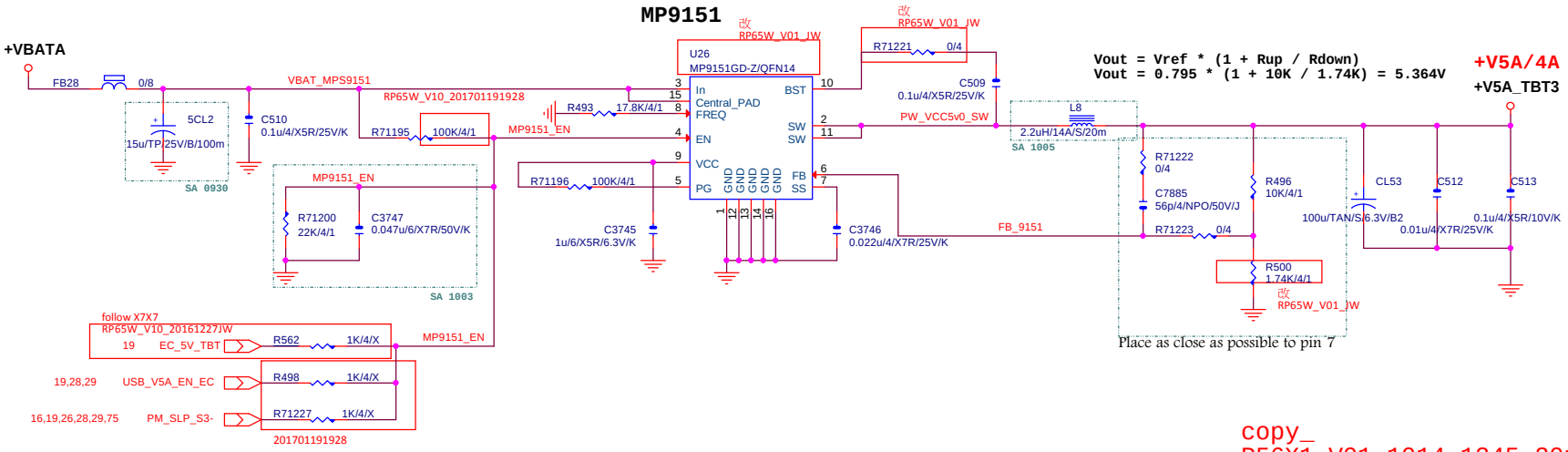
INTEL AR C version module (TBT + U31A) SCH 0.3 (2016/07/17) 4 Layers

Base on INTEL AR reference SCH 1.7 (2016/05/24)





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GIGABYTE	GIGABYTE TECHNOLOGY COPORATION	
	Title: +V5A_TBT3	
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