Model:SKYLAKE-U AIO
PCB Version:-1
PCB Number:14091
PCB P/N:
SCH Version:
ECO# number : 826756

BOM Configuration
(R_):UNMOUNT
(G_):GPU
(U_):UMA
(T_):TOUCH
(C_):REAR IO CONN(non-battery)
(X_):XDP & DEBUG USE(REMOVE AT 1A)
(D_):DEBUG USE(REMOVE AT MP)
(B_):BATTERY

PCB BOARD SIZE
6 Layers
185mm X 230mm

SA BUILD

Intel SKL-U Platform

LAN : Gb LAN RTL8111H

AUDIO: ALC3661

SIO_EC:ITE8739

<Variant Name>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

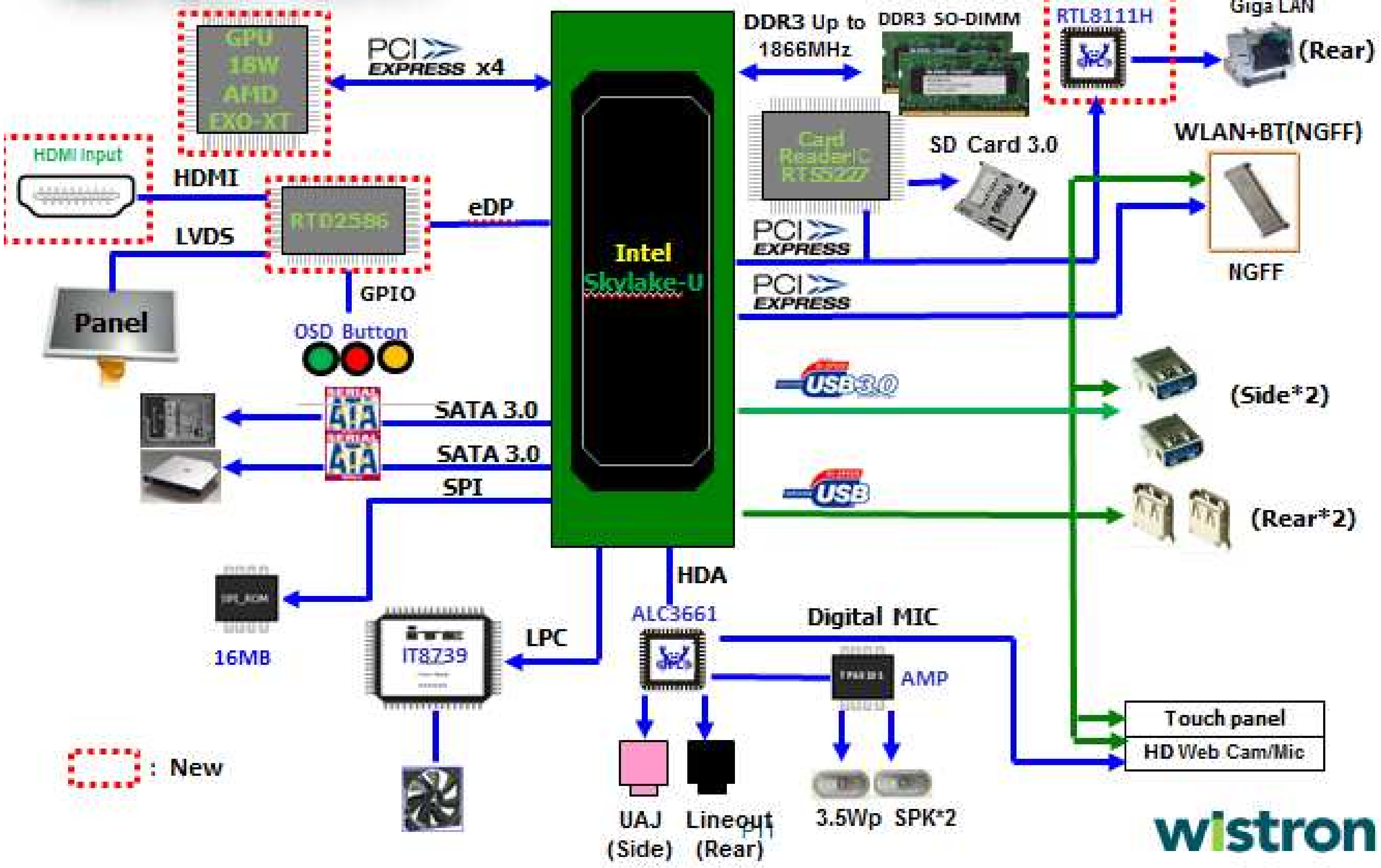
Title	001_Cover Page		
Size C	Document Number Rosa_SKL-U AIO		Rev -1
Date: Wednesday, July 01, 2015	Sheet 1 of 105		

Project Name: Jasmine-SKL-U AIO
Project Code: 3PD026010001
PCB Version: -1
PCB Number :14091

PCB BOARD SIZE
185mm X 230mm
6 Layer

Internal Slot/Header
Front/Rear IO
Chipset

Block Diagram for Intel SKL-U



<Variant Name>

wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	002_Block Diagram	
Size C	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 2 of 105	

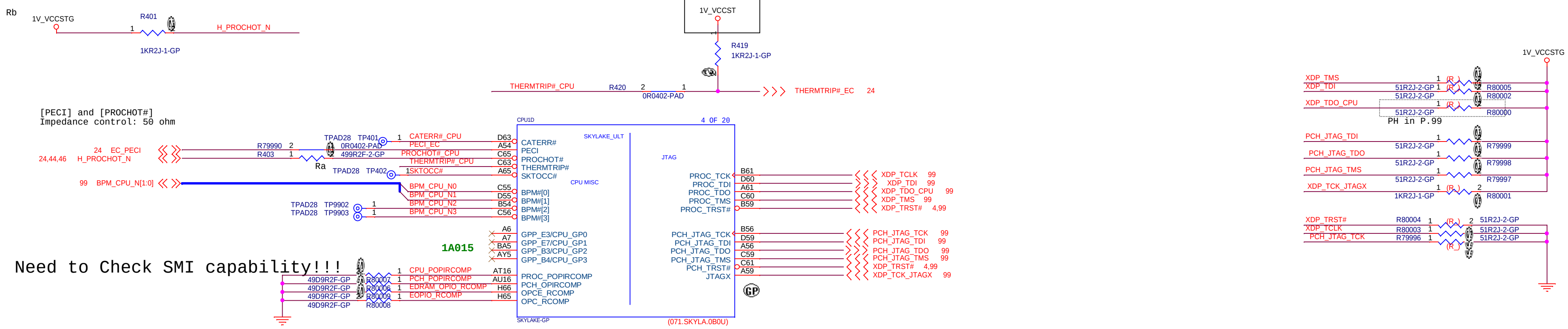
Blanking

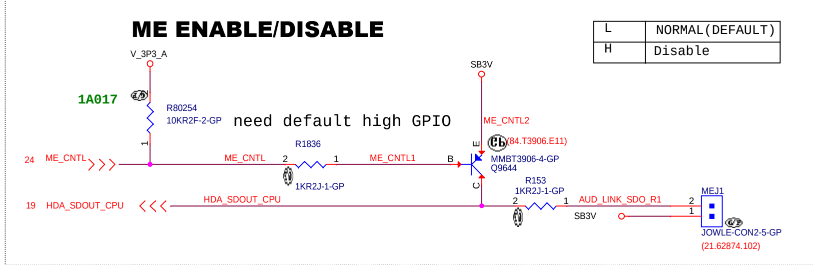
<Variant Name>

wistron		**Wistron Incorporated** 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	003_(Reserved)		
Size A	Document Number Rosa_SKL-U AIO		Rev -1
Date:	Wednesday, July 01, 2015	Sheet 3 of 105	

Main Func = CPU

#543016 Rev0.7: Ra = 500 ohm / Rb = 1k ohm
#544669 Rev0.52:
Ra = 56 ohm (TO BE CHANGED TO 100 OHMS) / Rb = 62 ohm and 150 ohm





L	NORMAL(DEFAULT)
H	Disable

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 004_CPU(JTAG/CPU SIDE BAND)

Size: C
Document Number: Rosa_SKL-U AIO
Rev: -1

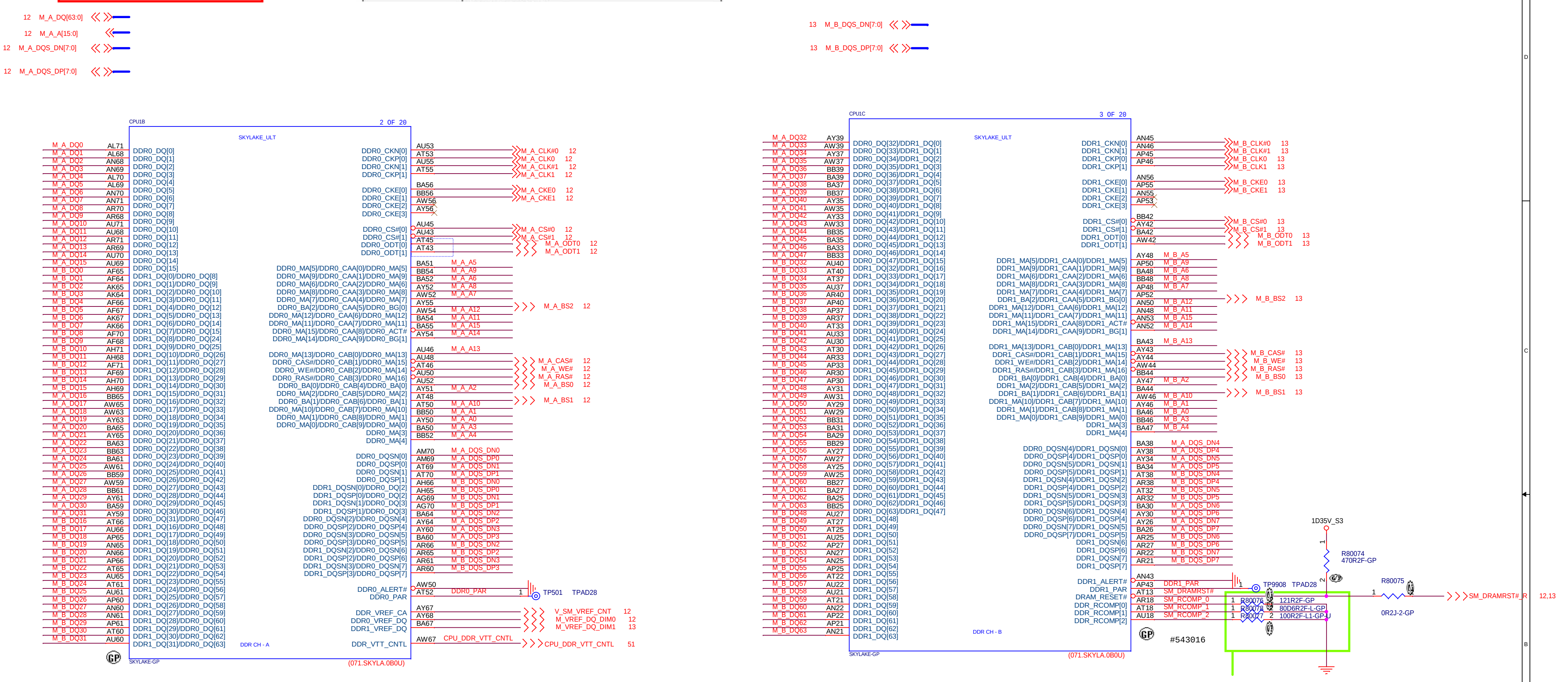
Date: Wednesday, July 01, 2015

Skylake-U DDR3L/RS SO-DIMM Checklist (Sheet 2 of 2)

Pin Name	Schematic Notes
DDR0_ODT[1:0]/ DDR1_ODT[1:0]	No Connect at processor side
ODT[1:0]	SO-DIMM connector ODT[1:0] pins tied to VDDQ through a FET and a resistor

DDR3L ball type: Non-Interleaved Type

Main Func = CPU



<Variant Name>

wistron

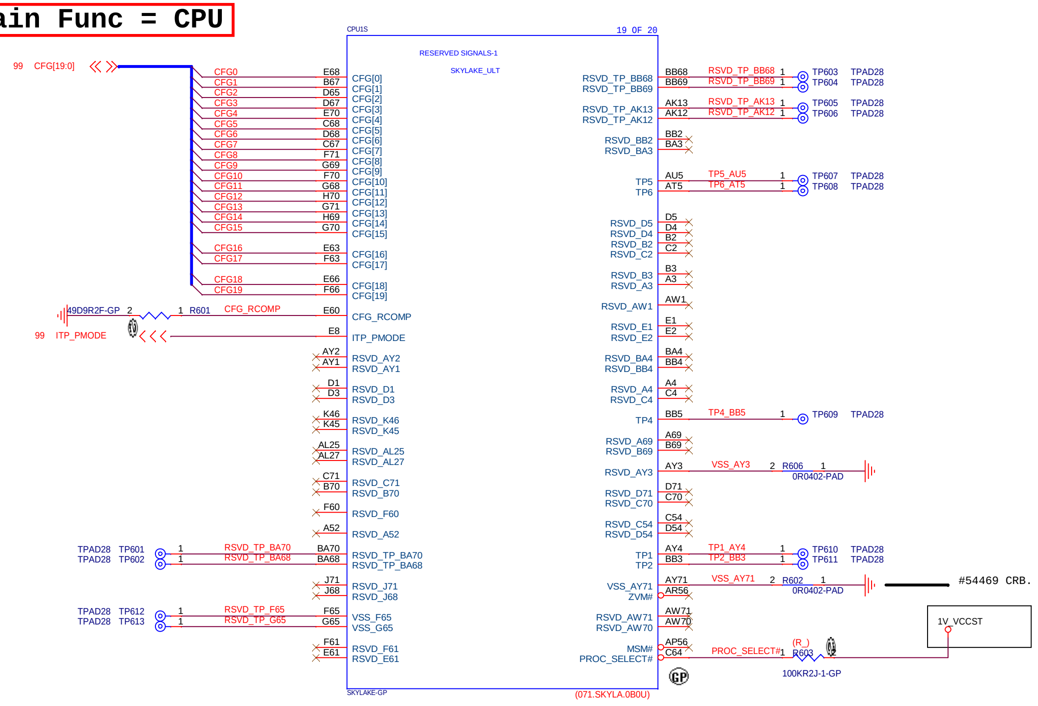
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 005_CPU(DDR3L)(NEW)

Size	Document Number	Rev
C	Rosa_SKL-U AIO	-1

Date: Wednesday, July 01, 2015 Sheet 5 of 105

Main Func = CPU



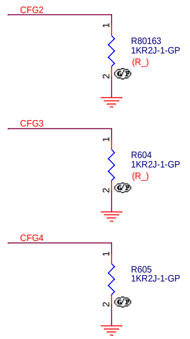
#54469 CRB.

Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

#543016

PCH strap pin:



[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

(#543016)

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 006_CPU_(CFG)

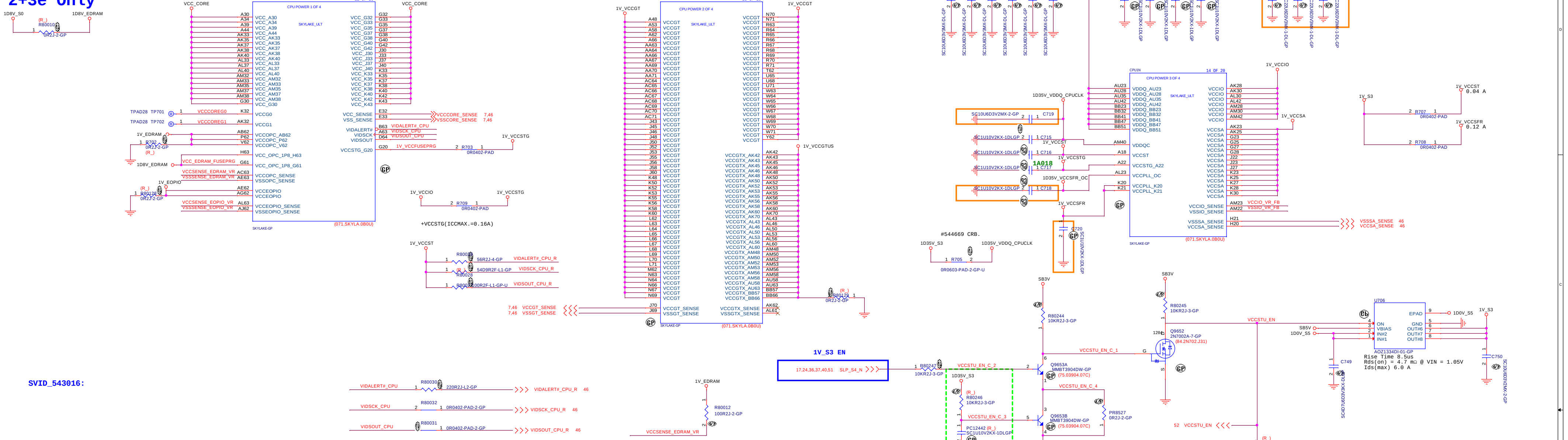
Size: C | Document Number: Rosa_SKL-U AIO | Rev: -1

Date: Wednesday, July 01, 2015 | Sheet 6 of 105

Main Func = CPU

+V_EOPIO_VR and +V_EDRAM_VR powere source from 1D0V_S0

2+3e Only

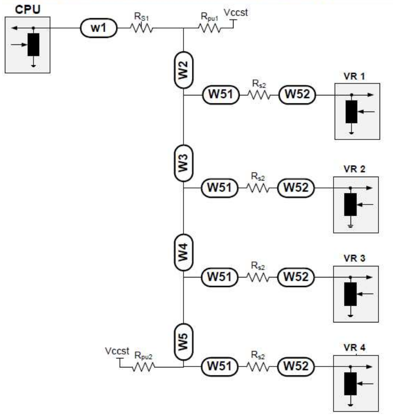


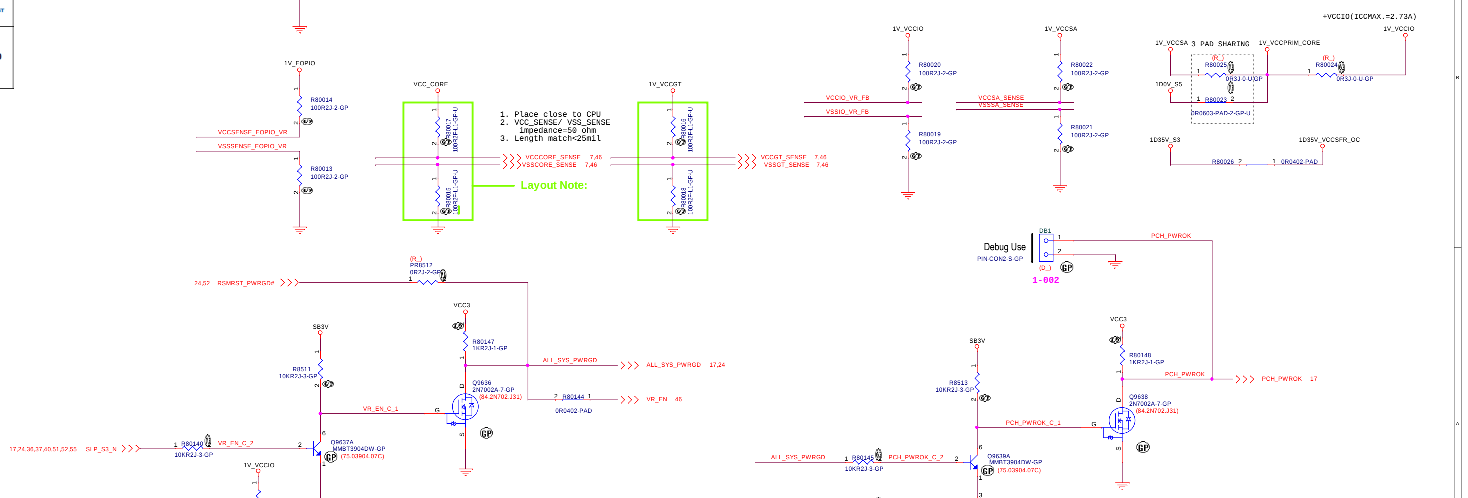
MANAGEMENT RAIL POWER GENERATION

Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

Figure 10-7. Routing Illustration for SVID Topology





Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 007_CPU(POWER)

Size: D | Document Number: Rosa_SKL-U AIO | Rev: -1

Date: Wednesday, July 01, 2015 | Sheet 7 of 105

Main Func = CPU

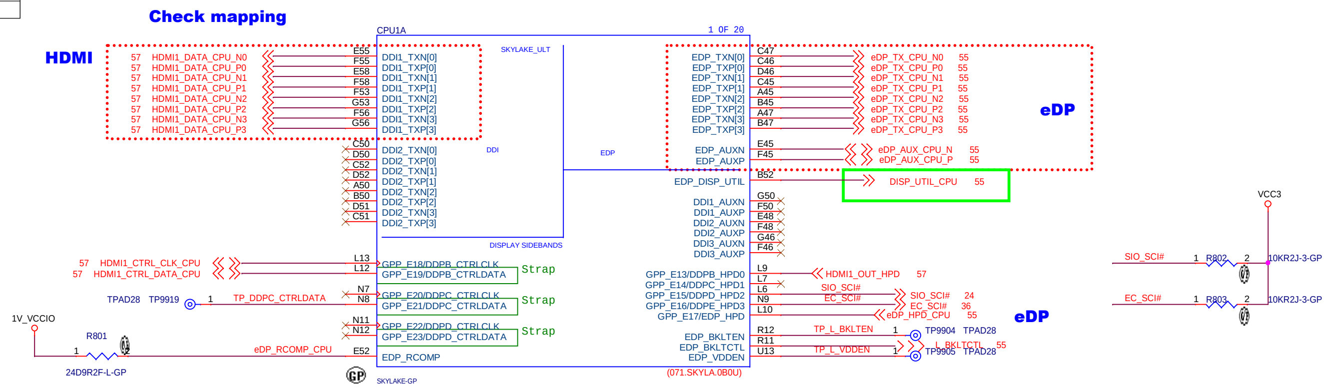
Table 5-10. DDI Disabling and Termination Connections

Pin Name	Recommendation
DDPB_AUXP DDPC_AUXP	No Connect
DDPB_AUXN DDPC_AUXN	No Connect
DDPB_HPD DDPC_HPD	No Connect
DDI1_TXP[3:0] DDI2_TXP[3:0]	No Connect
DDI1_TXN[3:0] DDI2_TXN[3:0]	No Connect
DDPB_CTRLCLK DDPB_CTRLDATA	No Connect
DDPC_CTRLCLK DDPC_CTRLDATA	No Connect

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

These two signals have weak internal pull-down.



<Variant Name>	
wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	008_CPU(DISPLAY)
Size C	Document Number Rosa_SKL-U AIO — Rev -1
Date: Wednesday, July 01, 2015	Sheet 8 of 105

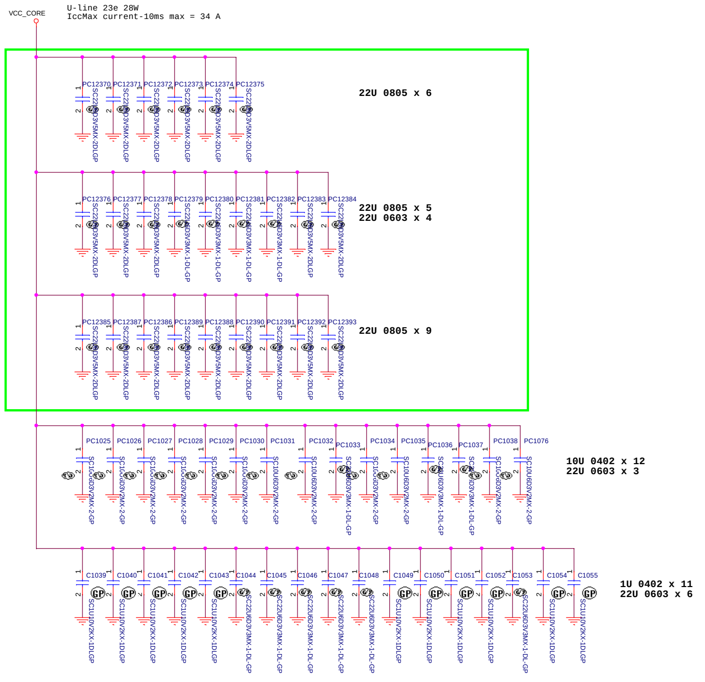
Blanking

<Variant Name>

Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	009_(Reserved)
Size B	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 9 of 105

Main Func = CPU

CORE CAP follow Cap_Sorting list



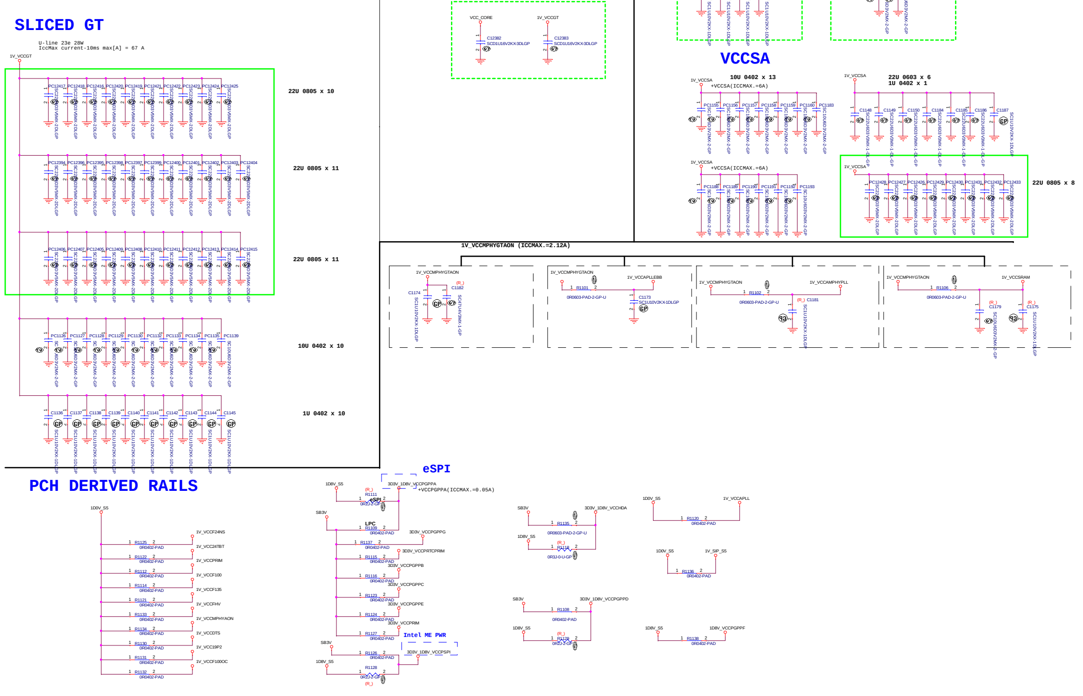
<Variant Name>

wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	010_CPU(POWER CAP1)
Size: Custom	Document Number: Rosa_SKL-U AIO — Rev: -1
Date: Wednesday, July 01, 2015	Sheet 10 of 105

Main Func = CPU

To support the full power state:

- vccprim_core Power well and VCCSPI power supply wells will be required to be powered by the 1.0 V and 3.3 V (or 1.8 V) power well, respectively.
- Support for power sequencing signals as described in the Skylake Platform Intel® Management Engine (Intel® ME) and Embedded Controller (EC) Interaction - Product Specification.

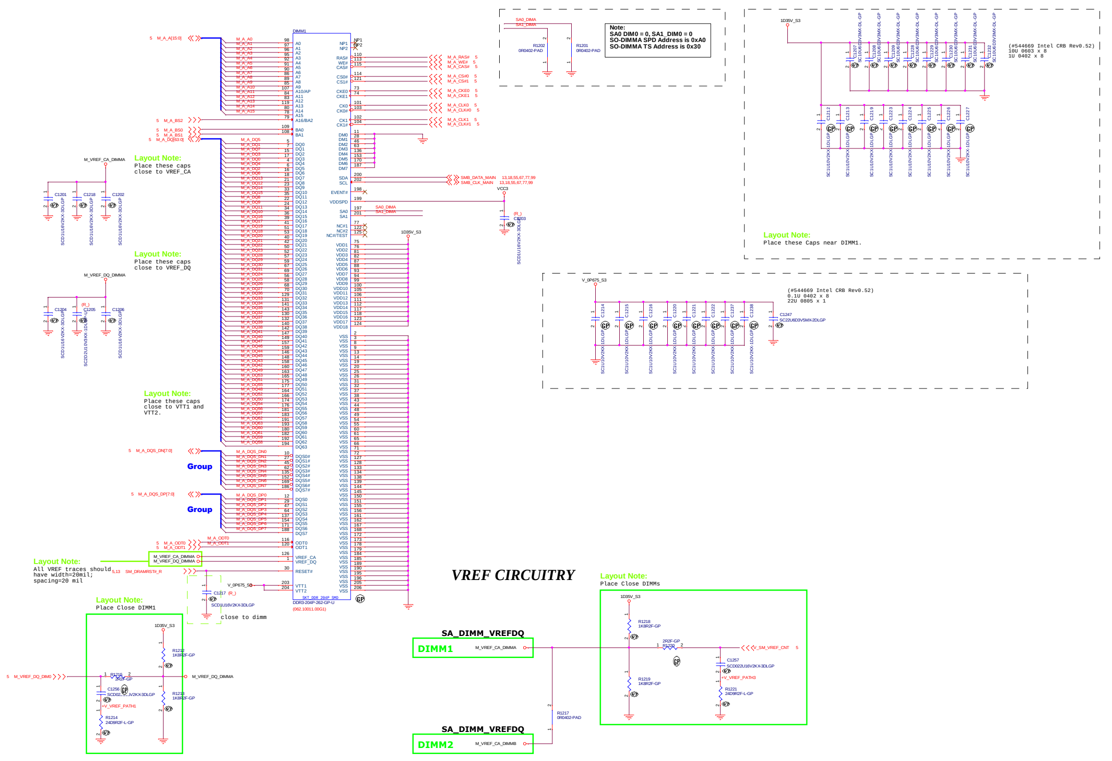


<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	011_CPU(POWER CAP2)	
Size: E	Document Number: Rosa_SKL-U AIO	Rev: -1
Date: Wednesday, July 01, 2015	Sheet 11 of 105	

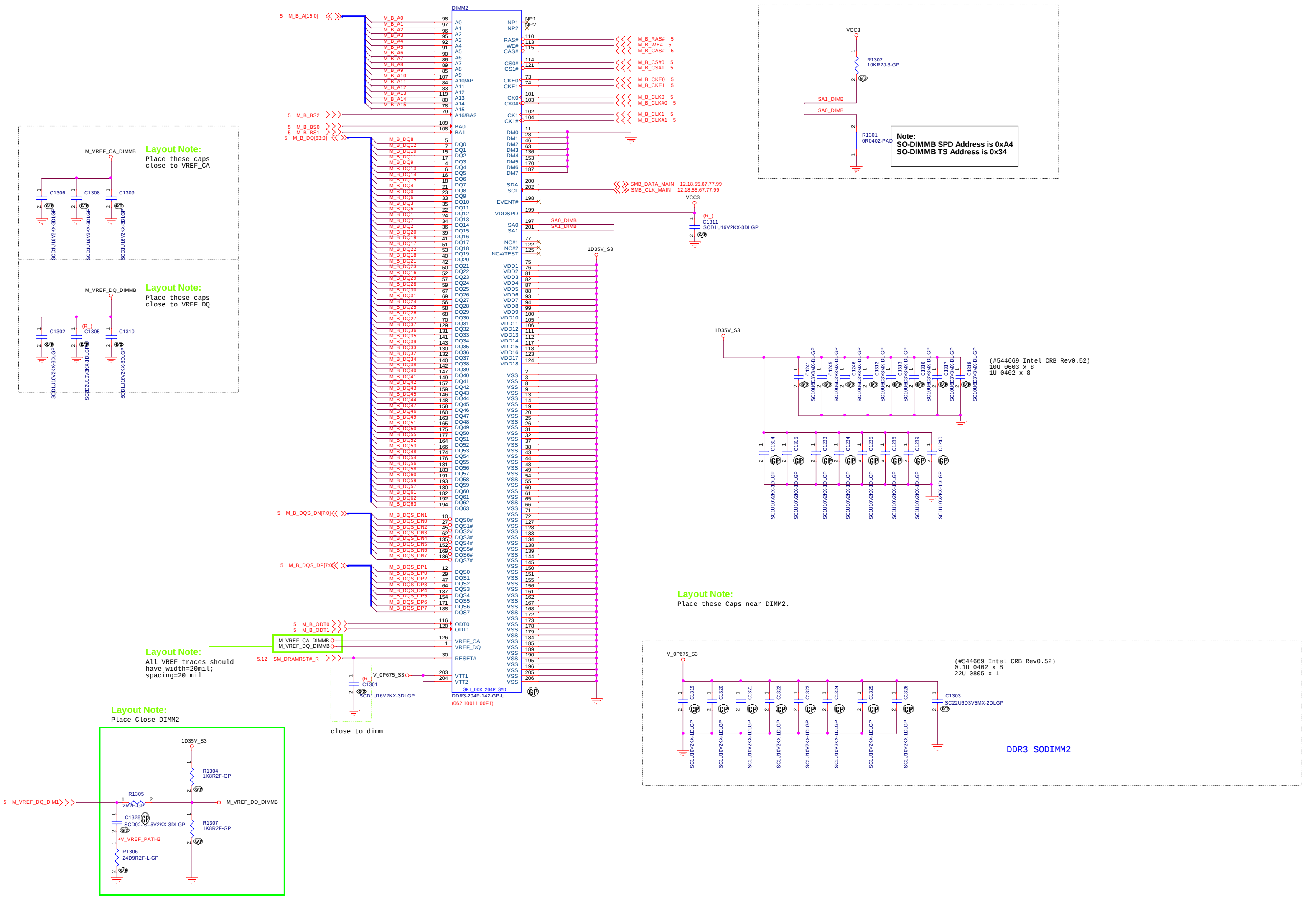
Main Func = DDR SODIMM



<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	012_DDR3_SODIMM1	
Size: E	Document Number: Rosa_SKL-U AIO	Rev: -1
Date: Wednesday, July 01, 2015	Sheet 12 of 105	

Main Func = DDR SODIMM



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 013_DDR3_SODIMM2

Size: D | Document Number: Rosa_SKL-U AIO | Rev: -1

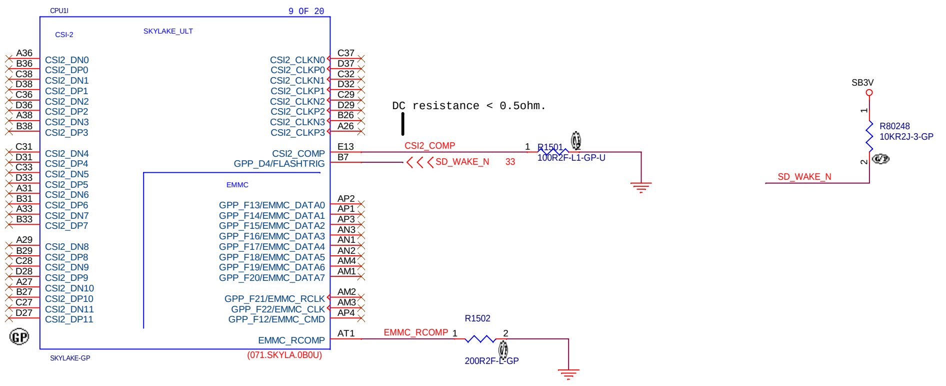
Date: Wednesday, July 01, 2015 | Sheet 13 of 105

Blanking

<Variant Name>

	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei		
Title	014_(Reserved)		
Size A4	Document Number Rosa_SKL-U AIO		Rev -1
Date: Wednesday, July 01, 2015	Sheet 14	of 105	

Main Func = PCH



<Variant Name>

wistron

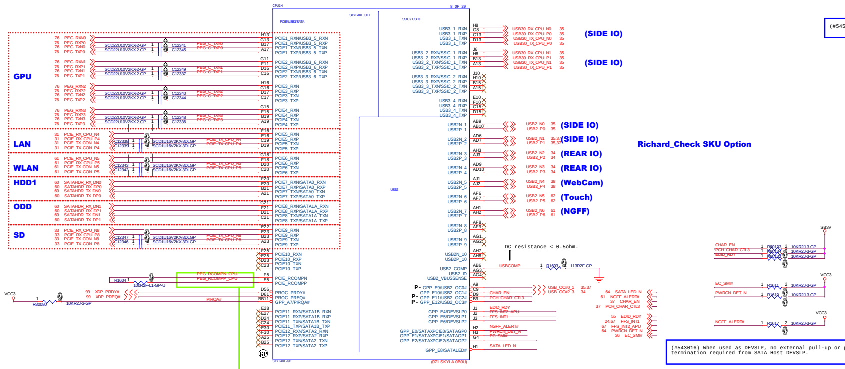
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	015_CPU(CSI2/EMMC)	
Size C	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 15 of 105	

Main Func = PCH

*SATA Port 1 can be configured to PCIe Port 8 or 11
Not all ports are available on all SKUs

Richard_Check PCIE Config



(#545659) The xHCI controller supports USB Debug port on all USB3.0 capable ports.

Richard_Check SKU Option

TBD

(#543016) When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

Layout Note:

1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
Note: Must maintain low DC resistance routing (<0.1 ohm).
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

(#543016)
The SATALED# signal is open-collector and requires a weak external pull-up (8.2 kΩ to 10 kΩ) to Vcc3_3.

(#543016) Unused SATAGP[2:0]/GPP_E[2:0] pins must be terminated to either 3.3 V rail or GND using 8.2 KΩ to 10 KΩ on the motherboard.
Do not use both pull-up and pull-down. Either pull-up or pull-down is acceptable.

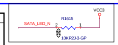


Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe Link Config	1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8	Port9		Port11	Port12
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5							
	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8				
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9	Port10		

USB2 Port6	Touch Panel
USB2 Port7	Card Reader
USB2 Port8	NC
USB2 Port9	NC
USB2 Port10	NC

PCIE Table

Port	Device	Share BUS
1	X	
2	X	
3	X	
4	X	
5	WLAN	PCIE
6	LAN	PCIE
7	HDD	SATA0
8	ODD	SATA1
9	SSD	PCIE
10	SSD	PCIE
11	SSD	PCIE
12	SSD	PCIE/SATA2

USB 2.0 Table

Pair	Device
1	USB2.0 Port1
2	USB2.0 Port2 (Debug Port)
3	USB2.0 Port3 (IO BD)
4	USB2.0 Port4 OC#4_5
5	X
6	WLAN
7	Touch Panel
8	Card Reader
9	X
10	X

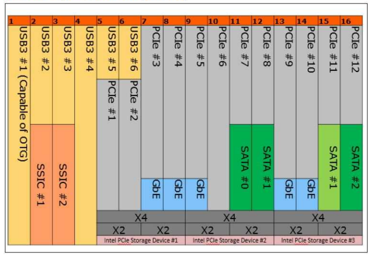
USB 3.0 Table

Pair	Device
1	USB3.0 Port1 OC#0_1
2	USB3.0 Port2 OC#2_3(Debug Port)
3	3D CAMERA
4	X
5	X
6	X

#543016:
220 nF nominal capacitors are recommended for Gen 3.
100 nF nominal capacitors are recommended for Gen 2.

#545659 (SKL_PCH_U_Y_EDS Rev0.7)

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)



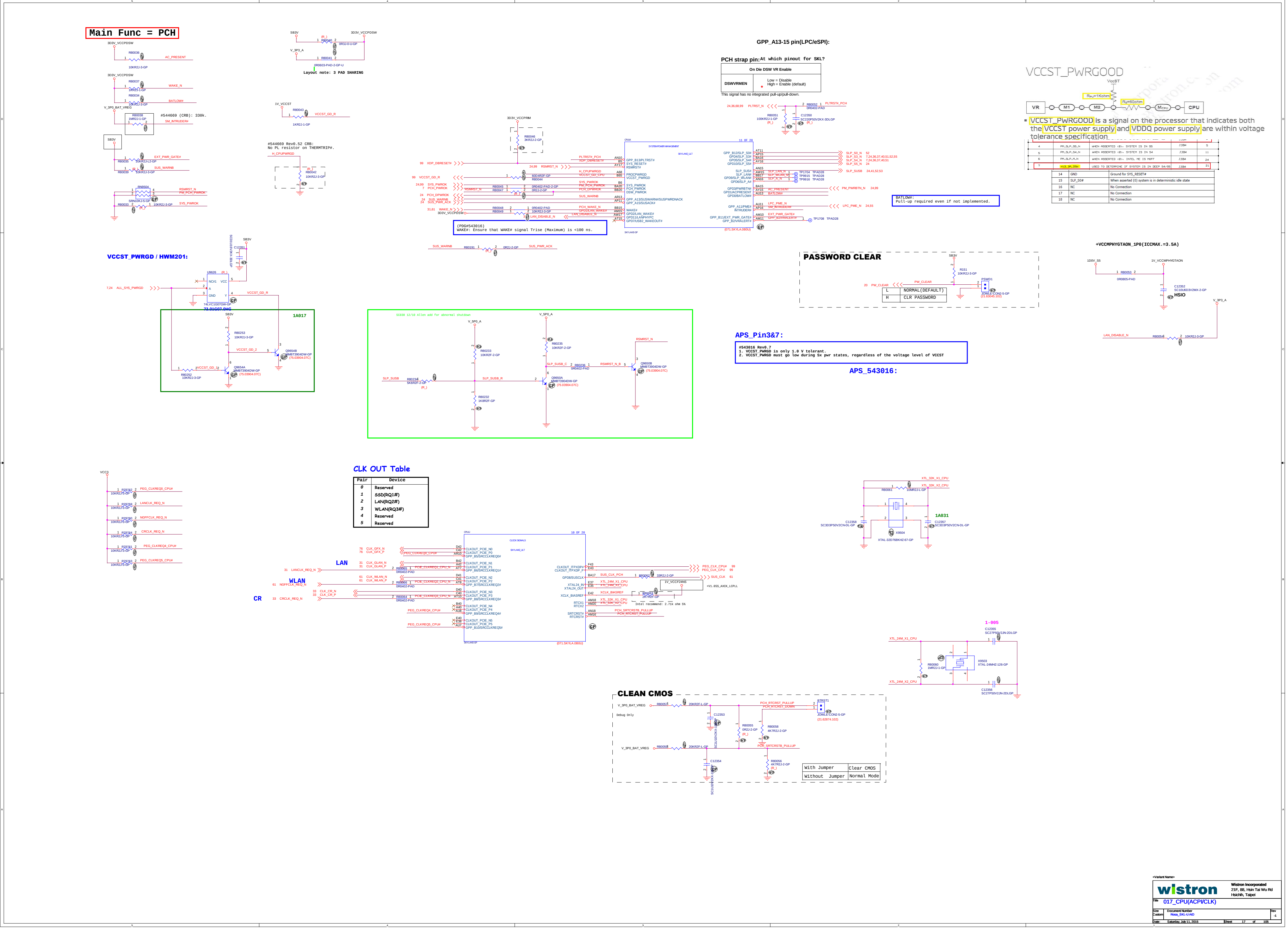
Overcurrent Pin Default Usage_543016

Note: GbE is for Intel LAN chip only.

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	016_CPU_(PCIE/SATA/USB)
Size	E
Document Number	Rosa_SKL-U AIO
Rev	-1
Date:	Wednesday, July 01, 2015
Sheet	16 of 105



Layout note: 3 PAD SHARING

#544669 (CRB): 330k.

#544669 Rev0.52 CRB:
No PL resistor on THERMTRIP#.

(PDG#543016)
WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns.

BATLOW#:
Pull-up required even if not implemented.

PCH strap pin: At which pinout for SKL?

	On Die DSW VR Enable
DSWVRMEN	Low = Disable High = Enable (default)

This signal has no integrated pull-up/pull-down.

- VCCST_PWRGOOD is a signal on the processor that indicates both the VCCST power supply and VDDQ power supply are within voltage tolerance specification

4	PM_SLP_S5_N	WHEN ASSERTED (0), SYSTEM IS IN S5	J3B4	5
5	PM_SLP_S4_N	WHEN ASSERTED (0), SYSTEM IS IN S4	J3B4	11
6	PM_SLP_M_N	WHEN ASSERTED (0), INTEL ME IS MOFF	J3B4	24
7	+V3.3A_DSW	USED TO DETERMINE IF SYSTEM IS IN DEEP S4/S5	J3B4	21

14	GND	Ground for SYS_RESET#
15	SLP_S0#	When asserted (0) system is in deterministic idle state
16	NC	No Connection
17	NC	No Connection
18	NC	No Connection

L	NORMAL(DEFAULT)
H	CLR PASSWORD

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

CLK OUT Table

Pair	Device
0	Reserved
1	SSD(RQ1#)
2	LAN(RQ2#)
3	WLAN(RQ3#)
4	Reserved
5	Reserved

Intel recommend: 2.71k ohm 1%

With Jumper	Clear CMOS
Without Jumper	Normal Mode

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	017_CPU(ACPI/CLK)	
Size: Custom	Document Number: Rosa_SKL-U AIO	Rev: -1
Date: Saturday, July 11, 2015	Sheet 17 of 105	

Main Func = PCH

PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. 1 = eSPI Is selected for EC.

This signal has a weak internal pull-down.

PCH strap pin:

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

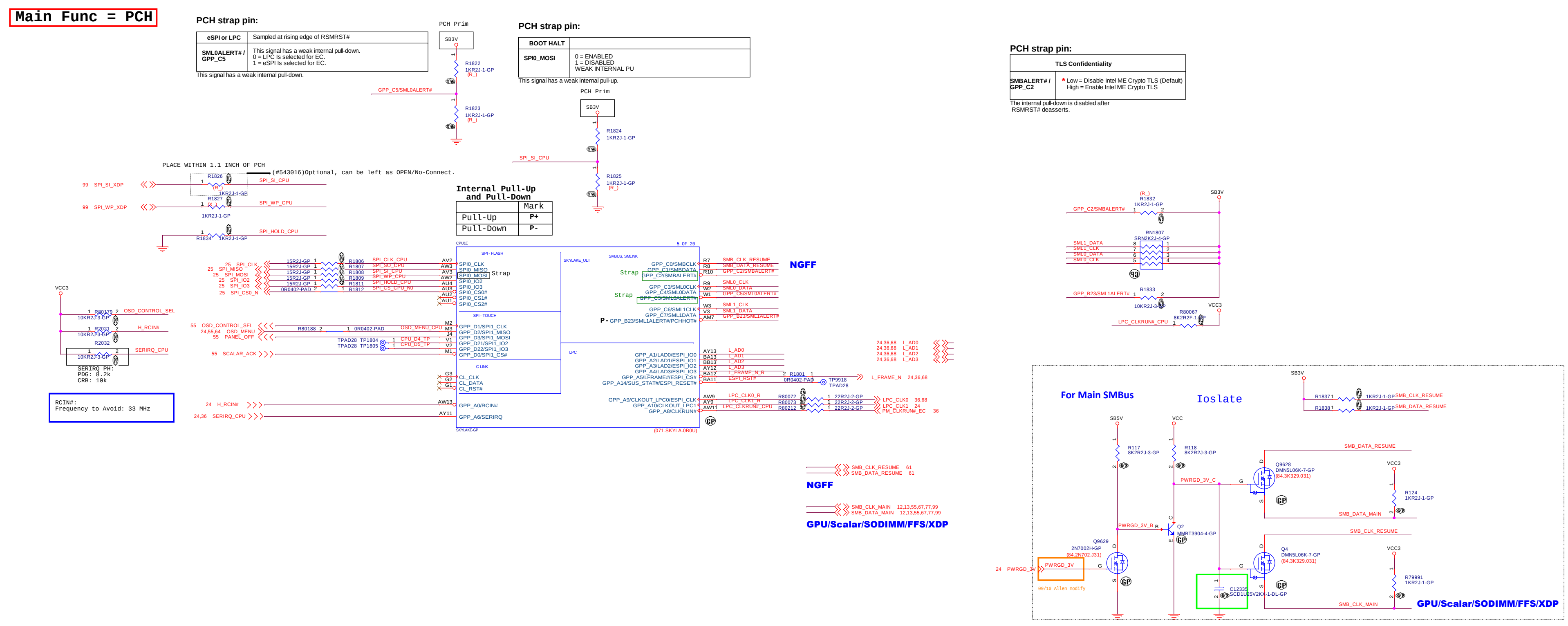
PCH strap pin:

TLS Confidentiality	
SMBALERT# / GPP_C2	* Low = Disable Intel ME Crypto TLS (Default) High = Enable Intel ME Crypto TLS

The internal pull-down is disabled after RSMRST# deasserts.

Internal Pull-Up and Pull-Down

	Mark
Pull-Up	P+
Pull-Down	P-



<Variant Name>

wistron Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei

Title	018_CPU(SPI/SMBUS/LPC)		
Size D	Document Number Rosa_SKL-U AIO		Rev -1
Date: Wednesday, July 01, 2015	Sheet 18 of 105		

Main Func = PCH

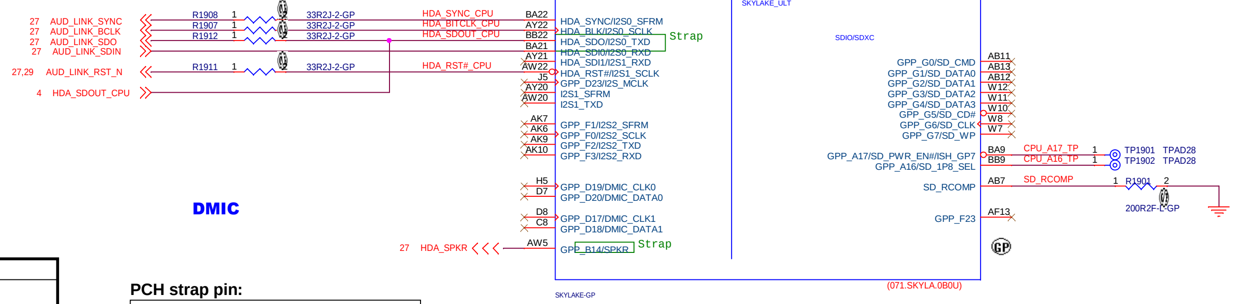
Card Reader by SDIO_545659:

AUDIO

PCH strap pin:

Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs

*



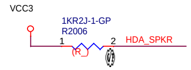
DMIC Table

Pair	Device
0	DMIC Port1
1	DMIC Port2

PCH strap pin:

Top Swap Override	
HDA_SPKR	* Low = Disable (Default) High = Enable

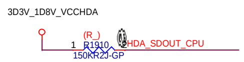
The internal pull-down is disabled after PLTRST# deasserts



PCH strap pin:

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

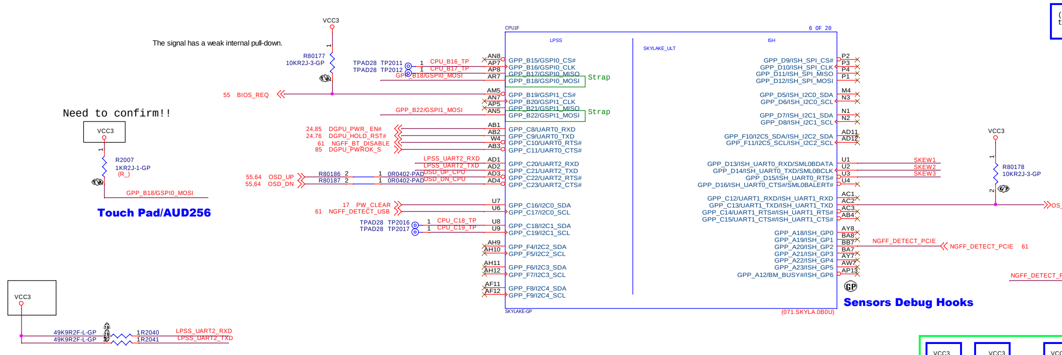
The internal pull-down is disabled after PLTRST# deasserts



<Variant Name>

wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	019_CPU(HDA)	
Size C	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 19 of 105	

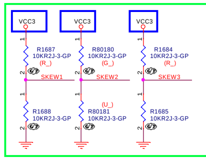
Main Func = PCH



(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

(PDG#543016) If the UART/GPIO functionality is also not used, the signals can be left as no-connect.

Sensor_548926:

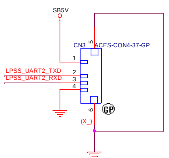


Skew ID Settings

MB Version	Skew1	Skew2	Skew3
GPU	0	1	1
UMA	0	0	1
GPU Touch	0	1	0
UMA Touch	0	0	0

Intel has removed EHCI controller from SKLU and proposed to use USB/UART Muxing for Win7 debug.

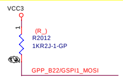
Pin height 2.3mm



PCH strap pin:

Boot BIOS Strap Bit BBS	
Boot BIOS Destination	* Low = SPI (Default) High = LPC

The internal pull-down is disabled after PLTRST# deasserts



Need double confirm, GPIO table set to GPI if that's needed PH or PL

<Variant Name>

wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	020_CPU(GPIO/UART/SPI/I2C)
Size: D	Document Number: Rosa_SKL-U AIO — Rev: -1
Date: Wednesday, July 01, 2015	Sheet 20 of 105

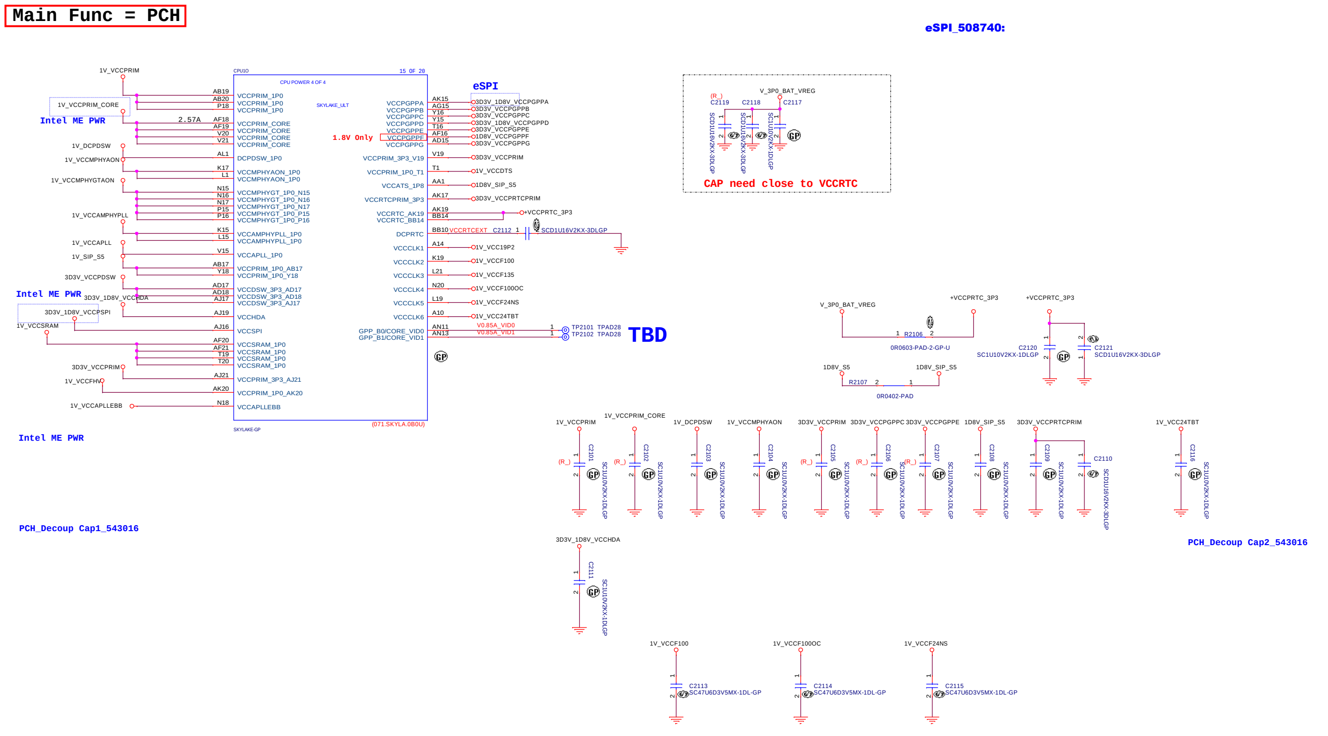


Table 55-8. Decoupling and Power Connection Requirements for SKL U PCH (Sheet 2 of 2)

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R)unway / (E)dge	Place capacitor(s) near ball(s)
V1.0A / V2.4A	VccPRIM	AK20	-	-	-	-	-
V3.3A	VccPRIM	V19, AJ21	1 uF	0402	1	E (<3 mm)	V19 (Note 1)
	VccPGPPB	AG15	1 uF	0402	1	E (<3 mm)	AG15 (Note 1)
	VccPGPPC	Y16	1 uF	0402	1	E (<10 mm)	Y16 (Note 1)
	VccPGPPE	T16	1 uF	0402	1	E (<10 mm)	T16 (Note 1)
V3.3A/ V1.5A/ V1.8A	VccHDA	AJ19	1 uF	0402	1	E (<10 mm)	AJ19 (Note 1)
V3.3A/ V1.8A	VccSPI	AJ16	-	-	-	-	-
	VccPGPPA	AK15	-	-	-	-	-
	VccPGPPD	Y15	-	-	-	-	-
	VccPGPPG	AD15	-	-	-	-	-
	VccRTCPRIM	AK17	1 uF	0402	1	E (<3 mm)	AK17
			0.1 uF	0402	1		
V3.3DSW (3.3V)	VccDSW	AD17, AD18, AJ17	-	-	-	-	-
V3.3RTC (3.3V)	VccRTC	AK19, BB14	1 uF	0402	1	E (<3 mm)	AK19
			0.1 uF	0402	1		
V1.8A	VccPGPPF	AF16	-	-	-	-	-
	VccATS	AA1	1 uF	0402	1	E (<10 mm)	AA1
PCH Internal VRM	DcpRTC	BB10	0.1 uF	0402	1	E (<3 mm)	BB10
	DcpDSW	AL1	1 uF	0402	1	E (<3 mm)	AL1

Note:
1. Placeholder only. Does not need to be stuffed.
2. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
3. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
4. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to "Loop Inductance Reduction Decoupling".

<Variant Name>

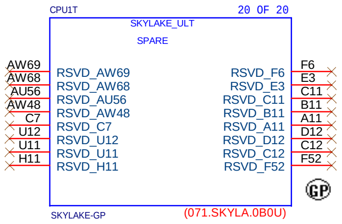
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 021_CPU(POWER)

Size: D | Document Number: Rosa_SKL-U AIO | Rev: -1

Date: Wednesday, July 01, 2015 | Sheet 21 of 105

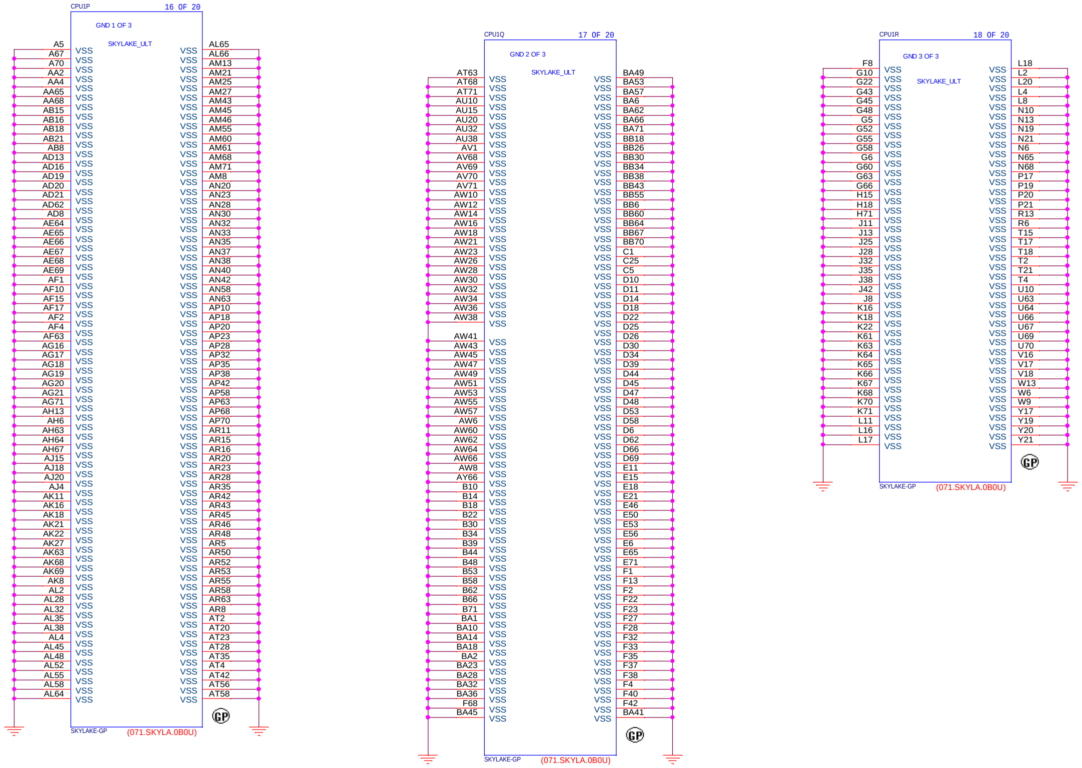
Main Func = PCH



<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	022_CPU(RSVD)		
Size A3	Document Number Rosa_SKL-U AIO		Rev -1
Date:	Wednesday, July 01, 2015	Sheet 22 of 105	

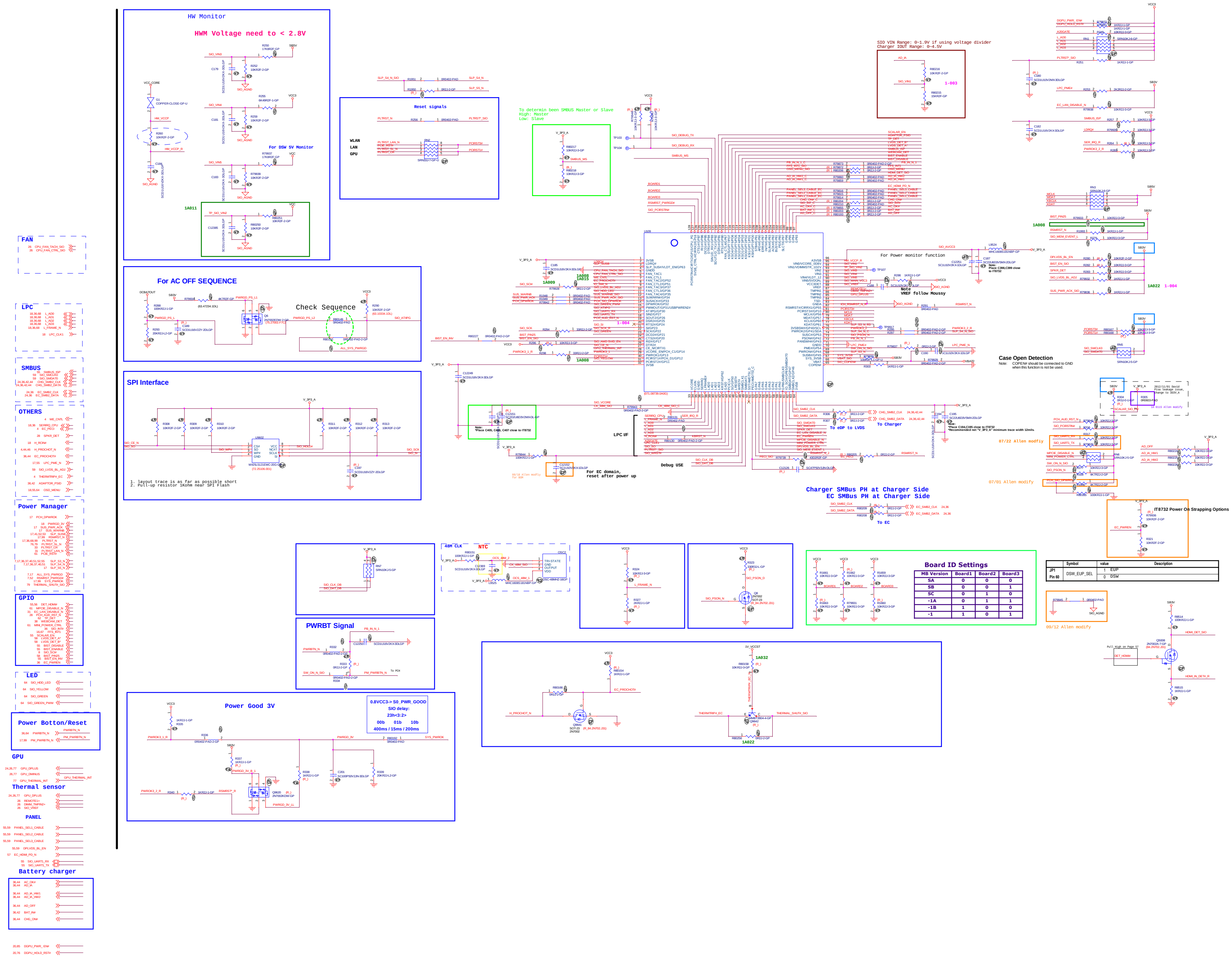
Main Func = PCH



<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	023_CPU(VSS)	
Size A2	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 23 of 105	



Board ID Settings

MB Version	Board1	Board2	Board3
SA	0	0	0
SB	0	0	1
SC	0	1	0
-1A	0	1	1
-1B	1	0	0
-1	1	0	1

Symbol	value	Description
JP1 Pin 60	1 EUP 0 DSW	DSW_EUP_SEL

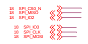
<Variant Name>

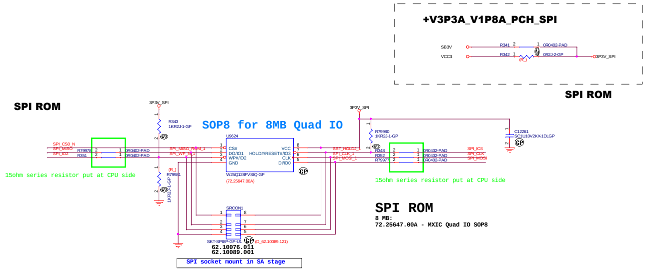
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

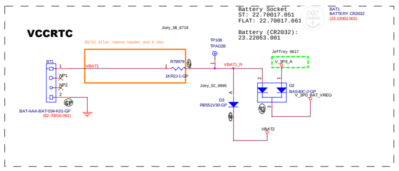
Title: 024_SIO_IT8739(NEW)

Size: E | Document Number: Rosa_SKL-U AIO | Rev: -1

Date: Monday, August 03, 2015 | Sheet 24 of 105

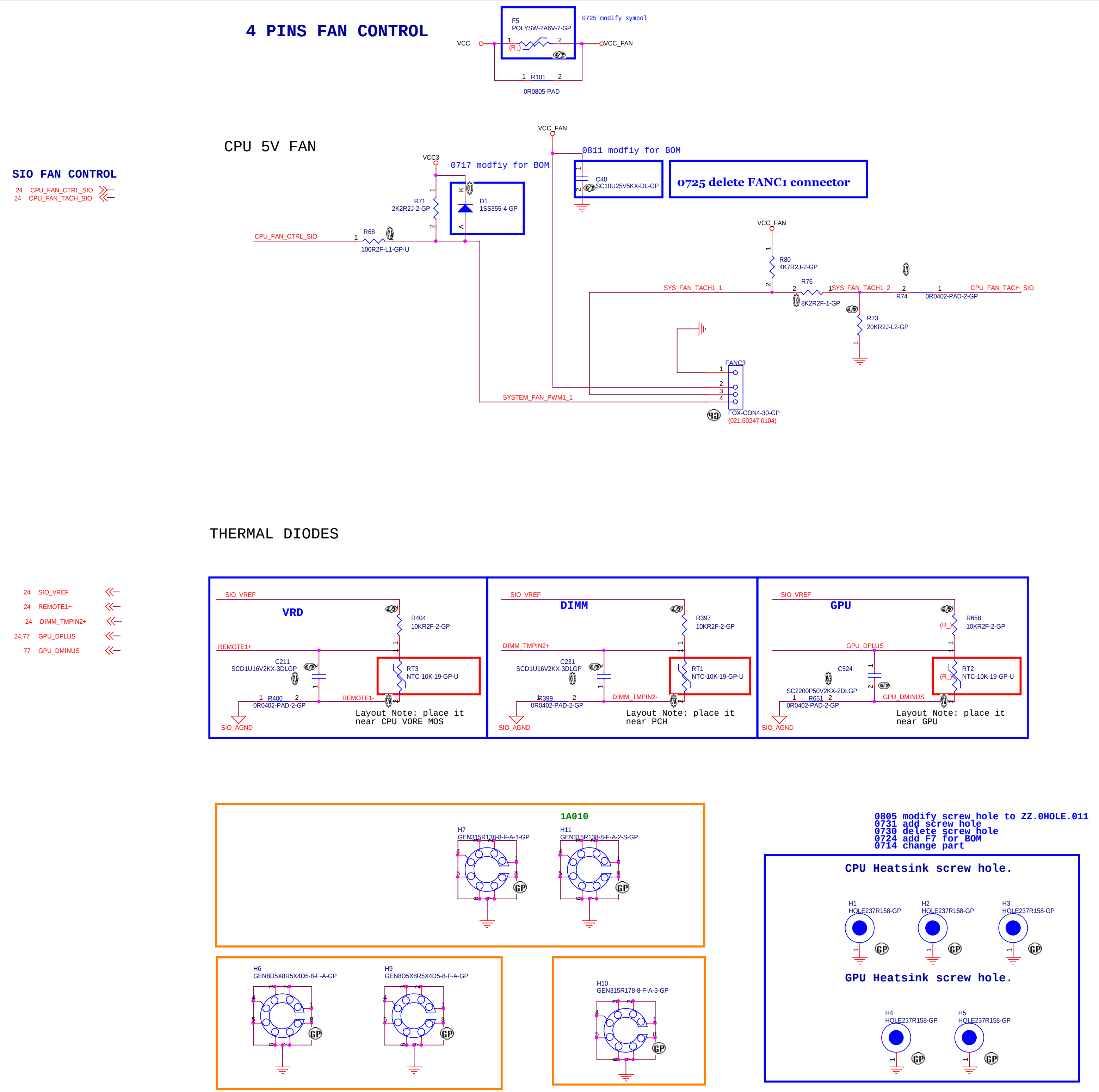






<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	025_Flash ROM/RTC(NEW)	
Size E	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 25 of 105	



<Variant Name>

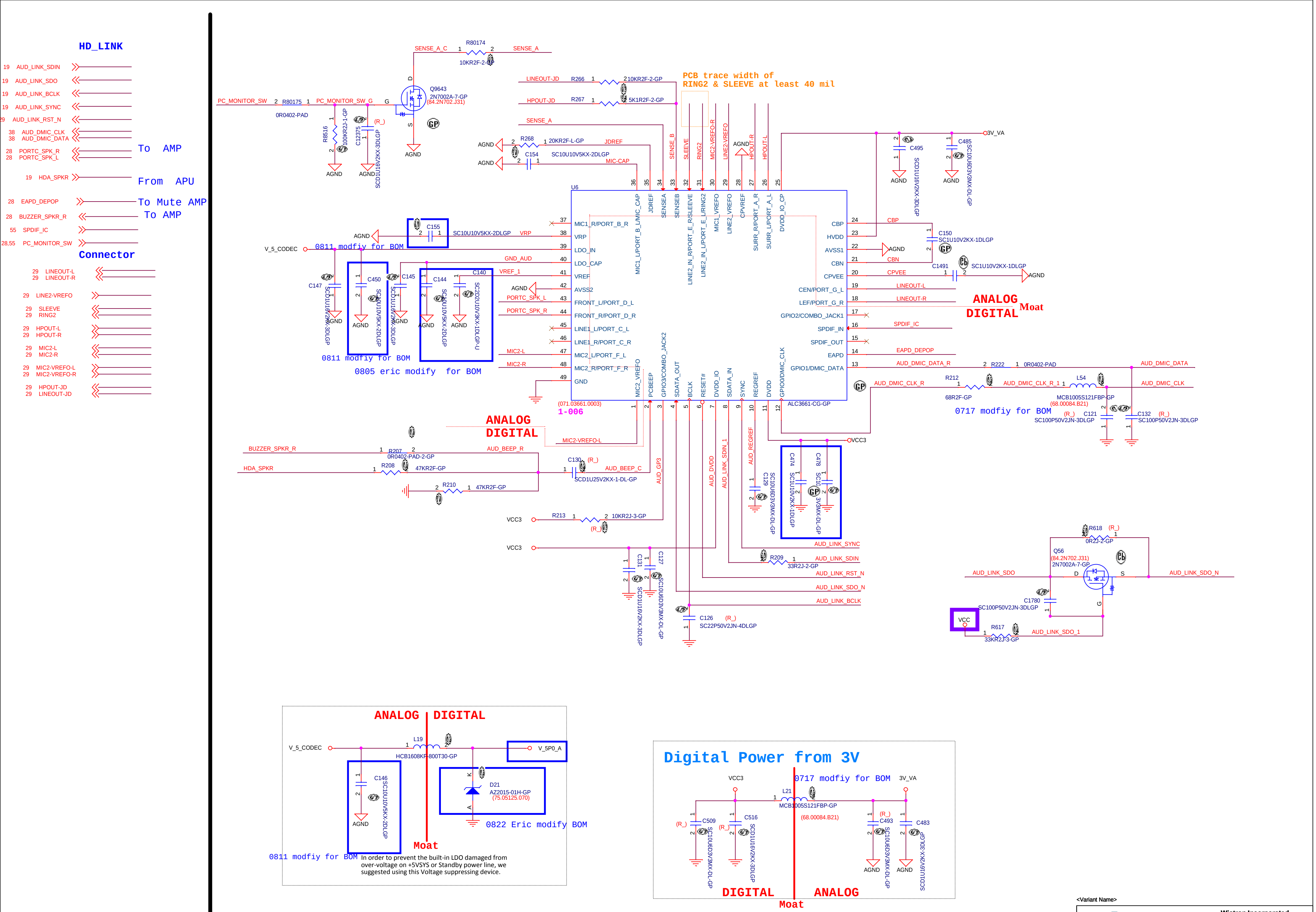
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 026_FAN CIRCUITS/HOLE/THER

Size	Document Number	Rev
C	Rosa_SKL-U AIO	-1

Date: Wednesday, July 01, 2015 Sheet 26 of 105

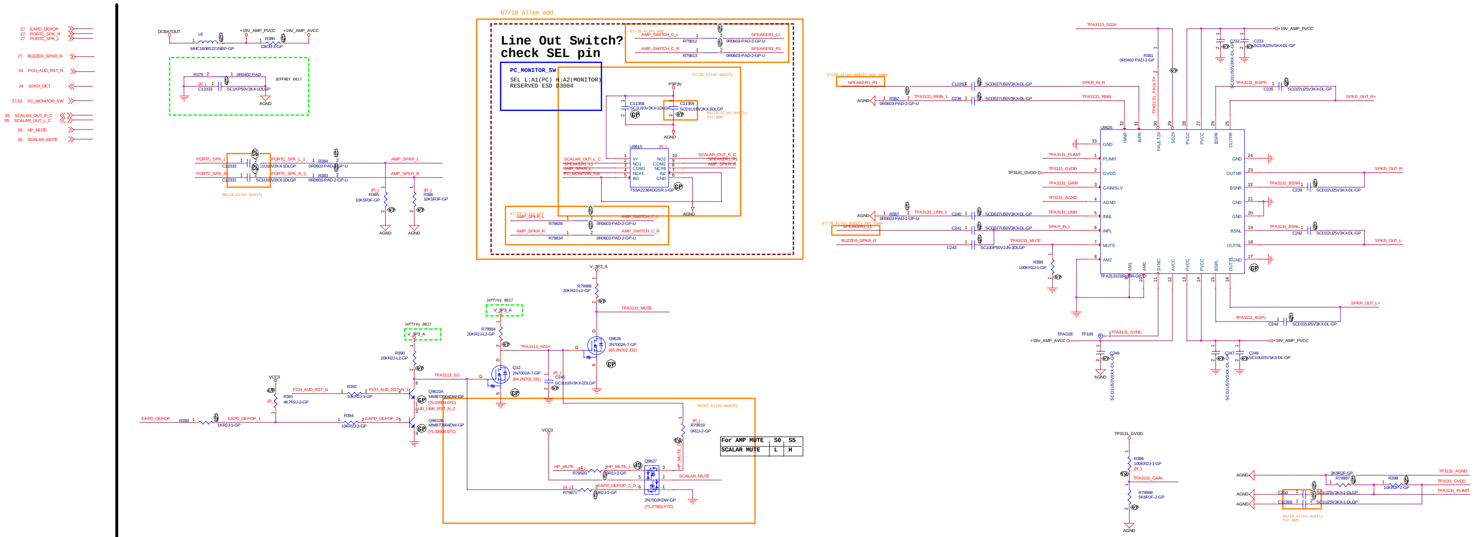


<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	027_AUDIO_ALC3661	
Size C	Document Number Rosa_SKL-U AIO	Rev -1
Date: Monday, August 03, 2015	Sheet 27 of 105	



Internal Speaker x 2

4W, 4ohm

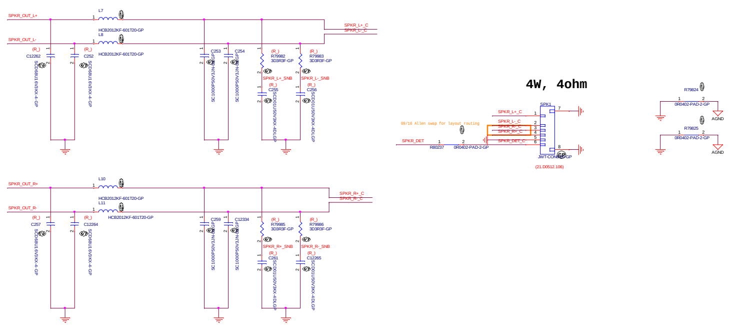


Table 1. GAIN and MASTER/SLAVE

MASTER / SLAVE MODE	GAIN	R1 (to GND)(1)	R2 (to GVDD)(1)	INPUT IMPEDANCE
Master	20 dB	5.6 kΩ	OPEN	60 kΩ
Master	26 dB	20 kΩ	100 kΩ	30 kΩ
Master	32 dB	39 kΩ	100 kΩ	15 kΩ
Master	36 dB	47 kΩ	75 kΩ	9 kΩ
Slave	20 dB	51 kΩ	51 kΩ	60 kΩ
Slave	26 dB	75 kΩ	47 kΩ	30 kΩ
Slave	32 dB	100 kΩ	39 kΩ	15 kΩ
Slave	36 dB	100 kΩ	16 kΩ	9 kΩ

(1) Resistor tolerance should be 5% or better.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \text{ for unclipped power} \quad (2)$$

Where:

R_S is the total series resistance including $R_{DS(on)}$, and output filter resistance.
R_L is the load resistance.
V_P is the peak amplitude
$V_P = 4 \times$ PLIMIT voltage if PLIMIT $< 4 \times V_P$
P_{OUT} (10%THD) = $1.25 \times P_{OUT}$ (unclipped)

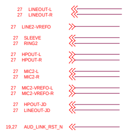
Table 3. POWER LIMIT Example

PV_{CC} (V)	PLIMIT VOLTAGE (V)(1)	R to GND	R to GVDD	OUTPUT VOLTAGE (V_{rms})
24 V	GVDD	Short	Open	17.90
24 V	3.3	45 kΩ	51 kΩ	12.67
24 V	2.25	24 kΩ	51 kΩ	9.00
12 V	GVDD	Short	Open	10.33
12 V	2.25	24 kΩ	51 kΩ	9.00
12 V	1.5	18 kΩ	68 kΩ	6.30

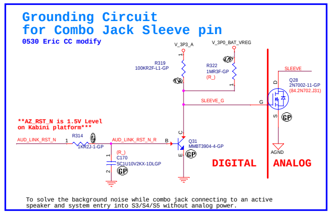
(1) PLIMIT measurements taken with EVM gain set to 26dB and input voltage set to $1V_{rms}$.

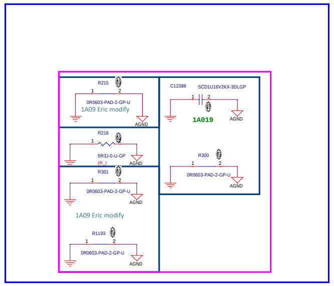
Table 2. Recommended Input AC-Coupling Capacitors

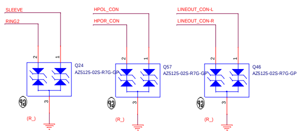
GAIN	INPUT IMPEDANCE	INPUT CAPACITANCE	HIGH-PASS FILTER
20 dB	60 kΩ	1.5 µF	1.8 Hz
26 dB	30 kΩ	3.3 µF	1.6 Hz
32 dB	15 kΩ	5.6 µF	2.3 Hz
36 dB	9 kΩ	10 µF	1.8 Hz

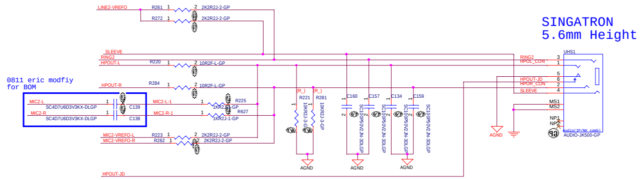


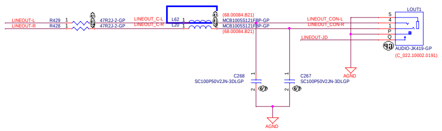
0731 Eric modfiy location for layout











Pin Define:
Pin1:HP_L
Pin2:HP_R
Pin3:Ring2
Pin4:Sleeve
Pin5:AGND
Pin6:JD
Pin7:GND
Pin8:GND

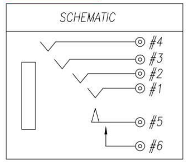
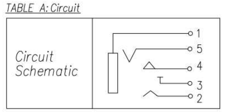
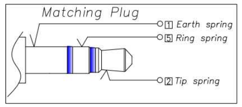


TABLE A:Circuit





4-pin 3.5mm Headset Connector Pinout

Nokia, Lenovo mobile

Pin Number	Pin Name	Description
1	Tip	Left Audio Out
2	Ring-1	Right Audio Out
3	Ring-2	**Microphone**
4	Sleeve	**Ground / Common**

iPhone, Samsung, Blackberry, HTC

Pin Number	Pin Name	Description
1	Tip	Left Audio Out
2	Ring-1	Right Audio Out
3	Ring-2	**Ground / Common**
4	Sleeve	**Microphone**

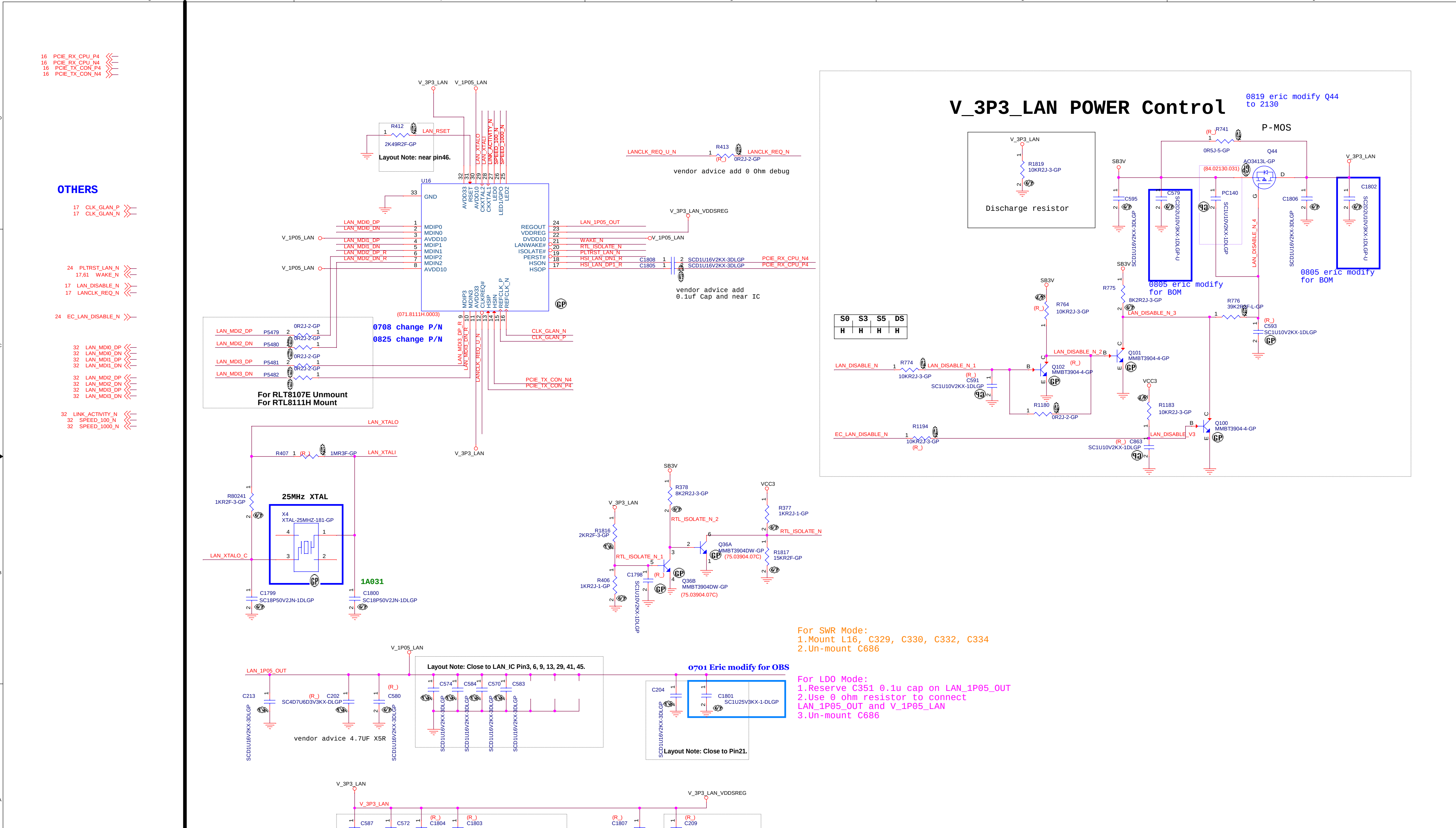
<Variant Name>

wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	029_MIC/SPEAKER/AUDIO JACK	
Size: Custom	Document Number: Rosa_SKL-U AIO	Rev: -1
Date: Wednesday, July 01, 2015	Sheet 29 of 105	

Blanking

<Variant Name>

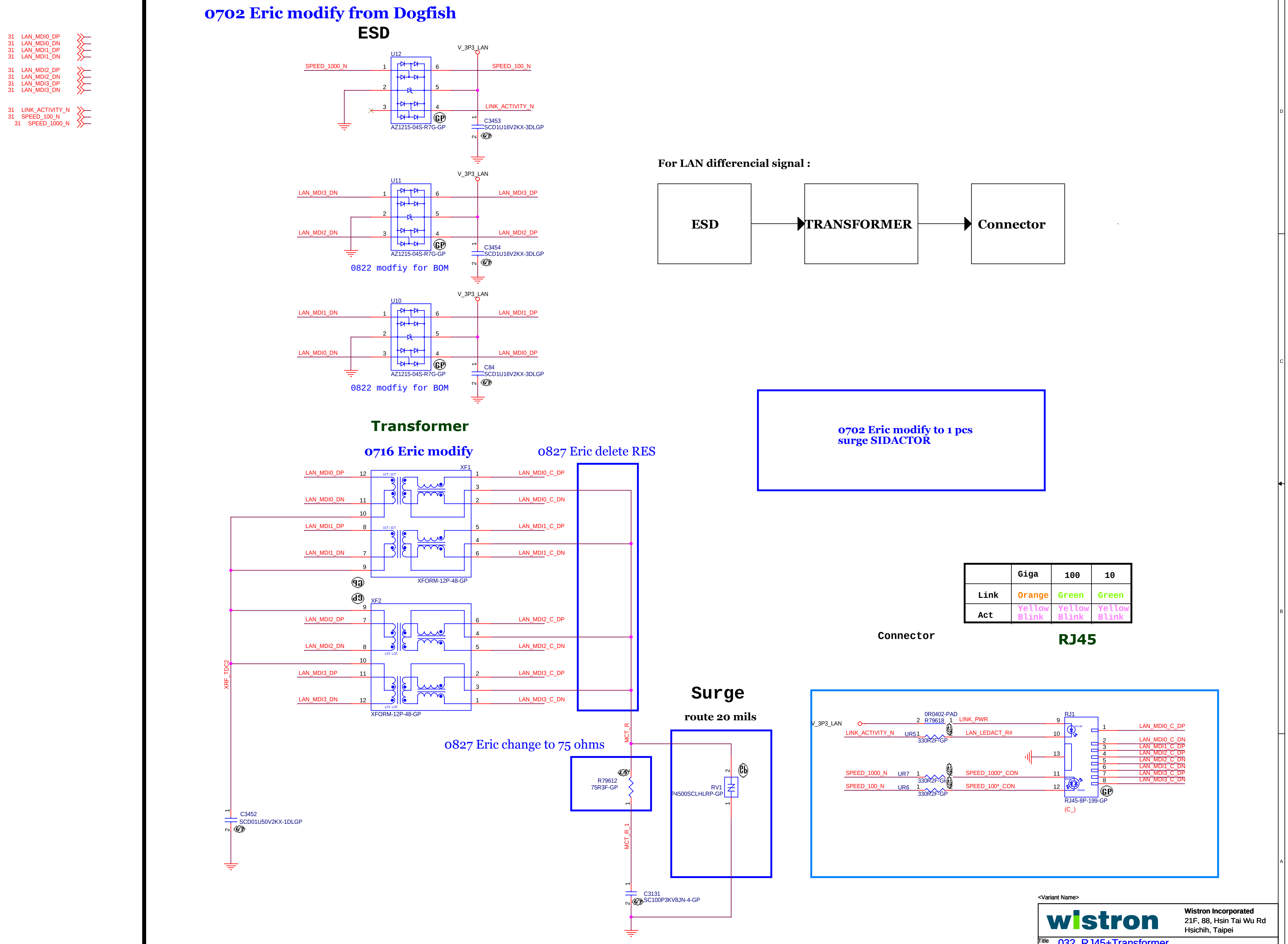
	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	030_(Reserved)	
Size A	Document Number Rosa_SKL-U AIO	Rev -1
Date:	Wednesday, July 01, 2015	Sheet 30 of 105



<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	031_LAN_RTL8111H	
Size: Custom	Document Number: Rosa_SKL-U AIO	Rev: -1
Date: Wednesday, July 01, 2015	Sheet 31 of 105	



	Giga	100	10
Link	Orange	Green	Green
Act	Yellow Blink	Yellow Blink	Yellow Blink

<Variant Name>

wistron

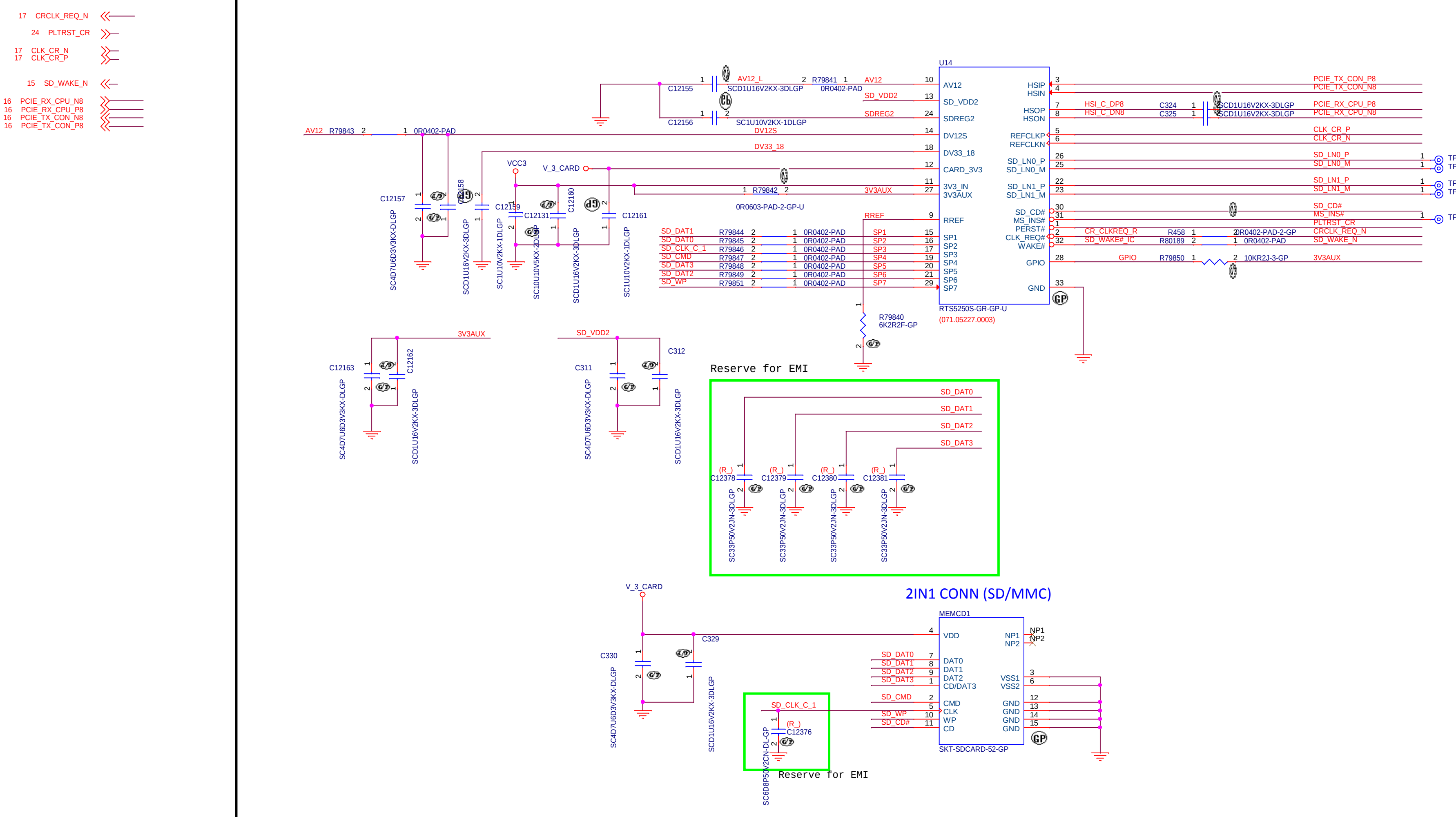
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 032_RJ45+Transformer

Size: C | Document Number: Rosa_SKL-U AIO | Rev: -1

Date: Wednesday, July 01, 2015 | Sheet 32 of 105

Card Reader



<Variant Name>

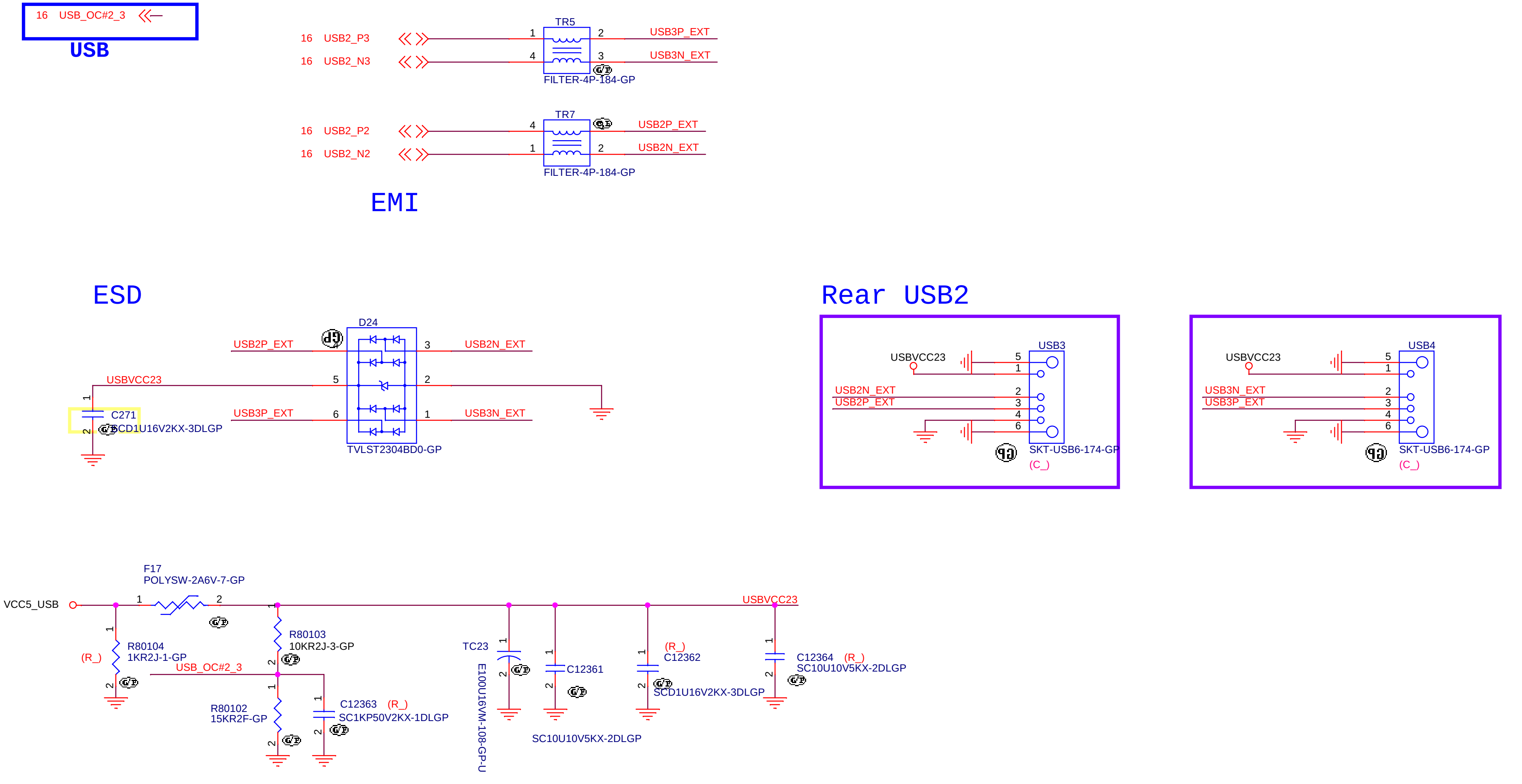
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 033_CardReader CONN

Size: C | Document Number: Rosa_SKL-U AIO | Rev: -1

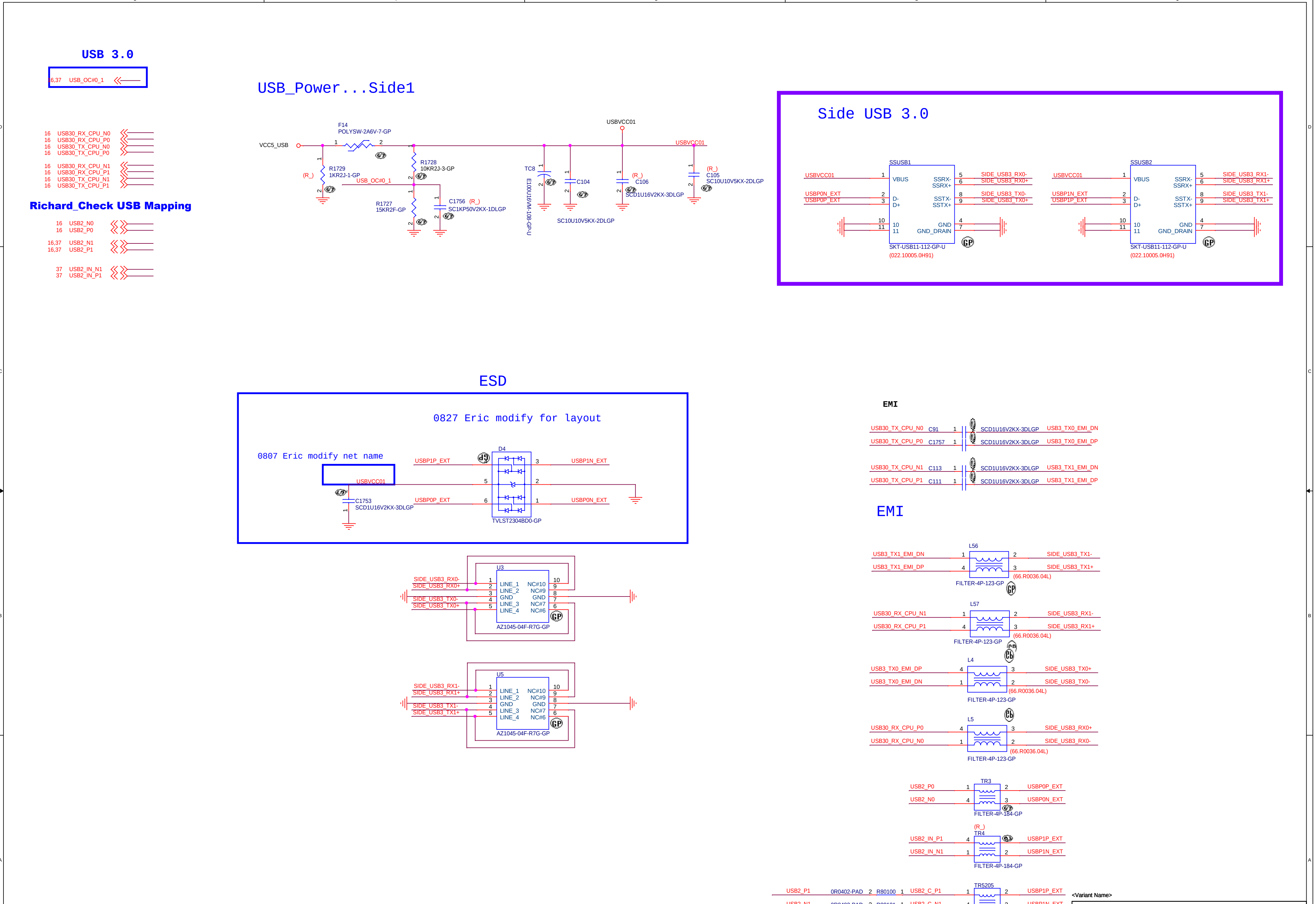
Date: Wednesday, July 01, 2015 | Sheet 33 of 105



<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	034_USB2.0 CONN	
Size B	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 34 of 105	



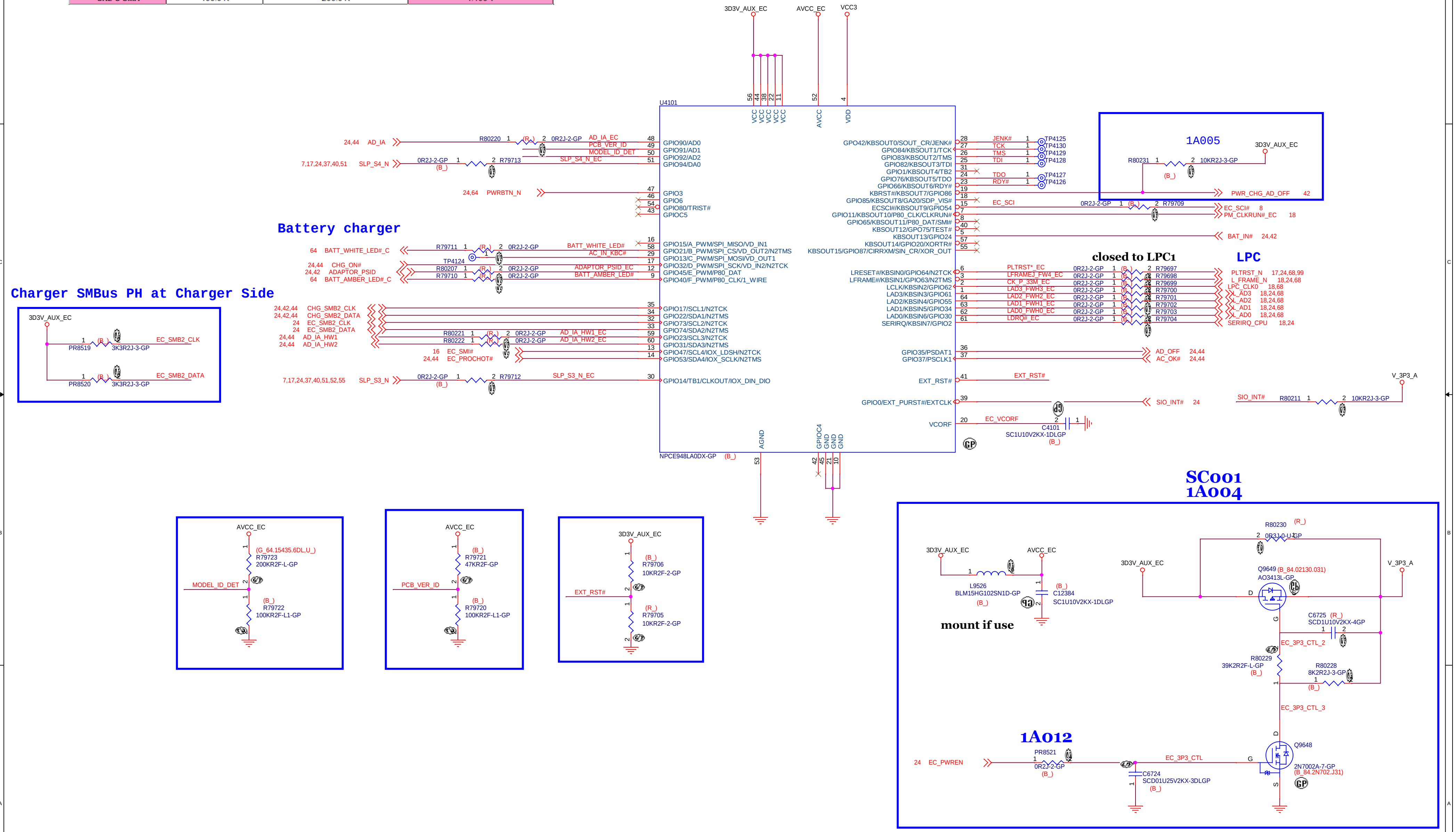
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	035_USB3.0 CONN	
Size C	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 35 of 105	

PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage
SA	100.0 K	10.0 K	3.000 V
SB	100.0 K	20.0 K	2.750 V
SC	100.0 K	33.0 K	2.481 V
-1	100.0 K	47.0 K	2.245 V

MOEDL_ID_DET	Pull-Low Register	Pull-High Register	Typical Voltage
Carrizo GPU	100.0 K	10.0 K	3.000 V
Carrizo UMA	100.0 K	13.7 K	2.902 V
Braswell GPU	100.0 K	57.6 K	2.094 V
Braswell UMA	100.0 K	64.9 K	2.001 V
SKL-U GPU	100.0 K	154.0 K	1.299 V
SKL-U UMA	100.0 K	200.0 K	1.100 V



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 036_EC_NPCE948L(RES)

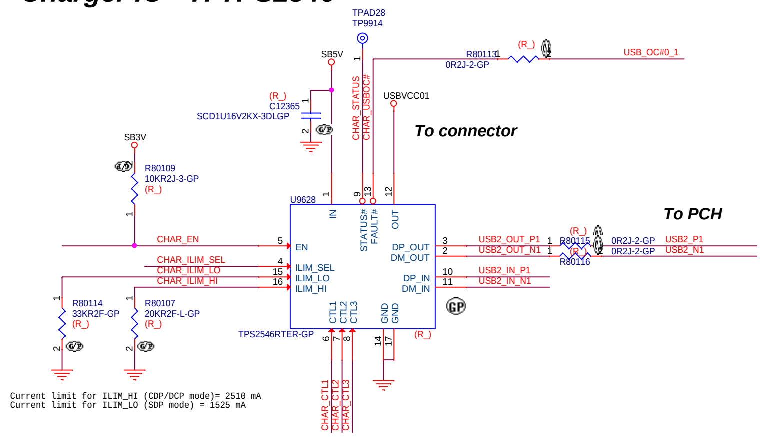
Size: C | Document Number: Rosa_SKL-U AIO | Rev: -1

Date: Wednesday, July 01, 2015 | Sheet 36 of 105

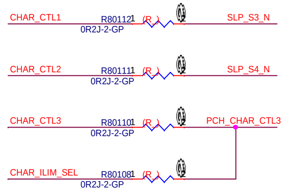
Charger IC - TI TPS2546

Charger IC Control

16,35 USB_OC#0_1
16,35 USB2_N1
16,35 USB2_P1
35 USB2_IN_P1
35 USB2_IN_N1
7,17,24,36,40,51,52,55 SLP_S3_N
7,17,24,36,40,51 SLP_S4_N
16 CHAR_EN
16 PCH_CHAR_CTL3



Current limit for ILIM_HI (CDP/DCP mode)= 2510 mA
Current limit for ILIM_LO (SDP mode) = 1525 mA



To PCH GPIO41

CTL1 SLP_S3#	CTL2 SLP_S4#	CTL3 GPIO41	ILIM_SEL GPIO41	Mode	State
0	0	0	0	Turn off power switch & discharge VBUS	S4/S5
0	0	1	1	DCP	S4/S5
0	1	0	0	SDP	S3
0	1	1	1	DCP with HID auto detect USB data pass through	S3
1	1	0	0	SDP	S0
1	1	1	1	CDP	S0

<Variant Name>

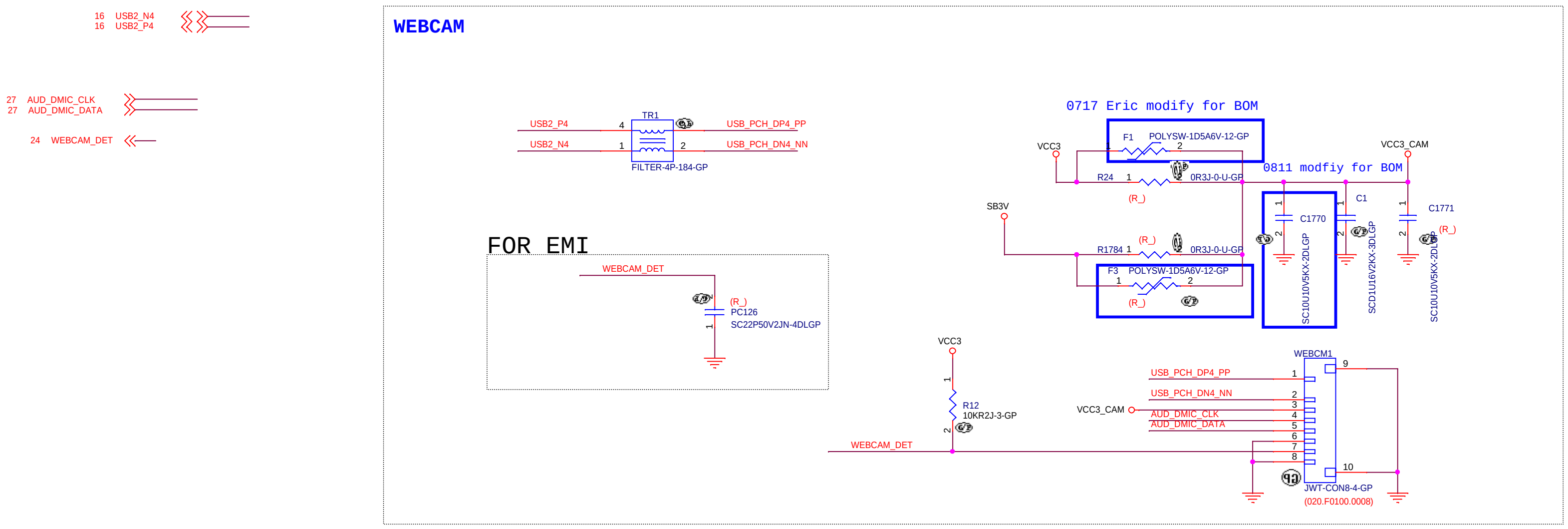
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 037_USB Charger (RES)

Size: C | Document Number: Rosa_SKL-U AIO | Rev: -1

Date: Wednesday, July 01, 2015 | Sheet 37 of 105

WEBCAM



<Variant Name>

wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei		
Title	038_WEBCAM		
Size C	Document Number Rosa_SKL-U AIO		Rev -1
Date: Wednesday, July 01, 2015	Sheet 38 of 105		

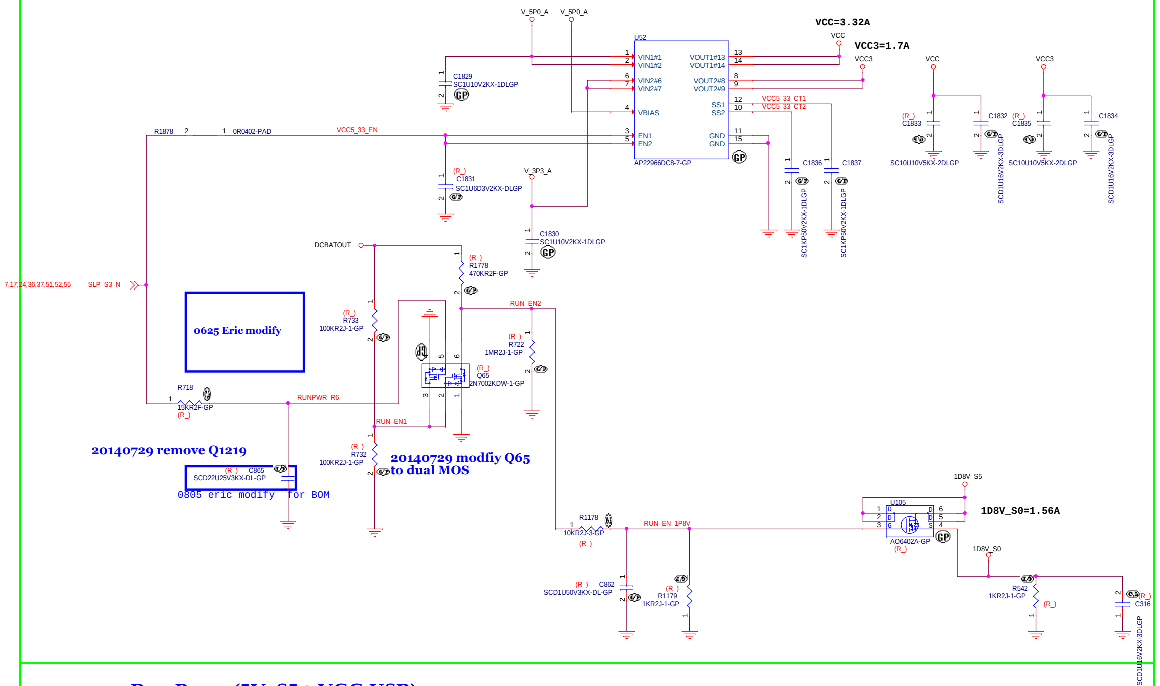
Blanking

<Variant Name>

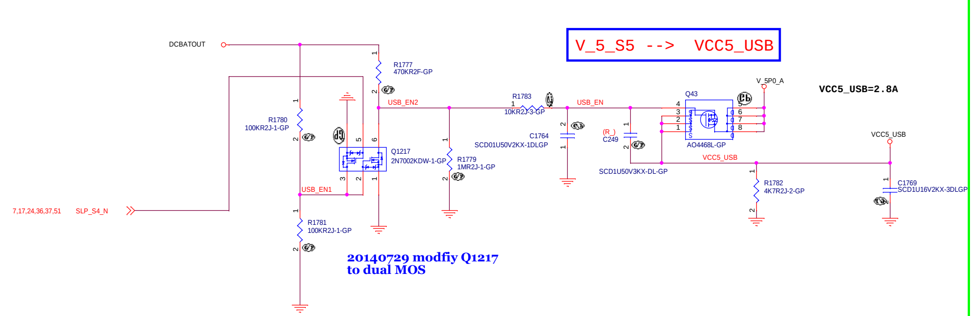
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	039_(Reserved)
Size	A
Document Number	Rosa_SKL-U AIO
Rev	-1
Date:	Wednesday, July 01, 2015
Sheet	39 of 105

Run Power(5V_S0,3.3V_S0,1.8V_S0)



Run Power(5V_S5->VCC USB)

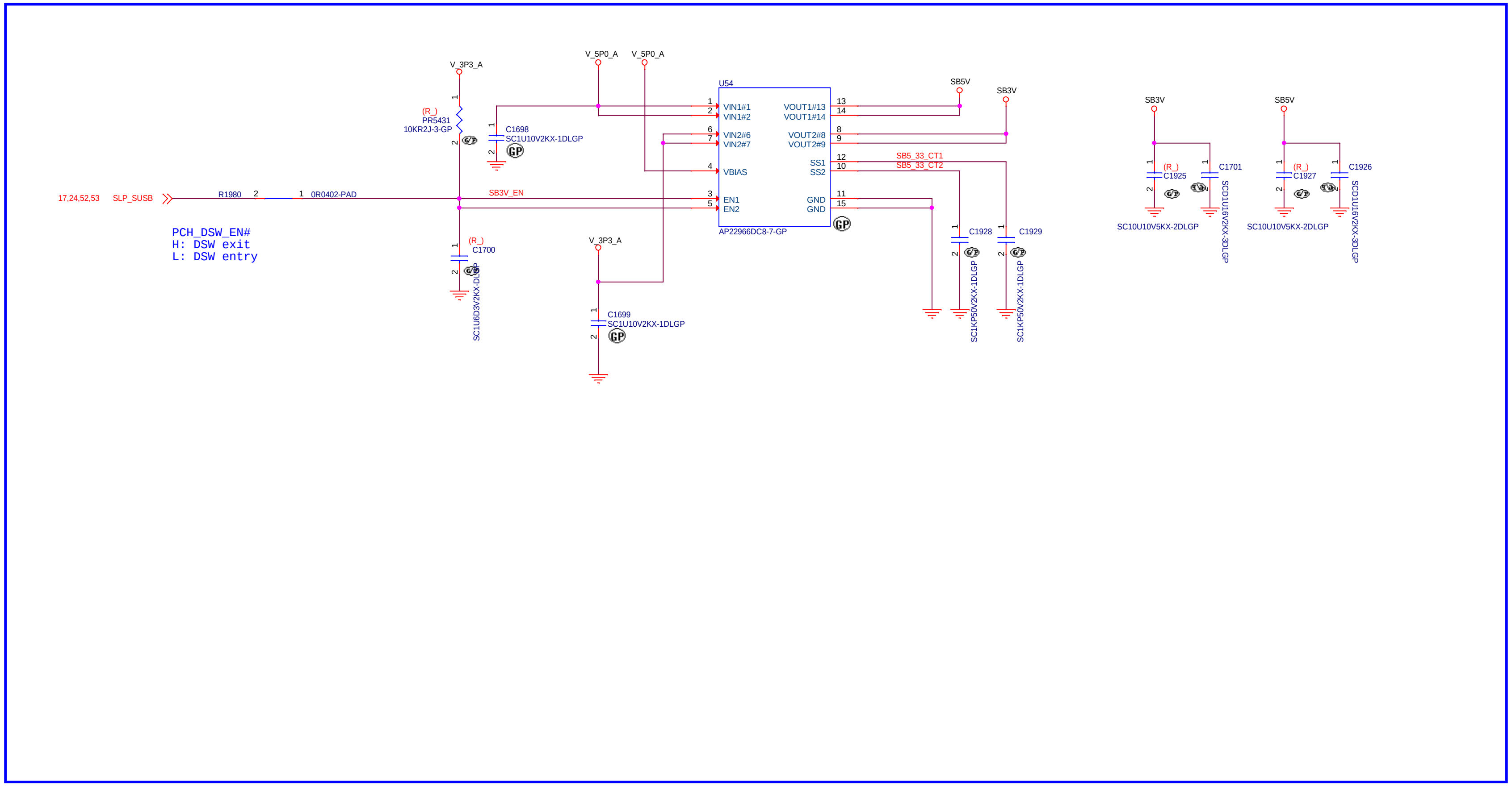


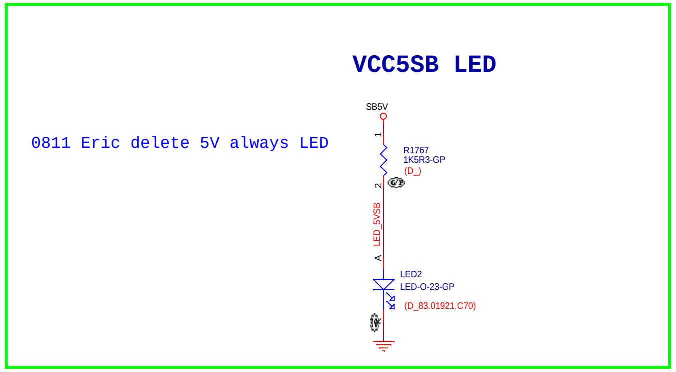
<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	040_Run PWR/USB PWR(NEW)	
Size Custom	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 40 of 105	





<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

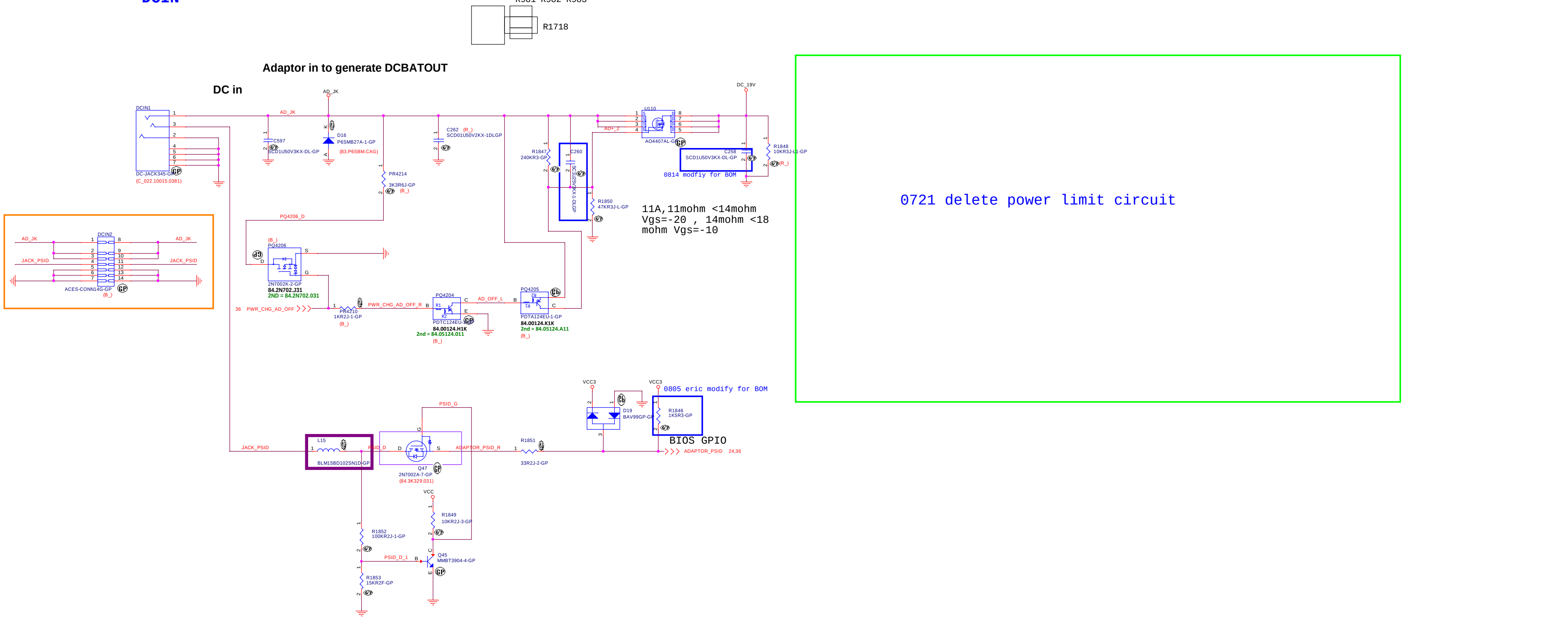
Title: 041_DSW_POWER_CTL

Size	Document Number	Rev
C	Rosa_SKL-U AIO	-1

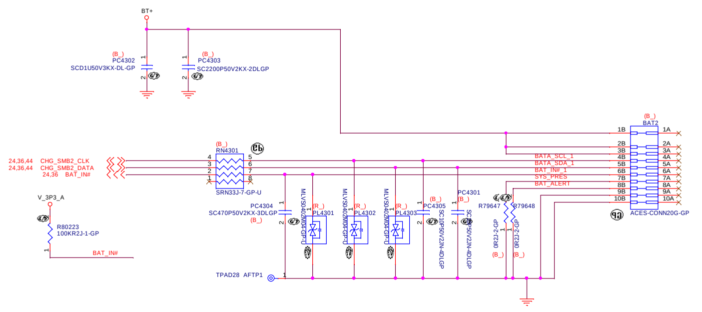
Date: Wednesday, July 01, 2015 Sheet 41 of 105

DCIN

For layout top and bottom the same



BATTERY CONNECTOR



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

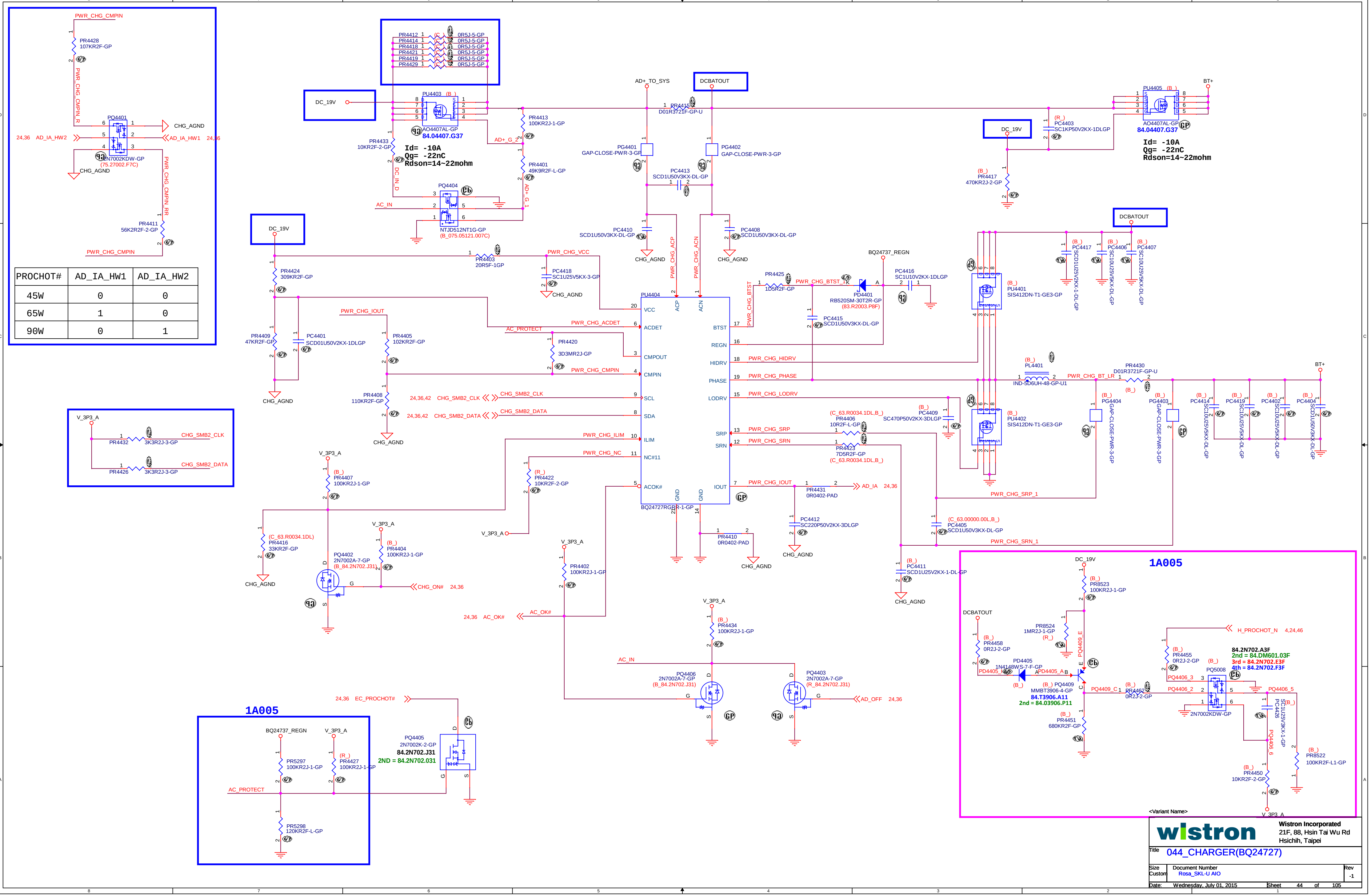
Title	042_DC IN/BATT CONN	
Size D	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 42 of 105	

Blanking

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	043_(Reserved)	
Size Custom	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 43 of 105	



PROCHOT#	AD_IA_HW1	AD_IA_HW2
45W	0	0
65W	1	0
90W	0	1

<Variant Name>

wistron

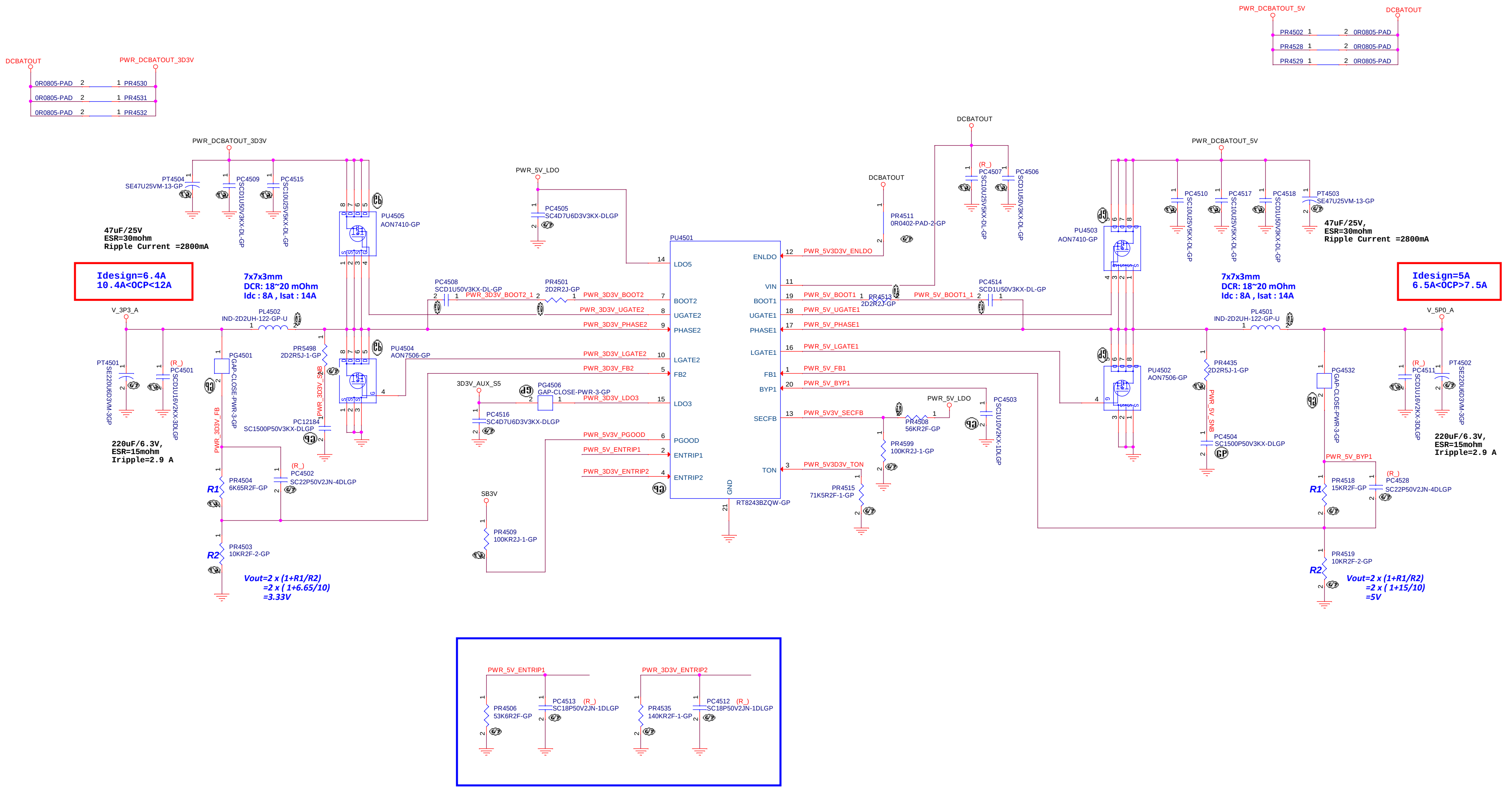
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 044_CHARGER(BQ24727)

Size: Custom | Document Number: Rosa_SKL-U AIO | Rev: -1

Date: Wednesday, July 01, 2015 | Sheet 44 of 105

SSID = PWR.Plane.Regulator_5V/3D3V

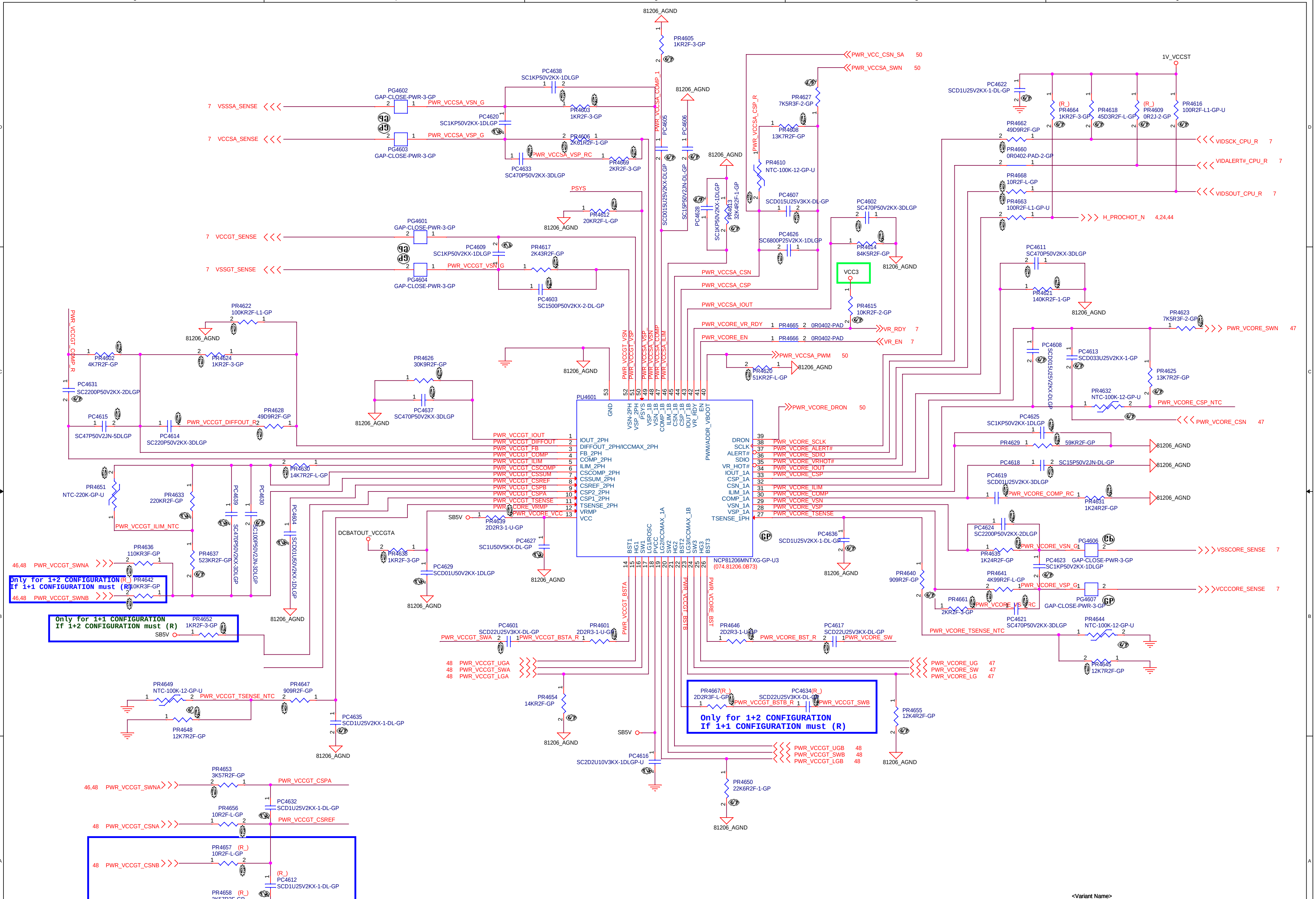


<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	045_RT8243BZQW_5V/3D3V	
Size A2	Document Number: Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 45 of 105	



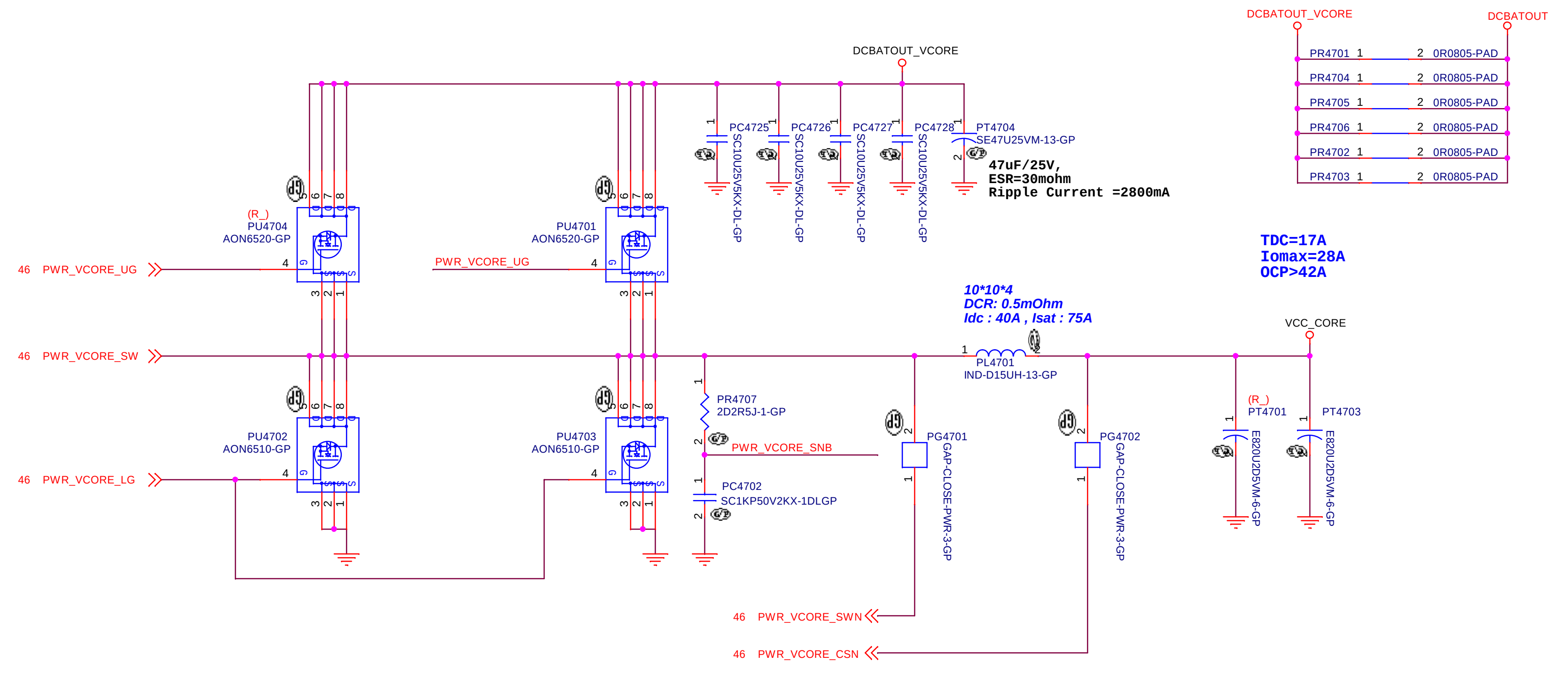
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 046_NCP81206MN_CPU_VCORE(1/3)

Size: C
Document Number: Rosa_SKL-U AIO
Rev: -1

Date: Wednesday, July 01, 2015
Sheet 46 of 105



<Variant Name>

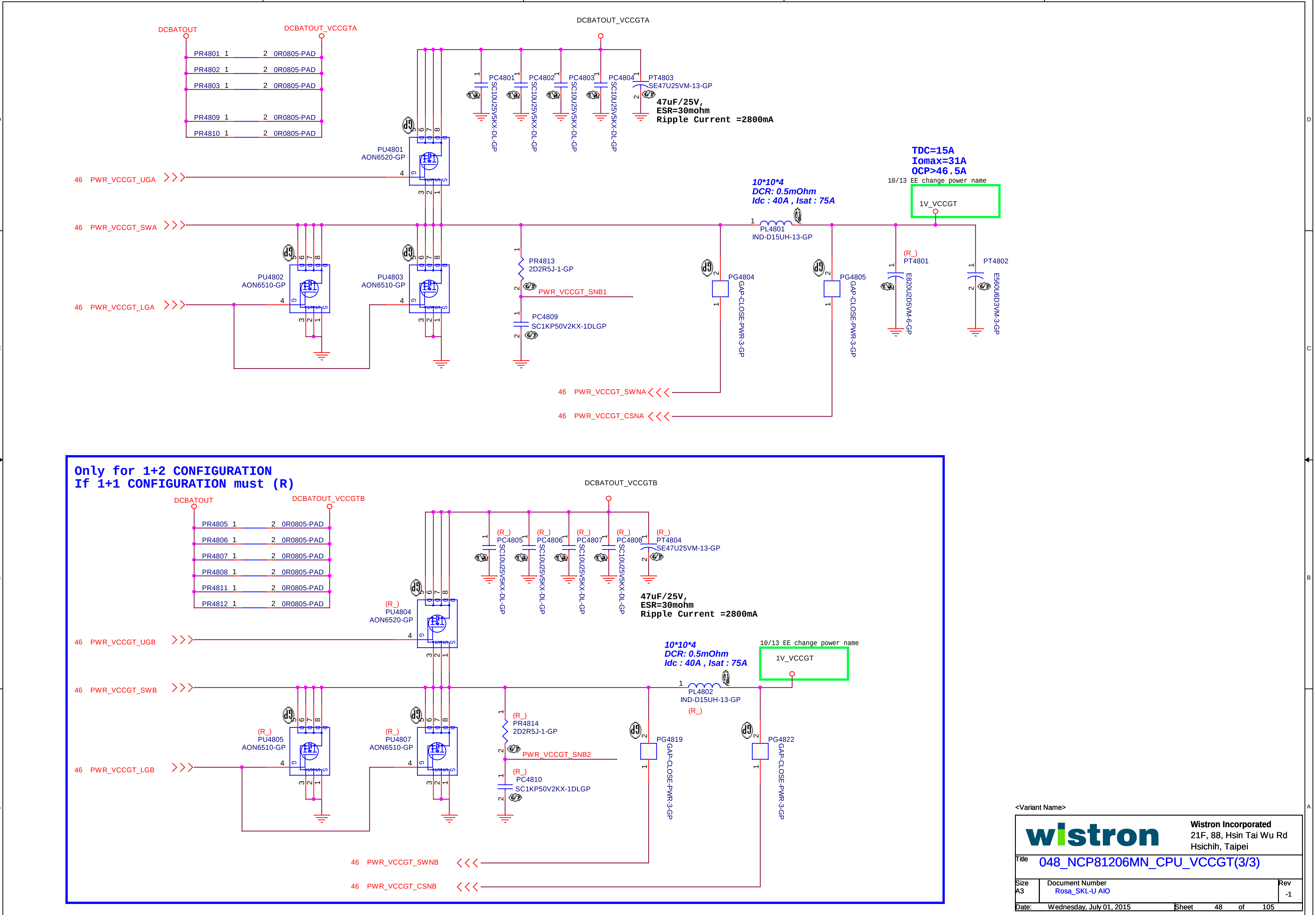
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 047_NCP81206MN_CPU_VCORE(2/3)

Size: A3 | Document Number: Rosa_SKL-U AIO | Rev: -1

Date: Wednesday, July 01, 2015 | Sheet 47 of 105



<Variant Name>

wistron

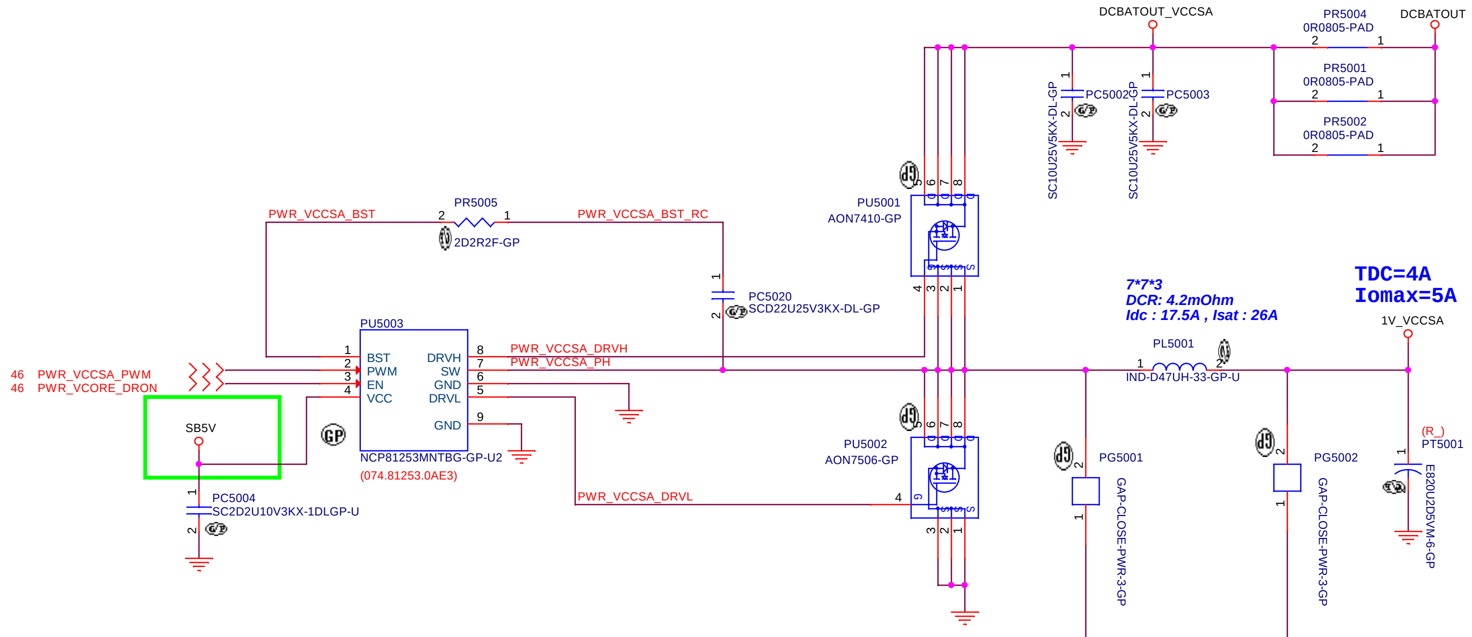
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 048_NCP81206MN_CPU_VCCGT(3/3)

Size	Document Number	Rev
A3	Rosa_SKL-U AIO	-1

Date: Wednesday, July 01, 2015 Sheet 48 of 105

Blanking

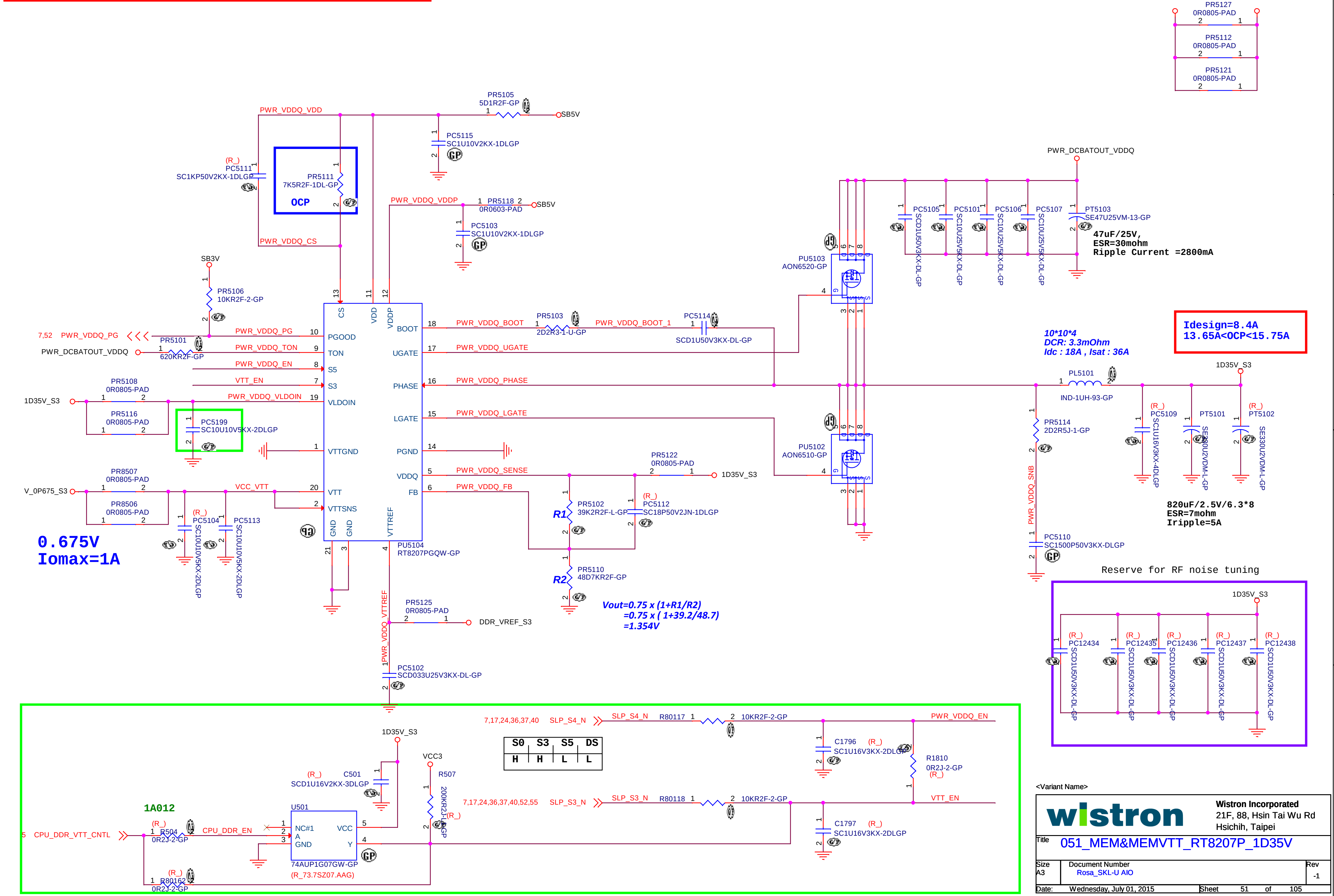


<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	050_NCP81253MN_CPU_VCCSA	
Size A3	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 50 of 105	

SSID = PWR.Plane.Regulator_1p35v0p675v



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

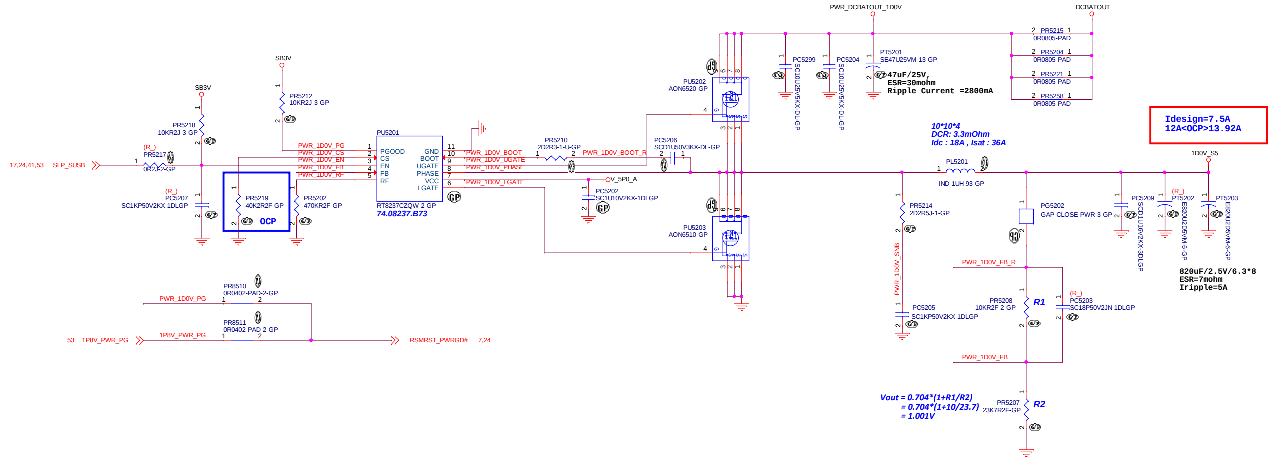
Title: 051_MEM&MEMVTT_RT8207P_1D35V

Size	Document Number	Rev
A3	Rosa_SKL-U AIO	-1

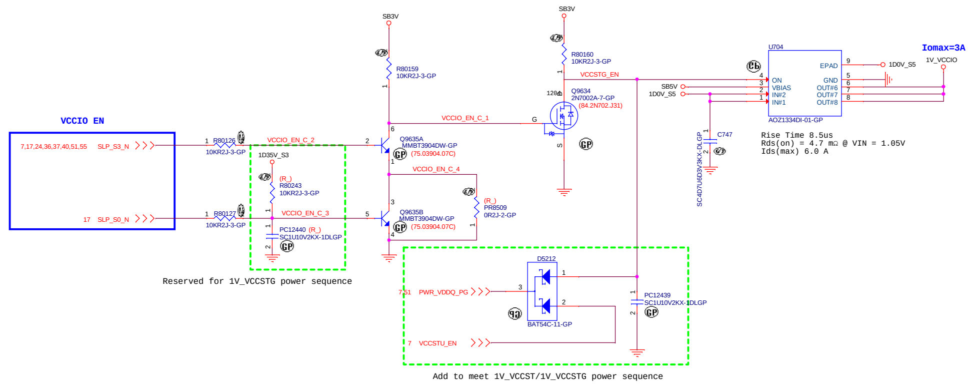
Date: Wednesday, July 01, 2015 Sheet 51 of 105

SSID = PWR.Plane.Regulator_1p0v

RT8237 for 1D0V



Load Switch for VCCIO



VCCPRIM_CORE Connects to 1D0V

Iomax=2.57A

Connection moved to page 7

<Variant Name>

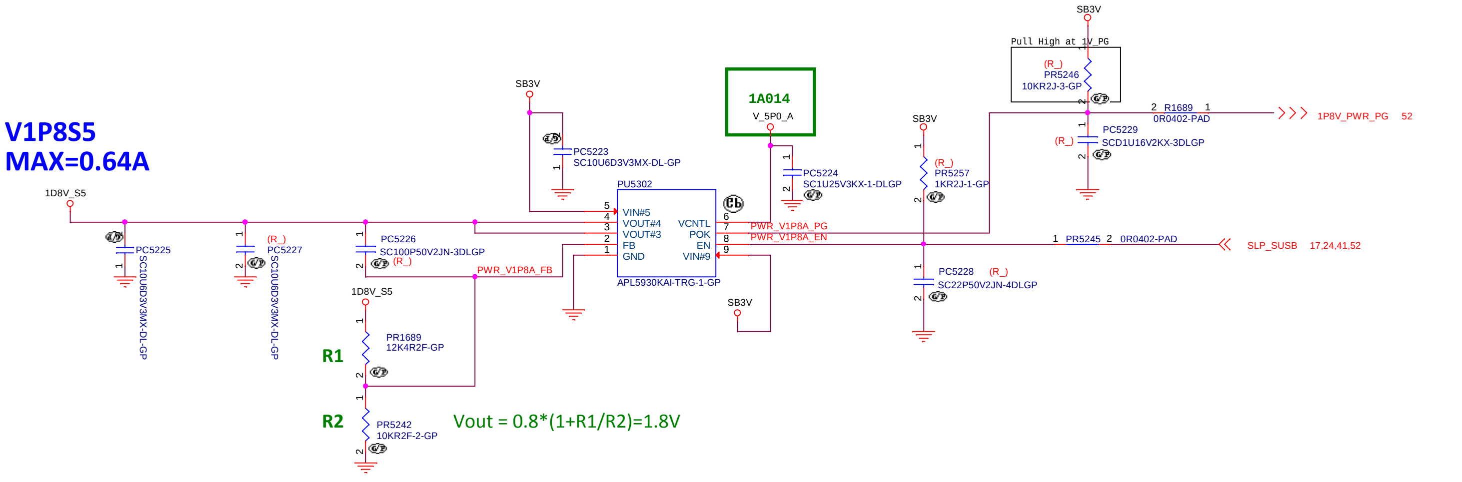
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 052_DCDC-1D0V/VCCIO/VCCPRIM

Size: Custom | Document Number: Rosa_SKL-U AIO | Rev: -1

Date: Wednesday, July 01, 2015 | Sheet 52 of 105

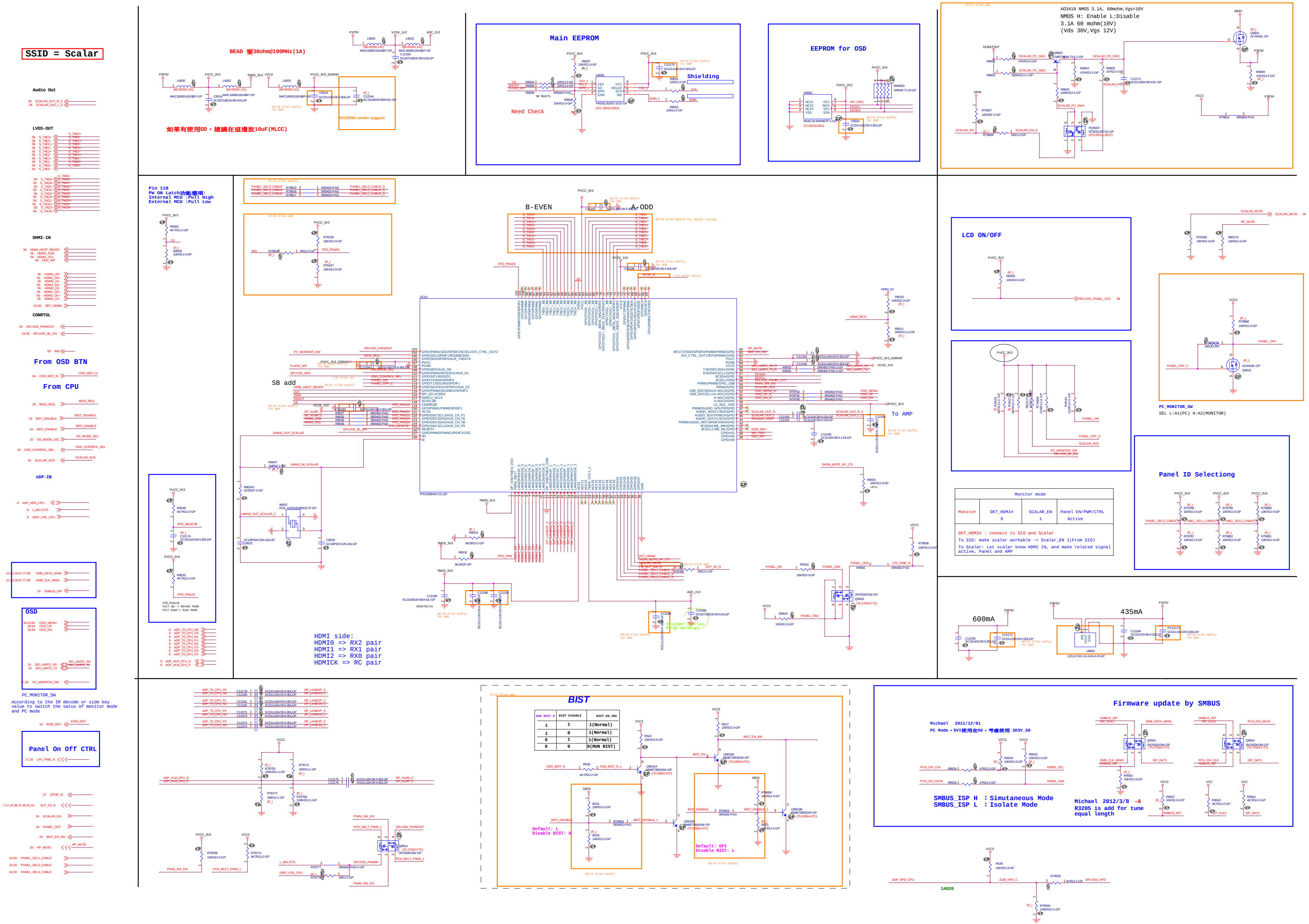


<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	053_LDO_APL5930KAI_1D8V	
Size: Custom	Document Number: Rosa_SKL-U AIO	Rev: -1
Date: Wednesday, July 01, 2015	Sheet 53 of 105	

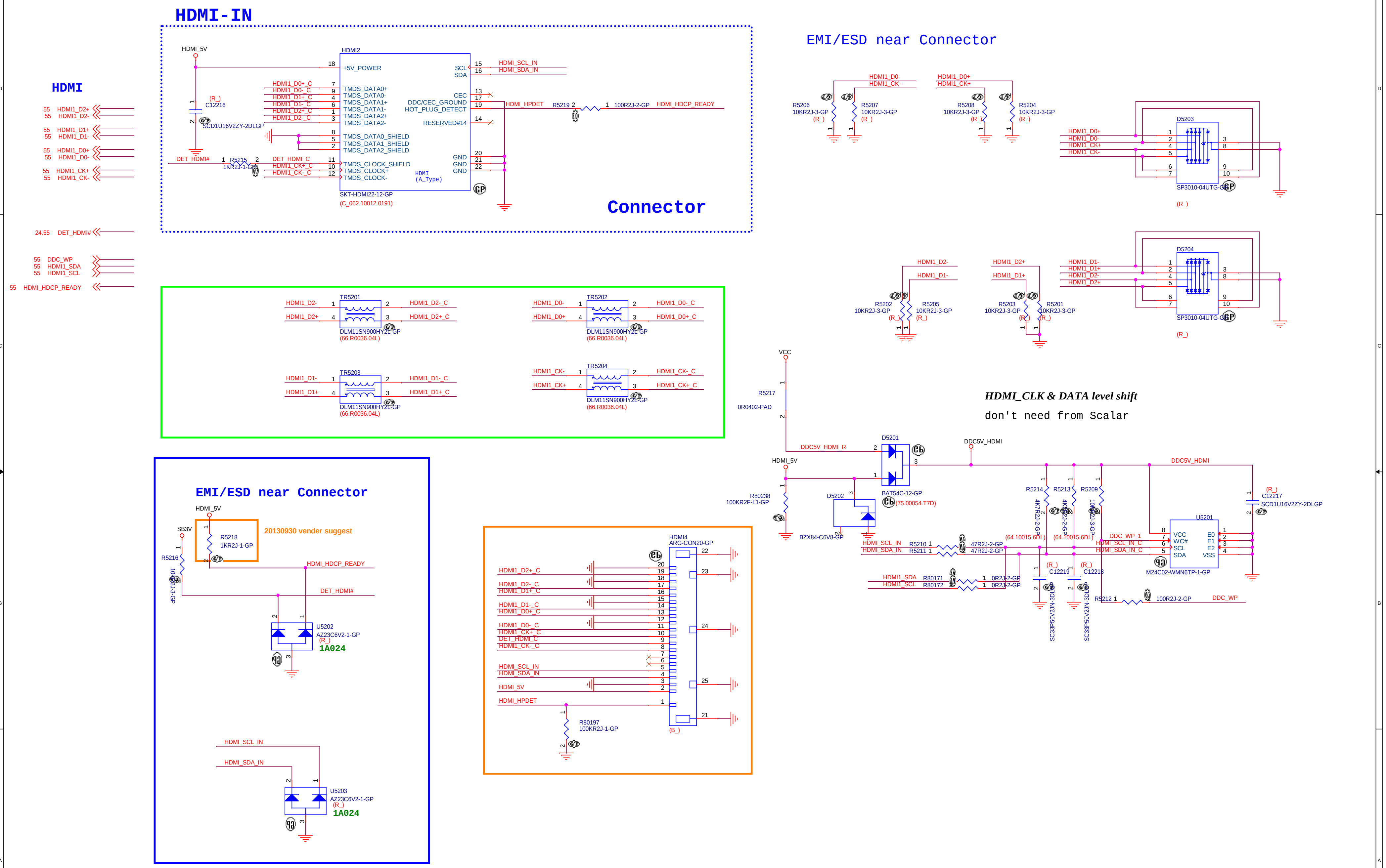
Blanking



<Variant Name>

wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	055_SCALAR
Size: E — Document Number: Rosa_SKL-U AIO	Rev: -1
Date: Wednesday, July 01, 2015	Sheet 55 of 105

HDMI-IN

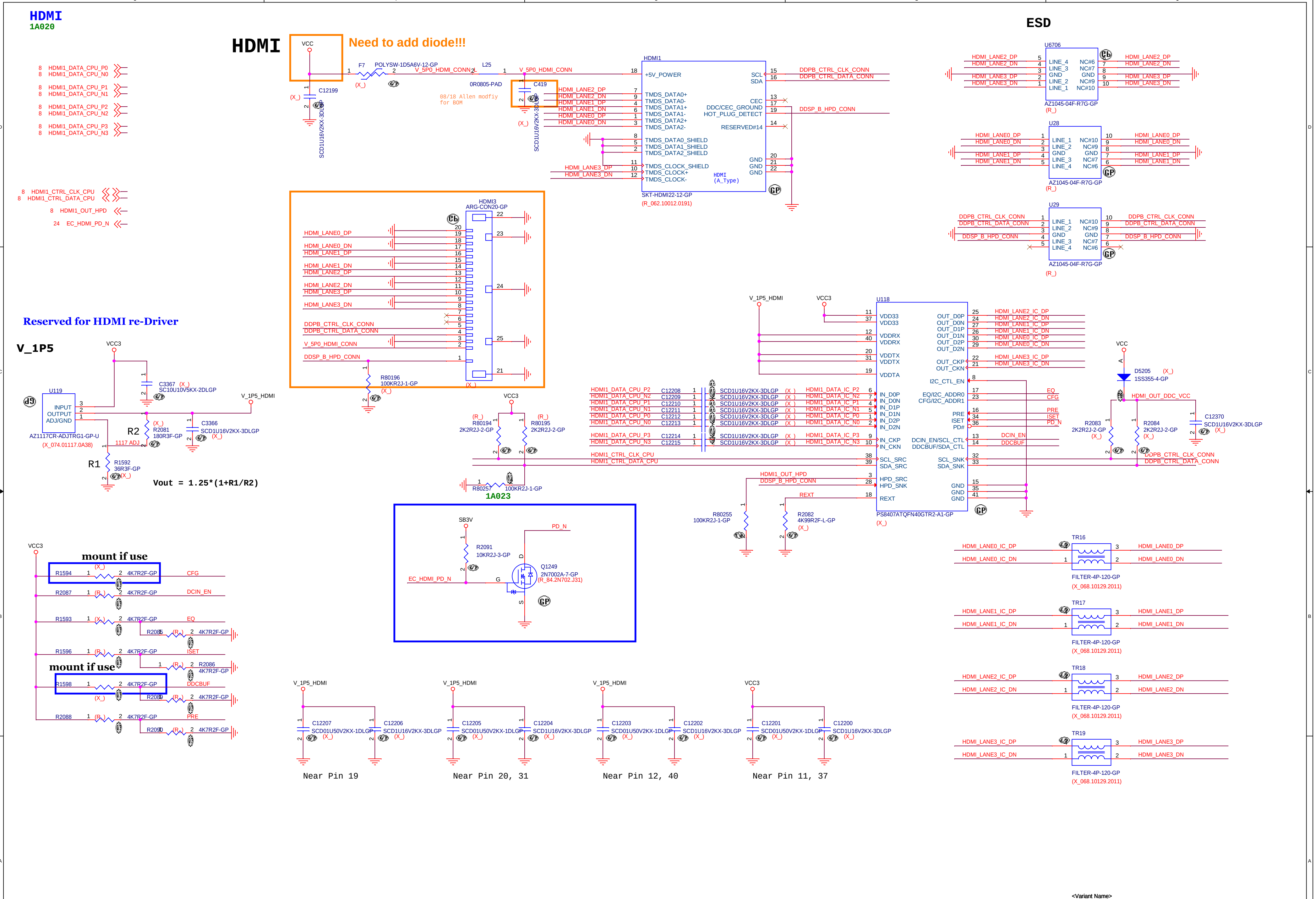


Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 056_HDMI_IN

Size: C | Document Number: Rosa_SKL-U AIO | Rev: -1

Date: Wednesday, July 01, 2015 | Sheet 56 of 105

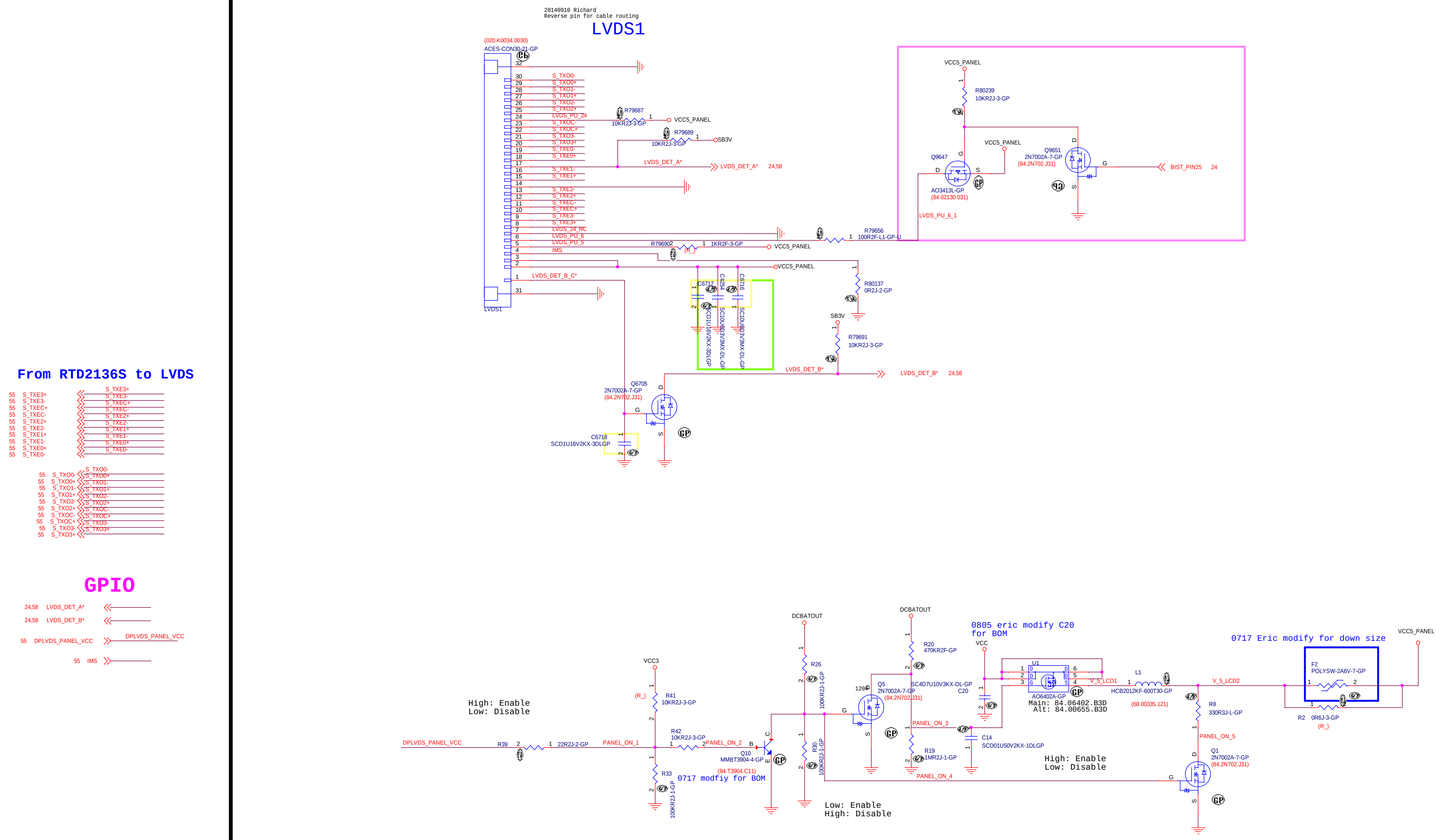


<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	057_HDMI_OUT	
Size C	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 57 of 105	

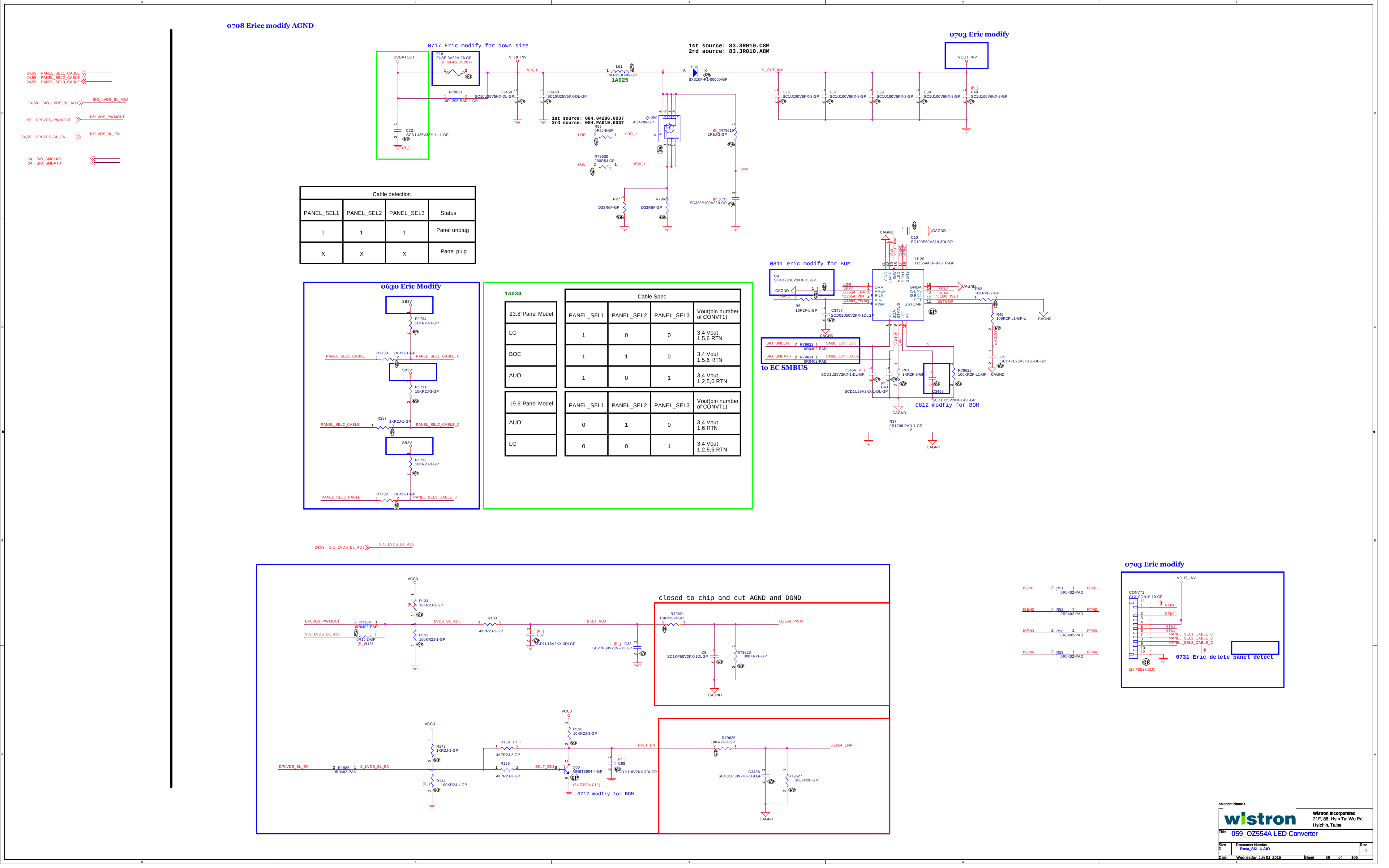


<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	058_Panel Control	
Size: Custom	Document Number: Rosa_SKL-U AIO	Rev: -1
Date: Wednesday, July 01, 2015	Sheet 58 of 105	



Cable detection

PANEL_SEL1	PANEL_SEL2	PANEL_SEL3	Status
1	1	1	Panel unplug
X	X	X	Panel plug

Cable Spec

23.8"Panel Model	PANEL_SEL1	PANEL_SEL2	PANEL_SEL3	Vout(pin number of CONVT1)
LG	1	0	0	3,4 Vout 1,5,6 RTN
BOE	1	1	0	3,4 Vout 1,5,6 RTN
AUO	1	0	1	3,4 Vout 1,2,5,6 RTN

19.5"Panel Model	PANEL_SEL1	PANEL_SEL2	PANEL_SEL3	Vout(pin number of CONVT1)
AUO	0	1	0	3,4 Vout 1,6 RTN
LG	0	0	1	3,4 Vout 1,2,5,6 RTN

<Variant Name>

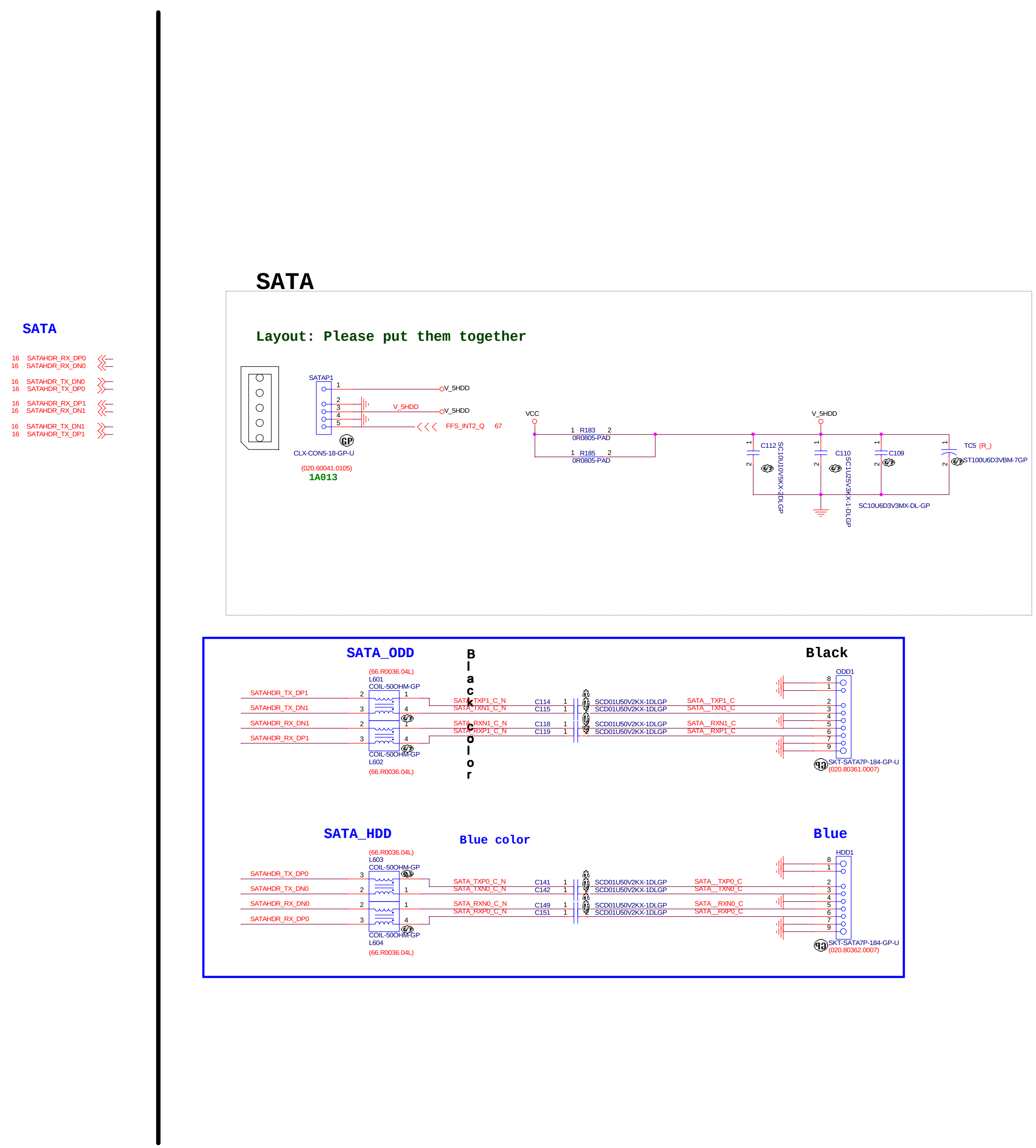
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 059_OZ554A LED Converter

Size: D | Document Number: Rosa_SKL-U AIO | Rev: -1

Date: Wednesday, July 01, 2015 | Sheet 59 of 105



<Variant Name>

wistron

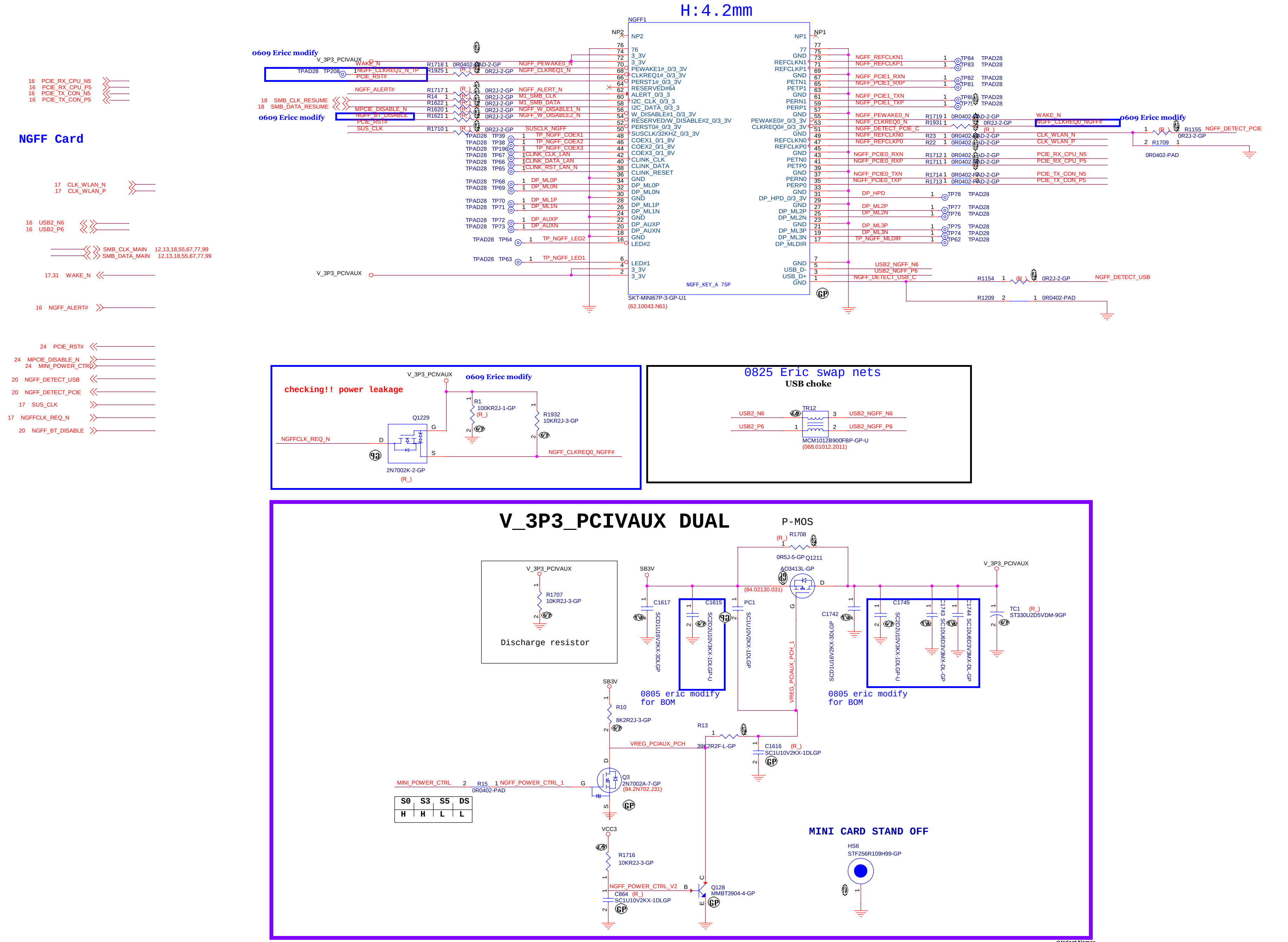
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 060_HDD/ODD

Size	Document Number	Rev
Custom	Rosa_SKL-U AIO	-1

Date: Wednesday, July 01, 2015 | Sheet 60 of 105

NGFF(A Key)



S0	S3	S5	DS
H	H	L	L

<Variant Name>

wistron

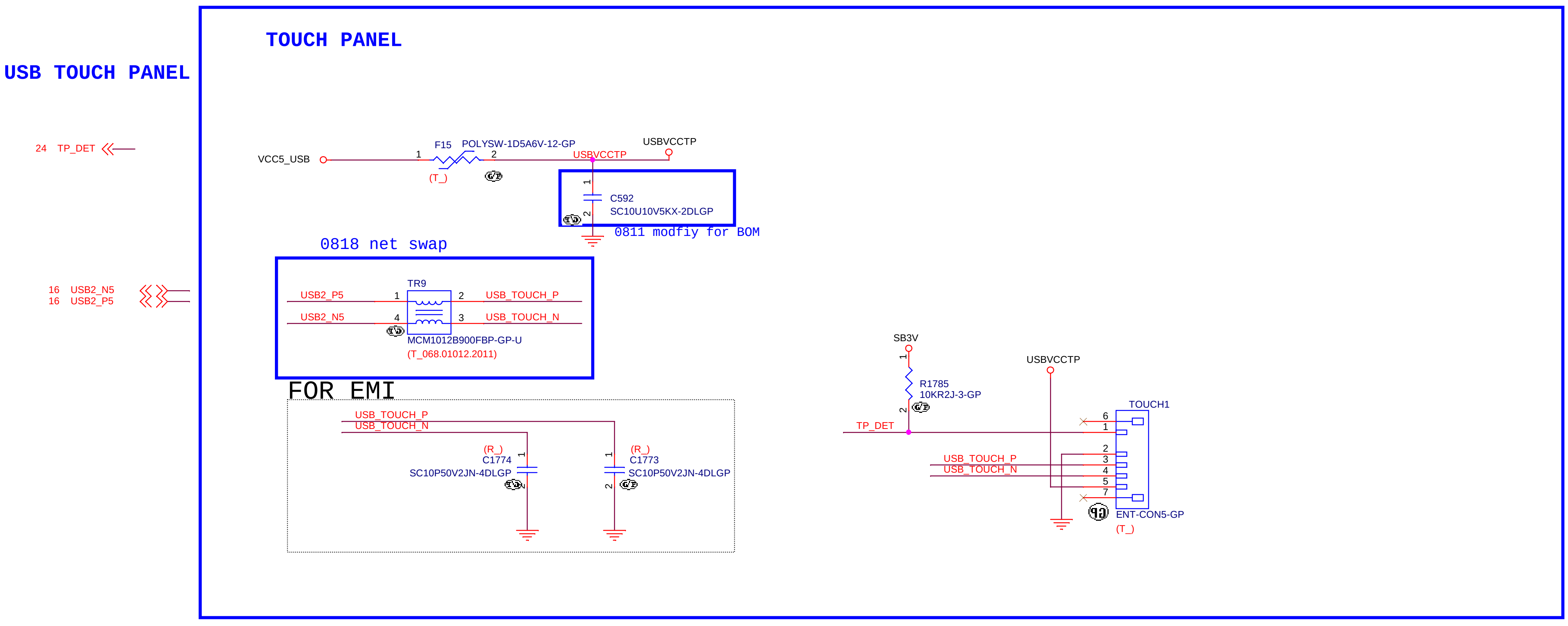
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 061_NGFF CONN

Size	Document Number	Rev
Custom	Rosa_SKL-U AIO	-1

Date: Wednesday, July 01, 2015 | Sheet 61 of 105

0626 Eric modify



<Variant Name>

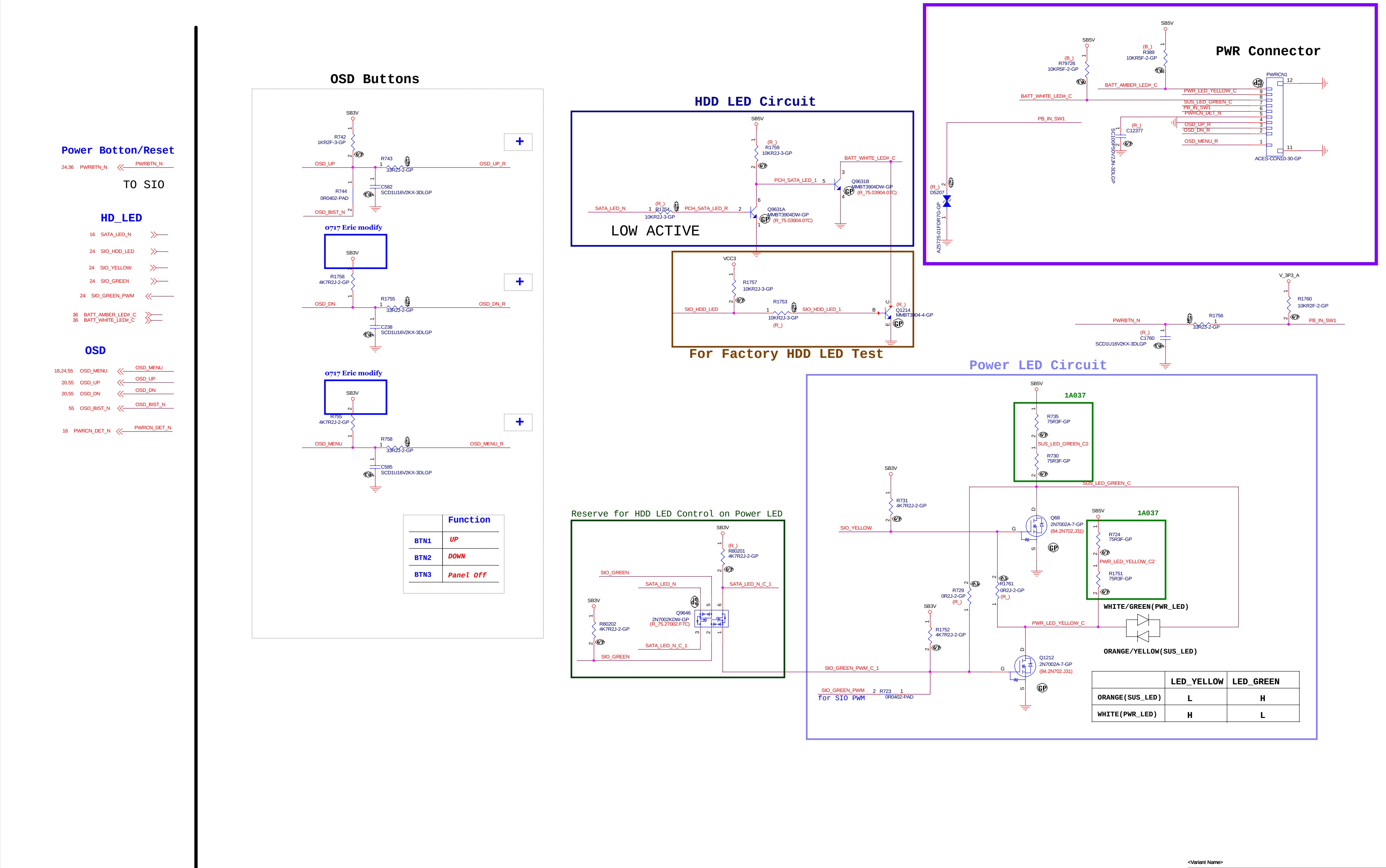
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	062_TOUCH	
Size B	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 62 of 105	

Blanking

<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	063_(Reserved)		
Size A4	Document Number Rosa_SKL-U AIO		Rev -1
Date:	Wednesday, July 01, 2015	Sheet 63 of 105	



	Function
BTN1	UP
BTN2	DOWN
BTN3	Panel Off

	LED_YELLOW	LED_GREEN
ORANGE(SUS_LED)	L	H
WHITE(PWR_LED)	H	L

Blanking

<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	065_(Reserved)		
Size A4	Document Number Rosa_SKL-U AIO		Rev -1
Date:	Wednesday, July 01, 2015	Sheet 65 of 105	

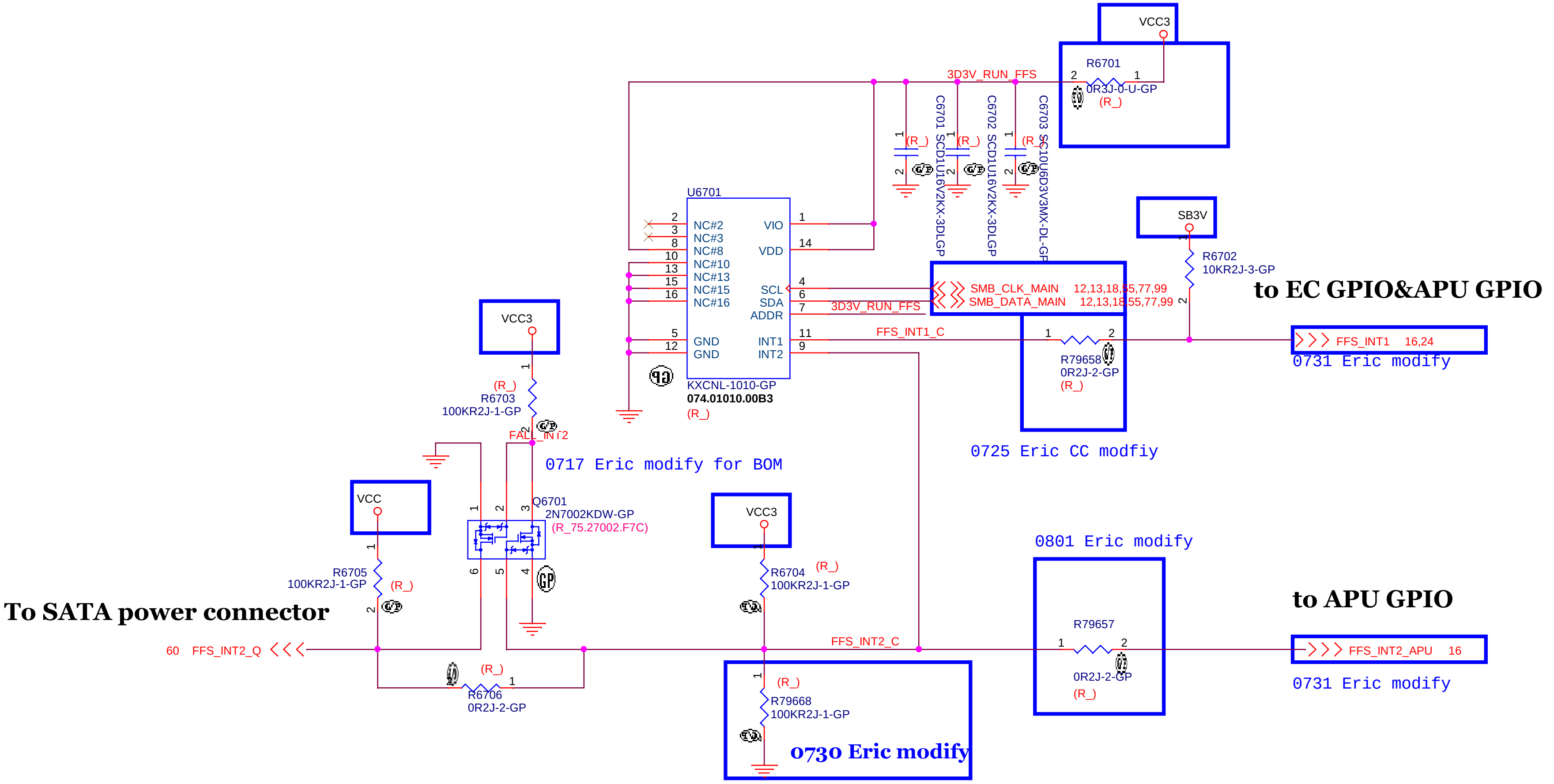
Blanking

<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	066_(Reserved)		
Size A3	Document Number Rosa_SKL-U AIO		Rev -1
Date:	Wednesday, July 01, 2015	Sheet 66 of 105	

Free Fall Sensor

0716 modfiy from PLANO



Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

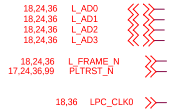
<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

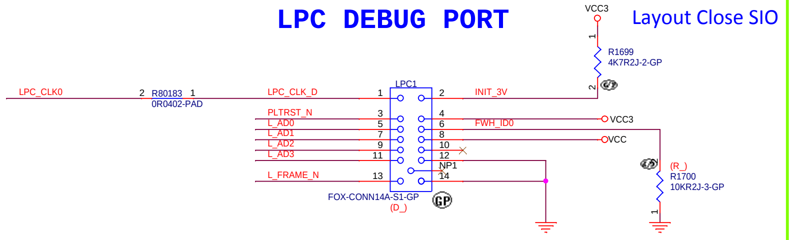
Title	067_FFS(NEW)	
Size B	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 67 of 105	

LPC DEBUG PORT



LPC DEBUG PORT

Layout Close SIO



Pin height 2.3mm

Follow Eagle

LPC

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 068_DEBUG/HDT(new)

Size	Document Number	Rev
C	Rosa_SKL-U AIO	-1

Date: Wednesday, July 01, 2015 Sheet 68 of 105

Blanking

<Variant Name>

Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	069_(Reserved)
Size: A	Document Number: Rosa_SKL-U AIO	Rev: -1
Date: Wednesday, July 01, 2015	Sheet 69 of 105

5 4 3 2 1

D C B A

Blanking

<Variant Name>

Blanking

<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	071_(Reserved)		
Size A4	Document Number Rosa_SKL-U AIO		Rev -1
Date:	Wednesday, July 01, 2015	Sheet 71 of 105	

Blanking

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	072_(Reserved)	
Size A3	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 72 of 105	

Blanking

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	073_(Reserved)	
Size A4	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 73 of 105	

Blanking

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	074_(Reserved)	
Size: A	Document Number: Rosa_SKL-U AIO	Rev: -1
Date: Wednesday, July 01, 2015	Sheet 74 of 105	

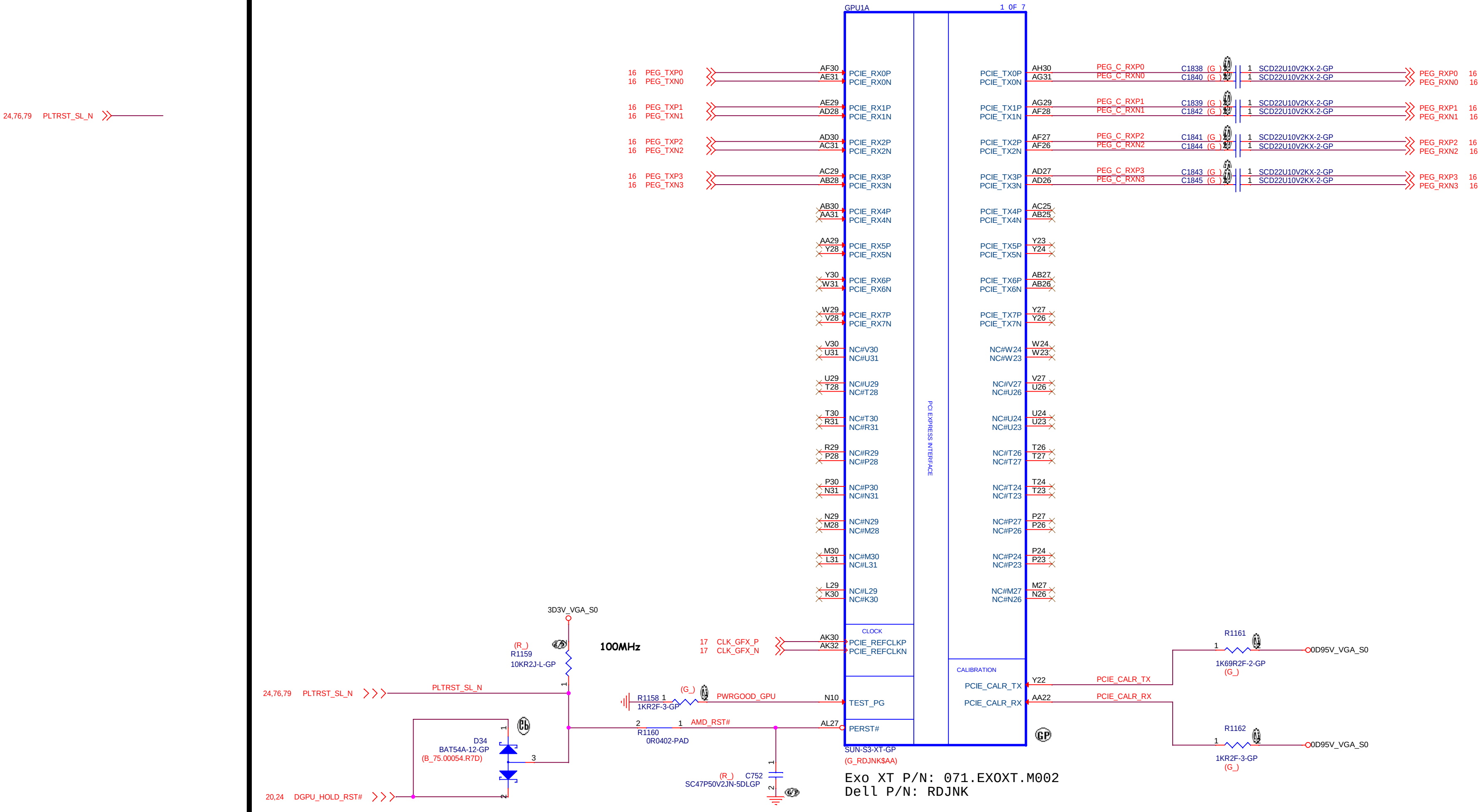
Blanking

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	075_(Reserved)	
Size A4	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 75 of 105	

PCIEX4



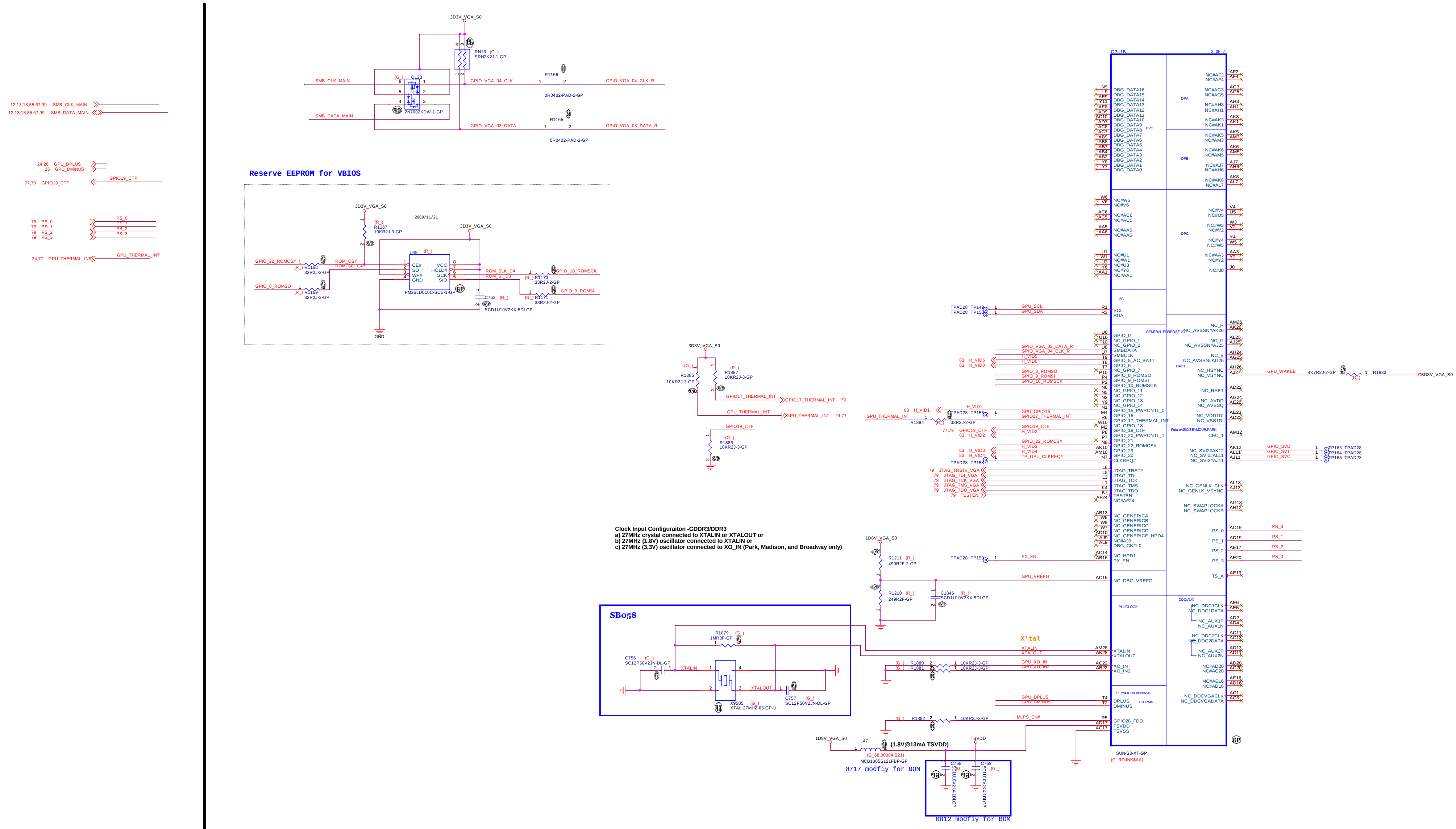
Exo XT P/N: 071.EXOXT.M002
Dell P/N: RDJNK

<Variant Name>

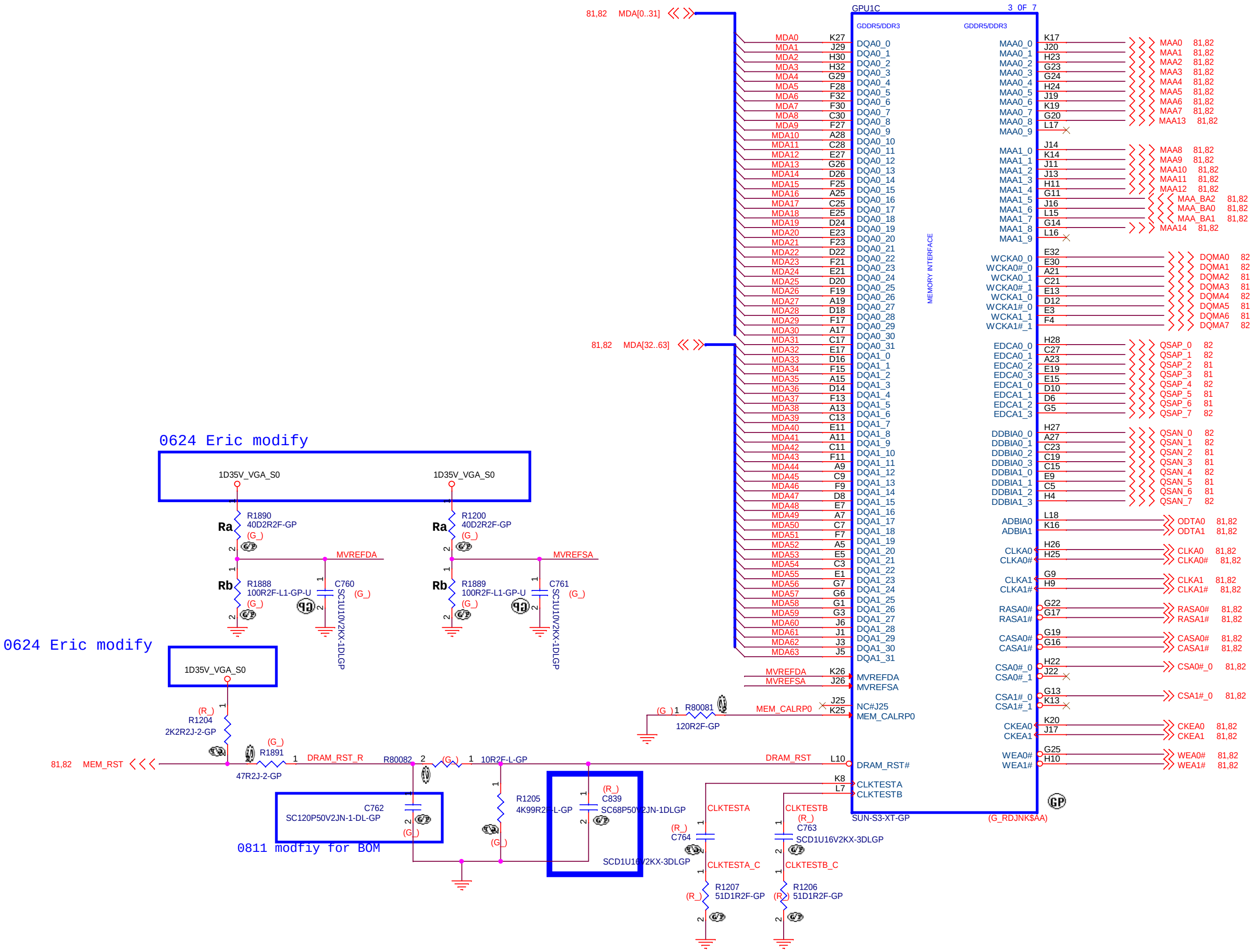
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	076_GPU_EXO(PCIE)		
Size C	Document Number Rosa_SKL-U AIO		Rev -1
Date: Wednesday, July 01, 2015		Sheet 76 of 105	



<Variant Name>
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title: 077_GPU_EXO(I/O)
Size: D
Document Number: Rosa_SKL-U AIO
Rev: -1
Date: Wednesday, July 01, 2015
Sheet 77 of 105



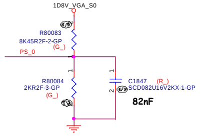
<Variant Name>

wistron

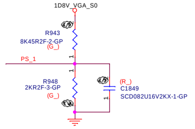
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	078_GPU_EXO(MEMORY)	
Size C	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 78 of 105	

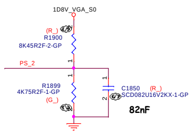
Aperture Size = 256MB
11001



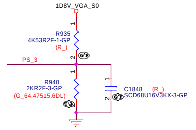
PS_1[1]=1 => PCIe GEN3 is supported
11001



11000

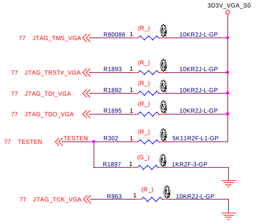


PS_3[3-1] => MEM_ID setting, need decide for AMD
11000



JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"0"(PD)	"1"(PU)	"0"(PD)
JTAG_TRST#	"1"(PU)	"1"(PU)	NC
JTAG_TCK	"0"(PD)	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC



000: Samsung
001: Hynix
010: Micron

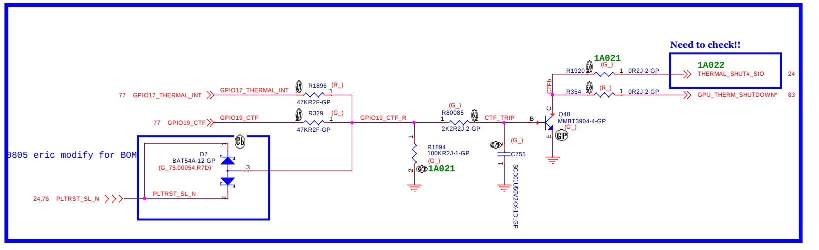
Table 3–22 Resistor Divider Lookup Table for Bits [3:1]

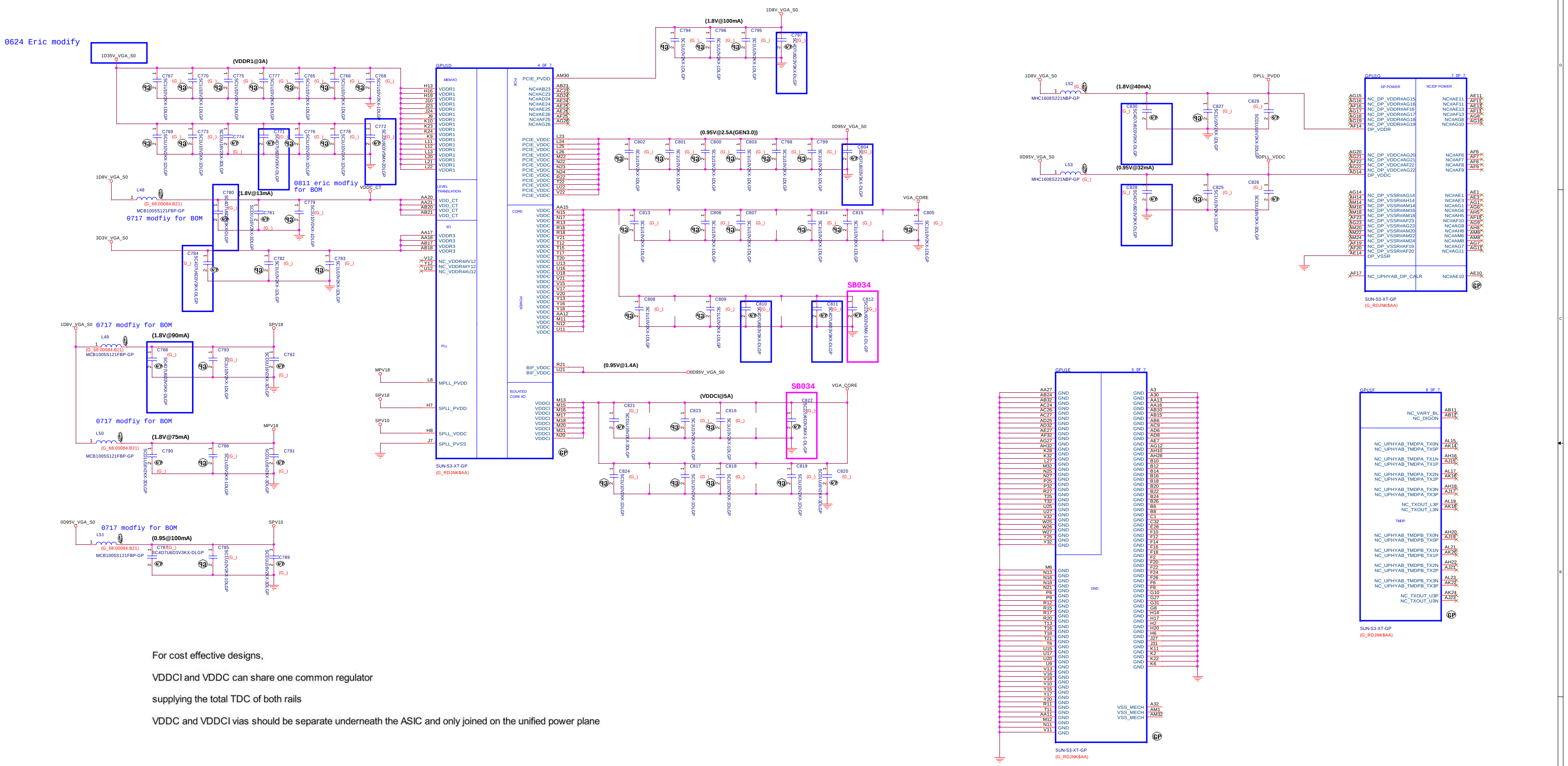
R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010

PS_2[4]	STRAP_BIF_VGA_DIS	VGA disable determines whether or not the card will be recognized as the system's VGA controller (through the SUBCLASS field in the PCI configuration space). 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_2[5]	N/A	Reserved	N/A
PS_0[4]	N/A	Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_ PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	Design dependent, see the description.

PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID	Design dependent, see the description.
PS_3[4] PS_3[5]	AUD_PORT_CONN_ PINSTRAP[1] AUD_PORT_CONN_ PINSTRAP[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user. This should be set to the maximum number of digital display audio outputs that can be enabled simultaneously in the product, which is limited by the ASIC silicon itself, the number and type of connectors on the board (DP/HDMI), and the number of sinks for each DP connector (the DP MST link policy of the video driver). Unused endpoints should be disabled. This pin strap is encoded as an active low binary as follows to ensure zero enables all endpoints. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	Design dependent, see the description.

THERMAL PROTECTION





For cost effective designs,

VDDCI and VDDC can share one common regulator

supplying the total TDC of both rails

VDDC and VDDCI vias should be separate underneath the ASIC and only joined on the unified power plane

For designs that target maximal performance,

a dedicated regulator for VDDCI with two selectable output levels is required.

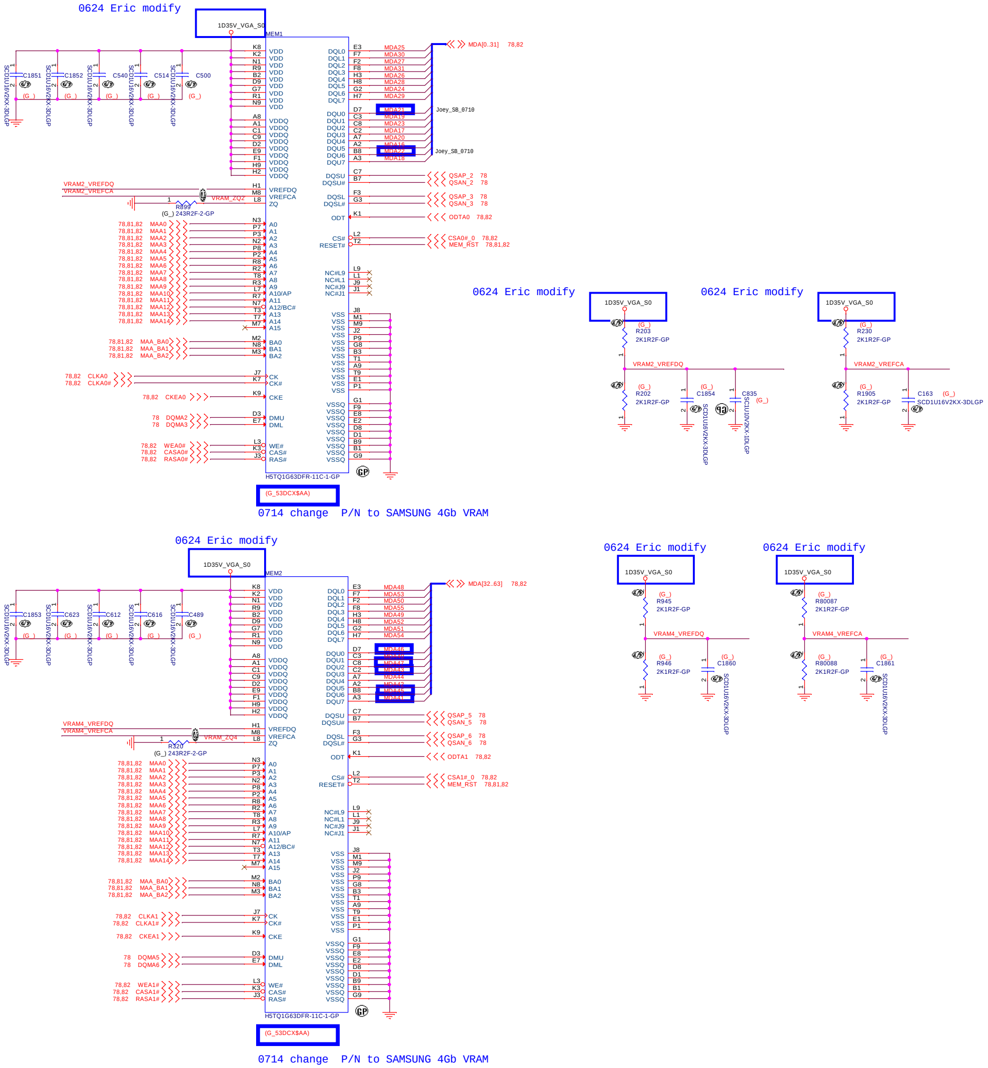
VDDCI FB is available on Topaz.

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	080_GPU_EXO(POWER)
Size D	Document Number: Rosa_SKL-U AIO
Rev	-1
Date:	Wednesday, July 01, 2015
Sheet	80 of 105



256M*16 VRAM
53DCX$AA - SAMSUNG K4W4G1646E-BC1A
PP8TP$AA - Micron MT41J256M16HA-093G:E
W5PXV$AA - Hynix H5TC4G63CFR-N0C

<Variant Name>

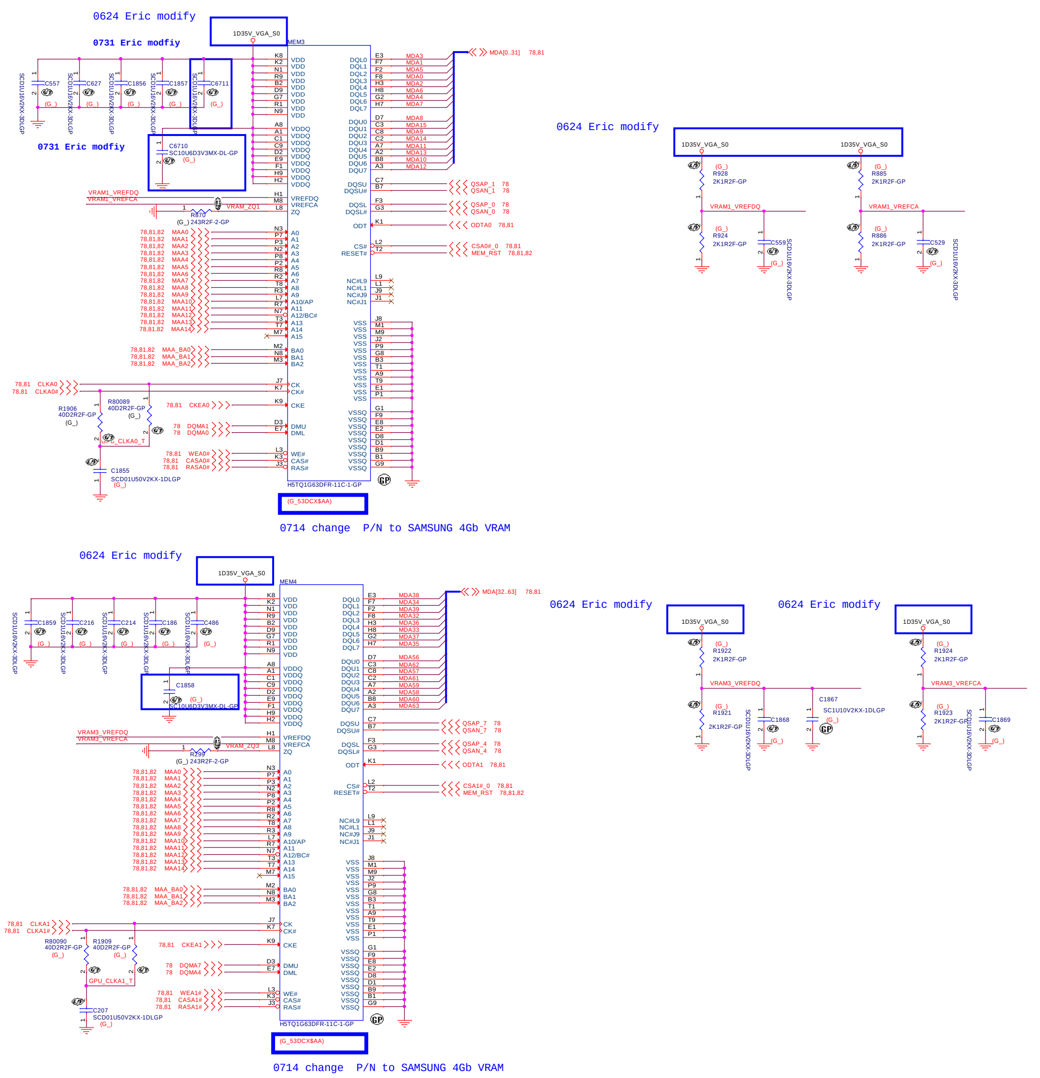
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 081_VRAM1,2(1/2)

Size: D | Document Number: Rosa_SKL-U AIO | Rev: -1

Date: Wednesday, July 01, 2015 | Sheet 81 of 105



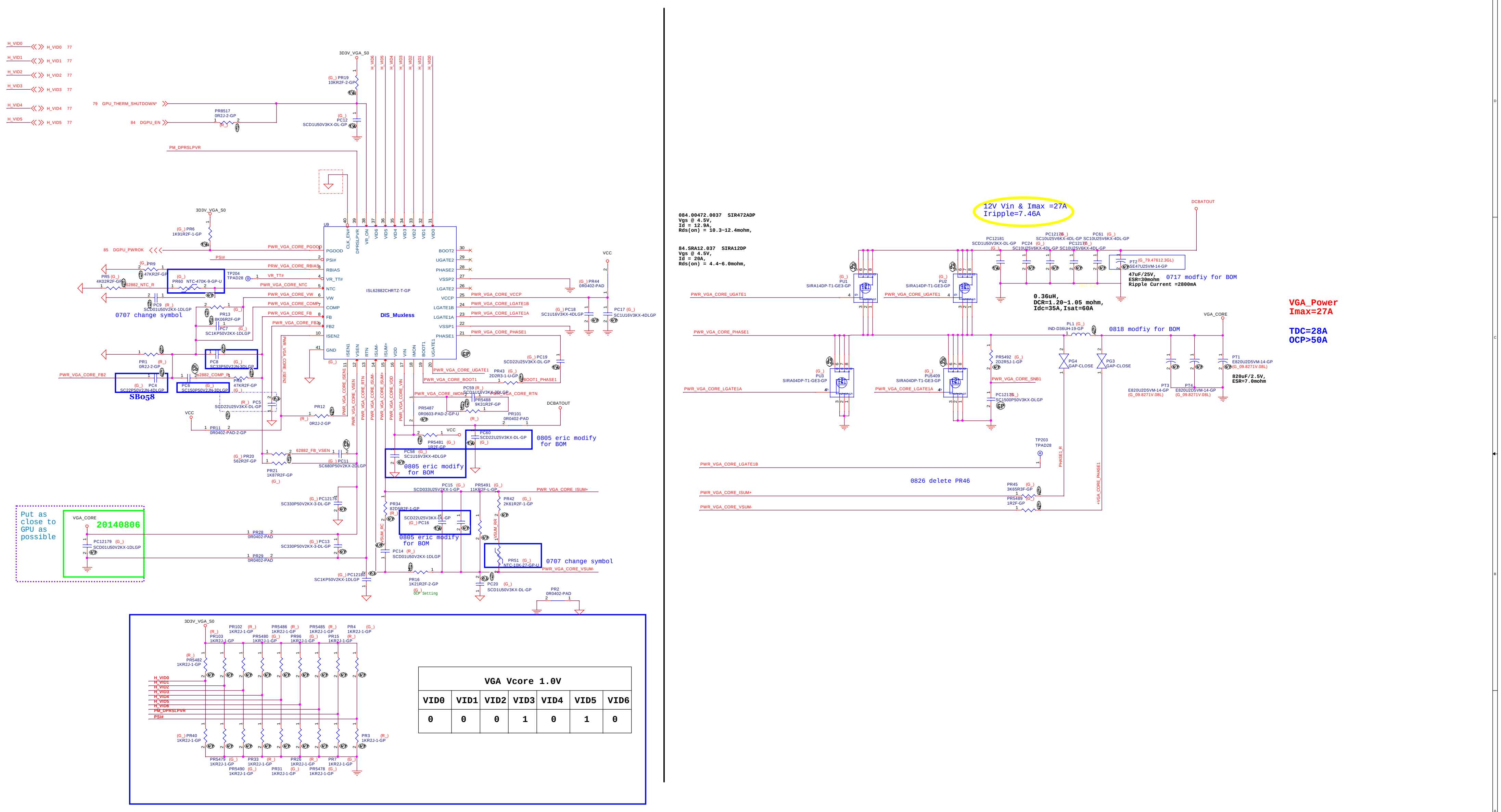
256M*16 VRAM
53DCX$AA - SAMSUNG K4W4G1646E-BC1A
PP8TP$AA - Micron MT41J256M16HA-093G:E
W5PXV$AA - Hynix H5TC4G63CFR-N0C

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	082_VRAM3,4(2/2)	
Size D	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 82 of 105	



VGA Vcore 1.0V

VID0	VID1	VID2	VID3	VID4	VID5	VID6
0	0	0	1	0	1	0

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

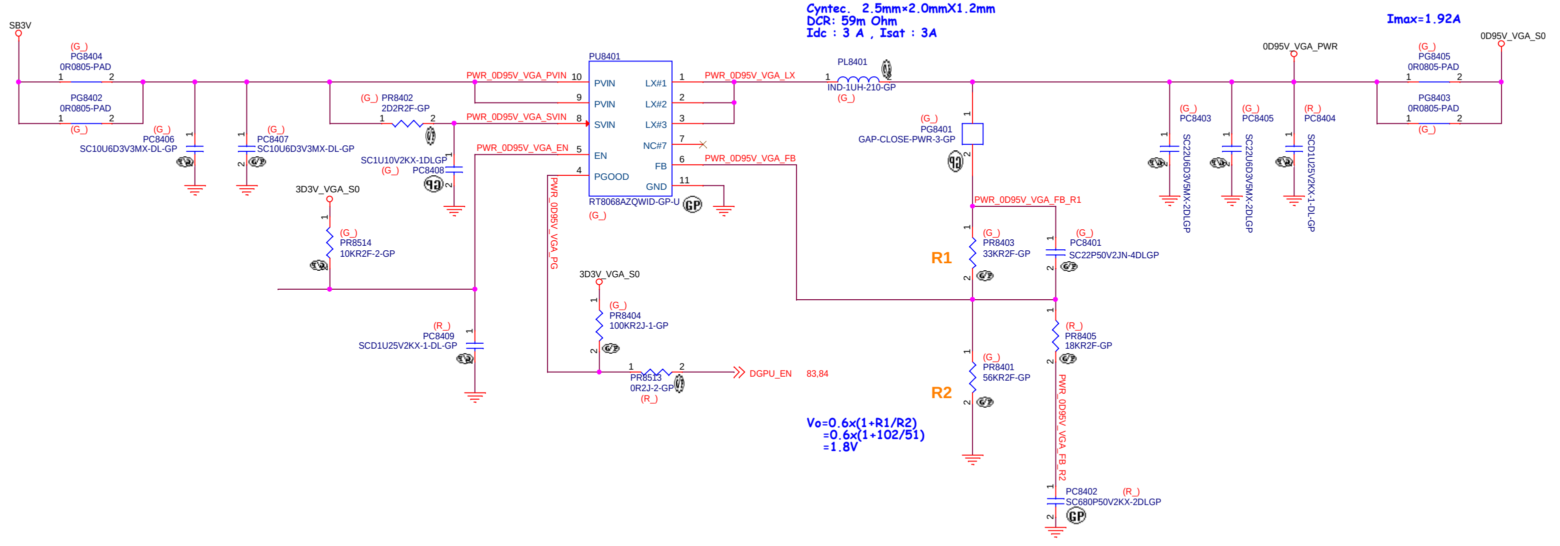
Title: 083_GPU_POWER CORE

Size: D | Document Number: Rosa_SKL-U AIO | Rev: -1

Date: Wednesday, July 01, 2015 | Sheet 83 of 105

0D95V_VGA_S0

RT8068 for 0D95_VGA

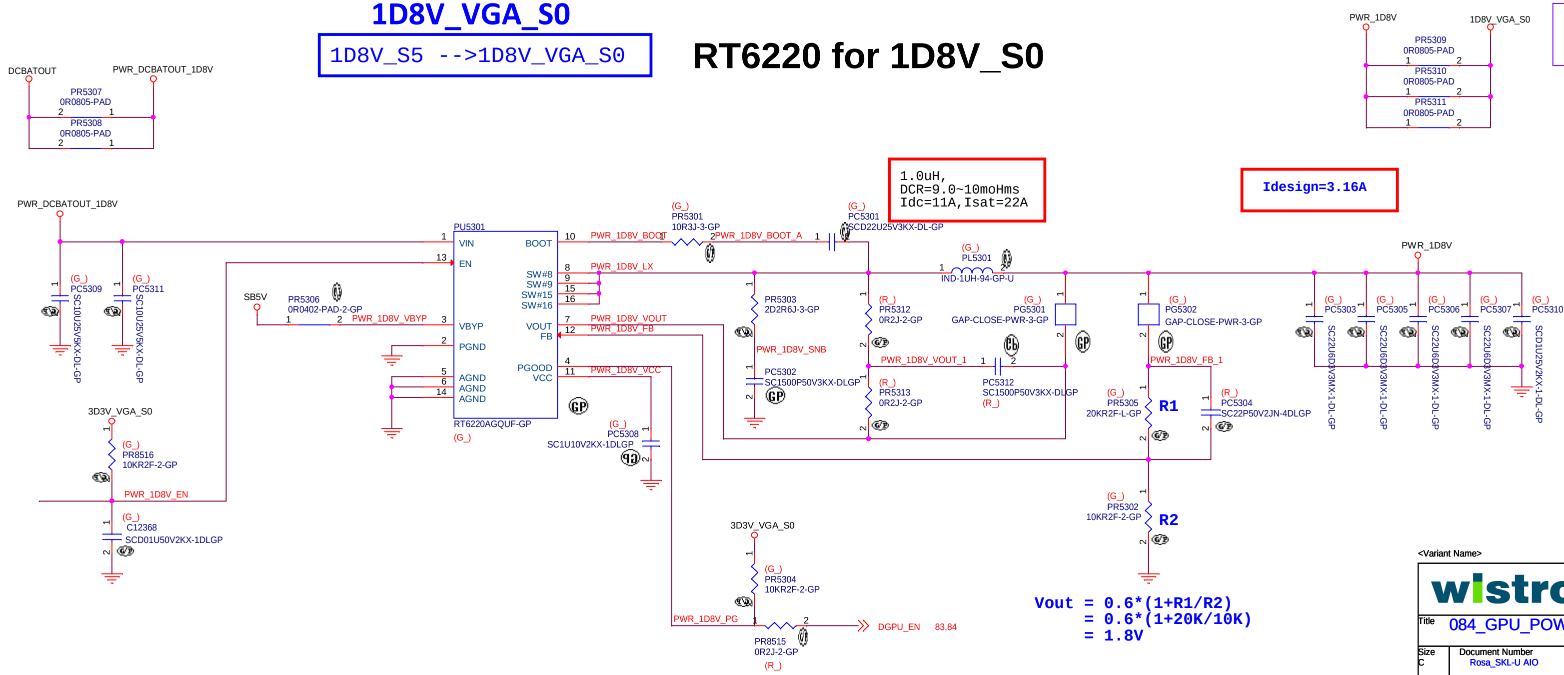


1D8V_VGA_S0

1D8V_S5 -->1D8V_VGA_S0

RT6220 for 1D8V_S0

Iomax=2A



Vout = 0.6*(1+R1/R2)
= 0.6*(1+20K/10K)
= 1.8V

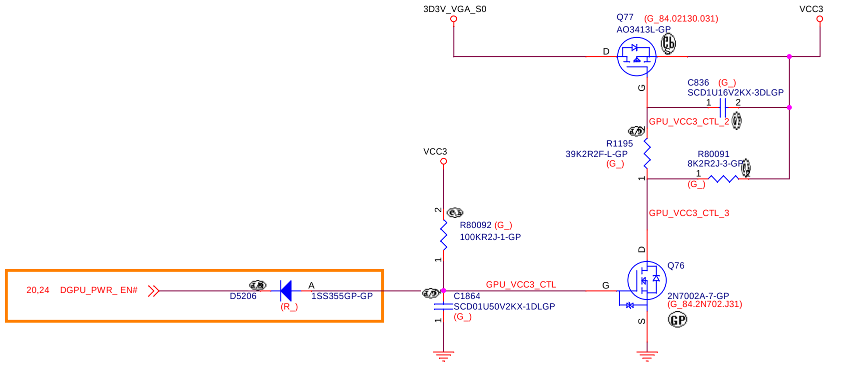
<Variant Name>

wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	084_GPU_POWER 0D95V/1D8V
Size C	Document Number Rosa_SKL-U AIO · Rev -1
Date: Wednesday, July 01, 2015	Sheet 84 of 105

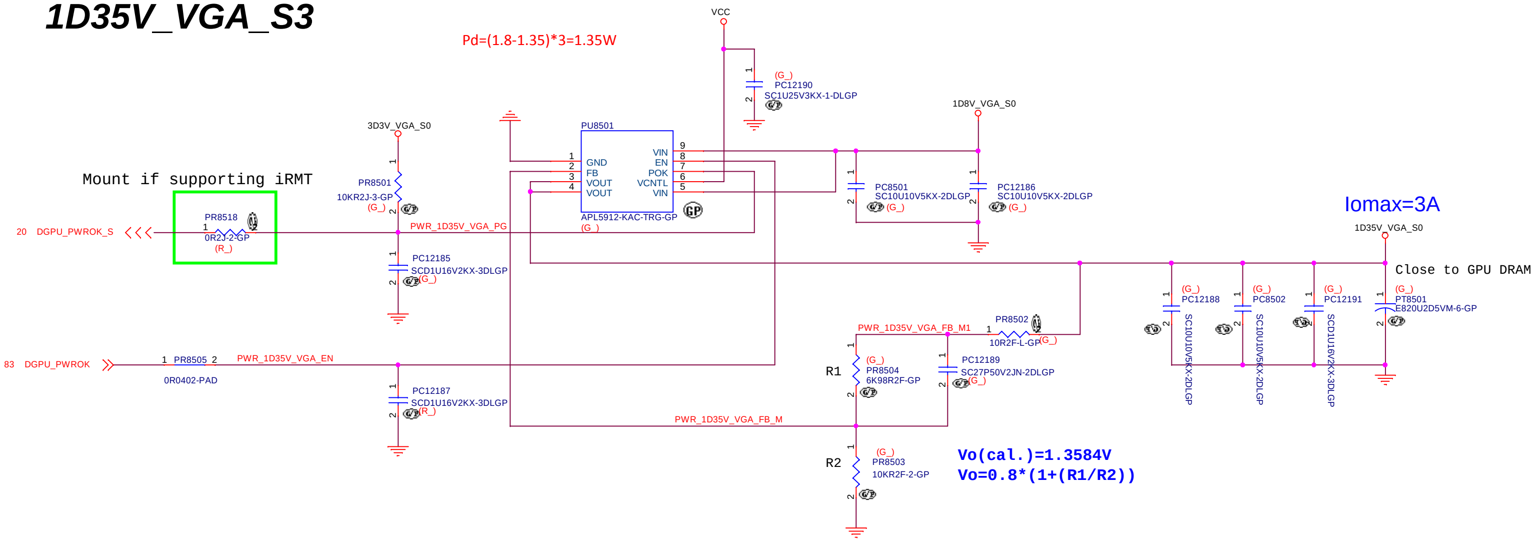
3D3V_VGA_S0

0528 Eric modify from victoria

3D3V_S0 to 3D3V_DELAY Transfer



1D35V_VGA_S3



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	085_GPU_POWER 3D3V/ 1D35V	
Size: Custom	Document Number: Rosa_SKL-U AIO	Rev: -1
Date: Wednesday, July 01, 2015	Sheet 85 of 105	

Blanking

<Variant Name>

wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	086_(Reserved)	
Size E	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 86 of 105	

Blanking

<Variant Name>

	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	087_(Reserved)
Size B	Document Number Rosa_SKL-U AIO — Rev -1
Date: Wednesday, July 01, 2015	Sheet 87 of 105

Blanking

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	088_(Reserved)		
Size B	Document Number Rosa_SKL-U AIO		Rev -1
Date:	Wednesday, July 01, 2015	Sheet 88 of 105	

Blanking

<Variant Name>

Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	089_(Reserved)
Size: A4	Document Number: Rosa_SKL-U AIO
Rev	-1
Date:	Wednesday, July 01, 2015
Sheet	89 of 105

Blanking

<Variant Name>

Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei		
Title 090_(Reserved)		
Size A4	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 90 of 105	

Blanking

<Variant Name>

wistron			Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	091_(Reserved)		
Size Custom	Document Number Rosa_SKL-U AIO		Rev -1
Date:	Wednesday, July 01, 2015	Sheet 91 of 105	

Blanking

<Variant Name>

Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei		
Title: 092_(Reserved)		
Size: C	Document Number: Rosa_SKL-U AIO	Rev: -1
Date: Wednesday, July 01, 2015	Sheet 92 of 105	

Blanking

<Variant Name>

Blanking

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	094_(Reserved)	
Size A4	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 94 of 105	

Blanking

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	095_(Reserved)	
Size A4	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 95 of 105	

Blanking

<Variant Name>

wistron	**Wistron Incorporated** 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	096_(Reserved)
Size A4	Document Number Rosa_SKL-U AIO — Rev -1
Date: Wednesday, July 01, 2015	Sheet 96 of 105

Blanking

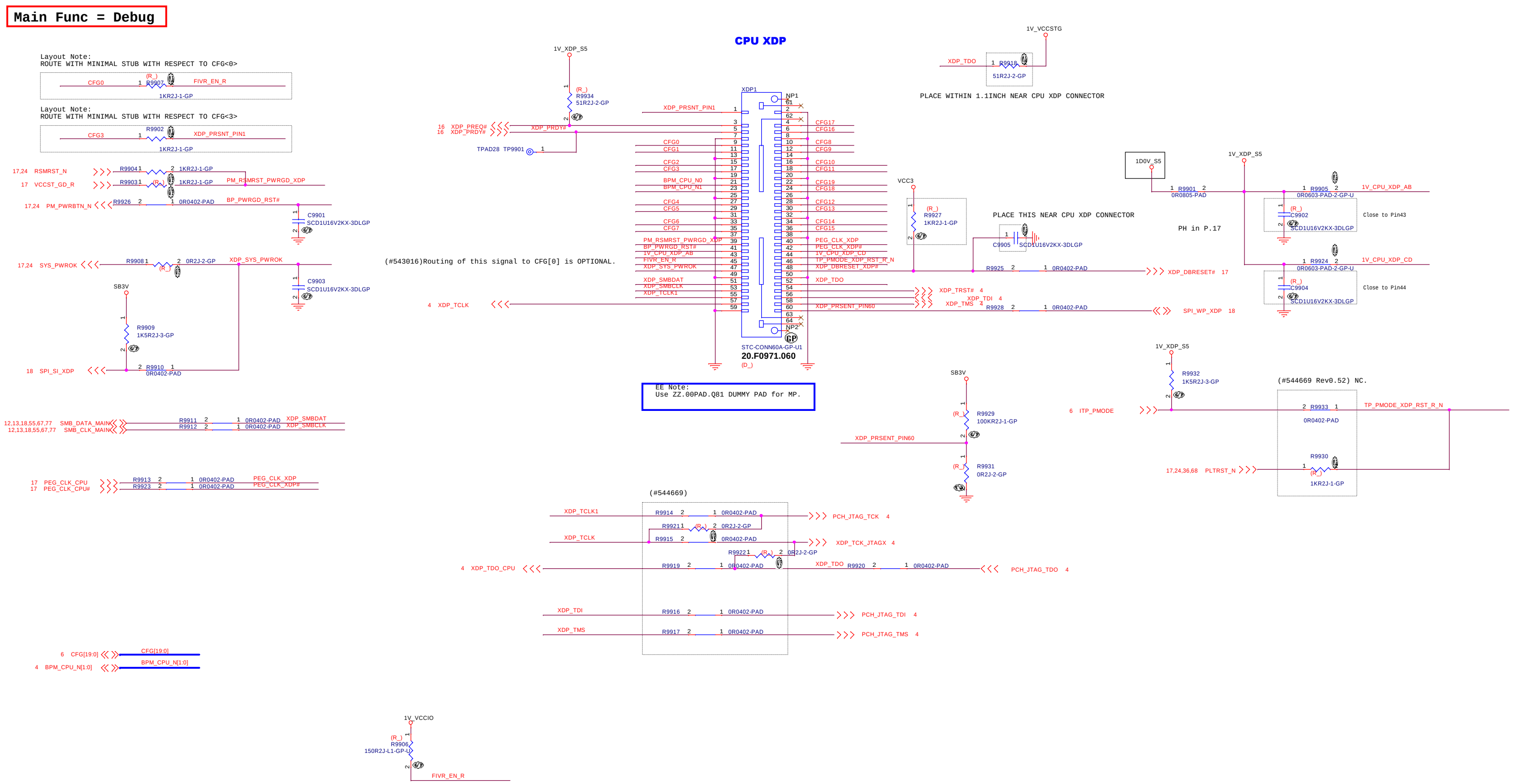
<Variant Name>

Wistron Incorporated	21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	097_(Reserved)
Size A4	Document Number Rosa_SKL-U AIO — Rev -1
Date: Wednesday, July 01, 2015	Sheet 97 of 105

Blanking

<Variant Name>

Wistron Incorporated	21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	098_(Reserved)
Size A4	Document Number Rosa_SKL-U AIO
Rev	-1
Date: Wednesday, July 01, 2015	Sheet 98 of 105


Main Func = Debug
CPU XDP
Layout Note:
ROUTE WITH MINIMAL STUB WITH RESPECT TO CFG<0>
Layout Note:
ROUTE WITH MINIMAL STUB WITH RESPECT TO CFG<3>
PLACE WITHIN 1.1INCH NEAR CPU XDP CONNECTOR
PLACE THIS NEAR CPU XDP CONNECTOR
PH in P.17
(#543016)Routing of this signal to CFG[0] is OPTIONAL.
EE Note:
Use ZZ.00PAD.Q81 DUMMY PAD for MP.
(#544669)
(#544669 Rev0.52) NC.
XDP1
STC-CONN60A-GP-U1
20.F0971.060
Close to Pin43
Close to Pin44
1V_XDP_S5
1V_VCCSTG
1V_VCCIO
VCC3
SB3V
1D0V_S5

Blanking

<Variant Name>

wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei		
Title	100_(Reserved)		
Size A4	Document Number Rosa_SKL-U AIO		Rev -1
Date: Wednesday, July 01, 2015	Sheet 100 of 105		

6-1.2-7c(2.40) stack up and impedance

疊構編號	6-1.2-7c	注意事項	1. Impedance Control tolerance +/- 10%
完成板厚 (mm)	1.2 ± 0.12		2. Coupon 製作方式及 Impedance report 請依照Wistron規範製作

Stack up

			Thickness (mil)
L1	TOP		1.7
		PP	2.7
L2	GP ※3		1.2
		Core	4
L3	Signal		1.2
		PP	24
L4	Signal		1.2
		Core	4
L5	GP		1.2
		PP	2.7
L6	Bottom		1.7
		Total	45.6

Impedance Request List

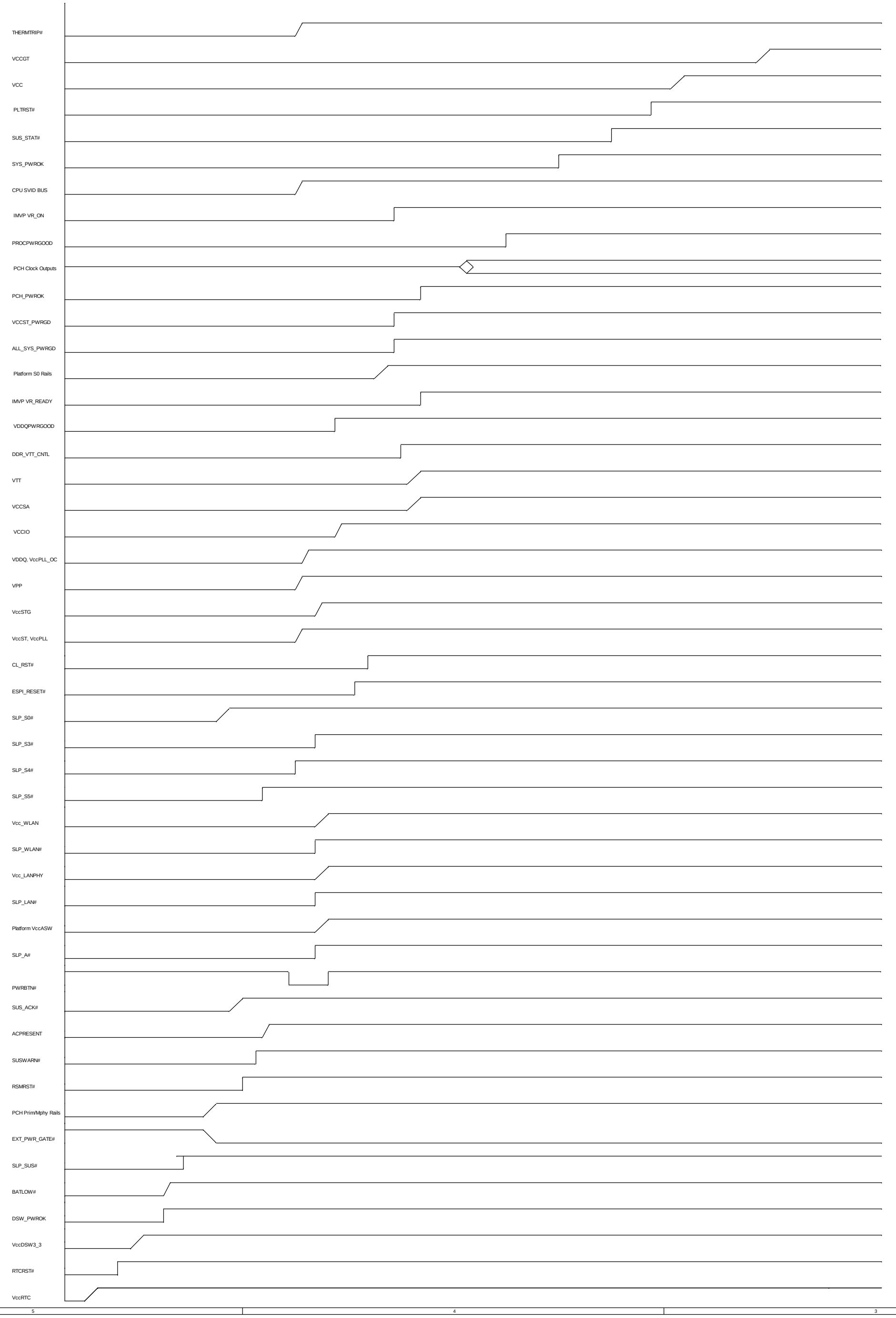
Spec \ Layer	L1 (Ref. Plane) ※1	L3 (Ref. Plane)	L4 (Ref. Plane)	L6 (Ref. Plane)
Single Ended Type (Trace width : mil)				
27.4Ω	12.0 (L2)	16.0 (L2/L5)	16.0 (L2/L5)	12.0 (L5)
33Ω	9.0 (L2)	12.0 (L2/L5)	12.0 (L2/L5)	9.0 (L5)
34Ω	8.5 (L2)	11.5(L2/L5)	11.5 (L2/L5)	8.5 (L5)
35Ω	8.0 (L2)	10.5 (L2/5)	10.5 (L2/5)	8.0 (L5)
37.5Ω	7.0 (L2)	9.5 (L2/L5)	9.5 (L2/L5)	7.0 (L5)
39Ω	6.5 (L2) ※4	9.0(L2/L5)	9.0(L2/L5)	6.5 (L5) ※4
40Ω	6.5 (L2) ※4	8.5 (L2/L5)	8.5 (L2/L5)	6.5 (L5) ※4
42Ω	5.5 (L2)	7.5 (L2/L5)	7.5 (L2/L5)	5.5 (L5)
45Ω	5.0 (L2)	6.5 (L2/L5)	6.5 (L2/L5)	5.0 (L5)
48Ω	4.5 (L2)	5.5 (L2/L5)	5.5 (L2/L5)	4.5 (L5)
50Ω	4.0 (L2)	5.0 (L2/L5)	5.0 (L2/L5)	4.0 (L5)
52Ω	3.5 (L2) ※2	4.5 (L2/L5)	4.5 (L2/L5)	3.5 (L5) ※2
55Ω	NA	4.0 (L2/L5)	4.0 (L2/L5)	NA
Differential Type (Trace width/Space width/Trace width: mil)				
110Ω	NA	3.5/13/3.5(L2/L5)	3.5/13/3.5(L2/L5)	NA
100Ω	3.5/10/3.5(L2)	4/9/4(L2/L5)	4/9/4(L2/L5)	3.5/10/3.5(L5)
95Ω	3.5/6/3.5(L2);4/10/4(L2)	4/6.5/4(L2/L5)	4/6.5/4(L2/L5)	3.5/6/3.5(L5);4/10/4(L5)
93Ω	3.5/5.5/3.5(L2);4/8/4(L2)	4/5.5/4(L2/L5);5/9/5(L2/L5)	4/5.5/4(L2/L5);5/9/5(L2/L5)	3.5/5.5/3.5(L5);4/8/4(L5)
90Ω	4/6/4(L2)	4/5/4(L2/L5); 5/8/5(L2/L5)	4/5/4(L2/L5); 5/8/5(L2/L5)	4/6/4(L5)
85Ω	4/4.5/4(L2);5/8/5(L2)	5/5.5/5(L2/L5);5/5.5/5(L2/L4)	5/5.5/5(L2/L5);5/5.5/5(L3/L5)	4/4.5/4(L5);5/8/5(L5)
80Ω	5/5/5(L2)	6/6/6(L2/L5)	6/6/6(L2/L5)	5/5/5(L5)
75Ω	6/6/6(L2)	7/6/7(L2/L5)	7/6/7(L2/L5)	6/6/6(L5)
72Ω	7/8/7(L2)	7/5/7(L2/L5)	7/5/7(L2/L5)	7/8/7(L5)
70Ω	7/6/7(L2)	8/6/8(L2/L5)	8/6/8(L2/L5)	7/6/7(L5)
68Ω	6.5/4/6.5(L2)	7.5/4/7.5(L2/L5)	7.5/4/7.5(L2/L5)	6.5/4/6.5(L5)
65Ω	8/6/8(L2)	9/5/9(L2/L5)	9/5/9(L2/L5)	8/6/8(L5)

Remark:

※ 1: "Ref. Plane" means the reference plane of the traces.
※ 2: Trace space should be wider than 4.0mil(Wistron internal only).
※ 3: G is GND, P is PWR
※ 4: Only choose one signal to control on layer L1&L6

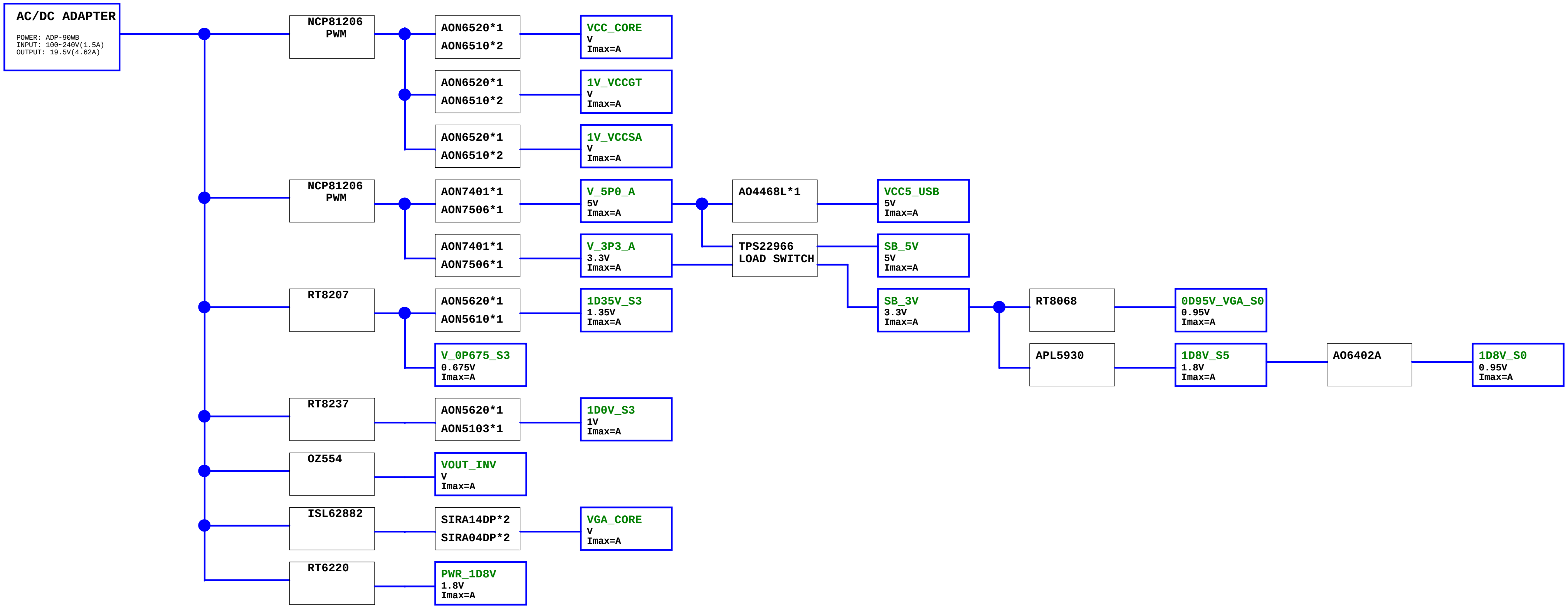
<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	101_PCB STACKUP	
Size B	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 101 of 105	



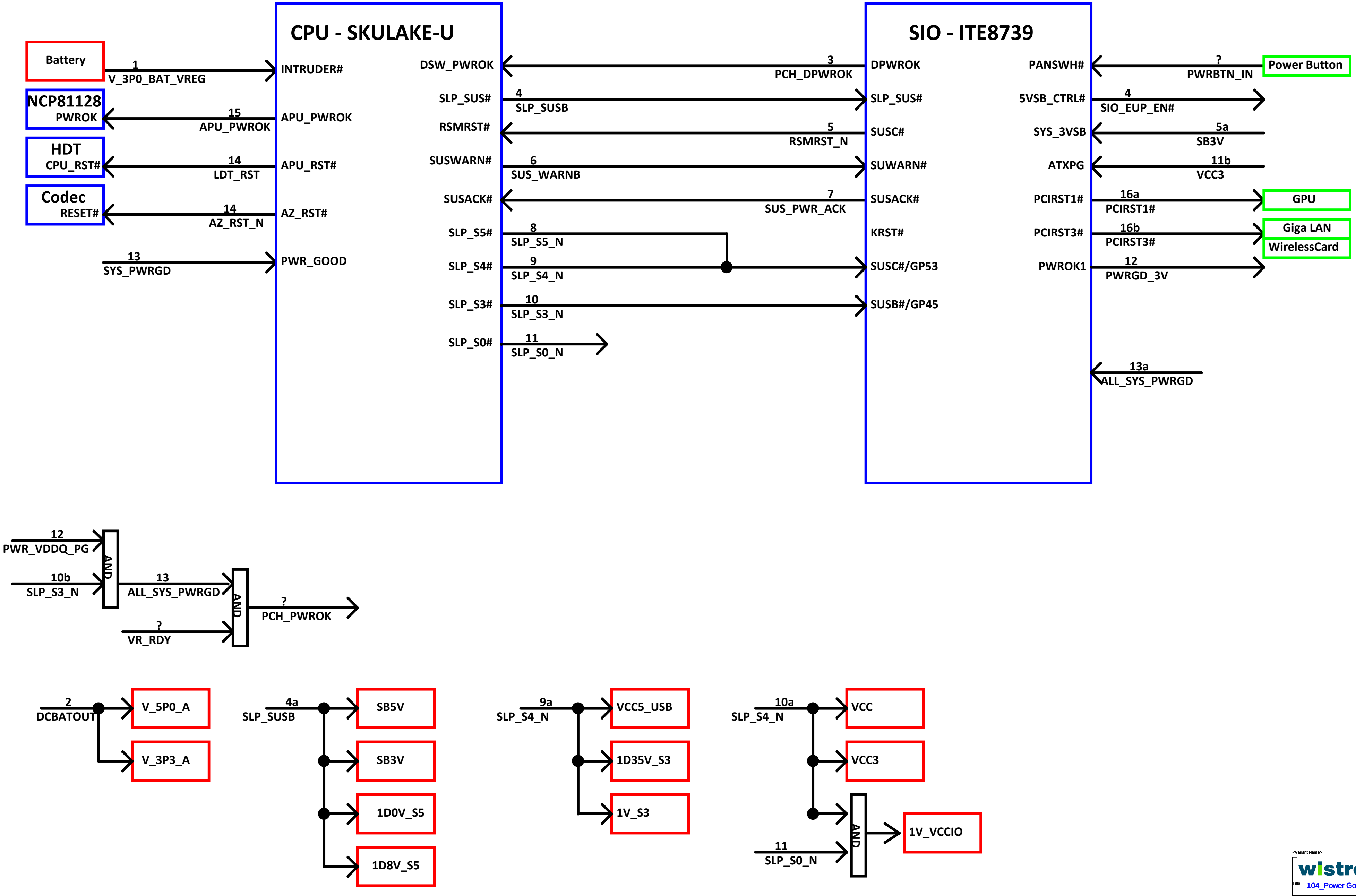
<Variant Name>

wistron	**Wistron Incorporated** 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	102_Power Sequence	
Size D	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015	Sheet 102 of 105	



<Variant Name>

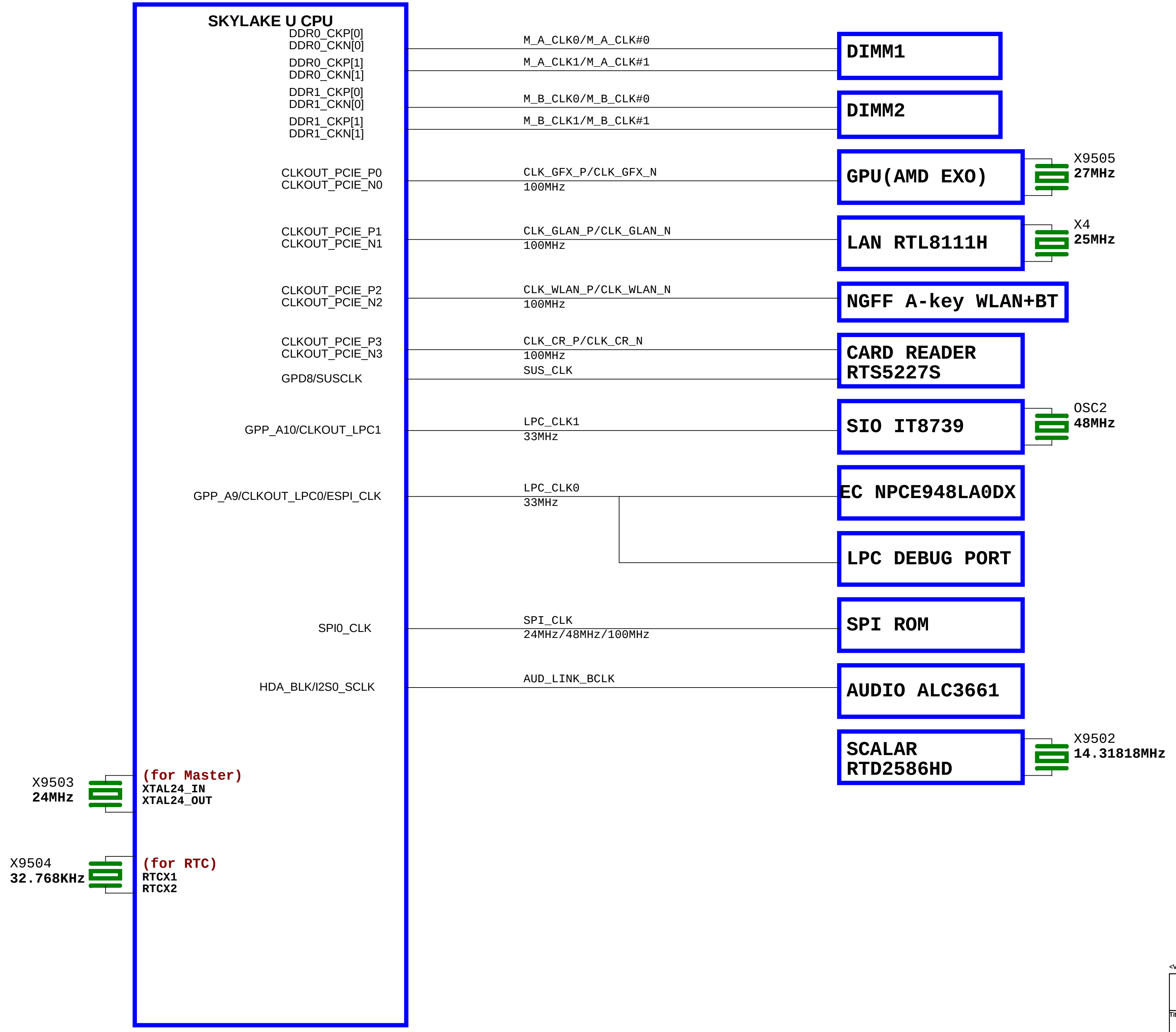
wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	103_Power Block Diagram		
Size Custom	Document Number Rosa_SKL-U AIO		Rev -1
Date:	Wednesday, July 01, 2015	Sheet 103 of 105	



<Variant Name>

wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	104_Power Good & Reset Diagram
Size D	Document Number Rosa_SKL-U AIO — Rev -1
Date: Wednesday, July 01, 2015	Sheet 104 of 105

1A035



<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 105_Clock Diagram

Size	Document Number	Rev
C	Rosa_SKL-U AIO	-1

Date: Wednesday, July 01, 2015 | Sheet 105 of 105