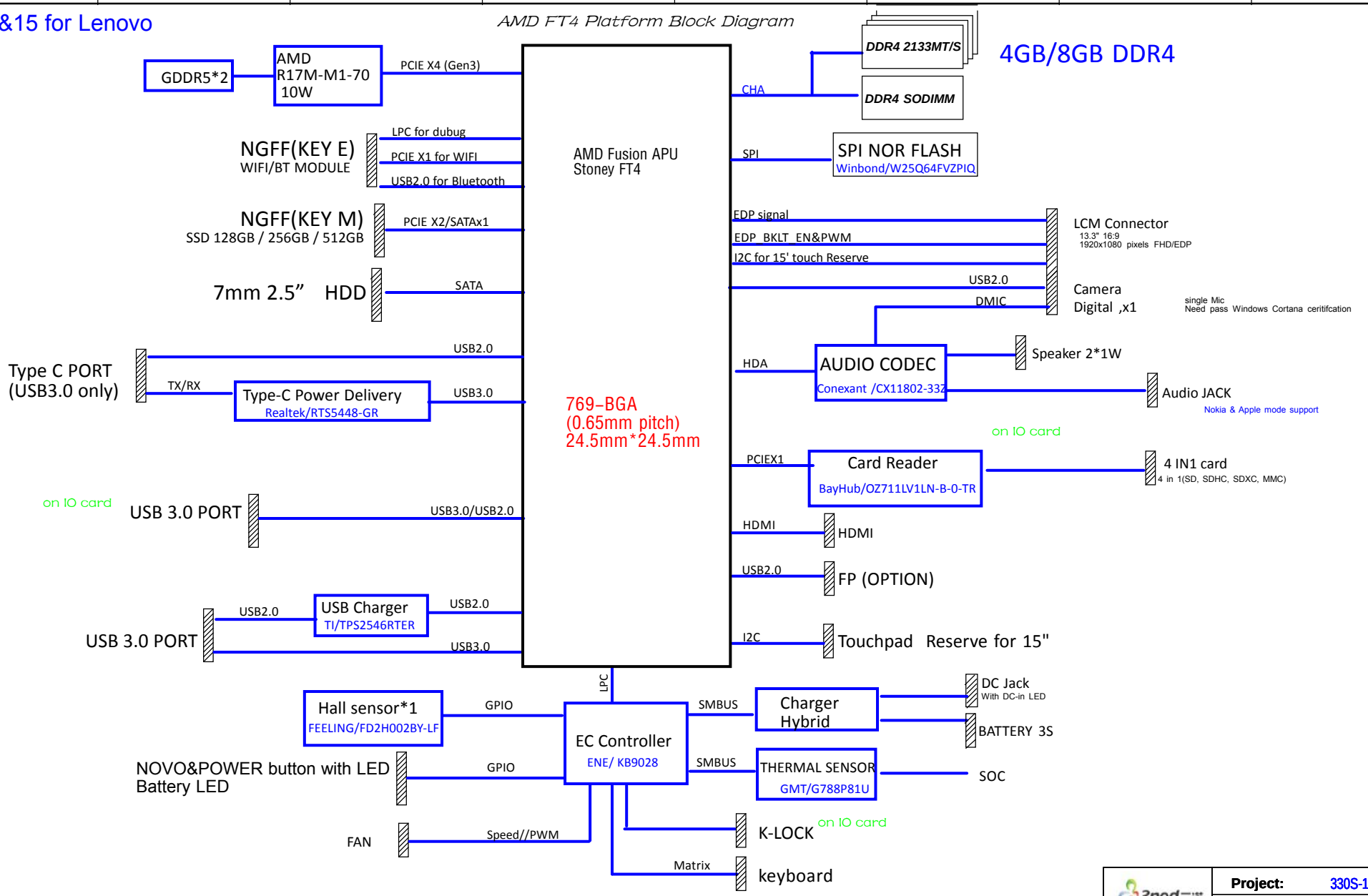
330S-14&15 for Lenovo

AMD FT4 Platform Block Diagram



3nod三诺	Project: 330S-14&15	
	Engineer: Ken	
Size: Custom	Title: Block Diagram	Rev: V01
Date: Monday, January 08, 2018	Sheet 1 of 81	

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INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd_...
Wed Jun 03 11:22:42 2015

3nod三诺	Project: 330S-14&15	
	Engineer: Ken	
Size: Custom	Title: TABLE OF CONTENTS	Rev: V01
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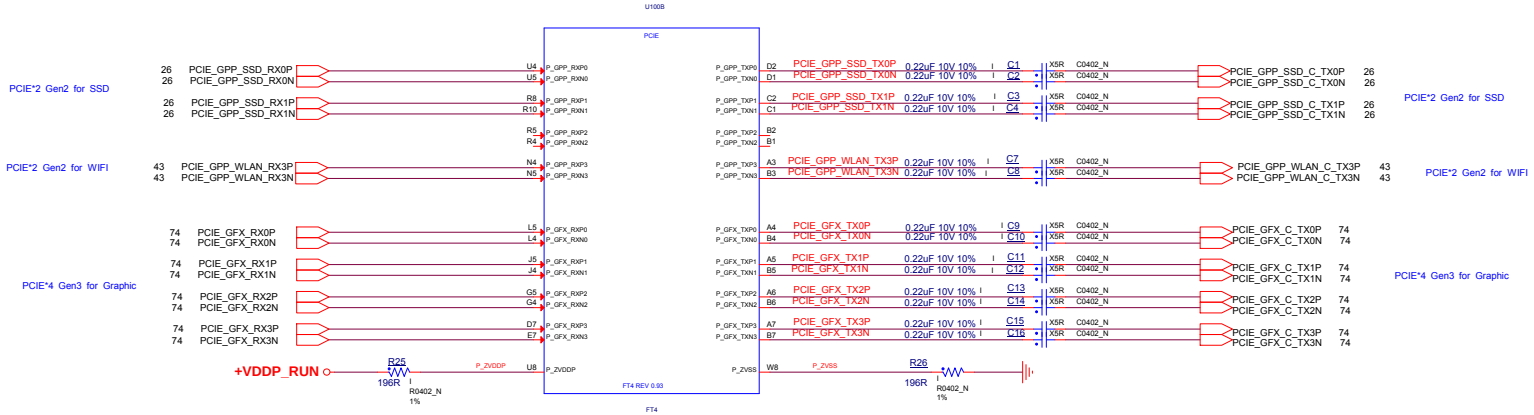
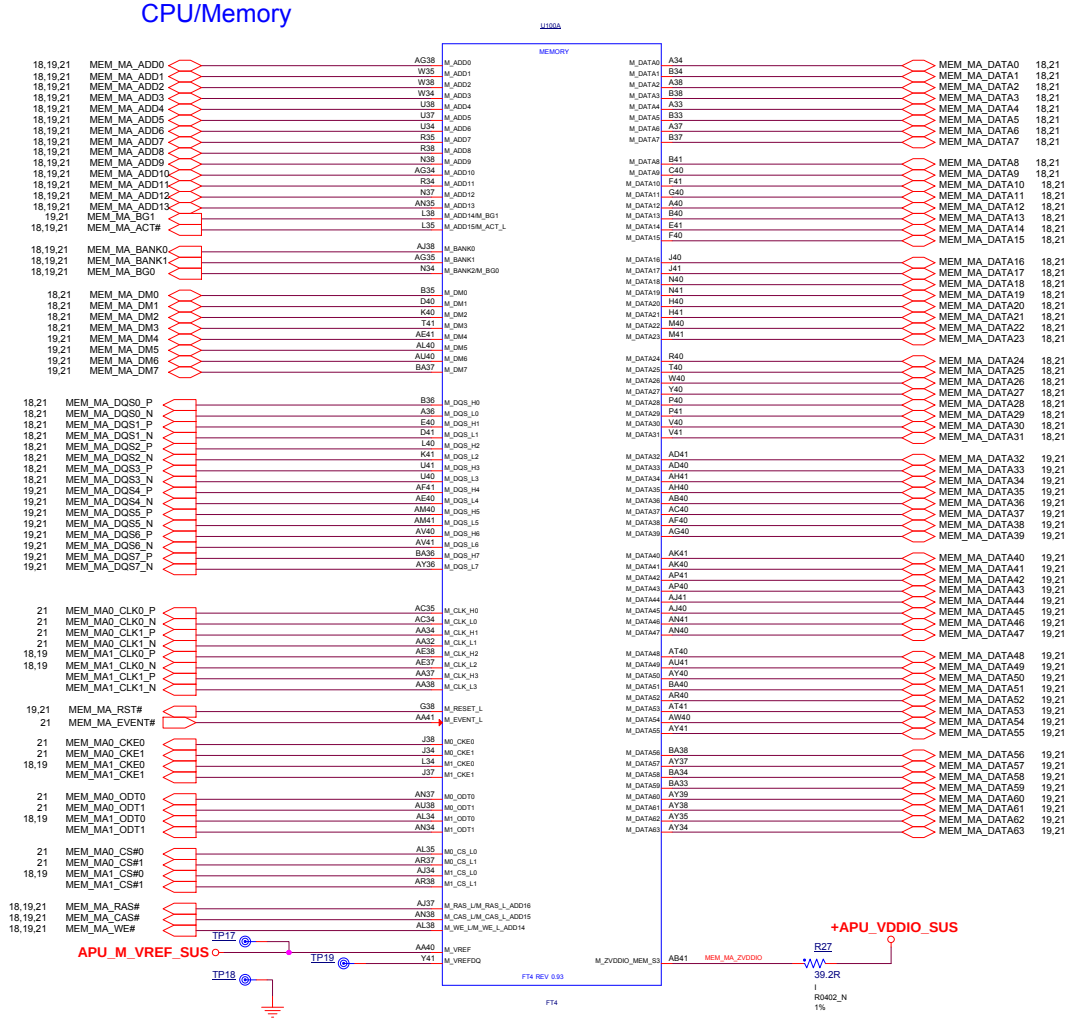
CPU/PCIE



3nod三诺	Project:	330S-14&15	
	Engineer:	Ken	
Size: Custom	Title:	03--FT4 PCIE I/F	Rev: V01
Date: Monday, January 08, 2018	Sheet	3 of 81	

CPU/Memory



18,19,21	MEM_MA_ADD0	AG38	M_ADD0	M_DATA0	A34	MEM_MA_DATA0	18,21
18,19,21	MEM_MA_ADD1	W35	M_ADD1	M_DATA1	B34	MEM_MA_DATA1	18,21
18,19,21	MEM_MA_ADD2	W38	M_ADD2	M_DATA2	A38	MEM_MA_DATA2	18,21
18,19,21	MEM_MA_ADD3	W34	M_ADD3	M_DATA3	B38	MEM_MA_DATA3	18,21
18,19,21	MEM_MA_ADD4	U38	M_ADD4	M_DATA4	A33	MEM_MA_DATA4	18,21
18,19,21	MEM_MA_ADD5	U37	M_ADD5	M_DATA5	B33	MEM_MA_DATA5	18,21
18,19,21	MEM_MA_ADD6	U34	M_ADD6	M_DATA6	A37	MEM_MA_DATA6	18,21
18,19,21	MEM_MA_ADD7	R35	M_ADD7	M_DATA7	B37	MEM_MA_DATA7	18,21
18,19,21	MEM_MA_ADD8	R38	M_ADD8				
18,19,21	MEM_MA_ADD9	N38	M_ADD9	M_DATA8	B41	MEM_MA_DATA8	18,21
18,19,21	MEM_MA_ADD10	AG34	M_ADD10	M_DATA9	C40	MEM_MA_DATA9	18,21
18,19,21	MEM_MA_ADD11	R34	M_ADD11	M_DATA10	F41	MEM_MA_DATA10	18,21
18,19,21	MEM_MA_ADD12	N37	M_ADD12	M_DATA11	G40	MEM_MA_DATA11	18,21
18,19,21	MEM_MA_ADD13	AN35	M_ADD13	M_DATA12	A40	MEM_MA_DATA12	18,21
19,21	MEM_MA_BG1	L38	M_ADD14/M_BG1	M_DATA13	B40	MEM_MA_DATA13	18,21
18,19,21	MEM_MA_ACT#	L35	M_ADD15/M_ACT_L	M_DATA14	E41	MEM_MA_DATA14	18,21
				M_DATA15	F40	MEM_MA_DATA15	18,21
18,19,21	MEM_MA_BANK0	AJ38	M_BANK0				
18,19,21	MEM_MA_BANK1	AG35	M_BANK1	M_DATA16	J40	MEM_MA_DATA16	18,21
18,19,21	MEM_MA_BG0	N34	M_BANK2/M_BG0	M_DATA17	J41	MEM_MA_DATA17	18,21
				M_DATA18	N40	MEM_MA_DATA18	18,21
18,21	MEM_MA_DM0	B35	M_DM0	M_DATA19	N41	MEM_MA_DATA19	18,21
18,21	MEM_MA_DM1	D40	M_DM1	M_DATA20	H40	MEM_MA_DATA20	18,21
18,21	MEM_MA_DM2	K40	M_DM2	M_DATA21	H41	MEM_MA_DATA21	18,21
18,21	MEM_MA_DM3	T41	M_DM3	M_DATA22	M40	MEM_MA_DATA22	18,21
19,21	MEM_MA_DM4	AE41	M_DM4	M_DATA23	M41	MEM_MA_DATA23	18,21
19,21	MEM_MA_DM5	AL40	M_DM5				
19,21	MEM_MA_DM6	AU40	M_DM6	M_DATA24	R40	MEM_MA_DATA24	18,21
19,21	MEM_MA_DM7	BA37	M_DM7	M_DATA25	T40	MEM_MA_DATA25	18,21
				M_DATA26	W40	MEM_MA_DATA26	18,21
18,21	MEM_MA_DQS0_P	B36	M_DQS_H0	M_DATA27	Y40	MEM_MA_DATA27	18,21
18,21	MEM_MA_DQS0_N	A36	M_DQS_L0	M_DATA28	P40	MEM_MA_DATA28	18,21
18,21	MEM_MA_DQS1_P	E40	M_DQS_H1	M_DATA29	P41	MEM_MA_DATA29	18,21
18,21	MEM_MA_DQS1_N	D41	M_DQS_L1	M_DATA30	V40	MEM_MA_DATA30	18,21
18,21	MEM_MA_DQS2_P	L40	M_DQS_H2	M_DATA31	V41	MEM_MA_DATA31	18,21
18,21	MEM_MA_DQS2_N	K41	M_DQS_L2				
18,21	MEM_MA_DQS3_P	U41	M_DQS_H3	M_DATA32	AD41	MEM_MA_DATA32	19,21
18,21	MEM_MA_DQS3_N	U40	M_DQS_L3	M_DATA33	AD40	MEM_MA_DATA33	19,21
19,21	MEM_MA_DQS4_P	AF41	M_DQS_H4	M_DATA34	AH41	MEM_MA_DATA34	19,21
19,21	MEM_MA_DQS4_N	AE40	M_DQS_L4	M_DATA35	AH40	MEM_MA_DATA35	19,21
19,21	MEM_MA_DQS5_P	AM40	M_DQS_H5	M_DATA36	AB40	MEM_MA_DATA36	19,21
19,21	MEM_MA_DQS5_N	AM41	M_DQS_L5	M_DATA37	AC40	MEM_MA_DATA37	19,21
19,21	MEM_MA_DQS6_P	AV40	M_DQS_H6	M_DATA38	AF40	MEM_MA_DATA38	19,21
19,21	MEM_MA_DQS6_N	AV41	M_DQS_L6	M_DATA39	AG40	MEM_MA_DATA39	19,21
19,21	MEM_MA_DQS7_P	BA36	M_DQS_H7				
19,21	MEM_MA_DQS7_N	AY36	M_DQS_L7	M_DATA40	AK41	MEM_MA_DATA40	19,21
				M_DATA41	AK40	MEM_MA_DATA41	19,21
21	MEM_MA0_CLK0_P	AC35	M_CLK_H0	M_DATA42	AP41	MEM_MA_DATA42	19,21
21	MEM_MA0_CLK0_N	AC34	M_CLK_L0	M_DATA43	AP40	MEM_MA_DATA43	19,21
21	MEM_MA0_CLK1_P	AA34	M_CLK_H1	M_DATA44	AJ41	MEM_MA_DATA44	19,21
21	MEM_MA0_CLK1_N	AA32	M_CLK_L1	M_DATA45	AJ40	MEM_MA_DATA45	19,21
18,19	MEM_MA1_CLK0_P	AE38	M_CLK_H2	M_DATA46	AN41	MEM_MA_DATA46	19,21
18,19	MEM_MA1_CLK0_N	AE37	M_CLK_L2	M_DATA47	AN40	MEM_MA_DATA47	19,21
	MEM_MA1_CLK1_P	AA37	M_CLK_H3				
	MEM_MA1_CLK1_N	AA38	M_CLK_L3	M_DATA48	AT40	MEM_MA_DATA48	19,21
				M_DATA49	AU41	MEM_MA_DATA49	19,21
19,21	MEM_MA_RST#	G38	M_RESET_L	M_DATA50	AY40	MEM_MA_DATA50	19,21
21	MEM_MA_EVENT#	AA41	M_EVENT_L	M_DATA51	BA40	MEM_MA_DATA51	19,21
				M_DATA52	AR40	MEM_MA_DATA52	19,21
21	MEM_MA0_CKE0	J38	M0_CKE0	M_DATA53	AT41	MEM_MA_DATA53	19,21
21	MEM_MA0_CKE1	J34	M0_CKE1	M_DATA54	AW40	MEM_MA_DATA54	19,21
18,19	MEM_MA1_CKE0	L34	M1_CKE0	M_DATA55	AY41	MEM_MA_DATA55	19,21
	MEM_MA1_CKE1	J37	M1_CKE1				
				M_DATA56	BA38	MEM_MA_DATA56	19,21
21	MEM_MA0_ODT0	AN37	M0_ODT0	M_DATA57	AY37	MEM_MA_DATA57	19,21
21	MEM_MA0_ODT1	AU38	M0_ODT1	M_DATA58	BA34	MEM_MA_DATA58	19,21
18,19	MEM_MA1_ODT0	AL34	M1_ODT0	M_DATA59	BA33	MEM_MA_DATA59	19,21
	MEM_MA1_ODT1	AN34	M1_ODT1	M_DATA60	AY39	MEM_MA_DATA60	19,21
				M_DATA61	AY38	MEM_MA_DATA61	19,21
21	MEM_MA0_CS#0	AL35	M0_CS_L0	M_DATA62	AY35	MEM_MA_DATA62	19,21
21	MEM_MA0_CS#1	AR37	M0_CS_L1	M_DATA63	AY34	MEM_MA_DATA63	19,21
18,19	MEM_MA1_CS#0	AJ34	M1_CS_L0				
	MEM_MA1_CS#1	AR38	M1_CS_L1				
18,19,21	MEM_MA_RAS#	AJ37	M_RAS_L/M_RAS_L_ADD16				
18,19,21	MEM_MA_CAS#	AN36	M_CAS_L/M_CAS_L_ADD15				
18,19,21	MEM_MA_WE#	AL38	M_WE_L/M_WE_L_ADD14				
		AA40	M_VREF				
		Y41	M_VREFDQ				

3nod三诺	Project:	330S-14&15	
	Engineer:	Ken	
Size: Custom	Title:	04--FT4 DDR4 I/F	Rev: V01
Date: Monday, January 08, 2018	Sheet 4 of 81		

CPU/Display&MSIC

+1.8V_RUN

R40 0R NI R0402_N 5%

R28 1K NI R0402_N 1% APU_SVT_R

R223 1K R0402_N 1% CPU_SVC R226 220R R0402_N 1% NI

R224 1K R0402_N 1% CPU_SVD R225 220R R0402_N 1% NI

SVC and SVD are the clock and serial data of the serial VID interface.

U100C

DISPLAY/SVI2/JTAG/TEST

64 CPU_SVT R52 0R R0402_N 5% APU_SVT_R H27 SVT

64 CPU_SVC CPU_SVC R30 22R R0402_N 5% APU_SVC_R E27 SVC

64 CPU_SVD CPU_SVD R32 22R R0402_N 5% APU_SVD_R D27 SVD

Thermal monitor device or circuit

C17 27pF 50V 5% NPO C0402_N NI

APU_SIC B30 SIC

APU_SID B29 SID

APU_ALERT#_D A30 ALERT_L

CPUVR_HOT A31 PROCHOT_L

+1.8V_RUN

PWROK is an APU output signal
Connect to VDDCR_CPU and VDDCR_NB regulator
PWROK input/VDD_18.

R63 300R 1% R0402_N I

R43 300R 1% R0402_N I

R41 0R R0402_N 5% NI

6,11,29,50,64 CPU_PWROK

6,11 APU_RST#

CPU_PWROK_R G25 PWROK

APU_RST# D29 RESET_L

RESET_L is an active-low bidirectiona signal that resets the APU when asserted VDD_18

R74 220R 1% R0402_N NI

C18 27pF 50V 5% NPO C0402_N NI

Debug Signals

11 APU_TDI B25 TDI

11 APU_TDO A27 TDO

11 APU_TCK B27 TCK

11 APU_TMS B26 TMS

11 APU_TRST# A29 TRST_L

11 APU_DBRDY A26 DBRDY

11 APU_DBREQ# A25 DBREQ_L

+1.8V_RUN

EC-SIV-13

R245 4.7k 1% R0402_N I

Q1001 2N7002KW 115mA 60V sot_323_dgs

50 APU_RES#_EC

APU_RST#

R218 0R NI R0402_N 5%

+1.8V_RUN

R38 1K R0402_N 1% APU_ALERT#_D

R39 1K R0402_N 1% CPUVR_HOT

R34 1K R0402_N 1% APU_SIC

R36 1K R0402_N 1% APU_SID

Thermal sensor

29 THER_SENSOR_CLK R250 0R NI R0402_N 5% APU_SIC

29 THER_SENSOR_DATA R251 0R NI R0402_N 5% APU_SID

29,50 CPU_THERMAL_ALERT# R252 0R NI R0402_N 5% APU_ALERT#_D

6,50,58,64 PROCHOT_N R172 0R NI R0402_N 5% CPUVR_HOT

The processor asserts PROCHOT_L when the hardware thermal control (HTC) is active.
External hardware can assert PROCHOT_L to reduce APU power consumption by forcing HTC activation

D9 RSVD_1

D11 RSVD_2

D13 RSVD_3

E4 RSVD_4

E31 RSVD_5

H11 RSVD_6

H13 RSVD_7

L11 RSVD_8

AE34 RSVD_9

AM15 RSVD_10

AM17 RSVD_11

AM19 RSVD_12

AN8 RSVD_13

AP13 RSVD_14

AP15 RSVD_15

AP17 RSVD_16

AR13 RSVD_17

AR15 RSVD_18

AR17 RSVD_19

AU4 RSVD_20

AU13 RSVD_21

AU15 RSVD_22

AU17 RSVD_23

AV7 RSVD_24

AV9 RSVD_25

AV11 RSVD_26

AV13 RSVD_27

AV15 RSVD_28

AV17 RSVD_29

AY3 RSVD_30

AY7 RSVD_31

FT4 REV 0.93

FT4

DP_VARY_BL, DP_BLON, DP_DIGON signals are VDD_18 level at the APU.

DP_BLON B23 APU_BLEN_R R29 0R R0402_N 5% APU_BLEN 36 LCD Backlight Inverter On

DP_DIGON B24 APU_DIGON_R R31 0R R0402_N 5% APU_DIGON 36 Control to Power LCD Logic Circuits

DP_VARY_BL A24 APU_BLPWM_R R33 0R R0402_N 5% APU_BLPWM 36 LCD Backlight Intensity

DP_AUX_ZVSS D21 DP_AUX_ZVSS R35 150R R0402_N 5%

DP_ZVSS B18 DP_ZVSS R37 2K R0402_N 1%

Sets the drive strength for the MainLink signals

DP0_AUXP G15 EDP_AUX_SOC_DP 36

DP0_AUXN H15 EDP_AUX_SOC_DN 36 For EDP

DP0_HPD D15 EDP_HPD 36 APU +3.3-V input level

DP1_AUXP G17 DDI1_DDC_SCK 35

DP1_AUXN H17 DDI1_DDC_SDA 35 For HDMI

DP1_HPD D17 DDI1_HPD 35 APU +3.3-V input level

DP2_AUXP G19

DP2_AUXN H19

DP2_HPD D19

Unused signals are left unconnected.

DP0_TXP0 A9 EDP_TX0_SOC_DP 36

DP0_TXN0 B9 EDP_TX0_SOC_DN 36

DP0_TXP1 A10 EDP_TX1_SOC_DP 36 For EDP

DP0_TXN1 B10 EDP_TX1_SOC_DN 36

DP0_TXP2 A11

DP0_TXN2 B11

DP0_TXP3 A12

DP0_TXN3 B12

Unused signals are left unconnected.

DP1_TXP0 A14 DDI1_TX0_DP 35

DP1_TXN0 B14 DDI1_TX0_DN 35

DP1_TXP1 A15 DDI1_TX1_DP 35

DP1_TXN1 B15 DDI1_TX1_DN 35

DP1_TXP2 A16 DDI1_TX2_DP 35 For HDMI

DP1_TXN2 B16 DDI1_TX2_DN 35

DP1_TXP3 A17 DDI1_TX3_DP 35

DP1_TXN3 B17 DDI1_TX3_DN 35

DP2_TXP0 A19

DP2_TXN0 B19

DP2_TXP1 A20

DP2_TXN1 B20

DP2_TXP2 A21

DP2_TXN2 B21

DP2_TXP3 A22

DP2_TXN3 B22

Unused signals are left unconnected.

TEST4 H29 APU_TEST4 TP45

TEST5 G29 APU_TEST5 TP46

TEST6 H25 APU_TEST6 TP47

TEST9 R32 APU_TEST9 TP48

TEST10 N32 APU_TEST10 TP49

TEST14 G21 APU_TEST14 R56 1K NI R0402_N 1%

TEST15 H21 APU_TEST15 TP51

TEST16 D23 APU_TEST16 R57 1K NI R0402_N 1%

TEST17 E23 APU_TEST17 R58 1K R0402_N 1%

TEST18 A28 APU_TEST18 R59 1K R0402_N 1%

TEST19 B28 APU_TEST19 R60 1K R0402_N 1%

TEST28_H N8 APU_TEST28_H TP56

TEST28_L N10 APU_TEST28_L TP57

TEST31 H31 APU_TEST31 TP58

DP_STEREOSYNC/TEST36 D25 DP_STEREOSYNC

TEST41 B31 TMON_CAL TP60

APU_TEST19 R170 0R R0402_N 5% APU_PLLTEST0 11

APU_TEST18 R171 0R R0402_N 5% APU_PLLTEST1 11

VDDCR_CPU_SENSE D31 FB_CPU_VDDCR_SOC 64 VDDCR_CPU regulator

VDDCR_NB_SENSE E33 FB_NB_VDDCR_SOC 64 VDDCR_NB regulator

VDDIO_MEM_S3_SENSE D35 APU_VDDIO_MEM_S3_FB 62

VDDP_SENSE AM21 APU_VDDP_ALW_FB 60 VDDP regulator

VSS_SENSE_A D33 FB_CPU_VSSC_SOC 64 VSS sense pin for VDDCR_CPU and VDDCR_NB regulators

VSS_SENSE_B AM23 APU_VDDP_VSSC_FB 60 VSS sense pin for VDDP regulator

EC-SIV-26

+1.8V_RUN

R310 1K 1% R0402_N I

DP_STEREOSYNC

R311 1K 1% R0402_N NI

3nod三诺	Project: 330S-14&15	
	Engineer: Ken	
Size: Custom	Title: 05--FT4 DISPLAY/MISC	Rev: V01
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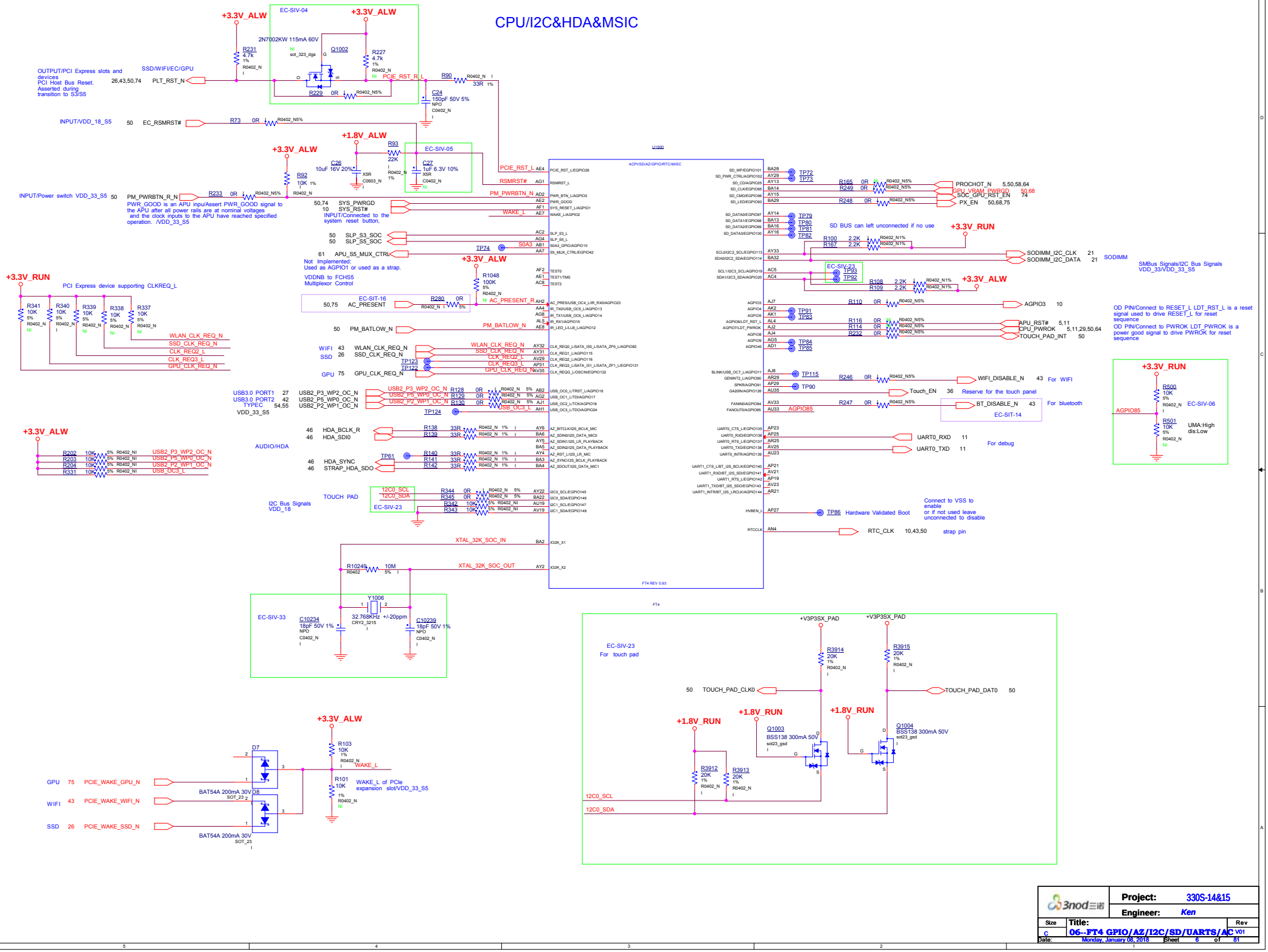
CPU/I2C&HDA&MSIC



Project:	330S-14&15	
Engineer:	Ken	
Size: C	Title: 06--FT4 GPIO/AZ/I2C/SD/UARTS/AC	Rev: V01
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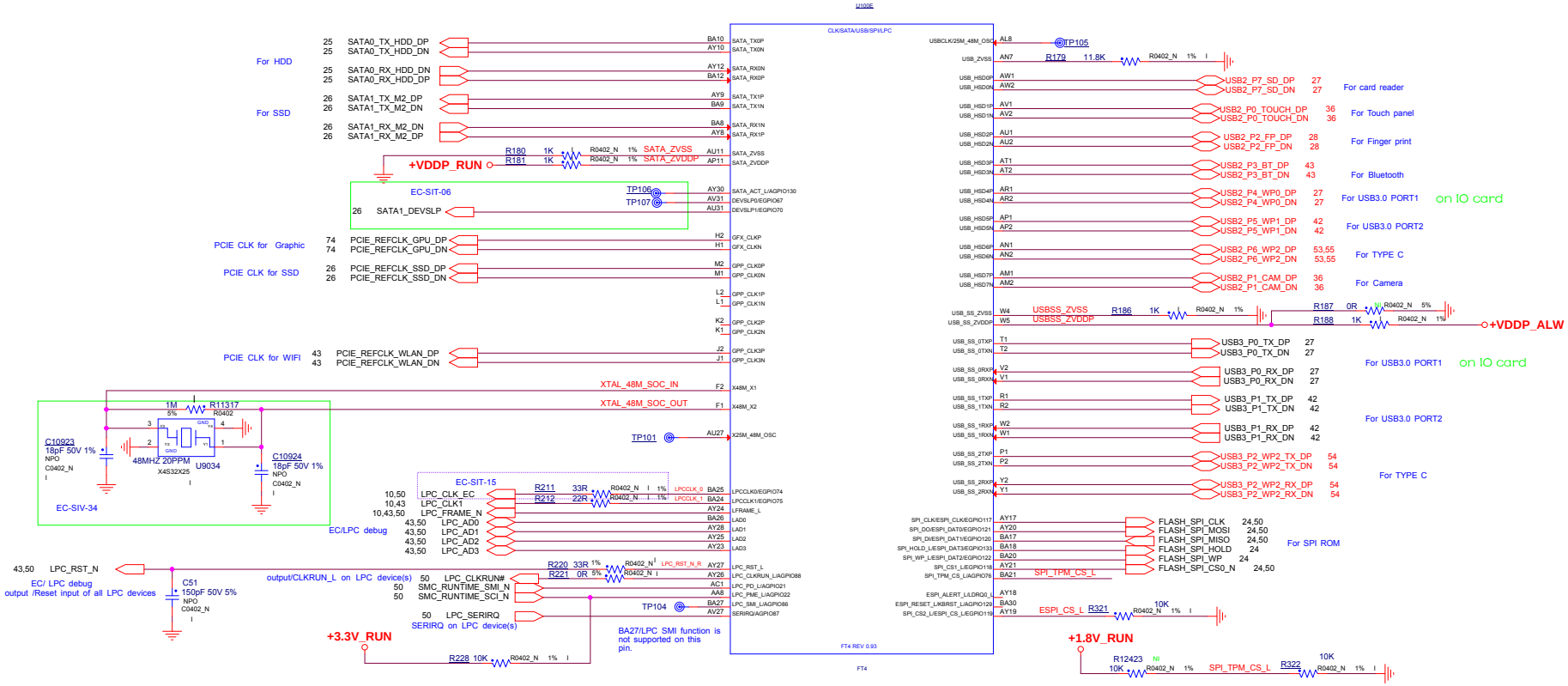
CPU/SATA&USB&LPC&SPI



3nod三诺	Project:	330S-14&15
	Engineer:	Ken
Size: Custom	Title:	07-- FT4 SATA/USB/LPC/SPI/eSPI
	Rev:	V01
Date: Tuesday, February 06, 2018	Sheet 7 of 81	

CPU/Power

Please note the capacitor placement for the cpu power

All BU(on bottom side under SOC)

BO(Bottom side outside SOC)

+APU_VDDIO_SUS

1.2V@1.9A

VDDIO_MEM_S3 is the main power supply for the DIMMs and also an auxiliary supply for the DDR section of the processor.

U1100E

POWER

+APU_VDDNB_RUN

0.75~1.2V@29A

VDDCR_NB powers the Northbridge and the GPU core

+APU_VDDCORE_RUN

0.75~1.5V@32A

VDDCR_CPU is the voltage rail for the CPU core.

+VDDCR_FCH_ALW

0.775V@0.4A

VDDCR_FCH_S5 is the supply voltage for the FCH core logic.

+VDDP_ALW

1.05V@0.8A

VDDP_S5 is the voltage rail for the USB physical layer.

+VDDP_RUN

0.95v@7A

VDDP is the supply voltage for PCIe GPP, PCIe GFX, DisplayPort, and SATA PHY logic.

+1.8V_RUN

1.8V@1.5A

+1.8V_ALW

1.8V@0.5A

+3.3V_RUN_APU

3.3V@0.2A

+3.3V_ALW

3.3V@0.2A

+1.8V_ALW

+VDDIO_AZ

1.5@0.2A

+RTCVCC

+ 3.3 V to + 1.5 V LDO through a 1 kΩ series resistor

R254 0R R0402_N1%

If 'Wake-on-Ring' is supported, connect to a S5 rail, else connect to a S0 rail.

C128 22UF 6.3V 20% X5R C0603_N BO

C129 1uF 6.3V 10% X5R C0201 BU

C131 0.22uF 6.3V 10% X5R C0402_N BU

FT4 REV 0.93

FT4

EC-SVT-05

+3.3V_RUN

R255 SHORT_0805

R255 FOR DEBUG ONLY

EC-SIV-03

+APU_VDDCORE_RUN

C52 22UF 6.3V 20% X5R C0603_N

C53 22UF 6.3V 20% X5R C0603_N

C54 22UF 6.3V 20% X5R C0603_N

C55 22UF 6.3V 20% X5R C0603_N

C57 22UF 6.3V 20% X5R C0603_N

C61 22UF 6.3V 20% X5R C0603_N

C63 22UF 6.3V 20% X5R C0603_N

C64 1uF 6.3V 10% X5R C0201

C68 180pF 50V 5% NPO C0402_N

All BU(on bottom side under SOC)

+APU_VDDNB_RUN

C69 22UF 6.3V 20% X5R C0603_N

C70 22UF 6.3V 20% X5R C0603_N

C71 22UF 6.3V 20% X5R C0603_N

C72 22UF 6.3V 20% X5R C0603_N

C74 22UF 6.3V 20% X5R C0603_N

C76 22UF 6.3V 20% X5R C0603_N

C77 22UF 6.3V 20% X5R C0603_N

C78 22UF 6.3V 20% X5R C0603_N

C79 22UF 6.3V 20% X5R C0603_N

C80 22UF 6.3V 20% X5R C0603_N

C81 22UF 6.3V 20% X5R C0603_N

C84 180pF 50V 5% NPO C0402_N

All BU(on bottom side under SOC)

+APU_VDDIO_SUS

C88 22UF 6.3V 20% X5R C0603_N

C89 22UF 6.3V 20% X5R C0603_N

C90 22UF 6.3V 20% X5R C0603_N

C91 22UF 6.3V 20% X5R C0603_N

C92 22UF 6.3V 20% X5R C0603_N

C93 22UF 6.3V 20% X5R C0603_N

C96 22UF 6.3V 20% X5R C0603_N

C97 22UF 6.3V 20% X5R C0603_N

C99 22UF 6.3V 20% X5R C0603_N

C100 1uF 6.3V 10% X5R C0201

C101 1uF 6.3V 10% X5R C0201

C104 180pF 50V 5% NPO C0402_N

All BU(on bottom side under SOC)

+VDDP_RUN

C105 22UF 6.3V 20% X5R C0603_N

C106 22UF 6.3V 20% X5R C0603_N

C107 1uF 6.3V 10% X5R C0201

C108 1uF 6.3V 10% X5R C0201

C109 1uF 6.3V 10% X5R C0201

C111 1uF 6.3V 10% X5R C0201

C112 1uF 6.3V 10% X5R C0201

C113 1uF 6.3V 10% X5R C0201

C114 1uF 6.3V 10% X5R C0201

C115 1uF 6.3V 10% X5R C0201

C110 180pF 50V 5% NPO C0402_N

BO(Bottom side outside SOC)

All BU(on bottom side under SOC)

+VDDCR_FCH_ALW

C116 22UF 6.3V 20% X5R C0603_N BO

C117 1uF 6.3V 10% X5R C0201 BU

C118 1uF 6.3V 10% X5R C0201

C119 1uF 6.3V 10% X5R C0201

C120 1uF 6.3V 10% X5R C0201

+VDDP_ALW

C124 22UF 6.3V 20% X5R C0603_N BO

C126 1uF 6.3V 10% X5R C0201

C125 1uF 6.3V 10% X5R C0201 BU

C127 1uF 6.3V 10% X5R C0201

+1.8V_ALW

C132 22UF 6.3V 20% X5R C0603_N BO

C134 1uF 6.3V 10% X5R C0201

C133 1uF 6.3V 10% X5R C0201 BU

+1.8V_RUN

C121 22UF 6.3V 20% X5R C0603_N BO

C122 1uF 6.3V 10% X5R C0201 BO

C123 1uF 6.3V 10% X5R C0201 BU

+3.3V_ALW

C135 22UF 6.3V 20% X5R C0603_N BO

C136 1uF 6.3V 10% X5R C0201

C137 1uF 6.3V 10% X5R C0201 BU

+3.3V_RUN_APU

C138 22UF 6.3V 20% X5R C0603_N BO

C139 1uF 6.3V 10% X5R C0201

C140 1uF 6.3V 10% X5R C0201 BU

DECOUPLING BETWEEN PROCESSOR AND DIMMs

ACROSS VDDIO AND VSS SPLIT

+APU_VDDIO_SUS

C144 0.22uF 16V 10% X7R C0402_N

C145 0.22uF 16V 10% X7R C0402_N

C146 0.22uF 16V 10% X7R C0402_N

C147 0.22uF 16V 10% X7R C0402_N

C148 180pF 50V 5% NPO C0402_N

C149 180pF 50V 5% NPO C0402_N

4x0.22UF (0402)+2x180PF(0402)

VDDBT_RTC_G

+RTC_BATT

W>=20mils

EC-SIT-12

U9025

VIN VOUT EN PAD GND

WL2815D15-4/TR dfn4_1x1x0p4_0p65_ths0p6

R10910 R0402_N 1K 5%

R10912 R0402_N 10K 5%

C12018 1uF 10V 10% X5R C0402

C12000 1uF 10V 10% X5R C0402

Imax=0.5uA

W>=15mils

+RTCVCC

R12433 10R 5% R0603

8,50 EC_CLEARCMOS

R12431 R0402_N 0R 5% NI

Q1005 2N7002 250mA 60V sot_23_dgs NI

8,50 EC_CLEARCMOS

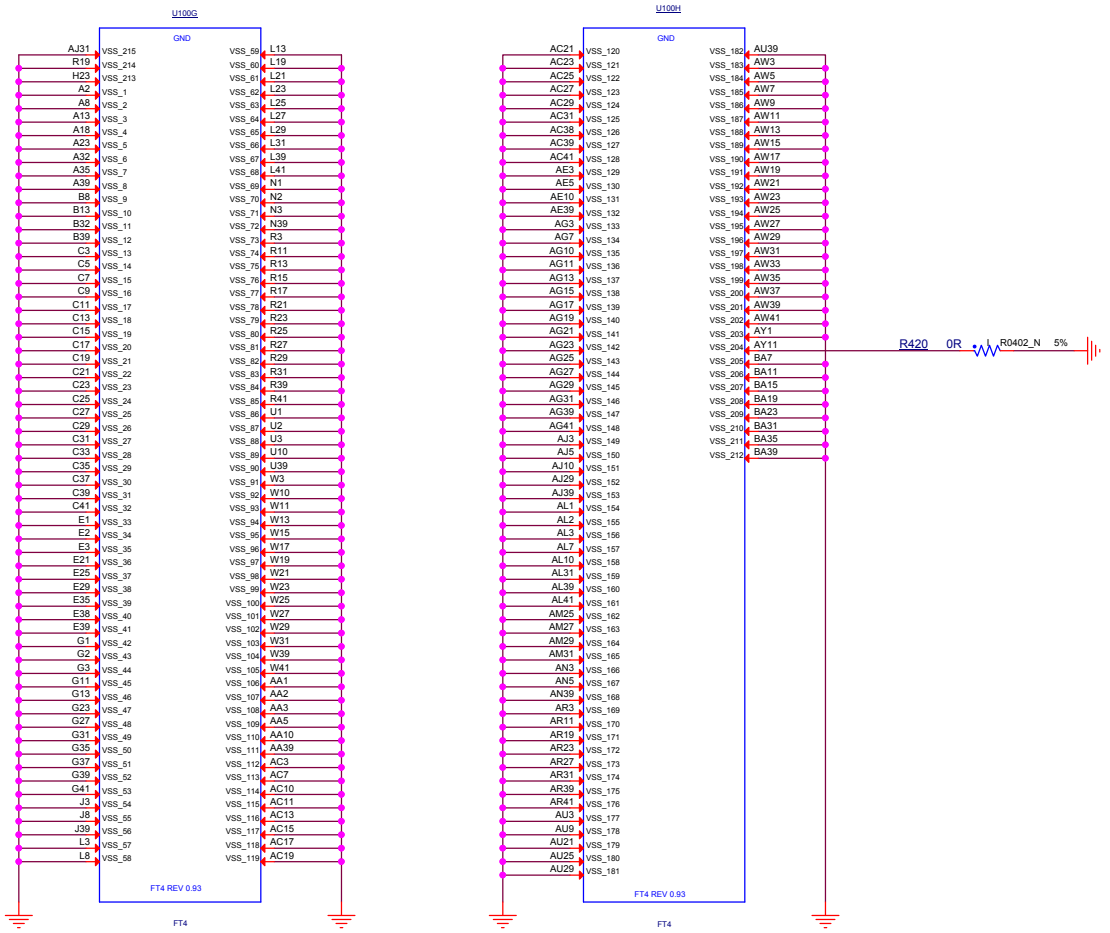
R12432 R0402_N 0R 5%

Q8967 2N7002 250mA 60V sot_23_dgs

EC-SIT-17

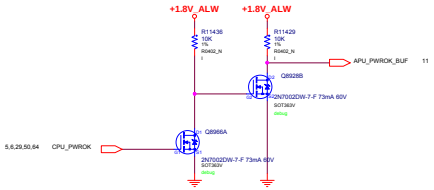
3nod三诺	Project:	330S-14&15
	Engineer:	Ken
Size: Custom	Title:	08--FT4 POWER
		Rev: V01
Date:	Friday, February 02, 2018	Sheet 8 of 81

CPU/GND

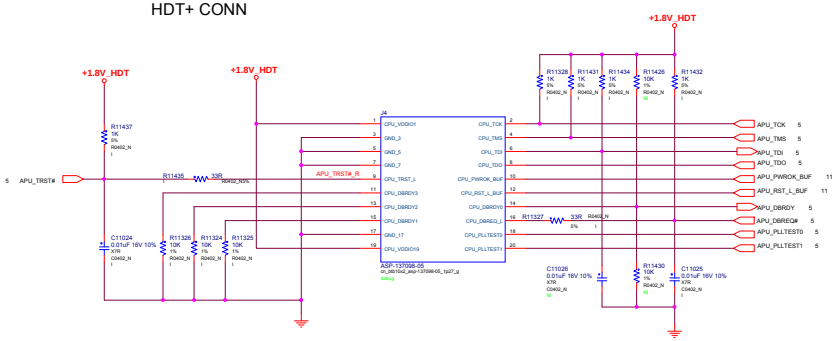


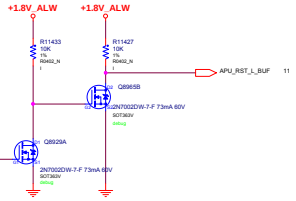
3nod三诺	Project: 330S-14&15	
	Engineer: Ken	
Size: Custom	Title: 09--FT4 GND	Rev: V01
Date: Monday, January 08, 2018	Sheet 9 of 81	

CPU/Debug

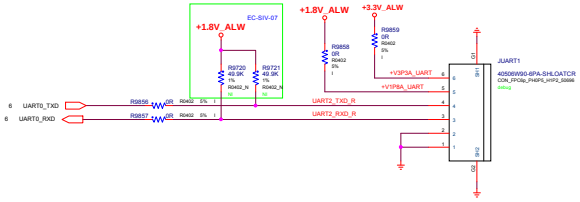


HDT+ CONN





UART Connector

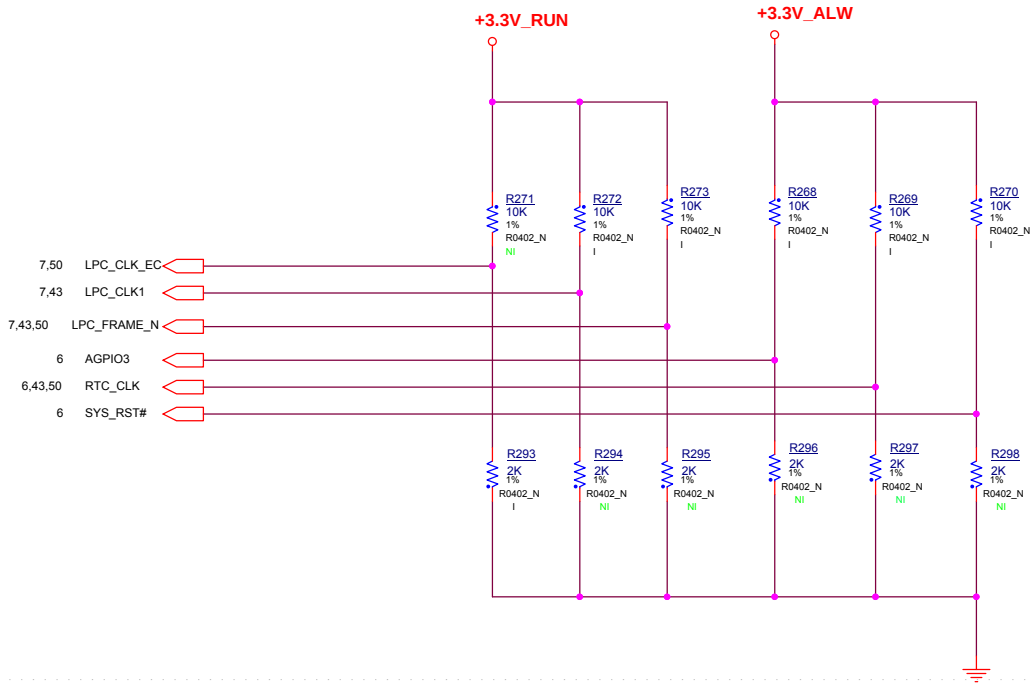


	Project:	330S-14&15
	Engineer:	Ken
Size: A	Title: RA	Rev: V01
Date: Monday, January 08, 2018	Sheet 11 of 81	

3nod三诺	Project: 330S-14&15	
	Engineer: Ken	
Size: Custom	Title: NA	Rev: V01
Date: Monday, January 08, 2018	Sheet 12 of 81	

3nod三诺	Project: 330S-14&15	
	Engineer: *Ken*	
Size: Custom	Title: NA	Rev: V01
Date: Monday, January 08, 2018	Sheet 13 of 81	

CPU/Straping



	LPC_CLK0	LPC_CLK1	LFRAME_L	AGPIO3 Int pull-up	RTC_CLK Int pull-up	SYS_RST# Int pull-up
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)	SPI ROM (DEFAULT)	Enhanced reset logic (for quicker S5 S5 resume) (DEFAULT)	Coin battery is on board. (DEFAULT)	normal reset mode (DEFAULT)
PULL LOW	BOOT FAIL TIMER DISABLED (DEFAULT)	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	LPC ROM	Default to traditional reset logic	Coin battery is not on board.	short reset mode

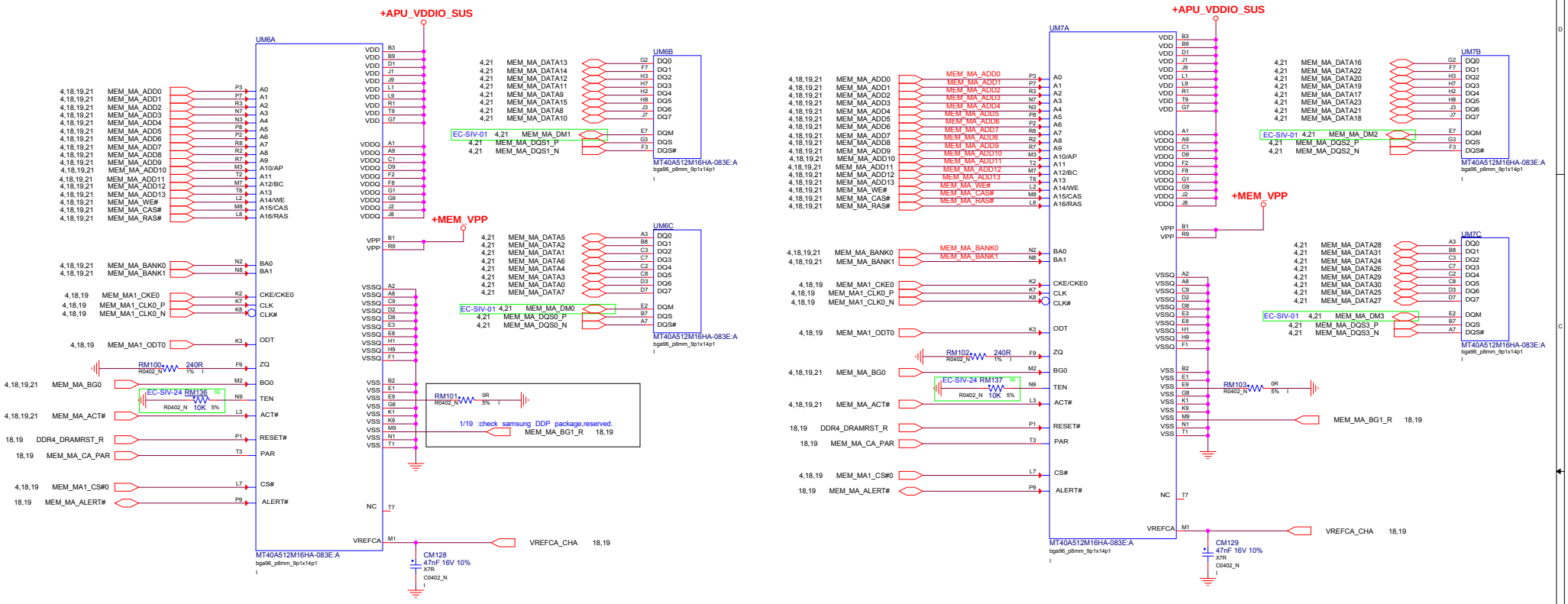
3nod三诺	Project:	330S-14&15
	Engineer:	Ken
Size: Custom	Title: NA	Rev: V01
Date: Monday, January 08, 2018	Sheet 14 of 81	

3nod三诺	Project:	330S-14&15	
	Engineer:	Ken	
Size	Title: NA		Rev
C			V01
Date:	Monday, January 08, 2018	Sheet 15 of 81	

3nod三诺	Project: 330S-14&15
	Engineer: *Ken*
Size: B	Title: NA
	Rev: V01
Date: Monday, January 08, 2018	Sheet 16 of 81

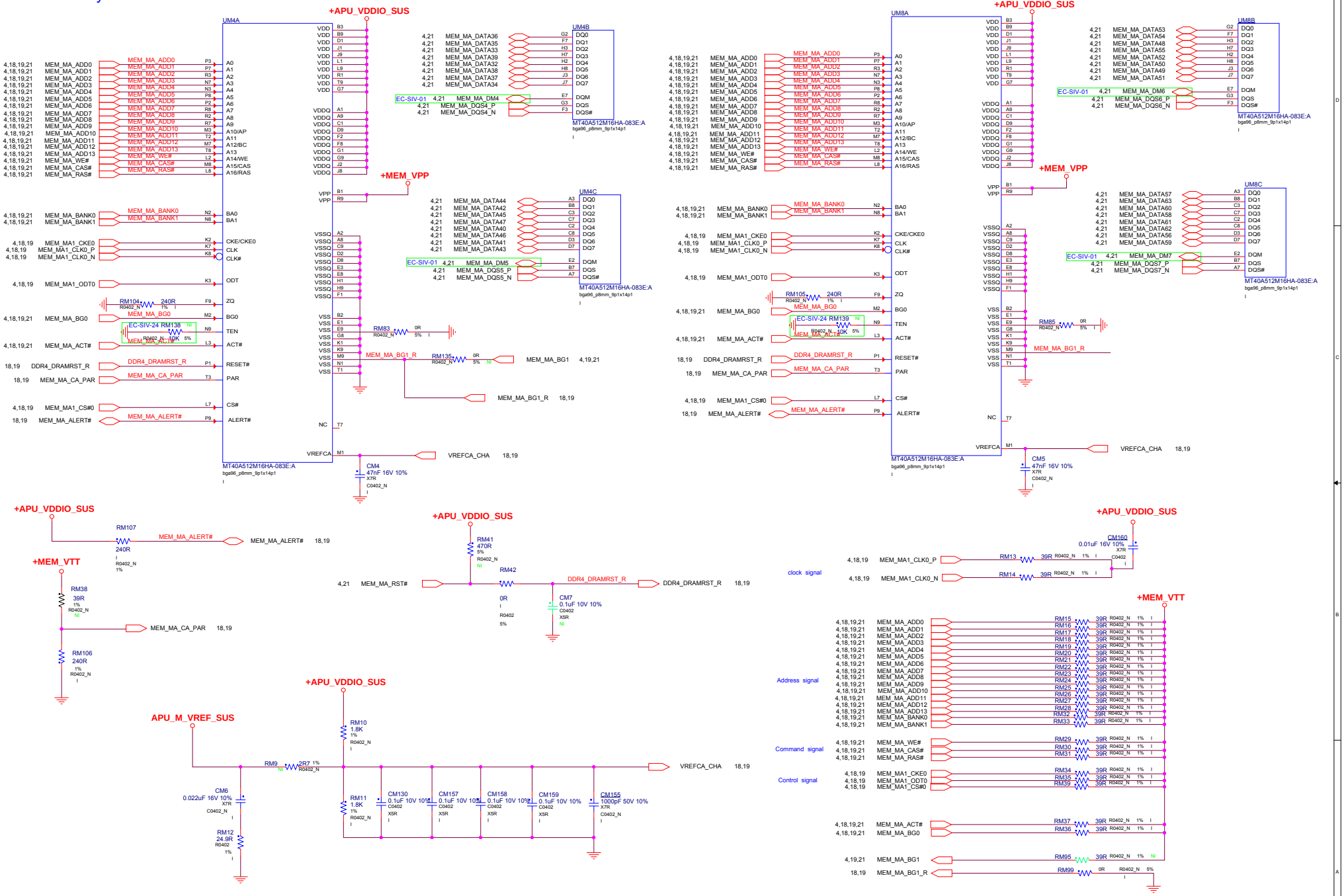
3nod三诺	Project:	330S-14&15
	Engineer:	Ken
Size: B	Title: NA	Rev: V01
Date: Monday, January 08, 2018	Sheet 17 of 81	

Memory down/DDR4*4



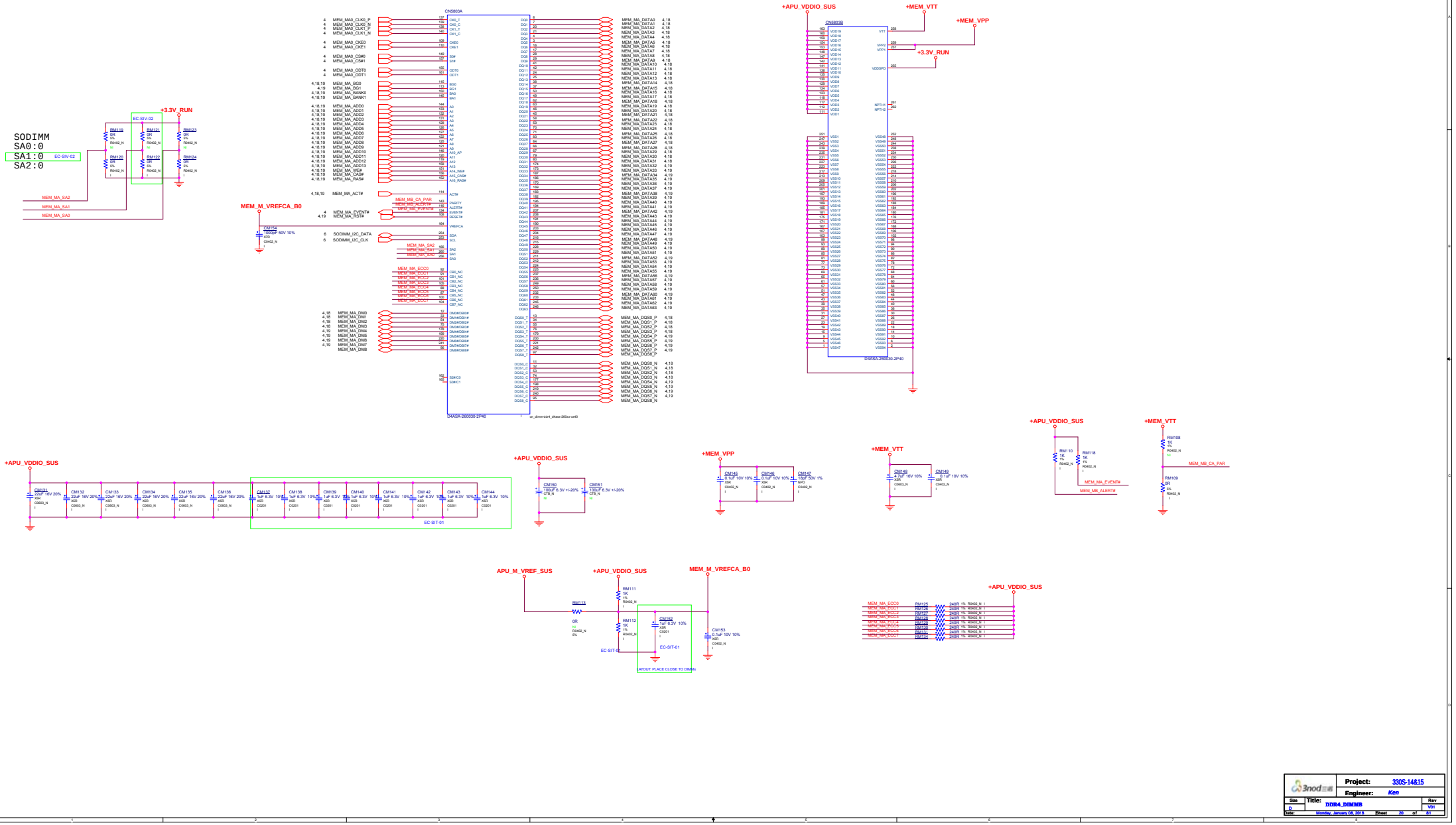
3nod三诺	Project: 330S-14&15	
	Engineer: Ken	
Size: C	Title: DDR4_CHA1	Rev: V01
Date: Monday, January 08, 2018	Sheet 18 of 81	

Memory down/DDR4*4



3nod三诺	Project:	330S-14&15
	Engineer:	Ken
Size: C	Title: DDR4_CHA2	Rev: V01
Date: Monday, January 08, 2018	Sheet 19 of 81	

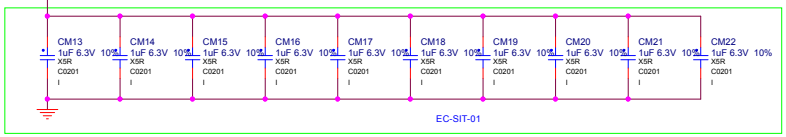
SODIMM



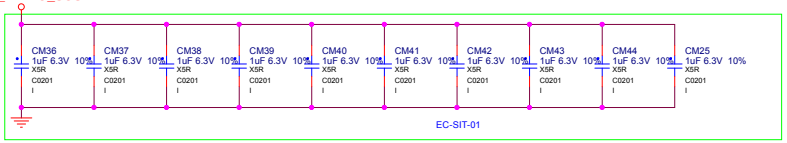
3nod三诺	Project:	330S-14&15
	Engineer:	Ken
Size: D	Title: DDR4_DIMMB	Rev: V01
Date: Monday, January 08, 2018	Sheet 29 of 51	

DDR4*4 /Decoupling capacitor

+APU_VDDIO_SUS

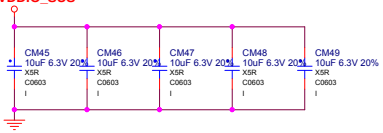


+APU_VDDIO_SUS



1uF:4 as near each x16 DRAM device as possible

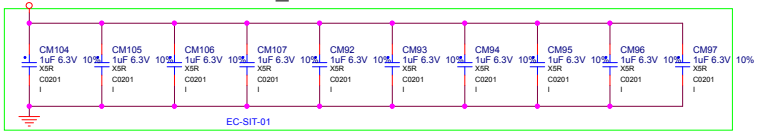
+APU_VDDIO_SUS



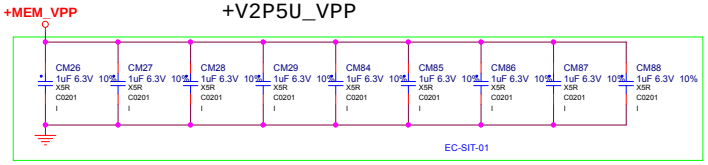
10uF:Distributed around the DRAM devices

1uF:2 as near each x20 DRAM device as possible

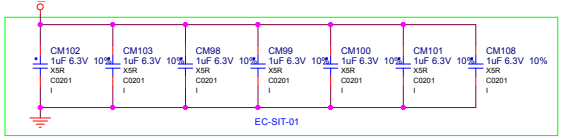
+MEM_VTT +V0.6S_VTT



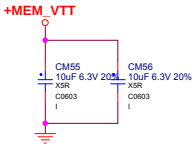
+MEM_VPP +V2P5U_VPP



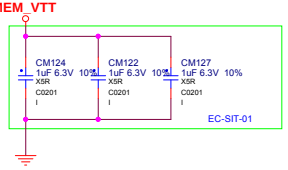
+MEM_VTT



+MEM_VTT

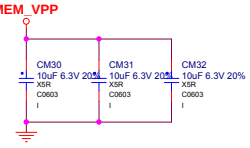


+MEM_VTT



1uF:2 as near each x16 DRAM device as possible

+MEM_VPP



10uF:Distributed around the DRAM devices

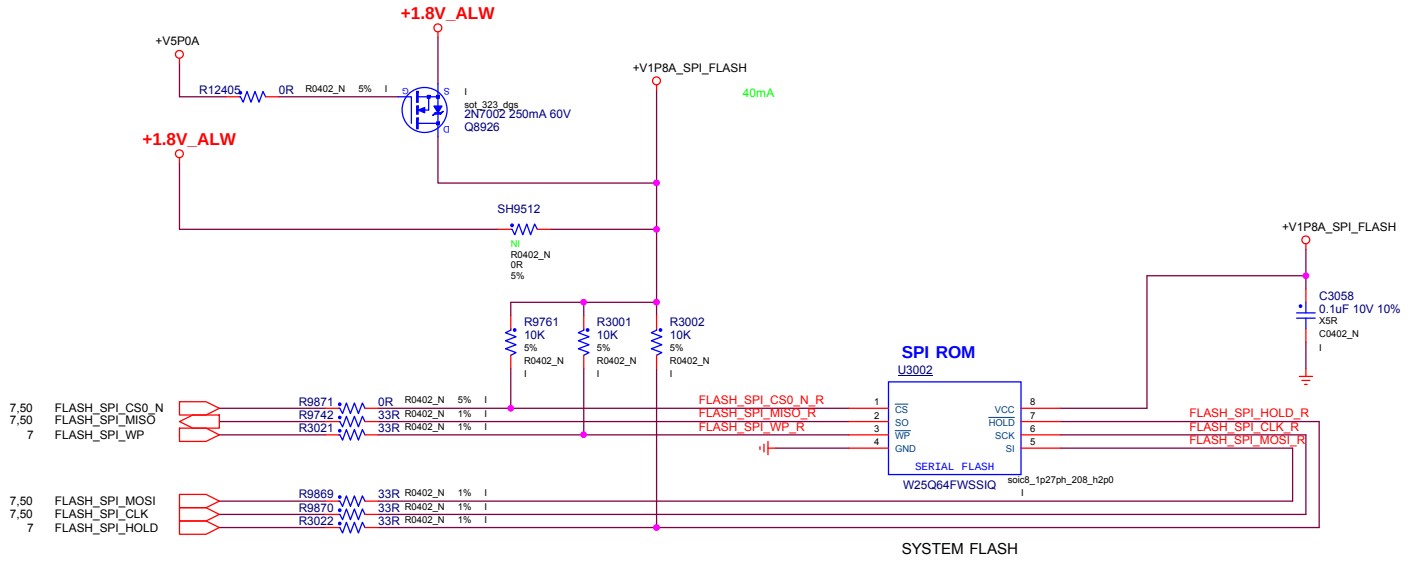
10uF:Distributed around the DRAM devices

3nod三诺	Project: 330S-14&15	
	Engineer: Ken	
Size: C	Title: DDR4 Decoupling	Rev: V01
Date: Monday, January 08, 2018	Sheet 21 of 81	

3nod三诺	Project: 330S-14&15	
	Engineer: *Ken*	
Size: Custom	Title: NA	Rev: V01
Date: Monday, January 08, 2018	Sheet 22 of 81	

3nod三诺	Project: 330S-14&15	
	Engineer: Ken	
Size: Custom	Title: RF / EMC Solution	Rev: V01
Date: Monday, January 08, 2018	Sheet 23 of 81	

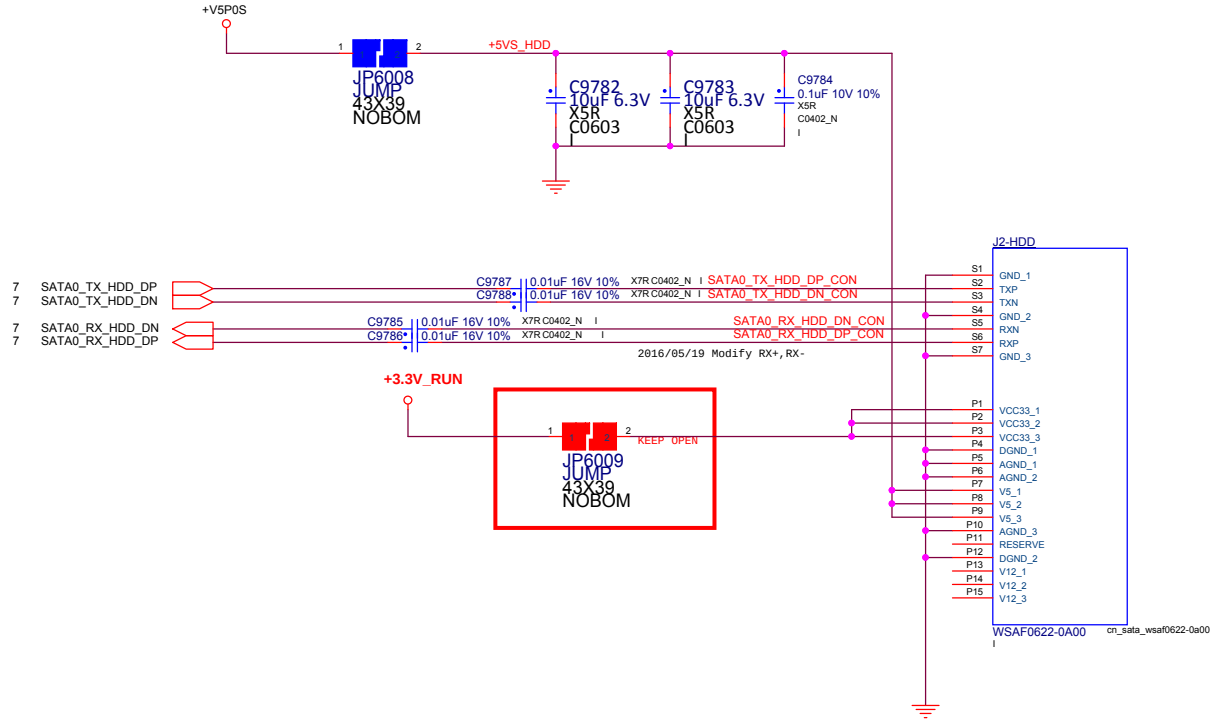
SPI ROM



Wed Jun 03 11:22:52 2015

3nod三诺	Project: 330S-14&15	
	Engineer: Ken	
Size: Custom	Title: SYSTEM FLASH	Rev: V01
Date: Monday, January 08, 2018	Sheet 24 of 81	

SATA HDD



INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.GND
Wed Jun 03 11:22:52 2015

3nod三诺	Project: 330S-14&15	
	Engineer: Ken	
Size: Custom	Title: HDD	Rev: V01
Date: Monday, January 08, 2018	Sheet 25 of 81	

M.2 SSD Module

EC-SVT-05

1.4A @ADATA 128GB SSD
2.6A @ADATA 256GB SSD

+3.3V_RUN — SH4200 (SHORT_0805) — +V3P3A_SSD

+V3P3A_SSD

C4209 22uF 6.3V 20% X5R C0603_N
C4204 22uF 6.3V 20% X5R C0603_N
C4205 0.1uF 10V 10% X5R C0402_N
C4206 0.1uF 10V 10% X5R C0402_N
C4207 0.1uF 10V 10% X5R C0402_N
C4208 0.1uF 10V 10% X5R C0402_N

JSSD1

1	GND_1	3.3V_2	2
3	GND_3	3.3V_4	4
5	PERn3	Reserved_6	6
7	PERp3	Reserved_8	8
9	GND_9	DAS/DSS# (O)(OD)	10
11	PETn3	3.3V_12	12
13	PETp3	3.3V_14	14
15	GND_15	3.3V_16	16
17	PERn2	3.3V_18	18
19	PERp2	Reserved_20	20
21	GND_21	Reserved_22	22
23	PETn2	Reserved_24	24
25	PETp2	Reserved_26	26
27	GND_27	Reserved_28	28
29	PERn1	Reserved_30	30
31	PERp1	Reserved_32	32
33	GND_33	Reserved_34	34
35	PETn1	Reserved_36	36
37	PETp1	DEVSLP (I)(0/3.3V)	38
39	GND_39	Reserved_40	40
41	PERn0/SATA-B+	Reserved_42	42
43	PERp0/SATA-B-	Reserved_44	44
45	GND_45	Reserved_46	46
47	PETn0/SATA-A-	Reserved_48	48
49	PETp0/SATA-A+	PERST# (I)(0/3.3V)	50
51	GND_51	CLKREQ# (IO)(0/3.3V)	52
53	REFCLKN	PEWake# (IO)(0/3.3V)	54
55	REFCLKP	Reserved_56	56
57	GND_57	Reserved_58	58
67	NC32	SUSCLK(32kHz) (I)(0/3.3V)	68
69	PEDET (OC-PCIe)	3.3V_70	70
71	GND_71	3.3V_72	72
73	GND_73	3.3V_74	74
75	GND_75		
76	GND12		
77	GND13		

Key M

51750-0750P-012
CON_75P_PH05_SMD_51736_RVS_M

20170718
yanzw
genhuan

3 PCIE_GPP_SSD_RX1N
3 PCIE_GPP_SSD_RX1P
3 PCIE_GPP_SSD_C_TX1N
3 PCIE_GPP_SSD_C_TX1P
M2_P0RXN
M2_P0RXP
M2_P0TXN
M2_P0TXP
7 PCIE_REFCLK_SSD_DN
7 PCIE_REFCLK_SSD_DP
R11367 0R R0402_N5%I PCIE_REFCLK_SSD_R_DN
R11362 0R R0402_N5%I PCIE_REFCLK_SSD_R_DP

+3.3V_ALW
R10869 100K 5% R0402_N I
R10870 100K 5% R0402_N NI
TP10111
SSD_PEDET
R10900 0R R0402_N5% NI
Pin69
PICE module spec is N/C
SATA module spec is GND

+V3P3A_SSD
R12430 0R R0402_N5% NI EC-SIT-06
SATA1_DEVSLP 7

+V3P3A_SSD
R4207 10K 5% R0402_N I
SSD_CLK_REQ_N_R
PCIE_WAKE_SSD_R_N
PLT_RST_N 6,43,50,74
R4206 0R R0402_N 5% I
R4205 0R R0402_N 5% NI
SSD_CLK_REQ_N 6
PCIE_WAKE_SSD_N 6
Pin54
PICE module spec is N/C
SATA module spec is N/C

PM_SUSCLK_SSD
TP9980
Pin68
PICE module spec is N/C
SATA module spec is N/C

3 PCIE_GPP_SSD_RX0P
3 PCIE_GPP_SSD_RX0N
0R C10911
0R C10912*
M2_P0RXP C10907 0.01uF 16V 10% X7R C0402_N NI
M2_P0RXN C10908 0.01uF 16V 10% X7R C0402_N NI
SATA1_RX_M2_DN 7
SATA1_RX_M2_DP 7

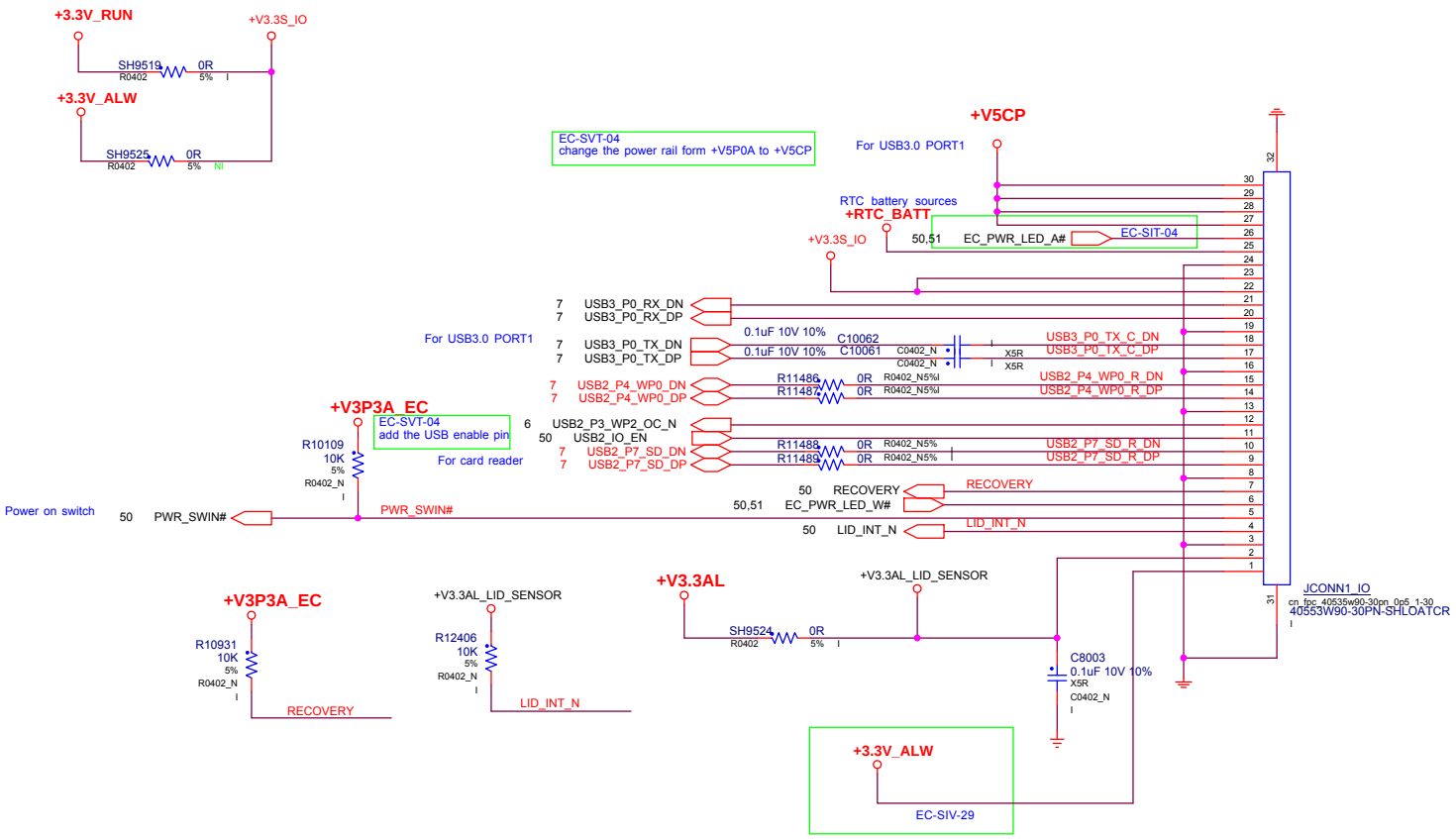
3 PCIE_GPP_SSD_C_TX0N
3 PCIE_GPP_SSD_C_TX0P
R4200 0R R0402_N5% I
R4201 0R R0402_N5% I
M2_P0TXN C10909 0.01uF 16V 10% X7R C0402_N NI
M2_P0TXP C10910 0.01uF 16V 10% X7R C0402_N NI
SATA1_TX_M2_DN 7
SATA1_TX_M2_DP 7

INTERNAL ONLY

BPAGE DRAWING
sky_y_mrd.+V3P3.26
Wed Jun 03 11:22:52 2015

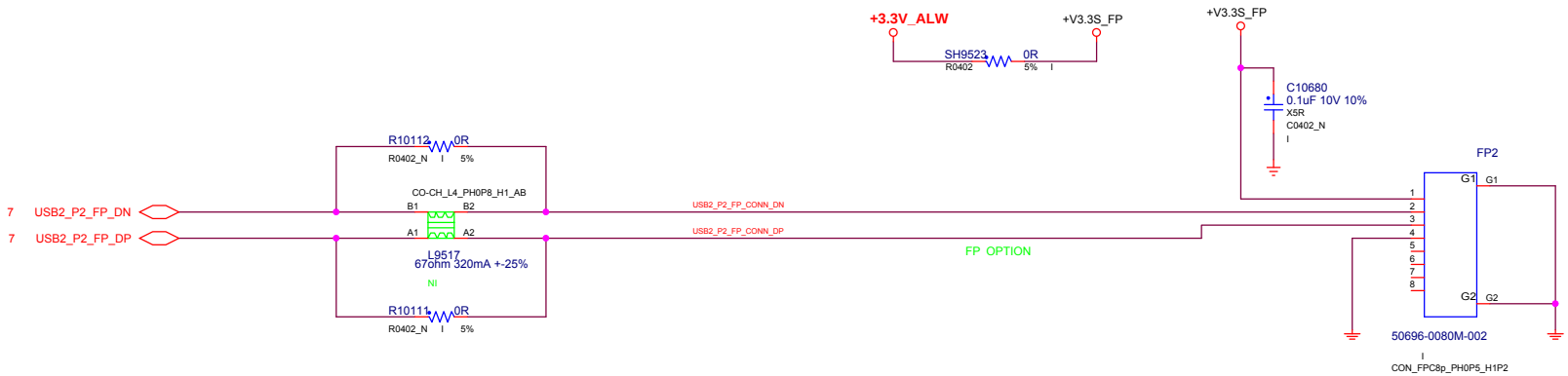
3nod三诺	Project: 330S-14&15	
	Engineer: Ken	
Size: Custom	Title: PCIE SSD MODULE	Rev: V01
Date: Monday, January 08, 2018	Sheet 26 of 81	

IO connector/USB3.0 PORT&USB card reader&LID sensor



3nod三诺	Project: 330S-14&15	
	Engineer: Ken	
Size: Custom	Title: IO CONNECTOR	Rev: V01
Date: Thursday, January 11, 2018	Sheet 27 of 81	

Finger Print



INTERNAL ONLY

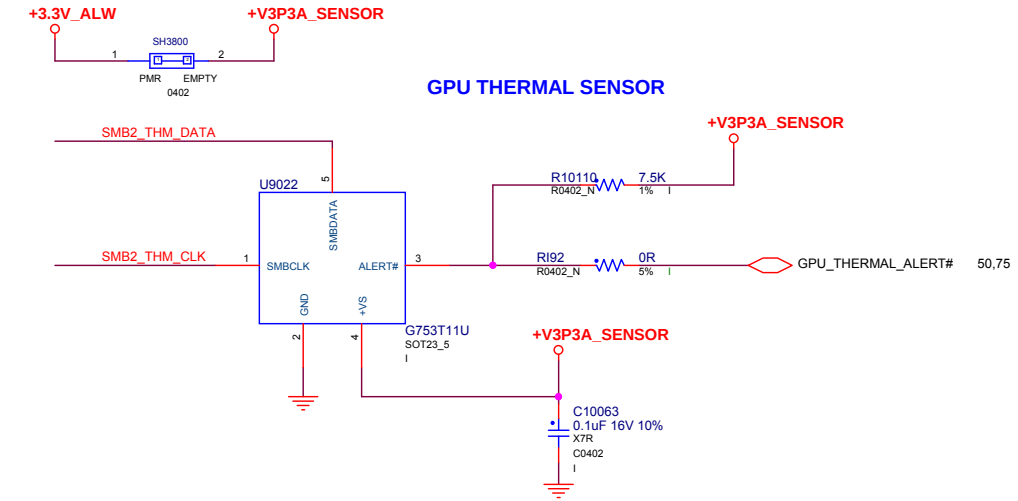
BPAGE DRAWING

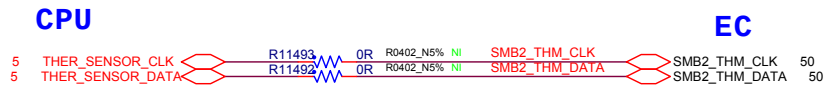
sky_y_mrd.GND
Wed Jun 03 11:22:53 2015

3nod三诺	Project: 330S-14&15	
	Engineer: Ken	
Size: Custom	Title: FINGER PRINT	Rev: V01
Date: Monday, January 08, 2018	Sheet 28 of 81	

Thermal Sensor

1/4 Add connect to SOC & EC





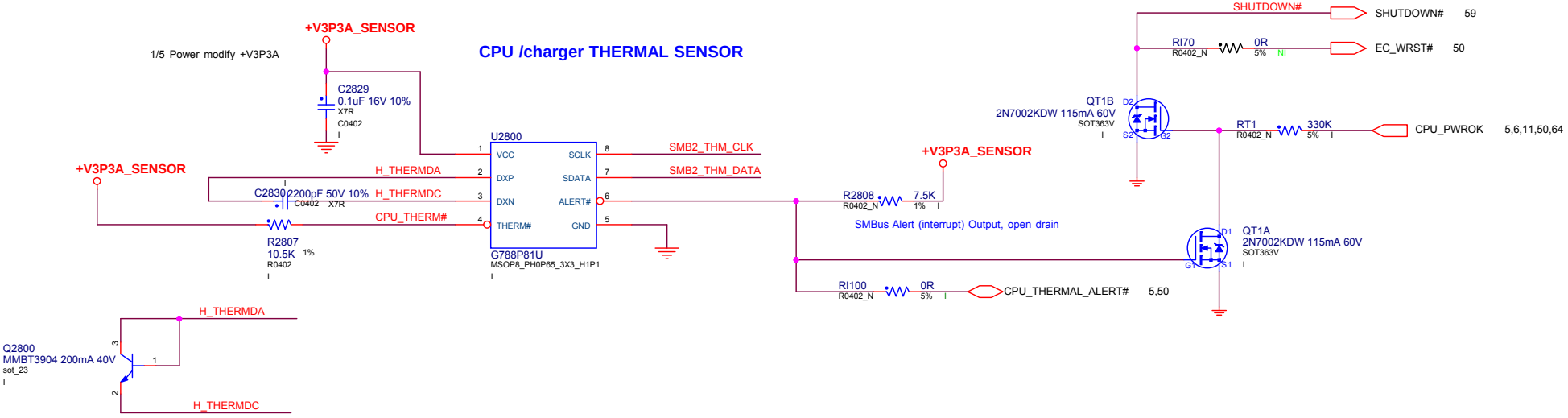
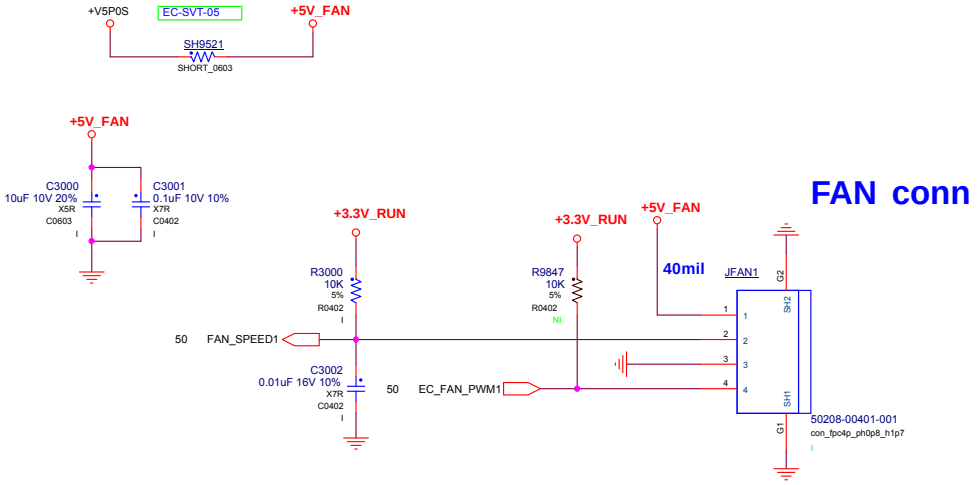


Table 10. Remote temperature $\overline{\text{THERM}}$ limit

The default value is trapping after power up 100ms by different pull-up resistors of $\overline{\text{THERM}}$ and $\overline{\text{ALERT}}$ pin:

TEMPERATURE (°C)		$\overline{\text{THERM}}$				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

3nod三诺	Project:	330S-14&15
	Engineer:	Ken
Size: B	Title: CPU THERMAL SENSOR	Rev: V01
Date: Monday, January 08, 2018	Sheet 29 of 81	



FAN conn

1/11 Update FAN pin define

CIS ok

3nod三诺	Project: 330S-14&15	
	Engineer: Ken	
Size: Custom	Title: FAN conn	Rev: V01
Date: Monday, January 08, 2018	Sheet 30 of 81	

Project:	3305-14835
Engineer:	Alex
Title:	NA

INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.+V3P3.32
Wed Jun 03 11:22:55 2015

3nod三诺	Project: 330S-14&15	
	Engineer: Ken	
Size: Custom	Title: NA	Rev: V01
Date: Monday, January 08, 2018	Sheet 32 of 81	

INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.+V1P0.33
Wed Jun 03 11:22:55 2015

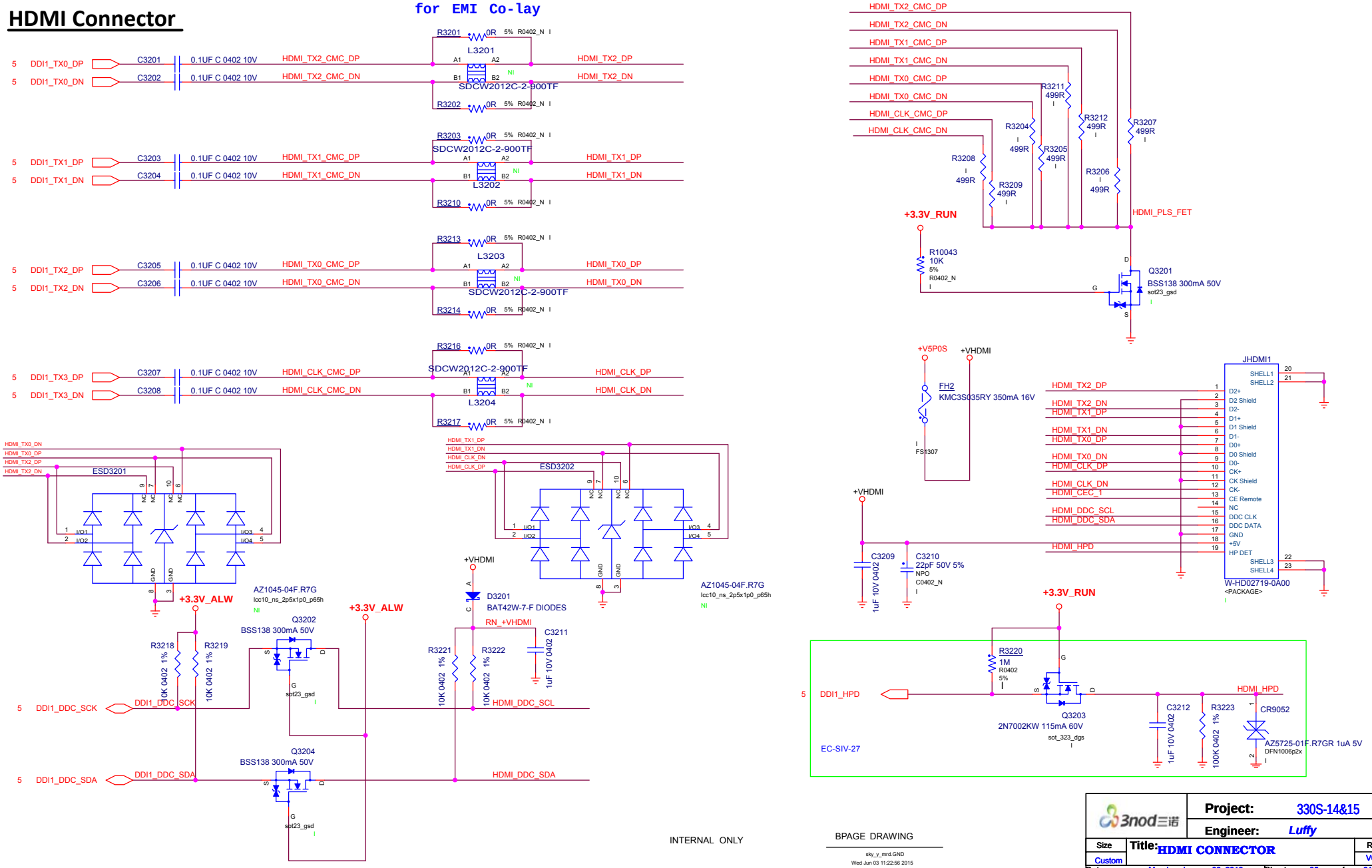
3nod三诺	Project: 330S-14&15	
	Engineer: Ken	
Size: Custom	Title: NA	Rev: V01
Date: Monday, January 08, 2018	Sheet 33 of 81	

Wed Jun 03 11:22:56 2015

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: NA	Rev: V01
Date: Monday, January 08, 2018	Sheet 34 of 81	

HDMI Connector

for EMI Co-lay



INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.GND
Wed Jun 03 11:22:56 2015

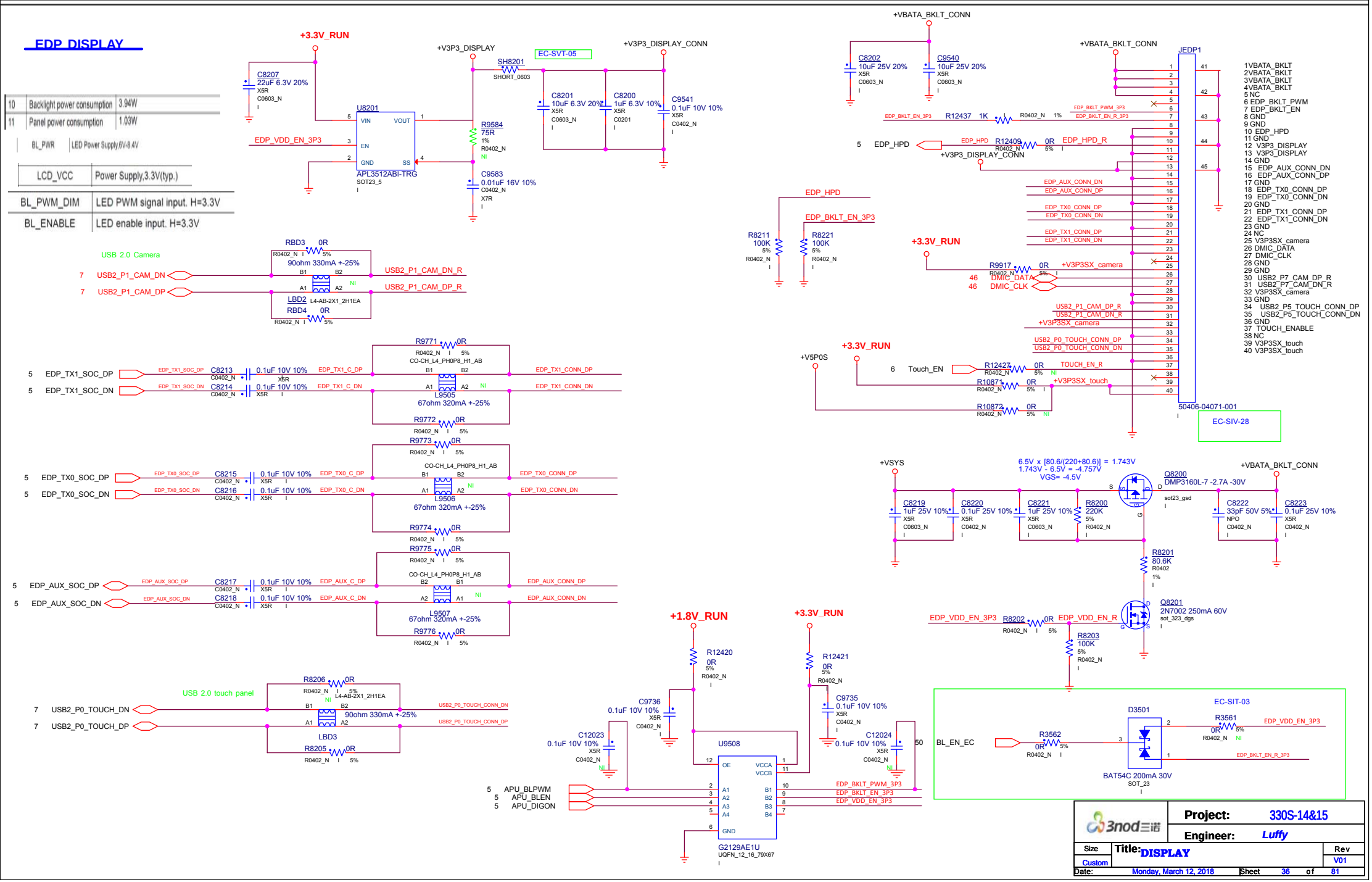
3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: HDMI CONNECTOR	Rev: V01
Date: Monday, January 08, 2018	Sheet 35 of 81	

EDP_DISPLAY

10	Backlight power consumption	3.94W
11	Panel power consumption	1.03W

BL_PWR | LED Power Supply,6V~8.4V

LCD_VCC	Power Supply,3.3V(typ.)
BL_PWM_DIM	LED PWM signal input. H=3.3V
BL_ENABLE	LED enable input. H=3.3V



Project:	330S-14&15		
Engineer:	Luffy		
Size: Custom	Title: DISPLAY		Rev: V01
Date: Monday, March 12, 2018	Sheet 36 of 81		

BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:32 2016

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: USB2.0	Rev: V01
Date: Monday, January 08, 2018	Sheet 37 of 81	

Sensors

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: LID	Rev: V01
Date: Monday, January 08, 2018	Sheet 38 of 81	

3nod三诺	Project: 330S-14&15	
	Engineer: *Luffy*	
Size: Custom	Title: NA	Rev: V01
Date: Monday, January 08, 2018	Sheet 39 of 81	

Wed Jun 03 11:22:59 2015

3nod三诺	Project: 330S-14&15		
	Engineer: *Luffy*		
Size: Custom	Title: NA		Rev: V01
Date: Monday, January 08, 2018	Sheet 40 of 81		

INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.+V3P3.41
Wed Jun 03 11:22:59 2015

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: NA	Rev: V01
Date: Monday, January 08, 2018	Sheet 41 of 81	

USB3.0

+V5CP → R10060 SHORT_0805 → +V5CP_R

EC-SVT-05

4/20 change rating

CC452 22uF 6.3V 20% X5R C0603_N

C3900 0.1uF 10V 10% X7R C0402_N

+V5CP_R

R3902 20K 5% R0402_N

R3903 82K 1% R0402_N EC-SIT-11 min 1.5A

USB2_P5_WP0_OC_N 6

U3900

+V5P0A_USB_WP2

4/7 change from +V3P3A to +V3.3AL.

7 USB2_P5_WP1_DN

7 USB2_P5_WP1_DP

USB2_P5_DN

USB2_P5_DP

+V3.3AL

R3958 100K 5% R0402_N

TPS2546RTER

USB_STATUS# → USB_STATUS# 50

TPS2546_CTL3 50

TPS2546_CTL2 50

TPS2546_CTL1 50

+V3.3AL

R3900 100K 5% R0402

50 EC_ACDET → R3961 0R R0402_N 5%

R3901 0R R0402_N 5% NI

EC_USB_PWR_EN_R

R3960 0R R0402_N 5%

50 EC_USB_PWR_EN

D+/D- ESD

USB2_P5_WP1_DP_CONN

USB2_P5_WP1_DN_CONN

CR9012 AZ5725-01F.R7GR 1uA 5V DFN1006p2x

CR9013 AZ5725-01F.R7GR 1uA 5V DFN1006p2x

+V5P0A_USB_WP2

5/22 change to 100uF

C10022 100uF 6.3V +/-20% SMD3.5X2.8mm

C9006 470pF 50V 5% COG C0402_N

C9007 4.7uF 10V 10% X5R C0603_N

CR9054 AZ5725-01F.R7GR 1uA 5V DFN1006p2x

5/22 add ESD

CR9081 0R 5% NI R0603_N

JUSB3-1

USB3_P1_TX_DP_CONN

USB3_P1_TX_DN_CONN

USB3_P1_RX_DN_CONN

USB3_P1_RX_DP_CONN

CR9006

AZ1045-04F.R7G lcc10_ns_2p5x1p0_p65h

R9007 0R R0402_N 5%

L9003 67ohm 320mA +-25% CO-CH_L4_PH0P8_H1_AB NI

R9006 0R R0402_N 5%

R9853 0R R0402_N 5%

7 USB3_P1_RX_DN

7 USB3_P1_RX_DP

L9508 67ohm 320mA +-25% NI

R9852 0R R0402_N 5%

R9012 0R R0402_N 5%

7 USB3_P1_TX_DN → C1271 0.1uF 10V 10% X5R C0402_N

7 USB3_P1_TX_DP → C1270 0.1uF 10V 10% X5R C0402_N

L9002 67ohm 320mA +-25% NI

R9011 0R R0402_N 5%

+V3.3AL

EC-SIT-02

R10934 100K 5% R0402_N

50 USB3.0_DETECT

W-US09809-0A00 cn_usb-3_w-us09809-0a00

VBUS D- D+ GND STDA_SSRX- STDA_SSRX+ GND_DRAIN STDA_SSTX- STDA_SSTX+ USB_DETECT GND1 GND2 GND3 GND4

CIS OK - 20170717 YD

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: USB3.0 CONN	Rev: V01
Date: Thursday, March 15, 2018	Sheet 42 of 81	

WIFI & BT Module

+3.3V_RUN
+V3P3SX_CWS
SH4302
SHORT_0603
EC-SVT-05
+3.3V_ALW
SH4303
0R
NI
R0603_N
5%
EC-SIT-13
+V3P3SX_CWS
C4320 4.7uF 6.3V 10% X5R C0603_N I
C4321 4.7uF 6.3V 10% X5R C0603_N I
C4322 0.1uF 10V 10% X5R C0402_N I
C4323 0.1uF 10V 10% X5R C0402_N I
C6001 & C6003 FOR PIN 72 &73
C6002 & C6000 FOR PIN 4 & 5
PCIE*2 Gen2 for WIFI

CIS ok

JWLAN1
SLOT A KEY E
KEY E
PLATFORM PIN OUT

1	GND_1	2	3.3V_2
3	USB_D+	4	3.3V_4
5	USB_D-	6	LED1_N
7	GND_7	8	PCM_CLK/I2S_SCK
9	SDIO_CLK	10	PCM_SYNC/I2S_WS
11	SDIO_CMD	12	PCM_IN/I2S_SD_IN
13	SDIO_DATA0	14	PCM_OUT/I2S_SD_OUT
15	SDIO_DATA1	16	LED2_N
17	SDIO_DATA2	18	GND_18
19	SDIO_DATA3	20	UART_WAKE_N
21	SDIO_WAKE_N	22	UART_RX
23	SDIO_RESET_N		
33	GND_33	32	UART_TX
35	PETP0	34	UART_CTS
37	PETN0	36	UART_RTS
39	GND_39	38	RESERVED_38
41	PERP0	40	RESERVED_40
43	PERN0	42	RESERVED_42
45	GND_45	44	COEX3
47	REFCLKP0	46	COEX2
49	REFCLKN0	48	COEX1
51	GND_51	50	SSCLK
53	CLKREQ0_N	52	PERST0_N
55	PEWAKE0_N	54	RESERVED_W_DISABLE2_N
57	GND_57	56	W_DISABLE1_N
59	RESERVED_2ND_PETP1	58	I2C_DATA
61	RESERVED_2ND_PETN1	60	I2C_CLK
63	GND_63	62	ALERT
65	RESERVED_2ND_PERP1	64	RESERVED_64
67	RESERVED_2ND_PERN1	66	UIM_SWP/PERST1_N
69	GND_69	68	UIM_PWR_SNK/CLREQ1_N
71	RESERVED/REFCLKN1	70	UIM_PWR_SRC/GPIO1/PEWAKE1_N
73	RESERVED/REFCLKP1	72	3.3V_72
75	GND_75	74	3.3V_74
76	GND76	77	GND77

51750-0750P-005
TBD I

7 USB2_P3_BT_DP
7 USB2_P3_BT_DN
R11485 0R R0402_N5%I
R11484 0R R0402_N5%I
+V3P3SX_CWS
TP9992
TP9993
WIFI/BT_SLOT_TX
WIFI/BT_SLOT_RX
TP9976
TP9977
3 PCIE_GPP_WLAN_C_TX3P
3 PCIE_GPP_WLAN_C_TX3N
3 PCIE_GPP_WLAN_RX3P
3 PCIE_GPP_WLAN_RX3N
7 PCIE_REFCLK_WLAN_DP
7 PCIE_REFCLK_WLAN_DN
R9890 0R R0402_N5%I PCIE_REFCLK_WLAN_R_DP
R9889 0R R0402_N5%I PCIE_REFCLK_WLAN_R_DN
6 WLAN_CLK_REQ_N
6 PCIE_WAKE_WIFI_N
WLAN_CLK_REQ_N
R11494 0R R0402_N5%I WLAN_CLK_REQ_R_N
7,10,50 LPC_FRAME_N
7,50 LPC_AD3
7,50 LPC_AD2
7,50 LPC_AD1
7,50 LPC_AD0
7,10 LPC_CLK1
R4320 0R R0402_N 5% I
SUS_CLK_R
WLAN_RST_R
RTC_CLK 6,10,50
BT_DISABLE_N
WIFI_DISABLE_N
BT_DISABLE_N 6 EC-SIT-14
WIFI_DISABLE_N 6
SM_BAT_DATA_DEBUG
SM_BAT_CLK_DEBUG
TP10009
TP10010

4/21 Add SM_BAT_DATA connect to JWLAN1.58,
Add SM_BAT_CLK connect to JWLAN1.60,
Debug card need.

4/21 Add R4325,R4326 0ohm for Debug card

6/27 R4325,R4326 change to NI,
because WLAN card "Intel 2x2AC 8260" I2C is 1.8V,
mother board I2C is 3.3V

CIS OK - 20170717 YD

WLAN PCIE AC CAPS

+V3P3SX_CWS
R4321 10K 5% R0402_N I
WLAN_CLK_REQ_N

+V3P3SX_CWS
R12410 10K 5% R0402_N NI
BT_DISABLE_N

+V3P3SX_CWS
R12411 10K 5% R0402_N I
WIFI_DISABLE_N

Difference with armour
Reserve PLT_RST_N to reset pin and install

WLAN_RST_R
R4323 0R R0402_N I 5%
R4324 0R R0402_N NI 5%
PLT_RST_N 6,26,50,74
LPC_RST_N 7,50

INTERNAL ONLY

BPAGE DRAWING
sky_y_mrd.+V3P3.43
Wed Jun 03 11:23:00 2015

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: WLAN WIFI BT MODULE	Rev: V01
Date: Tuesday, February 06, 2018	Sheet 43 of 81	

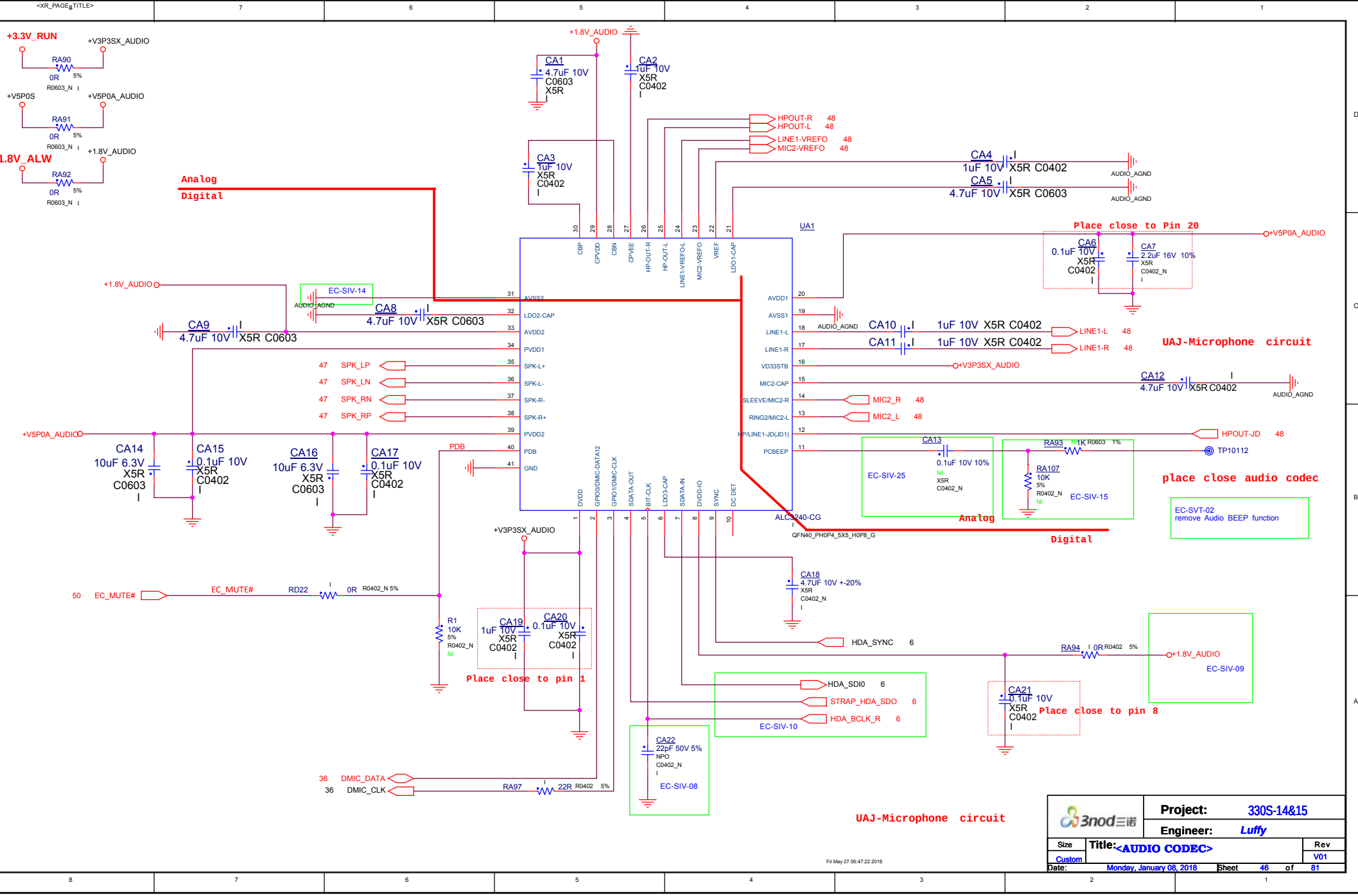
Project:	330S-14&15
Engineer:	Luffy
Size: Custom	Title: NA
Rev	V01
Date: Monday, January 08, 2018	Sheet 44 of 81

INTERNAL ONLY

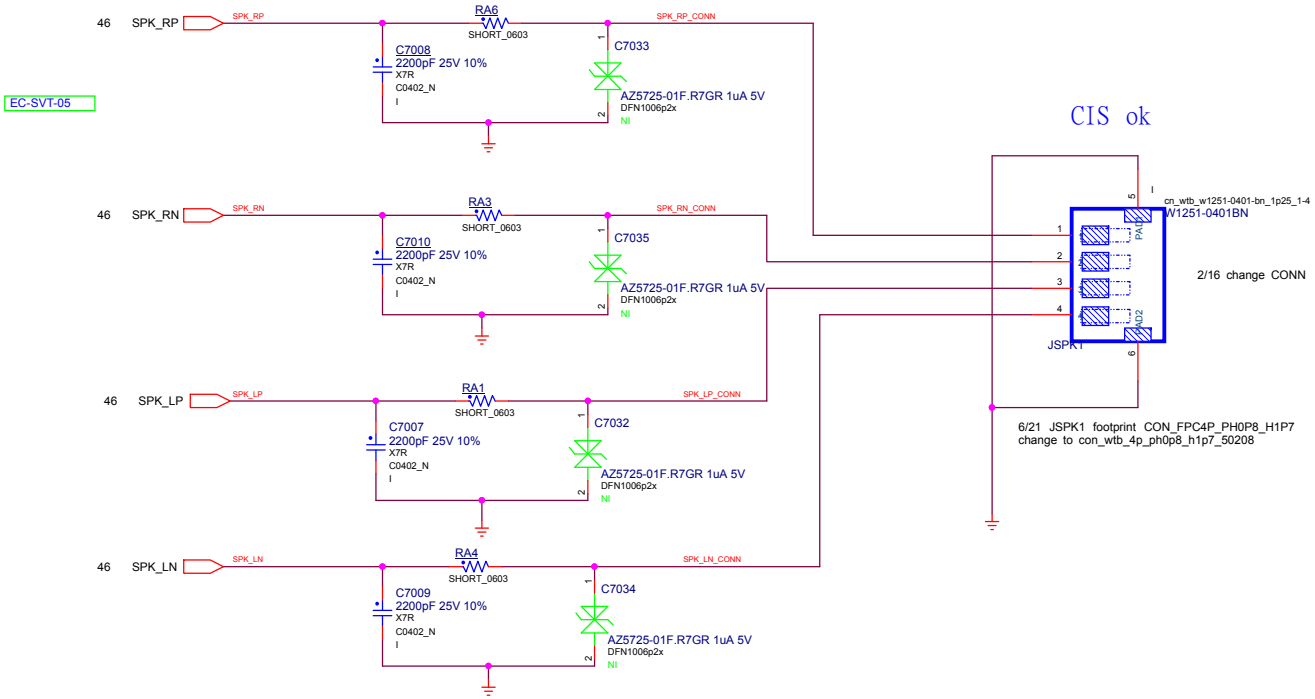
BPAGE DRAWING

sky_y_mrd.GND
Wed Jun 03 11:23:01 2015

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: NA	Rev: V01
Date: Monday, January 08, 2018	Sheet 45 of 81	


+3.3V_RUN
+V3P3SX_AUDIO
RA90
0R 5%
R0603_N
+V5P0S
+V5P0A_AUDIO
RA91
0R 5%
R0603_N
+1.8V_ALW
+1.8V_AUDIO
RA92
0R 5%
R0603_N
Analog
Digital
+1.8V_AUDIO
CA1
4.7uF 10V
C0603
X5R
CA2
1uF 10V
X5R
C0402
CA3
1uF 10V
X5R
C0402
HPOUT-R 48
HPOUT-L 48
LINE1-VREFO 48
MIC2-VREFO 48
CA4
1uF 10V X5R C0402
CA5
4.7uF 10V X5R C0603
AUDIO_AGND
UA1
CBP
CPVDD
CBN
CPVEE
HP-OUT-R
HP-OUT-L
LINE1-VREFO-L
MIC2-VREFO
VREF
LDO1-CAP
Place close to Pin 20
CA6
0.1uF 10V
X5R
C0402
CA7
2.2uF 16V 10%
X5R
C0402_N
+V5P0A_AUDIO
EC-SIV-14
AUDIO_AGND
CA8
4.7uF 10V X5R C0603
CA9
4.7uF 10V X5R C0603
AVSS2
LDO2-CAP
AVDD2
PVDD1
SPK-L+
SPK-L-
SPK-R-
SPK-R+
PVDD2
PDB
GND
AVDD1
AVSS1
LINE1-L
LINE1-R
VD33STB
MIC2-CAP
SLEEVE/MIC2-R
RING2/MIC2-L
HP/LINE1-JD(JD1)
PCBEEP
CA10
1uF 10V X5R C0402
CA11
1uF 10V X5R C0402
LINE1-L 48
LINE1-R 48
+V3P3SX_AUDIO
CA12
4.7uF 10V X5R C0402
MIC2_R 48
MIC2_L 48
HPOUT-JD 48
TP10112
UAJ-Microphone circuit
47 SPK_LP
47 SPK_LN
47 SPK_RN
47 SPK_RP
CA13
0.1uF 10V 10%
NI
X5R
C0402_N
EC-SIV-25
RA93 1K R0603 1%
RA107
10K
5%
R0402_N
NI
EC-SIV-15
place close audio codec
EC-SVT-02
remove Audio BEEP function
CA14
10uF 6.3V
X5R
C0603
CA15
0.1uF 10V
X5R
C0402
CA16
10uF 6.3V
X5R
C0603
CA17
0.1uF 10V
X5R
C0402
PDB
DVDD
GPIO0/DMIC-DATA1/2
GPIO1/DMIC-CLK
SDATA-OUT
BIT-CLK
LDO3-CAP
SDATA-IN
DVDD-IO
SYNC
DC DET
ALC3240-CG
QFN40_PH0P4_5X5_H0P8_G
Analog
Digital
+V3P3SX_AUDIO
CA18
4.7uF 10V +-20%
X5R
C0402_N
50 EC_MUTE#
EC_MUTE#
RD22
0R R0402_N 5%
R1
10K
5%
R0402_N
NI
CA19
1uF 10V
X5R
C0402
CA20
0.1uF 10V
X5R
C0402
Place close to pin 1
HDA_SYNC 6
RA94 0R R0402 5%
+1.8V_AUDIO
EC-SIV-09
HDA_SDI0 6
STRAP_HDA_SDO 6
HDA_BCLK_R 6
EC-SIV-10
CA21
0.1uF 10V
X5R
C0402
Place close to pin 8
CA22
22pF 50V 5%
NPO
C0402_N
EC-SIV-08
36 DMIC_DATA
36 DMIC_CLK
RA97 22R R0402 5%
UAJ-Microphone circuit
Fri May 27 06:47:22 2016
3nod三诺
Project: 330S-14&15
Engineer: Luffy
Size
Custom
Title: <AUDIO CODEC>
Rev
V01
Date: Monday, January 08, 2018
Sheet 46 of 81

Speaker



INTERNAL ONLY

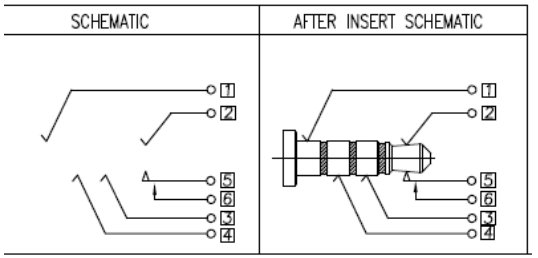
BPAGE DRAWING

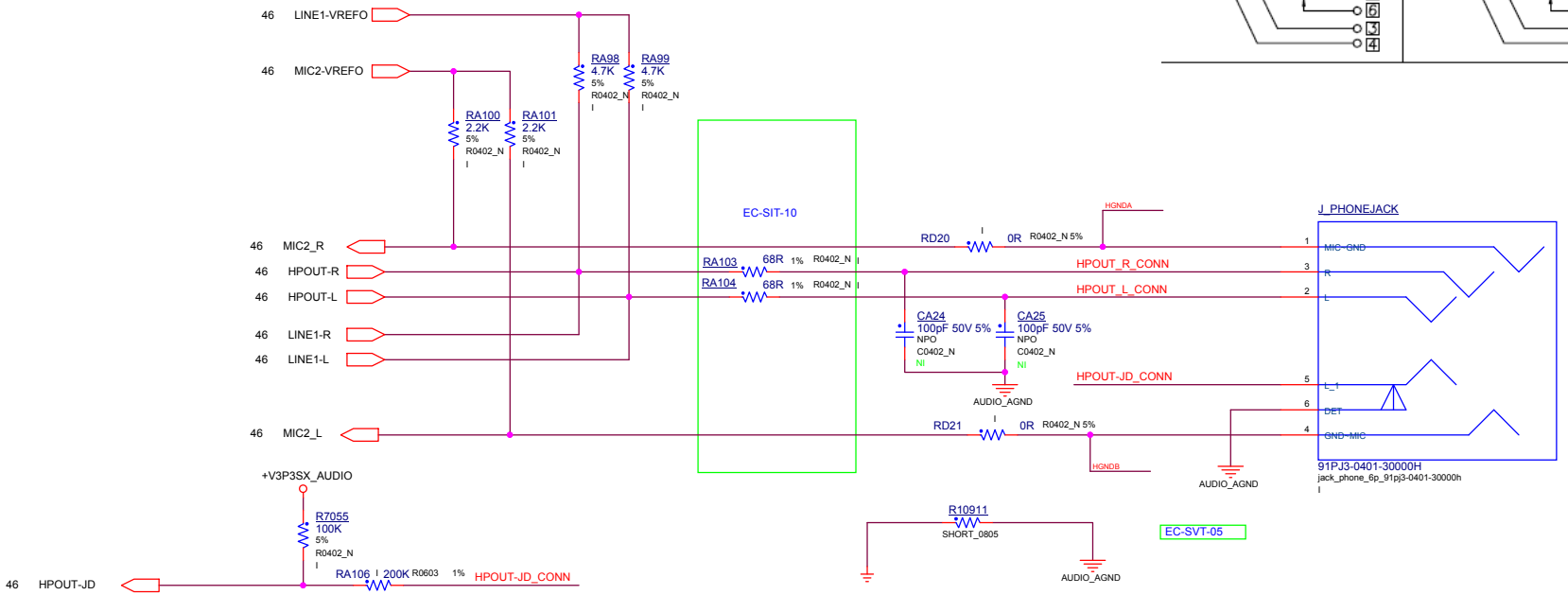
sky_y_mrd.GND
Wed Jun 03 11:23:02 2015

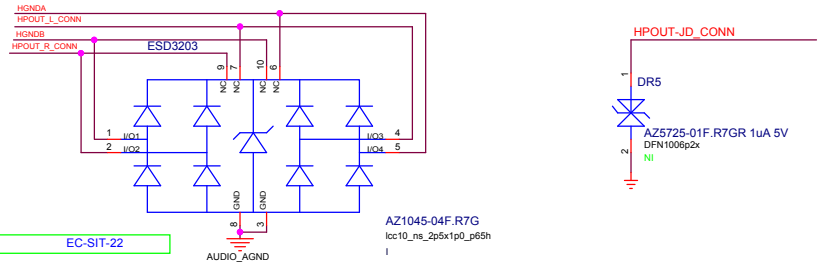
3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: Speaker	Rev: V01
Date: Wednesday, January 10, 2018	Sheet 47 of 81	

HEADSET JACK (Supports CTIA and OMTP headsets)

Important:
To ensure reliable headset detection for all fast/slow plug-in scenarios use a jack with the detect switch all the way at the end so that the switch is tripped only when the jack is plugged all the way in.







INTERNAL ONLY

BPAGE DRAWING

apl_tf.8A
Fri May 27 06:47:24 2016

3nod三诺	Project:	330S-14&15
	Engineer:	Luffy
Size: Custom	Title: <AUDIO_HEADSET>	Rev: V01
Date: Monday, January 08, 2018	Sheet 48 of 81	

BPAGE DRAWING

sky_y_rnrd.+VCHG.49
Wed Jun 03 11:23:03 2015

3nod三诺	Project: 330S-14&15	
	Engineer: *Luffy*	
Size: Custom	Title: NA	Rev: V01
Date: Monday, January 08, 2018	Sheet 49 of 81	

EC controller

version ID

version ID	14"	15"
VERSION_ID0	1	0

version ID	DIS	UMA
VERSION_ID1	1	0

Memory ID

Memory ID	Samsung 4GB	Hynix 4GB	Micron 4GB
SKU_ID0	0	0	0
SKU_ID1	0	0	1
SKU_ID2	0	1	0

MEM ID

Version ID

GFX
Charger
Thermal
Battery

KB connector

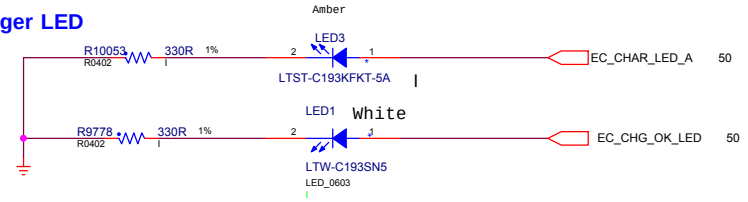
Keyboard backlight

Touch Pad

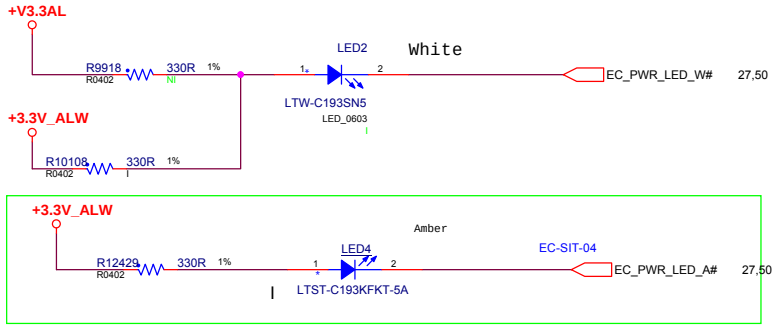
Power Supply Voltage 5.0 Volt ± 10%
Power Supply Current:3 mA nominal

Project:	330S-14&15	
Engineer:	Luffy	
Size: D	Title: EMBEDDED CONTROLLER	Rev: V01
Date: Wednesday, March 28, 2018	Sheet 59 of 81	

Charger LED



SYS LED



3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: BUTTON & LED	Rev: V01
Date: Monday, February 05, 2018	Sheet 51 of 81	

Project:	330S-14&15
Engineer:	Luffy
Size: Custom	Title: TYPE-C Switch
Rev: V01	
Date: Monday, January 08, 2018	Sheet 52 of 81

Type c connector 15"

54,55 C_TX2_N
RC470 0R 5% R0402_N I-15 CO-CH_L4_PH0P8_H1_AB
B1 B2 SSTX2-_CONN_15
A1 A2 NI SSTX2+_CONN_15
LC1 67ohm 320mA +-25%
54,55 C_TX2_P
RC471 0R 5% R0402_N I-15

54,55 C_TX1_N
RC472 0R 5% R0402_N I-15 CO-CH_L4_PH0P8_H1_AB
A1 A2 SSTX1-_CONN_15
B1 B2 NI SSTX1+_CONN_15
LC2 67ohm 320mA +-25%
54,55 C_TX1_P
RC473 0R 5% R0402_N I-15

54,55 C_RX2_N
RC474 0R 5% R0402_N I-15 CO-CH_L4_PH0P8_H1_AB
B1 B2 SSRX2-_CONN_15
A1 A2 NI SSRX2+_CONN_15
LC3 67ohm 320mA +-25%
54,55 C_RX2_P
RC475 0R 5% R0402_N I-15

54,55 C_RX1_N
RC476 0R 5% R0402_N I-15
A1 A2 SSRX1-_CONN_15
LC4
B1 B2 NI SSRX1+_CONN_15
67ohm 320mA +-25% CO-CH_L4_PH0P8_H1_AB
54,55 C_RX1_P
RC477 0R 5% R0402_N I-15

RC478 0R 5% R0402_N I-15
7,55 USB2_P6_WP2_DN
A1 A2 DP_CON DP_CON 55
LC5
7,55 USB2_P6_WP2_DP
B1 B2 NI DM_CON SWAP FOR ROUTING DM_CON 55
67ohm 320mA +-25% CO-CH_L4_PH0P8_H1_AB
RC479 0R 5% R0402_N I-15

For TYPE C

SSRX2-_CONN_15
SSRX2+_CONN_15
SSTX2+_CONN_15
SSTX2-_CONN_15
CR9520
ESD5344D
DFN10_PH0P5_ESD
I-15

SSRX1+_CONN_15
SSRX1-_CONN_15
SSTX1-_CONN_15
SSTX1+_CONN_15
CR9521
ESD5344D
DFN10_PH0P5_ESD
I-15

EC-SIV-22

JTYPE_C_15
USB11249-0500B-1H
I-15
+VBUS_TYPEC
+VBUS_TYPEC

20170718
yanzw
genhuan

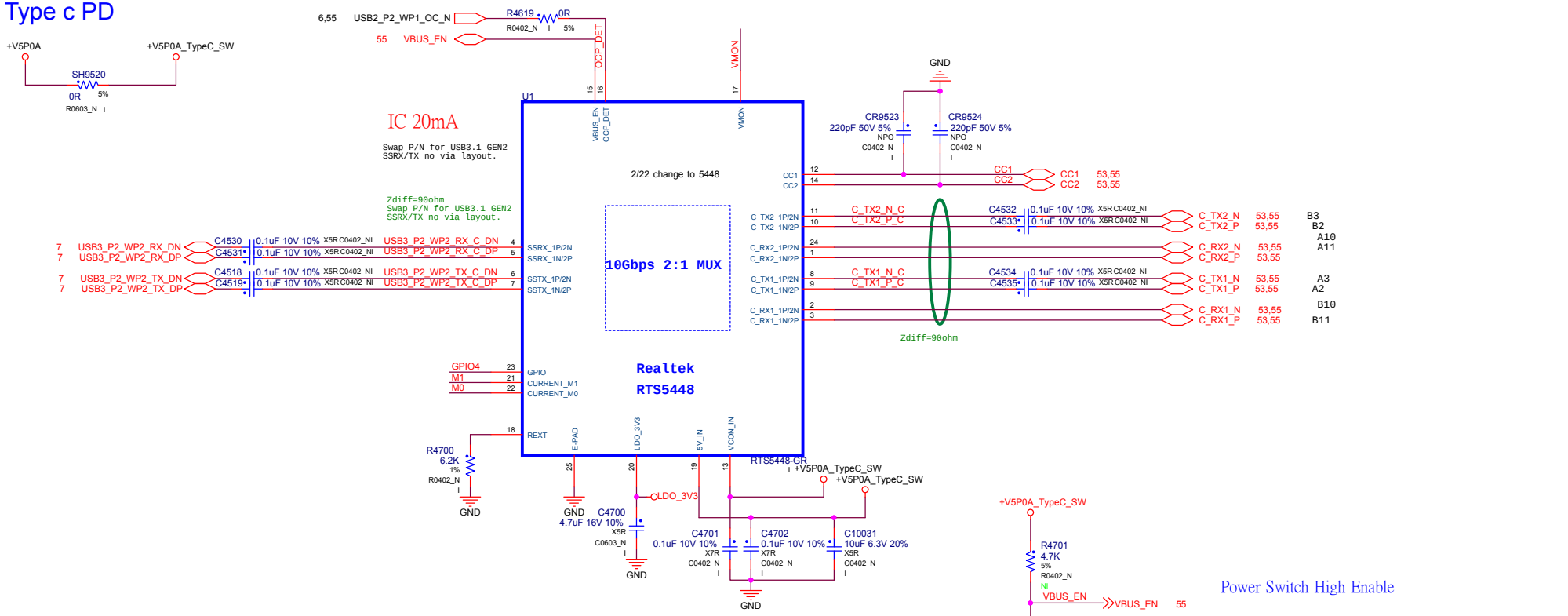
SSRX2+_CONN_15
SSRX2-_CONN_15
SBU1
DP_CON
DM_CON
SWAP FOR ROUTING
54,55 CC1
SSTX1-_CONN_15
SSTX1+_CONN_15

SSTX2+_CONN_15
SSTX2-_CONN_15
DM_CON
DP_CON
SBU2
CC2 54,55
SWAP FOR ROUTING
SSRX1-_CONN_15
SSRX1+_CONN_15

cn_usb-c_usb1124x-0500b-1h

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: TYPE-C CONN	Rev: V01
Date: Monday, January 08, 2018	Sheet 53 of 81	

Type c PD

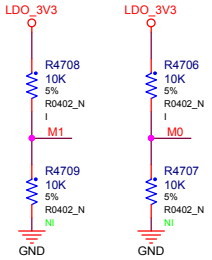


Power Switch High Enable

Power switch enable pin	Note
Low Active	R4701/R4702 mount
High Active	R4702 mount,R16 don't mount

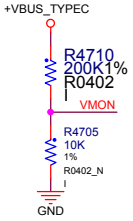
For C_VBUS
power switch enable pin

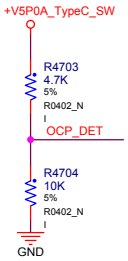
Rp configuration



	M1	M0
Rp:900mA	0	1
Rp:1.5A	1	0
Rp:3.0A	1	1

Rp:3A (now)





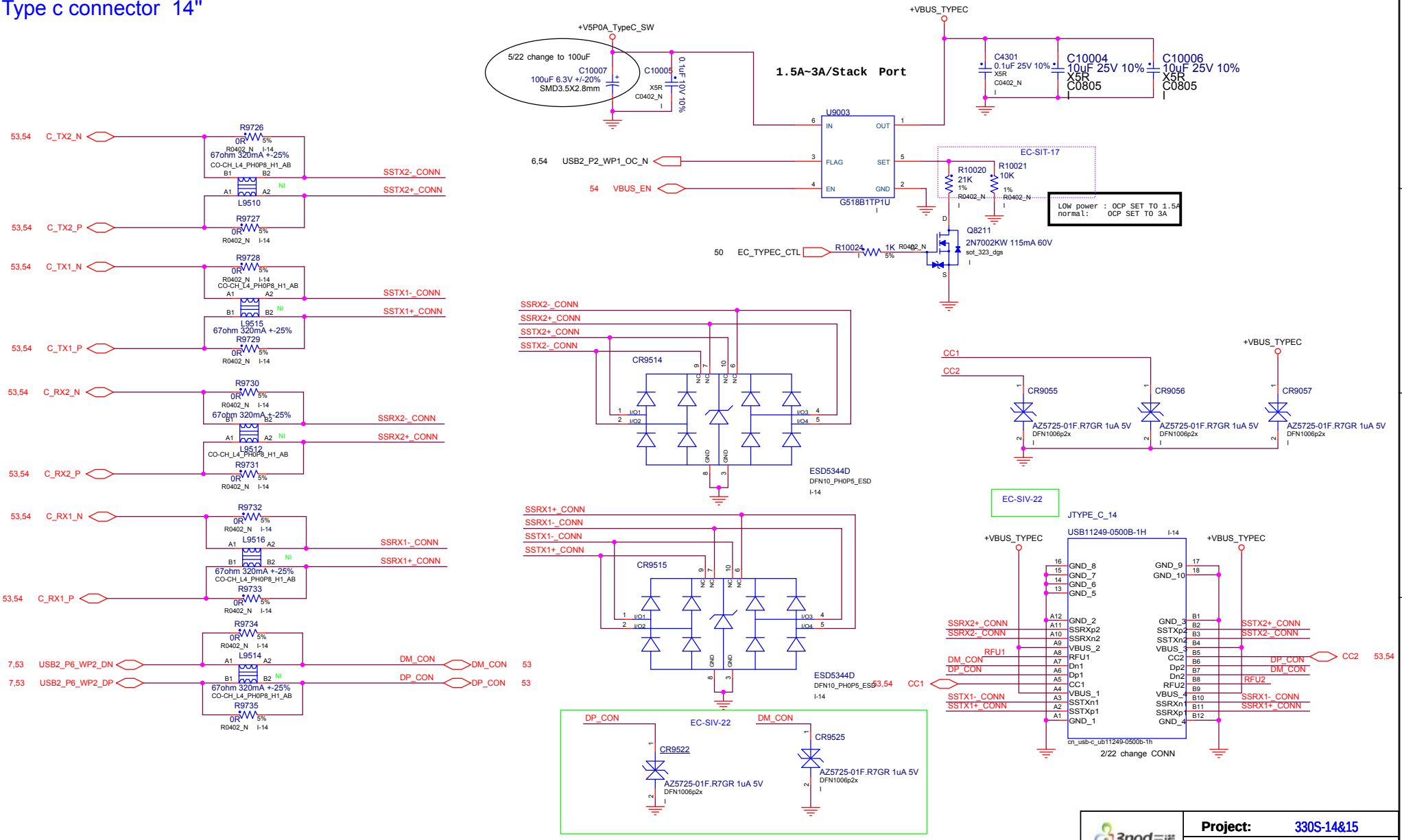
OCP Low Enable

Power switch OCP pin	Note
Low Active	R4704/R4703 mount
High Active	R4704 mount,R4703 don't mount

For C_VBUS
power switch OCP pin

3nod三诺	Project:	330S-14&15
	Engineer:	Luffy
Size: Custom	Title: TYPE-C Switch	Rev: V01
Date: Monday, January 08, 2018	Sheet 54 of 81	

Type c connector 14"



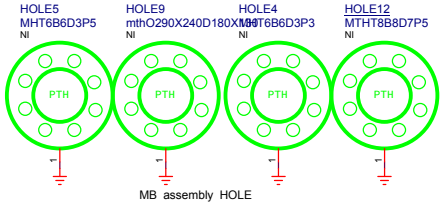
3nod三诺	Project:	330S-14&15
	Engineer:	Luffy
Size: Custom	Title: TYPE-C CONN	Rev: V01
Date: Tuesday, February 06, 2018	Sheet 55 of 81	

Shielding

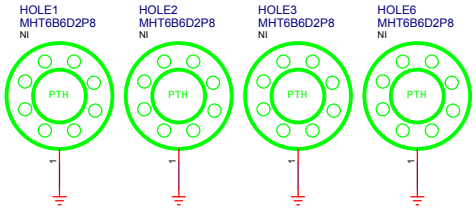
Holes

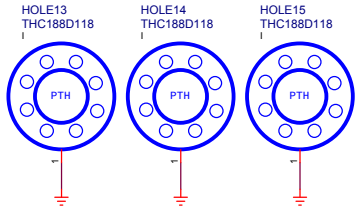
2.8mm

3/30 chnage screw

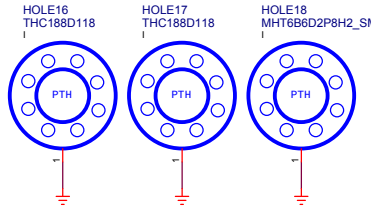


MB assembly HOLE

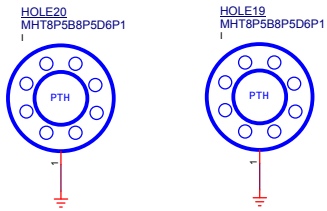


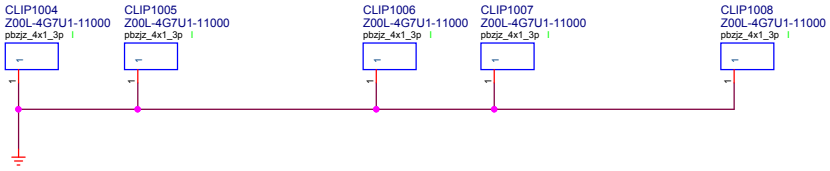


GPU THERMAL HOLE



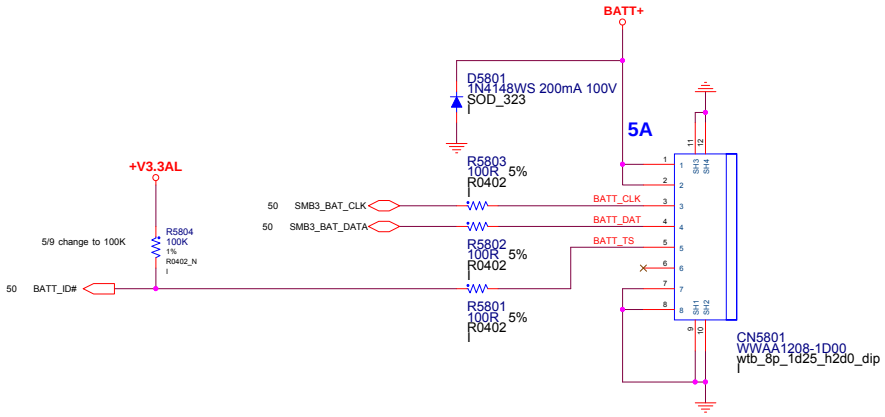
CPU THERMAL HOLE



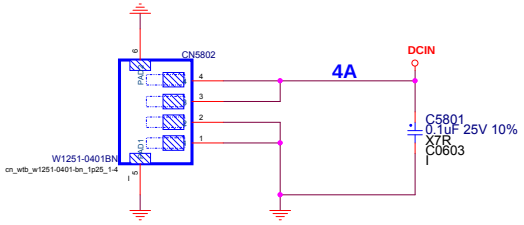


3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: UART CONN & HOLE & CLIP	Rev: V01
Date: Thursday, January 11, 2018	Sheet 56 of 81	

57: BATTERY CONNECTOR

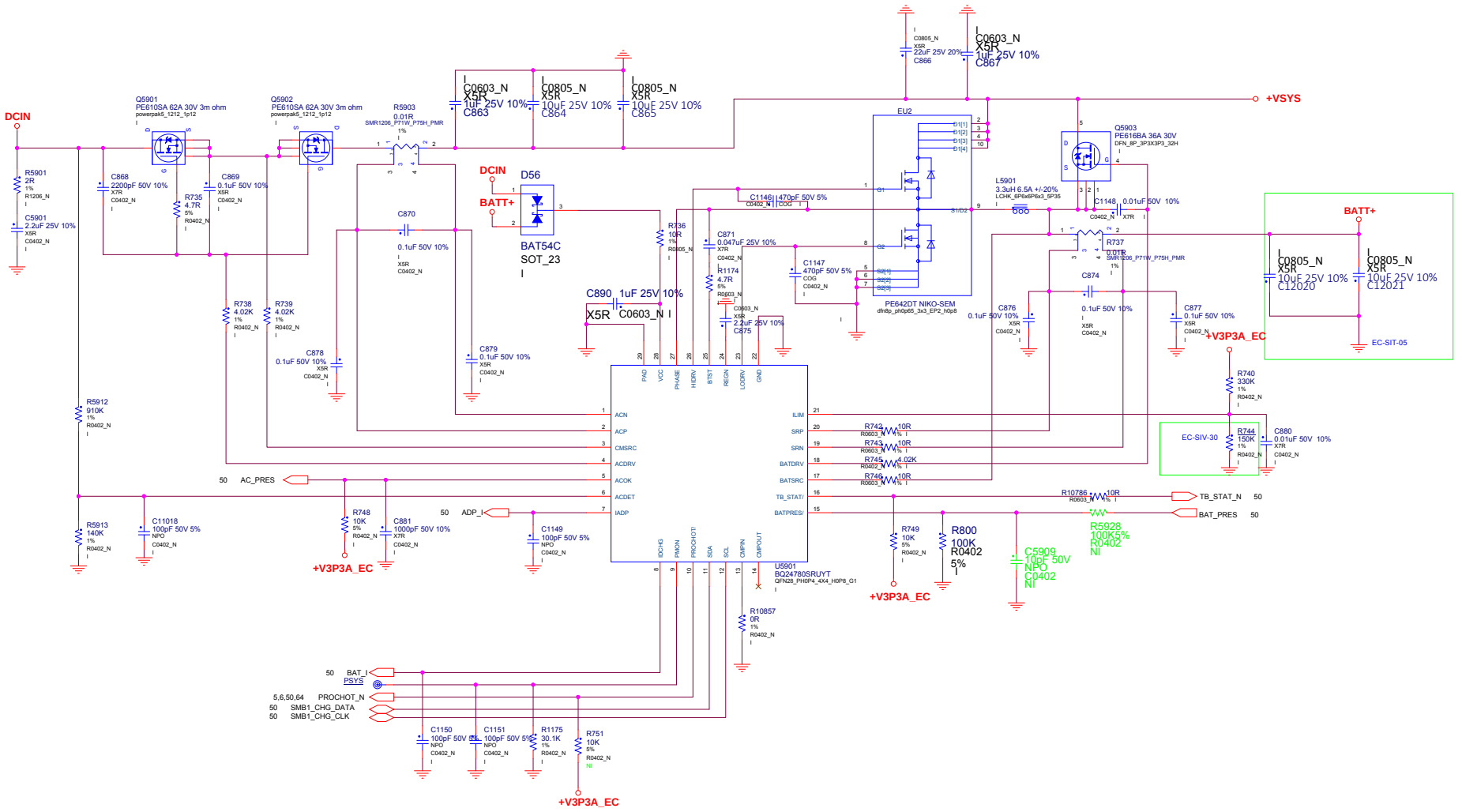


57: AC Adapter CONNECTOR



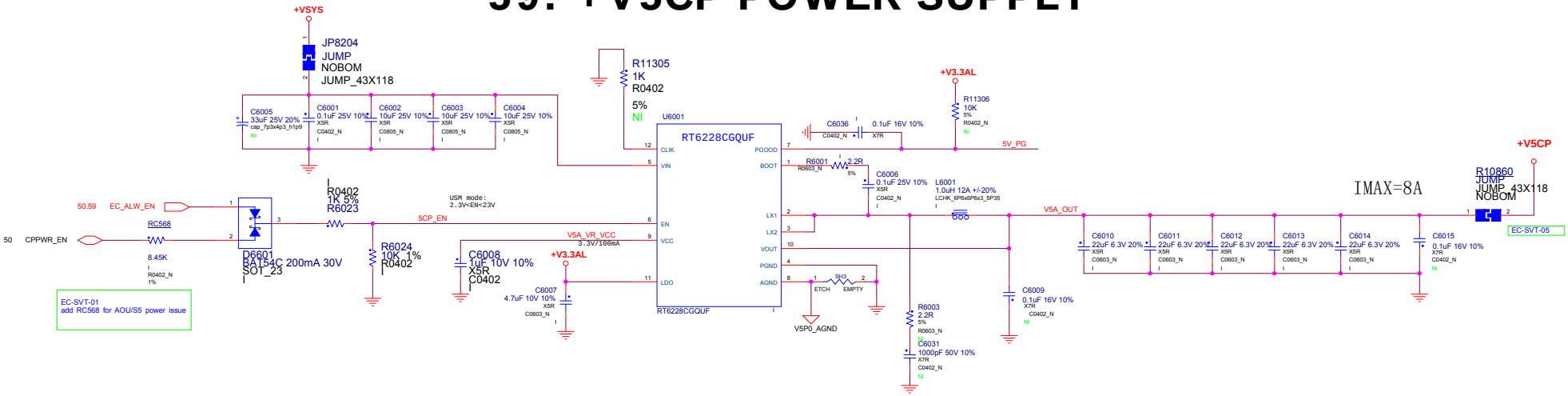
3nod三诺	Project: 330S	
	Engineer: GGS	
Size: C	Title: BATT CONN DC-IN	Rev: V01
Date: Monday, January 08, 2018	Sheet 57 of 81	

58: BATTERY CHARGER

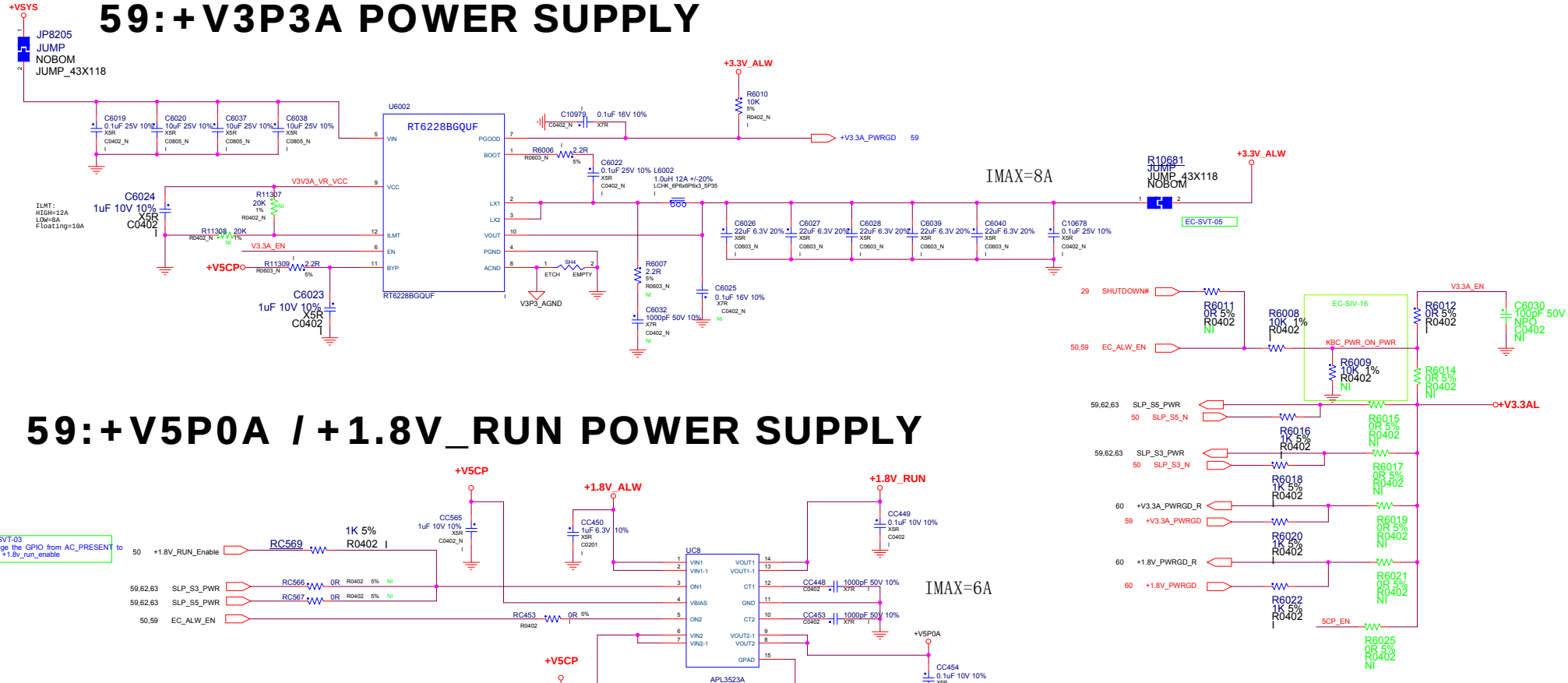


3nod三诺	Project: 330S	
	Engineer: GGS	
Size: C	Title: CHARGER	Rev: V01
Date: Monday, January 08, 2018	Sheet 58 of 81	

59: +V5CP POWER SUPPLY



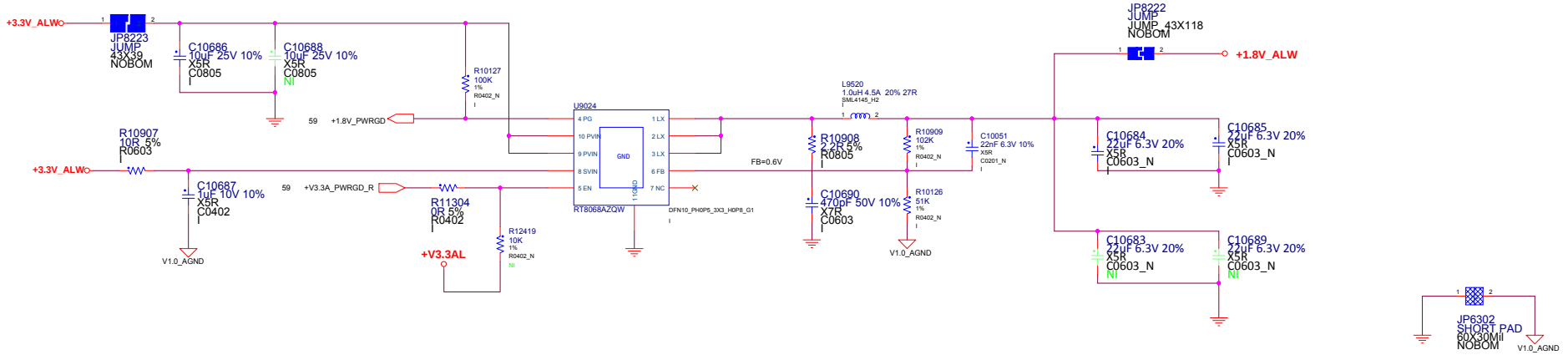
59:+V3P3A POWER SUPPLY



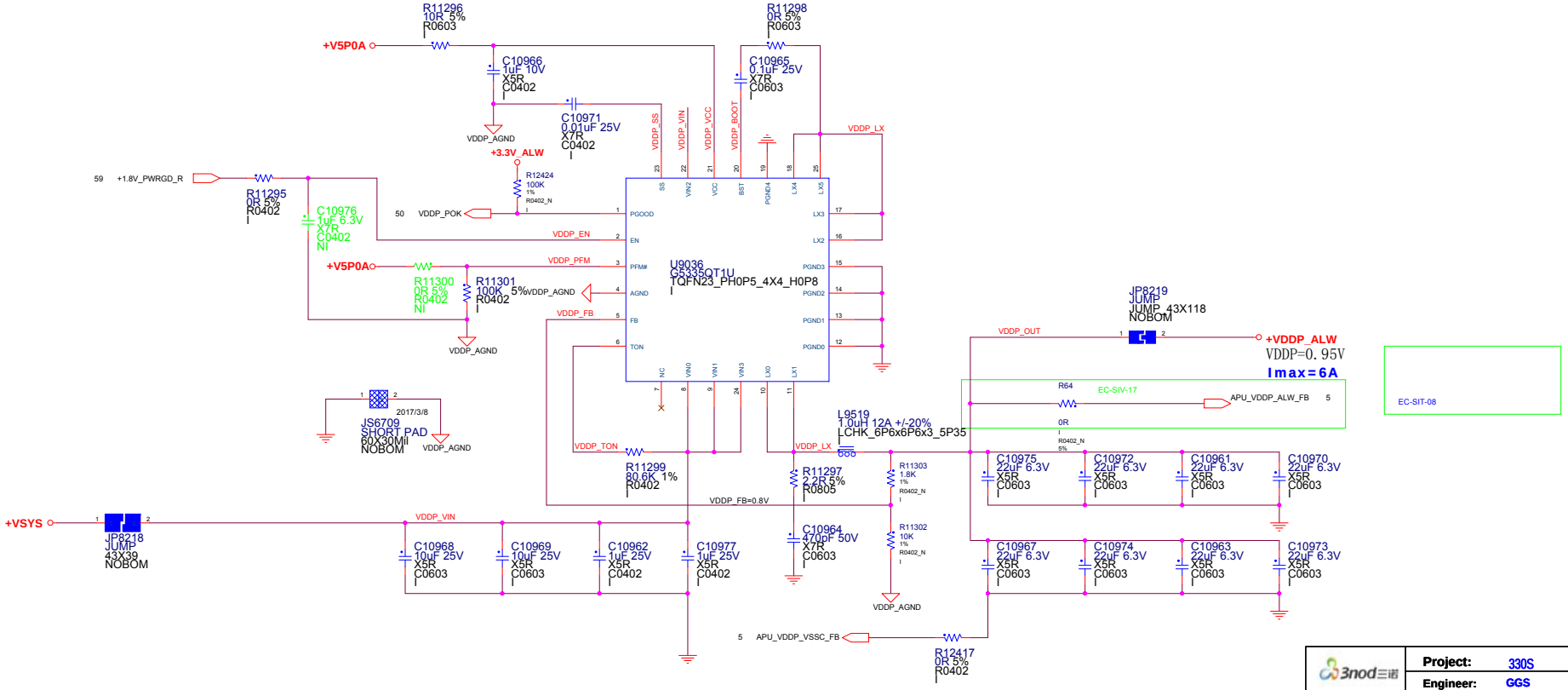
59:+V5P0A / +1.8V_RUN POWER SUPPLY

3nod三诺	Project: 330S		
	Engineer: GGS		
Size C	Title: +V5P0A / +V3P3A		Rev V01
Date: Friday, April 13, 2018	Sheet 59 of 81		

60:+1.8V_ALWPOWER SUPPLY

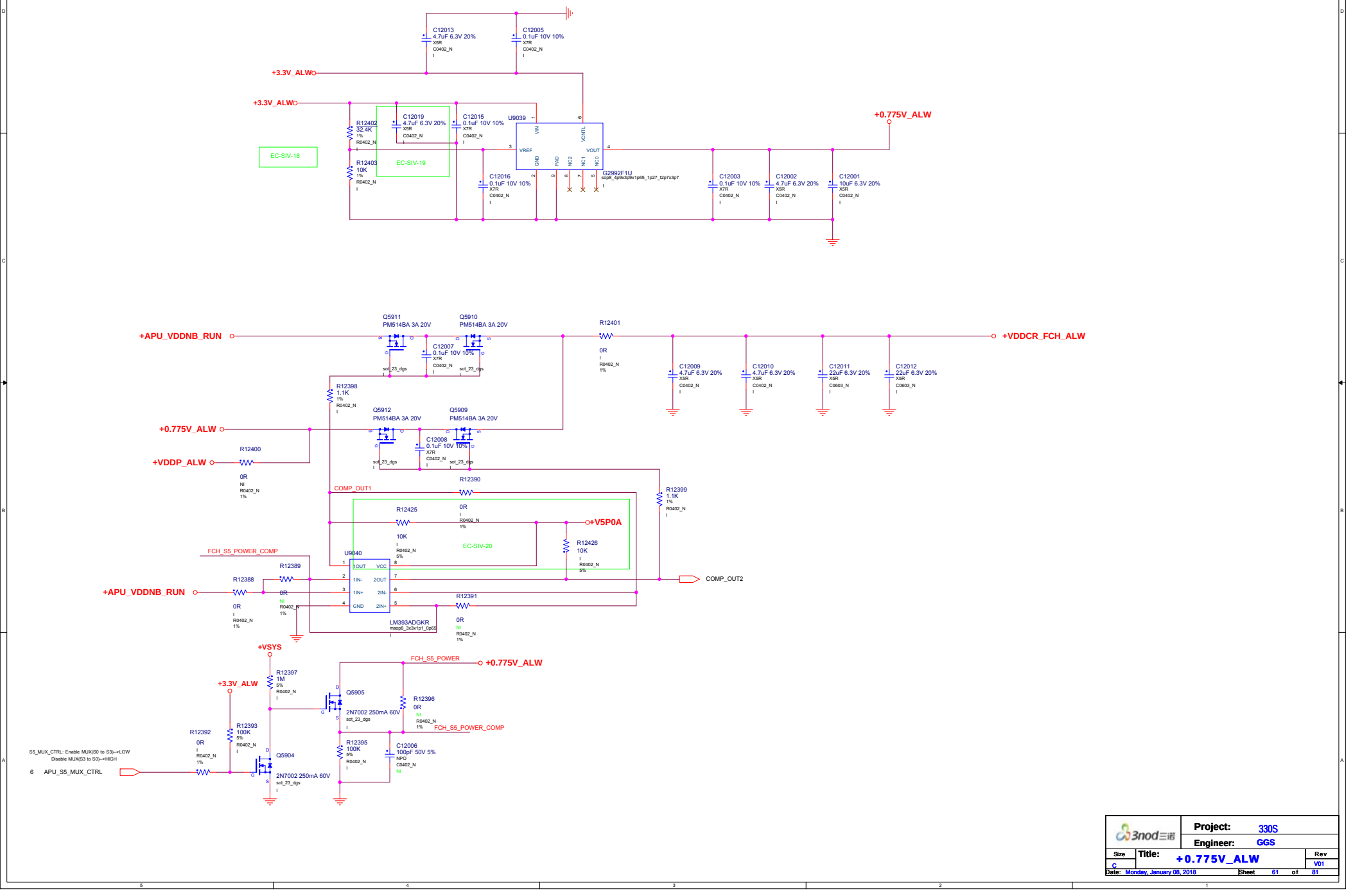


60:VDDP POWER SUPPLY



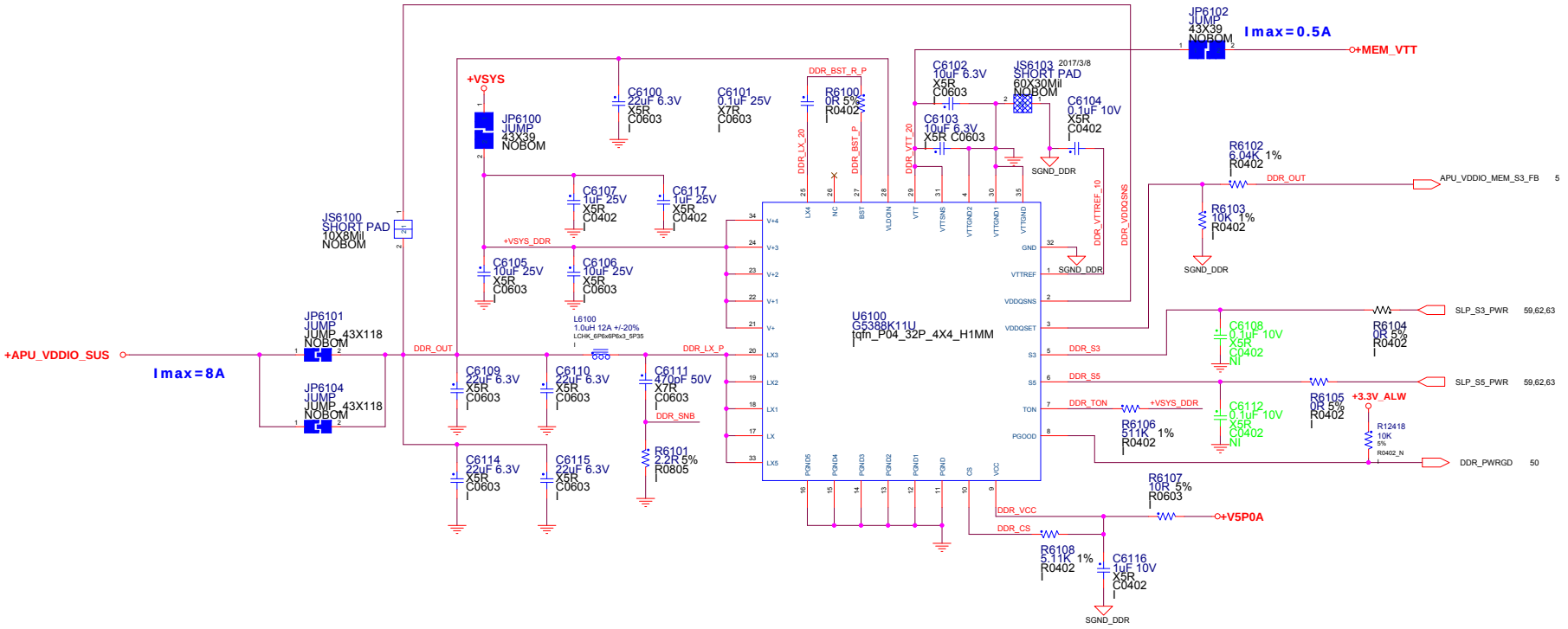
3nod三诺	Project: 330S	
	Engineer: GGS	
Size: C	Title: +1.8V_PRIM	Rev: V01
Date: Friday, March 02, 2018	Sheet 60 of 81	

61: +0.775V_ALW POWER SUPPLY

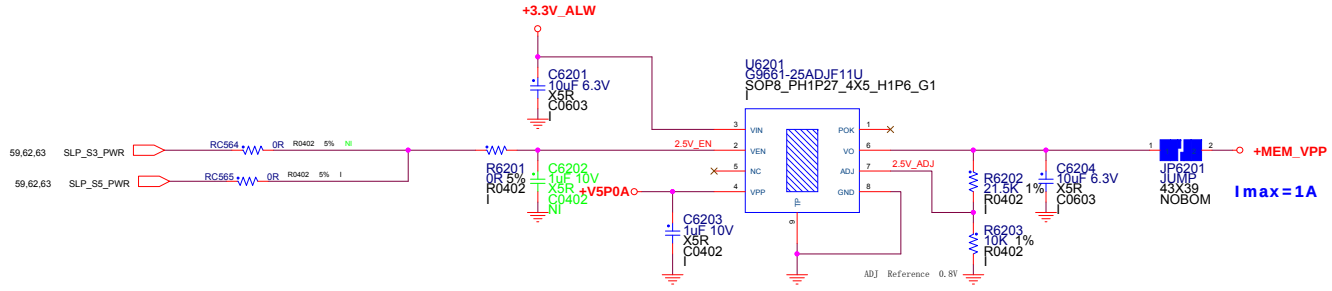


3nod三诺	Project: 330S	
	Engineer: GGS	
Size: C	Title: +0.775V_ALW	Rev: V01
Date: Monday, January 08, 2018	Sheet 61 of 81	

62: DDR POWER SUPPLY

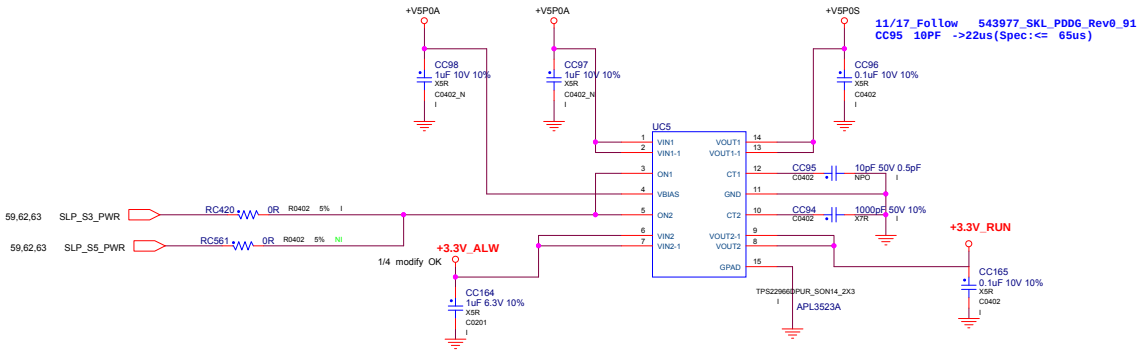


62 +MEM_VPP POWER SUPPLY

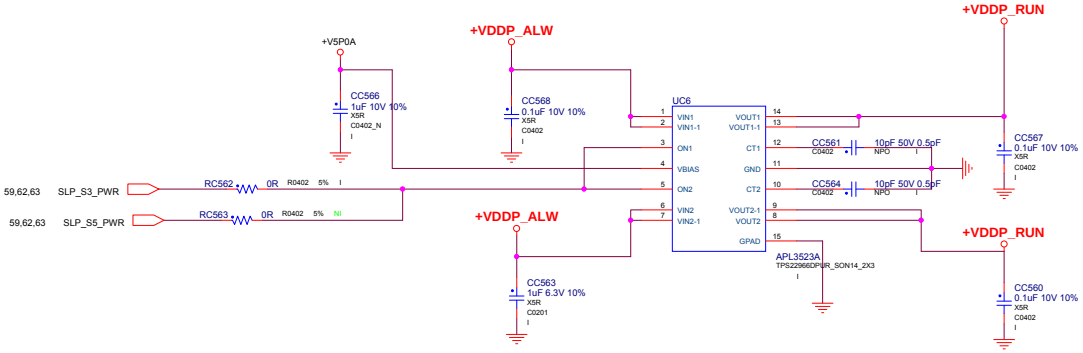


3nod三诺	Project: 330S		
	Engineer: GGS		
Size: C	Title: DDR Power		Rev: V01
Date: Friday, February 02, 2018	Sheet 62 of 81		

62: +V5P0S/+3.3V_RUN POWER SUPPLY

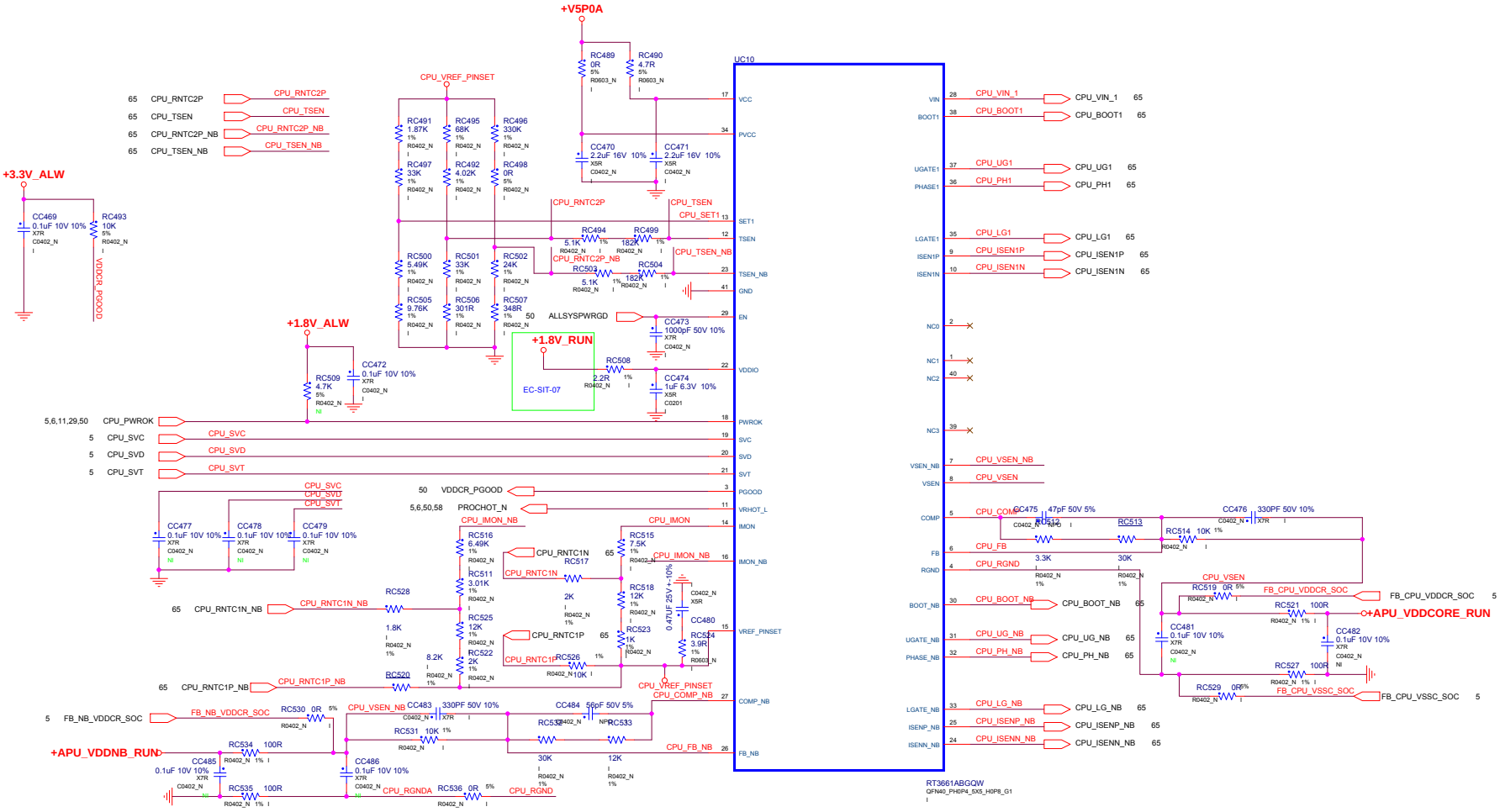


62: +VDDP_RUN POWER SUPPLY

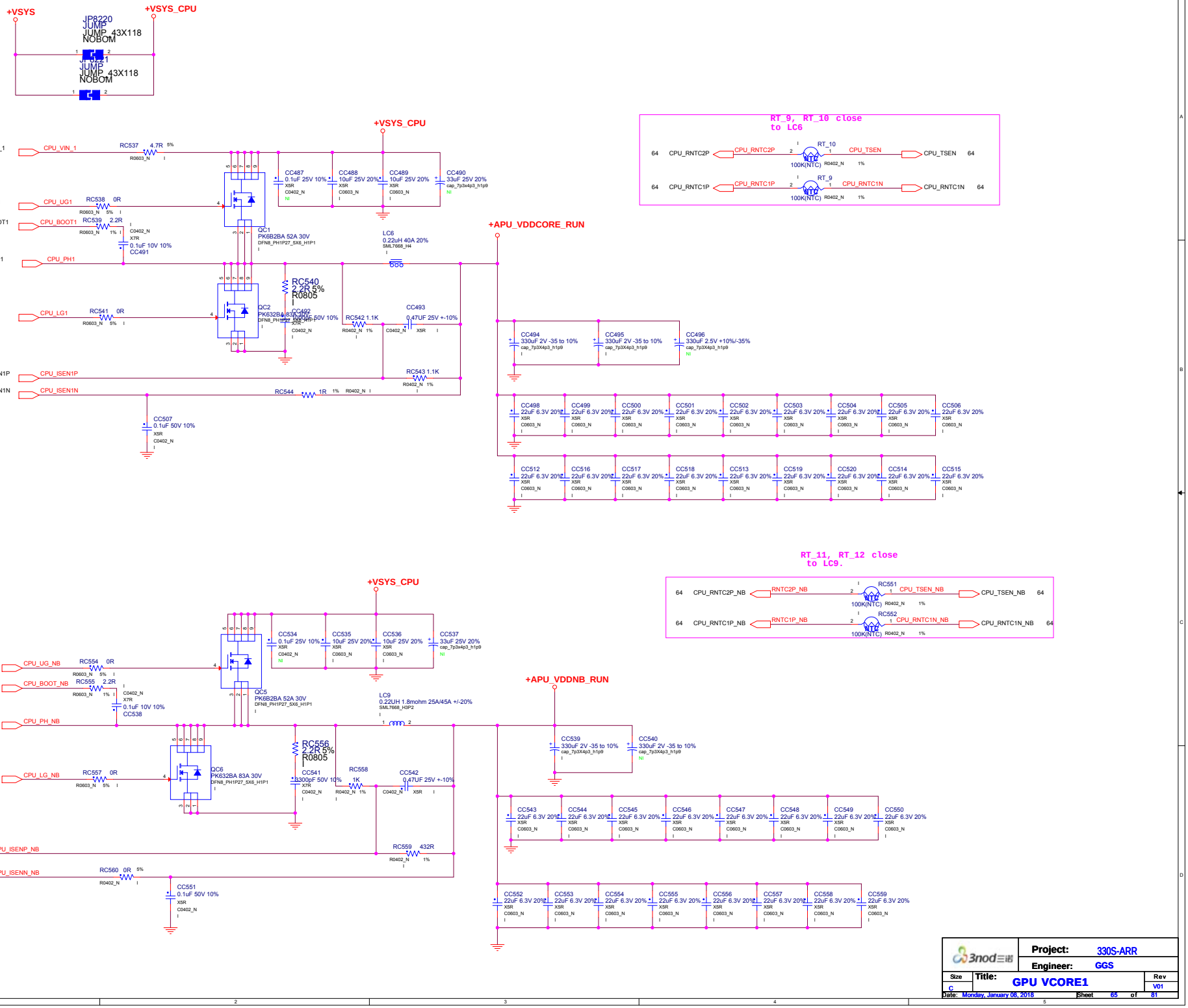


3nod三诺	Project: 330S-14&15	
	Engineer: Ken	
Size: C	Title: Power	Rev: V01
Date: Thursday, April 12, 2018	Sheet 63 of 81	

64: CPU POWER



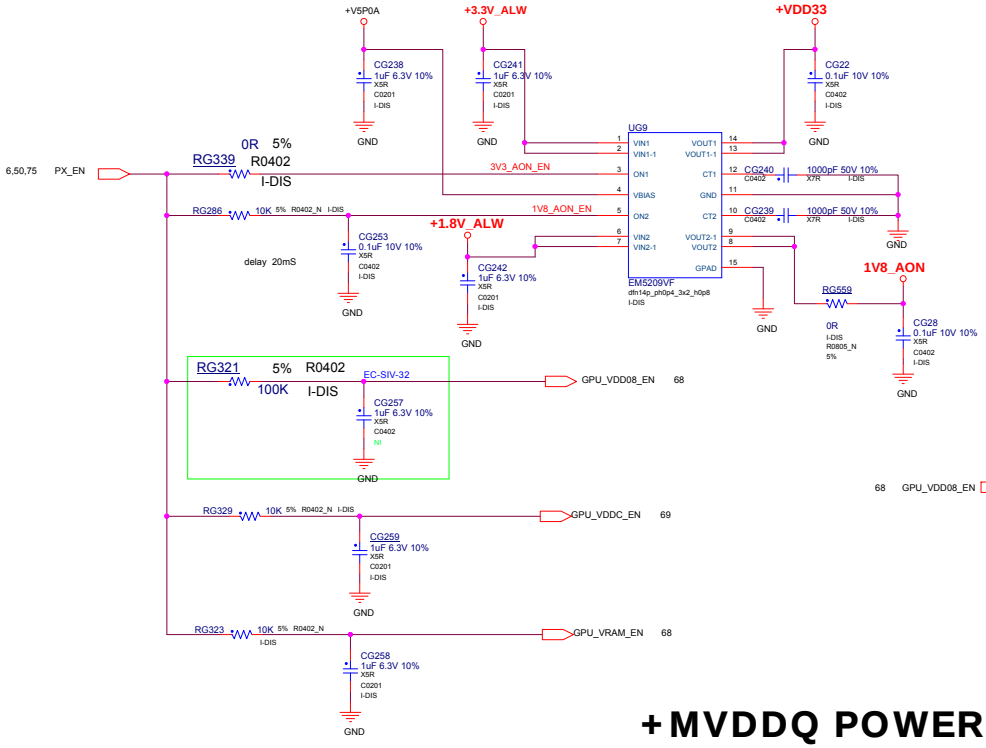
3nod三诺	Project:	330S-ARR	
	Engineer:	GGS	
Size: C	Title:	GPU VCORE1	Rev: V01
Date: Friday, April 13, 2018	Sheet	64 of 81	


+VSYS
+VSYS_CPU
JP8220
JUMP
JUMP_43X118
NOBOM
JP8221
JUMP
JUMP_43X118
NOBOM
+VSYS_CPU
CPU_VIN_1
RC537 4.7R 5%
CC487 0.1uF 25V 10%
CC488 10uF 25V 20%
CC489 10uF 25V 20%
CC490 33uF 25V 20%
CPU_UG1
RC538 0R
CPU_BOOT1
RC539 2.2R
CC491 0.1uF 10V 10%
QC1 PK6B2BA 52A 30V
DFN8_PH1P27_5X6_H1P1
LC6 0.22uH 40A 20%
SML7668_H4
+APU_VDDCORE_RUN
CPU_PH1
RC540 2.2R 5% R0805
CPU_LG1
RC541 0R
QC2 PK632BA 83A 30V
CC492 3300pF 50V 10%
RC542 1.1K
CC493 0.47UF 25V +-10%
CC494 330uF 2V -35 to 10%
CC495 330uF 2V -35 to 10%
CC496 330uF 2.5V +10%/-35%
CPU_ISEN1P
CPU_ISEN1N
RC543 1.1K
RC544 1R
CC507 0.1uF 50V 10%
CC498 22uF 6.3V 20%
CC499 22uF 6.3V 20%
CC500 22uF 6.3V 20%
CC501 22uF 6.3V 20%
CC502 22uF 6.3V 20%
CC503 22uF 6.3V 20%
CC504 22uF 6.3V 20%
CC505 22uF 6.3V 20%
CC506 22uF 6.3V 20%
CC512 22uF 6.3V 20%
CC516 22uF 6.3V 20%
CC517 22uF 6.3V 20%
CC518 22uF 6.3V 20%
CC513 22uF 6.3V 20%
CC519 22uF 6.3V 20%
CC520 22uF 6.3V 20%
CC514 22uF 6.3V 20%
CC515 22uF 6.3V 20%
RT_9, RT_10 close to LC6
CPU_RNTC2P
RT_10
100K(NTC)
CPU_TSEN
CPU_RNTC1P
RT_9
CPU_RNTC1N
RT_11, RT_12 close to LC9.
RNTC2P_NB
RC551
CPU_TSEN_NB
RNTC1P_NB
RC552
CPU_RNTC1N_NB
+VSYS_CPU
CPU_UG_NB
RC554 0R
CPU_BOOT_NB
RC555 2.2R
CC538 0.1uF 10V 10%
QC5 PK682BA 52A 30V
DFN8_PH1P27_5X6_H1P1
CC534 0.1uF 25V 10%
CC535 10uF 25V 20%
CC536 10uF 25V 20%
CC537 33uF 25V 20%
LC9 0.22UH 1.8mohm 25A/45A +/-20%
SML7668_H3P2
+APU_VDDNB_RUN
CPU_PH_NB
RC556 2.2R 5% R0805
CPU_LG_NB
RC557 0R
QC6 PK632BA 83A 30V
DFN8_PH1P27_5X6_H1P1
CC541 3300pF 50V 10%
RC558 1K
CC542 0.47UF 25V +-10%
CC539 330uF 2V -35 to 10%
CC540 330uF 2V -35 to 10%
CC543 22uF 6.3V 20%
CC544 22uF 6.3V 20%
CC545 22uF 6.3V 20%
CC546 22uF 6.3V 20%
CC547 22uF 6.3V 20%
CC548 22uF 6.3V 20%
CC549 22uF 6.3V 20%
CC550 22uF 6.3V 20%
CPU_ISENP_NB
CPU_ISENN_NB
RC559 432R
RC560 0R
CC551 0.1uF 50V 10%
CC552 22uF 6.3V 20%
CC553 22uF 6.3V 20%
CC554 22uF 6.3V 20%
CC555 22uF 6.3V 20%
CC556 22uF 6.3V 20%
CC557 22uF 6.3V 20%
CC558 22uF 6.3V 20%
CC559 22uF 6.3V 20%
Project: 330S-ARR
Engineer: GGS
Size: C
Title: GPU VCORE1
Rev: V01
Date: Monday, January 08, 2018
Sheet 65 of 81

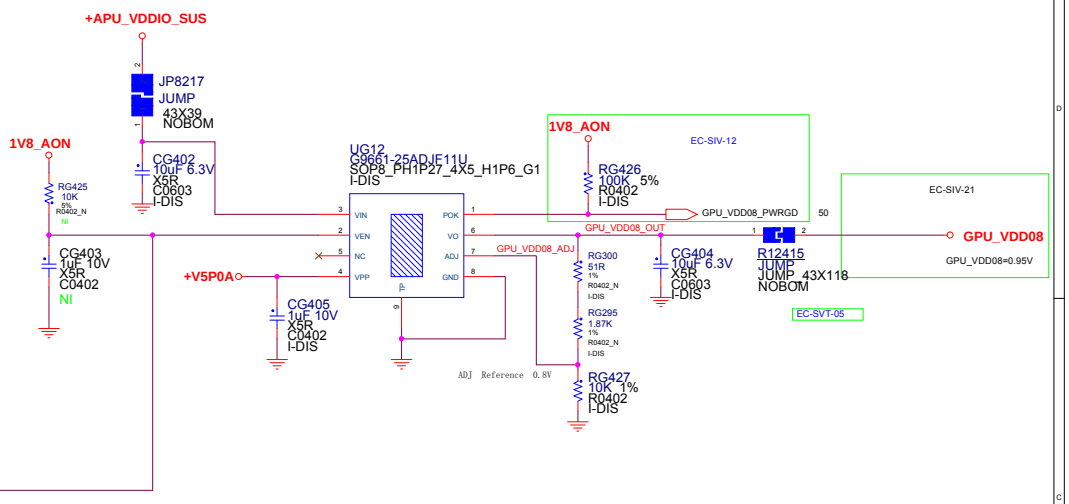
3nod三诺	Project: 330S	
	Engineer: GGS	
Size: C	Title: VDDP	Rev: V01
Date: Monday, January 08, 2018	Sheet 66 of 81	

3nod三诺	Project: 330S	
	Engineer: GGS	
Size C	Title:	Rev V01
Date: Monday, January 08, 2018	Sheet 67 of 81	

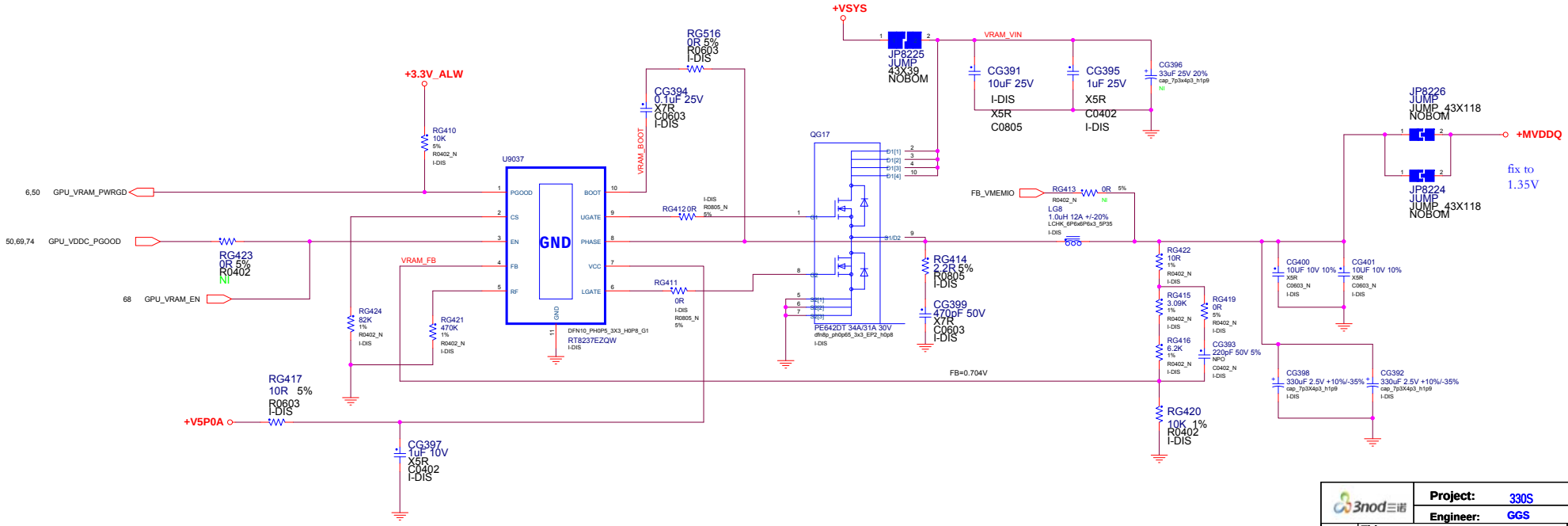
+VDD33/1V8_AON + POWER SUPPLY for GPU



GPU_VDD08 POWER SUPPLY for GPU

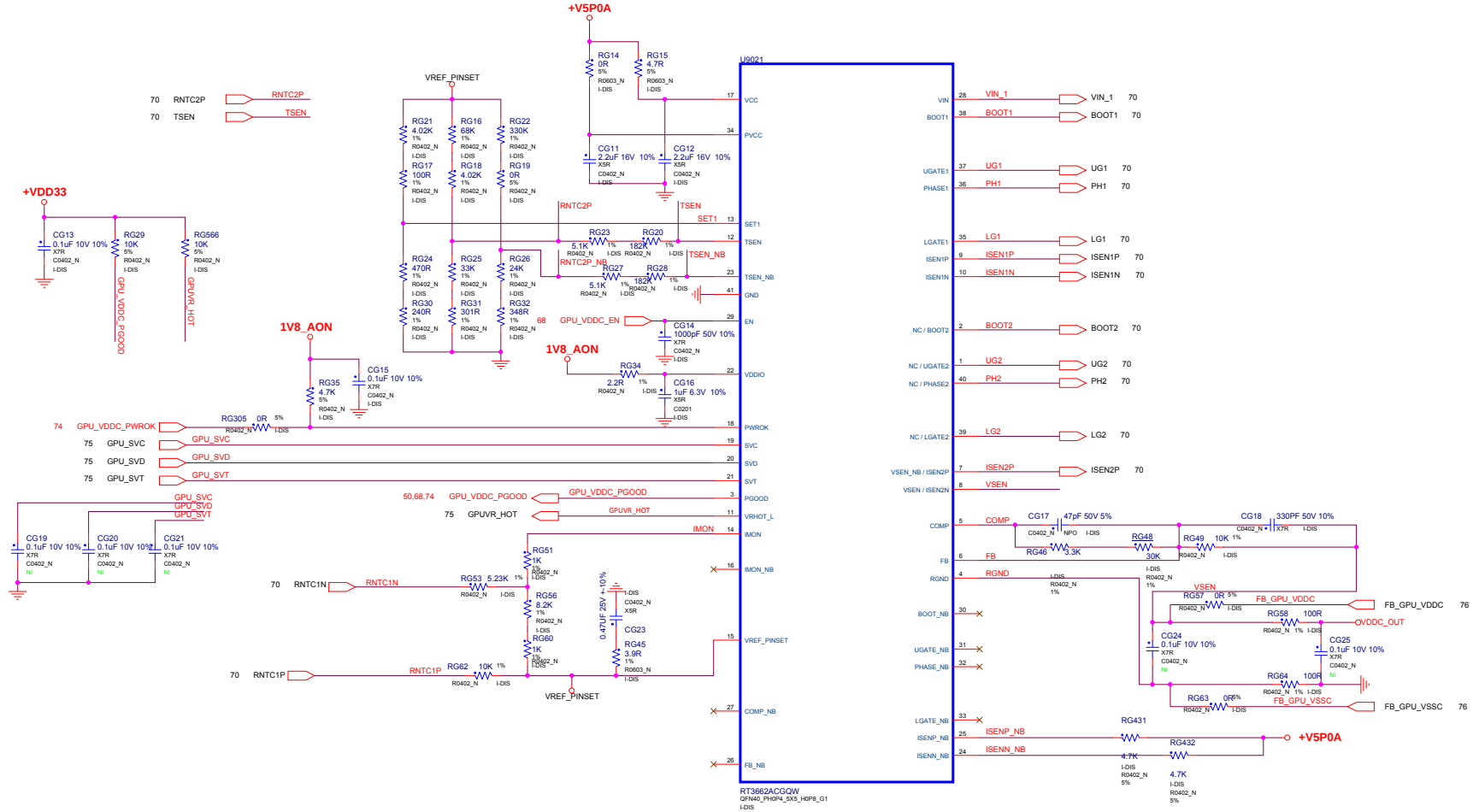


+MVDDQ POWER SUPPLY for GPU

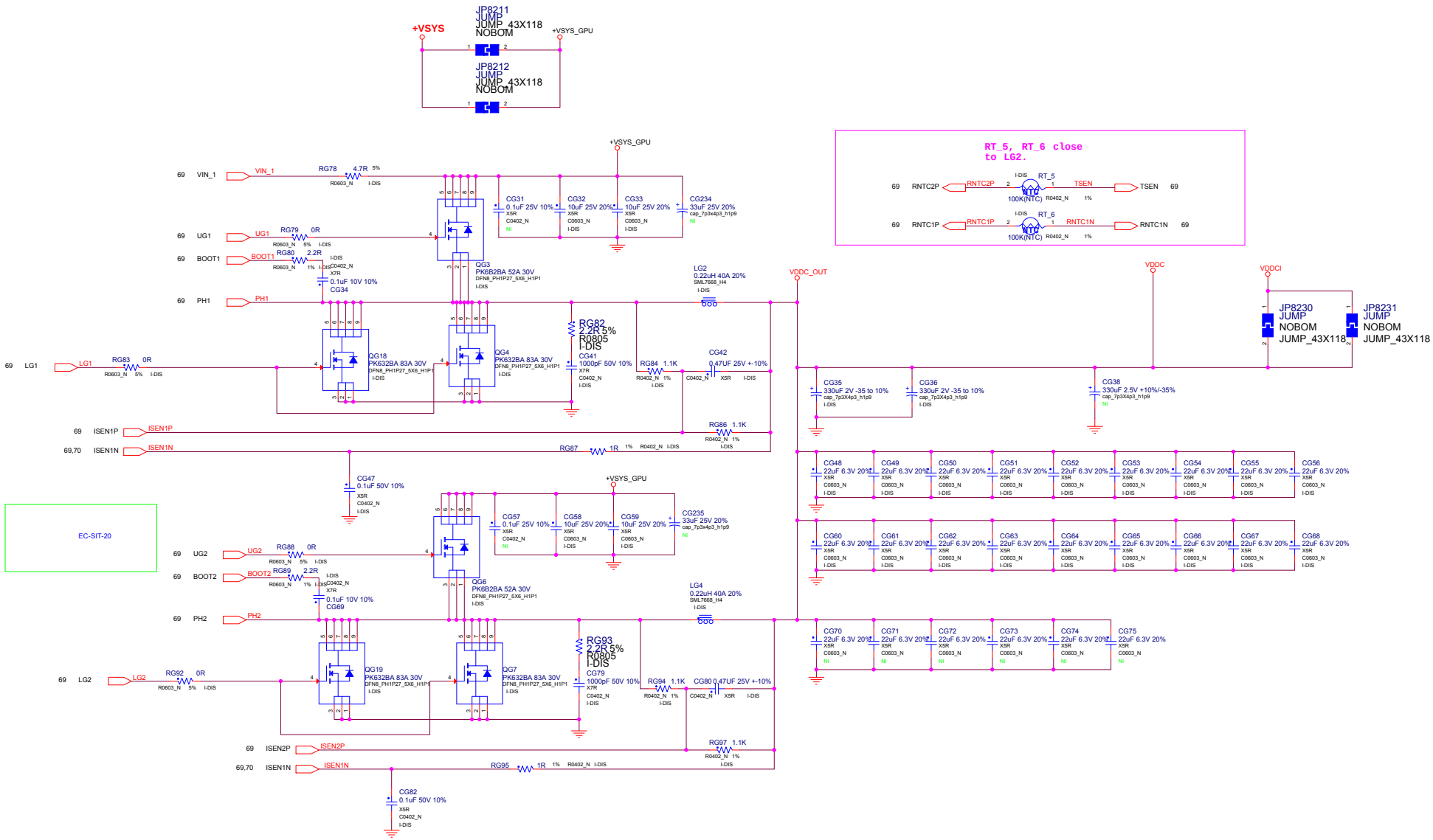


3nod三诺	Project: 330S	
	Engineer: GGS	
Size: C	Title: GPUVDD18 / VDD33 / VDD08 / VDDRAM	Rev: V01
Date: Monday, January 29, 2018	Sheet 68 of 81	

70: GPU POWER



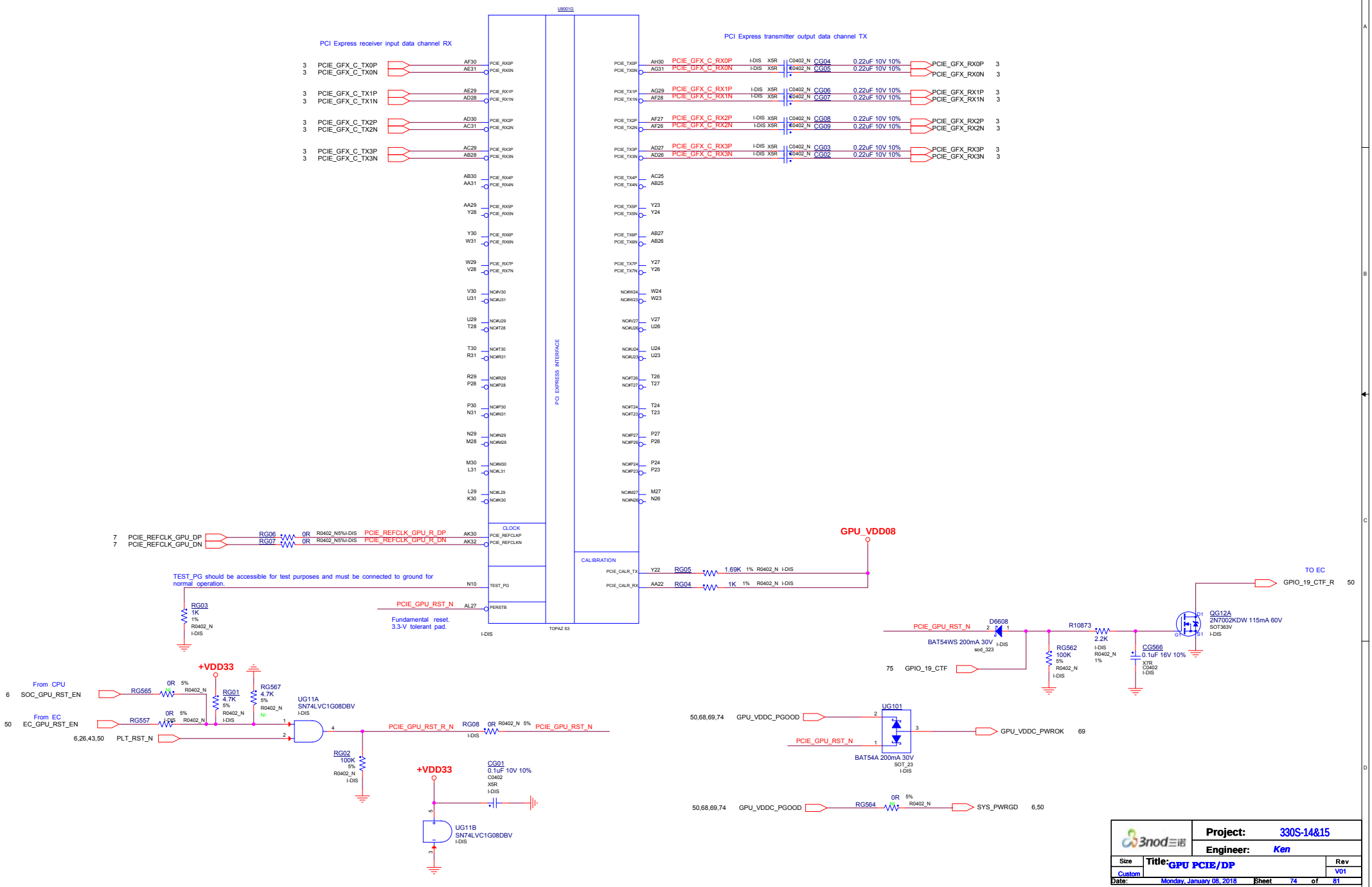
3nod三诺	Project: 330S		
	Engineer: GGS		
Size: C	Title: GPU NVVDD		Rev: V01
Date: Monday, January 29, 2018	Sheet 69 of 81		


JP8211
JUMP
JUMP_43X118
NOBOM
+VSYS
+VSYS_GPU
JP8212
JUMP
JUMP_43X118
NOBOM
RT_5, RT_6 close to LG2.
RNTC2P
RNTC1P
RT_5
RT_6
100K(NTC)
TSEN
RNTC1N
VIN_1
RG78 4.7R 5%
UG1
RG79 0R
BOOT1
RG80 2.2R
PH1
QG3 PK6B2BA 52A 30V DFN8_PH1P27_5X6_H1P1
QG4 PK632BA 83A 30V DFN8_PH1P27_5X6_H1P1
QG18 PK632BA 83A 30V DFN8_PH1P27_5X6_H1P1
LG1
RG83 0R
LG2 0.22uH 40A 20%
RG82 2.2R 5% R0805
CG41 1000pF 50V 10%
RG84 1.1K
CG42 0.47UF 25V +-10%
RG86 1.1K
RG87 1R
ISEN1P
ISEN1N
VDDC_OUT
VDDC
VDDCI
JP8230 JUMP NOBOM JUMP_43X118
JP8231 JUMP NOBOM JUMP_43X118
CG35 330uF 2V -35 to 10%
CG36 330uF 2V -35 to 10%
CG38 330uF 2.5V +10%/-35%
CG48 CG49 CG50 CG51 CG52 CG53 CG54 CG55 CG56 22uF 6.3V 20%
CG60 CG61 CG62 CG63 CG64 CG65 CG66 CG67 CG68 22uF 6.3V 20%
CG70 CG71 CG72 CG73 CG74 CG75 22uF 6.3V 20%
EC-SIT-20
UG2
RG88 0R
BOOT2
RG89 2.2R
PH2
QG6 PK6B2BA 52A 30V DFN8_PH1P27_5X6_H1P1
QG19 PK632BA 83A 30V DFN8_PH1P27_5X6_H1P1
QG7 PK632BA 83A 30V DFN8_PH1P27_5X6_H1P1
LG4 0.22uH 40A 20%
RG93 2.2R 5% R0805
CG79 1000pF 50V 10%
RG94 1.1K
CG80 0.47UF 25V +-10%
RG97 1.1K
RG95 1R
ISEN2P
CG82 0.1uF 50V 10%
CG47 0.1uF 50V 10%
CG69 0.1uF 10V 10%
CG34 0.1uF 10V 10%
CG31 CG32 CG33 CG234 CG57 CG58 CG59 CG235
0.1uF 25V 10% 10uF 25V 20% 33uF 25V 20%
RG92 0R
RG89 2.2R
RG88 0R
Project: 330S
Engineer: GGS
Title: GPU NVDD
Size: C
Rev: V01
Date: Monday, January 08, 2018
Sheet 70 of 81

3nod三诺	Project:	330S-14&15
	Engineer:	Luffy
Size: C	Title:	VDDCI
		Rev: V01
Date: Monday, January 08, 2018	Sheet 71 of 81	

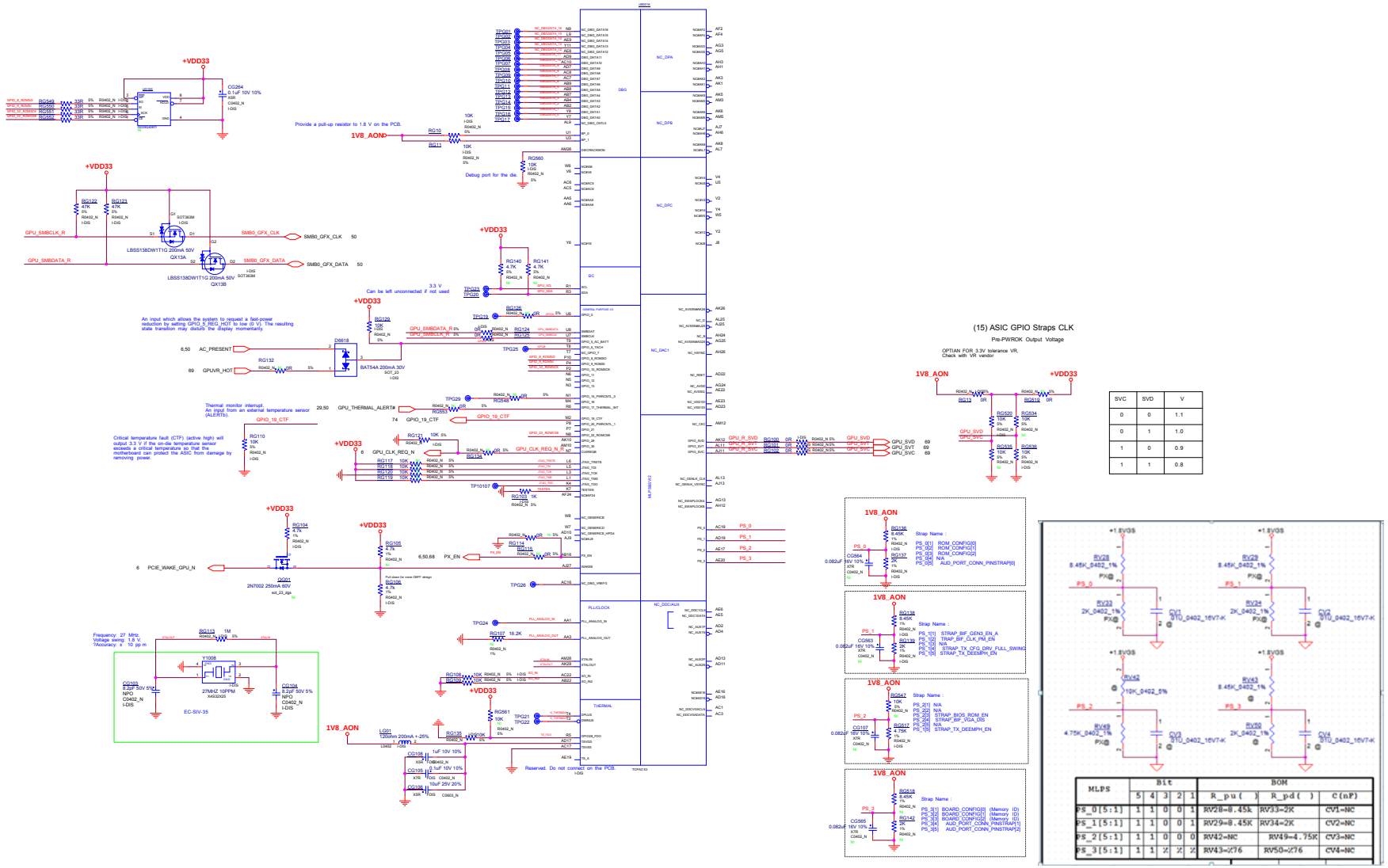
3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: C	Title: VDDCI	Rev: V01
Date: Monday, January 08, 2018	Sheet 72 of 81	

GPU/PCIE



Project:	330S-14&15	
Engineer:	Ken	
Size: Custom	Title: GPU PCIE/DP	Rev: V01
Date: Monday, January 08, 2018	Sheet 74 of 81	

GPU/MSIC



(15) ASIC GPIO Straps CLK

Pre-PWROK Output Voltage

OPTIAN FOR 3.3V tolerance VR.
Check with VR vendor

SVC	SVD	V
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

MLPS	Bit					BOM		
	5	4	3	2	1	R_pu( )	R_pd( )	C(nF)
PS_0[5:1]	1	1	0	0	1	RV28=8.45k	RV33=2K	CV1=NC
PS_1[5:1]	1	1	0	0	1	RV29=8.45K	RV34=2K	CV2=NC
PS_2[5:1]	1	1	0	0	0	RV42=NC	RV49=4.75K	CV3=NC
PS_3[5:1]	1	1	Z	Z	Z	RV43=Z76	RV50=Z76	CV4=NC

3nod三诺	Project:	330S-14&15
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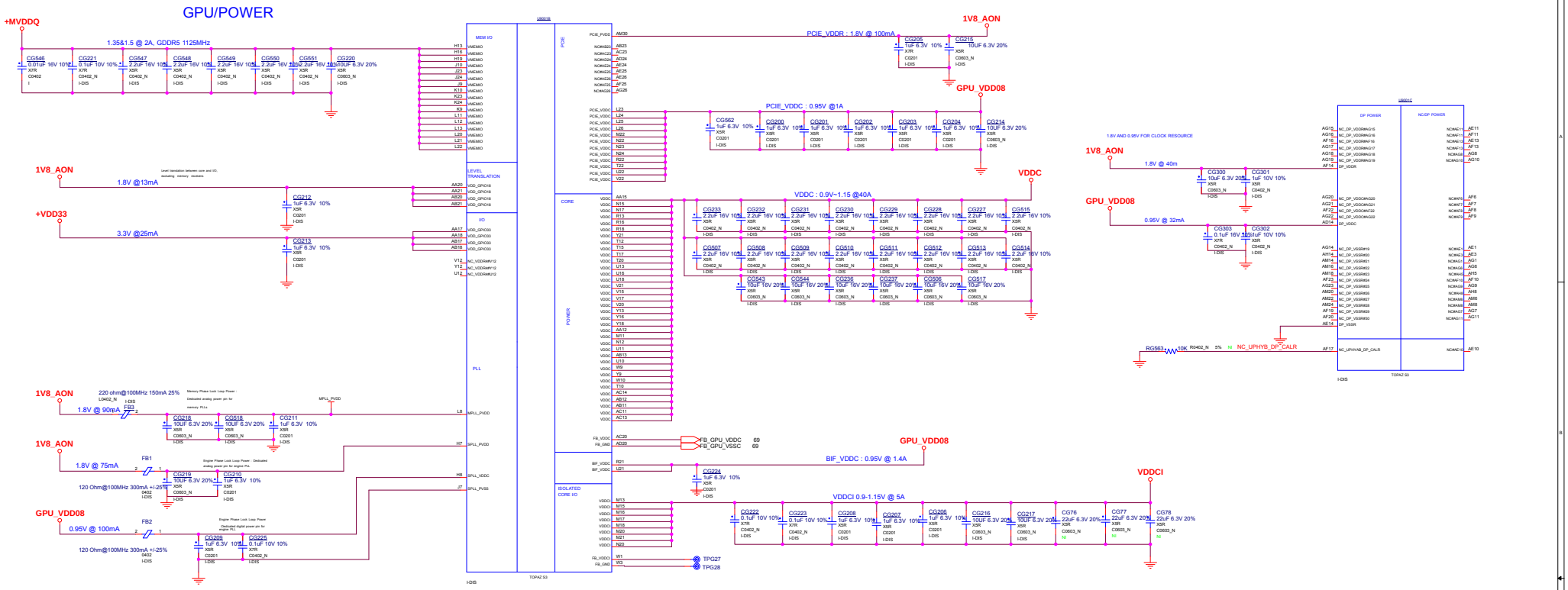

Signal Name	Nominal Set Voltage	DC Tolerance	AC Tolerance	Maximum Current
VDDC + VDDCI	"R17M-M2-50": 0.806 V to 1.225 V	VID_VDDC - I_VDDC × 1.0 mΩ ± 15 mV	Max: VID_VDDC + 50 mV Min: VID_VDDC - I_VDDC × 1.0 mΩ -30 mV	40 A (TDC)
	"R17M-M1-70": 0.806 V to 1.218 V			28 A (TDC)
VMEMIO	1.35 V or 1.50 V	±3%	±3%	2 A (TDC)

Signal Name	Nominal Set Voltage	DC Tolerance	AC Tolerance	Maximum Current
VDD_GPIO18	1.80 V	±3%	±3%	13 mA
DP_VDDC	0.95 V	±3%	±3%	Crystal Pad Digital Supply 50 mA
DP_VDDR	1.8 V	± 3%	± 3%	Crystal Pad Analog Supply 40 mA
SPLL_VDDC	0.95 V	± 3%	± 3%	100 mA
SPLL_PVDD	1.80 V	± 3%	± 3%	75 mA
MPLL_PVDD	1.80 V	± 3%	± 3%	90 mA
BIF_VDDC	0.95 V	± 3%	± 3%	0.8 A
PCIE_VDDC	0.95 V	± 3%	± 3%	1.0 A
PCIE_PVDD	1.80 V	± 3%	± 3%	100 mA
TSVDD	1.80 V	± 3%	± 3%	13 mA
VDD_GPIO33	3.30 V	± 9%	± 9%	25 mA

3nod三讯	Project:	330S-14&15
	Engineer:	Ken
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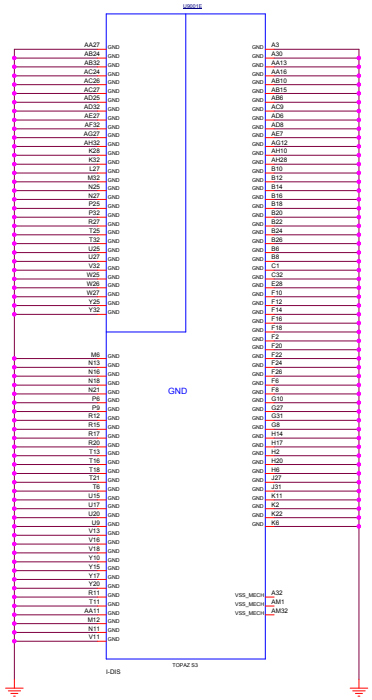
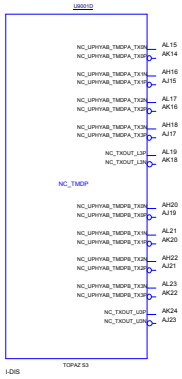
GPU/GND





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	Engineer: Ken	
Size: Custom	Title: GPU Power/GND	Rev: V01
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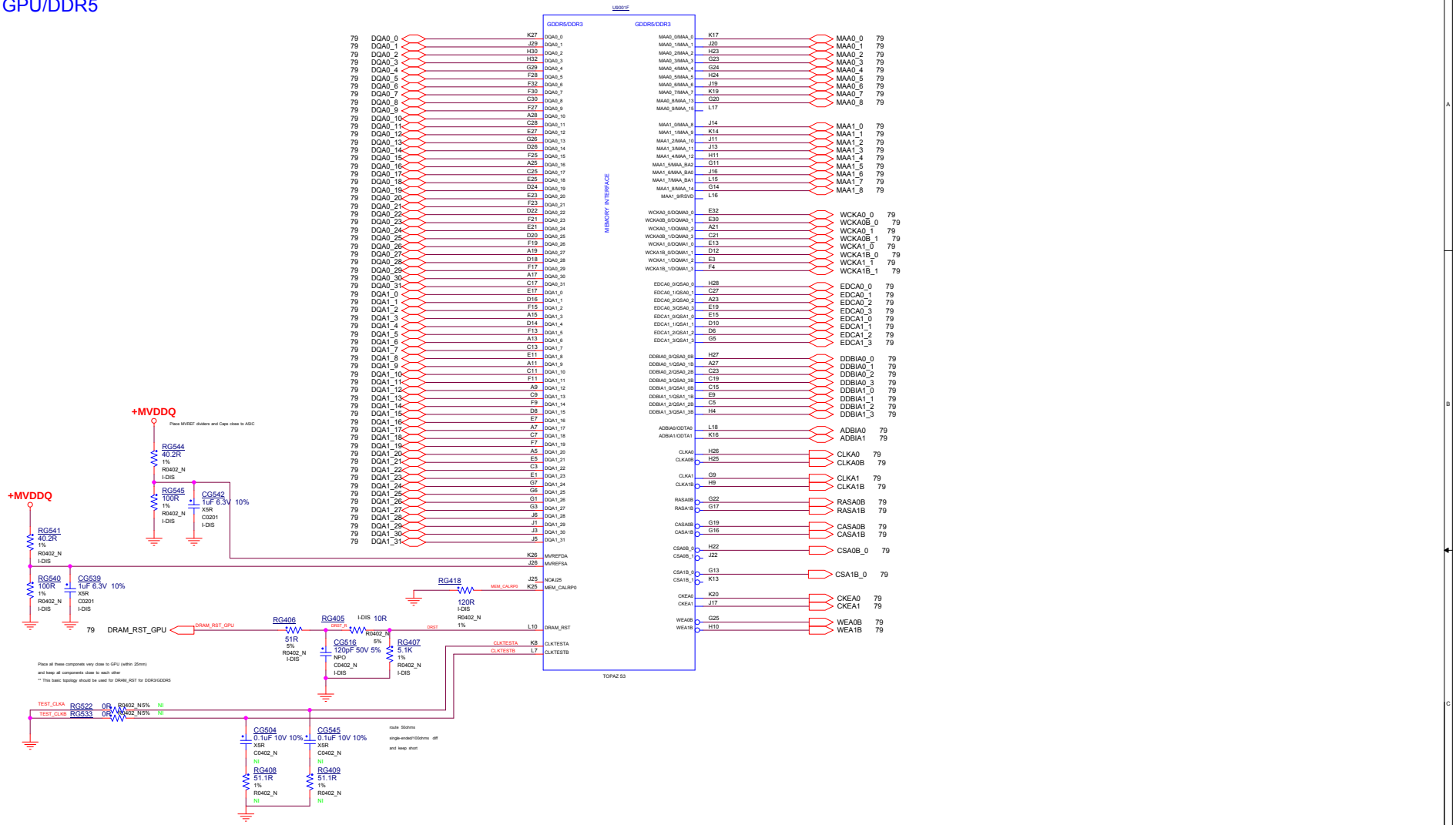
GPU/DDR5



3nod三诺	Project:	330S-14&15	
	Engineer:	Ken	
Size: C	Title:	NV _GPU MEM	Rev: V01
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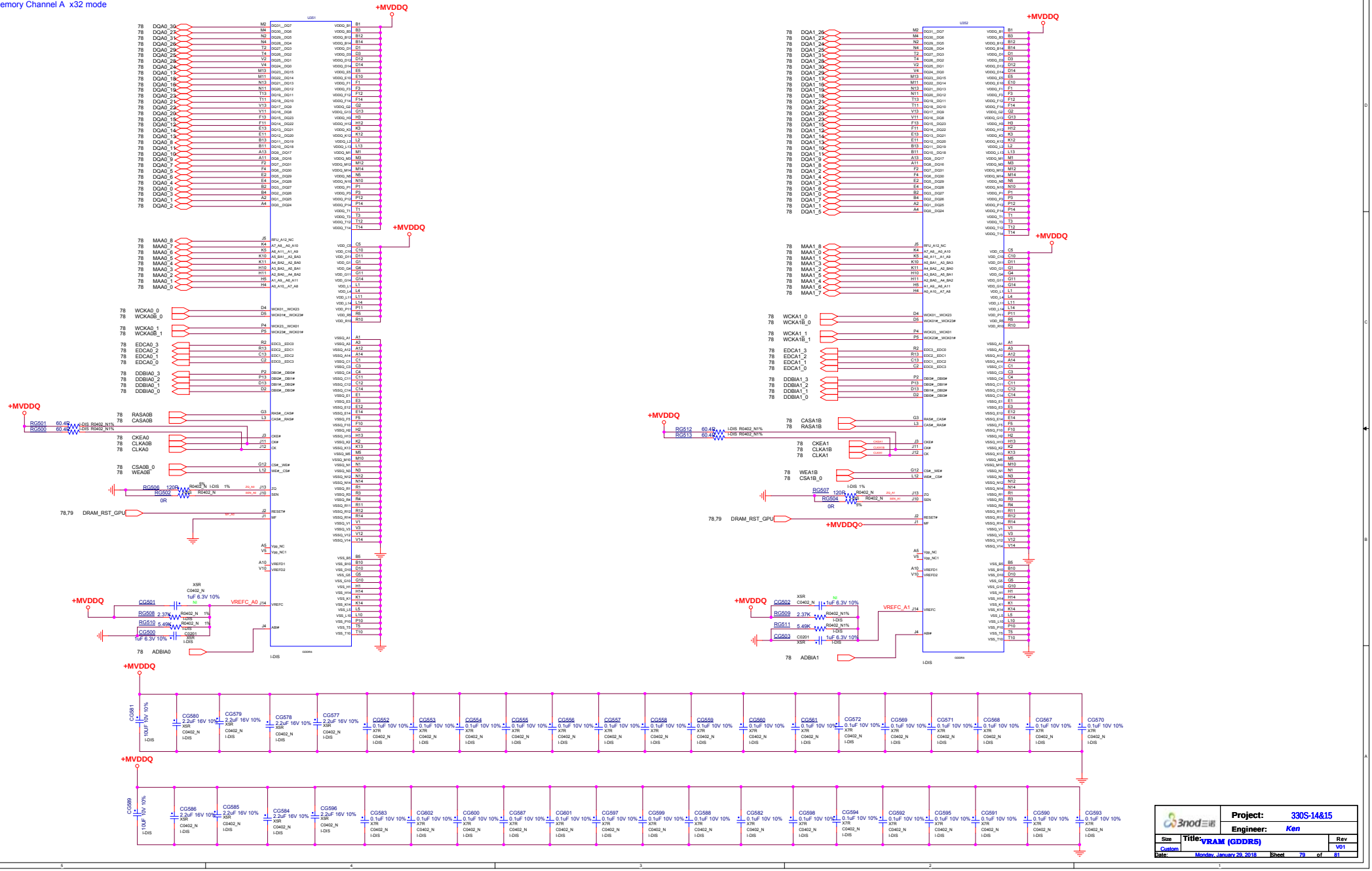
GDDR5 Memory Channel A x32 mode



3nod三诺	Project:	330S-14&15	
	Engineer:	Ken	
Size: Custom	Title:	VRAM (GDDR5)	Rev: V01
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	Engineer:	Ken
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3nod三诺	Project: 330S-14&15	
	Engineer: *Luffy*	
Size: C	Title: HW Change list	Rev: V01
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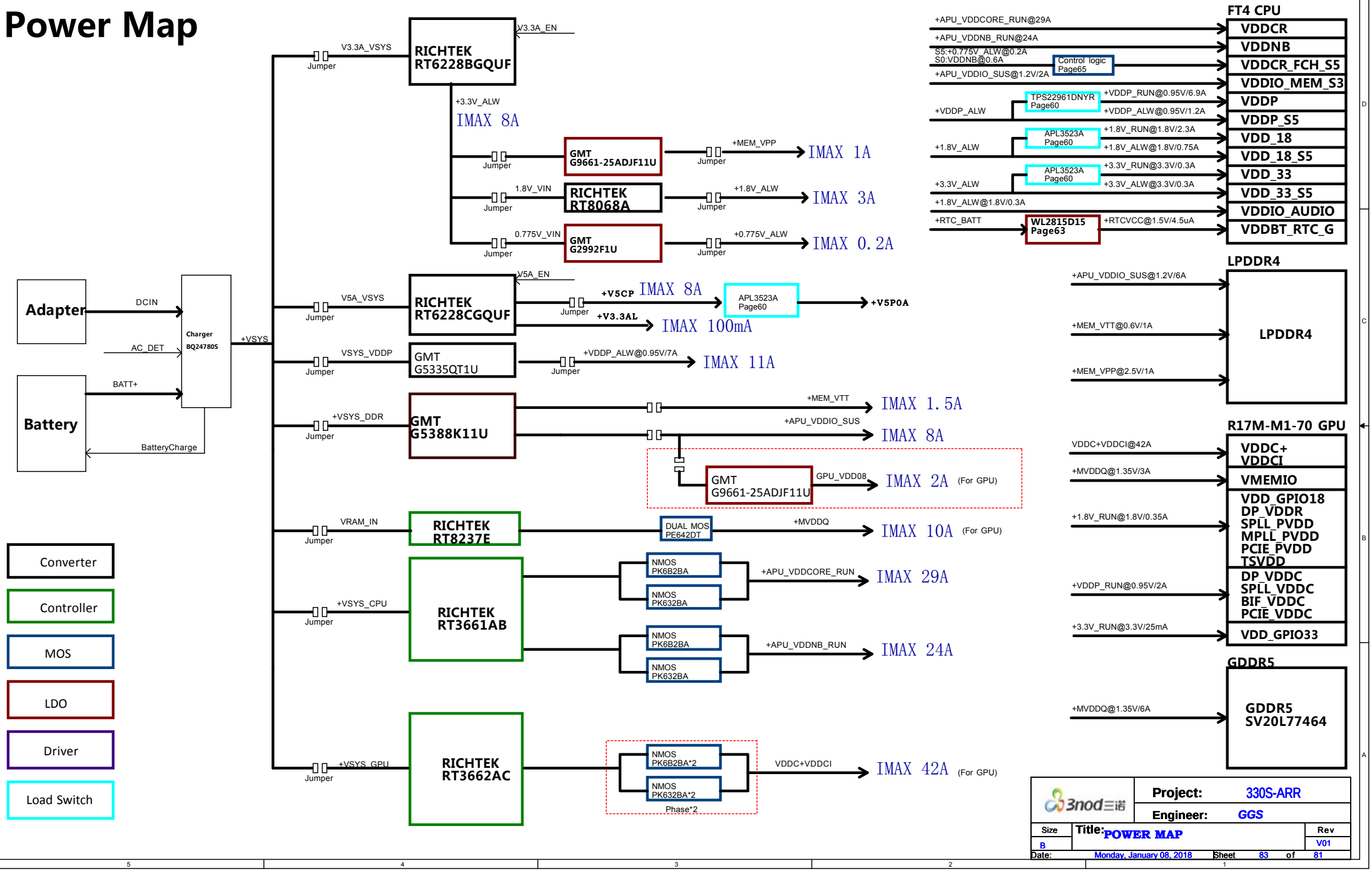
Power Map



3nod三诺	Project: 330S-ARR	
	Engineer: GGS	
Size: B	Title: POWER MAP	Rev: V01
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