GA-990FXA-UD3

Revision : 3.02

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Title: COVER SHEET

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Model Name:GA-990FXA-UD3

AM2-->AM3 Different: AE9-->AE7, H22-->H20. Extra pin:B2 AM3 socket is 938 pins. Only shift 2 pins.

Component value change history

Version: 3.02

P-Code: U98145-0

4 Layer, 4mil 50ohm +/- 15% X

Date	Version		Change Items
2011.03.17	0.1 New BOM Release.	PCB:0.1	Modify from 9M990FXA5-00-01
2011.04.13	1.0A BOM Release.	PCB:1.0	Add AMD Validation parts ,Add Thermal-Die schematic Delete AZ2025 for AUDIO
2011.04.27	1.0B BOM Release.	PCB:1.01	Remove PCB silkscreen SLI logo
2011.05.05	1.0C BOM Release.	PCB:1.01	更改 CPU RM 爲分離式
2011.05.05	1.0D BOM Release.	PCB:1.0	PCB Change to 1.0 (Silk W/SLI Logo)
2011.08.05	1.1A BOM Release.	PCB:1.1	Add Load-Line Droop control
2011.08.24	1.1B BOM Release.	PCB:1.1	modify PWM DR73 ,DR82 ,DR83 ,DR84 ISEN 196R ,轉 P-BOM
2011.09.29	1.1C BOM Release.	PCB:1.1	modify 黑色box header 印字銘板移印,字體方向也進行轉向
2012.01.02	1.1D BOM Release.	PCB:1.1	Modify LAN 8111E => 8111F
2012.02.20	1.1D ECN BOM Release.	PCB:1.1	Add mosfet second source Vishay 4+7
2012.04.02	1.1E BOM Release.	PCB:1.1	Modify USB_LAN, KB_MS_USB 料件紅色改黑色
2012.04.17	1.1F BOM Release.	PCB:1.11	Add CPU PWM MOSFET Thermal protect
2012.05.07	1.1G BOM Release.	PCB:1.11	R156 change to 2.32K for correct CPU PWM mosfet thermal range
2012.08.01	3.0A BOM Release.	PCB:3.0	Modify SIO IT8728 ,ErP 0.5W
2012.08.22	3.0B BOM Release.	PCB:3.01	Patch some PSU can't boot when ERP enable, STR issue
2012.10.12	3.0C P-BOM Release.	PCB:3.02	Remove EES 文字面 ,Modify Ultra Durable & Revision 文字面
2012.11.15	3.0C ECN BOM Release.	PCB:3.02	移除未上件 PCB 廠家 (全成信 文印不良)

Circuit or PCB layout change for next version

Date	Version	Reason
2011.03.16	0.1 Gerber-out	Modify from GA-990FXA-UD5 Rev 0.1
2011.04.12	1.0 Gerber-out	Add AMD Validation parts ,Add Thermal-Die schematic
2011.04.26	1.01 Gerber-out	Remove PCB silkscreen SLI logo
2011.08.04	1.1 Gerber-out	Add Load-Line Droop control
2012.04.16	1.11 Gerber-out	Add CPU PWM MOSFET Thermal protect
2012.07.31	3.0 Gerber-out	Modify SIO IT8728 ,ErP 0.5W
2012.08.21	3.01 Gerber-out	Patch some PSU can't boot when ERP enable, STR issue
2012.10.11	3.02 Gerber-out	Remove EES 文字面 ,Modify Ultra Durable & Revision 文字面

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Title: BOM & PCB HISTORY

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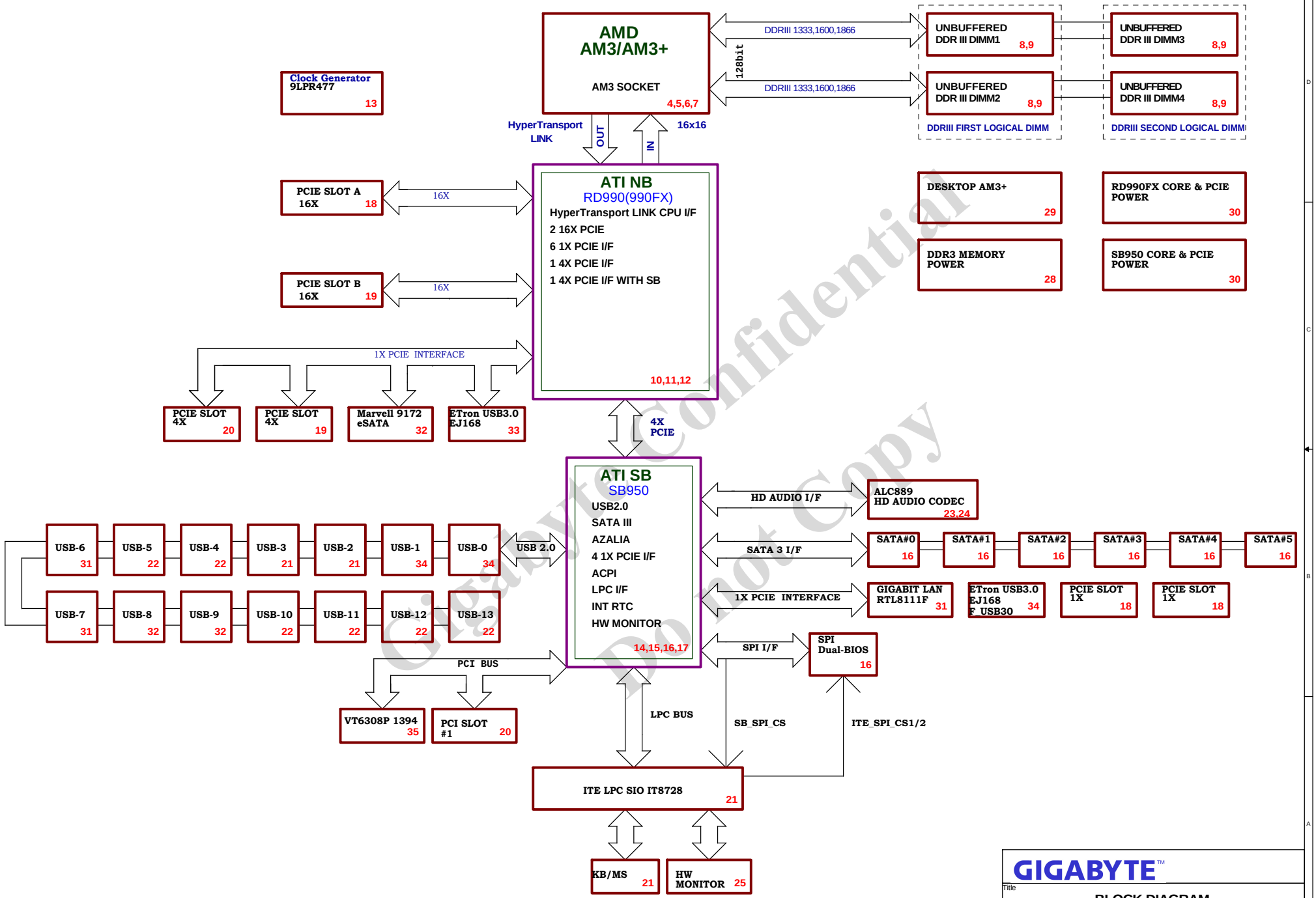

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Title: BLOCK DIAGRAM		
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L0_CADIN_L[0..15] L0_CADIN_L[0..15] 10
L0_CADIN_H[0..15] L0_CADIN_H[0..15] 10
L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] 10
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] 10

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPUA

HYPERTRANSPORT

10 L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1 10
10 L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1 10
10 L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0 10
10 L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0 10
10 L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1 10
10 L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1 10
10 L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0 10
10 L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0 10
	L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15	
	L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15	
	L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14	
	L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14	
	L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13	
	L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13	
	L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12	
	L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12	
	L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AF6	L0_CADOUT_H11	
	L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AF6	L0_CADOUT_L11	
	L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF5	L0_CADOUT_H10	
	L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10	
	L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9	
	L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9	
	L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8	
	L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8	
	L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7	
	L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7	
	L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6	
	L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6	
	L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5	
	L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5	
	L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4	
	L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4	
	L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3	
	L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3	
	L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2	
	L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2	
	L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1	
	L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1	
	L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0	
	L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0	

CPU-SK/941AM3/S/GF/[10SC1-A01942-01R_10SC1-A01942-02R]

VCORE
AC1 100P/4/NPO/50V/J/X
AC2 100P/4/NPO/50V/J/X
AC3 100P/4/NPO/50V/J/X
HT_BUS Vcore use

COUPON1 COUPON1 1 2 COUPON/X VCC
COUPON2 COUPON2 1 2 COUPON/X

K1 K1_ICT/X
K2 K1_ICT/X
K3 K1_ICT/X
K4 K1_ICT/X
K5 K1_ICT/X
K6 K1_ICT/X

M2CPU
AM3RM/SC/BL/MB/[12KRC-04K812-31R]

MH3 HOLE_3/X
MH9 HOLE_3/X
MH8 HOLE_3/X
MH1 HOLE_3/X
MH2 HOLE_3/X
MH4 HOLE_3/X
MH7 HOLE_3/X
MH5 HOLE_3/X
MH6 HOLE_3/X

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Title: COVER SHEET

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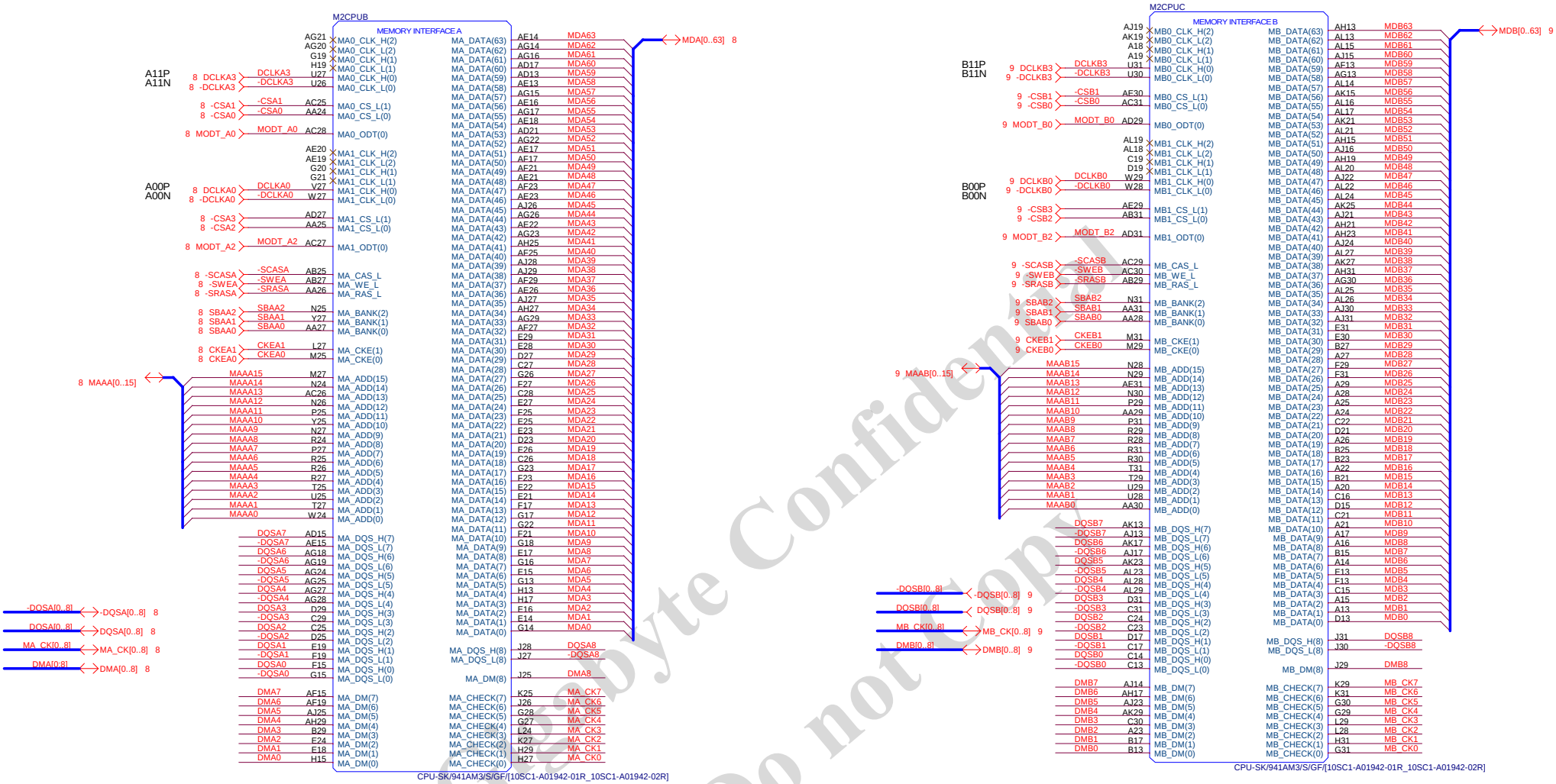

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SB600 CPU_PWR / DDR18V

DDR15V

-CPURST — AR1 300/4

-LDT_STOP — AR2 300/4

AC4 150P/4/NPO/50V/J/X

-CPURST

AC5 100P/4/NPO/50V/J

2.5V/0.5A

VDDA25

ABC1 4.7u/6X5R/6.3V/K

ABC2 3.3n/4/X7R/50V/K

ABC3 0.22U/6/X7R/16V/K

3.9n/4/X7R/50V/K

13 CPUCLK0_H — CPUCLK0_H — AC6 — CLKIN_H

13 CPUCLK0_L — CPUCLK0_L — AC7 — AR3 169/4/1 — CLKIN_L

3.9n/4/X7R/50V/K

11,14 -LDT_STOP

11,14,15 -CPURST

M2CPUD

MISC

C10 VDDA1

D10 VDDA2

A8 CLKIN_H

B8 CLKIN_L

CPU_PWRGD — C9 PWROK

-LDT_STOP — D8 LDTSTOP_L

-CPURST — C7 RESET_L

CPU_PRESENT_L — AL3 CPU_PRESENT_L

DG:AM3 1.04

DDR15V — AR4 1K/4/1 — SIC — AL6 SIC

21 SIC

21 SID — SID — AK6 SID

DDR15V — AR5 1K/4/1

15 CPU_TDI — CPU_TDI — AL10 TDI

CPU_TRST- — AJ10 TRST_L

CPU_TCK — AH10 TCK

15 CPU_TMS — CPU_TMS — AL9 TMS

CPU_DBREQ- — A5 DBREQ_L

29 COREFB+ — G2 VDD_FB_H

29,30 COREFB- — G1 VDD_FB_L

E12 VTT_SENSE

VTT_SENSE AM3 only, may not use, like AM2

CPU_M_VREF — F12 M_VREF

DDR15V — AR6 39.2/4/1 — AH11 M_ZN

AR7 39.2/4/1/X — AJ11 M_ZP

CPU_TEST25_H — A10 TEST25_H

CPU_TEST25_L — B10 TEST25_L

AR8 1K/4/1 — F10 TEST19

AR9 1K/4/1 — E9 TEST18

AJ7 TEST13

F6 TEST9

D6 TEST17

E7 TEST16

F8 TEST15

C5 TEST14

AH9 TEST12

AR10 1K/4/1

E5 TEST7

AJ5 TEST6

AG9 THERMDC

AG8 THERMDA

AH7 TEST3

AJ6 TEST2

21 GNDA

21 TMPIN2

M2CPUD

MISC

D2 VID(5)

D1 VID(4)

C1 VID(3) — SVC — SVC 29

E3 VID(2) — SVD — SVD 29

E2 VID(1) — AR20 300/4

E1 VID(0)

AM3 only

AK7 THERMTRIP_L

AL7 PROCHOT_L — -PROCHOT

AK10 TDO

B6 DBRDY

AK11 VDDIO_FB_H

AL11 VDDIO_FB_L

F1 PSI_L

V8 — AR52 46.4/4/1 — VCC12_HT

V7 — AR53 46.4/4/1

C11 — AR54 80.6/4/1/X

D11

AK8 TEST24

AH8 TEST23 — AR55 1K/4/1

AJ9 TEST22 — CPU_TEST22

AL8 TEST21 — CPU_TEST21

AJ8 TEST20 — CPU_TEST20

J10 TEST28_H

H9 TEST28_L

AK9 TEST27 — CPU_TEST27

AK5 TEST26 — CPU_TEST26

G7 TEST10

D4 TEST8

CPU-SK/941AM3/S/GF/[10SC1-A01942-01R_10SC1-A01942-02R]

DDR15V

AR16 1K/4/1

AR17 1K/4/1

AR18 1K/4/1

AR19 300/4

DDR15V

AR47 1K/4/1/X — CPU_TDI

AR48 1K/4/1/X — CPU_TRST-

AR49 1K/4/1/X — CPU_TCK

AR50 1K/4/1/X — CPU_TMS

AR51 300/4/X — CPU_DBREQ-

Route as 80-Ohm differential impedance

Keep trace to resistor less than 1" from CPU pin

LAYOUT: Route trace 50 mils wide and 500 to 750 mils long between these caps.

3VDUAL

AR24 8.2K/4/1

THERMTRIP_CPU_L — THERMTRIP_CPU_L 15,28

AQ5 MMBT2222A/SOT23/600mA/40 S0T23

DDR15V — AR22 1K/4/1 — AR23 1K/4/1

AQ4 MMBT2222A/SOT23/600mA/40 S0T23

AR21 1K/4/1

AR25 0/4/SHT/X — -PROCHOT_CPU — -PROCHOT_CPU 14,36

Erratum 133, Revision Guide for AMD NPT 0Fh Processors

DDR15V

CPU_TEST26 — AR26 1K/4/1

CPU_PRESENT_L — AR27 1K/4/1

CPU_TEST25_H — AR28 510/4/1/X

AR29 510/4/1

CPU_TEST25_L — AR30 510/4/1/X

AR31 510/4/1

CPU_TEST21 — AR32 1K/4/1

Erratum 133, Revision Guide for AMD NPT 0Fh Processors

DDR15V

CPU_TEST27 — AR33 1K/4/1

CPU_TEST20 — AR34 1K/4/1

CPU_TEST22 — AR35 1K/4/1

CPU_TEST24 — AR36 1K/4/1

3VDUAL

AR13 8.2K/4/1

VCC3

AR14 8.2K/4/1

PWM_PWRGD 29

DDR15V

AR11 300/4

AQ1

AQ2

AC8 0.1u/4/Y5V/16V/Z/X

14 CPU_PG_SB — AR12 1K/4/1

MMBT2222A/SOT23/600mA/40

2N7002/SOT23/25pF/5

DDR15V

AR15 1K/4/1

CPU_PWRGD

AMD comment for validation.

AQ3

AC9 0.1u/4/Y5V/16V/Z/X

2N7002/SOT23/25pF/5

CPUVREF

40 MILS WIDTH

DDR15V

CPU_M_VREF

SAR1 15/4/1

SABC1

SABC2

1N/4/X7R/50V/K

SABC3 1U/6/X7R/16V/K

SAR2 15/4/1

0.1U/4/X7R/16V/K

Layout: Place within 500mils of the CPU socket.

M2CPUE

INTERNAL MISC

L25 RSVD1

L26 RSVD2

L31 RSVD3

L30 RSVD4

MA_RESET-

MB_RESET-

ALERT-

SA0

RSVD21

AM3 only

E20 MA_RESET_L — MA_RESET_L 8

B19 MB_RESET_L — MB_RESET_L 9

AR37 1K/4/1 — DDR15V

AL4 CPU_ALERT-

AK4 AR40 1K/4/1

AK3

VCC3

3VDUAL

AR38 1K/4/1

AQ6

AR39 8.2K/4/1

SB_ALERT- 16

2N7002/SOT23/25pF/5

RSVD22

M_VDDIO_PWRGD

F2 CPU_IDLEEXIT-

F3 AR41 1K/4/1 — DDR15V

M_VDDIO_PWRGD AM3 Not support PID:40778

G4 COREFB_NB+ — COREFB_NB+ 29

G3 COREFB_NB-

G5 CORE_TYPE_DET — AR42 1K/4/1 — DDR15V

TP6

AM2: high, AM2R2: low

AM3 only

A10P — 8 DCLKA2 — DCLKA2 — W26

A10N — 8 -DCLKA2 — -DCLKA2 — W25

8 MODT_A3 — MODT_A3 — AE27

A01P — 8 DCLKA1 — DCLKA1 — U24

A01N — 8 -DCLKA1 — -DCLKA1 — V24

8 MODT_A1 — MODT_A1 — AE28

DCLKA2

DCLKA2-

MODT_A3

DCLKA1

DCLKA1-

MODT_A1

RSVD27 AD25

RSVD28 AE24

RSVD29 AE25

RSVD30 AJ18

RSVD31 AJ20

RSVD32 C18

RSVD33 C20

RSVD34 G24

RSVD35 G25

RSVD36 H25

V29

W30

AM3 only

B10P — 9 DCLKB2 — DCLKB2 — Y31

B10N — 9 -DCLKB2 — -DCLKB2 — Y30

9 MODT_B3 — MODT_B3 — AG31

B01P — 9 DCLKB1 — DCLKB1 — V31

B01N — 9 -DCLKB1 — -DCLKB1 — W31

9 MODT_B1 — MODT_B1 — AF31

DCLKB2

DCLKB2-

MODT_B3

DCLKB1

DCLKB1-

MODT_B1

MB_EVENT_L

MA_EVENT_L

AM3 =>DRAM Thermal Event Status

AR43 1K/4/1 — DDR15V

MB_EVENT_L — MB_EVENT_L 9

MA_EVENT_L — MA_EVENT_L 8

AR44 1K/4/1 — DDR15V

EVENT pins are for future AM3r2

Layout: Route as 60 ohms with 5/10 W/S from CPU pins.

3VDUAL

AR45 1K/4/1

AQ7

3VDUAL

AR46 8.2K/4/1

CPU_IDLEEXIT-

SB_IDLEEXIT- 15

2N7002/SOT23/25pF/5

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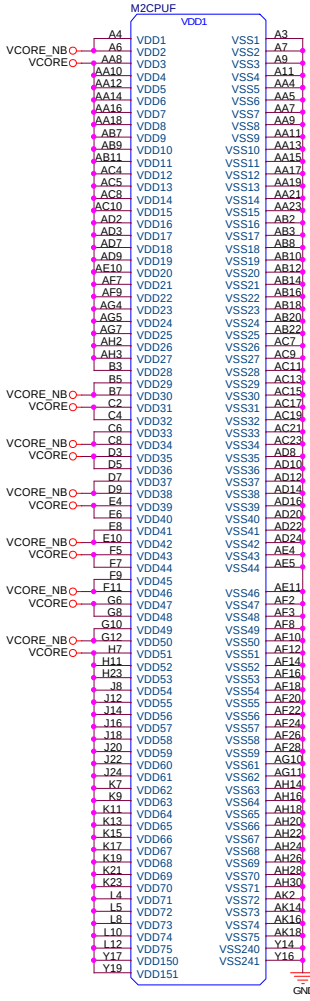
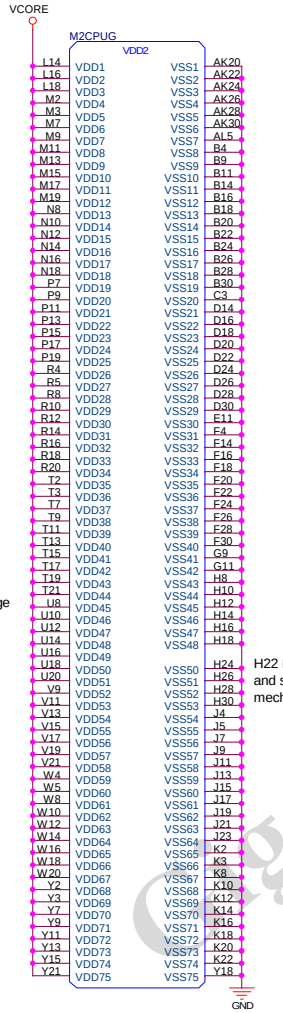
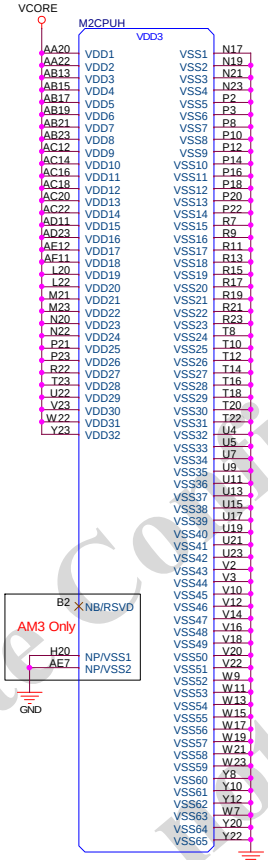
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

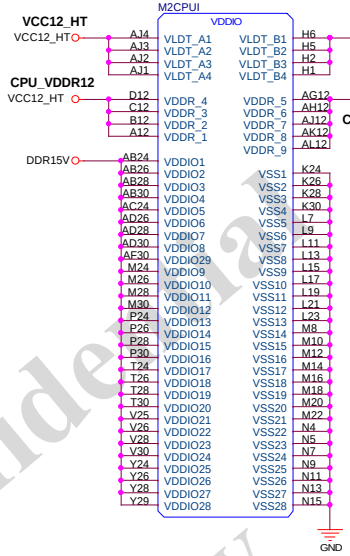


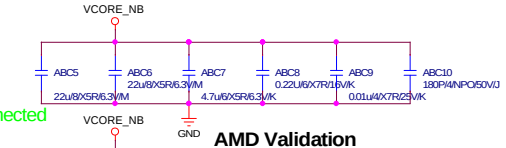
AE9 Missing pins on package and socket used for mechanical keying. =>AM3

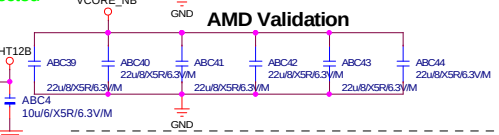


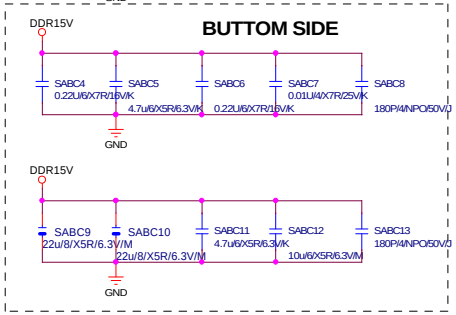


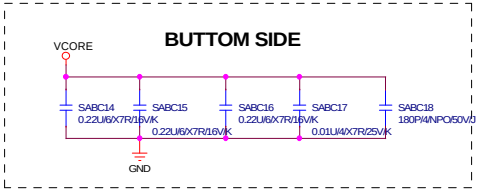
H22 Missing pins on package and socket used for mechanical keying. =>AM3

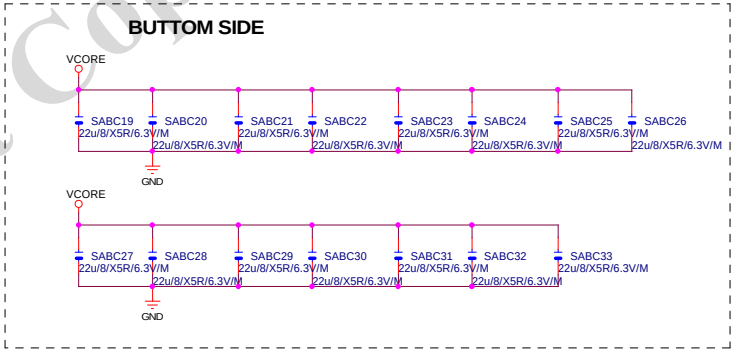


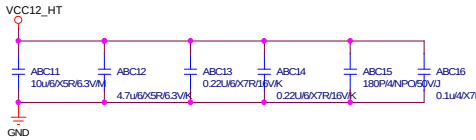


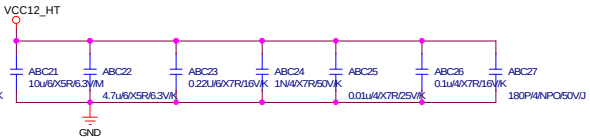


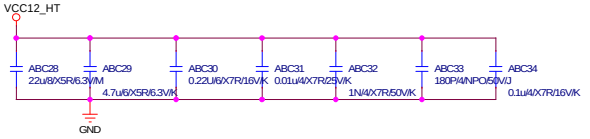


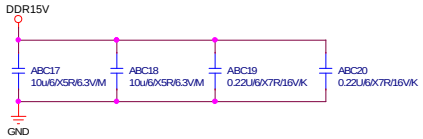


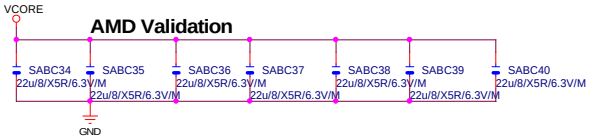


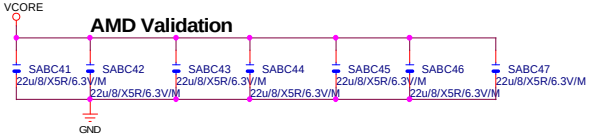


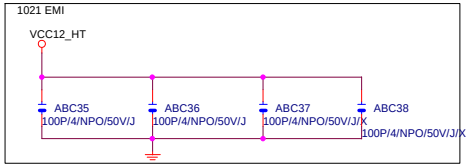












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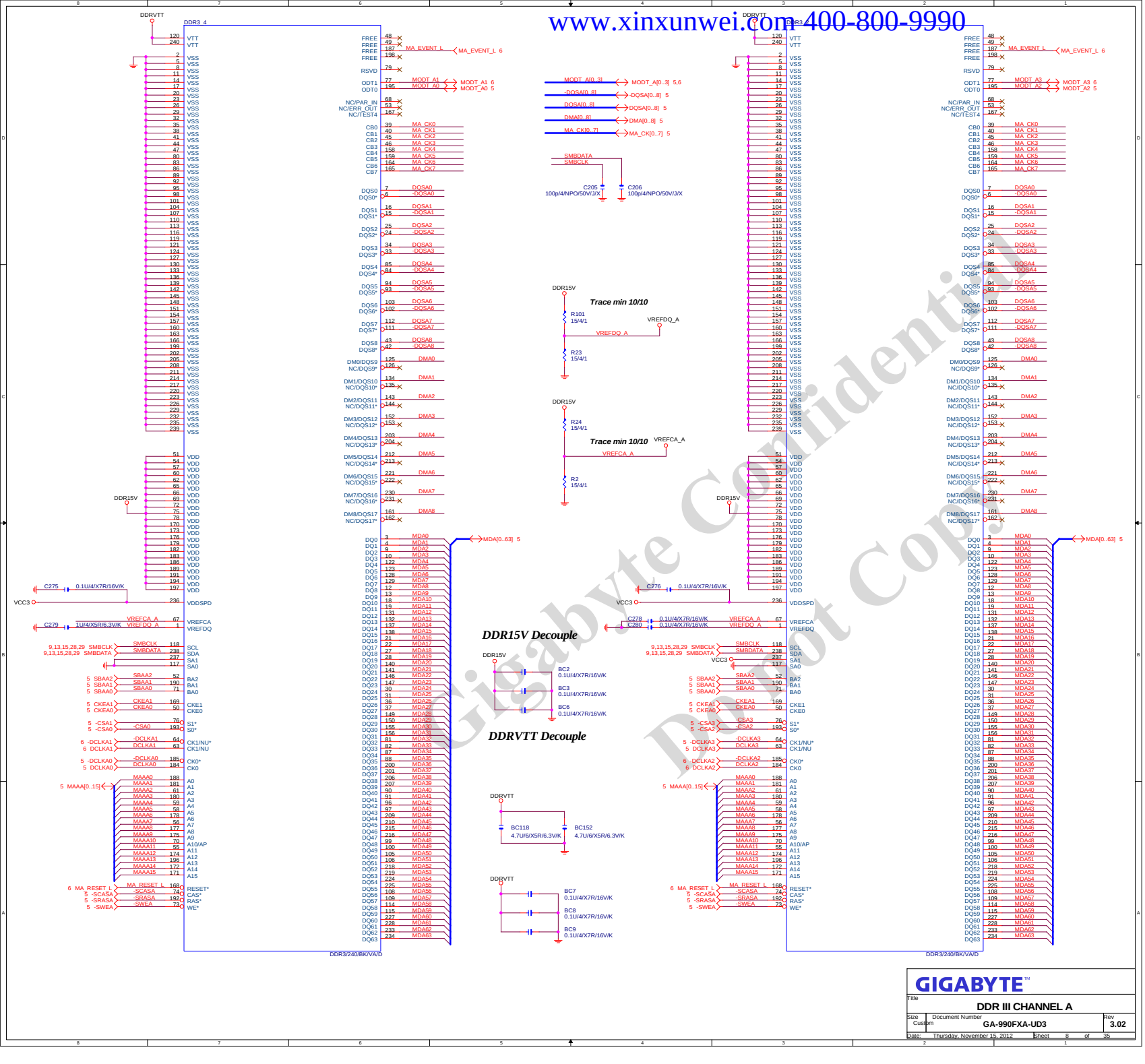
Title	CPU POWER & GND	
Size: Custom	Document Number: GA-990FXA-UD3	Rev: 3.02
Date: Thursday, November 15, 2012	Sheet 7 of 35	



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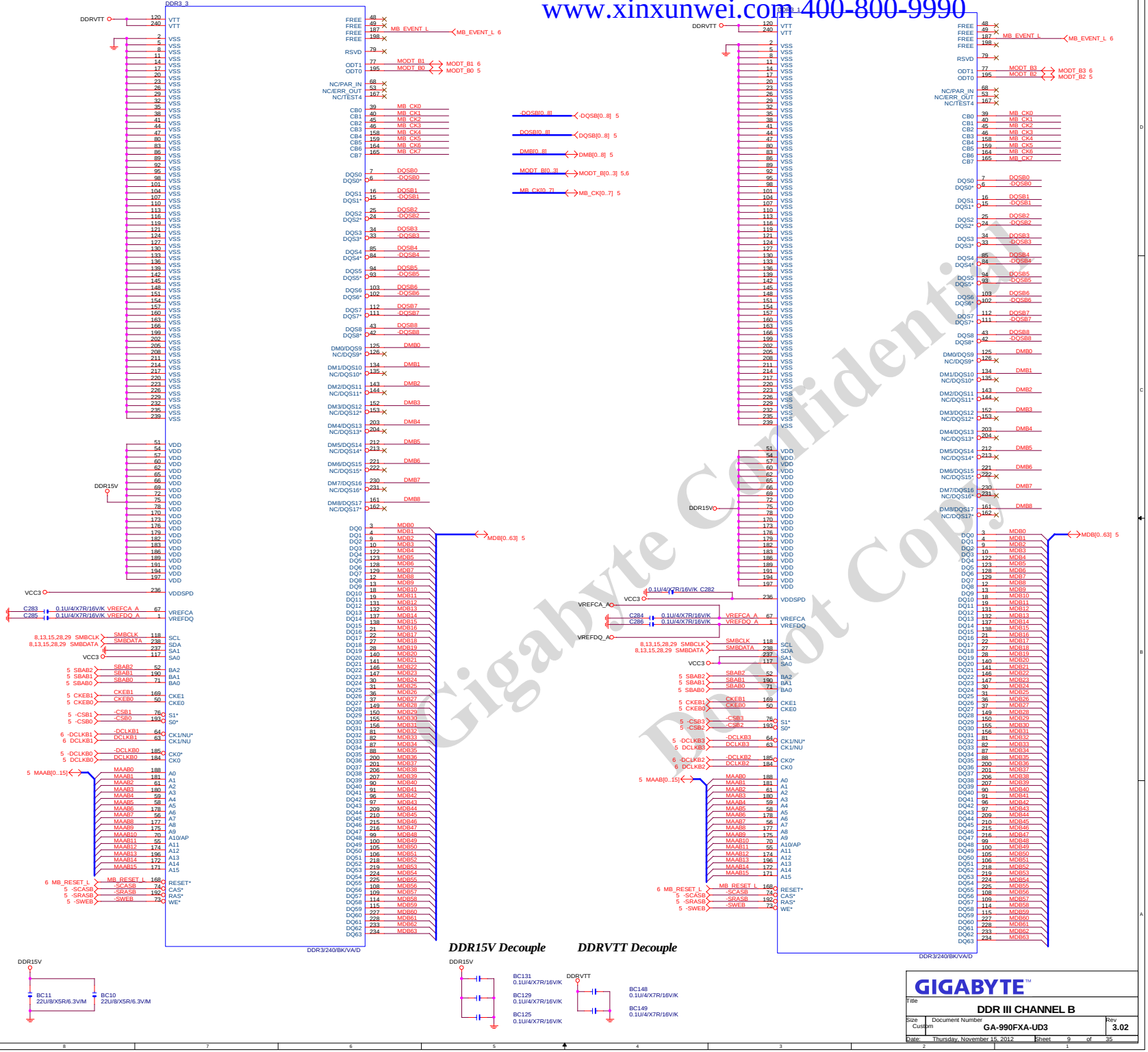
Title: DDR III CHANNEL A

Size	Document Number	Rev
Custom	GA-990FXA-UD3	3.02

Date: Thursday, November 15, 2012 Sheet 8 of 35



GIGABYTE™

Title: DDR III CHANNEL B

Size	Document Number	Rev
Custom	GA-990FXA-UD3	3.02

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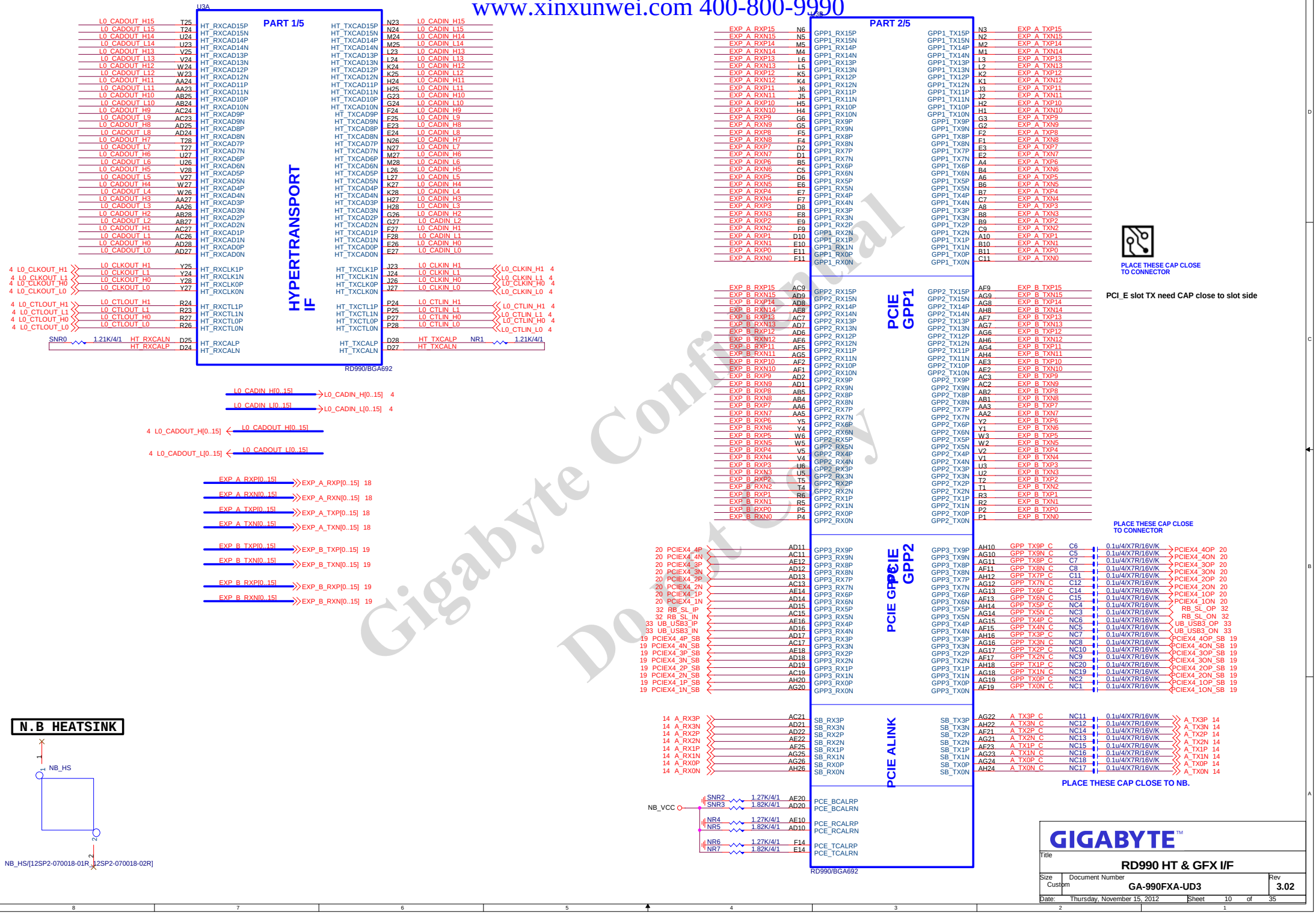
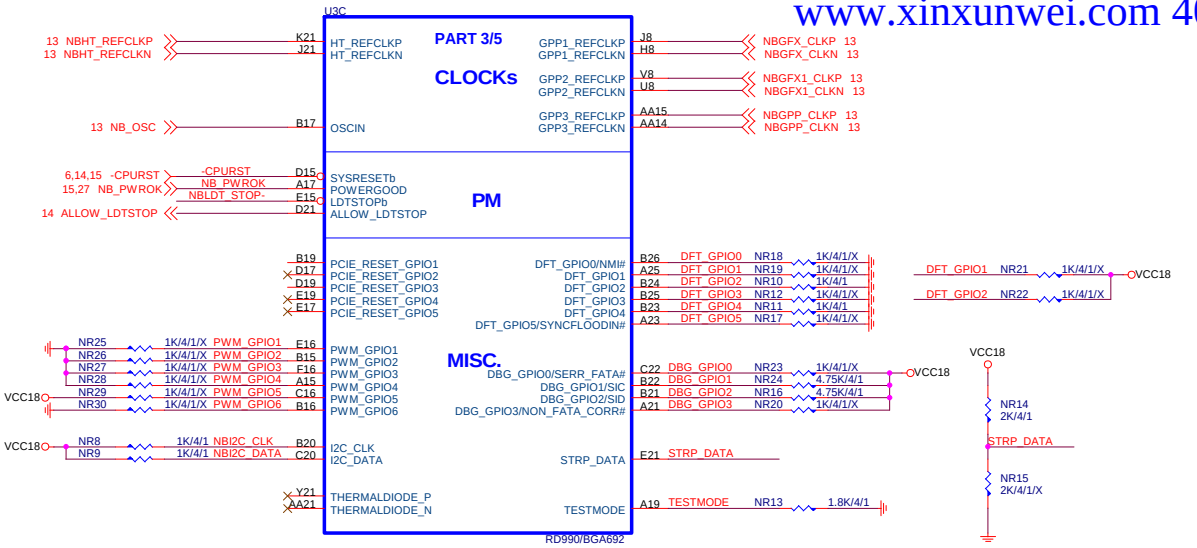


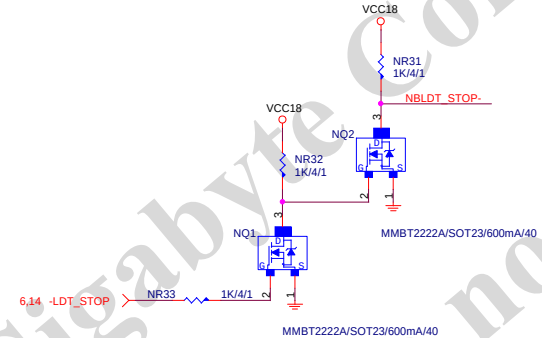
GIGABYTE™

Title: RD990 HT & GFX I/F

Size	Document Number	Rev
Custom	GA-990FXA-UD3	3.02

Date: Thursday, November 15, 2012 Sheet 10 of 35





DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
GPIO4:3:2
000 : 4:2:4 B
001 : 4:1:1:4 C
010 : 1:1:1:1:1:1:4 L (Hardware Default)
011 : 2:1:1:1:1:4 E
100 : 2:2:1:1:4 K
101: 2:2:2:4 C2
110: Hardware default (mode L) or EEPROM
111: Hardware default (mode L) or EEPROM
101 : 01100
111 : 01011

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

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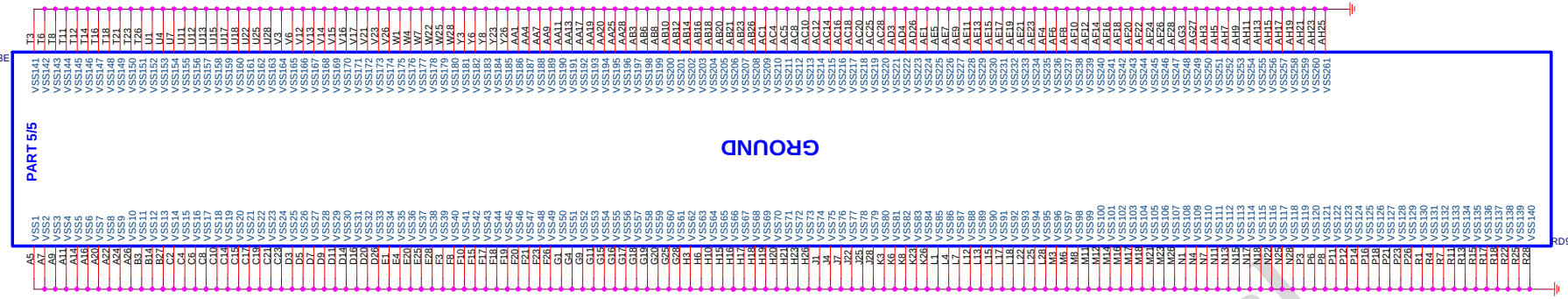
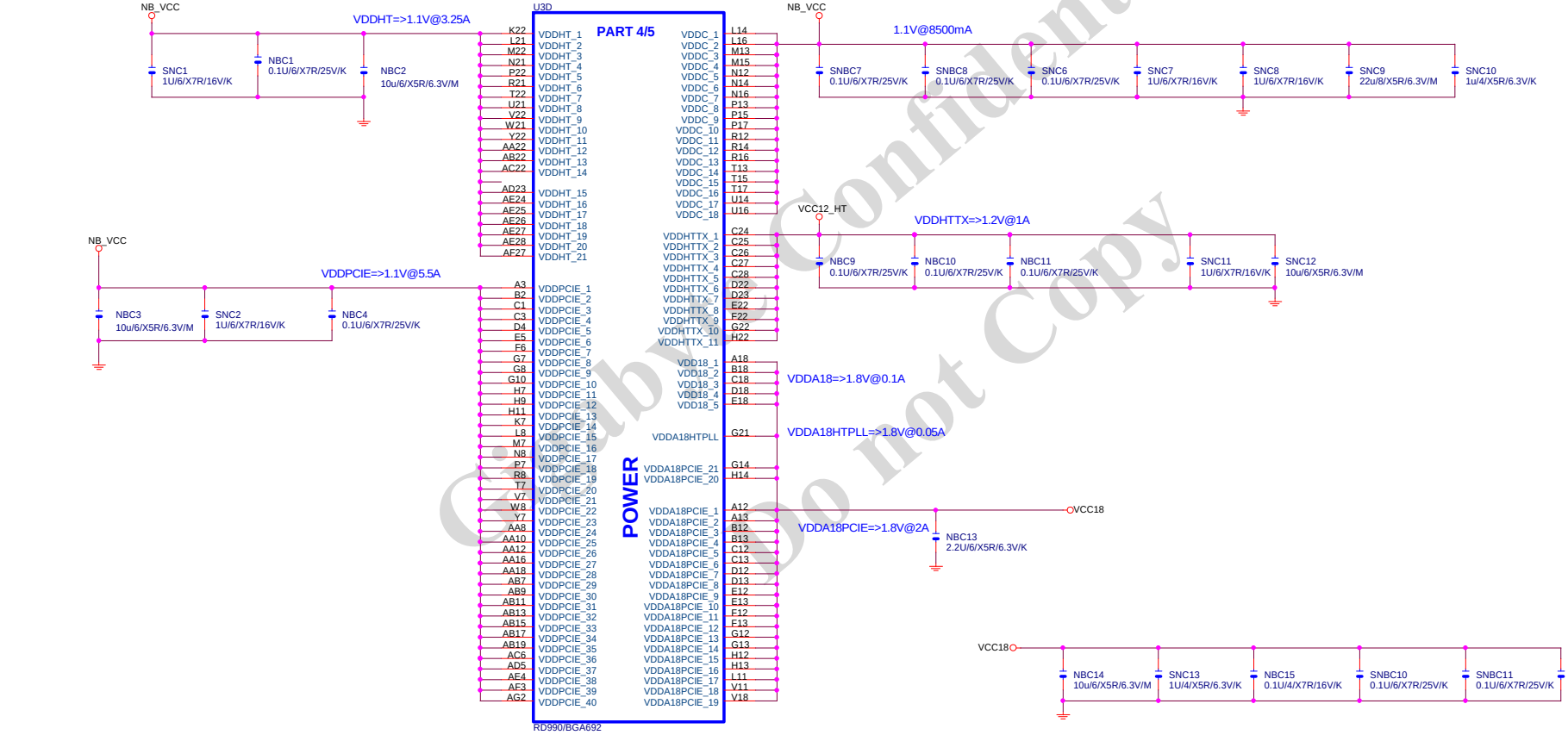
Title	RD990 CLOCK & SYSB I/F	
Size: Custom	Document Number: GA-990FXA-UD3	Rev: 3.02
Date: Thursday, November 15, 2012	Sheet 11 of 35	





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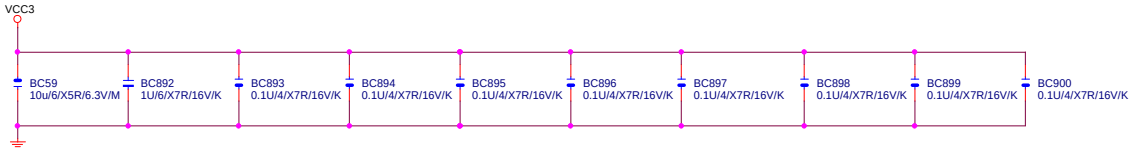
Title: RD990 POWER

Size: Custom | Document Number: GA-990FXA-UD3 | Rev: 3.02

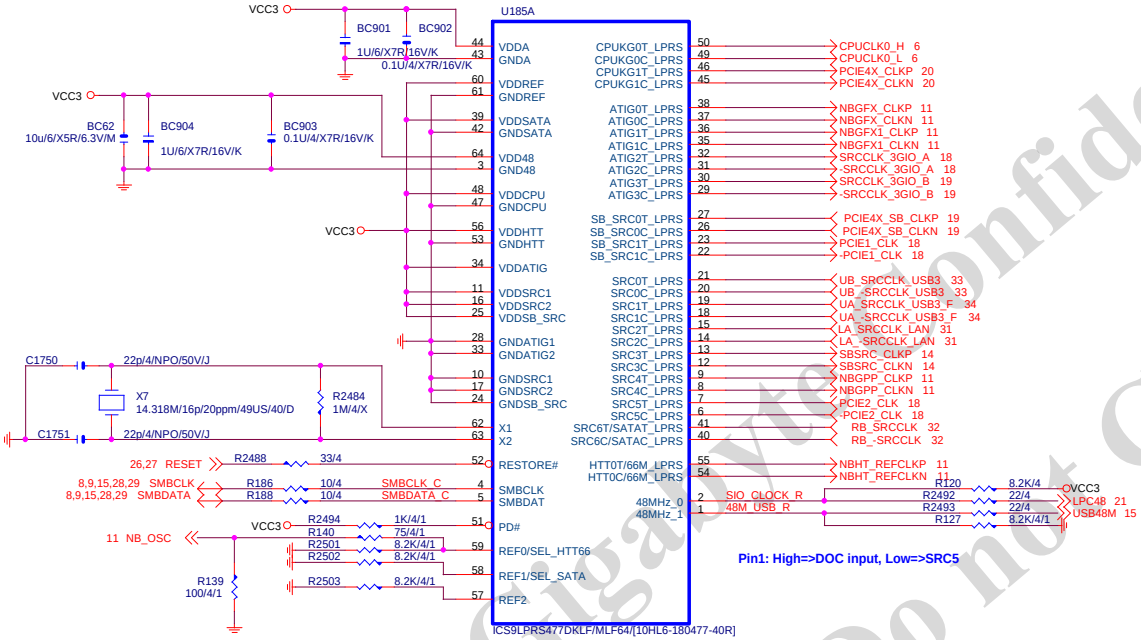
Date: Thursday, November 15, 2012 | Sheet 12 of 35



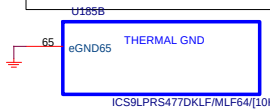
NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

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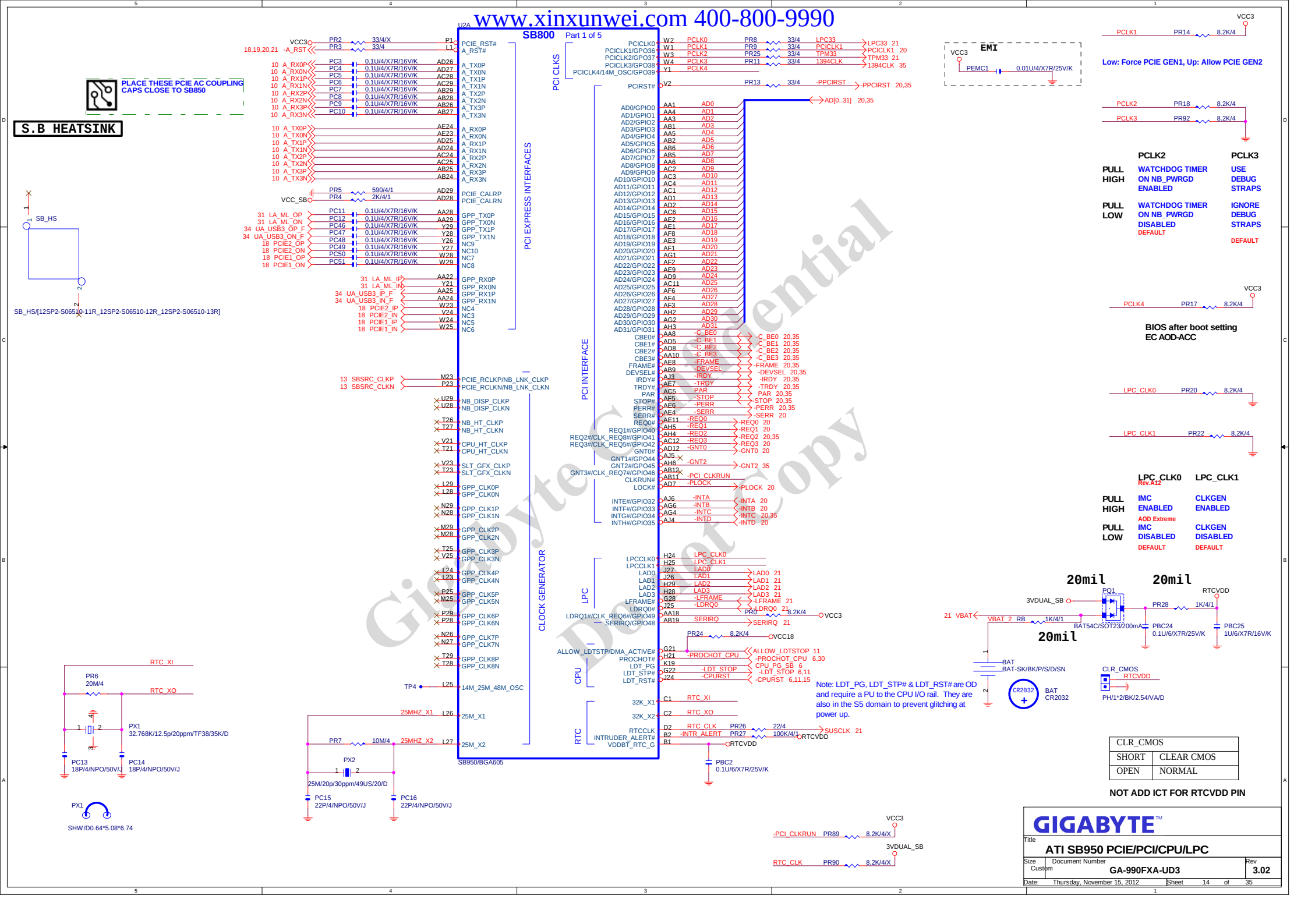
Title: ICS9LPRS477

Size: Custom | Document Number: GA-990FXA-UD3 | Rev: 3.02

Date: Thursday, November 15, 2012 | Sheet 13 of 35



USB11	FRONT PANEL
USB10	FRONT PANEL
USB9	FRONT PANEL
USB8	FRONT PANEL
USB7	FRONT PANEL
USB6	FRONT PANEL
USB5	FRONT PANEL
USB4	FRONT PANEL
USB3	REAR PANEL
USB2	REAR PANEL
USB1	REAR PANEL
USB0	REAR PANEL

either HWM inputs or PWR_GD signals can be used for power-up sequencer

3VDUAL_SB

IMC_GPIO200 PR61 2.2K/4/1

IMC_GPIO199 PR62 2.2K/4/1

IMC_GPIO200 IMC_GPIO199

ROM TYPE:

H, H = Reserved

H, L = SPI ROM DEFAULT

L, H = LPC ROM

L, L = FWH ROM

SB_TEST2 PR29 8.2K/4
SB_TEST1 PR30 8.2K/4
SB_TEST0 PR31 8.2K/4

VCC3

-SUS_STAT PR32 8.2K/4
SMBCLK PR55 1K/4/1
SMBDATA PR56 1K/4/1
WD_PWRGD PR33 8.2K/4
-LPCSMI PR46 8.2K/4

3VDUAL_SB

-RI PR34 8.2K/4
SMBCLK1 PR57 2.2K/4/1
SMBDATA1 PR58 2.2K/4/1
-PCIE_WAKE PR59 2.2K/4/1

-PCIPME PR60 2.2K/4/1 3VDUAL
UB_SMIB PR76 8.2K/4/1 3VDUAL
MOS_OT R89 8.2K/4/1 3VDUAL

SB_PWROK

PBC4 100P/4/NPO/50V/J/X

3VDUAL_SB PR91 20K/4/1/X -RSMRST

PBC3 2.2U/6/X5R/6.3V/K/X

SMBCLK
SMBDATA

PBC5 100P/4/NPO/50V/J/X
PBC6 100P/4/NPO/50V/J/X

AZ_BIT_CLK

PBC7 100P/4/NPO/50V/J/X

VCC3

AZ_SDATA_OUT PR36 8.2K/4/X
PR35 8.2K/4

Low: Performance Mode(D),
Up: Low Power Mode.

-AZ_RST PR37 8.2K/4

Low: Disable PCI MEM boot(D),
Up: Enable PCI MEM boot

26 -SYS_RST PR68 22/4

PC17 22P/4/N/50V/X

18,19,20,31,33,34 -PCIE_WAKE

6,28 THERMTRIP_CPU_L PR67 0/4/X

11,27 NB_PWROK

21 -RSMRST

19 EXP_B_PRSNT-

19 PE4_2PRSNT_SB_R-
18 PE0_PRSNT-
20 PE4_2PRSNT_R-

26 SPKR
8,9,13,28,29 SMBCLK
8,9,13,28,29 SMBDATA
18,19,20 SMBCLK1
18,19,20 SMBDATA1

VCC3 PR38 8.2K/4 DDR3_RST-

6 SB_IDLEEXIT-

30 MOS_OT
34 UA_SMIB PR93 0/4/SHT/X
33 UB_SMIB

31 -USBOC_R1

22 -USBOC_F1

23 AZ_BIT_CLK PR63 22/4
23 AZ_SDATA_OUT PR64 22/4
23 AZ_SDATA_IN0

23 AZ_SYNC PR65 22/4
23 -AZ_RST PR66 22/4

3VDUAL PR39 8.2K/4 GBE_COL
PR40 8.2K/4 GBE_CRS
PR41 8.2K/4 GBE_MDIO

PR42 8.2K/4 GBE_RXERR

3VDUAL PR43 8.2K/4 GBE_INTR

20,35 -PCIPME
25 -RI

21,27 -SLP_S3
21,27 SLP_S5-
21 -PSOUT
27 SB_PWROK
PR69 0/4/SHT/X PWRBTN

-SUS_STAT

SB_TEST2
SB_TEST1
SB_TEST0

21 A20GATE
21 -KBRST
21 -LPCPME
21 GP80
PR45 0/4/SHT/X LPCSMI

-RI
-PCIE_WAKE
-LPCPME
THERMTRIP_CPU_L
PE0_PRSNT-
SPKR
SMBCLK
SMBDATA
SMBCLK1
SMBDATA1

U2D

SB800
Part 4 of 5

PCI_PME#/GEVENT4#	J2		
RI#/GEVENT22#	K1		
SPI_CS3#/GBE_STAT1/GEVENT21#	D3		
SLP_S3#	F1		
SLP_S5#	H1		
PWR_BTN#	F2		
PWR_GOOD	H5		
SUS_STAT#	G6		
TEST0	B3		
TEST1/TMS	C4		
TEST2	F6		
GA20IN/GEVENT0#	AD21		
KBRST#/GEVENT1#	AE21		
LPC_PME#/GEVENT3#	K2		
LPC_SMI#/GEVENT23#	J29		
GEVENT5#	H2		
SYS_RESET#/GEVENT19#	J1		
WAKE#/GEVENT8#	H6		
IR_RX1/GEVENT20#	F3		
THRMTRIP#/SMBALERT#/GEVENT2#	J6		
NB_PWRGD	AC19		
RSMRST#	G1		
CLK_REQ4#/SATA_IS0#/GPIO64	AD19		
CLK_REQ3#/SATA_IS1#/GPIO63	AA16		
SMARTVOLT1/SATA_IS2#/GPIO50	AB21		
CLK_REQ0#/SATA_IS3#/GPIO60	AC18		
SATA_IS4#/FANOUT3/GPIO55	AF20		
SATA_IS5#/FANIN3/GPIO59	AE19		
SPKR/GPIO66	AF19		
SCL0/GPIO43	AD22		
SDA0/GPIO47	AE22		
SCL1/GPIO227	F5		
SDA1/GPIO228	F4		
CLK_REQ2#/FANIN4/GPIO62	AH21		
CLK_REQ1#/FANOUT4/GPIO61	AB18		
IR_LED#/LLB#/GPIO184	E1		
SMARTVOLT2/SHUTDOWN#/GPIO51	AJ21		
DDR3_RST#/GEVENT7#	H4		
GBE_LED0/GPIO183	D5		
GBE_LED1/GEVENT9#	D7		
GBE_LED2/GEVENT10#	G5		
GBE_STAT0/GEVENT11#	K3		
CLK_REQG#/GPIO65/OSCIN	AA20		
BLINK/USB_OC7#/GEVENT18#	H3		
USB_OC6#/IR_TX1/GEVENT6#	D1		
USB_OC5#/IR_TX0/GEVENT17#	E4		
USB_OC4#/IR_RX0/GEVENT16#	D4		
USB_OC3#/AC_PRES/TDO/GEVENT15#	E8		
USB_OC2#/TCK/GEVENT14#	F7		
USB_OC1#/TDI/GEVENT13#	E7		
USB_OC0#/TRST#/GEVENT12#	F8		
AZ_BITCLK	M3		
AZ_SDOUT	N1		
AZ_SDIN0/GPIO167	L2		
AZ_SDIN1/GPIO168	M2		
AZ_SDIN2/GPIO169	M1		
AZ_SDIN3/GPIO170	M4		
AZ_SYNC	N2		
AZ_RST#	P2		
GBE_COL	T1		
GBE_CRS	T4		
GBE_MDCK	L6		
GBE_MDIO	L5		
GBE_RXCLK	T9		
GBE_RXD3	U1		
GBE_RXD2	U3		
GBE_RXD1	T2		
GBE_RXD0	U2		
GBE_RXCTL/RXDV	T5		
GBE_RXERR	V5		
GBE_TXCLK	P5		
GBE_TXD3	M5		
GBE_TXD2	P9		
GBE_TXD1	T7		
GBE_TXD0	P7		
GBE_TXCTL/TXEN	M7		
GBE_PHY_PD	P4		
GBE_PHY_RST#	M9		
GBE_PHY_INTR	V7		
PS2_DAT/SDA4/GPIO187	E23		
PS2_CLK/SCL4/GPIO188	E24		
SPI_CS2#/GBE_STAT2/GPIO166	F21		
FC_RST#/GPO160	G29		
PS2KB_DAT/GPIO189	D27		
PS2KB_CLK/GPIO190	F28		
PS2M_DAT/GPIO191	F29		
PS2M_CLK/GPIO192	E27		
USBCLK/14M_25M_48M_OSC	A10		
USB_RCOMP	G19		
USB_FSD1P/GPIO186	J10		
USB_FSD1N	H11		
USB_FSD0P/GPIO185	H9		
USB_FSD0N	J8		
USB_HSD13P	B12	+USBP13	+USBP13 22
USB_HSD13N	A12	-USBP13	-USBP13 22
USB_HSD12P	F11	+USBP12	+USBP12 22
USB_HSD12N	E11	-USBP12	-USBP12 22
USB_HSD11P	E14	+USBP11	+USBP11 22
USB_HSD11N	E12	-USBP11	-USBP11 22
USB_HSD10P	J12	+USBP10	+USBP10 22
USB_HSD10N	J14	-USBP10	-USBP10 22
USB_HSD9P	A13	+USBP9	+USBP9 32
USB_HSD9N	B13	-USBP9	-USBP9 32
USB_HSD8P	D13	+USBP8	+USBP8 32
USB_HSD8N	C13	-USBP8	-USBP8 32
USB_HSD7P	G12	+USBP7	+USBP7 31
USB_HSD7N	G14	-USBP7	-USBP7 31
USB_HSD6P	G16	+USBP6	+USBP6 31
USB_HSD6N	G18	-USBP6	-USBP6 31
USB_HSD5P	D16	+USBP5	+USBP5 22
USB_HSD5N	C16	-USBP5	-USBP5 22
USB_HSD4P	B14	+USBP4	+USBP4 22
USB_HSD4N	A14	-USBP4	-USBP4 22
USB_HSD3P	E18	+USBP3	+USBP3 21
USB_HSD3N	E16	-USBP3	-USBP3 21
USB_HSD2P	J16	+USBP2	+USBP2 21
USB_HSD2N	J18	-USBP2	-USBP2 21
USB_HSD1P	B17	+USBP1	+USBP1 32
USB_HSD1N	A17	-USBP1	-USBP1 32
USB_HSD0P	A16	+USBP0	+USBP0 32
USB_HSD0N	B16	-USBP0	-USBP0 32
SCL2/GPIO193	D25		
SDA2/GPIO194	F23		
SCL3_LV/GPIO195	B26		
SDA3_LV/GPIO196	E26		
EC_PWM0/EC_TIMER0/GPIO197	F25		
EC_PWM1/EC_TIMER1/GPIO198	E22		
EC_PWM2/EC_TIMER2/GPIO199	F22	IMC_GPIO199	
EC_PWM3/EC_TIMER3/GPIO200	E21	IMC_GPIO200	
KSI_0/GPIO201	G24		
KSI_1/GPIO202	G25		
KSI_2/GPIO203	E28		
KSI_3/GPIO204	E29		
KSI_4/GPIO205	D29		
KSI_5/GPIO206	D28		
KSI_6/GPIO207	C29		
KSI_7/GPIO208	C28		
KSO_0/GPIO209	B28		
KSO_1/GPIO210	A27	IMC_TDO	
KSO_2/GPIO211	B27		
KSO_3/GPIO212	D26	IMC_TMS	
KSO_4/GPIO213	A26	IMC_TCK	
KSO_5/GPIO214	C26		
KSO_6/GPIO215	A24		
KSO_7/GPIO216	B25	IMC_CRST-	
KSO_8/GPIO217	A25		
KSO_9/GPIO218	D24		
KSO_10/GPIO219	B24		
KSO_11/GPIO220	C24		
KSO_12/GPIO221	B23		
KSO_13/GPIO222	A23		
KSO_14/GPIO223	D22		
KSO_15/GPIO224	C22		
KSO_16/GPIO225	A22		
KSO_17/GPIO226	B22		

ACPI / WAKE UP EVENTS
USB 1.1 USB MISC
USB 2.0
GPIO
USB OC
HD AUDIO
GBE LAN
EMBEDDED CTRL
EMBEDDED CTRL

SB950/BGA605

USB48M 13

SPR1 11.8K/4/1

D25 PR52 8.2K/4 3VDUAL_SB
F23 PR53 8.2K/4
B26 SCL3 PR95 8.2K/4
E26 SDA3 PR96 8.2K/4

DDR15V

PR51 8.2K/4/X
PQ9
IMC_CRST- PR98 100/4/1/X1
3 -CPURST -CPURST 6,11,14
2
MMBT3904/SOT23/200mA/30/X
SOT23

DDR15V

PR50 8.2K/4
PQ8
IMC_TMS PR10 100/4/1
3 CPU_TMS CPU_TMS 6
1
MMBT3904/SOT23/200mA/30
PBC19 33P/4/NPO/50V/J/X
SOT23

DDR15V

PR49 8.2K/4
PQ7
IMC_TCK PR88 100/4/1
3 CPU_TCK CPU_TCK 6
1
MMBT3904/SOT23/200mA/30
PBC23 33P/4/NPO/50V/J/X
SOT23

DDR15V

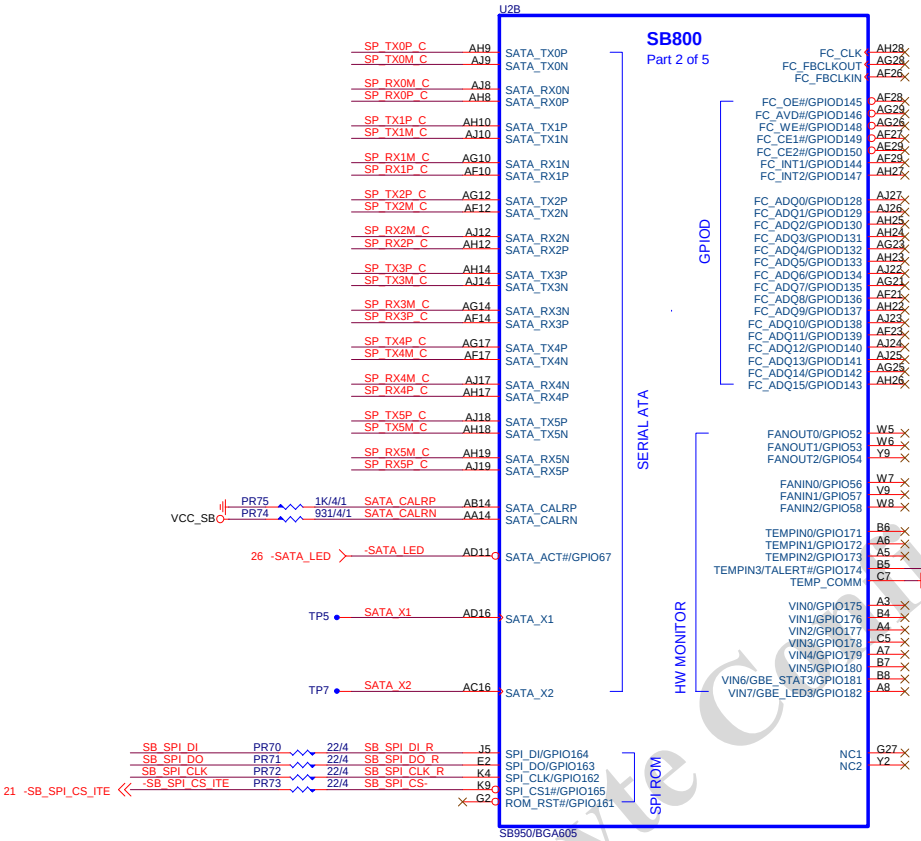
PR47 8.2K/4
PQ5
IMC_TDO PR54 100/4/1
3 CPU_TDI CPU_TDI 6
1
MMBT3904/SOT23/200mA/30
SOT23

GIGABYTE™

Title: ATI SB950 ACPI/USB/GPIO/AUDIO

Size	Document Number	Rev
Custom	GA-990FXA-UD3	3.02

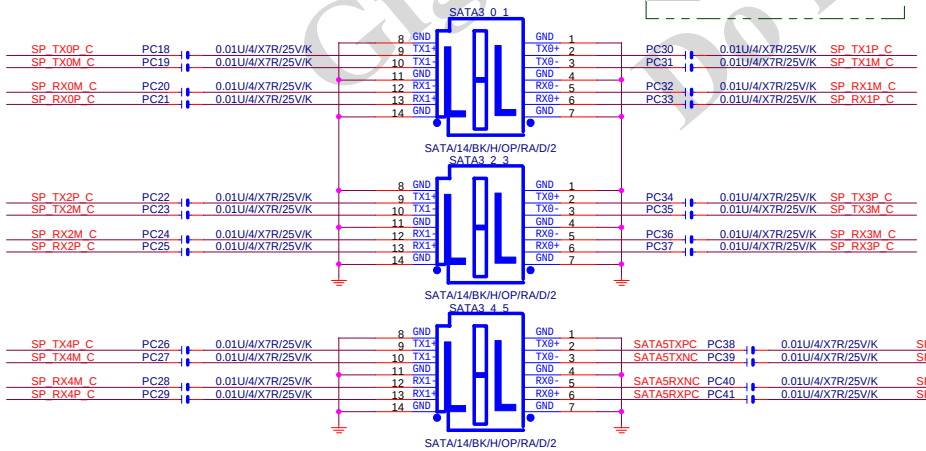
Date: Thursday, November 15, 2012 Sheet 15 of 35

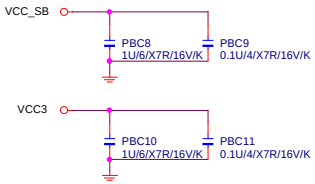


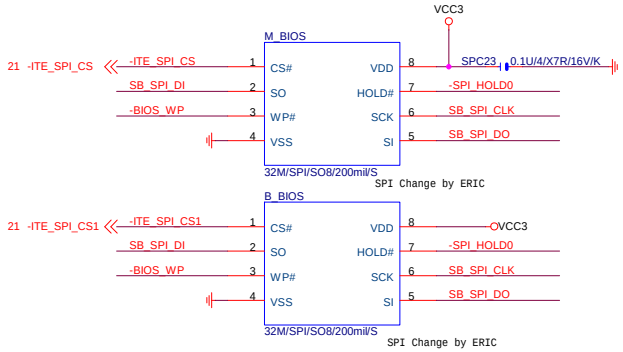
PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600

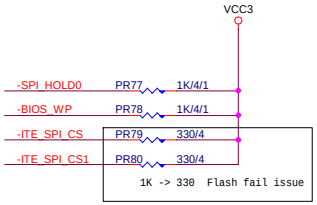
NOTE :
R650 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

PLACE SATA AC COUPLING CAPS CLOSE TO SB850









GIGABYTE™

Title: ATI SB950 SATA/IDE/HWM/SPI

Size	Document Number	Rev
Custom	GA-990FXA-UD3	3.02

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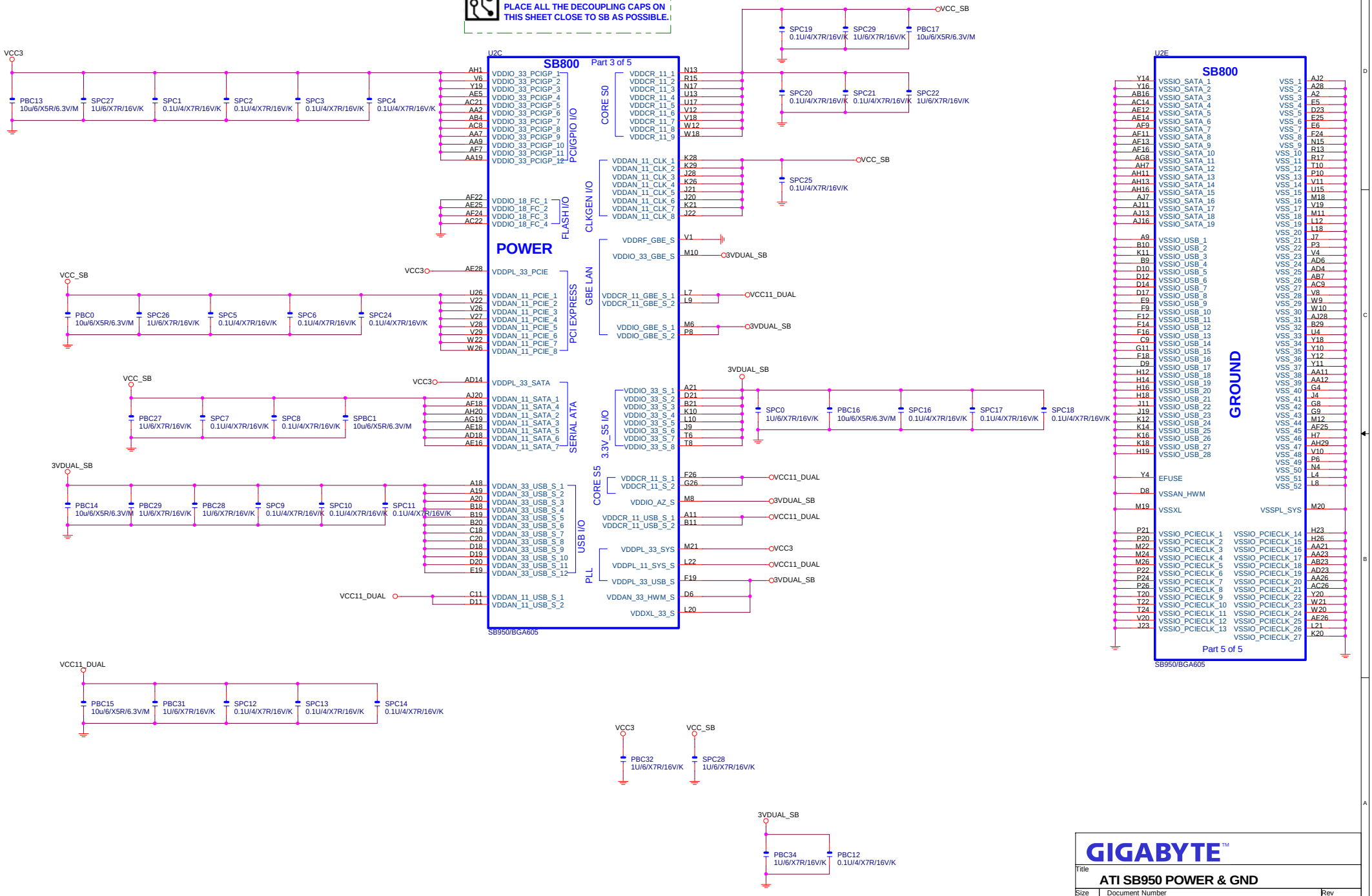
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



Title	ATI SB950 POWER & GND	
Size: Custom	Document Number: GA-990FXA-UD3	Rev: 3.02
Date: Thursday, November 15, 2012	Sheet 17 of 35	

Lay 在 PCIe slot 旁

PCIEX16_1 3GIO_*16

PCI-E/16X-164P/BK/LOWR EJECTOR

PCIEX1_2 3GIO_X1

PCI-E/1X-36P/BK/OL

PCIEX1_1 3GIO_X1

PCI-E/1X-36P/BK/OL

Title	PCI EXPRESS X 16 ,X1
Size	Custom
Document Number	GA-990FXA-UD3
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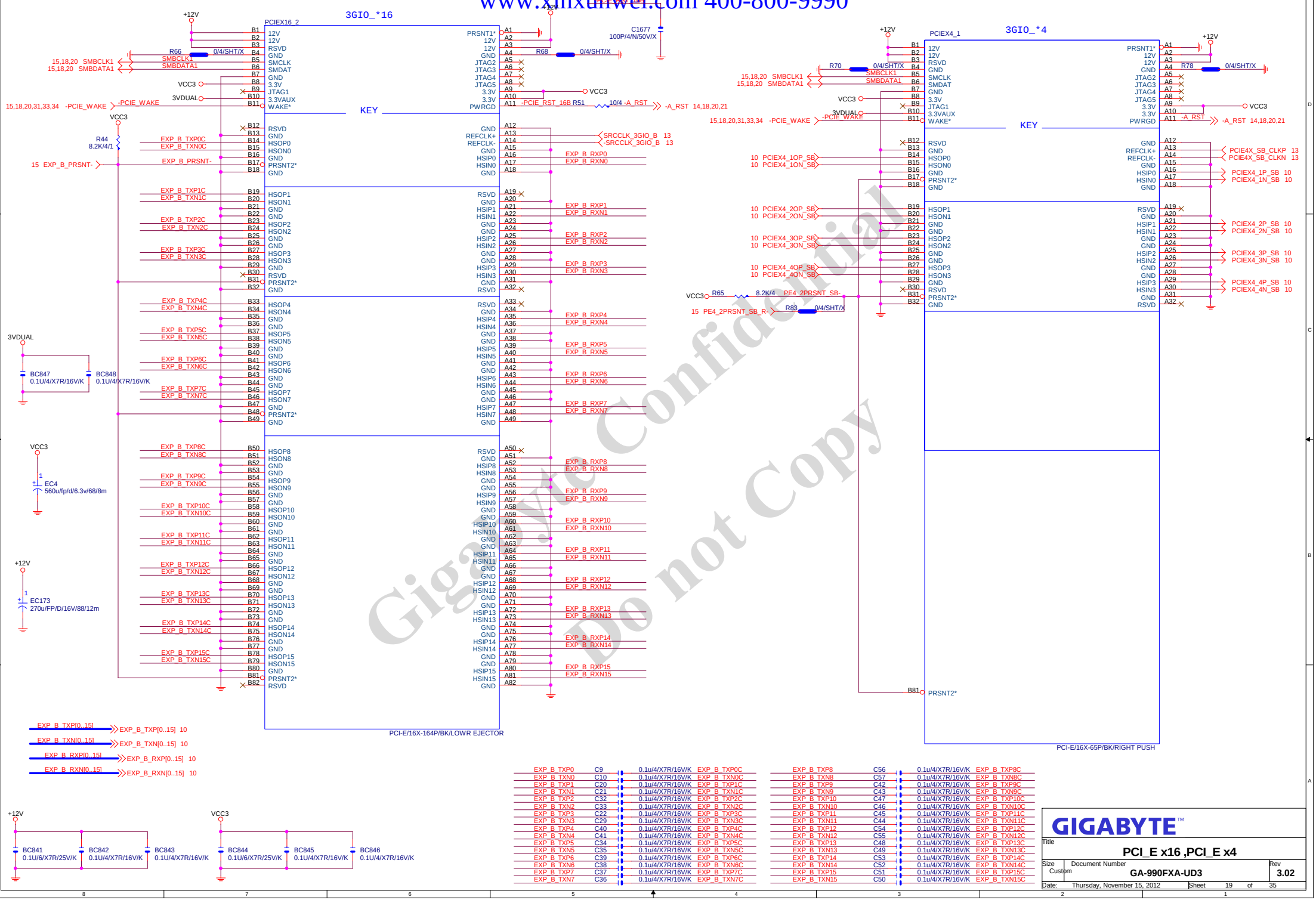

EXP_B_TXP0	C9	0.1u/4/X7R/16V/K	EXP_B_TXP0C	EXP_B_TXP8	C56	0.1u/4/X7R/16V/K	EXP_B_TXP8C
EXP_B_TXN0	C10	0.1u/4/X7R/16V/K	EXP_B_TXN0C	EXP_B_TXN8	C57	0.1u/4/X7R/16V/K	EXP_B_TXN8C
EXP_B_TXP1	C20	0.1u/4/X7R/16V/K	EXP_B_TXP1C	EXP_B_TXP9	C42	0.1u/4/X7R/16V/K	EXP_B_TXP9C
EXP_B_TXN1	C21	0.1u/4/X7R/16V/K	EXP_B_TXN1C	EXP_B_TXN9	C43	0.1u/4/X7R/16V/K	EXP_B_TXN9C
EXP_B_TXP2	C32	0.1u/4/X7R/16V/K	EXP_B_TXP2C	EXP_B_TXP10	C47	0.1u/4/X7R/16V/K	EXP_B_TXP10C
EXP_B_TXN2	C33	0.1u/4/X7R/16V/K	EXP_B_TXN2C	EXP_B_TXN10	C46	0.1u/4/X7R/16V/K	EXP_B_TXN10C
EXP_B_TXP3	C22	0.1u/4/X7R/16V/K	EXP_B_TXP3C	EXP_B_TXP11	C45	0.1u/4/X7R/16V/K	EXP_B_TXP11C
EXP_B_TXN3	C29	0.1u/4/X7R/16V/K	EXP_B_TXN3C	EXP_B_TXN11	C44	0.1u/4/X7R/16V/K	EXP_B_TXN11C
EXP_B_TXP4	C40	0.1u/4/X7R/16V/K	EXP_B_TXP4C	EXP_B_TXP12	C54	0.1u/4/X7R/16V/K	EXP_B_TXP12C
EXP_B_TXN4	C41	0.1u/4/X7R/16V/K	EXP_B_TXN4C	EXP_B_TXN12	C55	0.1u/4/X7R/16V/K	EXP_B_TXN12C
EXP_B_TXP5	C34	0.1u/4/X7R/16V/K	EXP_B_TXP5C	EXP_B_TXP13	C48	0.1u/4/X7R/16V/K	EXP_B_TXP13C
EXP_B_TXN5	C35	0.1u/4/X7R/16V/K	EXP_B_TXN5C	EXP_B_TXN13	C49	0.1u/4/X7R/16V/K	EXP_B_TXN13C
EXP_B_TXP6	C39	0.1u/4/X7R/16V/K	EXP_B_TXP6C	EXP_B_TXP14	C53	0.1u/4/X7R/16V/K	EXP_B_TXP14C
EXP_B_TXN6	C38	0.1u/4/X7R/16V/K	EXP_B_TXN6C	EXP_B_TXN14	C52	0.1u/4/X7R/16V/K	EXP_B_TXN14C
EXP_B_TXP7	C37	0.1u/4/X7R/16V/K	EXP_B_TXP7C	EXP_B_TXP15	C51	0.1u/4/X7R/16V/K	EXP_B_TXP15C
EXP_B_TXN7	C36	0.1u/4/X7R/16V/K	EXP_B_TXN7C	EXP_B_TXN15	C50	0.1u/4/X7R/16V/K	EXP_B_TXN15C

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Title	PCI_E x16 ,PCI_E x4	
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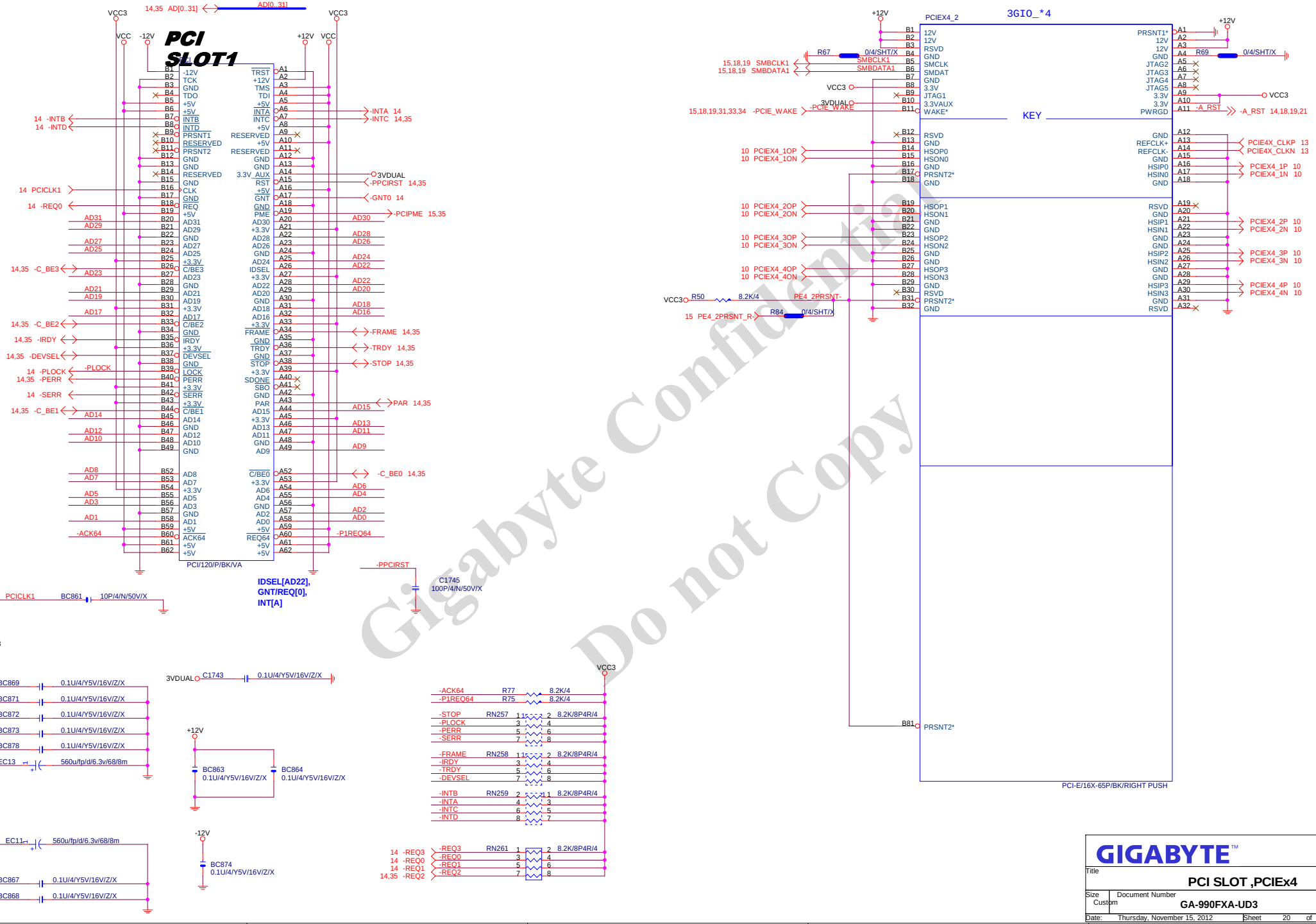

Title	PCI SLOT ,PCIEx4
Size	Custom
Document Number	GA-990FXA-UD3
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Date:	Thursday, November 15, 2012
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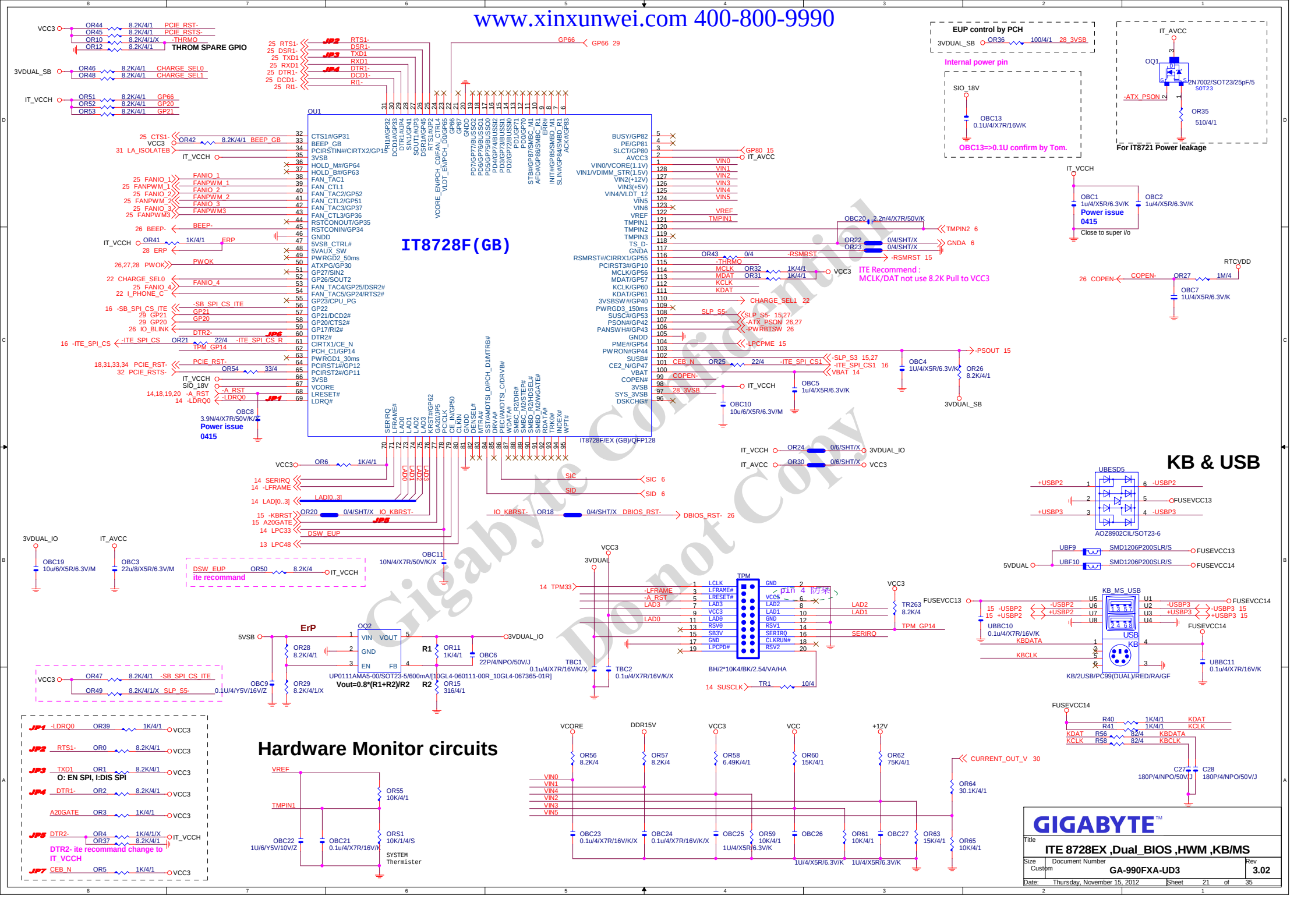

Title	ITE 8728EX ,Dual_BIOS ,HWM ,KB/MS
Size	Custom
Document Number	GA-990FXA-UD3
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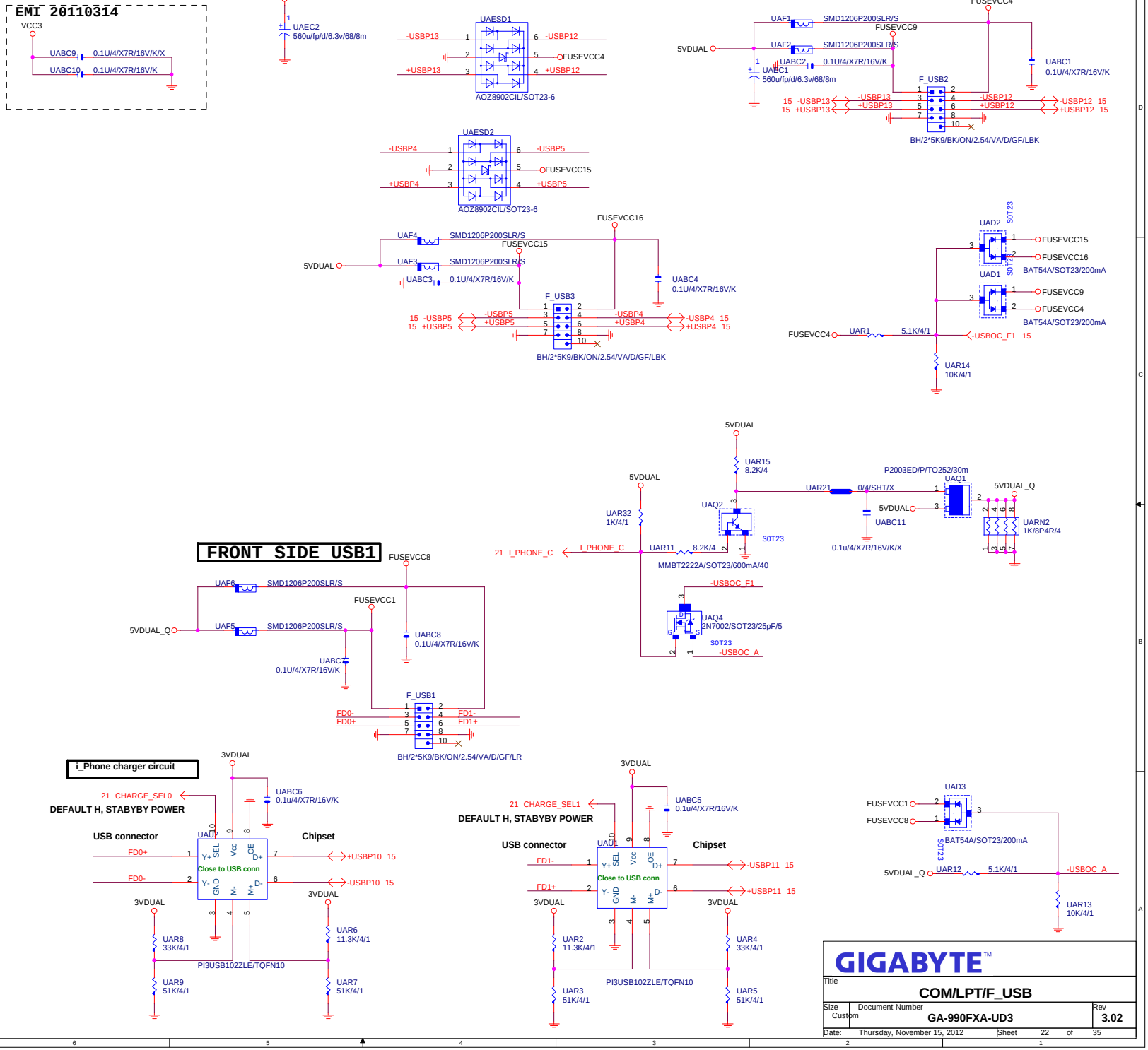


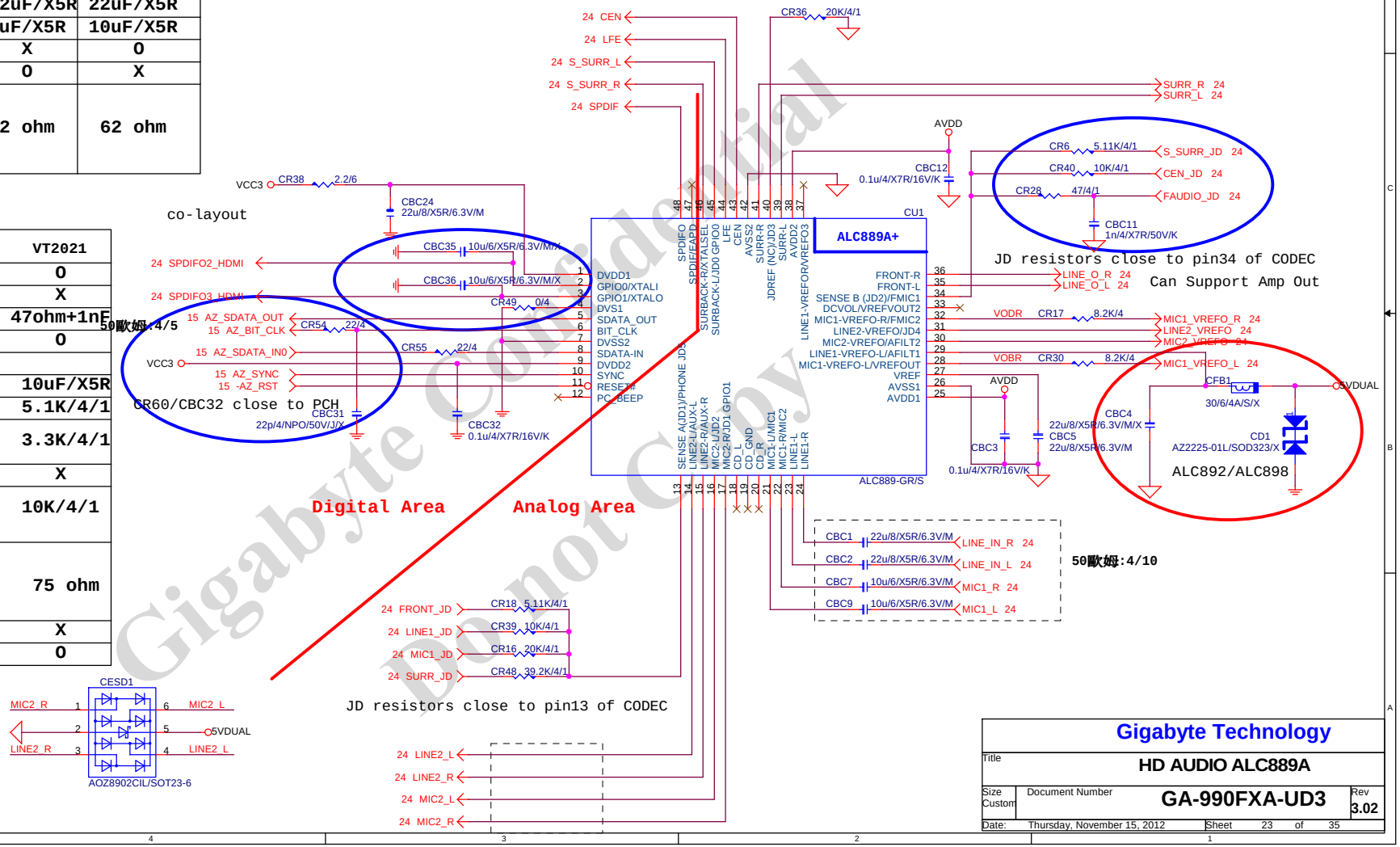
AZALIA CODEC

ALC889/ALC889B/ALC892/ALC898 Colay

	ALC889	ALC889B	ALC898/ALC892
CR65	0	0	X
CBC35	X	X	10uF/X5R
CBC39	X	10uF/X5R	X
CR31	0	X	0
CR66	X	0	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R
CBC5/CBC6/CBC9/CBC11	10uF/X5R	10uF/X5R	10uF/X5R
CR51/CD1/CBC7	X	X	0
CD2/CD3/CQ3/CQ5	0	0	X
CR5/CR8/CR1/CR14/ CR17/CR22/CR45/CR33/ CR47/CR40/CR26/CR37/ CR13/CR11/CR57/CR53	62 ohm	62 ohm	62 ohm

ALC889/VT2021 Colay

	ALC889	VT2021
CR49	0	0
CBC36	X	X
CR28/CBC11	47ohm+1nF	47ohm+1nF
CR52	0	0
CBC1/CBC2	22uF/X5R	10uF/X5R
CR36	20K/4/1	5.1K/4/1
CR17/CR30/ CR25/CR15/CR12/CR3/	8.2K/4	3.3K/4/1
CBC38/CBC39	X	X
CR10/CR8/CR20/CR45/ CR42/CR51/CR43/CR22/ CR27/CR26	22K/4	10K/4/1
CR7/CR9/CR5/CR13/ CR29/CR32/CR46/CR19/ CR50/CR41/CR21/CR47 CR2/CR11/CR14/CR24	62 ohm	75 ohm
CFB1/CD1/CBC4/CBC8	X	X
CD2/CD3/CQ3/CQ4	0	0



Gigabyte Technology	
Title	HD AUDIO ALC889A
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CODEC POWER/EMI PAD

EUP

5VDUAL — CD4 CD4148WP/1206/300mA — AVDD

CQ3 78L05/SOT89/0.1A

+12V — CD3 CD4148WP/1206/300mA

CR44 0/6/SHT/X

CBC38 0.01u/4/X7R/25V/K

CBC21 0.1u/4/X7R/16V/K/X

CBC8 22u/8/X5R/6.3V/M

CD2 AZ2225-01L/SOD323

ADD CD2 For ESD PROTECT DIODE

CR37 0/4/X

上ALC892時,此顆電容要保留

CR4 0/6/SHT/X

FUSEVCC14

23 SPDIF

OPTICAL

FR/5P/BK/T/D/S(GY)

23 SPDIFO2_HDMI — CR52 0/4 — SPDIFO_HDMI

23 SPDIFO3_HDMI — CR53 0/4/X

CBC37 100p/4/NPO/50V/J

PIN

SPDIF_O PH/1*2/BK/2.54/VA/D

For HDMI SPDIF

AZALIA JACK

BTX AZALIA CONNECTOR

11NR6-403007-21R

AUDIOB

23 LINE1_JD — LINE1_JD — AJ_A5 — AJ_A2 — GND LINE-IN — BLUE LINE-IN

23 FRONT_JD — FRONT_JD — AJ_B5 — AJ_B2 — GND LINE-OUT — GREEN LINE-OUT

23 MIC1_JD — MIC1_JD — AJ_C5 — AJ_C2 — GND MIC-IN — PINK MIC-IN

2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

AUDIOA

23 CEN_JD — CEN_JD — BJ_B5 — BJ_B2 — GND REAR — Orange CEN/LFE

23 SURR_JD — SURR_JD — BJ_C5 — BJ_C2 — GND CEN — Black SURROUND

23 S_SURR_JD — S_SURR_JD — BJ_A5 — BJ_A2 — GND SIDE — Gray SURROUND SIDE

2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

LINE-OUT

23 LINE_O_R — CEC2 100u/OS/D/16V/66/30m — CR7 62/4

23 LINE_O_L — CEC3 100u/OS/D/16V/66/30m — CR9 62/4

CR10 22K/4 — CR8 22K/4 — AJ_B5 — AJ_B2

CBC23 180p/4/NPO/50V/J — CBC26 180p/4/NPO/50V/J

LINE-IN

23 LINE_IN_R — CR5 62/4 — AJ_A5

23 LINE_IN_L — CR13 62/4 — AJ_A2

CBC18 180p/4/NPO/50V/J — CBC27 180p/4/NPO/50V/J

MIC-IN

23 MIC1_R — CR29 62/4 — AJ_C5

23 MIC1_L — CR32 62/4 — AJ_C2

23 MIC1_VREFO_L

23 MIC1_VREFO_R

CBC19 180p/4/NPO/50V/J — CBC22 180p/4/NPO/50V/J

SURROUND

EMI

23 SURR_R — CEC5 100u/OS/D/16V/66/30m — CR46 62/4

23 SURR_L — CEC7 100u/OS/D/16V/66/30m — CR19 62/4

CR20 22K/4 — CR45 22K/4 — BJ_C5 — BJ_C2

CBC29 180p/4/NPO/50V/J — CBC28 180p/4/NPO/50V/J

CEN/LFE

EMI

23 LFE — CEC9 100u/OS/D/16V/66/30m — CR50 62/4

23 CEN — CEC10 100u/OS/D/16V/66/30m — CR41 62/4

CR42 22K/4 — CR51 22K/4 — BJ_B5 — BJ_B2

CBC25 180p/4/NPO/50V/J — CBC34 180p/4/NPO/50V/J

SURR BACK

EMI

23 S_SURR_R — CEC8 100u/OS/D/16V/66/30m — CR21 62/4

23 S_SURR_L — CEC4 100u/OS/D/16V/66/30m — CR47 62/4

CR43 22K/4 — CR22 22K/4 — BJ_A5 — BJ_A2

CBC33 180p/4/NPO/50V/J — CBC30 180p/4/NPO/50V/J

AZALIA FRONT PANEL

CQ2 BAT54A/SOT23/200mA — 23 LINE2_VREFO — CR25 8.2K/4 — CR15 8.2K/4

CQ1 BAT54A/SOT23/200mA — 23 MIC2_VREFO — CR12 8.2K/4 — CR3 8.2K/4

EMI

23 MIC2_L — CBC20 10u/6/X5R/6.3V/M — CR2 62/4 — M2_L

23 MIC2_R — CBC15 10u/6/X5R/6.3V/M — CR11 62/4 — M2_R

23 FAUDIO_JD — L2_R — CR14 62/4 — L2-R

L2_L — CR24 62/4 — L2-L

CR1 0/4/X

F_AUDIO

CR27 22K/4 — CR26 22K/4

Digital Area — VCC3 — CR56 8.2K/4 — C_-ACZ_DET

CR35 20K/4/1 — CR31 39.2K/4/1

bh/2*5k8/bk/2.54/va/[11NH3-000205-P1R]

23 LINE2_R — CEC6 100u/OS/D/16V/66/30m — L2_R

23 LINE2_L — CEC1 100u/OS/D/16V/66/30m — L2_L

CBC10 180p/4/NPO/50V/J — CBC16 180p/4/NPO/50V/J — CBC17 180p/4/NPO/50V/J — CBC6 180p/4/NPO/50V/J

Gigabyte Technology

Title: AUDIO JACK

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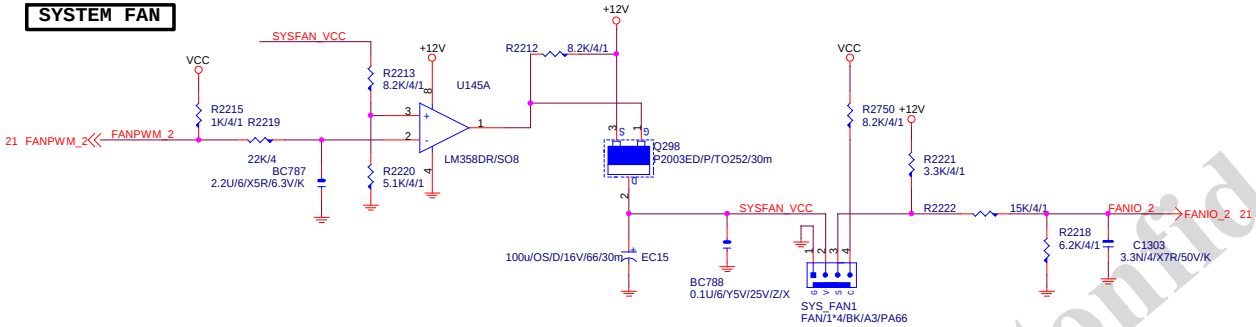
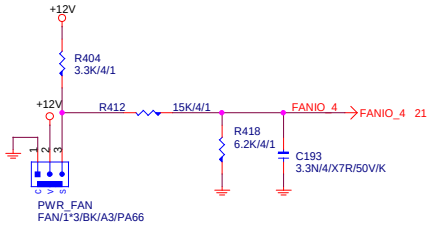
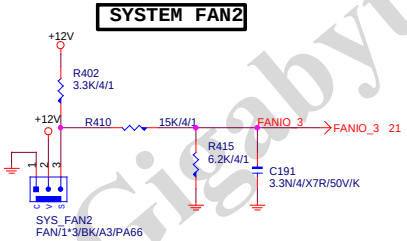
SYSTEM FAN



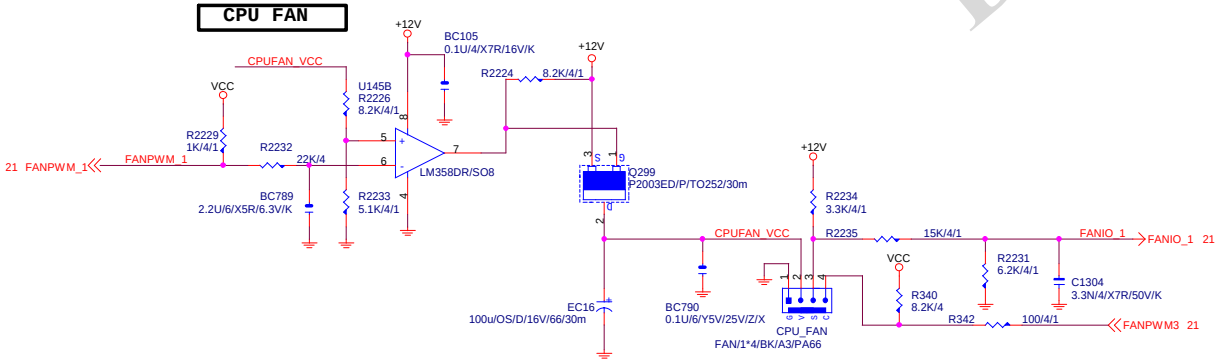
POWER FAN



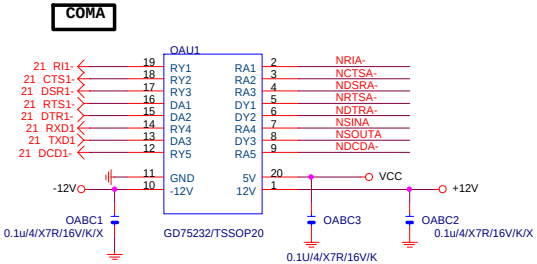
SYSTEM FAN2



CPU FAN

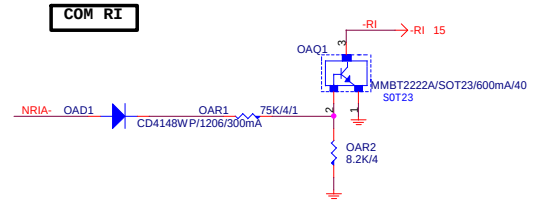


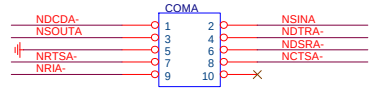
COMA



EMI 20120730

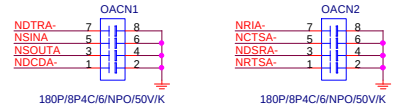
COM RI





BH/2*5K10/BK/2.54/VA/COM

11NH3-000205-Y1R/Y2R



GIGABYTE™

Title	FAN/HWMO/COM	
Size: Custom	Document Number: GA-990FXA-UD3	Rev: 3.02
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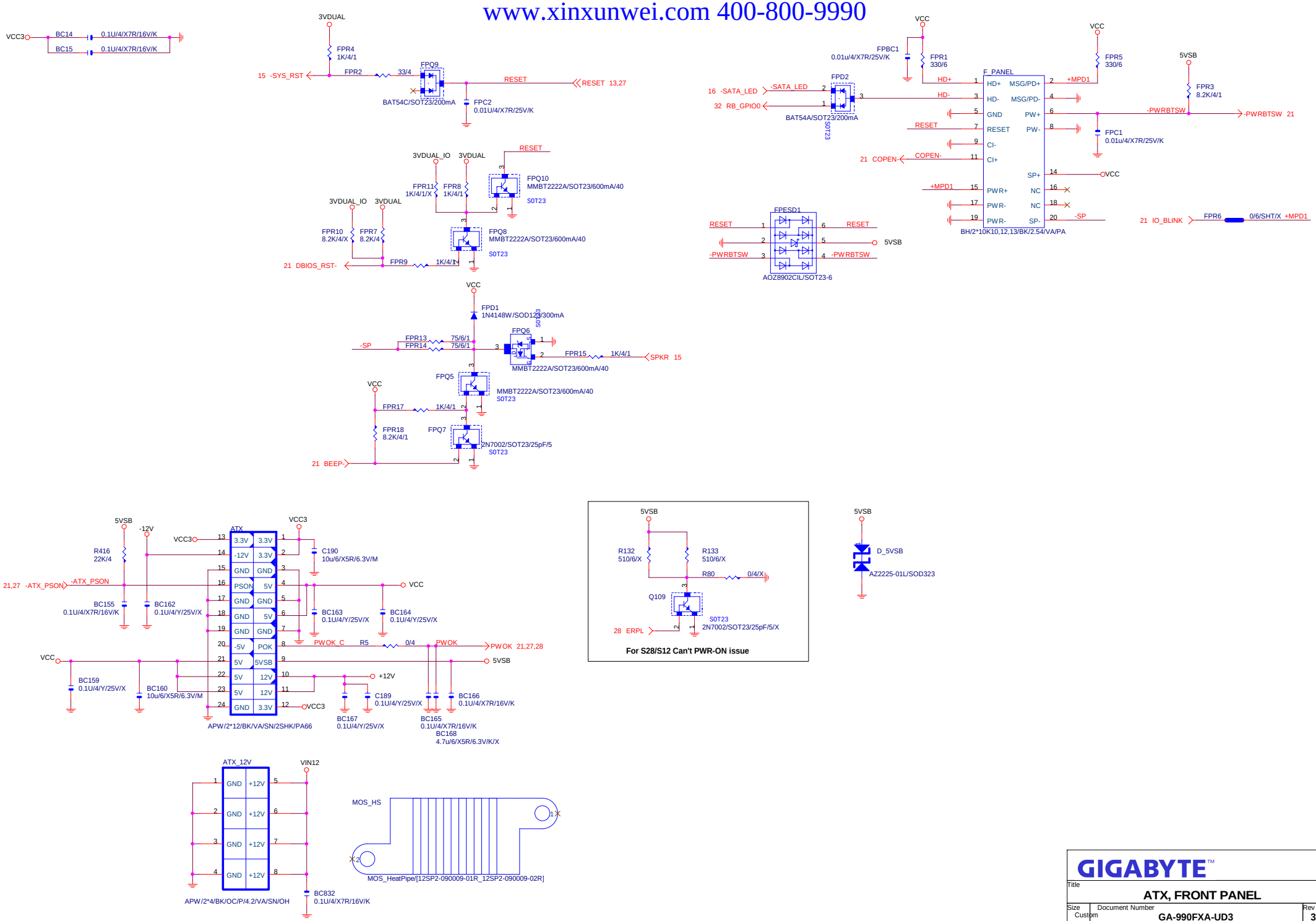

GIGABYTE™

Title: ATX, FRONT PANEL

Size	Document Number	Rev
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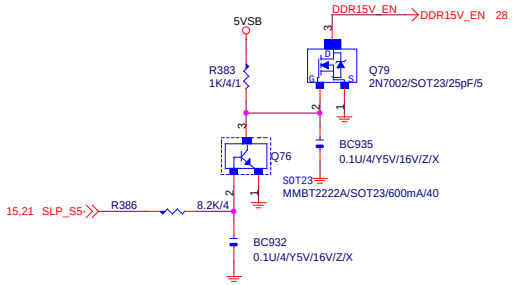

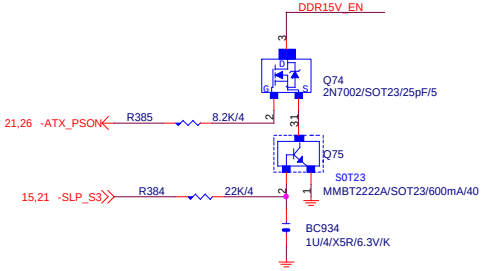

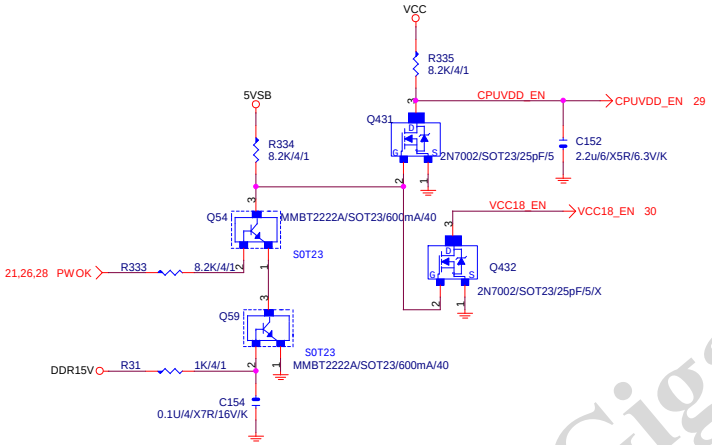

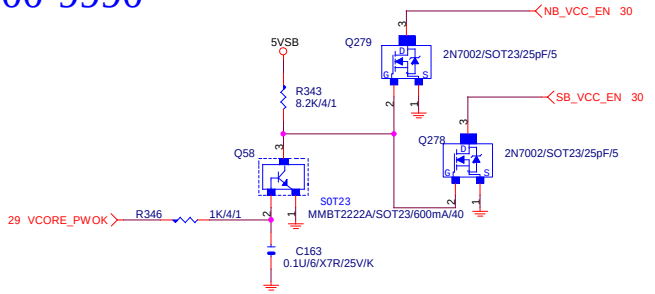

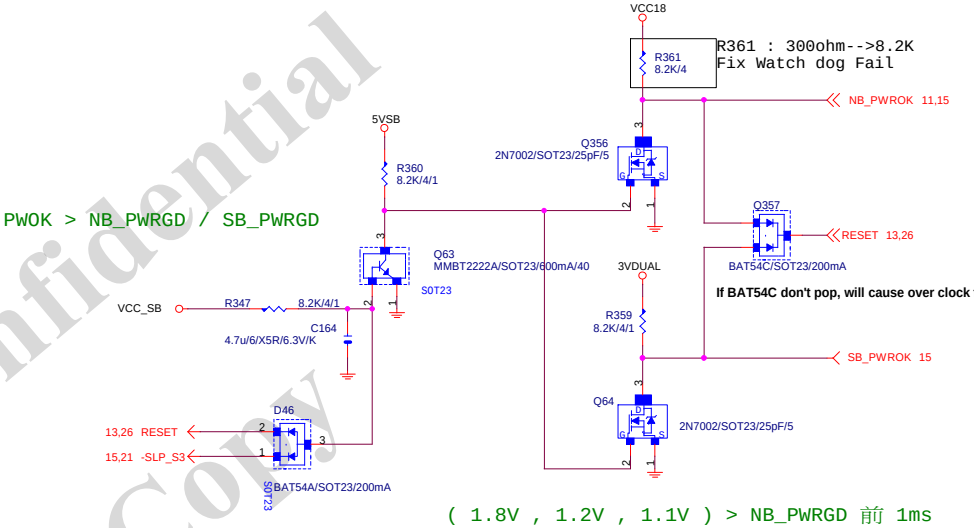

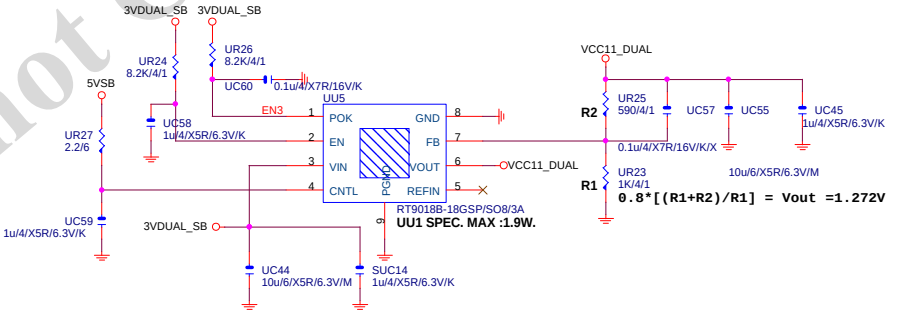

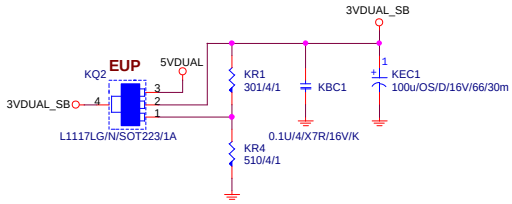

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Title: POWER SEQUENCE		
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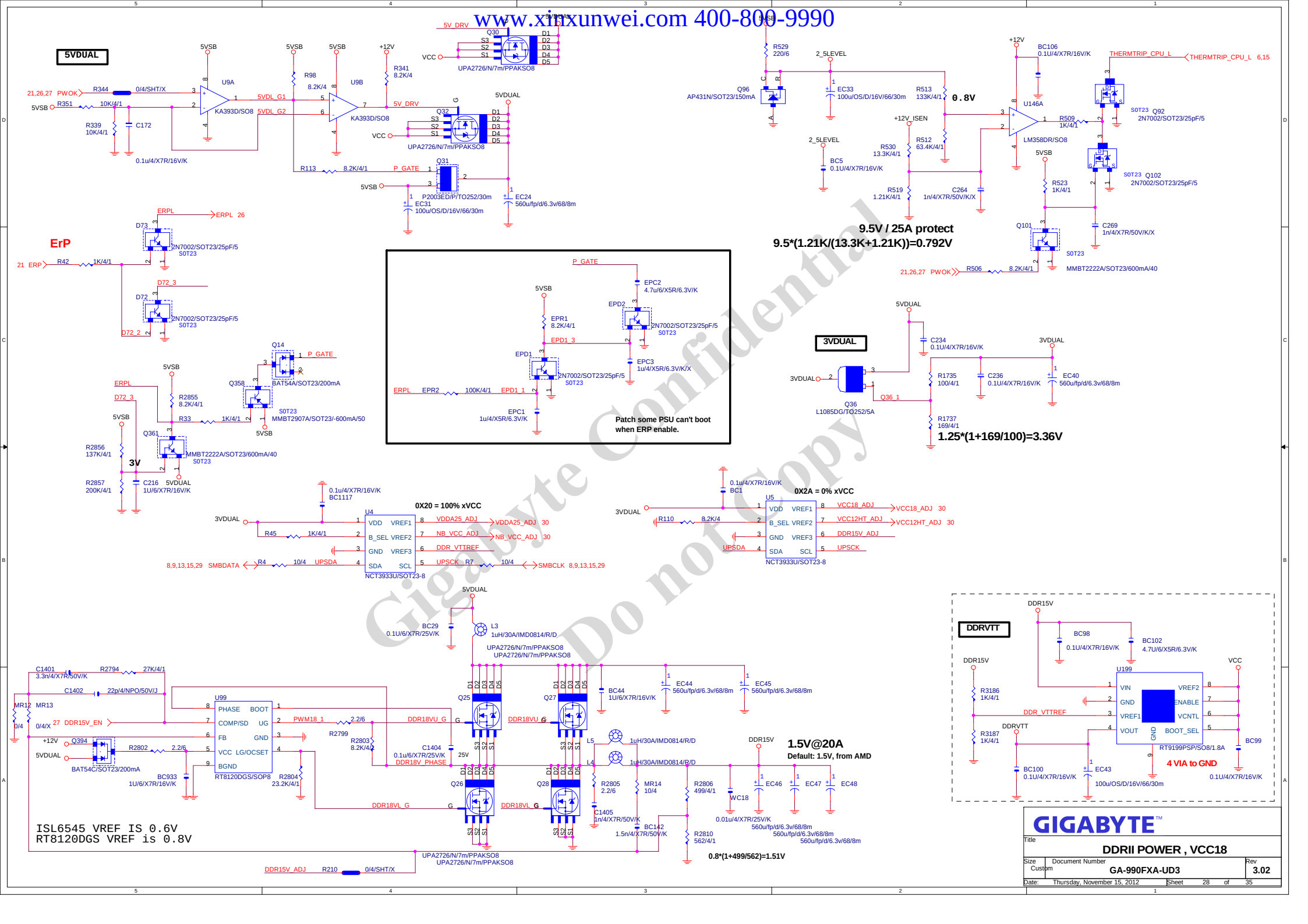

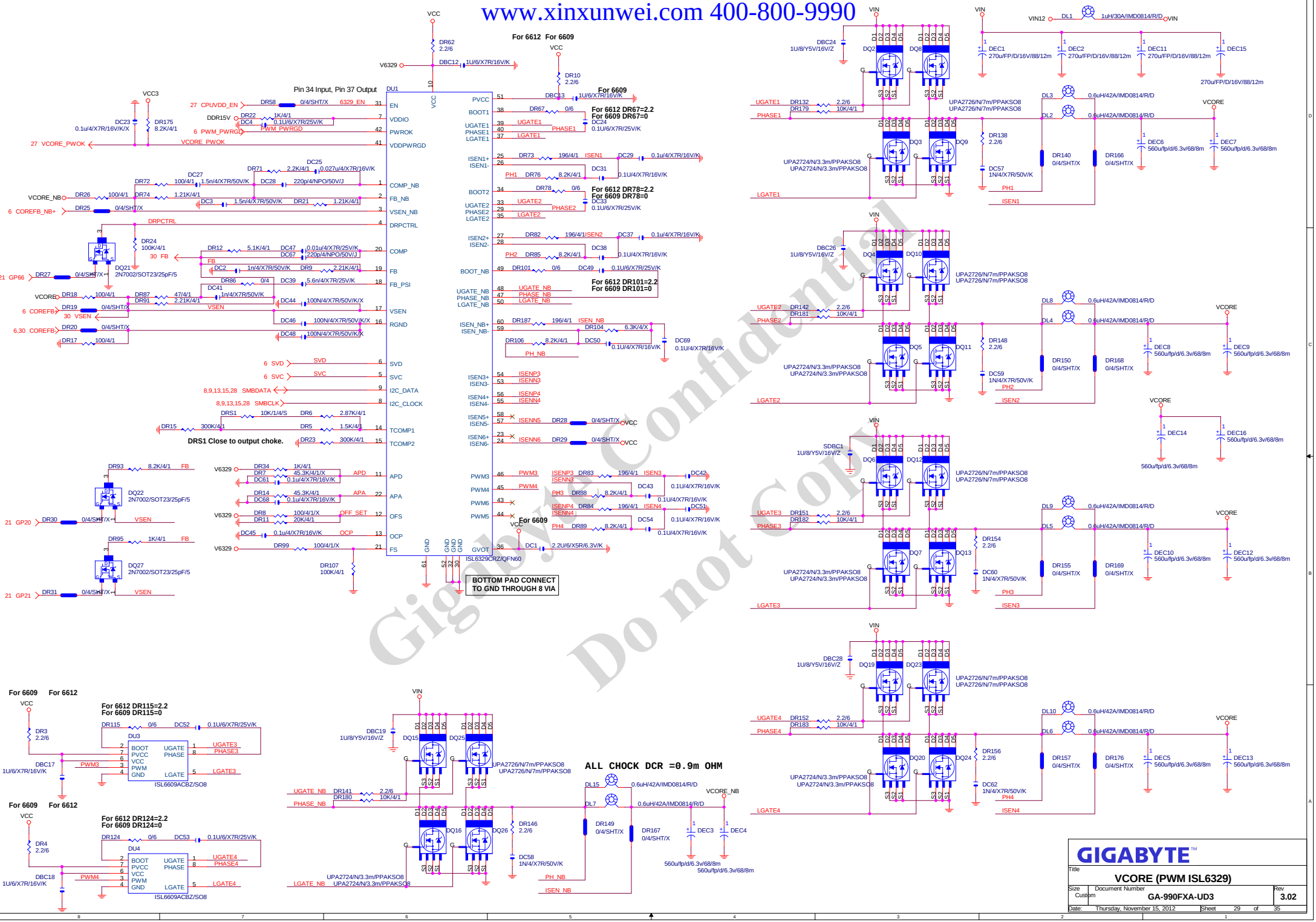

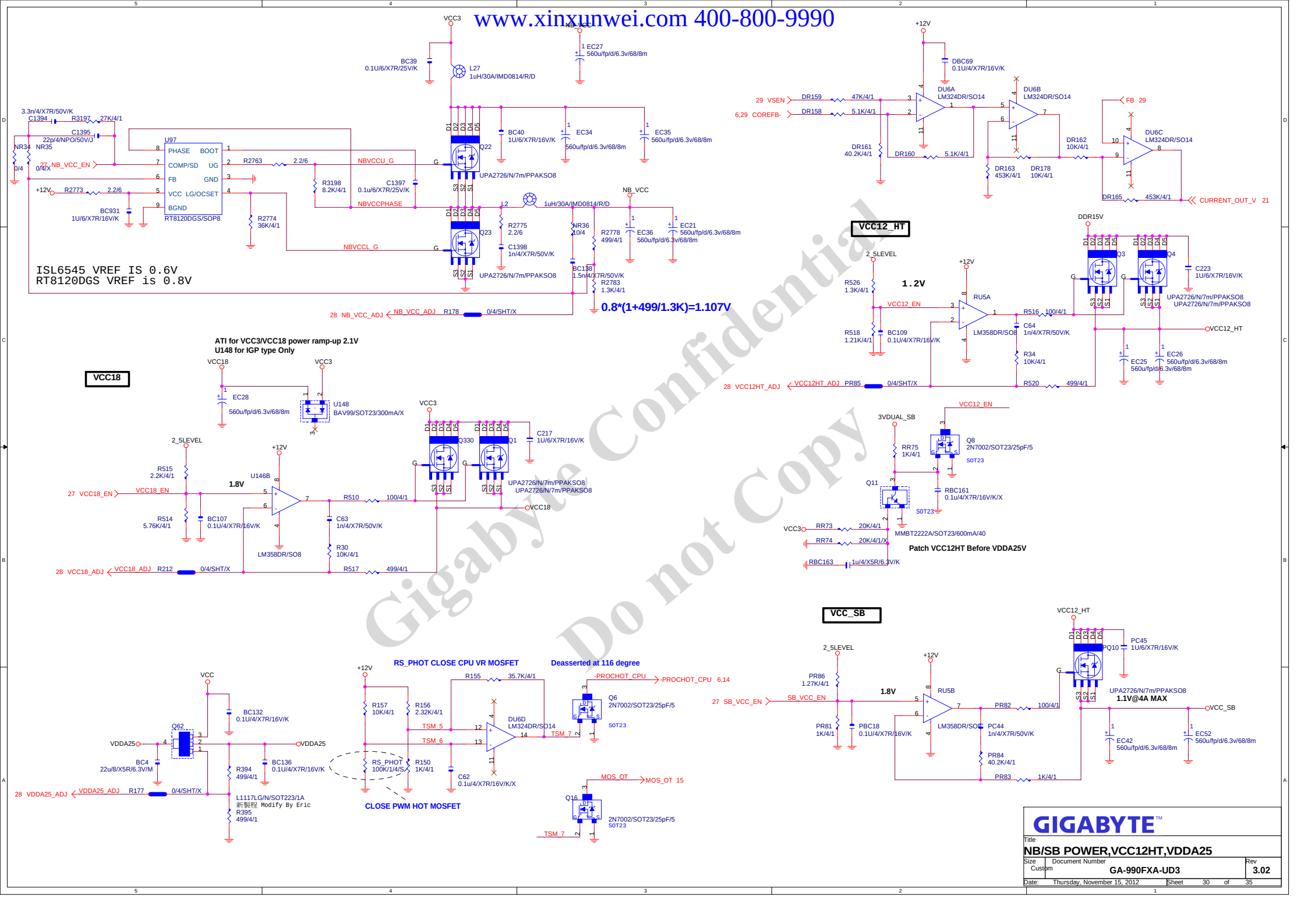

Title	NB/SB POWER,VCC12HT,VDDA25
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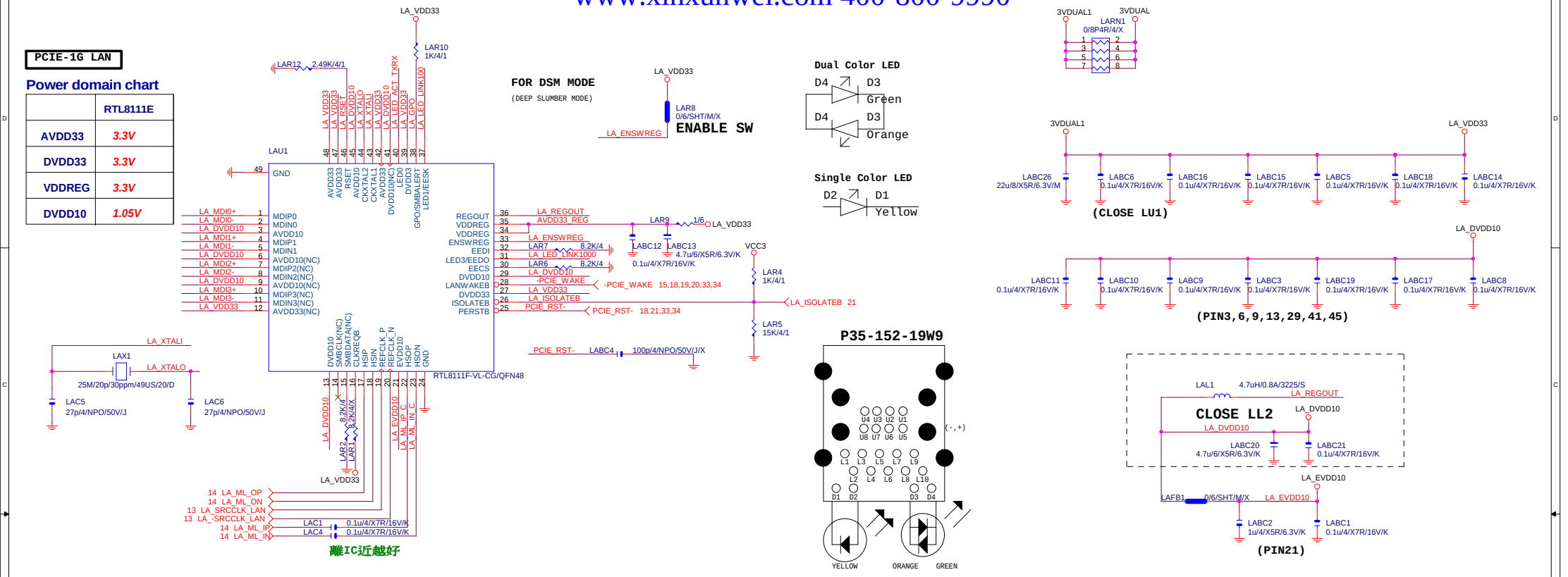
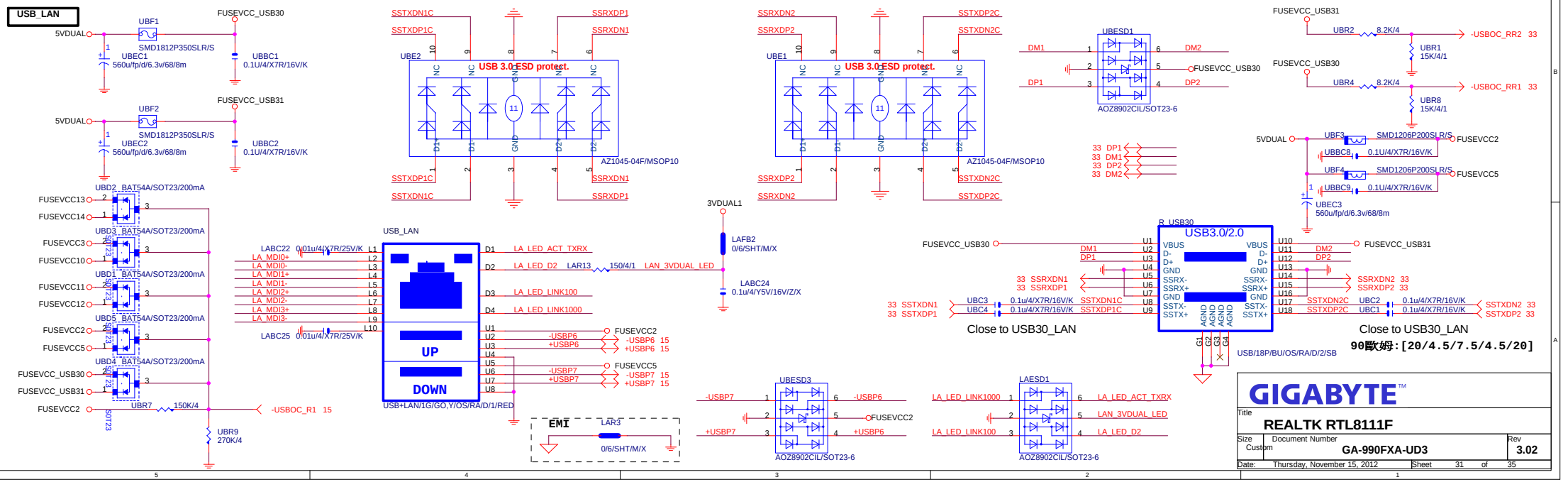
PCIE-1G LAN

Power domain chart

	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V



USB_LAN



Title	REALTK RTL8111F
Size	Custom
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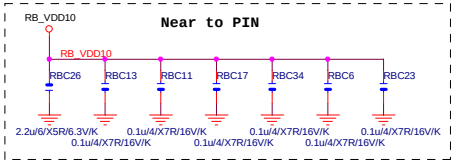

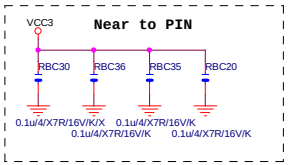

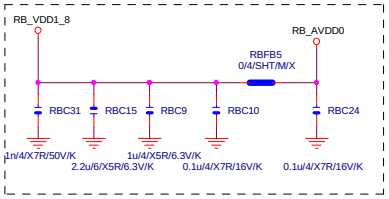

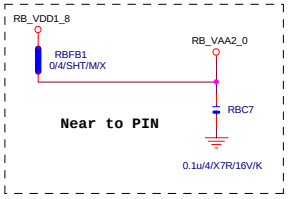

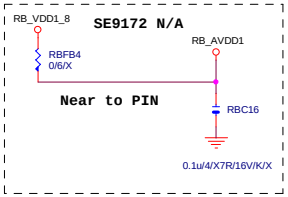

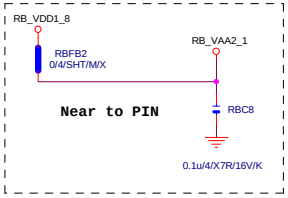

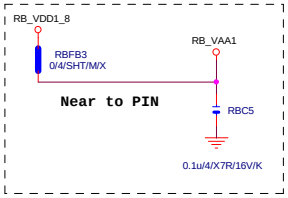

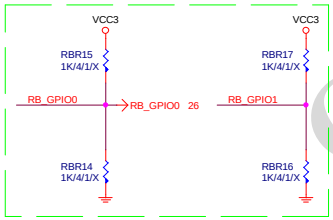

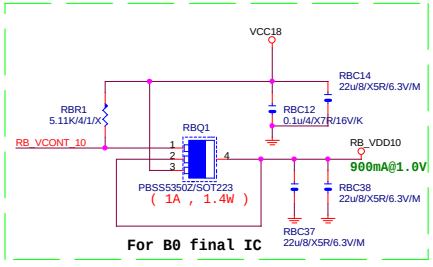

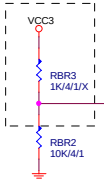

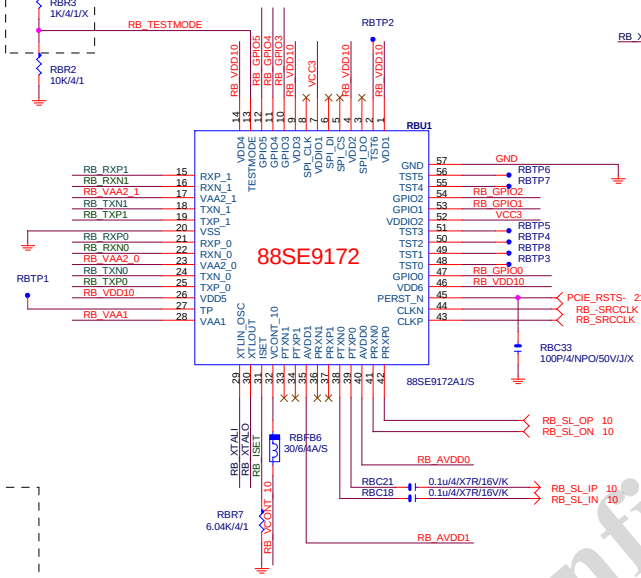

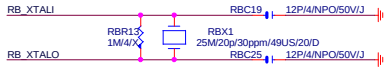

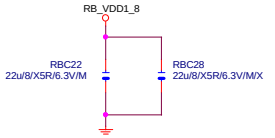

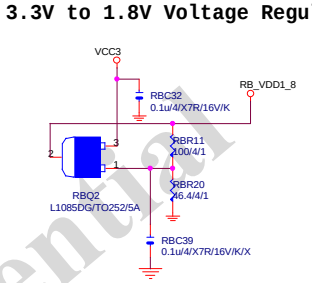

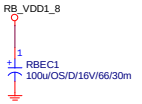

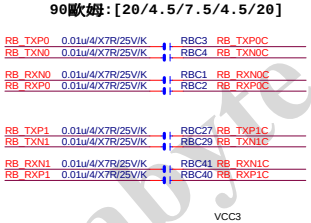

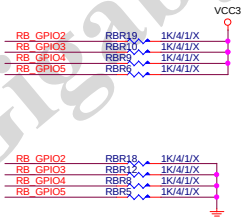

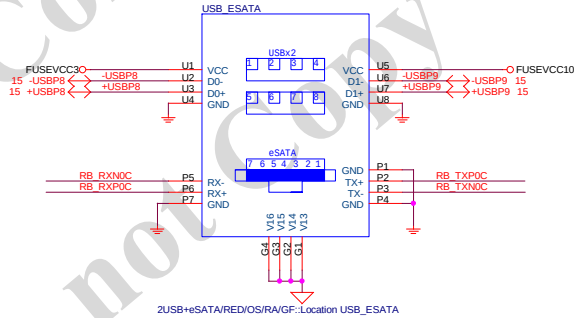

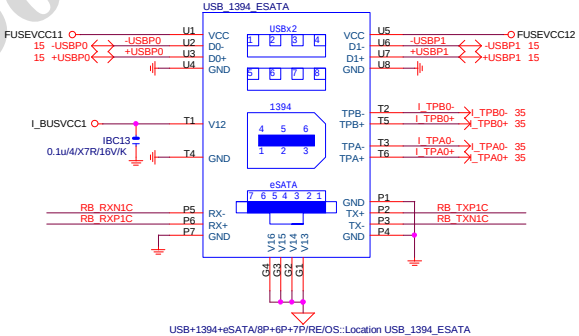

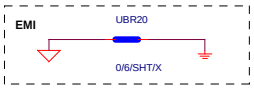

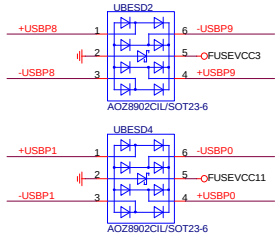

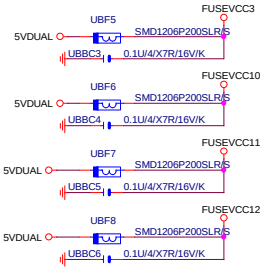

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Title: Marvell 9172_ESATA			
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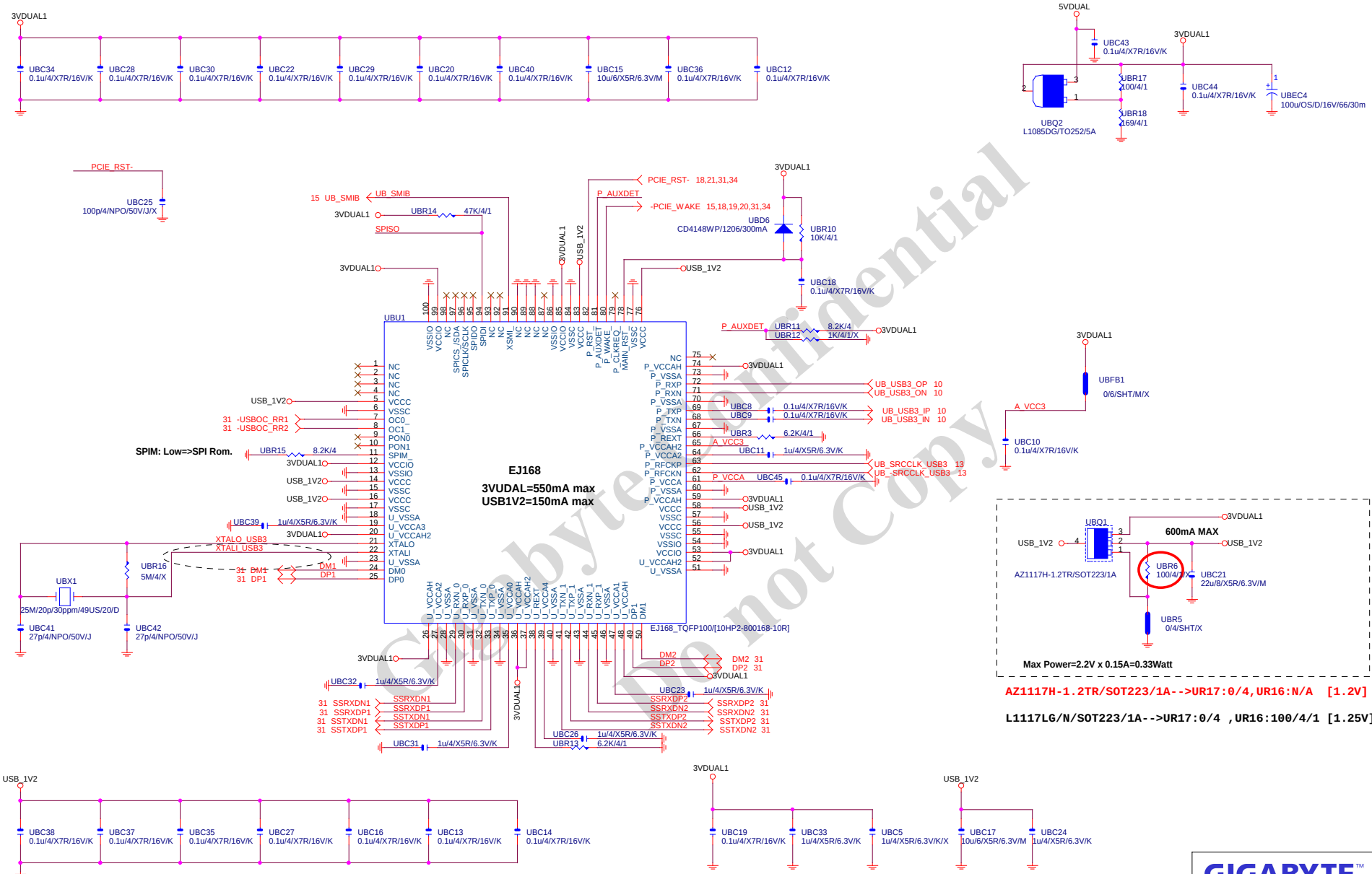

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Title: EJ168 R_USB30		
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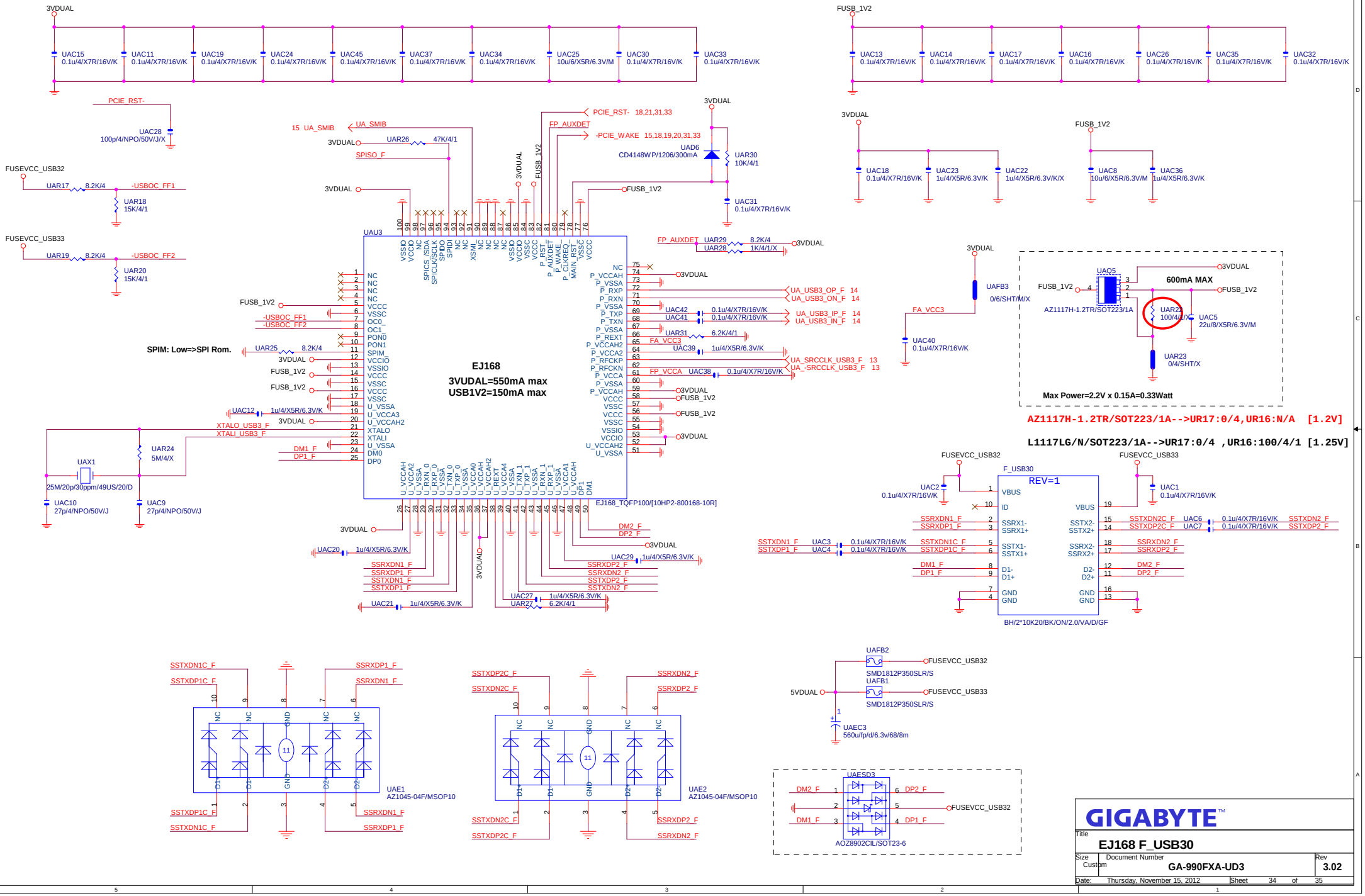

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Title	EJ168 F_USB30	
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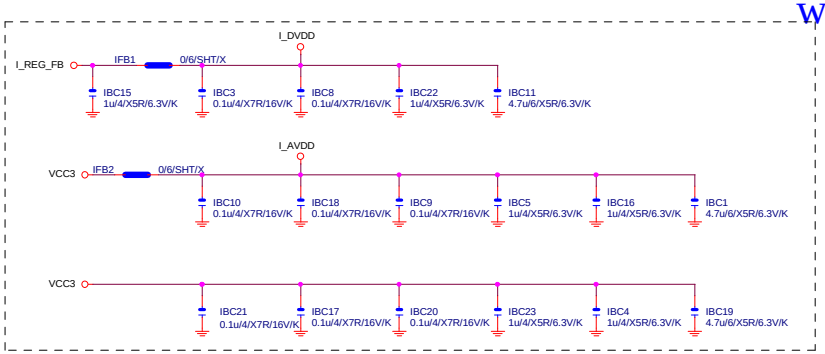
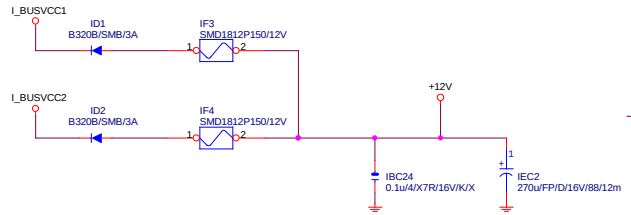
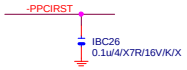
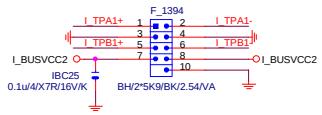
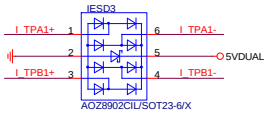


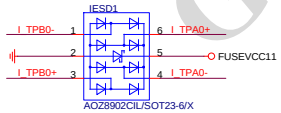




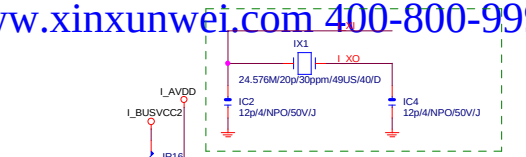


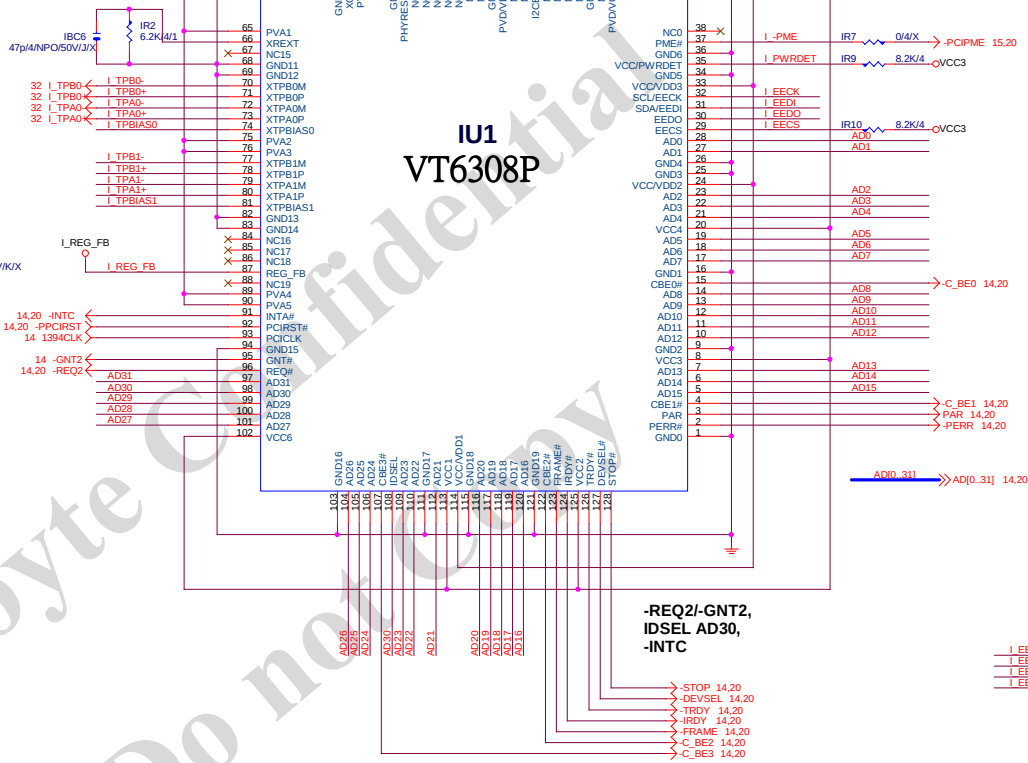


Place close to Header or connector

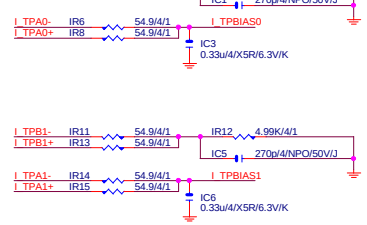


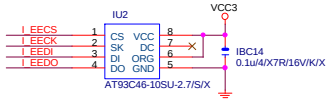
Place close to Header or connector





-REQ2/-GNT2,
IDSEL AD30,
-INTC





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