Compal Confidential

Schematics Document

Intel Huron River Platform
Sandy Bridge (Dual Core BGA 1023) With
Couger Point Core Logic

LA-7401P

2011-03-24

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

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Title: Cover Page

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Custom		1.0

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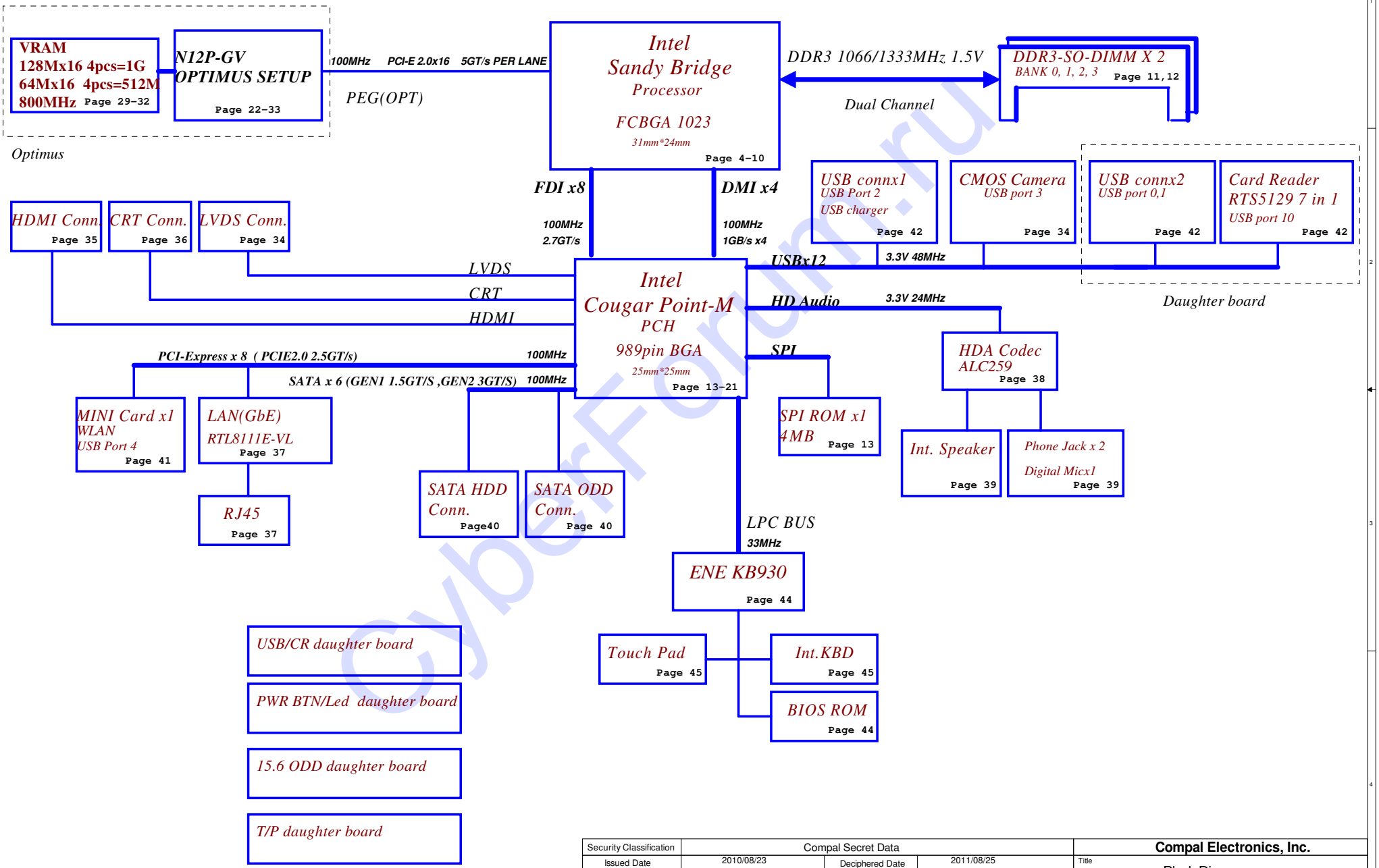
Model Name : PAJ80(14" UMA/Dis)/PAJ90(15.6" UMA/Dis)
File Name : LA-7401P



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Title: Block Diagrams

Size: Custom | Document Number: LA-7401P | Rev: 1.0

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_DGPU	+1.05VS to +1.05VS_DGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS	+VCCPP to +1.05VS switched power rail for CPU,PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+VRAM_1.5VS	+1.5V to +VRAM_1.5VS power rail for GPU	ON	OFF	OFF
+1.8VS	+5VALW to 1.8VS switched power rail to CPU,PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+LAN_IO	+3VALW to +LAN_IO power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 1.1	Port	2 External USB Port
EHCI1	UHCI0	0	CONN
		1	CONN
	UHCI1	2	CONN
		3	Camera
	UHCI2	4	Mini Card(WLAN/BT)
		5	NA
	UHCI3	6	
		7	
EHCI2	UHCI4	8	NA
		9	NA
	UHCI5	10	Card Reader
		11	
	UHCI6	12	
		13	

BTO Option Table

BTO Item	BOM Structure
Optimus	OPT@
Connector	CONN@
Unpop	@
14" PCB	14@
15.6" PCB	15@
UMA PCB	UMA@
Dis PCB (Optimus)	OPT@
X76 512M	512M@
X76 1G	1G@

2410M mean 2.3G CPU 2540M mean 2.6G CPU 2520M mean 2.5G CPU 2310M mean 2.2G CPU 2620M mean 2.7G CPU 2330M mean 2.2G CPU PCH R3 GPU R3

U2 2410MR3@ 2410M CPU
U2 2540MR3@ 2540M CPU
U2 2520MR3@ 2520M CPU
U2 2310MR3@ 2310M CPU
U2 2620MR3@ 2620M CPU
U14 PCHR3@ PCH B3
UV1 GPUR3@ GPU

U2 2410MR1@ 2410M CPU
U2 2540MR1@ 2540M CPU
U2 2520MR1@ 2520M CPU
U2 2310MR1@ 2310M CPU
U2 2620MR1@ 2620M CPU
U2 2330M@ 2330M CPU
U14 PCHR1@ PCH B3
UV1 GPUR1@ GPU

PCB DAZ
ZZZ1
PCB_LA-7401P

X7613432L03
ZZZ3
X76-VRAM
1G@

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9E H	1001 1110 b

SMBUS Control Table

	SOURCE	BATT	CPU THERMAL SENSOR	SODIMM 0 SODIMM 1	WLAN WWAN	LCD DDC ROM	HDMI DDC ROM	PCH	GPU
EC_SMB_CK1 EC_SMB_DA1	KB930	V							
EC_SMB_CK2 EC_SMB_DA2	KB930							V	V
PCH_LCD_CLK PCH_LCD_DATA	PCH					V			
SDVO_SCLK SDVO_SDATA	PCH						V		
PCH_SMBCLK PCH_SMBDATA	PCH			V	V				

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Title: Notes List

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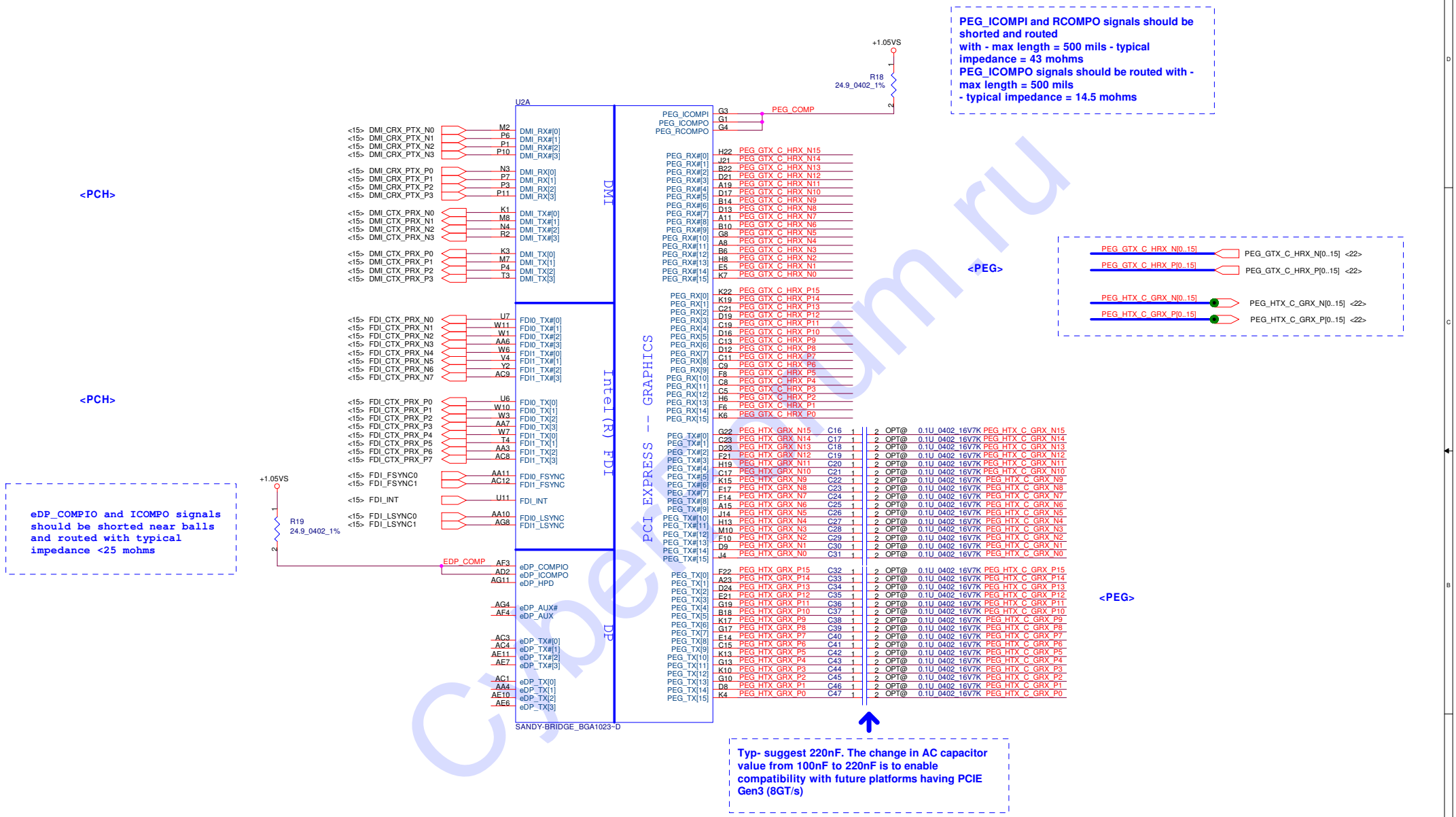

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Compal Electronics, Inc.			
Title: PROCESSOR(1/7) DMI,FDI,PEG			
Size: Custom	Document Number		Rev: 1.0
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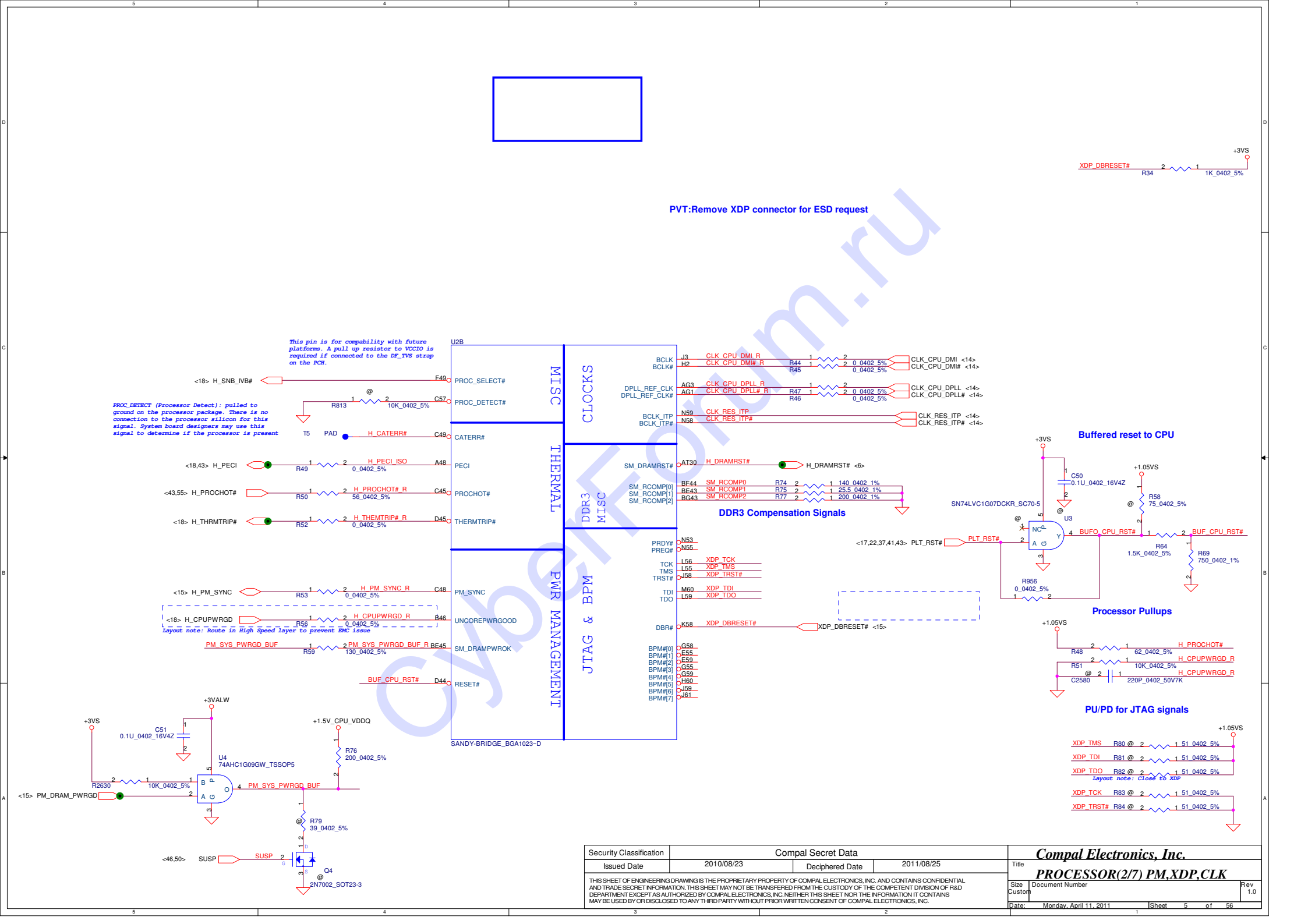

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Title	Compal Electronics, Inc.		
	PROCESSOR(2/7) PM,XDP,CLK		
Size	Document Number		Rev
Custom			1.0
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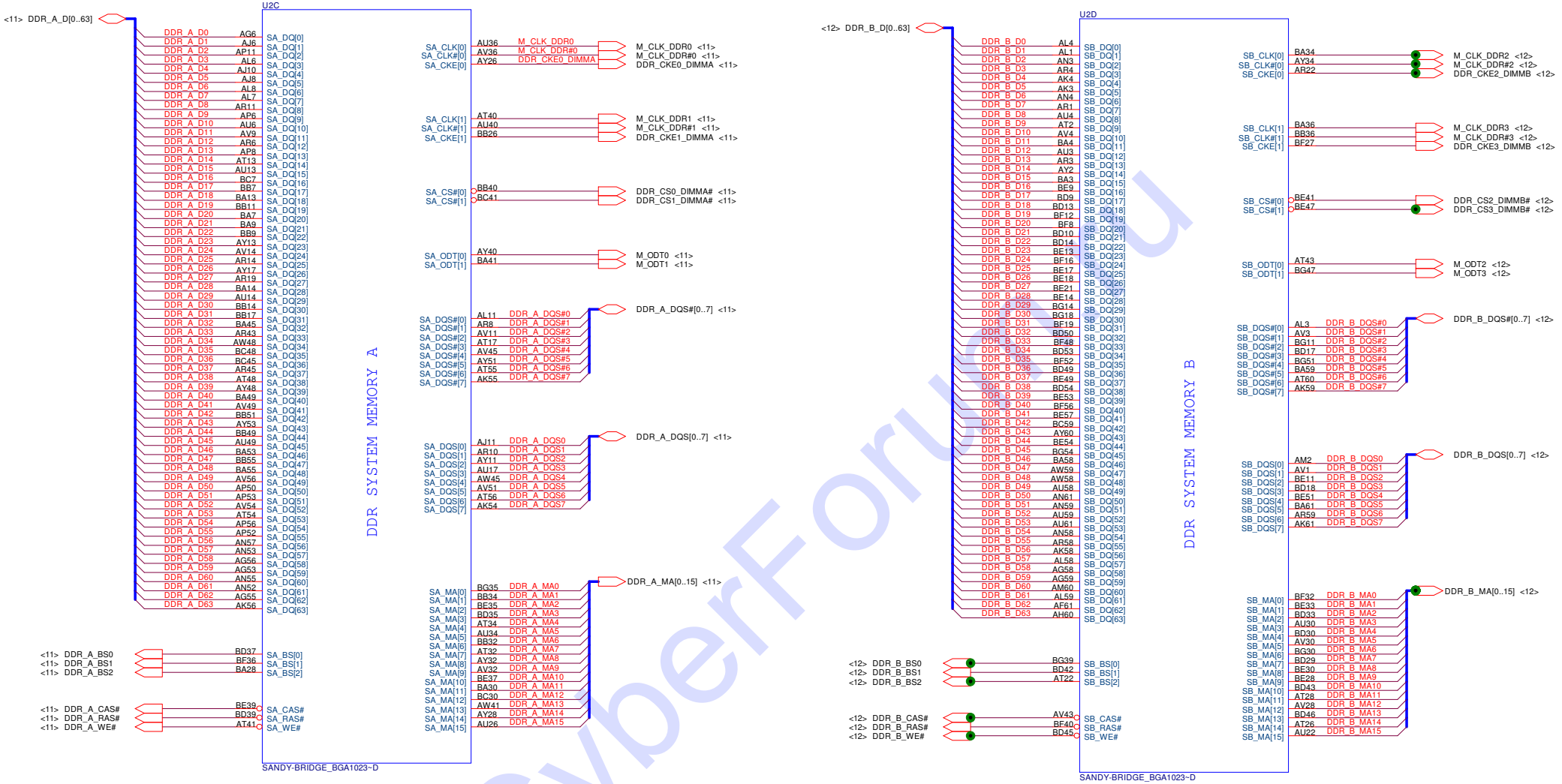

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Title: **PROCESSOR(3/7) DDRIII**

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Custom		1.0

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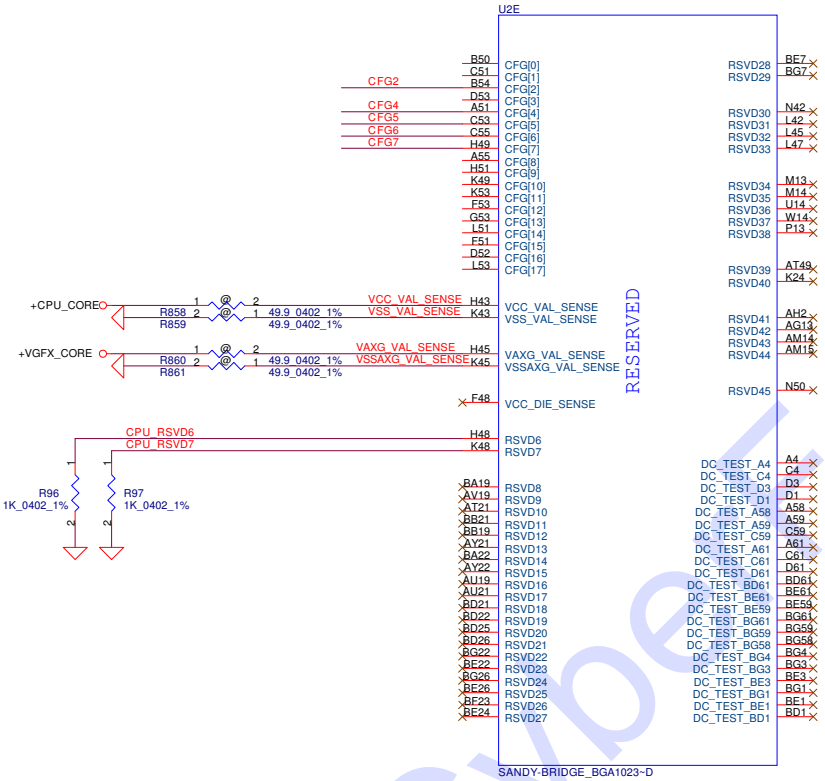
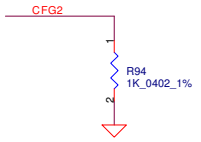
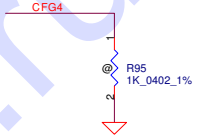
CFG Straps for Processor

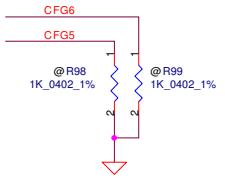




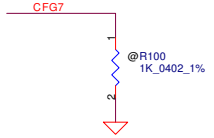
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/7) RSVD,CFG

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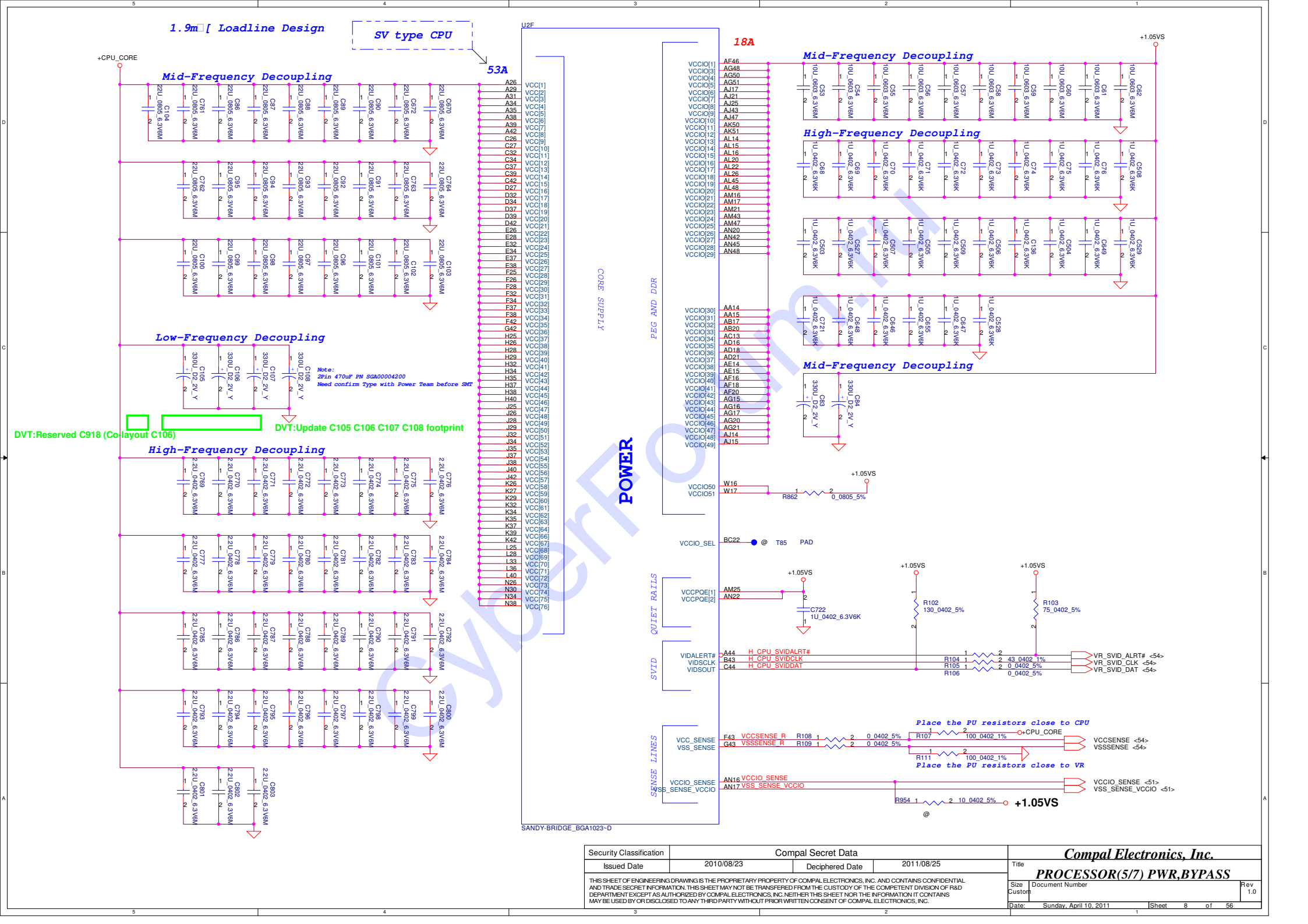

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Title: PROCESSOR(5/7) PWR,BYPASS

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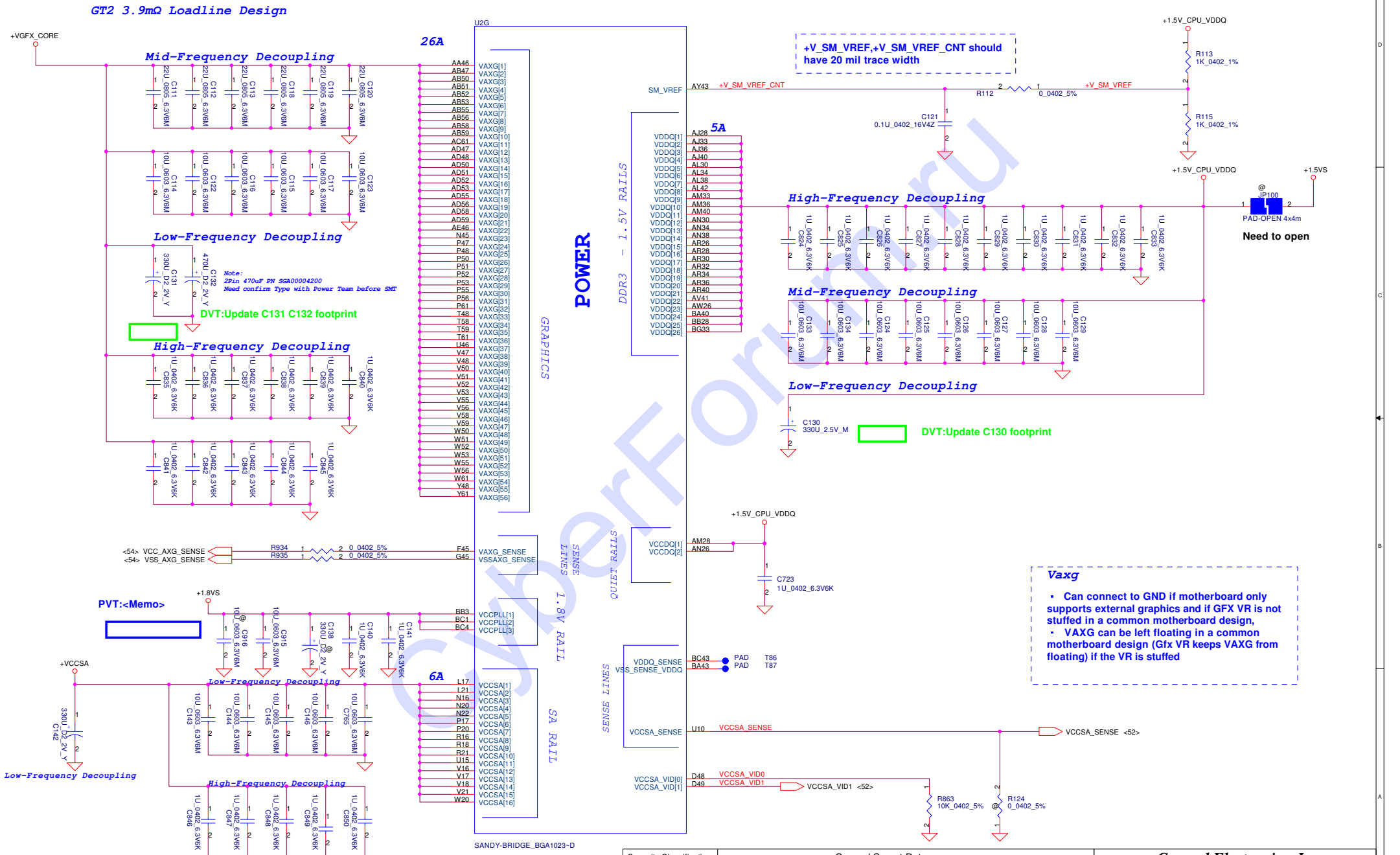

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Title: PROCESSOR(6/7) PWR			
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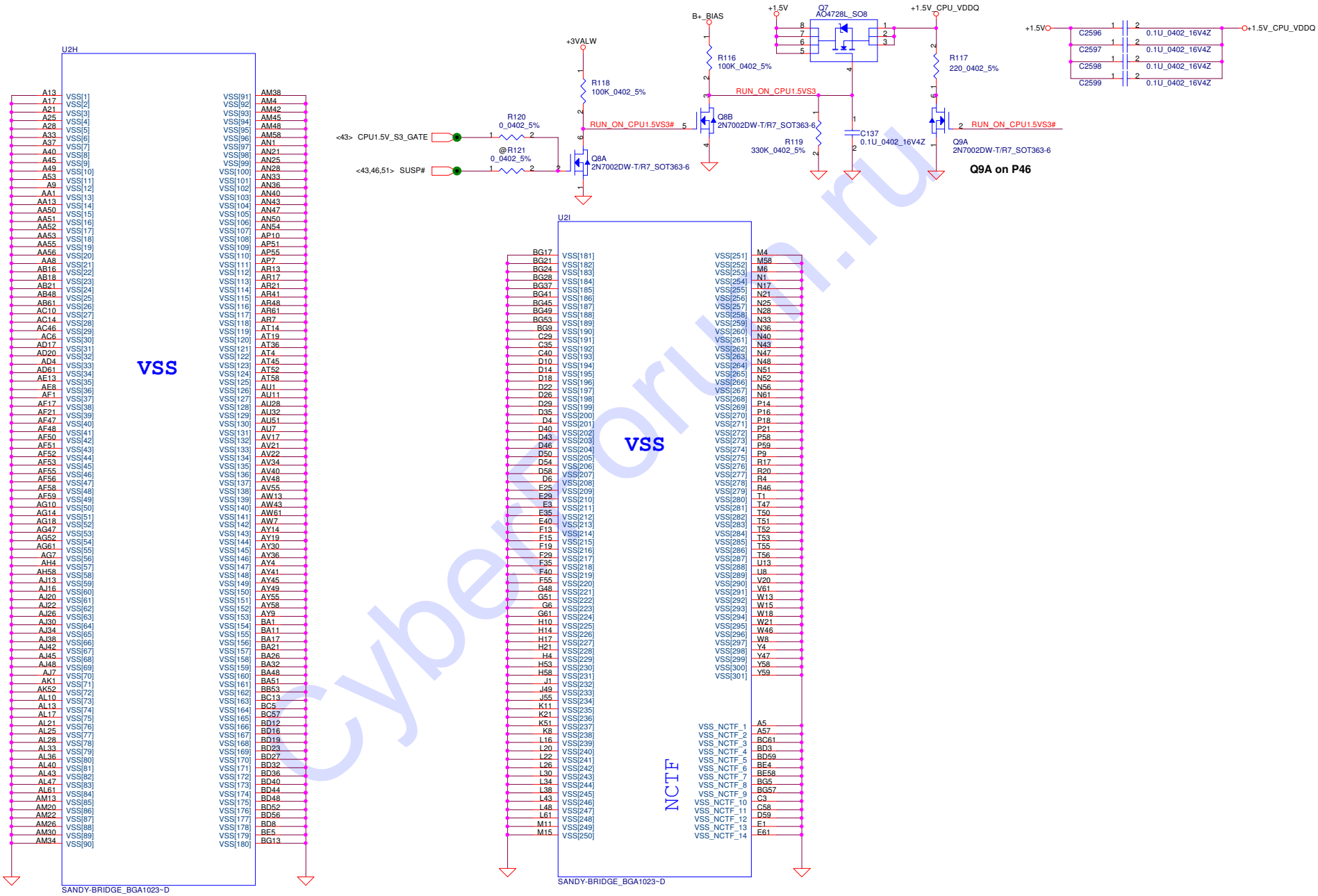
+1.5V_CPU_VDDQ Source



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Title: **PROCESSOR(7/7) VSS**

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All VREF traces should have 10 mil trace width

+1.5V +VREF_DQ_DIMMA

R2017 1K_0402_1%

R2018 1K_0402_1%

+1.5V +VREF_CA_DIMMA

R2609 1K_0402_1%

R2612 1K_0402_1%

+VREF_DQ_DIMMA +1.5V +1.5V

C2023 2.2U_0603_6.3V6K

C2000 0.1U_0402_16V4Z

JDIMM0

	VREF_DQ	1	2	VSS1	
DDR_A_D0	VSS2	3	4	DQ4	DDR_A_D4
DDR_A_D1	DQ0	5	6	DQ5	DDR_A_D5
	DQ1	7	8	VSS3	
DDR_A_DM0	VSS4	9	10	DQS#0	DDR_A_DQS#0
	DM0	11	12	DQS0	DDR_A_DQS0
DDR_A_D2	VSS5	13	14	VSS6	
DDR_A_D3	DQ2	15	16	DQ6	DDR_A_D6
	DQ3	17	18	DQ7	DDR_A_D7
DDR_A_D8	VSS7	19	20	VSS8	
DDR_A_D9	DQ8	21	22	DQ12	DDR_A_D12
	DQ9	23	24	DQ13	DDR_A_D13
DDR_A_DQS#1	VSS9	25	26	VSS10	
DDR_A_DQS1	DQS#1	27	28	DM1	DDR_A_DM1
	DQS1	29	30	RESET#	DDR3_DRAMRST#
DDR_A_D10	VSS11	31	32	VSS12	
DDR_A_D11	DQ10	33	34	DQ14	DDR_A_D14
	DQ11	35	36	DQ15	DDR_A_D15
DDR_A_D16	VSS13	37	38	VSS14	
DDR_A_D17	DQ16	39	40	DQ20	DDR_A_D20
	DQ17	41	42	DQ21	DDR_A_D21
DDR_A_DQS#2	VSS15	43	44	VSS16	
DDR_A_DQS2	DQS#2	45	46	DM2	DDR_A_DM2
	DQS2	47	48	VSS17	
DDR_A_D18	VSS18	49	50	DQ22	DDR_A_D22
DDR_A_D19	DQ18	51	52	DQ23	DDR_A_D23
	DQ19	53	54	VSS19	
DDR_A_D24	VSS20	55	56	DQ28	DDR_A_D28
DDR_A_D25	DQ24	57	58	DQ29	DDR_A_D29
	DQ25	59	60	VSS21	
DDR_A_DM3	VSS22	61	62	DQS#3	DDR_A_DQS#3
	DM3	63	64	DQS3	DDR_A_DQS3
DDR_A_D26	VSS23	65	66	VSS24	
DDR_A_D27	DQ26	67	68	DQ30	DDR_A_D30
	DQ27	69	70	DQ31	DDR_A_D31
	VSS25	71	72	VSS26	
<6> DDR_CKE0_DIMMA	DDR_CKE0_DIMMA	73	74	CKE1	DDR_CKE1_DIMMA
	CKE0	75	76	VDD2	DDR_CKE1_DIMMA <6>
	VDD1	77	78	A15	DDR_A_MA15
<6> DDR_A_BS2	NC1	79	80	A14	DDR_A_MA14
	BA2	81	82	VDD4	
DDR_A_MA12	VDD3	83	84	A11	DDR_A_MA11
DDR_A_MA9	A12/BC#	85	86	A7	DDR_A_MA7
	A9	87	88	VDD6	
DDR_A_MA8	VDD5	89	90	A6	DDR_A_MA6
DDR_A_MA5	A8	91	92	A4	DDR_A_MA4
	A5	93	94	VDD8	
DDR_A_MA3	VDD7	95	96	A2	DDR_A_MA2
DDR_A_MA1	A3	97	98	A0	DDR_A_MA0
	A1	99	100	VDD10	
<6> M_CLK_DDR0	VDD9	101	102	CK1	M_CLK_DDR1
<6> M_CLK_DDR#0	CK0	103	104	CK1#	M_CLK_DDR#1 <6>
	CK0#	105	106	VDD12	
DDR_A_MA10	VDD11	107	108	BA1	DDR_A_BS1
<6> DDR_A_BS0	A10/AP	109	110	RAS#	DDR_A_RAS# <6>
	BA0	111	112	VDD14	
<6> DDR_A_WE#	VDD13	113	114	S0#	DDR_CS0_DIMMA#
<6> DDR_A_CAS#	WE#	115	116	ODT0	M_ODT0 <6>
	CAS#	117	118	VDD16	
DDR_A_MA13	VDD15	119	120	ODT1	M_ODT1
<6> DDR_CS1_DIMMA#	A13	121	122	NC2	
	S1#	123	124	VDD18	
	VDD17	125	126	VREF_CA	+VREF_CA_DIMMA
	NCTEST	127	128	VSS28	
DDR_A_D32	VSS27	129	130	DQ36	DDR_A_D36
DDR_A_D33	DQ32	131	132	DQ37	DDR_A_D37
	DQ33	133	134	VSS30	
DDR_A_DQS#4	VSS29	135	136	DM4	DDR_A_DM4
DDR_A_DQS4	DQS#4	137	138	VSS31	
	DQS4	139	140	DQ38	DDR_A_D38
DDR_A_D34	VSS32	141	142	DQ39	DDR_A_D39
DDR_A_D35	DQ34	143	144	VSS33	
	DQ35	145	146	DQ44	DDR_A_D44
DDR_A_D40	VSS34	147	148	DQ45	DDR_A_D45
DDR_A_D41	DQ40	149	150	VSS35	
	DQ41	151	152	DQS#5	DDR_A_DQS#5
DDR_A_DM5	VSS36	153	154	DQS5	DDR_A_DQS5
	DM5	155	156	VSS38	
DDR_A_D42	VSS37	157	158	DQ46	DDR_A_D46
DDR_A_D43	DQ42	159	160	DQ47	DDR_A_D47
	DQ43	161	162	VSS40	
DDR_A_D48	VSS39	163	164	DQ52	DDR_A_D52
DDR_A_D49	DQ48	165	166	DQ53	DDR_A_D53
	DQ49	167	168	VSS42	
DDR_A_DQS#6	VSS41	169	170	DM6	DDR_A_DM6
DDR_A_DQS6	DQS#6	171	172	VSS43	
	DQS6	173	174	DQ54	DDR_A_D54
DDR_A_D50	VSS44	175	176	DQ55	DDR_A_D55
DDR_A_D51	DQ50	177	178	VSS45	
	DQ51	179	180	DQ60	DDR_A_D60
DDR_A_D56	VSS46	181	182	DQ61	DDR_A_D61
DDR_A_D57	DQ56	183	184	VSS47	
	DQ57	185	186	DQS#7	DDR_A_DQS#7
DDR_A_DM7	VSS48	187	188	DQS7	DDR_A_DQS7
	DM7	189	190	VSS50	
DDR_A_D58	VSS49	191	192	DQ62	DDR_A_D62
DDR_A_D59	DQ58	193	194	DQ63	DDR_A_D63
	DQ59	195	196	VSS52	
	VSS51	197	198	EVENT#	
	SA0	199	200	SDA	D_CK_SDATA
	VDDSPD	201	202	SCL	D_CK_SCLK
	SA1	203	204	VTT2	+0.75VS
	VTT1	205	206	G2	
	G1				

FOX_AS0A626-U4SN-7F

CONN@

+3VS +0.75VS

C2042 0.1U_0402_16V4Z

C2043 2.2U_0603_6.3V6K

R2028 10K_0402_5%

R2029 10K_0402_5%

C2036 2.2U_0603_6.3V6K

C2037 0.1U_0402_16V4Z

DDR_A_DQS#[0..7] <6>
DDR_A_DQS[0..7] <6>
DDR_A_D[0..63] <6>
DDR_A_MA[0..15] <6>

Layout Note: Place near JDIMM0

+1.5V

C2024 1U_0402_6.3V6K C2025 1U_0402_6.3V6K C2026 1U_0402_6.3V6K C2027 1U_0402_6.3V6K

+1.5V

C2029 10U_0603_6.3V6M C2030 10U_0603_6.3V6M C2031 10U_0603_6.3V6M C2032 10U_0603_6.3V6M C2033 10U_0603_6.3V6M C2034 10U_0603_6.3V6M C2035 10U_0603_6.3V6M C2028 330U_2.5V_M

DVT:Update C2028 footprint

Layout Note: Place near JDIMM0.203,204

+0.75VS

C2038 1U_0402_6.3V6K C2039 1U_0402_6.3V6K C2040 1U_0402_6.3V6K C2041 1U_0402_6.3V6K

DDR_A_DM0
DDR_A_DM1
DDR_A_DM2
DDR_A_DM3
DDR_A_DM4
DDR_A_DM5
DDR_A_DM6
DDR_A_DM7

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Title: DDRIII DIMMA

Size	Document Number	Rev
Custom	LA-7141P	1.0

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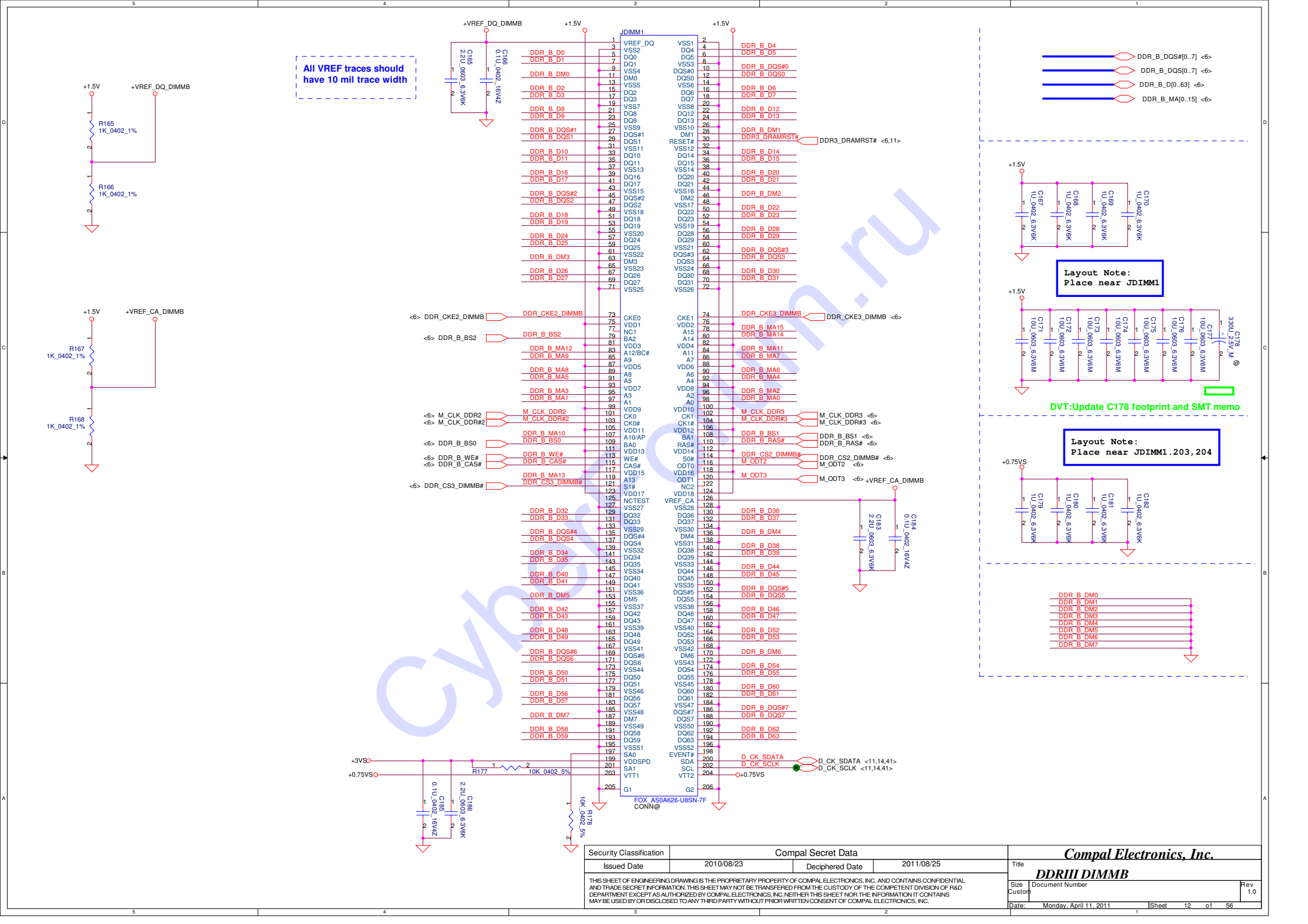

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Title: **DDRIII DIMMB**

Size	Document Number	Rev
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DVT:C188 C189 18p-->15p

DVT:Add U67 R987 R988 for SATA issue

W=20mils W=10mils W=20mils

Place C194 close to PCH.

INTVRMEN

* H : Integrated VRM enable
  L : Integrated VRM disable

(INTVRMEN should always be pull high.)

HDA_SDO

* HIGH= Enable (No Reboot)
  LOW= Disable (Default)

ME debug mode,this signal has a weak internal PD
* Low = Disabled (Default)
  High = Enabled [Flash Descriptor Security Overide]

This signal has a weak internal pull-down

On Die PLL VR Select is supplied by
* 1.5V when smapled high
  1.8V when sampled low
  Needs to be pulled High for Huron River platfrom

Need to open

CMOS

ME

Need to open

PVT:Reserved D28

SPI ROM FOR ME (4MByte)

If use SPI programmer, R211 should be open (Normal is pop)

32M MX25L3206EM2I-12G SOP 8P 3V

64M MX25L6405DZNI-12G WSON 8P

Prevent back drive issue; +3VLAW leakage to +3VS from HDA_SYNC

Reserve for EMI please close to U14

BD82CPMS-QMVY-A1_FCBGA989~D

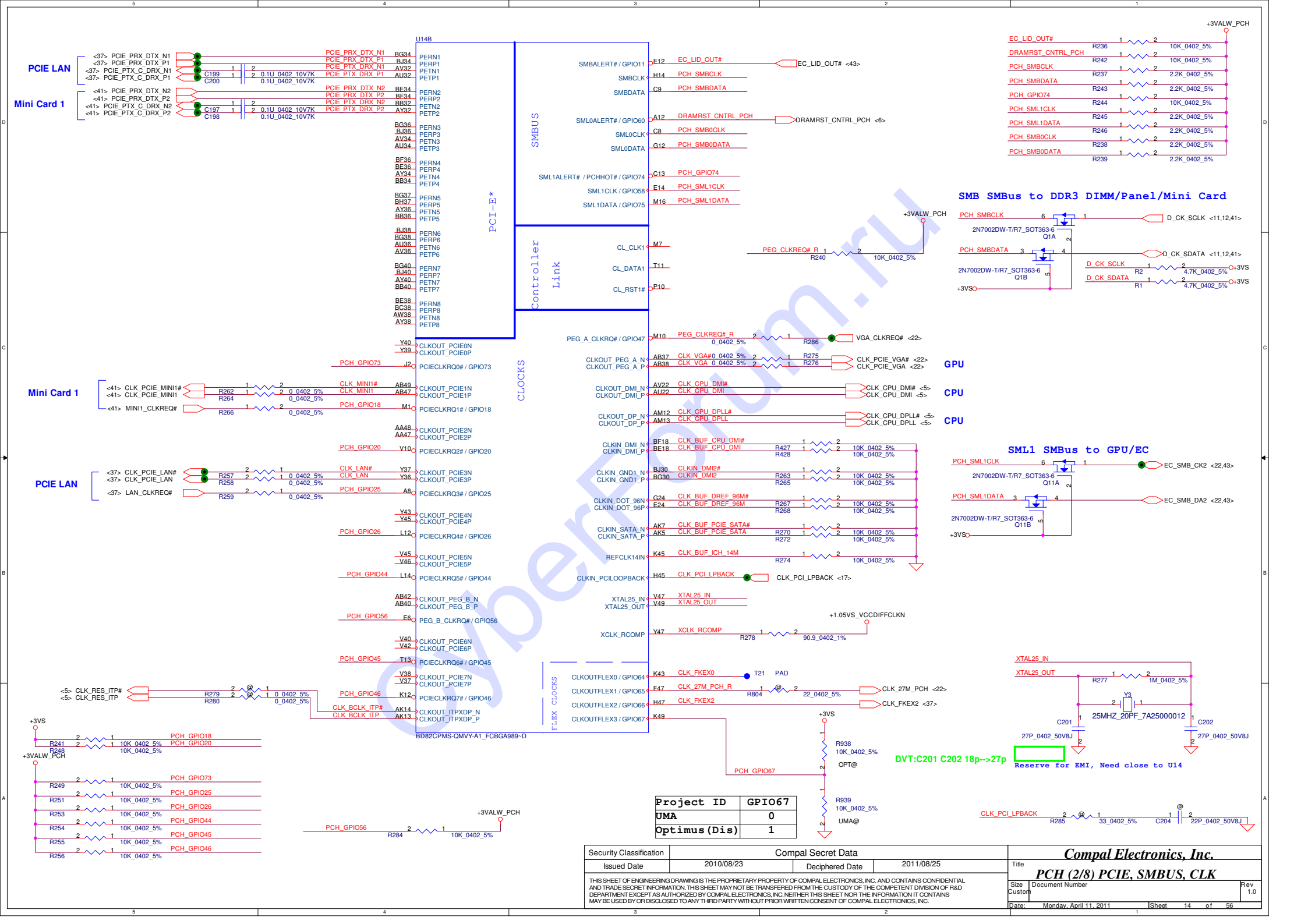
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

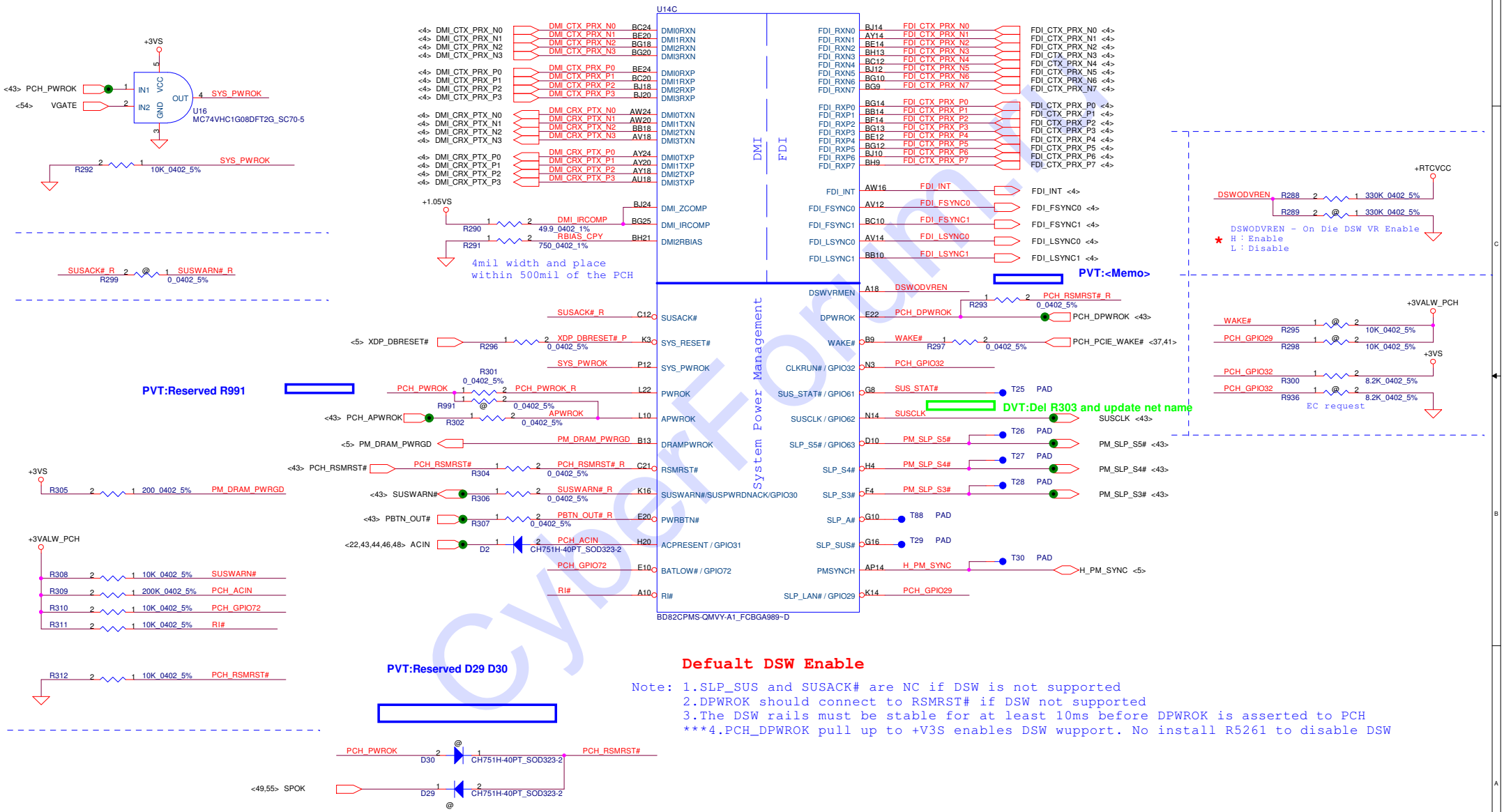
Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP

Size: Custom | Document Number | Rev: 1.0

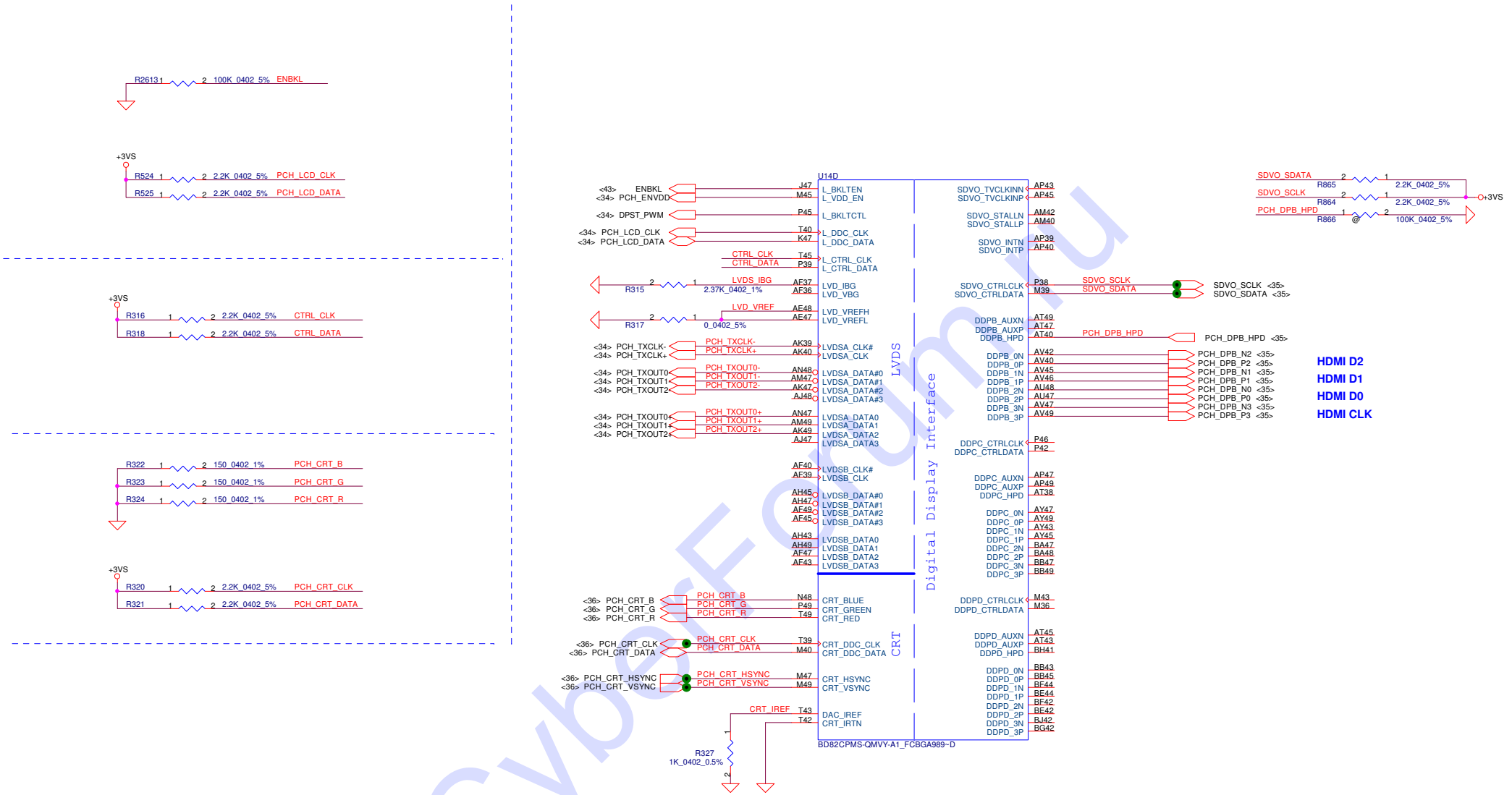
Date: Monday, April 11, 2011 | Sheet 13 of 56


PCIE LAN
Mini Card 1
U14B
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
BD82CPMS-QMVY-A1_FCBGA989~D
SMB SMBus to DDR3 DIMM/Panel/Mini Card
SML1 SMBus to GPU/EC
GPU
CPU
CPU
DVT:C201 C202 18p-->27p
Reserve for EMI, Need close to U14
Project ID | GPIO67
UMA | 0
Optimus(Dis) | 1
Compal Electronics, Inc.
PCH (2/8) PCIE, SMBUS, CLK
Security Classification | Compal Secret Data
Issued Date | 2010/08/23 | Deciphered Date | 2011/08/25
Monday, April 11, 2011
Sheet 14 of 56



Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.			
Title: PCH (3/8) DMI,FDI,PM,			
Size: Custom	Document Number		Rev: 1.0
Date: Monday, April 11, 2011		Sheet 15 of 56	



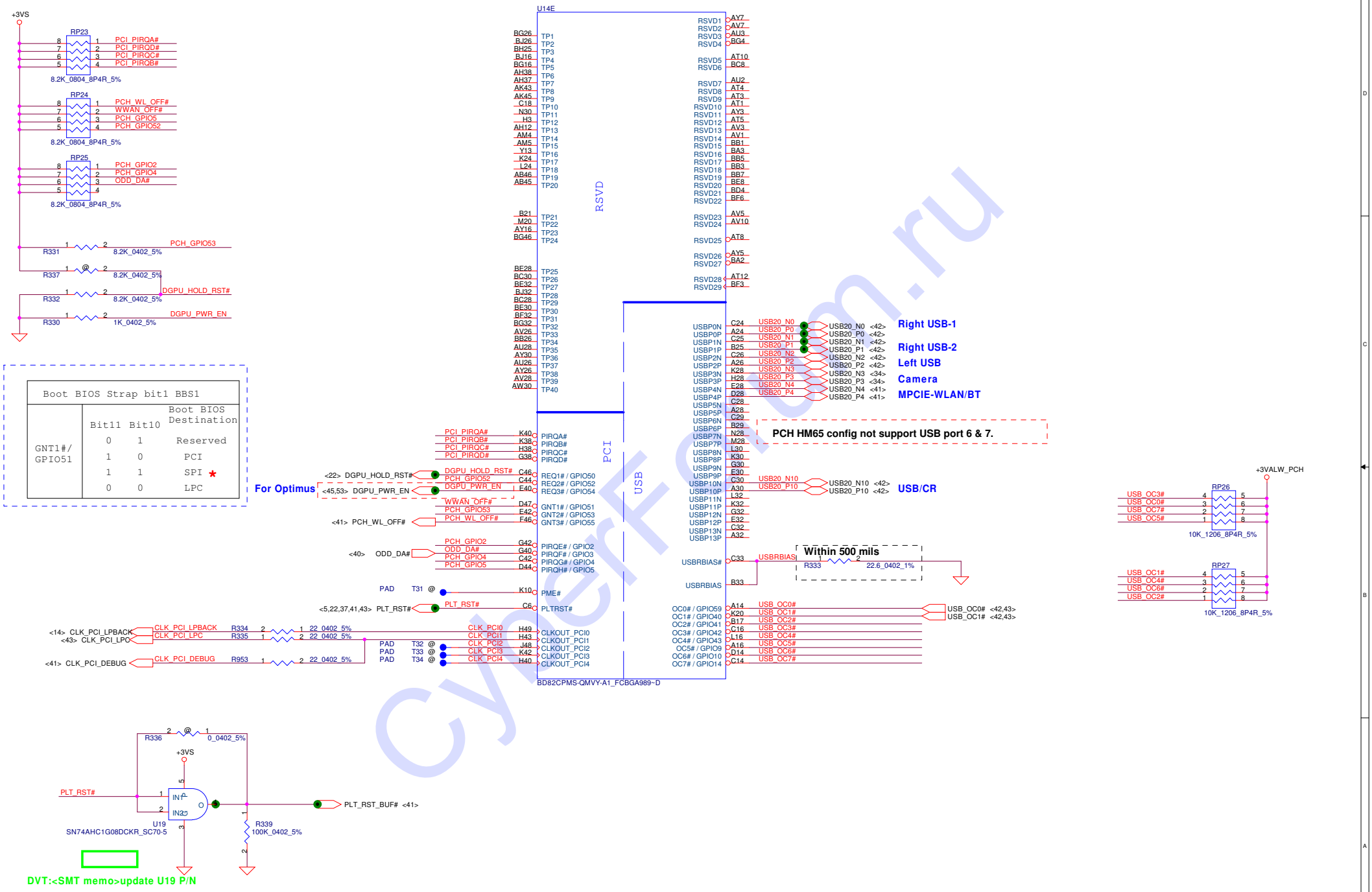
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: **PCH (4/9) LVDS,CRT,DP,HDMI**

Size	Document Number	Rev
Custom		1.0

Date: Monday, April 11, 2011 Sheet 16 of 56



Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.		
Title: PCH (5/9) PCI, USB, NVRAM		
Size: Custom	Document Number	Rev: 1.0
Date: Monday, April 11, 2011	Sheet 17 of 56	

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

R343 1K_0402_5% PCH_GPIO28

GPIO27
PCH_GPIO27 (Have internal Pull-High)

★ High: VCCVRM VR Enable
Low: VCCVRM VR Disable

R344 10K_0402_5% PCH_GPIO27

+3VS

Note: High - CRT Plugged

R342 10K_0402_5%

CRT_DET

<36> CRT_DET# Q12 2N7002_SOT23-3

+3VS

ODD_EN# R2614 10K_0402_5%

PCH_GPIO70 R2616 10K_0402_5%

PCH_GPIO71 R2617 10K_0402_5%

GATEA20 R346 10K_0402_5%

EC_KBRST# R345 10K_0402_5%

SATA2GP/GPIO36 & SATA3GP/GPIO37
Sampled at Rising edge of PWROK.
Weak internal pull-down. (weak internal pull-down is disabled after PLTRST# de-asserts)
NOTE: This signal should NOT be pulled high when strap is sampled

+3VS

R357 200K_0402_1% ODD_DETECT#

+3VS

R801 1K_0402_5% PCH_GPIO37

R776 100K_0402_5%

For Optimus

<45,53> DGPU_PWROK R350 0_0402_5% DGPU_PWROK_R

DVT:Add PCH_GPIO49 net off page

<13> PCH_GPIO49

U14F

CRT_DET	T7	BMBUSY# / GPIO0	
PCH_GPIO1	A42	TACH1 / GPIO1	
PCH_GPIO6	H36	TACH2 / GPIO6	
<43> EC_SCI#	E38	TACH3 / GPIO7	
<43> EC_SMI#	C10	GPIO8	
PCH_GPIO12	C4	LAN_PHY_PWR_CTRL / GPIO12	
USB30_SMI#	G2	GPIO15	
PCH_GPIO16	U2	SATA4GP / GPIO16	
DGPU_PWROK_R	D40	TACH0 / GPIO17	
PCH_GPIO22	T5	SCLOCK / GPIO22	
PCH_GPIO24	E8	GPIO24 / MEM_LED	
PCH_GPIO27	E16	GPIO27	
PCH_GPIO28	P8	GPIO28	
<41> BT_ON#	K1	STP_PCI# / GPIO34	
PCH_GPIO35	K4	GPIO35	
<40> ODD_DETECT#	V8	SATA2GP / GPIO36	
PCH_GPIO37	M5	SATA3GP / GPIO37	
PCH_GPIO38	N2	SLOAD / GPIO38	
PCH_GPIO39	M3	SDATAOUT0 / GPIO39	
PCH_GPIO48	V13	SDATAOUT1 / GPIO48	
PCH_GPIO49	V3	SATA5GP / GPIO49	
PCH_GPIO57	D6	GPIO57	

GPIO

TACH4 / GPIO68	C40	ODD_EN#	ODD_EN# <40>
TACH5 / GPIO69	B41	PCH_GPIO69	
TACH6 / GPIO70	C41	PCH_GPIO70	
TACH7 / GPIO71	A40	PCH_GPIO71	
A20GATE	P4		GATEA20 <43>
PECI	AU16	PCH_PECI_R R348 0_0402_5%	H_PECI <5,43>
RCIN#	P5		EC_KBRST# <43>
PROCPWRGD	AY11		H_CPUPWRGD <5>
THRMTRIP#	AY10	PCH_THRMTRIP#_R R351 390_0402_5%	H_THRMTRIP# <5>
INIT3_3V#	T14		
DF_TVS	AY1	NV_CLE R329 1K_0402_5%	H_SNB_IVB# <5>
TS_VSS1	AH8		
TS_VSS2	AK11		
TS_VSS3	AH10		
TS_VSS4	AK10		
NC_1	P37		

CPU/MISC

Note: This signal has weak internal PU, can't pull low

Layout note: CLOSE TO THE BRANCHING POINT

Project ID	GPIO69
14"	0
15.6"	1

+3VS

R2615 10K_0402_5% 15@

PCH_GPIO69

R940 10K_0402_5% 14@

+1.8VS

R328 2.2K_0402_5%

Intel Anti-Theft Techonlogy	
NV_ALE	High=Endabled
	Low=Disable(floating) ★

VSS_NCTF_1	A4	VSS_NCTF_15	BG2
VSS_NCTF_2	A44	VSS_NCTF_16	BG48
VSS_NCTF_3	A45	VSS_NCTF_17	BH3
VSS_NCTF_4	A46	VSS_NCTF_18	BH47
VSS_NCTF_5	A5	VSS_NCTF_19	BJ4
VSS_NCTF_6	A6	VSS_NCTF_20	BJ44
VSS_NCTF_7	B3	VSS_NCTF_21	BJ45
VSS_NCTF_8	B47	VSS_NCTF_22	BJ46
VSS_NCTF_9	BD1	VSS_NCTF_23	BJ5
VSS_NCTF_10	BD49	VSS_NCTF_24	BJ6
VSS_NCTF_11	BE1	VSS_NCTF_25	C2
VSS_NCTF_12	BE49	VSS_NCTF_26	C48
VSS_NCTF_13	BF1	VSS_NCTF_27	D1
VSS_NCTF_14	BF49	VSS_NCTF_28	D49
		VSS_NCTF_29	E1
		VSS_NCTF_30	F49
		VSS_NCTF_31	F1
		VSS_NCTF_32	F49

NCTF

BD82CPMS-QMVY-A1_FCBGA989-D

+3VS

R421 10K_0402_5% PCH_GPIO6
R420 10K_0402_5% PCH_GPIO1
R352 10K_0402_5% PCH_GPIO16
R353 10K_0402_5% DGPU_PWROK_R
R354 10K_0402_5% PCH_GPIO22
R347 10K_0402_5% PCH_GPIO38
R356 10K_0402_5% PCH_GPIO39

R358 10K_0402_5% BT_ON#
R359 10K_0402_5% PCH_GPIO48
R360 10K_0402_5% PCH_GPIO49

+3VALW_PCH

R361 10K_0402_5% PCH_GPIO12
R362 1K_0402_5% USB30_SMI#
R363 10K_0402_5% PCH_GPIO28
R364 10K_0402_5% PCH_GPIO57
R429 10K_0402_5% PCH_GPIO24

R365 10K_0402_5% PCH_GPIO35

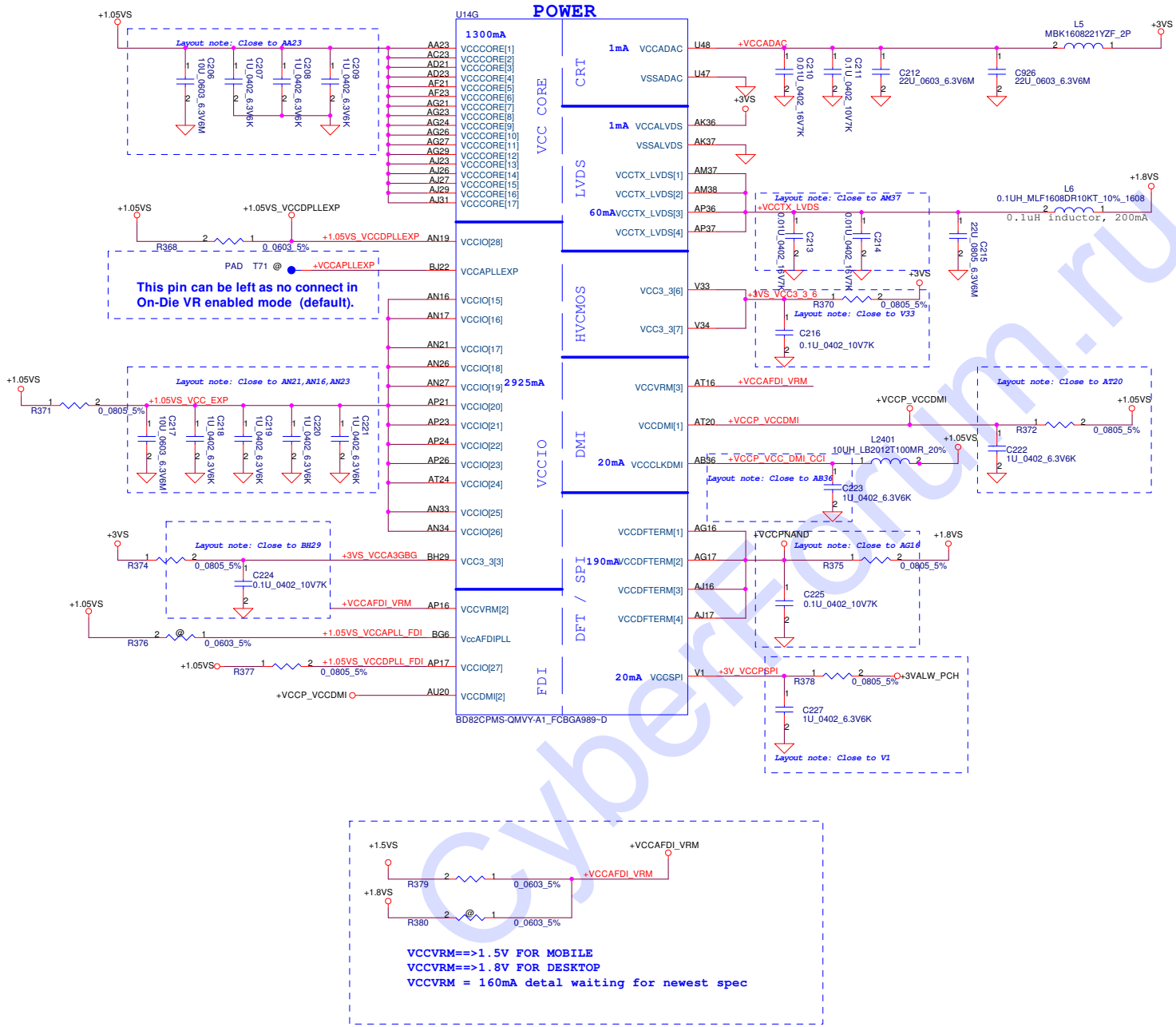
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: **PCH (6/9) GPIO, CPU, MISC**

Size	Document Number	Rev
Custom		1.0

Date: Monday, April 11, 2011 Sheet 18 of 56



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number | Rev: 1.0

Date: Sunday, April 10, 2011 | Sheet 19 of 56

Have internal VRM

VCC3_3 = 266mA detal waiting for newest spec

VCCDMI = 42mA detal waiting for newest spec

12/29 change SC1H751H010 to SCS00003500

DVT:Reserved C913 C914

PVT:<Memo>

POWER

U14J

BD82CPMS-QMVY-A1_FCBGA989~D

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

MISC

CPU

RTC

HDA

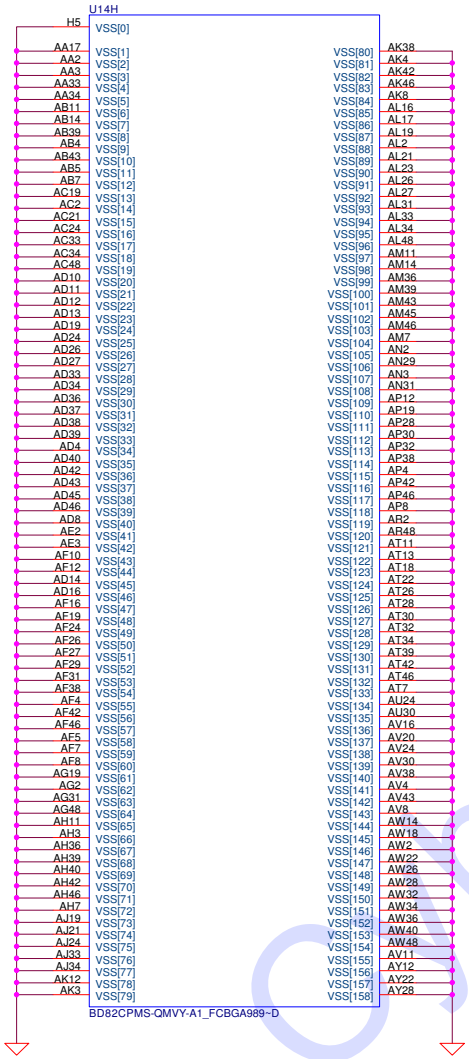
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

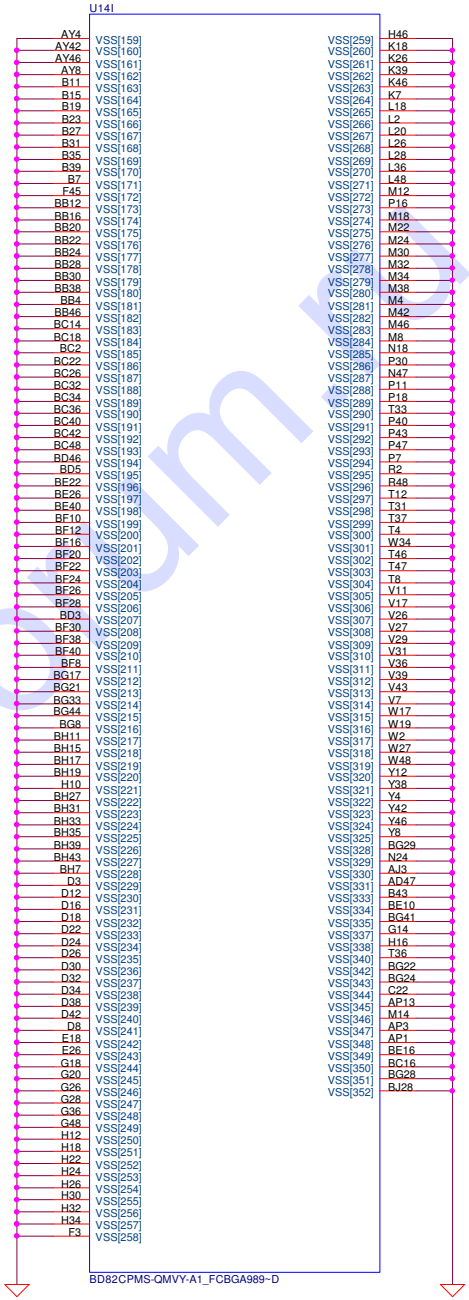
Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number | Rev: 1.0

Date: Monday, April 11, 2011 | Sheet 20 of 56





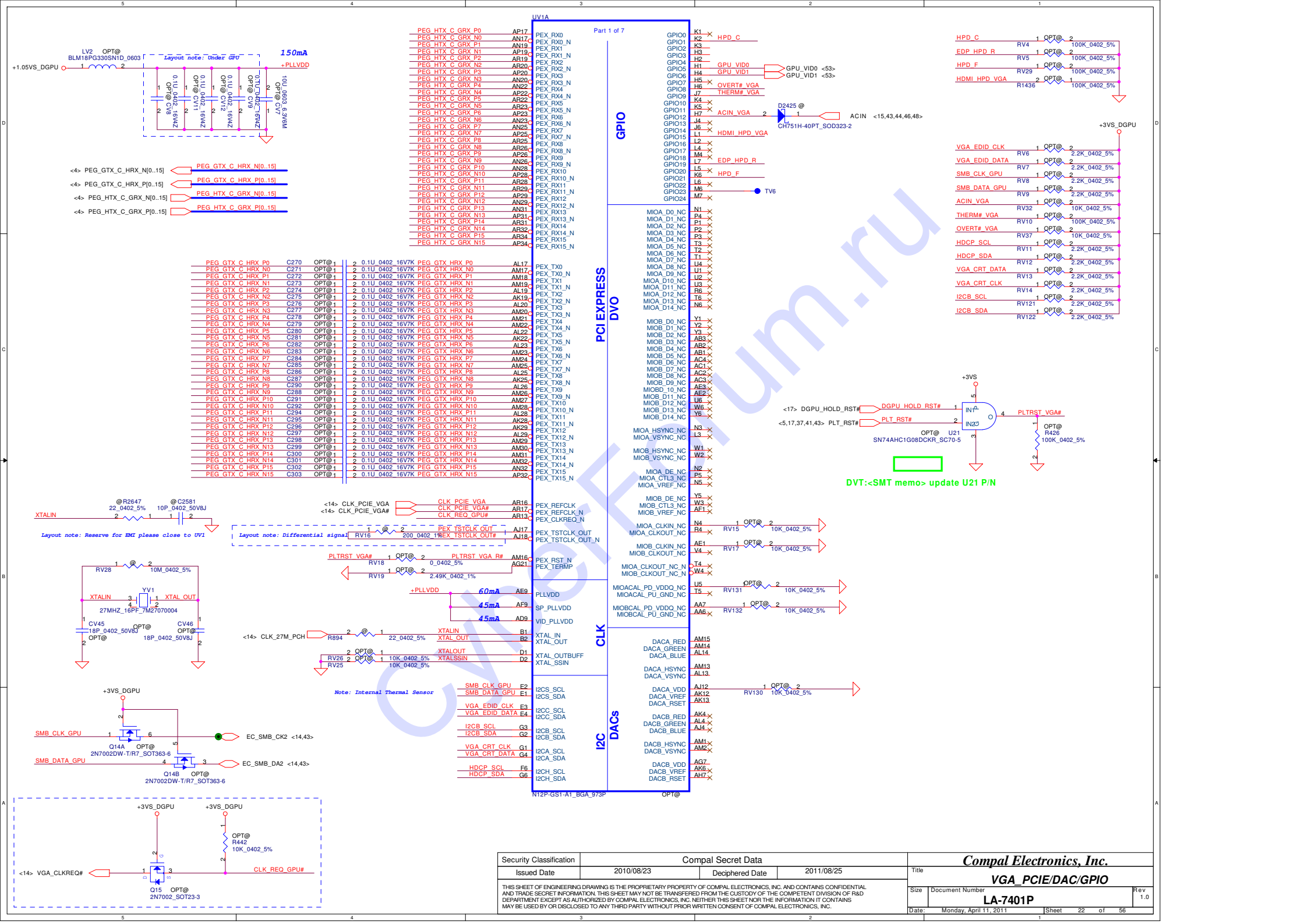
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: **PCH (9/9) VSS**

Size	Document Number	Rev
Custom		1.0

Date: Sunday, April 10, 2011 Sheet 21 of 56



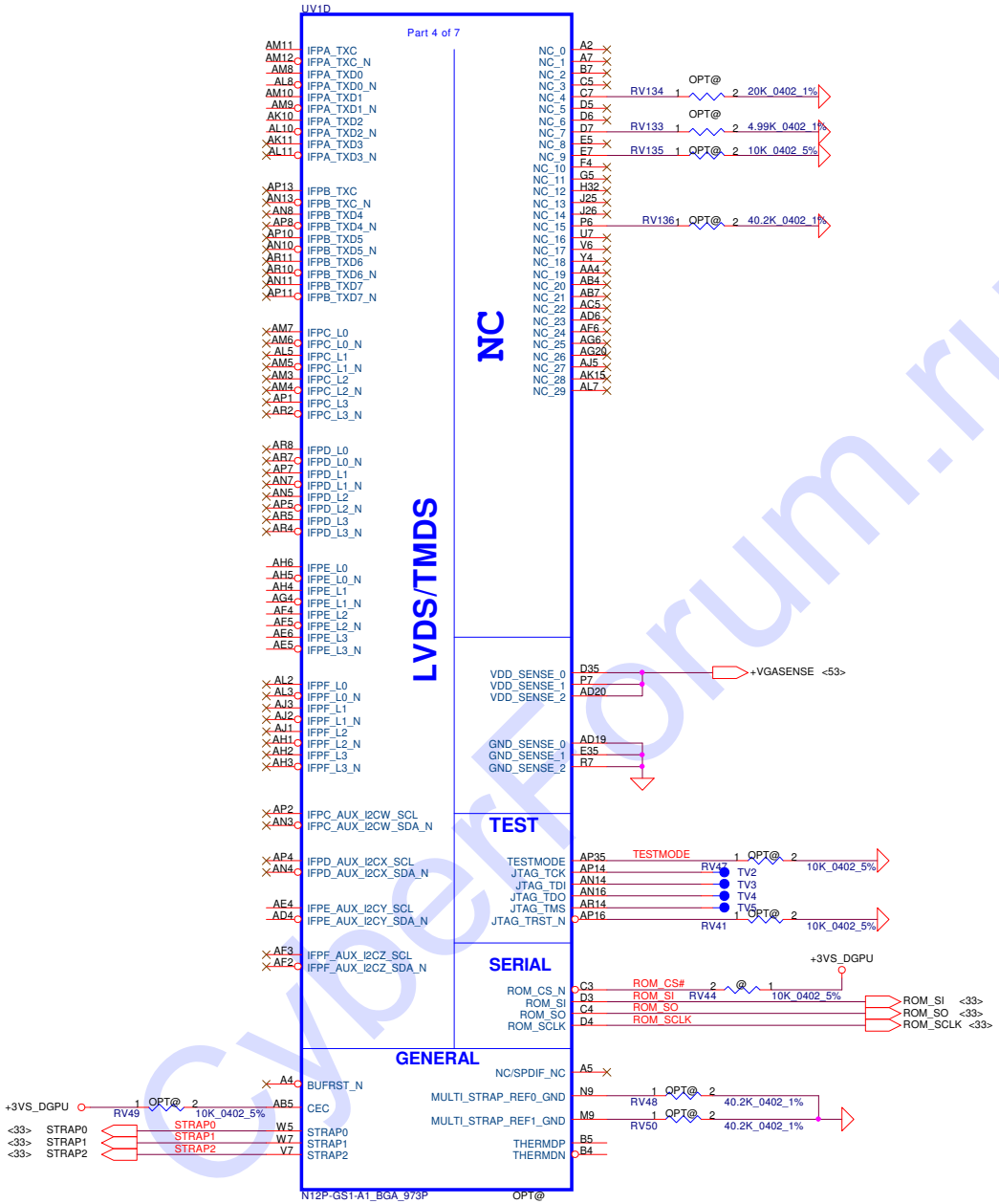
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: **VGA_PCIE/DAC/GPIO**

Size	Document Number	Rev
	LA-7401P	1.0

Date: Monday, April 11, 2011 Sheet 22 of 56



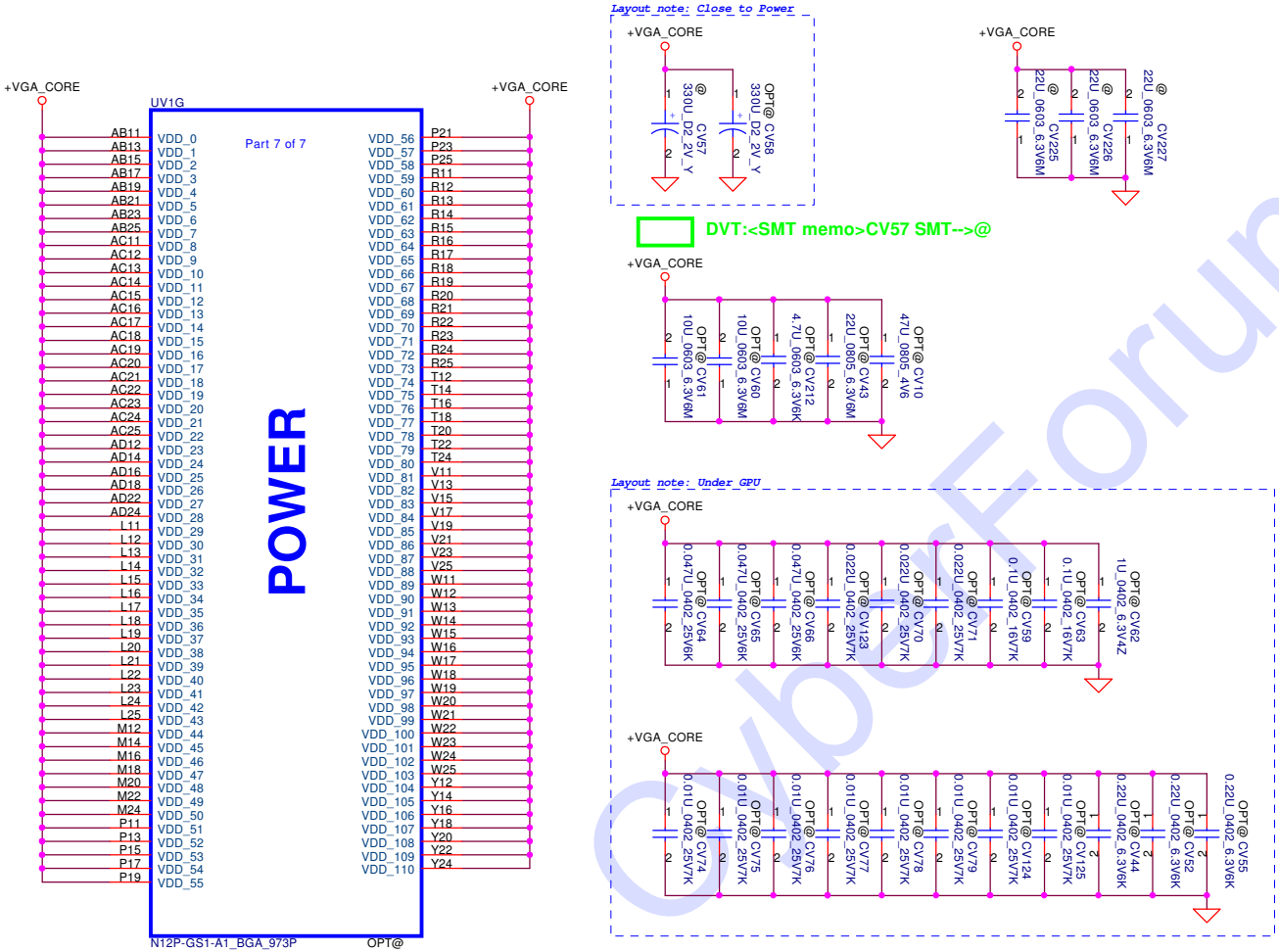
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: **VGA_STRAPS**

Size	Document Number	Rev
	LA-7401P	1.0

Date: Sunday, April 10, 2011 Sheet 23 of 56



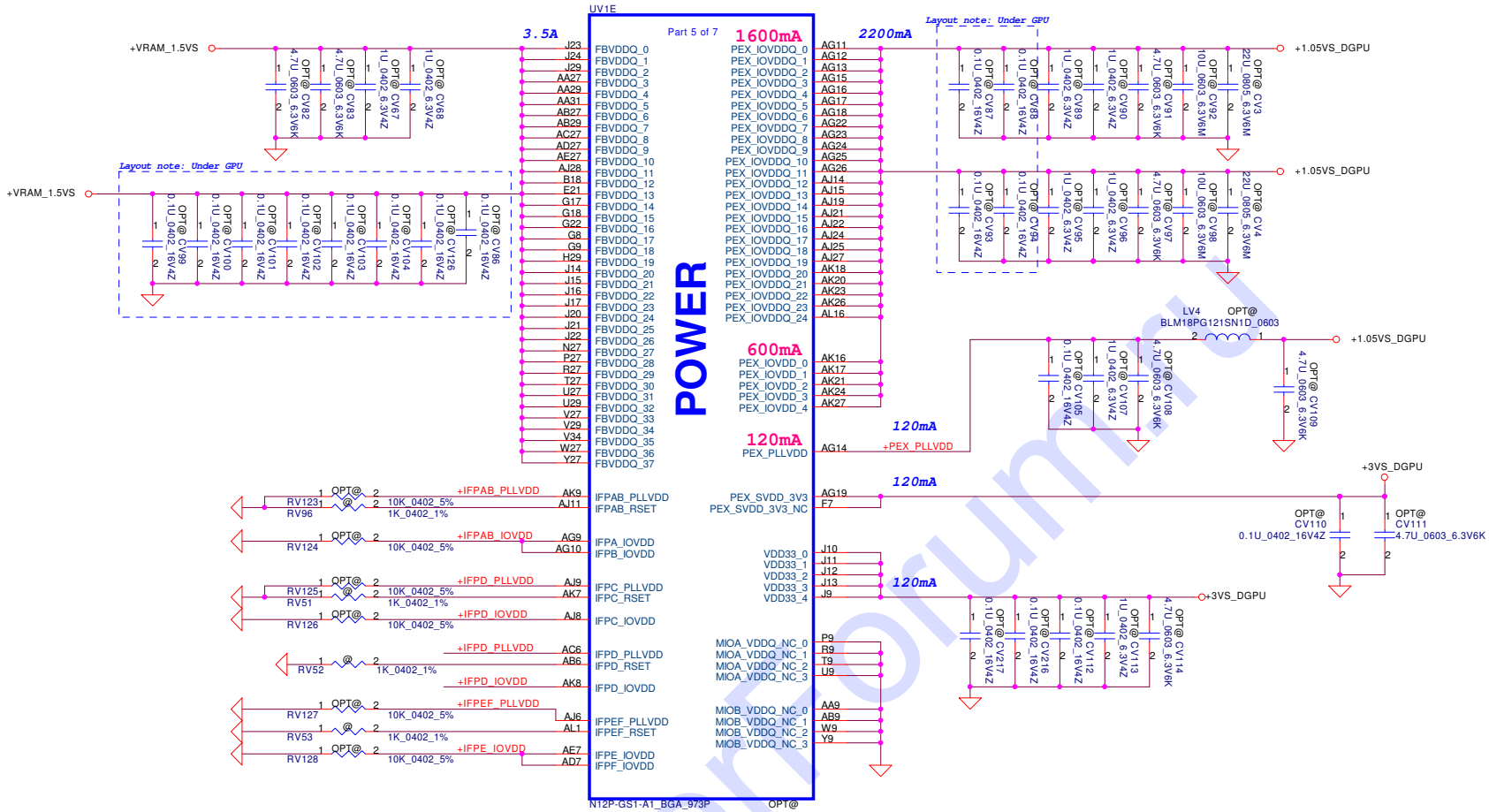
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: **VGA_VGA CORE**

Size	Document Number	Rev
	LA-7401P	1.0

Date: Sunday, April 10, 2011 | Sheet 24 of 56



Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.			
Title: VGA_POWER			
Size	Document Number: LA-7401P		Rev: 1.0
Date: Sunday, April 10, 2011	Sheet 25 of 56		

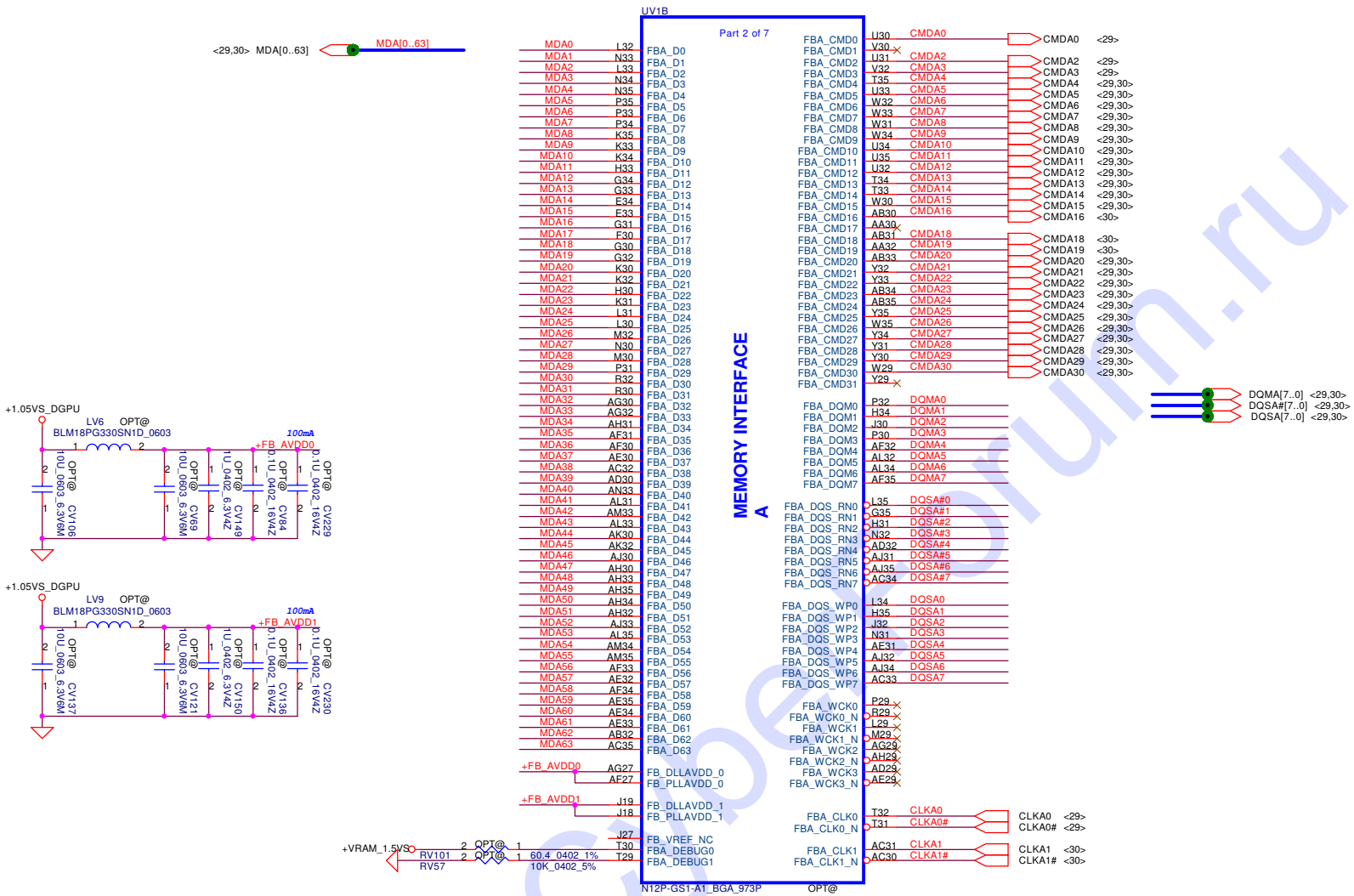
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: **VGA_GND**

Size | Document Number: **LA-7401P** | Rev: 1.0

Date: Sunday, April 10, 2011 | Sheet 26 of 56



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

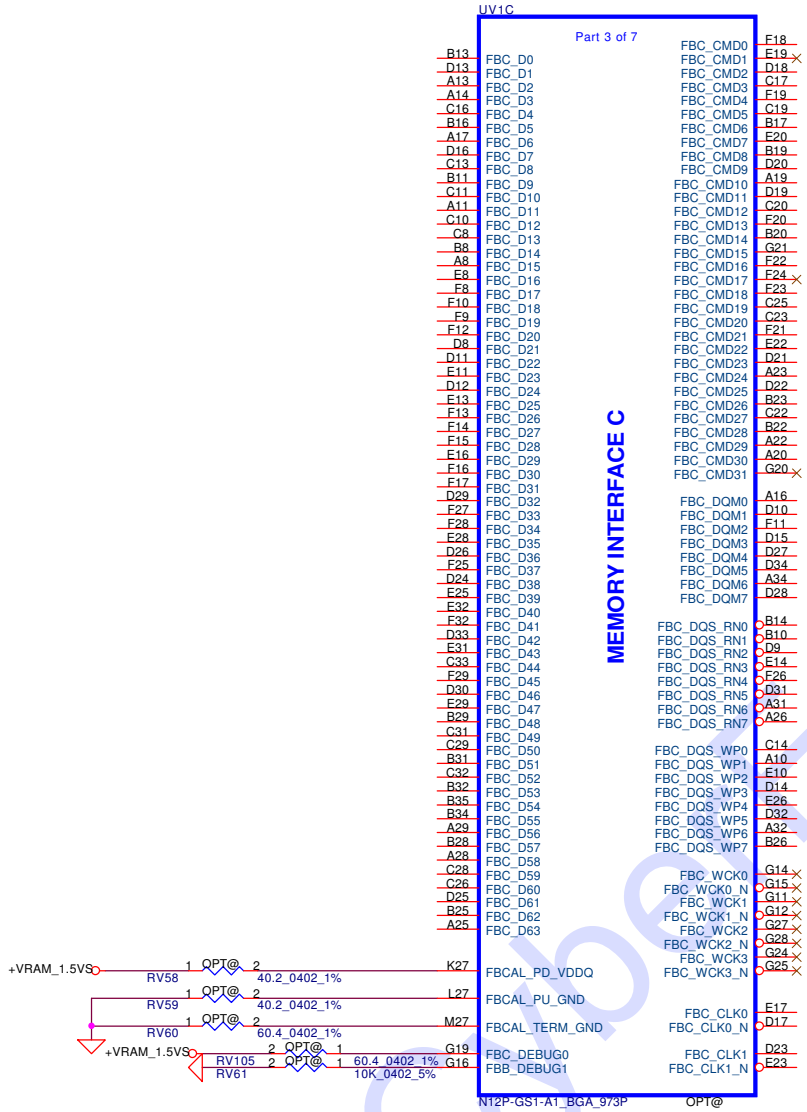
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: **VGA_MEM Interface A**

Size | Document Number: **LA-7401P** | Rev: 1.0

Date: Monday, April 11, 2011 | Sheet 27 of 56



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

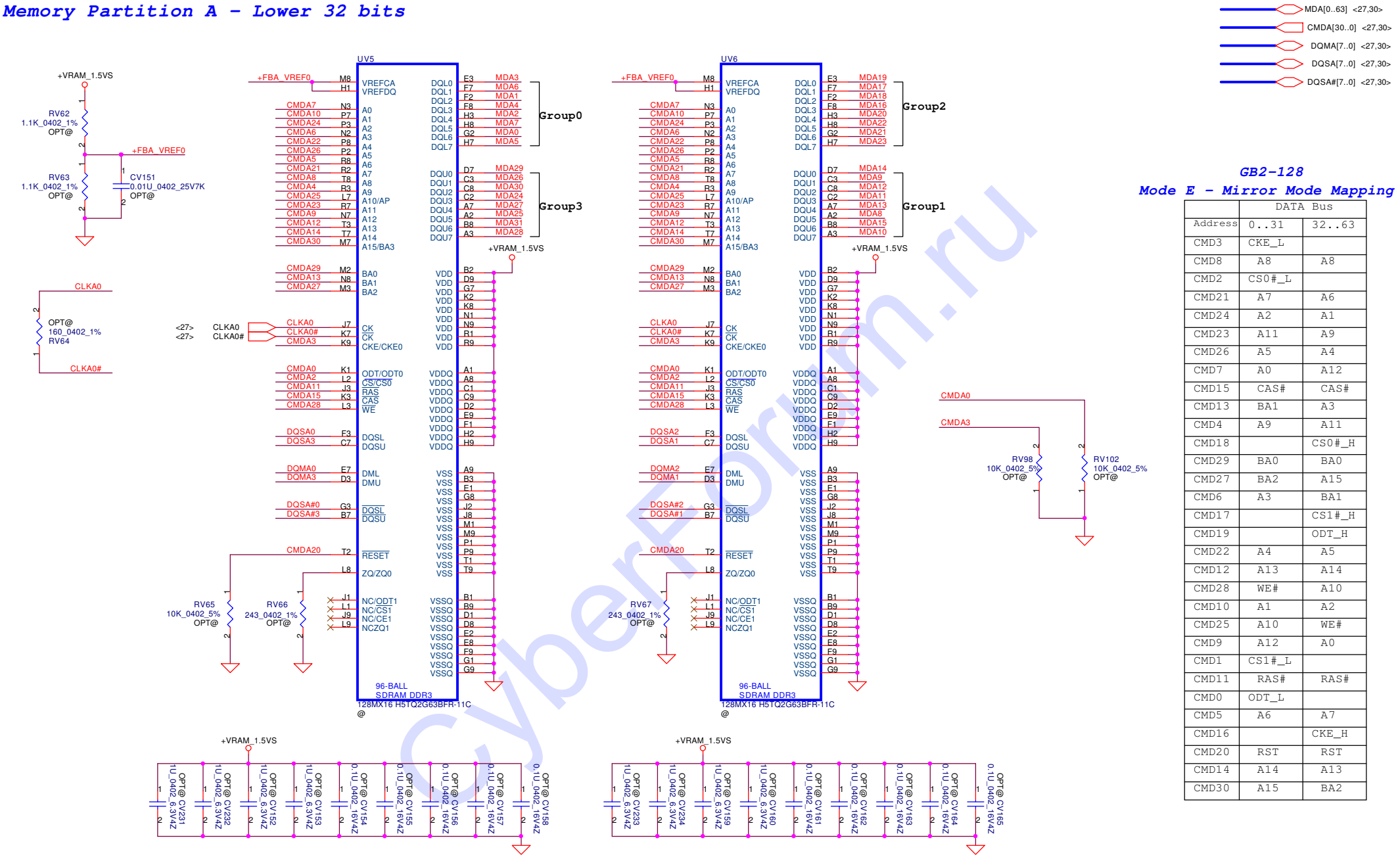
Compal Electronics, Inc.

Title: VGA_MEM Interface C

Size | Document Number: LA-7401P | Rev: 1.0

Date: Sunday, April 10, 2011 | Sheet 28 of 56

Memory Partition A - Lower 32 bits



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

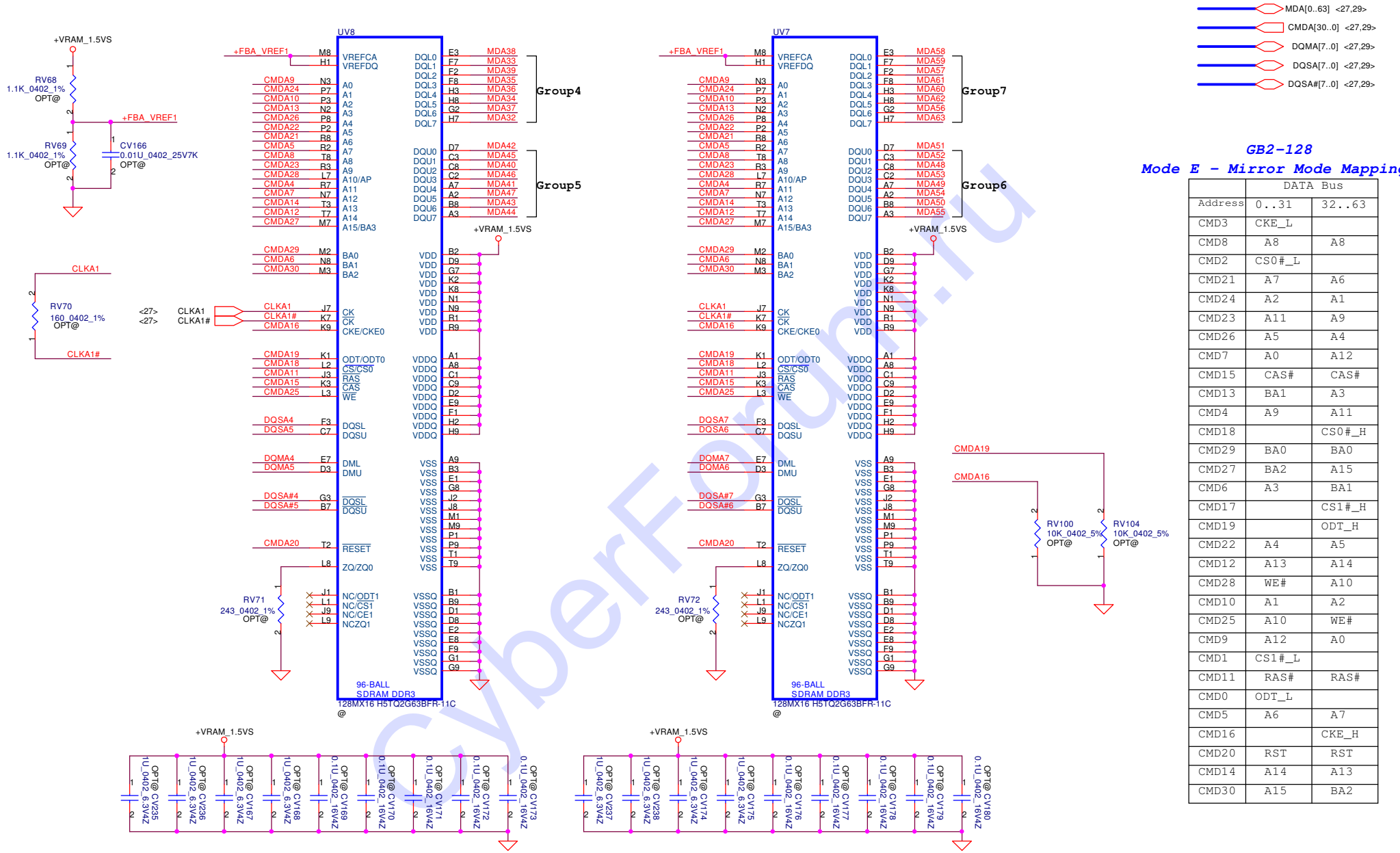
Compal Electronics, Inc.

Title: VGA_VRAM_A Lower

Size | Document Number: LA-7401P | Rev: 1.0

Date: Sunday, April 10, 2011 | Sheet 29 of 56

Memory Partition A - Upper 32 bits



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: VGA_VRAM_A Upper

Size | Document Number: LA-7401P | Rev: 1.0

Date: Sunday, April 10, 2011 | Sheet 30 of 56

Memory Partition C - Lower 32 bits

EVT:Del B ch VRAM

GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Compal Electronics, Inc.

Title: VGA_VRAM_C Lower

Size: Custom | Document Number: LA-7401P | Rev: 1.0

Date: Sunday, April 10, 2011 | Sheet 31 of 56

Memory Partition C - Upper 32 bits

EVT:Del B ch VRAM

GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: VGA_VRAM_C Upper

Size: Custom | Document Number: LA-7401P | Rev: 1.0

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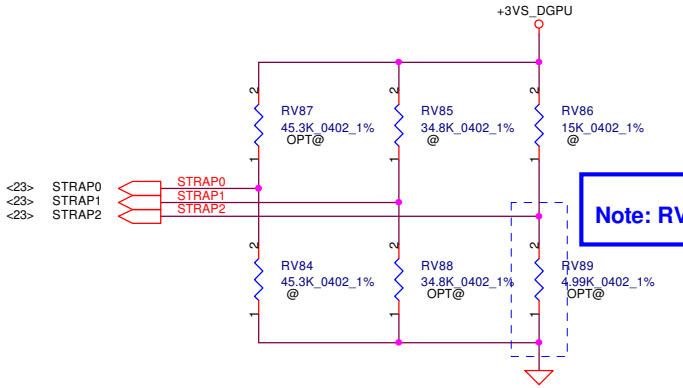
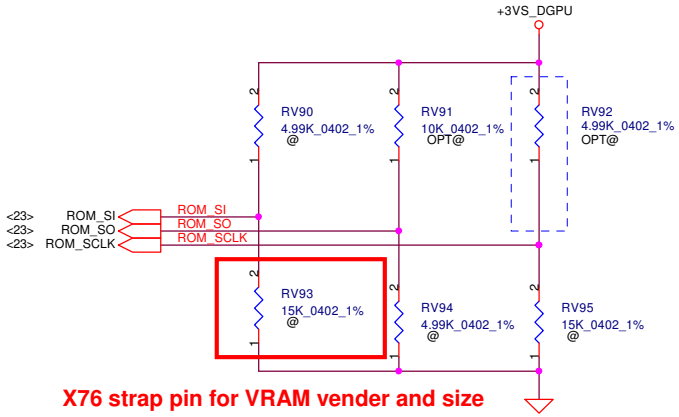


Note: RV89 = 5K for set N12P-GV ,ID=1050)



X76 strap pin for VRAM vender and size

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]

ROM_SI net for VRAM strap

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	Project	VRAM size	CH	Description	Compal VRAM P/N	VRAM description	ROM_SI net setup	PD or PU (RV93)	RP/N
N12P-GV (29x29) 64bit (Layout 4pcs only)	PAJ80(14")	512M(X4)	CHA	DDR3 Hynix 64Mx16 1.5V	SA0000324C0	H5TQ1G63DFR-12C 800MHz	0010	PD 15K	SD034150280(15K)
		512M(x4)	CHA	DDR3 Samsung 64Mx16 1.5V	SA00004HS00	K4W1G1646G-BC12 800MHz	0011	PD 20K	SD034200280(20K)
	PAJ90(15.6")	1G(x4)	CHA	DDR3 Hynix 128Mx16 1.5V	SA00003VS00	H5TQ2G63BFR-12C 800MHz	0110	PD 35K	SD034348280(34.8K)
		1G(x4)	CHA	DDR3 Samsung 128Mx16 1.5V	SA00003MQ40	K4W2G1646C-HC12 800MHz	0111	PD 45K	SD034453280(45.3K)

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLOCK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: **VGA_MSIC**

Size: Custom | Document Number: **LA-7401P** | Rev: 1.0

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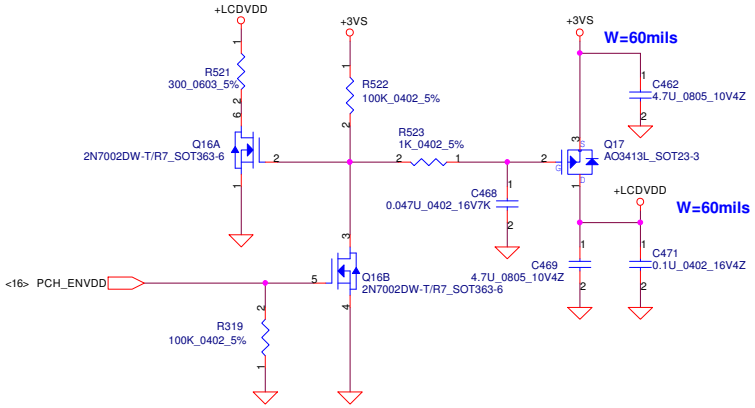
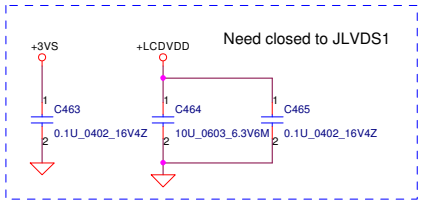
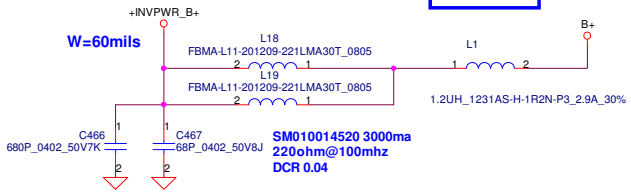
LCD POWER CIRCUIT

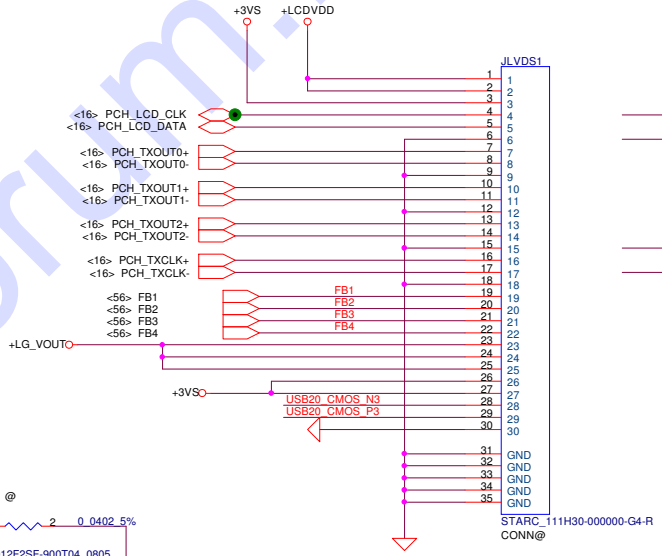


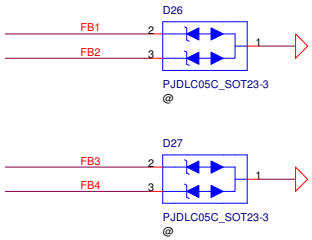


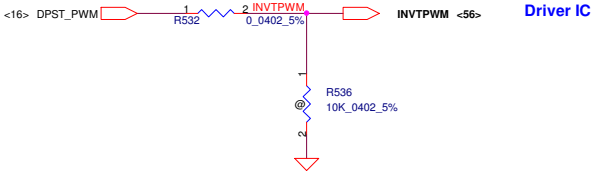
PVT:Add L1 for ESD reuqest

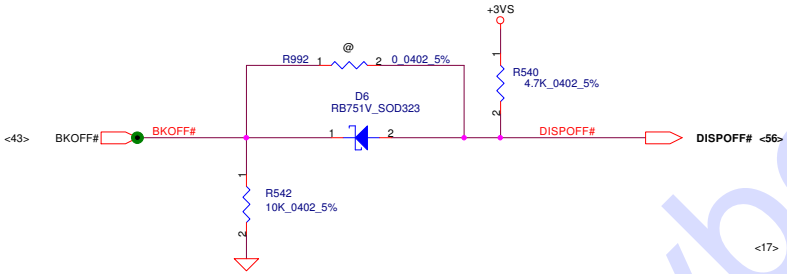


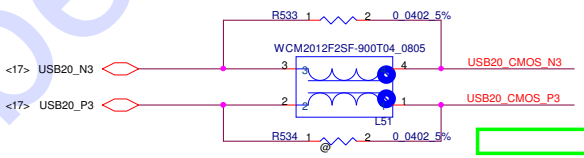
LCD/LED PANEL Connector



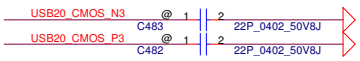


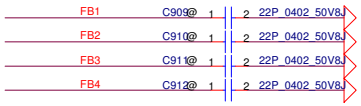


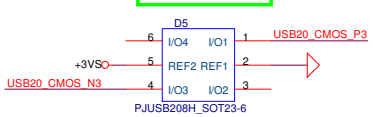




DVT:<EMI>L51 @-->SMT







DVT:<EMI>D5 @-->SMT

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: LVDS Connector

Size	Document Number	Rev
Custom		1.0

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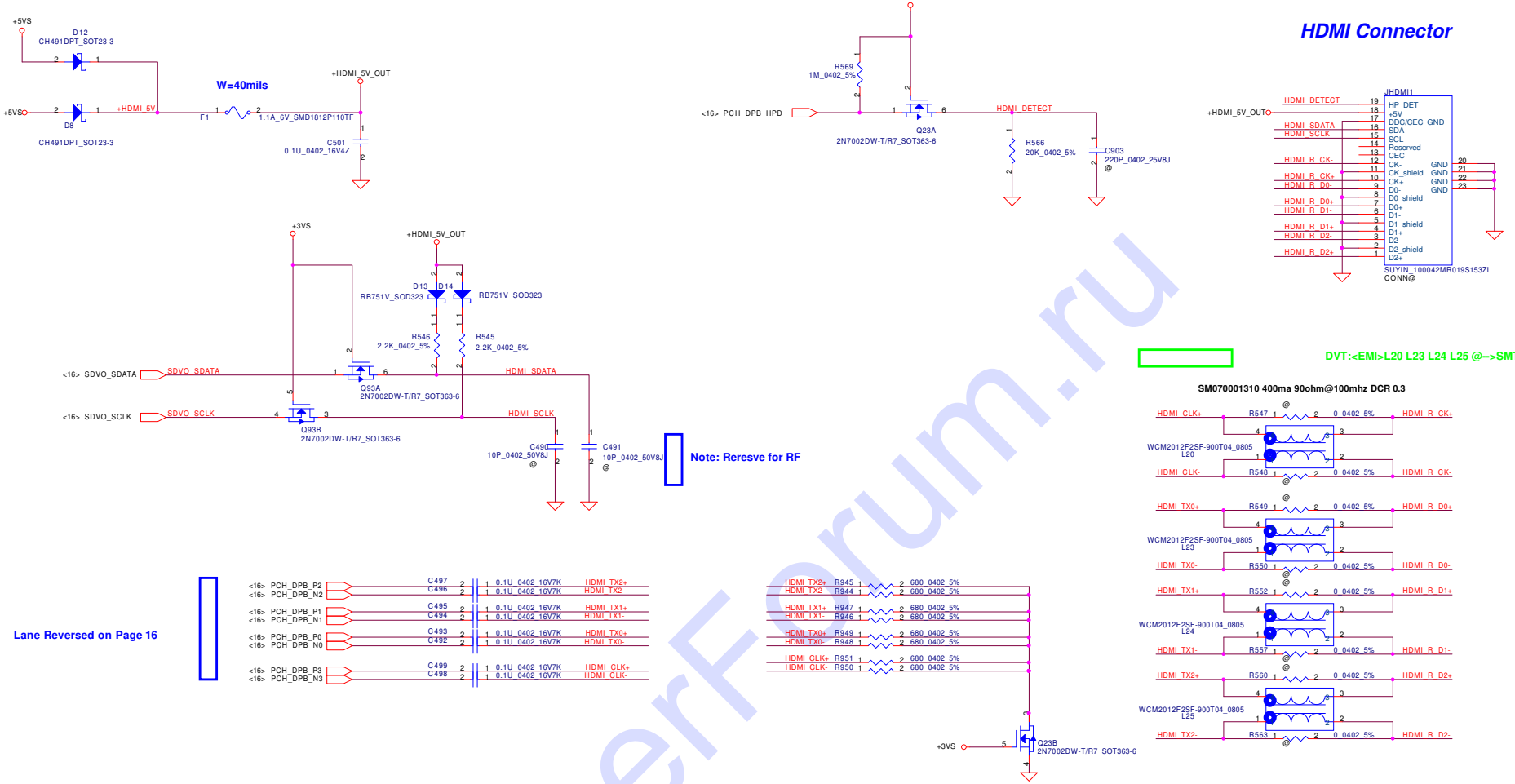
HDMI Connector



Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

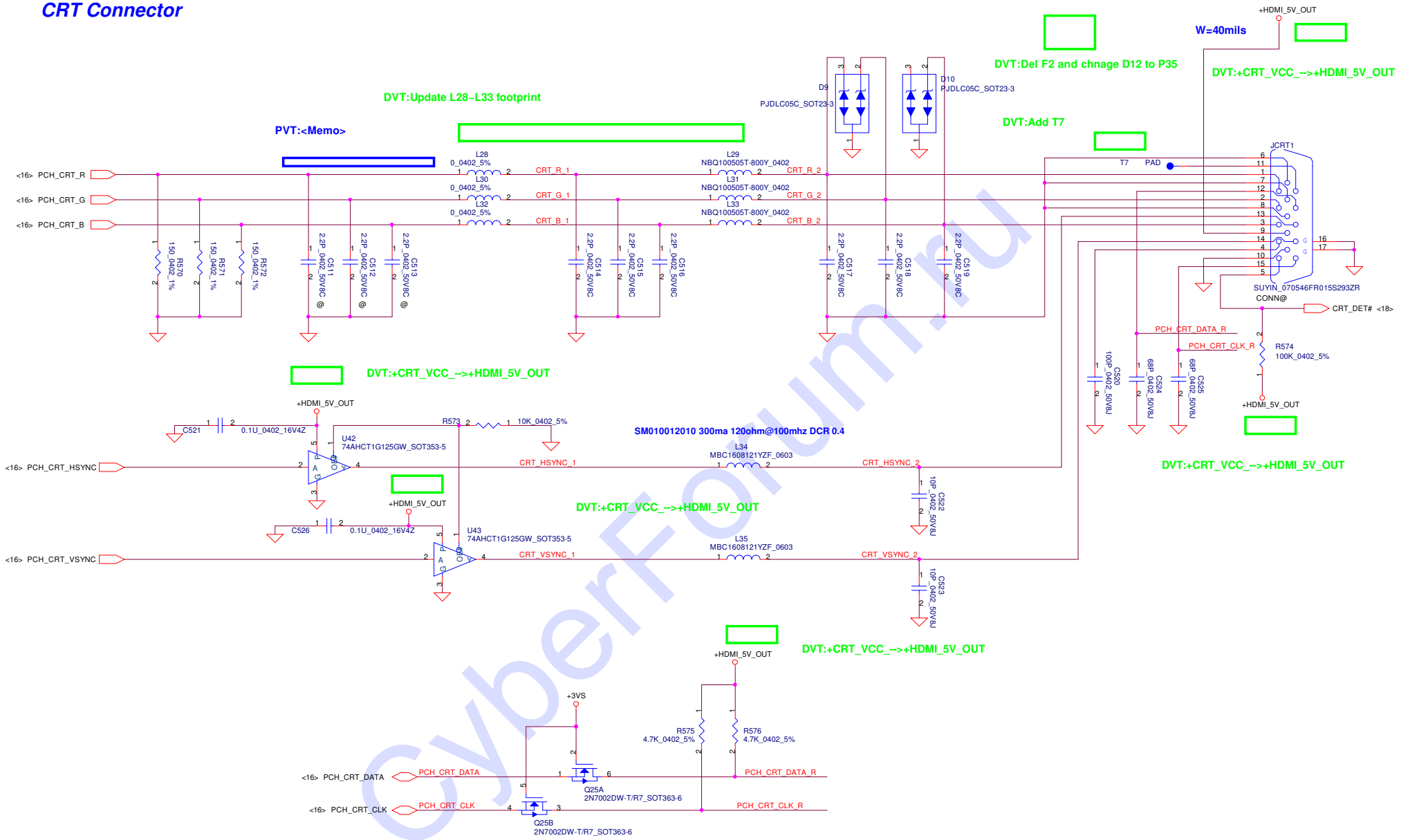
Compal Electronics, Inc.

Title: HDMI Connector

Size	Document Number	Rev
C		1.0

Date: Sunday, April 10, 2011 | Sheet 35 of 56

CRT Connector



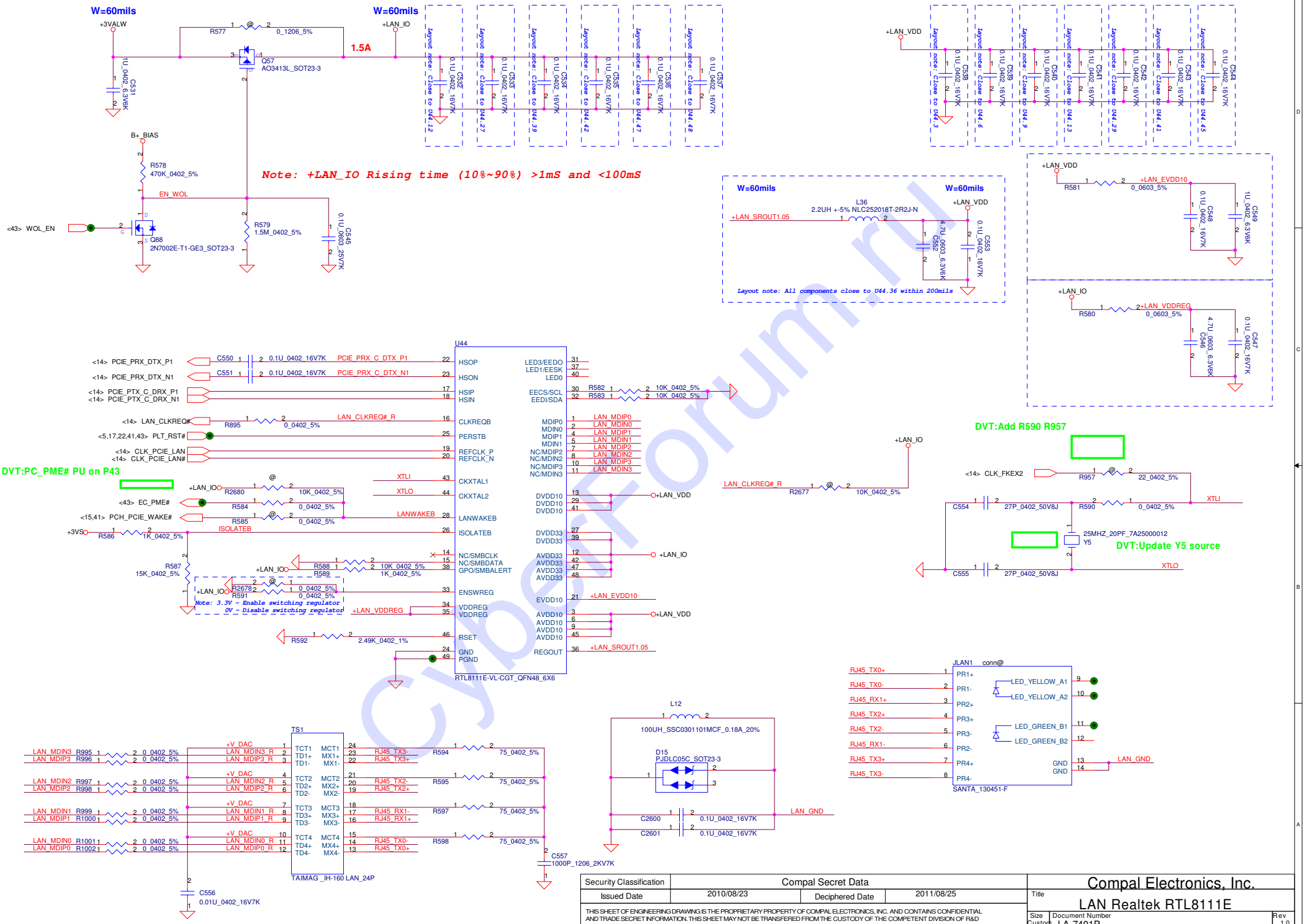
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: CRT Connector

Size: Custom | Document Number | Rev: 1.0

Date: Sunday, April 10, 2011 | Sheet 36 of 56



Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: LAN Realtek RTL8111E

Size	Document Number	Rev
Custom	LA-7401P	1.0

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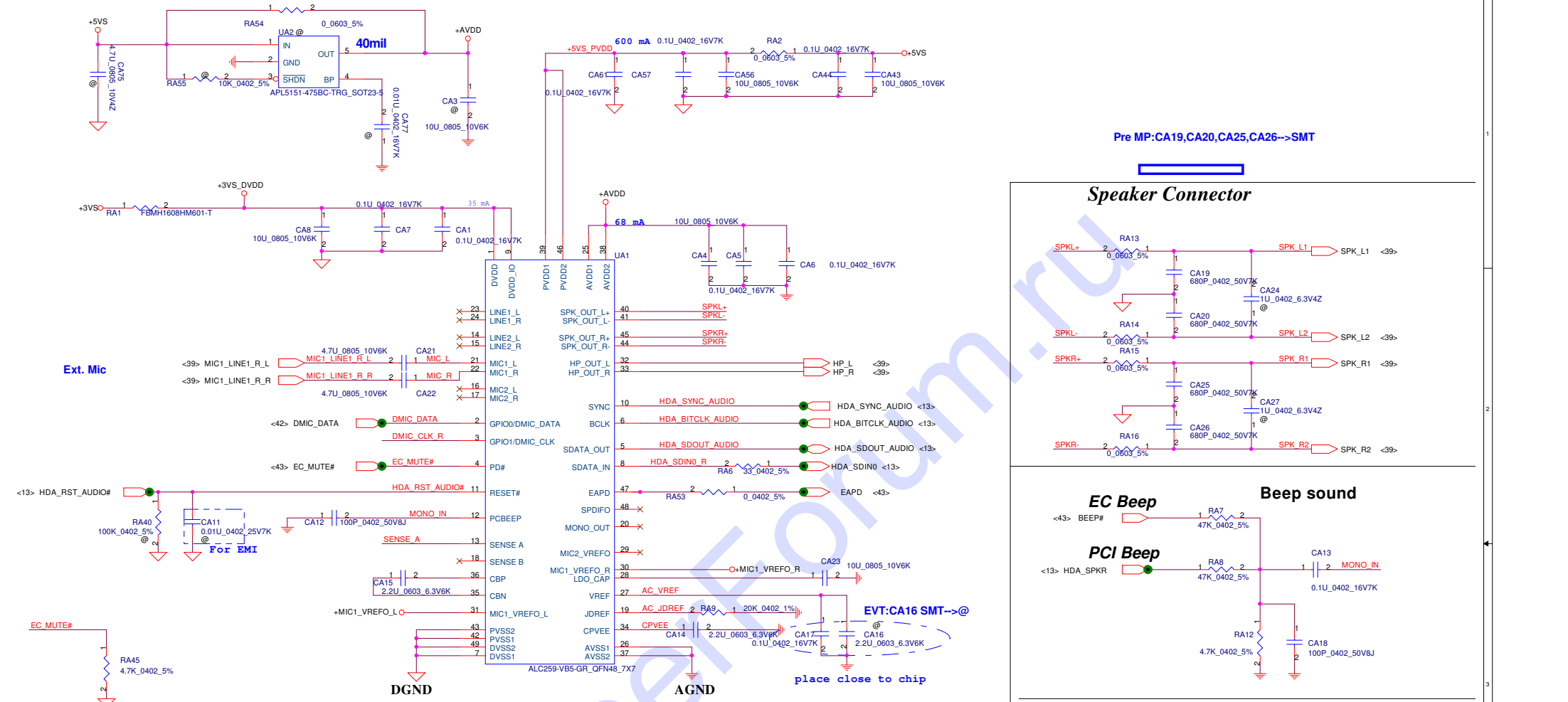

Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	

Security Classification	Compal Secret Data		
Issued Date	2010/04/28	Deciphered Date	2011/04/28

Compal Electronics, Inc.			
Title: Audio ALC259			
Size: Custom	Document Number: LA-7401P		Rev: 1.0
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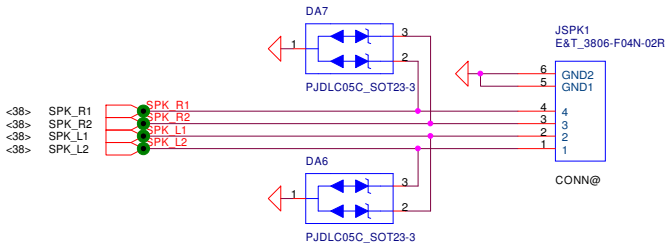
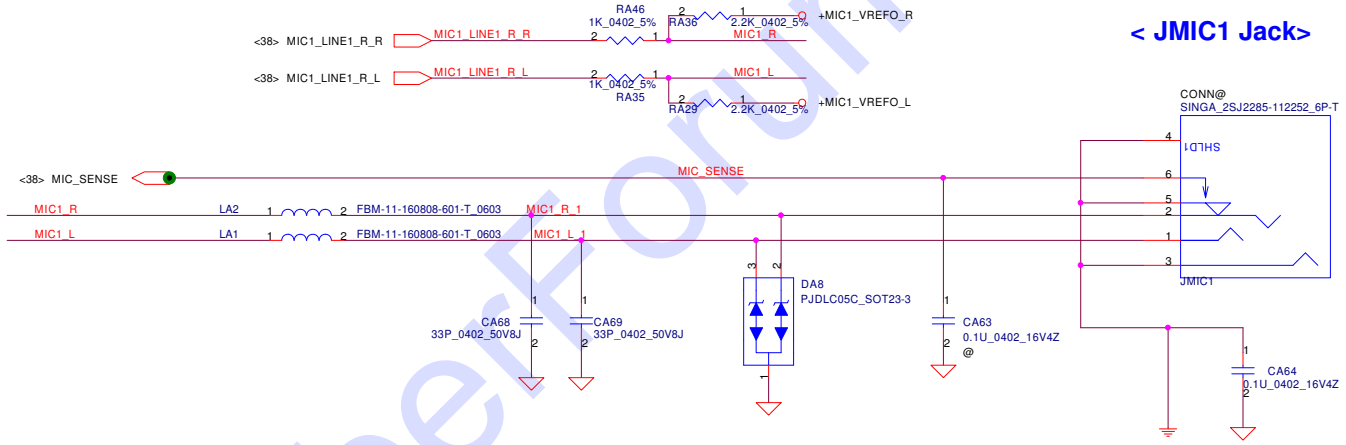
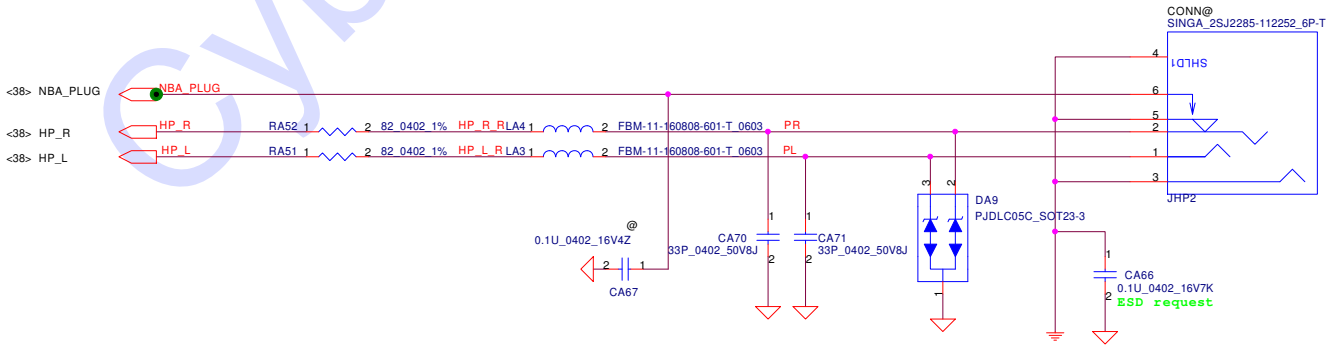
< SPK connector >



< JMIC1 Jack>

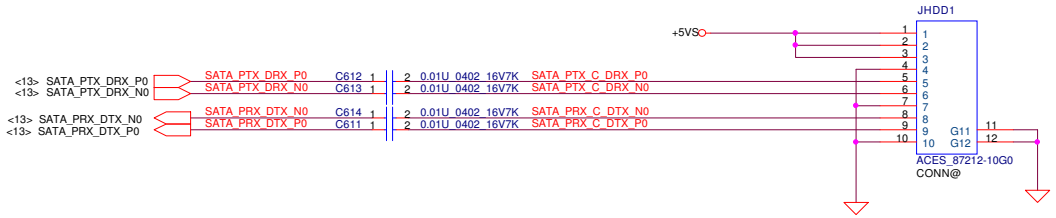


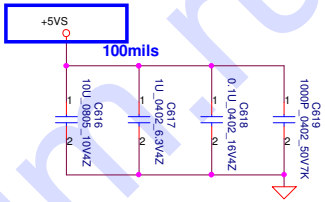
<JHP2 Head phone >

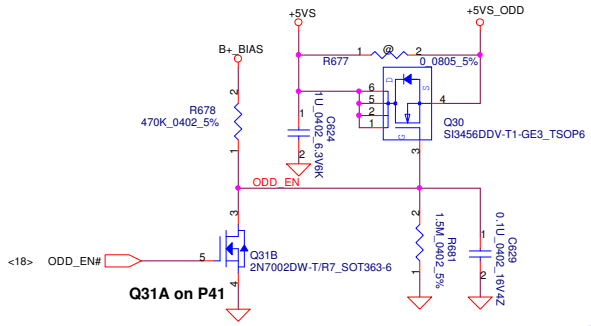


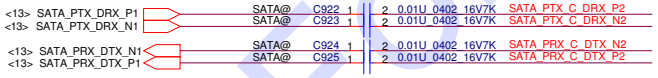
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/04/07	Deciphered Date	2012/10/21
Title	SPK/Jack		
Size	Document Number		Rev
	LA-7401P		1.0
Date:	Monday, April 11, 2011	Sheet	39 of 56

SATA HDD1 Connector

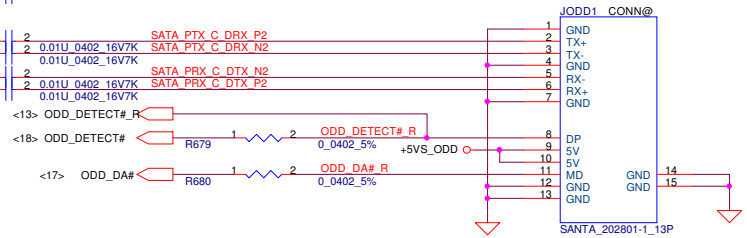


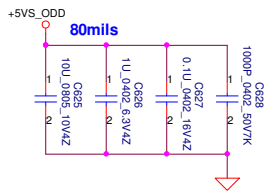






<14" SATA ODD Connector>





Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: HDD/ODD Connector

Size	Document Number	Rev
Custom		1.0

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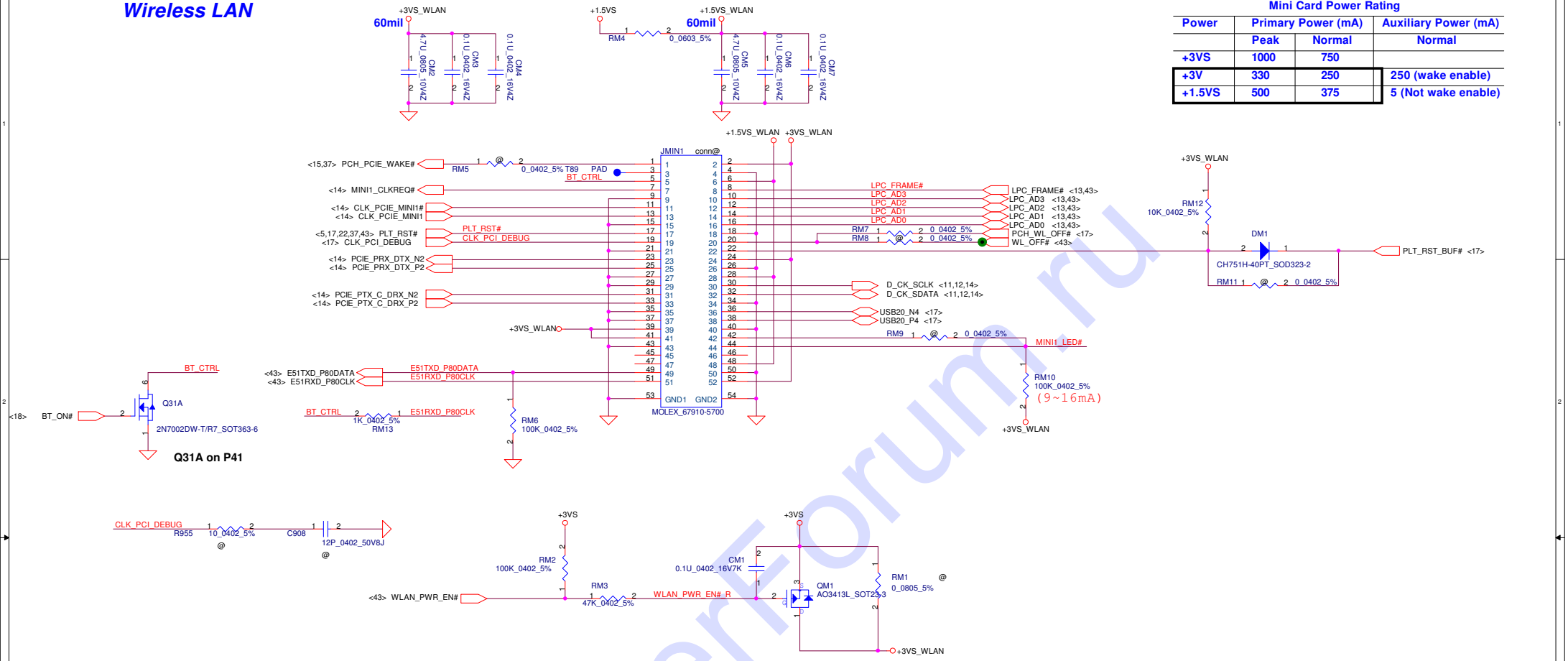
Wireless LAN



Mini Card Power Rating

Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

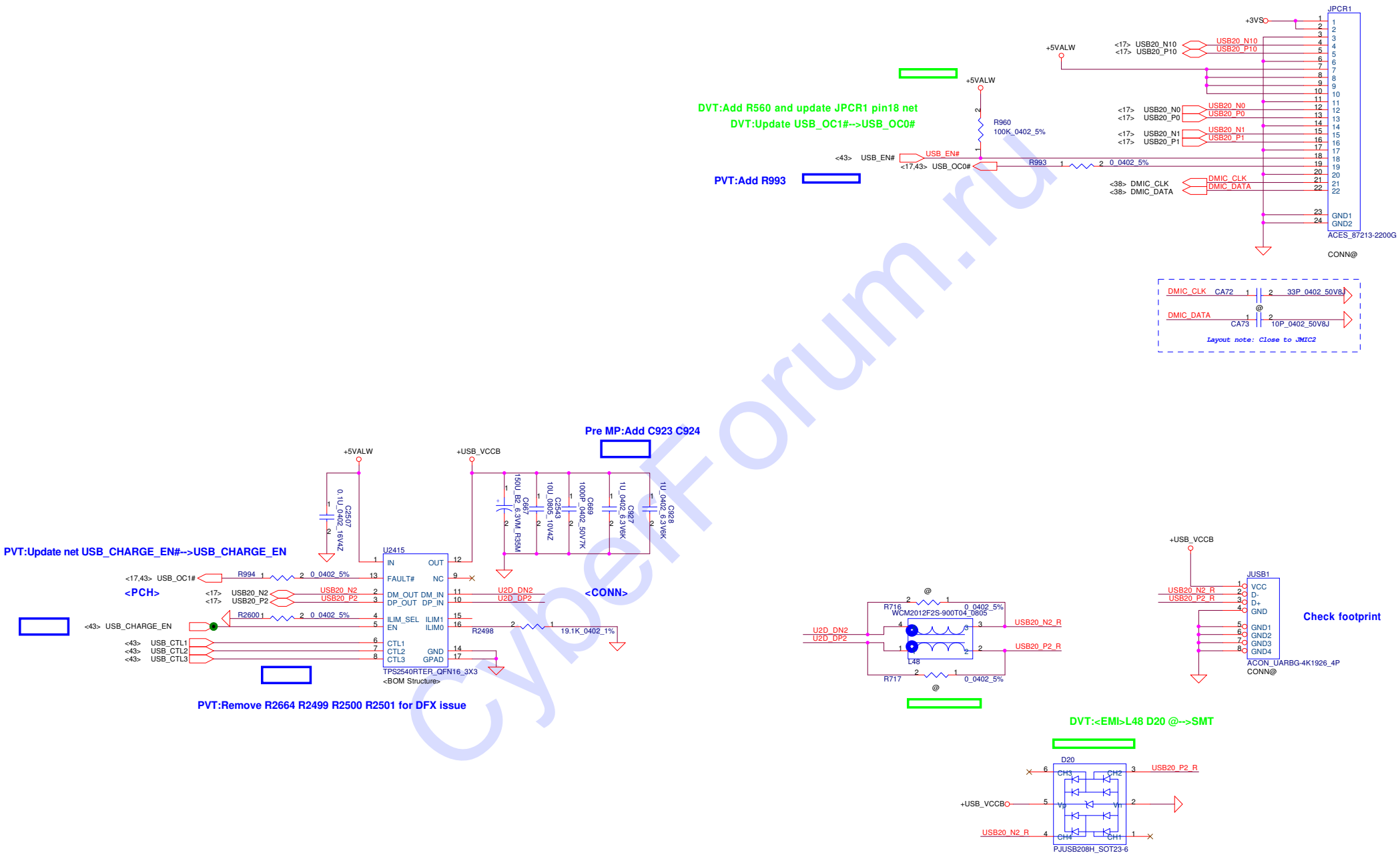
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: MINI CARD WLAN & WWAN

Size	Document Number	Rev
Custom		1.0

Date: Monday, April 11, 2011 Sheet 41 of 56



Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: USB Combo Connector

Size: Custom | Document Number | Rev: 1.0

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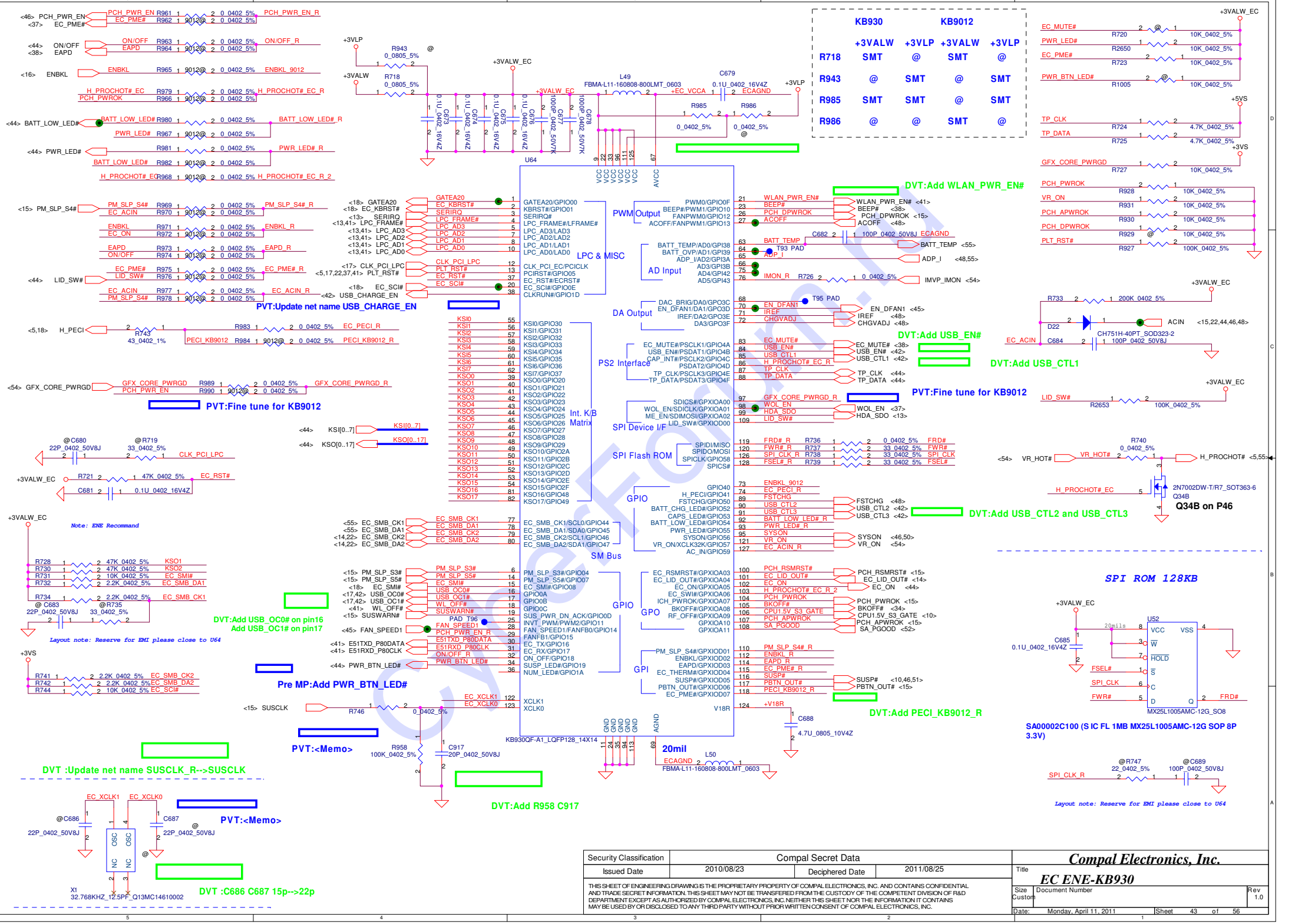
KB930 KB9012
+3VALW +3VLP +3VALW +3VLP
R718 SMT @ SMT @
R943 @ SMT @ SMT
R985 SMT SMT @ SMT
R986 @ @ SMT @
PVT:Update net name USB_CHARGE_EN
PVT:Fine tune for KB9012
DVT:Add WLAN_PWR_EN#
DVT:Add USB_EN#
DVT:Add USB_CTL1
PVT:Fine tune for KB9012
DVT:Add USB_CTL2 and USB_CTL3
Q34B on P46
SPI ROM 128KB
SA00002C100 (S IC FL 1MB MX25L1005AMC-12G SOP 8P 3.3V)
Note: ENE Recommand
Layout note: Reserve for EMI please close to U64
DVT:Add USB_OC0# on pin16
Add USB_OC1# on pin17
Pre MP:Add PWR_BTN_LED#
PVT:<Memo>
DVT :Update net name SUSCLK_R-->SUSCLK
PVT:<Memo>
DVT :C686 C687 15p-->22p
DVT:Add R958 C917
U64
KB930QF-A1_LQFP128_14X14
20mil
U52
MX25L1005AMC-12G_SO8
Security Classification
Compal Secret Data
Issued Date
2010/08/23
Deciphered Date
2011/08/25
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Compal Electronics, Inc.
Title
EC ENE-KB930
Size Custom
Document Number
Rev 1.0
Date: Monday, April 11, 2011
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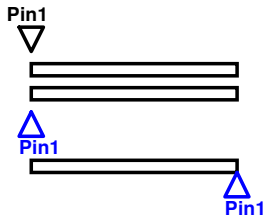
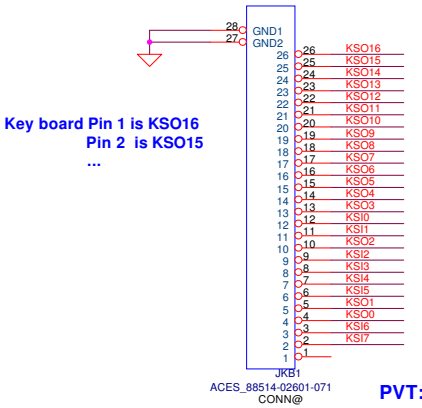
INT_KBD Connector
New key board

Key board pin define (Down)

CIS symbol (DVT)

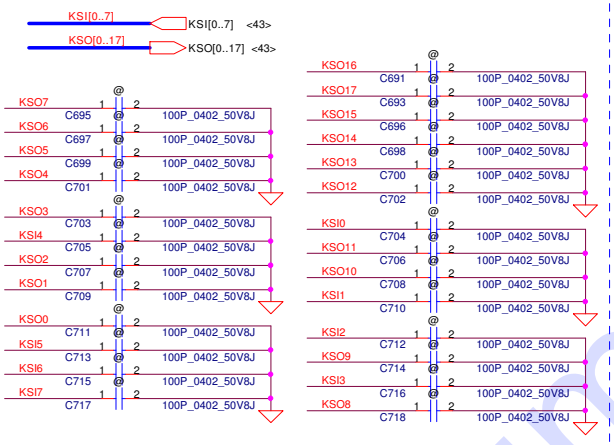
CIS symbol (PVT need reverese pin define)



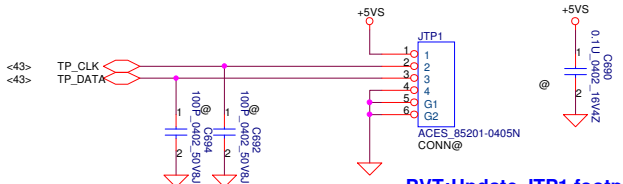


Key board Pin 1 is KSO16
Pin 2 is KSO15
...

PVT:Update JKB1 footprint

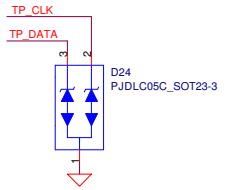


<T/P conn>

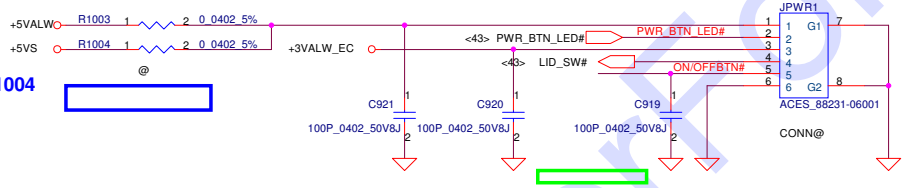


PVT:Update JTP1 footprint

EVT:Check pin define



<Power Button/Lid B conn>



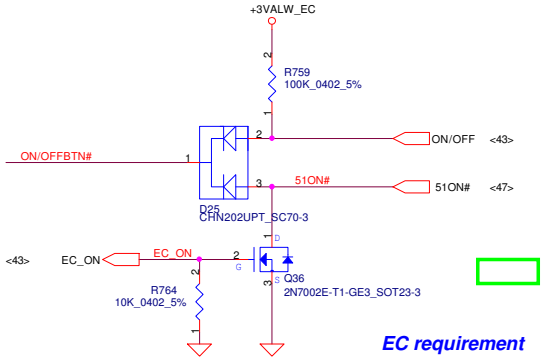
Pre MP:Add R1003 R1004

DVT:Update JPWR1 footprint and pin define

Pre MP:Update JPWR1 pin define

Power Button

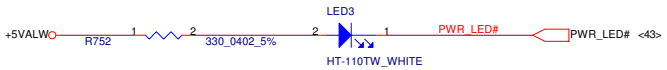
DVT:R759 pin1 +3VALW-->+3VALW_EC



DVT:Del R937

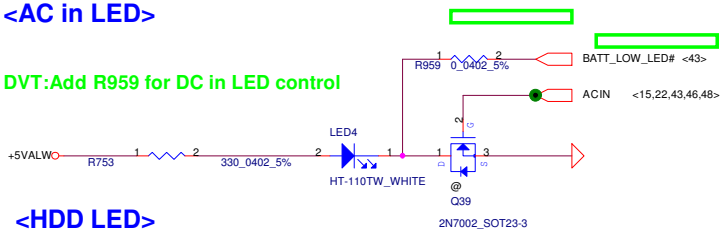
EC requirement

<Power on LED>

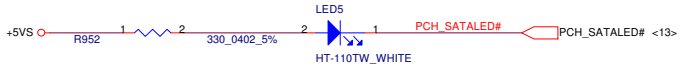


<AC in LED>

DVT:Add R959 for DC in LED control



<HDD LED>



Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: KB/TP/LED/FUNC

Size	Document Number	Rev
B		1.0

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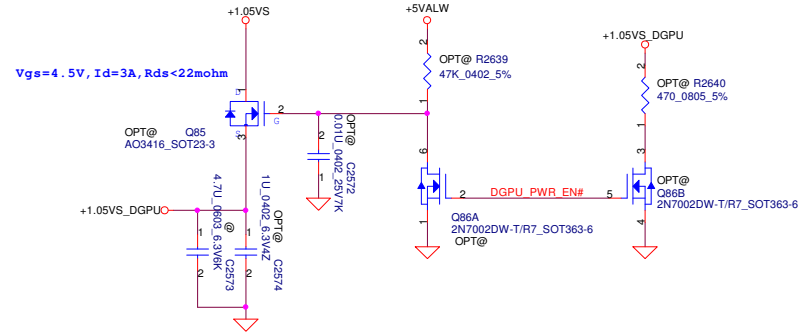
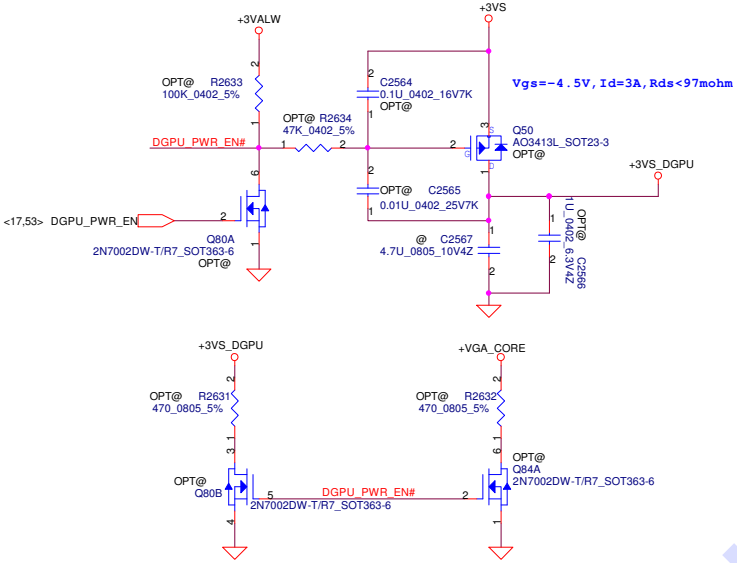
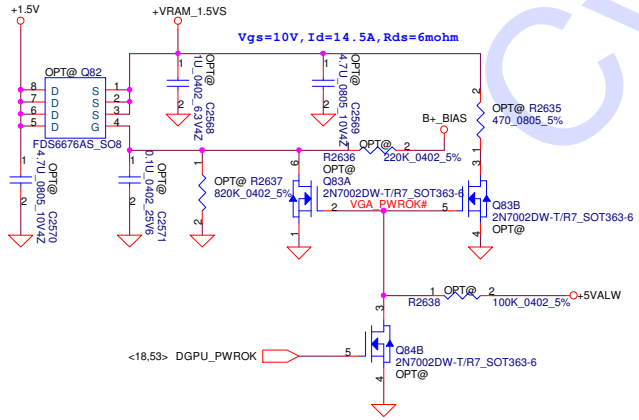
+1.05VS to +1.05VS_DGPU



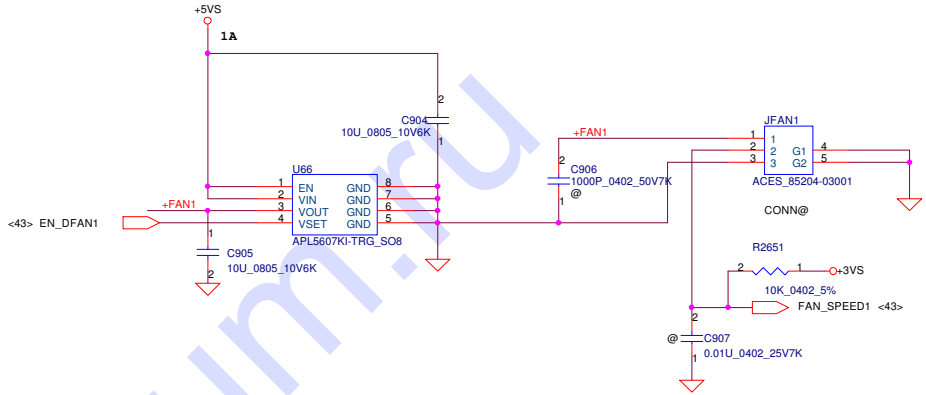
+3VS TO +3VS_DGPU



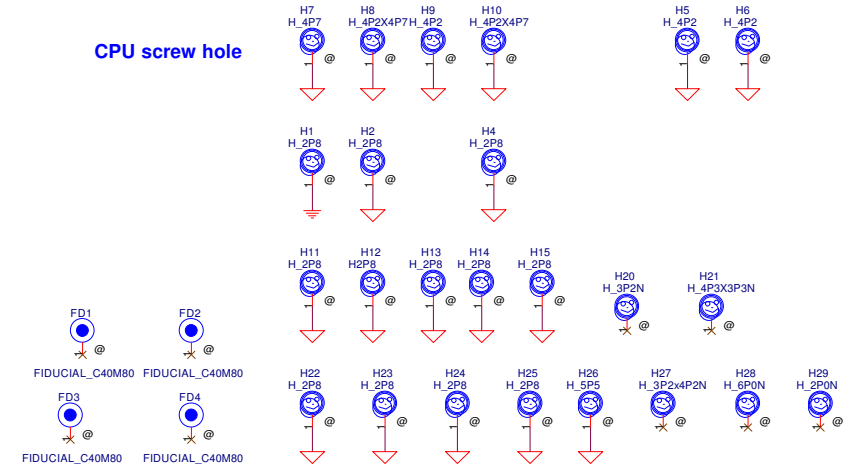
+1.5V to +VRAM_1.5VS



FAN Connector



CPU screw hole



Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: Optimus Power/FAN/Screw Hole

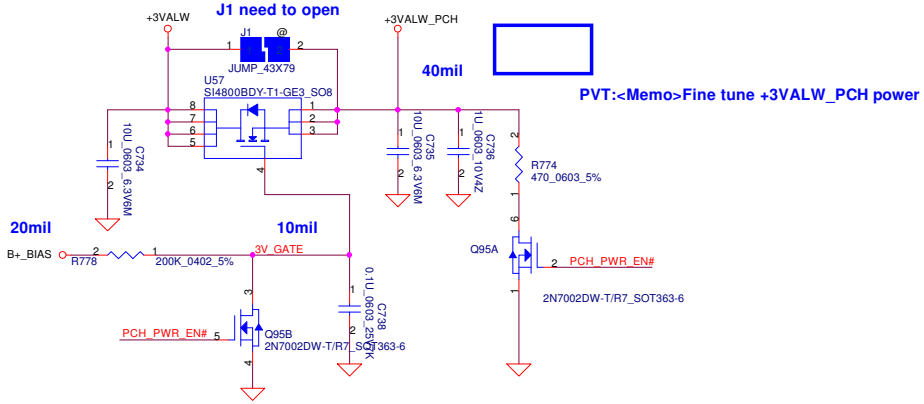
Size	Document Number	Rev
Custom		1.0

Date: Sunday, April 10, 2011 Sheet 45 of 56

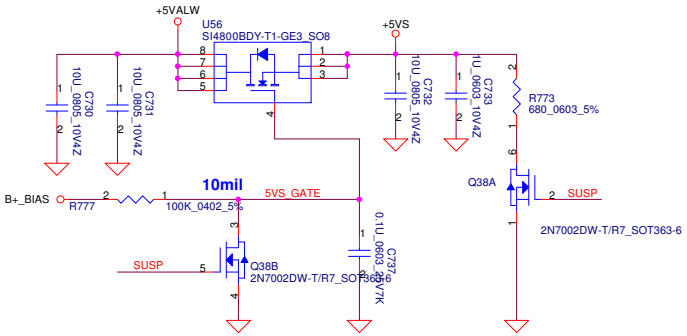
+3VALW TO +3VALW(PCH AUX Power)

Short J1 for PCH VCCSUS3.3

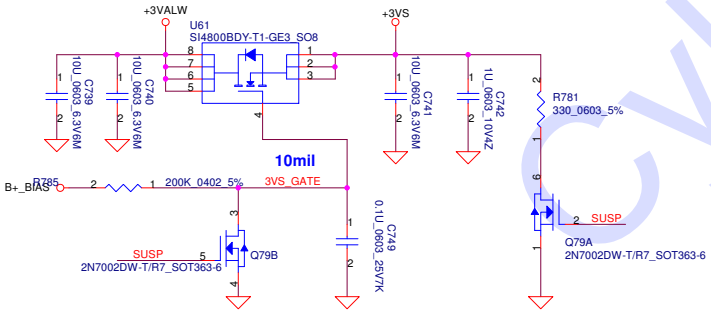
J1 need to open



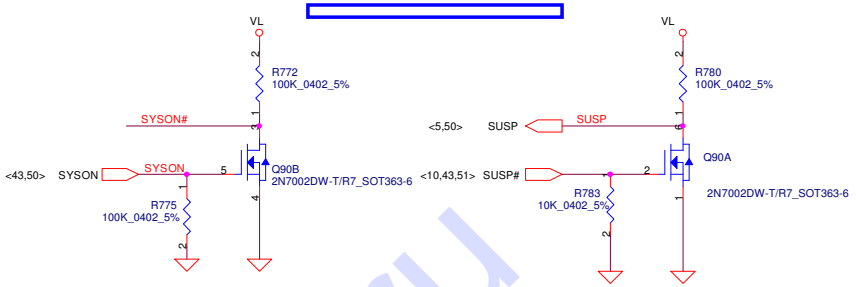
+5VALW TO +5VS

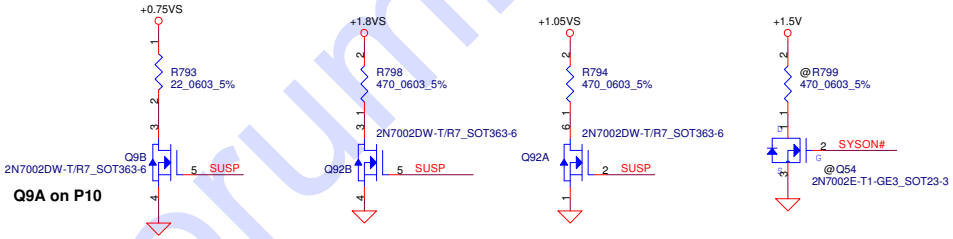


+3VALW TO +3VS

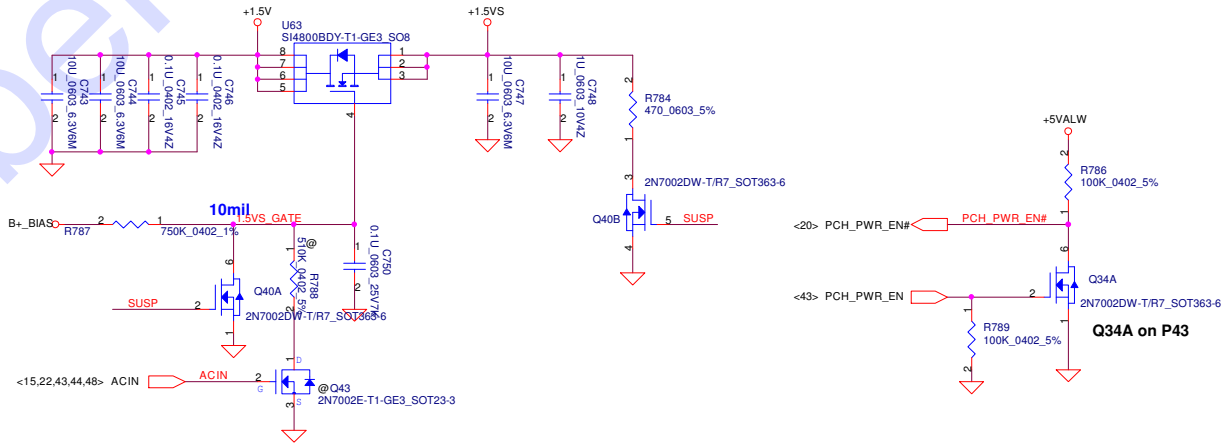


PVT:R780 R772 +5VALW-->VL





+1.5V to +1.5VS



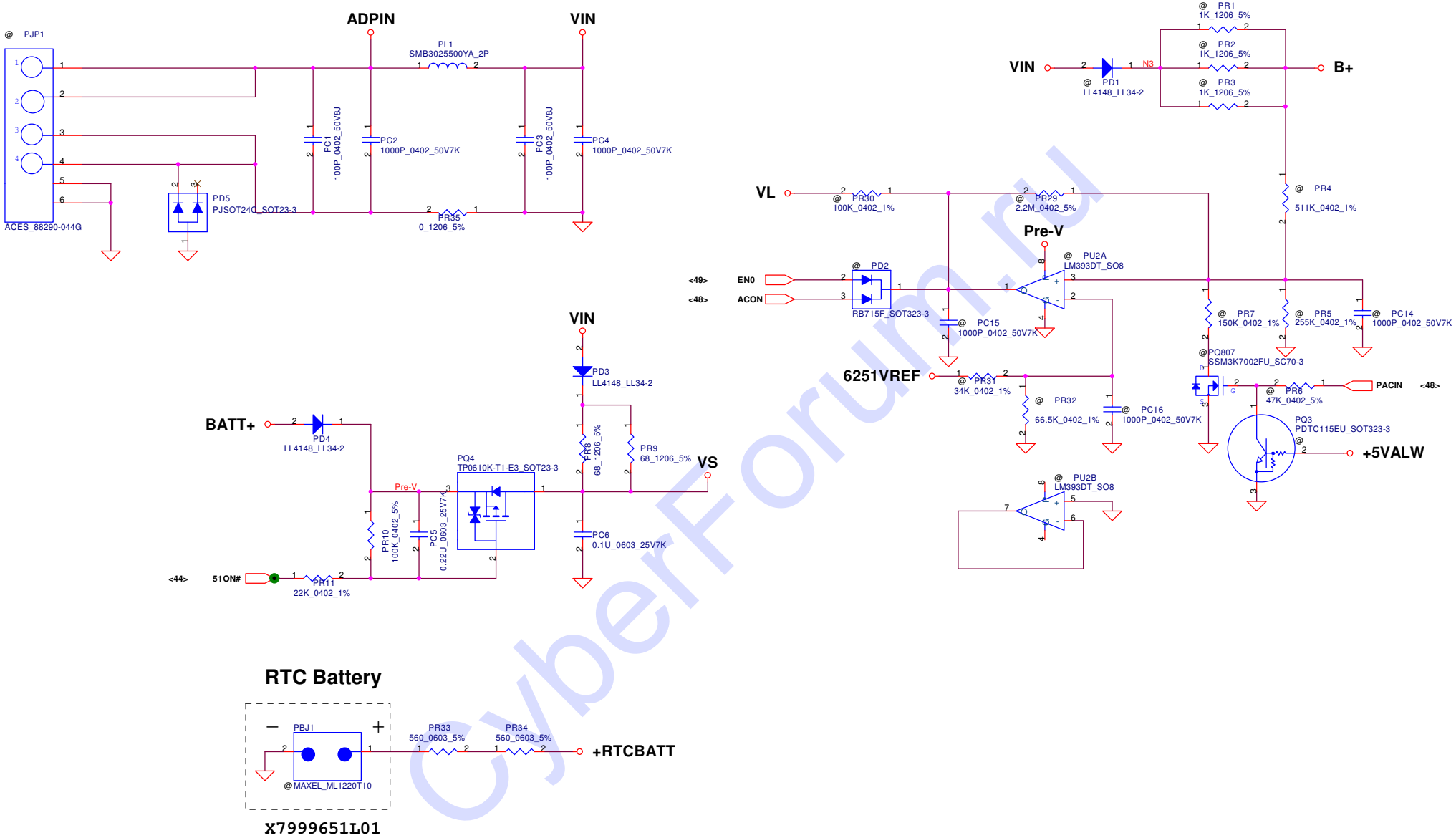
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: DC-DC Interface

Size: Custom | Document Number | Rev: 1.0

Date: Sunday, April 10, 2011 | Sheet 46 of 56

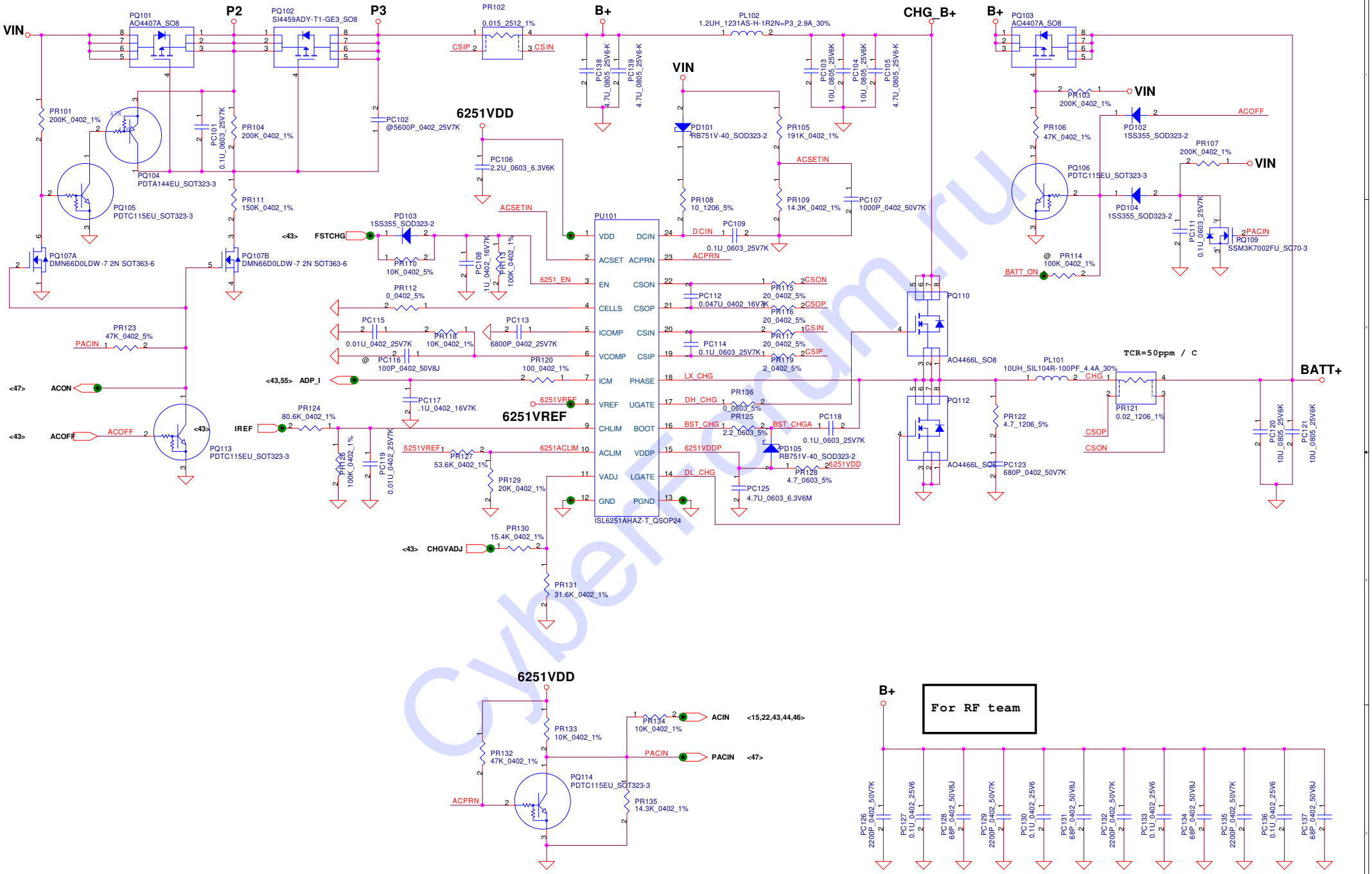


Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

Title: **PWR-DCIN / Pre-Charge / RTC**

Size	Document Number	Rev
Custom	DB-806P	0.1

Date: Monday, April 11, 2011 Sheet 47 of 56



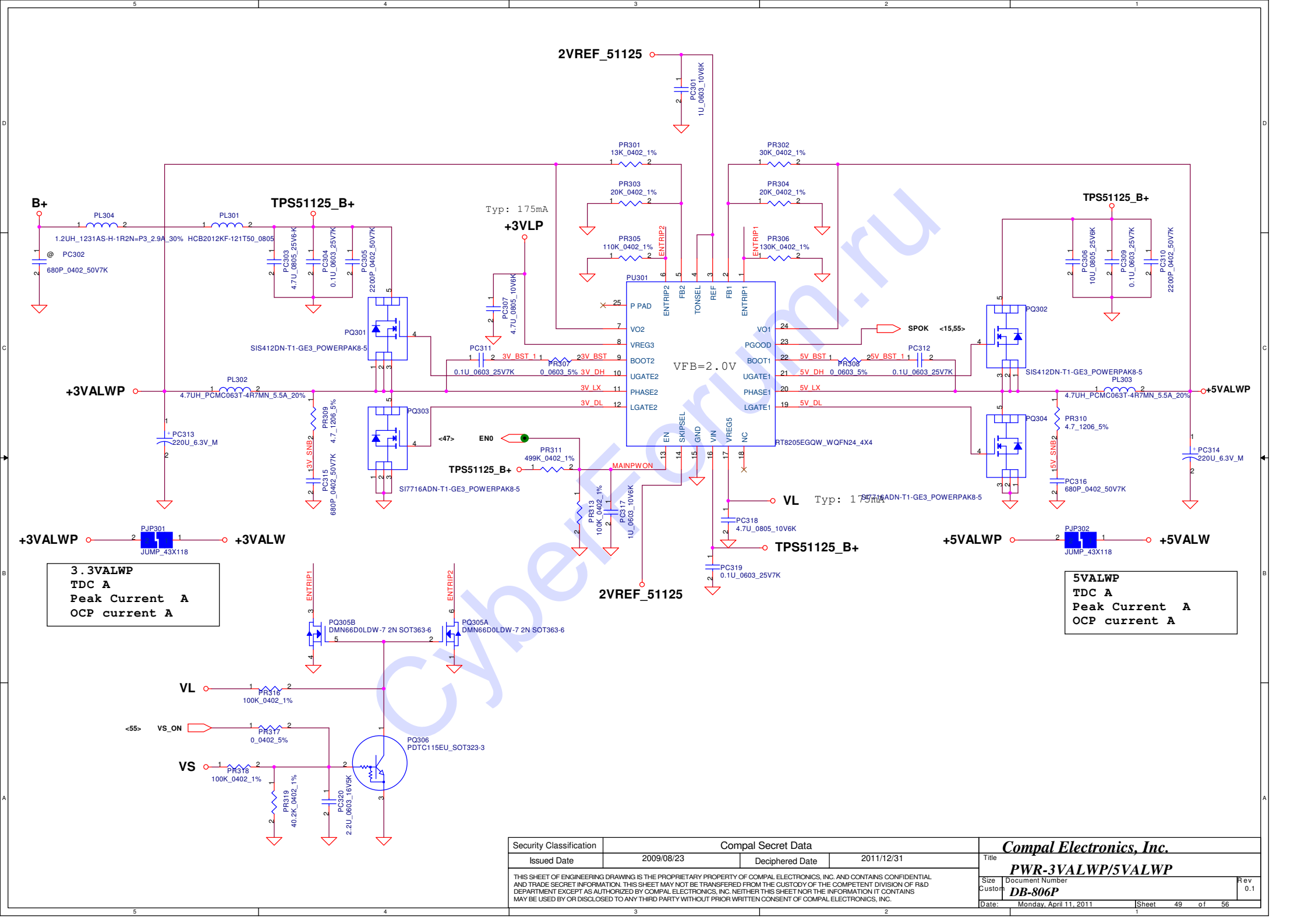
Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: **PWR-CHARGER**

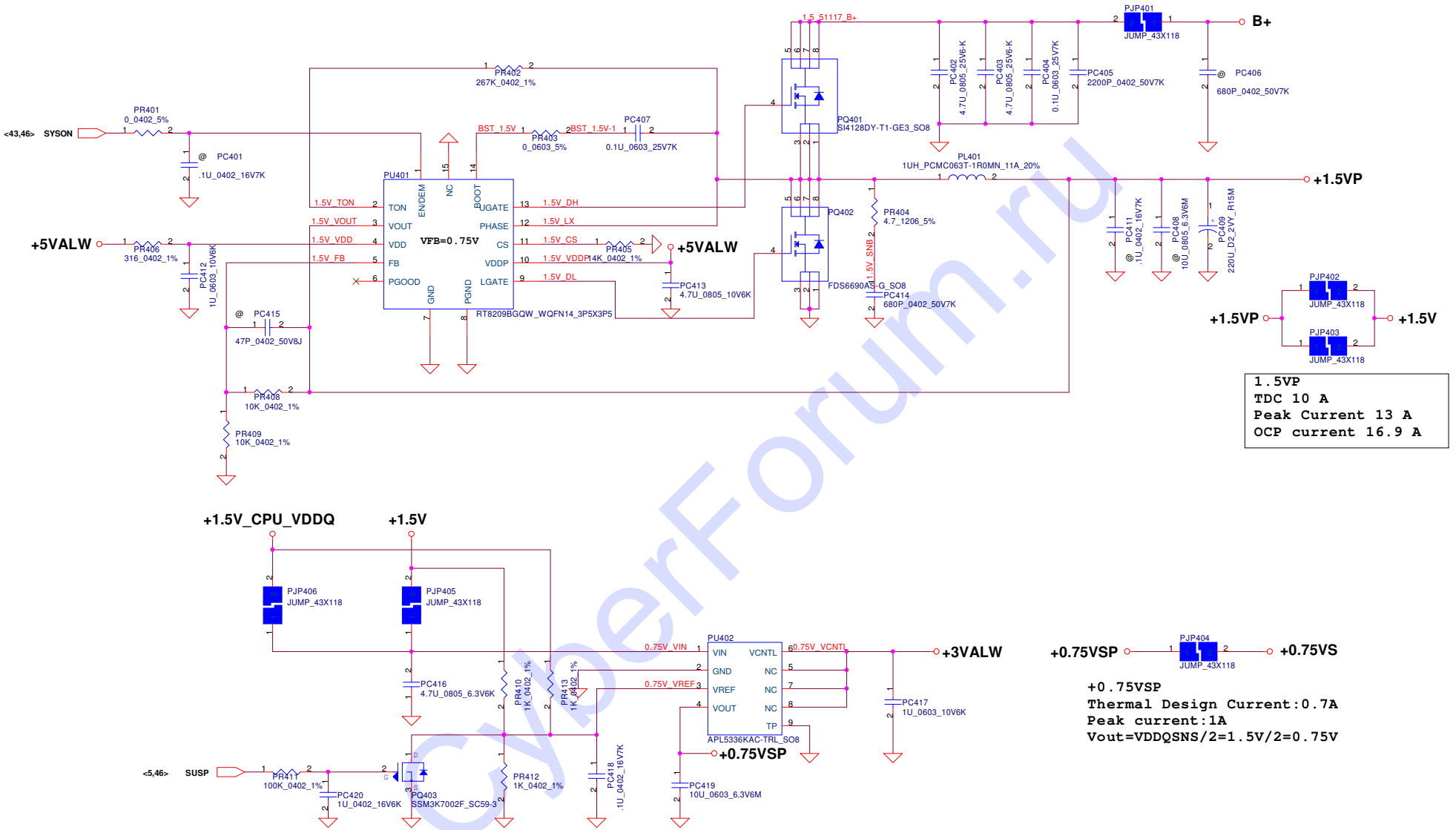
Size: Custom | Document Number: **DB-806P** | Rev: 0.1

Date: Monday, April 11, 2011 | Sheet 48 of 56



Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

Compal Electronics, Inc.			
Title: PWR-3VALWP/5VALWP			
Size: Custom	Document Number: DB-806P		Rev: 0.1
Date: Monday, April 11, 2011		Sheet 49 of 56	



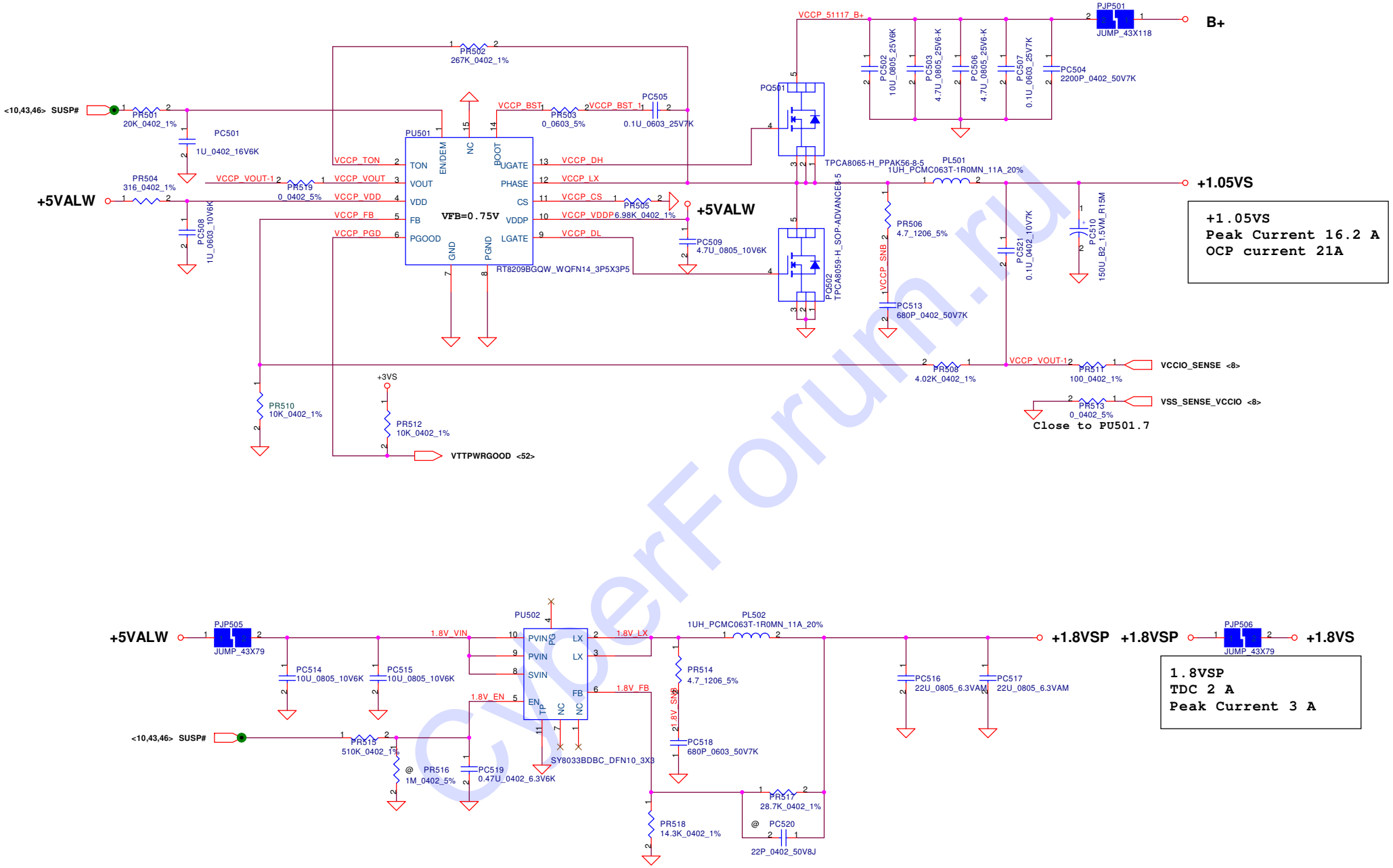
Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: **PWR-1.5VP/0.75VSP**

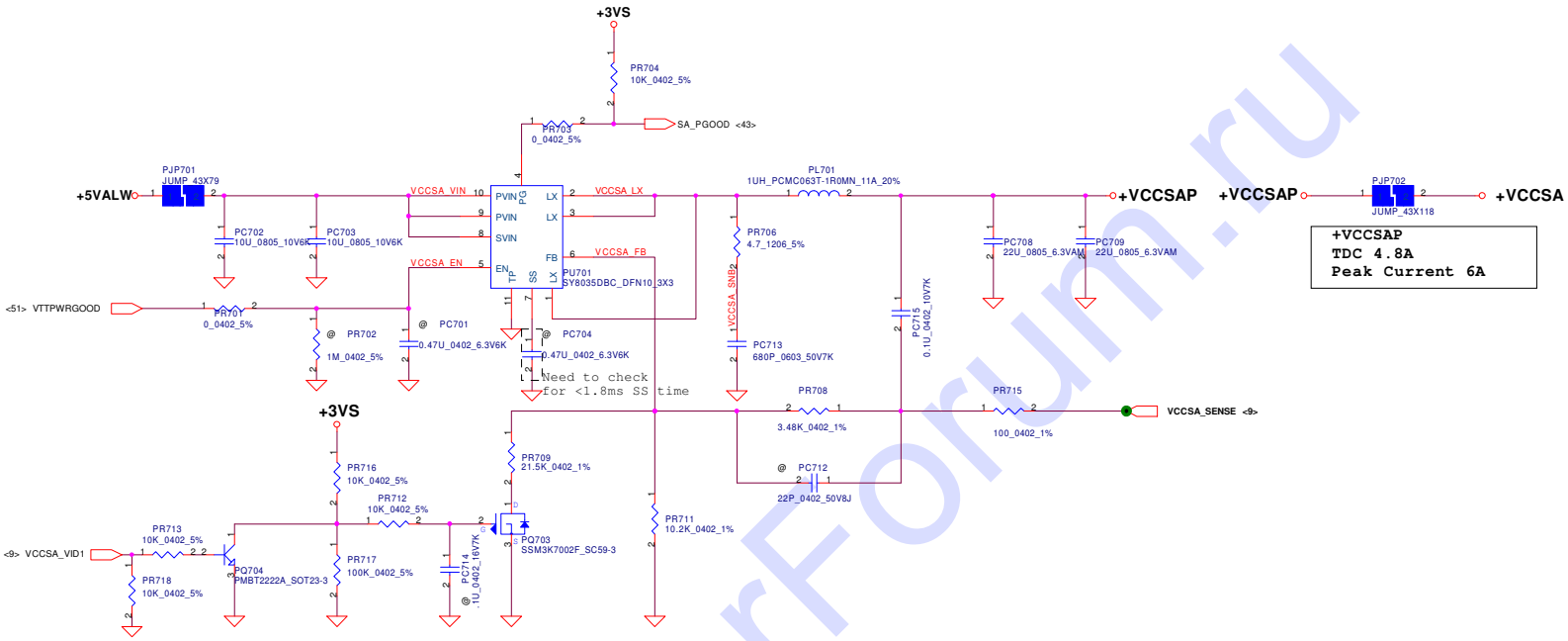
Size	Document Number	Rev
Custom		0.1

Date: Sunday, April 10, 2011 | Sheet 50 of 56



Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

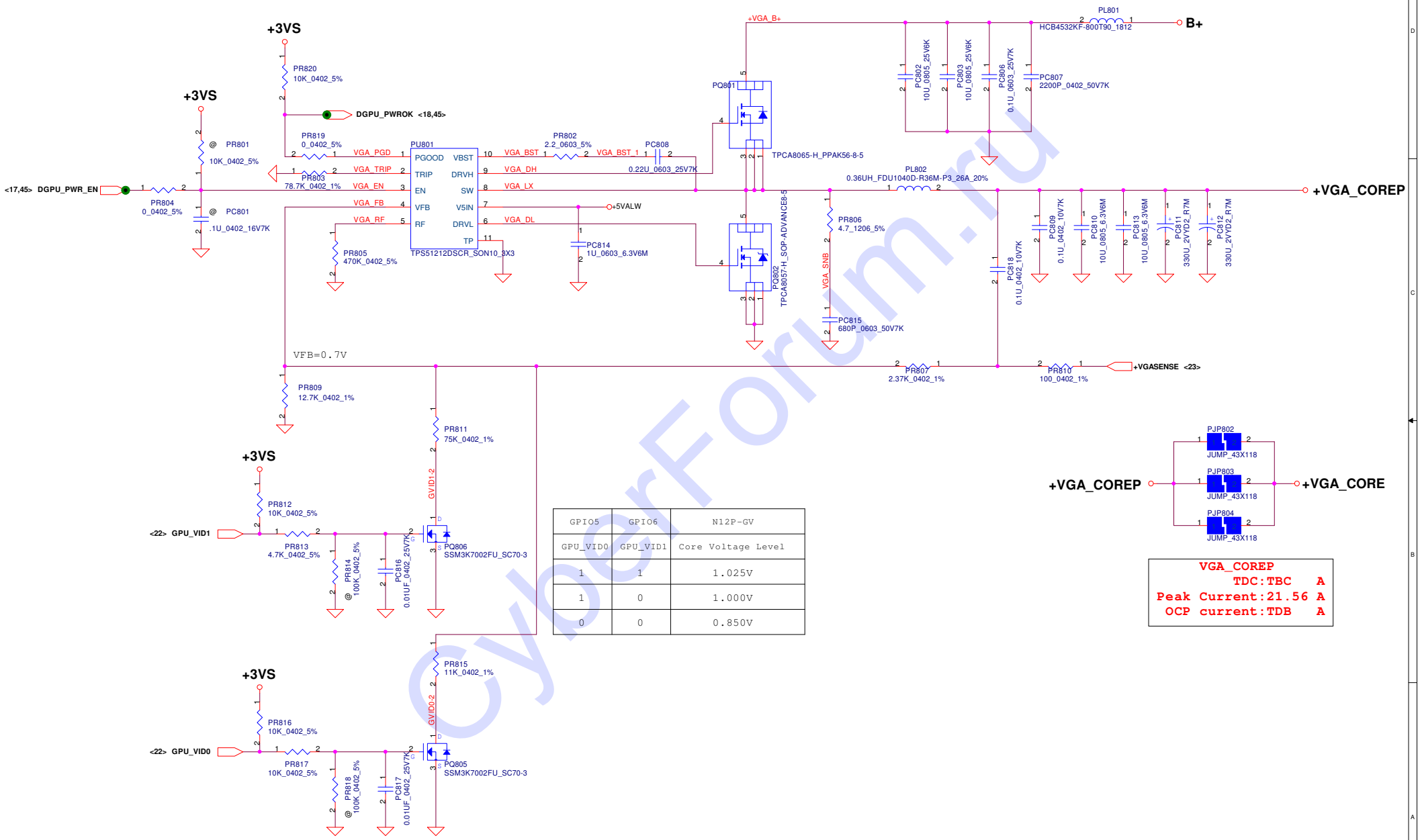
Compal Electronics, Inc.			
Title: PWR-VCCPP/1.8VSP			
Size: Custom	Document Number: DB-806P		Rev: 0.1
Date: Monday, April 11, 2011	Sheet 51 of 56		



VID[1]	VCCSA Vout	Required	Require on 2012	
0	0.9V		Yes	Yes
1	0.8V		Yes	Yes

Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

Compal Electronics, Inc.			
Title	PWR-VCCSAP		
Size C	Document Number DB-806P		Rev 0.1
Date: Monday, April 11, 2011		Sheet 52 of 56	

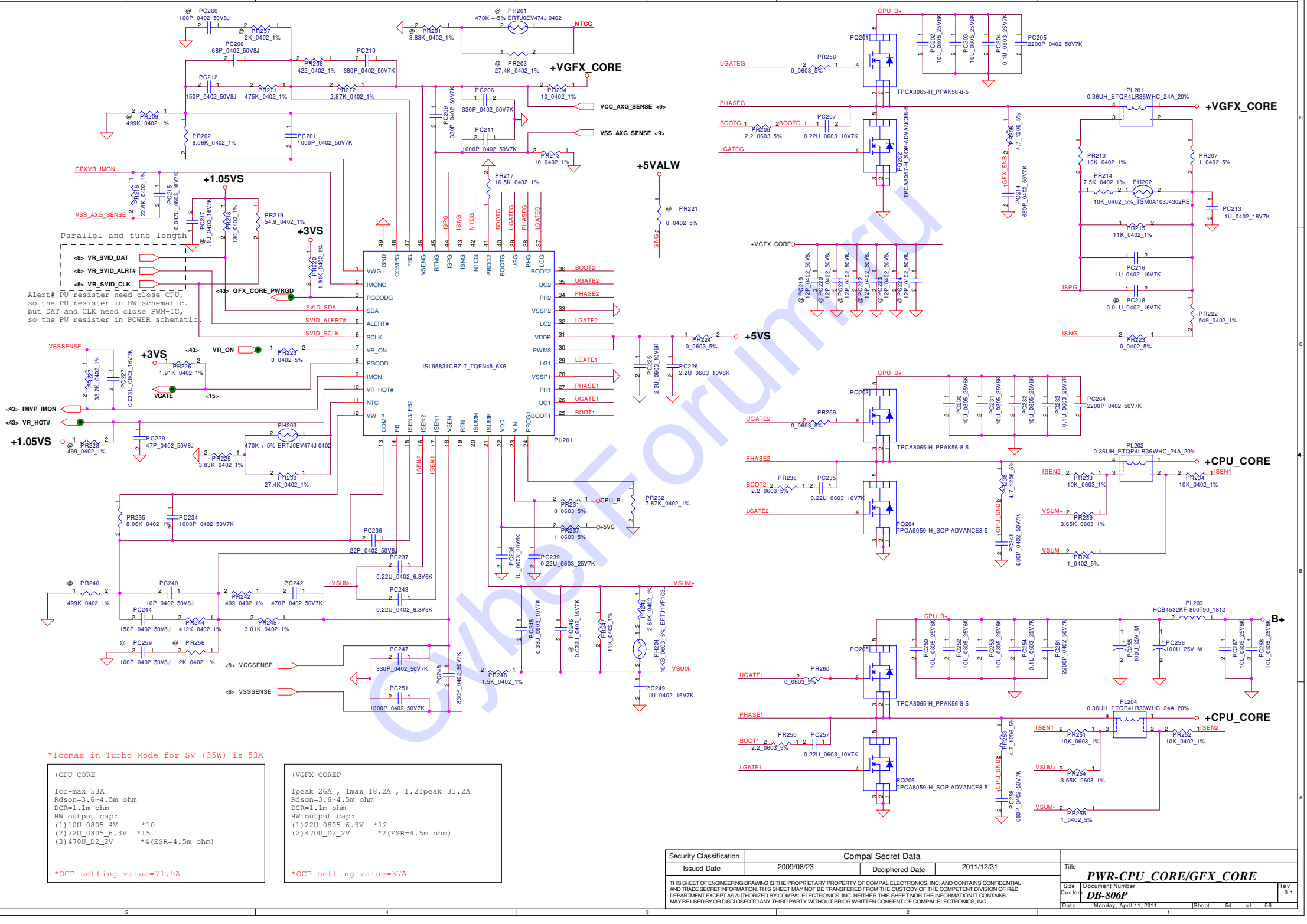


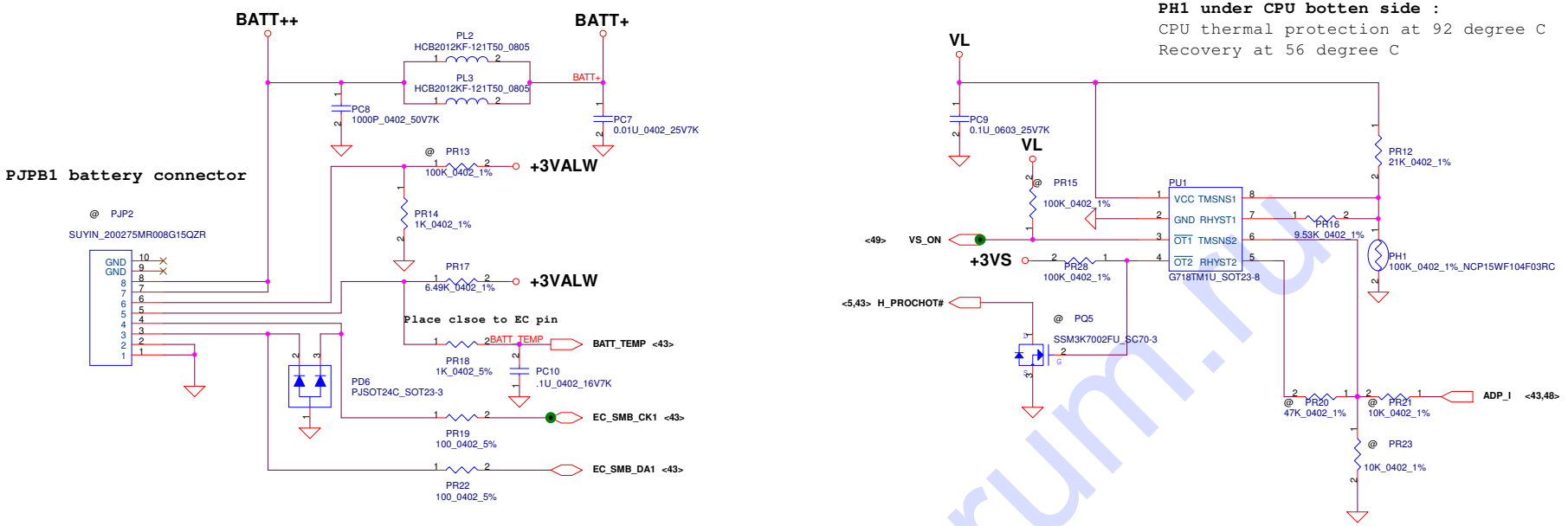
GPIO5	GPIO6	N12P-GV
GPU_VID0	GPU_VID1	Core Voltage Level
1	1	1.025V
1	0	1.000V
0	0	0.850V

VGA_COREP
TDC:TBC A
Peak Current:21.56 A
OCP current:TDB A

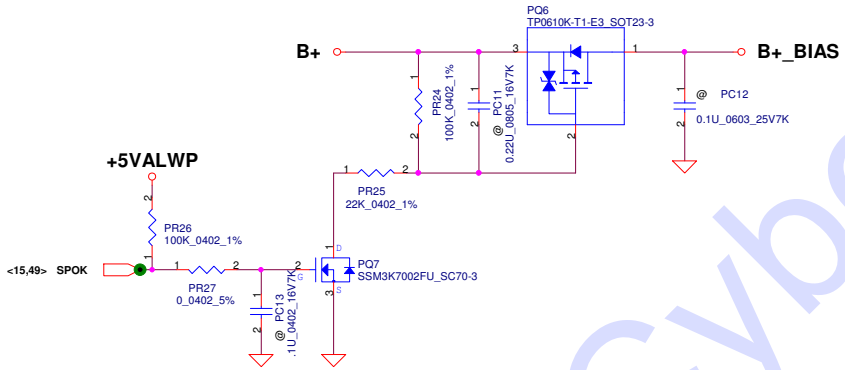
Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

Title	PWR-VGA_CORE		
Size: Custom	Document Number: DB-806P		Rev: 0.1
Date: Monday, April 11, 2011	Sheet 53 of 56		



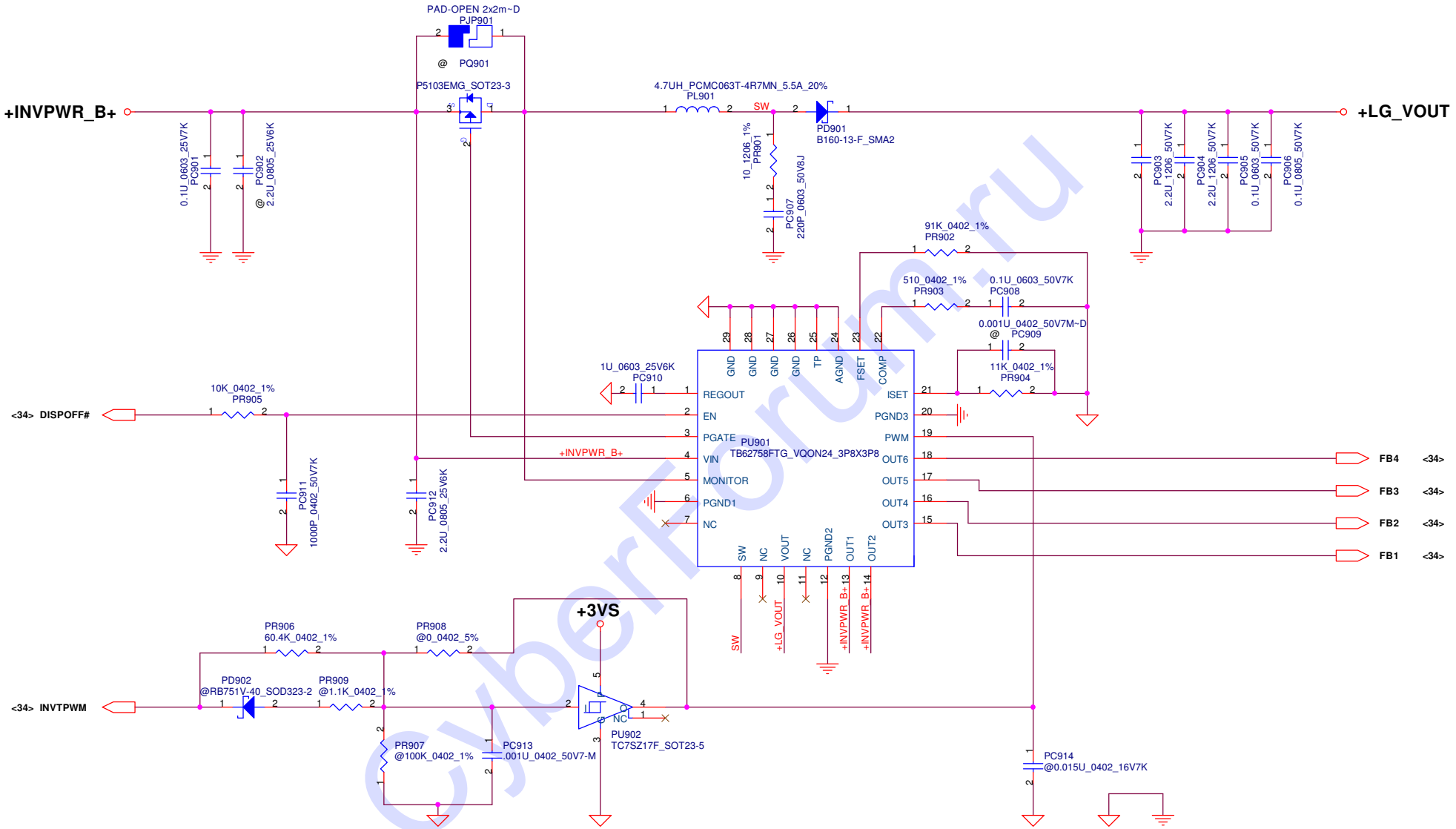


PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

Compal Electronics, Inc.			
Title	PWR-BATTERY CONN		
Size Custom	Document Number DB-806P		Rev 0.1
Date: Monday, April 11, 2011	Sheet 55 of 56		



Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

Title: **PWR-LED Converter**

Size: B | Document Number: **DB-806P** | Rev: 0.1

Date: Sunday, April 10, 2011 | Sheet 56 of 56