Compal confidential

JBK00 LA-4092P Schematics Document

Mobile AMD S1G2 CPU with ATI RX781 & SB700 core logic with M82-S

2008-02-20

REV:0.4

機密 等級 硬體二部 產出人員 產出日期 解密日期

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Title: *Cover Sheet*		
Size: Custom	Document Number: *LA-4092P*	Rev: 0.4
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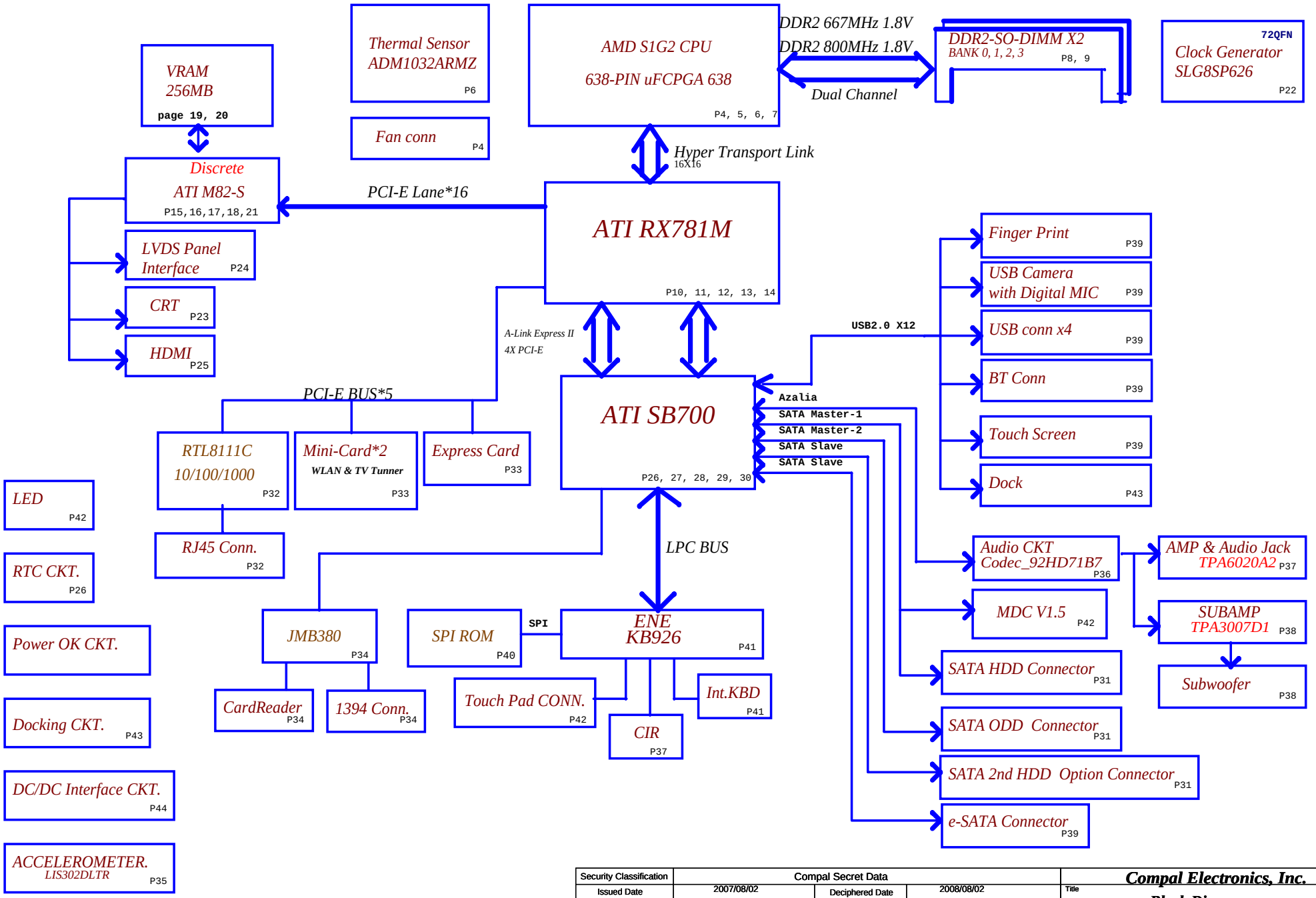
Consumer AMD UMA/DISCRETE 17"



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Title: **Block Diagram**

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Voltage Rails

State \ power plane	+B +3VL +5VL	+5VALW +3VALW +1.2VALW +3V_LAN	+1.8V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +VGA_CORE +1.2V_HT +CPU_CORE_NB +CPU_CORE_0 +CPU_CORE_1
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

O MEANS ON X MEANS OFF

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

Layout Notes

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010
ACCELEROMETER	3A	00111010

EC SM Bus1 address

Device	HEX	Address
Smart Battery	16H	0001 011X b
24C16	A0H	1010 000X b
CPU SIC interface	98H	1001 100X b

EC SM Bus2 address

Device	HEX	Address
ADI1032-2 CPU	9AH	1001 101X b
ADI1032-1 VGA	98H	1001 100X b

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR CPU & ADM1032	SODIMM I / II	CLK CHIP	MINI CARD Slot 2	LCD	HDMI	G-Sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X
I2C_CLK I2C_DATA	RS780M	X	X	X	X	X	X	X	V	X	X
DDC_CLK0 DDC_DATA0	RS780M	X	X	X	X	X	X	X	X	V	X
DDC_CLK1 DDC_DATA1	RS780M	X	X	X	X	X	X	X	X	X	X
SCL0 SDA0	SB700	X	X	X	X	V	V	X	X	X	V
SCL1 SDA1	SB700	X	X	X	X	X	X	V	X	X	X
SCL2 SDA2	SB700	X	X	X	X	X	X	X	X	X	X
SCL3 SDA3	SB700	X	X	X	X	X	X	X	X	X	X

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Title: Notes List

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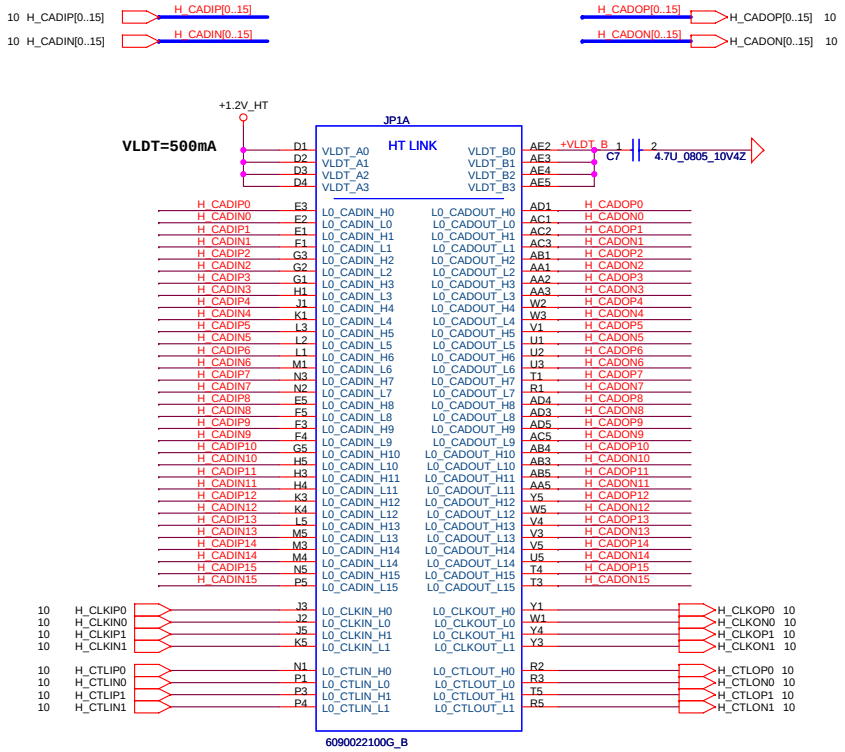
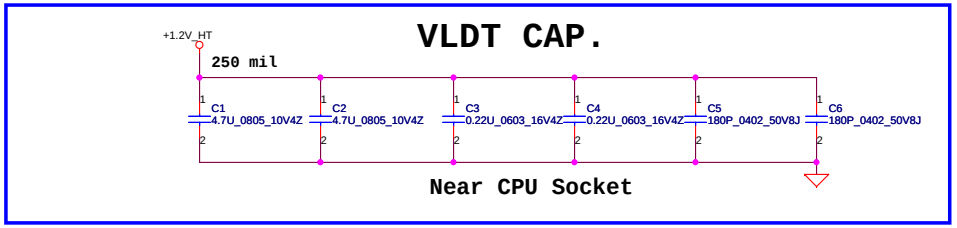
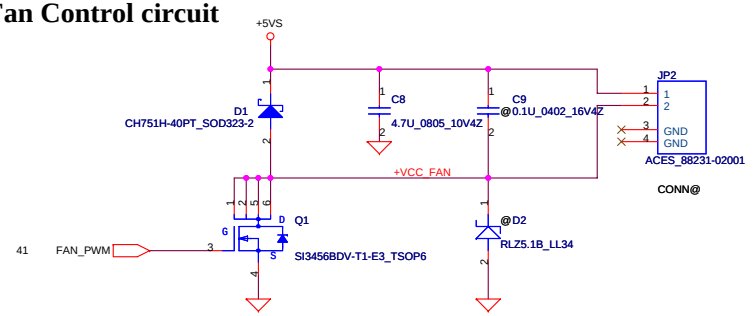




PWM Fan Control circuit



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Compal Electronics, Inc.			
Title: AMD CPU S1G2 HT I/F			
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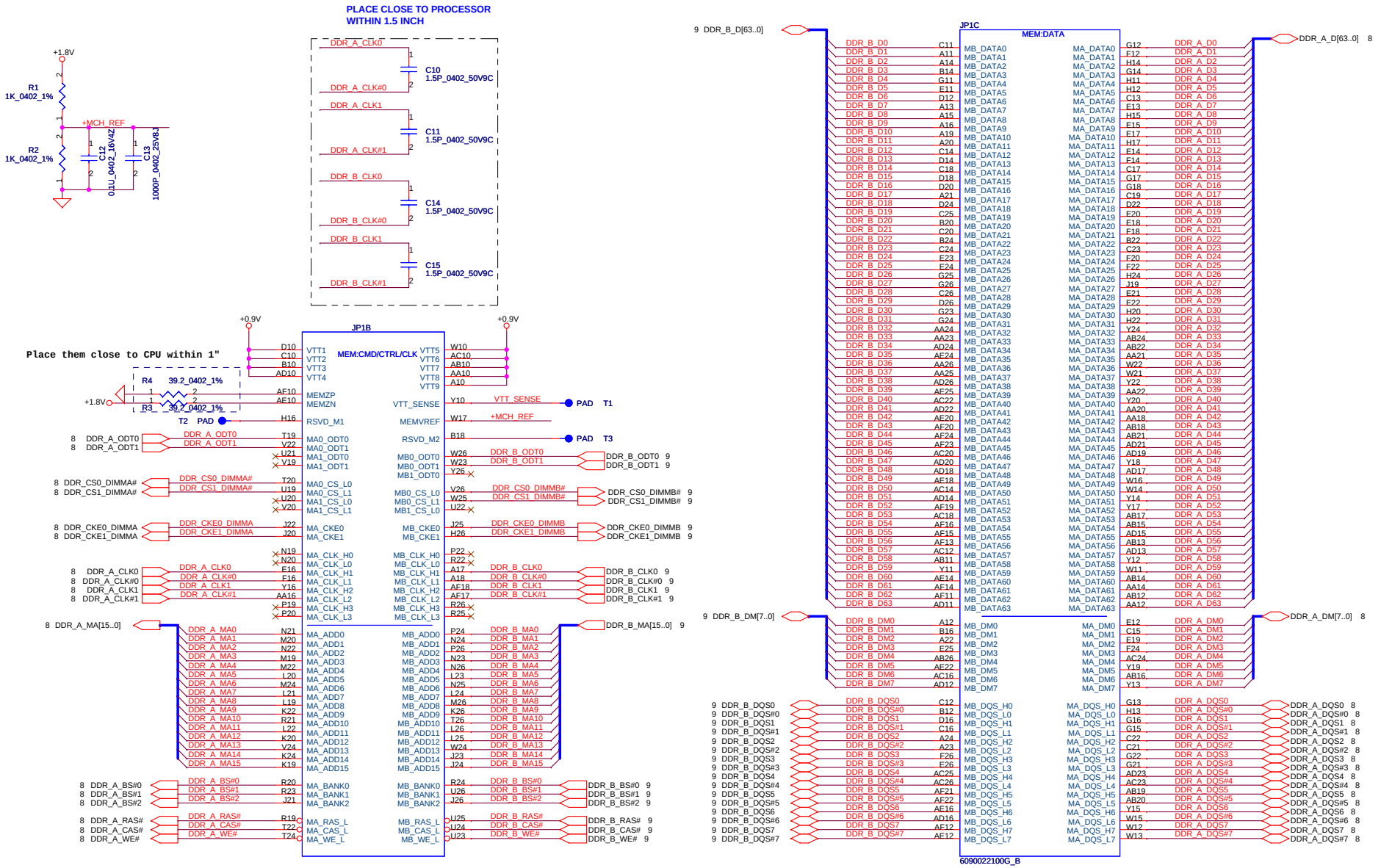
Processor DDR2 Memory Interface



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Title: **AMD CPU S1G2 DDRII I/F**

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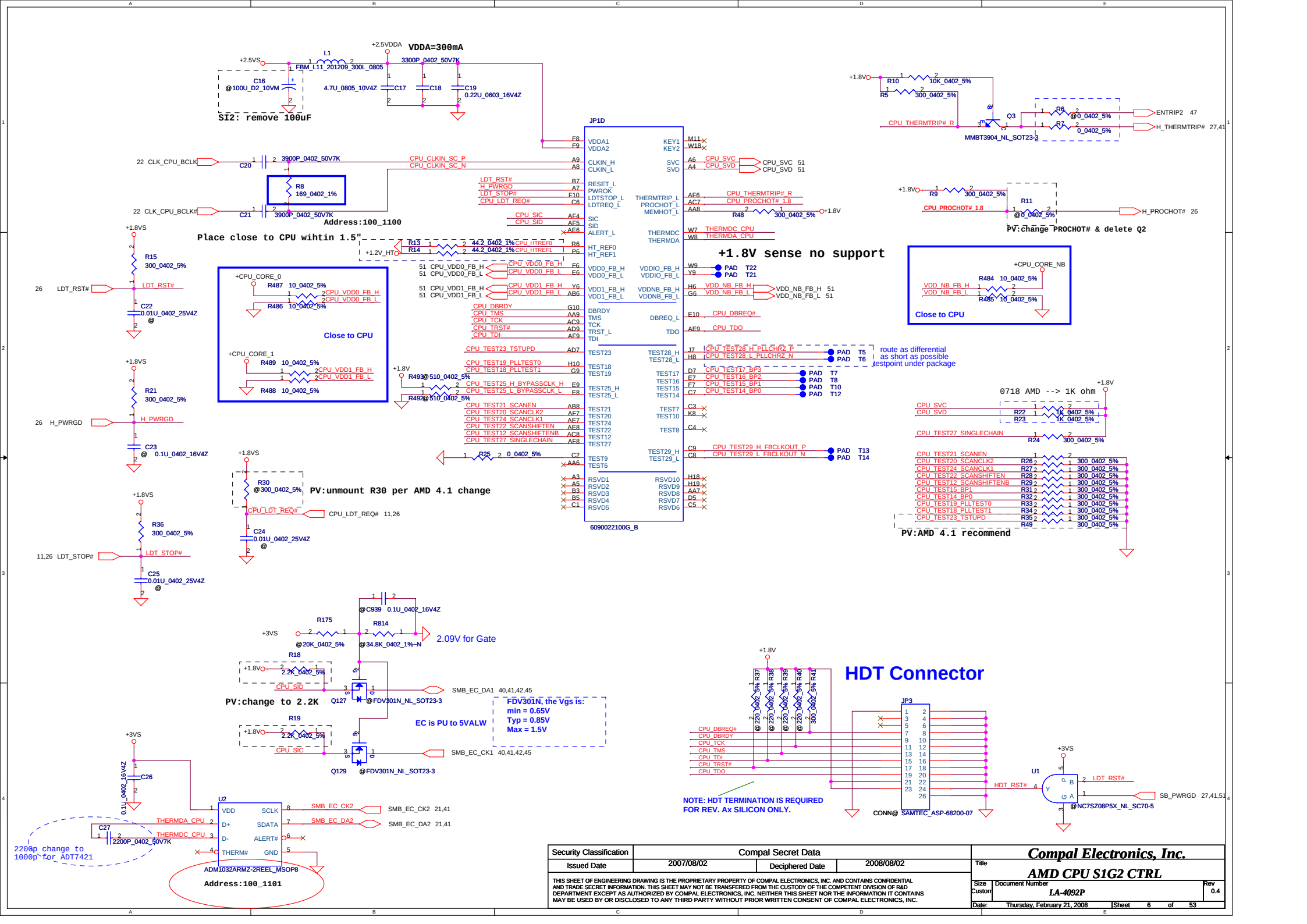

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Compal Electronics, Inc.			
Title: AMD CPU S1G2 CTRL			
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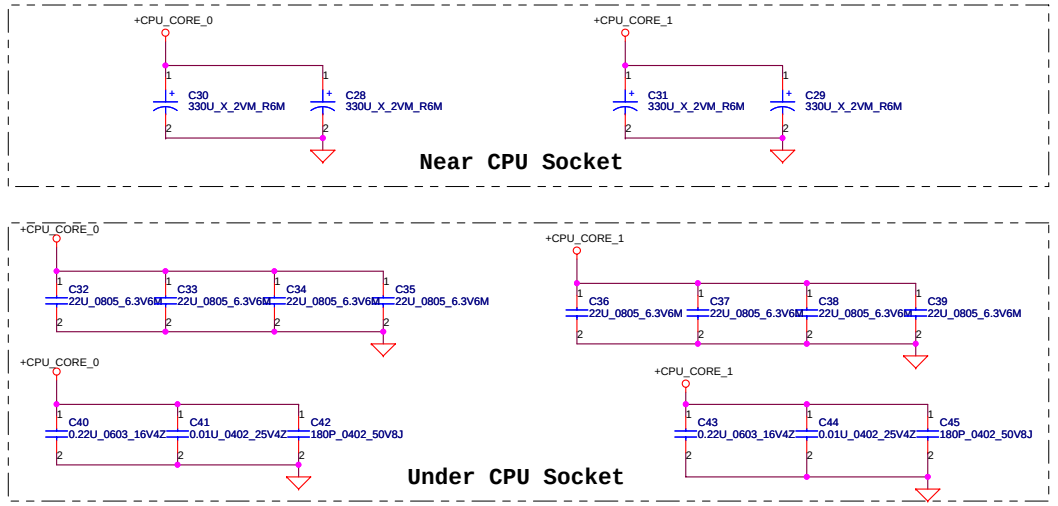
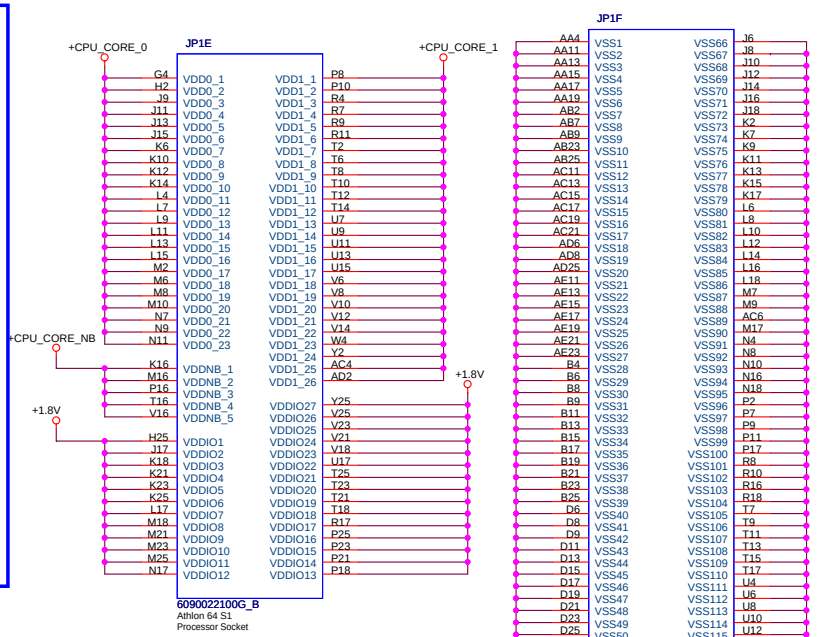
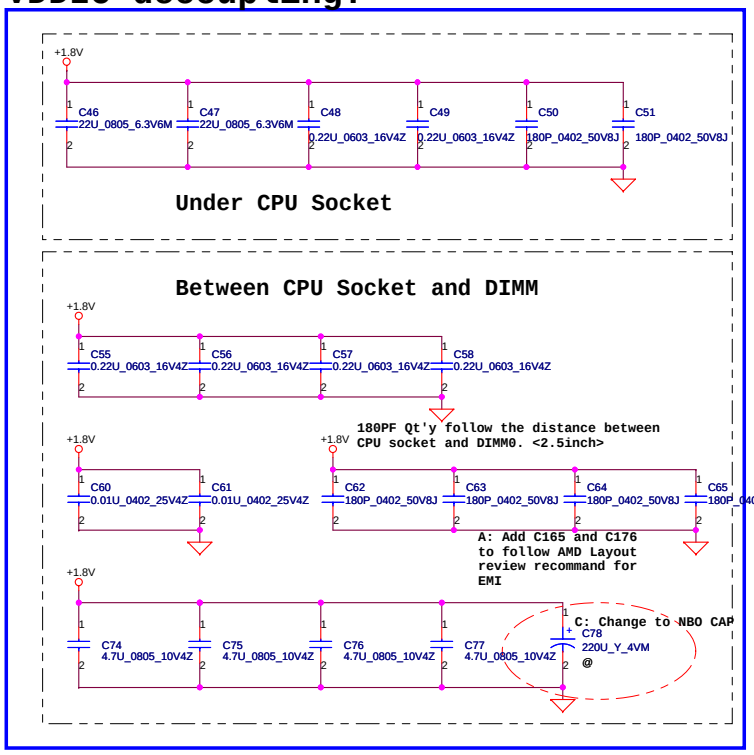
VDD(+CPU_CORE) decoupling.

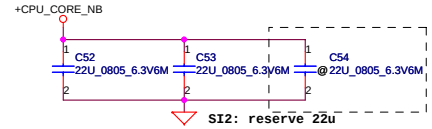




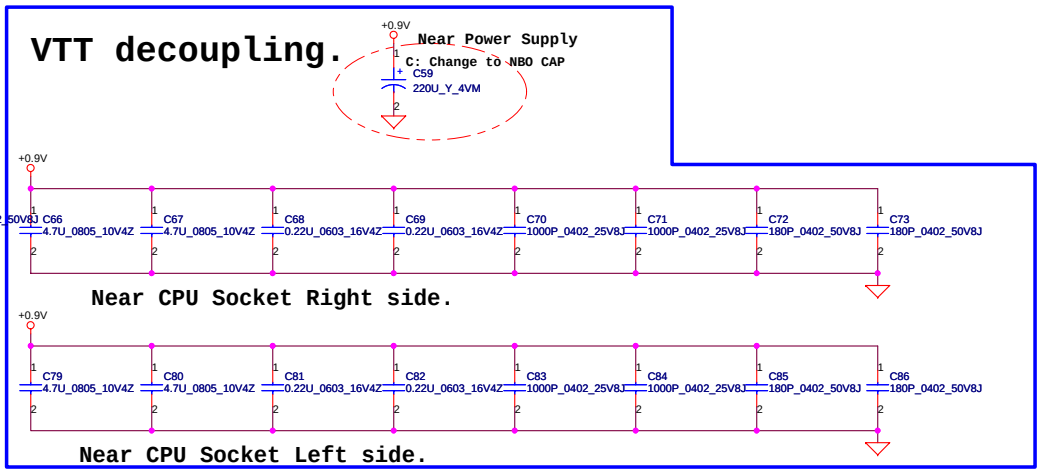
VDDIO decoupling.



+CPU_CORE_NB decoupling.



VTT decoupling.



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Title: AMD CPU S1G2 PWR & GND

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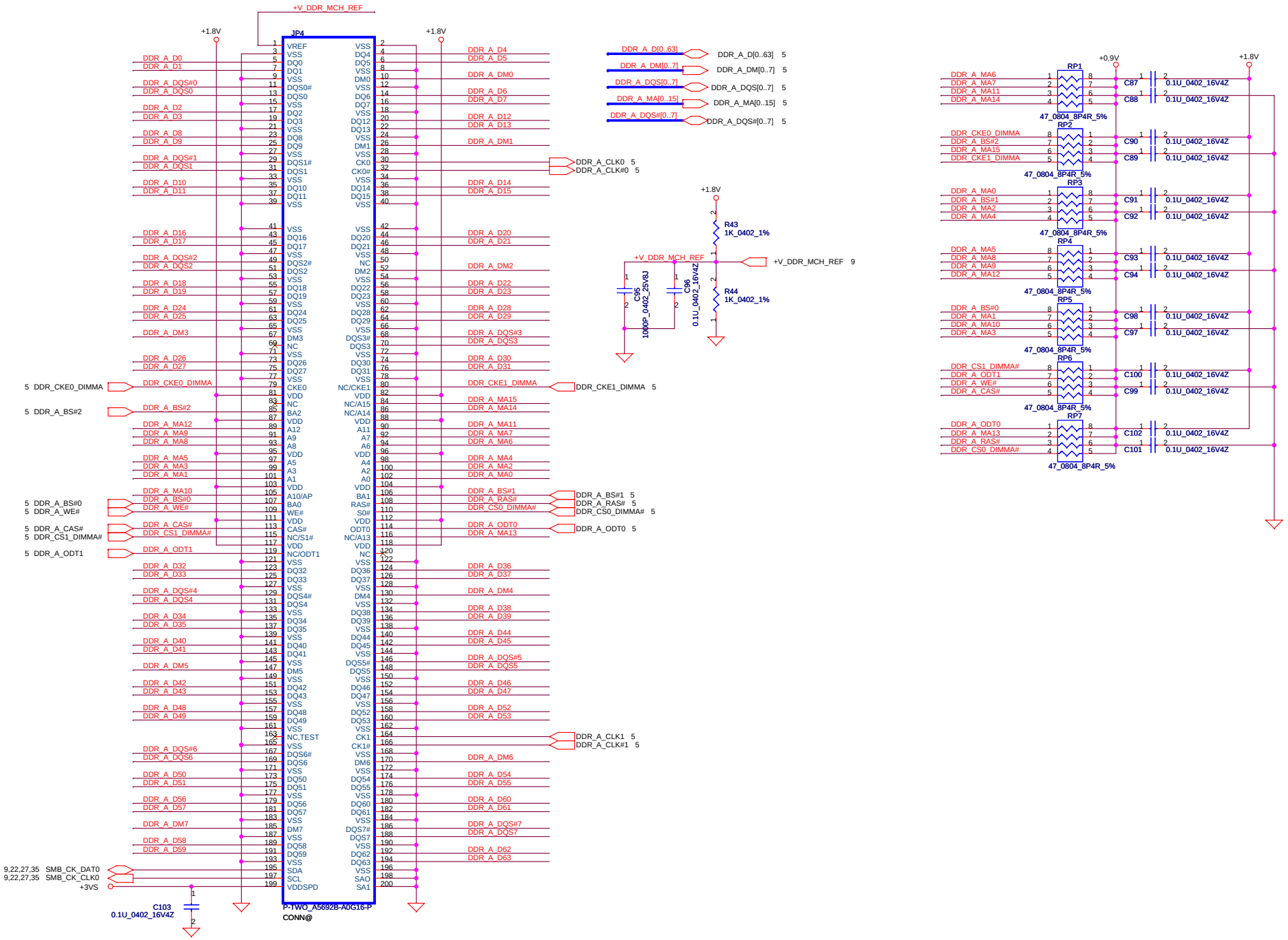

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Title: **DDRII SO-DIMM 0**

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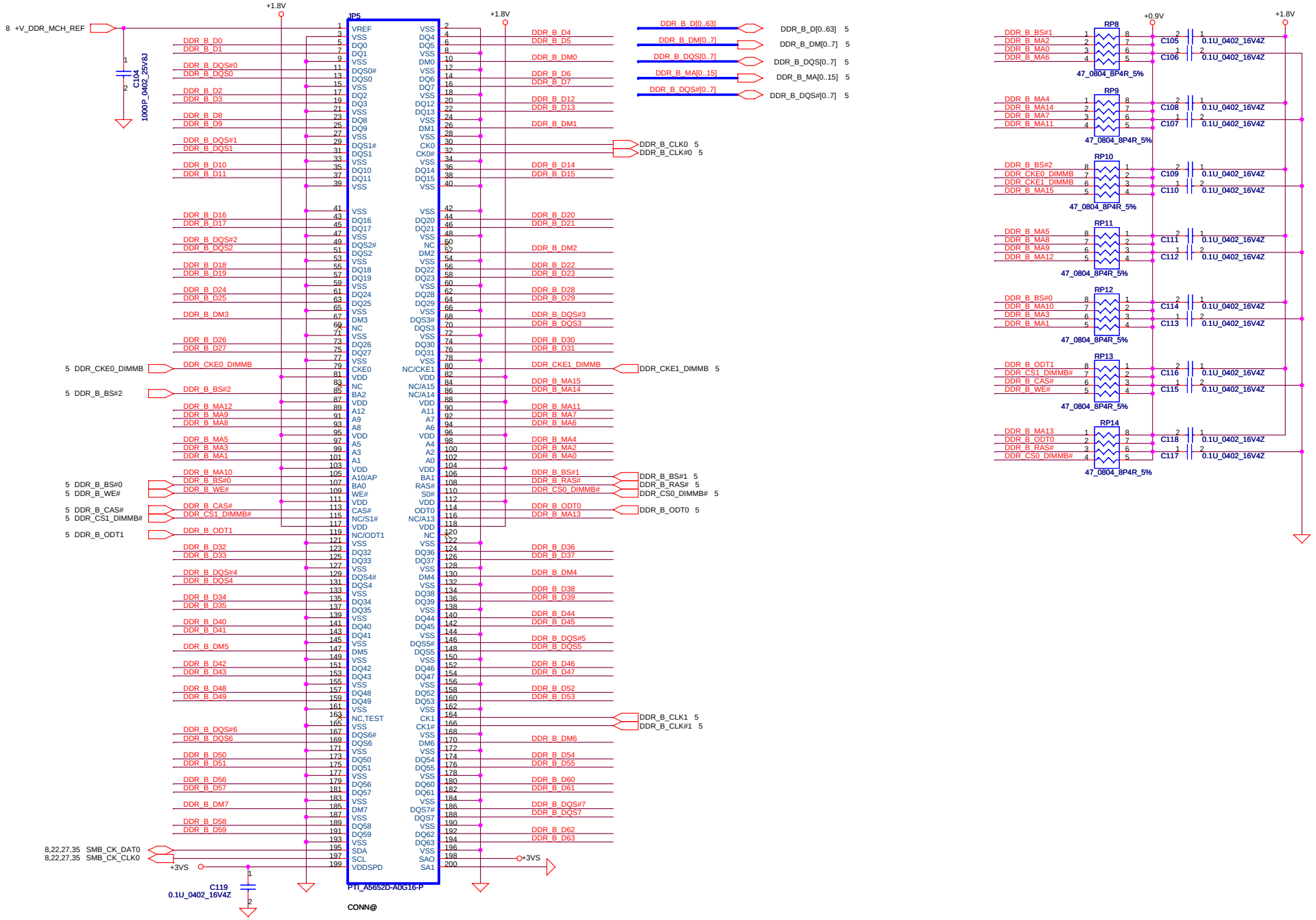

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Title: **DDRII SO-DIMM 1**

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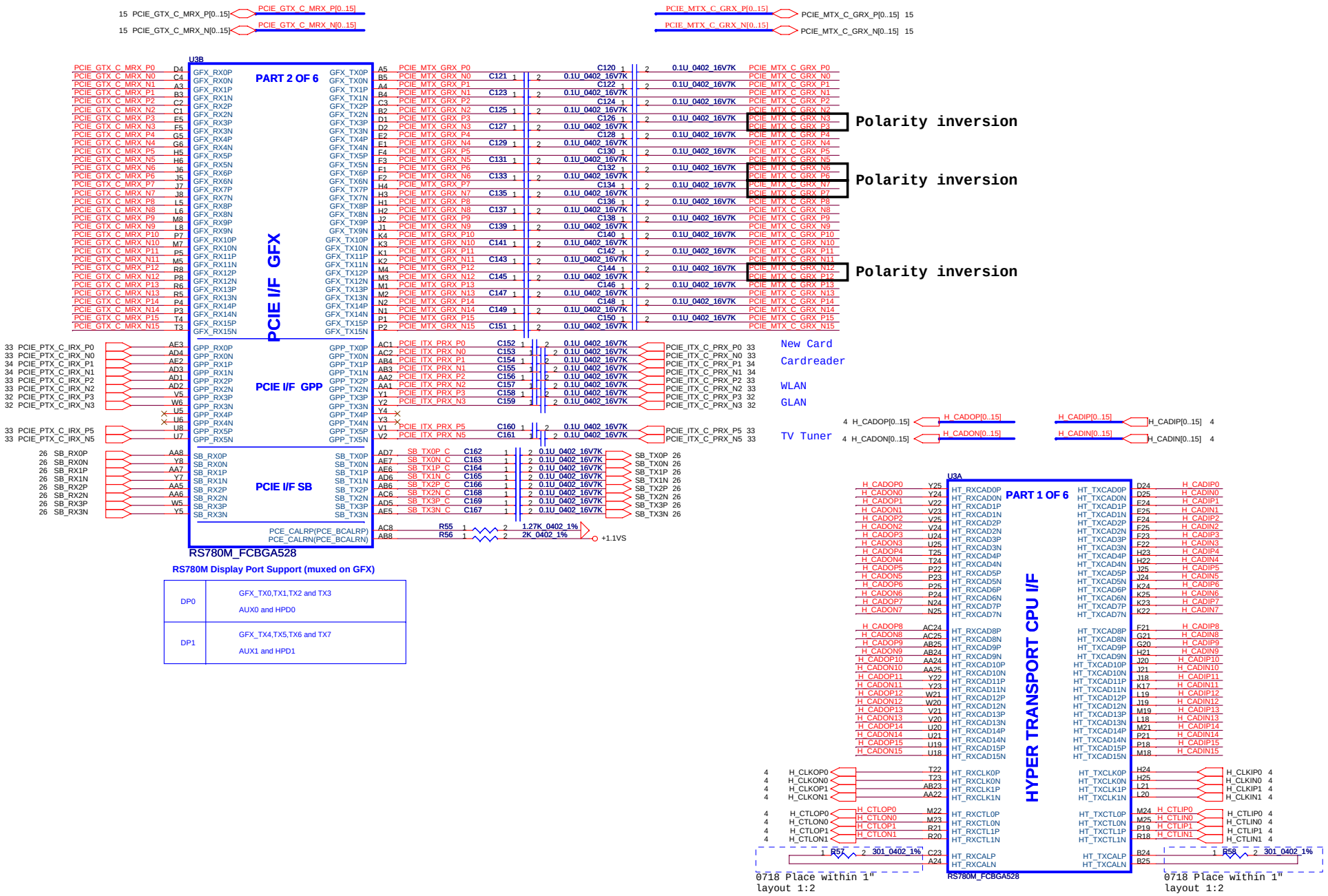

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

NEED CHECK R68 & R69 WITH AMD

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Title	RS780-HT/PCIE
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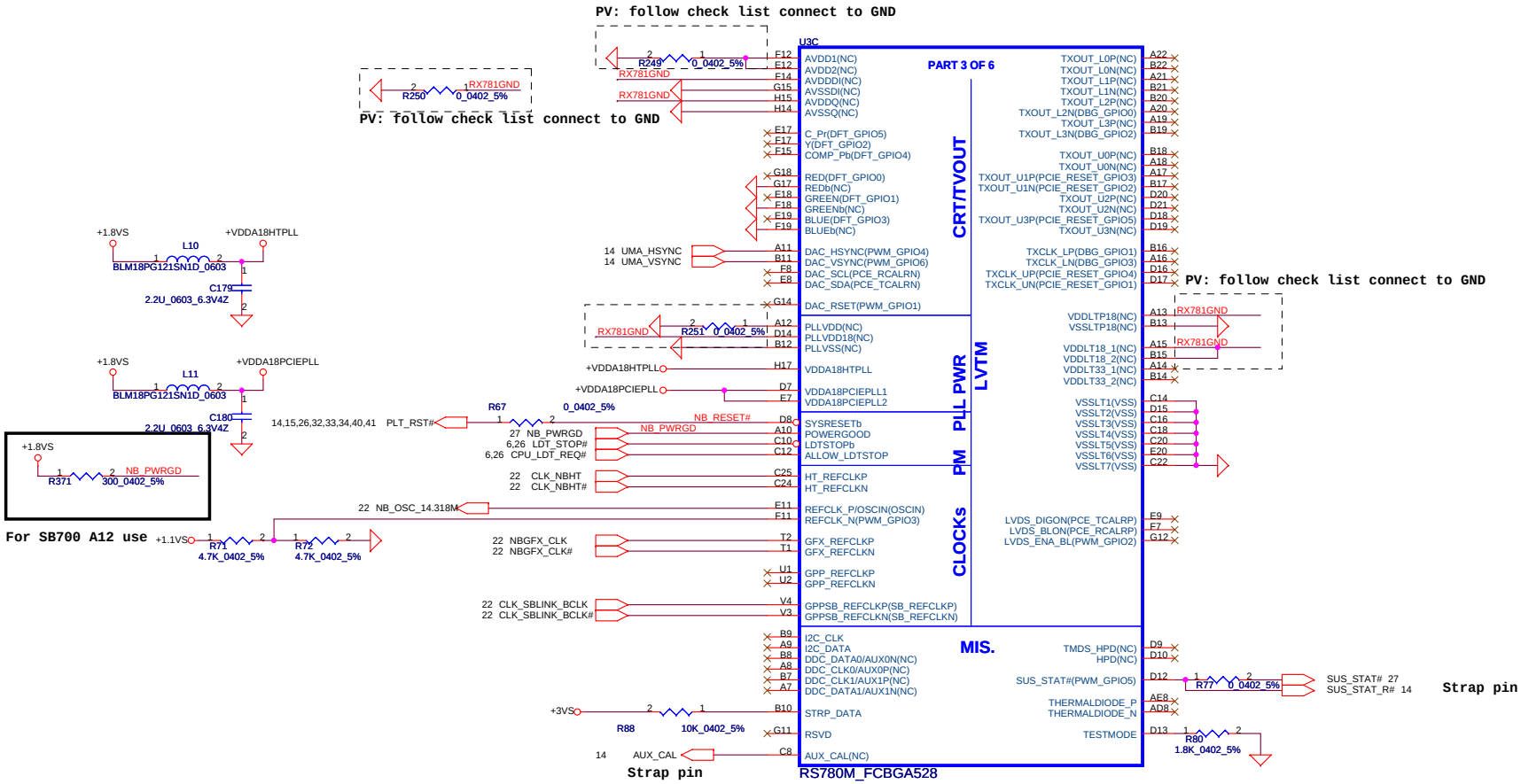

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Title: RS780 VEDIO/CLK GEN

Size	Document Number	Rev
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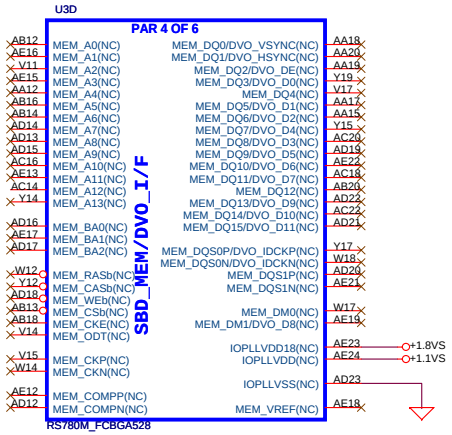

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Compal Electronics, Inc.

Title: **RS780 SIDE PORT**

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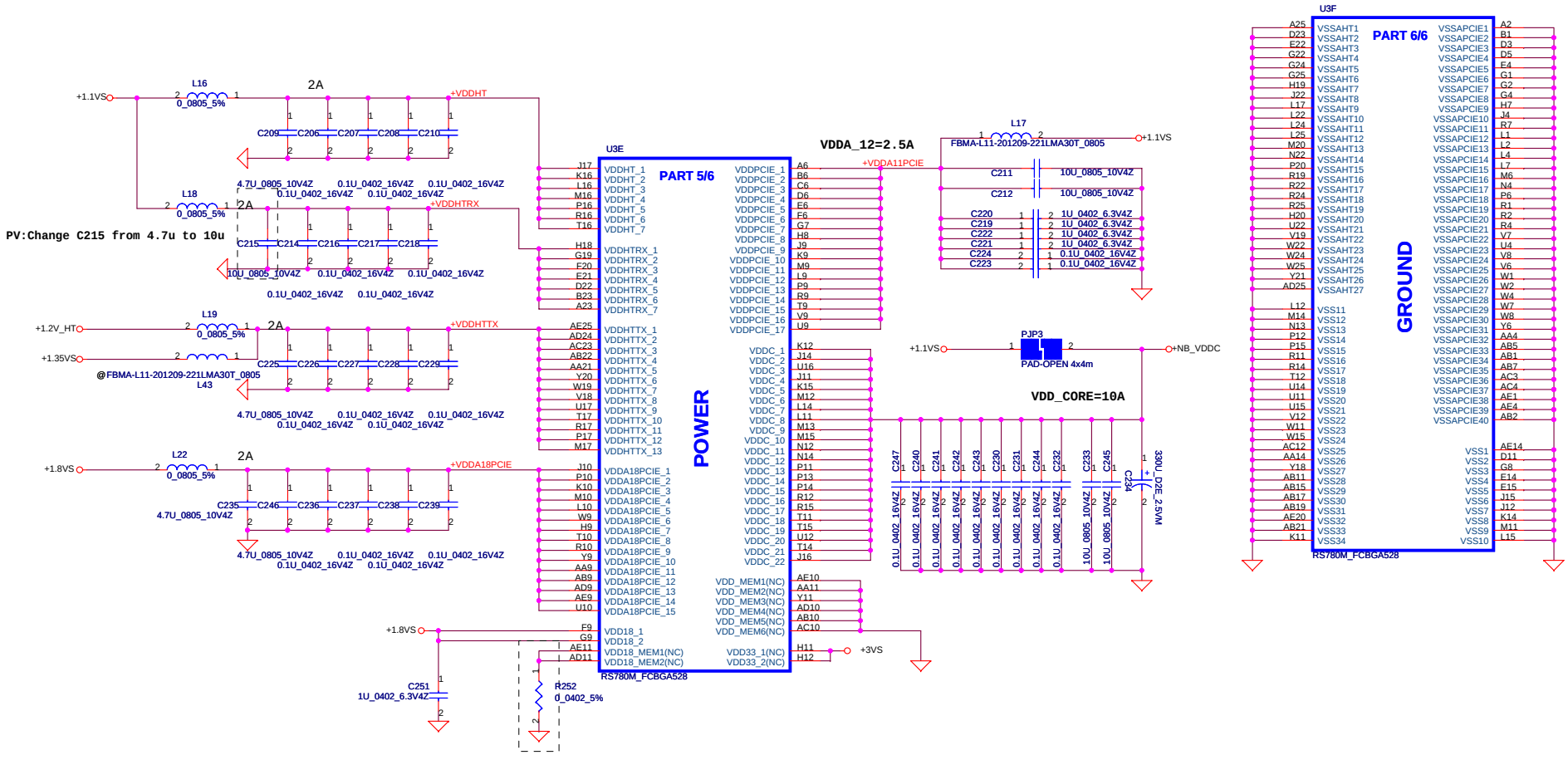

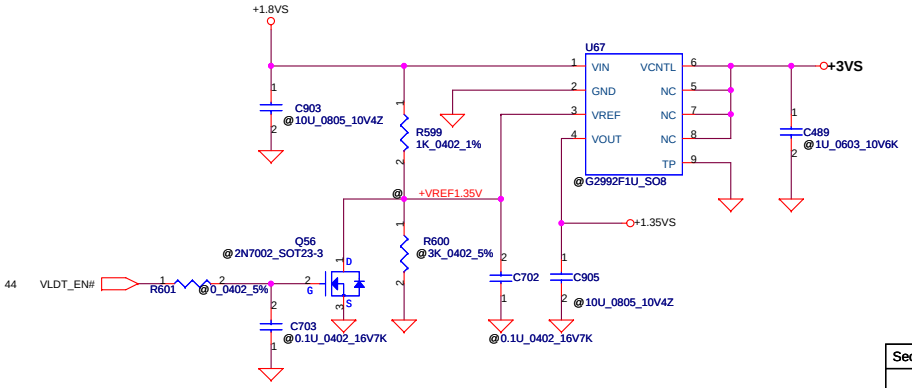

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Compal Electronics, Inc.

Title: **RS780 PWR/GND**

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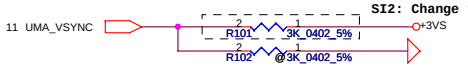
RS780 DFT_GPIO5 mux at CRT_VSYNC pull high to 3K

SI2: Change to 3K pull high



DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

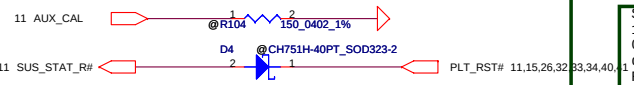
```
Enables the Test Debug Bus using GPIO.
1 : Enable (RX780, RS780)
0 : Disable (RX780, RS780)
PIN: RS740-->RS780_AUX_CAL; RX780-->NB_TV_C; RS780--> VSYNC#
```

RS780 use register to control PCI-E configure

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

```
These pin straps are used to configure PCI-E GPP mode.
000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011
```

RS780 DFT_GPIO1

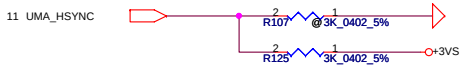


RX780 DFT_GPIO1 mux at GREEN(Ball E18) and change pull low form 150 to 3K.

DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740/RX780: DFT_GPIO1  RS780:SUS_STAT
```

RS780 use HSYNC to enable SIDE PORT (internal pull high)



DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

```
RX780: Enables the Test Debug Bus using PCIE bus
1 : Disable ( Can still be enabled using nbcfg register access )
0 : Enable

RS780: Enables Side port memory ( RS780 use HSYNC#)
1.  Disable (RS780)
0 : Enable (RS780)
```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Title: **RS780 STRAPS**

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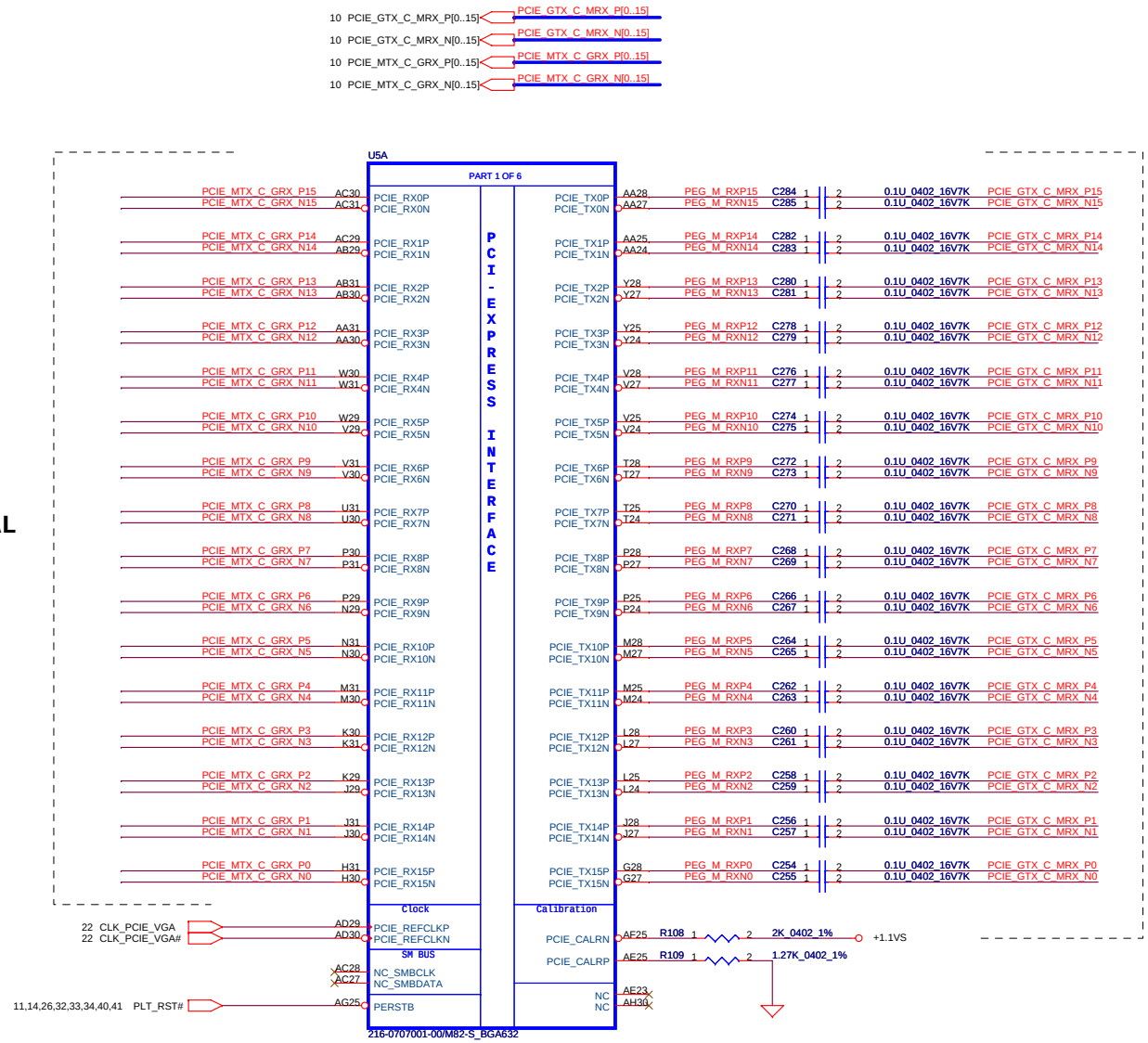
PCIE LANE REVERSAL

PCIE LANE REVERSAL



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Title: M82-S PCIE interface

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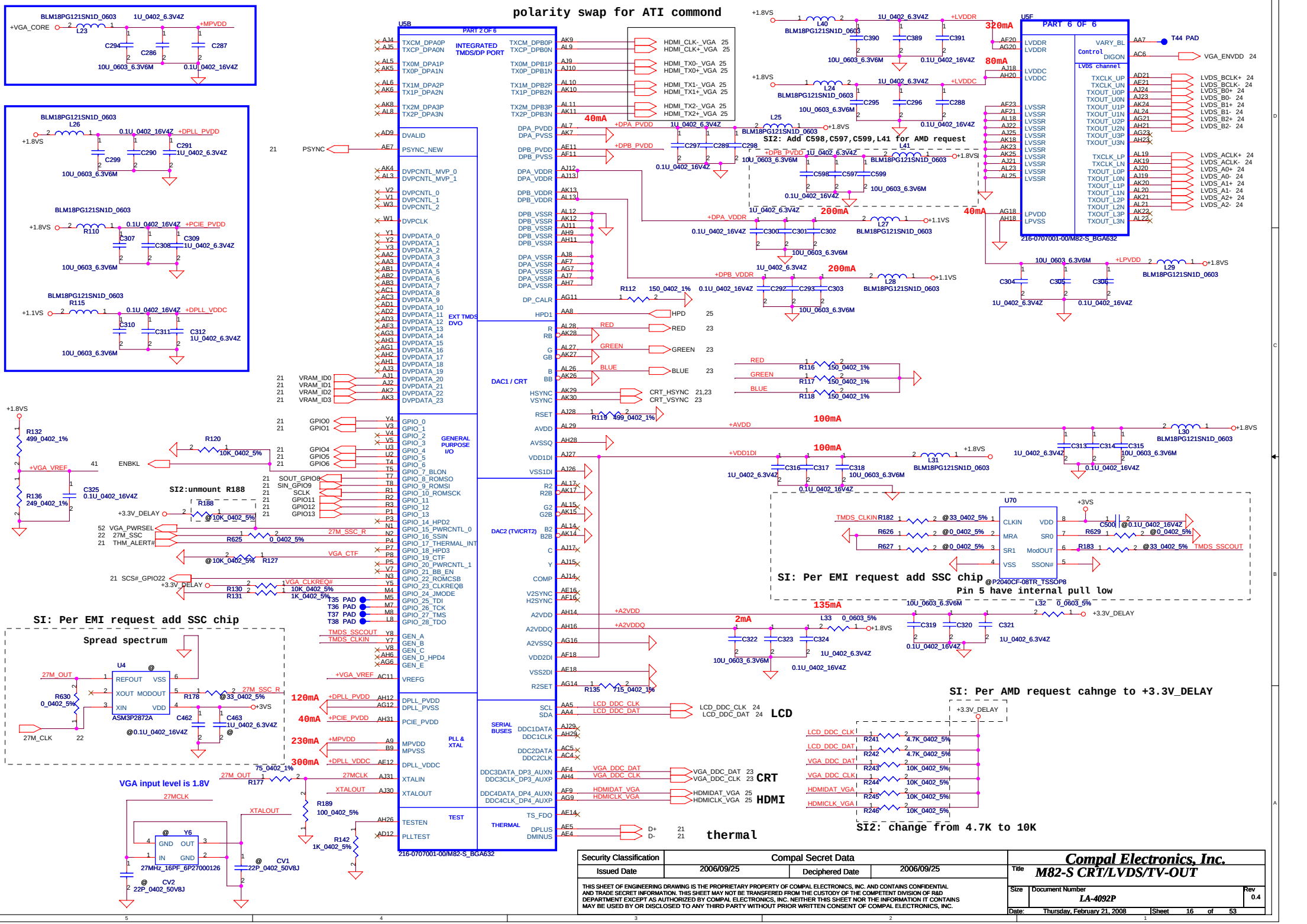
polarity swap for ATI commond



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Title: **M82-S CRT/LVDS/TV-OUT**

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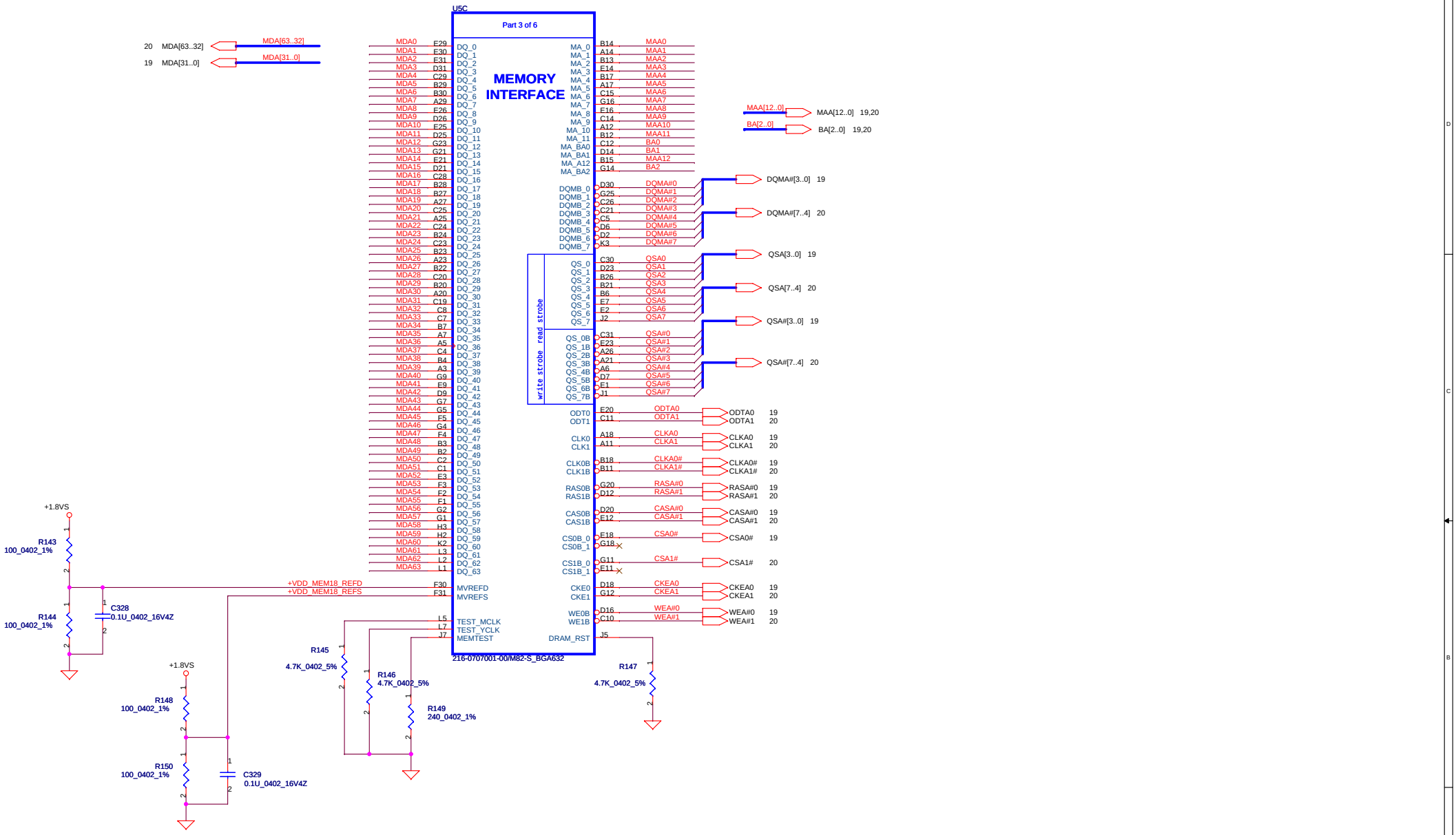

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Title: **M82-S MEM**

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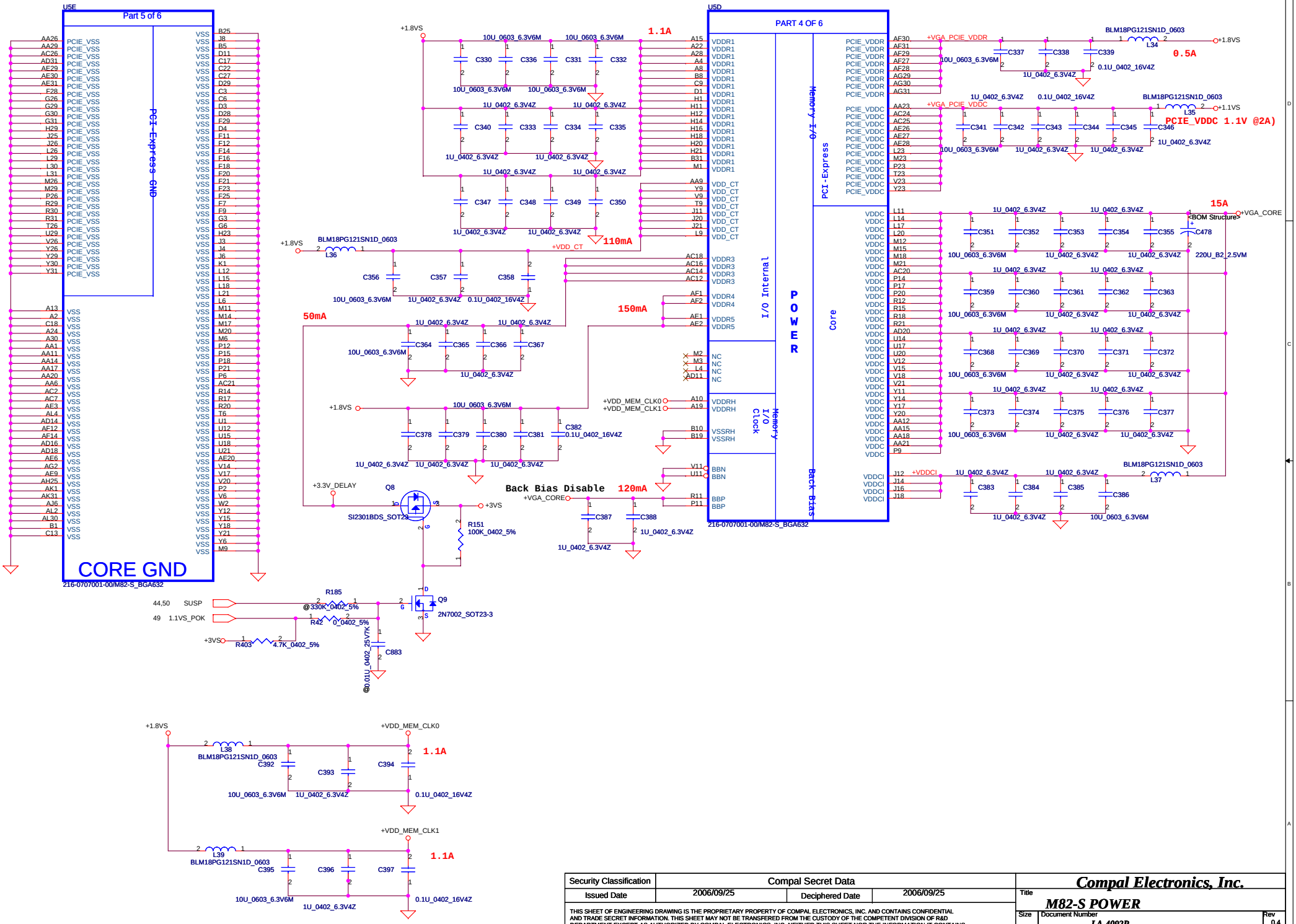
U5E
Part 5 of 6
PCI_VSS
PCI Express GND
VSS
CORE GND
216-0707001-00/M82-S_BGA632
U5D
PART 4 OF 6
VDDR1
VDDR3
VDDR4
VDDR5
VDDRH
VSSRH
BBN
BBP
VDD_CT
NC
I/O Internal
Memory I/O
PCI-Express
Clock I/O
Memory
Core
Back Bias
POWER
PCIE_VDDR
VDDC
VDDCI
+1.8VS
+VDD_CT
+VGA_CORE
+VDD_MEM_CLK0
+VDD_MEM_CLK1
+3.3V_DELAY
+3VS
+VGA_PCIE_VDDR
+VGA_PCIE_VDDC
+VDDCI
1.1A
110mA
50mA
150mA
15A
0.5A
Back Bias Disable
120mA
PCIE_VDDC 1.1V @2A)
BLM18PG121SN1D_0603
BLM18PG121SN1_0603
SI2301BDS_SOT23
2N7002_SOT23-3
R151 100K_0402_5%
R185 @330K_0402_5%
R42 0_0402_5%
R403 4.7K_0402_5%
C883 @0.01U_0402_25V7K
44,50 SUSP
49 1.1VS_POK
<BOM Structure>
220U_B2_2.5VM
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M82-S POWER
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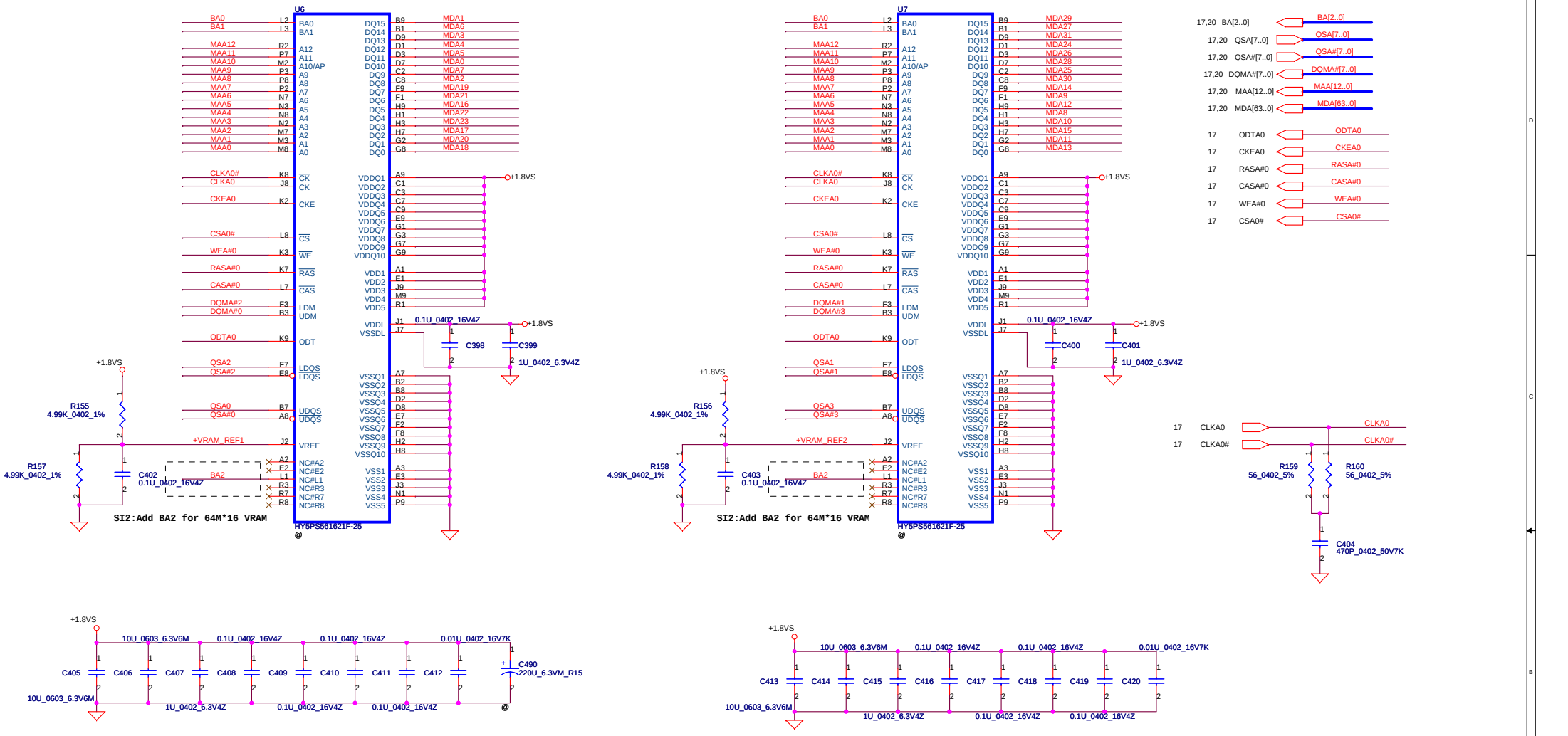

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Title: **M82-S VRAM**

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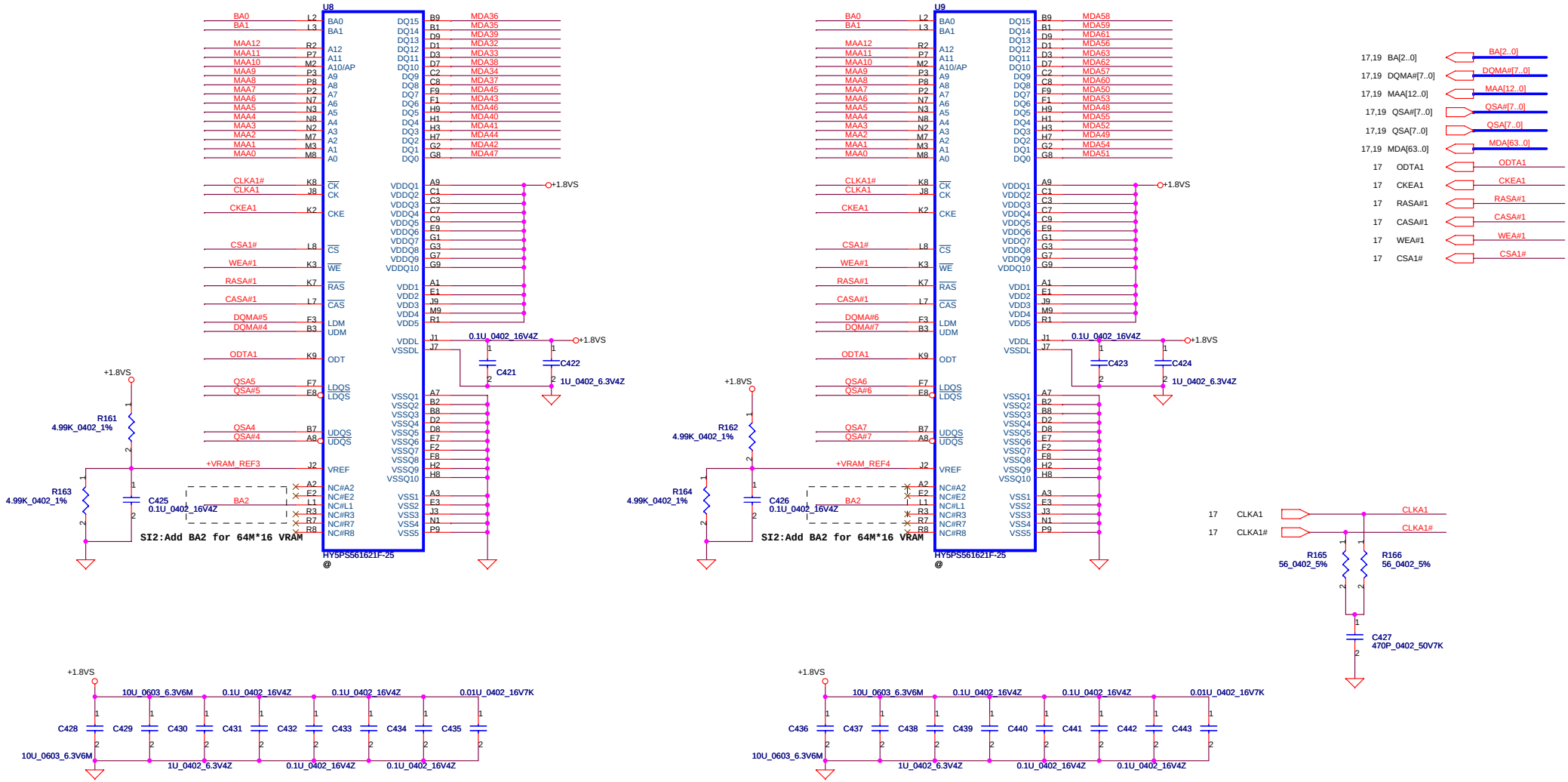

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Title: **M82-S VRAM**

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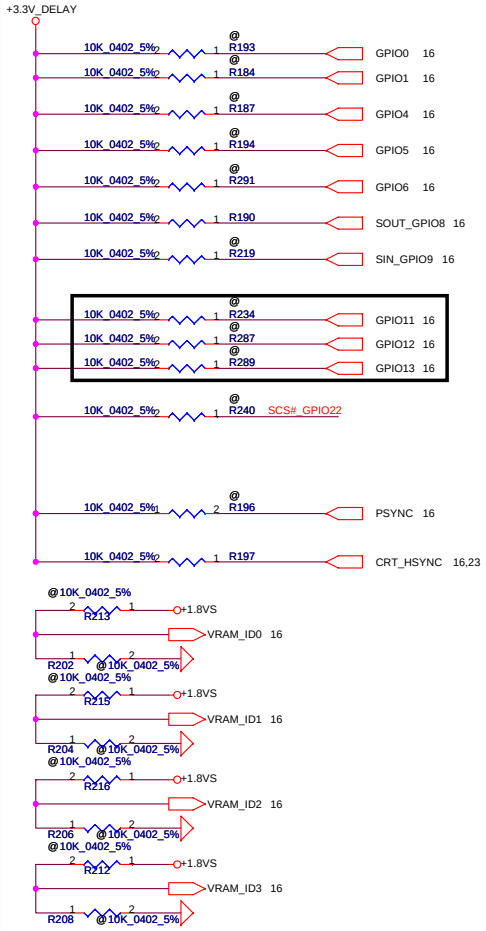


GPIO9 = 0 (BIOS_ROM_EN = 0)	
GPIO[13:11]	**MEMORY SIZE**
0 0 0	128MB
0 0 1	256MB
0 1 0	64MB
1 0 0	512MB

STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED M8X
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLES	0
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0
BIF_GEN2_EN_A	GPIO5	PCI-E 5.0GT/s or 2.5 GT/s select	0
DEBUG_ I2C_ENABLE	GPIO6	Internal use only	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO(M8X)	1
ROMIDCFG[3:0]	GPIO [9,13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 1 0 1
BIOS_ROM EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	0
BIF_VGA_DIS	PSYNC	VGA ENABLED===0 is enable	0
BIF_HDMI_EN	HSYNC	HDMI ENABLE	1
VRAM_ID[3:0]	DVPDATA (23,22,21,20)		VRAM_ID 3 ,2 ,1 ,0
		Samsung 64Mx16 1.8V	0 0 0 0
		Samsung 32Mx16 1.8V	0 0 0 1
		Hynix 64Mx16 1.8V	0 0 1 0
		Hynix 32Mx16 1.8V	0 0 1 1
		Qimonda 32Mx16 1.8V	0 1 0 0
		Qimonda 64Mx16 1.8V	0 1 0 1

ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESE

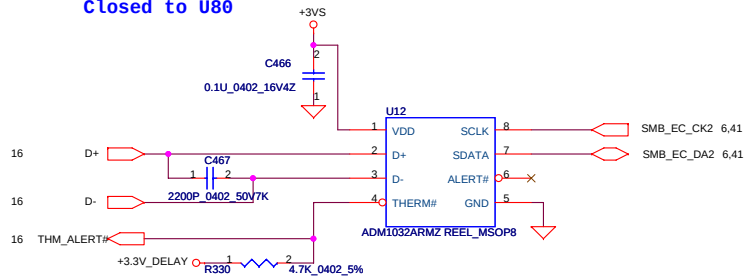
GPIO2 GPIO3 GPIO5 GPIO6 DVALID H2SYNC V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

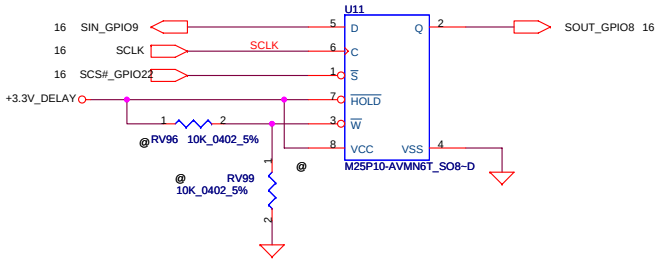
GENERICC GPIO21_BB_EN GPIO_28_TDO

VGA Thermal Sensor ADM1032ARMZ

Closed to U80



FLASH ROM



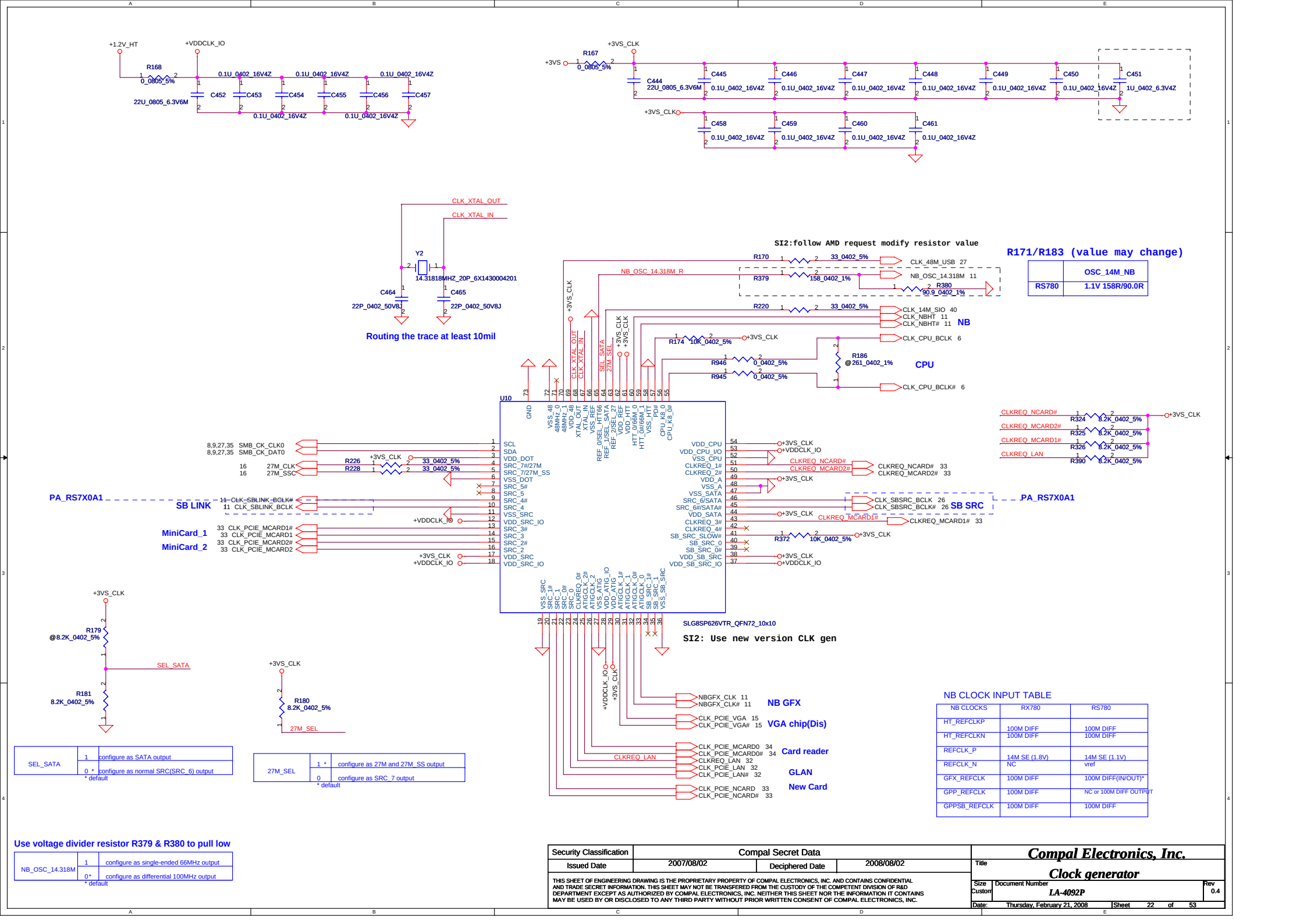
Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.

Title: **M82-S Filters / Strap**

Size	Document Number	Rev
	LA-4092P	0.3

Date: Thursday, February 21, 2008 Sheet 21 of 53



SEL_SATA		
	1	configure as SATA output
	0 *	configure as normal SRC(SRC_6) output

* default

27M_SEL		
	1 *	configure as 27M and 27M_SS output
	0	configure as SRC_7 output

* default

Use voltage divider resistor R379 & R380 to pull low

NB_OSC_14.318M		
	1	configure as single-ended 66MHz output
	0 *	configure as differential 100MHz output

* default

NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

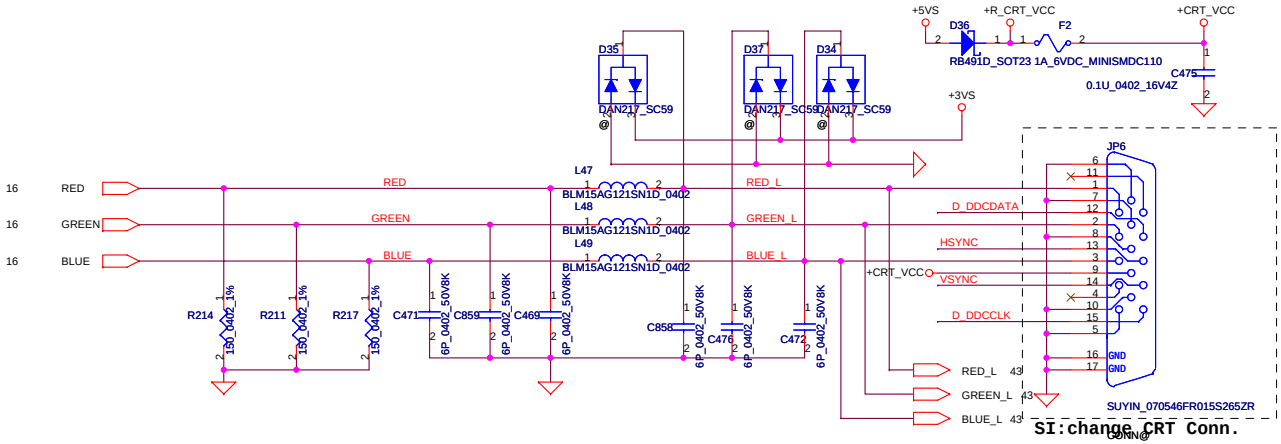
Compal Electronics, Inc.

Title: **Clock generator**

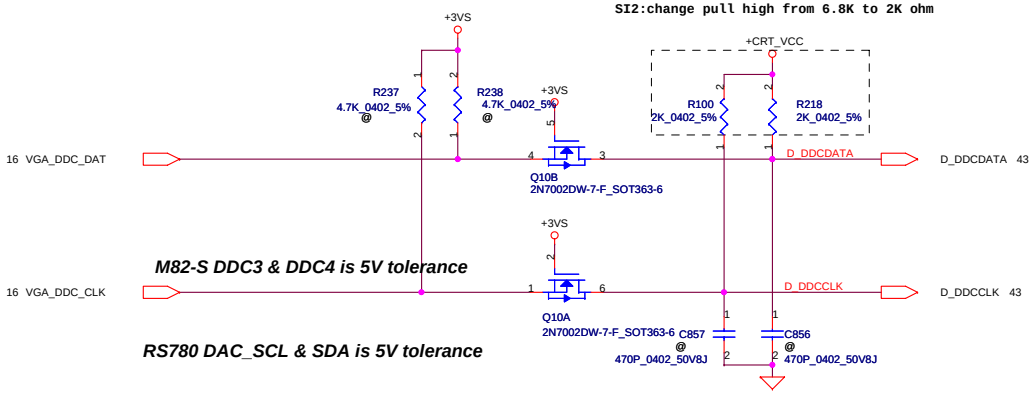
Size	Document Number	Rev
Custom	LA-4092P	0.4

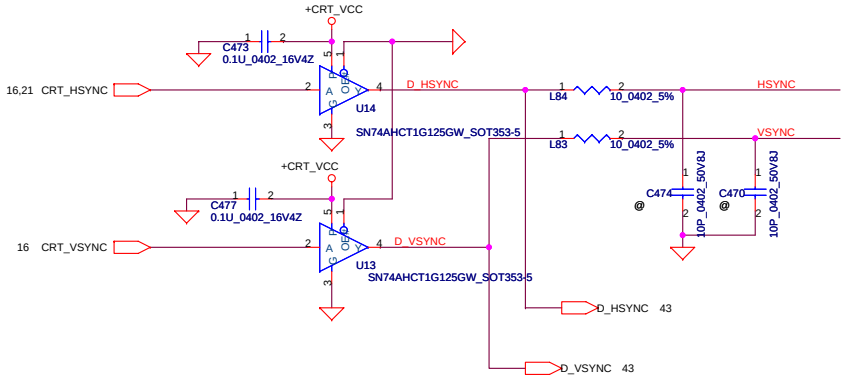
Date: Thursday, February 21, 2008 | Sheet 22 of 53

CRT CONNECTOR



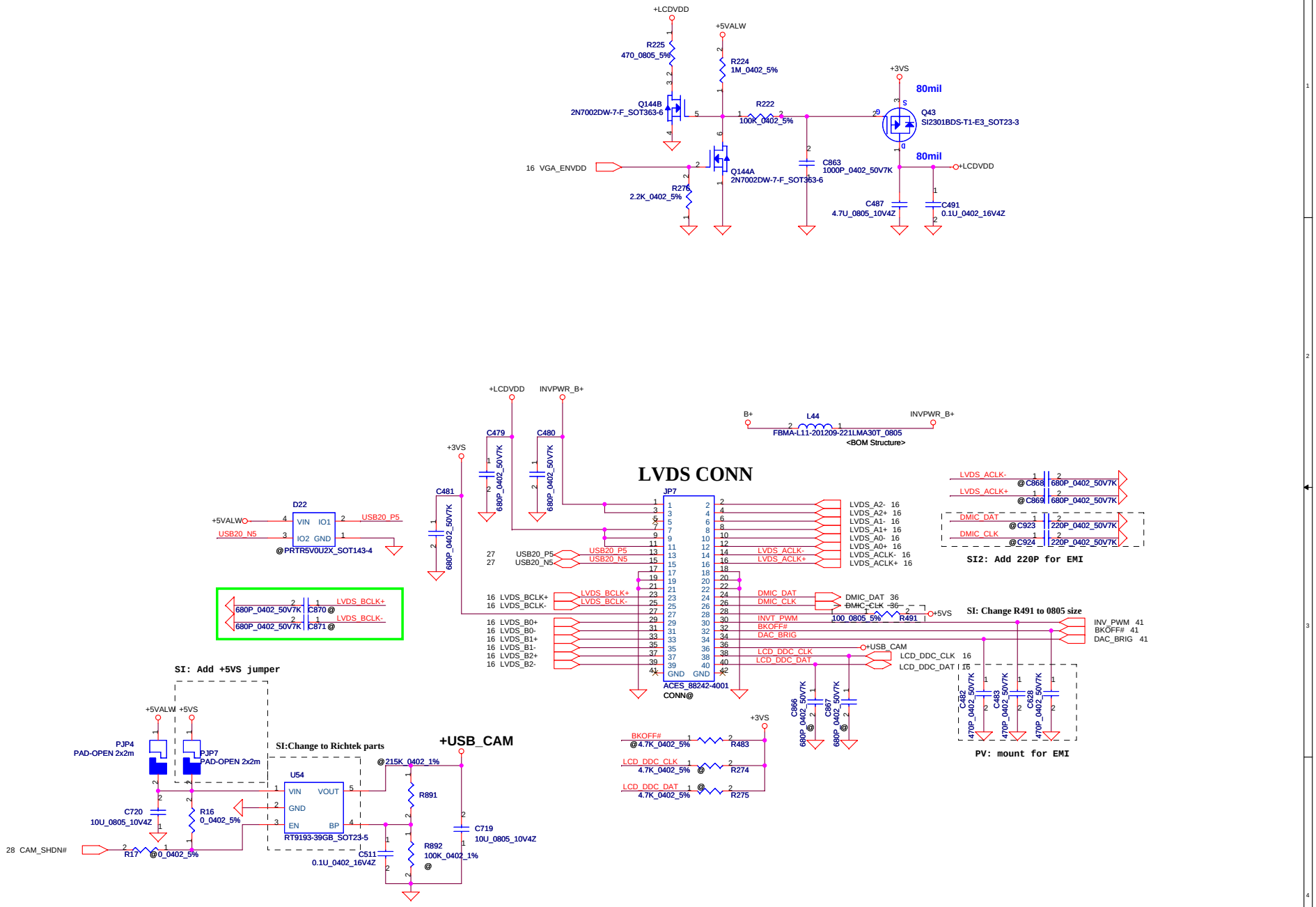
SI2:change pull high from 6.8K to 2K ohm





Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.			
Title: CRT Connector			
Size: Custom	Document Number: LA-4092P		Rev: 0.4
Date: Thursday, February 21, 2008	Sheet 23 of 53		

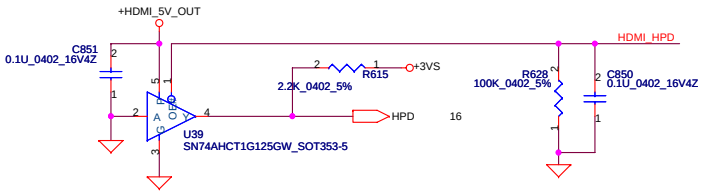


Compal Electronics, Inc.

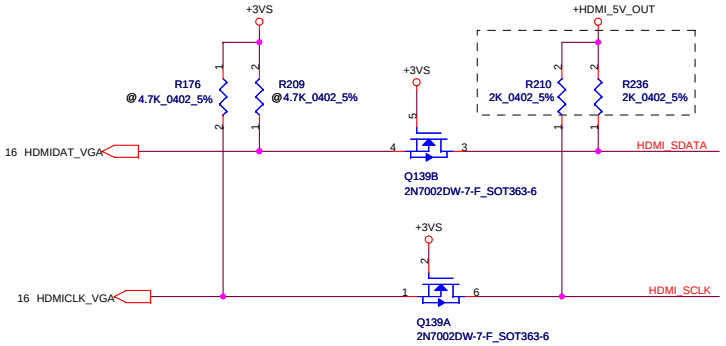
Title: **LCD CONN.**

Size	Document Number	Rev
Custom	LA-4092P	0.4

Date: Thursday, February 21, 2008 | Sheet 24 of 53

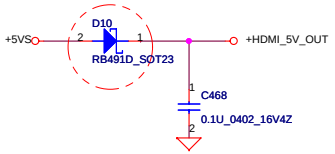


SI2:change pull high from 6.8K to 2K ohm

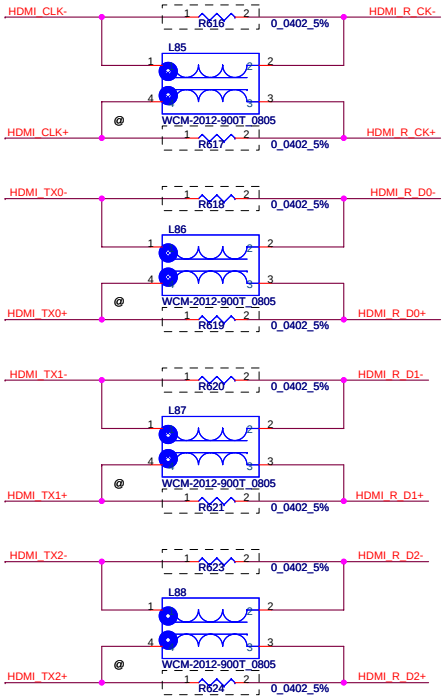


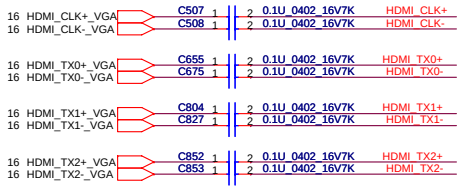
C:Chg. PN to SB770020010.

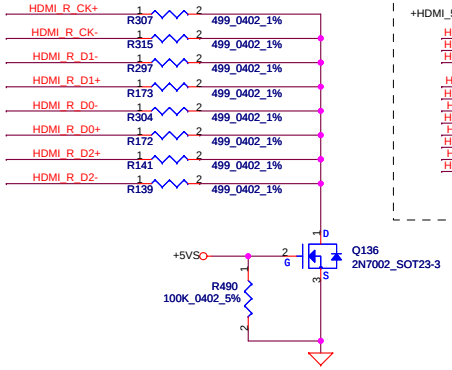
MP:Update D10 to meet HDMI.



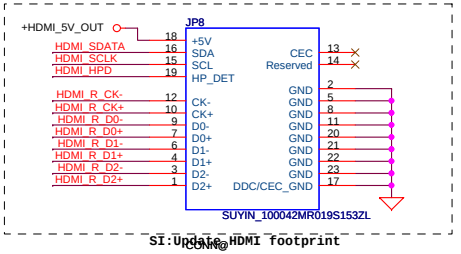
SI:Add R6161~R624 for EMI requset







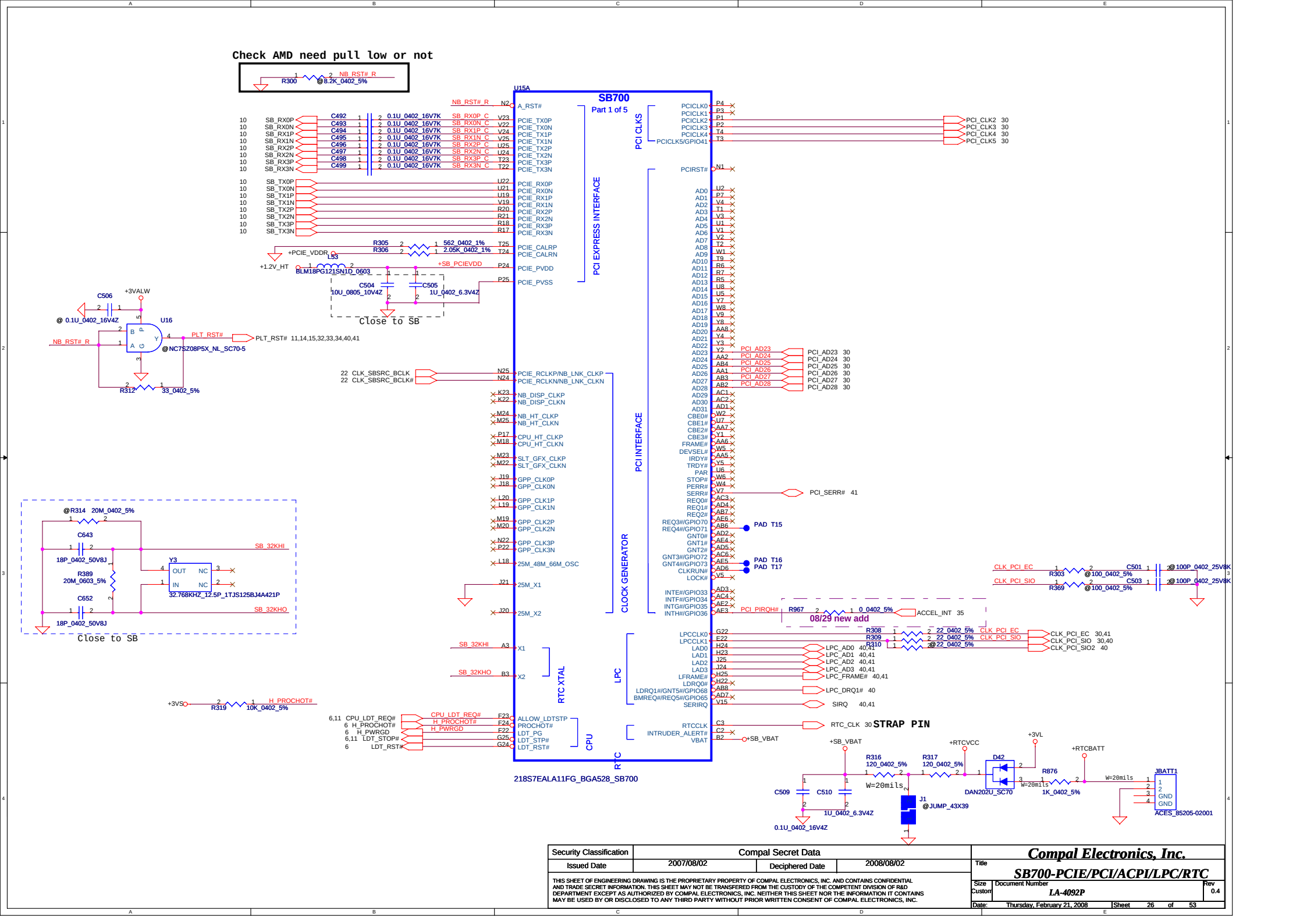
HDMI Connector



SI:Update HDMI footprint

Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.			
Title: HDMI			
Size: Custom	Document Number: LA-4092P		Rev: 0.4
Date: Thursday, February 21, 2008	Sheet 25 of 53		



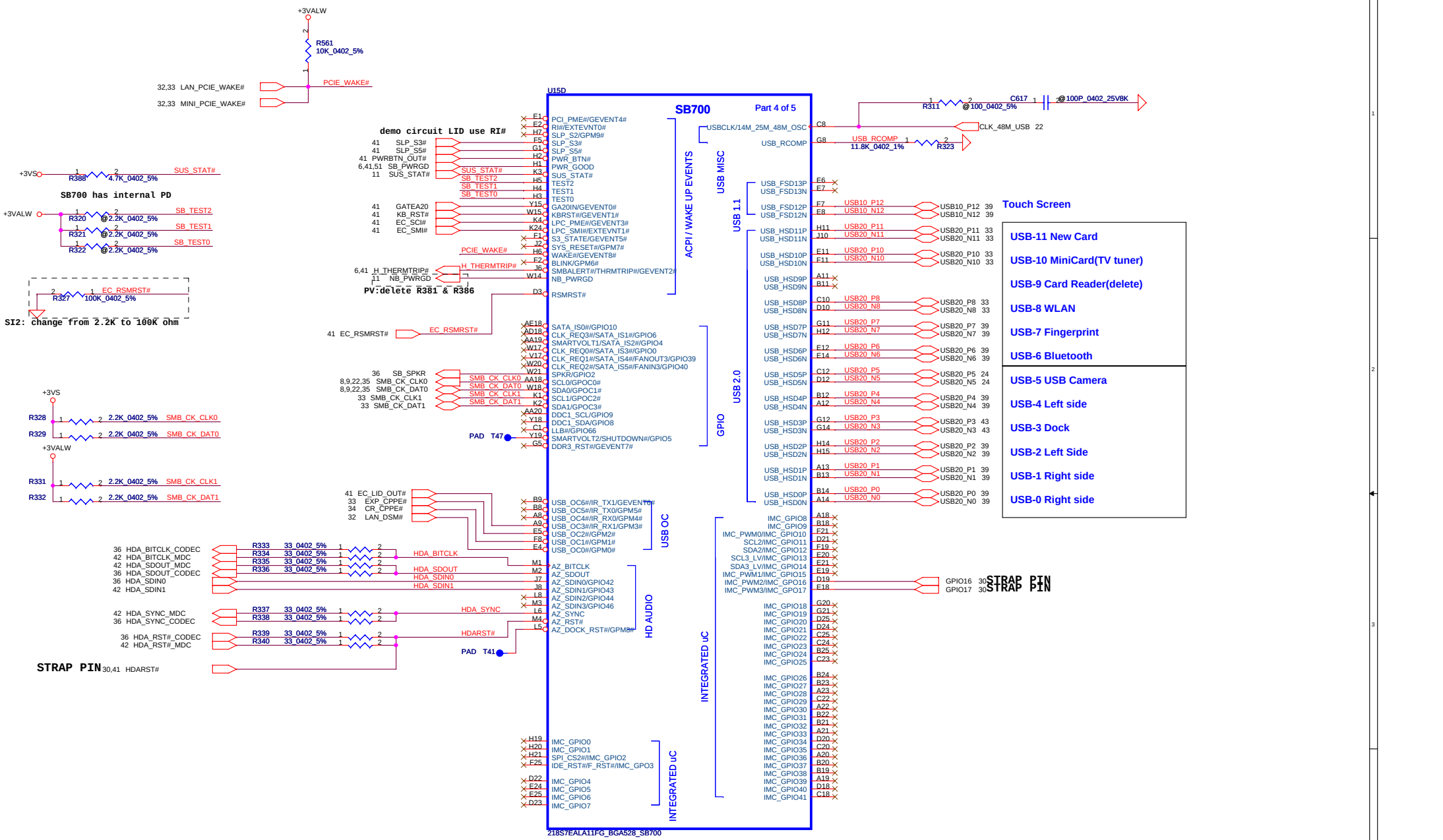
Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.

Title: **SB700-PCIE/PCI/ACPI/LPC/RTC**

Size	Document Number	Rev
Custom	LA-4092P	0.4

Date: Thursday, February 21, 2008 | Sheet 26 of 53



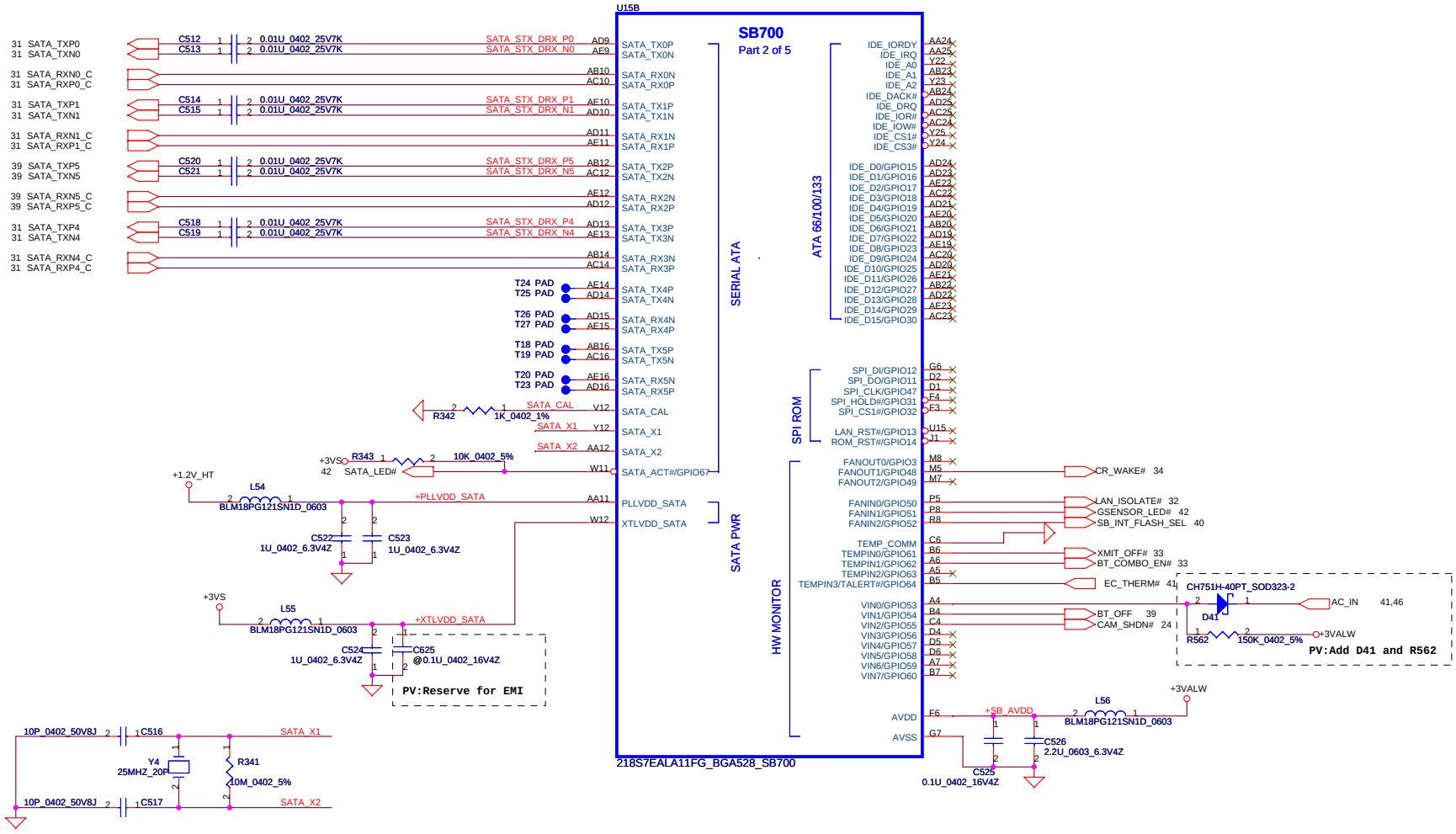
Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.

Title: **SB700 USB/AC97**

Size	Document Number	Rev
Custom	LA-4092P	0.4

Date: Thursday, February 21, 2008 Sheet 27 of 53



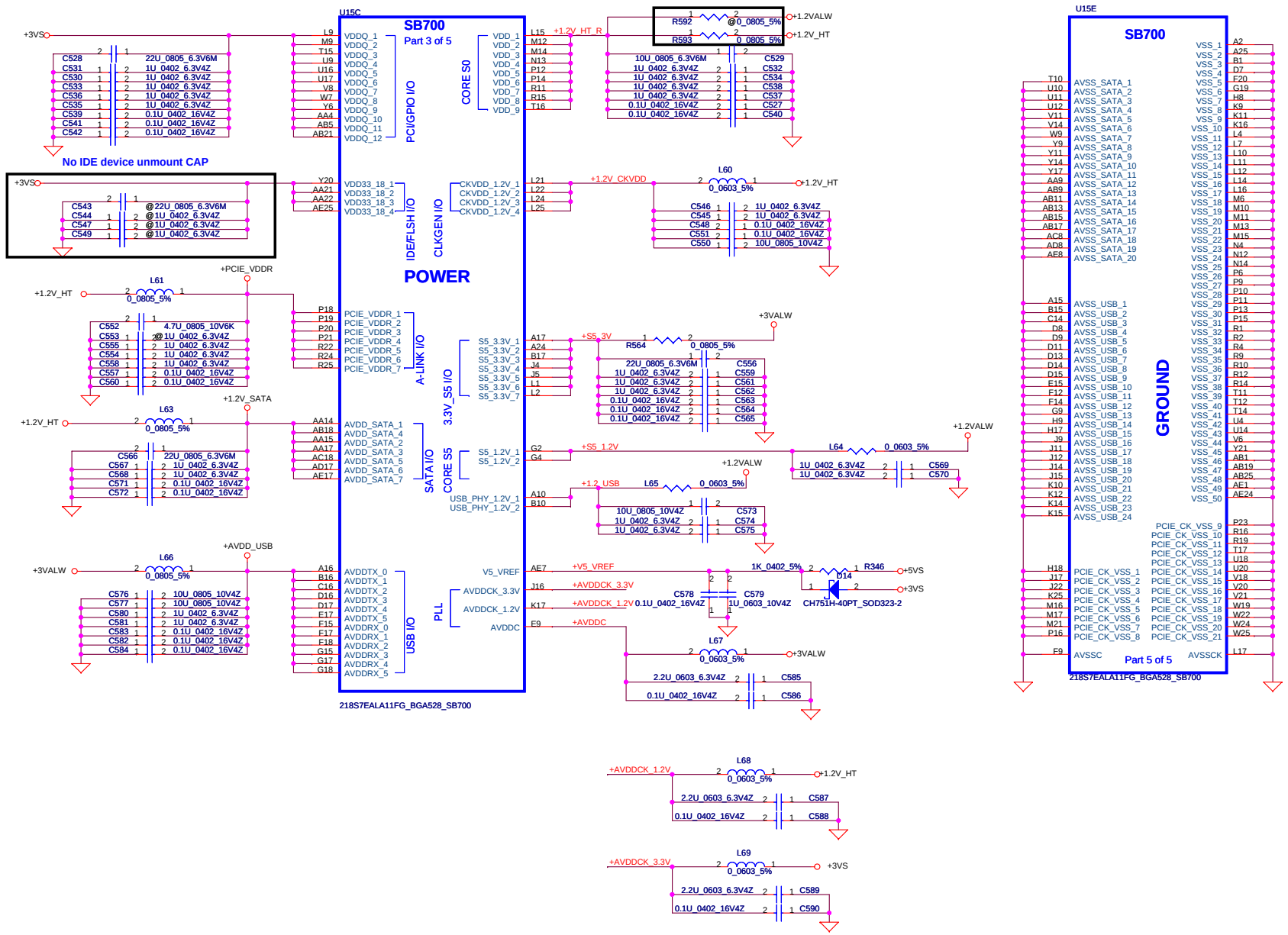
Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.

Title: **SB700 SATA/IDE/SPI**

Size	Document Number	Rev
Custom	LA-4092P	0.4

Date: Thursday, February 21, 2008 | Sheet 28 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.

Title: **Cover Sheet**

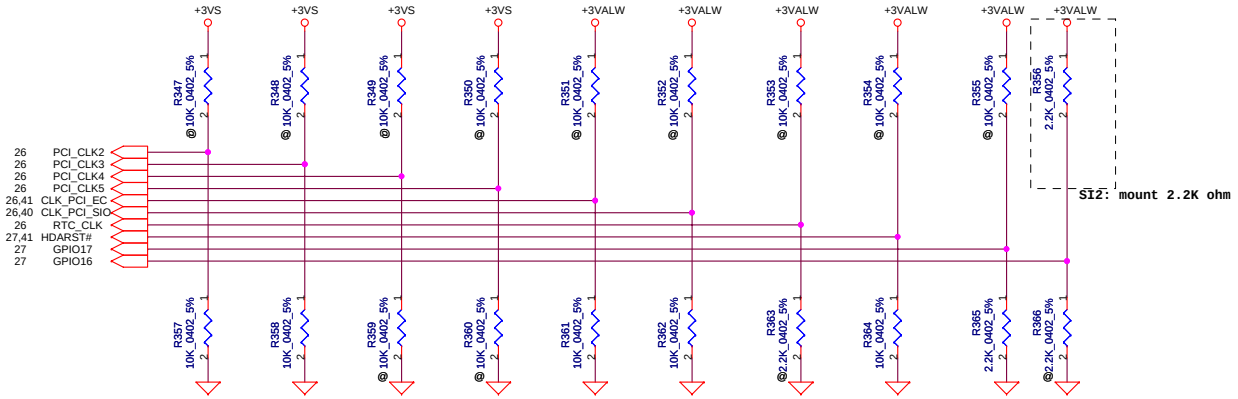
Size	Document Number	Rev
Custom	LA-4092P	0.4

Date: Thursday, February 21, 2008 | Sheet 29 of 53

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

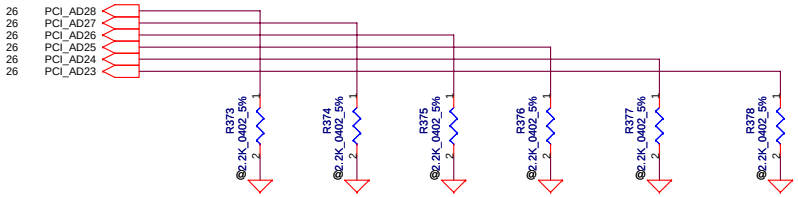
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM L,H = LPC ROM (Default) L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	



DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

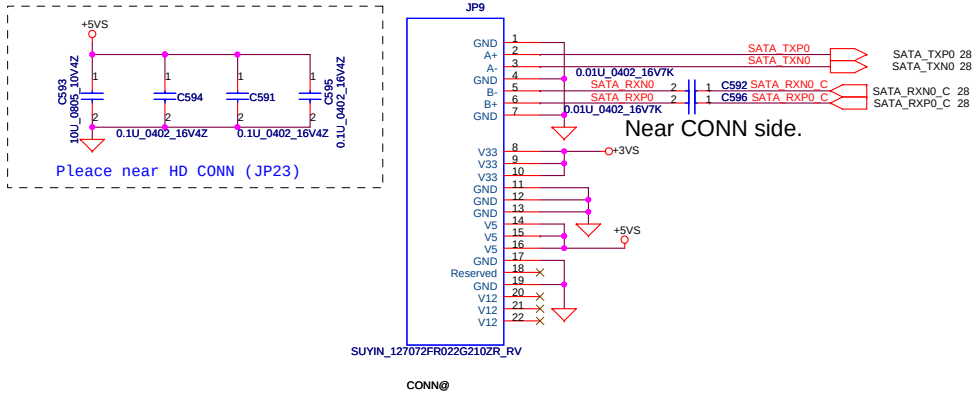
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



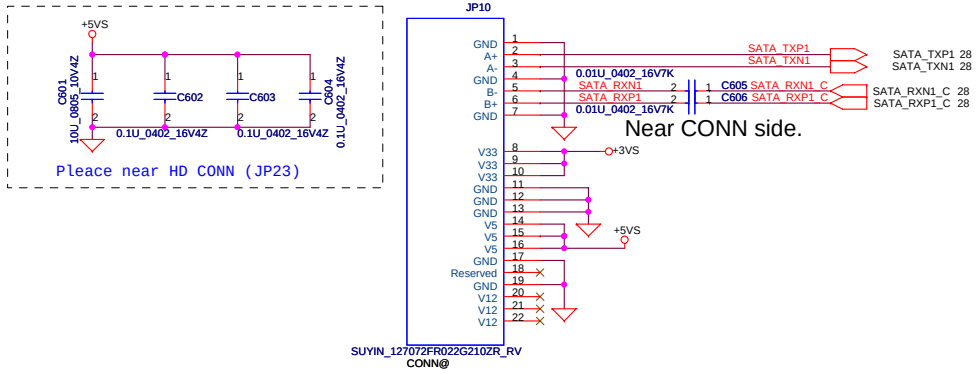
Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.			
Title: SB700 STRAPS			
Size: Custom	Document Number: LA-4092P		Rev: 0.4
Date: Thursday, February 21, 2008		Sheet 30 of 53	

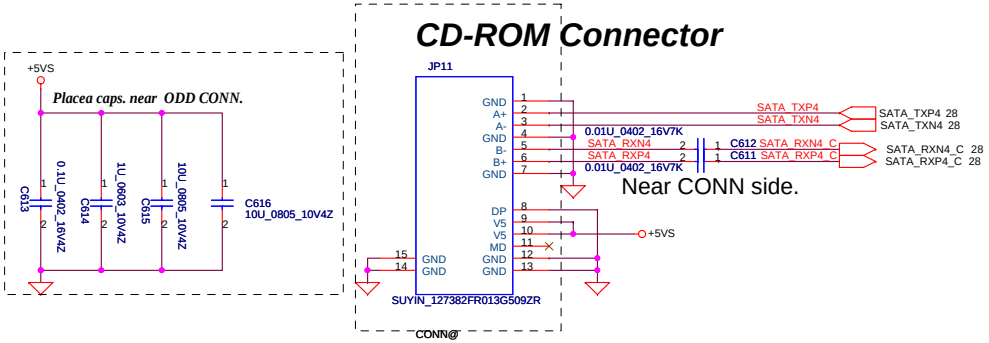
HDD Connector



2nd HDD Connector-option



CD-ROM Connector



SI: Update ODD footprint to fix pin reverse issue

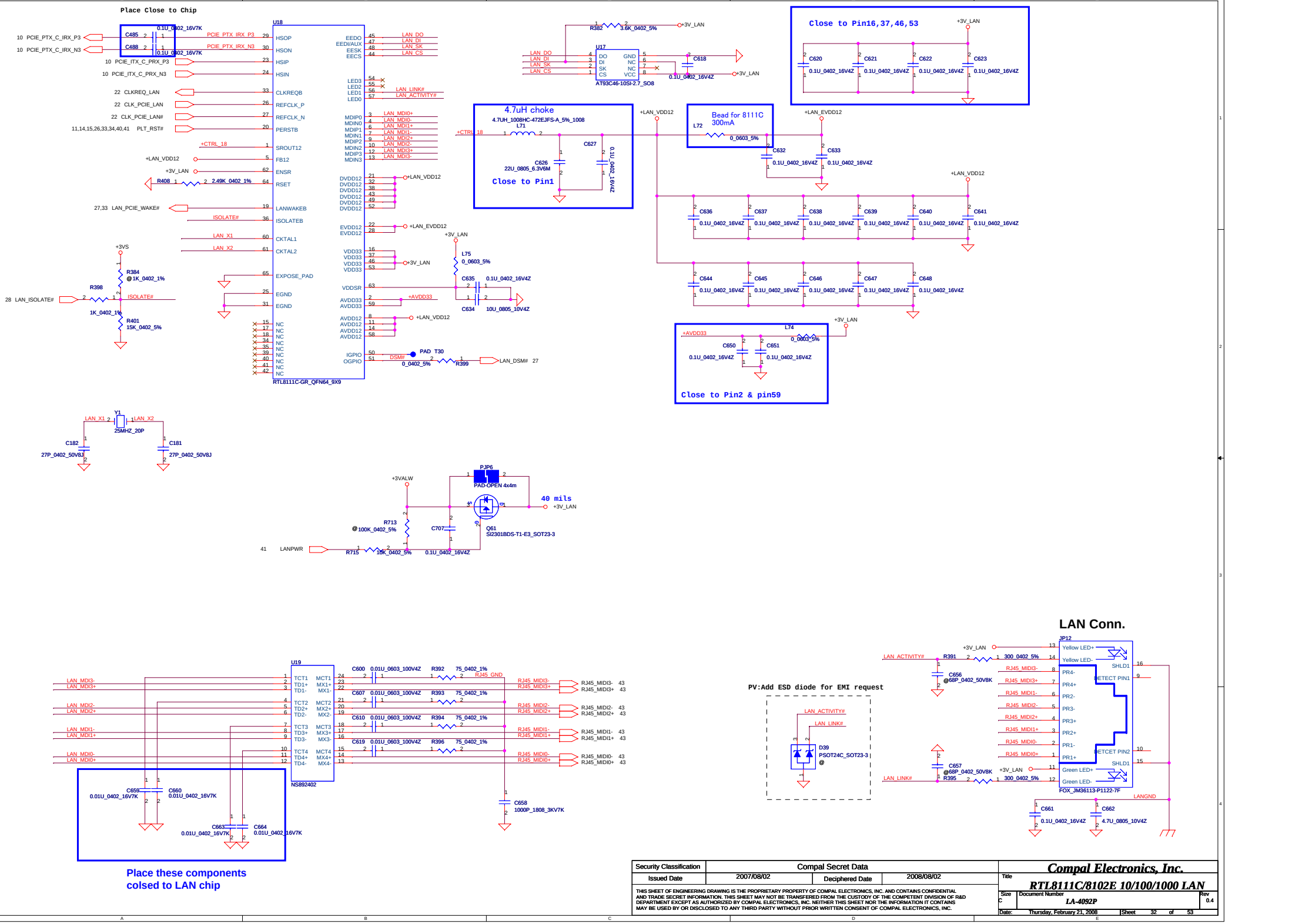
Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.

Title: **HDD/CDROM**

Size	Document Number	Rev
Custom	LA-4092P	0.4

Date: Thursday, February 21, 2008 | Sheet 31 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.

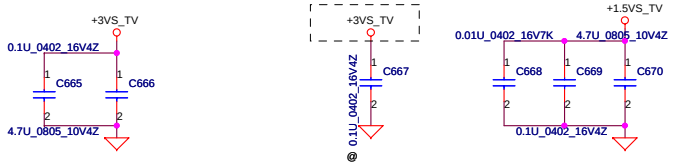
Title: **RTL8111C/8102E 10/100/1000 LAN**

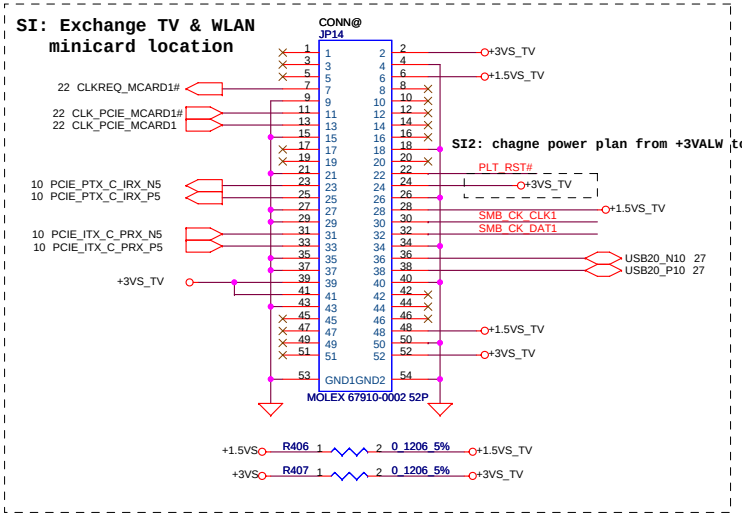
Size	Document Number	Rev
C	LA-4092P	0.4

Date: Thursday, February 21, 2008 | Sheet 32 of 53

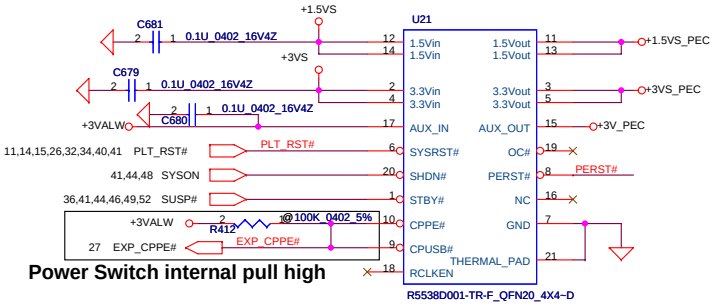
Mini Card---TV tuner

SI2: chagne power plan from +3VALW to +3VS_TV





New Card

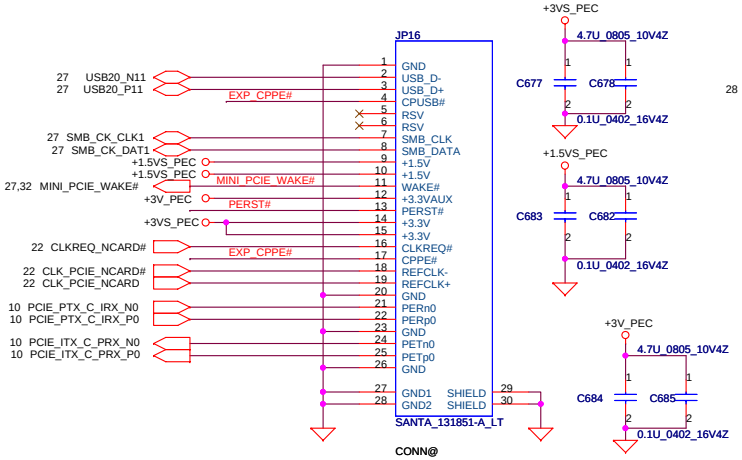


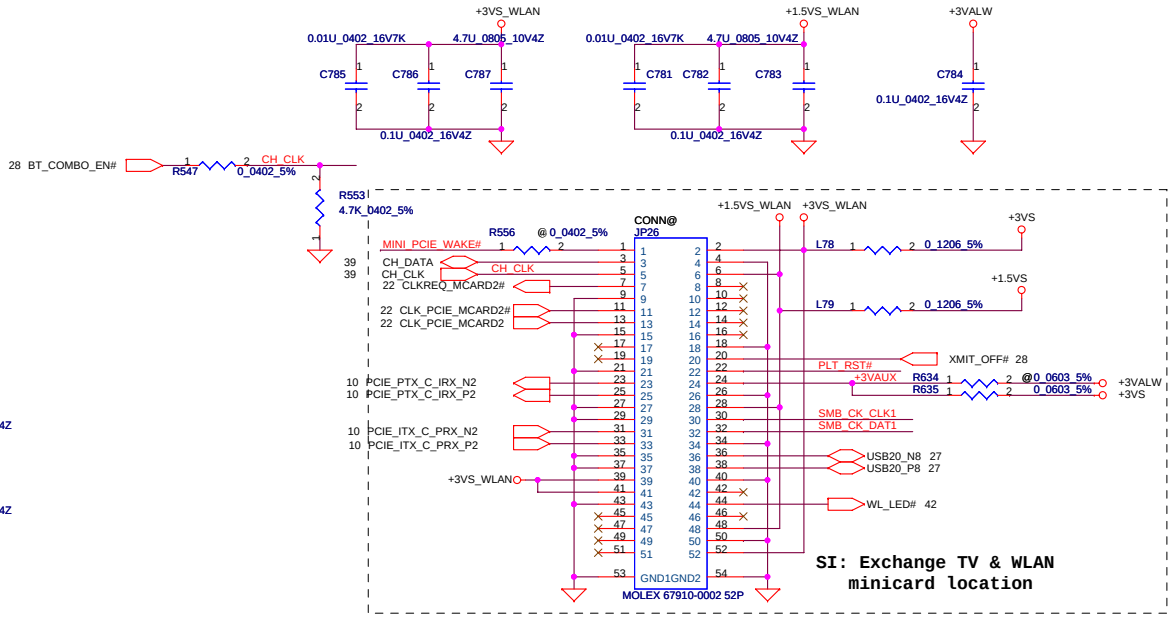
Power Switch internal pull high

USE TI TPS2231MRGPR

Mini-Express Card---WLAN

Near to Express Card slot.





Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.

Title: **Mini-Card/Mini-PCI/Express Card**

Size	Document Number	Rev
Custom	LA-4092P	0.4

Date: Thursday, February 21, 2008 Sheet 33 of 53

SI:Per ME request change
JP21 to new one

Card Reader Connector

JP21 — 7 IN 1 CONN — TAITW_R015-B10-LM — CONN@

+VCC_4IN1 (3)
XD_SD_MS_D0 (32) XD_SD_MS_D1 (10) XD_SD_MS_D2 (9) XD_SD_MS_D3 (8) XD_SD_D4 (7) XD_SD_D5 (6) XD_SD_D6 (5) XD_SD_D7 (4)
SDCMD_MSBS_XDWE# (34) XDWP#_SDWP# (33) XD_ALE (35) XD_CD# (40) XD_RB# (39) XD_RE# (38) XDCE# (37) XD_CLE (36)
7IN1 GND (11, 31, 41, 42)
XD-VCC XD-D0 XD-D1 XD-D2 XD-D3 XD-D4 XD-D5 XD-D6 XD-D7 XD-WE XD-WP XD-ALE XD-CD XD-R/B XD-RE XD-CE XD-CLE 7IN1 GND 7IN1 GND

SD-VCC (21) MS-VCC (28) → +VCC_4IN1
SD_CLK (20) → SDCLK
SD-DAT0 (12) → XD_SD_MS_D0
SD-DAT1 (30) → XD_SD_MS_D1
SD-DAT2 (29) → XD_SD_MS_D2
SD-DAT3 (27) → XD_SD_MS_D3
SD-DAT4 (23) → XD_SD_D4
SD-DAT5 (18) → XD_SD_D5
SD-DAT6 (16) → XD_SD_D6
SD-DAT7 (25) → XD_SD_D7
SD-CMD (14) → SDCMD_MSBS_XDWE#
SD-CD-SW (1) → XDCD0#_SDCD#
SD-WP-SW (2) → XDWP#_SDWP#
MS-SCLK (26) → MSCLK
MS-DATA0 (17) → XD_SD_MS_D0
MS-DATA1 (15) → XD_SD_MS_D1
MS-DATA2 (19) → XD_SD_MS_D2
MS-DATA3 (24) → XD_SD_MS_D3
MS-INS (22) → XDCD1#_MSCD#
MS-BS (13) → SDCMD_MSBS_XDWE#

+VCC_4IN1
10K_0402_5% R45 → XDWP#_SDWP#
10K_0402_5% → XD_RB#
R106

XDCE# — R411 100_0402_5%@ — C901 100P_0402_25V8K@

+3VS
10K_0402_5% R405 → XD_CLE
10K_0402_5% R122 → XD_ALE
200K_0402_5% R86 → XD_RE#

SI:Per Jmicro request change
R405 & R122 from 200K to 10K

SDCLK — R413 @100_0402_5% — C902 @100P_0402_25V8K
MSCLK — R410 @100_0402_5% — C900 @100P_0402_25V8K

SI2:Support D3E function

+3VS
R126 10K_0402_5%
Q54 2N7002_SOT23-3
27 CR_CPPE# → CPPE#
28 CR_WAKE# → 0_0402_5% R397 → XDCD0#_SDCD#

10 PCIE_PTX_C_IRX_N1 — C693 0.1U_0402_16V7K — PCIE_PTX_IRX_N1
10 PCIE_PTX_C_IRX_P1 — C697 0.1U_0402_16V7K — PCIE_PTX_IRX_P1

SI:Per Jmicro request change
R114 from 10K to 8.2K
8.2K_0402_5% R114

Power Circuit

U23 — JMB380 — JMB380-QGAZ0A_QFN48_7X7

22 CLK_PCIE_MCARD0# → APCLKN
22 CLK_PCIE_MCARD0 → APCLKP
10 PCIE_ITX_C_PRX_N1 → APRXN
10 PCIE_ITX_C_PRX_P1 → APRXP
APTXN APTXP APREXT
XIN XOUT → TXIN TXOUT
TAV33
XRSTN XTEST
SEEDAT SEECLK
CR1_CD1N CR1_CD0N
CR1_PCTLN
CR1_LEDN

APVDD (5) APV18 (10)
DV33 (19, 20, 44) DV18 (18, 37)
GND (49)

MDIO0 (48) → XD_SD_MS_D0
MDIO1 (47) → XD_SD_MS_D1
MDIO2 (46) → XD_SD_MS_D2
MDIO3 (45) → XD_SD_MS_D3
MDIO4 (43) → SDCMD_MSBS_XDWE#
MDIO5 (42) → SDCLK_MSCLK_XDCE#
MDIO6 (41) → XDWP#_SDWP#
MDIO7 (40) → XD_CLE
MDIO8 (29) → XD_SD_D4
MDIO9 (28) → XD_SD_D5
MDIO10 (27) → XD_SD_D6
MDIO11 (26) → XD_SD_D7
MDIO12 (25) → XD_RE#
MDIO13 (23) → XD_RB#
MDIO14 (22) → XD_ALE

TPA1P (34) → TPA+
TPBIAS_1 (35) → TPBIAS
TREXT (36) → R124 12K_0402_1%
TCPS (31) → TPB-
TPB1N (32) → TPB+
TPB1P (33) → TPA-
TPA1N

+1.8VS_OUT
0.1U_0402_16V4Z C892 — 10U_0805_10V4Z
1000P_0402_50V7K C688 C687 C893 — 0.1U_0402_16V4Z
R387 @0_0603_5% → +1.8VS

SI:Use build in Regulator
Chip unmount R387

+3VS
C691 C692 — 0.1U_0402_16V4Z
C686 C690 0.1U_0402_16V4Z — 0.1U_0402_16V4Z
+1.8VS_OUT

SDCLK_MSCLK_XDCE# — 22_0402_5% R457 SDCLK, R456 MSCLK, R455 XDCE#

SI:Use build in Regulator
Chip mount R383,C689,C694

+VCC_OUT — R383 0_0603_5% — +VCC_4IN1
C689 10U_0805_10V4Z — C694 0.1U_0402_16V4Z

+3VS
4.7K_0402_5% R121 → XDCD0#_SDCD#
4.7K_0402_5% R111 → XDCD1#_MSCD#

+5VS
R370 470_0402_5%
D5 HT-F196BP5_WHITE
Q53 2N7002_SOT23-3
CR_LED# — R113 4.7K_0402_5%

SI:Use new chip ,change to
High active control

+3VS — C695 0.1U_0402_16V4Z
11,14,15,26,32,33,40,41 PLT_RST#
CPPE#
XDCD1#_MSCD# XDCD0#_SDCD#
+VCC_OUT
CR_LED#

XDCD1#_MSCD# XDCD0#_SDCD# — D40 DAN202U_SC70 — XD_CD# — C696 270P_0402_50V7K

Close to Chip

C899 220P_0402_50V7K
R140 4.99K_0402_1%
R133 56_0402_5%
R199 56_0402_5%
TPB- TPB+ TPA- TPA+
JP19 @SUYIN_020115FR004S550ZL_4P-T
TPBIAS — C177 0.33U_0603_10V7K
R200 56_0402_5%
R290 56_0402_5%

SI:Change 1394 connector

SI:Use build in Regulator
Chip unmount U22 and relation parts

+VCC_OUT — +VCC_4IN1 — 40mil
+3VS
U22 — IN EN GND OUT OUT
C895 @0.1U_0402_16V4Z
@G5250C2T1U_SOT23-5
C896 @1U_0603_10V4Z
@ 150K_0402_5% R123
reserved power circuit

C897 22P_0402_50V8J — XIN
X2 24.576MHz_16P_3XG-24576-43E1
R134
C898 22P_0402_50V8J — XOUT 1M_0402_5%

SI2: Use B version chip

Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.

Title: JMB380/385 card reader/1394

Size	Document Number	Rev
Custom	LA-4092P	0.4

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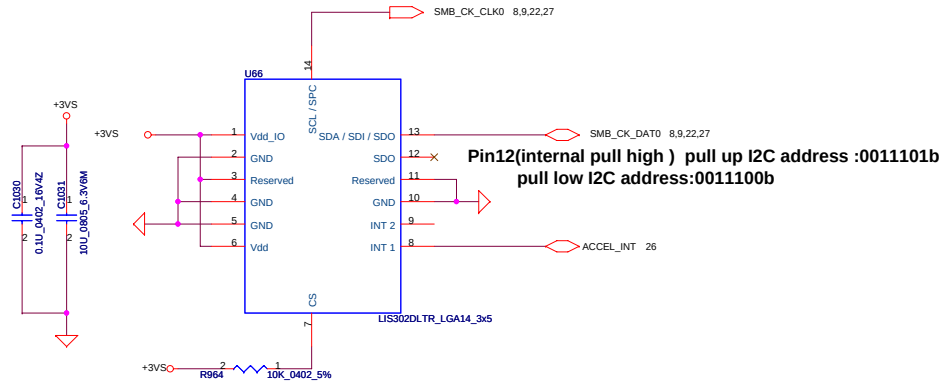
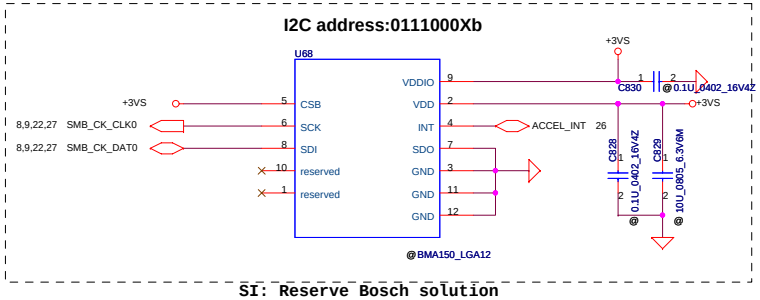
ACCELEROMETER





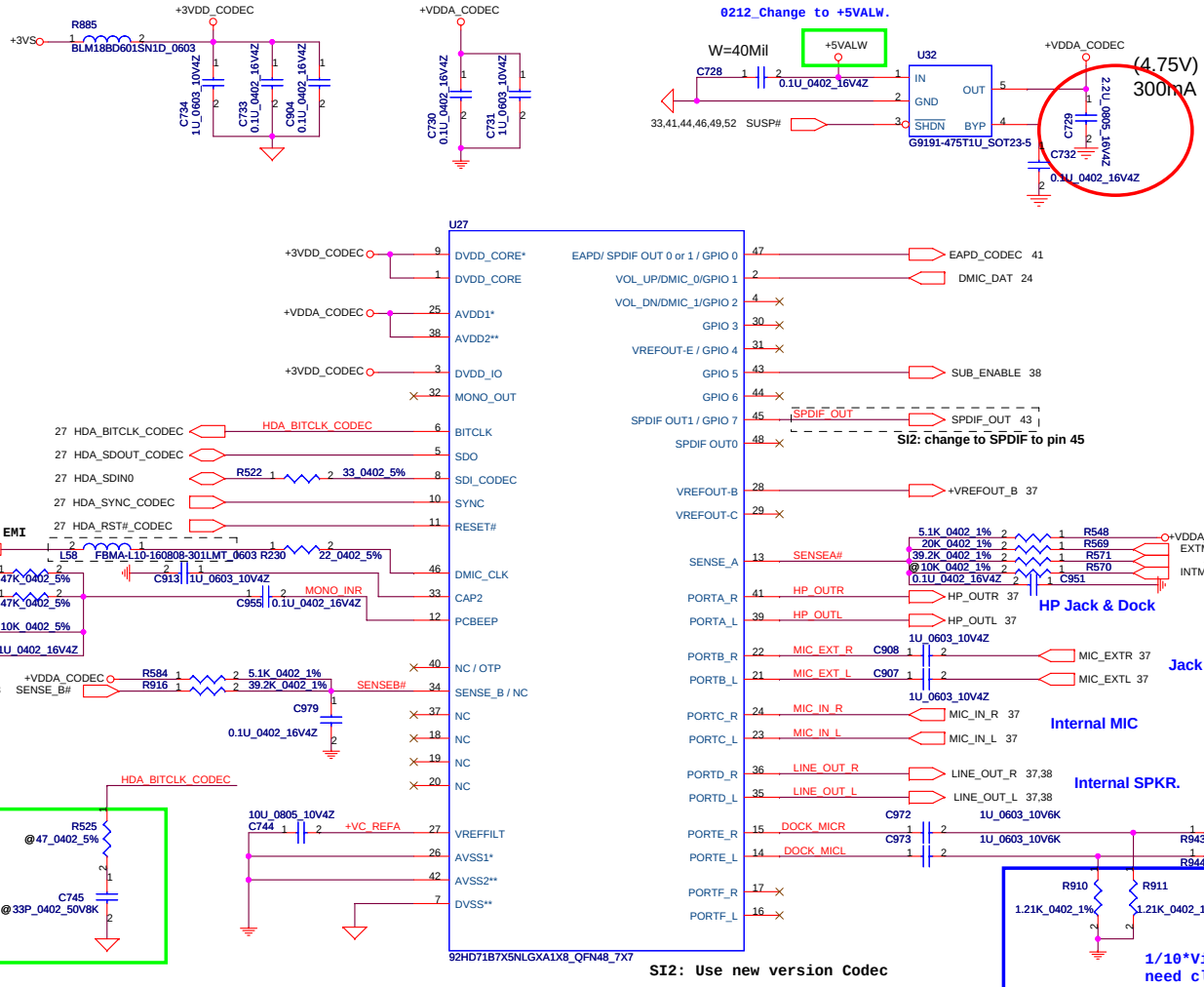
SI: Reserve Bosch solution

Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2006/10/06

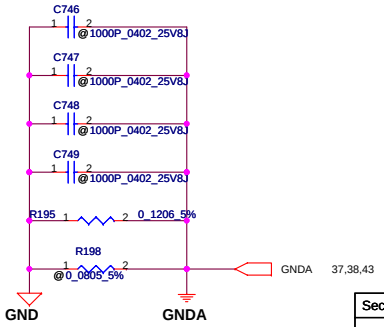
Compal Electronics, Inc.

Title	R5C833_1394	
Size: Custom	Document Number: LA-4092P	Rev: 0.4
Date: Thursday, February 21, 2008	Sheet 35 of 53	

CODEC POWER



SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K



HP_DET#	MIC_DET	LINEOUT	PORT-A <Earphone OUT>	MIC	EQ
0(LOW)	0(LOW)	OFF	ON	ON	Disable
0(LOW)	NC	OFF	ON	OFF	Disable
NC	0(LOW)	ON	OFF	ON	Enable
NC	NC	ON	OFF	OFF	Enable

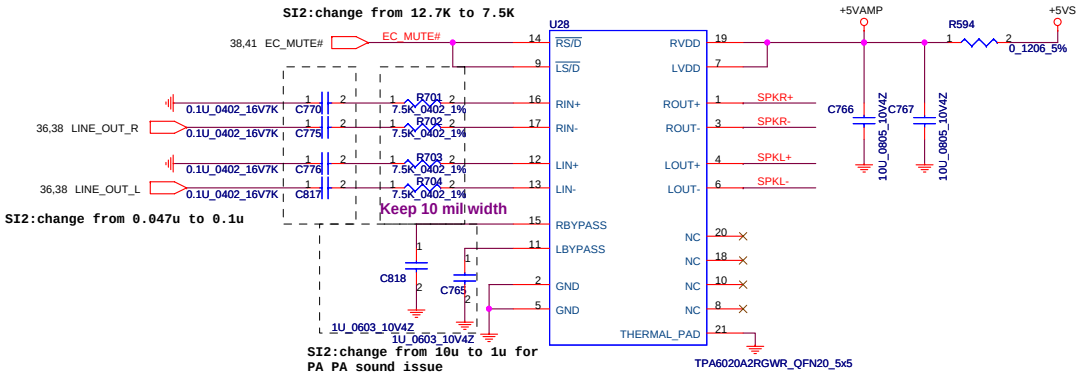
Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

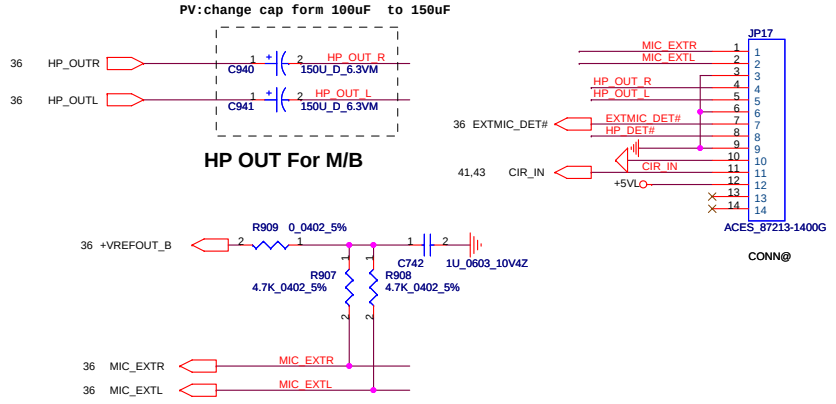
Compal Electronics, Inc.

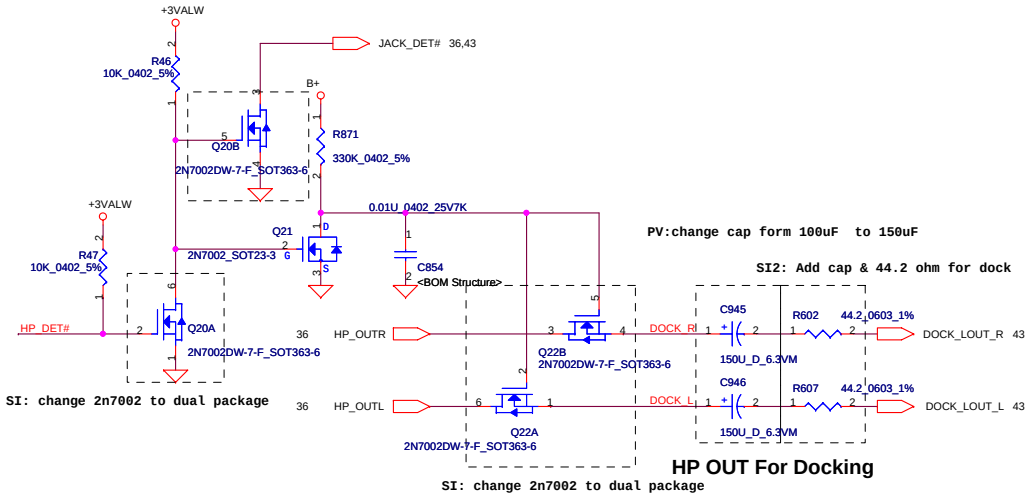
Title: Audio Codec-IDT9271B7

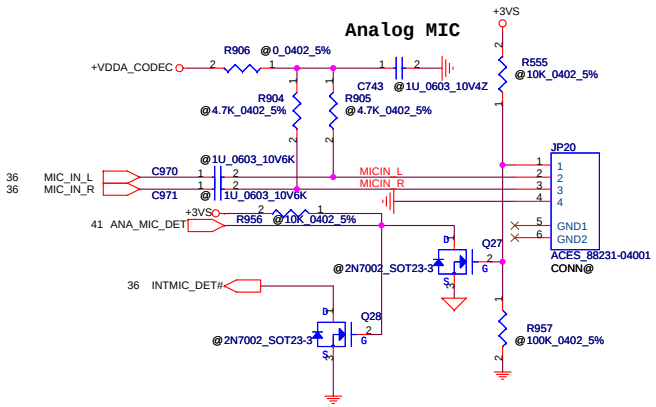
Size: Custom | Document Number: LA-4092P | Rev: 0.4

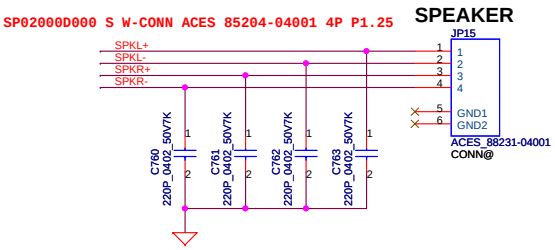
Date: Thursday, February 21, 2008 | Sheet 36 of 53





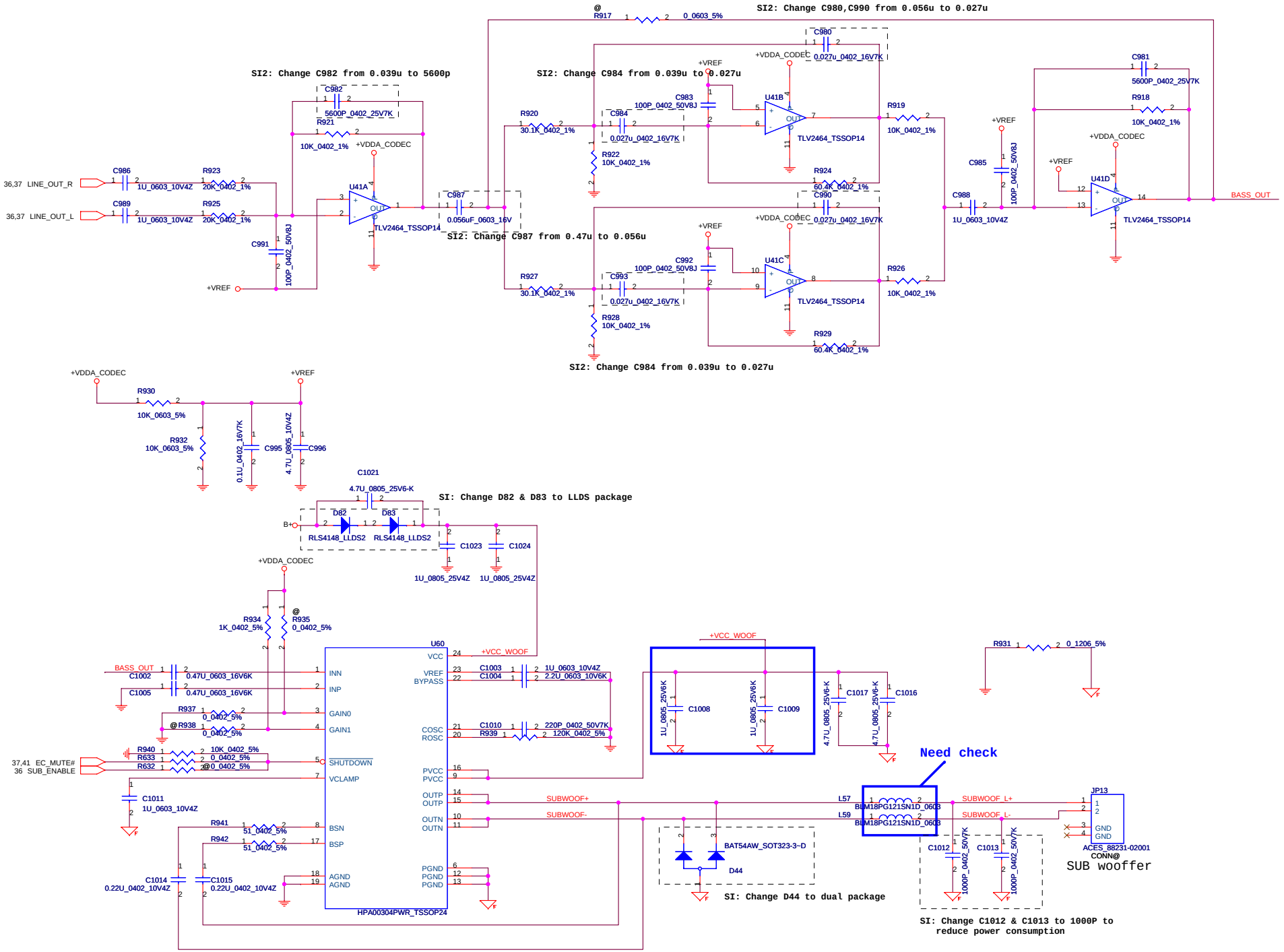






Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

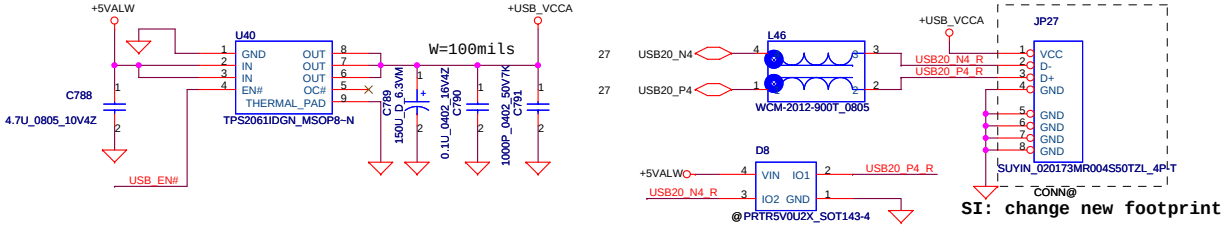
Compal Electronics, Inc.			
Title: AMP & Audio Jack			
Size: Custom	Document Number: LA-4092P		Rev: 0.4
Date: Thursday, February 21, 2008	Sheet 37 of 53		



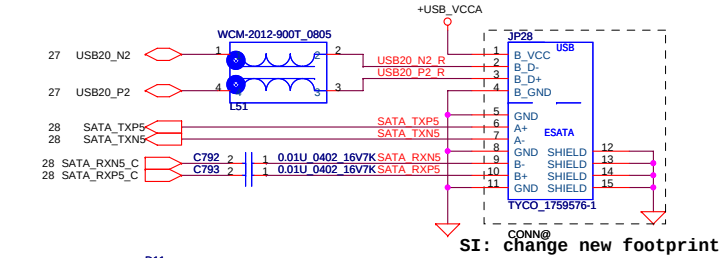
Security Classification	Compal Secret Data		
Issued Date	2006/10/26	Deciphered Date	2006/07/26

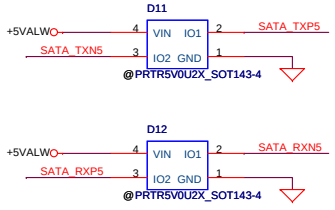
Title	EQ & Sub Woofer		
Size: Custom	Document Number: LA-4092P		Rev: 0.4
Date: Thursday, February 21, 2008	Sheet 38 of 53		

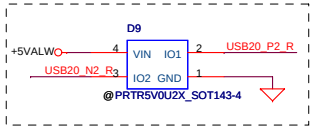
Left side USB CONNECTOR 0



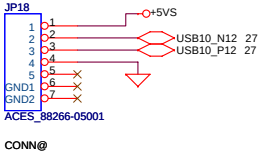
Left side ESATA/USB combination Connector



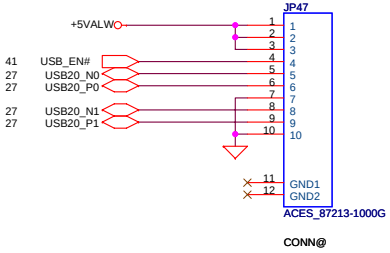




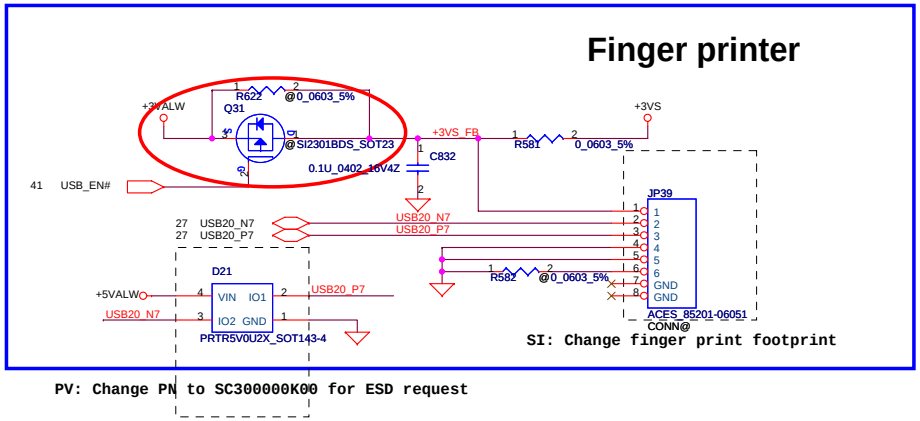
Touch screen



USB Board Conn

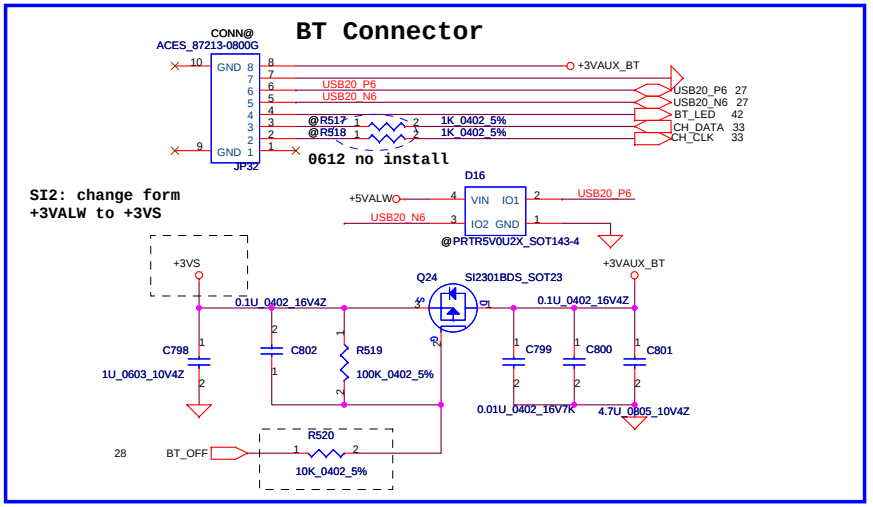


Finger printer



PV: Change PN to SC300000K00 for ESD request

BT Connector



SI: change to 10K ohm to make sure MOS can turn on

Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.			
Title: Cover Sheet			
Size: Custom	Document Number: LA-4092P		Rev: 0.4
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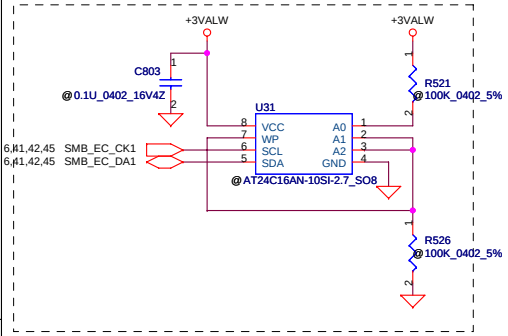
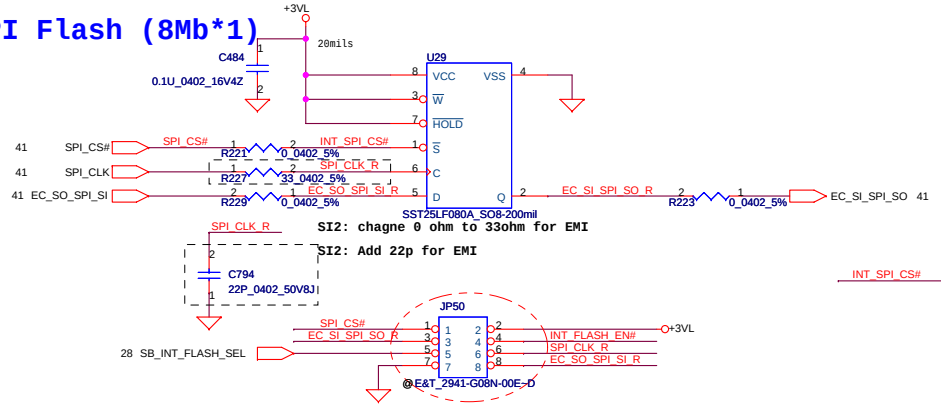
SI2: Change from +3VL to +3VALW and unmount this EEPROM



SPI Flash (8Mb*1)

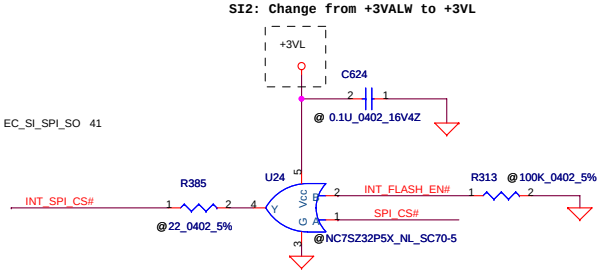


SI2: chagne 0 ohm to 33ohm for EMI

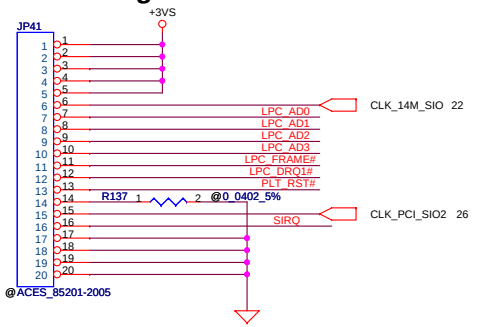
SI2: Add 22p for EMI

C:Chg. PN to LTC00000200

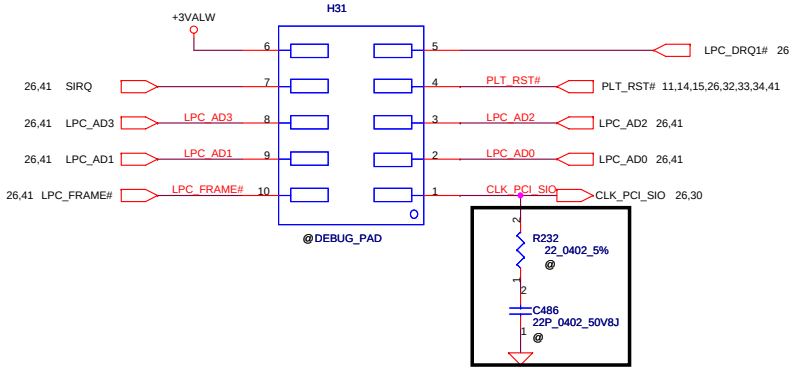
SI2: Change from +3VALW to +3VL



LPC Debug Port



LPC Debug Port

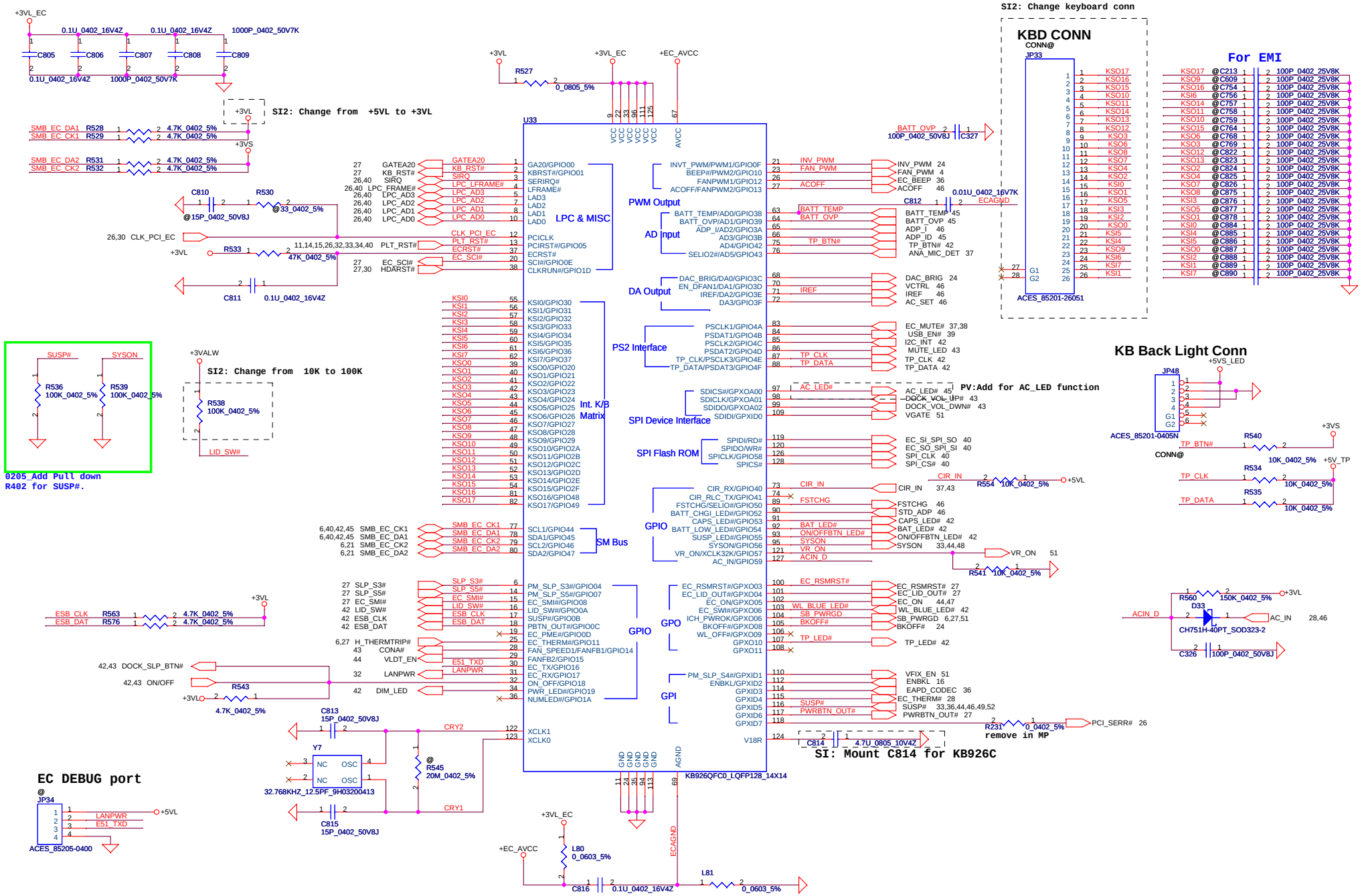


Compal Electronics, Inc.

Title: TCG/BIOS ROM/PS2/LED/SW

Size: Custom | Document Number: LA-4092P | Rev: 0.4

Date: Thursday, February 21, 2008 | Sheet 40 of 53


SI2: Change keyboard conn
KBD CONN
CONN@
JP33
ACES_85201-26051
For EMI
SI2: Change from +5VL to +3VL
SI2: Change from 10K to 100K
U33
KB926QFC0_LQFP128_14X14
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
Int. K/B Matrix
GPIO
SM Bus
GPO
GPI
KB Back Light Conn
JP48
ACES_85201-0405N
PV:Add for AC_LED function
0205_Add Pull down
R402 for SUSP#.
EC DEBUG port
@
JP34
ACES_85205-0400
Y7
32.768KHZ_12.5PF_9H03200413
CH751H-40PT_SOD323-2
SI: Mount C814 for KB926C
remove in MP
Security Classification
Compal Secret Data
Issued Date
2007/08/02
Deciphered Date
2008/08/02
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EC KB926/KB conn
Size
Custom
Document Number
LA-4092P
Rev
0.4
Date:
Thursday, February 21, 2008
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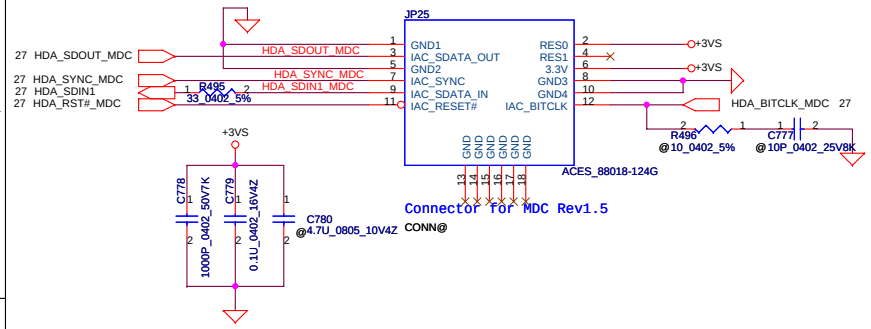
53

MDC 1.5 Conn.

Change type 4/25

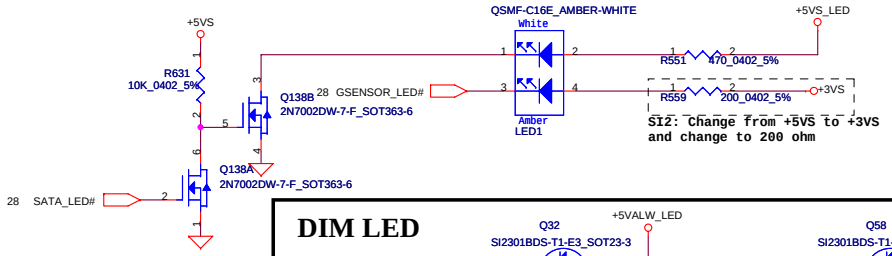


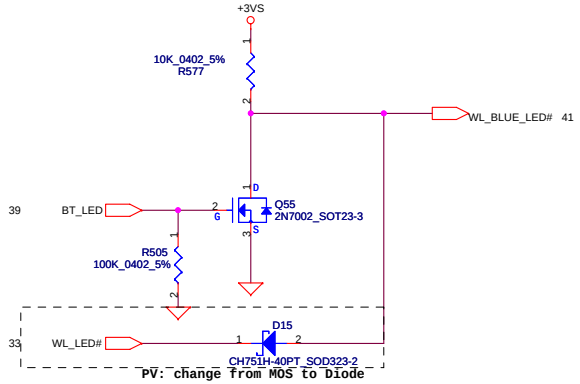
CAPS LOCK LED

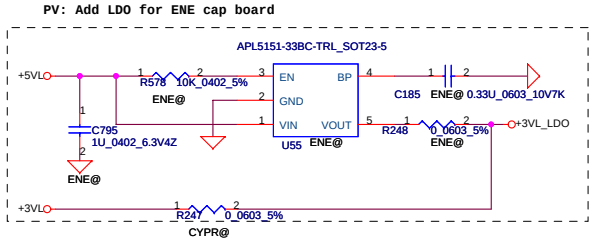
POWER LED(Left 1)

Battery Charge LED(Left 2)

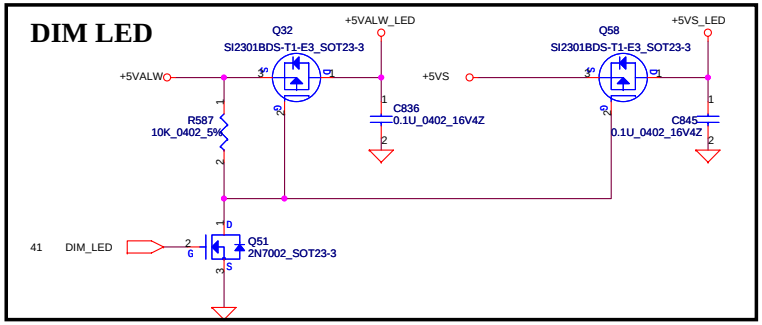
HDD LED(Left 3)





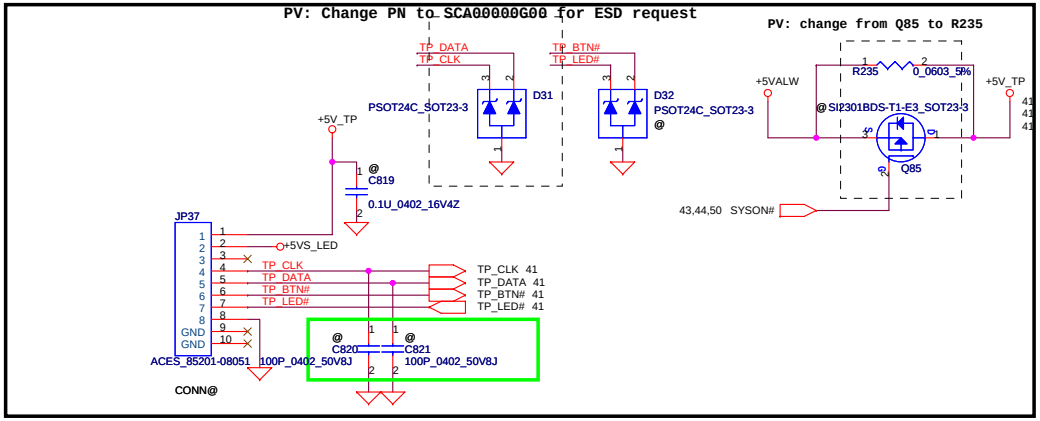


DIM LED

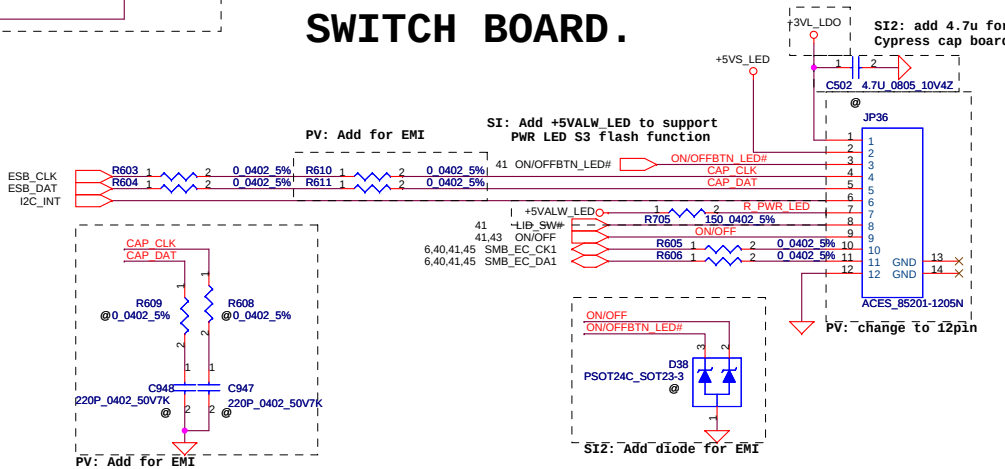


SI: Change to +3VL to support Qplay
bottom boot in BATT mode

T/P Board (Inculde T/P_ON/OFF)



SWITCH BOARD.



Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.			
Title	MDC/KBD/ON_OFF/LID		
Size: Custom	Document Number: LA-4092P		Rev: 0.4
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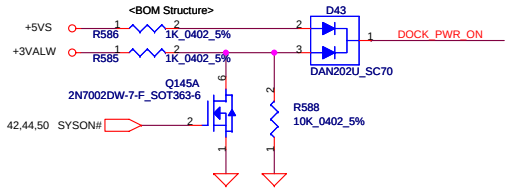
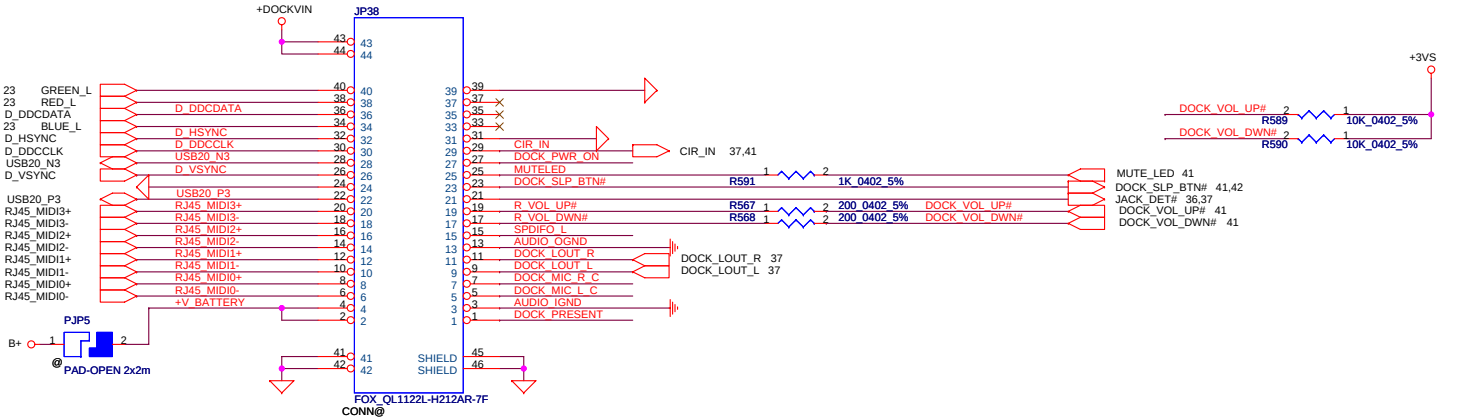
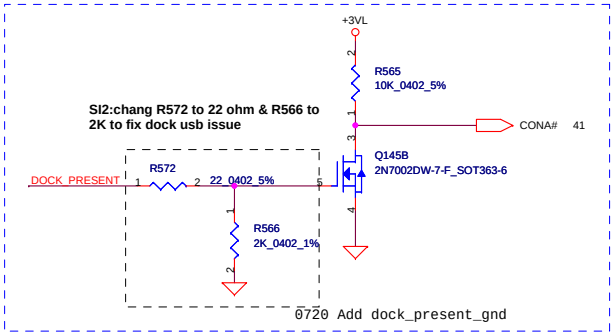
Atlas/ Saturn Dock

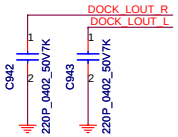


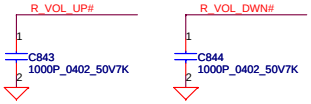
DOCK_PWR_ON Spec
0V = Notebook S4/S5, Dock off
2.5V = Notebook S3, Dock on
4V = Notebook S0, Dock on

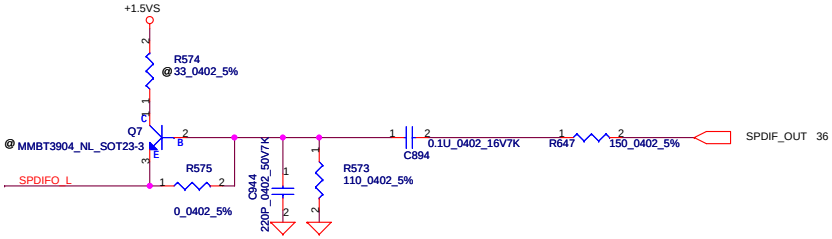


need change to reverse type connector



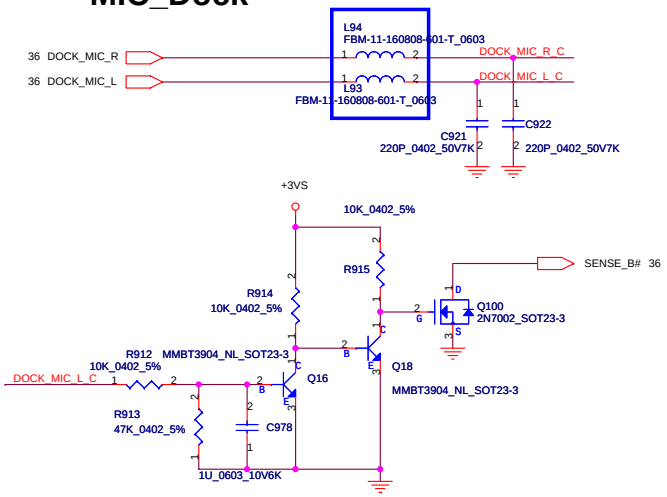






MIC_Dock

Need 600 Ohm 500 mA



Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.

Title: **DOCK CONN**

Size	Document Number	Rev
Custom	LA-4092P	0.4

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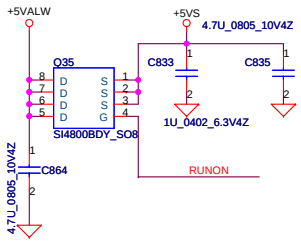
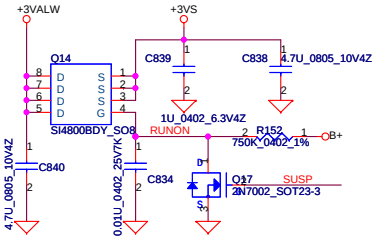
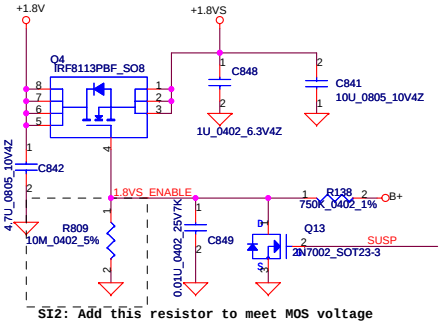
+5VALW TO +5VS



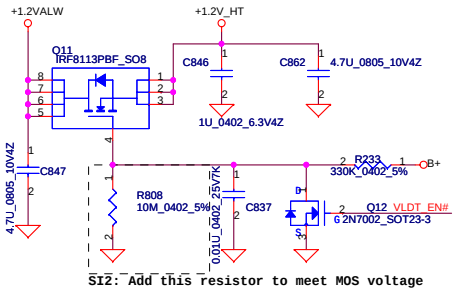
+3VALW TO +3VS

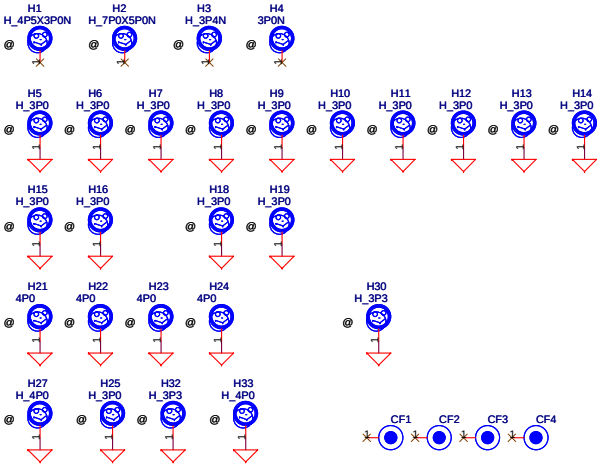


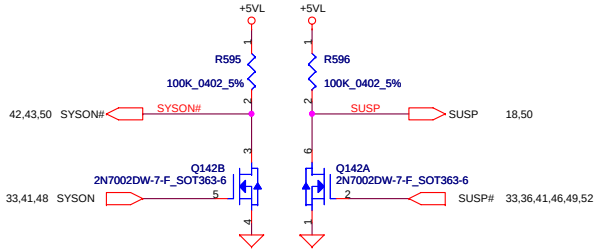
+1.8V TO +1.8VS



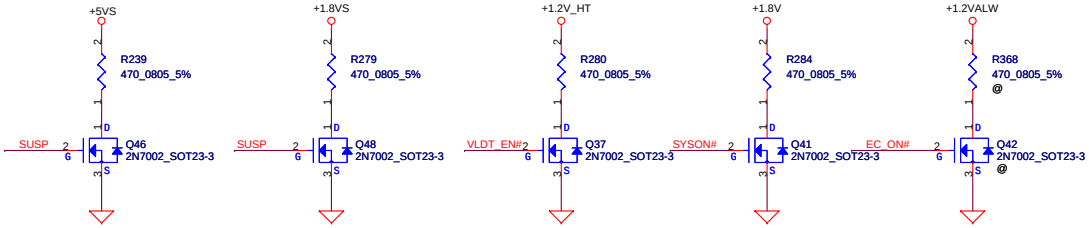
+1.2VALW TO +1.2V_HT

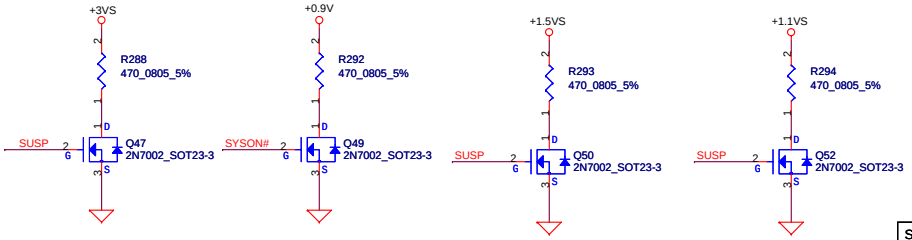


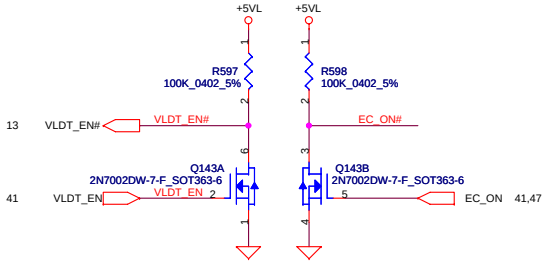




Discharge circuit







Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.

Title: **DC/DC Circuits**

Size	Document Number	Rev
Custom	LA-4092P	0.4

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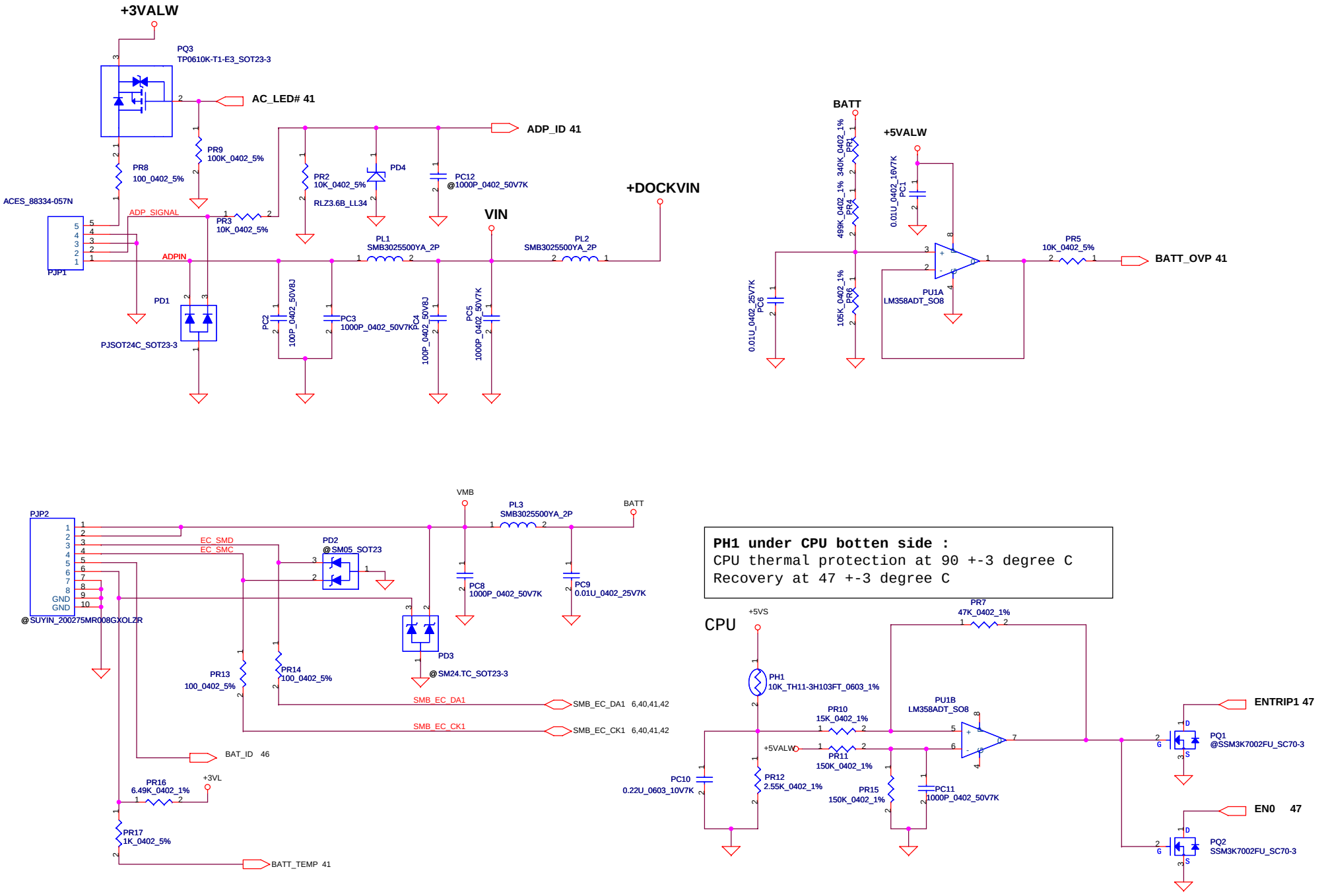


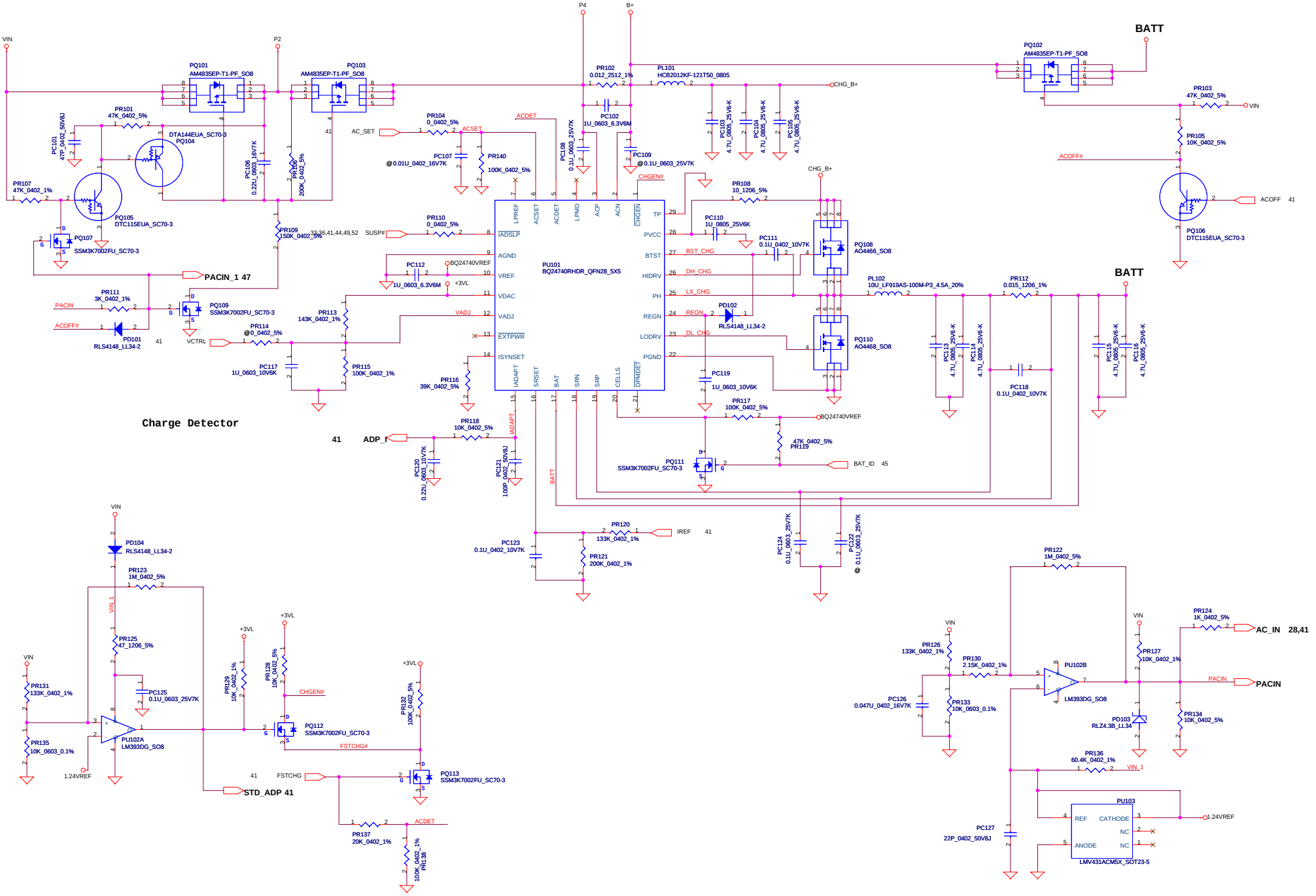
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **DC Connector/CPU_OTP**

Size	Document Number	Rev
	LA-4092P	0.1

Date: Thursday, February 21, 2008 | Sheet 45 of 53


Charge Detector
BATT
PU101
BQ24740RHDR_QFN28_5X5
PACIN_1 47
STD_ADP 41
AC_IN 28,41
PACIN
BAT_ID 45
IREF 41
ADP_I 41
VCTRL 41
FSTCHG 41
SUSP# 33,36,41,44,49,52
1.24VREF
LMV431ACM5X_SOT23-5
Security Classification
Compal Secret Data
Issued Date
2007/05/29
Deciphered Date
2008/05/29
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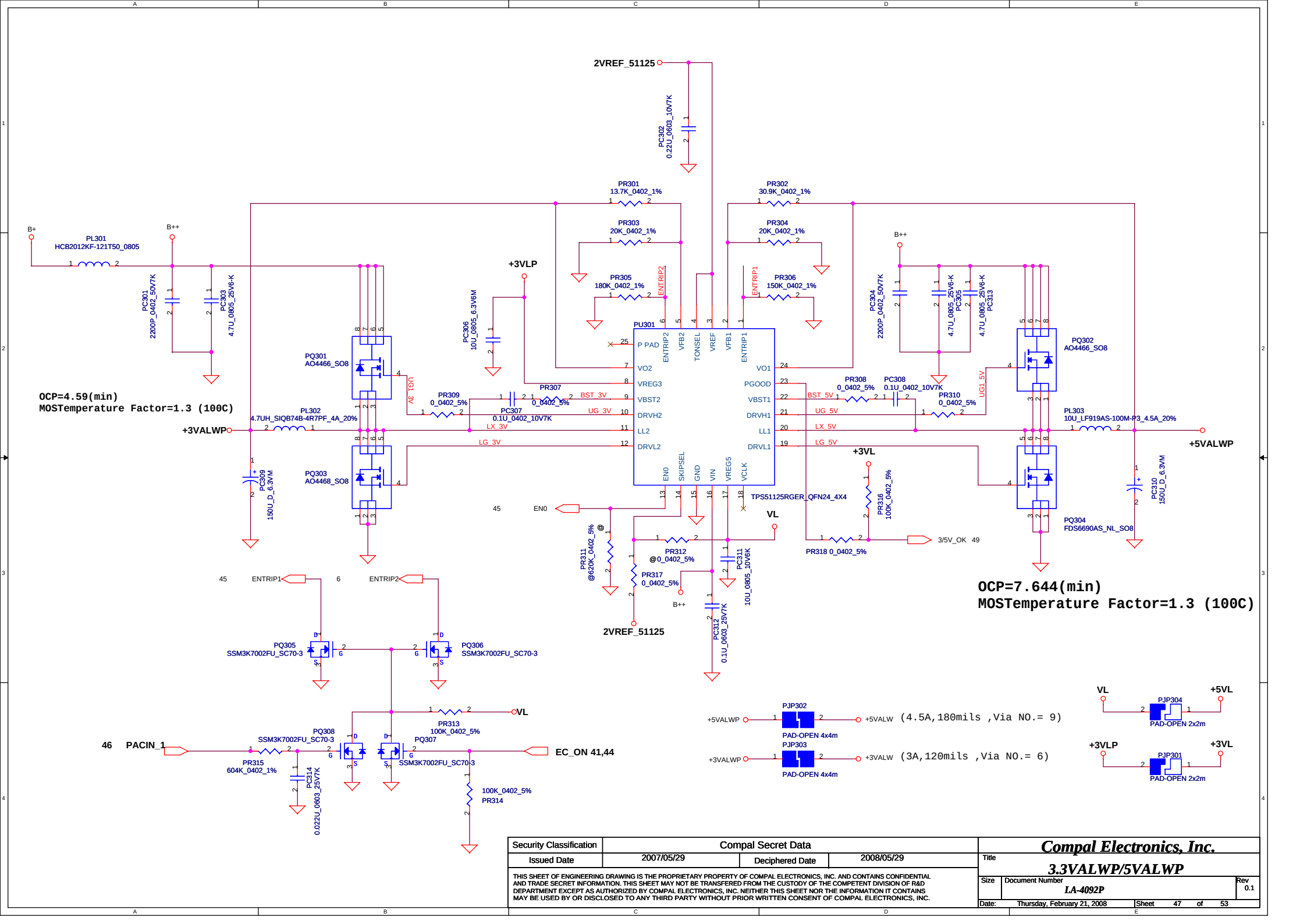
Compal Electronics, Inc.
Title
Charger
Size
Document Number
LA-4092P
Rev
0.1
Date: Thursday, February 21, 2008
Sheet 46 of 53



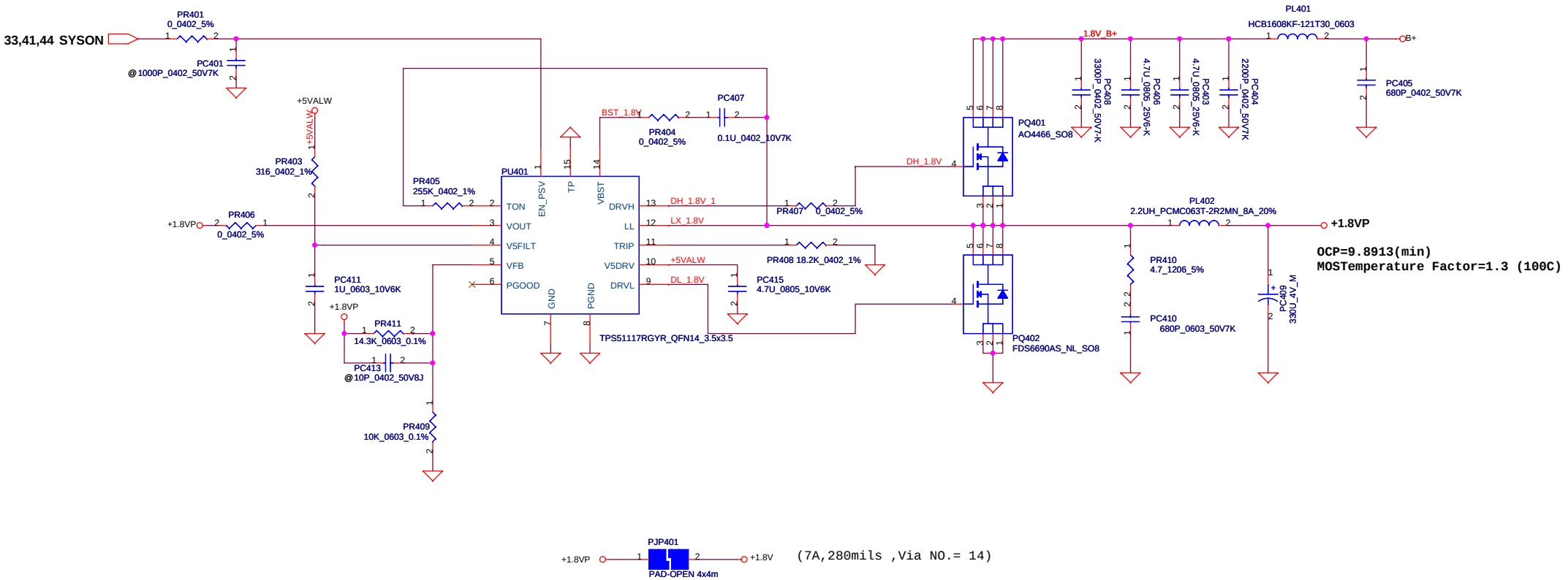
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **3.3VALWP/5VALWP**

Size	Document Number	Rev
	LA-4092P	0.1

Date: Thursday, February 21, 2008 | Sheet 47 of 53



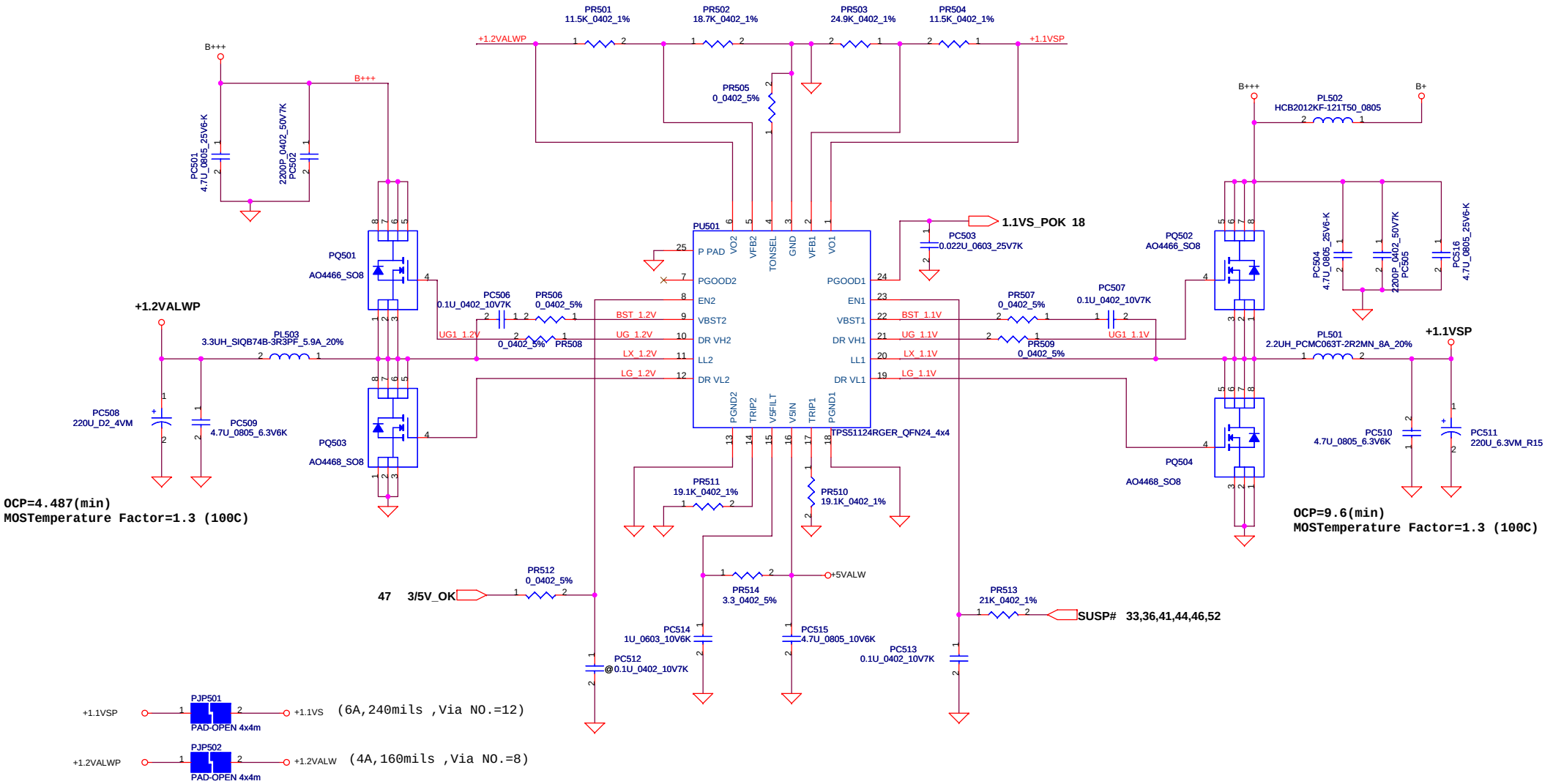
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **1.8VP**

Size	Document Number	Rev
	LA-4021P	0.1

Date: Thursday, February 21, 2008 | Sheet 48 of 53



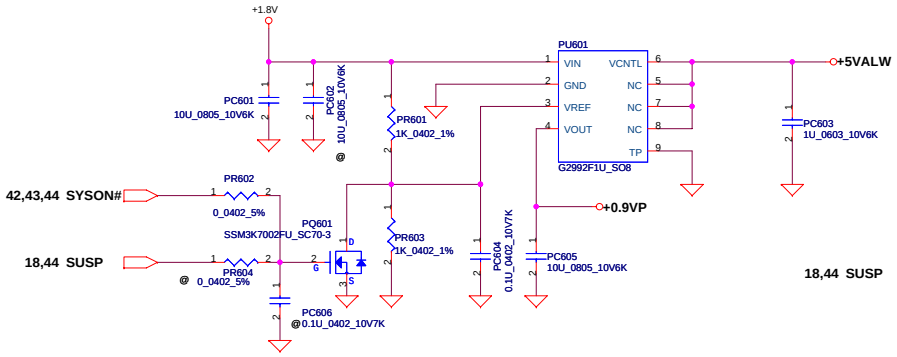
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

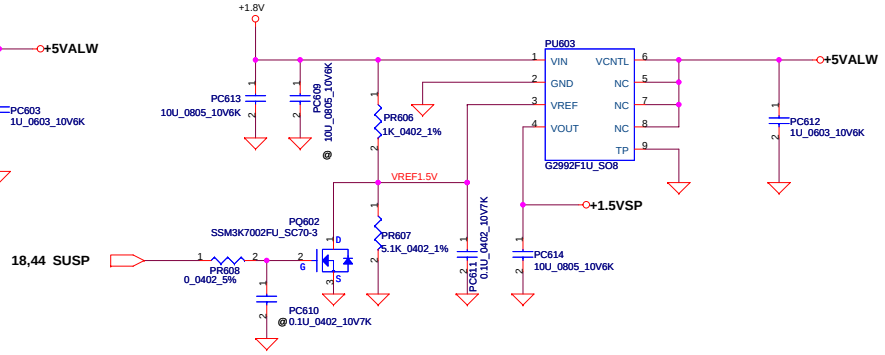
Compal Electronics, Inc.

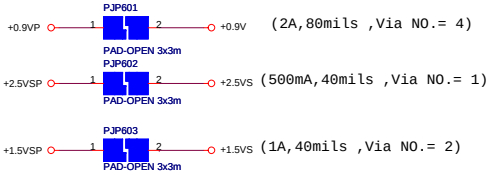
Title: **1.1VSP/1.2VALWP**

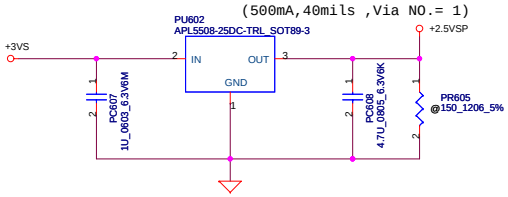
Size	Document Number	Rev
	LA-4092P	0.1

Date: Thursday, February 21, 2008 | Sheet 49 of 53









Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

Compal Electronics, Inc.

Title: **0.9VSP/2.5VSP/1.5VSP**

Size	Document Number	Rev
	LA-4092P	0.2

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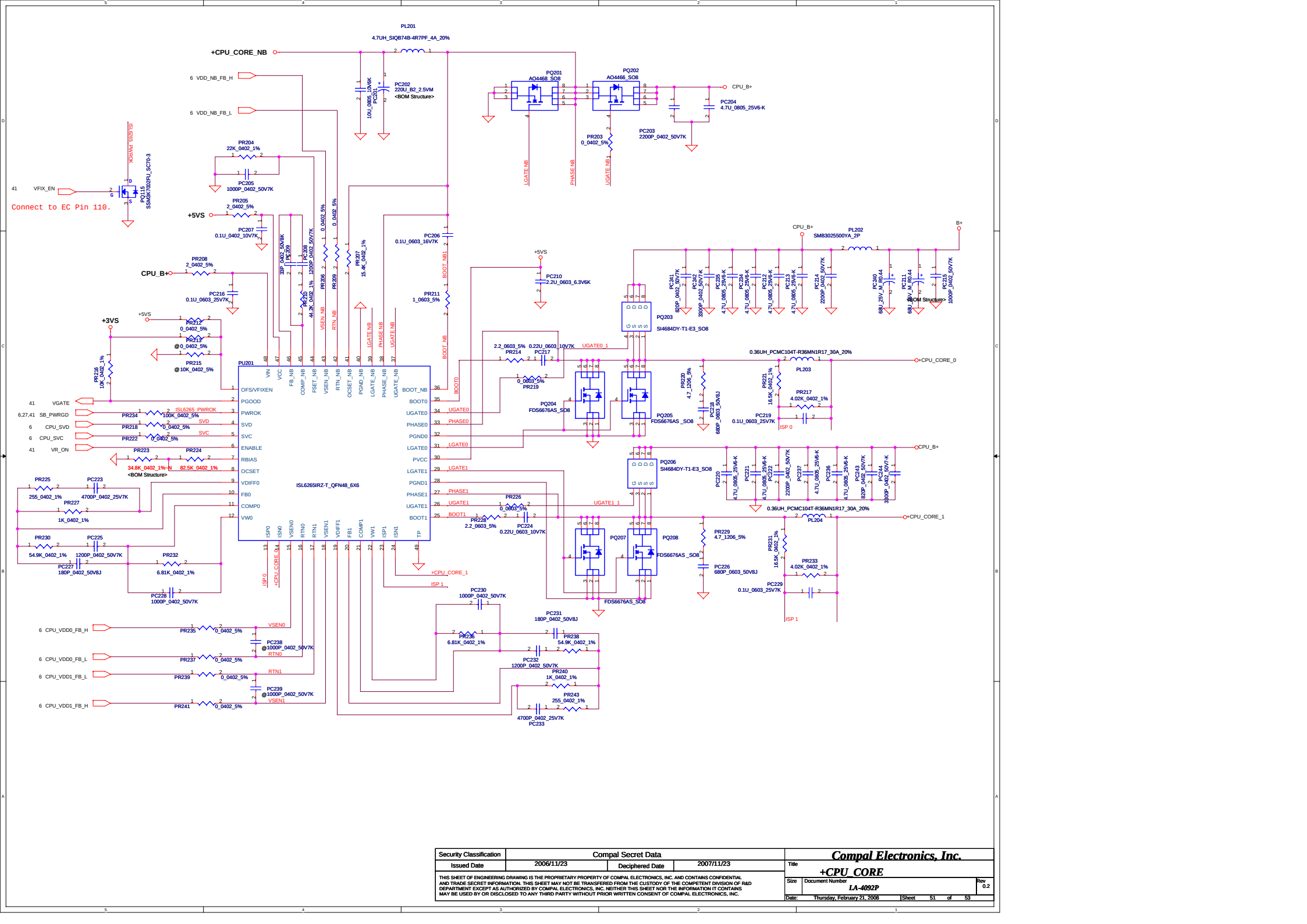


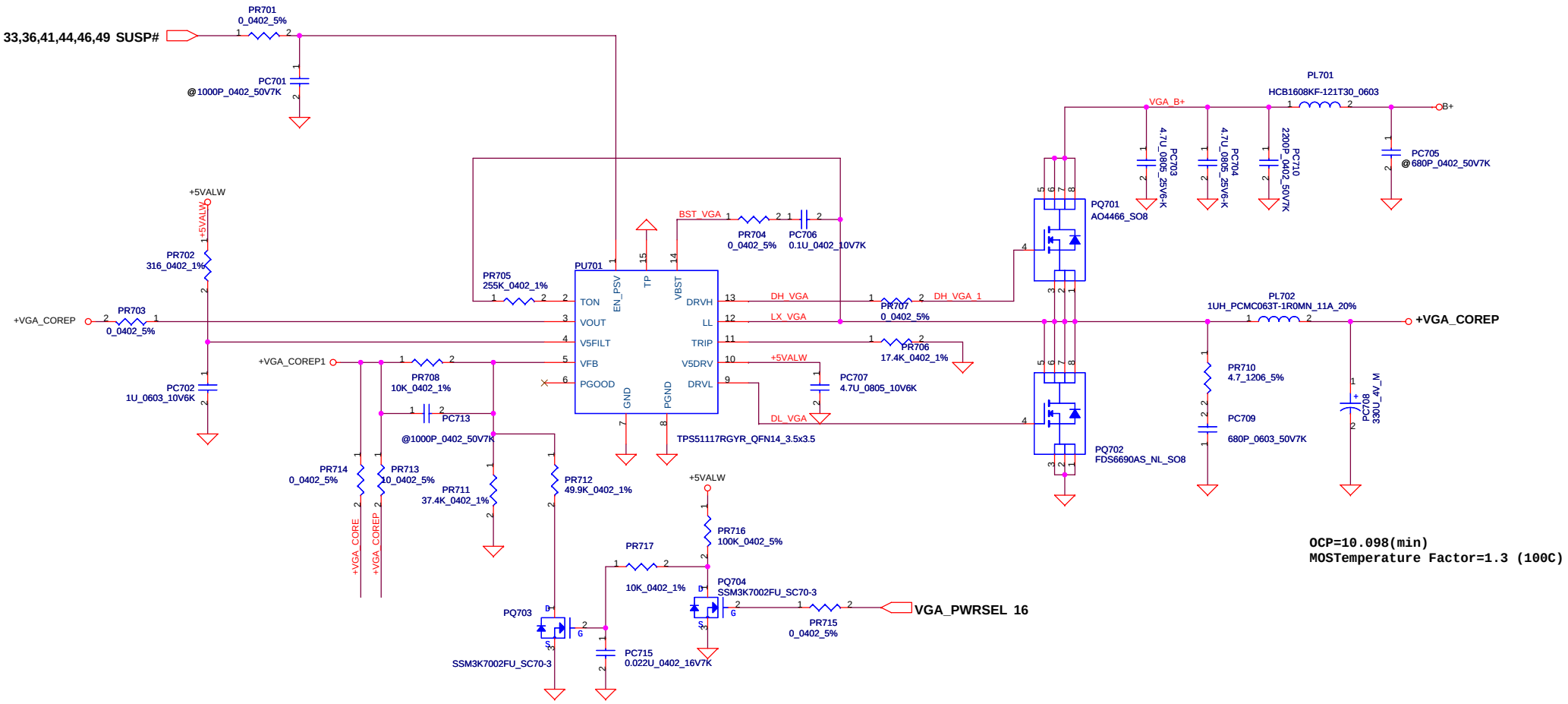
Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

Compal Electronics, Inc.

Title: **+CPU_CORE**

Size	Document Number	Rev
	LA-4092P	0.2

Date: Thursday, February 21, 2008 | Sheet 51 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: VGA_CORE

Size	Document Number	Rev
	LA-4092P	0.1

Date: Thursday, February 21, 2008 | Sheet 52 of 53

Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	48	1.8VP	10/23	Compal	for power requset	PU401 change the IC from "S IC RT8204PQW WQFN 16P" to "S IC TPS51117RGYR QFN 14P".	
2	46	Charger	10/30	Compal	for power requset	PQ104 swap the PQ104 1,3 Pin	
3	47	3V/5V	10/30	Compal	for power requset	Change PR301 to 13.7K modify output voltage	
4	47	3V/5V	10/30	Compal	for power requset	Change PR305 to 180K modify OCP	
5	47	3V/5V	10/30	Compal	for power requset	Change PR306 to 150K modify OCP	
6	47	3V/5V	10/30	Compal	for power requset	Change PR311 to 620K	
7	47	3V/5V	10/30	Compal	for power requset	Change PR315 to 604K modify sequence	
8	49	+1.1VSP	10/30	Compal	for power requset	Change PR510 to 19.1K modify OCP	
9	49	+1.2VALWP	10/30	Compal	for power requset	Change PR511 to 19.1K modify OCP	
10	46	Charger	10/30	Compal	for power requset	Del PR119	
11	51	CPU_CORE	10/30	Compal	for power requset	Change PC202 to B2 type for ME limit	
12	51	CPU_CORE	10/30	Compal	for power requset	Change PR223 to 17.8K and PR224 to 100K modify OCP	
13	51	CPU_CORE	10/30	Compal	for power requset	Change PR221,PR231 to 16.5K and PR217,PR233 to 4.02K for CPU_CORE compensation	
14	45	DC connector	10/30	Compal	for power requset	Add PR3,PD4,PC12 for ADP_ID function	
15	47	3V/5V	10/30	Compal	for power requset	Add PR317,PR318	
16	46	Charger	10/30	Compal	for power requset	Change net from +3VLP to +3VL	
17	49	+1.1VSP	10/30	Compal	for power requset	Change PR513 to 21K for HW power scquence.	
18	46	Charger	11/09	Compal	for power requset	Pop PR119 Unpop PR9	
19	50	0.9VSP	11/09	Compal	for power requset	Change PC601,PC605,PC611,PC603,PC613,PC614,PC612, PC201 for common part	
20	46	Charger	11/09	Compal	for power requset	Change PR112 to 0.015 Ohm	
21	49	+1.2VALWP	11/09	Compal	for power requset	Change PC508 to D2 size for ME limit	
22	51	CPU_CORE	12/05	Compal	for EMI requset	Add PR220,PR229 for EMI	
23	49	CPU_CORE	12/05	Compal	for EMI requset	Add PC218,PC226 for EMI	

Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	46	Charger	12/05	Compal	for power requset	Change PR120 to 133K to change charger current	
2	47	3V/5V	12/05	Compal	for power requset	Change PR302 to 30.9K for common part	
3	47	3V/5V	12/05	Compal	for power requset	Change PR304 to 20K for common part	
4	48	+1.8VP	12/05	Compal	for power requset	Change PR408 to 18.2K modify OCP	
5	52	VGA_CORE	12/05	Compal	for power requset	Change PR306 to 150K modify OCP	
6	52	VGA_CORE	12/05	Compal	for power requset	Change PR714 to 0 Ohm	
7	52	VGA_CORE	12/05	Compal	for power requset	Add PR713 100 Ohm	
8	45	DC Connector /CPU_OTP	12/25	Compal	for power requset	Del PR9	
9	46	Charger	12/25	Compal	for power requset	Reconnect from BQ24740VREF to +3VL	
10	47	3V/5V	12/25	Compal	for power requset	Add PU302	
11	52	VGA_CORE	12/25	Compal	for power requset	Del PC714 Change PC715 to 0.022u & PR713 to 10 Ohm	
12	51	CPU_CORE	12/27	Compal	for power requset	ADD PC204 & PC211 68uF	
13	48	+1.8VP	1/2	Compal	for EMI requset	Add PR410 4.7ohm and PC410 680P	
14	48	+1.8VP	1/2	Compal	for EMI requset	Add PC405 680P and 408 3.3nF	
15	51	CPU_CORE	1/2	Compal	for EMI requset	ADD PC241 820p & PC242 3300p	
16	52	VGA_CORE	1/2	Compal	for EMI requset	Add PR710 and PC709	
17	51	CPU_CORE	1/2	Compal	for EMI requset	ADD PC243 to 3.3n PC244 to 820p	
18	51	CPU_CORE	1/3	Compal	for power requset	ADD PR234 & PQ115	

Compal Electronics, Inc.

Title: Power Changed-List History-1

Size: Custom | Document Number: LA-4111P | Rev: 0.1

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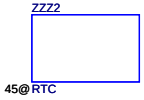
HW4 Product Improvement Record (P.I.R.)

1. Change R538 Pull high from +3VL to +3VALW
2. New add R563,R571 Pull high +3VS
3. Unmount BKOFF# Pull high R483
4. Unmount CPU_LDT_REQ# Pull high R318
5. Change LED1 P/N to SC500004C00
6. Change JP36 Pin2 from +5VS_LED to +5VALW_LED
7. Change C1012 & C1013 from 4700P to 1000P
8. Change R186 size from 0603 to 0402
9. Delete TV function and relation component
10. Add R554 for CIR pull high
11. Add C327 on BATT_OVT
12. Change L57 & L59 to 0603 BLM18PG121SN1D
13. exchange TV & WLAN mini card location
14. add LAN cable detect circuit
15. update ODD CONN footporint and symbol
16. delete Lid switch baord Conn
17. Change Cap sensor board power to +3VL to support Qplay boot

RTC



PCB

Security Classification	Compal Secret Data		
Issued Date	2007/5/18	Deciphered Date	2008/5/18

Compal Electronics, Inc.

Title: PIR

Size | Document Number | Rev 0.4

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