PCB Number: 11078-SA

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39	DC IN	
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45	Run PWR/USB PWR	
46	MEM_1D5V/MEM_VTT	
47	PCH_1D05V	
48	1D8V POWER	
49	GPU N12P-GV-B-A1	
50	GPU_SDRAM	
51	GPU_CORE(RT8208A)	
52	TBD	
53	TBD	

BOM Configuration
(R):Unmount
(G):GPU
(H):PCH
(D):Debug used
(S):Scalar

PCB BOARD SIZE
6 Layers
265mm X 190mm

SA BUILD

Sugar Bay :

LGA1155 : Sandy Brighe

Chipset : Cougar Point H61

LAN : Gb LAN 8111F

<Variant Name>

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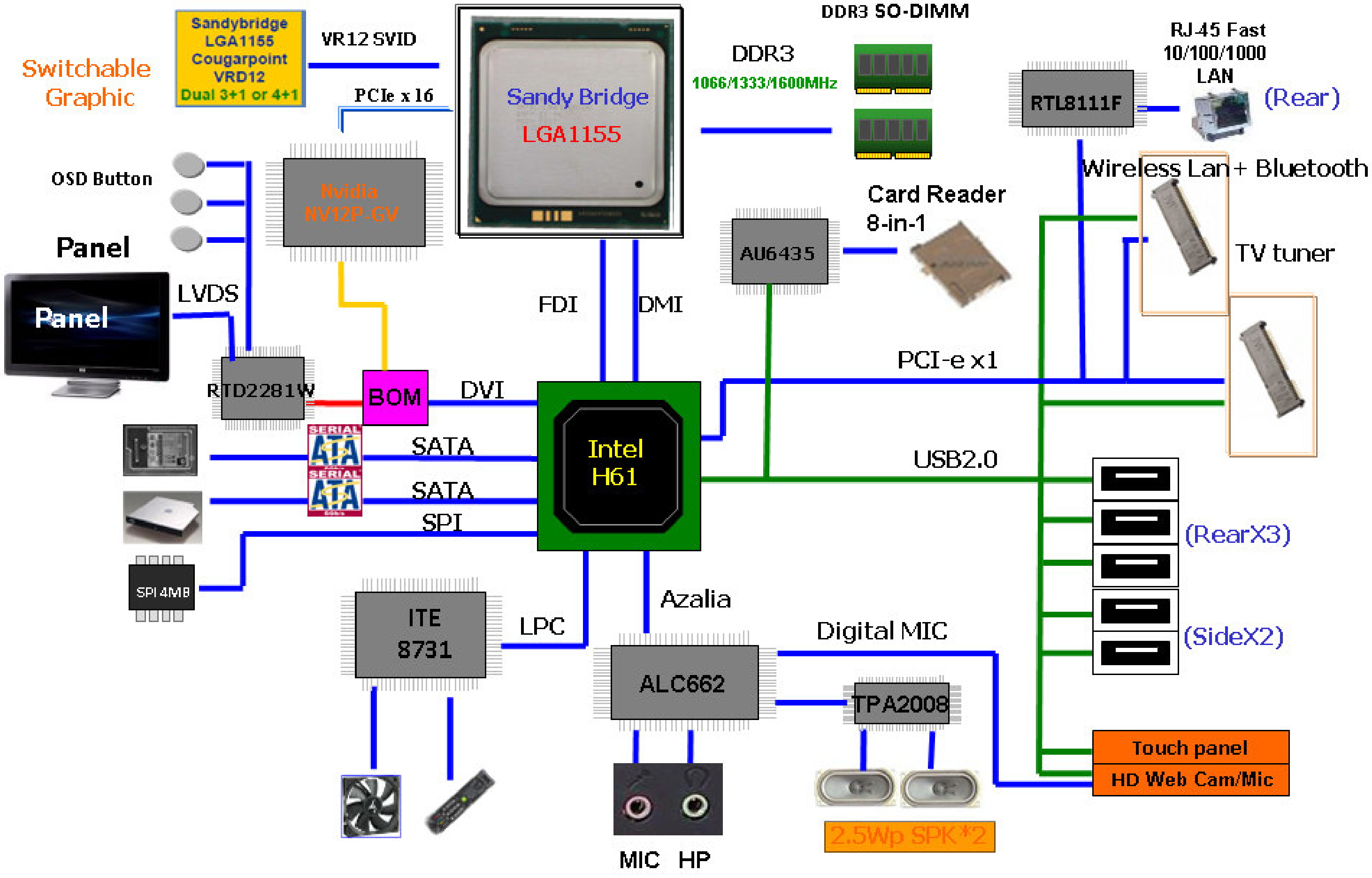
Title	Cover Page		
Size: Custom	Document Number: Rosa_Eagleton		Rev: SA
Date: Monday, February 13, 2012		Sheet 1 of 53	

Block Diagram for Eagleton

PCB BOARD SIZE
265mm X 184mm
4 Layer

Internal Slot/Header
Front/Rear IO
Chipset



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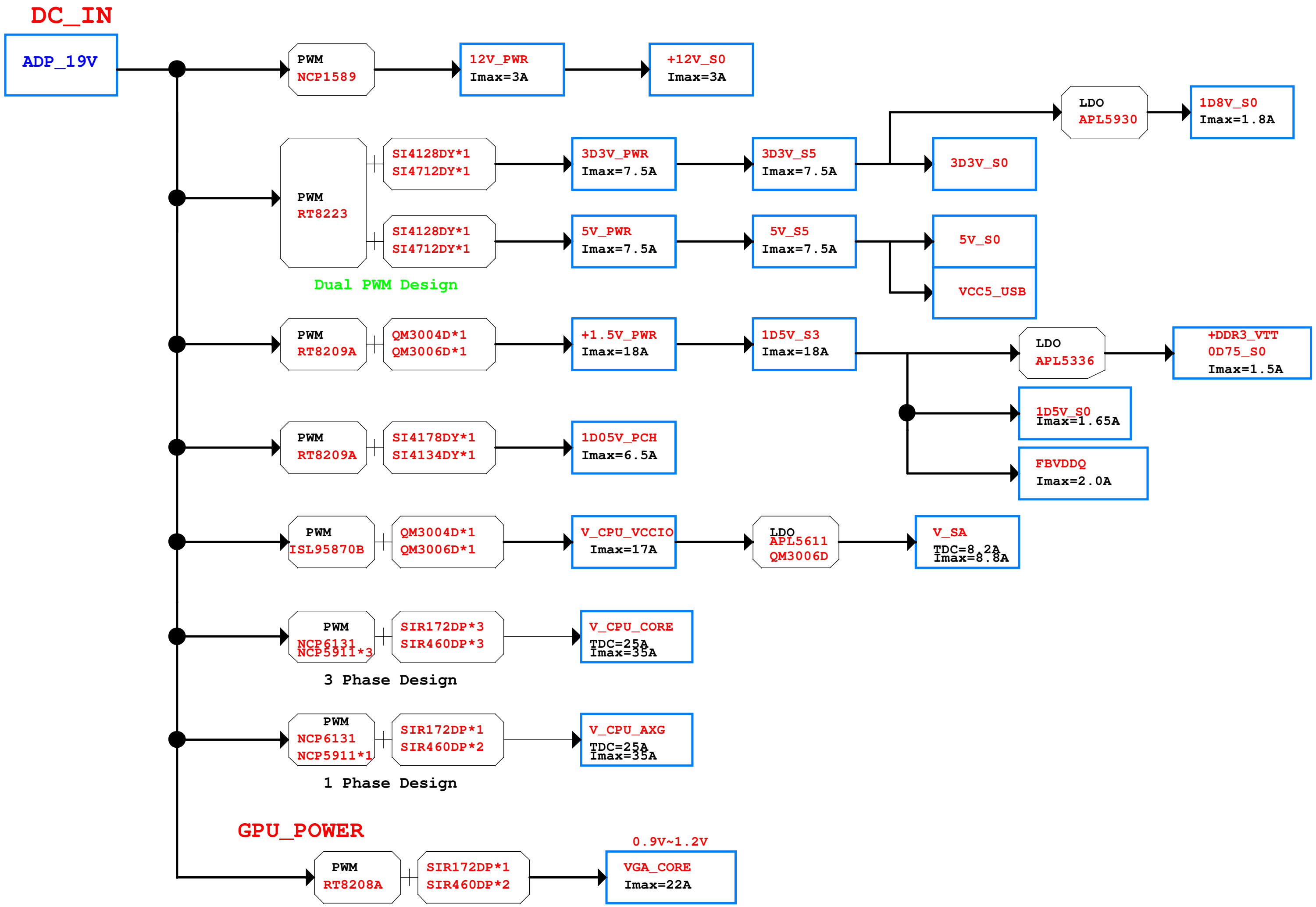
Title	Block Diagram	
Size: Custom	Document Number: Rosa_Eagleton	Rev: SA
Date: Monday, February 13, 2012	Sheet 2 of 53	



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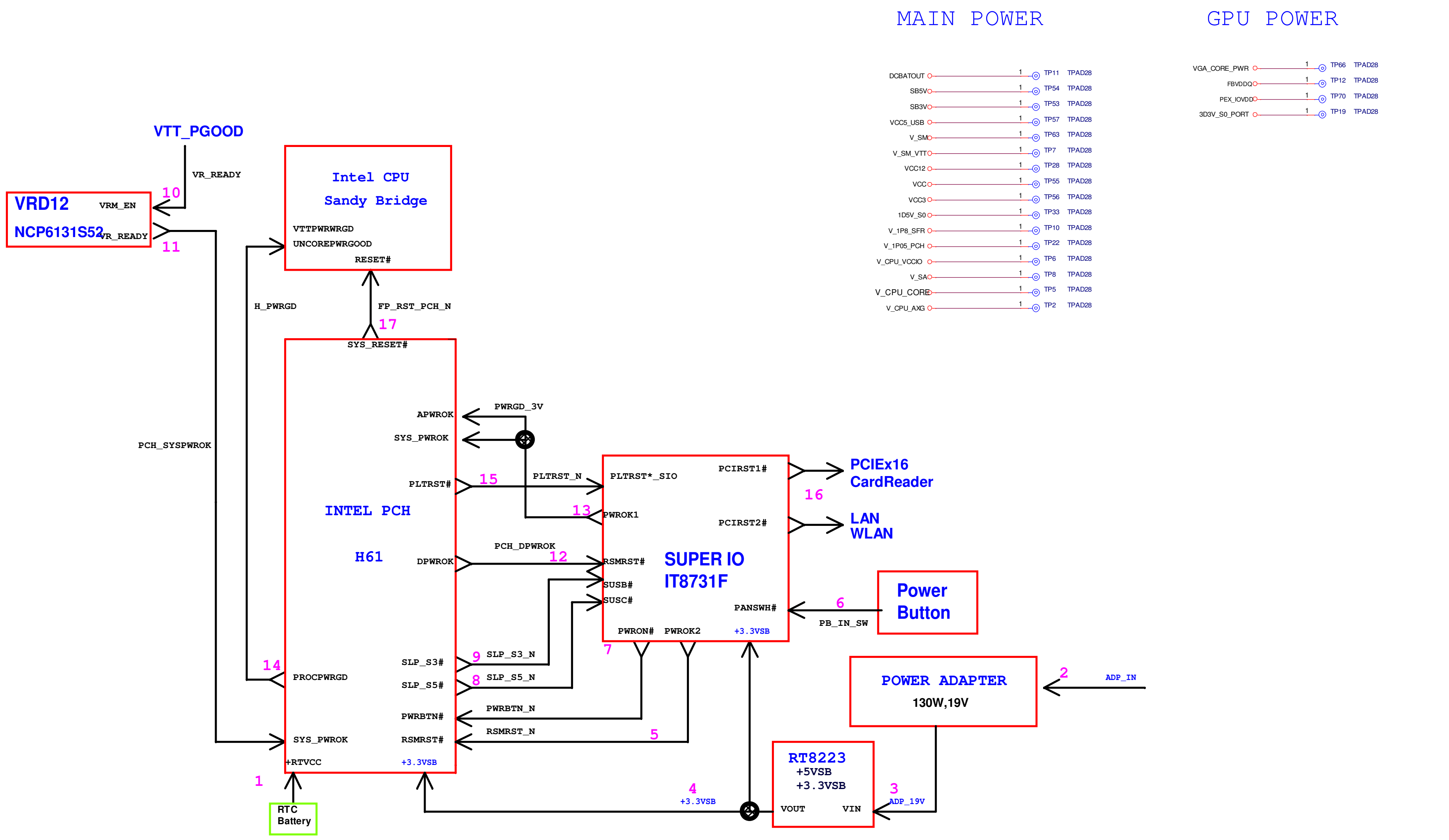
Title	Power Delivery	
Size C	Document Number Rosa_Eagleton	Rev SA
Date: Monday, February 13, 2012	Sheet 3 of 53	



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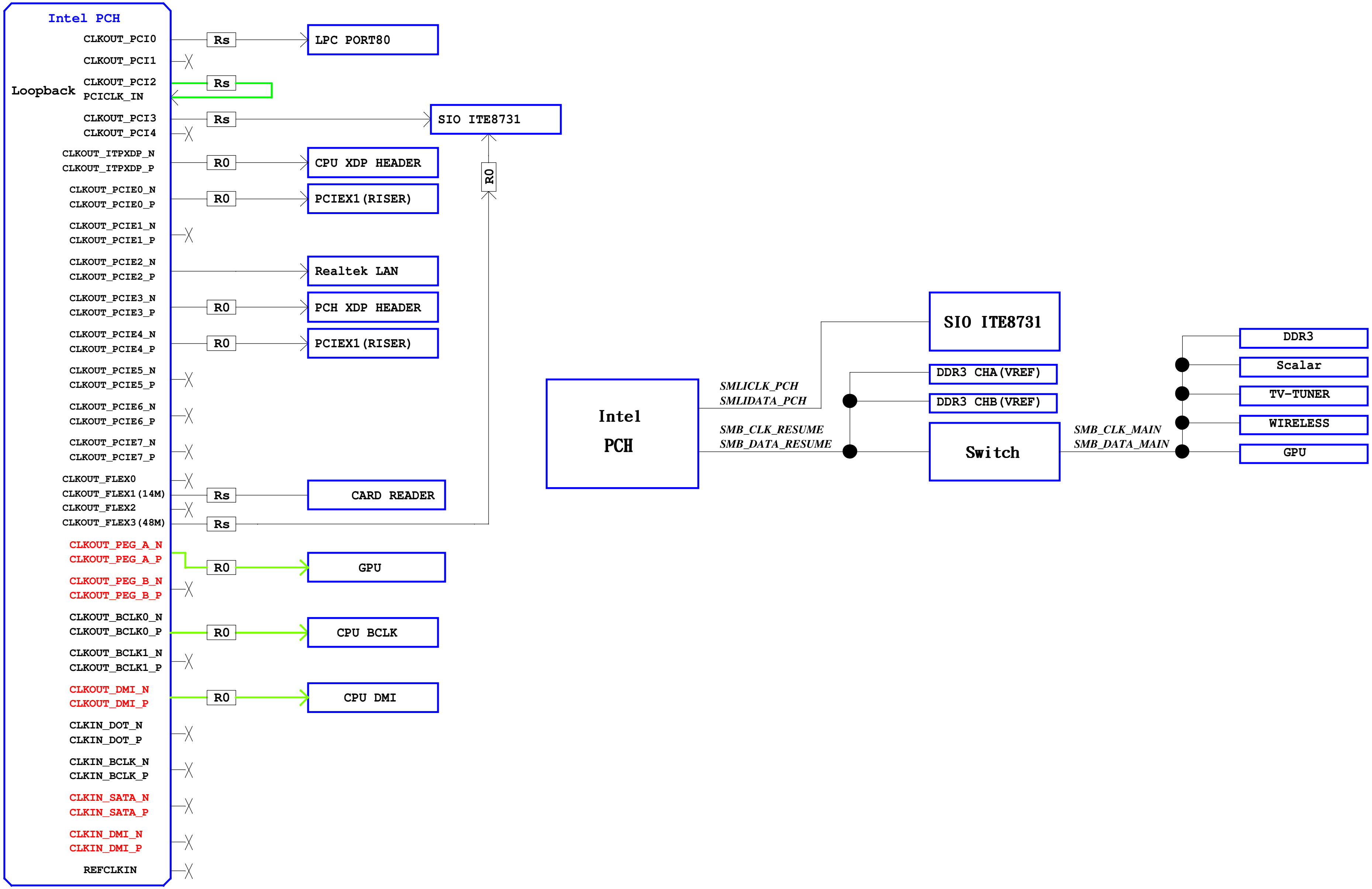
Hsichih, Taipei

Title: Power Good & Reset Diagram		
Size: C	Document Number: Rosa_Eagleton	Rev: SA
Date: Monday, February 13, 2012	Sheet 4 of 53	



Note: Red Color is Gen2 spec.
Note: R0 is 0 ohm optional resister
Note: Rs is serie resister
Note: Green Color is direct-parallel option

<Variant Name>

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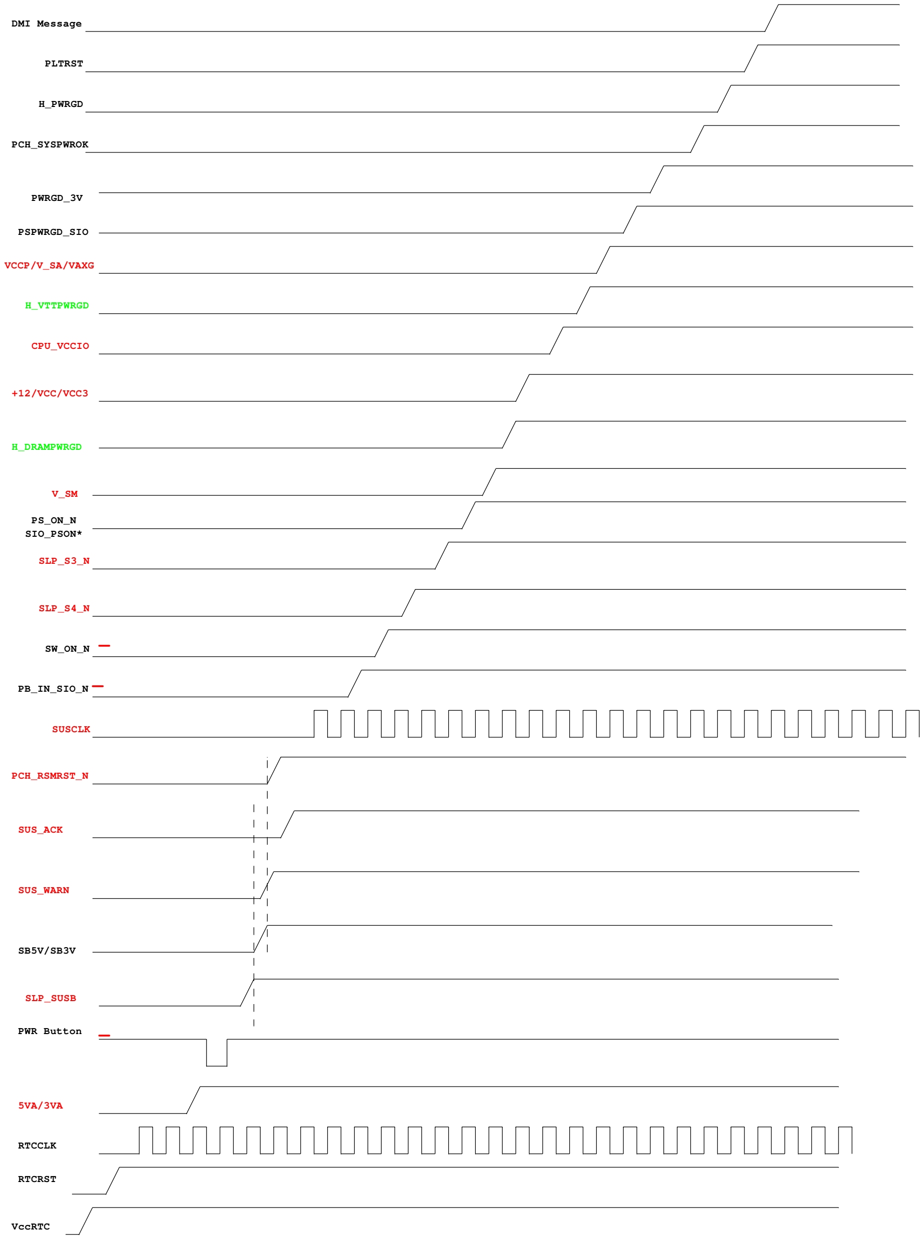
Title	Clock Diagram		
Size C	Document Number Rosa_Eagleton		Rev SA
Date: Monday, February 13, 2012		Sheet 5 of 53	

POWER ON SEQUENCE



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wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	Power Sequence	
Size D	Document Number Rosa_Eagleton	Rev SA
Date:	Monday , February 13, 2012	Sheet 6 of 53

<Variant Name>

wistron	**Wistron Incorporated** 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	TBD
Size B	Document Number Rosa_Eagleton	Rev SA
Date: Monday, February 13, 2012	Sheet 7 of 53

PCH (H61)

PIN NAME	PIN#	POWER WELL	USAGE(Sherwood)	USAGE(Eagleton)	Default value	BIOS Post Value	Notes
GPIO0	AW55	MAIN	PECI_REQ_N	PECI_REQ_N	GPI	no use	no use
GPIO1	BR19	MAIN	TACH1	PANEL_SEL1_CABLE_PCH	GPI	GPI	Panel select, input Please reference follow "PANEL_SEL_TAB"
GPIO2	BN9	MAIN	P_INTE_N	P_INTE_N	GPI	no use	no use
GPIO3	AV9	MAIN	P_INTF_N	P_INTF_N	GPI	no use	no use
GPIO4	BT15	MAIN	P_INTG_N	P_INTG_N	GPI	no use	no use
GPIO5	BR4	MAIN	P_INTH_N	P_INTH_N	GPI	no use	no use
GPIO6	BA22	MAIN	TACH2	PANEL_SEL2_CABLE_PCH	GPI	GPI	Panel select, input Please reference follow "PANEL_SEL_TAB"
GPIO7	BR16	MAIN	TACH3	PANEL_SEL3_CABLE_PCH	GPI	GPI	Panel select, input Please reference follow "PANEL_SEL_TAB"
GPIO8	BP51	RESUME	IO_SMI_N	SUSLED_PCH	GPO	GPO	LED control, output GPIO8, GPIO13 need control at the same time Default: High, High(Orange); Boot OK: Low, Low(White)
GPIO9	BJ41	RESUME	USB_OC5_R_N	USB_OC5_R_N	Native	no use	no use
GPIO10	BT45	RESUME	PW_CLEAR	PW_CLEAR	Native	GPI	Clear Password, input Default: High, Low: Clear PASSWORD
GPIO11	BN49	RESUME	LPC_PME_N	LPC_PME_N	Native	LPC_PME_N	Default: High, Low: enable PME
GPIO12	BK50	RESUME	PC_MODE	IO_SMI_N	Native	IO_SMI	Default: High, Low:enable SMI
GPIO13	BA25	RESUME	AV_MODE	PCH_PWRSW_LED	GPI	GPO	LED control, output GPIO8, GPIO13 need control at the same time High, High: Orange; Low, Low :White
GPIO14	BM45	RESUME	ME_CNTL	ME_CNTL	Native	GPO	ME_CNTL, output Default :High Enable ME, Low: Disable ME
GPIO15	BM55	RESUME	TLS_EN	TLS_EN	GPO	no use	no use
GPIO16	AU56	MAIN	BOARD_A	BOARD_A	GPI	GPI	input, BOARD_ID_A
GPIO17	BT17	MAIN	TACH0	TACH0	GPI	no use	no use
GPIO19	AY52	MAIN	SATA1GP	SATA1GP	GPI	no use	no use
GPIO20	AV43	MAIN	BOARD_ID_0	BOARD_ID_0(TP)	Native	no use	no use
GPIO21	BC54	MAIN	BOARD_B	BOARD_B	GPI	GPI	input, BOARD_ID_B
GPIO22	BA53	MAIN			GPI	no use	no use
GPIO23	BA20	MAIN	LPC_DRQ1_N	LPC_DRQ1_N	Native	no use	no use
GPIO24	BP53	RESUME	SUSLED*	H_SKTOCC_R_N	GPO	GPI	SKTOCC, input, Deafult: High, Low: CPU plug in
GPIO27	BJ43	Deep Sleep Power Well	PCH_GP27_PU	PCH_GP27_PU	GPO	no use	no use
GPIO28	BJ55	RESUME	PCH_GP28_PU	PCH_GP28_PU	GPI	no use	no use
GPIO29	BH49	RESUME	H_SKTOCC_R_N	TP_SLP_LAN(TP)	GPI	no use	no use
GPIO30	BU46	Deep Sleep Power Well	SUS_WARNB	SUS_WARNB	Native	SUS_WANB Function	SUS_WARNB function
GPIO31	BG43	Deep Sleep Power Well	PCH_GP31_PU	PCH_GP31_PU	GPI	no use	no use
GPIO32	BC56	MAIN	SMBUS_ISP	SMBUS_ISP	GPO	GPO	Firmware update, output, Default : Low, High: update Scalar FW
GPIO33	BC25	MAIN	BOARD_C	BOARD_C	GPO	GPI	input, BOARD_ID_C
GPIO34	BL56	MAIN	ADAPTOR_PSID	ADAPTOR_PSID	GPI	GPI	ADAPTOR_PSID, input
GPIO35	BJ57	MAIN	AUD_SPKMUTE*	PCH_AUD_MUTE	GPO	GPO	AUD_SPKMUTE, output, Default High, Low: Audio Mute
GPIO36	BB55	MAIN	SATA2GP	SATA2GP	GPI	no use	no use
GPIO37	BG53	MAIN	SATA3GP	SATA3GP	GPI	no use	no use
GPIO38	BE54	MAIN	LVDS_DET*	LVDS_DET*	GPI	GPI	LVDS_DET, Input, Default: High: no pulg, Low:plug in
GPIO39	BF55	MAIN	INV_DET*	INV_DET*	GPI	GPI	INV_DET, Input, Default: High: no pulg, Low:plug in
GPIO40	BD41	RESUME	USB_OC1_R_N	USBOC23*	Native	OC fucntion	USB port 2.3.4 OC fucntion
GPIO41	BG41	RESUME	USB_OC2_R_N	USB_OC2_R_N	Native	no use	no use
GPIO42	BK43	RESUME	USB_OC3_R_N	USB_OC3_R_N	Native	no use	no use
GPIO43	BP43	RESUME	USB_OC4_R_N	USB_OC4_R_N	Native	no use	no use
GPIO44	BL54	RESUME	LANCLK_REQ_N	LANCLK_REQ_N	Native	LANCLK_REQ_N function	LANCLK_REQ_N
GPIO45	AV44	RESUME	AVBOARD_DETECT		Native	no use	no use
GPIO46	BP55	RESUME	PC_STATUS		Native	no use	no use
GPIO48	AW53	MAIN	W1_DETECT_N	W1_DETECT_N	GPI	GPI	W1_detect, input Default:High: no pulg, Low:plug in
GPIO49	BA56	MAIN	MPCIE_DISABLE_N	MPCIE_DISABLE_N	GPI	GPO	W_disable, Output, Default: High, Enable; Low: Disable
GPIO50	BT5	MAIN	P_REQ_N1	P_REQ_N1	Native	no use	no use
GPIO51	AV8	MAIN	P_GNT_N1	P_GNT_N1	Native	no use	no use
GPIO52	BK8	MAIN	P_REQ_N2	P_REQ_N2	Native	no use	no use
GPIO53	BU12	MAIN	P_GNT_N2	P_GNT_N2	Native	no use	no use
GPIO54	AV11	MAIN	P_REQ_N3	P_REQ_N3	Native	no use	no use
GPIO55	BE2	MAIN	P_GNT_N3	P_GNT_N3	Native	no use	no use
GPIO57	BT53	RESUME	CAMERA_EN		GPI	no use	no use
GPIO58	BJ46	RESUME	SMLICLK_PCH	SMLICLK_PCH	Native	SMLICLK1 function	SMLICLK1 function
GPIO59	BM43	RESUME	USB_OC0_R_N	USBOC01*	Native	OC fucntion	USB port 0.1 OC fucntion
GPIO60	BU49	RESUME	SMLALERT_PCH	SMLALERT_PCH	Native	SMLALERT0 function	SMLALERT0 function
GPIO61	BN54	RESUME	SUS_STAT_N	SUS_STAT_N	Native	no use	no use

GPIO61	BN54	RESUME	SUS_STAT_N	SUS_STAT_N	Native	no use	no use
GPIO62	BA47	RESUME	SUSCLK	SUSCLK	Native	no use	no use
GPIO63	BH50	RESUME	SLP_S5_N	SLP_S5_N	Native	SLP_S5 function	SLP_S5 function
GPIO64	AT9	MAIN	CLKOUTFLEX0	CLKOUTFLEX0	Native	no use	no use
GPIO65	BA5	MAIN	CLKOUTFLEX1	CLKOUTFLEX1	Native	Card Reader_48MHz	CK_48M_CR
GPIO66	AW5	MAIN	CLKOUTFLEX2	CLKOUTFLEX2	Native	no use	no use
GPIO67	BA2	MAIN	CK_24M_FLEX	CK_24M_FLEX	Native	SIO_48MHz_CLK	CK_48M_SIO2
GPIO68	BU16	MAIN	TACH4	IR_DET	GPO	GPI	IR_DET, Input, Default: High: no pulg, Low:plug in
GPIO69	BM18	MAIN	TACH5	WEBCAM_DET	GPO	GPI	WEBCAM_DET, Input Default: High: no pulg, Low:plug in
GPIO70	BN17	MAIN	TV_EN	TV_EN	Native	GPO	TV_EN, Output, Default: High Enable, Low: Disable
GPIO71	BP15	MAIN	TP_DET	TP_DET	Native	GPI	TP_DET, Input, Default: High: no pulg, Low:plug in
GPIO72	AV46	RESUME			GPO	no use	no use
GPIO74	BR46	RESUME	SML1ALERT_PCH	SML1ALERT_PCH	Native	SMLALERT1 functione	SMLALERT1 function
GPIO75	BK46	RESUME	SMLIDATA_PCH	SMLIDATA_PCH	Native	SMLIDATA1 function	SMLIDATA1 function

"High-Z" Tri-state. Ibex Peak not driving the signal high or low.

"High" Ibex Peak is driving the signal to a logic 1.

"Low" Ibex Peak is driving the signal to a logic 0.

"Defined" Driven to a level that is defined by the function or external pull-up/pull-down resistor (will be high or low).

"Undefined" Ibex Peak is driving the signal, but the value is indeterminate.

"Running" Clock is toggling or signal is transitioning because function not stopping.

"Off" The power plane is off; Ibex Peak is not driving when configured as an output or sampling when configured as an input.

Joey different older

Eagleton ciferent Sherwood

ITE8731

GPIO#	Mux Function	Default Function	Default Status	BIOS Post Function	BIOS output type	USAGE	Notes
GP10	PCIRST3#/GP10	PCIRST3#	DO8	Power LED	DIOD8	LEDVCC	Power LED (White), Low active GP10.GP40 need low at the same time
GP11	PCIRST2#/GP11	PCIRST2#	DO8	PCIRST2#	DO8	PCIRST2#	PCIRST reset (LAN,WLAN)
GP12	PCIRST1#/GP12	PCIRST1#	DO8	PCIRST1#	DO8	PCIRST1#	PCIRST reset(GPU,CardReader)
GP13	PWROK1/GP13	PWROK1	DOD8	PWROK1	DIOD8	PWROK3_1	VCC3 power GOOD
GP14	PCH_C1/SVC_O/GP14	SVC_O	DOD8	PCH_C1	DIOD8	SMLICLK_PCH	SMbus function
GP15	SVD_O/PCIRSTIN#/CIRTX2/GP15	SVD_O	DOD8	no use		SIO_PCIRSTIN#	pull hgih
GP16	FAN_TAC4/CIRRX2/GP16	FAN_TAC4	DI	CIRRX2	DI	SIO_CIRRX1	IR Remote
GP17	RI2#/GP17	RI2#	DI	no use			
GP20	CTS2#/GP20	CTS2#	DI	no use			
GP21	DCD2#/GP21	DCD2#	DI	no use			
GP22	SCK/GP22	SCK	DO9	SCK	DO8	SIO_SCK_R	SIO SPI ROM clock
GP23	SI/GP23	SI	DIOD8	SI	DO8	SIO_SI	SIO SPI ROM Data
GP24	RTS2#/GP24	RTS2#	DO8	no use			
GP25	DSR2#/GP25	DSR2#	DI	no use			
GP26	SOUT2/GP26	SOUT2#	DO8	SOUT2#	DO8	SIO_UART1_TX	UART TX to Scalar
GP27	SIN2/GP27	SIN2	DI	SIN2	DI	SIO_UART1_RX	UART RX to Scalar
GP30	ATXPG/GP30	ATXPG	DI	no use	DI	SIO_ATXPG	pull high
GP31	CORE_TYPE/GP31	CORE_TYPE	DI	no use			
GP32	SVD_I/GP32	SVD_I	DI	no use			
GP33	SVC_I/GP33	SVC_I	DI	EUP_EN	DIOD8	CTRL0	High to close 3.3V/5V SB power (High Active)
GP34	GP34	GP34	DIOD8	SLP_SUSB	DIOD8	SLP_SUSB	SLP_SUSB functon
GP35	GP35	GP35	DIOD8	SUS_WARNB	DIOD8	SUS_WARNB_R	SUS_WARNB function
GP36	FAN_CTL3/GP36	FAN_CTL3	DO8	no use	DO8	TP_FAN_CTL3	Test Point
GP37	FAN_TAC3/GP37	FAN_TAC3	DI	no use	DI	TP_FAN_TAC3	Test Point
GP40	3VSBSW#/GP40	3VSBSW#	DOD8	SUS_LED	DIOD8	LED_O	SUS LED(Orange), High Active GP10.GP40 need high at the same time
GP41	PWROK2/GP41	PWROK2	DOD8	RSMRST	DIOD8	RSMRST_SIO_N_1	RSMRST
GP42	PSON#/GP42	PSON#	DOD8	PSON#	DOD8	SIO_PSON_N	Enable VCC12 control IC (Low:active)
GP43	PANSWH#/GP43	PANSWH#	DI	PANSWH#	DI	PB_IN_SW	Input,PWRBTN control,Default:High,Low:enable system
GP44	PWRON#/GP44	PWRON#	DOD8	PWRON#	DOD8	PWRBTN_N	output,default:High,Low: enable PCH PWBTN
GP46	D_RX0/SMBCLK2/GP46/IRRX	GP46	DIOD8	no use	DIO8	SMBCLK2_SIO	Pull high
GP47	D_TX0/SMBDAT2/IRTX/GP47	IRTX	DO8	no use	DIO8	TP_SMBDAT2_SIO	Test Point
GP50	SO/GP50	SO	DI	SO	DI	SIO_SO	SIO SPI ROM SO
GP51	FAN_CTL2/GP51	FAN_CTL2	DOD8	no use			
GP52	FAN_TAC2/GP52	FAN_TAC2	DI	IO_SMI	DIOD8	IO_SMI_N	IO_SMI_N
GP53	SUSC#/GP53	SUSC#	DI	SUSC#	DI	SLP_S5_SIO	SLP S5
GP54	PME#/GP54	PME#	DOD8	PME#	DOD8	LPC_PME_N	LPC_PME_N
GP55	RSMRST#/CIRRX1/GP55	RSMRST#	DOD8	DPWROK	DIOD8	PCH_DPWROK	DPWROK(PCH-->SIO)
GP56	MCLK/GP56	MCLK	DIOD24	no use	DIOD24	MCLK	Pull high
GP57	MDAT/GP57	MDAT	DIOD24	no use	DIOD24	MDAT	Pull high
GP60	KCLK/GP60	KCLK	DIOD24	no use	DIOD24	KBCLK	Pull high
GP61	KDAT/GP61	KDAT	DIOD24	no use	DIOD24	KDAT	Pull high
GP62	KRST#/GP62	KRST#	DO8	no use	DO8	KBRST_N	Connect to PCH
GP63	GP63	GP63	DIOD8	GPO	DIOD8	SUS_PWR_ACK_R	SUS_ACK function
GP70	GP70	GP70	DIOD24	GPO	DIOD24	SIO_PROCHOT_R_N	CPU PROCHOT#
GP71	GP71	GP71	DIOD24	GPO	DIOD24	CTRL1	Hight to close PCH 3.3V AUX power (High active)
GP72	GP72	GP72	DIOD24	GPO	DIOD24	OSD_MUTE	OSD Mute function
GP73	GP73	GP73	DIOD24	GPO	DIOD24	VOLBTN_UP	Input ,VOLBTN control,Default:High,Low: VOLBTN_UP

<Variant Name>

wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	GPIO TABLE	
Size C	Document Number Rosa_Eagleton	Rev SA
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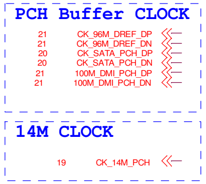

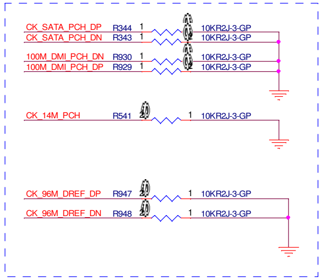

Terminate PCH CLK Inputs

Remove CLK GEN
Use PCH Internal CLK

<Variant Name>

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Title: CLOCK GEN - ICS9LRS4180

Size	Document Number	Rev
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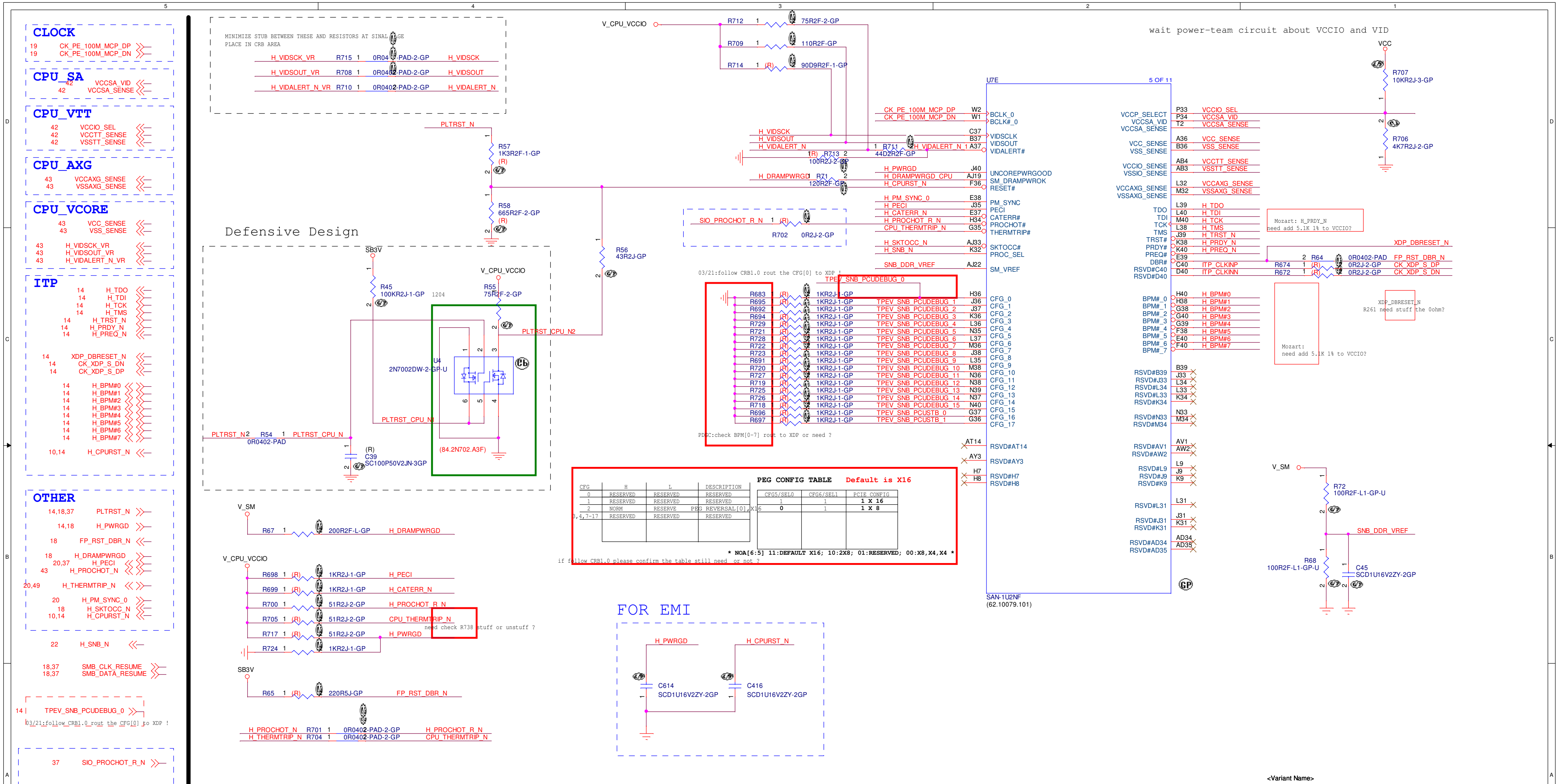

<Variant Name>

Wistron Incorporated
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Hsichih, Taipei

Title: CPU LGA 1155_1

Size	Document Number	Rev
Custom	Rosa_Eagleton	SA

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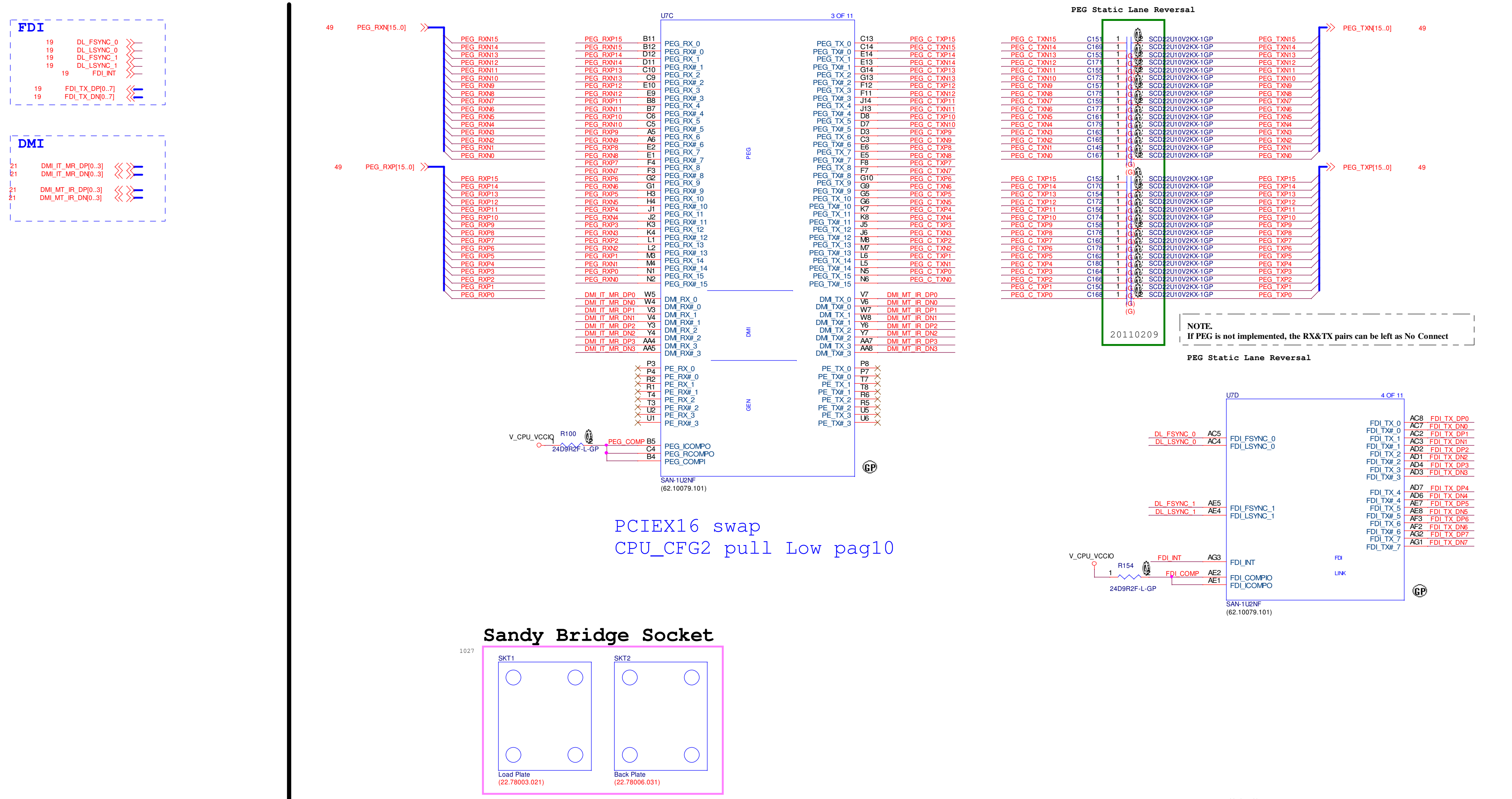

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wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	CPU LGA 1155_2	
Size: Custom	Document Number: Rosa_Eagleton	Rev: SA
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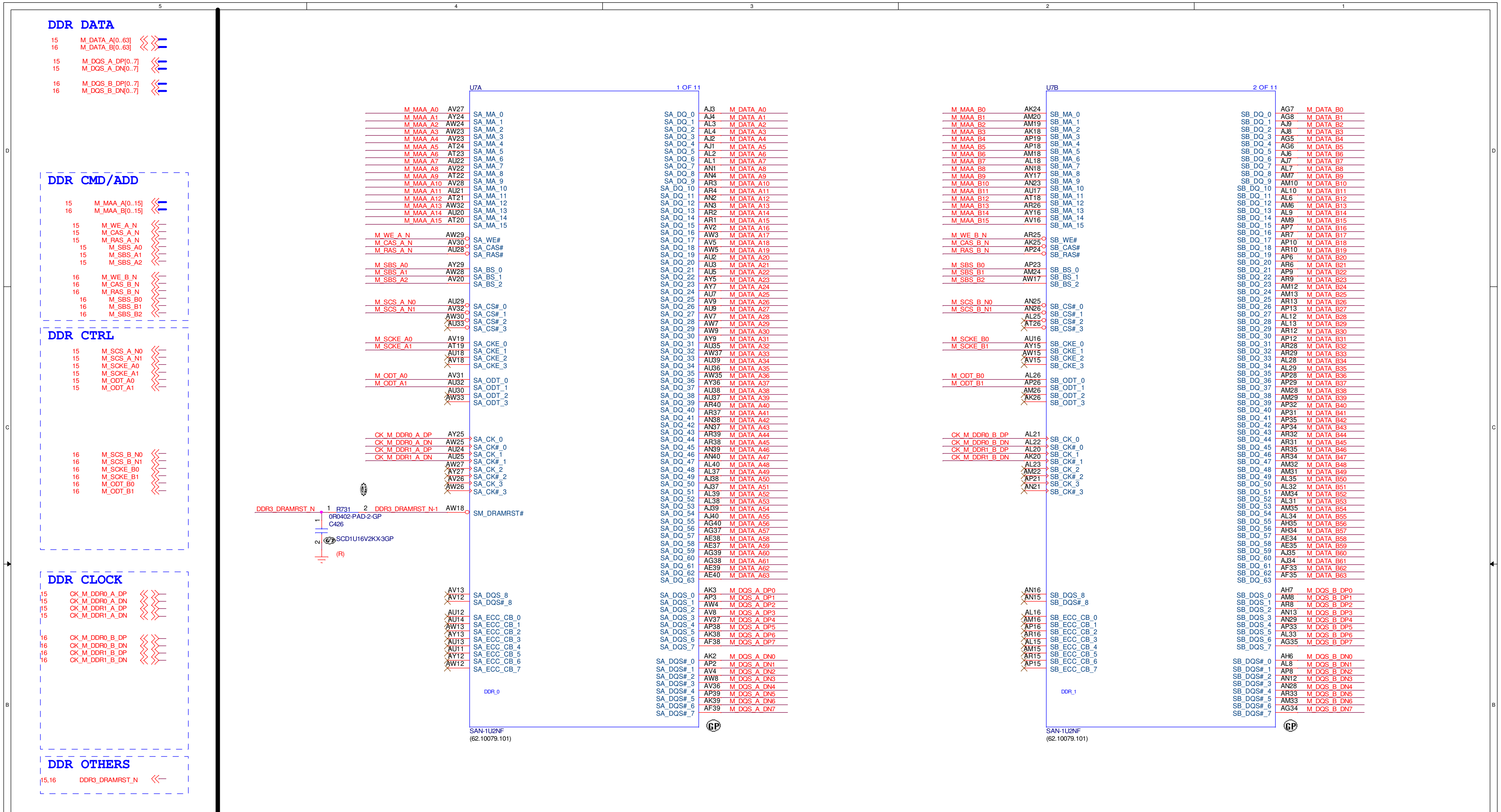

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU LGA 1155_3

Size	Document Number	Rev
C	Rosa_Eagleton	SA

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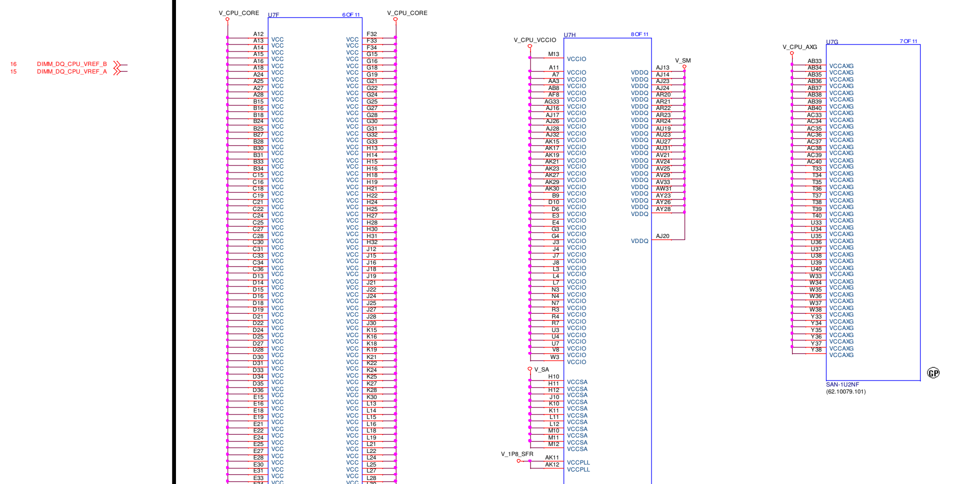
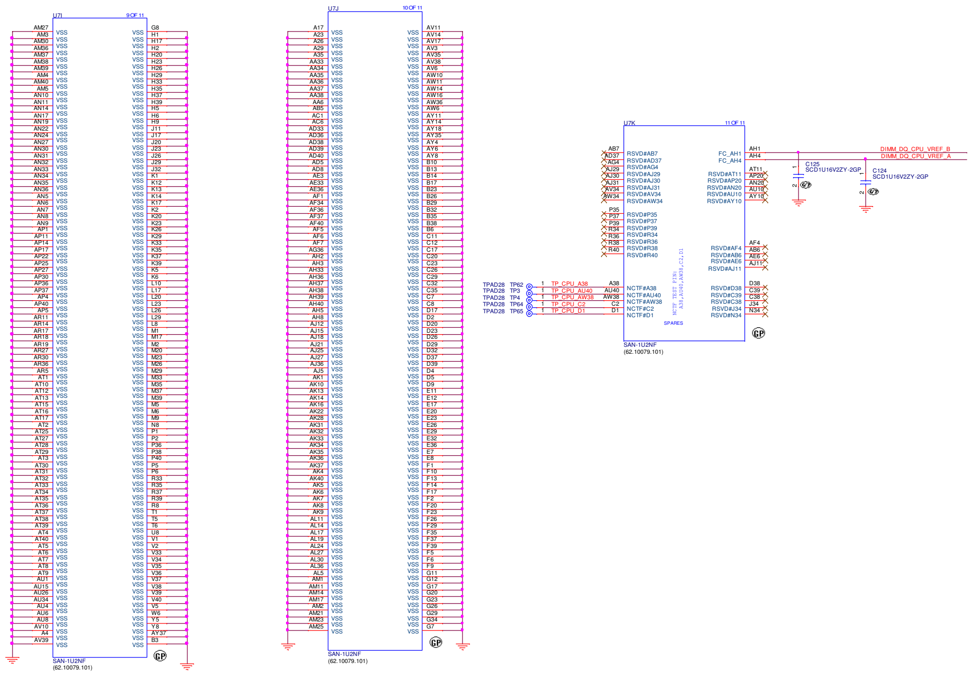
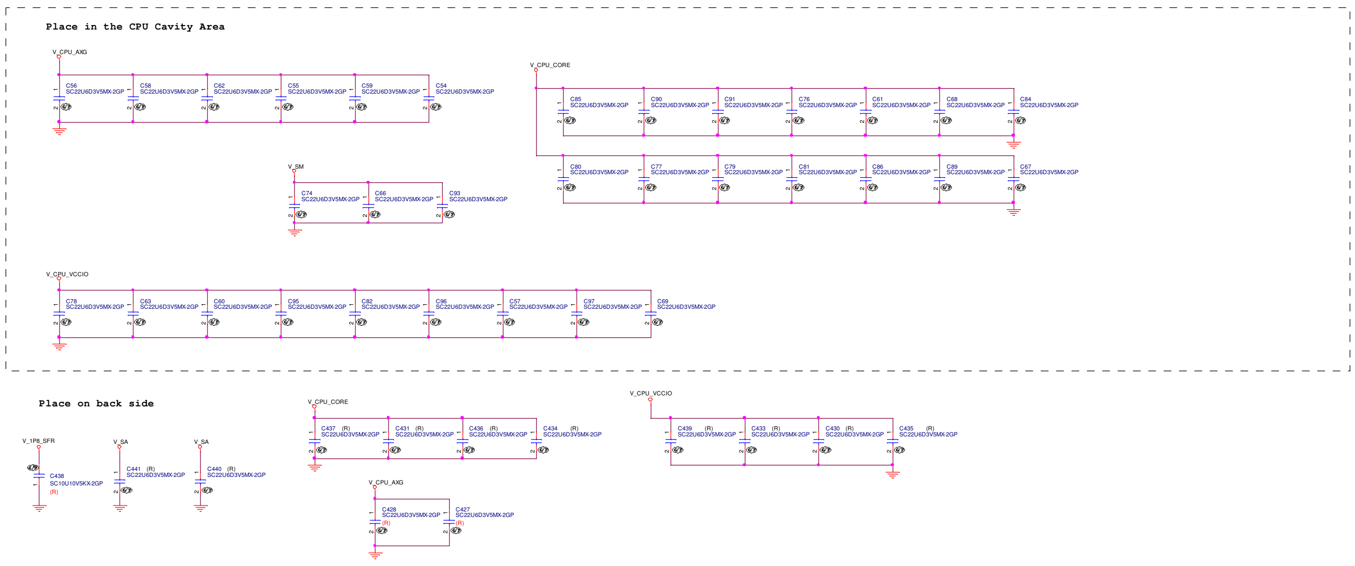




CPU Power Capacitor Quantity

Net	CAP	AMOUNT
Vcore	22uf 0805	14+4
VCCIO	22uf 0805	9+16(R)
V_AXG	22uf 0805	4+2(R)
VCCSA	10uf 0805	2+0
VDDQ	22uf 0805	9
VCCPLL	10uf 0805	1



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CPU LGA 1155_4		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title		
Size D	Document Number Rosa_Eagleton	Rev SA
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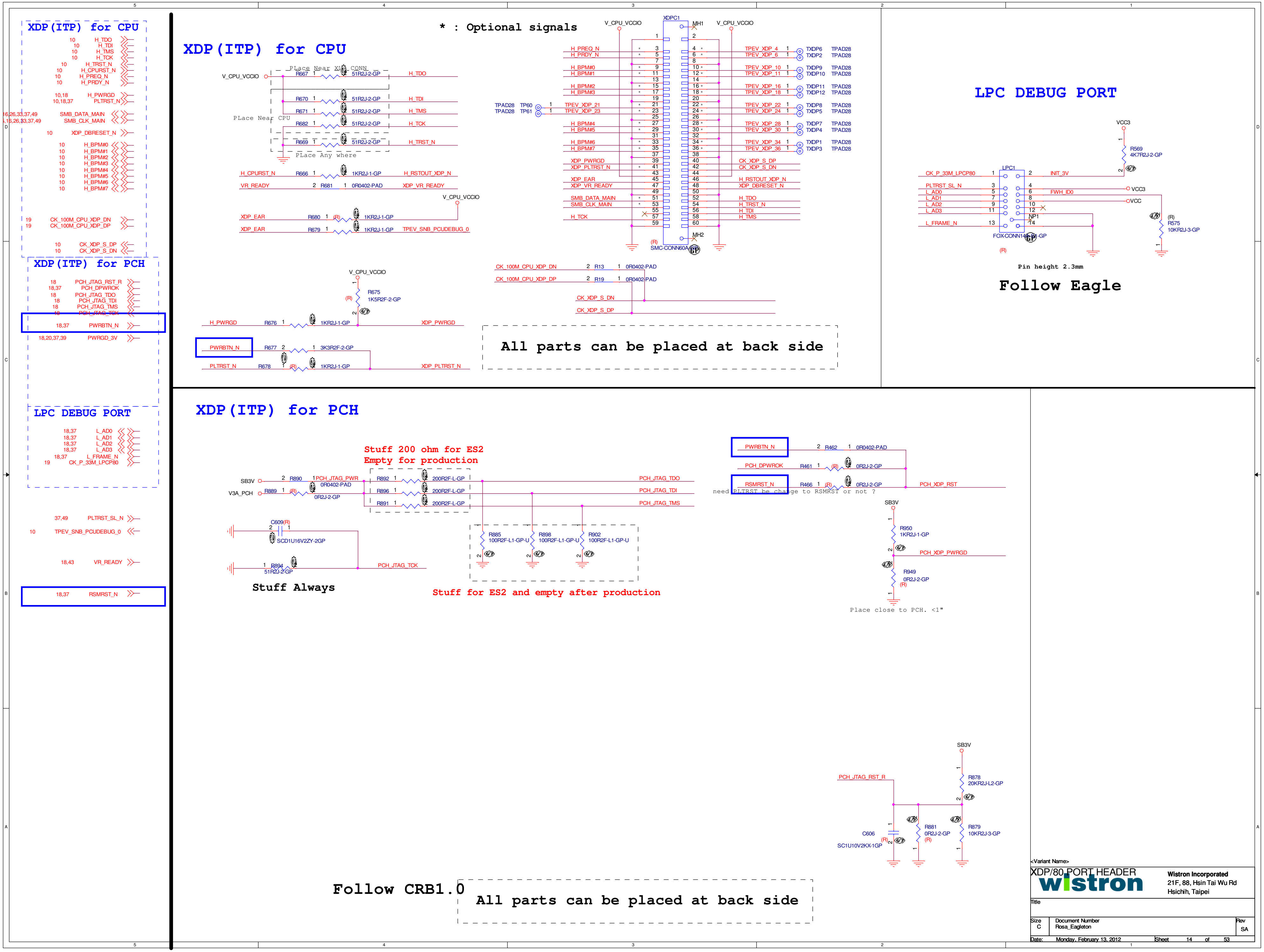
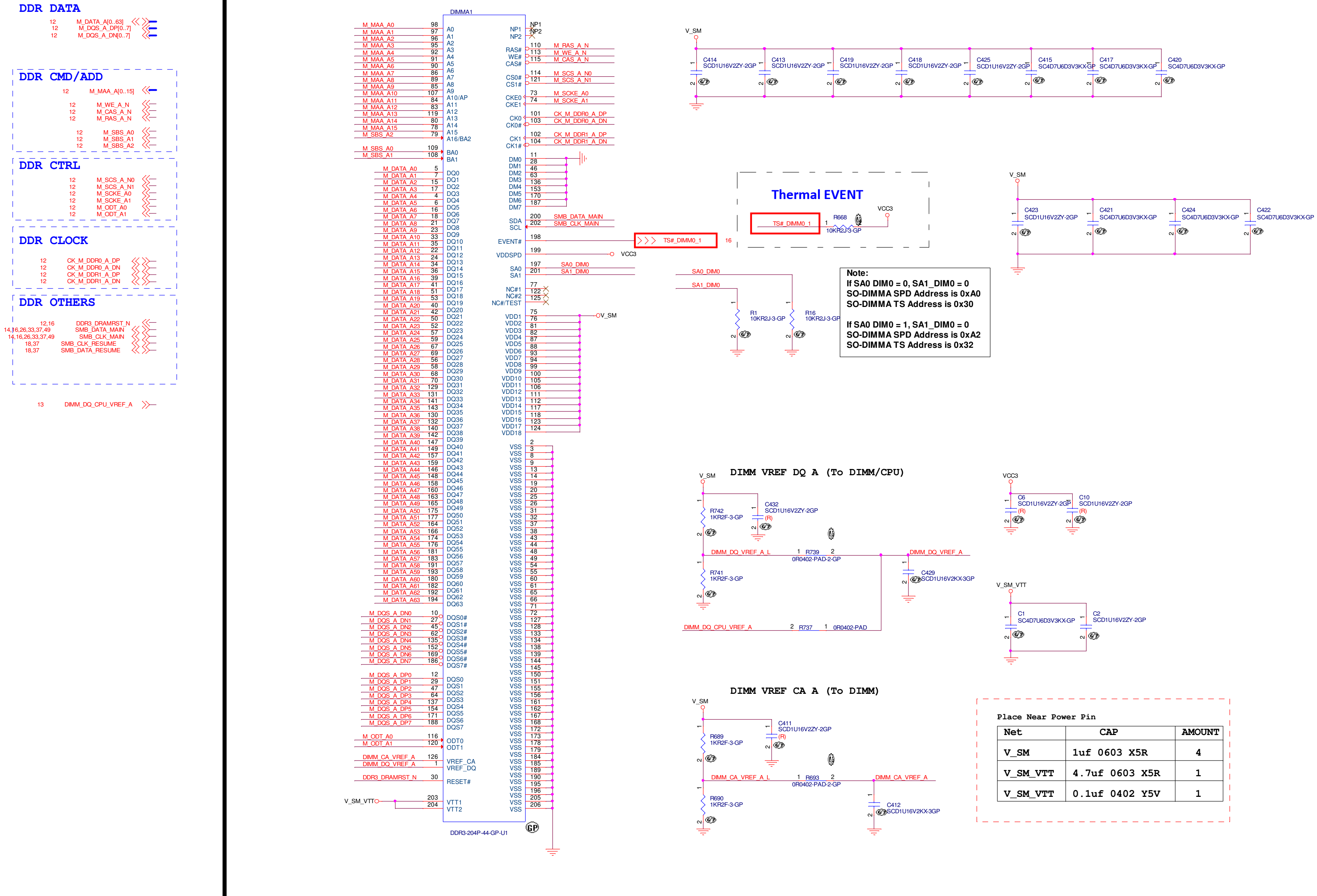

XDP (ITP) for CPU
* : Optional signals
XDP (ITP) for CPU
PLace Near XDP CONN
PLace Near CPU
PLace Any where
LPC DEBUG PORT
Pin height 2.3mm
Follow Eagle
All parts can be placed at back side
XDP (ITP) for PCH
LPC DEBUG PORT
XDP (ITP) for PCH
Stuff 200 ohm for ES2
Empty for production
Stuff Always
Stuff for ES2 and empty after production
need PLTRST be change to RSMRST or not ?
Place close to PCH. <1"
Follow CRB1.0
All parts can be placed at back side
<Variant Name>
XDP/80 PORT HEADER
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
Size C
Document Number
Rosa_Eagleton
Rev SA
Date: Monday, February 13, 2012
Sheet 14 of 53



Place Near Power Pin

Net	CAP	AMOUNT
V_SM	1uf 0603 X5R	4
V_SM_VTT	4.7uf 0603 X5R	1
V_SM_VTT	0.1uf 0402 Y5V	1

<Variant Name>

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Title	DIMM_A	
Size C	Document Number Rosa_Eagleton	Rev SA
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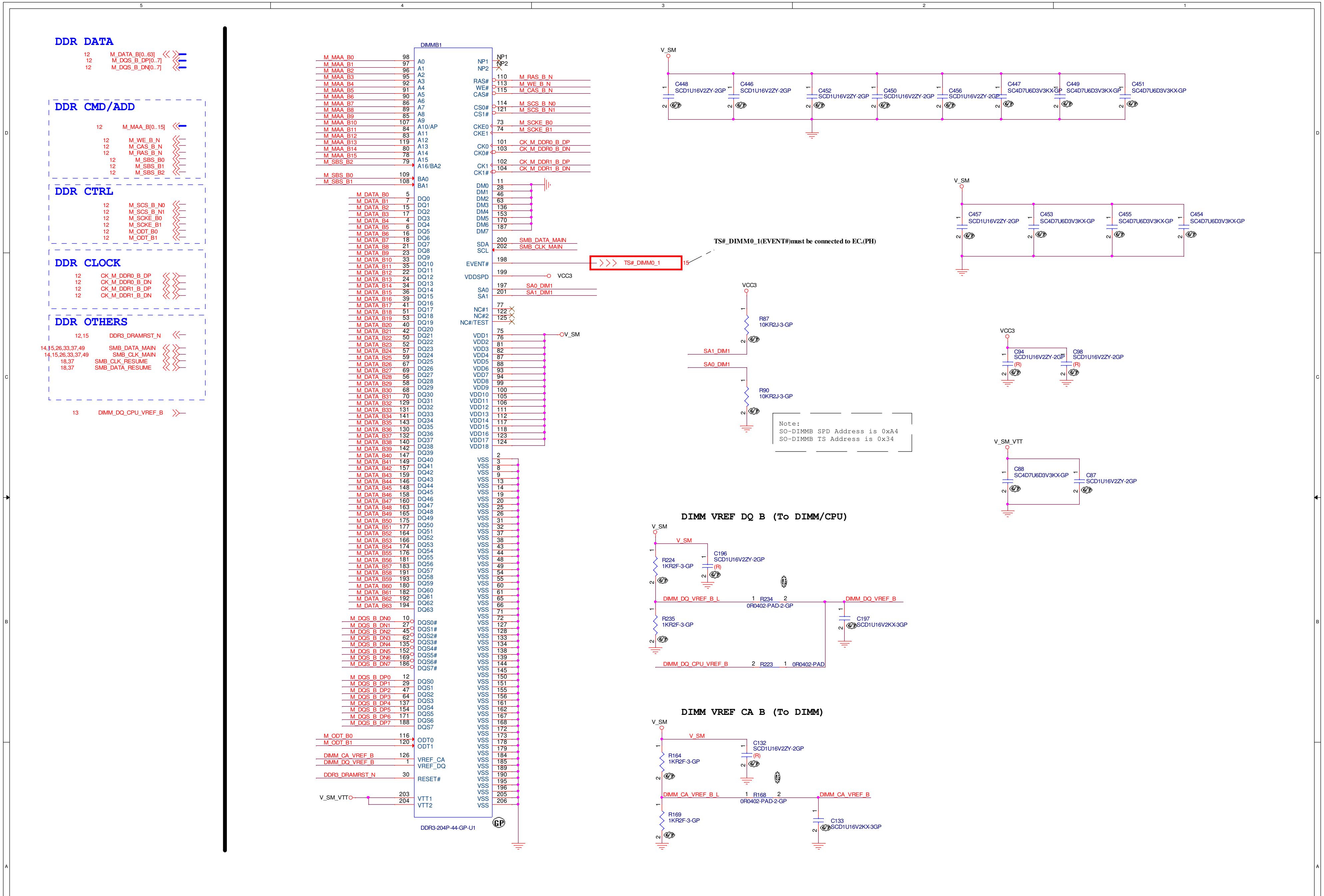

<Variant Name>

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Title	DIMM_B
Size	C
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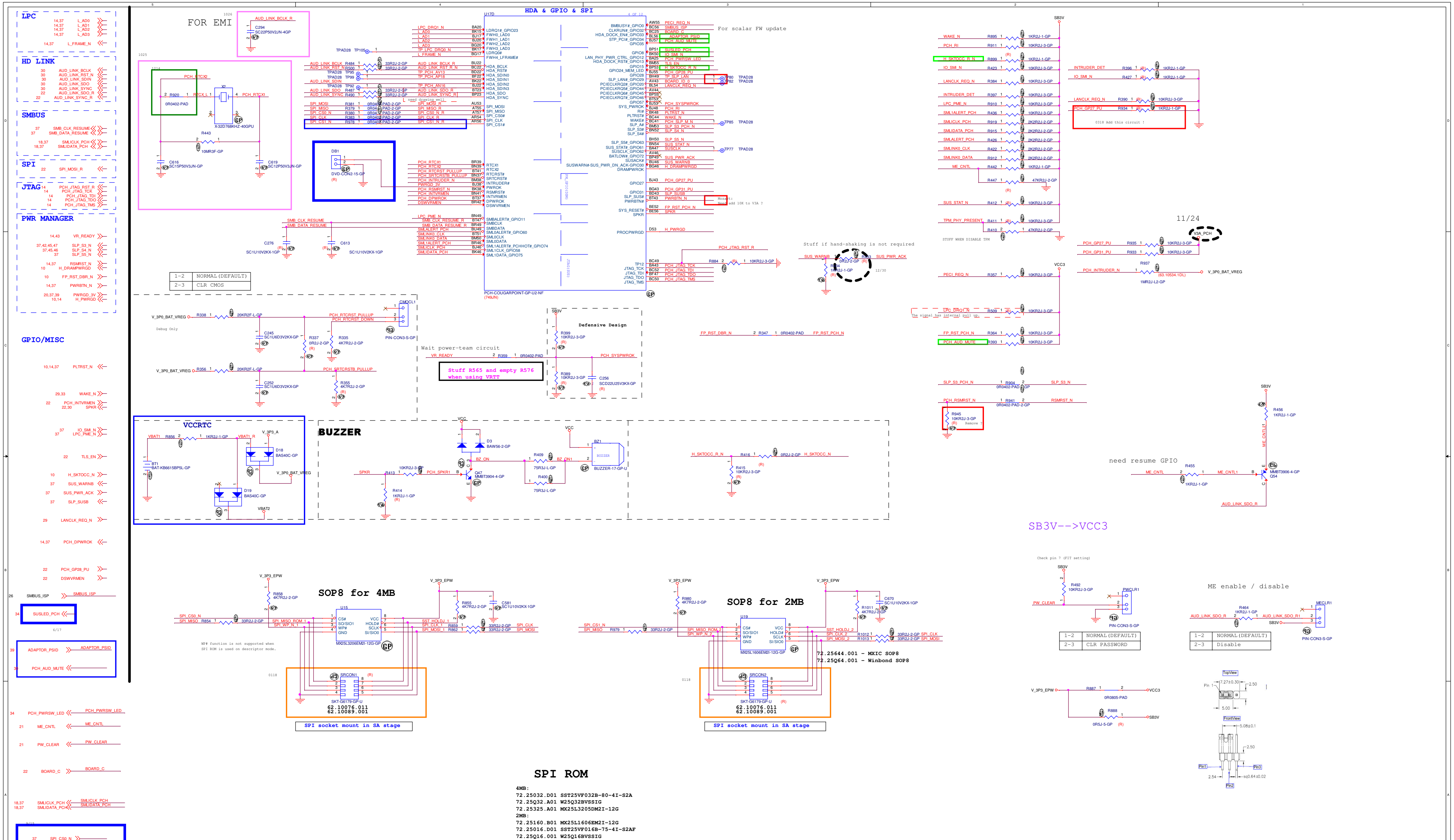
Remove Channel B, DIMM1

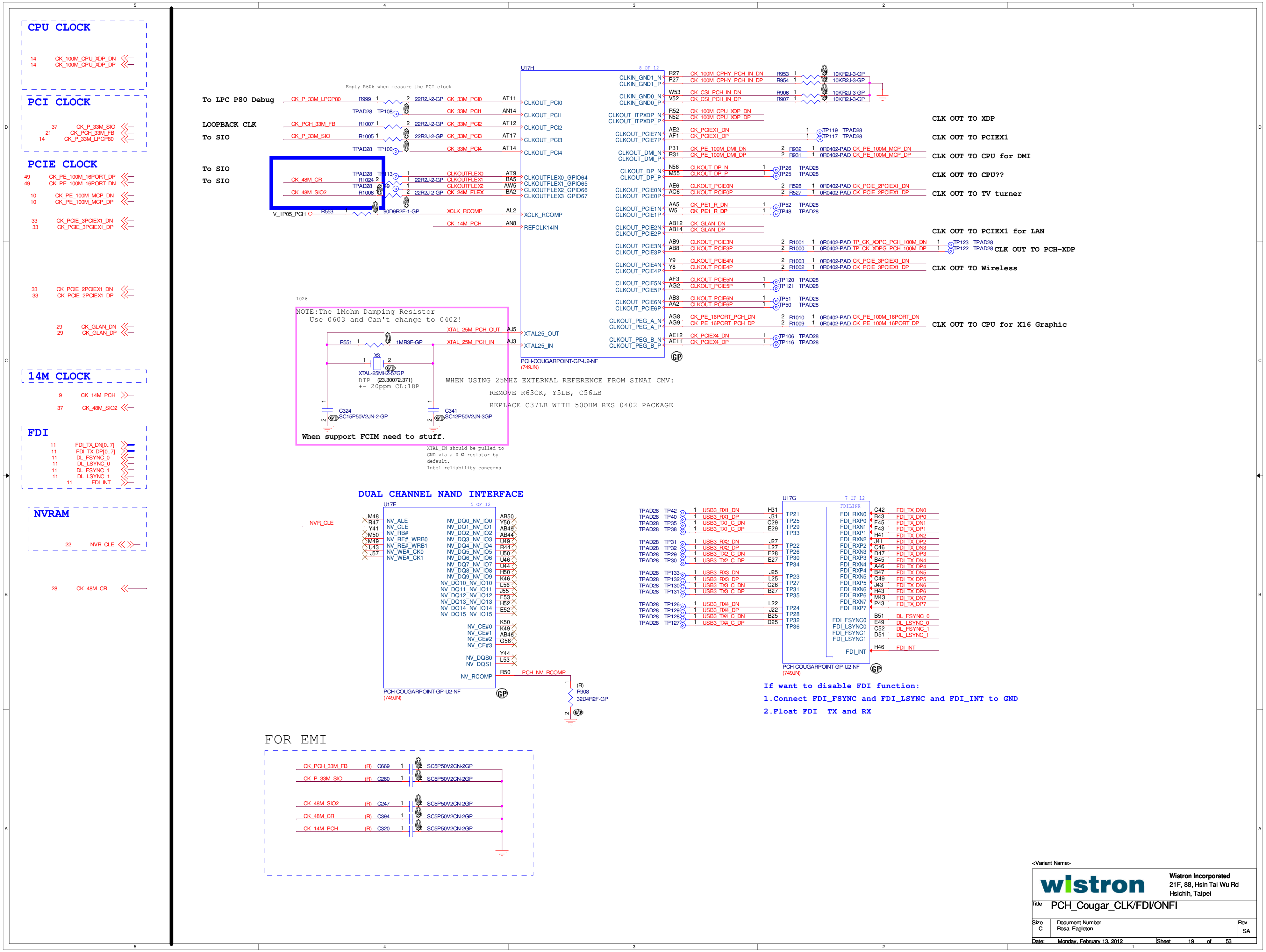


SPI ROM

4MB:
72.25032.D01 SST25VF032B-80-4I-S2A
72.25Q32.A01 W25Q32BVSSIG
72.25325.A01 MX25L3205DM2I-12G
2MB:
72.25160.B01 MX25L1606EM2I-12G
72.25016.D01 SST25VF016B-75-4I-S2AF
72.25Q16.001 W25Q16BVSSIG

<Variant Name>

wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	PCH_Cougar_AUDIO/GPIO
Size: D	Document Number: Rosa_Eagleton — Rev: SA
Date: Monday, February 13, 2012	Sheet 18 of 53


CPU CLOCK
CK_100M_CPU_XDP_DN
CK_100M_CPU_XDP_DP
PCI CLOCK
CK_P_33M_SIO
CK_PCH_33M_FB
CK_P_33M_LPCP80
PCIE CLOCK
CK_PE_100M_16PORT_DP
CK_PE_100M_16PORT_DN
CK_PE_100M_MCP_DN
CK_PE_100M_MCP_DP
CK_PCIE_3PCIEX1_DN
CK_PCIE_3PCIEX1_DP
CK_PCIE_2PCIEX1_DN
CK_PCIE_2PCIEX1_DP
CK_GLAN_DN
CK_GLAN_DP
14M CLOCK
CK_14M_PCH
CK_48M_SIO2
FDI
FDI_TX_DN[0..7]
FDI_TX_DP[0..7]
DL_FSYNC_0
DL_LSYNC_0
DL_FSYNC_1
DL_LSYNC_1
FDI_INT
NVRAM
NVR_CLE
CK_48M_CR
Empty R606 when measure the PCI clock
To LPC P80 Debug
LOOPBACK CLK
To SIO
To SIO
To SIO
U17H
CLKOUT_PCI0
CLKOUT_PCI1
CLKOUT_PCI2
CLKOUT_PCI3
CLKOUT_PCI4
CLKOUTFLEX0_GPIO64
CLKOUTFLEX1_GPIO65
CLKOUTFLEX2_GPIO66
CLKOUTFLEX3_GPIO67
XCLK_RCOMP
REFCLK14IN
XTAL25_OUT
XTAL25_IN
PCH-COUGARPOINT-GP-U2-NF
(749JN)
CLK OUT TO XDP
CLK OUT TO PCIEX1
CLK OUT TO CPU for DMI
CLK OUT TO CPU??
CLK OUT TO TV turner
CLK OUT TO PCIEX1 for LAN
CLK OUT TO PCH-XDP
CLK OUT TO Wireless
CLK OUT TO CPU for X16 Graphic
NOTE:The 1Mohm Damping Resistor
Use 0603 and Can't change to 0402!
XTAL-25MHZ-57GP
DIP (23.30072.371)
+- 20ppm CL:18P
WHEN USING 25MHZ EXTERNAL REFERENCE FROM SINAI CMV:
REMOVE R63CK, Y5LB, C56LB
REPLACE C37LB WITH 50OHM RES 0402 PACKAGE
When support FCIM need to stuff.
XTAL_IN should be pulled to GND via a 0-Ω resistor by default.
Intel reliability concerns
DUAL CHANNEL NAND INTERFACE
U17E
PCH-COUGARPOINT-GP-U2-NF
(749JN)
U17G
FDILINK
If want to disable FDI function:
1.Connect FDI_FSYNC and FDI_LSYNC and FDI_INT to GND
2.Float FDI TX and RX
FOR EMI
SC5P50V2CN-2GP
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Hsichih, Taipei
Title PCH_Cougar_CLK/FDI/ONFI
Size C
Document Number Rosa_Eagleton
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Date: Monday, February 13, 2012
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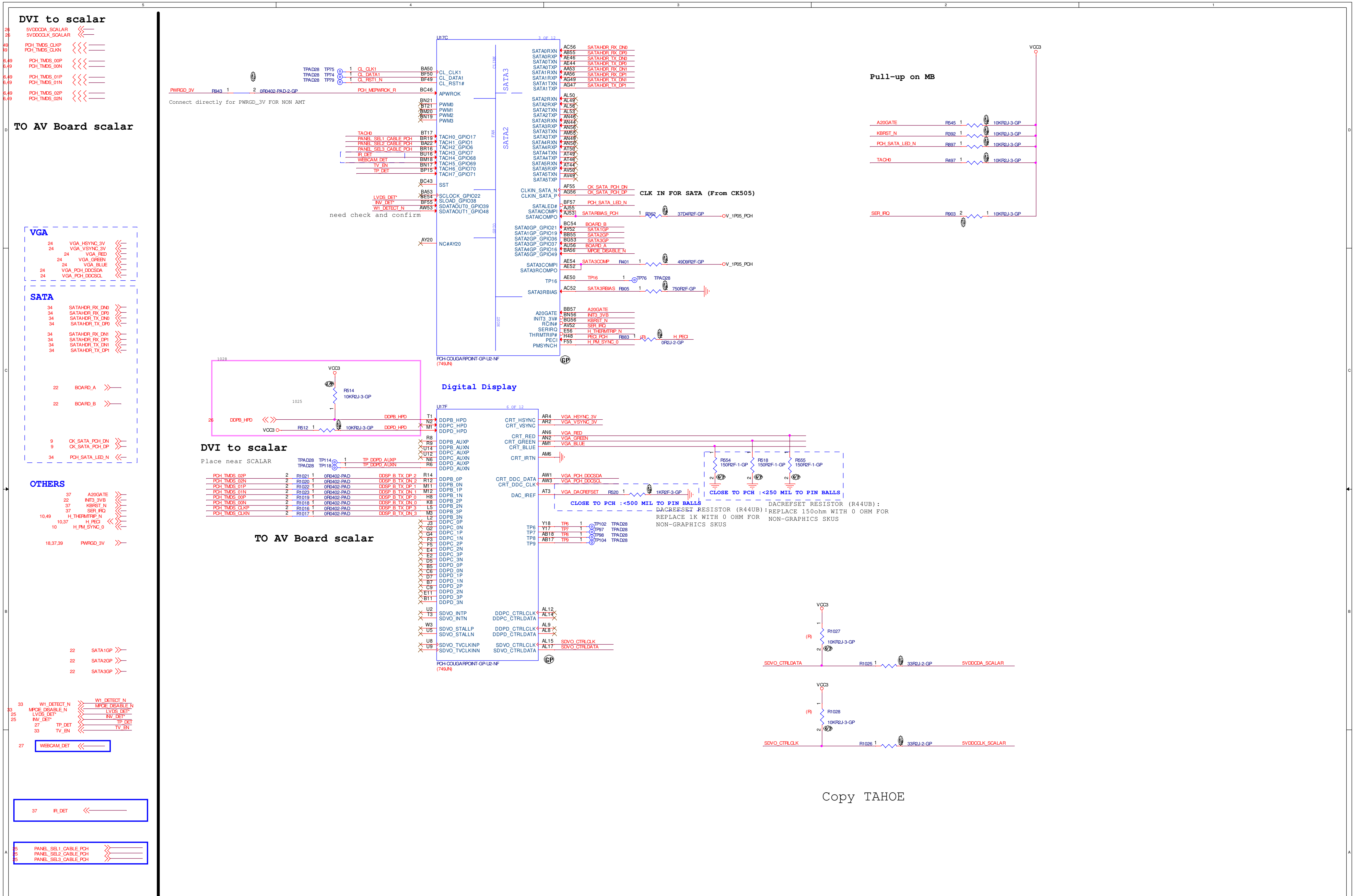

<Variant Name>

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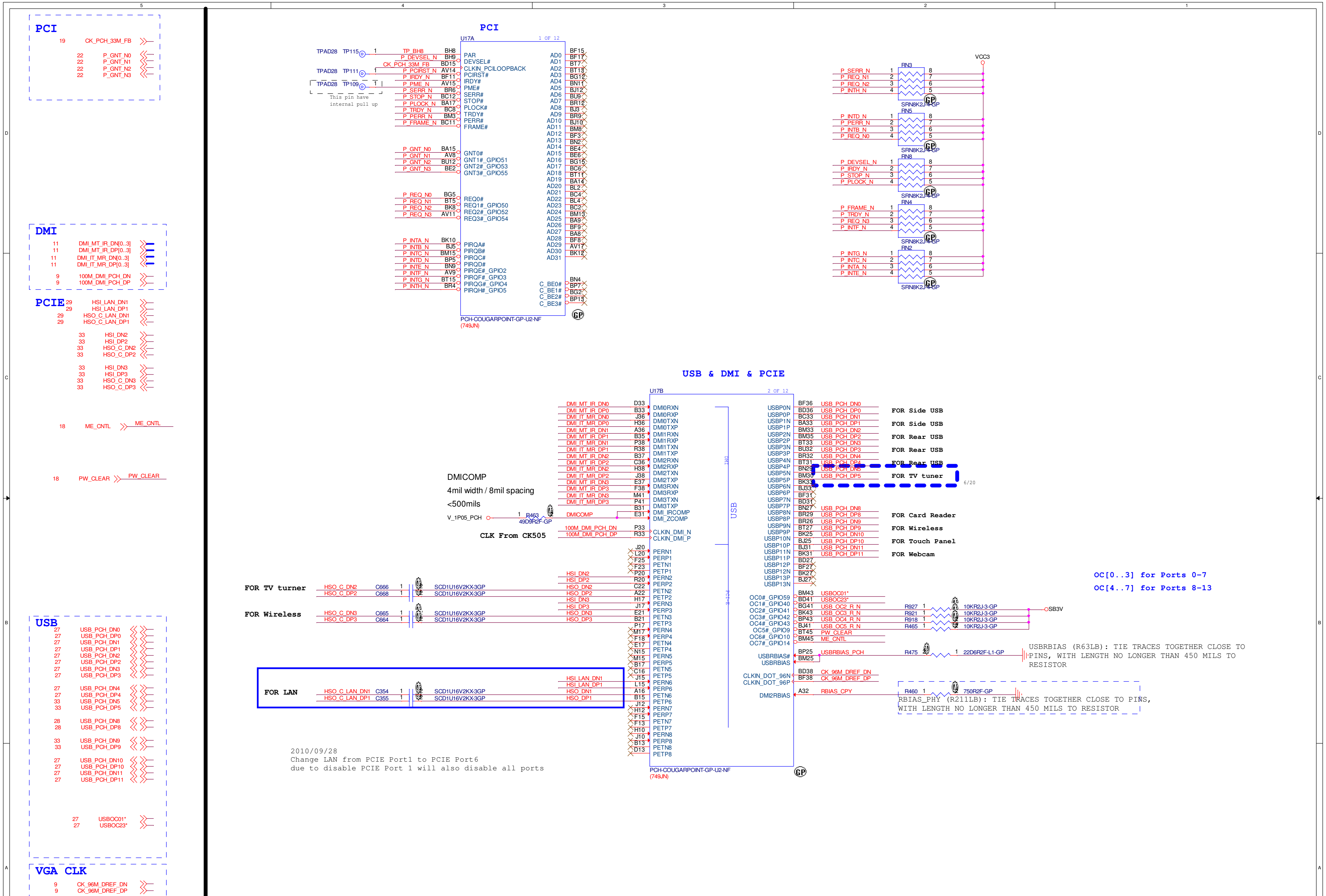
Title: PCH_Cougar_SATA/FAN/DP

Size: Custom | Document Number: Rosa_Eagleton | Rev: SA

Date: Monday, February 13, 2012 | Sheet 20 of 53



<Variant Name>

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Title	PCH_PCI/PCIE/DMI/USB	
Size C	Document Number Rosa_Eagleton	Rev SA
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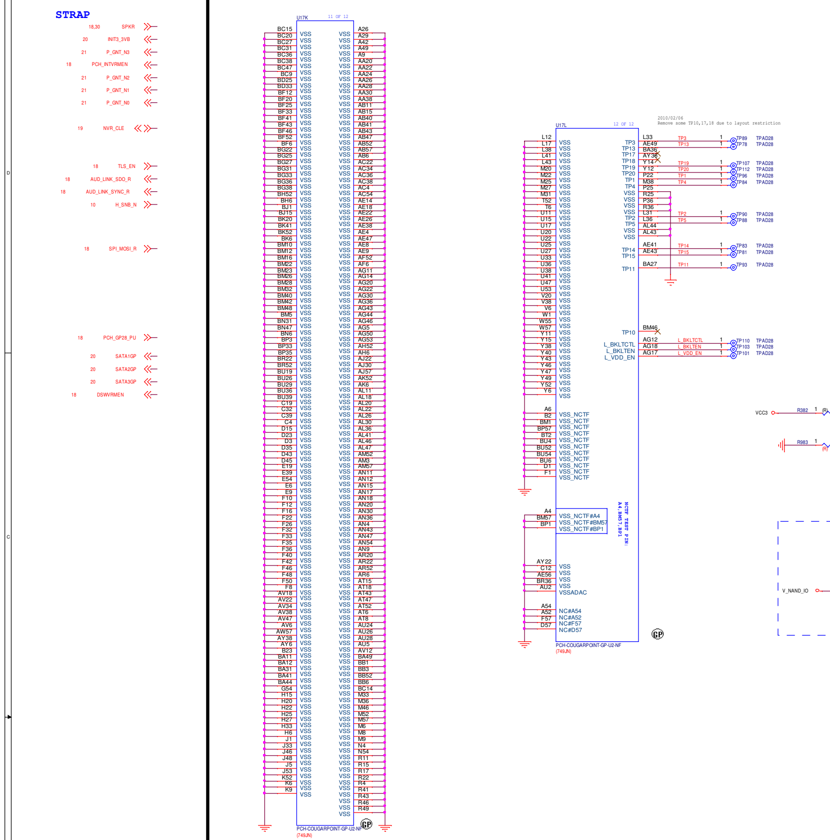
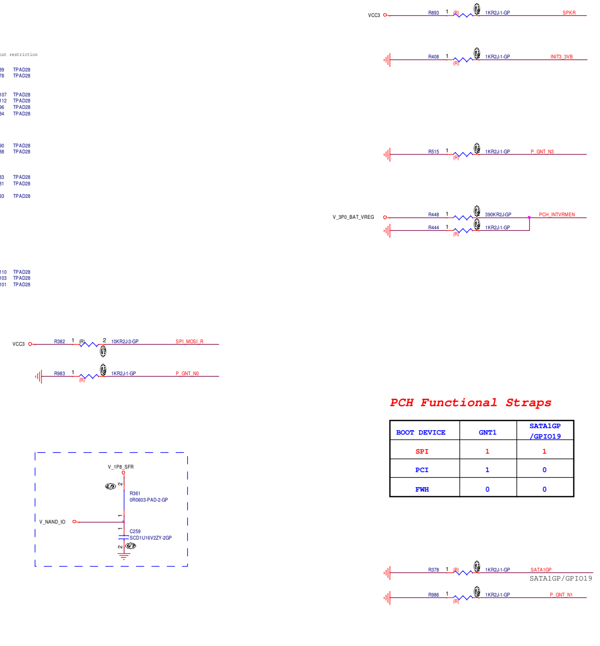




6' serial straping define

Table 2-27. Functional Strap Definitions (Sheet 1 of 5)

Signal	Usage	When Sampled	Comment
SPKR	No Reboot	Rising edge of PWROK	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Cougar Point will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers: Offset 3410h:Bit 5).
INIT3_3V#	Reserved	Rising edge of PWROK	This signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. **NOTE:** This signal should not be pulled low

Table 2-27. Functional Strap Definitions (Sheet 2 of 5)

Signal	Usage	When Sampled	Comment
GNT3# / GPIO55	Top-Block Swap Override	Rising edge of PWROK	The signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode (Cougar Point inverts A16 for all cycles targeting BIOS space). The status of this strap is readable via the Top Swap bit (Chipset Config Registers: Offset 3414h:Bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
INTVRMEN	Integrated 1.05 V VRM Enable / Disable	Always	Integrated 1.05 V VRMs is enabled when high **NOTE:** This signal should always be pulled high
GNT1#/ GPIO51/	Boot BIOS Strap bit 1 BBS1	Rising edge of PWROK	This Signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. This field determines the destination of accesses to the BIOS memory range. Also controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. Bit11 / Bit 10 / Boot BIOS Destination 0 / 1 / Reserved 1 / 0 / PCI 1 / 1 / SPI 0 / 0 / LPC **NOTE:** If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Cougar Point require SPI flash connected directly to the Cougar Point's SPI bus with a valid descriptor in order to boot. **NOTE:** Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® ME or Integrated GbE LAN. **NOTE:** PCI Boot BIOS destination is not supported on Mobile

Table 2-27. Functional Strap Definitions (Sheet 3 of 5)

Signal	Usage	When Sampled	Comment
SATA1GP/ GPIO19	Boot BIOS Strap bit 0 BBS0	Rising edge of PWROK	This Signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. This field determines the destination of accesses to the BIOS memory range. Also controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 / Bit 10 / Boot BIOS Destination 0 / 1 / Reserved 1 / 0 / PCI 1 / 1 / SPI 0 / 0 / LPC **NOTE:** If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Cougar Point require SPI flash connected directly to the Cougar Point's SPI bus with a valid descriptor in order to boot. **NOTE:** Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN. **NOTE:** PCI Boot BIOS destination is not supported on mobile.
GNT2#/ GPIO53	ESI Strap (Server Only)	Rising edge of PWROK	This Signal has a weak internal pull-up. **NOTE:** The internal pull-up is disabled after PLTRST# deasserts. Tying this strap low configures DMI for ESI compatible operation. **NOTE:** ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.

Signal	Usage	When Sampled	Comment
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	Rising edge of RSMRST#	Signal has a weak internal pull-down. If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default) If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up in manufacturing/debug environments ONLY. **NOTE:** The weak internal pull-down is disabled after PLTRST# deasserts. **NOTE:** Asserting the HDA_SDO high on the rising edge of RSMRST# will also halt Intel® Management Engine after chipset bringup and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug.
DF_TVS	DMI and FDI Tx/ Rx Termination Voltage	Rising edge of PWROK	This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts.
GPIO28	On-Die PLL Voltage Regulator	Rising edge of RSMRST# pin	This signal has a weak internal pull-up. **NOTE:** The internal pull-up is disabled after RSMRST# deasserts. The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select	Rising edge of RSMRST# pin	This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low.
GPIO15	TLS Confidentiality	Rising edge of RSMRST# pin	Low = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel ME Crypto TLS cipher suite with confidentiality This signal has a weak internal pull-down. **NOTE:** The weak internal pull-down is disabled after RSMRST# deasserts. **NOTE:** A strong pull-up may be needed for GPIO functionality **NOTE:** This signal must be pulled up to support Intel RPAT and Intel AMT with TLS. Intel ME configuration parameters also need to be set correctly to enable TLS.
L_DDC_DATA	LVDS Detected	Rising edge of PWROK	When '1'- LVDS is detected; When '0'- LVDS is not detected. This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts.

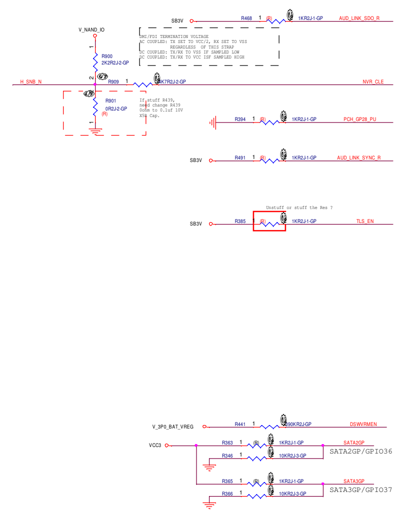
Table 2-27. Functional Strap Definitions (Sheet 5 of 5)

Signal	Usage	When Sampled	Comment
SDVO_CTRLDATA	Port B Detected	Rising edge of PWROK	When '1'- Port B is detected; When '0'- Port B is not detected This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts.
DDPC_CTRLDATA	Port C Detected	Rising edge of PWROK	When '1'- Port C is detected; When '0'- Port C is not detected This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts.
DDPD_CTRLDATA	Port D Detected	Rising edge of PWROK	When '1'- Port D is detected; When '0'- Port D is not detected This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts.
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable	Always	If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
SATA2GP/ GPIO36	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts. **NOTE:** This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts. **NOTE:** This signal should not be pulled high when strap is sampled.

NOTE: See Section 3.1 for full details on pull-up/pull-down resistors.

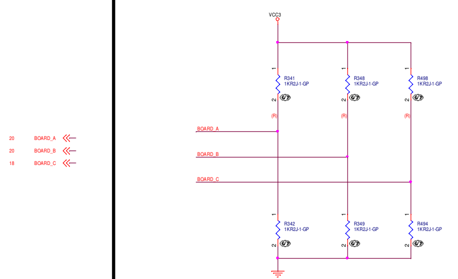
PCH Functional Straps

BOOT DEVICE	GNT1	SATA1GP /GPIO19
SPI	1	1
PCI	1	0
FWH	0	0



Board ID

Board_A/GPIO16	Board_B/GPIO21	Board_C/GPIO33	Note
0	0	0	GPU
0	0	1	UMA



<Variant Name>

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Title: PCH_Cougar_GND/STRAPS

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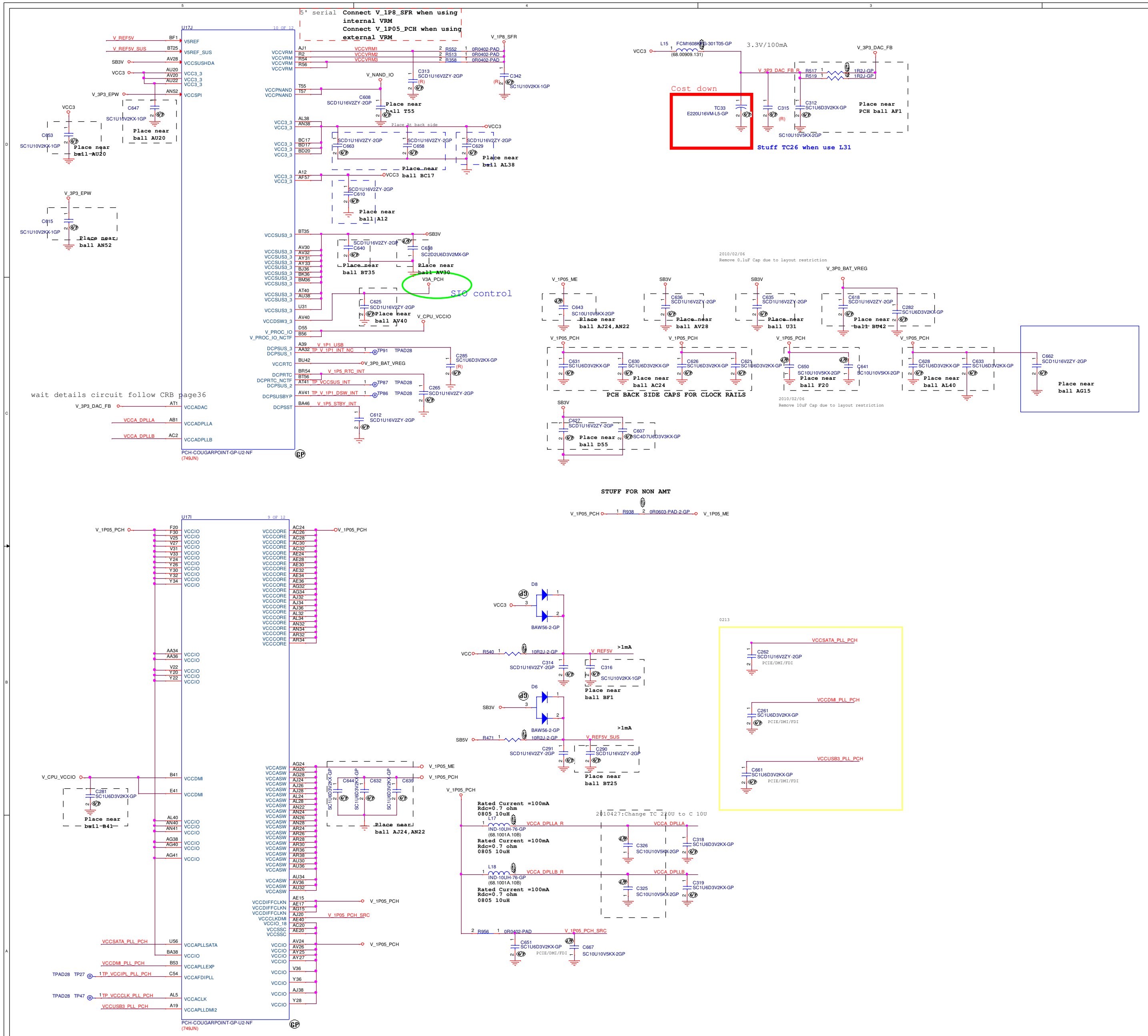

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wistron

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Hsichih, Taipei

Title: PCH_Cougar_POWER

Size	Document Number	Rev
D	Rosa_Eagleton	SA

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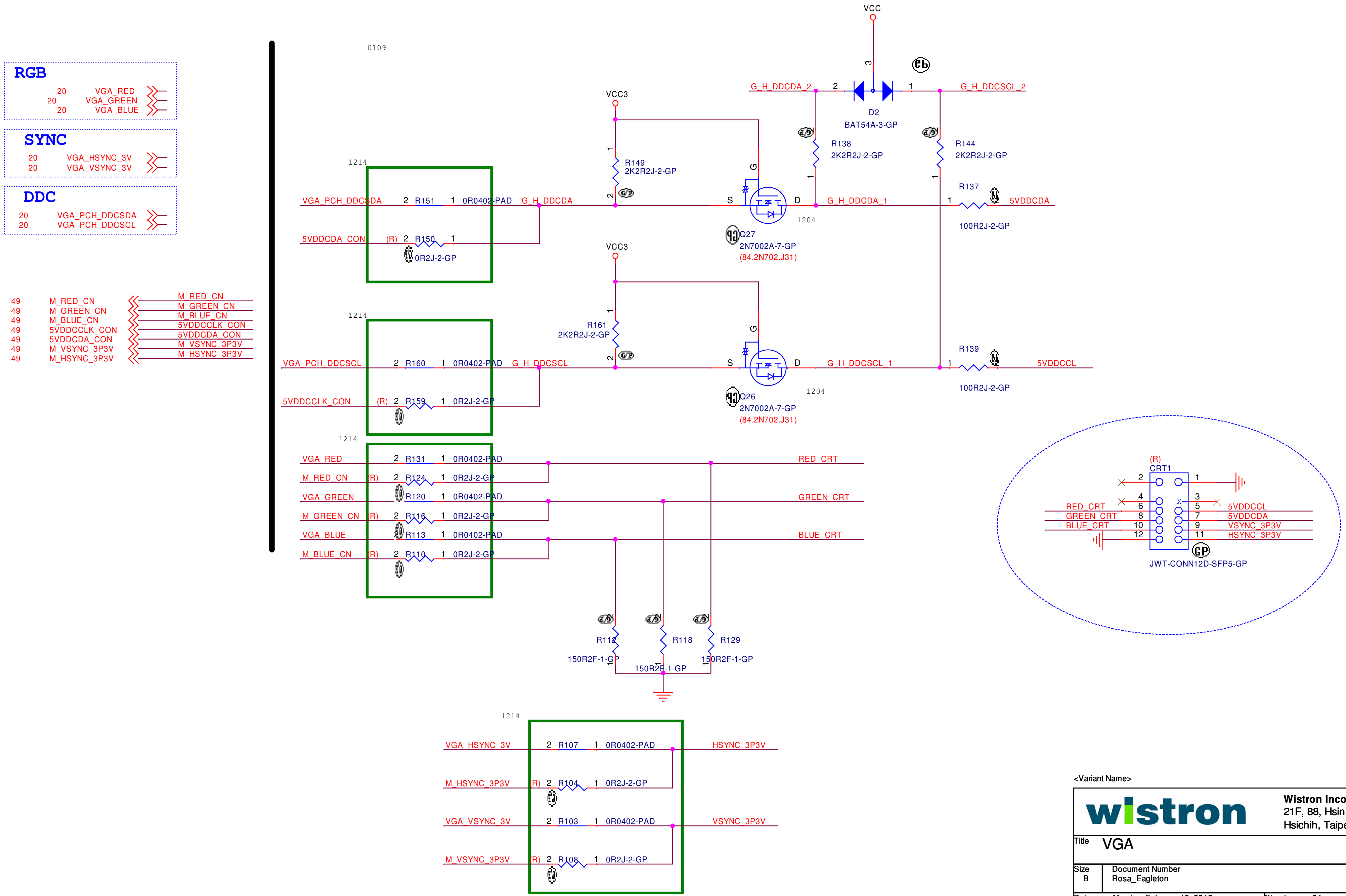

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Hsichih, Taipei

Title: VGA

Size	Document Number	Rev
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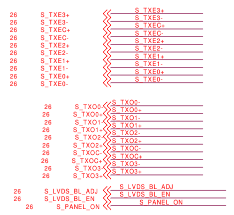
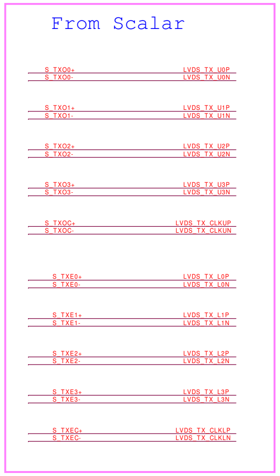
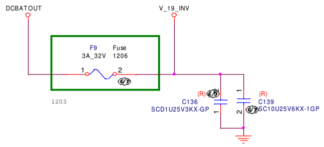
From Scalar to LVDS



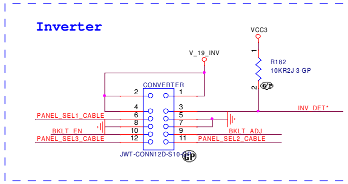
From GPU to LVDS

From Scalar

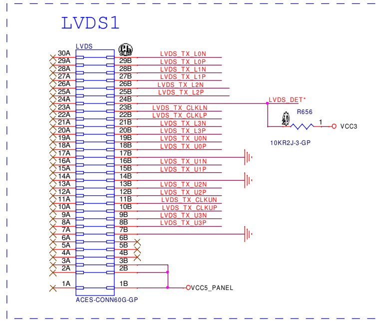


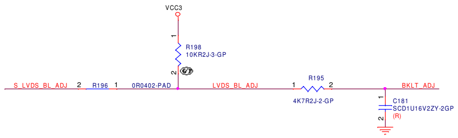


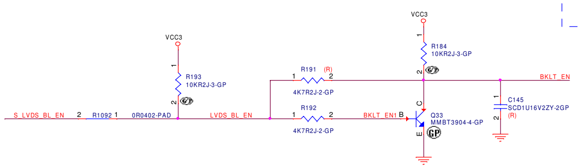
Inverter



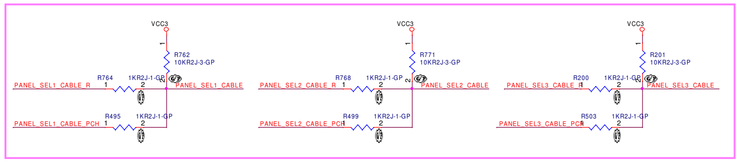
LVDS1



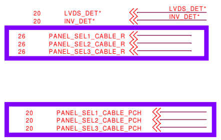




Selet cable

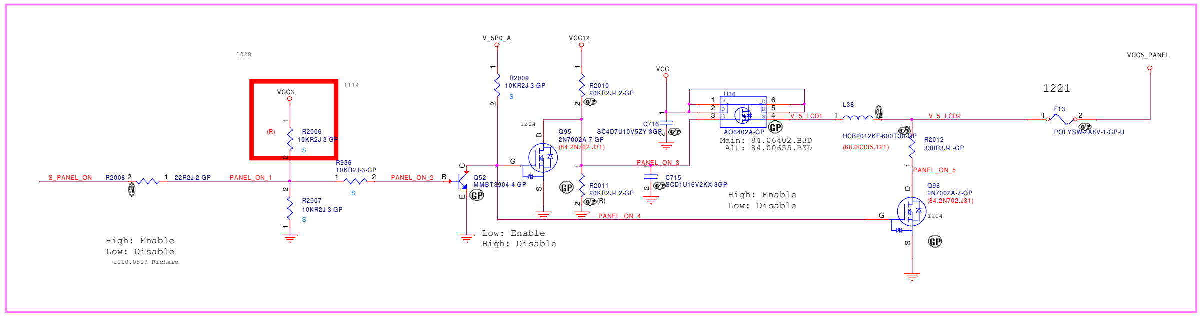


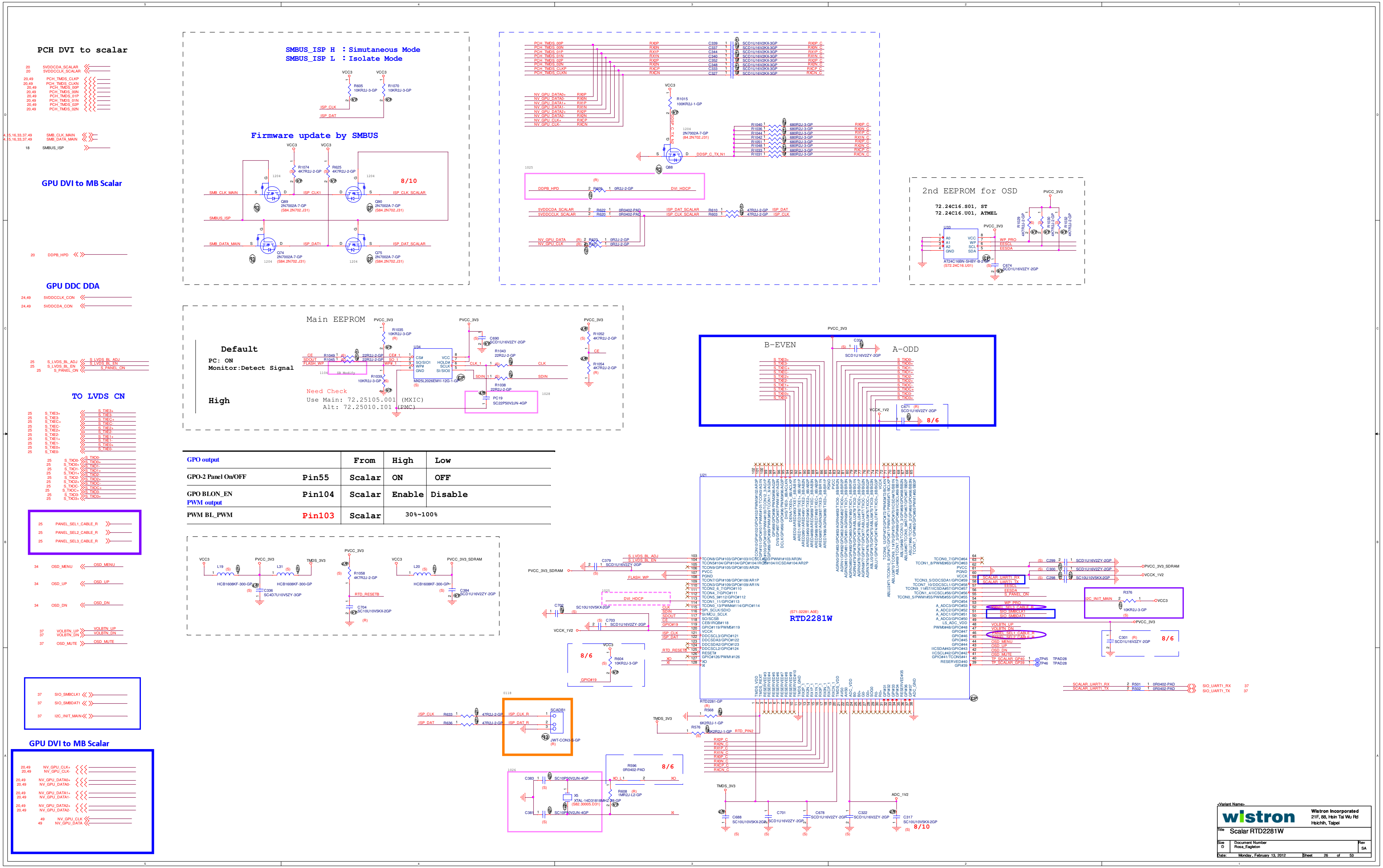
GPIO



PANEL_SEL_TAB

	PANEL_SEL1	PANEL_SEL2	PANEL_SEL3
Samsung	1	1	1
Chimei	1	1	0





GPO output		From	High	Low
GPO-2 Panel On/OFF	Pin55	Scalar	ON	OFF
GPO BLON_EN	Pin104	Scalar	Enable	Disable
PWM output				
PWM BL_PWM	Pin103	Scalar	30%~100%	

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Title: Scalar RTD2281W

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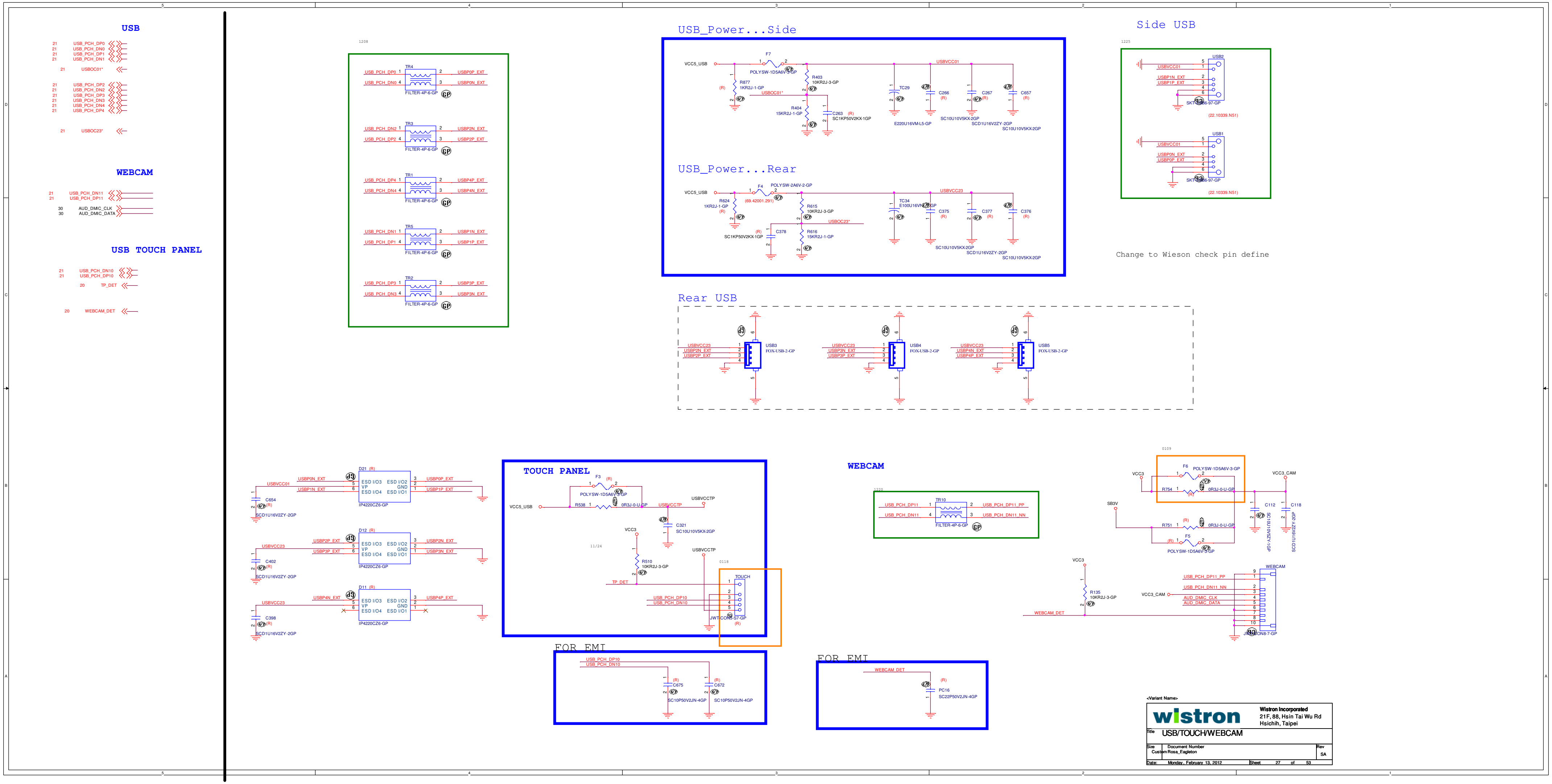
USB
USB_PCH_DP0
USB_PCH_DN0
USB_PCH_DP1
USB_PCH_DN1
USBOC01#
USB_PCH_DP2
USB_PCH_DN2
USB_PCH_DP3
USB_PCH_DN3
USB_PCH_DN4
USB_PCH_DP4
USBOC23#
WEBCAM
USB_PCH_DN11
USB_PCH_DP11
AUD_DMIC_CLK
AUD_DMIC_DATA
USB TOUCH PANEL
USB_PCH_DN10
USB_PCH_DP10
TP_DET
WEBCAM_DET
USB_Power...Side
VCC5_USB
POLYSW-1D5A6V-3-GP
USBVCC01
USB_Power...Rear
POLYSW-2A6V-2-GP
USBVCC23
Side USB
Change to Wieson check pin define
Rear USB
FOX-USB-2-GP
TOUCH PANEL
USBVCCTP
FOR EMI
WEBCAM
VCC3_CAM
FILTER-4P-6-GP
IP4220CZ6-GP
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
USB/TOUCH/WEBCAM
Size
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Custom
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SA
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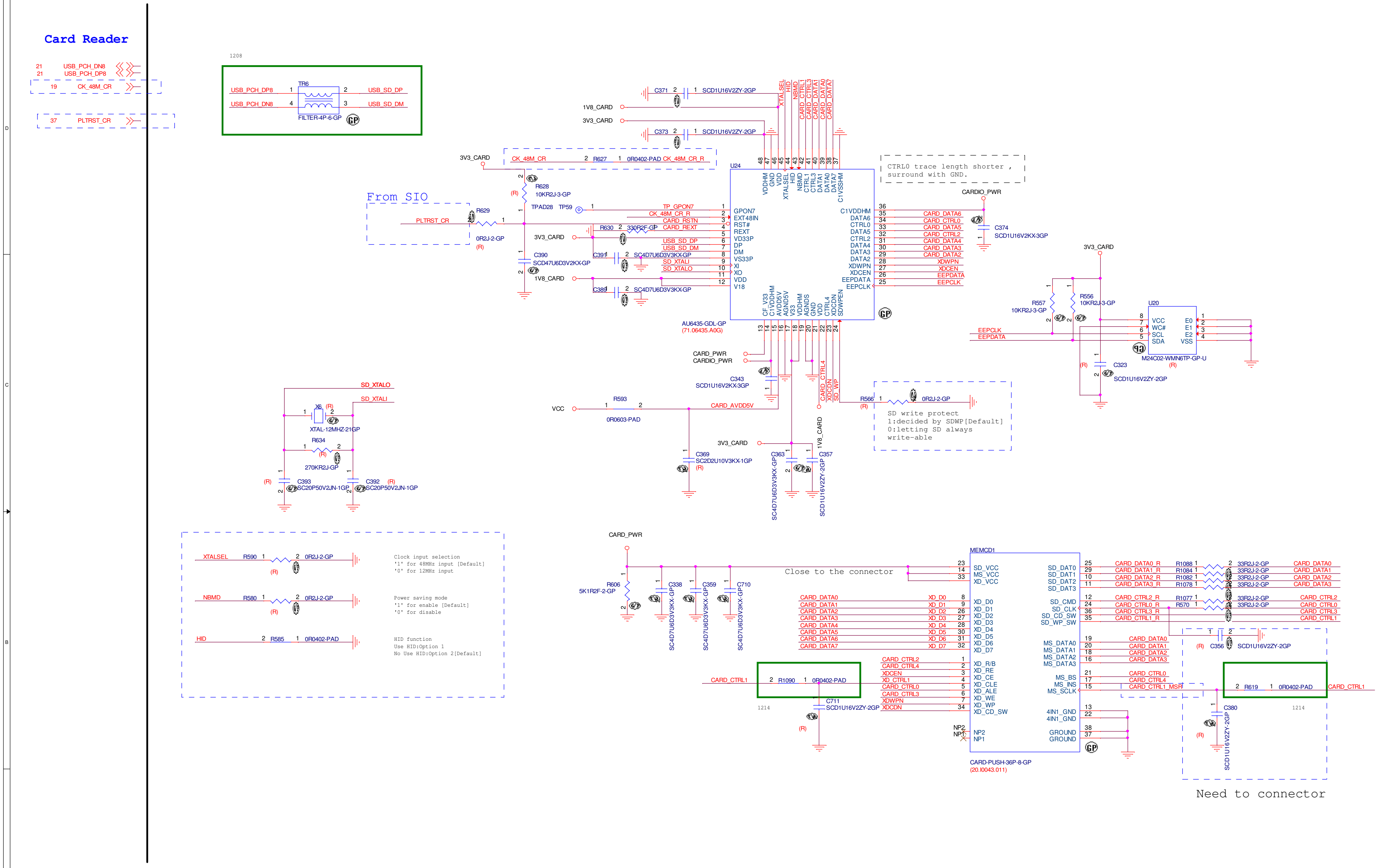
Card Reader



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	Card Reader AU6435	
Size C	Document Number Rosa_Eagleton	Rev SA
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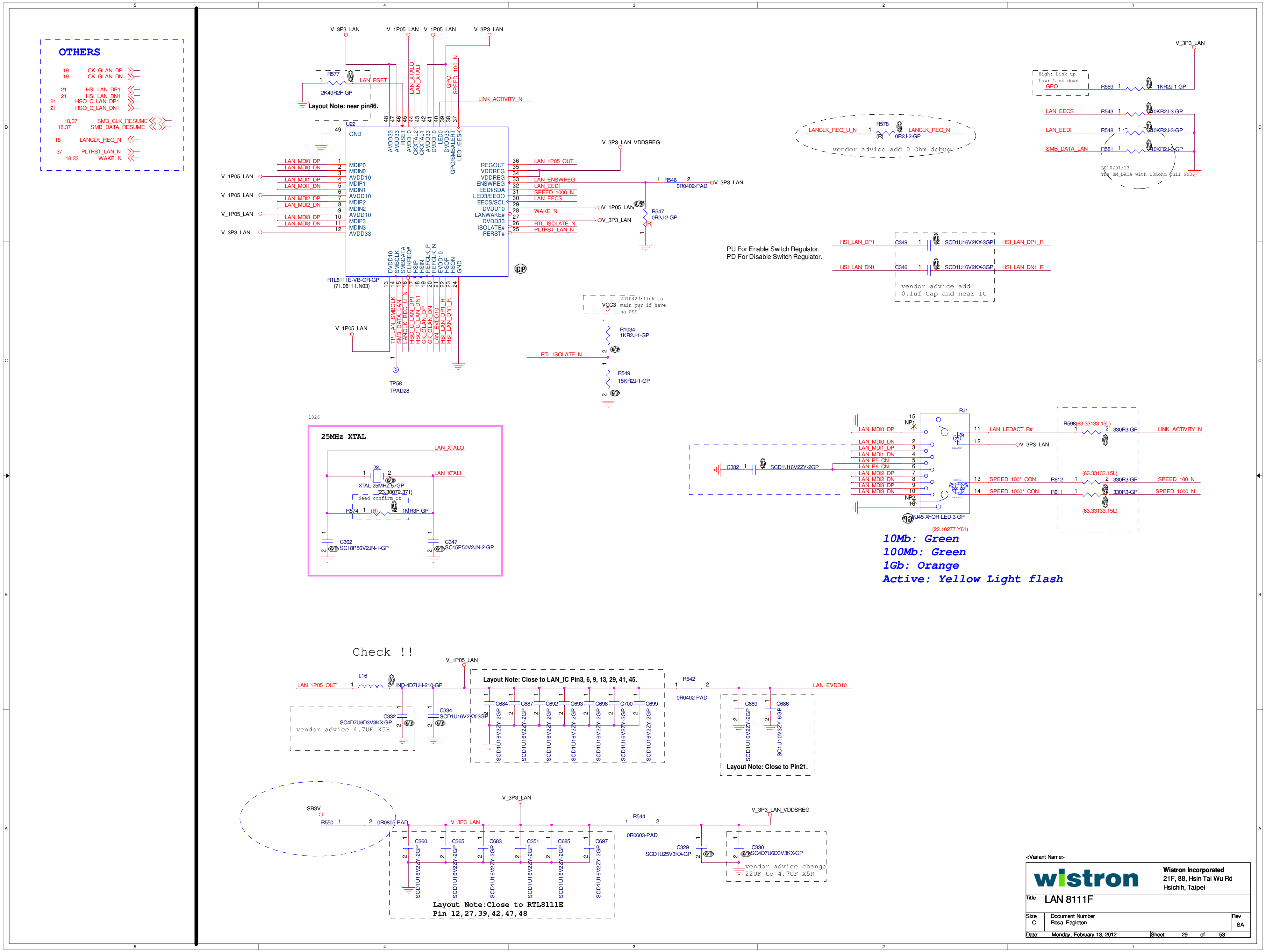
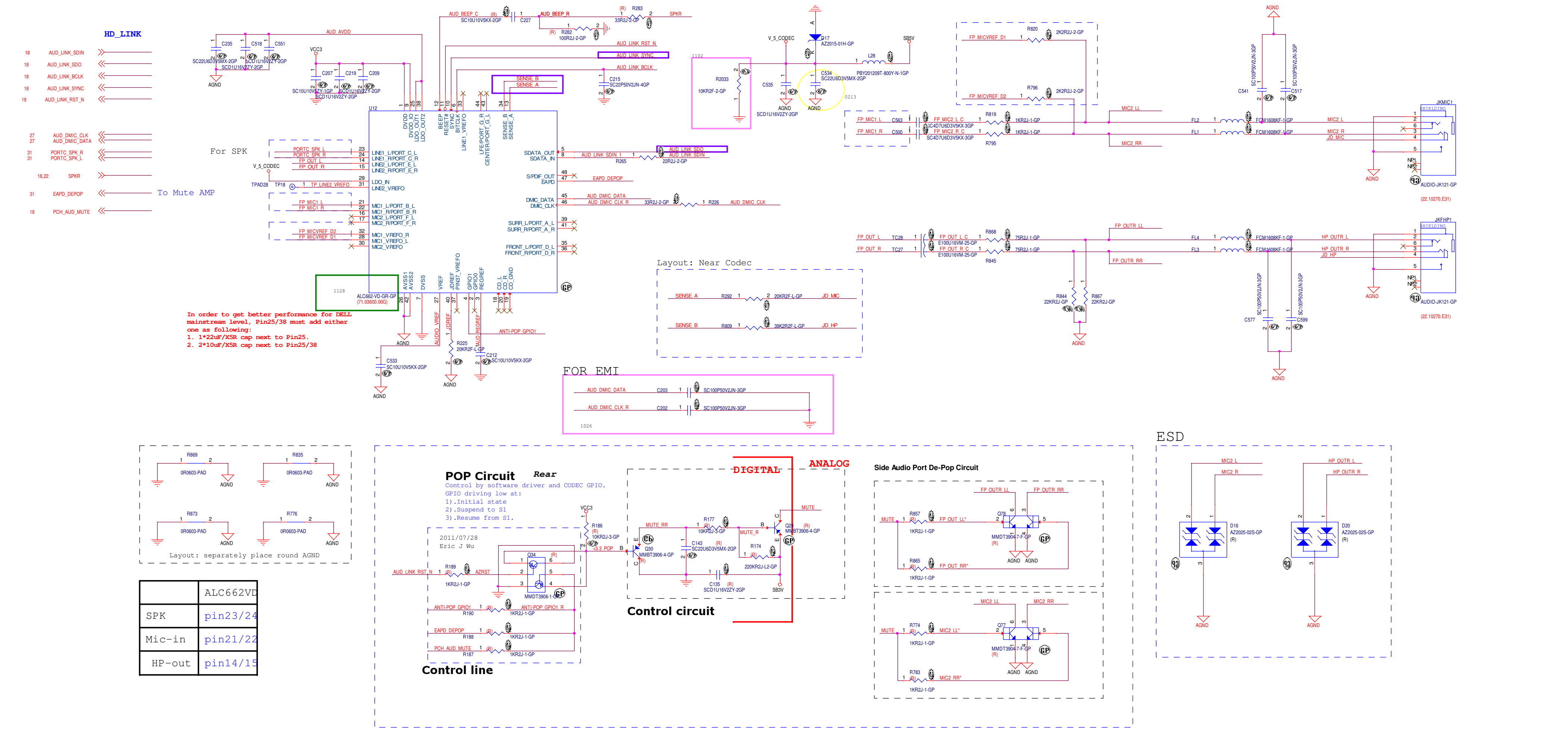

OTHERS
19 CK_GLAN_DP
19 CK_GLAN_DN
21 HSI_LAN_DP1
21 HSI_LAN_DN1
21 HSO_C_LAN_DP1
21 HSO_C_LAN_DN1
18,37 SMB_CLK_RESUME
18,37 SMB_DATA_RESUME
18 LANCLK_REQ_N
37 PLTRST_LAN_N
18,33 WAKE_N
V_3P3_LAN
V_1P05_LAN
R577
2K49R2F-GP
LAN_RSET
Layout Note: near pin46.
U22
GND
LAN_XTALO
LAN_XTALI
GPO
SPEED_100_N
LINK_ACTIVITY_N
MDIP0
MDIN0
AVDD10
MDIP1
MDIN1
MDIP2
MDIN2
MDIP3
MDIN3
AVDD33
LAN_MDI0_DP
LAN_MDI0_DN
LAN_MDI1_DP
LAN_MDI1_DN
LAN_MDI2_DP
LAN_MDI2_DN
LAN_MDI3_DP
LAN_MDI3_DN
REGOUT
VDDREG
ENSWREG
EEDI/SDA
LED3/EEDO
EECS/SCL
DVDD10
LANWAKE#
DVDD33
ISOLATE#
PERST#
LAN_1P05_OUT
LAN_ENSWREG
LAN_EEDI
SPEED_1000_N
LAN_EECS
WAKE_N
RTL_ISOLATE_N
PLTRST_LAN_N
V_3P3_LAN_VDDSREG
R546
0R0402-PAD
R547
0R2J-2-GP
RTL8111E-VB-GR-GP
(71.08111.N03)
TP58
TPAD28
VCC3
2010421:link to main pwr if have no AOE
R1034
1KR2J-1-GP
RTL_ISOLATE_N
R549
15KR2J-1-GP
R578
LANCLK_REQ_U_N
LANCLK_REQ_N
0R2J-2-GP
vendor advice add 0 Ohm debug
High: Link up
Low: Link down
GPO
R559
1KR2J-1-GP
LAN_EECS
R543
10KR2J-3-GP
LAN_EEDI
R548
10KR2J-3-GP
SMB_DATA_LAN
R581
10KR2J-3-GP
2010/01/13
The SM_DATA with 10Kohm pull GND
PU For Enable Switch Regulator.
PD For Disable Switch Regulator.
HSI_LAN_DP1
C349
SCD1U16V2KX-3GP
HSI_LAN_DP1_R
HSI_LAN_DN1
C346
SCD1U16V2KX-3GP
HSI_LAN_DN1_R
vendor advice add 0.1uf Cap and near IC
1026
25MHz XTAL
LAN_XTALO
X4
LAN_XTALI
XTAL-25MHZ-57GP
(23.30072.371)
Need confirm it
R574
1MR3F-GP
C362
SC18P50V2JN-1-GP
C347
SC15P50V2JN-2-GP
RJ1
LAN_LEDACT_R#
R598 (63.33133.15L)
330R3-GP
LINK_ACTIVITY_N
V_3P3_LAN
C382
SCD1U16V2ZY-2GP
LAN_P5_CN
LAN_P6_CN
SPEED_100*_CON
R612
330R3-GP
SPEED_100_N
SPEED_1000*_CON
R611
330R3-GP
SPEED_1000_N
(63.33133.15L)
RJ45-XFOR-LED-3-GP
(22.10277.Y61)
10Mb: Green
100Mb: Green
1Gb: Orange
Active: Yellow Light flash
Check !!
L16
IND-4D7UH-210-GP
LAN_1P05_OUT
C332
SC4D7U6D3V3KX-GP
vendor advice 4.7UF X5R
C334
SCD1U16V2KX-3GP
Layout Note: Close to LAN_IC Pin3, 6, 9, 13, 29, 41, 45.
C684 C687 C692 C693 C698 C700 C699
SCD1U16V2ZY-2GP
R542
0R0402-PAD
LAN_EVDD10
C689
SCD1U16V2ZY-2GP
C686
SC1U10V3ZY-6GP
Layout Note: Close to Pin21.
SB3V
R550
0R0805-PAD
V_3P3_LAN
C360 C365 C683 C351 C685 C697
SCD1U16V2ZY-2GP
Layout Note:Close to RTL8111E
Pin 12,27,39,42,47,48
R544
0R0603-PAD
V_3P3_LAN_VDDSREG
C329
SCD1U25V3KX-GP
C330
SC4D7U6D3V3KX-GP
vendor advice change 22UF to 4.7UF X5R
<Variant Name>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title LAN 8111F
Size C
Document Number Rosa_Eagleton
Rev SA
Date: Monday, February 13, 2012
Sheet 29 of 53

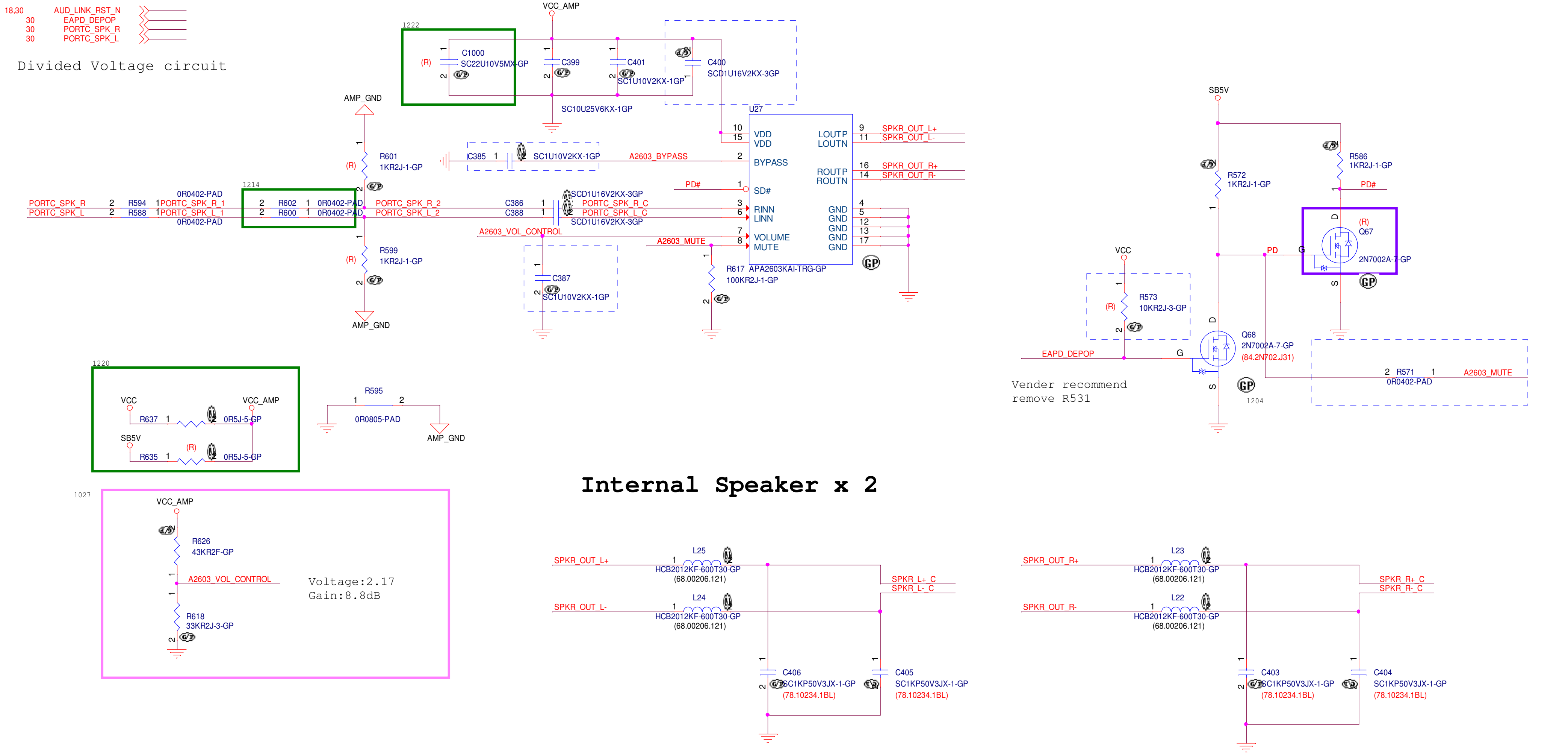


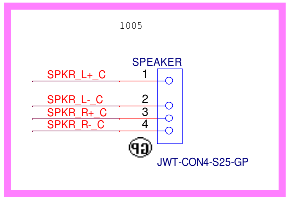
	ALC662VD
SPK	pin23/24
Mic-in	pin21/22
HP-out	pin14/15

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	AUDIO ALC662		
Size Custom	Document Number Rosa_Eagleton		Rev SA
Date: Monday, February 13, 2012	Sheet 30 of 53		





As you said, input voltage=1.24Vrms.
Under Po=2.5W, RL=4Ω condition.

2.5W=(Vo_rms)^2 / 4Ω ➔ Vo_rms=3.16V

Gain=20log(Vo_rms/Vi_rms) ➔ Gain=8.12dB
As APA2603 datasheet indicate of volume table:

29	8.8	41.96	43.94	42.95	2.098	2.197	2.15
30	8.4	43.44	45.42	44.43	2.172	2.271	2.22
31	8	44.92	46.90	45.91	2.246	2.345	2.30

You should set gain at least to **8.4dB.**

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: AMP APA2603

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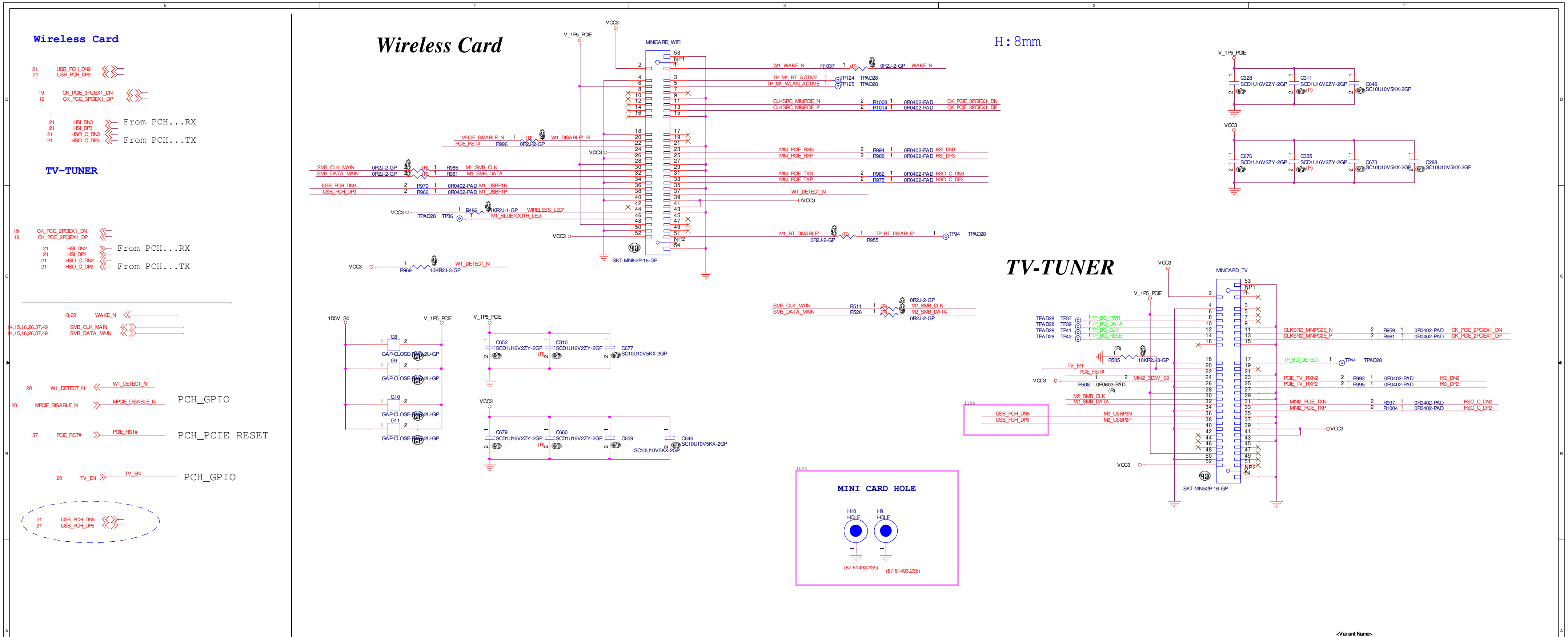
<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	TBD	
Size C	Document Number Rosa_Eagleton	Rev SA
Date:	Monday, February 13, 2012	Sheet 32 of 53



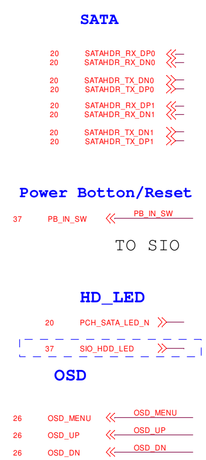
<Variant Name>

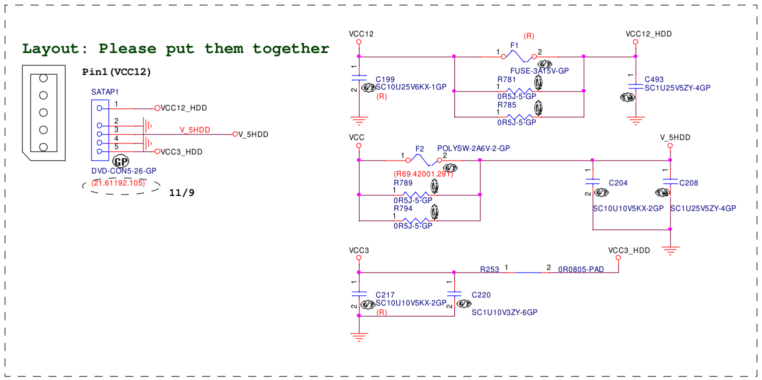
wistron

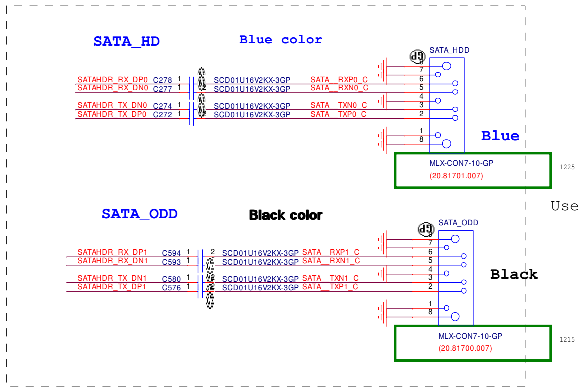
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	WIRELESS BT/TV TUNER	
Size: Custom	Document Number: Rosa_Eagleton	Rev: SA
Date: Monday, February 13, 2012	Sheet 33 of 53	

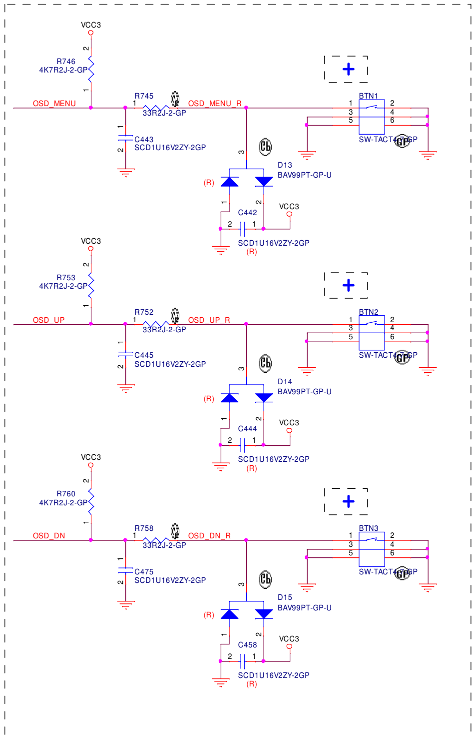
SATA



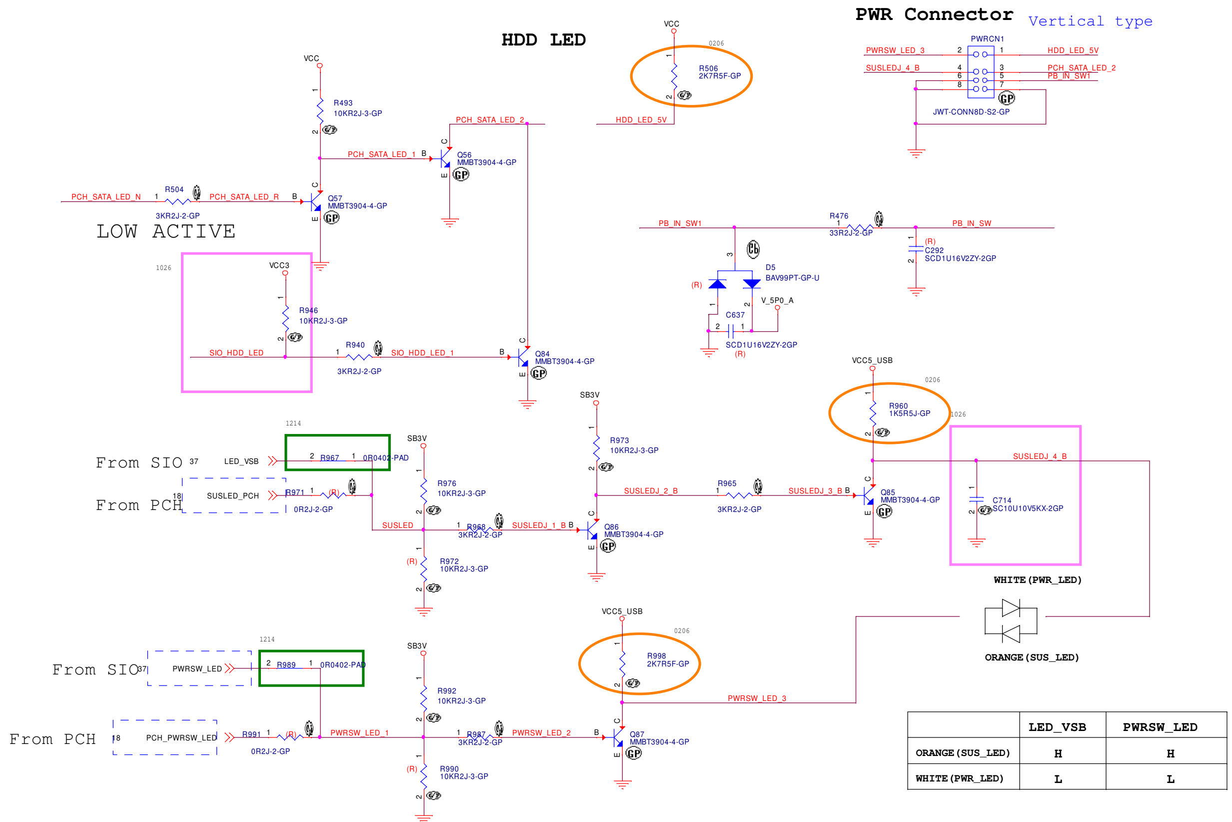




Use KORTAK vendor



	Function
BTN1	MENU
BTN2	UP
BTN3	DOWN



	LED_VSB	PWRSW_LED
ORANGE (SUS_LED)	H	H
WHITE (PWR_LED)	L	L

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: SATA/LED/BTN

Size: Custom | Document Number: Rosa_Eagleton | Rev: SA

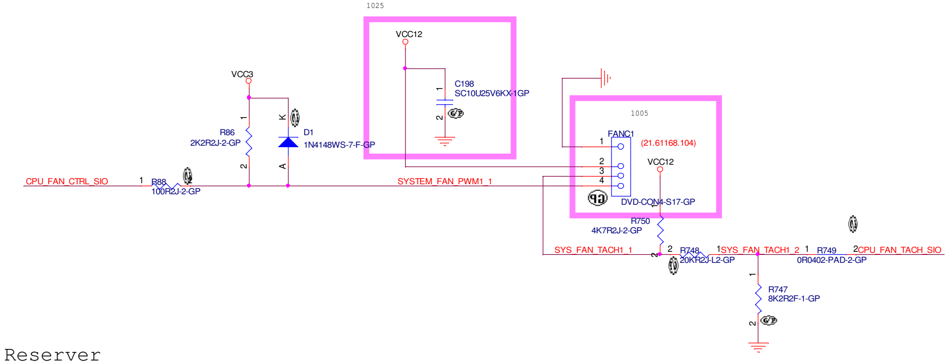
Date: Monday, February 13, 2012 | Sheet 34 of 53

SIO FAN CONTROL

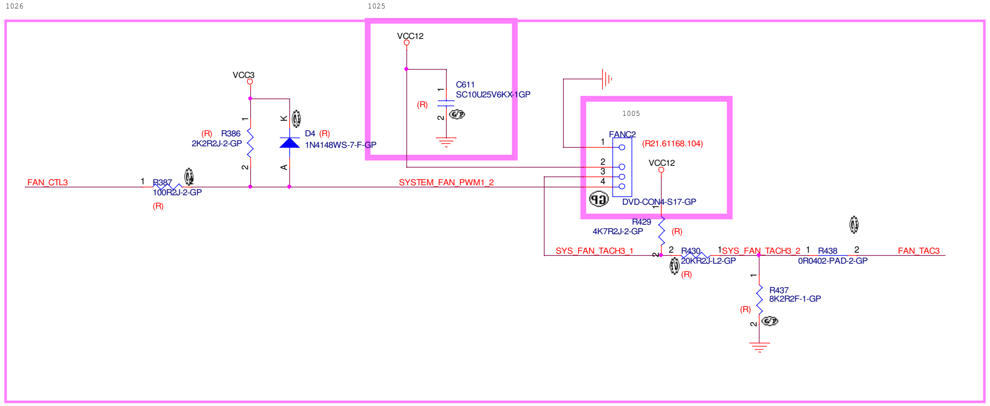
37 CPU_FAN_CTRL_SIO
37 CPU_FAN_TACH_SIO

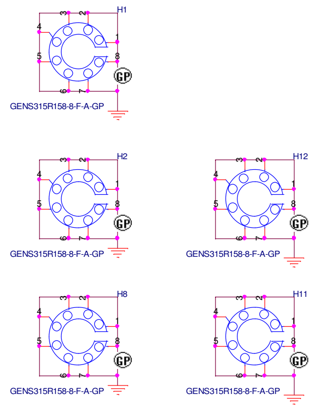
37 FAN_TAC3
37 FAN_CTL3

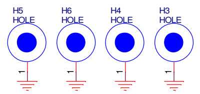
4 PINS FAN CONTROL



Reserver







CPU Heatsink screw hole.

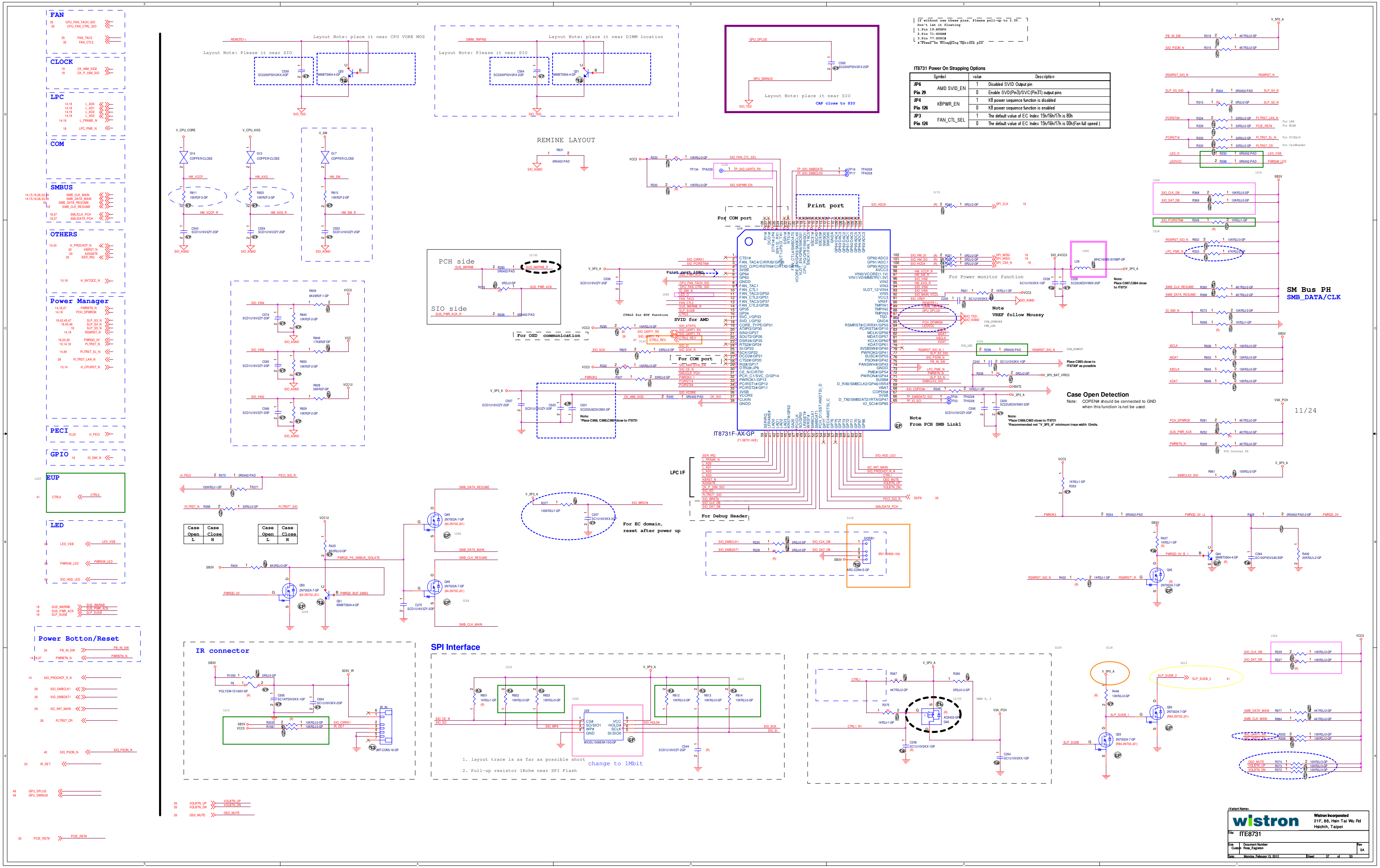
<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	FAN CIRCUITS/HOLE	
Size C	Document Number Rosa_Eagleton	Rev SA
Date: Monday, February 13, 2012	Sheet 35 of 53	

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	Remote control	
Size C	Document Number Rosa_Eagleton	Rev SA
Date: Monday, February 13, 2012	Sheet 36 of 53	



If without use these pins, Please pull-up to 3.3V.
Don't let it floating
1.Pin 19:ATXPG
2.Pin 71:SUSB#
3.Pin 77:SUSC#
4.Power On Strapping Options pin

IT8731 Power On Strapping Options

Symbol		value	Description
JP6 **Pin 29**	AMD SVID_EN	1	Disabled SVID Output pin
		0	Enable SVD(Pin3)/SVC(Pin31) output pins
JP4 **Pin 126**	K8PWR_EN	1	K8 power sequence function is disabled
		0	K8 power sequence function is enabled
JP3 **Pin 124**	FAN_CTL_SEL	1	The default value of EC Index 15h/16h/17h is 80h
		0	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	ITE8731		
Size: Custom	Document Number: Rosa_Eagleton		Rev: SA
Date: Monday, February 13, 2012	Sheet 37 of 53		

RESERVED

<Variant Name>

wistron	**Wistron Incorporated** 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	TBD
Size B	Document Number Rosa_Eagleton
Rev	SA
Date:	Monday, February 13, 2012
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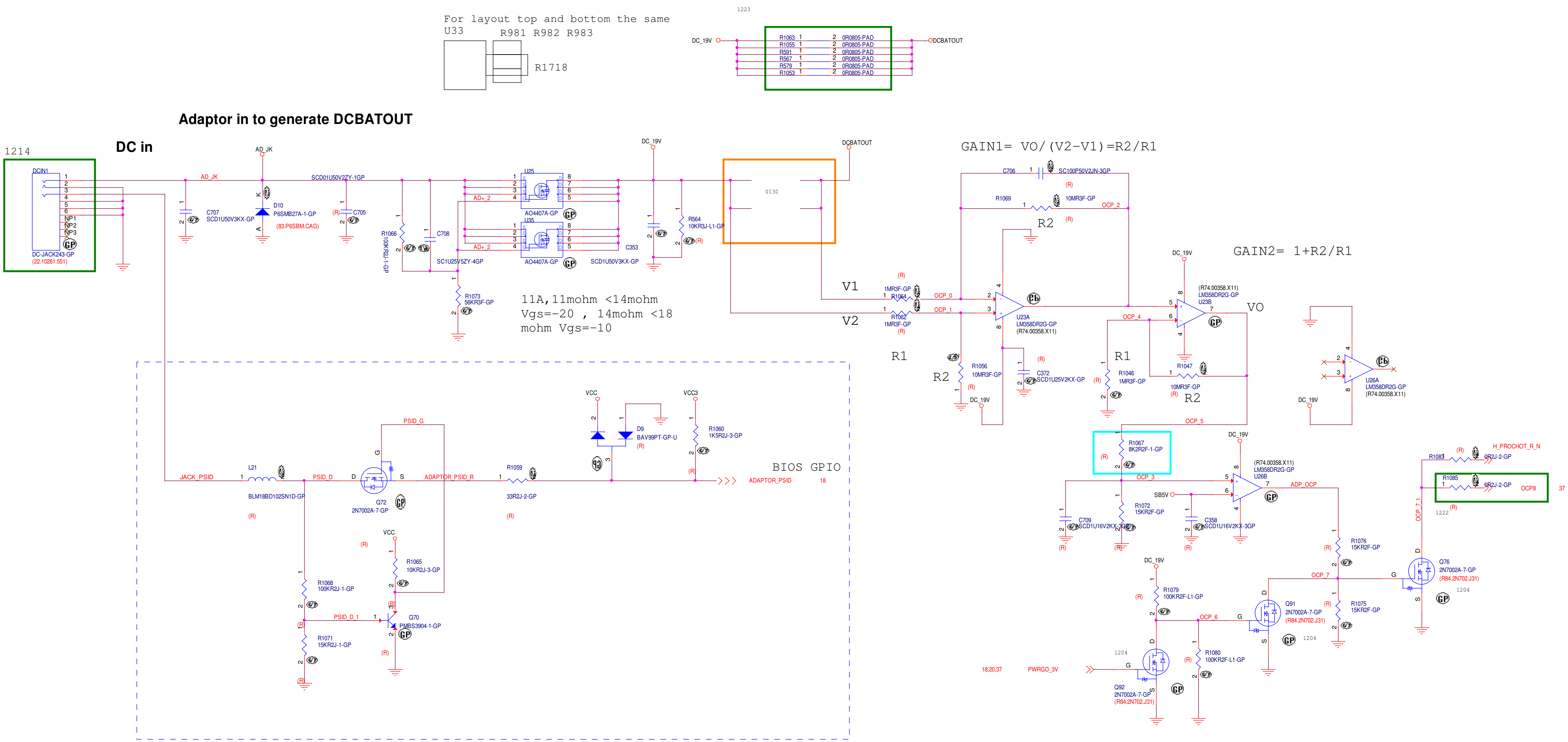
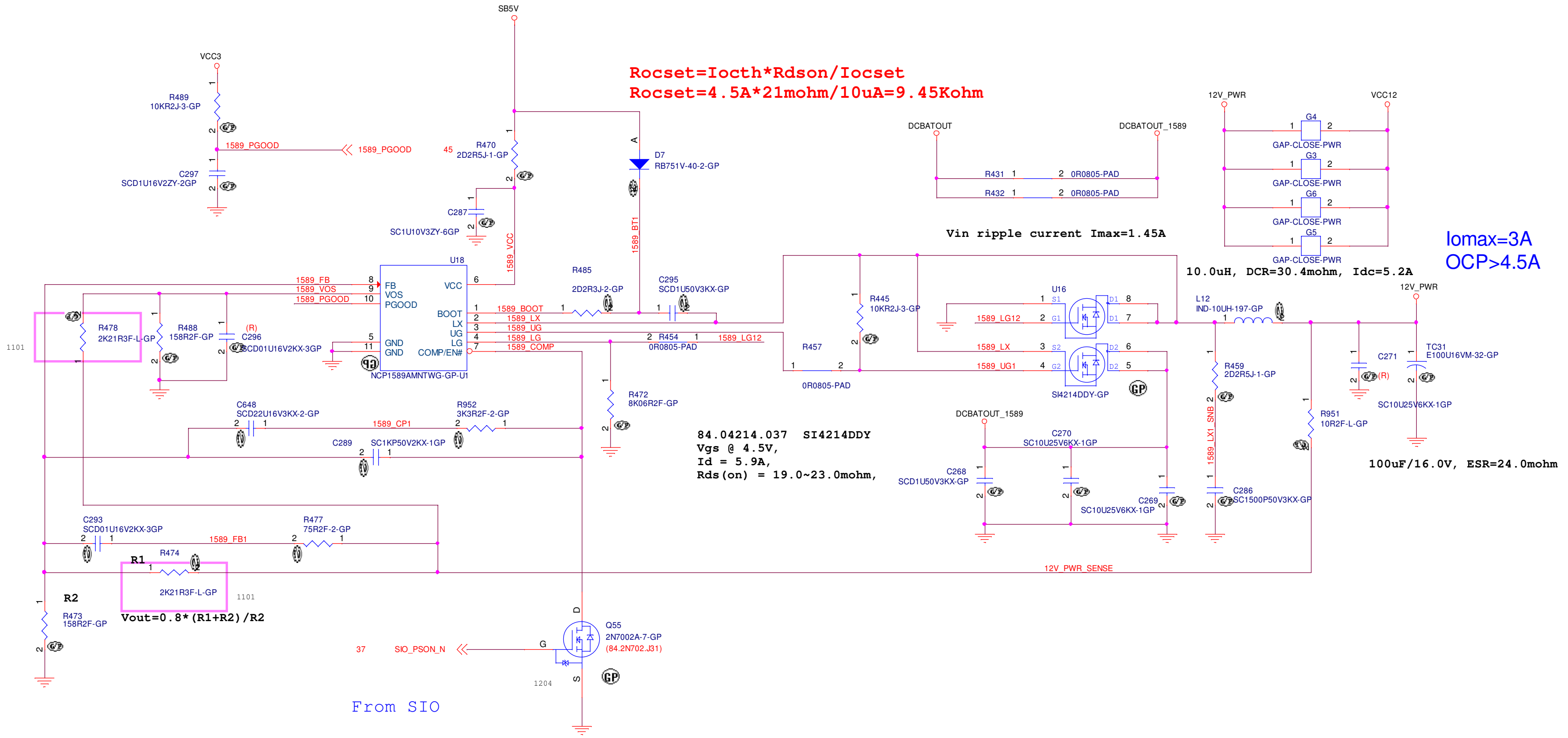


<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	DC IN	
Size: Custom	Document Number: Rosa_Eagleton	Rev: SA
Date: Monday, February 13, 2012	Sheet 39 of 53	



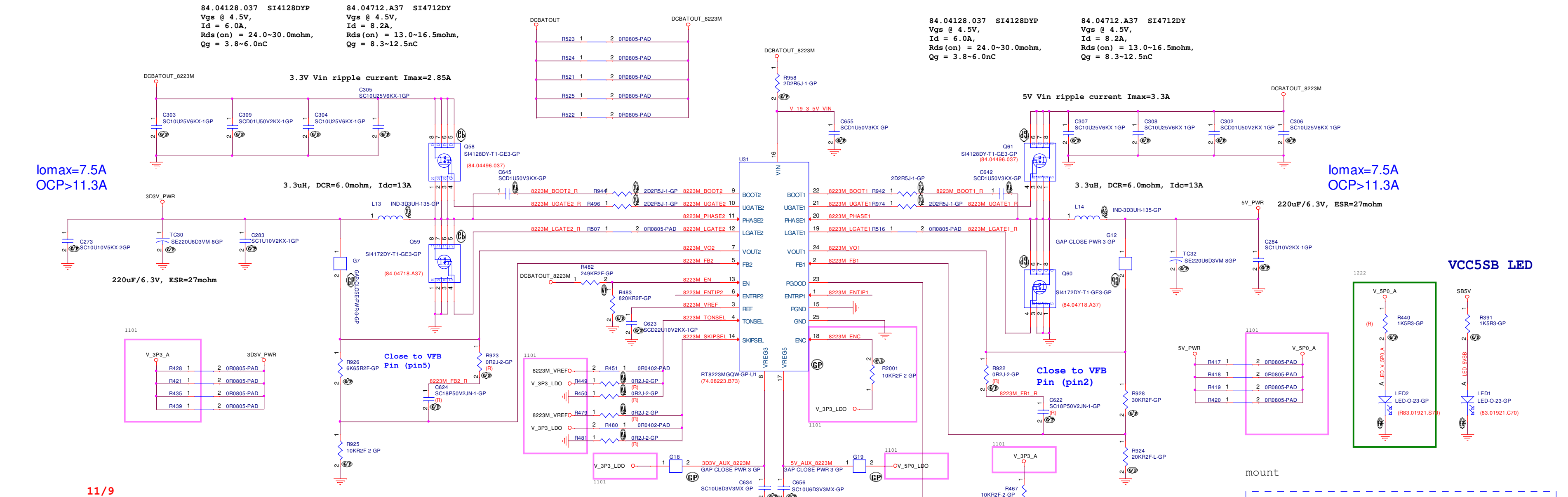
<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

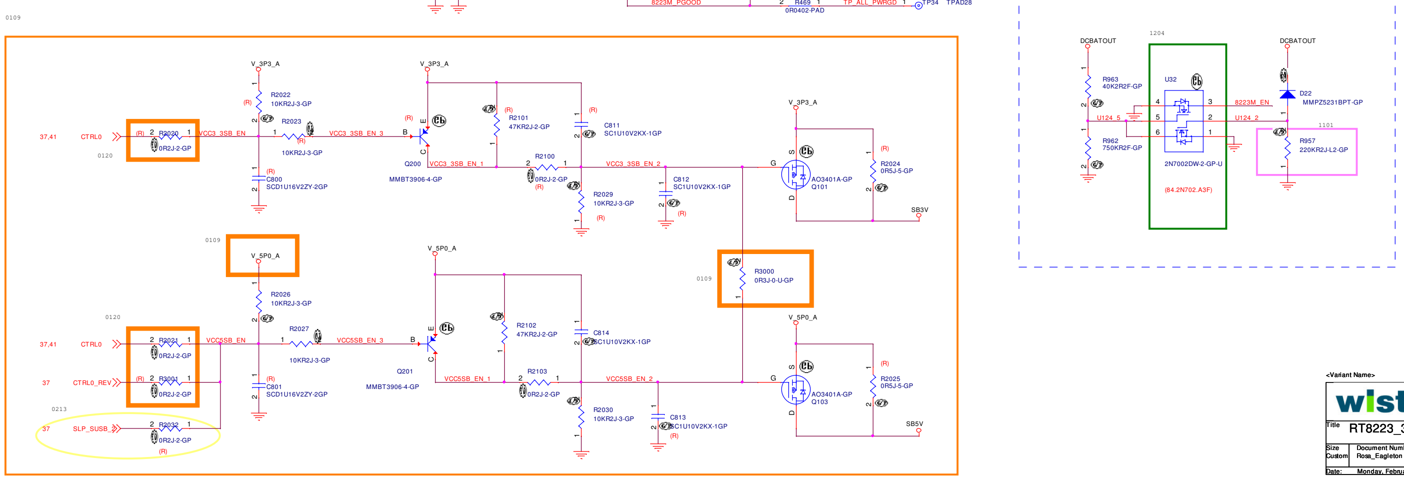
Title	NCP1589-> +12V	
Size: Custom	Document Number: Rosa_Eagleton	Rev: SA
Date: Monday, February 13, 2012	Sheet 40 of 53	

+3VSB/+5VSB

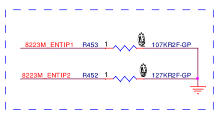


11/9

RT8223M	GND	VREF	VREG3	VREG5
SKIPSEL	SKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	300k/CH1 375k/CH2	400k/CH1 500k/CH2	400k/CH1 500k/CH2



OCP:13.125A



<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	RT8223_3V&5V
Size	Custom
Document Number	Rosa_Eagleton
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CPU VTT POWER

10 VCCIO_SEL
10 VCCTT_SENSE
10 VSSTT_SENSE
43 VTT_PGOOD

PCH

18,37,45,47 SLP_S3_N

CPU SA POWER

10 VCCSA_VID
10 VCCSA_SENSE

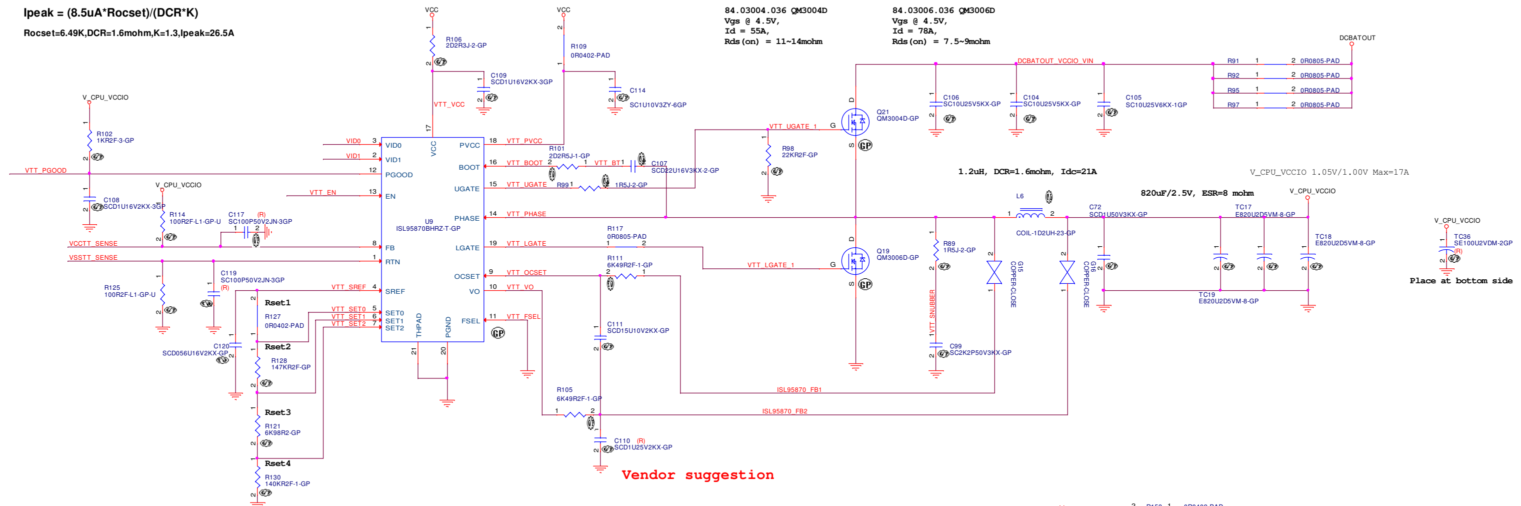
CPU VTT POWER

Ipeak = (8.5uA*Rocset)/(DCR*K)

Rocset=6.49K,DCR=1.6mohm,K=1.3,Ipeak=26.5A

84.03004.036 QM3004D
Vgs @ 4.5V,
Id = 55A,
Rds(on) = 11~14mohm

84.03006.036 QM3006D
Vgs @ 4.5V,
Id = 78A,
Rds(on) = 7.5~9mohm



Vout_max=0.5025*(1+(155.5198k/138.6k))
=1.066=1.05+1.5%

VID0	VID1	Vout
1	0	1.0V
0	0	1.05V

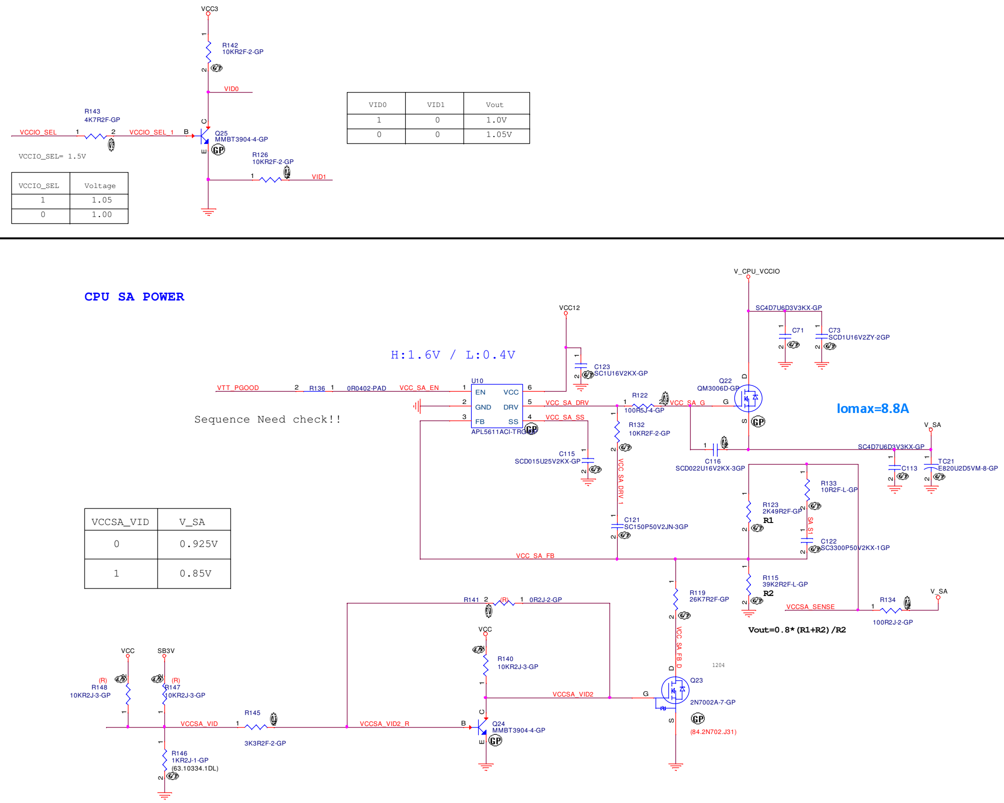
VCCIO_SEL	Voltage
1	1.05
0	1.00

CPU SA POWER

H:1.6V / L:0.4V

Sequence Need check!!

Iomax=8.8A



VCCSA_VID	V_SA
0	0.925V
1	0.85V

<Variant Name>

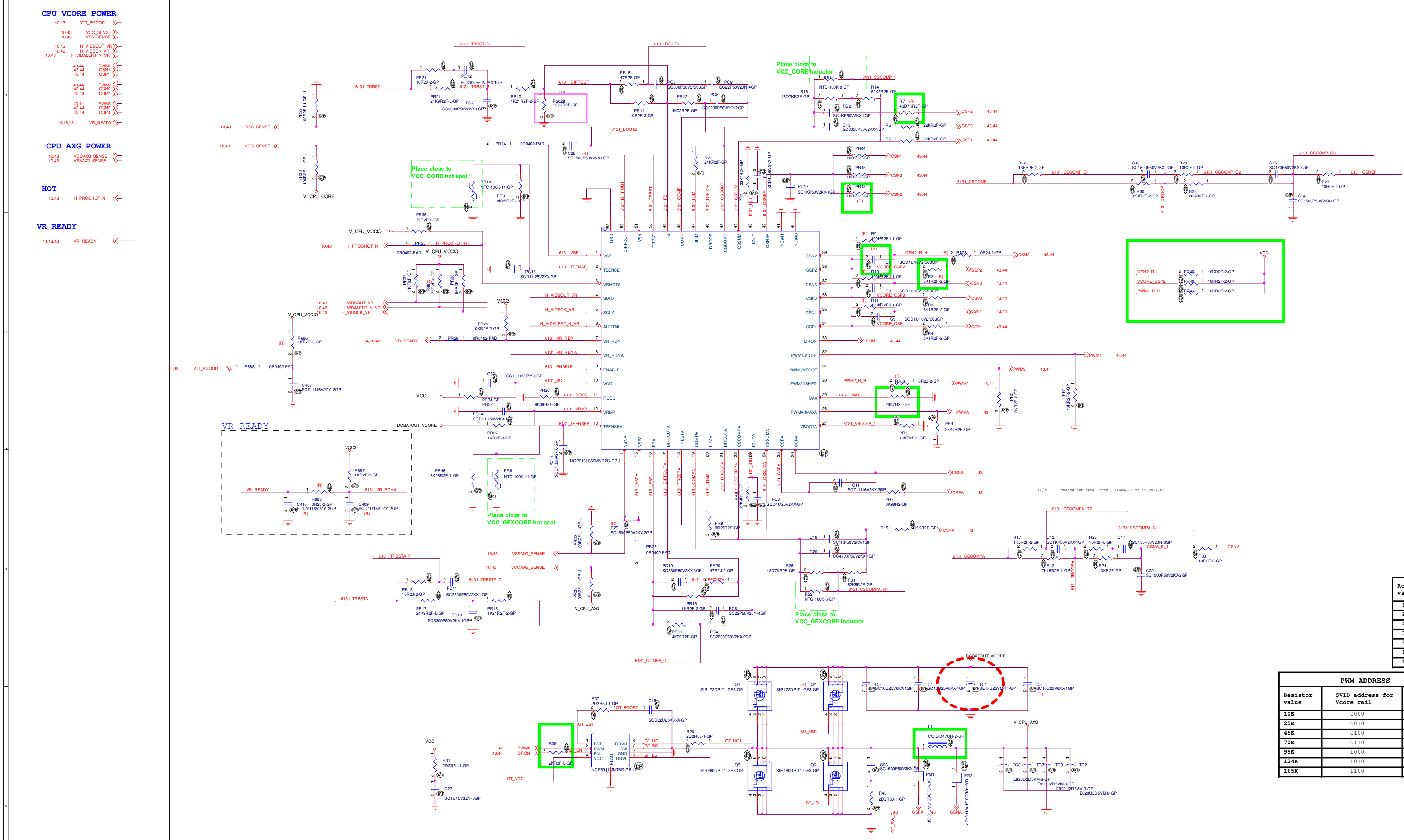
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU_VTT & CPU_SA

Size: Custom | Document Number: Rosa_Eagleton | Rev: SA

Date: Monday, February 13, 2012 | Sheet 42 of 53



Resistor value	Boot Voltage
10K	0V
25K	0.9V
45K	1V
70K	1.1V
95K	1.2V
125K	1.35V
165K	1.5V

PWM ADDRESS		
Resistor value	SVID address for Vcore rail	SVID address for VCC_AXG rail
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
124K	1010	1011
165K	1100	1101

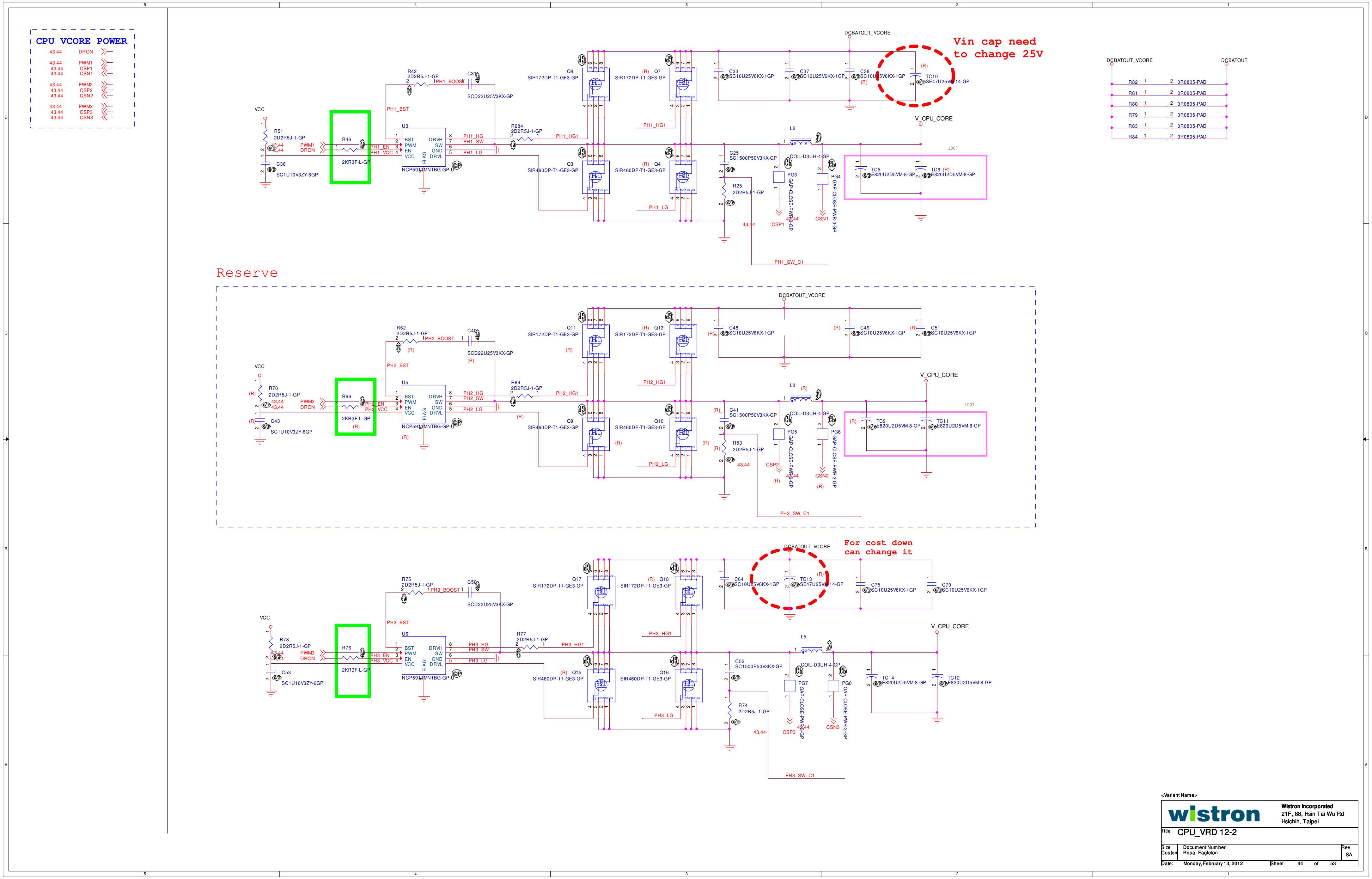
<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU_VRD 12-1 & CPU_AXG

Size	Document Number	Rev
D	Rosa_Eagleton	SA

Date: Monday, February 13, 2012 | Sheet 43 of 53



<Variant Name>

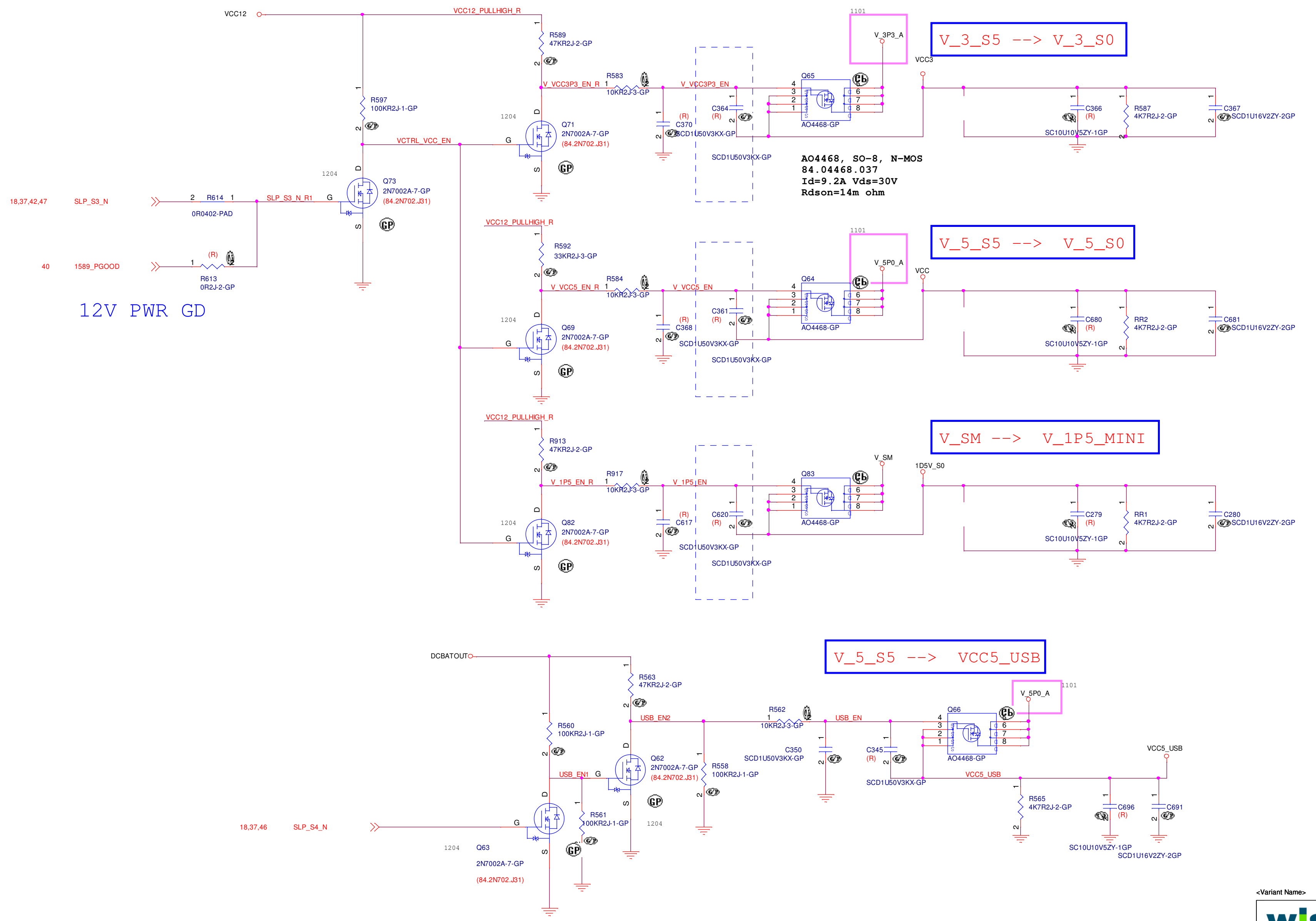
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU_VRD 12-2

Size: Custom | Document Number: Rosa_Eagleton | Rev: SA

Date: Monday, February 13, 2012 | Sheet 44 of 53

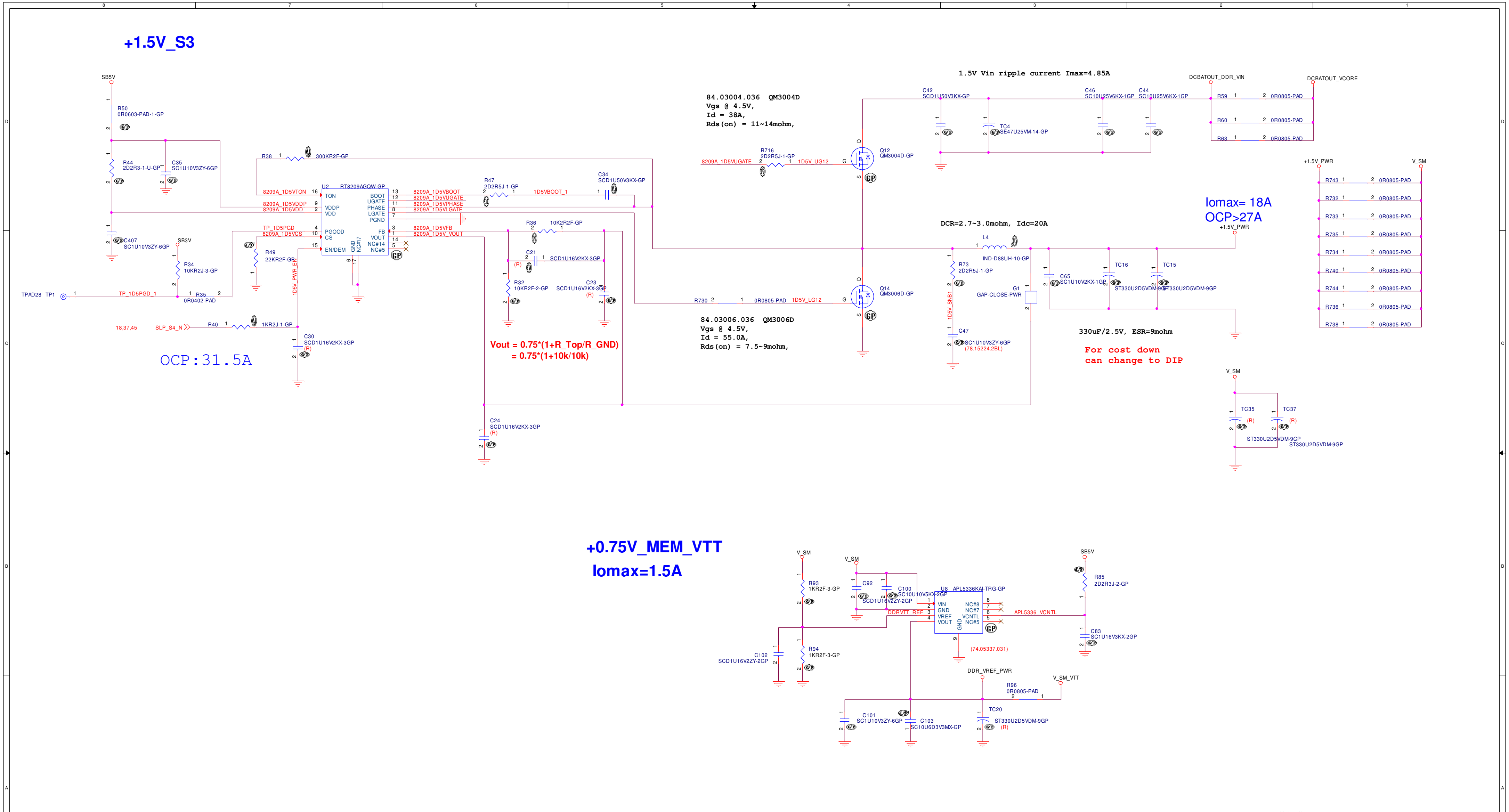


<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	Run PWR/USB PWR	
Size: Custom	Document Number: Rosa_Eagleton	Rev: SA
Date: Monday, February 13, 2012	Sheet 45 of 53	



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	MEM_1D5V/MEM_VTT	
Size: Custom	Document Number: Rosa_Eagleton	Rev: SA
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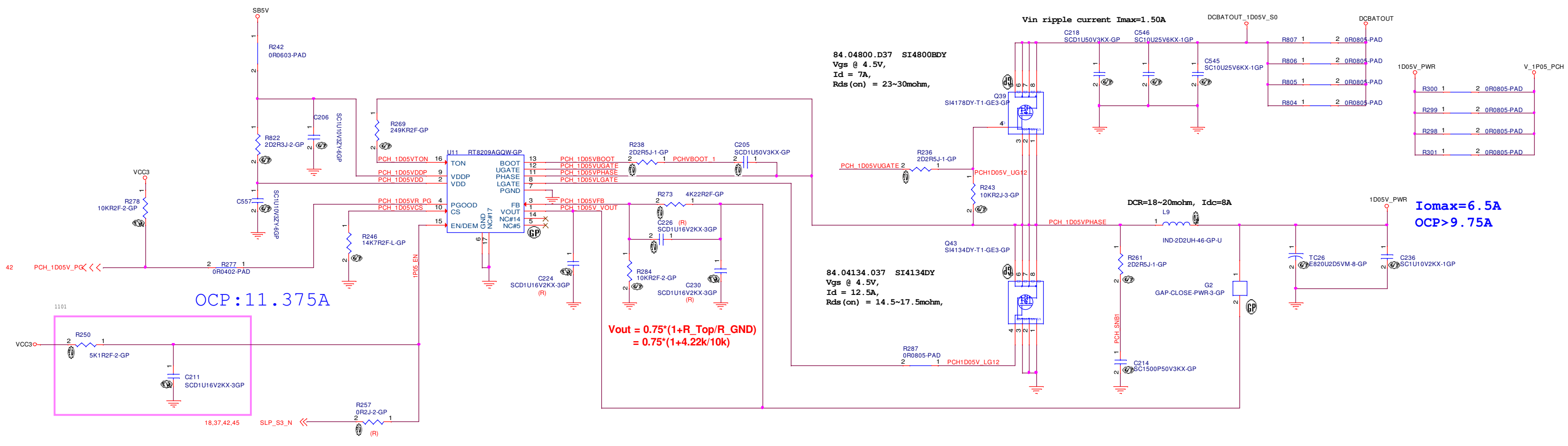
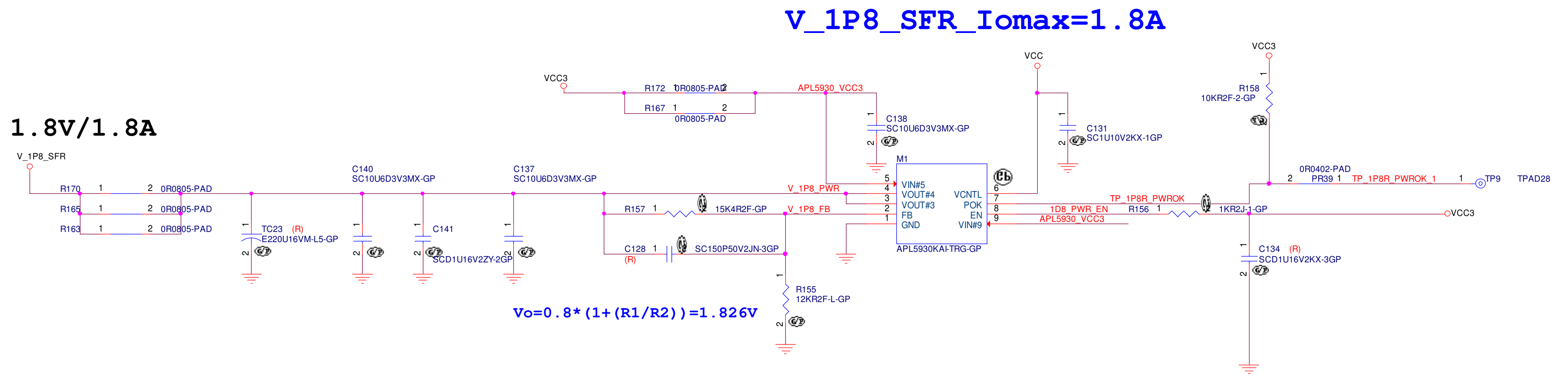
+1.05V(V_1D05_PCH)_RT8209A



<Variant Name>	
wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	PCH_1D05V
Size Custom	Document Number Rosa_Eagleton	Rev SA
Date: Monday, February 13, 2012	Sheet 47 of 53

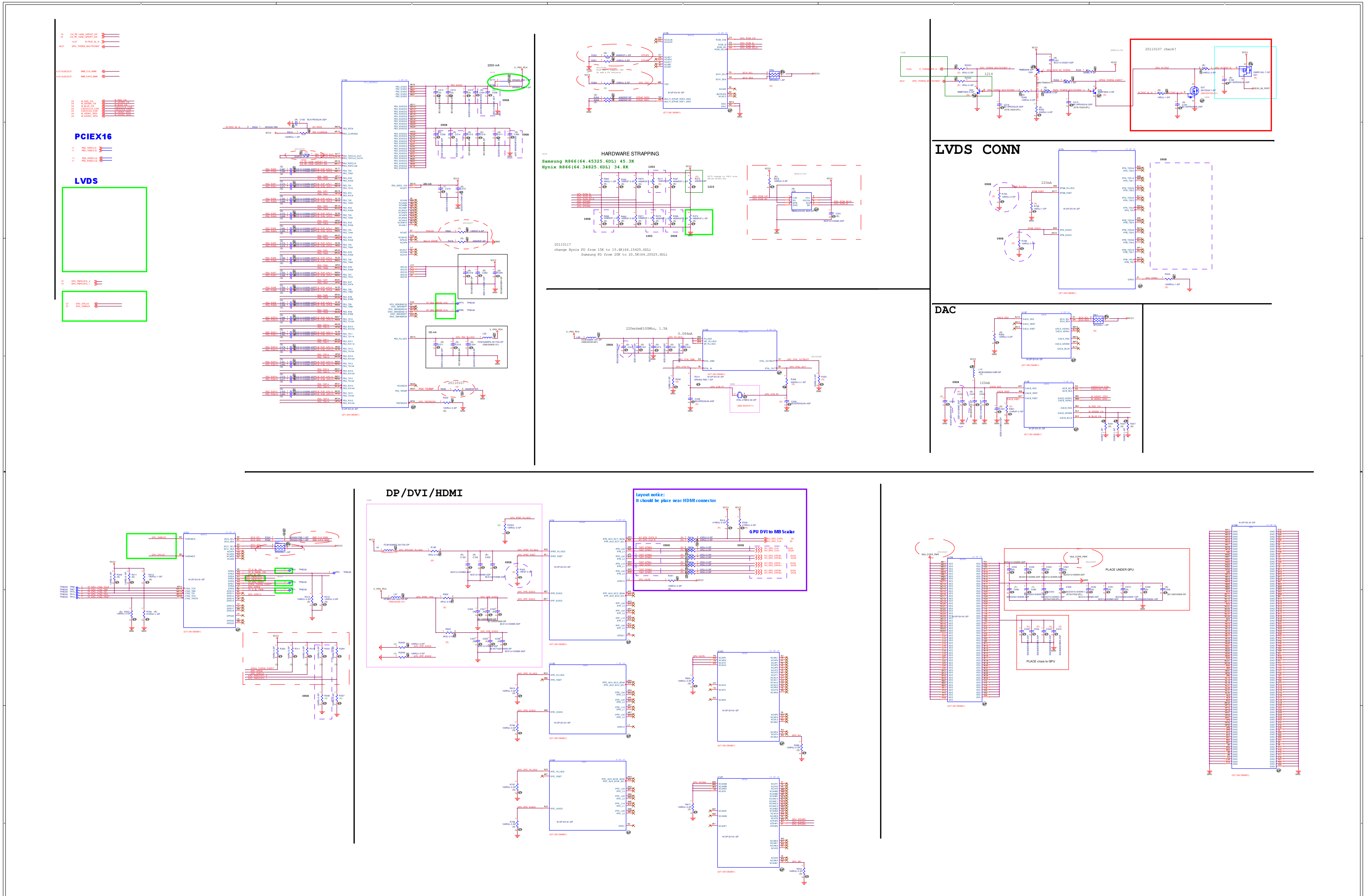


<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

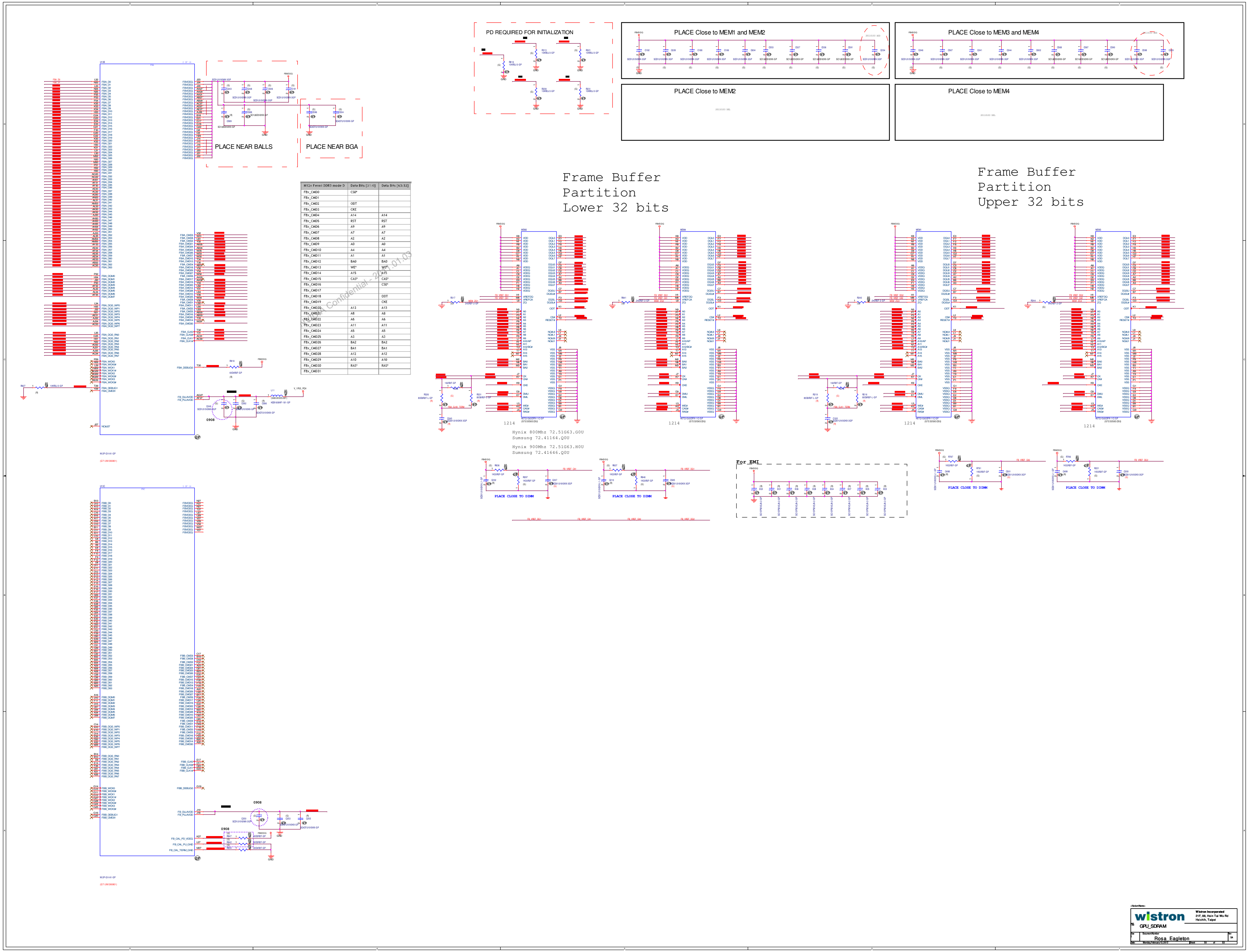
Title: 1D8V POWER		
Size: Custom	Document Number: Rosa_Eagleton	Rev: SA
Date: Monday, February 13, 2012	Sheet 48 of 53	



<VariantName>

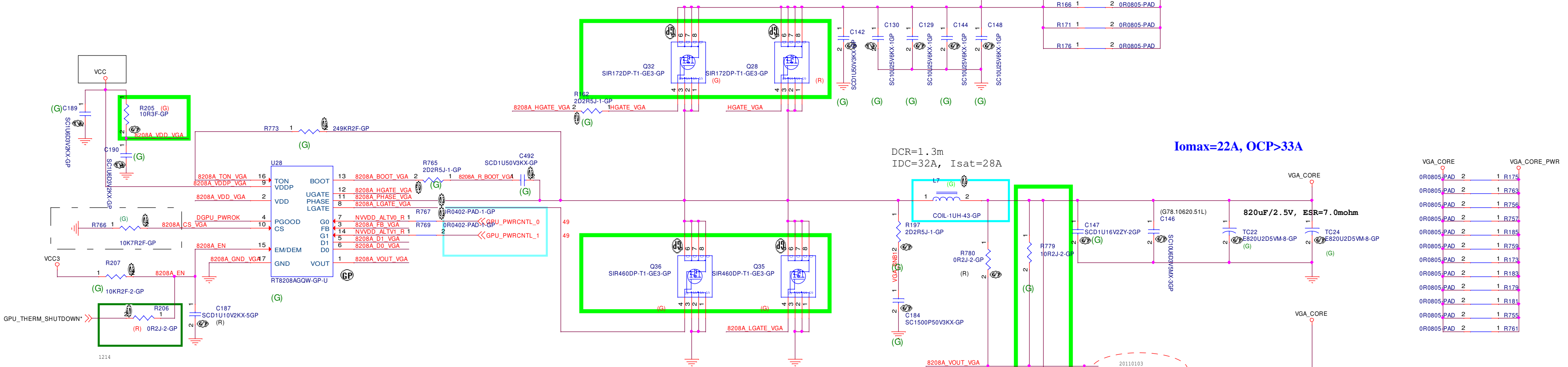
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	GPU_SDRAM		
Size: Custom	Document Number: Rosa_Eagleton		Rev: SA
Date:	Monday, February 13, 2012	Sheet 49 of 53	



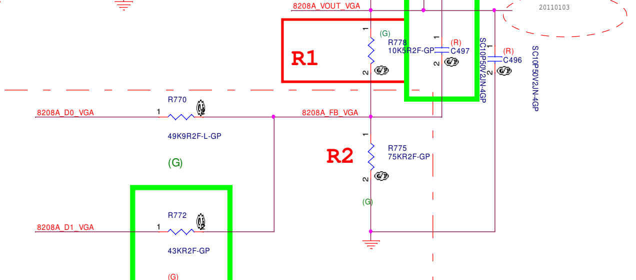
N12x Fermi DDR3 mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0*	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	A15	A15
FBx_CMD15	CAS*	CAS*
FBx_CMD16		CS0*
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS*	RAS*
FBx_CMD31		

RT8208A for GPU CORE POWER



9/13

P-State	GPU_PWRCNTL_0 GPIO5 (G0)	GPU_PWRCNTL_1 GPIO6 (G1)	VGA_CORE_PWR
P8	LOW	LOW	0.85V
P0-HOT	HIGH	LOW	1V
P0-COLD	LOW	HIGH	1.025V
	HIGH	HIGH	



Vout = 0.75*(1+R1/R2)

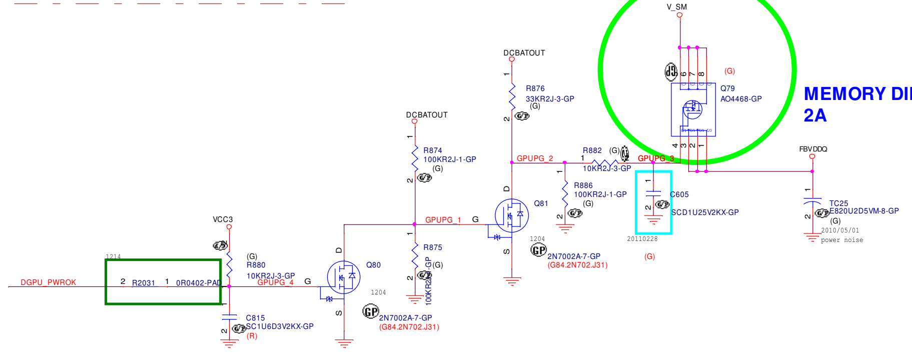
11M-32.4K(64.32425.6DL)
11P-49.9K(64.49925.6DL)

for 40nm GPU
32.4K of N11M
49.9K of N11P

20110103
GPU VCORE -> MEMORY POWER

RT9025 for 1D8V_VGA

+3VS to 1.8V Transfer



MEMORY DIE_S0
2A

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	GPU_CORE(RT8208A)	
Size Custom	Document Number Rosa_Eagleton	Rev SA
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<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
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wistron	**Wistron Incorporated** 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	TBD
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