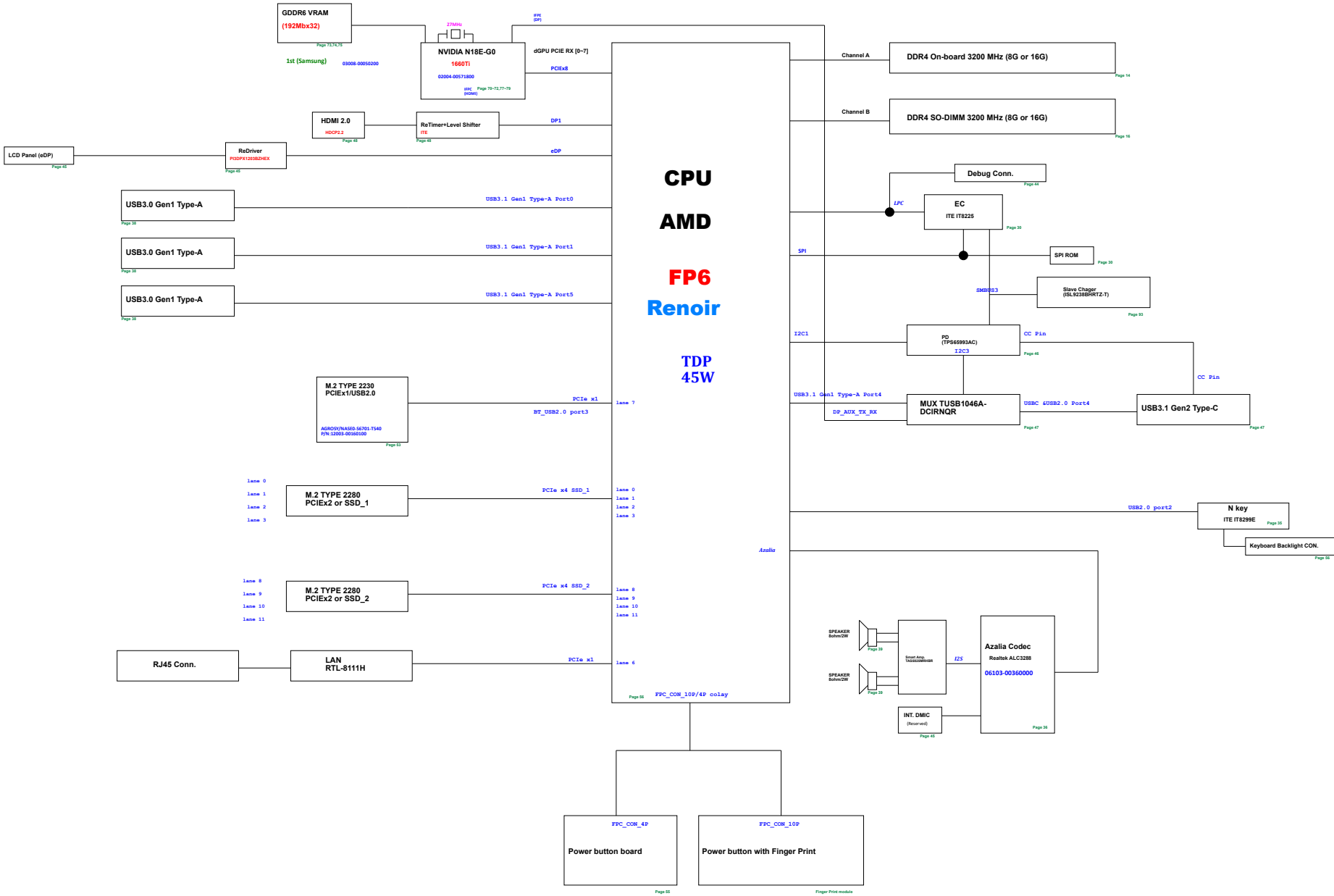
GA502IU AMD+NVIDIA Block Diagram

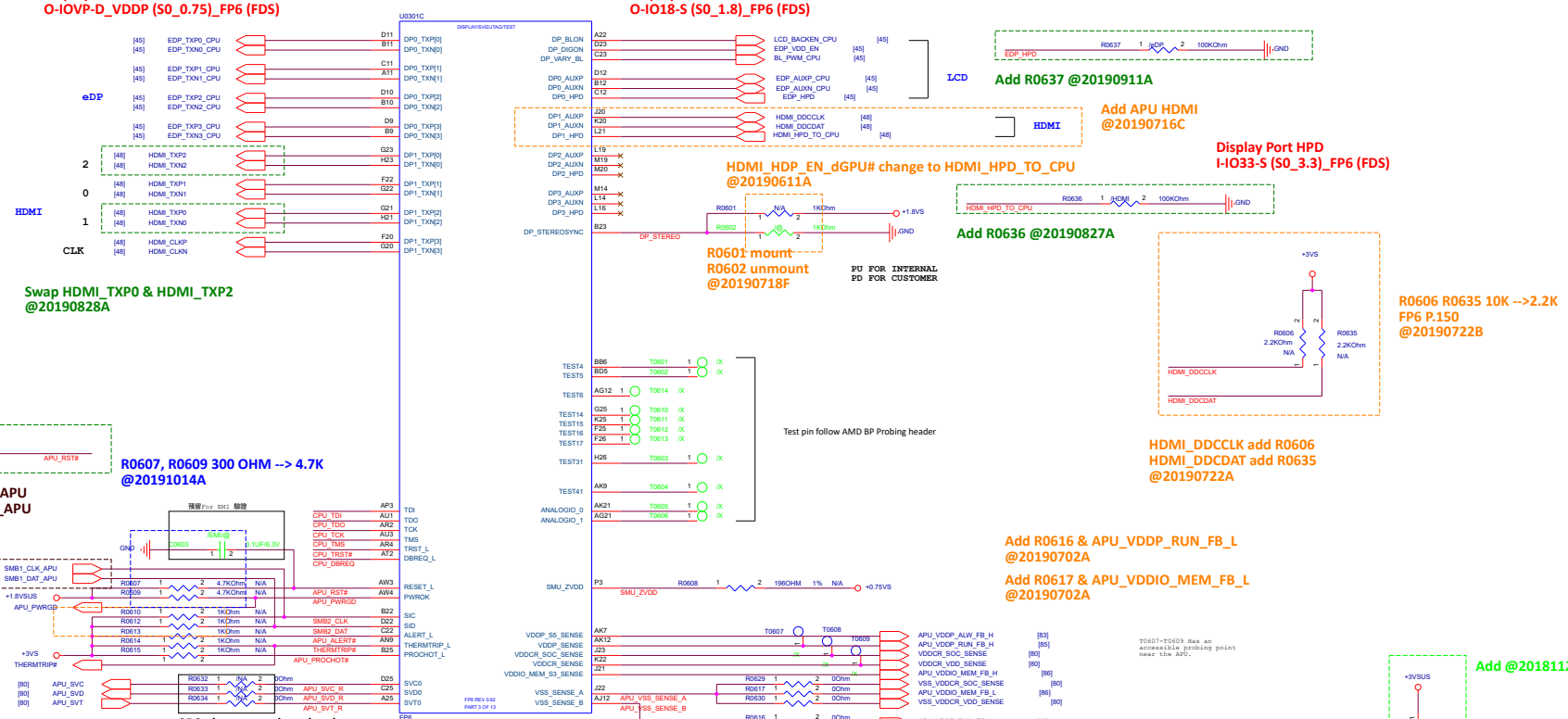


ASUS	Project Name: G703GI		Rev: R1.0
Title : CFL-H_Block Diagram_R1.3B			
Issued Date	Dept.:	Engineer:	NB1 RD2 EE1
Confidential			
Date: Tuesday, April 09, 2019	Sheet: 1	of: 94	

Display

Display Port TX/RX
O-IOVP-D_VDDP (S0_0.75)_FP6 (FDS)

Display Panel
O-IO18-S (S0_1.8)_FP6 (FDS)



Add R0637 @20190911A

Add APU HDMI
@20190716C

Display Port HPD
I-IO33-S (S0_3.3)_FP6 (FDS)

HDMI_HDP_EN_dGPU# change to HDMI_HPD_TO_CPU
@20190611A

Add R0636 @20190827A

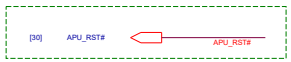
R0601 mount
R0602 unmount
@20190718F

PU FOR INTERNAL
PD FOR CUSTOMER

Swap HDMI_TXP0 & HDMI_TXP2
@20190828A

R0606 R0635 10K -->2.2K
FP6 P.150
@20190722B

Add @20190904A



R0607, R0609 300 OHM --> 4.7K
@20191014A

SMB2_CLK --> SMB1_CLK_APU
SMB2_DAT --> SMB1_DAT_APU
@20191119C

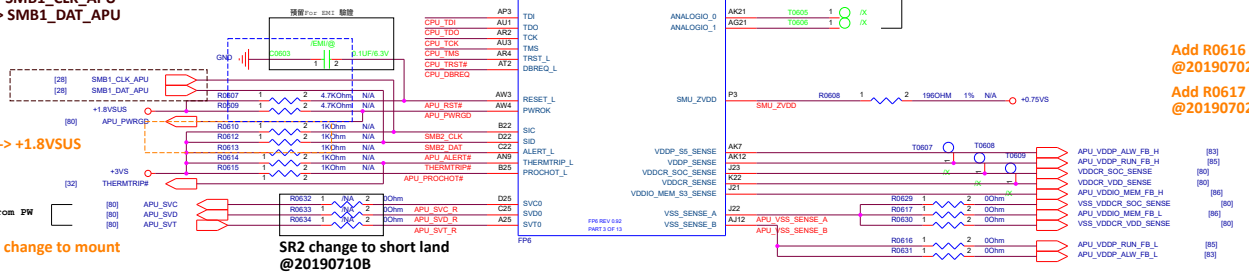
HDMI_DDCCLK add R0606
HDMI_DDCDAT add R0635
@20190722A

Test pin follow AMD BP Probing header

Add R0616 & APU_VDDP_RUN_FB_L
@20190702A

Add R0617 & APU_VDDIO_MEM_FB_L
@20190702A

R0609 +1.8VS --> +1.8VSUS
@20190722D

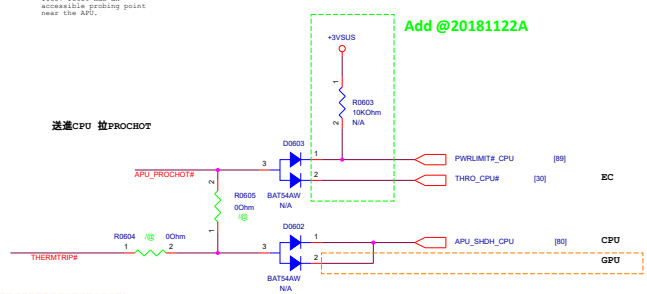


R0610, R0612 change to mount
@20190621C

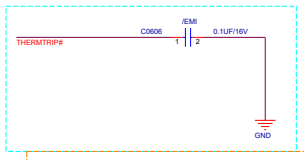
SR2 change to short land
@20190710B

APU_VDDP_ALW_FB_L
@20190626E

Add @20181122A

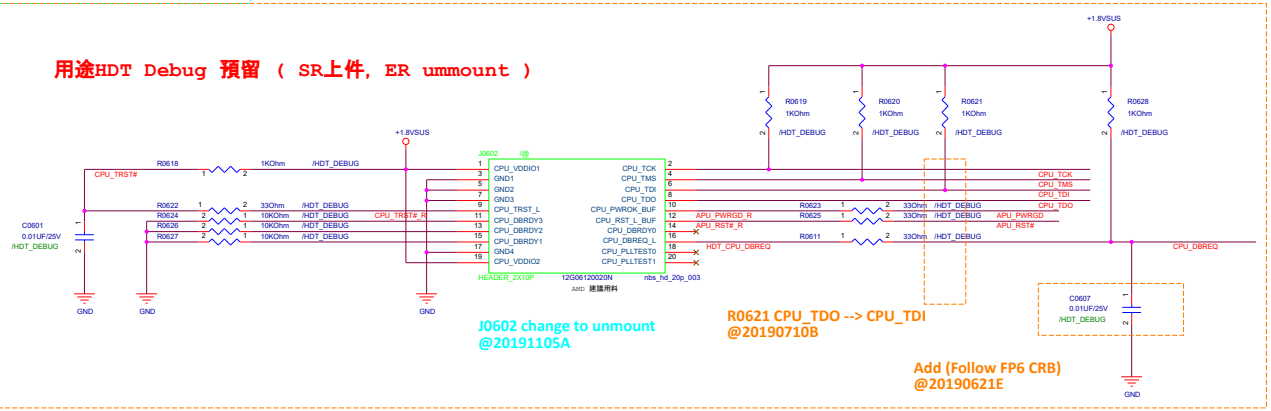


Add @20181219B (EMI request)



J0602 hd_2x10p_50_sam_nomask change to nbs_hd_20p_003
@20190618A

用途HDT Debug 預留 (SR上件, ER ummount)



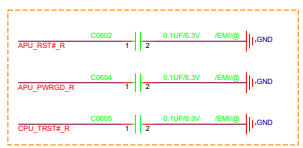
J0602 change to unmount
@20191105A

R0621 CPU_TDO --> CPU_TDI
@20190710B

Add (Follow FP6 CRB)
@20190621E

與POWER討論此PIN改由SW動作拉降頻(cost down)
故此PIN不接
P.30 &P.78 DGPU_LIMIT
@20181015E

Add @20181026A (EMI) request



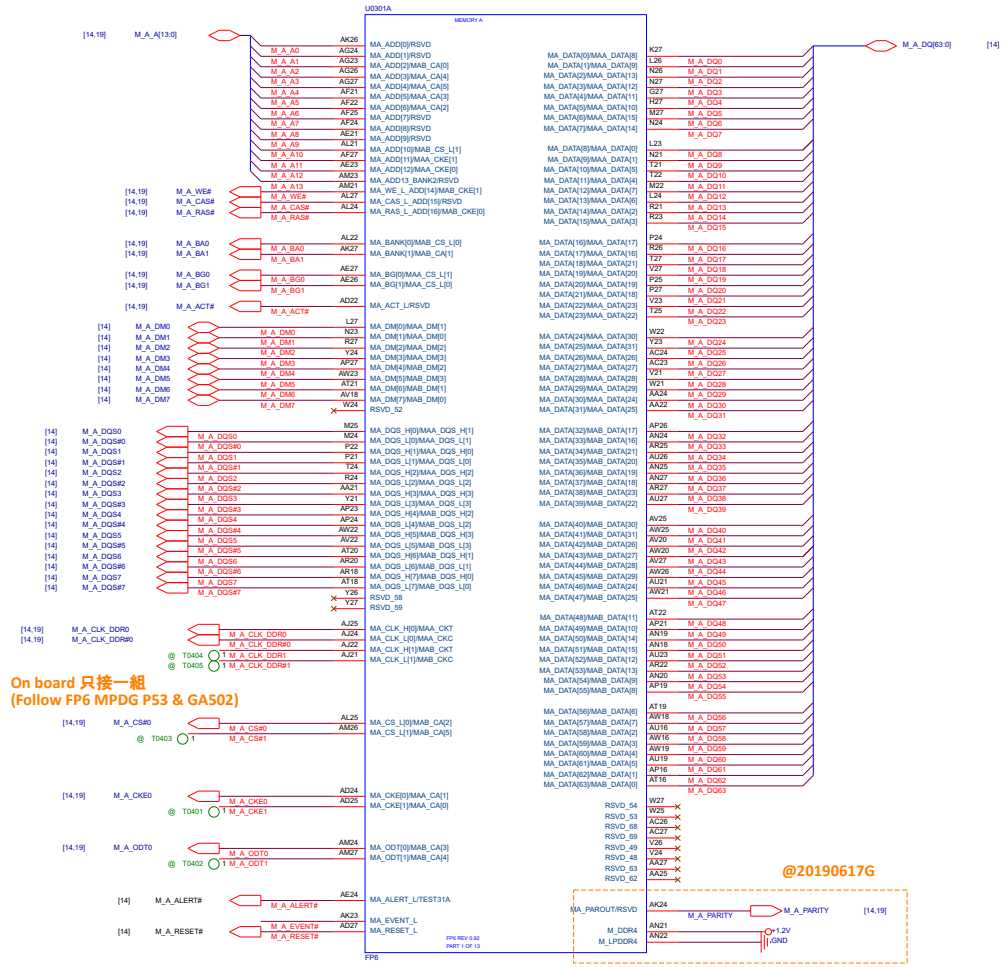
<Variant Name>

ASUS	Project Name: FX505DY	Rev: R1.0
Title :		
Size: C	Dept.: NB-SZ-RD3	Engineer:
Date: Tuesday, April 28, 2020	Sheet 6 of 104	

Memory Channel A

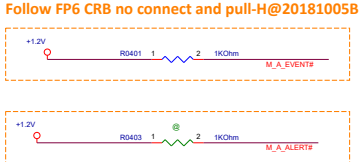
On Board DDR4

MA/B_
I/O-IOMEM-S/D VDDIO_MEM_S3 (S0_1.2)_FP6 (FDS)



On board 只接一組
(Follow FP6 MPDG P53 & GA502)

Follow FP6 CRB no connect and pull-H@20181005B



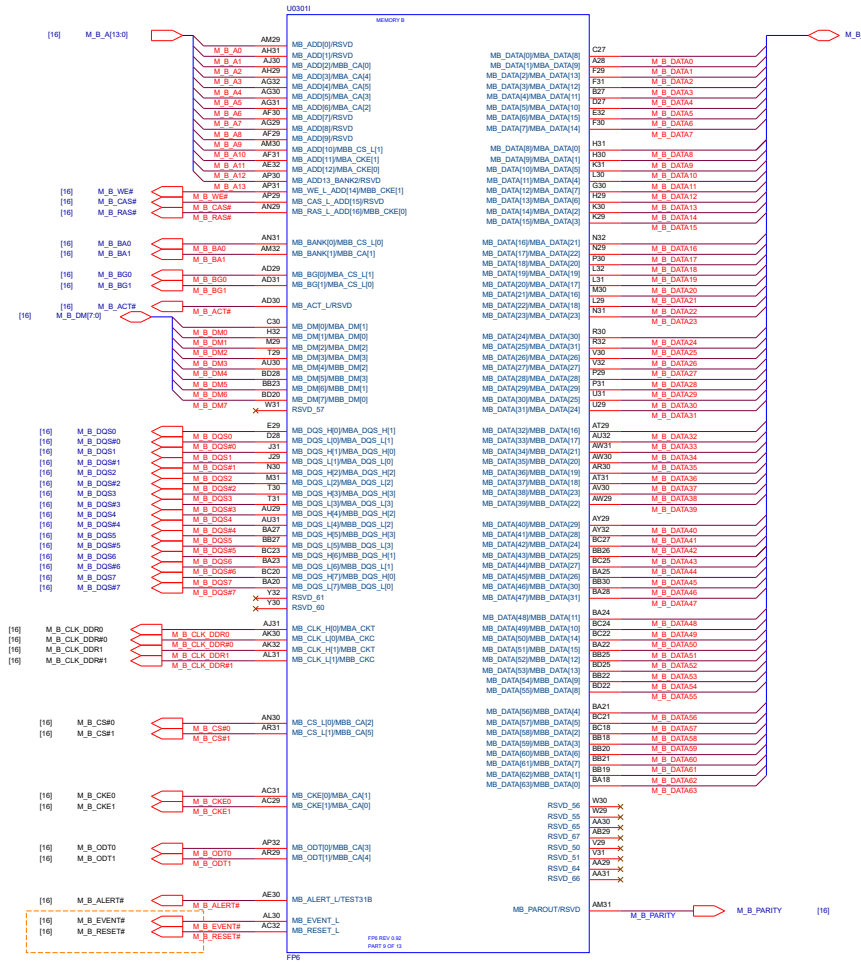
FP6 CRB預留不上

@20190617G

Memory Channel B

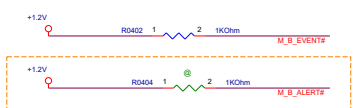
Main Board

SO-DIMM DDR4



EVENT# 對接pull-H +1.2V (FP6 CRB)

RESET# only對接 (FP6 CRB)



FP6 CRB預留不上

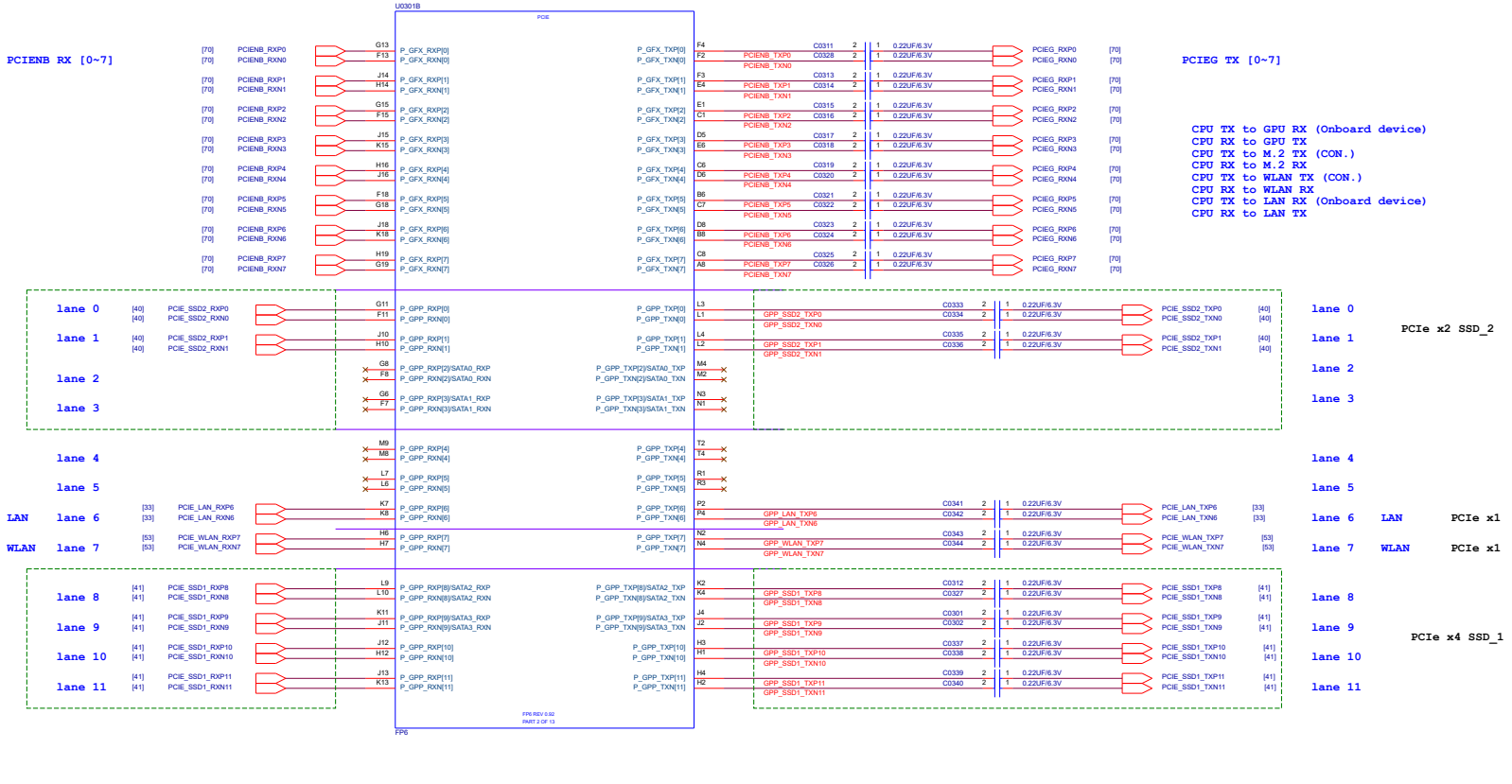
No Connect Fllow 17880D34747_FP5_Processor Motherboard Design_Guide

Project Name: FX505DY		Rev: R1.0
Title: AMD_CPU_DDR4		
Size: C	Dept.: ASUSTeK COMPUTER INC	Engineer: NB1 RD EE
Date: Tuesday, April 28, 2020	Sheet 4 of 104	

PCIE/WLAN/LAN/SSD

RX Side

TX Side



CPU TX to GPU RX (Onboard device)
CPU RX to GPU TX
CPU TX to M.2 TX (CON.)
CPU RX to M.2 RX
CPU TX to WLAN TX (CON.)
CPU RX to WLAN RX
CPU TX to LAN RX (Onboard device)
CPU RX to LAN TX

Project Name	FX505DY	Rev R1.0
Title :	CFL-H_CPU_DMI,PEG,FDI,eDP,DDI_R1.3B	
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1
Date: Tuesday, April 28, 2020	Sheet 3 of 104	

Project Name: GX502GX		Rev: R1.2
Title : CYPRESS CCG4		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: EE	
Date: Tuesday, April 28, 2020	Sheet 12 of 104	

Title <Title>		
Size A	Document Number <Doc>	Rev R1.0
Date: Tuesday, April 28, 2020	Sheet 13 of 104	

I2C/RST/GPIO/AZ

Delete RN0701, I2C1_SCL I2C1_SDA
@20191014D

Delete R0701, R0705 @20190829C

Delete @20190927A

Add R0741 @20190902A

I2C1 I2C0 PU +3VS
@20190722G

R0729 10K change to 2.2K
@20191230A

For SMBUB0

R0702 mount @20190822A

RSMRST_L_S5_1.8_FP6 (FDS)
PCIE_RST_O-IO33S5-S_FP6 (FDS)

DP_HPD_event#
Pull-H +3VSUS--> +3VS
@20191126A

PU +3.3V_ALW
(FP6 CRB)

Add @20190828B

DDR4_SPD_CLK/DATA

Add @20190927A
Delete I2C1_SDA, I2C1_SCL, I2C1_PD_IRQ#
@20191014D

For SMBUB1

Add @20190829C

DDR4

Tocuh pad

change @20200413A

Add @20190829C

EGPIO42 EXT_SMI# --> T0704
@20190910A

AGPIO5 T0703 --> EXT_SMI#
@20190910A

PD1_I2C_INT_APU --> I2C1_PD_IRQ#
@20190718E

Delete R0732 @20190902A

AZ_B-AUD-S (S5_1.8)_FP6 (FDS)

DP_HPD_event# : AGPIO5 --> AGPIO91
Add T0703
@20190909A

EXT_SMI# AGPIO40 --> EGPIO42
PCIE_SSD_RST# EGPIO42 --> AGPIO40
@20190710E

Audio

GC6 (S0_3.3)
@20190717D

@20181013B

Add @20190708C

DGPU_PWR_EN# (AGPIO84) --> T0701
DGPU_PWROK (AGPIO85) --> T0702
@20190903A

DGPU_PWROK change to AGPIO84
Delete T0701
@20190909D

Add @20190829C

Change @20190710E

Onboard Memory PCB-ID:
AGPIO6 =>DIMM_SEL0
AGPIO4 =>DIMM_SEL1

Delete R0723, R0724
Delete DIMM_SEL2 (AGPIO10)
@20190829B

DDR4 Memory Down pool

	Samsung (1024*8)	Samsung (2048*8)	Micron (1024*8)	Micron (2048x8)
	03012-00031000 DDR4 3200 1024M*8 1.2V K4A8G085WC-BCWE	03012-00060100 DDR4 3200 2048M*8 1.2V K4AAG085WA-BCWE	03012-00030900 Micron DDR4 3200 MT40A1G8SA-062E:J	03012-00060300 Micron DDR4 3200 MT40A2G8TA-062E:B
DIMM_SEL0	L	H	L	H
DIMM_SEL1	L	H	H	L

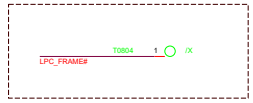
Change @20200102A

<Variant Name>

ASUS	Project Name: FX505DY	Rev: R1.0
Title :		
Size: C	Dept.: NB-SZ-RD3	Engineer:
Date: Tuesday, April 28, 2020	Sheet 7 of 104	

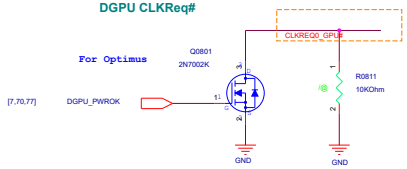
CPU_CLK

Add @20191127A



DGPU CLKReq#

For Optimus



CLKREQ6_GPU# --> CLKREQ0_GPU#
@20190624A

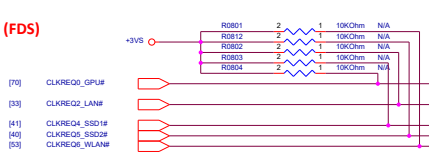
CLK_REQ
B-IO33-S (S0_3.3)_FP6 (FDS)

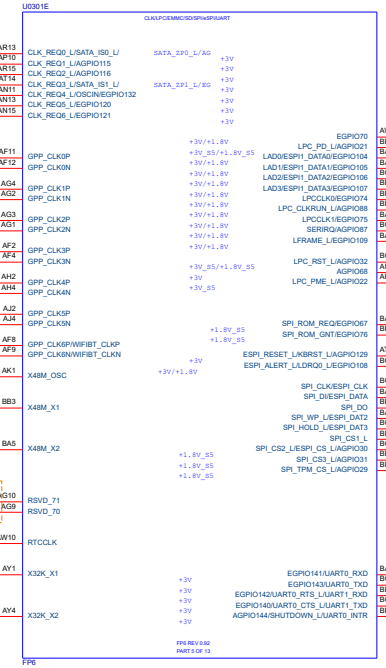
@20190624A

CLKREQ6_GPU# --> CLKREQ0_GPU#

CLKREQ0_SSD1# --> CLKREQ4_SSD1#
CLKREQ3_SSD2# --> CLKREQ5_SSD2#

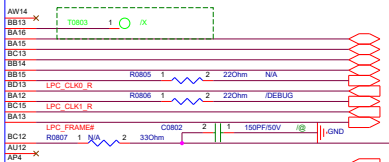
CLKREQ1_WLAN# --> CLKREQ6_WLAN#





Delete AGPIO21_HDMI_HDP_EN_dGPU#
Delete R0823
@20190716C

Delete port LPC_PD, Add T0803
@20190910B



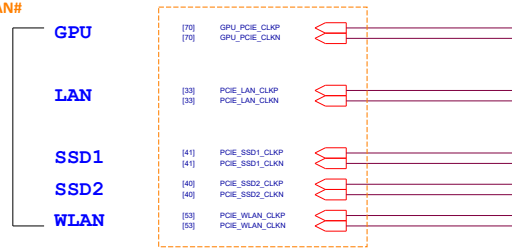
EGPIO104-107_S0_1.8/3.3_FP6 (FDS)

LPC

EGPIO74/75_S0_1.8/3.3_FP6 (FDS)
AGPIO88_S5_1.8/3.3
EGPIO109_S5_1.8/3.3
APGIO32_S5_1.8/3.3_FP6 (FDS)

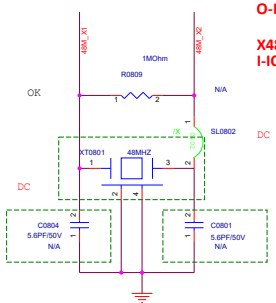
PCIE_CLK P/N
後端記得預留0 ohm

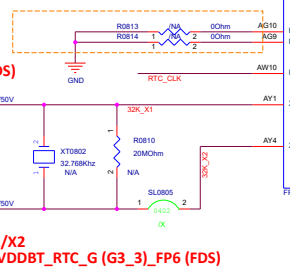
GPU
LAN
SSD1
SSD2
WLAN



GPP_CLK
O-IOVP-D_VDDP (S0_0.75)_FP6 (FDS)

X48M_X1/X2
I-IOVPS5-S_VDDP (S5_0.75)_FP6 (FDS)



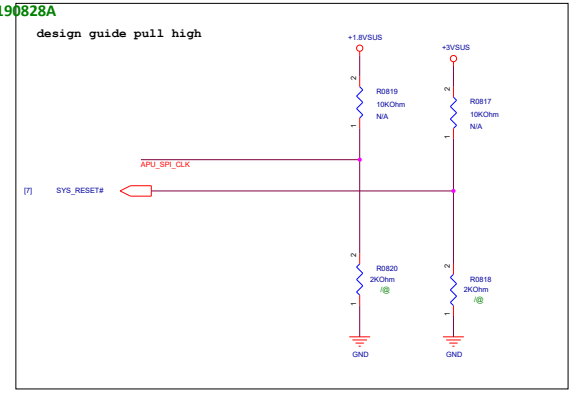


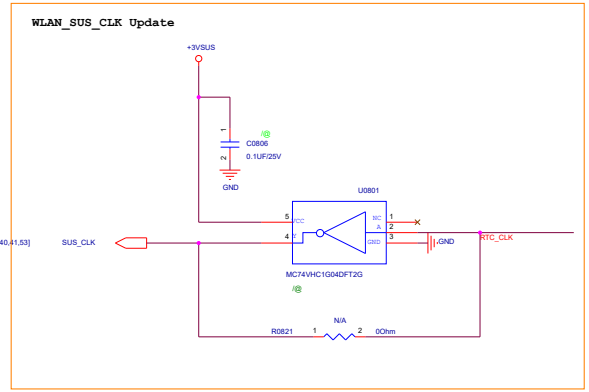
RTCCLK
O-IO18S5-S (S5_1.8)_FP6 (FDS)

X32K_X1/X2
I-RTC-S_VDDBT_RTC_G (G3_3)_FP6 (FDS)

C0804, C0801 3.9PF -->5.6PF
@20190910C

XT0801 07009-00090700 --> 07009-00095500
@20190828A





Add R0823 to +1.8VS (AMD comment)
R0815 --> unmount
@20190827A

R0815 --> mount
R0823 --> unmount
@20190910D

SPI

Add R0816
@20190801B

Delete port: ESI_ALERT_L
@20190910B

UART0/1_S0_3.3_FP6 (FDS)

Add T0801 & T0802 for UART debug
@20190909C

DGPU

DGPU_PWROK (EGPIO142) --> UART0_RTS
DGPU_PWR_EN# (EGPIO140) --> UART0_CTS
@20190909D

<variant_name>

ASUS	Project Name: FX505DY	Rev: R1.0
Title :		
Size: C	Dept.: NB-SZ-RD3	Engineer:
Date: Tuesday, April 28, 2020	Sheet 8 of 104	

PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	ACZRST	Native	SC_ID#		PU 10K	+3VS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_EMCPCI_PCH_R1			
GPP_A10	CLKOUT_LPC1	Native	CLK_DEBUG_R1			
GPP_A11	PME#	GPO	(N.C)			
GPP_A12	GPI	GPO	(N.C)			
GPP_A13	SUSWARN0#	Native	WL_PonPerOnAck		PU 10K(@)	+3VSUS
GPP_A14	SUS_STAT#	Native	PCH_SUS_STAT#			
GPP_A15	SUS_ACK#	Native	PM_SUSACK#			
GPP_A16	Native/GPI	GPO	(N.C)			
GPP_A17	GPI	GPO	(N.C)			
GPP_A18	GPI	GPO	(N.C)			
GPP_A19	GPI	GPO	(N.C)			
GPP_A20	GPI	GPO	(N.C)			
GPP_A21	GPI	GPO	SATA_MEDSET(Reserved)			
GPP_A22	GPI	GPO	PCH_BTO3_CIO_PWR_EN		PU 10K	+VCC3V3_SX
GPP_A23	GPI	GPO	PCH_BTO3_USB_PWR_EN		PD 100K	

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	(N.C)			
GPP_B1	GPI	GPI	TP47_I2C_INT_PCH		PU 10K	+3VSUS
GPP_B2	GPI	GPO	(N.C)			
GPP_B3	GPI	GPO	(N.C)			
GPP_B4	GPI	GPO	(N.C)			
GPP_B5	GPI	Native	CLK_REQ0#/CLKREQ0_PEGA#		PU 10K	+3VSUS
GPP_B6	GPI	Native	CLK_REQ1#		PU 10K(@)	+3VSUS
GPP_B7	GPI	Native	CLK_REQ2#/CLKREQ2_WLAN_AC#		PU 10K	+3VSUS
GPP_B8	GPI	Native	CLK_REQ3#		PU 10K(@)	+3VSUS
GPP_B9	GPI	Native	CLK_REQ4#/CLKREQ4_GLAN#		PU 10K	+3VSUS
GPP_B10	GPI	Native	CLK_REQ5#/CLKREQ5_TBT #		PU 10K	+3VSUS
GPP_B11	GPO	GPO	(N.C)			
GPP_B12	SLP_S0#	Native	SLP_S0#			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPP_B14	PD		
GPP_B15	GPI	GPI	PCH_GPP_B15/KB_LANG_ID0		PU 10K	+3VS
GPP_B16	GPI	GPI	PCH_GPP_B16/KB_LANG_ID1		PU 10K	+3VS
GPP_B17	GPI	GPO	PCH_GPP_B17/DRAM_RST#		PU 10K	
GPP_B18	GPO	Strap	PCH_GPP_B18	PD		
GPP_B19	GPI	GPO	PCH_GPP_B19/BT_ON_PCH		PD 10K(@)	
GPP_B20	GPI	GPO	PCH_GPP_B20/GPIOEVENT#_PCH		PU 10K	+3VSUS
GPP_B21	GPI	GPI	PCH_GPP_B21/GC6FAIN_PCH		PU 10K(@)	+3VS
GPP_B22	GPO	Strap	PCH_GPP_B22	PD		
GPP_B23	GPO	Native	SML1ALERT#	PD	PU 150K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		PU 2.2K	+3VSUS
GPP_C2	GPO	GPI	GPP_C2_BT_UART_WAKE_N	PD	PU 4.7K	+3VSUS
GPP_C3	SMLOCLK	Native	SMLO_CLK (Reserved)		PU 2.2K	+3VSUS
GPP_C4	SMLOGATA	Native	SMLO_DAT (Reserved)		PU 2.2K	+3VSUS
GPP_C5	GPO	Strap	PCH_GPP_C5	PD		
GPP_C6	SMLICLK	Native	SMLI_CLK		PU 2.2K	+3VSUS
GPP_C7	SMLIDATA	Native	SMLI_DAT		PU 2.2K	+3VSUS
GPP_C8	GPI	GPO	(N.C)			
GPP_C9	GPI	GPO	(N.C)			
GPP_C10	GPI	GPO	(N.C)			
GPP_C11	GPI	GPO	(N.C)			
GPP_C12	GPI	GPI	DIMM_SEL0			
GPP_C13	GPI	GPI	DIMM_SEL1			
GPP_C14	GPI	GPI	DIMM_SEL2			
GPP_C15	GPI	GPI	NFC_IO		PU 10K	+3VSUS
GPP_C16	GPI	Native	TBT_I2C_SDA_PCH		PU 2.2K	+3VSUS
GPP_C17	GPI	Native	TBT_I2C_SCL_PCH		PU 2.2K	+3VSUS
GPP_C18	GPI	Native	I2C1_SDA		PU 2.2K	+3VS
GPP_C19	GPI	Native	I2C1_SCL		PU 2.2K	+3VS
GPP_C20	GPI	GPI	PCH_GPP_C20/DGPU_PWROK		PU 10K	+3VS_WO
GPP_C21	GPI	GPO	PCH_GPP_C21/GPU_RST#		PD 10K	
GPP_C22	GPI	GPO	(N.C)			
GPP_C23	GPI	GPI	CPAD_INT#		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GPI	GPO	(N.C)			
GPP_D1	GPI	GPO	(N.C)			
GPP_D2	GPI	GPO	(N.C)			
GPP_D3	GPI	GPO	(N.C)			
GPP_D4	GPI	GPO	(N.C)			
GPP_D5	GPI	Native	PCH_BTO3_PCH_DP_HPD_R			
GPP_D6	GPI	Native	PCH_BTO3_PCH_DP_AUXP_R			
GPP_D7	GPI	Native	PCH_BTO3_PCH_DP_AUXN_R			
GPP_D8	GPI	GPO	PCH_BTO3_PCH_DP_LANE0_R		PD 75K	
GPP_D9	GPI	Native3	PCH_BTO3_PCH_DP_LANE1_R		PD 75K	
GPP_D10	GPI	Native3	PCH_BTO3_PCH_DP_LANE2_R		PD 75K	
GPP_D11	GPI	GPO	PCH_BTO3_PCH_DP_LANE3_R		PD 75K	
GPP_D12	GPI	GPO	PCH_BTO3_PCH_DP_AUXP_R		PD 100K(@)	
GPP_D13	GPI	GPO	PCH_BTO3_PCH_DP_AUXN_R			
GPP_D14	GPI	GPO	(N.C)			
GPP_D15	GPI	GPO	(N.C)			
GPP_D16	GPI	GPO	(N.C)			
GPP_D17	GPI	GPO	(N.C)			
GPP_D18	GPI	GPO	(N.C)			
GPP_D19	GPI	GPO	(N.C)			
GPP_D20	GPI	GPO	(N.C)			
GPP_D21	GPI	GPO	(N.C)			
GPP_D22	GPI	GPO	(N.C)			
GPP_D23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	GPI	Native	SATAXPCIE_DET0		PU 10K(@)	+3VS
GPP_E1	GPI	Native	SATAXPCIE_DET1		PU 10K	+3VS
GPP_E2	GPI	Native	SATAXPCIE_DET2		PU 10K(@)	+3VS
GPP_E3	GPI	GPI	EXT_SMI#		PU 10K	+3VS
GPP_E4	GPI	Native	SATA0_ACG1 DEVSLP		PU 10K(@)	+3VS
GPP_E5	GPI	Native	SATA1_HGPF3_DEVSLP		PU 10K(@)	+3VS
GPP_E6	GPI	Native	HGPF3_DEVSLP		PU 10K(@)	+3VSUS
GPP_E7	GPI	GPI	EXT_SCI#		PU 10K	+3VS
GPP_E8	GPI	Native	SATA_LED#		PU 10K	+3VS
GPP_E9	GPI	Native	USB_OC#0		PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1		PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2		PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3		PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	GPI	Native	SATAXPCIE_DET3		PU 10K(@)	+3VS
GPP_F1	GPI	Native	SATAXPCIE_DET4		PU 10K	+3VS
GPP_F2	GPI	GPO	(N.C)			
GPP_F3	GPI	GPO	(N.C)			
GPP_F4	GPI	GPO	(N.C)			
GPP_F5	GPI	GPO	(N.C)			
GPP_F6	GPI	GPO	(N.C)			
GPP_F7	GPI	GPO	(N.C)			
GPP_F8	GPI	GPO	(N.C)			
GPP_F9	GPI	GPO	(N.C)			
GPP_F10	GPI	GPO	(N.C)			
GPP_F11	GPI	GPO	(N.C)			
GPP_F12	GPI	GPO	(N.C)			
GPP_F13	GPI	GPO	(N.C)			
GPP_F14	GPI	GPO	(N.C)			
GPP_F15	GPI	Native	USB_OC#4		PU 10K	+3VSUS
GPP_F16	GPI	Native	USB_OC#5		PU 10K	+3VSUS
GPP_F17	GPI	Native	USB_OC#6		PU 10K	+3VSUS
GPP_F18	GPI	Native	USB_OC#7		PU 10K	+3VSUS
GPP_F19	GPI	GPO	(N.C)			
GPP_F20	GPI	GPO	(N.C)			
GPP_F21	GPI	GPO	(N.C)			
GPP_F22	GPI	GPO	(N.C)			
GPP_F23	GPI	GPO	PCH_GPPF23		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_G0	GPI	GPO	(N.C)			
GPP_G1	GPI	GPO	(N.C)			
GPP_G2	GPI	GPO	(N.C)			
GPP_G3	GPI	GPO	(N.C)			
GPP_G4	GPI	GPO	(N.C)			
GPP_G5	GPI	GPO	(N.C)			
GPP_G6	GPI	GPO	(N.C)			
GPP_G7	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	GPI	Native	CLK_REQ6#/CLKREQ6_HGPF1#		PU 10K	+3VSUS
GPP_H1	GPI	Native	CLK_REQ7#/CLKREQ7_HGPF2#		PU 10K	+3VSUS
GPP_H2	GPI	Native	CLK_REQ8#/CLKREQ8_HGPF3#		PU 10K	+3VSUS
GPP_H3	GPI	Native	CLK_REQ9#		PU 10K(@)	+3VSUS
GPP_H4	GPI	Native	CLK_REQ10#		PU 10K(@)	+3VSUS
GPP_H5	GPI	Native	CLK_REQ11#		PU 10K(@)	+3VSUS
GPP_H6	GPI	Native	CLK_REQ12#		PU 10K(@)	+3VSUS
GPP_H7	GPI	Native	CLK_REQ13#		PU 10K(@)	+3VSUS
GPP_H8	GPI	Native	CLK_REQ14#		PU 10K(@)	+3VSUS
GPP_H9	GPI	Native	CLK_REQ15#		PU 10K(@)	+3VSUS
GPP_H10	GPI	GPO	(N.C)			
GPP_H11	GPI	GPO	(N.C)			
GPP_H12	GPO	GPO	(N.C)	PD	PU 20K(@)	
GPP_H13	GPI	GPO	(N.C)			
GPP_H14	GPI	GPO	(N.C)			
GPP_H15	GPI	GPO	SML3ALERT#		PU 100K	+3VSUS
GPP_H16	GPI	GPI	HSIO_0			
GPP_H17	GPI	GPI	HSIO_1			
GPP_H18	GPI	GPI	HSIO_2			
GPP_H19	GPI	GPO	(N.C)			
GPP_H20	GPI	GPO	(N.C)			
GPP_H21	GPI	GPO	(N.C)			
GPP_H22	GPI	GPO	(N.C)			
GPP_H23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GPI	GPO	(N.C)			
GPP_I1	GPI	GPO	(N.C)			
GPP_I2	GPI	GPO	(N.C)			
GPP_I3	GPI	GPO	(N.C)			
GPP_I4	CNV_RGI_DT	Native	CNV_RGI_DT		PU 4.7K	+1.8VSUS
GPP_I5	CNV_RGI_RSP	Native	CNV_RGI_RSP		PU 20K(@)	+1.8VSUS
GPP_I6	CNV_RGI_DT	Native	CNV_RGI_DT		PU 75K	
GPP_I7	CNV_RGI_RSP	Native	CNV_RGI_RSP		PU 20K(@)	+1.8VSUS
GPP_I8	GPO	GPO	(N.C)			
GPP_I9	GPO	GPO	(N.C)			
GPP_I10	GPI	GPO	(N.C)			
GPP_I11	A4WP_PRESENT	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_J0	GPI	GPO	(N.C)			
GPP_J1	CPU_HSIO_PWR_GATE#	Native	CPU_C10_GATE#_PCH		PU 100K	+1.8VSUS
GPP_J2	GPI	GPO	(N.C)			
GPP_J3	GPI	GPO	(N.C)			
GPP_J4	CNV_RGI_DT	Native	CNV_RGI_DT		PU 4.7K	+1.8VSUS
GPP_J5	CNV_RGI_RSP	Native	CNV_RGI_RSP		PU 20K(@)	+1.8VSUS
GPP_J6	CNV_RGI_DT	Native	CNV_RGI_DT		PU 75K	
GPP_J7	CNV_RGI_RSP	Native	CNV_RGI_RSP		PU 20K(@)	+1.8VSUS
GPP_J8	GPI	GPO	(N.C)			
GPP_J9	GPO	GPO	(N.C)			
GPP_J10	GPI	GPO	(N.C)			
GPP_J11	A4WP_PRESENT	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_K0	GPI	GPO	GPIO_3_FORCE_PWR		PU 100K	
GPP_K1	GPI	GPI	PCH_I2C		PU 10K	
GPP_K2	GPI	GPI	PCH_I2C		PU 10K	
GPP_K3	GPI	GPO	GPP_K3/WLAN_BT_LED		PU 100K	
GPP_K4	GPI	GPO	GPP_K4/WLAN_LED		PU 100K	
GPP_K5	GPI	GPO	VGL_DOMB#(N.C)			
GPP_K6	GPI	GPO	VGL_DPW(N.C)			
GPP_K7	GPI	GPO	GPP_K7/TPAD_WAKE#		PU 10K	+3VS
GPP_K8	GPI	GPO	GPP_K8/DGPU_PWR_EN#		PU 10K(@)	+3VS
GPP_K9	GPI	GPO	WLAN_OFF		PU 100K	
GPP_K10	Reserved	GPO	GPP_K10/WLAN1_RST#		PU 10K	+3VS
GPP_K11	Reserved	GPO	GPP_K11/SP_WAKE#		PU 10K	+3VS
GPP_K12	GPI	GPO	(N.C)			
GPP_K13	GPI	GPO	(N.C)			
GPP_K14	GPI	GPO	(N.C)			
GPP_K15	GPI	GPO	(N.C)			
GPP_K16	GPI	GPO	(N.C)			
GPP_K17	GPI	GPO	(N.C)			
GPP_K18	GPI	GPO	(N.C)			
GPP_K19	GPI	GPO	(N.C)			
GPP_K20	Reserved	GPO	(N.C)			
GPP_K21	Reserved	GPO	(N.C)			
GPP_K22	GPI	GPO	(N.C)			
GPP_K23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	PM_BATLOW#		PU 10K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_R1		PD 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	LAN_WAKE#(N.C)		PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#		PU 10K(@)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#		PD 100K	
GPD5	SLP_S4#	Native	SLP_S4#		PD 100K	
GPD6	SLP_A#	Native	SLP_A# (N.C)			
GPD7	GPO	GPO	PCH_GPD7		PU 10K	+3VA_DSW
GPD8	SUSCLK	Native	SUS_CLK#			
GPD9	SLP_WLAN#	Native	SLP_WLAN# (N.C)			
GPD10	SLP_S5#	Native	SLP_S5# (N.C)			
GPD11	LANPHYPC	GPO	LAN_PHYEN (N.C)		PU 10K(@)	+3VA_DSW

IT8225VG-128/BX GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	0	GPO	PWR_LED	PU 1M	
GPA1	OD	GPO	CHG_LED#		
GPA2	OD	GPO	CHG_FULL_LED#		
GPA3	Alt	PWM	FAN2_PWM		
GPA4	0	GPO	EC_GPA4(N.C)		
GPA5	Alt	PWM	FAN1_PWM		
GPA6	Alt	GPO	EC_GPA6(N.C)		
GPA7	0	GPO	EC_GPA7(N.C)		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_OC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	EC_GPB2(N.C)		
GPB3	Alt	GPI	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PB_ON_EC		
GPB5	0	GPO	EC_GPB5/RKey_WAIT	PU 10K	
GPB6	OD	GPO	EC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	0	GPO	EC_GPC0		
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	0	GPO	PM_PWRBTN#	PU 10K(@)	+3VSUS
GPC4	I	GPI	EC_GPC4/PM_SUSB#	PU 100K	
GPC5	I	GPI	PM_SUSC#	PU 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PU 100K	
GPC7	0	GPO	EC_GPC7/RKEY_PWR_EN	PU 10K(@)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	0	GPO	EC_GPD0/EC_CV_DIR		
GPD1	0	GPO	EC_GPD1/MB_AC_PRESENT		
GPD2	Alt	GPI	BUF_PLT_RST#	PD 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	0	GPO	EC_GPD5/GP_SI#		
GPD6	Alt	GPI	FAN1_TACH	PU 10K	+3VS
GPD7	Alt	GPI	FAN2_TACH	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	0	GPO	EC_GPE0/SUSB_EC#	PD 4.7K	
GPE1	0	GPO	EC_GPE1/SUSC_EC#	PD 4.7K	
GPE2	0	GPO	3.3V_ON		
GPE3	0	GPO	5VSUS_ON	PD 1M & PU 100K	+3VA_EC
GPE4	0	GPO	VSUS_ON	PD 1M & PU 100K	+3VA_EC
GPE5	I	GPO	5VALW_ON	PU 100K	+3VA_EC
GPE6	OD	GPO	WLAN_PWR_EN	PD 100K	
GPE7	OD	GPO	TURO_CPU#	PU 10K	+3VA_DSW

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	0	GPO	CAP_LED#		
GPF1	0	GPO	MUM_LED#		
GPF2	Alt	SMBus	P_SMB3_CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB3_DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	PECI	EC_PECI	PU 10K(@)	
GPF7	0	GPO	PCH_SPI_CS		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	0	GPO	DGPU_LIMIT		
GPG1	0	GPO	PCH_HSYNC#		
GPG2	I	GPI	EC_GPG2	PU 100K	+3VA_EC
GPG6	0	GPO	EC_GPG6(N.C)		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB3_CLK/TBT_I2C_SCL_EC	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB3_DAT/TBT_I2C_SDA_EC	PU 4.7K	+3VA_EC
GPH3	0	GPO	PM_SUSB#_P	PU 10K	
GPH4	0	GPO	SPWROK_EC	PU 10K	
GPH5	0	GPO	PM_PWROK	PU 10K	
GPH6	0	GPO	PM_SYSPWROK	PU 10K	
GPH7	0	GPO	LCD_BACKOFF#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_S03#	PU 100K(@)	
GPI1	I	GPI	3VSUS_PWRGD	PU 100K	+3VSUS
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3VS
GPI3	I	GPI	1HOVR_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD_EC	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN0#	PU 10K(@)	+3VSUS
GPI6	Alt	AD	A/D_MAX_POWER		
GPI7	Alt	AD	MB_MAX_POWER	PU 150K&PD 270K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	0	GPO	EC_GPJ0		
GPJ1	0	GPI	GC6FAIN_PCH	PU 10K(@)	+3VS
GPJ2	Alt	GPI	EC_GPJ2/PSTA_I2C_INT_EC		
GPJ3	0	GPO	EC_GPJ3/SSB_BC1.2_OFF#		
GPJ4	Alt	GPO	EC_GPJ4/USB30_5VSUS		
GPJ5	0	GPI	EC_GPJ5/MB_100K_SACK_DETECT	PU 100K(@)	+3VA
GPJ6	I	GPI	RKEY_INT#	PU 10K	+VSA_DSW_RKey/PWR
GPJ7	0	GPO	USB_CHARGE_OE#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/KIO0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/KIO1		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/KIO2		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/KIO3		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/EC		CLK_EMCPCI_PCH		
GPM5	LFRAME#/KCS#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

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G703GI Source:

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	**SM-Bus Address**
SO-DIMM A(0)	A0h
SO-DIMM B(0)	A4h
SO-DIMM A(1)	A2h
SO-DIMM B(1)	A6h
EC Master (SMB1)	**SM-Bus Address**
SM-Bus Device	
CPU INT. Thermal sensor	98h, 9Ch
CPU Thermal Sensor	90h
TI, TAS5766M*2	98h, 9Ah
AGM1562	66h
GPU (Thermistor sense)	74h
PWR(Thermistor sense)	76h, 7Ch, 7Ah, 78h, 7Eh

Device Identification

CPU Thermal Sensor		
1st	0h(0x31)/1h(0x33)	0h(0x77)/1h(0x79)
2nd		

SPU Thermistor		
1st	0h(0x1)/1h(0x3)/2h(0x5)	APL3512AB-TNG
2nd		

USB3.0/PCIE/SATA Setting

1	USB3@1	
2	USB3@2	
3	USB3@3	USB Port1
4	USB3@4	
5	USB3@5	USB Port3
6	USB3@6	USB Port4
7	USB3@7	Card Reader
8	PCIE@2	
9	PCIE@3	
10	PCIE@4	
11	PCIE@5	
12	PCIE@6	ThunderBolt x4
13	PCIE@7	
14	PCIE@8	
15	PCIE@9	
16	PCIE@10	PCIE3.0 x 4 SSD
17	PCIE@11	
18	PCIE@12	
19	PCIE@13(SATA@0)	SATA HDD
20	PCIE@14(SATA@1)	
21	PCIE@15	GLAN
22	PCIE@16	WLAN_11AC
23	PCIE@17	
24	PCIE@18	PCIE3.0 x 4 SSD
25	PCIE@19	
26	PCIE@20	
27	PCIE@21	
28	PCIE@22	PCIE3.0 x 4 SSD
29	PCIE@23	
30	PCIE@24	

USB2.0 Setting

1	USB2@1	
2	USB2@2	
3	USB2@3	USB Port1
4	USB2@4	
5	USB2@5	USB Port3
6	USB2@6	USB Port4
7	USB2@7	Card Reader
8	USB2@8	XBOX WLAN
9	USB2@9	Camera
10	USB2@10	M-Key
11	USB2@11	
12	USB2@12	Tobii IS4
13	USB2@13	TBT
14	USB2@14	BT

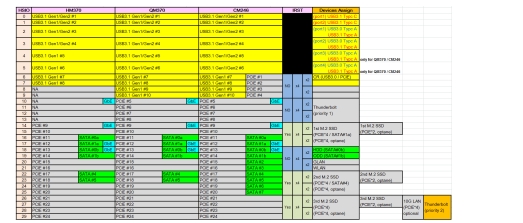

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Figure 14-1. High Speed I/O (HSIO) Lane Multiplexing in PCH-H

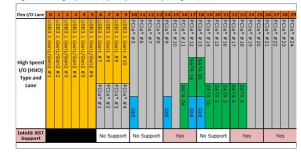

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Table 1-7. PCH HSIO Detail (SKU 8+11of 11)

Flex I/O Lane	SKU		
	HM370	QM370	CM246
0	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
3	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
4	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
5	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
6	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
7	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
8	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
9	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
10	GbE	PCIe*, GbE	PCIe*, GbE
11	N/A	PCIe*	PCIe*
12	N/A	PCIe*	PCIe*
13	N/A	PCIe*	PCIe*
14	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
15	PCIe*	PCIe*	PCIe*
16	PCIe*, SATA 0A	PCIe*, SATA 0A	PCIe*, SATA 0A
17	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A
18	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B
19	PCIe*, SATA 1B	PCIe*, SATA 1B	PCIe*, SATA 1B
20	PCIe*	PCIe*	PCIe*, SATA 2
21	PCIe*	PCIe*	PCIe*, SATA 3
22	PCIe*, SATA 4	PCIe*, SATA 4	PCIe*, SATA 4
23	PCIe*, SATA 5	PCIe*, SATA 5	PCIe*, SATA 5
24	PCIe*	PCIe*	PCIe*, SATA 6
25	PCIe*	PCIe*	PCIe*, SATA 7
26	PCIe*	PCIe*	PCIe*
27	PCIe*	PCIe*	PCIe*
28	PCIe*	PCIe*	PCIe*
29	PCIe*	PCIe*	PCIe*

Project Name	G703GI		Rev
Title :	CFL-R System Setting_R1.1E		R1.1
Size	Dept. :	Engineer:	NB1 RD2 EE1
Date: Tuesday, April 09, 2019	Sheet 1 of 130		

CPU_CAP

7pcs 22UF /1pcs 1uF/1pcs 180pF
@20190614E

+APU_VDDCORE_RUN

16pcs 22UF /1pcs 180pF
All BU(on bottom side under SOC)

+APU_VDDSOC_RUN

C1018,C1022,C1020 change to 22uF
@20190614E

All BU(on bottom side under SOC)

Follow FP6 CRB
@20190614E

C1083,C1082,C1067C1066C1065 change to unmount
@20190614E

+1.2V PI 模擬後的修改 total 5 close to CPU

+APU_VDDIO_SUS

9pcs 22uF /2pcs 1uF/1pcs 180pF
All BU(on bottom side under SOC)

+APU_VDDIO_SUS

ACROSS VDDIO AND VSS SPLIT

DECOUPLING BETWEEN PROCESSOR AND DIMMs

4pcs 0.22uF / 2pcs 180pF

All BU(on bottom side under SOC)

+APU_VDDCORE_RUN

TBD 4pcs 0.22uF / 2pcs 180pF

DECOUPLING BETWEEN PROCESSOR AND DIMMs ACROSS VDDIO AND VSS SPLIT

+APU_VDDIO_SUS

RESERVED FOR DEBUG

Add @20190617E

If the VSS plane is cut to create a VDDIO_MEM_S3 plane, ceramic capacitors with NP0 or C0G dielectric are connected across the VDDIO_MEM_S3 and VSS plane split.

+VDDP change to +0.75VS
@20190704D

+VDDP_ALW

1pcs 22uF / 3pcs 1uF

+VDDP_RUN

2pcs 22uF / 8pcs 1uF / 1pcs 180pF

1pcs 0.22uF / 1pcs 1uF

+VDD_18_S5 change to +1.8VSUS
@20190704D

Add @20190617D

+1.8V_ALW

1pcs 22uF / 2pcs 1uF

+1.8V_RUN

1pcs 22uF / 2pcs 1uF

+VDDBT_RTC

11G232210526360 (1UF/10V) change to 11G232210515320 (1UF/6.3V)
C0902
@20190705C

C1072 mount
@20190722D

N1,RPC22UF

不上件

+VDD_18 change to +1.8VS
@20190704D

+3.3V_ALW

1pcs 22uF / 2pcs 1uF

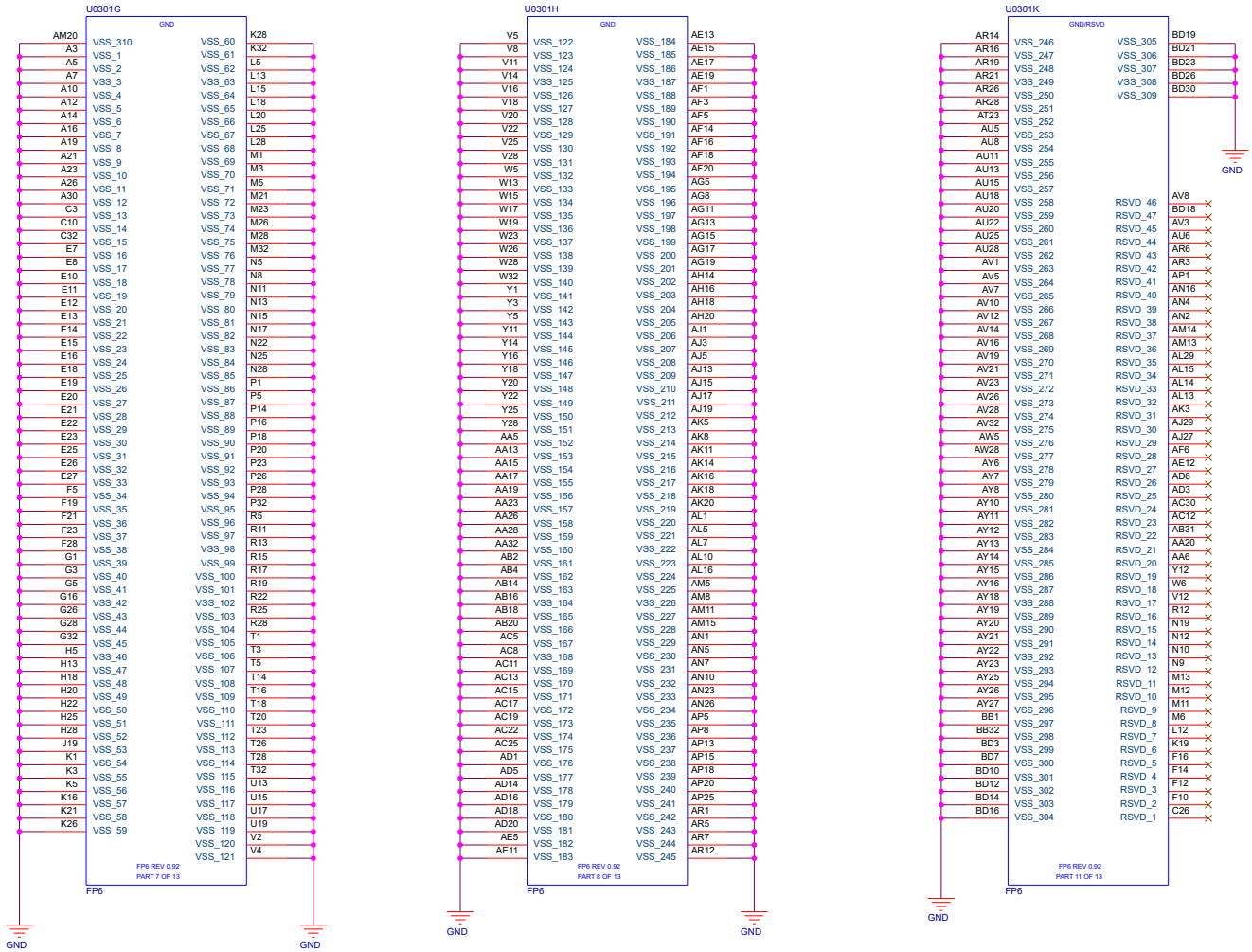
+3.3V_RUN

1pcs 22uF / 2pcs 1uF

Project Name	FX505DY
Rev	R1.0
Title :	CFL-H_CPU_PWR(1)_R1.3B
Size	C
Dept.:	ASUSTeK COMPUTER INC.
Engineer:	RD EE3
Date:	Tuesday, April 28, 2020
Sheet	10 of 104

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, April 28, 2020	Sheet 15 of 104	

CPU_GND



Project Name: FX505DY		Rev: R1.0
Title : AMD_CPU_GND		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: RD2 EE3	
Date: Tuesday, April 28, 2020	Sheet 5 of 104	

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, April 28, 2020	Sheet 17 of 104	

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, April 28, 2020	Sheet 11 of 104	

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, April 28, 2020	Sheet 22 of 104	

CPU_Power

20A EDC
0.7~1.325V @ 15A TDC

96A EDC
0.3~1.400V 58A TDC

+VDDCR_SOC

+APU_VDDSOC_RUN @15A TDC @20A EDC

+VDDCR_VDD

+APU_VDDCORE_RUN @58A TDC @96A EDC

U0301F

VDDIO_MEM_S3 @ 6A
1.2±0.06

+1.2V

11G232210526360 (1UF/10V) change to 11G232210515320 (1UF/6.3V)
C0902
@20190705C

BO (Bottom side outside SOC)
BU (on bottom side under SOC)

1pcs 22uF / 1pcs 1uF

C0901 22UF/6.3V
C0902 1UF/6.3V
C0903 22UF/6.3V
R0902 0Ohm /NA
R0904 0Ohm

VDDIO_AUDIO: 1.8±0.09
VDD_33: 3.3±0.165
VDD_18: 1.8±0.09
VDD_18_S5: 1.8±0.09
VDD_33_S5: 3.3±0.165
VDDP_S5: 0.75±0.0375
VDDP:0.75±0.0375
VDDBT_RTC_G: 1.425 ~ 3.465

VDDIO_AZ_ALW @ 0.2A
VDD_18 @ 2.5A
VDD_18_ALW @ 1A
VDD_33 @ 0.25A
VDD_33_ALW @ 0.25A
VDDP_S5 @ 2A
VDDP @ 2A

R0906 R0907 R0909 R0908 R0910 R0911 R0912 R0901 1KOhm N/A

[10,32] VDDBT_RTC_G

FP6

RTC Power

+3VA
SL0907 0603 /@
R0905 45.3KOhm
C0907 10PF/50V
GND
RTC battery

+VCC_RTC
D0902 BAV70_L
+RTC_BAT
R0903 N/A 10KOhm
+RTCBAT
BAT0901
SIDE1 SIDE2
WTOB_CON_2P
12G17100002C
C0908 0.1UF/6.3V
C0906 0.1UF/6.3V /@

R0903 1K change to 10K (FP6 CRB)
@20190613A

Delete PU0901, C0903, C0904
Add SL0906
@20190613A

+3VA_RTC
SL0906 0603 /@
+VCC_RTC

Project Name: FX505DY			Rev: R1.0
Title: CFL-H_CPU_PWR(1)_R1.3B			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD EE3	
Date: Tuesday, April 28, 2020	Sheet 9 of 104		

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, April 28, 2020	Sheet 24 of 104	

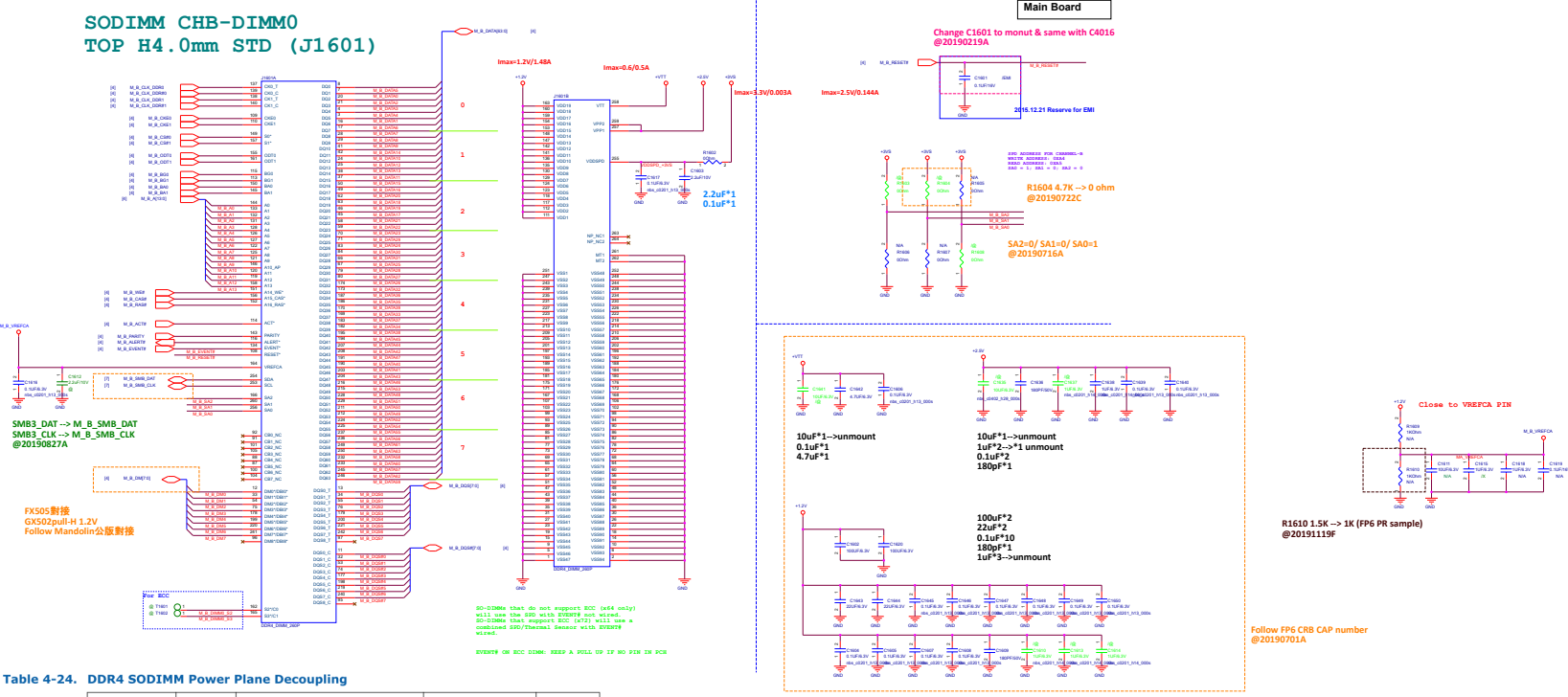


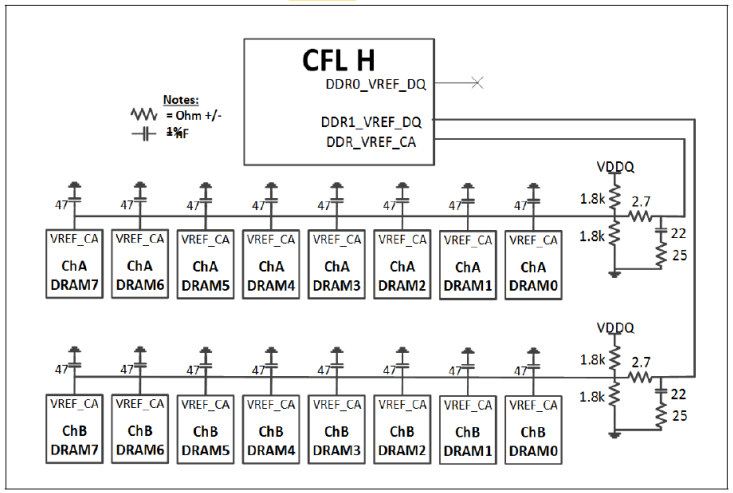
Table 4-24. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM **1DPC**	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Placed on VTT plane close to DIMM, 1 cap stuffed, 1 placeholder	2x 10µF (0603)	
		Placed on VTT plane close to DIMM	4x 1µF (0402)	
	VPP	DIMM Pin side, 1 per DIMM	2x 10µF (0603)	
		DIMM Pin side, 1 per DIMM	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	2x 0.1µF (0402)	
		Place close to DIMM	2x 2.2µF (0402)	

DDR4 - 2666MHz (8G)
1st : Hynix - 03A08-00051400
2nd : Samsung - 03A08-00051300
DDR4 - 2666MHz (16G)
1st : Hynix - 03A08-00061400
2nd : Samsung - 03A08-00061500

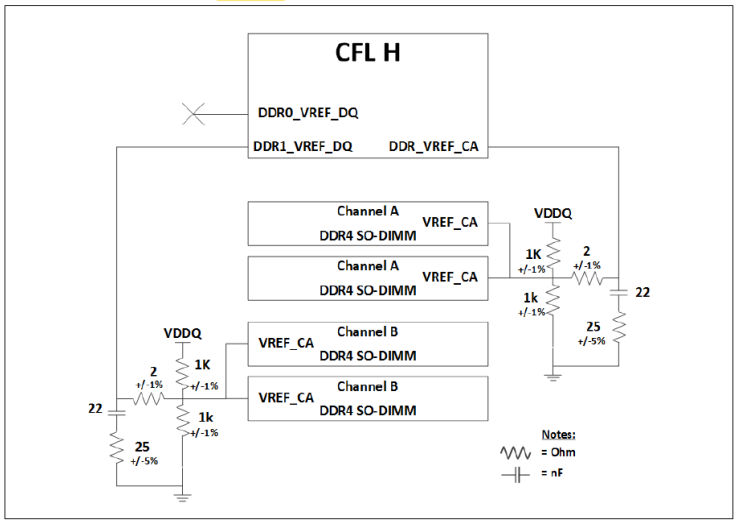
Memory Down Vref

Figure 4-24. CFL-H DDR4 x8 Memory Down V_{REF-CA} Overview

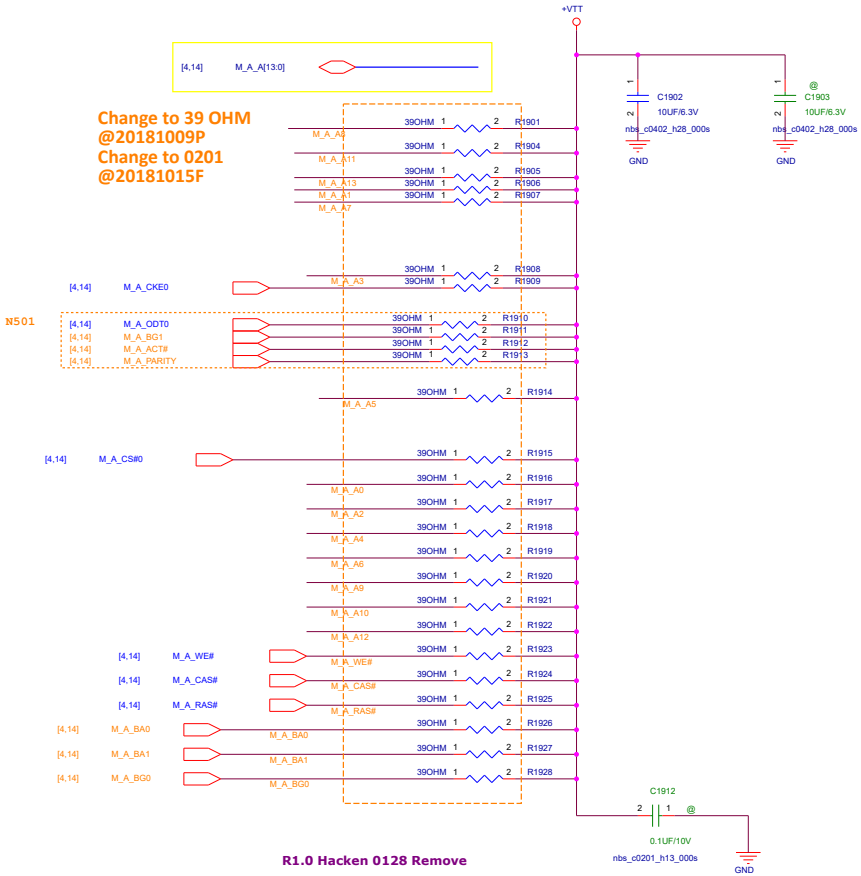


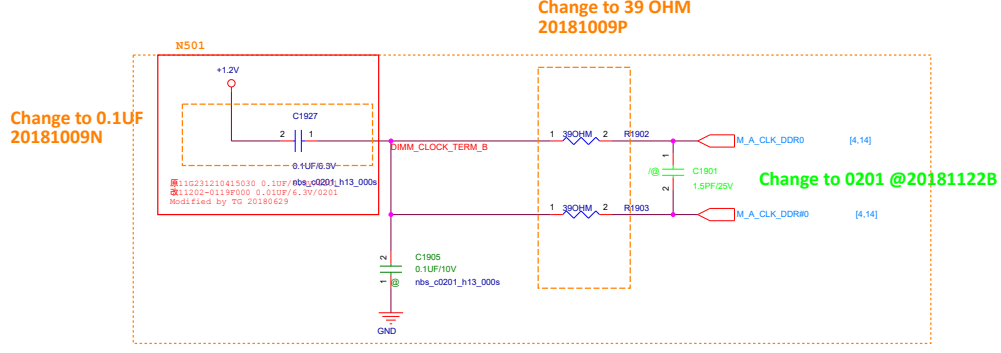
SO-DIMM1 Vref

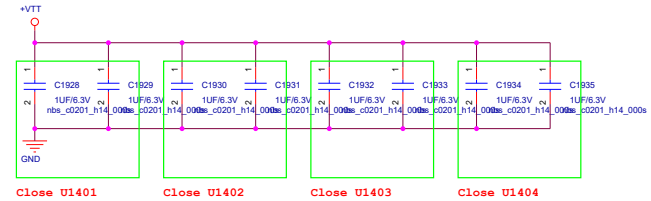
Figure 4-22. CFL-H DDR4 SO-DIMM V_{REF-CA} Overview

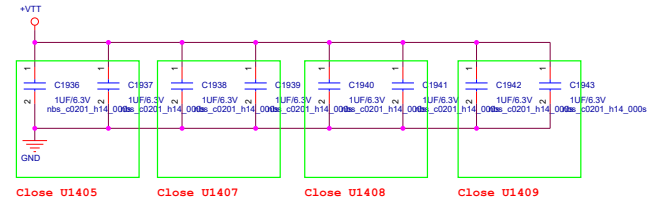


Project Name: GX531GX		Rev: 1.0
Title : DIM_CA/DQ Voltage		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Tuesday, April 28, 2020	Sheet 18 of 104	









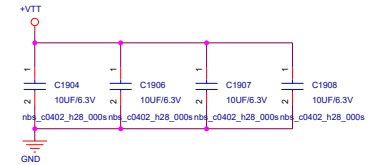
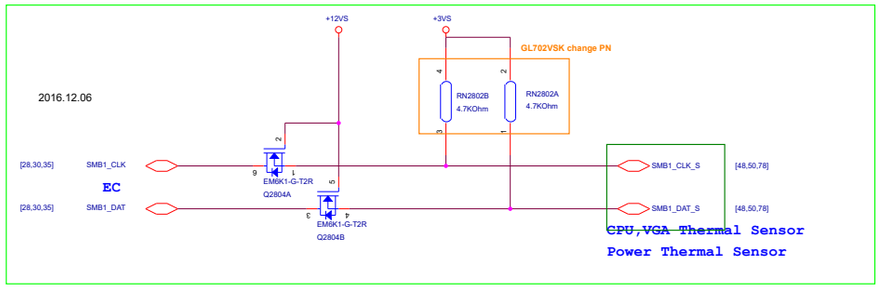


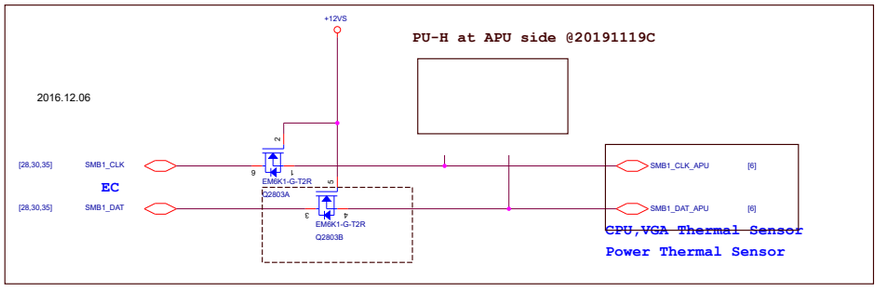
Table 4-25. DDR4 Memory Down Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 Memory Down x8- 8 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x8 DRAM device as possible	64x 1µF (0402) (min of 48 stuffed)	
		Distributed around the DRAM devices	20x 10µF (0603) (min of 12 stuffed)	
	VPP	2 as near each x8 DRAM device as possible	32x 1µF (0402)	
		Distributed around the DRAM devices	10x 10µF (0603)	
	VTT	Distributed along termination resistors	32x 1µF (0402)	
		Distributed evenly across domain	8x 10µF (0603)	

Follow GL702ZM
@20181022C



Avoid SIC, SID leakage
@20191119D

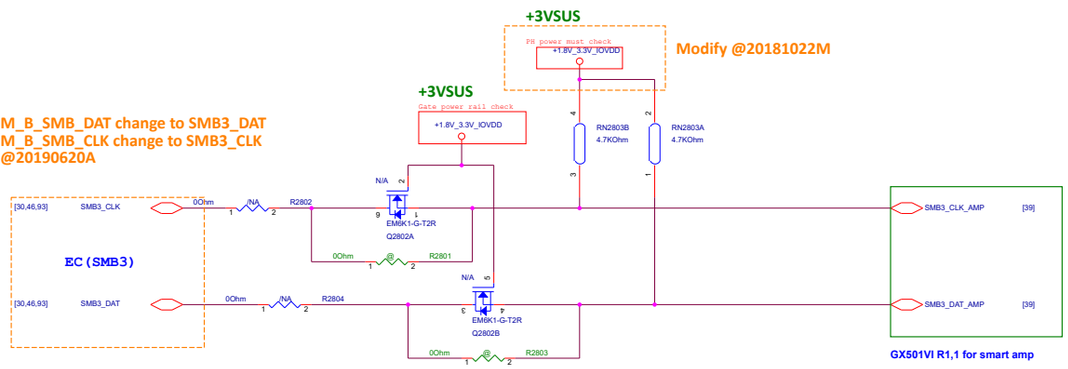


Q06B --> Q2308B @20191119D

+3VSUS

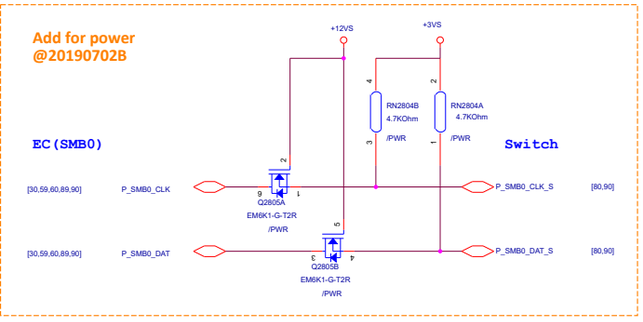
Modify @20181022M

M_B_SMB_DAT change to SMB3_DAT
M_B_SMB_CLK change to SMB3_CLK
@20190620A



GX501VI R1,1 for smart amp

Add for power
@20190702B



RN2804, Q2805 --> mount
@20191016A

NKEY_預留0 OHM對接

EC_PU +3VA

EC (SMB1)	Isolation	+3VS	GPU sensor VRAM sensor CPU sensor HDMI_預留

APU I2C3_PU +3VSUS

DDR4 SO-DIMM_對接

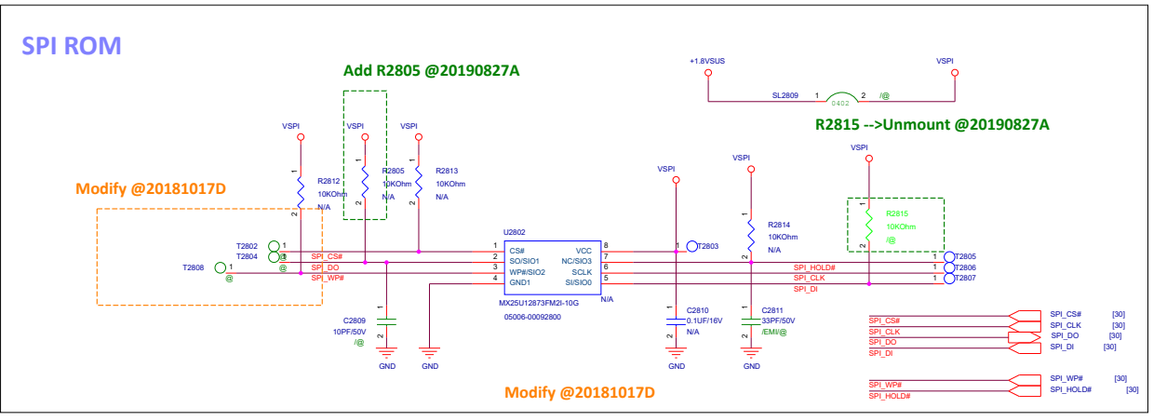
EC (SMB3)

Type-C PD

Slave charger

EC (SMB3) M_B_SMB_DAT	Isolation	+3VSUS SMB3_CLK_AMP	Audio AMP

SPI ROM change to P.28
@20190731C



Project Name: GX531GX			Rev: 1.0
Title: PCH-SPI ROM,OTH			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Tuesday, April 28, 2020	Sheet 28 of 104		

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, April 28, 2020	Sheet 20 of 104	

CPU_USB

Delete J2101
@20190708A

USB_DP1 change to USB0_DP @20190606A

USB3.0 TX/RX
I/O-IOVPS5-D_VDDP (S5_0.75)_FP6 (FDS)

U3_U3TXDP1 change to USB0_TXP @20190606A

USB Port0 USB3.1 Gen1 Type-A Port0

USB Port1 USB3.1 Gen1 Type-A Port1

USB 2.0 Port2 N-KEY

USB 2.0 Port3 BT USB2.0

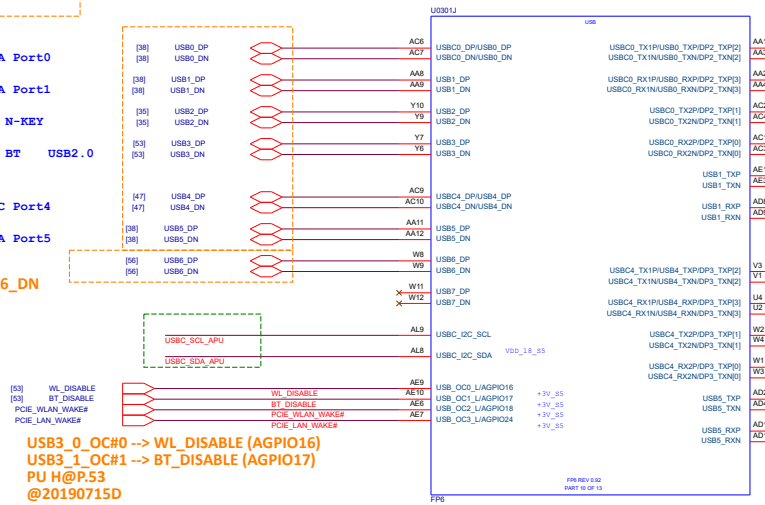
USB Port4 USB3.1 Gen2 Type-C Port4

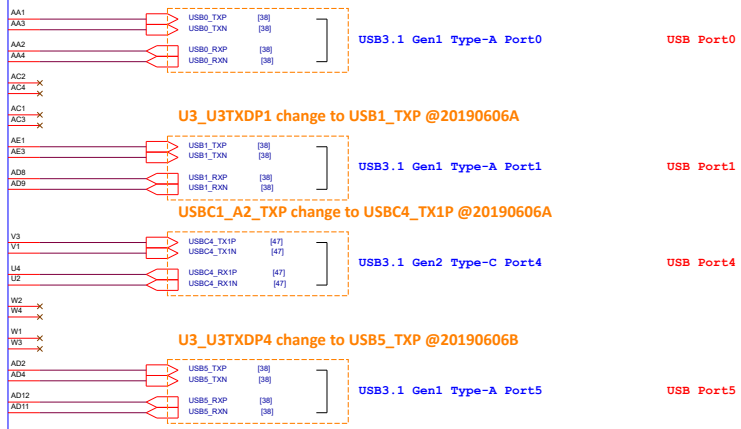
USB Port5 USB3.1 Gen1 Type-A Port5

USB 2.0 Port6

USB 2.0 Port7

Add USB6_DP, USB6_DN
@20190708A



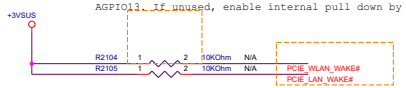


PCIE_LAN_WAKE#
@20190703C

USB3_0_OC#0 --> WL_DISABLE (AGPIO16)
USB3_1_OC#1 --> BT_DISABLE (AGPIO17)
PU H@P.53
@20190715D

AMD Design check

AGPIO13, if unused, enable internal pull down by software.

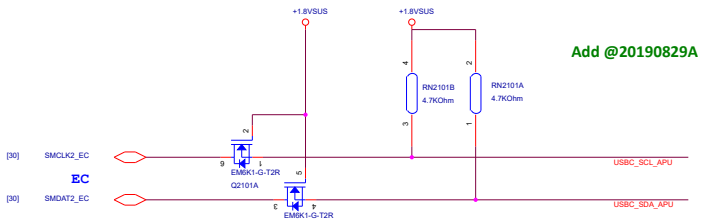


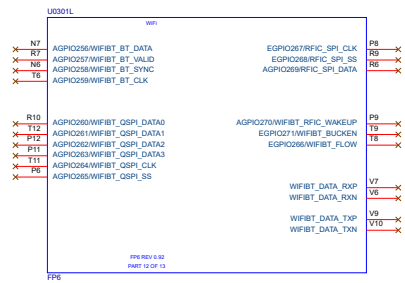
Delete R2108 R2106
@20190715D

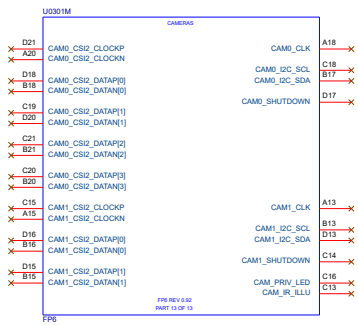
Rename
@20190702B

USB Port 0,1,4,5
USB-A USB3.2 Gen1(5Gbps): 304.8mm (12000mil)
USB-C USB3.2 Gen1(5Gbps): 177.8mm (7000mil)
USB-A & USB-C USB3.2 Gen2(10Gbps): 152.4mm (6000mil)

Add @20190829A







<Variant Name>

ASUS	Project Name: FX505DY	Rev: R1.0
Title :		
Size: C	Dept.: NB-SZ-RD3	Engineer:
Date: Tuesday, April 28, 2020	Sheet 21 of 104	

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
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Micron 8G
03012-00030900
2Gb4 32bit 1Gx64M*8 1.2V FBGA78
MT40A1G8SA-062E:J

Micron 16G
03012-00060200
2Gb4 32bit 2Gx8M*8 1.2V FBGA78
MT40A2G8VA-062E:B

重新端料
03012-00060100
Samsung K4AAG085WA-BCW是最大集合
@20191120B

Follow FP6 MPDG製接
Follow GX502預置1.2V pull-H
@20181005H

Change Footprint to nbs_bga_78p_010c
Change PN to 03012-00006300
@20190705A

1Gx8(IO)
Total: 1Gx8ea = 8G

Imax=1.2V/0.28A

Imax=2.5V/30mA

Add R1409- R1416 (Vendor suggestion)
@20190902D

Close to VREFCA PIN

R1418 1.5K -> 1K (FP6 PR sample)
@20191119F

10uF*1
1uF*4

Close U1401

Close U1402

Close U1403

Close U1404

Close U1405

Close U1407

Close U1408

Close U1409

Close U1401~U1404 pin J1

Close U1405~U1409 pin J1

Add C1401 C1402 C1458
調放置未端
@20190713A

Delete C1402 C1458
C1401 0805 -> 0603
調放置未端
@20190715E

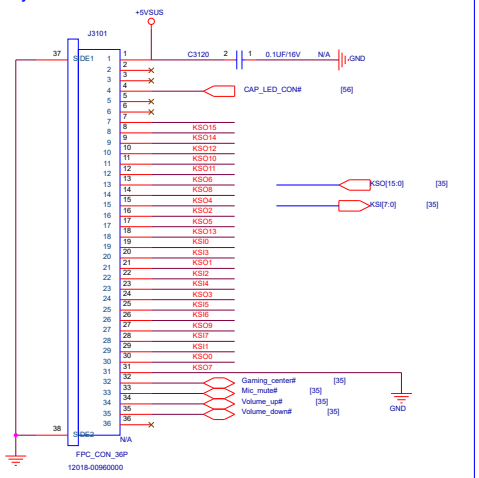
CE1402, CE1401 (220uf) change to CE1601 (330uf)
@20190626A

DIM Thermal Sensor

Table 4-25. DDR4 Memory Down Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 Memory Down x8- 8 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x8 DRAM device as possible	64x 1µF (0402) (min of 48 stuffed)	
		Distributed around the DRAM devices	20x 10µF (0603) (min of 12 stuffed)	
	VPP	2 as near each x8 DRAM device as possible	32x 1µF (0402)	
		Distributed around the DRAM devices	10x 10µF (0603)	
	VTT	Distributed along termination resistors	32x 1µF (0402)	
		Distributed evenly across domain	8x 10µF (0603)	

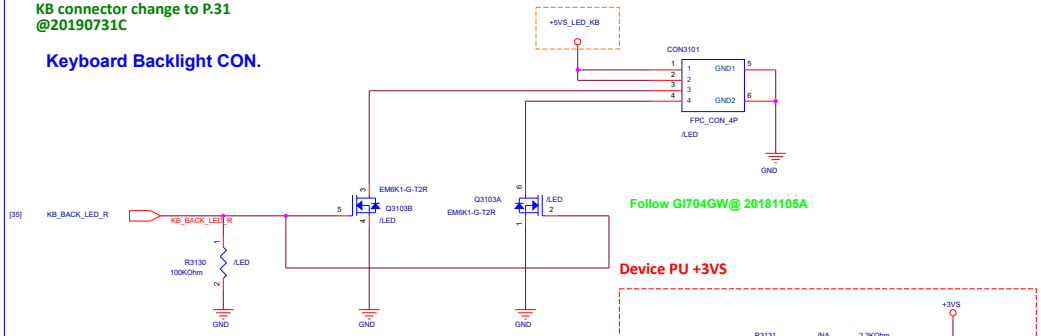
Keyboard Connector



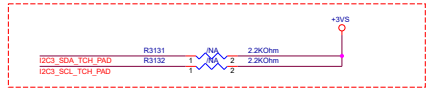
2017.02.08 update Keyboard connector

KB connector change to P.31
@20190731C

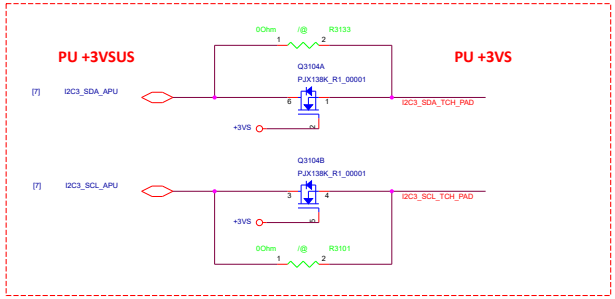
Keyboard Backlight CON.



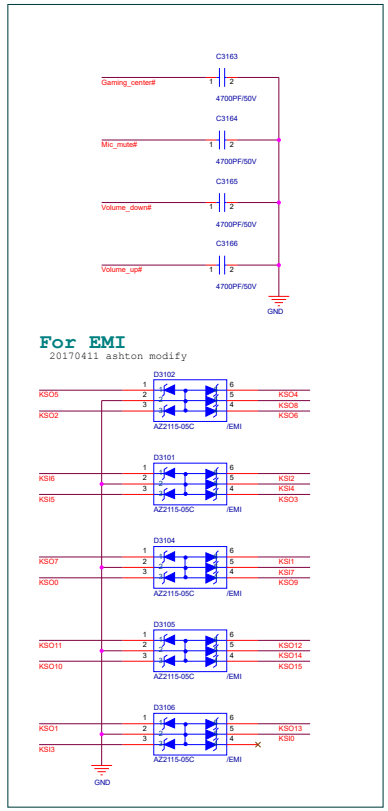
Device PU +3VS



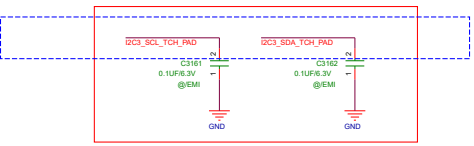
Add@20200413



Main Board



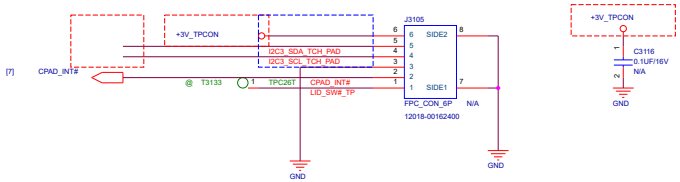
EMI Reserve
如要上件請確認容值(選擇Pico等級)



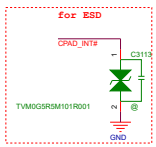
I2C0_SCL_TCH_PAD --> I2C3_SCL_TCH_PAD
I2C0_SDA_TCH_PAD --> I2C3_SDA_TCH_PAD
@20190927A

+3VSUS_TPCON --> +3V_TPCON
@20200413

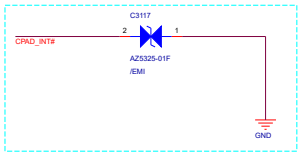
TP Conn.



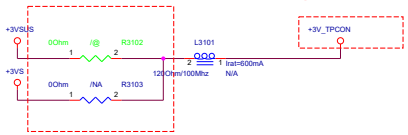
D3110 ESD Diode
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D



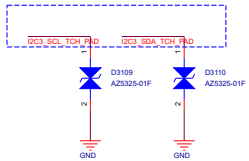
Add @20181219B (EMI request)



Add@20200413



+3VSUS_TPCON --> +3V_TPCON
@20200413



<Variant Name>

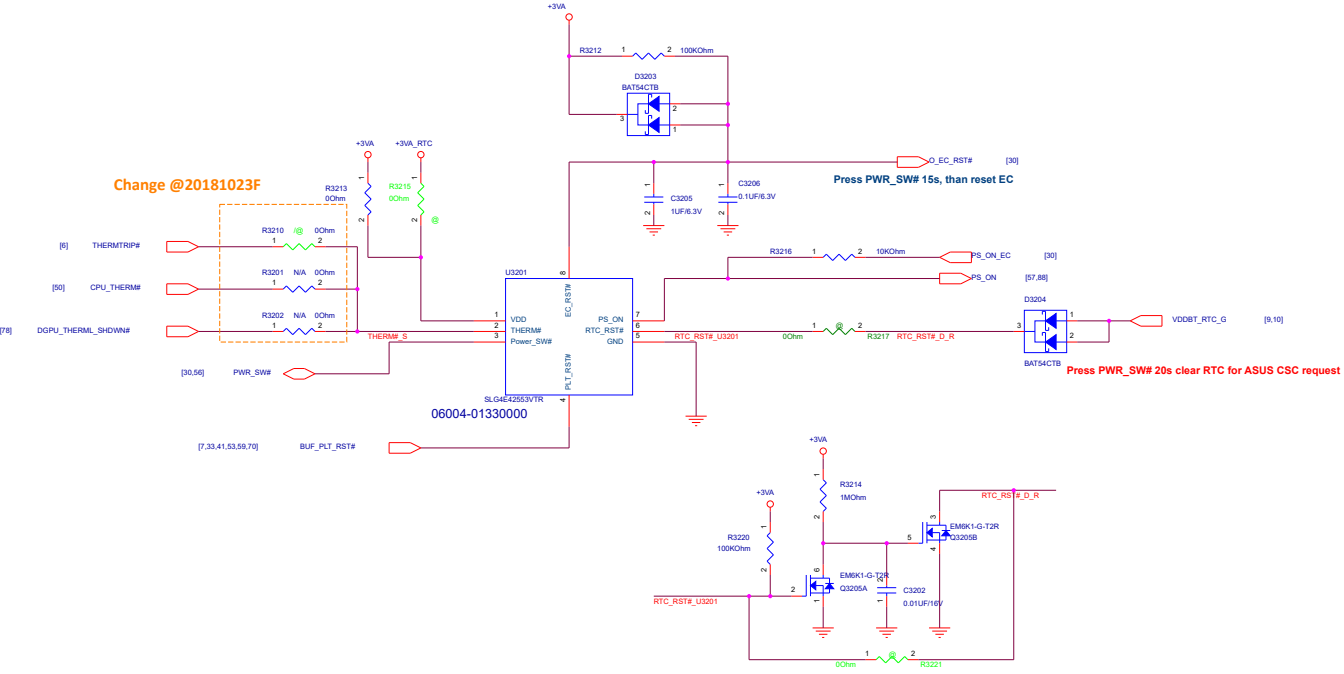
ASUSTeK COMPUTER	Title : KBC_KB & TP	
	Engineer: EE	
Size: C	Project Name: GM501	Rev: R1.0
Date: Tuesday, April 28, 2020	Sheet 31 of 104	

Modern standby project should use Silego solution for EC/RTC reset (Microsoft hardware requirements)

6.6.2 Power button behavior

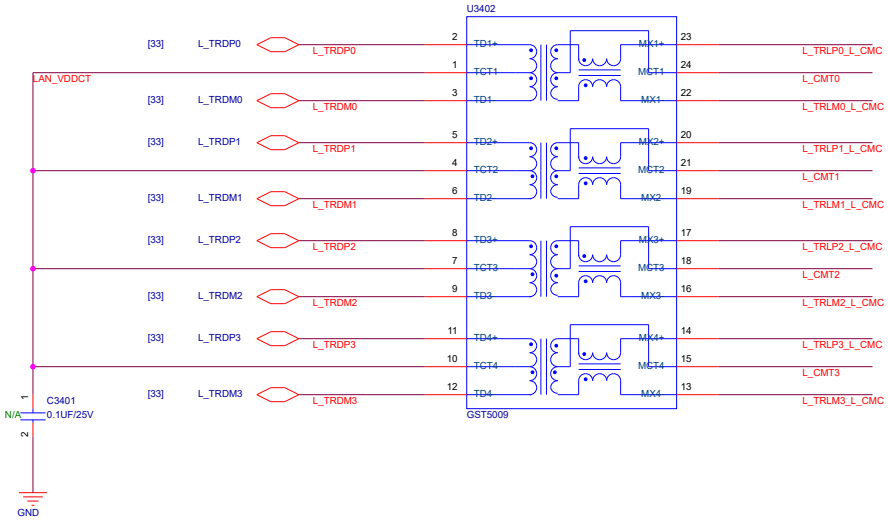
https://docs.microsoft.com/en-us/windows-hardware/design/minimum/minimum-hardware-requirements-overview#section-60---shared-minimum-hardware-requirements-for-components

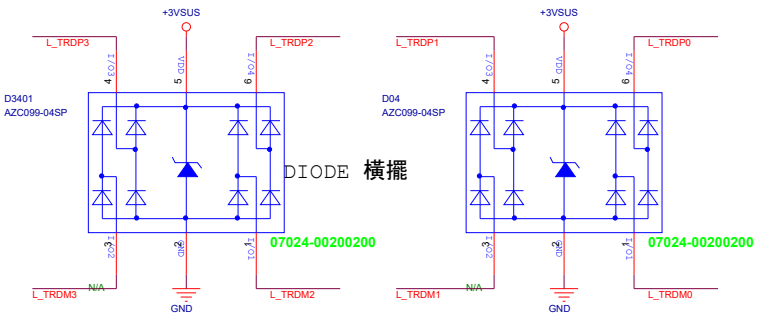
UX362FA R1.3 board will verify this circuit 7/E



Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, April 28, 2020	Sheet 23 of 104	

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, April 28, 2020	Sheet 25 of 104	



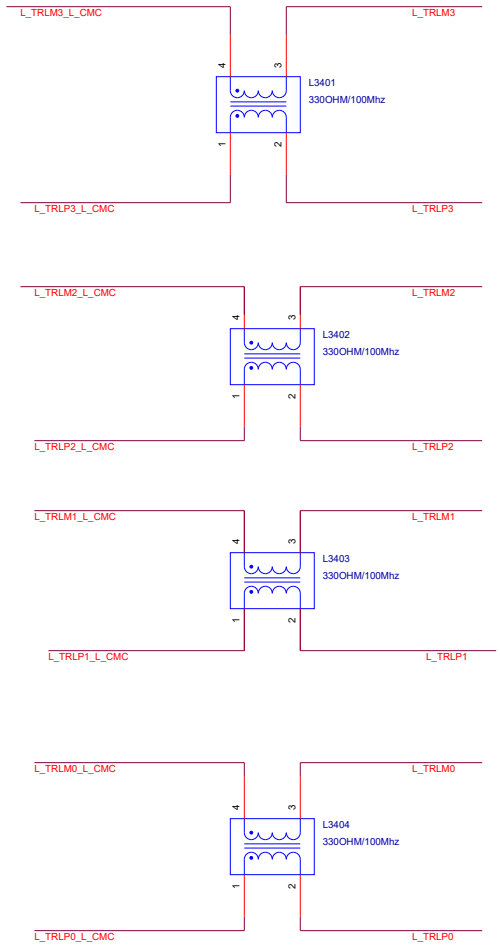


D3401,D3402 ESD Diode

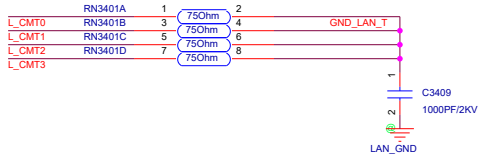
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

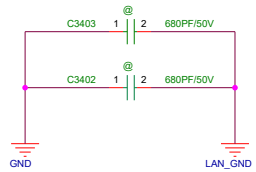
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

Main Board

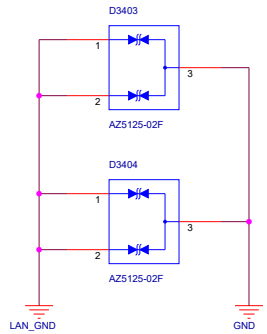


Main Board



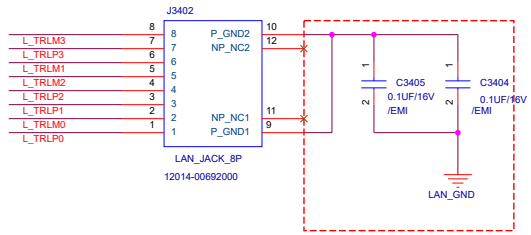


Place near chassis GND

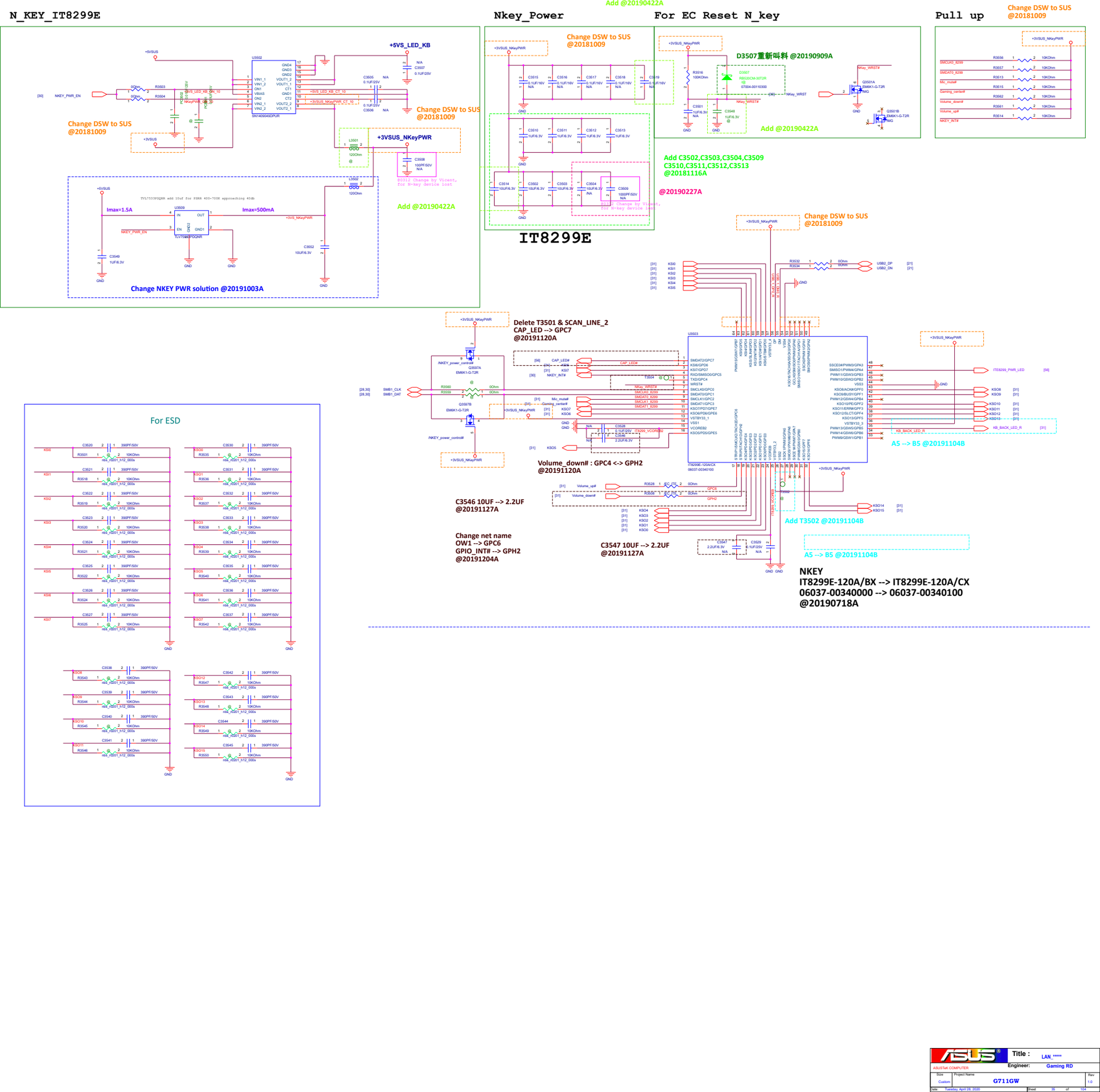


LAN Connector

Add C3405,C3404 @20200423A



ASUS	Project Name: GU502DU	Rev: 1.0
Title : LAN_RJ45_CON		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: NB1 RD2 EE1
Date: Tuesday, April 28, 2020	Sheet 34 of 104	

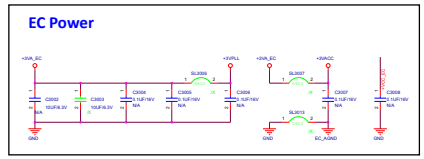


ASUSTeK COMPUTER	Title : LAN_*****
	Engineer: Gaming RD
Size: Custom	Project Name: G711GW
Date: Tuesday, April 28, 2020	Sheet 35 of 104

<Variant Name>

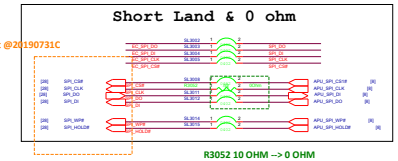
Title <Title>		
Size B	Document Number GA401	Rev <RevCode>
Date: Tuesday, April 28, 2020	Sheet 27 of 104	

EC Chip - IT8225



SPI ROM change to P.28
@20190731C

SPI_CLK 10k change to 10 OHM @20181029G



Add port @20190731C

R3052 10 OHM --> 0 OHM
@20190801B

Add @20190628B

Delete Q3001
@20190909B

R3056 PU +3VS --> +12VS
@20190801B

R3045 100K --> 10K & mount
R3056 10K --> 15K
@20190904A

EC GPIO

Add GPG1
@20190725C

VCC => +3VS system power ; LPC
VSTBY=>+3VA_EC ; Power supply of EC power

EC_GPG6 --> ADP_INSERT_NG#
@20191115A

U3001.06037-00260200 --> 06037-00370100
@20190828B

+3VACC==+3VA_EC,
+3VAPLL==+3VA_EC_0906

Follow GX502
@20181009E

Add REST_AMP#@20190430A

FAN_V_Switch
@20190701C

Add FAN_V_Switch @20181218C

Delete R3059 PU-H +3VA_EC (AMP_SLEEP#)
PU-H @ P.36
@20191204A

Add U3002 (High speed switch)
@20190904A

R3011, R3057, U3002 --> mount
@20190909B

U3002 06096-01120000 change to 06016-02220000
@20191003A

Table 1. TMUX1101 Truth table

SEL	SWITCH STATE
0	OFF (HI-Z)
1	ON

Table 2. TMUX1102 Truth table

SEL	SWITCH STATE
0	ON
1	OFF (HI-Z)

Add @20181219B (EMI request)

ADP_INSERT_NG# --> EC_GPG2
@20191115A

Check with EC

Delete OP_SD#_GPD5
@20190621B

C3028 0.1UF --> 100PF
@20191115A

GPH6 --> WLAN_RST#_EC
GPC0 --> LAN_PWR_EN
GPD5 --> LAN_RST#_EC
@20190911D

R3016 & R3017 mount
@20191120A

0.9 change to 0.75
@20190618D

AMD_SPI_CLK

M_B_S_DAT change to SMB3_DAT
M_B_SMB_CLK change to SMB3_CLK
@20190620A

C3015 0.1UF --> 0.01UF @20191115A

@20200416A

PM_PWROK_EC del intersheet ref, 0910

Add GPI5, GPI6, GPI7
@20190628D

Support Slave CHG
(Prevent from leakage)

Add @20190702A (From GX502)

Add R3077,R3078
@20200428A

@20200416A

C3016 0.1UF --> 100PF @20191115A

R3004 unmount
@20191007A

Add EC_GPI3, APU_RST#, R3004
@20190904A

Add EC_GPJ4, R3065, AC_PRESENT_EC
@20191014D

Add PD_IRQ# (GPI2)
Remove I2C0_INT_EC (GPJ5)
@20190620C

Add ADAPTER_IN#_R (GPI5)
@20190702A

@20200427A

@20200416A

Add R3036 R3061
@20190711A

R3018 & R3022 unmount (shipping mode OD test)
@20200427

Add R3071
@20191120A

0.9 change to 0.75
@20190618D

Del 1.8V_ON_EC NET, 0910

C3019 Change to mount @201812198

PWRLIMIT_EC# --> ADP_INSERT_NG#
@20190710E

Add @20190711A

EC_GPG2 PU +3VA --> +3VA_EC
@20191209A

Add @20200416A

Add R3069 (EC HW Strap Pin)
@20191115A

teknisi-indonesia

Project Name	FX505YD
Title :	EC
Size: D	Dept.:
Date: Tuesday, April 28, 2020	Engineer:
Sheet 39 of 104	

SPK Power

AC_BAT_SYS, +PVDD_AMP
R3901 1 2 0Ohm N/A
R3931 1 2 0Ohm N/A

IO Power

+1.8VSUS, +3VSUS
0926 Modify
R3907 1 2 @ 0Ohm
R3921 1 2 0Ohm
5mA
+1.8V_3.3V_IOVDD
C3907 1 2 1UF/6.3V
GND

INTERNAL SPK1 Conn.

SPK L+ L- R+ R- trace width
Speaker 8 ohm
Max = 1.5W / Channel
I = 0.43 A

(Smart AMP MAX 2A/Channel) ==> 60mils

H_SPKL-_CON	R3928	0Ohm	ADR_AMP
H_SPKL+_CON	R3929	0Ohm	J3901_pin4
H_SPKR-_CON	R3926	0Ohm	J3901_pin3
H_SPKR+_CON	R3927	0Ohm	J3901_pin2
			J3901_pin1

J3901 SIDE2 SIDE1 WTOB_CON_6P 12017-00011400 GND

Keep for test @20181017A

C3938 C3947 C3944 C3946 change to 11G233222412150 @20190705B

+PVDD_AMP
C3903 22UF/25V
C3904 22UF/25V
C3905 0.1UF/50V
GND

+1.8V_3.3V_IOVDD
C3911 4.7UF/10V
C3910 0.1UF/16V
GND

C3947 0.22UF/25V H_SPKL- H_SPKL-
C3944 0.22UF/25V H_SPKR- H_SPKR-
C3938 0.22UF/25V H_SPKL+ H_SPKL+
C3946 0.22UF/25V H_SPKR+ H_SPKR+
C3939 1UF/16V
R3913 1KOHM ADR_AMP

U3905A TAS5825MRHBR

1	GPIO0	BST_A+	2
2	GPIO1	OUT_A+	3
3	GPIO2	PVDD1	4
4	LRCLK	PVDD2	5
5	SCLK	DGND	6
6	SDIN	DVDD	7
7	SDA	VR_DIG	8
8	SCL	ADR	
9		GND1	33
10		PGND4	32
11		PGND3	31
12		OUT_A-	30
13		BST_A-	29
14		BST_B-	28
15		OUT_B-	27
16		PGND2	26
17		PGND1	25
18		BST_B+	24
19		OUT_B+	23
20		PVDD4	22
21		PVDD3	21
22		AGND	20
23		AVDD	19
24		GVDD	18
25		PDN#	17

C3942 1UF/16V
C3943 1UF/16V

+PVDD_AMP
C3945 0.1UF/50V
C3914 22UF/25V
C3912 22UF/25V
GND

+1.8V_3.3V_IOVDD
R3930 10KOhm
R3902 0Ohm REST_AMP# [30]
AMP_PDN#
C3948 0.1UF/16V @
GND

0926 Change for additional 13 VIA

Add REST_AMP#@20190430A

U3905B TAS5825MRHBR

34	GND2	GND1	33
35	GND3	GND4	32
36	GND4	GND3	31
37	GND5	GND2	30
38	GND6	GND1	29
39	GND7	GND4	28
40	GND8	GND3	27
41	GND9	GND2	26
42	GND10	GND1	25
43	GND11		
44	GND12		
45	GND13		
46	GND14		

GND

+1.8V_3.3V_IOVDD
R3924 @ 10KOhm AMP_GPIO0
R3925 @ 10KOhm AMP_GPIO2

TBD

[36] I2S_Codec_SDIN
[36] I2S_LRCLK
[36] I2S_BCLK
[36] I2S_Codec_SDOUT
I2S_Codec_SDIN
I2S_LRCLK
I2S_BCLK
I2S_Codec_SDOUT

SMB3_CLK_AMP [28]
SMB3_DAT_AMP [28]

I2C Address Table

	ADR_AMP(SPK)	Address 8bit
Main(N.C.)	Open	0x9A
Second	Short	0x98

Modify @20181017A

SPK Output

L3901 H_SPKL- 30Ohm/100Mhz H_SPKL-_CON
D3903 AZ5325-01F @
C3915 1000PF/50V

L3902 H_SPKR- 30Ohm/100Mhz H_SPKR-_CON
D3904 AZ5325-01F @
C3919 1000PF/50V

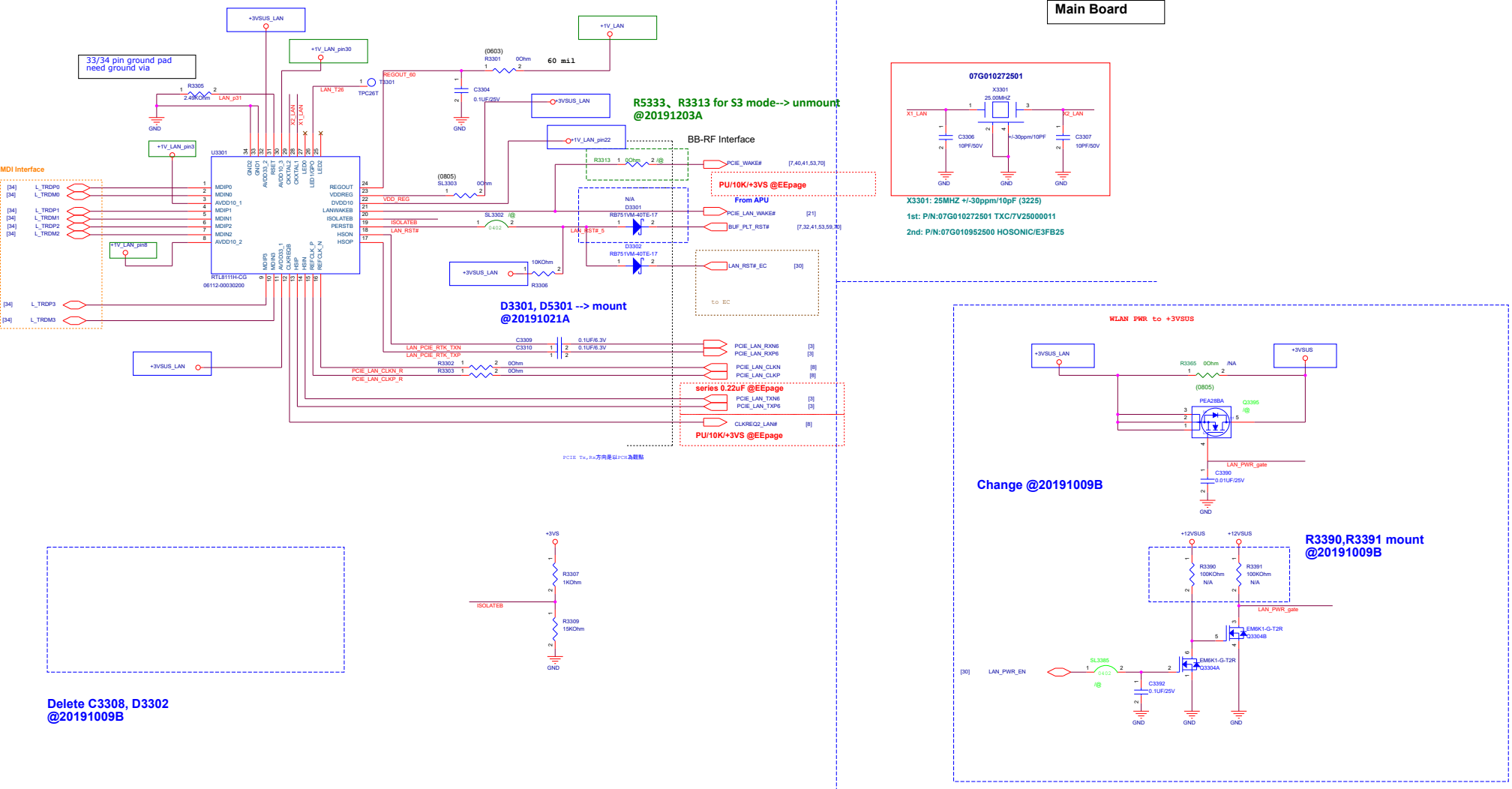
L3903 H_SPKL+ 30Ohm/100Mhz H_SPKL+_CON
D3905 AZ5325-01F @
C3917 1000PF/50V

L3904 H_SPKR+ 30Ohm/100Mhz H_SPKR+_CON
D3906 AZ5325-01F @
C3921 1000PF/50V

GND

ASUS	Project Name: GX531GX	Rev: 1.0
Title : AUD_INT SPK		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Date: Tuesday, April 28, 2020	Sheet 39 of 104	

Main Board

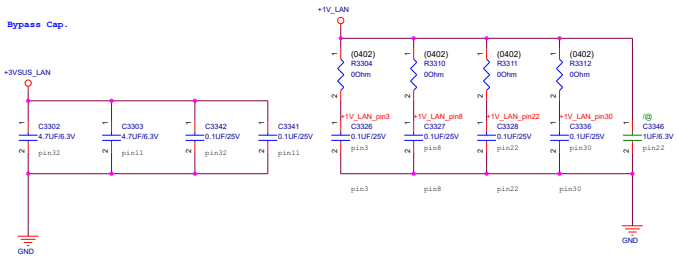


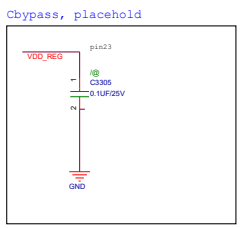
X3301: 25MHZ +/-30ppm/10pF (3225)

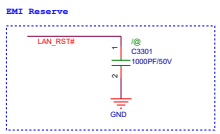
1st: P/N:07G010272501 TXC/7V25000011

2nd: P/N:07G010952500 HOSONIC/E3FB25

Delete C3308, D3302 @20191009B







ASUS	Project Name: GU502DU		Rev: R1.0
Title : LAN RTL8111GUX-CG			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE	
Date: Tuesday, April 28, 2020	Sheet 33 of 104		

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, April 28, 2020	Sheet 26 of 104	

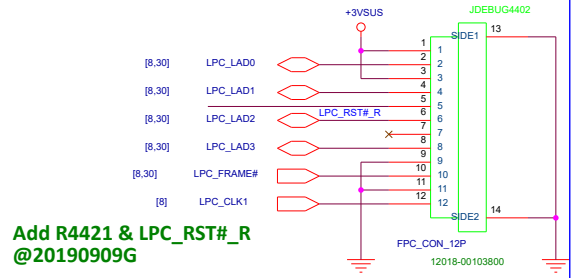
<Variant Name>

ASUSTeK COMPUTER	Title : XDD_HDD & ODD CON	
	Engineer: EE	
Size: A	Project Name: GX502GX	Rev: 1.0
Date: Tuesday, April 28, 2020	Sheet 42 of 104	

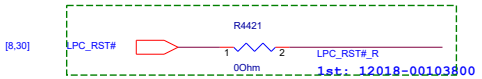
LPC Debug Port

2017/11/10

/@



Add R4421 & LPC_RST#_R
@20190909G

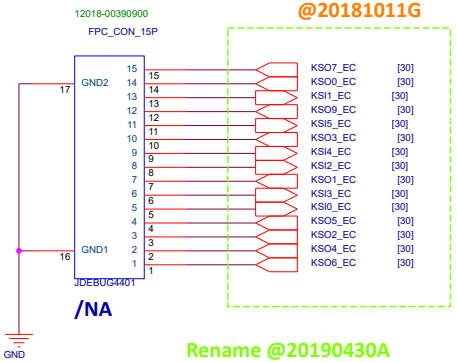


1st: 12018-00103800
2nd :12018-00103300

Flash BIOS

2017/11/10

Rename
@20181011G



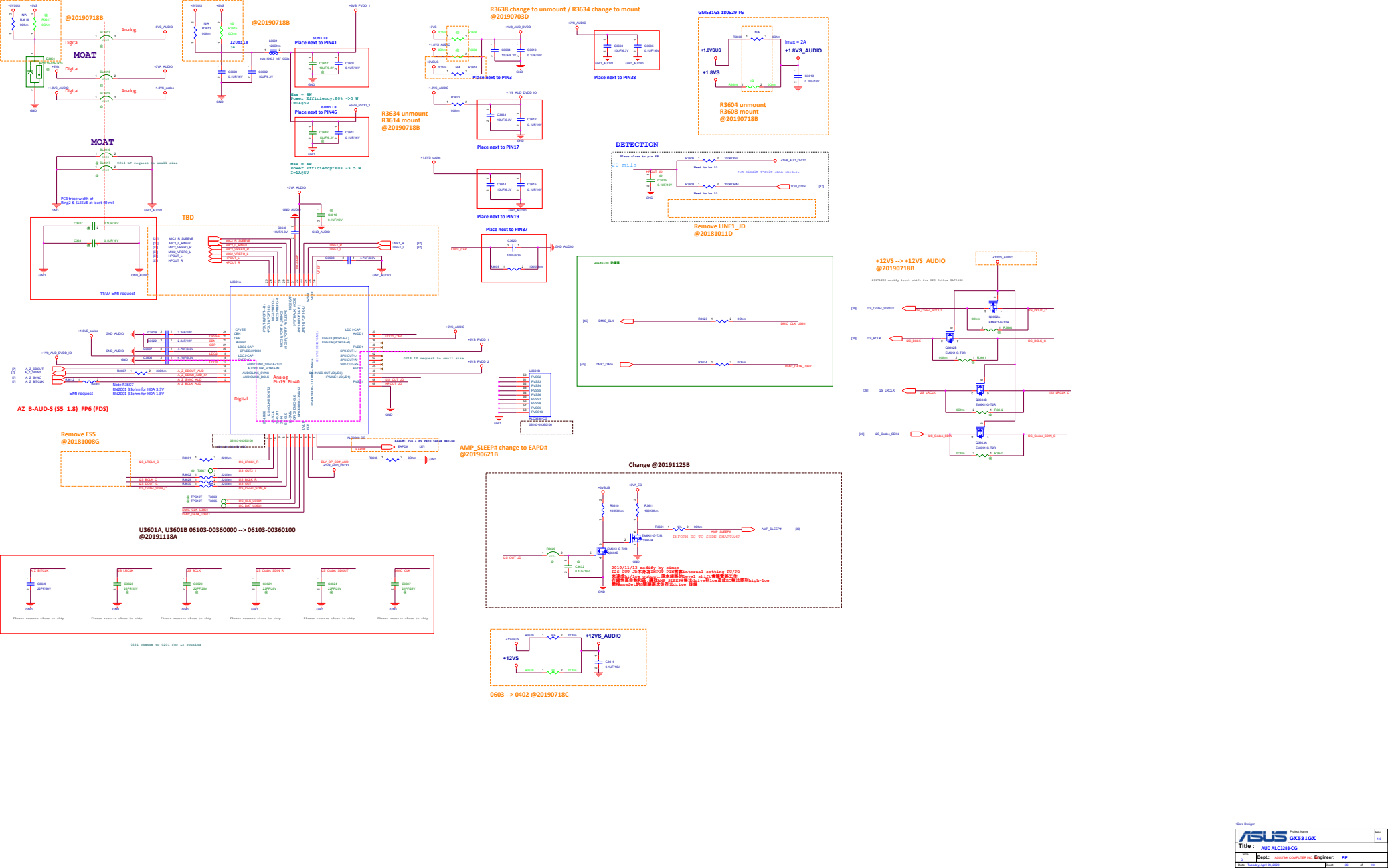
/NA

Rename @20190430A

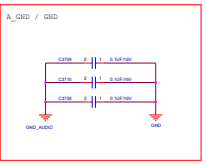
Delete J4401, R4401-R4420, C4401-4404
@20190909C

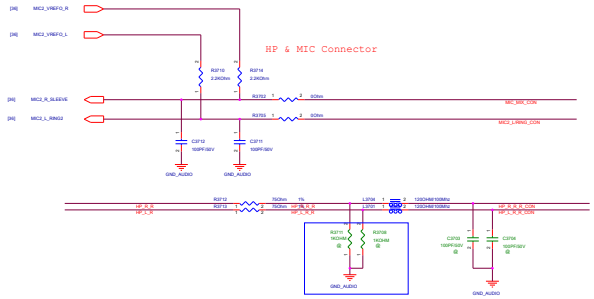
<Core Design>

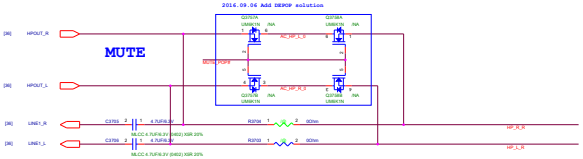
ASUSTeK COMPUTER	Title : DEBUG_LPC	
	Engineer: EE	
Size: B	Project Name: GX502GX	Rev: 1.0
Date: Tuesday, April 28, 2020	Sheet 44 of 104	

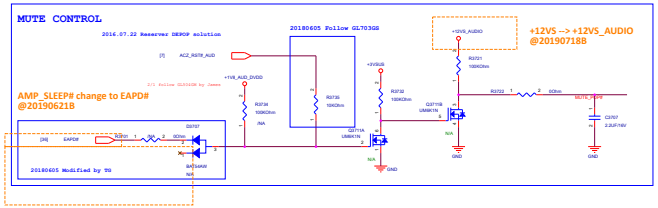

@20190718B
MOAT
Digital
Analog
+3VS_AUDIO
+1.8VS_codec
@20190718B
120mils
3A
60mils
Place next to PIN41
Max = 4W
Power Efficiency:80% ->5 W
I=1A@5V
60mils
Place next to PIN46
Max = 4W
Power Efficiency:80% -> 5 W
I=1A@5V
R3638 change to unmount / R3634 change to mount
@20190703D
Place next to PIN3
Place next to PIN38
GM531GS 180S29 TG
+1.8VSUS
+1.8VS
Imax = 2A
+1.8VS_AUDIO
R3604 unmount
R3608 mount
@20190718B
R3634 unmount
R3614 mount
@20190718B
Place next to PIN17
Place next to PIN19
Place next to PIN37
DETECTION
Place close to pin 18
20 mils
Need to be 1%
FOR Single 4-Pole JACK DETECT.
Need to be 1%
Remove LINE1_JD
@20181011D
TBD
PCB trace width of
Ring2 & SLEEVE at least 40 mil
11/27 EMI request
EMI request
Note R3822
RN2001 33ohm for HDA 3.3V
RN2001 33ohm for HDA 1.8V
AZ_B-AUD-S (SS_1.8)_FP6 (FDS)
Analog
Pin19~Pin40
Digital
Remove ESS
@20181008G
AMP_SLEEP# change to to EAPD#
@20190621B
Change @20191125B
2019/11/13 modify by simon
I2S_OUT_JD 改成 GPIO 控制
客户提供逻辑电路，通过MAX_SLEEP#输出driver到low或是OC输出控制high-low
增加mosfet防止两端同时改变出现drive 锁住
U3601A, U3601B 06103-00360000 --> 06103-00360100
@20191118A
0221 change to 0201 for LY routing
+12VS --> +12VS_AUDIO
@20190718B
0603 --> 0402 @20190718C
ASUS
Project Name
GX531GX
Title :
AUD ALC3288-CG
Dept.:
Engineer:
EE
Date: Tuesday, April 28, 2020
Sheet 30 of 106

Headphone&MIC





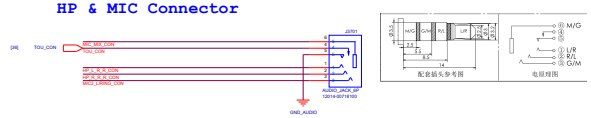




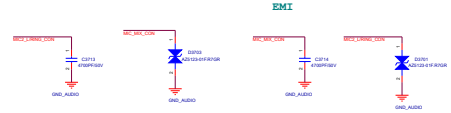
ESS ES9118EQ

Delete OP_SD#
@201906218

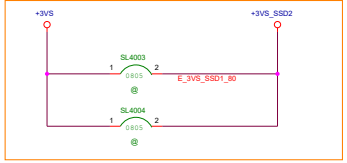
HP & MIC Connector



EMI



ASUS	Project Name: GX531GX		Rev: 1.0
Title : AUDIO ALC3236-CG/VB2 Jack			
Size: D	Dept.: ASUSTeK COMPUTER INC.	Engineer:	
Date: Tuesday, April 28, 2020	Sheet: 37	of: 104	



Follow GX502_1002_2330

2st NGFF PCIE x2

CPU PCIE

lane 3

lane 2

lane 1

lane 0

Delete Lane11,10
@20190716C

PCIe x4 SSD_1 --> Lane 8-11
PCIe x2 SSD_2 --> Lane 0-1
@20190902A

[3] PCIE_SSD2_RXN1
[3] PCIE_SSD2_RXP1
[3] PCIE_SSD2_TXN1
[3] PCIE_SSD2_TXP1
[3] PCIE_SSD2_RXN0
[3] PCIE_SSD2_RXP0
[3] PCIE_SSD2_TXN0
[3] PCIE_SSD2_TXP0
[8] PCIE_SSD2_CLKN
[8] PCIE_SSD2_CLKP

R4009 1 0Ohm N/A 2
R4004 1 0Ohm 2
PCIE_SSD2_CLKN_R
PCIE_SSD2_CLKP_R

For AMD checklist @20181018H

Follow FX505DY & 公板
@20181015J

Delete R4005 & R4017
@20190614B

J4001

+3VS_SSD2
R4001 10KOhm
DAS_DSS_LED2#
SATA2_DEVSLP_C
NGFF_PERST#
NGFF2_PEWAKE#
NGFF2_SUSCLK
SIDE2
SIDE1
NP_NC2
NP_NC1
MINI_PCI_TAB_REMOVAB
GND

J4001_NGFF M-KEY PCIEx4 Connector H=5.0mm
1st Source: P/N:12003-00162500 ARGOSY/NASM0-S6701-TS50

C4002 8PF/25V
C4003 10UF/6.3V
C4004 10UF/6.3V
C4005 10UF/6.3V
C4006 10UF/6.3V
C4007 10UF/6.3V
C4011 0.1UF/6.3V
C4012 0.1UF/6.3V
C4013 0.1UF/6.3V
C4014 0.1UF/6.3V
C4015 0.1UF/6.3V

Add C4009, C4008
@20191009B

C4009 22UF/6.3V N/A
C4008 22UF/6.3V N/A

NGFF2_PERST# --> NGFF_PERST#
Delete D4002, R4008
@20190902A

NGFF_PERST# [41]
CLKREQ5_SSD2# [8]
PCIE_WAKE# [7,33,41,53,70]
Q4001 2N7002K
CLKREQ3_SSD2# --> CLKREQ5_SSD2#
@20190624A

R4012 1 @ 2 0Ohm
+3VS_SSD2
SUS_CLK [8,41,53]

Add @20181013C

改不上件
@20181015H

EMI
NGFF_PERST#
D4001 VPORT0402L331V05 @
GND

NGFF1 Device Sleep
SATA2_DEVSLP_C
R4014 0Ohm
/Enable Devslp
GND

Delete NGFF2_DEVSLP @20181107A

Add @20181219B (EMI request)

C4017 /EMI 0.1UF/16V
C4016 /EMI 0.1UF/16V
PCIE_WAKE#
GND

Remove MUX @20181102C

+3VS
R4030 1 @/PCIE 2 0Ohm
R4060 10KOhm
D4006 BAT54AW
R4022 1 @/PCIE 2 0Ohm
[41] DAS_DSS_LED1#
DAS_DSS_LED1#
DAS_DSS_LED2#
DAS_DSS_LED# [56]

13020-01371400 --> 13020-01379900
@20190909B

H4002 N/A
CT236CB176D146
13020-01379900
GND

Project Name	GX502GX	Rev 1.0
Title :	NGFF_SSD_PCIE_CON	
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: NB1 RD2 EE1
Date: Tuesday, April 28, 2020	Sheet 40 of 104	

<Core Design>

	Project Name **GX502GX**	Rev 1.0

Title : ANT

Size		
C	**Dept.:** ASUSTeK COMPUTER	**Engineer:** EE

Date: Tuesday, April 28, 2020	Sheet	49	of	104

< KEY-M NGFF_SSD_PCH >

Follow GX502_1002_2330

PCIe x4 SSD_1 --> Lane 8-11
PCIe x2 SSD_2 --> Lane 0-1
@20190902A

1nd NGFF PCIE x4

Add @20190902A

lane 11
lane 10
lane 9
lane 8

For AMD checklist @20181018H

Delete R4005 & R4017
@20190614B

Follow FX505DY & 公板
@20181015J

Add C4106, C4107
@20191009B

NGFF1_PERST# --> NGFF_PERST#
Delete D4102, R4121
@20190902A

CLKREQ0_SSD1# --> CLKREQ4_SSD1#
@20190624A

13020-01371400 --> 13020-01379900
@20190909B

New PN : 12003-00079400

EMI

改不上件
@20181015H

HW_Control NGFF Device Sleep

Close to Device connector

Remove MUX @20181102C

Delete NGFF1_DEVSLP @20181107A

<Core Design>

Title : NGFF_SSD_CPU
ASUSTeK COMPUTER
Engineer: EE
Size: C | Project Name: GX502GX | Rev: 1.0
Date: Tuesday, April 28, 2020 | Sheet 41 of 104

Thermal Sensor : SN170027

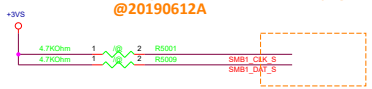
ALERT/SDA/SCL: Open-drain output; pullup resistor 5Kohm

Pin function Supply voltage.: 1.62 V to 3.6 V

Change to unmount. Pull-H @page28
@20190612A

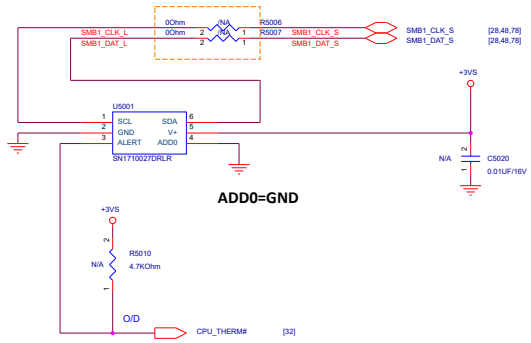
power rail : 3.3V

SMBUS1 to EC



CPU

Add @20190612B

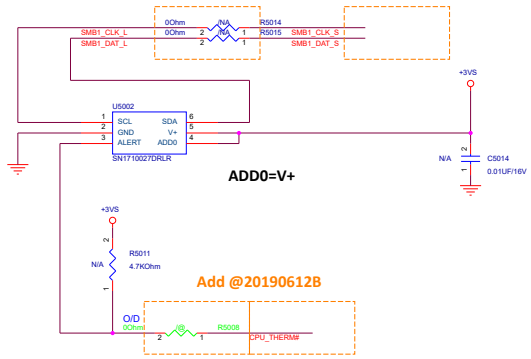


Near CPU

SMBUS addr=10010000 (90)

VRAM

Add @20190612B

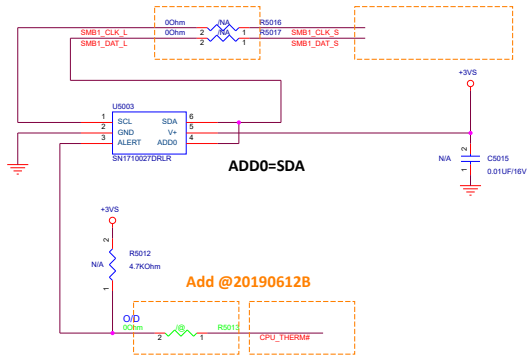


Near VRAM

SMBUS addr=10010001 (91)

GPU

Add @20190612B

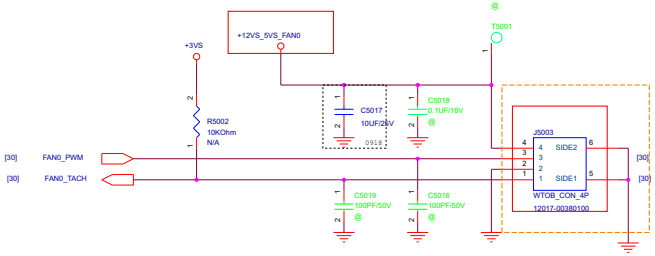


Near GPU

SMBUS addr=10010010 (92)

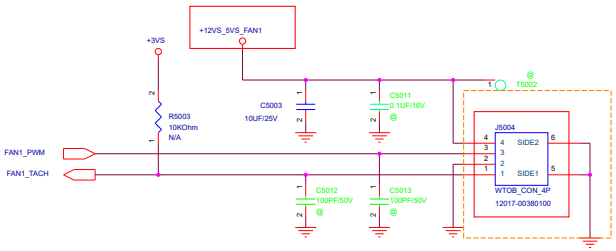
CPU&GPU FAN

Note : connector and power are by project design



1st: 12017-00330300
2nd :12G171010049

Change to 12017-00380100
@20190611B

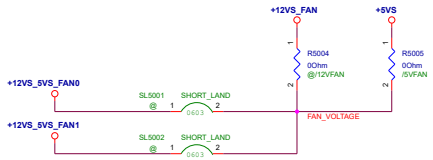


1st: 12017-00330300
2nd :12G171010049

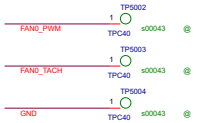
Change to 12017-00380100
@20190611B

ADD0: Address select. Connect to GND, SDA, SCL, or V+

DEVICE TWO-WIRE ADDRESS		ADD0 PIN CONNECTION	Output
1001000	90	Ground	CPU
1001001	91	V+	VRAM
1001010	92	SDA	GPU
1001011	93	SCL	



Delete TP5001 @20190619A

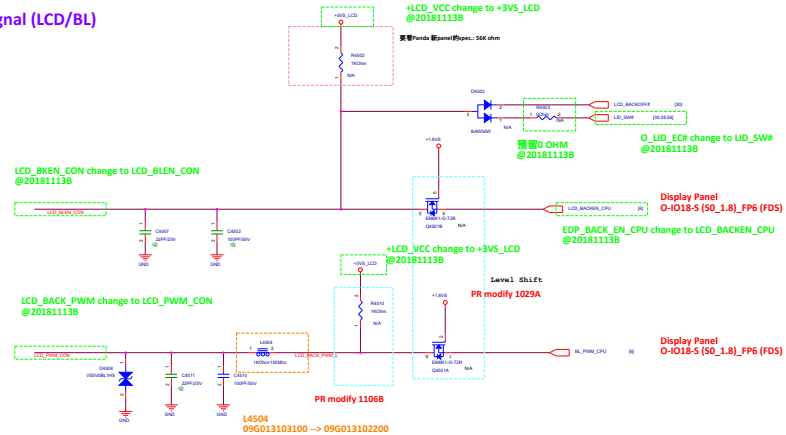


<Core Design>

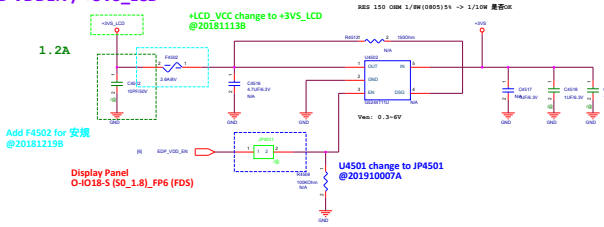
ASUSTeK COMPUTER	Title : FAN_Thermal Sensor & Fan	
	Engineer: EE	
Size: C	Project Name: GX502GX	Rev: 1.0
Date: Tuesday, April 28, 2020	Sheet 50 of 104	

HDMI Switch

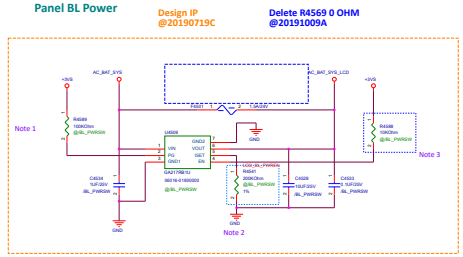
Controll Signal (LCD/BL)



LCD VDDEN / +3VS_LCD



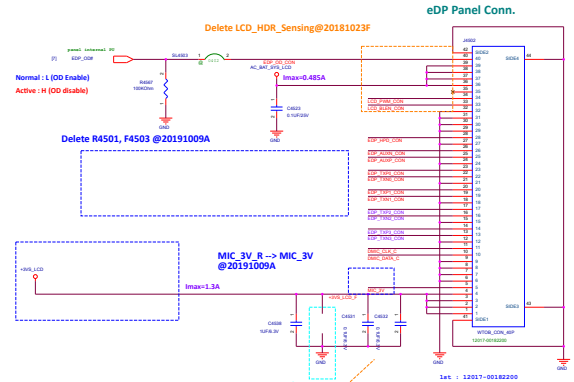
Panel BL Power



Add R4507 F4504
@20190719C

Delete R4507 F4504
@20191009A

eDP Panel Conn.



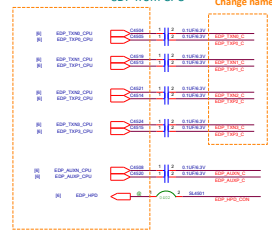
Remove C4503 for EMI LAN
@20181227G

@20190719D

PIN NO	Symbol	PIN NO	Symbol
1	NC	24	LCD GND
2	H_GND	25	LCD GND
3	Lane3_N	26	LCD GND
4	Lane3_P	27	HPD
5	H_GND	28	BL_GND
6	Lane2_N	29	BL_GND
7	Lane2_P	30	BL_GND
8	H_GND	31	BL_GND
9	Lane1_N	32	BL_Enable
10	Lane1_P	33	BL PWM DIM
11	H_GND	34	NC
12	Lane0_N	35	NC
13	Lane0_P	36	BL_PWR
14	H_GND	37	BL_PWR
15	AUX_CH_P	38	BL_PWR
16	AUX_CH_N	39	BL_PWR
17	H_GND	40	NC
18	LCD_VCC		
19	LCD_VCC		
20	LCD_VCC		
21	LCD_VCC		
22	LCD_Self_Test		
23	LCD GND		

Rename
@20181015B

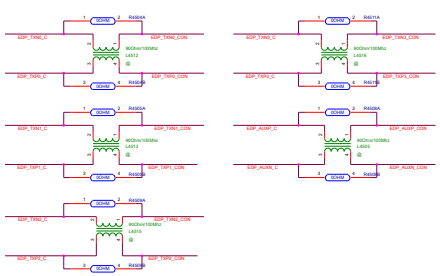
eDP from CPU



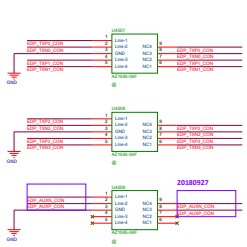
Change name Re-timer@20181023F

Delete Re-timer@20181023F

For EMI

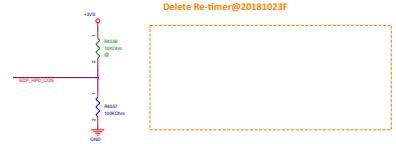


For ESD



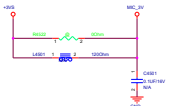
eDP_HPD (CPU)

Rename
@20181017H



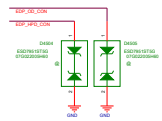
Delete Re-timer@20181023F

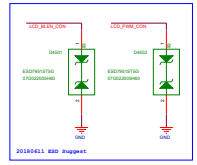
MIC module



MIC

For ESD

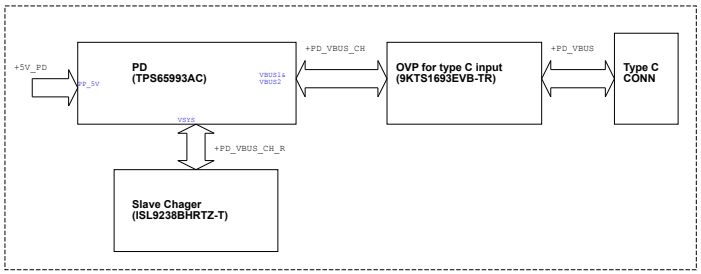




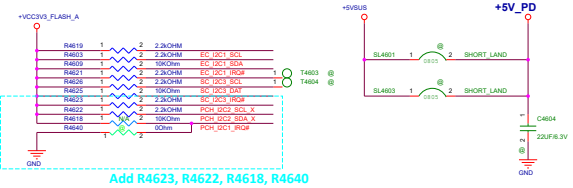
Delete @20181022M

Title :	CRT_eDP
Engineer:	EE
Project Name	GX502GX
Rev	1.0

Power Flow Chart

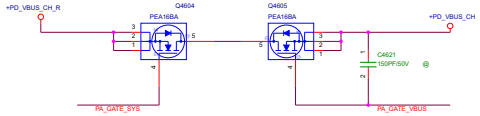


Imax=1port+1CC=3.6A



Add R4623, R4622, R4618, R4640
@20191105A

Delete R4606
@20190717F

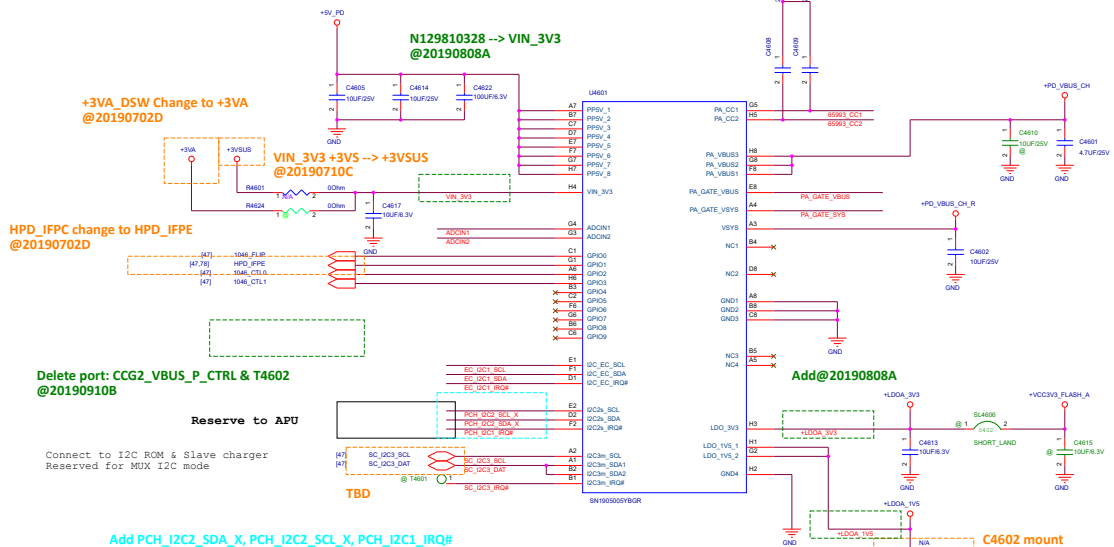


N129810328 --> VIN_3V3
@20190808A

+3VA_DSW Change to +3VA
@20190702D

VIN_3V3 +3VS --> +3VSUS
@20190710C

HPD_IFPC change to HPD_IFPE
@20190702D



Delete port: CCG2_VBUS_P_CTRL & T4602
@20190910B

Reserve to APU

Connect to I2C ROM & Slave charger
Reserved for MUX I2C mode

TBD

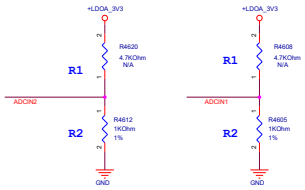
Add@20190808A

Add PCH_I2C2_SDA_X, PCH_I2C2_SCL_X, PCH_I2C1_IRQ#
@20191105A

C4602 mount
@20190719A

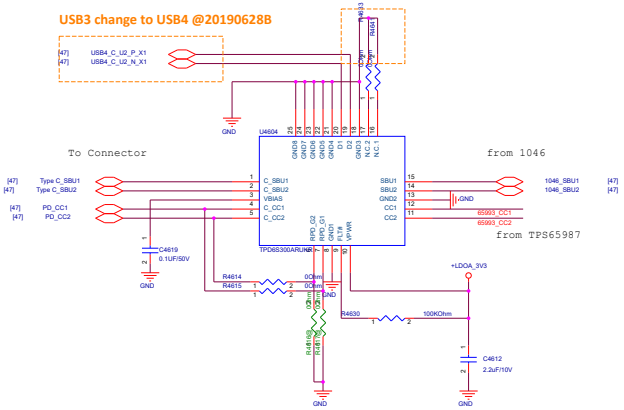
EC & Slave Charger

I2C Default Slave Address -> 0x42

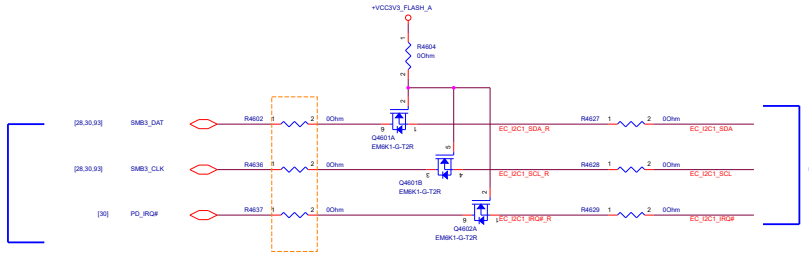


Change to R4633 R4641
@20190702D

USB3 change to USB4 @20190628B



Delete R4642 R4643 R4644
@20190718E



To PD

Delete R4607,R4610,R4611,Q4602B,Q4603
@20191014D

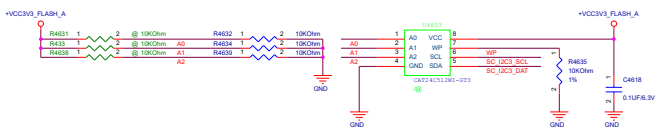
Add R4607 R4610 R4611
@20190718E

FW from PCH or APU

teknisi-indonesia

update I2C ROM to PD

I2C ROM



Change Q4603 net name, Pin 1 & 4 connect to I2C ROM, PD and MUX , Pin 3 & 6 connect to slave charger for reserved
@20190710C

ASUS	Project Name: Type-C_ALT_USB3-10G + DP + PD + Slave_Charger_TI		Rev: 1.0
Title : PD_TPS65993AC			
Size: Custom	Dept.:	Engineer: Design IP	
Date: Tuesday, April 28, 2020	Sheet: 46 of 104		

Main Board

U3808, U3807 06016-02010000 -->06016-00030100
@20190718D

USB3.1 Gen1 Port 0 support charge circuit

Max 2A

@20190715D

USB3_1_OC#0 --> USB3_0_OC#0
+5V_USB3_1 --> +5V_USB3_0
+5V_USB3_1_CON --> +5V_USB3_0_CON
@20190713A

USB3.1 Gen1 Port 0

12013-00054300

USB Port0
Left connector

U3808, U3807 06016-02010000 -->06016-00030100
@20190718D

Max 2

@20190715D

USB3.1 Gen1 Port 1

USB Port1
Right down connector

12013-00054300

USB3.1 Gen1 Port5

USB Port5
Right connector

12013-00054300

USB3_2_OC#1 --> USB3_1_OC#1
+5V_USB3_0_2_OUT -->+5V_USB3_1
+5V_USB3_2_CON --> +5V_USB3_1_CON
+5V_USB3_0_CON --> +5V_USB3_5_CON
@20190713A

HALL SENSOR
06033-00210000

06045-00040000 --> 06033-00210000
@20190830A

current: 1mA

USB3.1 Gen1 Port0

U3_U3TXDP1 change to USB0_TXP @20190606A

U3805 U3809 U3810 change to mount
@20190628B

Add @20190619C

USB3.0 EMI-Protection

C3855 C3856 C3859 C3860 C3863 C3864
0.1UF --> 0.22UF
@20190711B

Close to Connector side

redriver suggest

USB3.1 Gen1 Port 0

Delete R3831 C3849 R3832 C3850
@20190725A

R3837-R3844 unmount
C3859-C3866 unmount
C3840-C3843 C3845-C3848 mount
R3846-R3847, C3839 C3844 mount
C3825-C3828, C3802, C3806, C3821, C3833 mount
@20190923A

USB3.1 Gen1 Port1

Delete R3835 C3853 R3836 C3854
@20190725A

USB3.1 Gen1 Port5

Delete R3835 C3853 R3836 C3854
@20190725A

USB1_DP_RC --> USB1_DP
@20190904B

USB3.0 ESD-Protection

ESD PROTECTION
1st Source: P/N 07024-01360000 ESD PROTECTION AZ5865-01B

USB3.1 Gen1 Port5

Redriver Control strap pin

	USB1		USB2		USB3	
	USB1_C1	USB1_C2	USB2_C1	USB2_C2	USB3_C1	USB3_C2
PULL HIGH	DNI: unmout	DNI: unmout	DNI: unmout	DNI: unmout	DNI: unmout	DNI: unmout
OPEN MEDIUM						
PULL LOW	DNI: unmout	DNI: unmout	DNI: unmout	DNI: unmout	DNI: unmout	DNI: unmout

DNI: unmout
NI: mout

CPU 到 USB redriver 長度: 11 inch -> 建議先使用Medium (原是Ball 再改Low)
Vendor layout 建議: 每一段等長至5mil 以內; 建議穿環植能換2次 ;

Add @20200420A

USB2.0 ESD-Protection

07024-02000200

1st Source: P/N 07024-01360000 ESD PROTECTION AZ5865-01B

USB3.1 Gen1 Port 0

USB2.0 EMI-Protection With ECMF(PCB 1.05mm_10Layer)

From CPU USB2.0 Port

Rename
@20190725A

USB Port0
Left connector

Note : 1. This part & symbol only apply for standard PCB stack-up listed in datasheet appendix I
Please check your project must matching the thickness , DF and DK value of PCB every layer
2. C3859&C3810 must replaced with 18pF 0201 capacitors and the tolerance of capacitance value is 5%
3. Pin7 & Pin8 & Pin11 & Pin12 must be connected to system ground
4. Pin13 to Pin16 are floated in regular scheme

temp_M08_000010層名順序是：TOP/GND/IN1/GND1/IN2/VCC/GND2/IN3/GND3/BOTTOM

USB3.1 Gen1 Port1

USB2.0 EMI-Protection With ECMF(PCB 1.05mm_10Layer)

From CPU USB2.0 Port

USB Port1
Right down connector

Note : 1. This part & symbol only apply for standard PCB stack-up listed in datasheet appendix I
Please check your project must matching the thickness , DF and DK value of PCB every layer
2. C3811&C3812 must replaced with 18pF 0201 capacitors and the tolerance of capacitance value is 5%
3. Pin7 & Pin8 & Pin11 & Pin12 must be connected to system ground
4. Pin13 to Pin16 are floated in regular scheme

temp_M08_000010層名順序是：TOP/GND/IN1/GND1/IN2/VCC/GND2/IN3/GND3/BOTTOM

USB3.1 Gen1 Port5

USB2.0 EMI-Protection With ECMF(PCB 1.05mm_10Layer)

From CPU USB2.0 Port

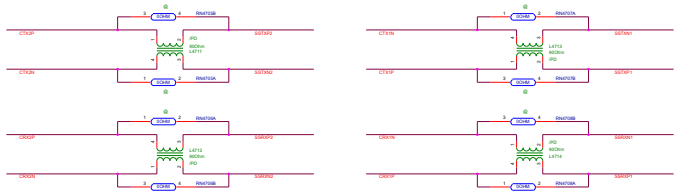
USB Port5
Right connector

Note : 1. This part & symbol only apply for standard PCB stack-up listed in datasheet appendix I
Please check your project must matching the thickness , DF and DK value of PCB every layer
2. C3811&C3812 must replaced with 18pF 0201 capacitors and the tolerance of capacitance value is 5%
3. Pin7 & Pin8 & Pin11 & Pin12 must be connected to system ground
4. Pin13 to Pin16 are floated in regular scheme

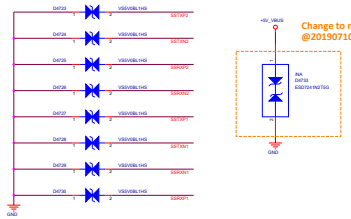
temp_M08_000010層名順序是：TOP/GND/IN1/GND1/IN2/VCC/GND2/IN3/GND3/BOTTOM

Title : Aud_HP Jack, MIC
Engineer: EE
GX531GX

USB EMI-Protection



USB3.0 ESD-Protection

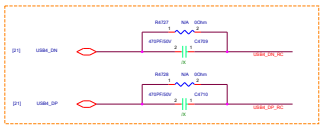


NOTE 8. PIN ASSIGNMENT (FRONT VIEW)

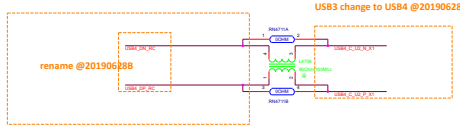
Pin No.	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
	GND	TX1+	TX1-	V_{BUS}	CC1	D+	D-	SBU1	V_{BUS}	RX2-	RX2+	GND
	GND	RX1+	RX1-	V_{BUS}	SBU2	D-	D+	CC2	V_{BUS}	TX2-	TX2+	GND
Pin No.	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

NOTE 9. LASER WELD POINTS MAY BE DISCOLORED.

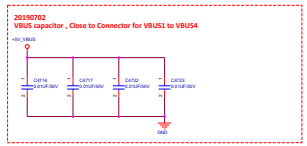
Add RC @20190628B

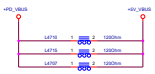


Delete 65987_USB2_N_BC12, 65987_USB2_P_BC12
R4729 & R4724
@20190704A

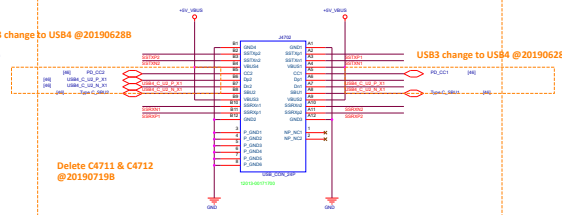


Add C4716 C4717 C4722 C4723
@201907198

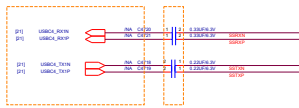




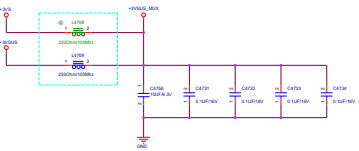
TYPE-C Connector



C4718 C4719 0.1uf --> 0.22uf
C4720 C4721 0.1uf --> 0.33uf
@20190715A



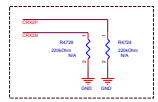
Change L4709、L4708 from 120 ohm to 220 ohm to meet reference schematic and increase power trace
@20191105A

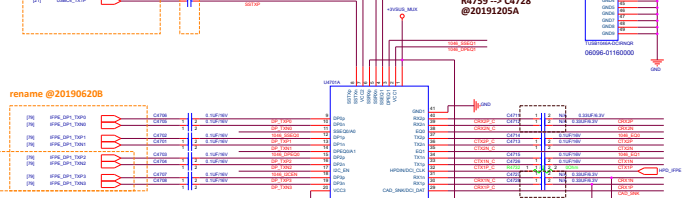


R4756 --> C4711
R4757 --> C4712
R4758 --> C4727
R4759 --> C4728
@20191205A

Delete C4711 C4712 C4727 C4728
Add R4732
@20190909A

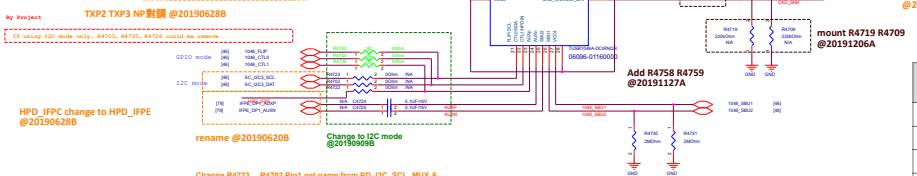
mount R4719 R4709
@20191206A





HPD_IFPC change to HPD_IFPE
@20190621G

TXP2 TXP3 NP對調 @20190628B



Change R4723 、R4702 Pin1 net name from PD_I2C_SCL_MUX & PD_I2C_SDA_MUX to SC_I2C3_SCL & SC_I2C3_DAT
@20190710C

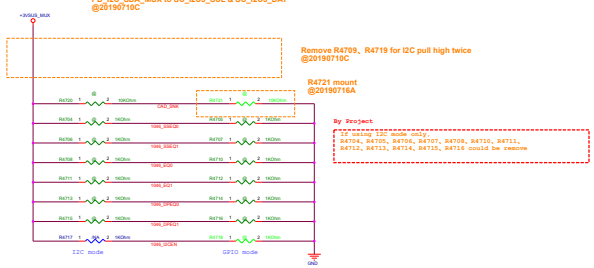
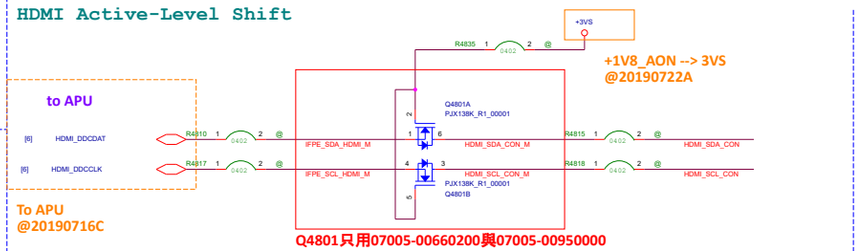


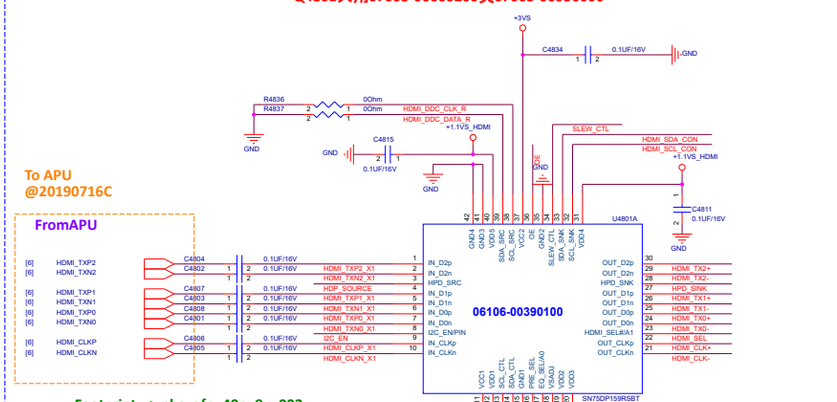
Table 2. GPIO Configuration Control

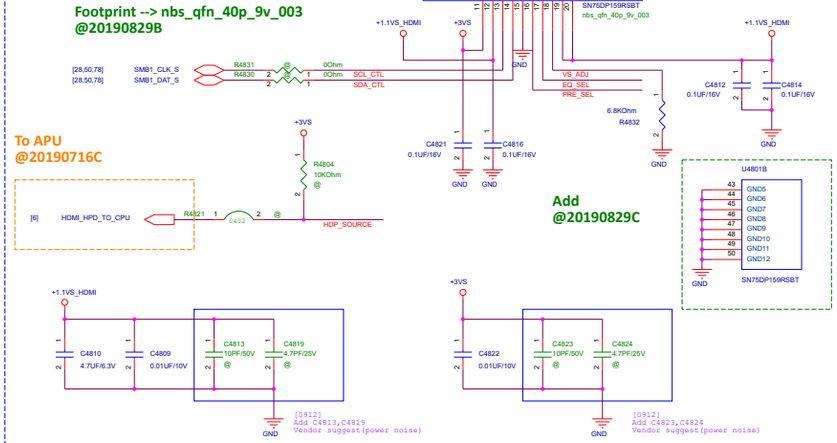
CTL1 PIN	CTL0 PIN	FLIP PIN	TUSB1046-DCI CONFIGURATION	VESA DisplayPort ALT MODE DFP_D CONFIGURATION
L	L	L	Power Down	—
L	L	H	Power Down	—
L	H	L	One Port USB 3.1 - No Flip	—
L	H	H	One Port USB 3.1 – With Flip	—
H	L	L	4 Lane DP - No Flip	C and E
H	L	H	4 Lane DP – With Flip	C and E
H	H	L	One Port USB 3.1 + 2 Lane DP- No Flip	D and F
H	H	H	One Port USB 3.1 + 2 Lane DP– With Flip	D and F

Main Board

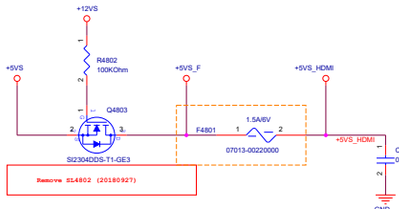
HDMI Active-Level Shift





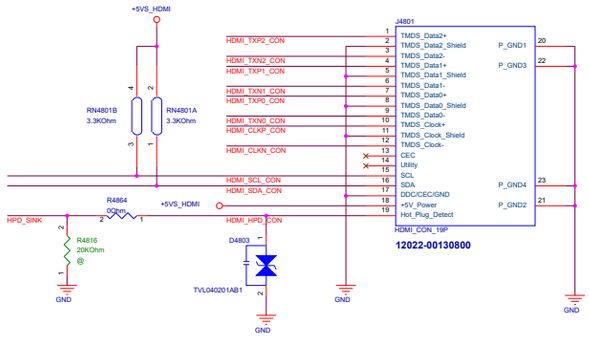


HDMI PWR_+5VS_HDMI

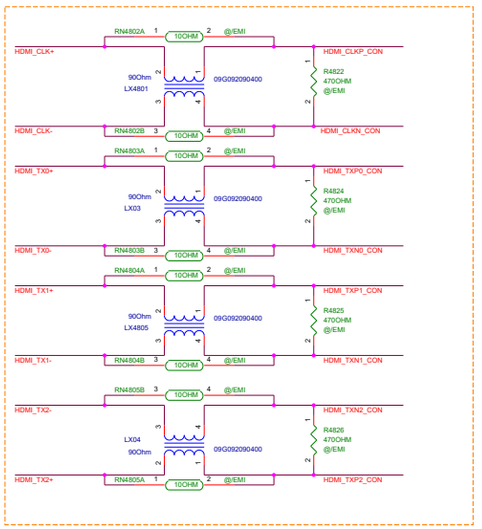


F4801 change to 07013-00220000
@20190626E

HDMI Conn.

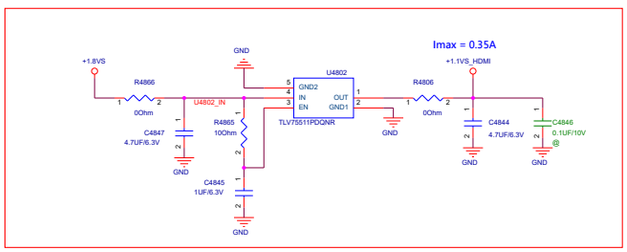


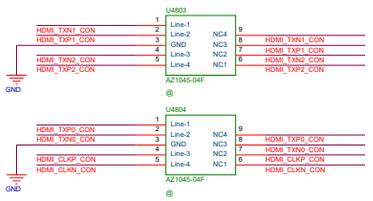
HDMI EMI

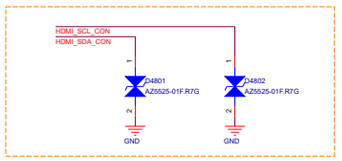


Add Co-lay device
@20190626E

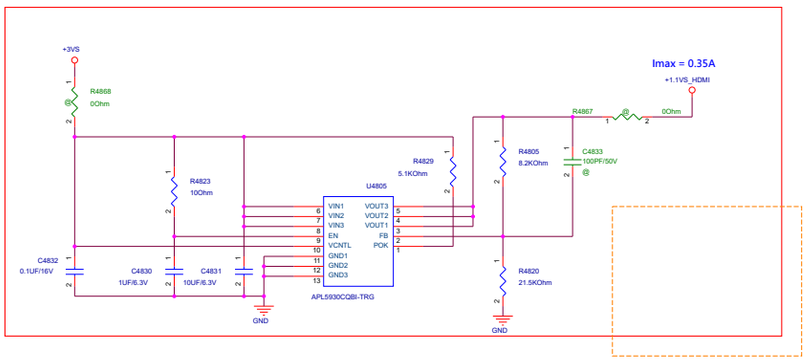
HDMI LDO 1.1VS







D4801/4802 change to 07024-00880000
@20190705C



Delete C4820 C4828
@20190626E

Slew rate control when I2C_EN/PIN = Low.
SLEW_CTL = H, fastest data rate
SLEW_CTL = L, 5 ps slow
SLEW_CTL = No Connect, 10 ps slow

HDMI_SEL when I2C_EN/PIN = Low
HDMI_SEL = High: Device configured for DVI
HDMI_SEL = Low: Device configured for HDMI

Input Receive Equalization pin strap when I2C_EN/PIN = Low
EQ_SEL = L: Fixed EQ at 7.5 dB
EQ_SEL = No Connect: Adaptive EQ
EQ_SEL = H: Fixed at 14 dB

De-emphasis pin strap when I2C_EN/PIN = Low.
PRE_SEL = L: - 2 dB de-emphasis level
PRE_SEL = No Connect: 0 dB
PRE_SEL = H: Reserved

I2C_EN/PIN = High; puts device into I2C control mode
I2C_EN/PIN = Low; puts device into pin strap mode

Operation enable/reset pin
OE = L: Power-down mode OE = H: Normal operation
Internal weak pullup: Resets device when transitions from H to L

Project Name	Rev
Design IP	0.1A

Title : HDMI ReTimer_Revision History_R0.1A

Size	Dept.:	Engineer:
Custom	ASUSTeK COMPUTER	EE

Date: Tuesday, April 28, 2020 Sheet 48 of 104

TYPE-C USB3.1

<Core Design>

Title : BT_Bluetooth

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
C	GX502GX	1.0

Date:	Tuesday, April 28, 2020	Sheet	61	of	104

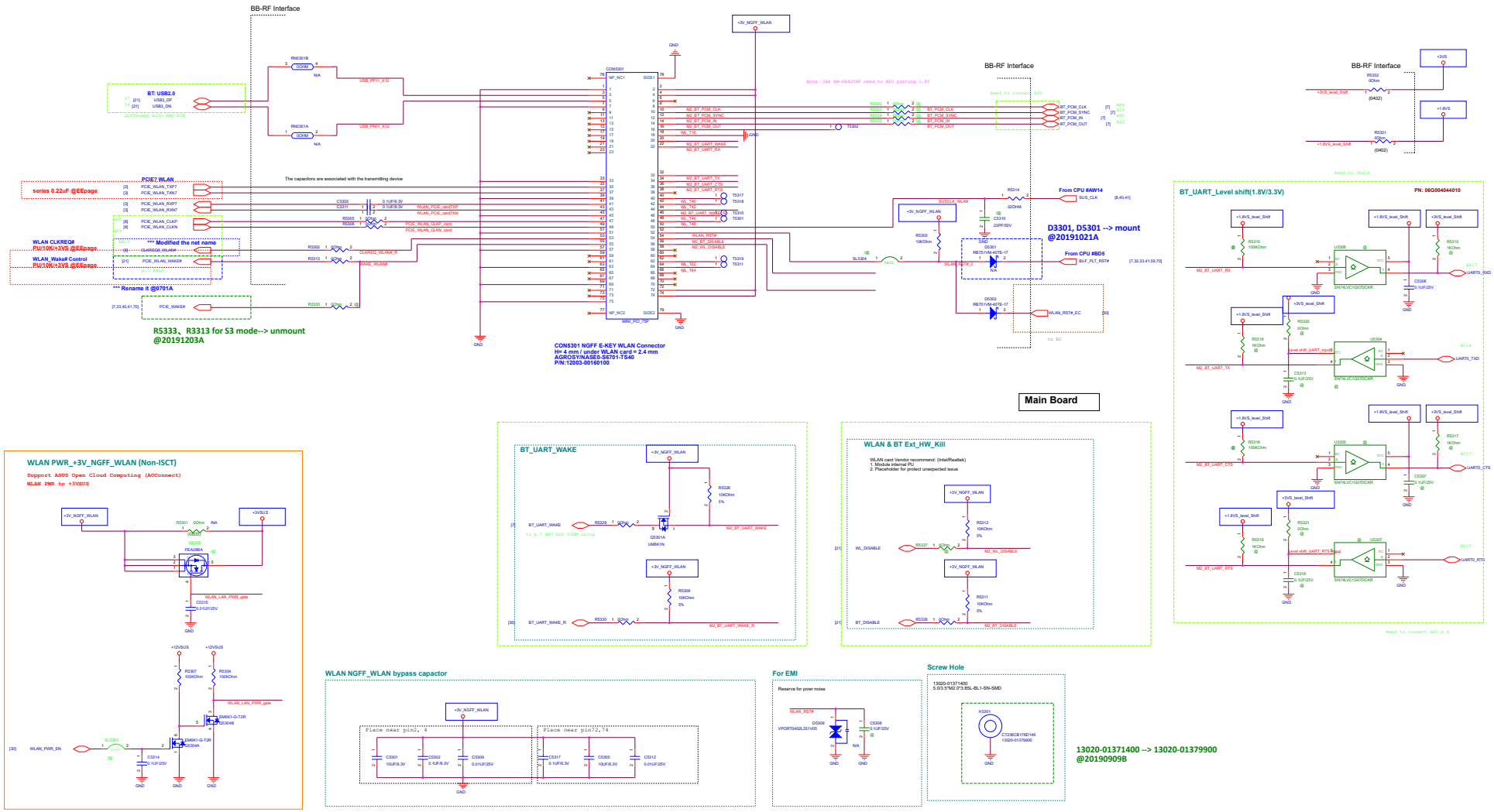
Title : USB Charger

Engineer: EE

Size: A3 | Project Name: GX502GX | Rev: 1.0

Sheet 53 of 59

NGFF M.2 TYPE_E-KEY WIFI



Title	NGFF Type_WLAN&BT
Engineer:	RF
ASUSTeK COMPUTER	
Project Name	GA502IV
Rev	R1.0
Date	Tuesday, April 28, 2020

Title : NGFF SSD(MAXIM)

ASUSTeK COMPUTER

Engineer: Wendell_Lo

Size	Project Name	Rev
D	GL752VW	1.0

Date: Tuesday, April 28, 2020 Sheet 63 of 104

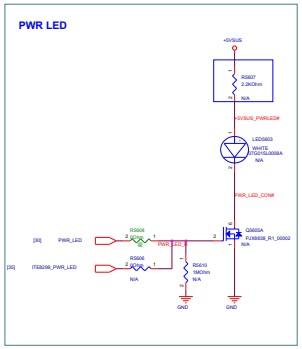
Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, April 28, 2020	Sheet 54 of 104	

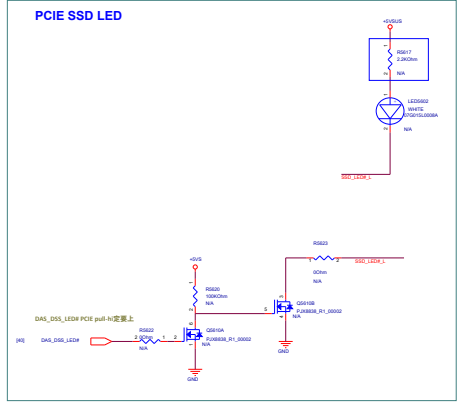
Title :

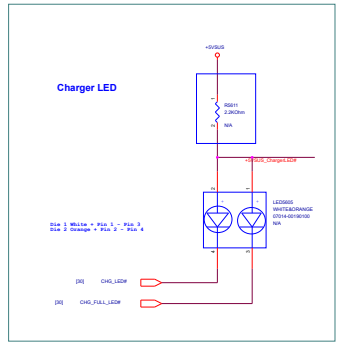
ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
A	**GX502GX**	1.0

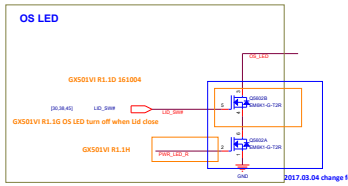






@20181013C

PWR LED	PCIE SSD LED	Charger LED



2017.03.04 change for DXF Limitation

/FP change to @/FP
@20191003A

MB_PWR BUTTON CON._10PIN & 4PIN co-lay

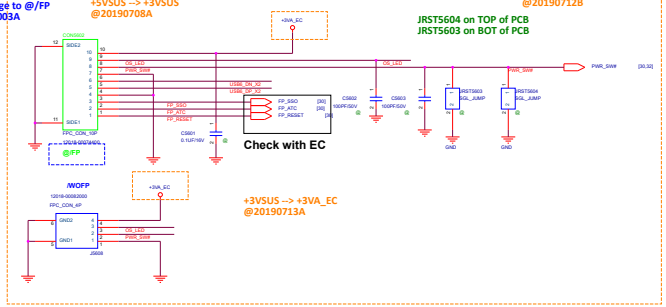
JS607 change to CON5602
+5VSUS --> +3VSUS
@20190708A

50mA

Connected to Power Key Board 55

Change pin define
@20190712B

JRST5604 on TOP of PCB
JRST5603 on BOT of PCB



+3VSUS --> +3VA_EC
@20190713A

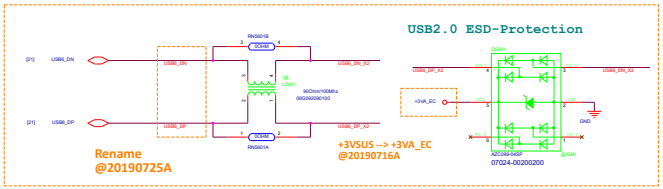
KB connector change to P.31
@20190731C

CAPS LOCK LED
@20181015C

CAP LED

Change to monut @ 20181129A

FP No	GA502 FP Pwrbtn	GA502 小板	GA502 小板 pin No
10	LED+	LED+	4
9	LED-	LED-	3
8	PWRBTN	PWRBTN	2
7	GND	GND	1
6	USB_D-	-	-
5	USB_D+	-	-
4	GND	-	-
3	SSO	-	-
2	ATC	-	-
1	RESETn	-	-



Delete R5609 C5604 R5612 C5605
@20190725A

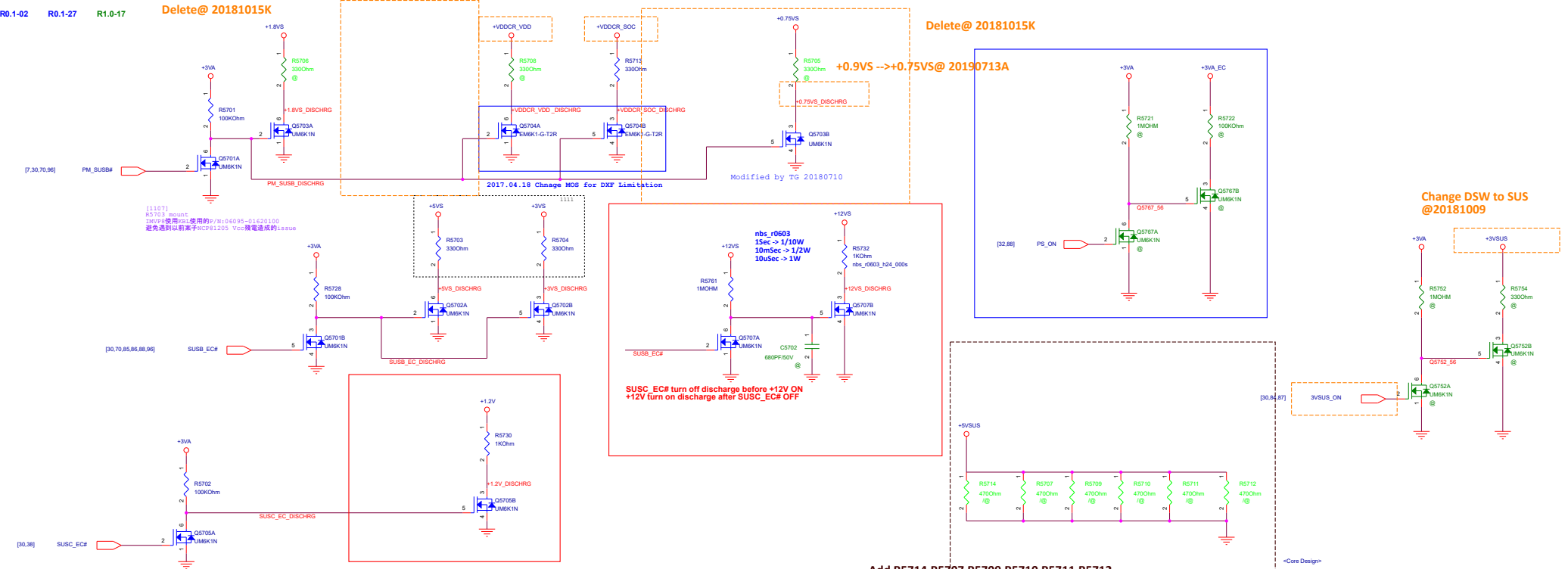
R0.1-02 R0.1-27 R1.0-17

Delete@ 20181015K

Delete@ 20181015K

+0.9VS -->+0.75VS@ 20190713A

Change DSW to SUS
@20181009



<Core Design>

ASUSTeK COMPUTER

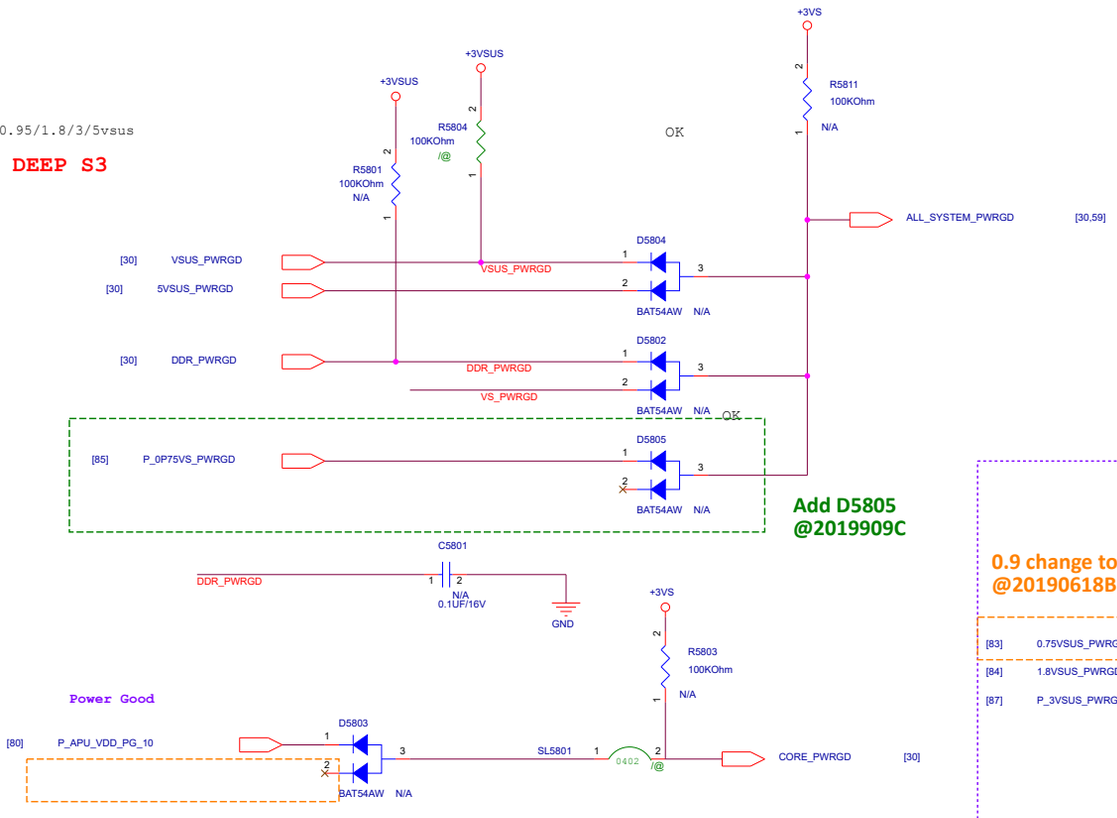
Title : DSG_Discharge

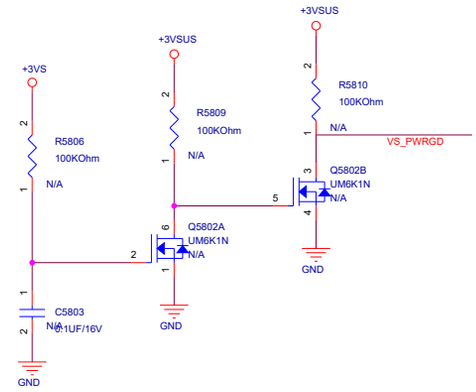
Engineer: EE

Size	Project Name	Rev
Custom	GX502GX	1.0

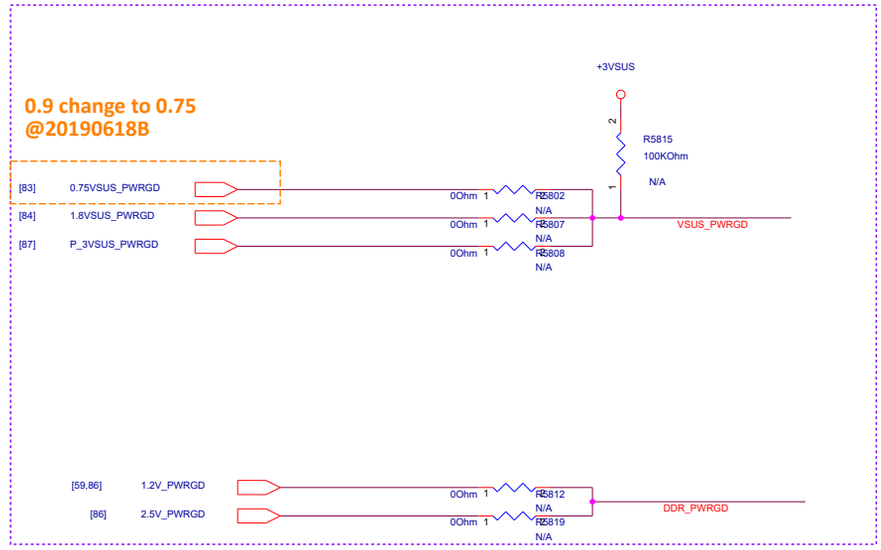
Date: Tuesday, April 28, 2020 Sheet 57 of 104

POWER GOOD DETECTER





Power Good



Remove AMD GPU PWRGD
@20181009K

Project Name: FX505DY		Rev: R1.0
Title : POWER GOOD DETECTER		
Size: Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: RD2 EE3	
Date: Tuesday, April 28, 2020	Sheet 58 of 104	

<Core Design>

Title : OTH_for test only

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
A	GX502GX	1.0

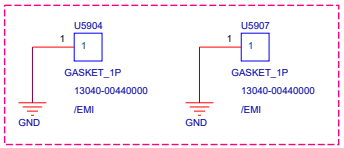
Date:	Tuesday, April 28, 2020	Sheet	68	of	104

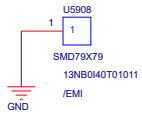
EMI1 SPRING (4.7H) 13060-00570000*1

EMI2 SPRING (2.6H) *3
13NB0I50M01011

EMI2 SPRING (4H) *3
13NK00B1M01011

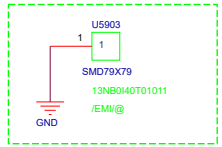
U6906 U6910 change to 13040-00440000(SMT Gasket H=2.5mm)
@20190213A



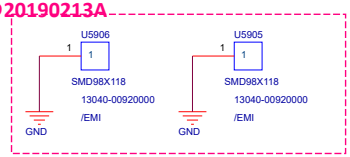


Delete U6912 U6913
@20190626A

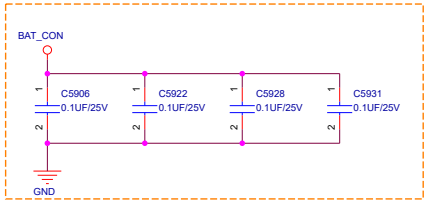
Modify @20181122A(EMI req.)

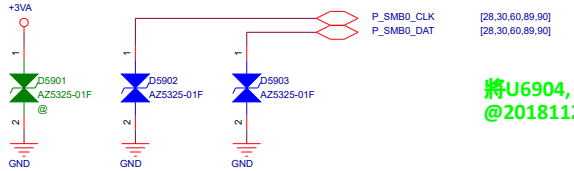


U6907 U6909 change to 13040-00920000(SMT Gasket H=3mm)
@20190213A



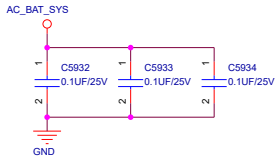
EMI request @20181026A

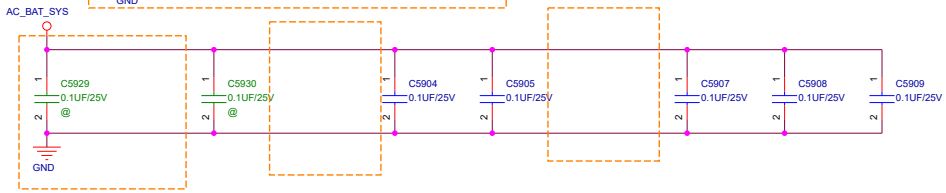




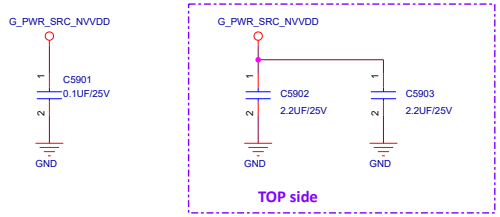
將U6904, U6908(改裸銅), U6905(改裸銅) 移除
@20181122C

2017/04/05 EMI

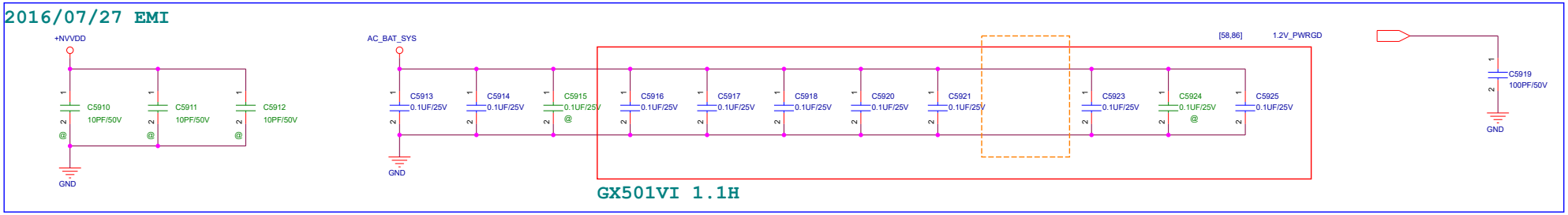


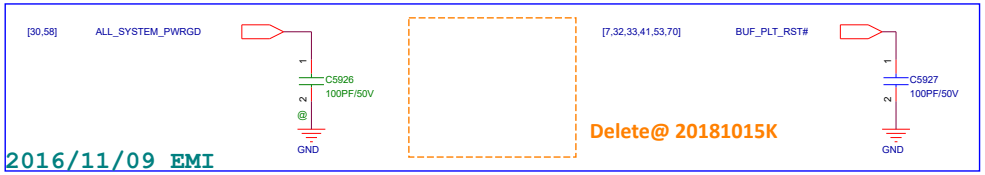


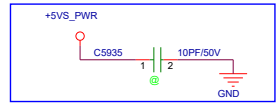
4/2 for EMI



2016/07/27 EMI







<Core Design> 2017.05.02 EMI Reserve

ASUSTeK COMPUTER

Title : OTH_EMI

Engineer: EE

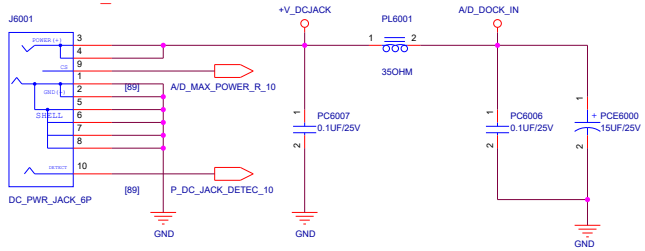
Size	Project Name	Rev
B	GX502GX	1.0

Date: Tuesday, April 28, 2020 Sheet 59 of 104

DC-IN Connector

DC Jack使用請詢用River_Hsu

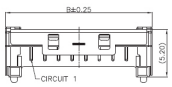
New 6 Phi 4 Pin DC_Jack

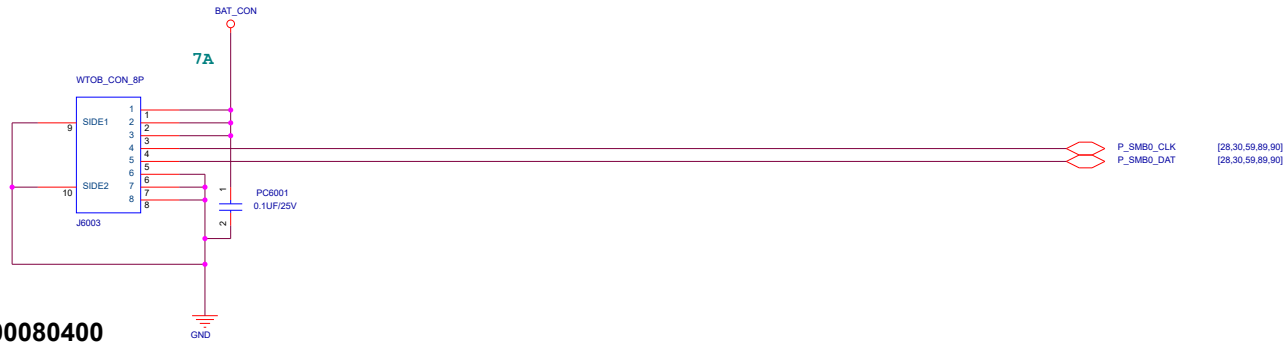


CHIP Cap (H=2.1)

	3.4CH	1.55CH
J6001	12033-00020200	12033-00020300

Battery Connector





12017-00080400

Note:Battery Connector 正確性與BAT1_IN_OC#是否預留!

ASUS	Project Name: GA502IV		Rev: R1.0
Title : DC & BAT IN			
Size: A3	Dept.: NB_Power team	Engineer: CS Lin	
Date: Tuesday, April 28, 2020	Sheet 60 of 104		

Title : I/O board Audio/USB

ASUSTeK COMPUTER

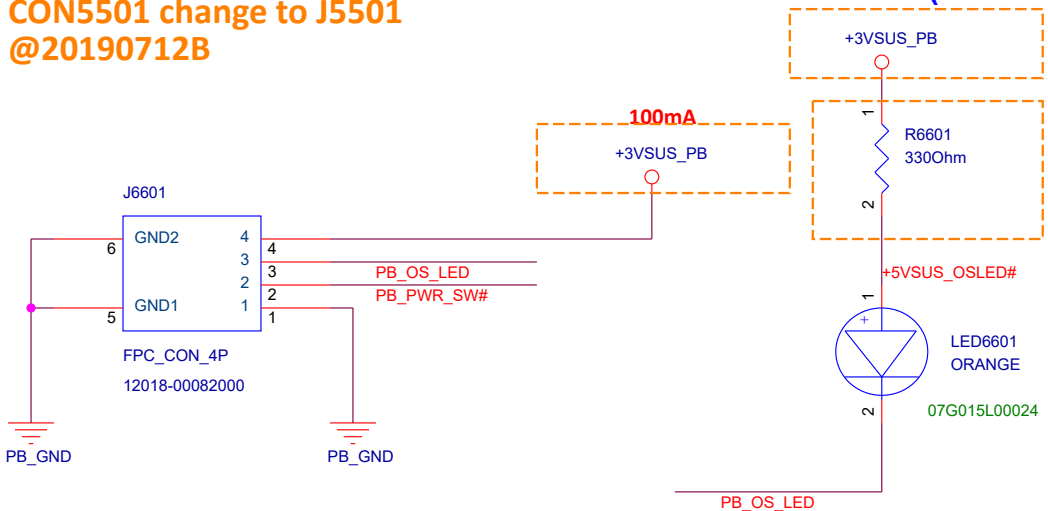
Engineer: Wendell_Lo

Size	Project Name	Rev
C	GL752VW	1.0

Connected to MB Page56

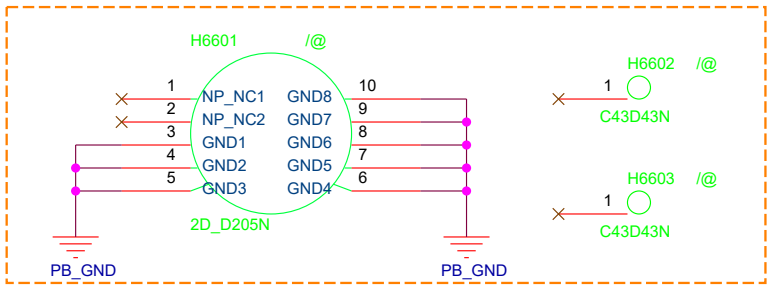
CON5501 change to J5501 @20190712B

OS LED (PWRBTN)

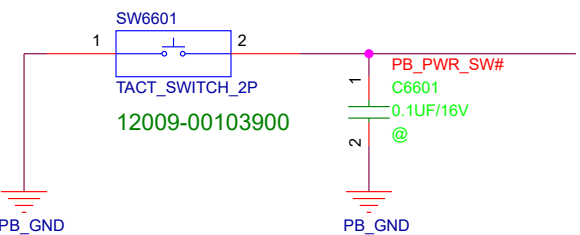


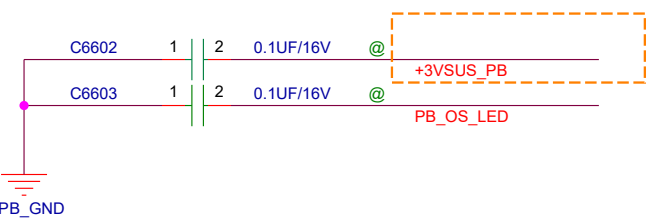
+5VSUS_PB --> +3VSUS_PB
R5510 750 OHM --> 330 OHM
@20190708A

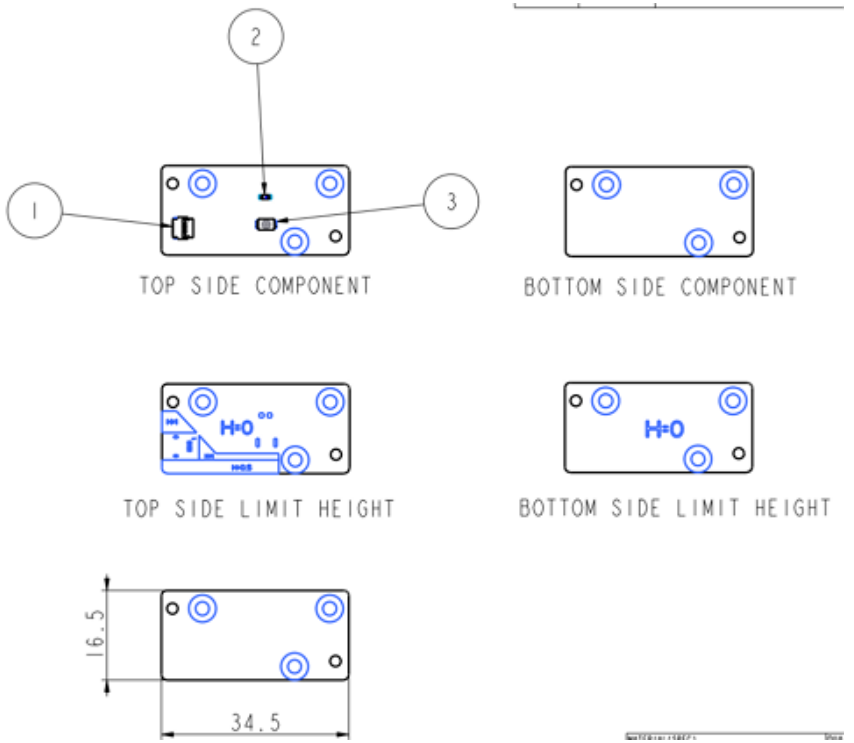
Change @20181026B



POWER button







<Core Design>

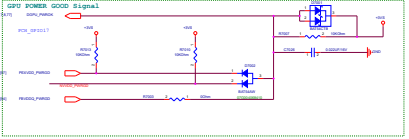
ASUSTeK COMPUTER	Title : IO Con. to MB		
	Engineer: EE		
Size: A	Project Name: GX502GX		Rev: 1.0
Date: Tuesday, April 28, 2020	Sheet 66 of 104		

<Core Design>

ASUSTeK COMPUTER	Title : ME_Screw Hole & Nut	
	Engineer: EE	
Size: A	Project Name: GX502GX	Rev: 1.0
Date: Tuesday, April 28, 2020	Sheet 67 of 104	

<Core Design>

ASUSTeK COMPUTER	Title : I/O_Main board Conn.	
	Engineer: EE	
Size: A	Project Name: GX502GX	Rev: 1.0
Date: Tuesday, April 28, 2020	Sheet 69 of 104	



NVVDD POWER GOOD LOOPBACK

Remove Q7005A, Q7002B, R7018, Q7002A
@20190716A

GPU POWER SEQUENCE CONTROL

Add DGPU_PWR_EN# for GPU GCOFF

GC6 follow GL704GW
@20190717D

06004-01350000 change to 06004-01410000 @20190606B

U7002重新吸料
@20190627D

AGPIO12 change to DGPU_PWR_EN#_AGPIO12
@20190703B

Delete R7011, DGPU_PWR_EN#
@20190910B

1016_參考GL704GW線路

Main Board

電容數量未符合Reference

REQ6-> REQ0
@20190624A

REQ6-> REQ0
@20190624A

CLKREQ6_GPU# --> CLKREQ0_GPU#
@20190624A

0.47UF/4V --> 1UF/6.3V
@20191125A

0.47UF/4V --> 1UF/6.3V
@20191125A

0.47uF x 16
4.7uF x 3

10uF x 3
22uF x 2

0.47UF/4V --> 1UF/6.3V
@20191125A

0.47uF x 10
4.7uF x 3

10uF x 3
22uF x 2

For EMI

teknisi-indonesia

ASUS	Project Name: GX502GX	Rev: 2.0
Title : GPU_PDE IF		
Size: Custom	Dept.:	Engineer:
Date: Tuesday, April 28, 2020	Sheet 79 of 105	

40 OHm_NET
FBA_Partition 31..0
MF=1 Mirror

40 OHm_NET
FBA_Partition 64..32
MF=0 Normal

待換Samsung 03014-00010100

U73001

待換Samsung 03014-00010100

U73002

VRAM unomunt. Please Add VG BOM
@20191128A

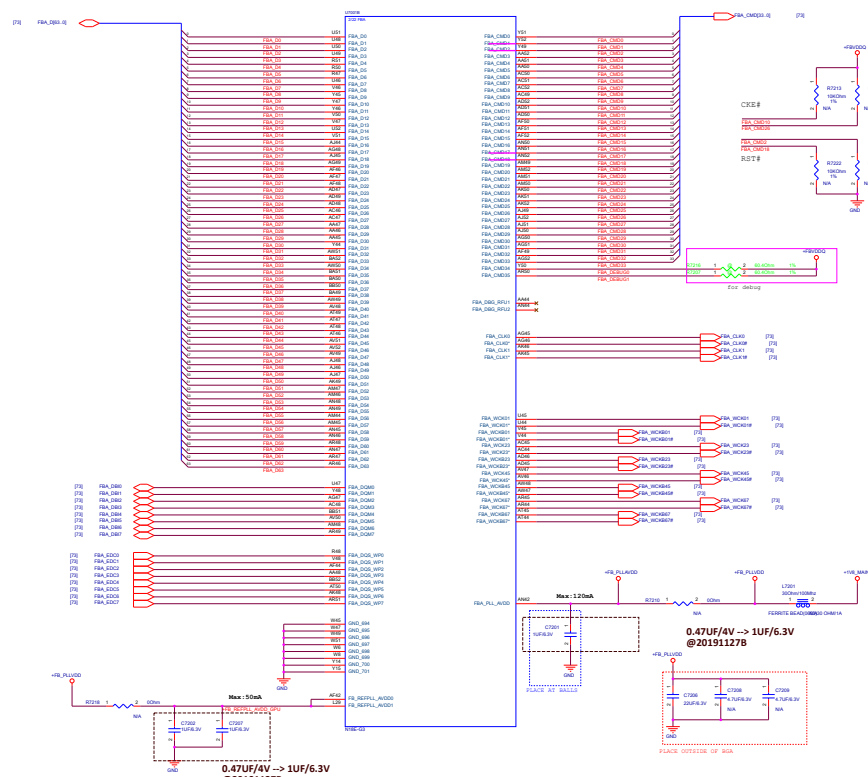
<Core Design>

<Title>

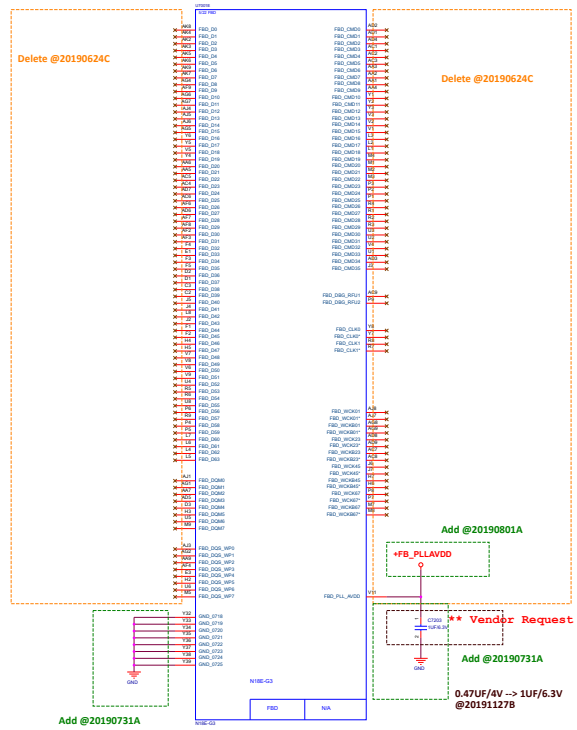
Document Number
GX30G024

Tuesday, April 28, 2020

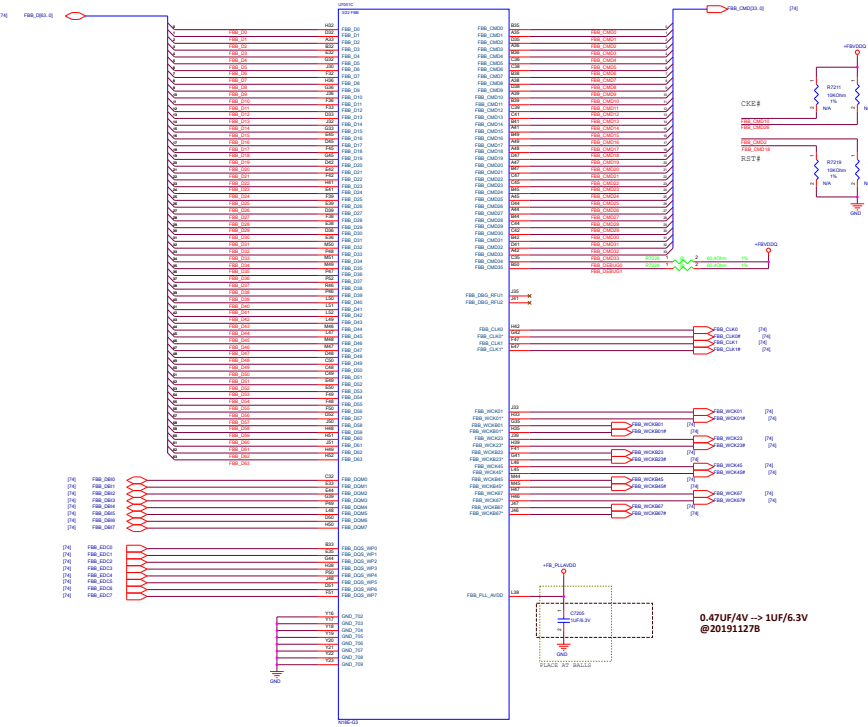
MEMORY: GPU FB Partition A



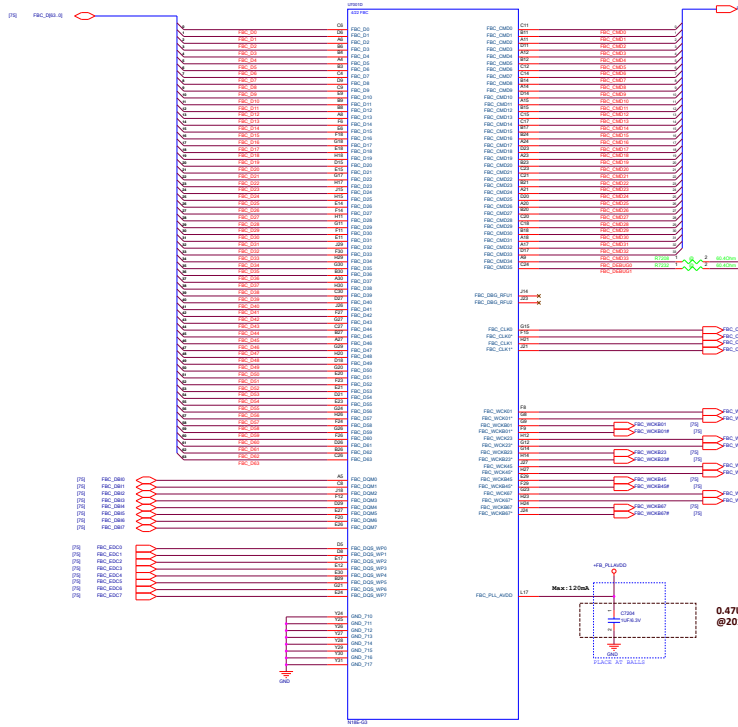
MEMORY: GPU FB Partition D



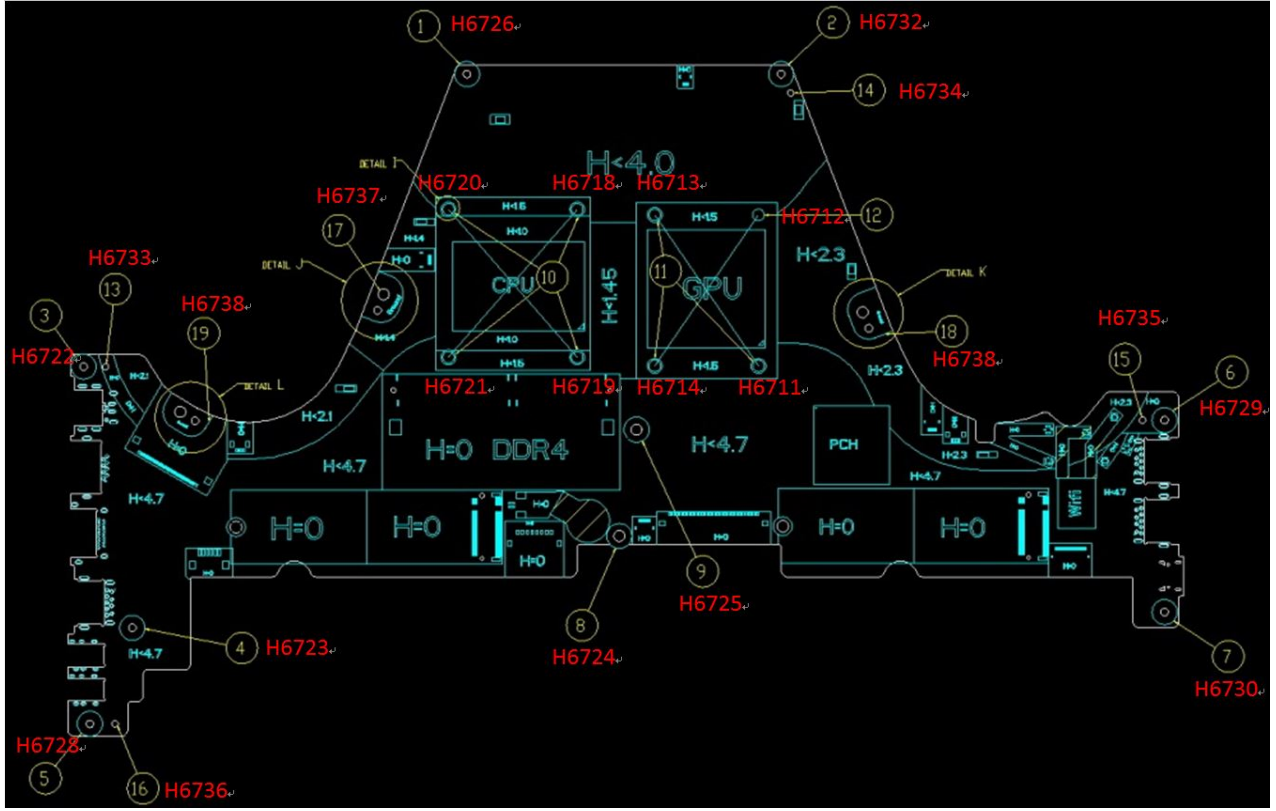
MEMORY: GPU FB Partition B



MEMORY: GPU FB Partition C



ASUS	Project Name: GX502GX		Rev: 81.0
Title : GPU_FRAME BUFFER			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE1_RD1	
Date: Tuesday, April 28, 2020	Sheet: 73 of 104		



GPU

TOP 3.7/6.5, BOT 3.7/4.7

H6511 1 @ CT256CB185D146

H6512 1 @ C146D146N

H6513 1 @ CT256CB185D146

H6514 1 @ CT256CB185D146

CPU

TOP 3.7/6.5, BOT 3.7/4.7

H6517 1 @ CT256CB185D146

H6518 1 @ CT256CB185D146

H6519 1 @ CT256CB185D146

H6520 1 @ CT256CB185D146

TOP&BOT 2.4/8

GND 1 H6525 C315D94 @

GND 1 H6529 C315D94 @

GND 1 H6521 C315D94 @

GND 1 H6522 C315D94 @

GND 1 H6527 C315D94 @

GND 1 H6528 C315D94 @

GND 1 H6515 C315D94 @

GND 1 H6516 C315D94 @

Add @20181029C

TOP&BOT 3.5/8

GND 1 H6523 C315D138 @

GND 1 H6524 C315D138 @

Change @20181023F

H6526

GND GND 1 2 3 NP_NC GND1 GND2 GND4 GND3 5 4 GND GND

C315D94N /@

H6531 1 C79D79N /@

Change @20181023F

NC @20181030B

H6530

GND GND 1 2 3 NP_NC GND1 GND2 GND4 GND3 5 4 GND GND

CT236D79N s12526 @

H6532

GND GND 1 2 3 NP_NC GND1 GND2 GND4 GND3 5 4 GND GND

CT236D79N s12526 @

Change @20181025A

GND 1 H6533 /@ GND NP_NC 2

2D_D138_D94N

GND 1 H6535 /@

CRT349X338CRB547X782D138

Change @20181023E

GND /@ 1 H6534 2

s12570 2D_D138_D94

<Core Design>

ASUSTeK COMPUTER

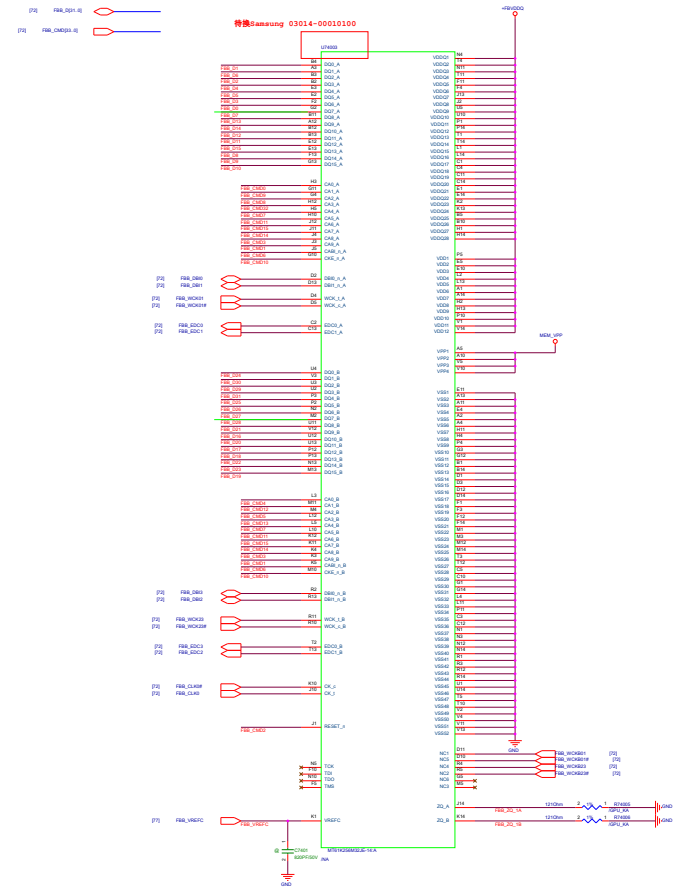
Title : I/O board FUNC key

Engineer: EE

Size	Project Name	Rev
B	GX502GX	1.0

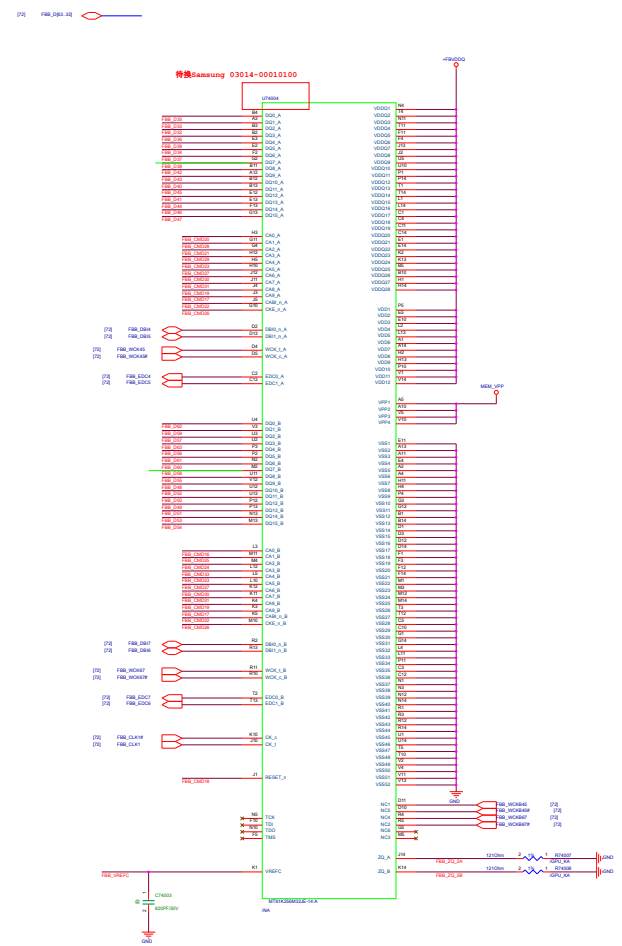
Date: Tuesday, April 28, 2020 Sheet 65 of 104

40 OHm_NET
FBB Partition 31..0
MF=1 Mirror



VRAM unomunt. Please Add VG BOM
@20191128A

40 OHm_NET
FBB Partition 64..32
MF=0 Normal

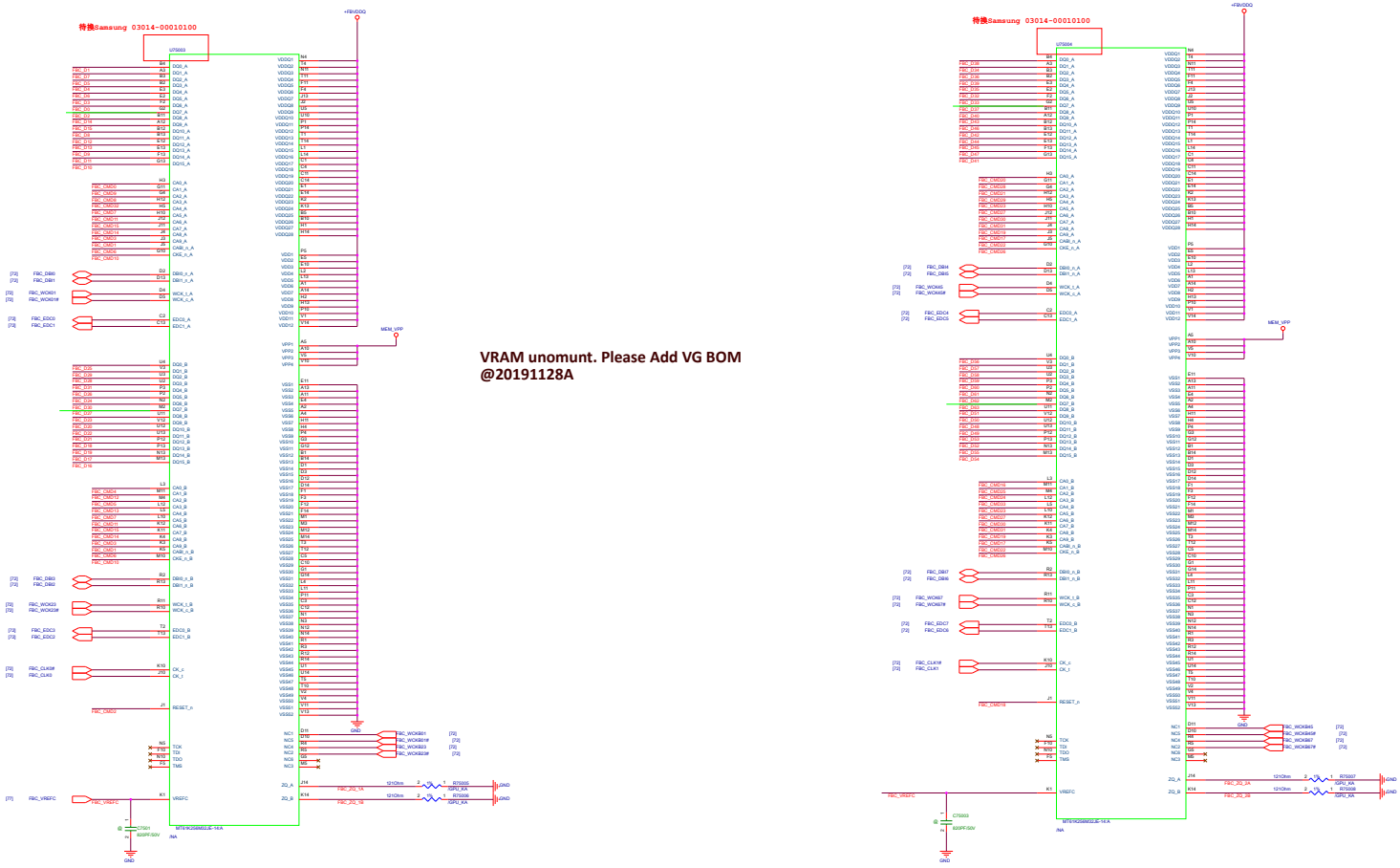


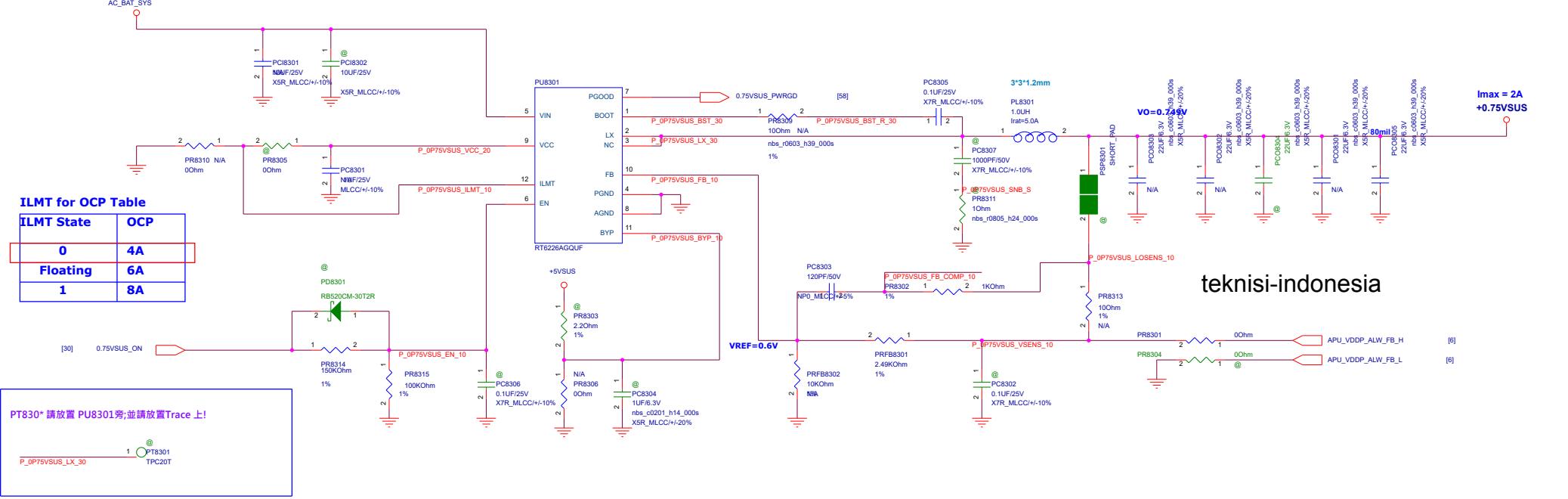
<Core Design>

Title	<Title>		
Size	Document Number		Rev
A1	GX60G04		0.0.0
Date:	Tuesday, April 28, 2020	Sheet	73 of 105

40 OHm NET
FBC Partition 31..0
MF=1 Mirror

40 OHm NET
FBC Partition 64..32
MF=0 Normal





ILMT for OCP Table

ILMT State	OCP
0	4A
Floating	6A
1	8A

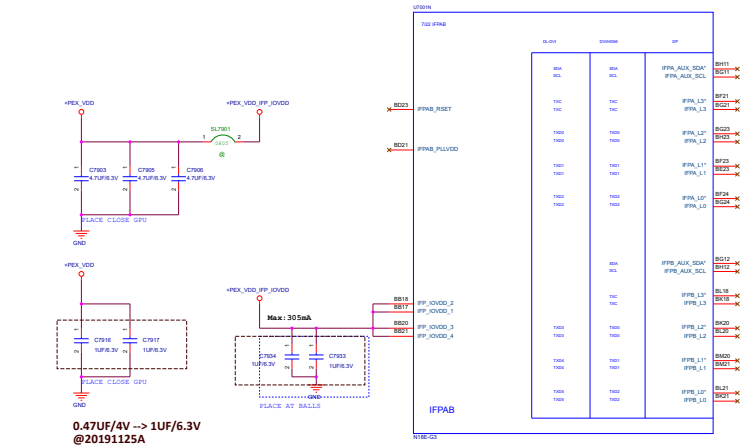
PT830* 請放置 PU8301旁;並請放置Trace 上!

P_0P75VSUS_LX_30 — PT8301 TPC20T

<Variant Name>

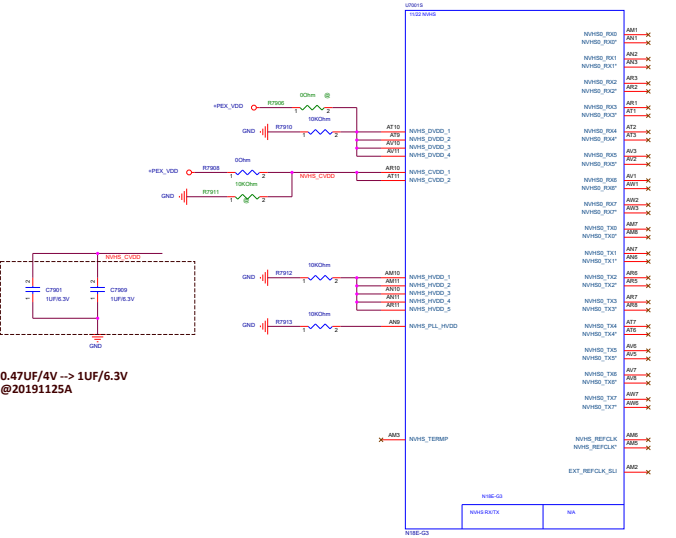
ASUS	Project Name: GA502IV	Rev: R1.0
Title : PW_+0.75VSUS		
Size: A3	Dept.: NB Power team	Engineer: CS Lin
Date: Tuesday, April 28, 2020	Sheet 83 of 104	

Delete @20190624B



0.47UF/4V --> 1UF/6.3V
@20191125A

NVLink (not used)



0.47UF/4V --> 1UF/6.3V
@20191125A

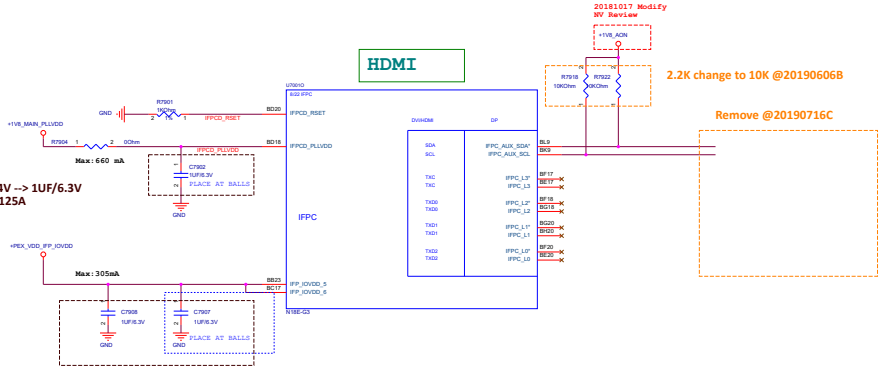
0.47UF/4V --> 1UF/6.3V
@20191125A

HDMI

20181017 Modify
NV Review

2.2K change to 10K @20190606B

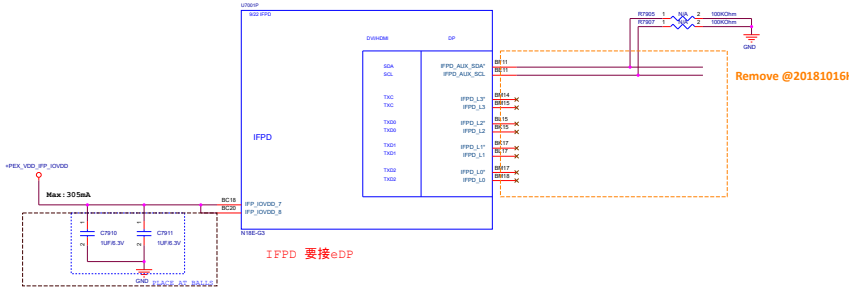
Remove @20190716C



0.47UF/4V --> 1UF/6.3V
@20191125A

EDP(4Lane Panel)

Remove @20181016H

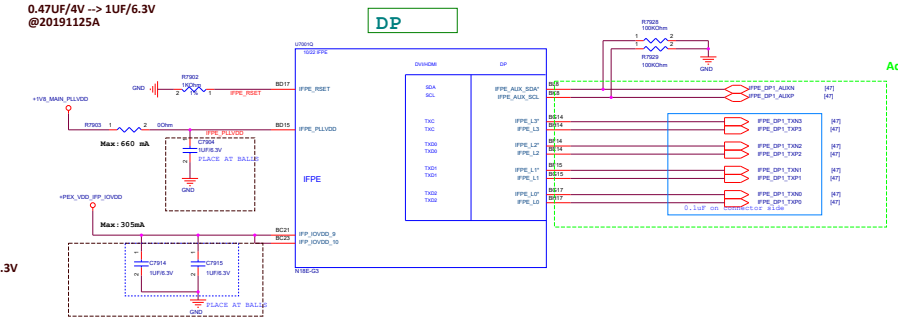


IFPD 要接eDP

0.47UF/4V --> 1UF/6.3V
@20191125A

DP

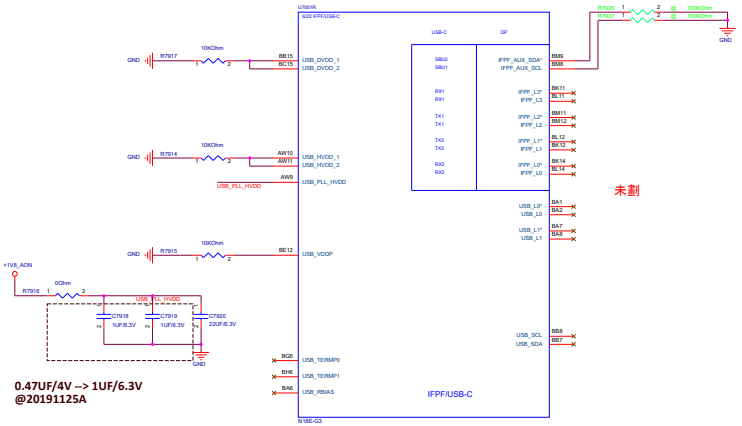
Add @20181108C



0.47UF/4V --> 1UF/6.3V
@20191125A

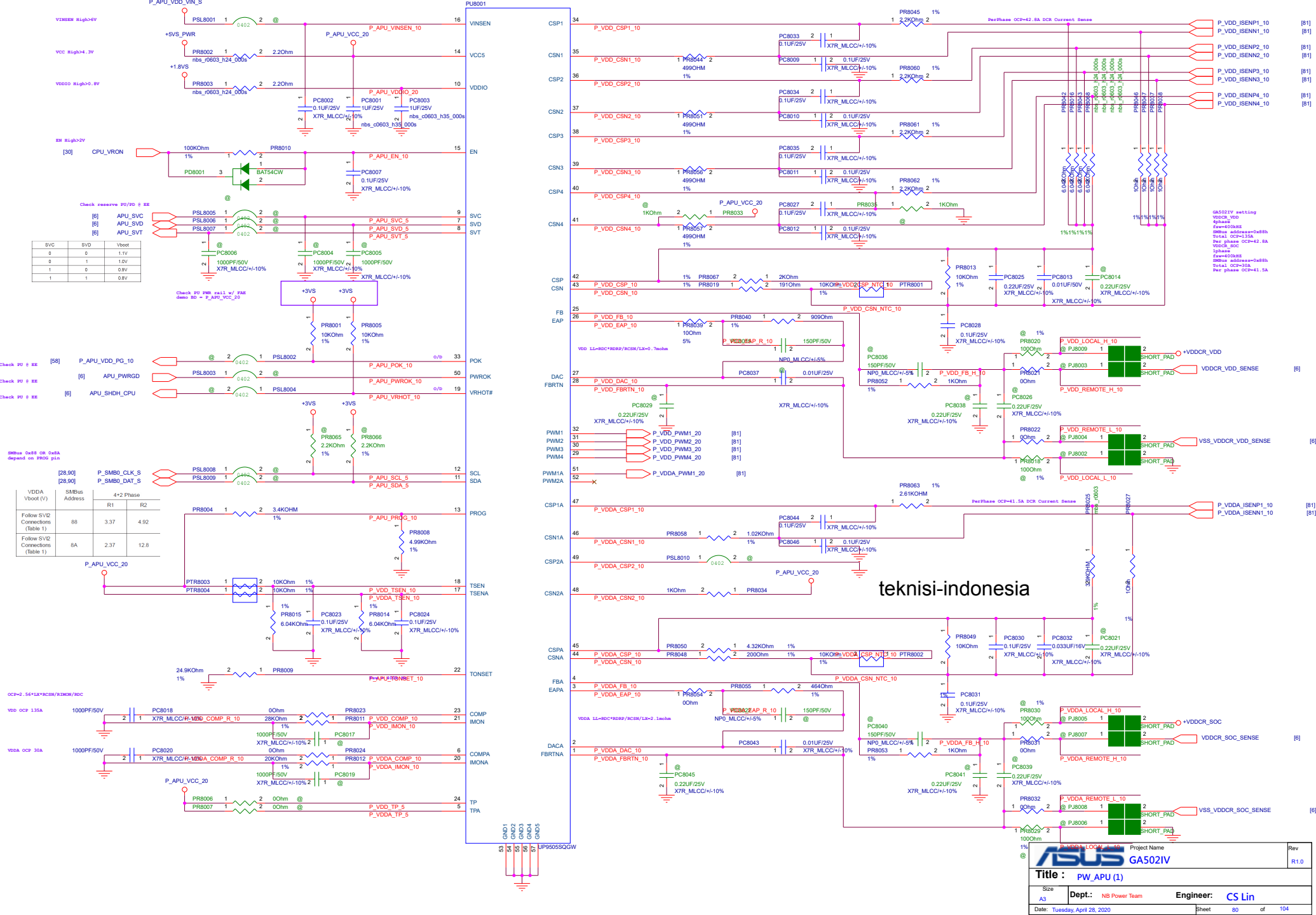
USB-C/DP (not used)

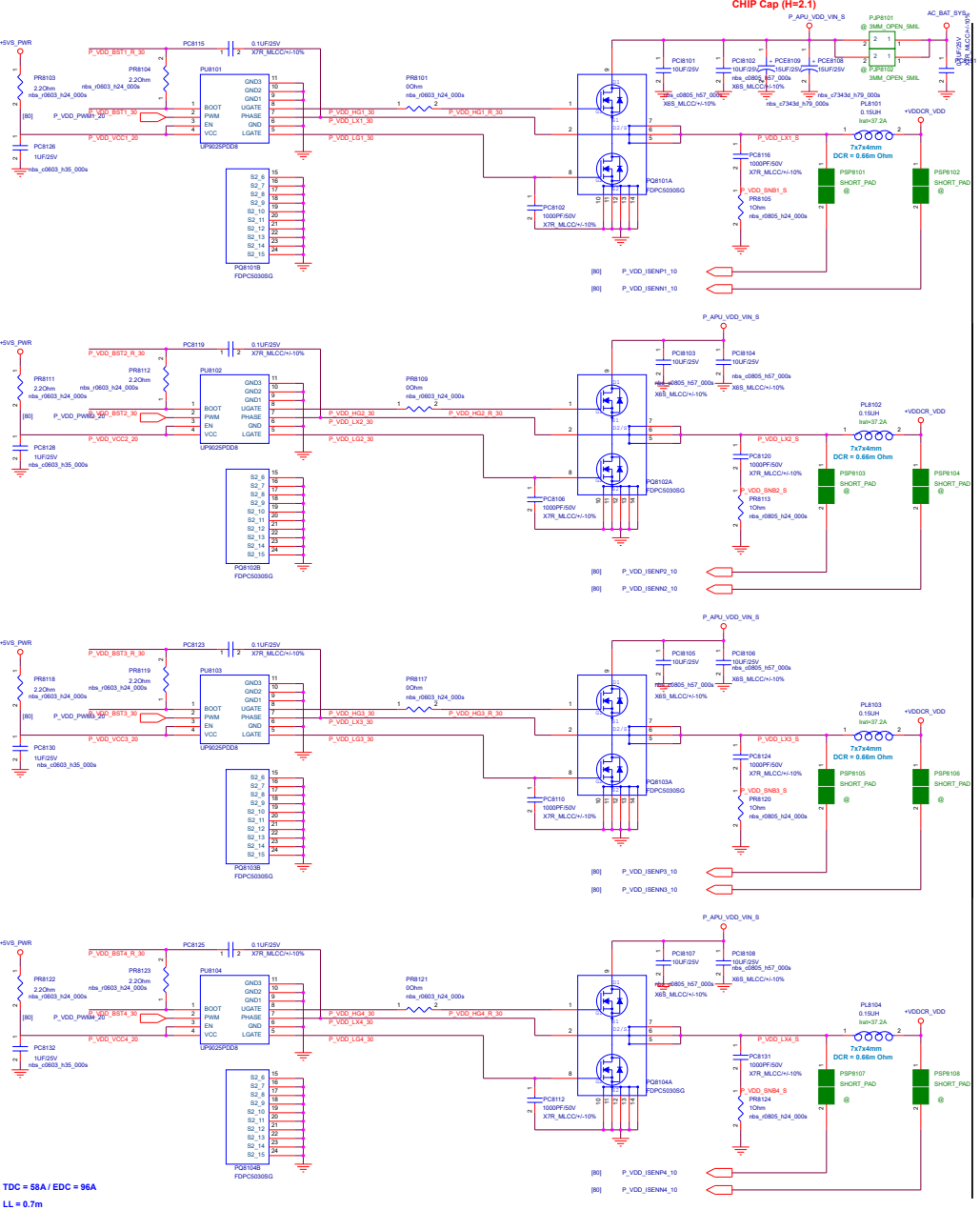
未劃



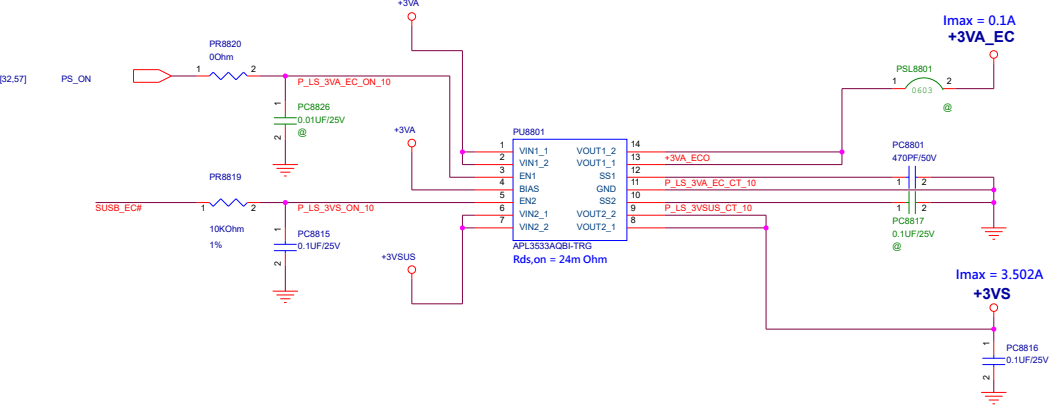
IFPF 要接USBC

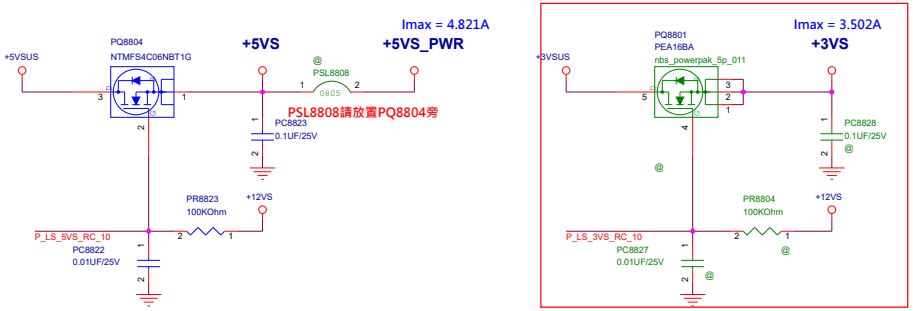
ASUS	Project Name: GX502GX		Rev: R1.3
Title : GPU_DP/EDP/HDMI/LVDS/CRT			
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: NB1 RD2 EE1	
Date: Tuesday, April 28, 2020	Sheet: 79 of 104		

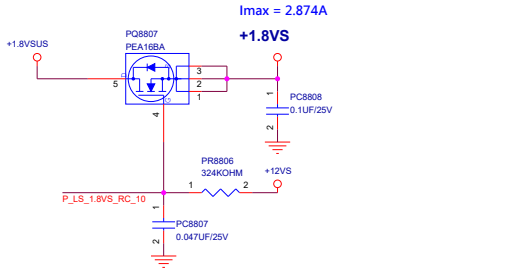

PU8001
UP9505SQGW
VINSEN
VCC5
VDDIO
EN
SVC
SVD
SVT
POK
PWROK
VRHOT#
SCL
SDA
PROG
TSEN
TSENA
TONSET
COMP
IMON
COMPA
IMONA
TP
TPA
CSP1
CSN1
CSP2
CSN2
CSP3
CSN3
CSP4
CSN4
CSP
CSN
FB
EAP
DAC
FBRTN
PWM1
PWM2
PWM3
PWM4
PWM1A
PWM2A
CSP1A
CSN1A
CSP2A
CSN2A
CSPA
CSNA
FBA
EAPA
DACA
FBRTNA
GND1
GND2
GND3
GND4
GND5
P_APU_VDD_VIN_S
P_APU_VINSEN_10
P_APU_VCC_20
P_APU_VDDIO_20
P_APU_EN_10
P_APU_SVC_5
P_APU_SVD_5
P_APU_SVT_5
P_APU_POK_10
P_APU_PWROK_10
P_APU_VRHOT_10
P_SMB0_CLK_S
P_SMB0_DAT_S
P_APU_SCL_5
P_APU_SDA_5
P_APU_PROG_10
P_VDD_TSEN_10
P_VDDA_TSEN_10
P_APU_TONSET_10
P_VDD_COMP_10
P_VDD_IMON_10
P_VDDA_COMP_10
P_VDDA_IMON_10
P_VDD_TP_5
P_VDDA_TP_5
P_VDD_CSP1_10
P_VDD_CSN1_10
P_VDD_CSP2_10
P_VDD_CSN2_10
P_VDD_CSP3_10
P_VDD_CSN3_10
P_VDD_CSP4_10
P_VDD_CSN4_10
P_VDD_CSP_10
P_VDD_CSN_10
P_VDD_CSN_NTC_10
P_VDD_FB_10
P_VDD_EAP_10
P_VDD_EAP_R_10
P_VDD_DAC_10
P_VDD_FBRTN_10
P_VDD_PWM1_20
P_VDD_PWM2_20
P_VDD_PWM3_20
P_VDD_PWM4_20
P_VDDA_PWM1_20
P_VDDA_CSP1_10
P_VDDA_CSN1_10
P_VDDA_CSP2_10
P_VDDA_CSN2_10
P_VDDA_CSP_10
P_VDDA_CSN_10
P_VDDA_CSN_NTC_10
P_VDDA_FB_10
P_VDDA_EAP_10
P_VDDA_EAP_R_10
P_VDDA_DAC_10
P_VDDA_FBRTN_10
P_VDD_FB_H_10
P_VDD_REMOTE_H_10
P_VDD_REMOTE_L_10
P_VDD_LOCAL_H_10
P_VDD_LOCAL_L_10
P_VDDA_FB_H_10
P_VDDA_REMOTE_H_10
P_VDDA_REMOTE_L_10
P_VDDA_LOCAL_H_10
P_VDDA_LOCAL_L_10
P_VDD_ISENP1_10
P_VDD_ISENN1_10
P_VDD_ISENP2_10
P_VDD_ISENN2_10
P_VDD_ISENP3_10
P_VDD_ISENN3_10
P_VDD_ISENP4_10
P_VDD_ISENN4_10
P_VDDA_ISENP1_10
P_VDDA_ISENN1_10
PerPhase OCP=42.8A DCR Current Sense
PerPhase OCP=41.5A DCR Current Sense
GA502IV setting
VDDCR_VDD
4phase
fsw=400kHz
SMBus address=0x88h
Total OCP=135A
Per phase OCP=42.8A
VDDCR_SOC
1phase
fsw=400kHz
SMBus address=0x86h
Total OCP=30A
Per phase OCP=41.5A
VDD LL=RDC*RDRP/RCSN/LX=0.7mohm
VDDA LL=RDC*RDRP/RCSN/LX=2.1mohm
OCP=2.56*LX*RCSN/RIMON/RDC
VDD OCP 135A
VDDA OCP 30A
SMBus 0x88 OR 0x8A depand on PROG pin
Check PU PWR rail w/ FAE demo RD = P_APU_VCC_20
Check PU @ EE
VINSEN High>6V
VCC High>4.3V
VDDIO High>0.8V
EN High>2V
SVC SVD Vboot
0 0 1.1V
0 1 1.0V
1 0 0.9V
1 1 0.8V
VDDA Vboot (V) | SMBus Address | 4+2 Phase R1 | 4+2 Phase R2
Follow SVI2 Connections (Table 1) | 88 | 3.37 | 4.92
Follow SVI2 Connections (Table 1) | 8A | 2.37 | 12.8
teknisi-indonesia
Project Name GA502IV
Rev R1.0
Title : PW_APU (1)
Size A3
Dept.: NB Power Team
Engineer: CS Lin
Date: Tuesday, April 28, 2020
Sheet 80 of 104

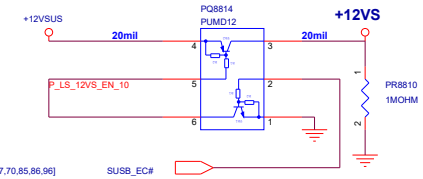


Project Name: GA502IV			Rev: R1.0
Title: PW_APU (1)			
Size: A2	Dept.: NB Power Team	Engineer: CS Lin	
Date: Tuesday, April 28, 2020	Sheet: 81	of: 104	



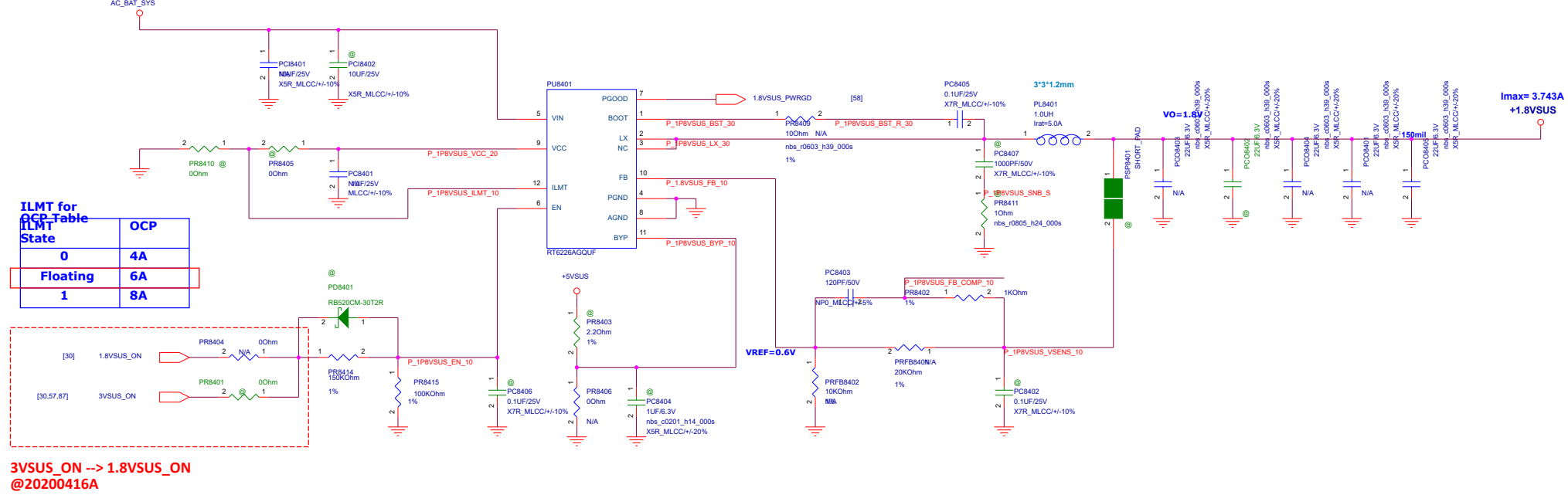






ASUS	Project Name: GA502IV		Rev: R1.0
Title : PW_LOAD SWITCH			
Size: A3	Dept.: NB Power team	Engineer: CS Lin	
Date: Tuesday, April 28, 2020	Sheet 88 of 104		

Title <Title>		
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, April 28, 2020	Sheet 82 of 104	



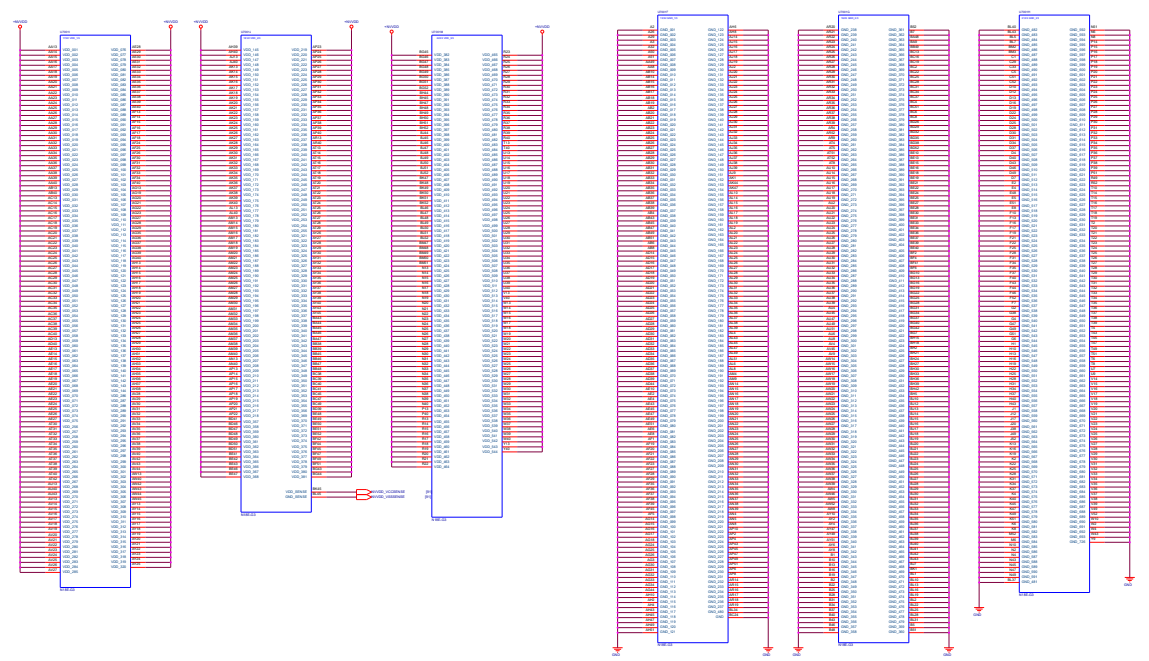
3VSUS_ON --> 1.8VSUS_ON
@20200416A

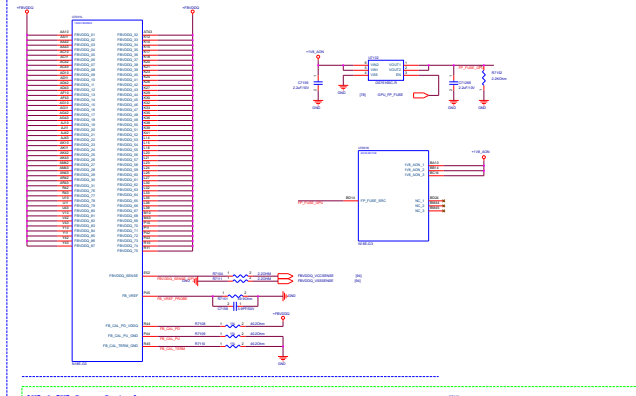
PT840* 請放置 PU8401旁;並請放置Trace 上!

<Variant Name>

Project Name: GA502IV		Rev: R1.0
Title : PW_+1.8VSUS		
Size: A3	Dept.: NB Power team	Engineer: CS Lin
Date: Tuesday, April 28, 2020	Sheet 84 of 104	

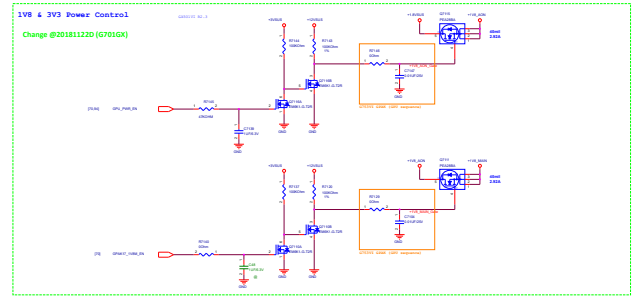
Main Board



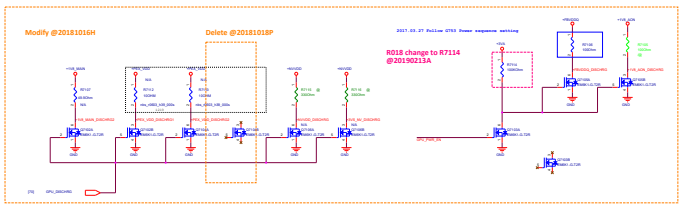


1V8 & 3V3 Power Control

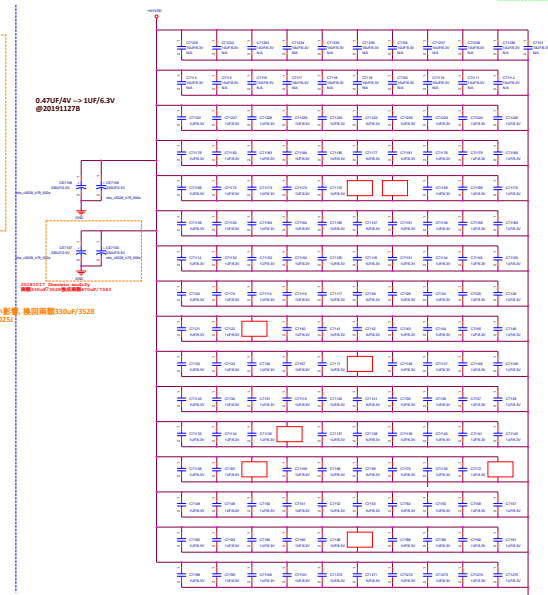
Change @20181122D (G701GX)



Discharge Discharge

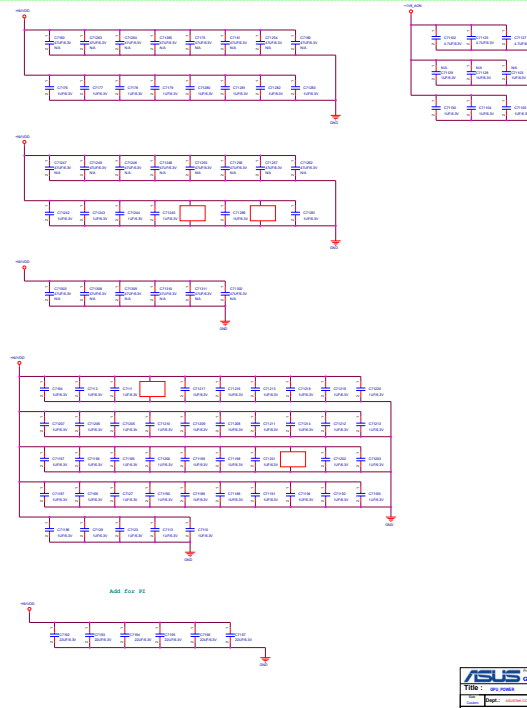


0.47UF/4V --> 1UF/6.3V
@20191127B



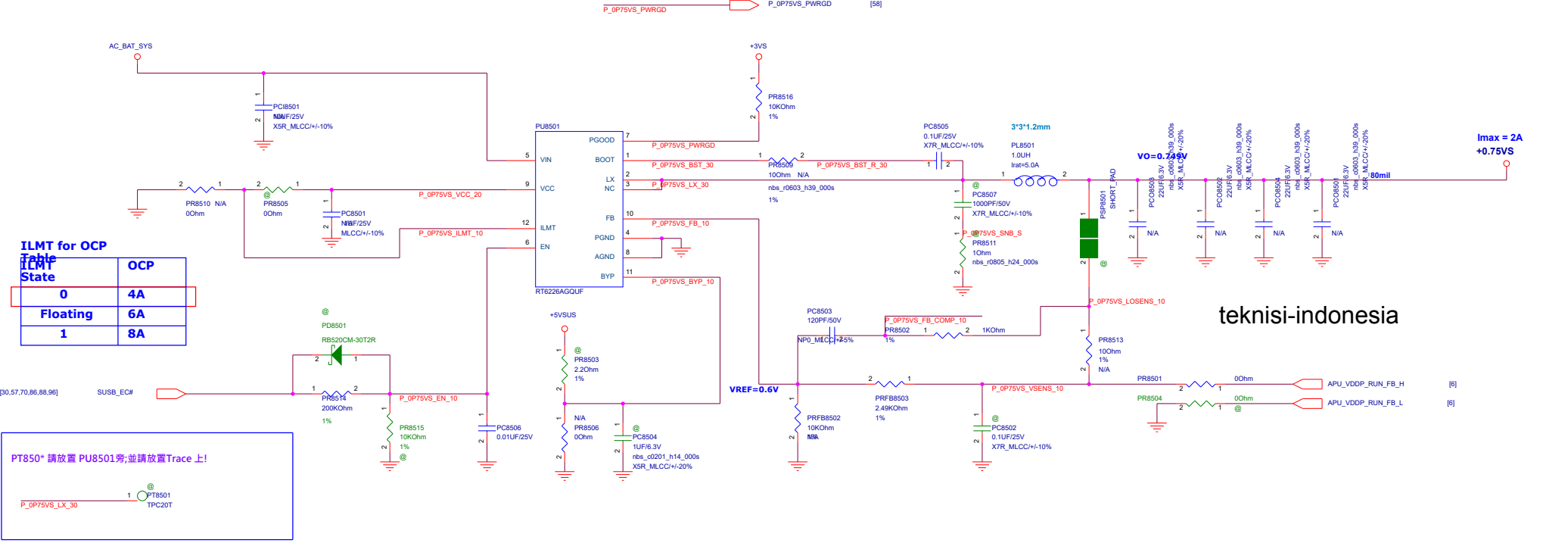
20181017 Discharge modify
兼容330uF/3528換成兼容470uF/7343

元件大小影響, 換回兩顆330uF/3528
@20181025I



Add for PI

ASUS	Project Name: GX701		Rev: 1.0
Title : GPU POWER			
Size: Custom	Dept.:	Engineer: Ashton_yang	
Date: Tuesday, April 09, 2019		Sheet: 71 of 100	



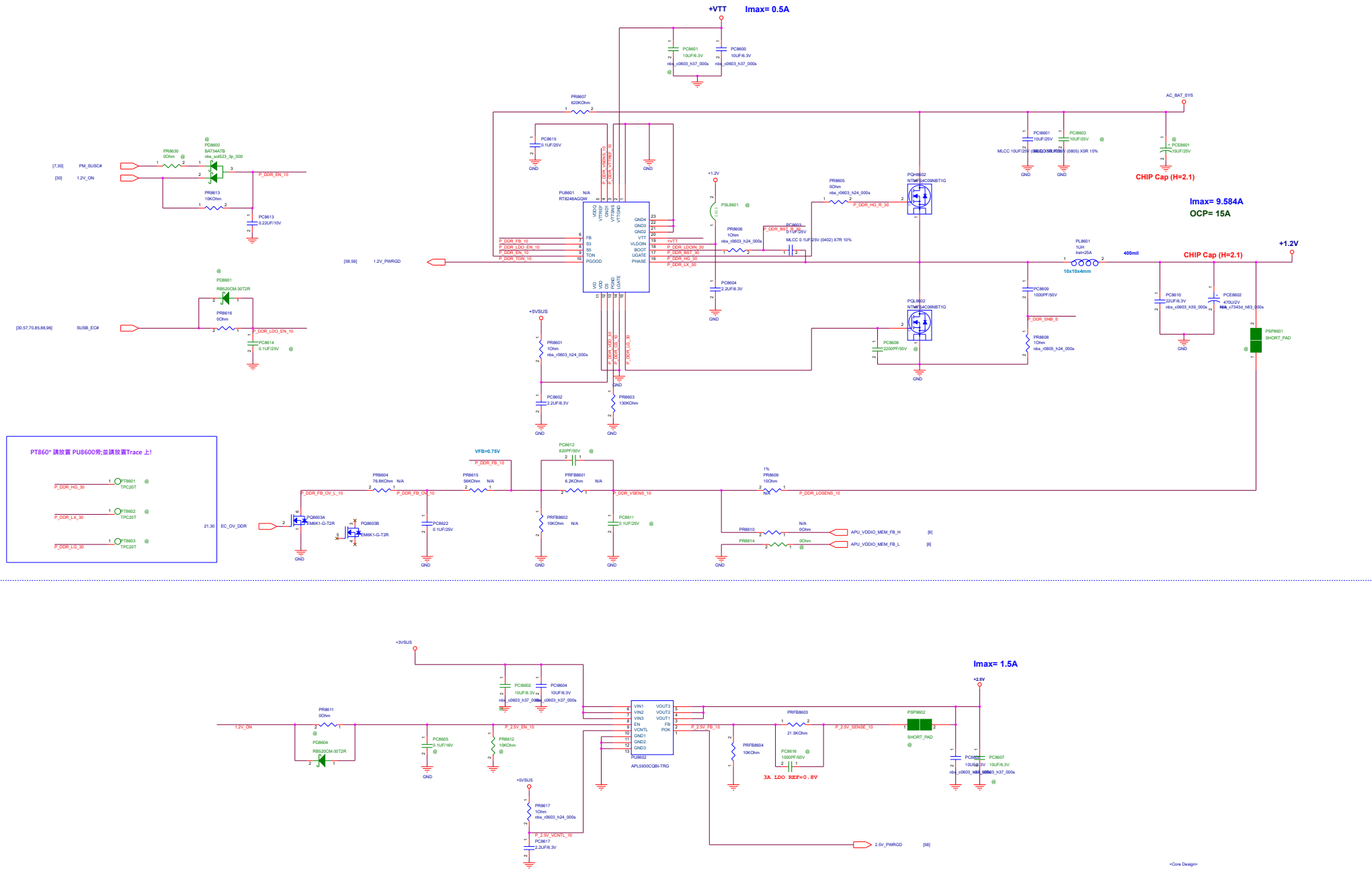
ILMT for OCP Table

ILMT State	OCP
0	4A
Floating	6A
1	8A

<Variant Name>

Project Name: GA502IV		Rev: R1.0
Title : PW_+0.75VS		
Size: A3	Dept.: NB Power team	Engineer: CS Lin
Date: Tuesday, April 28, 2020	Sheet 85 of 104	

+1.2V / +VTT / +2.5V[For Memory]

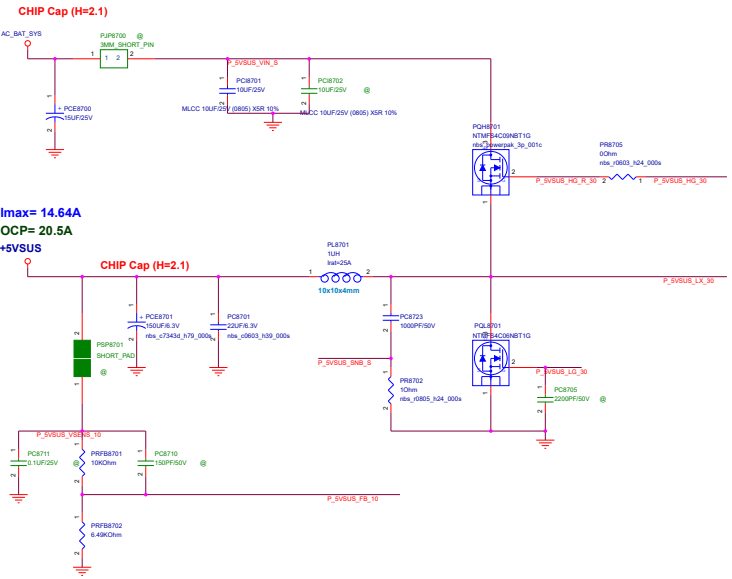


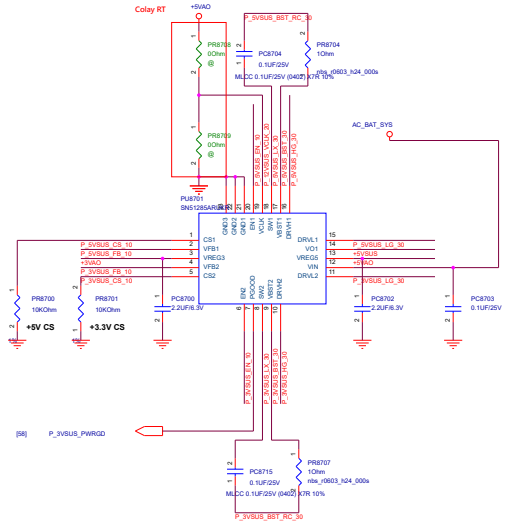
<Core Design>

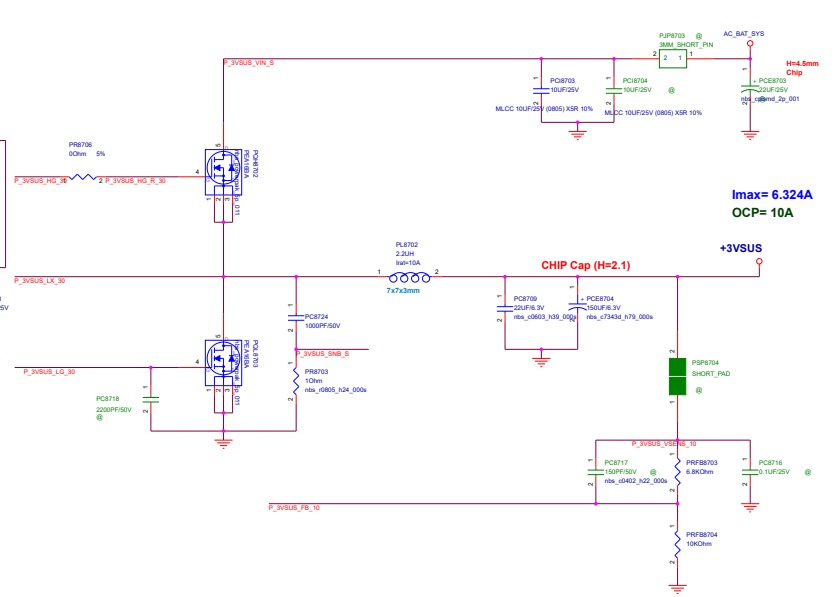
ASUS	Project Name: GA502IV		Rev: R1.0
Title : PW_+1.2V/+VTT/+2.5V			
Size: A2	Dept.: NB Power team	Engineer: HON	
Date: Tuesday, April 28, 2020	Sheet: 86	of: 104	

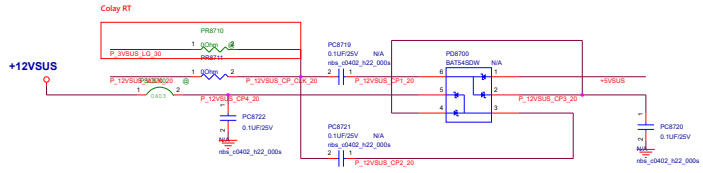
Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, April 28, 2020	Sheet 95 of 104	

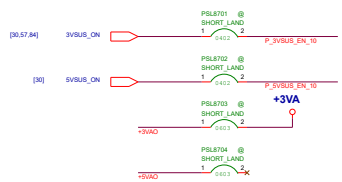
+3VSUS / +5VSUS [System Power]











請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm

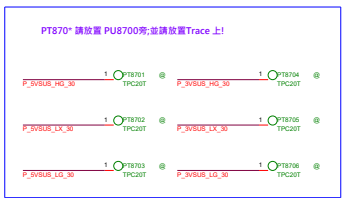
Adaptor Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0

PT870* 請放置 PU8700旁;並請放置Trace 上!



<variant_name>

ASUS	Project Name: GA502IV		Rev: R1.0
Title : PW_+3VA_DSW/+5VSUS			
Size: A2	Dept.: NB Power team	Engineer: CS Lin	
Date: Tuesday, April 28, 2020	Sheet: 87	of: 104	

EE PART

GM531GX R1.0 SKU Table

			CPU	Power	DIMM	VRAM			
Option	PCB	SKU							

Title :	GM531GX SKU Table_R1.0		
Engineer:	EE		
Size	Project Name		Rev
C	GX502GX		1.0
Date: Tuesday, April 09, 2019	Sheet	103	of 104

9. Card Reader: AU6435--02G630002400 (Page42)

10. USB Charger IC: (Page52) Silego SLG55584AVTR -- 06016-00040000
MAXIM MAX14566AEETA+ -- 06G016196011

11. USB3.0 Repeater IC:(Page67)
Parade : PS8710B -- 06053-00200000
Maxim : MAX14972CTG+ -- 06053-00030000

13. Audio Codec : 02043-00130000 (663-VA4)

Main Board

PRS8901	ADP<120W	ADP<=230W	ADP>230W	ADP>330W
	TBD	5m	5m	2m
	TBD	10125-00068100	10126-00068000	10126-00068000

PRS8903	ADP=120W	ADP=150W	ADP=180W	ADP=230W	ADP=280W	ADP=330W
	200m	255m	X	X	X	560m
	10114-00188000	10114-00221000	X	X	X	10114-00311000

AC_BAT_SYS

AD : 17.8V

BAT

3 limit : Charge 4A
DisCharge 16A

AC limit = 100% ADP
Bat limit = byte 7 x 1.7

dGPU_PD# ---> GPIO12(EE page 75 or 78)

AD : 17.5V
Place Close to PU8901

PT8904請放置於DC JACK 旁邊

PT890* 請放置 PU8900先並請放置Trace 上!

Adaptor select
total power = 90% ADP

Adaptor select			
		8/7X Series	6 Series
PRS8901		10m	5m
PR8936			
14K	0.4V	30W	120W
31.6K	0.8V	40W	150W
56K	1.2V	45W	180W
93.1K	1.6V	65W	230W
150K	2.0V	75W	300W
270K	2.4V	90W	330W
560K	2.8V	120W	400W

POP window

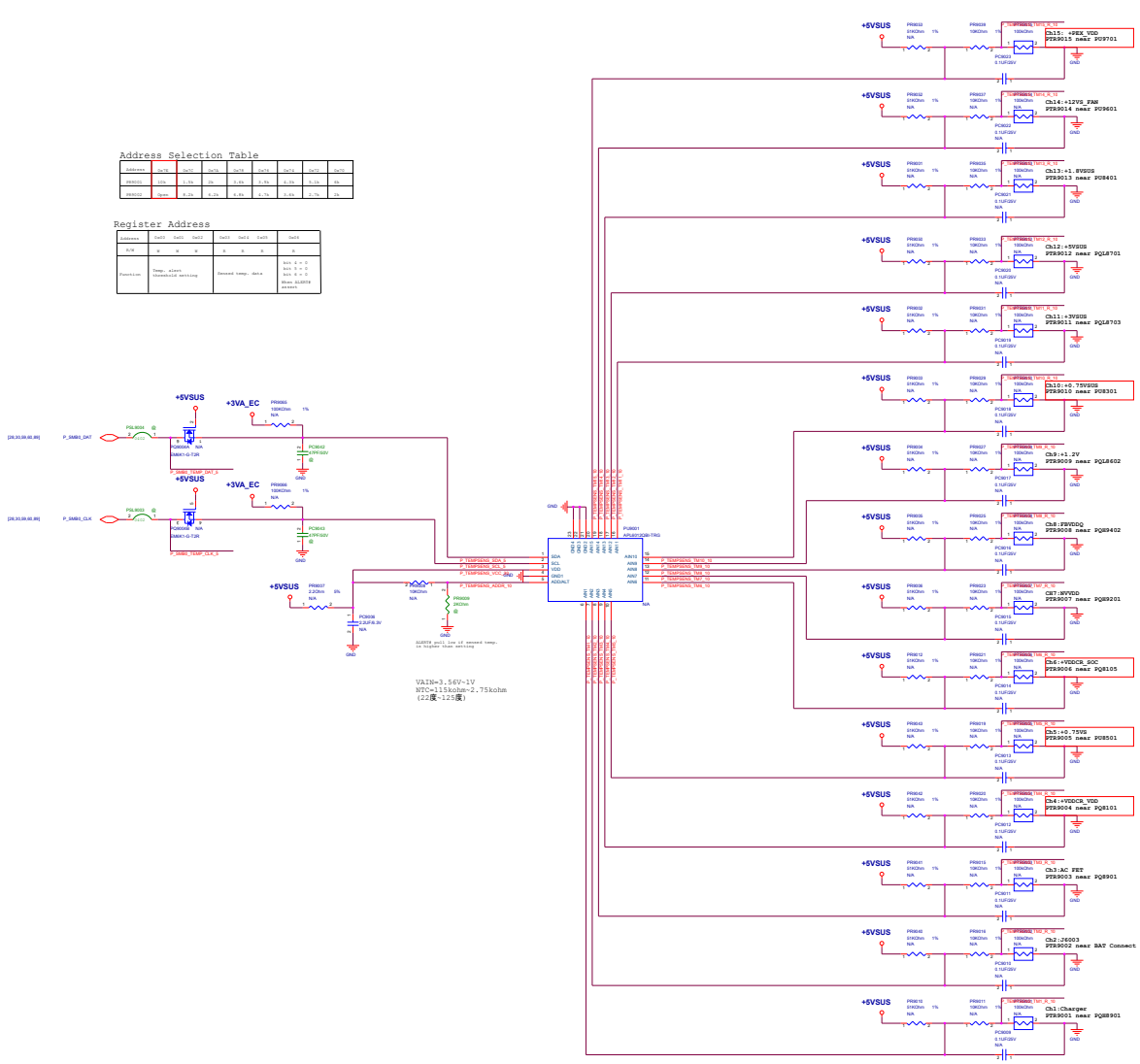
Project Name	Coffee lake-H
Title	PW_CHARGER
Dept.	MB Power Team
Engineer	Benson
Date	Tuesday, April 28, 2020

Address Selection Table

Address	0x78	0x7C	0x7A	0x7E	0x7B	0x7D	0x79	0x7F
R9002	10k	1.1k	2k	4.4k	5.5k	6.8k	9.1k	8k
R9001	Open	8.2k	3.2k	4.8k	5.7k	7.2k	2.7k	2k

Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x20
R/W	R	W	W	R	R	R	R
Function		Temp. alert threshold setting		Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# asserts



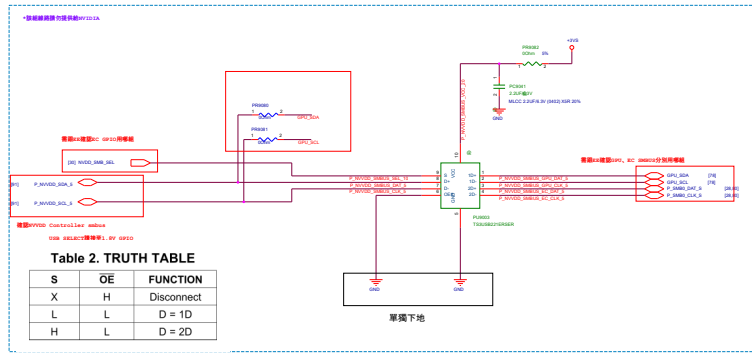
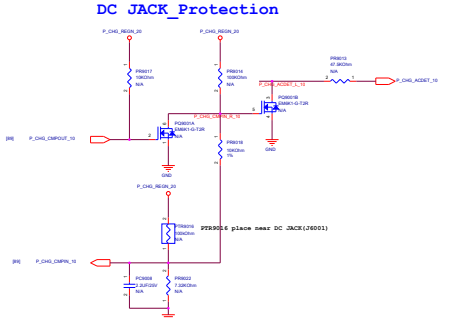


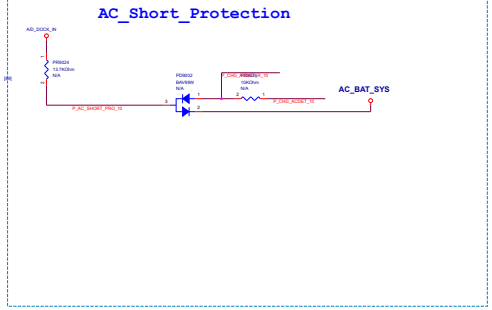
Table 2. TRUTH TABLE

S	$\overline{OE}$	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

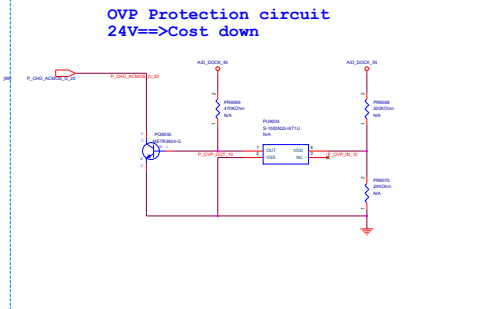
DC JACK_Protection



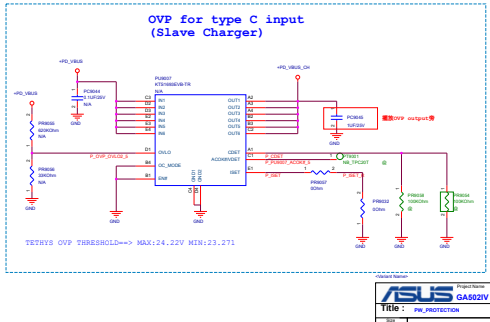
AC_Short_Protection



OVP Protection circuit 24V==>Cost down



OVP for type C input (Slave Charger)



ASUS	Project Name: GA502IV		Rev: 0.2
Title :	PW_PROTECTION		
Size: A1	Dept.: NB Power Team	Engineer: CS Lin	
Date: Tuesday, April 28, 2020	Sheet 90 of 104		

FBVDDQ
VRAM side

FBVDDQ
GPU side

Channel A

Close to DRAM
0.47uF x 3pcs
10nF x 2pcs

Around DRAM
22nF x 6pcs
10nF x 2pcs

C77851 10uF ->47uF
@2019102A

0.47uF/6V -> 1UF/6.3V
@2019111T6

0.47uF x 4pcs
4.7nF x 1pcs

0.47uF/6V -> 1UF/6.3V
@2019111T6

Close to DRAM
0.47uF x 3pcs
10nF x 2pcs

Around DRAM
22nF x 6pcs
10nF x 2pcs

Close to DRAM
0.47uF x 4pcs
4.7nF x 1pcs

VRAM PWR_FBVDDQ

0.47UF/6V -> 1UF/6.3V
@2019111T6

Restriction A
under GPU

Restriction B
under GPU

Restriction C
under GPU

Restriction D
under GPU

Close GPU

Close GPU

0.47uF x 12pcs
10nF x 2pcs

0.47uF x 12pcs
10nF x 2pcs

0.47uF x 12pcs
10nF x 2pcs

10nF x 7pcs
22nF x 6pcs

Add for P2

Near C78501

Channel B

Close to DRAM
0.47nF x 3pcs
10nF x 2pcs

Around DRAM
22nF x 6pcs
10nF x 2pcs

Close to DRAM
0.47uF x 4pcs
4.7nF x 1pcs

Close to DRAM
0.47nF x 3pcs
10nF x 2pcs

Around DRAM
22nF x 6pcs
10nF x 2pcs

Close to DRAM
0.47uF x 4pcs
4.7nF x 1pcs

For power sequence measurement

GRAM VRP power v1.0U

Remove @2019051118

VRAM Thermal Sensor

Delete VRAM Channel D CAP
(2019062A

Channel C

Close to DRAM
0.47nF x 3pcs
10nF x 2pcs

Around DRAM
22nF x 6pcs
10nF x 2pcs

Close to DRAM
0.47uF x 4pcs
4.7nF x 1pcs

Close to DRAM
0.47nF x 3pcs
10nF x 2pcs

Around DRAM
22nF x 6pcs
10nF x 2pcs

Close to DRAM
0.47uF x 4pcs
4.7nF x 1pcs

Delete R7711 R7712 R7713
(2019071A

Channel D

Close to DRAM
0.47nF x 3pcs
10nF x 2pcs

Around DRAM
22nF x 6pcs
10nF x 2pcs

Close to DRAM
0.47uF x 4pcs
4.7nF x 1pcs

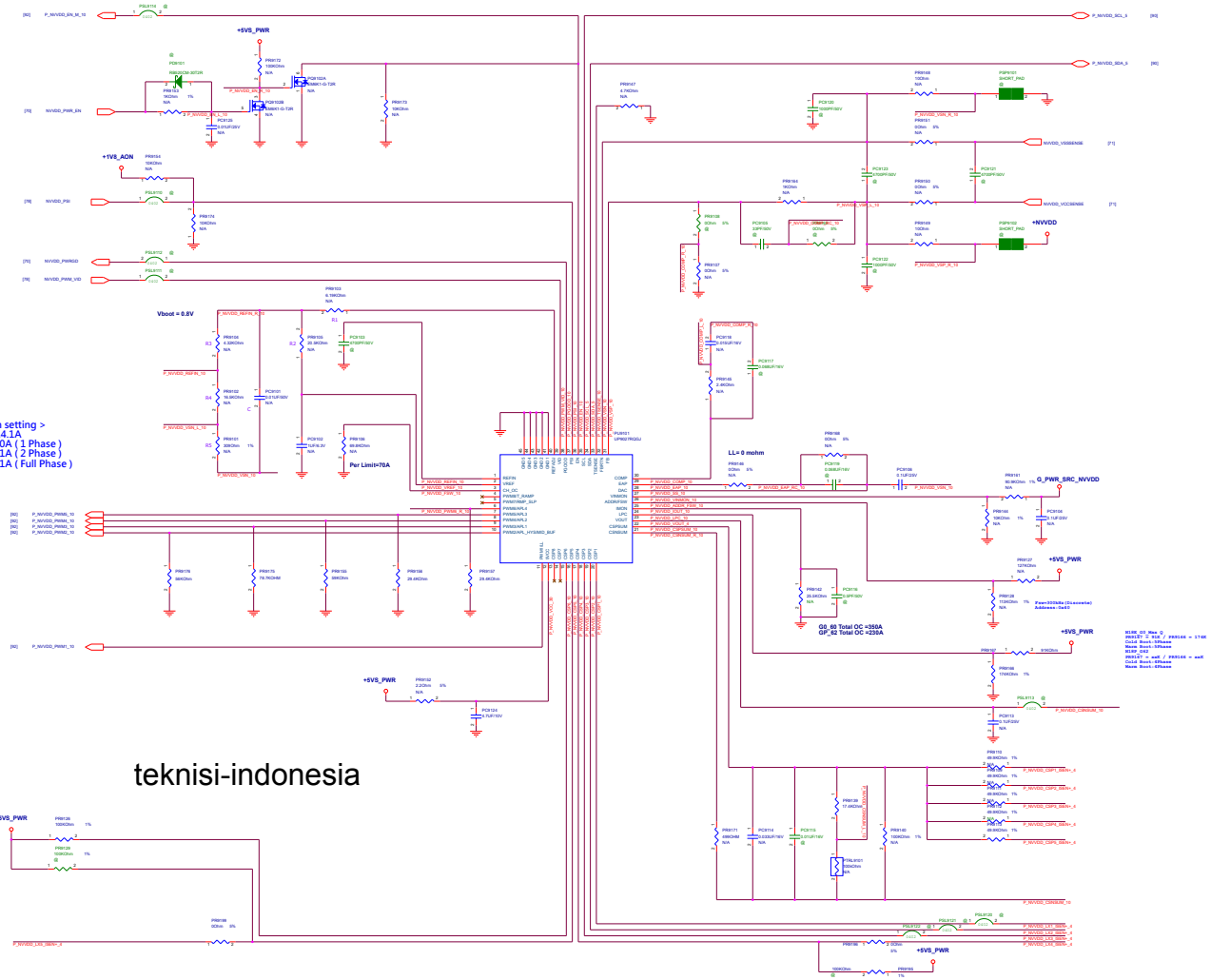
Close to DRAM
0.47nF x 3pcs
10nF x 2pcs

Around DRAM
22nF x 6pcs
10nF x 2pcs

Close to DRAM
0.47uF x 4pcs
4.7nF x 1pcs

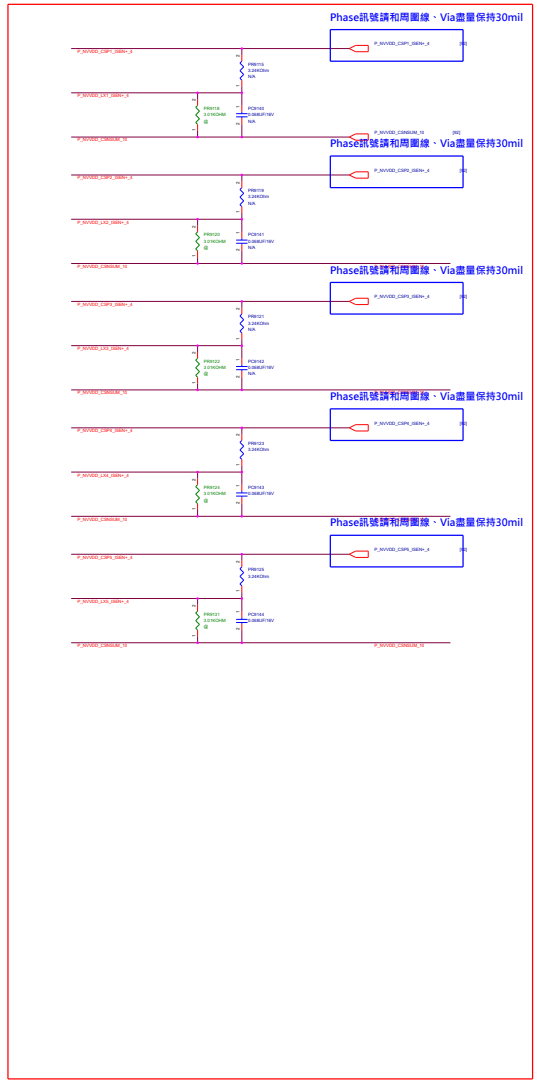
C77268
C77224
C77225
C77267
C77619
C77125
C77126
C77682
C77681
C71595
C77751
C71252
C71253
C77288
C75562
C77254
C77255
C77256
C77257
C77258
C77259
C77225
C77263
C77262
0603CG82
@2019051A

+NVVDD [For DGPU]



< HW Strap Function setting >
PWM2 : APL_Hys = 14.1A
PWM3 : VAPL1 = 17.0A (1 Phase)
PWM4 : VAPL2 = 34.1A (2 Phase)
PWM5 : VAPL3 = 34.1A (Full Phase)

請放靠近PU9101



Title :	PW_+NVVDD (1)	Project Name: GA502IV	Rev: R3.0
Size: A3	Dept.: NB Power Team	Engineer: CD Lin	
Date: Tuesday, April 28, 2020	Sheet: 81 of 104		

1016_移除Discrete mode切換電路

1016_移除MS-Hybrid切換元件

VGA INT. Thermal sensor address 0x9E and 0x9C

0.47UF/4V ~> 1UF/6.3V
@20191125A

X7801: 27MHZ +/-15ppm/10pF (3225)
1st: P/N:6T0S91026270I TXC/7V27000050
2nd: P/N:6T0S91052701 HOSONIC/E3FB27.0000F10E11

R7834,R7819 unmount
Please Add VG BOM
@20191128A

STRAP PIN

R7819 /VRAM --> /VR
@20190904A

If VRAM Micron R7819上件
@20190201A

R7850 change to unmount
@20181129A

1016_移除Discrete mode切換元件

If VRAM Samsung R7834 上件
@20190201A

R7840 change to mount
@20181129A

1016_移除Discrete mode切換電路

Thermal Protection

Remove R7814 & R7818 @20190606B

Add R7814 10K @20190606B

Remove @20181016F

VGA EXT. Thermal Sensor

Add DP HPD @20181108B

Change IFPE_DP_HPD to HPD_IFPE
@20181108B

GPU GPIO INPUT

1016_移除HPD_IFPx開關電路

For GC off MS hybrid

Delete Q7804 R7866 R7865 R7849
Delete HPD_IFPC_GPU#, IFPC_HDMI_HPD, HDMI_HDP_EN_dGPU#
@20190716C

For EMI

R7500 mount
@20181108B

1016_移除跳冥

Change HPD_IFPE to HPD_IFPC_GPU#
@20181112A

PGC6 STATE FOR NV3R PANEL
GPIO 未CHECK

Physical Configuration		
Level Option	Pull-Up to 1.8V via resistor (see Note 3) (Notebook designs also see Note 2.)	Pull-Down to GND via resistor [Note 1]
1.8V ("HIGH") Level	Populate	Do Not Populate
0.9V ("MIDDLE") Level	Populate	Populate
GND ("LOW") Level	No Stuff	Populate

Note 1: Resistor should be 10K Ohms. 5% tolerance is acceptable.
Note 2: Notebook graphics circuit designs should pull down the 1V8_SOR signal rather than to 3V3_MAIN.

Strap Pins see Note			FL_OVERT Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FL_OVERT function ENABLED
L	L	H	FL_OVERT Function DISABLED (Default, do not configure)
all other configurations			RSVRVD, do not configure)

Strap Pins see Note	RAMCFG Setting Number (see memory RVL for memory configs corresponding to these numbers)	
STRAP2	STRAP1	STRAP0	
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
R	L	R	8 (0x0008)
L	R	L	9 (0x0009)
L	R	R	10 (0x000A)
L	R	H	11 (0x000B)
R	L	L	12 (0x000C)
R	L	R	13 (0x000D)
R	L	H	14 (0x000E)
R	H	L	15 (0x000F)
R	H	R	16 (0x0010)
R	H	H	17 (0x0011)
H	R	L	18 (0x0012)
H	R	R	19 (0x0013)
H	R	H	20 (0x0014)
R	R	R	21 (0x0015)
R	R	L	22 (0x0016)
R	R	H	23 (0x0017)
R	H	R	24 (0x0018)
R	H	H	25 (0x0019)
R	R	R	26 (0x001A)

Strap Pins Note 1						Functions Selected by This Strapping
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	FORC_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	R	0	0	1	1
L	H	L	0	1	0	0
L	H	R	0	1	1	1
H	L	L	1	0	0	0
H	L	R	1	0	1	1
H	H	L	1	1	0	0
H	H	R	1	1	1	1

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REMAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

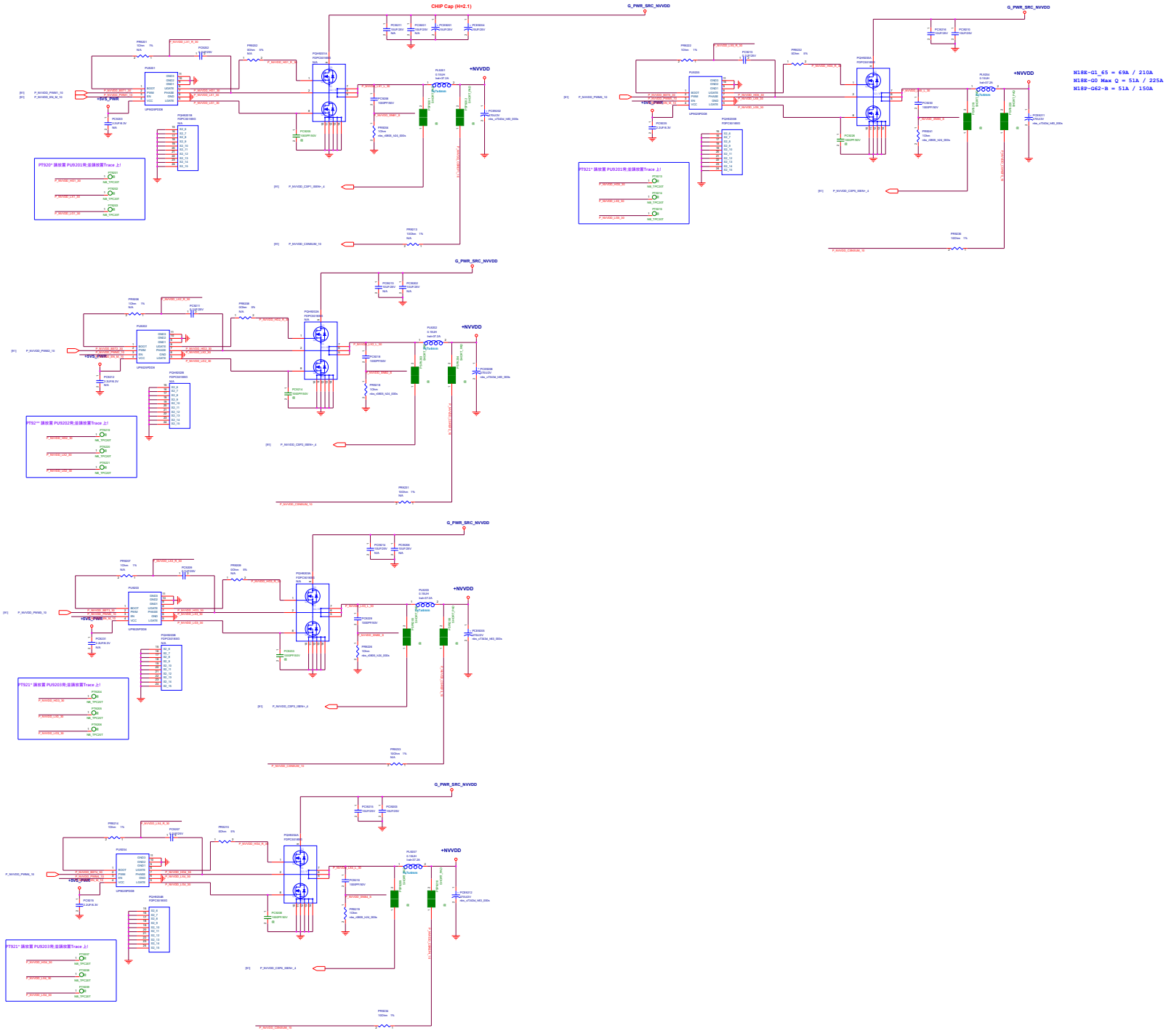
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

DEFULT : L L H

Assorted Configuration Straps:
1. SMB_ALT_ADDR Enable: "H" signal (SMB settings 0/1 address mode); "L" Disable (SMB settings 0/1 address mode); "R" must be strapped to GND, could also be accessed 10%
2. DEVID_SEL: G-sync function – "0" normal GPU ID, "1" support G-sync GPU ID.
3. PCIE_CFG: PCIE Swing –"0" PCIE Swing default, "1" PCIE swing reduce.
4. VGA_DEVICE: Graphics circuit – "0"/ MS-Hybrid, "1" Discrete.

Project Name		Rev
ASUS	GX502GX	20.3
Title :	GPU CLOCK&STRAP&IFPD	
Size:	Dept.: ASUSTeK COMPUTER INC Engineer:	NB1 RD2 EE1
Date: Tuesday, April 28, 2020	Sheet 19 of 58	

+NVVDD [For DGPU]



+FBVDDQ [For VRAM]

BOM Option for EE:
N18E-G1_65 = PR9409 (stuff) = fix 1.2V
N18E-G0 Max Q = PR9499 (stuff) = fix 1.25V
N18P-G62-B = PR9499 (stuff) = fix 1.25V

DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.35V	1.25V
PR9404	10KOhm	
PR9409	21.5KOhm	
PR9423	75KOhm	

DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.35V	1.2V
PR9404	10KOhm	
PR9409	21.5KOhm	
PR9423	53.6KOhm	

DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.25V	1.2V
PR9404	10KOhm	
PR9409	16.9KOhm	
PR9423	140KOhm	

Fixed Vout		
@	PC9403/PR9423/PQ9401 PR9402/PR9414	
Voltage	1.25V	1.2V
PR9404	10KOhm	
PR9409	16.9KOhm	15.4KOhm

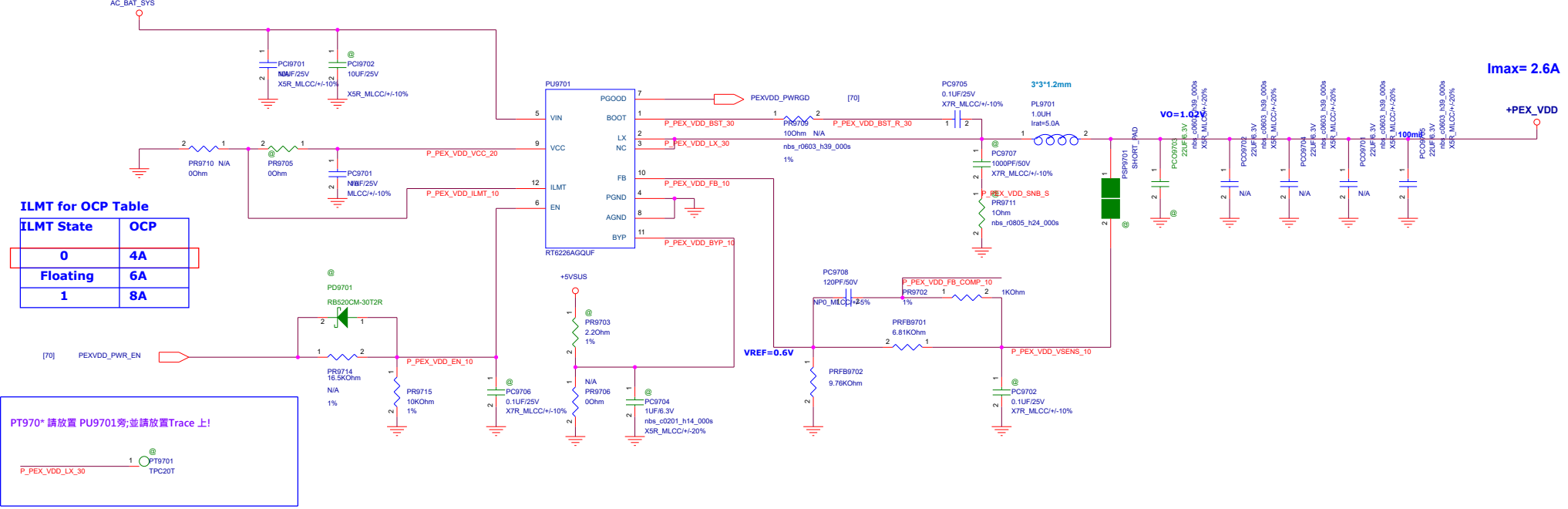
N18E-G1_65 = 1.2V
N18E-G0 Max Q = 1.25
N18P-G62 = 1.25V

CHIP Cap (H=2.1)

N18E-G1_65 = 21A / 24A
N18E-G0 Max Q = 27A / 32A
N18P-G62-B = 18A / 19A
OCP= 50A

PT940* 請放置 PU9401旁;並請放置Trace 上!

Project Name	GA502IV	Rev	R1.0
Title :	PW_+FBVDDQ		
Size	Custom	Dept.:	NB Power Team
Engineer:	CS Lin		
Date:	Tuesday, April 28, 2020	Sheet	94 of 104



<Variant Name>

ASUS	Project Name: GA502IV	Rev: R1.0
Title : PW_+PEX_VDD		
Size: A3	Dept.: NB Power team	Engineer: CS Lin
Date: Tuesday, April 28, 2020	Sheet 97 of 104	

1. P.01-30 reference FX505DY, P.31-104 reference GX502_(WW39_20180927C)
2. Net connection_(WW39_20180928A)
20181004
P.03
P.07
P.30 Copy FX505DY P.30
P.32 Modify Reset circuit
P.34 Modify LAN connector
P.35 Modify M-KEY IT8291E to IT8299E
P.36 修路
P.37 Modiffy Headpohne, Mic, ESS
P.39 Remove Mute control
P.40 Modify circuit
P.41 Modify circuit & 修孔, 0 ohm short keep
P.45 Add Mic and HDR circuit
P.48 Keep SL4802
P.49 Modify circuit
P.50

ASUSTeK COMPUTER	Title : GB5202_SKU Table_R1.0		
	Engineer: EE		
Size: C	Project Name: GX502GX		Rev: 1.0
Date: Tuesday, April 09, 2019	Sheet 103 of 104		

9. Card Reader: AU6435--02G630002400 (Page42)

10. USB Charger IC: (Page52) Silego SLG55584AVTR -- 06016-00040000
MAXIM MAX14566AEETA+ -- 06G016196011

11. USB3.0 Repeater IC:(Page67)
Parade : PS8710B -- 06053-00200000
Maxim : MAX14972CTG+ -- 06053-00030000

13. Audio Codec : 02043-00130000 (663-VA4)

Rev	Date	Description
1.0	2017.03.03	P21 Remove CN
	2017.03.04	Q5602, Q5601 change for DXF Limitation
	2017.03.10	+1V9_MAIN, +3VS_NV Follow G753 Power sequence setting
	2017.03.11	R7821 Follow GL702 GPU Power seq
	2017.03.11	+PEX_VDD GPU Sequence update
	2017.03.14	PCE8104, PCE8107, PCE8106 update Cap for DXF Limit
	2017.03.14	GX501VIK Remove useless nut in P67
	2017.03.15	J5301 Connector list update
	2017.03.15	H6716, H6706, H6724, H6723 Screw Hole update
	2017.03.16	J5602 change LID SW for Angle Simulation
	2017.03.17	EMI Reserve C5606, C5607 Cap
	2017.03.17	RM3002, L4512, L4513, L4504, L4515, L4505 SWAP for Layout
1.1	2017.03.21	P30, P37, P39 AMP Change SNL04M25555
	2017.03.21	EMI Reserve P30 C77360 Cap and P69 Caps and Spring
	2017.03.23	AMP Change Remove P37 MUTE CONTROL schematic
	2017.03.23	AMP Change Reserve Q3701
	2017.03.27	P71 +PBVDDQ Discharge setting Follow G753 Power sequence setting
	2017.03.29	P12 Remove TBT Power Low Switch for Layout
1.2	2017.03.30	Change Cap C7105, C7101 for thermal request
	2017.03.30	Thermal Request for H6728
	2017.04.05	EMI Reserve Cap and Spring in P69
	2017.04.06	Reserve C2601 for +VCCPGPP_EF Ripple
	2017.04.07	25.00MHz Cap C1126, C1124 change for Vendor Suggest
	2017.04.07	27MHz Cap C7811, C7801 change for Vendor Suggest
2.0	2017.04.11	P48 Reserve 0 ohm for SDA and SCL
	2017.04.17	P71 Add Caps for NVVDD Ripple
	2017.04.18	Q5704 Chnage MOS for DXF Limitation
	2017.04.20	P71 Add Caps for NVVDD Ripple
	2017.04.21	P67 Screw Hole H6705 update
	2017.04.21	P71 Add Caps for NVVDD Ripple C71119~C71122
	2017.04.25	P71 C7122, C7123, C7127, C7135, C7143, C7144, C7156, C7164, C7166,, C7186, C7187 change to 10UF
	2017.04.25	P70 C7007, C7002 change to 4.7UF
	2017.04.25	P70 C7020, C7024 change to 22UF
	2017.05.02	EMI Reserve C6948, C6949, C6950, C6951, C6952, C6953, C6954 and remove U6913
	2017.05.02	H6711, H6712 change screw hole type fot EMI Solution
	2017.05.03	Remove J4502 Pin 36 GND fot Factory Issue
	2017.05.05	P88, P58 Remove VCCST_PWRGD signal
	2017.05.05	P79, P45 Remove eDP Lan2 and Lan3 Signal
	2017.08.10	P31 R3121,R3122 change to unmount

Rev	Date	Description

Rev	Date	Description

Rev	Date	Description

ASUSTeK COMPUTER INC.

Title : Revision History

Engineer: EE

Size: D | Project Name: GX502GX | Rev: 1.0

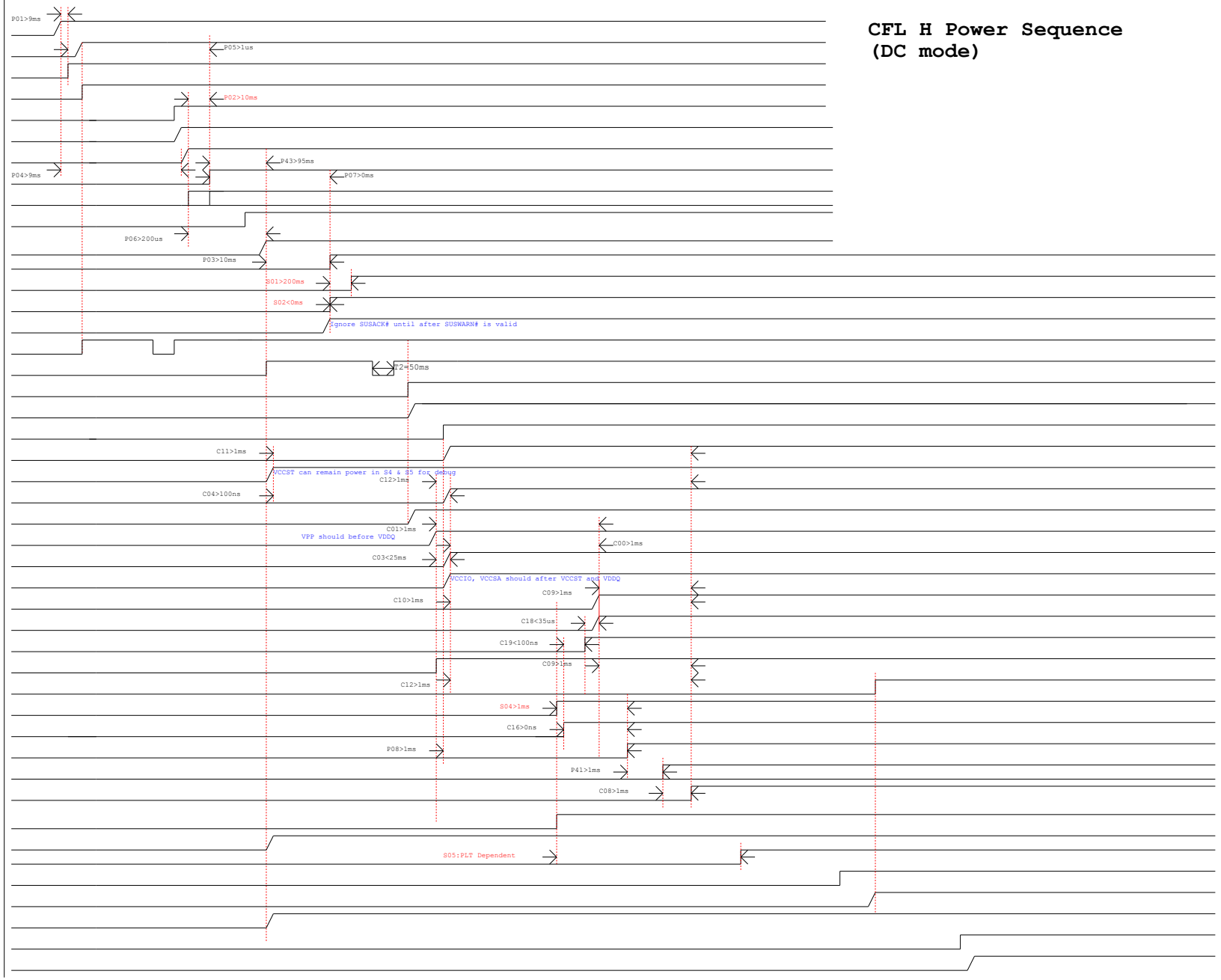
Date: Tuesday, April 28, 2020 | Sheet 102 of 106

CFL H Power Sequence (DC mode)

DC-IN Mode

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#) +12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#) +12VS/+5VS/+3VS
(VSUS_ON) +1.0V_VCCST,VCCPLL (VCCST_PWRGD)
(+VCCIO) +VCCSTG
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
(+12VS) +VCCPLL_OC
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL) +0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT



Project Name: GX502GX			Rev: 1.0
Title: Power On Timing-DC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: NB1 RD2 EE1	
Date: Tuesday, April 28, 2020	Sheet 101 of 104		

AC-IN Mode

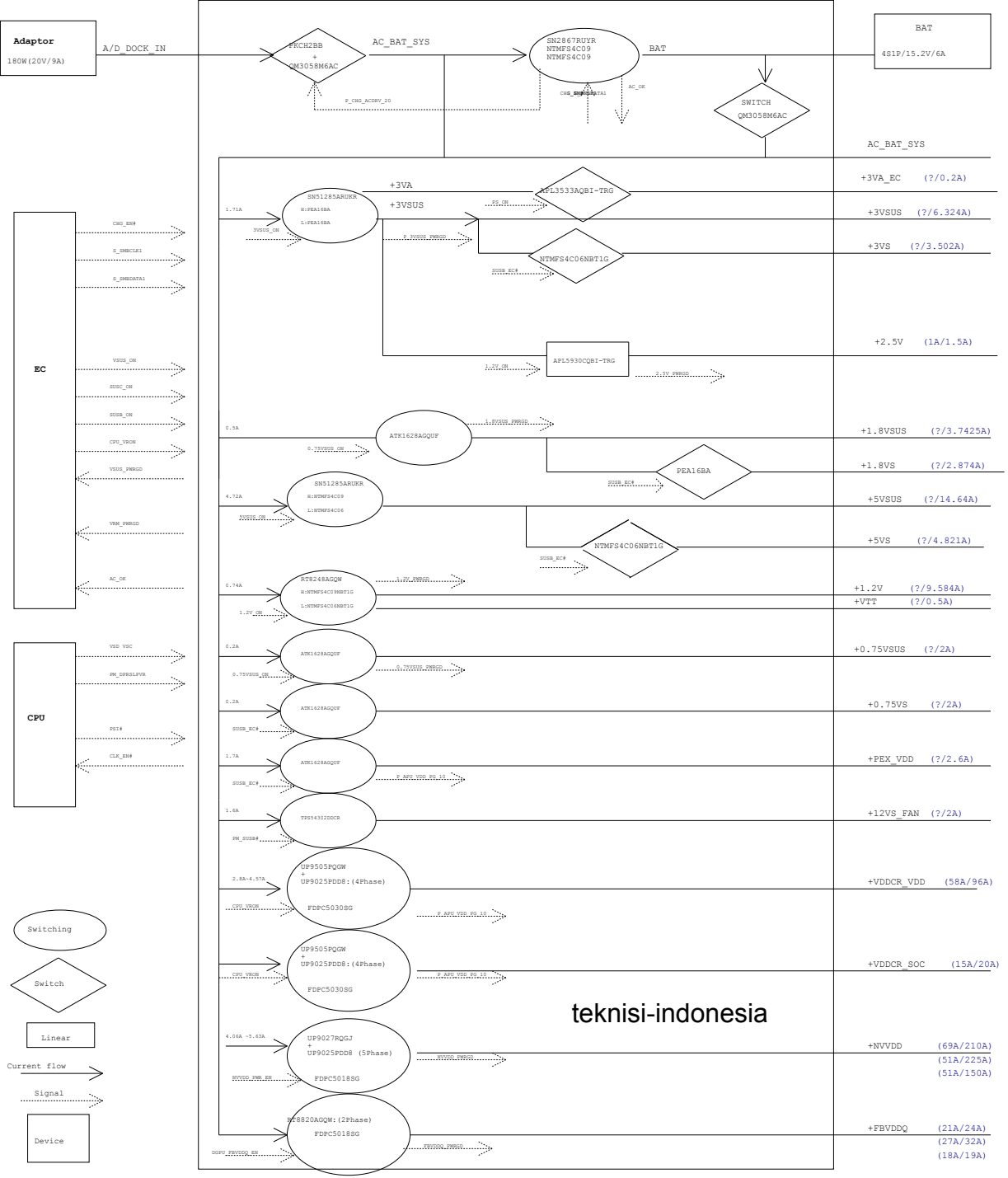
CFL H Power Sequence (AC mode)

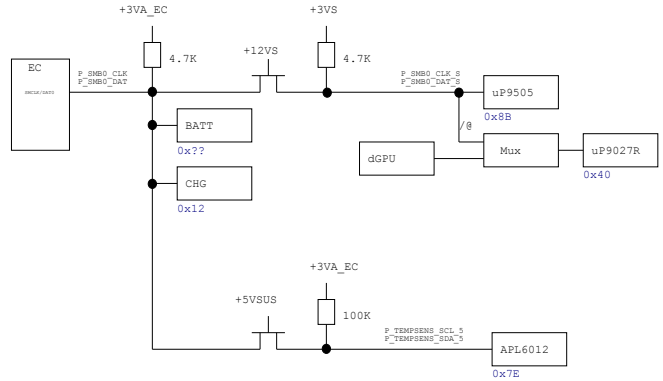
C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#) +12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#) +12VS/+5VS/+3VS
(SUSB_EC#) +1.0V_VCCST, VCCPLL
(SUSB_EC#) +VCCIO, (+12VS) +VCCSTG
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
(+12VS) +VCCPLL_OC
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL) +0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT

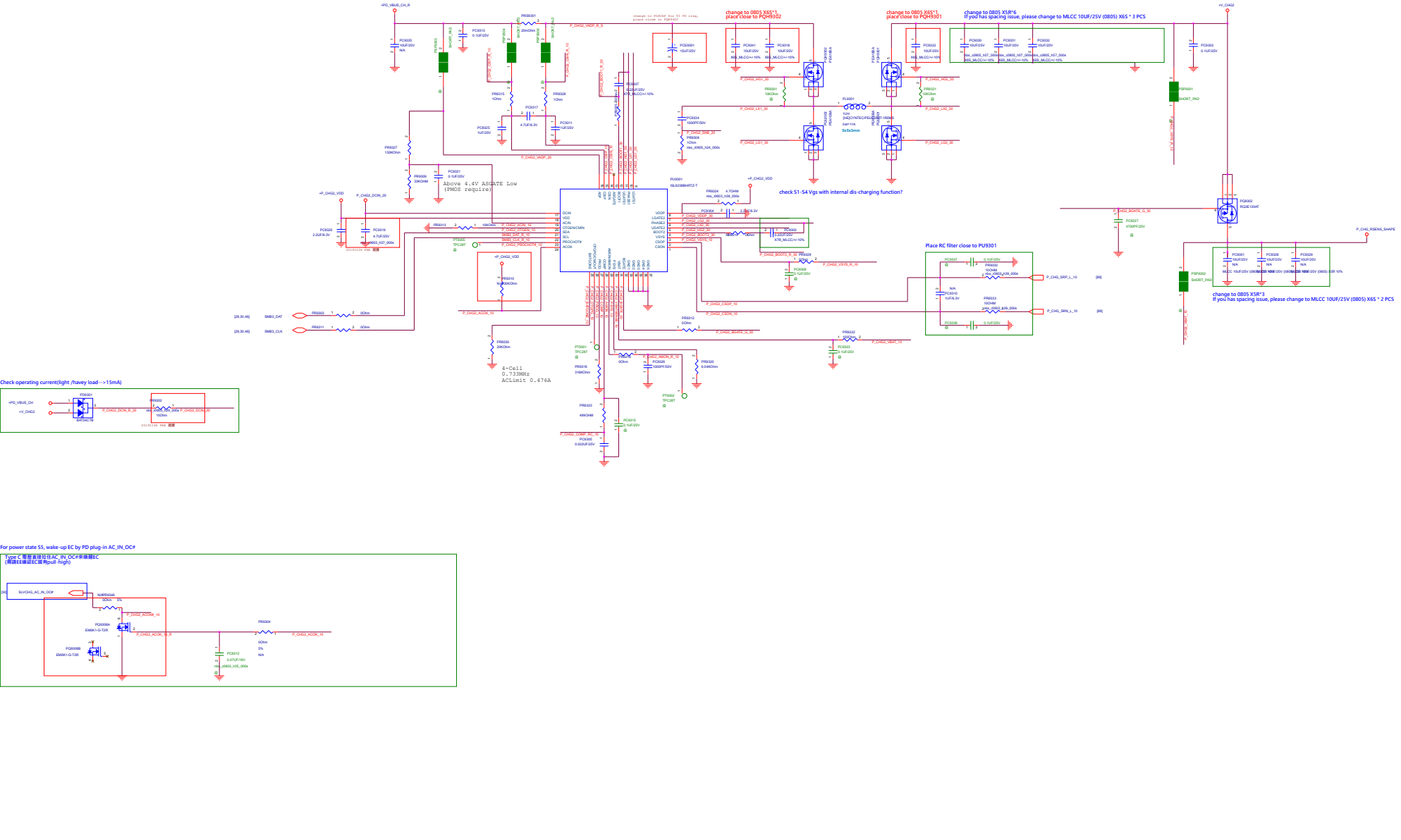
P01>9ms
P05>1us
P02>10ms
P43>95ms
P04>9ms
P07>0ms
P06>200us
P03>10ms
S01>200ms
S02<0ms
Ignore SUSACK# until after SUSWARN# is valid
T2=50ms
C11>1ms
VCCST can remain power in S4 & S5 for debug
C12>1ms
C04>100ns
C01>1ms
VPP should before VDDQ
C00>1ms
C03<25ms
VCCIO, VCCSA should after VCCST and VDDQ
C10>1ms
C09>1ms
C18<35us
C19<100ns
C09>1ms
C12>1ms
S04>1ms
C16>0ns
P08>1ms
P41>1ms
C08>1ms
S05:PLT Dependent

ASUS	Project Name: GX502GX		Rev: 1.0
Title : Power On Timing--AC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1	
Date: Tuesday, April 28, 2020	Sheet 100 of 104		

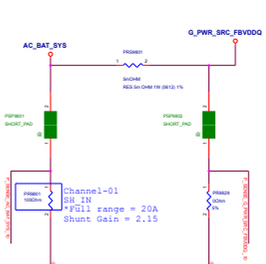


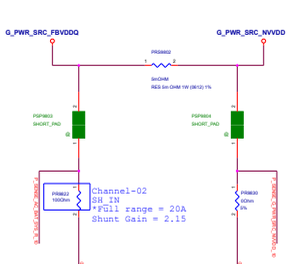


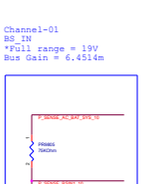
Charger ISL9238 (NVDC)

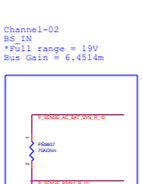


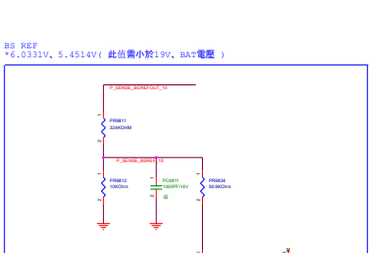
Project Name: GA502IV			Rev: R1.2
Title : Thunderbolt			
Size: A1	Dept.: ASUS Power Team	Engineer: CS Lin	
Date: Tuesday, April 28, 2020	Sheet 93 of 104		

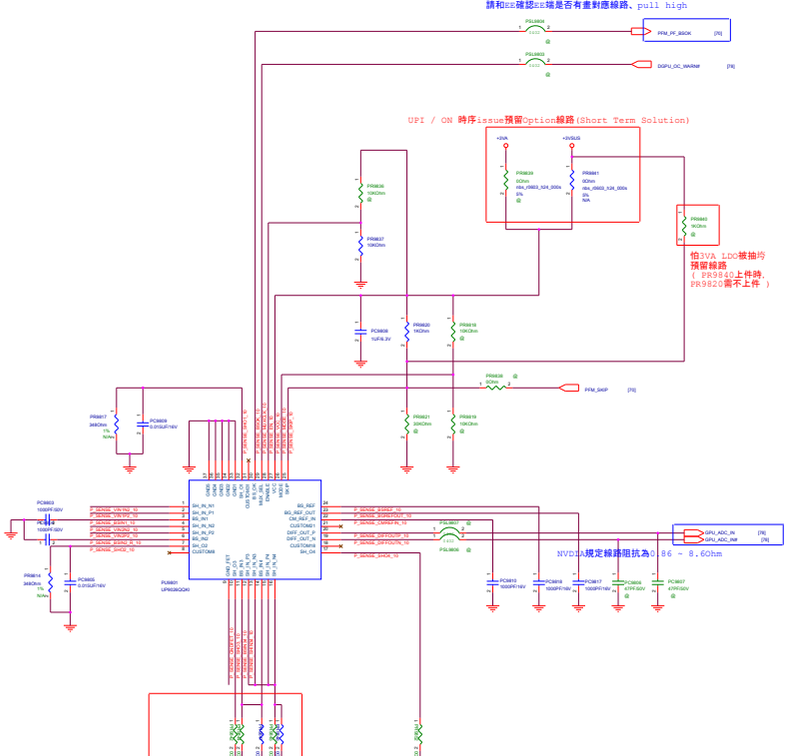












N18E

150W+

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	100Ω(10G2121000140l0)	
PR9817	127Ω (10G2121270140l0)	169Ω (10G2121690140l0)
PR9822	100Ω(10G2121000140l0)	
PR9814	127Ω (10G2121270140l0)	169Ω (10G2121690140l0)
PR9805	75kΩ(10G2127502140l0)	
PR9806	487Ω (10G2124870140l0)	649Ω (10G2126490140l0)
PR9807	75kΩ(10G2127502140l0)	
PR9808	487Ω (10G2124870140l0)	649Ω (10G2126490140l0)
PR9811	324kΩ (10G2123243140l0)	243kΩ (10G2122433140l0)
PR9812	10kΩ(10G2121002140l0)	
PR9834	90.9kΩ(10G2129092140l0)	

115W ~ 130W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9817	143Ω (10G2121430140l0)	191Ω (10G2121910140l0)
PR9814	143Ω (10G2121430140l0)	191Ω (10G2121910140l0)

100W ~ 110W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9817	165Ω (10G2121650140l0)	221Ω (10G2122210140l0)
PR9822		
PR9814	165Ω (10G2121650140l0)	221Ω (10G2122210140l0)

75W ~ 90W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9817	215Ω (10102-00571000)	287Ω (10G2122870140l0)
PR9822		
PR9814	215Ω (10102-00571000)	287Ω (10G2122870140l0)

75W-

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9817	357Ω (10G2123570140l0)	475Ω (10G2124750140l0)
PR9822		
PR9814	357Ω (10G2123570140l0)	475Ω (10G2124750140l0)

N18E-G1_65
N18E-G0_Max Q
N18P-G62-B

PR9817 357Ω (10G2123570140l0)
PR9814
348Ω (10G2123480140l0)

N18P

75W-

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	100Ω(10G2121000140l0)	
PR9817	357Ω (10G2123570140l0)	475Ω (10G2124750140l0)
PR9822	100Ω(10G2121000140l0)	
PR9814	357Ω (10G2123570140l0)	475Ω (10G2124750140l0)
PR9805	75kΩ(10G2127502140l0)	
PR9806	487Ω (10G2124870140l0)	649Ω (10G2126490140l0)
PR9807	75kΩ(10G2127502140l0)	
PR9808	487Ω (10G2124870140l0)	649Ω (10G2126490140l0)
PR9811	324kΩ (10G2123243140l0)	243kΩ (10G2122433140l0)
PR9812	10kΩ(10G2121002140l0)	
PR9834	90.9kΩ(10G2129092140l0)	

150w+

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	200Ω(10G2122000140l0)	
PR9817	127Ω (10G2121270140l0)	
PR9822	200Ω(10G2122000140l0)	
PR9814	127Ω (10G2121270140l0)	
PR9805	33kΩ (10G2123302140l0)	
PR9806	431Ω (10102-00581000)	
PR9807	33kΩ (10G2123302140l0)	
PR9808	431Ω (10102-00581000)	
PR9811	324kΩ (10G2123243140l0)	
PR9812	10kΩ(10G2121002140l0)	
PR9834	90.9kΩ(10G2129092140l0)	

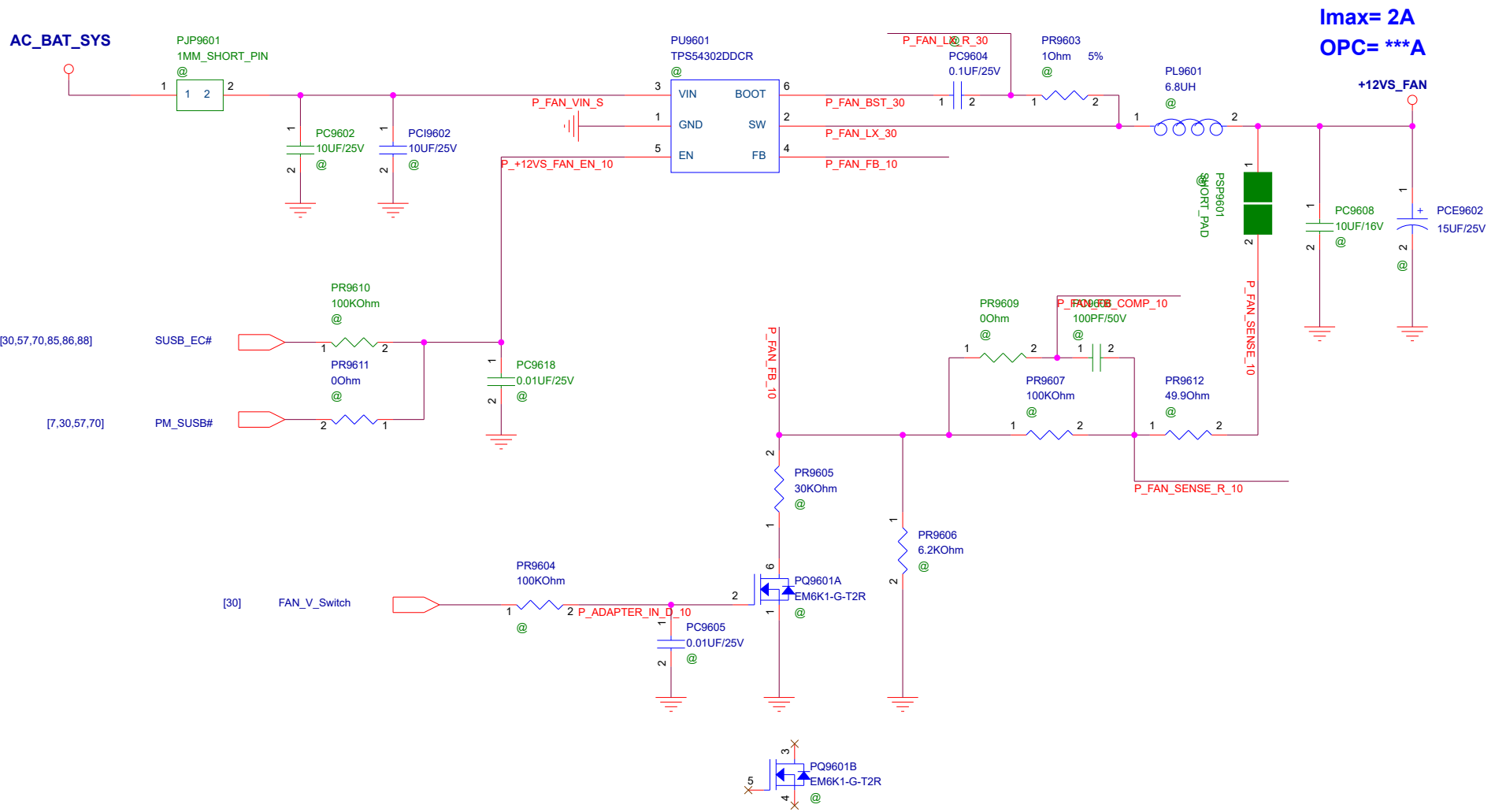
115W ~ 130W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	200Ω(10G2122000140l0)	
PR9817	143Ω (10G2121430140l0)	
PR9822	200Ω(10G2122000140l0)	
PR9814	143Ω (10G2121430140l0)	
PR9805	33kΩ (10G2123302140l0)	
PR9806	431Ω (10102-00581000)	
PR9807	33kΩ (10G2123302140l0)	
PR9808	431Ω (10102-00581000)	
PR9811	324kΩ (10G2123243140l0)	
PR9812	10kΩ(10G2121002140l0)	
PR9834	90.9kΩ(10G2129092140l0)	

75W ~ 90W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	200Ω(10G2122000140l0)	
PR9817	215Ω (10102-00571000)	
PR9822	200Ω(10G2122000140l0)	
PR9814	215Ω (10102-00571000)	
PR9805	33kΩ (10G2123302140l0)	
PR9806	431Ω (10102-00581000)	
PR9807	33kΩ (10G2123302140l0)	
PR9808	431Ω (10102-00581000)	
PR9811	324kΩ (10G2123243140l0)	
PR9812	10kΩ(10G2121002140l0)	
PR9834	90.9kΩ(10G2129092140l0)	

+12VS_FAN [For FAN]



<Variant Name>

ASUS	Project Name: GA502IV	Rev: R1.0
Title : PW_+12VS_FAN		
Size: A4	Dept.: NB Power team	Engineer: CS Lin
Date: Tuesday, April 28, 2020	Sheet 96 of 104	