1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

X2203/MLB

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
6	0031723518	ENGINEERING RELEASED	2021-10-03

LAST_MODIFICATION=Sun Oct 3 21:59:49 2021

LAST_MODIFICATION=Sun Oct 3 21:59:49 2021

LAST_MODIFICATION=Sun Oct 3 21:59:49 2021

X2203GHUB = https://github.pie.apple.com/MobileMacIX/j413_hw/blob/master/j413/

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SYNC_MASTER=eli SYNC_DATE=09/10/2021

DRAWING TITLE: SCHEM,MLB,X2203

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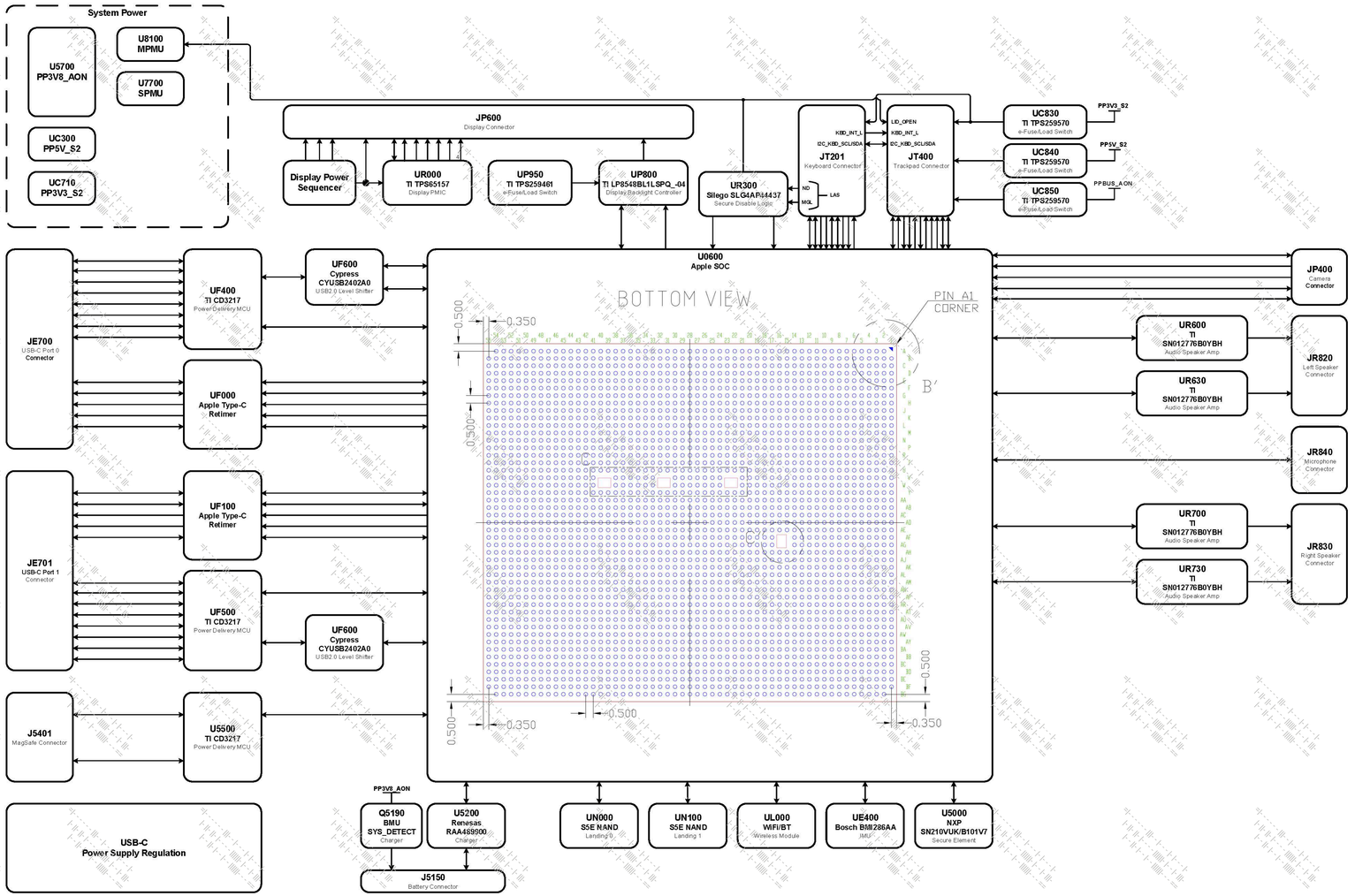
Block Diagram



SYNC_DATE=09/28/2021

PAGE TITLE

PAGE_TITLE=Block Diagram

Apple Inc.

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A BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	SCHEM,PCBF,COMMON,MLB_PROGPARTS,MLB_USBC,MLB_POWER,MLB_PMU,MLB_MECH,MLB_MISC,MLB_BLC,MLB_TCON,MLB_WIRELESS,EVT
MLB_USBC	ATCRTMR:B0,USBCPC:LAPTOP_B3,RT13_EFUSE:VDDIO,EUSB_LS:B0,ACE_WILL_BE_OTPED:YES,LFKA_TEST_MODE:YES
MLB_PROGPARTS	SOC_ROM:BLANK,RT13_ROM:BLANK,SE:DEV_SW_LN,UPC01_ROM:EVT,UPC5_ROM:EVT
MLB_POWER	P3V8AON_IC:A2_R170,P3V8AON_LPM,WHAMOLA:0A5-13V7,P5VS2PWREN_BYPASS:NO
MLB_PMU	MPMU_IC:A0_JPI,SPMU_IC:A0_JPI,PMU_BULK_VDDQL,PMU_32K_CLK:XOSC,PMU_FB:FF,BUCK6_BULK_REG
MLB_MECH	SHLD_CAN_MLB:EVT,BRKT_KBD:EVT
MLB_MISC	BOARD_ID,TPAD_32KCLK:NO,SYSDET:FET,BOOT_CFG_0,PMU_OUT32K:WLBT,SENSOR_IMU,MIPI_PWR:NO,REFIMU_IC:BMI284,QS360_DLY:YES,SOC_R9706:80HM,OCELOT_BYPASS:100NF
MLB_DEV	SENSORS:DEV,DEVELOPMENT,USBC_DBG,BTN_DBG
MLB_BLC	BLC_BEN_IC:V8,BLC_5V_CAP:4P7_UF,BLC_5V_SERIES:10_OHM,BLC_KBD_BOOST_USED:NO
MLB_TCON	PMIC_SDG_VBUCK1:NO,SDG_TI_PROG:X2203,SDG_TI
MLB_WIRELESS	RF-CONN

B Build Specific Groups

BOM GROUP	BOM OPTIONS
BOARD_ID	BOARD_ID_3
PROTO0	BOARD_REV_3,BOARD_REV_2,BOARD_REV_1,BOARD_REV_0
PROTO1	BOARD_REV_3,BOARD_REV_2,BOARD_REV_1
PROTO1B	BOARD_REV_3,BOARD_REV_2,BOARD_REV_0
PROTO2	BOARD_REV_3,BOARD_REV_2
PROTO2B	BOARD_REV_3,BOARD_REV_1,BOARD_REV_0
EVT	BOARD_REV_3,BOARD_REV_1
DVT	BOARD_REV_3,BOARD_REV_0
PVT	BOARD_REV_3

Pull-ups: BOARD_ID[7:0] = 8'b0010_1000
Pull-downs: 4'b0000
Pull-downs: 4'b0001
Pull-downs: 4'b0010
Pull-downs: 4'b0011
Pull-downs: 4'b0100
Pull-downs: 4'b0101
Pull-downs: 4'b0110
Pull-downs: 4'b0111

C DC/DC BOM Groups

BOM GROUP	BOM OPTIONS
DCDC_COMMON	SCHEM,PCBF,COMMON,MLB_POWER,MLB_PMU,MLB_MECH,MLB_MISC,MLB_BLC,EVT

D RF BOM Groups

BOM GROUP	BOM OPTIONS
RF_COMMON	SCHEM,PCBF,RF-CONN

E Top-Level APNs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-07020	1	SCHEM,MLB,X2203	SCHEM	CRITICAL	SCHEM
820-02536	1	PCBF,MLB,X2203	PCBF	CRITICAL	PCBF
685-00426	1	COMMON PARTS,MLB,X2203	CBOM	CRITICAL	CMN_PARTS_BOM
685-00427	1	NAND1,MLB,X2203	PIBOM	CRITICAL	PARTS_SSDNAND1
985-01536	1	DEV PARTS,MLB,X2203	DEV1	CRITICAL	DEV_PARTS_BOM

F Reference Design Pack Options

USB-C

PACK_OPTIONS TO INCLUDE IN NETLIST
USBC_SPI_UPC0
USBC_DEBUG_UPC0
USBC01_VR5V_LOCAL_NO
USBC_LAPTOP
PKGS:SMALL_PITCH
USBC_LAPTOP_CC_PRT
ACE2_SS_CAP
USBC_SPI_NO_2ND_ROM
USBC_SPI_UPC0_AND_NO_2ND_ROM
ACTIVE_READY:SMALL_PITCH_CHECK_WITH_DFM
INV:DPW

Iceman VR

PACK_OPTIONS TO INCLUDE IN NETLIST
3V8_AON_PBUS-18V
3V8_AON_I2C-DEV
3V8_INDUCTOR:1P5MM
3V8_AON_MLCC-LN

Wireless

PACK_OPTIONS TO INCLUDE IN NETLIST
SUNWAY
WLBT_D2R_TP_STATEN
WLBT_TP_0P2

Audio

PACK_OPTIONS TO INCLUDE IN NETLIST
SPKRAMP_A
SPKRAMP_B
SPKRAMP_D
SPKRAMP_E
SPKRAMP_ICC_GB

PP3V3_S2 VR

PACK_OPTIONS TO INCLUDE IN NETLIST
3V3_S2_PBUS-18V
3V3_S2_MLCC-LN
3V3_S2_VOUT-B12

Charger

PACK_OPTIONS TO INCLUDE IN NETLIST
CHGR_72W
CHGR_PBUS18V
CHGR_MLCC-LN

PP5V_S2 VR

PACK_OPTIONS TO INCLUDE IN NETLIST
5V_S2_PBUS18V
5V_S2_VOUT-B12
5V_S2_IND-15
5V_S2_MLCC-LN
5V_S2_THINSTNCL

Display Backlight

PACK_OPTIONS TO INCLUDE IN NETLIST
BLC_CBULK:0603
BLC_FET:OFF
BLC_IND:10UH
PANELPWR_MINNIE
BLC_FERRITE:YES

SOC

PACK_OPTIONS TO INCLUDE IN NETLIST
SOC_MIPI_ENABLE
SOC_MIPI_1SIDE
ONE_SIDED
PCIE_GP0
LPDP_INT_RCAL
LPDPRX0_RCAL
OCELOT_BYPASS:10UF

NAND

PACK_OPTIONS TO INCLUDE IN NETLIST
SSD_4_3UF_0402THIN

PMU

PACK_OPTIONS TO INCLUDE IN NETLIST
TPAD32K:PMU
PMU_32K_MEMS
PMU_32K_XOSC

This is on purpose

IMU

PACK_OPTIONS TO INCLUDE IN NETLIST
REFIMU_VDD:LCFILT
REFIMU_TEST:NO

SYNC_DATE=09/10/2021

PAGE TITLE: BOM Configuration

Apple Inc.

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A Mounting Holes

SH0400
TH-NSP
1
SL-3.41X2.0-5.91X4.5
998-19374

SH0401
4.6R2.0-NSP
1
998-25030

SH0403
4.6X5.2R1.7X2.3-NSP
1
998-11114

SH0402
5.0R2.0-NSP
1
998-25031

B MDB Cowling Bosses

SH0440
2.7X1.8R-1.4ID-1.26H-SM
1
860-01964

C MagSafe/USB-C Cowling Bosses

SH0450
2.7X1.8R-1.4ID-1.16H-SM
1
860-01916

SH0451
2.7X1.8R-1.4ID-1.16H-SM
1
860-01916

SH0452
2.7X1.8R-1.4ID-1.16H-SM
1
860-01916

SH0453
2.7X1.8R-1.4ID-1.16H-SM
1
860-01916

D WiFi Module Cowling Boss

SH0470
1.8X2.7R-1.64H-SM
1
860-01957

E Right Speaker Cowling Boss

SH0480
6.12X1.8R-2HOLE-1.38H
1
860-01912

F MLB Shield Fence

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-32496	1	SHIELD,FENCE,THERMAL,MLB,P1,X2147	SHLD1	CRITICAL	SHLD_CAN_MLB:P2
806-35214	1	FENCE,MLB,EVT,X2147	SHLD1	CRITICAL	SHLD_CAN_MLB:EVT

SH0430
TH-NSP
1
SL-0.5X1.28-1.25X2.03
998-21458

SH0432
TH-NSP
1
SL-0.5X1.28-1.25X2.03
998-21458

SH0434
TH
1
SL-0.4X1.20
998-1681

SH0436
TH-NSP
1
SL-0.5X1.28-1.25X2.03
998-21458

SH0431
TH-NSP
1
SL-0.5X1.28-1.25X2.03
998-21458

SH0433
TH-NSP
1
SL-0.5X1.28-1.25X2.03
998-21458

SH0435
TH
1
SL-0.4X1.20
998-1681

SH0437
TH-NSP
1
SL-0.5X1.28-1.25X2.03
998-21458

G SOC Thermal Module Bosses

SH0490
STDOFF-3.8X2.5R-1.36H-SM
1
860-01913

SH0491
STDOFF-3.8X2.5R-1.36H-SM
1
860-01913

SH0492
STDOFF-3.8X2.5R-1.36H-SM
1
860-01913

SH0493
STDOFF-3.8X2.5R-1.36H-SM
1
860-01913

H Antenna Cowling Bosses

SH04A0
2.44X2.44SQ-1.15ID-1.044H-SM
1
860-02043

SH04A1
2.44X2.44SQ-1.15ID-1.044H-SM
1
860-02043

I Spacers

SH04B0
SPACER-MLB-X2147
SM
1
806-31591

SH04B2
SPACER-MLB-SMT-SML
SM
1
806-31120

SH04B1
SPACER-MLB-SMT
SM
1
806-31119

SH04B3
SPACER-MLB-SMT-LRG
SM
1
806-31121

J Keyboard Bracket

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-32523	1	BRKT,MLB,SMT,X2147	BRKT1	CRITICAL	BRKT_KBD:P2
806-35209	1	BRKT,MLB,EVT,X2147	BRKT1	CRITICAL	BRKT_KBD:EVT

BOM_COST_GROUP=MECHANICALS

SYNC_DATE=09/10/2021

PAGE TITLE
PD Parts

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DRAWING NUMBER 051-07020
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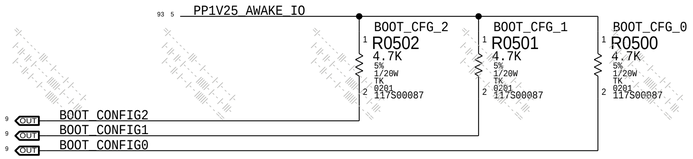
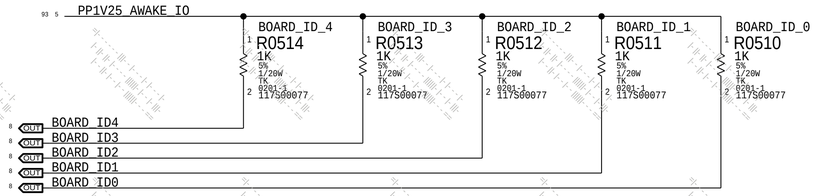
A BOOT CONFIG ID



STATEN BOOT AND POWER uARCH SPEC 2.1.5 (Section 2.2, Table 2.3):

BOOT_CFG[2:0]	MODE
000	NAND, 1.2V SPI0, 12MHZ, TESTMODE
001	NOR, 1.2V SPI1, 40MHZ
010	NAND, 1.2V SPI0, 12MHZ
011	NAND, 1.2V SPI0, 40MHZ
100	NOR, 1.2V SPI1, 12MHZ, TESTMODE
101	NOR, 1.2V SPI1, 40MHZ, TESTMODE
110	NOR, 1.2V SPI1, 6MHZ, TESTMODE
111	NOR, 1.2V SPI1, 12MHZ

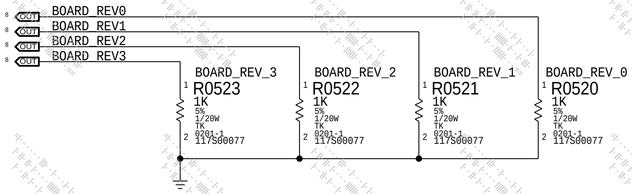
B BOARD ID



- BOARD_ID[7:0] assignments by product at link in QR Code.
- BOARD_ID[7:5] come from SOC
- BOARD_ID[4:0] are straps on MLB, sampled 100US after cold reset deassert.
- Staten Boot Power Micro Architecture Spec 2.1.3

BoardID Wiki URL:

C BOARD REV



- Stuffing the Resistor Results in a Logic Low (1'b0)

BOM_COST_GROUP=SOC

SYNC_MASTER=SOC SYNC_DATE=10/01/2021

PAGE TITLE: SOC: CONFIG STRAPS

Apple Inc.

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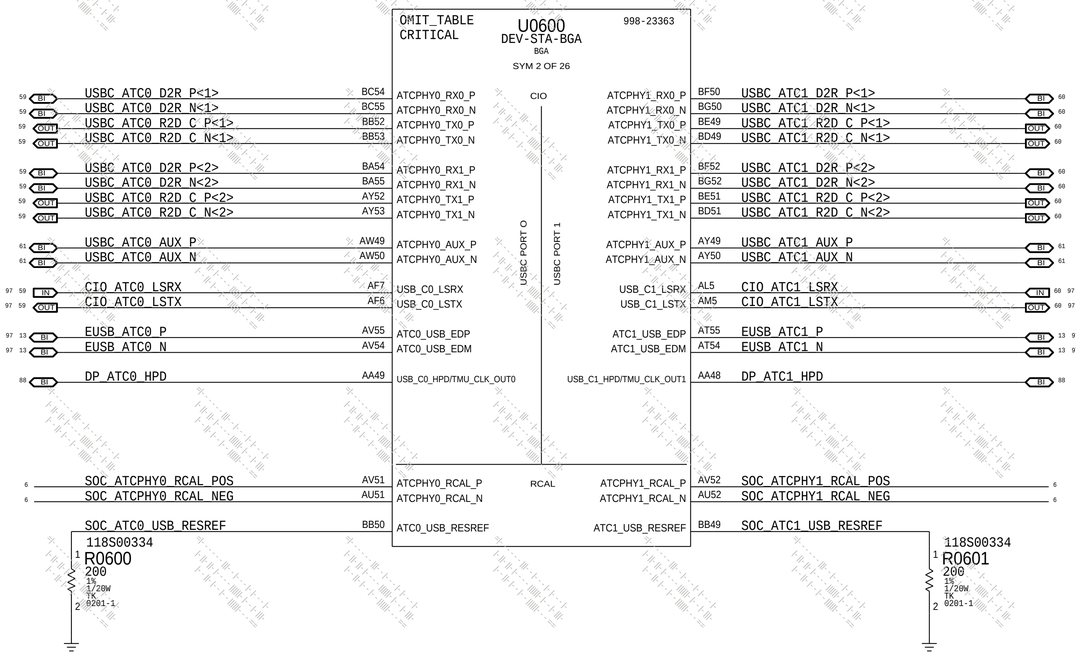
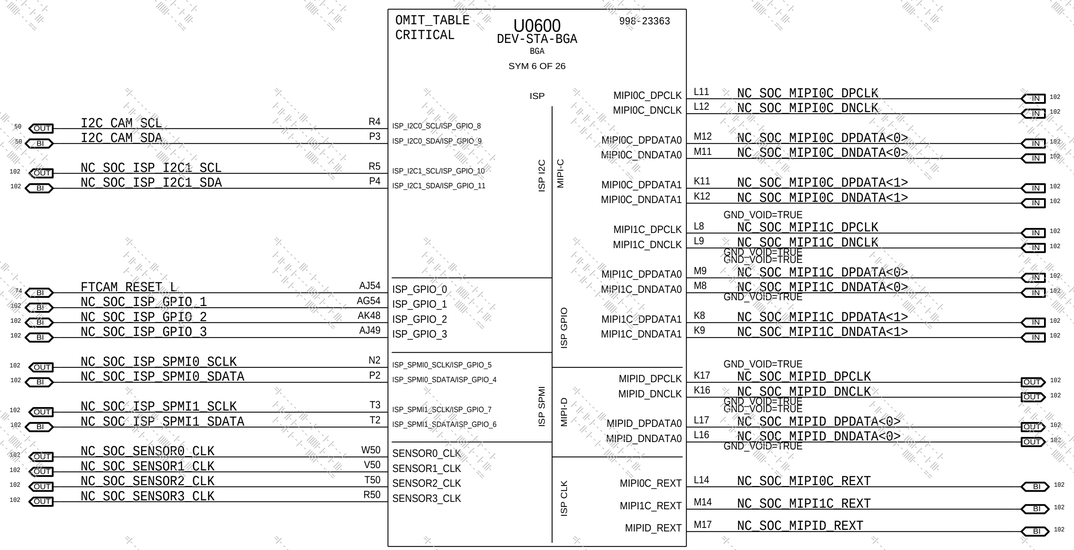
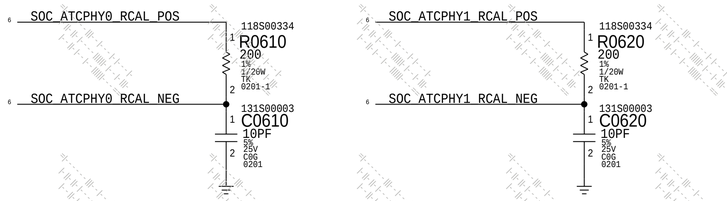




A Termination Resistance Calibration (RCAL)



Scan for RCAL Info:

BOM_COST_GROUP=SOC

SYNC_MASTER=SOC SYNC_DATE=10/01/2021

PAGE TITLE: SOC: CIO, MIPI

Apple Inc.

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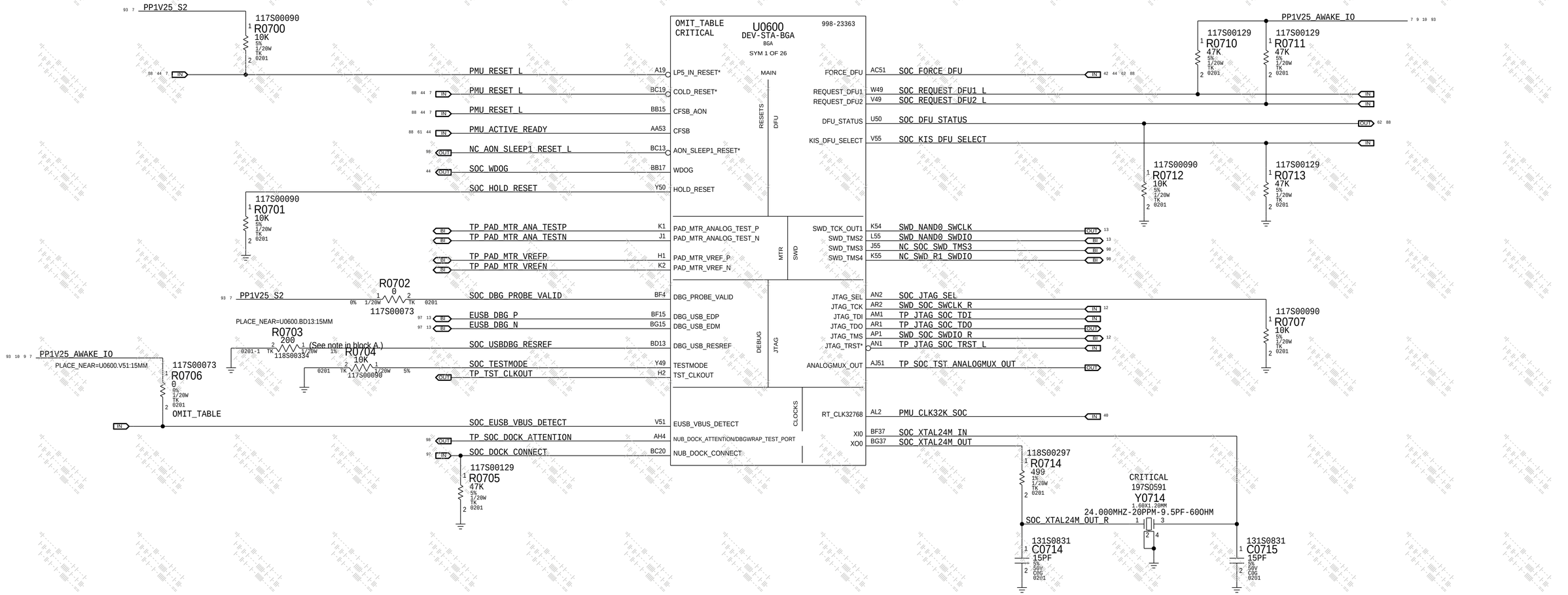

A RESREF Notes

- The RESREF node is sensitive to noise.
- 1-sided PCBs may be able to place R0703 less than 15mm from SOC pin on the perimeter of the SOC.
- 2-sided PCBs may be able to place R0703 less than 5mm from SOC pin.

B EUSB_VBUS_DETECT BOM Table

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S00090	1	RES,TK,10K OHM,5%,1/20W,0201	R0706	SOC_R0706:10KOHM
117S00073	1	RES,TK,0 OHM,1A MAX,1/20W,0201	R0706	SOC_R0706:0OHM

BOM_COST_GROUP=SOC

SYNC_MASTER=SOC SYNC_DATE=10/01/2021

PAGE TITLE: SOC: RESETS, DEBUG, MISC

Apple Inc.

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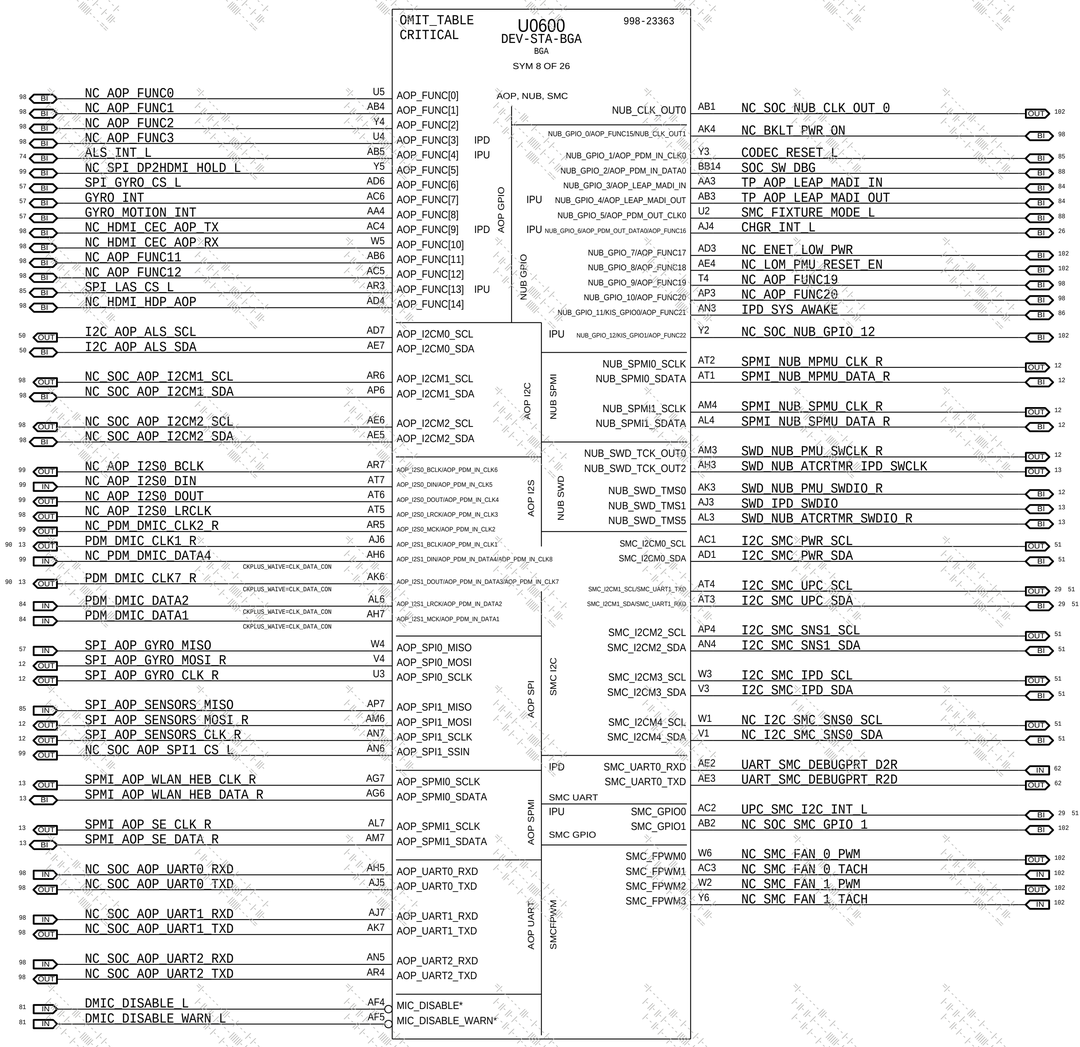

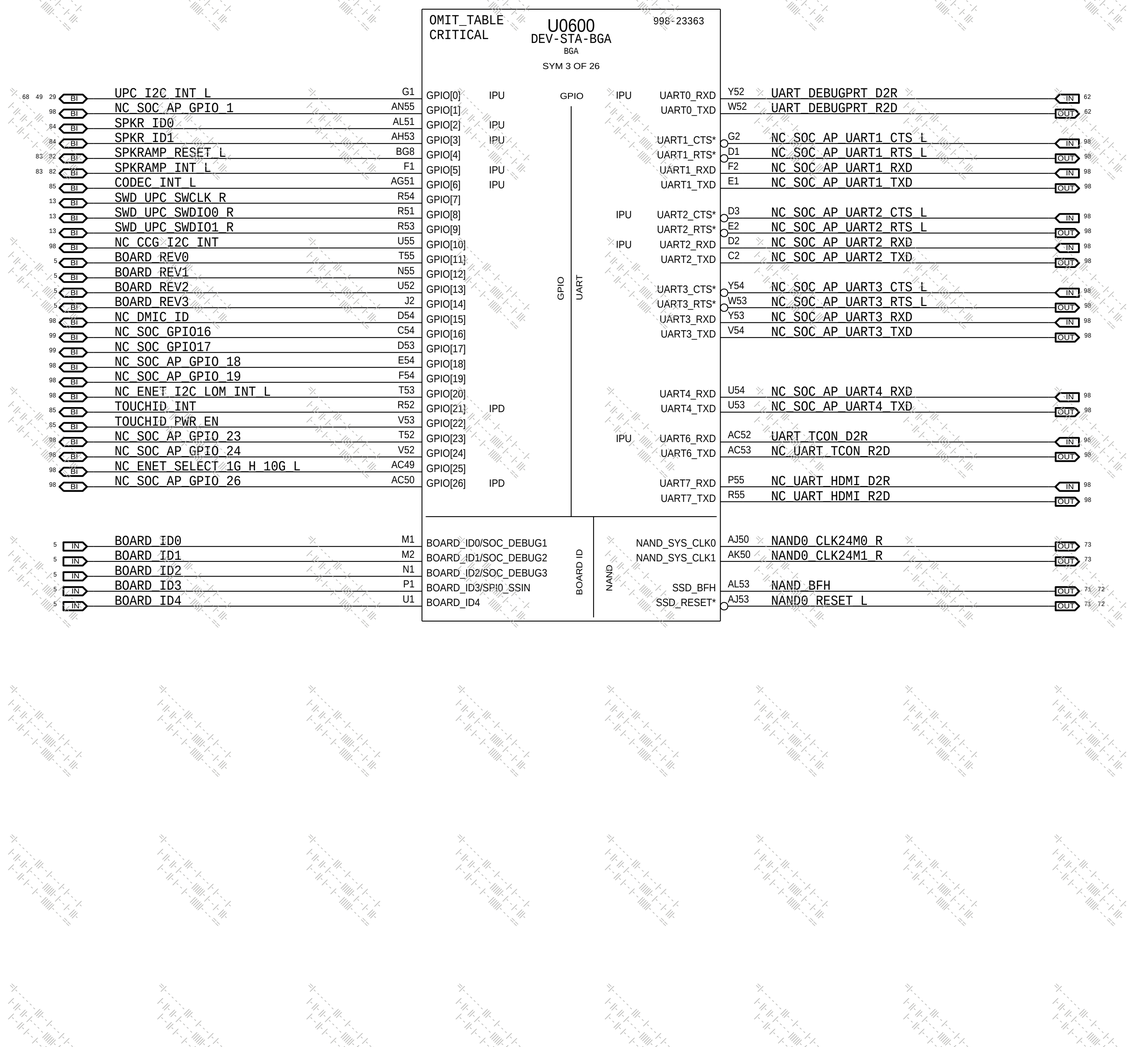

BOM_COST_GROUP=SOC

SYNC_MASTER=SOC SYNC_DATE=10/01/2021

PAGE TITLE: SOC: GPIOS

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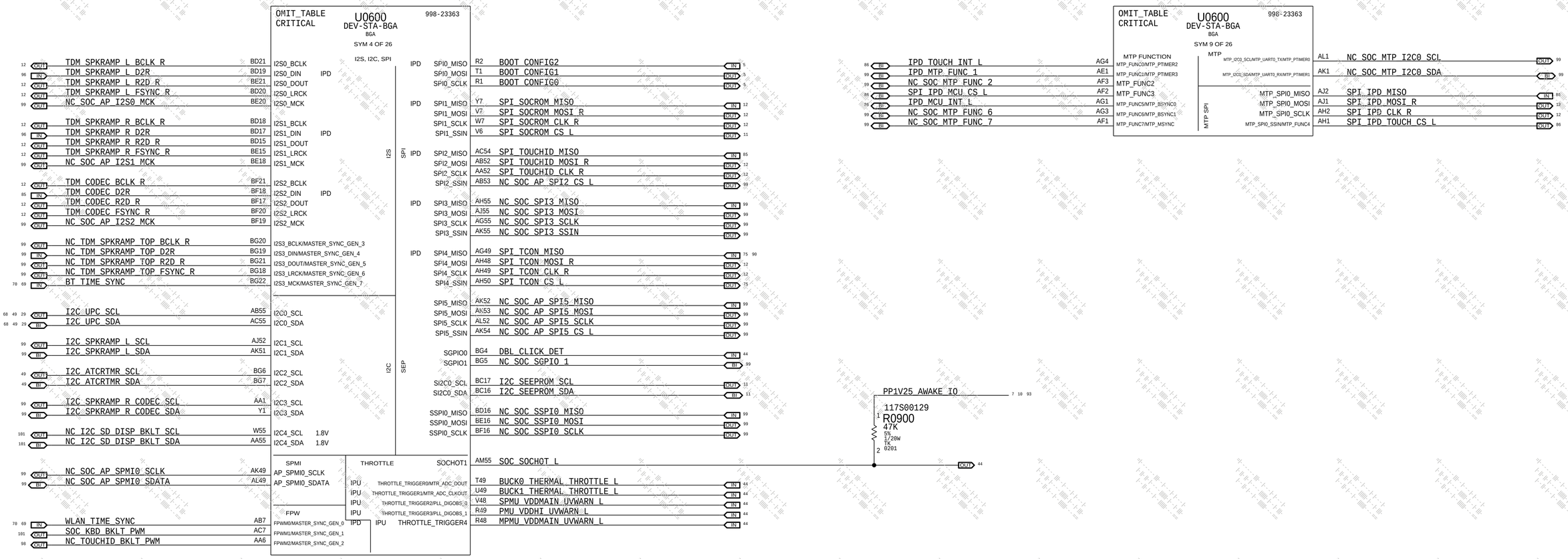

SYNC_MASTER=SOC SYNC_DATE=10/01/2021

PAGE TITLE

SOC: GPIOS

Apple Inc.

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BOM_COST_GROUP=SOC

OMIT_TABLE
CRITICAL
U0600
DEV-STA-BGA
BGA
998-23363
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LPDP & DISP
LPDP_FTCAM_AUX_C
NC_SOC_LPDP_RX_AUX_D1
NC_SOC_LPDP_RX_AUX_D2
NC_SOC_LPDP_RX_AUX_D3
NC_SOC_LPDP_RX_AUX_D4
NC_SOC_LPDP_RX_AUX_D5
NC_SOC_LPDP_RX_AUX_D6
NC_SOC_LPDP_RX_AUX_D7
NC_SOC_LPDP_RX_AUX_D8
NC_SOC_LPDP_RX_AUX_D9
NC_SOC_LPDP_RX_AUX_D10
NC_SOC_LPDP_RX_AUX_D11
LPDP_FTCAM_DATA_P<0>
LPDP_FTCAM_DATA_N<0>
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NC_SOC_LPDP_RX_D1N
NC_SOC_LPDP_RX_D2P
NC_SOC_LPDP_RX_D2N
NC_SOC_LPDP_RX_D3P
NC_SOC_LPDP_RX_D3N
NC_SOC_LPDP_RX_D4P
NC_SOC_LPDP_RX_D4N
NC_SOC_LPDP_RX_D5P
NC_SOC_LPDP_RX_D5N
NC_SOC_LPDP_RX_D6P
NC_SOC_LPDP_RX_D6N
NC_SOC_LPDP_RX_D7P
NC_SOC_LPDP_RX_D7N
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NC_SOC_LPDP_RX_D8N
NC_SOC_LPDP_RX_D9P
NC_SOC_LPDP_RX_D9N
NC_SOC_LPDP_RX_D10P
NC_SOC_LPDP_RX_D10N
NC_SOC_LPDP_RX_D11P
NC_SOC_LPDP_RX_D11N
SOC_LPDPRX_RCAL_POS
SOC_LPDPRX_RCAL_NEG
NC_SOC_LPDP_RX1_RCAL_POS
NC_SOC_LPDP_RX1_RCAL_NEG
LPDP_INT_DATA_C_P<0>
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LPDP_INT_DATA_C_N<2>
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LPDP_INT_DATA_C_N<3>
LPDP_INT_AUX_C_P
LPDP_INT_AUX_C_N
SOC_LPDP_INT_RCAL_POS
SOC_LPDP_INT_RCAL_NEG
NC_LPDP_EXT_DATA_CP<0>
NC_LPDP_EXT_DATA_CN<0>
NC_LPDP_EXT_DATA_CP<1>
NC_LPDP_EXT_DATA_CN<1>
NC_LPDP_EXT_DATA_CP<2>
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NC_LPDP_EXT_DATA_CN<3>
NC_LPDP_EXT_AUX_CP
NC_LPDP_EXT_AUX_CN
NC_SOC_LPDP_DP2HDMI_RCAL_POS
NC_SOC_LPDP_DP2HDMI_RCAL_NEG
LPDP_INT_HPD
NC_LPDP_EXT_HPD
I2C_DISP_BKLT_SCL
I2C_DISP_BKLT_SDA
NC_SPI_DISP_BKLT_CLK_R
NC_SPI_DISP_BKLT_CS_L
NC_SPMI_DISP_BKLT_CLK
NC_SPMI_DISP_BKLT_DATA
NC_SOC_DISP_POL
NC_DISP_BKLT_FSYNC
DISP_BKLT_LSYNC
NC_SOC_DISP_TOUCH_BSYNC_0
NC_SOC_DISP_TOUCH_BSYNC_1
NC_SOC_DISP_TOUCH_EB
NC_BKLT_BOOST_THROTTLE_L
NC_SOC_DFR_DISP_TE
OMIT_TABLE
CRITICAL
U0600
DEV-STA-BGA
BGA
998-23363
SYM 7 OF 26
PCIE, MTR
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SOC_ST_PCIE_RCAL_POS
SOC_ST_PCIE_RCAL_NEG
PCIE_WLBT_D2R_P
PCIE_WLBT_D2R_N
PCIE_WLBT_R2D_C_P
PCIE_WLBT_R2D_C_N
PCIE_CLK100M_WLBT_P
PCIE_CLK100M_WLBT_N
WLBT_CLKREQ_L
WLBT_RESET_L
NC_SOC_GP_PCIE_RX1P
NC_SOC_GP_PCIE_RX1N
NC_SOC_GP_PCIE_TX1P
NC_SOC_GP_PCIE_TX1N
NC_SOC_GP_PCIE_CLK1_100MP
NC_SOC_GP_PCIE_CLK1_100MN
NC_SOC_GP_PCIE_CLKREQ_1_L
NC_SOC_GP_PCIE_PERST_1_L
NC_SOC_GP_PCIE_RX2P
NC_SOC_GP_PCIE_RX2N
NC_SOC_GP_PCIE_TX2P
NC_SOC_GP_PCIE_TX2N
NC_SOC_GP_PCIE_CLK2_100MP
NC_SOC_GP_PCIE_CLK2_100MN
NC_SOC_GP_PCIE_CLKREQ_2_L
NC_SOC_GP_PCIE_PERST_2_L
NC_SOC_GP_PCIE_RX3P
NC_SOC_GP_PCIE_RX3N
NC_SOC_GP_PCIE_TX3P
NC_SOC_GP_PCIE_TX3N
NC_SOC_GP_PCIE_CLK3_100MP
NC_SOC_GP_PCIE_CLK3_100MN
NC_SOC_GP_PCIE_CLKREQ_3_L
NC_SOC_GP_PCIE_PERST_3_L
SOC_GP_PCIE_RCAL_POS
SOC_GP_PCIE_RCAL_NEG
A Termination Resistance Calibration (RCAL)
R1020 200
C1020 10PF
R1021 200
C1021 10PF
R1022 200
C1022 10PF
R1023 200
C1023 10PF
R1024 200
C1024 10PF
R1025 200
C1025 10PF
Scan for RCAL Info:
B PCIe CLKREQ/PERST Pull-Ups/Downs
PP1V25_AWAKE_IO
R1000 47K WLBT_CLKREQ_L
R1001 47K NC_SOC_GP_PCIE_CLKREQ_1_L
R1002 47K NC_SOC_GP_PCIE_CLKREQ_2_L
R1003 47K NC_SOC_GP_PCIE_CLKREQ_3_L
R1004 47K NAND0_CLKREQ0_L
R1005 47K NAND0_CLKREQ1_L
R1010 47K WLBT_RESET_L
R1011 47K NC_SOC_GP_PCIE_PERST_1_L
R1012 47K NC_SOC_GP_PCIE_PERST_2_L
R1013 47K NC_SOC_GP_PCIE_PERST_3_L
R1014 47K NAND0_PCIE_RESET_L
BOM_COST_GROUP=SOC
SYNC_MASTER=SOC
PAGE TITLE
SOC: LPDP, PCIE
Apple Inc.
DRAWING NUMBER 051-07020
SIZE D
REVISION 6.0.0
BRANCH evt-1
PAGE 10 OF 801
SHEET 10 OF 113
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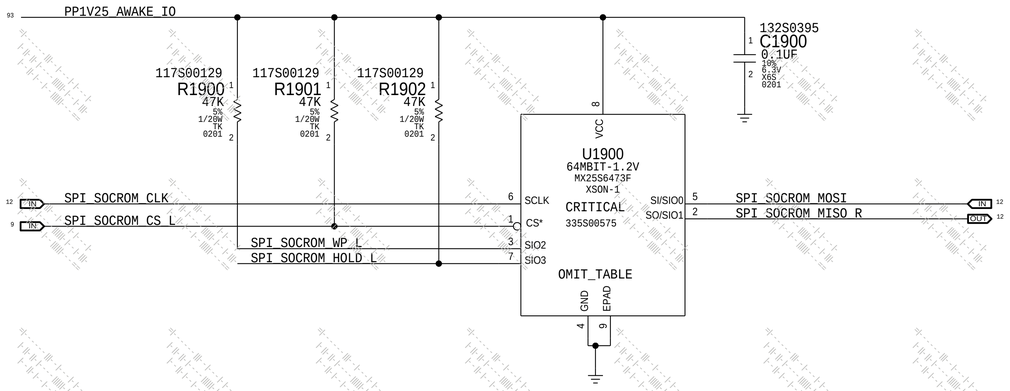
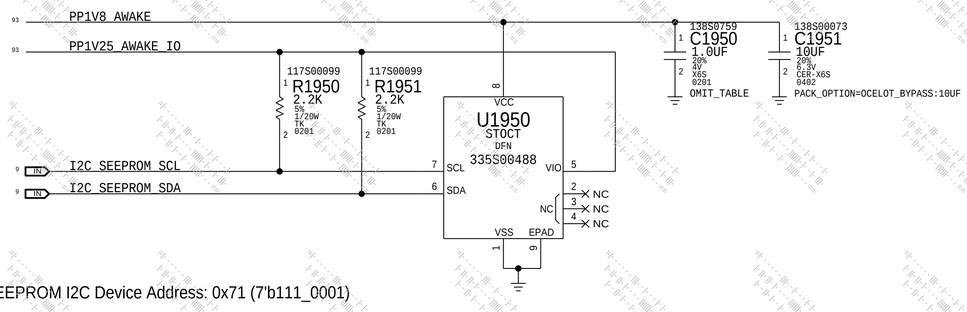
A SPI ROM



B SEP EEPROM



SEP EEPROM I2C Device Address: 0x71 (7'b111_0001)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S0759	1	CAP,CER,1UF,20%,4V,X6S,0201	C1950		OCELOT_BYPASS:1UF
132S0395	1	CAP,CER,0.1UF,10%,6.3V,X6S,0201	C1950		OCELOT_BYPASS:100NF

BOM_COST_GROUP=SOC

SYNC_MASTER=SOC SYNC_DATE=10/01/2021

PAGE TITLE: SOC: SPI NOR, SEP ROM

Apple Inc.

DRAWING NUMBER: 051-07020 SIZE: D

REVISION: 6.0.0

BRANCH: evt-1

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A SOC ROM Source Terminations

R2000 — 20 — 1% 1/20W TK 0201 — 118S00467
SPI_SOCROM_MISO (OUT, 9) → SPI_SOCROM_MISO_R (IN, 11)
PLACE_NEAR=U0600.Y7:10MM

R2001 — 20 — 1% 1/20W TK 0201 — 118S00467
SPI_SOCROM_MOSI_R (IN, 9) → SPI_SOCROM_MOSI (OUT, 11)
PLACE_NEAR=U0600.V7:10MM

R2002 — 20 — 1% 1/20W TK 0201 — 118S00467
SPI_SOCROM_CLK_R (IN, 8) → SPI_SOCROM_CLK (OUT, 11)
PLACE_NEAR=U0600.W7:10MM

B TOUCHID Source Terminations

R2004 — 20 — 1% 1/20W TK 0201 — 118S00467
SPI_TOUCHID_MOSI_R (IN, 9) → SPI_TOUCHID_MOSI (OUT, 85)
PLACE_NEAR=U0600.AB52:10MM

R2005 — 20 — 1% 1/20W TK 0201 — 118S00467
SPI_TOUCHID_CLK_R (IN, 9) → SPI_TOUCHID_CLK (OUT, 85)
PLACE_NEAR=U0600.AA52:10MM

C IPD Source Terminations

R2006 — 20 — 1% 1/20W TK 0201 — 118S00467
SPI_IPD_MOSI_R (IN, 9) → SPI_IPD_MOSI (OUT, 86)
PLACE_NEAR=U0600.AJ1:10MM

R2007 — 20 — 1% 1/20W TK 0201 — 118S00467
SPI_IPD_CLK_R (IN, 9) → SPI_IPD_CLK (OUT, 86)
PLACE_NEAR=U0600.AH2:10MM

D TCON Source Terminations

R2090 — 20 — 1% 1/20W TK 0201 — 118S00467
SPI_TCON_MOSI_R (IN, 9) → SPI_TCON_MOSI (OUT, 75 90)
PLACE_NEAR=U0600.AH48:10MM

R2091 — 20 — 1% 1/20W TK 0201 — 118S00467
SPI_TCON_CLK_R (IN, 9) → SPI_TCON_CLK (OUT, 75 90)
PLACE_NEAR=U0600.AH49:10MM

E IMU Source Terminations

SENSOR_IMU
R2008 — 20 — 1% 1/20W TK 0201 — 118S00467
SPI_AOP_GYRO_MOSI_R (IN, 8) → SPI_AOP_GYRO_MOSI (OUT, 57)
PLACE_NEAR=U0600.V4:10MM

SENSOR_IMU
R2009 — 20 — 1% 1/20W TK 0201 — 118S00467
SPI_AOP_GYRO_CLK_R (IN, 8) → SPI_AOP_GYRO_CLK (OUT, 57)
PLACE_NEAR=U0600.U3:10MM

F SOC SWD Source Terminations

R2084 — 20 — 1% 1/20W TK 0201 — 118S00467
SWD_SOC_SWCLK_R (IN, 7) → SWD_SOC_SWCLK (OUT, 62)
PLACE_NEAR=U0600.AR2:10MM

R2085 — 20 — 1% 1/20W TK 0201 — 118S00467
SWD_SOC_SWDIO_R (IN, 7) → SWD_SOC_SWDIO (OUT, 62)
PLACE_NEAR=U0600.AP1:10MM

G SOC SPMI MPMU Source Terminations

R2060 — 33 — 1% 1/20W TK 0201 — 118S00377
SPMI_NUB_MPMU_CLK_R (IN, 8) → SPMI_NUB_MPMU_CLK (OUT, 41)
PLACE_NEAR=U0600.AT2:10MM

R2061 — 33 — 1% 1/20W TK 0201 — 118S00377
SPMI_NUB_MPMU_DATA_R (BI, 8) → SPMI_NUB_MPMU_DATA (BI, 41)
PLACE_NEAR=U0600.AT1:10MM

H SOC SPMI SPMU Source Terminations

R2062 — 33 — 1% 1/20W TK 0201 — 118S00377
SPMI_NUB_SPMU_CLK_R (IN, 8) → SPMI_NUB_SPMU_CLK (OUT, 35)
PLACE_NEAR=U0600.AM4:10MM

R2063 — 33 — 1% 1/20W TK 0201 — 118S00377
SPMI_NUB_SPMU_DATA_R (BI, 8) → SPMI_NUB_SPMU_DATA (BI, 35)
PLACE_NEAR=U0600.AL4:10MM

I PMU SWD Series R

R2072 — 15 — 1% 1/20W TK 0201 — 118S00465
SWD_NUB_PMU_SWCLK_R (IN, 8) → SWD_NUB_PMU_SWCLK
PLACE_NEAR=U0600.AM3:10MM

R2075 — 15 — 1% 1/20W TK 0201 — 118S00465
SWD_NUB_PMU_SWDIO_R (BI, 8) → SWD_NUB_PMU_SWDIO
PLACE_NEAR=U0600.AK3:10MM

R2070 — 49.9 — 1% 1/20W TK 0201 — 118S00309
SWD_NUB_PMU_SWCLK → SWD_NUB_SWCLK_SPMU (OUT, 96)
PLACE_NEAR=R2071.1:10MM

R2071 — 49.9 — 1% 1/20W TK 0201 — 118S00309
SWD_NUB_SWCLK_SPMU → SWD_NUB_SWCLK_MPMU (OUT, 96)
PLACE_NEAR=R2070.1:10MM

R2073 — 49.9 — 1% 1/20W TK 0201 — 118S00309
SWD_NUB_PMU_SWDIO → SWD_NUB_SWDIO_SPMU (BI, 96)
PLACE_NEAR=R2074.1:10MM

R2074 — 49.9 — 1% 1/20W TK 0201 — 118S00309
SWD_NUB_SWDIO_SPMU → SWD_NUB_SWDIO_MPMU (BI, 96)
PLACE_NEAR=R2073.1:10MM

J LAS Source Terminations

R2080 — 20 — 1% 1/20W TK 0201 — 118S00467
SPI_AOP_SENSORS_CLK_R (IN, 8) → SPI_AOP_SENSORS_CLK (OUT, 85)
PLACE_NEAR=U0600.AN7:10MM

R2081 — 20 — 1% 1/20W TK 0201 — 118S00467
SPI_AOP_SENSORS_MOSI_R (IN, 8) → SPI_AOP_SENSORS_MOSI (OUT, 85)
PLACE_NEAR=U0600.AM6:10MM

L TDM Source Terminations

R2010 — 20 — 1% 1/20W TK 0201 — 118S00467
TDM_SPKRAMP_L_BCLK_R (IN, 9) → TDM_SPKRAMP_L_BCLK (MAKE_BASE=TRUE) (82)
PLACE_NEAR=U0600.BD21:10MM

R2011 — 20 — 1% 1/20W TK 0201 — 118S00467
TDM_SPKRAMP_L_R2D_R (IN, 9) → TDM_SPKRAMP_L_R2D (MAKE_BASE=TRUE) (82)
PLACE_NEAR=U0600.BE21:10MM

R2012 — 20 — 1% 1/20W TK 0201 — 118S00467
TDM_SPKRAMP_L_FSYNC_R (IN, 9) → TDM_SPKRAMP_L_FSYNC (MAKE_BASE=TRUE) (82)
PLACE_NEAR=U0600.BD20:10MM

R2020 — 20 — 1% 1/20W TK 0201 — 118S00467
TDM_SPKRAMP_R_BCLK_R (IN, 9) → TDM_SPKRAMP_R_BCLK (MAKE_BASE=TRUE) (83)
PLACE_NEAR=U0600.BD18:10MM

R2021 — 20 — 1% 1/20W TK 0201 — 118S00467
TDM_SPKRAMP_R_R2D_R (IN, 9) → TDM_SPKRAMP_R_R2D (MAKE_BASE=TRUE) (83)
PLACE_NEAR=U0600.BD15:10MM

R2022 — 20 — 1% 1/20W TK 0201 — 118S00467
TDM_SPKRAMP_R_FSYNC_R (IN, 9) → TDM_SPKRAMP_R_FSYNC (MAKE_BASE=TRUE) (83)
PLACE_NEAR=U0600.BE15:10MM

R2030 — 20 — 1% 1/20W TK 0201 — 118S00467
TDM_CODEC_BCLK_R (IN, 9) → TDM_CODEC_BCLK (OUT, 85 90)
PLACE_NEAR=U0600.BF21:10MM

R2031 — 20 — 1% 1/20W TK 0201 — 118S00467
TDM_CODEC_R2D_R (IN, 9) → TDM_CODEC_R2D (OUT, 85)
PLACE_NEAR=U0600.BF17:10MM

R2032 — 20 — 1% 1/20W TK 0201 — 118S00467
TDM_CODEC_FSYNC_R (IN, 9) → TDM_CODEC_FSYNC (OUT, 85)
PLACE_NEAR=U0600.BF20:10MM

BOM_COST_GROUP=SOC

SYNC_DATE=09/28/2021

PAGE TITLE
PAGE_TITLE=SOC: SOURCE TERMS

Apple Inc.

DRAWING NUMBER 051-07020 | SIZE D
REVISION 6.0.0
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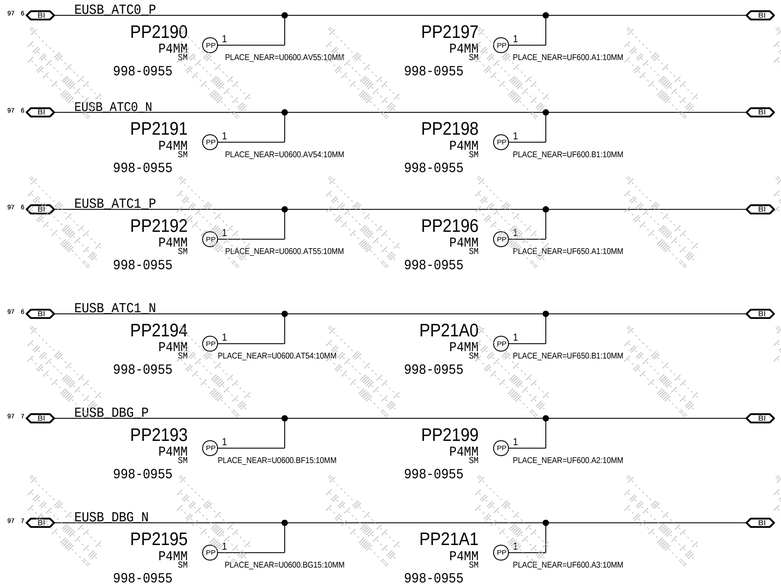
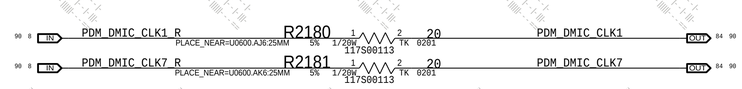
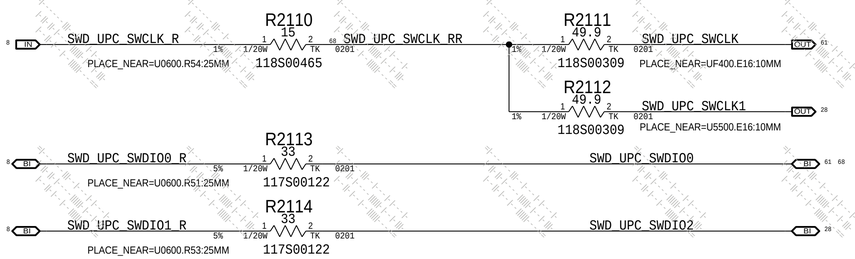
A EUSB Series Resistors & Test Points



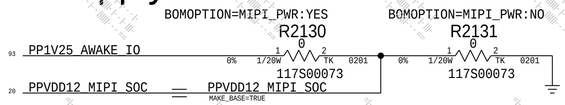
B DMIC Source Term



C UPC SWD Source Term

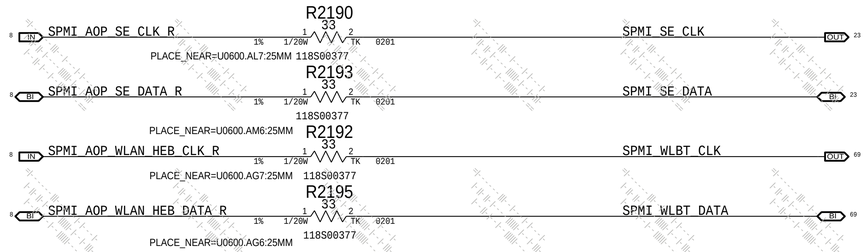


D MIPI PPVDD12 Supply Select

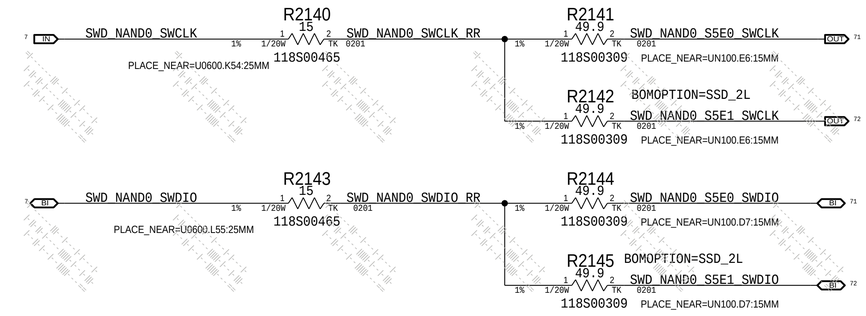


X2203 does not use the MIPI Interface on the SOC Interface
Per Moon Jung Kim (SEG Analog), VDD12_MIPIC and VDD12_MIPID can be tied to GND.

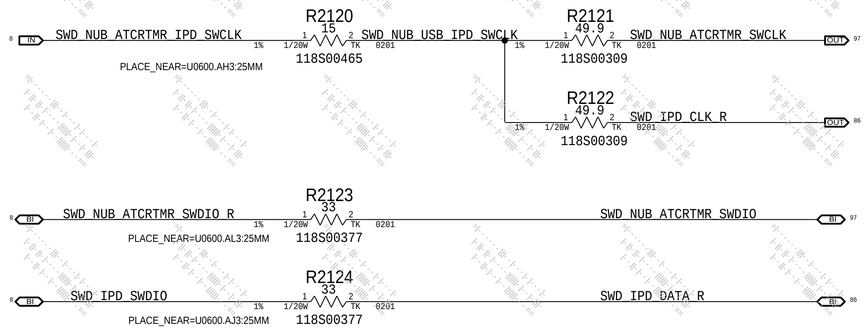
E Secure Element and WiFi SPMU Source Term



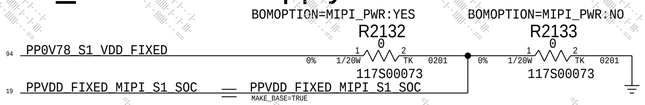
F NAND SWD Source Term



G IPD and ATC SWD Source Term

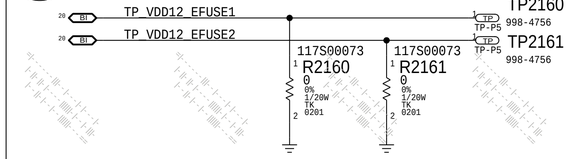


H MIPI PPVDD_FIXED S1 Supply Select



X2203 does not use the MIPI Interface on the SOC Interface
Per Moon Jung Kim (SEG Analog), VDD_FIXED_MIPIC_S1, VDD_FIXED_MIPID_PLL_S1, and VDD_FIXED_MIPID_S1 can be tied to GND.

I EFUSE Support



BOM_COST_GROUP=SOC

PAGE_TITLE=SOC: SOURCE TERMS

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SYNC_DATE=09/28/2021

DRAWING NUMBER	051-07020
SIZE	D
REVISION	6.0.0
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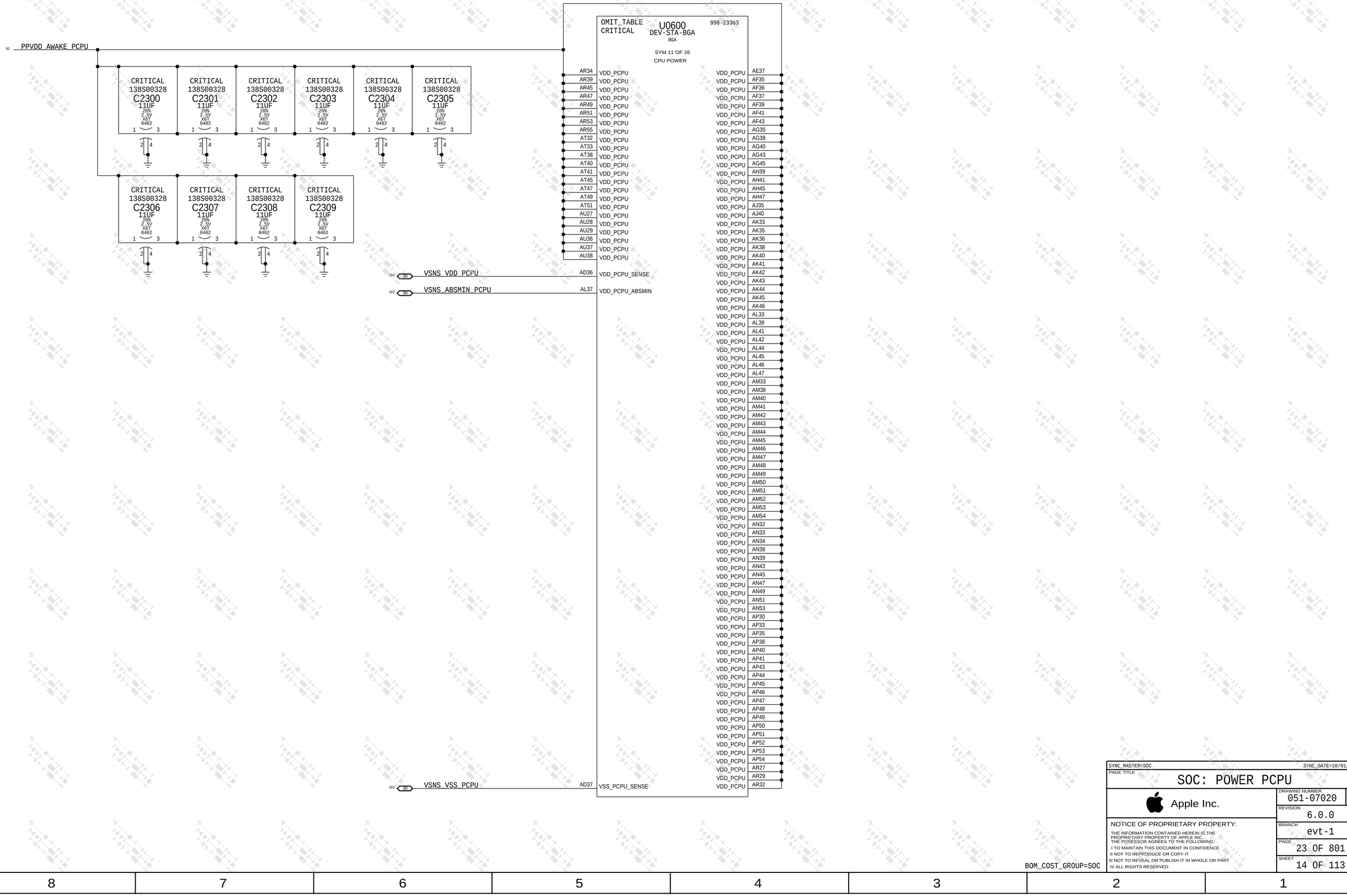
92 PPVDD_AWAKE_PCPU
CRITICAL 138S00328 C2300 11UF 20% 2.5V X6T 0402
CRITICAL 138S00328 C2301 11UF 20% 2.5V X6T 0402
CRITICAL 138S00328 C2302 11UF 20% 2.5V X6T 0402
CRITICAL 138S00328 C2303 11UF 20% 2.5V X6T 0402
CRITICAL 138S00328 C2304 11UF 20% 2.5V X6T 0402
CRITICAL 138S00328 C2305 11UF 20% 2.5V X6T 0402
CRITICAL 138S00328 C2306 11UF 20% 2.5V X6T 0402
CRITICAL 138S00328 C2307 11UF 20% 2.5V X6T 0402
CRITICAL 138S00328 C2308 11UF 20% 2.5V X6T 0402
CRITICAL 138S00328 C2309 11UF 20% 2.5V X6T 0402
OMIT_TABLE
CRITICAL
U0600
DEV-STA-BGA
BGA
998-23363
SYM 11 OF 26
CPU POWER
102 BI VSNS_VDD_PCPU
102 BI VSNS_ABSMIN_PCPU
102 BI VSNS_VSS_PCPU
AR34 AR39 AR45 AR47 AR49 AR51 AR53 AR55 AT32 AT33 AT38 AT40 AT41 AT45 AT47 AT49 AT51 AU27 AU28 AU29 AU36 AU37 AU38
VDD_PCPU
AD36 VDD_PCPU_SENSE
AL37 VDD_PCPU_ABSMIN
AD37 VSS_PCPU_SENSE
AE37 AF35 AF36 AF37 AF39 AF41 AF43 AG35 AG38 AG40 AG43 AG45 AH39 AH41 AH45 AH47 AJ35 AJ40 AK33 AK35 AK36 AK38 AK40 AK41 AK42 AK43 AK44 AK45 AK46 AL33 AL39 AL41 AL42 AL44 AL45 AL46 AL47 AM33 AM38 AM40 AM41 AM42 AM43 AM44 AM45 AM46 AM47 AM48 AM49 AM50 AM51 AM52 AM53 AM54 AN32 AN33 AN34 AN38 AN39 AN43 AN45 AN47 AN49 AN51 AN53 AP30 AP33 AP35 AP38 AP40 AP41 AP43 AP44 AP45 AP46 AP47 AP48 AP49 AP50 AP51 AP52 AP53 AP54 AR27 AR29 AR32
BOM_COST_GROUP=SOC
SYNC_MASTER=SOC
SYNC_DATE=10/01/2021
PAGE TITLE
SOC: POWER PCPU
Apple Inc.
DRAWING NUMBER 051-07020
SIZE D
REVISION 6.0.0
BRANCH evt-1
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SHEET 14 OF 113
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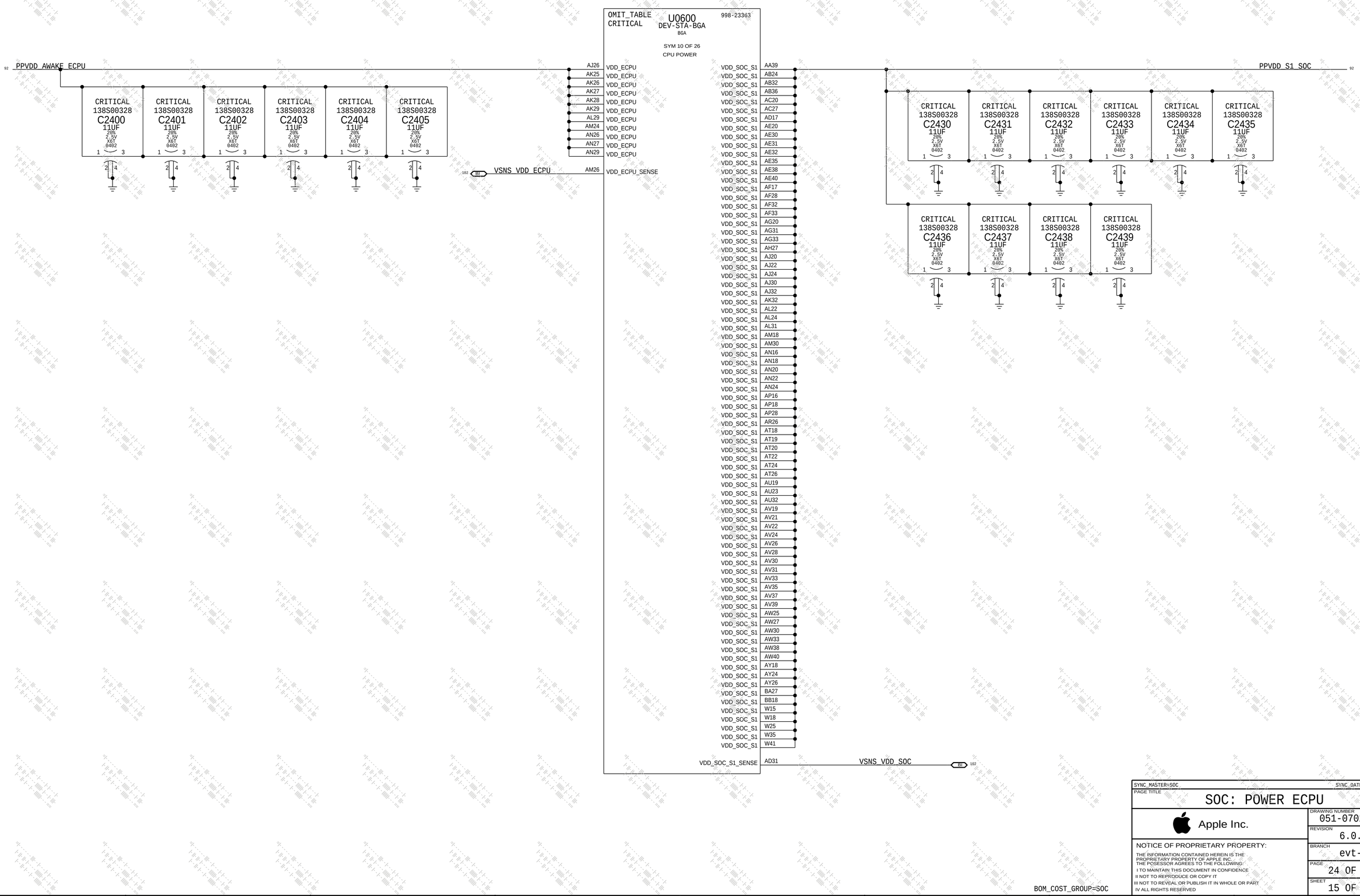
92 PPVDD_AWAKE_ECPU
CRITICAL 138S00328 C2400 11UF 20% 2.5V X6T 0402
CRITICAL 138S00328 C2401 11UF 20% 2.5V X6T 0402
CRITICAL 138S00328 C2402 11UF 20% 2.5V X6T 0402
CRITICAL 138S00328 C2403 11UF 20% 2.5V X6T 0402
CRITICAL 138S00328 C2404 11UF 20% 2.5V X6T 0402
CRITICAL 138S00328 C2405 11UF 20% 2.5V X6T 0402
102 BI VSNS_VDD_ECPU
OMIT_TABLE
CRITICAL
U0600
DEV-STA-BGA
998-23363
BGA
SYM 10 OF 26
CPU POWER
AJ26 VDD_ECPU
AK25 VDD_ECPU
AK26 VDD_ECPU
AK27 VDD_ECPU
AK28 VDD_ECPU
AK29 VDD_ECPU
AL29 VDD_ECPU
AM24 VDD_ECPU
AN26 VDD_ECPU
AN27 VDD_ECPU
AN29 VDD_ECPU
AM26 VDD_ECPU_SENSE
VDD_SOC_S1 AA39
VDD_SOC_S1 AB24
VDD_SOC_S1 AB32
VDD_SOC_S1 AB36
VDD_SOC_S1 AC20
VDD_SOC_S1 AC27
VDD_SOC_S1 AD17
VDD_SOC_S1 AE20
VDD_SOC_S1 AE30
VDD_SOC_S1 AE31
VDD_SOC_S1 AE32
VDD_SOC_S1 AE35
VDD_SOC_S1 AE38
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VDD_SOC_S1 AJ22
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VDD_SOC_S1 AJ30
VDD_SOC_S1 AJ32
VDD_SOC_S1 AK32
VDD_SOC_S1 AL22
VDD_SOC_S1 AL24
VDD_SOC_S1 AL31
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VDD_SOC_S1 AM30
VDD_SOC_S1 AN16
VDD_SOC_S1 AN18
VDD_SOC_S1 AN20
VDD_SOC_S1 AN22
VDD_SOC_S1 AN24
VDD_SOC_S1 AP16
VDD_SOC_S1 AP18
VDD_SOC_S1 AP28
VDD_SOC_S1 AR26
VDD_SOC_S1 AT18
VDD_SOC_S1 AT19
VDD_SOC_S1 AT20
VDD_SOC_S1 AT22
VDD_SOC_S1 AT24
VDD_SOC_S1 AT26
VDD_SOC_S1 AU19
VDD_SOC_S1 AU23
VDD_SOC_S1 AU32
VDD_SOC_S1 AV19
VDD_SOC_S1 AV21
VDD_SOC_S1 AV22
VDD_SOC_S1 AV24
VDD_SOC_S1 AV26
VDD_SOC_S1 AV28
VDD_SOC_S1 AV30
VDD_SOC_S1 AV31
VDD_SOC_S1 AV33
VDD_SOC_S1 AV35
VDD_SOC_S1 AV37
VDD_SOC_S1 AV39
VDD_SOC_S1 AW25
VDD_SOC_S1 AW27
VDD_SOC_S1 AW30
VDD_SOC_S1 AW33
VDD_SOC_S1 AW38
VDD_SOC_S1 AW40
VDD_SOC_S1 AY18
VDD_SOC_S1 AY24
VDD_SOC_S1 AY26
VDD_SOC_S1 BA27
VDD_SOC_S1 BB18
VDD_SOC_S1 W15
VDD_SOC_S1 W18
VDD_SOC_S1 W25
VDD_SOC_S1 W35
VDD_SOC_S1 W41
VDD_SOC_S1_SENSE AD31
VSNS_VDD_SOC BI 102
92 PPVDD_S1_SOC
CRITICAL 138S00328 C2430 11UF 20% 2.5V X6T 0402
CRITICAL 138S00328 C2431 11UF 20% 2.5V X6T 0402
CRITICAL 138S00328 C2432 11UF 20% 2.5V X6T 0402
CRITICAL 138S00328 C2433 11UF 20% 2.5V X6T 0402
CRITICAL 138S00328 C2434 11UF 20% 2.5V X6T 0402
CRITICAL 138S00328 C2435 11UF 20% 2.5V X6T 0402
CRITICAL 138S00328 C2436 11UF 20% 2.5V X6T 0402
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CRITICAL 138S00328 C2438 11UF 20% 2.5V X6T 0402
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Apple Inc.
DRAWING NUMBER 051-07020
SIZE D
REVISION 6.0.0
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PPVDD_AWAKE_CPU_SRAM
PPVDD_S1_DCS
PP0V779_S1_SRAM
VDD_DCS_S1_SENSE
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BGA
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998-23363
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VDD_DCS_S1: AA40 AD15 AE15 AH15 AJ15 U18 U26 U37 V20 V21 V24 V25 V27 V29 V30 V33 V34 V36 V38 Y41
VDD_DCS_S1_SENSE: AB40
VDD_SRAM_S1: AB17 AB20 AB26 AB28 AB30 AB35 AC21 AC40 AD20 AD24 AD28 AD30 AD35 AD39 AE33 AF18 AF20 AF22 AF26 AF30 AF34 AG28 AH17 AH19 AH21 AH23 AH25 AH29 AH31 AJ33 AK18 AK21 AK23 AK31 AL20 AM16 AM23 AN17 AN30 AP21 AP23 AR19 AR21 AR23 AR25 AU18 AU21 AU25 AU31 AV29 AV38 AV40 AW26 AW28 AW32 AW36 AY25 Y17 Y20 Y25 Y32 Y35 Y40

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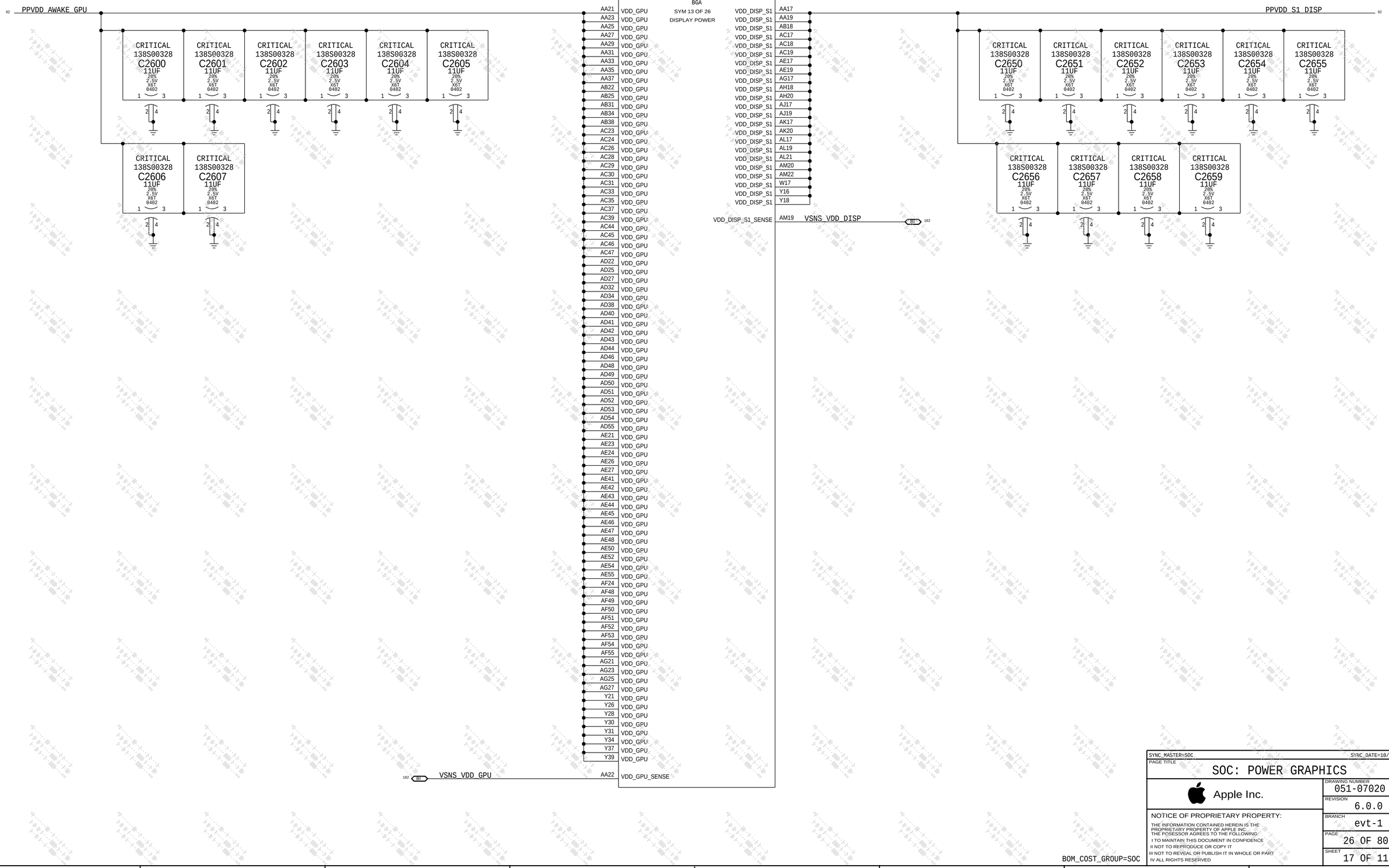
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VDD_GPU_SENSE
VSNS_VDD_GPU
182
BI
VDD_DISP_S1
VDD_DISP_S1_SENSE
AM19
VSNS_VDD_DISP
87
102
PPVDD_S1_DISP
92
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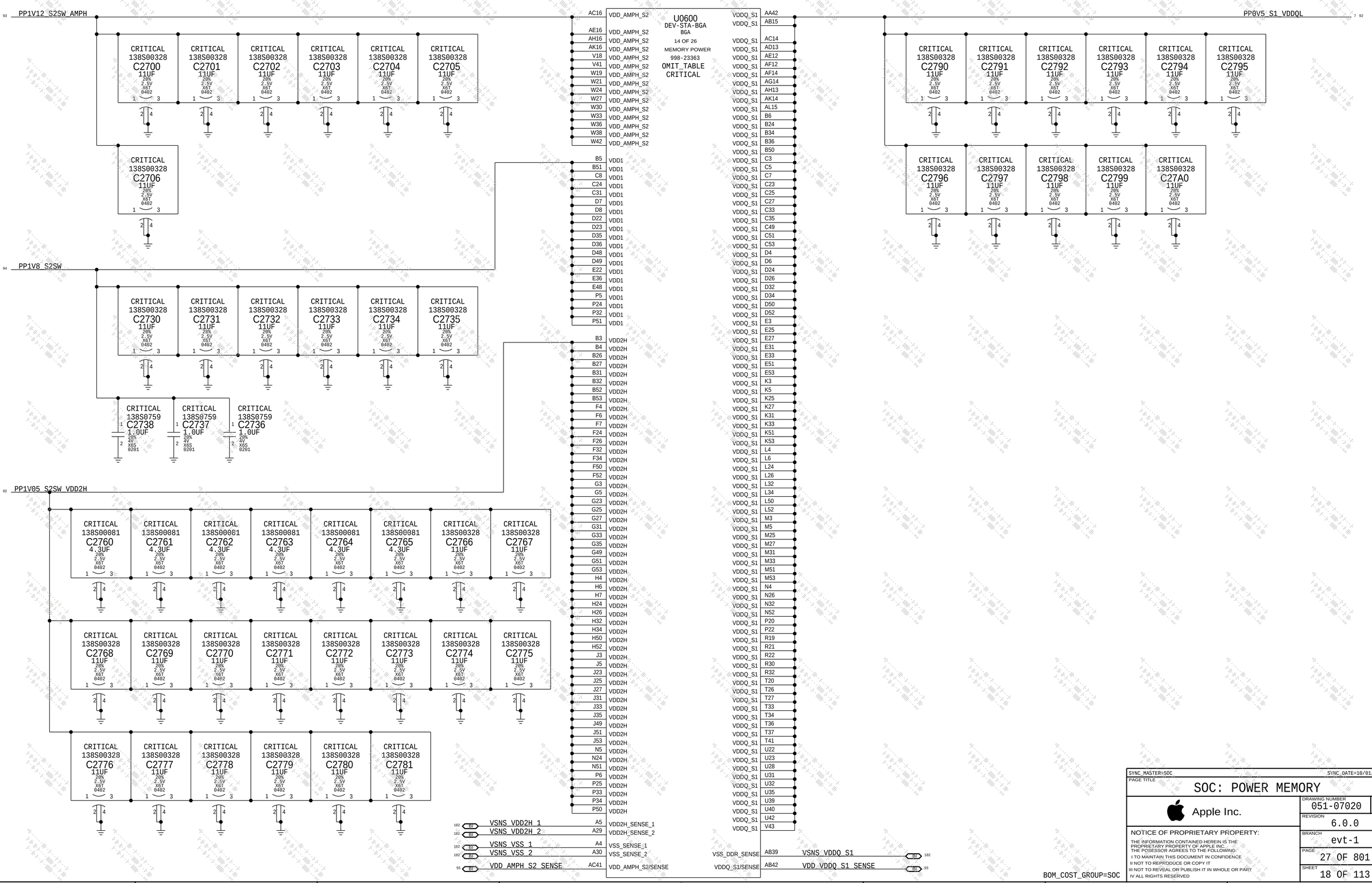
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92 PP1V05_S2SW_VDD2H
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CRITICAL 138S00328 C2701 11UF 20% 2.5V X6T 0402
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AH16 VDD_AMPH_S2
AK16 VDD_AMPH_S2
V18 VDD_AMPH_S2
V41 VDD_AMPH_S2
W19 VDD_AMPH_S2
W21 VDD_AMPH_S2
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W38 VDD_AMPH_S2
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B51 VDD1
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SIZE D
REVISION 6.0.0
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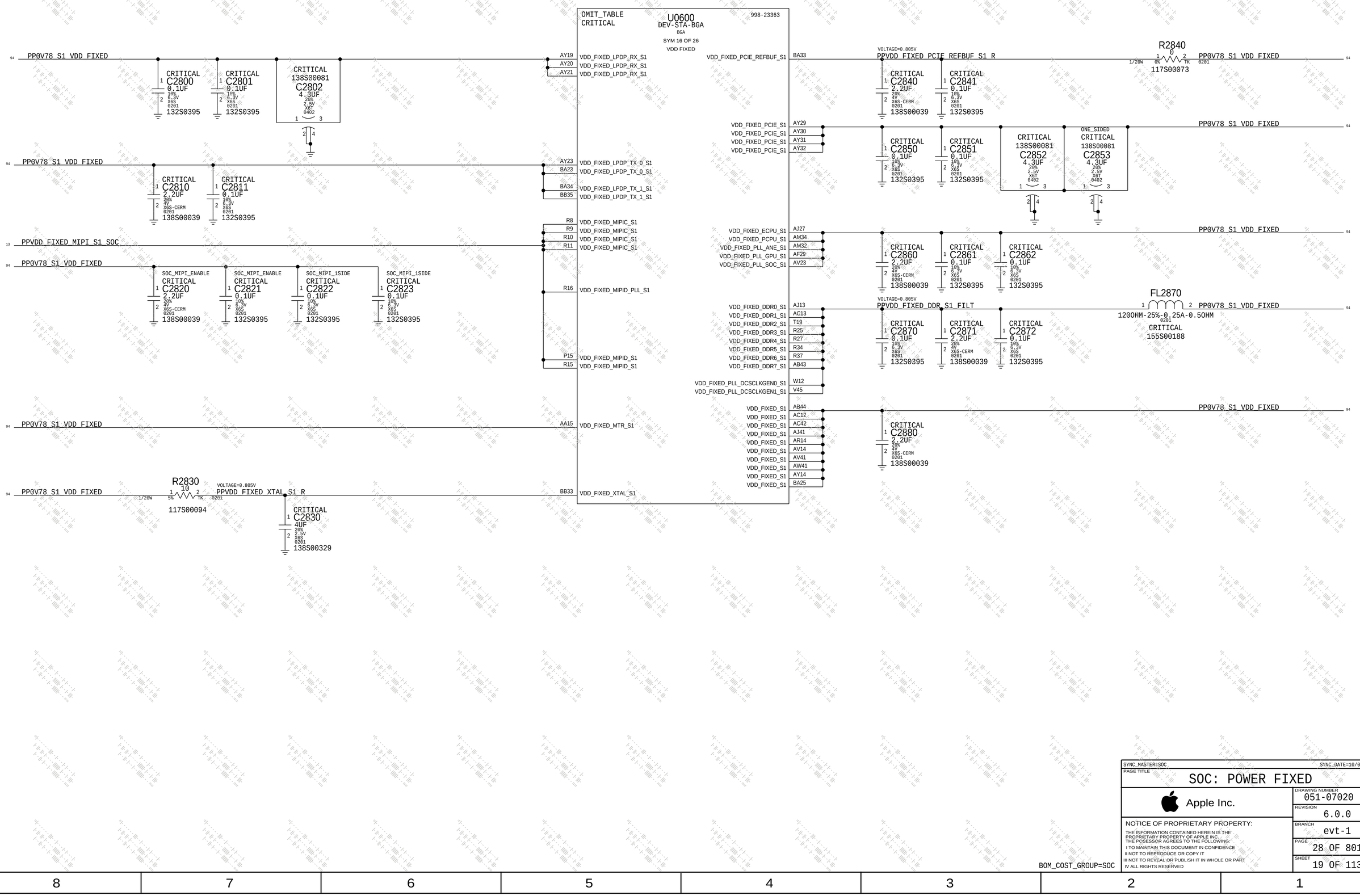
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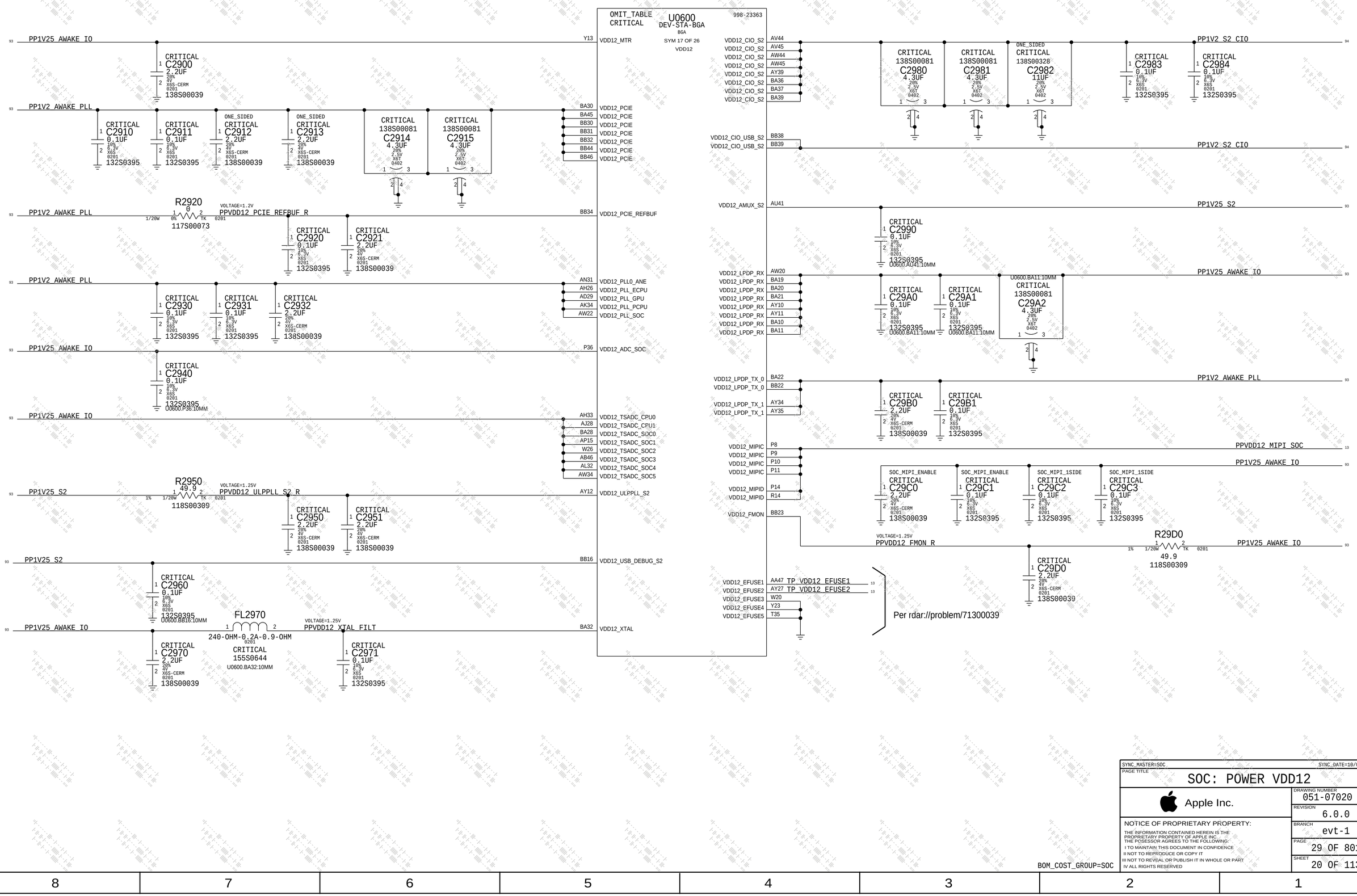
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PP1V2_AWAKE_PLL
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PP1V25_AWAKE_IO
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PP1V2_AWAKE_PLL
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PPVDD12_XTAL_FILT
PPVDD12_FMON_R
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BA45 VDD12_PCIE
BB30 VDD12_PCIE
BB31 VDD12_PCIE
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BB44 VDD12_PCIE
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AH26 VDD12_PLL_ECPU
AD29 VDD12_PLL_GPU
AK34 VDD12_PLL_PCPU
AW22 VDD12_PLL_SOC
P36 VDD12_ADC_SOC
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BA28 VDD12_TSADC_SOC0
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W26 VDD12_TSADC_SOC2
AB46 VDD12_TSADC_SOC3
AL32 VDD12_TSADC_SOC4
AW34 VDD12_TSADC_SOC5
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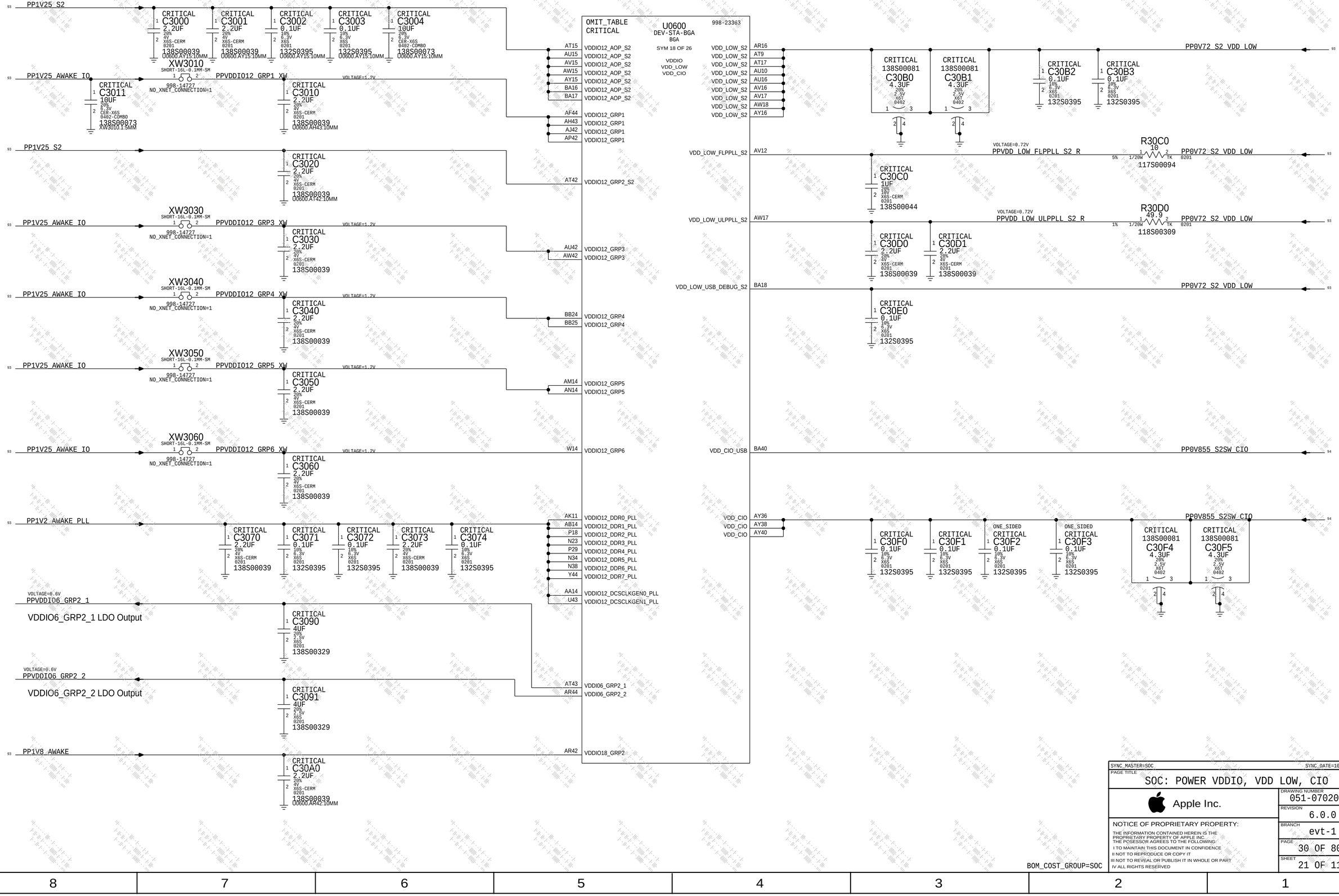
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VDD_CIO
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PP1V25_AWAKE_IO
PP1V2_AWAKE_PLL
PP1V8_AWAKE
PPVDDIO12_GRP1_XW
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PPVDDIO12_GRP6_XW
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998-14727
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XW3040
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XW3060
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AT15 VDDIO12_AOP_S2
AU15 VDDIO12_AOP_S2
AV15 VDDIO12_AOP_S2
AW15 VDDIO12_AOP_S2
AY15 VDDIO12_AOP_S2
BA16 VDDIO12_AOP_S2
BA17 VDDIO12_AOP_S2
AF44 VDDIO12_GRP1
AH43 VDDIO12_GRP1
AJ42 VDDIO12_GRP1
AP42 VDDIO12_GRP1
AT42 VDDIO12_GRP2_S2
AU42 VDDIO12_GRP3
AW42 VDDIO12_GRP3
BB24 VDDIO12_GRP4
BB25 VDDIO12_GRP4
AM14 VDDIO12_GRP5
AN14 VDDIO12_GRP5
W14 VDDIO12_GRP6
AK11 VDDIO12_DDR0_PLL
AB14 VDDIO12_DDR1_PLL
P18 VDDIO12_DDR2_PLL
N23 VDDIO12_DDR3_PLL
P29 VDDIO12_DDR4_PLL
N34 VDDIO12_DDR5_PLL
N38 VDDIO12_DDR6_PLL
Y44 VDDIO12_DDR7_PLL
AA14 VDDIO12_DCSCLKGEN0_PLL
U43 VDDIO12_DCSCLKGEN1_PLL
AT43 VDDI06_GRP2_1
AR44 VDDI06_GRP2_2
AR42 VDDIO18_GRP2
VDD_LOW_S2
AR16
AT9
AT17
AU10
AU16
AV16
AV17
AW18
AY16
VDD_LOW_FLPPLL_S2
AV12
VDD_LOW_ULPPLL_S2
AW17
VDD_LOW_USB_DEBUG_S2
BA18
VDD_CIO_USB
BA40
VDD_CIO
AY36
AY38
AY40
PP0V72_S2_VDD_LOW
PPVDD_LOW_FLPPLL_S2_R
PPVDD_LOW_ULPPLL_S2_R
PP0V855_S2SW_CIO
R30C0
10
117S00094
R30D0
49.9
118S00309
BOM_COST_GROUP=SOC
SYNC_MASTER=SOC
SYNC_DATE=10/01/2021
PAGE TITLE
SOC: POWER VDDIO, VDD LOW, CIO
Apple Inc.
DRAWING NUMBER
051-07020
SIZE
D
REVISION
6.0.0
BRANCH
evt-1
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SHEET
21 OF 113
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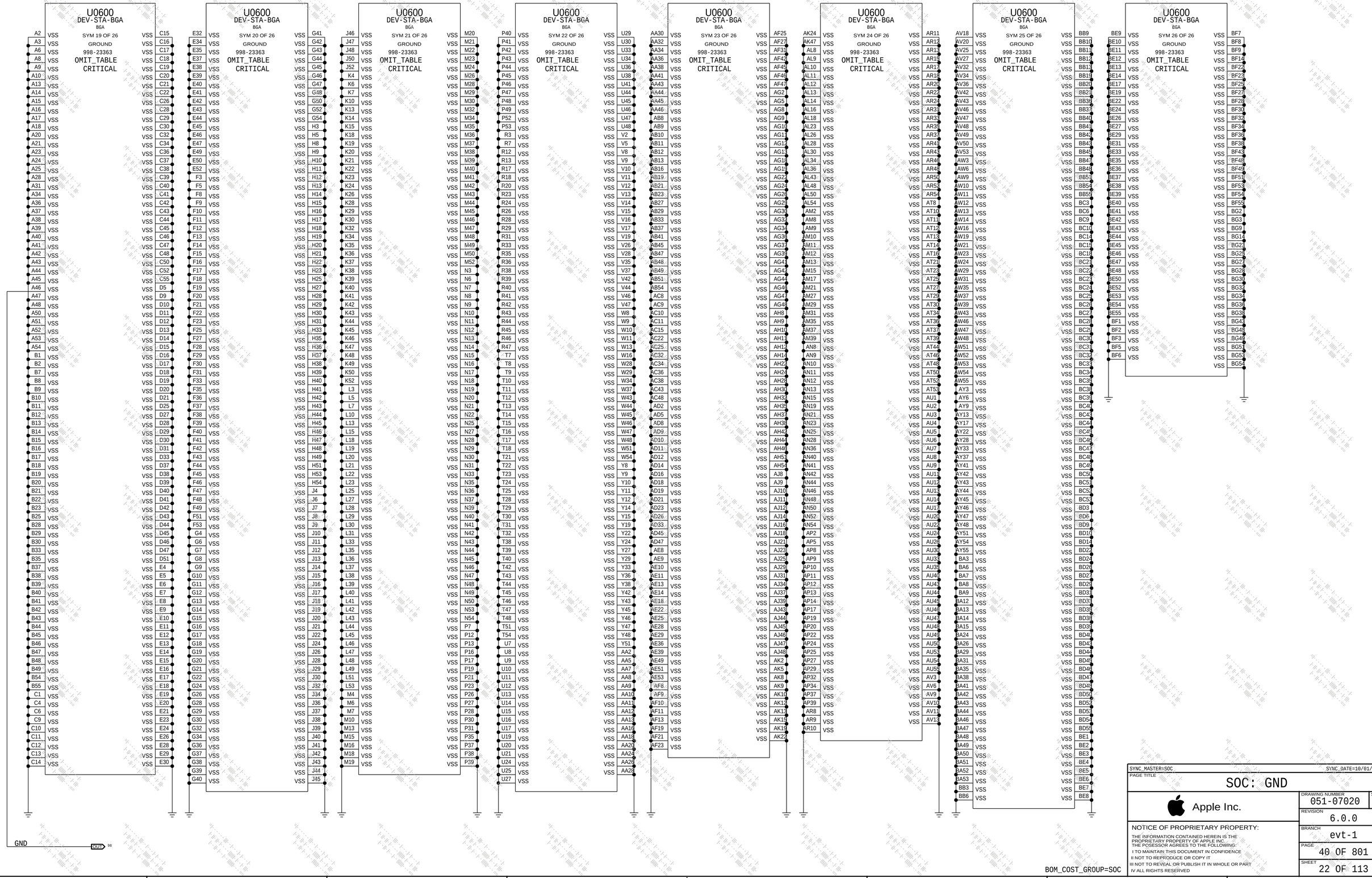

SYNC_MASTER=SOC SYNC_DATE=10/01/2021

PAGE TITLE

SOC: GND

Apple Inc.

DRAWING NUMBER 051-07020 SIZE D

REVISION 6.0.0

BRANCH evt-1

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SHEET 22 OF 113

BOM_COST_GROUP=SOC

Timing Requirements:
- VBAT supply ramp time: 20ms

Ceres - Secure Element

*** OK2INTEGRATE ***

Per TGA Power Block Diagram v0.3

92 PP1V8_S2
IccMax SE only: 125mA

U5000.F9:3mm C5014 1.0UF 20% 6.3V X5R 0201-1

U5000.F8:3mm C5002 0.22UF 20% 6.3V X5R 0201

U5000.E7:3mm C5003 0.22UF 20% 6.3V X5R 0201

PP1V25_S2 93
IccMax SE only: 10mA

Based on SPMI only use case

R5030 0 1/20W TK 0201 0%

VDDBOOST_SE

VUP_SE

VDDPLL_SE
VDDNV_SE
VDDC_SE

U5000.B5:3mm C5008 0.22UF 20% 6.3V X5R 0201

U5000.E8:3mm C5009 0.22UF 20% 6.3V X5R 0201

U5000.E9:3mm C5010 0.22UF 20% 6.3V X5R 0201

C5051 2.2UF 20% 10V X5R 0201

PP3V8_AON 23 92

IccMax: 100mA

As per NXP preliminary estimate, final pending

U5000
SN210VUK/B101V7
WLCSP
OMIT_TABLE

H9	PMUVCC1		
J9	PMUVCC2		
G8	SIMVCC1		
H8	SIMVCC2		
A8	VDDBOOST		
A9	VDDBOOST		
B4	VDDA		
E9	VDDC		
F9	VDDCIN		
F8	VDDIO		
E7	VDDIO_I2C		
J1	VDDIO_SE		
A5	VDDMIX		
E8	VDDNV		
B2	VDDPA		
B5	VDDPLL		
A2	VUP		
A7	VBAT		
D9	VBATPWR		
D4	NFC_CLK_32K		
H6	NFC_CLK_REQ		
A6	NFC_CLK_XTAL1		
23 SE_CTLR_FW_DWLD	G4	NFC_DWL_REQ	
96 NC_SE_GPIO0	F6	NFC_GPIO0	
NC	J7	NFC_GPIO1	
NC	J5	NFC_GPIO2_AO	
NC	H4	NFC_GPIO3_AO	
R5042 47K 1/20W TK 0201 5%	E6	NFC_HSU_CTS	
NC_UART_SE_D2R_CTS_L	F5	NFC_HSU_RTS	
R5041 47K 1/20W TK 0201 5%	G5	NFC_HSU_RX	
UART_SE_R2D	E5	NFC_HSU_TX	
NC	E4	NFC_I2C_SCL	
NC	F4	NFC_I2C_SDA	
NC	J6	NFC_IRQ	
NC	G9	NFC_SIM_SWIO1	
NC	J8	NFC_SIM_SWIO2	
13 IN SPMI_SE_CLK	H7	NFC_SPMI_SCLK	
13 BI SPMI_SE_DATA	G7	NFC_SPMI_SDATA	
23 SE_DEV_WAKE	H5	NFC_WKUP_REQ	
NC	B6	NFC_XTAL2	
	G6	TM	
	A3	RXP	
	A4	RXN	
	F7	VSS_DIG	
	J3	VSS_DIG	
	E1	VSS_DIG_2	
	J4	VSS_DIG_LN	
	C3	VSS_NFC	
	B1	VSS_PA	
	C4	VSS_PLL	
	D6	VSS_PMU	
	C8	VSS_PWR	
	C9	VSS_PWR	
	C6	VSS_REF	
	D8	VSS_SUB	
	E3	VSS_SUB	
	H3	SE_GPIO0	NC
	F3	SE_GPIO1	NC
	G1	SE_I2C_SCL	NC_I2C_SE_SCL
	H1	SE_I2C_SDA	NC_I2C_SE_SDA
	F2	SE_ISO_CLK	NC
	F1	SE_ISO_IO	NC
	G3	SE_ISO_RST	NC
	G2	SE_SPI_CLK	NC
	J2	SE_SPI_CS	NC
	H2	SE_SPI_MISO	NC
	E2	SE_SPI_MOSI	NC
	D2	TXVCASCP	NC
	D1	TXVCASCN	NC
	B3	RXVCM	NC
	C2	TXVCM	NC
	A1	TX1	NC
	C1	TX2	NC
	D7	VCASCHI	NC
	C7	VCASCLO	NC
	B8	BOOST_LX	PP3V8_AON
	B9	BOOST_LX	
	B7	VHV	VHV_SE
	D3	VTUNE	NC
	D5	VEN	SE_PWR_EN
	C5	VREF	VREF_SE

50K internal pull-down

Pulls to be added in system, can be NC'd if unused

96 IN NC_I2C_SE_SCL
96 BI NC_I2C_SE_SDA

R5050 1M 5% 1/20W TK 0201

R5051 1M 5% 1/20W TK 0201

C5004 0.1UF 10% 6.3V CERM-X5R 0201

C5017 0.22UF 20% 6.3V X5R 0201

R5000 47K 5% 1/20W TK 0201 — SE_CTLR_FW_DWLD 23
R5006 47K 5% 1/20W TK 0201 — SE_DEV_WAKE 23

<rdar://problem/52067756> [SN200V] Wired Mode SE Only Reference Design Material
<rdar://problem/45108950> Mac - Venus Reference guide and De-coupling requirements

BOM_COST_GROUP=SECURE ELEMENT

SYNC_MASTER=
SYNC_DATE=09/18/2021

PAGE TITLE: Secure Element

Apple Inc.

DRAWING NUMBER: 051-07020
SIZE: D
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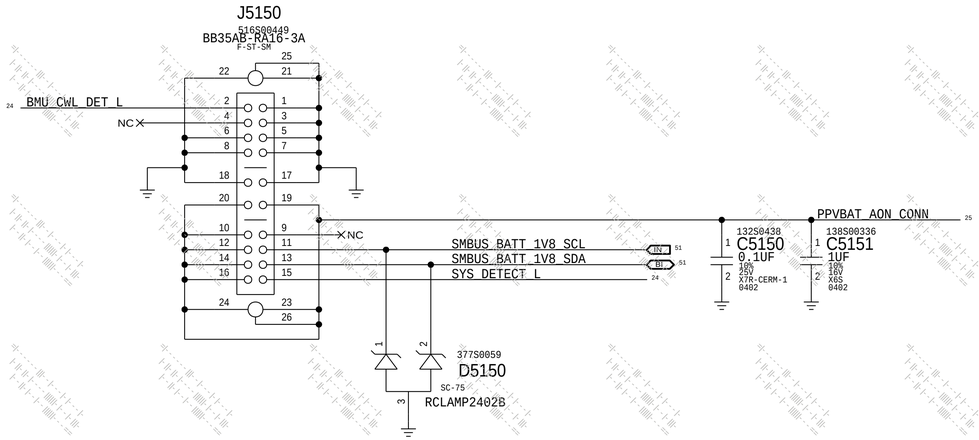
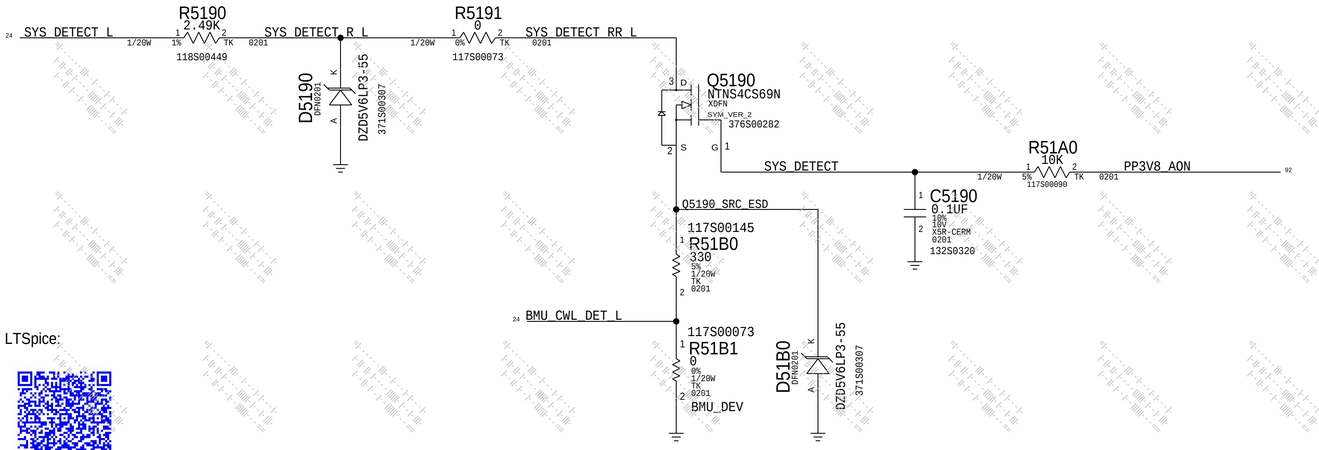
A BMU Connector



B BMU SYS_DETECT Circuit



LTSpice:

$X2203GHUB/mlb/sim/ltspice/bmu_sys_detect/bmu_sys_detect.asc

C BMU SYS_DETECT NOTES

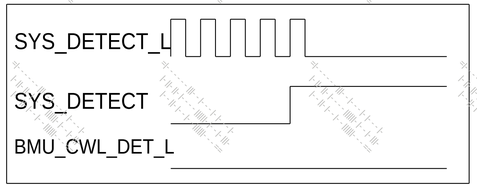
The BMU SYS_DETECT circuit relies on the system assembly in order to be properly enabled. During assembly, a metal gasket is placed between the cowling and the top-side of the BMU flex. The gasket is used to connect the BMU_CWL_DET_L signal, located between J5150.1 and Q5190.2, to GND. Once BMU_CWL_DET_L is tied to GND, then the SYS_DETECT circuit is ready to be enabled.

The BMU VBAT output will be enabled after the BMU flex and cowling are installed and power is supplied by connecting a power adapter to either the USB-C or MagSafe Connectors.

Thus the MLB remains in an unpowered state during system assembly.

Once the MLB is assembled into an enclosure, the BMU SYS_DETECT circuit output, SYS_DETECT_L, is continuously sampled by the Gas Gauge IC at a rate of once per second until it detects a logic low. During the once per second interval, an internal pull-up within the Gas Gauge IC is enabled for 4us to conserve battery charge. Once a logic low is detected, then the BMU enables the VBAT outptu voltage.

Below is an example waveform showing how the BMU SYS_DETECT circuit works.



In the event that the cowling needs to be removed while retaining power to the MLB, resistor R51B1 can be loaded.

BOM_COST_GROUP=BATTERY

PAGE TITLE: BMU Connector

Apple Inc.

DRAWING NUMBER: 051-07020 SIZE: D
REVISION: 6.0.0
BRANCH: evt-1
PAGE: 51 OF 801
SHEET: 24 OF 113

*** OK2INTEGRATE ***

PPDCIN_AON_CHGR_R
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1800

C520A 2.2UF 20% 35V X5R-CERM 0402-0.1MM 138S00030
C520B 2.2UF 20% 35V X5R-CERM 0402-0.1MM 138S00030
C520C 2.2UF 20% 35V X5R-CERM 0402-0.1MM 138S00030
C520D 2.2UF 20% 35V X5R-CERM 0402-0.1MM 138S00030
PACK_IGNORE=TRUE
PACK_OPTION=CHGR_MLCC-STD

CRITICAL C520A 2.2UF 20% 35V X5R 0402-4 138S00409
CRITICAL C520B 2.2UF 20% 35V X5R 0402-4 138S00409
CRITICAL C520C 2.2UF 20% 35V X5R 0402-4 138S00409
CRITICAL C520D 2.2UF 20% 35V X5R 0402-4 138S00409
PACK_OPTION=CHGR_MLCC-LN

CRITICAL C5202 6.8UF 20% 35V-0.090OHM POLY-TANT CASE-B1-B3-COMBO CAPMAT=POLY-TANT
CRITICAL C5203 6.8UF 20% 35V-0.090OHM POLY-TANT CASE-B1-B3-COMBO CAPMAT=POLY-TANT
CRITICAL C5204 6.8UF 20% 35V-0.090OHM POLY-TANT CASE-B1-B3-COMBO CAPMAT=POLY-TANT
CRITICAL C5205 6.8UF 20% 35V-0.090OHM POLY-TANT CASE-B1-B3-COMBO CAPMAT=POLY-TANT
CRITICAL C5206 6.8UF 20% 35V-0.090OHM POLY-TANT CASE-B1-B3-COMBO CAPMAT=POLY-TANT
PACK_OPTION=CHGR_72W

FROM USB-C SOURCE

92 29 25 PPDCIN_AON_CHGR

CRITICAL C5201 6.8UF 20% 35V-0.090OHM POLY-TANT CASE-B1-B3-COMBO CAPMAT=POLY-TANT

CRITICAL R5220 0.01 0.5% 1W MF 0612-1-COMBO

107S00044 NO_XNET_CONNECTION=1 (AMON) 2-CELL: 0.02 OHM 3-CELL: 0.01 OHM

CHGR_CSI_P
CHGR_CSI_N
PLACE_NEAR=U5200.D5:2MM
PLACE_NEAR=U5200.C5:2MM
R5221 1 1% 1/20W TK 0201
R5222 1 1% 1/20W TK 0201
CHGR_CSI_FILT_P
CHGR_CSI_FILT_N
CRITICAL C5221 0.1UF 10% 50V CERM-X7R 0402
CRITICAL C5222 0.047UF 10% 50V CER-X7R 0402
CRITICAL C5220 0.47UF 20% 4V CERM-X5R-1 201
NO_XNET_CONNECTION=1

CHGR_PHASE1 25
NOSTUFF R5235 1.5 5% 1/16W TK 0402 116S00026
CHGR_SNB1 DIDT=TRUE SWITCH_NODE=TRUE
NOSTUFF C5235 150PF 5% 50V C0G-CERM 0402 131S0514

CHGR_PHASE2 25
NOSTUFF R5245 1.5 5% 1/16W TK 0402 116S00026
CHGR_SNB2 DIDT=TRUE SWITCH_NODE=TRUE
NOSTUFF C5245 150PF 5% 50V C0G-CERM 0402 131S0514

CRITICAL L5230 1.4UH-20%-12A-0.0108OHM PIRR071G-SM 152S01459
CHGR_PHASE1_1
CRITICAL L5240 1.4UH-20%-12A-0.0108OHM PIRR071G-SM 152S01459

CHGR_PHASE1 25 DIDT=TRUE SWITCH_NODE=TRUE
CHGR_PHASE2 25 DIDT=TRUE SWITCH_NODE=TRUE

Q5230 NTTFD4D1N03P1E WDFN8
Q5240 NTTFD4D1N03P1E WDFN8
CRITICAL

CHGR_GATE_Q1_R DIDT=TRUE SWITCH_NODE=TRUE
CHGR_GATE_Q2_R DIDT=TRUE GATE_NODE=TRUE
CHGR_GATE_Q3_R DIDT=TRUE GATE_NODE=TRUE
CHGR_GATE_Q4_R DIDT=TRUE SWITCH_NODE=TRUE
R5251 0 5% 1/16W MF 0402-1 116S00044
R5252 0 5% 1/16W MF 0402-1 116S00044
R5253 0 5% 1/16W MF 0402-1 116S00044
R5254 0 5% 1/16W MF 0402-1 116S00044
CHGR_GATE_Q1 DIDT=TRUE SWITCH_NODE=TRUE
CHGR_GATE_Q2 DIDT=TRUE GATE_NODE=TRUE
CHGR_GATE_Q3 DIDT=TRUE GATE_NODE=TRUE
CHGR_GATE_Q4 DIDT=TRUE SWITCH_NODE=TRUE

CHGR_LX1 DIDT=TRUE SWITCH_NODE=TRUE
XW5230 SM
CRITICAL C5230 0.1UF 10% 25V X7R-CERM-1 0402
CHGR_BOOT1_RC DIDT=TRUE SWITCH_NODE=TRUE
R5230 0 5% 1/16W MF 0402-1 116S00044
CHGR_BOOT1 DIDT=TRUE SWITCH_NODE=TRUE

CHGR_LX2 DIDT=TRUE SWITCH_NODE=TRUE
XW5240 SM
CRITICAL C5240 0.1UF 10% 25V X7R-CERM-1 0402
CHGR_BOOT2_RC DIDT=TRUE SWITCH_NODE=TRUE
R5240 0 5% 1/16W MF 0402-1 116S00044
CHGR_BOOT2 DIDT=TRUE SWITCH_NODE=TRUE

PPVBAT_AON_CHGR_REG 25
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

CRITICAL C5256 2.2UF 20% 35V X6S-CERM 0402 138S00042
CRITICAL C5257 2.2UF 20% 35V X6S-CERM 0402 138S00042
CRITICAL C5256 2.2UF 20% 25V X6S 0402-1 138S00410
CRITICAL C5257 2.2UF 20% 25V X6S 0402-1 138S00410
CRITICAL C5258 1000PF 10% 100V X7R 0201
PACK_IGNORE=TRUE
PACK_OPTION=CHGR_MLCC-STD
PACK_OPTION=CHGR_MLCC-LN

CAPGEARATE CRITICAL C5252 33UF 20% 16V TANT CASE-T 128S00009
CAPGEARATE CRITICAL C5253 33UF 20% 16V TANT CASE-T 128S00009
CAPGEARATE CRITICAL C5254 33UF 20% 16V TANT CASE-T 128S00009
CAPGEARATE CRITICAL C5255 33UF 20% 16V TANT CASE-T 128S00009
CAPGEARATE CRITICAL C5282 33UF 20% 16V TANT CASE-T 128S00009
CAPGEARATE CRITICAL C5283 33UF 20% 16V TANT CASE-T 128S00009
CAPGEARATE CRITICAL C5284 33UF 20% 16V TANT CASE-T 128S00009
CAPGEARATE CRITICAL C5285 33UF 20% 16V TANT CASE-T 128S00009
PACK_IGNORE=TRUE
PACK_OPTION=CHGR_PBUS16V

CAPGEARATE CRITICAL C5252 27UF 20% 18V TANT-POLY CASE-B12 128S00107
CAPGEARATE CRITICAL C5253 27UF 20% 18V TANT-POLY CASE-B12 128S00107
CAPGEARATE CRITICAL C5254 27UF 20% 18V TANT-POLY CASE-B12 128S00107
CAPGEARATE CRITICAL C5255 27UF 20% 18V TANT-POLY CASE-B12 128S00107
CAPGEARATE CRITICAL C5282 27UF 20% 18V TANT-POLY CASE-B12 128S00107
CAPGEARATE CRITICAL C5283 27UF 20% 18V TANT-POLY CASE-B12 128S00107
CAPGEARATE CRITICAL C5284 27UF 20% 18V TANT-POLY CASE-B12 128S00107
CAPGEARATE CRITICAL C5285 27UF 20% 18V TANT-POLY CASE-B12 128S00107
PACK_OPTION=CHGR_PBUS18V

PPVBAT_AON_CHGR_REG 25
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

CRITICAL F5200 12A-32V-0.00450HM 1206
TO SYSTEM
PPBUS_AON 92

PPVBAT_AON_CHGR_R
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500

CRITICAL C5265 2.2UF 20% 25V X6S-CERM 0402 138S00042
CRITICAL C5266 2.2UF 20% 25V X6S-CERM 0402 138S00042
CRITICAL C5265 2.2UF 20% 25V X6S 0402-1 138S00410
CRITICAL C5266 2.2UF 20% 25V X6S 0402-1 138S00410
CRITICAL C5267 0.1UF 10% 25V X5R 0201
CRITICAL C5268 0.01UF 10% 25V X5R-CERM 0201
PACK_IGNORE=TRUE
PACK_OPTION=CHGR_MLCC-STD
PACK_OPTION=CHGR_MLCC-LN

NO_XNET_CONNECTION=1
CRITICAL R5260 0.005 (PMON) 1% 1W MF 0612-8 107S00087
3-CELL: 0.010 OHM
5-CELL: 0.005 OHM

CRITICAL Q5265 SI7655DN-COMBO PWRPK-1212-8 SYM-VER-2

TO/FROM BATTERY
PPVBAT_AON_CONN 24
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500

C5269 0.1UF 10% 25V X5R 0201
C5264 1000PF 10% 25V X7R 0201
C5263 4700PF 10% 25V CER-X5R 0201

PPVBAT_AON_CHGR_REG 25
CRITICAL C5278 2.2UF 20% 25V X6S-CERM 0402 138S00042
CRITICAL C5278 2.2UF 20% 25V X6S 0402-1 138S00410
PACK_OPTION=CHGR_MLCC-LN
PACK_IGNORE=TRUE
PACK_OPTION=CHGR_MLCC-STD

PPCHGR_VDDA
PPCHGR_VDDP
R5275 4.7 5% 1/20W TK 0201
R5276 1 5% 1/20W TK 0201
CRITICAL C5275 2.2UF 20% 25V X5R-CERM 0402-1
CRITICAL C5277 10UF 20% 25V X5R-CERM 0603

PPDCIN_AON_CHGR 92 29 25
R5215 787K 1% 1/20W TK 0201
CRITICAL 376S1112 Q5216 DMN5L06TK SOT523 SYM_VER_2
<RDAR://68945820>
MAGSAFE: ACE GPIO6
USBC: ACE GPIO5
NOSTUFF C5216 0.01UF 10% 25V X5R-CERM 0201
R5216 158K 1% 1/20W TK 0201
CHGR_AUX_DET
68 IN CHGR_AUX_DET_SHORT_3V3
R5217 10K 5% 1/20W TK 0201 117S00090
92 26 C5280 1.0UF 20% 6.3V X5R 0201-1

U5200 RAA489900 WLCSP

B5	P_IN	GATE_Q1	H1
C5	CSIN	BOOT1	F1
D5	CSIP	LX1	G1
A5	PBUS_PWR	GATE_Q2	E1
D3	AUX_DET	GATE_Q3	D1
		LX2	B1
		BOOT2	C1
		GATE_Q4	A1
		PBUS_Q4SNS	A3
		CSOP	A4
		CSON	B4
		BGATE	B3
		VBAT	C3
		EN_VR1	F2
		SMC_RST*	H4
		IRQ_L	H3
		CBC_ON	H2
		(5V) EN_MVR	F4
		(OD) AUX_OK	F3
		AMON	D4
		BMON	C4
F5	VDDIO1P8		
G5	SDA		
H5	SCL		
G2	SMC_RST_IN		
G3	HPWR_EN*		
E5	COMP		
G4	CELL		
B2	NC0		
C2	NC1		
E4	NC2		
E3	AGND		
E2	PGND		

CRITICAL 376S1112 Q5216 DMN5L06TK SOT523 SYM_VER_2
OMIT_TABLE
SCH SYMBOL 353S02432

PP1V8_S2
51 IN SMBUS_CHGR_1V8_SDA
51 IN SMBUS_CHGR_1V8_SCL
43 IN CHGR_RST_IN

CHGR_COMP
CRITICAL C5270 0.12UF 10% 10V X5R 0402
CRITICAL C5271 0.12UF 10% 10V X5R 0402

CHGR_CSO_P
CHGR_CSO_N
PLACE_NEAR=U5200.A4:2MM
PLACE_NEAR=U5200.B4:2MM
R5261 1 1% 1/20W TK 0201
R5262 1 1% 1/20W TK 0201
CHGR_CSO_FILT_P
CHGR_CSO_FILT_N
CRITICAL C5261 0.047UF 10% 50V CER-X7R 0402
CRITICAL C5262 0.047UF 10% 50V CER-X7R 0402
CRITICAL C5260 0.47UF 20% 4V CERM-X5R-1 201
NO_XNET_CONNECTION=1

XW5260 SM
PLACE_NEAR=Q5240.3:2MM

XW5263 SM
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

CHGR_VBAT_XW
R5263 1K 5% 1/20W TK 0201-1

CRITICAL Q5270 <rdar://37259372&39763505>
NTNS4CS69N XDFN SYM_VER_1
SAVE_BAT_S
R5270 24K 5% 1/20W TK 0201
SAVE_BAT_G
CRITICAL D5270 DFN0201 ALLOW_APPLE_PREFIX=D DZD5V6LP3-55
PPDCIN_AON_CHGR 25 29 92
R5271 200K 1% 1/20W TK 0201

CHGR_BGATE
CHGR_VBAT
NC_CHGR_EN_VR1 96
NC_CHGR_SMC_RST_L 96
CHGR_INT_1V8_L OUT 26
NC_CHGR_CBC_ON 96
CHGR_EN_MVR OUT 26
CHGR_AUX_OK OUT 26
CHGR_AMON OUT 52
CHGR_BMON OUT 52
CHGR_PBUS_SNS MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000

ID REGISTER 0XFF => 0X000D

BOM_COST_GROUP=BATTERY

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02633	1	RAA489900,PMIC,WHAMOLA,OTP-2,WCSP40	U5200	CRITICAL	WHAMOLA:0A5
353S02990	1	RAA489900,PMIC,WHAMOLA,OTP-6,WCSP40	U5200	CRITICAL	WHAMOLA:0A5-13V7

SYNC_MASTER=Charger SYNC_DATE=09/10/2021

PAGE TITLE
PBUS SUPPLY & BATTERY CHARGER

Apple Inc.

DRAWING NUMBER 051-07020
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BRANCH evt-1
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SHEET 25 OF 113

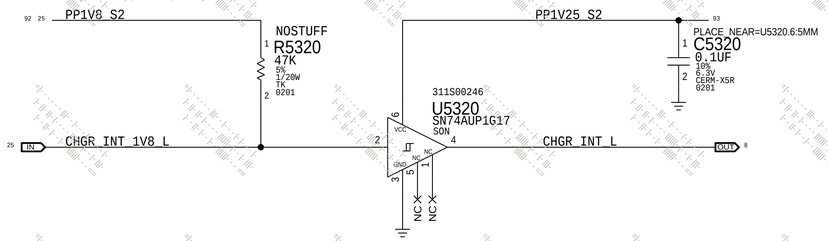
*** OK2INTEGRATE ***

CHGR I2C Level Translation

SMBUS_CHGR_1V8_[SCL/SDA]: Level translation circuit to be placed in project specific I2C page.

CHGR_INT_L Level Translation

Stuff R5320 in case, glitch during power sequencing is a concern.

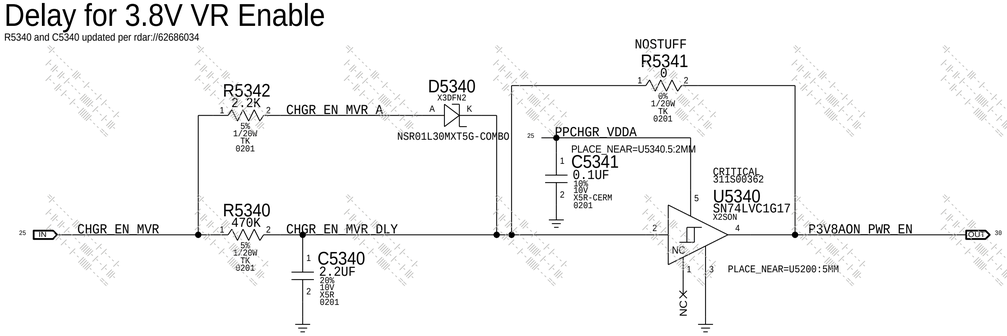


CHGR_AUX_OK Pull Up

Pull up to MPMU LDO9, or rely on MPMU internal pull up.
OK, to completely remove pull up , but consult PMU architecture and check OTP before that

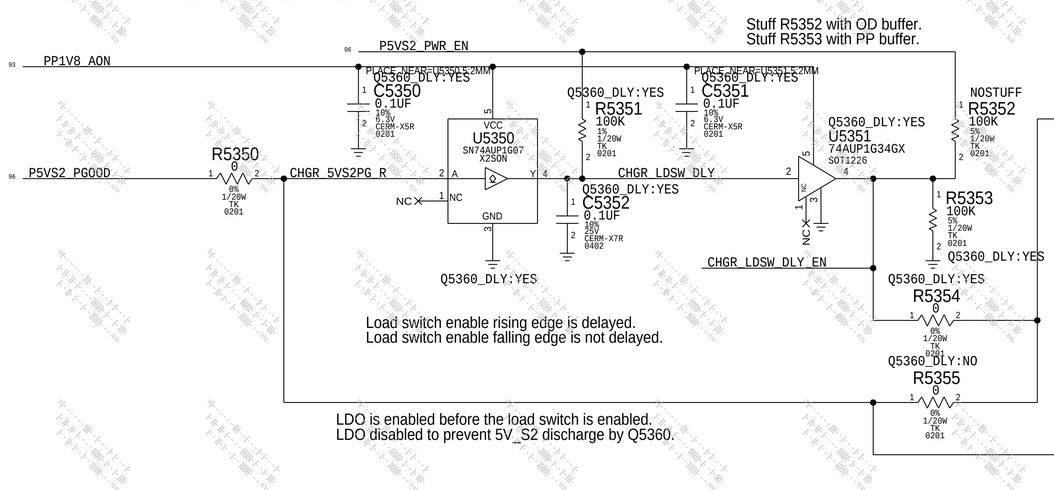
Delay for 3.8V VR Enable

R5340 and C5340 updated per rdar://62686034



Probe points - bottom

SWITCHOVER TO EXTERNAL 5V



BOM_COST_GROUP=BATTERY

SYNC_MASTER=Charger SYNC_DATE=03/10/2021

PAGE TITLE: BATTERY CHARGER SUPPORT

Apple Inc.

DRAWING NUMBER: 051-07020 SIZE: D
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BRANCH: evt-1
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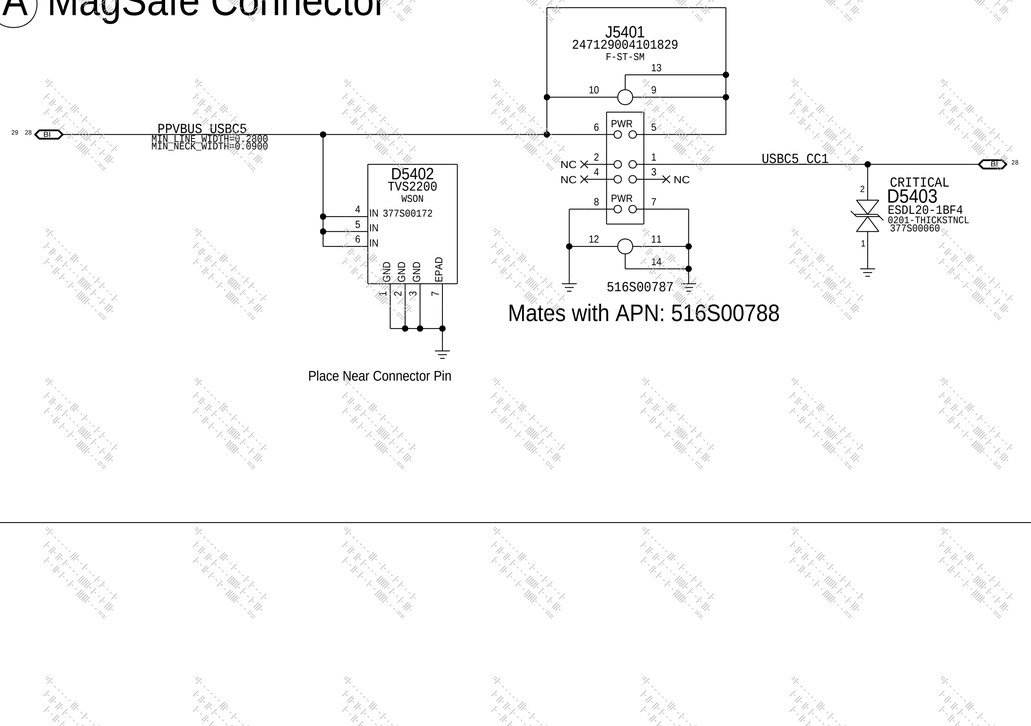
A MagSafe Connector



Mates with APN: 516S00788

Place Near Connector Pin

BOM_COST_GROUP=MAGSAFE

PAGE TITLE	MAGSAFE: CONNECTOR
Apple Inc.	DRAWING NUMBER 051-07020 · SIZE D
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Either a Testpoint or Arkanoid connector
must be present for GPIO0
(EVEN IN PRODUCTION)

PPHV_INT5_AONSW
R5502 1K PD_ACE5_VCONN
PD_ACE5_VCONN
PD_ACE5_VCONN

MAX 100uF TOTAL ON RAIL

PP3V3_UPC5_LDO

R5506 100K
R5507 10K UPC5_GPIO2
R5534 100K
R5531 100K
R5573 100K
R5572 100K
R5574 100K
R5575 100K

NC_UPC5_RESET_L
PD_UPC5_MRESET
NC_UPC5_RESET_L
UPC5_SER_DBG
UPC5_GPIO1
UPC5_GPIO2
UPC5_GPIO3
UPC5_GPIO4
UPC5_GPIO5
UPC5_GPIO6
UPC5_GPIO7
UPC5_GPIO8
UPC5_GPIO9
UPC5_GPIO10

ACE_WILL_BE_OTPED:NO
84.5K R5550 UPC5_I2C_ADDR
GND
UPC5_I2C_ADDR
UPC5_R_OSC

R5503 15K CRITICAL
I2C_UPC5_SDA
I2C_UPC5_SCL

ACE_WILL_BE_OTPED:NO
R5510 1M I2C_UPC5_SDA
ACE_WILL_BE_OTPED:YES
R5508 1M I2C_UPC5_SDA CKPLUS_WAIVE=I2C_PULLUP

R5509 1M I2C_UPC5_SCL CKPLUS_WAIVE=I2C_PULLUP

I2C_UPC_SDA
I2C_UPC_SCL
UPC_I2C_INT_L
I2C_SMC_UPC_SDA
I2C_SMC_UPC_SCL
UPC_SMC_I2C_INT_L

SPI_UPC5_R_CLK
SPI_UPC5_R_MOSI
SPI_UPC5_R_MISO
SPI_UPC5_R_CS_L

SWD_UPC_SWDIO2
SWD_UPC_SWCLK1
R5505 1M UART_UPC5
UART_UPC5

PD_UPC5_USB_RP
R5577 100K
PD_UPC5_USB_RP
PD_UPC5_PORT_MUX
PD_UPC5_PORT_MUX

ROM_UPC5_WP_L
R5578 100K
PD_UPC5_DBG_R
R5576 100K
PD_UPC5_DBG_R
ROM_UPC5_WP_L

U5500
CD3217B12GACER
FCBGA

CRITICAL
OMIT_TABLE

HRESET
MRESET
RESET*
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
BUSPOWER
I2C_ADDR IPU-BOOT
R_OSC
I2CM_SDA_CNFG
I2CM_SCL_CNFG
I2C_SDA1
I2C_SCL1
I2C_IRQ1*
I2C_SDA2
I2C_SCL2
I2C_IRQ2*
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_SSZ
SWD_DATA IPU
SWD_CLK IPU
UART_RX
UART_TX
USB_RP1_P
USB_RP1_N
USB_RP2_P
USB_RP2_N
USB_RP3_P
USB_RP3_N
AUX_P
AUX_N
HPD
DEBUG0
DEBUG1
DEBUG2
DEBUG3
DEBUG4
DEBUG5
DEBUG6
DEBUG7

DIGITAL CORE I/O & CONTROL
PORT_MUX
TYPE-C
GND
POWER

PP_5V0
PP_CABLE
PP_HV
VBUS

PPVBUS_USBC5

PLACE_NEAR=U5500.G6:5MM
C5521 2200PF 10% 25V CER-X7R 0201
PLACE_NEAR=U5500.H5:5MM
C5522 2200PF 10% 25V CER-X7R 0201
PLACE_NEAR=U5500.J6:5MM
C5523 3300PF 10% 25V CER-X7R 0201
PLACE_NEAR=U5500.K5:5MM
C5524 3300PF 10% 25V CER-X7R 0201
PLACE_NEAR=U5500.L6:5MM
C5525 0.01UF 10% 25V X7R 0201
PLACE_NEAR=U5500.M5:5MM
C5526 0.01UF 10% 25V X7R 0201
D5501 SDM2U40CSP X3-WLB1608-1
C5501 1UF 10% 35V X5R 0402

VIN_3V3 C20 PP3V3_S2_LDO
VDDIO A12 PP1V25_S2
VDDIO_CFG D11 GND
LDO_3V3 C22 D21 PP3V3_UPC5_LDO
C5508 10UF 20% 6.3V CERM 0402
VIN_LV L20 UPC5_LV
R5501 1K 5% 1/20W TK 0201-1
VOUT_LV L18
C5502 1.0UF 20% 6.3V X5R 0201-1
VRET C16
C5500 10UF 20% 6.3V CERM 0402
SS L22 UPC5_SS

LDO_CORE E22 PP1V5_UPC5_LDO_CORE
C5505 10UF 20% 6.3V CERM 0402
VBUS_OPT D5 PPVBUS_USBC5
PP_HV_OPT F5 PPHV_INT5_AONSW
C5509 0.68UF 5% 6.3V X6S 0402

C_CC1 M15 N16 USBC5_CC1
C_CC2 M17 N18 USBC5_CC2
C5514 220PF 5% 50V C0G 0201-1
RPD_G1 L14 USBC5_CC1
RPD_G2 L16 GND
C_USB_TP K19 PD_UPC5_USB2
C_USB_TN K21 PD_UPC5_USB2
C_USB_BP J20 PD_UPC5_USB2
C_USB_BN J22 PD_UPC5_USB2
R5579 100K 5% 1/20W TK 0201
C_SBU1 J16 PD_UPC5_USB2
C_SBU2 H15 PD_UPC5_USB2
C5513 220PF 5% 50V C0G 0201-1

GND_OPT C18
GND_OPT E18
GND_OPT D17
GND_OPT G18

GND
A22 H9 N20 B21 K15 N22

Configured as UPC5 (the 6th slot)

ACE_WILL_BE_OTPED:YES (POR)
If Ace can be OTPed
before installing bundle.
(ICT station is ready)

I2C_ADDR=Float
I2CM_SCL_CNFG=HIGH
I2CM_SDA_CNF=LOW

ACE_WILL_BE_OTPED:NO
Like in P0, Or EE bring up
Prevents I2C Conflict with
Other Aces before OTP

I2C_ADDR=84.5K PD
I2CM_SCL_CNFG=HIGH
I2CM_SDA_CNFG=HIGH

SPI ROM

PP3V3_UPC5_LDO
NOSTUFF R5561 3.3K
R5560 3.3K
R5563 3.3K
R5562 3.3K
C5560 1UF 10% 6.3V CERM 402
U5560 8MBIT-3.0V W25Q80DVUXIE USON
VCC
CLK
CS*
WP*(IO2)
HOLD*(IO3)
DI(IO0)
DO(IO1)
GND EPAD
OMIT_TABLE CRITICAL
SPI_UPC5_MOSI
SPI_UPC5_MISO
R5565 15
R5566 15
SPI_UPC5_R_MOSI
SPI_UPC5_R_MISO
ROM_UPC5_WP_L
ROM_UPC5_HOLD_L
R5564 3.3K
NOSTUFF R5567 47K
SPI_UPC5_CLK
SPI_UPC5_CS_L
R5568 15
R5569 15
SPI_UPC5_R_CLK
SPI_UPC5_R_CS_L

DISABLING BOOTING FROM SPI

AARDVARKANOID CONN

APN 516S00115
J5502 505070-1222
PACK_TYPE=M-ST-SM
PACK_IGNORE=TRUE
PACK_OPTION=MAGSAFE_ACE_UPC_DBG:SMALL
USBC_DBG
PP1V25_S2
SWD_UPC_SWDIO2
SWD_UPC_SWCLK1
SPI_UPC5_MISO
I2C_UPC01_3V3_SDA
I2C_UPC01_3V3_SCL
SPI_UPC5_CS_L
SPI_UPC5_CLK
SPI_UPC5_MOSI
UPC5_SER_DBG
NC_MAGSAFE_ACE_DEB_CON_10
NC

BOM_COST_GROUP=MAGSAFE

PAGE TITLE
MAGSAFE: PORT CONTROLLER

Apple Inc.

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SIZE D
REVISION 6.0.0
BRANCH evt-1
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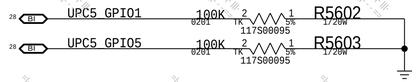
A 20V Aliases

POWER ALIASES

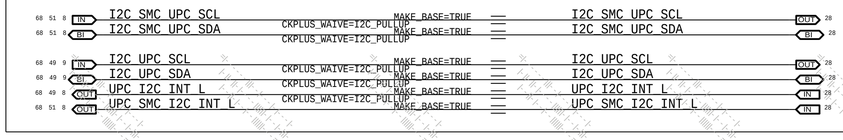
GPIOs



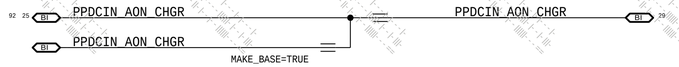
DEBUG PORT

B Power/Fuse for UPC5

C I2C Aliases



D Charger Aliases



BOM_COST_GROUP=MAGSAFE

PAGE TITLE
MAGSAFE: CONTROLLER SUPPORT

Apple Inc.

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3V8 AON CONTROLLER
30A ICC MAX

PPBUS_AON
92 89 31
5.5 < VIN < 13.5 V
PACK_IGNORE=TRUE
3V8_AON_MLCC-STD
C5704
2.2UF
20%
25V
X6S-CERM
0402
138S00042
BYPASS=U5700.8::15MM
3V8_AON_MLCC-LN
C5704
2.2UF
20%
25V
X6S
0402-1
138S00410
BYPASS=U5700.8::15MM

PP5V_S2_P3V8AON_VDRV
32
4.75 < VDRV < 5.5 V
VDRV IS EXTERNAL OPTION TO
POWER IC INSTEAD OF VIN
TO SAVE POWER
C5700
10UF
20%
10V
X6S
0603-1
138S00248
BYPASS=U5700.6::15MM
0603 SIZE REQUESTED BY DCDC
CRITICAL

PP5V_AON
92
4.75 < LDO5 < 5.25 V
MAX I_OUT TYP 160 MA
LDO5 NOT TO BE USED BY
SYSTEM IN 30A DESIGNS
C5702
10UF
20%
10V
X6S
0603-1
138S00248
BYPASS=U5700.7::15MM
0603 SIZE REQUESTED BY DCDC
CRITICAL

P3V8AON_PVCC
31
ONLY FOR USE BY GATE
DRIVE CIRCUITRY
C5701
10UF
20%
10V
X6S
0603-1
138S00248
BYPASS=U5700.5::15MM
0603 SIZE REQUESTED BY DCDC
CRITICAL

P3V8AON_PWR_EN
26 IN
R5710
0
0%
1/20W
1K
0201
117S00073
P3V8AON_PWR_EN_R
VIH_MIN 1.07 V
VIL_MAX 0.63 V

P3V8AON_LPM
42 IN
R5711
0
0%
1/20W
1K
0201
117S00073
P3V8AON_LPM_R
VIH_MIN 1.1 V
VIL_MAX 0.5 V

PP5V_AON
92
R5712
47K
5%
1/20W
1K
0201
117S00129

PU TO INT LDO5 OR OTHER RAIL
P3V8AON_FAULT_L
FAULT PULL DOWN CURRENT 1-2 MA TYPICAL

P3V8AON_IMON
IMON NOT TO BE USED SYSTEM SIDE
<RDAR://58648650>
IMON IS 2.52 V @ 30 A
VENDOR REQUIRES R > 1M, C < 50 PF
R5750
1M
5%
1/20W
1M
0201
117S00096
C5751
10PF
5%
25V
C0G
0201
131S00003
NOSTUFF
R5751
2.21K
1%
1/20W
TK
0201
118S00367
P3V8AON_IMON_P3V8AON

I2C_P3V8AON_SCL
30
I2C_P3V8AON_SDA
39
VIH_MIN 1.1 V
VIL_MAX 0.5 V
GND'ED FOR POR (DATASHEET TABLE 1.5)
I2C ADDRESS
7 BIT: 0X36
8 BIT WR: 0X6C

P3V8AON_GPIO
OPEN FOR PRODUCTION APPLICATION
PER DATASHEET REV 1.0

NOSTUFF
R5700
100K
5%
1/20W
TK
0201
117S00095

P3V8AON_SS
LONG STARTUP TIME SO INRUSH
BELOW 0.5A USB LIMIT
C5703
0.22UF
10%
10V
X5R
0201-1
132S00202
CRITICAL

U5700
RAA225501A-B0M1
QFN
OMIT_TABLE

"BOM1" SCH SYMBOL
FOR 30A OTP

APN OF SYMBOL
353S02326

VIN	8	
VDRV	6	
LDO5	7	
PVCC	5	
ENABLE	12	(9M PD)
LPM	13	(9M PD)
SCL	10	
SDA	9	
FAULT*	14	(OD)
IMON	18	(0-4.5V)
GPIO	11	
SOFTSTART	17	
EPAD	33	

F_SW IS REGISTER CONTROLLED
ICC MAX 30A DESIGN: 1 MHZ

BOOT1	4	P3V8AON_BST1	IN 31
UGATE1	3	P3V8AON_DRVH1	OUT 31
PHASE1	2	P3V8AON_SW1	IN 31 89
LGATE1	1	P3V8AON_DRVL1	OUT 31
BOOT2	29	P3V8AON_BST2	IN 31
UGATE2	30	P3V8AON_DRVH2	OUT 31
PHASE2	31	P3V8AON_SW2	IN 31 89
LGATE2	32	P3V8AON_DRVL2	OUT 31
BOOT3	28	P3V8AON_BST3	IN 31
UGATE3	27	P3V8AON_DRVH3	OUT 31
PHASE3	26	P3V8AON_SW3	IN 31 89
LGATE3	25	P3V8AON_DRVL3	OUT 31
VSEN	15	P3V8AON_VSENSE	IN 31
VRTN	16	P3V8AON_VRTN	IN 31
CSP1	19	P3V8AON_ISEN1_P	IN 31
CSN1	20	P3V8AON_ISEN1_N	IN 31
CSP2	21	P3V8AON_ISEN2_P	IN 31
CSN2	22	P3V8AON_ISEN2_N	IN 31
CSP3	23	P3V8AON_ISEN3_P	IN 31
CSN3	24	P3V8AON_ISEN3_N	IN 31

3V8_AON_I2C-DEV
998-0955
PP5700
P4MM
SM
TPT_P3V8AON_PU_RAIL

PACK_OPTION=3V8_AON_I2C-DEV
NOSTUFF
R5760
1K
5%
1/20W
TK
0201-1
117S00077

PACK_OPTION=3V8_AON_I2C-DEV
NOSTUFF
R5761
1K
5%
1/20W
TK
0201-1
117S00077

CKPLUS_WAIVE=I2C_PULLUP
I2C_P3V8AON_SCL
30
CKPLUS_WAIVE=I2C_PULLUP
I2C_P3V8AON_SDA
39

PACK_OPTION=3V8_AON_I2C-DEV
R5762
0
0%
1/20W
TK
0201
117S00073

PACK_OPTION=3V8_AON_I2C-DEV
R5763
0
0%
1/20W
TK
0201
117S00073

3V8_AON_I2C-POR
GND
MAKE_BASE=TRUE

3V8_AON_I2C-POR
GND
MAKE_BASE=TRUE

BOM_COST_GROUP=SOC POWER

30A OTP CHANGES DOCUMENTED IN <RDAR://61519509>
BOM5 IS A CONTINUATION OF BOM1 SINCE BOM1 IS FROZEN FOR TGA PROGRAMS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
353S02326	1	IC,RAA225501,3-PH VOLT REG,TQFN32	U5700	CRITICAL	P3V8AON_IC:A0	
353S02472	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B0,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B0	
353S02544	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B1,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B1	
353S02560	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B2,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B2	
353S02576	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B3,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B3	
353S02592	1	IC,RAA225501B,ICE,BOM1,A2,OTP-R0B0,QFN32	U5700	CRITICAL	P3V8AON_IC:A2_R0B0	<- 30A BOM1 OTP TGA PROGRAMS ARE GOING TO RAMP WITH
353S02645	1	IC,RAA225501C,ICE,BOM5,A2,OTP-R170,QFN32	U5700	CRITICAL	P3V8AON_IC:A2_R170	<- NEW BOM5 OTP FOR FUTURE PROGRAMS

SYNC_MASTER=MainVR
SYNC_DATE=10/01/2021
PAGE TITLE
POWER: 3V8 AON (1/2)

Apple Inc.

DRAWING NUMBER 051-07020
SIZE D
REVISION 6.0.0
BRANCH evt-1
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ICCMAX = 30 A

BOM_COST_GROUP=SOC POWER

SYNC_MASTER=MainVR SYNC_DATE=10/01/2021

PAGE TITLE: POWER: 3V8 AON (2/2)

Apple Inc.

DRAWING NUMBER: 051-07020 SIZE: D

REVISION: 6.0.0

BRANCH: evt-1

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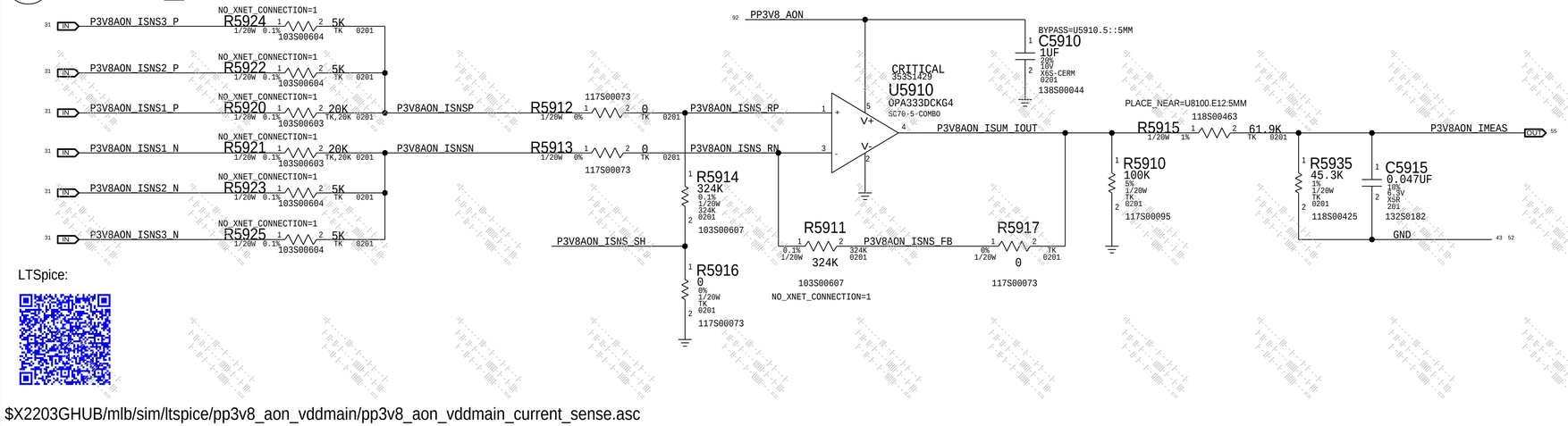
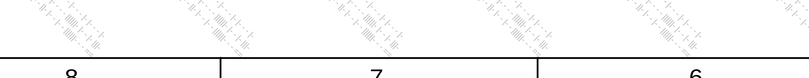
A PP3V8_AON Current Sense



LTSpice:

$X2203GHUB/mlb/sim/ltspice/pp3v8_aon_vddmain/pp3v8_aon_vddmain_current_sense.asc

B PP5V_S2 to PP3V8_AON VDRV Connection



BOM_COST_GROUP=SOC POWER

SYNC_MASTER=jwe59 SYNC_DATE=09/28/2021

PAGE TITLE: POWER: 3V8 AON SUPPORT

Apple Inc.

DRAWING NUMBER 051-07020 SIZE D

REVISION 6.0.0

BRANCH evt-1

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*** OK2INTEGRATE ***

PP3V8_AON

OMIT_TABLE
998-23585

U7700
VALE
CSP
SYM 1 OF 4

VOLTAGE INPUTS
SENSE
BUCK OUTPUTS

VDD_BUCK10_8 A7
VDD_BUCK10_8 B7
VDD_BUCK10_8 A11
VDD_BUCK10_8 B11
VDD_BUCK14_5 G13
VDD_BUCK14_5 G14
VDD_BUCK14_5 L12
VDD_BUCK14_5 L13
VDD_BUCK14_5 L14
VDD_MAIN_BUCK6 L1
VDD_BUCK6 M2
VDD_BUCK6 N2
VDD_BUCK6 P2
VDD_BUCK12 N6
VDD_BUCK12 P6
VDD_MAIN H5
VDD_MAIN_NORTH C11
VDD_MAIN_SOUTH N10
VDD_MAIN_SNS E4
VDD_BOOST_SNS F6
VDD_ANA C7
VDD_ANA D4
VDD_ANA D10
VDD_ANA G5
VDD_ANA G12
VDD_ANA K3
VDD_ANA M6
VDD_ANA N12
VDD_DIG D11
VDD_DIG E8
VDD_DIG K5
VDD_DIG L11
BSTLQ_LX C14
BSTLQ_VOUT D14
VDD_HI_INT1 D5
VDD_HI_INT2 E5
VDD_HI_INT3 L4
VDD_HI_INT4 N11
VDD_HI_INT5 E11
VDDIO_1V2 J10
VDDIO_1V8 H10
VDDIO_1V2_1V8 G10
VREF G4
VREF_ADC H4

PPVDD_SPMU_VDD_MAIN_SNS
PPVDD_SPMU_VDD_BOOST_SNS
PP1V5_LDOINT_SPMU
PP1V5_LDOINT_SPMU
SPMU_BSTLQ_LX
PP5V_SPMU_BSTLQ_XW
PP5V_SPMU_BSTLQ
PP1V25_S2
PP1V8_S2
PP1V2_AON_SPMU
PPVREF_SPMU
PP1V5_SPMU_VREFADC
GND_VREF_RTN_SPMU VOLTAGE=0V
GND_ADC_RTN_SPMU VOLTAGE=0V

PACK_IGNORE=TRUE
PMU_VDDMAIN_EXTRA_CAPS

BUCK5_LX0 H14
BUCK5_LX1 K12
BUCK5_LX1 K13
BUCK5_LX1 K14
BUCK5_FB H11
BUCK5_VSS_FB H12
BUCK6_VOUT M1
BUCK6_VOUT N1
BUCK6_VOUT P1
BUCK6_LX M3
BUCK6_LX N3
BUCK6_LX P3
BUCK6_FB L3
BUCK6_VSS_FB K2
BUCK8_LX0 A12
BUCK8_LX1 A10
BUCK8_LX1 B10
BUCK8_LX2 A8
BUCK8_LX2 B8
BUCK8_FB D12
BUCK8_VSS_FB C12
BUCK10_LX A6
BUCK10_LX B6
BUCK10_FB D6
BUCK10_VSS_FB C6
BUCK12_LX N5
BUCK12_LX P5
BUCK12_FB L5
BUCK12_VSS_FB M5
BUCK14_LX F13
BUCK14_LX F14
BUCK14_FB F11
BUCK14_VSS_FB F12

CRITICAL L7750 1.0UH-20%-4A-0.034OHM PIKD20161B 152S01283
BUCK5_LX0 SWITCH_NODE=TRUE DIDT=TRUE
PP0V779_S1_SRAM
CRITICAL L7751 0.22UH-20%-6.7A-0.023OHM PINA201217-SM 152S00204
BUCK5_LX1 SWITCH_NODE=TRUE DIDT=TRUE
R7750 0 0% 1/20W TK 0201
998-14727 XW7750 SHORT-16L-0.1MM-SM
BUCK5_FB BUCK5_FB_R NO_XNET_CONNECTION=1
BOMOPTION=PMU_FB:FF
GND
PP2V58_AWAKE_NAND_VCC
CRITICAL L7760 0.47UH-20%-6.9A-0.022OHM MEMX2520-SM 152S01325
BUCK6_LX SWITCH_NODE=TRUE DIDT=TRUE
R7760 0 0% 1/20W TK 0201
998-0313 XW7760 SHORT-16L-0.1MM-SM
BUCK6_FB BUCK6_FB_R NO_XNET_CONNECTION=1
BOMOPTION=BUCK6_BULK_REG
GND
CRITICAL L7780 1.0UH-20%-4A-0.034OHM PIKD20161B 152S01283
BUCK8_LX0 SWITCH_NODE=TRUE DIDT=TRUE
PPVDD_S1_DISP
CRITICAL L7781 0.1UH-20%-10.3A-0.010HM PCCE20161B-SM 152S01268
BUCK8_LX1 BUCK8_LX2 SWITCH_NODE=TRUE DIDT=TRUE
R7780 0 0% 1/20W TK 0201
998-0313 XW7780 SHORT-16L-0.1MM-SM
BUCK8_FB BUCK8_FB_R NO_XNET_CONNECTION=1
GND BOMOPTION=PMU_FB:FF
CRITICAL L77A0 0.47UH-20%-4A-0.024OHM PIKD20121B-SM 152S01263
BUCK10_LX SWITCH_NODE=TRUE DIDT=TRUE
PP0V5_S1_VDDQL
R77A0 0 0% 1/20W TK 0201
998-0313 XW77A0 SHORT-16L-0.1MM-SM
BUCK10_FB BUCK10_FB_R NO_XNET_CONNECTION=1
GND BOMOPTION=PMU_FB:FF
CRITICAL L77C0 0.47UH-20%-4A-0.024OHM PIKD20121B-SM 152S01263
BUCK12_LX SWITCH_NODE=TRUE DIDT=TRUE
PP0V88_S1
R77C0 0 0% 1/20W TK 0201
998-0313 XW77C0 SHORT-16L-0.1MM-SM
BUCK12_FB BUCK12_FB_R NO_XNET_CONNECTION=1
GND
CRITICAL L77E0 0.47UH-20%-4A-0.024OHM PIKD20121B-SM 152S01263
BUCK14_LX SWITCH_NODE=TRUE DIDT=TRUE
PP1V12_S2SW_AMPH
R77E0 0 0% 1/20W TK 0201
998-0313 XW77E0 SHORT-16L-0.1MM-SM
BUCK14_FB BUCK14_FB_R NO_XNET_CONNECTION=1
BOMOPTION=PMU_FB:FF
GND

PP0V779_S1_SRAM
PP2V58_AWAKE_NAND_VCC
PPVDD_S1_DISP
PP0V5_S1_VDDQL
PP0V88_S1
PP1V12_S2SW_AMPH

BOMOPTION=BUCK6_BULK_REG
PACK_IGNORE=TRUE
PACK_OPTION=BUCK6_LOCAL_CAPS
NOSTUFF
PACK_IGNORE=TRUE
PACK_OPTION=BUCK8_LOCAL_CAPS
BOMOPTION=PMU_BULK_VDDQL
PACK_IGNORE=TRUE
PACK_OPTION=BUCK14_LOCAL_CAPS

152S00874 L7700 0.47UH-20%-1.7A-0.175OHM PIJT1005FE-SM-COMBO
SPMU_BSTLQ_LX SWITCH_NODE=TRUE DIDT=TRUE
PP3V8_AON
XW7700 SHORT-12L-0.25MM-SM
PP5V_SPMU_BSTLQ_XW
VOLTAGE=5
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
PP5V_SPMU_BSTLQ

BOM_COST_GROUP=SOC POWER

SYNC_MASTER=MPMU_SPMU
SYNC_DATE=10/01/2021
PAGE TITLE
SPMU: INPUT PWR, BULK, BSTLQ
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LDO INPUTS

92 PP3V8_AON	M8	VDD_CTRL_LDOG	
92 PP3V8_AON	A1	VDD_BOOST_LDO	
	A2	VDD_BOOST_LDO	
	A3	VDD_BOOST_LDO	
92 PP3V8_AON	C1	VDD_MAIN_LDO	
	C2	VDD_MAIN_LDO	
	C3	VDD_MAIN_LDO	
92 PP3V8_AON	A4	VDD_LDO15	
93 34 PP1V25_S2	N7	VDD_LDO4	
92 PP0V88_S1	N8	VDD_LDO12	
92 34 PP1V8_S2	M13	VDD_SW4	
93 34 PP1V25_S2	P13	VDD_SW5	
	P14	VDD_SW5	
92 34 PP0V88_S1	P12	VDD_SW6	
92 PP0V88_S1	P10	VDD_SW7	

LOAD SWITCHES

LDO OUTPUTS

VLDO4	P7	PP0V72_S2_VDD_LOW	93
VLDO6	D3	NC_SPMU_VLDO6	93
VLDO9	D1	PP1V8_AON_SPMU	94
VLDO9B	B1	PP1V2_AON_SPMU	94
VLDO12	P8	PP0V78_S1_VDD_FIXED	94
VLDO15	B4	NC_SPMU_VLDO15	94
VLDO17	B2	NC_SPMU_VLDO17	94
VLDO18	B3	NC_SPMU_VLDO18	94
VLDOINT	D2	PP1V5_LDOINT_SPMU	94
VSW4	M14	PP1V8_AWAKE_SPMU_GPIO	34 93
VSW5	N13	PP1V25_AWAKE_NAND_VCCQ	34 93
VSW5	N14		
VSW6	P11	PP0V88_AWAKE_NAND_VDD	34 93
VSW7	P9		

LDO4 300MA MAX
LDO6 50MA MAX
LDO9 10MA MAX
LDO9B 10MA MAX
LDO12 850MA MAX
LDO15 100MA MAX
LDO17 250MA MAX
LDO18 250MA MAX
LDOINT 150MA MAX
VSW4 200MA MAX, 125MOHM MAX
VSW5 890MA MAX, 23MOHM MAX
VSW6 150MA MAX, 23MOHM MAX
VSW7 820MA MAX, 23MOHM MAX

VDD_LDO4
DECOUPLNIG SHARED WITH J10 (VDDIO_1V2)

93 34 PP1V25_S2

CRITICAL 138S00073 C7820 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C7821 10UF 20% 6.3V CER-X6S 0402-COMBO

VLDO4

93 PP0V72_S2_VDD_LOW

CRITICAL 138S00073 C7840 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C7841 10UF 20% 6.3V CER-X6S 0402-COMBO

VLDO12

94 PP0V78_S1_VDD_FIXED

CRITICAL 138S00073 C78C0 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C78C1 10UF 20% 6.3V CER-X6S 0402-COMBO

VDD_SW4
DECOUPLNIG SHARED WITH H10 (VDDIO_1V8)

92 34 PP1V8_S2

CRITICAL 138S00073 C7830 10UF 20% 6.3V CER-X6S 0402-COMBO

VSW4

93 34 PP1V8_AWAKE_SPMU_GPIO

CRITICAL 138S00044 C7850 1UF 20% 16V X6S-CERM 0201

VLDO9

94 PP1V8_AON_SPMU

CRITICAL 138S00073 C7890 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C7891 10UF 20% 6.3V CER-X6S 0402-COMBO

VLDOINT

94 PP1V5_LDOINT_SPMU

CRITICAL 138S00073 C7810 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C7811 10UF 20% 6.3V CER-X6S 0402-COMBO

VDD_SW5
DECOUPLNIG SHARED WITH J10 (VDDIO_1V2)

93 34 PP1V25_S2

CRITICAL 138S00073 C7822 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C7823 10UF 20% 6.3V CER-X6S 0402-COMBO

VSW5

93 34 PP1V25_AWAKE_NAND_VCCQ

CRITICAL 138S00073 C7860 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C7861 10UF 20% 6.3V CER-X6S 0402-COMBO

VLDO9B

94 PP1V2_AON_SPMU

CRITICAL 138S00073 C78A0 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C78A1 10UF 20% 6.3V CER-X6S 0402-COMBO

UN-UNUSED LDOS

LDO 6, 15, 17, 18

VDD_SW6/7
DECOUPLNIG SHARED VDD_LDO12

92 34 PP0V88_S1

CRITICAL 138S00073 C7831 10UF 20% 6.3V CER-X6S 0402-COMBO

VSW6/7

93 34 PP0V88_AWAKE_NAND_VDD

CRITICAL 138S00073 C7870 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C7871 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C7872 10UF 20% 6.3V CER-X6S 0402-COMBO

BOM_COST_GROUP=SOC POWER

PAGE TITLE: SPMU: LDO, SW

Apple Inc.

DRAWING NUMBER: 051-07020
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56	IN	SPMU_AMUXTDEV_TERM	H1	TDEV1	
56	IN	SPMU_TDEV2	J1	TDEV2	
56	IN	SPMU_AMUXTDEV_TERM	H2	TDEV3	
56	IN	SPMU_TDEV4	G2	TDEV4	
56	IN	SPMU_TDEV5	J2	TDEV5	
		SPMU_TCAL	G1	TCAL	
36	IN	SPMU_ADC_IN	G3	ADC_IN	
55	IN	LCDBKLT_HS_ISENSE	E2	AMUX_A<0>	ADC
55	IN	KBDBKLT_5V_ISENSE	F2	AMUX_A<1>	
55	IN	IMON_PBUS_AONSW_IPD	F1	AMUX_A<2>	
55	IN	IMON_P3V3_S2SW_IPD	E1	AMUX_A<3>	
36	BI	SPMU_AMUX_AY	H3	AMUX_AY	
55	IN	IMON_PBUS_AONSW_LCD	F3	AMUX_B<0>	
55	IN	IMON_P5V_S2SW_IPD	F4	AMUX_B<1>	
55	IN	WLANBT_3V3_ISENSE	F5	AMUX_B<2>	
55	IN	SPMU_AMUXTDEV_TERM	E3	AMUX_B<3>	
36	BI	SPMU_AMUX_BY	J3	AMUX_BY	
12	IN	SPMI_NUB_SPMU_CLK	L9	SPMI_SCLK	
12	BI	SPMI_NUB_SPMU_DATA	L8	SPMI_SDATA	
41	IN	SGPIO_SCLK	L7	SGPIO_SCLK	
41	BI	SGPIO_SDATA	M7	SGPIO_SDATA	
36	IN	SPMU_RESET_IN	G6	RESET_IN	
36	IN	SPMU_FORCE_SYNC	F9	FORCE_SYNC	INTERFACE
96	BI	SWD_NUB_SWDIO_SPMU	F8	SWD_TMS	
36	IN	GND	H8	DFT_CTRL0	
96	IN	SWD_NUB_SWCLK_SPMU	J9	DFT_CTRL1	
36	IN	GND	J5	DFT_CTRL2	
44		GND	M10	VPP	

		GPIO0	D8	LCD_OCP_FLT	
		GPIO1	J7	NC_SPMU_GPIO_1	
		GPIO2	K7	NC_SPMU_GPIO_2	
		GPIO3	J8	NC_SPMU_GPIO_3	
		GPIO4	G9	NC_SPMU_GPIO_4	GPIO
		GPIO5	D9	NC_SPMU_GPIO_5	
		GPIO6	K8	NC_SPMU_GPIO_6	
		GPIO7	H7	NC_SPMU_GPIO_7	
		GPIO8	L10	NC_SPMU_GPIO_8	
		GPIO9	K9	NC_SPMU_GPIO_9	
		GPIO10	H9	NC_SPMU_GPIO_10	
		GPIO11	E10	NC_SPMU_GPIO_11	
		GPIO12	K6	NC_SPMU_GPIO_12	
		GPIO13	K10	NC_SPMU_GPIO_13	
		GPIO14	H6	NC_SPMU_GPIO_14	
		GPIO15	E9	NC_SPMU_GPIO_15	
36 44	OUT	UVWARN*	G7	SPMU_VDDMAIN_UVWARN_L	THROTTLE
41	BI	SCRASH*	F7	SPMU_SCRASH_L	
41	IN	SGPIO_READY_REQ	G8	PMU_SGPIO_READY_REQ	

103S00584
R7950
3.92K
0.1%
1/20W
TF
0201

131S0805
C7950
100PF
50
25V
C0G
0201

56 36 GND_TCAL_SPMU
VOLTAGE=0V

OMIT_TABLE
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U7700
VALE
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J12	VSS_BUCK5	VSS	B12
J13	VSS_BUCK5	VSS	C4
J14	VSS_BUCK5	VSS	C5
		VSS	C8
A9	VSS_BUCK8	VSS	C9
B9	VSS_BUCK8	VSS	C10
A13	VSS_BUCK8	VSS	C13
B13	VSS_BUCK8	VSS	D7
		VSS	D13
A5	VSS_BUCK10	VSS	E6
B5	VSS_BUCK10	VSS	E7
		VSS	E12
N4	VSS_BUCK12_6	VSS	F10
P4	VSS_BUCK12_6	VSS	G11
		VSS	H13
E13	VSS_BUCK14	VSS	J6
E14	VSS_BUCK14	VSS	J11
		VSS	K1
A14	VSS_BSTLQ	VSS	K4
B14	VSS_BSTLQ	VSS	K11
		VSS	L2
J4	VSS_REF	VSS	L6
		VSS	M4
		VSS	M9
		VSS	M11
		VSS	M12
		VSS	N9

33 GND_VREF_RTN_SPMU

998-14727
XW7910
SHORT-16L-0.1MM-SM
1 2

44 36 35 33 GND

GND 33 35 36 44

PLACEMENT NOTES

CONNECT VSS_REF THROUGH ALL GND LAYERS
PLACE XW AT VSS_REF PIN, ROUTE RTN SIGNAL BACK TO PASSIVES

BOM_COST_GROUP=SOC POWER

PAGE TITLE
PAGE_TITLE=SPMU: GPIO, VSS

Apple Inc.

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A SPMU GPIO

35	LCD_OCP_FLT	LCD_OCP_FLT MAKE_BASE=TRUE 78
35	NC_SPMU_GPIO_1	NC_SPMU_GPIO_1 MAKE_BASE=TRUE
35	NC_SPMU_GPIO_2	NC_SPMU_GPIO_2 MAKE_BASE=TRUE
35	NC_SPMU_GPIO_3	NC_SPMU_GPIO_3 MAKE_BASE=TRUE
35	NC_SPMU_GPIO_4	NC_SPMU_GPIO_4 MAKE_BASE=TRUE
35	NC_SPMU_GPIO_5	NC_SPMU_GPIO_5 MAKE_BASE=TRUE
35	NC_SPMU_GPIO_6	NC_SPMU_GPIO_6 MAKE_BASE=TRUE
35	NC_SPMU_GPIO_7	NC_SPMU_GPIO_7 MAKE_BASE=TRUE
35	NC_SPMU_GPIO_8	NC_SPMU_GPIO_8 MAKE_BASE=TRUE
35	NC_SPMU_GPIO_9	NC_SPMU_GPIO_9 MAKE_BASE=TRUE
35	NC_SPMU_GPIO_10	NC_SPMU_GPIO_10 MAKE_BASE=TRUE
35	NC_SPMU_GPIO_11	NC_SPMU_GPIO_11 MAKE_BASE=TRUE
35	NC_SPMU_GPIO_12	NC_SPMU_GPIO_12 MAKE_BASE=TRUE
35	NC_SPMU_GPIO_13	NC_SPMU_GPIO_13 MAKE_BASE=TRUE
35	NC_SPMU_GPIO_14	NC_SPMU_GPIO_14 MAKE_BASE=TRUE
35	NC_SPMU_GPIO_15	NC_SPMU_GPIO_15 MAKE_BASE=TRUE
35	GND	GND MAKE_BASE=TRUE 33 35 36 44
35	GND	GND MAKE_BASE=TRUE 33 35 36 44

B Probe Points

35	BI SPMU_AMUX_AY	1 PP	PP8000 P4MM SM
35	BI SPMU_AMUX_BY	1 PP	PP8001 P4MM SM
33	IN BUCK5_LX0	1 PP	PP8050 P4MM SM
33	IN BUCK5_LX1	1 PP	PP8051 P4MM SM
33	IN BUCK6_LX	1 PP	PP8060 P4MM SM
33	IN BUCK8_LX0	1 PP	PP8080 P4MM SM
33	IN BUCK8_LX1	1 PP	PP8081 P4MM SM
33	IN BUCK8_LX2	1 PP	PP8082 P4MM SM
33	IN BUCK10_LX	1 PP	PP80A0 P4MM SM
33	IN BUCK12_LX	1 PP	PP80C0 P4MM SM
33	IN BUCK14_LX	1 PP	PP80E0 P4MM SM
33	IN SPMU_BSTLQ_LX	1 PP	PP80F0 P4MM SM

C SPMU Quiet GND Connections

44 36 35 33	GND	GND MAKE_BASE=TRUE
55 54 53	GND	GND MAKE_BASE=TRUE
56 35	GND_TCAL_SPMU	XW8030 SHORT-16L-0.1MM-SM 1 2 998-14727 GND MAKE_BASE=TRUE
33	GND_ADC_RTN_SPMU	XW8031 SHORT-16L-0.1MM-SM 1 2 998-14727 GND MAKE_BASE=TRUE

D SPMU Input Protection

35	SPMU_ADC_IN	R8010 1M 5% 1/20W TK 0201 117S00096	
35	SPMU_RESET_IN	R8011 100K 5% 1/20W TK 0201 117S00095	
35	SPMU_FORCE_SYNC	R8012 10K 5% 1/20W TK 0201 117S00090	

E SPMU/SOC Throttle Pull-Up

PP1V25_AWAKE_IO 42 93

117S00090

R8020
10K
5%
1/20W
TK
0201

SPMU_VDDMAIN_UVWARN_L

F SPMU Sense Connections

33	PPVDD_SPMU_VDD_MAIN_SNS	XW8020 SHORT-16L-0.1MM-SM 1 2 998-14727 NO_XNET_CONNECTION=1	PP3V8_AON OUT 33 36 92
	PPVDD_SPMU_VDD_MAIN_SNS MAKE_BASE=TRUE		
33	PPVDD_SPMU_VDD_BOOST_SNS	XW8021 SHORT-16L-0.1MM-SM 1 2 998-14727 NO_XNET_CONNECTION=1	PP3V8_AON OUT 33 36 92
	PPVDD_SPMU_VDD_BOOST_SNS MAKE_BASE=TRUE		

BOM_COST_GROUP=SOC POWER

SYNC_MASTER= SYNC_DATE=09/10/2021

PAGE TITLE: SPMU: ALIASES, SUPPORT

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PP3V8_AON

138S00073 CRITICAL C81A0 10UF 20% 6.3V X6S CER-X6S 0402-COMBO
138S00073 CRITICAL C81A1 10UF 20% 6.3V X6S CER-X6S 0402-COMBO
138S00073 CRITICAL C81A2 10UF 20% 6.3V X6S CER-X6S 0402-COMBO
138S00073 CRITICAL C81A3 10UF 20% 6.3V X6S CER-X6S 0402-COMBO
138S00073 CRITICAL C81A4 10UF 20% 6.3V X6S CER-X6S 0402-COMBO
138S00073 CRITICAL C81A5 10UF 20% 6.3V X6S CER-X6S 0402-COMBO
138S00073 CRITICAL C81A6 10UF 20% 6.3V X6S CER-X6S 0402-COMBO
138S00073 CRITICAL C81A7 10UF 20% 6.3V X6S CER-X6S 0402-COMBO
138S00073 CRITICAL C81A8 10UF 20% 6.3V X6S CER-X6S 0402-COMBO
138S00073 CRITICAL C81A9 10UF 20% 6.3V X6S CER-X6S 0402-COMBO
138S00073 CRITICAL C81AA 10UF 20% 6.3V X6S CER-X6S 0402-COMBO
138S00073 CRITICAL C81AB 10UF 20% 6.3V X6S CER-X6S 0402-COMBO
138S00073 CRITICAL C81AC 10UF 20% 6.3V X6S CER-X6S 0402-COMBO
138S00073 CRITICAL C81AD 10UF 20% 6.3V X6S CER-X6S 0402-COMBO
138S00073 CRITICAL C81AE 10UF 20% 6.3V X6S CER-X6S 0402-COMBO
138S00073 CRITICAL C81AF 10UF 20% 6.3V X6S CER-X6S 0402-COMBO
138S00073 CRITICAL C81AG 10UF 20% 6.3V X6S CER-X6S 0402-COMBO
138S00073 CRITICAL C81AH 10UF 20% 6.3V X6S CER-X6S 0402-COMBO
138S00377 CRITICAL C8140 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8141 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8142 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8143 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8144 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8145 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8146 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8147 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8148 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8149 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8150 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8151 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8152 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8153 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8154 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8155 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8156 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8157 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8158 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8159 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8160 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8161 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8162 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8163 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8164 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8165 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8166 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8167 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8168 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8169 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8170 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8171 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8172 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8173 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8174 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8175 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8176 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8177 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8178 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8179 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8180 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8181 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8182 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8183 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8184 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8185 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8186 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8187 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8188 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8189 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8190 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8191 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8192 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8193 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8194 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8195 1UF 20% 10V X6S-CERM 0201

PMU_VDDMAIN_EXTRA_CAPS
PACK_IGNORE=TRUE
PMU_VDDMAIN_EXTRA_CAPS
PMU_VDDMAIN_EXTRA_CAPS
PACK_IGNORE=TRUE
PMU_VDDMAIN_EXTRA_CAPS

OMIT_TABLE
998-23524

U8100
STOWE_00
CSP
SYM 1 OF 5

VOLTAGE INPUTS
B1 VDD_BUCK_MP
B2 VDD_BUCK_MP
B3 VDD_BUCK_MP
B4 VDD_BUCK_MP
F1 VDD_BUCK_MP
F2 VDD_BUCK_MP
F3 VDD_BUCK_MP
F4 VDD_BUCK_MP
K1 VDD_BUCK_MP
K2 VDD_BUCK_MP
K3 VDD_BUCK_MP
K4 VDD_BUCK_MP
P1 VDD_BUCK_MP
P2 VDD_BUCK_MP
P20 VDD_BUCK_MP
P21 VDD_BUCK_MP
V20 VDD_BUCK_MP
V21 VDD_BUCK_MP
A7 VDD_BUCK_MP
B7 VDD_BUCK_MP
A11 VDD_BUCK_MP
B11 VDD_BUCK_MP
C11 VDD_BUCK_MP
A15 VDD_BUCK_MP
B15 VDD_BUCK_MP
U2 VDD_BUCK_MP
V2 VDD_BUCK_MP
W2 VDD_BUCK_MP
Y2 VDD_BUCK_MP
U6 VDD_BUCK_MP
V6 VDD_BUCK_MP
W6 VDD_BUCK_MP
Y6 VDD_BUCK_MP
U10 VDD_BUCK_MP
V10 VDD_BUCK_MP
W10 VDD_BUCK_MP
Y10 VDD_BUCK_MP
W14 VDD_BUCK_MP
Y14 VDD_BUCK_MP
W18 VDD_BUCK_MP
Y18 VDD_BUCK_MP
A19 VDD_BUCK13_3
B19 VDD_BUCK13_3
C19 VDD_BUCK13_3
J9 VDD_MAIN
C15 VDD_MAIN1
V16 VDD_MAIN2
M16 VDD_MAIN3

BUCK OUTPUTS
BUCK0_LX0 R1 R2
BUCK0_LX1 U3 V3 W3 Y3
BUCK0_LX3 U5 V5 W5 Y5
BUCK0_LX2 U7 V7 W7 Y7
BUCK0_LX4 U9 V9 W9 Y9
BUCK0_FB R4
BUCK0_VSS_FB R5
BUCK1_LX0 A6 B6
BUCK1_LX1 C1 C2 C3 C4
BUCK1_LX3 E1 E2 E3 E4
BUCK1_LX2 G1 G2 G3 G4
BUCK1_LX4 J1 J2 J3 J4
BUCK1_FB D6
BUCK1_VSS_FB E6
BUCK2_LX0 Y19
BUCK2_LX1 U20 U21
BUCK2_LX3 R20 R21
BUCK2_LX2 W17 Y17
BUCK2_LX4 W15 Y15
BUCK2_FB U18
BUCK2_VSS_FB T18

SENSE
PPVDD_MPMU_VDD_MAIN_SNS J8 VDD_MAIN_SNS
PBUS_DIV_SNS J6 VDD_BOOST_SNS

PP1V5_LDOINT_MPMU
132S00030 C8130 0.1UF 10% 10V X6S-CERM 0201
132S00030 C8131 0.1UF 10% 10V X6S-CERM 0201
C7 VDD_ANA
D14 VDD_ANA
D19 VDD_ANA
H5 VDD_ANA
J10 VDD_ANA
M18 VDD_ANA
P3 VDD_ANA
T8 VDD_ANA
V14 VDD_ANA
V19 VDD_ANA

PP1V5_LDOINT_MPMU
132S00030 C8132 0.1UF 10% 10V X6S-CERM 0201
132S00030 C8133 0.1UF 10% 10V X6S-CERM 0201
E18 VDD_DIG
G12 VDD_DIG
H6 VDD_DIG
L15 VDD_DIG
N6 VDD_DIG

CRITICAL L8100 1.0UH-20%-4A-0.034OHM PIKD20161B 152S01283
BUCK0_LX0 SWITCH_NODE=TRUE DIDT=TRUE
PPVDD_AWAKE_PCPU
CRITICAL L8101 0.1UH-20%-10.3A-0.01OHM PCCE20161B-SM 152S01268
BUCK0_LX1 SWITCH_NODE=TRUE DIDT=TRUE
BUCK0_LX3 SWITCH_NODE=TRUE DIDT=TRUE
CRITICAL L8102 0.1UH-20%-10.3A-0.01OHM PCCE20161B-SM 152S01268
BUCK0_LX2 SWITCH_NODE=TRUE DIDT=TRUE
BUCK0_LX4 SWITCH_NODE=TRUE DIDT=TRUE
R8100 0 0% 1/20W TK 0201
BUCK0_FB_R
BOMOPTION=PMU_FB:FF
XW8100 SHORT-16L-0.1MM-SM 998-14727 NO_XNET_CONNECTION=1
GND

CRITICAL L8110 1.0UH-20%-4A-0.034OHM PIKD20161B 152S01283
BUCK1_LX0 SWITCH_NODE=TRUE DIDT=TRUE
PPVDD_AWAKE_GPU
CRITICAL L8111 0.1UH-20%-10.3A-0.01OHM PCCE20161B-SM 152S01268
BUCK1_LX1 SWITCH_NODE=TRUE DIDT=TRUE
BUCK1_LX3 SWITCH_NODE=TRUE DIDT=TRUE
CRITICAL L8112 0.1UH-20%-10.3A-0.01OHM PCCE20161B-SM 152S01268
BUCK1_LX2 SWITCH_NODE=TRUE DIDT=TRUE
BUCK1_LX4 SWITCH_NODE=TRUE DIDT=TRUE
R8110 0 0% 1/20W TK 0201
BUCK1_FB_R
BOMOPTION=PMU_FB:FF
XW8110 SHORT-16L-0.1MM-SM 998-14727 NO_XNET_CONNECTION=1
GND

CRITICAL L8120 1.0UH-20%-4A-0.034OHM PIKD20161B 152S01283
BUCK2_LX0 SWITCH_NODE=TRUE DIDT=TRUE
PPVDD_S1_SOC
CRITICAL L8121 0.1UH-20%-10.3A-0.01OHM PCCE20161B-SM 152S01268
BUCK2_LX1 SWITCH_NODE=TRUE DIDT=TRUE
BUCK2_LX3 SWITCH_NODE=TRUE DIDT=TRUE
CRITICAL L8122 0.1UH-20%-10.3A-0.01OHM PCCE20161B-SM 152S01268
BUCK2_LX2 SWITCH_NODE=TRUE DIDT=TRUE
BUCK2_LX4 SWITCH_NODE=TRUE DIDT=TRUE
R8120 0 0% 1/20W TK 0201
BUCK2_FB_R
BOMOPTION=PMU_FB:FF
XW8120 SHORT-16L-0.1MM-SM 998-14727 NO_XNET_CONNECTION=1
GND

PPVDD_AWAKE_PCPU
CRITICAL 138S1058 C8100 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8101 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8102 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8103 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8104 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8105 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8106 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8107 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8108 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8109 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C810A 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C810B 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S00039 C810C 2.2UF 20% 6.3V X6S-CERM 0201
CRITICAL 138S00039 C810D 2.2UF 20% 6.3V X6S-CERM 0201

PPVDD_AWAKE_GPU
CRITICAL 138S1058 C8110 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8111 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8112 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8113 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8114 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8115 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8116 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8117 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8118 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8119 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C811A 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C811B 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C811C 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C811D 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S00039 C811E 2.2UF 20% 6.3V X6S-CERM 0201
CRITICAL 138S00039 C811F 2.2UF 20% 6.3V X6S-CERM 0201

PPVDD_S1_SOC
CRITICAL 138S1058 C8120 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8121 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8122 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8123 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8124 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8125 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8126 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8127 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8128 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8129 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S00039 C812A 2.2UF 20% 6.3V X6S-CERM 0201
CRITICAL 138S00039 C812B 2.2UF 20% 6.3V X6S-CERM 0201

BOM_COST_GROUP=SOC POWER

SYNC_MASTER=MPMU_SPMU SYNC_DATE=10/01/2021
PAGE TITLE: MPMU: INPUT PWR, BUCK 0, 1, 2
Apple Inc.
DRAWING NUMBER 051-07020 SIZE D
REVISION 6.0.0
BRANCH evt-1
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*** OK2INTEGRATE ***

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U8100
STOWE_00
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MPMU_BSTLQ_LX — T15 BSTLQ_LX
PP5V_MPMU_BSTLQ_XW — T16 BSTLQ_VOUT
PP5V_MPMU_BSTLQ — D17 VDD_HI_INT1, G7 VDD_HI_INT2, E21 VDD_HI_INT3, M19 VDD_HI_INT4, J15 VDD_HI_INT5
PP1V25_S2 — N13 VDDIO_1V2
PP1V8_S2 — P15 VDDIO_1V8
PP1V2_AON_MPMU — M13 VDDIO_1V2_1V8
PPVREF_MPMU — H11 VREF
PP1V5_MPMU_VREFADC — H7 VREF_ADC
GND_VREF_RTN_MPMU VOLTAGE=0V
GND_ADC_RTN_MPMU VOLTAGE=0V
H9 VBAT
H8 IBAT
MPMU_VBAT
MPMU_IBAT
NC_MPMU_XIN — M21 XIN
MPMU_XOUT — L21 XOUT
PMU_CLK32K_SOC_R — M7 SLEEP_32K
PMU_CLK32K_WLBT_IPD_R — M8 OUT_32K
PP1V8_S2 — N20 VDD_SW1
PP1V8_S2 — N16 VDD_SW2
PP1V25_S2 — N18 VDD_SW3

138S00041 CRITICAL C8211 2.2UF 10% 10V X6S-CERM 0402
132S0406 CRITICAL C8210 0.22UF 20% 6.3V X6S-CERM 0201

CLOCK
LOAD SWITCHES
BUCK OUTPUTS

BUCK3_LX — A18, B18
BUCK3_FB — D18
BUCK3_VSS_FB — C18
BUCK4_LX0 — A16
BUCK4_LX1 — A14, B14
BUCK4_LX2 — A12, B12
BUCK4_FB — D16
BUCK4_VSS_FB — C16
BUCK7_LX0 — N1
BUCK7_LX1 — L1, L2, L3
BUCK7_FB — N4
BUCK7_VSS_FB — N3
BUCK9_LX0 — A8
BUCK9_LX1 — A10, B10, C10
BUCK9_FB — D8
BUCK9_VSS_FB — C8
BUCK11_LX0 — Y13
BUCK11_LX1 — V11, W11, Y11
BUCK11_FB — U13
BUCK11_VSS_FB — V13
BUCK13_LX — A20, B20, C20
BUCK13_FB — E20
BUCK13_VSS_FB — D20
VSW1 — N21
VSW2 — N17
VSW3 — N19

GND — 37 38 40 42 43 44

BUCK3_LX: CRITICAL L8230 0.47UH-20%-4A-0.024OHM PIKD20121B-SM 152S01263; R8230 0 1/20W TK 0201 0%; BUCK3_FB_R; XW8230 SHORT-16L-0.1MM-SM 998-14727 NO_XNET_CONNECTION=1 → PP1V8_S2 (43 92)

BUCK4_LX0/LX1/LX2: CRITICAL L8240 1.0UH-20%-4A-0.034OHM PIKD20161B 152S01283; L8241 0.1UH-20%-10.3A-0.01OHM PCCE20161B-SM CRITICAL 152S01268; R8240 0 1/20W TK 0201 0%; BUCK4_FB_R; XW8240 SHORT-16L-0.1MM-SM 998-14727 NO_XNET_CONNECTION=1 → PP1V05_S2SW_VDD2H (92)
BOMOPTION=PMU_FB:FF

BUCK7_LX0/LX1: CRITICAL L8270 1.0UH-20%-4A-0.034OHM PIKD20161B 152S01283; L8271 0.22UH-20%-6.7A-0.023OHM PINA2012T-SM 152S00204; R8270 0 1/20W TK 0201 0%; BUCK7_FB_R; XW8270 SHORT-16L-0.1MM-SM 998-14727 NO_XNET_CONNECTION=1 → PPVDD_AWAKE_CPU_SRAM (92)
BOMOPTION=PMU_FB:FF

BUCK9_LX0/LX1: CRITICAL L8290 1.0UH-20%-4A-0.034OHM PIKD20161B 152S01283; L8291 0.22UH-20%-6.7A-0.023OHM PINA2012T-SM 152S00204; R8290 0 1/20W TK 0201 0%; BUCK9_FB_R; XW8290 SHORT-16L-0.1MM-SM 998-14727 NO_XNET_CONNECTION=1 → PPVDD_S1_DCS (92)
BOMOPTION=PMU_FB:FF

BUCK11_LX0/LX1: CRITICAL L82B0 1.0UH-20%-4A-0.034OHM PIKD20161B 152S01283; L82B1 0.22UH-20%-6.7A-0.023OHM PINA2012T-SM 152S00204; R82B0 0 1/20W TK 0201 0%; BUCK11_FB_R; XW82B0 SHORT-16L-0.1MM-SM 998-14727 NO_XNET_CONNECTION=1 → PPVDD_AWAKE_ECPU (92)
BOMOPTION=PMU_FB:FF

BUCK13_LX: CRITICAL L82D0 0.47UH-20%-6.9A-0.022OHM MEMK2520-SM 152S01325; R82D0 0 1/20W TK 0201 0%; BUCK13_FB_R; XW82D0 SHORT-16L-0.1MM-SM 998-14727 NO_XNET_CONNECTION=1 → PP1V25_S2 (43 93)
BOMOPTION=PMU_FB:FF

GND
PP1V8_AWAKE — 38 93
NC_PPVOUT_MPMU_SW2_REG — 93
PP1V25_AWAKE_IO — 38 93

VSW4 700MA MAX, 23MOHM MAX
VSW5 350MA MAX, 125MOHM MAX
VSW6 200MA MAX, 23MOHM MAX

PP1V8_S2: CRITICAL 138S00073 C8230–C8239, C823A, C823B 10UF 20% 6.3V CER-X6S 0402-COMBO (92)

PP1V05_S2SW_VDD2H: CRITICAL 138S1058 C8240–C8249, C824A, C824B 15UF 20% 2V X6S 0402-2; CRITICAL 138S00039 C824C, C824D 2.2UF 20% 4V X6S-CERM 0201 (92)

PPVDD_AWAKE_CPU_SRAM: CRITICAL 138S1058 C8270–C8279 15UF 20% 2V X6S 0402-2; CRITICAL 138S00039 C8278, C8279 2.2UF 20% 4V X6S-CERM 0201 (92)

PPVDD_S1_DCS: CRITICAL 138S00039 C8298, C8299 2.2UF 20% 4V X6S-CERM 0201; CRITICAL 138S1058 C8290–C8297 15UF 20% 2V X6S 0402-2 (92)
NOSTUFF NOSTUFF

PPVDD_AWAKE_ECPU: CRITICAL 138S1058 C82B0–C82B7 15UF 20% 2V X6S 0402-2; CRITICAL 138S00039 C82B8, C82B9 2.2UF 20% 4V X6S-CERM 0201 (92)

PP1V25_S2: CRITICAL 138S1058 C82D0–C82D5 15UF 20% 2V X6S 0402-2 (93)

VDD_SW1: PP1V8_S2 (92 38) — CRITICAL 138S00073 C8200 10UF 20% 6.3V CER-X6S 0402-COMBO — PLACE_NEAR=U8100.N20:5MM

VDD_SW3: PP1V25_S2 (93 38) — CRITICAL 138S00073 C8201 10UF 20% 6.3V CER-X6S 0402-COMBO — PLACE_NEAR=U8100.N18:5MM

VSW1: PP1V8_AWAKE (93 38) — CRITICAL 138S00073 C8202, C8203 10UF 20% 6.3V CER-X6S 0402-COMBO

VSW3: PP1V25_AWAKE_IO (93 38) — CRITICAL 138S00073 C8204, C8205 10UF 20% 6.3V CER-X6S 0402-COMBO

BOM_COST_GROUP=SOC POWER

SYNC_MASTER=MPMU_SPMU SYNC_DATE=10/01/2021

PAGE TITLE: MPMU: BUCK 3, 4, 7, 9, 11, 13, SW

Apple Inc.

DRAWING NUMBER 051-07020 SIZE D
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OMIT_TABLE
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U8100
STOWE_00
CSP
SYM 3 OF 5

LDO INPUTS

VDDMAIN>>
92 PP3V8_AON — F15 VDD_CTRL_LDOG
92 42 40 39 37 PP3V8_AON — G17 VDD_BOOST_LDO; G18 VDD_BOOST_LDO; H17 VDD_BOOST_LDO; H18 VDD_BOOST_LDO; J18 VDD_BOOST_LDO
92 42 40 39 37 PP3V8_AON — J17 VDD_MAIN_LDO; K17 VDD_MAIN_LDO; K19 VDD_MAIN_LDO
92 PP3V8_AON — L18 VDD_RTC_ALT
BUCK3 OR BUCK13>>
43 39 PPVDD_LDO20_14_8_3 — F19 VDD_LDO20_14_8_3; F20 VDD_LDO20_14_8_3; G20 VDD_LDO20_14_8_3; H20 VDD_LDO20_14_8_3
BUCK4>>
92 39 PP1V05_S2SW_VDD2H — J20 VDD_LDO11
BUCK4>>
92 PP1V05_S2SW_VDD2H — F16 VDD_LDO16
42 IN NC_MPMU_LDO1_EN — R13 LDO1_EN

LDO OUTPUTS

VLDO1 G19 NC_MPMU_VLDO1 — 93
VLDO2 J16 PP1V8_AON — 93
VLDO3 F18 NC_MPMU_VLDO3 — 93
VLDO5 G16 NC_MPMU_VLDO5 — 93
VLDO7 H19 PP3V3_S2_LDO — 93
VLDO8 H21 PP1V2_AWAKE_PLL — 93
VLDO9 K16 PP1V8_AON_MPMU — 93
VLDO9B K18 PP1V2_AON_MPMU — 93
VLDO10 H16 PP3V3_AON — 94
VLDO11 J21 PP0V855_S2SW_CIO — 94
VLDO13 J19 PP3V3_S2SW_SNS — 94
VLDO14 F21 NC_MPMU_VLDO14 — 94
VLDO16 F17 NC_MPMU_VLDO16 — 94
VLDO20 G21 PP1V2_S2_CIO — 94
VLDOINT K20 PP1V5_LDOINT_MPMU — 94
VLDORTC L19 PP1V5_LDOINT_MPMU — 94
VLDORTC2 L20 GND — 42

LDO1 300MA MAX
LDO2 50MA MAX
LDO3 600MA MAX
LDO5 250MA MAX
LDO7 250MA MAX
LDO8 730MA MAX
LDO9 10MA MAX
LDO9B 10MA MAX
LDO10 250MA MAX
LDO11 1000MA MAX
LDO13 250MA MAX
LDO14 300MA MAX
LDO16 1500MA MAX
LDO20 400MA MAX
LDOINT 150MA MAX

VDD LDO 3/8/14/20

43 39 PPVDD_LDO20_14_8_3
CRITICAL 138S00073 C8300 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C8301 10UF 20% 6.3V CER-X6S 0402-COMBO

LDO 2 DECOUPLING

93 PP1V8_AON
CRITICAL 138S0750 C8320 4.7UF 6.3V X6S 0402

LDO 9 DECOUPLING

93 41 PP1V8_AON_MPMU
CRITICAL 138S00073 C8310 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C8311 10UF 20% 6.3V CER-X6S 0402-COMBO

LDO 11 DECOUPLING

94 PP0V855_S2SW_CIO
CRITICAL 138S00073 C83B5 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C83B6 10UF 20% 6.3V CER-X6S 0402-COMBO

LDO INT DECOUPLING

94 PP1V5_LDOINT_MPMU
CRITICAL 138S00073 C8380 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C8381 10UF 20% 6.3V CER-X6S 0402-COMBO

VDD LDO 11

92 39 PP1V05_S2SW_VDD2H
CRITICAL 138S00073 C83B0 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C83B1 10UF 20% 6.3V CER-X6S 0402-COMBO

LDO 7 DECOUPLING

93 PP3V3_S2_LDO
CRITICAL 138S00073 C8330 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C8331 10UF 20% 6.3V CER-X6S 0402-COMBO

LDO 9B DECOUPLING

93 PP1V2_AON_MPMU
CRITICAL 138S00073 C8340 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C8341 10UF 20% 6.3V CER-X6S 0402-COMBO

LDO 13 DECOUPLING

94 PP3V3_S2SW_SNS
CRITICAL 138S00073 C83D0 10UF 20% 6.3V CER-X6S 0402-COMBO

UN-UNUSED LDOS

LDO 1, 3, 5, 14, 16

LDO RTC

(TIED TO LDOINT FOR PORTABLES)

LDO 8 DECOUPLING

93 PP1V2_AWAKE_PLL
CRITICAL 138S00073 C8360 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C8361 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C8362 10UF 20% 6.3V CER-X6S 0402-COMBO
NOSTUFF

LDO 10 DECOUPLING

94 PP3V3_AON
CRITICAL 138S00073 C83A0 10UF 20% 6.3V CER-X6S 0402-COMBO

LDO 20 DECOUPLING

94 PP1V2_S2_CIO
CRITICAL 138S00073 C8350 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C8351 10UF 20% 6.3V CER-X6S 0402-COMBO

BOM_COST_GROUP=SOC POWER

SYNC_MASTER=MPMU_SPMU SYNC_DATE=10/01/2021
PAGE TITLE: MPMU: LDO
Apple Inc.
DRAWING NUMBER 051-07020 SIZE D
REVISION 6.0.0
BRANCH evt-1
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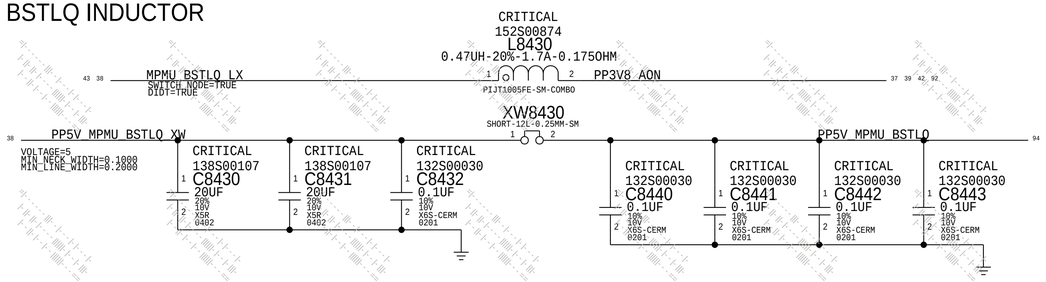
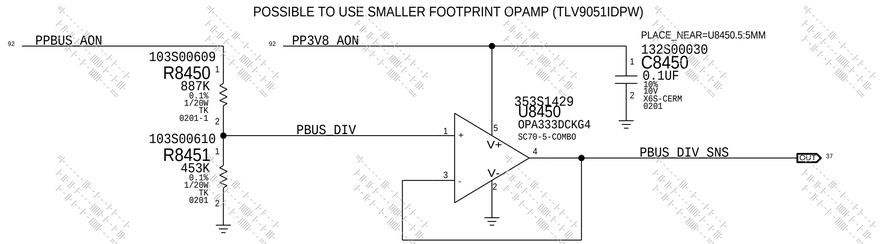
SHEET 39 OF 113

*** OK2INTEGRATE ***

BSTLQ INDUCTOR



PBUS SENSE



32K CLOCK XO (PACK_OPTION PMU_32K_OSC)

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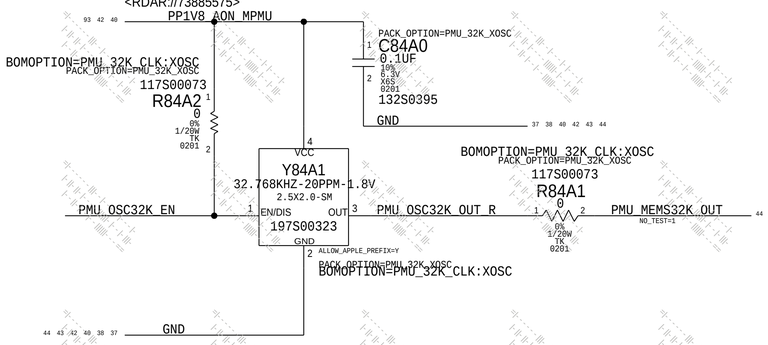
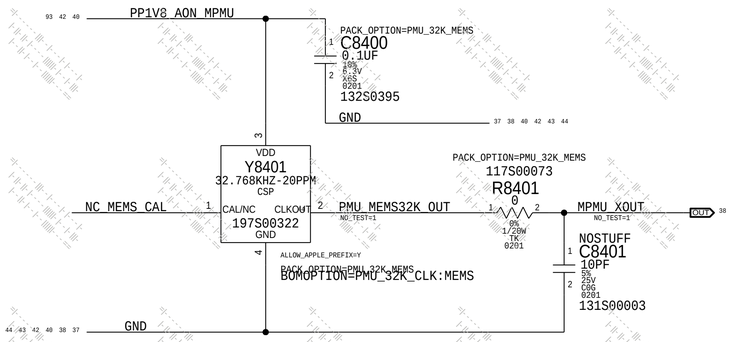
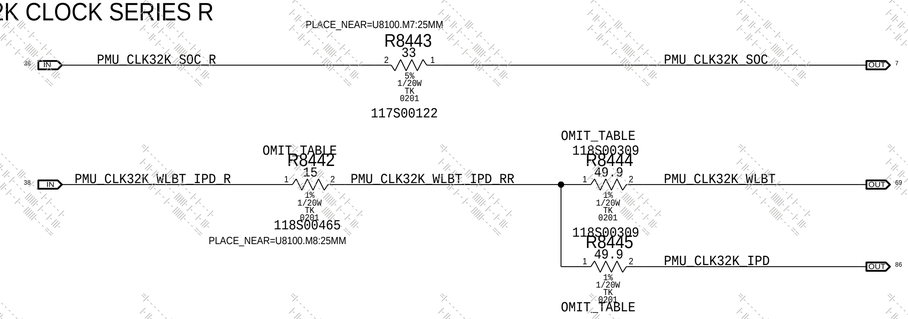


32K CLOCK MEMS (PACK_OPTION: PMU_32K_MEMS)



32K CLOCK SERIES R



OMIT_TABLE
998-23524

U8100
STOWE_00
CSP
SYM 5 OF 5

T1	VSS_BUCK0	VSS	B8
T2	VSS_BUCK0	VSS	B16
U1	VSS_BUCK0	VSS	C5
V1	VSS_BUCK0	VSS	C6
W1	VSS_BUCK0	VSS	C12
Y1	VSS_BUCK0	VSS	C13
U4	VSS_BUCK0	VSS	C14
V4	VSS_BUCK0	VSS	C17
W4	VSS_BUCK0	VSS	D5
Y4	VSS_BUCK0	VSS	D7
U8	VSS_BUCK0	VSS	D9
V8	VSS_BUCK0	VSS	D10
W8	VSS_BUCK0	VSS	D11
Y8	VSS_BUCK0	VSS	D12
		VSS	D13
A1	VSS_BUCK1	VSS	D15
A2	VSS_BUCK1	VSS	D21
A3	VSS_BUCK1	VSS	E5
A4	VSS_BUCK1	VSS	E15
A5	VSS_BUCK1	VSS	E16
B5	VSS_BUCK1	VSS	E17
D1	VSS_BUCK1	VSS	E19
D2	VSS_BUCK1	VSS	F5
D3	VSS_BUCK1	VSS	F14
D4	VSS_BUCK1	VSS	G5
H1	VSS_BUCK1	VSS	G11
H2	VSS_BUCK1	VSS	G15
H3	VSS_BUCK1	VSS	H13
H4	VSS_BUCK1	VSS	H15
		VSS	J5
T20	VSS_BUCK2	VSS	J7
T21	VSS_BUCK2	VSS	J11
W16	VSS_BUCK2	VSS	J12
Y16	VSS_BUCK2	VSS	K9
W20	VSS_BUCK2	VSS	K10
Y20	VSS_BUCK2	VSS	K21
W21	VSS_BUCK2	VSS	L4
Y21	VSS_BUCK2	VSS	L16
		VSS	L17
A13	VSS_BUCK4_3		
B13	VSS_BUCK4_3	VSS	M4
A17	VSS_BUCK4_3	VSS	M17
B17	VSS_BUCK4_3	VSS	M20
		VSS	N2
M1	VSS_BUCK7	VSS	N11
M2	VSS_BUCK7	VSS	N15
M3	VSS_BUCK7	VSS	P4
		VSS	P16
A9	VSS_BUCK9	VSS	P17
B9	VSS_BUCK9	VSS	P18
C9	VSS_BUCK9	VSS	P19
		VSS	R3
V12	VSS_BUCK11	VSS	R18
W12	VSS_BUCK11	VSS	R19
Y12	VSS_BUCK11	VSS	T3
		VSS	T4
A21	VSS_BUCK13	VSS	T5
B21	VSS_BUCK13	VSS	T6
C21	VSS_BUCK13	VSS	T7
		VSS	T9
T14	VSS_BSTLQ	VSS	T19
		VSS	U11
H10	VSS_REF	VSS	U12
		VSS	U14
		VSS	U19
		VSS	V15
		VSS	V17
		VSS	V18
		VSS	W13
		VSS	W19

GND_VREF_RTN_MPMU

998-14727
XW8410
SHORT-16L-0.1MM-SM

PLACEMENT NOTES

CONNECT VSS_REF THROUGH ALL GND LAYERS
PLACE XW AT VSS_REF PIN, ROUTE RTN SIGNAL BACK TO PASSIVES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S00465	1	RES,TK,15 OHM,1%,1/20W,0201	R8442		PMU_OUT32K:TEE
117S00122	1	RES,TK,33 OHM,5%,1/20W,0201	R8442		PMU_OUT32K:WLBT
118S00309	2	RES,TK,49.9 OHM,1%,1/20W,0201	R8444,R8445		PMU_OUT32K:TEE
117S00073	1	RES,TK,0 OHM,1A MAX,1/20W,0201	R8444		PMU_OUT32K:WLBT

BOM_COST_GROUP=SOC POWER

PAGE_TITLE=MPMU: MISC CKT, VSS

Apple Inc.

PAGE TITLE	
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*** OK2INTEGRATE ***

OMIT_TABLE
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U8100
STOWE_00
CSP
SYM 4 OF 5

56 IN	MPMU_AMUXTDEV_TERM	F8	TDEV1		GPIO0	R12	IPD_LID_OPEN_1V8 BI 42
56 IN	MPMU_TDEV2	F13	TDEV2		GPIO1	R6	CODEC_WAKE_L BI 42
56 IN	MPMU_TDEV3	F9	TDEV3		GPIO2	M11	IPD_OCP_FLT BI 42
56 IN	MPMU_TDEV4	F10	TDEV4		GPIO3	P9	NC_MPMU_GPIO_3 BI 42
56 IN	MPMU_TDEV5	F11	TDEV5	HLD	GPIO4	M10	CHGR_AUX_OK BI 42
56 IN	MPMU_TDEV6	F12	TDEV6		GPIO5	N9	WLBT_WAKE BI 42
56 IN	MPMU_TDEV7	G9	TDEV7	HLD	GPIO6	T10	IPD_PWR_EN BI 42
56 IN	MPMU_TDEV8	G8	TDEV8		GPIO7	N10	NC_MPMU_GPIO_7 BI 42
	MPMU_TCAL	E14	TCAL	SEQ	GPIO8	T11	IPD_TOUCH_RESET_L BI 42
42 IN	GND	E13	BRICK_ID1	SEQ	GPIO9	U15	NC_MPMU_GPIO_9 BI 42
42 IN	GND	E9	BRICK_ID2	SEQ	GPIO10	U16	LCD_PWR_EN BI 42
42 IN	MPMU_ADC_IN	G14	ADC_IN	SEQ	GPIO11	P11	P3V3S2_PWR_EN_MPMU BI 42
55 IN	DCIN_VSENSE	E11	AMUX_A<0>	SEQ	GPIO12	P12	PVDD1_PWR_EN BI 42
55 IN	DCIN_ISENSE	E10	AMUX_A<1>	SEQ	GPIO13	R15	WLBT_PWR_EN BI 42
55 IN	PBUS_VSENSE	E8	AMUX_A<2>	SEQ	GPIO14	P7	TPAD_KBD_WAKE_L BI 42
55 IN	BMON_ISENSE	E7	AMUX_A<3>	SEQ	GPIO15	P6	SE_PWR_EN BI 42
43 BI	MPMU_AMUX_AY	G13	AMUX_AY	SEQ	GPIO16	P5	NC_MPMU_GPIO_16 BI 42
55 IN	P3V8AON_IMEAS	E12	AMUX_B<0>	SEQ	GPIO17	R8	NAND0_LPB_L BI 42
55 IN	P3V3S2_HS_ISENSE	F6	AMUX_B<1>	SEQ	GPIO18	R9	BL_PWR_EN BI 42
55 IN	P5VS2_HS_ISENSE	F7	AMUX_B<2>	SEQ,HLD	GPIO19	R7	P3V8AON_LPM BI 42
55 IN	MPMU_AMUXTDEV_TERM	G6	AMUX_B<3>	SEQ,HLD	GPIO20	R10	P5VS2TPS_PWR_EN BI 42
43 BI	MPMU_AMUX_BY	G10	AMUX_BY	SEQ	GPIO21	P10	NC_MPMU_GPIO_21 BI 42
42 IN	PMU_ONOFF_L	N12	BUTTON1	SEQ	GPIO22	R11	NC_MPMU_GPIO_22 BI 42
44 IN	PMU_RSLOC_RST_L	L13	BUTTON2	SEQ	GPIO23	T12	NC_MPMU_GPIO_23 BI 42
42 IN	NC_MPMU_BUTTON3	K15	BUTTON3	SEQ	GPIO24	T13	IPD_MCU_RESET_L BI 42
42 IN	NC_MPMU_BUTTON4	K13	BUTTON4	SEQ	GPIO25	R16	NC_MPMU_GPIO_25 BI 42
				SEQ,HV	GPIO26	R17	NC_MPMU_GPIO_26 BI 42

ADC
GPIO
BUTTONS

			BUTTONO1	L14	NC_MPMU_BUTTONO1 OUT 42
			BUTTONO2	K14	NC_MPMU_BUTTONO2 OUT 42
			BUTTONO3	M12	NC_MPMU_BUTTONO3 OUT 42
			DBLCLICK_DET	T17	DBL_CLICK_DET OUT 44
			RESET*	L6	PMU_RESET_L OUT 44
42 IN	NC_MPMU_RESET_IN0	K7	RESET_IN0		
44 IN	SOC_WDOG	L9	RESET_IN1		
42 IN	UPC_PMU_RESET_1V8	K5	RESET_IN2		
44 IN	SOC_SOCHOT_L	M9	RESET_IN3		
42 IN	MPMU_SHDN	K11	SHDN	FORCE_DFU	H14	MPMU_SOC_FORCE_DFU_R
42 IN	MPMU_REQUEST_DFU	L12	REQUEST_DFU	WAKE2MS	R14	NC_MPMU_WAKE2MS OUT 42
44 IN	NC_MPMU_VBUS_DET	L11	VBUS_DETECT	OFF_REQ	U17	NC_MPMU_OFF_REQ OUT 42
				SYS_ALIVE	K6	PMU_SYS_ALIVE OUT 42 73 88 96
				ACTIVE_READY	L10	PMU_ACTIVE_READY OUT 44
				CRASH*	L8	PMU_CRASH_L OUT 42 46
				FAULT_OUT*	L7	MPMU_FAULT_OUT_L OUT 42
				SCRASH*	M6	MPMU_SCRASH_L BI 35
12 IN	SPMI_NUB_MPMU_CLK	M14	SPMI_SCLK			
12 BI	SPMI_NUB_MPMU_DATA	M15	SPMI_SDATA			
35 OUT	SGPIO_SCLK	P14	SGPIO_SCLK			
35 BI	SGPIO_SDATA	N14	SGPIO_SDATA			
35 OUT	PMU_SGPIO_READY_REQ	P13	SGPIO_READY_REQ			
96 IN	SWD_NUB_SWDIO_MPMU	K12	SWD_TMS			
42 IN	GND	J14	DFT_CTRL0			
96 IN	SWD_NUB_SWCLK_MPMU	J13	DFT_CTRL1			
42 BI	GND	H12	DFT_CTRL2			
42 IN	MPMU_OTP_SEL	N5	OTP_SEL			
44	GND	K8	VPP			

STATE MACHINE
INTERFACE
THROTTLE

			THROTTLE0*	L5	BUCK0_THERMAL_THROTTLE_L OUT 42 44
			THROTTLE1*	N7	BUCK1_THERMAL_THROTTLE_L OUT 42 44
			THROTTLE2*	P8	TPT_MPMU_THROTTLE2_L OUT 42 44
			THROTTLE3*	N8	PMU_VDDHI_UVWARN_L OUT 42 44
			UVWARN*	M5	MPMU_VDDMAIN_UVWARN_L OUT 42 44

103S00584
R8550
3.92K
0.1% 1/20W TK 0201

131S0805
C8550
100PF
5% 25V C0G 0201

GND_TCAL_MPMU
VOLTAGE=0V

117S00113
R8540
20
5% 1/20W TK 0201

117S00113
R8541
20
5% 1/20W TK 0201

117S00099
R8562
2.2K
5% 1/20W TK 0201
SOC_FORCE_DFU OUT 44

NOSTUFF
117S00090
R8561
10K
5% 1/20W TK 0201

PP1V8_AON_MPMU 39 93

>> IPU: LDO9
117S00077
R8560
1K
5% 1/20W TK 0201-1
SPMU_SCRASH_L BI 35

BOM_COST_GROUP=SOC POWER

SYNC_MASTER=MPMU_SPMU	SYNC_DATE=10/01/2021
PAGE TITLE	MPMU: GPIO
Apple Inc.	DRAWING NUMBER 051-07020 SIZE D
	REVISION 6.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH evt-1
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A MPMU GPIO Aliases

IO OTP SETTINGS (WIP), IF NOT OTP IT WILL BE CONFIGURED AS SW OVERRIDE..
SUPPLY:LDO9 (1.8V AON), BUCK13 (1.25V S2), BUCK3 (1.8V S2), SLDO9B (1.2V AON)
IO TYPE: INPUT, OUTPUT OPEN DRAIN, OR OUTPUT PUSH PULL
PULLS: IPU, IPD, NONE

GPIO0: LDO9 IN IPD
GPIO1: LDO9 IN IPU
GPIO2: LDO9 IN IPD
GPIO3: BUCK13 IN IPD
GPIO4: -WIP- IN IPU
GPIO5: BUCK13 IN IPD
GPIO6: LDO9 PP NONE
GPIO7: LDO9 IN IPD
> NEEDS OVERRIDE?
GPIO8: LDO9 OD NONE
GPIO9: LDO9 IN IPD
> NEEDS OVERRIDE?
GPIO10: LDO9 PP NONE
GPIO11: LDO9 PP NONE
GPIO12: LDO9 OD NONE
GPIO13: -WIP- PP NONE
GPIO14: LDO9 IN NONE
GPIO15: LDO9 PP NONE
GPIO16: LDO9 IN IPD
> NEEDS OVERRIDE?
GPIO17: BUCK13 PP NONE
GPIO18: LDO9 PP NONE
GPIO19: LDO9 PP IPD
GPIO20: LDO9 PP NONE
GPIO21: LDO9 IN IPD
> NEEDS OVERRIDE?
GPIO22: LDO9 IN IPD
> NEEDS OVERRIDE?
GPIO23: LDO9 IN IPD
> NEEDS OVERRIDE?
GPIO24: LDO9 OD NONE
GPIO25: WIP PP NONE
GPIO26: LDO9 IN IPD
> NEEDS OVERRIDE?

41 BI IPD_LID_OPEN_1V8 = IPD_LID_OPEN_1V8 MAKE_BASE=TRUE — 81 87
41 BI CODEC_WAKE_L = CODEC_WAKE_L MAKE_BASE=TRUE — 85
41 BI IPD_OCP_FLT = IPD_OCP_FLT MAKE_BASE=TRUE — 48
41 BI NC_MPMU_GPIO_3 = NC_MPMU_GPIO_3 MAKE_BASE=TRUE
41 BI CHGR_AUX_OK = CHGR_AUX_OK MAKE_BASE=TRUE — 26
41 BI WLBT_WAKE = WLBT_WAKE MAKE_BASE=TRUE — 69 70
41 BI IPD_PWR_EN = IPD_PWR_EN MAKE_BASE=TRUE — 42 48
41 BI NC_MPMU_GPIO_7 = NC_MPMU_GPIO_7 MAKE_BASE=TRUE
41 BI IPD_TOUCH_RESET_L = IPD_TOUCH_RESET_L MAKE_BASE=TRUE — 42 86
41 BI NC_MPMU_GPIO_9 = NC_MPMU_GPIO_9 MAKE_BASE=TRUE
41 BI LCD_PWR_EN = LCD_PWR_EN MAKE_BASE=TRUE — 76
41 BI P3V3S2_PWR_EN_MPMU = P3V3S2_PWR_EN_MPMU MAKE_BASE=TRUE — 42 46
41 BI PVDD1_PWR_EN = PVDD1_PWR_EN MAKE_BASE=TRUE — 48
41 BI WLBT_PWR_EN = WLBT_PWR_EN MAKE_BASE=TRUE — 69 70
41 BI TPAD_KBD_WAKE_L = TPAD_KBD_WAKE_L MAKE_BASE=TRUE — 86
41 BI SE_PWR_EN = SE_PWR_EN MAKE_BASE=TRUE — 23
41 BI NC_MPMU_GPIO_16 = NC_MPMU_GPIO_16 MAKE_BASE=TRUE
41 BI NAND0_LPB_L = NAND0_LPB_L MAKE_BASE=TRUE — 71 72
41 BI BL_PWR_EN = BL_PWR_EN MAKE_BASE=TRUE — 77
41 BI P3V8AON_LPM = P3V8AON_LPM MAKE_BASE=TRUE — 30 42
41 BI P5VS2TPS_PWR_EN = P5VS2TPS_PWR_EN MAKE_BASE=TRUE — 42 46
41 BI NC_MPMU_GPIO_21 = NC_MPMU_GPIO_21 MAKE_BASE=TRUE
41 BI NC_MPMU_GPIO_22 = NC_MPMU_GPIO_22 MAKE_BASE=TRUE
41 BI NC_MPMU_GPIO_23 = NC_MPMU_GPIO_23 MAKE_BASE=TRUE
41 BI IPD_MCU_RESET_L = IPD_MCU_RESET_L MAKE_BASE=TRUE — 42 86
41 BI NC_MPMU_GPIO_25 = NC_MPMU_GPIO_25 MAKE_BASE=TRUE
41 BI NC_MPMU_GPIO_26 = NC_MPMU_GPIO_26 MAKE_BASE=TRUE

B MPMU Input Protection & Pull-Downs

42 30 P3V8AON_LPM — R8630 100K 5% 1/20W TK 0201 — 117S00095
46 42 P5VS2TPS_PWR_EN — R8631 100K 5% 1/20W TK 0201 — 117S00095
46 42 P3V3S2_PWR_EN_MPMU — R8632 100K 5% 1/20W TK 0201 — 117S00095
42 41 MPMU_OTP_SEL — R8622 0 0% 1/20W TK 0201 — 117S00073
PD FOR PORTABLES
41 MPMU_ADC_IN — R8610 1M 5% 1/20W TK 0201 — 117S00096
38 MPMU_IBAT — R8611 1M 5% 1/20W TK 0201 — 117S00096
41 MPMU_REQUEST_DFU — R8612 10K 5% 1/20W TK 0201 — 117S00090
41 MPMU_SHDN — R8613 10K 5% 1/20W TK 0201 — 117S00090
38 MPMU_VBAT — R8614 1M 5% 1/20W TK 0201 — 117S00096
88 62 44 7 SOC_FORCE_DFU — R8615 47K 5% 1/20W TK 0201 — 117S00129
PMOS OD
48 42 IPD_PWR_EN — R8616 100K 5% 1/20W TK 0201 — 117S00095

C MPMU Pull-Ups

PP1V8_AON_MPMU — 40 93

R8620 117S00090 10K 5% 1/20W TK 0201 PMU_CRASH_L — 41 46
R8621 117S00095 100K 5% 1/20W TK 0201 MPMU_FAULT_OUT_L — 41
R8623 117S00090 10K 5% 1/20W TK 0201 PMU_ONOFF_L — 42 43 85 88
R8624 117S00090 10K 5% 1/20W TK 0201 PMU_RSLOC_RST_L — 43 44 85 88
R8625 117S00095 100K 5% 1/20W TK 0201 IPD_TOUCH_RESET_L — 42 86
R8626 117S00095 100K 5% 1/20W TK 0201 IPD_MCU_RESET_L — 42 86

PP1V25_S2 — 93

R8640 117S00090 10K 5% 1/20W TK 0201 PMU_SYS_ALIVE — 41 73 88 96
NOSTUFF

PP1V25_AWAKE_IO — 36 93

R8651 117S00090 10K 5% 1/20W TK 0201 BUCK0_THERMAL_THROTTLE_L — 41 44
NOSTUFF
R8652 117S00090 10K 5% 1/20W TK 0201 BUCK1_THERMAL_THROTTLE_L — 41 44
NOSTUFF
R8653 117S00090 10K 5% 1/20W TK 0201 TPT_MPMU_THROTTLE2_L — 41 44
R8654 117S00090 10K 5% 1/20W TK 0201 PMU_VDDHI_UVWARN_L — 41 44
NOSTUFF
R8650 117S00090 10K 5% 1/20W TK 0201 MPMU_VDDMAIN_UVWARN_L — 41 44
NOSTUFF

D MPMU Misc Aliases

41 GND = GND MAKE_BASE=TRUE — 37 38 40 42 43 44
41 GND = GND MAKE_BASE=TRUE — 37 38 40 42 43 44
41 GND = GND MAKE_BASE=TRUE — 37 38 40 42 43 44
41 GND = GND MAKE_BASE=TRUE — 37 38 40 42 43 44

39 NC_MPMU_LDO1_EN = NC_MPMU_LDO1_EN MAKE_BASE=TRUE
41 NC_MPMU_OFF_REQ = NC_MPMU_OFF_REQ MAKE_BASE=TRUE
42 41 MPMU_OTP_SEL = MPMU_OTP_SEL MAKE_BASE=TRUE — 41 42
41 NC_MPMU_WAKE2MS = NC_MPMU_WAKE2MS MAKE_BASE=TRUE

VLDORTC2 IS PLANNED FOR B0, AND CURRENTLY NOT IMPLEMENTED

39 GND = GND MAKE_BASE=TRUE — 37 38 40 42 43 44

E MPMU VDD_MAIN Sense

37 PPVDD_MPMU_VDD_MAIN_SNS — XW8661 SHORT-16L-0.1MM-SM 998-14727 NO_XNET_CONNECTION=1 — PP3V8_AON — OUT 37 39 40 92
PPVDD_MPMU_VDD_MAIN_SNS MAKE_BASE=TRUE

F MPMU Button and Reset Aliases

41 OUT PMU_ONOFF_L = PMU_ONOFF_L MAKE_BASE=TRUE — 42 43 85 88
41 NC_MPMU_BUTTON3 = NC_MPMU_BUTTON3 MAKE_BASE=TRUE
41 NC_MPMU_BUTTON4 = NC_MPMU_BUTTON4 MAKE_BASE=TRUE
41 NC_MPMU_BUTTONO1 = NC_MPMU_BUTTONO1 MAKE_BASE=TRUE
41 NC_MPMU_BUTTONO2 = NC_MPMU_BUTTONO2 MAKE_BASE=TRUE
41 NC_MPMU_BUTTONO3 = NC_MPMU_BUTTONO3 MAKE_BASE=TRUE
41 NC_MPMU_RESET_IN0 = NC_MPMU_RESET_IN0 MAKE_BASE=TRUE
41 UPC_PMU_RESET_1V8 = UPC_PMU_RESET_1V8 MAKE_BASE=TRUE — 43

BOM_COST_GROUP=SOC POWER

PAGE TITLE: MPMU: ALIAS, PULLS
Apple Inc.
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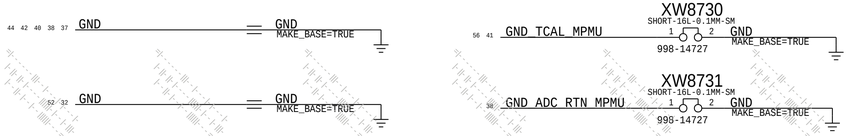
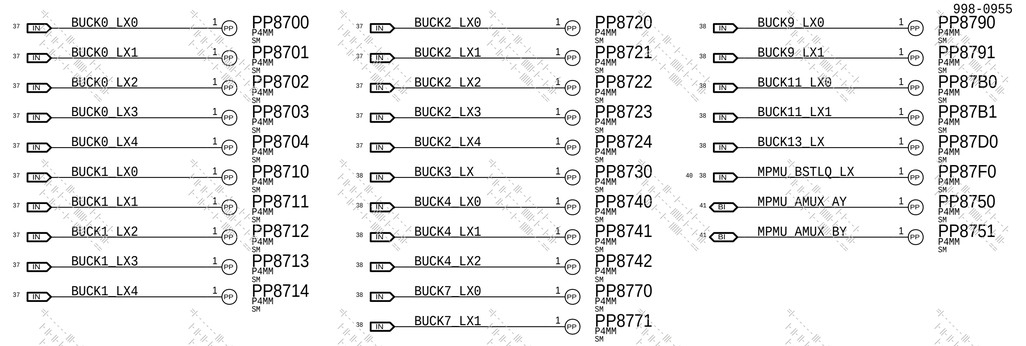
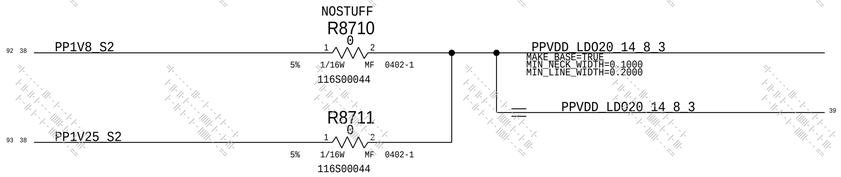
A MPMU Quiet GND Connections



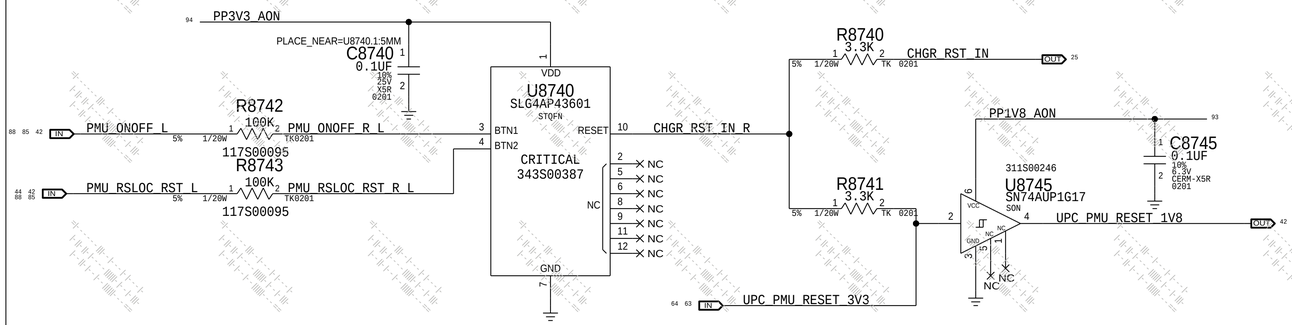
B MPMU Probe Points



C MPMU BUCK3/13 Option for LDO3/8/14/20 VDDIN



D MPMU Charger Reset Circuit



BOM_COST_GROUP=SOC POWER

SYNC_MASTER=jawebb SYNC_DATE=09/28/2021

PAGE TITLE: MPMU: SUPPORT

Apple Inc.

DRAWING NUMBER: 051-07020 SIZE: D

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A MPMU Misc Aliases

41	PMU_RSLOC_RST_L (OUT)	=	PMU_RSLOC_RST_L MAKE_BASE=TRUE	42 43 85 88
38	NC_MPMU_XIN	=	NC_MPMU_XIN MAKE_BASE=TRUE	
41	SOC_WDOG	=	SOC_WDOG MAKE_BASE=TRUE	7
41	SOC_SOCHOT_L	=	SOC_SOCHOT_L MAKE_BASE=TRUE	9
41	PMU_RESET_L	=	PMU_RESET_L MAKE_BASE=TRUE	7 88
41	PMU_ACTIVE_READY	=	PMU_ACTIVE_READY MAKE_BASE=TRUE	7 61 88
41	DBL_CLICK_DET	=	DBL_CLICK_DET MAKE_BASE=TRUE	9
41	SOC_FORCE_DFU	=	SOC_FORCE_DFU MAKE_BASE=TRUE	7 42 62 88
42 41	BUCK0_THERMAL_THROTTLE_L	=	BUCK0_THERMAL_THROTTLE_L MAKE_BASE=TRUE	9
42 41	BUCK1_THERMAL_THROTTLE_L	=	BUCK1_THERMAL_THROTTLE_L MAKE_BASE=TRUE	9
42 41	TPT_MPMU_THROTTLE2_L	=	TPT_MPMU_THROTTLE2_L MAKE_BASE=TRUE	
42 41	PMU_VDDHI_UVWARN_L	=	PMU_VDDHI_UVWARN_L MAKE_BASE=TRUE	9
42 41	MPMU_VDDMAIN_UVWARN_L	=	MPMU_VDDMAIN_UVWARN_L MAKE_BASE=TRUE	9
41	NC_MPMU_VBUS_DET	=	NC_MPMU_VBUS_DET MAKE_BASE=TRUE	
41	GND	=	GND MAKE_BASE=TRUE	37 38 40 42 43

B SPMU Misc Aliases

9	SPMU_VDDMAIN_UVWARN_L	=	SPMU_VDDMAIN_UVWARN_L MAKE_BASE=TRUE	44
36 35	SPMU_VDDMAIN_UVWARN_L	=	SPMU_VDDMAIN_UVWARN_L MAKE_BASE=TRUE	44
35	GND	=	GND MAKE_BASE=TRUE	33 35 36

C 32.768kHz Clock Aliases

40	PMU_MEMS32K_OUT	=	PMU_MEMS32K_OUT MAKE_BASE=TRUE	40

BOM_COST_GROUP=SOC POWER

SYNC_MASTER= SYNC_DATE=09/10/2021

PAGE TITLE: PMU: SUPPORT - FF

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* OK2INTEGRATE *

5V_S2 Voltage Regulator

SET ONE OPTION FOR THE PBUS POLY CAPS
- PACK_OPTION=5V_S2_PBUS-B12
- PACK_OPTION=5V_S2_PBUS-D2
- PACK_OPTION=5V_S2_PBUS-D12
- PACK_OPTION=5V_S2_PBUS18V

SET ONE OPTION FOR THE OUTPUT CAPS
- PACK_OPTION=5V_S2_VOUT-B2
- PACK_OPTION=5V_S2_VOUT-B12

SET ONE OPTION FOR THE INDUCTOR
- PACK_OPTION=5V_S2_IND-24
- PACK_OPTION=5V_S2_IND-15

SET ONE OPTION FOR THE MLCC CAPS
- PACK_OPTION=5V_S2_MLCC-STD
- PACK_OPTION=5V_S2_MLCC-LN

SET ONE OPTION FOR UC300
- PACK_OPTION=5V_S2_THINSTNCL
- PACK_OPTION=5V_S2_THICKSTNCL

Startup time MIN/TYP/MAX 4.3/7.9/15.9 ms

Vout=5.15V
EDC=6.6A
F=1.5MHz

PPBUS_5VS2_VIN

CC320 27UF 20% 16V TANT-POLY CASE-B12 128S00107
CC321 27UF 20% 16V TANT-POLY CASE-B12 128S00107
CC322 27UF 20% 16V TANT-POLY CASE-B12 128S00107
PACK_OPTION=5V_S2_PBUS18V

CC320 33UF 20% 16V TANT CASE-T 128S00009
CC321 33UF 20% 16V TANT CASE-T 128S00009
CC322 33UF 20% 16V TANT CASE-T 128S00009
PACK_IGNORE=TRUE
PACK_OPTION=5V_S2_PBUS-B12

CC340 68UF 20% 16V POLY-TANT CASE-D2E-SM 128S0264
CC341 68UF 20% 16V POLY-TANT CASE-D2E-SM 128S0264
PACK_IGNORE=TRUE
PACK_OPTION=5V_S2_PBUS-D2

CC350 33UF 20% 16V TANT CASED12-SM 128S0436
CC351 33UF 20% 16V TANT CASED12-SM 128S0436
PACK_IGNORE=TRUE
PACK_OPTION=5V_S2_PBUS-D12

CC323 2.2UF 20% 25V X6S-CERM 0402 138S00042
CC324 2.2UF 20% 25V X6S-CERM 0402 138S00042
CC325 2.2UF 20% 25V X6S-CERM 0402 138S00042
CC326 2.2UF 20% 25V X6S-CERM 0402 138S00042
PACK_IGNORE=TRUE
PACK_OPTION=5V_S2_MLCC-STD

CC323 2.2UF 20% 25V X6S 0402-1 138S00410
CC324 2.2UF 20% 25V X6S 0402-1 138S00410
CC325 2.2UF 20% 25V X6S 0402-1 138S00410
CC326 2.2UF 20% 25V X6S 0402-1 138S00410
PACK_OPTION=5V_S2_MLCC-LN

UC300
LT8642-1
LQFN-THICKSTNCL
353S02631
CRITICAL
PACK_IGNORE=TRUE
PACK_OPTION=5V_S2_THICKSTNCL

PPBUS_5VS2_VIN	4,5,12,13	VIN	
P5VS2_EN	14	EN/UV	
P5VS2_VC	19	VC	
P5VS2_PGOOD	1	PG	
P5VS2_FB	20	FB	
P5VS2_SS	18	SS	
P5VS2_RT	17	RT	
P5VS2_AGND	15	SYNC/MODE	
P5VS2_BIAS	2	BIAS	
P5VS2_INTVCC	3	INTVCC	
P5VS2_BST	7	BST	
P5VS2_SW	8,9,10	SW	
NC	16	CLKOUT	
	6,11,21	GND	
	22,23,24,25	NC	

RC328 100K 5% 1/20W TK 0201 117S00095
P5VS2_PGOOD — P5VS2_EN

PACK_OPTION=5V_S2_THINSTNCL

UC300
LT8642-1
LQFN
353S02631
CRITICAL

PPBUS_5VS2_VIN	4,5,12,13	VIN	
P5VS2_EN	14	EN/UV	
P5VS2_VC	19	VC	
P5VS2_PGOOD	1	PG	
P5VS2_FB	20	FB	
P5VS2_SS	18	SS	
P5VS2_RT	17	RT	
P5VS2_AGND	15	SYNC/MODE	
P5VS2_BIAS	2	BIAS	
P5VS2_INTVCC	3	INTVCC	
P5VS2_BST	7	BST	
P5VS2_SW	8,9,10	SW	
NC	16	CLKOUT	
	6,11,21	GND	
	22,23,24,25	NC	

P5VS2_BST_R: SWITCH_NODE=TRUE, DIDT=TRUE
P5VS2_SW: SWITCH_NODE=TRUE, DIDT=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000

CC330 2.2UF 20% 25V X6S-CERM 0402 138S00042

RC332 1.5 5% 1/20W TK 0201 117S00110

CC332 47NF 10% 10V X6S-CERM 0201 132S00028

PACK_OPTION=5V_S2_IND-15
CRITICAL
LC320 1UH-20%-11A-0.01150HM PIRR061E-SM 152S01458

PACK_OPTION=5V_S2_IND-24
CRITICAL
LC320 1UH-20%-11A-0.0127OHM PIMH062N-SM 152S00265

RC327 0 0% 1/20W TK 0201 117S00073
PACK_IGNORE=TRUE
PACK_OPTION=5V_S2_MLCC-STD

CC331 2.2UF 20% 25V X6S-CERM 0402 138S00042
CC331 2.2UF 20% 25V X6S 0402-1 138S00410
PACK_OPTION=5V_S2_MLCC-LN

RC333 0 0% 1/20W TK 0201 117S00073
P5VS2_PWR_EN — P5VS2_EN

RC321 20.5K 1% 1/20W TK 0201 118S00365
P5VS2_VC_R

CC328 1000PF 10% 16V X7R-1 0201 132S0651
CC329 100PF 5% 25V C0G 0201 131S0805
CC327 0.015UF 10% 16V X7R-CERM 0402 132S0381
RC320 25.5K 1% 1/20W TK 0201 118S00369
XWC320 SM

P5VS2_AGND

P5VS2_FB_XW

RC322 10 5% 1/20W TK 0201 117S00094

P5VS2_FB_RC
RC326 47K 1% 1/20W TK 0201 118S00286
P5VS2_FB_C
CC333 470PF 10% 16V X5R-X7R-CERM 0201 132S0361
P5VS2_FB

RC323 9.31K 1% 1/20W TK 0201 118S00427
P5VS2_FB_RC2

CRITICAL
RC324 200K 0.1% 1/20W TK 0201 103S00560

CRITICAL
RC325 27.4K 0.1% 1/20W TK 0201 103S00590

PP5V_S2

CC337 2.2UF 20% 25V X6S-CERM 0402 138S00042
CC338 2.2UF 20% 25V X6S-CERM 0402 138S00042
CC337 2.2UF 20% 25V X6S 0402-1 138S00410
CC338 2.2UF 20% 25V X6S 0402-1 138S00410
PACK_IGNORE=TRUE
PACK_OPTION=5V_S2_MLCC-STD
PACK_OPTION=5V_S2_MLCC-LN

CC334 150UF 20% 6.3V TANT CASE-B-SM 128S00038
CC335 150UF 20% 6.3V TANT CASE-B-SM 128S00038
CC334 150UF 20% 6.3V TANT-POLY CASE-B1S-1 128S00067
CC335 150UF 20% 6.3V TANT-POLY CASE-B1S-1 128S00067
CC336 150UF 20% 6.3V TANT-POLY CASE-B1S-1 128S00067
PACK_IGNORE=TRUE
PACK_OPTION=5V_S2_VOUT-B2
PACK_OPTION=5V_S2_VOUT-B12

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: POWER: 5V S2

Apple Inc.

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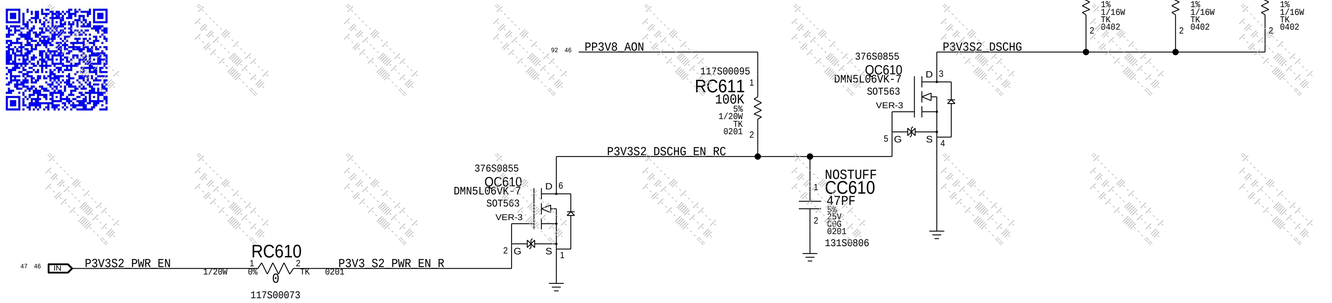
A PP3V3_S2 Discharge Circuit

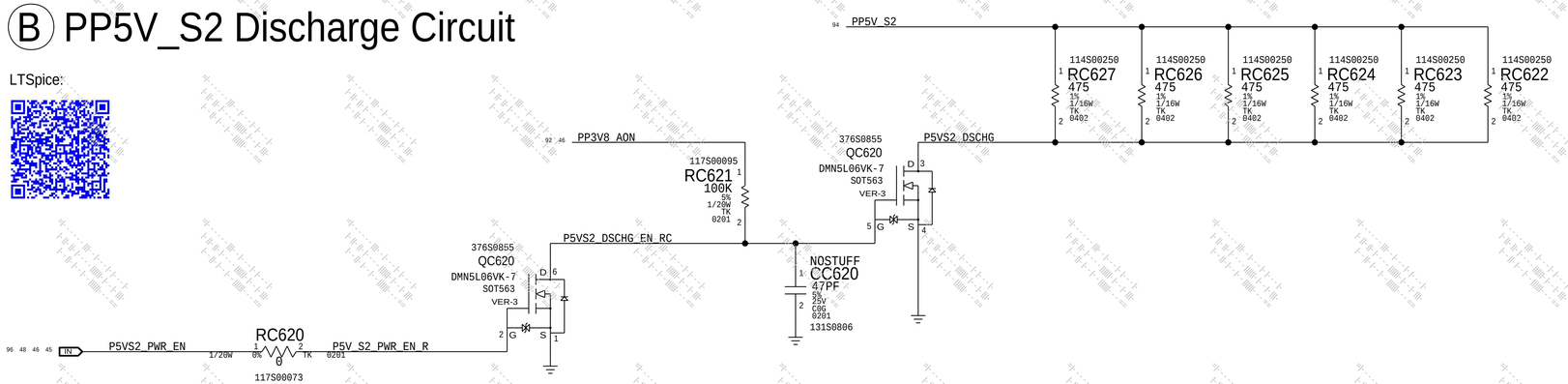
LTSpice:



$X2203GHUB/mlb/sim/ltspice/pp3v3_s2_discharge/pp3v3_s2_discharge_diodes_inc.asc

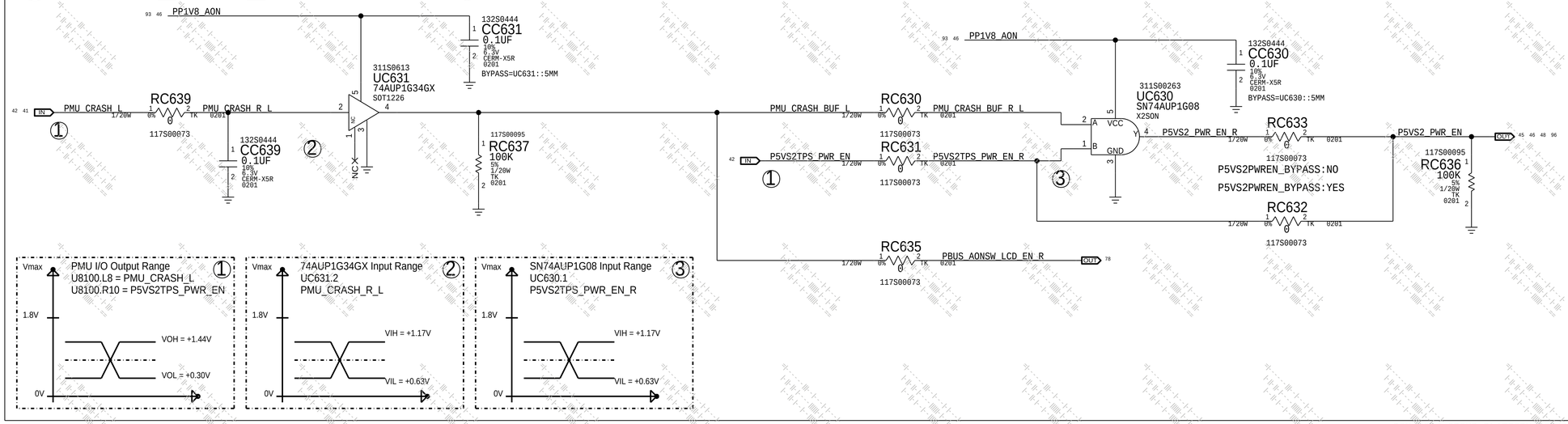
B PP5V_S2 Discharge Circuit

LTSpice:



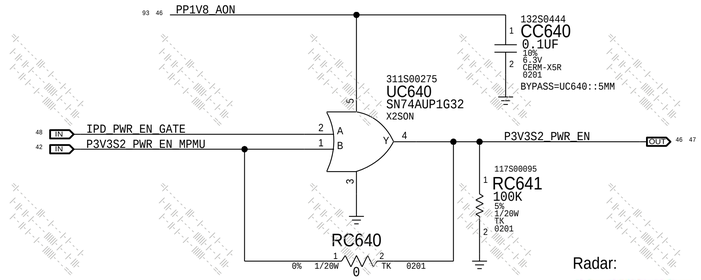
$X2203GHUB/mlb/sim/ltspice/pp5v_s2_discharge/pp5v_s2_discharge_diodes_inc.asc

C P5VS2_PWR_EN Control Logic



BOM_COST_GROUP=PLATFORM POWER

D P3V3S2_PWR_EN Control Logic



Radar:

NOTE:
Per Stowe PMU OTP, GPIO11 is OFF when the System is OFF.
A side-effect is that during the SIP_SMC->AWAKE transition the rail goes from ON->OFF->ON, which means we lose trackpad power during the OFF transition.
IPD_PWR_EN and PP5VS2_PWR_EN were moved to GPIOs that Stowe PMU can hold off.

SYNC_MASTER: SYNC_DATE=09/10/2021

PAGE TITLE: POWER: 5V, 3V3 Support

Apple Inc.

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* OK2INTEGRATE *

3V3_S2 VR

SET ONE OPTION FOR PBUS CAPS

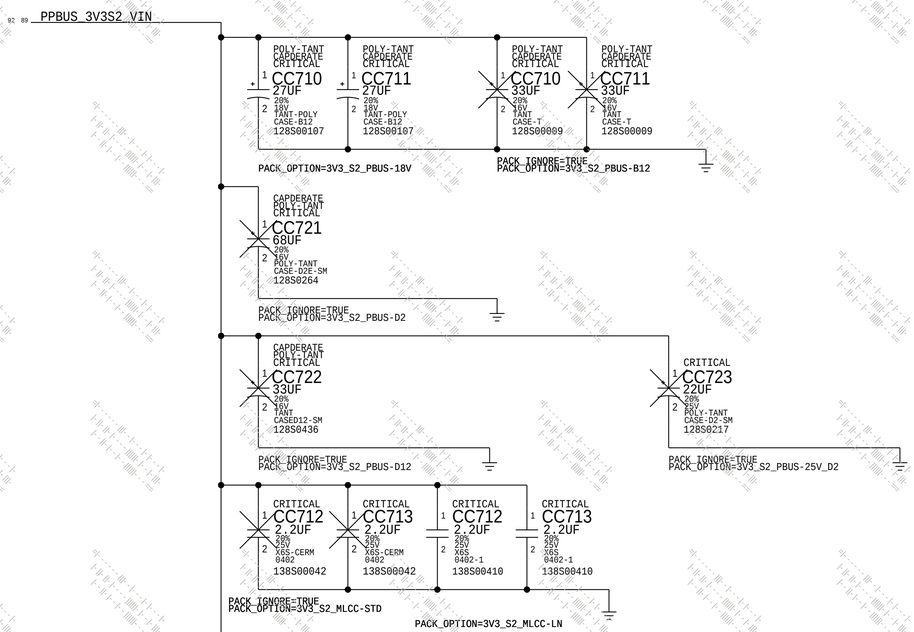
PACK_OPTION=3V3_S2_PBUS-18V
PACK_OPTION=3V3_S2_PBUS-B12
PACK_OPTION=3V3_S2_PBUS-D2
PACK_OPTION=3V3_S2_PBUS-D12
PACK_OPTION=3V3_S2_PBUS-25V_D2

SET ONE OPTION FOR THE OUTPUT POLY CAPS

PACK_OPTION=3V3_S2_VOUT-B2
PACK_OPTION=3V3_S2_VOUT-B12

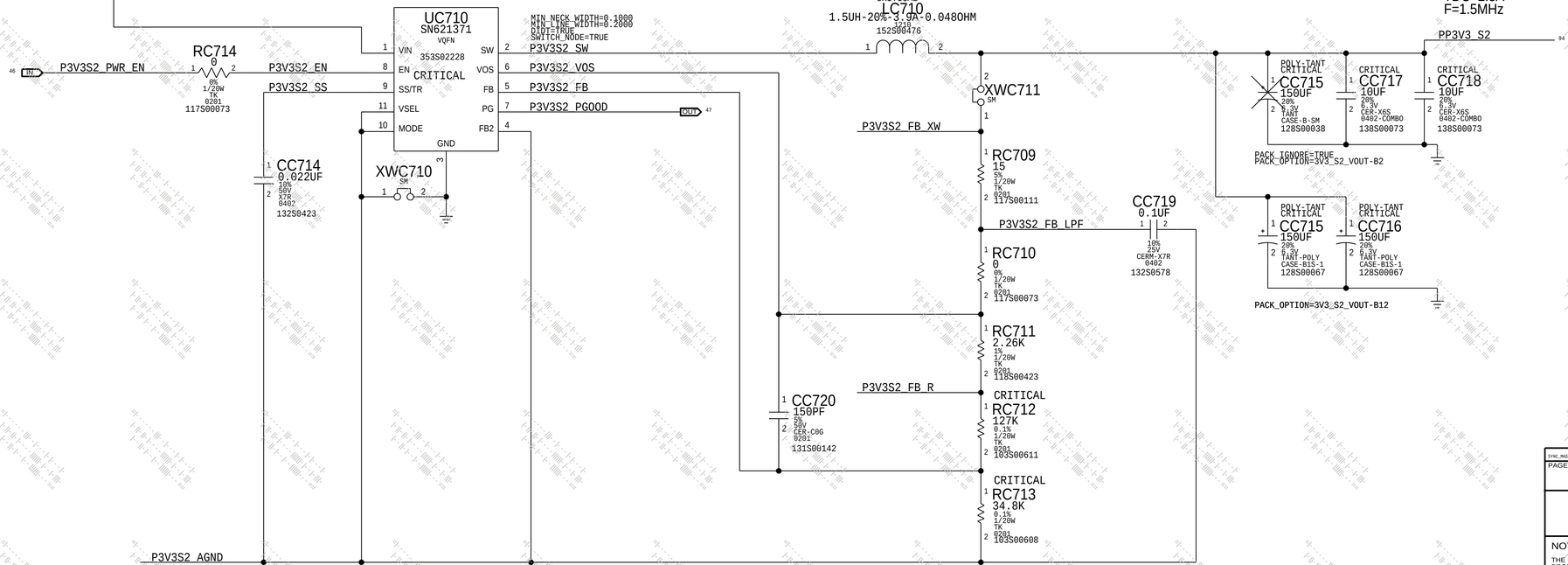
SET ONE OPTION FOR MLCC CAPS

PACK_OPTION=3V3_S2_MLCC-STD
PACK_OPTION=3V3_S2_MLCC-LN



Startup time
min=4.3ms
typ=6.4ms
max=8.81ms

VOUT=3.3V
EDC=2.5A
TDC=2.5A
F=1.5MHz



BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER: SYNC_DATE=09/18/2020

PAGE TITLE: POWER: 3V3 S2

Apple Inc.

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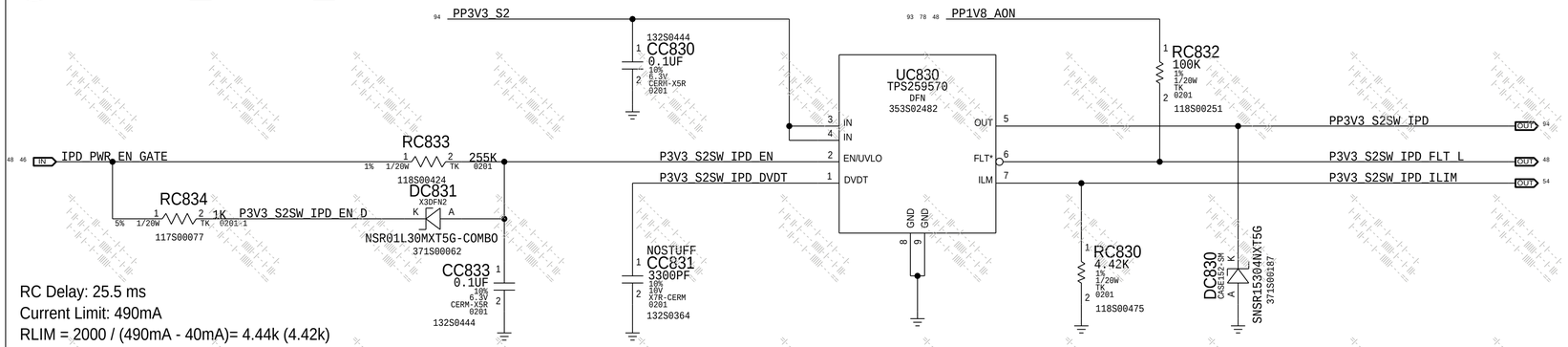
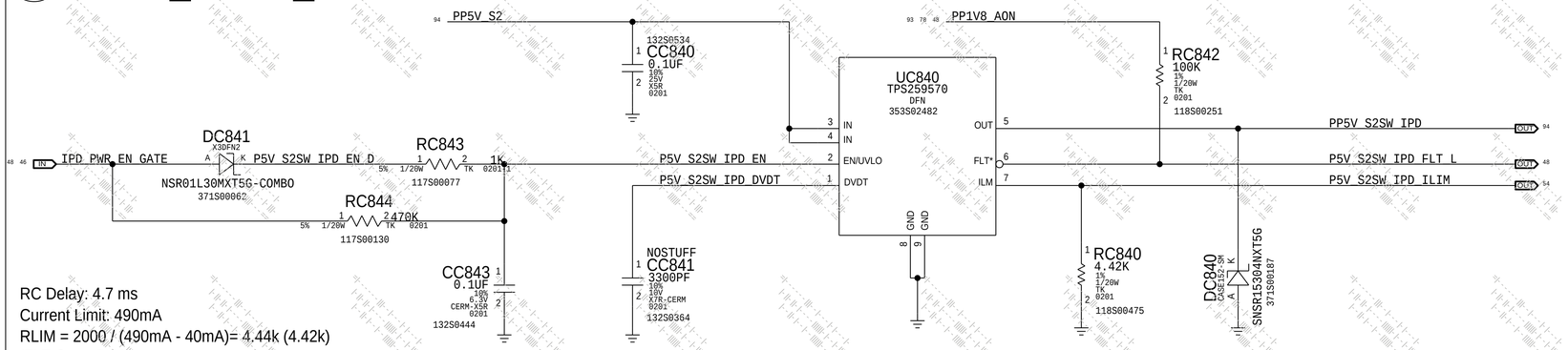
A PP3V3_S2SW_IPD Load Switch & e-Fuse



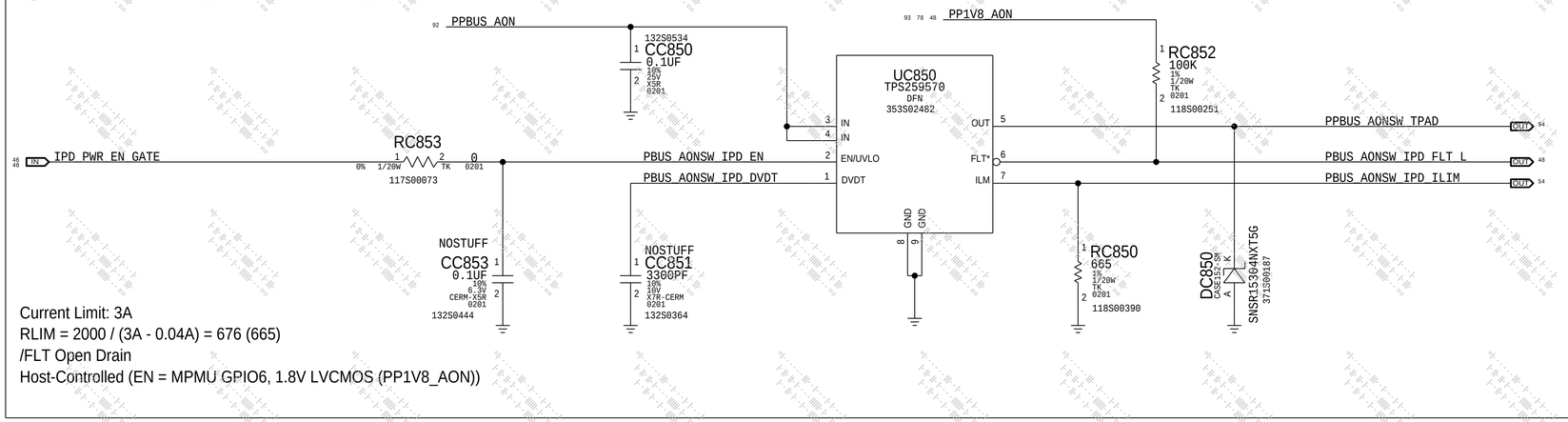
RC Delay: 25.5 ms
Current Limit: 490mA
RLIM = 2000 / (490mA - 40mA)= 4.44k (4.42k)
/FLT Open Drain
Host-Controlled (EN = MPMU GPIO6, 1.8V LVCMOS (PP1V8_AON))
$X2203GHUB/mlb/sim/ltspice/ocp_rc_filters/ocp_filters.asc

B PP5V_S2SW_IPD Load Switch & e-Fuse



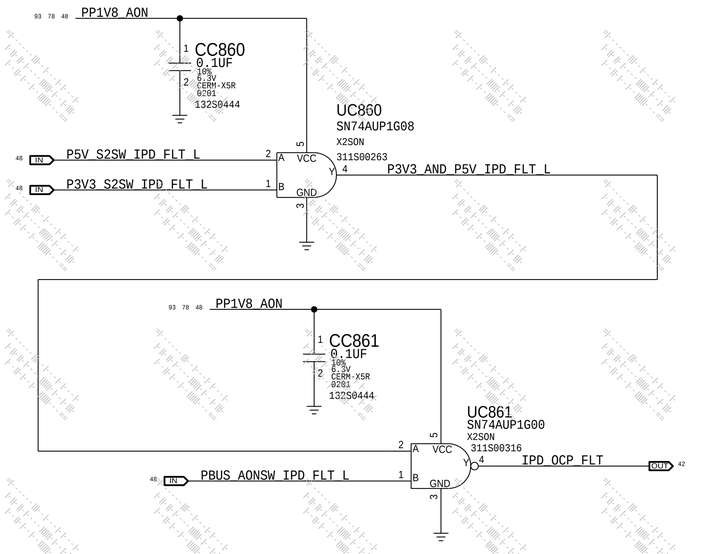
RC Delay: 4.7 ms
Current Limit: 490mA
RLIM = 2000 / (490mA - 40mA)= 4.44k (4.42k)
/FLT Open Drain
Host-Controlled (EN = MPMU GPIO6, 1.8V LVCMOS (PP1V8_AON))
$X2203GHUB/mlb/sim/ltspice/ocp_rc_filters/ocp_filters.asc

C PPBUS_AONSW_IPD Load Switch & e-Fuse

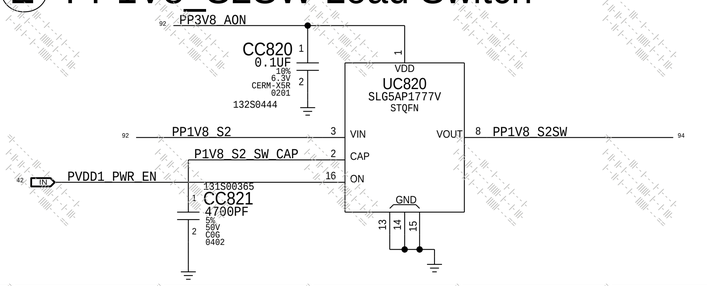


Current Limit: 3A
RLIM = 2000 / (3A - 0.04A) = 676 (665)
/FLT Open Drain
Host-Controlled (EN = MPMU GPIO6, 1.8V LVCMOS (PP1V8_AON))

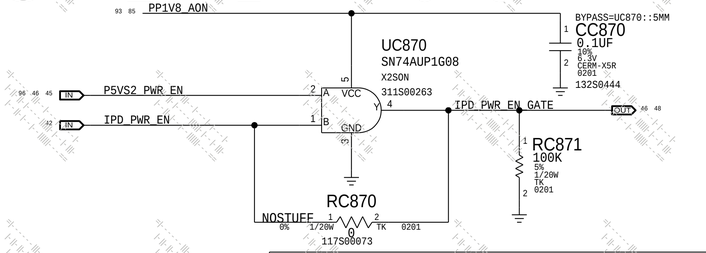
C IPD_OCP_FLT Control Logic



E PP1V8_S2SW Load Switch



F IPD_PWR_EN Gating Logic



BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER= SYNC_DATE=09/18/2020

PAGE TITLE: Power: Load Switches

Apple Inc.

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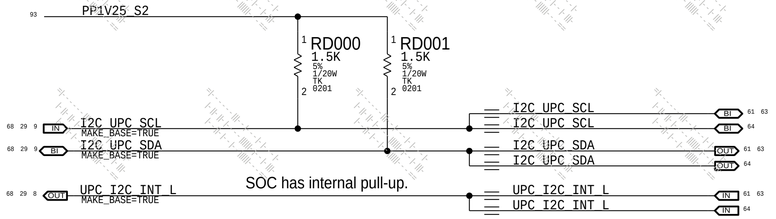
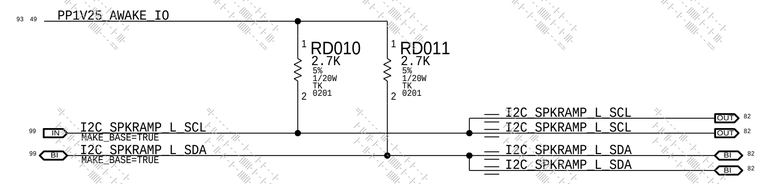
A AP_I2C0 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	0	400 kHZ	0X38	0X71	ACE2 - 0
AP	0	400 kHZ	0X3F	0X7F	ACE2 - 1
AP	0	400 kHZ	0X3A	0X75	ACE2 - MagSafe



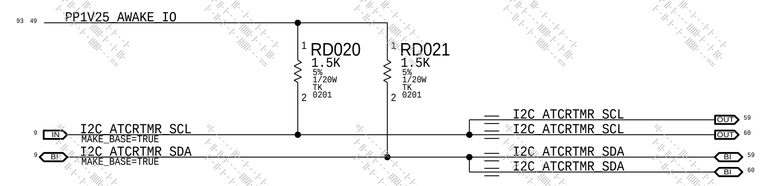
B AP_I2C1 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	1	400 kHZ	0X38	0X71	Left SpkrAmp A
AP	1	400 kHZ	0X39	0X73	Left SpkrAmp B



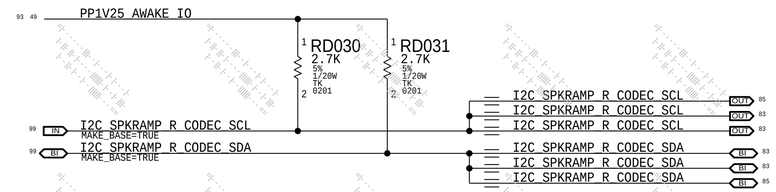
C AP_I2C2 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	2	100 kHZ/400 kHz	0X18	0X31	RT13 Port 0
AP	2	100 kHZ/400 kHz	0X19	0X33	RT13 Port 1



D AP_I2C3 - I2C Interface

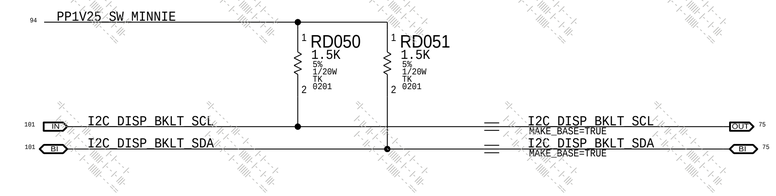
MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	3	400 kHZ	0X3B	0X77	Right SpkrAmp D
AP	3	400 kHZ	0X3C	0X79	Right SpkrAmp E
AP	3	400 kHZ	0X4B	0X97	CODEC



E AP_I2C4 - I2C Interface (Unused)

F DISP_I2C - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
DISP	0	100 kHZ	0X2F	0X5F	Minnie Bklt Drvr



BOM_COST_GROUP=SENSORS

SYNC_MASTER=
SYNC_DATE=09/10/2021

PAGE TITLE

I2C: AP, DISP

Apple Inc.

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BRANCH evt-1
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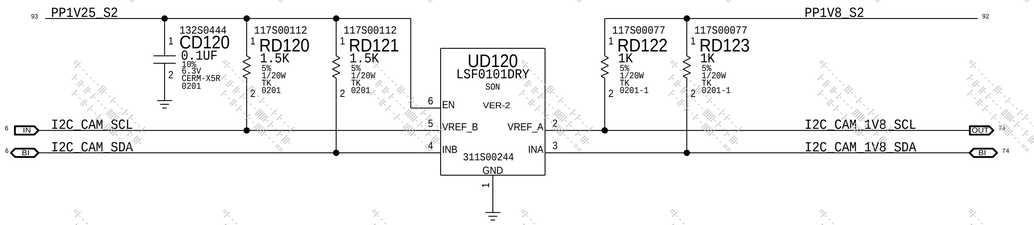
A ISP_I2C0 - I2C Interface

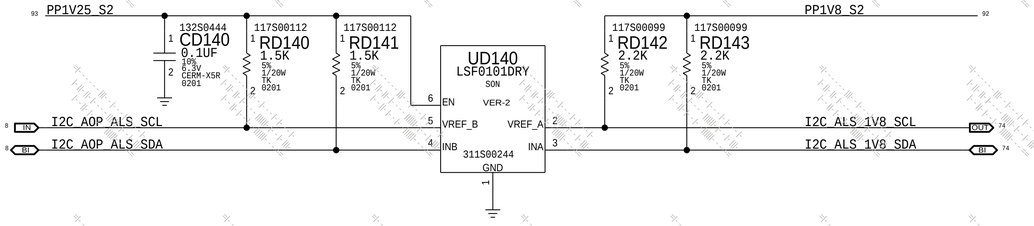
MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
ISP	0	400 kHz	0X10	0X21	Camera PMIC
ISP	0	400 kHz	0X36	0X6D	Image Sensor



B ISP_I2C1 - I2C Interface (Unused)

C AOP_I2CM0 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AOP	0	400 kHz	0X48	0X91	TMP108
AOP	0	400 kHz	0X29	0X53	TETRA2 ALS



D AOP_I2CM1 - I2C Interface (Unused)

E AOP_I2CM2 - I2C Interface (Unused)

F SEP_I2C0 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SEP	0	400 kHz/1 MHz	0X71	0XE3	SEP Custom App
SEP	0	400 kHz/1 MHz	0X51	0XA3	SEP EEPROM App

I2C Pull-Ups at EEPROM (U1950)

BOM_COST_GROUP=SENSORS

SYNC_MASTER= SYNC_DATE=09/10/2021

PAGE TITLE: I2C: ISP, AOP, SEP

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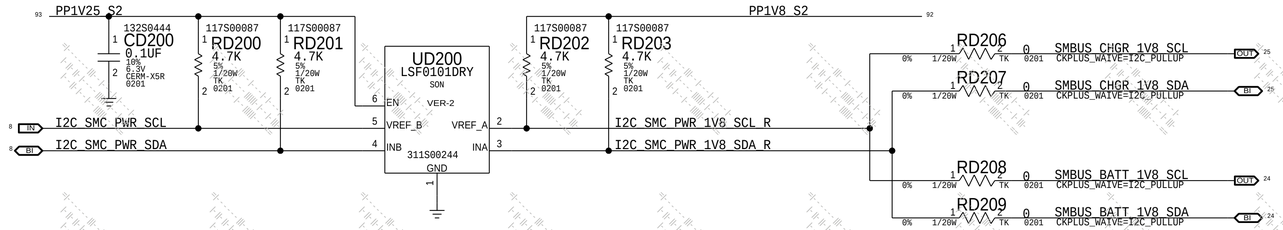
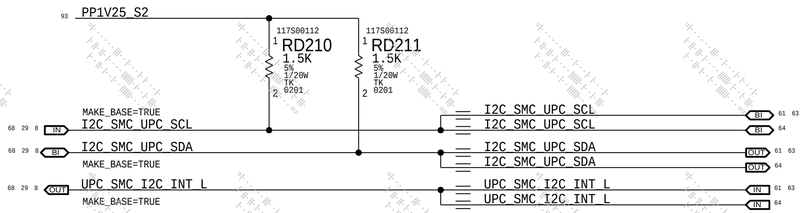
A SMC_I2C0 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	0	100 kHz	0X09	0X13	Whamola Charger
SMC	0	100 kHz	0X0B	0X16	Battery BMU
SMC	0	100 kHz	0X40	0X81	INA233 - U202
SMC	0	100 kHz	0X44	0X89	INA233 - U203
SMC	0	100 kHz	0X45	0X8B	INA233 - U201



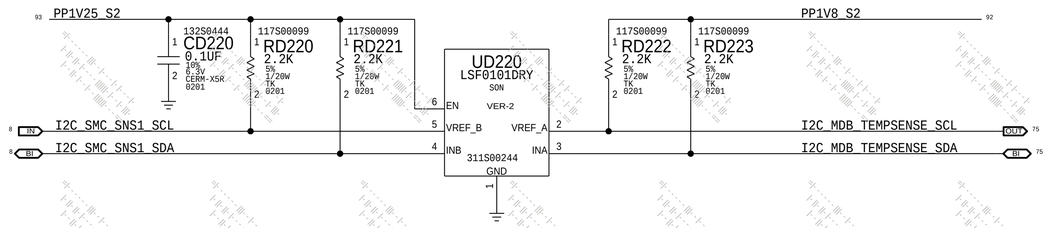
B SMC_I2C1 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	1	400 kHZ	0X38	0X71	ACE2 - 0
SMC	1	400 kHZ	0X3F	0X7F	ACE2 - 1
SMC	1	400 kHZ	0X3A	0X75	ACE2 - MagSafe



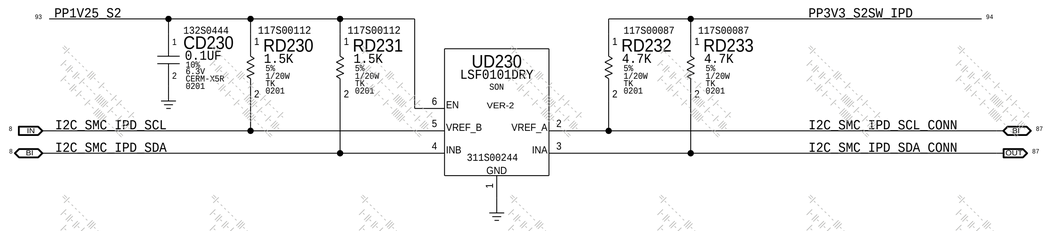
C SMC_I2C2 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	2	100 kHZ	0X48	0X91	MDB - TMP468



D SMC_I2C3 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	3	100 kHZ	0X4C	0X99	PALM - TempSense



E SMC_I2C4 - I2C Interface (Unused)

BOM_COST_GROUP=SENSORS

$SYNC_MASTER=jwen01 $SYNC_DATE=09/28/2021

PAGE TITLE: I2C: SMC

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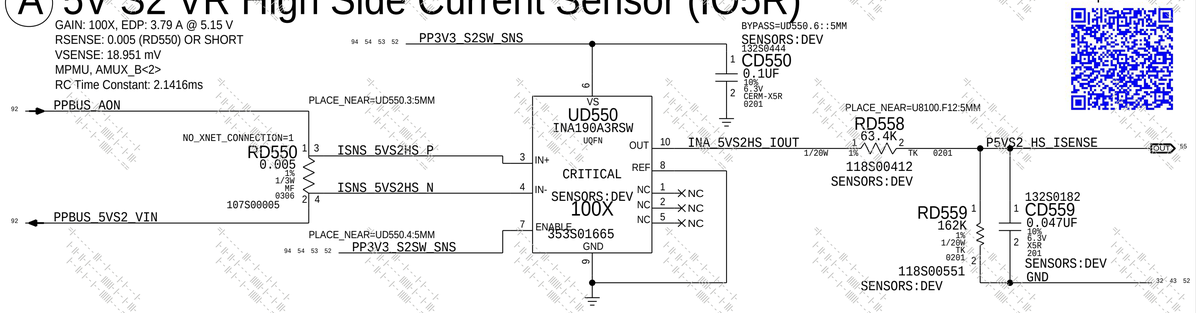
A 5V S2 VR High Side Current Sensor (IO5R)

GAIN: 100X, EDP: 3.79 A @ 5.15 V
RSENSE: 0.005 (RD550) OR SHORT
VSENSE: 18.951 mV
MPMU, AMUX_B<2>
RC Time Constant: 2.1416ms

LTSpice:

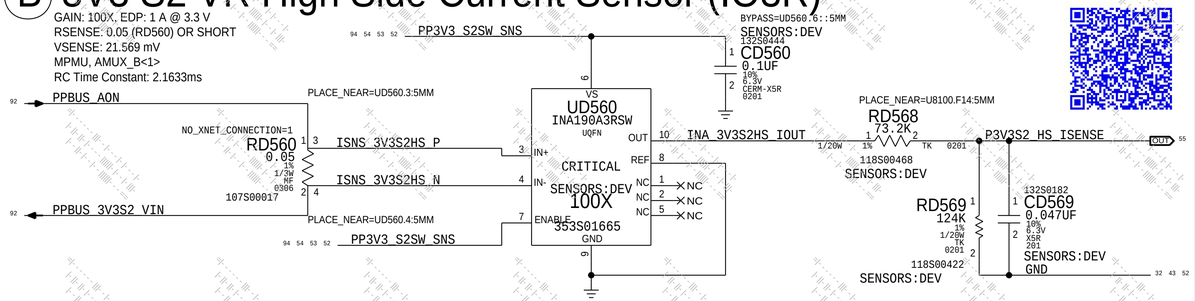


$X2203GHUB/mlb/sim/ltspice/io5r_p5vs2_hs_isense/io5r_p5vs2_hs_isense.asc

B 3V3 S2 VR High Side Current Sensor (IO3R)

GAIN: 100X, EDP: 1 A @ 3.3 V
RSENSE: 0.05 (RD560) OR SHORT
VSENSE: 21.569 mV
MPMU, AMUX_B<1>
RC Time Constant: 2.1633ms

LTSpice:

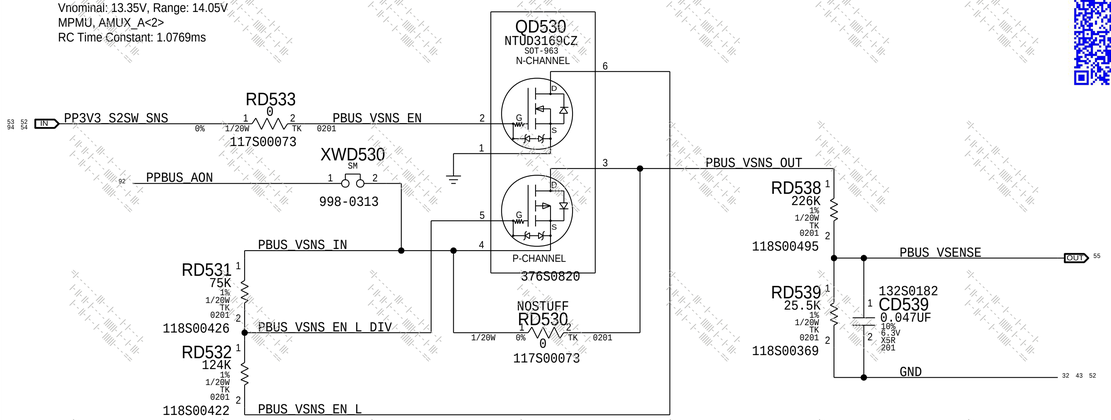


$X2203GHUB/mlb/sim/ltspice/io3r_p3v3s2_hs_isense/io3r_p3v3s2_hs_isense.asc

C PPBUS Voltage Sensor (VP0R)

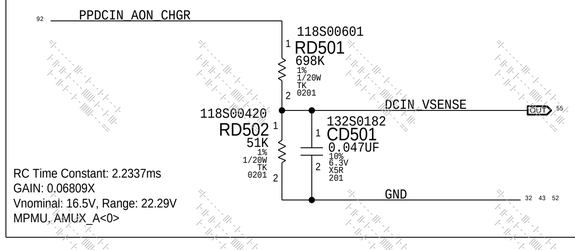
GAIN: 0.1014X
Vnominal: 13.35V, Range: 14.05V
MPMU, AMUX_A<2>
RC Time Constant: 1.0769ms

LTSpice:



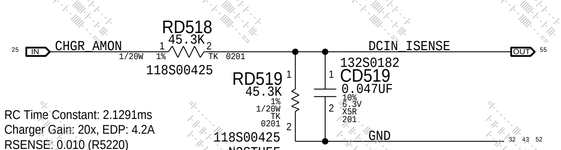
$X2203GHUB/mlb/sim/ltspice/vp0r_sense/vp0r_pbus_vsense_pulse_diodesinc.asc
$X2203GHUB/mlb/sim/ltspice/vp0r_sense/vp0r_pbus_vsense_pulse_onsemi.asc

D DCIN Voltage Sensor (VD0R)



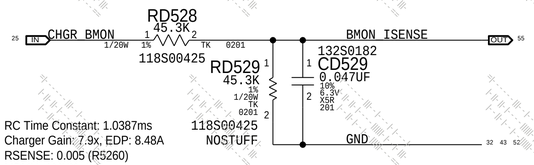
RC Time Constant: 2.2337ms
GAIN: 0.06809X
Vnominal: 16.5V, Range: 22.29V
MPMU, AMUX_A<0>

E DCIN Current Sensor (ID0R)



RC Time Constant: 2.1291ms
Charger Gain: 20x, EDP: 4.2A
RSENSE: 0.010 (R5220)
MPMU, AMUX_A<1>

F BMON Current Sensor (IPBR)



RC Time Constant: 1.0387ms
Charger Gain: 7.9x, EDP: 8.48A
RSENSE: 0.005 (R5260)
MPMU, AMUX_A<3>

G Production Sensor BOM Table

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S00095	1	RES,TK,100K OHM,5%,,1/20W,0201	RD559		SENSORS:PROD
117S00095	1	RES,TK,100K OHM,5%,,1/20W,0201	RD569		SENSORS:PROD

BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: POWER HIGH SIDE (1/2)

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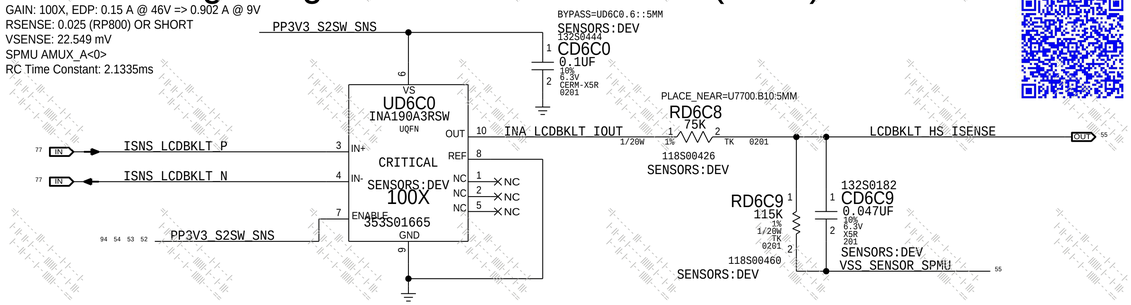
A LCD Backlight High Side Current Sensor (IBLR)

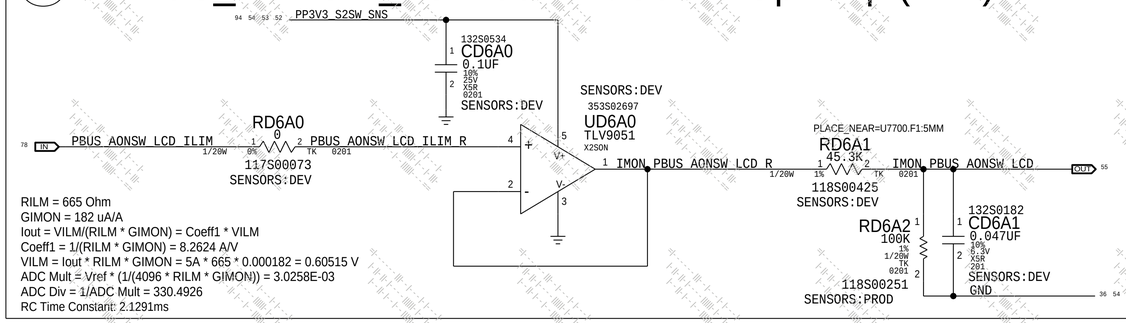
GAIN: 100X, EDP: 0.15 A @ 46V => 0.902 A @ 9V
RSENSE: 0.025 (RP800) OR SHORT
VSENSE: 22.549 mV
SPMU AMUX_A<0>
RC Time Constant: 2.1335ms

LTSpice:



$X2203GHUB/mlb/sim/ltspice/iblr_lcdbklt_hs_isense/iblr_lcdbklt_hs_isense.asc

B PPBUS_AONSW_LCD Current Sense Op-Amp (IBlR)



RILM = 665 Ohm
GIMON = 182 uA/A
Iout = VILM/(RILM * GIMON) = Coeff1 * VILM
Coeff1 = 1/(RILM * GIMON) = 8.2624 A/V
VILM = Iout * RILM * GIMON = 5A * 665 * 0.000182 = 0.60515 V
ADC Mult = Vref * (1/(4096 * RILM * GIMON)) = 3.0258E-03
ADC Div = 1/ADC Mult = 330.4926
RC Time Constant: 2.1291ms

C Production Sensor BOM Table

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S00095	1	RES,TK,100K OHM,5%,,1/20W,0201	RD6C9		SENSORS:PROD

BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: POWER HIGH SIDE (2/2)

Apple Inc.

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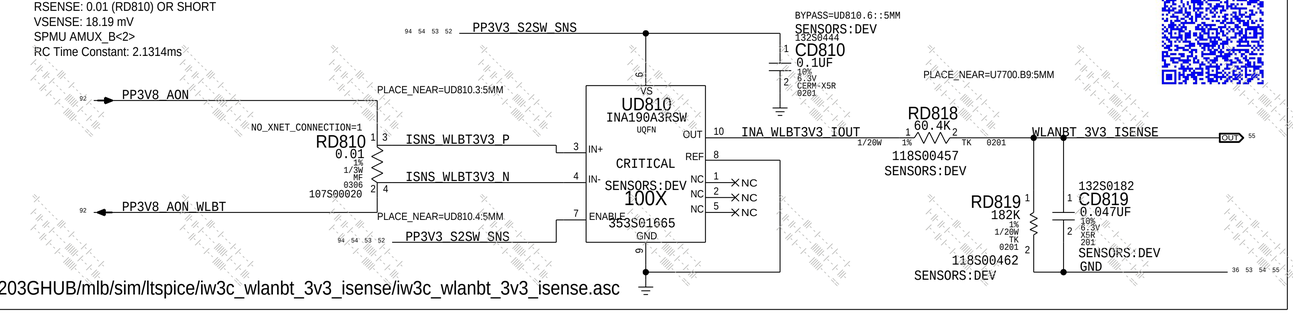
A WLAN BT 3V8 AON Current Sensor (IW3C)

GAIN: 100X, EDP: 1.819 A @ 3.8 V
RSENSE: 0.01 (RD810) OR SHORT
VSENSE: 18.19 mV
SPMU AMUX_B<2>
RC Time Constant: 2.1314ms

LTSpice:

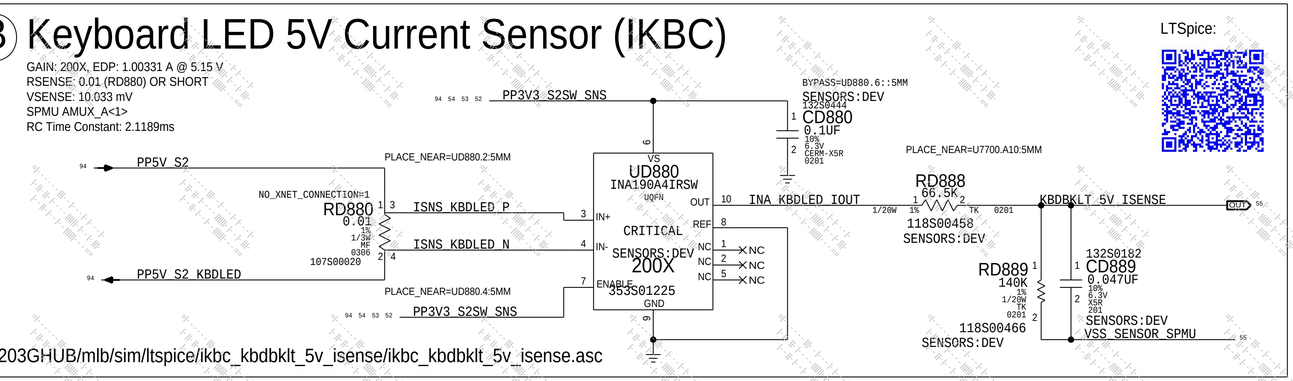


$X2203GHUB/mlb/sim/ltspice/iw3c_wlanbt_3v3_isense/iw3c_wlanbt_3v3_isense.asc

B Keyboard LED 5V Current Sensor (IKBC)

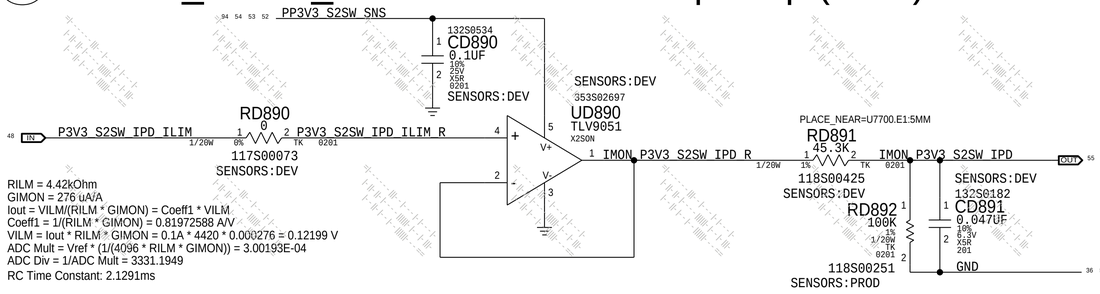
GAIN: 200X, EDP: 1.00331 A @ 5.15 V
RSENSE: 0.01 (RD880) OR SHORT
VSENSE: 10.033 mV
SPMU AMUX_A<1>
RC Time Constant: 2.1189ms

LTSpice:



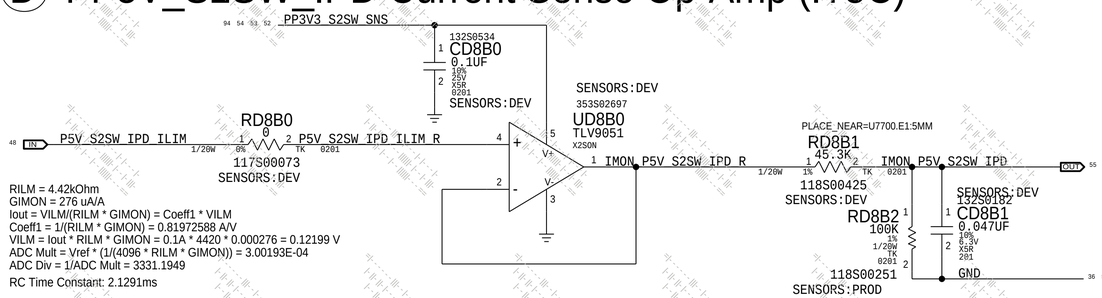
$X2203GHUB/mlb/sim/ltspice/ikbc_kbdbklt_5v_isense/ikbc_kbdbklt_5v_isense.asc

C PP3V3_S2SW_IPD Current Sense Op-Amp (IT3C)



RILM = 4.42kOhm
GIMON = 276 uA/A
Iout = VILM/(RILM * GIMON) = Coeff1 * VILM
Coeff1 = 1/(RILM * GIMON) = 0.81972588 A/V
VILM = Iout * RILM * GIMON = 0.1A * 4420 * 0.000276 = 0.12199 V
ADC Mult = Vref * (1/(4096 * RILM * GIMON)) = 3.00193E-04
ADC Div = 1/ADC Mult = 3331.1949
RC Time Constant: 2.1291ms

D PP5V_S2SW_IPD Current Sense Op-Amp (IT5C)



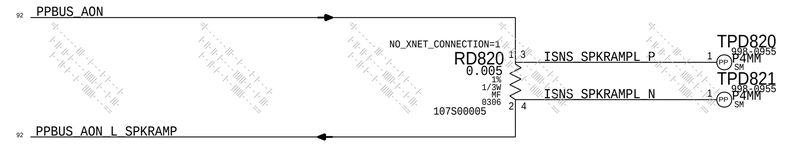
RILM = 4.42kOhm
GIMON = 276 uA/A
Iout = VILM/(RILM * GIMON) = Coeff1 * VILM
Coeff1 = 1/(RILM * GIMON) = 0.81972588 A/V
VILM = Iout * RILM * GIMON = 0.1A * 4420 * 0.000276 = 0.12199 V
ADC Mult = Vref * (1/(4096 * RILM * GIMON)) = 3.00193E-04
ADC Div = 1/ADC Mult = 3331.1949
RC Time Constant: 2.1291ms

E Right Speaker Amplifier Current Sensor (Ixxx)

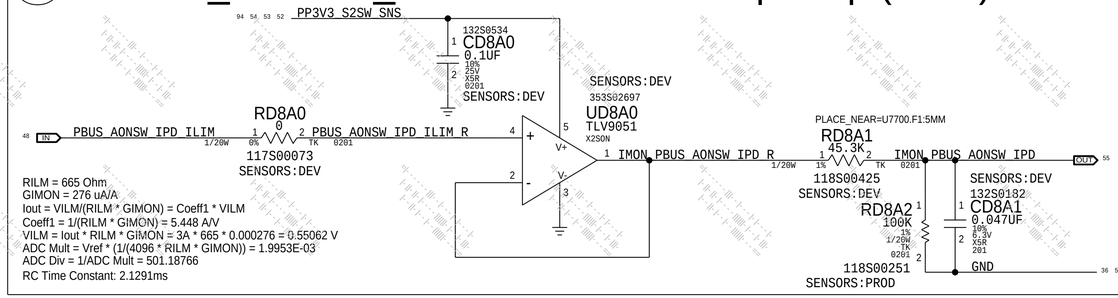
GAIN: 100X, EDP: 2.6 A
RSENSE: 0.005 (RD820) OR SHORT
VSENSE: 13 mV, RANGE: 3.3 A

F Left Speaker Amplifier Current Sensor (Ixxx)

GAIN: 100X, EDP: 2.6 A
RSENSE: 0.005 (RD820) OR SHORT
VSENSE: 13 mV, RANGE: 3.3 A



G PPBUS_AONSW_IPD Current Sense Op-Amp (ITPR)



RILM = 665 Ohm
GIMON = 276 uA/A
Iout = VILM/(RILM * GIMON) = Coeff1 * VILM
Coeff1 = 1/(RILM * GIMON) = 5.448 A/V
VILM = Iout * RILM * GIMON = 3A * 665 * 0.000276 = 0.55062 V
ADC Mult = Vref * (1/(4096 * RILM * GIMON)) = 1.9953E-03
ADC Div = 1/ADC Mult = 501.18766
RC Time Constant: 2.1291ms

H Production Sensor BOM Table

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S00095	1	RES,TK,100K OHM,5%,,1/20W,0201	RD819		SENSORS:PROD
117S00095	1	RES,TK,100K OHM,5%,,1/20W,0201	RD889		SENSORS:PROD

BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: POWER LOW SIDE (1/2)

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A ADC Input Aliases

MASTER PMU AMUX ALIAS

52	IN	DCIN_VSENSE (MAKE_BASE=TRUE)	DCIN_VSENSE	OUT	41
52	IN	DCIN_ISENSE (MAKE_BASE=TRUE)	DCIN_ISENSE	OUT	41
52	IN	PBUS_VSENSE (MAKE_BASE=TRUE)	PBUS_VSENSE	OUT	41
52	IN	BMON_ISENSE (MAKE_BASE=TRUE)	BMON_ISENSE	OUT	41
32	IN	P3V8AON_IMEAS (MAKE_BASE=TRUE)	P3V8AON_IMEAS	OUT	41
52	IN	P3V3S2_HS_ISENSE (MAKE_BASE=TRUE)	P3V3S2_HS_ISENSE	OUT	41
52	IN	P5VS2_HS_ISENSE (MAKE_BASE=TRUE)	P5VS2_HS_ISENSE	OUT	41
55		MPMU_AMUXTDEV_TERM (MAKE_BASE=TRUE)	MPMU_AMUXTDEV_TERM	OUT	41

SLAVE PMU AMUX ALIAS

53	IN	LCDBKLT_HS_ISENSE (MAKE_BASE=TRUE)	LCDBKLT_HS_ISENSE	OUT	35
54	IN	KBDBKLT_5V_ISENSE (MAKE_BASE=TRUE)	KBDBKLT_5V_ISENSE	OUT	35
54	IN	IMON_PBUS_AONSW_IPD (MAKE_BASE=TRUE)	IMON_PBUS_AONSW_IPD	OUT	35
54	IN	IMON_P3V3_S2SW_IPD (MAKE_BASE=TRUE)	IMON_P3V3_S2SW_IPD	OUT	35
53	IN	IMON_PBUS_AONSW_LCD (MAKE_BASE=TRUE)	IMON_PBUS_AONSW_LCD	OUT	35
56	IN	IMON_P5V_S2SW_IPD (MAKE_BASE=TRUE)	IMON_P5V_S2SW_IPD	OUT	35
54	IN	WLANBT_3V3_ISENSE (MAKE_BASE=TRUE)	WLANBT_3V3_ISENSE	OUT	35
55		SPMU_AMUXTDEV_TERM (MAKE_BASE=TRUE)	SPMU_AMUXTDEV_TERM	OUT	35

B SOC Sense Lines

102	VSNS_VDD_PCPU	PPE0A1	P4MM SM 1 PP
102	VSNS_VSS_PCPU	PPE0A2	P4MM SM 1 PP
102	VSNS_VDD_GPU	PPE0A3	P4MM SM 1 PP
102	VSNS_VDD_SOC	PPE0A4	P4MM SM 1 PP
102	VSNS_VDD_ECPU	PPE0A5	P4MM SM 1 PP
102	VSNS_VDD_DISP	PPE0A6	P4MM SM 1 PP
102	VSNS_ABSMIN_PCPU	PPE0A7	P4MM SM 1 PP
102	VSNS_VSS_1	PPE0A8	P4MM SM 1 PP
102	VSNS_VDD2H_1	PPE0A9	P4MM SM 1 PP
102	VSNS_VSS_2	PPE0AA	P4MM SM 1 PP
102	VSNS_VDD2H_2	PPE0AB	P4MM SM 1 PP
102	VSNS_VDDQ_S1	PPE0AC	P4MM SM 1 PP
16	VDD_DCS_S1_SENSE	PPE0B0	P4MM SM 1 PP
18	VDD_AMPH_S2_SENSE	PPE0B1	P4MM SM 1 PP
18	VDD_VDDQ_S1_SENSE	PPE0B2	P4MM SM 1 PP

PPE0AE: P4MM SM 1 PP — PLACE_NEAR=PPE0A3:2MM

PPE0AF: P4MM SM 1 PP

998-0955

C Unused MPMU AMUX/TDEV Termination

RECOMMENDED NOT TO LEAVE AMUX/TDEV FLOATING.

55 MPMU_AMUXTDEV_TERM
56 MPMU_AMUXTDEV_TERM
→ MPMU_AMUXTDEV_TERM (MAKE_BASE=TRUE)
RE010 100K 5% 1/20W TK 0201 117S00095

D Unused SPMU AMUX/TDEV Termination

RECOMMENDED NOT TO LEAVE AMUX/TDEV FLOATING.

55 SPMU_AMUXTDEV_TERM
56 SPMU_AMUXTDEV_TERM
56 SPMU_AMUXTDEV_TERM
→ SPMU_AMUXTDEV_TERM (MAKE_BASE=TRUE)
RE020 100K 5% 1/20W TK 0201 117S00095

E I/V Sensor Ground Reference Aliases

Slave PMU ADC Ground Alias

54 VSS_SENSOR_SPMU
53 VSS_SENSOR_SPMU
→ VSS_SENSOR_SPMU (MAKE_BASE=TRUE)
XWE020 SM 1 2 GND
36 53 54

BOM_COST_GROUP=SENSORS

PAGE TITLE: SENSORS: POWER SUPPORT

Apple Inc.

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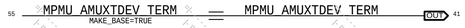
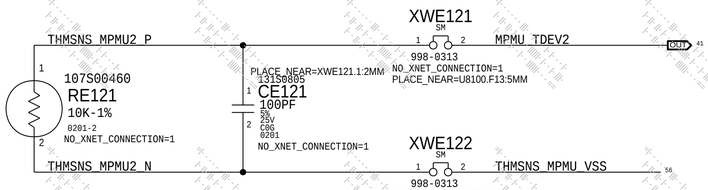
A Master PMU TDEV1 (Txxx)

Location: TBD



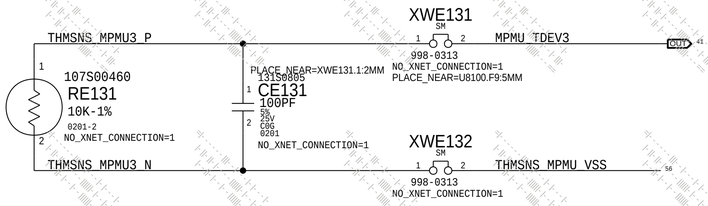
B Master PMU TDEV2 (Tm0B)

Location: Ambient



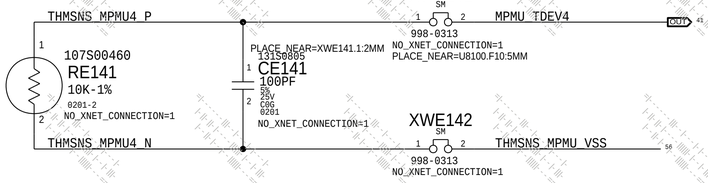
C Master PMU TDEV3 (TIOP)

Location: Thunderbolt Proximity

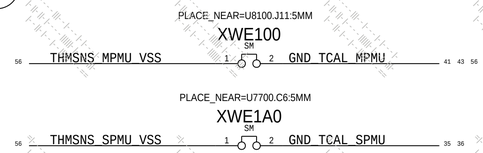


D Master PMU TDEV4 (TW0P)

Location: Wireless Proximity

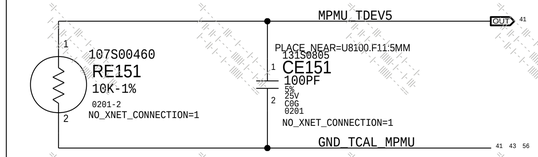


E Master/Slave PMU VSS Connection



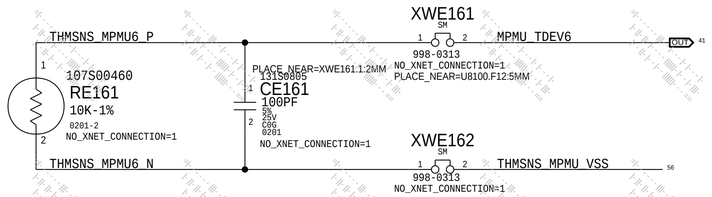
F Master PMU TDEV5 (TPMP)

Location: Master PMU Proximity



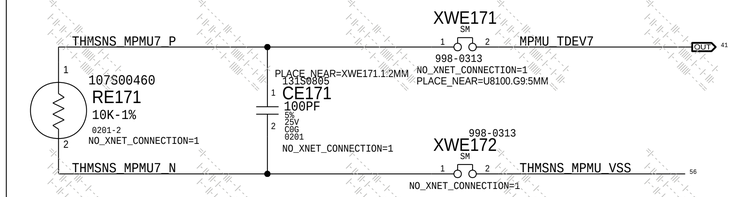
G Master PMU TDEV6 (T5SP)

Location: PP5V_S2 (UC300)



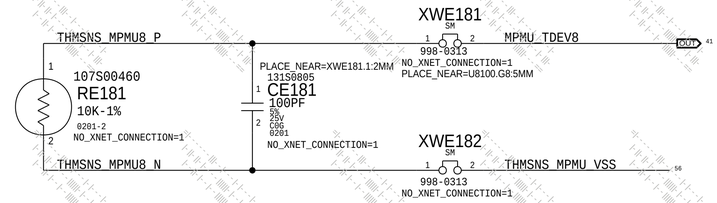
H Master PMU TDEV7 (TCHP)

Location: Charger Proximity



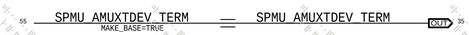
I Master PMU TDEV8 (TMVR)

Location: Main VR (PP3V8_AON_VDDMAIN)



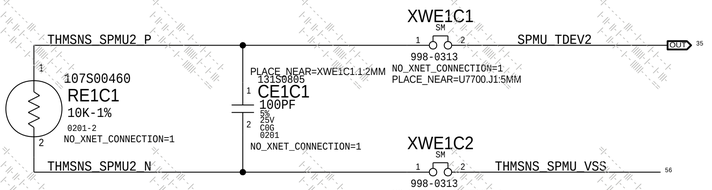
J Slave PMU TDEV1 (Txxx)

Location: TBD



K Slave PMU TDEV2 (TH0T)

Location: NAND Proximity

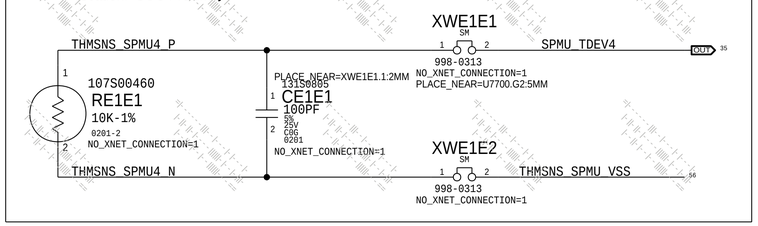


L Slave PMU TDEV3 (Txxx)

Location: TBD

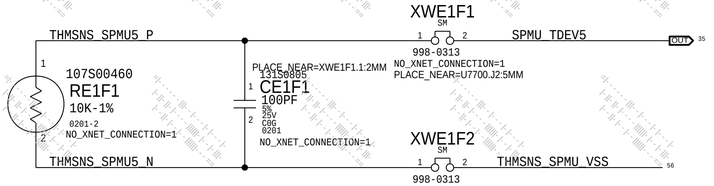
M Slave PMU TDEV4 (TSCD)

Location: SOC Proximity



N Slave PMU TDEV5 (TPSP)

Location: Slave PMU Proximity



BOM_COST_GROUP=SENSORS

SYNC_DATE=09/10/2021

PAGE TITLE: SENSORS: THERMAL

Apple Inc.

DRAWING NUMBER: 051-07020

SIZE: D

REVISION: 6.0.0

BRANCH: evt-1

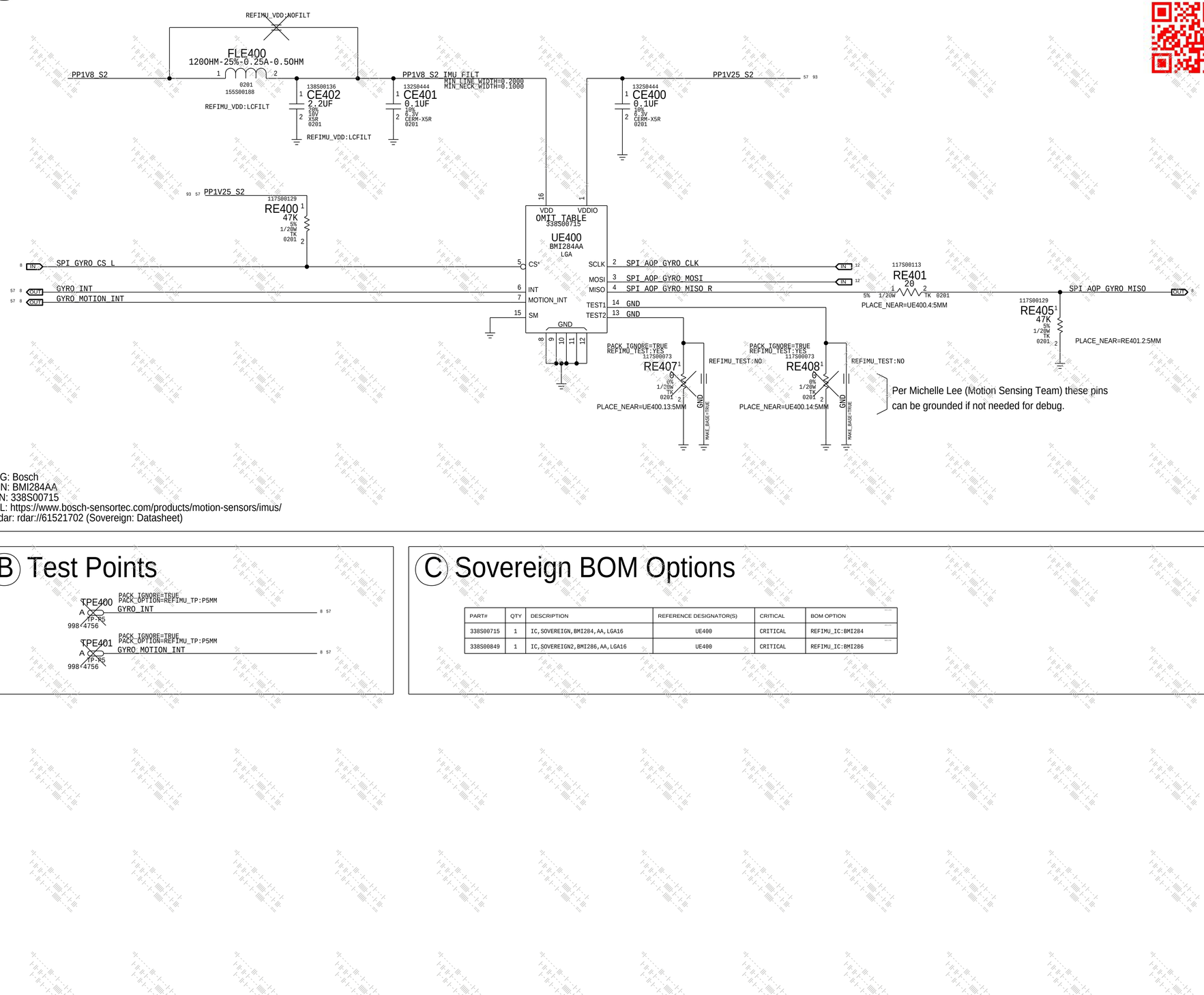
PAGE: 141 OF 801

SHEET: 56 OF 113

*** OK2INTEGRATE ***

A Sovereign Accelerometer and Gyroscope

Datasheet Radar:



MFG: Bosch
MPN: BMI284AA
APN: 338S00715
URL: https://www.bosch-sensortec.com/products/motion-sensors/imus/
Radar: rdar://61521702 (Sovereign: Datasheet)

B Test Points

C Sovereign BOM Options

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00715	1	IC,SOVEREIGN,BMI284,AA,LGA16	UE400	CRITICAL	REFIMU_IC:BMI284
338S00849	1	IC,SOVEREIGN2,BMI286,AA,LGA16	UE400	CRITICAL	REFIMU_IC:BMI286

BOM_COST_GROUP=SENSORS

PAGE TITLE: SENSORS: MOTION

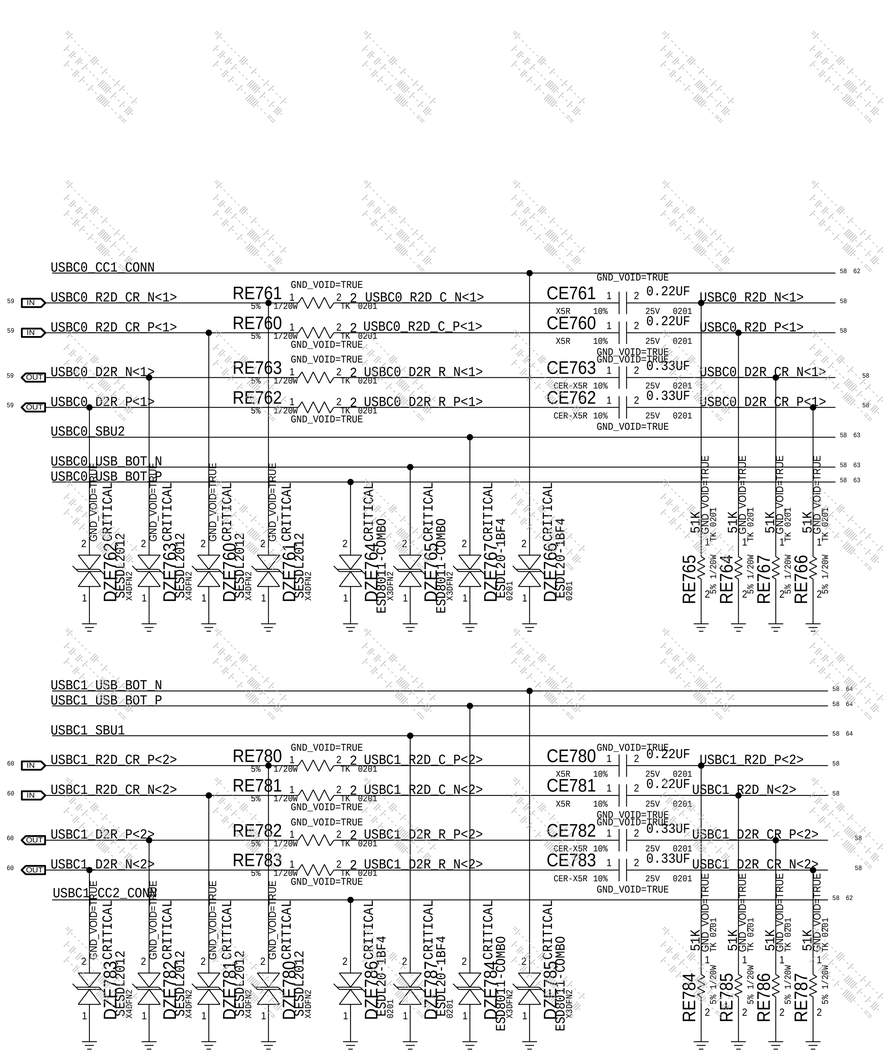
Apple Inc.

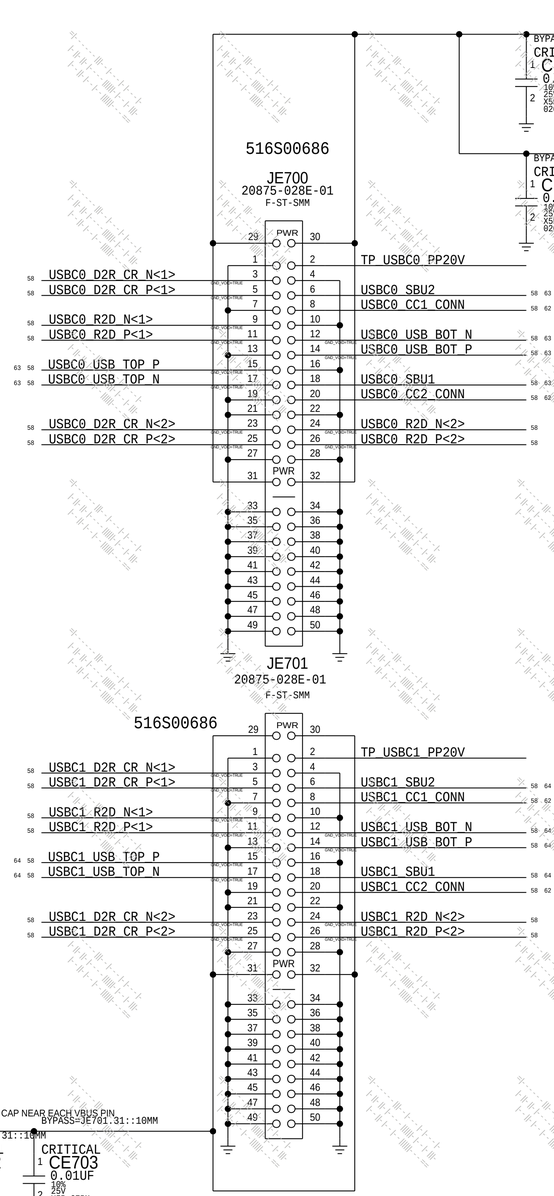
DRAWING NUMBER: 051-07020
SIZE: D
REVISION: 6.0.0
BRANCH: evt-1
PAGE: 144 OF 801
SHEET: 57 OF 113

---- Reference only ----

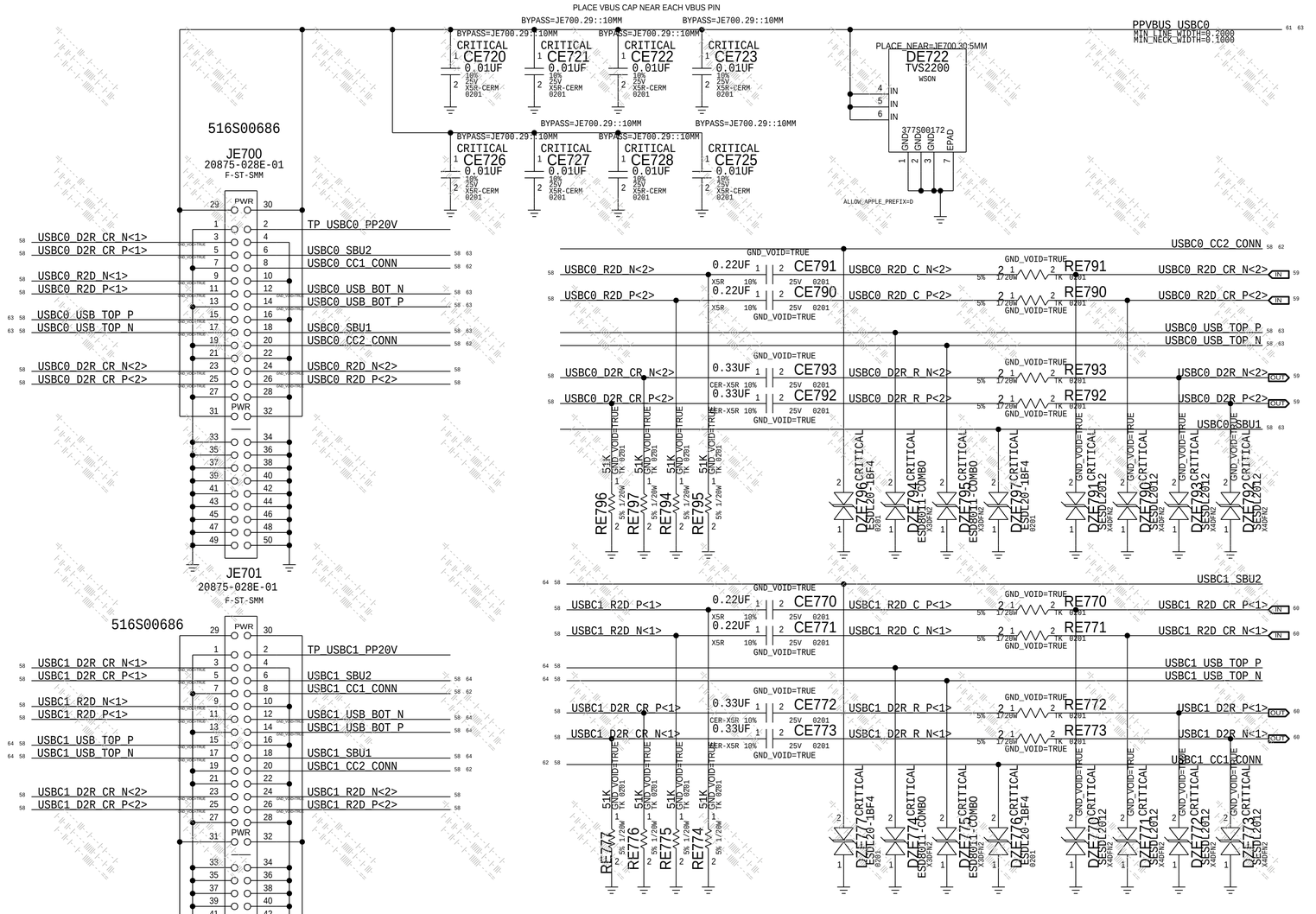
Left Rear Port

FOR POR, VERIFY 20% TOLERANCE ON 0.22UF AC COUPLING CAP IS OK

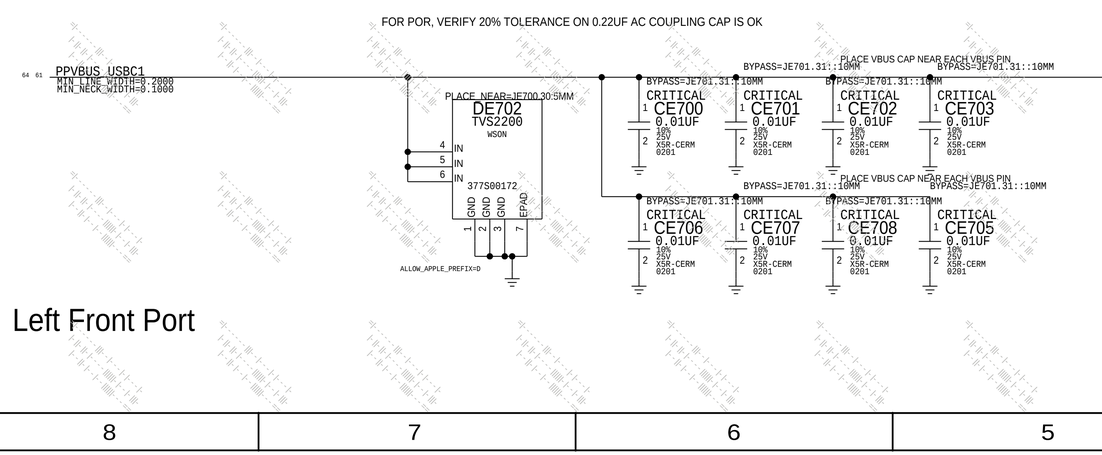




PLACE VBUS CAP NEAR EACH VBUS PIN



FOR POR, VERIFY 20% TOLERANCE ON 0.22UF AC COUPLING CAP IS OK



Left Front Port

BOM_COST_GROUP=USB-C

SYNC_MASTER/ SYNC_DATE=05/10/2021

PAGE TITLE: USB-C: Connector(s)

Apple Inc.

DRAWING NUMBER: 051-07020 | SIZE: D

REVISION: 6.0.0

BRANCH: evt-1

PAGE: 147 OF 801

SHEET: 58 OF 113

*** OK2INTEGRATE ***

No lane swapping is allowed

Re-timer to SOC connections are set

Re-timer to connector connections are set

USBC HIGH-SPEED AC COUPLING

IN	USBC_ATC0_R2D_C_P<1>	CF020 0.22UF	USBC_ATC0_R2D_P<1>		59
IN	USBC_ATC0_R2D_C_N<1>	CF021 0.22UF	USBC_ATC0_R2D_N<1>		59
IN	USBC_ATC0_R2D_C_P<2>	CF024 0.22UF	USBC_ATC0_R2D_P<2>		59
IN	USBC_ATC0_R2D_C_N<2>	CF025 0.22UF	USBC_ATC0_R2D_N<2>		59
BI	USBC_ATC0_D2R_P<1>	CF022 0.22UF	USBC_ATC0_D2R_C_P<1>		59
BI	USBC_ATC0_D2R_N<1>	CF023 0.22UF	USBC_ATC0_D2R_C_N<1>		59
BI	USBC_ATC0_D2R_P<2>	CF026 0.22UF	USBC_ATC0_D2R_C_P<2>		59
BI	USBC_ATC0_D2R_N<2>	CF027 0.22UF	USBC_ATC0_D2R_C_N<2>		59

All: GND_VOID=TRUE; 0.22UF 10% 6.3V X5R 0201

PP1V2_USBC_VDDIO — 59 62 68 95

RF045 47K 5% 1/20W TK 0201 — ATCRTMR0_JTAG_TDO — 59

ATCRTMR0_XTAL24M_OUT — 59

RF060 499 1% 1/20W TK 0201

197S0591 CRITICAL YF000 1.6X1.2MM 24.000MHZ-20PPM-9.5PF-60OHM

ATC0_24M_O_R

ATCRTMR0_XTAL24M_IN — 59

CRITICAL CF060 15PF 5% 50V C0G 0201

CRITICAL 131S0831 CF061 15PF 5% 50V C0G 0201

PP0V855_USBC_CIO — 95

CF030 14UF 20% 4V X5R 0402-D2X-1 — 138S00149

CF031 14UF 20% 4V X5R 0402-D2X-1

CF032 0.1UF 10% 6.3V X6S 0201

CF033 0.1UF 10% 6.3V X6S 0201

PP0V805_USBC_FIXED — 95 59

CF040 0.1UF 10% 6.3V X6S 0201

CF041 0.1UF 10% 6.3V X6S 0201

CF042 2.2UF 20% 4V X6S-CERM 0201

CF043 2.2UF 20% 4V X6S-CERM 0201

CF044 2.2UF 20% 4V X6S-CERM 0201

CF045 14UF 20% 4V X5R 0402-D2X-1

CF046 14UF 20% 4V X5R 0402-D2X-1

PP0V805_USBC_FIXED — 95 59

CF050 0.1UF 10% 6.3V X6S 0201

PLACE_NEAR=UF000.G7:5MM

PPVDD_FIXED_ATCRTMR0_XTAL_R

RF051 10 5% 1/20W TK 0201 — VOLTAGE=0.805V

PP0V805_USBC_FIXED — 95

CF051 4UF 20% 2.5V X6S 0201 — 138S00329

117S00094

UF000 TMNB25B0-C1 FCCSP 99B-25504 SYM 2 OF 2

OMIT_TABLE CRITICAL

J4	VDD_CIO_0	VDDIO12_CIO_0	K5
J6	VDD_CIO_0	VDDIO12_CIO_0	K7
J8	VDD_CIO_0	VDDIO12_CIO_0	L6
F4	VDD_CIO_1	VDDIO12_CIO_1	D6
F6	VDD_CIO_1	VDDIO12_CIO_1	E5
F8	VDD_CIO_1	VDDIO12_CIO_1	E7
G4	VDD_FIXED	VDDIO12_PLL_SOC0	K8
G5	VDD_FIXED	VDDIO12_PLL_SOC1	H8
H5	VDD_FIXED	VDDIO12_XTAL	H9
H6	VDD_FIXED	VDDIO12	E9
G7	VDD_FIXED_PLL	VDDIO12	H3
G9	VDD_FIXED_XTAL	VDDIO12	K9
		VDDIO12_EFUSE1	F3
		VDDIO12_AMUX	F7

VSS: A1 A2 A4 A6 A8 A10 A11 B2 B4 B6 B8 B10 C3 C5 C6 C7 C9 D1 D5 D7 D11 E3 E4 E6 E8 F2 F5 F10 G3 G6 G8

VSS: H4 H7 J2 J3 J5 J7 J10 K4 K6 L1 L5 L7 L11 M3 M5 M6 M7 M9 N2 N4 N6 N8 N10 P1 P2 P4 P6 P8 P10 P11

132S0395 CF034 0.1UF 10% 6.3V X6S 0201

138S00039 CF035 2.2UF 20% 4V X6S-CERM 0201

CF036 14UF 20% 4V X5R 0402-D2X-1

CF037 14UF 20% 4V X5R 0402-D2X-1

PP1V2_USBC_VDDIO — 59 62 68 95

138S00039 CF052 2.2UF 20% 4V X6S-CERM 0201 — PLACE_NEAR=UF000.K8:5MM

PP1V2_USBC_VDDIO — 95

PP1V2_ATCRTMR0_VDDIO_XTAL_F — VOLTAGE=1.2V

155S0644 FLF000 240-OHM-0.2A-0.9-OHM 0201

PP1V2_USBC_VDDIO — 95

CF062 0.1UF 10% 6.3V X6S 0201 — 132S0395

CF063 2.2UF 20% 4V X6S-CERM 0201 — 138S00039

Connect to GND directly or via a resistor

ATCRTMR0_VDDIO_EFUSE — 68 97

PP1V2_USBC_VDDIO — 95

132S0395 CF064 0.1UF 10% 6.3V X6S 0201

CF011 10PF 5% 25V C0G 0201

ATCRTMR0_CFP_RCAL_NEG — 59

RF011 200 1% 1/20W TB 0201-1

ATCRTMR0_CFP_RCAL_POS — 59

CF010 10PF 5% 25V C0G 0201

ATCRTMR0_SFP_RCAL_NEG — 59

RF010 200 1% 1/20W TK 0201-1

ATCRTMR0_SFP_RCAL_POS — 59

UF000 TMNB25B0-C1 FCCSP OMIT_TABLE CRITICAL 998-25504 SYM 1 OF 2

	USBC_ATC0_D2R_C_P<1>	P9	SFP_PHY_RXTX_0_P	SFP PHY	
	USBC_ATC0_D2R_C_N<1>	N9	SFP_PHY_RXTX_0_N		
	USBC_ATC0_D2R_C_P<2>	P5	SFP_PHY_RXTX_2_P		
	USBC_ATC0_D2R_C_N<2>	N5	SFP_PHY_RXTX_2_N		
	USBC_ATC0_R2D_P<1>	P7	SFP_PHY_RXTX_1_P		
	USBC_ATC0_R2D_N<1>	N7	SFP_PHY_RXTX_1_N		
	USBC_ATC0_R2D_P<2>	P3	SFP_PHY_RXTX_3_P		
	USBC_ATC0_R2D_N<2>	N3	SFP_PHY_RXTX_3_N		
BI	USBC_ATC0_AUX_C_P	L4	SFP_LPDP_AUX_P	CFP PHY	
BI	USBC_ATC0_AUX_C_N	M4	SFP_LPDP_AUX_N		
IN	CIO_ATC0_LSTX	G1	USB4_SFP_SB_RX		
OUT	CIO_ATC0_LSRX	G2	USB4_SFP_SB_TX		
	ATCRTMR0_SFP_RCAL_POS	M8	SFP_PHY_RCAL_P		
	ATCRTMR0_SFP_RCAL_NEG	L8	SFP_PHY_RCAL_N		
IN	ATCRTMR0_CHIPID_0	M1	CHIP_ID_0	GPIO PERIPHERAL	
IN	ATCRTMR0_CHIPID_1	N1	CHIP_ID_1		
IN	ATCRTMR0_BOOT_CONFIG0	H2	BOOT_CONFIG0		
IN	ATCRTMR0_BOOT_CONFIG1	J1	BOOT_CONFIG1		
IN	ATCRTMR0_BOOT_CONFIG2	K1	BOOT_CONFIG2		
IN	ATCRTMR0_FORCE_DFU	C1	FORCE_DFU		
	TP_ATCRTMR0_GPIO_0	K2	GPIO0		
	NC_ATCRTMR0_GPIO_1 (NO_TEST=1)	L3	GPIO1		
	TP_ATCRTMR0_GPIO_2	K3	GPIO2		
	TP_ATCRTMR0_GPIO_3	L10	GPIO3		
IN	ATCRTMR0_COLD_RESET_L	L2	COLD_RESET*	CLOCKS AND RESET	
IN	ATCRTMR0_CFSB	M2	CFSB		
	ATCRTMR0_XTAL24M_IN	F11	XI0		
	ATCRTMR0_XTAL24M_OUT	E11	XO0		
OUT	USBC0_R2D_CR_P<1>	A9	CFP_PHY_RXTX_0_P	SFP PHY	
OUT	USBC0_R2D_CR_N<1>	B9	CFP_PHY_RXTX_0_N		
OUT	USBC0_R2D_CR_P<2>	A5	CFP_PHY_RXTX_2_P		
OUT	USBC0_R2D_CR_N<2>	B5	CFP_PHY_RXTX_2_N		
BI	USBC0_D2R_P<1>	A7	CFP_PHY_RXTX_1_P		
BI	USBC0_D2R_N<1>	B7	CFP_PHY_RXTX_1_N		
BI	USBC0_D2R_P<2>	A3	CFP_PHY_RXTX_3_P		
BI	USBC0_D2R_N<2>	B3	CFP_PHY_RXTX_3_N		
BI	USBC0_AUX_P	D4	CFP_LPDP_AUX_P	CFP PHY	
BI	USBC0_AUX_N	C4	CFP_LPDP_AUX_N		
IN	USBC0_CIO_LSRX	F1	USB4_CFP_SB_RX		
BI	USBC0_CIO_LSTX	E1	USB4_CFP_SB_TX		
OUT	ATCRTMR0_LSTX_DIR	H1	USB4_CFP_SB_TX_DIR		
	ATCRTMR0_CFP_RCAL_POS	C8	CFP_PHY_RCAL_P		
	ATCRTMR0_CFP_RCAL_NEG	D8	CFP_PHY_RCAL_N		
	SPI_ATCRTMR0_CS_L	N11	QSPI_CS*	GPIO PERIPHERAL	
	SPI_ATCRTMR0_CLK	M11	QSPI_SCLK		
	SPI_ATCRTMR0_DIO<0>	K10	QSPI_DQ0		
	SPI_ATCRTMR0_DIO<1>	K11	QSPI_DQ1		
	SPI_ATCRTMR0_DIO<2>	J9	QSPI_DQ2		
	SPI_ATCRTMR0_DIO<3>	J11	QSPI_DQ3		
IN	I2C_ATCRTMR_SCL	C2	I2C0_SCL		49
BI	I2C_ATCRTMR_SDA	D3	I2C0_SDA		49
IN	I2C_UPC0_ATCRTMR0_SCL_1V2	E2	I2C1_SCL		97
BI	I2C_UPC0_ATCRTMR0_SDA_1V2	D2	I2C1_SDA		97
OUT	INT_I2C_UPC0_ATCRTMR0_L	B1	I2C1_INT		61 63 68
	ATCRTMR0_TESTMODE	L9	TESTMODE	CLOCKS AND RESET	
	SWD_NUB_ATCRTMR_SWCLK	B11	JTAG_SEL	TEST AND DEBUG	
BI	SWD_NUB_ATCRTMR_SWDIO	D10	JTAG_TCK		
	TP_ATCRTMR0_JTAG_TDI	D9	JTAG_TMS		
	ATCRTMR0_JTAG_TDO	C10	JTAG_TDI		
	ATCRTMR0_JTAG_TRESET	E10	JTAG_TDO		
	TP_ATCRTMR0_ANALOGMUX_OUT	F9	JTAG_TRST*		
	TP_ATCRTMR0_TST_CLKOUT	M10	ANALOGMUX_OUT		
	NC_ATCRTMR0_CLK_LVDS_P<0> (NO_TEST=1)	H10	TST_CLKOUT		
	NC_ATCRTMR0_CLK_LVDS_N<0> (NO_TEST=1)	H11	TST_CLK_LVDS_0_P		
	NC_ATCRTMR0_CLK_LVDS_P<1> (NO_TEST=1)	G11	TST_CLK_LVDS_0_N		
	NC_ATCRTMR0_CLK_LVDS_N<1> (NO_TEST=1)	G10	TST_CLK_LVDS_1_P		
			TST_CLK_LVDS_1_N		

RF097 33 1/20W 5% TK 0201 — SPI_ATCRTMR0_DIO<0> — SPI_ATCRTMR0_R_DIO<0> — 59

RF098 33 1/20W 5% TK 0201 — SPI_ATCRTMR0_DIO<1> — SPI_ATCRTMR0_R_DIO<1> — 59

PP1V2_USBC_VDDIO — 95

RF090 3.3K 5% 1/20W TK 0201

NOSTUFF RF091 3.3K 5% 1/20W TK 0201

NOSTUFF RF092 3.3K 5% 1/20W TK 0201

NOSTUFF RF093 3.3K 5% 1/20W TK 0201

CF090 1.0UF 20% 6.3V X5R 0201-1

VCC OMIT_TABLE CRITICAL 335S00574 UF090 64MBIT-1.2V W25Q64NE XSON-1

SPI_ATCRTMR0_CLK	RF094 33	SPI_ATCRTMR0_CLK_R	6 CLK
SPI_ATCRTMR0_CS_L			1 CS*
SPI_ATCRTMR0_DIO<2>	RF095 33	SPI_ATCRTMR0_R_DIO<2>	3 WP*(IO2)
SPI_ATCRTMR0_DIO<3>	RF096 33	SPI_ATCRTMR0_R_DIO<3>	7 HOLD*(IO3)

DI(IO0) 5 SPI_ATCRTMR0_R_DIO<0> 59

DO(IO1) 2 SPI_ATCRTMR0_R_DIO<1> 59

GND 4 EPAD 9

RF047 47K 1/20W 5% — ATCRTMR0_JTAGL_SEL — 59

RF040 10K 1/20W 5% — ATCRTMR0_TESTMODE — 59

RF043 47K 1/20W 5% — CIO_ATC0_LSTX — 6 59 97

RF044 47K 1/20W 5% — CIO_ATC0_LSRX — 6 59 97

BOM_COST_GROUP=TBT

PAGE TITLE: USB-C: High Speed ATC0

Apple Inc.

DRAWING NUMBER: 051-07020 SIZE: D

REVISION: 6.0.0

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*** OK2INTEGRATE ***

No lane swapping is allowed
Re-timer to SOC connections are set

Re-timer to connector connections are set

USBC HIGH-SPEED AC COUPLING

USBC_ATC1_R2D_C_P<1>	CF120 0.22UF	USBC_ATC1_R2D_P<1>	USBC_ATC1_R2D_C_P<1>	CFP_PHY_RXTX_0_P	USBC1_R2D_CR_P<1>
USBC_ATC1_R2D_C_N<1>	CF121 0.22UF	USBC_ATC1_R2D_N<1>	USBC_ATC1_R2D_C_N<1>	CFP_PHY_RXTX_0_N	USBC1_R2D_CR_N<1>
USBC_ATC1_R2D_C_P<2>	CF124 0.22UF	USBC_ATC1_R2D_P<2>	USBC_ATC1_R2D_C_P<2>	CFP_PHY_RXTX_2_P	USBC1_R2D_CR_P<2>
USBC_ATC1_R2D_C_N<2>	CF125 0.22UF	USBC_ATC1_R2D_N<2>	USBC_ATC1_R2D_C_N<2>	CFP_PHY_RXTX_2_N	USBC1_R2D_CR_N<2>
USBC_ATC1_D2R_P<1>	CF122 0.22UF	USBC_ATC1_D2R_C_P<1>	USBC_ATC1_D2R_C_P<1>	CFP_PHY_RXTX_1_P	USBC1_D2R_P<1>
USBC_ATC1_D2R_N<1>	CF123 0.22UF	USBC_ATC1_D2R_C_N<1>	USBC_ATC1_D2R_C_N<1>	CFP_PHY_RXTX_1_N	USBC1_D2R_N<1>
USBC_ATC1_D2R_P<2>	CF126 0.22UF	USBC_ATC1_D2R_C_P<2>	USBC_ATC1_D2R_C_P<2>	CFP_PHY_RXTX_3_P	USBC1_D2R_P<2>
USBC_ATC1_D2R_N<2>	CF127 0.22UF	USBC_ATC1_D2R_C_N<2>	USBC_ATC1_D2R_C_N<2>	CFP_PHY_RXTX_3_N	USBC1_D2R_N<2>

PP1V2_USBC_VDDIO — RF145 47K 5% 1/20W TK 0201 — ATCRTMR1_JTAG_TDO

ATCRTMR1_XTAL24M_OUT — RF160 499 1% 1/20W TK 0201 — ATCRTMR1_XTAL24M_IN
YF100 197S0591 CRITICAL 1.6X1.2MM 24.000MHZ-20PPM-9.5PF-60OHM
ATC1_24M_O_R — CF160 15PF 5% 50V C0G 0201 — 131S0831 CF161 15PF 5% 50V C0G 0201

PP0V855_USBC_CIO — CF130 14UF 20% 4V X5R 0402-D2X-1 — CF131 14UF 20% 4V X5R 0402-D2X-1 — 138S00149
CF132 0.1UF 10% 6.3V X6S 0201 — CF133 0.1UF 10% 6.3V X6S 0201

PP0V805_USBC_FIXED — CF140 0.1UF 10% 6.3V X6S 0201 — CF141 0.1UF 10% 6.3V X6S 0201 — CF142 2.2UF 20% 4V X6S-CERM 0201 — CF143 2.2UF 20% 4V X6S-CERM 0201 — CF144 2.2UF 20% 4V X6S-CERM 0201
CF145 14UF 20% 4V X5R 0402-D2X-1 — CF146 14UF 20% 4V X5R 0402-D2X-1

PP0V805_USBC_FIXED — CF150 0.1UF 10% 6.3V X6S 0201 — PLACE_NEAR=UF100.G7:5MM

PPVDD_FIXED_ATCRTMR1_XTAL_R — RF151 10 5% 1/20W TK 0201 — 117S00094 — VOLTAGE=0.805V
PP0V805_USBC_FIXED — CF151 4UF 20% 2.5V X6S 0201 — 138S00329

UF100 TMNB25B0-C1 FCCSP 998-25504 SYM 2 OF 2
OMIT_TABLE CRITICAL

J4	VDD_CIO_0	VDDIO12_CIO_0	K5
J6	VDD_CIO_0	VDDIO12_CIO_0	K7
J8	VDD_CIO_0	VDDIO12_CIO_0	L6
F4	VDD_CIO_1	VDDIO12_CIO_1	D6
F6	VDD_CIO_1	VDDIO12_CIO_1	E5
F8	VDD_CIO_1	VDDIO12_CIO_1	E7
G4	VDD_FIXED	VDDIO12_PLL_SOC0	K8
G5	VDD_FIXED	VDDIO12_PLL_SOC1	H8
H5	VDD_FIXED	VDDIO12_XTAL	H9
H6	VDD_FIXED	VDDIO12	E9
G7	VDD_FIXED_PLL	VDDIO12	H3
G9	VDD_FIXED_XTAL	VDDIO12	K9
		VDDIO12_EFUSE1	F3
		VDDIO12_AMUX	F7

VSS: A1, A2, A4, A6, A8, A10, A11, B2, B4, B6, B8, B10, C3, C5, C6, C7, C9, D1, D5, D7, D11, E3, E4, E6, E8, F2, F5, F10, G3, G6, G8; H4, H7, J2, J3, J5, J7, J10, K4, K6, L1, L5, L7, L11, M3, M5, M6, M7, M9, N2, N4, N6, N8, N10, P1, P2, P4, P6, P8, P10, P11

PP1V2_USBC_VDDIO — 132S0395 CF134 0.1UF 10% 6.3V X6S 0201 — 138S00039 CF135 2.2UF 20% 6.3V X6S-CERM 0201
CF136 14UF 20% 4V X5R 0402-D2X-1 — CF137 14UF 20% 4V X5R 0402-D2X-1

PP1V2_USBC_VDDIO — 138S00039 CF152 2.2UF 20% 6.3V X6S-CERM 0201 — PLACE_NEAR=UF100.K8:5MM
PP1V2_ATCRTMR1_VDDIO_XTAL_F — VOLTAGE=1.2V — 155S0644 FLF100 240-OHM-0.2A-0.9-OHM 0201 — PP1V2_USBC_VDDIO
CF162 0.1UF 10% 6.3V X6S 0201 — 132S0395
CF163 2.2UF 20% 6.3V X6S-CERM 0201 — 138S00039
ATCRTMR1_VDDIO_EFUSE

PP1V2_USBC_VDDIO — 132S0395 CF164 0.1UF 10% 6.3V X6S 0201

Connect to GND directly or via a resistor

CF111 10PF 5% 25V C0G 0201 — RF111 200 1% 1/20W TK 0201-1 — ATCRTMR1_CFP_RCAL_NEG / ATCRTMR1_CFP_RCAL_POS
CF110 10PF 5% 25V C0G 0201 — RF110 200 1% 1/20W TK 0201-1 — ATCRTMR1_SFP_RCAL_NEG / ATCRTMR1_SFP_RCAL_POS

UF100 TMNB25B0-C1 FCCSP 998-25504 SYM 1 OF 2
OMIT_TABLE CRITICAL

USBC_ATC1_D2R_C_P<1>	P9	SFP_PHY_RXTX_0_P	SFP PHY	CFP_PHY_RXTX_0_P	USBC1_R2D_CR_P<1>
USBC_ATC1_D2R_C_N<1>	N9	SFP_PHY_RXTX_0_N		CFP_PHY_RXTX_0_N	USBC1_R2D_CR_N<1>
USBC_ATC1_D2R_C_P<2>	P5	SFP_PHY_RXTX_2_P		CFP_PHY_RXTX_2_P	USBC1_R2D_CR_P<2>
USBC_ATC1_D2R_C_N<2>	N5	SFP_PHY_RXTX_2_N		CFP_PHY_RXTX_2_N	USBC1_R2D_CR_N<2>
USBC_ATC1_R2D_P<1>	P7	SFP_PHY_RXTX_1_P		CFP_PHY_RXTX_1_P	USBC1_D2R_P<1>
USBC_ATC1_R2D_N<1>	N7	SFP_PHY_RXTX_1_N		CFP_PHY_RXTX_1_N	USBC1_D2R_N<1>
USBC_ATC1_R2D_P<2>	P3	SFP_PHY_RXTX_3_P		CFP_PHY_RXTX_3_P	USBC1_D2R_P<2>
USBC_ATC1_R2D_N<2>	N3	SFP_PHY_RXTX_3_N		CFP_PHY_RXTX_3_N	USBC1_D2R_N<2>
USBC_ATC1_AUX_C_P	L4	SFP_LPDP_AUX_P		CFP_LPDP_AUX_P	USBC1_AUX_P
USBC_ATC1_AUX_C_N	M4	SFP_LPDP_AUX_N		CFP_LPDP_AUX_N	USBC1_AUX_N
CIO_ATC1_LSTX	G1	USB4_SFP_SB_RX		USB4_CFP_SB_RX	USBC1_CIO_LSRX
CIO_ATC1_LSRX	G2	USB4_SFP_SB_TX		USB4_CFP_SB_TX	USBC1_CIO_LSTX
				USB4_CFP_SB_TX_DIR	ATCRTMR1_LSTX_DIR
ATCRTMR1_SFP_RCAL_POS	M8	SFP_PHY_RCAL_P		CFP_PHY_RCAL_P	ATCRTMR1_CFP_RCAL_POS
ATCRTMR1_SFP_RCAL_NEG	L8	SFP_PHY_RCAL_N		CFP_PHY_RCAL_N	ATCRTMR1_CFP_RCAL_NEG
ATCRTMR1_CHIPID_0	M1	CHIP_ID_0	GPIO PERIPHERAL	QSPI_CS*	SPI_ATCRTMR1_CS_L
ATCRTMR1_CHIPID_1	N1	CHIP_ID_1		QSPI_SCLK	SPI_ATCRTMR1_CLK
ATCRTMR1_BOOT_CONFIG0	H2	BOOT_CONFIG0		QSPI_DQ0	SPI_ATCRTMR1_DIO<0>
ATCRTMR1_BOOT_CONFIG1	J1	BOOT_CONFIG1		QSPI_DQ1	SPI_ATCRTMR1_DIO<1>
ATCRTMR1_BOOT_CONFIG2	K1	BOOT_CONFIG2		QSPI_DQ2	SPI_ATCRTMR1_DIO<2>
ATCRTMR1_FORCE_DFU	C1	FORCE_DFU		QSPI_DQ3	SPI_ATCRTMR1_DIO<3>
TP_ATCRTMR1_GPIO_0	K2	GPIO0		I2C0_SCL	I2C_ATCRTMR_SCL
NC_ATCRTMR1_GPIO_1 (NO_TEST=1)	L3	GPIO1		I2C0_SDA	I2C_ATCRTMR_SDA
TP_ATCRTMR1_GPIO_2	K3	GPIO2		I2C1_SCL	I2C_UPC1_ATCRTMR1_SCL_1V2
TP_ATCRTMR1_GPIO_3	L10	GPIO3		I2C1_SDA	I2C_UPC1_ATCRTMR1_SDA_1V2
				I2C1_INT	INT_I2C_UPC1_ATCRTMR1_L
ATCRTMR1_COLD_RESET_L	L2	COLD_RESET*	CLOCKS AND RESET	TESTMODE	ATCRTMR1_TESTMODE
ATCRTMR1_CFSB	M2	CFSB	TEST AND DEBUG	JTAG_SEL	ATCRTMR1_JTAGL_SEL
ATCRTMR1_XTAL24M_IN	F11	XI0		JTAG_TCK	SWD_NUB_ATCRTMR_SWCLK
ATCRTMR1_XTAL24M_OUT	E11	XO0		JTAG_TMS	SWD_NUB_ATCRTMR_SWDIO
				JTAG_TDI	TP_ATCRTMR1_JTAG_TDI
				JTAG_TDO	ATCRTMR1_JTAG_TDO
				JTAG_TRST*	TP_ATCRTMR1_JTAG_TRESET
				ANALOGMUX_OUT	TP_ATCRTMR1_ANALOGMUX_OUT
				TST_CLKOUT	TP_ATCRTMR1_TST_CLKOUT
				TST_CLK_LVDS_0_P	NC_ATCRTMR1_CLK_LVDS_P<0> (NO_TEST=1)
				TST_CLK_LVDS_0_N	NC_ATCRTMR1_CLK_LVDS_N<0> (NO_TEST=1)
				TST_CLK_LVDS_1_P	NC_ATCRTMR1_CLK_LVDS_P<1> (NO_TEST=1)
				TST_CLK_LVDS_1_N	NC_ATCRTMR1_CLK_LVDS_N<1> (NO_TEST=1)

SPI_ATCRTMR1_DIO<0> — RF197 33 1/20W 5% TK 0201 — SPI_ATCRTMR1_R_DIO<0>
SPI_ATCRTMR1_DIO<1> — RF198 33 1/20W 5% TK 0201 — SPI_ATCRTMR1_R_DIO<1>

PP1V2_USBC_VDDIO — RF190 3.3K 5% 1/20W TK 0201 — NOSTUFF RF191 3.3K 5% 1/20W TK 0201 — NOSTUFF RF192 3.3K 5% 1/20W TK 0201 — NOSTUFF RF193 3.3K 5% 1/20W TK 0201 — CF190 1.0UF 20% 6.3V X5R 0201-1

UF190 64MBIT-1.2V W25Q64NE XSON-1 (OMIT_TABLE CRITICAL 335S00574)

SPI_ATCRTMR1_CLK	RF194 33	6	CLK
SPI_ATCRTMR1_CS_L		1	CS*
SPI_ATCRTMR1_DIO<2>	RF195 33	3	WP*(IO2)
SPI_ATCRTMR1_DIO<3>	RF196 33	7	HOLD*(IO3)
		5	DI(IO0) — SPI_ATCRTMR1_R_DIO<0>
		2	DO(IO1) — SPI_ATCRTMR1_R_DIO<1>
		8	VCC
		4	GND
		9	EPAD

RF147 47K — ATCRTMR1_JTAGL_SEL
RF140 10K — ATCRTMR1_TESTMODE
RF143 47K — CIO_ATC1_LSTX
RF144 47K — CIO_ATC1_LSRX

BOM_COST_GROUP=TBT

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Apple Inc.

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*** OK2INTEGRATE ***

PP3V3_UPC0_LDO

RF260 3.3K 5% 1/20W TK 0201

RF261 3.3K 5% 1/20W TK 0201

RF263 3.3K 5% 1/20W TK 0201

RF262 3.3K 5% 1/20W TK 0201

CF260 1UF 10% 6.3V CERM 402

UF260 8MBIT-3.0V W25Q80DVUXIE USON

VCC CLK CS* WP*(IO2) HOLD*(IO3) DI(IO0) DO(IO1) GND EPAD

OMIT_TABLE CRITICAL 335S00133

ROM_UPC01_WP_L

ROM_UPC01_HOLD_L

NOSTUFF RF264 3.3K 5% 1/20W TK 0201

SPI_UPC01_MOSI

SPI_UPC01_MISO

SPI_UPC01_CLK

SPI_UPC01_CS_L

NO_XNET_CONNECTION=1

SPI Master Ace

RF289 15 SPI_UPC01_R_MOSI

RF288 15 SPI_UPC01_R_MISO

RF284 100 SPI_UPC01_CLK_DBG

RF285 15 SPI_UPC01_R_CLK

RF287 15 SPI_UPC01_R_CS_L

PACK_IGNORE=TRUE
PACK_OPTION=USBC_SPI_2ND_ROM

PP3V3_UPC1_LDO

RF250 3.3K 5% 1/20W TK 0201

NOSTUFF RF251 3.3K 5% 1/20W TK 0201

RF253 3.3K 5% 1/20W TK 0201

RF252 3.3K 5% 1/20W TK 0201

CF250 1UF 10% 6.3V CERM 402

UF250 8MBIT-3.0V W25Q80DVUXIE USON

VCC CLK CS* WP*(IO2) HOLD*(IO3) DI(IO0) DO(IO1) GND EPAD

OMIT_TABLE CRITICAL 335S00133

RF259 3.3K 5% 1/20W TK 0201

SPI Secondary Ace

RF254 15

RF255 15

RF257 15

RF258 15

GND

PP1V25_S2

PP3V3_S2_LDO

CF230 0.1UF 10% 6.3V CERM-X5R 0201

UF230 SN74AXC1T45-S SOT-5X3

VCCA VCCB DIR A B

PMU_ACTIVE_READY

ATCRTMR01_ACTIVE_READY_3V3

PACK_IGNORE=TRUE
PACK_OPTION=ACTIVE_READY:LARGE_PITCH

CF231 0.1UF 10% 6.3V CERM-X5R 0201

UF230 SN74AXC1T45 X2SON

311S00212

PACK_OPTION=ACTIVE_READY:SMALL_PITCH_CHECK_WITH_DFM

RF212 1.5K 5% 1/20W TK 0201

RF213 1.5K 5% 1/20W TK 0201

INT_I2C_EUSBLS0_L

INT_I2C_EUSBLS1_L

RF211 0 0% 1/20W TK 0201

RF216 0 0% 1/20W TK 0201

INT_I2C_UPC0_ATCRTMR0_L

INT_I2C_UPC1_ATCRTMR1_L

CF236 0.1UF 10% 6.3V CERM-X5R 0201

USBC_ATC1_AUX_P

USBC_ATC1_AUX_N

USBC_ATC1_AUX_C_P

USBC_ATC1_AUX_C_N

CF237 0.1UF 10% 6.3V CERM-X5R 0201

CF275 0.1UF 10% 6.3V CERM-X5R 0201

USBC_ATC0_AUX_P

USBC_ATC0_AUX_N

USBC_ATC0_AUX_C_P

USBC_ATC0_AUX_C_N

CF276 0.1UF 10% 6.3V CERM-X5R 0201

Ace 0 is SPI Ace?

Ace 1 is SPI Ace?

PACK_OPTION=USBC_SPI_UPC0

SPI_UPC01_R_CLK
SPI_UPC01_R_CS_L
SPI_UPC01_R_MOSI
SPI_UPC01_R_MISO

MAKE_BASE=TRUE

PACK_OPTION=USBC_SPI_UPC1

GND GND GND GND

SWD_UPC_SWCLK
SWD_UPC_SWDIO0
PP3V3_UPC0_LDO

SWD_UPC01_UART_CLK
SWD_UPC01_UART_DATA
PP3V3_UPC1_LDO

Ace 1 is UART Ace?

Ace 0 is UART Ace?

PACK_OPTION=USBC_SPI_UPC0_AND_NO_2ND_ROM

PACK_OPTION=USBC_SPI_UPC1

PACK_OPTION=USBC_SPI_UPC0

RF273 100K 1/20W 5% TK 0201 PD_UPC1_HPD

RF274 100K 1/20W 5% TK 0201 PD_UPC0_HPD

SPI Ace UART_UPC01_TX UART_UPC01_RX

UART Ace UART_UPC01_TX UART_UPC01_RX

ACE ARKANOID CONN

JF200 505070-1222 M-ST-SM

USBC_DBG

PACK_IGNORE=TRUE
PACK_OPTION=KEEP_SMALL_ARKANOID_CONN

SMC

ATCRTMR0_FORCE_DFU
I2C_SMC_UPC_SCL
I2C_SMC_UPC_SDA
UPC_SMC_I2C_INT_L
SPI_UPC01_CLK_DBG
UART_UPC01_TX

SOC

UPC_I2C_INT_L
I2C_UPC_SCL
I2C_UPC_SDA
UPC0_SER_DBG
UPC1_SER_DBG
UART_UPC01_RX

SPI Ace

BRIDGE ARKANOID CONN

JF201 505070-1222 M-ST-SM

ATCRTMR0_RESET_L
UPC0_ATCRTMR01_PWR_EN
PP1V2_USBC_VDDIO
PP0V855_USBC_CIO
ATCRTMR1_RESET_L
I2C_UPC1_ATCRTMR1_SDA

INT_I2C_UPC0_ATCRTMR0_L
I2C_UPC0_ATCRTMR0_SCL
I2C_UPC0_ATCRTMR0_SDA
UPC1_ATCRTMR01_PWR_EN
INT_I2C_UPC1_ATCRTMR1_L
I2C_UPC1_ATCRTMR1_SCL

USBC_DBG

RF280 200K 0201 5% 1/20W TK

VREFB_ARDV01

PP3V3_S2_LDO

PP1V25_S2

CF281 0.1UF 10% 6.3V CERM-X5R 0201

CF280 0.1UF 10% 6.3V CERM-X5R 0201

RF282 5.1K 5% 1/20W TK 0201

RF283 5.1K 5% 1/20W TK 0201

PACK_OPTION=PKGS:SMALL_PITCH

UF280 LSF0102 X2SON-COMBO 311S00234

VREF_A VREF_B EN A1 A2 B1 B2 GND

I2C_UPC_SCL
I2C_UPC_SDA

I2C_UPC01_3V3_SCL
I2C_UPC01_3V3_SDA

PACK_IGNORE=TRUE
PACK_OPTION=PKGS:LARGER_PITCH

UF280 LSF0102 VSSOP 311S00257

AARDVARKANOID CONN

JF202 505070-1222 M-ST-SM

USBC_DBG

PACK_IGNORE=TRUE
PACK_OPTION=KEEP_SMALL_ARKANOID_CONN

SPI ACE

PP1V25_S2
SWD_UPC_SWDIO0_CONN
SWD_UPC_SWCLK_CONN
SPI_UPC01_MISO
I2C_UPC01_3V3_SDA
I2C_UPC01_3V3_SCL

SPI_UPC01_CS_L
SPI_UPC01_CLK
SPI_UPC01_MOSI
SWD_UPC01_UART_CLK
SWD_UPC01_UART_DATA
PP1V25_S2

UART ACE

ATCRTMR01_ACTIVE_READY_3V3

NO_XNET_CONNECTION=1

RF290 100K 5% 1/20W TK 0201

USBC0_AUX_N
USBC0_AUX_P

CF290 0.1UF 10% 6.3V CERM-X5R 0201

CF291 0.1UF 10% 6.3V CERM-X5R 0201

USBC0_AUX_C_N
USBC0_AUX_C_P

RF292 33K 5% 1/20W TK 0201

RF293 33K 5% 1/20W TK 0201

RF291 100K 5% 1/20W TK 0201

RF298 100K 5% 1/20W TK 0201

USBC1_AUX_N
USBC1_AUX_P

CF292 0.1UF 10% 6.3V CERM-X5R 0201

CF293 0.1UF 10% 6.3V CERM-X5R 0201

USBC1_AUX_C_N
USBC1_AUX_C_P

RF296 33K 5% 1/20W TK 0201

RF297 33K 5% 1/20W TK 0201

RF299 100K 5% 1/20W TK 0201

HV POWER ALIASES

Fuses for laptop charging.

PACK_OPTION=USBC_LAPTOP

Desktops only need connection for programming OTP.

PACK_IGNORE=TRUE
PACK_OPTION=USBC_DESKTOP

CRITICAL 0603-1 FF200 6A-32V 740S00053

PPDCIN_AON_CHGR

PLACE_NEAR=UF400:5MM

MAKE_BASE=TRUE VOLTAGE=20V

PPHV_INT0_AONSW

RF200 0 0% 1/20W TK 0201

CRITICAL 0603-1 FF201 6A-32V 740S00053

PLACE_NEAR=UF500:5MM

PPHV_INT1_AONSW

RF201 0 0% 1/20W TK 0201

PPVBUS_USBC0
PPVBUS_USBC1

SYNC_MASTER=USBC	SYNC_DATE=09/26/2022
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BOM_COST_GROUP=USB-C

*** OK2INTEGRATE ***

Ace 0 is Debug Port?

PACK_OPTION=USBC_DEBUG_UPC0 — ATC0 / UPC0 / RTMR0 — PACK_OPTION=USBC_DEBUG_UPC1

UART_DEBUGPRT_R2D (IN)	UART_DEBUGPRT_R2D	UART_DEBUGPRT_R2D (IN)
UART_DEBUGPRT_D2R (OUT)	UART_DEBUGPRT_D2R	UART_DEBUGPRT_D2R (IN)
SWD_SOC_SWCLK (BI)	SWD_SOC_SWCLK	SWD_SOC_SWCLK (OUT)
SWD_SOC_SWDIO (BI)	SWD_SOC_SWDIO	SWD_SOC_SWDIO (OUT)
UART_SMC_DEBUGPRT_R2D (IN)	UART_SMC_DEBUGPRT_R2D	UART_SMC_DEBUGPRT_R2D (OUT)
UART_SMC_DEBUGPRT_D2R (OUT)	UART_SMC_DEBUGPRT_D2R	UART_SMC_DEBUGPRT_D2R (IN)
USB_DBG_LS_P (BI)	USB_DBG_LS_P	USB_DBG_LS_P (BI)
USB_DBG_LS_N (BI)	USB_DBG_LS_N	USB_DBG_LS_N (BI)

Ace 1 is Debug Port?

ATC1 / UPC1 / RTMR1

PD_UPC1_DBG0_R (OUT)
PD_UPC1_DBG1_R (IN)
PD_UPC1_DBG2_R (IN)
PD_UPC1_DBG3_R (IN)
PD_UPC1_DBG4_R (OUT)
PD_UPC1_DBG5_R (IN)
PD_UPC1_USBP2_RP (BI)
PD_UPC1_USBP2_RN (BI)

Main Debug Port

Ace2 GPIOs

SOC_DOCK_CONNECT (OUT)	SOC_DOCK_CONNECT	SOC_DOCK_CONNECT (IN)
SOC_DFU_STATUS (IN)	SOC_DFU_STATUS	SOC_DFU_STATUS (OUT)
SOC_FORCE_DFU (OUT)	SOC_FORCE_DFU	SOC_FORCE_DFU (IN)

PACK_OPTION=USBC_DEBUG_UPC0

PD_UPC1_GPIO7 (OUT)
PD_UPC1_GPIO9 (OUT)
PD_UPC1_GPIO10 (OUT)

Ace 1 is non-debug Port?

ATC1 / UPC1 / RTMR1

RF320	PD_UPC1_DBG0_R	PD_UPC1_DBG0_R
RF321	PD_UPC1_DBG1_R	PD_UPC1_DBG1_R
RF322	PD_UPC1_DBG2_R	PD_UPC1_DBG2_R
RF323	PD_UPC1_DBG3_R	PD_UPC1_DBG3_R
RF324	PD_UPC1_DBG4_R	PD_UPC1_DBG4_R
RF325	PD_UPC1_DBG5_R	PD_UPC1_DBG5_R
RF328	PD_UPC1_USBP2_RP	PD_UPC1_USBP2_RP
RF329	PD_UPC1_USBP2_RN	PD_UPC1_USBP2_RN

100K 1/20W 5% TK 0201 MAKE_BASE=TRUE

Ace2 GPIOs

RF373	PD_UPC1_GPIO7	PD_UPC1_GPIO7 (OUT)
RF374	PD_UPC1_GPIO9	PD_UPC1_GPIO9 (OUT)
RF375	PD_UPC1_GPIO10	PD_UPC1_GPIO10 (OUT)

CKPLUS_WAIVE=SINGLE_NODENET on all nets above.

Ace 0 is non-debug Port?

PACK_IGNORE=TRUE
PACK_OPTION=USBC_DEBUG_UPC1

ATC0 / UPC0 / RTMR0

RF310	PD_UPC0_DBG0_R	UART_DEBUGPRT_R2D
RF311	PD_UPC0_DBG1_R	UART_DEBUGPRT_D2R
RF312	PD_UPC0_DBG2_R	SWD_SOC_SWCLK
RF313	PD_UPC0_DBG3_R	SWD_SOC_SWDIO
RF314	PD_UPC0_DBG4_R	UART_SMC_DEBUGPRT_R2D
RF315	PD_UPC0_DBG5_R	UART_SMC_DEBUGPRT_D2R
RF318	PD_UPC0_USBP2_RP	USB_DBG_LS_P
RF319	PD_UPC0_USBP2_RN	USB_DBG_LS_N

100K 1/20W 5% TK 0201 MAKE_BASE=TRUE

Ace2 GPIOs

RF363	PD_UPC0_GPIO7	SOC_DOCK_CONNECT
RF364	PD_UPC0_GPIO9	SOC_DFU_STATUS
RF365	PD_UPC0_GPIO10	SOC_FORCE_DFU (10K)

CKPLUS_WAIVE=SINGLE_NODENET on all nets above.

Non-debug Port

GND (BI) — MAKE_BASE=TRUE

PACK_OPTION=USBC_SPI_NO_2ND_ROM

Unused ports

RF397	PD_UPC0_GPIO1	PD_UPC0_GPIO1
RF398	PD_UPC0_GPIO6	PD_UPC0_GPIO6
RF31A	PD_UPC0_USBP3_RP	PD_UPC0_USBP3_RP
RF31B	PD_UPC0_USBP3_RN	PD_UPC0_USBP3_RN

100K 1/20W 5% TK 0201 MAKE_BASE=TRUE

Secondary ACE ROM Options

RF396	PD_UPC1_GPIO1	PD_UPC1_GPIO1
RF399	PD_UPC1_GPIO6	PD_UPC1_GPIO6
RF32A	PD_UPC1_USBP3_RP	PD_UPC1_USBP3_RP
RF32B	PD_UPC1_USBP3_RN	PD_UPC1_USBP3_RN

100K 1/20W 5% TK 0201 MAKE_BASE=TRUE

Connections for Laptops (USBC power in)

PACK_OPTION=USBC_LAPTOP

PP3V3_UPC0_LDO (OUT)	PP3V3_UPC0_LDO (IN)
USBC0_CC1 (BI)	USBC0_CC1 (BI)
USBC0_CC2 (BI)	USBC0_CC2 (BI)

Connections for Desktops (No USBC power in)

PACK_OPTION=USBC_DESKTOP — MAKE_BASE=TRUE

Connections for Laptops (USBC power in)

PACK_OPTION=USBC_LAPTOP

PP3V3_UPC1_LDO (OUT)	PP3V3_UPC1_LDO (IN)
USBC1_CC1 (BI)	USBC1_CC1 (BI)
USBC1_CC2 (BI)	USBC1_CC2 (BI)

Connections for Desktops (No USBC power in)

PACK_OPTION=USBC_DESKTOP — MAKE_BASE=TRUE

USBC0 PP_CABLE Protection

PP3V3_UPC0_LDO — CF300 1UF 10% 6.3V CERM 402
USBC0_VBIAS_PRT — CF301 0.1UF 10% 50V CERM-X7R 0402
MIN_LINE_WIDTH=0.0990 MIN_NECK_WIDTH=0.0990

UF300 TPD4S311A BGA

NC_USBC0_CC_FLT_L (NO_TEST=1)	FLT* (B4)
USBC0_CC1	D3 / CC1
USBC0_CC2	D4 / CC2
	SBU1 (D1)
	SBU2 (D2)
	C_SBU1 (B1)
	C_SBU2 (A1)
	C_CC1 (A2)
	C_CC2 (A3)
	RPD_G1 (B2)
	RPD_G2 (B3)
	GND (C1, C2, C3)

338S00753

USBC0_CC1_CONN, USBC0_CC2_CONN (BI) — MAKE_BASE=TRUE — PACK_OPTION=USBC_DESKTOP

PACK_OPTION=USBC_LAPTOP_CC_PRT
pack option for all component

USBC1 PP_CABLE Protection

PP3V3_UPC1_LDO — CF350 1UF 10% 6.3V CERM 402
USBC1_VBIAS_PRT — CF351 0.1UF 10% 50V CERM-X7R 0402
MIN_LINE_WIDTH=0.0990 MIN_NECK_WIDTH=0.0990

UF350 TPD4S311A BGA

NC_USBC1_CC_FLT_L (NO_TEST=1)	FLT* (B4)
USBC1_CC1	D3 / CC1
USBC1_CC2	D4 / CC2
	SBU1 (D1)
	SBU2 (D2)
	C_SBU1 (B1)
	C_SBU2 (A1)
	C_CC1 (A2)
	C_CC2 (A3)
	RPD_G1 (B2)
	RPD_G2 (B3)
	GND (C1, C2, C3)

338S00753

USBC1_CC1_CONN, USBC1_CC2_CONN (BI) — MAKE_BASE=TRUE — PACK_OPTION=USBC_DESKTOP

PACK_OPTION=USBC_LAPTOP_CC_PRT
pack option for all component

ATC0: I2C_ADDR=GND, I2CM_*_CNFG=1M\u03a9 3V3_LDO_X pull-ups
ATC1: I2C_ADDR=Float, I2CM_*_CNFG=1M\u03a9 3V3_LDO_X pull-ups
ATC2: I2C_ADDR=GND, I2CM_*_CNFG=1M\u03a9 pull-downs
ATC3: I2C_ADDR=Float, I2CM_*_CNFG=1M\u03a9 pull-downs

GND — NC_UPC1_I2C_ADDR — NC_UPC1_I2C_ADDR (NO_TEST=1) — MAKE_BASE=TRUE

Configure to enable VDDIO and use it for SWD.

GND — GND — MAKE_BASE=TRUE

Is UPCx_5V_EN being used?

UPC0_5V_EN	RF350	100K
UPC1_5V_EN	RF351	100K

5% 1/20W TK 0201

PACK_OPTION=USBC01_VR5V_LOCAL_NO
BOM_COST_GROUP=USB-C

ATCRTMR Boot Config

[2:0] = [011] 30Mhz QSPI and Test Mode Enabled
POR config should be [010] Test Mode Disabed

RF380	ATCRTMR0_BOOT_CONFIG2	(OUT)
RF381	ATCRTMR0_BOOT_CONFIG1	(OUT)
RF382	ATCRTMR0_BOOT_CONFIG0	(OUT)
RF383	ATCRTMR1_BOOT_CONFIG2	(OUT)
RF384	ATCRTMR1_BOOT_CONFIG1	(OUT)
RF385	ATCRTMR1_BOOT_CONFIG0	(OUT)

10K 5% 1/20W TK 0201 — NOSTUFF — LFKA_TEST_MODE:NO

LFKA_TEST_MODE:YES

RF386	RF387	RF388
RF389	RF390	RF391

PP1V2_USBC_VDDIO — 10K 5% 1/20W TK 0201 — NOSTUFF

ATCRTMR0_BOOT_CONFIG2 (OUT)
ATCRTMR0_BOOT_CONFIG1 (OUT)
ATCRTMR0_BOOT_CONFIG0 (OUT)
ATCRTMR1_BOOT_CONFIG2 (OUT)
ATCRTMR1_BOOT_CONFIG1 (OUT)
ATCRTMR1_BOOT_CONFIG0 (OUT)

ATCRTMR0 CHIP 0X00

RF392	ATCRTMR0_CHIPID_0	(OUT)
RF393	ATCRTMR0_CHIPID_1	(OUT)

10K 5% 1/20W TK 0201

ATCRTMR1 CHIP 0X01

PP1V2_USBC_VDDIO
RF395 47K 5% 1/20W TK 0201
ATCRTMR1_CHIPID_0 (OUT)

RF394 10K 5% 1/20W TK 0201 — ATCRTMR1_CHIPID_1 (OUT)

ATCRTMR0_RESET_1V2_L (IN)	RF330	ATCRTMR0_COLD_RESET_L (OUT)
	RF331	ATCRTMR0_CFSB (OUT)
P1V2_ATC01_PGOOD (IN)	RF332	NOSTUFF
ATCRTMR1_RESET_1V2_L (IN)	RF333	ATCRTMR1_COLD_RESET_L (OUT)
	RF334	ATCRTMR1_CFSB (OUT)
P1V2_ATC01_PGOOD (IN)	RF335	NOSTUFF

0 0% 1/20W TK 0201

SYNC_MASTER=USBC — SYNC_DATE=09/26/2022

PAGE TITLE: USB-C: Support 2 ATC01

Apple Inc.

DRAWING NUMBER	051-07020
SIZE	D
REVISION	6.0.0
BRANCH	evt-1
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*** OK2INTEGRATE ***

PP3V3_UPC0_LDO 61 62 63

Internal Pull-ups
Enabled after reading straps

470K RF409 5% 1/20W TK 0201 I2C_UPC0_ACTCRTMR0_SCL CKPLUS_WAIVE=I2C_PULLUP 61 63 66 68

470K RF408 5% 1/20W TK 0201 I2C_UPC0_ACTCRTMR0_SDA CKPLUS_WAIVE=I2C_PULLUP 61 63 66 68

1M RF405 5% 1/20W TK 0201 UART_UPC01_RX 61 63

100K RF406 5% 1/20W TK 0201 PD_UPC0_MRESET 63

Either a Testpoint or Arkanoid connector
must be present for GPIO0
(EVEN IN PRODUCTION)

CRITICAL
RF403 15K 0.1% 1/20W TK 0201

GND I2C_ADDR
PRIMARY ONLY

REAR PORT:
CONNECT UPC SPI TO ROM
FRONT PORT:
GROUND UPC SPI

PPHV_INT0_AONSW 61

MAX 100uF TOTAL ON RAIL

PP5V_S2 94 64

PP5V_S2 94 64

138S00070 CF406 4.7UF 20% 25V X5R 0402

PACK_IGNORE=TRUE
PACK_OPTION=ACE2_5V_INPUT_CAP

K9 L10 M9 N10 K11 L12 M11 N12 N14 M13 — PP_5V0 / PP_CABLE

G2 G4 H1 H3 J2 J4 K1 K3 L2 L4 M1 M3 N2 N4 — PP_HV

G6 G8 H5 H7 J6 J8 K5 K7 L6 L8 M5 M7 N6 N8 — VBUS

353S02993
CRITICAL
OMIT_TABLE

UF400
CD3217B13HACE
FCBGA

	B13	HRESET	
63 PD_UPC0_MRESET	A14	MRESET	
68 66 61 OUT ATCRTMR0_RESET_L	B17	RESET*	3V3
68 61 OUT UPC0_SER_DBG	A2	GPIO0	OUT,PP
	B1		
62 OUT PD_UPC0_GPIO1	D1	GPIO1	BI,N_OD
68 61 59 IN INT_I2C_UPC0_ATCRTMR0_L	F1	GPIO2	1V2 IN
62 OUT UPC0_5V_EN	C2	GPIO3	3V3 OUT,P_OD
68 61 59 OUT ATCRTMR0_FORCE_DFU	E2	GPIO4	1V2 OUT,PP
68 OUT UPC0_CHGR_AUX_DET_SHORT	B3	GPIO5	3V3 OUT,P_OD
62 IN PD_UPC0_GPIO6	C4	GPIO6	IN DIGITAL CORE I/O & CONTROL
62 OUT SOC_DOCK_CONNECT	D3	GPIO7	OUT,P_OD
64 43 OUT UPC_PMU_RESET_3V3	E4	GPIO8	3V3 OUT,P_OD
62 IN SOC_DFU_STATUS	F3	GPIO9	IN
62 OUT SOC_FORCE_DFU	F7	GPIO10	OUT,P_OD
62 PP3V3_UPC0_LDO	A18	BUSPOWER	
62 GND	M19	I2C_ADDR	IPU-BOOT
UPC0_R_OSC	M21	R_OSC	
68 66 63 61 BI I2C_UPC0_ACTCRTMR0_SDA	A16	I2CM_SDA_CNFG	IPU-AFTER-BOOT
68 66 63 61 BI I2C_UPC0_ACTCRTMR0_SCL	B15	I2CM_SCL_CNFG	IPU-AFTER-BOOT
61 49 BI I2C_UPC_SDA	B5	I2C_SDA1	
61 49 BI I2C_UPC_SCL	A4	I2C_SCL1	
61 49 OUT UPC_I2C_INT_L	D7	I2C_IRQ1*	
61 51 BI I2C_SMC_UPC_SDA	B7	I2C_SDA2	
61 51 BI I2C_SMC_UPC_SCL	A6	I2C_SCL2	
61 51 OUT UPC_SMC_I2C_INT_L	C8	I2C_IRQ2*	
61 OUT SPI_UPC01_R_CLK	B9	SPI_CLK	
61 OUT SPI_UPC01_R_MOSI	B11	SPI_MOSI	
61 IN SPI_UPC01_R_MISO	A10	SPI_MISO	
61 OUT SPI_UPC01_R_CS_L	A8	SPI_SSZ	
61 BI SWD_UPC_SWDIO0	E20	SWD_DATA	IPU
61 IN SWD_UPC_SWCLK	E16	SWD_CLK	IPU
63 61 IN UART_UPC01_RX	B19	UART_RX	
61 OUT UART_UPC01_TX	A20	UART_TX	
68 BI USB2_UPC0_P1_P	H19	USB_RP1_P	
68 BI USB2_UPC0_P1_N	H21	USB_RP1_N	
62 BI USB_DBG_LS_P	G20	USB_RP2_P	
62 BI USB_DBG_LS_N	G22	USB_RP2_N	
62 BI PD_UPC0_USBP3_RP	F19	USB_RP3_P	
62 BI PD_UPC0_USBP3_RN	F21	USB_RP3_N	
61 BI USBC0_AUX_C_P	J12	AUX_P	
61 BI USBC0_AUX_C_N	H11	AUX_N	
61 OUT PD_UPC0_HPD	C12	HPD	
62 IN UART_DEBUGPRT_R2D	G12	DEBUG0	
62 OUT UART_DEBUGPRT_D2R	F11	DEBUG1	
62 OUT SWD_SOC_SWCLK	E8	DEBUG2	
62 BI SWD_SOC_SWDIO	E12	DEBUG3	
62 IN UART_SMC_DEBUGPRT_R2D	G16	DEBUG4	
62 OUT UART_SMC_DEBUGPRT_D2R	F15	DEBUG5	
66 BI USBC0_CIO_LSTX_3V3	D15	DEBUG6	
66 OUT USBC0_CIO_LSRX_3V3	D19	DEBUG7	

PORT_MUX

POWER

TYPE-C

GND

PPVBUS_USBC0 68 61

CF401 1UF 20% 35V X5R 0402

CRITICAL
DF400 X3-WLB1608-1 SDM2U40CSP

PP3V3_S2_LDO 61 64 93

CF400 10UF 20% 6.3V CERM 0402

PP1V25_S2 61 64 93

CF402 1.0UF 20% 6.3V X5R 0201-1

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=3.3V

PP3V3_UPC0_LDO 61 62 63

138S0801 CF408 10UF 20% 6.3V CERM 0402

PP1V8_S2 92

132S0444 CF403 0.1UF 10% 6.3V CERM-XSR 0201

VIN_3V3	C20		
VDDIO	A12		
VDDIO_CFG	D11	GND	62
LDO_3V3	C22		
	D21		
VIN_LV	L20		
VOUT_LV	L18	UPC0_ATCRTMR01_PWR_EN	61 66 68
VRET	C16		
SS	L22	UPC0_SS	
LDO_CORE	E22	PP1V5_UPC0_LDO_CORE	
VBUS_OPT	D5	PPVBUS_USBC0	61
PP_HV_OPT	F5	PPHV_INT0_AONSW	61
C_CC1	M15	USBC0_CC1	BI 62
	N16		
C_CC2	M17	USBC0_CC2	BI 62
	N18		
RPD_G1	L14	USBC0_CC1	BI 62
RPD_G2	L16	USBC0_CC2	BI 62
C_USB_TP	K19	USBC0_USB_TOP_P	BI 58
C_USB_TN	K21	USBC0_USB_TOP_N	BI 58
C_USB_BP	J20	USBC0_USB_BOT_P	BI 58
C_USB_BN	J22	USBC0_USB_BOT_N	BI 58
C_SBU1	J16	USBC0_SBU1	BI 58
C_SBU2	H15	USBC0_SBU2	BI 58

(cap needed when used as power source)

PACK_OPTION=ACE2_SS_CAP

VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750

138S0801 CF405 10UF 20% 6.3V CERM 0402

CF409 0.68UF 5% 6.3V X6S 0402

PACK_OPTION=ACE2_SS_GND
GND
MAKE_BASE=TRUE

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500

131S00464 CF414 220PF 20% 50V C0G 0201-1

131S00464 CF413 220PF 20% 50V C0G 0201-1

GND_OPT	C18	
GND_OPT	E18	
GND_OPT	D17	
GND_OPT	G18	

GND

GND

A22 H9 N20 B21 K15 N22

BOM_COST_GROUP=USB-C

SYNC_MASTER=GBC SYNC_DATE=09/26/2022

PAGE TITLE
USB-C: Port Controller ATC0

Apple Inc.

DRAWING NUMBER 051-07020
SIZE D
REVISION 6.0.0
BRANCH evt-1
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*** OK2INTEGRATE ***

PP3V3_UPC1_LDO 61 62 64

1 470K 2 RF509 5% 1/20W TK 0201 I2C_UPC1_ATCRTMR1_SCL 61 64 66 68 CKPLUS_WAIVE=I2C_PULLUP

1 470K 2 RF508 5% 1/20W TK 0201 I2C_UPC1_ATCRTMR1_SDA 61 64 66 68 CKPLUS_WAIVE=I2C_PULLUP

1 1M 2 RF505 5% 1/20W TK 0201 UART_UPC01_TX 61 64

1 100K 2 RF506 5% 1/20W TK 0201 PD_UPC1_MRESET 64

Either a Testpoint or Arkanoid connector must be present for GPIO0 (EVEN IN PRODUCTION)

CRITICAL RF503 15K 0.1% 1/20W TK 0201 — GND_I2C_ADDR PRIMARY ONLY

REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI

61 PPHV_INT1_AONSW

MAX 100uF TOTAL ON RAIL

94 63 PP5V_S2

94 63 PP5V_S2

138S00070 CF506 4.7UF 20% 25V X5R 0402

PACK_IGNORE=TRUE
PACK_OPTION=ACE2_5V_INPUT_CAP

PP_5V0 (K9 L10 M9 N10 K11 L12 M11 N12 N14 M13)

PP_CABLE (G2 G4 H1 H3 J2 J4 K1 K3 L2 L4 M1 M3 N2 N4)

PP_HV (G6 G8 H5 H7 J6 J8 K5 K7 L6 L8 M5 M7 N6 N8)

VBUS

353S02993 CRITICAL OMIT_TABLE

UF500 CD3217B13HACE FCBGA

	B13	HRESET	
64 PD_UPC1_MRESET	A14	MRESET	
66 61 OUT ATCRTMR1_RESET_L	B17	RESET*	3V3
68 61 OUT UPC1_SER_DBG	A2	GPIO0	OUT,PP
	B1		
62 OUT PD_UPC1_GPIO1	D1	GPIO1	BI,N_OD
68 61 66 IN INT_I2C_UPC1_ATCRTMR1_L	F1	GPIO2	1V2 IN
62 OUT UPC1_5V_EN	C2	GPIO3	3V3 OUT,P_OD
60 OUT ATCRTMR1_FORCE_DFU	E2	GPIO4	1V2 OUT,PP
68 OUT UPC1_CHGR_AUX_DET_SHORT	B3	GPIO5	3v3 OUT,P_OD
62 IN PD_UPC1_GPIO6	C4	GPIO6	IN DIGITAL CORE I/O & CONTROL
62 OUT PD_UPC1_GPIO7	D3	GPIO7	OUT,P_OD
63 43 OUT UPC_PMU_RESET_3V3	E4	GPIO8	3v3 OUT,P_OD
62 IN PD_UPC1_GPIO9	F3	GPIO9	IN
62 OUT PD_UPC1_GPIO10	F7	GPIO10	OUT,P_OD
62 PP3V3_UPC1_LDO	A18	BUSPOWER	
62 NC_UPC1_I2C_ADDR	M19	I2C_ADDR	IPU-BOOT
UPC1_R_OSC	M21	R_OSC	
68 66 64 61 BI I2C_UPC1_ATCRTMR1_SDA	A16	I2CM_SDA_CNFG	IPU-AFTER-BOOT
68 66 64 61 BI I2C_UPC1_ATCRTMR1_SCL	B15	I2CM_SCL_CNFG	IPU-AFTER-BOOT
49 BI I2C_UPC_SDA	B5	I2C_SDA1	
49 BI I2C_UPC_SCL	A4	I2C_SCL1	
49 OUT UPC_I2C_INT_L	D7	I2C_IRQ1*	
51 BI I2C_SMC_UPC_SDA	B7	I2C_SDA2	
51 BI I2C_SMC_UPC_SCL	A6	I2C_SCL2	
51 OUT UPC_SMC_I2C_INT_L	C8	I2C_IRQ2*	
61 OUT GND	B9	SPI_CLK	
61 OUT GND	B11	SPI_MOSI	
64 IN GND	A10	SPI_MISO	
61 OUT GND	A8	SPI_SSZ	
61 BI SWD_UPC01_UART_DATA	E20	SWD_DATA	IPU
61 BI SWD_UPC01_UART_CLK	E16	SWD_CLK	IPU
64 61 IN UART_UPC01_TX	B19	UART_RX	
61 OUT UART_UPC01_RX	A20	UART_TX	
68 BI USB2_UPC1_P1_P	H19	USB_RP1_P	
68 BI USB2_UPC1_P1_N	H21	USB_RP1_N	
62 BI PD_UPC1_USBP2_RP	G20	USB_RP2_P	
62 BI PD_UPC1_USBP2_RN	G22	USB_RP2_N	
62 BI PD_UPC1_USBP3_RP	F19	USB_RP3_P	
62 BI PD_UPC1_USBP3_RN	F21	USB_RP3_N	
61 BI USBC1_AUX_C_P	J12	AUX_P	
61 BI USBC1_AUX_C_N	H11	AUX_N	
61 OUT PD_UPC1_HPD	C12	HPD	
62 BI PD_UPC1_DBG0_R	G12	DEBUG0	
62 BI PD_UPC1_DBG1_R	F11	DEBUG1	
62 OUT PD_UPC1_DBG2_R	E8	DEBUG2	
62 BI PD_UPC1_DBG3_R	E12	DEBUG3	
62 BI PD_UPC1_DBG4_R	G16	DEBUG4	
62 BI PD_UPC1_DBG5_R	F15	DEBUG5	
66 BI USBC1_CIO_LSTX_3V3	D15	DEBUG6	
66 OUT USBC1_CIO_LSRX_3V3	D19	DEBUG7	

PORT_MUX

POWER

TYPE-C

GND

PPVBUS_USBC1 58 61

CF501 1UF 20% 35V X5R 0402

CRITICAL DF500 X3-WLB1608-1 SDM2U40CSP

PP3V3_S2_LDO 61 63 93

138S0801 CF500 10UF 20% 6.3V CERM 0402

PP1V25_S2 61 63 93

CF502 1.0UF 20% 6.3V X5R 0201-1

MIN_LINE_WIDTH=0.2800
MIN_NECK_WIDTH=0.0750
VOLTAGE=3.3V

PP3V3_UPC1_LDO 61 62 64

138S0801 CF508 10UF 20% 6.3V CERM 0402

PP1V8_S2 92

132S0444 CF503 0.1UF 10% 6.3V CERM-X5R 0201

(cap needed when used as power source)

UPC1_ATCRTMR01_PWR_EN 61 66 68

VIN_3V3	C20	
VDDIO	A12	
VDDIO_CFG	D11	GND 62
LDO_3V3	C22 / D21	
VIN_LV	L20	
VOUT_LV	L18	
VRET	C16	
SS	L22	UPC1_SS
LDO_CORE	E22	PP1V5_UPC1_LDO_CORE
VBUS_OPT	D5	PPVBUS_USBC1 61
PP_HV_OPT	F5	PPHV_INT1_AONSW 61
C_CC1	M15 / N16	USBC1_CC1 BI 62
C_CC2	M17 / N18	USBC1_CC2 BI 62
RPD_G1	L14	USBC1_CC1 BI 62
RPD_G2	L16	USBC1_CC2 BI 62
C_USB_TP	K19	USBC1_USB_TOP_P BI 58
C_USB_TN	K21	USBC1_USB_TOP_N BI 58
C_USB_BP	J20	USBC1_USB_BOT_P BI 58
C_USB_BN	J22	USBC1_USB_BOT_N BI 58
C_SBU1	J16	USBC1_SBU1 BI 58
C_SBU2	H15	USBC1_SBU2 BI 58

VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2800
MIN_NECK_WIDTH=0.0750

138S0801 CF505 10UF 20% 6.3V CERM 0402

PACK_OPTION=ACE2_SS_CAP

CF509 0.68UF 5% 6.3V X6S 0402

PACK_OPTION=ACE2_SS_GND
GND
MAKE_BASE=TRUE

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500

131S00464 CF514 220PF 5% 50V C0G 0201-1

131S00464 CF513 220PF 5% 50V C0G 0201-1

GND_OPT	C18	
GND_OPT	E18	
GND_OPT	D17	
GND_OPT	G18	

GND

GND
A22 H9 N20 B21 K15 N22

BOM_COST_GROUP=USB-C

SYNC_MASTER=USBC SYNC_DATE=09/26/2022

PAGE TITLE: USB-C: Port Controller ATC1

Apple Inc.

DRAWING NUMBER 051-07020 SIZE D
REVISION 6.0.0
BRANCH evt-1
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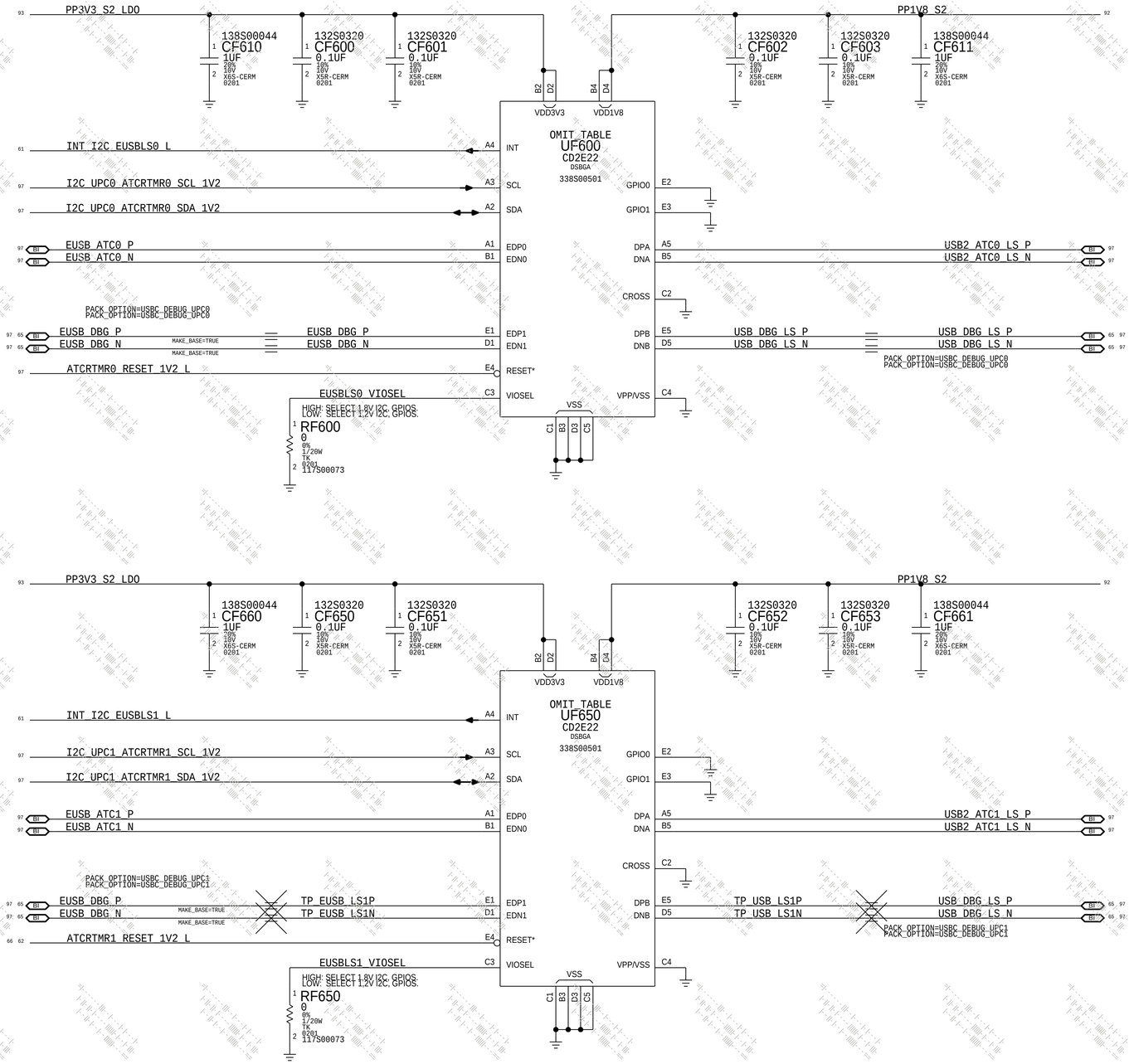
SHEET 64 OF 113

*** OK2INTEGRATE ***



BOM_COST_GROUP=USB-C

SYNC_MASTER=USBC SYNC_DATE=09/26/2021

PAGE TITLE

USB-C: USB2 RPT

Apple Inc.

DRAWING NUMBER 051-07020 SIZE D

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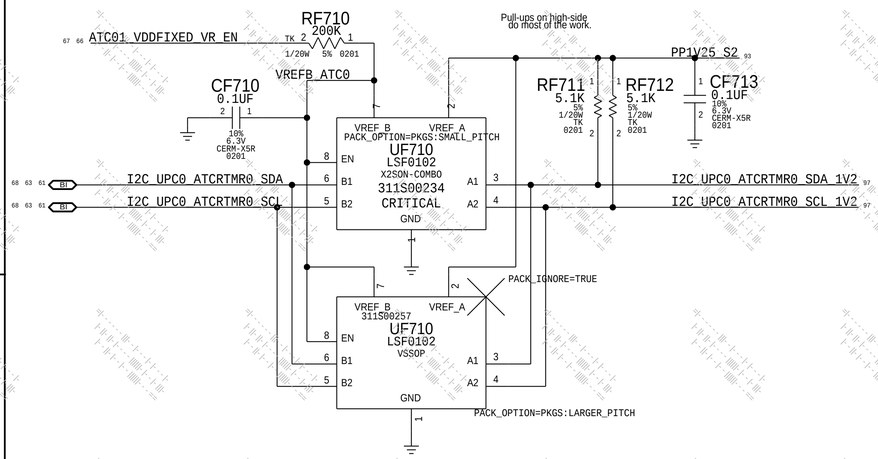
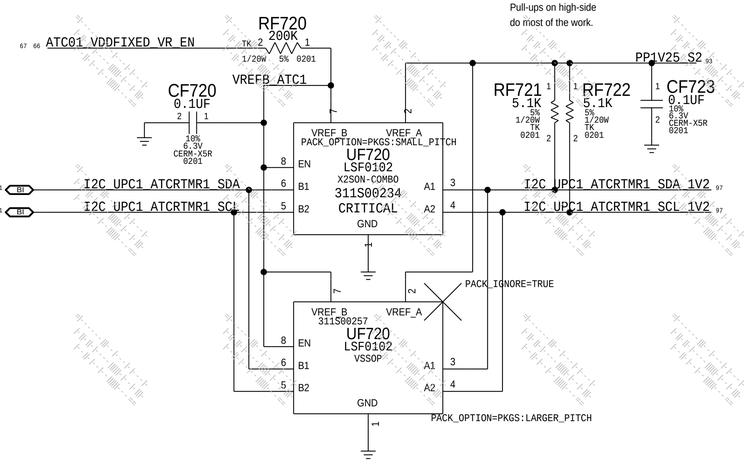
*** OK2INTEGRATE ***

Sequencing Requirements: 3.3V to UF790 --> system 1.2V (UF710,UF720) same time or before system 1.8V (UF400&UF500 VIN_LV pin)

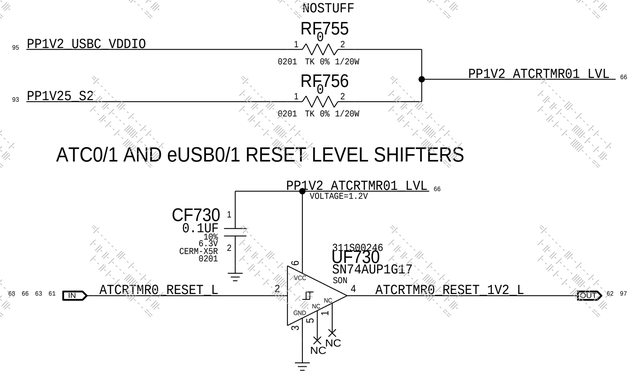
ATC0 RE-TIMER I2C LEVEL SHIFTERS



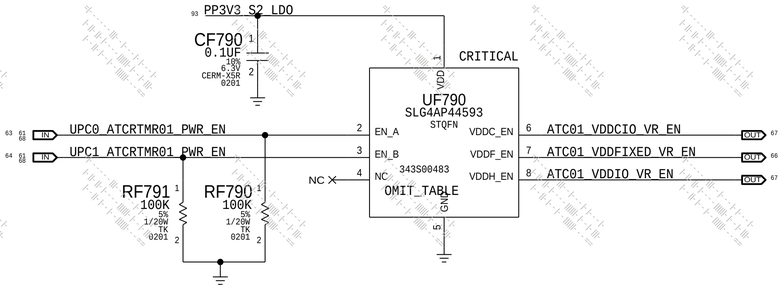
ATC1 RE-TIMER I2C LEVEL SHIFTERS

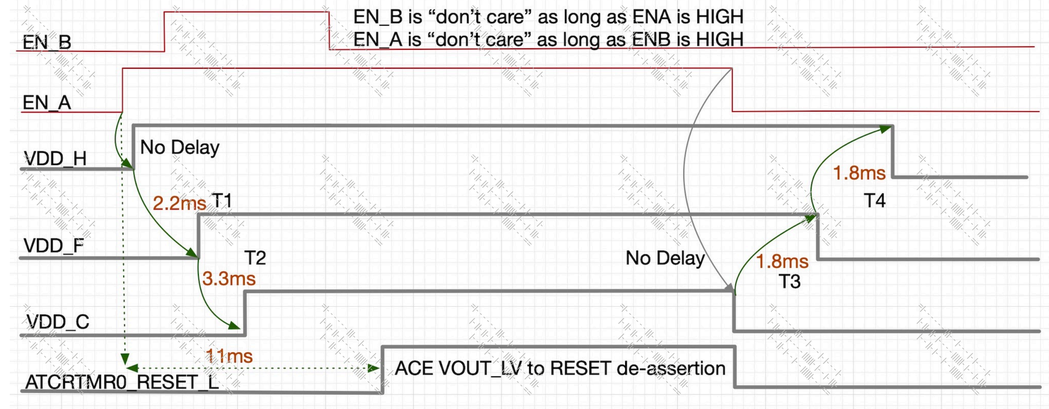


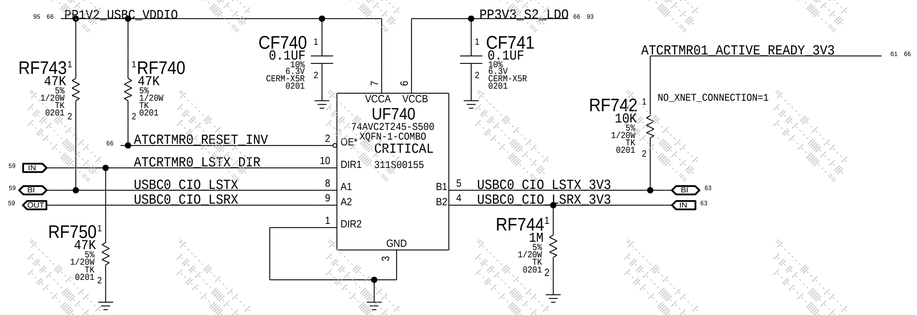
ATC0/1 AND eUSB0/1 RESET LEVEL SHIFTERS

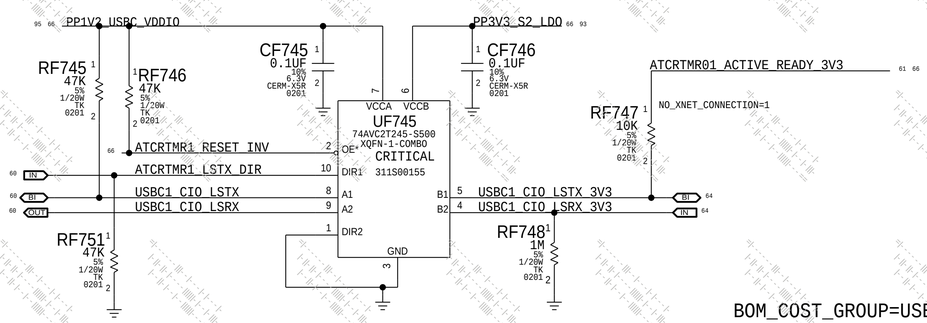


The 3.3V needs to be HIGH before VIN_LV of ACEs









BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: HS Level Shifters

Apple Inc.

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*** OK2INTEGRATE ***

Vout = 1.213V
Iout Max = 0.96A
F = 1.8 MHZ

Vout = 0.8621V
Iout Max = 0.5A
F = 1.8 MHZ

Vout = 0.8073V
Iout Max =0.7A
F = 1.8 MHZ

BOM_COST_GROUP=TBT

$PAGE_TITLE=USB-C: ATC01 REGULATORS

09/26/2021

Apple Inc.

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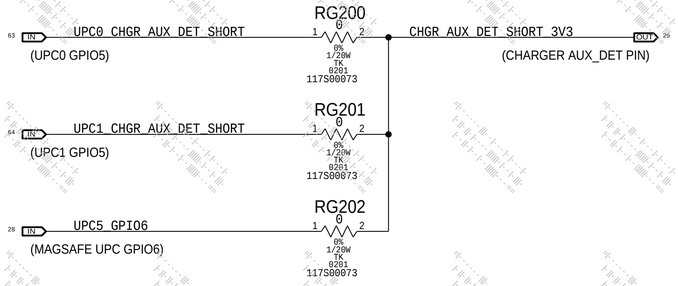
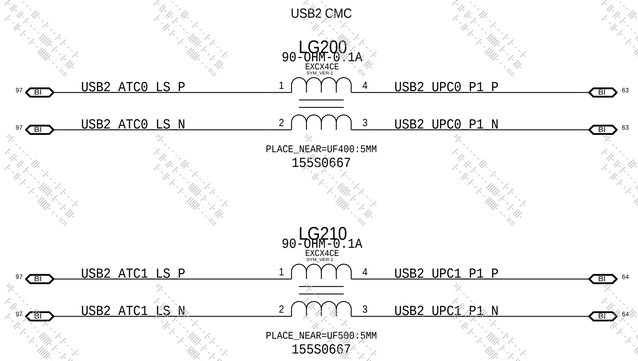
A Charger AUX_DET Connections

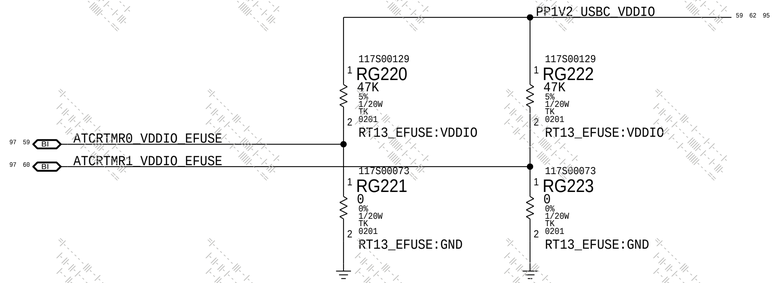
CHARGER AUX DET CONNECTIONS
<RDAR://70072178>
ALLOW ACE TO SEND A SIGNAL TO CHARGER
TO BLOCK SYSTEM CURRENT THROUGH ACE2 FETS DURING ACE2 SOFT START



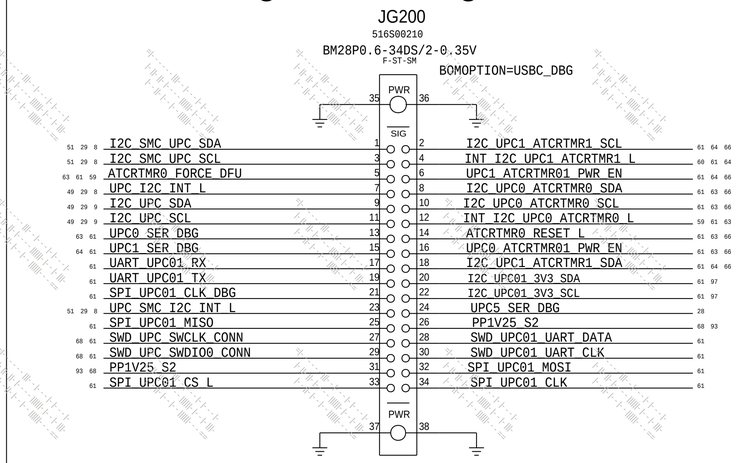
B USB 2.0 Common Mode Choke



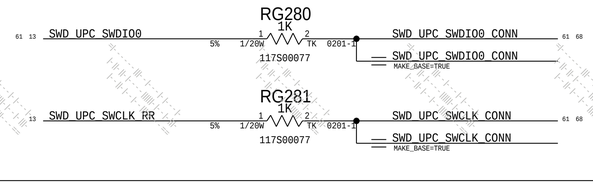
C RT13 VDDIO_EFUSE Selection



D USB-C/MagSafe Debug Connector



E USB-C SWDIO Aliases



BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: PROJECT SUPPORT

Apple Inc.

DRAWING NUMBER: 051-07020
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BRANCH: evt-1
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FOR SYSTEM INTEGRATION INFORMATION REFER TO
RDAR://PROBLEM/59047597

TYPHOON WIFI/BT MODULE

PLACE_NEAR=UL000.48:4MM
PLACE_NEAR=UL000.48:3MM
PLACE_NEAR=UL000.48:3MM PP3V8_AON_WLBT 69 92
CL005 10UF 20% 10V X5R-CERM 0402-8
CRITICAL CL030 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CL020 12PF 5% 25V NP0-C0G 0201
VBAT

PLACE_NEAR=UL000.14:4MM
PLACE_NEAR=UL000.14:3MM
PLACE_NEAR=UL000.14:3MM PP3V8_AON_WLBT 69 92
CL006 10UF 20% 10V X5R-CERM 0402-8
CRITICAL CL031 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CL021 12PF 5% 25V NP0-C0G 0201
2GFEM

PLACE_NEAR=UL000.38:4MM
PLACE_NEAR=UL000.38:3MM
PLACE_NEAR=UL000.38:3MM PP3V8_AON_WLBT 69 92
CL007 10UF 20% 10V X5R-CERM 0402-8
CRITICAL CL032 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CL022 12PF 5% 25V NP0-C0G 0201
5GFEM_C0

PLACE_NEAR=UL000.76:4MM
PLACE_NEAR=UL000.76:3MM
PLACE_NEAR=UL000.76:3MM PP3V8_AON_WLBT 69 92
CL008 10UF 20% 10V X5R-CERM 0402-8
CRITICAL CL033 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CL023 12PF 5% 25V NP0-C0G 0201
5GFEM_C1

PLACE_NEAR=UL000.23:4MM
PLACE_NEAR=UL000.23:3MM PP1V8_S2 69 92
CL010 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL CL024 12PF 5% 25V NP0-C0G 0201
2GFEM_C0

PLACE_NEAR=UL000.4:4MM
PLACE_NEAR=UL000.4:3MM PP1V8_S2 69 92
CL011 10UF 20% 10V X5R-CERM 0402-8
CRITICAL CL025 12PF 5% 25V NP0-C0G 0201
2GFEM_C1

PLACE_NEAR=UL000.33:4MM
PLACE_NEAR=UL000.33:3MM PP1V8_S2 69 92
CL012 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL CL034 3.0PF +/-0.1PF 25V NP0-C0G 0201
5GFEM_C0

PLACE_NEAR=UL000.82:4MM
PLACE_NEAR=UL000.82:3MM PP1V8_S2 69 92
CL013 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL CL035 3.0PF +/-0.1PF 25V NP0-C0G 0201
5GFEM_C1

PP1V8_S2 92 69
PP3V8_AON_WLBT 92 69
PP1V25_S2 92
PLACE_NEAR=UL000.51:4MM
CL014 0.1UF 10% 6.3V CERM-X5R 0201

UL000
2103-601908-80
LGA
SYM 1 OF 4
OMIT_TABLE

70 BI	RF_ANT_0	NO_TEST=1	28	ANT_X
70 BI	RF_ANT_1	NO_TEST=1	87	ANT_Y
96 70 BI	NC_RF_BT_DED	NO_TEST=1	72	BT_DEDICATED
	NC_BT_GPIO_2	NO_TEST=1	431	BT_GPIO_2
70 69 9 OUT	BT_TIME_SYNC		36	BT_GPIO_3
	NC_BT_GPIO_4	NO_TEST=1	43	BT_GPIO_4
	NC_BT_GPIO_5	NO_TEST=1	128	BT_GPIO_5
69 13 IN	SPMI_WLBT_CLK		119	SPMI_HEB_CLK
69 13 BI	SPMI_WLBT_DATA		321	SPMI_HEB_DAT
69	BT_LHL_GPIO2		136	LHL_GPIO2
	NC_SPMI_IDC_CLK		120	SPMI_IDC_CLK
	NC_SPMI_IDC_DATA		343	SPMI_IDC_DAT
70 69 42 IN	WLBT_PWR_EN		41	WLBT_REG_ON
70 69 40 IN	PMU_CLK32K_WLBT		515	WLBT_CLK_32K
69	WLAN_JTAG_SEL		54	JTAG_SEL
			497	SFLASH_OPTION_2

RL002 10K 5% 1/20W TK 0201

TYPHOON ES2.X

WL_GPIO_0	126	WLBT_WAKE	OUT	42 69 70
WL_GPIO_2	388	TPT_WLAN_JTAG_TCK		69 70 96
WL_GPIO_3	410	TPT_WLAN_JTAG_TMS		69 70 96
WL_GPIO_4	500	TPT_WLAN_JTAG_TDI		69 96
WL_GPIO_5	501	WLAN_TIME_SYNC	OUT	9 69 70
WL_GPIO_6	366	TPT_WLAN_JTAG_TRSTN		69 96
WL_GPIO_7	137	WL_GPIO_7		69
WL_GPIO_8	151	UART_WLAN_R2D_R		69
WL_GPIO_9	150	UART_WLAN_D2R_R		69
WL_GPIO_10	498	UART_WLAN_R2D_RTS_L_R		69
WL_GPIO_11	499	UART_WLAN_D2R_CTS_L_R		69
WL_GPIO_12	453	NC_WL_GPIO_12	NO_TEST=1	
WL_GPIO_13	160	NC_WL_GPIO_13	NO_TEST=1	
WL_GPIO_14	159	NC_WL_GPIO_14	NO_TEST=1	
WL_GPIO_15	475	NC_WL_GPIO_15	NO_TEST=1	
WL_GPIO_16	513	NC_WL_GPIO_16	NO_TEST=1	
WL_GPIO_18	512	NC_WL_GPIO_18	NO_TEST=1	
WL_GPIO_19	476	NC_WL_GPIO_19	NO_TEST=1	
WLBT_PCIE_PERST_L	505	WLBT_RESET_L	IN	10 69 70
WLBT_PCIE_CLKREQ_L	508	WLBT_CLKREQ_R_L		69
WLBT_PCIE_RXD_P	145	PCIE_WLBT_R2D_P		69
WLBT_PCIE_RXD_N	146	PCIE_WLBT_R2D_N		69
WLBT_PCIE_TXD_P	142	PCIE_WLBT_D2R_C_P		69
WLBT_PCIE_TXD_N	143	PCIE_WLBT_D2R_C_N		69
WLBT_PCIE_REFCLK_P	139	PCIE_CLK100M_WLBT_P	IN	10 69
WLBT_PCIE_REFCLK_N	140	PCIE_CLK100M_WLBT_N	IN	10 69

TPL001 A TP-P5 PMU_CLK32K_WLBT 40 69 70
TPL002 A TP-P5 WLBT_PWR_EN 42 69 70
TPL003 A TP-P5 WLBT_WAKE 42 69 70
TPL004 A TP-P5 TPT_WLAN_JTAG_TCK 69 70 96
TPL005 A TP-P5 TPT_WLAN_JTAG_TMS 69 70 96
TPL006 A TP-P5 TPT_WLAN_JTAG_TDI 69 96
TPL007 A TP-P5 WLAN_TIME_SYNC 9 69 70
WLAN_JTAG_TDO
TPL008 A TP-P5 TPT_WLAN_JTAG_TRSTN 69 96
TPL009 A TP-P5 WLAN_JTAG_SEL 69
TPL010 A TP-P5 BT_TIME_SYNC 9 69 70
TPL011 A TP-P5 UART_WLAN_R2D_R 69
TPL012 A TP-P5 UART_WLAN_D2R_R 69
TPL013 A TP-P5 UART_WLAN_R2D_RTS_L_R 69
TPL014 A TP-P5 UART_WLAN_D2R_CTS_L_R 69

TPL018 A TP-P5 SPMI_WLBT_CLK 13 69
TPL019 A TP-P5 SPMI_WLBT_DATA 13 69
TPL020 A TP-P5 BT_LHL_GPIO2 69

PACK_IGNORE=TRUE
PACK_OPTION=WLBT_TP_0P4
TPL028 A TP-R4
PACK_IGNORE=TRUE
PACK_OPTION=WLBT_TP_0P4
TPL029 A TP-R4
P2MM SM PP PPL021 1 PACK_OPTION=WLBT_TP_0P2 PCIE_CLK100M_WLBT_P 10 69
PLACE_SIDE=BOTTOM
P2MM SM PP PPL022 1 PACK_OPTION=WLBT_TP_0P2 PCIE_CLK100M_WLBT_N 10 69
PLACE_SIDE=BOTTOM

TPL023 A TP-P5 WLBT_RESET_L 10 69 70
TPL024 A TP-P5 WLBT_CLKREQ_L 10 69 70
TPL025 A TP-P5 WL_GPIO_7 69
PACK_IGNORE=TRUE
PACK_OPTION=WLBT_D2R_TP_JADE
PLACE_NEAR=UL000.A41:10MM
P2MM SM PP PPL026 1 PCIE_WLBT_D2R_P 10 69
PLACE_SIDE=BOTTOM
PACK_IGNORE=TRUE
PACK_OPTION=WLBT_D2R_TP_JADE
PLACE_NEAR=UL000.B41:10MM
P2MM SM PP PPL027 1 PCIE_WLBT_D2R_N 10 69
PLACE_SIDE=BOTTOM

GND_VOID=TRUE
PLACE_NEAR=UL000.145:4MM
CL001 0.1UF 10% 6.3V CERM-X5R 0201
10 IN PCIE_WLBT_R2D_C_P — PCIE_WLBT_R2D_P 69
CL002 0.1UF 10% 6.3V CERM-X5R 0201
10 IN PCIE_WLBT_R2D_C_N — PCIE_WLBT_R2D_N 69
PLACE_NEAR=UL000.146:4MM
GND_VOID=TRUE

69 13 SPMI_WLBT_CLK — RL003 51K JK 0201 1/20W 5%
69 13 SPMI_WLBT_DATA — RL004 51K JK 0201 1/20W 5%

GND_VOID=TRUE
PACK_IGNORE=TRUE
PACK_OPTION=WLBT_D2R_TP_JADE
PLACE_NEAR=UL000.142:4MM
CL003 0.1UF 10% 6.3V CERM-X5R 0201
69 PCIE_WLBT_D2R_C_P — PCIE_WLBT_D2R_P OUT 10 69
CL004 0.1UF 10% 6.3V CERM-X5R 0201
69 PCIE_WLBT_D2R_C_N — PCIE_WLBT_D2R_N OUT 10 69
PLACE_NEAR=UL000.143:4MM
PACK_IGNORE=TRUE
PACK_OPTION=WLBT_D2R_TP_JADE
GND_VOID=TRUE

GND_VOID=TRUE
PACK_OPTION=WLBT_D2R_TP_STATEN
PLACE_NEAR=U0600.BF29:10MM
CL043 0.1UF 10% 6.3V CERM-X5R 0201
69 PCIE_WLBT_D2R_C_P — PCIE_WLBT_D2R_P 10 69
CL044 0.1UF 10% 6.3V CERM-X5R 0201
69 PCIE_WLBT_D2R_C_N — PCIE_WLBT_D2R_N 10 69
GND_VOID=TRUE
PLACE_NEAR=U0600.BG29:10MM
PACK_OPTION=WLBT_D2R_TP_STATEN

69 WLBT_CLKREQ_R_L — RL001 1K 0201-1 1/20W 5% 1K — WLBT_CLKREQ_L BI 10 69 70

BOM_COST_GROUP=WIRELESS

TYPHOON BOM TABLE:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S00912	1	MODULE,WLAN/BT,TYPHOON, ES4.7	UL000	CRITICAL	

PAGE TITLE: WIFI/BT: MODULE

Apple Inc.

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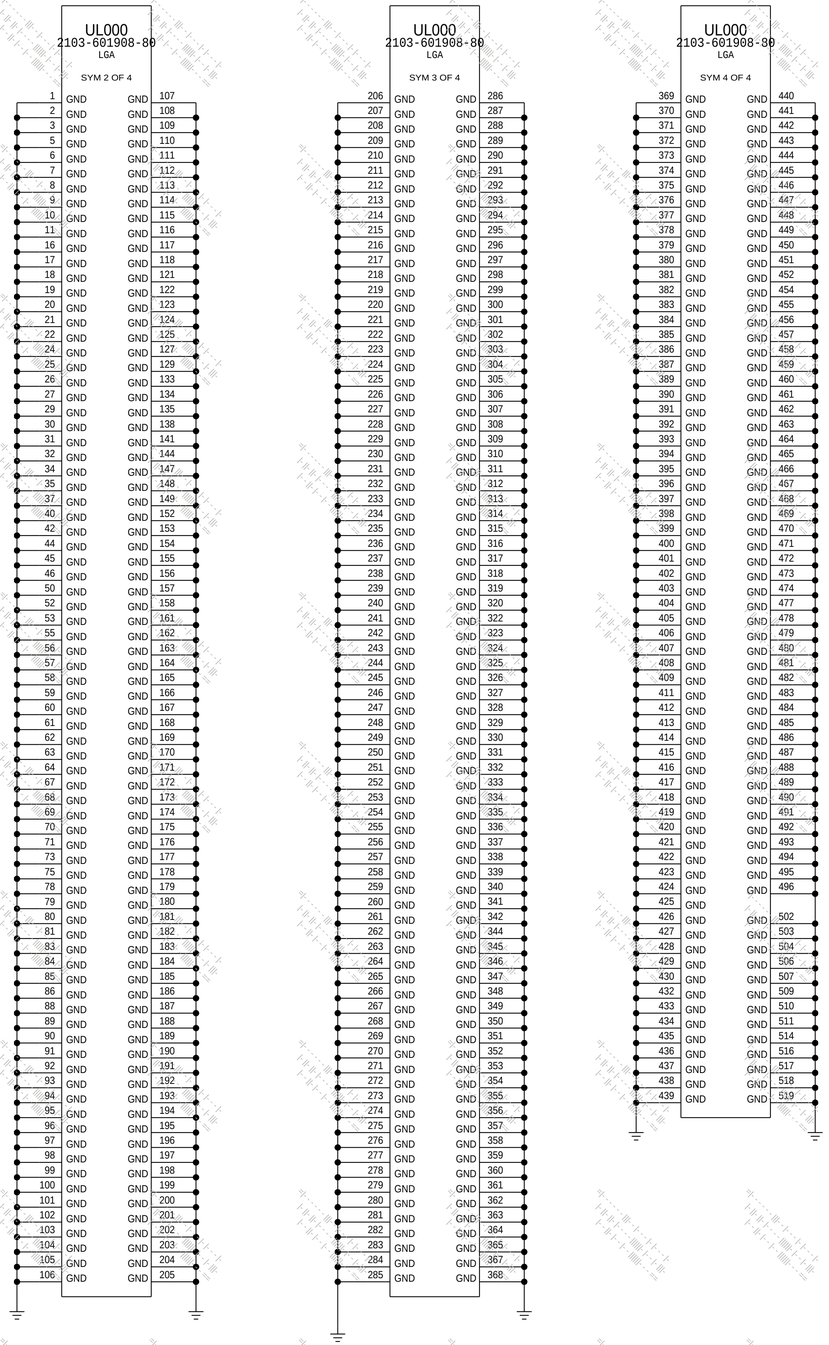
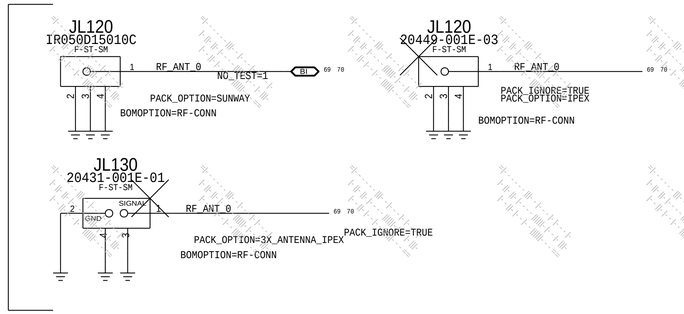
TYPHOON WIFI/BT MODULE GND

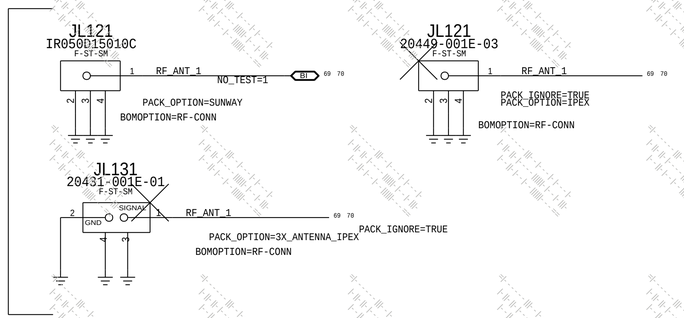


ANTENNA CONNECTORS

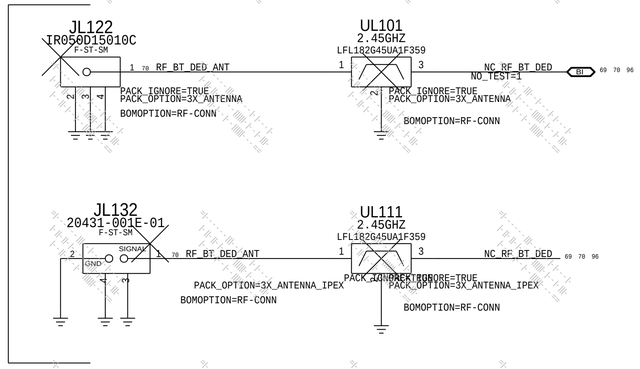
2G_C0
5G_C0
BT_C0



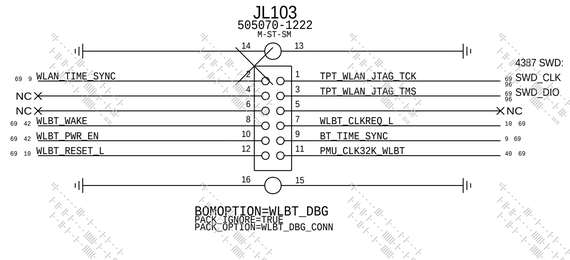
2G_C1
5G_C1
BT_C1



BT_C1_DED



WLBT DEBUG CONNECTOR



BOM_COST_GROUP=WIRELESS

PAGE TITLE
WIFI/BT: ANTENNA and GND

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*** OK2INTEGRATE ***

NAND0 S5E0

PP1V25_AWAKE_NAND_VCCQ

CN030 4.3UF 20% 4V CERM 0402-THICK&TNCL

PACK_OPTION=SSD_4_3UF_0402THICK
PACK_IGNORE=TRUE

PACK_OPTION=SSD_4_3UF_0402THIN

CN030 4.3UF 20% 4V CERM 0402

PP1V25_AWAKE_NAND_VCCQ

CN032 20UF 20% 10V X5R 0402

CN034 2.2UF 20% 10V X5R 0201

CN035 2.2UF 20% 10V X5R 0201

CN036 2.2UF 20% 10V X5R 0201

CN037 2.2UF 20% 10V X5R 0201

CN038 2.2UF 20% 10V X5R 0201

CN039 2.2UF 20% 10V X5R 0201

CN03A 2.2UF 20% 10V X5R 0201

PP0V88_AWAKE_NAND_VDD

CN010 20UF 20% 10V X5R 0402

CN011 20UF 20% 10V X5R 0402

CN012 2.2UF 20% 10V X5R 0201

CN013 2.2UF 20% 10V X5R 0201

CN014 2.2UF 20% 10V X5R 0201

CN015 0.1UF 10% 6.3V CERM-X5R 0201

CN016 0.1UF 10% 6.3V CERM-X5R 0201

CN017 0.1UF 10% 6.3V CERM-X5R 0201

TPT_NAND0_S5E0_ANI1_VREF

TPT_NAND0_S5E0_ANI0_VREF

PP2V58_AWAKE_NAND_VCC

CN020 20UF 20% 10V X5R 0402

CN022 2.2UF 20% 10V X5R 0201

CN023 2.2UF 20% 10V X5R 0201

CN024 2.2UF 20% 10V X5R 0201

CN025 2.2UF 20% 10V X5R 0201

PP1V25_AWAKE_NAND_VCCQ

RN010 2 1% 1/20W TK 0201

PLACE_NEAR=UN000.L2:10MM

CN047 2.2UF 20% 10V X5R 0201

CN046 0.1UF 10% 6.3V CERM-X5R 0201

MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000

PP1V2_NAND0_S5E0_AVDD1X_PLL

FLN000 10OHM-50%-1A-0.050HM 0201

PLACE_NEAR=UN000.J6:10MM

PP1V2_NAND0_S5E0_PCI_AVDD_H

CN045 4.7UF 20% 6.3V CER-X5R 0201

CN044 0.1UF 10% 6.3V CERM-X5R 0201

The inductance from CN047, CN046, CN045, CN044 to their S5E pins shall be less than 1100pH

MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000

PP0V9_NAND0_S5E0_VDD_PLL

NC_NAND0_S5E0_VPP

FLN001 10OHM-50%-1A-0.050HM 0201

PLACE_NEAR=UN000.R4:10MM

PP0V88_AWAKE_NAND_VDD

PLACE_NEAR=FLN001.2:5MM

CN083 4.7UF 20% 4V CER-X5R 0201

J6 PCIE_AVDD_H
J8 PCIE_VDD
W9 PCIE_VDD
N6 PCIE_VDD
N8 PCIE_VDD
L2 AVDD1X_PLL
G12 AN0_VREF
J4 AN1_VREF
G6 VDD
G8 VDD
L6 VDD
L8 VDD
R6 VDD
R8 VDD
J2 VDDIO_1
K9 VDDIO_1
T5 VDDIO_1
E10 VDDIO_2
E2 VDDIO_2
N2 VDDIO_2
P9 VDDIO_2
D3 VCC
E12 VCC
G4 VCC
L12 VCC
R2 VCC
R4 VDD_PLL
F3 VPP
F5 VDP5

CN085 10PF 5% 25V C0G 0201

RN004 200 0.1% 1/20W TK 0201-2

GND_VOID=TRUE

CN003 0.22UF 10% 6.3V X5R-CERM 0201

CN004 0.22UF 10% 6.3V X5R-CERM 0201

CN001 0.22UF 10% 6.3V X5R-CERM 0201

CN002 0.22UF 10% 6.3V X5R-CERM 0201

PCIE_NAND0_R2D_C_P<0>
PCIE_NAND0_R2D_C_N<0>
PCIE_NAND0_D2R_P<0>
PCIE_NAND0_D2R_N<0>

NAND0_CLK24M_0 M3 CLK_IN
PCIE_CLK100M_NAND0_0_P K11 PCIE_REFCLK_P
PCIE_CLK100M_NAND0_0_N J12 PCIE_REFCLK_N
NAND0_CLKREQ0_R_L P5 PCIE_CLKREQ*
NAND0_S5E0_PCIE_RESREF H7 PCIE_RESREF
PCIE_NAND0_R2D_P<0> M11 PCIE_RX0_P
PCIE_NAND0_R2D_N<0> N12 PCIE_RX0_N
PCIE_NAND0_D2R_C_P<0> R12 PCIE_TX0_P
PCIE_NAND0_D2R_C_N<0> T11 PCIE_TX0_N

OMIT_TABLE

UN000 S5E-MCP-STUDY LGA

NAND0_RESET_L L4 RESET*
NAND0_JTAG_TRST_L G10 TRST*
NAND0_S5E0_ZQ_0 C10 ZQ_0
NAND0_S5E0_ZQ_1 K3 ZQ_1

PLACE_NEAR=UN000.C10:15MM

RN006 300 1% 1/20W TK 0201

PLACE_NEAR=UN000.K3:15MM

RN005 300 1% 1/20W TK 0201

VSS

A12 A2 B1 B13 C12 C2 D1 D13 F1 F11 F13 F7 F9 H1 H11 H13 H3 H5 H9 J10 K1 K13 K5 K7 L10 M1 M13 M5 M7 N10 N4 P1 P11 P13 P3 P7 R10 T1 T13 T7 T9 U12 U2

VSS_R

A10 A4 A6 A8 U10 U4 U6 U8

EXT_D0/BOOT0 B3 NAND0_LPB_L
EXT_D1/BOOT1 C4 NAND_BFH
EXT_D2/BOOT2/SPINAND_SCLK B5 NAND0_BOOT2
EXT_D3/SWD_UID0/SPINAND_MISO C6 NAND0_S5E0_SWD_UID0
EXT_D4/SPI_CS B7
EXT_D5/SWD_UID1/SPINAND_MOSI C8 NAND0_S5E0_SWD_UID1
EXT_D6/BOOT3 B9
EXT_D7/SPF B11 NAND0_PFN_L
EXT_DQS/BCM* D11 NAND0_BCM_L
EXT_NCE/PERST* E8 NAND0_PCIE_RESET_L
EXT_NRE/JTAG_TMS D7 SWD_NAND0_S5E0_SWDIO
EXT_NWE/JTAG_TCK E6 SWD_NAND0_S5E0_SWCLK
EXT_RNB/JTAG_TDO E4 NAND0_S5E0_JTAG_TDO
EXT_CLE/JTAG_TDI D5 TPT_NAND0_S5E0_JTAG_TDI
EXT_ALE/JTAG_SEL D9 NAND0_JTAG_SEL
DROOP* T3 TPT_NAND0_S5E0_DROOP_L
WP* G2 NAND0_WP_L

NAND0_BOOT2
NAND0_JTAG_SEL
NAND0_JTAG_TRST_L

RN000 47K 1% 1/20W TK 0201

RN002 47K 1% 1/20W TK 0201

RN021 0 0% 1/20W TK 0201

Spec recommends to tie Boot2 directly to Gnd

PP1V25_AWAKE_NAND_VCCQ

RN001 0 0% 1/20W TK 0201

RN007 0 0% 1/20W TK 0201

NAND0_BCM_L
NAND0_WP_L

Spec recommends to tie BCM, WP directly to 1.2V rail

NAND0_S5E0_SWD_UID0
NAND0_S5E0_SWD_UID1

RN009 47K 1% 1/20W TK 0201

RN008 47K 1% 1/20W TK 0201

BOM_COST_GROUP=SSD

SYNC_MASTER=
SYNC_DATE=09/10/2021

PAGE TITLE

STORAGE: SSD0 S5E <0>

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*** OK2INTEGRATE ***

NAND0 S5E1

PP1V25_AWAKE_NAND_VCCQ

SSD_2L CN130 4.3UF 20% 4V CERM 0402-THICKSTNCL

PACK_OPTION=SSD_4_3UF_0402THICK
PACK_IGNORE=TRUE

PACK_OPTION=SSD_4_3UF_0402THIN

93 72 PP0V88_AWAKE_NAND_VDD

SSD_2L CN110 20UF 20% 10V X5R 0402
SSD_2L CN111 20UF 20% 10V X5R 0402
SSD_2L CN112 2.2UF 20% 10V X5R 0201
SSD_2L CN113 2.2UF 20% 10V X5R 0201
SSD_2L CN114 2.2UF 20% 10V X5R 0201
SSD_2L CN115 0.1UF 10% 6.3V CERM-X5R 0201
SSD_2L CN116 0.1UF 10% 6.3V CERM-X5R 0201
SSD_2L CN117 0.1UF 10% 6.3V CERM-X5R 0201

SSD_2L CN132 20UF 20% 10V X5R 0402
SSD_2L CN134 2.2UF 20% 10V X5R 0201
SSD_2L CN135 2.2UF 20% 10V X5R 0201
SSD_2L CN136 2.2UF 20% 10V X5R 0201
SSD_2L CN137 2.2UF 20% 10V X5R 0201
SSD_2L CN138 2.2UF 20% 10V X5R 0201
SSD_2L CN139 2.2UF 20% 10V X5R 0201
SSD_2L CN13A 2.2UF 20% 10V X5R 0201

PP1V25_AWAKE_NAND_VCCQ 71 72 93

73 TPT_NAND0_S5E1_ANI1_VREF
73 TPT_NAND0_S5E1_ANI0_VREF

PP2V58_AWAKE_NAND_VCC 71 92

SSD_2L CN120 20UF 20% 10V X5R 0402
SSD_2L CN122 2.2UF 20% 10V X5R 0201
SSD_2L CN123 2.2UF 20% 10V X5R 0201
SSD_2L CN124 2.2UF 20% 10V X5R 0201
SSD_2L CN125 2.2UF 20% 10V X5R 0201

SSD_2L RN110 2 1% 1/20W TK 0201
PP1V25_AWAKE_NAND_VCCQ
PLACE_NEAR=UN100.L2:10MM

MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000

SSD_2L CN147 2.2UF 20% 10V X5R 0201
SSD_2L CN146 0.1UF 10% 6.3V CERM-X5R 0201
PP1V2_NAND0_S5E1_AVDD1X_PLL

SSD_2L FLN100 100HM-50%-1A-0.050HM 0201
PLACE_NEAR=UN100.J6:10MM

MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000

SSD_2L CN145 4.7UF 20% 6.3V CER-X5R 0201
SSD_2L CN144 0.1UF 10% 6.3V CERM-X5R 0201
PP1V2_NAND0_S5E1_PCI_AVDD_H

The inductance from CN147, CN146, CN145, CN144 to their S5E pins shall be less than 1100pH

MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000

PP0V9_NAND0_S5E1_VDD_PLL

SSD_2L FLN101 100HM-50%-1A-0.050HM 0201
PLACE_NEAR=UN100.R4:10MM

PP0V88_AWAKE_NAND_VDD 72 93

PLACE_NEAR=FLN101.2:5MM
SSD_2L CN183 4.7UF 20% 4V CER-X5R 0201

NC_NAND0_S5E1_VPP 96

J6	J8	W9	N6	N8	L2	G12	J4	G6	G8	L6	L8	R6	R8	J2	K9	T5	E10	E2	N2	P9	D3	E12	G4	L12	R2	R4	F3	F5
PCIE_AVDD_H	PCIE_VDD	PCIE_VDD	PCIE_VDD	PCIE_VDD	AVDD1X_PLL	AN0_VREF	AN1_VREF	VDD						VDDIO_1				VDDIO_2				VCC				VDD_PLL	VPP	VDP5

SSD_2L CN185 10PF 5% 25V C0G 0201
SSD_2L RN104 200 0.1% 1/20W TK 0201-2

73 IN	NAND0_CLK24M_1	M3	CLK_IN	
10 IN	PCIE_CLK100M_NAND0_1_P	K11	PCIE_REFCLK_P	
10 IN	PCIE_CLK100M_NAND0_1_N	J12	PCIE_REFCLK_N	
73 OUT	NAND0_CLKREQ1_R_L	P5	PCIE_CLKREQ*	
	NAND0_S5E1_PCIE_RESREF	H7	PCIE_RESREF	
10 IN	PCIE_NAND0_R2D_C_P<1>	M11	PCIE_RX0_P	
10 IN	PCIE_NAND0_R2D_C_N<1>	N12	PCIE_RX0_N	
10 OUT	PCIE_NAND0_D2R_P<1>	R12	PCIE_TX0_P	
10 OUT	PCIE_NAND0_D2R_N<1>	T11	PCIE_TX0_N	

SSD_2L CN103 0.22UF 10% 6.3V X5R-CERM 0201 GND_VOID=TRUE
SSD_2L CN104 0.22UF 10% 6.3V X5R-CERM 0201 GND_VOID=TRUE
SSD_2L CN101 0.22UF 10% 6.3V X5R-CERM 0201 GND_VOID=TRUE
SSD_2L CN102 0.22UF 10% 6.3V X5R-CERM 0201 GND_VOID=TRUE

OMIT_TABLE
UN100
S5E-MCP-STUDY
LGA

	EXT_D0/BOOT0	B3	NAND0_LPB_L	IN 42 71
	EXT_D1/BOOT1	C4	NAND_BFH	IN 8 71
	EXT_D2/BOOT2/SPINAND_SCLK	B5	NAND0_BOOT2	71
	EXT_D3/SWD_UID0/SPINAND_MISO	C6	NAND0_S5E1_SWD_UID0	72
	EXT_D4/SPI_CS	B7		
	EXT_D5/SWD_UID1/SPINAND_MOSI	C8	NAND0_S5E1_SWD_UID1	72
	EXT_D6/BOOT3	B9		
	EXT_D7/SPF	B11	NAND0_PFN_L	IN 71 73
	EXT_DQS/BCM*	D11	NAND0_BCM_L	IN 71
	EXT_NCE/PERST*	E8	NAND0_PCIE_RESET_L	IN 10 71
	EXT_NRE/JTAG_TMS	D7	SWD_NAND0_S5E1_SWDIO	IN 13
	EXT_NWE/JTAG_TCK	E6	SWD_NAND0_S5E1_SWCLK	IN 13
	EXT_RNB/JTAG_TDO	E4	TPT_NAND0_S5E1_JTAG_TDO	OUT 73
	EXT_CLE/JTAG_TDI	D5	NAND0_S5E0_JTAG_TDO	IN 71
	EXT_ALE/JTAG_SEL	D9	NAND0_JTAG_SEL	IN 71
	DROOP*	T3	TPT_NAND0_S5E1_DROOP_L	73
	WP*	G2	NAND0_WP_L	IN 71

71 8 IN NAND0_RESET_L → L4 RESET*
71 IN NAND0_JTAG_TRST_L → G10 TRST*
NAND0_S5E1_ZQ_0 → C10 ZQ_0
NAND0_S5E1_ZQ_1 → K3 ZQ_1

PLACE_NEAR=UN100.C10:15MM
SSD_2L RN106 300 1% 1/20W TK 0201

PLACE_NEAR=UN100.K3:15MM
SSD_2L RN105 300 1% 1/20W TK 0201

A12	A2	B1	B13	C12	C2	D1	D13	F1	F11	F13	F7	F9	H1	H11	H13	H3	H5	H9	J10	K1	K13	K5	K7	L10	M1	M13	M5	M7	N10	N4	P1	P11	P13	P3	P7	R10	T1	T13	T7	T9	U12	U2	A10	A4	A6	A8	U10	U4	U6	U8
	VSS																																									VSS_R								

PP1V25_AWAKE_NAND_VCCQ 71 72 93

SSD_2L RN108 47K 1% 1/20W TK 0201
72 NAND0_S5E1_SWD_UID0

SSD_2L RN109 47K 1% 1/20W TK 0201
72 NAND0_S5E1_SWD_UID1

BOM_COST_GROUP=SSD

SYNC_MASTER=
SYNC_DATE=09/10/2021

PAGE TITLE: STORAGE: SSD0 S5E <1>

Apple Inc.

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REVISION: 6.0.0
BRANCH: evt-1
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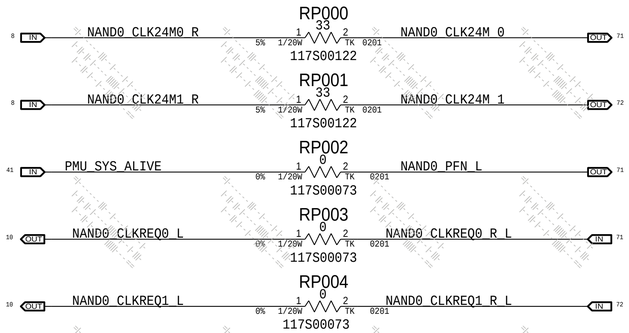
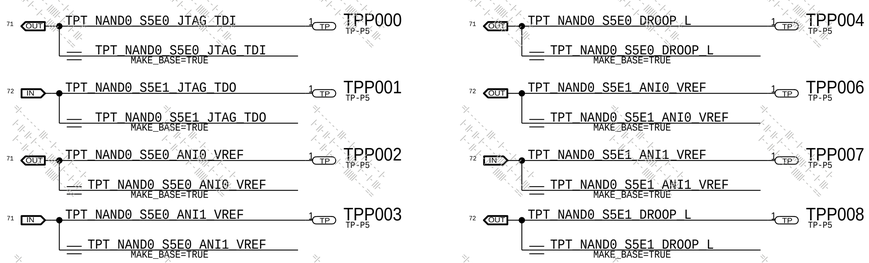
A SSD Termination Resistors



B S5E Test Points



BOM_COST_GROUP=SSD

SYNC_MASTER=
SYNC_DATE=09/10/2021

PAGE TITLE
STORAGE: SSD Support

Apple Inc.

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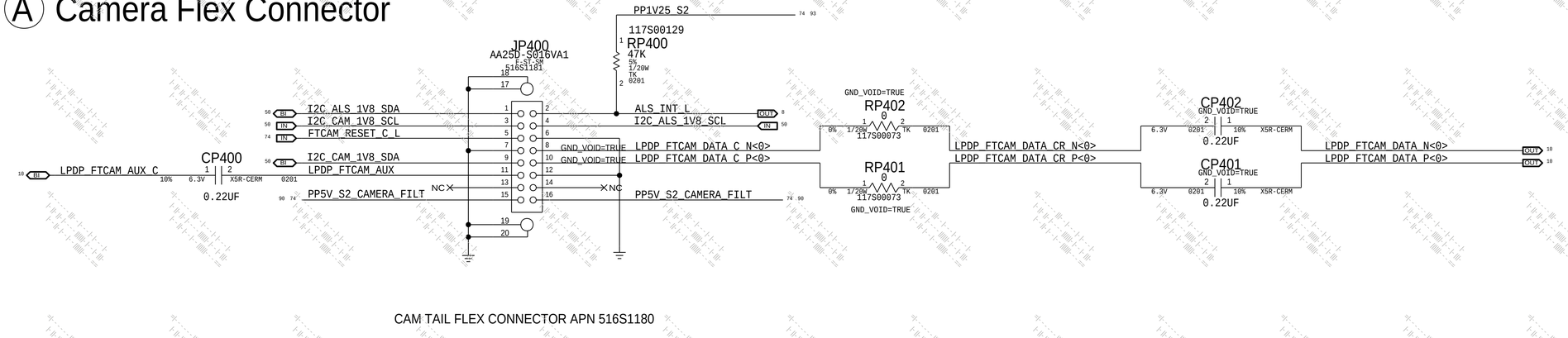
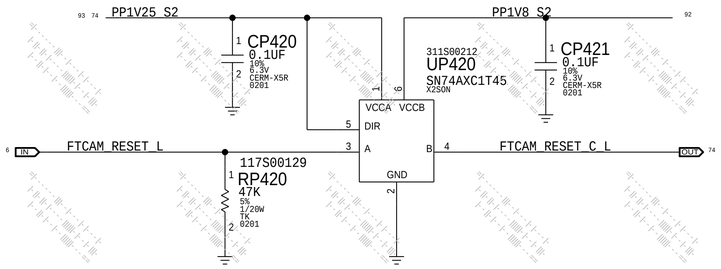
A Camera Flex Connector

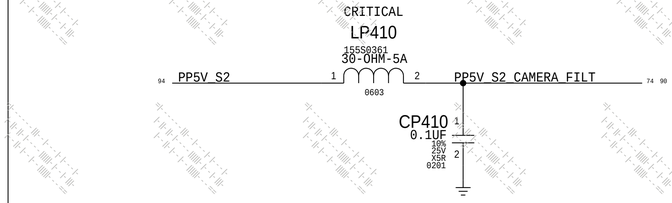


CAM TAIL FLEX CONNECTOR APN 516S1180

B Camera Reset Level Shifter



C Camera Power Filter(s)



BOM_COST_GROUP=CAMERA

SYNC_MASTER=	SYNC_DATE=09/10/2021
PAGE TITLE	CAMERA: FLEX CONNECTOR
Apple Inc.	DRAWING NUMBER 051-07020 · SIZE D
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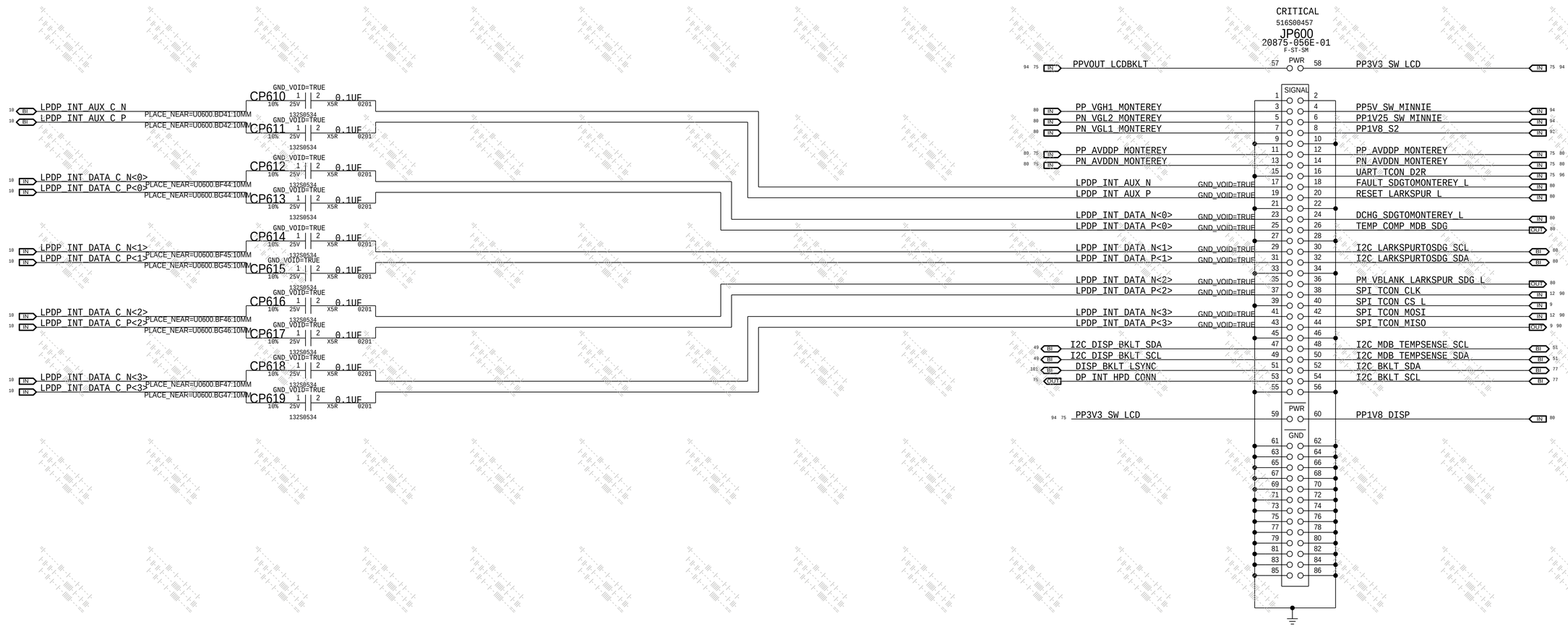
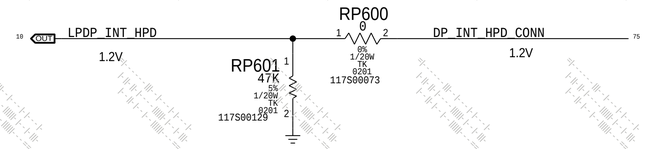
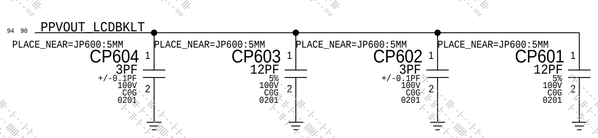
A LCD Panel Interface



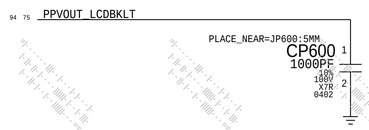
B LCD Panel Support



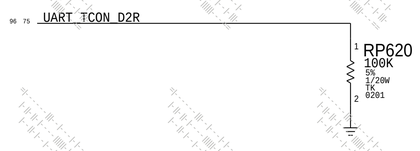
C LCD Panel Desense



D LCD Panel Bypass



E UART PULLDOWN



BOM_COST_GROUP=DISPLAY

SYNC_MASTER:
SYNC_DATE=09/10/2021

PAGE TITLE
eDP Display Connector

Apple Inc.

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*** OK2INTEGRATE ***

93 PP1V25_S2

CAN BE EITHER 1.2V OR 1.8V

94 PP5V_S2

CONSULT YOUR DISPLAY DRI FOR DETAILS
GENERAL GUIDELINE IS
3V3 FOR 2020 SYSTEMS
3V8 FOR 2021 SYSTEMS

94 PP3V3_S2

92 PP1V8_S2

BYPASS=UP710::3MM
CP770
0.1UF
10%
10V
X5R-CERM
0201

UP710
SLG4AP43605V
STQFN

42 LCD_PWR_EN → PANEL_EN_IN (2)
96 PMU_SYS_ALIVE → SYS_ALIVE (3)
NC (5) NC (6) NC (7) NC (8) NC (12)
PANEL_EN_OUT (11) → EDP_PANEL_1V8_EN → 80
PANEL_PWR_EN (4) → EDP_PANEL_PWR_EN
BLC_VDDIO_EN (13) → EDP_BLC_VDDIO_EN
BLC_5V_EN (14) → EDP_BLC_5V_EN
PANEL_DISCHARGE (10) → EDP_PANEL_DISCHARGE
VDD (1), GND (9)

PACK_OPTION=PANELPWR_MINNIE
CP720
0.1UF
10%
10V
X5R-CERM
0201

PACK_OPTION=PANELPWR_MINNIE
CRITICAL
UP700
SLG5AP1451V
DFN
VDD (6), GND (7)
ON1 (3), ON2 (2)
D1 (4), S1 (5), D2 (1), S2 (8)

PACK_OPTION=PANELPWR_MINNIE
CP717
0.1UF
10%
10V
X5R-CERM
0201

PACK_OPTION=PANELPWR_MINNIE
PACK_OPTION=PANELPWR_MINNIE
PP1V25_SW_MINNIE 94
CP713
0.1UF
10%
10V
X5R-CERM
0201
CP714
10UF
20%
10V
X5R-CERM
0402-7

PACK_OPTION=PANELPWR_MINNIE
PACK_OPTION=PANELPWR_MINNIE
PP5V_SW_MINNIE 94
CP711
0.1UF
10%
10V
X5R-CERM
0201
CP712
10UF
20%
10V
X5R-CERM
0402-7

CRITICAL
UP701
SLG5AP1564V
STDFN
VDD (1), GND (8)
ON (2), D (3), S (5), PG (7) NC

CP710
1.0UF
20%
6.3V
X5R
0201-1

PP3V3_SW_LCD 94
CP718
0.1UF
10%
10V
X5R-CERM
0201
CP719
10UF
20%
10V
X5R-CERM
0402-7

116S00029
RP700
300
5%
1/16W
TK
0402

PPPANEL_PANEL_DISCHARGE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

376S1140
QP700
DMN2300UFB4
X2-DFN1006-3-COMBO
SYM_VER_1
G (1), D (3), S (2)

117S00095
RP701
100K
5%
1/20W
TK
0201

BOM_COST_GROUP=DISPLAY

PAGE TITLE: DISPLAY POWER SEQUENCER

Apple Inc.

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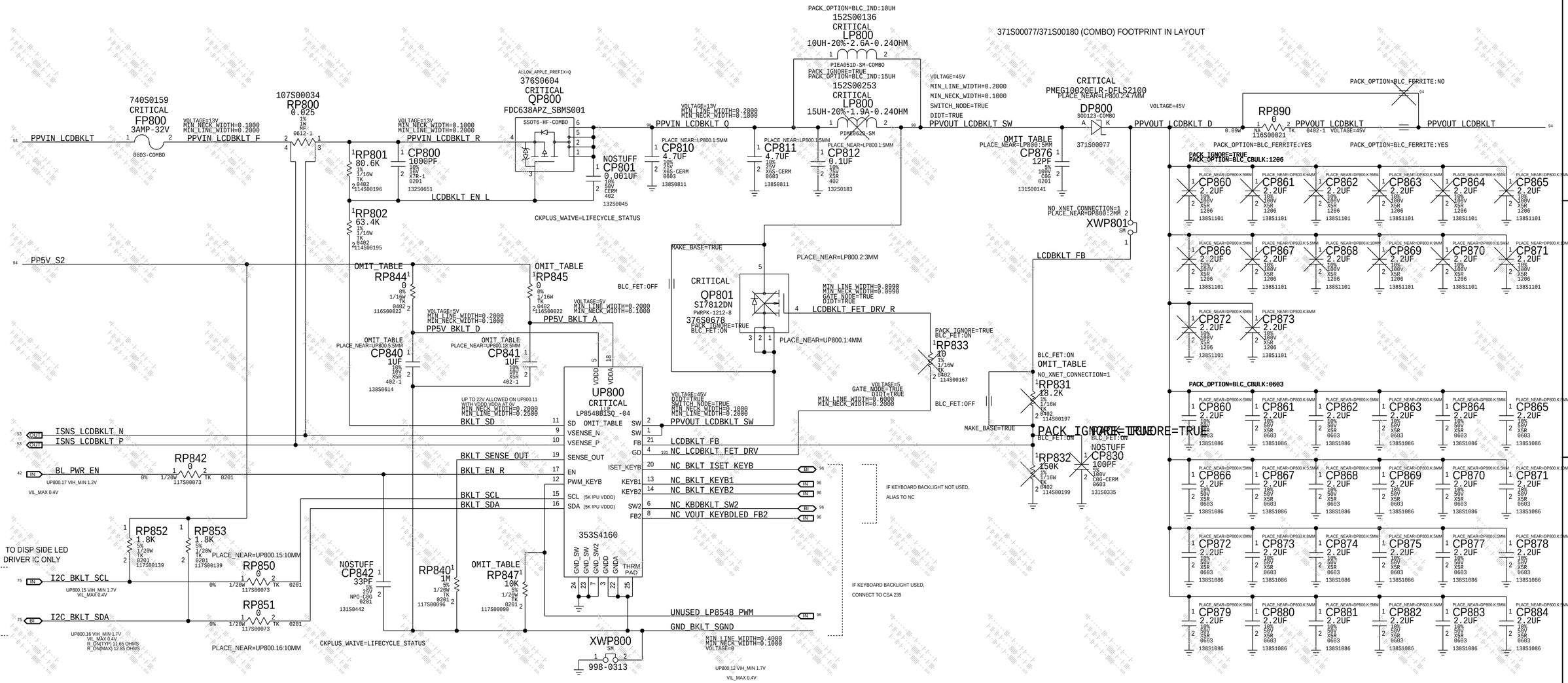
*** OK2INTEGRATE ***

BEN IC: DISPLAY/KBD BACKLIGHT BOOST CONVERTER



BEN IC VERSION TO MATCH VERSION OF JERRY/MINNIE IC IS ON THE PANEL

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S4160	1	IC,LP8548B1-04,DC/DC CVTR,BOOST,QFN-24	UP800		BLC_BEN_IC:V4
353S02256	1	IC,LP8548B1A-07,DC/DC BOOST CVTR,QFN24	UP800		BLC_BEN_IC:V7
353S02616	1	IC,LP8548B1A-08,DC/DC BOOST CVTR,QFN24	UP800		BLC_BEN_IC:V8

BACKLIGHT SWITCH NODE DESENSE OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S00141	1	CAP,C0G,12PF,5%,100V,0201	CP876		BLC_SW_NODE_DESENSE

10K IF KEYBOARD PWM INPUT IS NOT PRESENT (X941, X1536)
100K IF KEYBOARD PWM INPUT IS PRESENT (X1536)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S00090	1	RES,TK,10K OHM,5%,1/20W,0201	RP847		BLC_KBD_BOOST_USED:NO
118S00251	1	RES,TK,160K OHM,1%,1/20W,0201	RP847		BLC_KBD_BOOST_USED:YES

BACKLIGHT BOOST VOLTAGE LEVEL BASED ON NUMBER OF LEDS PER STRING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S00197	1	RES,TK,18.2KOHM,1%,1/16W,0402	RP831		BLC_LEDS_PER_STRING:16
114S00198	1	RES,TK,28.7KOHM,1%,1/16W,0402	RP831		BLC_LEDS_PER_STRING:18

BOM OPTION FOR BLC 5V RC FILTER, BASED ON PER PROJECT 5V RIPPLE CHARACTERIZATION.
AS COMPARED TO BLC TEAM'S 50 MV RIPPLE SPEC FOR VDDD & VDDA. SEE <RDAR://50682542>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S00022	2	RES,TK,0 OHM,2A MAX,1/16W,0402	RP844,RP845		BLC_5V_SERIES:0_OHM
114S00167	2	RES,TK,10 OHM,1%,1/16W,0402	RP844,RP845		BLC_5V_SERIES:10_OHM
138S0614	2	CAP,CER,X5R,1UF,10%,10V,0402	CP840,CP841		BLC_5V_CAP:1_UF
138S0070	2	CAP,CER,X5R,4.7UF,20%,25V,0402	CP840,CP841		BLC_5V_CAP:4P7_UF

BOM_COST_GROUP=DISPLAY

SYNC_MASTER=DisplayBacklight SYNC_DATE=09/26/2021

PAGE TITLE: BEN: CONTROLLER

Apple Inc.

DRAWING NUMBER: 051-07020 SIZE: D

REVISION: 6.0.0

BRANCH: evt-1

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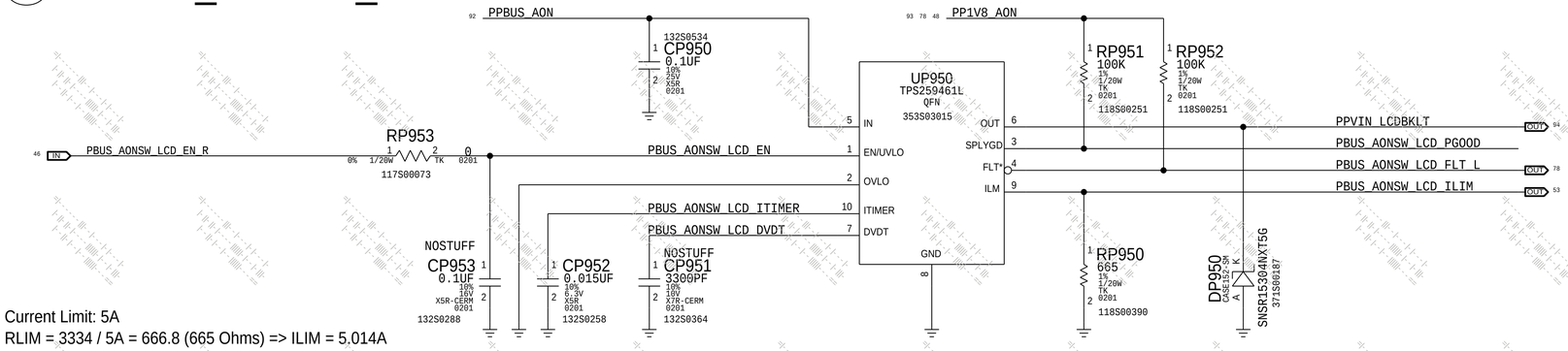
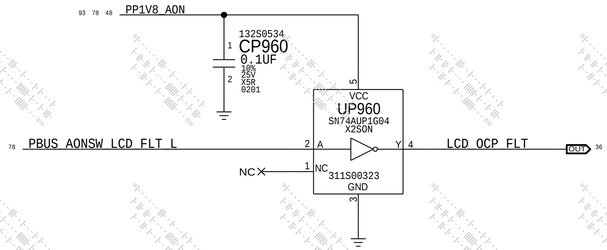
A PPBUS_AONSW_LCD Load Switch & e-Fuse



Current Limit: 5A
RLIM = 3334 / 5A = 666.8 (665 Ohms) => ILIM = 5.014A
/FLT Open Drain
Host-Controlled (EN = MPMU GPIO6, 1.8V LVCMOS (PP1V8_AON))

B LCD_OCP_FLT Control Logic



BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=
SYNC_DATE=09/10/2021
PAGE TITLE: BEN: PBUS E-Fuse
Apple Inc.
DRAWING NUMBER: 051-07020
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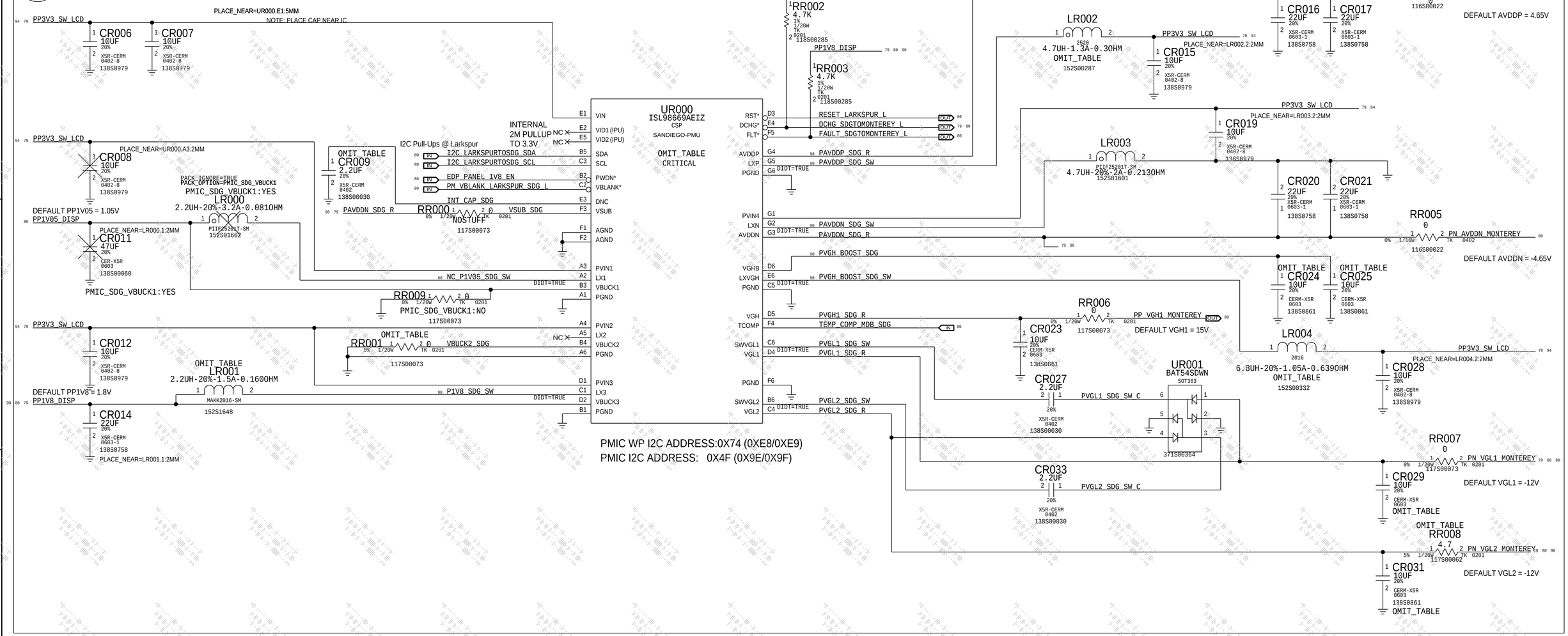
*** OK2INTEGRATE ***

A Display PMU IC



B BOMOPTIONs: TI vs. Intersil

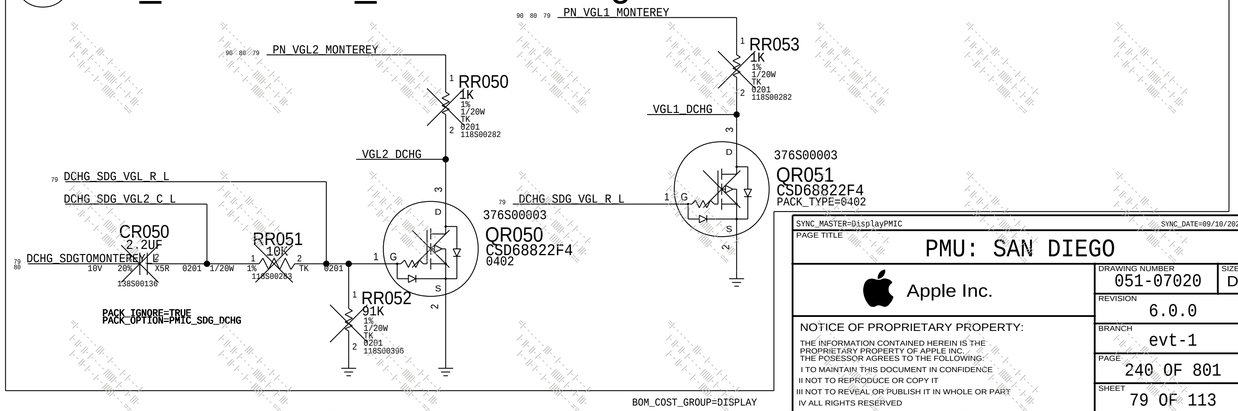
Texas Instruments Option Table

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S00844	1	IC,TPS65157B0E2,PMU,SAN DIEGO,BGA42	UR000	SDG_TI_PROG:X2203
338S00185	1	IC,TPS65157,SAN DIEGO,A1,DSBGA42	UR000	SDG_TI_PROG:BLANK
152S00289	2	IND,4.7UH,2016,PIYA2016T-4R7MDR	LR001	SDG_TI
152S01601	1	IND,MLD,4.7UH,20%,2A,0.213OHM,2520	LR002	SDG_TI
152S00332	1	IND,6.8UH,2016,PISA20161T6R8-013	LR004	SDG_TI
138S0861	2	CAP,CER,10UF,20%,35V,X5R,0603	CR029,CR031	SDG_TI
138S0861	2	CAP,CER,10UF.20%,35V,X5R,0603	CR024,CR025	SDG_TI
138S00030	1	CAP,CER,2.2UF.20%,35V,X5R,0402	CR009	SDG_TI
117S00073	1	RES,TK,0 OHM,1A MAX,1/20W,0201	RR008	SDG_TI

Intersil Option Table

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S00183	1	IC,ISL98669,SAN DIEGO,A1,CSP42	UR000	SDG_ISL
152S1648	2	IND,2.2UH,2016,MAKK2016T2R2M	LR001	SDG_ISL
152S00286	1	IND,2.2UH,2520,VLS252010HBX-2R2M	LR002	SDG_ISL
152S00483	1	IND,10UH,2016,LQE2MEN00MG0	LR004	SDG_ISL
138S0709	2	CAP,CER,4.7UF.10%,35V,X5R,0603	CR029,CR031	SDG_ISL
138S0709	2	CAP,CER,4.7UF.10%,35V,X5R,0603	CR024,CR025	SDG_ISL
116S00022	1	RES,0 OHM,1A,0402	CR009	SDG_ISL
117S00062	1	RES,TK,4.7 OHM,5%,1/20W,0201	RR008	SDG_ISL
117S00073	1	RES,TK,0 OHM,1A MAX,1/20W,0201	RR001	SDG_ISL

C PN_VGL1 & PN_VGL2 Discharge Circuit



SYNC_MASTER=DisplayPMIC SYNC_DATE=09/10/2021

PAGE TITLE: PMU: SAN DIEGO

Apple Inc.

DRAWING NUMBER: 051-07020 SIZE: D
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A Power Connections Alias

75	PP1V8_DISP MAKE_BASE=TRUE	=	PP1V8_DISP	79	90
	PP1V05_DISP MAKE_BASE=TRUE	=	PP1V05_DISP	79	
75	PN_VGL1_MONTEREY MAKE_BASE=TRUE	=	PN_VGL1_MONTEREY	79	90
75	PN_VGL2_MONTEREY MAKE_BASE=TRUE	=	PN_VGL2_MONTEREY	79	90
75	PP_AVDDP_MONTEREY MAKE_BASE=TRUE	=	PP_AVDDP_MONTEREY	79	
75	PN_AVDDN_MONTEREY MAKE_BASE=TRUE	=	PN_AVDDN_MONTEREY	79	
75	PP_VGH1_MONTEREY MAKE_BASE=TRUE	=	PP_VGH1_MONTEREY	79	
	NC_P1V05_SDG_SW MAKE_BASE=TRUE	=	NC_P1V05_SDG_SW	79	

B Signal Connections Alias

75	I2C_LARKSPURTOSDG_SDA MAKE_BASE=TRUE CKPLUS_WAIVE=I2C_PULLUP	=	I2C_LARKSPURTOSDG_SDA	79	
	I2C Pull-Up @ Larkspur				
75	I2C_LARKSPURTOSDG_SCL MAKE_BASE=TRUE CKPLUS_WAIVE=I2C_PULLUP	=	I2C_LARKSPURTOSDG_SCL	79	
	I2C Pull-Up @ Larkspur				
76	EDP_PANEL_1V8_EN MAKE_BASE=TRUE	=	EDP_PANEL_1V8_EN	79	
75	PM_VBLANK_LARKSPUR_SDG_L MAKE_BASE=TRUE	=	PM_VBLANK_LARKSPUR_SDG_L	79	
75	RESET_LARKSPUR_L MAKE_BASE=TRUE	=	RESET_LARKSPUR_L	79	
75	DCHG_SDGTOMONTEREY_L MAKE_BASE=TRUE	=	DCHG_SDGTOMONTEREY_L	79	
75	FAULT_SDGTOMONTEREY_L MAKE_BASE=TRUE	=	FAULT_SDGTOMONTEREY_L	79	
75	TEMP_COMP_MDB_SDG MAKE_BASE=TRUE	=	TEMP_COMP_MDB_SDG	79	

SYNC_DATE=09/10/2021

PAGE TITLE

PMU: SAN DIEGO SUPPORT

Apple Inc.

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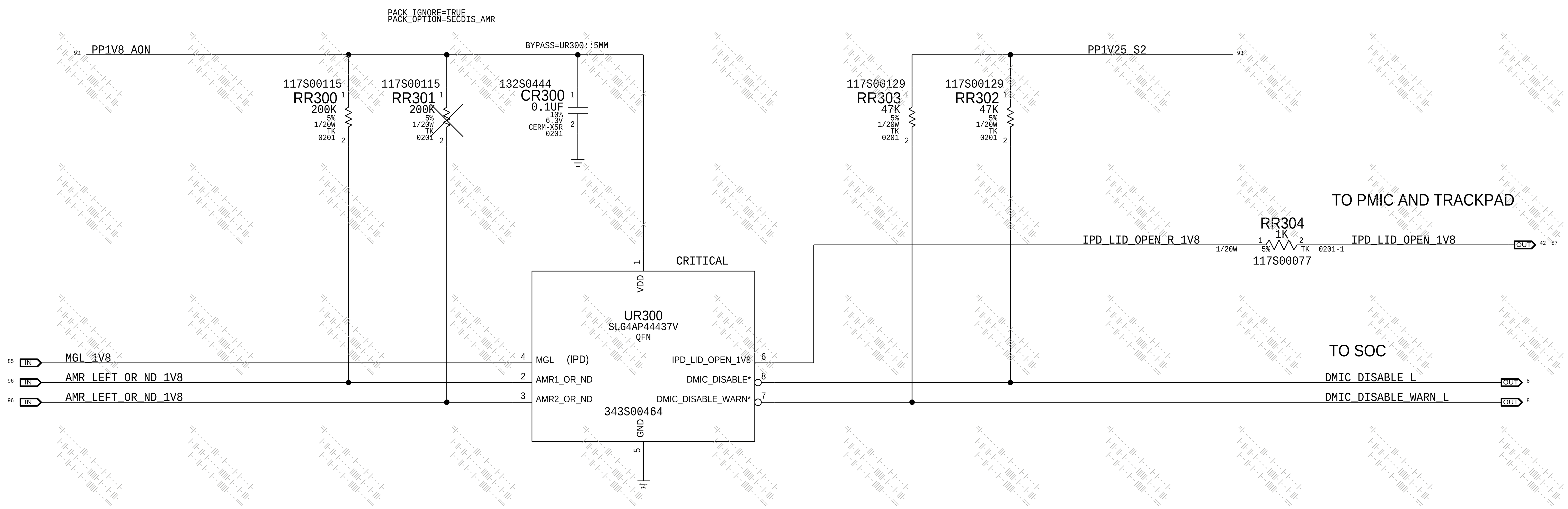
*** OK2INTEGRATE ***

LID SECDIS LOGIC



BOM_COST_GROUP=SOC

PAGE TITLE	SECDIS: SAK
DRAWING NUMBER	051-07020
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*** OK2INTEGRATE ***

AMP A

PP1V8_AWAKE
PP1V25_AWAKE_IO
PP3V8_AON — MAX CURRENT EDC = 1A (PER AMP)
PPBUS_AON_L_SPKRAMP — MAX CURRENT EDC = 4A (PER AMP)

SPKRAMP_A_DREG
CR600 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_A PLACE_NEAR=UR600.E5:5MM
CR601 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_A PLACE_NEAR=UR600.F3:5MM
CR602 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_A PLACE_NEAR=UR600.C2:5MM

CR603 0.1UF 10% 25V X5R 0201 — SPKRAMP_A PLACE_NEAR=UR600.C5:5MM
CR604 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_A PLACE_NEAR=UR600.C5:10MM
CR605 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_A PLACE_NEAR=UR600.C5:10MM
CR606 0.1UF 10% 25V X5R 0201 — SPKRAMP_A PLACE_NEAR=UR600.D5:5MM
CR607 10UF 20% 10V X5R-CERM 0402-7 — SPKRAMP_A PLACE_NEAR=UR600.D5:10MM

XWR600 SHORT-16L-0.1MM-SM * SEE NOTE — SPKRAMP_A

UR600 SN012776B0YBH DSBGA — SPKRAMP_A — TAWANG B0

SPKRAMP_A_VSENSEP * SEE NOTE
SPKRAMP_A_VSENSEN
SPKRAMP_A_PVDD_SNS

SPKRAMP_A BYPASS=UR600.B2:B3:10MM NO_XNET_CONNECTION=1

SPKRAMP_A_BOOTP — MIN_LINE_WIDTH=0.1000 — CR608 0.1UF 10% 25V X5R 0201
SPKRAMP_A_OUTP_R — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE
SPKRAMP_A_OUTN_R — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE
SPKRAMP_A_BOOTN — MIN_LINE_WIDTH=0.1000 — CR609 0.1UF 10% 25V X5R 0201

RR602 0 1% 1/3W 0603 — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE
RR603 0 1% 1/3W 0603 — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE

SPKRAMP_A_OUTP * SEE NOTE
SPKRAMP_A_OUTN * SEE NOTE

CR610 220PF 10% 25V X7R-CERM 201 NOSTUFF
CR611 220PF 10% 25V X7R-CERM 201 NOSTUFF

SPKRAMP_A_ADDR 0x70 — RR605 0 5% 1/20W TK 0201
SPKRAMP_B_ADDR 0x72 — RR635 470 5% 1/20W TK 0201
SPKRAMP_C_ADDR 0x74 — RR664 470 5% 1/20W TK 0201 — PACK_IGNORE=TRUE SPKRAMP_C

I2C_SPKRAMP_L_SCL
I2C_SPKRAMP_L_SDA
SPKRAMP_A_ADDR
TDM_SPKRAMP_L_BCLK
TDM_SPKRAMP_L_FSYNC
TDM_SPKRAMP_L_R2D
TDM_SPKRAMP_L_D2R
SPKRAMP_ABC_ICC
TP_SPKRAMP_A_LV_EN
SPKRAMP_INT_L
SPKRAMP_RESET_L

RR600 33 5% 1/20W TK 0201 — TDM_SPKRAMP_A_D2R_R — PLACE_NEAR=UR600.D1:10MM
RR601 33 5% 1/20W TK 0201 — SPKRAMP_A_ICC_R — PLACE_NEAR=UR600.F5:10MM

SBCLK E1 · FSYNC D2 · SDIN E2 · SDOUT D1 · ICC F5 · BYP_EN D3 · IRQ* E3 · SD* F4 · DREG C2

* SEE NOTE

AMP B

PP1V8_AWAKE
PP1V25_AWAKE_IO
PP3V8_AON
PPBUS_AON_L_SPKRAMP

SPKRAMP_B_DREG
CR630 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_B PLACE_NEAR=UR630.E5:5MM
CR631 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_B PLACE_NEAR=UR630.F3:5MM
CR632 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_B PLACE_NEAR=UR630.C2:5MM

CR633 0.1UF 10% 25V X5R 0201 — SPKRAMP_B PLACE_NEAR=UR630.C5:5MM
CR634 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_B PLACE_NEAR=UR630.C5:10MM
CR635 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_B PLACE_NEAR=UR630.C5:10MM
CR636 0.1UF 10% 25V X5R 0201 — SPKRAMP_B PLACE_NEAR=UR630.D5:5MM
CR637 10UF 20% 10V X5R-CERM 0402-7 — SPKRAMP_B PLACE_NEAR=UR630.D5:10MM

XWR601 SHORT-16L-0.1MM-SM * SEE NOTE — SPKRAMP_B

UR630 SN012776B0YBH DSBGA — SPKRAMP_B — TAWANG B0

SPKRAMP_B_VSENSEP * SEE NOTE
SPKRAMP_B_VSENSEN
SPKRAMP_B_PVDD_SNS

SPKRAMP_B BYPASS=UR630.B2:B3:10MM NO_XNET_CONNECTION=1

SPKRAMP_B_BOOTP — MIN_LINE_WIDTH=0.1000 — CR638 0.1UF 10% 25V X5R 0201
SPKRAMP_B_OUTP_R — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE
SPKRAMP_B_OUTN_R — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE
SPKRAMP_B_BOOTN — MIN_LINE_WIDTH=0.1000 — CR639 0.1UF 10% 25V X5R 0201

RR632 0 1% 1/3W 0603 — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE
RR633 0 1% 1/3W 0603 — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE

SPKRAMP_B_OUTP * SEE NOTE
SPKRAMP_B_OUTN * SEE NOTE

CR640 220PF 10% 25V X7R-CERM 201 NOSTUFF
CR641 220PF 10% 25V X7R-CERM 201 NOSTUFF

I2C_SPKRAMP_L_SCL
I2C_SPKRAMP_L_SDA
SPKRAMP_B_ADDR
TDM_SPKRAMP_L_BCLK
TDM_SPKRAMP_L_FSYNC
TDM_SPKRAMP_L_R2D
TDM_SPKRAMP_L_D2R
SPKRAMP_ABC_ICC
TP_SPKRAMP_B_LV_EN
SPKRAMP_INT_L
SPKRAMP_RESET_L

RR630 33 5% 1/20W TK 0201 — TDM_SPKRAMP_B_D2R_R — PLACE_NEAR=UR630.D1:10MM
RR631 33 5% 1/20W TK 0201 — SPKRAMP_B_ICC_R — PLACE_NEAR=UR630.F5:10MM

SBCLK E1 · FSYNC D2 · SDIN E2 · SDOUT D1 · ICC F5 · BYP_EN D3 · IRQ* E3 · SD* F4 · DREG C2

* SEE NOTE

THIS RESISTOR TIES ICC SIGNAL
BETWEEN AMPS A,B,C AND AMPS D,E,F:
0R --> GLOBAL ICC (ABCDEF)
DNE --> LOCAL ICC (ABC, DEF)

SPKRAMP_ICC_GB
RR693 0 0% 1/20W TK 0201
SPKRAMP_ABC_ICC ↔ SPKRAMP_DEF_ICC
SPKRAMP_ICC_GB

AMP C

=PP3V8_AON_C_SPKRAMP
=PPBUS_AON_C_SPKRAMP

SPKRAMP_C_DREG
CR660 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_C PLACE_NEAR=UR660.E5:5MM
CR661 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_C PLACE_NEAR=UR660.F3:5MM
CR662 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_C PLACE_NEAR=UR660.C2:5MM

CR663 0.1UF 10% 25V X5R 0201 — SPKRAMP_C PLACE_NEAR=UR660.C5:5MM
CR664 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_C PLACE_NEAR=UR660.C5:10MM
CR665 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_C PLACE_NEAR=UR660.C5:10MM
CR666 0.1UF 10% 25V X5R 0201 — SPKRAMP_C PLACE_NEAR=UR660.D5:5MM
CR667 10UF 20% 10V X5R-CERM 0402-7 — SPKRAMP_C PLACE_NEAR=UR660.D5:10MM

XWR602 SHORT-16L-0.1MM-SM * SEE NOTE — SPKRAMP_C

UR660 SN012776B0YBH DSBGA — SPKRAMP_C — TAWANG B0

SPKRAMP_C_VSENSEP * SEE NOTE
SPKRAMP_C_VSENSEN
SPKRAMP_C_PVDD_SNS

SPKRAMP_C BYPASS=UR660.B2:B3:10MM NO_XNET_CONNECTION=1

SPKRAMP_C_BOOTP — MIN_LINE_WIDTH=0.0990 — CR668 0.1UF 10% 25V X5R 0201
SPKRAMP_C_OUTP_R — MIN_LINE_WIDTH=0.0990 MIN_NECK_WIDTH=0.0990 SWITCH_NODE=TRUE
SPKRAMP_C_OUTN_R — MIN_LINE_WIDTH=0.0990 MIN_NECK_WIDTH=0.0990 SWITCH_NODE=TRUE
SPKRAMP_C_BOOTN — MIN_LINE_WIDTH=0.0990 — CR669 0.1UF 10% 25V X5R 0201

RR662 0 1% 1/3W 0603 — MIN_NECK_WIDTH=0.0990 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE
RR663 0 1% 1/3W 0603 — MIN_NECK_WIDTH=0.0990 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE

SPKRAMP_C_OUTP * SEE NOTE
SPKRAMP_C_OUTN * SEE NOTE

CR670 220PF 10% 25V X7R-CERM 201 NOSTUFF
CR671 220PF 10% 25V X7R-CERM 201 NOSTUFF

=I2C_SPKRAMP_C_SCL
=I2C_SPKRAMP_C_SDA
SPKRAMP_C_ADDR
TDM_SPKRAMP_L_BCLK
TDM_SPKRAMP_L_FSYNC
TDM_SPKRAMP_L_R2D
=TDM_SPKRAMP_C_D2R
SPKRAMP_ABC_ICC
TP_SPKRAMP_C_LV_EN
SPKRAMP_INT_L
SPKRAMP_RESET_L

RR660 33 5% 1/20W TK 0201 — TDM_SPKRAMP_C_D2R_R — PLACE_NEAR=UR660.D1:10MM
RR661 33 5% 1/20W TK 0201 — SPKRAMP_C_ICC_R — PLACE_NEAR=UR660.F5:10MM

SBCLK E1 · FSYNC D2 · SDIN E2 · SDOUT D1 · ICC F5 · BYP_EN D3 · IRQ* E3 · SD* F4 · DREG C2

* SEE NOTE

PP1V25_AWAKE_IO
NOSTUFF RR691 47K 5% 1/20W TK 0201
SPKRAMP_INT_L
SPKRAMP_RESET_L
RR692 47K 5% 1/20W TK 0201

NOTES:
- SEE TEST POINTS SIGNALS AND LOCATIONS ON REF DESIGN PAGE 1.
- VSENSEP/N SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
- PVDD_SNS XW SHOULD BE LOCATED BY MAIN PBUS SHAPE.
- THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
  - SPKRAMP_XX_OUTP/N_R
  - SPKRAMP_XX_OUTP/N
  - PVDD SUPPLY
- FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.
- BULK CAPACITORS SHOULD BE ADDED TO SPEAKER CONNECTOR PAGE.

BOM_COST_GROUP=AUDIO

SYNC_MASTER=Speaker1pp — SYNC_DATE=09/10/2021

PAGE TITLE: AUDIO AMPLIFIERS (1/2)

Apple Inc.

DRAWING NUMBER: 051-07020 — SIZE: D
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*** OK2INTEGRATE ***

AMP D

PP1V8_AWAKE
PP1V25_AWAKE_IO
PP3V8_AON
MAX CURRENT EDC = 1A (PER AMP)
PPBUS_AON_R_SPKRAMP
MAX CURRENT EDC = 4A (PER AMP)
SPKRAMP_D_DREG
SPKRAMP_D_PVDD_SNS
SPKRAMP_D_VSENSEP
SPKRAMP_D_VSENSEN
SPKRAMP_D_BOOTP
SPKRAMP_D_OUTP_R
SPKRAMP_D_OUTN_R
SPKRAMP_D_BOOTN
SPKRAMP_D_OUTP
SPKRAMP_D_OUTN
SPKRAMP_D_ADDR
SPKRAMP_D_BYPASS=UR700_B2:B3:10MM_NO_XNET_CONNECTION=1
SPKRAMP_D_BYPASS=UR700_A2:A5:10MM_NO_XNET_CONNECTION=1
CR700 1.0UF 20% 6.3V X5R 0201-1
CR701 1.0UF 20% 6.3V X5R 0201-1
CR702 1.0UF 20% 6.3V X5R 0201-1
CR703 0.1UF 10% 25V X5R 0201
CR704 10UF 20% 25V X5R-CERM 0603
CR705 10UF 20% 25V X5R-CERM 0603
CR706 0.1UF 10% 25V X5R 0201
CR707 10UF 20% 10V X5R-CERM 0402-7
XWR700 SHORT-16L-0.1MM-SM
UR700 SN012776B0YBH DSBGA
TAWANG B0
I2C_SPKRAMP_R_CODEC_SCL
I2C_SPKRAMP_R_CODEC_SDA
SPKRAMP_D_ADDR
TDM_SPKRAMP_R_BCLK
TDM_SPKRAMP_R_FSYNC
TDM_SPKRAMP_R_R2D
TDM_SPKRAMP_R_D2R
SPKRAMP_DEF_ICC_R
TP_SPKRAMP_D_LV_EN
SPKRAMP_INT_L
SPKRAMP_RESET_L
RR700 33 5% 1/20W TK 0201
RR701 33 5% 1/20W TK 0201
TDM_SPKRAMP_D_D2R_R
SPKRAMP_D_ICC_R
CR708 0.1UF 10% 25V X5R 0201
CR709 0.1UF 10% 25V X5R 0201
RR702 0 1% 1/16W 0603 1/5W
RR703 0 1% 1/16W 0603 1/5W
CR710 220PF 10% 25V X7R-CERM 201 NOSTUFF
CR711 220PF 10% 25V X7R-CERM 201 NOSTUFF
RR705 2.2K 5% 1/20W TK 0201
RR734 2.2K 5% 1/20W TK 0201
RR765 10K 1% 1/20W MF 201
RR706 0 0% 1/20W TK 0201
RR707 0 0% 1/20W TK 0201 NOSTUFF
SPKRAMP_DEF_ICC
SPKRAMP_DEF_ICC_R

RR706 TO REDUCE STUB LENGTH FOR LOCAL ICC OPERATION. RR707 PROVIDES THE OPTION TO GND FLOATING SPKRAMP_DEF_ICC TRACE

AMP E

PP1V8_AWAKE
PP1V25_AWAKE_IO
PP3V8_AON
PPBUS_AON_R_SPKRAMP
SPKRAMP_E_DREG
SPKRAMP_E_PVDD_SNS
SPKRAMP_E_VSENSEP
SPKRAMP_E_VSENSEN
SPKRAMP_E_BOOTP
SPKRAMP_E_OUTP_R
SPKRAMP_E_OUTN_R
SPKRAMP_E_BOOTN
SPKRAMP_E_OUTP
SPKRAMP_E_OUTN
SPKRAMP_E_ADDR
SPKRAMP_E_BYPASS=UR730_B2:B3:10MM_NO_XNET_CONNECTION=1
SPKRAMP_E_BYPASS=UR730_A2:A5:10MM_NO_XNET_CONNECTION=1
CR730 1.0UF 20% 6.3V X5R 0201-1
CR731 1.0UF 20% 6.3V X5R 0201-1
CR732 1.0UF 20% 6.3V X5R 0201-1
CR733 0.1UF 10% 25V X5R 0201
CR734 10UF 20% 25V X5R-CERM 0603
CR735 10UF 20% 25V X5R-CERM 0603
CR736 0.1UF 10% 25V X5R 0201
CR737 10UF 20% 10V X5R-CERM 0402-7
XWR701 SHORT-16L-0.1MM-SM
UR730 SN012776B0YBH DSBGA
TAWANG B0
I2C_SPKRAMP_R_CODEC_SCL
I2C_SPKRAMP_R_CODEC_SDA
SPKRAMP_E_ADDR
TDM_SPKRAMP_R_BCLK
TDM_SPKRAMP_R_FSYNC
TDM_SPKRAMP_R_R2D
TDM_SPKRAMP_R_D2R
SPKRAMP_DEF_ICC_R
TP_SPKRAMP_E_LV_EN
SPKRAMP_INT_L
SPKRAMP_RESET_L
RR730 33 5% 1/20W TK 0201
RR731 33 5% 1/20W TK 0201
TDM_SPKRAMP_E_D2R_R
SPKRAMP_E_ICC_R
CR738 0.1UF 10% 25V X5R 0201
CR739 0.1UF 10% 25V X5R 0201
RR732 0 1% 1/16W 0603 1/5W
RR733 0 1% 1/16W 0603 1/5W
CR740 220PF 10% 25V X7R-CERM 201 NOSTUFF
CR741 220PF 10% 25V X7R-CERM 201 NOSTUFF

AMP F

PP1V8_AWAKE
PP1V25_AWAKE_IO
=PP3V8_AON_F_SPKRAMP
=PPBUS_AON_F_SPKRAMP
SPKRAMP_F_DREG
SPKRAMP_F_PVDD_SNS
SPKRAMP_F_VSENSEP
SPKRAMP_F_VSENSEN
SPKRAMP_F_BOOTP
SPKRAMP_F_OUTP_R
SPKRAMP_F_OUTN_R
SPKRAMP_F_BOOTN
SPKRAMP_F_OUTP
SPKRAMP_F_OUTN
SPKRAMP_F_ADDR
SPKRAMP_F_BYPASS=UR760_B2:B3:10MM_NO_XNET_CONNECTION=1
SPKRAMP_F_BYPASS=UR760_A2:A5:10MM_NO_XNET_CONNECTION=1
CR760 1.0UF 20% 6.3V X5R 0201-1
CR761 1.0UF 20% 6.3V X5R 0201-1
CR762 1.0UF 20% 6.3V X5R 0201-1
CR763 0.1UF 10% 25V X5R 0201
CR764 10UF 20% 25V X5R-CERM 0603
CR765 10UF 20% 25V X5R-CERM 0603
CR766 0.1UF 10% 25V X5R 0201
CR767 10UF 20% 10V X5R-CERM 0402-7
XWR702 SHORT-16L-0.1MM-SM
UR760 SN012776B0YBH DSBGA
TAWANG B0
=I2C_SPKRAMP_F_SCL
=I2C_SPKRAMP_F_SDA
SPKRAMP_F_ADDR
TDM_SPKRAMP_R_BCLK
TDM_SPKRAMP_R_FSYNC
TDM_SPKRAMP_R_R2D
=TDM_SPKRAMP_F_D2R
SPKRAMP_DEF_ICC_R
TP_SPKRAMP_F_LV_EN
SPKRAMP_INT_L
SPKRAMP_RESET_L
RR760 33 5% 1/20W TK 0201
RR761 33 5% 1/20W TK 0201
TDM_SPKRAMP_F_D2R_R
SPKRAMP_F_ICC_R
CR768 0.1UF 10% 25V X5R 0201
CR769 0.1UF 10% 25V X5R 0201
RR762 0 1% 1/16W 0603 1/5W
RR763 0 1% 1/16W 0603 1/5W
CR770 220PF 10% 25V X7R-CERM 201 NOSTUFF
CR771 220PF 10% 25V X7R-CERM 201 NOSTUFF

BOM_COST_GROUP=AUDIO

NOTES:
- SEE TEST POINTS SIGNALS AND LOCATIONS ON REF DESIGN PAGE 1.
- VSENSEP/N SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
- PVDD_SNS XW SHOULD BE LOCATED BY MAIN PBUS SHAPE.
- THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
  - SPKRAMP_XX_OUTP/N_R
  - SPKRAMP_XX_OUTP/N
  - PVDD SUPPLY
- FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.
- BULK CAPACITORS SHOULD BE ADDED TO SPEAKER CONNECTOR PAGE.

SYNC_MASTER=SpeakerMemp
SYNC_DATE=09/10/2021
PAGE TITLE: AUDIO AMPLIFIERS (2/2)
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SIZE: D
REVISION: 6.0.0
BRANCH: evt-1
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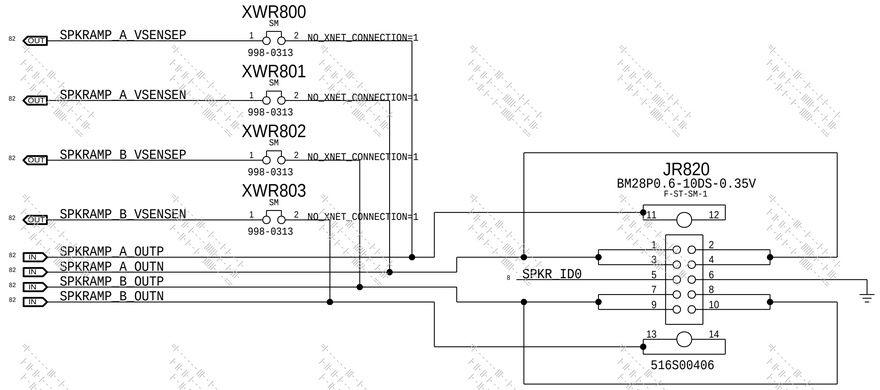
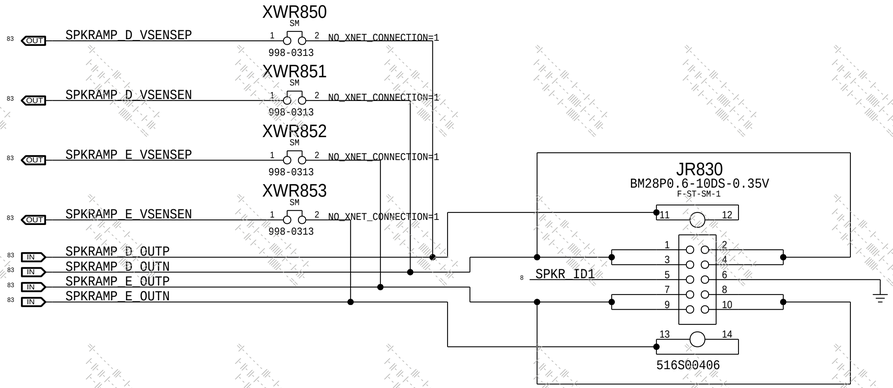
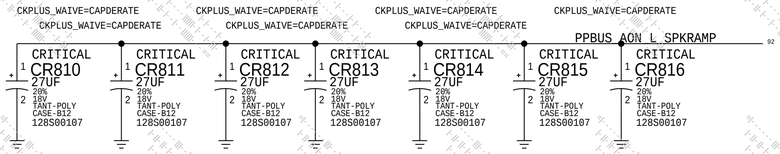
A LEFT SPEAKER CONNECTOR



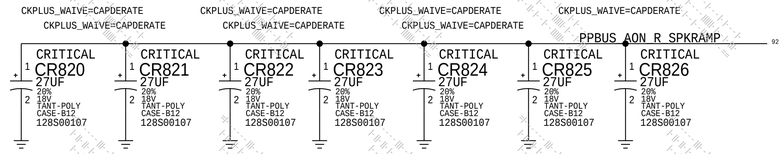
B RIGHT SPEAKER CONNECTOR



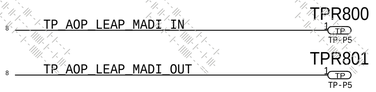
C LEFT SPEAKER AMP BULK CAP



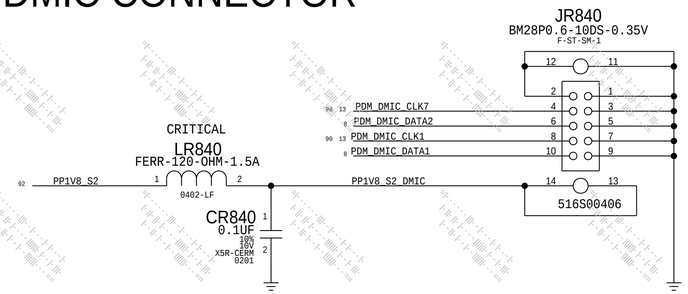
D RIGHT SPEAKER AMP BULK CAP



E MADI TEST POINT



F DMIC CONNECTOR



BOM_COST_GROUP=AUDIO

DESIGN: T651/MLB
LAST CHANGE: Fri Oct 11 18:06:02 2019

PAGE TITLE
Audio Connectors

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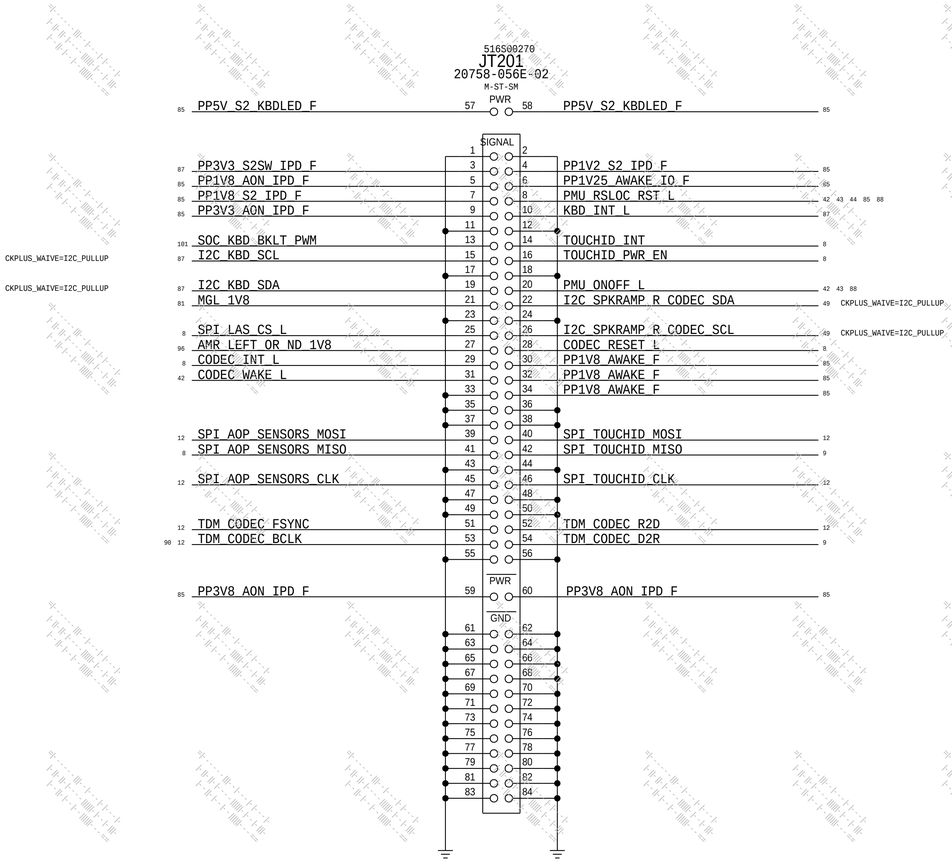
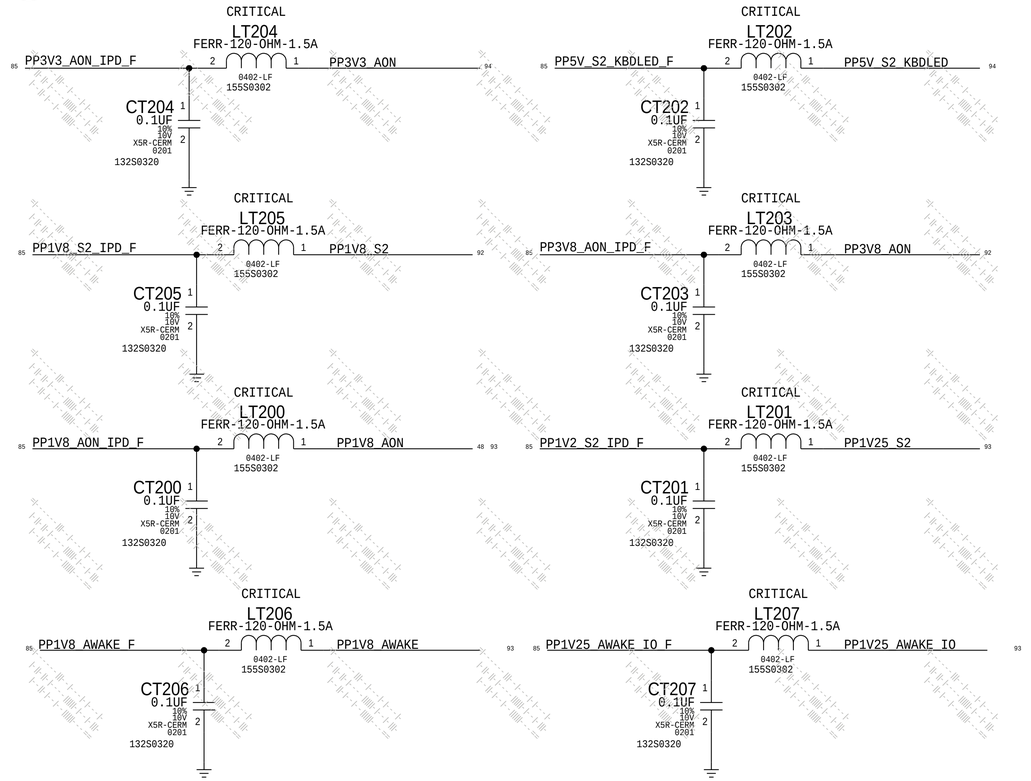
A KBD B2B CONNECTOR

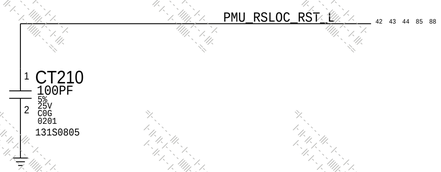


KBD Flex Receptacle APN 516S00457

B KBD PWR FILTER



C Keyboard Control



BOM_COST_GROUP=KEYBOARD

SYNC_MASTER	SYNC_DATE=05/10/2021
PAGE TITLE	Keyboard Connector
Apple Inc.	DRAWING NUMBER 051-07020 SIZE D
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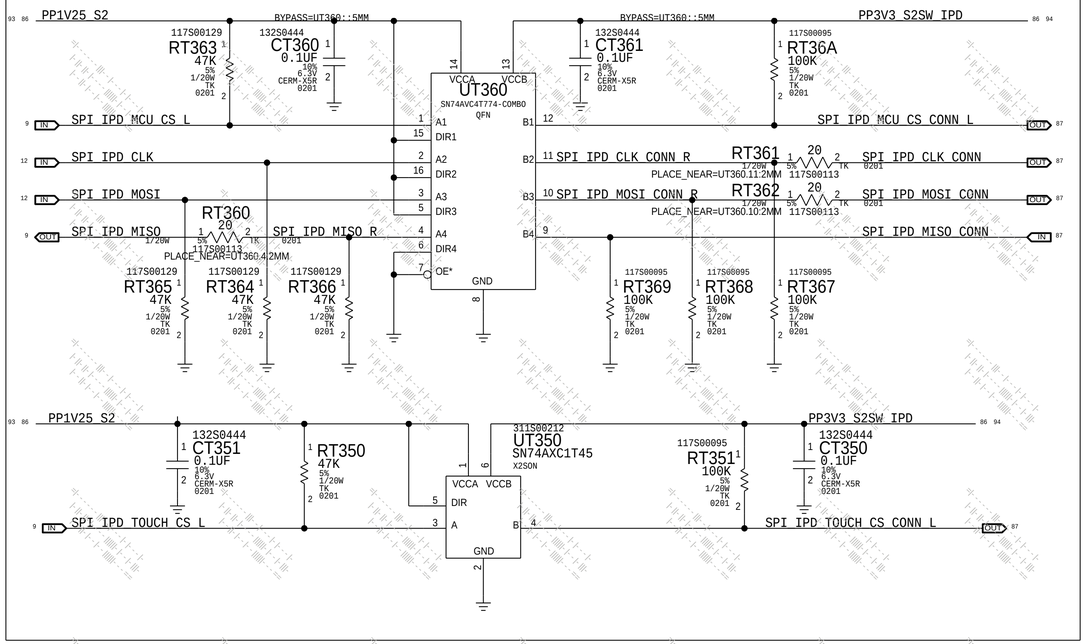
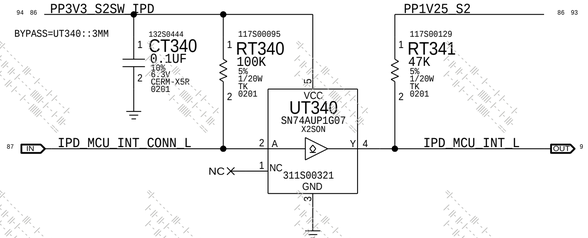
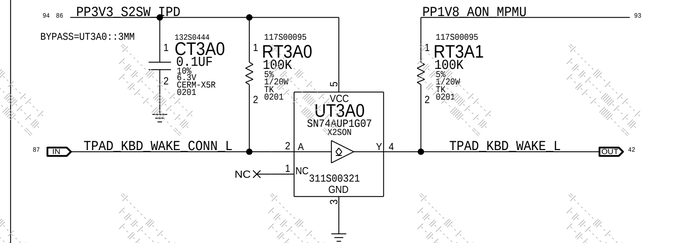
A Trackpad SPI Bus Level Shifter



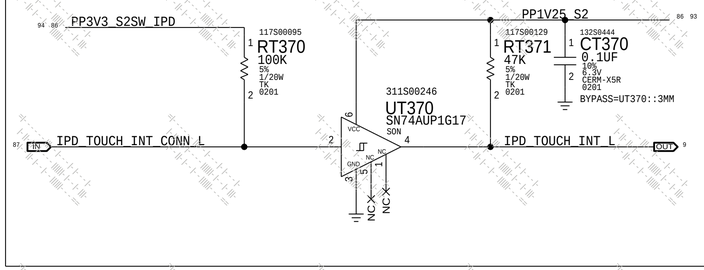
B Trackpad MCU_INT_L LS



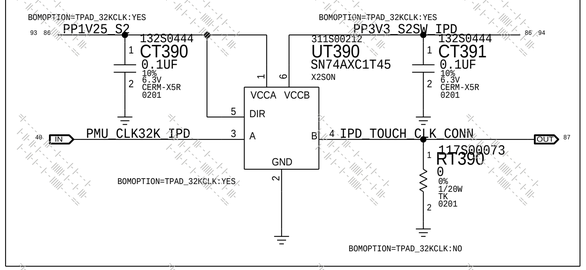
C Trackpad WAKE_L LS



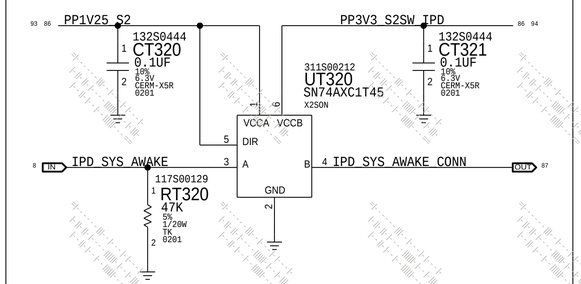
D Trackpad TOUCH_INT_L LS



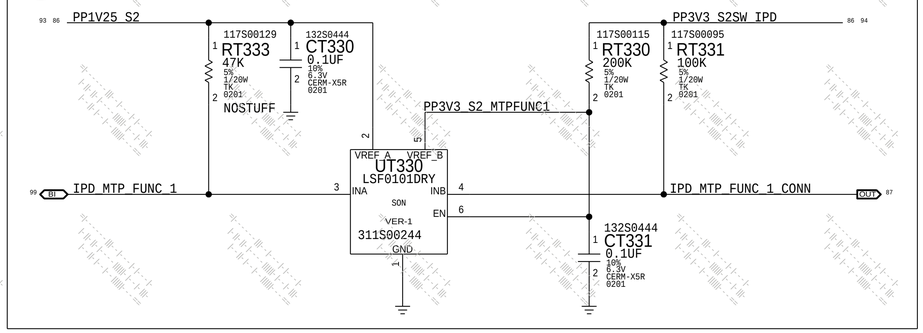
E Trackpad 32kHz Clock LS



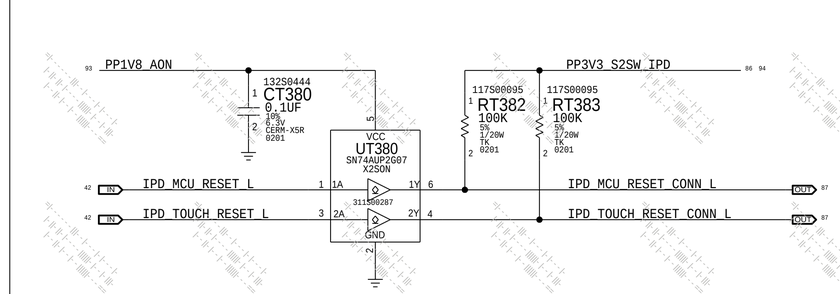
F Trackpad SYS_AWAKE LS



G Trackpad MTP_FUNC1 LS

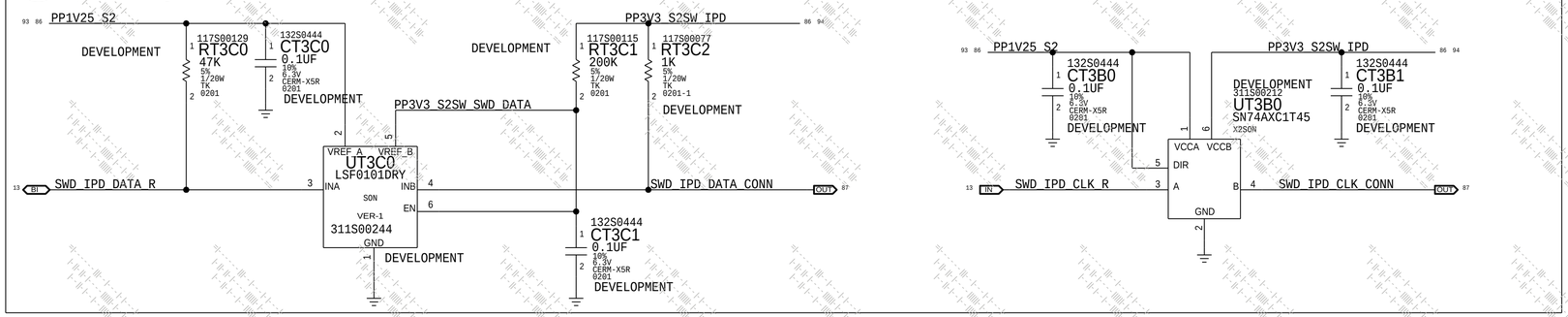


H Trackpad RESET Level Shifter



See Trackpad IPD design for RESET Pull-Up Info.

I Trackpad SWD Level Shifter



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SYNC_MASTER=	SYNC_DATE=09/10/2021
PAGE TITLE	Trackpad Support
Apple Inc.	DRAWING NUMBER 051-07020 · SIZE D
	REVISION 6.0.0
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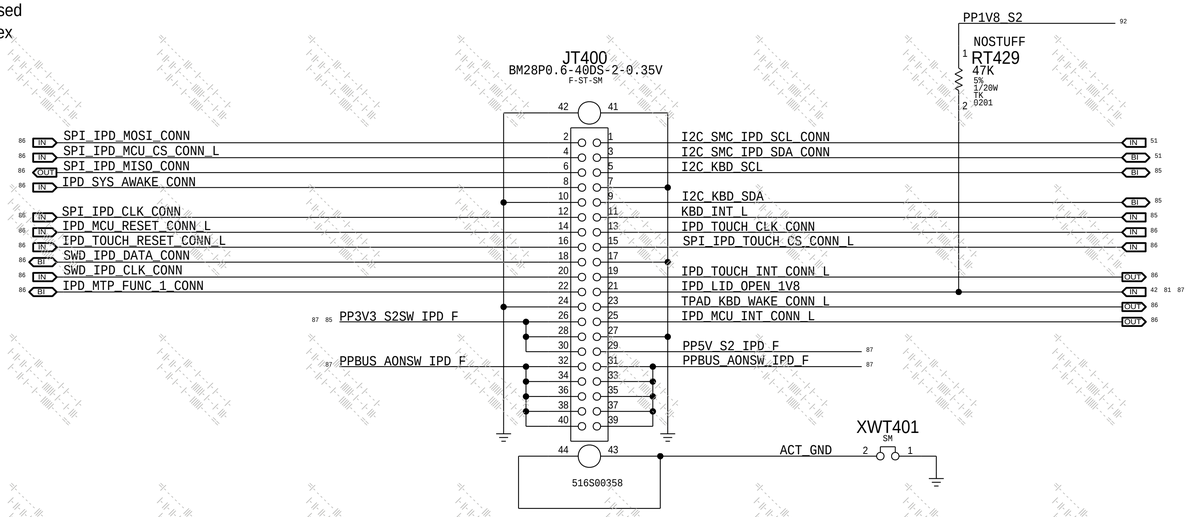
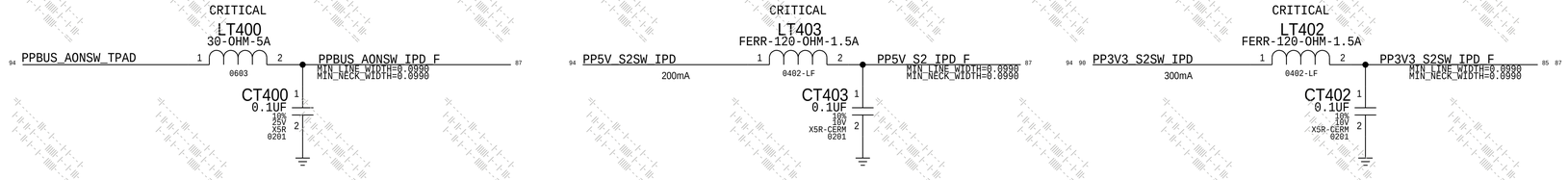
A Trackpad Connector

Bottom side contacts used
Pinout reversed from flex



C Trackpad Control

B Trackpad Power Supply Filters



BOM_COST_GROUP=TRACKPAD

SYNC_MASTER=
SYNC_DATE=09/10/2021

PAGE TITLE: Trackpad Connector

Apple Inc.

DRAWING NUMBER: 051-07020
SIZE: D
REVISION: 6.0.0
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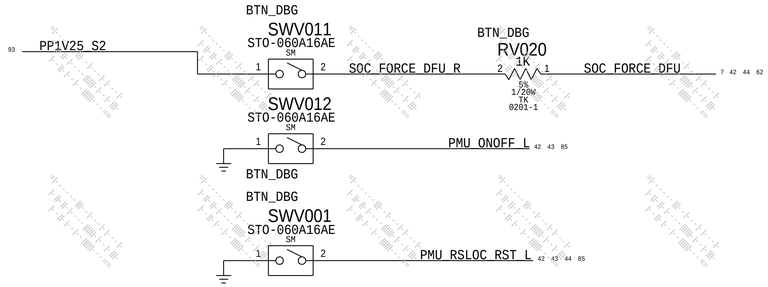
A Debug Push-Buttons



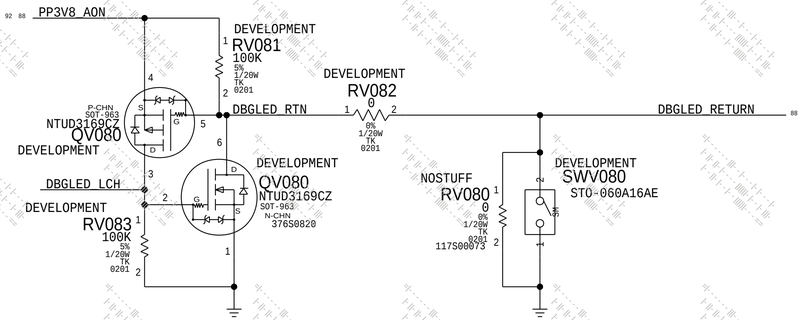
B Debug LED Control

Debug LED Latch

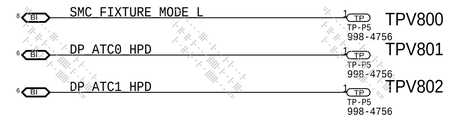
Press button once to engage.

Remove power to disengage.

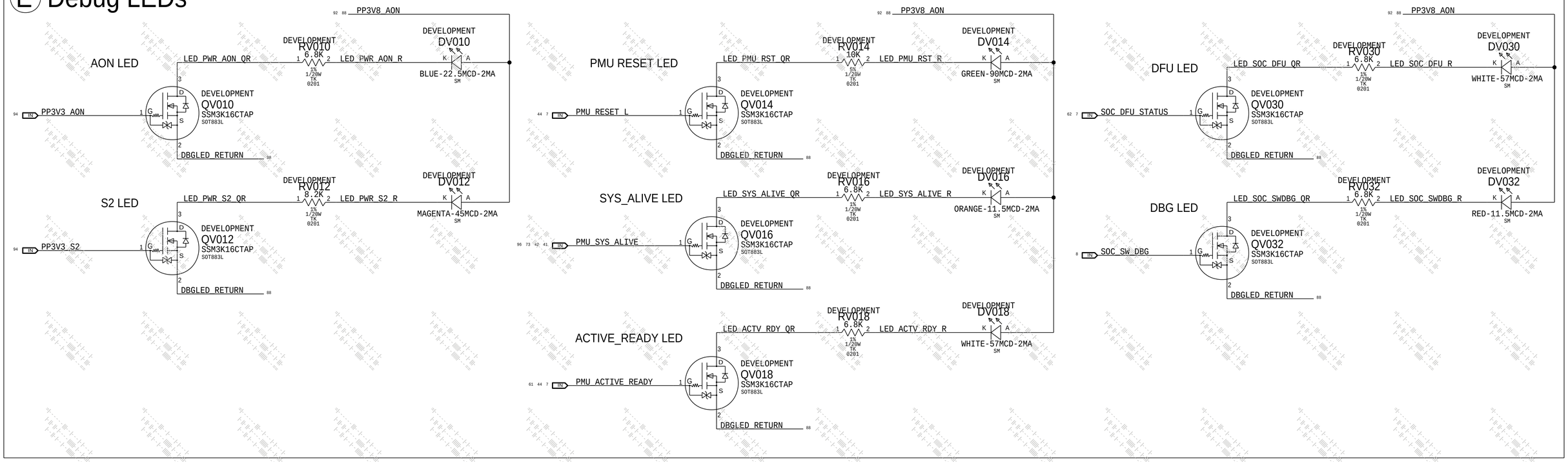
Debug LED Enable



D Debug Test Points



E Debug LEDs



BOM_COST_GROUP=DEBUG

SYNC_MASTER=jawe68 SYNC_DATE=09/28/2021

PAGE TITLE: DEBUG

Apple Inc.

DRAWING NUMBER: 051-07020 SIZE: D

REVISION: 6.0.0

BRANCH: evt-1

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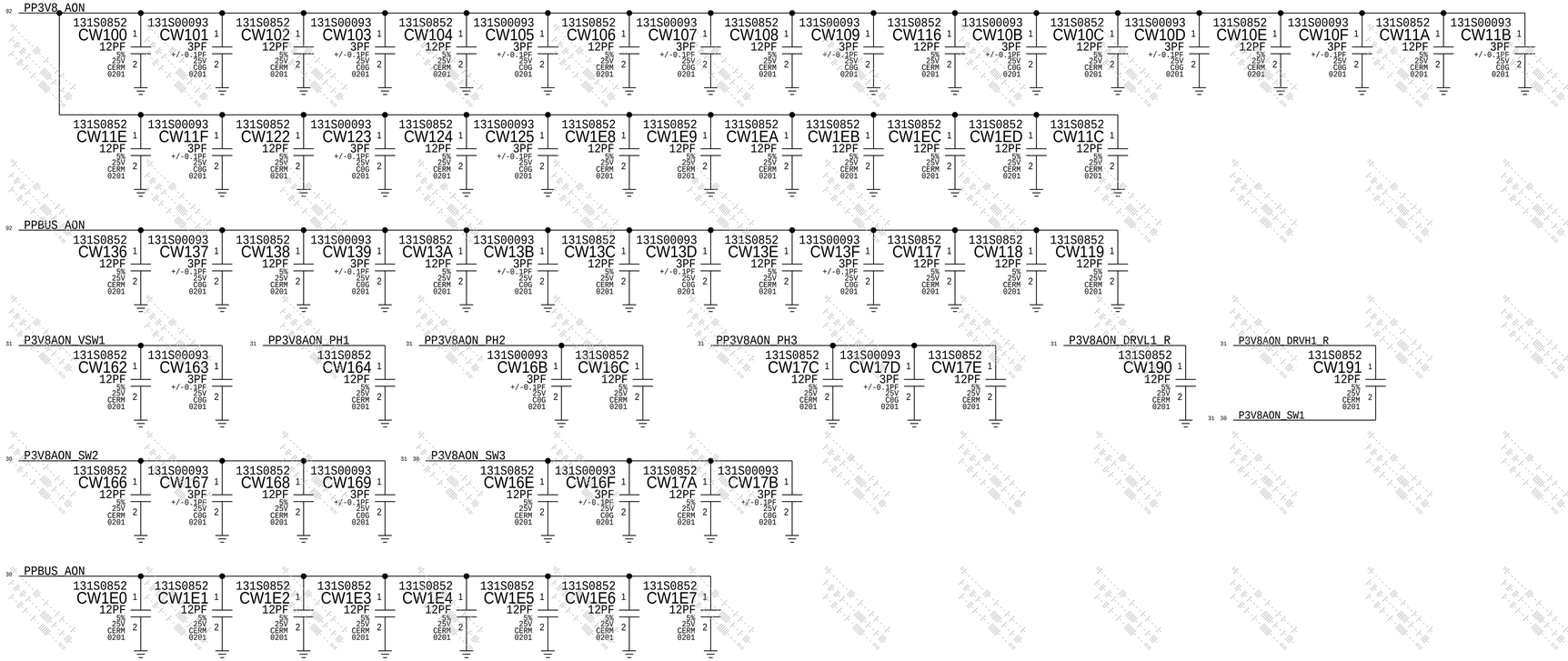
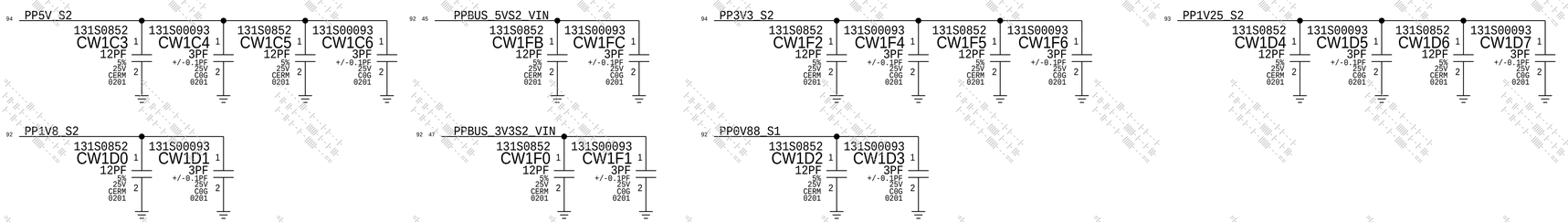
A ICEMAN Desense



B BUCK POWER Desense



BOM_COST_GROUP=DESENSE

09/10/2021

PAGE TITLE: Desense 1

Apple Inc.

DRAWING NUMBER: 051-07020 | SIZE: D

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A Display PMIC Desense

94 PP3V3_SW_LCD
131S0852 CW200 1 12PF 5% 25V CERM 0201 2
131S00093 CW201 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW202 1 12PF 5% 25V CERM 0201 2
131S00093 CW203 1 3PF +/-0.1PF 25V C0G 0201 2

79 PAVDDP_SDG_SW
131S0852 CW218 1 12PF 5% 25V CERM 0201 2 NOSTUFF

79 PAVDDN_SDG_SW
131S0852 CW219 1 12PF 5% 25V CERM 0201 2 NOSTUFF

80 79 PP1V8_DISP
131S0852 CW206 1 12PF 5% 25V CERM 0201 2
131S00093 CW207 1 3PF +/-0.1PF 25V C0G 0201 2

80 79 PN_VGL2_MONTEREY
131S0852 CW208 1 12PF 5% 25V CERM 0201 2
131S00093 CW209 1 3PF +/-0.1PF 25V C0G 0201 2

80 79 PN_VGL1_MONTEREY
131S0852 CW210 1 12PF 5% 25V CERM 0201 2
131S00093 CW211 1 3PF +/-0.1PF 25V C0G 0201 2

79 PVGH_BOOST_SDG_SW
131S0852 CW21A 1 12PF 5% 25V CERM 0201 2 NOSTUFF

79 P1V8_SDG_SW
131S0852 CW21B 1 12PF 5% 25V CERM 0201 2 NOSTUFF

79 PVGH_BOOST_SDG
131S0852 CW212 1 12PF 5% 25V CERM 0201 2
131S00093 CW213 1 3PF +/-0.1PF 25V C0G 0201 2

79 PAVDDN_SDG_R
131S0852 CW214 1 12PF 5% 25V CERM 0201 2
131S00093 CW215 1 3PF +/-0.1PF 25V C0G 0201 2

79 PAVDDP_SDG_R
131S0852 CW216 1 12PF 5% 25V CERM 0201 2
131S00093 CW217 1 3PF +/-0.1PF 25V C0G 0201 2

B Audio Desense

92 PPBUS_AON_L_SPKRAMP
131S0852 CW220 1 12PF 5% 25V CERM 0201 2
131S00093 CW221 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW222 1 12PF 5% 25V CERM 0201 2
131S00093 CW223 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW224 1 12PF 5% 25V CERM 0201 2
131S00093 CW225 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW226 1 12PF 5% 25V CERM 0201 2
131S00093 CW227 1 3PF +/-0.1PF 25V C0G 0201 2

84 13 PDM_DMIC_CLK1
131S0852 CW228 1 12PF 5% 25V CERM 0201 2

84 13 PDM_DMIC_CLK7
131S0852 CW229 1 12PF 5% 25V CERM 0201 2

92 PPBUS_AON_R_SPKRAMP
131S0852 CW230 1 12PF 5% 25V CERM 0201 2
131S00093 CW231 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW232 1 12PF 5% 25V CERM 0201 2
131S00093 CW233 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW234 1 12PF 5% 25V CERM 0201 2
131S00093 CW235 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW236 1 12PF 5% 25V CERM 0201 2
131S00093 CW237 1 3PF +/-0.1PF 25V C0G 0201 2

13 8 PDM_DMIC_CLK1_R
131S0852 CW238 1 12PF 5% 25V CERM 0201 2

13 8 PDM_DMIC_CLK7_R
131S0852 CW239 1 12PF 5% 25V CERM 0201 2

85 12 TDM_CODEC_BCLK
131S0852 CW23A 1 12PF 5% 25V CERM 0201 2

C Display and Keyboard Backlight Desense

94 75 PPVOUT_LCDBKLT
131S00141 CW240 1 12PF 5% 100V C0G 0201 2
131S00140 CW241 1 3PF +/-0.1PF 100V C0G 0201 2
131S00141 CW242 1 12PF 5% 100V C0G 0201 2
131S00140 CW243 1 3PF +/-0.1PF 100V C0G 0201 2

94 PP5V_S2_KBDLED
131S0852 CW254 1 12PF 5% 25V CERM 0201 2
131S00093 CW255 1 3PF +/-0.1PF 25V C0G 0201 2

77 PPVOUT_LCDBKLT_SW
131S00141 CW244 1 12PF 5% 100V C0G 0201 2 NOSTUFF
131S00140 CW245 1 3PF +/-0.1PF 100V C0G 0201 2 NOSTUFF

77 PPVIN_LCDBKLT_Q
131S00141 CW246 1 12PF 5% 100V C0G 0201 2
131S00140 CW247 1 3PF +/-0.1PF 100V C0G 0201 2
131S00141 CW248 1 12PF 5% 100V C0G 0201 2
131S00140 CW249 1 3PF +/-0.1PF 100V C0G 0201 2
131S00141 CW24A 1 12PF 5% 100V C0G 0201 2
131S00140 CW24B 1 3PF +/-0.1PF 100V C0G 0201 2
131S00141 CW24C 1 12PF 5% 100V C0G 0201 2
131S00140 CW24D 1 3PF +/-0.1PF 100V C0G 0201 2

94 PPVOUT_LCDBKLT_D
131S00141 CW24E 1 12PF 5% 100V C0G 0201 2
131S00140 CW24F 1 3PF +/-0.1PF 100V C0G 0201 2
131S00141 CW250 1 12PF 5% 100V C0G 0201 2
131S00140 CW251 1 3PF +/-0.1PF 100V C0G 0201 2
131S00141 CW252 1 12PF 5% 100V C0G 0201 2
131S00140 CW253 1 3PF +/-0.1PF 100V C0G 0201 2

D NAND Desense

92 PP2V58_AWAKE_NAND_VCC
131S0852 CW270 1 12PF 5% 25V CERM 0201 2
131S00093 CW271 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW272 1 12PF 5% 25V CERM 0201 2
131S00093 CW273 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW274 1 12PF 5% 25V CERM 0201 2
131S00093 CW275 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW276 1 12PF 5% 25V CERM 0201 2
131S00093 CW277 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW278 1 12PF 5% 25V CERM 0201 2
131S00093 CW279 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW27A 1 12PF 5% 25V CERM 0201 2
131S00093 CW27B 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW27C 1 12PF 5% 25V CERM 0201 2
131S00093 CW27D 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW27E 1 12PF 5% 25V CERM 0201 2
131S00093 CW27F 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW280 1 12PF 5% 25V CERM 0201 2
131S00093 CW281 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW282 1 12PF 5% 25V CERM 0201 2
131S00093 CW283 1 3PF +/-0.1PF 25V C0G 0201 2

93 PP1V25_AWAKE_NAND_VCCQ
131S0852 CW284 1 12PF 5% 25V CERM 0201 2
131S00093 CW285 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW286 1 12PF 5% 25V CERM 0201 2
131S00093 CW287 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW288 1 12PF 5% 25V CERM 0201 2
131S00093 CW289 1 3PF +/-0.1PF 25V C0G 0201 2

93 PP0V88_AWAKE_NAND_VDD
131S0852 CW28A 1 12PF 5% 25V CERM 0201 2
131S00093 CW28B 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW28C 1 12PF 5% 25V CERM 0201 2
131S00093 CW28D 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW28E 1 12PF 5% 25V CERM 0201 2
131S00093 CW28F 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW290 1 12PF 5% 25V CERM 0201 2
131S00093 CW291 1 3PF +/-0.1PF 25V C0G 0201 2

E Camera Desense

74 PP5V_S2_CAMERA_FILT
131S0852 CW2A0 1 12PF 5% 25V CERM 0201 2

F Trackpad Desense

94 87 PP3V3_S2SW_IPD
131S0852 CW2B0 1 12PF 5% 25V CERM 0201 2 PLACE_NEAR=LT402.1:5MM
131S00093 CW2B1 1 3PF +/-0.1PF 25V C0G 0201 2 PLACE_NEAR=LT402.1:5MM

G Display TCON Desense

75 12 SPI_TCON_CLK
131S0852 CW2C0 1 12PF 5% 25V CERM 0201 2

75 9 SPI_TCON_MISO
131S0852 CW2C1 1 12PF 5% 25V CERM 0201 2

75 12 SPI_TCON_MOSI
131S0852 CW2C2 1 12PF 5% 25V CERM 0201 2

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A SOC Desense

92 91 PPVDD_AWAKE_PCPU
131S0852 CW300 1 12PF 5% 25V CERM 0201 2
131S00093 CW301 1 3PF +/-0.1PF 25V C0G 0201 2

92 91 PPVDD_AWAKE_PCPU
131S0852 CW302 1 12PF 5% 25V CERM 0201 2
131S00093 CW303 1 3PF +/-0.1PF 25V C0G 0201 2

92 91 PPVDD_AWAKE_CPU_SRAM
131S0852 CW304 1 12PF 5% 25V CERM 0201 2
131S00093 CW305 1 3PF +/-0.1PF 25V C0G 0201 2

92 91 PPVDD_AWAKE_CPU_SRAM
131S0852 CW306 1 12PF 5% 25V CERM 0201 2
131S00093 CW307 1 3PF +/-0.1PF 25V C0G 0201 2

92 91 PPVDD_S1_SOC
131S0852 CW308 1 12PF 5% 25V CERM 0201 2
131S00093 CW309 1 3PF +/-0.1PF 25V C0G 0201 2

92 91 PPVDD_S1_SOC
131S0852 CW310 1 12PF 5% 25V CERM 0201 2
131S00093 CW311 1 3PF +/-0.1PF 25V C0G 0201 2

92 91 PPVDD_S1_DCS
131S0852 CW312 1 12PF 5% 25V CERM 0201 2
131S00093 CW313 1 3PF +/-0.1PF 25V C0G 0201 2

92 91 PPVDD_S1_DCS
131S0852 CW314 1 12PF 5% 25V CERM 0201 2
131S00093 CW315 1 3PF +/-0.1PF 25V C0G 0201 2

92 91 PP0V779_S1_SRAM
131S0852 CW316 1 12PF 5% 25V CERM 0201 2
131S00093 CW317 1 3PF +/-0.1PF 25V C0G 0201 2

92 91 PP0V779_S1_SRAM
131S0852 CW318 1 12PF 5% 25V CERM 0201 2
131S00093 CW319 1 3PF +/-0.1PF 25V C0G 0201 2

92 91 PPVDD_S1_DISP
131S0852 CW320 1 12PF 5% 25V CERM 0201 2
131S00093 CW321 1 3PF +/-0.1PF 25V C0G 0201 2

92 91 PPVDD_S1_DISP
131S0852 CW322 1 12PF 5% 25V CERM 0201 2
131S00093 CW323 1 3PF +/-0.1PF 25V C0G 0201 2

92 91 PPVDD_AWAKE_GPU
131S0852 CW324 1 12PF 5% 25V CERM 0201 2
131S00093 CW325 1 3PF +/-0.1PF 25V C0G 0201 2

92 91 PPVDD_AWAKE_GPU
131S0852 CW326 1 12PF 5% 25V CERM 0201 2
131S00093 CW327 1 3PF +/-0.1PF 25V C0G 0201 2

92 91 PP1V05_S2SW_VDD2H
131S0852 CW328 1 12PF 5% 25V CERM 0201 2
131S00093 CW329 1 3PF +/-0.1PF 25V C0G 0201 2

92 91 PP1V05_S2SW_VDD2H
131S0852 CW330 1 12PF 5% 25V CERM 0201 2
131S00093 CW331 1 3PF +/-0.1PF 25V C0G 0201 2

93 91 PP1V12_S2SW_AMPH
131S0852 CW332 1 12PF 5% 25V CERM 0201 2
131S00093 CW333 1 3PF +/-0.1PF 25V C0G 0201 2

93 91 PP1V12_S2SW_AMPH
131S0852 CW334 1 12PF 5% 25V CERM 0201 2
131S00093 CW335 1 3PF +/-0.1PF 25V C0G 0201 2

92 91 PPVDD_AWAKE_ECPU
131S0852 CW336 1 12PF 5% 25V CERM 0201 2
131S00093 CW337 1 3PF +/-0.1PF 25V C0G 0201 2

92 91 PPVDD_AWAKE_ECPU
131S0852 CW338 1 12PF 5% 25V CERM 0201 2
131S00093 CW339 1 3PF +/-0.1PF 25V C0G 0201 2

93 PP1V2_AWAKE_PLL
131S0852 CW33A 1 12PF 5% 25V CERM 0201 2
131S00093 CW33B 1 3PF +/-0.1PF 25V C0G 0201 2

93 PP0V72_S2_VDD_LOW
131S0852 CW33C 1 12PF 5% 25V CERM 0201 2
131S00093 CW33D 1 3PF +/-0.1PF 25V C0G 0201 2

94 PP0V78_S1_VDD_FIXED
131S0852 CW33E 1 12PF 5% 25V CERM 0201 2
131S00093 CW33F 1 3PF +/-0.1PF 25V C0G 0201 2

92 91 PP1V05_S2SW_VDD2H
131S0852 CW35B 1 12PF 5% 25V CERM 0201 2
131S00093 CW35C 1 3PF +/-0.1PF 25V C0G 0201 2

94 PP1V2_S2_CIO
131S0852 CW340 1 12PF 5% 25V CERM 0201 2
131S00093 CW341 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW342 1 12PF 5% 25V CERM 0201 2
131S00093 CW343 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW344 1 12PF 5% 25V CERM 0201 2
131S00093 CW345 1 3PF +/-0.1PF 25V C0G 0201 2

92 91 PPVDD_AWAKE_GPU
131S00093 CW35D 1 3PF +/-0.1PF 25V C0G 0201 2

94 PP1V8_S2SW
131S0852 CW346 1 12PF 5% 25V CERM 0201 2
131S00093 CW347 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW348 1 12PF 5% 25V CERM 0201 2
131S0852 CW349 1 12PF 5% 25V CERM 0201 2
131S00093 CW34A 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW34B 1 12PF 5% 25V CERM 0201 2
131S00093 CW34C 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW34D 1 12PF 5% 25V CERM 0201 2
131S00093 CW34E 1 3PF +/-0.1PF 25V C0G 0201 2

92 PP0V5_S1_VDDQL
131S0852 CW34F 1 12PF 5% 25V CERM 0201 2
131S00093 CW350 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW351 1 12PF 5% 25V CERM 0201 2
131S00093 CW352 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW353 1 12PF 5% 25V CERM 0201 2
131S00093 CW354 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW355 1 12PF 5% 25V CERM 0201 2
131S00093 CW356 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW357 1 12PF 5% 25V CERM 0201 2
131S00093 CW358 1 3PF +/-0.1PF 25V C0G 0201 2
131S0852 CW359 1 12PF 5% 25V CERM 0201 2
131S00093 CW35A 1 3PF +/-0.1PF 25V C0G 0201 2

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USBC DCIN

61 PPDCIN_AON_CHGR
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ PPDCIN_AON_CHGR 25 29
→ PPDCIN_AON_CHGR 52

PBUS

25 PPBUS_AON
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.0970
→ PPBUS_AON 54
→ PPBUS_AON 54
→ PPBUS_AON 78
→ PPBUS_AON 48
→ PPBUS_AON 48
→ PPBUS_AON 52
→ PPBUS_AON 53
→ PPBUS_AON 30 31 89
→ PPBUS_AON 52
→ PPBUS_AON 89

52 PPBUS_5VS2_VIN
MIN_LINE_WIDTH=0.0970
MIN_NECK_WIDTH=0.1000
MAKE_BASE=TRUE
→ PPBUS_5VS2_VIN 45 89

52 PPBUS_3V3S2_VIN
MIN_LINE_WIDTH=0.0970
MIN_NECK_WIDTH=0.1000
MAKE_BASE=TRUE
→ PPBUS_3V3S2_VIN 47 89

54 PPBUS_AON_L_SPKRAMP
MIN_LINE_WIDTH=0.0970
MIN_NECK_WIDTH=0.1000
MAKE_BASE=TRUE
→ PPBUS_AON_L_SPKRAMP 84
→ PPBUS_AON_L_SPKRAMP 82
→ PPBUS_AON_L_SPKRAMP 82
→ PPBUS_AON_L_SPKRAMP 90

54 PPBUS_AON_R_SPKRAMP
MIN_LINE_WIDTH=0.0970
MIN_NECK_WIDTH=0.1000
MAKE_BASE=TRUE
→ PPBUS_AON_R_SPKRAMP 84
→ PPBUS_AON_R_SPKRAMP 83
→ PPBUS_AON_R_SPKRAMP 83
→ PPBUS_AON_R_SPKRAMP 90

P3V8 VDD_MAIN

31 PP3V8_AON
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ PP3V8_AON 69
→ PP3V8_AON 88
→ PP3V8_AON 23
→ PP3V8_AON 54
→ PP3V8_AON 37 39 40 42
→ PP3V8_AON 39
→ PP3V8_AON 40
→ PP3V8_AON 33 36
→ PP3V8_AON 34
→ PP3V8_AON 34
→ PP3V8_AON 34
→ PP3V8_AON 34
→ PP3V8_AON 48
→ PP3V8_AON 24
→ PP3V8_AON 39
→ PP3V8_AON 82
→ PP3V8_AON 82
→ PP3V8_AON 83
→ PP3V8_AON 83
→ PP3V8_AON 32
→ PP3V8_AON 46
→ PP3V8_AON 67
→ PP3V8_AON 67
→ PP3V8_AON 67
→ PP3V8_AON 67
→ PP3V8_AON 85

P3V8 VDD_MAIN_WLBT

54 PP3V8_AON_WLBT
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ PP3V8_AON_WLBT 69

MPMU BUCK 0

37 PPVDD_AWAKE_PCPU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ PPVDD_AWAKE_PCPU 14
→ PPVDD_AWAKE_PCPU 91
→ PPVDD_AWAKE_PCPU 37

MPMU BUCK 1

37 PPVDD_AWAKE_GPU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ PPVDD_AWAKE_GPU 17
→ PPVDD_AWAKE_GPU 91
→ PPVDD_AWAKE_GPU 37

MPMU BUCK 2

37 PPVDD_S1_SOC
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ PPVDD_S1_SOC 15
→ PPVDD_S1_SOC 37
→ PPVDD_S1_SOC 91

MPMU BUCK 3

43 38 PP1V8_S2
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ PP1V8_S2 84
→ PP1V8_S2 38
→ PP1V8_S2 89
→ PP1V8_S2 38
→ PP1V8_S2 38
→ PP1V8_S2 38
→ PP1V8_S2 34
→ PP1V8_S2 33
→ PP1V8_S2 48
→ PP1V8_S2 76
→ PP1V8_S2 85
→ PP1V8_S2 87
→ PP1V8_S2 23
→ PP1V8_S2 57
→ PP1V8_S2 74
→ PP1V8_S2 69
→ PP1V8_S2 25 26
→ PP1V8_S2 75
→ PP1V8_S2 50
→ PP1V8_S2 50
→ PP1V8_S2 51
→ PP1V8_S2 51
→ PP1V8_S2 63
→ PP1V8_S2 64
→ PP1V8_S2 65
→ PP1V8_S2 65

MPMU BUCK 4

38 PP1V05_S2SW_VDD2H
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.5000
→ PP1V05_S2SW_VDD2H 18
→ PP1V05_S2SW_VDD2H 39
→ PP1V05_S2SW_VDD2H 39
→ PP1V05_S2SW_VDD2H 38
→ PP1V05_S2SW_VDD2H 91

Powers Unused MPMU LDO16

SPMU BUCK 5

33 PP0V779_S1_SRAM
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ PP0V779_S1_SRAM 16
→ PP0V779_S1_SRAM 33
→ PP0V779_S1_SRAM 91

SPMU BUCK 6

33 PP2V58_AWAKE_NAND_VCC
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ PP2V58_AWAKE_NAND_VCC 71 72
→ PP2V58_AWAKE_NAND_VCC 90
→ PP2V58_AWAKE_NAND_VCC 33

MPMU BUCK 7

38 PPVDD_AWAKE_CPU_SRAM
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.0990
MIN_LINE_WIDTH=0.2000
→ PPVDD_AWAKE_CPU_SRAM 16
→ PPVDD_AWAKE_CPU_SRAM 91
→ PPVDD_AWAKE_CPU_SRAM 38

SPMU BUCK 8

33 PPVDD_S1_DISP
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ PPVDD_S1_DISP 17
→ PPVDD_S1_DISP 91
→ PPVDD_S1_DISP 33

MPMU BUCK 9

38 PPVDD_S1_DCS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ PPVDD_S1_DCS 16
→ PPVDD_S1_DCS 91
→ PPVDD_S1_DCS 38

SPMU BUCK 10

33 PP0V5_S1_VDDQL
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ PP0V5_S1_VDDQL 7 18
→ PP0V5_S1_VDDQL 91
→ PP0V5_S1_VDDQL 33

MPMU BUCK 11

38 PPVDD_AWAKE_ECPU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ PPVDD_AWAKE_ECPU 19
→ PPVDD_AWAKE_ECPU 91
→ PPVDD_AWAKE_ECPU 38

SPMU BUCK 12

33 PP0V88_S1
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.0990
MIN_LINE_WIDTH=0.2000
→ PP0V88_S1 34
→ PP0V88_S1 34
→ PP0V88_S1 34
→ PP0V88_S1 33
→ PP0V88_S1 89

P5V LDO5

30 PP5V_AON
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ PP5V_AON
→ GDS_LDO_Enable 30

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MPMU BUCK 13

43 38 PP1V25_S2 ═══ PP1V25_S2
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000 88

PP1V25_S2 38
PP1V25_S2 89
PP1V25_S2 36
PP1V25_S2 38
PP1V25_S2 33
PP1V25_S2 34
PP1V25_S2 34
PP1V25_S2 42
PP1V25_S2 20
PP1V25_S2 21
PP1V25_S2 21
PP1V25_S2 20
PP1V25_S2 26
PP1V25_S2 7
PP1V25_S2 50
PP1V25_S2 51
PP1V25_S2 51
PP1V25_S2 51
PP1V25_S2 51
PP1V25_S2 50
PP1V25_S2 49
PP1V25_S2 81
PP1V25_S2 21
PP1V25_S2 69
PP1V25_S2 57
PP1V25_S2 26
PP1V25_S2 28
PP1V25_S2 61 63 64
PP1V25_S2 74
PP1V25_S2 85
PP1V25_S2 66
PP1V25_S2 66
PP1V25_S2 66
PP1V25_S2 68
PP1V25_S2 76
PP1V25_S2 86

SPMU BUCK 14

33 PP1V12_S2SW_AMPH ═══ PP1V12_S2SW_AMPH
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V12_S2SW_AMPH 18
PP1V12_S2SW_AMPH 33
PP1V12_S2SW_AMPH 91

MPMU BUCK 3 SW 1

38 PP1V8_AWAKE ═══ PP1V8_AWAKE
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V8_AWAKE 21
PP1V8_AWAKE 11
PP1V8_AWAKE 85
PP1V8_AWAKE 82 83

MPMU BUCK 3 SW 2

38 NC_PPVOUT_MPMU_SW2_REG ═══ NC_PPVOUT_MPMU_SW2_REG
MAKE_BASE=TRUE

MPMU BUCK 13 SW 3

38 PP1V25_AWAKE_IO ═══ PP1V25_AWAKE_IO
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V25_AWAKE_IO 21
PP1V25_AWAKE_IO 21
PP1V25_AWAKE_IO 21
PP1V25_AWAKE_IO 21
PP1V25_AWAKE_IO 21
PP1V25_AWAKE_IO 20
PP1V25_AWAKE_IO 20
PP1V25_AWAKE_IO 20
PP1V25_AWAKE_IO 20
PP1V25_AWAKE_IO 20
PP1V25_AWAKE_IO 20
PP1V25_AWAKE_IO 20
PP1V25_AWAKE_IO 13
PP1V25_AWAKE_IO 11
PP1V25_AWAKE_IO 11
PP1V25_AWAKE_IO 5
PP1V25_AWAKE_IO 7 9 10
PP1V25_AWAKE_IO 49
PP1V25_AWAKE_IO 36 42
PP1V25_AWAKE_IO 82
PP1V25_AWAKE_IO 85
PP1V25_AWAKE_IO 82 83

SPMU BUCK 3 SW 4

34 PP1V8_AWAKE_SPMU_GPIO ═══ PP1V8_AWAKE_SPMU_GPIO
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

SPMU BUCK 13 SW 5

34 PP1V25_AWAKE_NAND_VCCQ ═══ PP1V25_AWAKE_NAND_VCCQ
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V25_AWAKE_NAND_VCCQ 71 72
PP1V25_AWAKE_NAND_VCCQ 90

SPMU BUCK 12 SW 6/7

34 PP0V88_AWAKE_NAND_VDD ═══ PP0V88_AWAKE_NAND_VDD
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP0V88_AWAKE_NAND_VDD 71
PP0V88_AWAKE_NAND_VDD 72
PP0V88_AWAKE_NAND_VDD 90

SPMU BUCK 12 SW 7

TIED TO SW6

MPMU LDO 1

39 NC_MPMU_VLDO1 ═══ NC_MPMU_VLDO1
MAKE_BASE=TRUE

MPMU LDO 2

39 PP1V8_AON ═══ PP1V8_AON
MAKE_BASE=TRUE

PP1V8_AON 39
PP1V8_AON 43
PP1V8_AON 81
PP1V8_AON 48 70
PP1V8_AON 48 85
PP1V8_AON 86
PP1V8_AON 46
PP1V8_AON 26

MPMU LDO 3

39 NC_MPMU_VLDO3 ═══ NC_MPMU_VLDO3
MAKE_BASE=TRUE

SPMU LDO 4

34 PP0V72_S2_VDD_LOW ═══ PP0V72_S2_VDD_LOW
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP0V72_S2_VDD_LOW 34
PP0V72_S2_VDD_LOW 21
PP0V72_S2_VDD_LOW 21
PP0V72_S2_VDD_LOW 21
PP0V72_S2_VDD_LOW 21
PP0V72_S2_VDD_LOW 91

MPMU LDO 5

39 NC_MPMU_VLDO5 ═══ NC_MPMU_VLDO5
MAKE_BASE=TRUE

SPMU LDO 6

34 NC_SPMU_VLDO6 ═══ NC_SPMU_VLDO6
MAKE_BASE=TRUE

MPMU LDO 7

39 PP3V3_S2_LDO ═══ PP3V3_S2_LDO
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP3V3_S2_LDO 39
PP3V3_S2_LDO 61 63 64
PP3V3_S2_LDO 28
PP3V3_S2_LDO 66
PP3V3_S2_LDO 65
PP3V3_S2_LDO 65
PP3V3_S2_LDO 66

MPMU LDO 8

39 PP1V2_AWAKE_PLL ═══ PP1V2_AWAKE_PLL
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.5000

PP1V2_AWAKE_PLL 39
PP1V2_AWAKE_PLL 20
PP1V2_AWAKE_PLL 20
PP1V2_AWAKE_PLL 20
PP1V2_AWAKE_PLL 20
PP1V2_AWAKE_PLL 21
PP1V2_AWAKE_PLL 91

MPMU LDO 9

39 PP1V8_AON_MPMU ═══ PP1V8_AON_MPMU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.0990
MIN_LINE_WIDTH=0.2000

PP1V8_AON_MPMU 39 41
PP1V8_AON_MPMU 40 42
PP1V8_AON_MPMU 26
PP1V8_AON_MPMU 86

MPMU LDO 9B

39 PP1V2_AON_MPMU ═══ PP1V2_AON_MPMU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.0990
MIN_LINE_WIDTH=0.0990

PP1V2_AON_MPMU 39
PP1V2_AON_MPMU 38

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SPMU LDO 9

34 PP1V8_AON_SPMU

PP1V8_AON_SPMU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V8_AON_SPMU 34

SPMU LDO 9B

34 PP1V2_AON_SPMU

PP1V2_AON_SPMU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V2_AON_SPMU 34
PP1V2_AON_SPMU 33

MPMU LDO 10

39 PP3V3_AON

PP3V3_AON
MAKE_BASE=TRUE

PP3V3_AON 39
PP3V3_AON 43
PP3V3_AON 85
PP3V3_AON 88

MPMU LDO 11

39 PP0V855_S2SW_CIO

PP0V855_S2SW_CIO
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.5000

PP0V855_S2SW_CIO 21
PP0V855_S2SW_CIO 21
PP0V855_S2SW_CIO 39

SPMU LDO12

34 PP0V78_S1_VDD_FIXED

PP0V78_S1_VDD_FIXED
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP0V78_S1_VDD_FIXED 34
PP0V78_S1_VDD_FIXED 19
PP0V78_S1_VDD_FIXED 19
PP0V78_S1_VDD_FIXED 15
PP0V78_S1_VDD_FIXED 13
PP0V78_S1_VDD_FIXED 19
PP0V78_S1_VDD_FIXED 19
PP0V78_S1_VDD_FIXED 19
PP0V78_S1_VDD_FIXED 19
PP0V78_S1_VDD_FIXED 19
PP0V78_S1_VDD_FIXED 19
PP0V78_S1_VDD_FIXED 91

UC710 - 3V3_S2

47 PP3V3_S2

Sourced from PBus
Enabled by P3V3S2_PWR_EN

PP3V3_S2
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
MAKE_BASE=TRUE

PP3V3_S2 47
PP3V3_S2 46
PP3V3_S2 89
PP3V3_S2 48
PP3V3_S2 76
PP3V3_S2 88

UC300 - 5V S2

45 PP5V_S2

Sourced from PBus
Enabled by P5VS2_PWR_EN

PP5V_S2
MIN_LINE_WIDTH=0.0990
MIN_NECK_WIDTH=0.0990
MAKE_BASE=TRUE

PP5V_S2 46
PP5V_S2 32
PP5V_S2 77
PP5V_S2 76
PP5V_S2 54
PP5V_S2 48
PP5V_S2 74
PP5V_S2 63 64
PP5V_S2 63 64
PP5V_S2 26

Trackpad - 5V S2

48 PP5V_S2SW_IPD

PP5V_S2SW_IPD
MIN_LINE_WIDTH=0.0970
MIN_NECK_WIDTH=0.1000
MAKE_BASE=TRUE

PP5V_S2SW_IPD 87

MPMU LDO13

39 PP3V3_S2SW_SNS

PP3V3_S2SW_SNS
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.0970
MIN_NECK_WIDTH=0.1000

PP3V3_S2SW_SNS 39
PP3V3_S2SW_SNS 52 53 54

MPMU LDO14

39 NC_MPMU_VLDO14

NC_MPMU_VLDO14
MAKE_BASE=TRUE

SPMU LDO15

34 NC_SPMU_VLDO15

NC_SPMU_VLDO15
MAKE_BASE=TRUE

MPMU LDO16

39 NC_MPMU_VLDO16

NC_MPMU_VLDO16
MAKE_BASE=TRUE

SPMU LDO17

34 NC_SPMU_VLDO17

NC_SPMU_VLDO17
MAKE_BASE=TRUE

SPMU LDO18

34 NC_SPMU_VLDO18

NC_SPMU_VLDO18
MAKE_BASE=TRUE

48 PP3V3_S2SW_IPD

PP3V3_S2SW_IPD
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.0970
MIN_NECK_WIDTH=0.1000

PP3V3_S2SW_IPD 87 90
PP3V3_S2SW_IPD 86
PP3V3_S2SW_IPD 51

76 PP3V3_SW_LCD

PP3V3_SW_LCD
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

PP3V3_SW_LCD 75
PP3V3_SW_LCD 90
PP3V3_SW_LCD 79

76 PP5V_SW_MINNIE

PP5V_SW_MINNIE
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

PP5V_SW_MINNIE 75

76 PP1V25_SW_MINNIE

PP1V25_SW_MINNIE
MAKE_BASE=TRUE

PP1V25_SW_MINNIE 75
PP1V25_SW_MINNIE 49

48 PP1V8_S2SW

PP1V8_S2SW
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000

PP1V8_S2SW 18
PP1V8_S2SW 91

Keyboard Backlight - 5V S2

54 PP5V_S2_KBDLED

PP5V_S2_KBDLED
MIN_LINE_WIDTH=0.0970
MIN_NECK_WIDTH=0.1000
MAKE_BASE=TRUE

PP5V_S2_KBDLED 85
PP5V_S2_KBDLED 90

48 PPBUS_AONSW_TPAD

PPBUS_AONSW_TPAD
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.0990
MIN_NECK_WIDTH=0.0990

PPBUS_AONSW_TPAD 87

Digital Ground

GND

MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.0900

MPMU LDO19

(NOT USED)

MPMU LDO20

39 PP1V2_S2_CIO

PP1V2_S2_CIO
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.5000

PP1V2_S2_CIO 39
PP1V2_S2_CIO 20
PP1V2_S2_CIO 20
PP1V2_S2_CIO 91

MPMU LDOINT

39 PP1V5_LDOINT_MPMU

PP1V5_LDOINT_MPMU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V5_LDOINT_MPMU 39
PP1V5_LDOINT_MPMU 37
PP1V5_LDOINT_MPMU 37
PP1V5_LDOINT_MPMU 39

SPMU LDOINT

34 PP1V5_LDOINT_SPMU

PP1V5_LDOINT_SPMU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V5_LDOINT_SPMU 34
PP1V5_LDOINT_SPMU 33
PP1V5_LDOINT_SPMU 33

MPMU VDD BOOST

40 PP5V_MPMU_BSTLQ

PP5V_MPMU_BSTLQ
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP5V_MPMU_BSTLQ 38

SPMU VDD BOOST

33 PP5V_SPMU_BSTLQ

PP5V_SPMU_BSTLQ
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP5V_SPMU_BSTLQ 33

MPMU LDO RTC

SHORTED TO MPMU LDOINT FOR PORTABLES

Display Backlight Rails

77 PPVOUT_LCDBKLT

PPVOUT_LCDBKLT
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.1000

PPVOUT_LCDBKLT 75
PPVOUT_LCDBKLT 75 90

78 PPVIN_LCDBKLT

PPVIN_LCDBKLT
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.1000

PPVIN_LCDBKLT 77

98 PPVOUT_LCDBKLT_D

PPVOUT_LCDBKLT_D
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.1000

SYNC_DATE=09/10/2021

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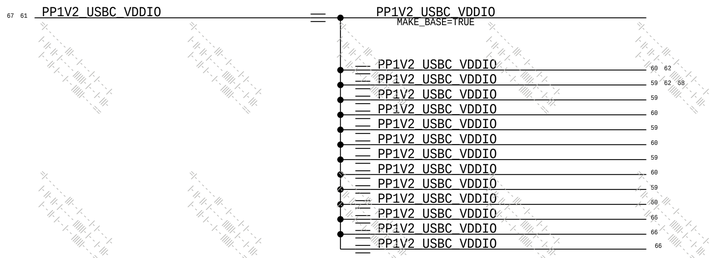
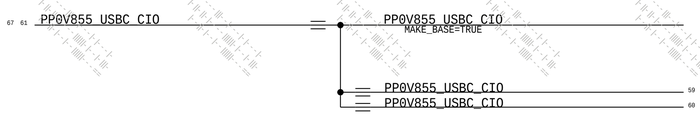
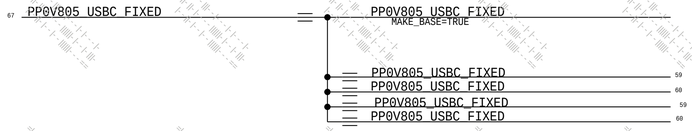
USB 1V2 VDDIO



USB 0V855 CIO



USB 0V805 Fixed



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A Lid Angle Sensor Aliases

85	AMR_LEFT_OR_ND_1V8	MAKE_BASE=TRUE	AMR_LEFT_OR_ND_1V8	81
			AMR_LEFT_OR_ND_1V8	81

B Speaker Amplifier Aliases

9	IN TDM_SPKRAMP_L_D2R	MAKE_BASE=TRUE	TDM_SPKRAMP_L_D2R	82
			TDM_SPKRAMP_L_D2R	82
9	IN TDM_SPKRAMP_R_D2R	MAKE_BASE=TRUE	TDM_SPKRAMP_R_D2R	83
			TDM_SPKRAMP_R_D2R	83

C PMU Aliases

35	SWD_NUB_SWCLK_SPMU	MAKE_BASE=TRUE	SWD_NUB_SWCLK_SPMU	12
35	SWD_NUB_SWDIO_SPMU	MAKE_BASE=TRUE	SWD_NUB_SWDIO_SPMU	12
41	SWD_NUB_SWCLK_MPMU	MAKE_BASE=TRUE	SWD_NUB_SWCLK_MPMU	12
41	SWD_NUB_SWDIO_MPMU	MAKE_BASE=TRUE	SWD_NUB_SWDIO_MPMU	12
76	PMU_SYS_ALIVE	MAKE_BASE=TRUE	PMU_SYS_ALIVE	41 42 73 88

D Charger Aliases

26	P5VS2_PGOOD	MAKE_BASE=TRUE	P5VS2_PGOOD	45
25	NC_CHGR_CBC_ON	MAKE_BASE=TRUE	NC_CHGR_CBC_ON	
25	NC_CHGR_EN_VR1	MAKE_BASE=TRUE	NC_CHGR_EN_VR1	
25	NC_CHGR_SMC_RST_L	MAKE_BASE=TRUE	NC_CHGR_SMC_RST_L	

E PP5V_S2 Aliases

26	P5VS2_PWR_EN	MAKE_BASE=TRUE	P5VS2_PWR_EN	45 46 48
45	P5VS2_EN	MAKE_BASE=TRUE	P5VS2_EN	45

F Display Aliases

75	UART_TCON_D2R	MAKE_BASE=TRUE	UART_TCON_D2R	8
77	NC_BKLT_ISET_KEYB	MAKE_BASE=TRUE	NC_BKLT_ISET_KEYB	
77	NC_BKLT_KEYB1	MAKE_BASE=TRUE	NC_BKLT_KEYB1	
77	NC_BKLT_KEYB2	MAKE_BASE=TRUE	NC_BKLT_KEYB2	
77	NC_KBDBKLT_SW2	MAKE_BASE=TRUE	NC_KBDBKLT_SW2	
77	NC_VOUT_KEYBDLED_FB2	MAKE_BASE=TRUE	NC_VOUT_KEYBDLED_FB2	
77	UNUSED_LP8548_PWM	MAKE_BASE=TRUE	UNUSED_LP8548_PWM	

G Secure Element Aliases

23	NC_SE_GPIO0	MAKE_BASE=TRUE	NC_SE_GPIO0	
23	NC_I2C_SE_SCL	MAKE_BASE=TRUE	NC_I2C_SE_SCL	
23	NC_I2C_SE_SDA	MAKE_BASE=TRUE	NC_I2C_SE_SDA	

H NAND Aliases

71	NC_NAND0_S5E0_VPP	MAKE_BASE=TRUE	NC_NAND0_S5E0_VPP	
72	NC_NAND0_S5E1_VPP	MAKE_BASE=TRUE	NC_NAND0_S5E1_VPP	

I Wireless Module Aliases

70 69	NC_RF_BT_DED	MAKE_BASE=TRUE	NC_RF_BT_DED	
	TPT_WLAN_JTAG_TCK	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TCK	69 70
	TPT_WLAN_JTAG_TMS	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TMS	69 70
	TPT_WLAN_JTAG_TRSTN	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TRSTN	69
	TPT_WLAN_JTAG_TDI	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TDI	69

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A USB-C Aliases: USB 2.0 I/F

65	USB2_ATC0_LS_P	MAKE_BASE=TRUE	USB2_ATC0_LS_P		68
65	USB2_ATC0_LS_N	MAKE_BASE=TRUE	USB2_ATC0_LS_N		68
65	USB2_ATC1_LS_P	MAKE_BASE=TRUE	USB2_ATC1_LS_P		68
65	USB2_ATC1_LS_N	MAKE_BASE=TRUE	USB2_ATC1_LS_N		68
65	USB_DBG_LS_P	MAKE_BASE=TRUE	USB_DBG_LS_P		62
65	USB_DBG_LS_N	MAKE_BASE=TRUE	USB_DBG_LS_N		62

B USB-C Aliases: CIO Debug I/F

	CIO_ATC0_LSRX	MAKE_BASE=TRUE	CIO_ATC0_LSRX	6	59
	CIO_ATC0_LSTX	MAKE_BASE=TRUE	CIO_ATC0_LSTX	6	59
	CIO_ATC1_LSRX	MAKE_BASE=TRUE	CIO_ATC1_LSRX	6	60
	CIO_ATC1_LSTX	MAKE_BASE=TRUE	CIO_ATC1_LSTX	6	60

C USB-C Aliases: EUSB I/F

65	EUSB_ATC0_P	MAKE_BASE=TRUE	EUSB_ATC0_P	6	13
65	EUSB_ATC0_N	MAKE_BASE=TRUE	EUSB_ATC0_N	6	13
65	EUSB_ATC1_P	MAKE_BASE=TRUE	EUSB_ATC1_P	6	13
65	EUSB_ATC1_N	MAKE_BASE=TRUE	EUSB_ATC1_N	6	13
13 7	EUSB_DBG_P	MAKE_BASE=TRUE	EUSB_DBG_P	65	
13 7	EUSB_DBG_N	MAKE_BASE=TRUE	EUSB_DBG_N	65	
65	ATCRTMR0_RESET_1V2_L	MAKE_BASE=TRUE	ATCRTMR0_RESET_1V2_L	62	66

D USB-C Aliases: I2C I/F

59	I2C_UPC0_ATCRTMR0_SDA_1V2	MAKE_BASE=TRUE	I2C_UPC0_ATCRTMR0_SDA_1V2		66
65	I2C_UPC0_ATCRTMR0_SDA_1V2				
59	I2C_UPC0_ATCRTMR0_SCL_1V2	MAKE_BASE=TRUE	I2C_UPC0_ATCRTMR0_SCL_1V2		66
65	I2C_UPC0_ATCRTMR0_SCL_1V2				
60	I2C_UPC1_ATCRTMR1_SDA_1V2	MAKE_BASE=TRUE	I2C_UPC1_ATCRTMR1_SDA_1V2		66
65	I2C_UPC1_ATCRTMR1_SDA_1V2				
60	I2C_UPC1_ATCRTMR1_SCL_1V2	MAKE_BASE=TRUE	I2C_UPC1_ATCRTMR1_SCL_1V2		66
65	I2C_UPC1_ATCRTMR1_SCL_1V2				

E USB-C Aliases: SWD I/F

59	SWD_NUB_ATCRTMR_SWCLK	MAKE_BASE=TRUE	SWD_NUB_ATCRTMR_SWCLK		13
60	SWD_NUB_ATCRTMR_SWCLK				
59	SWD_NUB_ATCRTMR_SWDIO	MAKE_BASE=TRUE	SWD_NUB_ATCRTMR_SWDIO		13
60	SWD_NUB_ATCRTMR_SWDIO				

F USB-C Aliases: CC I/F

97 62	NC_USBC0_CC_FLT_L	MAKE_BASE=TRUE	NC_USBC0_CC_FLT_L	62	97
97 62	NC_USBC1_CC_FLT_L	MAKE_BASE=TRUE	NC_USBC1_CC_FLT_L	62	97

G USB-C Aliases: GPIO

59	TP_ATCRTMR0_GPIO_0	MAKE_BASE=TRUE	TP_ATCRTMR0_GPIO_0		
59	NC_ATCRTMR0_GPIO_1	MAKE_BASE=TRUE	NC_ATCRTMR0_GPIO_1		
59	TP_ATCRTMR0_GPIO_2	MAKE_BASE=TRUE	TP_ATCRTMR0_GPIO_2		
59	TP_ATCRTMR0_GPIO_3	MAKE_BASE=TRUE	TP_ATCRTMR0_GPIO_3		
60	TP_ATCRTMR1_GPIO_0	MAKE_BASE=TRUE	TP_ATCRTMR1_GPIO_0		
60	NC_ATCRTMR1_GPIO_1	MAKE_BASE=TRUE	NC_ATCRTMR1_GPIO_1		
60	TP_ATCRTMR1_GPIO_2	MAKE_BASE=TRUE	TP_ATCRTMR1_GPIO_2		
60	TP_ATCRTMR1_GPIO_3	MAKE_BASE=TRUE	TP_ATCRTMR1_GPIO_3		

Leave these as TP, so that RT13 debug modes can be enabled.

H USB-C Aliases: VDD I/O Fuse I/F

68 59	ATCRTMR0_VDDIO_EFUSE	MAKE_BASE=TRUE	ATCRTMR0_VDDIO_EFUSE		
68 60	ATCRTMR1_VDDIO_EFUSE	MAKE_BASE=TRUE	ATCRTMR1_VDDIO_EFUSE		

I USB-C Aliases: SOC Dock Connect

62	SOC_DOCK_CONNECT	MAKE_BASE=TRUE	SOC_DOCK_CONNECT		7

J USB-C Aliases: UPC I2C

28	I2C_UPC01_3V3_SDA	MAKE_BASE=TRUE	I2C_UPC01_3V3_SDA	61	68
28	I2C_UPC01_3V3_SCL	MAKE_BASE=TRUE	I2C_UPC01_3V3_SCL	61	68

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A GPIO AOP ALIAS

NC_SOC_AOP_I2CM1_SCL	NC_SOC_AOP_I2CM1_SCL	MAKE_BASE=TRUE
NC_SOC_AOP_I2CM1_SDA	NC_SOC_AOP_I2CM1_SDA	MAKE_BASE=TRUE
NC_SOC_AOP_I2CM2_SCL	NC_SOC_AOP_I2CM2_SCL	MAKE_BASE=TRUE
NC_SOC_AOP_I2CM2_SDA	NC_SOC_AOP_I2CM2_SDA	MAKE_BASE=TRUE
NC_AOP_I2S0_LRCLK	NC_AOP_I2S0_LRCLK	MAKE_BASE=TRUE
NC_AOP_I2S0_LRCLK	NC_AOP_I2S0_LRCLK	MAKE_BASE=TRUE
NC_SOC_AOP_UART0_RXD	NC_SOC_AOP_UART0_RXD	MAKE_BASE=TRUE
NC_SOC_AOP_UART0_TXD	NC_SOC_AOP_UART0_TXD	MAKE_BASE=TRUE
NC_SOC_AOP_UART1_RXD	NC_SOC_AOP_UART1_RXD	MAKE_BASE=TRUE
NC_SOC_AOP_UART1_TXD	NC_SOC_AOP_UART1_TXD	MAKE_BASE=TRUE
NC_SOC_AOP_UART2_RXD	NC_SOC_AOP_UART2_RXD	MAKE_BASE=TRUE
NC_SOC_AOP_UART2_TXD	NC_SOC_AOP_UART2_TXD	MAKE_BASE=TRUE
NC_AOP_FUNC0	NC_AOP_FUNC0	MAKE_BASE=TRUE
NC_AOP_FUNC1	NC_AOP_FUNC1	MAKE_BASE=TRUE
NC_AOP_FUNC2	NC_AOP_FUNC2	MAKE_BASE=TRUE
NC_AOP_FUNC3	NC_AOP_FUNC3	MAKE_BASE=TRUE
NC_AOP_FUNC11	NC_AOP_FUNC11	MAKE_BASE=TRUE
NC_AOP_FUNC12	NC_AOP_FUNC12	MAKE_BASE=TRUE
NC_AOP_FUNC20	NC_AOP_FUNC20	MAKE_BASE=TRUE
NC_HDMI_CEC_AOP_TX	NC_HDMI_CEC_AOP_TX	MAKE_BASE=TRUE
NC_HDMI_CEC_AOP_RX	NC_HDMI_CEC_AOP_RX	MAKE_BASE=TRUE
NC_HDMI_HDP_AOP	NC_HDMI_HDP_AOP	MAKE_BASE=TRUE
TP_SOC_DOCK_ATTENTION	TP_SOC_DOCK_ATTENTION	MAKE_BASE=TRUE
NC_AOP_FUNC19	NC_AOP_FUNC19	MAKE_BASE=TRUE
NC_TOUCHID_BKLT_PWM	NC_TOUCHID_BKLT_PWM	MAKE_BASE=TRUE

B GPIO AP ALIAS

NC_BKLT_PWR_ON	NC_BKLT_PWR_ON	MAKE_BASE=TRUE
NC_SOC_AP_GPIO_1	NC_SOC_AP_GPIO_1	MAKE_BASE=TRUE
NC_CCG_I2C_INT	NC_CCG_I2C_INT	MAKE_BASE=TRUE
NC_DMIC_ID	NC_DMIC_ID	MAKE_BASE=TRUE
NC_SOC_AP_GPIO_18	NC_SOC_AP_GPIO_18	MAKE_BASE=TRUE
NC_SOC_AP_GPIO_19	NC_SOC_AP_GPIO_19	MAKE_BASE=TRUE
NC_ENET_I2C_LOM_INT_L	NC_ENET_I2C_LOM_INT_L	MAKE_BASE=TRUE
NC_SOC_AP_GPIO_23	NC_SOC_AP_GPIO_23	MAKE_BASE=TRUE
NC_SOC_AP_GPIO_24	NC_SOC_AP_GPIO_24	MAKE_BASE=TRUE
NC_ENET_SELECT_1G_H_10G_L	NC_ENET_SELECT_1G_H_10G_L	MAKE_BASE=TRUE
NC_SOC_AP_GPIO_26	NC_SOC_AP_GPIO_26	MAKE_BASE=TRUE
NC_SOC_AP_UART1_CTS_L	NC_SOC_AP_UART1_CTS_L	MAKE_BASE=TRUE
NC_SOC_AP_UART1_RTS_L	NC_SOC_AP_UART1_RTS_L	MAKE_BASE=TRUE
NC_SOC_AP_UART1_RXD	NC_SOC_AP_UART1_RXD	MAKE_BASE=TRUE
NC_SOC_AP_UART1_TXD	NC_SOC_AP_UART1_TXD	MAKE_BASE=TRUE
NC_SOC_AP_UART3_CTS_L	NC_SOC_AP_UART3_CTS_L	MAKE_BASE=TRUE
NC_SOC_AP_UART3_RTS_L	NC_SOC_AP_UART3_RTS_L	MAKE_BASE=TRUE
NC_SOC_AP_UART3_RXD	NC_SOC_AP_UART3_RXD	MAKE_BASE=TRUE
NC_SOC_AP_UART3_TXD	NC_SOC_AP_UART3_TXD	MAKE_BASE=TRUE
NC_SOC_AP_UART4_RXD	NC_SOC_AP_UART4_RXD	MAKE_BASE=TRUE
NC_SOC_AP_UART4_TXD	NC_SOC_AP_UART4_TXD	MAKE_BASE=TRUE
NC_UART_TCON_R2D	NC_UART_TCON_R2D	MAKE_BASE=TRUE
NC_UART_HDMI_D2R	NC_UART_HDMI_D2R	MAKE_BASE=TRUE
NC_UART_HDMI_R2D	NC_UART_HDMI_R2D	MAKE_BASE=TRUE
NC_SOC_AP_UART2_RXD	NC_SOC_AP_UART2_RXD	MAKE_BASE=TRUE
NC_SOC_AP_UART2_TXD	NC_SOC_AP_UART2_TXD	MAKE_BASE=TRUE
NC_SOC_AP_UART2_CTS_L	NC_SOC_AP_UART2_CTS_L	MAKE_BASE=TRUE
NC_SOC_AP_UART2_RTS_L	NC_SOC_AP_UART2_RTS_L	MAKE_BASE=TRUE

C DEBUG ALIAS

NC_AON_SLEEP1_RESET_L	NC_AON_SLEEP1_RESET_L	MAKE_BASE=TRUE
NC_SOC_SWD_TMS3	NC_SOC_SWD_TMS3	MAKE_BASE=TRUE
NC_SWD_R1_SWDIO	NC_SWD_R1_SWDIO	MAKE_BASE=TRUE

D GND ALIAS

The DUT_GND_DETECT signal is for dev only,
and should be tied to GND.

GND — MAKE_BASE=TRUE — GND — IN — 22

SYNC_MASTER=jwebb SYNC_DATE=09/28/2021

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A SPI & I2S ALIAS

9	NC_TDM_SPKRAMP_TOP_BCLK_R	NC_TDM_SPKRAMP_TOP_BCLK_R	MAKE_BASE=TRUE
9	NC_TDM_SPKRAMP_TOP_D2R	NC_TDM_SPKRAMP_TOP_D2R	MAKE_BASE=TRUE
9	NC_TDM_SPKRAMP_TOP_R2D_R	NC_TDM_SPKRAMP_TOP_R2D_R	MAKE_BASE=TRUE
9	NC_TDM_SPKRAMP_TOP_FSYNC_R	NC_TDM_SPKRAMP_TOP_FSYNC_R	MAKE_BASE=TRUE
9	NC_SOC_AP_SPMI0_SCLK	NC_SOC_AP_SPMI0_SCLK	MAKE_BASE=TRUE
9	NC_SOC_AP_SPMI0_SDATA	NC_SOC_AP_SPMI0_SDATA	MAKE_BASE=TRUE
9	NC_SOC_AP_SPI5_MISO	NC_SOC_AP_SPI5_MISO	MAKE_BASE=TRUE
9	NC_SOC_AP_SPI5_MOSI	NC_SOC_AP_SPI5_MOSI	MAKE_BASE=TRUE
9	NC_SOC_AP_SPI5_SCLK	NC_SOC_AP_SPI5_SCLK	MAKE_BASE=TRUE
9	NC_SOC_AP_SPI5_CS_L	NC_SOC_AP_SPI5_CS_L	MAKE_BASE=TRUE
9	NC_SOC_SSPI0_MISO	NC_SOC_SSPI0_MISO	MAKE_BASE=TRUE
9	NC_SOC_SSPI0_MOSI	NC_SOC_SSPI0_MOSI	MAKE_BASE=TRUE
9	NC_SOC_SSPI0_SCLK	NC_SOC_SSPI0_SCLK	MAKE_BASE=TRUE
9	NC_SOC_SGPIO_1	NC_SOC_SGPIO_1	MAKE_BASE=TRUE
9	NC_SOC_AP_SPI2_CS_L	NC_SOC_AP_SPI2_CS_L	MAKE_BASE=TRUE
99 9	NC_SOC_AP_I2S0_MCK	NC_SOC_AP_I2S0_MCK	MAKE_BASE=TRUE 99
99 9	NC_SOC_AP_I2S1_MCK	NC_SOC_AP_I2S1_MCK	MAKE_BASE=TRUE 99
99 9	NC_SOC_AP_I2S2_MCK	NC_SOC_AP_I2S2_MCK	MAKE_BASE=TRUE 99
8	NC_PDM_DMIC_DATA4	NC_PDM_DMIC_DATA4	MAKE_BASE=TRUE
8	NC_PDM_DMIC_CLK2_R	NC_PDM_DMIC_CLK2_R	MAKE_BASE=TRUE
8	NC_AOP_I2S0_BCLK	NC_AOP_I2S0_BCLK	MAKE_BASE=TRUE
8	NC_AOP_I2S0_DIN	NC_AOP_I2S0_DIN	MAKE_BASE=TRUE
8	NC_AOP_I2S0_DOUT	NC_AOP_I2S0_DOUT	MAKE_BASE=TRUE
8	NC_SOC_AOP_SPI1_CS_L	NC_SOC_AOP_SPI1_CS_L	MAKE_BASE=TRUE
99 8	NC_SPI_DP2HDMI_HOLD_L	NC_SPI_DP2HDMI_HOLD_L	MAKE_BASE=TRUE 99
99 9	NC_SOC_AP_I2S0_MCK	NC_SOC_AP_I2S0_MCK	MAKE_BASE=TRUE 99
99 9	NC_SOC_AP_I2S1_MCK	NC_SOC_AP_I2S1_MCK	MAKE_BASE=TRUE 99
99 9	NC_SOC_AP_I2S2_MCK	NC_SOC_AP_I2S2_MCK	MAKE_BASE=TRUE 99
99 8	NC_SPI_DP2HDMI_HOLD_L	NC_SPI_DP2HDMI_HOLD_L	MAKE_BASE=TRUE 99
9	NC_SOC_SPI3_MOSI	NC_SOC_SPI3_MOSI	MAKE_BASE=TRUE
9	NC_SOC_SPI3_MISO	NC_SOC_SPI3_MISO	MAKE_BASE=TRUE
9	NC_SOC_SPI3_SCLK	NC_SOC_SPI3_SCLK	MAKE_BASE=TRUE
9	NC_SOC_SPI3_SSIN	NC_SOC_SPI3_SSIN	MAKE_BASE=TRUE
8	NC_SOC_GPIO16	NC_SOC_GPIO16	MAKE_BASE=TRUE
8	NC_SOC_GPIO17	NC_SOC_GPIO17	MAKE_BASE=TRUE

B GPIO MTP ALIAS

9	NC_SOC_MTP_I2C0_SCL	NC_SOC_MTP_I2C0_SCL	MAKE_BASE=TRUE
9	NC_SOC_MTP_I2C0_SDA	NC_SOC_MTP_I2C0_SDA	MAKE_BASE=TRUE
9	NC_SOC_MTP_FUNC_6	NC_SOC_MTP_FUNC_6	MAKE_BASE=TRUE
9	NC_SOC_MTP_FUNC_7	NC_SOC_MTP_FUNC_7	MAKE_BASE=TRUE
9	IPD_MTP_FUNC_1	IPD_MTP_FUNC_1	MAKE_BASE=TRUE 86
9	NC_SOC_MTP_FUNC_2	NC_SOC_MTP_FUNC_2	MAKE_BASE=TRUE

C AUDIO I2C

9	I2C_SPKRAMP_L_SDA	I2C_SPKRAMP_L_SDA	MAKE_BASE=TRUE 49
9	I2C_SPKRAMP_L_SCL	I2C_SPKRAMP_L_SCL	MAKE_BASE=TRUE 49
9	I2C_SPKRAMP_R_CODEC_SDA	I2C_SPKRAMP_R_CODEC_SDA	MAKE_BASE=TRUE 49
9	I2C_SPKRAMP_R_CODEC_SCL	I2C_SPKRAMP_R_CODEC_SCL	MAKE_BASE=TRUE 49

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SOC: ALIASES SPI, I2S

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A LPDP ALIAS

NC_SOC_LPDP_RX_AUX_D1	NC_SOC_LPDP_RX_AUX_D1	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_AUX_D2	NC_SOC_LPDP_RX_AUX_D2	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_AUX_D3	NC_SOC_LPDP_RX_AUX_D3	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_AUX_D4	NC_SOC_LPDP_RX_AUX_D4	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_AUX_D5	NC_SOC_LPDP_RX_AUX_D5	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_AUX_D6	NC_SOC_LPDP_RX_AUX_D6	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_AUX_D7	NC_SOC_LPDP_RX_AUX_D7	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_AUX_D8	NC_SOC_LPDP_RX_AUX_D8	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_AUX_D9	NC_SOC_LPDP_RX_AUX_D9	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_AUX_D10	NC_SOC_LPDP_RX_AUX_D10	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_AUX_D11	NC_SOC_LPDP_RX_AUX_D11	MAKE_BASE=TRUE
NC_SOC_ST_PCIE_PERST_1_L	NC_SOC_ST_PCIE_PERST_1_L	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D1P	NC_SOC_LPDP_RX_D1P	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D1N	NC_SOC_LPDP_RX_D1N	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D2P	NC_SOC_LPDP_RX_D2P	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D2N	NC_SOC_LPDP_RX_D2N	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D3P	NC_SOC_LPDP_RX_D3P	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D3N	NC_SOC_LPDP_RX_D3N	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D4P	NC_SOC_LPDP_RX_D4P	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D4N	NC_SOC_LPDP_RX_D4N	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D5P	NC_SOC_LPDP_RX_D5P	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D5N	NC_SOC_LPDP_RX_D5N	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D6P	NC_SOC_LPDP_RX_D6P	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D6N	NC_SOC_LPDP_RX_D6N	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D7P	NC_SOC_LPDP_RX_D7P	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D7N	NC_SOC_LPDP_RX_D7N	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D8P	NC_SOC_LPDP_RX_D8P	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D8N	NC_SOC_LPDP_RX_D8N	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D9P	NC_SOC_LPDP_RX_D9P	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D9N	NC_SOC_LPDP_RX_D9N	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D10P	NC_SOC_LPDP_RX_D10P	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D10N	NC_SOC_LPDP_RX_D10N	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D11P	NC_SOC_LPDP_RX_D11P	MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D11N	NC_SOC_LPDP_RX_D11N	MAKE_BASE=TRUE
NC_LPDP_EXT_DATA_CP<0>	NC_LPDP_EXT_DATA_CP<0>	MAKE_BASE=TRUE
NC_LPDP_EXT_DATA_CN<0>	NC_LPDP_EXT_DATA_CN<0>	MAKE_BASE=TRUE
NC_LPDP_EXT_DATA_CP<1>	NC_LPDP_EXT_DATA_CP<1>	MAKE_BASE=TRUE
NC_LPDP_EXT_DATA_CN<1>	NC_LPDP_EXT_DATA_CN<1>	MAKE_BASE=TRUE
NC_LPDP_EXT_DATA_CP<2>	NC_LPDP_EXT_DATA_CP<2>	MAKE_BASE=TRUE
NC_LPDP_EXT_DATA_CN<2>	NC_LPDP_EXT_DATA_CN<2>	MAKE_BASE=TRUE
NC_LPDP_EXT_DATA_CP<3>	NC_LPDP_EXT_DATA_CP<3>	MAKE_BASE=TRUE
NC_LPDP_EXT_DATA_CN<3>	NC_LPDP_EXT_DATA_CN<3>	MAKE_BASE=TRUE
NC_LPDP_EXT_AUX_CP	NC_LPDP_EXT_AUX_CP	MAKE_BASE=TRUE
NC_LPDP_EXT_AUX_CN	NC_LPDP_EXT_AUX_CN	MAKE_BASE=TRUE
NC_LPDP_EXT_HPD	NC_LPDP_EXT_HPD	MAKE_BASE=TRUE
NC_SOC_LPDP_RX1_RCAL_POS	NC_SOC_LPDP_RX1_RCAL_POS	MAKE_BASE=TRUE
NC_SOC_LPDP_RX1_RCAL_NEG	NC_SOC_LPDP_RX1_RCAL_NEG	MAKE_BASE=TRUE

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SOC: ALIASES LPDP RX

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A PCIe ALIAS

10	NC_SOC_GP_PCIE_RX1P	NC_SOC_GP_PCIE_RX1P	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_RX1N	NC_SOC_GP_PCIE_RX1N	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_TX1P	NC_SOC_GP_PCIE_TX1P	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_TX1N	NC_SOC_GP_PCIE_TX1N	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_CLK1_100MP	NC_SOC_GP_PCIE_CLK1_100MP	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_CLK1_100MN	NC_SOC_GP_PCIE_CLK1_100MN	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_CLKREQ_1_L	NC_SOC_GP_PCIE_CLKREQ_1_L	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_PERST_1_L	NC_SOC_GP_PCIE_PERST_1_L	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_RX2P	NC_SOC_GP_PCIE_RX2P	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_RX2N	NC_SOC_GP_PCIE_RX2N	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_TX2P	NC_SOC_GP_PCIE_TX2P	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_TX2N	NC_SOC_GP_PCIE_TX2N	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_CLK2_100MP	NC_SOC_GP_PCIE_CLK2_100MP	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_CLK2_100MN	NC_SOC_GP_PCIE_CLK2_100MN	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_CLKREQ_2_L	NC_SOC_GP_PCIE_CLKREQ_2_L	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_PERST_2_L	NC_SOC_GP_PCIE_PERST_2_L	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_RX3P	NC_SOC_GP_PCIE_RX3P	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_RX3N	NC_SOC_GP_PCIE_RX3N	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_TX3P	NC_SOC_GP_PCIE_TX3P	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_TX3N	NC_SOC_GP_PCIE_TX3N	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_CLK3_100MP	NC_SOC_GP_PCIE_CLK3_100MP	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_CLK3_100MN	NC_SOC_GP_PCIE_CLK3_100MN	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_CLKREQ_3_L	NC_SOC_GP_PCIE_CLKREQ_3_L	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_PERST_3_L	NC_SOC_GP_PCIE_PERST_3_L	MAKE_BASE=TRUE

B DISP ALIAS

9	NC_I2C_SD_DISP_BKLT_SCL	NC_I2C_SD_DISP_BKLT_SCL	MAKE_BASE=TRUE
9	NC_I2C_SD_DISP_BKLT_SDA	NC_I2C_SD_DISP_BKLT_SDA	MAKE_BASE=TRUE
10	I2C_DISP_BKLT_SCL	I2C_DISP_BKLT_SCL	MAKE_BASE=TRUE 49
10	I2C_DISP_BKLT_SDA	I2C_DISP_BKLT_SDA	MAKE_BASE=TRUE 49
10	NC_SPI_DISP_BKLT_CLK_R	NC_SPI_DISP_BKLT_CLK_R	MAKE_BASE=TRUE
10	NC_SPI_DISP_BKLT_CS_L	NC_SPI_DISP_BKLT_CS_L	MAKE_BASE=TRUE
10	NC_SPMI_DISP_BKLT_CLK	NC_SPMI_DISP_BKLT_CLK	MAKE_BASE=TRUE
10	NC_SPMI_DISP_BKLT_DATA	NC_SPMI_DISP_BKLT_DATA	MAKE_BASE=TRUE
10	NC_SOC_DISP_POL	NC_SOC_DISP_POL	MAKE_BASE=TRUE
10	NC_DISP_BKLT_FSYNC	NC_DISP_BKLT_FSYNC	MAKE_BASE=TRUE
75	DISP_BKLT_LSYNC	DISP_BKLT_LSYNC	MAKE_BASE=TRUE 10
10	NC_SOC_DISP_TOUCH_BSYNC_0	NC_SOC_DISP_TOUCH_BSYNC_0	MAKE_BASE=TRUE
10	NC_SOC_DISP_TOUCH_BSYNC_1	NC_SOC_DISP_TOUCH_BSYNC_1	MAKE_BASE=TRUE
10	NC_SOC_DISP_TOUCH_EB	NC_SOC_DISP_TOUCH_EB	MAKE_BASE=TRUE
10	NC_BKLT_BOOST_THROTTLE_L	NC_BKLT_BOOST_THROTTLE_L	MAKE_BASE=TRUE
10	NC_SOC_DFR_DISP_TE	NC_SOC_DFR_DISP_TE	MAKE_BASE=TRUE
77	NC_LCDBKLT_FET_DRV	NC_LCDBKLT_FET_DRV	MAKE_BASE=TRUE

D LPDP Aliases

10	NC_SOC_LPDP_DP2HDMI_RCAL_POS	NC_SOC_LPDP_DP2HDMI_RCAL_POS	MAKE_BASE=TRUE
10	NC_SOC_LPDP_DP2HDMI_RCAL_NEG	NC_SOC_LPDP_DP2HDMI_RCAL_NEG	MAKE_BASE=TRUE

C Keyboard Backlight

9	SOC_KBD_BKLT_PWM	SOC_KBD_BKLT_PWM	MAKE_BASE=TRUE
85	SOC_KBD_BKLT_PWM		

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SOC: ALIASES PCIE, LPDP TX

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A SMC & NUB ALIAS

8	NC_SOC_SMC_GPIO_1	NC_SOC_SMC_GPIO_1	MAKE_BASE=TRUE
8	NC_SMC_FAN_0_PWM	NC_SMC_FAN_0_PWM	MAKE_BASE=TRUE
8	NC_SMC_FAN_0_TACH	NC_SMC_FAN_0_TACH	MAKE_BASE=TRUE
8	NC_SMC_FAN_1_PWM	NC_SMC_FAN_1_PWM	MAKE_BASE=TRUE
8	NC_SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	MAKE_BASE=TRUE
8	NC_SOC_NUB_CLK_OUT_0	NC_SOC_NUB_CLK_OUT_0	MAKE_BASE=TRUE
8	NC_SOC_NUB_GPIO_12	NC_SOC_NUB_GPIO_12	MAKE_BASE=TRUE
8	NC_ENET_LOW_PWR	NC_ENET_LOW_PWR	MAKE_BASE=TRUE
8	NC_LOM_PMU_RESET_EN	NC_LOM_PMU_RESET_EN	MAKE_BASE=TRUE

B SENSE ALIAS

14	VSNS_VDD_PCPU	VSNS_VDD_PCPU	MAKE_BASE=TRUE	55
14	VSNS_VSS_PCPU	VSNS_VSS_PCPU	MAKE_BASE=TRUE	55
14	VSNS_ABSMIN_PCPU	VSNS_ABSMIN_PCPU	MAKE_BASE=TRUE	55
15	VSNS_VDD_ECPU	VSNS_VDD_ECPU	MAKE_BASE=TRUE	55
17	VSNS_VDD_GPU	VSNS_VDD_GPU	MAKE_BASE=TRUE	55
15	VSNS_VDD_SOC	VSNS_VDD_SOC	MAKE_BASE=TRUE	55
17	VSNS_VDD_DISP	VSNS_VDD_DISP	MAKE_BASE=TRUE	55
18	VSNS_VDD2H_1	VSNS_VDD2H_1	MAKE_BASE=TRUE	55
18	VSNS_VSS_1	VSNS_VSS_1	MAKE_BASE=TRUE	55
18	VSNS_VDD2H_2	VSNS_VDD2H_2	MAKE_BASE=TRUE	55
18	VSNS_VSS_2	VSNS_VSS_2	MAKE_BASE=TRUE	55
18	VSNS_VDDQ_S1	VSNS_VDDQ_S1	MAKE_BASE=TRUE	55

C ISP ALIAS

6	NC_SOC_ISP_GPIO_1	NC_SOC_ISP_GPIO_1	MAKE_BASE=TRUE
6	NC_SOC_ISP_GPIO_2	NC_SOC_ISP_GPIO_2	MAKE_BASE=TRUE
6	NC_SOC_ISP_GPIO_3	NC_SOC_ISP_GPIO_3	MAKE_BASE=TRUE
6	NC_SOC_ISP_SPMI0_SCLK	NC_SOC_ISP_SPMI0_SCLK	MAKE_BASE=TRUE
6	NC_SOC_ISP_SPMI0_SDATA	NC_SOC_ISP_SPMI0_SDATA	MAKE_BASE=TRUE
6	NC_SOC_ISP_SPMI1_SCLK	NC_SOC_ISP_SPMI1_SCLK	MAKE_BASE=TRUE
6	NC_SOC_ISP_SPMI1_SDATA	NC_SOC_ISP_SPMI1_SDATA	MAKE_BASE=TRUE
6	NC_SOC_ISP_I2C1_SCL	NC_SOC_ISP_I2C1_SCL	MAKE_BASE=TRUE
6	NC_SOC_ISP_I2C1_SDA	NC_SOC_ISP_I2C1_SDA	MAKE_BASE=TRUE
6	NC_SOC_SENSOR0_CLK	NC_SOC_SENSOR0_CLK	MAKE_BASE=TRUE
6	NC_SOC_SENSOR1_CLK	NC_SOC_SENSOR1_CLK	MAKE_BASE=TRUE
6	NC_SOC_SENSOR2_CLK	NC_SOC_SENSOR2_CLK	MAKE_BASE=TRUE
6	NC_SOC_SENSOR3_CLK	NC_SOC_SENSOR3_CLK	MAKE_BASE=TRUE

D MIPI Aliases

6	NC_SOC_MIPI0C_DPCLK	NC_SOC_MIPI0C_DPCLK	MAKE_BASE=TRUE
6	NC_SOC_MIPI0C_DNCLK	NC_SOC_MIPI0C_DNCLK	MAKE_BASE=TRUE
6	NC_SOC_MIPI0C_DPDATA<0>	NC_SOC_MIPI0C_DPDATA<0>	MAKE_BASE=TRUE
6	NC_SOC_MIPI0C_DNDATA<0>	NC_SOC_MIPI0C_DNDATA<0>	MAKE_BASE=TRUE
6	NC_SOC_MIPI0C_DPDATA<1>	NC_SOC_MIPI0C_DPDATA<1>	MAKE_BASE=TRUE
6	NC_SOC_MIPI0C_DNDATA<1>	NC_SOC_MIPI0C_DNDATA<1>	MAKE_BASE=TRUE
6	NC_SOC_MIPI1C_DPCLK	NC_SOC_MIPI1C_DPCLK	MAKE_BASE=TRUE
6	NC_SOC_MIPI1C_DNCLK	NC_SOC_MIPI1C_DNCLK	MAKE_BASE=TRUE
6	NC_SOC_MIPI1C_DPDATA<0>	NC_SOC_MIPI1C_DPDATA<0>	MAKE_BASE=TRUE
6	NC_SOC_MIPI1C_DNDATA<0>	NC_SOC_MIPI1C_DNDATA<0>	MAKE_BASE=TRUE
6	NC_SOC_MIPI1C_DPDATA<1>	NC_SOC_MIPI1C_DPDATA<1>	MAKE_BASE=TRUE
6	NC_SOC_MIPI1C_DNDATA<1>	NC_SOC_MIPI1C_DNDATA<1>	MAKE_BASE=TRUE
6	NC_SOC_MIPID_DPCLK	NC_SOC_MIPID_DPCLK	MAKE_BASE=TRUE
6	NC_SOC_MIPID_DNCLK	NC_SOC_MIPID_DNCLK	MAKE_BASE=TRUE
6	NC_SOC_MIPID_DPDATA<0>	NC_SOC_MIPID_DPDATA<0>	MAKE_BASE=TRUE
6	NC_SOC_MIPID_DNDATA<0>	NC_SOC_MIPID_DNDATA<0>	MAKE_BASE=TRUE
6	NC_SOC_MIPI0C_REXT	NC_SOC_MIPI0C_REXT	MAKE_BASE=TRUE
6	NC_SOC_MIPI1C_REXT	NC_SOC_MIPI1C_REXT	MAKE_BASE=TRUE
6	NC_SOC_MIPID_REXT	NC_SOC_MIPID_REXT	MAKE_BASE=TRUE

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SOC: ALIASES CAMERA, USB, MISC

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SCSET RULES

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_(N)X Calculates dielectric distance from stackup, shortest distance is used unless 'L'is defined	EXAMPLE: 1,3-5,7L,8L-10L 2-10
A_DIELECTRIC_(N)XD XV,XVL,X Calculates dielectric distance from Hybrid Table and stackup, shortest distance is used unless 'L' defined	EXAMPLE: 2,1DL,3D-5D,7V,8VL-10VL PLEASE USE HYBRID TABLE
A_DIELECTRIC_(N)XIN_(N)XOUT Calculates dielectric distance from stackup, shortest distance is used unless 'L' is defined	EXAMPLE: 2_4,3L_5L

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17.4 RULES

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PHYSICAL CONSTRAINT SET, CLASS ASSIGNMENT

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	DOMAIN E,P,S	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
I2C	P	A_45_OHM_SE	*SMB*SCL*,*SMB*SDA*,*I2C*SCL*,*I2C*SDA*,*I2C*INT*	Y
SPI	P	A_45_OHM_SE	*SPI*MISO*,*SPI*MOSI*,*SPI*CLK*,*SPI*CS*	Y
SPMI	P	A_45_OHM_SE	*SPMI*	Y
SWD	P	A_45_OHM_SE	SWD_NAND*,SWD_NUB*	Y
JTAG	P	A_45_OHM_SE	*JTAG*SEL,*JTAG*TCK,*JTAG*TDI,*JTAG*TDO,*JTAG*TMS	Y
CLOCK_24M	P	A_45_OHM_SE	SOC_XTAL24M*,SOC_24M_O_R,NAND0_CLK24M*	Y
CLOCK_32K	P	A_45_OHM_SE	PMU_CLK32K*	Y
TDM_LEFT	P	A_45_OHM_SE	TDM_SPKRAMP_L*	Y
TDM_RIGHT	P	A_45_OHM_SE	TDM_SPKRAMP_R*	Y
TDM_CODEC	P	A_45_OHM_SE	TDM_CODEC*	Y
SPKR_ICC	P	A_45_OHM_SE	SPKRAMP_ICC,SPKRAMP_*_ICC_R	Y
UART	P	A_45_OHM_SE	UART_*	Y
RESETS	P	A_45_OHM_SE	*RST*,*RESET*,*PERST*	Y
WDOG	P	A_45_OHM_SE	SOC_WDOG	Y
SOCHOT	P	A_45_OHM_SE	SOC_SOCHOT_L	Y
POWER_BUTTON	P	A_45_OHM_SE	*PMU_ONOFF*	Y
FAULT	P	A_45_OHM_SE	*FAULT*	Y
DMIC_PDM	P	A_45_OHM_SE	PDM_DMIC_DATA*,DMIC_DATA*,PDM_DMIC_CLK*,DMIC_CLK*	Y
CIO_D2R	P	A_85_OHM_DIFF	DP:DP_USBC*_D2R*	Y
CIO_R2D	P	A_85_OHM_DIFF	DP:DP_USBC*_R2D*	Y
PCIE_NAND_D2R	P	A_85_OHM_DIFF	DP:DP_PCIE_NAND*_D2R*	Y
PCIE_NAND_R2D	P	A_85_OHM_DIFF	DP:DP_PCIE_NAND*_R2D*	Y
PCIE_WLBT_D2R	P	A_85_OHM_DIFF	DP:DP_PCIE_WLBT*_R2D*	Y
PCIE_WLBT_R2D	P	A_85_OHM_DIFF	DP:DP_PCIE_WLBT*_D2R*	Y
LPDP	P	A_85_OHM_DIFF	DP:DP_LPDP_INT_DATA*	Y
LPDP_FTCAM	P	A_85_OHM_DIFF	DP:DP_LPDP_FTCAM_DATA*	Y
PCIE_CLK	P	A_85_OHM_DIFF	DP:DP_PCIE_CLK100M*	Y
PCIE_CLKREQ	P	A_45_OHM_SE	*CLKREQ*	Y
EUSB	P	A_85_OHM_DIFF	DP:DP_EUSB*	Y
GROUND	P	DEFAULT	GND	Y
POWER	P	POWER	PP*,PN*	Y

PHYSICAL CONSTRAINT SET, NET ASSIGNMENT

DOMAIN (E,P,S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)

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SPACING CONSTRAINT SET, CLASS ASSIGNMENT

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	DOMAIN E,P,S	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
CLOCK_24M	S	A_DIELECTRIC_3X	=	Y
CLOCK_32K	S	A_DIELECTRIC_3X	=	Y
CIO_D2R	S	A_DIELECTRIC_9X	=	Y
CIO_R2D	S	A_DIELECTRIC_9X	=	Y
PCIE_NAND_D2R	S	A_DIELECTRIC_9X	=	Y
PCIE_NAND_R2D	S	A_DIELECTRIC_9X	=	Y
PCIE_WLBT_D2R	S	A_DIELECTRIC_7X	=	Y
PCIE_WLBT_R2D	S	A_DIELECTRIC_7X	=	Y
PCIE_CLK	S	A_DIELECTRIC_6X	=	Y
LPDP	S	A_DIELECTRIC_6X	=	Y
LPDP_FTCAM	S	A_DIELECTRIC_5X	=	Y
EUSB	S	A_DIELECTRIC_5X	=	Y
GROUND	S	DEFAULT	=	Y
POWER	S	DEFAULT	=	Y
RF	S	RF	RF_ANT*	Y

SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
CIO_D2R	GROUND	DEFAULT_WITH_4X_TO_SHAPE
CIO_R2D	GROUND	DEFAULT_WITH_4X_TO_SHAPE
LPDP	GROUND	DEFAULT_WITH_4X_TO_SHAPE
LPDP_FTCAM	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_CLK	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_D2R	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_R2D	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_D2R	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_R2D	GROUND	DEFAULT_WITH_4X_TO_SHAPE
CIO_D2R	POWER	DEFAULT_WITH_4X_TO_SHAPE
CIO_R2D	POWER	DEFAULT_WITH_4X_TO_SHAPE
LPDP	POWER	DEFAULT_WITH_4X_TO_SHAPE
LPDP_FTCAM	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_CLK	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_D2R	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_R2D	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_D2R	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_R2D	POWER	DEFAULT_WITH_4X_TO_SHAPE
CIO_D2R	CIO_D2R	A_DIELECTRIC_4X
CIO_D2R	PCIE_NAND_D2R	A_DIELECTRIC_4X
CIO_D2R	PCIE_WLBT_D2R	A_DIELECTRIC_4X
CIO_D2R	LPDP_FTCAM	A_DIELECTRIC_4X
CIO_D2R	CIO_R2D	A_DIELECTRIC_7X
PCIE_NAND_D2R	PCIE_NAND_D2R	A_DIELECTRIC_4X
PCIE_NAND_D2R	PCIE_WLBT_D2R	A_DIELECTRIC_4X
PCIE_NAND_D2R	LPDP_FTCAM	A_DIELECTRIC_4X
PCIE_NAND_D2R	PCIE_NAND_R2D	A_DIELECTRIC_7X
PCIE_WLBT_D2R	PCIE_WLBT_R2D	A_DIELECTRIC_4X
PCIE_WLBT_D2R	LPDP_FTCAM	A_DIELECTRIC_4X
CIO_R2D	CIO_R2D	A_DIELECTRIC_4X
CIO_R2D	PCIE_NAND_R2D	A_DIELECTRIC_4X
CIO_R2D	PCIE_WLBT_R2D	A_DIELECTRIC_4X
CIO_R2D	PCIE_CLK	A_DIELECTRIC_4X
CIO_R2D	LPDP	A_DIELECTRIC_4X
PCIE_NAND_R2D	PCIE_NAND_R2D	A_DIELECTRIC_4X
PCIE_NAND_R2D	PCIE_WLBT_R2D	A_DIELECTRIC_4X
PCIE_NAND_R2D	PCIE_CLK	A_DIELECTRIC_4X
PCIE_NAND_R2D	LPDP	A_DIELECTRIC_4X
PCIE_WLBT_R2D	PCIE_CLK	A_DIELECTRIC_4X
PCIE_WLBT_R2D	LPDP	A_DIELECTRIC_4X
PCIE_CLK	PCIE_CLK	A_DIELECTRIC_4X
PCIE_CLK	LPDP	A_DIELECTRIC_4X
LPDP	LPDP	A_DIELECTRIC_3X
LPDP_FTCAM	LPDP_FTCAM	A_DIELECTRIC_3X

LPDP	LPDP	A_DIELECTRIC_3X
LPDP_FTCAM	LPDP_FTCAM	A_DIELECTRIC_3X

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SOC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
939-11077	1	PCBA,CORBETT,X2203	U0600	CRITICAL	CPU:INTERPOSER
998-23363	1	IC,DEV,STA,BGA	U0600	CRITICAL	CPU:DEV

B0 BEST

998-26981	1	SOC,STA B0+8G,1Y,10FSTP,LP,BX,H,M2565		U0600	CRITICAL	CPU:SOC_8GB_BEST
998-26978	998-26981	ALT_CMN	ALL	Micron ATK/SCK/ASE		
998-26982	1	SOC,STA B0+16G,1Y,10FSTP,LP,BX,H,M2565		U0600	CRITICAL	CPU: SOC_16GB_BEST
998-26979	998-26982	ALT_CMN	ALL	Micron ATK/SCK/ASE		
998-26984	1	SOC,STA B0+24G,1Z,10FSTP,LP,BX,H,M2565		U0600	CRITICAL	CPU: SOC_24GB_BEST
998-26980	998-26984	ALT_CMN	ALL	Micron ATK/SCK/ASE		

B0 GOOD

998-26988	1	SOC,STA B0+8G,1Y,9FSTP,AP,BX,H,M2565		U0600	CRITICAL	CPU: SOC_8GB_GOOD
998-26985	998-26988	ALT_CMN	ALL	Micron ATK/SCK/ASE		
998-26981	998-26988	ALT_CMN	ALL	Hynix ATK/SCK/ASE - BEST		
998-26978	998-26988	ALT_CMN	ALL	Micron ATK/SCK/ASE - BEST		
998-26989	1	SOC,STA B0+16G,1Y,9FSTP,AP,BX,H,M2565		U0600	CRITICAL	CPU:SOC_16GB_GOOD
998-26986	998-26989	ALT_CMN	ALL	Micron ATK/SCK/ASE		
998-26982	998-26989	ALT_CMN	ALL	Hynix ATK/SCK/ASE - BEST		
998-26979	998-26989	ALT_CMN	ALL	Micron ATK/SCK/ASE - BEST		
998-26990	1	SOC,STA B0+24G,1Z,9FSTP,AP,BX,H,M2565		U0600	CRITICAL	CPU:SOC_24GB_GOOD
998-26987	998-26990	ALT_CMN	ALL	Micron ATK/SCK/ASE		

A1 BEST

998-25075	1	SOC,STA A0+8G,1Y,10C,DEV,BX,H,ATK,M2565		U0600	CRITICAL	CPU:SOC_8GB_BEST_A1
998-25074	998-25075	ALT_CMN	ALL	Hynix SCK		
998-25076	998-25075	ALT_CMN	ALL	Hynix ASE		
998-25077	998-25075	ALT_CMN	ALL	Micron SCK		
998-25078	998-25075	ALT_CMN	ALL	Micron ATK		
998-25079	998-25075	ALT_CMN	ALL	Micron ASE		
998-25081	1	SOC,STA A0+16G,1Y,10C,DEV,BX,H,ATK,M2565		U0600	CRITICAL	CPU: SOC_16GB_BEST_A1
998-25080	998-25081	ALT_CMN	ALL	Hynix SCK		
998-25082	998-25081	ALT_CMN	ALL	Hynix ASE		
998-25083	998-25081	ALT_CMN	ALL	Micron SCK		
998-25084	998-25081	ALT_CMN	ALL	Micron ATK		
998-25085	998-25081	ALT_CMN	ALL	Micron ASE		

A1 GOOD

998-25087	1	SOC,STA A0+8G,1Y,9C,DEV,BX,H,ATK,M2565		U0600	CRITICAL	CPU: SOC_8GB_GOOD_A1
998-25086	998-25087	ALT_CMN	ALL	Hynix SCK		
998-25088	998-25087	ALT_CMN	ALL	Hynix ASE		
998-25089	998-25087	ALT_CMN	ALL	Micron SCK		
998-25090	998-25087	ALT_CMN	ALL	Micron ATK		
998-25091	998-25087	ALT_CMN	ALL	Micron ASE		
998-25075	998-25087	ALT_CMN	ALL	Hynix ATK - BEST		
998-25074	998-25087	ALT_CMN	ALL	Hynix SCK - BEST		
998-25076	998-25087	ALT_CMN	ALL	Hynix ASE - BEST		
998-25077	998-25087	ALT_CMN	ALL	Micron SCK - BEST		
998-25078	998-25087	ALT_CMN	ALL	Micron ATK - BEST		
998-25079	998-25087	ALT_CMN	ALL	Micron ASE - BEST		
998-25093	1	SOC,STA A0+16G,1Y,9C,DEV,BX,H,ATK,M2565		U0600	CRITICAL	CPU:SOC_16GB_GOOD_A1
998-25092	998-25093	ALT_CMN	ALL	Hynix SCK		
998-25094	998-25093	ALT_CMN	ALL	Hynix ASE		
998-25095	998-25093	ALT_CMN	ALL	Micron SCK		
998-25096	998-25093	ALT_CMN	ALL	Micron ATK		
998-25097	998-25093	ALT_CMN	ALL	Micron ASE		
998-25081	998-25093	ALT_CMN	ALL	Hynix ATK - BEST		
998-25080	998-25093	ALT_CMN	ALL	Hynix SCK - BEST		
998-25082	998-25093	ALT_CMN	ALL	Hynix ASE - BEST		
998-25083	998-25093	ALT_CMN	ALL	Micron SCK - BEST		
998-25084	998-25093	ALT_CMN	ALL	Micron ATK - BEST		
998-25085	998-25093	ALT_CMN	ALL	Micron ASE - BEST		

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NAND BOM GROUPS

BOM GROUP	BOM OPTIONS
NANDCFG:ITLC_S5E_128G_TO	NAND_L0:ITLC_128G_TO
NANDCFG:ITLC_S5E_128G_SD	NAND_L0:ITLC_128G_SD
NANDCFG:ITLC_S5E_256G_HY	NAND_L0:ITLC_256G_HY
NANDCFG:ITLC_S5E_256G_SD	NAND_L0:ITLC_256G_SD
NANDCFG:ITLC_S5E_256G_TO	NAND_L0:ITLC_256G_TO
NANDCFG:ITLC_S5E_512G_SD	NAND_L0:ITLC_512G_SD,NAND_L1:ITLC_512G_SD,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_512G_TO	NAND_L0:ITLC_512G_TO,NAND_L1:ITLC_512G_TO,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_512G_HY	NAND_L0:ITLC_512G_HY,NAND_L1:ITLC_512G_HY,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_1P0T_HY	NAND_L0:ITLC_1P0T_HY,NAND_L1:ITLC_1P0T_HY,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_1P0T_TO	NAND_L0:ITLC_1P0T_TO,NAND_L1:ITLC_1P0T_TO,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_2P0T_TO	NAND_L0:ITLC_2P0T_TO,NAND_L1:ITLC_2P0T_TO,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_2P0T_HY	NAND_L0:ITLC_2P0T_HY,NAND_L1:ITLC_2P0T_HY,PARTS_SSDNAND1
NANDCFG:INTERPOSER	NAND_L0:INTERPOSER,NAND_L1:INTERPOSER,PARTS_SSDNAND1
NANDCFG:NONE	NAND_L0:OFF,NAND_L1:OFF,PARTS_SSDNAND1

NAND Landing 0

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-18368	1	IC,NAND,S5E MCP ROUTING STUDY,LGA110	UN000	CRITICAL	NAND_L0:S5E_STUDY
335S00462	1	NAND,3DV4,128GBT,XXX,S5E,256G,T,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_128G_TO
335S00470	1	NAND,3DV4,128GBT,XXX,S5E,256G,SD,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_128G_SD
335S00504	1	NAND,3DV6T,256GB,S5E,XX.X,512G,H,LGA110	UN000	CRITICAL	NAND_L0:ITLC_256G_HY
335S00531	1	NAND,BICS5T,256GB,S5E,XX.X,512G,W,LGA110	UN000	CRITICAL	NAND_L0:ITLC_256G_SD
335S00517	1	NAND,BICS5T,256GB,S5E,XX.X,512G,K,LGA110	UN000	CRITICAL	NAND_L0:ITLC_256G_TO
335S00532	1	NAND,BICS5T,320GB,S5E,XX.X,512G,W,LGA110	UN000	CRITICAL	NAND_L0:ITLC_512G_SD
335S00518	1	NAND,BICS5T,320GB,S5E,XX.X,512G,K,LGA110	UN000	CRITICAL	NAND_L0:ITLC_512G_TO
335S00504	1	NAND,3D6T,256GB,S5E,XX.X,512G,H,LGA110	UN000	CRITICAL	NAND_L0:ITLC_512G_HY
335S00506	1	NAND,3DV6T,512GB,S5E,XX.X,512G,H,LGA110	UN000	CRITICAL	NAND_L0:ITLC_1P0T_HY
335S00519	1	NAND,BICS5T,512GB,S5E,XX.X,512G,K,LGA110	UN000	CRITICAL	NAND_L0:ITLC_1P0T_TO
335S00521	1	NAND,BICS5T,1TB,S5E,XX.X,512G,K,LGA110	UN000	CRITICAL	NAND_L0:ITLC_2P0T_TO
335S00508	1	NAND,3DV6T,1TB,S5E,XX.X,512G,H,LGA110	UN000	CRITICAL	NAND_L0:ITLC_2P0T_HY
939-08815	1	PCBA,BANDIPUR,X1711	UN000	CRITICAL	NAND_L0:INTERPOSER

NAND Landing 1

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-18368	1	IC,NAND,S5E MCP ROUTING STUDY,LGA110	UN100	CRITICAL	NAND_L1:S5E_STUDY
335S00531	1	NAND,BICS5T,256GB,S5E,XX.X,512G,W,LGA110	UN100	CRITICAL	NAND_L1:ITLC_512G_SD
335S00517	1	NAND,BICS5T,256GB,S5E,XX.X,512G,K,LGA110	UN100	CRITICAL	NAND_L1:ITLC_512G_TO
335S00504	1	NAND,3D6T,256GB,S5E,XX.X,512G,H,LGA110	UN100	CRITICAL	NAND_L1:ITLC_512G_HY
335S00506	1	NAND,3DV6T,512GB,S5E,XX.X,512G,H,LGA110	UN100	CRITICAL	NAND_L1:ITLC_1P0T_HY
335S00519	1	NAND,BICS5T,512GB,S5E,XX.X,512G,K,LGA110	UN100	CRITICAL	NAND_L1:ITLC_1P0T_TO
335S00521	1	NAND,BICS5T,1TB,S5E,XX.X,512G,K,LGA110	UN100	CRITICAL	NAND_L1:ITLC_2P0T_TO
335S00508	1	NAND,3DV6T,1TB,S5E,XX.X,512G,H,LGA110	UN100	CRITICAL	NAND_L1:ITLC_2P0T_HY
939-08815	1	PCBA,BANDIPUR,X1711	UN100	CRITICAL	NAND_L1:INTERPOSER

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A Module Parts

RT13 Retimer

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-21959	2	IC,LIFUKA,A0,USB-C RETIMER,FCCSP154	UF000,UF100	CRITICAL	ATCRTMR:A0
998-25504	2	IC,LIFUKA,B0,USB-C RETIMER,DEV,CSP154	UF000,UF100	CRITICAL	ATCRTMR:B0

Ace2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02158	3	IC,CD3217,ACE2,B2,USB PWR SW W/HV,BGA123	UF400,UF500,U5500	CRITICAL	USBCPC:LAPTOP_B2_PPO
353S02742	3	IC,CD3217,ACE2,B2,USB PWR SW W/HV,BGA123	UF400,UF500,U5500	CRITICAL	USBCPC:LAPTOP_B2
353S02993	3	IC,ACE2,B3,USB PWR SW W/HV,RDR3,BGA123	UF400,UF500,U5500	CRITICAL	USBCPC:LAPTOP_B3

eUSB Level Shifter

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00628	2	IC,PARROT,CD2E226B,B0 LSB1,OTP-6,CSP25	UF600,UF650	CRITICAL	EUSB_LS:B0

Re-timer Sequencer

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S00483	2	IC,SLG4AP44593,PWR RAIL SEQUENCER,QFN8	UF790	CRITICAL	

SECURE ELEMENT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00629	1	IC,SN210V,B1,CERES,DEV,VER=LN,WLCSP81	U5000	CRITICAL	SE:DEV_SW_LN
338S00630	1	IC,SN210V,B1,CERES,PROD,VER=MU,WLCSP81	U5000	CRITICAL	SE:PROD_SW_MU

B Programmable Parts

USBC ACE2 ROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	UF260	CRITICAL	UPC01_ROM:BLANK

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00537	335S00133	UPC01_ROM:BLANK	UF260	rdar://80303180
335S00570	335S00133	UPC01_ROM:BLANK	UF260	rdar://80303180
335S00571	335S00133	UPC01_ROM:BLANK	UF260	rdar://80303180

341S01912	1	ROM,ACE-P01 (V2.112.0.5) PROTO-0,X2203	UF260	CRITICAL	UPC01_ROM:P0
341S01998	1	ROM,ACE-P01 (V2.116.0.5) PROTO-2,X2203	UF260	CRITICAL	UPC01_ROM:P2
341S02052	1	Description: ROM,ACE-P01 (V2.131.3.6) EVT,X2203	UF260	CRITICAL	UPC01_ROM:EVT

MagSafe ACE2 ROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	U5560	CRITICAL	UPC5_ROM:BLANK

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00537	335S00133	UPC5_ROM:BLANK	U5560	rdar://80303078
335S00570	335S00133	UPC5_ROM:BLANK	U5560	rdar://80303078
335S00571	335S00133	UPC5_ROM:BLANK	U5560	rdar://80303078

341S01913	1	ROM,ACE-P5 (V2.112.0.3) PROTO-0,X2203	U5560	CRITICAL	UPC5_ROM:P0
341S01999	1	ROM,ACE-P5 (V2.116.0.3) PROTO-2,X2203	U5560	CRITICAL	UPC5_ROM:P2
341S02053	1	ROM,ACE-P5 (V2.131.3.6) EVT,X2203	U5560	CRITICAL	UPC5_ROM:EVT

SOC ROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-22994	1	IC,FLASH,64MBIT,1.2V,QE=1,M,4X4MM,SON8	U1900	CRITICAL	SOC_ROM:BLANK_P1
335S00575	1	IC,FLASH,64MBIT,1.2V,QE=1,M,4X4MM,SON8	U1900	CRITICAL	SOC_ROM:BLANK

RT13 ROM(s)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-22993	2	IC,FLASH,64MBIT,1.2V,QE=1,M,4X4MM,SON8	UF890,UF190	CRITICAL	RT13_ROM:BLANK_P1
335S00574	2	IC,FLASH,64MBIT,1.2V,QE=1,M,4X4MM,SON8	UF090,UF190	CRITICAL	RT13_ROM:BLANK

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00575	335S00574	RT13_ROM:BLANK	UF090,UF190	rdar://76779010

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SPMU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-23585	1	IC,PMU,VALE,CSP196	U7700	CRITICAL	SPMU_IC:DEV
998-24583	1	IC,PMU,VALE,A0,OTP-JPC,CSP196	U7700	CRITICAL	SPMU_IC:A0_JPC
998-25434	1	IC,PMU,VALE,A0,OTP-JPD,WLCSP196	U7700	CRITICAL	SPMU_IC:A0_JPD
998-26179	1	IC,PMU,VALE,A0,OTP-JPE,WLCSP196	U7700	CRITICAL	SPMU_IC:A0_JPE
998-26198	1	IC,PMU,VALE,A0,OTP-JPF,WLCSP196	U7700	CRITICAL	SPMU_IC:A0_JPF
998-26683	1	IC,PMU,VALE,A0,OTP-JPG,WLCSP196	U7700	CRITICAL	SPMU_IC:A0_JPG
998-26878	1	IC,PMU,VALE,A0,OTP-JPH,WLCSP196	U7700	CRITICAL	SPMU_IC:A0_JPH
998-27502	1	IC,PMU,VALE,A0,OTP-JPI,WLCSP196	U7700	CRITICAL	SPMU_IC:A0_JPI

MPMU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-23524	1	IC,PMU,STOWE,CSP420	U8100	CRITICAL	MPMU_IC:DEV
998-24581	1	IC,PMU,STOWE,A0,OTP-JPC,CSP420	U8100	CRITICAL	MPMU_IC:A0_JPC
998-25433	1	IC,PMU,STOWE,A0,OTP-JPD,WLCSP420	U8100	CRITICAL	MPMU_IC:A0_JPD
998-26178	1	IC,PMU,STOWE,A0,OTP-JPE,WLCSP420	U8100	CRITICAL	MPMU_IC:A0_JPE
998-26197	1	IC,PMU,STOWE,A0,OTP-JPF,WLCSP420	U8100	CRITICAL	MPMU_IC:A0_JPF
998-26682	1	IC,PMU,STOWE,A0,OTP-JPG,WLCSP420	U8100	CRITICAL	MPMU_IC:A0_JPG
998-26877	1	IC,PMU,STOWE,A0,OTP-JPH,WLCSP420	U8100	CRITICAL	MPMU_IC:A0_JPH
998-27501	1	IC,PMU,STOWE,A0,OTP-JPI,WLCSP420	U8100	CRITICAL	MPMU_IC:A0_JPI

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Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0846	138S0811	ALT_CMN	ALL	rdar://problem/59474499
376S1053	376S0604	ALT_CMN	ALL	rdar://problem/59475163
740S00041	740S0159	ALT_CMN	ALL	rdar://problem/59438907
107S00033	107S00034	ALT_CMN	ALL	rdar://problem/59471007
376S0948	376S00076	ALT_CMN	ALL	rdar://problem/59134310
128S00031	128S00011	ALT_CMN	ALL	rdar://problem/73938832
128S00026	128S00011	ALT_CMN	ALL	rdar://problem/73938832
128S00087	128S00011	ALT_CMN	ALL	rdar://problem/73938832
376S00228	376S1179	ALT_CMN	ALL	rdar://problem/73939839
376S00007	376S1179	ALT_CMN	ALL	rdar://problem/73939839
376S1147	376S00281	ALT_CMN	ALL	rdar://problem/73940207
107S00029	107S00087	ALT_CMN	ALL	rdar://problem/73982640
138S00332	138S00328	ALT_CMN	ALL	rdar://problem/74145755
138S0863	138S1058	ALT_CMN	ALL	rdar://problem/74148337
138S00229	138S00107	ALT_CMN	ALL	rdar://problem/74148104
138S00022	138S0801	ALT_CMN	ALL	rdar://problem/74146716
152S00398	152S00204	ALT_CMN	ALL	rdar://problem/73959393
152S01317	152S01268	ALT_CMN	ALL	rdar://problem/73958701
152S00997	152S00476	ALT_CMN	ALL	rdar://problem/73957803
107S00055	107S00090	ALT_CMN	ALL	rdar://problem/73982769
138S00181	138S0835	ALT_CMN	ALL	rdar://problem/74150148
138S00291	138S0835	ALT_CMN	ALL	rdar://problem/74150148
377S00166	377S00160	ALT_CMN	ALL	rdar://problem/59407974
138S00330	138S00081	ALT_CMN	ALL	rdar://problem/74146122
377S00123	377S00031	ALT_CMN	ALL	rdar://problem/59407768
377S00186	377S00060	ALT_CMN	ALL	rdar://problem/59407847
311S00230	311S00212	ALT_CMN	ALL	rdar://problem/71866385
138S0771	138S00336	ALT_CMN	ALL	rdar://problem/71832350
138S00343	138S00329	ALT_CMN	ALL	rdar://problem/71832255
107S00076	107S00044	ALT_CMN	ALL	rdar://problem/71831138
138S00151	138S00149	ALT_CMN	ALL	rdar://problem/71832189
138S00150	138S00149	ALT_CMN	ALL	rdar://problem/71832189
138S00148	138S00149	ALT_CMN	ALL	rdar://problem/71832189
107S00365	107S00373	ALT_CMN	ALL	rdar://problem/71831414
132S00176	132S0640	ALT_CMN	ALL	rdar://problem/71831575
138S00164	138S00138	ALT_CMN	ALL	rdar://problem/71831667
138S00280	138S00138	ALT_CMN	ALL	rdar://problem/71831667
138S00139	138S00138	ALT_CMN	ALL	rdar://problem/71831667
138S00047	138S00073	ALT_CMN	ALL	rdar://problem/71831776
138S00097	138S0750	ALT_CMN	ALL	rdar://problem/74149037
155S00007	155S0667	ALT_CMN	ALL	rdar://problem/73218092
740S00081	740S00053	ALT_CMN	ALL	rdar://problem/73218321
377S00210	377S00172	ALT_CMN	ALL	rdar://problem/73218476
376S00292	376S1140	ALT_CMN	ALL	rdar://problem/73218568
376S00303	376S00012	ALT_CMN	ALL	rdar://problem/73218339
128S00106	128S00107	ALT_CMN	ALL	rdar://problem/73938270
128S00110	128S00107	ALT_CMN	ALL	rdar://problem/73938270
371S00220	371S00307	ALT_CMN	ALL	rdar://problem/73940785
152S00991	152S00984	ALT_CMN	ALL	rdar://problem/73958066
152S01378	152S01283	ALT_CMN	ALL	rdar://problem/80602206
152S01494	152S01263	ALT_CMN	ALL	rdar://problem/73957626
152S00979	152S00874	ALT_CMN	ALL	rdar://problem/73960389
311S00322	311S00321	ALT_CMN	ALL	rdar://problem/72334560
335S00232	335S00133	ALT_CMN	ALL	rdar://problem/73953460
138S00197	138S00409	ALT_CMN	ALL	rdar://problem/75264457
138S00413	138S00410	ALT_CMN	ALL	rdar://problem/75264676
376S00521	376S00519	ALT_CMN	ALL	rdar://problem/74496873
197S00318	197S00323	ALT_CMN	ALL	rdar://problem/75588335
197S00335	197S00323	ALT_CMN	ALL	rdar://problem/75588335

Alternate Vendor	Primary Vendor
Samsung	Murata
Diodes Inc	Fairchild
Bourns	LittelFuse
TFT	Cyntec
Diodes Inc	Toshiba
ROHM CORP	Kemet
NEC	Kemet
Panasonic	Kemet
Fairchild	Vishay
AOS	Vishay
On Semi	AOS
TFT	Yageo
Kyocera	Murata
Taiyo	Murata
Kyocera	Murata
Taiyo	Murata/Samsung
Taiyo	Cyntec
Taiyo	Cyntec
Chilisin	Murata
Cyntec	TFT
Samsung	Murata
Kyocera	Murata
Semtech	On Semi
SEMCO	Murata
Semtech	On Semi
Semtech	ST Micro
Nexperia	TI
Taiyo	Murata
Kyocera	Murata
Taiyo	Murata
Yageo	Cyntec
Taiyo	Murata
Kyocera	Murata
Samsung	Kyocera
Murata	Kyocera
Taiyo	Murata
Taiyo Yuden	Murata
Taiyo	Pansonic
Bourns	AEM
Semtech	TI
Nexperia	Diodes Inc
Diodes Inc	TI
Tokin	Kemet
Samsung	Kemet
On Semi	Diodes Inc
Taiyo	Cyntec
Microgate	Cyntec
Taiyo	Cyntec
Taiyo	Cyntec
Nexperia	TI
Macronix	Winbond
Murata	Taiyo
Murata	Taiyo
Vishay	On Semi
NDK	TXC
Kyocera	TXC

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
371S00085	371S00190	ALT_CMN	ALL	rdar://problem/59404601
311S00156	311S00129	ALT_CMN	ALL	rdar://problem/59489090
376S1080	376S0620	ALT_CMN	ALL	rdar://problem/59439026
311S00269	311S00234	ALT_CMN	ALL	rdar://problem/59489341
376S1128	376S00282	ALT_CMN	ALL	rdar://problem/73941008
376S00224	376S00282	ALT_CMN	ALL	rdar://problem/73941008
107S00101	107S00005	ALT_CMN	ALL	TBD
107S00102	107S00017	ALT_CMN	ALL	TBD
107S0276	107S00020	ALT_CMN	ALL	TBD
107S00370	107S00371	ALT_CMN	ALL	TBD
107S00372	107S00371	ALT_CMN	ALL	TBD
107S00298	107S00460	ALT_CMN	ALL	TBD
107S0150	107S00460	ALT_CMN	ALL	TBD
138S00284	138S00136	ALT_CMN	ALL	rdar://problem/74149755
138S0852	138S0818	ALT_CMN	ALL	TBD
155S0275	155S00188	ALT_CMN	ALL	TBD
155S0706	155S0302	ALT_CMN	ALL	TBD
155S0741	155S0361	ALT_CMN	ALL	TBD
155S0823	155S0644	ALT_CMN	ALL	TBD
311S00267	311S00244	ALT_CMN	ALL	TBD
311S00268	311S00246	ALT_CMN	ALL	TBD
152S01163	152S00136	ALT_CMN	ALL	Per Louisa Zhang
138S00031	138S0861	ALT_CMN	ALL	rdar://73954319
152S00810	152S01601	ALT_CMN	ALL	TBD
152S00809	152S00332	ALT_CMN	ALL	TBD
740S0118	740S00028	ALT_CMN	ALL	rdar://problem/74350704
740S0144	740S00028	ALT_CMN	ALL	rdar://problem/74350704
128S00094	128S00067	ALT_CMN	ALL	rdar://problem/73939352
128S00069	128S00067	ALT_CMN	ALL	rdar://problem/73939352
138S00385	138S00377	ALT_CMN	ALL	rdar://problem/73954116
152S01521	152S01459	ALT_CMN	ALL	rdar://problem/74521339
152S01520	152S01458	ALT_CMN	ALL	rdar://problem/74521392
152S01519	152S01457	ALT_CMN	ALL	rdar://problem/74521425
311S00317	311S00316	ALT_CMN	ALL	TBD
311S00272	311S00287	ALT_CMN	ALL	TBD
311S00336	311S0613	ALT_CMN	ALL	TBD
138S00416	138S00328	ALT_CMN	ALL	rdar://problem/74145755
138S00087	138S1086	ALT_CMN	ALL	TBD
376S00332	376S0855	ALT_CMN	ALL	rdar://problem/75989879
376S00074	376S0855	ALT_CMN	ALL	rdar://problem/75989879
197S0590	197S0591	ALT_CMN	ALL	rdar://problem/73953315
197S0588	197S0591	ALT_CMN	ALL	rdar://problem/73953315
311S0612	311S00263	ALT_CMN	ALL	rdar://problem/76165274
311S00057	311S00263	ALT_CMN	ALL	rdar://problem/76165274
152S01548	152S00289	ALT_CMN	ALL	rdar://problem/76165749
353S02402	353S1429	ALT_CMN	ALL	rdar://problem/76165876
371S00284	371S00187	ALT_CMN	ALL	rdar://problem/76171510
371S00240	371S00364	ALT_CMN	ALL	rdar://problem/76171942
376S00516	376S1112	ALT_CMN	ALL	rdar://problem/74046107
152S00343	152S01325	ALT_CMN	ALL	rdar://problem/78474169
107S00479	107S00478	ALT_CMN	ALL	rdar://problem/80035462
311S00352	311S00353	ALT_CMN	ALL	rdar://problem/80101244
138S1065	138S1058	ALT_CMN	ALL	rdar://problem/80325043
371S00205	371S00077	ALT_CMN	ALL	rdar://problem/80305372
107S00474	107S00017	ALT_CMN	ALL	rdar://problem/80289091
107S00475	107S00044	ALT_CMN	ALL	rdar://problem/71831138
107S00443	107S00005	ALT_CMN	ALL	rdar://80470921

Alternate Vendor	Primary Vendor
On Semi	Diodes Inc
Nexperia	TI
Diodes Inc	On Semi
Nexperia	TI
Diodes Inc	On Semi
Nexperia	On Semi
Yageo	Cyntec
Yageo	Cyntec
Cyntec	TFT
Yageo	Cyntec/Yageo
Vishay	Cyntec/Yageo
TDK	Murata
Panasonic	Murata
Kyocera	Murata
Samsung	Murata
Taiyo Yuden	Murata
Taiyo Yuden	Murata
Murata	TDK
TDK/Taiyo	Murata
Nexperia	TI
Nexperia	TI
Chilisin	Cyntec
Murata/Taiyo	Murata
Taiyo Yuden	Cyntec
Taiyo Yuden	Cyntec
Polytronics	Bussmann
LittelFuse	Bussman
Tokin/Kemet	Panasonic
Rohm	Panasonic
Kyocera	Murata
Chilisin	Cyntec
Chilisin	Cyntec
Chilisin	Cyntec
Nexperia	TI
Nexperia	TI
TI	NXP/Diodes
Taiyo Yuden	Murata
Taiyo Yuden	Murata
Nexperia	Diodes Inc
Toshiba	Diodes Inc
EPSON	NDK
TXC	NDK
NXP	TI
Diodes Inc	TI
Murata	Cyntec
On Semi	TI
NXP	On Semi
NXP	Diodes Inc.
On Semi	Diodes Inc.
Murata	Taiyo Yuden
Yageo	Cyntec
Nexperia	TI
Taiyo Yuden	Murata
Vishay	Nexperia
TFT	Cyntec
Yageo	Cyntec
TFT	Cyntec

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S00078	311S00275	ALT_CMN	ALL	rdar://80479617
311S00006	311S00323	ALT_CMN	ALL	rdar://72334608
152S01461	152S01283	ALT_CMN	ALL	rdar://80602206
104S00138	104S00135	ALT_CMN	ALL	rdar://80471945
371S00370	371S00062	ALT_CMN	ALL	rdar://80501286
311S00361	311S00362	ALT_CMN	ALL	rdar://81349317
311S00360	311S00362	ALT_CMN	ALL	rdar://81349317
116S00014	116S00044	ALT_CMN	ALL	rdar://80606250
311S00335	311S00155	ALT_CMN	ALL	rdar://82988239
376S0725	376S0604	ALT_CMN	ALL	rdar://82961072

Alternate Vendor	Primary Vendor
Nexperia	Ti
Nexperia	Ti
Sunlord	Cyntec
TFT	Cyntec/Yageo
Diodes	On Semi
Diodes	Ti
Nexperia	Ti
Cyntec/ROHM	TFT
Ti	Nexperia
Vishay	Fairchild

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EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
	685-00426	COMMON PARTS,MLB,X2203	MLB_COMMON,ALTERNATE:PART,ALT_CMN
	685-00427	PARTS,SSD NAND1,MLB,X2203	SSD_2L,ALTERNATE:PART,ALT_CMN
0VRW	939-10926	PCBA,MLB,DCDC,X2203	MLB_COMMON,DEV_PARTS_BOM,NANDCFG:INTERPOSER,CPU:INTERPOSER,ALTERNATE:PART,ALT_CMN
1620	939-11657	PCBA,MLB,RF-CHAR,X2203	RF_COMMON
	985-01536	DEV PARTS,MLB,X2203	MLB_DEV,ALTERNATE:PART,ALT_CMN

SOC (BEST), Hynix and Micron 8GB

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
0W89	639-15199	PCBA,MLB,BEST,SOC,M-8G,SD-128G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_SSE_128G_SD
0W8C	639-15200	PCBA,MLB,BEST,SOC,M-8G,TO-128G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_SSE_128G_TO
0W8H	639-15203	PCBA,MLB,BEST,SOC,M-8G,HY-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_SSE_256G_HY
0W8J	639-15204	PCBA,MLB,BEST,SOC,M-8G,SD-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_SSE_256G_SD
0W8K	639-15205	PCBA,MLB,BEST,SOC,M-8G,TO-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_SSE_256G_TO
0W8P	639-15209	PCBA,MLB,BEST,SOC,M-8G,SD-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_SSE_512G_SD
0W8Q	639-15210	PCBA,MLB,BEST,SOC,M-8G,TO-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_SSE_512G_TO
1JQJ	639-16109	PCBA,MLB,BEST,SOC,M-8G,HY-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_SSE_512G_HY
0W8V	639-15213	PCBA,MLB,BEST,SOC,M-8G,HY-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_SSE_1P0T_HY
0W8W	639-15214	PCBA,MLB,BEST,SOC,M-8G,TO-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_SSE_1P0T_TO
0W90	639-15217	PCBA,MLB,BEST,SOC,M-8G,HY-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_SSE_2P0T_HY
0W91	639-15218	PCBA,MLB,BEST,SOC,M-8G,TO-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_SSE_2P0T_TO

SOC (GOOD), Hynix and Micron 8GB

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
Q2D9	639-15221	PCBA,MLB,GOOD,SOC,M-8G,SD-128G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_SSE_128G_SD
Q2DC	639-15222	PCBA,MLB,GOOD,SOC,M-8G,TO-128G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_SSE_128G_TO
Q2DD	639-15225	PCBA,MLB,GOOD,SOC,M-8G,HY-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_SSE_256G_HY
Q2DF	639-15226	PCBA,MLB,GOOD,SOC,M-8G,SD-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_SSE_256G_SD
Q2DG	639-15227	PCBA,MLB,GOOD,SOC,M-8G,TO-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_SSE_256G_TO
Q2DH	639-15231	PCBA,MLB,GOOD,SOC,M-8G,SD-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_SSE_512G_SD
Q2DJ	639-15232	PCBA,MLB,GOOD,SOC,M-8G,TO-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_SSE_512G_TO
1JQK	639-16110	PCBA,MLB,GOOD,SOC,M-8G,HY-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_SSE_512G_HY
Q2DK	639-15235	PCBA,MLB,GOOD,SOC,M-8G,HY-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_SSE_1P0T_HY
Q2DL	639-15236	PCBA,MLB,GOOD,SOC,M-8G,TO-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_SSE_1P0T_TO
Q2DM	639-15239	PCBA,MLB,GOOD,SOC,M-8G,HY-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_SSE_2P0T_HY
Q2DN	639-15240	PCBA,MLB,GOOD,SOC,M-8G,TO-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_SSE_2P0T_TO

SOC (BEST), Hynix and Micron 16GB

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
0W8F	639-15201	PCBA,MLB,BEST,SOC,M-16G,SD-128G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_SSE_128G_SD
0W8G	639-15202	PCBA,MLB,BEST,SOC,M-16G,TO-128G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_SSE_128G_TO
0W8L	639-15206	PCBA,MLB,BEST,SOC,M-16G,HY-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_SSE_256G_HY
0W8M	639-15207	PCBA,MLB,BEST,SOC,M-16G,SD-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_SSE_256G_SD
0W8N	639-15208	PCBA,MLB,BEST,SOC,M-16G,TO-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_SSE_256G_TO
0W8R	639-15211	PCBA,MLB,BEST,SOC,M-16G,SD-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_SSE_512G_SD
0W8T	639-15212	PCBA,MLB,BEST,SOC,M-16G,TO-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_SSE_512G_TO
1JQL	639-16111	PCBA,MLB,BEST,SOC,M-16G,HY-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_SSE_512G_HY
0W8X	639-15215	PCBA,MLB,BEST,SOC,M-16G,HY-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_SSE_1P0T_HY
0W8Y	639-15216	PCBA,MLB,BEST,SOC,M-16G,TO-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_SSE_1P0T_TO
0W92	639-15219	PCBA,MLB,BEST,SOC,M-16G,HY-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_SSE_2P0T_HY
0W93	639-15220	PCBA,MLB,BEST,SOC,M-16G,TO-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_SSE_2P0T_TO

SOC (GOOD), Hynix and Micron 16GB

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
0W96	639-15223	PCBA,MLB,GOOD,SOC,M-16G,SD-128G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_SSE_128G_SD
0W97	639-15224	PCBA,MLB,GOOD,SOC,M-16G,TO-128G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_SSE_128G_TO
0W9D	639-15228	PCBA,MLB,GOOD,SOC,M-16G,HY-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_SSE_256G_HY
0W9F	639-15229	PCBA,MLB,GOOD,SOC,M-16G,SD-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_SSE_256G_SD
0W9G	639-15230	PCBA,MLB,GOOD,SOC,M-16G,TO-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_SSE_256G_TO
0W9K	639-15233	PCBA,MLB,GOOD,SOC,M-16G,SD-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_SSE_512G_SD
0W9L	639-15234	PCBA,MLB,GOOD,SOC,M-16G,TO-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_SSE_512G_TO
1JQM	639-16112	PCBA,MLB,GOOD,SOC,M-16G,HY-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_SSE_512G_HY
0W9P	639-15237	PCBA,MLB,GOOD,SOC,M-16G,HY-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_SSE_1P0T_HY
0W9Q	639-15238	PCBA,MLB,GOOD,SOC,M-16G,TO-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_SSE_1P0T_TO
0W9V	639-15241	PCBA,MLB,GOOD,SOC,M-16G,HY-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_SSE_2P0T_HY
0W9W	639-15242	PCBA,MLB,GOOD,SOC,M-16G,TO-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_SSE_2P0T_TO

SOC (BEST), Hynix and Micron 24GB

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
1MNQ	639-16519	PCBA,MLB,BEST,SOC,M-24G,HY-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_BEST,NANDCFG:ITLC_SSE_256G_HY
1MNP	639-16518	PCBA,MLB,BEST,SOC,M-24G,SD-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_BEST,NANDCFG:ITLC_SSE_256G_SD
1MPJ	639-16537	PCBA,MLB,BEST,SOC,M-24G,TO-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_BEST,NANDCFG:ITLC_SSE_256G_TO
1MNT	639-16521	PCBA,MLB,BEST,SOC,M-24G,SD-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_BEST,NANDCFG:ITLC_SSE_512G_SD
1MNV	639-16522	PCBA,MLB,BEST,SOC,M-24G,TO-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_BEST,NANDCFG:ITLC_SSE_512G_TO
1MNR	639-16520	PCBA,MLB,BEST,SOC,M-24G,HY-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_BEST,NANDCFG:ITLC_SSE_512G_HY
1MNW	639-16523	PCBA,MLB,BEST,SOC,M-24G,HY-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_BEST,NANDCFG:ITLC_SSE_1P0T_HY
1MNX	639-16524	PCBA,MLB,BEST,SOC,M-24G,TO-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_BEST,NANDCFG:ITLC_SSE_1P0T_TO
1MNY	639-16525	PCBA,MLB,BEST,SOC,M-24G,HY-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_BEST,NANDCFG:ITLC_SSE_2P0T_HY
1MP0	639-16526	PCBA,MLB,BEST,SOC,M-24G,TO-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_BEST,NANDCFG:ITLC_SSE_2P0T_TO

SOC (GOOD), Hynix and Micron 24GB

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
1MP1	639-16527	PCBA,MLB,GOOD,SOC,M-24G,HY-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_GOOD,NANDCFG:ITLC_SSE_256G_HY
1MP2	639-16528	PCBA,MLB,GOOD,SOC,M-24G,SD-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_GOOD,NANDCFG:ITLC_SSE_256G_SD
1MP3	639-16529	PCBA,MLB,GOOD,SOC,M-24G,TO-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_GOOD,NANDCFG:ITLC_SSE_256G_TO
1MP4	639-16530	PCBA,MLB,GOOD,SOC,M-24G,SD-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_GOOD,NANDCFG:ITLC_SSE_512G_SD
1MP5	639-16531	PCBA,MLB,GOOD,SOC,M-24G,TO-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_GOOD,NANDCFG:ITLC_SSE_512G_TO
1MP6	639-16532	PCBA,MLB,GOOD,SOC,M-24G,HY-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_GOOD,NANDCFG:ITLC_SSE_512G_HY
1MP7	639-16533	PCBA,MLB,GOOD,SOC,M-24G,HY-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_GOOD,NANDCFG:ITLC_SSE_1P0T_HY
1MP8	639-16534	PCBA,MLB,GOOD,SOC,M-24G,TO-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_GOOD,NANDCFG:ITLC_SSE_1P0T_TO
1MP9	639-16535	PCBA,MLB,GOOD,SOC,M-24G,HY-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_GOOD,NANDCFG:ITLC_SSE_2P0T_HY
1MPC	639-16536	PCBA,MLB,GOOD,SOC,M-24G,TO-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_GOOD,NANDCFG:ITLC_SSE_2P0T_TO

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