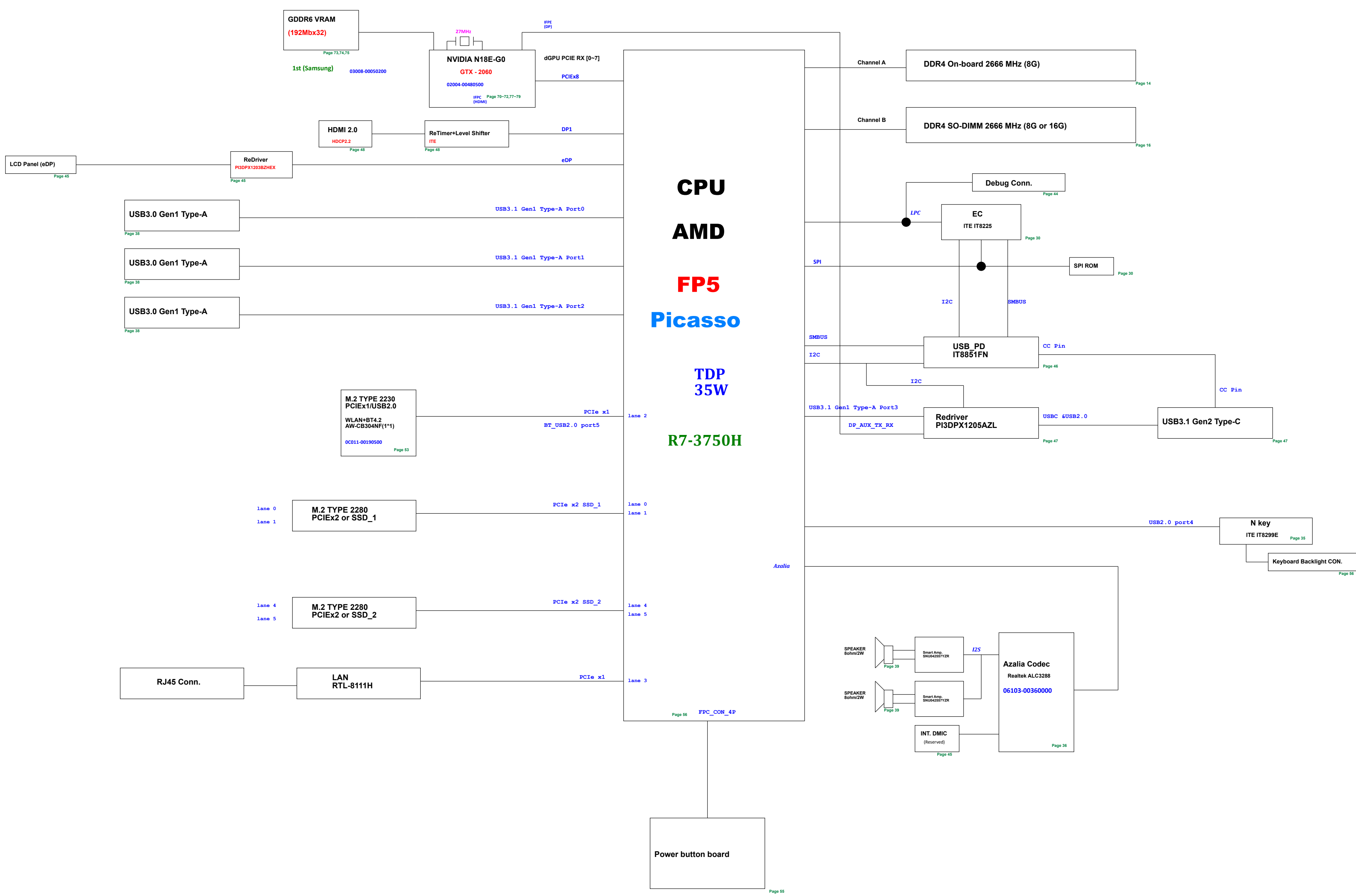
GA502DU AMD+NVIDIA Block Diagram



ASUS
Project Name: G703GI
Title : CFL-H_Block Diagram_R1.3B
Rev R1.0
Dept.: ASUSTeK COMPUTER INC.
Engineer: NB1 RD2 EE1
Date: Monday, April 29, 2019
Sheet 1 of 104

PCIE/WLAN/LAN/SSD

APU: change 01002-01170700 to 01002-01250200
@20181022F

Follow FX505DY, SR先用0201
@20181018J

RX Side

Rename to PCIENB RX [0-7]
20180928B

TX Side

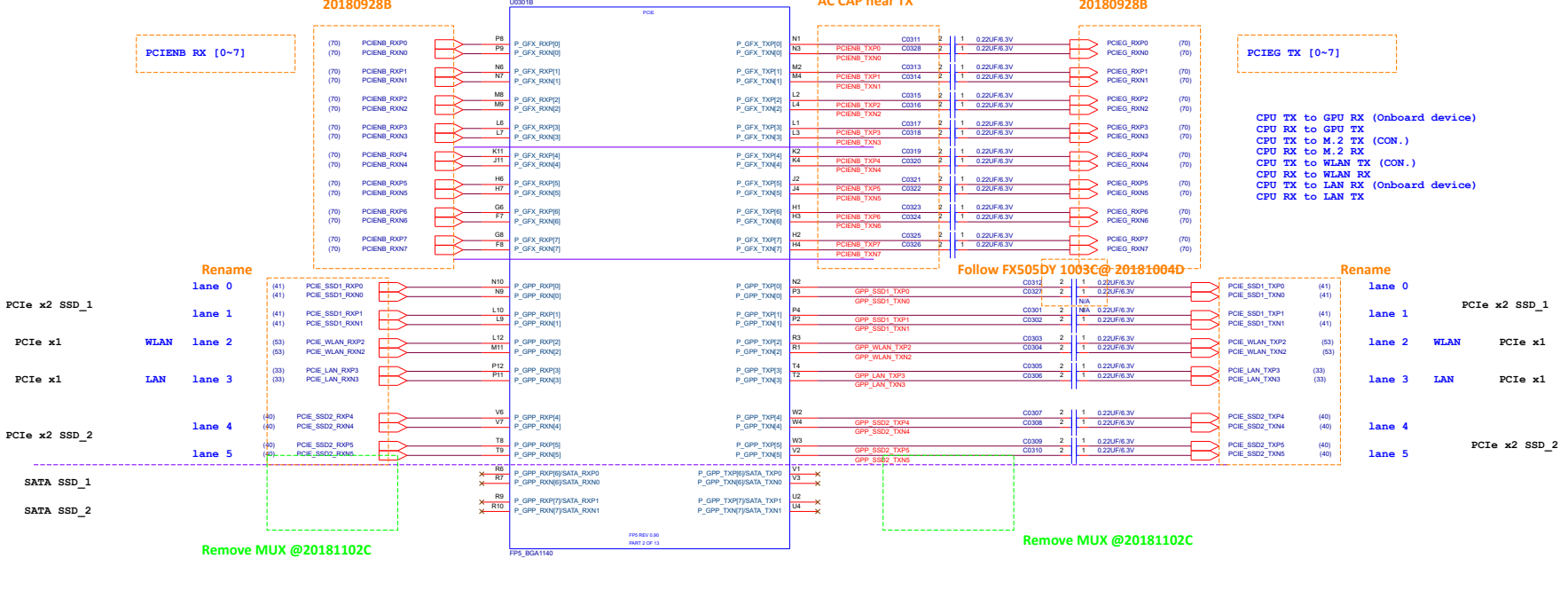
Rename to PCIENB TX [0-7]
20180928B
AC CAP near TX

Rename to PCIEG RX [0-7]
20180928B

PCIENB RX [0~7]

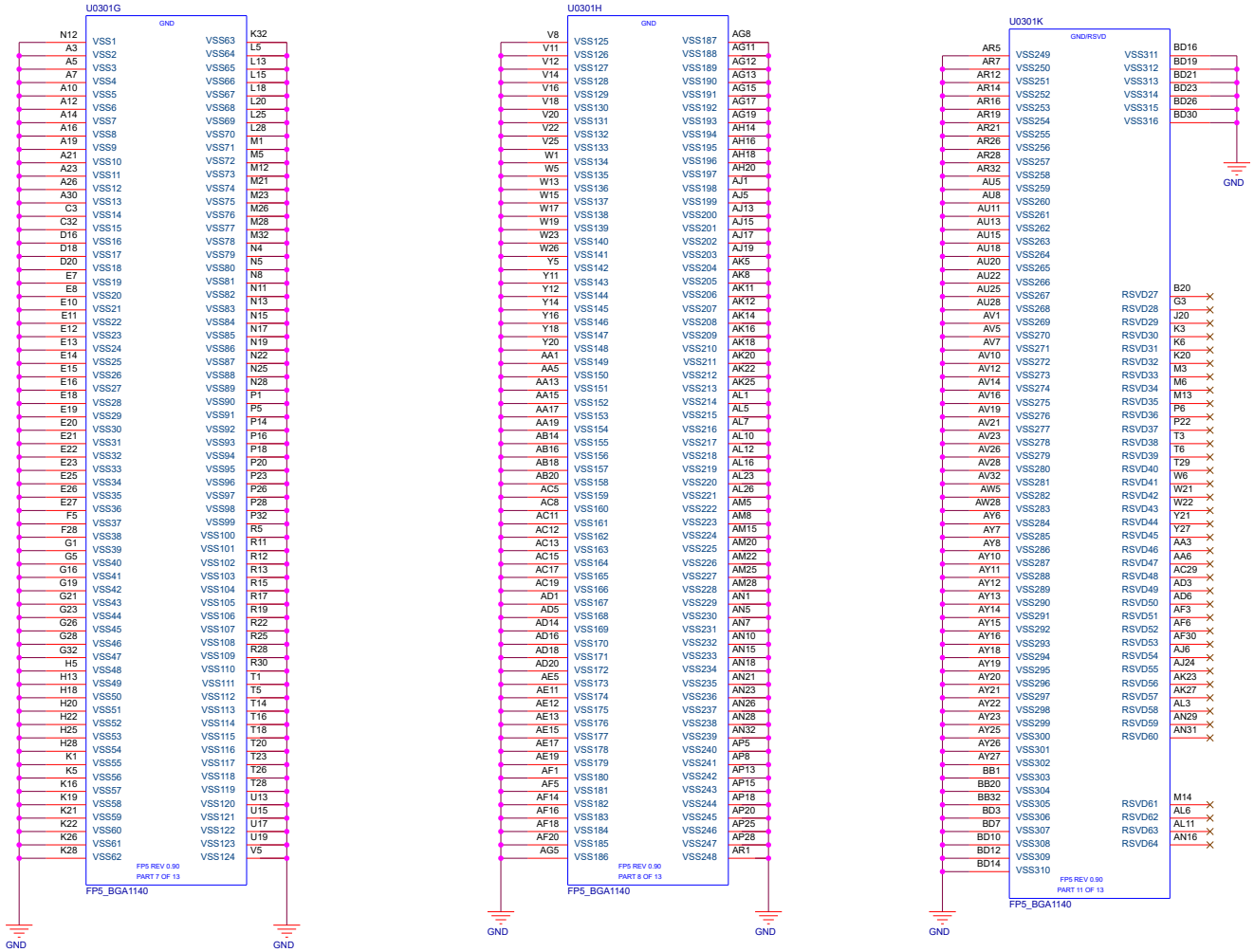
PCIEG TX [0~7]

CPU TX to GPU RX (Onboard device)
CPU RX to GPU TX
CPU TX to M.2 TX (CON.)
CPU RX to M.2 RX
CPU TX to WLAN TX (CON.)
CPU RX to WLAN RX
CPU TX to LAN RX (Onboard device)
CPU RX to LAN TX



ASUS	Project Name: FX505DY		Rev: R1.0
Title :	CFL-H_CPU_DMI,PEG,FDI,eDP,DDI_R1.3B		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1	
Date: Monday, April 29, 2019	Sheet 3	of 104	

CPU_GND



Project Name: FX505DY		Rev: R1.0
Title : AMD_CPU_GND		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: RD2 EE3	
Date: Monday, April 29, 2019	Sheet 5 of 104	

Display

Rename
20181001C

L_VDDEN_CPU change to EDP_VDD_EN
@20181113B

L_BKLTCTL_CPU change to BL_PWM_CPU
@20181112A

Remove DP from APU @20181108C

Add @20181022D

Test pin follow AMD BP Probing header

Add @20181219B (EMI request)

Add @20181122A

Modify
@20181023J

送進CPU 拉PROCHOT

直接改unmount?
@20181013B

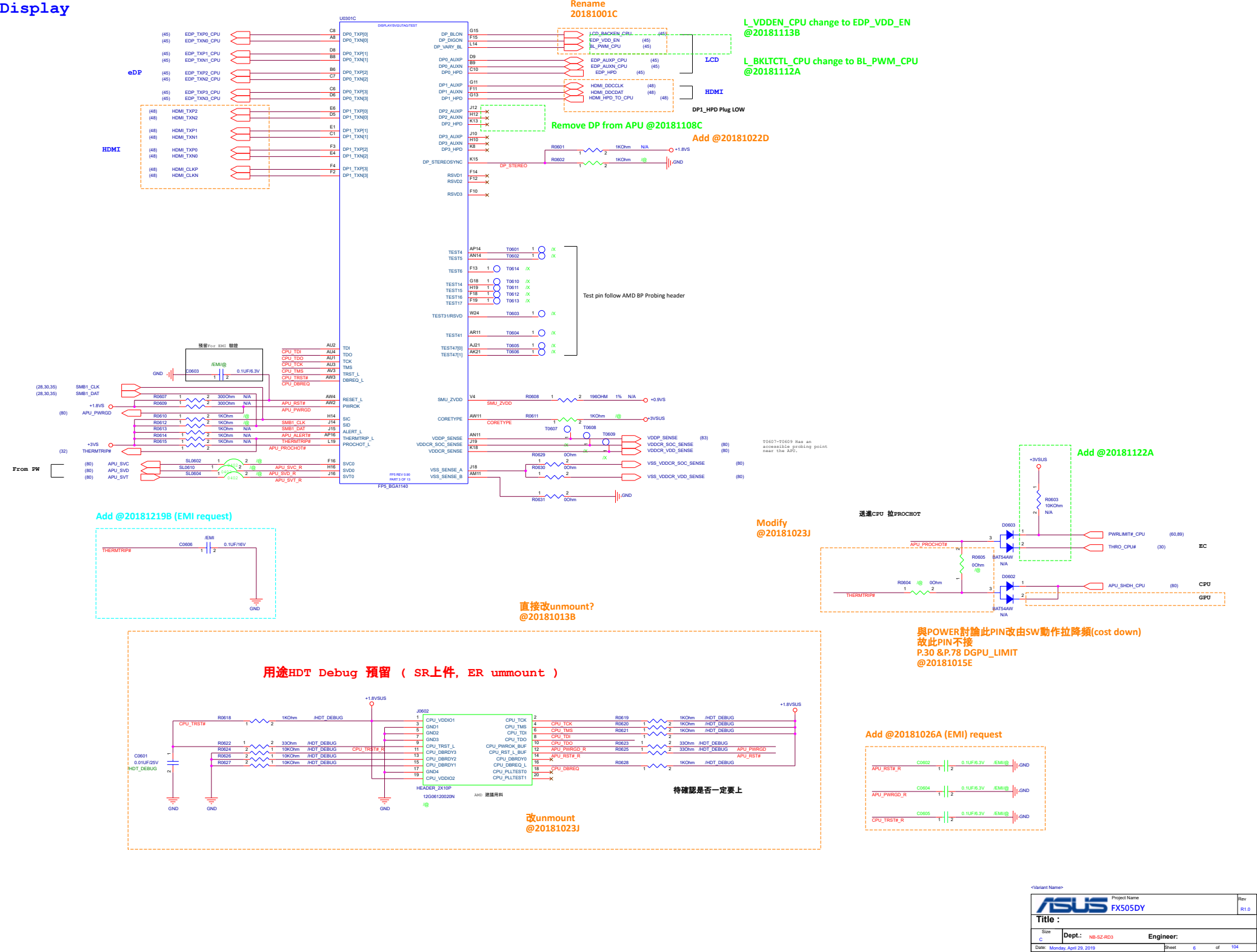
與POWER討論此PIN改由SW動作拉降頻(cost down)
故此PIN不接
P.30 &P.78 DGPU_LIMIT
@20181015E

用途HDT Debug 預留 (SR上件, ER ummount)

待確認是否一定要上

改unmount
@20181023J

Add @20181026A (EMI) request



<Variant Name>

ASUS	Project Name: FX505DY	Rev: R1.0
Title :		
Size: C	Dept.: NB-SZ-RD3	Engineer:
Date: Monday, April 29, 2019	Sheet 6 of 104	

I2C/RST/GPIO/AZ

EGPIO27: internal pull down by software.

R0702, C0701 mount, PCIE_RST1_L/EGPIO27 請預留0 ohm 至BUF_PLT_RST#
@20181022C

Add @20181218F

R0706.1 & R0711.1 +3VSUS to +3VS
Follow FX505DY 1003C@ 20181004D

@20181023K

DDR4_SPD_CLK/DATA

PD

Add PD I2C
@20181218E

DDR4

Tocuh pad

Change @20181218G

Follow FX505DY &公板
@20181015H

Change @20181218G

Remove SATA_LED# @20181016A

特確認Pull-H or L @20181013C

Audio

@20181018J

DGPU

@20181013B

Add HDMI_HDP_EN_dGPU#
@20181107A

Change HDMI_HDP_EN_dGPU# to DP_HPD_event#
@20181108C

Onboard Memory PCB-ID:
AGPIO3 =>DIMM_SEL0
AGPIO4 =>DIMM_SEL1
AGPIO10 =>DIMM_SEL2

LLL to Micron
LLH to Samsung
@20181227C

Default Samsung
@20190201A

Add @20181218G

DDR4 Memory Down pool

	Micron (1Rx8Gb) 03012-00030700 Micron DDR4 2666 MT40A1G8SA-075:E	Samsung (1Rx16Gb) 03012-00060000 Samsung DDR4 2666 K4AAG085WA-BCTD		
DIMM_SEL0	L	L		
DIMM_SEL1	L	L		
DIMM_SEL2	L	H		

LLL to Micron
LLH to Samsung
@20181227C

<Variant Name>

ASUS	Project Name: FX505DY	Rev: R1.0
Title :		
Size: B	Dept.: NB-SZ-RD3	Engineer:
Date: Monday, April 29, 2019	Sheet 7 of 104	

CPU CLK

Add @20181017E

DGPU CLKReq#

For Optimus

Q0801 2N7002K

CLKREQ6_GPU#

R0811 10KOhm

(7,70,77) DGPU_PWROK

GND

改回 @20190129B

For AMD checklist @20181018H

+3VS

R0801 R0812 R0802 R0803 R0804 10KOhm N/A

U0301E

CLK/LPCE/EMMC/SD/SPI/eSPI/UART

(41) CLKREQ0_SSD1#
(53) CLKREQ1_WLAN#
(33) CLKREQ2_LAN#
(40) CLKREQ3_SSD2#

TBD

(70) CLKREQ6_GPU#

CLK_REQ0_L/SATA_IS0_L /SATA_IP0_L/AGPIO92
CLK_REQ1_L/AGPIO115
CLK_REQ2_L/AGPIO116
CLK_REQ3_L/SATA_IS1_L /SATA_IP1_L/EGPIO131
CLK_REQ4_L/OSCIN/EGPIO132
CLK_REQ5_L/EGPIO120
CLK_REQ6_L/EGPIO121

GPU

SSD

WLAN

LAN

(41) PCIE_SSD1_CLKP
(41) PCIE_SSD1_CLKN
(53) PCIE_WLAN_CLKP
(53) PCIE_WLAN_CLKN
(33) PCIE_LAN_CLKP
(33) PCIE_LAN_CLKN
(40) PCIE_SSD2_CLKP
(40) PCIE_SSD2_CLKN

GPP_CLK0P GPP_CLK0N
GPP_CLK1P GPP_CLK1N
GPP_CLK2P GPP_CLK2N
GPP_CLK3P GPP_CLK3N
GPP_CLK4P GPP_CLK4N
GPP_CLK5P GPP_CLK5N
GPP_CLK6P GPP_CLK6N

PCIE_CLK_P/N
都有預留電阻於後端

GPU

(70) GPU_PCIE_CLKP
(70) GPU_PCIE_CLKN

To GPU CLK 20181001A

X48M_OSC
X48M_X1
X48M_X2
RSVD4
RSVD5
RTCCLK
X32K_X1
X32K_X2

48M_X1 48M_X2 1MOhm R0809 N/A SL0802 XT0801 C0804 3.9PF/50V C0801 3.9PF/50V

RTC_CLK C0803 15PF/50V C0805 15PF/50V 32K_X1 32K_X2 XT0802 32.768Khz N/A R0810 20MOhm N/A SL0805

FP5_BGA1140

EGPIO70/SD_CLK
LPC_PD_L/SD_CMD/AGPIO21
LAD0/SD_DATA0/EGPIO104
LAD1/SD_DATA1/EGPIO105
LAD2/SD_DATA2/EGPIO106
LAD3/SD_DATA3/EGPIO107
LPCCLK0/EGPIO74
LPC_CLKRUN_L/AGPIO88
LPCCLK1/EGPIO75
SERIRQ/AGPIO87
LFRAME_L/EGPIO109
LPC_RST_L/SD_WP_L/AGPIO32
AGPIO68/SD_CD
LPC_PME_L/SD_PWR_CTRL/AGPIO22

LPC_LAD0 (30,44)
LPC_LAD1 (30,44)
LPC_LAD2 (30,44)
LPC_LAD3 (30,44)
LPC_CLK0 (30)
LPC_CLKRUN# (30)
LPC_CLK1 (44)
INT_SERIRQ (30)
LPC_FRAME# (30,44)
LPC_RST# (30)
EXT_SCI# (30)

R0805 22Ohm N/A LPC_CLK0_R
R0806 22Ohm /DEBUG LPC_CLK1_R
C0802 150PF/50V /@ GND
R0807 N/A 33Ohm APGIO68

LPC

EXT_SCI# R0808 10KOhm N/A +3VSUS

Delete .BA11 SSD_SATA1_PCIE_DET @20181107A

SPI_ROM_REQ/EGPIO67
SPI_ROM_GNT/AGPIO76
ESPI_RESET_L/KBRST_L/AGPIO129
ESPI_ALERT_L/LDRQ0_L/EGPIO108
SPI_CLK/ESPI_CLK
SPI_DI/ESPI_DAT1
SPI_DO/ESPI_DAT0
SPI_WP_L/ESPI_DAT2
SPI_HOLD_L/ESPI_DAT3
SPI_CS1_L/EGPIO118
SPI_CS2_L/ESPI_CS_L/AGPIO30
SPI_CS3_L/AGPIO31
SPI_TPM_CS_L/AGPIO29

RC_IN# (30) R0815 10KOhm N/A +3VS
ESI_ALERT_L

Add @20190429A

APU_SPI_CLK (30)
APU_SPI_DI (30)
APU_SPI_DO (30)
APU_SPI_WP# (30)
APU_SPI_HOLD# (30)
APU_SPI_CS1# (30)

SPI

Add T0803 & T0804 for AMD request @20190213A

T0803 /@
T0804 /@

UART0_RXD/EGPIO136
UART0_TXD/EGPIO138
UART0_RTS_L/UART2_RXD/EGPIO137
UART0_CTS_L/UART2_TXD/EGPIO135
UART0_INTR/AGPIO139

FX505DY connect to DGPU @20181013B
Change test point @20181018H

T0801 /@
T0802 /@

EGPIO141/UART1_RXD
EGPIO143/UART1_TXD
EGPIO142/UART1_RTS_L/UART3_RXD
EGPIO140/UART1_CTS_L/UART3_TXD
AGPIO144/UART1_INTR

DGPU Power EN pin

DGPU Power EN pin

APGIO144

Delete .BB16 SSD_SATA2_PCIE_DET @20181107A

+3VSUS R0813 10KOhm /@ APGIO68 R0814 10KOhm /@ APGIO144 GND

Add APGIO68&144 @20181109B

teknisi-indonesia

design guide pull high

+1.8VSUS +3VSUS R0819 10KOhm N/A R0817 10KOhm N/A APU_SPI_CLK (7) SYS_RESET# R0820 2KOhm /@ R0818 2KOhm /@ GND

WLAN_SUS_CLK Update

+3VSUS C0806 0.1UF/25V /@ GND U0801 MC74VHC1G04DFT2G /@ (40,41,53) SUS_CLK RTC_CLK GND R0821 0Ohm N/A

<Variant Name>

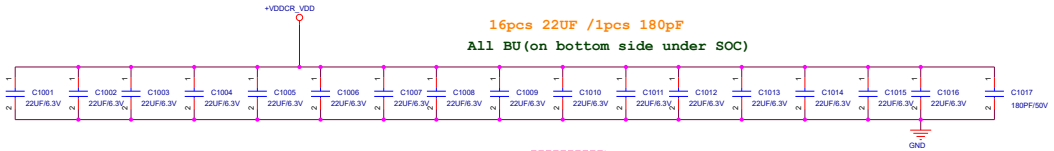
ASUS Project Name FX505DY Rev R1.0

Title :

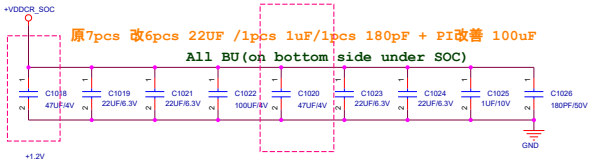
Size C Dept.: NB-SZ-RD3 Engineer:

Date: Monday, April 29, 2019 Sheet 8 of 104

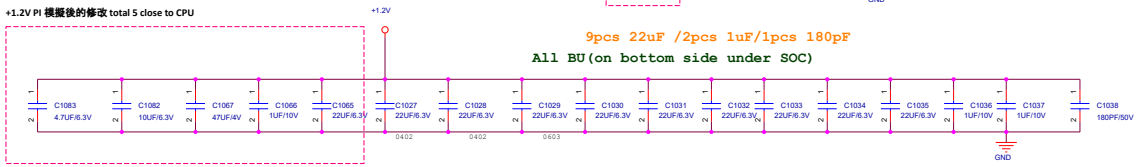
CPU_CAP

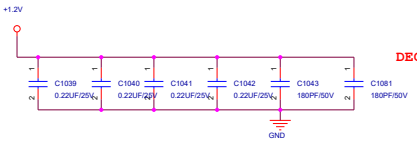


Change C1018 C1020 11G233222625150
to 11204-0004D000
@20190223A



+1.2V PI 模擬後的修改 total 5 close to CPU

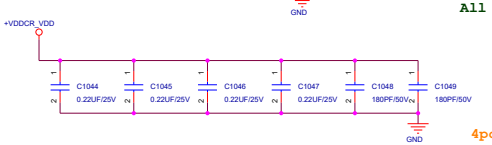




DECOUPLING BETWEEN PROCESSOR AND DIMMs

4pcs 0.22uF / 2pcs 180pF

All BU(on bottom side under SOC)



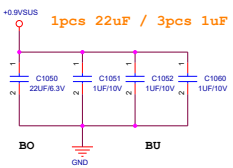
4pcs 0.22uF / 2pcs 180pF

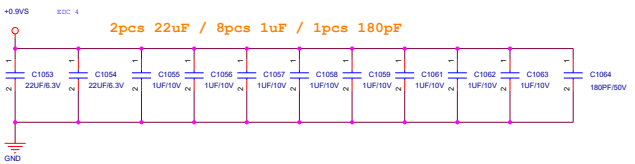
DECOUPLING BETWEEN PROCESSOR AND DIMMs ACROSS VDDIO AND VSS SPLIT

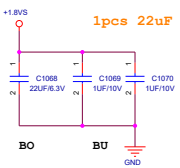
If the VSS plane is cut to create a VDDIO_MEM_S3 plane, ceramic capacitors with NP0 or C0G dielectric are connected across the VDDIO_MEM_S3 and VSS plane split.

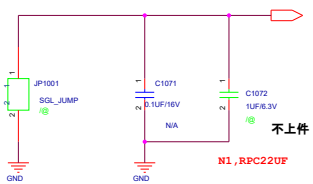
POWER RAIL

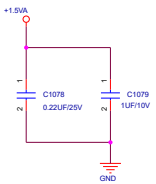
CPU	CPU_FP5	FX505ZD	CRB線路
Power rail	VDDCR_SOC	+VDDCR_SOC	+APU_VDDSOC_RUN
	VDDIO_MEM_S3	+1.2V	+APU_VDDIO_SUS
	VDDIO_AUDIO	+1.8VS	+VDD_AUD_ALW
	VDD_33	+3VS	+3.3V_RUN
	VDD_18	+1.8VS	+1.8V_RUN
	VDD_18_S5	+1.8VSUS	+1.8V_ALW
	VDD_33_S5	+3VSUS	+3.3V_ALW
	VDDP_S5	+0.9VSUS	+VDDP_ALW
	VDDP	+0.9VS	+VDDP_RUN
	VDDBT_RTC	+1.5VA	+VDDBT_RTC
	VDDCR	+VDDCR_VDD	+APU_VDDCORE_RUN



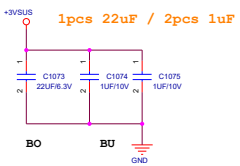


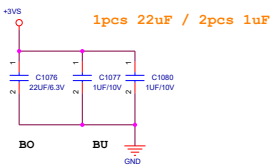






1pcs 0.22uF / 1pcs 1uF





ASUS	Project Name: FX505DY	Rev: R1.0
Title :	CFL-H_CPU_PWR(1)_R1.3B	
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD EE3
Date: Monday, April 29, 2019	Sheet 10 of 104	

PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	RCIN#	Native	RC_IN#		PU 10K	+3VS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_KBCPCI_PCH_X1			
GPP_A10	CLKOUT_LPC1	Native	CLK_DEBUG_X1			
GPP_A11	PME#	GPO	(N.C)			
GPP_A12	GPI	GPO	(N.C)			
GPP_A13	SUSWANRN#	Native	ME_SusPwrDnAck		PU 10K(@)	+3VSUS
GPP_A14	SUS_STAT#	Native	PCH_SUS_STAT#			
GPP_A15	SUS_ACK#	Native	PM_SUSACK#			
GPP_A16	Native/GPI	GPO	(N.C)			
GPP_A17	GPI	GPO	(N.C)			
GPP_A18	GPI	GPO	(N.C)			
GPP_A19	GPI	GPO	(N.C)			
GPP_A20	GPI	GPO	(N.C)			
GPP_A21	GPI	GPO	TBTA_MRESET(Reserved)			
GPP_A22	GPI	GPO	PCH_RTD3_CIO_PWR_EN		PU 10K	+VCC3V3_SX
GPP_A23	GPI	GPO	PCH_RTD3_USB_PWR_EN		PD 100K	

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	(N.C)			
GPP_B1	GPI	GPI	TBT_I2C_INT_PCH		PU 10K	+3VSUS
GPP_B2	GPI	GPO	(N.C)			
GPP_B3	GPI	GPO	(N.C)			
GPP_B4	GPI	GPO	(N.C)			
GPP_B5	GPI	Native	CLK_REQ0#/CLKREQ0_PEGA#		PU 10K	+3VSUS
GPP_B6	GPI	Native	CLK_REQ1#		PU 10K(@)	+3VSUS
GPP_B7	GPI	Native	CLK_REQ2#/CLKREQ2_WLAN_AC#		PU 10K	+3VSUS
GPP_B8	GPI	Native	CLK_REQ3#		PU 10K(@)	+3VSUS
GPP_B9	GPI	Native	CLK_REQ4#/CLKREQ4_GLAN#		PU 10K	+3VSUS
GPP_B10	GPI	Native	CLK_REQ5#/CLKREQ5_TBT #		PU 10K	+3VSUS
GPP_B11	GPO	GPO	(N.C)			
GPP_B12	SLP_S0#	Native	SLP_S0#			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPPB14	PD		
GPP_B15	GPI	GPI	PCH_GPPB15/KB_LANG_ID0		PU 10K	+3VS
GPP_B16	GPI	GPI	PCH_GPPB16/KB_LANG_ID1		PU 10K	+3VS
GPP_B17	GPI	GPO	PCH_GPPB17/XBOX_WRST		PD 10K	
GPP_B18	GPO	Strap	PCH_GPPB18	PD		
GPP_B19	GPI	GPO	PCH_GPPB19/BT_ON_PCH		PD 10K(@)	
GPP_B20	GPI	GPO	PCH_GPPB20/GPUEVENT#_PCH		PU 10K	+3VSUS
GPP_B21	GPI	GPI	PCH_GPPB21/GC6FBEN_PCH		PU 10K(@)	+3VS
GPP_B22	GPO	Strap	PCH_GPPB22	PD		
GPP_B23	GPO	Native	SML1ALERT#	PD	PU 150K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		PU 2.2K	+3VSUS
GPP_C2	GPO	GPI	GPP_C2_BT_UART_WAKE_N	PD	PU 4.7K	+3VSUS
GPP_C3	SML0CLK	Native	SML0_CLK (Reserved)		PU 2.2K	+3VSUS
GPP_C4	SML0DATA	Native	SML0_DAT (Reserved)		PU 2.2K	+3VSUS
GPP_C5	GPO	Strap	PCH_GPPC5	PD		
GPP_C6	SML1CLK	Native	SML1_CLK		PU 2.2K	+3VSUS
GPP_C7	SML1DATA	Native	SML1_DAT		PU 2.2K	+3VSUS
GPP_C8	GPI	GPO	(N.C)			
GPP_C9	GPI	GPO	(N.C)			
GPP_C10	GPI	GPO	(N.C)			
GPP_C11	GPI	GPO	(N.C)			
GPP_C12	GPI	GPI	DIMM_SEL0			
GPP_C13	GPI	GPI	DIMM_SEL1			
GPP_C14	GPI	GPI	DIMM_SEL2			
GPP_C15	GPI	GPI	NFC_ID		PU 10K	+3VSUS
GPP_C16	GPI	Native	TBT_I2C_SDA_PCH		PU 2.2K	+3VSUS
GPP_C17	GPI	Native	TBT_I2C_SCL_PCH		PU 2.2K	+3VSUS
GPP_C18	GPI	Native	I2C1_SDA		PU 2.2K	+3VS
GPP_C19	GPI	Native	I2C1_SCL		PU 2.2K	+3VS
GPP_C20	GPI	GPI	PCH_GPPC20/DGPU_PWROK		PU 10K	+3VS_NV
GPP_C21	GPI	GPO	PCH_GPPC21/GPU_RST#		PD 10K	
GPP_C22	GPI	GPO	(N.C)			
GPP_C23	GPI	GPI	CPAD_INT#		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GPI	GPO	(N.C)			
GPP_D1	GPI	GPO	(N.C)			
GPP_D2	GPI	GPO	(N.C)			
GPP_D3	GPI	GPO	(N.C)			
GPP_D4	GPI	GPO	(N.C)			
GPP_D5	GPI	Native3	PCH_GPPD5/M.2_BT_PCMFRM_CRF_RST_N		PD 75K	
GPP_D6	GPI	Native3	PCH_GPPD6/M.2_BT_PCMOUT_CLKREQ0		PD 75K(@)	
GPP_D7	GPI	GPO	PCH_GPPD7/M.2_BT_PCMIN		PD 100K(@)	
GPP_D8	GPI	GPO	PCH_GPPD8/M.2_BT_PCMCLK			
GPP_D9	GPI	GPO	(N.C)			
GPP_D10	GPI	GPO	(N.C)			
GPP_D11	GPI	GPO	(N.C)			
GPP_D12	GPI	GPO	(N.C)			
GPP_D13	GPI	GPO	(N.C)			
GPP_D14	GPI	GPO	(N.C)			
GPP_D15	GPI	GPO	(N.C)			
GPP_D16	GPI	GPO	(N.C)			
GPP_D17	GPI	GPO	(N.C)			
GPP_D18	GPI	GPO	(N.C)			
GPP_D19	GPI	GPO	(N.C)			
GPP_D20	GPI	GPO	(N.C)			
GPP_D21	GPI	GPO	(N.C)			
GPP_D22	GPI	GPO	(N.C)			
GPP_D23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	GPI	Native	SATAPCIE_DET0		PU 10K(@)	+3VS
GPP_E1	GPI	Native	SATAPCIE_DET1		PU 10K	+3VS
GPP_E2	GPI	Native	SATAPCIE_DET2		PU 10K(@)	+3VS
GPP_E3	GPI	GPI	EXT_SMI#		PU 10K	+3VS
GPP_E4	GPI	Native	SATA0_HDD1_DEVSLP		PU 10K(@)	+3VS
GPP_E5	GPI	Native	SATA1_NGFF3_DEVSLP		PU 10K(@)	+3VS
GPP_E6	GPI	Native	NGFF3_DEVSLP		PU 10K(@)	+3VSUS
GPP_E7	GPI	GPI	EXT_SCI#		PU 10K	+3VS
GPP_E8	GPI	Native	SATA_LED#		PU 10K	+3VS
GPP_E9	GPI	Native	USB_OC#0		PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1		PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2		PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3		PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	GPI	Native	SATAPCIE_DET3		PU 10K(@)	+3VS
GPP_F1	GPI	Native	SATAPCIE_DET4		PU 10K	+3VS
GPP_F2	GPI	GPO	(N.C)			
GPP_F3	GPI	GPO	(N.C)			
GPP_F4	GPI	GPO	(N.C)			
GPP_F5	GPI	GPO	(N.C)			
GPP_F6	GPI	GPO	(N.C)			
GPP_F7	GPI	GPO	(N.C)			
GPP_F8	GPI	GPO	(N.C)			
GPP_F9	GPI	GPO	(N.C)			
GPP_F10	GPI	GPO	(N.C)			
GPP_F11	GPI	GPO	(N.C)			
GPP_F12	GPI	GPO	(N.C)			
GPP_F13	GPI	GPO	(N.C)			
GPP_F14	GPI	GPO	(N.C)			
GPP_F15	GPI	Native	USB_OC#4		PU 10K	+3VSUS
GPP_F16	GPI	Native	USB_OC#5		PU 10K	+3VSUS
GPP_F17	GPI	Native	USB_OC#6		PU 10K	+3VSUS
GPP_F18	GPI	Native	USB_OC#7		PU 10K	+3VSUS
GPP_F19	GPI	GPO	(N.C)			
GPP_F20	GPI	GPO	(N.C)			
GPP_F21	GPI	GPO	(N.C)			
GPP_F22	GPI	GPO	(N.C)			
GPP_F23	GPI	GPO	PCH_GPPF23		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_G0	GPI	GPO	(N.C)			
GPP_G1	GPI	GPO	(N.C)			
GPP_G2	GPI	GPO	(N.C)			
GPP_G3	GPI	GPO	(N.C)			
GPP_G4	GPI	GPO	(N.C)			
GPP_G5	GPI	GPO	(N.C)			
GPP_G6	GPI	GPO	(N.C)			
GPP_G7	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	GPI	Native	CLK_REQ6#/CLKREQ6_NGFF1#		PU 10K	+3VSUS
GPP_H1	GPI	Native	CLK_REQ7#/CLKREQ7_NGFF2#		PU 10K	+3VSUS
GPP_H2	GPI	Native	CLK_REQ8#/CLKREQ8_NGFF3#		PU 10K	+3VSUS
GPP_H3	GPI	Native	CLK_REQ9#		PU 10K(@)	+3VSUS
GPP_H4	GPI	Native	CLK_REQ10#		PU 10K(@)	+3VSUS
GPP_H5	GPI	Native	CLK_REQ11#		PU 10K(@)	+3VSUS
GPP_H6	GPI	Native	CLK_REQ12#		PU 10K(@)	+3VSUS
GPP_H7	GPI	Native	CLK_REQ13#		PU 10K(@)	+3VSUS
GPP_H8	GPI	Native	CLK_REQ14#		PU 10K(@)	+3VSUS
GPP_H9	GPI	Native	CLK_REQ15#		PU 10K(@)	+3VSUS
GPP_H10	GPI	GPO	(N.C)			
GPP_H11	GPI	GPO	(N.C)			
GPP_H12	GPO	GPO	(N.C)	PD	PD 20K(@)	
GPP_H13	GPI	GPO	(N.C)			
GPP_H14	GPI	GPO	(N.C)			
GPP_H15	GPI	GPO	SML3ALERT#		PU 100K	+3VSUS
GPP_H16	GPI	GPI	KBID_0			
GPP_H17	GPI	GPI	KBID_1			
GPP_H18	GPI	GPI	KBID_2			
GPP_H19	GPI	GPO	(N.C)			
GPP_H20	GPI	GPO	(N.C)			
GPP_H21	GPI	GPO	(N.C)			
GPP_H22	GPI	GPO	(N.C)			
GPP_H23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GPI	GPO	(N.C)			
GPP_I1	GPI	GPO	(N.C)			
GPP_I2	GPI	GPO	(N.C)			
GPP_I3	GPI	GPO	(N.C)			
GPP_I4	GPI	GPO	EDP_HPD		PD 100K	
GPP_I5	GPI	GPO	(N.C)			
GPP_I6	GPO	GPO	(N.C)			
GPP_I7	GPI	GPO	(N.C)			
GPP_I8	GPO	GPO	(N.C)			
GPP_I9	GPI	GPO	(N.C)			
GPP_I10	GPO	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_J0	GPI	GPO	(N.C)			
GPP_J1	CPU_VCCIO_PWR_GATE#	Native	CPU_C10_GATE#_PCH		PU 100K	+1.8VSUS
GPP_J2	GPI	GPO	(N.C)			
GPP_J3	GPI	GPO	(N.C)			
GPP_J4	CNV_BRI_DT	Native	CNV_BRI_DT		PU 4.7K	+1.8VSUS
GPP_J5	CNV_BRI_RSP	Native	CNV_BRI_RSP		PU 20K(@)	+1.8VSUS
GPP_J6	CNV_RGI_DT	Native	CNV_RGI_DT		PD 75K	
GPP_J7	CNV_RGI_RSP	Native	CNV_RGI_RSP		PU 20K(@)	+1.8VSUS
GPP_J8	GPI	GPO	(N.C)			
GPP_J9	GPO	GPO	(N.C)			
GPP_J10	GPI	GPO	(N.C)			
GPP_J11	A4WP_PRESENT	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_K0	GPI	GPO	GPIO_3_FORCE_PWR		PD 100K	
GPP_K1	GPI	GPI	PCB_ID0		PD 10K	
GPP_K2	GPI	GPI	PCB_ID1		PD 10K	
GPP_K3	GPI	GPO	GPP_K3/WLAN_BT_LED		PD 100K	
GPP_K4	GPI	GPO	GPP_K4/WLAN_LED		PD 100K	
GPP_K5	GPI	GPO	VOL_DOWN#(N.C)			
GPP_K6	GPI	GPO	VOL_UP#(N.C)			
GPP_K7	GPI	GPO	GPP_K7/TBT_HPD#		PU 10K	+3VS
GPP_K8	GPI	GPO	GPP_K8/DGPU_PWR_EN#		PU 10K(@)	+3VS
GPP_K9	GPI	GPO	WLAN_ON#		PD 100K	
GPP_K10	Reserved	GPO	GPP_K10/HDMI_HPD#		PU 10K	+3VS
GPP_K11	Reserved	GPO	GPP_K11/DP_HPD#		PU 10K	+3VS
GPP_K12	GPI	GPO	(N.C)			
GPP_K13	GPI	GPO	(N.C)			
GPP_K14	GPI	GPO	(N.C)			
GPP_K15	GPI	GPO	(N.C)			
GPP_K16	GPI	GPO	(N.C)			
GPP_K17	GPI	GPO	(N.C)			
GPP_K18	GPI	GPO	(N.C)			
GPP_K19	GPI	GPO	(N.C)			
GPP_K20	Reserved	GPO	(N.C)			
GPP_K21	Reserved	GPO	(N.C)			
GPP_K22	GPI	GPO	(N.C)			
GPP_K23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	PM_BATLOW#		PU 10K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_X1		PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	LAN_WAKE#(N.C)		PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#		PU 10K(@)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#		PD 100K	
GPD5	SLP_S4#	Native	SLP_S4#		PD 100K	
GPD6	SLP_A#	Native	SLP_A# (N.C)			
GPD7	GPO	GPO	PCH_GPD7		PU 10K	+3VA_DSW
GPD8	SUSCLK	Native	SUS_CLK#			
GPD9	SLP_WLAN#	Native	SLP_WLAN# (N.C)			
GPD10	SLP_S5#	Native	SLP_S5# (N.C)			
GPD11	LANPHYPC	GPO	LAN_PWREN (N.C)		PU 10K(@)	+3VA_DSW

IT8225VG-128/BX GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	O	GPO	PWR_LED	PD 1M	
GPA1	OD	GPO	CHG_LED#		
GPA2	OD	GPO	CHG_FULL_LED#		
GPA3	Alt	PWM	FAN2_PWM		
GPA4	O	GPO	EC_GPA4(N.C)		
GPA5	Alt	PWM	FAN1_PWM		
GPA6	Alt	GPO	EC_GPA6(N.C)		
GPA7	O	GPO	EC_GPA7(N.C)		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_OC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	EC_GPB2(N.C)		
GPB3	Alt	GPI	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PS_ON_EC		
GPB5	O	GPO	EC_GPB5/NKey_WRST	PD 10K	
GPB6	OD	GPO	RC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	O	GPO	EC_GPC0		
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	O	GPO	PM_PWRBTN#	PU 10K(@)	+3VSUS
GPC4	I	GPI	EC_GPC4/PM_SUSB#	PD 100K	
GPC5	I	GPI	PM_SUSC#	PD 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PD 100K	
GPC7	O	GPO	EC_GPC7/NKEY_PWR_EN	PD 10K(@)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPO	EC_GPD0/EC_OV_DDR		
GPD1	O	GPO	EC_GPD1/ME_AC_PRESENT		
GPD2	Alt	GPI	BUF_PLT_RST#	PD 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	O	GPO	EC_GPD5/OP_SD#		
GPD6	Alt	GPI	FAN1_TACH	PU 10K	+3VS
GPD7	Alt	GPI	FAN2_TACH	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PD 4.7K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PD 4.7K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO	5VSUS_ON	PD 1M & PU 100K	+3VA_EC
GPE4	O	GPO	VSUS_ON	PD 1M & PU 100K	+3VA_EC
GPE5	I	GPO	3VADSW_ON	PU 100K	+3VA_EC
GPE6	OD	GPO	WLAN_PWR_EN	PD 100K	
GPE7	OD	GPO	THRO_CPU#	PU 10K	+3VA_DSW

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	CAP_LED#		
GPF1	O	GPO	NUM_LED#		
GPF2	Alt	SMBus	P_SMB0_CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB0_DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	PECI	EC_PECI	PD 10K(@)	
GPF7	O	GPO	PCH_SPI_OV		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	O	GPO	PCH_SUSACK#		
GPG2	I	GPI	EC_GPG2	PU 100K	+3VA_EC
GPG6	O	GPO	EC_GPG6(N.C)		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB3_CLK/TBT_I2C_SCL_EC	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB3_DAT/TBT_I2C_SDA_EC	PU 4.7K	+3VA_EC
GPH3	O	GPO	PM_RSMRST#	PD 10K	
GPH4	O	GPO	DPWROK_EC	PD 10K	
GPH5	O	GPO	PM_PWROK	PD 10K	
GPH6	O	GPO	PM_SYSPWROK	PD 10K	
GPH7	O	GPO	LCD_BACKOFF#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_SUS#	PD 100K(@)	
GPI1	I	GPI	3VSUS_PWRGD	PU 100K	+3VSUS
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3VS
GPI3	I	GPI	IMVP8_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD_EC	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#	PU 10K(@)	+3VSUS
GPI6	Alt	AD	A/D_MAX_POWER		
GPI7	Alt	AD	MB_MAX_POWER	PU 100K&PD 270K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	O	GPO	EC_GPJ0		
GPJ1	O	GPI	GC6FBEN_PCH	PU 10K(@)	+3VS
GPJ2	Alt	GPI	EC_GPJ2/TBTA_I2C_INT_EC		
GPJ3	O	GPO	EC_GPJ3/USB_BC1.2_OFF#		
GPJ4	Alt	GPO	EC_GPJ4/USB30_5VBUS		
GPJ5	O	GPI	EC_GPJ5/MB_DOCK_JACK_DETECT	PU 100K(@)	+3VA
GPJ6	I	GPI	NKEY_INT#	PU 10K	+3VA_DSW_NKeyPWR
GPJ7	O	GPO	USB_CHARGE_ON#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/EIO0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/EIO1		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/EIO2		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/EIO3		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/ESCK		CLK_KBCPCI_PCH		
GPM5	LFRAME#/ECS#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

G703GI Source:

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	**SM-Bus Address**
SO-DIMM A(0)	A0h
SO-DIMM B(0)	A4h
SO-DIMM A(1)	A2h
SO-DIMM B(1)	A6h
EC Master (SMB1)	**SM-Bus Address**
SM-Bus Device	
GPU INT. Thermal sensor	9Eh, 9Ch
CPU Thermal Sensor	90h
TI_TAS5766M*2	98h, 9Ah
ASM1562	66h
GPU (Thermistor sense)	74h
PWR(Thermistor sense)	7Eh, 7Ch, 7Ah, 78h, 76h

Device Identification

CPU Thermal Senser		
1st	06G023123010	NCT7717U
2nd		

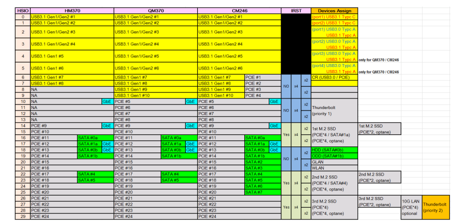
GPU Thermistor		
1st	06021-00260000	APL6002A8I-TRG
2nd		

USB3.0/PCIE/SATA Setting

1	USB3#1	
2	USB3#2	
3	USB3#3	USB Port1
4	USB3#4	
5	USB3#5	USB Port3
6	USB3#6	USB Port4
7	USB3#7	Card Reader
8	PCIE#2	
9	PCIE#3	
10	PCIE#4	
11	PCIE#5	ThunderBolt x4
12	PCIE#6	
13	PCIE#7	
14	PCIE#8	
15	PCIE#9	PCIE3.0 x 4 SSD
16	PCIE#10	
17	PCIE#11	
18	PCIE#12	
19	PCIE#13(SATA0B)	SATA HDD
20	PCIE#14(SATA1B)	
21	PCIE#15	GLAN
22	PCIE#16	WLAN_11AC
23	PCIE#17	PCIE3.0 x 4 SSD
24	PCIE#18	
25	PCIE#19	
26	PCIE#20	
27	PCIE#21	PCIE3.0 x 4 SSD
28	PCIE#22	
29	PCIE#23	
30	PCIE#24	

USB2.0 Setting

1	USB2#1	
2	USB2#2	
3	USB2#3	USB Port1
4	USB2#4	
5	USB2#5	USB Port3
6	USB2#6	USB Port4
7	USB2#7	Card Reader
8	USB2#8	XBOX WLAN
9	USB2#9	Camera
10	USB2#10	N-Key
11	USB2#11	
12	USB2#12	Tobii IS4
13	USB2#13	TBT
14	USB2#14	BT



571391_CFL_H_PDG_Rev0p71, page 230

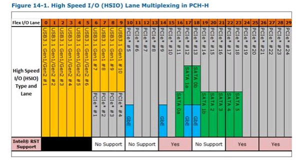


Figure 14-1. High Speed I/O (HSIO) Lane Multiplexing in PCH-H

571182_CNL_PCH_H_EDS_Vol_1_Rev_0_7, page24

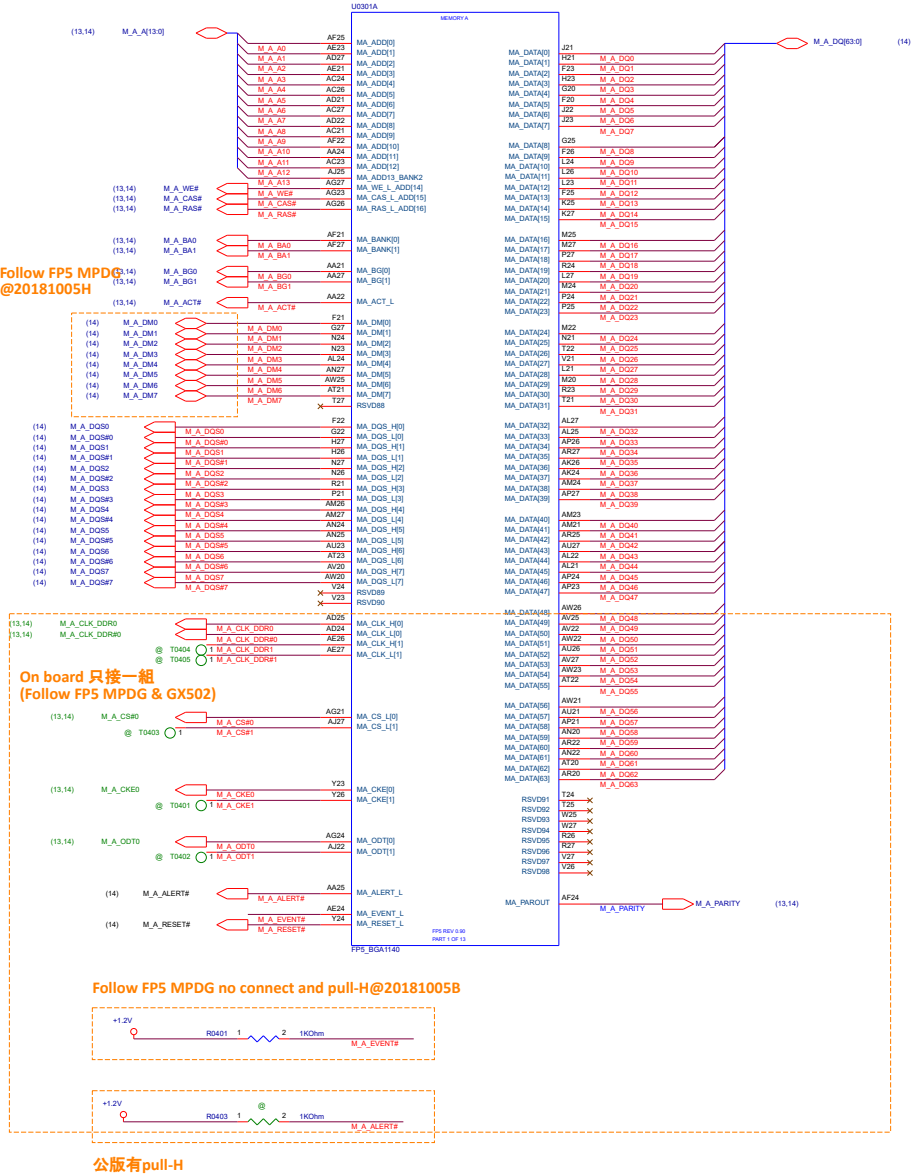
Table 1-7. PCH HSIO Detail (SKU 9-11of 11)

Flex I/O Lane	SKU HM370	SKU QM370	SKU CM246
0	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
3	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
4	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
5	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
6	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
7	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
8	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
9	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
10	GbE	PCIe*, GbE	PCIe*, GbE
11	N/A	PCIe*	PCIe*
12	N/A	PCIe*	PCIe*
13	N/A	PCIe*	PCIe*
14	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
15	PCIe*	PCIe*	PCIe*
16	PCIe*, SATA 0A	PCIe*, SATA 0A	PCIe*, SATA 0A
17	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A
18	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B
19	PCIe*, SATA 1B	PCIe*, SATA 1B	PCIe*, SATA 1B
20	PCIe*	PCIe*	PCIe*, SATA 2
21	PCIe*	PCIe*	PCIe*, SATA 3
22	PCIe*, SATA 4	PCIe*, SATA 4	PCIe*, SATA 4
23	PCIe*, SATA 5	PCIe*, SATA 5	PCIe*, SATA 5
24	PCIe*	PCIe*	PCIe*, SATA 6
25	PCIe*	PCIe*	PCIe*, SATA 7
26	PCIe*	PCIe*	PCIe*
27	PCIe*	PCIe*	PCIe*
28	PCIe*	PCIe*	PCIe*
29	PCIe*	PCIe*	PCIe*

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, April 29, 2019	Sheet 11 of 104	

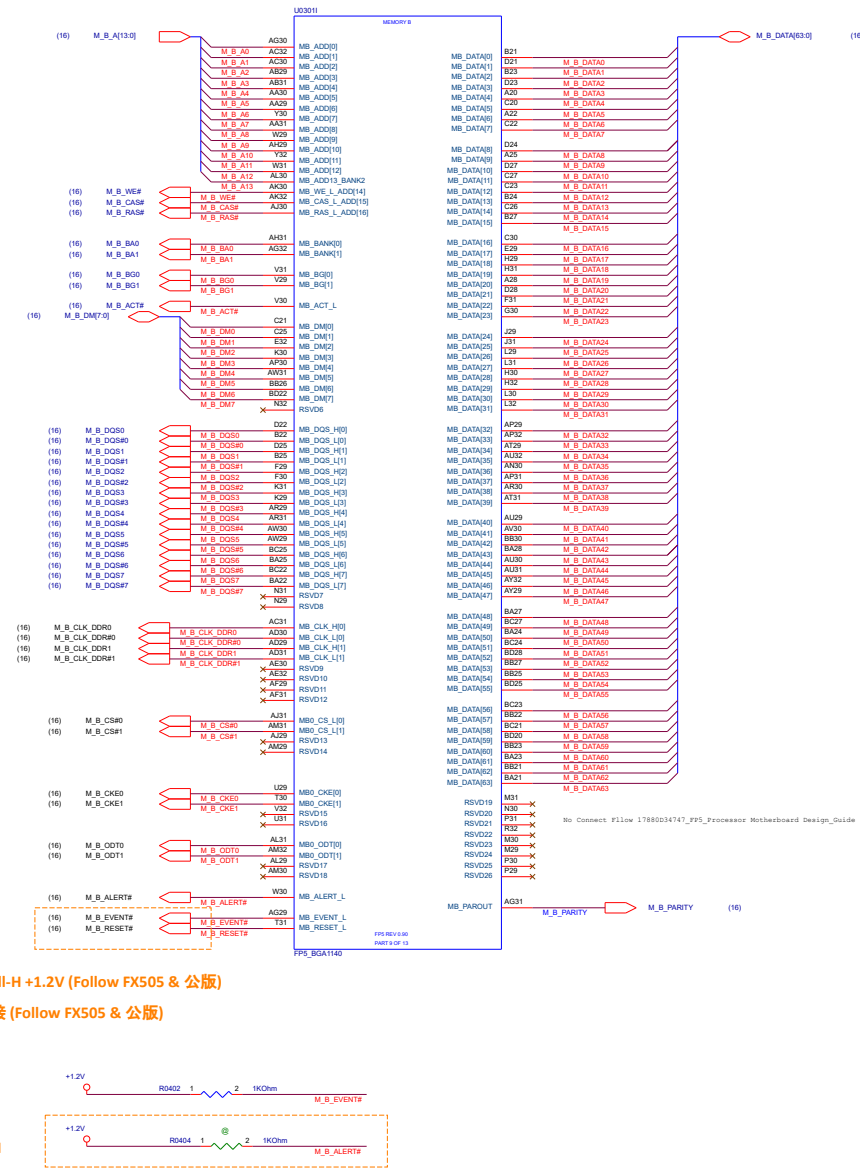
Memory Channel A

On Board DDR4



Memory Channel B

SO-DIMM DDR4



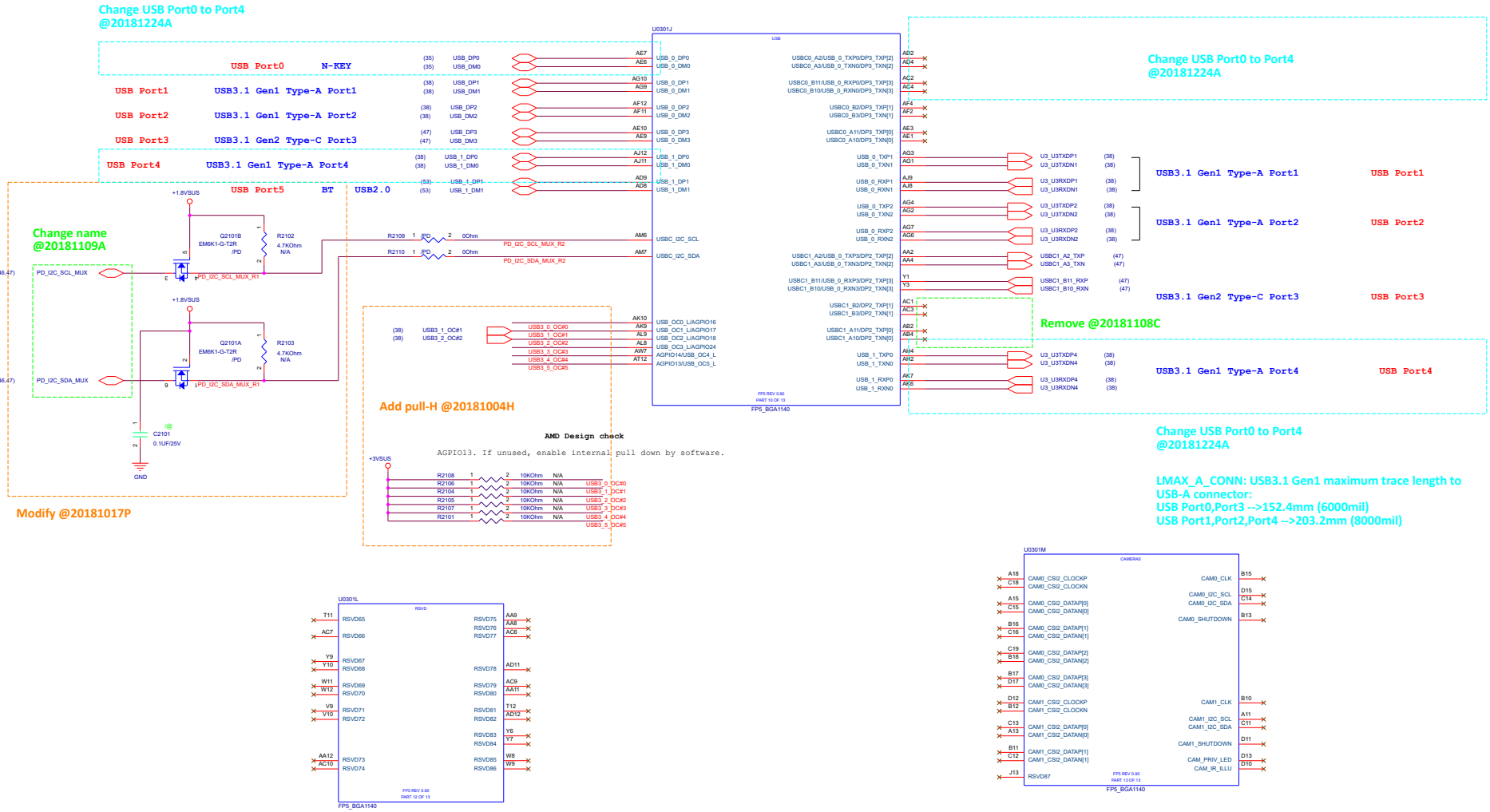
Project Name	FX505DY
Rev	R1.0
Title :	AMD_CPU_DDR4
Size	C
Dept.:	ASUSTeK COMPUTER INC
Engineer:	NB1 RD EE
Date:	Monday, April 29, 2019
Sheet	4 of 104

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, April 29, 2019	Sheet 15 of 104	

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, April 29, 2019	Sheet 17 of 104	

Title <Title>		
Size A	Document Number <Doc>	Rev R1.0
Date: Monday, April 29, 2019	Sheet 19 of 104	

CPU_USB



<Variant Name>

ASUS	Project Name: FX505DY	Rev: R1.0
Title :		
Size: C	Dept.: NB-SZ-RD3	Engineer:
Date: Monday, April 29, 2019	Sheet 21 of 104	

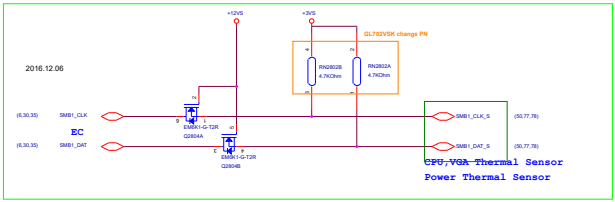
Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, April 29, 2019	Sheet 22 of 104	

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, April 29, 2019	Sheet 23 of 104	

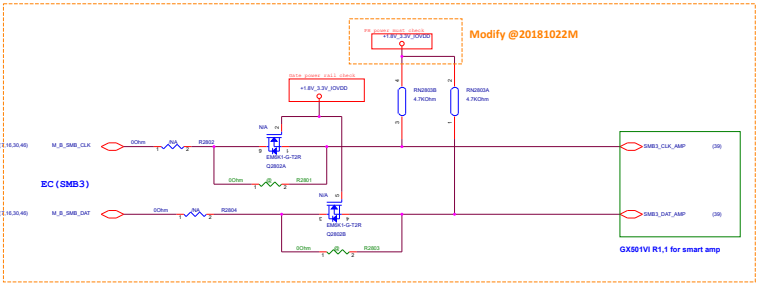
Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, April 29, 2019	Sheet 24 of 104	

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, April 29, 2019	Sheet 25 of 104	

Follow GL702ZM
@20181022C



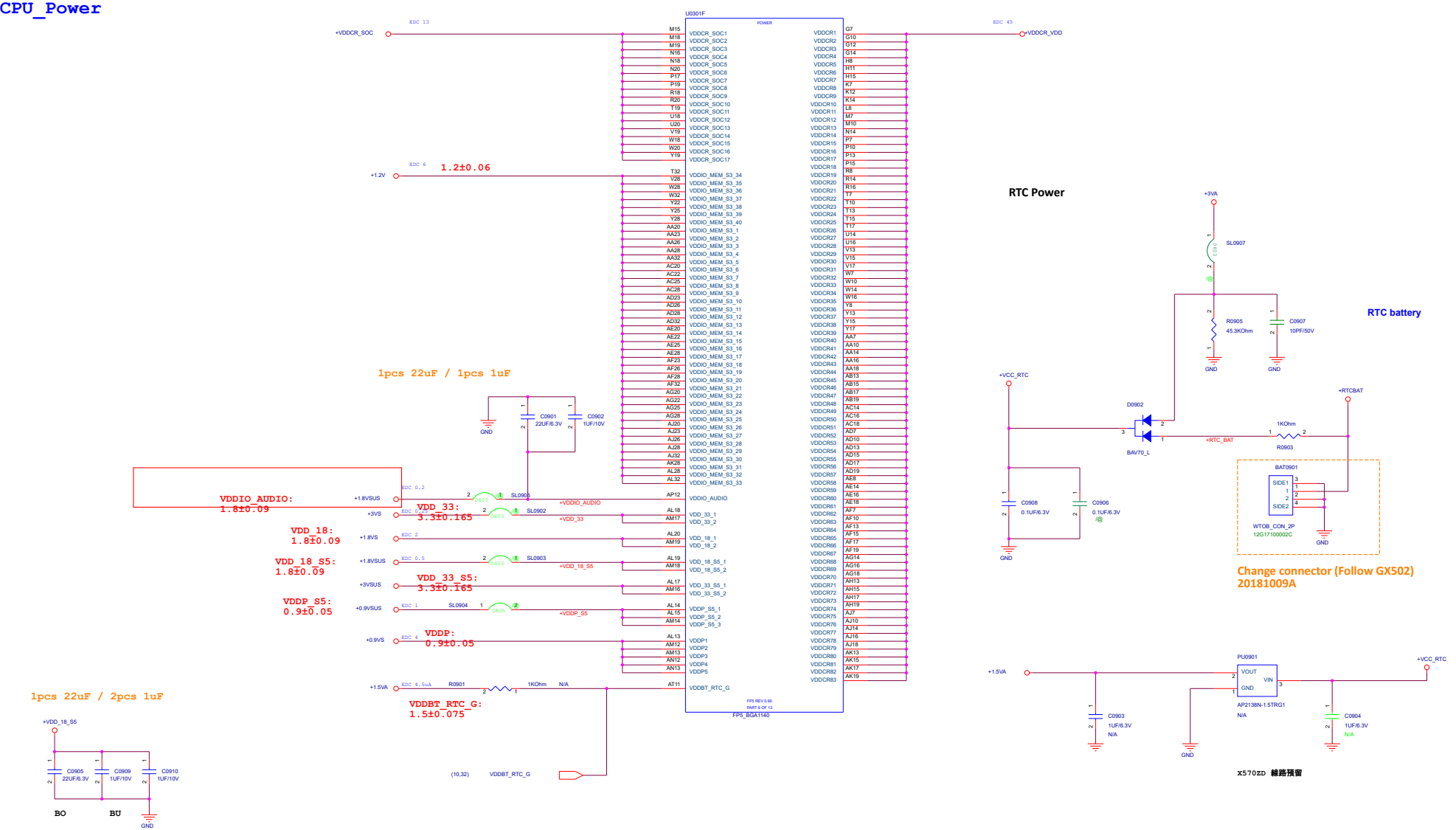
Add @20181017N



ASUS	Project Name: GX531GX		Rev: 1.0
Title :	PCH-SPI ROM,OTH		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Monday, April 29, 2019	Sheet: 28 of 104		

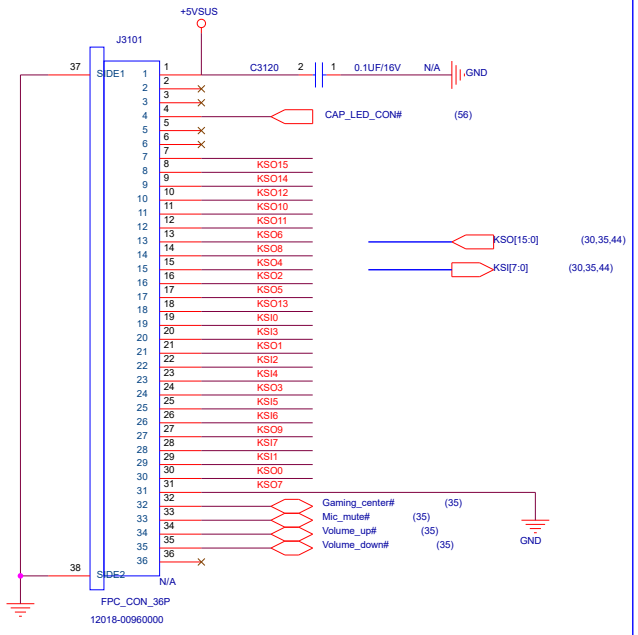
Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, April 29, 2019	Sheet 29 of 104	

CPU_Power

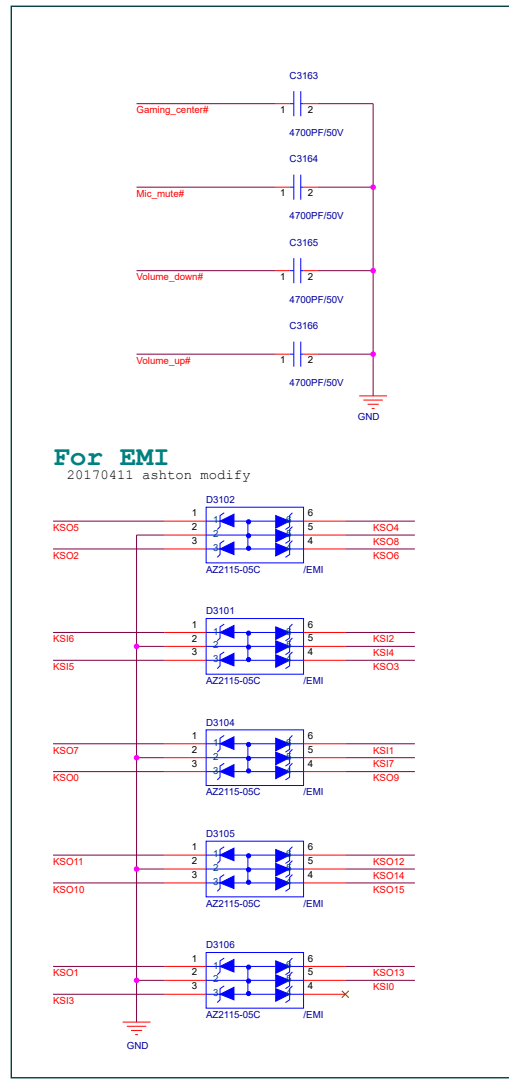


Project Name: FX505DY			Rev: R1.0
Title: CFL-H_CPU_PWR(1)_R1.3B			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD EE3	
Date: Monday, April 29, 2019	Sheet 9 of 104		

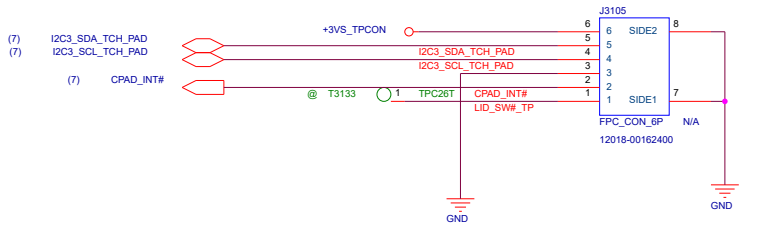
Keyboard Connector



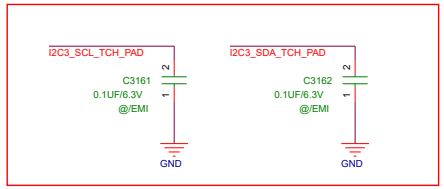
2017.02.08 update Keyboard connector



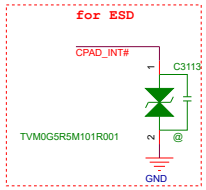
TP Conn.



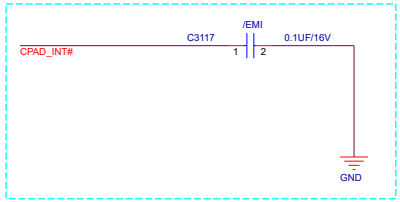
EMI Reserve
如要上件請確認容值(選擇Pico等級)

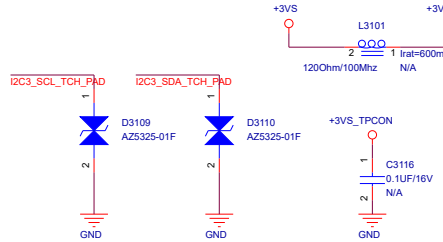


D3110 ESD Diode
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D



Add @20181219B (EMI request)





<Variant Name>

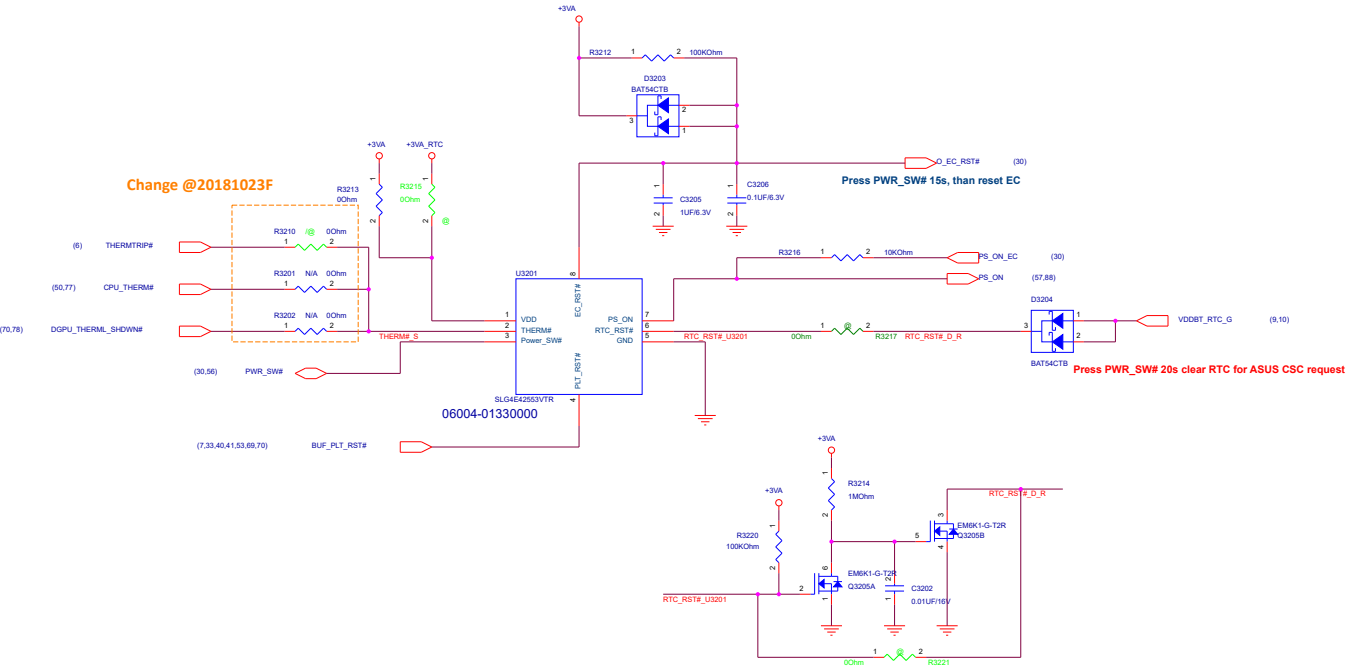
ASUSTeK COMPUTER	Title : KBC_KB & TP	
	Engineer: EE	
Size: B	Project Name: GM501	Rev: R1.0
Date: Monday, April 29, 2019	Sheet 31 of 104	

Modern standby project should use Silego solution for EC/RTC reset (Microsoft hardware requirements)

6.6.2 Power button behavior

https://docs.microsoft.com/en-us/windows-hardware/design/minimum/minimum-hardware-requirements-overview#section-60---shared-minimum-hardware-requirements-for-components

UX362FA R1.3 board will verify this circuit 7/E



<Variant Name>

ASUSTeK COMPUTER INC. NB4	Title : RST_Reset Circuit	
	Engineer: SZNB1	
Size: C	Project Name: FX505DY	Rev: R1.0
Date: Monday, April 29, 2019	Sheet 32 of 104	

33/34 pin ground pad
need ground via

MDI Interface

BB-RF Interface

U3301 RTL8111H-CG
02043-00091100

PCIE Tx,Rx方向是以PCH為觀點

07G010272501

X3301: 25MHZ +/-30ppm/10pF (3225)

1st: P/N:07G010272501 TXC/7V25000011

2nd: P/N:07G010952500 HOSONIC/E3FB25

PU/10K/+3VS @EEpage

series 0.22uF @EEpage

LAN PWR to +3VSUS

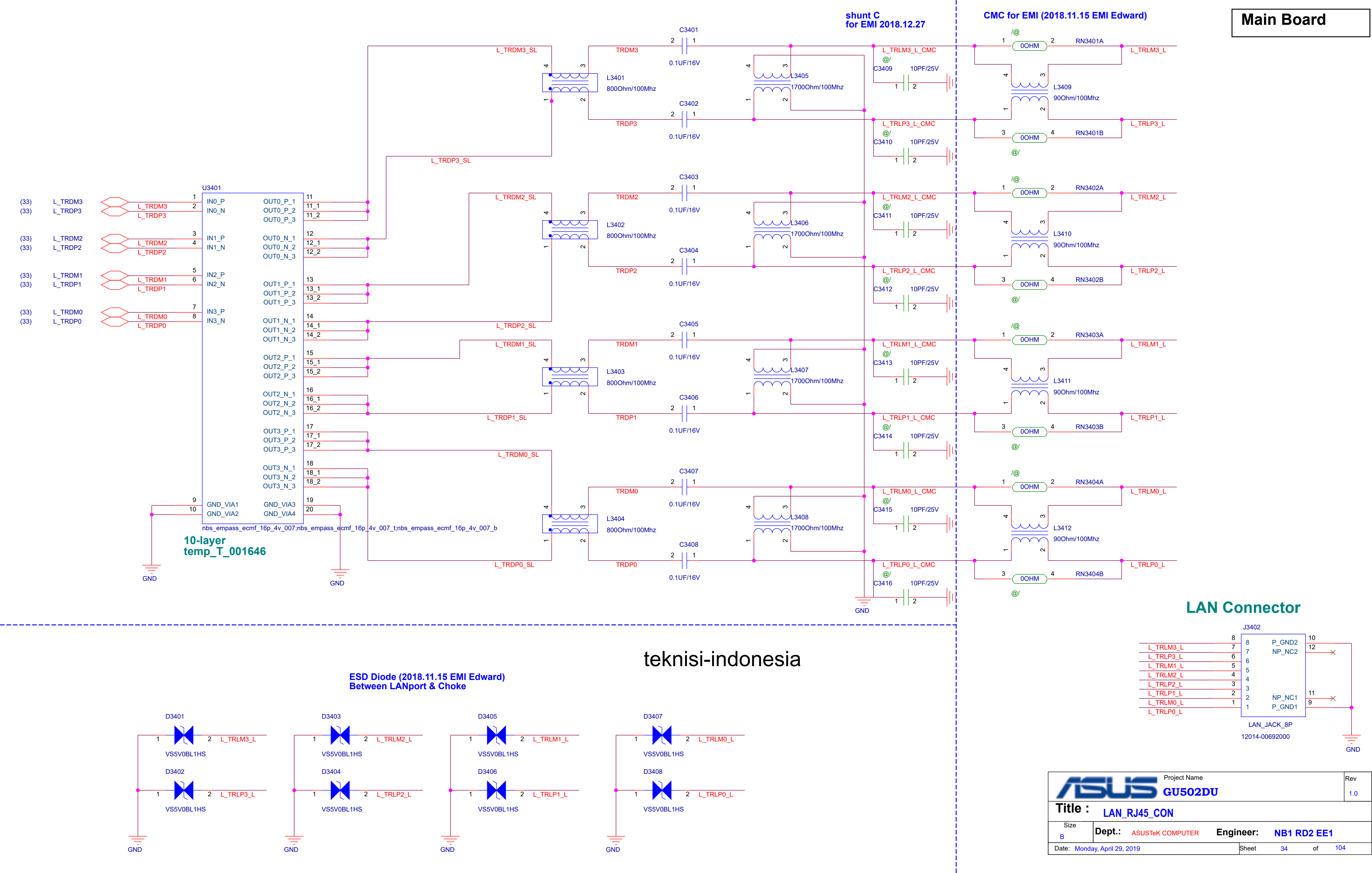
Bypass Cap.

Cbypass, placehold

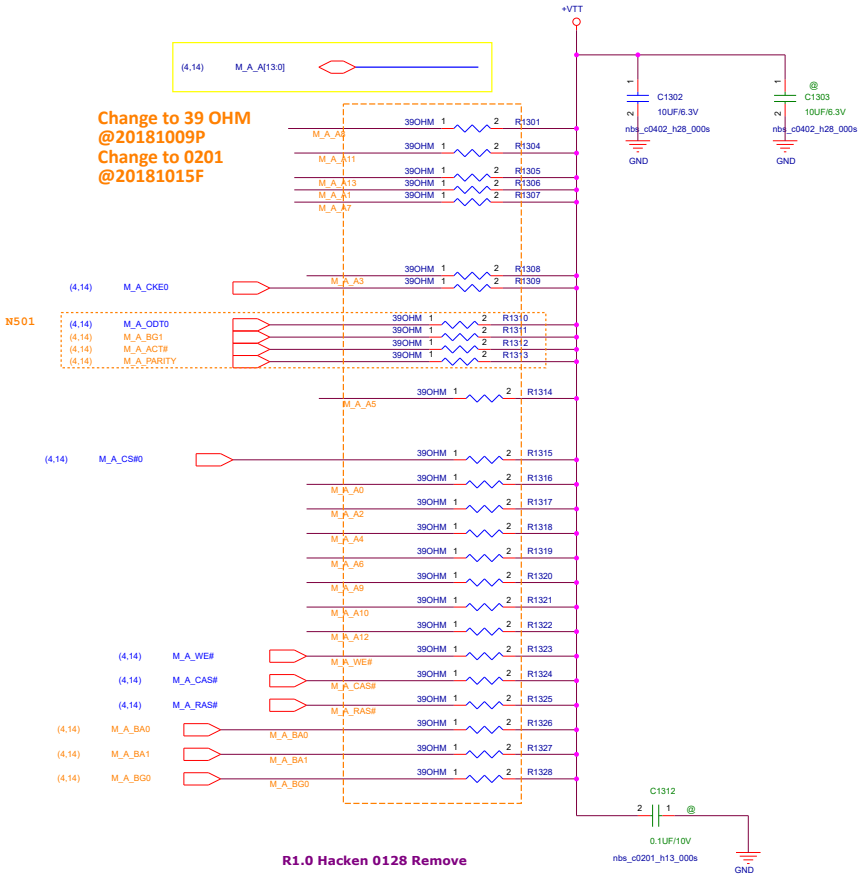
EMI Reserve

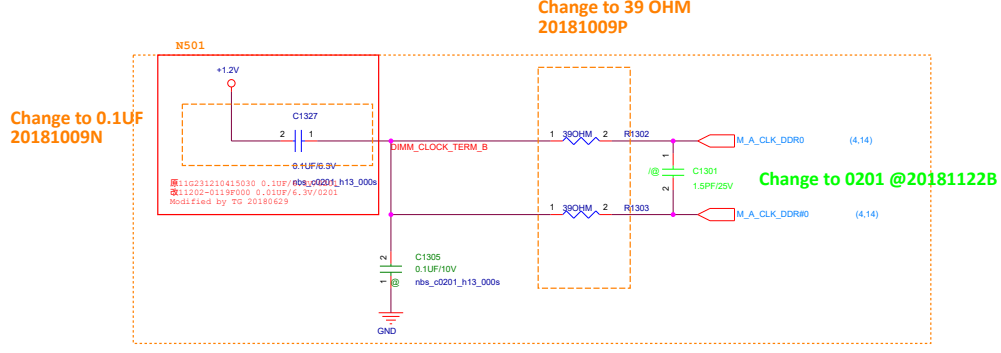
Project Name	GU502DU
Rev	R1.0
Title :	LAN RTL8111GUX-CG
Size	B
Dept.:	ASUSTeK COMPUTER INC.
Engineer:	EE
Date:	Monday, April 29, 2019
Sheet	33 of 104

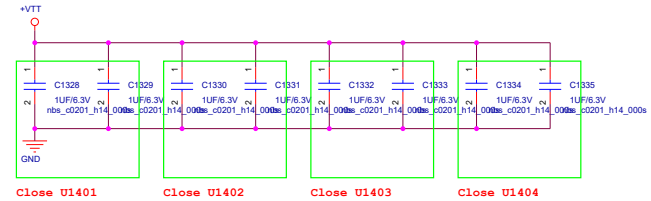
Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, April 29, 2019	Sheet 12 of 104	

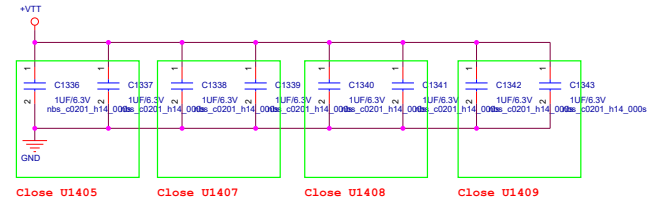

shunt C
for EMI 2018.12.27
CMC for EMI (2018.11.15 EMI Edward)
U3401
IN0_P
IN0_N
IN1_P
IN1_N
IN2_P
IN2_N
IN3_P
IN3_N
OUT0_P_1
OUT0_P_2
OUT0_P_3
OUT0_N_1
OUT0_N_2
OUT0_N_3
OUT1_P_1
OUT1_P_2
OUT1_P_3
OUT1_N_1
OUT1_N_2
OUT1_N_3
OUT2_P_1
OUT2_P_2
OUT2_P_3
OUT2_N_1
OUT2_N_2
OUT2_N_3
OUT3_P_1
OUT3_P_2
OUT3_P_3
OUT3_N_1
OUT3_N_2
OUT3_N_3
GND_VIA1
GND_VIA2
GND_VIA3
GND_VIA4
nbs_empass_ecmf_16p_4v_007;nbs_empass_ecmf_16p_4v_007_t;nbs_empass_ecmf_16p_4v_007_b
10-layer
temp_T_001646
(33) L_TRDM3
(33) L_TRDP3
(33) L_TRDM2
(33) L_TRDP2
(33) L_TRDM1
(33) L_TRDP1
(33) L_TRDM0
(33) L_TRDP0
L_TRDM3_SL
L_TRDP3_SL
L_TRDM2_SL
L_TRDP2_SL
L_TRDM1_SL
L_TRDP1_SL
L_TRDM0_SL
L_TRDP0_SL
L3401 800Ohm/100Mhz
L3402 800Ohm/100Mhz
L3403 800Ohm/100Mhz
L3404 800Ohm/100Mhz
C3401 0.1UF/16V
C3402 0.1UF/16V
C3403 0.1UF/16V
C3404 0.1UF/16V
C3405 0.1UF/16V
C3406 0.1UF/16V
C3407 0.1UF/16V
C3408 0.1UF/16V
TRDM3
TRDP3
TRDM2
TRDP2
TRDM1
TRDP1
TRDM0
TRDP0
L3405 1700Ohm/100Mhz
L3406 1700Ohm/100Mhz
L3407 1700Ohm/100Mhz
L3408 1700Ohm/100Mhz
L_TRLM3_L_CMC
L_TRLP3_L_CMC
L_TRLM2_L_CMC
L_TRLP2_L_CMC
L_TRLM1_L_CMC
L_TRLP1_L_CMC
L_TRLM0_L_CMC
L_TRLP0_L_CMC
C3409 10PF/25V
C3410 10PF/25V
C3411 10PF/25V
C3412 10PF/25V
C3413 10PF/25V
C3414 10PF/25V
C3415 10PF/25V
C3416 10PF/25V
0OHM RN3401A
0OHM RN3401B
0OHM RN3402A
0OHM RN3402B
0OHM RN3403A
0OHM RN3403B
0OHM RN3404A
0OHM RN3404B
L3409 90Ohm/100Mhz
L3410 90Ohm/100Mhz
L3411 90Ohm/100Mhz
L3412 90Ohm/100Mhz
L_TRLM3_L
L_TRLP3_L
L_TRLM2_L
L_TRLP2_L
L_TRLM1_L
L_TRLP1_L
L_TRLM0_L
L_TRLP0_L
GND
LAN Connector
J3402
P_GND2
NP_NC2
NP_NC1
P_GND1
LAN_JACK_8P
12014-00692000
teknisi-indonesia
ESD Diode (2018.11.15 EMI Edward)
Between LANport & Choke
D3401 VS5V0BL1HS L_TRLM3_L
D3402 VS5V0BL1HS L_TRLP3_L
D3403 VS5V0BL1HS L_TRLM2_L
D3404 VS5V0BL1HS L_TRLP2_L
D3405 VS5V0BL1HS L_TRLM1_L
D3406 VS5V0BL1HS L_TRLP1_L
D3407 VS5V0BL1HS L_TRLM0_L
D3408 VS5V0BL1HS L_TRLP0_L

Project Name	GU502DU		Rev 1.0
Title :	LAN_RJ45_CON		
Size B	Dept.: ASUSTeK COMPUTER	Engineer:	NB1 RD2 EE1
Date: Monday, April 29, 2019		Sheet 34	of 104









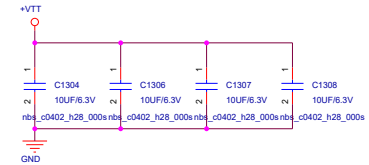


Table 4-25. DDR4 Memory Down Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 Memory Down x8- 8 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x8 DRAM device as possible	64x 1µF (0402) (min of 48 stuffed)	
		Distributed around the DRAM devices	20x 10µF (0603) (min of 12 stuffed)	
	VPP	2 as near each x8 DRAM device as possible	32x 1µF (0402)	
		Distributed around the DRAM devices	10x 10µF (0603)	
	VTT	Distributed along termination resistors	32x 1µF (0402)	
		Distributed evenly across domain	8x 10µF (0603)	

Change@20181220C

Micron 8G
03012-00030700
DDR4 2666 1024MB*8 1.2V FBGA78
MT40A1G8SA-075:E

Samsung 16G
03012-00060000
DDR4 2666 2048MB*8 1.2V FBGA78
K4A8G085WA-BCTD

1Gx8(IO)
Total: 1Gx8ea = 8G

Follow FPS MPDG
Follow GX502預留1.2V pull-H
@20181005H

新增M_A_VREFCA (Follow FX505) and remove page18

Close to VREFCA PIN

10uF*1
1uF*4

Close U1401

Close U1402

Close U1403

Close U1404

Close U1405

Close U1407

Close U1408

Close U1409

Close U1401~U1404 pin J1

Close U1405~U1409 pin J1

DIM Thermal Sensor

Table 4-25. DDR4 Memory Down Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 Memory Down x8- 8 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x8 DRAM device as possible	64x 1µF (0402) (min of 48 stuffed)	
		Distributed around the DRAM devices	20x 10µF (0603) (min of 12 stuffed)	
	VPP	2 as near each x8 DRAM device as possible	32x 1µF (0402)	
		Distributed around the DRAM devices	10x 10µF (0603)	
	VTT	Distributed along termination resistors	32x 1µF (0402)	
		Distributed evenly across domain	8x 10µF (0603)	

Title : DDR4_ON-BOARD_A1
Engineer: EE
GX531GX

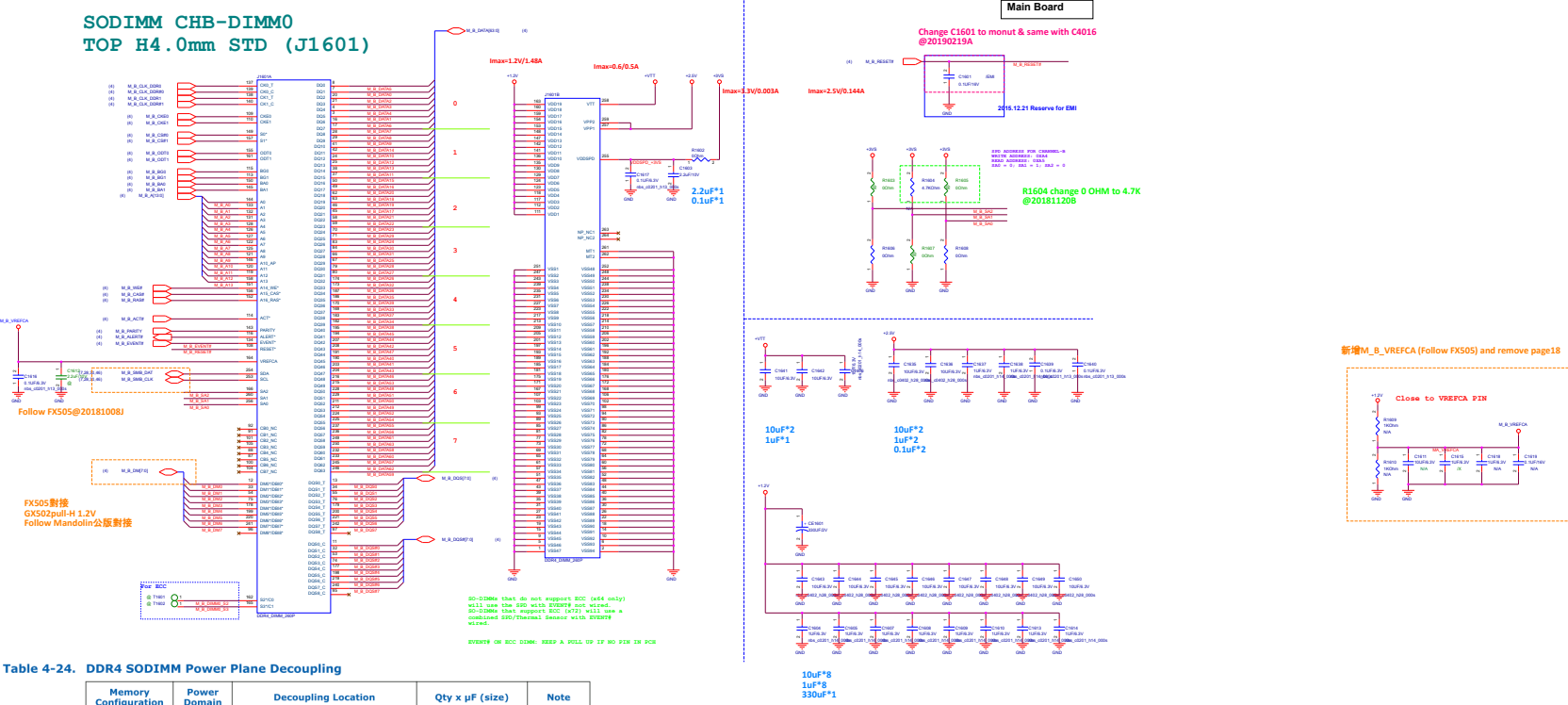


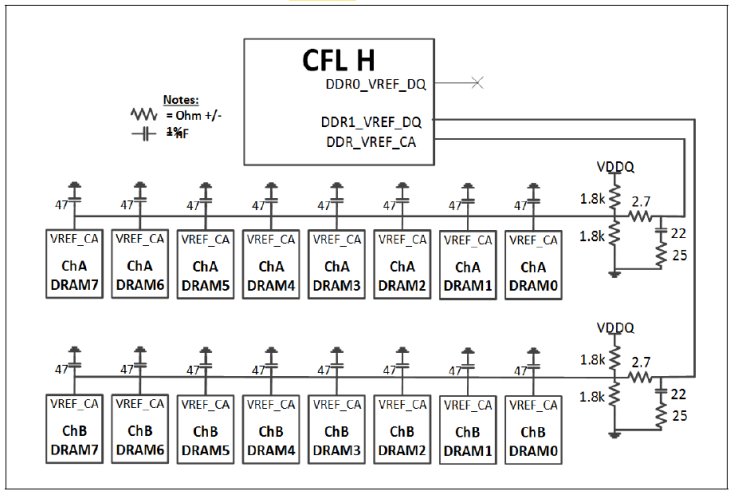
Table 4-24. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM **1DPC**	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Placed on VTT plane close to DIMM, 1 cap stuffed, 1 placeholder	2x 10µF (0603)	
		Placed on VTT plane close to DIMM	4x 1µF (0402)	
	VPP	DIMM Pin side, 1 per DIMM	2x 10µF (0603)	
		DIMM Pin side, 1 per DIMM	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	2x 0.1µF (0402)	
		Place close to DIMM	2x 2.2µF (0402)	

DDR4 - 2666MHz (8G)
1st : Hynix - 03A08-00051400
2nd : Samsung - 03A08-00051300
DDR4 - 2666MHz (16G)
1st : Hynix - 03A08-00061400
2nd : Samsung - 03A08-00061500

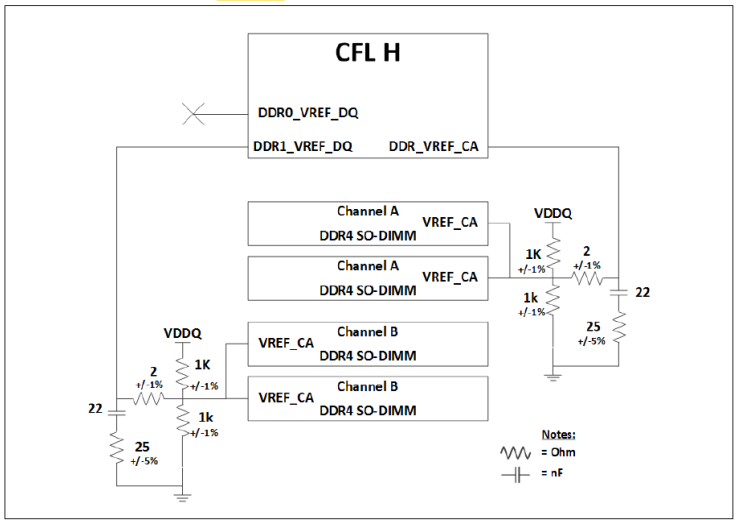
Memory Down Vref

Figure 4-24. CFL-H DDR4 x8 Memory Down V_{REF-CA} Overview



SO-DIMM1 Vref

Figure 4-22. CFL-H DDR4 SO-DIMM V_{REF-CA} Overview

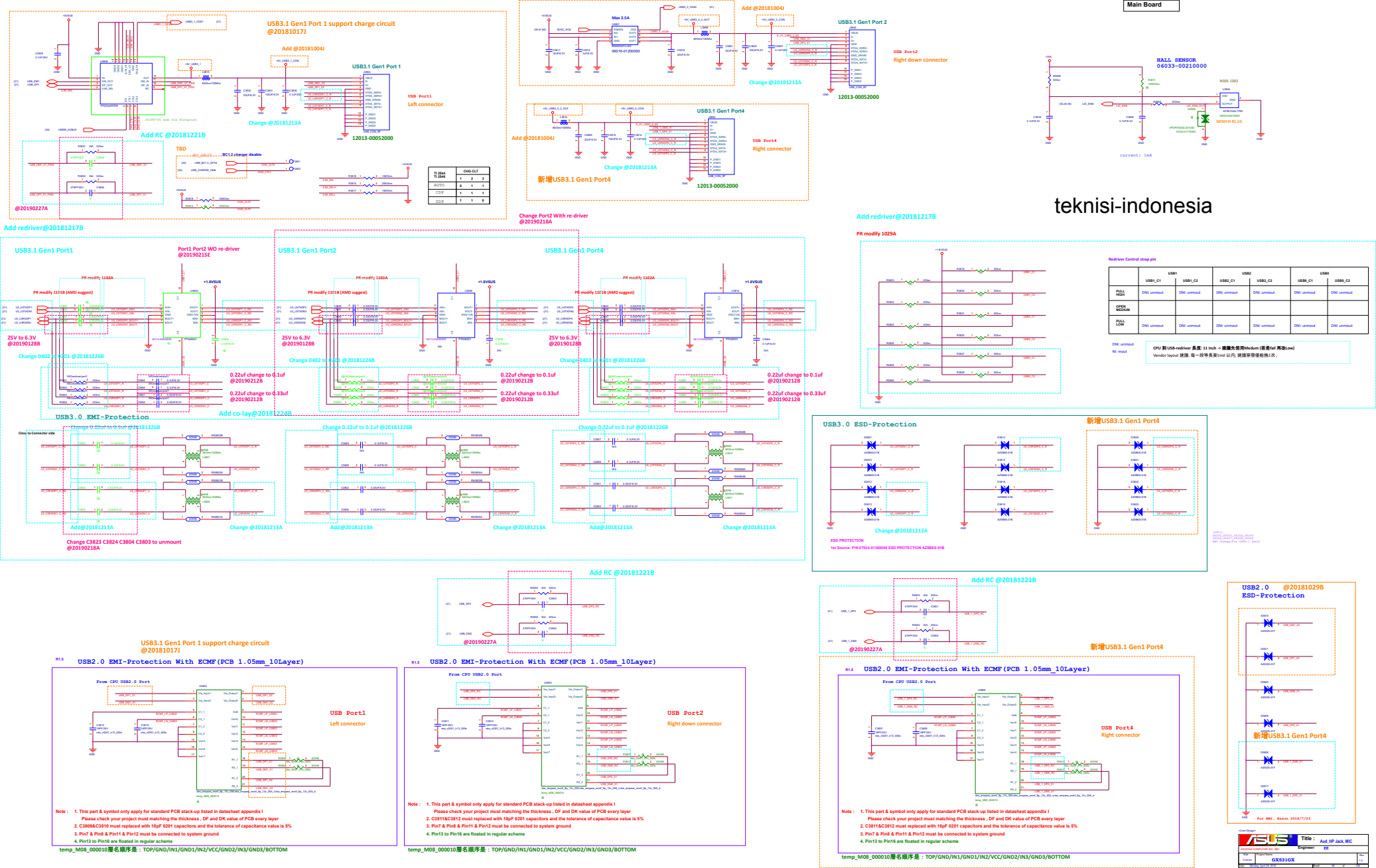


Project Name: GX531GX		Rev: 1.0
Title : DIM_CA/DQ Voltage		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Monday, April 29, 2019	Sheet 18 of 104	

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, April 29, 2019	Sheet 20 of 104	

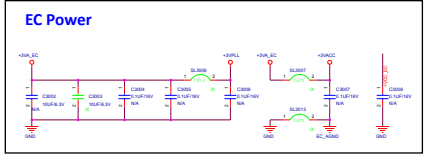
Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, April 29, 2019	Sheet 26 of 104	

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, April 29, 2019	Sheet 27 of 104	


Main Board
USB3.1 Gen1 Port 1 support charge circuit @20181017J
Add @20181004J
USB3.1 Gen1 Port 1
USB Port1
Left connector
12013-00052000
Change @20181213A
Add RC @20181221B
TBD
@20190227A
Add redriver@20181217B
USB3.1 Gen1 Port 2
USB Port2
Right down connector
12013-00052000
Change @20181213A
USB3.1 Gen1 Port4
USB Port4
Right connector
新增USB3.1 Gen1 Port4
12013-00052000
Change @20181213A
Add @20181004J
Change Port2 With re-driver @20190218A
HALL SENSOR
06033-00210000
NS01 1202
GX501W1 R1.1G
current: 1mA
teknisi-indonesia
USB3.1 Gen1 Port1
Port1 Port2 WO re-driver @20190215E
USB3.1 Gen1 Port2
USB3.1 Gen1 Port4
PR modify 1102A
PR modify 1101B (AMD suggest)
25V to 6.3V @20190128B
Change 0402 to 0201 @20181226B
0.22uf change to 0.1uf @20190212B
0.22uf change to 0.33uf @20190212B
Add co-lay@20181224B
USB3.0 EMI-Protection
Change 0.22uf to 0.1uf @20181226B
Change C3823 C3824 C3803 to unmount @20190218A
Add@20181213A
Change @20181213A
Add redriver@20181217B
PR modify 1029A
Redriver Control strap pin
USB3.0 ESD-Protection
新增USB3.1 Gen1 Port4
ESD PROTECTION
1st Source: P/N:07824-01360000 ESD PROTECTION AZ5865-01B
USB2.0 EMI-Protection With ECMF(PCB 1.05mm_10Layer)
From CPU USB2.0 Port
USB Port1
Left connector
USB Port2
Right down connector
USB Port4
Right connector
Note : 1. This part & symbol only apply for standard PCB stack-up listed in datasheet appendix I
Please check your project must matching the thickness , DF and DK value of PCB every layer
2. C3809&C3810 must replaced with 18pF 0201 capacitors and the tolerance of capacitance value is 5%
3. Pin7 & Pin8 & Pin11 & Pin12 must be connected to system ground
4. Pin13 to Pin16 are floated in regular scheme
temp_M08_000010層名順序是：TOP/GND/IN1/GND1/IN2/VCC/GND2/IN3/GND3/BOTTOM
USB2.0 @20181029B
ESD-Protection
新增USB3.1 Gen1 Port4
For EMI , Kason 2018/7/25
Title : Aud_HP Jack, MIC
Engineer: EE
GX531GX

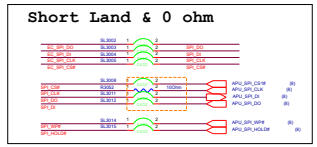
EC Chip - IT8225

EC Power



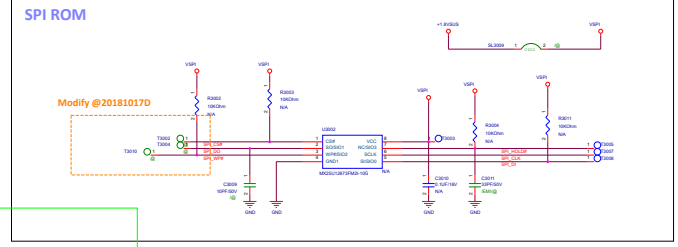
SPI_CLK 10k change to 10 OHM @20181029G

Short Land & 0 ohm



SPI ROM

Modify @20181017D



VCC => +3VS system power ; LPC
VSTBY=>+3VA_EC ;Power supply of EC power

+3VACC==+3VA_EC,
+3VAPLL==+3VA_EC,0906

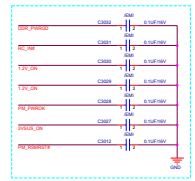
Follow GX502
@20181009E

@20181025G

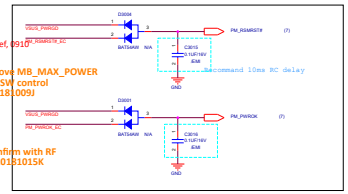
Add FAN_V_Switch @20181218C

Change netname @20181127A

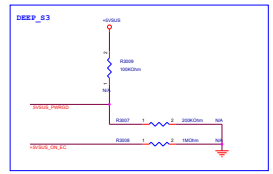
Add @20181219B (EMI request)



C3015 Change to mount @20181219B



C3016 Change to mount @20181219B



Remove EC_OV_DDR
@20181009E

Remove TP_PS2_CLK &DAT
@20181009E

Change PS_ON to PS_ON_EC @20181023D

PM_PWROK_EC del intersheet ref, 0910

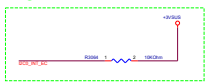
TBD

Remove MB_MAX_POWER
@20181009J

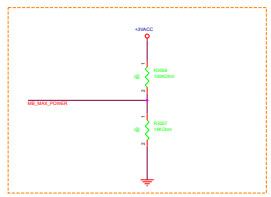
Confirm with RF
@20181015K

Remove SUSC_EC#
@20181016C

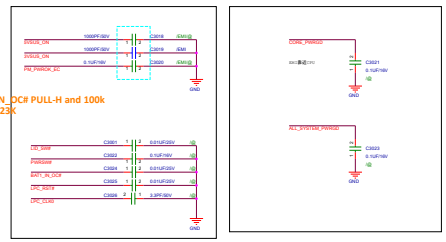
Add @20181108C



Add @20181023A



C3019 Change to mount @20181219B



Del 1.8V_ON_EC NET, 0910

Change PS_ON to PS_ON_EC
@20181023D

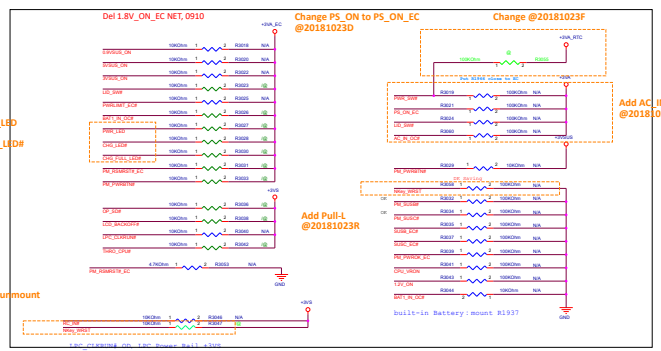
Change @20181023F

Add AC_IN_DC# PULL-H and 100k
@20181023K

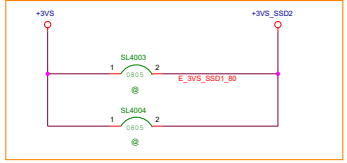
Add Pull-L
@20181023R

Change PWR_LED# to PWR_LED
CHG_LED#_O to CHG_LED#
CHG_LED#_W to CHG_FULL_LED#
@20181017E

Change netname and unmount
@20181017E



built-in Battery : mount R1937



Follow GX502_1002_2330

CPU PCIE

2018/7/20
PR need to modify to short land

2st NGFF PCIE x2

Remove MUX @20181102C

PCIE Lane1

PCIE Lane0

(3) PCIE_SSD2_RXN5
(3) PCIE_SSD2_RXP5
(3) PCIE_SSD2_TXN5
(3) PCIE_SSD2_TXP5
(3) PCIE_SSD2_RXN4
(3) PCIE_SSD2_RXP4
(3) PCIE_SSD2_TXN4
(3) PCIE_SSD2_TXP4
(8) PCIE_SSD2_CLKN
(8) PCIE_SSD2_CLKP

R4005 1 2 0Ohm N/A
R4017 1 2 0Ohm N/A
PCIE_SSD2_RXN4_R
PCIE_SSD2_RXP4_R

R4009 1 0Ohm N/A
R4004 1 0Ohm 2
PCIE_SSD2_CLKN_R
PCIE_SSD2_CLKP_R

For AMD checklist @20181018H

Follow FX505DY & 公板 @20181015J

+3VS_SSD2
R4001 10KOhm
DAS_DSS_LED2#
SATA2_DEVSLP_C
NGFF2_PERST#
NGFF2_PEWAKE#
NGFF2_SUSCLK
GND

J4001

MINI_PCI_SIR_REMOVE

J4001_NGFF M-KEY PCIEx4 Connector H=5.0mm

1st Source: P/N:12003-00162500 ARGOSY/NASM0-S6701-TS50

C4002 8PF/25V
C4003 10UF/6.3V
C4004 10UF/6.3V
C4005 10UF/6.3V
C4006 10UF/6.3V
C4007 10UF/6.3V
C4011 0.1UF/6.3V
C4012 0.1UF/6.3V
C4013 0.1UF/6.3V
C4014 0.1UF/6.3V
C4015 0.1UF/6.3V

R4008 1 N/A 2 100KOhm +3VS_SSD2
N/A
3
BAT54AW
2 D4002
PCIE_SSD_RST# (7,41)
BUF_PLT_RST# (7,32,33,41,53,69,70)
CLKREQ3_SSD2# (8)
PCIE_WAKE# (7,33,41,53,70)

Q4001 ZN7002K
@

Follow FX505DY &公板 @20181015H

CLKREQ0_SSD1# Change to CLKREQ3_SSD2# @20190129A

R4012 1 @ 2 0Ohm +3VS_SSD2
SUS_CLK (8,41,53)

Add @20181013C

改不上件 @20181015H

EMI

NGFF2_PERST#
D4001 VPORT0402L331V05 /@
GND

NGFF1 Device Sleep

SATA2_DEVSLP_C
R4014 0Ohm
/Enable Devslp
GND

Delete NGFF2_DEVSLP @20181107A

Add @20181219B (EMI request)

C4017 /EMI 0.1UF/16V
C4016 /EMI 0.1UF/16V
PCIE_WAKE#
GND

Remove MUX @20181102C

+3VS
R4030 1 @PCIE_ 2 0Ohm
R4060 10KOhm
D4006
BAT54AW
R4022 1 @PCIE_ 2 0Ohm
(41) DAS_DSS_LED1#
DAS_DSS_LED1#
DAS_DSS_LED2#
DAS_DSS_LED# (56)

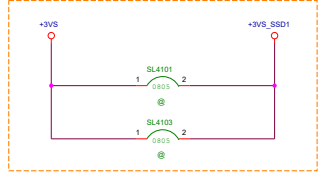
Follow GX502_1002_2330

H4002 N/A
CT236CB176D146
13020-01371400
GND

Project Name	GX502GX	Rev	1.0
Title :	NGFF_SSD_PCIE_CON		
Size	Custom	Dept.: ASUSTeK COMPUTER	Engineer: NB1 RD2 EE1
Date:	Monday, April 29, 2019	Sheet 40	of 104

< KEY-M NGFF_SSD_PCH >

Follow GX502_1002_2330



1nd NGFF PCIE x2

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Remove MUX @20181102C

2018/7/20
PR need to modify to short land

@20181015P

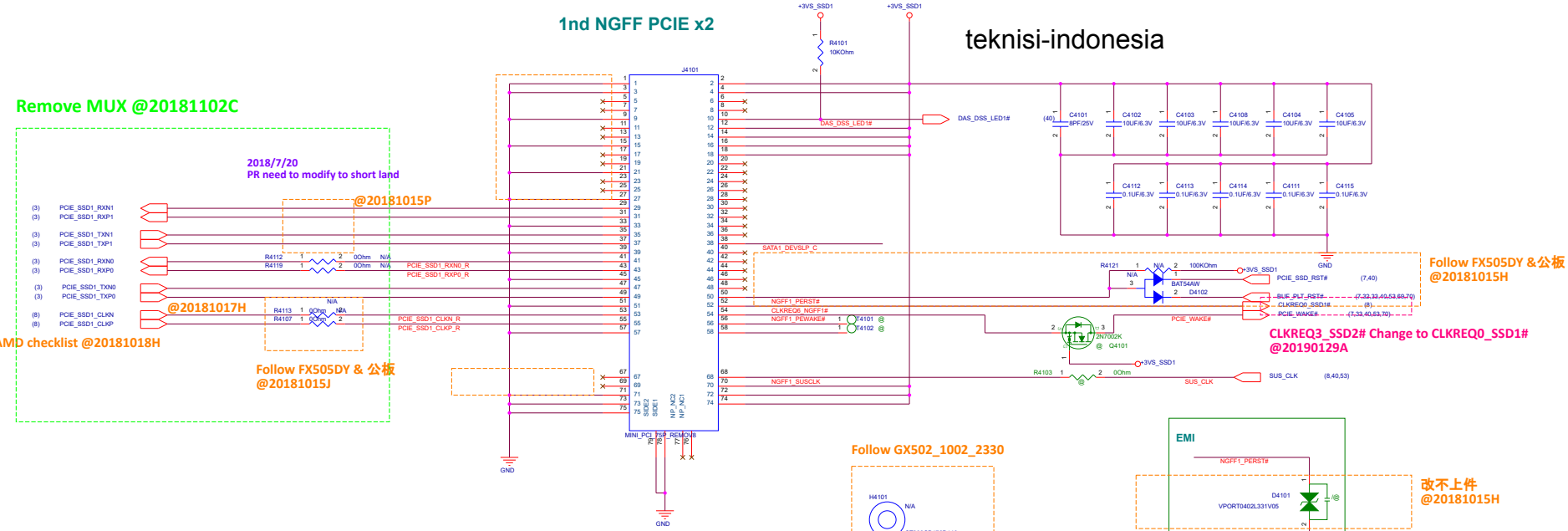
PCIE Lane5

PCIE Lane4

@20181017H

For AMD checklist @20181018H

Follow FX505DY & 公板
@20181015J

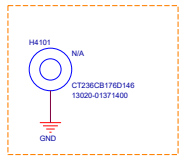


Follow FX505DY &公板
@20181015H

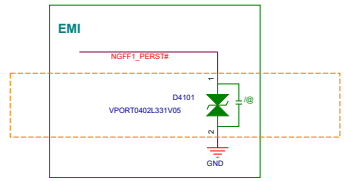
CLKREQ3_SSD2# Change to CLKREQ0_SSD1#
@20190129A

New PN : 12003-00079400

Follow GX502_1002_2330



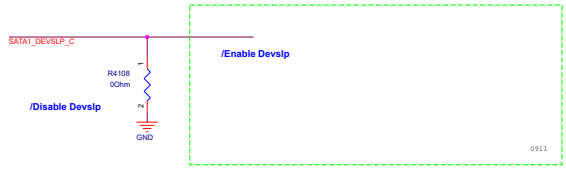
EMI



改不上件
@20181015H

Remove MUX @20181102C

HW_Control NGFF Device Sleep



Close to Device connector

Delete NGFF1_DEVSLP @20181107A

<Core Design>

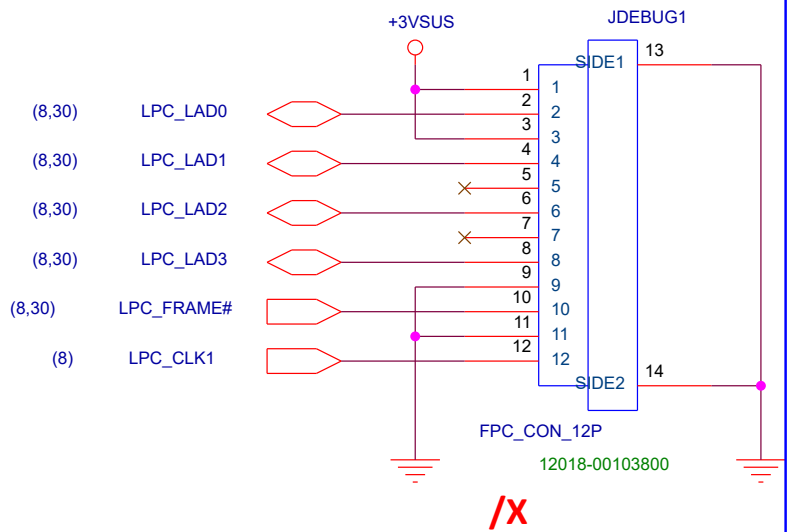
ASUSTeK COMPUTER	Title : NGFF_SSD_CPU		
	Engineer: EE		
Size: C	Project Name: GX502GX		Rev: 1.0
Date: Monday, April 29, 2019	Sheet 41 of 104		

HDMI Switch

ASUS	Project Name: GX502GX	Rev: 1.0
Title : CB_CON		
Size: A3	Dept.: MOBATHE COMPUTER	Engineer: EE
Date: Monday, April 09, 2018	Sheet 43 of 104	

LPC Debug Port

2017/11/10



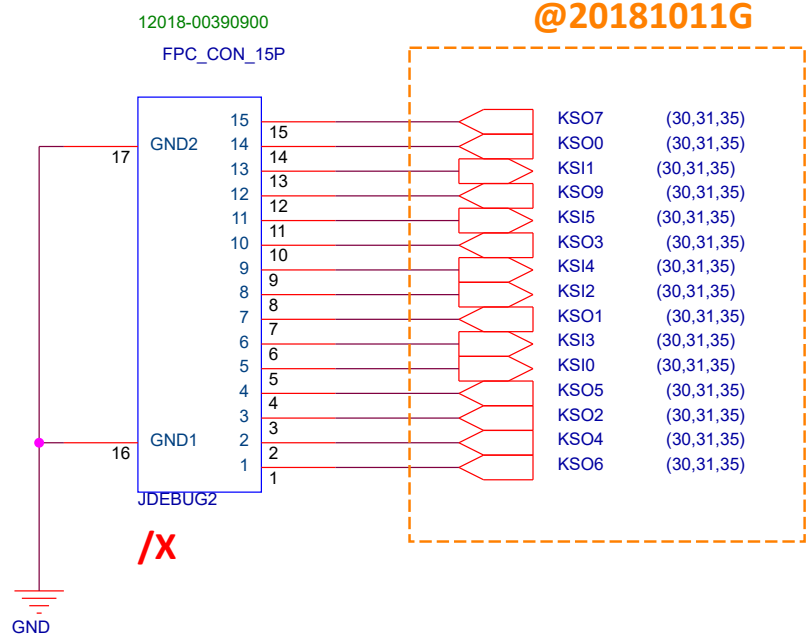
/X

1st: 12018-00103800
2nd :12018-00103300

2017/11/10

Flash BIOS

Rename
@20181011G

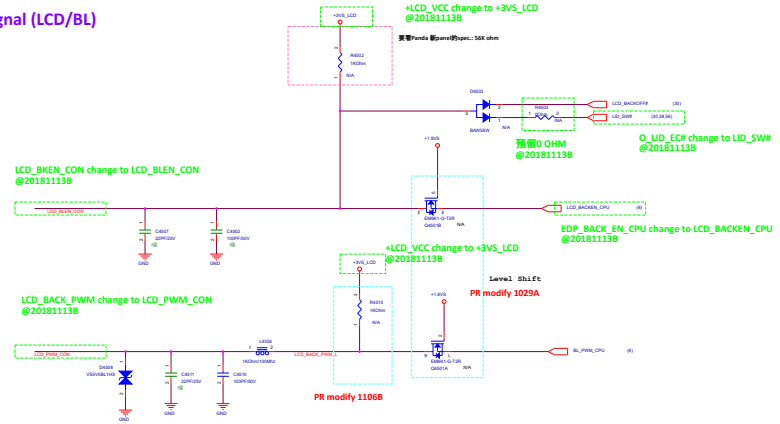


/X

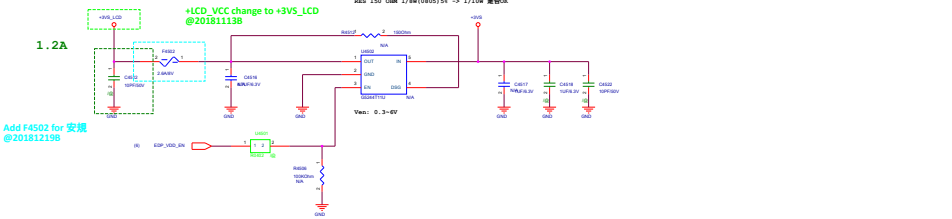
<Core Design>

ASUSTeK COMPUTER	Title : DEBUG_LPC	
	Engineer: EE	
Size: A	Project Name: GX502GX	Rev: 1.0
Date: Monday, April 29, 2019	Sheet 44 of 104	

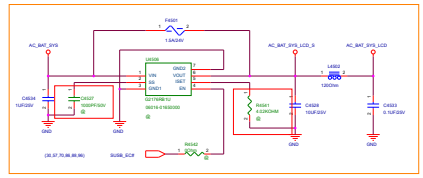
Controll Signal (LCD/BL)



LCD VDDEN / +3VS_LCD

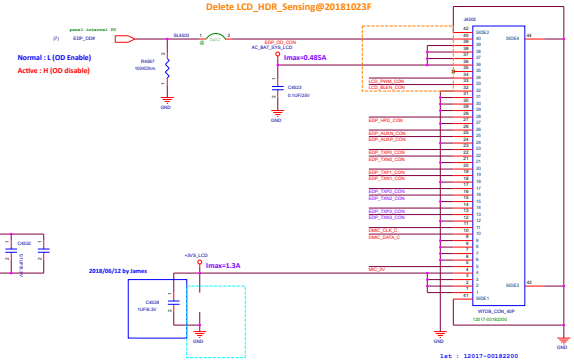


Panel BL Power

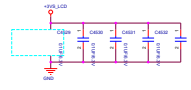


GT53V1 Morgan

Delete LCD_HDR_Sensing@20181023F



Remove C4503 for EMI LAN
@20181227G

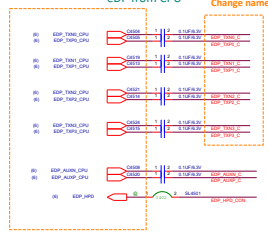


Remove C4506 for EMI LAN
@20181227G

Rename
@20181015B

eDP from CPU

Change name Re-timer@20181023F

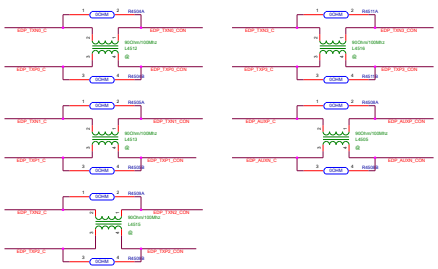


Delete Re-timer@20181023F

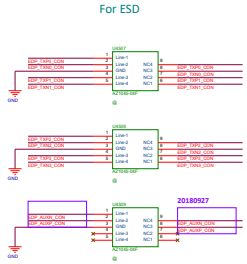
Panel Vender : AUO
PN : B156HAN08.2(HW_2A)

PIN NO	Symbol	PIN NO	Symbol
1	NC	24	LCD GND
2	H_GND	25	LCD GND
3	Lane3_N	26	LCD GND
4	Lane3_P	27	HPD
5	H_GND	28	BL_GND
6	Lane2_N	29	BL_GND
7	Lane2_P	30	BL_GND
8	H_GND	31	BL_GND
9	Lane1_N	32	BL_Enable
10	Lane1_P	33	BL PWM DIM
11	H_GND	34	NC
12	Lane0_N	35	NC
13	Lane0_P	36	BL_PWR
14	H_GND	37	BL_PWR
15	AUX_CH_P	38	BL_PWR
16	AUX_CH_N	39	BL_PWR
17	H_GND	40	NC
18	LCD_VCC		
19	LCD_VCC		
20	LCD_VCC		
21	LCD_VCC		
22	LCD_Self_Test		
23	LCD GND		

For EMI



For ESD



Rename
@20181017H

eDP_HPD (CPU)

Delete Re-timer@20181023F

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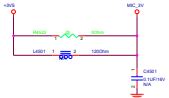
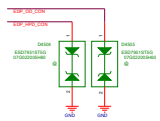
MIC module

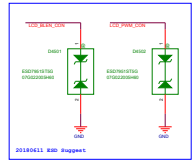


MIC

C4556 change to unmunt
R4507(10ohm) change to L4503
@20190102A

For ESD





Delete @20181022M

Title :	CRT_eDP		
Engineer:	EE		
Project Name	GX502GX		Rev 1.0
Date: Monday, April 29, 2019		Sheet 45 of 108	

N_KEY_IT8299E

Nkey_Power

For EC Reset N_key

Pull up

Change DSW to SUS @20181009

Add @20190422A

Change DSW to SUS @20181009

+5VS_LED_KB

Change DSW to SUS @20181009

+3VSUS_NKeyPWR

Change DSW to SUS @20181009

Add @20190422A

Change DSW to SUS @20181009

Add C3502,C3503,C3504,C3509 C3510,C3511,C3512,C3513 @20181116A

@20190227A

IT8299E

Change DSW to SUS @20181009

Change USB_1_DP0 to USB_DP0 @20181224A

4 ZONE RGB@20181105A

Remove 4 ZONE RGB@20181213A

Remove 4 ZONE RGB@20181213A

Add C3546 @20190131A Unmount @20190201A

Follow GX502 1011_1700 @20181015E

Remove 4Zone RGB @20181213A

@20190227A

C3546 change to 10uf @20190422A

Remove IT8299E_GPB0-7, GPA0-3 @20181017E

Remove 4Zone RGB@20181213A

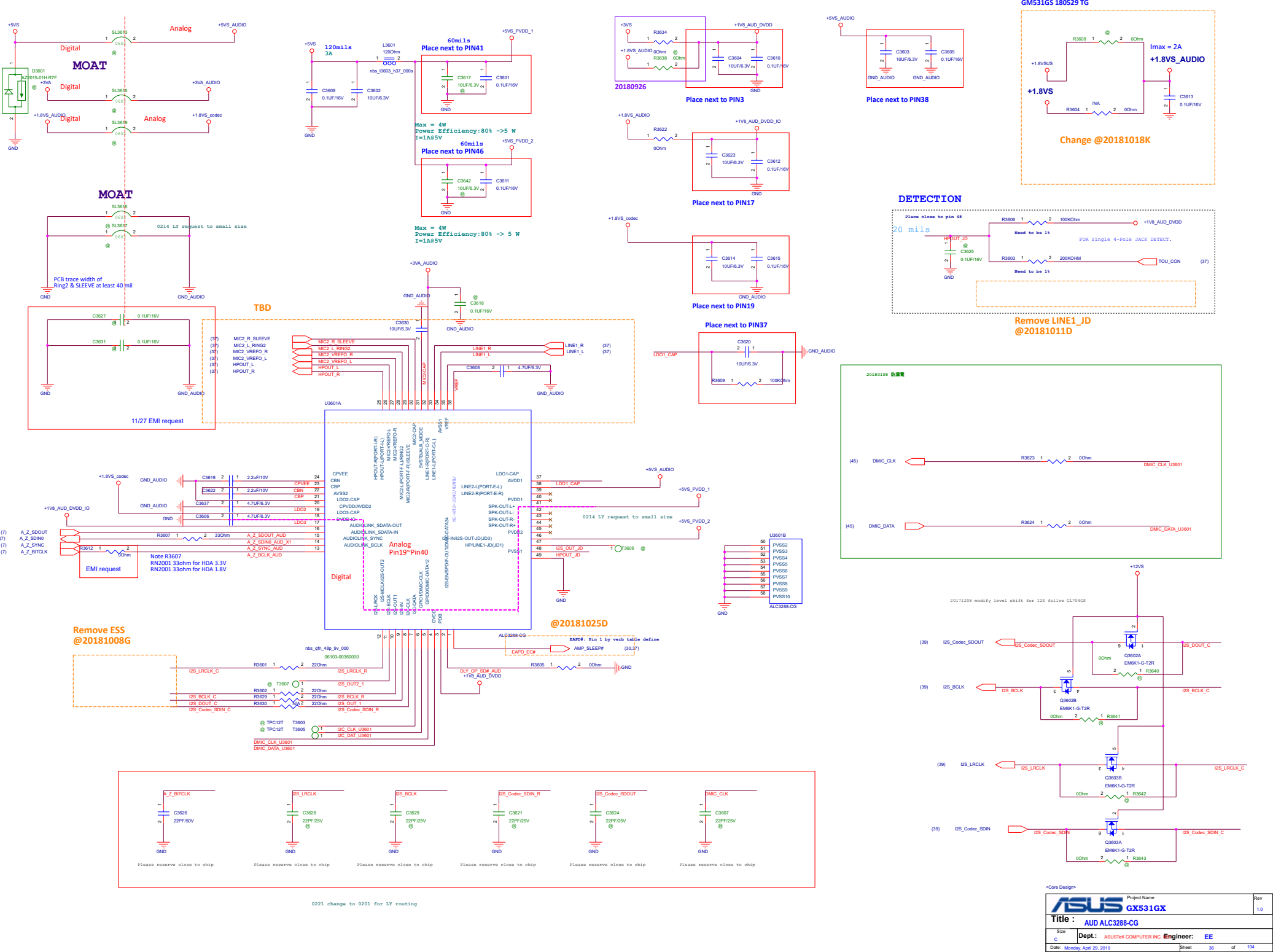
Modfify @20181017K

Add C3547 @20190131A Unmount @20190201A

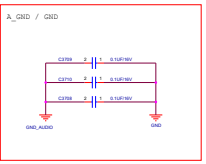
For ESD

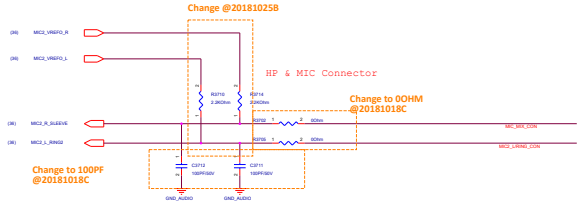
Remove KB RGB 4 Zone LED@20181213A

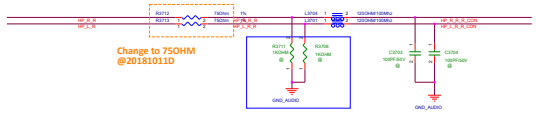
Title :	LAN_*****
Engineer:	Gaming RD
Project Name	G711GW
Size	Custom
Rev	1.0
Date:	Monday, April 29, 2019
Sheet	35 of 104

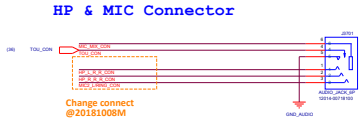

GM531GS 180529 TG
MOAT
Digital
Analog
Change @20181018K
DETECTION
Remove LINE1_JD
@20181011D
TBD
11/27 EMI request
Place next to PIN41
Place next to PIN46
Place next to PIN3
Place next to PIN38
Place next to PIN17
Place next to PIN19
Place next to PIN37
Max = 4W
Power Efficiency:80% ->5 W
I=1A@5V
Max = 4W
Power Efficiency:80% -> 5 W
I=1A@5V
PCB trace width of
Ring2 & SLEEVE at least 40 mil
0214 LY request to small size
Analog
Pin19~Pin40
Digital
EMI request
Note R3607
RN2001 33ohm for HDA 3.3V
RN2001 33ohm for HDA 1.8V
Remove ESS
@20181008G
@20181025D
0221 change to 0201 for LY routing
20171208 modify level shift for I2S follow GL704GS
Project Name
GX531GX
Title :
AUD ALC3288-CG
Dept.:
ASUSTeK COMPUTER INC.
Engineer:
EE
Date:
Monday, April 29, 2019
Sheet
36
of
104

Headphone&MIC



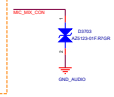




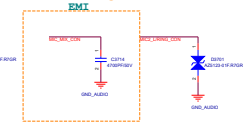


Remove EXTERNAL MIC
@20181009A

Remove
@20181017A

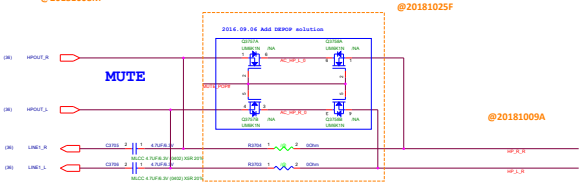


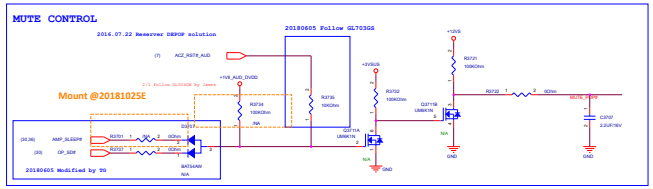
Remove
@20181017A



Remove ESS
@20181008M

@20181025F





@20181009F

ESS ES9118EQ

Remove ESS
@20181008G

Remove ESS
@20181008M

ASUS	Project Name: GX531GX		Rev: 1.0
Title : AUDIO ALC3236-CG/VB2 Jack			
Size: D	Dept.: ASUSTeK COMPUTER INC.	Engineer:	
Date: Monday, April 29, 2019	Sheet: 37	of: 106	

Main Board

Internal Regulator option

LDO OUT

LDO IN

+1.8VSUS

+3VS_OVDD

+1VS_RGOUT

C4801 10UF/6.3V

C4802 10UF/6.3V

L4801 600ohm/100MHz

L4802 600ohm/100MHz @HDMI

C4801 close to IC as close as possible

C4802 close to IC as close as possible

預留0歐電阻 option.

L4802 Change netname +1.8VS to +3VS_OVDD
Follow FX505DY 1003C@ 20181004D

Retimer

+3VS_OVDD

+1VS_IVDD

+1VS_RGOUT

+3VS_RAVCC

+1VS_TAVCC

HDMI_TXP2 HDMI_TXN2 HDMI_TXP1 HDMI_TXN1 HDMI_TXP0 HDMI_TXN0 HDMI_CLKP HDMI_CLKN

HDMI_TXP2_C HDMI_TXN2_C HDMI_TXP1_C HDMI_TXN1_C HDMI_TXP0_C HDMI_TXN0_C HDMI_CLKP_C HDMI_CLKN_C

HDMI_TXP2_R HDMI_TXN2_R HDMI_TXP1_R HDMI_TXN1_R HDMI_TXP0_R HDMI_TXN0_R HDMI_CLKP_R HDMI_CLKN_R

HDMI_DDCCAT HDMI_DDCCLK HDMI_DDC_CAT_R HDMI_DDC_CLK_R

HDMI_RGIN

T4801 TPC28T

T4802 TPC28T

U4801A

HDMI_TXP2 HDMI_TXN2 HDMI_TXP1 HDMI_TXN1 HDMI_TXP0 HDMI_TXN0 HDMI_CLKP HDMI_CLKN

+1VS_TAVCC

+3VS_TVCC +3VS_RVCC

R4805 TRKOhm

+3VS_MCUVDD

GPIO

HPD_SINK

U4801B

IT8631TFN 06111-00110000

Delete@20181015M

R4820 Unmount @20181114A

HDMI_HPD_TO_CPU

R4808 100KOhm HDMI

pull down電阻R4816改為上件47K @20181114A

HW strapping

Output Swing	GPIO	TRIB3
Level 1 (Lowest)	0	0
Level 2 (Default)	0	1
Level 3	1	0
Level 4 (Highest)	1	1

Level 2(default)

R4831 22KOHM GPIO

R4830 100KOhm

R4822 22KOHM

R4824 100KOhm

UNGHG for driving control
High --> High driving
Low --> Normal driving

LX4801 LX4802 LX4803 LX4804 change to 09G092120001 @20190213A

RN4802 RN4803 RN4804 RN4805 change to unmount @20190213A

DDC LEVEL SHIFT

R4811 & R4812 change 2.2K to 10K @20190218A

R4811 10KOhm N/A

R4812 10KOhm N/A

UM6K31N Q4602A

R4813 2.2KOhm N/A

R4814 2.2KOhm N/A

R4813,R4814 10k change to 2.2k (FAE) @20181114A

Add 22OHM (FAE) @20181114A

HDMI_DDCCLK HDMI_DDCDAT

HDMI_SCL_CON HDMI_SDA_CON

R4804 R4809 220Ohm

FW update path

R4817 R4818 220Ohm

ISPSCL ISPSDA

HDMI PWR_+5VS_HDMI

+5VS

R4802 100KOhm

+5VS_F

Q4802 SI2336DDS-T1-GE3

F4801 0.75A/13.2V 0ZCS0175FF2E10

+5VS_HDMI

L4806 600ohm/100MHz N/A

C4808 0.1UF/16V

JP4801 1MM_OPEN_SML

Modify @20181016J

Remove @20181108B

HDMI Conn.

HDMI_TXP2_CON HDMI_TXN2_CON HDMI_TXP1_CON HDMI_TXN1_CON HDMI_TXP0_CON HDMI_TXN0_CON HDMI_CLKP_CON HDMI_CLKN_CON HDMI_SCL_CON HDMI_SDA_CON +5V_HDMI HDMI_HPD_CON

J4801 HDMI_CON_19P 12022-001120000

P_GND1 P_GND3 P_GND4 P_GND2

R4803 47KOhM N/A

D4803 TVLD4020140-1

C4817 0.1UF/16V

Add C4817 @20181114A

RN4802,RN4803,RN4804,RN4805 change to mount
LX4801,LX4802,LX4803,LX4804 change to unmount
@20181101B

Remove R4815,R4804,R4819,R4823 (原本預留不上) @20181101A

HDMI EMI

HDMI_CLK- HDMI_CLK+ HDMI_TXD- HDMI_TXD+ HDMI_TXC- HDMI_TXC+ HDMI_TXB- HDMI_TXB+

RN4802 RN4803 RN4804 RN4805 80ohm

HDMI_CLK_CON HDMI_TXD_CON HDMI_TXC_CON HDMI_TXB_CON

R4815 470OHM @EMI

LX4801 LX4802 LX4803 LX4804 120OHM/100MHz

5 ohm + driving 能力(level 2)

Add R4815,R4810,R4819,R4823 @20181114A

Remove R4810,R4819,R4823 @20181121A (FAE)

C_M_Choke_..._0_09G092120001

Change to 0 OHM (FAE) @20181114A

HDMI_SCL_CON HDMI_SDA_CON

D4801 VSSV5BC1GS

D4802 VSSV5BC1GS

U4802 U4803 AZ1045-04F @EMI

I2C

+3VS_OVDD

R4805 10KOhm T4SDA

R4807 10KOhm T4SCL

R4808 10KOhm HDMI_DDC_DAT_R

R4809 10KOhm HDMI_DDC_CLK_R

R4810 10KOhm PCADR

PCADR:
Control of serial programming device address
0:0x70 (default , internal pull down)
1:0x7A

ASUS Project Name GX502GX Rev 1.0

Title : HDMI

Size: D Dept.: ASUSTeK COMPUTER Engineer: EE

Date: Monday, April 29, 2019 Sheet 48 of 104

SPK Power

AC_BAT_SYS — R3901 1 2 0Ohm N/A — +PVDD_AMP
R3931 1 2 0Ohm N/A

IO Power

+1.8VSUS — R3907 1 2 @ 0Ohm — +1.8V_3.3V_IOVDD
+3VSUS — R3921 1 2 0Ohm
0926 Modify
5mA
C3907 1UF/6.3V
GND

INTERNAL SPK1 Conn.

SPK L+ L- R+ R- trace width
Speaker 8 ohm
Max = 1.5W / Channel
I = 0.43 A

(Smart AMP MAX 2A/Channel) ==> 60mils

H_SPKL-_CON	R3928	0Ohm	ADR_AMP
H_SPKL+_CON	R3929	0Ohm	J3901_pin4
H_SPKR-_CON	R3926	0Ohm	J3901_pin3
H_SPKR+_CON	R3927	0Ohm	J3901_pin2
			J3901_pin1

J3901 — SIDE2 / SIDE1 — WTOB_CON_6P — 12017-00011400 — GND

Keep for test @20181017A

+PVDD_AMP
C3903 22UF/25V
C3904 22UF/25V
C3905 0.1UF/50V
GND
+1.8V_3.3V_IOVDD
C3911 4.7UF/10V
C3910 0.1UF/16V
GND

C3947 0.22UF/50V — H_SPKL- — GND
C3944 0.22UF/50V — H_SPKR- — GND
C3938 0.22UF/50V — H_SPKL+
C3939 1UF/16V — R3913 1KOHM — ADR_AMP — GND

U3905A (TAS5825MRHBR)
GND1 PGND4 PGND3 OUT_A- BST_A- BST_B- OUT_B- PGND2 PGND1
BST_A+ OUT_A+ PVDD1 PVDD2 DGND DVDD VR_DIG ADR
BST_B+ OUT_B+ PVDD4 PVDD3 AGND AVDD GVDD PDN#
GPIO0 GPIO1 GPIO2 LRCLK SCLK SDIN SDA SCL

+1.8V_3.3V_IOVDD
R3924 @ 10KOhm — AMP_GPIO0
R3925 @ 10KOhm — AMP_GPIO2

C3946 0.22UF/50V — H_SPKR+
C3942 1UF/16V
C3943 1UF/16V
AMP_PDN#

+PVDD_AMP
C3945 0.1UF/50V
C3914 22UF/25V
C3912 22UF/25V
GND

+1.8V_3.3V_IOVDD
R3930 10KOhm
C3948 0.1UF/16V @
GND

U3905B
GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10 GND11 GND12 GND13 GND14
TAS5825MRHBR

0926 Change for additional 13 VIA

I2C Address Table

	ADR_AMP(SPK)	Address 8bit
Main(N.C.)	Open	0x9A
Second	Short	0x98

(36) I2S_Codec_SDIN — I2S_Codec_SDIN
(36) I2S_LRCLK — I2S_LRCLK
(36) I2S_BCLK — I2S_BCLK
(36) I2S_Codec_SDOUT — I2S_Codec_SDOUT

SMB3_CLK_AMP (28)
SMB3_DAT_AMP (28)

TBD

Modify @20181017A

SPK Output

L3901 30Ohm/100Mhz — H_SPKL- — H_SPKL-_CON
D3903 AZ5325-01F @
C3915 1000PF/50V

L3902 30Ohm/100Mhz — H_SPKR- — H_SPKR-_CON
D3904 AZ5325-01F @
C3919 1000PF/50V

L3903 30Ohm/100Mhz — H_SPKL+ — H_SPKL+_CON
D3905 AZ5325-01F @
C3917 1000PF/50V

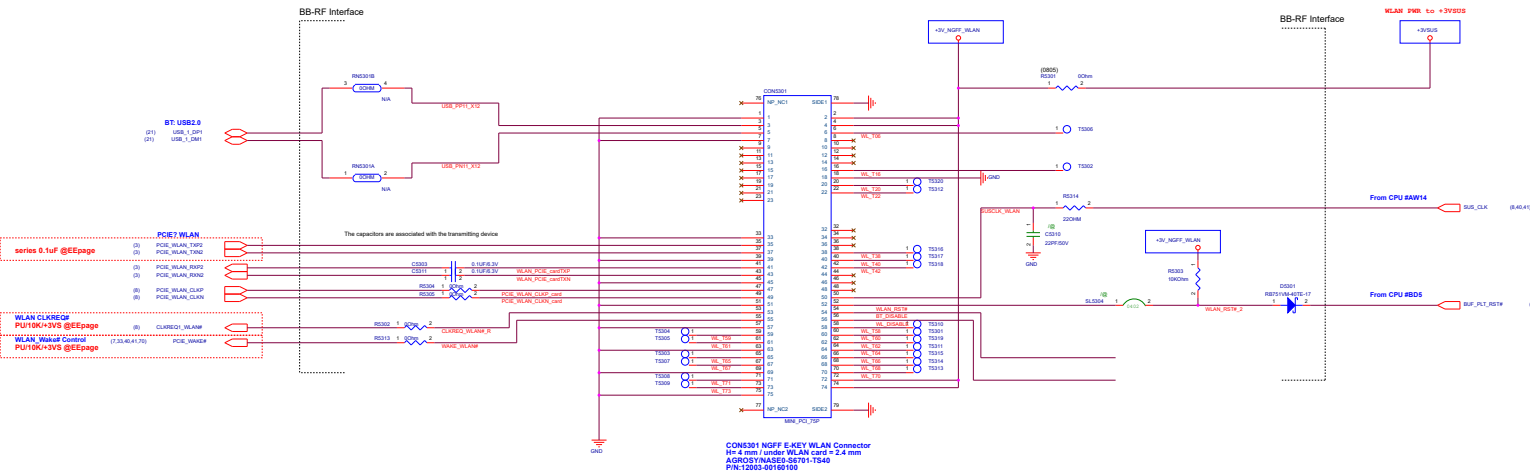
L3904 30Ohm/100Mhz — H_SPKR+ — H_SPKR+_CON
D3906 AZ5325-01F @
C3921 1000PF/50V

Project Name	GX531GX	Rev 1.0
Title :	AUD_INT SPK	
Size B	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Date: Monday, April 29, 2019	Sheet 39 of 104	

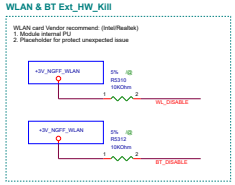
TYPE-C USB3.1

AMD-1.0

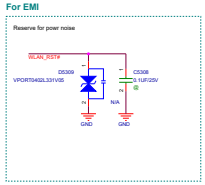
NGFF M.2 TYPE_E-KEY WIFI



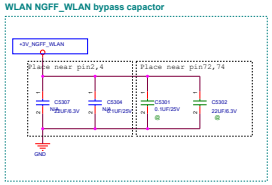
WLAN & BT Ext_HW_Kill



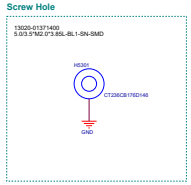
For EMI



WLAN NGFF_WLAN bypass capactor



Screw Hole



Variant Name			
ASUSTeK COMPUTER	Engineer: EE	Title: NGFF Type_WLAN&BT	
Size: Custom	Project Name: GU502DU		Rev: R1.0
Date: Monday, April 29, 2019	Sheet 53 of 104		

<Variant Name>

ASUSTeK COMPUTER	Title : XDD_HDD & ODD CON	
	Engineer: EE	
Size: A	Project Name: GX502GX	Rev: 1.0
Date: Monday, April 29, 2019	Sheet 42 of 104	

Title : I/O_Main board Conn.

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
A	GX502GX	1.0

20180716a
Ian: change PD controller to ITE8851
20180702
Ian: modify component location

C4609 C4607 change to 1uf, 11202-0027F000 to 11G231210525320 @20190222A

C4609 C4607 Change to 0.1uf, 11G231210525320 to 11202-0027F000 @20190422A

Add @20190422A

Imax =650mA

+5V_VCONN

20180724
add for reserved
20180807
unmount

20180724
delete net because no slave charger
20180725
modify VBUS_DISCHARGE net to GP2
20180801
delete and wired to test point

20180726
add type-c 5V VBUS
power switch enable pin

20180725
modify for VBUS sensing circuit

Add @20181109A

20180719
8851 need to change to D version, waiting for P/N, part, symbol
20180723
change to D version: 06050-00380200
20180813
update symbol

20180815
change to shortland
and reserve place
for bead

20180725
add test point for DBGR

20180726
add test point for DBGR

Add @20181109A

Change 0402 to 0201 @20181227G

Add for PD FW @20181227F

20180719
delete 5V_PD
sensing circuit,
not support fast
role swap

20180808
modify R4626/R4627 resistor

20180807
modify VBUS sensing circuit

20180312 Change by Vicent,
unmount reserved

Different power plan prevent leakage

20180724
remove Q4602 and unconnected Q4601A

MUX (1205A)

Add I2C0_SCL, I2C0_SDA, PD1_I2C_INT_PCH
@20181218B

EC

6.3 I2C0 Slave ID Decode

IT8851 provides one I2C slave interface, I2C0, for communication and four different slave ID decodes for I2C0 slave.

Table 6-1. I2C0 Slave ID Decode

AD1	AD0	Slave ID
0	0	7'h40
0	1	7'h42
1	0	7'h50
1	1	7'h52

Project Name	G711GW	Rev 1.0
Title :	PD_IT8851FN	
Size C	Dept.: ASUSTeK COMPUTER	Engineer: Wendell_Lo
Date: Monday, April 29, 2019	Sheet 46 of 104	

Max:200mA

+3VSUS_MUX

C4756 chagne to 22uf, 11G232210625320 to 11203-0072F000
@20190222A

94733_24

Table 4-7. EN is the channel enable pin

EN	Channel Enable Setting
0	Disabled
1	Enabled (Default)

To Type C Connector
90 ohm

From GPU
90 ohm

06113-00340000

Slave address : 0xA0

20180727
modify net name

20180723
change to unmount

NOTE 8. PIN ASSIGNMENT (FRONT VIEW)

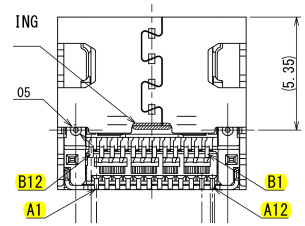
Pin No.	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
	GND	TX1+	TX1-	V_{BUS}	CC1	D+	D-	SBU1	V_{BUS}	RX2-	RX2+	GND
	GND	RX1+	RX1-	V_{BUS}	SBU2	D-	D+	CC2	V_{BUS}	TX2-	TX2+	GND
Pin No.	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

NOTE 9. LASER WELD POINTS MAY BE DISCOLORED.

20180726
delete L4705/4706/4707

20180803
change VBUS capacitor

Add C4729 C4730
@20190215B



Add C4731
@20190215B

U4702 Change to 06016-01290000 @20181124A

U4702 change to 06016-01300200
@20190215B

Add L4706
@20190215D

TYPE-C Connector

Change 12013-00117100 to
12013-00175600 @20181116A

Change @20181109A

Add RC @20181221B

USB2.0 EMI-Protection With ECMF(PCB 1.05mm_10Layer)

From PCH USB2.0 Port

Note :
1. This part & symbol only apply for standard PCB stack-up listed in datasheet appendix I
Please check your project must matching the thickness , DF and DK value of PCB every layer
2. C3809&C3810 must replaced with 18pF 0201 capacitors and the tolerance of capacitance value is 5%
3. Pin7 & Pin8 & Pin11 & Pin12 must be connected to system ground
4. Pin13 to Pin16 are floated in regular scheme
temp_M08_000010層名順序是：TOP/GND/IN1/GND1/IN2/VCC/GND2/IN3/GND3/BOTTOM

USB EMI-Protection

CC pin
OVP Protection

20180727
delete CC pin OVP because do not support PD 20V

USB3.0
ESD-Protection

USB2.0
ESD-Protection

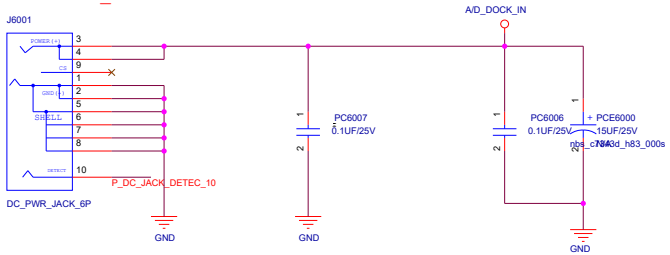
PD Discharging

20180801
no PD function, delete discharging circuit

Project Name	G711GW		Rev. 3.0
Title :	TYPE-C USB3.1_R1.5_4		
Size: D	Dept.: ASUSTeK COMPUTER INC.	Engineer: Ashton_yang	
Date: Monday, April 29, 2019		Sheet 43 of 104	

DC-IN Connector

New 6 Phi 4 Pin DC_Jack 1.55ch

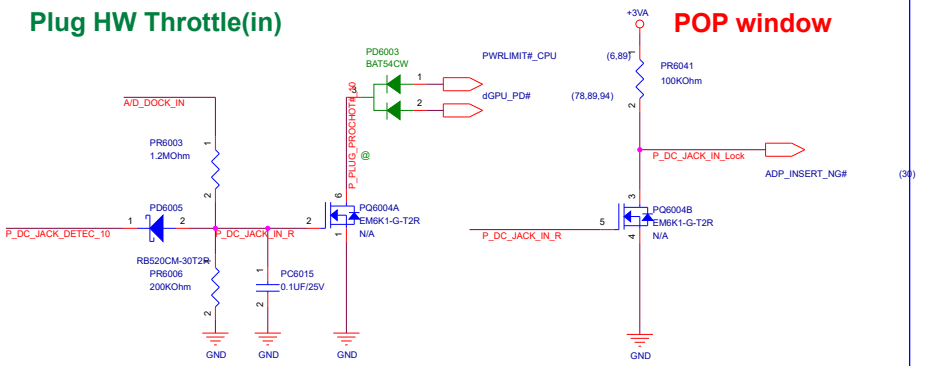


12033-00020300

	3.4CH	1.55CH
J6001	12033-00020200	12033-00020300

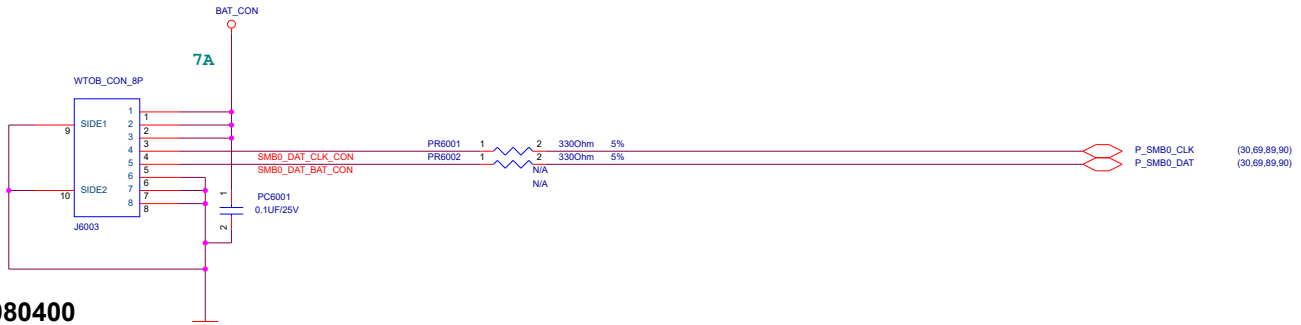
Mode	ADP_INSERT_NG#	AC_IN_OC#
AC Mode	0 (POP,throttling, stop charging)	0
	1	

Plug HW Throttle(in)



POP window

Battery Connector



12017-00080400

Note:Battery Connector 正確性與BAT1_IN_OC#是否預留!

ASUS	Project Name: GX700		Rev: R1.0
Title : DC & BAT IN			
Size: A3	Dept.: NB_Power team	Engineer: Benson	
Date: Monday, April 29, 2019	Sheet 60 of 104		

Title : I/O board Audio/USB

ASUSTeK COMPUTER

Engineer: Wendell_Lo

Size	Project Name	Rev
C	GL752VW	1.0

EMI1 SPRING (4.7H) 13060-00570000*1

EMI2 SPRING (2.6H) *3
13NB0I50M01011

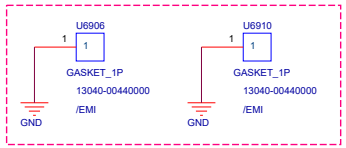
EMI2 SPRING (4H) *3
13NK00B1M01011

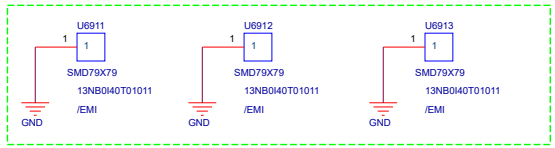
U6906 U6910 change to 13040-00440000(SMT Gasket H=2.5mm)
@20190213A

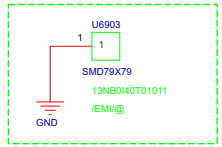
Modify @20181122A(EMI req.)

Modify @20181122A(EMI req.)

Unmount @20181029D

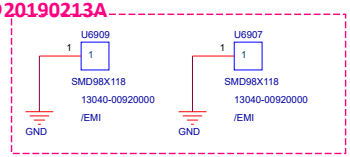




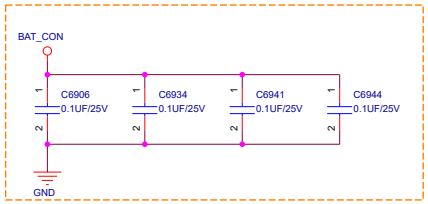


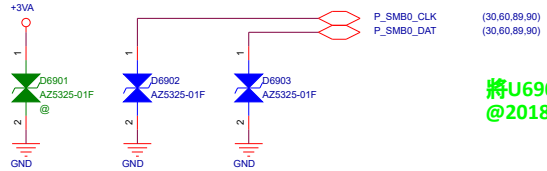
teknisi-indonesia

U6907 U6909 change to 13040-00920000(SMT Gasket H=3mm)
@20190213A



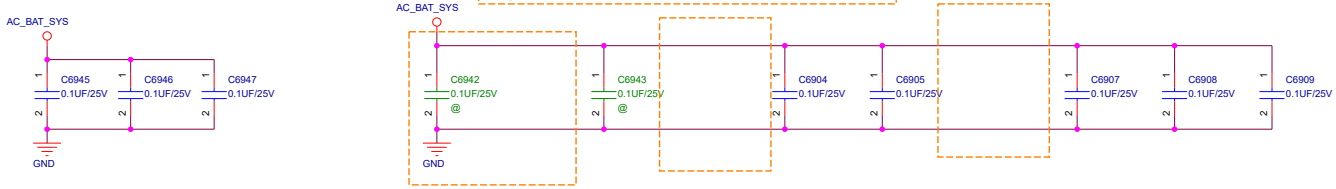
EMI request @20181026A



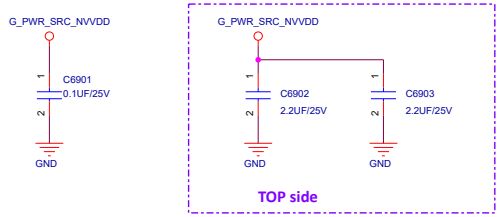


將U6904, U6908(改裸銅), U6905(改裸銅) 移除
@20181122C

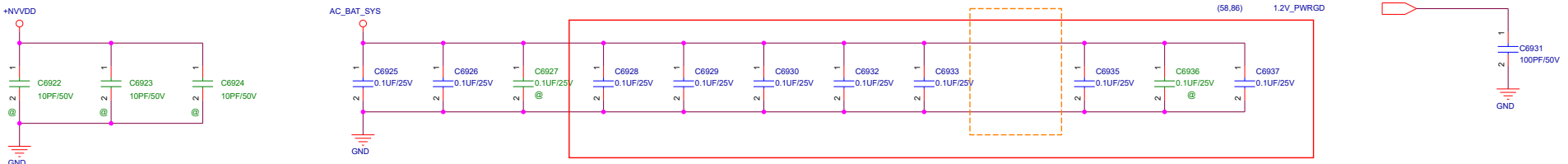
2017/04/05 EMI

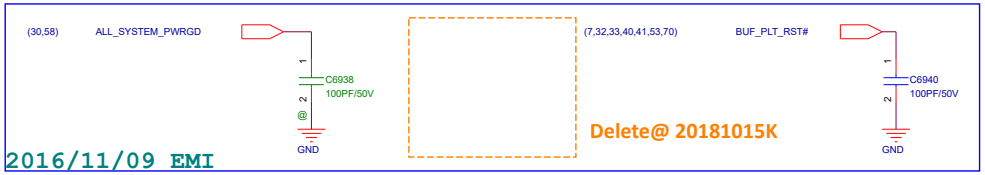


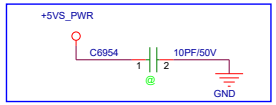
4/2 for EMI



2016/07/27 EMI







<Core Design> 2017.05.02 EMI Reserve

ASUSTeK COMPUTER	Title : OTH_EMI	
	Engineer: EE	
Size: B	Project Name: GX502GX	Rev: 1.0
Date: Monday, April 29, 2019	Sheet 69 of 104	

<Core Design>

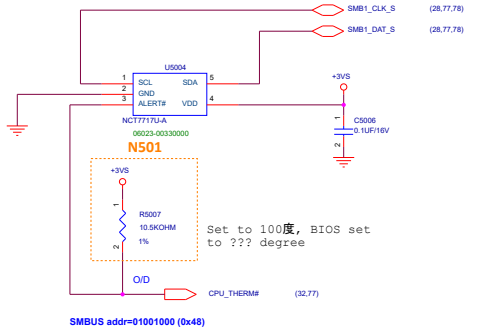
	Project Name **GX502GX**	Rev 1.0

Title : ANT

Size C	**Dept.:** ASUSTeK COMPUTER	**Engineer:** EE

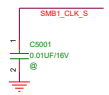
Date: Monday, April 29, 2019	Sheet	49	of	104

CPU Thermal Sensor



Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

Reserve for powr noise



06G023123010為RD不建議用料: 此為舊版，建議改用新板(cost低)06023-00330000/NCT7717U-A。

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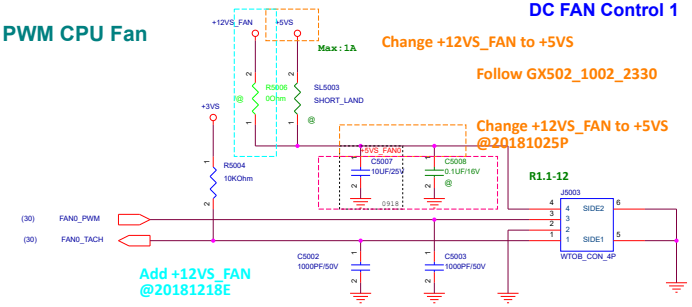
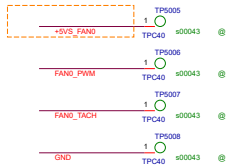
PWM CPU Fan

DC FAN Control 1

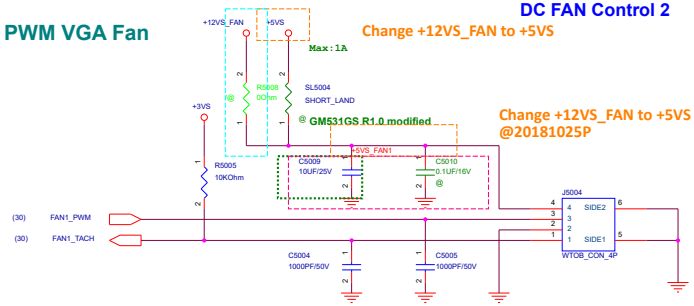


Change +12VS_FAN to +5VS
@20181025P



PWM VGA Fan

DC FAN Control 2



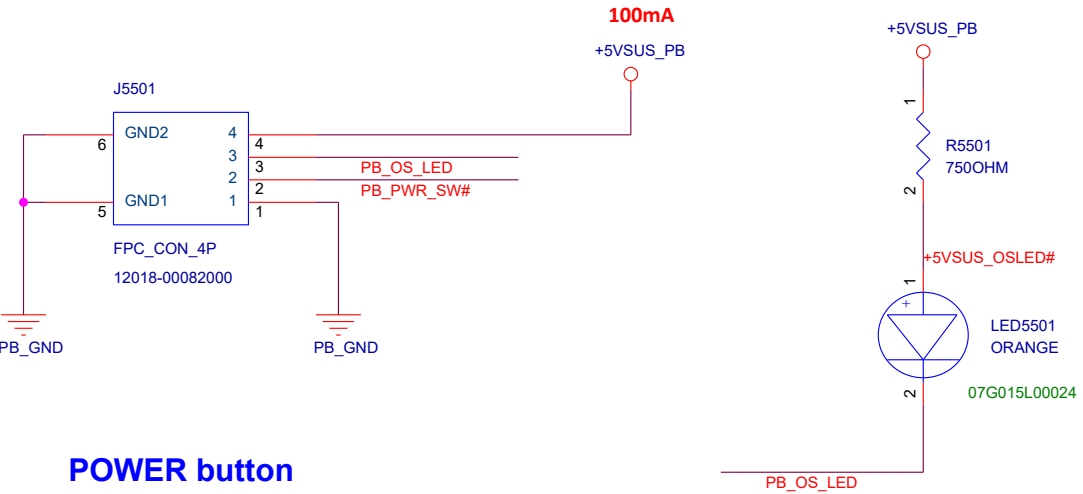
C017 change to C5007
C018 change to C5008
C021 change to C5009
C023 change to C5010
@20190128A

Main Board

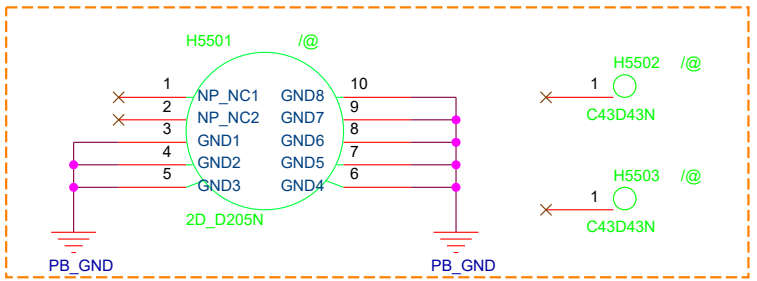
Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, April 29, 2019	Sheet 54 of 104	

Connected to MB Page56

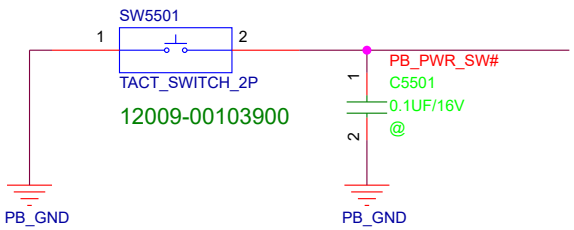
OS LED (PWRBTN)

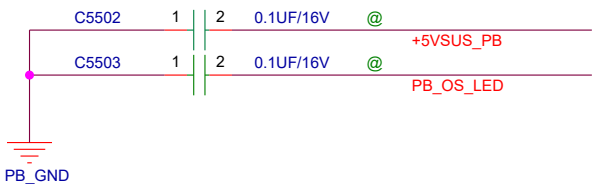


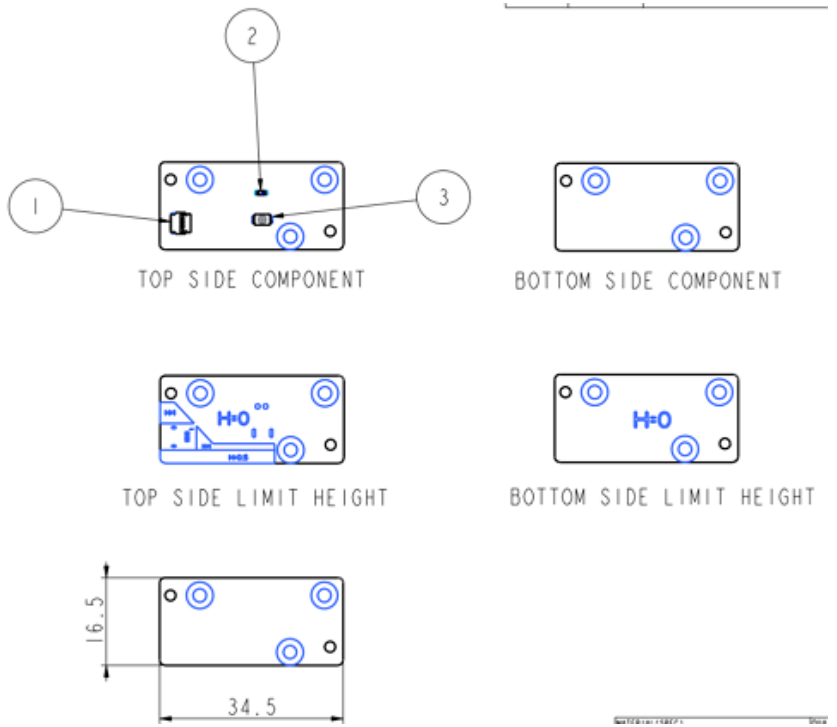
Change @20181026B



POWER button



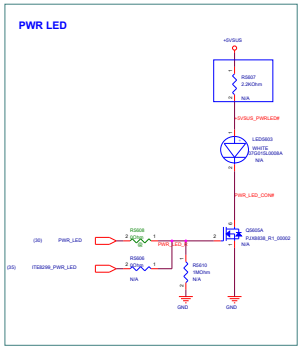




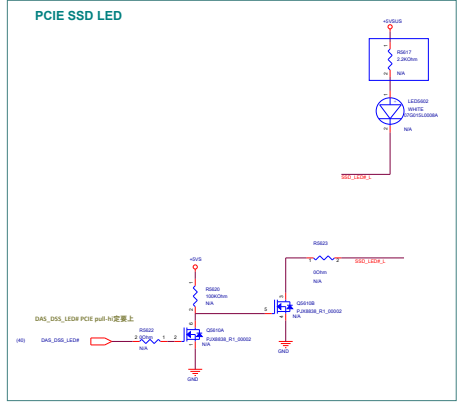
<Core Design>

ASUSTeK COMPUTER	Title : IO Con. to MB	
	Engineer: EE	
Size: A	Project Name: GX502GX	Rev: 1.0
Date: Monday, April 29, 2019	Sheet 55 of 104	

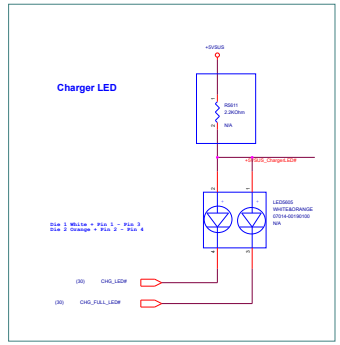
PWR LED



PCIE SSD LED



Charger LED

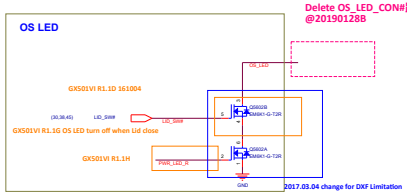


@20181013C

PWR LED PCIE SSD LED Charger LED

OS LED

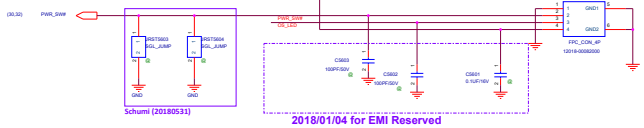
Delete OS_LED_CON#跨頁
@20190128B



2017.03.04 change for DXF Limitation

JRST5604 on TOP of PCB
JRST5603 on BOT of PCB

50mA Connected to Power Key Board 55



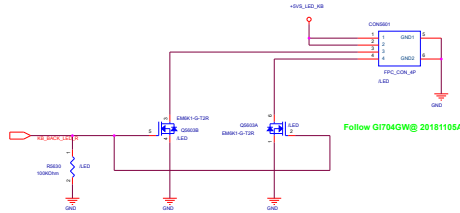
Schumi (20180531)

2018/01/04 for EMI Reserved

Keyboard Backlight CON.

Modfify @20181017K

Change Keyboard Backlight Con. to 4pin
@20181011C



Follow GI704GW@ 20181105A

Change to monut @ 20181129A

KB RGB LED

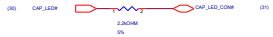
D item- RGB LED

Remove@20181009N

Keyboard LED Connector Follow GI704GW@ 20181105A Remove 4 ZONE RGB@20181213A

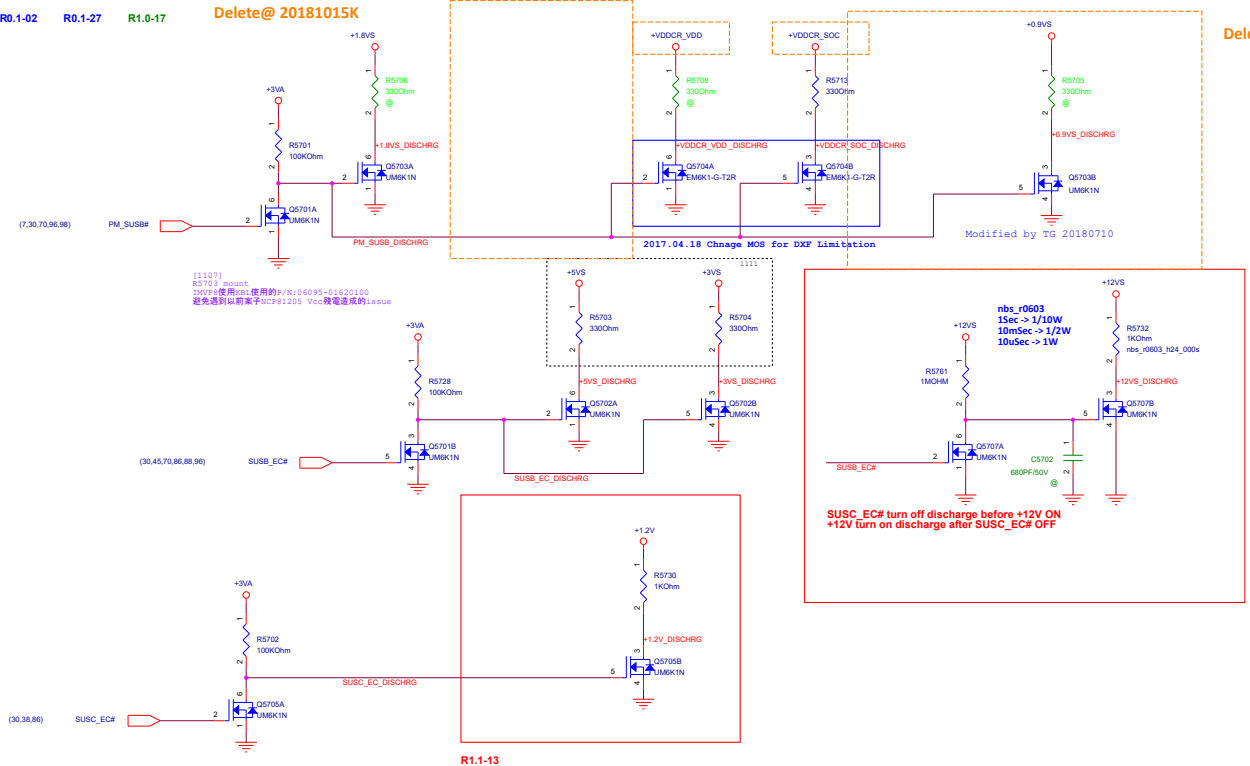
CAPS LOCK LED
@20181015C

CAP LED

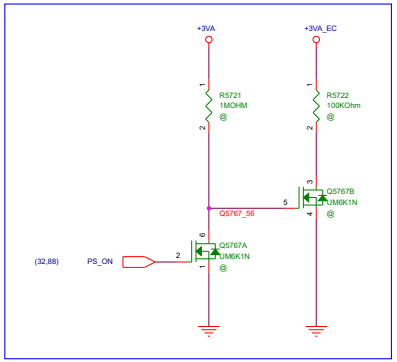


R0.1-02 R0.1-27 R1.0-17

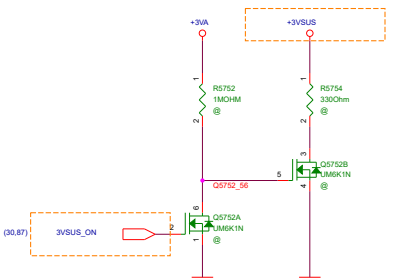
Delete@ 20181015K



Delete@ 20181015K



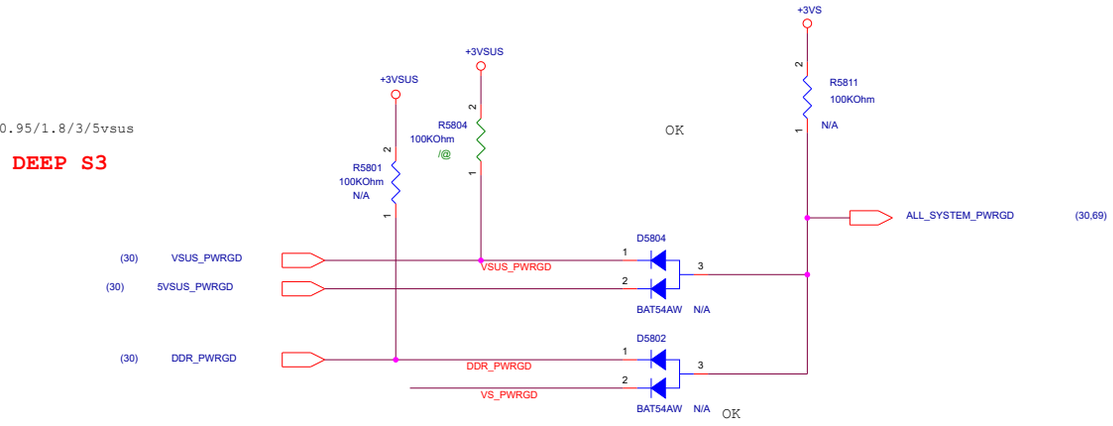
Change DSW to SUS
@20181009

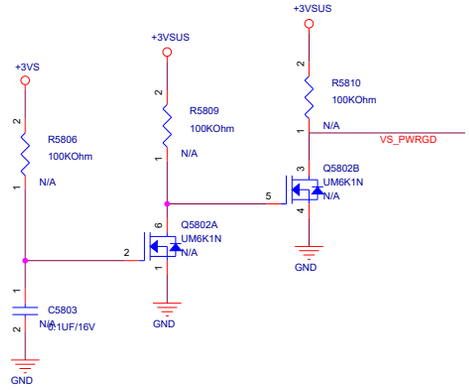


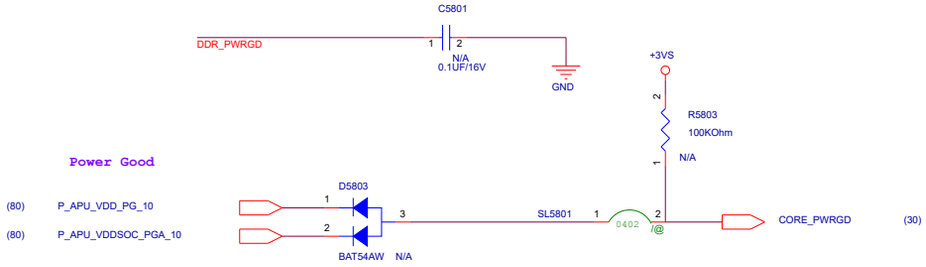
<Core Design>

ASUSTeK COMPUTER	Title : DSG_Discharge	
	Engineer: EE	
Size: Custom	Project Name: GX502GX	Rev: 1.0
Date: Monday, April 29, 2019	Sheet 57 of 104	

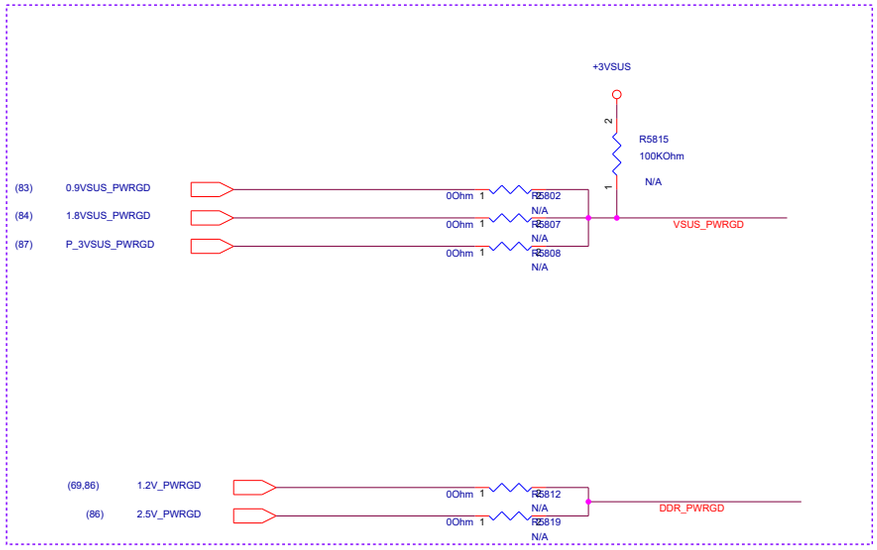
POWER GOOD DETECTER





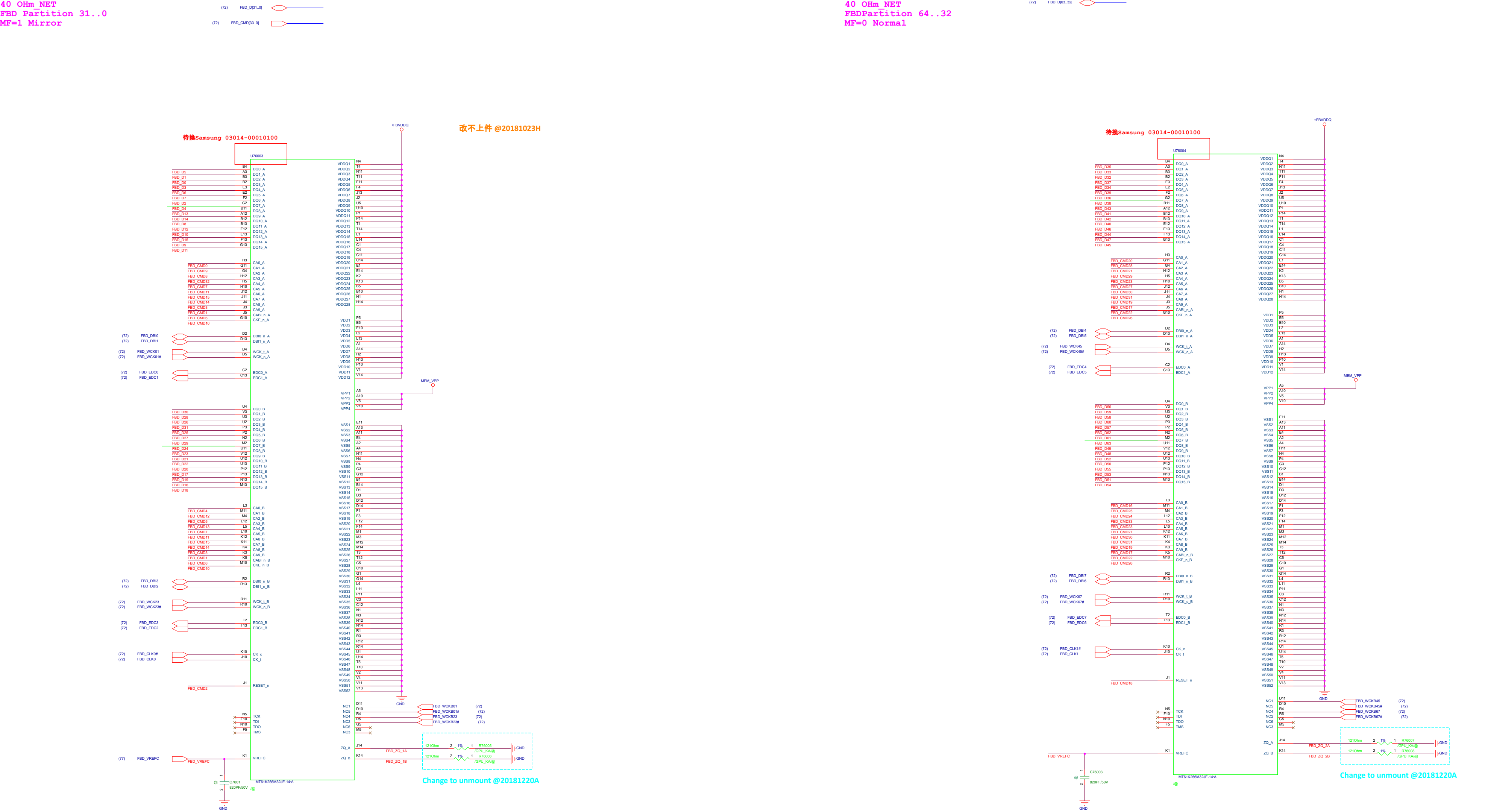


Power Good



Remove AMD GPU PWRGD
@20181009K

ASUS	Project Name: FX505DY	Rev: R1.0
Title : POWER GOOD DETECTER		
Size: Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: RD2 EE3	
Date: Monday, April 29, 2019	Sheet 58 of 104	



<Core Design>

Title
<Title>

Size	Document Number	Rev
A1	GX502GX	R1.0

Date: Monday, April 29, 2019 Sheet 76 of 104

<Core Design>

ASUSTeK COMPUTER

Title : BT_Bluetooth

Engineer: EE

Size	Project Name	Rev
C	GX502GX	1.0

Date:	Monday, April 29, 2019	Sheet	61	of	104

Title : NGFF SSD(MAXIM)

ASUSTeK COMPUTER

Engineer: Wendell_Lo

Size	Project Name	Rev
D	GL752VW	1.0

Date: Monday, April 29, 2019 Sheet 63 of 104

<Core Design>

ASUSTeK COMPUTER

Title : ME_Screw Hole & Nut

Engineer: EE

Size	Project Name	Rev
A	teknisi-indonesia GX502GX	1.0

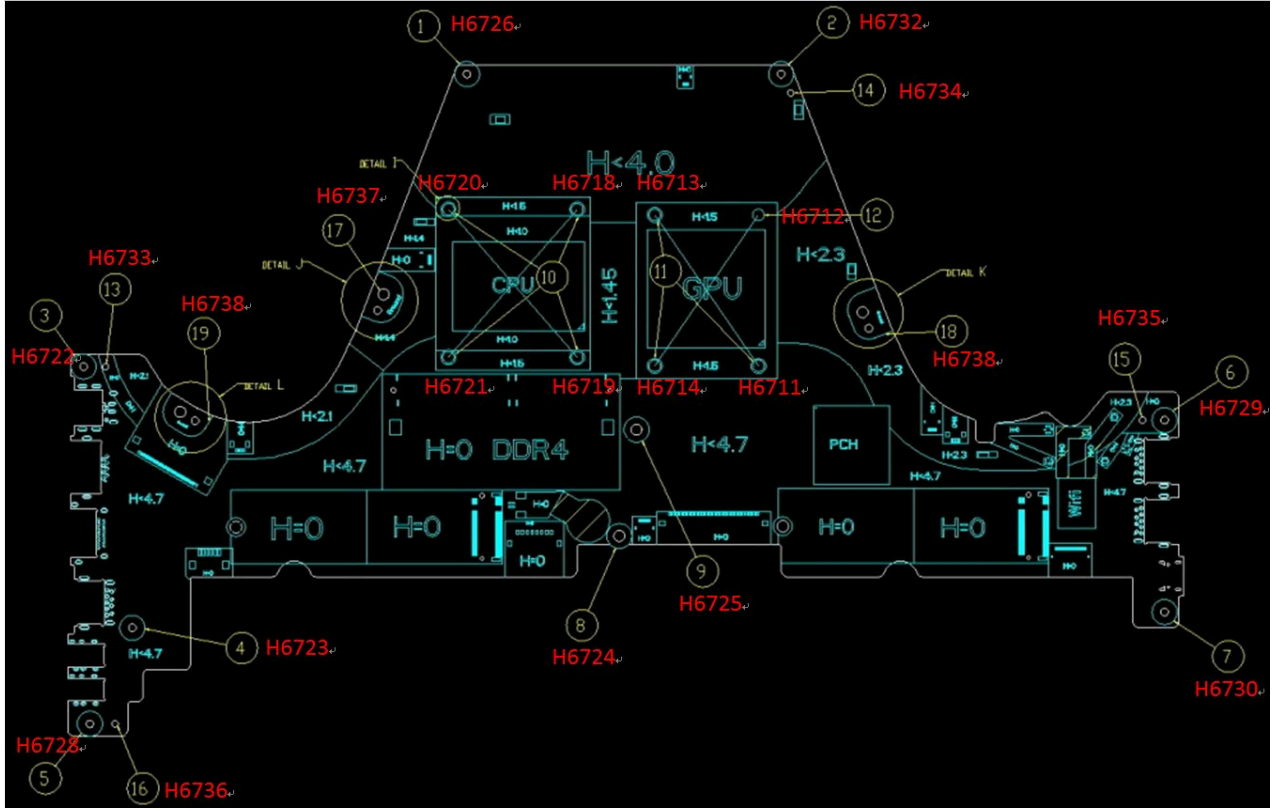
Date: Monday, April 29, 2019 Sheet 65 of 104

Title :

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
A	**GX502GX**	1.0



GPU

TOP 3.7/6.5, BOT 3.7/4.7

H6711 1 @ CT256CB185D146

H6712 1 @ C146D146N

H6713 1 @ CT256CB185D146

H6714 1 @ CT256CB185D146

CPU

TOP 3.7/6.5, BOT 3.7/4.7

H6718 1 @ CT256CB185D146

H6719 1 @ CT256CB185D146

H6720 1 @ CT256CB185D146

H6721 1 @ CT256CB185D146

TOP&BOT 2.4/8

GND 1 H6726 C315D94 @

GND 1 H6732 C315D94 @

GND 1 H6722 C315D94 @

GND 1 H6723 C315D94 @

GND 1 H6729 C315D94 @

GND 1 H6730 C315D94 @

GND 1 H6715 C315D94 @

GND 1 H6716 C315D94 @

Add @20181029C

TOP&BOT 3.5/8

GND 1 H6724 C315D138 @

GND 1 H6725 C315D138 @

Change @20181023F

H6728

GND GND 1 2 3 NP_NC GND1 GND2 GND4 GND3 5 4 GND GND

C315D94N /@

H6735 1 C79D79N /@

Change @20181023F

NC @20181030B

H6734

GND GND 1 2 3 NP_NC GND1 GND2 GND4 GND3 5 4 GND GND

CT236D79N s12526 @

H6736

GND GND 1 2 3 NP_NC GND1 GND2 GND4 GND3 5 4 GND GND

CT236D79N s12526 @

Change @20181025A

GND 1 H6737 /@ GND NP_NC 2

2D_D138_D94N

GND 1 H6739 /@

CRT349X338CRB547X782D138

Change @20181023E

GND /@ 1 H6738 2

s12570 2D_D138_D94

<Core Design>

ASUSTeK COMPUTER

Title : I/O board FUNC key

Engineer: EE

Size	Project Name	Rev
B	GX502GX	1.0

Date: Monday, April 29, 2019 Sheet 67 of 104

<Core Design>

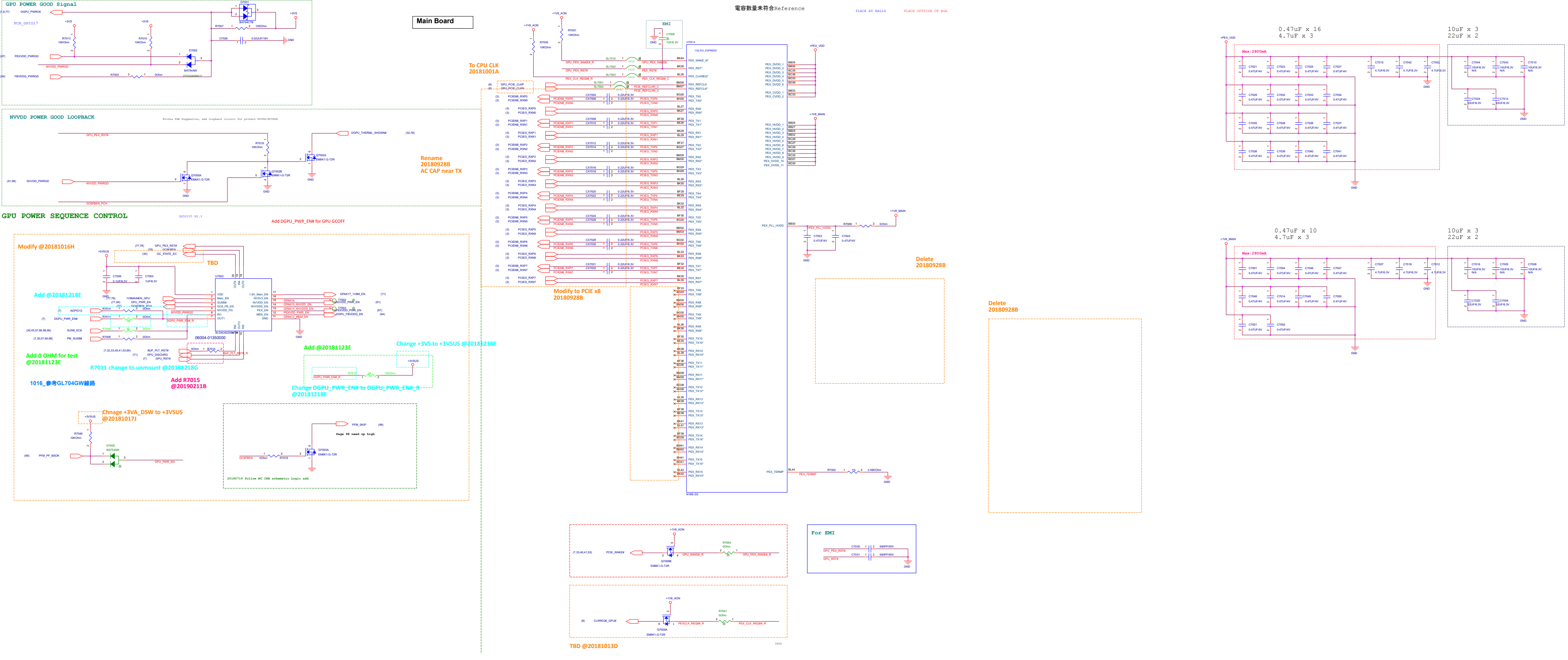
Title : OTH_for test only

ASUSTeK COMPUTER

Engineer: EE

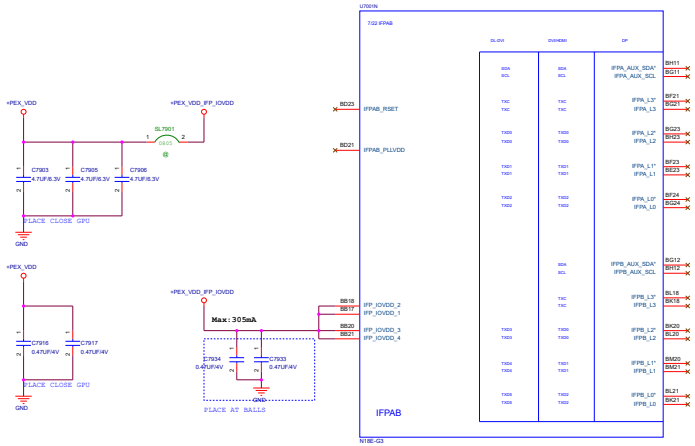
Size	Project Name	Rev
A	GX502GX	1.0

Date:	Monday, April 29, 2019	Sheet	68	of	104

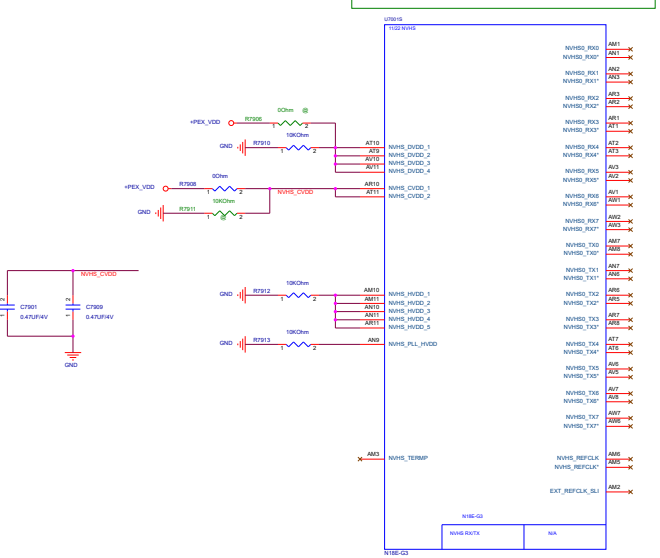


GPU POWER GOOD Signal
NVVDD POWER GOOD LOOPBACK
GPU POWER SEQUENCE CONTROL
Main Board
電容數量未符合Reference
PLACE AT BALLS
PLACE OUTSIDE OF BGA
To CPU CLK
20181001A
Rename
20180928B
AC CAP near TX
Modify to PCIE x8
20180928B
Add DGPU_PWR_EN# for GPU GCOFF
Modify @20181016H
TBD
Add @20181218E
Add 0 OHM for test
@20181123E
R7011 change to unmount @20181218G
1016_參考GL704GW線路
Add R7015
@20190211B
Add @20181123E
Change +3VS to +3VSUS @20181218E
Change DGPU_PWR_EN# to DGPU_PWR_EN#_R
@20181218E
Chnage +3VA_DSW to +3VSUS
@20181017J
Page 98 need up high
20180719 follow WC CRB schematic Logic add
0.47uF x 16
4.7uF x 3
10uF x 3
22uF x 2
0.47uF x 10
4.7uF x 3
10uF x 3
22uF x 2
Max:2800mA
Max:2800mA
Delete
20180928B
Delete
20180928B
For EMI
TBD @20181013D
EMI

Project Name	GX502GX	Rev 2.0
Title :	GPU_PCIE I/F	
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer:
Date: Monday, April 29, 2019	Sheet 70 of 104	



NVLink (not used)



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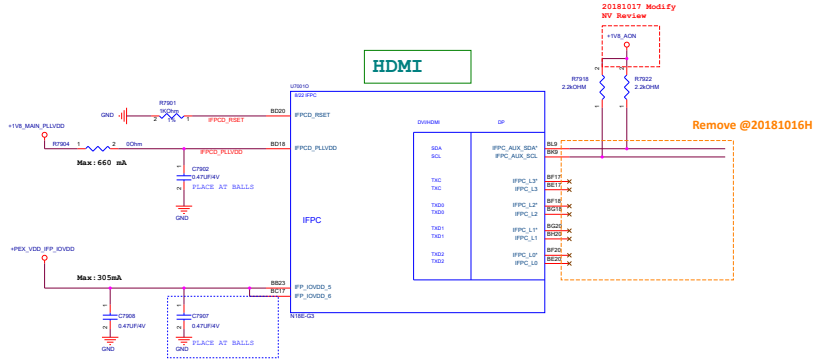
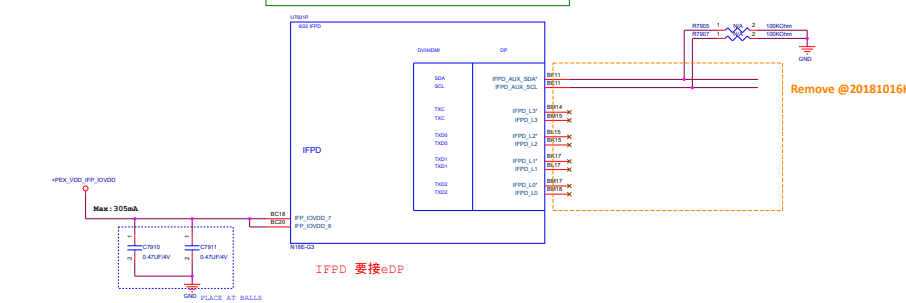
HDMI

20181017 Modify
NV Review

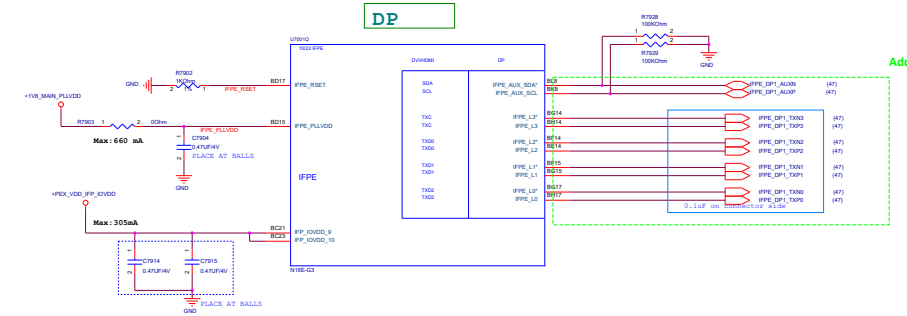


EDP(4Lane Panel)

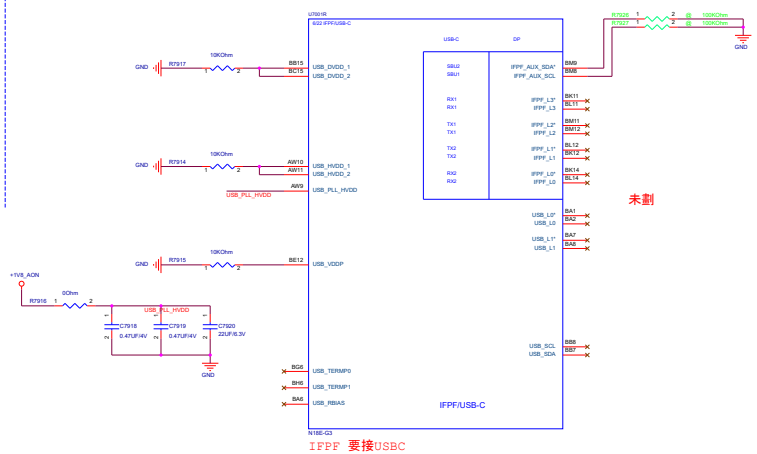


IFPD 要接eDP

DP



USB-C/DP (not used)

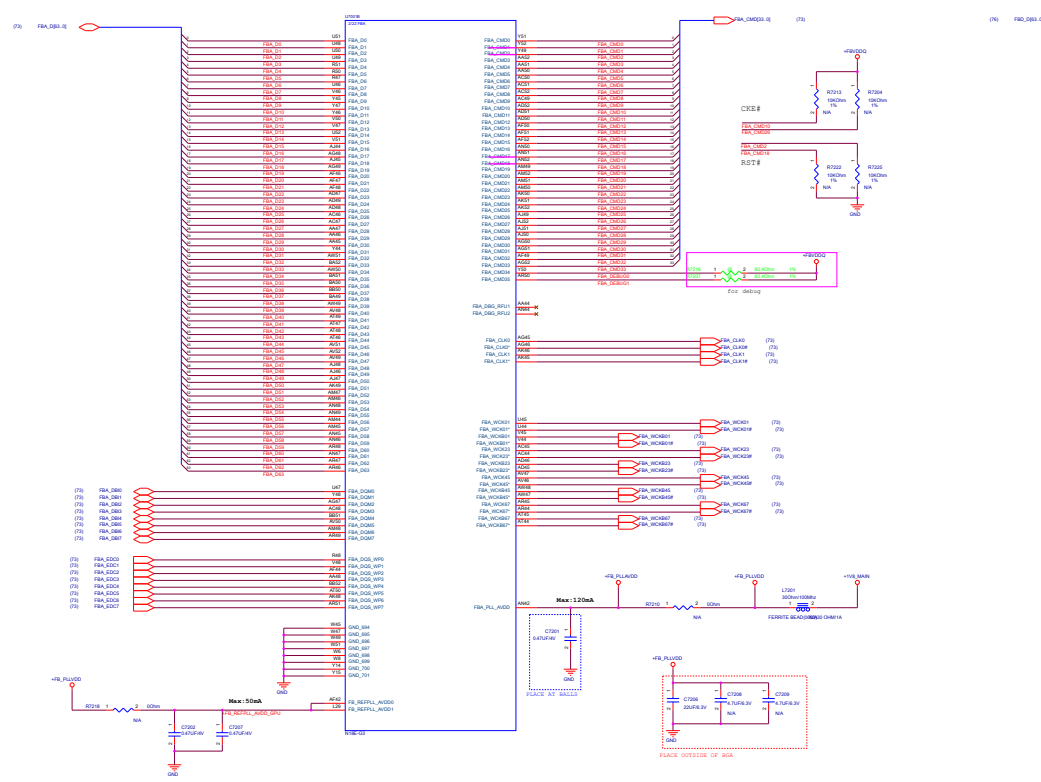


未劃

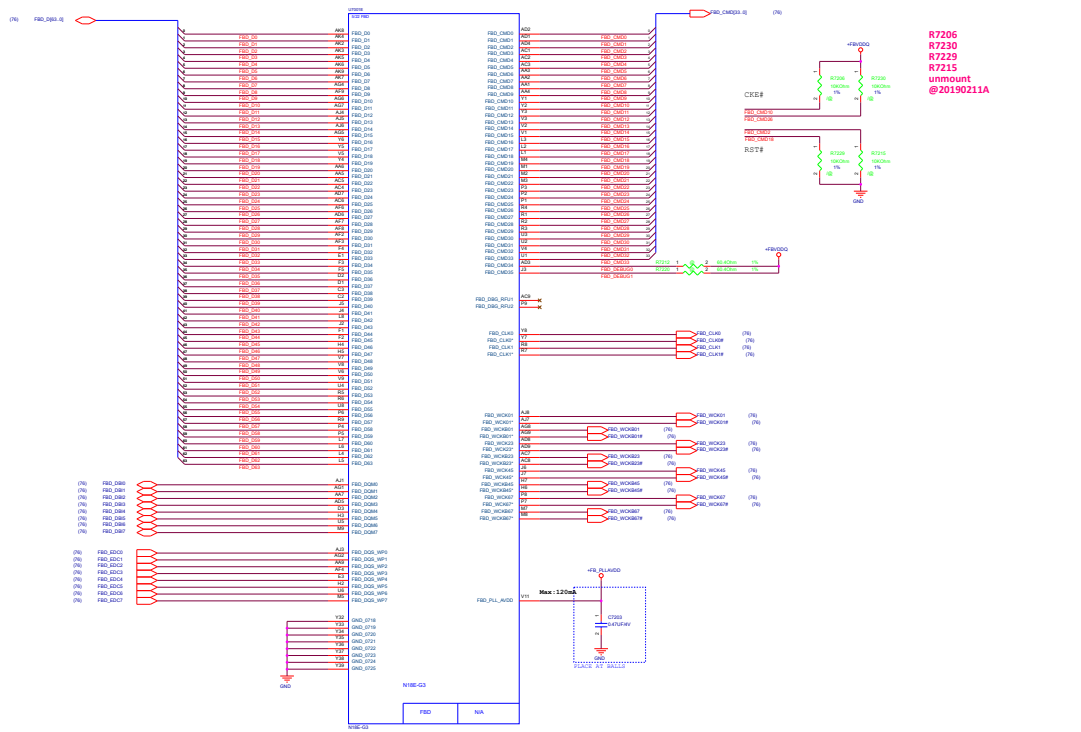
IFPF 要接USBC

ASUS	Project Name: GX502GX		Rev: R1.3
Title : GPU_DP/EDP/HDMI/LVDS/CRT			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1	
Date: Monday, April 29, 2019	Sheet: 79 of 104		

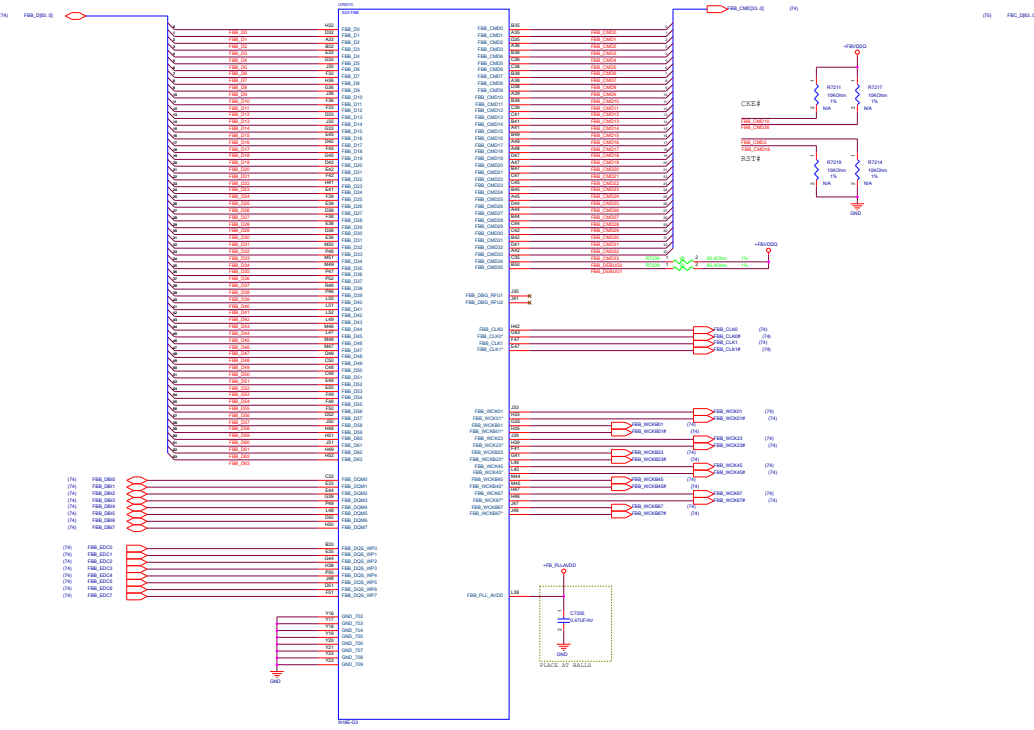
MEMORY: GPU FB Partition A



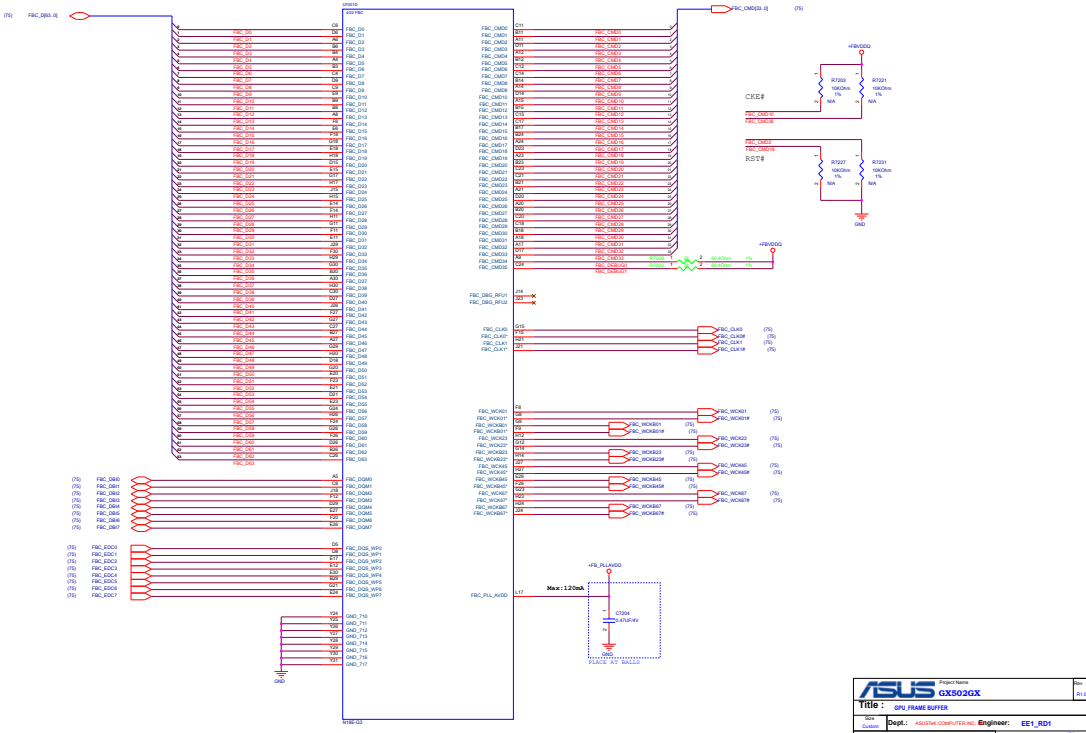
MEMORY: GPU FB Partition D



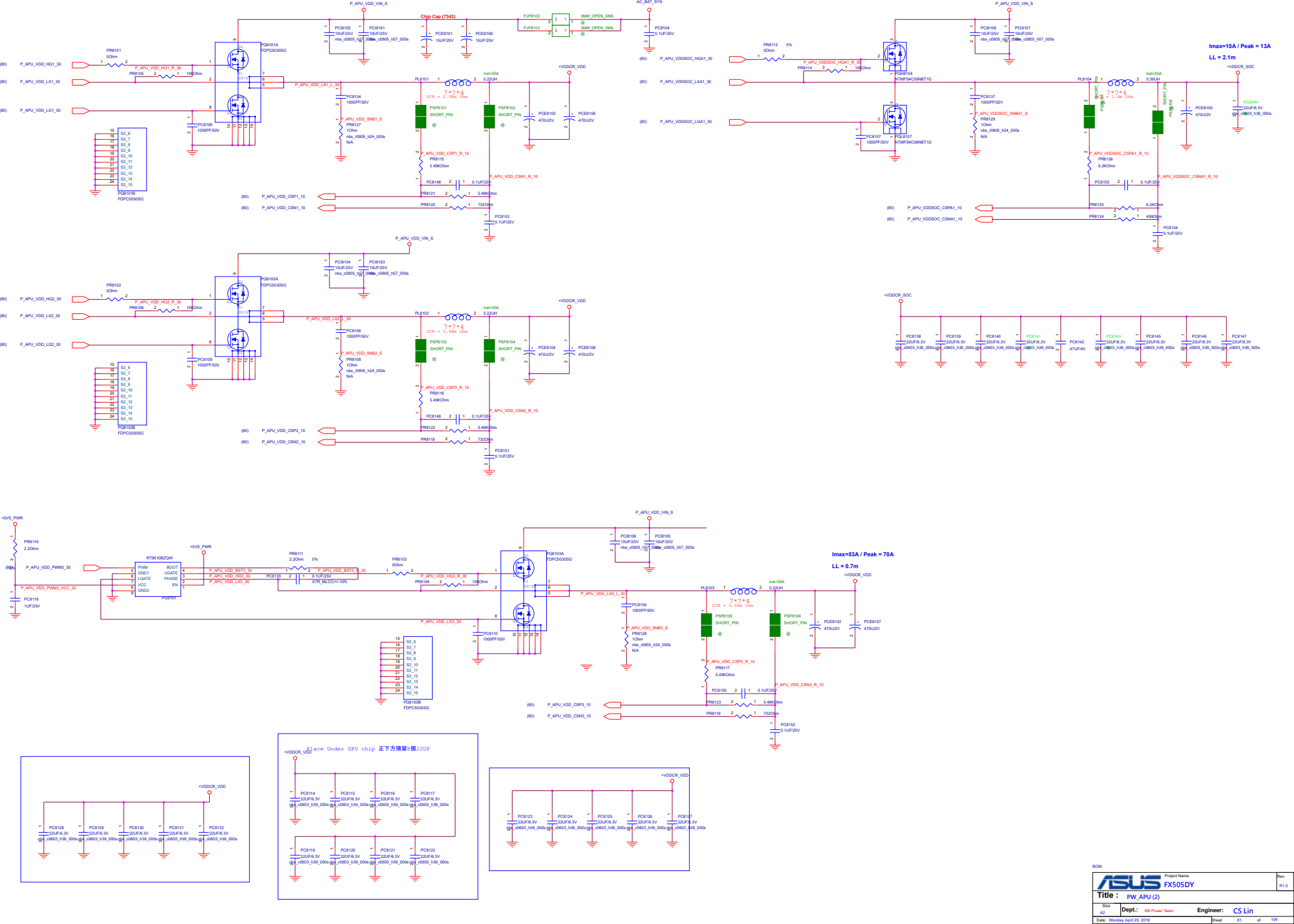
MEMORY: GPU FB Partition B



MEMORY: GPU FB Partition C

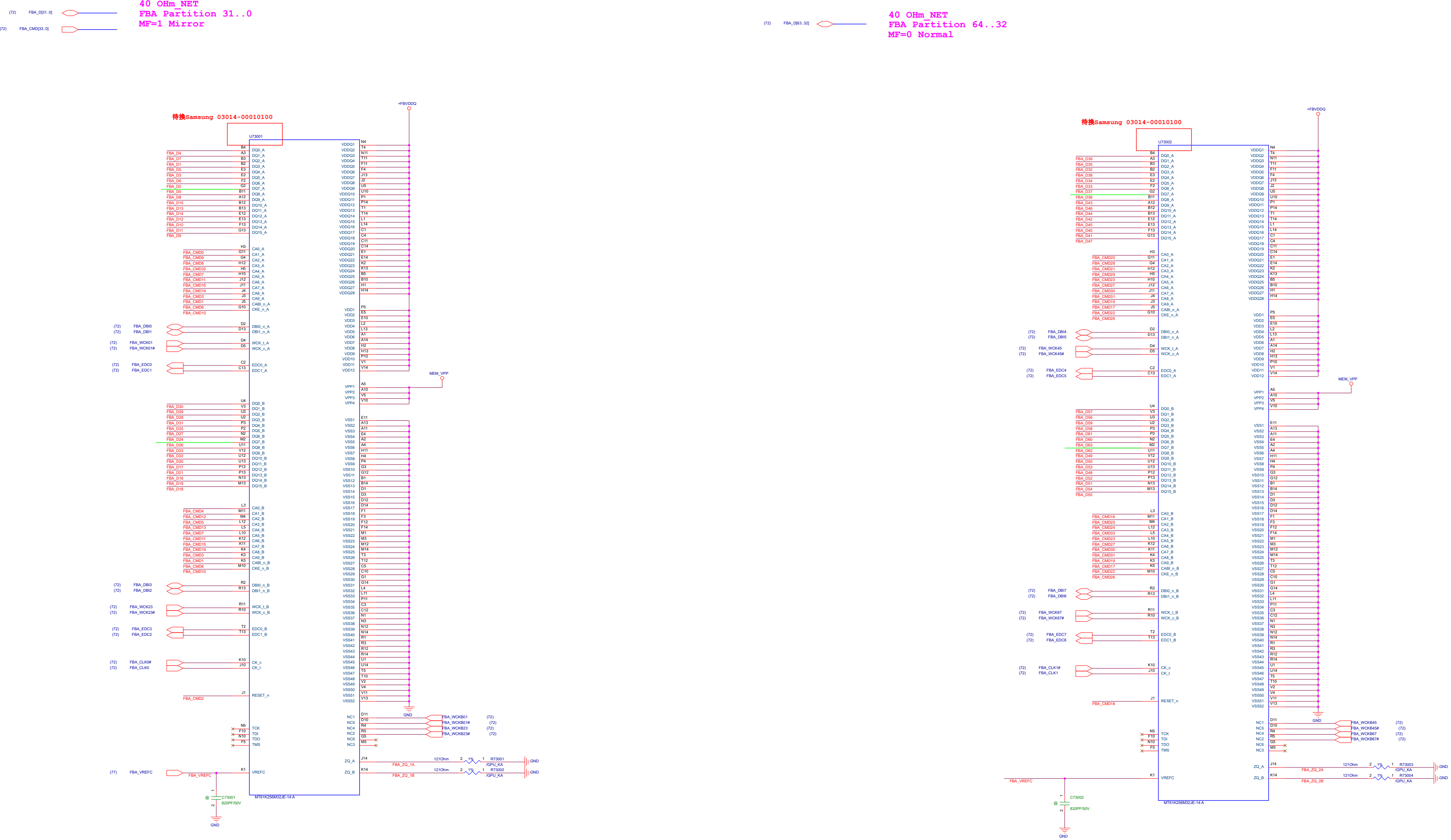


ASUS	Project Name: GX502GX		Rev: 81.0
Title : GPU_FRAME BUFFER			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE1_RD1	
Date: Monday, April 29, 2019	Sheet: 72 of 104		



BOM

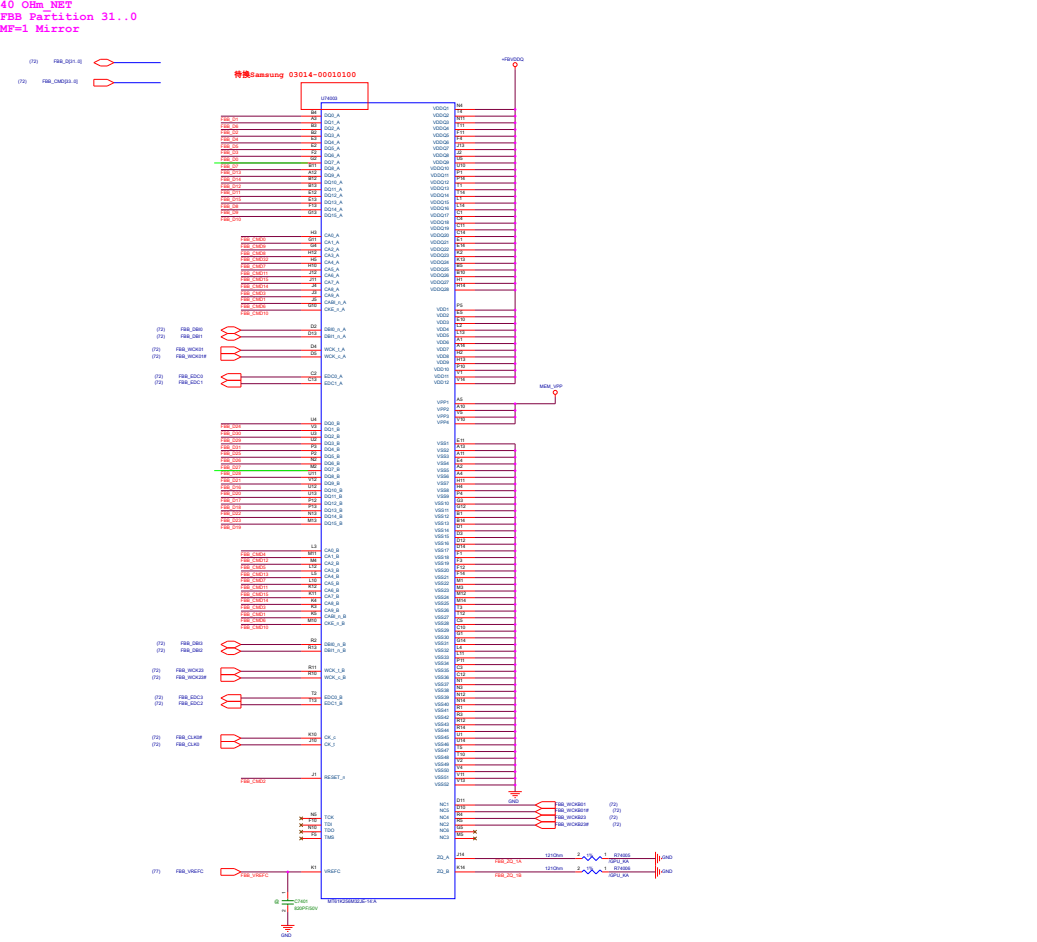
ASUS	Project Name: FX505DY	Rev: R1.0
Title : PW_APU (2)		
Size: A2	Dept.: NB Power Team	Engineer: CS Lin
Date: Monday, April 29, 2019	Sheet: 81 of 104	



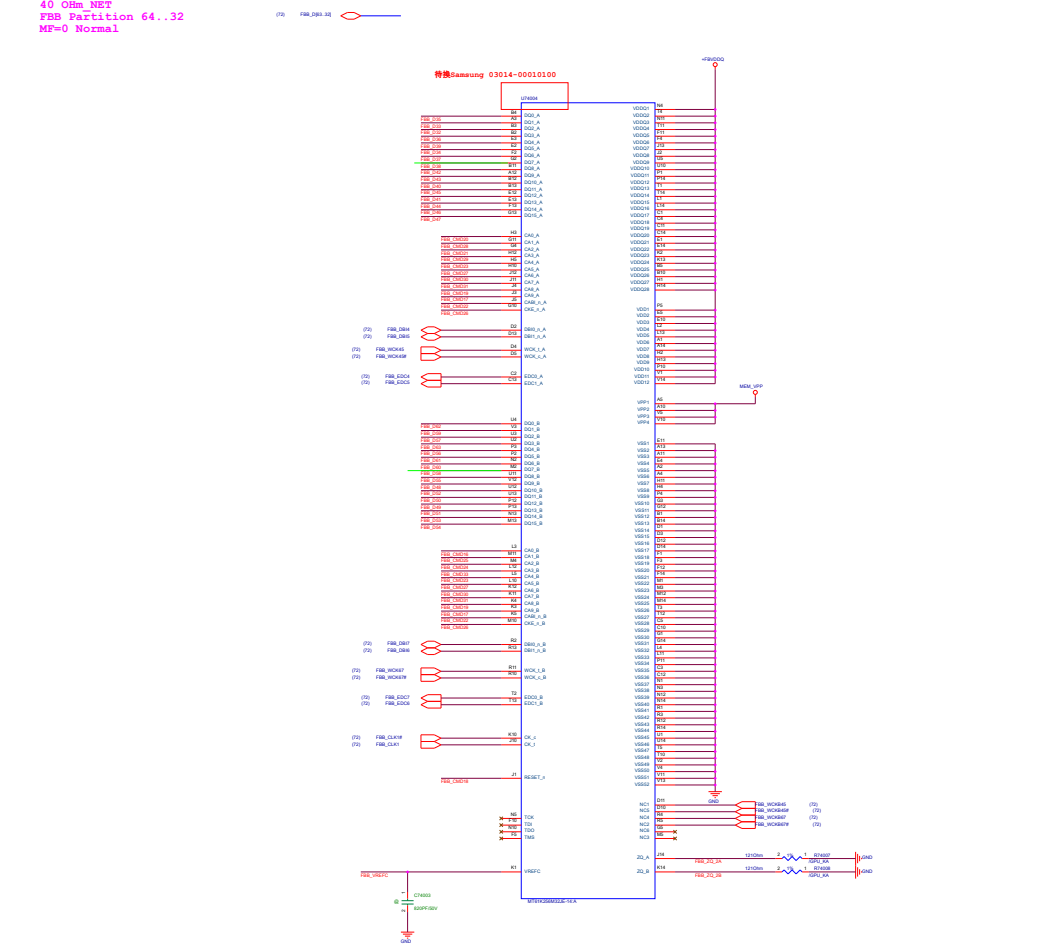
<Core Design>

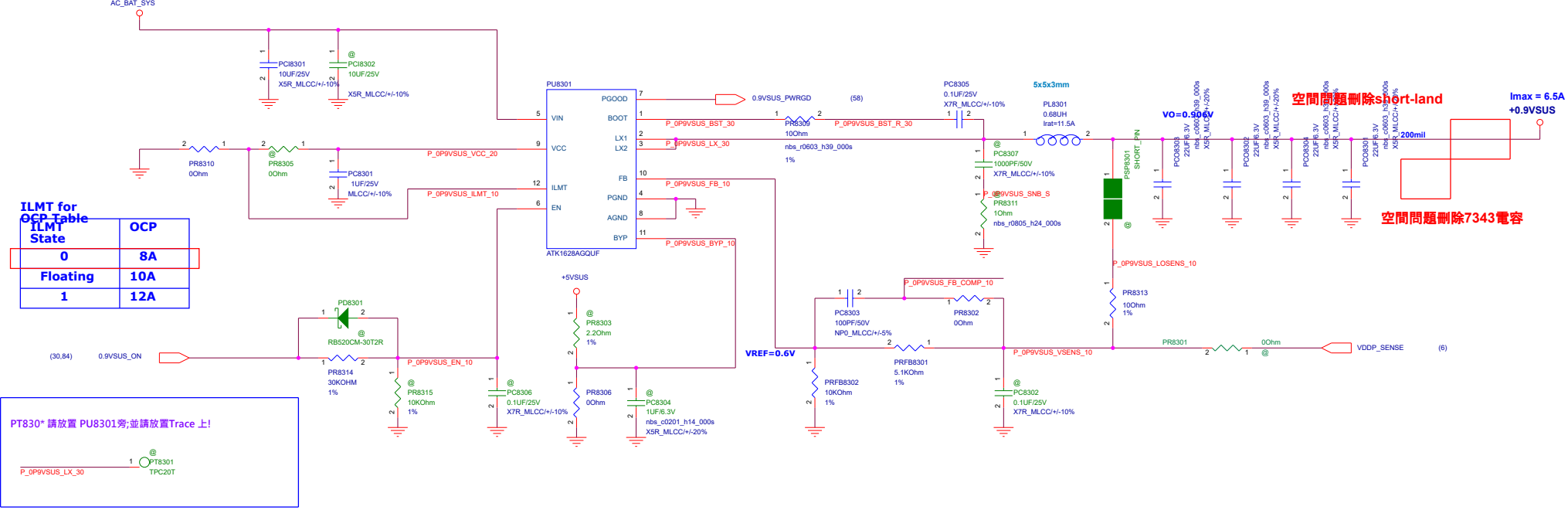
Title	<Title>	
Size A1	Document Number GX502GX	Rev R1.0
Date: Monday, April 29, 2019	Sheet 73 of 104	

40 OHm_NET
FBB Partition 31..0
MF=1 Mirror



40 OHm_NET
FBB Partition 64..32
MF=0 Normal

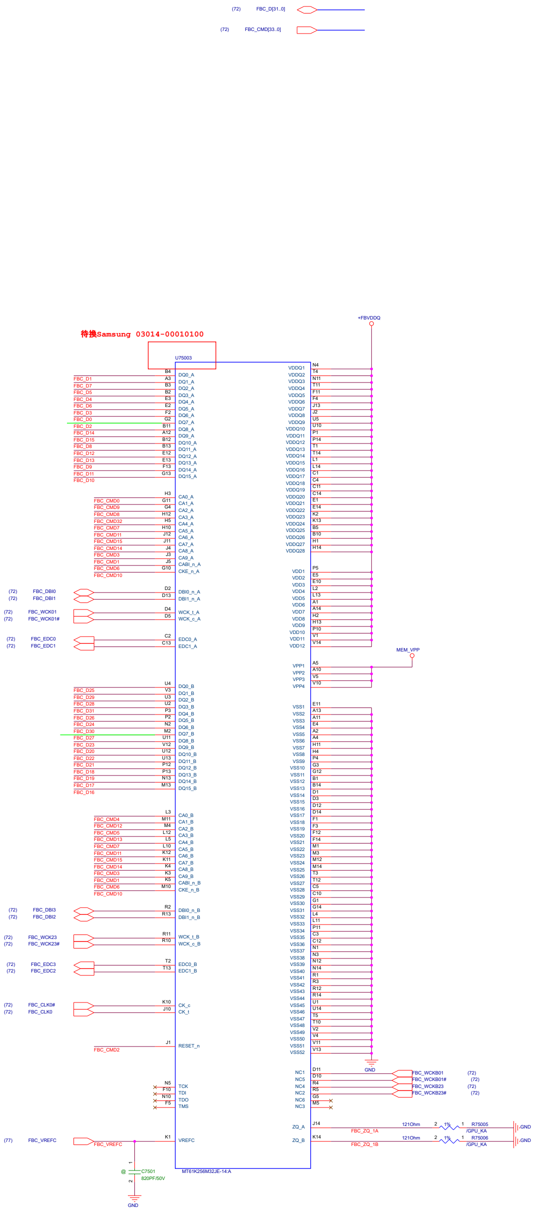




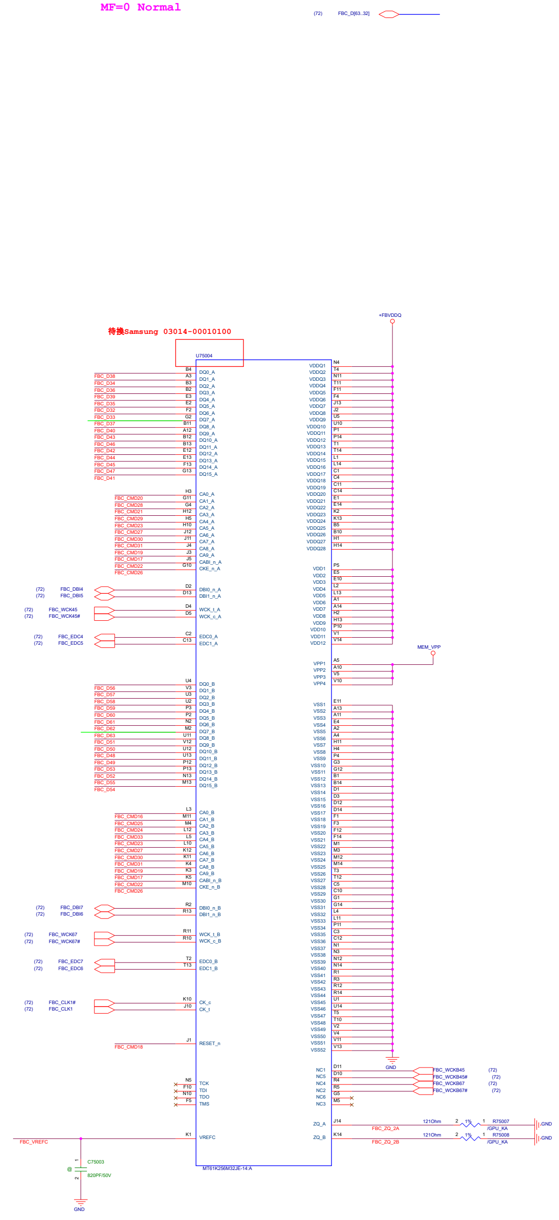
<Variant Name>

ASUS	Project Name: FX505DY	Rev: R1.0
Title : PW_+0.9VSUS		
Size: A3	Dept.: NB Power team	Engineer: CS Lin
Date: Monday, April 29, 2019	Sheet 83 of 104	

40 OHm_NET
FBC Partition 31..0
MF=1 Mirror



40 OHm_NET
FBC Partition 64..32
MF=0 Normal



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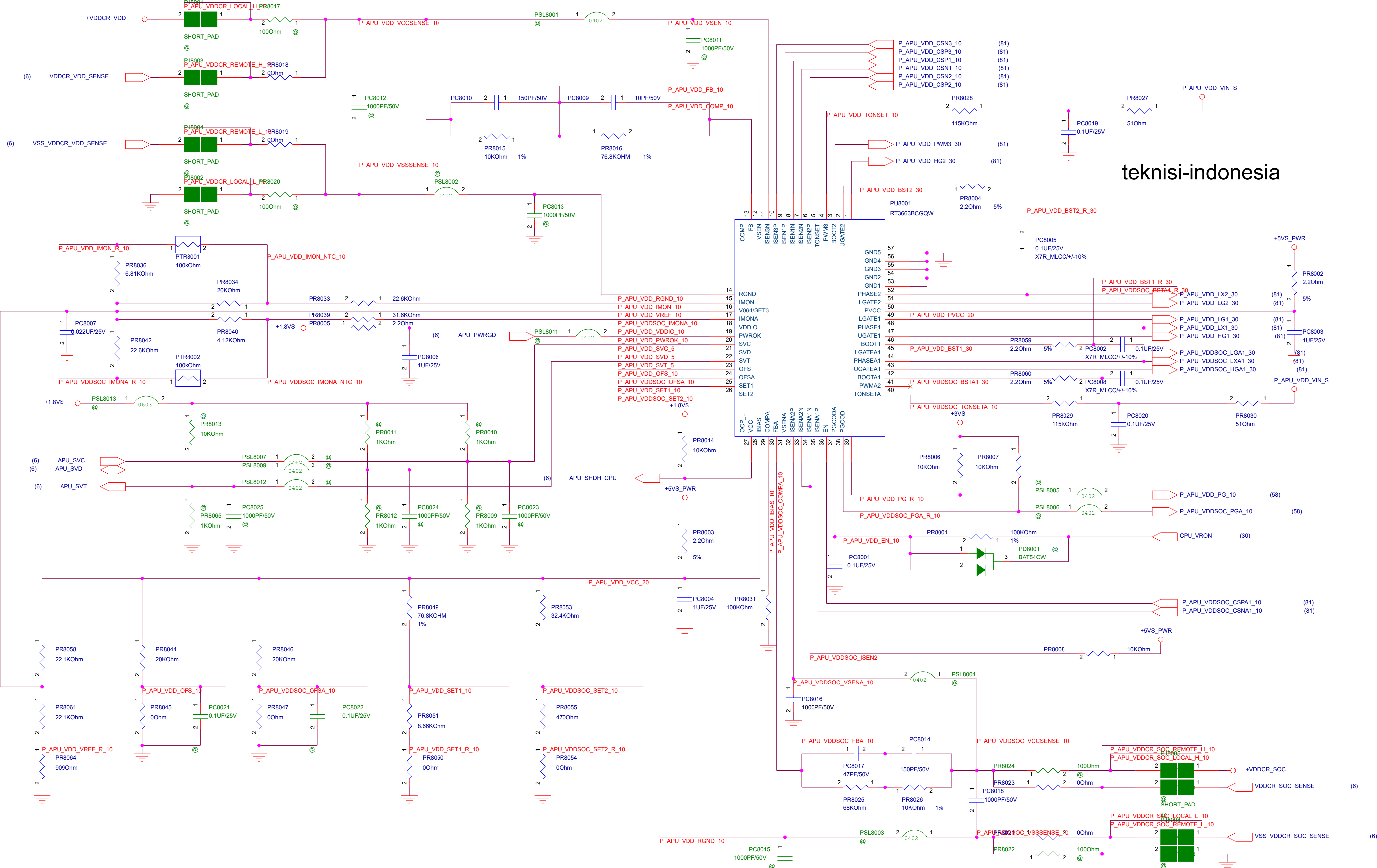
Title	<Title>	
Size A1	Document Number GX502GX	Rev R1.0
Date: Monday, April 29, 2019	Sheet 75 of 104	

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, April 29, 2019	Sheet 85 of 104	



Project Name: FX505DY

Rev: R1.0

Title : PW_APU (1)

Size: A3

Dept.: NB Power Team

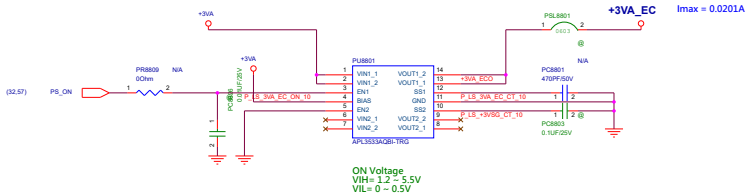
Engineer: CS Lin

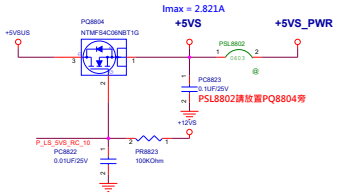
Date: Monday, April 29, 2019

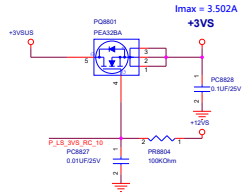
Sheet 80 of 104

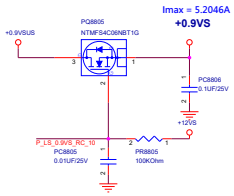
Load Switch

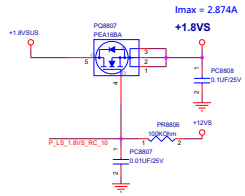
Main Board

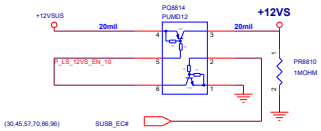










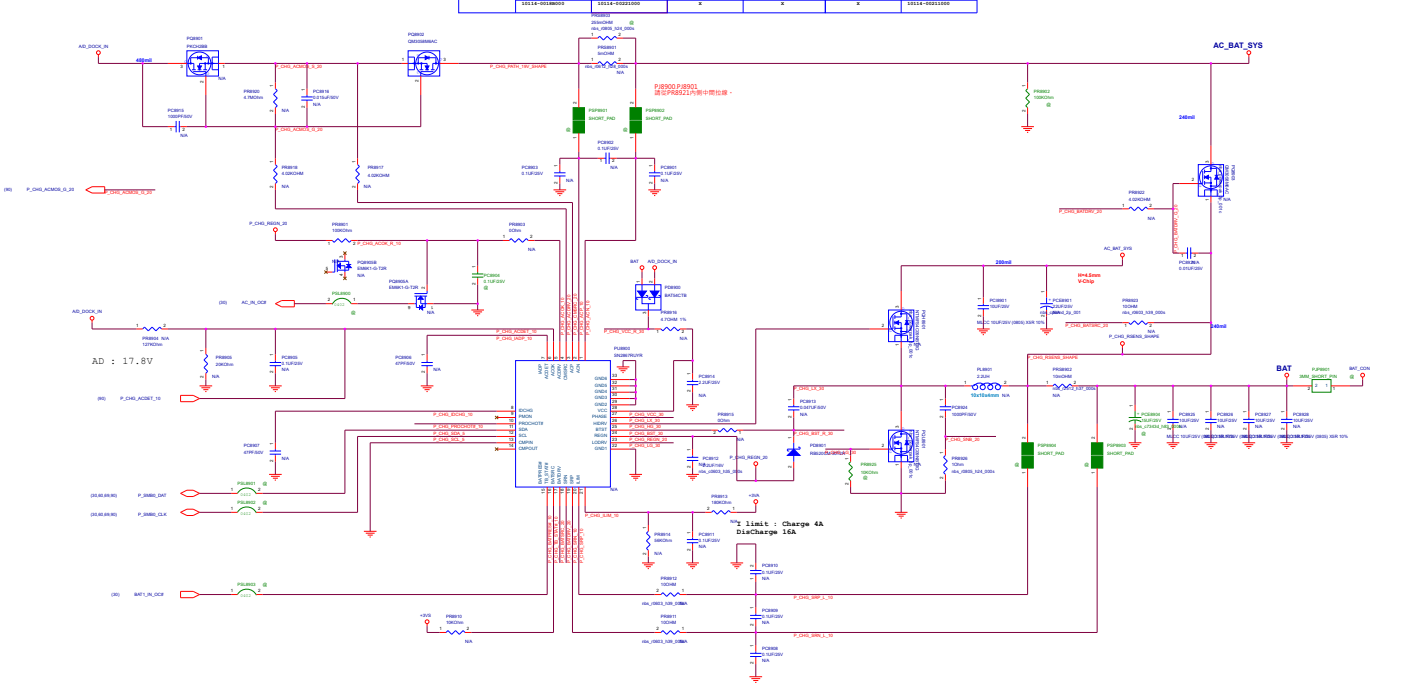


ASUS	Project Name: GX501GI		Rev: R1.0
Title : PW_LOAD SWITCH			
Size: A2	Dept.: NB Power team	Engineer: Ming	
Date: Monday, April 29, 2019	Sheet 88 of 104		

Main Board

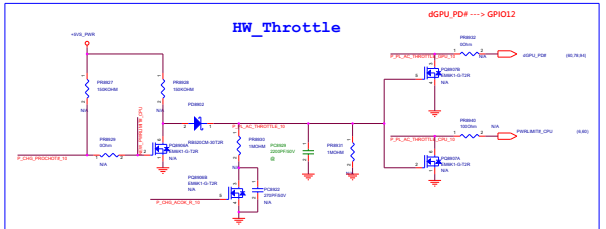
PR88901	ADP<120W	ADP<=230W	ADP>230W	ADP>330W
	TBD	5m	5m	2m
	TBD	10125-0008B100	10108-0008B000	10108-0008B000

PR88903	ADP<120W	ADP=150W	ADP=180W	ADP=230W	ADP=280W	ADP=330W
	200m	255m	X	X	X	560m
	10114-0018B000	10114-0021I000	X	X	X	10114-0021I000



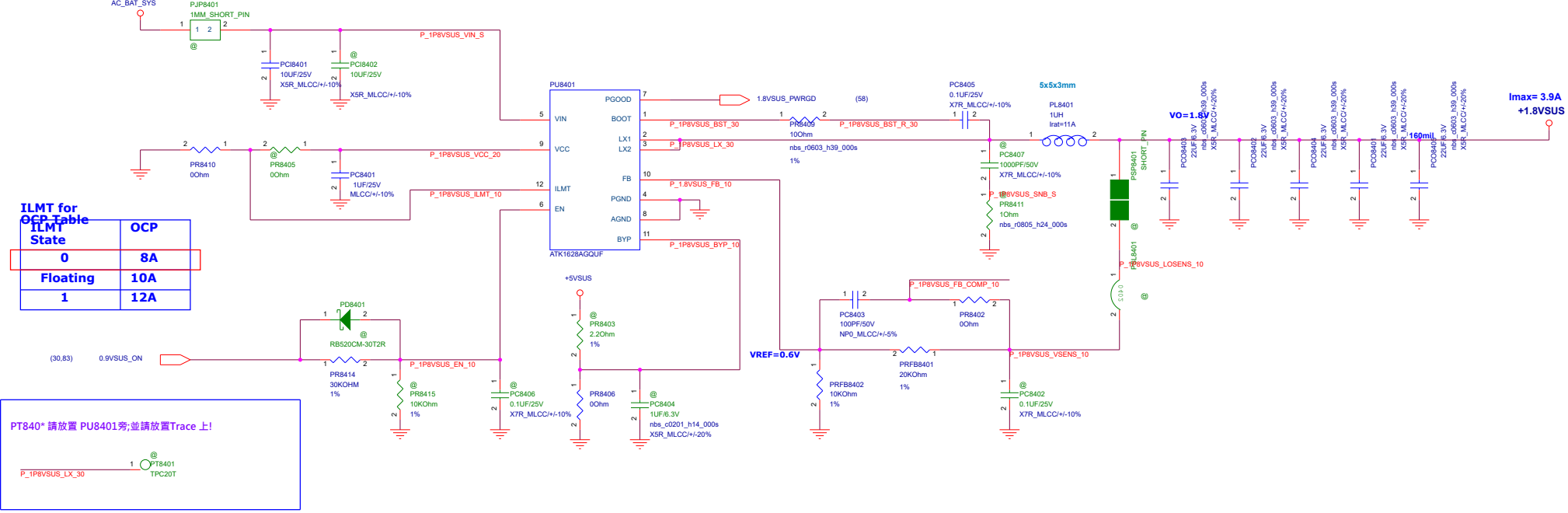
Adaptor select
total power = 90% ADP

Adaptor select			
	M Series	S Series	
PR8921	10m	5m	
PR8936			
14K	0.4V	30W	120W
31.6K	0.8V	40W	150W
56K	1.2V	45W	180W
93.1K	1.6V	65W	230W
150K	2.0V	75W	280W
270K	2.4V	90W	330W
560K	2.8V	120W	400W



ASUS	Project Name: Coffee lake-H	Rev: R1.0
Title :	PW_CHARGER	
Size: A2	Dept.: MB Power Team	Engineer: Benson
Date: Monday, April 29, 2019	Sheet: 85 of 104	

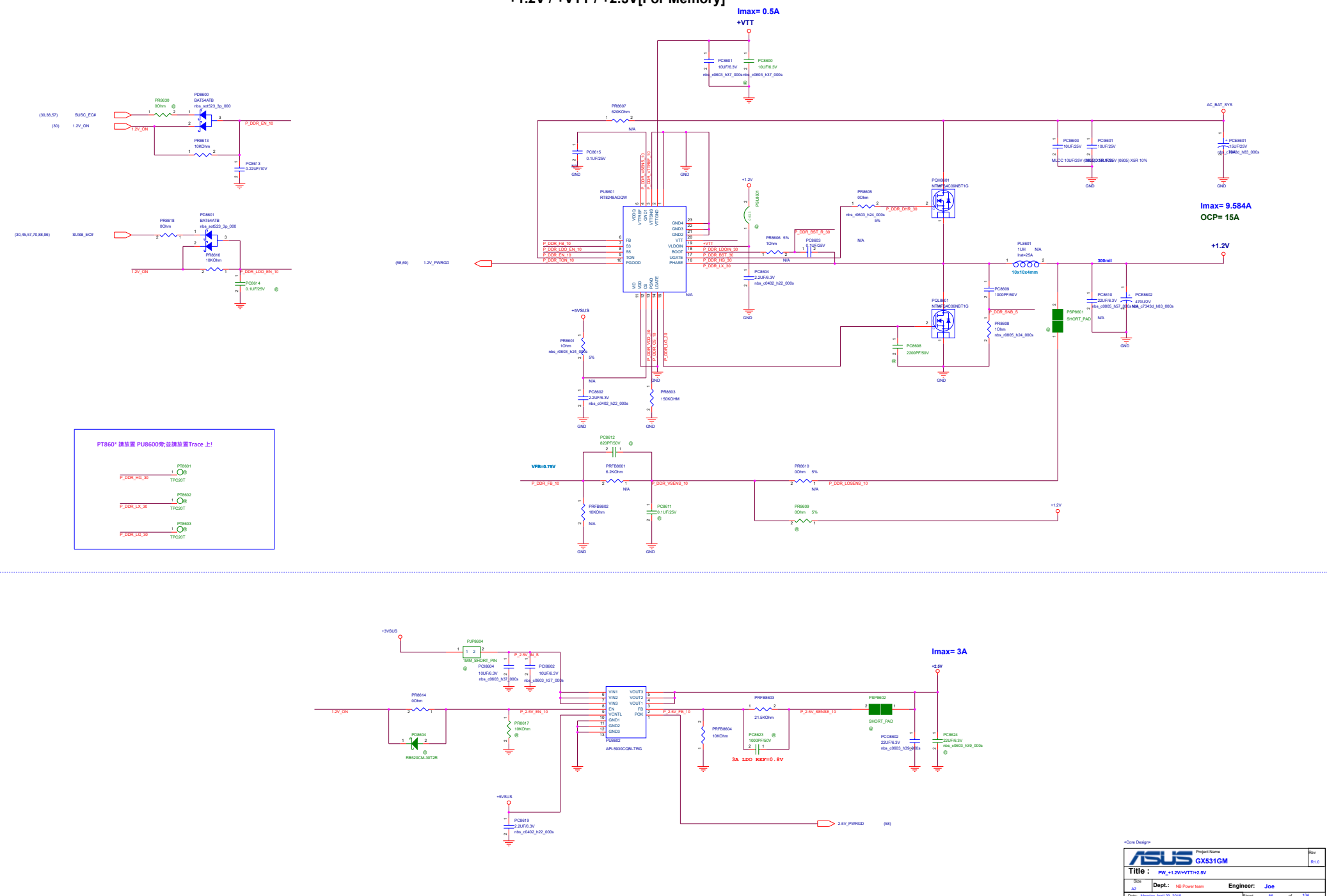
Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, April 29, 2019	Sheet 82 of 104	



<Variant Name>

Project Name: FX505DY		Rev: R1.0
Title : PW_+1.8VSUS		
Size: A3	Dept.: NB Power team	Engineer: CS Lin
Date: Monday, April 29, 2019	Sheet 84 of 104	

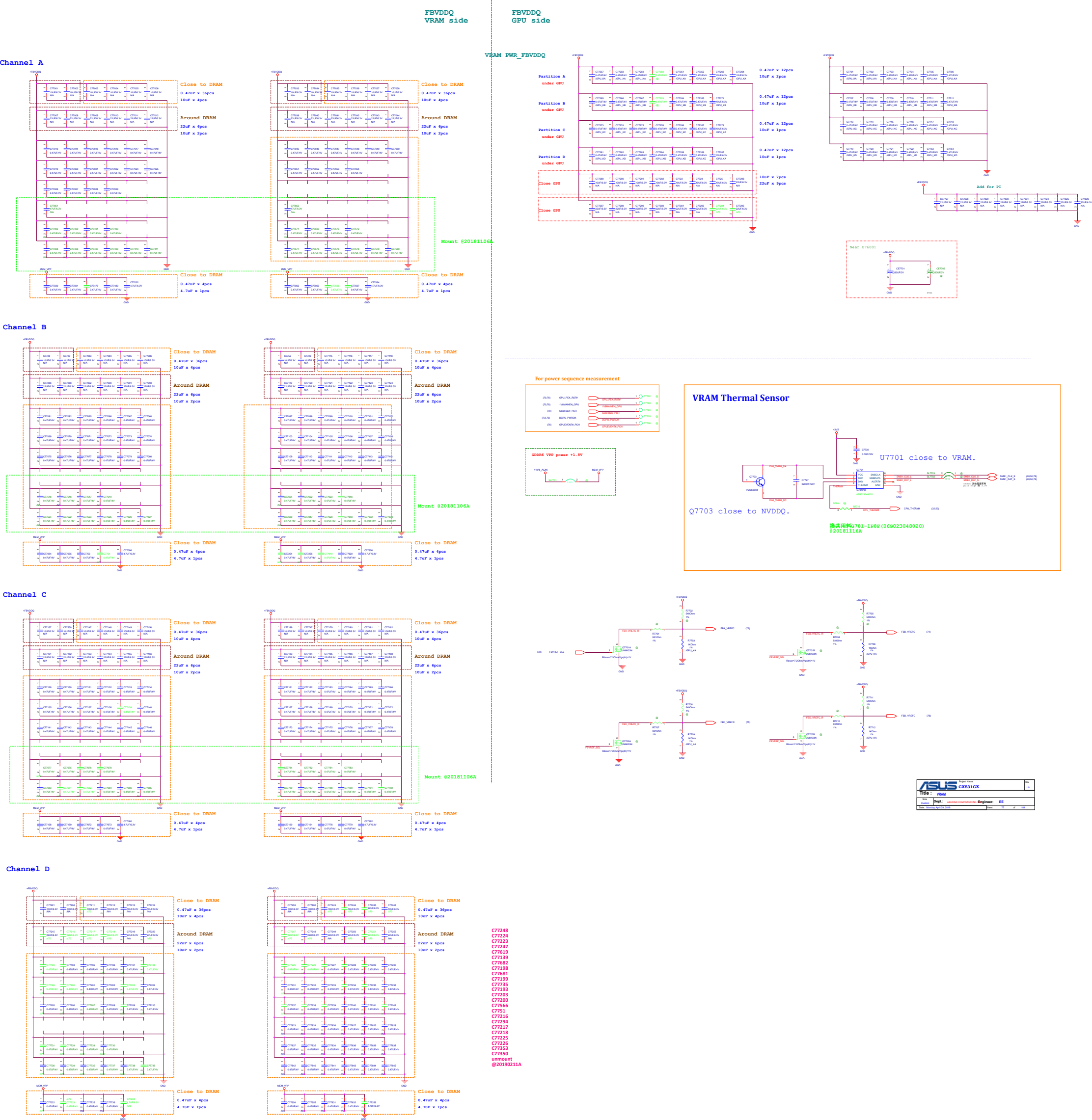
+1.2V / +VTT / +2.5V[For Memory]



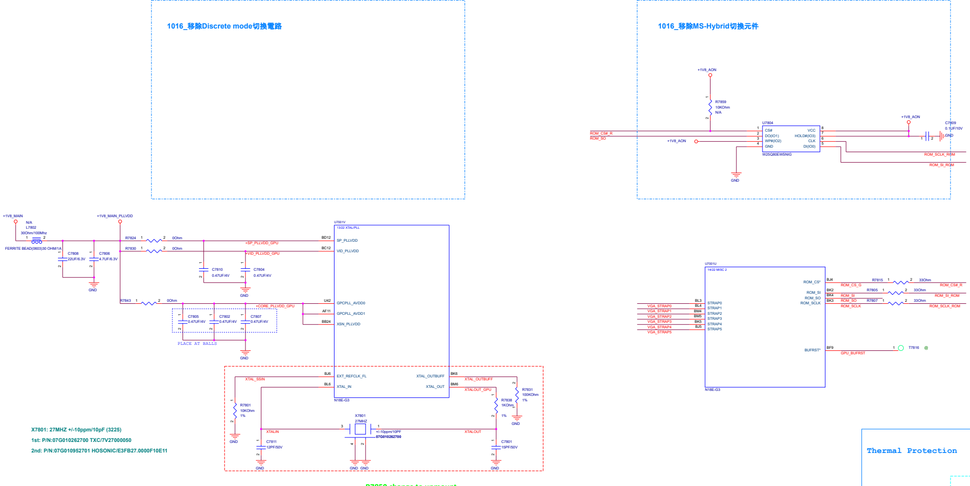
<Core Design>

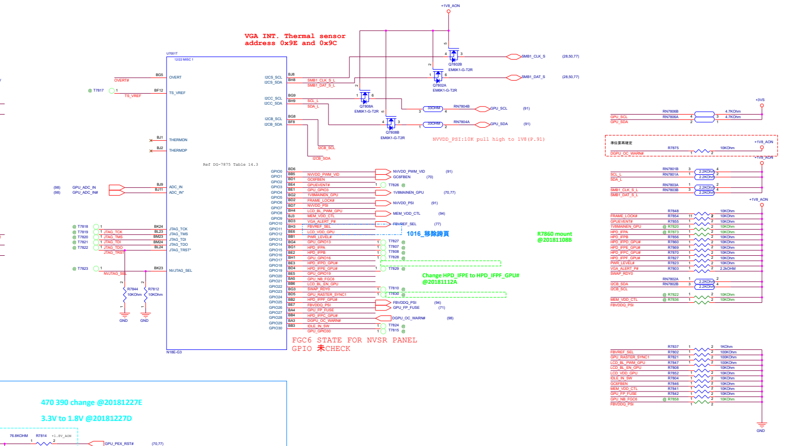
ASUS	Project Name: GX531GM		Rev: R1.0
Title :	PW_+1.2V/+VTT/+2.5V		
Size: A2	Dept.: NB Power team	Engineer: Joe	
Date: Monday, April 29, 2019	Sheet 86 of 104		

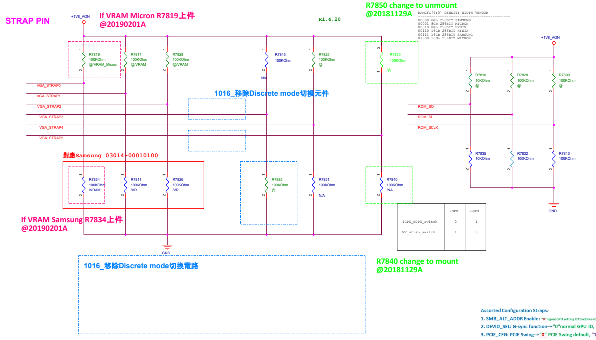
Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, April 29, 2019	Sheet 93 of 104	



FBVDDQ
VRAM side
FBVDDQ
GPU side
VRAM PWR_FBVDDQ
Channel A
Close to DRAM
0.47uF x 36pcs
10uF x 4pcs
Around DRAM
22uF x 6pcs
10uF x 2pcs
Mount @20181106A
Close to DRAM
0.47uF x 4pcs
4.7uF x 1pcs
Partition A
under GPU
Partition B
under GPU
Partition C
under GPU
Partition D
under GPU
Close GPU
Close GPU
0.47uF x 12pcs
10uF x 2pcs
0.47uF x 12pcs
10uF x 1pcs
0.47uF x 12pcs
10uF x 1pcs
0.47uF x 12pcs
10uF x 1pcs
10uF x 7pcs
22uF x 9pcs
Add for PI
Near U76001
Channel B
Close to DRAM
0.47uF x 36pcs
10uF x 4pcs
Around DRAM
22uF x 6pcs
10uF x 2pcs
Mount @20181106A
Close to DRAM
0.47uF x 4pcs
4.7uF x 1pcs
For power sequence measurement
GDDR6 VPP power +1.8V
VRAM Thermal Sensor
U7701 close to VRAM.
Q7703 close to NVDDQ.
換共用料Q781-1P8F(06G023048020)
@20181116A
Channel C
Close to DRAM
0.47uF x 36pcs
10uF x 4pcs
Around DRAM
22uF x 6pcs
10uF x 2pcs
Mount @20181106A
Close to DRAM
0.47uF x 4pcs
4.7uF x 1pcs
FBA_VREFC
FBB_VREFC
FBC_VREFC
FBD_VREFC
Channel D
Close to DRAM
0.47uF x 36pcs
10uF x 4pcs
Around DRAM
22uF x 6pcs
10uF x 2pcs
Close to DRAM
0.47uF x 4pcs
4.7uF x 1pcs
C77248
C77224
C77223
C77247
C77619
C77139
C77682
C77198
C77681
C77199
C77735
C77193
C77203
C77200
C77566
C7751
C77294
C77217
C77216
C77218
C77225
C77226
C77353
C77350
unmount
@20190211A
ASUS
GX531GX
Title : VRAM



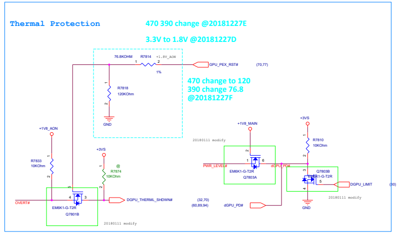


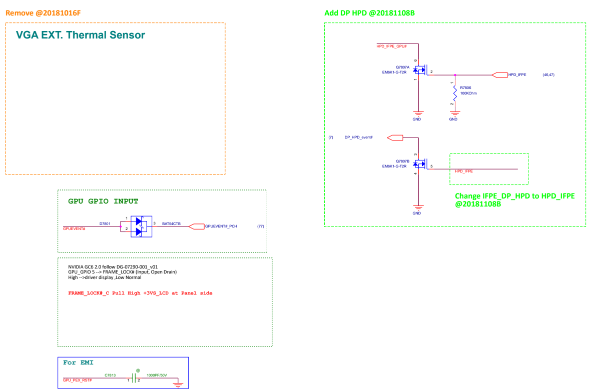


	Physical Configuration	
Level Option	Pull-Up to 1.8V via resistor (see Note 1). (Notebook designs also see Note 2.)	Pull-Down to GND via resistor Note 1
1.8V ("HIGH") Level	Populate	No Stuff
0.9V ("MIDDLE") Level	Populate	Populate
GND ("LOW") Level	No Stuff	Populate

Note 1: Resistor should be 100K Ohms. 5% tolerance is acceptable.
Note 2: Notebook graphics circuit designs should pull up to the 1V8_AON rail rather than to 1V8_MAIN.

Strap Pins see Note			FS_OVERT* Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function ENABLED
L	L	H	FS_OVERT* function DISABLED (Reserved; do not configure)
all other configurations			(Invalid; do not configure)





GPIO Pin Name	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	No Pull Up or Down
GPIO1	GC6:GC6_FB_EN	O		10K Pull Down
GPIO2	GC6:GPU_EVENT*	I		10K Pull Up
GPIO3	UNUSED	O		
GPIO4	GC6:1V8_MAIN_EN	O		10K Pull Up
GPIO5	FRAME_LOCK*	I	Frame lock	10K Pull UP
GPIO6	NVVDD_PSI*	O	Phase Shedding (see Section 14.1.3)	PU/PD with series resistor depending on PSI topology
GPIO7	LCD_BL_PWM	I/O	LCD Panel Backlight PWM	100K Pull Down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	PU/PD depending on DVS topology
GPIO9	THERM_ALERT*	O	Active Low Thermal Alert	10 kΩ Pull Up to 1V8
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	10K Pull Down
GPIO11	LCD_VCC	O		10K Pull Down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	10K Pull Up
GPIO13	UNUSED	O		
GPIO14	HPD_IFPA*	I	Hot Plug Detect for IFPA	10K Pull Up to 1V8_AON
GPIO15	HPD_IFPB*	I	Hot Plug Detect for IFPB	10K Pull Up to 1V8_AON
GPIO16	UNUSED	O		
GPIO17	HPD_IFPD*	I	Hot Plug Detect for IFPD	10K Pull Up to 1V8_AON
GPIO18	HPD_IFPE*	I	Hot Plug Detect for IFPE	10K Pull Up to 1V8_AON
GPIO19	Reserved	O		
GPIO20	GC6:NB_FGC6			10K Pull Down
GPIO21	LCD_BLEN		LCD Panel Backlight enable	100K Pull Down
GPIO22	SWAPRDY_IN			2.2K Pull Up, see circuit
GPIO23	RASTER_SYNC1			100K Pull Down
GPIO24	HPD_IFPF*/USBC_HPD* or DONGLE_DET*	I	Hot plug detect for IFPF or USBC	10K Pull Up to 1V8_AON
GPIO25	FBVDD_PSI	O		Pull Up/Pull down with series resistor depending on PSI topology
GPIO26	FP_FUSE			10K Pull Down
GPIO27	HPD_IFPC*	I	Hot plug detect for IFPC	10K Pull Up to 1V8_AON
GPIO28	INA_INT* / ADC_MUX_SEL			10K Pull Up
GPIO29	IDLE_IN_SW	I		10K Pull Down
GPIO30	UNUSED			

1016_移除HPD_IFPx開關電路

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

Assorted Configuration Straps-
1. SMB_ALT_ADDR Enable: "0" signal GPU setting I2CS address 0x9E, "1" Dual GPU setting I2CS address add 0x9C, used when a second GPU
2. DEVID_SEL: G-sync function→"0"normal GPU ID, "1" support G-sync GPU ID
3. PCIE_CFG: PCIE Swing→"0" PCIE Swing default, "1" PCEI swing reduce
4. VGA_DEVICE: Graphics circuit→"0" MS-Hybrid, "1" Discrete

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

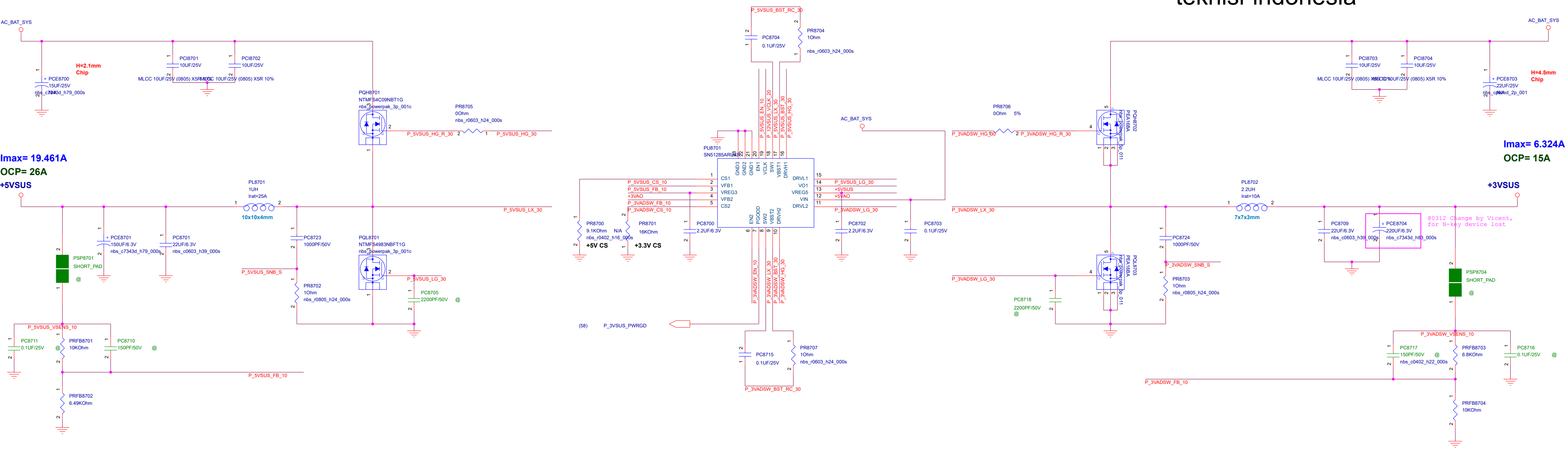
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

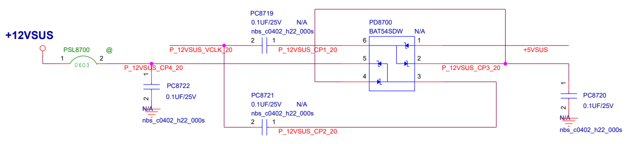
DEFULT : L L H

ASUS	Project Name: GX502GX		Rev: R1.3
Title : GPU_CLOCK/STRAP/GPIO			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1	
Date: Monday, April 29, 2019		Sheet 78	of 104

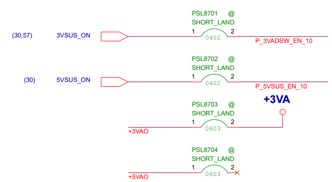
+3VA_DSW / +5VSUS [System Power]

teknisi-indonesia





請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm



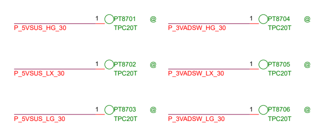
Adaptor Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0

PT870* 請放置 PU8700旁;並請放置Trace 上!

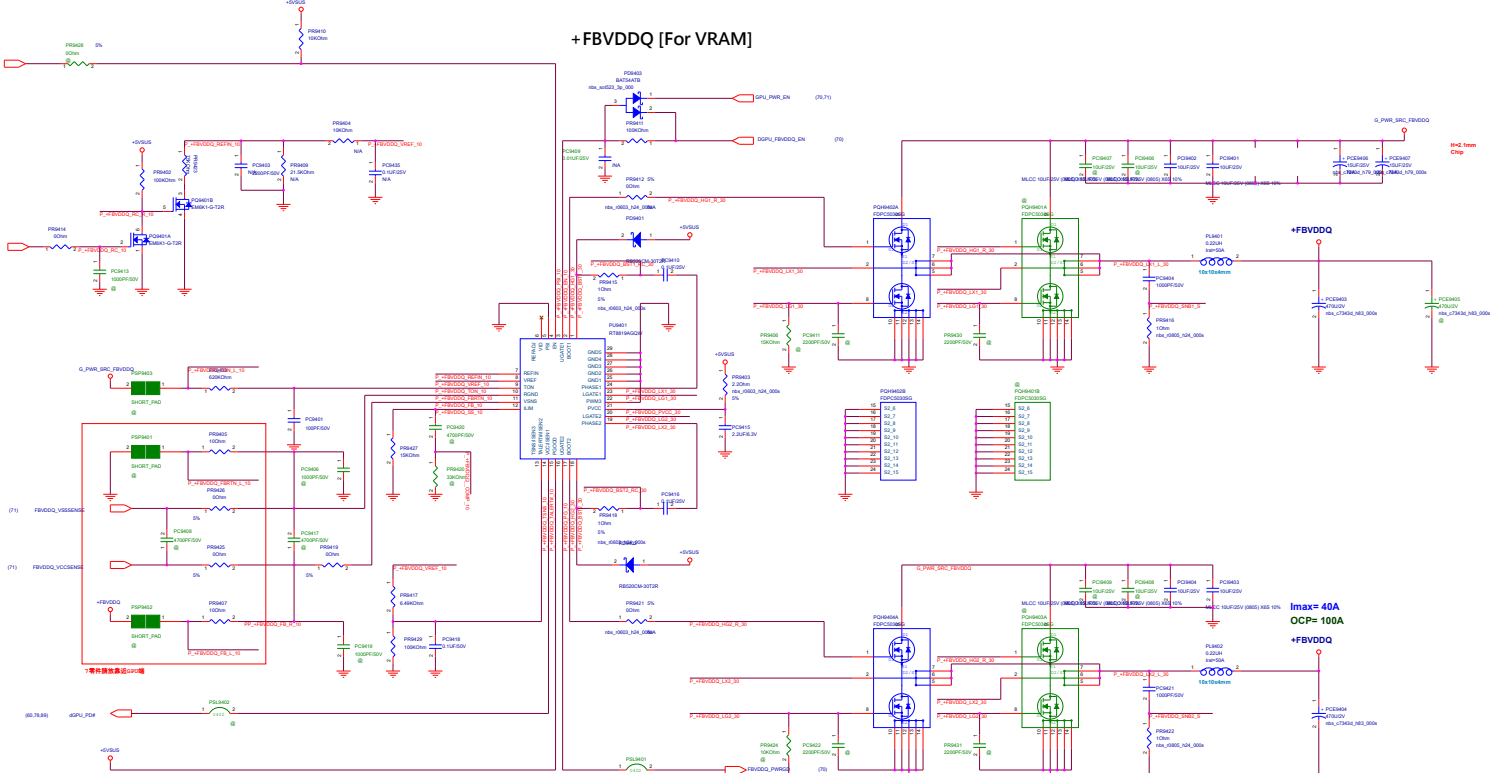


<Variant Name>

Project Name: Coffelake-H
Rev: R1.0
Title : PW_+3VA_DSW/+5VSUS
Size: A2
Dept.: NB Power team
Engineer: Joe
Date: Monday, April 29, 2019
Sheet 87 of 104

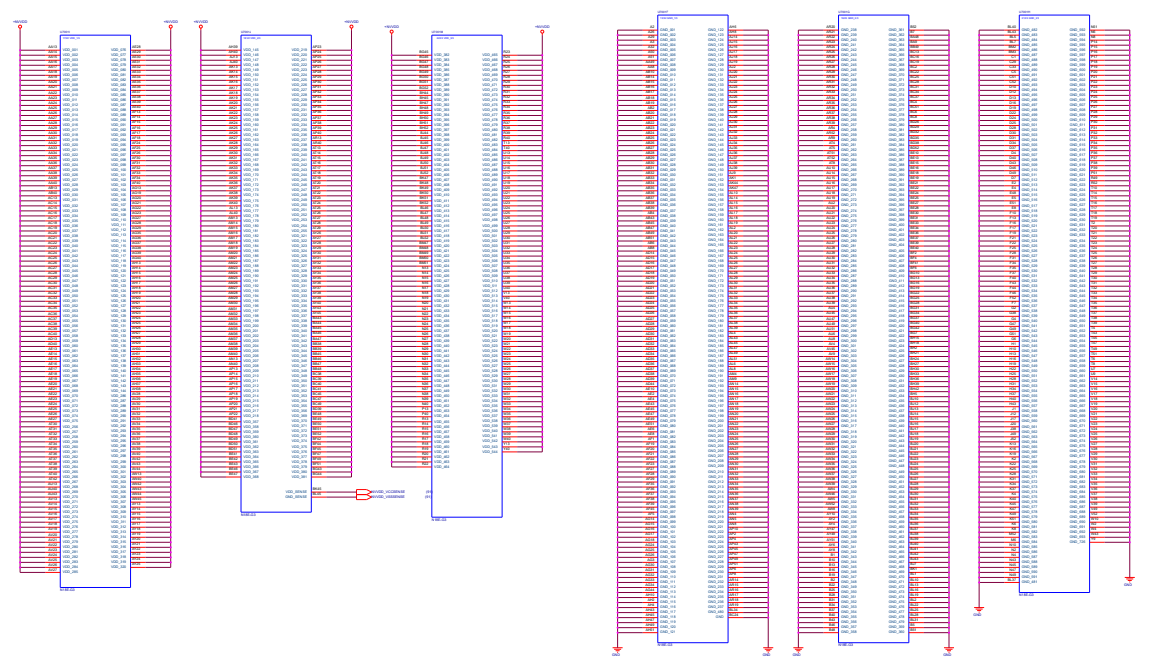
+FBVDDQ [For VRAM]

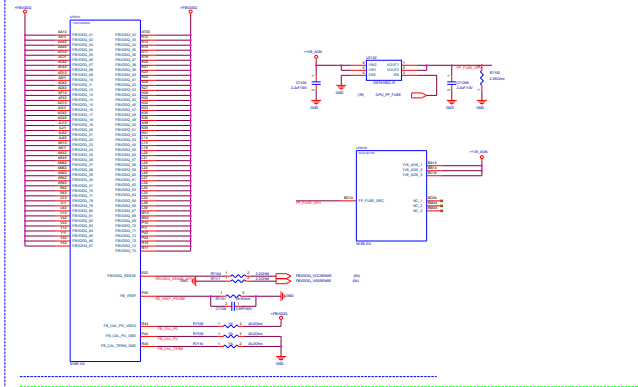
DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.35V	1.25V
R9R404	10KOhm	
R9R409	21.5KOhm	
R9R423	75KOhm	



<Variant Name>	Project Name: GM531GX	Rev: R1.0
	Title : PW_+FBVDDQ	
Size: Custom	Dept.: NB Power Team	Engineer: Joe
Date: Monday, April 29, 2019	Sheet: 94 of 104	

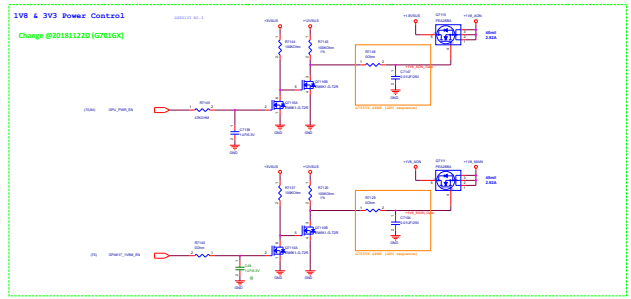
Main Board



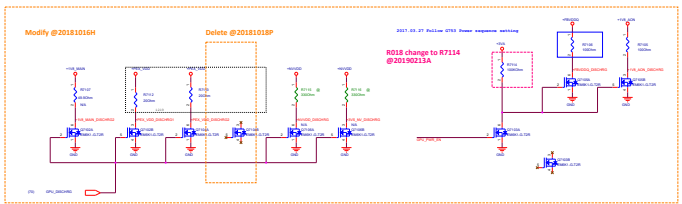


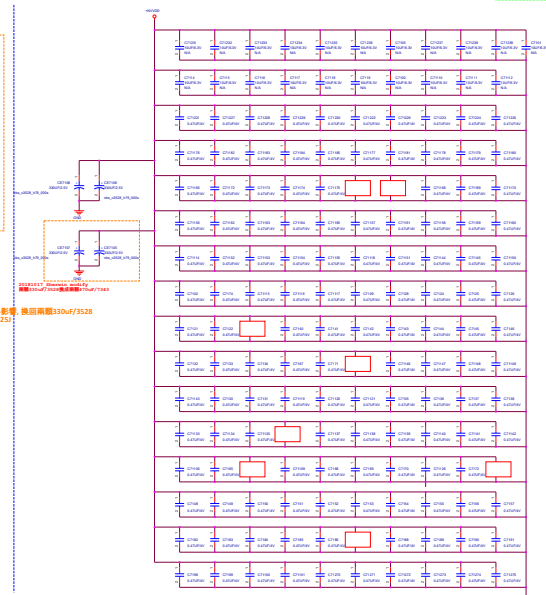
1V8 & 3V3 Power Control

Change @20181122D (G701GX)

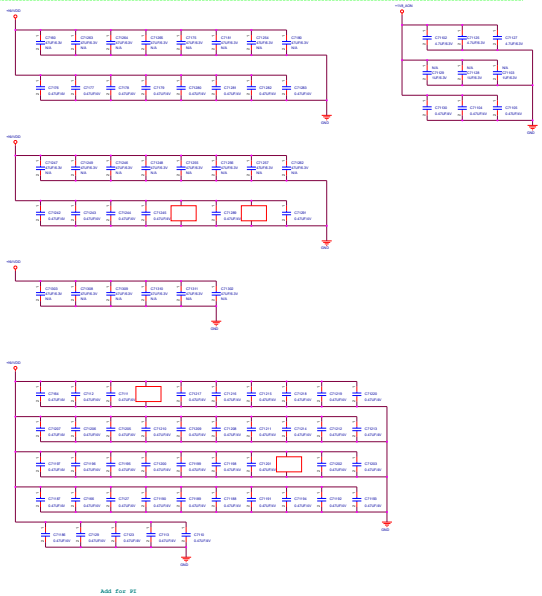


Discharge Discharge

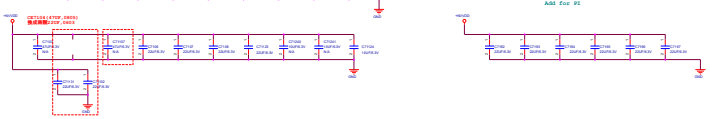




元件大小影響, 換回兩顆330uF/3528
@20180025I



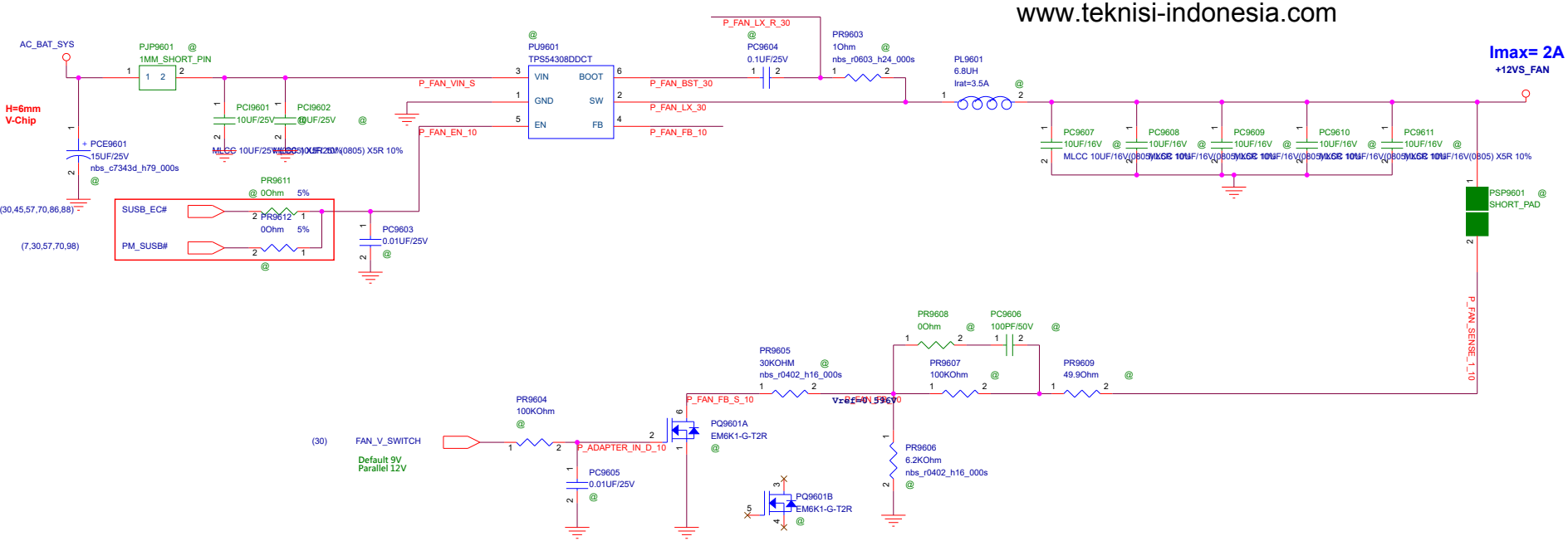
Add for PI



ASUS	Project Name: GX701		Rev: 1.0
Title :	GPU POWER		
Size: Custom	Dept.:	Engineer: Ashton_yang	
Date: Monday, April 08, 2019		Sheet: 71 of 100	

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, April 29, 2019	Sheet 95 of 104	

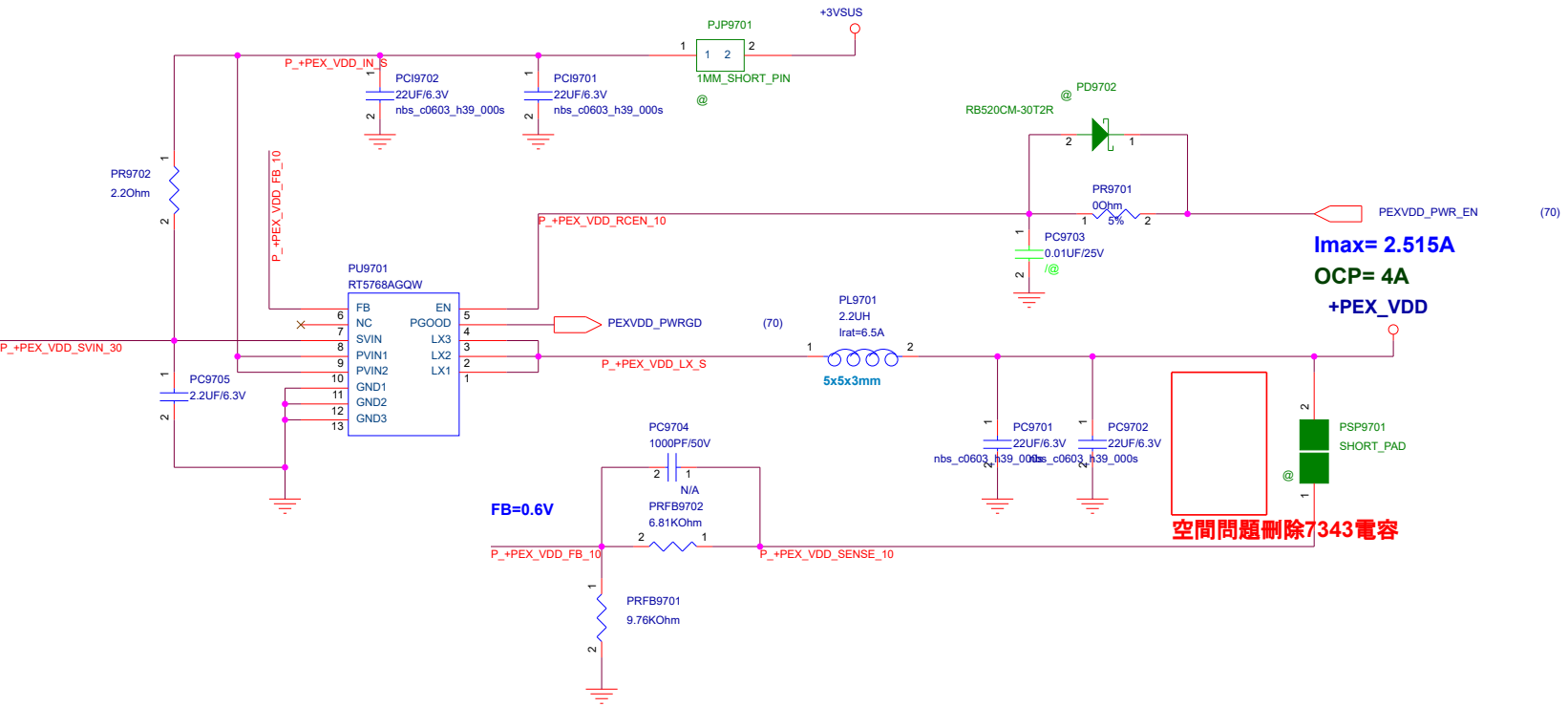
+12VS_FAN [For FAN]



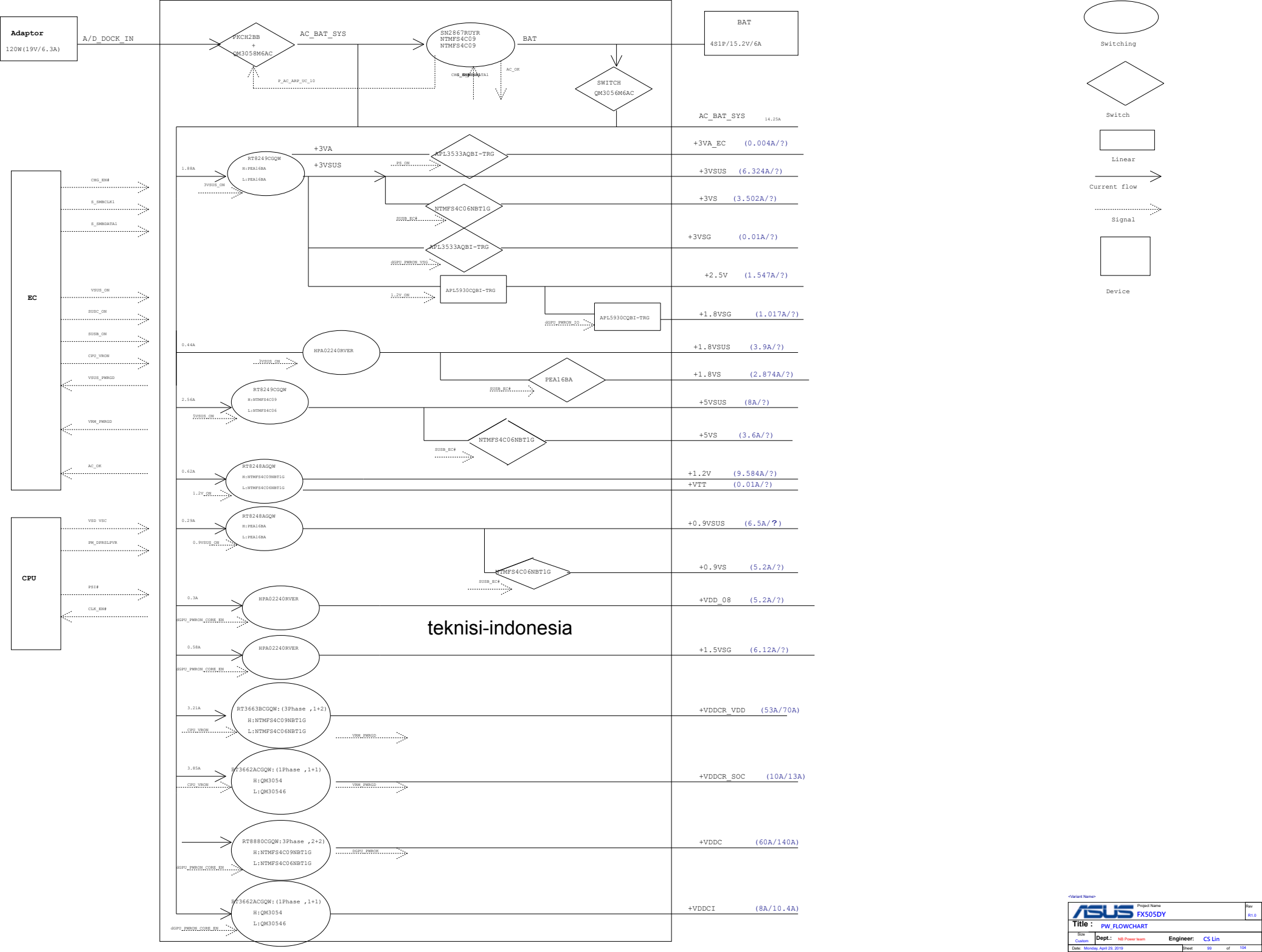
<Variant Name>

Project Name: Coffeelake-H		Rev: R1.0
Title : PW_+12VS_FAN		
Size: B	Dept.: NB Power team	Engineer: Hon
Date: Monday, April 29, 2019	Sheet 96 of 104	

PEX_VDD [For GPU]



ASUS	Project Name: G703GI	Rev: R1.0
Title : *****		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: HON	
Date: Monday, April 29, 2019	Sheet 97 of 104	



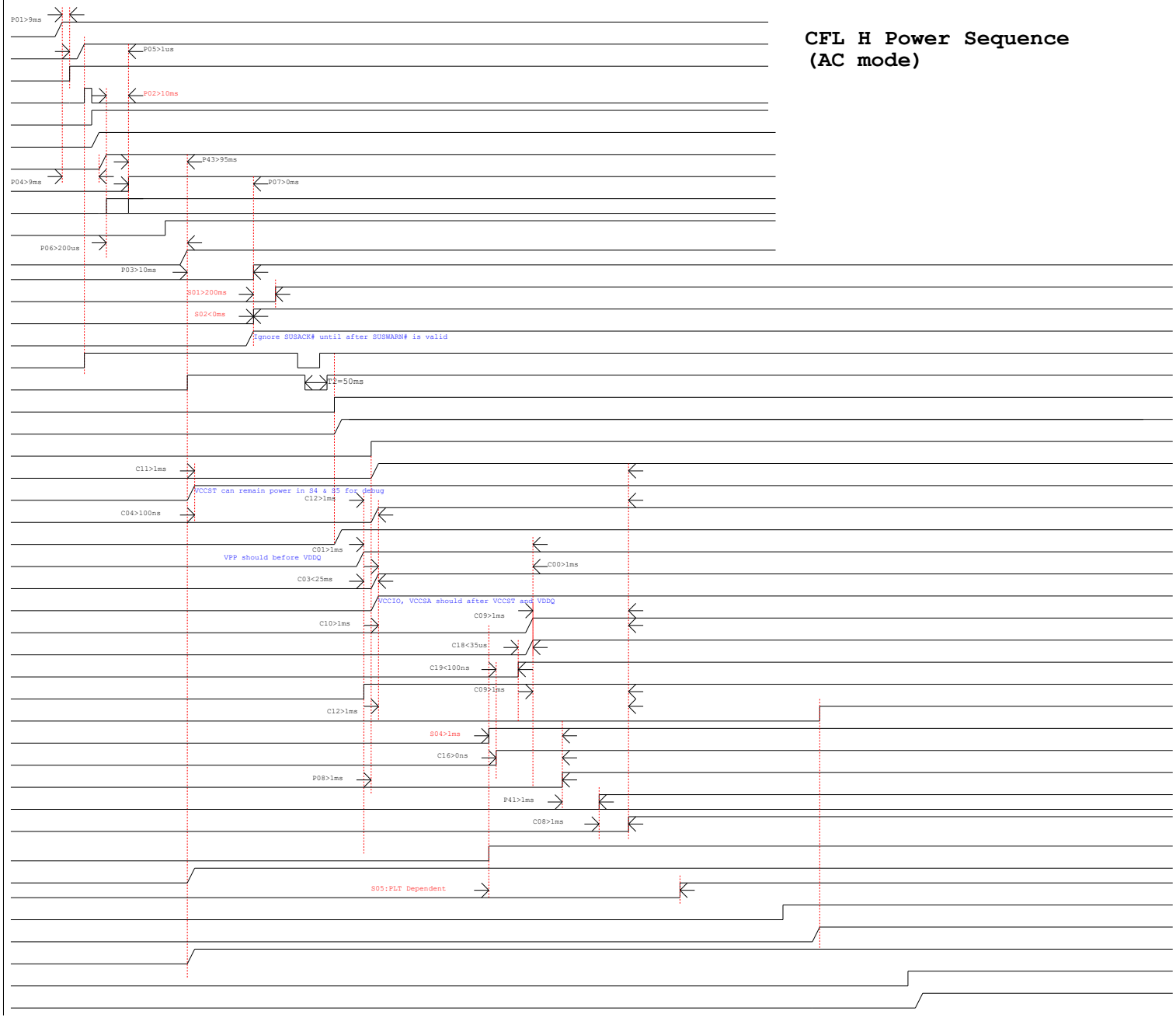
<Variant Name>

ASUS	Project Name: FX505DY	Rev: R1.0
Title : PW_FLOWCHART		
Size: Custom	Dept.: NB Power team	Engineer: CS Lin
Date: Monday, April 29, 2019	Sheet 99 of 104	

AC-IN Mode

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#) +12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#) +12VS/+5VS/+3VS
(SUSB_EC#) +1.0V_VCCST, VCCPLL
(SUSB_EC#) +VCCIO, (+12VS) +VCCSTG
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
(+12VS) +VCCPLL_OC
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL) +0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT



CFL H Power Sequence (AC mode)

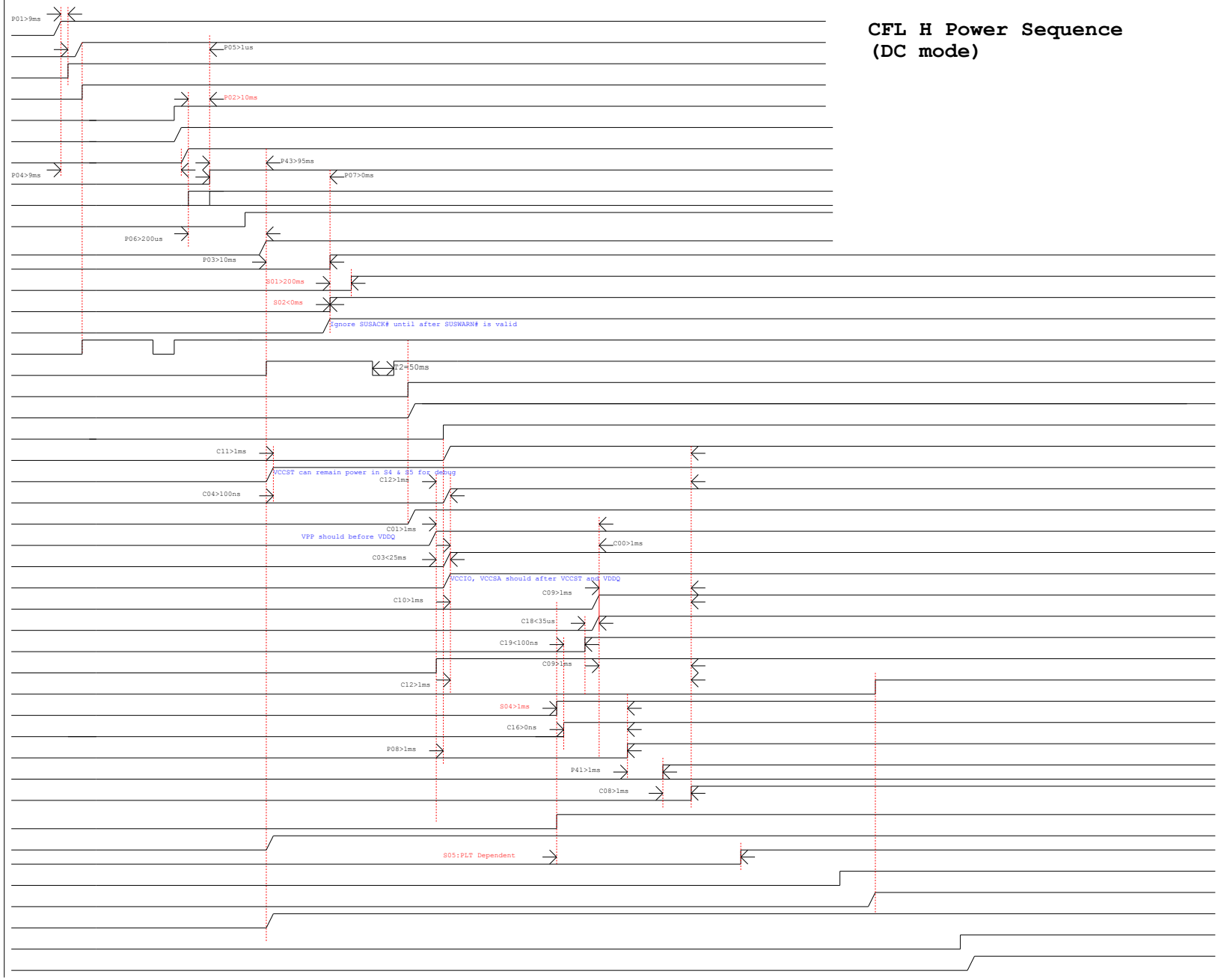
ASUS	Project Name: GX502GX		Rev: 1.0
Title : Power On Timing--AC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1	
Date: Monday, April 29, 2019	Sheet 100 of 104		

CFL H Power Sequence (DC mode)

DC-IN Mode

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#) +12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#) +12VS/+5VS/+3VS
(VSUS_ON) +1.0V_VCCST,VCCPLL (VCCST_PWRGD)
(+VCCIO) +VCCSTG
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
(+12VS) +VCCPLL_OC
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL) +0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT



ASUS	Project Name: GX502GX		Rev: 1.0
Title : Power On Timing-DC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: NB1 RD2 EE1	
Date: Monday, April 29, 2019	Sheet 101 of 104		

Rev	Date	Description
1.0	2017.03.03	P21 Remove CN
	2017.03.04	Q5602, Q5601 change for DXF Limitation
	2017.03.10	+1V9_MAIN, +3VS_NV Follow G753 Power sequence setting
	2017.03.11	R7821 Follow GL702 GPU Power seq
	2017.03.11	+PEX_VDD GPU Sequence update
	2017.03.14	PCE8104, PCE8107, PCE8106 update Cap for DXF Limit
	2017.03.14	GX501VIK Remove useless nut in P67
	2017.03.15	J5301 Connector list update
	2017.03.15	H6716, H6706, H6724, H6723 Screw Hole update
	2017.03.16	J5602 change LID SW for Angle Simulation
	2017.03.17	EMI Reserve C5606, C5607 Cap
	2017.03.17	RM3002, L4512, L4513, L4504, L4515, L4505 SWAP for Layout
1.1	2017.03.21	P30, P37, P39 AMP Change SNL04M25555
	2017.03.21	EMI Reserve P30 C77360 Cap and P69 Caps and Spring
	2017.03.23	AMP Change Remove P37 MUTE CONTROL schematic
	2017.03.23	AMP Change Reserve Q3701
	2017.03.27	P71 +PBVDDQ Discharge setting Follow G753 Power sequence setting
	2017.03.29	P12 Remove TBT Power Low Switch for Layout
1.2	2017.03.30	Change Cap C7105, C7101 for thermal request
	2017.03.30	Thermal Request for H6728
	2017.04.05	EMI Reserve Cap and Spring in P69
	2017.04.06	Reserve C2601 for +VCCPGPP_EF Ripple
	2017.04.07	25.00MHZ Cap C1126, C1124 change for Vendor Suggest
	2017.04.07	27MHz Cap C7811, C7801 change for Vendor Suggest
2.0	2017.04.11	P48 Reserve 0 ohm for SDA and SCL
	2017.04.17	P71 Add Caps for NVVDD Ripple
	2017.04.18	Q5704 Chnage MOS for DXF Limitation
	2017.04.20	P71 Add Caps for NVVDD Ripple
	2017.04.21	P67 Screw Hole H6705 update
	2017.04.21	P71 Add Caps for NVVDD Ripple C71119~C71122
	2017.04.25	P71 C7122, C7123, C7127, C7135, C7143, C7144, C7156, C7164, C7166,, C7186, C7187 change to 10UF
	2017.04.25	P70 C7007, C7002 change to 4.7UF
	2017.04.25	P70 C7020, C7024 change to 22UF
	2017.05.02	EMI Reserve C6948, C6949, C6950, C6951, C6952, C6953, C6954 and remove U6913
	2017.05.02	H6711, H6712 change screw hole type fot EMI Solution
	2017.05.03	Remove J4502 Pin 36 GND fot Factory Issue
	2017.05.05	P88, P58 Remove VCCST_PWRGD signal
	2017.05.05	P79, P45 Remove eDP Lan2 and Lan3 Signal
	2017.08.10	P31 R3121,R3122 change to unmount

Rev	Date	Description

Rev	Date	Description

Rev	Date	Description

ASUSTeK COMPUTER INC.

Title : Revision History

Engineer: EE

Size: D | Project Name: GX502GX | Rev: 1.0

Date: Monday, April 09, 2018 | Sheet 102 of 106

1. P.01-30 reference FX505DY, P.31-104 reference GX502_(WW39_20180927C)
2. Net connection_(WW39_20180928A)
20181004
P.03
P.07
P.30 Copy FX505DY P.30
P.32 Modify Reset circuit
P.34 Modify LAN connector
P.35 Modify N-KEY IT8291E to IT8299E
P.36 線路
P.37 Modiffy Headpohne, Mic, ESS
P.39 Remove Mute control
P.40 Modify circuit
P.41 Modify circuit & 螺孔, 0 ohm先keep
P.45 Add Mic and HDR circuit
P.48 Keep SL4802
P.49 Modify circuit
P.50

ASUS	Title : GM531GX_SKU Table_R1.0		
ASUSTeK COMPUTER	Engineer: EE		
Size C	Project Name GX502GX		Rev 1.0
Date: Monday, April 29, 2019	Sheet 104 of 104		

9. Card Reader: AU6435--02G630002400 (Page42)

10. USB Charger IC: (Page52) Silego SLG55584AVTR -- 06016-00040000
MAXIM MAX14566AEETA+ -- 06G016196011

11. USB3.0 Repeater IC:(Page67)
Parade : PS8710B -- 06053-00200000
Maxim : MAX14972CTG+ -- 06053-00030000

13. Audio Codec : 02043-00130000 (663-VA4)

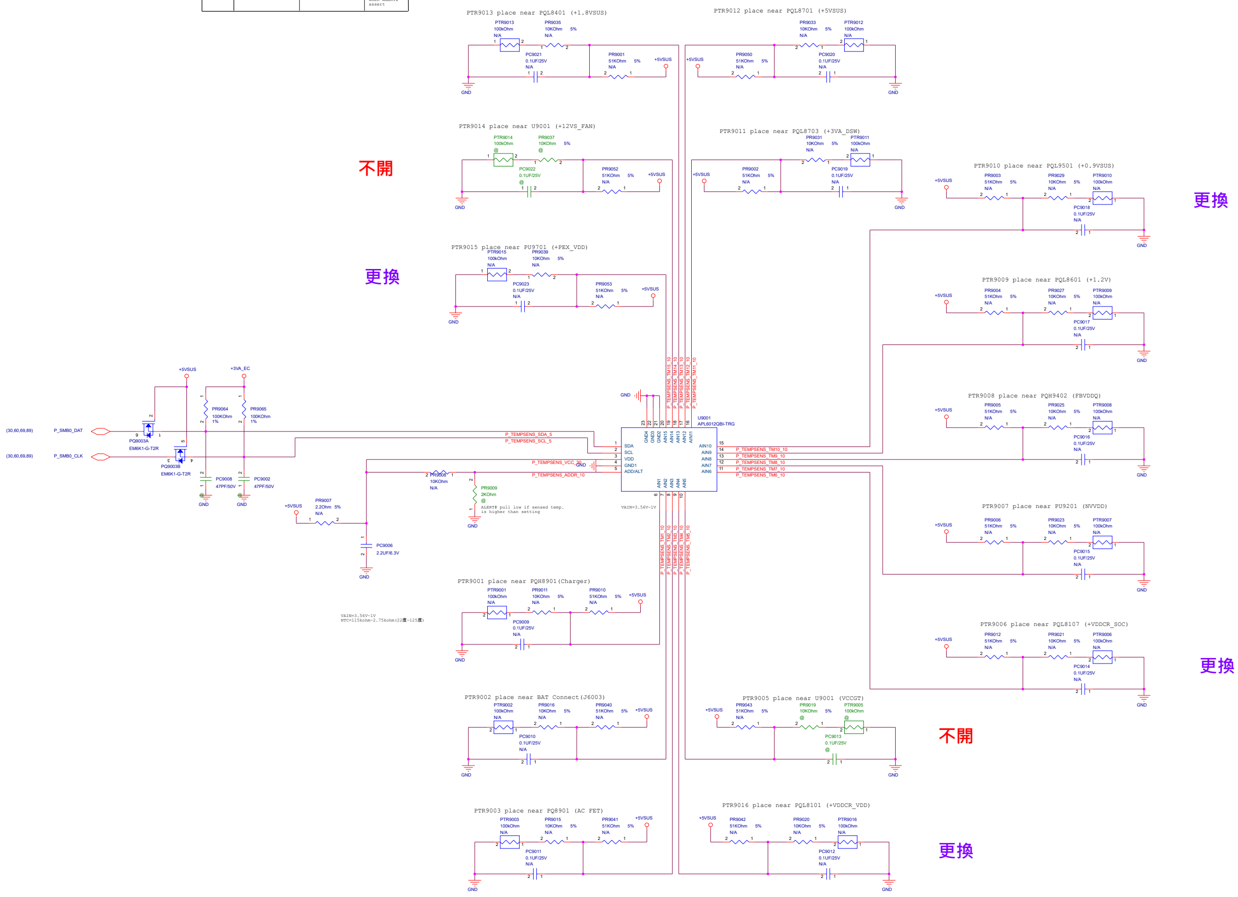
Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Register Address

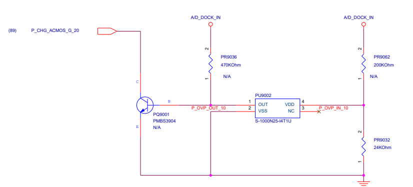
Address	0x00 0x01 0x02	0x03 0x04 0x05	0x06
R/W	W W W	R R R	R
Function	Temp. alert threshold setting	Sensed temp. data	bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert

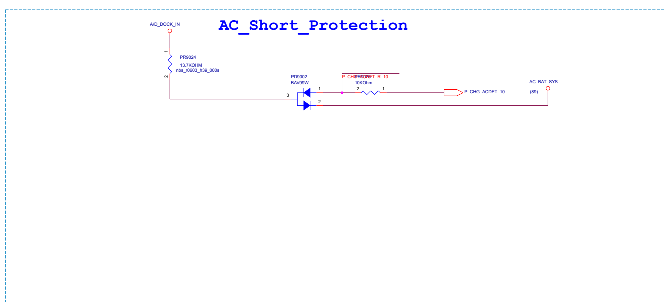
PROTECTION



PTR9013 place near PQL8401 (+1.8VSUS)
PTR9012 place near PQL8701 (+5VSUS)
PTR9014 place near U9001 (+12VS_FAN)
PTR9011 place near PQL8703 (+3VA_DSW)
PTR9010 place near PQL9501 (+0.9VSUS)
PTR9015 place near PU9701 (+PEX_VDD)
PTR9009 place near PQL8601 (+1.2V)
PTR9008 place near PQH9402 (FBVDDQ)
PTR9007 place near PU9201 (NVVDD)
PTR9001 place near PQH8901(Charger)
PTR9006 place near PQL8107 (+VDDCR_SOC)
PTR9002 place near BAT Connect(J6003)
PTR9005 place near U9001 (VCCGT)
PTR9003 place near PQ8901 (AC FET)
PTR9016 place near PQL8101 (+VDDCR_VDD)
不開
更換
更換
更換
不開
更換
U9001
APL6012QBI-TRG
P_SMB0_DAT
P_SMB0_CLK
P_TEMPSENS_SDA_5
P_TEMPSENS_SCL_5
P_TEMPSENS_VCC_10
P_TEMPSENS_ADDR_10
ALERT# pull low if sensed temp. is higher than setting
+5VSUS
+3VA_EC
GND

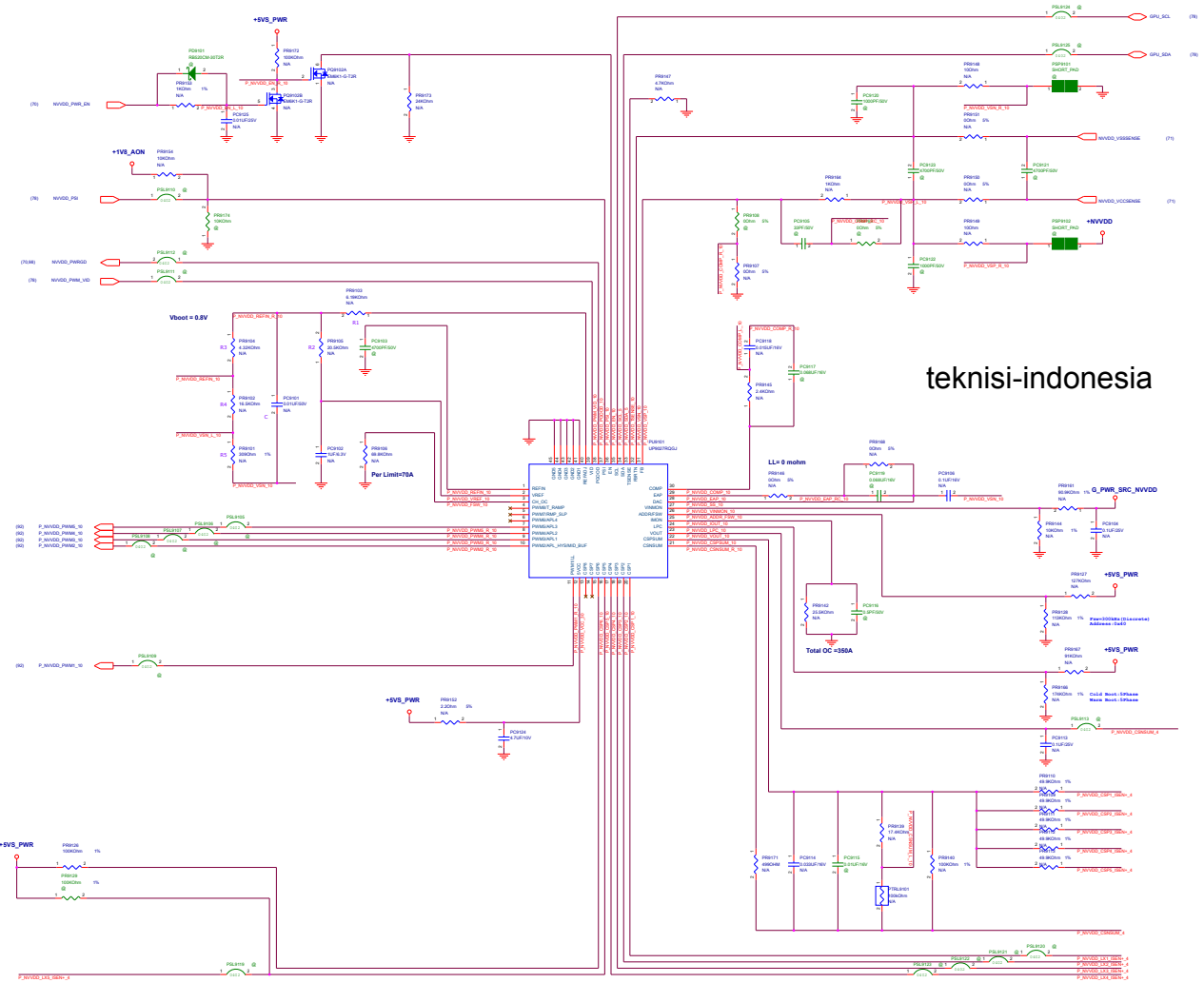
OVP Protection circuit 24V==>Cost down



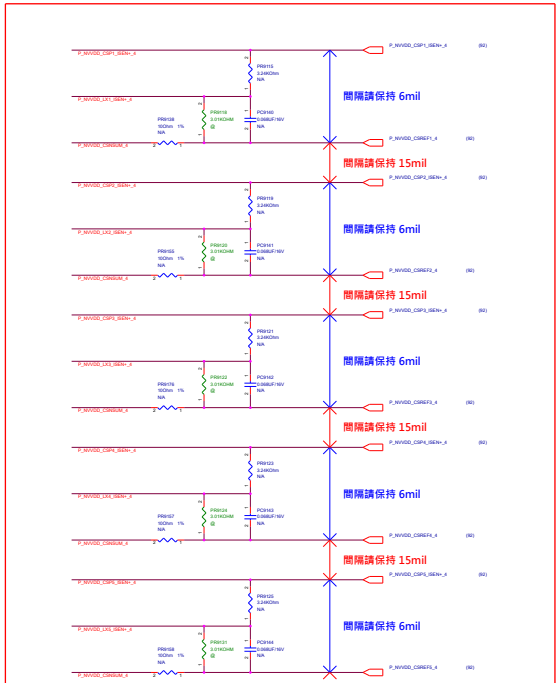


Project Name GM501GS
Title : PW_PROTECTION
Dept.: NB Power Team
Engineer: Edison
Date Monday, April 29, 2019
Sheet 90 of 104

+NVVDD [For DGPU]

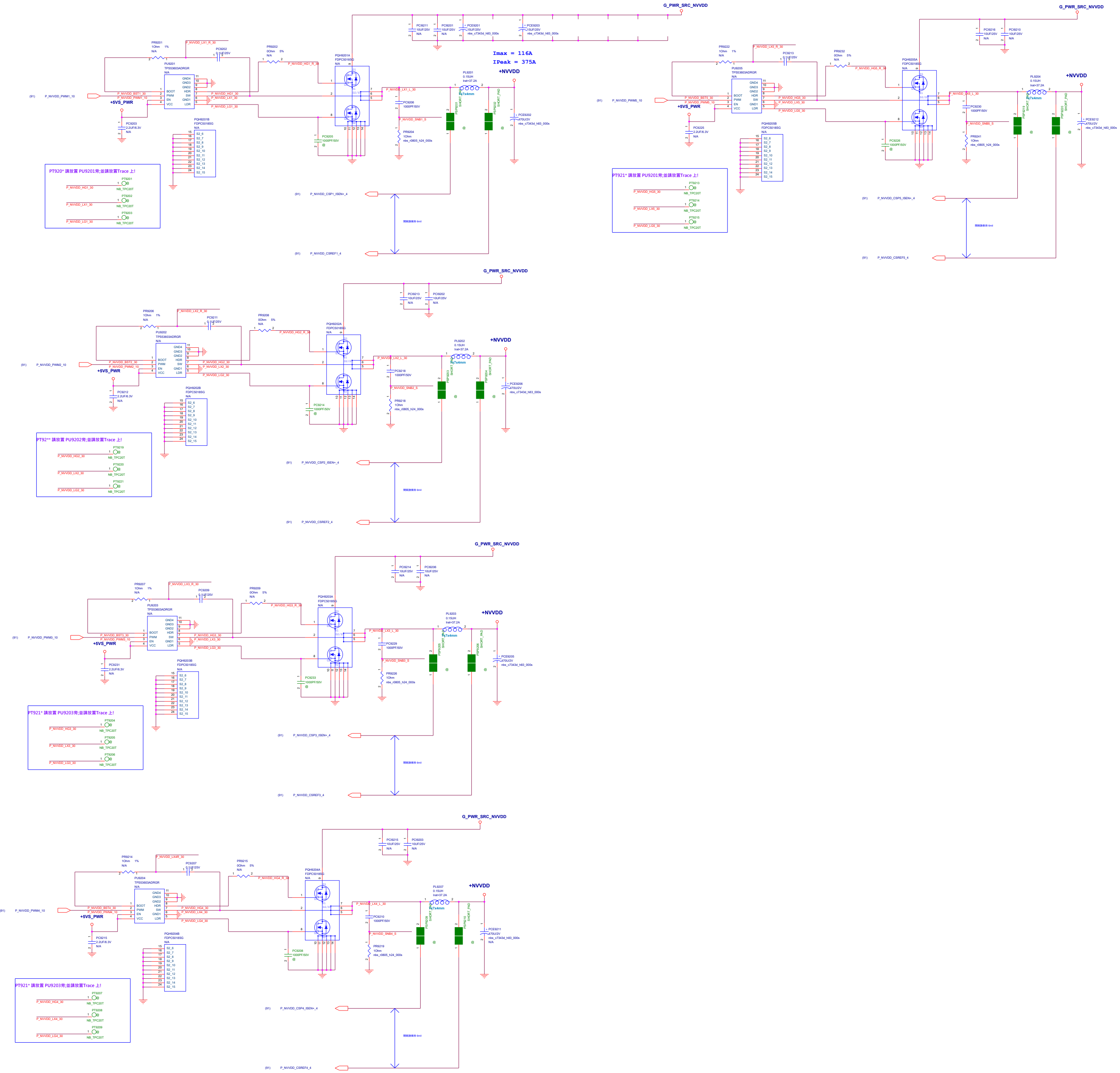


請放靠近PU9101



ASUS	Project Name: G711GW		Rev: R1.0
Title :	PW_+NVVDD (1)		
Size: A0	Dept.: NB Power team	Engineer: Neil	
Date: Monday, April 29, 2019	Sheet 91 of 104		

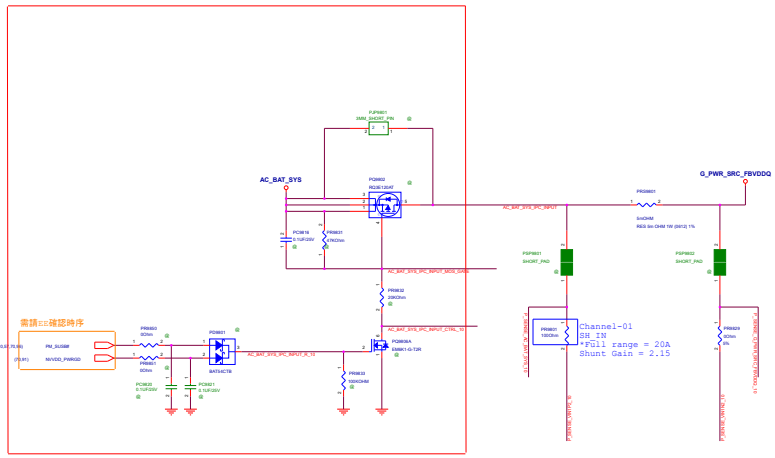
+NVVDD [For DGPU]

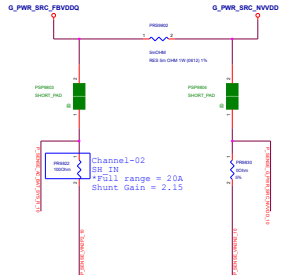


<Core Design>

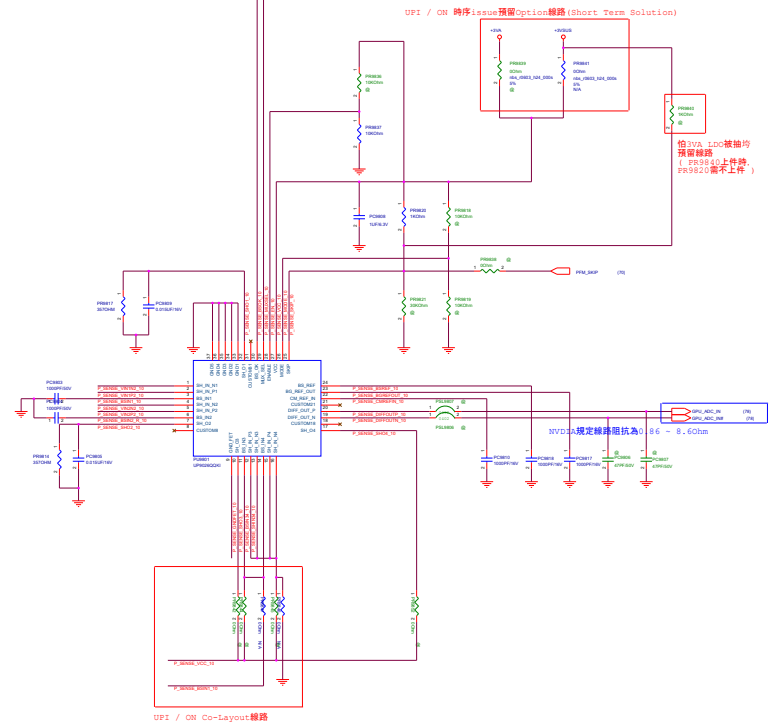
ASUS	Project Name: G711GW	Rev: R1.0
Title : PW_+NVVDD (2)		
Size: A0	Dept.: NB Power team	Engineer: Neil
Date: Monday, April 29, 2019	Sheet 92	of 104

UPI / ON 時序issue預留Option線路(Short Term Solution)
SS : 103us ~ 275us
OFF : 8.1ms ~ 12.4ms

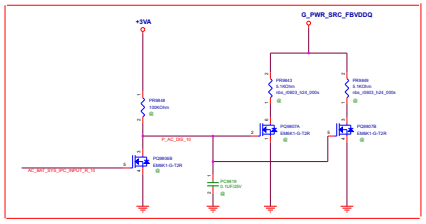




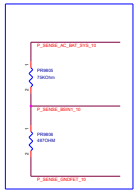
請和EE確認EE端是否有畫對應線路, pull high



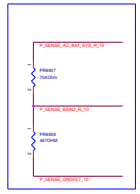
AC_BAT_SYS Discharge線路
T-DisCharge : 0.626s(Worst case 10 Phase)



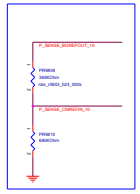
Channel-01
BS_IN
*Full range = 19V
Bus Gain = 6.4514m



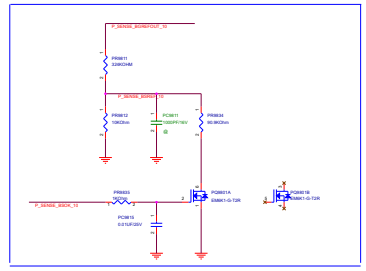
Channel-02
BS_IN
*Full range = 19V
Bus Gain = 6.4514m



CM REF IN
*0.85V(實際0.8459V)



BS REF
*6.0331V、5.4514V(此值需小於19V、BAT電壓)



N18E

150W+

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	100Ω(10G2121000014010)	
PR9817	127Ω (10G2121270014010)	169Ω (10G2121690014010)
PR9822	100Ω(10G2121000014010)	
PR9814	127Ω (10G2121270014010)	169Ω (10G2121690014010)
PR9805	75kΩ(10G2127502140l0)	
PR9806	487Ω (10G2124870140l0)	649Ω (10G2126490140l0)
PR9807	75kΩ(10G2127502140l0)	
PR9808	487Ω (10G2124870140l0)	649Ω (10G2126490140l0)
PR9811	324kΩ (10G2123243140l0)	243kΩ (10G2122433140l0)
PR9812	10kΩ(10G2121002140l0)	
PR9834	90.9kΩ(10G2129092140l0)	

115W ~ 130W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9817	143Ω (10G2121430140l0)	191Ω (10G2121910140l0)
PR9814	143Ω (10G2121430140l0)	191Ω (10G2121910140l0)

100W ~ 110W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9817	165Ω (10G2121650140l0)	221Ω (10G2122210140l0)
PR9822		
PR9814	165Ω (10G2121650140l0)	221Ω (10G2122210140l0)

75W ~ 90W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9817	215Ω (10102-00571000)	287Ω (10G2122870140l0)
PR9822		
PR9814	215Ω (10102-00571000)	287Ω (10G2122870140l0)

75W-

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9817	357Ω (10G2123570140l0)	475Ω (10G2124750140l0)
PR9822		
PR9814	357Ω (10G2123570140l0)	475Ω (10G2124750140l0)

N18P

75W-

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	100Ω(10G2121000014010)	
PR9817	357Ω (10G2123570140l0)	475Ω (10G2124750140l0)
PR9822	100Ω(10G2121000014010)	
PR9814	357Ω (10G2123570140l0)	475Ω (10G2124750140l0)
PR9805	75kΩ(10G2127502140l0)	
PR9806	487Ω (10G2124870140l0)	649Ω (10G2126490140l0)
PR9807	75kΩ(10G2127502140l0)	
PR9808	487Ω (10G2124870140l0)	649Ω (10G2126490140l0)
PR9811	324kΩ (10G2123243140l0)	243kΩ (10G2122433140l0)
PR9812	10kΩ(10G2121002140l0)	
PR9834	90.9kΩ(10G2129092140l0)	

150w+

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	200Ω(10G2122000014010)	
PR9817	127Ω (10G2121270140l0)	
PR9822	200Ω(10G2122000014010)	
PR9814	127Ω (10G2121270140l0)	
PR9805	33kΩ (10G2123302140l0)	
PR9806	431Ω (10102-00581000)	
PR9807	33kΩ (10G2123302140l0)	
PR9808	431Ω (10102-00581000)	
PR9811	324kΩ (10G2123243140l0)	
PR9812	10kΩ(10G2121002140l0)	
PR9834	90.9kΩ(10G2129092140l0)	

115W ~ 130W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	200Ω(10G2122000014010)	
PR9817	143Ω (10G2121430140l0)	
PR9822	200Ω(10G2122000014010)	
PR9814	143Ω (10G2121430140l0)	
PR9805	33kΩ (10G2123302140l0)	
PR9806	431Ω (10102-00581000)	
PR9807	33kΩ (10G2123302140l0)	
PR9808	431Ω (10102-00581000)	
PR9811	324kΩ (10G2123243140l0)	
PR9812	10kΩ(10G2121002140l0)	
PR9834	90.9kΩ(10G2129092140l0)	

75W ~ 90W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	200Ω(10G2122000014010)	
PR9817	215Ω (10102-00571000)	
PR9822	200Ω(10G2122000014010)	
PR9814	215Ω (10102-00571000)	
PR9805	33kΩ (10G2123302140l0)	
PR9806	431Ω (10102-00581000)	
PR9807	33kΩ (10G2123302140l0)	
PR9808	431Ω (10102-00581000)	
PR9811	324kΩ (10G2123243140l0)	
PR9812	10kΩ(10G2121002140l0)	
PR9834	90.9kΩ(10G2129092140l0)	

GM531GX R1.0 SKU Table

			CPU	Power	DIMM	VRAM			
Option	PCB	SKU							
60NB0H10-MB1030	R1.0	GM531GX SKU1	/I7-7700HQ	/230W	TBD	VBG_Micron			
60NB0H10-MB2000	R1.0	GM531GX SKU2	/I5-7300HQ	/230W	TBD	VBG_Samsung			

ASUSTeK COMPUTER	Title :	GM531GX SKU Table_R1.0		
	Engineer:	EE		
Size	Project Name			Rev
C	GX502GX			1.0
Date: Monday, April 09, 2018	Sheet	103	of	104

9. Card Reader: AU6435--02G630002400 (Page42)

10. USB Charger IC: (Page52) Silego SLG55584AVTR -- 06016-00040000
MAXIM MAX14566AEETA+ -- 06G016196011

11. USB3.0 Repeater IC:(Page67)
Parade : PS8710B -- 06053-00200000
Maxim : MAX14972CTG+ -- 06053-00030000

13. Audio Codec : 02043-00130000 (663-VA4)