Compal Confidential

Lotus M/B Schematics Document

14": Elise; 15.6" Exige

Intel Ivy Bridge ULV Processor with DDRIII + Panther Point

Date : 2011/10/27
Version 0.1

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.			
Title: Block Diagrams			
Size: Custom	Document Number: LA-8551P		Rev: 0.1
Date: Friday, March 02, 2012	Sheet 1 of 55		

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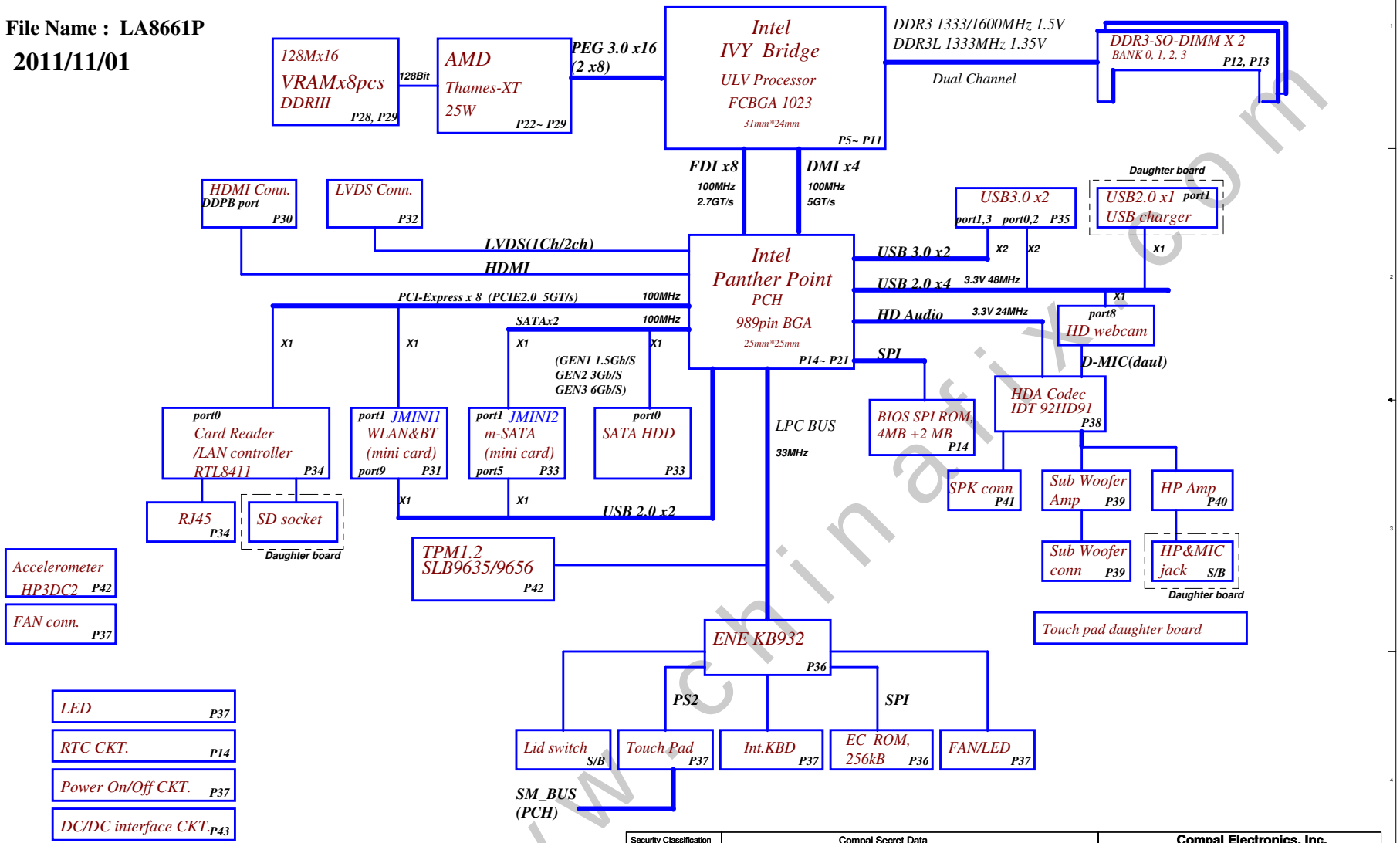
Model Name : Lotus

File Name : LA8661P

2011/11/01



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Compal Electronics, Inc.

Title: Block Diagrams

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QAU30/50 (LA-8661P Ver:0.1)

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
		ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VCCP	+V1.05SP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+VCCP	+VCCP (1.05V) power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII (1.35V OR 1.5V)	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW) to 1.8V switched power rail to PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+LAN_IO	+3VALW to +LAN_IO power rail for LAN	ON	ON	ON*
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V_PCH	+5VALW to +5V_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	B+ to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Power Plane	Description	S1	S3	S5
+VGA_CORE	GPU power	PX	OFF	OFF
+3VGS	GPU power	PX	OFF	OFF
+1.8VGS	GPU power	PX	OFF	OFF
+1.5VGS	GPU power	PX	OFF	OFF
+1.0VGS	GPU power	PX	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	
G-sensor	0x50/0x52

PCH SM Bus address

Device	Address
DDR DIMM0	
DDR DIMM1	
Mini Card1	
Mini Card2	
TP module	

EC SM Bus2 address

Device	Address
PCH (Reserve)	

SMBUS Control Table

	SOURCE	BATT	WLAN MIINI1	BATT Charger	TP	SODIMM	EC_SMB_CK2 EC_SMB_DA2	PCH_SML1CLK PCH_SML1DATA	G-Sensor	GPU	HP AMP
EC_SMB_CK1 EC_SMB_DA1	KB930	V		V					V		
EC_SMB_CK2 EC_SMB_DA2	KB930							V		V	V
PCH_SMBCLK PCH_SMBDATA	PCH		@		V	V					
PCH_SML0CLK PCH_SML0DATA	PCH										
PCH_SML1CLK PCH_SML1DATA	PCH						V				

CLKOUT	DESTINATION
PCI0	PCH_LPBACK
PCI1	PCI_LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	SATA, JHDD1
SATA1	m-SATA,JMINI2
SATA2	None
SATA3	None
SATA4	None
SATA5	None

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB2.0 (left Side)
		1	USB2.0 (right Side)
	UHCI1	2	USB2.0 (left Side)
		3	None
	UHCI2	4	None
		5	None
	UHCI3	6	None
		7	None
EHCI2	UHCI4	8	Camera
		9	Mini Card(WLAN& BT)
	UHCI5	10	None
		11	None
	UHCI6	12	None
		13	None

USB 3.0	Port	2 External USB Port
	1	USB3.0 (left Side)
	2	None
	3	USB3.0 (left Side)
	4	None

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	PCIE LAN CARD READER	CLKOUTFLEX0	None
			CLKOUTFLEX1	None
	CLKOUT_PCIE1	mini WLAN	CLKOUTFLEX2	None
	CLKOUT_PCIE2	None	CLKOUTFLEX3	DGPU_PRSNT#
	CLKOUT_PCIE3	None		
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

BY SKU		
TPM	9635@	9656@
CPU	CPUUMA1@ CPUUMA2@ CPUDIS@	
VRAM	X76@	H2G@
	M2G@	S2G@

Option	@	CONN@	USB30@	PX@	UMA@	DIS@	THA@
UMA	X	X	V	X	V	X	X
DIS	X	X	V	V	X	V	V

Symbol Note :
: means Digital Ground
: means Analog Ground

Project ID	30UMA@	30DIS@	50UMA@	50DIS@

PCB	LA-8661P	LA-8662P
	PX@	UMA@

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.			
Title	Notes List		
Size C	Document Number LA-8661P		Rev 0.1
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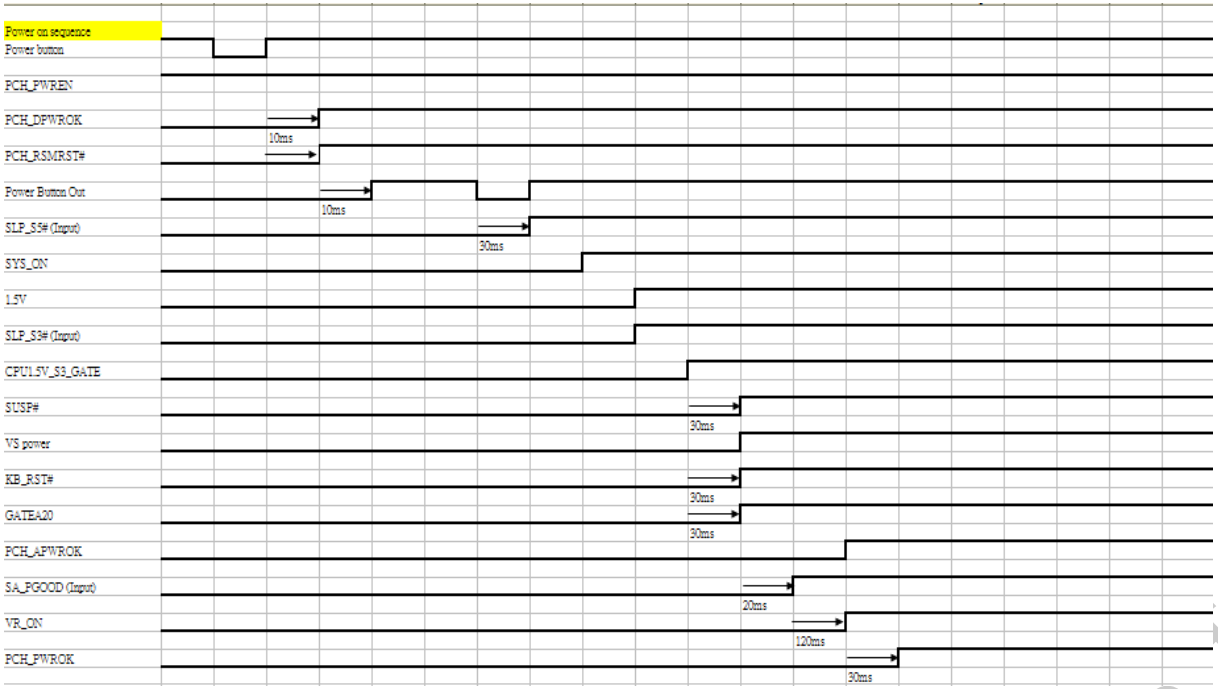

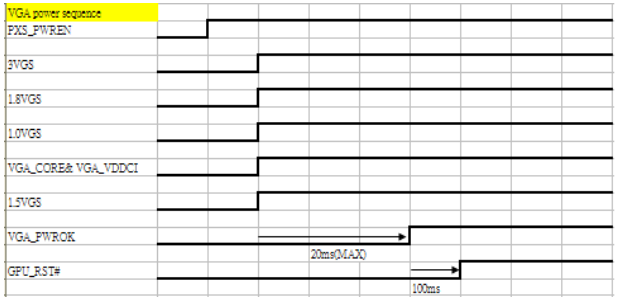

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Title	***PROCESSOR(1/7) DMI,FDI,PEG***		
Size B	Document Number		Rev 0.1
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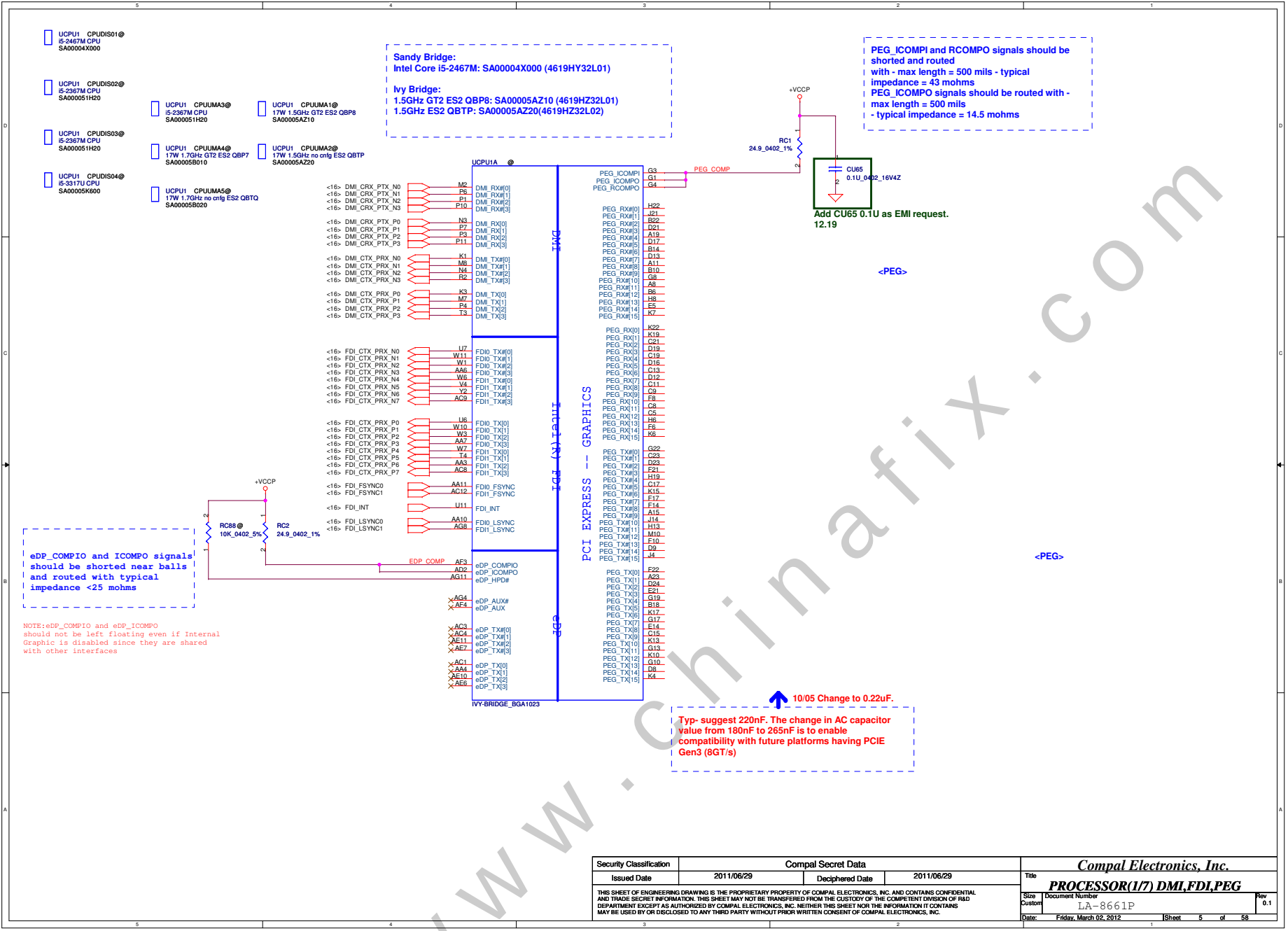

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Compal Electronics, Inc.

Title: PROCESSOR(1/7) DMI,FDI,PEG

Size	Document Number	Rev
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Buffered reset to CPU

Reset# signal is driven by the PCH to multiple agents on the platform.
PCH Reset# output DC levels are 0-V and 3.3 V.
processor Reset input DC levels are 0V and 1.0 V.
Processor high-voltage level is lower than PCH high voltage level, therefore a voltage level shifter is required on the Reset# signal.
In order for Reset# to meet the signal quality requirement at the input to the processor OD buffer must be placed on the motherboard between the PCH and the processor.

Requires a series resistor of 43±5% between processor and PCH. It also a needs an Rtt of 75±5% to VCCP after the OD buffer and before the series resistor.

Processor Pullups

SI2 change to 0201
12.19

SI2 change to 0201
12.19

SI2 change to 0201
12.19

SI2 change to 0201
12.19

SI2 change to 0201
12.19

SI2 change to 0201
12.19

SI2 change to 0201
12.19

UNCOREPWRGOOD:非CORE外的電OK

SM_DRAMPWROK:DRAM power ok

2011.10.18 delete all reserved XDP conponent.
Just reserve test point for XDP.

DDR3 Compensation Signals

PU/PD for JTAG signals

2011.10.18 delete all reserved XDP conponent.
Just reserve test point for XDP.

11.06 Change to +3V_PCH

Part Number = SA00003Y000

6/27 Add ESD solution

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PROCESSOR(2/7) PM,XDP,CLK

Size	Document Number	Rev
C	LA-8041P	0.1

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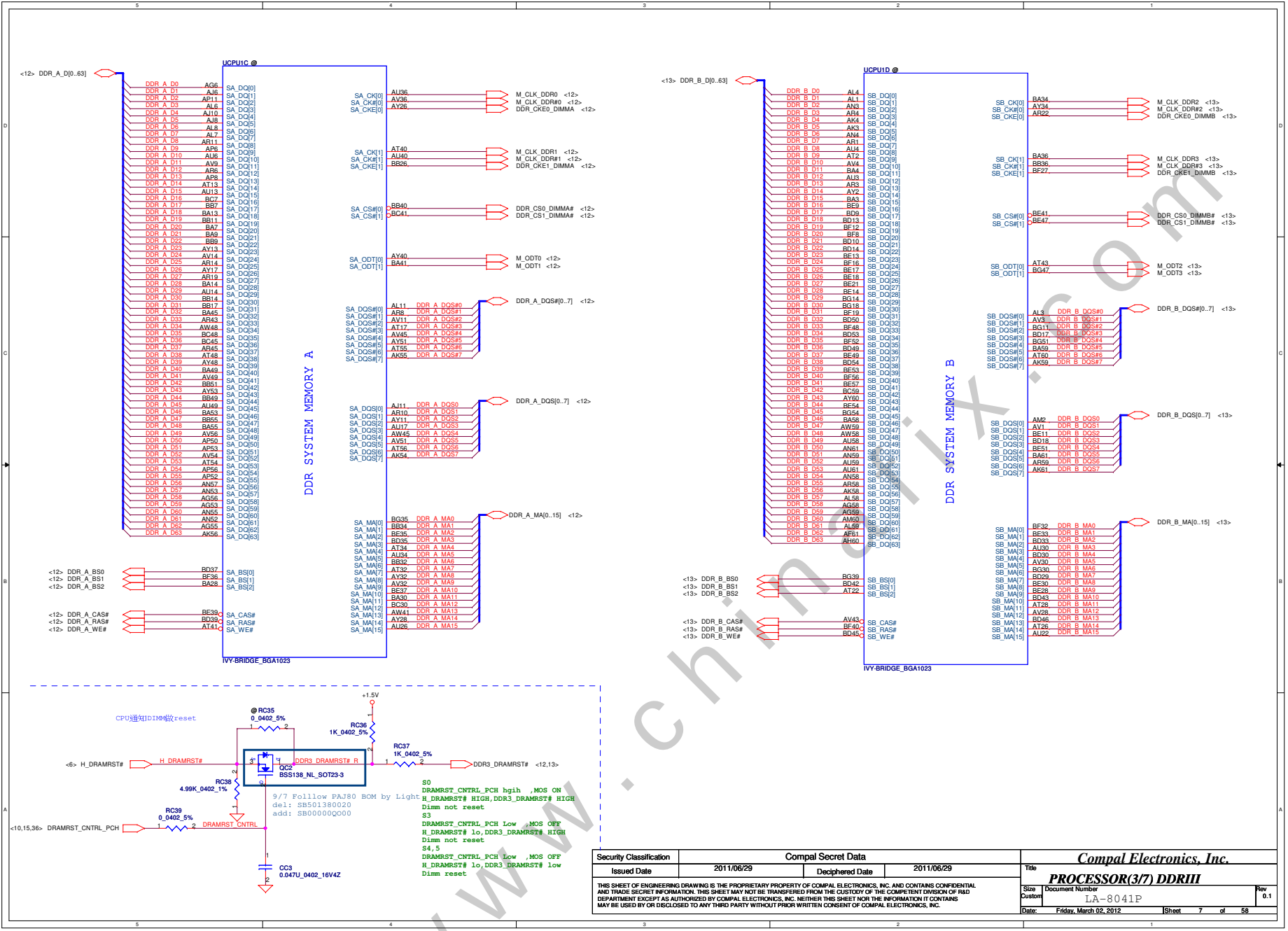

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Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

Size	Document Number	Rev
Custom	LA-8041P	0.1

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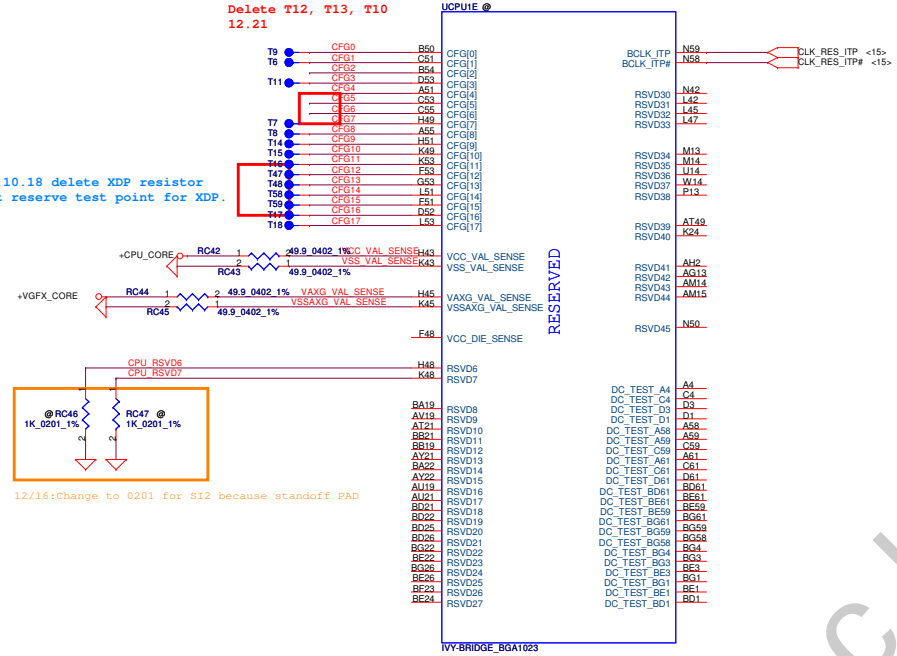
CFG Straps for Processor

PEG bus is reversed, need to PD.
11.01

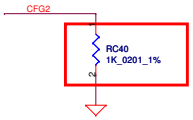
Change to part G.

Delete T12, T13, T10
12.21

2011.10.18 delete XDP resistor
just reserve test point for XDP.

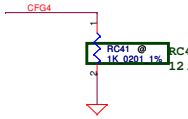


12/16:Change to 0201 for SI2 because standoff PAD



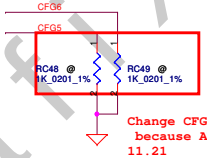
RC40 SI2 change to 0201
12.19

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



RC41 SI2 change to 0201
12.19

Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

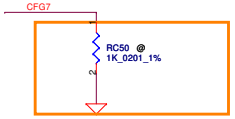


RC48, RC49 SI2 change to 0201
12.19

Change CFG[6:5] to 11 = 1 x 16 PCI Express
because AMD driver can't install issue
11.21

PCIE Port Bifurcation Straps	
CFG[6:5]	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express *

12/16:Change to 0201 for SI2 because standoff PAD



PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size	Document Number	Rev
Custom	LA-8661P	0.1

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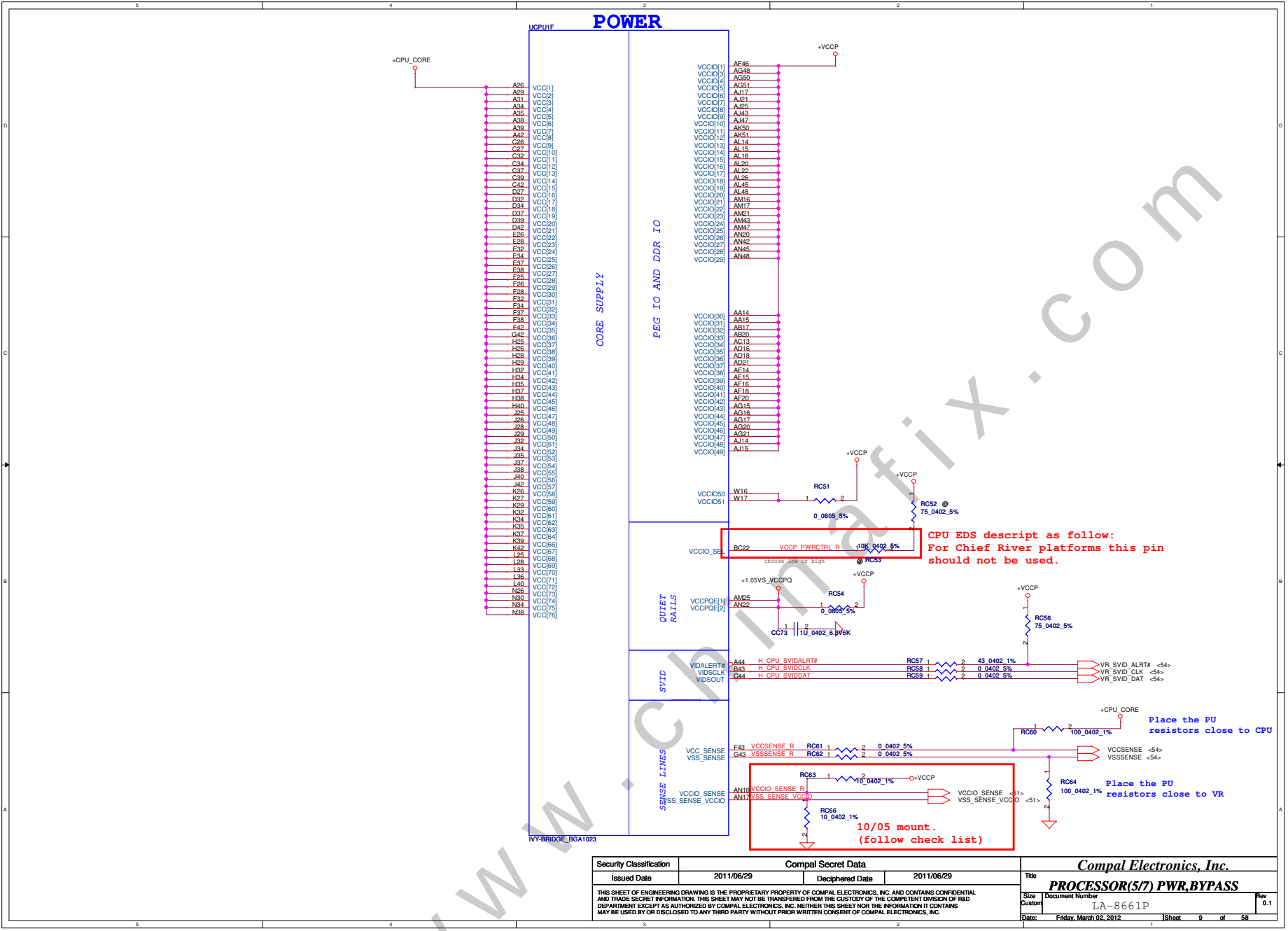

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Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

Size	Document Number	Rev
Custom	LA-8661P	0.1

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POWER

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

+V_SM_VREF should have 20 mil trace width

10/03 add +V_DDR_REFB

Check with Power Team
CC100 (330UF) can be taken off.
10.31

QC4 Change to SA0000JA00 for small package 1016

+1.5V_CPU_VDDQ Source

Follow DG 0.71 page 6

For Chief River only

M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

10/03 add +V_DDR_REFB

Delete CC25 330U cap 10.19
(after check with power)

SI# BOM Change CC118 0.1u 25V form 0.1u 16V

UCPU1G

GRAPHICS | VREF | DDR3 - 1.5V RAILS | SENSE LINES | QUIET RAILS | 1.8V RAIL | SENSE LINES | SA RAIL | VCCSA_VID lines

IVY-BRIDGE_BGA1023

VID[0]	VID[1]		2011	2012
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: PROCESSOR(6/7) PWR

Size	Document Number	Rev
Custom	LA-8661P	0.1

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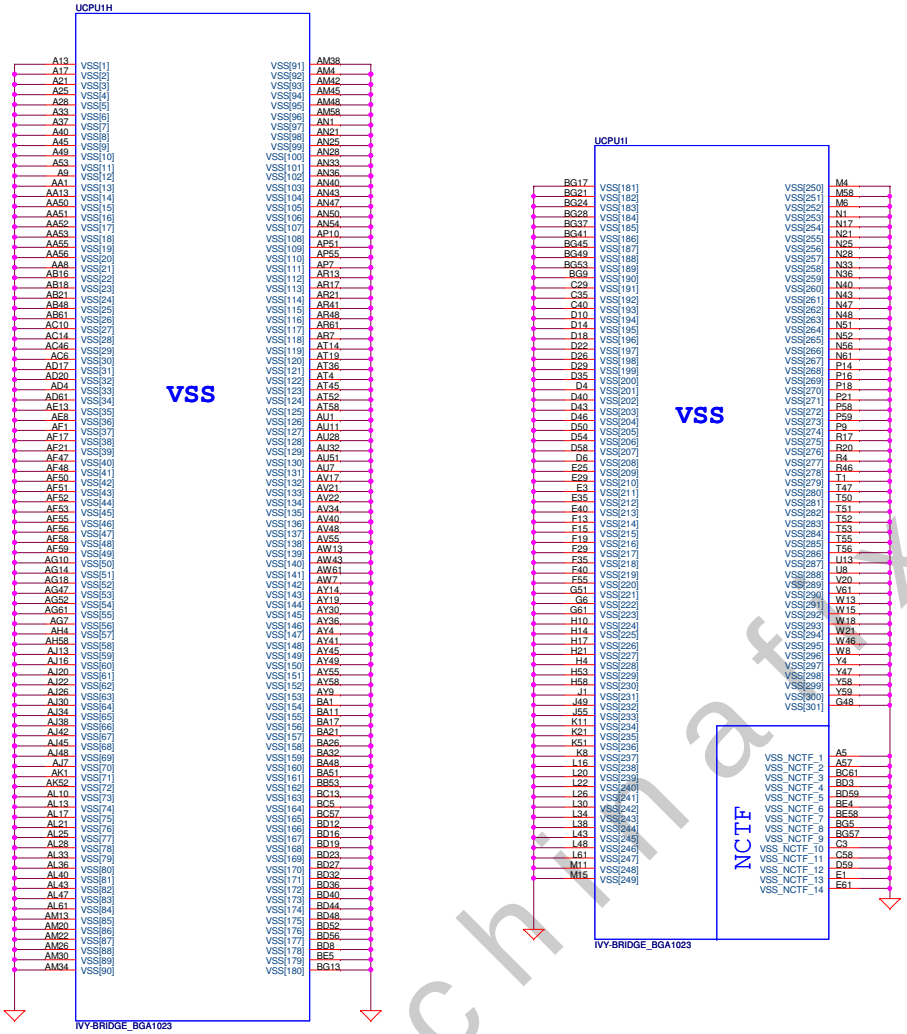

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Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

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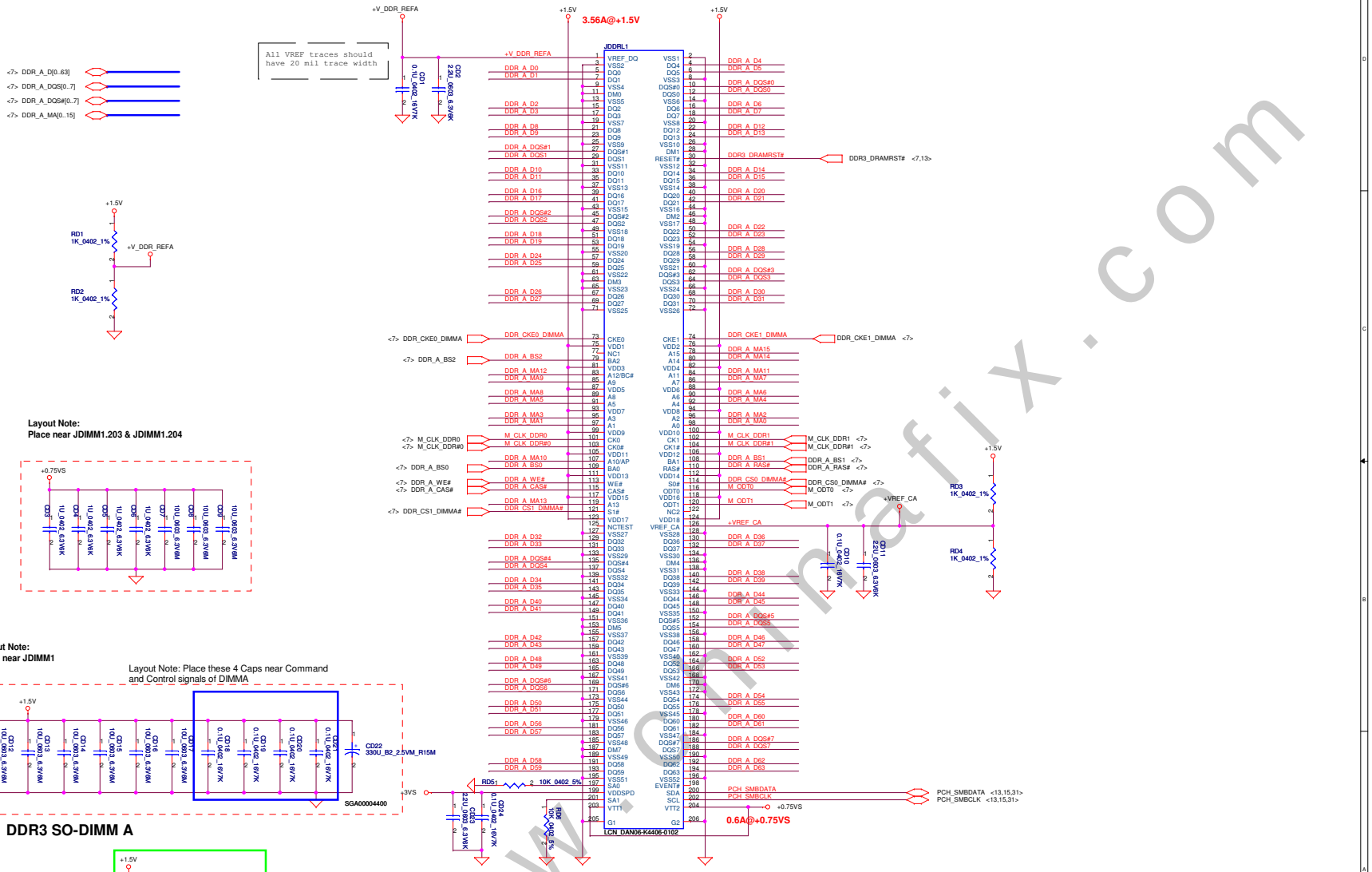
DDR3 SO-DIMM A



DDR3 SO-DIMM A

SI# 8/16 Reserve 4 pcs 0.1uF for EMI noise issue

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Issued Date	2011/06/29	Deciphered Date	2011/06/29

Title	DDRIII DIMM		
Size: C	Document Number: LA-8661P		Rev: 0.1
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DDR3 SO-DIMM B

10/03 change to +V_DDR_REFB

3.56A@+1.5V

All VREF traces should have 20 mil trace width

Delete DDR_B_DM[0..7]

10/03 change to +V_DDR_REFB

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

10/03 change to +VREF_CB

0.6A@+0.75VS

10/05 change to PH.

Standard
<Address(SA1,SA0):10>

Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title: DDRIII-DDRH

Size	Document Number	Rev
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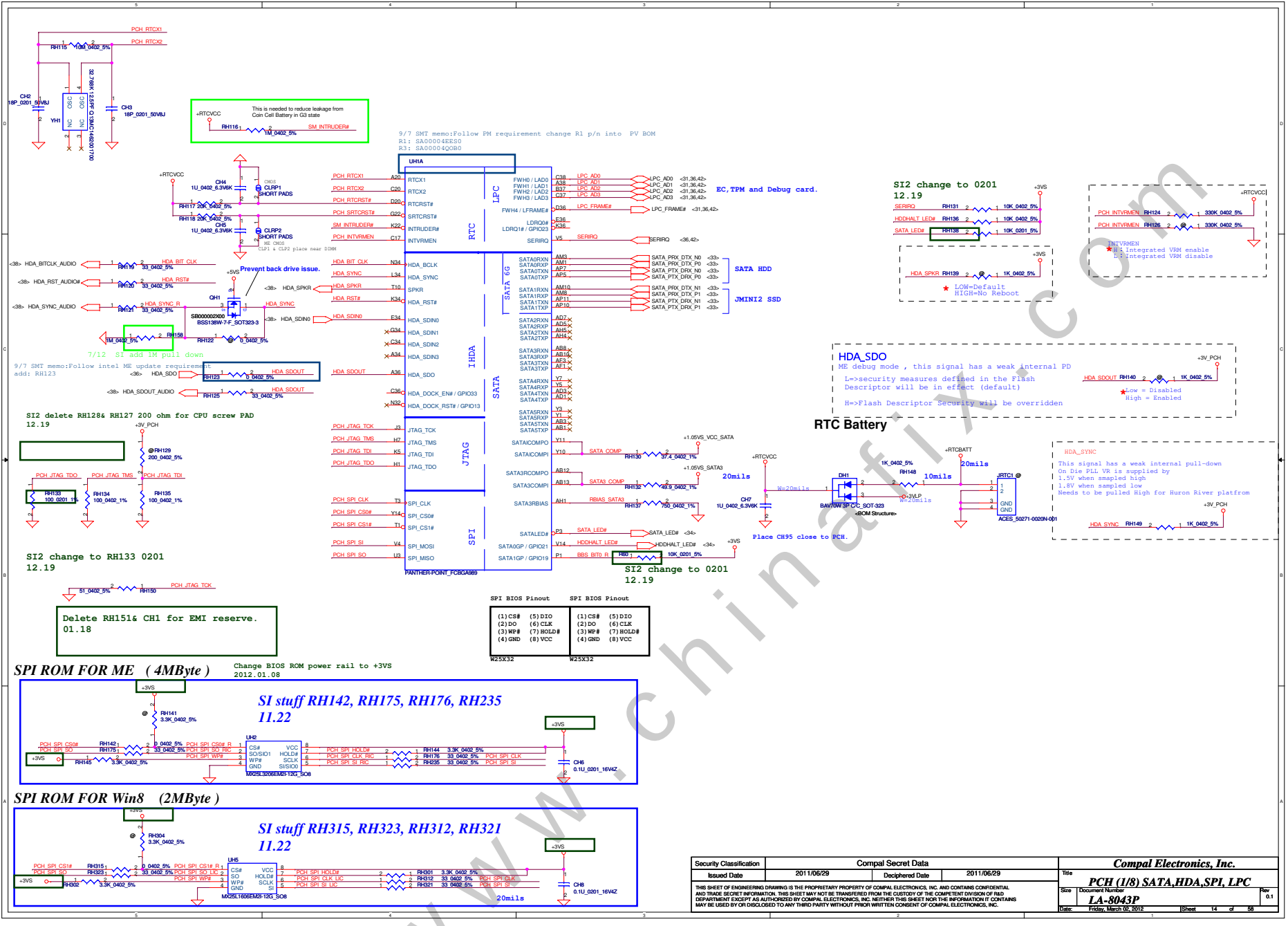

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA,SPI, LPC

Size: | Document Number: LA-8043P | Rev: 0.1

Date: Friday, March 02, 2012 | Sheet 14 of 58

PV# 9/13 change power rail form +3VALW->+3V_PCH

10/03 change to PCIE port1.

PCIE LAN/Card Reader

Mini card WLAN

UH1B

PCI-E*

SMBUS

Controller Link

CLOCKS

FLEX CLOCKS

PANTHER-POINT_FCBGA989

SI2 change to 0201
12.19

PCIE LAN/Card Reader

MiniWLAN

SI2 change to 0201
12.19

SI2 change to 0201
12.19

SI2 change to 0201
12.19

Change WL_OFF# to GPIO45 (pull-high) +3V_PCH
2012.01.04

SI2 YH2 change to SJ10000DJ00
12.19

Reserve for EMI please close to UH1

Reserve for EMI please close to UH1

12/16:Change to 0201 for SI2

If use external CLK gen, please place close to CLK gen else, please place close to PCH

100MHz

100MHz

SI# 8/8 Add SML1CLK/SML1DATA for EC detect Thermal

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Issued Date	2011/06/29	Deciphered Date	2011/06/29

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Title: PCH (2/8) PCIE, SMBUS, CLK

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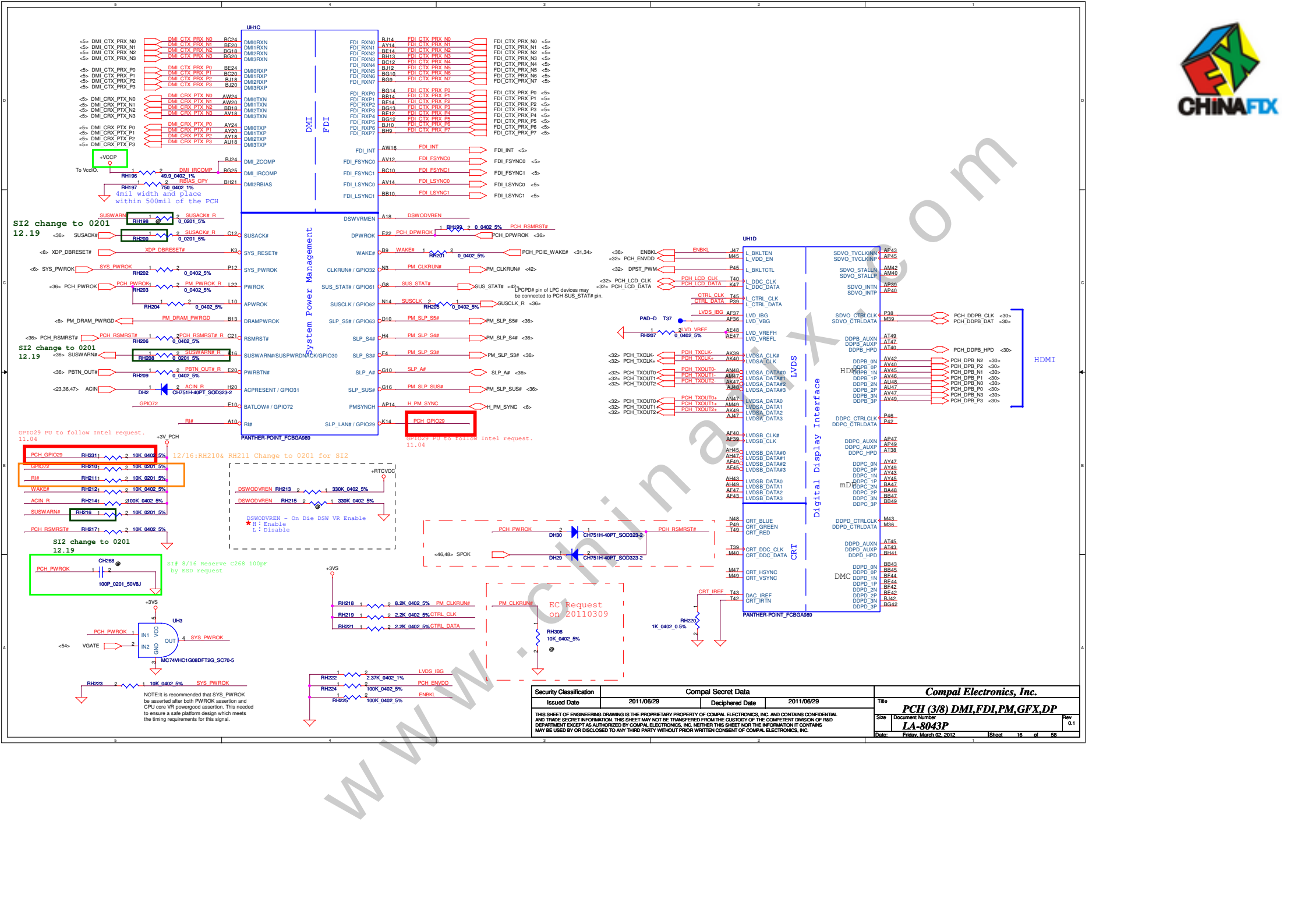

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Title: **PCH (3/8) DMI,FDI,PM,GFX,DP**

Size	Document Number	Rev
	LA-8043P	0.1

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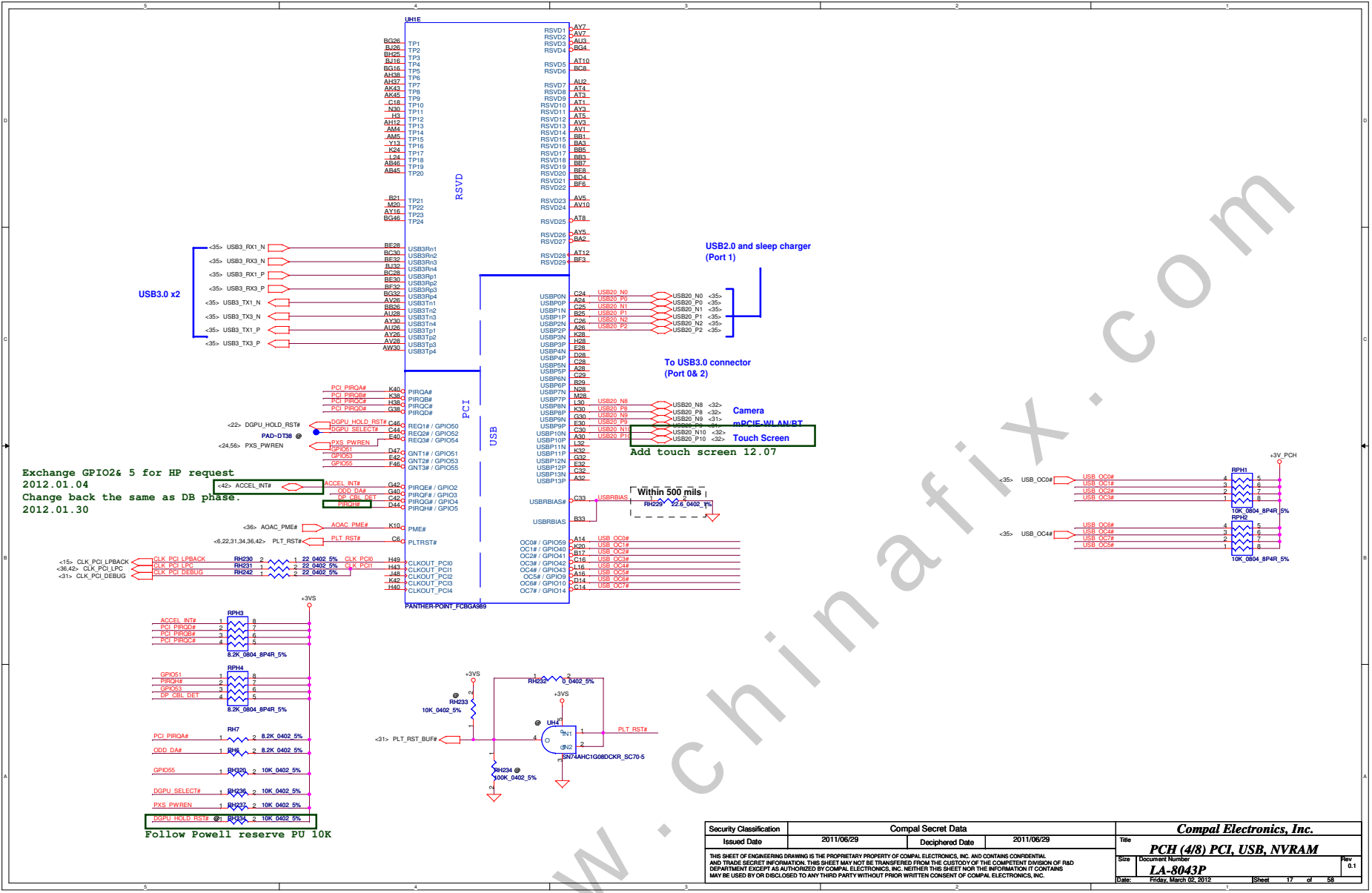

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Title: **PCH (4/8) PCI, USB, NVRAM**

Size	Document Number	Rev
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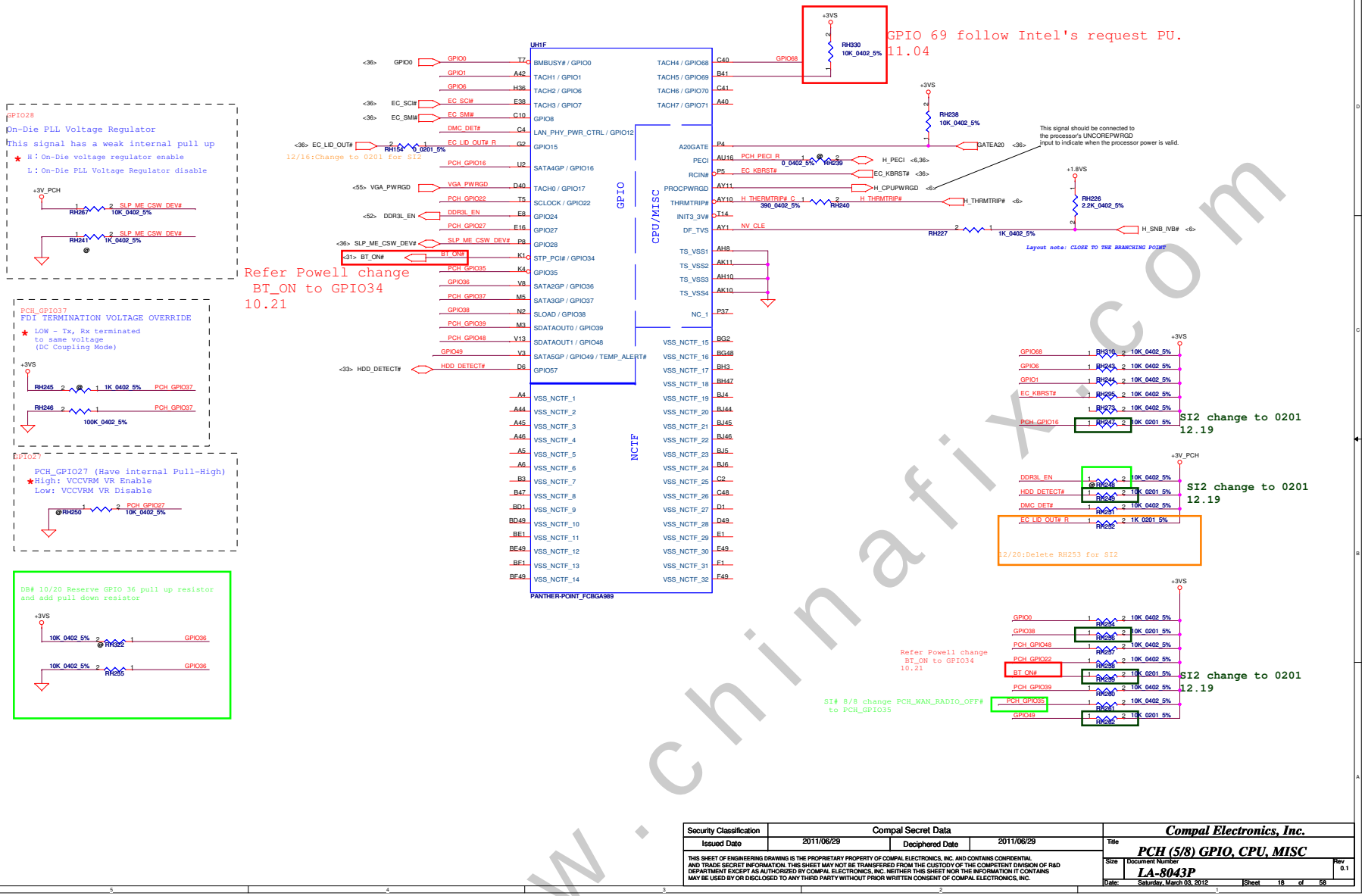

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.	
Title	PCH (5/8) GPIO, CPU, MISC
Size	Document Number: LA-8043P
Rev	0.1
Date:	Saturday, March 03, 2012
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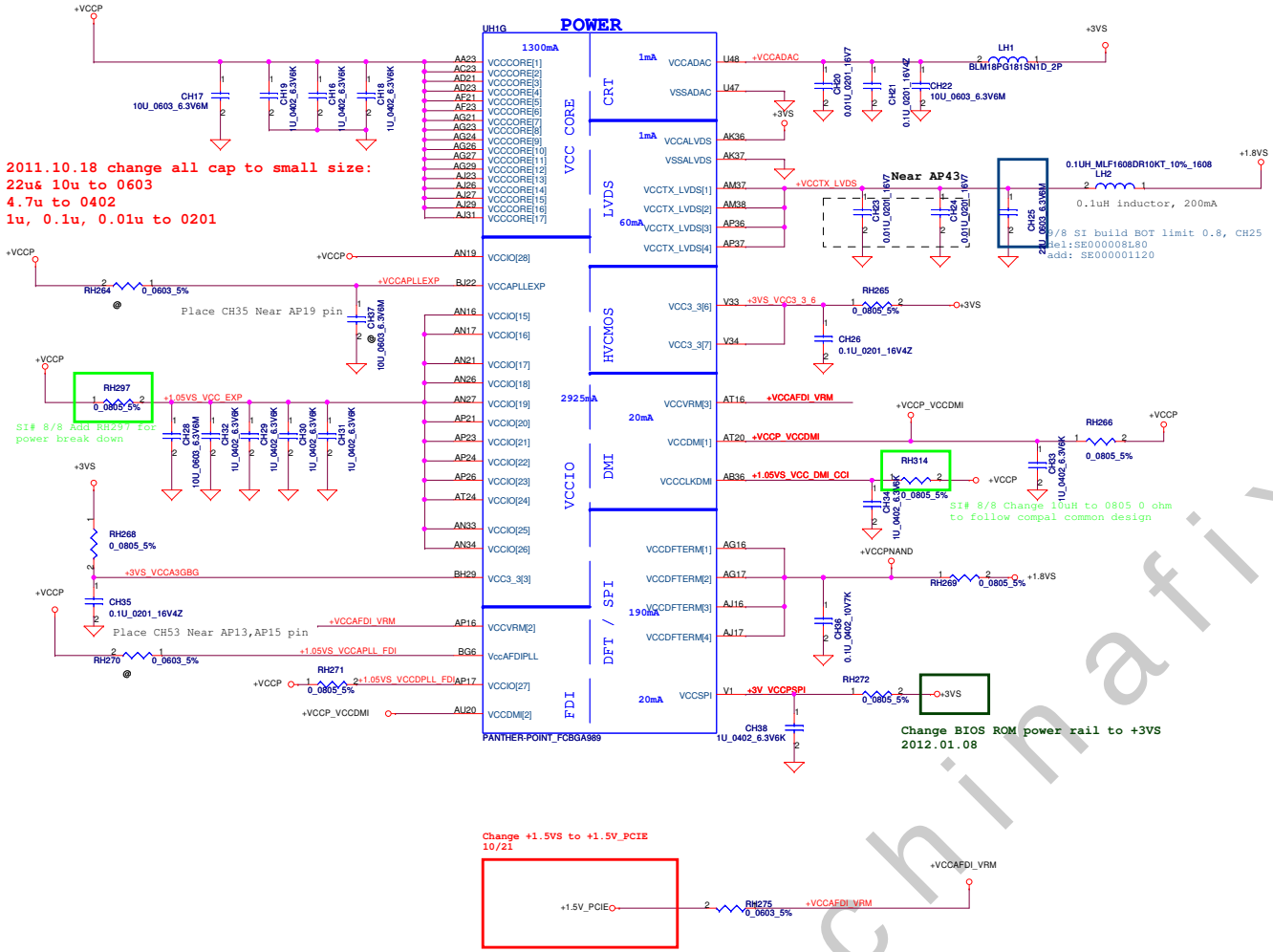


PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

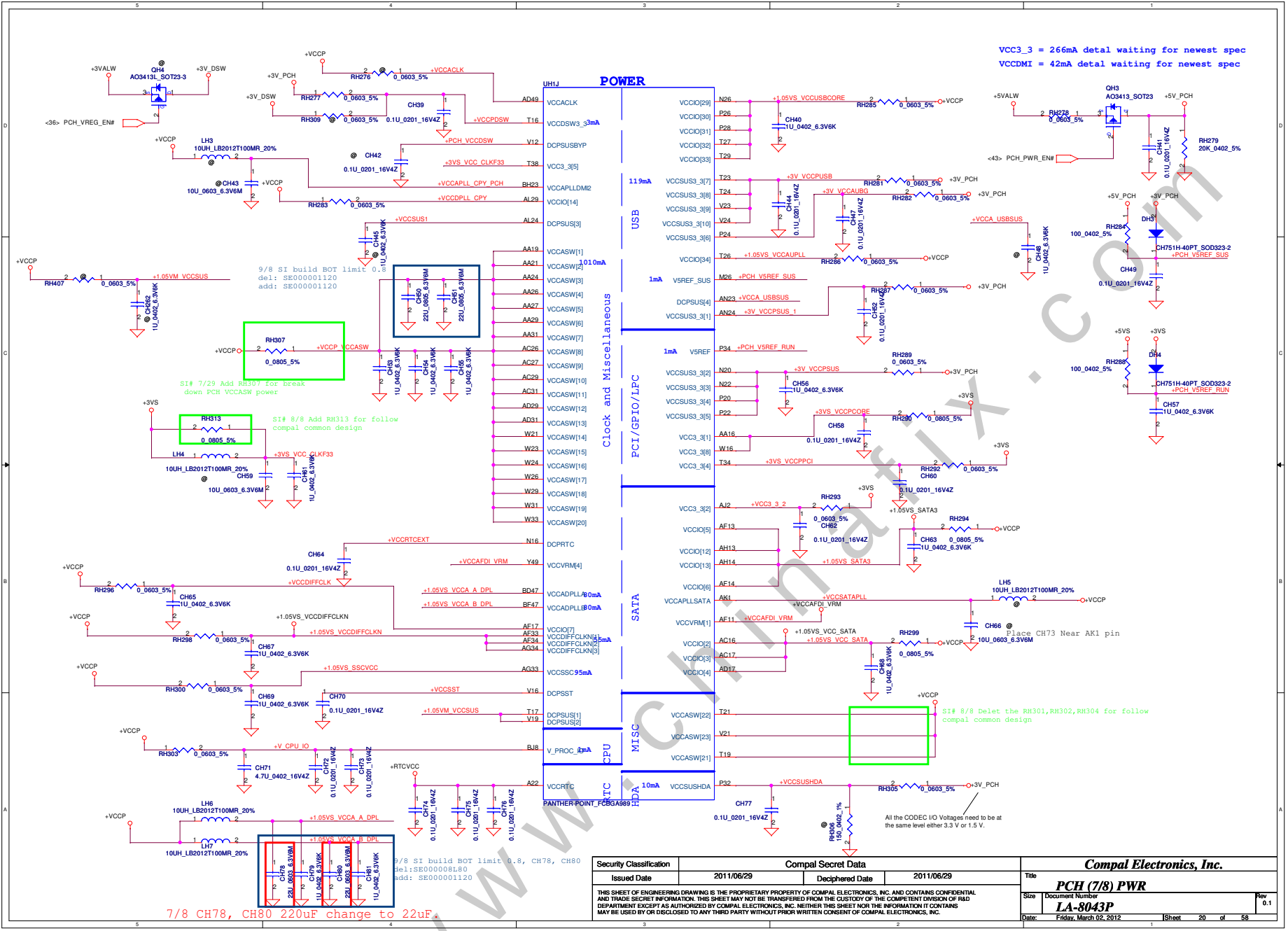
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: **PCH (6/8) PWR**

Size | Document Number: **LA-8043P** | Rev: 0.1

Date: Friday, March 02, 2012 | Sheet 19 of 58

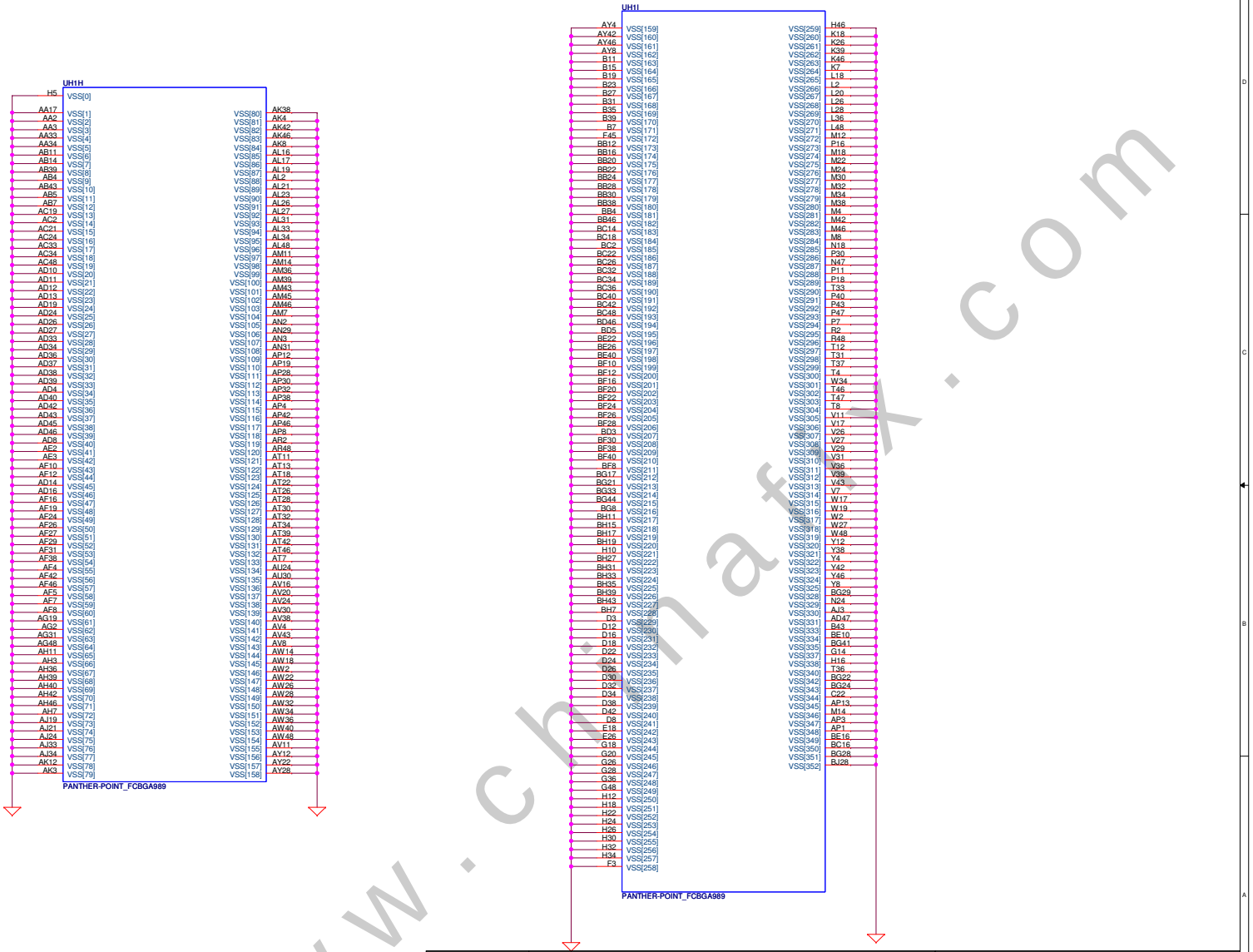


Compal Electronics, Inc.

Title: **PCH (7/8) PWR**

Size: | Document Number: **LA-8043P** | Rev: 0.1

Date: Friday, March 02, 2012 | Sheet 20 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

Size	Document Number	Rev
	LA-8043P	0.1

Date: Friday, March 02, 2012 | Sheet 21 of 58

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_PCIE/LVDS

Size	Document Number	Rev
C	LA7691P	0.1

Date: Friday, March 02, 2012 Sheet 22 of 58

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_Main_MSIC

Size	Document Number	Rev
C	LA7691P	0.1

Date: Friday, March 02, 2012 Sheet 23 of 58

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_BACO POWER

Size	Document Number	Rev
C	LA7691P	0.1

Date: Friday, March 02, 2012 Sheet 24 of 58

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SetmourXT_M2_PWR_GND

Size	Document Number	Rev
C	LA7691P	0.1

Date: Friday, March 02, 2012 Sheet 25 of 58

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_Power

Size	Document Number	Rev
C	LA7691P	0.1

Date: Friday, March 02, 2012 Sheet 26 of 58

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_MEM IF

Size	Document Number	Rev
C	LA7691P	0.1

Date: Friday, March 02, 2012 Sheet 27 of 58

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_VRAM_A

Size	Document Number	Rev
C	LA7691P	0.1

Date: Friday, March 02, 2012 Sheet 28 of 58

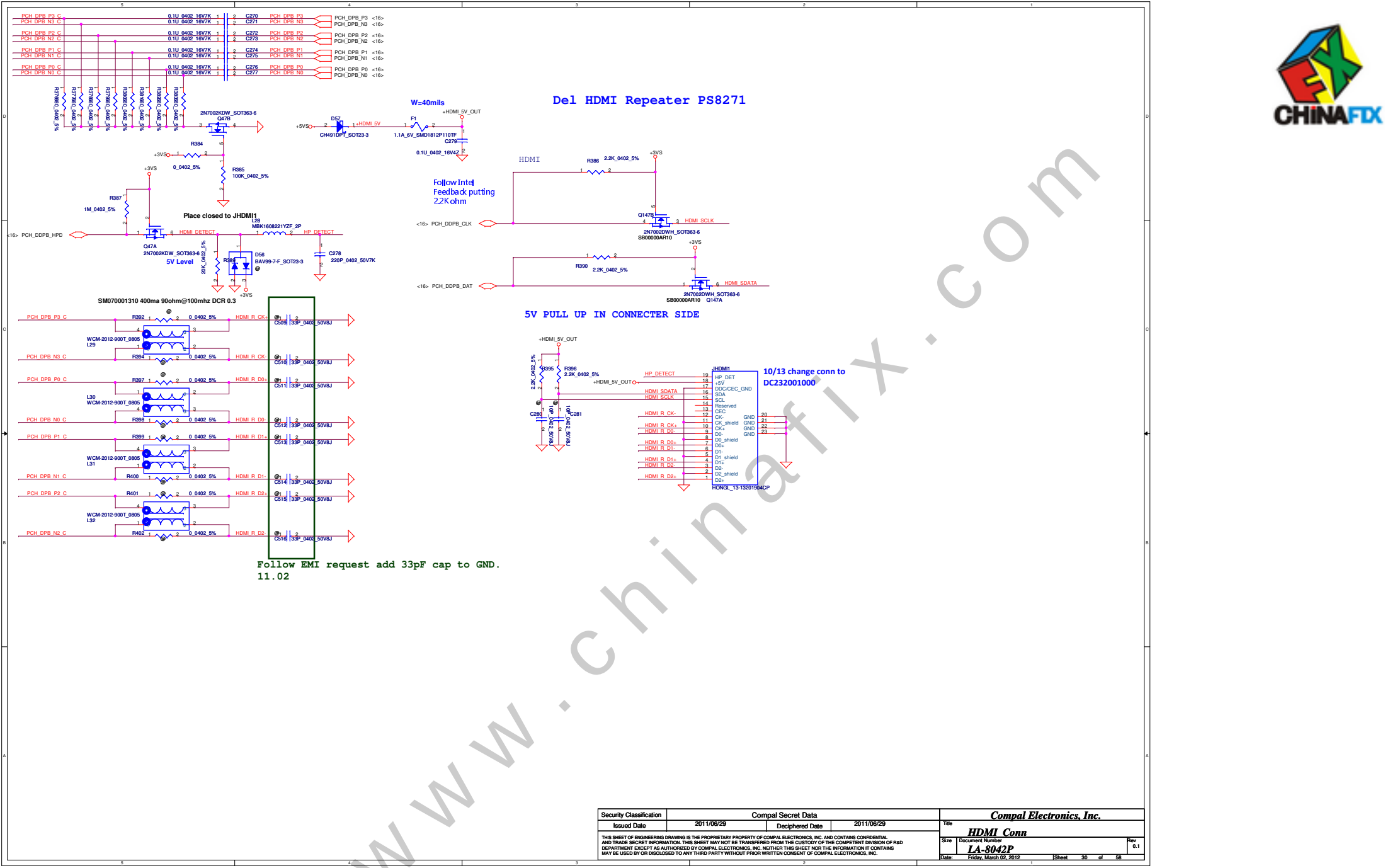
Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_VRAM_B

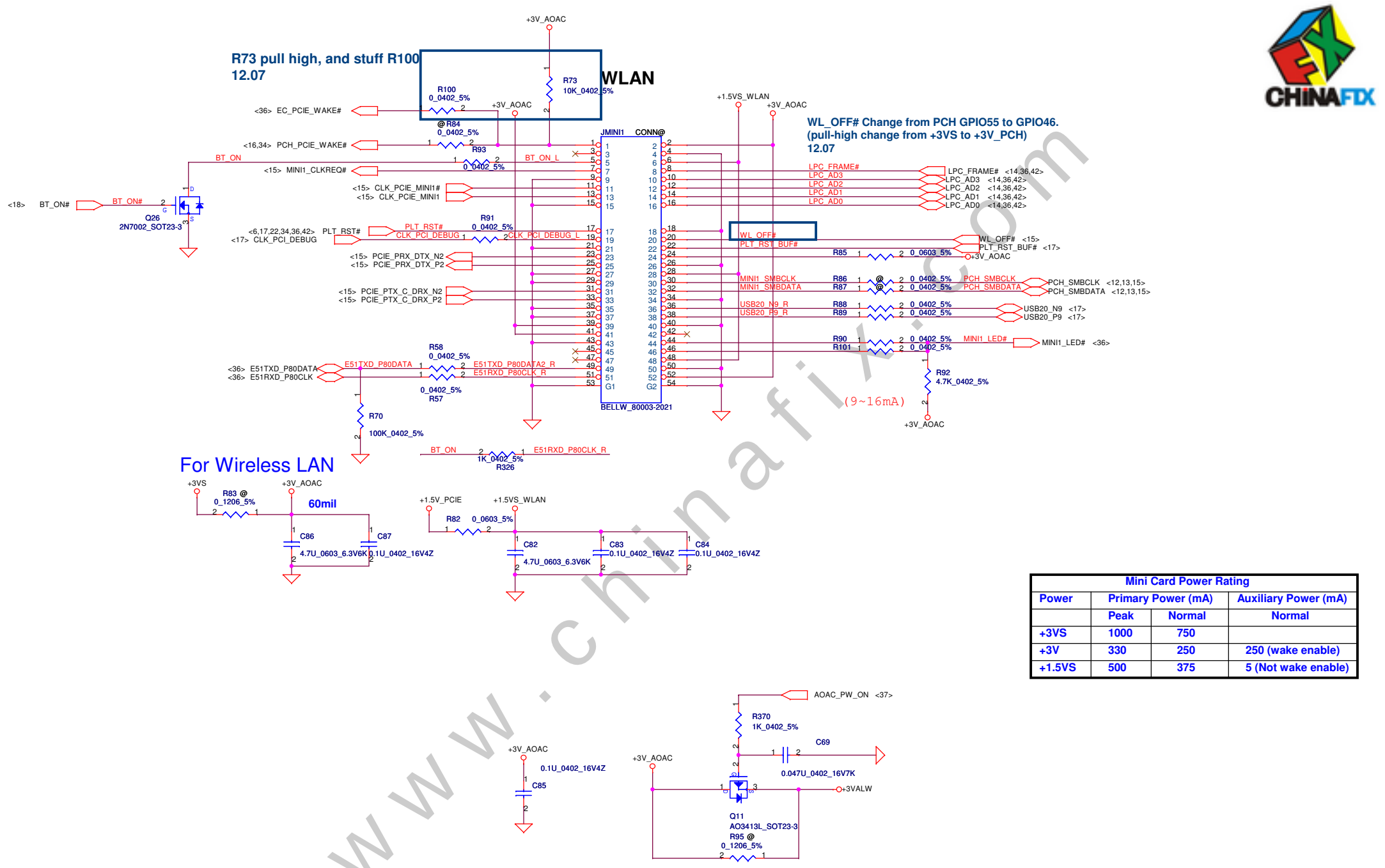
Size	Document Number	Rev
C	LA7691P	0.1

Date: Friday, March 02, 2012 Sheet 29 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

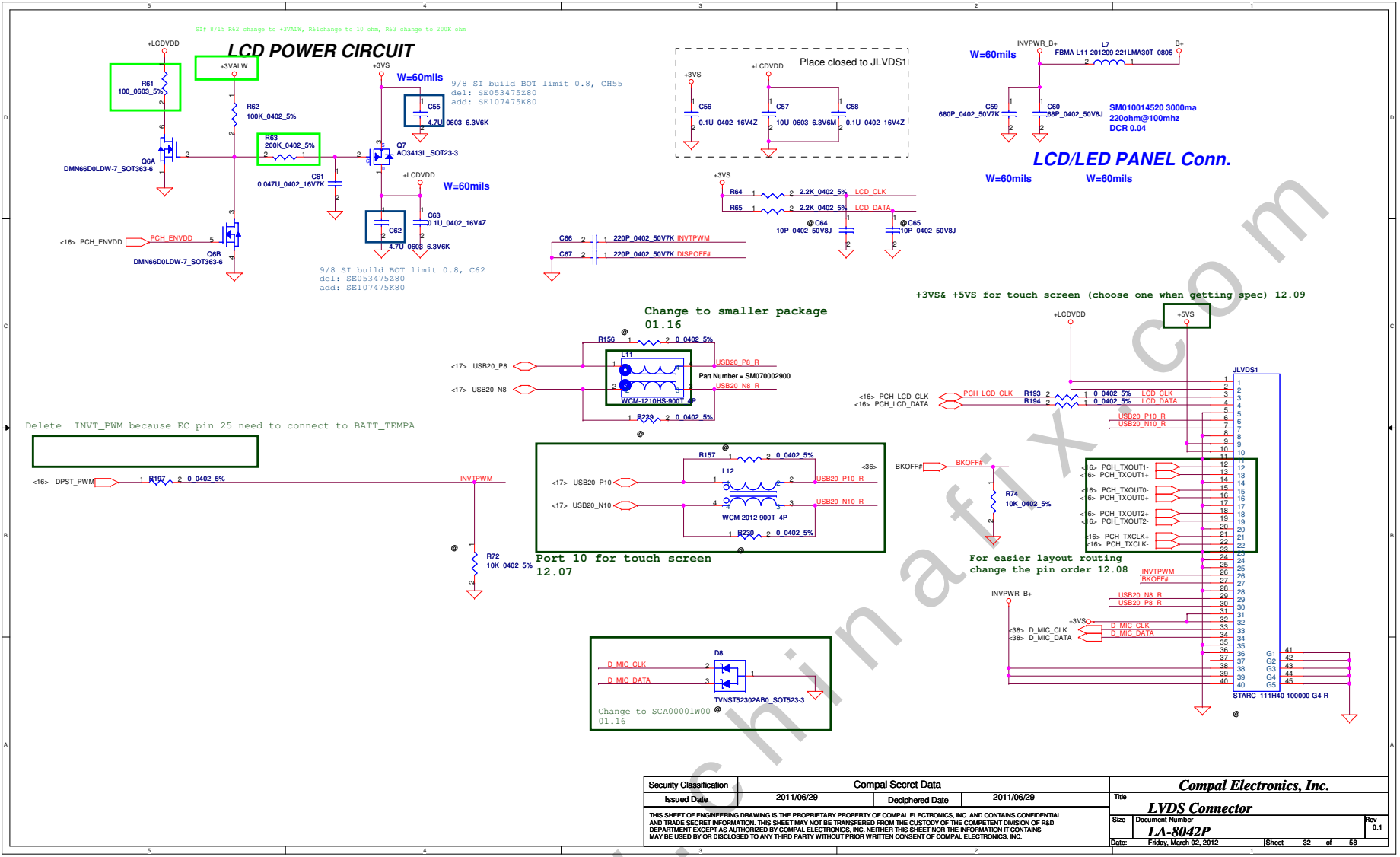
Compal Electronics, Inc.			
Title: HDMI Conn			
Size	Document Number: LA-8042P		Rev: 0.1
Date: Friday, March 02, 2012		Sheet 30 of 58	



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.			
Title	MiniCard & WLan		
Size	Document Number		Rev
	LA-8042P		0.1
Date:	Friday, March 02, 2012	Sheet	31 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

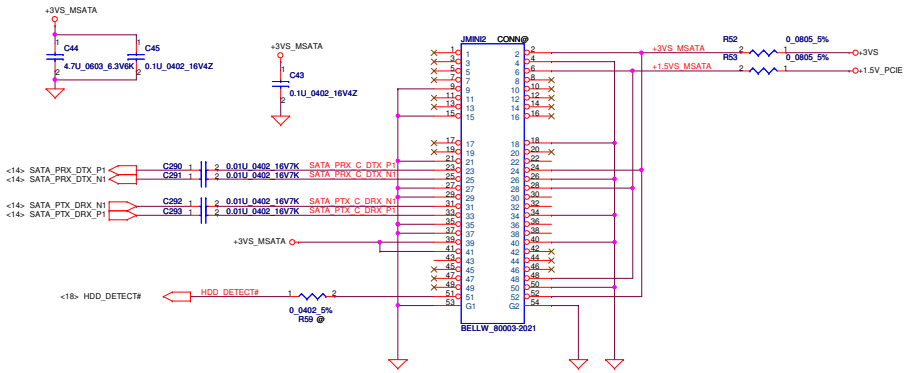
Compal Electronics, Inc.

Title: **LVDS Connector**

Size	Document Number	Rev
	LA-8042P	0.1

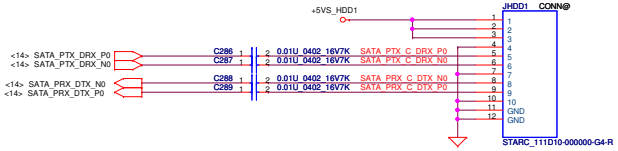
Date: Friday, March 02, 2012 Sheet 32 of 58

mSATA Conn.

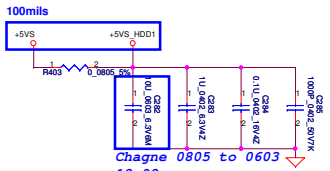


Exchange port 0 & port 1 for SI as customer request
11.30

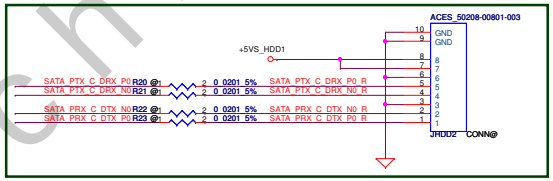
Change footprint to Starconn (PAD is bigger)
11.30



SATA connector



Chagne 0805 to 0603
12.08



Co-layout for wire type connector
01.16
Change connector to ACES_50376
01.31
Change connector to ACES_50208 because current limit issue
02.06

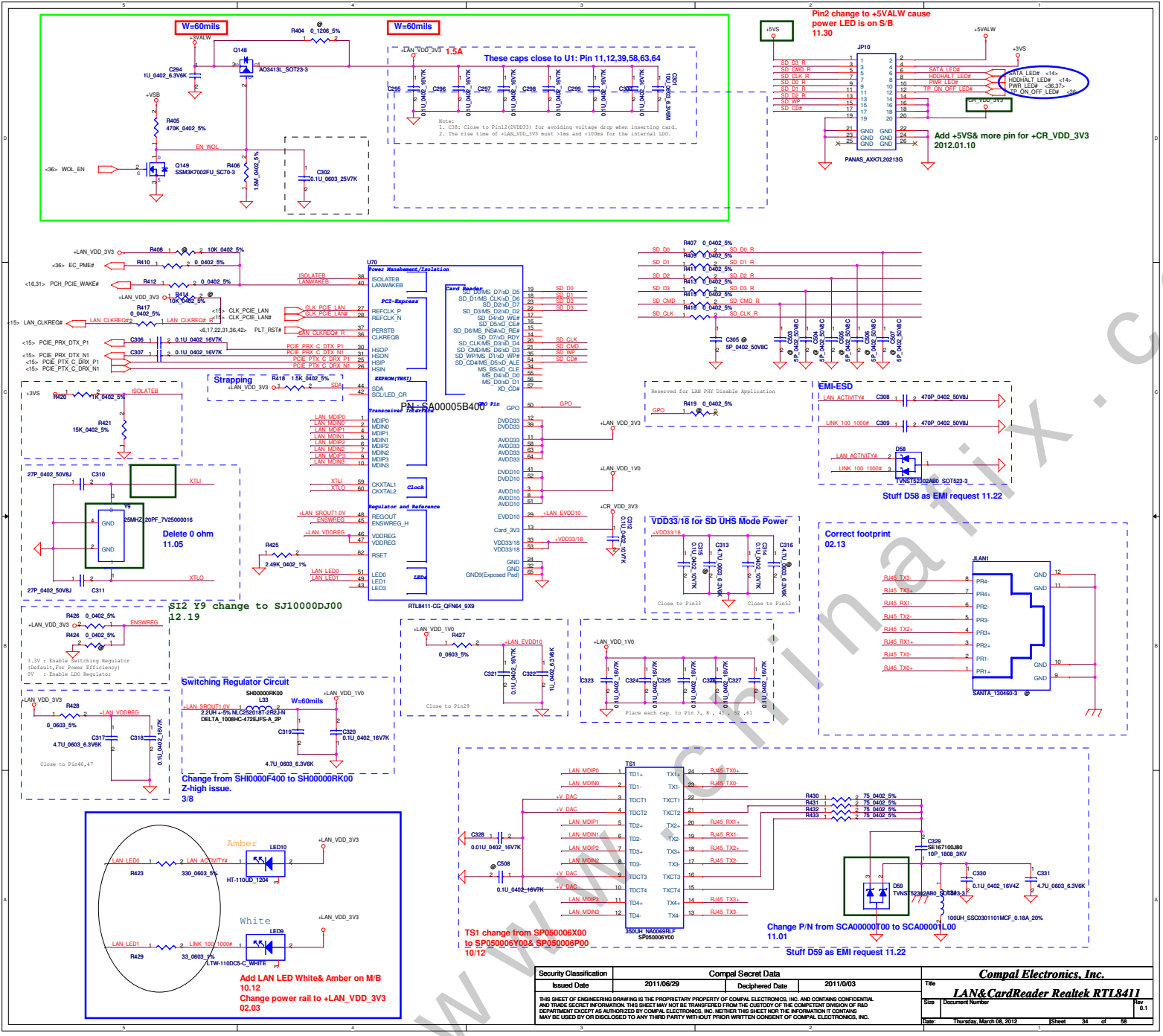
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: mSATA Connector

Size	Document Number	Rev
C	LA-8042P	0.1

Date: Friday, March 02, 2012 Sheet 33 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/0/03

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Compal Electronics, Inc.

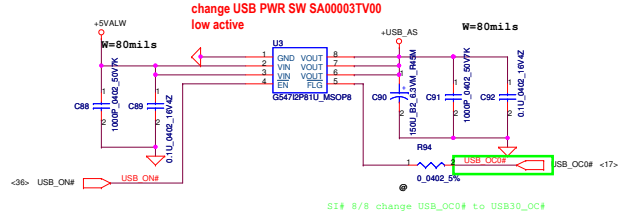
Title: **LAN&CardReader Realtek RTL8411**

Size | Document Number | Rev 0.1

Date: Thursday, March 08, 2012 | Sheet 34 of 58

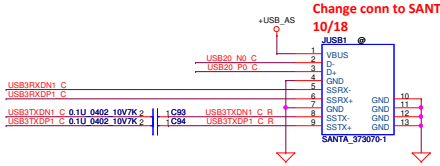
USB3.0

USB3.0 need support 2.5A
change USB PWR SW SA00003TV00
low active

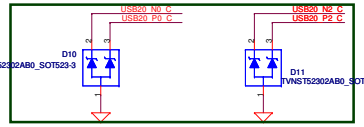


SI# 8/8 change USB_OC0# to USB30_OC#

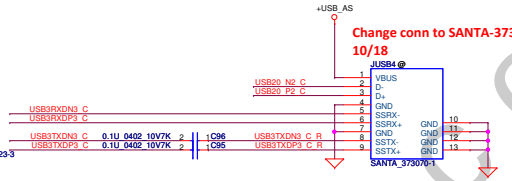
Change conn to SANTA-373070
10/18

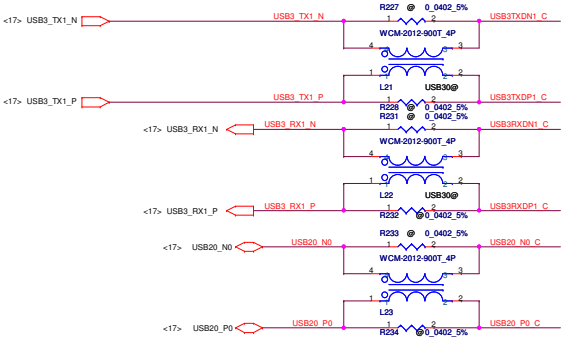


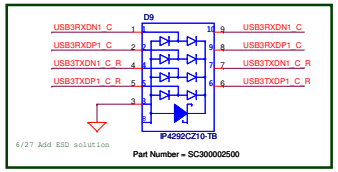
Change P/N from SCA00000T00 to SCA00001L00
11.01
Change P/N to SCA00001W00 for smaller size, 10*10 choke
02.13

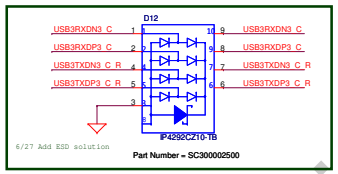


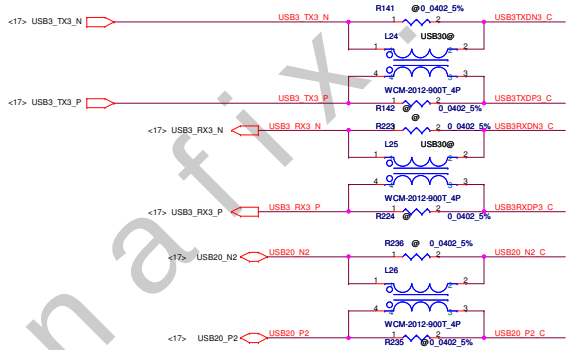
Change conn to SANTA-373070
10/18











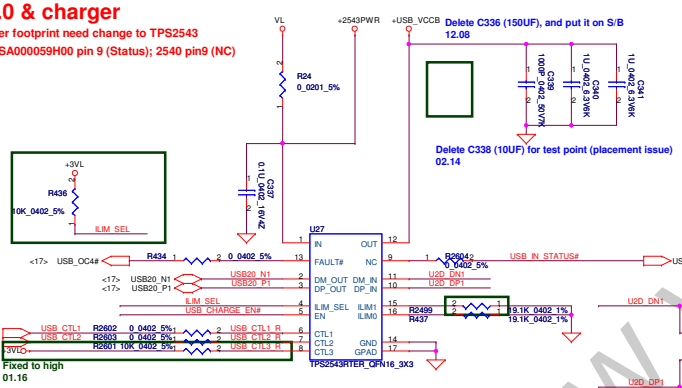
USB2.0 & charger

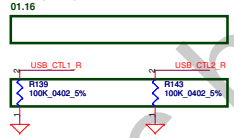
USB charger footprint need change to TPS2543
TPS2543 : SA000059H00 pin 9 (Status); 2540 pin9 (NC)

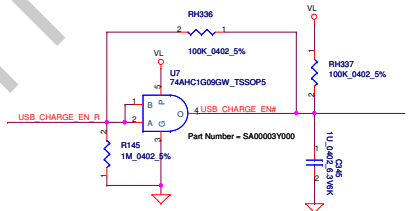
Delete C336 (150UF), and put it on S/B
12.08

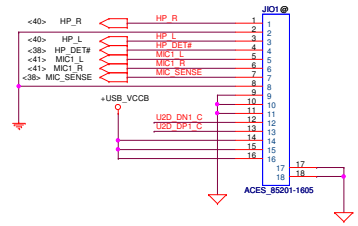
Delete C338 (10UF) for test point (placement issue)
02.14

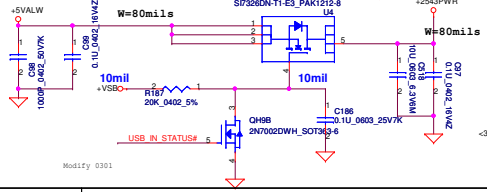
Delete pull-high resistors
01.16

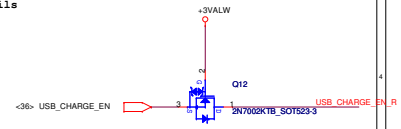


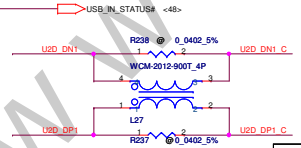












Follow EMI request add choke
11.08

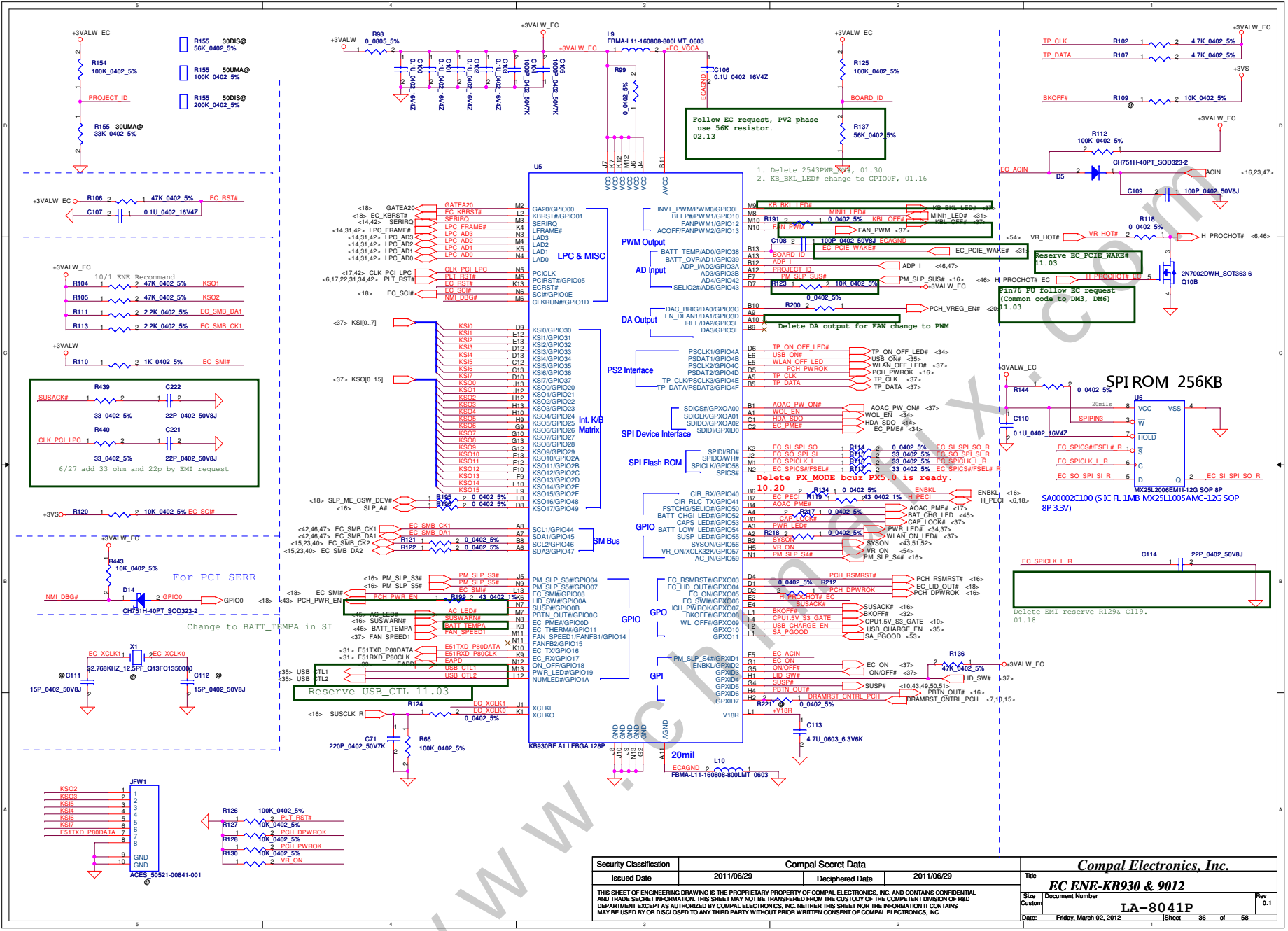
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

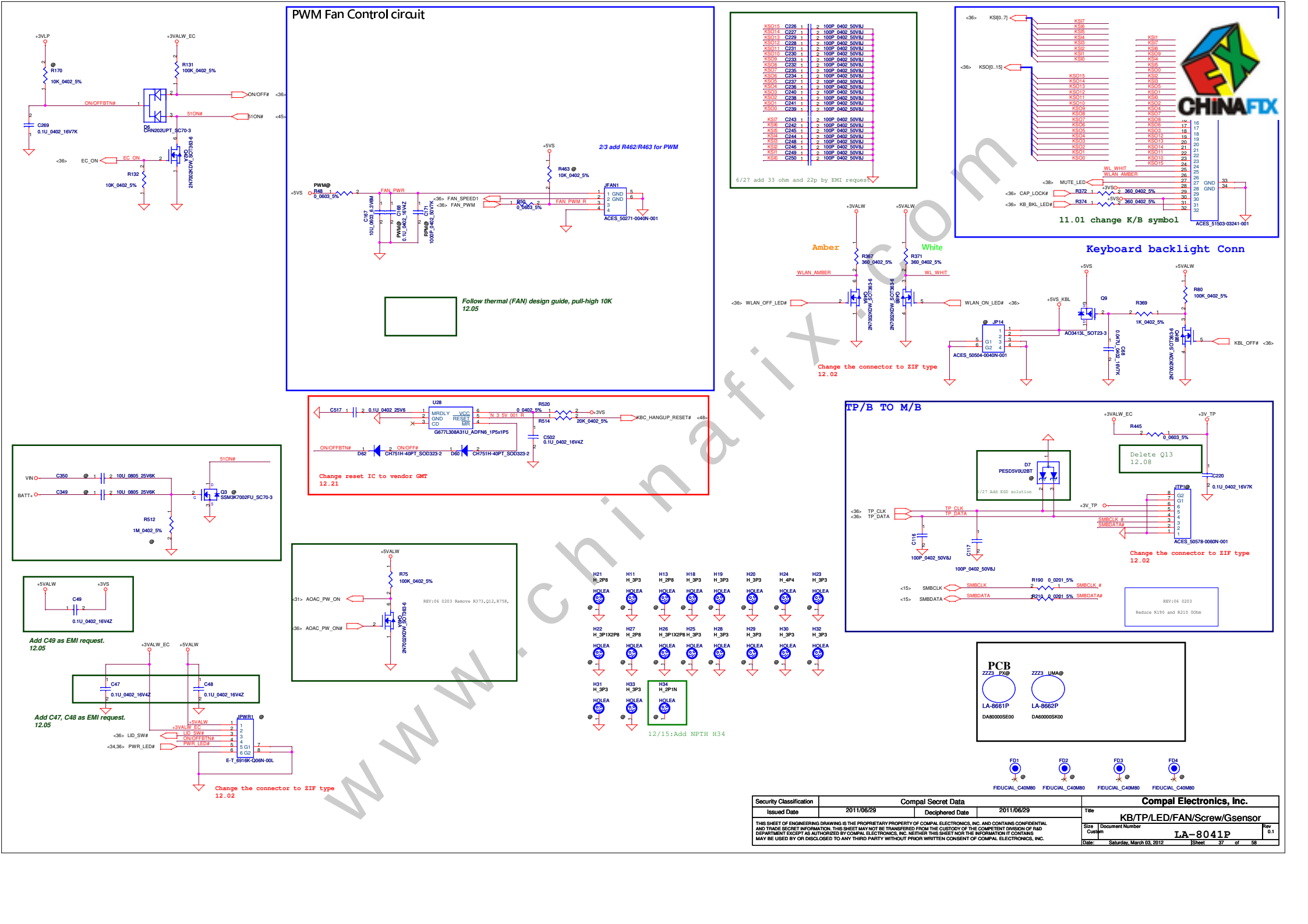
Compal Electronics, Inc.

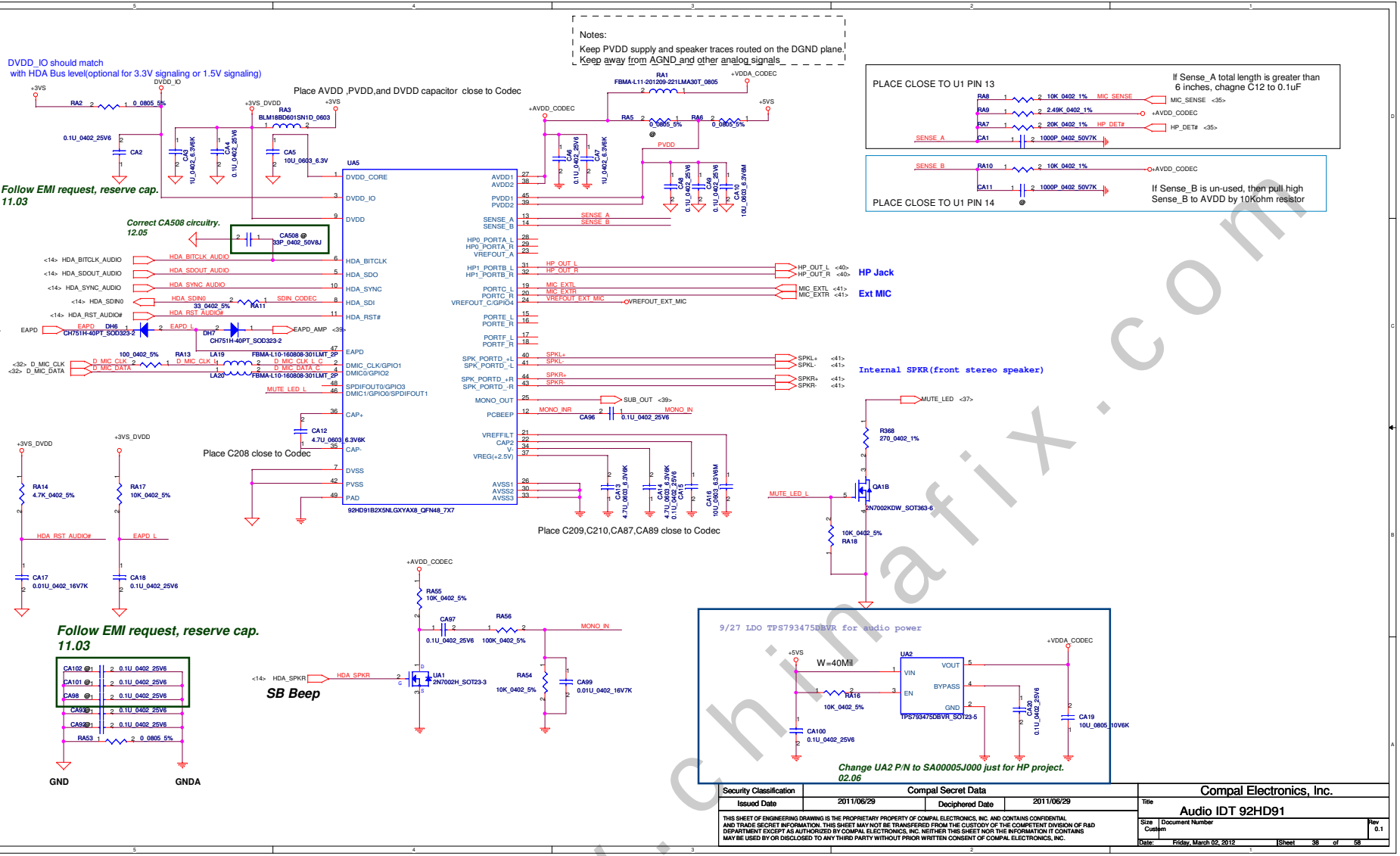
Title: USB Con & Daughter Con

Size: C | Document Number | Rev: 0.1

Date: Monday, March 05, 2012 | Sheet 35 of 58




PWM Fan Control circuit
2/3 add R462/R463 for PWM
Follow thermal (FAN) design guide, pull-high 10K
12.05
6/27 add 33 ohm and 22p by EMI request
11.01 change K/B symbol
Keyboard backlight Conn
Amber
White
Change the connector to ZIF type
12.02
Change reset IC to vendor GMT
12.21
TP/B TO M/B
Delete Q13
12.08
Change the connector to ZIF type
12.02
Add C49 as EMI request.
12.05
Add C47, C48 as EMI request.
12.05
Change the connector to ZIF type
12.02
12/15:Add NPTH H34
PCB
LA-8661P
LA-8662P
Compal Electronics, Inc.
KB/TP/LED/FAN/Screw/Gsensor
LA-8041P
Compal Secret Data
2011/06/29
2011/06/29
Saturday, March 03, 2012



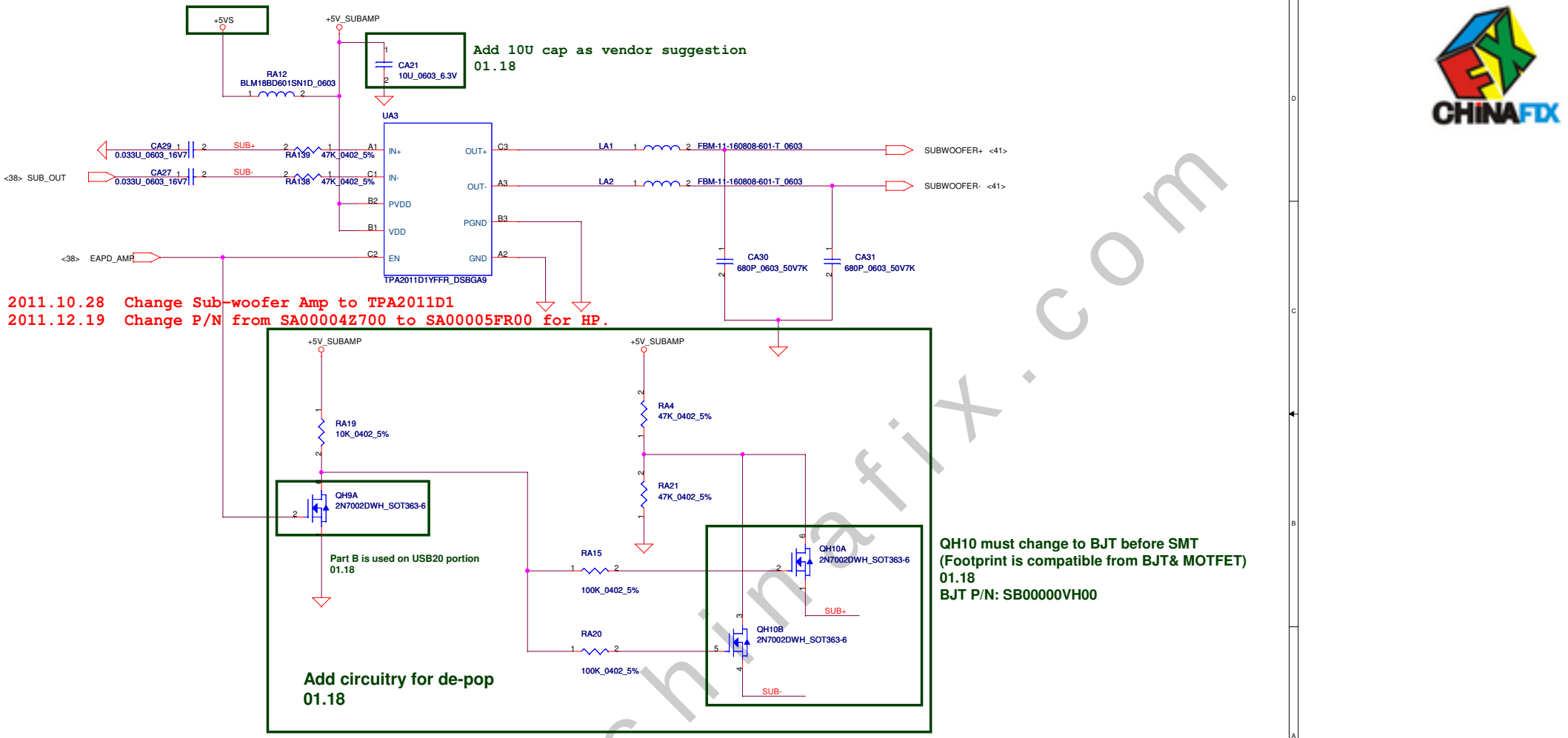
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: Audio IDT 92HD91

Size	Document Number	Rev
Custom		0.1

Date: Friday, March 02, 2012 Sheet 38 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

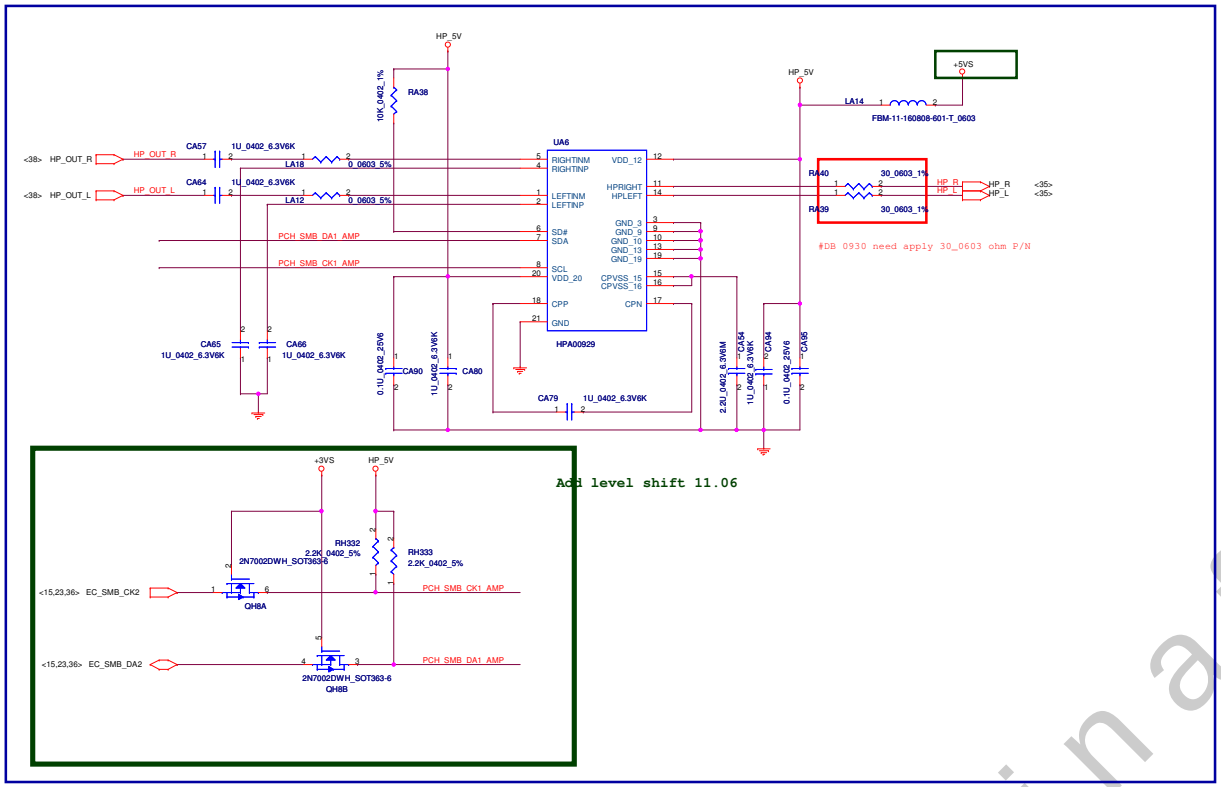
Compal Electronics, Inc.

Title: Audio Woofer Amplifier

Size	Document Number	Rev
B		0.1

Date: Friday, March 02, 2012 Sheet 39 of 58

Headphone amplifier



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

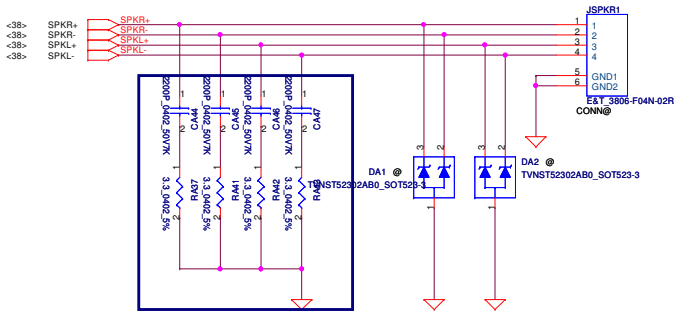
Compal Electronics, Inc.

Title: Audio SPK/HP Amplifier

Size	Document Number	Rev
Custom		0.1

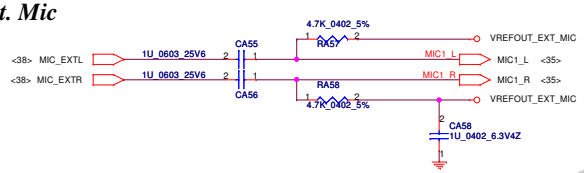
Date: Wednesday, March 07, 2012 Sheet 40 of 58

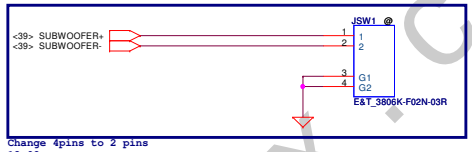
Front Speaker Connector 1



Need place rear Audio Codec (UA5)

Ext. Mic





Change 4pins to 2 pins
12.08

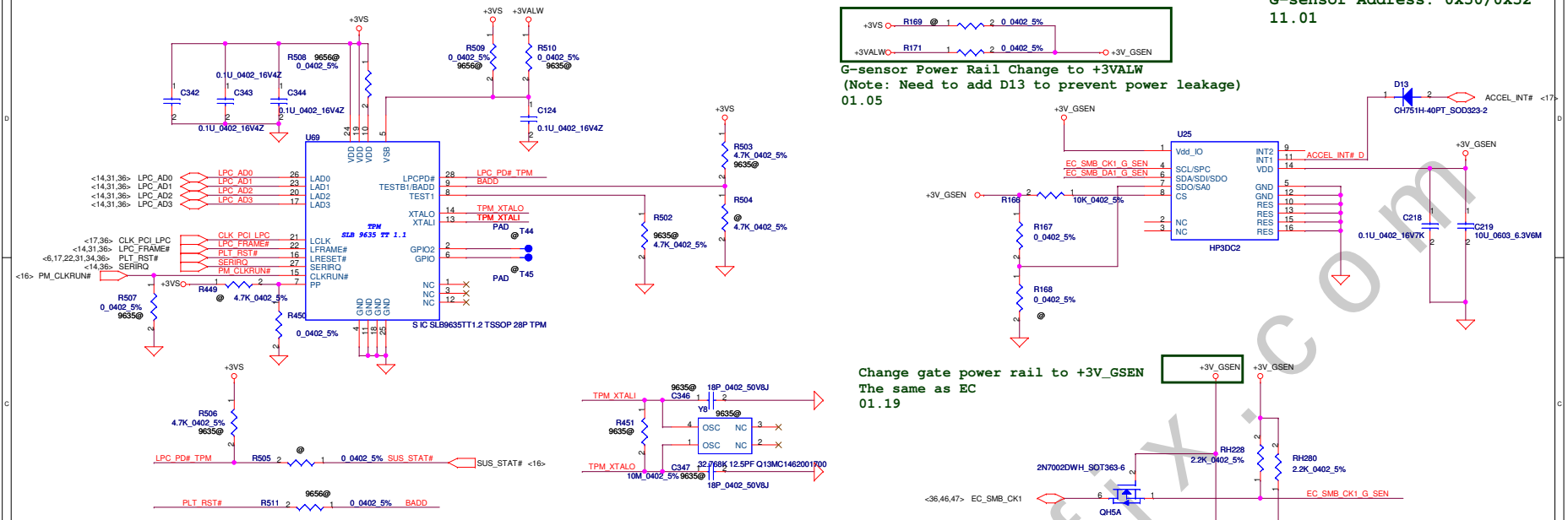
Security Classification	Compal Secret Data		
Issued Date	2009/04/07	Deciphered Date	2012/10/21

Compal Electronics, Inc.

Title: Audio SPK Conn/Jack/MIC

Size	Document Number	Rev
Custom	PAV10	0.1

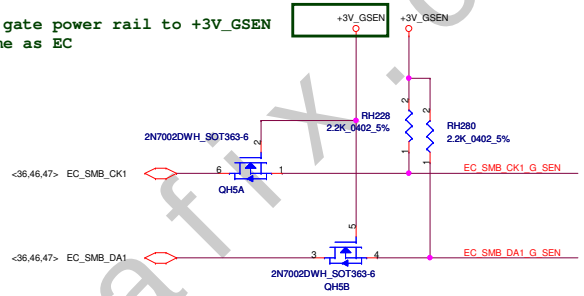
Date: Friday, March 02, 2012 Sheet 41 of 58



G-sensor Address: 0x50/0x52
11.01

G-sensor Power Rail Change to +3VALW
(Note: Need to add D13 to prevent power leakage)
01.05

Change gate power rail to +3V_GSEN
The same as EC
01.19



Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.

Title: TCG/BIOS ROM/PS2/LED/SW

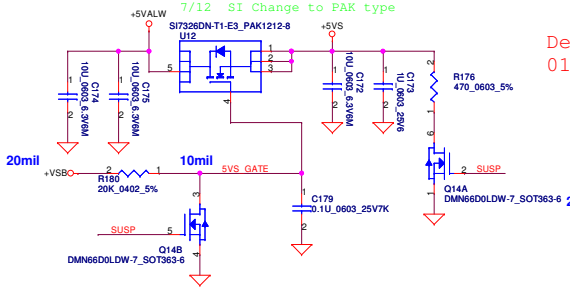
Size	Document Number	Rev
	LA3262P_DIS__M64	0.1

Date: Wednesday, March 07, 2012 Sheet 42 of 58

10.21 Change to PAK type

+5VALW TO +5VS

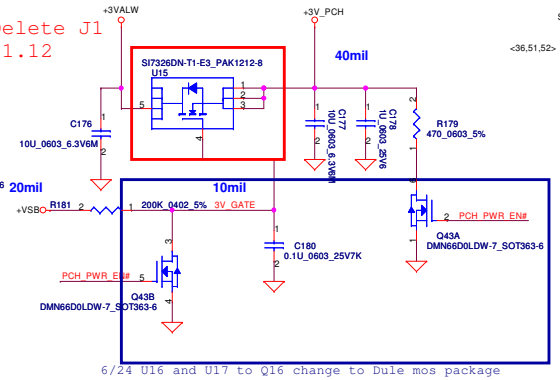
7/12 SI Change to PAK type



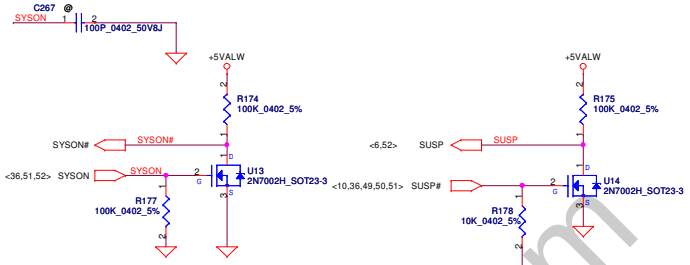
+3VALW TO +3VALW(PCH AUX Power)

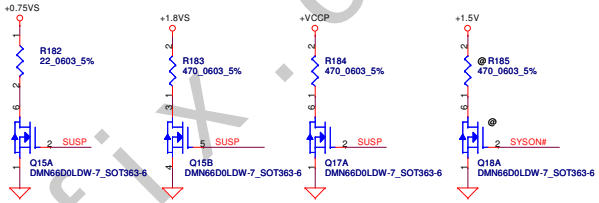
Short J1 for PCH VCCSUS3.3

Delete J1
01.12

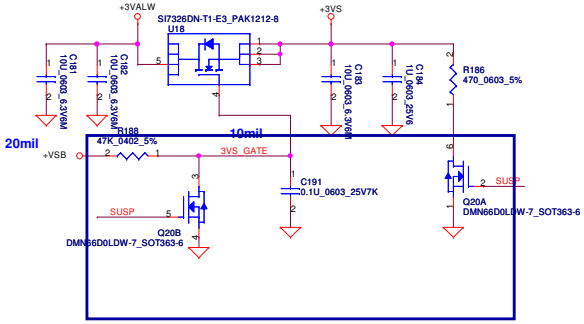


6/24 U16 and U17 to Q16 change to Dule mos package

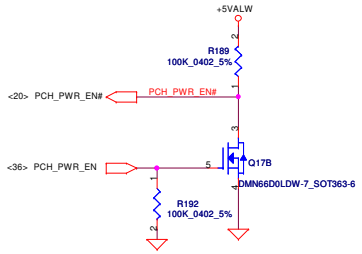




+3VALW TO +3VS



6/24 Q20 and Q21 to Q20 change to Dule mos package



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

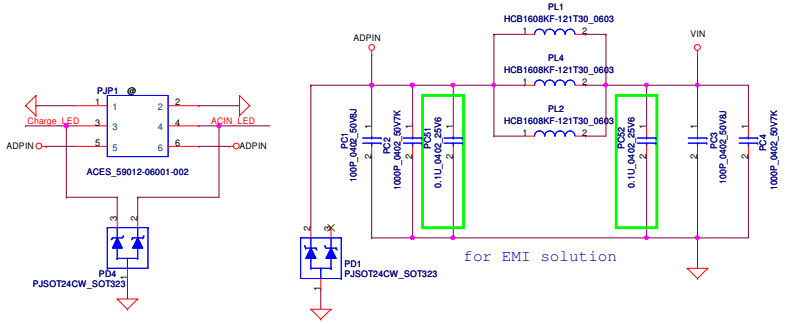
Title: DC Interface

Size	Document Number	Rev
Custom	LA-8661P	0.1

Date: Friday, March 02, 2012 Sheet 43 of 58

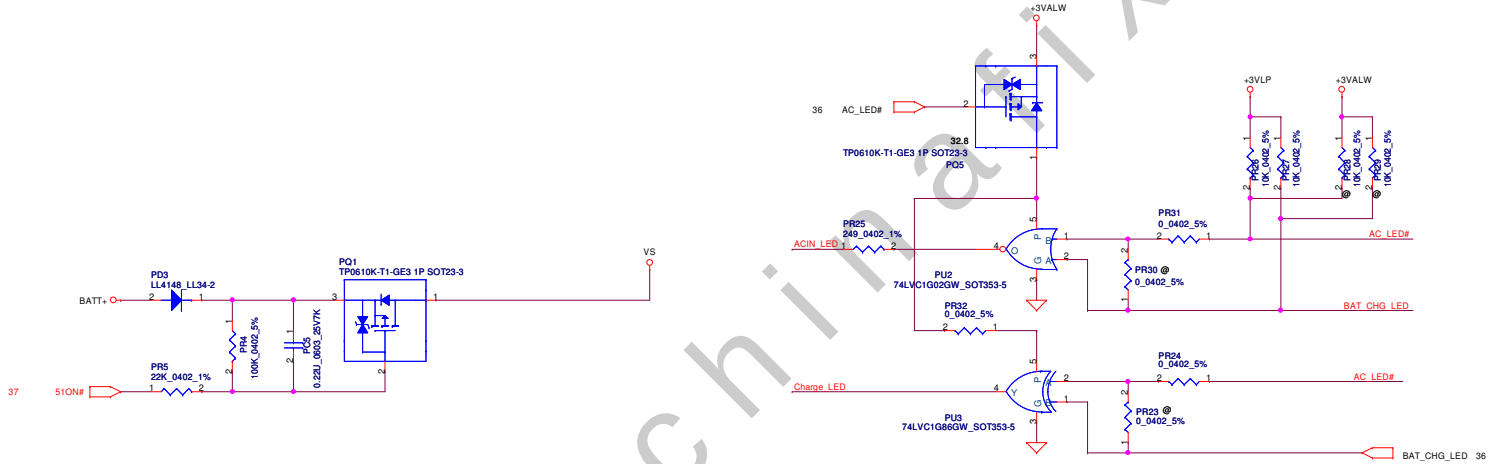
	QAZ60 Strap pin Table		@:un_install	
	Netname	setting	BOM config	
CPU	CFG2	1	RC40 @	1: Normal Operation; Lane # definition matchessocket pin map definition 0: Lane Reversed
	CFG4	1	RC41 @	1 : Disabled; No Physical Display Portattached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
	CFG[6:5]	0 1	RC49 RC48 @	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
	CFG7	1	RC50 @	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
PCH	PCH_INTVRMEN	H	RH124 RH126 @	H ： Integrated VRM enable L ： Integrated VRM disable
	HDA_SPKR	L	RH139 @	H:No Reboot L:Default
	HDA_SYNC	H	RH149	This signal has a weak internal pull-downOn Die PLL VR is supplied by H:1.5V when smapled high L:1.8V when sampled low Needs to be pulled High for Huron River platfrom
	HDA_SDOUT	L	RH140 @	ME debug mode , this signal has a weak internal PD L=>security measures defined in the Flash Descriptor will be in effect (default) H=>Flash Descriptor Security will be overridden
	DSWODVREN	H	RH213 RH215 @	On Die DSW VR Enable H ： Enable L ： Disable
	SLP_ME_CSW_DEV#	H	RH267 RH241 @	On-Die PLL Voltage Regulator This signal has a weak internal pull up H ： On-Die voltage regulator enable L ： On-Die PLL Voltage Regulator disable
	PCH_GPIO37	L	RH245 @ RH246	FDI TERMINATION VOLTAGE OVERRIDE L: Tx, Rx terminated to same voltage(DC Coupling Mode)
	GPIO27	H	RH250 @	PCH_GPIO27 (Have internal Pull-High) H: VCCVRM VR Enable L: VCCVRM VR Disable

Compal Electronics, Inc.			
Title: Strap pin table			
Size: Custom	Document Number: LA-8041P		Rev: 0.1
Date: Friday, March 02, 2012	Sheet 44 of 58		



ESD diode : SCA00001G00

KBC output		Input to Battery		
AC_LED#	BAT_CHG_LED	ACIN_LED	Charge_LED	LED Status
0	0	1	0	White LED light
0	1	0	1	Amber LED light
1	0	0	0	X (don't care)
1	1	0	0	X (don't care)



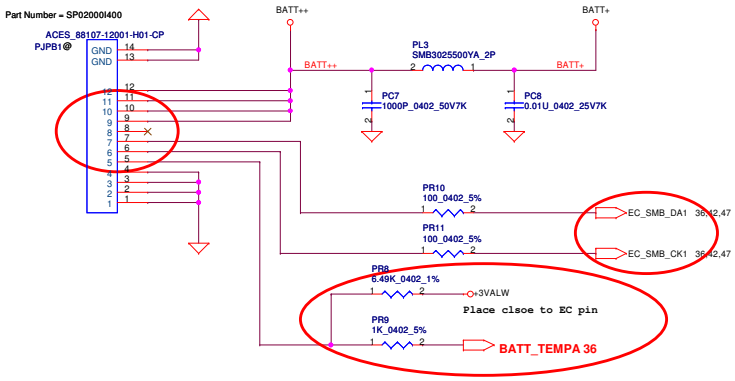
Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

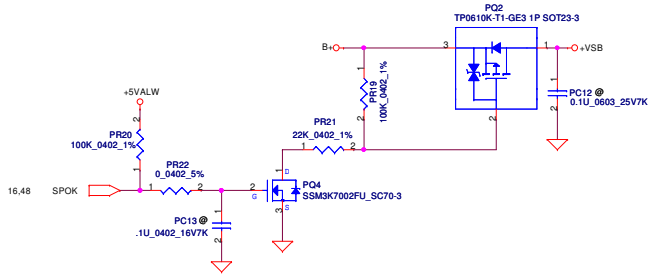
Compal Electronics, Inc.

Title: PWR- DCIN / Vin Detector

Size	Document Number	Rev
Custom	LA-8551P	0.1

Date: Saturday, March 03, 2012 Sheet 45 of 59

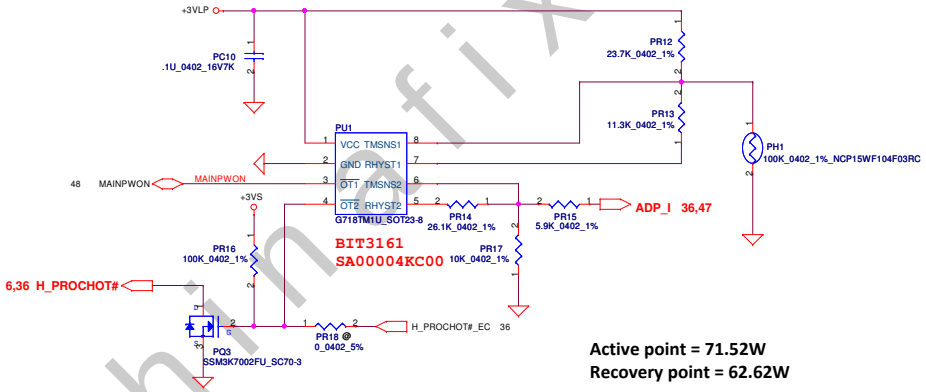




For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 56 +-3 degree C

Rset = 3 * Rtmh
Rhyst = (Rset* Rtml) / (3*Rtml - Rset)
Rtmh at 90C = 7.8K, Rtml at 56C = 26.1K
Rset = 3 * 7.8K = 23.4K ==> 23.7K
Rhyst = (23.4K * 26.1K) / (3 * 26.1K - 23.4K) = 11.12K ==> 11.3K



Active point = 71.52W
Recovery point = 62.62W

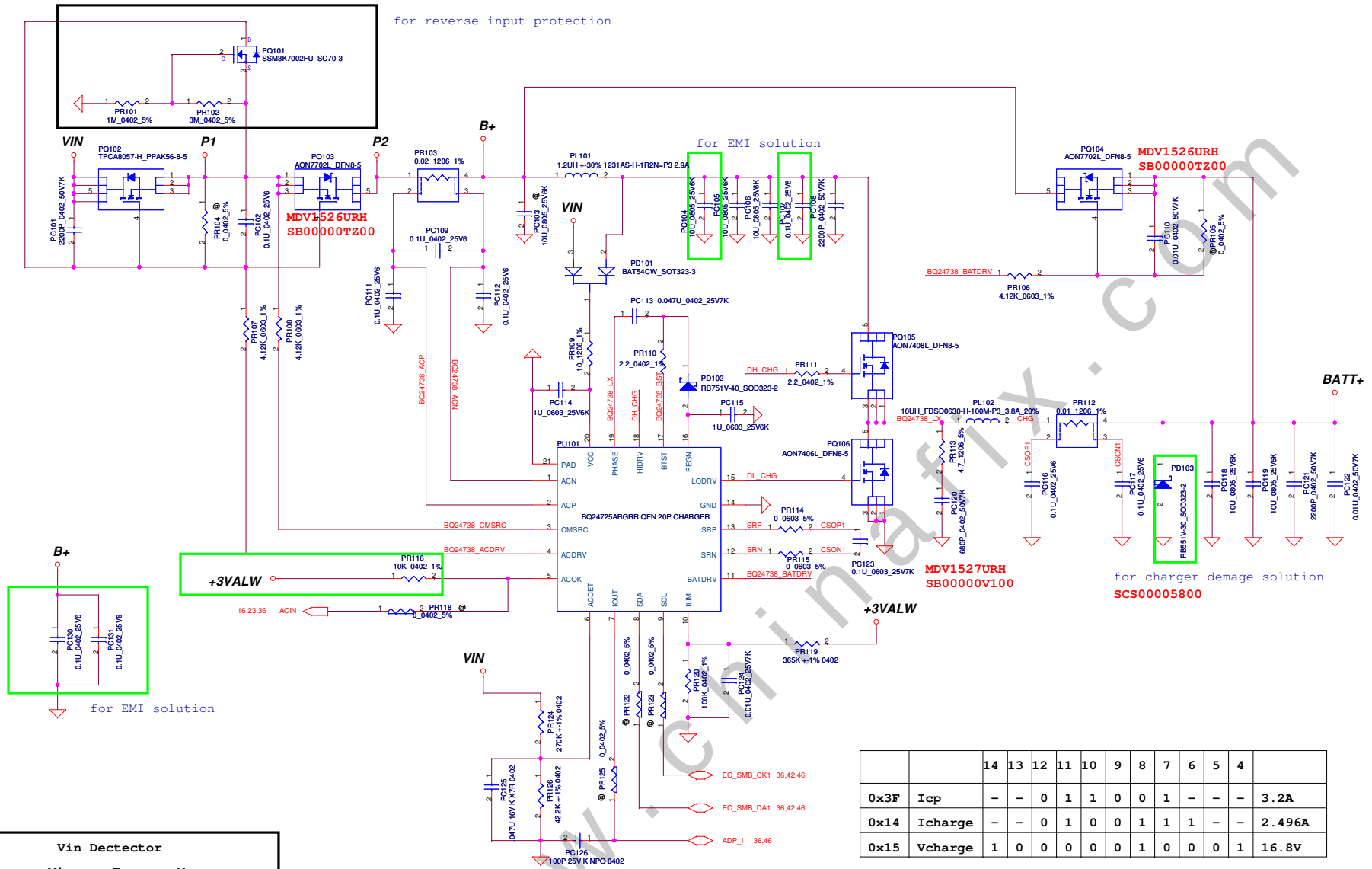
Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: PWR- BATTERY CONN

Size: Custom | Document Number: LA-8551P | Rev: 0.1

Date: Saturday, March 03, 2012 | Sheet 46 of 59



		14	13	12	11	10	9	8	7	6	5	4	
0x3F	Icp	-	-	0	1	1	0	0	1	-	-	-	3.2A
0x14	Icharge	-	-	0	1	0	0	1	1	1	-	-	2.496A
0x15	Vcharge	1	0	0	0	0	0	1	0	0	0	1	16.8V

Vin Dectector

	Min.	Typ.	Max.
L-->H	17.45V	17.92V	18.42V
H-->L	16.89V	17.52V	18.16V

ILIM and external DPM
3.54A

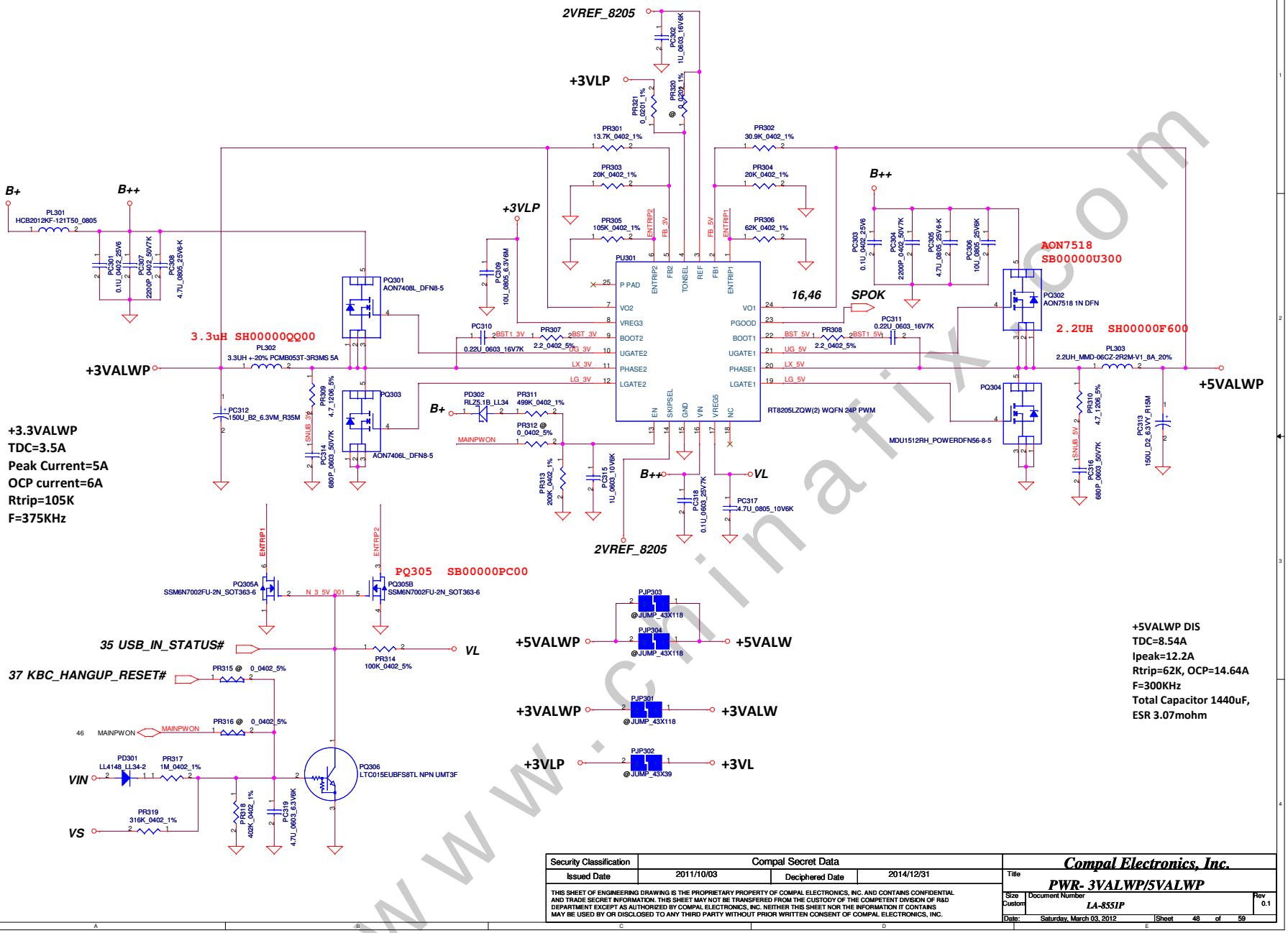
Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: PWR- CHARGER

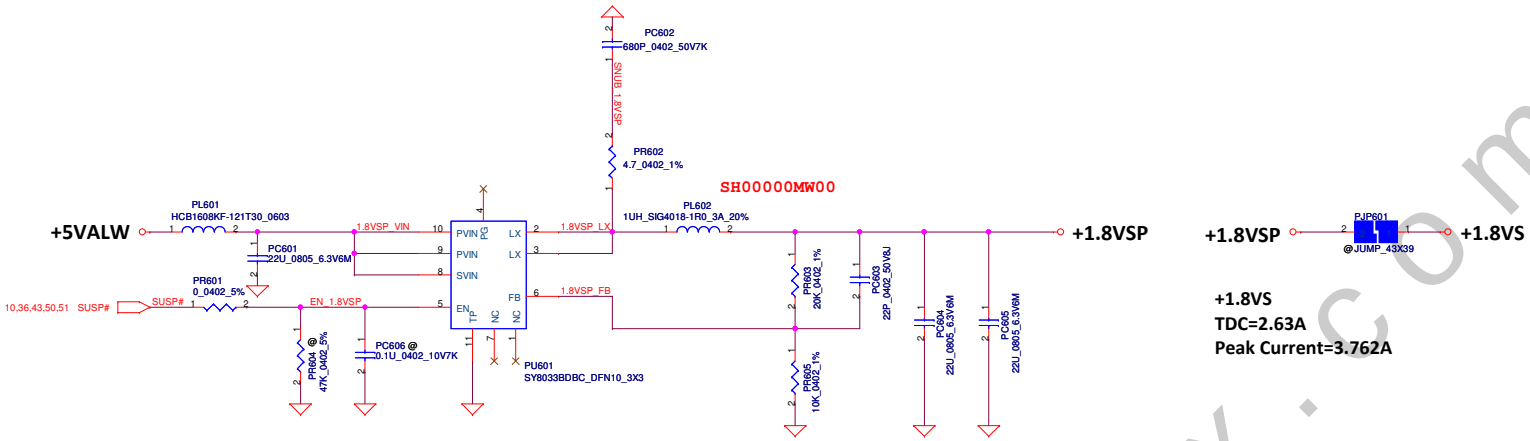
Size	Document Number	Rev
	LA-8551P	0.1

Date: Saturday, March 03, 2012 Sheet 47 of 59



Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

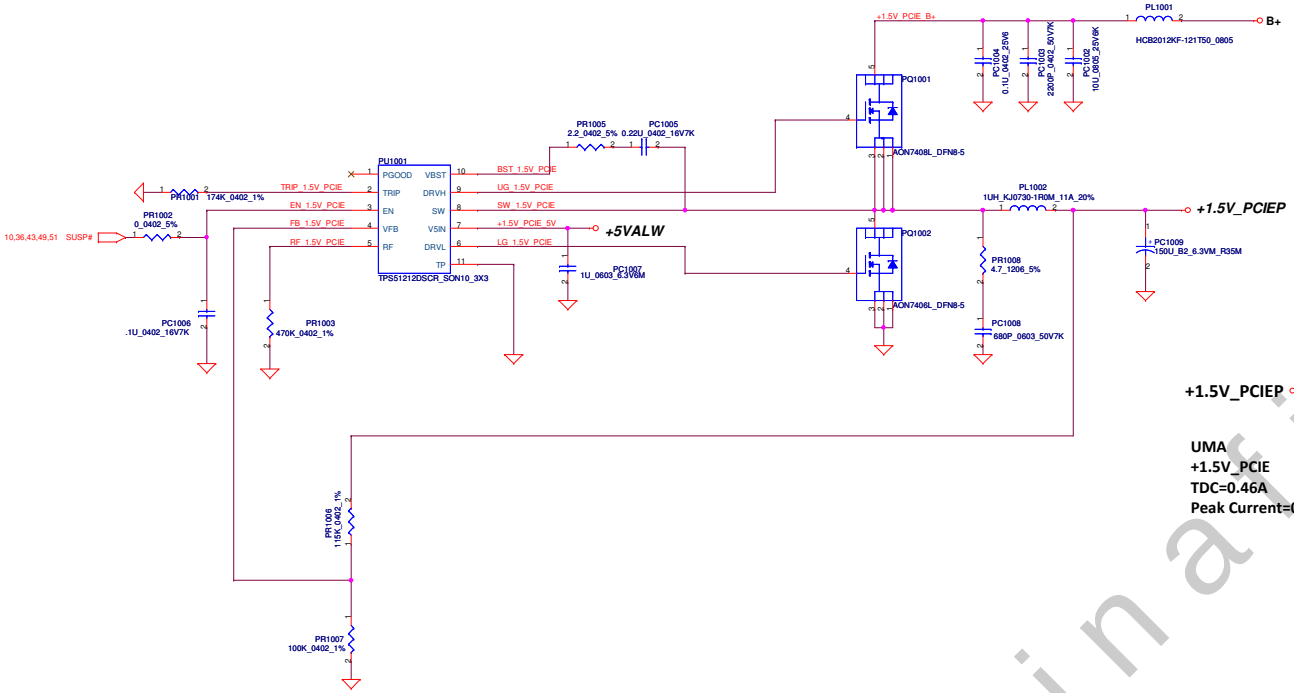
Compal Electronics, Inc.			
Title	PWR- 3VALWP/5VALWP		
Size: Custom	Document Number: LA-8551P		Rev: 0.1
Date: Saturday, March 03, 2012	Sheet 48 of 59		



+1.8VS
TDC=2.63A
Peak Current=3.762A

Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.			
Title: PWR- 1.8VS			
Size	Document Number: LA-8551P		Rev: 0.1
Date: Saturday, March 03, 2012		Sheet 49 of 59	



+1.5V_PCIEP — PJP1001 JUMP_43X118 — +1.5V_PCIE

UMA	DIS
+1.5V_PCIE	+1.5V_PCIE
TDC=0.46A	TDC=6A
Peak Current=0.66A	Peak Current=8A

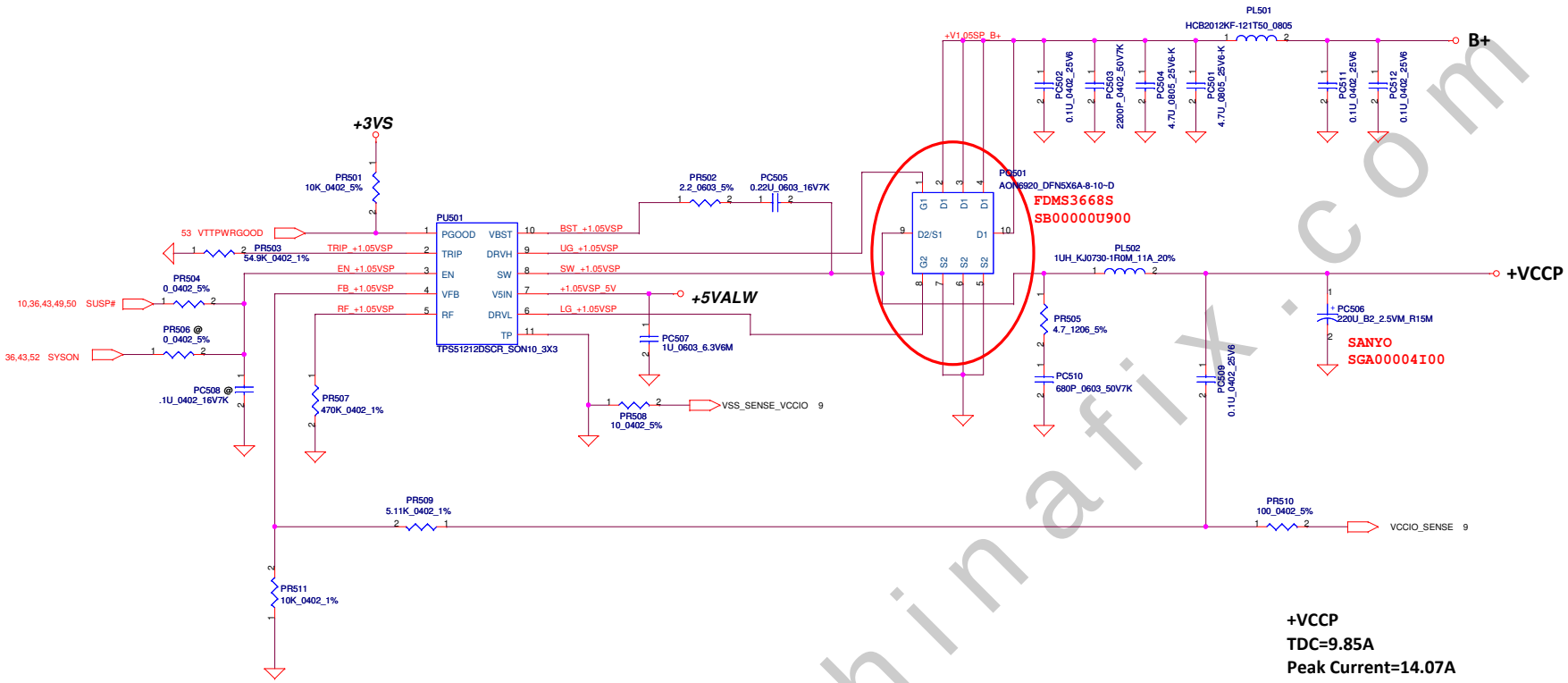
Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: PWR- VGA_VDDC

Size	Document Number	Rev
C	LA-8551P	0.1

Date: Saturday, March 03, 2012 Sheet 50 of 59



+VCCP
TDC=9.85A
Peak Current=14.07A
OCP current=16.88A
Rtrip = 54.9K

Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

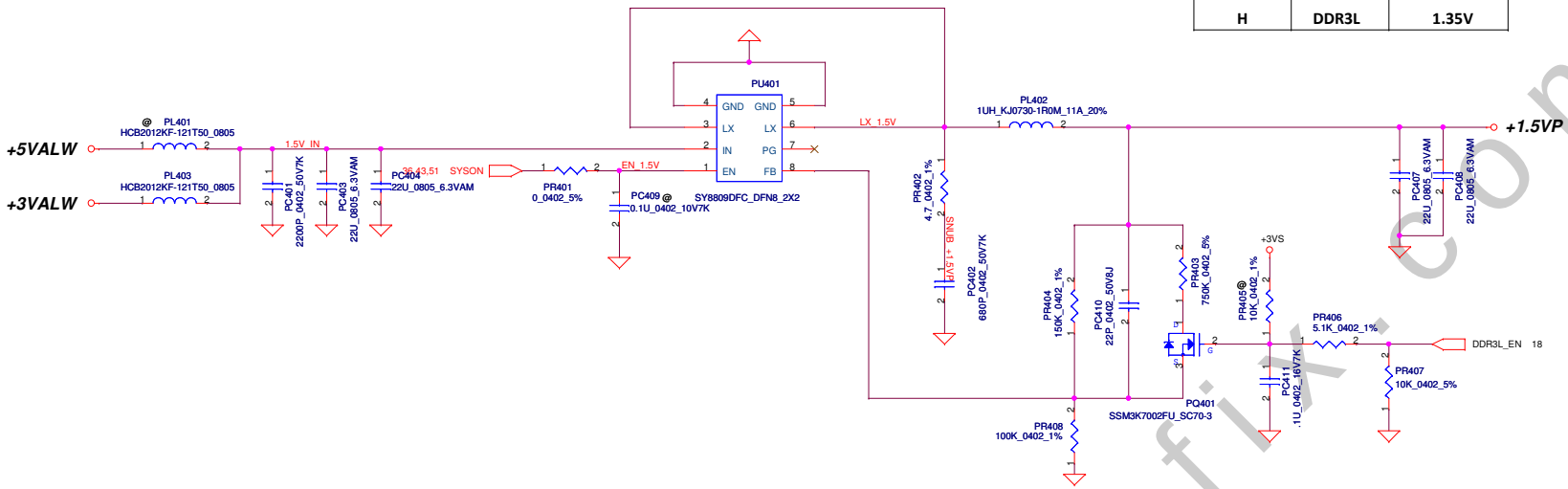
Compal Electronics, Inc.

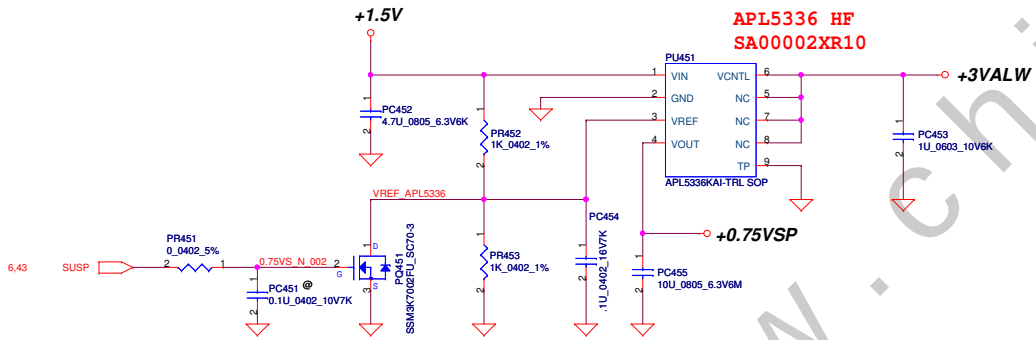
Title: PWR- VCCP

Size: Custom | Document Number: LA-8551P | Rev: 0.1

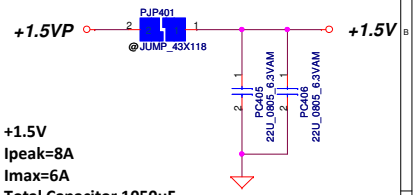
Date: Saturday, March 03, 2012 | Sheet 51 of 59

DDR3L_EN		1.5VP
L	DDR3	1.5V
H	DDR3L	1.35V





+0.75VSP
TDC=1.4A
Peak Current=2A



+1.5V
Ipeak=8A
Imax=6A
Total Capacitor 1050uF,
ESR 4.43mohm

HW side:
C106 330uF 17m
C218 390uF 10m
VGA@ CV122 390uF 10m
@ C189 330uF 15m

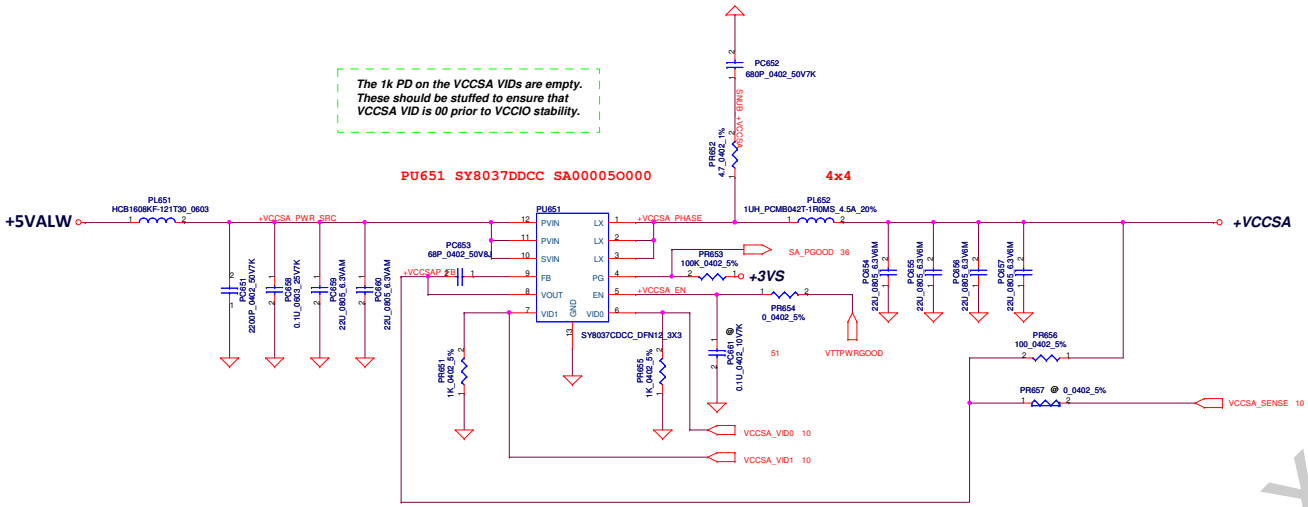
Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: **PWR- 1.5VP/0.75VSP**

Size	Document Number	Rev
Custom	LA-8551P	0.1

Date: Saturday, March 03, 2012 Sheet 52 of 59



+VCCSA
Itdc=3A
Imax=4A

Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

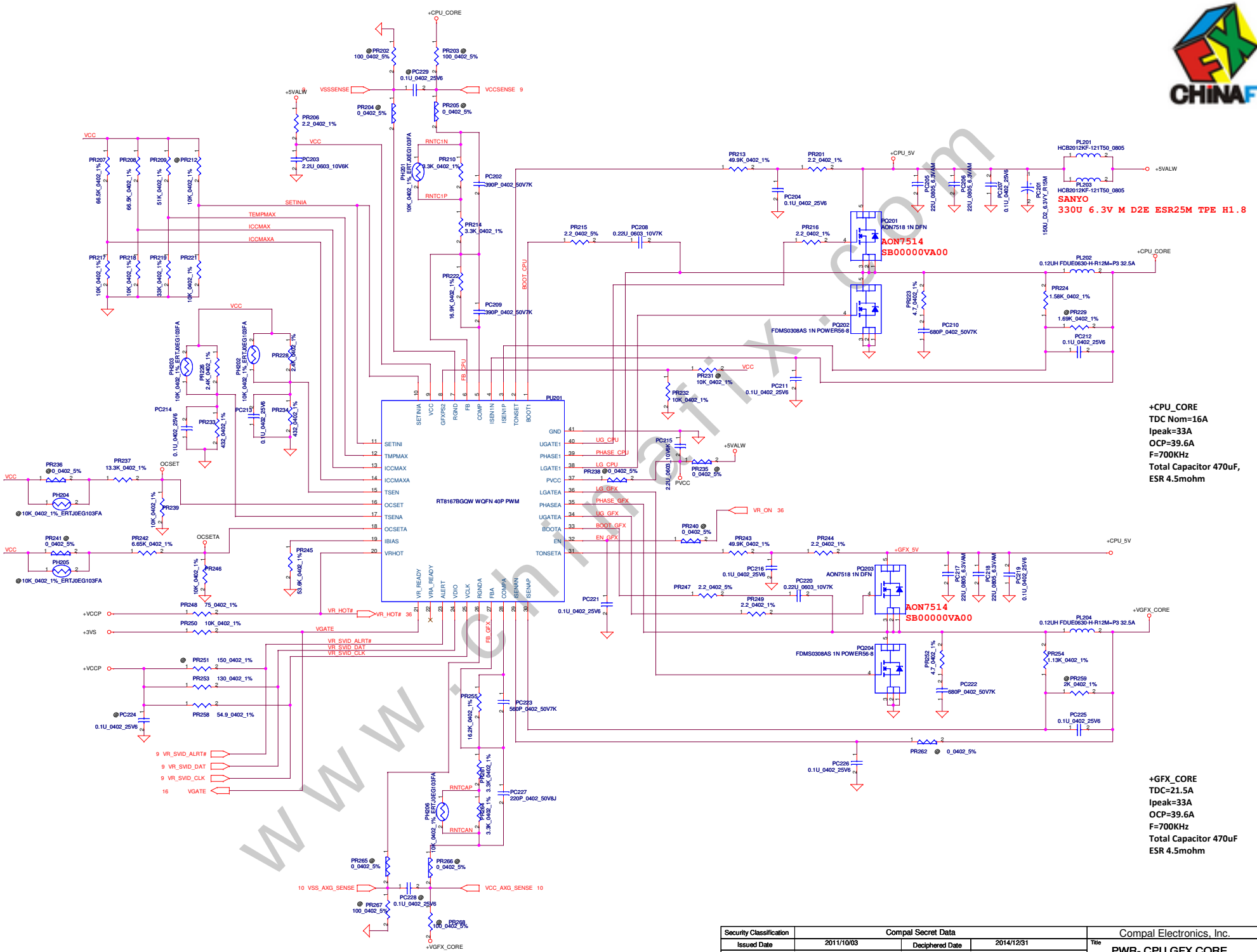
Compal Electronics, Inc.

Title: PWR- VCCSA

Size	Document Number	Rev
C	LA-8551P	0.1

Date: Saturday, March 03, 2012 Sheet 53 of 59

QCL70



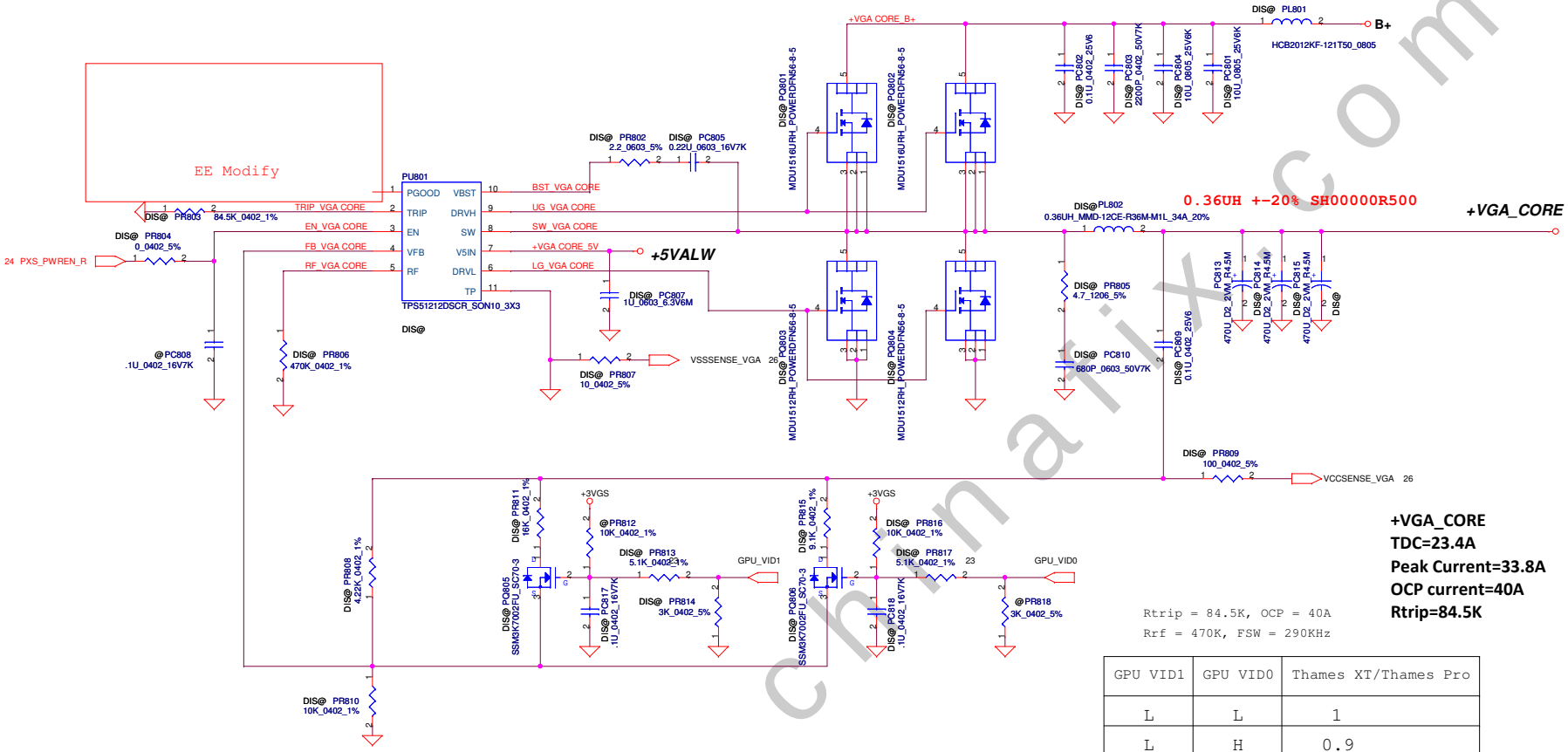
Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: PWR- CPU GFX CORE

Size	Document Number	Rev
A2	LA-8551P	0.1

Date: Saturday, March 03, 2012 Sheet 54 of 59



GPU VID1	GPU VID0	Thames XT/Thames Pro
L	L	1
L	H	0.9
H	L	0.94
H	H	0.875

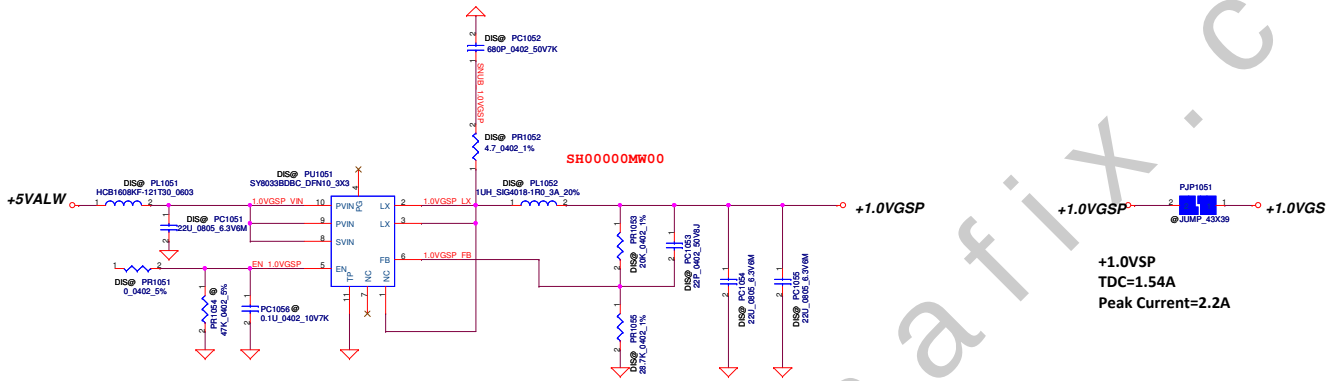
Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: PWR- VGA_VDDC

Size: Custom | Document Number: LA-8551P | Rev: 0.1

Date: Wednesday, March 07, 2012 | Sheet 55 of 59



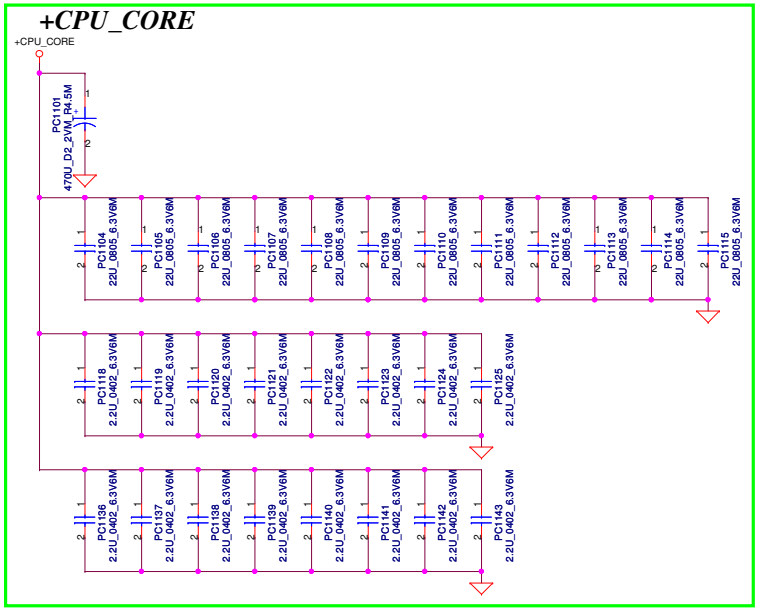
Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

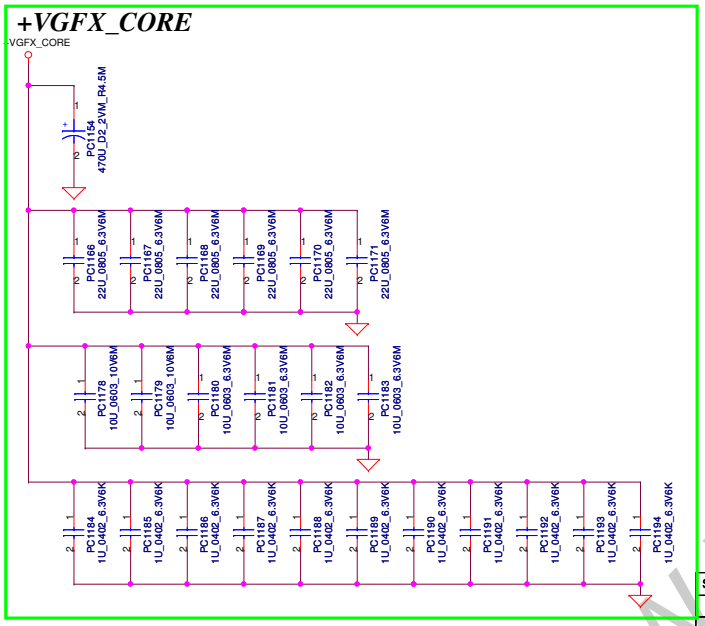
Compal Electronics, Inc.

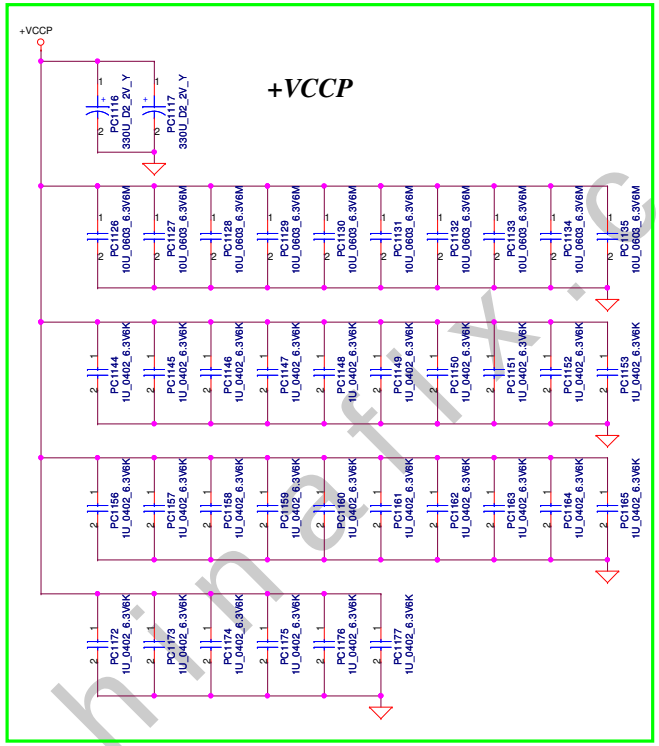
Title: **PWR- VGA 1.0VGSP**

Size	Document Number	Rev
C	LA-8551P	0.1

Date: Monday, March 05, 2012 Sheet 56 of 59







Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: **PWR - PROCESSOR DECOUPLING**

Size	Document Number	Rev
	LA-8551P	0.1

Date: Saturday, March 03, 2012 Sheet 57 of 59

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	47	change PC111 to 0402	2011/11/28		For layout space		
2	47	remove PR121	2011/11/28		0ohm, not needed		
3	47	change PR124 to 270K, PR126 to 42.2K	2011/11/28		change Vin detector setting		
4	47	change PC125 to 0.047uF	2011/11/28				
5	47	change PR125 to 0ohm, PC126 to 100pF	2011/11/28		FAE review recommand		
6	47	change PR119 to 365K	2011/11/28		modify charge Ilimit to 3.54A		
7	47	change PR111 to 0ohm	2011/11/28				
8	47	add PL101	2011/11/28				
9	46	delete PD5, PD6	2011/11/28		imbedded battery, ESD diode is not needed		
10	46	SMC, SMD exchange	2011/11/28				
11	46	delete pin8 and pin5, add battery temp sense at pin5.	2011/11/28		EC request to need one detect pin if SMB communication fail.		
12	47	change PQ302 to AON7518	2011/11/28				
13	50, 52	change PU1001, PU401 from SY8036HDBC to SY8036LDBC	2011/11/28				
14	53	change PU651 from SY8037DCC to SY8037ADCC	2011/11/28				
15	52	add PQ401, PR406, PR407, PC411	2011/11/28				
16	56	change PR1055 to 28.7K	2011/11/28		for correct 1.0V voltage		
17	54	change PL202, PL204 to SH00000PP00, 0.12uH	2011/11/28				
18	54	change PU201 to RT8167, SA00005AU00	2011/11/28				
19	54	change PQ201, PQ203 to AON7518, SB00000U300	2011/11/28				
20	54	change PQ202, PQ204 to FDMS0308AS, SB00000U400	2011/11/28				
21	55	change PL802 to 0.36uH, SH00000HD00	2011/11/28				
22	52	change PU401 to SY8809DFC	2011/11/29				
23	45, 48	change PD2, PD301 DIO CD4148WN-1 1206	2011/11/29		For cost and layout space		
24	51	add PC511, PC512	2011/12/11				
25	54	change PL201 to 0805, and add PL203	2011/12/11				
26	48	add PR320	2011/12/11		tune frequency		
27	55	change PC813, PC814, PC815, PC816 tp 330uF 9m	2011/12/11				
28	47	change PQ101 to SB000009610	2011/12/11				
29	54	change PR210, PR214, PR261, PR264 to 3.3K; PR222 to 15.8K; PR255 to 10.5K; PC202, PC209 to 270p; PC223 to 220p; PC227 to 560p; PR224, PR254 to 1.82K; PR207 to 127K	2011/12/11		Fine tune CPU, GFX transient		
30	47, 54	change PR111, PR110, PR216, PR249 to 2.2 ohm	2011/12/12		For EMI solution		
31	53, 56	change PL602, PL1052 to SH00000MW00	2011/12/12		For crack issue		
32	55	change PL802 to SH00000HQ00	2011/12/12		For thermal solution		
33	48	change PL303 to SH000000N00	2011/12/12		For thermal solution		
34	47	change PR114, PR115 to 0 ohm	2011/12/14		Prevent charger damaged by negative output voltage		
35	54	change PR207 to 66.5K	2011/12/14		For GFX GT2 current limit		
36	54	change PR237 to 23.7K +-1% 0402	2011/12/23				
37	54	change PR241 to 1/16W 0 +-5% 0402	2011/12/23				
38	54	change PR242 to 23.7K +-1% 0402	2011/12/23				
39	47	change PQ103, PQ104 to SB00000TZ00	2011/12/23				
40	47, 48	change PQ106, PQ303 to SB00000H700	2011/12/23				
41	54	change PR210,PR261,PR264 to 3.3K +-1% 0402	2011/12/23				
42	53	change PL651 to SY8037CDCC	2012/1/11		For latch mode		
43	57	change PC1180, PC1181, PC1182, PC1183 to SE000005T80	2012/1/11		For height limit		
44	46	Delete PC11	2012/1/12		For ME request		

Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

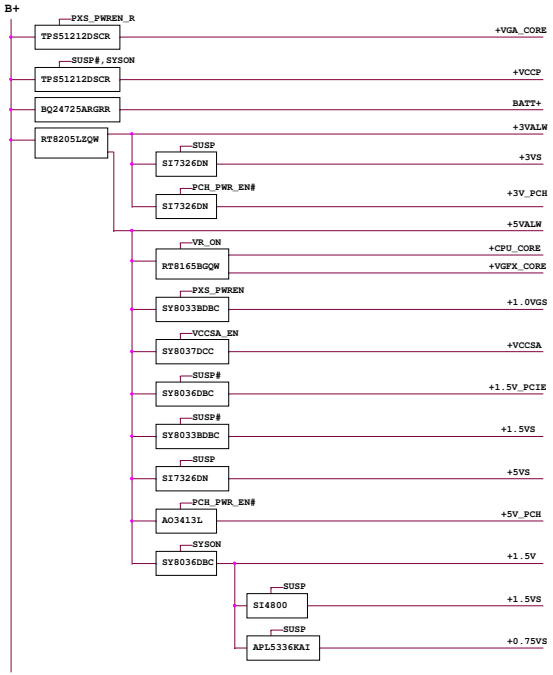
Compal Electronics, Inc.			
Title	PWR - PIR		
Size	Document Number		Rev
	LA-8551P		0.1
Date:	Saturday, March 03, 2012	Sheet	58 of 59

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
45	47	change PR114 to 10, PR115 to 6.8ohm, add PD103	2012/1/30		For Charger issue		
46	47	Add PC130, PC131, PC104, PC107	2012/1/30		For EMI solution		
47	48	Add PR321	2012/1/30		Choose working frequency to improve efficiency and thermal		
48	50	change 1.5VPCIE Circuit	2012/1/30		Change input voltage form 5V to 19V to slove thermal issue		
49	52	Add PL403	2012/1/30		Choose input voltage to slove thermal issue		
50	54	Change PR224 to1.58Kohm, PC209 to 220PF, PC202 to 390PF, PR222 to 16.9Kohm, PR237 to 21.5K	2012/1/30		Base on SI layout, FAE review recommand value		
51	48	change PL303 to SH00000F600	2012/1/30		For thermal issue		
52	45	Delete PD2, PR2, PR3, PC6	2012/1/30		For Layout space		
53	47, 48, 54	Change PQ302, PQ201, PQ203 to AON7514	2012/1/30		For efficiency		
54	51	Delete PJP501	2012/1/30		For Layout space		
55	55	Change PC813, PC814, PC815 to 470uF, delete PC816 Change PL802 0.36uF to 13*13*3.5 size	2012/1/30		For thermal issue		
56	55	Add PC820, PC821, PC822	2012/1/30		For VGA transient voltage		
57	57	Change PC1180, PC1181, PC1182, PC1183 to SE000005T80	2012/1/30		For ME request		
58	47	change PQ102 to TPCA8057	2012/1/30				
59	54	change PC223 to 560pF, PC227 to 220pF	2012/2/17		For FAE suggesstion		
60	48	change PQ302 to AON7518	2012/2/17		For efficiency		
61	55	change PL802 to 13*13*3 size	2012/2/17		For thermal solution		
62	47	change PR114, PR115 to 0 ohm, PD103 to SCS00005800	2012/2/17		For HP and soucer request		
63	54	change PC201 to 330uF	2012/2/17		For acoustic solution		
64	45	change LED circuit	2012/2/23				
65	48	change PL303 to 3.3uH 10*10*3H, PC313 to 150U_B2_6.3VM_R35M, remove 5V output jumper	2012/2/23		For thermal solution		
66	53	change PU651 to SY8037DDCC	2012/2/23		For ULV CPU and latch mode		
67	55	change PR812 and PR816 power to +3VGS	2012/2/23		For leakage issue		
68	45	change LED circuit	2012/2/29				
69	54	change PC209 to 390pF, PR237 to 13.3Kohm, PR254 to 1.13Kohm, PR255 to 16.2Kohm, PR242 to 6.65Kohm	2012/2/29		Base on PV layout		
70	45	change PL1, PL2 to 0603 size, add PL4	2012/2/29		EMI request		

Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.			
Title	PWR - PIR		
Size	Document Number		Rev
	LA-8551P		0.1
Date:	Saturday, March 03, 2012	Sheet	59 of 59



File	<Title>		
Size: B	Document Number: <Doc>		Rev: <RevCode>
Date: Saturday, March 03, 2012	Sheet 60 of 59		