LF15V/A
Schematics Document

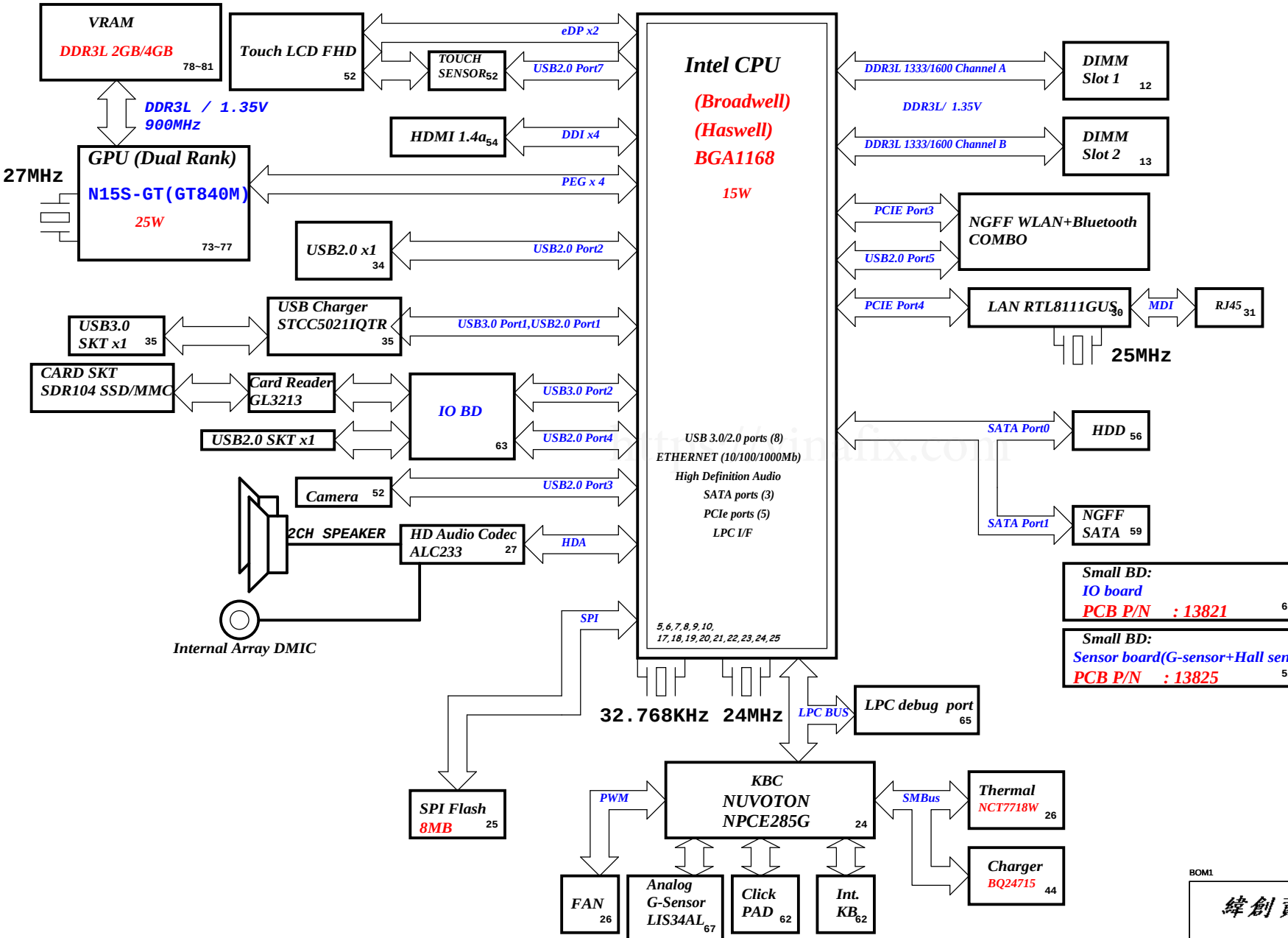
BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Cover Page**		
Size: A3	Document Number: **LF15V**	Rev: **-1**
Date: Monday, July 14, 2014	Sheet 1 of 102	

LF15V/A Board Block Diagram

Project code : 4PD00W010001
PCB P/N : 13286



CHARGER BQ24715	44
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC TPS51225	45
INPUTS	OUTPUTS
DCBATOUT	5V_Charger 3D3V_S5

CPU DC/DC TPS51622	46-47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC SYS8208A	48
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC RT8207	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3

SYSTEM DC/DC	
INPUTS	OUTPUTS

SYSTEM DC/DC RT9025	51
INPUTS	OUTPUTS
DCBATOUT	1D5V_S0

RT8812A	82
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

Switches	83
INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0
1D35V_S0	1D35V_VGA_S0
1D05V_VTT	1D05V_VGA_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

BOM1

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Title: Block Diagram

Size	Document Number	Rev
Custom	LF15V	-1

Date: Monday, July 14, 2014 Sheet 2 of 102

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

LF15V Page Arrangement

BOM1

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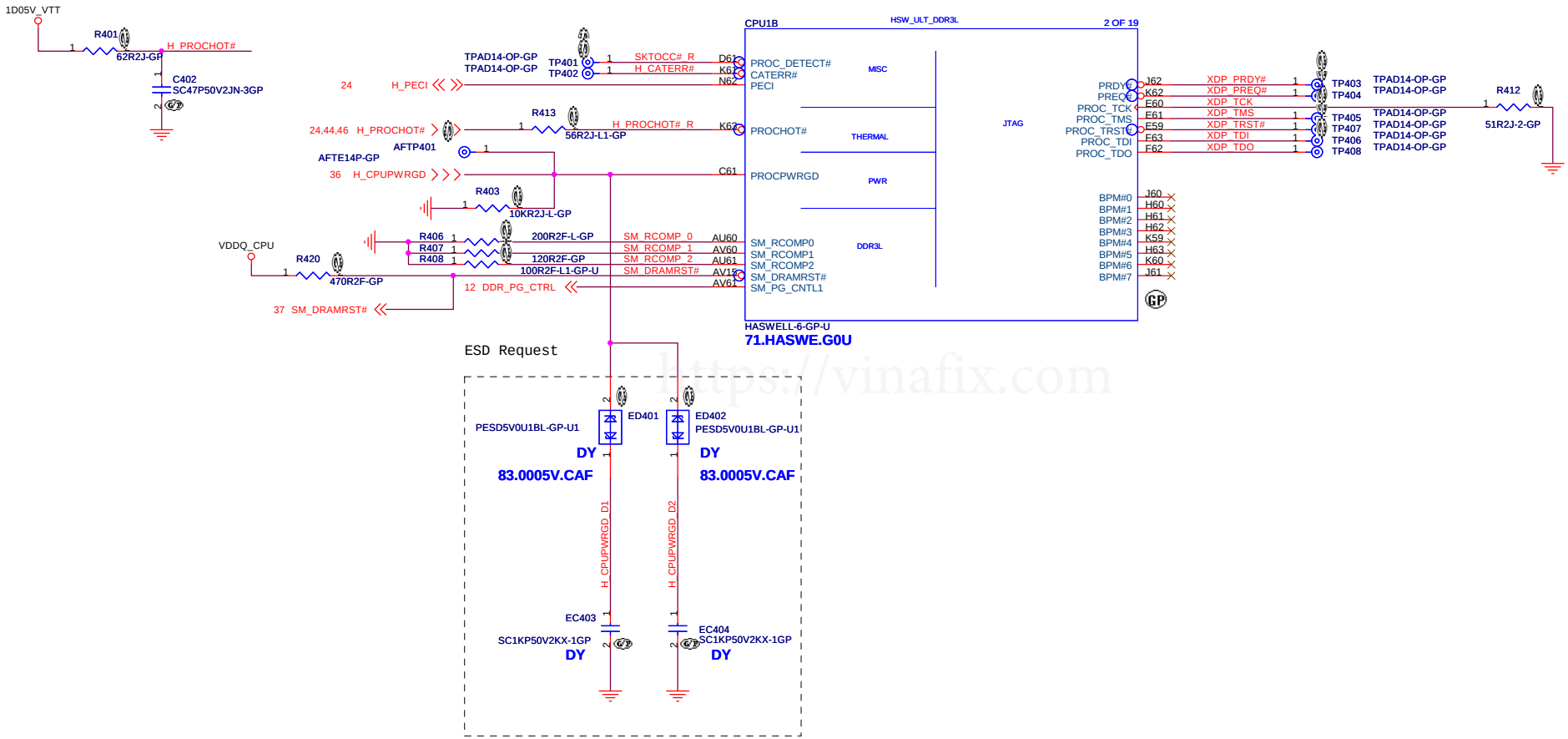
Title: Table of Content

Size	Document Number	Rev
A3	LF15V	-1

Date: Monday, July 14, 2014 Sheet 3 of 102

SSID = CPU



BOM1

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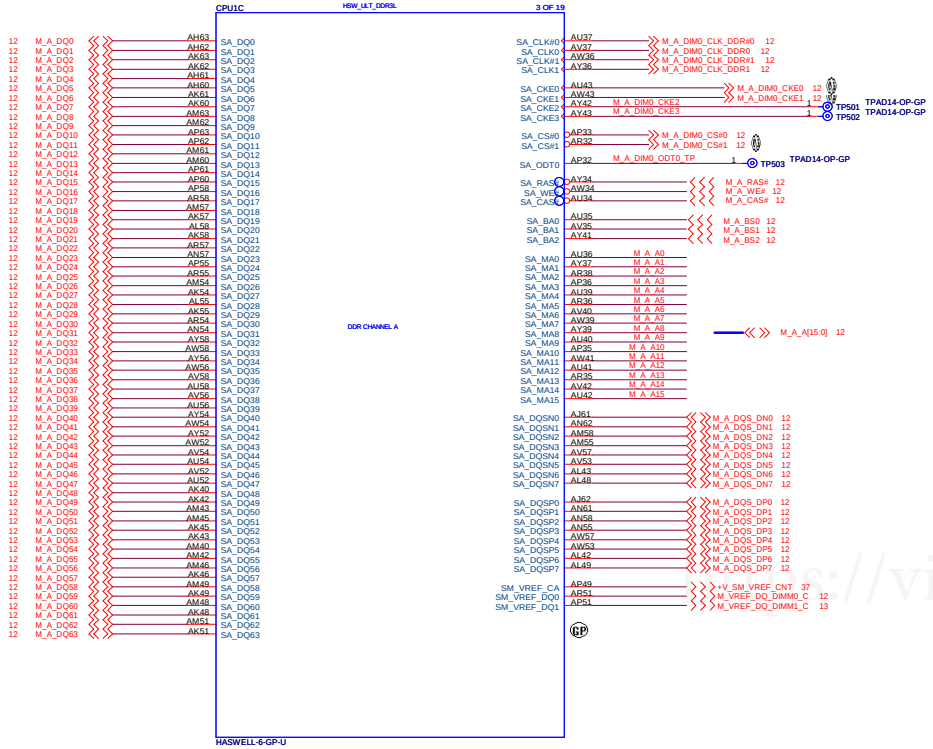
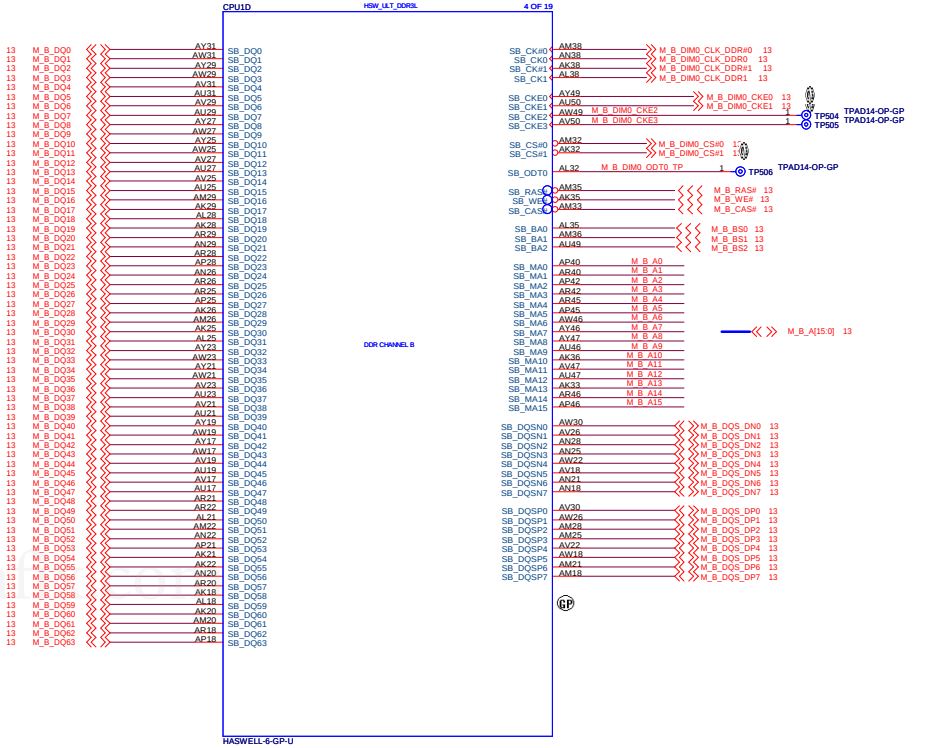
Title: CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
A3	LF15V	-1

Date: Thursday, October 30, 2014 Sheet 4 of 102

SSID = CPU





BOM1

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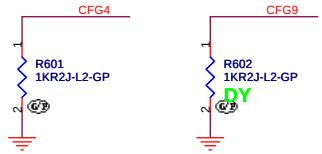
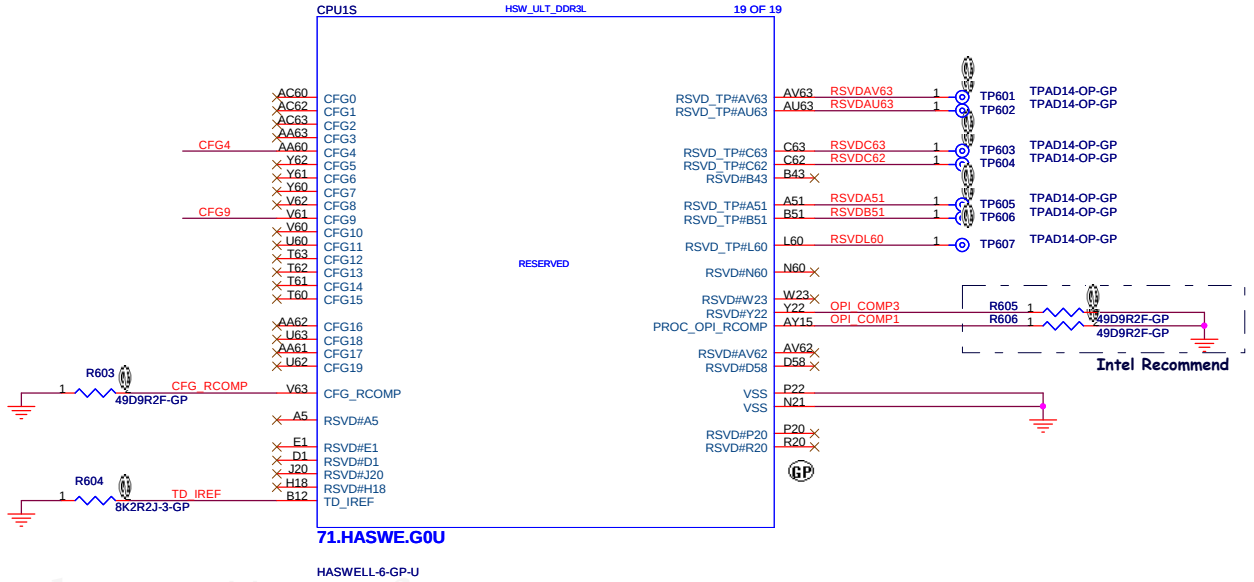
Title	***CPU (DDR)***	
Size A2	Document Number **LF15V**	Rev **-1**
Date: Monday, July 28, 2014	Sheet 5 of 102	

SSID = CPU

eDP Enable	
CFG4	1:Disable 0:Enable





Signal Name	Description	Direction/ Buffer Type
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. • **CFG[3:0]:** Reserved configuration lane. A test point may be placed on the board for these lanes. • PCI Express* Static x16 Lane Numbering Reversal. — — • • **CFG[4]: eDP enable** — 1 = Disabled — 0 = Enabled • **[19:5]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	-
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	
		continued...

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7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left un-connected

BOM1

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Title: **CPU (CFG)**

Size	Document Number	Rev
Custom	LF15V	-1

Date: Thursday, October 30, 2014 Sheet 6 of 102

SSID = CPU

SA_delete R716

SA_delete R702 ; R708 ;R709

1D35V_S3 VDDQ_CPU

PG701 PG702 PG703 PG704 PG705 PG706 GAP-CLOSE-PWR

1D05V_VTT

R703 130R2F-1-GP H_CPU_SVIDDAT

R704 75R2F-2-GP VR_SVID_ALERT#

Close to CPU

VDDQ_CPU VCC_CORE VCOMP_OUT

TP702 TPAD14-OP-GP

VCC_SENSE VCCIO_OUT

R705 43R2J-GP H_CPU_SVIDALRT#

46 VR_SVID_ALERT#
46 H_CPU_SVIDCLK
46 H_CPU_SVIDDAT

VCCST_PWRGD

46 H_VR_EN R711 10KR2J-L-GP H_VR_READY

17,26,36,46 IMVP_PWRGD R712 0R0402-PAD PWR_DEBUG

1D05V_VTT

R717 10KR2J-L-GP DY IMVP_PWRGD

R710 10KR2J-L-GP DY VCCST_PWRGD

Follow Intel CRB

1D05V_VTT

R706 150R2F-4-L-GP PWR_DEBUG

VCC_CORE

R701 100R2F-L1-GP-U

46 VCC_SENSE

R901 close to CPU

RN702

36,37,46,48 1.05VTT_PWRGD VCCST_PWRGD

SRN10KJ-4-GP

1D05V_VTT

C703 SC22U6D3V5MX-1-GP DY C715 SC1U6D3V2KX-1-GP

SA
C703,C715放置AC22 AE22 AE23

CPU1L HSW_ULT_DDR3L 12 OF 19

L59	RSVD#L59	VCC	C36
J58	RSVD#J58	VCC	C40
		VCC	C44
AH26	VDDQ	VCC	C48
AJ31	VDDQ	VCC	C52
AJ33	VDDQ	VCC	C56
AJ37	VDDQ	VCC	E23
AN33	VDDQ	VCC	E25
AP43	VDDQ	VCC	E27
AR48	VDDQ	VCC	E29
AY35	VDDQ	VCC	E31
AY40	VDDQ	VCC	E33
AY44	VDDQ	VCC	E35
AY50	VDDQ	VCC	E37
		VCC	E39
F59	VCC	VCC	E41
N58	RSVD#N58	VCC	E43
AC58	RSVD#AC58	VCC	E45
		VCC	E47
E63	VCC_SENSE	VCC	E49
AB23	RSVD#AB23	VCC	E51
A59	VCCIO_OUT	VCC	E53
E20	VCCIOA_OUT	VCC	E55
AD23	RSVD#AD23	VCC	E57
AA23	RSVD#AA23	VCC	F24
AE59	RSVD#AE59	VCC	F28
		VCC	F32
L62	VIDALERT#	VCC	F36
N63	VIDSCLK	VCC	F40
L63	VIDSOUT	VCC	F44
B59	VCCST_PWRGD	VCC	F48
F60	VR_EN	VCC	F52
C59	VR_READY	VCC	F56
		VCC	G23
D63	VSS	VCC	G25
H59	PWR_DEBUG#	VCC	G27
P62	VSS	VCC	G29
P60	RSVD_TP#P60	VCC	G31
P61	RSVD_TP#P61	VCC	G33
N59	RSVD_TP#N59	VCC	G35
N61	RSVD_TP#N61	VCC	G37
T59	RSVD#T59	VCC	G39
AD60	RSVD#AD60	VCC	G41
AD59	RSVD#AD59	VCC	G43
AA59	RSVD#AA59	VCC	G45
AE60	RSVD#AE60	VCC	G47
AC59	RSVD#AC59	VCC	G49
AG58	RSVD#AG58	VCC	G51
U59	RSVD#U59	VCC	G53
V59	RSVD#V59	VCC	G55
		VCC	G57
AC22	VCCST	VCC	H23
AE22	VCCST	VCC	J23
AE23	VCCST	VCC	K23
		VCC	K57
AB57	VCC	VCC	L22
AD57	VCC	VCC	M23
AG57	VCC	VCC	M57
C24	VCC	VCC	P57
C28	VCC	VCC	U57
C32	VCC	VCC	W57

HSW ULT POWER

HASWELL-6-GP-U

71.HASWE.G0U

BOM1

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Title: CPU (VCC_CORE)

Size: A3 | Document Number: LF15V | Rev: -1

Date: Monday, July 28, 2014 | Sheet 7 of 102

SSID = CPU

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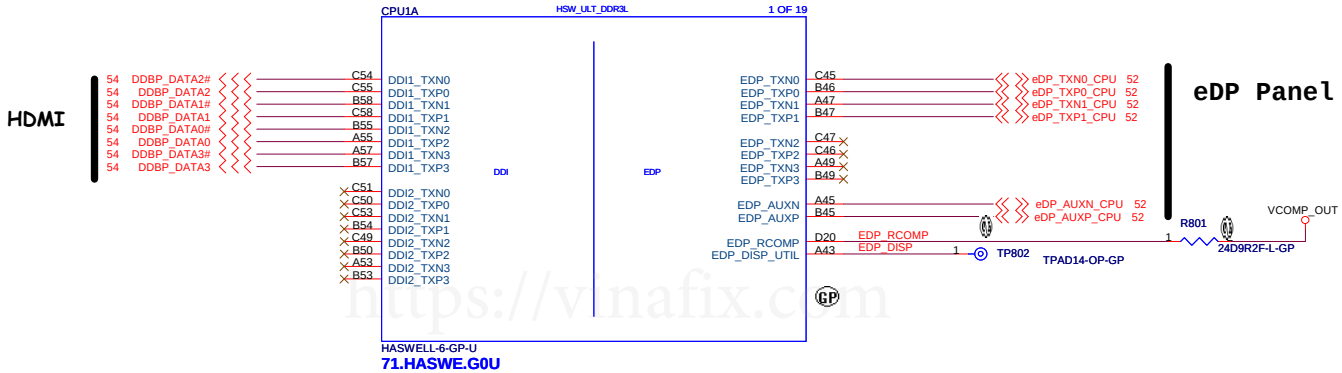

BOM1

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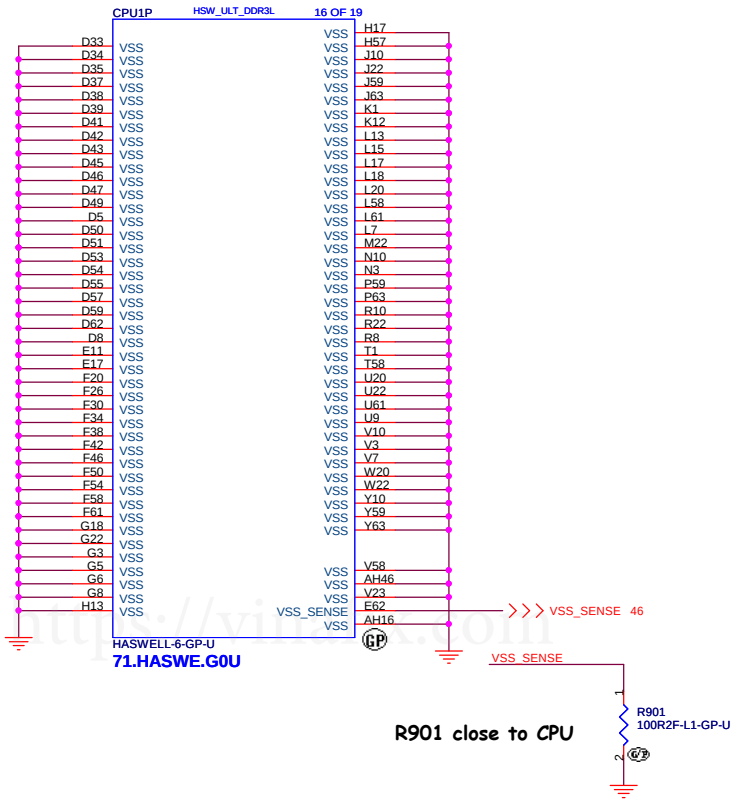
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDI/EDP)

Size	Document Number	Rev
Custom	LF15V	-1

Date: Thursday, October 30, 2014 Sheet 8 of 102

SSID = CPU



BOM1

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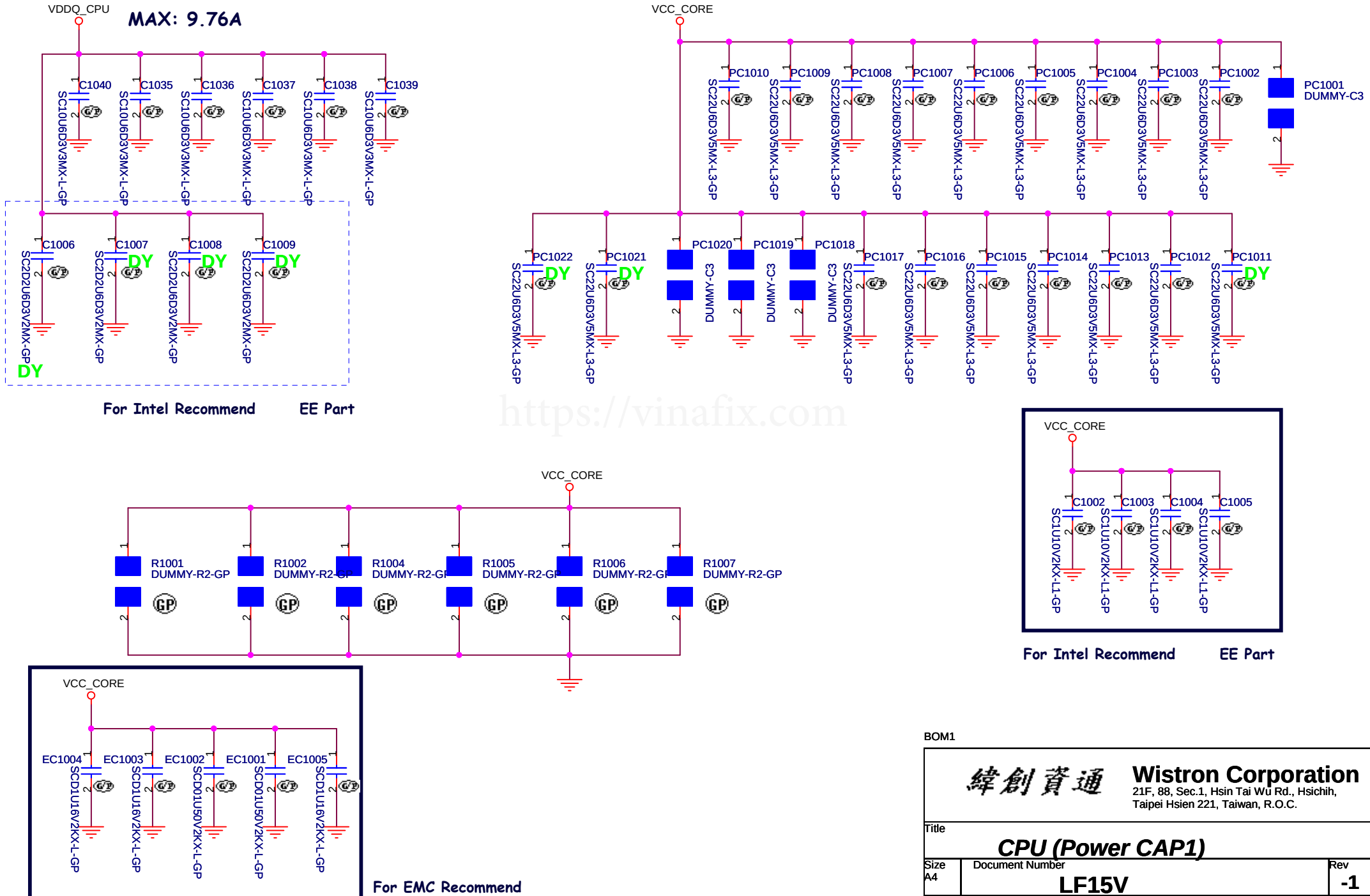
Title: CPU (VSS)		
Size: A3	Document Number: LF15V	Rev: -1
Date: Monday, July 28, 2014	Sheet 9 of 102	



BOM1

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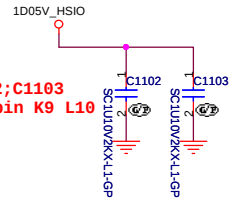
Title

CPU (Power CAP1)

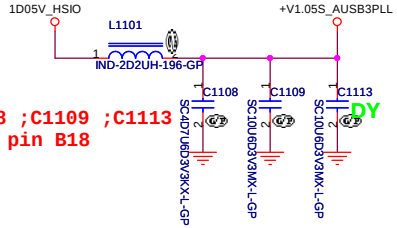
Size	Document Number	Rev
A4	LF15V	-1

Date: Thursday, October 30, 2014 Sheet 10 of 102

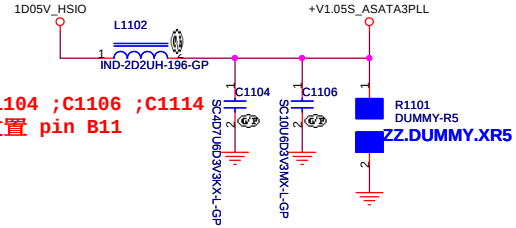
MAX: 1.92A



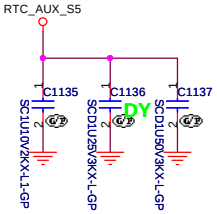
C1102;C1103
放置pin K9 L10

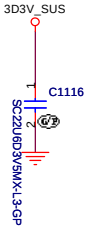


C1108 ;C1109 ;C1113
放置 pin B18



C1104 ;C1106 ;C1114
放置 pin B11

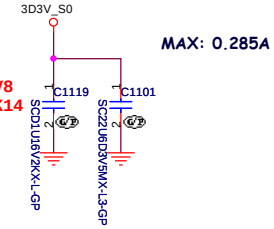




C1116放置 pin AC9

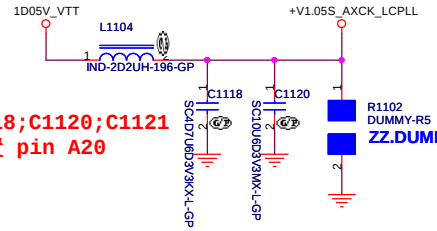
C1135;C1136;C1137
放置 pin AG10

MAX: 3.51A

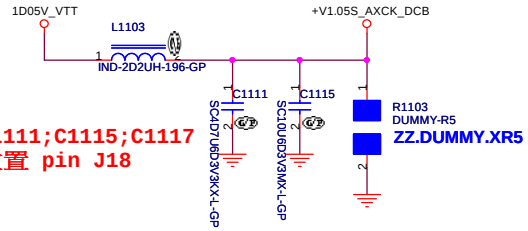


MAX: 0.285A

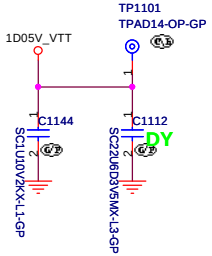
C1101 放置 pin V8
C1119 放置 pin K14



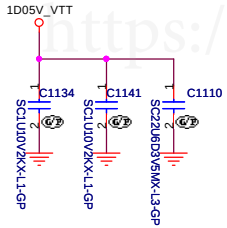
C1118;C1120;C1121
放置 pin A20



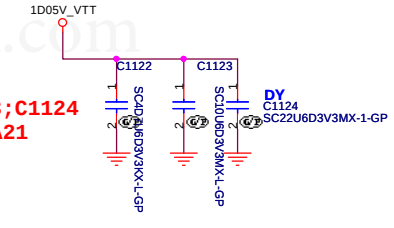
C1111;C1115;C1117
放置 pin J18



C1144;C1112
放置 pin AE9



C1110 放置 pin J11
C1134 C1141 放置 pin J11, AE8



C1122;C1123;C1124
放置 pin AA21

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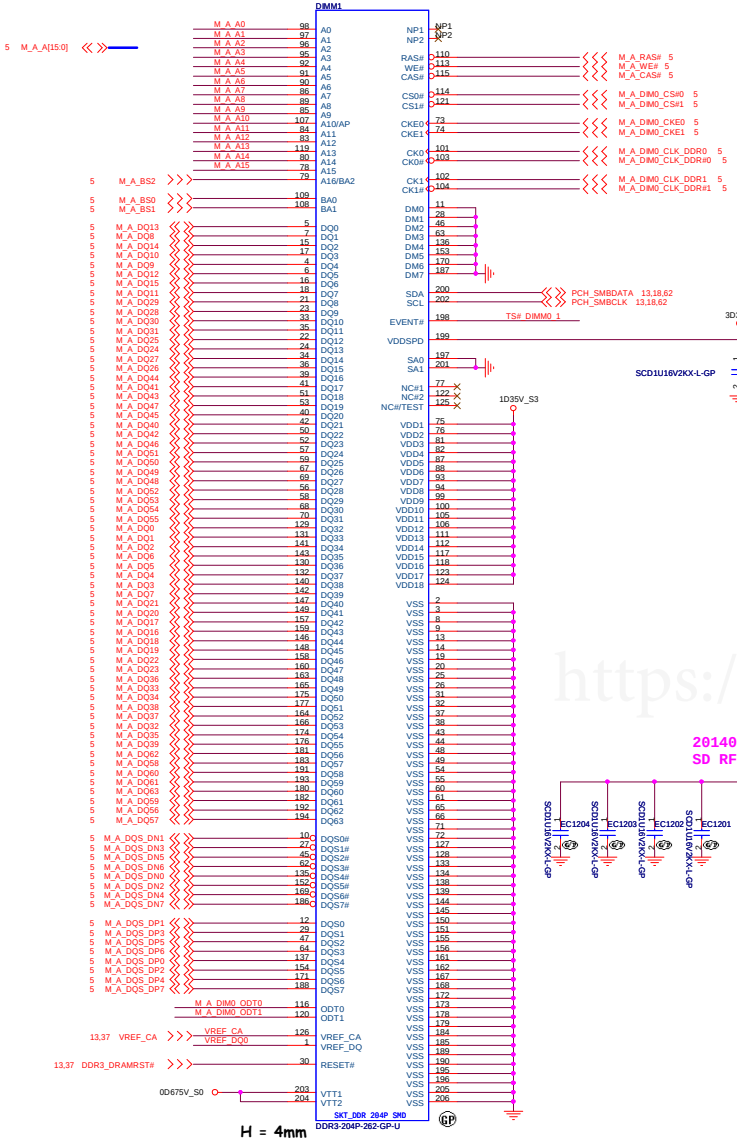
Title: CPU (Power CAP2)

Size: Custom | Document Number: LF15V | Rev: -1

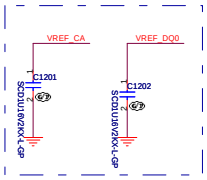
Date: Thursday, October 30, 2014 | Sheet 11 of 102

SSID = MEMORY



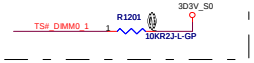
H = 4mm

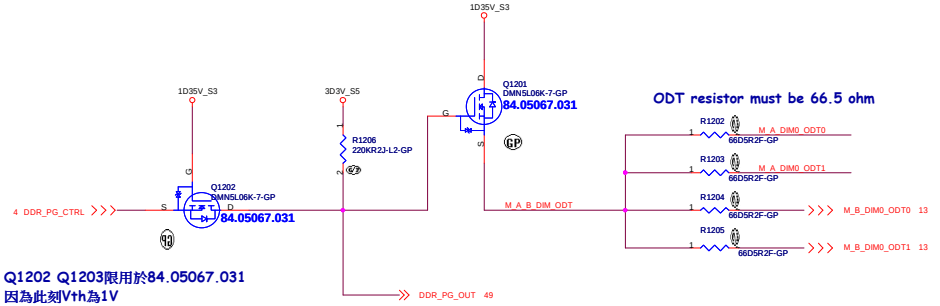
62.10024.S21



Close RAM1 CA & DQ pin

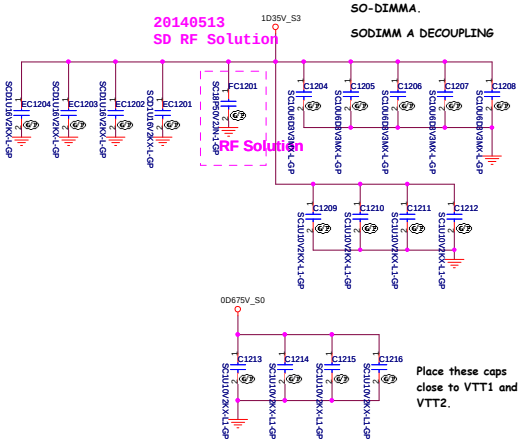
Thermal EVENT





Q1202 Q1203限用於84.05067.031
因為此刻Vth為1V

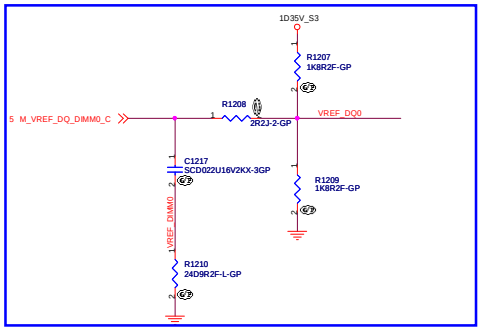
20140513
SD RF Solution



Layout Note:
Place these Caps near SO-DIMMA.

SODIMM A DECOUPLING

Place these caps close to VTT1 and VTT2.



For Intel Recommend Close to DIMM

BOM1

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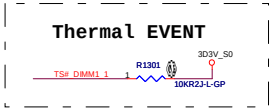
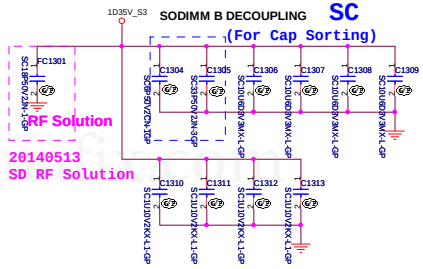
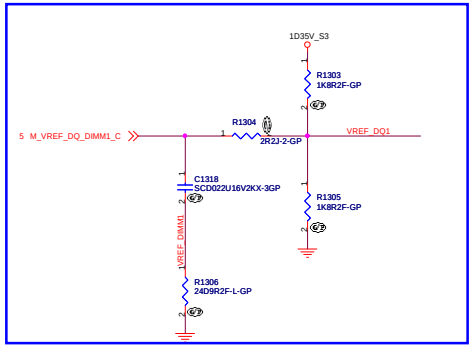
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DDR3L-SODIMM1		
Size: A2	Document Number: LF15V	Rev: -1
Date: Thursday, October 30, 2014	Sheet 12 of 102	

SSID = MEMORY

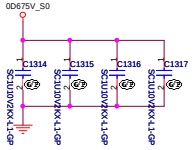


Layout Note:
Place these Caps near
SO-DIMMB.

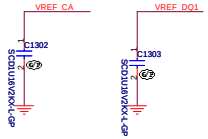




For Intel Recommend Close to DIMM



Place these caps
close to VTT1 and
VTT2.



Vinafix.com

BOM1

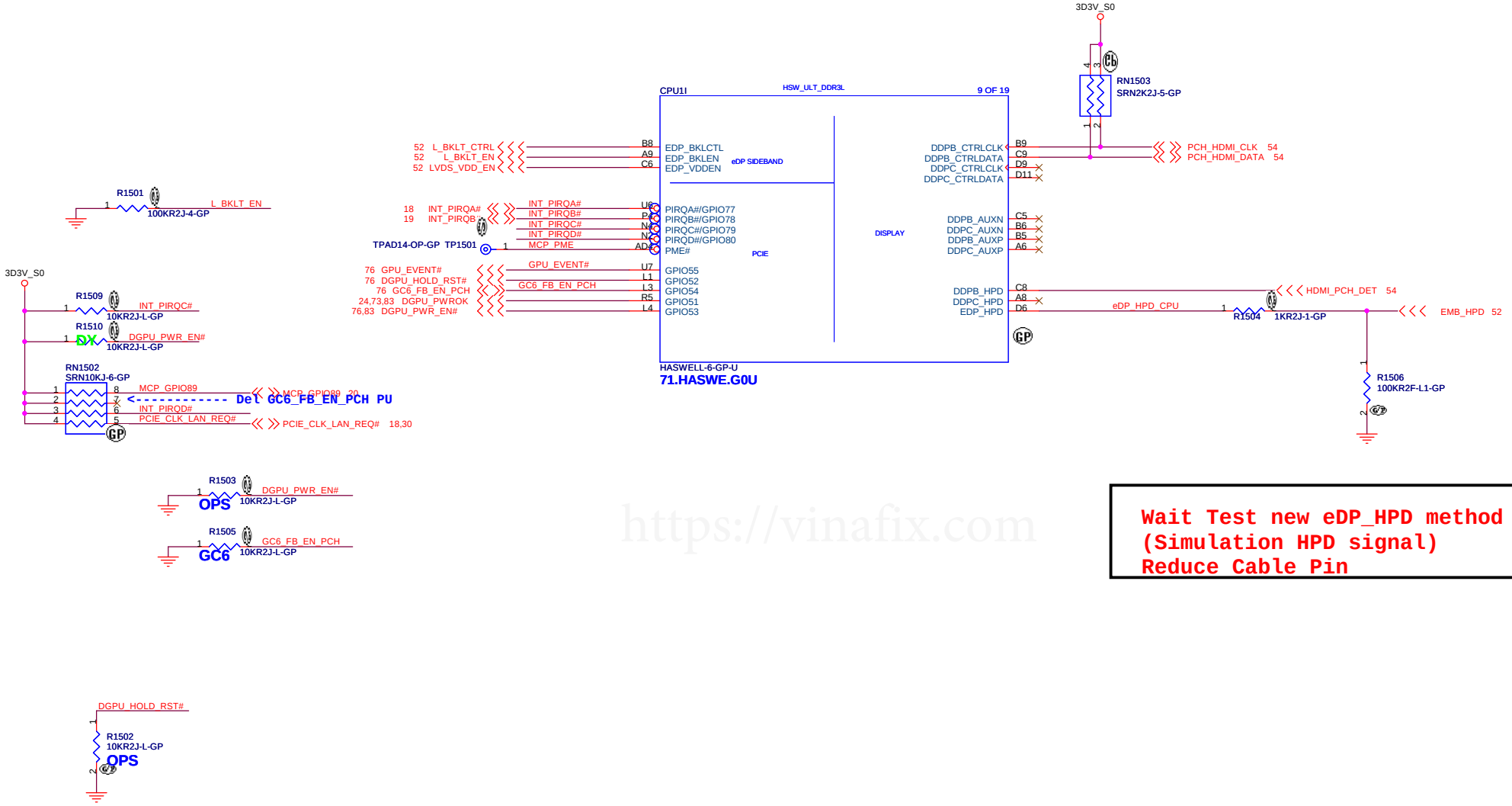
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DDR3L-SODIMM2		
Size: A2	Document Number: LF15V	Rev: -1
Date: Thursday, October 30, 2014	Sheet 13 of 102	

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)_SODIMM_SODIMM4

Size	Document Number	Rev
A4	**LF15V** Vinafix.com	-1
Date: Monday, July 14, 2014	Sheet 14 of 102	



Del GC6_FB_EN_PCH PU

Wait Test new eDP_HPD method
(Simulation HPD signal)
Reduce Cable Pin

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(EDP SIDEBAND/GPIO/DDI)

Size	Document Number	Rev
A3	LF15V	-1

Date: Thursday, October 30, 2014 Sheet 15 of 102

SSID = PCH

USB2.0 Table

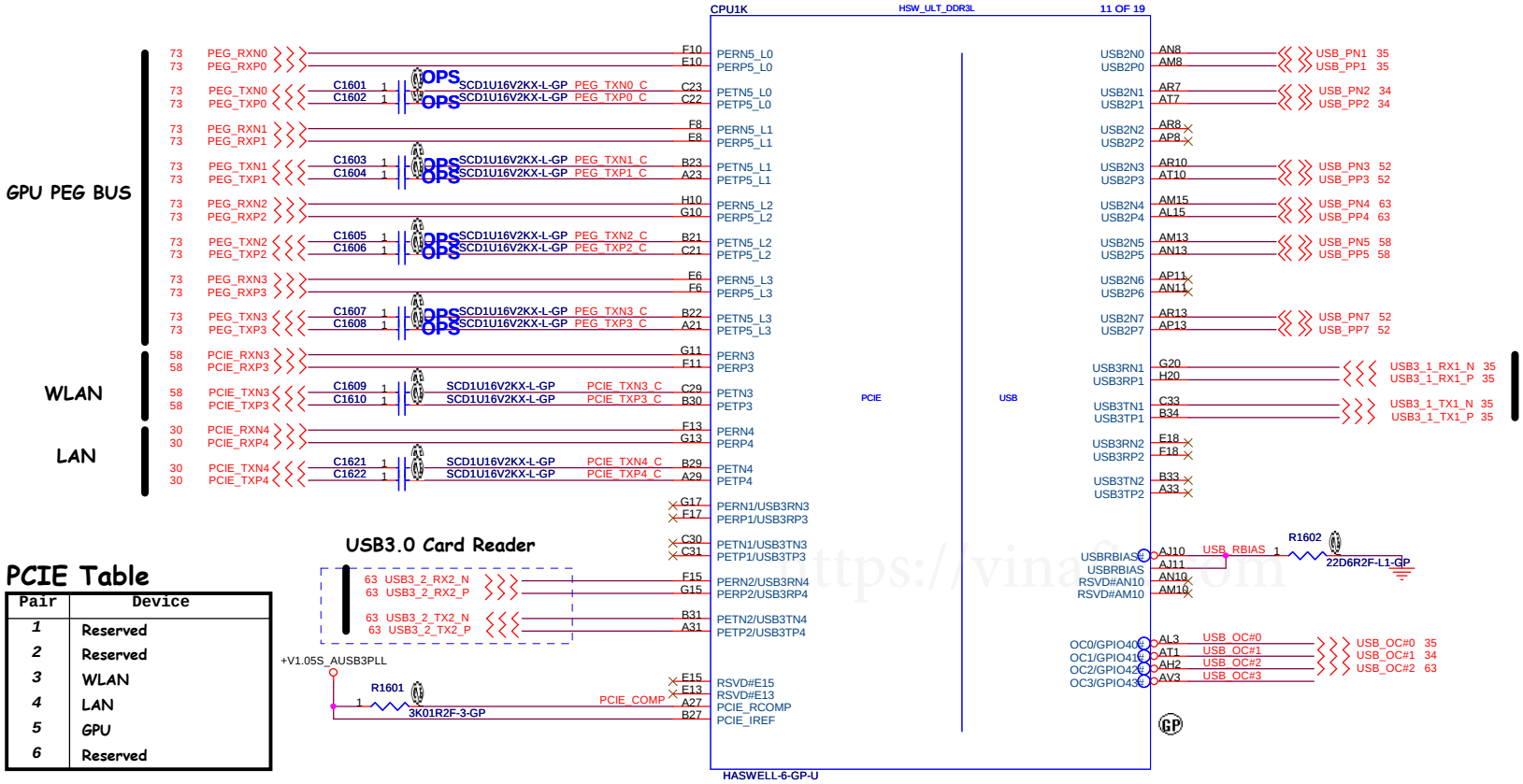
Pair	Device
0	USB3.0 Port 1 (USB_OC#0)
1	USB2.0 Port 2 (with Debug Function) (USB_OC#1)
2	NC
3	Camera
4	USB2.0 Port 4 (USB_OC#2)
5	WLAN(Bluetooth)
6	NC
7	Panel Touch

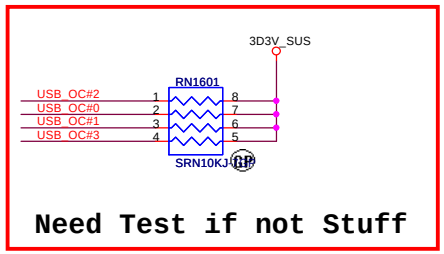
USB3.0 Table

Pair	Device
1	USB3.0 Charger Port 1
2	Reserved
3	Reserved
4	USB3.0 Card Reader Port 2

PCIE Table

Pair	Device
1	Reserved
2	Reserved
3	WLAN
4	LAN
5	GPU
6	Reserved





BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCI/USB)

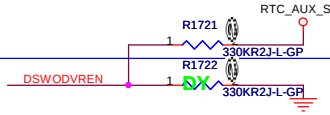
Size	Document Number	Rev
A3	LF15V	-1

Date: Thursday, October 30, 2014 Sheet 16 of 102

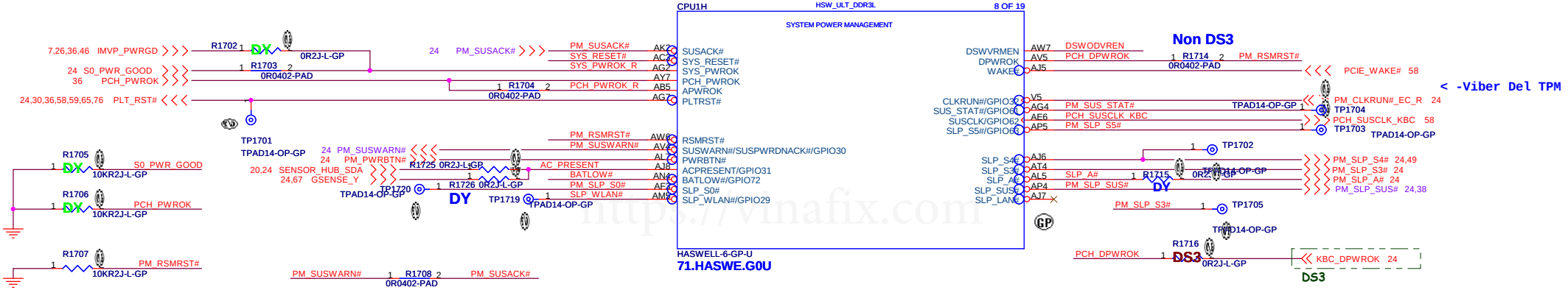
SSID = PCH

Bit	Description
31:3	Reserved
2	**WAKE# Pin Deep Sx Enable (WAKE_PIN__DSX_EN)** - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case). When this bit is '0': • Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. • Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled. **NOTE:** Deep Sx disabled configuration must leave this bit at '0'.

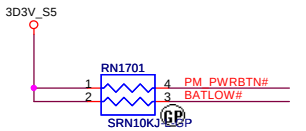
DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

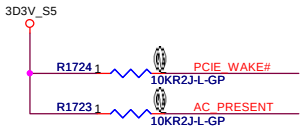


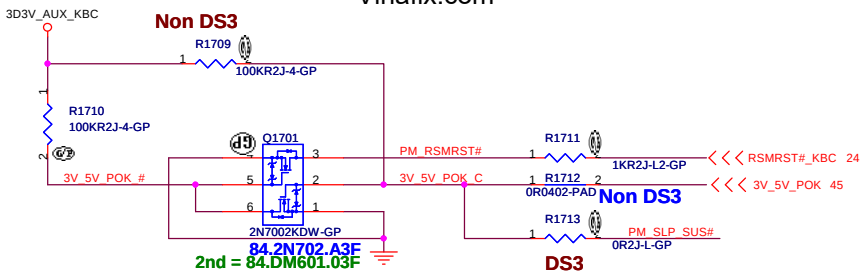
Follow Intel CRB

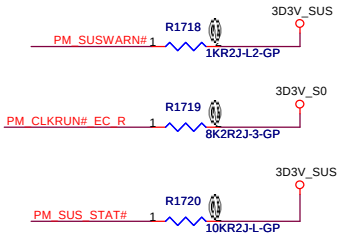


Vinafix.com









BOM1

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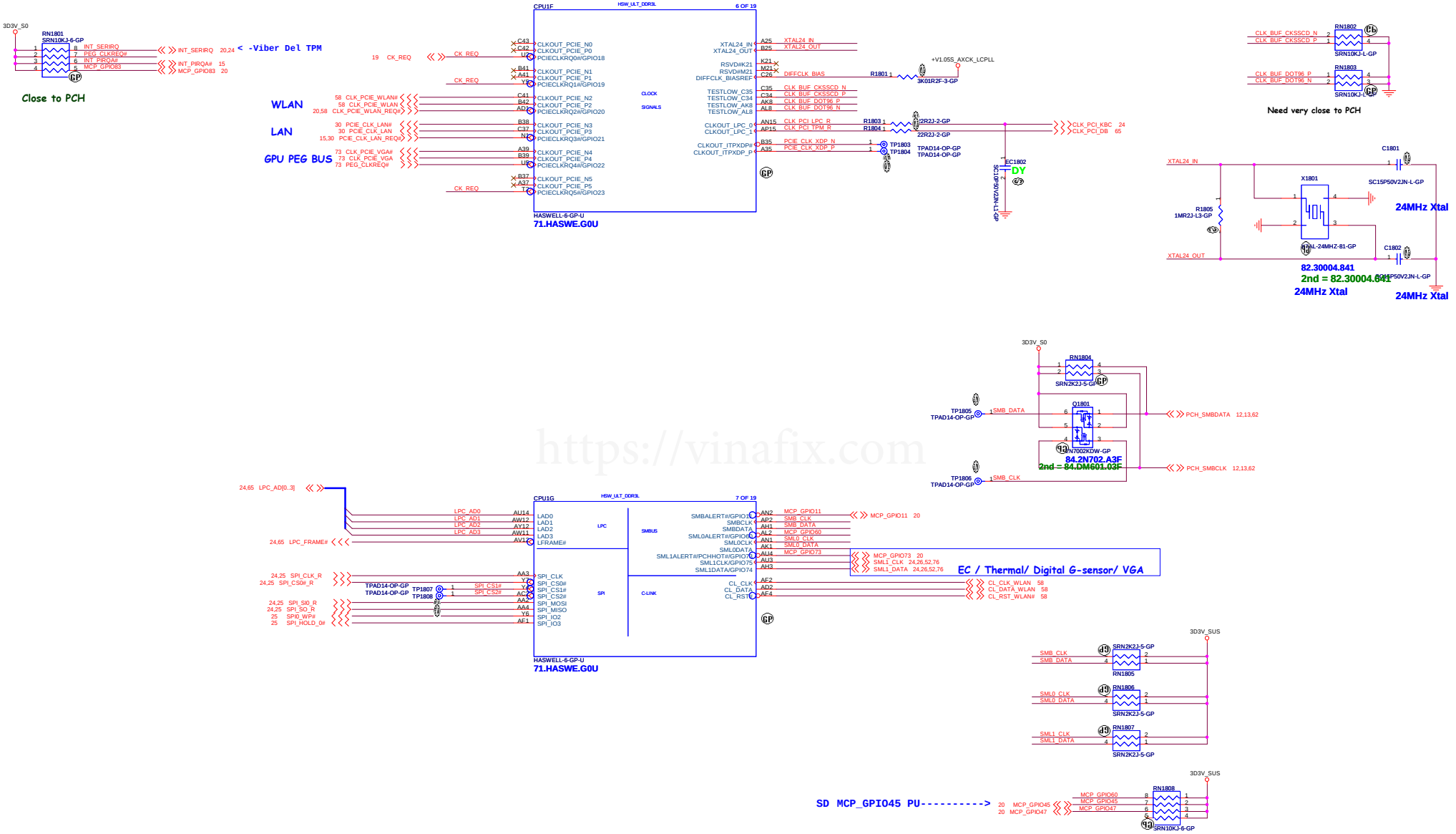
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (DMI/FDI/PM)**

Size	Document Number	Rev
A3	LF15V	-1

Date: Thursday, October 30, 2014 Sheet 17 of 102

SSID = PCH



BOM1

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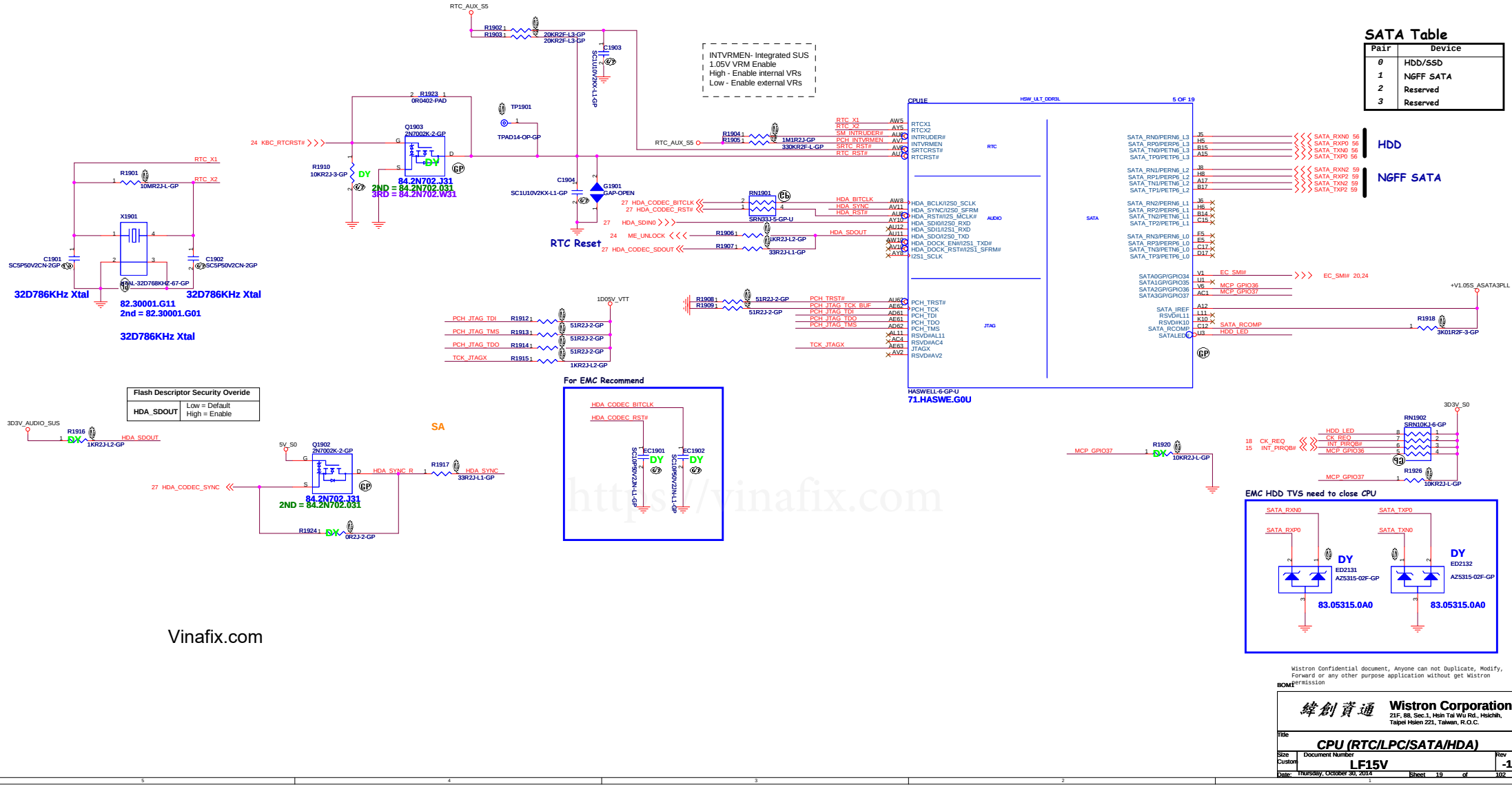
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCI-E/SMBUS/CLOCK/CL)

Size	Document Number	Rev
A2	LF15V	-1

Date: Thursday, October 30, 2014 Sheet 18 of 102

SSID = PCH



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BOM1

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Title: CPU (RTC/LPC/SATA/HDA)

Size: Custom | Document Number: LF15V | Rev: -1

Date: Thursday, October 30, 2014 | Sheet 19 of 102

Thermal

SSID = PCH

Thermal
NCT7718: 1
Thermal VD : 0

NCT7718&TV

SKU	Fun./Location	7718/TV
SKU1,2	R2037	ASM
SKU3	R2036	ASM

SB

CPU1J — HSW_ULT_DDR3L — 10 OF 19 — HASWELL-6-GP-U — 71.HASWE.G0U

Viber Del ODD----------->

<----------Viber Del ODD

<---Viber NGFF SATA

Viber NGFF SATA--->

<-----Default:Low

< -Viber Del TPM

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

	GSPIO_MOSI_BBS0_R(SSD_PWR)
PU	RESERVED
PD	SPI BUS

DGPU_PRSNT#
UMA: 1
Optimus(Muxless) : 0

UMA&OPS

SKU	Fun./Location	UMA/DIS
SKU1	R2013	ASM
SKU2~5	R2014	ASM

BOM1

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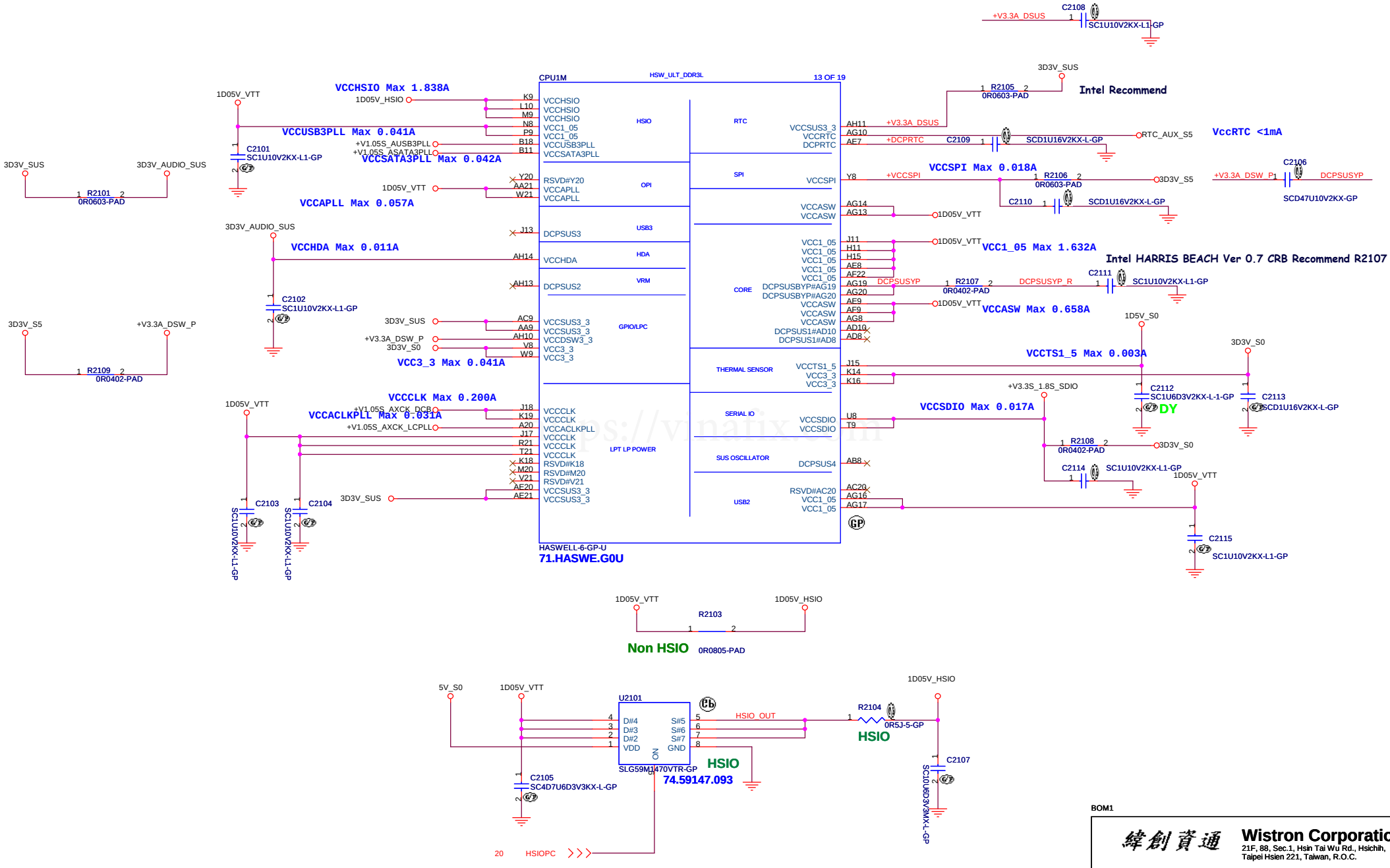
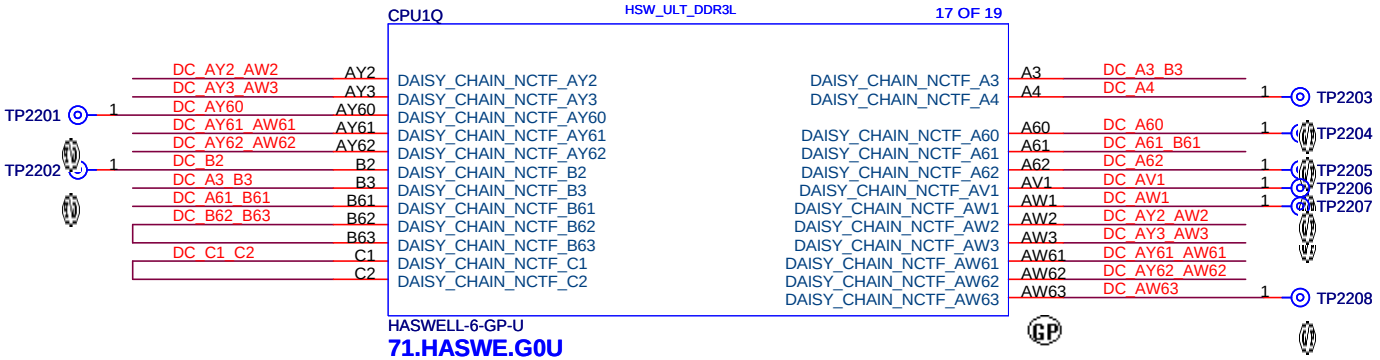
Taipei Hsien 221, Taiwan, R.O.C.

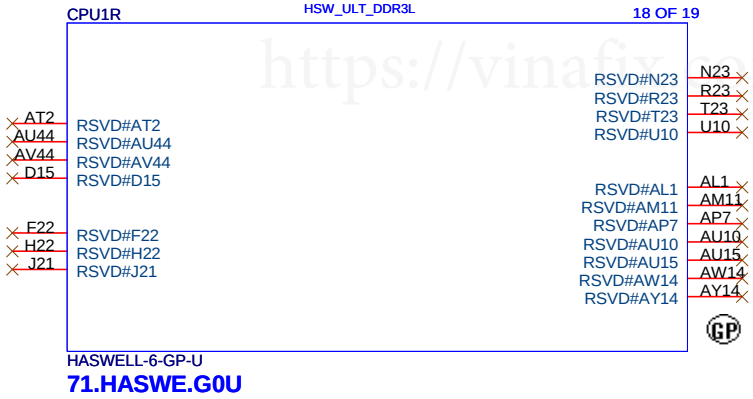
Title: CPU (GPIO/MISC)
Size: Custom | Document Number: LF15V | Rev: -1
Date: Thursday, October 30, 2014 | Sheet 20 of 102



BOM1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CPU (POWER1)**	
Size A3	Document Number **LF15V**	Rev **-1**
Date: Thursday, October 30, 2014	Sheet 21 of 102	





BOM1

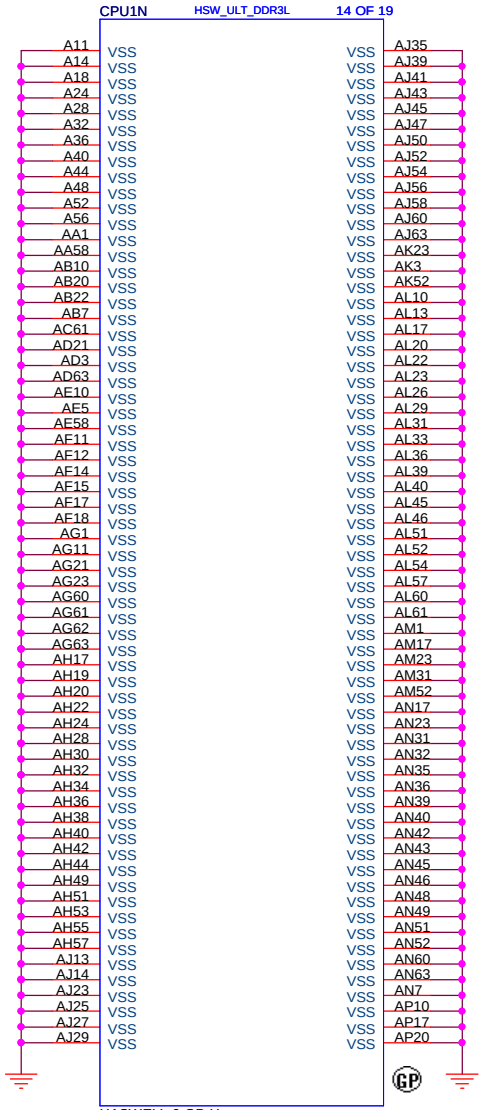
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

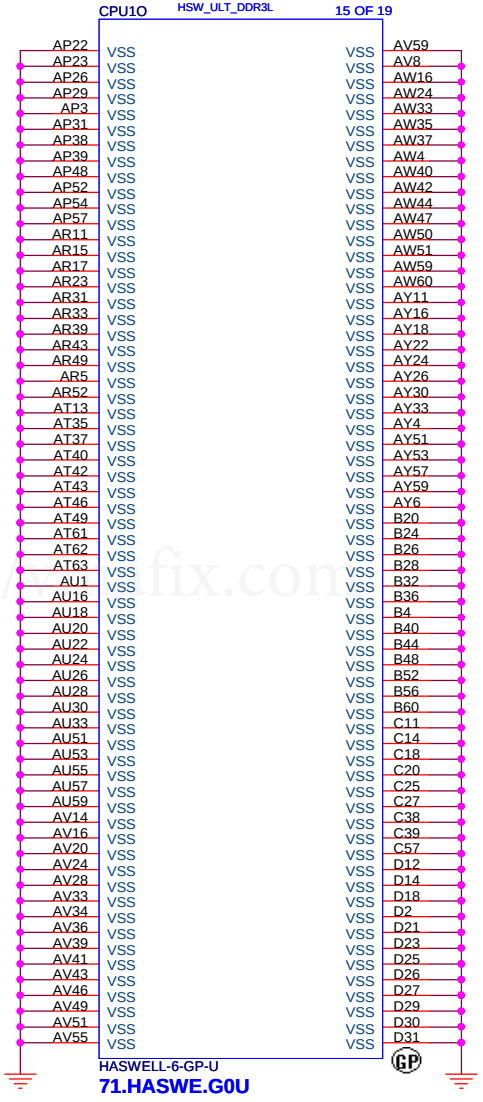
Title: ***CPU (RSVD)***

Size	Document Number	Rev
Custom	LF15V	-1

Date: Monday, July 14, 2014 Sheet 22 of 102

SSID = PCH





BOM1

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size	Document Number	Rev
Custom	LF15V	-1

Date: Monday, July 14, 2014 Sheet 23 of 102

SSID = KBC

Vinafix.com

Model_ID_BOM Ctrl

MODEL ID

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
NA	100.0K	10.0K 64.10025.6DL	3.0V
NA	100.0K	20.0K 64.20025.1.0L	2.75V
LF15V Intel Broadwell	100.0K	33.0K 64.33025.1.0L	2.48V
NA	100.0K	47.0K 64.47025.6DL	2.24V
NA	100.0K	64.9K 64.64925.6DL	2.0V
NA	100.0K	76.8K 64.76825.6DL	1.87V
LF15V Intel Haswell	100.0K	215.0K 64.21535.6DL	1.048V

PCB VERSION

SVT

BOM Ctrl_VER

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
-1	100.0K	64.9K	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

SPEC: ADT PWR Detection Function V1 3

DELTA Model:ADP65FD BB-PD03 ADP

PIN 3 PIN 1 PIN 2

TABLE	
PIN 1	SIGNAL
PIN 3	287~ohm(1% TOLERANCE)
PIN 2	

ADP internal Resis 287ohm
3.3*287/1037=0.91V (65W)

45W_65W#
High: 45W / Low 65W
DISCRETE#
High: UMA / Low: Discrete

AC Adapter	ADT_TYPE	System Power Limit
130W	1.663V < ID <= 2.102V	90W
90W	1.172V < ID <= 1.618V	90W
SA 65W	0.693V < ID <= 1.134V	65W
45W	0.214V < ID <= 0.663V	45W

Prevent BIOS data loss solution

NPCE285G

BATTERY / CHARGER ---->
PCH / GPU N15S / Gsensor /NCT7718

SD
Reserved Vol_down PU

TP----> SB

SD Add Vol_UP PD for DG

2014/4/28 SD
SW Max
DY R1717

Reserved AOAC

071.00285.001G

NOTE:
Please be aware that the SPI interface trace length between PCH and EC should not exceed 650mils. The mismatch of SPI interface signals between EC and SPI flash should not exceed 500mils.

NOTE:
Locate resistors R2415 and R2417 close to the U2481.

<---- Viber Del DOCK and reserved PU

<---- Viber Del TPM

KBC PWR supply at PSL mode.

NOVO button Fun define: one key to recover OS.

NOVO button wake KBC at PSL mode.		
KBC_NOVO_BTN#	KBC_PWRBTN_EC#	
Low	Low	

KBC_PWRBTN_EC#:Low
(1) 4sec: PWR Button shut down
(2) 8sec: KBC reset

2013/9/12
GPIO83/SOUT_CR & GPIO87/SIN_CR
Need reserved TP for Debug

R2472 close to Pin103

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

NOTE:
PWM Signal:
1. If unused, select altrnative GPIO function and enable internal pull-down.
2. Please measure and make sure that the rise time of VCC_POR is less than 10us.

Nuvoton KBC PSL Power Logic

1.Enter PSL mode (Entry S5 after 10sec) :
3D3V_AUX_KBC : OFF (KBC PWR supply)
2.At PSL mode (SPEC: S5<10mW)

PSL mode(AC or DC):		
EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Hi	Low	OFF

PSL Wake(AC or DC):		
EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Low	Hi	ON

84.02130.031

84.2N702.J31

EC_GPIO47 High Active

2nd = 84.2N702.031

Test point

SC

SB

EC GPIO PH

Reserved AOAC

SD Reserved Vol_down PU

SD Add Vol_UP PU for AG

SB

EC GPIO PL

SD
Add Vol_UP PD for DG

<Core Design>

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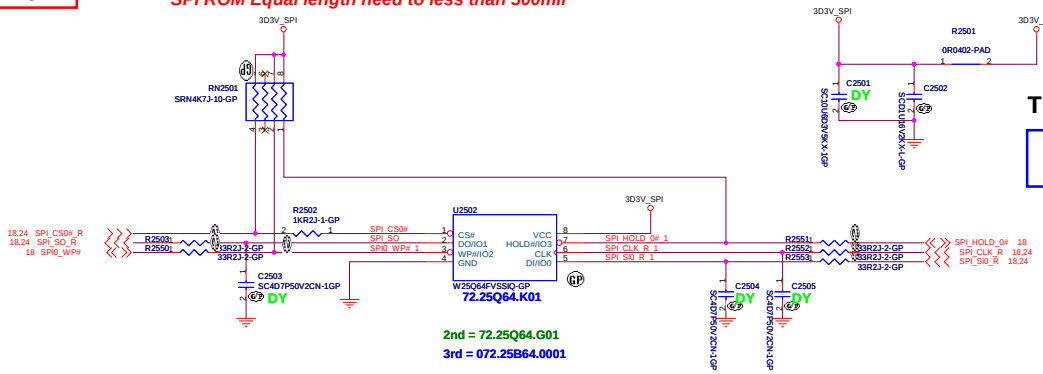
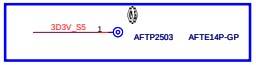
Title: KBC_NPCE985P
Size: A3 | Document Number: LF15V | Rev: -1
Date: Thursday, October 30, 2014 | Sheet 24 of 102

SSID = Flash.ROM

SPI ROM Equal length need to less than 500mil

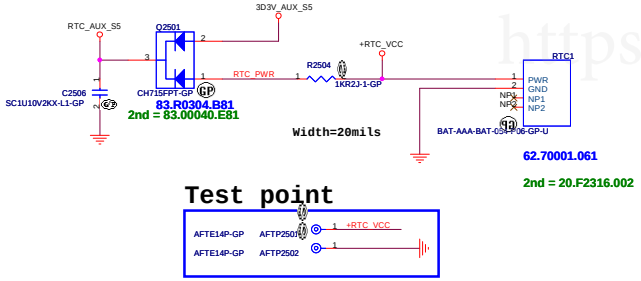


Test point



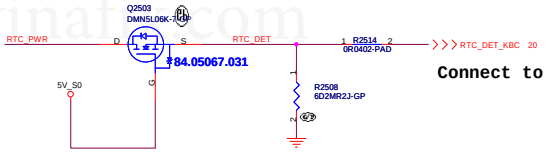
SSID = RBATT

SSID = RBATT



Test point

High Detect
Need to Check whether to PD in PCH Side



Connect to CPU GPIO57

BOM1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Flash(KBC+PCH)/RTC***

Size: A2 | Document Number: LF15V | Rev: -1

Date: Thursday, October 30, 2014 | Sheet 25 of 102

SSID = Thermal

Thermal sensor NCT 7718W

***Layout* 15 mil**

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

2.System Sensor, Put on palm rest

ALERT# /T_CRIT#
Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

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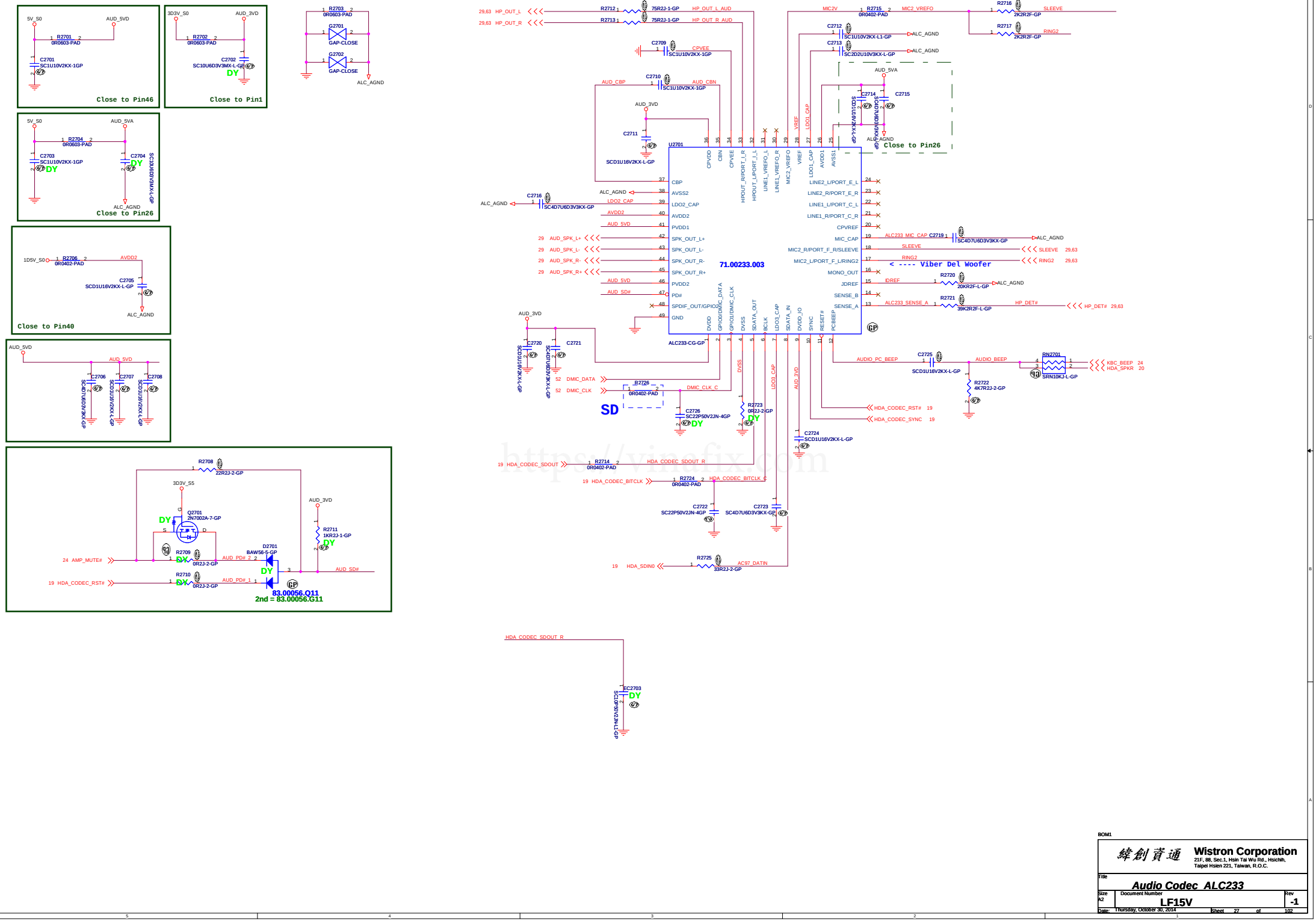
Title	Thermal 7718/Fan Controllor P2793
Size: A2	Document Number: LF15V
Rev	-1
Date: Thursday, October 30, 2014	Sheet 26 of 102


Close to Pin46
Close to Pin1
Close to Pin26
Close to Pin40
71.00233.003
< ---- Viber Del Woofer
SD
83.00056.Q11
2nd = 83.00056.G11
ALC233-CG-GP
U2701
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Audio Codec ALC233
LF15V
-1
Thursday, October 30, 2014

BOM1

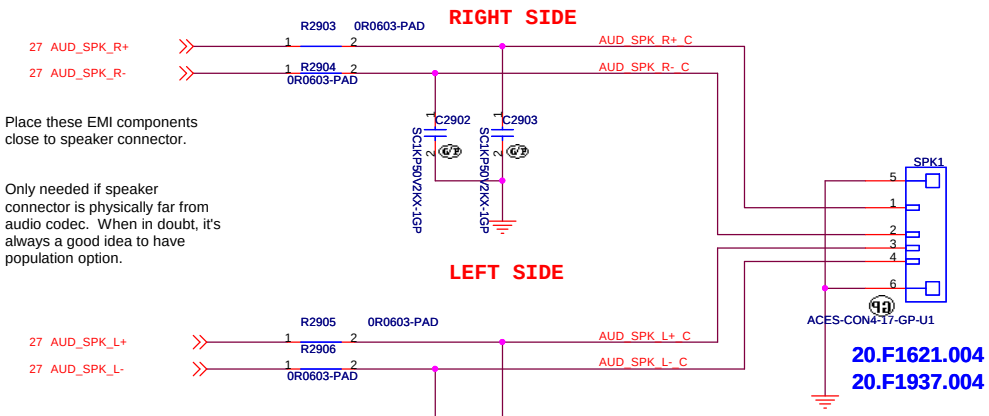
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

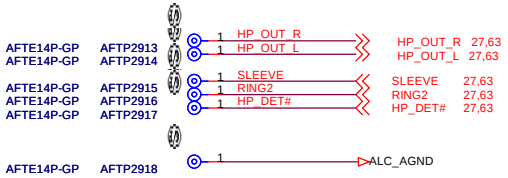
Title: ***Audio Codec ALC233(Reserved)***

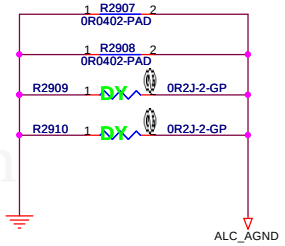
Size	Document Number	Rev
A2	LF15V	-1

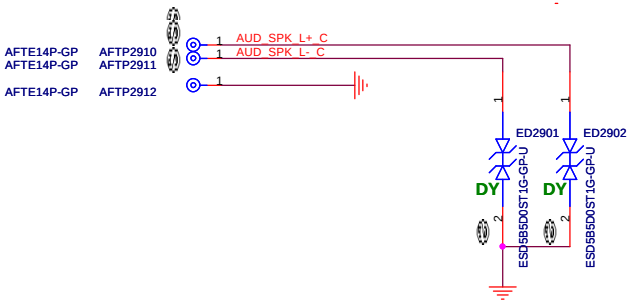
Date: Monday, July 14, 2014 Sheet 28 of 102

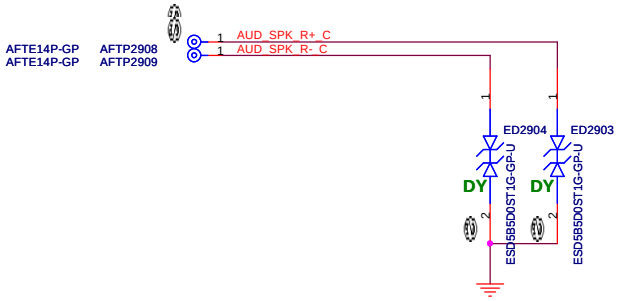
INTERNAL STEREO SPEAKERS











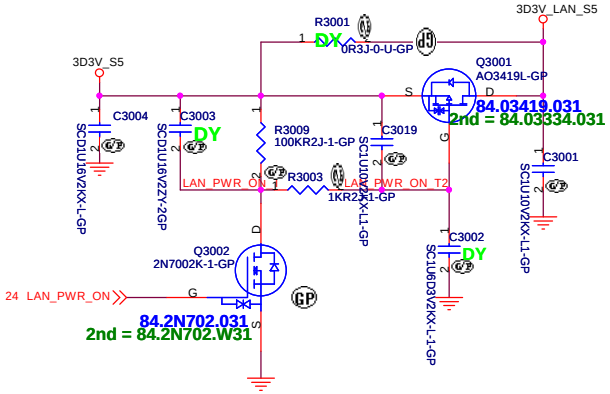
BOM1

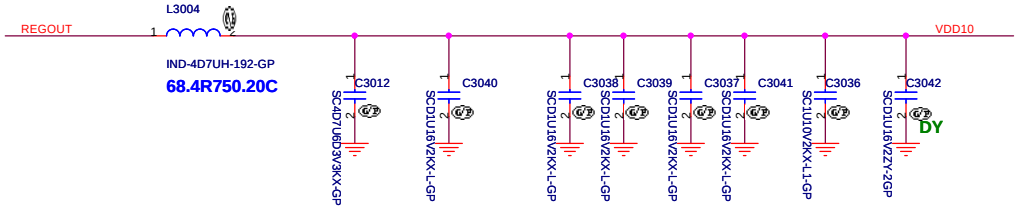
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

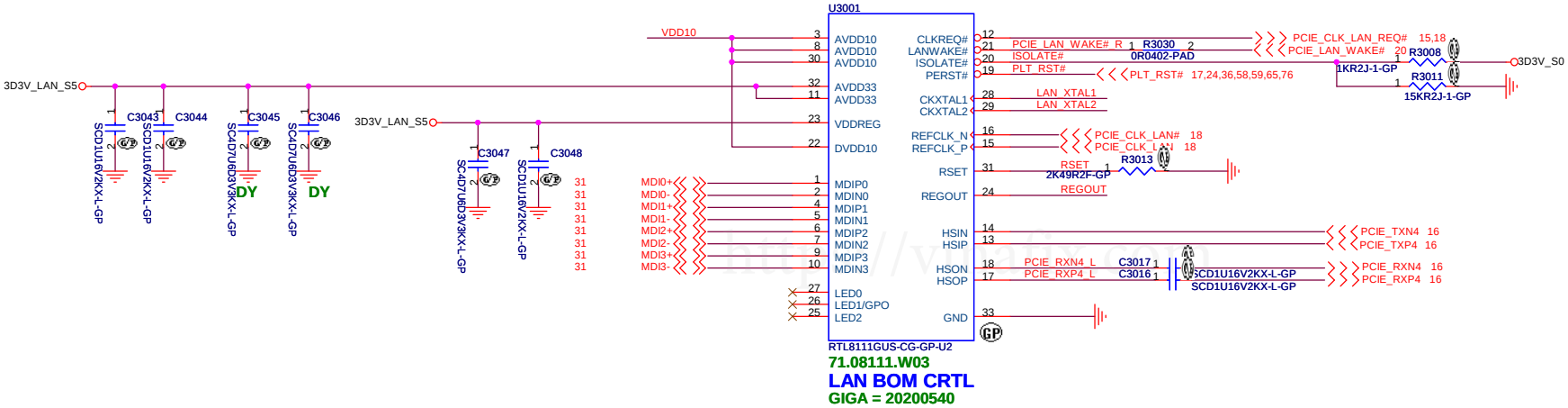
Title: **MIC/SPEAKER/AUDIO JACK**

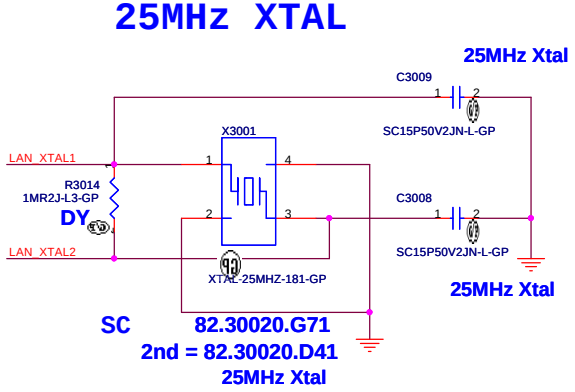
Size	Document Number	Rev
Custom	LF15V	-1

Date: Thursday, October 30, 2014 Sheet 29 of 102









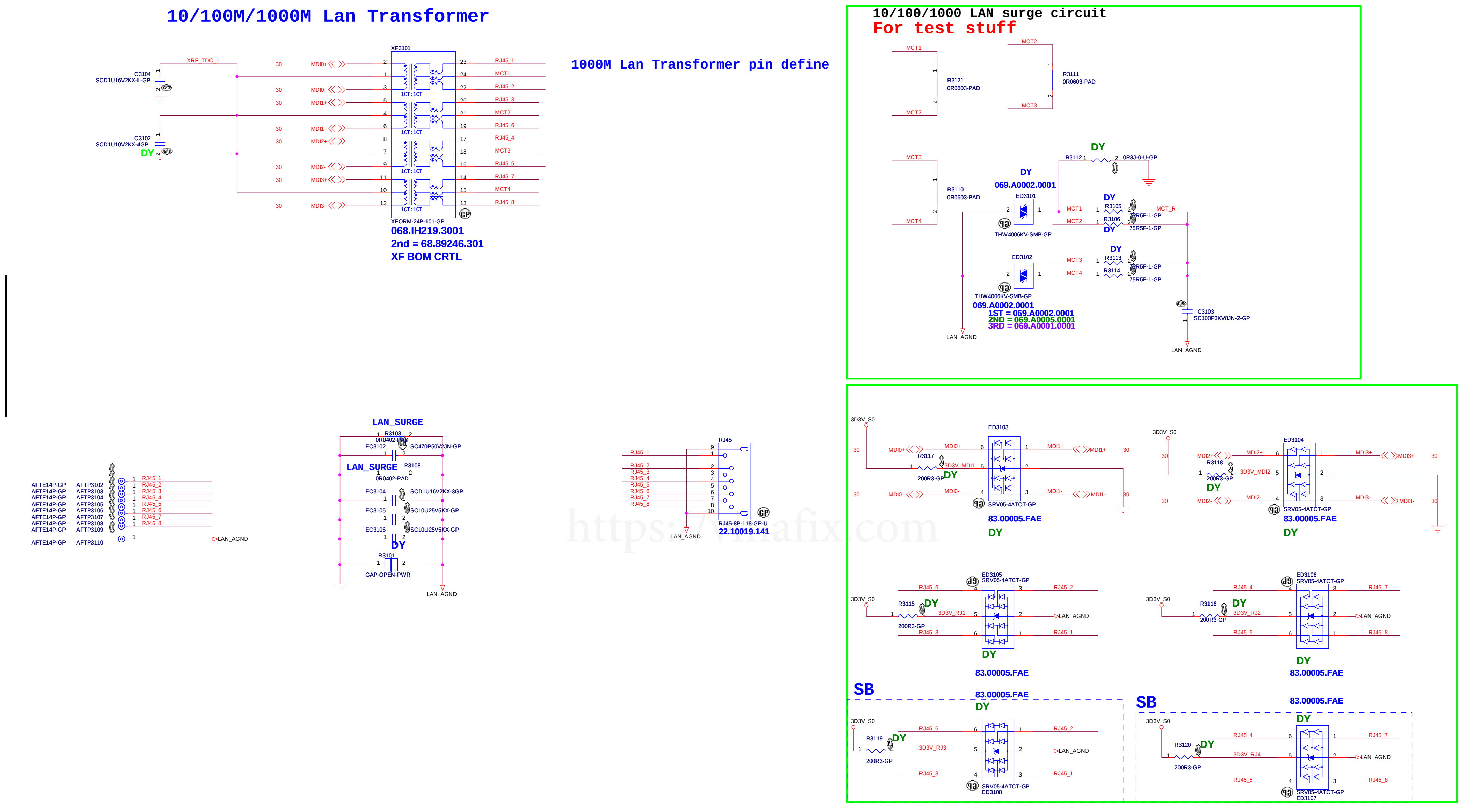
BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8111GUS RTL8106EUS

Size	Document Number	Rev
A3	LF15V	-1

Date: Thursday, October 30, 2014 Sheet 30 of 102



BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	*LAN CONNECTOR*	
Size A2	Document Number LF15V	Rev -1
Date: Thursday, October 30, 2014	Sheet 31 of 102	

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CARD READER(Reserved)

Size	Document Number	Rev
Custom	**LF15V**	**-1**

Date: Monday, July 14, 2014 Sheet 32 of 102

BOM1

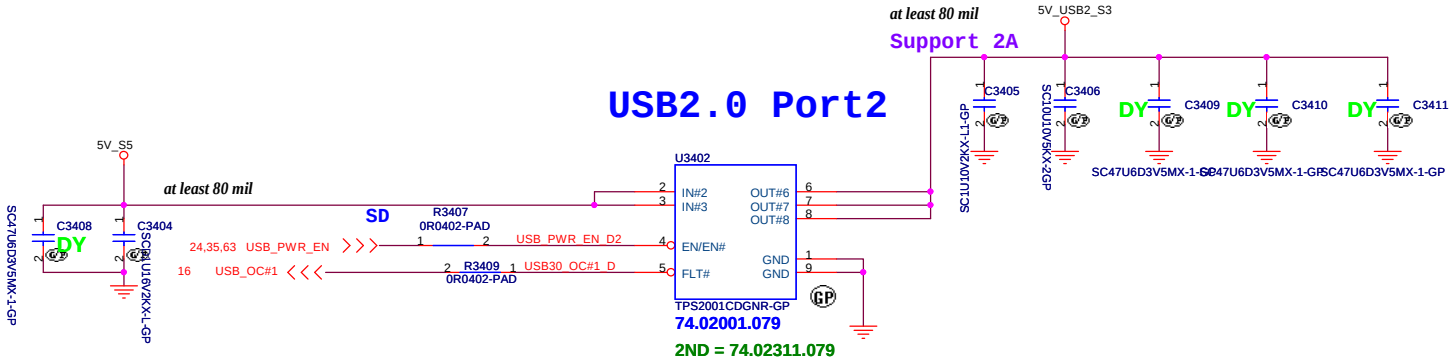
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

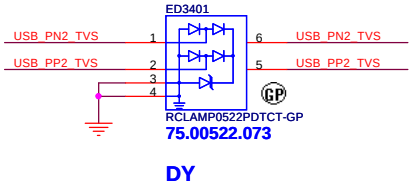
Title
CARD Reader

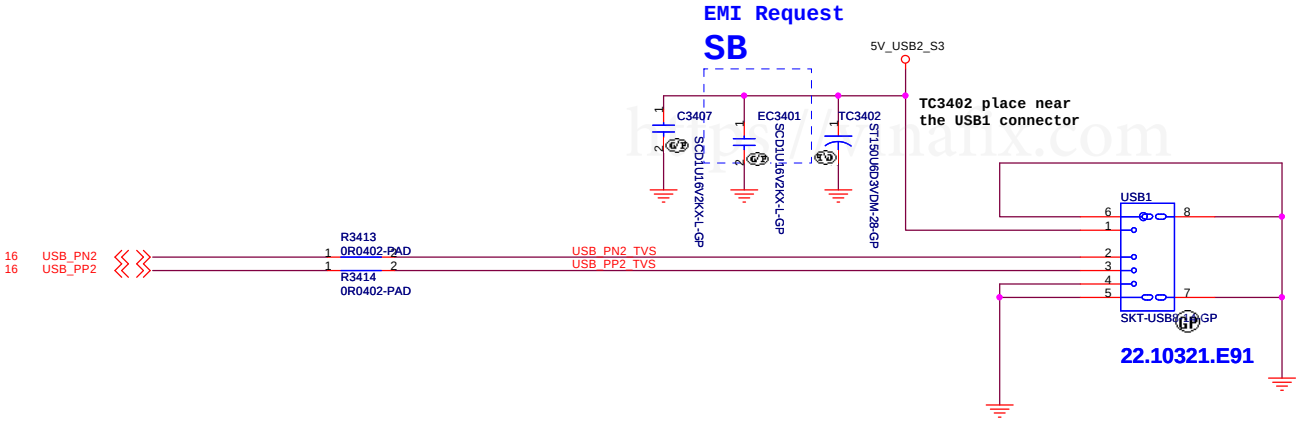
Size	Document Number	Rev
A4	**LF15V**	**-1**

Date: Monday, July 14, 2014 Sheet 33 of 102

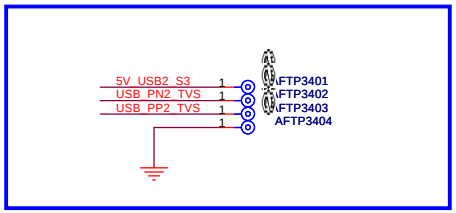
USB2.0 Port2







Test point



BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB 2.0**

Size	Document Number	Rev
A3	LF15V	-1

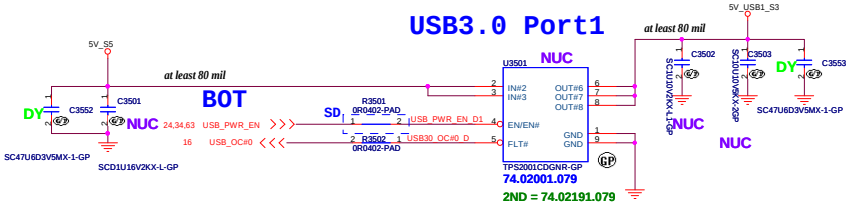
Date: Thursday, October 30, 2014 Sheet 34 of 102

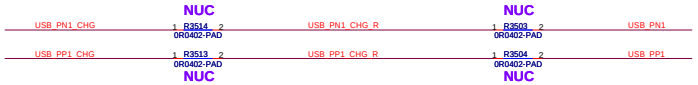
SB UC, UC_ST, DY_UC_TI不上件

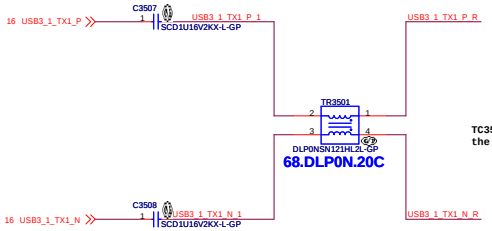
USB charger

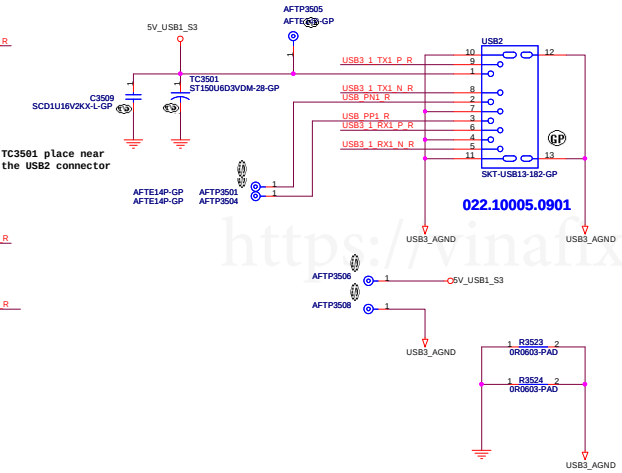
USB3.0 Port1

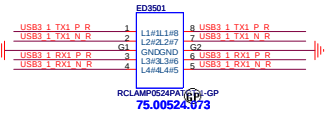
Support 2A

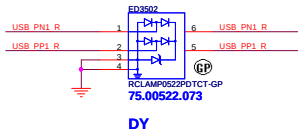






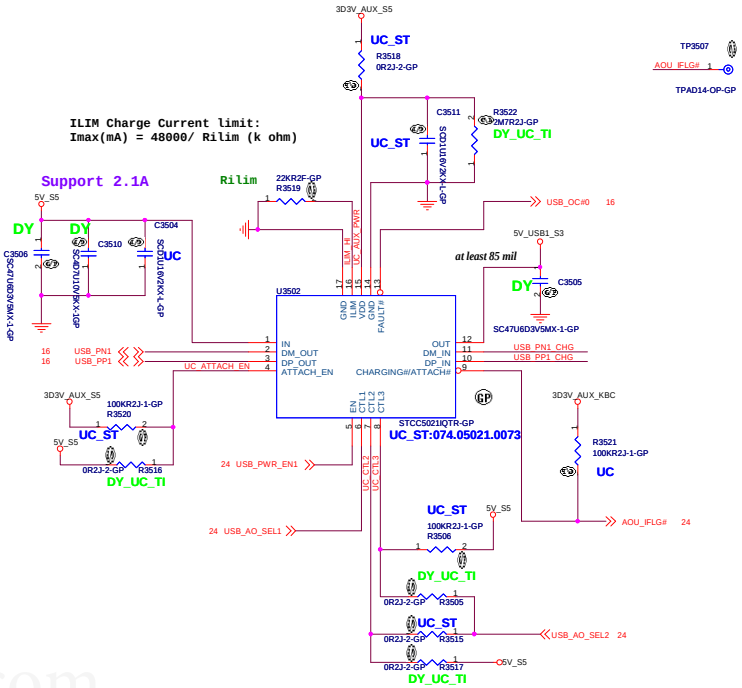






ILIM Charge Current limit:
Imax(mA) = 48000/ Rilim (k ohm)

Support 2.1A



M40

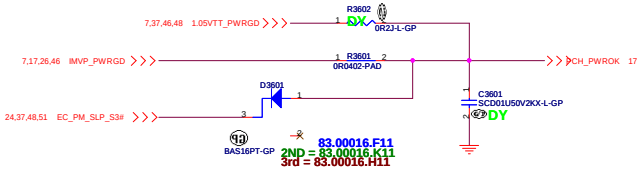
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

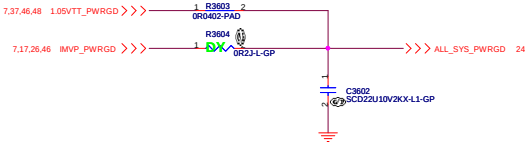
Title: USB 2.0 / 3.0 Port

Size: A2 | Document Number: LF15V | Rev: -1

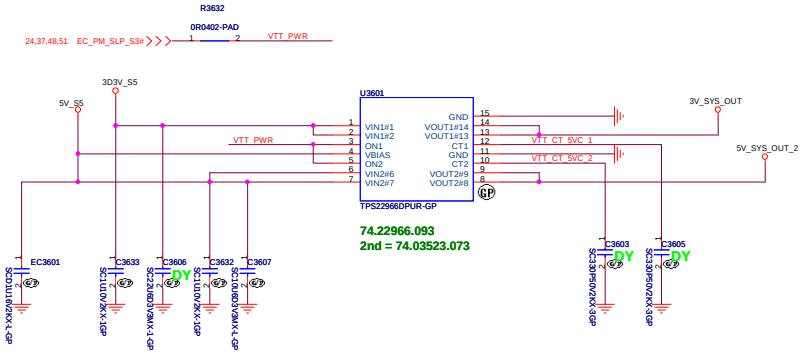
Date: Thursday, October 30, 2014 | Sheet 35 of 102

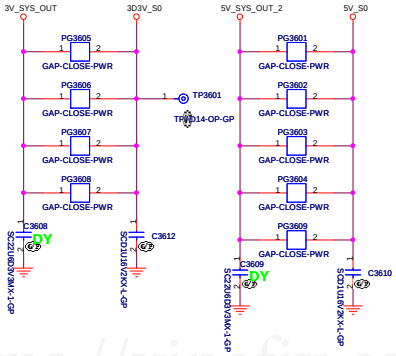
Power Sequence



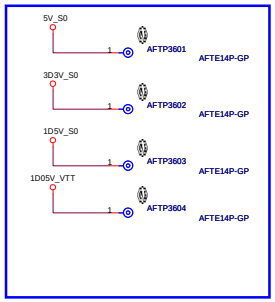


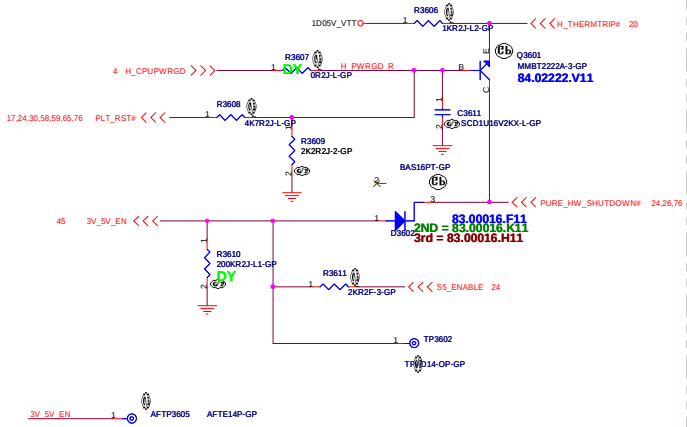
Run Power



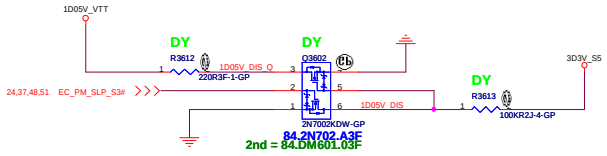


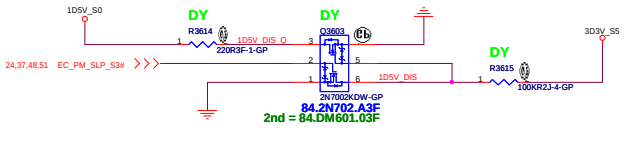
Test point

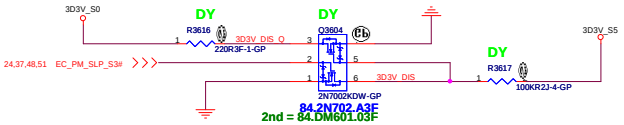


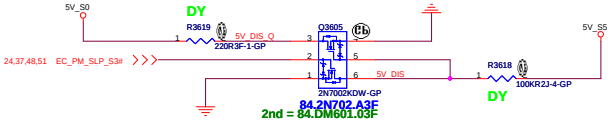


Discharge circuit









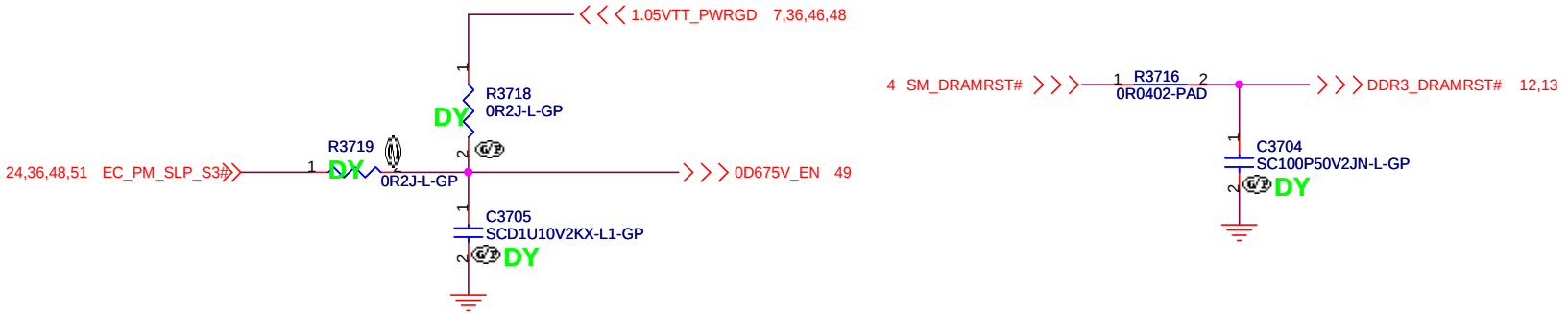
BOM1

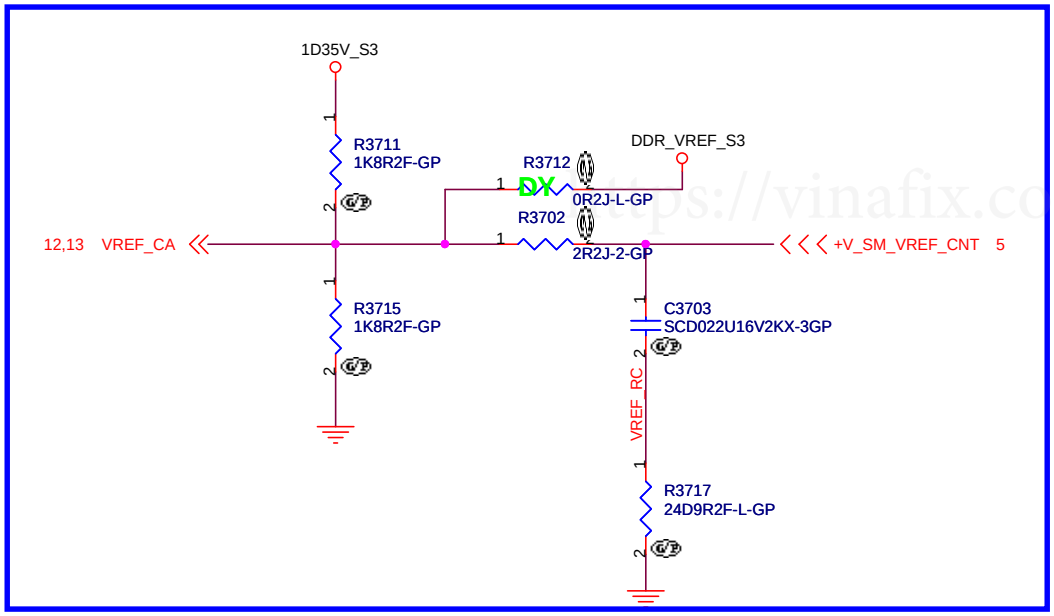
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable & SEQUENCE

Size	Document Number	Rev
A2	LF15V	-1

Date: Thursday, October 30, 2014 Sheet 36 of 102





For Intel Recommend Close to DIMM

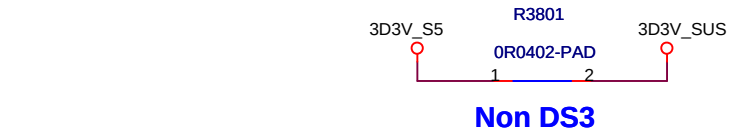
BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

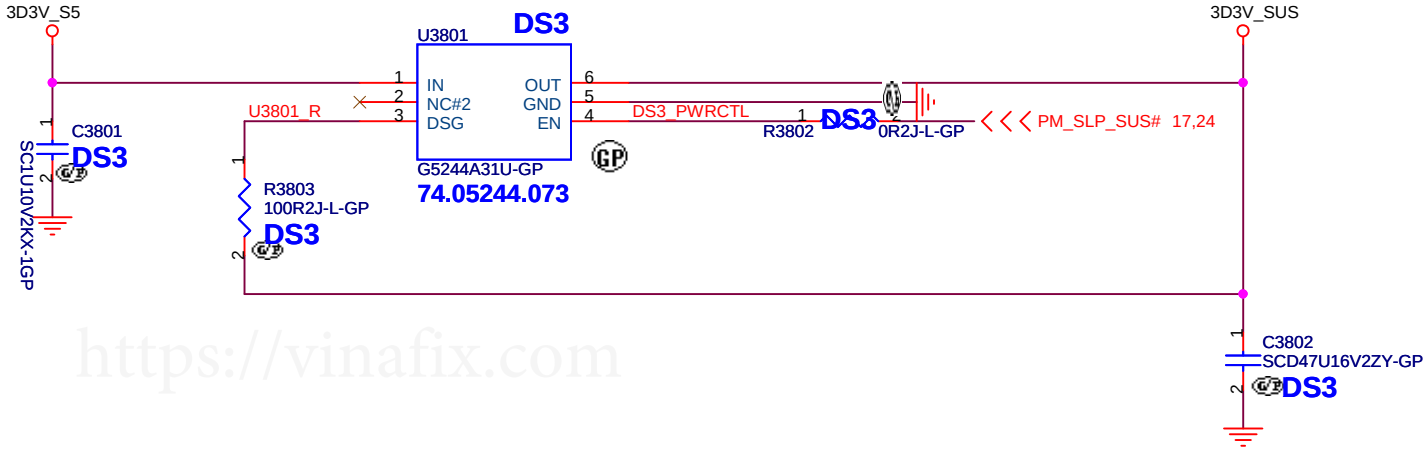
Title: ADAPTER OCP / S3 reduction

Size	Document Number	Rev
Custom	LF15V	-1

Date: Monday, July 28, 2014 Sheet 37 of 102



Non DS3



BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***(Reserved)***		
Size: A4	Document Number: **LF15V**	Rev: **-1**
Date: Thursday, October 30, 2014	Sheet 38 of 102	

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***1D05_M***	
Size: Custom	Document Number: **LF15V**	Rev: **-1**
Date: Monday, July 14, 2014	Sheet 39 of 102	

BOM1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Connected Standby1

Size	Document Number	Rev
A	**LF15V**	**-1**

Date: Monday, July 14, 2014 Sheet 40 of 102

BOM1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

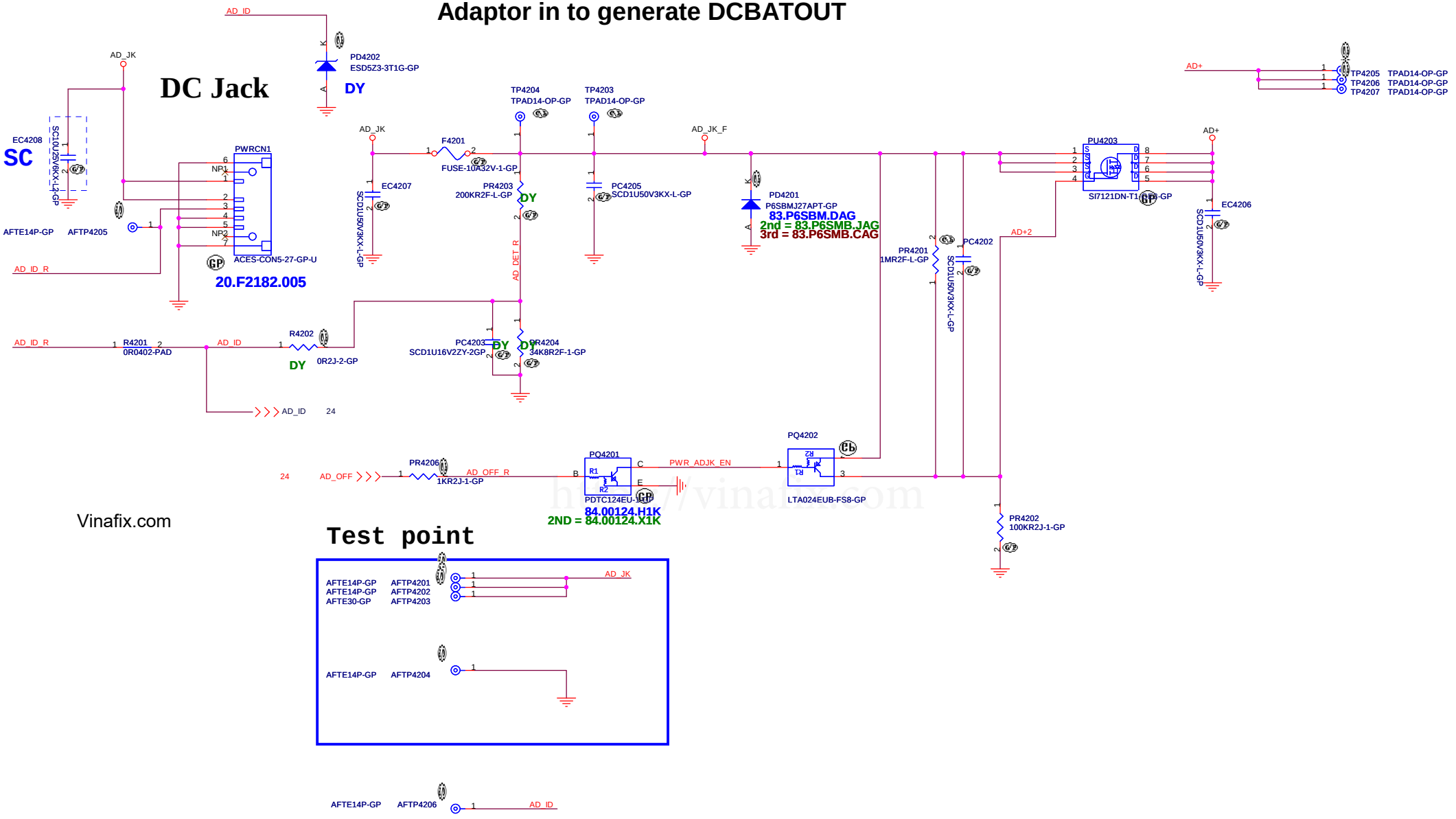
Title

Connected Standby2

Size	Document Number	Rev
A	**LF15V**	**-1**

Date: Monday, July 14, 2014 Sheet 41 of 102

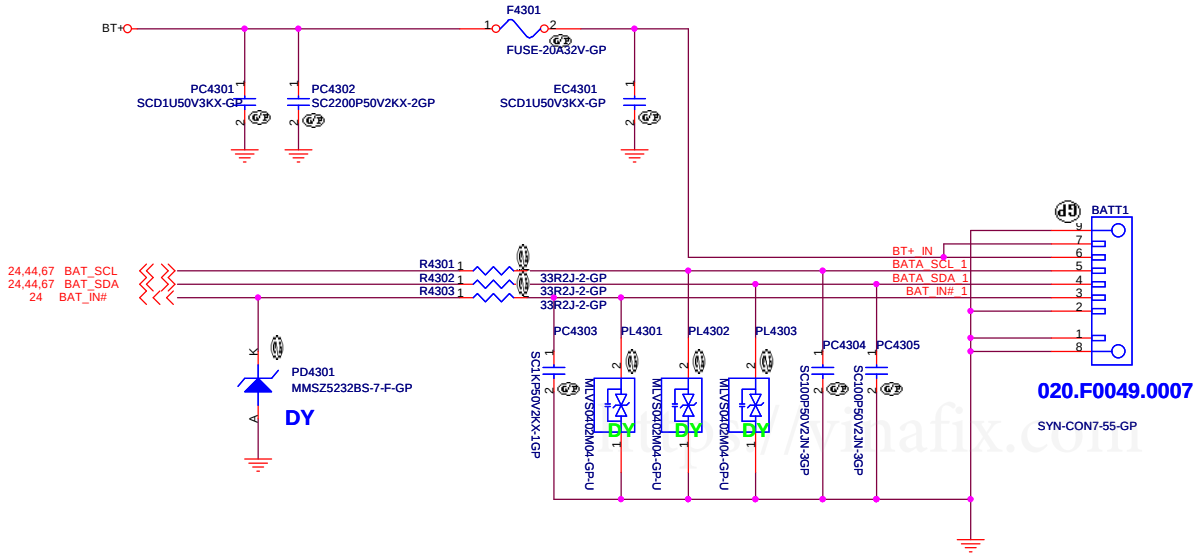
Adaptor in to generate DCBATOUT

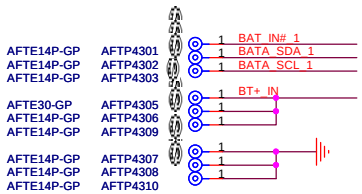


BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DCIN JACK		
Size: A3	Document Number: LF15V	Rev: -1
Date: Thursday, October 30, 2014	Sheet 42 of 102	

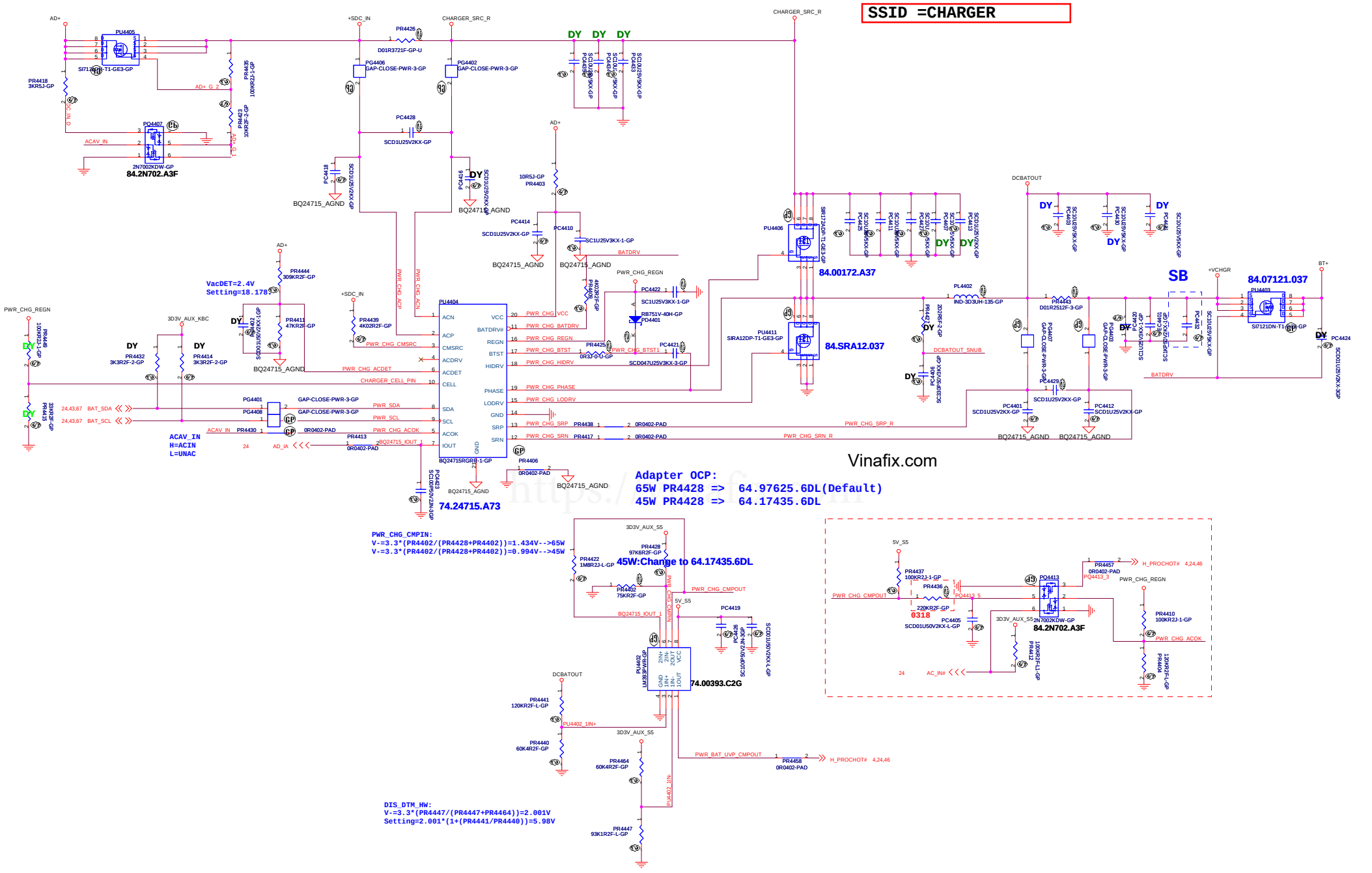
BATTERY CONNECTOR





BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BATT CONN		
Size: A3	Document Number: LF15V	Rev: -1
Date: Thursday, October 30, 2014	Sheet 43 of 102	

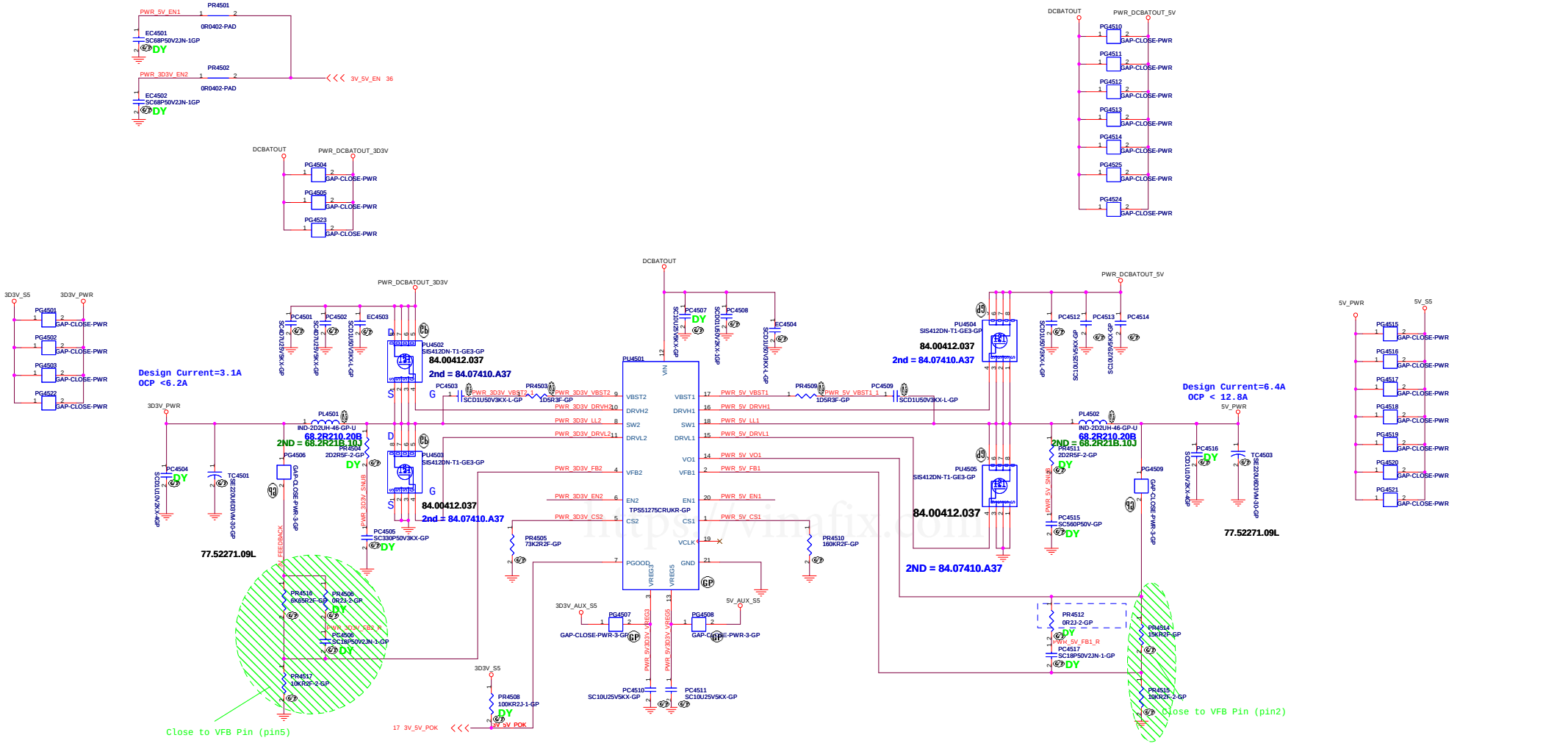


<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER_BQ24715

Size	Document Number	Rev
A2	LF15V	-1

Date: Thursday, October 30, 2014 Sheet 44 of 102



<Core Design>

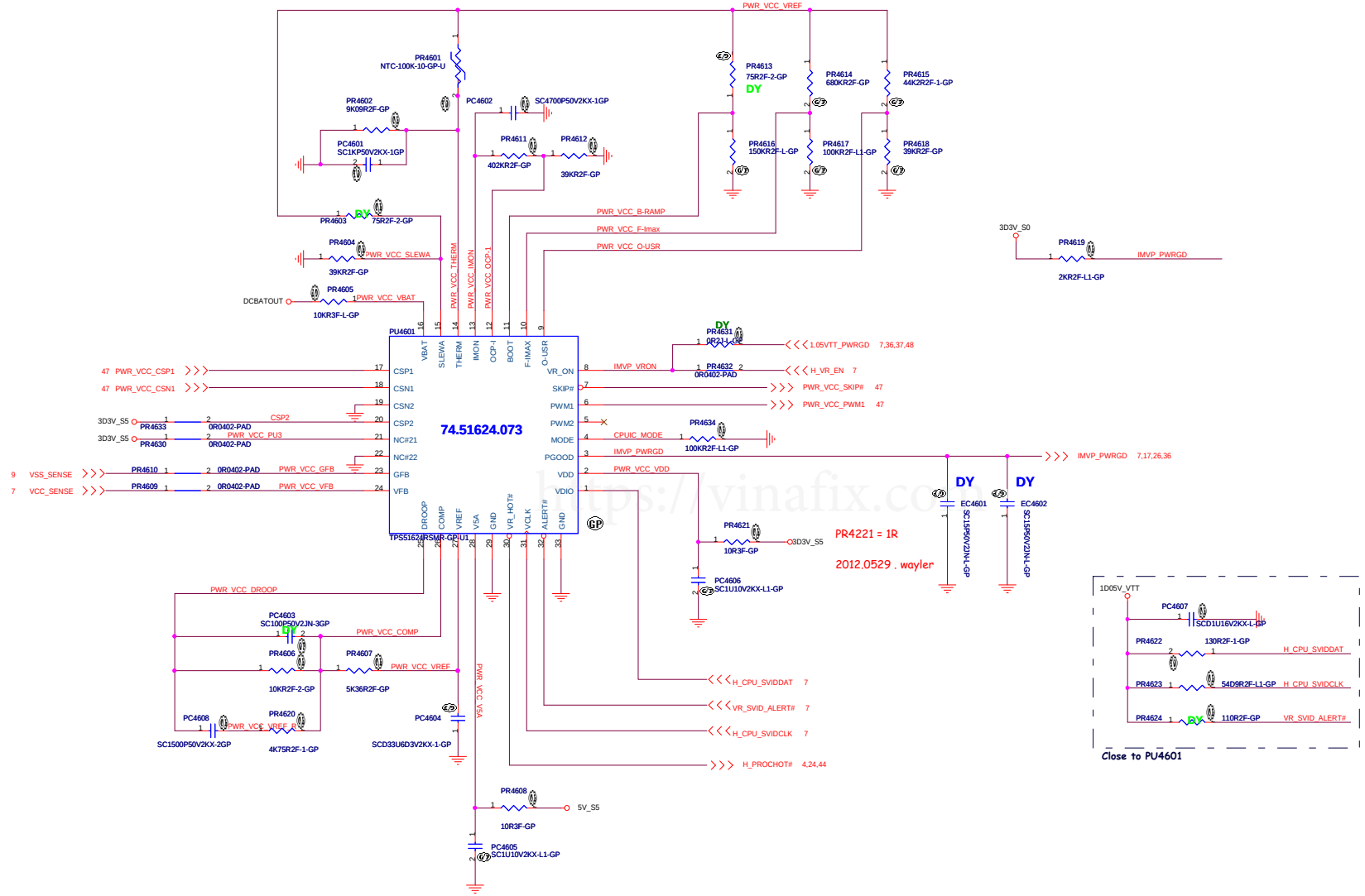
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51275 5V/3D3V

Size: A2 | Document Number: LF15V teknisi indonesia | Rev: -1

Date: Thursday, October 30, 2014 | Sheet 45 of 102

SSID = CPU.Regulator



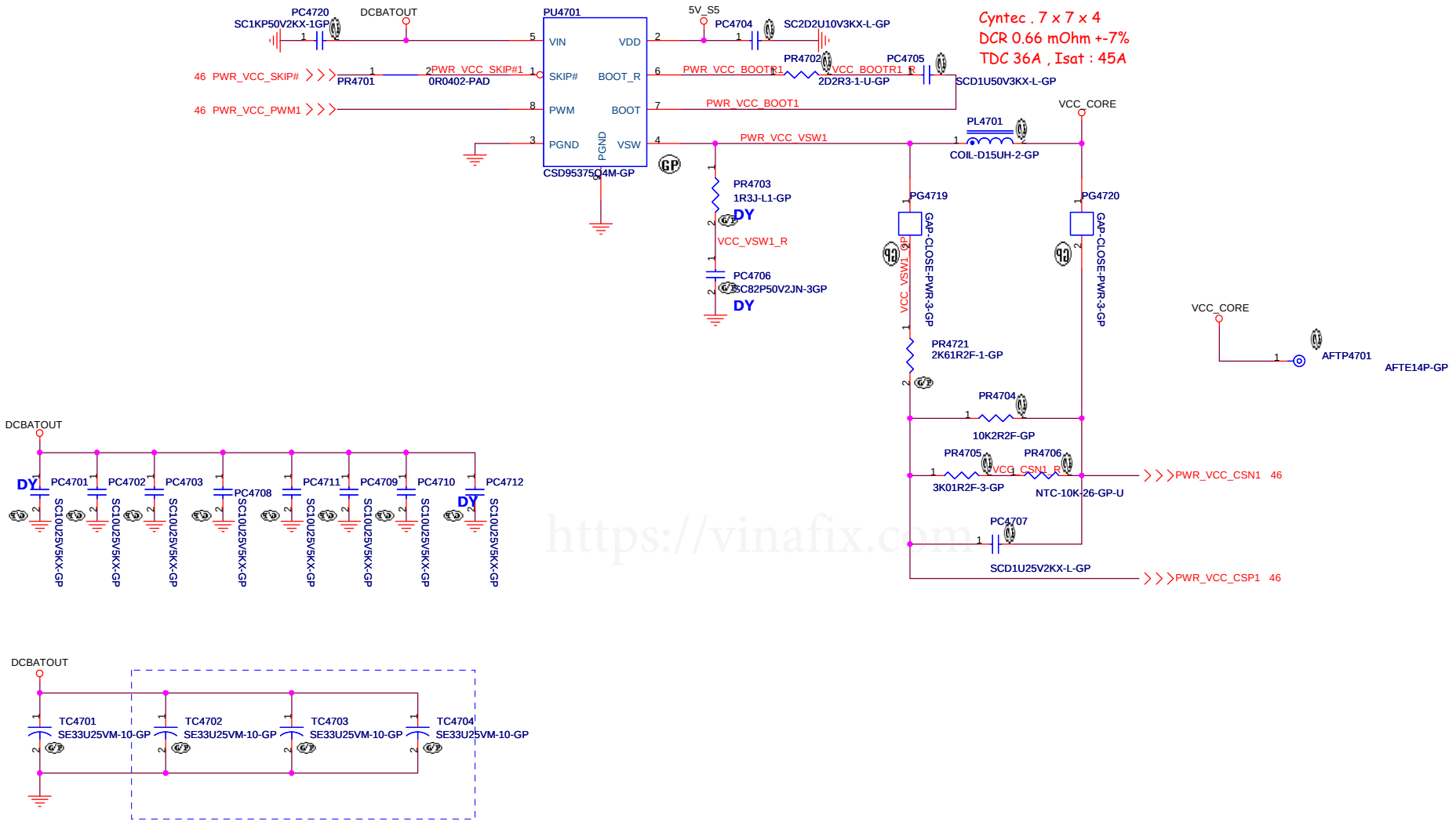
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51624_CPUCORE(1/2)

Size: C | Document Number: LF15V | Rev: -1

Date: Thursday, October 30, 2014 | Sheet 46 of 102



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

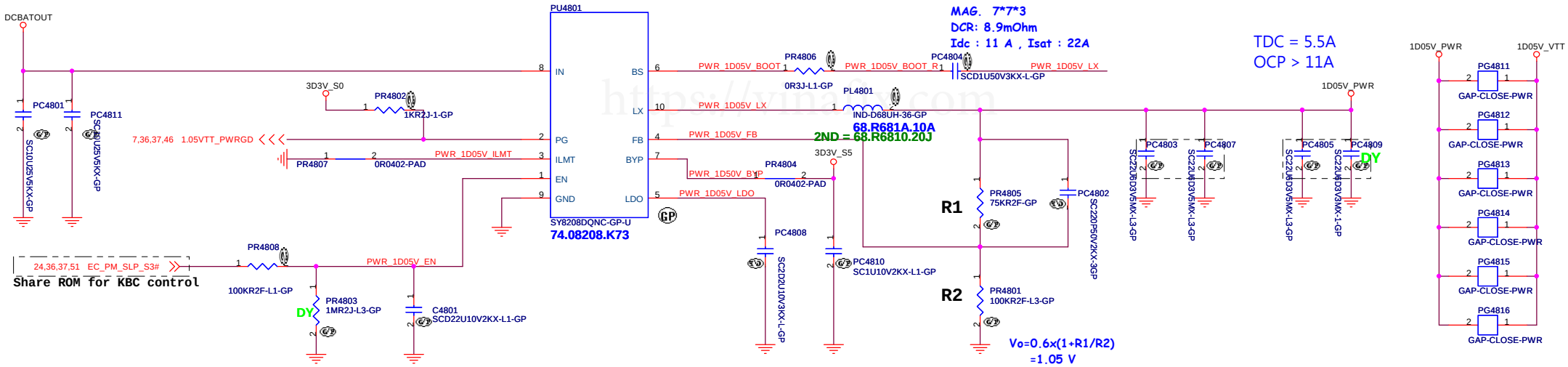
Title: **TPS51624_CPUCORE(2/2)**

Size	Document Number	Rev
B	LF15V	-1

Date: Thursday, October 30, 2014 Sheet 47 of 102

SY8208D for 1D05V

Vinafix.com



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DC to DC_1D05V(SY8208)		
Size: A3	Document Number: LF15V	Rev: -1
Date: Thursday, October 30, 2014	Sheet 48 of 102	

SSID = PWR.Plane.Regulator_1p2v0p6v

RT8207L for VDDQ

DCBATOUT
PWR_DCBATOUT_VDDQ
PG4901 GAP-CLOSE-PWR
PG4902 GAP-CLOSE-PWR
PG4903 GAP-CLOSE-PWR
PG4904 GAP-CLOSE-PWR

17,24 PM_SLP_S4#
PR4902 0R0402-PAD
PWR_VDDQ_EN
PC4901 SCD1U10V2KX-5GP DY
Follow Wistron SB ULT CRB

SB

PWR_VDDQ_VCC5
PR4903 5D1R2F-GP 5V_S5
PC4903 SC1U10V2KX-1GP
PC4902 SC1KP50V2KX-1GP
PR4904 7.87R2F-GP
PWR_VDDQ_CS
PWR_VDDQ_VDDP
PR4905 0R0603-PAD 5V_S5
PC4904 SC1U10V2KX-1GP

3D3V_S5
PR4906 10KR2F-2-GP
Follow Wistron SB ULT CRB
Del RUNPWROK

PU4901 RT8207MZQW-GP-U

Pin	Name	Net
13	CS	
11	VDD	
12	VDDP	
10	PGOOD	1D35V_PWRGD
9	TON	PWR_VDDQ_TON
8	S5	PWR_VDDQ_EN
7	S3	PWR_VTT_EN
19	VLDOIN	PWR_VDDQ_VTTIN
1	VTTGND	
20	VTT	DDR_VREF_PWR
2	VTTSNS	
21	GND	
3	GND	
4	VTTREF	1PWR_VDDQ_VTTREF
18	BOOT	PWR_VDDQ_BOOT
17	UGATE	PWR_VDDQ_UGATE
16	PHASE	PWR_VDDQ_PHASE
15	LGATE	PWR_VDDQ_LGATE
14	PGND	
5	VDDQ	PWR_VDDQ_SENSE
6	FB	PWR_VDDQ_FB

PR4908 2D2R3-1-U-GP
PWR_VDDQ_PHASE_L
PC4905 SCD1U50V3KX-1GP

PWR_DCBATOUT_VDDQ
PR4907 620KR2F-GP
PC4906 SC10U10V5KX-L1-GP
PG4905 GAP-CLOSE-PWR
PG4906 GAP-CLOSE-PWR
1D35V_S3

74.08207.C73
2nd = 74.01566.073

R1 PR4910 40K2R2F-GP
PC4908 SC18P50V2JN-1-GP
R2 PR4911 48K7R2F-1-GP
Vout setting
Close to PIN9

Vout=0.75 x (1+R1/R2)
=0.75 x (1+40/49.9)
=1.35

PG4909 GAP-CLOSE-PWR 1D35V_S3
PR4909 0R0402-PAD DDR_VREF_S3
PC4907 SCD033U16V2KX-GP

+0.675VS
Iomax: 1A

0D675V_S0
PG4907 GAP-CLOSE-PWR
PG4908 GAP-CLOSE-PWR
DDR_VREF_PWR
PC4909 SC10U6D3V5KX-1GP
PC4910 DY
AFTP4901 AFTE14P-GP

12 DDR_PG_OUT
PR4912 0R0402-PAD PWR_VTT_EN
37 0D675V_EN
PR4913 DY 0R2J-2-GP
Follow Wistron SB ULT CRB

PWR_DCBATOUT_VDDQ
PC4911 SCD47U25V5KX-GP
PC4912 SCD47U25V5KX-GP
PC4913 SCD47U25V5KX-GP
OPS
PC4914 SC1U50V3KX-1-GP

PU4902 SIR172ADP-T1-GE3-GP
84.00172.A37
PU4903 SIRA12DP-T1-GE3-GP
84.SRA12.037

IccTDC = 9.5A
OCP <19A

PL4901 IND-1UH-94-GP
68.1R01B.10K
1D35V_S3
EC4902 SC1U16V2KX-L-GP
EC4901 SC1U16V2KX-L-GP
PC4915 SC1U16V3KX-5GP DY
PT4901 SEE330U2V5VM-1-GP
PT4902 DY SEE220U2VDM-8GP
SC

1D35V_S3 AFTP4902 AFTE14P-GP

<Core Design>

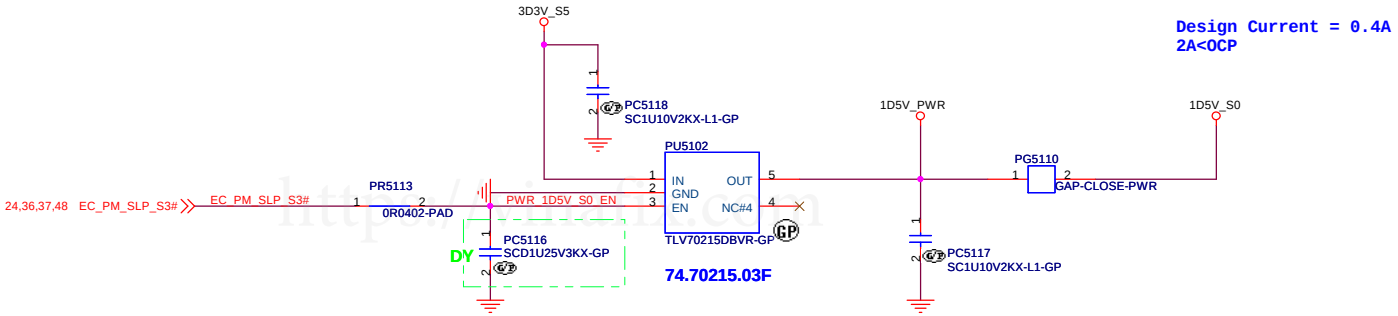
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8207(VDDQ_VTT)
Size: Custom | Document Number: LF15V | Rev: -1
Date: Thursday, October 30, 2014 | Sheet 49 of 102

BOM1

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***1D8V_S0***		
Size: A4	Document Number: **LF15V**	Rev: **-1**
Date: Monday, July 14, 2014	Sheet 50 of 102	

TLV70215 for 1D5V_S0



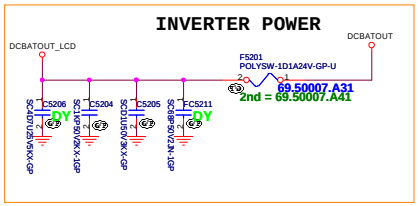
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***1D5V_S0 RT9025***	
Size A3	Document Number **LF15V**	Rev **-1**
Date: Thursday, October 30, 2014	Sheet 51 of 102	

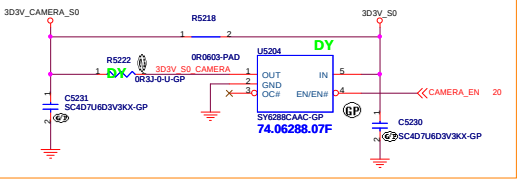
SSID = VIDEO

INVERTER POWER

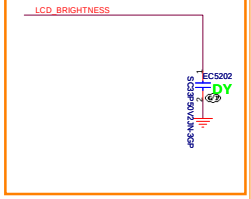


CAMERA POWER

Layout 40 mil



Close to eDP connector

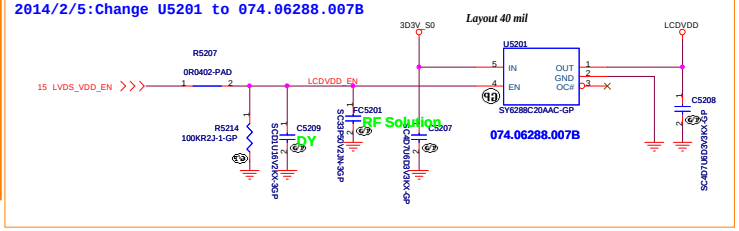


SSID = VIDEO

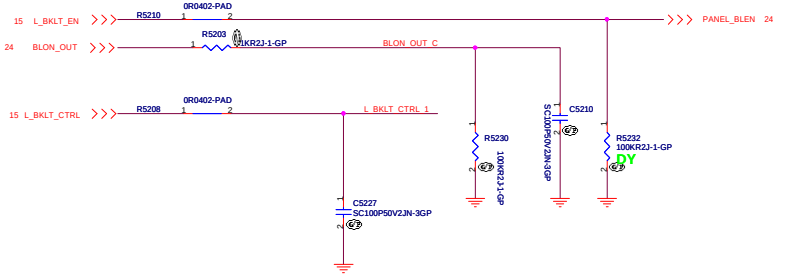
LCD POWER (Do Not use SW 74.09724.09F)

2014/2/5:Change U5201 to 074.06288.007B

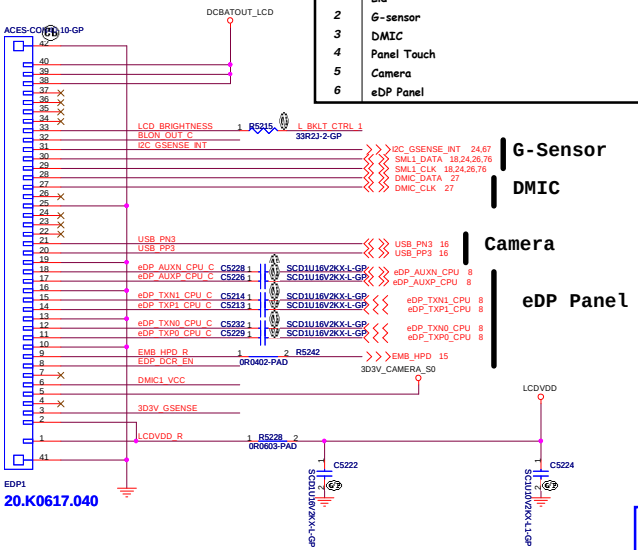
Layout 40 mil



Panel BL brightness/Power En/BL En



eDP connector



eDP Device

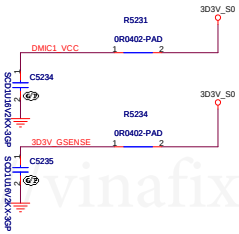
Item	Device
1	Lid
2	G-sensor
3	DMIC
4	Panel Touch
5	Camera
6	eDP Panel

G-Sensor

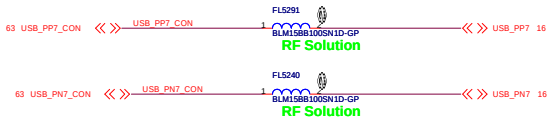
DMIC

Camera

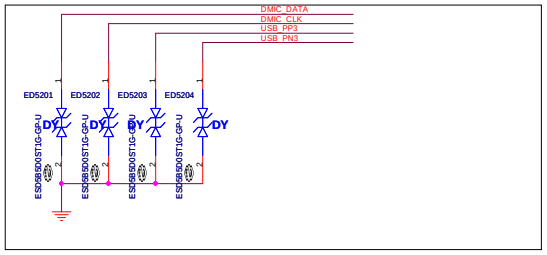
eDP Panel



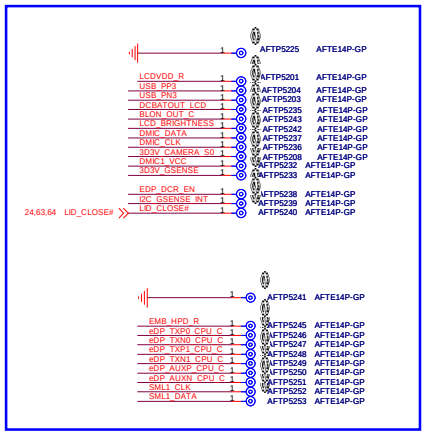
Vinafix.com



ESD Request



Test point



M40

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LCD Connector		
Size: A2	Document Number: LF15V	Rev: -1
Date: Thursday, October 30, 2014	Sheet 52 of 102	

BOM1

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CRT Board Connector

Size	Document Number	Rev
Custom	LF15V	-1

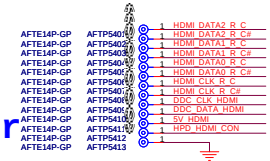
Date: Monday, July 14, 2014 Sheet 53 of 102

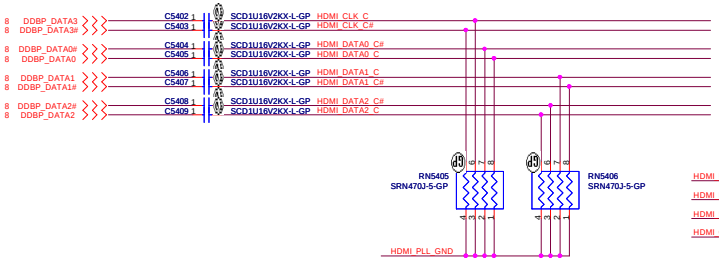
SSID = VIDEO

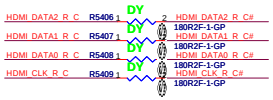
HDMI CONNECTOR

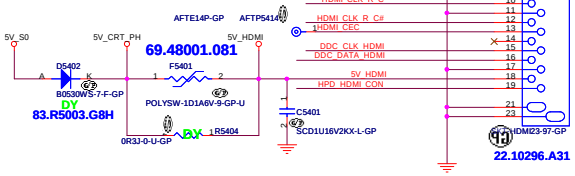
HDMI Passive Level Shifter

Close to HDMI Connector

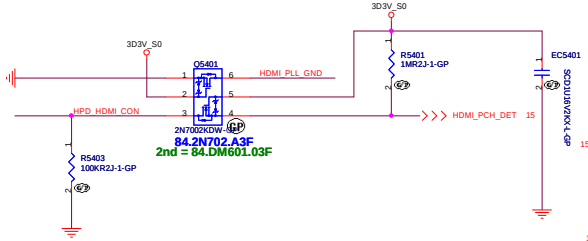


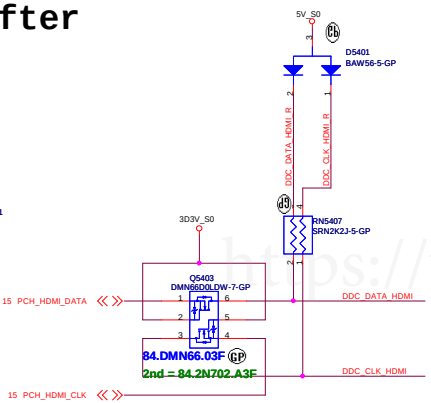


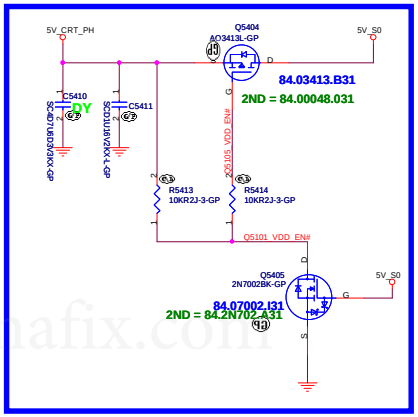


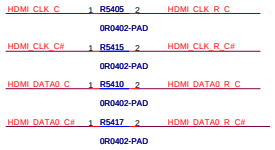


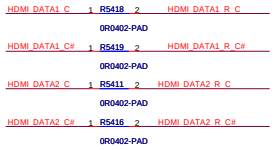
HDMI DDC Passive Level Shifter

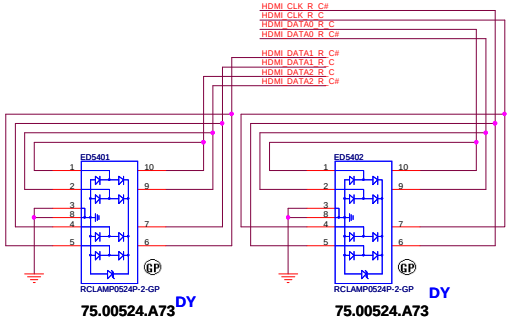


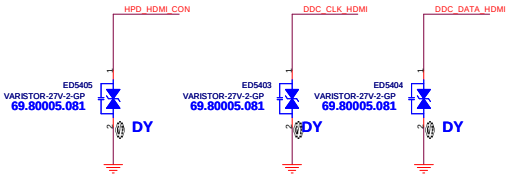












BOM1

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	HDMI Level Shifter/Connector
Size: A2	Document Number: LF15V
Rev	-1
Date: Thursday, October 30, 2014	Sheet 54 of 102

BOM1

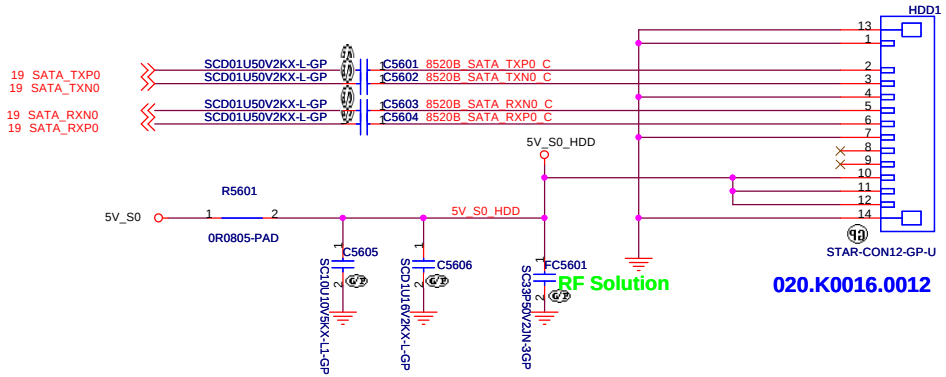
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

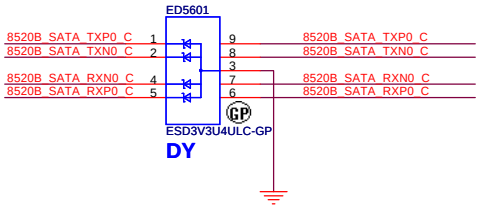
Title: ***TRAVIS***

Size	Document Number	Rev
A2	LF15V	-1

Date: Monday, July 14, 2014 Sheet 55 of 102

SSID = SATA





Vinafix.com

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HDD / NGFF_SSD***

Size	Document Number	Rev
A3	LF15V	-1

Date: Thursday, October 30, 2014 Sheet 56 of 102

BOM1

緯創資通

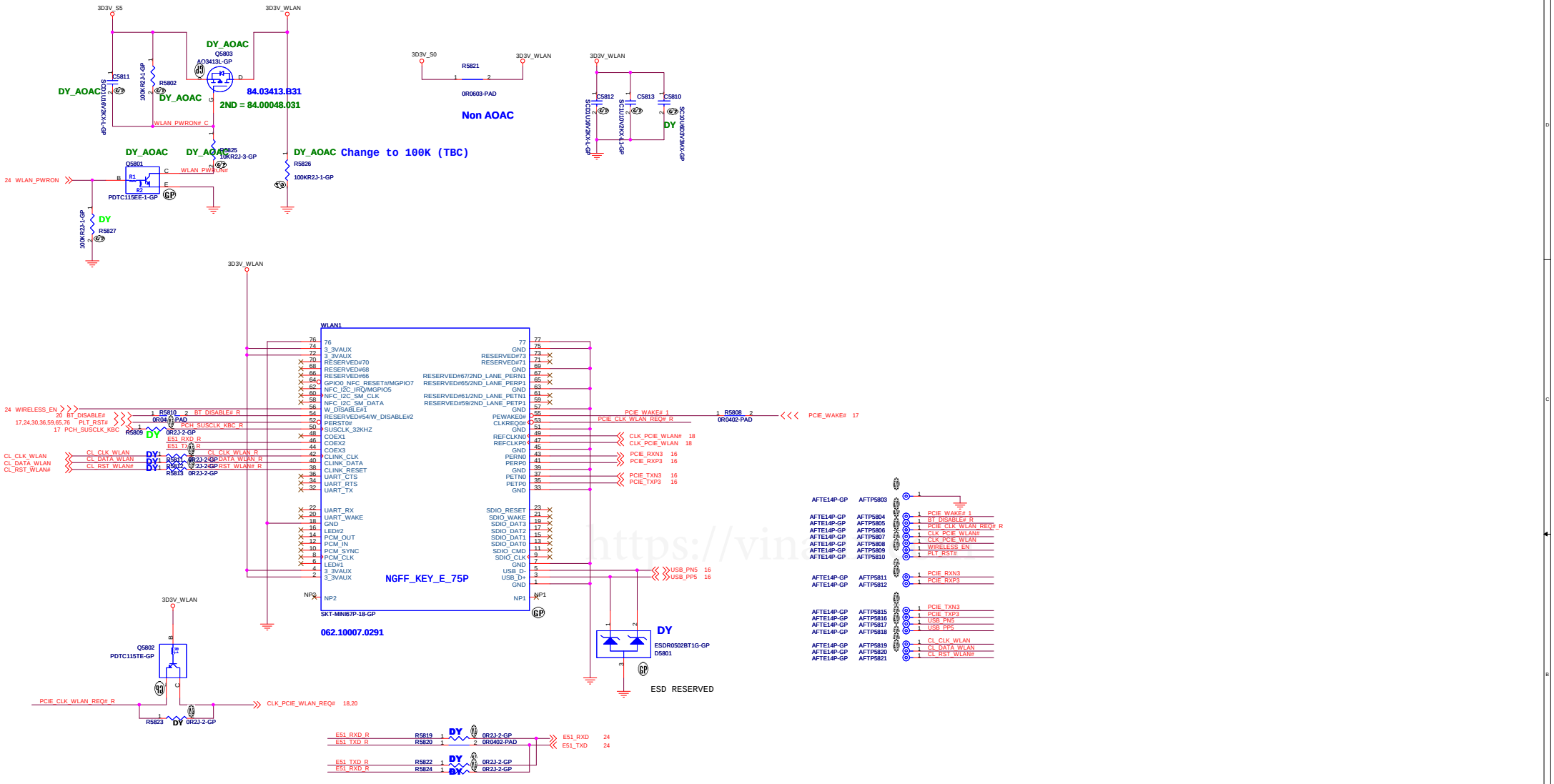
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

E-SATA

Size	Document Number	Rev
A4	**LF15V**	**-1**

Date: Monday, July 14, 2014 Sheet 57 of 102



BOM1

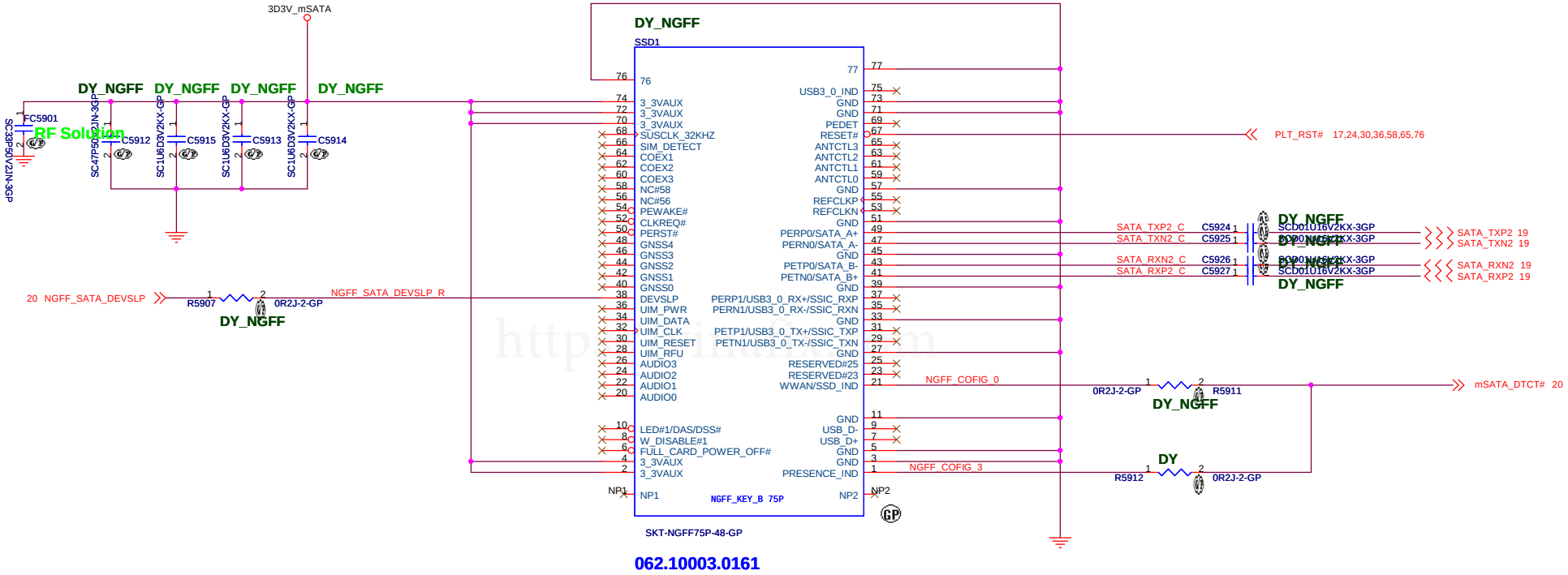
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

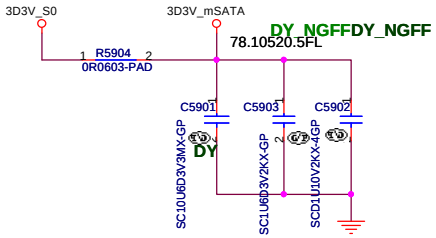
Title: **NGFF WLAN**

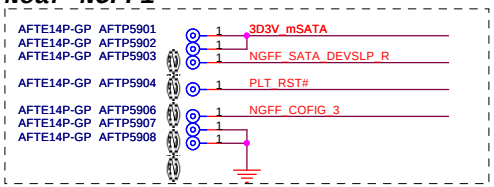
Size	Document Number	Rev
A2	LF15V	-1

Date: Thursday, October 30, 2014 Sheet 58 of 102

SSID = Wireless







BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NGFF_SATA

Size	Document Number	Rev
A3	LF15V	-1

Date: Thursday, October 30, 2014 Sheet 59 of 102

BOM1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

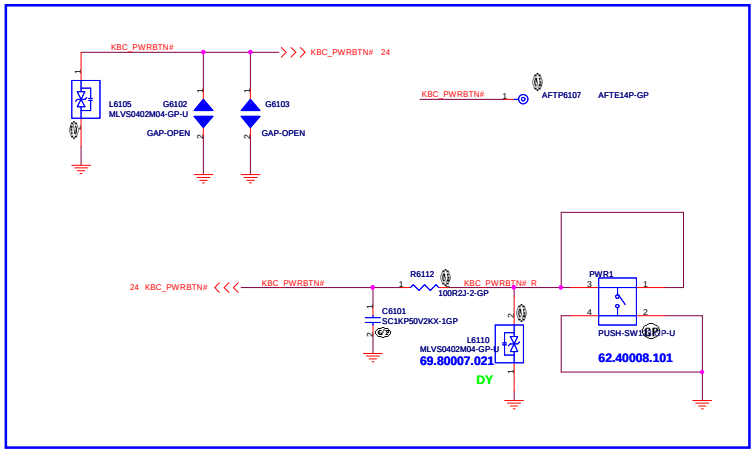
Title

mSATA Connector

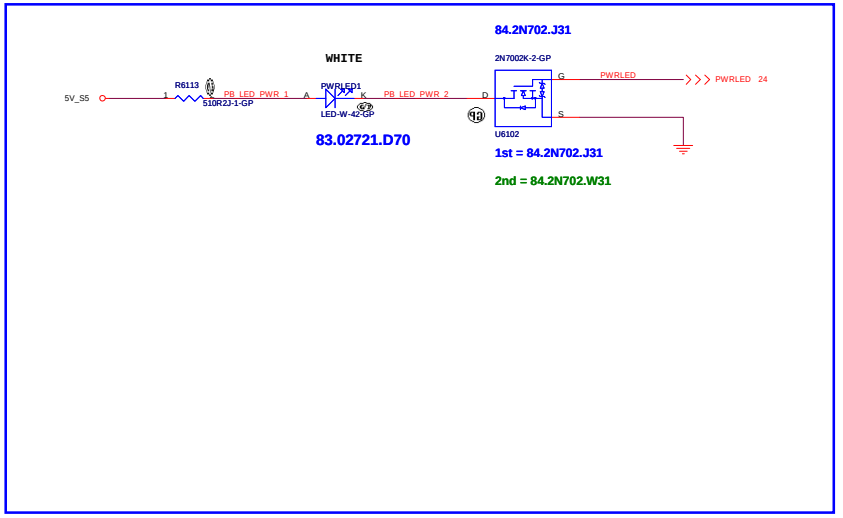
Size	Document Number	Rev
A4	**LF15V**	**-1**

Date: Monday, July 14, 2014 Sheet 60 of 102

Power Button

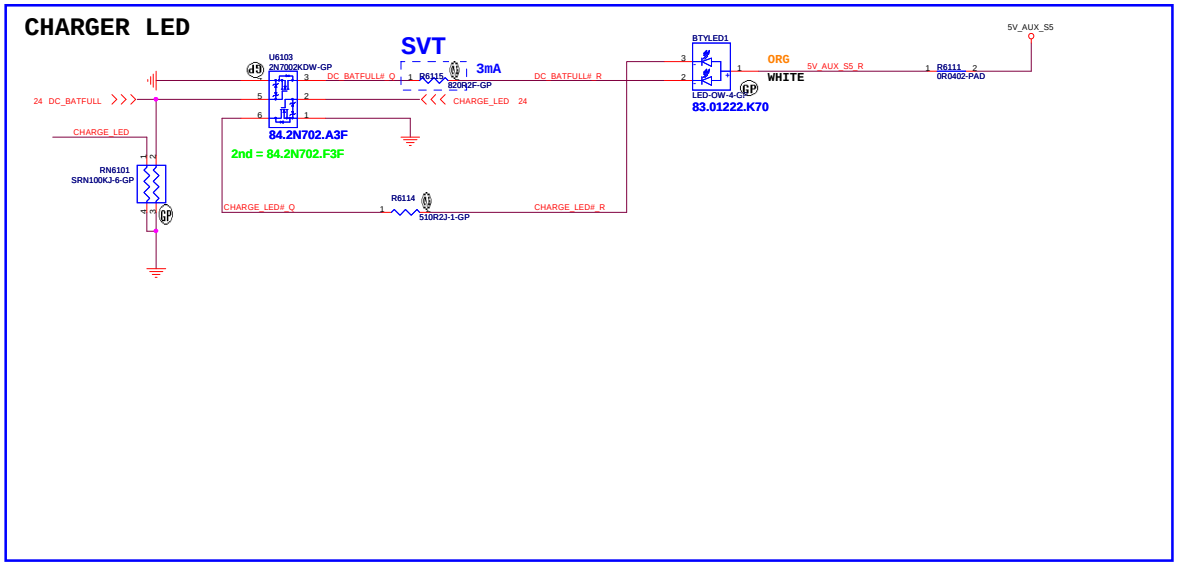


POWER BTN LED

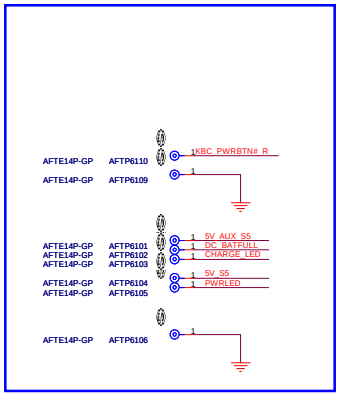


Vinafix.com

CHARGER LED



Test point



BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

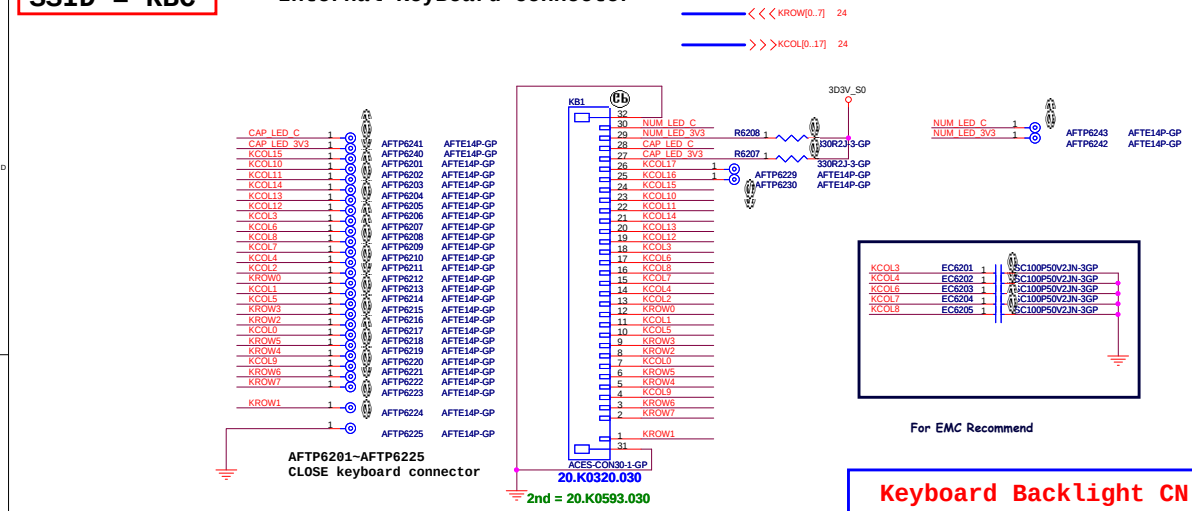
Title: LED Bard/Power Button

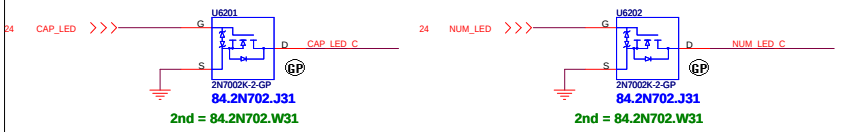
Size: A2 | Document Number: LF15V | Rev: -1

Date: Thursday, October 30, 2014 | Sheet 61 of 102

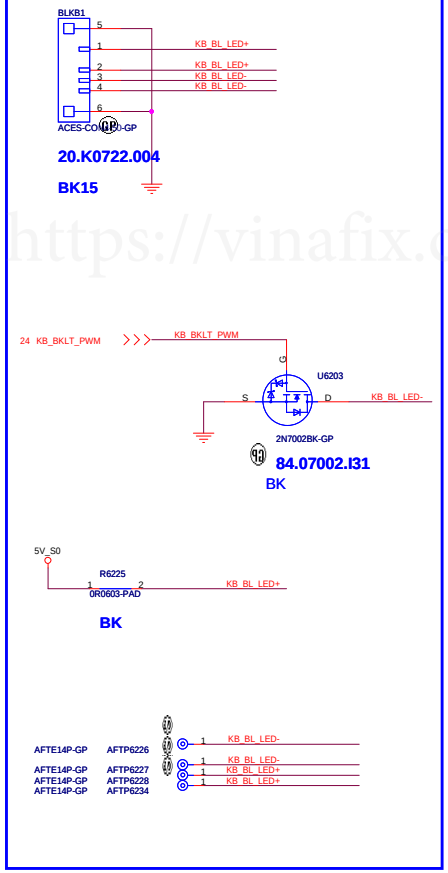
SSID = KBC

Internal KeyBoard Connector

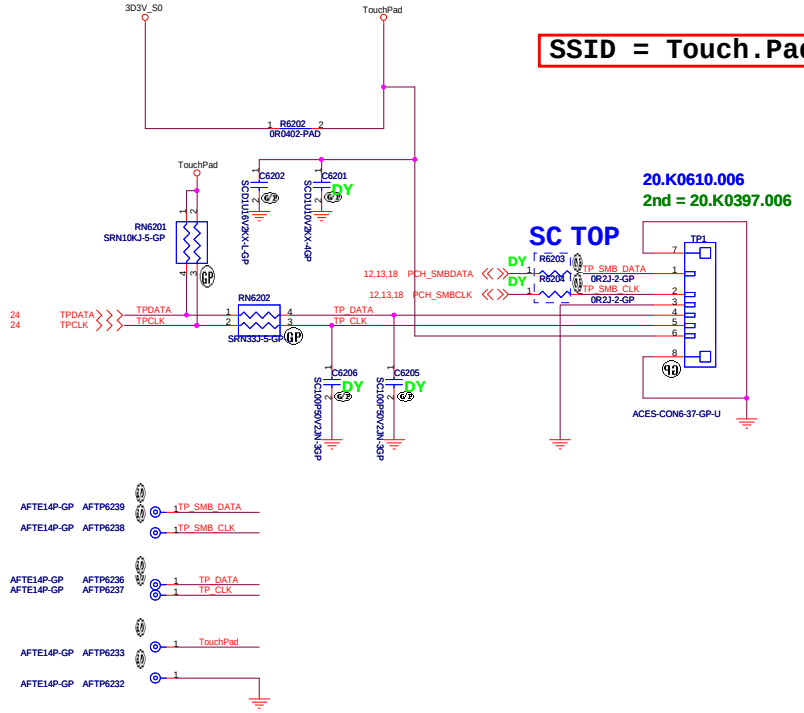




Keyboard Backlight CN



SSID = Touch.Pad



BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Key Board/Touch Pad**

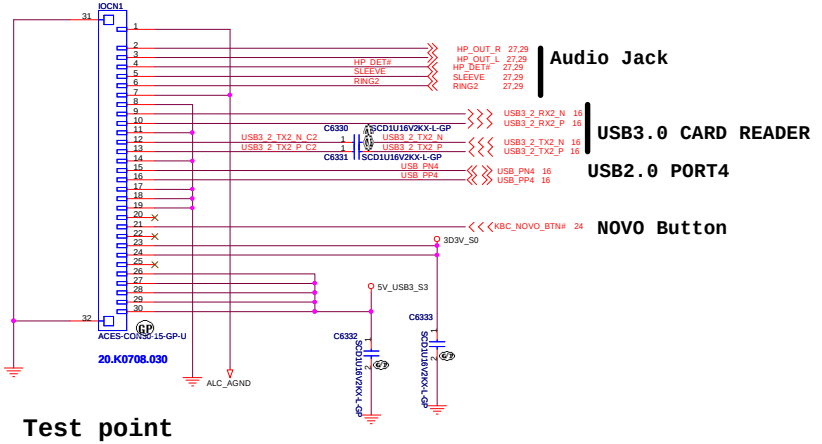
Size	Document Number	Rev
Custom	LF15V	-1

Date: Thursday, October 30, 2014 Sheet 62 of 102

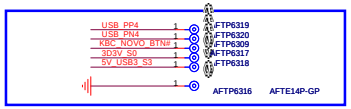
IO BD Device

Item	Device
1	Audio Jack
2	USB Card Reader
3	USB2.0 Port4
4	NOVO Button

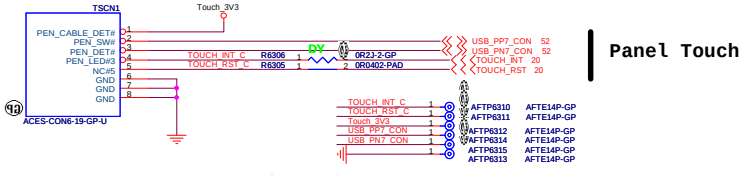
IO BD Viber



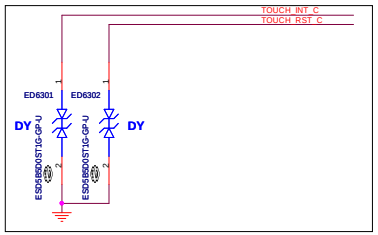
Test point



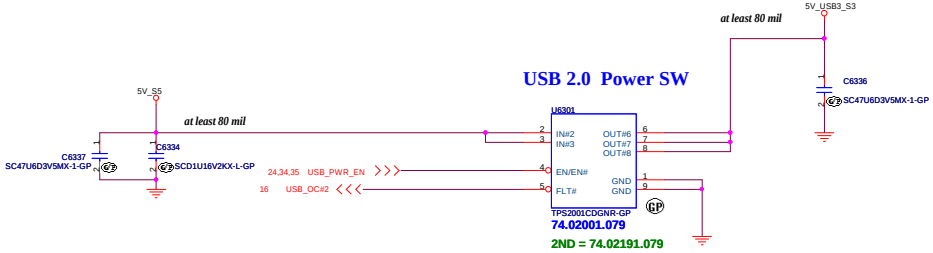
Control Board CONN



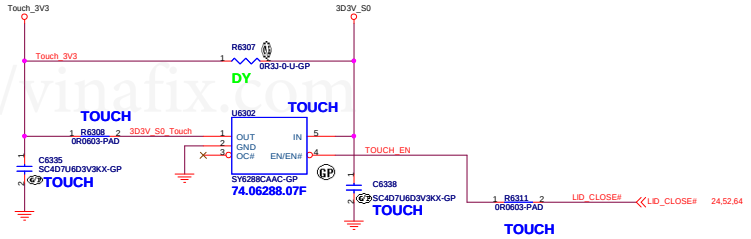
ESD Request



USB 2.0 Power SW



U6301 place near to IOCN1



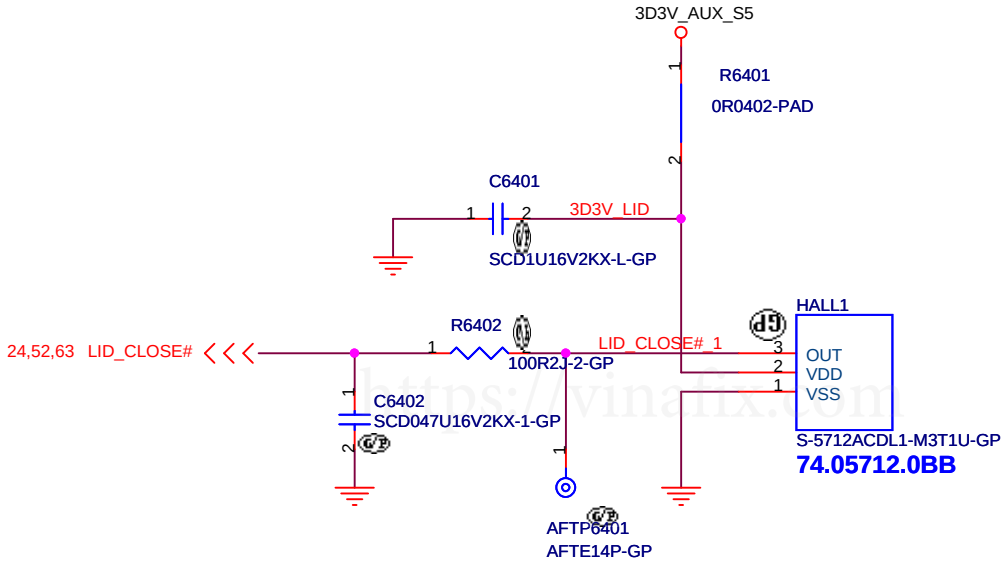
BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **IO Board Connector**

Size	Document Number	Rev
A2	LF15V	-1

Date: Thursday, October 30, 2014 Sheet 63 of 102



BOM1

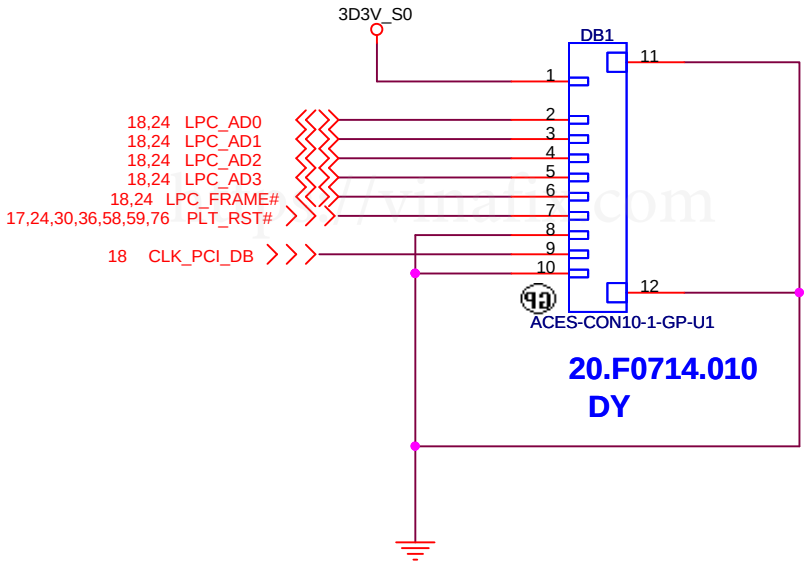
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	LF15V	-1

Date: Thursday, October 30, 2014 Sheet 64 of 102

Debug Connector



BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Dubug connector*		
Size: A4	Document Number: LF15V	Rev: -1
Date: Monday, July 28, 2014	Sheet 65 of 102	

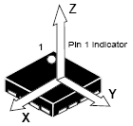
(Blanking)

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***SENSOR HUB***		
Size: A3	Document Number: **LF15V**	Rev: **-1**
Date: Monday, July 14, 2014	Sheet 66 of 102	

Free Fall Sensor

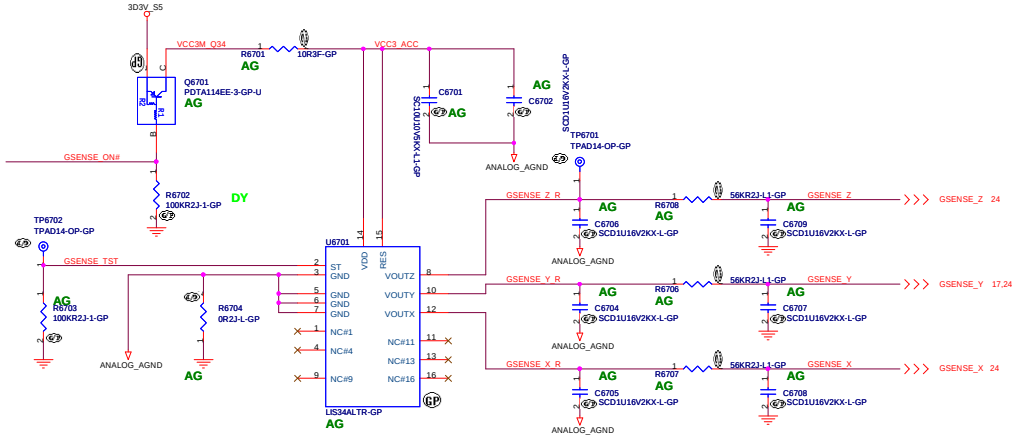
Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"

Analog G-Sensor



STMicro LIS34AL: 74.00034.0BZ
2nd = 74.KXTC8.0BZ

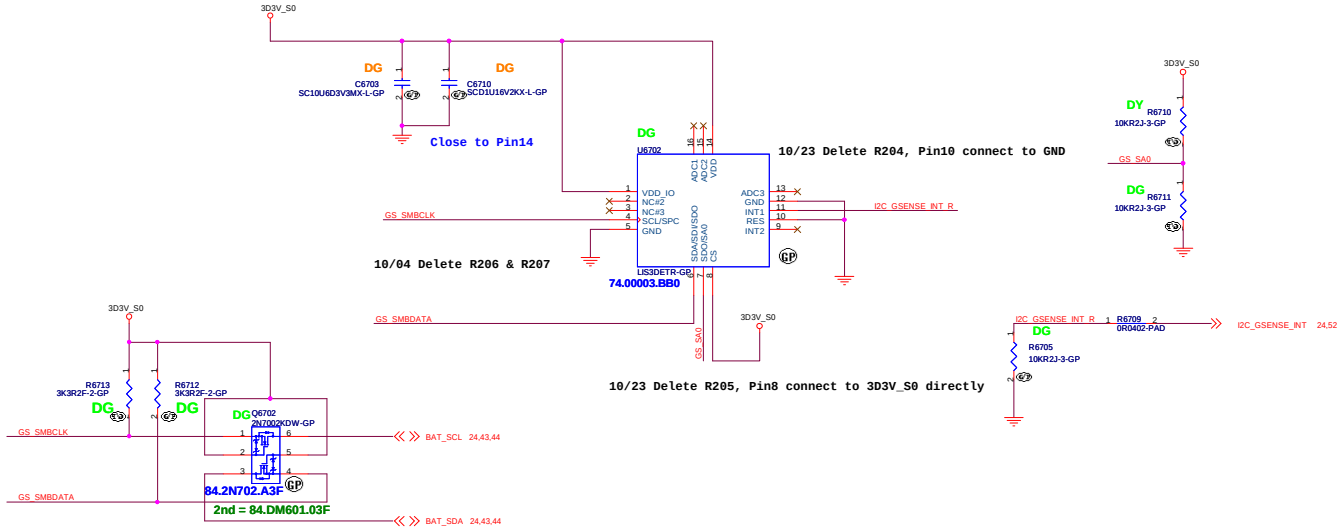
Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.

SC Digital_G-sensor

The Slave ADdress (SAD) associated to the LIS3DH is 001100xb. SDO/SA0 pad can be used to modify less significant bit of the device address. If SA0 pad is connected to voltage supply, LSb is '1' (address 0011001b) else if SA0 pad is connected to ground, LSb value is '0' (address 0011000b). This solution permits to connect and address two different accelerometers to the same I2C lines.



M40

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: G Sensor

Size	Document Number	Rev
A2	LF15V	-1

Date: Thursday, October 30, 2014 Sheet 67 of 102

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thunderbolt (1/5)***

Size	Document Number	Rev
Custom	**LF15V**	**-1**

Date: Monday, July 14, 2014 Sheet 68 of 102

BOM1

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Title: ***Thunderbolt (2/5)***

Size	Document Number	Rev
Custom	LF15V	-1

Date: Monday, July 14, 2014 Sheet 69 of 102

BOM1

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Title: ***Thunderbolt (3/5)***

Size	Document Number	Rev
Custom	**LF15V**	**-1**

Date: Monday, July 14, 2014 Sheet 70 of 102

BOM1

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Title: ***Thunderbolt (4/5)***

Size	Document Number	Rev
Custom	**LF15V**	**-1**

Date: Monday, July 14, 2014 Sheet 71 of 102

BOM1

緯創資通

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Title

Thunderbolt (5/5)

Size	Document Number	Rev
A4	**LF15V**	**-1**

Date: Monday, July 14, 2014 Sheet 72 of 102

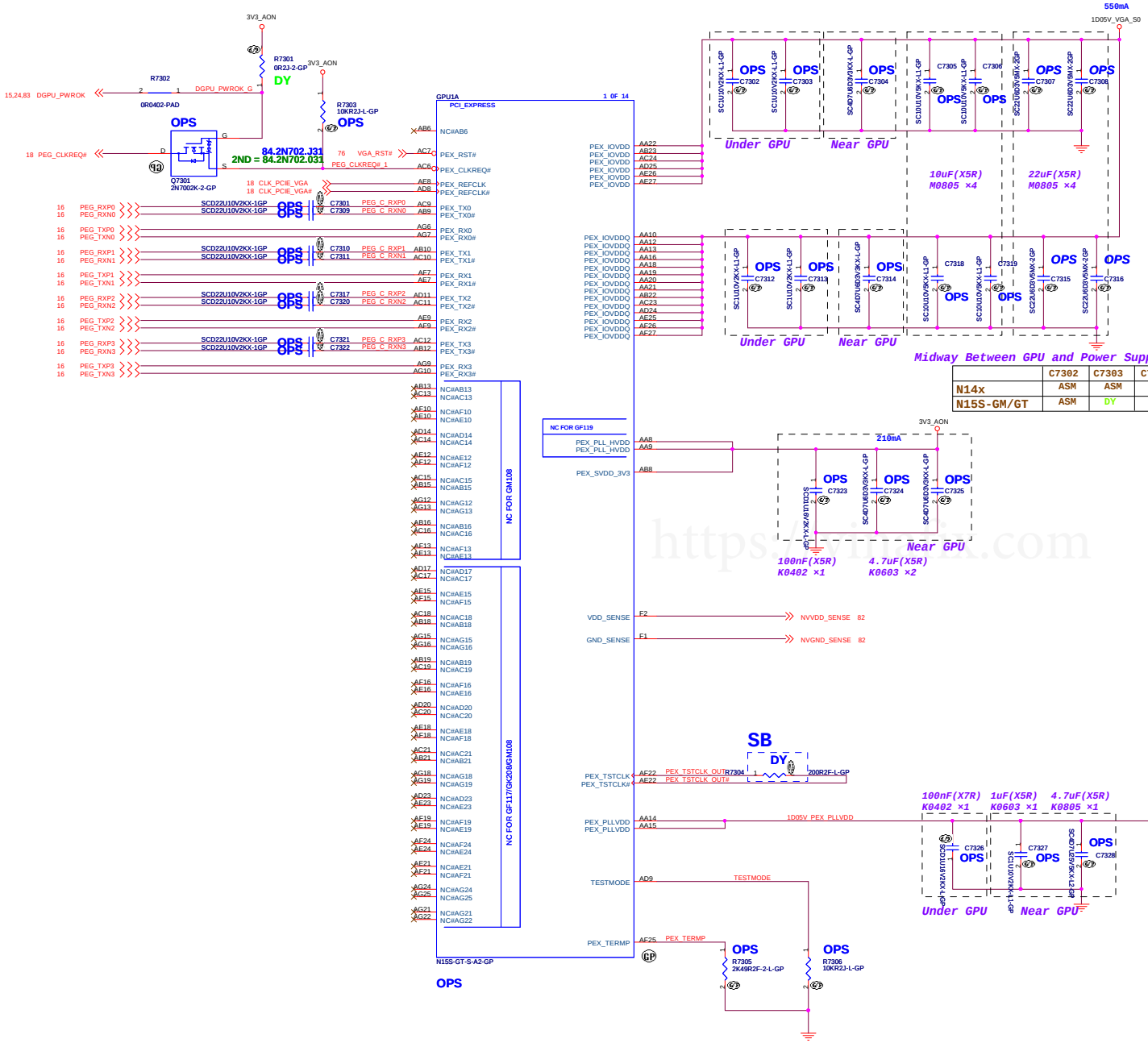

Table 3. PEX_IOVDD/Q Decoupling

Capacitor Type			Typical N14x Population	N15V-GM Population	N15S-GV Population	N15S-GM/-GT Population	Location
100uF	X6S	0402	4	4	4	1	Under GPU
4.7uF	X6S	0603	2	2	2	1	Under GPU
10uF	X5R	0805	4	4	4	1	Near GPU
22uF	X5R	0805	4	4	4	1	Near GPU

	C7302	C7303	C7304	C7305	C7306	C7307	C7308	C7312	C7313	C7314	C7318	C7319	C7315	C7316
N14x	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM
N15S-GM/GT	ASM	DY	ASM	ASM	DY	ASM	DY	DY	DY	DY	DY	DY	DY	DY

M40

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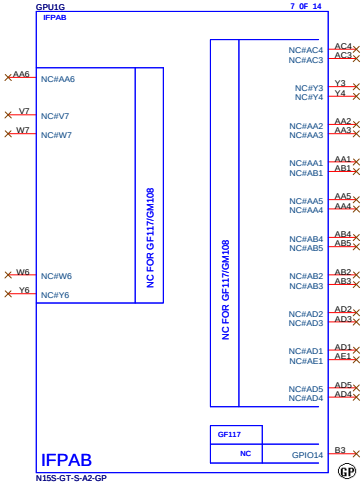
Title: GPU(PEG)

Size: A2 | Document Number: LF15V | Rev: -1

Date: Thursday, July 31, 2014 | Sheet 73 of 102



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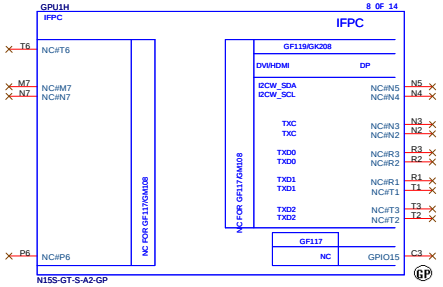

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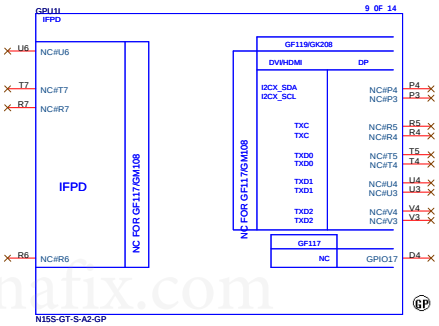

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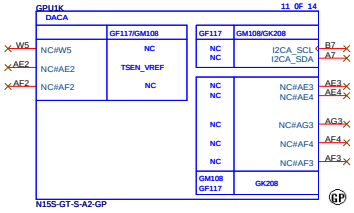

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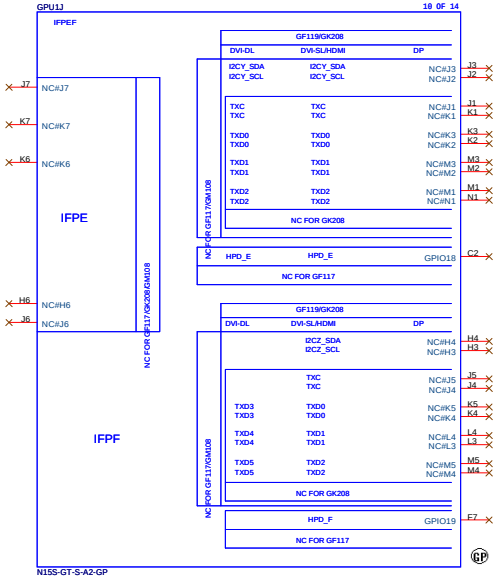

OPS

M40

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Taipei Hsien 221, Taiwan, R.O.C.

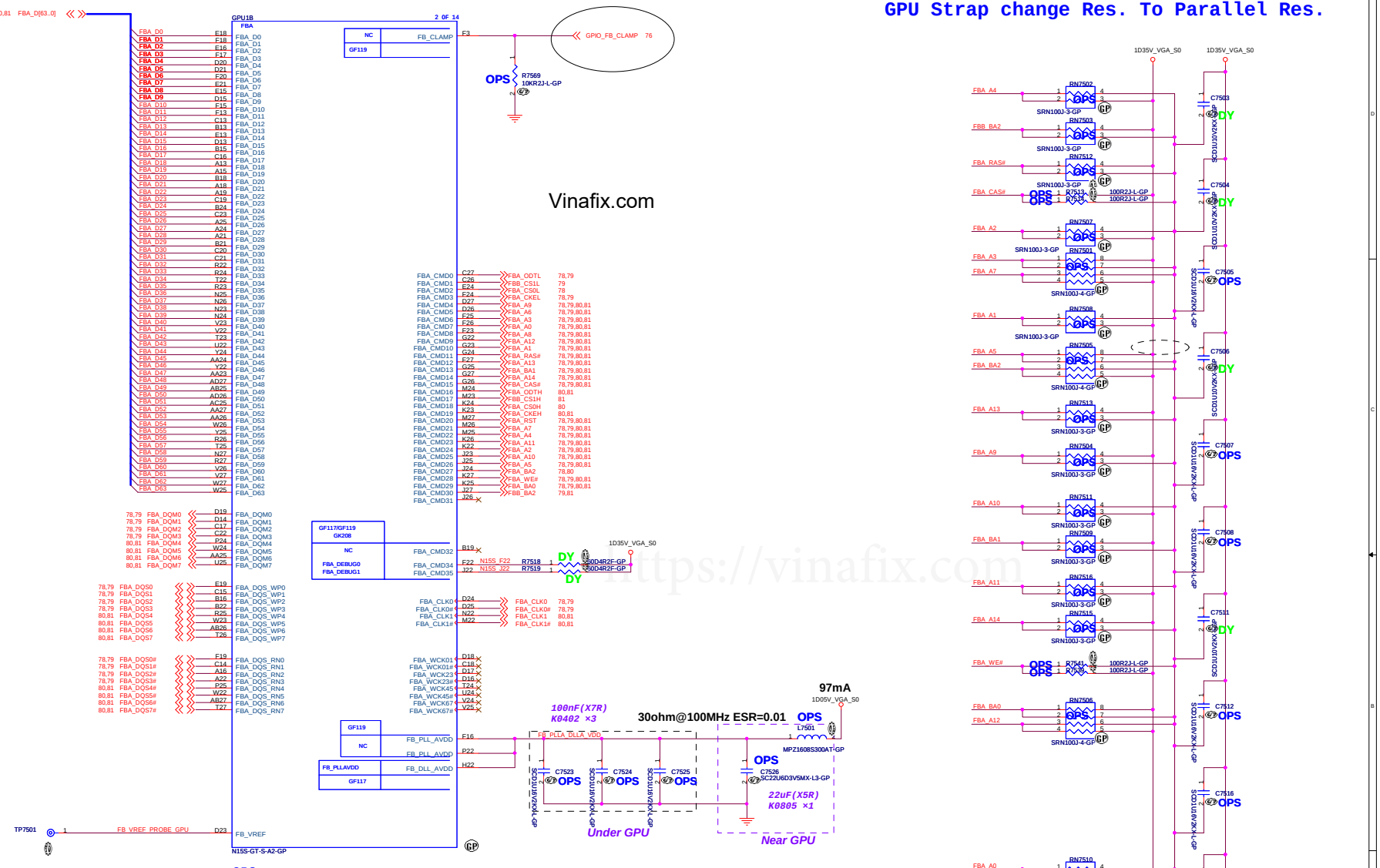
Title: GPU (DIGITALOUT)

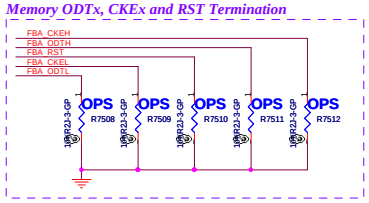
Size: A2 | Document Number: LF15V | Rev: -1

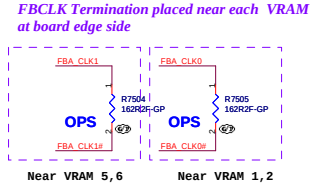
Date: Monday, July 14, 2014 | Sheet 74 of 102

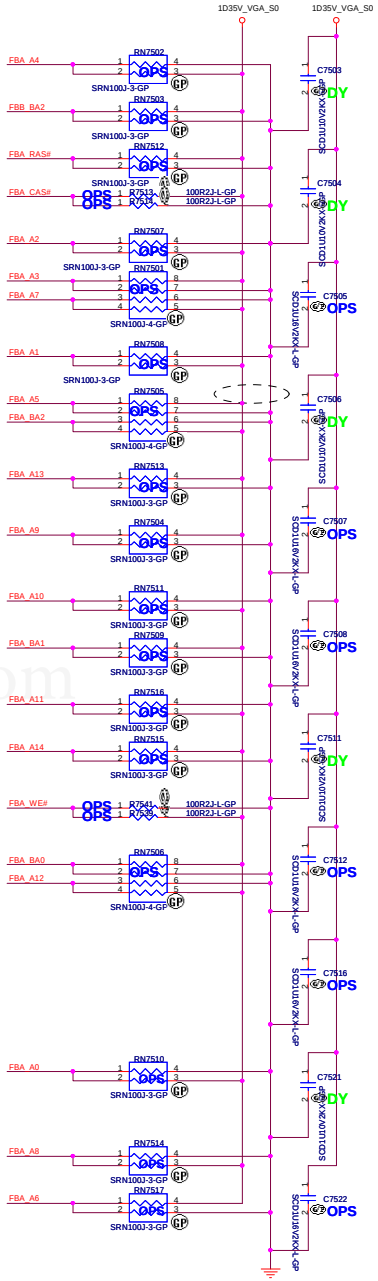
check "EC_FB_CLAMP" is original name

GPU Strap change Res. To Parallel Res.









M40

Wistron Corporation
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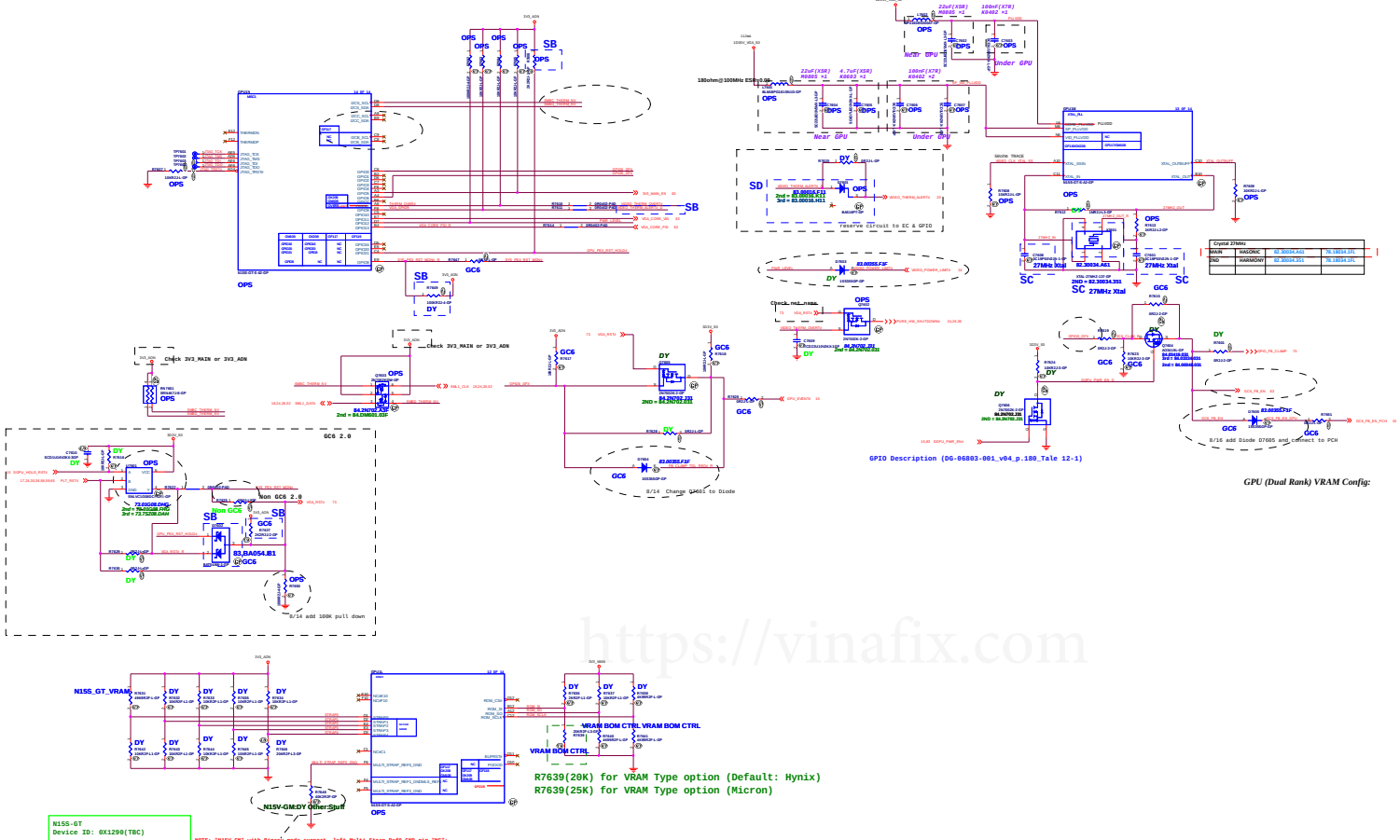
Title: GPU (VRAM I/F)

Size	Document Number	Rev
Custom	LF15V	-1

Date: Thursday, October 30, 2014 Sheet 75 of 102



R7639(20K) for VRAM Type option (Default: Hynix)
R7639(25K) for VRAM Type option (Micron)

N15S-GT
Device ID: 0X1290(TBC)

NOTE: "N15V-GM" with Binary mode support, left Multi_Strap_Ref0_GND pin "NC";
All other N15x GPUs, connect Multi_Strap_Ref0_GND pin to GND per 40.2K resister

NVIDIA TABLE		N15S-GT Hynix 256Mx16 H5TC4G63AFR-11C Device ID 0X1140(TBC)	N15S-GT Micron 256Mx16 MT41J256M16HA-093G:E Device ID 0X1140(TBC)
ROM_SI(Depend on VRAM type)	R7636	DY	DY
	R7639	20Kohm	25Kohm
ROM_SO	R7637	DY	DY
	R7640	4.99Kohm	4.99Kohm
ROM_CLK	R7638	DY	DY
	R7641	4.99Kohm	4.99Kohm
STRAP0	R7631	50Kohm	50Kohm
	R7642	DY	DY
STRAP1	R7632	DY	DY
	R7643	DY	DY
STRAP2	R7633	DY	DY
	R7644	DY	DY
STRAP3	R7635	DY	DY
	R7645	DY	DY
STRAP4	R7634	DY	DY
	R7646	DY	DY

NVVDD Boot Voltage 0.9V

SKU4, SKU5 ------> 4GB (VRAM*8)

SKU2, SKU3 ------> 2GB(VRAM*4)(VRAM1,2,5,6 ASM)

1D35V Compatible VRAM P/N List

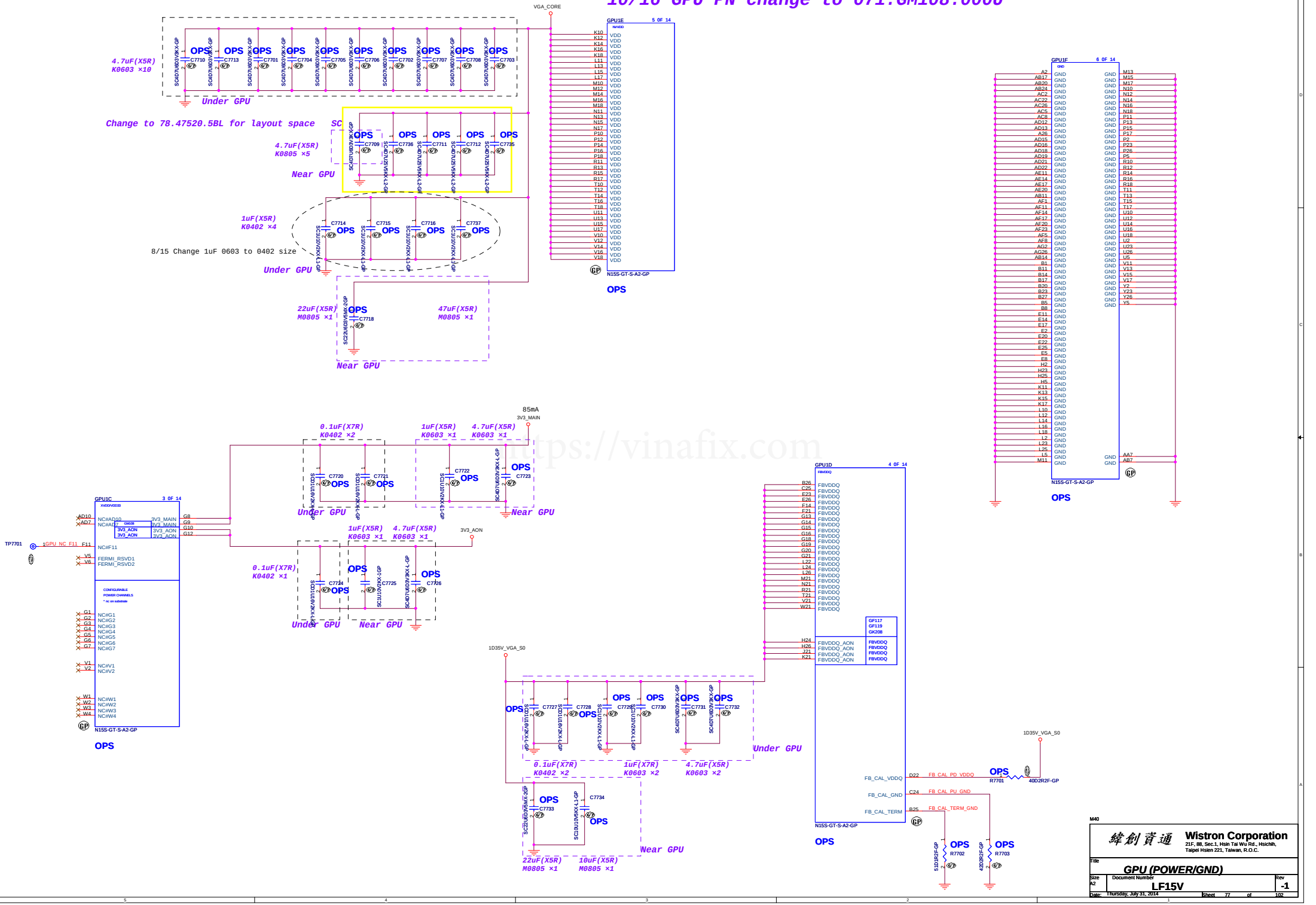
Vendor	Vendor P/N	Lenovo P/N	1 chip VRAM Size
Hynix	H5TC4G63AFR-11C	1100897	512MB
Micron	MT41J256M16HA-093G:E	1101018	512MB

GPU Config:

GPU	SKU1 UMA	SKU2	SKU3	SKU4	SKU5
N15S-GT 071.0N15S.0C0U	NA	STUFF	STUFF	STUFF	STUFF

Wistron Corporation
GPU (GPIO/STRAP)
1D35V
-1

10/16 GPU PN change to 071.GM108.000U



M40

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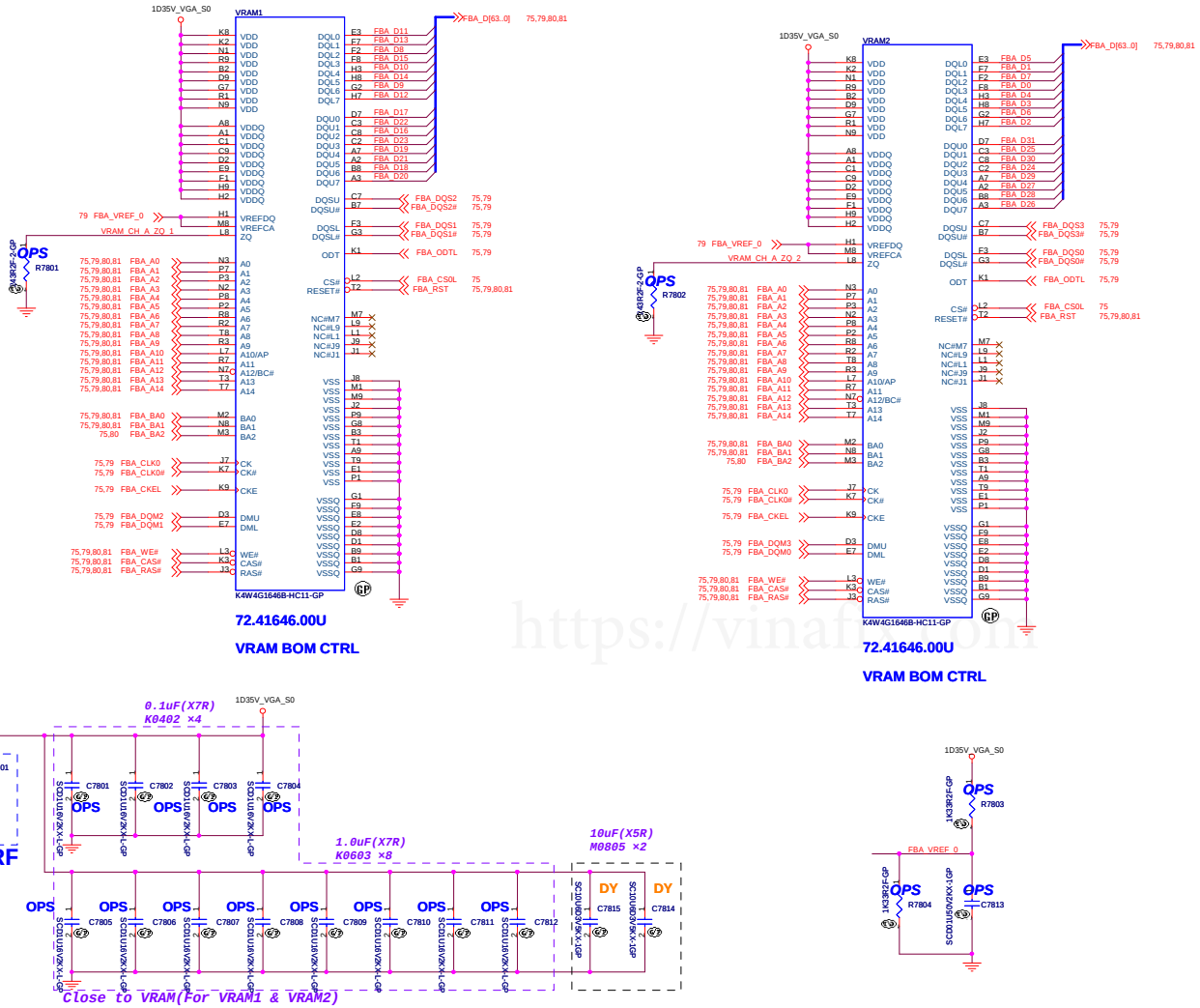
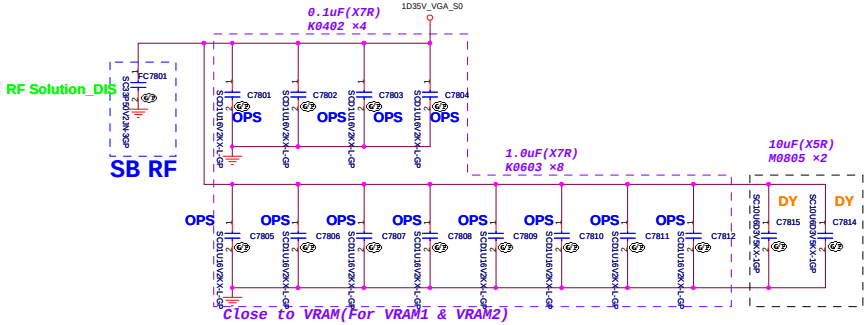
Title: GPU (POWER/GND)

Size	Document Number	Rev
A2	LF15V	-1

Date: Thursday, July 31, 2014 Sheet 77 of 102

Data Bits 31:0 RANK 0





BOM1

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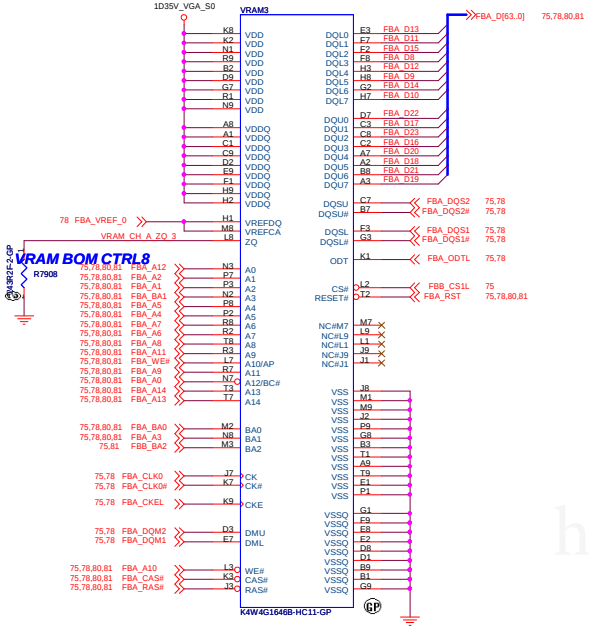
Title: ***GPU-VRAM1,2 (1/4)***

Size	Document Number	Rev
A2	LF15V	-1

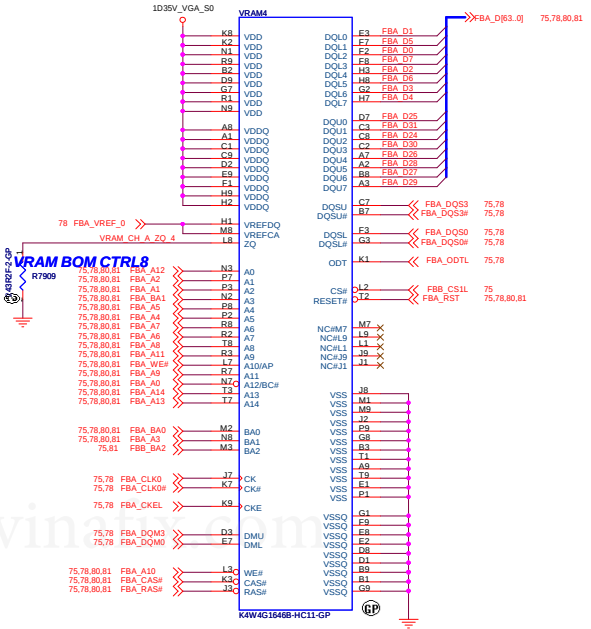
Date: Monday, July 28, 2014 Sheet 78 of 102

Data Bits 31:0 RANK 1



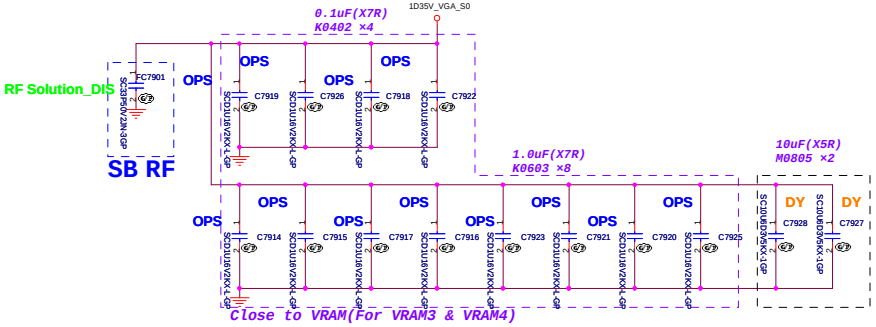
72.41646.00U

VRAM BOM CTRL8



72.41646.00U

VRAM BOM CTRL8



BOM1

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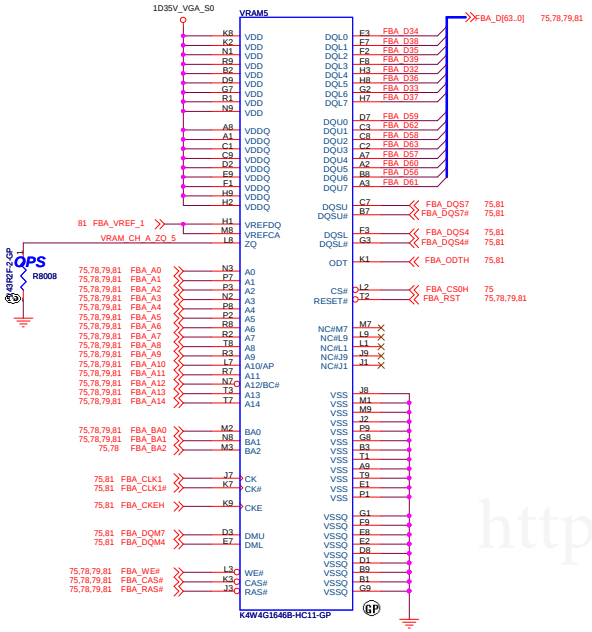
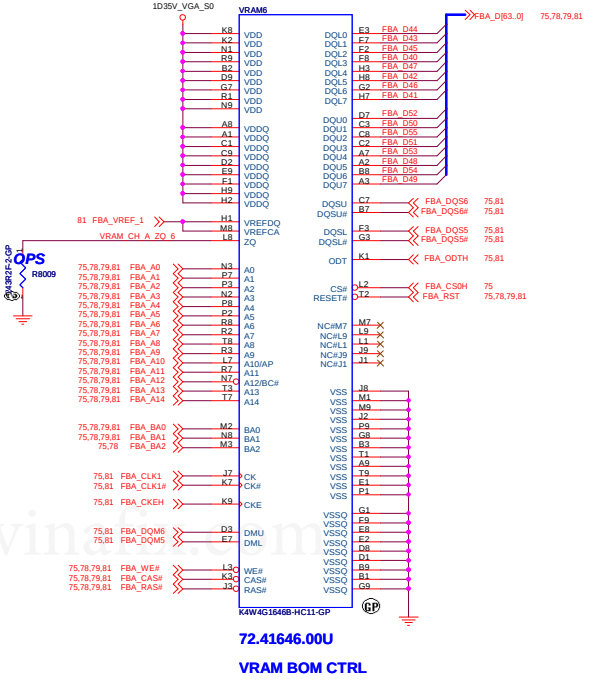
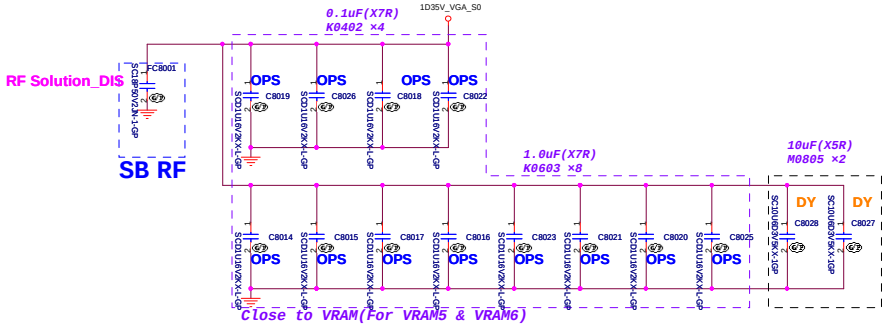
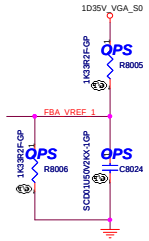
Title: *GPU-VRAM3,4 (2/4)*		
Size: A2	Document Number: LF15V	Rev: -1
Date: Monday, July 28, 2014	Sheet 79 of 102	

Data Bits 63:32 RANK 0









BOM1

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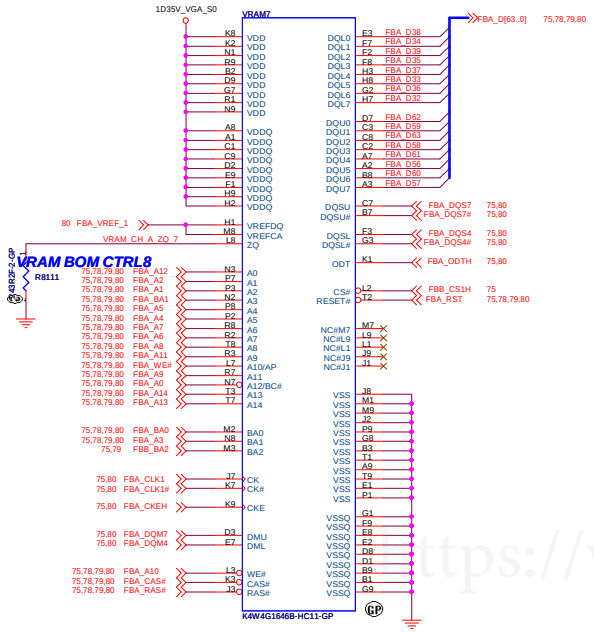
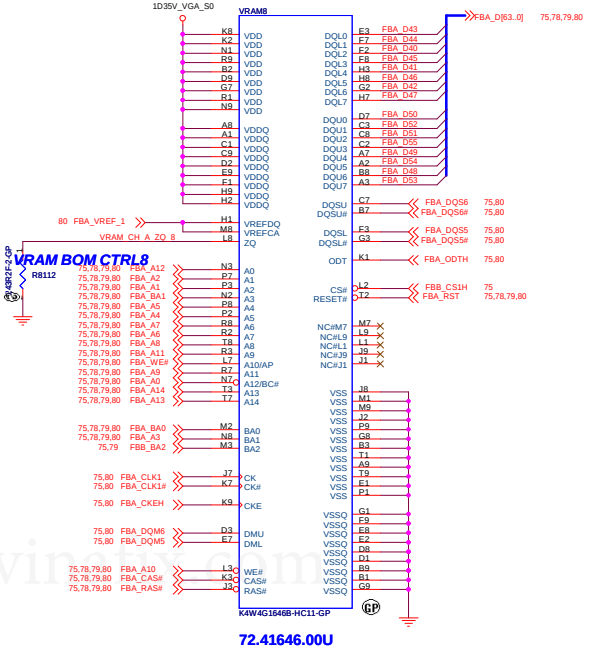
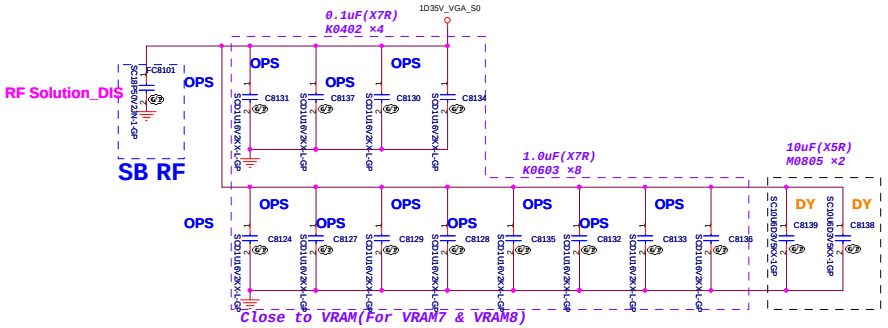
Title: GPU-VRAM5,6 (3/4)		
Size: A2	Document Number: LF15V	Rev: -1
Date: Monday, July 28, 2014	Sheet 80 of 102	

Data Bits 63:32 RANK 1







BOM1

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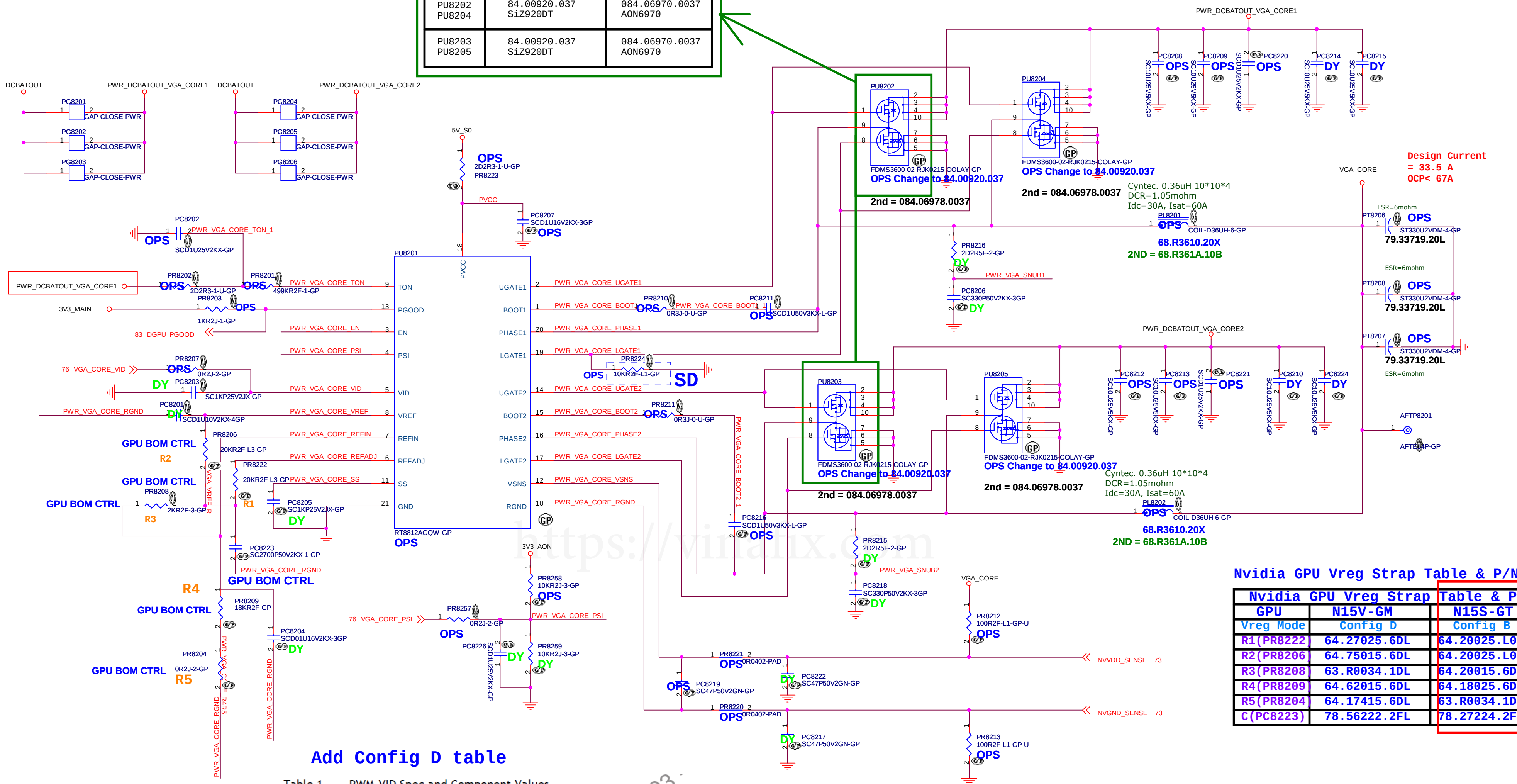
Title: **GPU-VRAM7,8 (4/4)**

Size	Document Number	Rev
A2	LF15V	-1

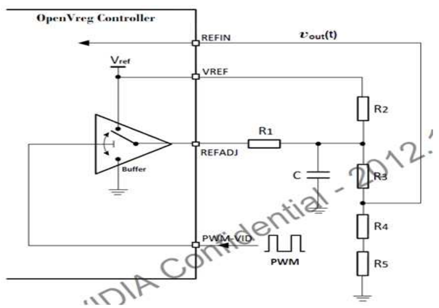
Date: Monday, July 28, 2014 Sheet 81 of 102

	Main source	2nd source
PU8202 PU8204	84.00920.037 SiZ920DT	084.06970.0037 AON6970
PU8203 PU8205	84.00920.037 SiZ920DT	084.06970.0037 AON6970



Nvidia GPU Vreg Strap Table & P/N:

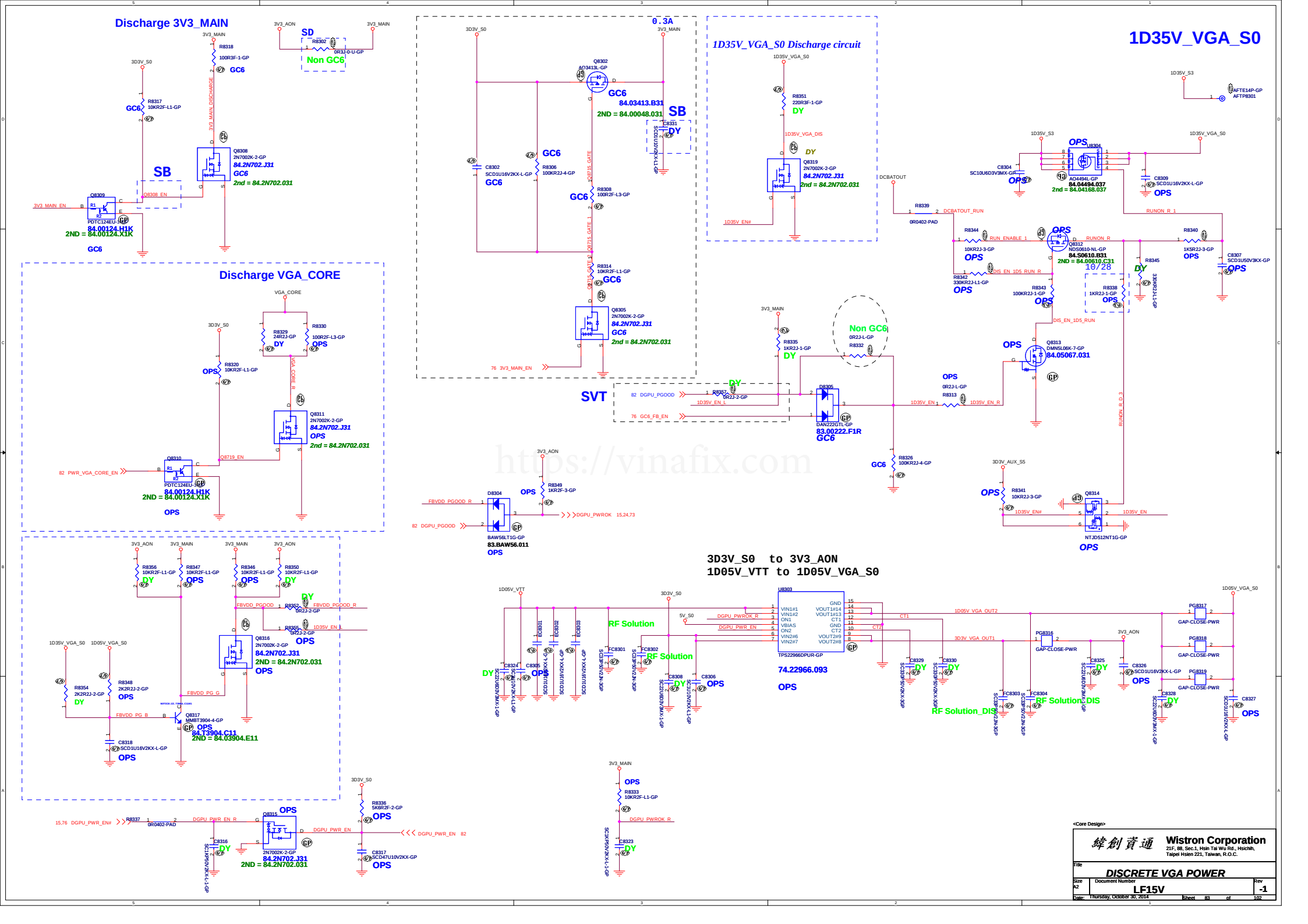
Nvidia GPU Vreg Strap Table & P/N		
GPU	N15V-GM	N15S-GT
Vreg Mode	Config D	Config B
R1(PR8222)	64.27025.6DL	64.20025.L0L
R2(PR8206)	64.75015.6DL	64.20025.L0L
R3(PR8208)	63.R0034.1DL	64.20015.6DL
R4(PR8209)	64.62015.6DL	64.18025.6DL
R5(PR8204)	64.17415.6DL	63.R0034.1DL
C(PC8223)	78.56222.2FL	78.27224.2FL



Add Config D table

Table 1. PWM-VID Spec and Component Values

PWM-VID Specification					
		Config A	Config B	Config C	Config D
Vmin	V	0.6	0.6	0.65	0.9
Vmax	V	1.2	1.2	1.15	1.15
Vboot	V	0.875	0.9	0.9	1.028
Voltage Step Vstep	mV	6.25	6.25	25	12.5
Number of Voltage Levels N	level	96	96	20	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676	0.676
PWM Minimum Pulse Width T_{DMIN}	ns	9.26	9.26	74	74
VID Transient Time T	us	<100	<100	<100	<100
Component Value					
R1 (1%)	KΩ	39	20	39	27
R2 (1%)	KΩ	39	20	30	7.5
R3 (1%)	KΩ	1.5	2	3	0
R4 (1%)	KΩ	30	18	24	6.2
R5 (1%)	KΩ	1.5	0	3	1.74
C	nF	1.5	2.7	1.8	5.6


Discharge 3V3_MAIN
SD
Non GC6
SB
Discharge VGA_CORE
0.3A
SB
SVT
1D35V_VGA_S0 Discharge circuit
1D35V_VGA_S0
3D3V_S0 to 3V3_AON
1D05V_VTT to 1D05V_VGA_S0
RF Solution
RF Solution_DIS
TPS22966DPUR-GP
74.22966.093
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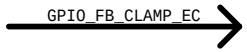
DISCRETE VGA POWER
LF15V
-1
Thursday, October 30, 2014
Sheet 83 of 102

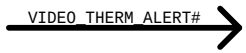
Undefined Sys <-> GPU IO

KBC <-> GPU

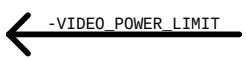


KBC output

KBC input

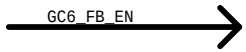


KBC GPIO (Reserved)

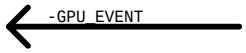


KBC output (Reserved)

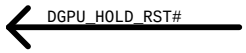
PCH <-> GPU



PCH input



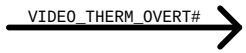
PCH output



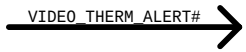
PCH output

PCH output

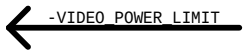
Thermal IC <-> GPU



Thermal IC input(Reserved)



Thermal IC GPIO(Reserved)



Thermal IC output(Reserved)

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Switchable GFX LCD(1/2)*		
Size: A4	Document Number: LF15V	Rev: -1
Date: Monday, July 14, 2014	Sheet 84 of 102	

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Switchable GFX LCD(2/2)

Size	Document Number	Rev
A4	**LF15V**	**-1**

Date: Monday, July 14, 2014 Sheet 85 of 102

H11~H13 change to
when Gerber Out last version circuit

H1~H2 change to
when symbol complete

Structure boss

H4 HOLE237R95-GP ZZ.00PAD.921
H5 HOLE276R178-GP ZZ.00PAD.N11
H6 HOLE276R178-GP ZZ.00PAD.N11
H7 HOLE276R178-GP ZZ.00PAD.N11
H8 HOLE276R178-GP ZZ.00PAD.N11

Stand off

H9 STF236R128H88-GP 34.4LY03.001 DY_NGFF
H10 STF236R128H88-GP 34.4LY03.001
H15 STF237R128H42-GP 34.4GD01.101
H16 STF237R128H42-GP 34.4GD01.101
H17 STF237R128H42-GP 34.4GD01.101 OPS
H18 STF237R128H42-GP 34.4GD01.101
H19 STF237R128H42-GP 34.4GD01.101 OPS

EMI

DCBATOUT
EC8601 SCD1U25V2KX-GP
EC8602 SCD1U25V2KX-GP
EC8603 SCD1U25V2KX-GP
EC8604 SCD1U25V2KX-GP
EC8605 SCD1U25V2KX-GP
EC8606 SCD1U25V2KX-GP

H20 HOLET237B315X315R91-S-GP-U2 ZZ.00PAD.591

1D35V_S3
FC8601 FC8602 FC8603 FC8604 FC8605 FC8606 FC8607 FC8608 FC8609 FC8610
SC18P50V2JN-1-GP
RF Solution

1D35V_VGA_S0
FC8611 FC8612 FC8613 FC8614 FC8615 FC8616 FC8617 FC8618 FC8619
SC18P50V2JN-1-GP
RF Solution_DIS

RF Request

SPR1 SPRING-9-GP 34.49U23.001
SPR2 SPRING-157-GP 34.4YW17.001
SPR3 SPRING-9-GP 34.49U23.001
SPR4 SPRING-9-GP 34.49U23.001
SPR5 SPRING-6-GP 34.13B01.001
SPR6 SPRING-57-GP 34.42T14.002
SPR7 SPRING-57-GP 34.42T14.002

BOM1

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Title: UNUSED PARTS/EMI Capacitors
Size: A3 | Document Number: LF15V | Rev: -1
Date: Thursday, October 30, 2014 | Sheet 86 of 102