ARES/ARTEMIS Block Diagram

SI - PHASE

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

RUN POWER SW PG 36,37

AC/BATT CONNECTOR PG 34

BATT CHARGER PG 34

CPU VR PG 38

DC/DC +3VSUS +5VSUS PG 33

Turion64 Sempron

25W/35W
AMD Socket S1 638P
PG 2,3,4

DDRII-SODIMM1 PG 5 — *DDRII 667mhz*

DDRII-SODIMM2 PG 5 — *DDRII 667mhz*

HT Link

nVIDIA MCP67 MCP67D

Integraded VGA Function
836PIN
PG 5,6,7,8,9,10,11

PCI-E X 1

Mini PCI-E Card
PCI Express Mini Card
(Wireless LAN/WAN)
PG 27

Express Card
(NEW CARD)
PG 28

SIM CARD PG 27

PCI-Express 16X

NVDIA NB8M-64bit
Graphics
PG 12,13,14,15,16,17

Option for 17" only
HDMI CON PG 18

TV_OUT

CRT_OUT

CRT/S-VIDEO PG 19

LVDS(2 Channel)

Panel Connector
15" / 17" PG 18

Cable Docking PG 31

- TV_OUT
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

CLOCK INTERFACE

USB2.0

Bluetooth PG 28

FingrPrint PG 28

USB2.0 I/O Ports X3 PG 26

Camera 1.3MP PG 23

Mini PCI-E Card x1
Express Card x1
Cable Docking x1

Option for 17" only
SATA - HDD PG 26 — *SATA1*

SATA - HDD PG 26 — *SATA0*

PATA- CD-ROM PG 26 — *PATA (66/100/133)*

PCI BUS / 33MHz

LAN

HD AUDIO

Conexant
Venice AMOM
CX20549-12
PG 23

Two-element microphone PG 23

Audio Jacks
-Phone
-SPDIF
-MIC
PG 23

REALTEK
RTL8201CL (10/100)
RTL8211B (10/100/Gigabit)
PG 20

LAN RJ45 PG 20

RICOH
RICOH R5C832
R5C833
PG 21

IEEE1394 CONN PG 21

Memory Card Reader PG 22

TPM SLB9635 PG 28 — *LPC*

Keyboard Touch Pad PG 29

CIR PG 23

Capacitive Sense SW PG 29

ENE KBC
KB3920 Bx
KB3926
PG 30,31

X-Bus

FAN PG 31

SPI ROM PG 30

AUDIO Amplifier TPA0312 PG 25

Jack to Speaker PG 25

MDC DAA CX20548-S PG 24

MODEM RJ 11 PG 20

VAULE DEFINE

A=0603,B=0805,C=1206,F=1%,
OTHER IS 0402
V=Y5V,U=Y5U,R=X5R,S=X6S,
X=X7R,G=COG,O=NPO

EXAMPLE

10R=10ohm(0402)
10A=10ohm(0603)
10B=10ohm(0805)
10C=10ohm(1206)
10/F=10ohm(0402 and 1%)

EXAMPLE

0.1U/16V/R=0.1U/16V/X5R(0402)
0.47UA/10V/X=0.47U/10V/X7R(0603)
10UB/10V/U=10U/10V/Y5U(0805)

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD21	INTA#,INTB#	RICOH832

02

[6] HT_RXD#[15..0] HT_RXD#[15..0]
[6] HT_RXD[15..0] HT_RXD[15..0]
[6] HT_TXD[15..0] HT_TXD[15..0]
[6] HT_TXD#[15..0] HT_TXD#[15..0]

C669 0.22U/6.3V/R
C670 0.22UA/10V/X
C668 4.7UA/6.3V/R
C672 4.7UA/6.3V/R
1.2V_HT
DB2 MODIFY 1107
FOR AMD RECOMMEND

U27A
V_HT0_A1 V_HT0_A2 V_HT0_A3 V_HT0_A4
V_HT0_B1 V_HT0_B2 V_HT0_B3 V_HT0_B4
AE2 AE3 AF4 AE5 1.2V_HT

C673 4.7UA/6.3V/R
C671 180PA/50V/O
C674 180P/50V/O
1.2V_HT
DB2 MODIFY 1106
FOR AMD RECOMMEND

HT_RXD0 HT_RXD1 HT_RXD2 HT_RXD3 HT_RXD4 HT_RXD5 HT_RXD6 HT_RXD7 HT_RXD8 HT_RXD9 HT_RXD10 HT_RXD11 HT_RXD12 HT_RXD13 HT_RXD14 HT_RXD15
HT_TXD0 HT_TXD1 HT_TXD2 HT_TXD3 HT_TXD4 HT_TXD5 HT_TXD6 HT_TXD7 HT_TXD8 HT_TXD9 HT_TXD10 HT_TXD11 HT_TXD12 HT_TXD13 HT_TXD14 HT_TXD15

HT_RXD#0 HT_RXD#1 HT_RXD#2 HT_RXD#3 HT_RXD#4 HT_RXD#5 HT_RXD#6 HT_RXD#7 HT_RXD#8 HT_RXD#9 HT_RXD#10 HT_RXD#11 HT_RXD#12 HT_RXD#13 HT_RXD#14 HT_RXD#15
HT_TXD#0 HT_TXD#1 HT_TXD#2 HT_TXD#3 HT_TXD#4 HT_TXD#5 HT_TXD#6 HT_TXD#7 HT_TXD#8 HT_TXD#9 HT_TXD#10 HT_TXD#11 HT_TXD#12 HT_TXD#13 HT_TXD#14 HT_TXD#15

[6] HT_CPU_UPCLK0 HT_CPU_UPCLK0 J3
[6] HT_CPU_UPCLK1 HT_CPU_UPCLK1 J5
HT_RXCLK0 HT_RXCLK1 HT_TXCLK0 HT_TXCLK1
Y1 Y4 HT_CPU_DWNCLK0 HT_CPU_DWNCLK1
HT_CPU_DWNCLK0 [6] HT_CPU_DWNCLK1 [6]

[6] HT_CPU_UPCLK#0 HT_CPU_UPCLK#0 J2
[6] HT_CPU_UPCLK#1 HT_CPU_UPCLK#1 K5
HT_RXCLK#0 HT_RXCLK#1 HT_TXCLK#0 HT_TXCLK#1
W1 Y3 HT_CPU_DWNCLK#0 HT_CPU_DWNCLK#1
HT_CPU_DWNCLK#0 [6] HT_CPU_DWNCLK#1 [6]

[6] HT_CPU_UPCTL0 HT_CPU_UPCTL0 N1
1.2V_HT R563 49.9/F
HT_CPU_UPCTL1 P3
HT_RXCTL0 HT_RXCTL1 HT_TXCTL0 HT_TXCTL1
R2 T5 HT_CPU_DWNCTL0 HT_CPU_DWNCTL1
HT_CPU_DWNCTL0 [6] T119

[6] HT_CPU_UPCTL0 P1
R562 49.9/F HT_CPU_UPCTL1 P4
HT_RXCTL#0 HT_RXCTL#1 HT_TXCTL#0 HT_TXCTL#1
R3 R5 HT_CPU_DWNCTL#0 HT_CPU_DWNCTL#1
HT_CPU_DWNCTL#0 [6] T118

AMD S1 SOCKET

HT_RXCTL1/HT_RXCRL#1 MUST <1.5" FROM CPU PIN

TEST PU/PL MUST FOLLOW ERRATUM 133

REVISION GUIDE FROM AMD NPT 0Fh CPU

CPUTEST2 CPUTEST3 CPUTEST6 CPUTEST7 CPUTEST8 CPUTEST10 CPUTEST27 CPUTEST28 CPUTEST28#

DB2 MODIFY 1027
REMOVE TEST POINTS FOR AMD RECOMMEND

CPU_THERMDA CPU_THERMDC
FBCLKOUT R43 80.6/F FBCLKOUT#

ROUTE TRACES 80ohm DIFF IMPEDENCE 8/5/20 SPACING

U27E
TEST2 TEST3 THERMDA THERMDC TEST6 TEST7 TEST8 TEST9 TEST10 TEST12 TEST13 TEST14 TEST15 TEST16 TEST17 TEST18 TEST19 TEST20 TEST21 TEST22 TEST23 TEST24 TEST25 TEST25# TEST26 TEST27 TEST28 TEST28# TEST29 TEST29#
RESET# PWROK LDTSTOP#
HTREF0 HTREF1 VDD_FB VDD_FB# VDDIO_FB VDDIO_FB#
CLKIN CLKIN# DBRDY DBREQ# TMS TCK TRST# TDI TDO CPU_PRESENT# PSI# VID0 VID1 VID2 VID3 VID4 VID5 SID SIC PROCHOT# THERMTRIP#
VDDA_1 VDDA_2
RSVD_1 RSVD_2 RSVD_3 RSVD_4 RSVD_5 RSVD_6 RSVD_7 RSVD_8 RSVD_9 RSVD_10 RSVD_11
RSVD_12 RSVD_13 RSVD_14 RSVD_15 RSVD_16 RSVD_17 RSVD_18 RSVD_19 RSVD_20 RSVD_21

AMD S1 SOCKET

W/S= 15 mil/20mil
2.5V
C49 CPU2.5V 0.22U/6.3V/R
L74 48/6A/3216
C684 100U/6.3V/6032

F9 F8 CPU2.5V
C683 4.7UA/6.3V/R
C56 3300P/50V/X
DB2 BOM MODIFY 1107

B7 HTCPU_RST1# R580 *300R 1.8VSUS
A7 HTCPU_PWROK1 R585 *300R 1.8VSUS
F10 HTCPU_STOP1# R571 *300R 1.8VSUS

R6 CPUHTREF0 R565 44.2/F
P6 CPUHTREF1 R564 44.2/F 1.2V_HT
F6 CPU_CORE_FB CPU_CORE_FB [38]
E6 CPU_CORE_FB# CPU_CORE_FB# [38]
W9 CPU_SUS_FB CPU_SUS_FB [37]

CPUCLKIN T130
CPU_DBRDY T126
CPU_DBRDY# T15
CPU_TMS T14
CPU_TCK T12
CPU_TRST# T123
CPU_TDI T128
CPU_TDO T135
CPU_PRES# T131

R552 1K CPU_PSI# [38] 1.8VSUS

CPU_VID0_L R22 *300R
CPU_VID1_L R27 300R
CPU_VID2_L R20 *300R
CPU_VID3_L R28 *300R
CPU_VID4_L R29 *300R
CPU_VID5_L R23 *300R
CPU_SID
CPU_SIC
CPU_PROCHOT#
CPU_THERMIP# R553 300R R561 300R 1.8VSUS

CPUCLKIN C692 3900P/25V/X CPU_CLK [6]
CPUCLKIN# C687 3900P/25V/X CPU_CLK# [6]
CPUCLKIN# R569 169/F CPUCLKIN

KEEP TRACE RESISTOR <0.6" FROM CPU AND TRACE TO AC CAP <1.25"
CPUVID1 PU REQUIRED FOR COMPATIBILITY WITH FUTURE CPU

1.8VSUS
CPU_SID R555 *300R
CPU_SIC R554 *300R
R550 300R

If AMD SI is not used SID can be left, SIC 300ohm to VSS.

CPU THERMAL SENSOR & CONTROL

3V R55 200R 6648VCC C83 0.1U/16V/V
10/20mils
CPU_THERMDA
C102 2200P/50V/X
CPU_THERMDC

3V
R57 2.7K LM86_SMC
R56 2.7K LM86_SMD
R72 10K THERM_ALERT#
[10] THERM_OVER#

U3
SCLK SDA ALERT# OVERT# VCC DXP DXN GND
G781P8
MAX6657,G781P8,W83L771G
ADDRESS: 98H

3V R71 *10K
REMOVE FOR MCP67 INTERNAL PULL-UP

MBCLK [15,29,30,31,34] MBDATA [15,29,30,31,34]
Q2 RHU002N06 Q6 RHU002N06
3V 3V
LM86_SMC LM86_SMC [5] LM86_SMD LM86_SMD [5]

MBCLK/MBDATA NEED PU TO 3VPCU

HT LINK CONTROL LEVEL SHIFTER

MUST KEEP LOW DURING S3-S5 TO MEET HT IO LINK SPEC

1.8VSUS
HTCPU_RST1# R62 0R
[6] HTCPU_RST#
[10,14,30] ECPWROK
U26 *74LVC1G08GW
HTCPU_RST1#
For AMD Warm Reset R63 *0R

HTCPU_PWROK1 R74 0R
[6] HTCPU_PWRGD
ECPWROK
U28 *74LVC1G08GW
HTCPU_PWROK1

HTCPU_STOP1# R568 0R
[6] HTCPU_STOP#
ECPWROK
U25 *74LVC1G08GW
HTCPU_STOP1#

FOLLOW AMD AND NVIDIA RECOMMEND 0904

OVER TEMP CONTROL

PLACE CLOSE CPU
SI MODIFY 1219
MCP67_THERMIP# [6]
R829 0R
Q43 *PDTC144EU
1.8VSUS
CPU_THERMIP#

CPU OR THERM IC THERMTRIP TO SHUTDOWN SYS FROM MCP67

D34 CH500H
R557 10K
Q44 MMBT3904
MCP67_THERMIP#
SYS_SHDN# [30,33]
ECPWROK [10,14,30]
DB2 BOM MODIFY 1101
DB2 MODIFY
1.8VSUS
SI MODIFY 1219

D50 CH500H
R830 10KA 3V
Q73 MMBT3904
D33 CH500H THERM_ALERT#
SYS_SHDN# [30,33]
ECPWROK [10,14,30]
SI MODIFY 1219

CPU PROCHOT INPUT FROM THERMAL IC OR SODIMM SENSOR

[31] EC_PROCHOT# D31 CH500H
[5] DIMM_THEM# D32 *CH500H
MODIFY 0809 [6] MCP67_PROCHOT# D30 *CH500H
THERM_OVER#
3V
Q45 PDTC144EU
CPU_PROCHOT#

1.2V_HT [6,10,11]
1.8VSUS [3,4,5,6,32,36,37]
2.5V [13,32,36]
3V [5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]

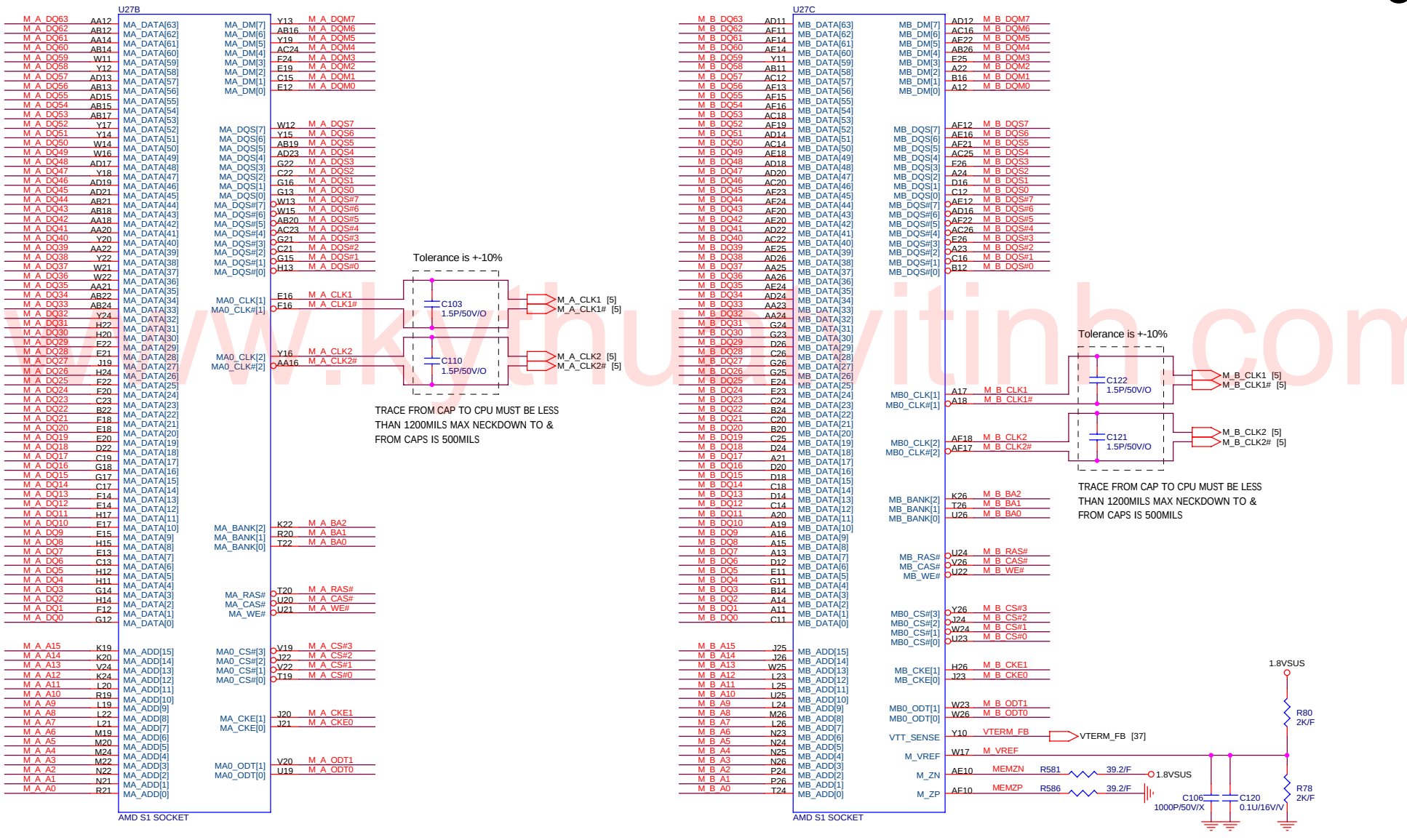
NEED TO CONFIRM NVIDIA FOR THE USAGE CONNECTION TO SB

CPU_VID3_L R37 0A CPU_VID3 [38]
CPU_VID2_L R30 0A CPU_VID2 [38]
CPU_VID4_L R33 0R CPU_VID4 [38]
CPU_VID5_L R34 0A CPU_VID5 [38]
CPU_VID1_L R21 0A CPU_VID1 [38]
CPU_VID0_L R24 0R CPU_VID0 [38]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU (HT_I/F,CTL)	C2A
Date: Friday, December 29, 2006	Sheet 2 of 40	



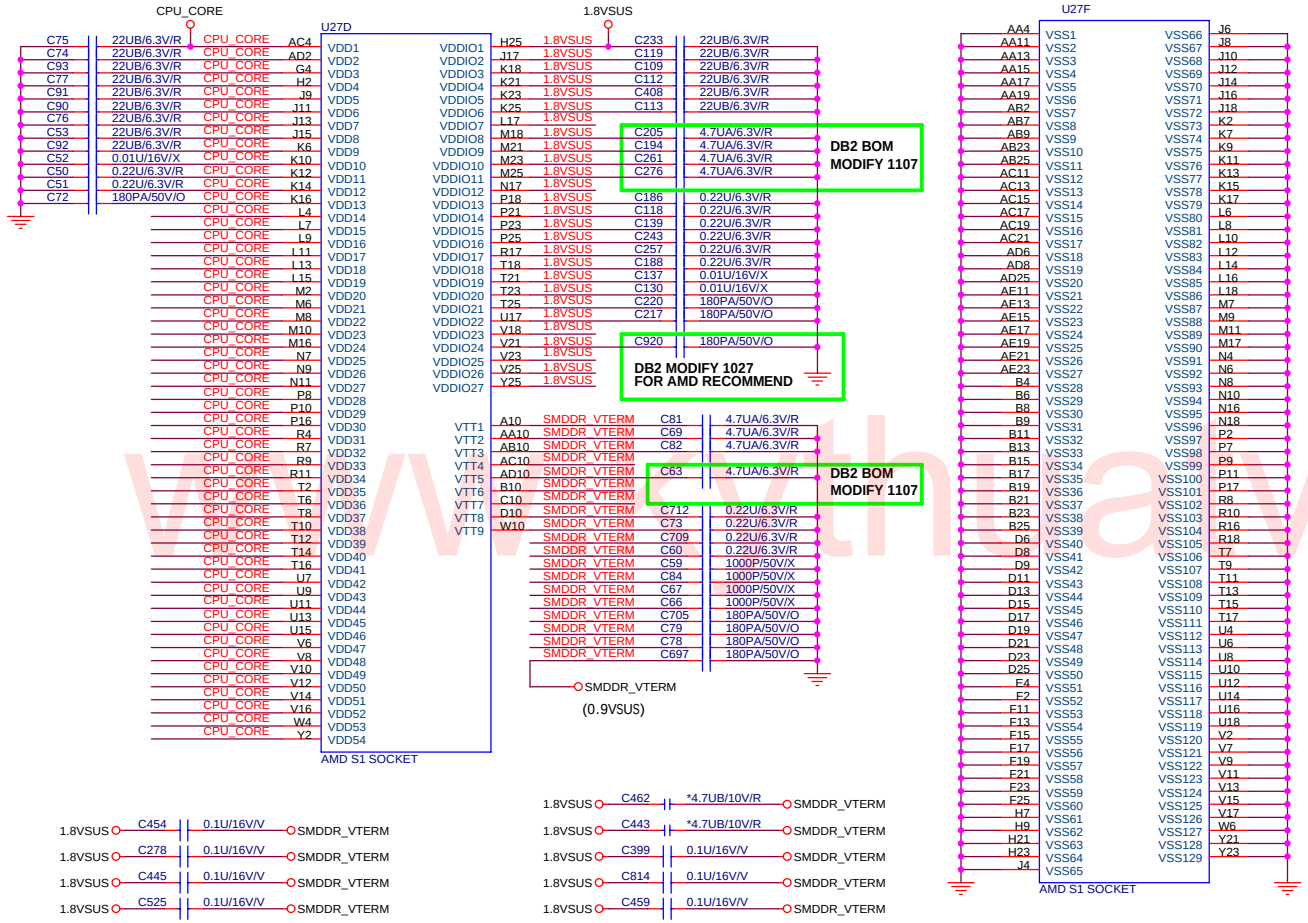
PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU (MEM_I/F)	C2A

NB5/RD2/HW1

Date: Friday, December 29, 2006 Sheet 3 of 40

CPU POWER PLANE AND BY PASS CAP

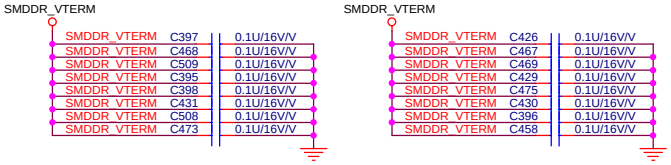


DDR2 TERMINATION BYPASS CAP

04

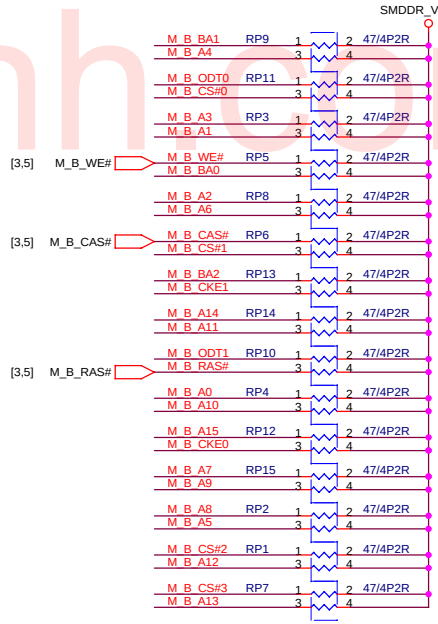
CHANNEL A

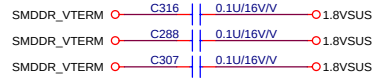
CHANNEL B



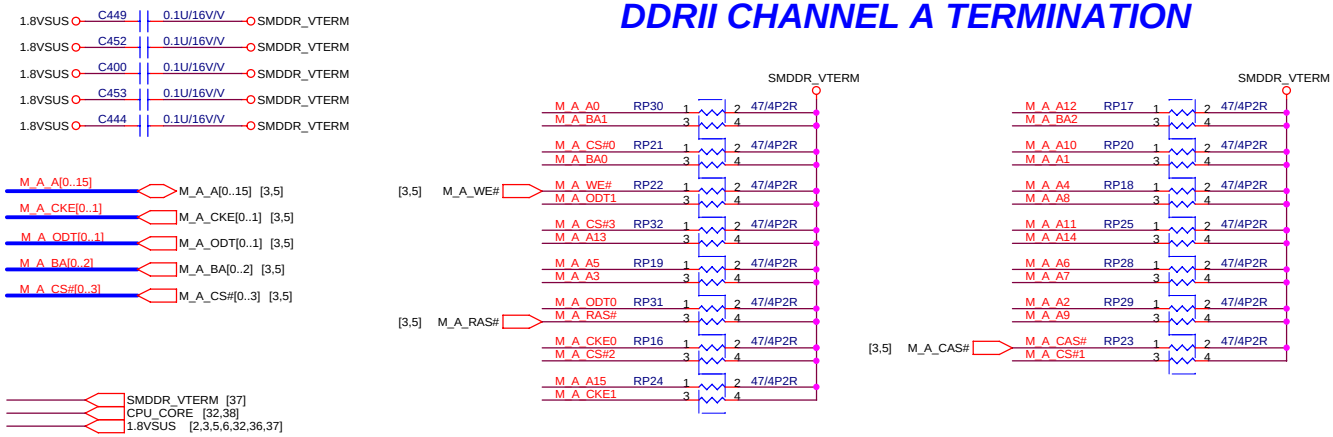
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

DDRII CHANNEL B TERMINATION





DDRII CHANNEL A TERMINATION



NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU (POWER,GND),DDR2_TERM	C2A
Date: Friday, December 29, 2006	Sheet 4 of 40	

M_A_RAS# M_A_CAS# M_A_WE# → M_A_RAS# [3,4] M_A_CAS# [3,4] M_A_WE# [3,4]
M_A_CLK1 M_A_CLK1# M_A_CLK2 M_A_CLK2# → M_A_CLK1 [3] M_A_CLK1# [3] M_A_CLK2 [3] M_A_CLK2# [3]
M_A_BA[0..2] → M_A_BA[0..2] [3,4]
M_A_CS#[0..3] → M_A_CS#[0..3] [3,4]
M_A_CKE[0..1] → M_A_CKE[0..1] [3,4]
M_A_ODT[0..1] → M_A_ODT[0..1] [3,4]
M_A_DQ[0..63] → M_A_DQ[0..63] [3]
M_A_A[15..0] → M_A_A[15..0] [3,4]
M_A_DQM[0..7] → M_A_DQM[0..7] [3]
M_A_DQS[0..7] → M_A_DQS[0..7] [3]
M_A_DQS#[0..7] → M_A_DQS#[0..7] [3]

M_B_RAS# M_B_CAS# M_B_WE# → M_B_RAS# [3,4] M_B_CAS# [3,4] M_B_WE# [3,4]
M_B_CLK1 M_B_CLK1# M_B_CLK2 M_B_CLK2# → M_B_CLK1 [3] M_B_CLK1# [3] M_B_CLK2 [3] M_B_CLK2# [3]
M_B_BA[0..2] → M_B_BA[0..2] [3,4]
M_B_CS#[0..3] → M_B_CS#[0..3] [3,4]
M_B_CKE[0..1] → M_B_CKE[0..1] [3,4]
M_B_ODT[0..1] → M_B_ODT[0..1] [3,4]
M_B_DQ[0..63] → M_B_DQ[0..63] [3]
M_B_A[0..15] → M_B_A[0..15] [3,4]
M_B_DQM[0..7] → M_B_DQM[0..7] [3]
M_B_DQS[0..7] → M_B_DQS[0..7] [3]
M_B_DQS#[0..7] → M_B_DQS#[0..7] [3]

CKE 0,1

CN28A
2-1734073-1
PC2100 DDR2 SDRAM SO-DIMM (200P)
HEIGHT=9.2mm

M_A_DQ5	5	DQ0	DQ32	123	M_A_DQ32
M_A_DQ1	7	DQ1	DQ33	125	M_A_DQ36
M_A_DQ2	17	DQ2	DQ34	135	M_A_DQ34
M_A_DQ3	19	DQ3	DQ35	137	M_A_DQ37
M_A_DQ0	4	DQ4	DQ36	124	M_A_DQ33
M_A_DQ4	6	DQ5	DQ37	126	M_A_DQ38
M_A_DQ6	14	DQ6	DQ38	134	M_A_DQ39
M_A_DQ7	16	DQ7	DQ39	136	M_A_DQ35
M_A_DQ9	23	DQ8	DQ40	141	M_A_DQ40
M_A_DQ8	25	DQ9	DQ41	143	M_A_DQ41
M_A_DQ10	35	DQ10	DQ42	151	M_A_DQ42
M_A_DQ14	37	DQ11	DQ43	153	M_A_DQ46
M_A_DQ13	20	DQ12	DQ44	140	M_A_DQ44
M_A_DQ12	22	DQ13	DQ45	142	M_A_DQ45
M_A_DQ15	36	DQ14	DQ46	152	M_A_DQ43
M_A_DQ11	38	DQ15	DQ47	154	M_A_DQ47
M_A_DQ17	43	DQ16	DQ48	157	M_A_DQ55
M_A_DQ21	45	DQ17	DQ49	159	M_A_DQ54
M_A_DQ18	55	DQ18	DQ50	173	M_A_DQ49
M_A_DQ16	57	DQ19	DQ51	175	M_A_DQ52
M_A_DQ20	44	DQ20	DQ52	158	M_A_DQ48
M_A_DQ19	46	DQ21	DQ53	160	M_A_DQ53
M_A_DQ22	56	DQ22	DQ54	174	M_A_DQ50
M_A_DQ23	58	DQ23	DQ55	176	M_A_DQ51
M_A_DQ24	61	DQ24	DQ56	179	M_A_DQ57
M_A_DQ25	63	DQ25	DQ57	181	M_A_DQ61
M_A_DQ27	73	DQ26	DQ58	189	M_A_DQ63
M_A_DQ30	75	DQ27	DQ59	191	M_A_DQ62
M_A_DQ28	62	DQ28	DQ60	180	M_A_DQ56
M_A_DQ29	64	DQ29	DQ61	182	M_A_DQ60
M_A_DQ26	74	DQ30	DQ62	192	M_A_DQ59
M_A_DQ31	76	DQ31	DQ63	194	M_A_DQ58
M_A_A0	102	A0	DM0	10	M_A_DQM0
M_A_A1	101	A1	DM1	26	M_A_DQM1
M_A_A2	100	A2	DM2	52	M_A_DQM2
M_A_A3	99	A3	DM3	67	M_A_DQM3
M_A_A4	98	A4	DM4	130	M_A_DQM4
M_A_A5	97	A5	DM5	147	M_A_DQM5
M_A_A6	94	A6	DM6	170	M_A_DQM6
M_A_A7	92	A7	DM7	185	M_A_DQM7
M_A_A8	93	A8	DQS0	13	M_A_DQS0
M_A_A9	91	A9	DQS0	11	M_A_DQS#0
M_A_A10	105	A10/AP	DQS1	31	M_A_DQS1
M_A_A11	90	A11	DQS1	29	M_A_DQS#1
M_A_A12	89	A12	DQS2	51	M_A_DQS2
			DQS2	49	M_A_DQS#2
M_A_BA0	107	BA0	DQS3	70	M_A_DQS3
M_A_BA1	106	BA1	DQS3	68	M_A_DQS#3
M_A_BA2	85	NC/BA2	DQS4	131	M_A_DQS4
			DQS4	129	M_A_DQS#4
M_A_CLK1	30		DQS5	148	M_A_DQS5
M_A_CLK1#	32	CLK0	DQS5	146	M_A_DQS#5
		CLK0	DQS6	169	M_A_DQS6
M_A_CLK2	164		DQS6	167	M_A_DQS#6
M_A_CLK2#	166	CLK1	DQS7	188	M_A_DQS7
		CKL1	DQS7	186	M_A_DQS#7
DDR_SMBCLK	197	SCL			
DDR_SMBDTA	195	SDA	CS0	110	M_A_CS#0
DIM1_SA0	198	SA0	CS1	115	M_A_CS#1
DIM1_SA1	200	SA1	RAS	108	M_A_RAS#
			CAS	113	M_A_CAS#
3V	199	VDDSPD	WE	109	M_A_WE#
			CKE0	79	M_A_CKE0
			CKE1	80	M_A_CKE1

CKE 2,3

CN26A
1565917-4
PC2100 DDR2 SDRAM SO-DIMM (200P)
HEIGHT=5.2mm

M_B_DQ1	5	DQ0	DQ32	123	M_B_DQ36
M_B_DQ4	7	DQ1	DQ33	125	M_B_DQ37
M_B_DQ3	17	DQ2	DQ34	135	M_B_DQ38
M_B_DQ2	19	DQ3	DQ35	137	M_B_DQ34
M_B_DQ0	4	DQ4	DQ36	124	M_B_DQ32
M_B_DQ5	6	DQ5	DQ37	126	M_B_DQ33
M_B_DQ7	14	DQ6	DQ38	134	M_B_DQ39
M_B_DQ6	16	DQ7	DQ39	136	M_B_DQ35
M_B_DQ9	23	DQ8	DQ40	141	M_B_DQ44
M_B_DQ8	25	DQ9	DQ41	143	M_B_DQ41
M_B_DQ14	35	DQ10	DQ42	151	M_B_DQ47
M_B_DQ15	37	DQ11	DQ43	153	M_B_DQ46
M_B_DQ12	20	DQ12	DQ44	140	M_B_DQ40
M_B_DQ13	22	DQ13	DQ45	142	M_B_DQ45
M_B_DQ10	36	DQ14	DQ46	152	M_B_DQ42
M_B_DQ11	38	DQ15	DQ47	154	M_B_DQ43
M_B_DQ17	43	DQ16	DQ48	157	M_B_DQ55
M_B_DQ20	45	DQ17	DQ49	159	M_B_DQ54
M_B_DQ19	55	DQ18	DQ50	173	M_B_DQ53
M_B_DQ18	57	DQ19	DQ51	175	M_B_DQ48
M_B_DQ16	44	DQ20	DQ52	158	M_B_DQ51
M_B_DQ21	46	DQ21	DQ53	160	M_B_DQ50
M_B_DQ22	56	DQ22	DQ54	174	M_B_DQ49
M_B_DQ23	58	DQ23	DQ55	176	M_B_DQ52
M_B_DQ24	61	DQ24	DQ56	179	M_B_DQ57
M_B_DQ25	63	DQ25	DQ57	181	M_B_DQ60
M_B_DQ30	73	DQ26	DQ58	189	M_B_DQ62
M_B_DQ31	75	DQ27	DQ59	191	M_B_DQ59
M_B_DQ28	62	DQ28	DQ60	180	M_B_DQ61
M_B_DQ29	64	DQ29	DQ61	182	M_B_DQ56
M_B_DQ27	74	DQ30	DQ62	192	M_B_DQ58
M_B_DQ26	76	DQ31	DQ63	194	M_B_DQ63
M_B_A0	102	A0	DM0	10	M_B_DQM0
M_B_A1	101	A1	DM1	26	M_B_DQM1
M_B_A2	100	A2	DM2	52	M_B_DQM2
M_B_A3	99	A3	DM3	67	M_B_DQM3
M_B_A4	98	A4	DM4	130	M_B_DQM4
M_B_A5	97	A5	DM5	147	M_B_DQM5
M_B_A6	94	A6	DM6	170	M_B_DQM6
M_B_A7	92	A7	DM7	185	M_B_DQM7
M_B_A8	93	A8	DQS0	13	M_B_DQS0
M_B_A9	91	A9	DQS0	11	M_B_DQS#0
M_B_A10	105	A10/AP	DQS1	31	M_B_DQS1
M_B_A11	90	A11	DQS1	29	M_B_DQS#1
M_B_A12	89	A12	DQS2	51	M_B_DQS2
			DQS2	49	M_B_DQS#2
M_B_BA0	107	BA0	DQS3	70	M_B_DQS3
M_B_BA1	106	BA1	DQS3	68	M_B_DQS#3
M_B_BA2	85	NC/BA2	DQS4	131	M_B_DQS4
			DQS4	129	M_B_DQS#4
M_B_CLK1	30		DQS5	148	M_B_DQS5
M_B_CLK1#	32	CLK0	DQS5	146	M_B_DQS#5
		CLK0	DQS6	169	M_B_DQS6
M_B_CLK2	164		DQS6	167	M_B_DQS#6
M_B_CLK2#	166	CLK1	DQS7	188	M_B_DQS7
		CKL1	DQS7	186	M_B_DQS#7
DDR_SMBCLK	197	SCL			
DDR_SMBDTA	195	SDA	CS0	110	M_B_CS#0
DIM2_SA0	198	SA0	CS1	115	M_B_CS#1
DIM2_SA1	200	SA1	RAS	108	M_B_RAS#
			CAS	113	M_B_CAS#
3V	199	VDDSPD	WE	109	M_B_WE#
			CKE0	79	M_B_CKE0
			CKE1	80	M_B_CKE1

SMDDR_VREF_DIMM 1 → VREF
C526 C819 C840 C813 C815 C402 C817 C821 C822 C824 C816: 2.2UA/6.3V/R 1.8VSUS 81 / 2.2UA/6.3V/R 1.8VSUS 82 / 2.2UA/6.3V/R 1.8VSUS 87 / 0.1U/16V/V 1.8VSUS 88 / 0.1U/16V/V 1.8VSUS 95 / 0.1U/16V/V 1.8VSUS 96 / 0.1U/16V/V 1.8VSUS 103 / 0.1U/16V/V 1.8VSUS 104 / 0.1U/16V/V 1.8VSUS 111 / 0.1U/16V/V 1.8VSUS 112 / 0.1U/16V/V 1.8VSUS 117
1.8VSUS 118
M_A_ODT0 114 → ODT0
M_A_ODT1 119 → ODT1
M_A_CS#2 83 → NC_1
M_A_A15 84 → NC_2
M_A_A14 86 → NC_3
M_A_A13 116 → NC_4/A15
M_A_CS#3 120 → NC_5/A14
163 → NC_6/A13
NC_7
NC_8
VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58
VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_59
VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7 VDD_8 VDD_9 VDD_10 VDD_11 VDD_12

CN28B
2-1734073-1
PC2100 DDR2 SDRAM SO-DIMM (200P)

SMDDR_VREF_DIMM 1 → VREF
C820 C818 C466 C838 C839 C836 C835 C401 C450 C823 C837: 2.2UA/6.3V/R 1.8VSUS 81 / 2.2UA/6.3V/R 1.8VSUS 82 / 2.2UA/6.3V/R 1.8VSUS 87 / 0.1U/16V/V 1.8VSUS 88 / 0.1U/16V/V 1.8VSUS 95 / 0.1U/16V/V 1.8VSUS 96 / 0.1U/16V/V 1.8VSUS 103 / 0.1U/16V/V 1.8VSUS 104 / 0.1U/16V/V 1.8VSUS 111 / 0.1U/16V/V 1.8VSUS 112 / 0.1U/16V/V 1.8VSUS 117
1.8VSUS 118
M_B_ODT0 114 → ODT0
M_B_ODT1 119 → ODT1
M_B_CS#2 83 → NC_1
M_B_A15 84 → NC_2
M_B_A14 86 → NC_3
M_B_A13 116 → NC_4/A15
M_B_CS#3 120 → NC_5/A14
163 → NC_6/A13
NC_7
NC_8
VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58
VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_59
VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7 VDD_8 VDD_9 VDD_10 VDD_11 VDD_12

CN26B
1565917-4

SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.

Close DDR2 socket
3V
C520 0.1U/16V/V 3V — 3V C507 *2.2UA/6.3V/R
C483 2.2UA/6.3V/R — C463 0.1U/16V/V

SMDDR_VREF_DIMM — R259 *0R — SMDDR_VREF [37]
R258 2K/F — R253 2K/F — 1.8VSUS
C474 0.1U/16V/V — SMDDR_VREF_DIMM — C457 0.1U/16V/V
C407 2.2UA/6.3V/R — SMDDR_VREF_DIMM — C472 2.2UA/6.3V/R

SMDDR_VREF_DIMM :
TRACE WIDTH > 20 MIL
PUT BYPASS CAP ON EACH DIMM

R320 10K DIM1_SA0
R321 10K DIM1_SA1
SMbus address A0

DIM2_SA0 R280 10K 3V
DIM2_SA1 R266 10K
SMbus address A2

DDR_SMBDTA 1 — Q13 2N7002E 3 — CGDAT_SMB [10]
2 — 3V
DDR_SMBCLK 1 — Q11 2N7002E 3 — CGCLK_SMB [10]
2 — 3V

DDR_SMBDTA R281 2.2K 3V
DDR_SMBCLK R282 2.2K

Address:92h
U34
3V
3V — 7 A0, 6 A1, 5 A2
+VS — 8 — C804 *0.1U/16V/V
O.S — 3 — DIMM_THEM# — DIMM_THEM# [2]
[2] LM86_SMD — LM86_SMD 1 SDA
[2] LM86_SMC — LM86_SMC 2 SCL
GND — 4
*G751 (LM75CIMM3)

3V R673 *10K DIMM_THEM#

1.8VSUS [2,3,4,6,32,36,37]
3V [2,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]

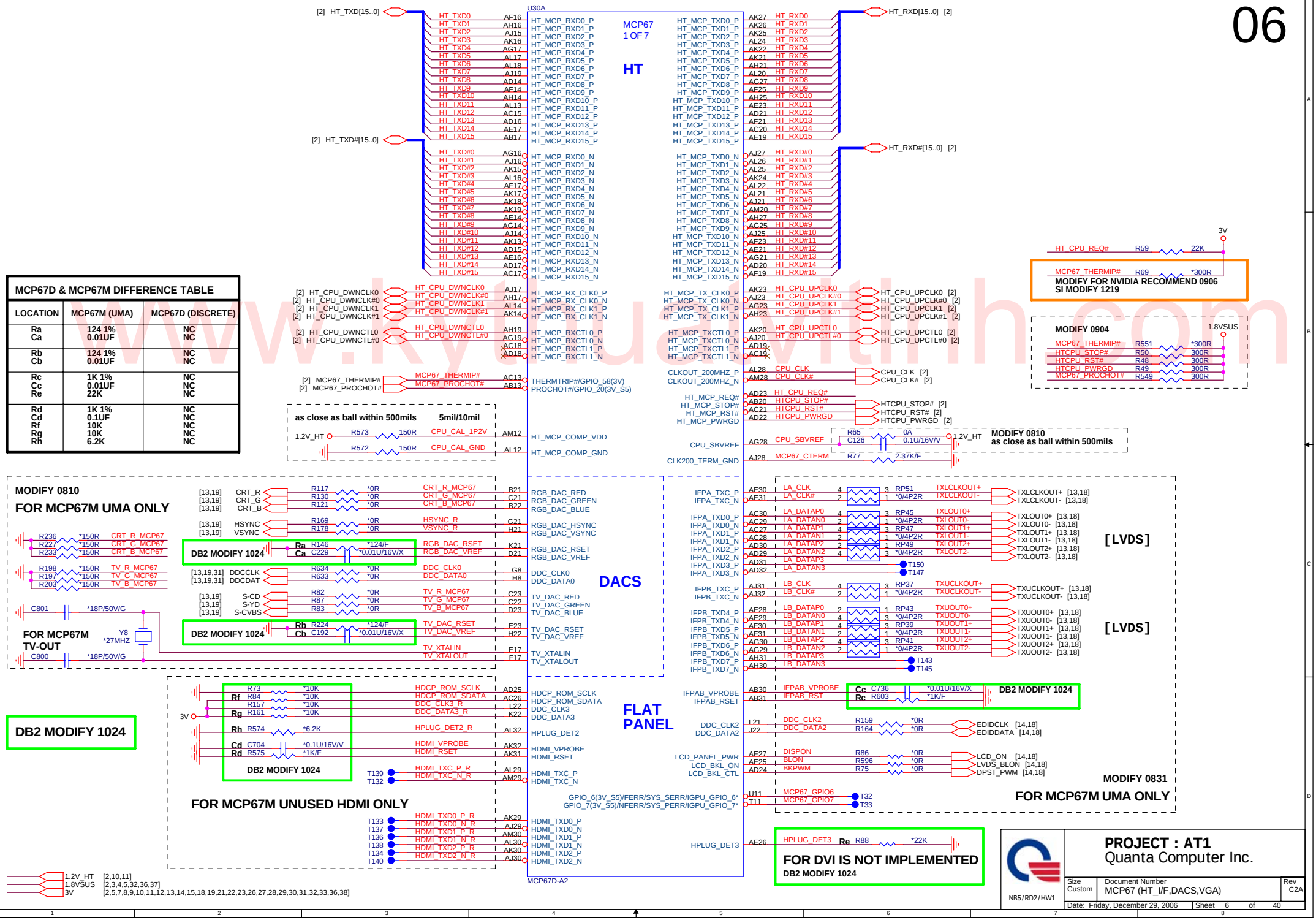
NB5/RD2/HW1

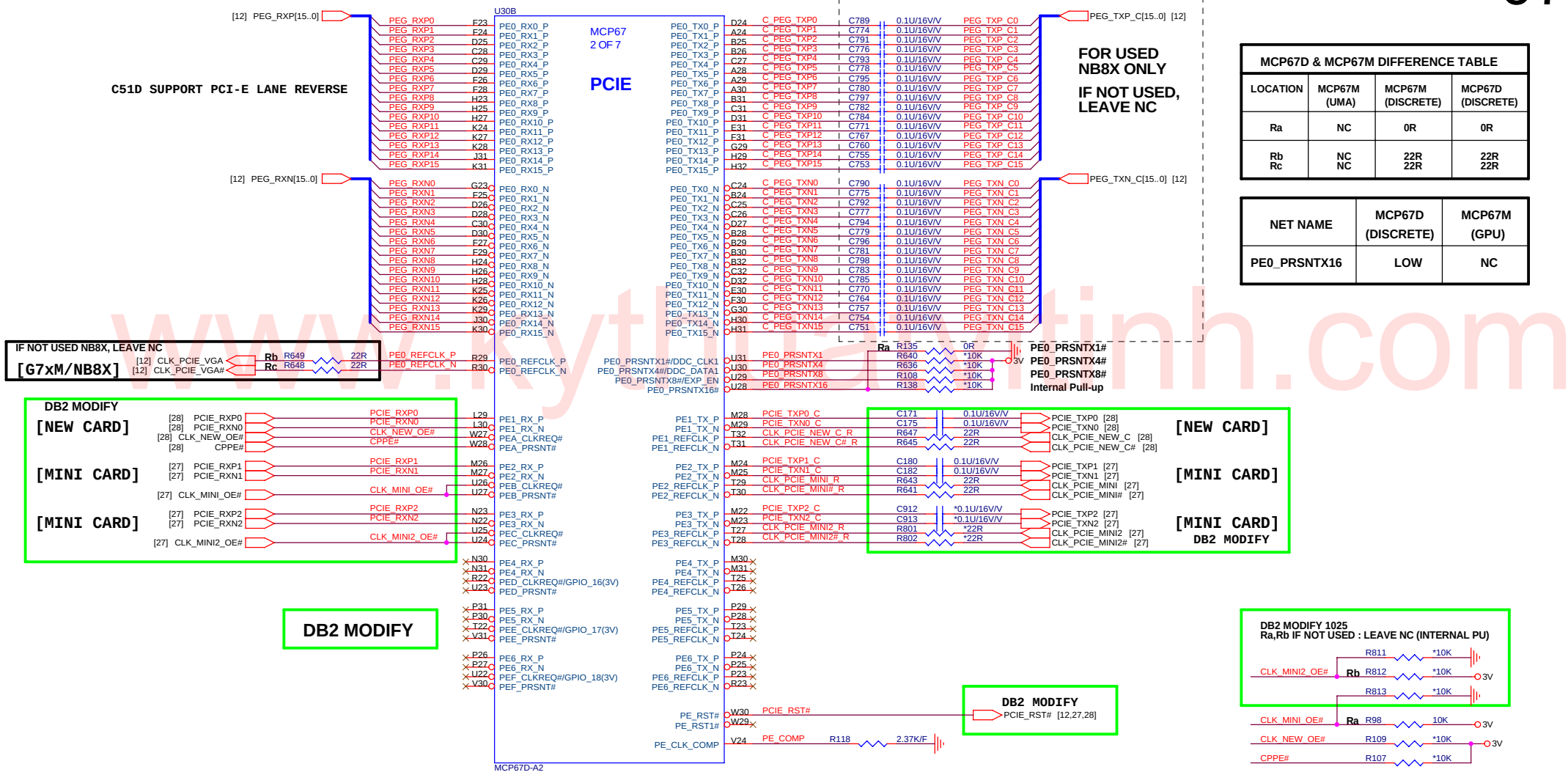
PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR SO-DIMMx2 (200P)	C2A

Date: Friday, December 29, 2006 Sheet 5 of 40

MCP67D & MCP67M DIFFERENCE TABLE		
LOCATION	MCP67M (UMA)	MCP67D (DISCRETE)
Ra Ca	124 1% 0.01UF	NC NC
Rb Cb	124 1% 0.01UF	NC NC
Rc Cc Re	1K 1% 0.01UF 22K	NC NC NC
Rd Cd Rf Rg Rh	1K 1% 0.1UF 10K 10K 6.2K	NC NC NC NC NC





MCP67D & MCP67M DIFFERENCE TABLE			
LOCATION	MCP67M (UMA)	MCP67M (DISCRETE)	MCP67D (DISCRETE)
Ra	NC	0R	0R
Rb Rc	NC NC	22R 22R	22R 22R

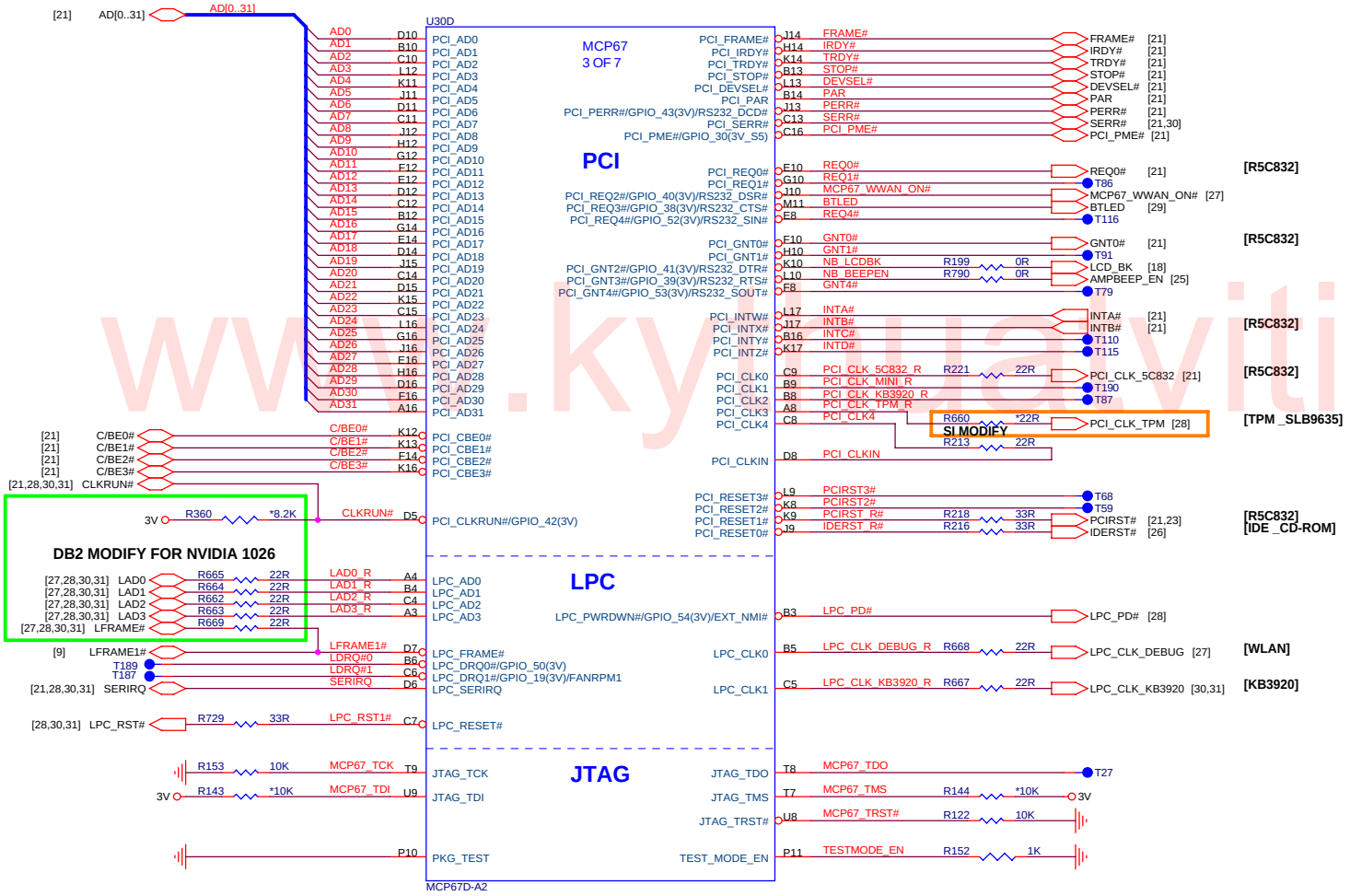
NET NAME	MCP67D (DISCRETE)	MCP67M (GPU)
PE0_PRSNTX16	LOW	NC

NB5/RD2/HW1

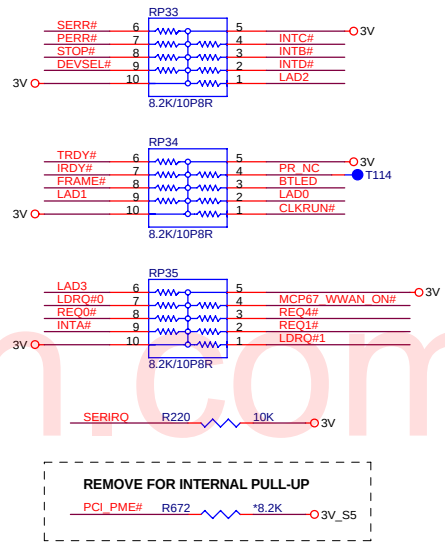
PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MCP67 (PCI-E_I/F)	C2A

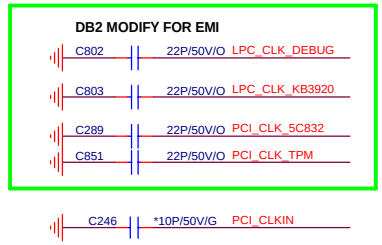
Date: Friday, December 29, 2006 Sheet 7 of 40



PCI/LPC PULL-UP



CLOCK BYPASS



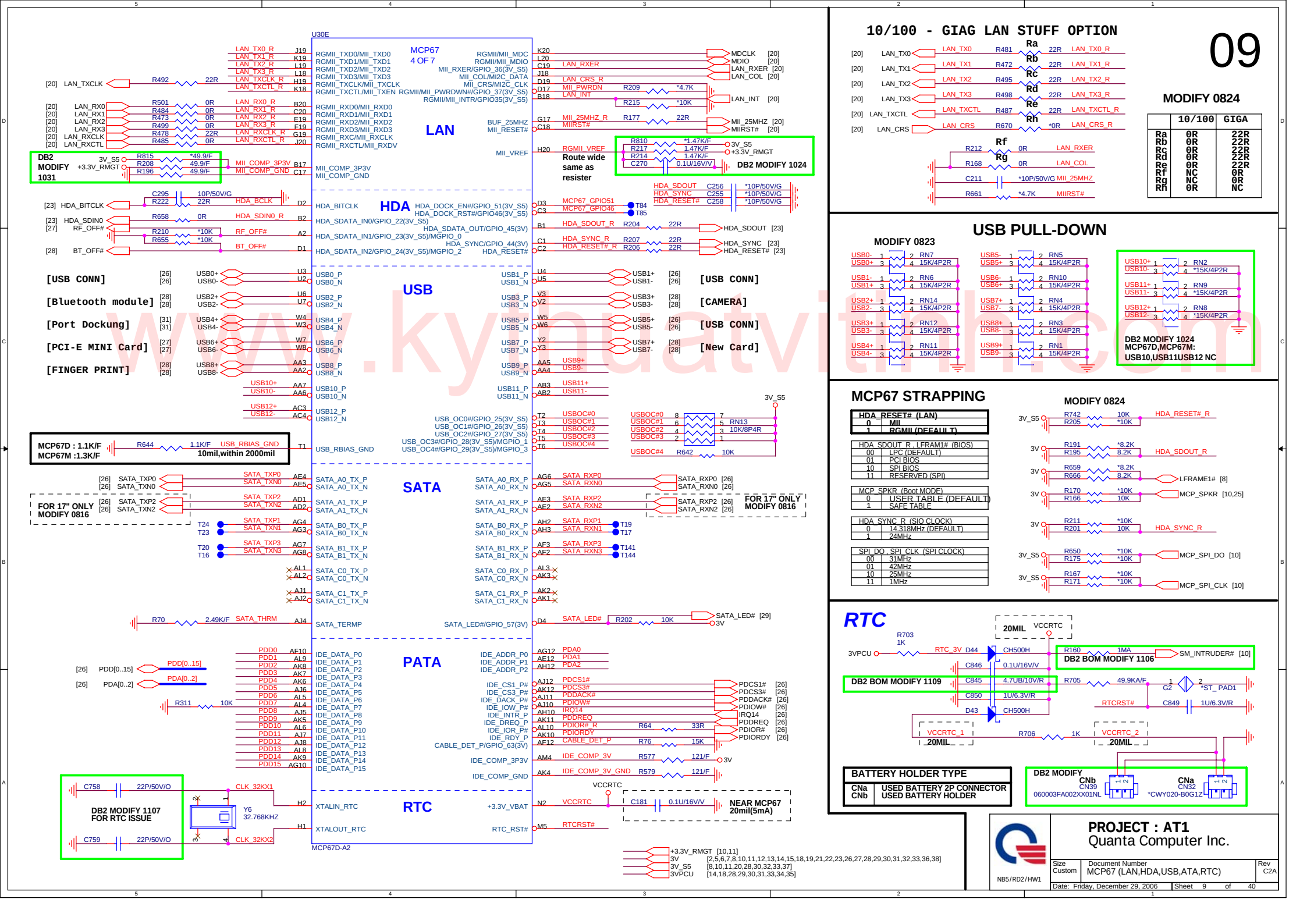
3V [2,5,6,7,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
3V_S5 [9,10,11,20,28,30,32,33,37]

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MCP67 (PCI,LPC,JTAG)	C2A

NB5/RD2/HW1

Date: Friday, December 29, 2006 Sheet 8 of 40



10/100 - GIAG LAN STUFF OPTION

	10/100	GIGA
Ra	0R	22R
Rb	0R	22R
Rc	0R	22R
Rd	0R	22R
Re	0R	22R
Rf	NC	0R
Rg	NC	0R
Rh	0R	NC

09

MODIFY 0824

USB PULL-DOWN

MODIFY 0823

DB2 MODIFY 1024
MCP67D,MCP67M:
USB10,USB11USB12 NC

MCP67 STRAPPING

HDA_RESET# (LAN)
0 MII
1 RGMII (DEFAULT)

HDA_SDOUT_R , LFRAM1# (BIOS)
00 LPC (DEFAULT)
01 PCI BIOS
10 SPI BIOS
11 RESERVED (SPI)

MCP_SPKR (Boot MODE)
0 USER TABLE (DEFAULT)
1 SAFE TABLE

HDA_SYNC_R (SIO CLOCK)
0 14.318MHz (DEFAULT)
1 24MHz

SPI_DO , SPI_CLK (SPI CLOCK)
00 31MHz
01 42MHz
10 25MHz
11 1MHz

RTC

BATTERY HOLDER TYPE
CNa USED BATTERY 2P CONNECTOR
CNb USED BATTERY HOLDER

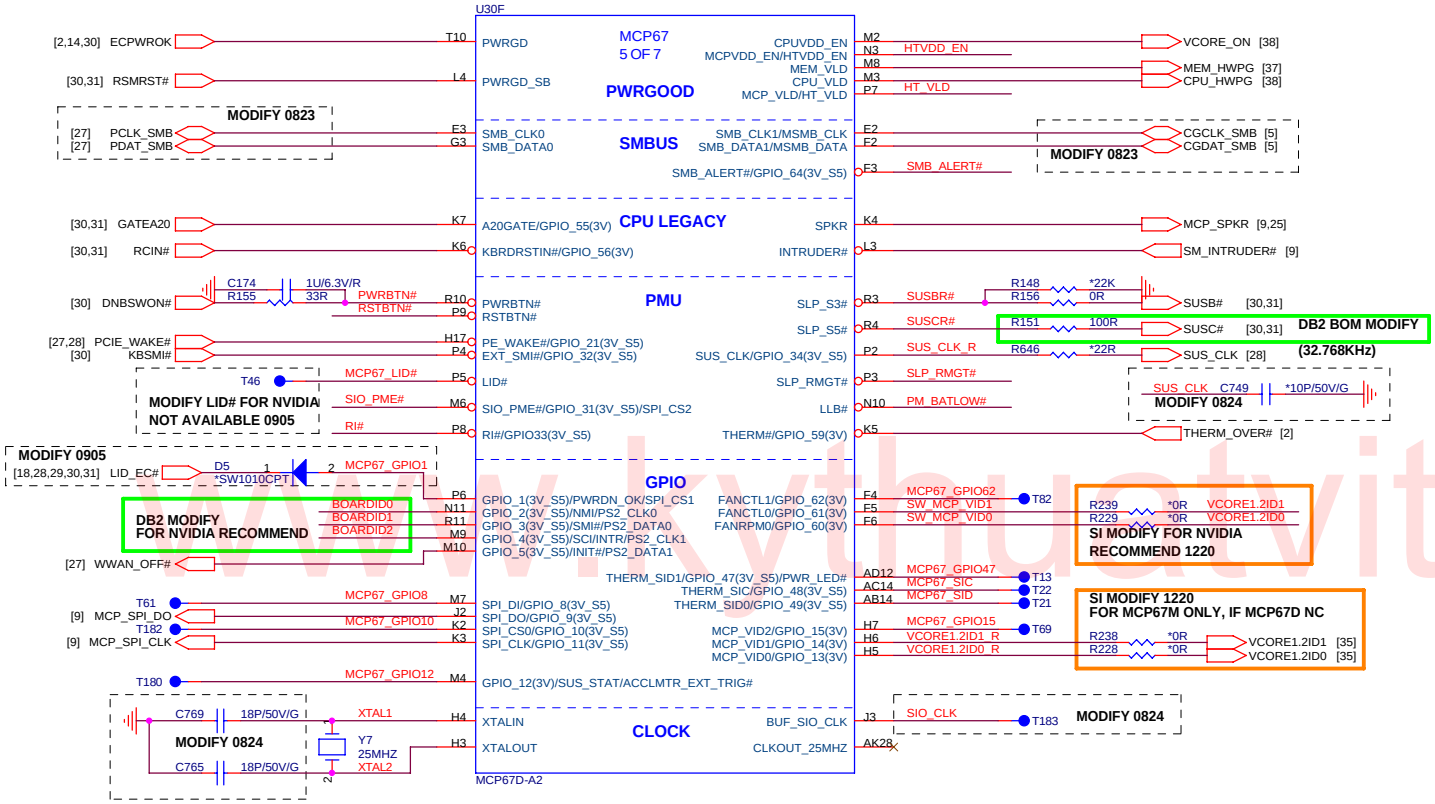
DB2 BOM MODIFY 1106
DB2 BOM MODIFY 1109
NEAR MCP67 20mil(5mA)

DB2 MODIFY
CNb CN39 060003FA002XX01NL
CNa CN32 *CWY020-B0G1Z

PROJECT : AT1
Quanta Computer Inc.

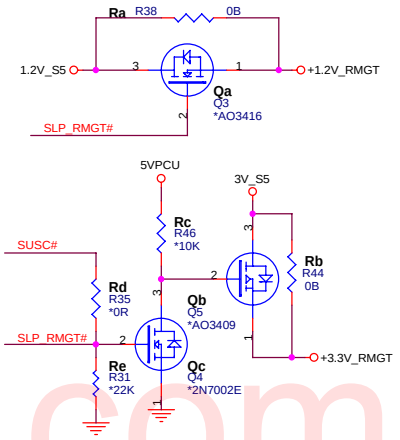
Size	Document Number	Rev
Custom	MCP67 (LAN,HDA,USB,ATA,RTC)	C2A
Date: Friday, December 29, 2006	Sheet 9 of 40	

NB5/RD2/HW1



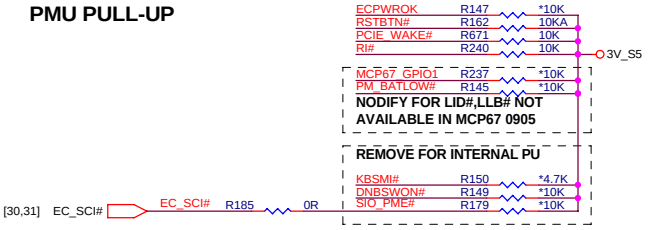
CORE POWER CIRCIUT FOR SLEEP MODE
MCP67M SUPPORT ONLY

10



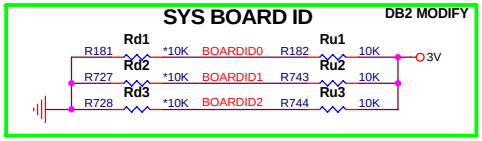
MCP67M & MCP67D DIFFERENCE TABLE		
	MCP67M UMA	MCP67D DISCRETE
Ra	NC	STUFF
Rb	NC	STUFF
Rc	STUFF	NC
Rd	NC	NC
Re	STUFF	NC
Qa	STUFF	NC
Qb	STUFF	NC
Qc	STUFF	NC

PMU PULL-UP



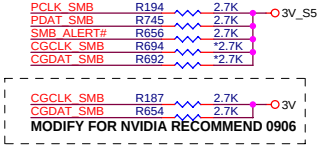
SKU (BOARD ID)	AT1A (DISCRETE)	AT1A (UMA)	AT1B (UMA ONLY)	AT2A (DISCRETE)	AT2A (UMA)
Board ID	010	X00	X00	111	X01
ID0 STUFF	Rd1	Rd1	Rd1	Ru1	Ru1
ID1 STUFF	Ru2	Rd2	Rd2	Ru2	Rd2
ID2 STUFF	Rd3			Ru3	

Board ID :	0/1	0/1	0/1
DIFINE	RESERVE / RESERVE	UMA / DISCRETE	AT1 / AT2

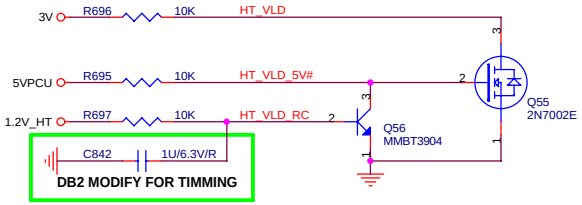


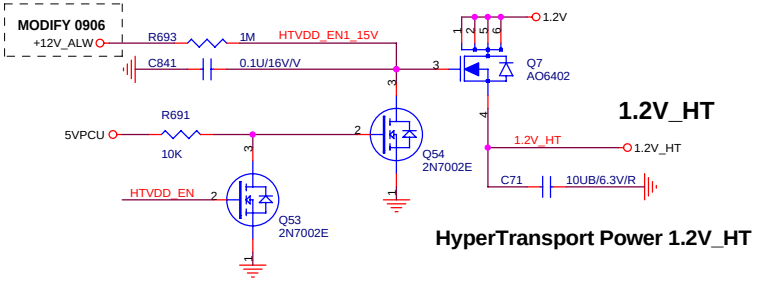
CPU LEGACY PULL-UP

SMB/I2C PULL-UP



HyperTransport Link 1.2 V_HT Power Valid





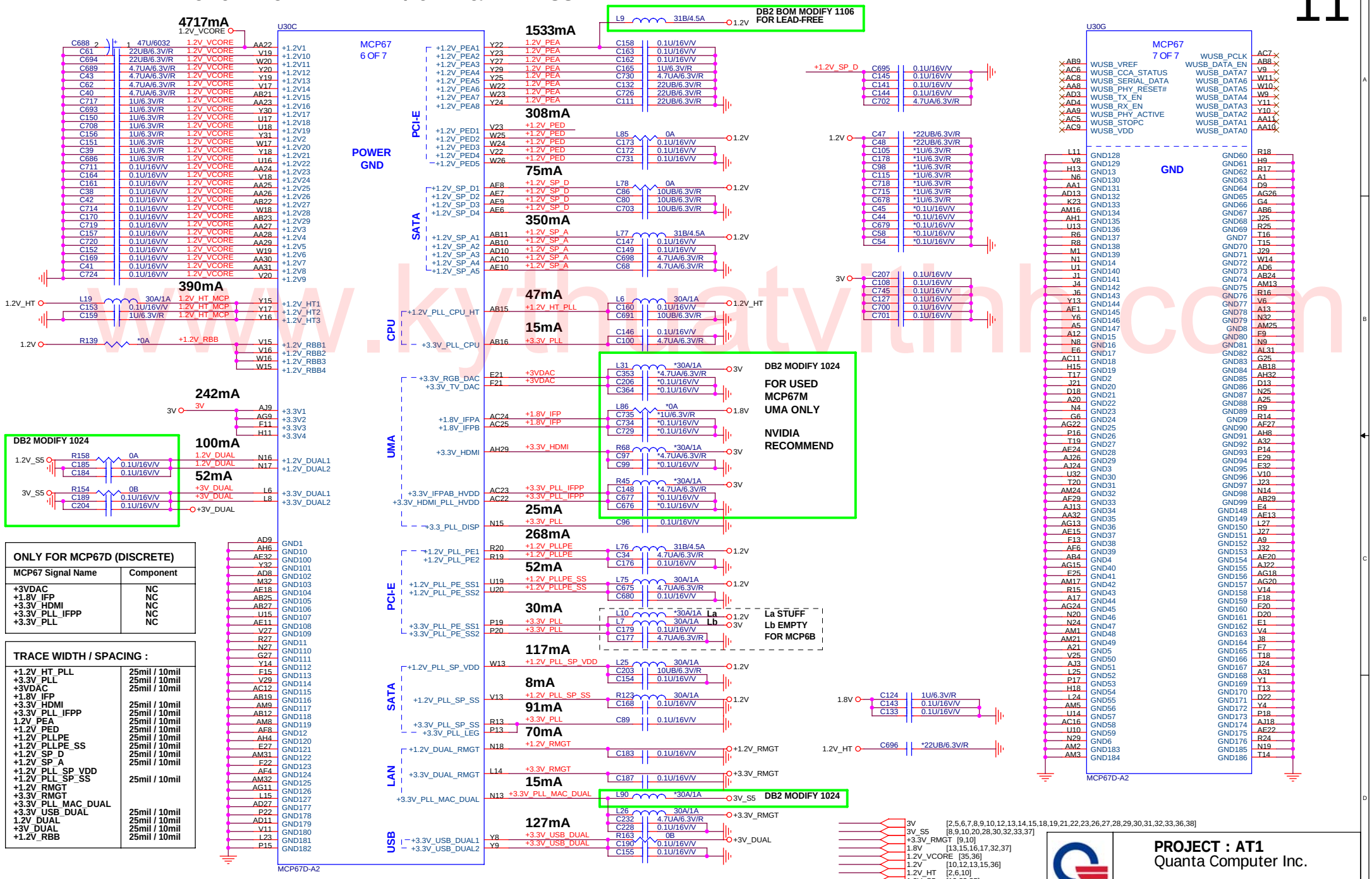
HyperTransport Power 1.2V_HT

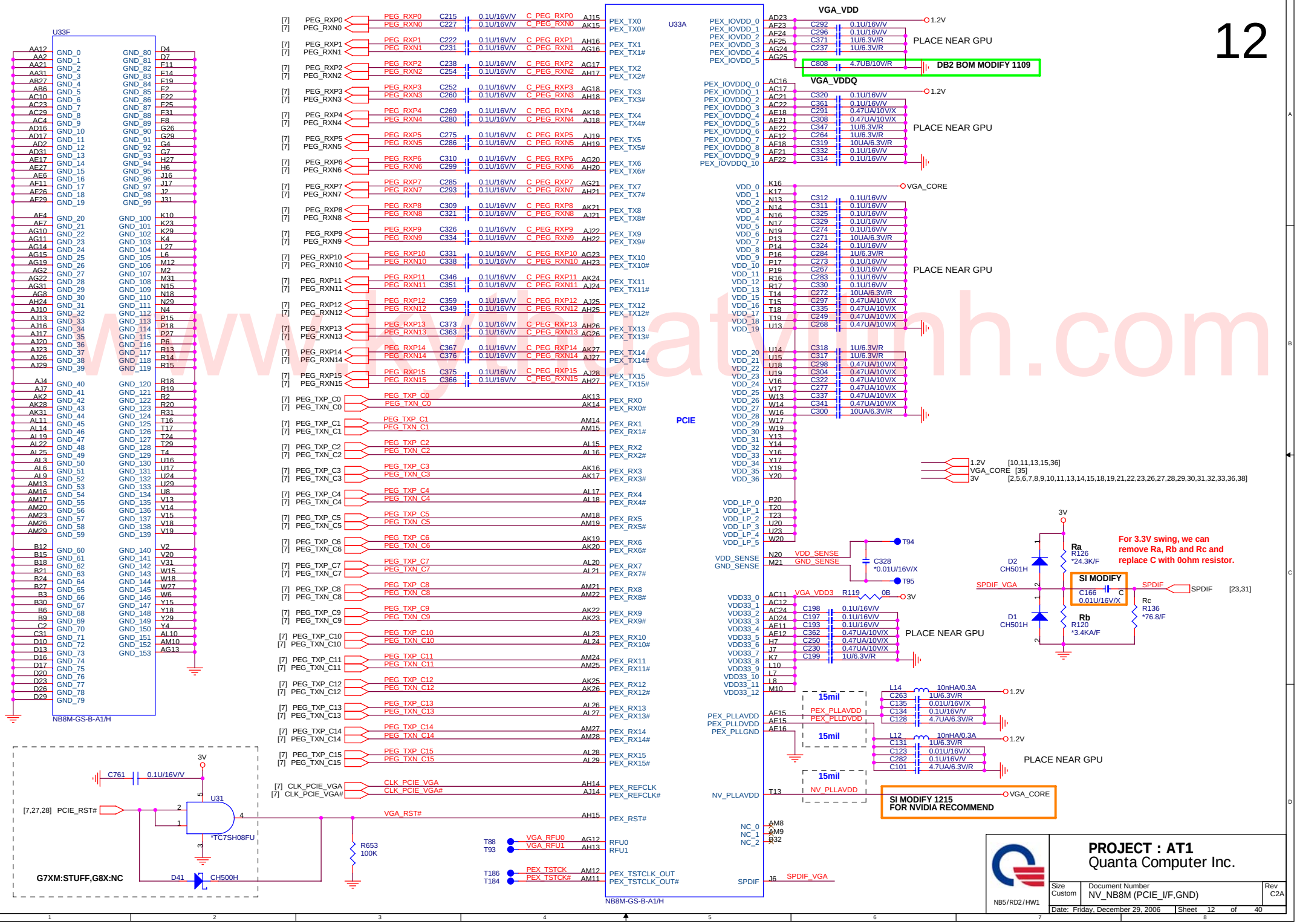
+1.2V_RMGT [11]
1.2V_S5 [11,32,35]
1.2V_HT [2,6,11]
1.2V [11,12,13,15,36]
+3.3V_RMGT [9,11]
3V [2,5,6,7,8,9,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
3V_S5 [8,9,11,20,28,30,32,33,37]
5VPCU [23,33,34,35,36,37,38]
+12V_ALW [18,32,33]

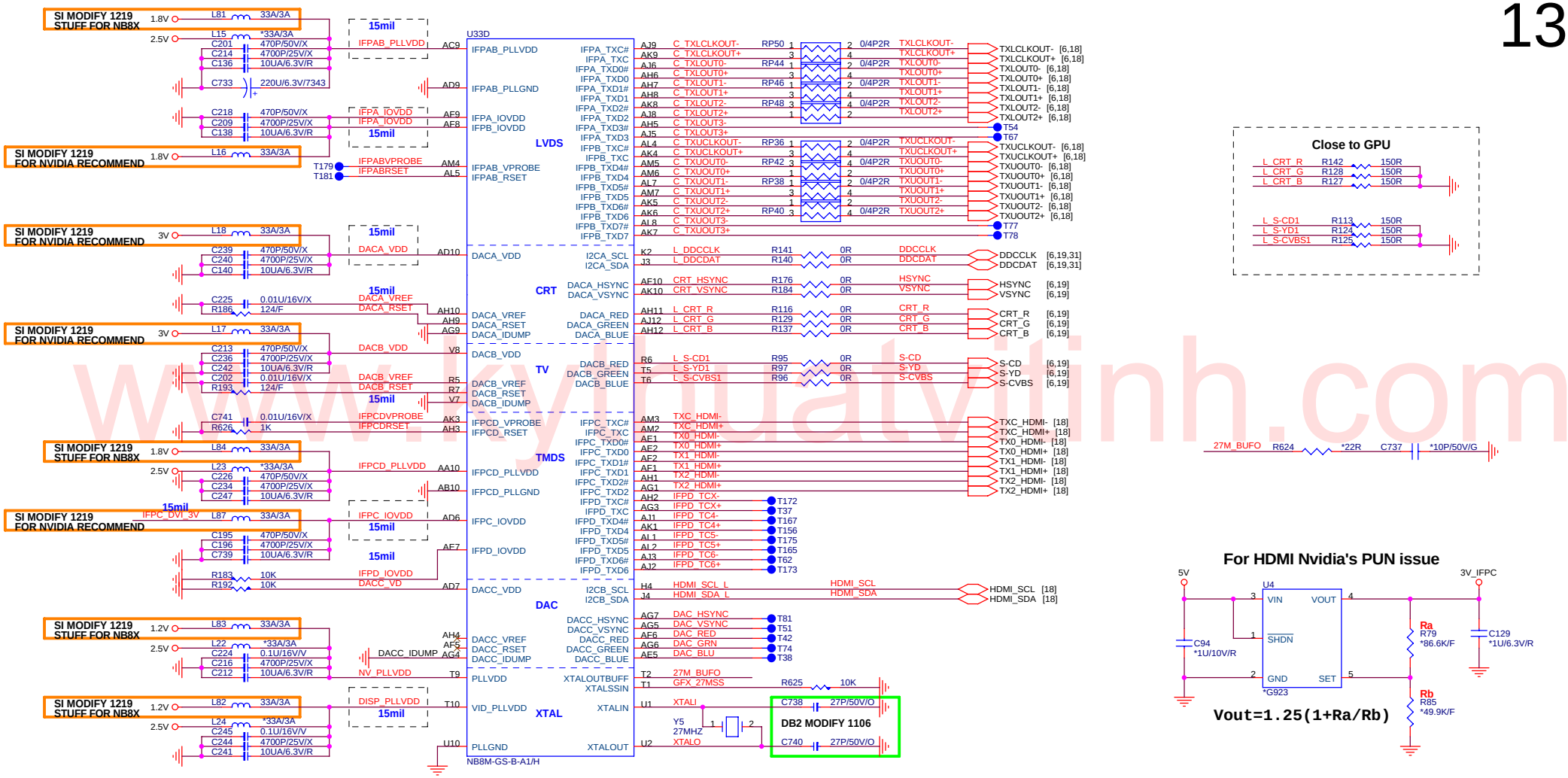
PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MCP67 (PG,SMB,PMU,GPIO,CLK)	C2A
NB5/RD2/HW1	Date: Friday, December 29, 2006	Sheet 10 of 40

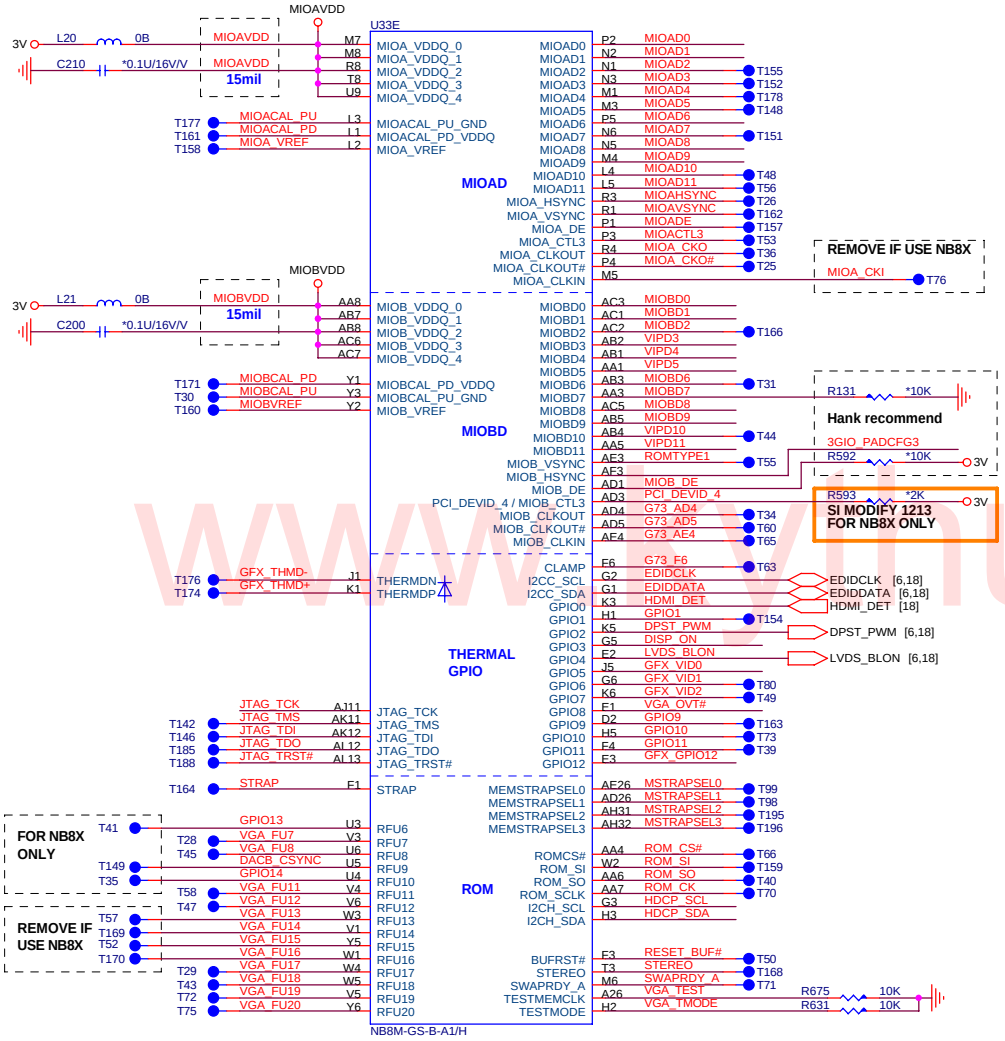
MCP67 POWER PLANE/GND & BYPASS

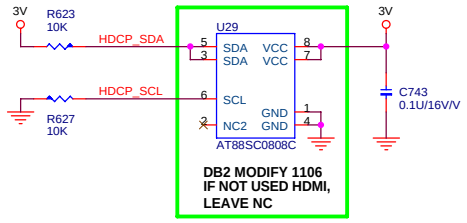


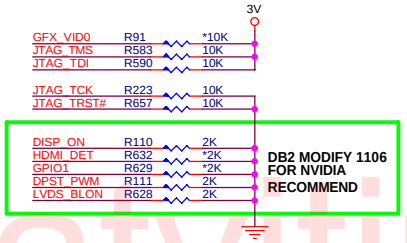


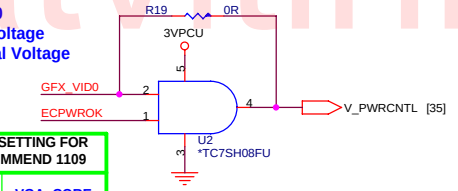


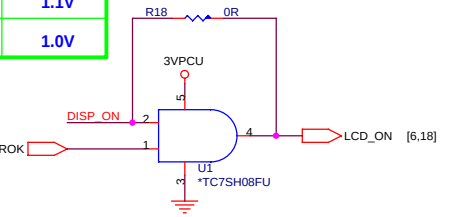
PROJECT	AT1
Company	Quanta Computer Inc.
Size	Custom
Document Number	NV_NB8M (LVDS,CRT,TV,HDMI)
Rev	C2A
Date	Friday, December 29, 2006
Sheet	13 of 40
	NB5/RD2/HW1









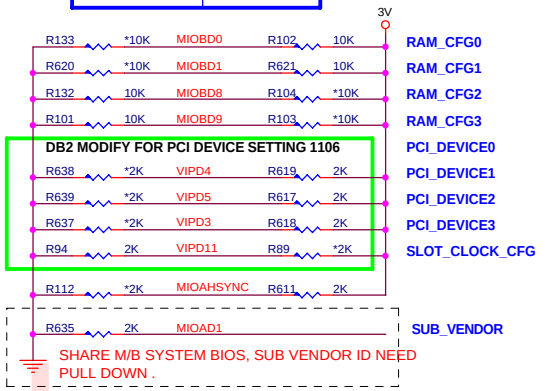


DB2 MODIFY SETTING FOR NVIDIA RECOMMEND 1109

GFX_VID0 (GPIO5)	VGA_CORE (NB8X)
HI	1.1V
LO	1.0V

PCI DEVICE ID SETTING

PCI_DEVICE[4:0]	DESCRIPTION
00111	NB8M
OTHERS	RESERVED

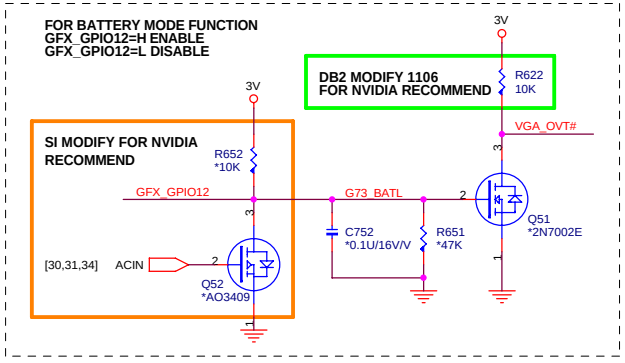


NB8X 64bit VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
0001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
0010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
0011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
0110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
0111	DDR2 32Mx16x4, 64bit, 256MB	Hynix
1000	DDR2 16Mx16x2, 32bit, 64MB	Elpida
1001	DDR2 16Mx16x2, 32bit, 64MB	Samsung
1010	DDR2 16Mx16x2, 32bit, 64MB	Infineon
1011	DDR2 16Mx16x2, 32bit, 64MB	Hynix
others	Reserved	

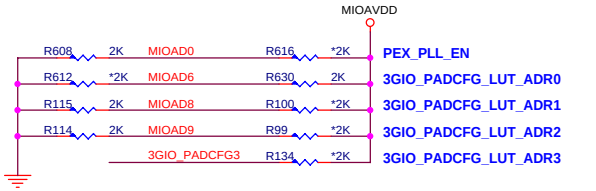
NB8X 128bit VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x8, 128bit, 256MB	Elpida
0001	DDR2 16Mx16x8, 128bit, 256MB	Samsung
0010	DDR2 16Mx16x8, 128bit, 256MB	Infineon
0011	DDR2 16Mx16x8, 128bit, 256MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
0110	DDR2 32Mx16x8, 128bit, 512MB	Infineon
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix
1000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
1001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
1010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
1011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
1100	Reserved	
1101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
1110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
1111	DDR2 32Mx16x4, 64bit, 256MB	Hynix



3GIO_PADCFG STRAP

3GIO_PDACFG[3:0]	DESCRIPTION
0000	DESKTOP
0001	MOBILE
OTHERS	RESERVED



3V [2,5,6,7,8,9,10,11,12,13,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
3VPCU [9,18,28,29,30,31,33,34,35]

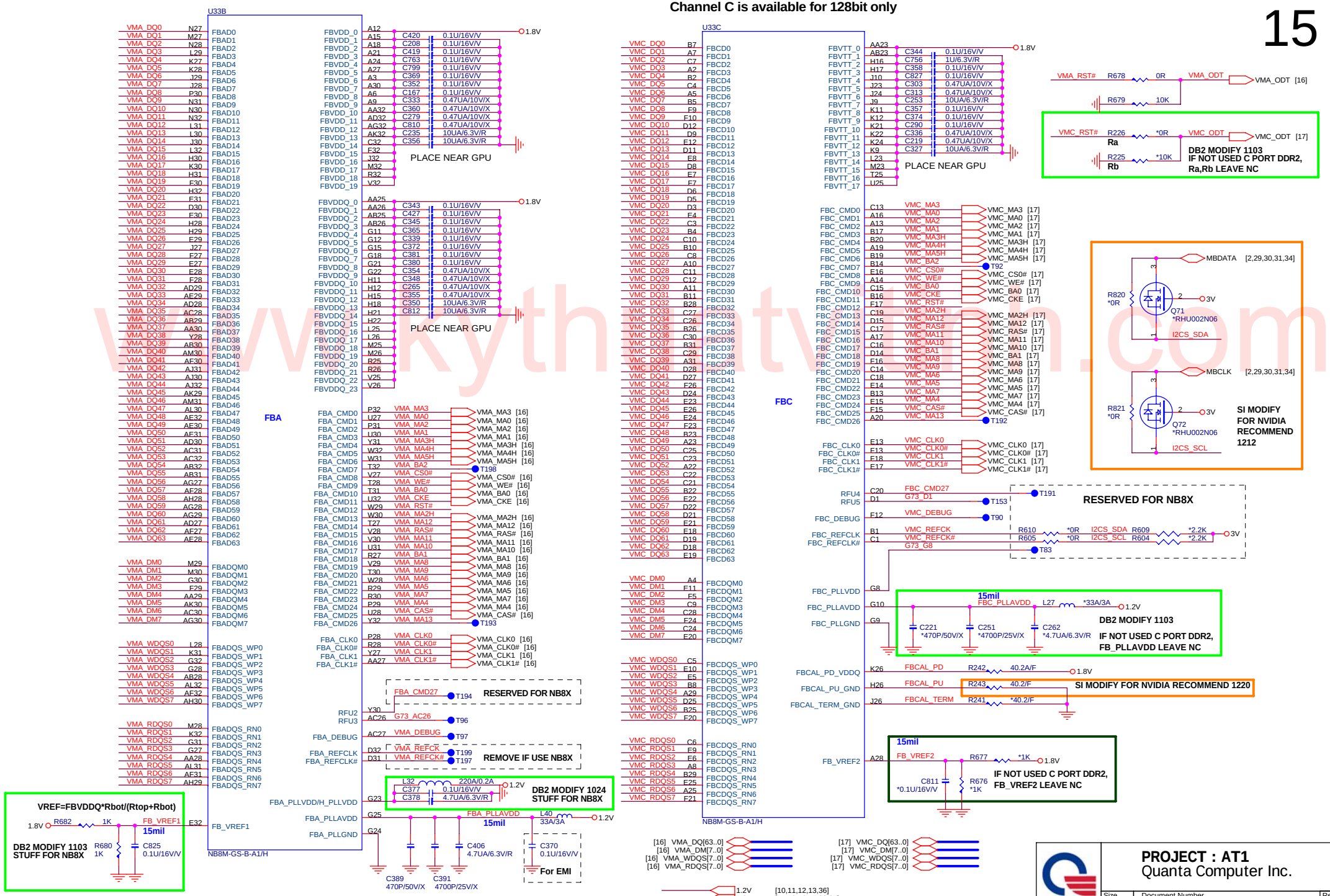
NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV_NB8M (ROM,GPIO,STRAP)	C2A

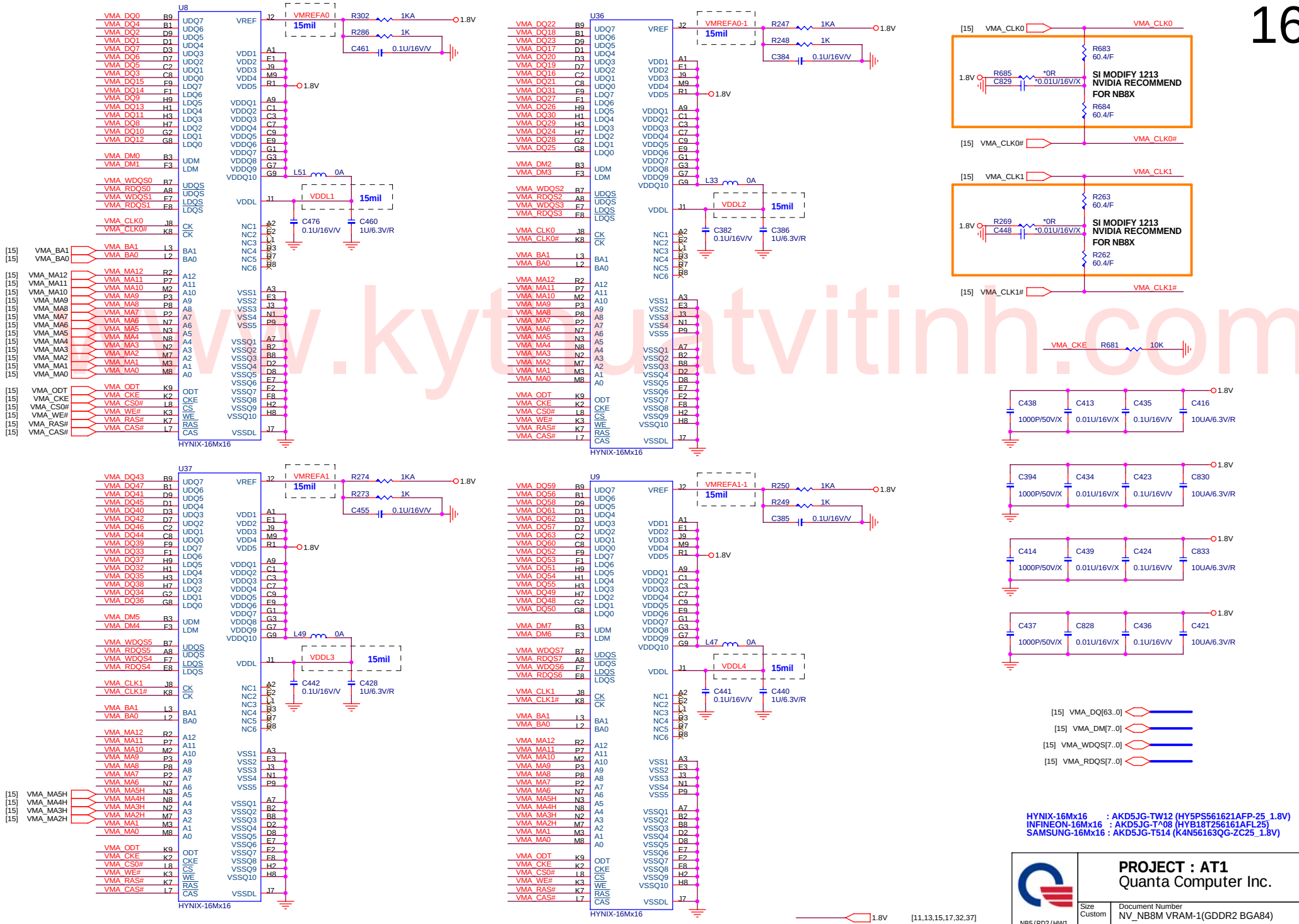
Date: Friday, December 29, 2006 Sheet 14 of 40

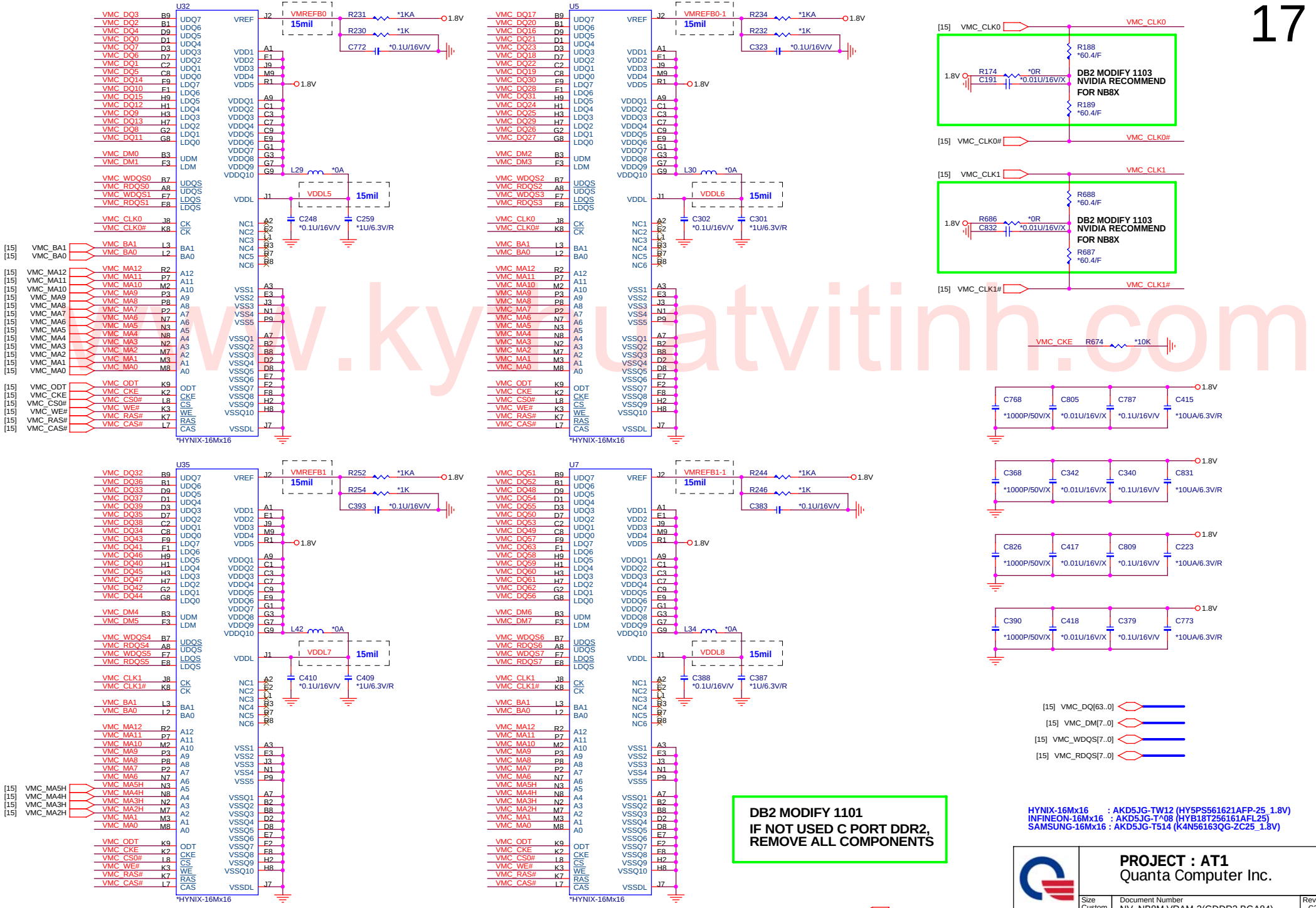
Channel C is available for 128bit only



Size: Custom	Document Number: NV_NB8M (MEM_I/F)	Rev: C2A
Date: Friday, December 29, 2006	Sheet 15 of 40	

PROJECT : AT1
Quanta Computer Inc.
NB5/RD2/HW1





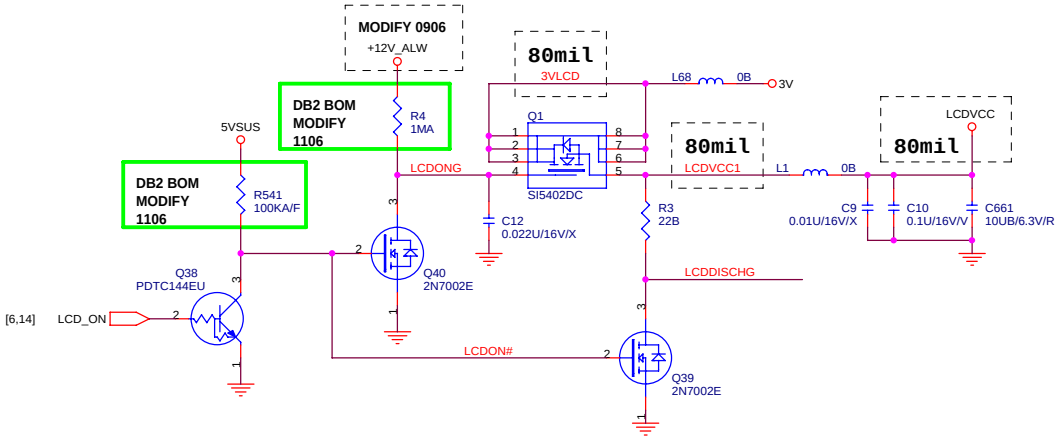
HYNIX-16Mx16 : AKD5JG-TW12 (HY5PS561621AFP-25_1.8V)
INFINEON-16Mx16 : AKD5JG-T^08 (HYB18T256161AFL25)
SAMSUNG-16Mx16 : AKD5JG-T514 (K4N56163QG-ZC25_1.8V)

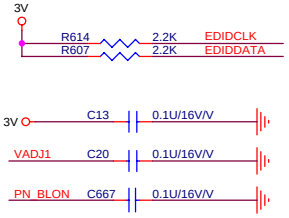
NB5/RD2/HW1

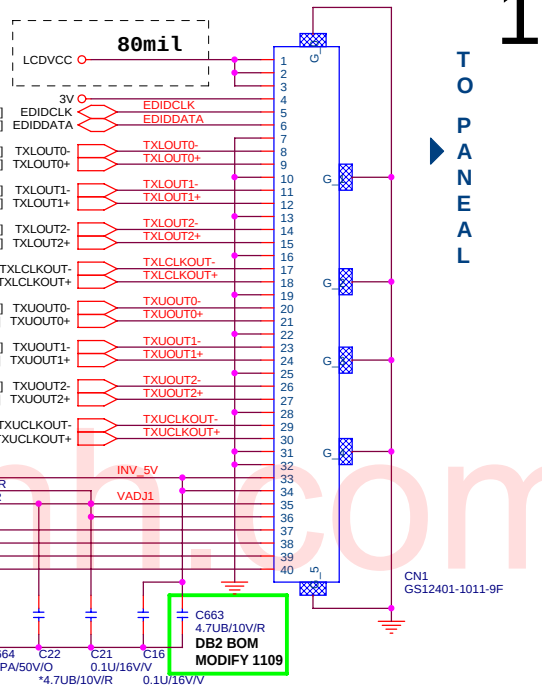
PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV_NB8M VRAM-2(GDDR2 BGA84)	C2A
Date: Friday, December 29, 2006	Sheet 17 of 40	

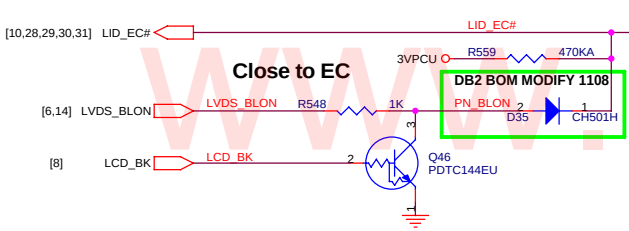
LCD CONNECTOR

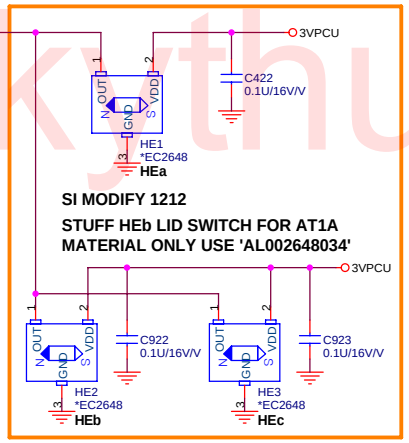


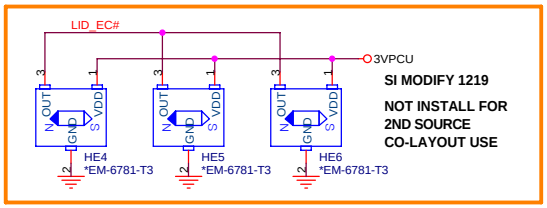


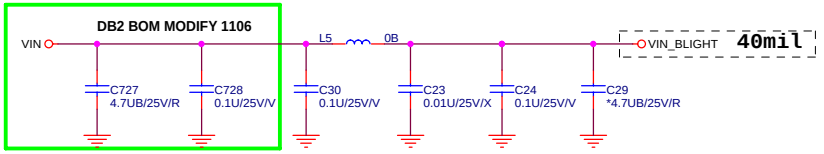


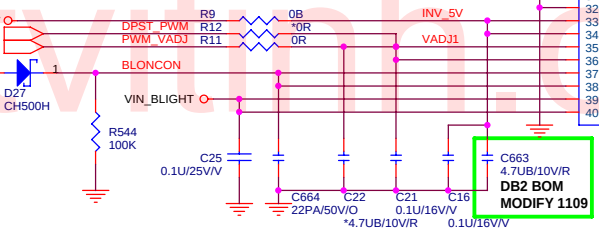
TO PANEAL



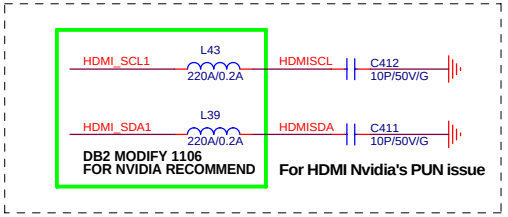


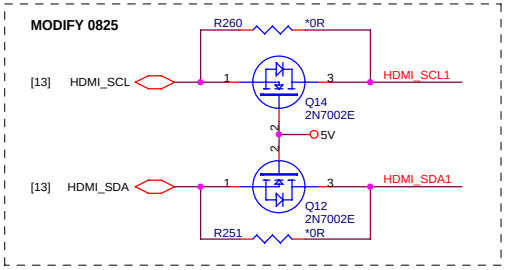


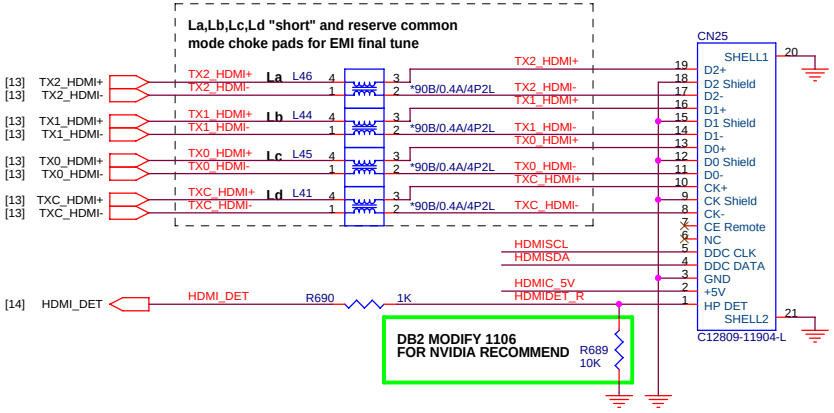


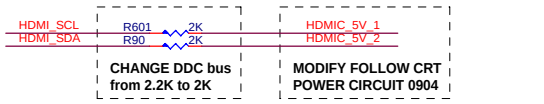


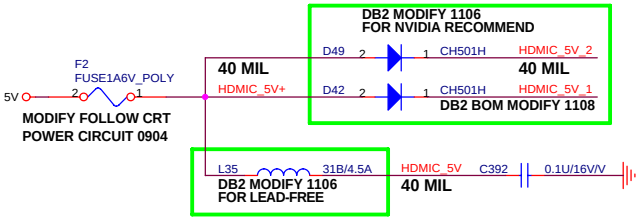
HDMI PORT









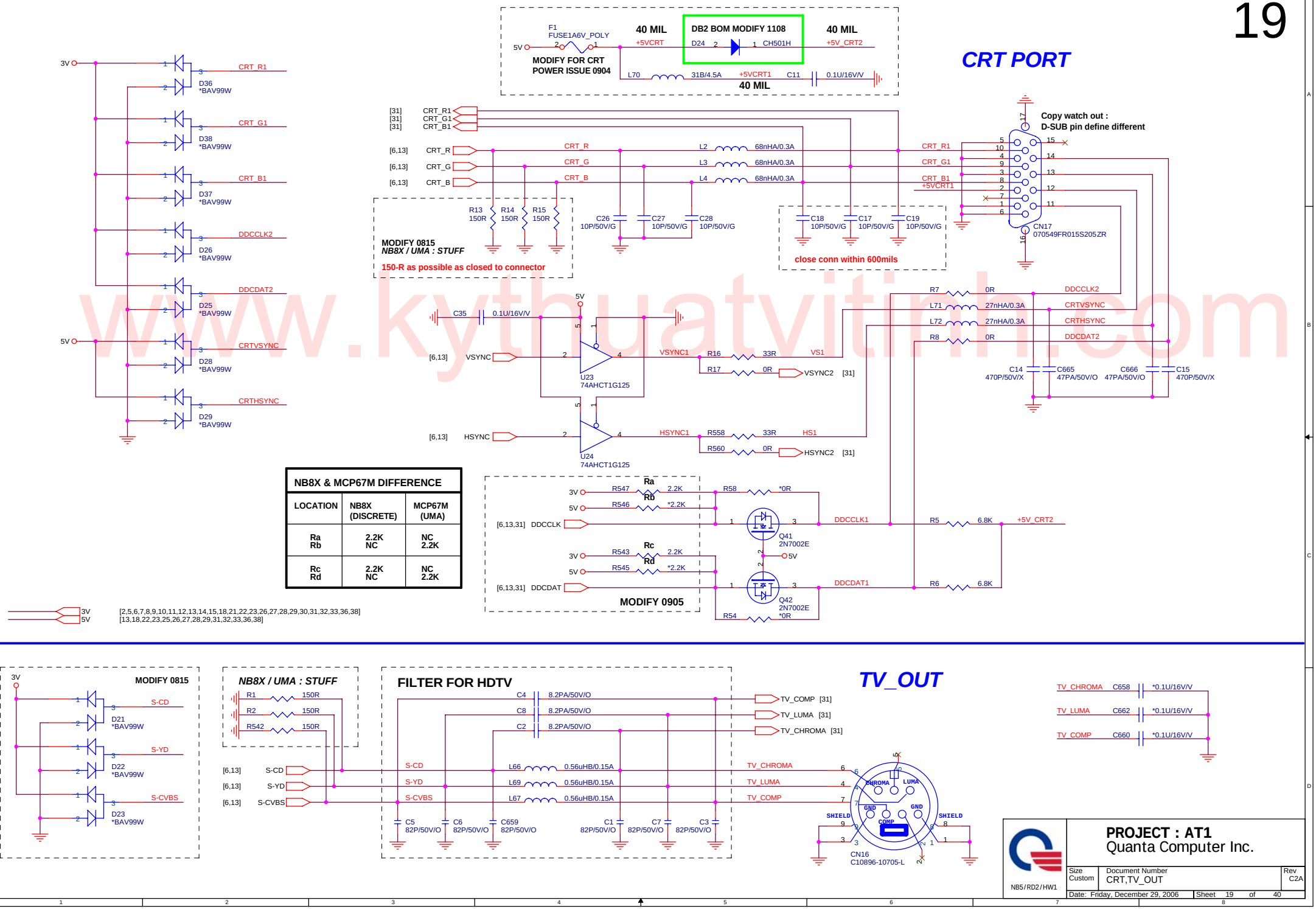


3V	[2,5,6,7,8,9,10,11,12,13,14,15,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
3VPCU	[9,14,28,29,30,31,33,34,35]
5V	[13,19,22,23,25,26,27,28,29,31,32,33,36,38]
5VSUS	[26,28,30,31,32,33,37]
+12V_ALW	[10,32,33]
VIN	[31,32,33,34,35,36,37,38]

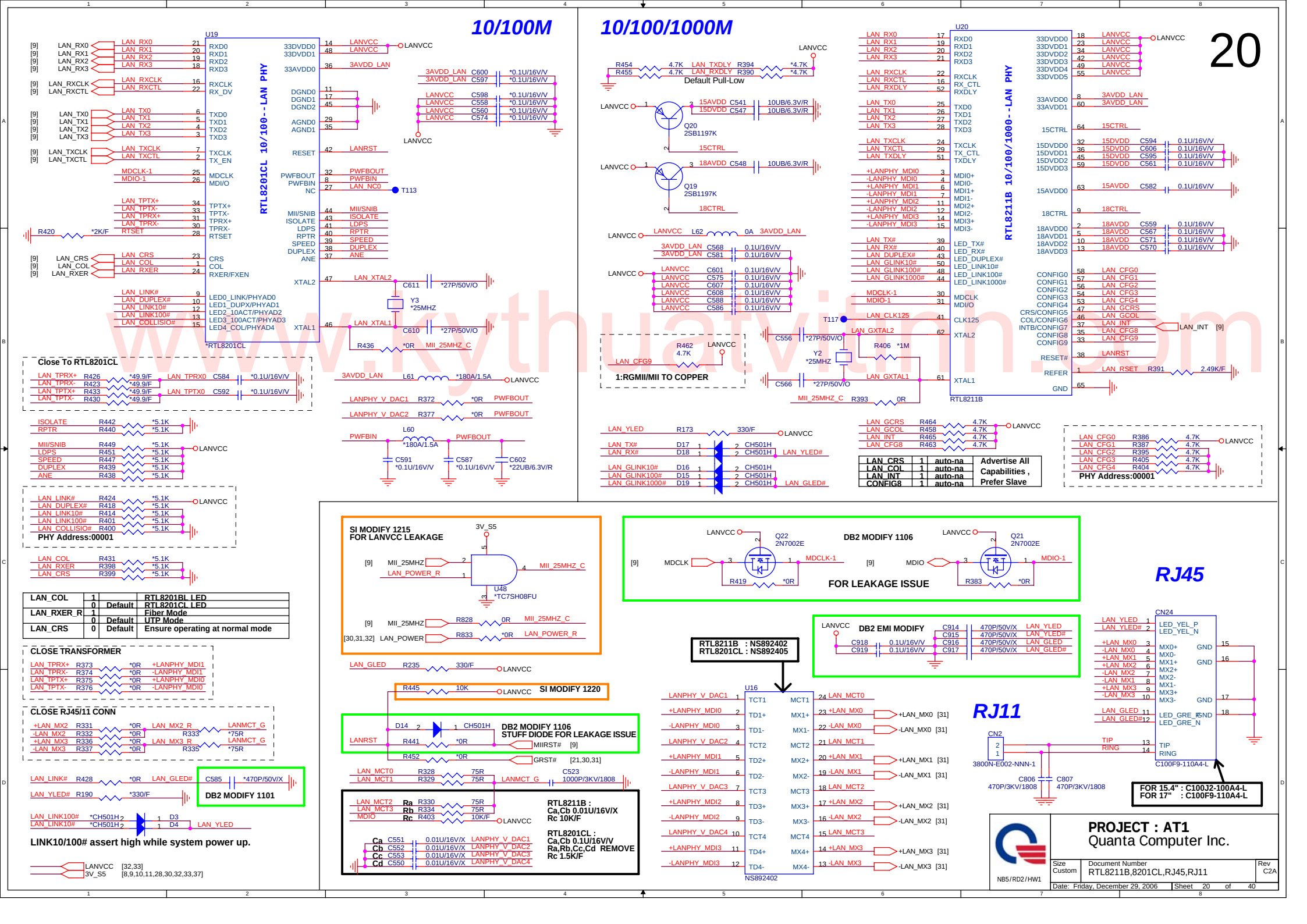
NB5/RD2/HW1

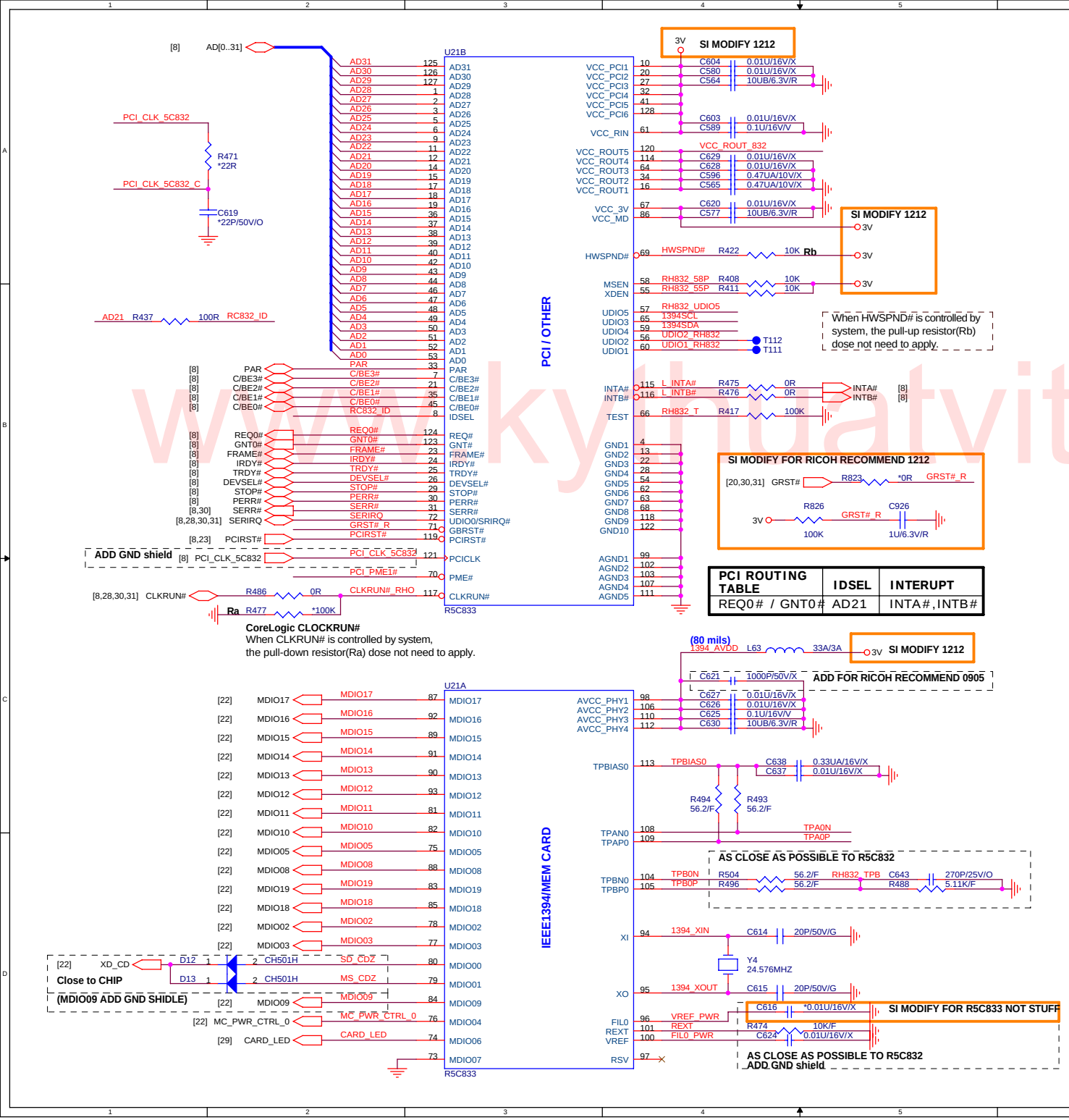
PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD,HDMI,LID_SW	C2A
Date: Friday, December 29, 2006	Sheet 18 of 40	

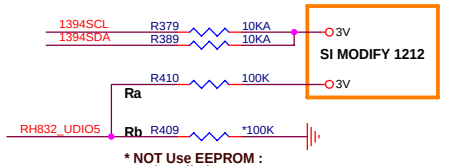


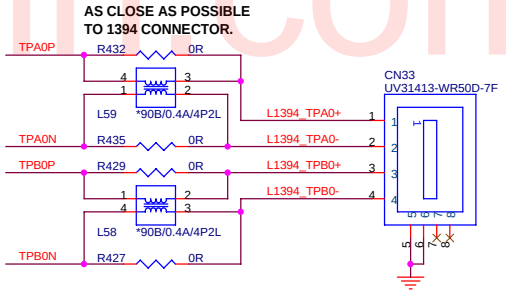
PROJECT : AT1	Quanta Computer Inc.	
Size: Custom	Document Number: CRT,TV_OUT	Rev: C2A
NB5/RD2/HW1	Date: Friday, December 29, 2006	Sheet 19 of 40





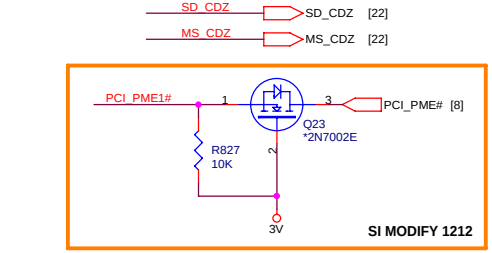
Serial EEPROM





*TPA/TPA#,TPB/TPB# pair trace : As close as possible.
*TPA/TPA#,TPB/TPB# pair trace : Same length electrically.And layout with shields.

*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).



3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,22,23,26,27,28,29,30,31,32,33,36,38]

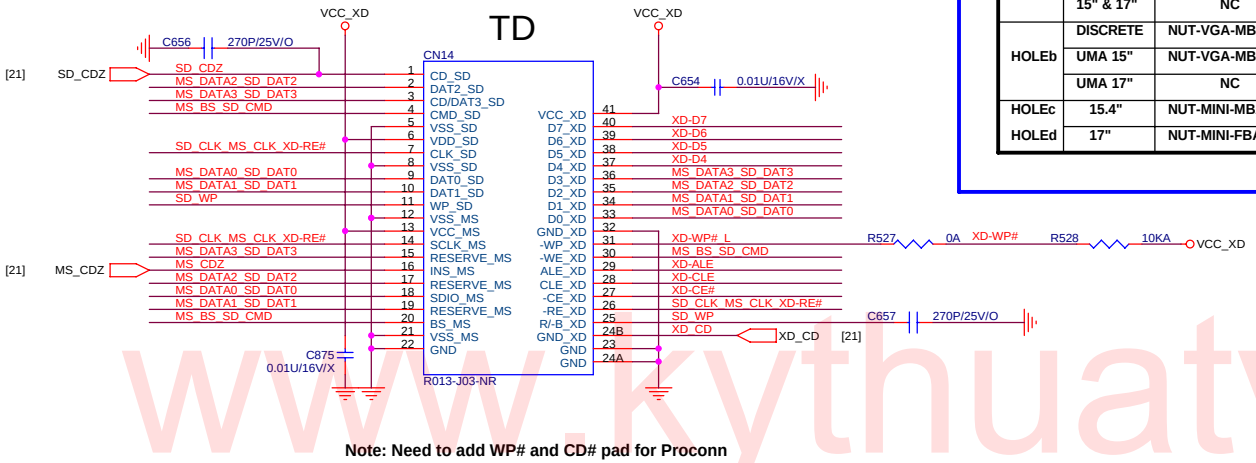
PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	R5C832V00,1394 PORT	C2A

NB5/RD2/HW1

Date: Friday, December 29, 2006 Sheet 21 of 40

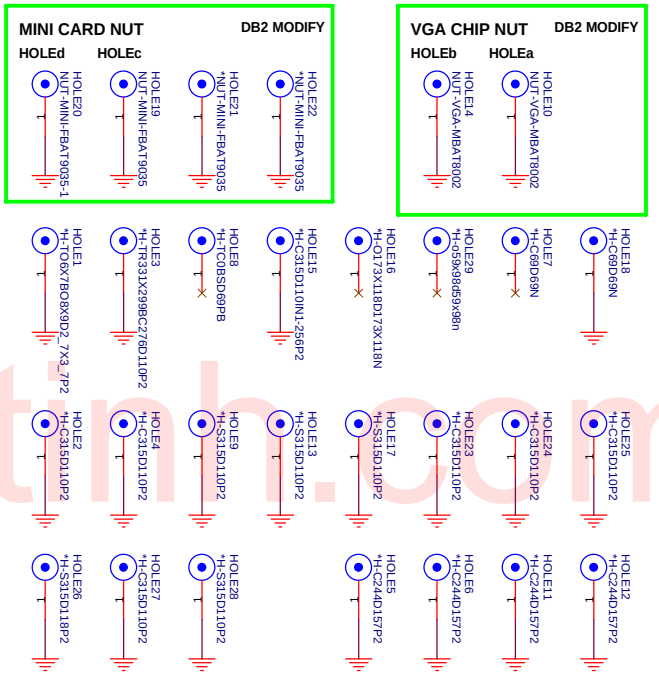
4 IN1 CARD READER
XD,MMC/SD,MS/MSP

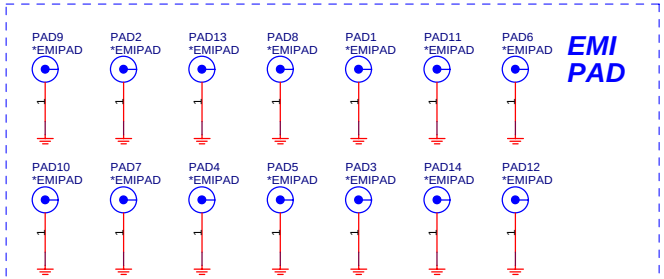


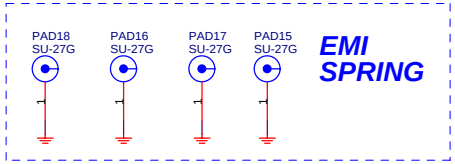
Note: Need to add WP# and CD# pad for Proconn

15.4" & 17" AND DISCRETE & UMA		
HOLE	STATUS	NUT
HOLEa	DISCRETE	NUT-VGA-MBAT8002
	15" & 17"	NC
HOLEb	DISCRETE	NUT-VGA-MBAT8002
	UMA 15"	NUT-VGA-MBAT8002
	UMA 17"	NC
HOLEc	15.4"	NUT-MINI-MBAT8004
HOLEd	17"	NUT-MINI-FBAT9035

SCREW HOLE

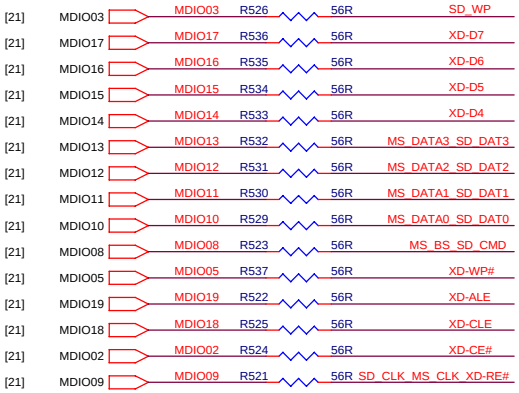


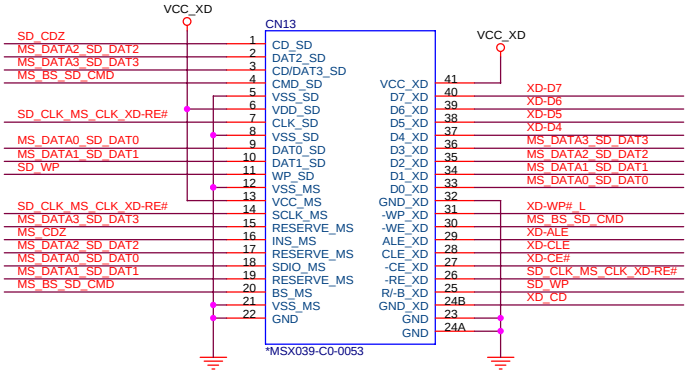




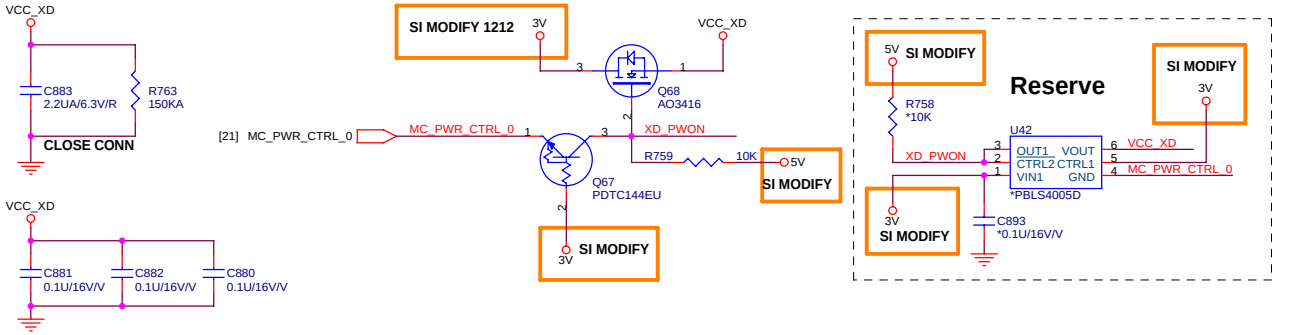
3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,23,26,27,28,29,30,31,32,33,36,38]
5V [13,18,19,23,25,26,27,28,29,31,32,33,36,38]

2ND SOURCE





*** NOT INSTALL FOR 2ND SOURCE CO-LAYOUT USED**



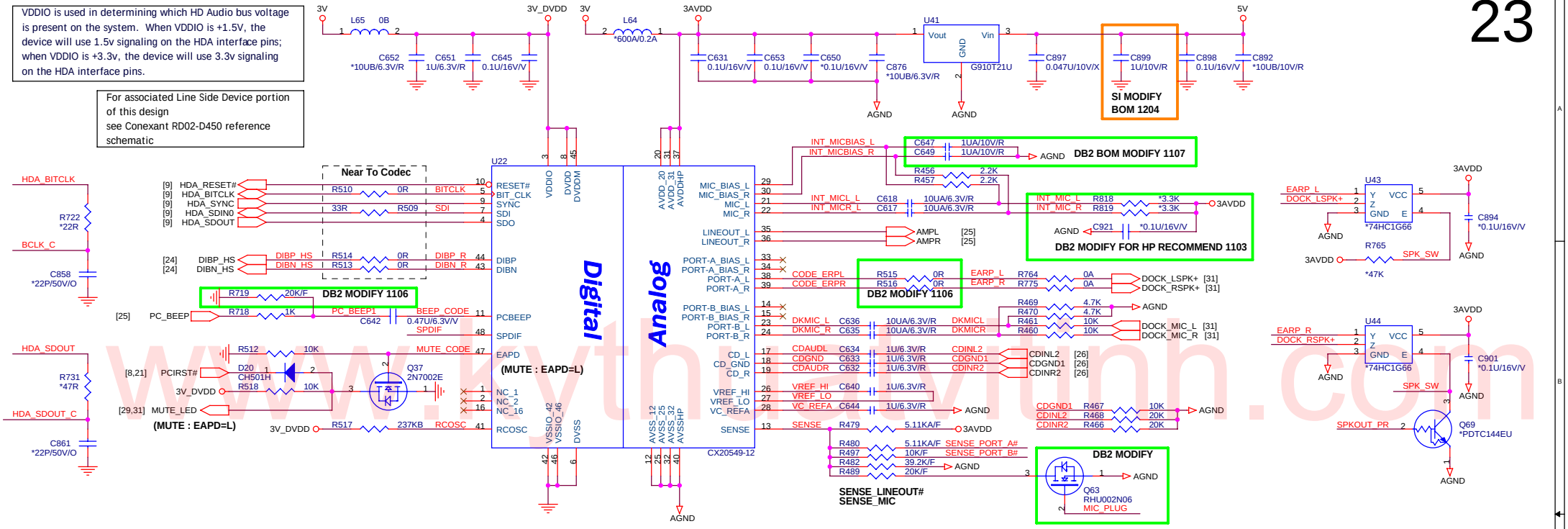
NB5/RD2/HW1

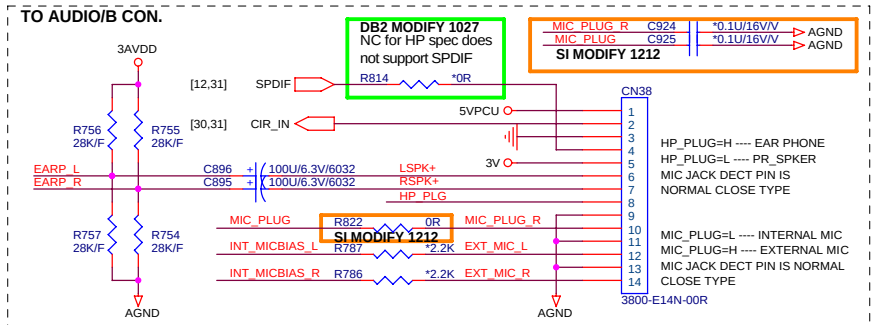
PROJECT : AT1
Quanta Computer Inc.

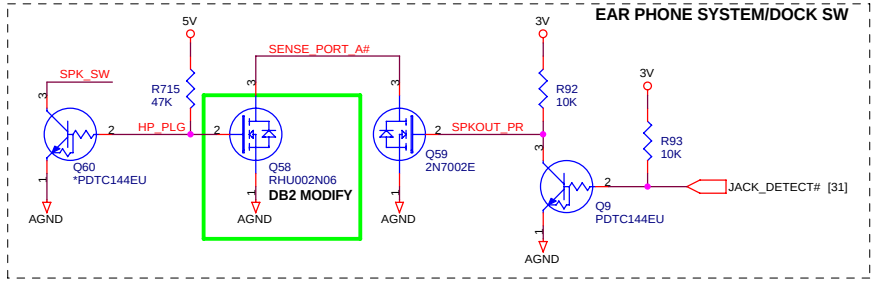
Size	Document Number	Rev
Custom	CARD_READER,HOLE,NUT,SPRING	C2A
Date: Friday, December 29, 2006	Sheet 22 of 40	

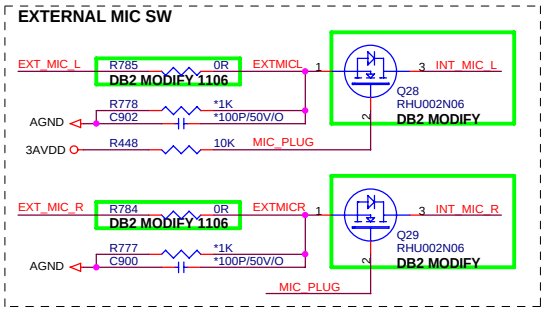
VDDIO is used in determining which HD Audio bus voltage is present on the system. When VDDIO is +1.5V, the device will use 1.5v signaling on the HDA interface pins; when VDDIO is +3.3v, the device will use 3.3v signaling on the HDA interface pins.

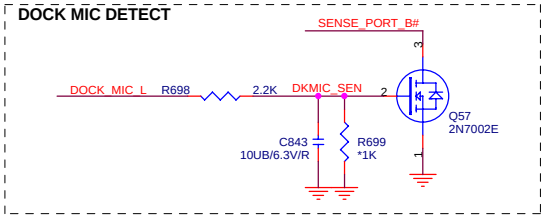
For associated Line Side Device portion of this design see Conexant RD02-D450 reference schematic

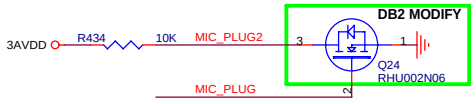


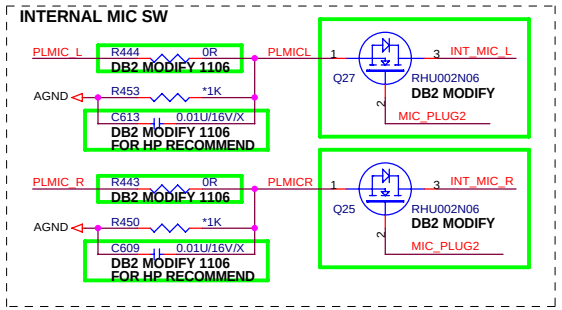


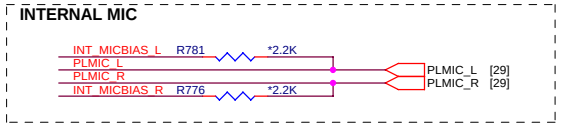












3AVDD	[25]
3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,26,27,28,29,30,31,32,33,36,38]
5V	[13,18,19,22,25,26,27,28,29,31,32,33,36,38]
5VPCU	[10,33,34,35,36,37,38]

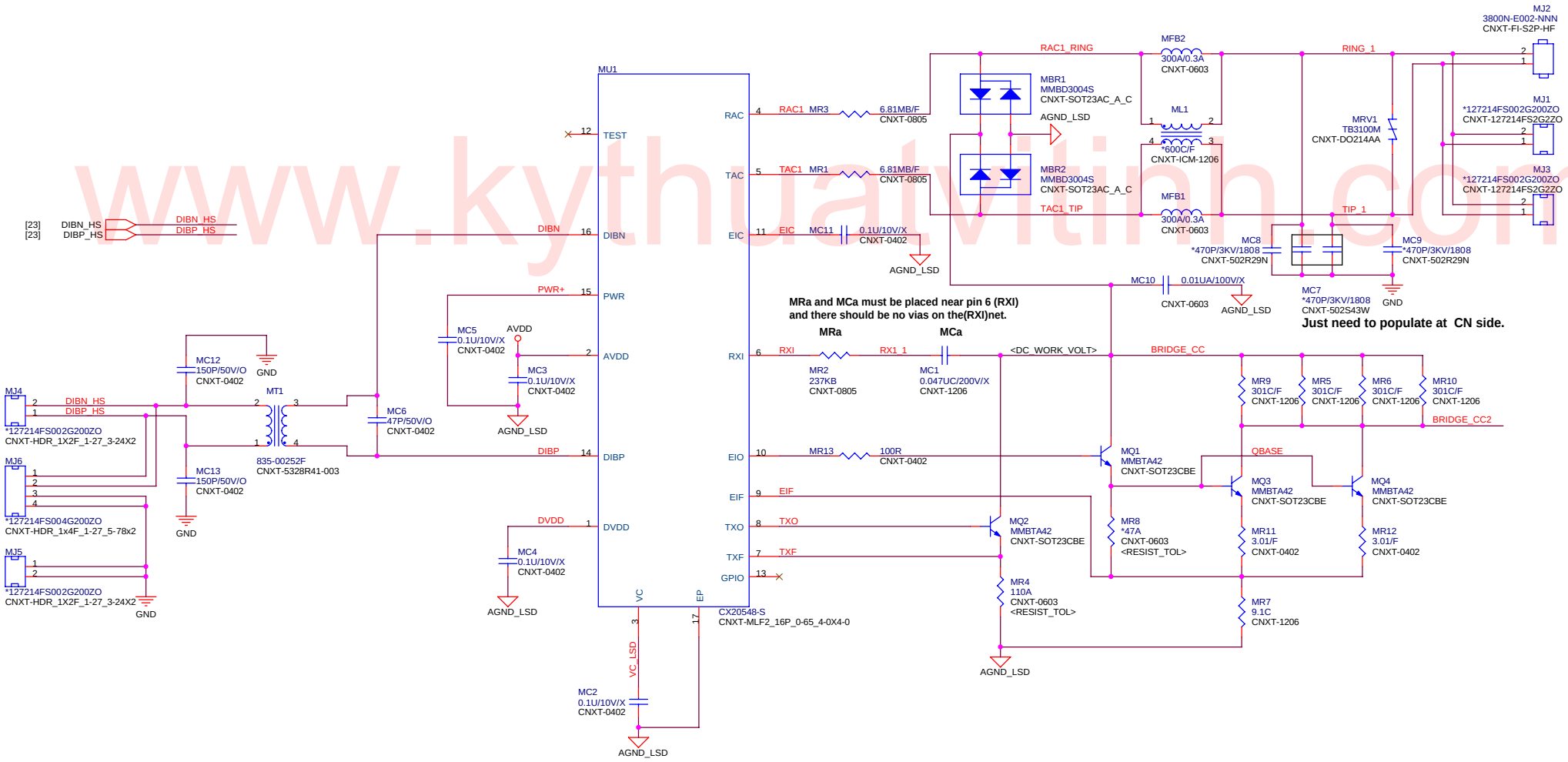
PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDA_CX20549-12,AUDIO_BOARD	C2A

NB5/RD2/HW1

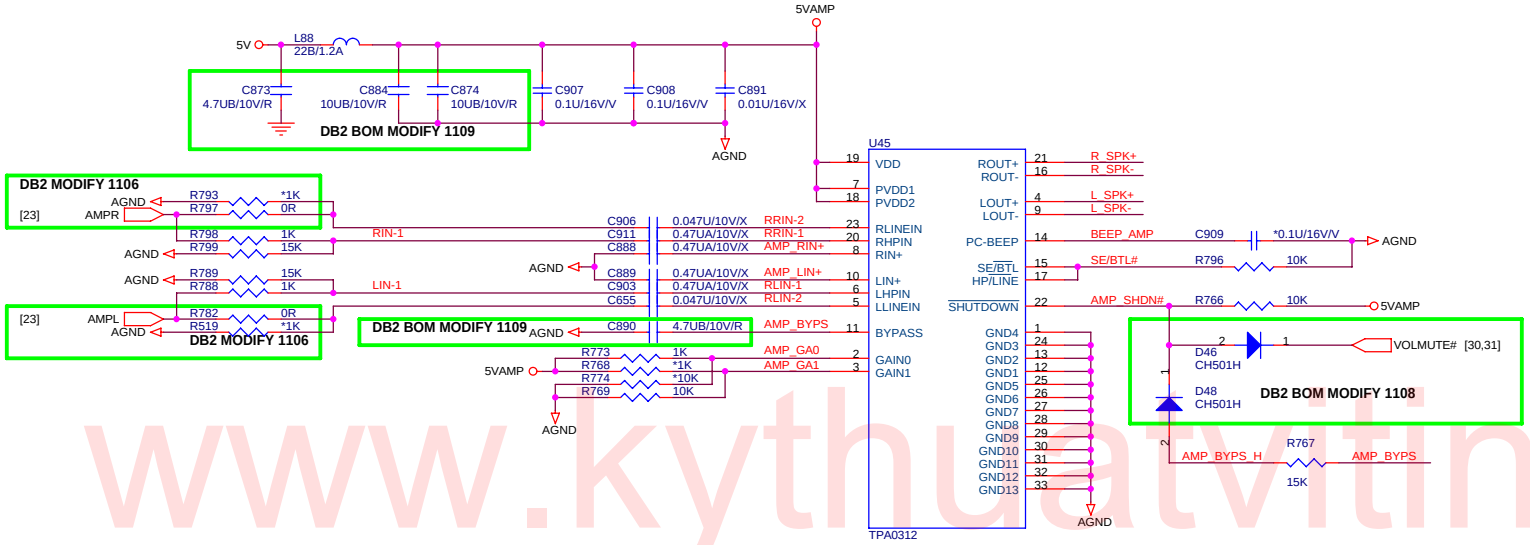
Date: Friday, December 29, 2006 Sheet 23 of 40

Revision History		
REV	Description	Date
0	Initial Release	April 26, 2005
4		



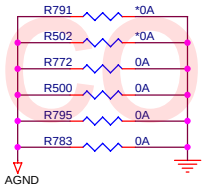
NB5/RD2/HW1	PROJECT : AT1 Quanta Computer Inc.	
	Size: Custom	Document Number: MODEM(DAA)_CX20548-S
	Date: Friday, December 29, 2006	Sheet 24 of 40

AUDIO AMPLIFIER

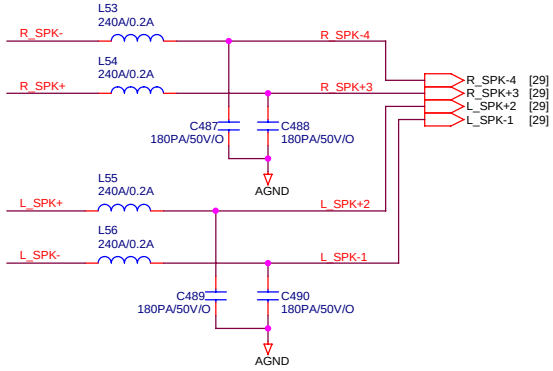


0312 Gain Table

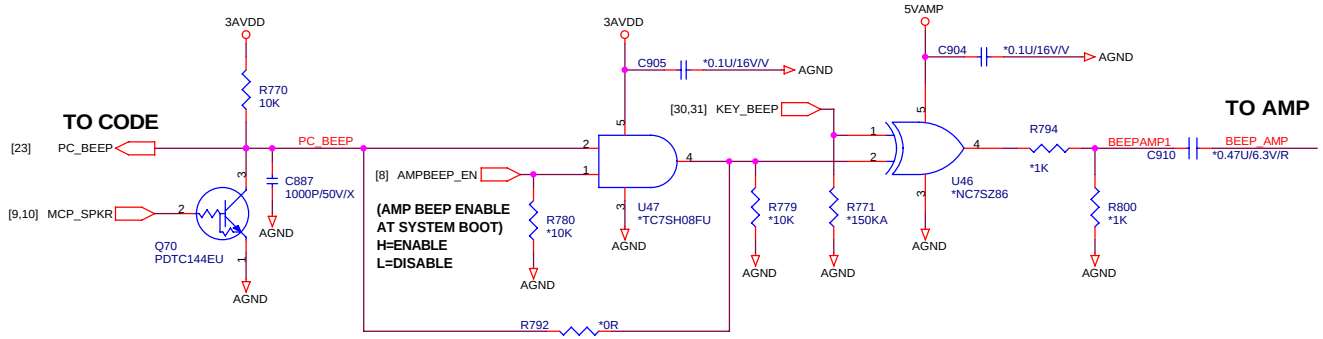
GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	**0**	**0**	**15.6dB**
1	1	0	21.6dB
x	x	1	4.1dB



INT. SPEAKER



PCSPK BEEP



3AVDD [23]
5V [13,18,19,22,23,26,27,28,29,31,32,33,36,38]

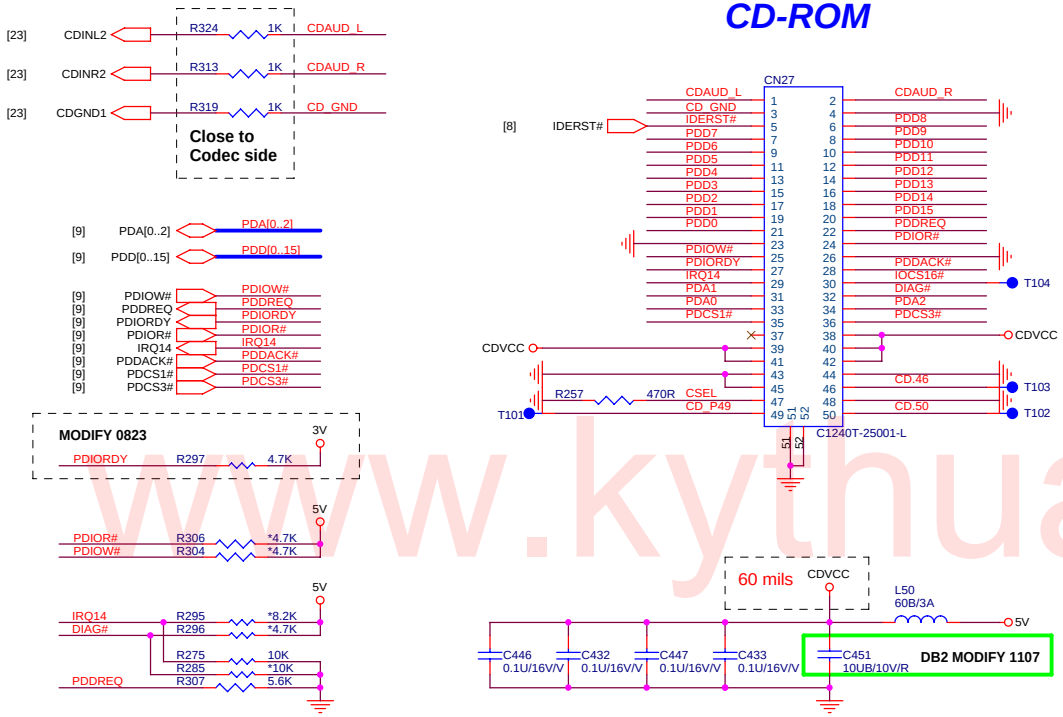
PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMP_TPA0312	C2A

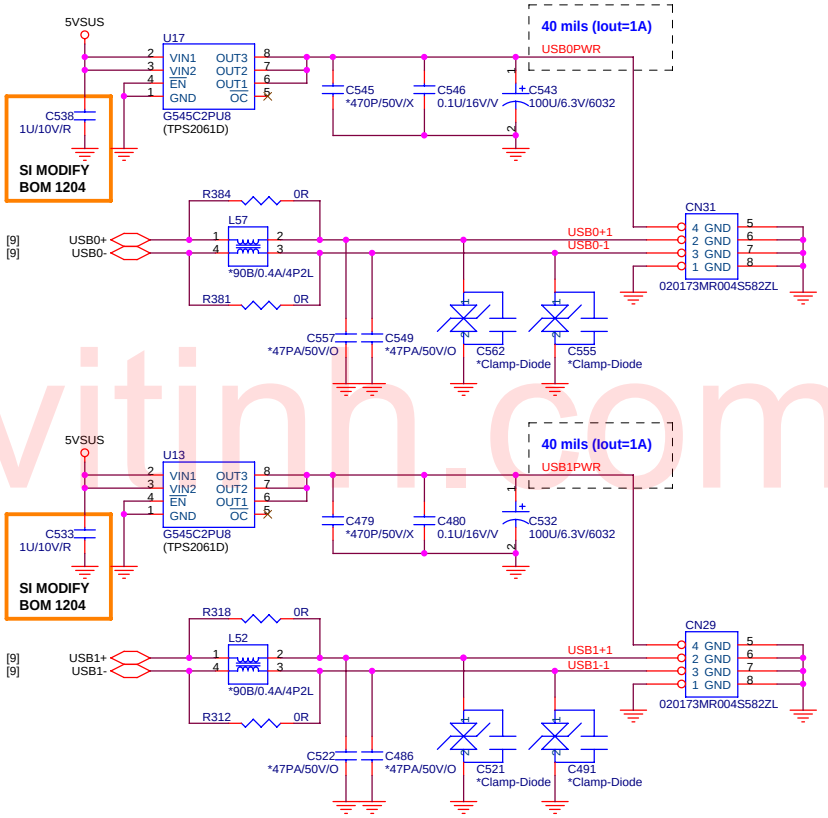
NB5/RD2/HW1

Date: Friday, December 29, 2006 Sheet 25 of 40

CD-ROM

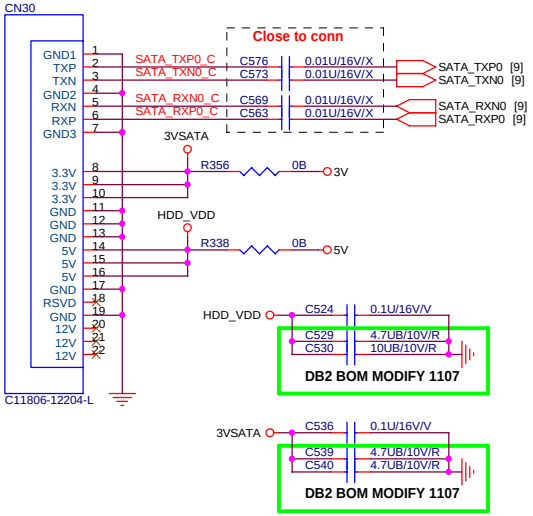


USB DIP CONNECTOR X 2

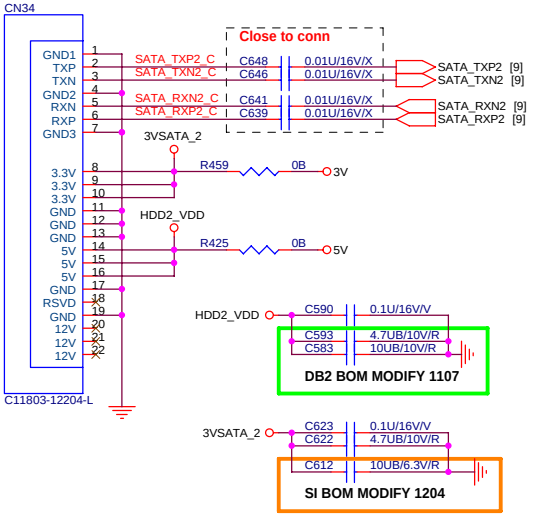


For 17"W Second HDD

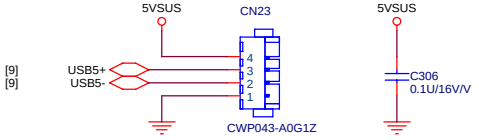
SATA_1 CONNECTOR



SATA_2 CONNECTOR



USB WIRE TO DC BOARD X 1



3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,27,28,29,30,31,32,33,36,38]
5VSUS [18,28,30,31,32,33,37]
5V [13,18,19,22,23,25,27,28,29,31,32,33,36,38]

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDDx2,CD-ROM,USBx3	C2A

NB5/RD2/HW1

Date: Friday, December 29, 2006 Sheet 26 of 40

Mini PCI-E Card 1
WLAN

1) Pins 39, 41 should be 3V
2) Pins 37, 43 should be GND

CN36

DB2 MODIFY

MODIFY FOR EMI SOLUTION 0911

FOR 15.4" ONLY

SW3 *NSS508-012N-AAAD1B-A

Q65 2N7002E

Q62 2N7002E

Q64 PDTC144EU

Mini PCI-E Card 2
(WWAN/SIM)
FOR 15.4" ONLY (RESERVE)

No need to stuff.

U40

(To GPIO pin)

SI BOM MODIFY 1213

FOR KBC DEBUG

CN37

DB2 MODIFY FORWLAN

FOR 17" SW BOARD

SI MODIFY 1213 FOR WLAN

U39 *CM1213_04ST

CN35 *CFS064-A0G16

D47 *BAV99W

Q61 *PDTC144EU

Q66 *PDTC144EU

*1827680-1
67910-0002

1.5V	[28,31,32,36]
3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,28,29,30,31,32,33,36,38]
3VSUS	[28,29,32,33]
5V	[13,18,19,22,23,25,26,28,29,31,32,33,36,38]

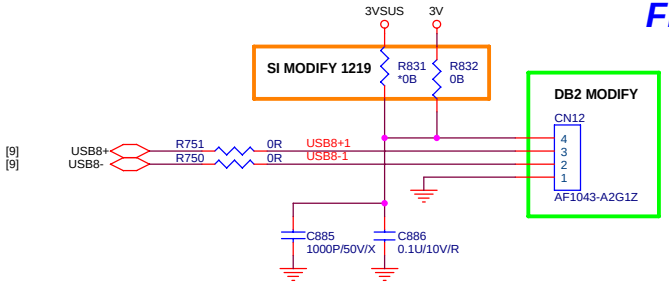
NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

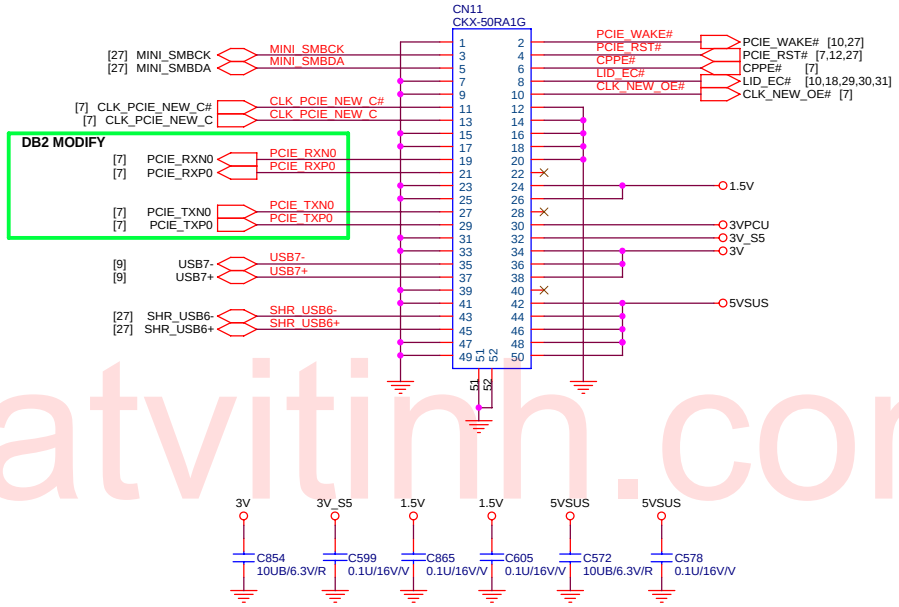
Size	Document Number	Rev
Custom	MINI CARDx2 (WLAN,WWAN,SIM)	C2A

Date: Friday, December 29, 2006 | Sheet 27 of 40

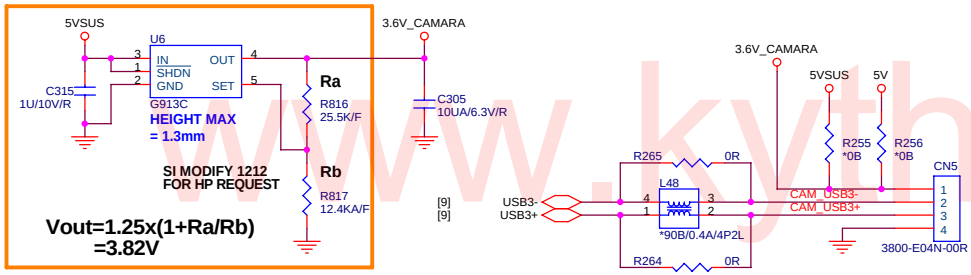
FINGER PRINT



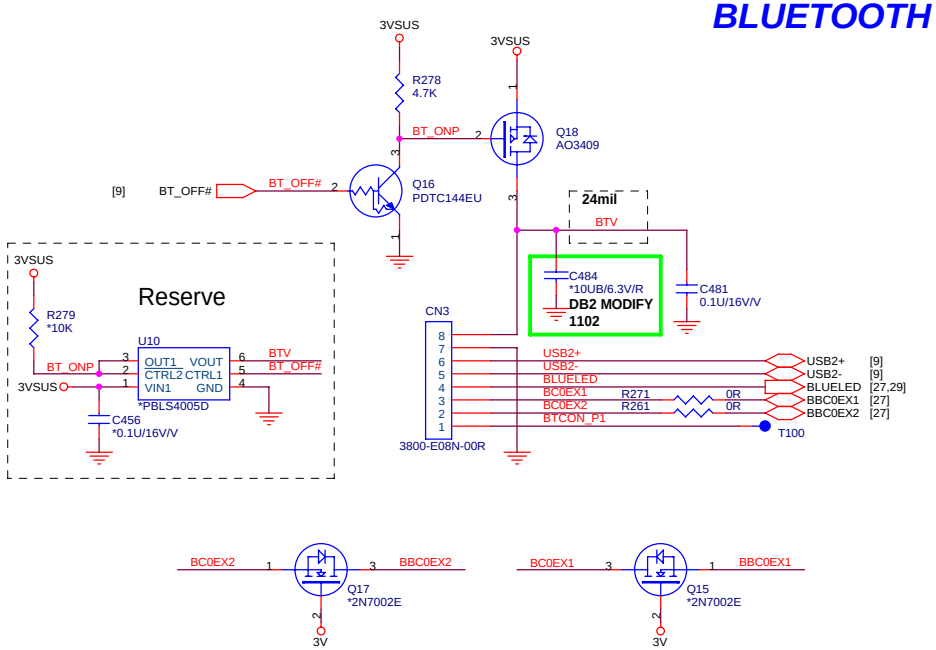
NEW CARD



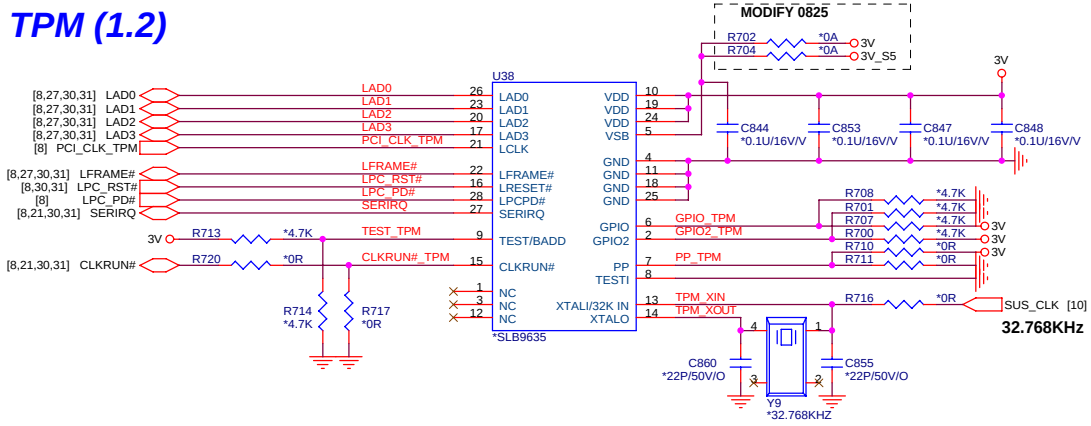
CAMERA

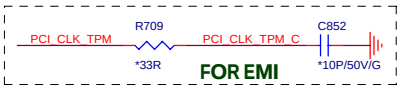


BLUETOOTH



TPM (1.2)





Address

	BADD
HIGH	4EH/4F (dafault)
LOW	2EH/2FH

*** DEFAULT**

PP (PHYSICAL PRESENCE)	
*L	PLATFORM PROTECT
H	USER ACCESS

1.5V	[27,31,32,36]
3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,29,30,31,32,33,36,38]
3VSUS	[27,29,32,33]
3V_S5	[8,9,10,11,20,30,32,33,37]
3VPCU	[9,14,18,29,30,31,33,34,35]
5V	[13,18,19,22,23,25,26,27,29,31,32,33,36,38]
5VSUS	[18,26,30,31,32,33,37]

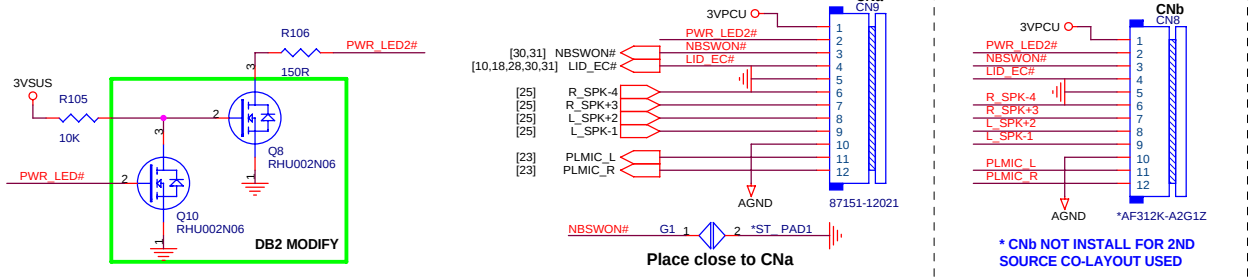
NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NEW CARD,CAMER,TPM,F/P,B/T	C2A

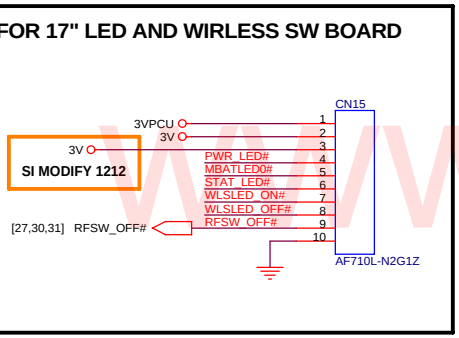
Date: Friday, December 29, 2006 Sheet 28 of 40

FOR POWER ON AND INTERNAL SPK / MIC SW BOARD

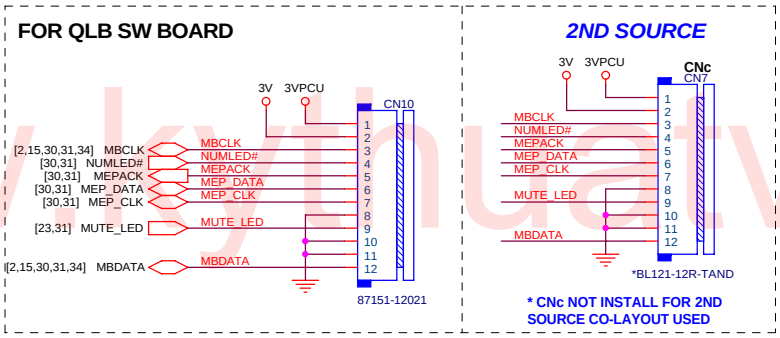


2ND SOURCE

FOR 17" LED AND WIRLESS SW BOARD

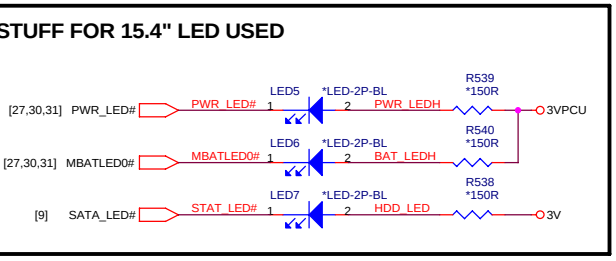


FOR QLB SW BOARD



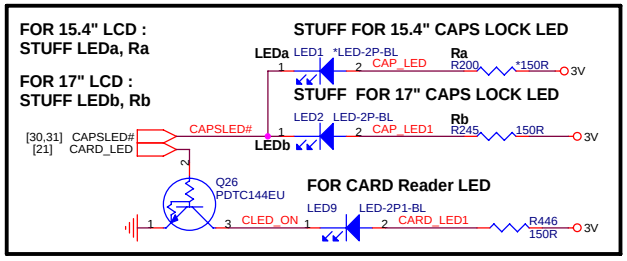
2ND SOURCE

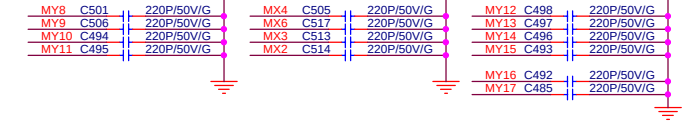
STUFF FOR 15.4" LED USED



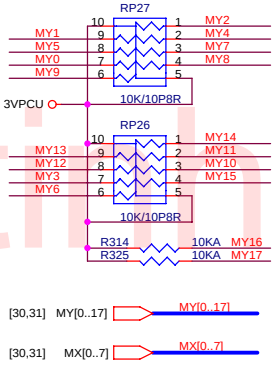
FOR 15.4" LCD : STUFF LEDa, Ra

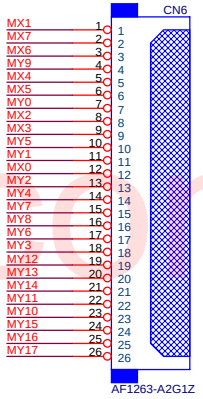
FOR 17" LCD : STUFF LEDb, Rb

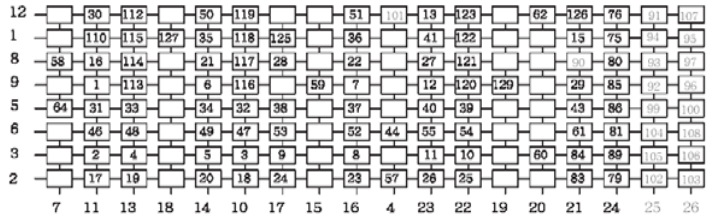


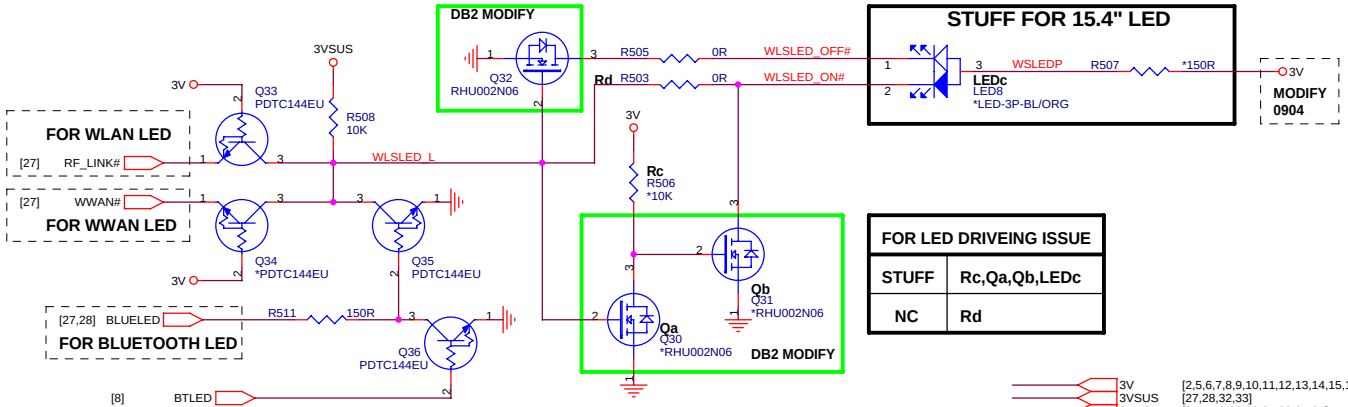


KEYBOARD PULL-UP



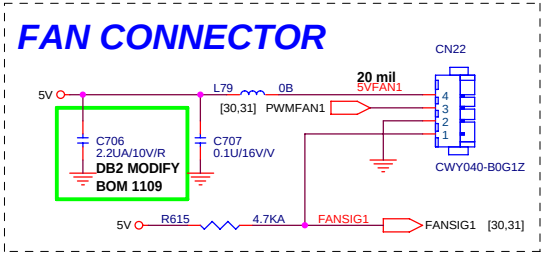






FOR LED DRIVEING ISSUE	
STUFF	Rc,Qa,Qb,LEDc
NC	Rd

FAN CONNECTOR



3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,30,31,32,33,36,38]
3VSUS	[27,28,32,33]
3VPCU	[9,14,18,28,30,31,33,34,35]
5V	[13,18,19,22,23,25,26,27,28,31,32,33,36,38]

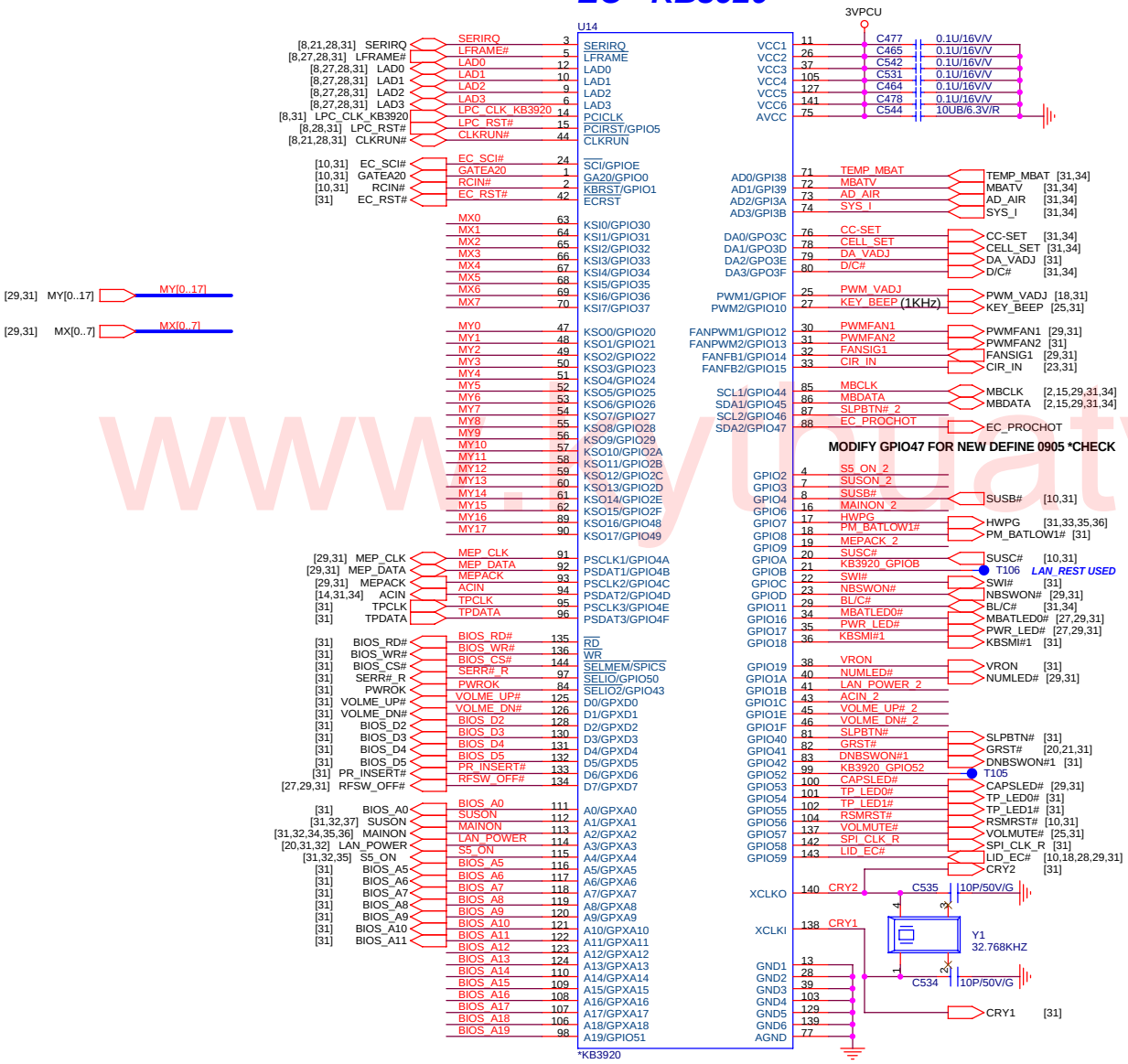
NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB,FAN,LED,SW (PWR,QLB,LED)	C2A

Date: Friday, December 29, 2006 Sheet 29 of 40

EC - KB3920

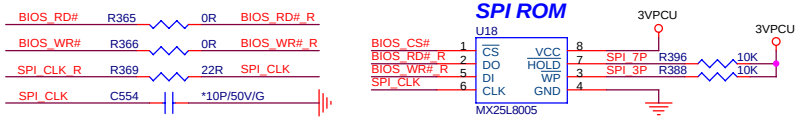


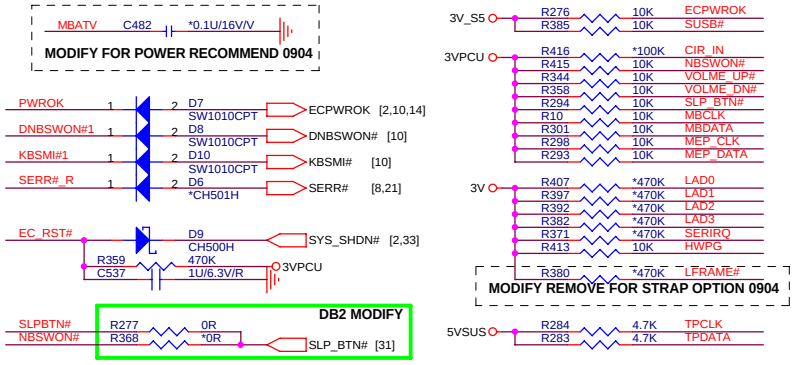
IF USED KB3920 : Ra stuff 0 ohm

IF USED KB3926 : Ra leave NC

STRAP PIN (*INTERNAL PULL-UP)

MY0	47	TP_TEST: Clock Test Mode Low: Test Mode. HIGH: *32kHz clock in normal runing	MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: *Boot from ISA flash part
MY1	48	TP_PLL: DPLL Test Mode Low: Test Mode. HIGH: *Normal operation	MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: *Normal Mode





3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,31,32,33,36,38]
3V_S5	[8,9,10,11,20,28,32,33,37]
3VPCU	[9,14,18,28,29,31,33,34,35]
5VSUS	[18,26,28,31,32,33,37]

PROJECT : AT1
Quanta Computer Inc.

NB5/RD2/HW1

Size	Document Number	Rev
Custom	KB3920,SPI_ROM	C2A

Date: Friday, December 29, 2006 Sheet 30 of 40

EC - KB3926

U15 — KB3926

[8,21,28,30] SERIRQ	SERIRQ	3	SERIRQ	VCC1	9
[8,27,28,30] LFRAME#	LFRAME#	4	LFRAME	VCC2	22
[8,27,28,30] LAD0	LAD0	10	LAD0	VCC3	33
[8,27,28,30] LAD1	LAD1	8	LAD1	VCC4	96
[8,27,28,30] LAD2	LAD2	7	LAD2	VCC5	111
[8,27,28,30] LAD3	LAD3	5	LAD3	VCC6	125
[8,30] LPC_CLK_KB3920	LPC_CLK_KB3920	12	PCICLK	AVCC	67
[8,28,30] LPC_RST#	LPC_RST#	13	PCIRST/GPIO5		
[8,21,28,30] CLKRUN#	CLKRUN#	38	CLKRUN		
[10,30] EC_SCI#	EC_SCI#	20	SCI/GPIOE		
[10,30] GATEA20	GATEA20	1	GA20/GPIO0		
[10,30] RCIN#	RCIN#	2	KBRST/GPIO1		
[30] EC_RST#	EC_RST#	37	ECRST		
	MX0	55	KSI0/GPIO30	AD0/GPI38	63
	MX1	56	KSI1/GPIO31	AD1/GPI39	64
	MX2	57	KSI2/GPIO32	AD2/GPI3A	65
	MX3	58	KSI3/GPIO33	AD3/GPI3B	66
	MX4	59	KSI4/GPIO34		
	MX5	60	KSI5/GPIO35		
	MX6	61	KSI6/GPIO36	PWM1/GPIOE	21
	MX7	62	KSI7/GPIO37	PWM2/GPIO10	23
	MY0	39	KSO0/GPIO20	FANPWM1/GPIO12	26
	MY1	40	KSO1/GPIO21	FANPWM2/GPIO13	27
	MY2	41	KSO2/GPIO22	FANFB1/GPIO14	28
	MY3	42	KSO3/GPIO23	FANFB2/GPIO15	29
	MY4	43	KSO4/GPIO24		
	MY5	44	KSO5/GPIO25	SCL1/GPIO44	77
	MY6	45	KSO6/GPIO26	SDA1/GPIO45	78
	MY7	46	KSO7/GPIO27	SCL2/GPIO46	79
	MY8	47	KSO8/GPIO28	SDA2/GPIO47	80
	MY9	48	KSO9/GPIO29		
	MY10	49	KSO10/GPIO2A		
	MY11	50	KSO11/GPIO2B		
	MY12	51	KSO12/GPIO2C		
	MY13	52	KSO13/GPIO2D		
	MY14	53	KSO14/GPIO2E	GPIO4	6
	MY15	54	KSO15/GPIO2F	GPIO7	14
	MY16	81	KSO16/GPIO48	GPIO8	15
	MY17	82	KSO17/GPIO49		
[29,30] MEP_CLK	MEP_CLK	83	PSCLK1/GPIO4A	GPIOA	16
[29,30] MEP_DATA	MEP_DATA	84	PSDAT1/GPIO4B	GPIOB	17
[29,30] MEPACK	MEPACK	85	PSCLK2/GPIO4C	GPIOC	18
[14,30,34] ACIN	ACIN	86	PSDAT2/GPIO4D	GPIOD	19
[30] TPCLK	TPCLK	87	PSCLK3/GPIO4E	GPIO11	25
[30] TPDATA	TPDATA	88	PSDAT3/GPIO4F	GPIO16	30
				GPIO17	31
				GPIO18	32
[30] BIOS_RD#	BIOS_RD#	119	RD	GPIO19	34
[30] BIOS_WR#	BIOS_WR#	120	WR	GPIO1A	36
[30] BIOS_CS#	BIOS_CS#	128	SELMEM/SPICS		
[30] SERR#_R	SERR#_R	89	SELIO/GPIO50		
[30] PWROK	PWROK	76	SELIO2/GPIO43		
[30] VOLME_UP#	VOLME_UP#	109	D0/GPXD0		
[30] VOLME_DN#	VOLME_DN#	110	D1/GPXD1		
[30] BIOS_D2	BIOS_D2	112	D2/GPXD2		
[30] BIOS_D3	BIOS_D3	114	D3/GPXD3	GPIO40	73
[30] BIOS_D4	BIOS_D4	115	D4/GPXD4	GPIO41	74
[30] BIOS_D5	BIOS_D5	116	D5/GPXD5	GPIO42	75
[30] PR_INSERT#	PR_INSERT#	117	D6/GPXD6	GPIO52	90
[27,29,30] RFSW_OFF#	RFSW_OFF#	118	D7/GPXD7	GPIO53	91
				GPIO54	92
[30] BIOS_A0	BIOS_A0	97	A0/GPXA0	GPIO55	93
[30,32,37] SUSON	SUSON	98	A1/GPXA1	GPIO56	95
[30,32,34,35,36] MAINON	MAINON	99	A2/GPXA2	GPIO57	121
[20,30,32] LAN_POWER	LAN_POWER	100	A3/GPXA3	GPIO58	126
[30,32,35] S5_ON	S5_ON	101	A4/GPXA4	GPIO59	127
[30] BIOS_A5	BIOS_A5	102	A5/GPXA5		
[30] BIOS_A6	BIOS_A6	103	A6/GPXA6		
[30] BIOS_A7	BIOS_A7	104	A7/GPXA7		
[30] BIOS_A8	BIOS_A8	105	A8/GPXA8		
[30] BIOS_A9	BIOS_A9	106	A9/GPXA9		
[30] BIOS_A10	BIOS_A10	107	A10/GPXA10	XCLKO	123
[30] BIOS_A11	BIOS_A11	108	A11/GPXA11	XCLKI	122
				GND1	11
				GND2	24
				GND3	35
				GND4	94
				GND5	113
T108	KB3926_V18R	124	V18R	AGND	69

TEMP_MBAT	TEMP_MBAT [30,34]		
MBATV	MBATV [30,34]		
AD_AIR	AD_AIR [30,34]		
SYS_I	SYS_I [30,34]		
CC-SET	CC-SET [30,34]		
CELL_SET	CELL_SET [30,34]		
DA_VADJ	DA_VADJ [30]		
D/C#	D/C# [30,34]		
PWM_VADJ	PWM_VADJ [18,30]		
KEY_BEEP (1KHz)	KEY_BEEP [25,30]		
PWMFAN1	PWMFAN1 [29,30]		
PWMFAN2	PWMFAN2 [30]		
FANSIG1	FANSIG1 [29,30]		
CIR_IN	CIR_IN [23,30]		
MBCLK	MBCLK [2,15,29,30,34]		
MBDATA	MBDATA [2,15,29,30,34]		
PR_INSERT#_2	PR_INSERT#_2 [30]		
EC_PROCHOT#	EC_PROCHOT# [2]		
SUSB#	SUSB# [10,30]		
HWPG	HWPG [30,33,35,36]		
PM_BATLOW1#	PM_BATLOW1# [30]		
SUSC#	SUSC# [10,30]		
KB3926_GPIOB	T107		
SWI#	SWI# [30]		
NBSWON#	NBSWON# [29,30]		
BL/C#	BL/C# [30,34]		
MBATLED0#	MBATLED0# [27,29,30]		
PWR_LED#	PWR_LED# [27,29,30]		
KBSMI#1	KBSMI#1 [30]		
VRON	VRON [30]		
NUMLED#	NUMLED# [29,30]		
SLPBTN#	SLPBTN# [30]		
GRST#	GRST# [20,21,30]		
DNBSWON#1	DNBSWON#1 [30]		
KB3926_GPIO52	T109		
CAPSLED#	CAPSLED# [29,30]		
TP_LED0#	TP_LED0# [30]		
TP_LED1#	TP_LED1# [30]		
RSMRST#	RSMRST# [10,30]		
VOLMUTE#	VOLMUTE# [25,30]		
SPI_CLK_R	SPI_CLK_R [30]		
LID_EC#	LID_EC# [10,18,28,29,30]		
CRY2	[30]		
CRY1	[30]		

MODIFY GPIO46,47 FOR NEW DEFINE 0905 *CHECK

SPI H/W STRAPPING

BIOS_A0 R315 1K

DB2 MODIFY 1101

[29,30] MY[0..17]

[29,30] MX[0..7]

LPC_CLK_KB3920 R421 *0R LPC_CLK_KB3920_C C579 *10P/50V/G

MODIFY FOR EMI SOLUTION 0911

TOUCH PAD CONNECTOR

SW1 MX4 MY7 *TACT-SWITCH

(Amber) LED3 TP_LED0# TPLD1 *150R R342 3V

TP_LED1# TPLD2 *150R R341 3V (Blue)

*LED-4P-BL/ORG

FOR 15.4"

SW2 MX4 MY7 TACT-SWITCH

(Amber) LED4 TP_LED0# TPLD3 150R R402 3V

TP_LED1# TPLD4 150R R412 3V (Blue)

LED-4P-BL/ORG

FOR 17"

5VSUS L36 80A/0.6A L37 220A/0.2A L38 220A/0.2A

TPCLK TPCLK-1

TPDATA TPDATA-1

C403 0.1U/16V/V

25 mils 5VTP

CN4 AF1043-A2G1Z

C404 *10P/50V/G C405 *10P/50V/G

CABLE DOCK

CN21 — QL1122L-H212CR-7F-44P

DB2 MODIFY 1107 FOR EMI SOLUTION

[19] CRT_G1	CRT_G1	R36	120/0.5A	CRT_GDK	38	
[19] CRT_R1	CRT_R1	R32	120/0.5A	CRT_RDK	40	
[6,13,19] DDCDAT	DDCDAT	R51	0R	DDAT_DK	34	
[19] CRT_B1	CRT_B1	R40	120/0.5A	CRT_BDK	36	
[19] HSYNC2	HSYNC2	R25	0R	HSY_DK	30	
[6,13,19] DDCCLK	DDCCLK	R53	0R	DCLK_DK	32	
				USB4-1	26	
[19] VSYNC2	VSYNC2	R26	0R	VSY_DK	28	
				USB4+1	22	
[20] +LAN_MX3	+LAN_MX3				24	
[20] -LAN_MX3	-LAN_MX3				18	
[20] +LAN_MX2	+LAN_MX2				20	
[20] -LAN_MX2	-LAN_MX2				14	
[20] +LAN_MX1	+LAN_MX1				16	
[20] -LAN_MX1	-LAN_MX1				10	
[20] +LAN_MX0	+LAN_MX0				12	
[20] -LAN_MX0	-LAN_MX0				6	
					8	
VIN					2	
					4	
				VSS	42	
				VSS	46	

VA_P	VDD	44	VDD	43	VA_P
		39			
TV_LUMA [19]	SYD_DK R566 0R TV_LUMA	37			
TV_CHROMA [19]	SCD_DK R567 0R TV_CHROMA	35			
TV_COMP [19]	SCVBS_DK R570 0R TV_COMP	33			
	VIDEO_GND R576 0R	31			
CIR_IN [23,30]	CIRIN_DK R578 0R CIR_IN	29			
	PWR_ON	27			
MUTE_LED [23,29]	MUTE_LED	25			
SLP_BTN# [30]	SLP_BTN#	23			
JACK_DETECT# [23]	JACK_DETECT#	21			
VOLME_UP# [30]	VOLME_UP#	19			
VOLME_DN# [30]	VOLME_DN#	17			
	SPDIF_DOCK	15			
AGND	AUDIO_G R606 0R	13			
	RSPK_DK	11			
	LSPK_DK	9			
DOCK_MIC_R [23]	RMIC_DK R588 0R	7			
DOCK_MIC_L [23]	LMIC_DK R599 0R	5			
AGND	MIC_GND R597 0R	3			
	DOCK_PRESENT	1			
		41	VSS	41	
		45	VSS	45	

SPDIF	C723	*270P/25V/O	
JACK_DETECT#	C713	270P/25V/O	
CIR_IN	C710	*120P/50V/O	
VOLME_DN#	C716	*120P/50V/O	

DB2 MODIFY 1030 FOR POWER RECOMMEND

VA L89 0.015B/4A L73 0.015B/4A

150 mils VA_P

C681 0.1U/25V/V C682 0.1U/25V/V MODIFY 0831

5VSUS R582 1K DK_PWRON D40 SW1010CPT D39 SW1010CPT 5V

DB2 MODIFY 1106

R60 1.5K/F PWR_ON

S0: 4V S3: 2.5V S4/S5: 0V

*Check voltage on DB

3VPCU R595 *100K

[30] PR_INSERT# R600 *0R PR_INSERT_L#

DOCK_PRESENT R598 1K DKPR# Q50 *MMBT3904

R602 2KA/F

1.5V R587 33R SPDDK_V SPD_DK L80 0A SPDIF_DOCK

Q49 MMBT3904

[12,23] SPDIF SPDIF R591 510/F SPDIF_DK R589 510/F C722 68P/50V/G

RSPK_DK R67 *0R C107 100U/6.3V/3528 DOCK_RSPK+ [23]

LSPK_DK C142 100U/6.3V/3528 DOCK_LSPK+ [23]

R81 *0R

[9] USB4- [9] USB4+ R61 0R L8 *90B/0.33A/4P2L R66 0R USB4-1 USB4+1

RESERVE FOR EMI SOULTION

TV_LUMA	C55	*82P/50V/O	RSPK_DK	C104	*10P/50V/G
TV_CHROMA	C64	*82P/50V/O	LSPK_DK	C116	*10P/50V/G
TV_COMP	C70	*82P/50V/O	RMIC_DK	C721	*10P/50V/G
SYD_DK	C685	*82P/50V/O	LMIC_DK	C725	*10P/50V/G
SCD_DK	C690	*82P/50V/O			
SCVBS_DK	C699	*82P/50V/O			
CRT_GDK	C36	*10P/50V/G	USB4+1	C95	*10P/50V/G
CRT_RDK	C33	*10P/50V/G	USB4-1	C88	*10P/50V/G
CRT_BDK	C57	*10P/50V/G			
CRT_G1	C37	*10P/50V/G	+LAN_MX0	C762	*10P/50V/G
CRT_R1	C32	*10P/50V/G	-LAN_MX0	C766	*10P/50V/G
CRT_B1	C46	*10P/50V/G	+LAN_MX1	C125	*10P/50V/G
HSY_DK	C31	*10P/50V/G	-LAN_MX1	C117	*10P/50V/G
VSY_DK	C87	*10P/50V/G	+LAN_MX2	C281	*10P/50V/G
DDAT_DK	C65	*10P/50V/G	-LAN_MX2	C294	*10P/50V/G
DCLK_DK	C85	*10P/50V/G	+LAN_MX3	C786	*10P/50V/G
			-LAN_MX3	C788	*10P/50V/G

1.5V	[27,28,32,36]
3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,32,33,36,38]
3VPCU	[9,14,18,28,29,30,33,34,35]
5VSUS	[18,26,28,30,32,33,37]
5V	[13,18,19,22,23,25,26,27,28,29,32,33,36,38]
VA	[34]
VIN	[18,32,33,34,35,36,37,38]

NB5/RD2/HW1

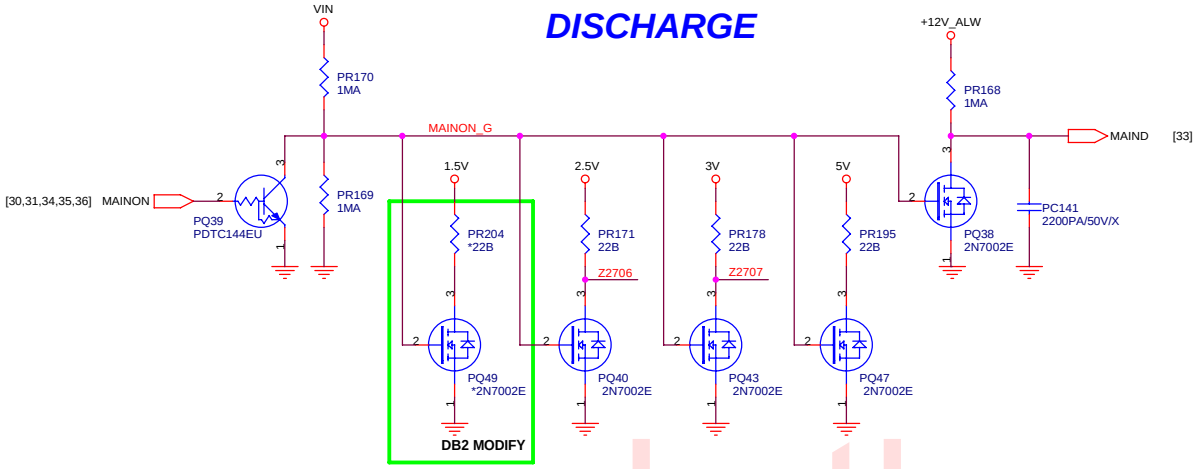
PROJECT : AT1

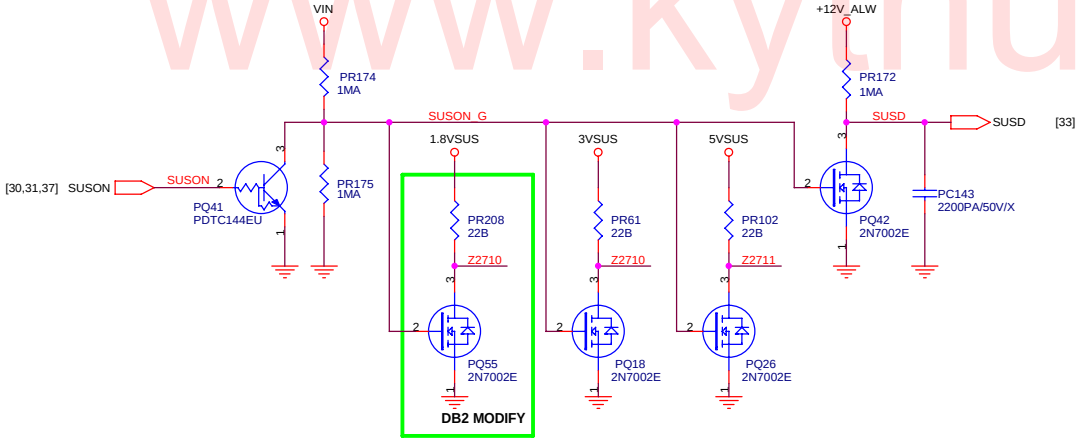
Quanta Computer Inc.

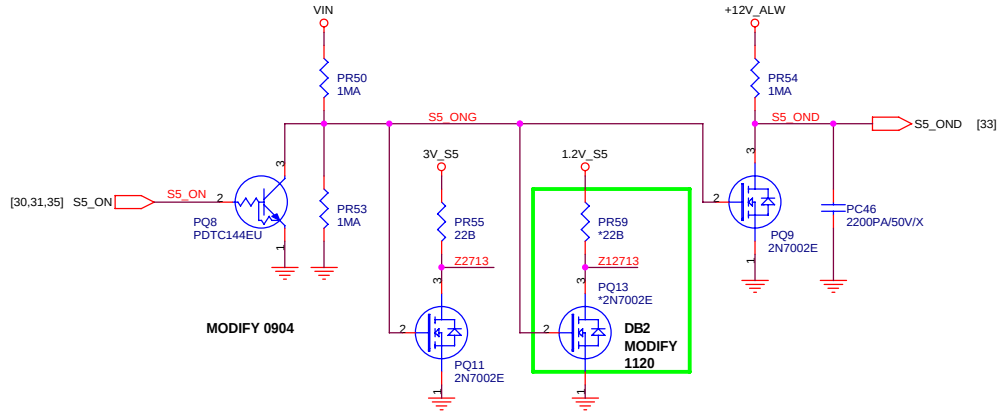
Size	Document Number	Rev
Custom	KB3926,DOCKING,TOUCH_PAD	C2A

Date: Friday, December 29, 2006 Sheet 31 of 40

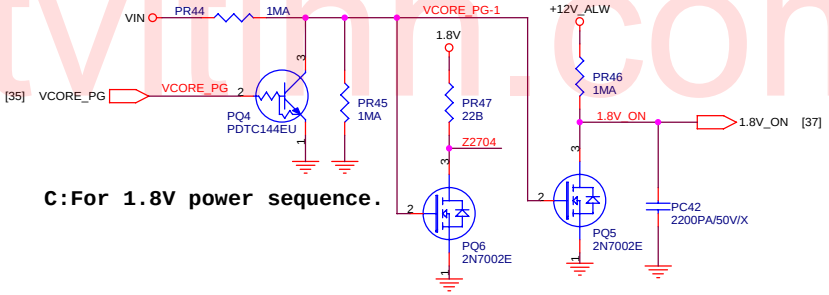
DISCHARGE



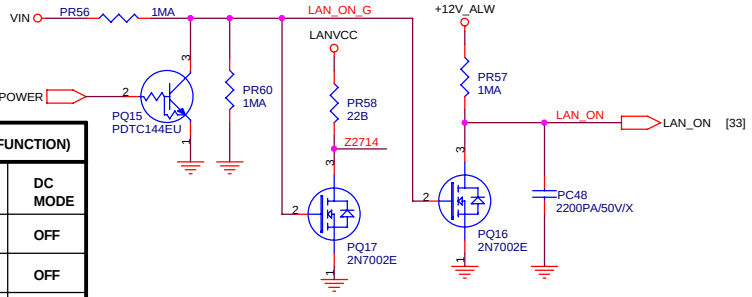




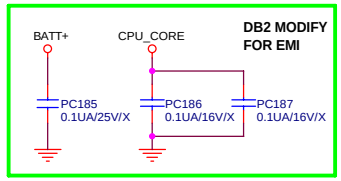
SI POWER MODIFY



C:For 1.8V power sequence.



LAN_POWER (WOL FUNCTION)		
POWER STATES	AC MODE	DC MODE
S4 / S5	OFF	OFF
S3	ON	OFF
S0	ON	ON



CPU_CORE	[4,38]
1.2V_S5	[10,11,35]
1.5V	[27,28,31,36]
1.8V	[11,13,15,16,17,37]
1.8VSUS	[2,3,4,5,6,36,37]
2.5V	[2,13,36]
LANVCC	[20,33]
3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,33,36,38]
3VSUS	[27,28,29,33]
3V_S5	[8,9,10,11,20,28,30,33,37]
5V	[13,18,19,22,23,25,26,27,28,29,31,33,36,38]
5VSUS	[18,26,28,30,31,33,37]
+12V_ALW	[10,18,33]
VIN	[18,31,33,34,35,36,37,38]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE	C2A
Date: Friday, December 29, 2006	Sheet 32 of 40	

DC/DC 3VPCU/ 5VPCU/ +12V_ALW

TOPN: OUT1/OUT2
GND=400KHz/500KHz
REF = 400KHz /300KHz
VCC5=200KHz/300KHz

5 Volt +/- 5%
5VPCU
C/C:8A
P/C:10A

Vout=0.7(Ra+Rb)/Rb
Rb around 49.9k

3.3 Volt +/- 5%
3VPCU
C/C:8A
P/C:10A

Place these CAPs close to FETs

Place these CAPs close to FETs

I_lim*MOSFET(RDSON)=V_ILIM(mV)/10
V_ILIM(mV)=5uA*R_ILIM

DB2 MODIFY

DB2 MODIFY

Rds(on) 13m ohm

Rds(on) 13m ohm

1A
S0-S5

1.6A
S0-S3

4.59A
S0-S1

5A
S0-S3

LANVCC
0.2A

3V
9.0A
S0-S1

+12V_ALW	[10,18,32]
LANVCC	[20,32]
3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,36,38]
3VSUS	[27,28,29,32]
3V_S5	[8,9,10,11,20,28,30,32,37]
3VPCU	[9,14,18,28,29,30,31,34,35]
5V	[13,18,19,22,23,25,26,27,28,29,31,32,36,38]
5VSUS	[18,26,28,30,31,32,37]
5VPCU	[10,23,34,35,36,37,38]
VIN	[18,31,32,34,35,36,37,38]

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ISL6236 (5VPCU,3VPCU)	C2A
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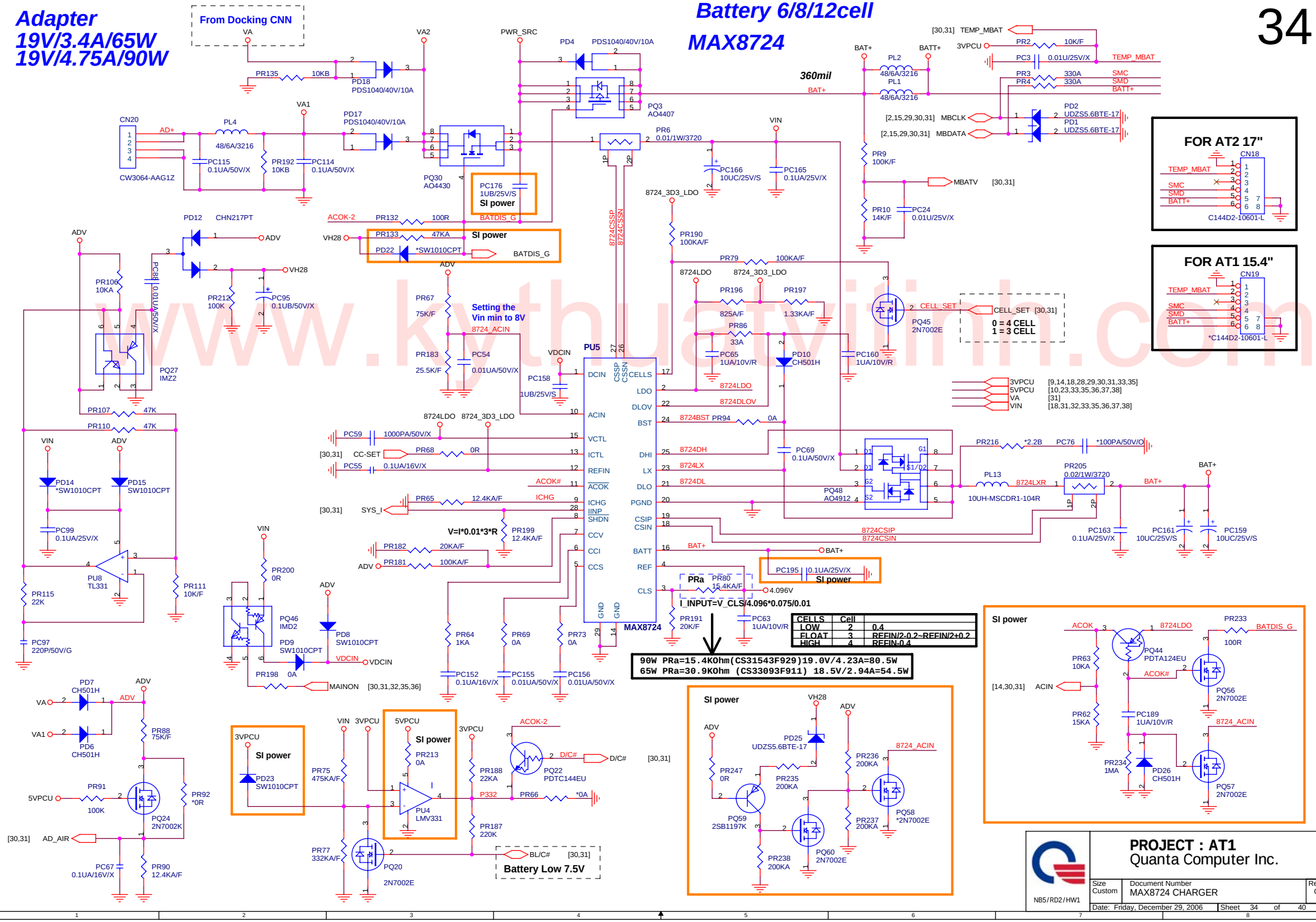
NB5/RD2/HW1

Adapter
19V/3.4A/65W
19V/4.75A/90W

Battery 6/8/12cell
MAX8724

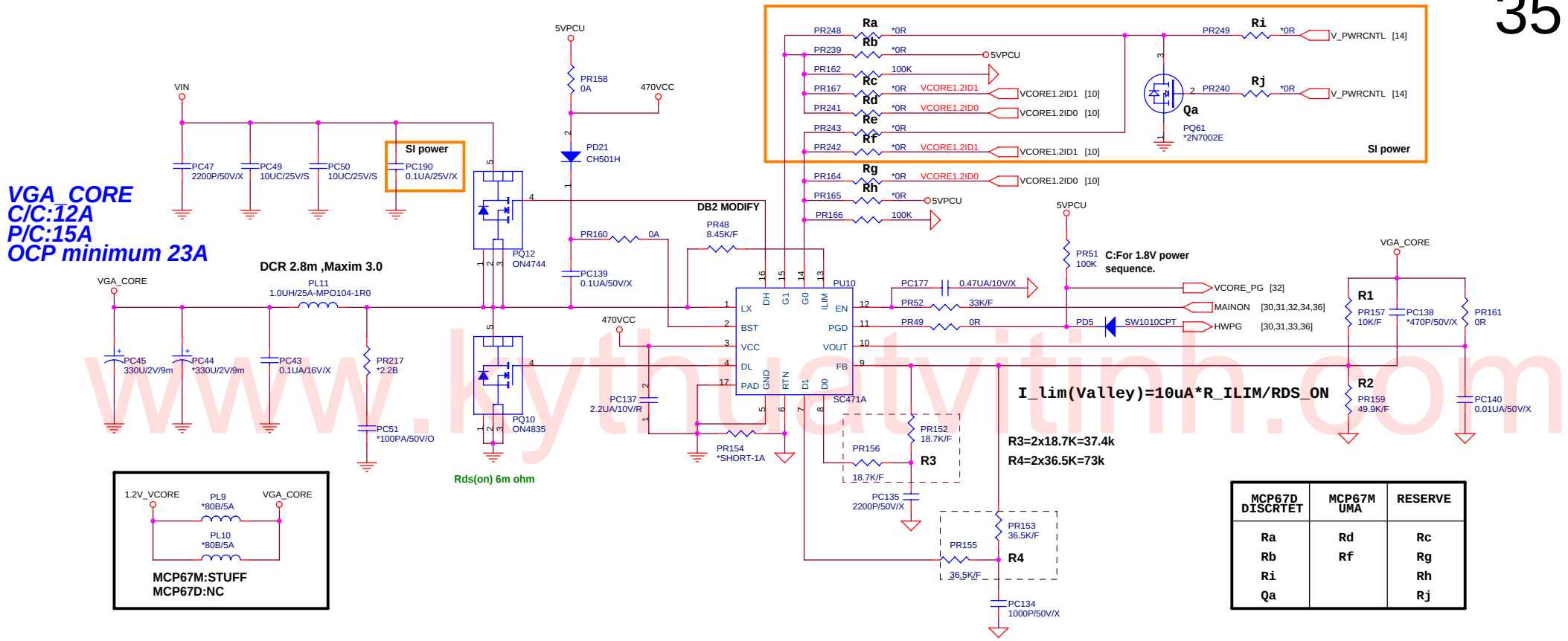


NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MAX8724 CHARGER	C2A

Date: Friday, December 29, 2006 Sheet 34 of 40



MCP67D DISCRTET	MCP67M UMA	RESERVE
Ra	Rd	Rc
Rb	Rf	Rg
Ri		Rh
Qa		Rj

INPUTS		OUTPUTS			VGA_CORE
G0	G1	OD1	OD2	OD3	
0	0	0.75x(1+R1/R2+R1/R3+R1/R4)			1.2V
0	1	0.75x(1+R1/R2+R1/R3)			1.1V
1	0	0.75x(1+R1/R2+R1/R4)			1.0V
1	1	0.75x(1+R1/R2)			0.9V

GFX_VID0
H: Normal Voltage
L: Low Voltage

VGACORECTL	NB8X	R2	R3/PR294	PR1293/PR295
HI	1.2V	CS43012FB10	NA	Mounted
LO	1.XV			

1.2V_S5 [10,11,32]
1.2V_VCORE [11,36]
VGA_CORE [12]
3VPCU [9,14,18,28,29,30,31,33,34]
5VPCU [10,23,33,34,36,37,38]
VIN [18,31,32,33,34,36,37,38]

PROJECT : AT1
Quanta Computer Inc.

NB5/RD2/HW1

Size	Document Number	Rev
Custom	SC471A (VGA_CORE),1.2V_S5	C2A

Date: Friday, December 29, 2006 Sheet 35 of 40

MAX1992

S0-S1

1.2V
C/C:6A
P/C:8A
OCP minimum 10A

DCR 14m ,Maxim 15mohm

MODIFY 0825
1.2V_VCORE — PL7 80B/5A — 1.2V
PL6 80B/5A
MCP67M:NC
MCP67D:STUFF

Vout=0.7V(1+Ra/Rb)

Vcs=I_L(A)*L_DCR(mOHM)=V_ILIM(mV)/10

1.5A
S0-S1

SI POWER — 5V — PR186 10K — EN_G966
[30,31,33,35] HWPG — PR189 *0R
PU12 G966 (POK, VEN, VIN, VPP, GND, ADJ, VO, NC)
1.8VSUS
PC153 *0.1UA/16V/X
PC151 10UB/6.3V/R
PC154 0.1UA/16V/X
PC157 0.1UA/16V/X
R1 PR201 88.7K/F
R2 PR203 100K/A/F
PC170 10UB/6.3V/R
PC168 0.1UA/16V/X
1.5V

Vo=0.8(R1+R2)/R2
R2<120Kohm

SI power
3V — PU13 G913C (VIN, VOUT, SHDN, GND, SET) — 2.5V
PC191 1UA/10V/R
PR244 10K
R1 PR245 100K/F
R2 PR246 100K/F
PC192 4.7UB/10V/R

2.5V
0.1A
S0-S1

Vout=1.25(1+R1/R2)

1.2V_VCORE [11,35]
1.2V [10,11,12,13,15]
1.5V [27,28,31,32]
1.8VSUS [2,3,4,5,6,32,37]
2.5V [2,13,32]
3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,38]
5V [13,18,19,22,23,25,26,27,28,29,31,32,33,38]
5VPCU [10,23,33,34,35,37,38]
VIN [18,31,32,33,34,35,37,38]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MAX1992 (1.2V),1.5V,2.5V	C2A

Date: Friday, December 29, 2006 Sheet 36 of 40

S0-S3

1.8VSUS
C/C:12A
P/C:15.2A
OCP minimum 25A

1.8 Volt +/-5%

DCR 2.8m ,Maxim 3.0

Rds(on) 4.2m ohm

Ra=(Vout-0.75)/0.75*Rb

Rb value from 100K to 300K ohm

I_lim(Valley)=10uA*R_ILIM/RDS_ON

For OCP set.

S0-S3

SMDDR_VTERM
1.53A / 0.9V

SI MODIFY FOR POWER SEQUENCE 1211

0.9 Volt +/-5%
Design Current:1.5A
Maximum Current: 1.8A

Fix 1.8V Output

100pF for SC480

S0-S3

SMDDR_VTERM
0.9V
?A

0.9V/1.2A

*TPS51100DGQR

1.8V
4.75A

S0-S1

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

V_TRIP(mV)=R_TRIP(Kohm)*10(uA)

I_OCP=V_trip/Rds_on+I_Ripple/2

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	V_ vddqsns/2	DDR
V5IN	1.8	V _vddqsns/2	DDR2
FB	adjustable	V_VDDQSNS/2	1.5V<VDDQ<3V

SMDDR_VTERM [4]
1.8V [11,13,15,16,17,32]
1.8VSUS [2,3,4,5,6,32,36]
3V_S5 [8,9,10,11,20,28,30,32,33]
5VSUS [18,26,28,30,31,32,33]
5VPCU [10,23,33,34,35,36,38]
VIN [18,31,32,33,34,35,36,38]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	TI51116 (1.8VSUS,VTER),1.8V	C2A

Date: Friday, December 29, 2006 Sheet 37 of 40

CPU_CORE MAX8774

Slew rate=(12.5mVus)*(71.5K/R_TIME)
VFB=V_VID+0.125(VREF-VOFS)
VRHOT is low when VTHRM below 1.5V
Tsw=16.26pF(R_TON+6.5K)ohm
CCV CAP=470pF*(2/total phase)*300kHZ/fsw

TON=200K Ohm/ 300K Hz

D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.5500V
0	0	0	0	0	1	1.5250V
0	0	0	0	1	0	1.5000V
0	0	0	0	1	1	1.4750V
0	0	0	1	0	0	1.4500V
0	0	0	1	0	1	1.4250V
0	0	0	1	1	0	1.4000V
0	0	0	1	1	1	1.3750V
0	0	1	0	0	0	1.3500V
0	0	1	0	0	1	1.3250V
0	0	1	0	1	0	1.3000V
0	0	1	0	1	1	1.2750V
0	0	1	1	0	0	1.2500V
0	0	1	1	0	1	1.2250V
0	0	1	1	1	0	1.2000V
0	0	1	1	1	1	1.1750V
0	1	0	0	0	0	1.1500V
0	1	0	0	0	1	1.1250V
0	1	0	0	1	0	1.1000V
0	1	0	0	1	1	1.0750V
0	1	0	1	0	0	1.0500V
0	1	0	1	0	1	1.0250V
0	1	0	1	1	0	1.0000V
0	1	0	1	1	1	0.9750V
0	1	1	0	0	0	0.9500V
0	1	1	0	0	1	0.9250V
0	1	1	0	1	0	0.9000V
0	1	1	0	1	1	0.8750V
0	1	1	1	0	0	0.8500V
0	1	1	1	0	1	0.8250V
0	1	1	1	1	0	0.8000V
0	1	1	1	1	1	0.7750V

D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	0.7625V
1	0	0	0	0	1	0.7500V
1	0	0	0	1	0	0.7375V
1	0	0	0	1	1	0.7250V
1	0	0	1	0	0	0.7125V
1	0	0	1	0	1	0.7000V
1	0	0	1	1	0	0.6875V
1	0	0	1	1	1	0.6750V
1	0	1	0	0	0	0.6625V
1	0	1	0	0	1	0.6500V
1	0	1	0	1	0	0.6375V
1	0	1	0	1	1	0.6250V
1	0	1	1	0	0	0.6125V
1	0	1	1	0	1	0.6000V
1	0	1	1	1	0	0.5875V
1	0	1	1	1	1	0.5750V
1	1	0	0	0	0	0.5625V
1	1	0	0	0	1	0.5500V
1	1	0	0	1	0	0.5375V
1	1	0	0	1	1	0.5250V
1	1	0	1	0	0	0.5125V
1	1	0	1	0	1	0.5000V
1	1	0	1	1	0	0.4875V
1	1	0	1	1	1	0.4750V
1	1	1	0	0	0	0.4625V
1	1	1	0	0	1	0.4500V
1	1	1	0	1	0	0.4375V
1	1	1	0	1	1	0.4250V
1	1	1	1	0	0	0.4125V
1	1	1	1	0	1	0.4000V
1	1	1	1	1	0	0.3875V
1	1	1	1	1	1	0.3750V

DCR=1.1m/+-5%

CPU_CORE
C/C:35A
P/C:35A
OCP minimum 44A

DCR=1.1m/+-5%

SI MODIFY FOR POWER SEQUENCE 1211

DB2 BOM MODIFY 1108

DB2 MODIFY

CPU_CORE [4,32]
3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36]
5V [13,18,19,22,23,25,26,27,28,29,31,32,33,36]
5VPCU [10,23,33,34,35,36,37]
VIN [18,31,32,33,34,35,36,37]

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
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